PERENCANAAN DAN PEMBUATAN ALAT PENCATAT TEMPERATUR YANG DI ANTARMUKAKAN KE KOMPUTER MELALUI PORT LPT 1

SKRIPSI

Disusun dan diajukan sebagai salah satu syarat untuk memperoleh gelar sarjana Teknik Elektronika Strata-satu (S-1)

Disusun Oleh:

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FAKULTAS TEKNOLOGI INDUSTRI
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MALANG

2009

LEMBAR PERSETUJUAN

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PERENCANAAN DAN PEMBUATAN ALAT PENCATAT TEMPERATUR YANG DI ANTAR MUKAKAN KE KOMPUTER MELALUI PORT LPT 1

Abstrak

Makalah ini membahas perancangan sistem akuisisi data suhu yang menggunakan komponen-konponen dasar berupa sebuah sensor suhu, ADC dan komputer sebagai fasilitas penampil. Sistem akuisisi data suhu menjadi satu hal yang sangat penting dalam kegiatan perindustrian, karena merupakan sebagian kecil dari sebuah proses kontrol. Berkenaan dengan pentingnya sistem, maka dilakukan perancangan sistem akusisi data suhu yang mampu melakukan kegiatan monitoring suhu secara akurat.

Data yang akan diukur merupakan sebuah besaran fisis temperature sehingga untuk dapat diolah dan ditampilkan dalam bentuk sistem elektris digunakan sensor suhu LM35 yang mampu mengkonversi besaran tersebut dengan kenaikan 10mV/°C, dan sebuah thermocouple yang merupakan dua buah bahan konduktor yang berbeda dan berpasangan digunakan untuk mengkonversikan arus bolak balik atau arus searah menjadi tegangan dan dapat diukur melalui suatu alat ukur. Untuk dapat merancang sistem maka pertama kali dilakukan proses mengubah suhu menjadi tegangan analog menggunakan sensor suhu LM35 dan thermocouple. Setelah melalui proses pengkondisian sinyal dengan cara dikuatkan, tegangan analog diubah menjadi data digital menggunakan ADC 0804.

Data digital yang diperoleh kemudian diolah oleh Komputer dan ditampilkan di layar komputer, sehingga didapatkan suatu informasi mengenai suhu dengan satuan °C pada sebuah layar komputer.

***Kata kunci** : sistem akuisis data suhu, sensor suhu, ADC 0804*

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Puji syukur penulis panjatkan ke Hadirat Allah SWT atas Rahmat dan hidayah-Nya kepada penulis sehingga upaya penyusunan skripsi ini dapat terselesaikan dengan baik.

Penyusunan skripsi ini dimaksudkan untuk memenuhi syarat kelulusan program studi S1 Jurusan Teknik Elektro S-1 Konsentrasi Teknik Elektronika Fakultas Teknologi Industri Institut Teknologi Nasional Malang.

Selama dalam proses penyusunan skripsi ini penulis menyadari sekali hambatan-hambatan yang penulis hadapi, akan tetapi berkat bantuan dan bimbingan dari semua pihak sehingga skripsi ini dapat terselesaikan dengan baik. Pada kesempatan ini penulis mengucapkan terima kasih kepada :

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Malang, Maret 2009

Penulis

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BAB I

PENDAHULUAN

1.1 Latar Belakang

Kita mengenal suhu sebagai panas atau dingin. Jika suhu tinggi kita sebut panas dan sebaliknya jika suhu rendah maka kita menyebutnya dingin. Jadi suhu hanyalah suatu konsep intuisi untuk menyatakan suatu benda itu "panas" atau "dingin".

Dalam penjabaran prinsip kedua termodinamika, suhu dihubungkan dengan kalor (heat), karena diketahui bahwa kalor mengalir dari suhu tinggi ke suhu rendah. Dalam teori kinetik gas dan termodinamika statistik telah dibuktikan bahwa suhu berhubungan dengan energi kinetik rata-rata molekul gas ideal. Teori tersebut menunjukkan adanya hubungan antara suhu dan tingkat energi pada zat cair dan zat padat. Secara prinsip, konsep suhu ini penting dalam hampir semua cabang ilmu pengetahuan alam. Karena itu perlu adanya penguasaan dan pemahaman tentang metode-metode untuk pengukuran suhu (derajat panas atau dingin).

Sistem Instrumentasi yang berbentuk akuisisi data telah dipergunakan secara luas dalam kegiatan perindustrian, karena merupakan bagian dari proses kontrol. Pengukuran besaran fisis adalah salah satu langkah dalam akuisisi data. Temperatur merupakan salah satu besaran fisis yang sering dipakai dalam suatu sistem kontrol baik hanya untuk sistem monitoring saja atau untuk proses pengendalian lebih lanjut. Dalam kaitannya dengan hal tersebut, maka kami membuat sebuah alat pendeteksi suhu yang dapat di kontrol oleh sebuah komputer. Dengan menampilkan suatu hasil

pengukuran secara digital, pemantauan terhadap proses dapat dilakukan dengan lebih mudah.

Perancangan alat ini diharapkan memberi kontribusi yang cukup handal dalam membantu pencatatan temperatur suhu dan dapat dikembangkan untuk membantu di segala bidang yang berhubungan dengan temperatur, namun dibutuhkan desain, uji coba dan kajian yang nantinya dapat diimplementasikan dalam memenuhi kebutuhan akan perangkat elektronika yang dapat membantu perusahaan, masyarakat ataupun dunia pendidikan.

1.2 Tujuan

Tujuan dari perancangan ini adalah merancang suatu alat yang dapat membantu dan dapat digunakan dalam pencatatan temperatur secara otomatis dan memilih sensor yang akan digunakan kemudian di tampilkan pada layar komputer melalui port LPT1.

1.3 Rumusan Masalah

Mengacu pada permasalahan yang di uraikan pada latar belakang maka rumusan masalah di tekankan pada bagaimana merancang suatu alat akuisis data yang dapat di kontrol dengan menggunakan komputer melalui port LPT1.

1.4 Batasan Masalah

1 Sensor di batasi hanya 2 sensor yaitu sensor thermocople dan sensor LM 35

2 Rancangan sistem elektronika yang digunakan :

2.1 Relay dan Driver Relay

2.2 ADC 0804

Metodologi Penulisan

Metodologi penulisan yang dipakai dalam pembuatan skripsi ini.

1. Studi Literatur
2. Perancangan dan pembuatan alat
3. Pelaksanaan uji coba Alat
4. Penyusunan Laporan Skripsi

2.3 Sistematika Pembahasan

Penulisan skripsi ini terbagi dalam lima bab dengan sistematika sebagai berikut:

BAB I PENDAHULUAN

Berisi latar belakang tujuan, permasalahan, batasan masalah, metodologi, dan sistematika penulisan.

BAB II LANDASAN TEORI

Berisi tentang terori dasar tentang sensor L35, Thermocouple, penguat opamp,relay, driver relay dan ADC0804, teori tentang pemrograman DELPHI 6 dan teori dasar lainnya yang berhubungan dengan alat yang dibuat.

BAB III PERANCANGAN DAN PEMBUATAN ALAT

Membahas tentang perancangan alat baik perangkat keras maupun perangkat lunak, serta cara kerja blok diagram..

BAB IV ANALISA

Mencakup pembahasan tentang proses Analisa dan pengujian alat yang terdiri dari peralatan yang digunakan, langkah kerja alat yang di buat.

BAB V PENUTUP

Berisi kesimpulan – kesimpulan yang di dapat selama perencanaan dan pembuatan alat dan saran – saran.

BAB II

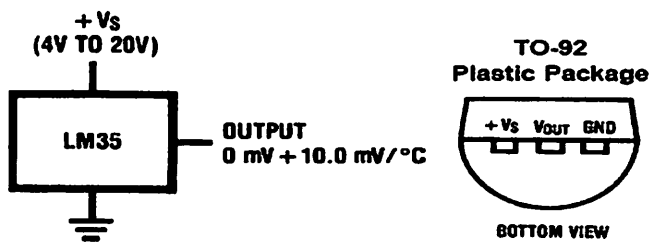
LANDASAN TEORI

2.1. SENSOR TEMPERATUR

2.1.1. SENSOR LM35

IC LM 35 sebagai sensor suhu yang teliti dan terkemas dalam bentuk Integrated Circuit (IC), dimana output tegangan keluaran sangat linear berpadanan dengan perubahan suhu. Sensor ini berfungsi sebagai pegubah dari besaran fisis suhu ke besaran tegangan yang memiliki koefisien sebesar 10 mV /°C yang berarti bahwa kenaikan suhu 1° C maka akan terjadi kenaikan tegangan sebesar 10 mV.

IC LM 35 ini tidak memerlukan pengkalibrasian atau penyetelan dari luar karena ketelitiannya sampai lebih kurang seperempat derajat celcius pada temperature ruang. Jangka sensor mulai dari – 55°C sampai dengan 150°C, IC LM35 penggunaannya sangat mudah, difungsikan sebagai kontrol dari indicator tampilan catu daya terbelah. IC LM 35 dapat dialiri arus 60 μ A dari supplay sehingga panas yang ditimbulkan sendiri sangat rendah kurang dari 0 ° C di dalam suhu ruangan.



Gambar 2-1. Bentuk dan simbol IC LM 35
Sumber : www_electroniclab_com - main page.htm

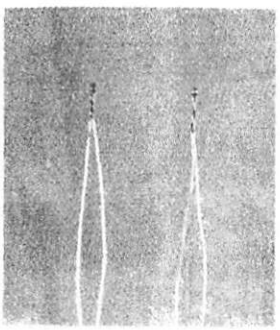
Adapun keistimewaan dari IC LM 35 adalah :

- Kalibrasi dalam satuan derajat celcius.
- Lineritas +10 mV/ ° C.
- Akurasi 0,5 ° C pada suhu ruang.
- Range +2 ° C – 150 ° C.
- Dioperasikan pada catu daya 4 V – 30 V.
- Arus yang mengalir kurang dari 60 μA

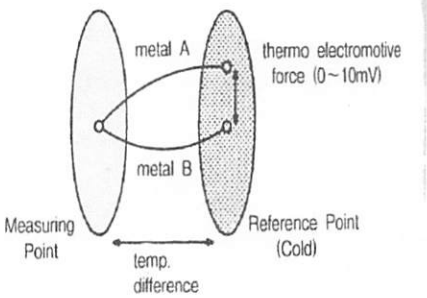
2.1.2. THEMOCOUPLE

Thermokopel merupakan dua buah bahan konduktor yang berbeda dan berpasangan digunakan untuk mengkonversikan arus bolak balik atau arus searah menjadi tegangan dan dapat diukur melalui suatu alat ukur ukur.

Bila suatu perbedaan temperature $T - T_1$ terdapat antara kedua titik ,maka gaya gerak listrik dibangkitkan dalam sirkuit tersebut yang memungkinkan arus mengalir didalamnya.Lihat gambar 2 -1 berikut ini ;



(a)



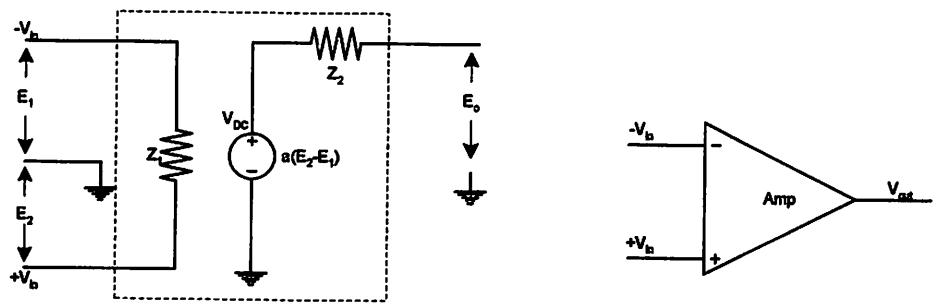
(b)

Gambar 2-2 Thermocouple

Termokopel ini mempunyai karakteristik yaitu pengukuran temperature thermokopel dikonversikan dari milivolts ke derajad pada range yang tersedia. Sehingga pada saat pengukuran akan diperoleh harga temperatu mutlak dan akan diperoleh kenaikan temperature.

2.2. MODEL RANGKAIAN OP AMP

Op amp adalah high gain, dc coupled amplifier yang mempunyai differential atau single ended input. Output biasanya single-ended terhadap tanah. Model rangkaian yang sederhana seperti gambar 2.1 untuk differential amplifier.



(a) (b)

A. Model

B. Simbol Rangkaian Untuk Op Amp

Gambar 2-3 Rangkaian Op Amp

Signal E_2 dimasukkan keterminal + 1 N dikuatkan oleh positive (non inverting) gain, + A. Signal E_1 dimasukkan keterminal - 1 N dikuatkan oleh negative (inverting) gain, - A.

Output $E_O = A (E_2 - E_1)$.

Single-ended amplifier apabila + 1 N ditanahkan.

Dalam menganalisa rangkaian feedback, model ideal untuk Op Amp adalah penting.

Karakteristik idealnya adalah :

1. Gain = $\sim (A \rightarrow \sim)$
2. $E_O = 0$ bila $E_2 = E_1$
3. Impedansi input = $\sim (Z_i \rightarrow \sim)$
4. Impedansi output = $0 (Z_O \rightarrow 0)$
5. Band width = $\sim$ (zero response time).

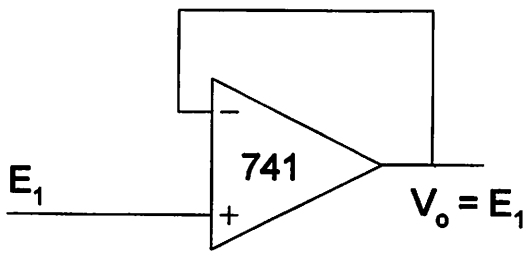
Karakteristik ideal ini dipakai untuk mengembangkan persamaan-persamaan untuk rangkaian feedback dasar. Dengan bertitik tolak dari karakteristik ideal ini , yang merupakan basis (pokok) untuk memilih bermacam-macam op amp didalam rangkaian –rangkaian praktis.

2.2.1. VOLTAGE FOLLOWER (PEMBUNTUT TEGANGAN)

Pembuntut tegangan (Volltage follower), atau pembuntut sumber (source follower), merupakan penguat non Inverting berpenguatan satu. Tegangan masukannya E_i, diterapkan langsung kemasukan (+) nya, karena tegangan antar pasak (+) dan pasak (-) dari op-amp itu bisa dianggap nol maka

$$V_0 = E_1$$

Oleh karenanya tegangan output betul-betul merupakan reproduksi tegangan output. Seperti penguat non Inverting lainnya, rangkain ini mempunyai impedansi input tinggi yang praktis sama dengan input Intrinsik op-amp. Pembuat tegangan digunakan untuk menyangga (buffer) sinyal input dari bebannya, berkat Impedansi inputnya yang tinggi dan impedansi outputnya yang rendah.



Gambar 2-4 Rangkaian pembuntut tegangan

Tegangan keluaran menyamai tegangan masukan baik besarnya maupun tandanya. Gain tegangannya adalah 1 (satu satuan)

$$A_{cl} = \frac{V_0}{E_i} = 1$$

2.2.2. INVERTING AMPLIFIER (PENGUAT MEMBALIK)

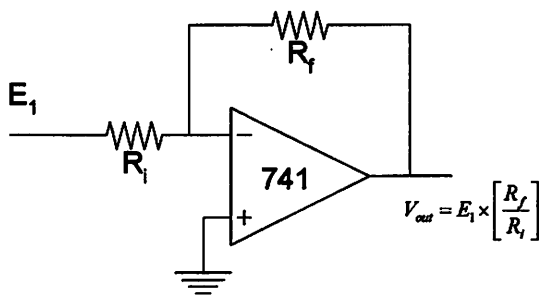
Pada gambar 2-2 adalah merupakan op-amp yang terangkai sebagai penguat inverting. Sinyal input disuapkan ke input inverting (-) op-amp melalui tahanan R_1 yang disebut elemen input. Tahanan R_f merupakan elemen umpan balik. Tegangan antara input (+)dan (-) pada dasarnya sama dengan 0V.

Penurunan tegangan melalui R_i adalah E_i. Arus I yang mengalir melalui R_i adalah $I = \frac{E_i}{R_i}$

Seluruh masukan I mengalir melalui R_f, disebabkan jumlah yang dialirkan oleh terminal masukan (-) nya dapat diabaikan. Arus yang melalui R_f ditentukan oleh R_i dan E_i, dan bukan oleh R_f V_f atau op-ampnya.

Penurunan tegangan yang melalui R_f adalah

$$V_{Rf} = I \times R_f = \frac{E_i}{R_i} R_f$$



Gambar 2-5 Penguat Inverting

Satu ujung R_f dan satu ujung R_L beban telah dihubungkan. Tegangan dari hubungan tersebut ke ground adalah V_0. ujung R_f dan R_L yang lain berada pada posisi ground. Karena itu, V_0 menyamai V_{Rf} dan menambah tanda minus.

Sehingga akan didapat :

$$V_0 = E_i \frac{R_f}{R_I}$$

Gain untaian tertutup dari penguat tersebut sebagai A_{cL}. adalah

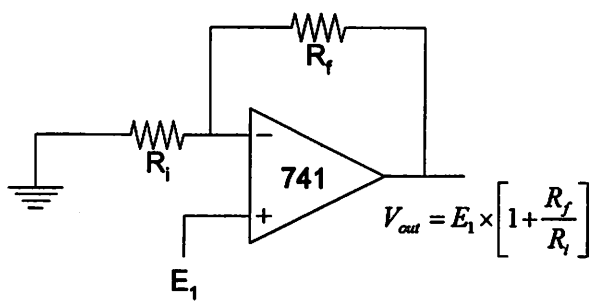
$$A_{cL} = \frac{V_0}{E_i} = \frac{R_f}{R_i}$$

Tanda minus menandakan bahwa polaritas keluaran V_0 terbalik terhadap input E_i. Oleh karenanya rangkaian tersebut dinamakan rangkaian pembalik.

2.2.3. NON INVERTING AMPLIFIER (PENGUAT TAK MEMBALIK).

Sinyal input E_i disuapkan ke input non inverting (+) op-amp. Tahanan masukan dari penguat pembalik adalah R_i. Tegangan keluaran, V_0 mempunyai polaritas yang sama seperti tegangan masukan E_i. Tegangan antara input (+) dan output (-) dari op-amp adalah 0V, E_i tampak melintasi R_i. E_i menyebabkan arus I mengalir, sehingga :

$$I = \frac{E_i}{R_i}$$



Gambar 2-6 Rangkaian Non Inverting

Arus I mengalir melalui R_f dan penurunan tegangan melintasi R_f dinyatakan oleh V_{Rf} dan dinyatakan

$$V_{Rf} = R_f = \frac{R_f}{R_i} \times E_i$$

Tegangan keluaran V_0 didapat dengan menambahkan E_i dengan tegangan yang melintsi V_{Rf}, yaitu V_{Rf}

$$V_0 = E_i + \frac{R_f}{R_i} \times E_i$$

$$= \left(1 + \frac{R_f}{R_i}\right) E_i$$

Oleh karena itu, penguatan tegangan penguat non Inverting akan lebih besar besar dari satu, tidak soal barapapun besarnya nalai R_f yang digunakan.

Perbedaan antara tegangan input dan output hanyalah fakta bahwa tegangan output akan $1 + R_f/R_i$ kali lebih besar dari inputnya

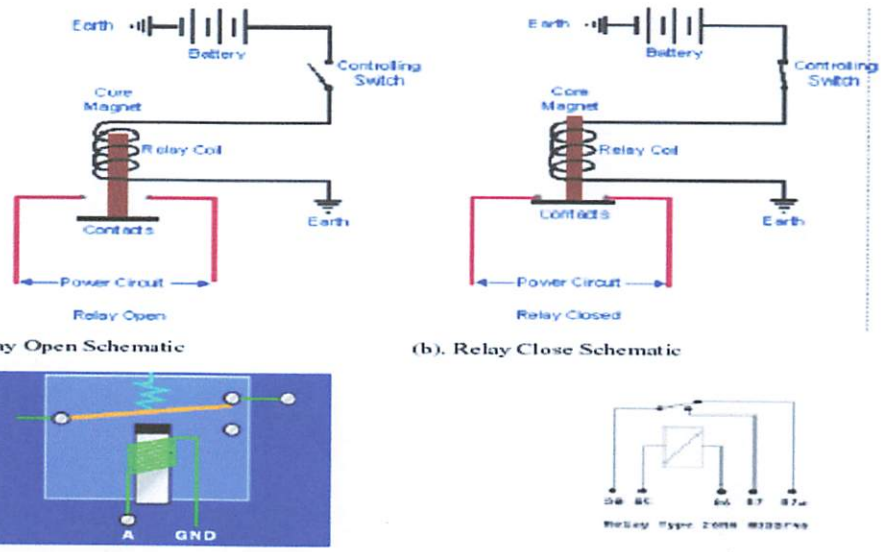
Untuk medapatkan gain tegangannya di dapatkan:

$$A_{cl} = \frac{V_0}{E_i} = 1 + \frac{R_f}{R_i}$$

2.3. RANGKAIAN RELAY

Relai merupakan aplikasi elektromagnetik sesungguhnya dimana ia tersusun atas kumparan kawat beserta sebuah inti besi lunak, (Hall, 1985). Pendapat lain mengatakan, relai adalah saklar elektromagnetik yang terdiri dari sebuah kumparan, inti besi lunak, armatur dan lengan kontak. Jika arus listrik mengalir sepanjang koil elektromagnetik, armatur akan menarik (pulls-

in) dan memindahkan kontak dari posisi normal (0) ke posisi kerja (1) dan sebaliknya jika tidak ada arus yang mengalir maka kontak kembali ke posisi normal, (Sand, 1973). Pada dasarnya relai adalah sakelar elektromagnetik yang bekerja apabila arus mengalir melalui kumparannya, sehingga inti besi menjadi magnet dan manarik kontak bila gaya magnet mengalahkan gaya pagas yang melawannya, (Loveday, 1992).



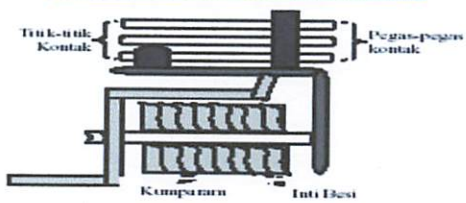
(a). Relay Open Schematic

(b). Relay Close Schematic

(c). Wiring Diagram

Gambar 1. Bagian-bagian fungsional relai.
http://www.relay wiring.com/

Gambar 2. Relay Construction
http://www.Relay Contruction.com/



Gambar 3. Konstruksi Relai
(Loveday, 1992)

Gambar 2-7 Relai

Dasar kerja relay adalah jika kumparan dialiri arus maka terjadi perubahan medan magnet di sekitar kumparan, akibatnya besi lunak yang terdapat dalam inti kumparan berubah menjadi magnet dan menarik lidah berpegas sehingga kontak *Normally Open (NO)* menjadi saklar tertutup.Lidah inilah yang dijadikan sebagai salah satu kontak saklar. Jika arus dimatikan, berarti kumparan kehilangan arus maka sifat magnet pada besi lunak hilang dan lidah tertarik oleh pegas sehingga kontak *Normally Closed (NC)* tertutup. Pemasangan kumparan relay dihubungkan secara seri dengan rangkaian driver dan lidah kontak juga dihubungkan seri dengan beban. Hal ini akan menjaga keamanan rangkaian dari arus beban yang lebih besar daripada arus driver.

2.4. PENGUBAH ANALOG KE DIGITAL (ADC)

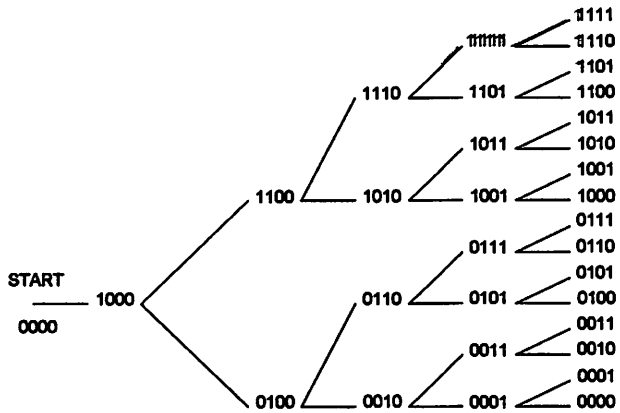
Apabila dalam suatu sistem elektronik hanya dapat mengolah data dalam bentuk biner saja, atau sering disebut pemrosesan besaran digital, maka setiap data analog yang akan diproses oleh sistem tersebut harus diubah dahulu kedalam kode biner (digital).

Jadi untuk menghubungkan sistem digital suatu rangkaian, sistem analog dari dunia nyata dibutuhkan suatu pengubah (konverter) sistem analog ke sistem digital, yang biasanya lebih dikenal dengan nama ADC (Analog to Digital Converter). Fungsi dasar dari sebuah konverter A/D adalah mengubah tegangan analog ke dalam kode-kode biner (digit) sehingga dapat diolah oleh sistem digital.

Tegangan analog yang merupakan masukan bagi ADC yang berasal dari penguat operasional, yang diinputi oleh transduser. Tegangan listrik yang

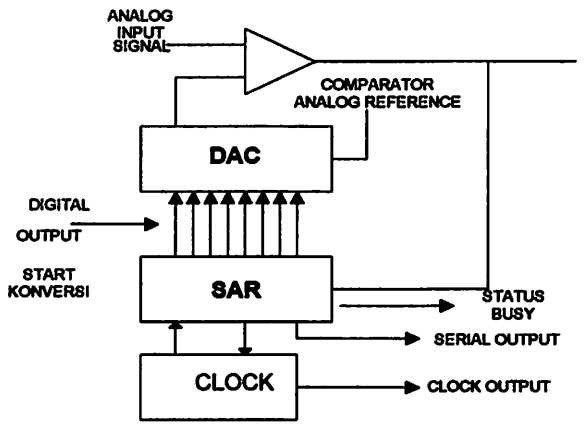
dihasilkan oleh penguat operasional ini berubah-ubah sesuai dengan perubahan tegangan pada transduser. Tegangan analog ini yang kemudian diubah oleh ADC menjadi bentuk degital yang sebanding dengan tegangan analognya. Kode biner hasil konversi inilah yang kemudian dipakai sebagai data yang diolah melalui data busnya. Pengubah analog ke digital merupakan merupakan jantung dari sistem data acquisition yang berfungsi untuk mengubah data ke dalam bentuk digital sehingga cocok untuk diproses oleh komputer melalui port LPT 1.

Dalam Penelitian ini digunakan ADC 0804 dari nasional semikonduktor. ADC jenis ini adalah jenis SAR (Successive Aproximation Register) ini memiliki rangkaian yang lebih kompleks dibandingkan dengan jenis ADC jenis yang laian. Dikatakan demikian karena konverter jenis ini peralatan konversinya tidak menggunakan counter untuk memberikan input blok konverter digital ke analognya. Sebagai gantinya konverter ini menggunakan register yang disebut Successive Aproximation Register (SAR), serta menggunakan sebuah konverter digital ke analognya yang mengontrol kerjanya sendiri. Keuntungan utama dari pemakaian SAR ini adalah dengan resolusi bit hanya dibutuhkan selang waktu n buah pulsa clock untuk konversi. Rangkaian utamanya terletak pada register yang mempunyai keluaran digital terlihat pada gambar 2-7 dibawah ini .



Gambar 2-7. Sistem Operasi Konversi SAR

Pada awal start konversi akan aktif yang mana akan menclear data yang sebelumnya, pada saat ini MSB (Most Significant Bit) "1", apabila kontrol register ini menyatakan keluaran kurang besar, maka bit yang di set tetap dan bit berikutnya lalu di set. Sebaliknya apabila kontrol menyatakan keluaran terlalu besar, maka bit awal yang diset akan direset kembali dan bit berikutnya akan diset. Urutan ini akan dikerjakan terus sampai urutan bit yang terakhir, sehingga data digital yang paling sebanding dengan tegangan analognya.



Gambar 2-8. Blok Diagram Aproxiamation Register

Dari gambar diatas, mula-mula dari register mempunyai harga digital tengah dengan membuat MSB set = "1", dan diberikan kekonverter digital ke analog yang mempunyai keluaran tegangan yang diumpankan pada komparator. Apabila harga tegangan ini kecil dari komparator akan menjadi "1" yang mengontrol SAR supaya menset bit berikutnya sehingga keluaran menjadi besar.

Dalam keadaan sebaliknya keluaran komparator akan menjadi "0" yang akan mengontrol SAR supaya mereset bit yang baru di set, dan menset bit berikutnya agar keluaran konverter digital ke analog lebih kecil.

Metoda SAR memiliki keunggulan dibandingkan jenis ADC lain yaitu :

1. Waktu konversi yang cepat.
2. Mempunyai waktu resolusi yang tinggi untuk diatas 12 bit.
3. Waktu konversi yang tetap yang mana tidak tergantung pada tegangan input.

4. Masing-masing output konversi tidak tergantung pada output sebelumnya. Kondisi ini terjadi sebab output sebelumnya telah diclearkan / direset sebelum melakukan konversi baru.

Makin banyak jumlah outputnya, berarti makin baik resolusinya dan kemampuan membedakan level tegangannya makin baik. Untuk membedakan resolusi/persen resolusi dari ADC dapat dicari dengan rumus :

$$\text{Resolusi} = 1/2^n \times E$$

Dimana : E = tegangan analog skala penuh

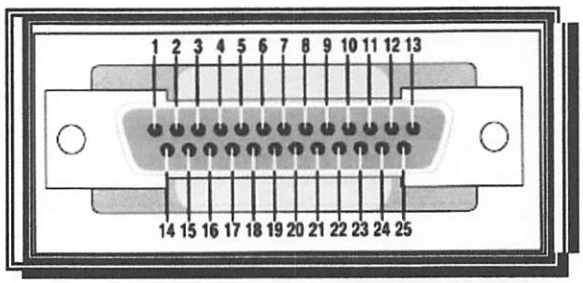
n = jumlah bit digitalnya.

Sedangkan persen resolusinya = $1/2^n \times 100\ \%$

2.5. PORT PARALLEL LPT

Dalam komunikasi data, bit-bit yang membentuk karakter dapat ditransmisikan secara paralel maupun secara serial. Pada komunikasi data paralel, dibutuhkan jumlah kanal yang sama banyak dengan jumlah bit pembentuk karakter dan bit-bit data dikirim secara serentak. Sedangkan pada komunikasi data serial hanya dibutuhkan satu kanal transmisi, setiap bit data dikirimkan satu per satu. Karena banyaknya jumlah kanal yang dibutuhkan dalam komunikasi paralel, komunikasi ini lebih banyak digunakan untuk komunikasi data jarak dekat, untuk komunikasi data jarak jauh lebih sesuai menggunakan komunikasi serial.

Untuk komunikasi paralel pada tranmisi data dari komputer ke printer biasanya digunakan *Female Conector* DB-25 seperti terlihat pada gambar 2-9 berikut:



Gambar 2-9. Konfigurasi Port Serial DB-25

Sumber : JimPrice.Com.1996-1997.2

Level tegangan pada DB-25 adalah level tegangan TTL (*Transistor-Trasistor Logic*) atau level tegangan baku dalam rangkaian digital. Yang simaksud dengan level tegangan TTL adalah Keadaan '0' dinyatakan dengan tegangan kurang dari 0,8 V sedangkan keadaan '1' dinyatakan dengan tegangan lebih besar dari 2,4 V. Tegangan kerja digital dengan level tegangan TTL adalah tegangan dengan level toleransi +/- 0,25 V.

Gambar 2-9. Konfigurasi Port Serial DB-25

Sumber : JimPrice.Com.1994 - [09/12]

level tegangan pada DP-25 adalah level tegangan TTL (Transistor-Transistor Logic) atau level tegangan buka dalam rangkaian digital. Yang simaksud dengan level tegangan TTL adalah kondisi "0" dinyatakan dengan tegangan kurang dari 0,8 V sedangkan kondisi "1" dinyatakan dengan tegangan lebih besar dari 2,4 V. Tegangan logik digital dengan level tegangan TTL adalah tegangan dengan level toleransi +/- 0,25 V

Tabel 2.1 Definisi Pin-Pin Konektor DB-25

Sumber : JimPrice.Com.1996-1997.3

Pin No (D-Type 25)	Pin No Centronic	SPP Signal	Directions in/out	Register	Hardware Inverted
1	1	nStrobe	In/Out	Control	Yes
2	2	Data 0	Out	Data	
3	3	Data 1	Out	Data	
4	4	Data 2	Out	Data	
5	5	Data 3	Out	Data	
6	6	Data 4	Out	Data	
7	7	Data 5	Out	Data	
8	8	Data 6	Out	Data	
9	9	Data 7	Out	Data	
10	10	nAck	In	Status	
11	11	Bussy	In	Status	Yes
12	12	Paper-Out PaperEnd	In	Status	
13	13	Select	In	Status	
14	14	nAuto-Linefeed	In/Out	Control	Yes
15	15	nError/nFault	In	Status	
16	16	nInitialize	In/Out	Control	
17	17	nSelect-Printer nSelact In	In/Out	Control	Yes
18 - 25	19 - 30	Gnd	Gnd		

2.6. BORLAND DELPHI

Bahasa pemrograman Delphi dapat digunakan untuk berbagai keperluan baik untuk perhitungan matematis, aplikasi perkantoran, aplikasi multimedia, pembuatan aplikasi pengolah, aplikasi control industri sampai kepada aplikasi *database*.

Tabel 2.1 Definisi Pin-Pin Konektor DB-25

Sumber : JimPrice.Com 1996-1997

Pin No (D-Type 25)	Pin No Centronic	SPP Signal	Directions in/out	Register	Hardware Inverted
1	1	nStrobe	In/Out	Control	Yes
2	2	Data 0	Out	Data	
3	3	Data 1	Out	Data	
4	4	Data 2	Out	Data	
5	5	Data 3	Out	Data	
6	6	Data 4	Out	Data	
7	7	Data 5	Out	Data	
8	8	Data 6	Out	Data	
9	9	Data 7	Out	Data	
10	10	nAck	In	Status	
11	11	Busy	In	Status	Yes
12	12	Paper-Out/PaperEnd	In	Status	
13	13	Select	In	Status	
14	14	nAuto-Linefeed	In/Out	Control	Yes
15	15	nError/nFault	In	Status	
16	16	nInitialize	In/Out	Control	
17	17	nSelect-Printer/nSelect-In	In/Out	Control	Yes
18 - 25	19 - 30	Gnd	Gnd		

2.6. BORLAND DELPHI

Bahasa pemrograman Delphi dapat digunakan untuk berbagai keperluan baik untuk perhitungan matematis, aplikasi perkantoran, aplikasi multimedia, pembuatan aplikasi pengolah, aplikasi control industri sampai kepada aplikasi database.

Bahasa pemrograman Delphi disebut bahasa prosedural artinya bahasa yang digunakan mengikuti urutan tertentu (prosedur). Ada jenis pemrograman *non-prosedural* seperti pemrograman untuk kecerdasan buatan seperti *Prolog*. Delphi termasuk keluarga visual sekelas Visual Basic, Visual C, artinya perintah-perintah untuk membuat objek dapat dilakukan secara visual. Pemrograman tinggal memilih objek apa yang ingin dimasukan kedalam *Form/Windows*, lalu tingkah laku objek properti dan *methode /procedure* dikemas menjadi satu kemasan (*encapsulate*).

Delphi adalah sebuah perangkat lunak (bahasa pemrograman) untuk membuat program /aplikasi komputer berbasis *windows*. Delphi merupakan bahasa pemrograman berbasis objek . artinya semua komponen yang ada merupakan objek-objek. Cii sebuah objek adalah memiliki nama, *property* dan *methode/procedure*. Delphi disebut juga visual programing artinya komponen komponen yang ada tidak hanya berupa teks (yang sebenarnya program kecil) tetapi muncul berupa gambar gambar. Dengan menggunakan delphi dapat diciptakan aplikasi *interfacing* dengan tampilan yang menarik dan atraktif bagi pengguna program.

2.6.1. STRUKTUR DATA DELPHI

Delphi memliki struktur data yang merupakan tipe data tumpukan dan tipe data buatan dari pengembangan tipe data baku. Berikut adalah tipe data baku pada delphi:

- *Char*

  Char adalah tipe data karakter yang memliki panjang 1 byte (8 bit) yang dapat dipresentasikan dengan suatu nilai ordinal atau dalam bentuk ASCII code atau dalam bentuk suatu karakter biasa, sebagai contoh untuk menjelaskan karakter 'A" dapat direpresentasikan dalam bentuk #65 (ASCII code) atau dalam bentuk nilai ordinal 101 ekuivalen desimalnya.

- *String*

  String adalah tipe data kumpulan dari karakter yang memiliki panjang 255 karakter yang dapat dipersentasikan dalam bentuk ASCII code atau dalam bentuk suatu karakter biasa, sebagai contoh untuk menjelaskan string yang berisi 'AAA' dapat direpresentasikan dalam bentuk #65#65#65 (ASCII code). *String* juga dapat dikatakan larik (*array*) dari karakter.

- *Integer*

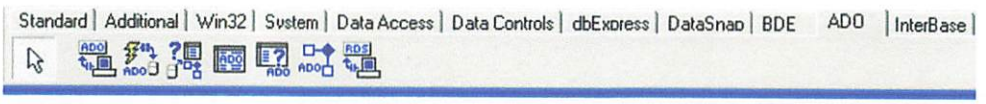
  Integer adalah tipe data numerik yang hanya dapat menampung bilangan bulat , *integer* memliki jangkauan dari -32768 sampai 32768 dengan kapasitas 2 byte (16 bit).

- *Real (floating point)*

  Real adalah tipe data numerik yang dapat menampung bilangan bulat ataupun bilangan pecahan (*floating point*)dengan panjang bit 6 bit.

2.6.2 *DATABASE* PADA DELPHI

Dukungan perangkat lunak delphi terhadap aplikasi *database* merupakan salah satu fitur kunci lingkungan pemrograman. Delphi memberikan seperangkat komponen serta pelengkap lainnya sehingga pembuatan aplikasi *database* menjadi lebih mudah. Komponen komponen database dikelompokan dalam *Component pallete data access datacontrol* dan BDE serta ADO seperti pada gambar di bawah ini:



Gambar 2.10 kelompok komponen dalam *database*

- Data access dan BDE (*Borland database engine*)

  Keuntungan menggunakan BDE integrasi yang sangat baik dengan Delphi. Elemen elemen terdokumentasi dengan baik dan merupakan solusi terbaik untuk pengaksesan file *database* lokal seperti *Dbase* dan *paradok.*

- *Data Control*

  Lebih menekankan pada pengaturan data yang terpasang pada aplikasi seperti *DBLabel, DBNavigator, DBImage, DBMemo, DBEdit, DBCombobox*, dan lain sebagainya.

- ADO (*activeX data object*)

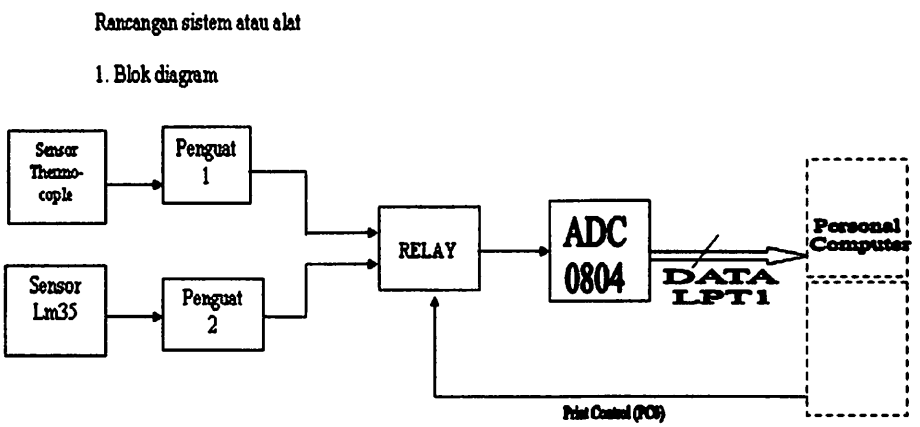
  Digunakan untuk komunikasi program dengan *Database MS Access* sehingga data yang dibuat dengan *MS Access* akan dapat diintergrasikan dengan Delphi.

BAB III

PERANCANGAN ALAT

3.1. PERANCANGAN SISTEM

Perancangan dan pembuatan alat untuk skripsi ini ditunjukkan pada blok diagram dari rancangan sistem atau alat di bawah ini :



Gambar 3 – 1 Blok Diagram System

Pada gambar 3-1 Diagram Blok Rancangan sistem yang terdiri atas :

- **Sensor Thermocople**

  Untuk membaca besaran temperatur menjadi elektrik dengan perubahan tegangan tertentu

- **Sensor LM 35**

  Untuk mendeteksi suhu yang dapat dikalibrasikan langsung dalam °C, LM 35 ini difungsikan sebagai basic temperature sensor. Vout dari LM 35 ini dihubungkan dengan ADC (Analog To Digital Converter). Dalam suhu

kamar (25°C) tranduser ini mampu mengeluarkan tegangan 250mV dan 1,5V pada suhu 150°C dengan kenaikan sebesar 10mV/°C.

- **Penguat Sensor Sensor 1 & 2**

  Menguatkan sinyal keluaran sensor yang masih lemah menjadi level tegangan yang sesuai untuk blok berikutnya

- **Relay**

  Untuk memilih data sensor yang akan di ukur

- **Rangkaian Analog to Digital Converter (ADC)**

  ADC pada rancangan ini digunakan untuk mengubah masukan analog keluaran sensor suhu yang sudah dikuatkan menjadi data digital 8 bit. Tipe ADC yang digunakan adalah ADC 0804

- **Personal Computer / PC**

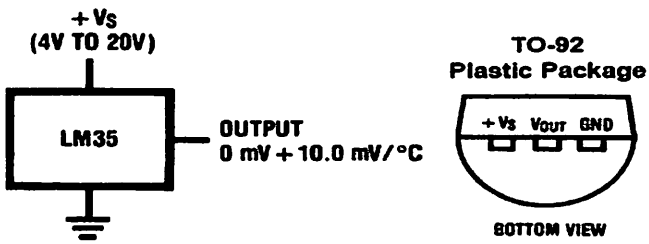
  Sebagai pembaca data digital melalui port LPT1 bagian data, pemilihan pembacaan sensor di control oleh port printer control (PC 0), selain itu sebagai sarana penyimpan data dari pembacaan sensor

3.1.1 PERANCANGAN HARDWARE

3.1.1.1 SENSOR LM35

Sensor suhu LM35 berfungsi untuk mengubah besaran fisis yang berupa suhu menjadi besaran elektris tegangan. Sensor ini memiliki parameter bahwa setiap kenaikan 1°C tegangan keluarannya naik sebesar 10mV dengan batas maksimal keluaran sensor adalah 1,5 V pada suhu 150°C. Pada perancangan kita tentukan keluaran adc mencapai full scale

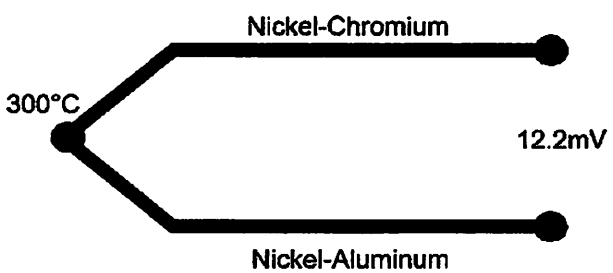
pada saat suhu 100°C, sehingga saat suhu 100°C tegangan keluaran transduser (10mV/°C x 100°C) = 1V. Dari pengukuran secara langsung saat suhu ruang, keluaran LM35 adalah 0.3V (300mV). Tegangan ini diolah dengan menggunakan rangkaian pengkondisi sinyal agar sesuai dengan tahapan masukan ADC..



Gambar 3-2 IC LM 35

3.1.1.2 SENSOR THERMOCOUPLE

Bila suatu perbedaan temperature T $-T_1$ terdapat antara kedua titik ,maka gaya gerak listrik dibangkitkan dalam sirkuit tersebut yang memungkinkan arus mengalir didalamnya.



Gambar 3-3 Thermocouple

Termokopel ini mempunyai karakteristik yaitu pengukuran temperature thermokopel dikonversikan dari milivolts ke derajad pada range

yang tersedia. Sehingga pada saat pengukuran akan diperoleh harga temperatu mutlak dan akan diperoleh kenaikan temperature.

3.1.1.3 PENGUAT SINYAL

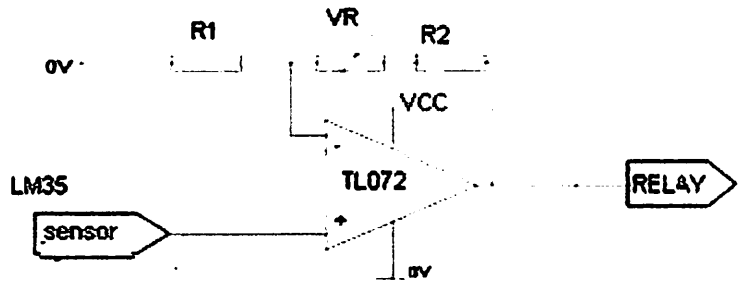
Penguat sinyal berfungsi untuk menguatkan tegangan keluaran sensor suhu LM35 dan thermocouple agar mampu diproses pada peralatan selanjutnya dalam hal ini oleh ADC 0804 Diinginkan bahwa pengukuran suhu dapat dilakukan pada range 25°C – 100°C, sedangkan saat suhu kamar LM35 sudah mengeluarkan tegangan sebesar 0,3V, sehingga untuk dapat mengatur agar masukan ADC sebesar 0V pada suhu ruang, ditambahkan sebuah penguat differensial, demikian juga dengan sensor thermocouple. Keluaran penguat differensial dikuatkan lagi dengan rangkaian penguat non inverting. Dengan Vin = 1V pada 100°C dan Vout yang diinginkan sebesar 5V (Vx) maka dapat dihitung nilai tahanan untuk penguat non-inverting sebagai berikut :

$$\frac{Vo}{Vi} = \left(1 + \frac{Rf}{Ri}\right)$$

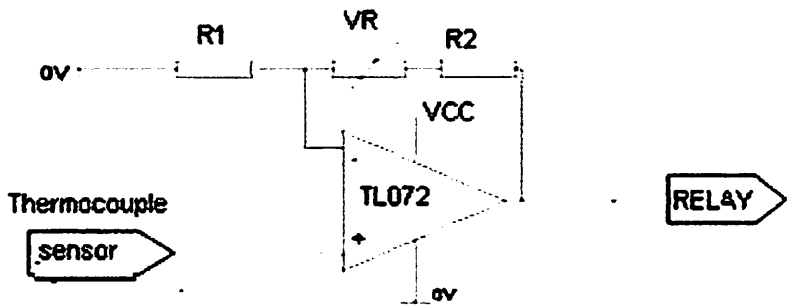
$$\frac{5}{1} = \left(1 + \frac{Rf}{Ri}\right)$$

$$4 = \frac{Rf}{Ri}$$

Jika Ri = 1K maka, Rf = 4K dalam aplikasi digunakan potensiometer 50K untuk Rf.



a.



b.

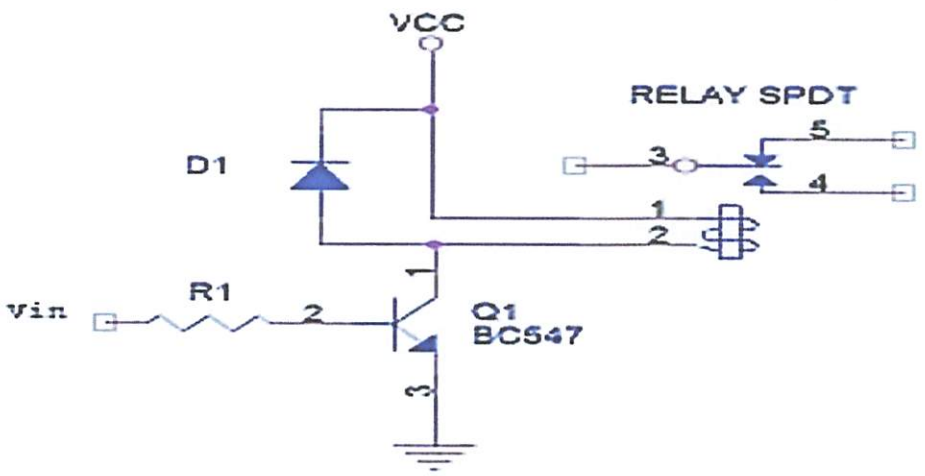
Gambar 3-4 Pengkondisi Sinyal

a. Pengkondisi sinyal untuk LM35

b. Pengkondisi Sinyal Thermocouple

3.1.1.4. PERANCANGAN RELAY

Relay pada perancangan alat ini berfungsi sebagai pemilih inputan yang akan di gunakan, sebelum di teruskan ke ADC 0804.



Gambar 3-5 Relay

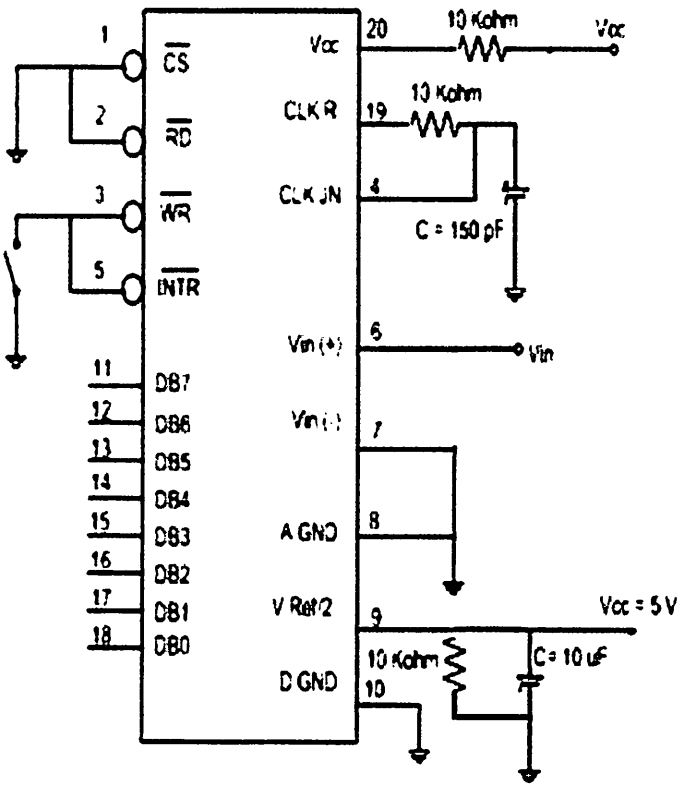
3.1.1.5. PERANCANGAN ANALOG TO DIGITAL CONVERTER (ADC)

ADC pada rancangan ini digunakan untuk mengubah masukan yang berupa sinyal analog dari rangkaian pengondisi sinyal menjadi data digital 8 bit. Tipe ADC yang digunakan adalah ADC 0804 dengan mode kerja free running, mode ini dipilih karena waktu konversi ADC 0804 jauh lebih cepat terhadap tingkat perubahan suhu dari plant, sehingga setiap kali suhu berubah, ADC selalu telah selesai melakukan konversi data sehingga data sudah valid untuk dicuplik.

Untuk ADC 0804 dengan jumlah bit sebesar 8 bit dan Vref = 5V maka resolusinya (ΔV) = 5 x 2-8 = 19,53mV. Masukan tegangan analog ADC yang berasal dari keluaran pengkondisi sinyal saat full scale dengan nilai sebesar Vx dapat dihitung sebagai berikut:

$$Vx = 5\left(\frac{1}{2^1}+\frac{1}{2^2}+\frac{1}{2^3}+\frac{1}{2^4}+\frac{1}{2^5}+\frac{1}{2^6}+\frac{1}{2^7}+\frac{1}{2^8}\right) = 5\frac{255}{256} = 4{,}9804v$$

dengan demikian saat tegangan masukan ADC 4,9804 keluaran ADC akan bernilai FFH.seperti pada gambar 3.6



Gambar 3.6 Rangkaian free running ADC

Untuk membuat mode kerja ADC menjadi free running, maka harus diketahui urutan pemberian nilai pada -RD dan -WR serta perubahan nilai pada -INTR. Urutan pemberian nilai pada -RD, -WR dan perubahan pada -INTR ditunjukkan pada tabel 3.1

Tabel 3-1 Pemberian nilai pada -RD dan -WR serta perubahan nilai pada -INTR

Langkah	$\overline{INTR}$	$\overline{WR}$	$\overline{RD}$
1	0	0	0
2	1	1	0

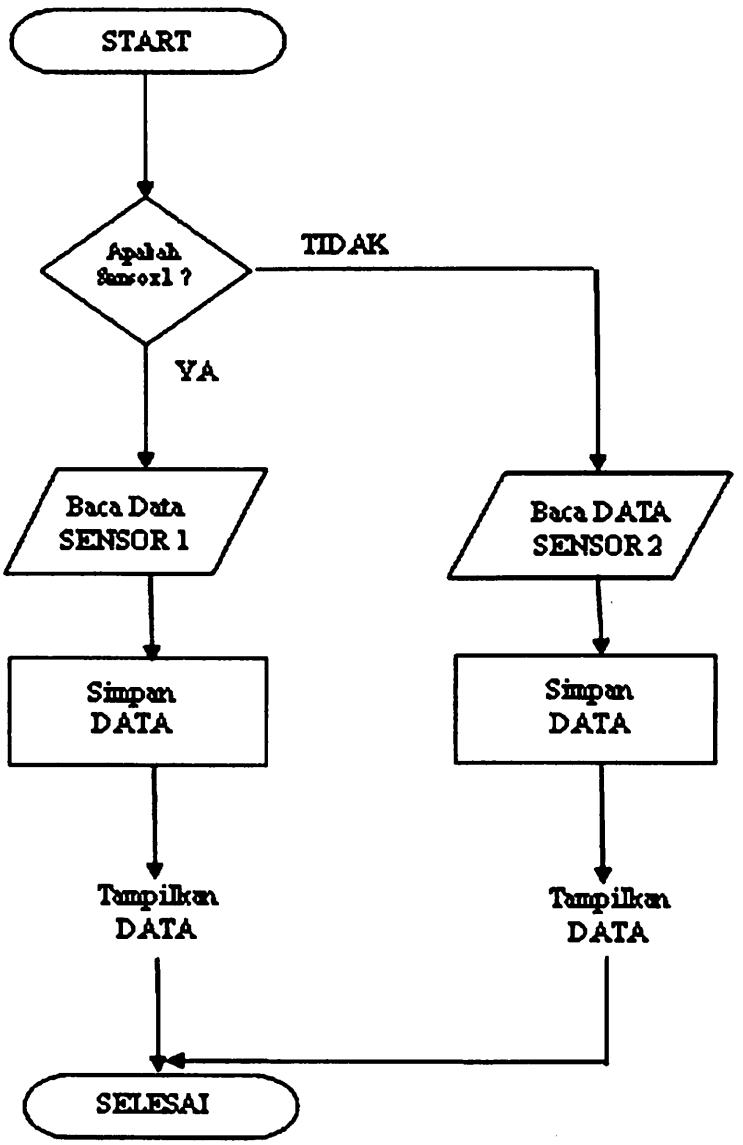
3.1.2 PERANCANGAN SOFTWARE

3.1.2.1 FLOWCHART DAN CARA KERJA ALAT

A. CARA KERJA ALAT

Saat sistem dihidupkan maka sistem akan mencari sensor yang akan digunakan, setelah sensor temperatur sudah terpilih maka akan dilakukan pembacaan data pada sensor yang dipilih, kemudian data di simpan sesuai dengan pemilihan waktu simpan yang diperlukan dan ditampilkan pada layar komputer berupa tabel yang berisi waktu pencatatan, kenaikan temperatur dan kemudian di tampilkan berupa grafik, pencatatan ini dapat di cetak bila di perlukan. Apabila akan melakuakn pencatatan pada sensor yang lain maka tekan tombol reset kemudian system akan melakuan pembacaan seperti pada pembacaan sensor sebelumnya.

B. FLOW CART



Gambar 3-6 Flow Chart Pencatat temperatur

3.1.3 PEMBAHASAN PERANGKAT LUNAK

Untuk mendukung kerja alat pencatatan temperatur ini juga di buat program untuk mengendalikan perangkat kerasnya. Program ini di tanam di dalam PC (Personal Computer), didalam software ini terdapat beberapa program yang di masukkan ke Personal Computer dengan menggunakan program Delphi 6 antara lain pembacaan temperatur, pemilih sensor, program pembaca ADC.

1. Pembacaan Temperatur

   Program pembacaan temperatur berfungsi untuk membaca temperatur sensor yang digunakan , kemudian memanggil rutin ADC 0804, data yang terbaca disimpan pada alamat yag telah ditentukan.

2. Pemilih Sensor

   Program ini berfungsi untuk menjalankan relay guna memilih sensor atau inputan yang akan di ukur, sebelum data atau hasil pengukuran di tampilkan ke layar komputer dengan bentuk grafik dan tabel.

3. Program Pembaca ADC

   ADC 0804 berfungsi untuk mengubah data analog dari sensor suhu yang sebelumnya telah dikuatkan terlebih dahulu dengan pengkondisi sinyal menjadi data digital yang kemudian akan diolah lebih lanjut oleh Personal Computer melalui port LPT 1, dengan alamat 378 untuk data dan 37A untuk kontrol.

BAB IV

ANALISA DAN PENGUJIAN ALAT

Setelah alat selesai dikerjakan maka untuk memastikan bahwa alat tersebut bekerja atau tidak maka perlu diadakannya suatu pengujian alat, pengujian ini meliputi pengujian pada perangkat keras dan pengujian pada perangkat lunaknya.

Dalam pengujian ini meliputi pengujian di setiap blok sehingga bila ada kesalahan atau kegagalan dalam merangcang alat dapat di minimalisasi dan segera dibenahi.

4.1. PENGUJIAN SETIAP BLOK

4.1.1. PENGUJIAN LM35

Sensor suhu LM35 diuji dengan cara memberikan catu 5V dan memberikan pemanasan secara tidak langsung, sedangkan tegangan keluaran langsung diamati dengan voltmeter digital guna menghindari kesalahan pembacaan ,dan dengan perhitungan seperti di bawah ini

{Vout = temp X 10 mV (° C)}

Pengujian sensor LM35 ini dilakukan dengan membandingkan pembacaan alat sensor LM35 dengan termometer digital kemudian dicatat secara manual, sehingga dari pengujian sensor LM 35 di dapatkan data sebagai berikut.

Tabel 4-1. Hasil pengujian sensor LM35

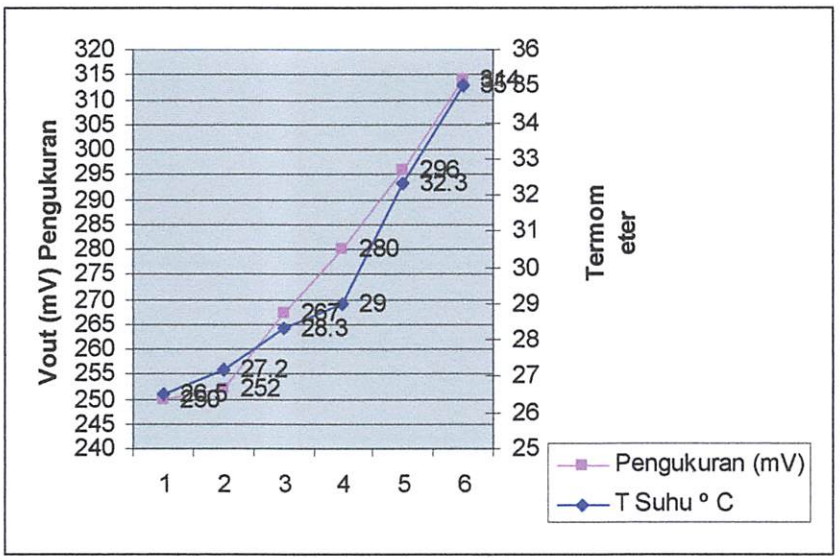
No	T Suhu ° C	Pengukuran (mV)	Perhitungan (mV)	Error
1	26,5	250	265	0.06
2	27,2	252	272	0.09
3	28,3	267	283	0.05
4	30	280	300	0.07
5	32,3	296	323	0.09
6	35	314	350	0.1

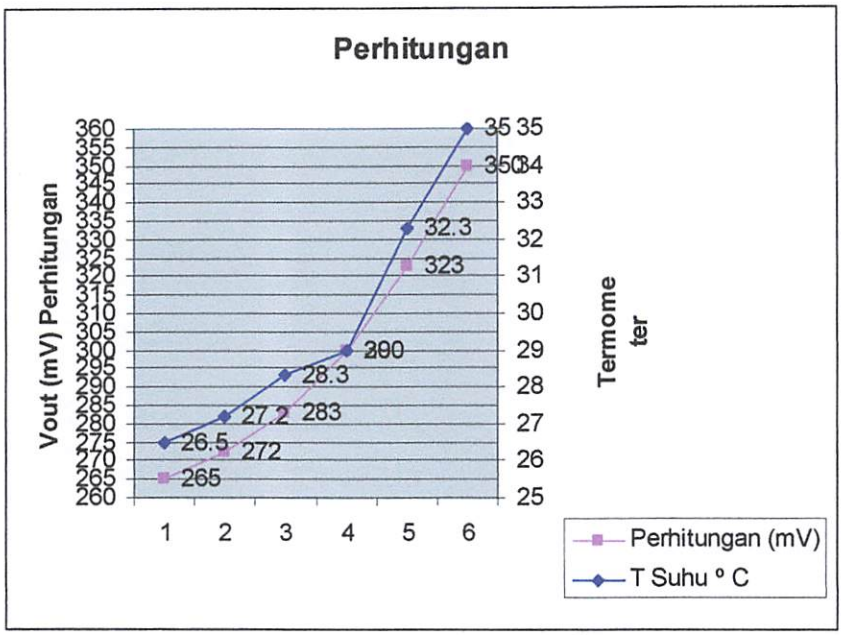
Prosentase kesalahan dihitung dengan persamaan :

$$\%\ \text{Kesalahan} = \left|\frac{N-n}{n}\right| \times 100\%$$

Dengan N : Pengukuran dengan Thermometer
n : Display dari sensor suhu

Adapun Hubungan antara alat sensor LM35 dan tampilan termometer serta perhitungan ditunjukkan pada grafik seperti pada gambar 4-1





Gambar 4-1 Grafik Sensor LM35

Dari grafik di atas di peroleh hasil perhitungan dengan termometer dan pengukuran dengan termometer dapat disimpulkan bahwa pada perhitungan dan pengukuran mempunyai tingkat kesalahan atau error yang cukup kecil yaitu 0.09 mV

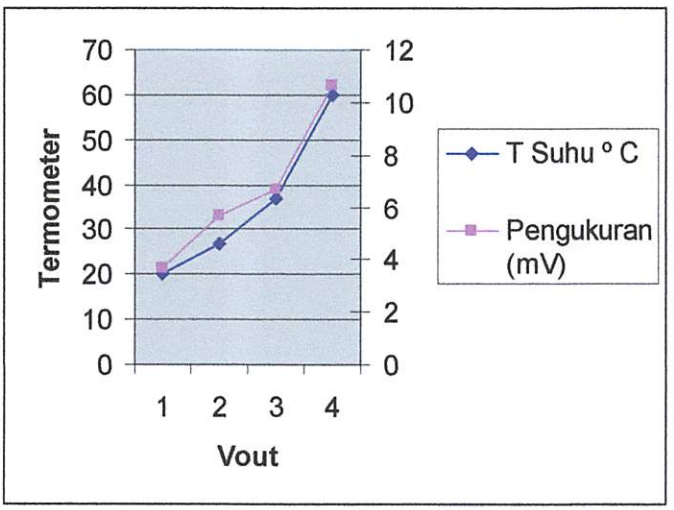
4.1.2. PENGUJIAN THERMOCOUPLE

Sensor thermocouple diuji dengan cara memberikan pemanasan langsung dengan bantuan solder yang di tempelkan pada thermocouple sedangkan tegangan keluaran langsung diamati dengan voltmeter digitall dan termometer air raksa yang mempunyai skala derajat minimal lebih dari 50 ° C. Dari pengujian didapatkan data sebagai berikut.

Tabel 4-2. Hasil pengujian sensor thermocouple

No.	T Suhu ° C	Pengukuran (mV)
1	20	3.7
2	27	5.7
3	37	6.7
4	60	10.6

Adapun Hubungan antara alat sensor thermocouple dan tampilan termometer ditunjukkan pada grafik seperti pada gambar 4-3



Gambar 4-2 Grafik Thermocouple

Dari grafik di atas di peroleh antara pengukuran dan tegangan yang di keluarkan oleh thrmocouple semakin derajat pengukuran termometer naik semakin naik pula tegangan yang dikeluarkan oleh sensor thermocouple.

4.1.3. PENGUJIAN PENGUAT SINYAL

Pengujian rangkaian penguat sinyal dilakukan dengan cara memberikan tegangan berubah-ubah pada bagian masukan penguat akhir (penguat non

inverting) kemudian mengukur keluarannya untuk kemudian dihitung tingkat penguatan tegangan.

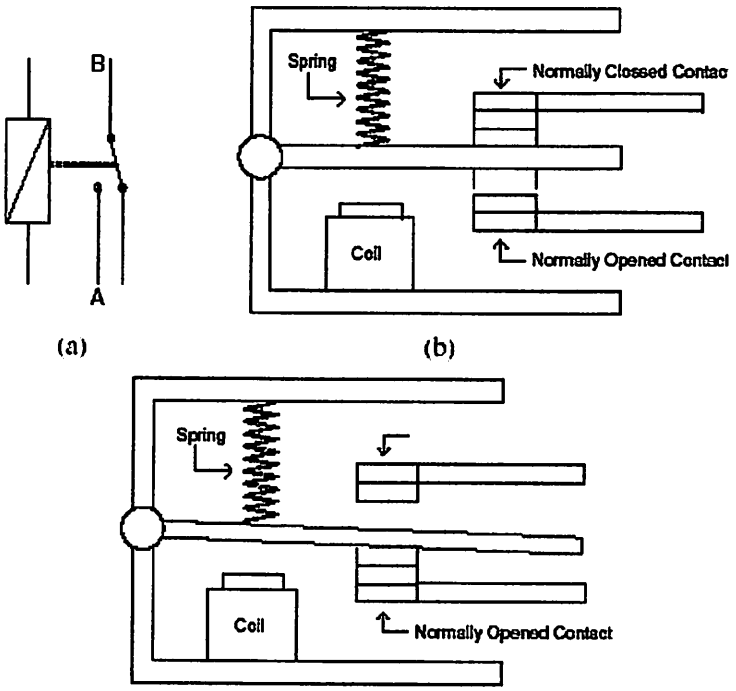
Tabel 4-3. Hasil pengujian pengkondisi sinyal

No	Vin	Vout	AV= (Vout/Vin)
1	0.1	0.5 V	5
2	0.2	1 V	5
3	0.3	1.5 V	5
4	0.4	2 V	5
5	0.5	2.5 V	5

Dari data tabel diketahui bahwa tingkat penguatan tegangan rangkaian pengkondisi sinyal adalah 5 kali, maka rangkaian telah dapat bekerja dengan baik

4.1.4. PENGUJIAN RELAY

Pengujian rangkaian relay ini dilakukan dengan cara memberikan tegangan 12V Jika arus dimatikan, berarti kumparan kehilangan arus maka sifat magnet pada besi lunak hilang dan lidah tertarik oleh pegas sehingga kontak *Normally Closed (NC)* tertutup. Pemasangan kumparan relay dihubungkan secara seri dengan rangkaian driver dan lidah kontak juga dihubungkan seri dengan beban. Hal ini akan menjaga keamanan rangkaian dari arus beban yang lebih besar daripada arus driver.



Gambar 4-3 Relay SPDT

(a) Simbol relay SPDT

(b) Konstruksi relay tanpa tegangan

(c) Konstruksi relay dengan tegangan

Relay mempunyai dua buah kontak yaitu *Normally Open(NO)* dan *Normally Closed (NC). Normally Open* adalah kontak relay dimana kontak ini terbuka pada saat kumparan relay tidak dialiri arus, sedang *Normally Closed* adalah kontak relay yang akan tertutup pada saat relay tidak dialiri arus dan secepatnya membuka kembali ketika kumparan diberi arus. Agar lebih jelas berikut cara kerja dari sebuah relay :

a) Mula-mula relay dalam keadaan tanpa arus, posisi kontak dalam keadaan *Normally Closed (NO)*, karena lidah tertarik oleh gaya pegas,

b) Arus diberikan pada koil, terjadi medan magnet dalam kumparan dengan inti besi lunak

c) Medan magnet yang dihasilkan dalam inti besi menarik lidah berpegas

sampai terhubung dengan kontak *Normally Open*, keadaan ini mengubah kontak *Normally Closed* terbuka dan kontak *Normally Open tertutup.*

d) Jika sumber arus dihilangkan maka medan elektromagnet pada inti besi lunak hilang dan lidah tertarik oleh gaya pegas. Lidah kontak seperti posisi semula dan posisi kontak *Normally Closed* tertutup.

Bahan yang digunakan sebagai kontaktor relay bermacam-macam, disesuaikan dengan kebutuhan dan harga yang dimiliki oleh kontak tersebut. Bahan-bahan tersebut rata-rata merupakan suatu penghantar yang baik seperti silver / perak, Perak *Cadmium Oxide*, *Palladium*, *Platina*, dan Emas. Pemilihan bahan ini tentu saja berpengaruh pada harga dan kualitas barang yang digunakan.

4.1.5. PENGUJIAN ADC

Pengujian dilakukan dengan cara memberi tegangan masukan pada ADC 0804 dan mencatat data digital keluaran yang dihasilkan melalui tampilan Avometer digital.

Tabel 4-4 Hasil Pengujian ADC

No	Vi	D7	D6	D5	D4	D3	D2	D1	D0
1	0	0	0	0	0	0	0	0	0
2	0.15	0	0	0	0	1	0	0	1
3	1.43	0	0	0	0	1	0	0	1
4	2.56	1	0	0	0	0	1	1	0
5	3.95	1	1	0	0	1	0	1	1
6	4.39	1	1	1	0	0	0	1	1
7	5.00	1	1	1	1	1	1	1	1

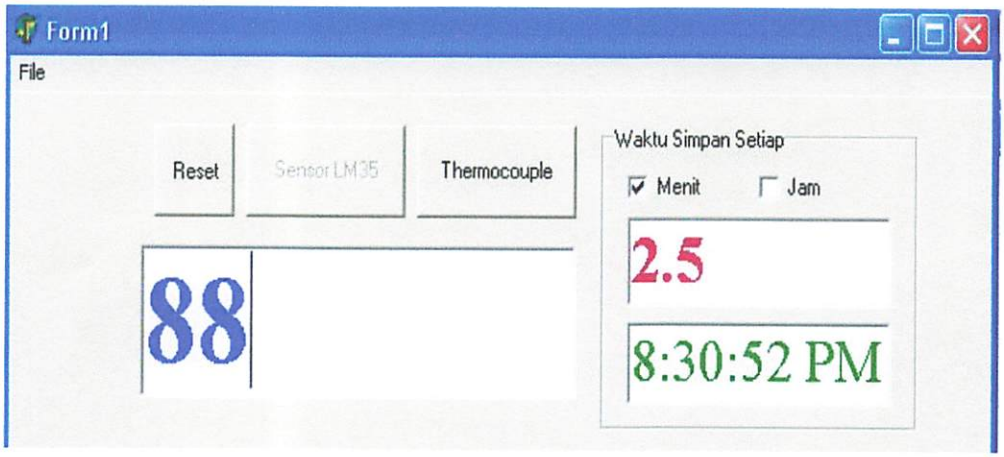
Data hasil pengujian ADC di atas menunjukkan bahwa komponen ini dapat bekerja dengan baik dengan resolusi 20mV

4.2 PENGUJIAN SOFTWARE

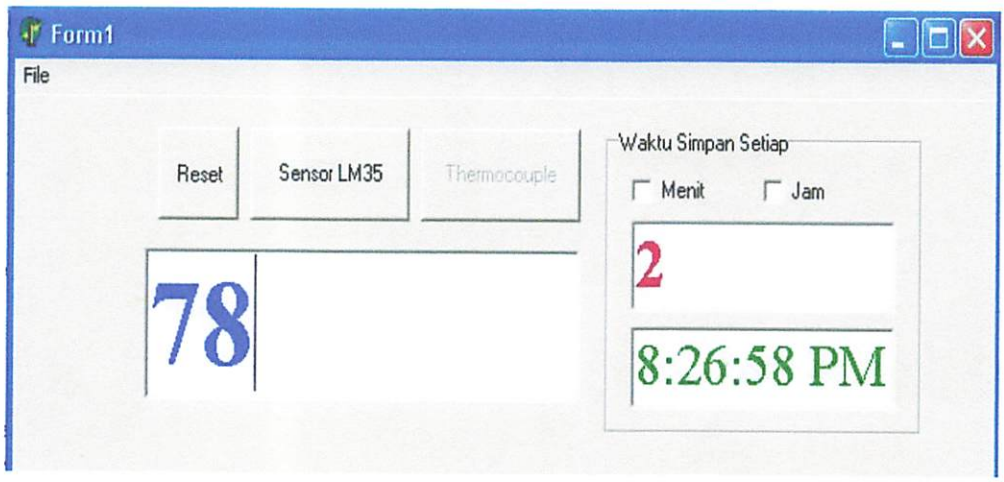
Pengujian software meliputi pengujian program pencatat data suhu dan kalibrasi data akuisisi terhadap tampilan suhu pada Layar komputer. Proses pengujiannya dilakukan dengan melihat secara visual data digital yang tertampil pada layar komputer yang merupakan data yang diakuisisi , penyimpanan data, serta dengan mengisi jeda waktu penyimpanan data berupa menit atau jam penyimpanan data sebelum di tampilkan pada grafik dan tabel.

Pada Tampilan Waktu Simpan diplih jeda waktu yang di inginkan, kenaikan suhu yang tampil pada layar akan di simpan sesuai dengan waktu simpan yang telah dipilih kemudian di masukkan ke dalam tabel senelum di tampilkan ke dalam bentuk grafik.

Setelah tampilan dalam bentuk grafik sudah terbentuk maka data tersebut dapat disimpan kemudian di cetak bila diperlukan.



A



B.

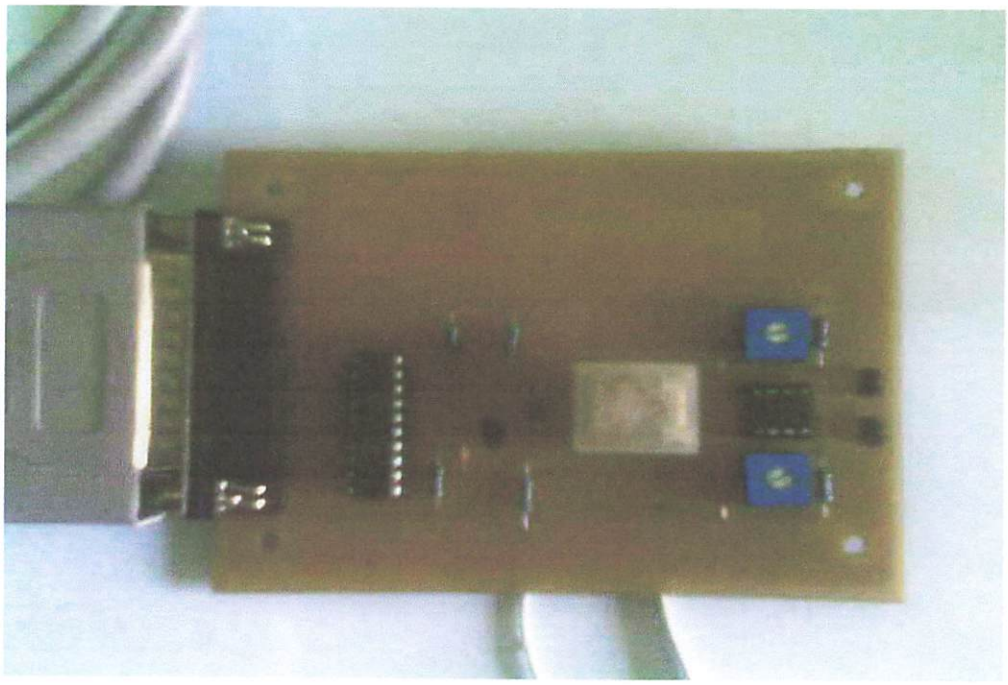
Gambar 4-4 Gambar tampilan digital

a. Tampilan sensor Thermocouple

b. Tampilan Sensor LM35

Gambar 4-5 Tampilan Grafik dan tabel sensor Thermocouple dan Sensor LM35

Pada gambar 4-5 tampilan grafik menunjukkan waktu simpan setiap 1 menit sehingga tiap satu menit akan menyimpan hasil dari pembacaan alat pada tiap-tiap sensor.



Gambar 4-6 Foto Alat pencatat Temperatur

Gambar 1.5 Foto Alat pencatat Temperatur

BAB V

PENUTUP

5.1. KESIMPULAN

Dari hasil perancangan dan pembuatan perangkat sistem akuisisi suhu dapat disimpulkan hal – hal sebagai berikut :

1. Hasil pengujian ADC menunjukkan bahwa untuk masukan sebesar 4,9V data digital sudah mencapai FFh, maka akan mengakibatkan terjadinya kesalahan penunjukkan suhu dimana saat tegangan masukan 4,9V suhu tertampil sudah mencapai 100°C pada sensor LM35
2. LM35 memiliki tegangan keluaran sensor dengan kenaikan sebesar 50 mV untuk setiap 5°C atau 10 mV/°C, maka sensor memiliki kenaikan yang cukup linier.

5.2. SARAN

Alat yang dibuat masih banyak kekurangan ,untuk penelitian selanjutnya penulis memiliki saran sebagai berikut :

1. Untuk pengukuran Thermocouple gunakan termometer ruangan atau yang mempunyai derajat maksimal atau dapat menggunakan termometer digital pada AVO meter
2. Alat ini masih menggunakan satu macam sensor yaitu sensor suhu dan dalam pengembangan dapat digunakan lebih dari dua sensor.
3. Penggunaan Alat ini bermanfaat bagi penelitian di Lab. Elektronika dan dapat digunakan pada industri yang berhubungan dengan temperatur.

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8. *http://depokinstruments.files.wordpress.com/2008/09/lm35.pdf*

INSTITUT TEKNOLOGI NASIONAL
MALANG
Jl. Raya Karangploso KM.2

FORMULIR BIMBINGAN SKRIPSI

Nama : **Anton Eko Yunaryanto**
Nim : **9517019**
Masa Bimbingan : **22 – 1 - 2009 s/d 17 – 3 - 2009**
Judul Skripsi : **Perancangan Dan Pembuatan Alat Pencatat Temperatur Yang Di Antar Mukakan Ke Komputer Melalui Port LPT 1**

No.	Tgl.	Uraian	Paraf
1	22 - 1 - 2009	Latar belakang dan tujuan.	
2	17 - 2 - 2009	teori dasar.	
3	10 - 3 - 2009	Susunan BAB III	
4	13 - 3 - 2009	susunan BAB IV dan uji alat.	
5	17 - 3 - 2009	Laporan makalah Seminar Hasil.	
6	23 - 3 - 2009	Laporan dan uji Alat ujian komprh	

Malang
Dosen Pembimbing I

I Komang Somawirata, ST, MT

Form S-4B

INSTITUT TEKNOLOGI NASIONAL
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MALANG

PERSETUJUAN PERBAIKAN SKRIPSI

Dari hasil Ujian Kompreherensip Jenjang Strata Satu (S-1) Jurusan Teknik Elektro Konsentrasi Elektronika yang diselenggarakan pada :

Hari : Selasa
Tanggal : 24 Maret 2009

Telah dilaksanakan Perbaikan skripsi oleh saudara :

Nama : Anton Eko Yunaryanto
N I M : 95.17.019

Perbaikan tersebut meliputi :

No	Materi Perbaikan	Paraf Dosen
1	Abstrak Diganti	
2	Tujuan Disempurnakan	
3	Batasan Masalah Diperbaiki	
4	Kesimpulan Diperbaiki	
5	Letak Tabel Di atas	

Malang, Maret 2009

Disetujui Oleh

Penguji I

(Ir. TH. Mimien Mustikawati, MT)

Mengetahui

Dosen Pembimbing I

(I Komang Somawirata, ST, MT)

INSTITUT TEKNOLOGI NASIONAL
Jl. Raya Karanglo KM 2
MALANG

PERSETUJUAN PERBAIKAN SKRIPSI

Dari hasil Ujian Kompreherensip Jenjang Strata Satu (S-1) Jurusan Teknik Elektro Konsentrasi Elektronika yang diselenggarakan pada :

Hari : Selasa
Tanggal : 24 Maret 2009

Telah dilaksanakan Perbaikan skripsi oleh saudara :

Nama : Anton Eko Yunaryanto
N I M : 95.17.019

Perbaikan tersebut meliputi :

No	Materi Perbaikan	Paraf Dosen
1	Penulisan Tabel	
2	Dicocokkan antara Rancangan dengan Perencanaan ADC, Pengkondisi Sinyal	
3	Tambakan Penjelasan Grafik Sensor LM35	

Malang, Maret 2009

Disetujui Oleh

Penguji II

(M. Ibrahim Ashari, ST, MT)

Mengetahui

Dosen Pembimbing I

(I Komang Somawirata, ST, MT)

```
unit skripsi;
interface
uses
  Windows, Messages, SysUtils, Variants, Classes, Graphics, Controls, Forms,
  Dialogs, Menus, ExtCtrls, SmallPort, StdCtrls, Buttons;
type
  TForm1 = class(TForm)
    SmallPort1: TSmallPort;
    Timer1: TTimer;
    MainMenu1: TMainMenu;
    File1: TMenuItem;
    Simpan1: TMenuItem;
    Cetak1: TMenuItem;
    Keluar1: TMenuItem;
    Label1: TLabel;
    Button1: TButton;
    Edit1: TEdit;
    Button2: TButton;
    RadioGroup1: TRadioGroup;
    Edit2: TEdit;
    CheckBox1: TCheckBox;
    CheckBox2: TCheckBox;
    Edit3: TEdit;
    BitBtn1: TBitBtn;
    procedure Keluar1Click(Sender: TObject);
    procedure Timer1Timer(Sender: TObject);
    procedure Button1Click(Sender: TObject);
    procedure Button2Click(Sender: TObject);
    procedure Button3Click(Sender: TObject);
    procedure BitBtn1Click(Sender: TObject);
  private
    { Private declarations }
  public
    { Public declarations }
  end;
var
  Form1: TForm1;
  a,b,c : integer;
implementation
{$R *.dfm}
procedure TForm1.Keluar1Click(Sender: TObject);
begin
      Close;
```

```
end;
procedure TForm1.Timer1Timer(Sender: TObject);
var
  DateTime : TDateTime;
  str : string;
begin
      Edit1.Text := IntToStr(SmallPort1.Port[$378]);
      DateTime := Time;
      str := TimeToStr(DateTime);
      Edit3.Text := str;
end;
procedure TForm1.Button1Click(Sender: TObject);
begin
      SmallPort1.Port[$37a] := $f0;
      Button2.Enabled :=false;
end;
procedure TForm1.Button2Click(Sender: TObject);
begin
      SmallPort1.Port[$37a] := $f1;
      Button1.Enabled := false;
end;
procedure TForm1.Button3Click(Sender: TObject);
begin
      SmallPort1.Port[$378] := 255;
      SmallPort1.Port[$37a]  := 255;
      SmallPort1.Port[$379]  := 255;
end;
procedure TForm1.BitBtn1Click(Sender: TObject);
begin
      Button1.Enabled := true;
      Button2.Enabled := true;
end;
end.
```

- Low Power Consumption
- Wide Common-Mode and Differential Voltage Ranges
- Low Input Bias and Offset Currents
- Output Short-Circuit Protection
- Low Total Harmonic Distortion
  0.003% Typ
- Low Noise
  V_n = 18 nV/$\sqrt{Hz}$ Typ at f = 1 kHz
- High Input Impedance . . . JFET Input Stage
- Internal Frequency Compensation
- Latch-Up-Free Operation
- High Slew Rate . . . 13 V/μs Typ
- Common-Mode Input Voltage Range Includes V_{CC+}

description

The JFET-input operational amplifiers in the TL07_ series are designed as low-noise versions of the TL08_ series amplifiers with low input bias and offset currents and fast slew rate. The low harmonic distortion and low noise make the TL07_ series ideally suited for high-fidelity and audio preamplifier applications. Each amplifier features JFET inputs (for high input impedance) coupled with bipolar output stages integrated on a single monolithic chip.

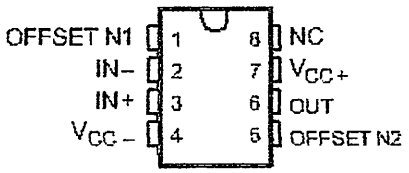
The C-suffix devices are characterized for operation from 0°C to 70°C. The I-suffix devices are characterized for operation from −40°C to 85°C. The M-suffix devices are characterized for operation over the full military temperature range of −55°C to 125°C.

AVAILABLE OPTIONS

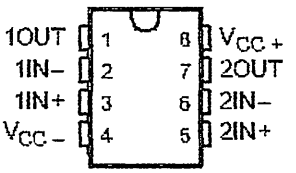
T_A	V_{IO}max AT 25°C	PACKAGE							
		SMALL OUTLINE (D)†	CHIP CARRIER (FK)	CERAMIC DIP (J)	CERAMIC DIP (JG)	PLASTIC DIP (N)	PLASTIC DIP (P)	TSSOP PACKAGE (PW)	FLAT PACKAGE (W)
0°C to 70°C	10 mV	TL071CD	—	—	—	—	TL071CP	TL071CPWLE	—
	6 mV	TL071ACD					TL071ACP	—	
	3 mV	TL071BCD					TL071BCP	—	
	10 mV	TL072CD	—	—	—	—	TL072CP	TL072CPWLE	—
	6 mV	TL072ACD					TL072ACP	—	
	3 mV	TL072BCD					TL072BCP	—	
	10 mV	TL074CD	—	—	—	TL074CN	—	TL074CPWLE	—
	6 mV	TL074ACD				TL074ACN		—	
	3 mV	TL074BCD				TL074BCN		—	
−40°C to 85°C	6 mV	TL071ID	—	—	—	—	TL071IP	—	—
		TL072ID				—	TL072IP		
		TL074ID				TL074IN	—		
−55°C to 125°C	6 mV	—	TL071MFK	—	TL071MJG	—	—	—	—
	6 mV		TL072MFK	—	TL072MJG	—	TL072MP		—
	9 mV		TL074MFK	TL074MJ	—	TL074MN	—		TL074MW

† The D package is available taped and reeled. Add the suffix R to the device type (e.g., TL071CDR). The PW package is only available left-ended taped and reeled (e.g., TL072CPWLE).

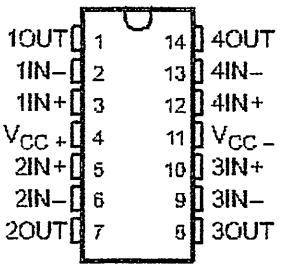
TL071, TL071A, TL071B
D, JG, P, OR PW PACKAGE
(TOP VIEW)



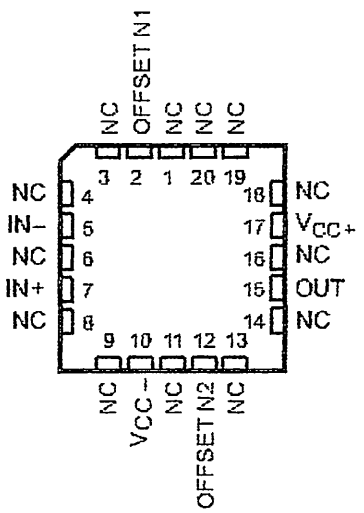
TL072, TL072A, TL072B
D, JG, P, OR PW PACKAGE
(TOP VIEW)



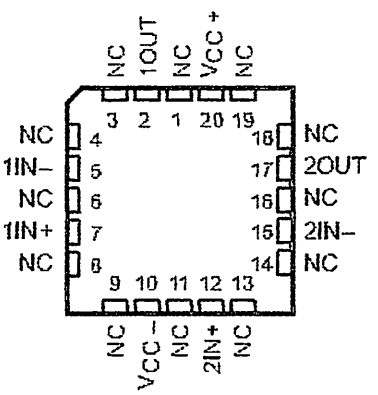
TL074, TL074A, TL074B
D, J, N, OR PW PACKAGE
TL074 . . . W PACKAGE
(TOP VIEW)



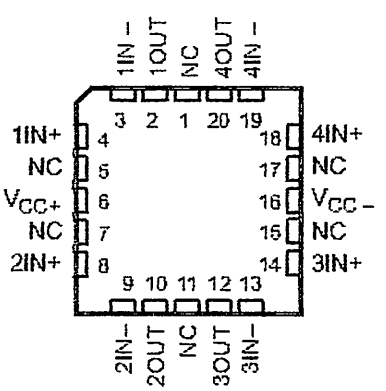
TL071
FK PACKAGE
(TOP VIEW)



TL072
FK PACKAGE
(TOP VIEW)



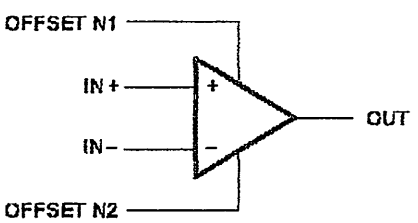
TL074
FK PACKAGE
(TOP VIEW)



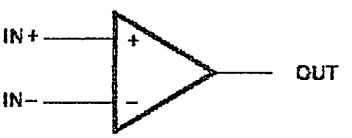
NC – No internal connection

symbols

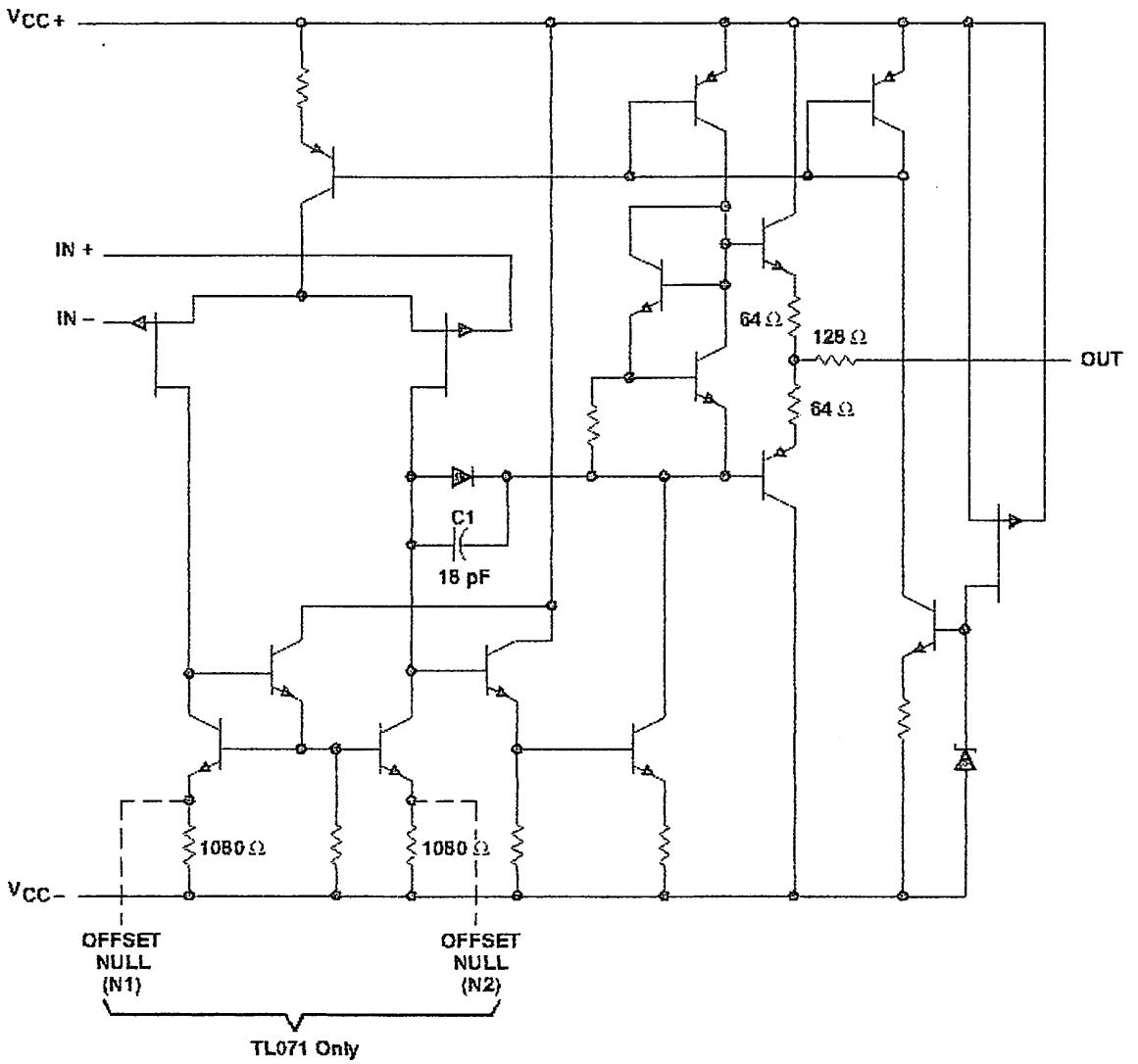
TL071



TL072 (each amplifier)
TL074 (each amplifier)



schematic (each amplifier)



All component values shown are nominal.

COMPONENT COUNT†			
COMPONENT TYPE	TL071	TL072	TL074
Resistors	11	22	44
Transistors	14	28	56
JFET	2	4	6
Diodes	1	2	4
Capacitors	1	2	4
epi-FET	1	2	4

†Includes bias and trim circuitry

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage, V_{CC+} (see Note 1) ..... 18 V
Supply voltage, V_{CC-} (see Note 1) ..... −18 V
Differential input voltage, V_{ID} (see Note 2) ..... ±30 V
Input voltage, V_I (see Notes 1 and 3) ..... +15 V
Duration of output short circuit (see Note 4) ..... unlimited
Continuous total power dissipation ..... See Dissipation Rating Table
Operating free-air temperature range, T_A: C suffix ..... 0°C to 70°C
I suffix ..... −40°C to 85°C
M suffix ..... −55°C to 125°C
Storage temperature range ..... −65°C to 150°C
Case temperature for 60 seconds: FK package ..... 260°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds: J, JG, or W package ..... 300°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds: D, N, P, or PW package ..... 260°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. All voltage values, except differential voltages, are with respect to the midpoint between V_{CC+} and V_{CC-}.
2. Differential voltages are at IN+ with respect to IN−.
3. The magnitude of the input voltage must never exceed the magnitude of the supply voltage or 15 V, whichever is less.
4. The output may be shorted to ground or to either supply. Temperature and/or supply voltages must be limited to ensure that the dissipation rating is not exceeded.

DISSIPATION RATING TABLE

PACKAGE	T_A = 25°C POWER RATING	DERATING FACTOR	DERATE ABOVE T_A	T_A = 70°C POWER RATING	T_A = 85°C POWER RATING	T_A = 125°C POWER RATING
D (8 pin)	680 mW	5.8 mW/°C	33°C	465 mW	378 mW	N/A
D (14 pin)	680 mW	7.6 mW/°C	60°C	604 mW	490 mW	N/A
FK	680 mW	11.0 mW/°C	88°C	680 mW	680 mW	273 mW
J	680 mW	11.0 mW/°C	88°C	680 mW	680 mW	273 mW
JG	680 mW	8.4 mW/°C	69°C	672 mW	546 mW	210 mW
N	680 mW	9.2 mW/°C	76°C	680 mW	597 mW	N/A
P	680 mW	8.0 mW/°C	65°C	640 mW	520 mW	N/A
PW (8 pin)	525 mW	4.2 mW/°C	70°C	526 mW	N/A	N/A
PW (14 pin)	700 mW	5.6 mW/°C	70°C	700 mW	N/A	N/A
W	680 mW	8.0 mW/°C	65°C	640 mW	520 mW	200 mW

electrical characteristics, $V_{CC\pm}$ = ±15 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS†	T_A‡	TL071C TL072C TL074C			TL071AC TL072AC TL074AC			TL071BC TL072BC TL074BC			TL071I TL072I TL074I			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
V_{IO}	Input offset voltage	V_O = 0, R_S = 50 Ω	25°C		3	10		3	6		2	3		3	6	mV
			Full range			13			7.5			5			8	
α_{VIO}	Temperature coefficient of input offset voltage	V_O = 0, R_S = 50 Ω	Full range		18			18			18			18		µV/°C
I_{IO}	Input offset current	V_O = 0	25°C		5	100		5	100		5	100		5	100	pA
			Full range			10			2			2			2	nA
I_{IB}	Input bias current§	V_O = 0	25°C		65	200		65	200		65	200		65	200	pA
			Full range			7			7			7			20	nA
V_{ICR}	Common-mode input voltage range		25°C	+11	−12 to 15		±11	−12 to 15		±11	−12 to 15		±11	−12 to 15		V
V_{OM}	Maximum peak output voltage swing	R_L = 10 kΩ	25°C	±12	±13.5		±12	±13.5		±12	±13.5		±12	±13.5		V
		R_L ≥ 10 kΩ	Full range	±12			±12			±12			±12			
		R_L ≥ 2 kΩ		±10			±10			±10			±10			
A_{VD}	Large-signal differential voltage amplification	V_O = ±10 V, R_L ≥ 2 kΩ	25°C	25	200		50	200		50	200		50	200		V/mV
			Full range	15			25			25			25			
B_1	Unity-gain bandwidth		25°C		3			3			3			3		MHz
r_i	Input resistance		25°C		10^{12}			10^{12}			10^{12}			10^{12}		Ω
CMRR	Common-mode rejection ratio	V_{IC} = V_{ICR}min, V_O = 0, R_S = 50 Ω	25°C	70	100		75	100		75	100		75	100		dB
k_{SVR}	Supply-voltage rejection ratio ($\Delta V_{CC\pm}/\Delta V_{IO}$)	V_{CC} = +9 V to +15 V, V_O = 0, R_S = 50 Ω	25°C	70	100		80	100		80	100		80	100		dB
I_{CC}	Supply current (each amplifier)	V_O = 0, No load	25°C		1.4	2.5		1.4	2.5		1.4	2.5		1.4	2.5	mA
V_{O1}/V_{O2}	Crosstalk attenuation	A_{VD} = 100	25°C		120			120			120			120		dB

† All characteristics are measured under open-loop conditions with zero common-mode voltage unless otherwise specified.
‡ Full range is T_A = 0°C to 70°C for TL07_C, TL07_AC, TL07_BC and is T_A = −40°C to 85°C for TL07_I.
§ Input bias currents of a FET-input operational amplifier are normal junction reverse currents, which are temperature sensitive as shown in Figure 4. Pulse techniques must be used that maintain the junction temperature as close to the ambient temperature as possible.

electrical characteristics, $V_{CC\pm}$ = ±15 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS†	T_A‡	TL071M TL072M			TL074M			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	
V_{IO}	Input offset voltage	V_O = 0, R_S = 50 Ω	25°C		3	6		3	9	mV
			Full range			9			15	
α_{VIO}	Temperature coefficient of input offset voltage	V_O = 0, R_S = 50 Ω	Full range		18			18		μV/°C
I_{IO}	Input offset current	V_O = 0	25°C		5	100		5	100	pA
			Full range			20			20	nA
I_{IB}	Input bias current‡	V_O = 0	25°C		65	200		65	200	pA
						50			50	nA
V_{ICR}	Common-mode input voltage range		25°C	±11	−12 to 15		−11	−12 to 15		V
V_{OM}	Maximum peak output voltage swing	R_L = 10 kΩ	25°C	±12	±13.5		−12	−13.5		V
		R_L ≥ 10 kΩ	Full range	±12			−12			
		R_L ≥ 2 kΩ		±10			−10			
A_{VD}	Large-signal differential voltage amplification	V_O = −10 V, R_L ≥ 2 kΩ	25°C	35	200		35	200		V/mV
				15			15			
B_1	Unity-gain bandwidth	T_A = 25°C			3			3		MHz
r_i	Input resistance	T_A = 25°C			10^{12}			10^{12}		Ω
CMRR	Common-mode rejection ratio	V_{IC} = V_{ICR}min, V_O = 0, R_S = 50 Ω	25°C	80	86		80	86		dB
k_{SVR}	Supply-voltage rejection ratio (ΔV_{CC}+/ΔV_{IO})	V_{CC} = ±9 V to ±15 V, V_O = 0, R_S = 50 Ω	25°C	80	86		80	86		dB
I_{CC}	Supply current (each amplifier)	V_O = 0, No load	25°C		1.4	2.5		1.4	2.5	mA
V_{O1}/V_{O2}	Crosstalk attenuation	A_{VD} = 100	25°C		120			120		dB

† Input bias currents of a FET-input operational amplifier are normal junction reverse currents, which are temperature sensitive as shown in Figure 4. Pulse techniques must be used that will maintain the junction temperature as close to the ambient temperature as possible.

‡ All characteristics are measured under open-loop conditions with zero common-mode voltage unless otherwise specified. Full range is T_A = −55°C to 125°C.

operating characteristics, $V_{CC\pm} = \pm 15$ V, $T_A = 25°C$

PARAMETER		TEST CONDITIONS		TL07xM			ALL OTHERS			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	
SR	Slew rate at unity gain	V_I = 10 V, C_L = 100 pF,	R_L = 2 kΩ, See Figure 1	5	13		8	13		V/μs
t_r	Rise time overshoot factor	V_I = 20 mV, C_L = 100 pF,	R_L = 2 kΩ, See Figure 1		0.1			0.1		μs
					20%			20%		
V_n	Equivalent input noise voltage	R_S = 20 Ω	f = 1 kHz		18			18		nV/√Hz
			f = 10 Hz to 10 kHz		4			4		μV
I_n	Equivalent input noise current	R_S = 20 Ω,	f = 1 kHz		0.01			0.01		pA/√Hz
THD	Total harmonic distortion	$V_I$rms = 6 V, R_L ≥ 2 kΩ, f = 1 kHz	A_{VD} = 1, R_S ≤ 1 kΩ,		0.003%			0.003%		

PARAMETER MEASUREMENT INFORMATION

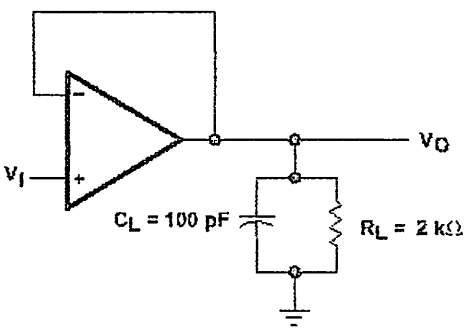


Figure 1. Unity-Gain Amplifier

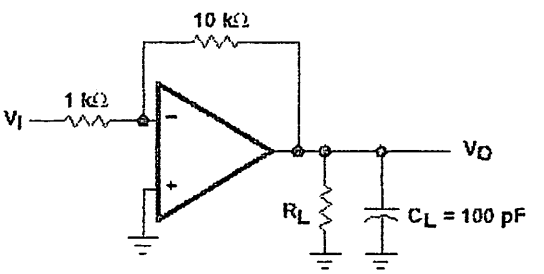


Figure 2. Gain-of-10 Inverting Amplifier

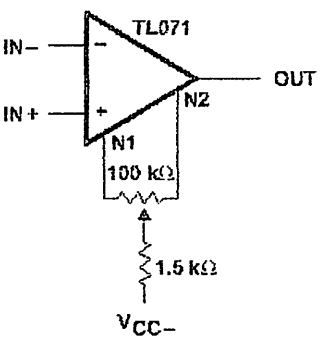


Figure 3. Input Offset Voltage Null Circuit

TYPICAL CHARACTERISTICS

Table of Graphs

			FIGURE
I_{IB}	Input bias current	vs Free-air temperature	4
V_{OM}	Maximum output voltage	vs Frequency vs Free-air temperature vs Load resistance vs Supply voltage	5, 6, 7 8 9 10
A_{VD}	Large-signal differential voltage amplification	vs Free-air temperature vs Frequency	11 12
	Phase shift	vs Frequency	12
	Normalized unity-gain bandwidth	vs Free-air temperature	13
	Normalized phase shift	vs Free-air temperature	13
CMRR	Common-mode rejection ratio	vs Free-air temperature	14
I_{CC}	Supply current	vs Supply voltage vs Free-air temperature	15 16
P_D	Total power dissipation	vs Free-air temperature	17
	Normalized slew rate	vs Free-air temperature	18
V_n	Equivalent input noise voltage	vs Frequency	19
THD	Total harmonic distortion	vs Frequency	20
	Large-signal pulse response	vs Time	21
V_O	Output voltage	vs Elapsed time	22

TYPICAL CHARACTERISTICS†

INPUT BIAS CURRENT
vs
FREE-AIR TEMPERATURE

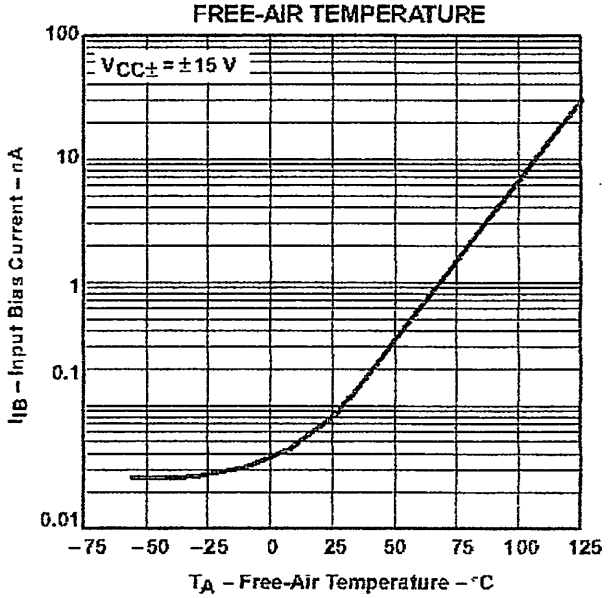


Figure 4

MAXIMUM PEAK OUTPUT VOLTAGE
vs
FREQUENCY

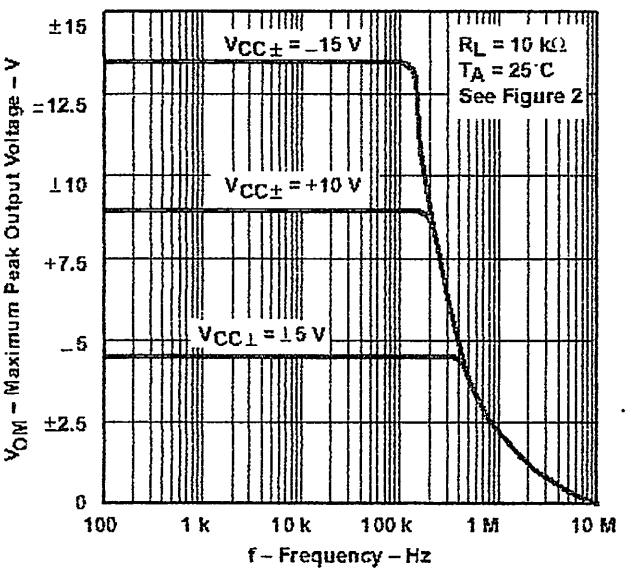


Figure 5

MAXIMUM PEAK OUTPUT VOLTAGE
vs
FREQUENCY

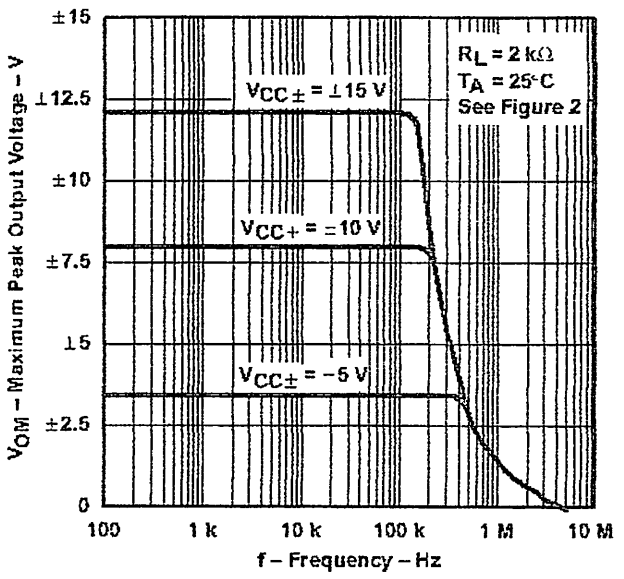


Figure 6

MAXIMUM PEAK OUTPUT VOLTAGE
vs
FREQUENCY

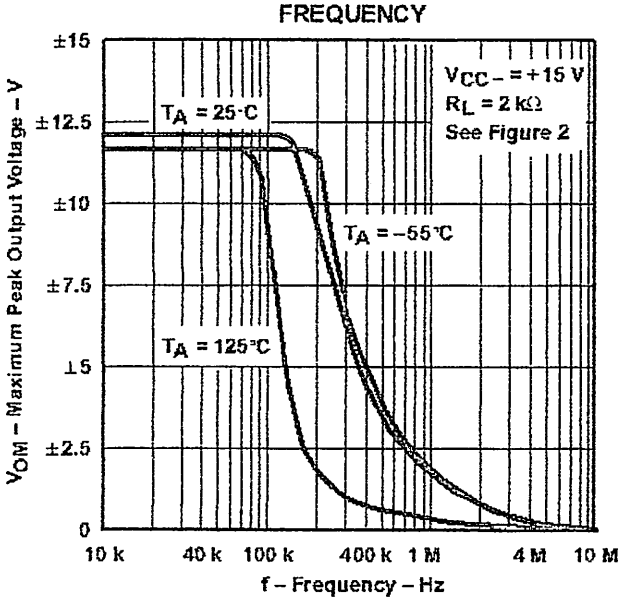


Figure 7

† Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

TYPICAL CHARACTERISTICS†

MAXIMUM PEAK OUTPUT VOLTAGE
vs
FREE-AIR TEMPERATURE

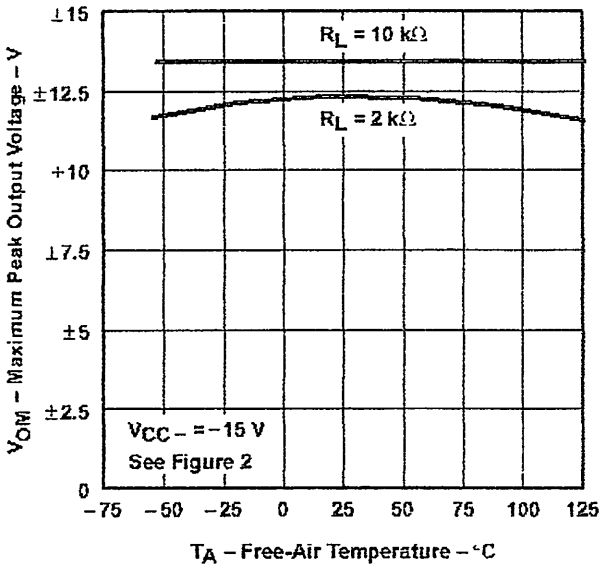


Figure 8

MAXIMUM PEAK OUTPUT VOLTAGE
vs
LOAD RESISTANCE

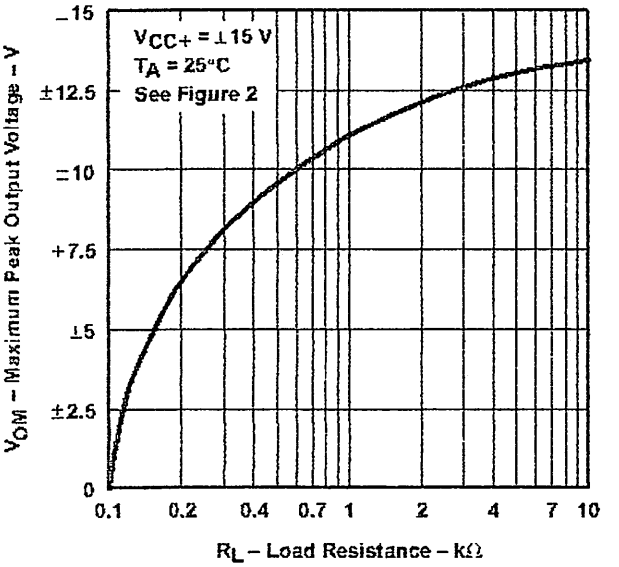


Figure 9

MAXIMUM PEAK OUTPUT VOLTAGE
vs
SUPPLY VOLTAGE

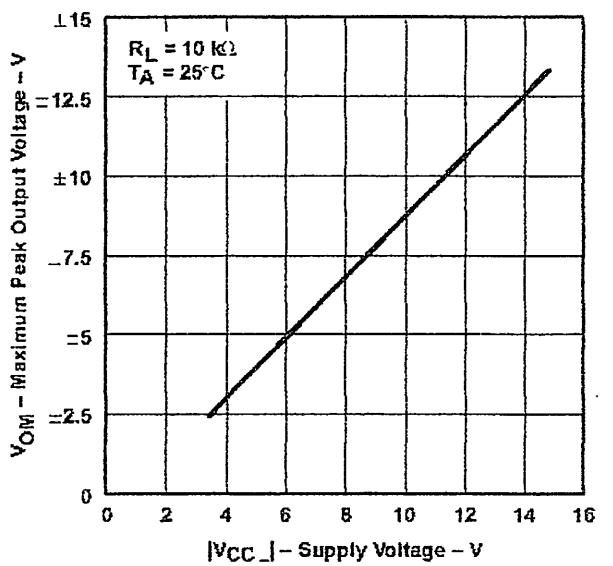


Figure 10

LARGE-SIGNAL
DIFFERENTIAL VOLTAGE AMPLIFICATION
vs
FREE-AIR TEMPERATURE

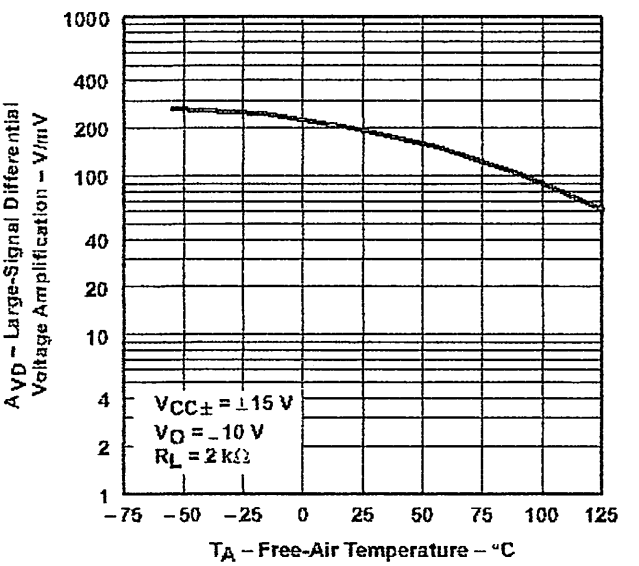


Figure 11

†Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

TYPICAL CHARACTERISTICS†

LARGE-SIGNAL
DIFFERENTIAL VOLTAGE AMPLIFICATION
AND PHASE SHIFT
vs
FREQUENCY

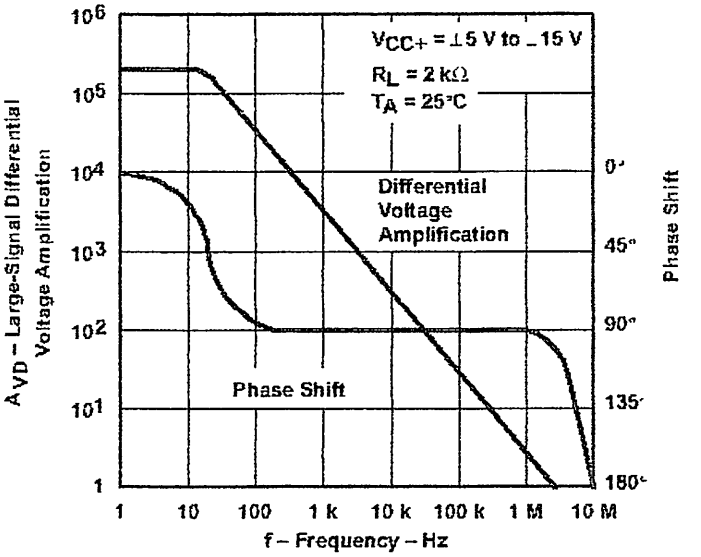


Figure 12

NORMALIZED UNITY-GAIN BANDWIDTH
AND PHASE SHIFT
vs
FREE-AIR TEMPERATURE

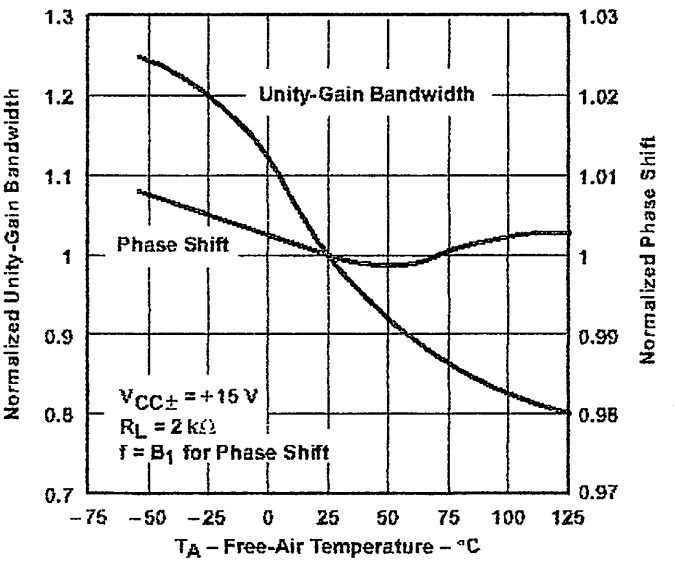


Figure 13

† Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

TYPICAL CHARACTERISTICS†

COMMON-MODE REJECTION RATIO
vs
FREE-AIR TEMPERATURE

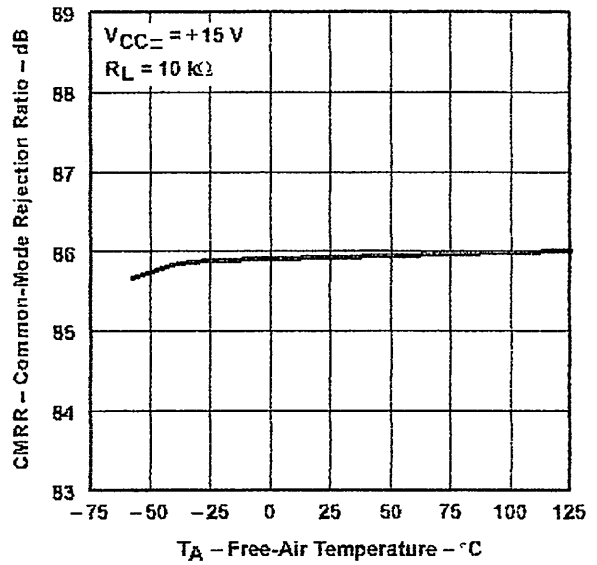


Figure 14

SUPPLY CURRENT PER AMPLIFIER
vs
SUPPLY VOLTAGE

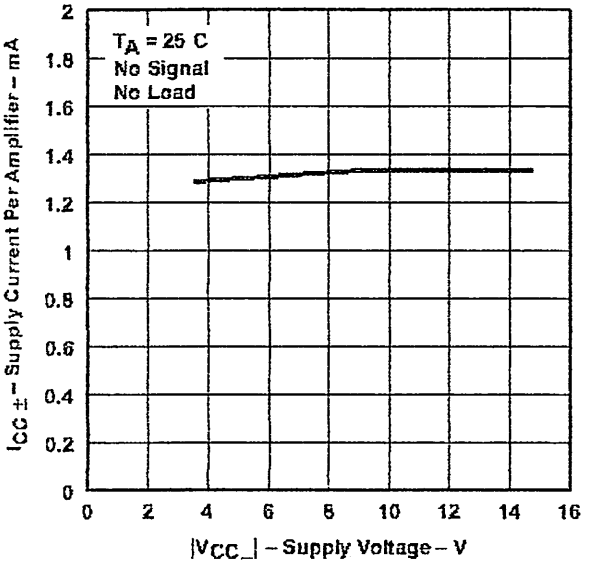


Figure 15

SUPPLY CURRENT PER AMPLIFIER
vs
FREE-AIR TEMPERATURE

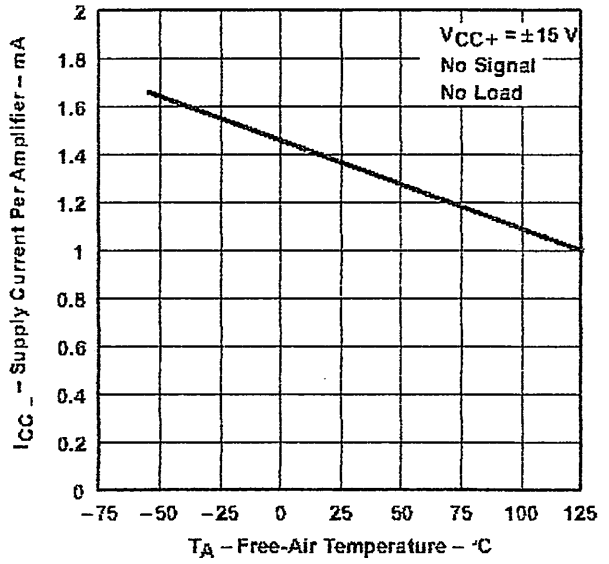


Figure 16

TOTAL POWER DISSIPATION
vs
FREE-AIR TEMPERATURE

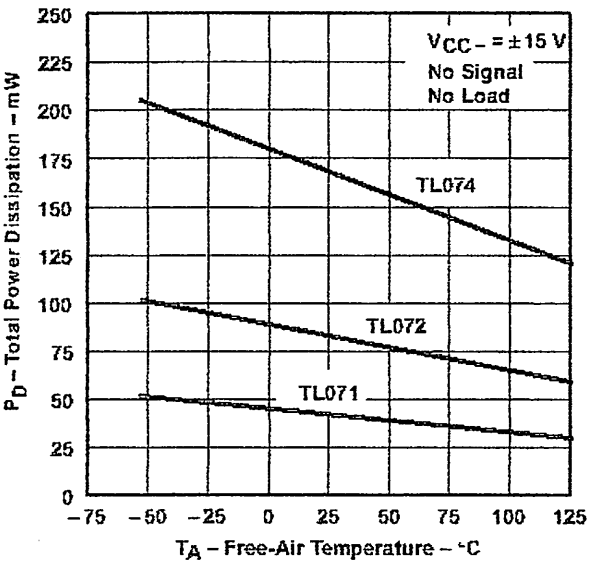


Figure 17

†Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

TYPICAL CHARACTERISTICS

NORMALIZED SLEW RATE
vs
FREE-AIR TEMPERATURE

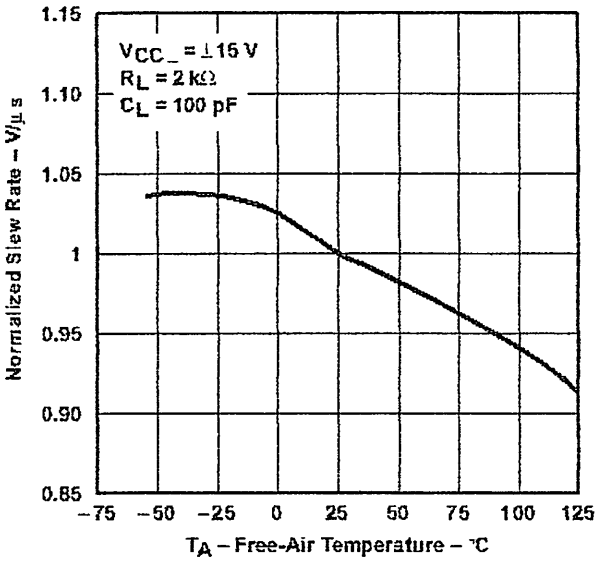


Figure 18

EQUIVALENT INPUT NOISE VOLTAGE
vs
FREQUENCY

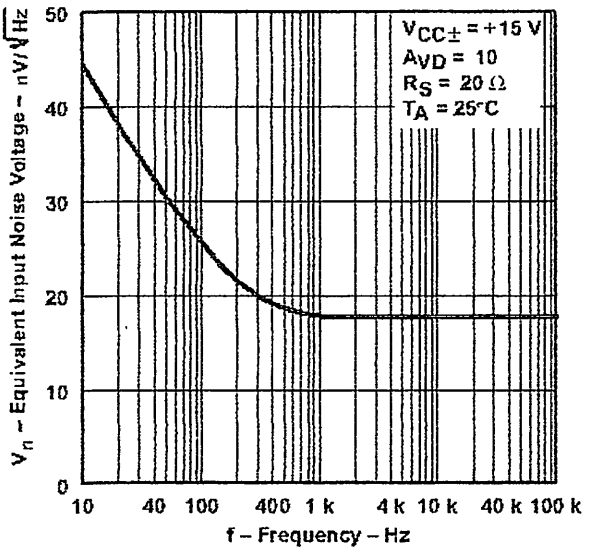


Figure 19

TOTAL HARMONIC DISTORTION
vs
FREQUENCY

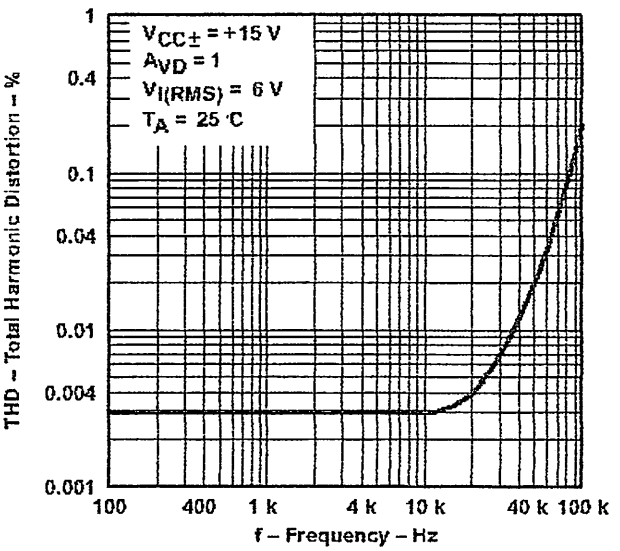


Figure 20

VOLTAGE-FOLLOWER
LARGE-SIGNAL PULSE RESPONSE

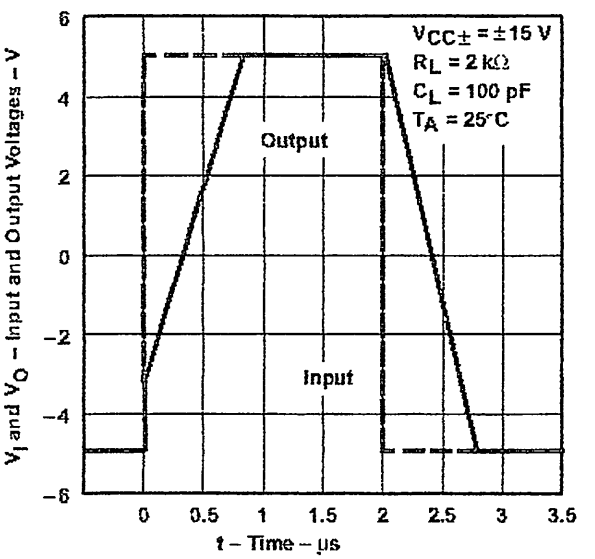


Figure 21

TYPICAL CHARACTERISTICS

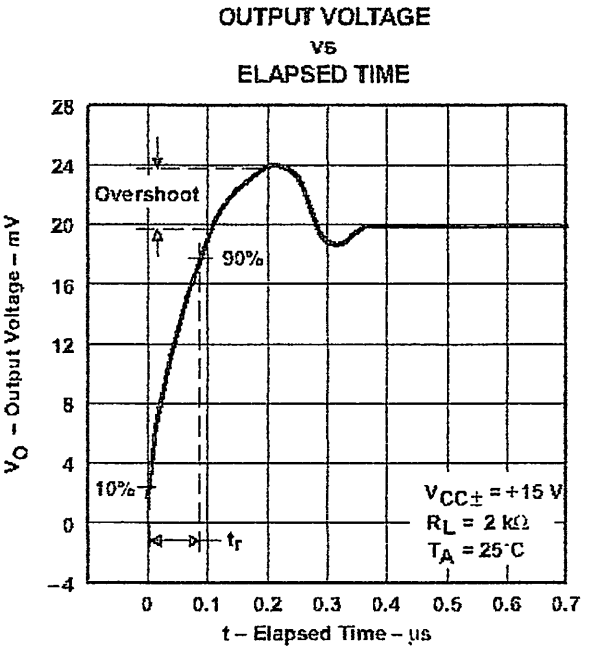


Figure 22

APPLICATION INFORMATION

Table of Application Diagrams

APPLICATION DIAGRAM	PART NUMBER	FIGURE
0.5-Hz square-wave oscillator	TL071	23
High-Q notch filter	TL071	24
Audio-distribution amplifier	TL074	25
100-kHz quadrature oscillator	TL072	26
AC amplifier	TL071	27

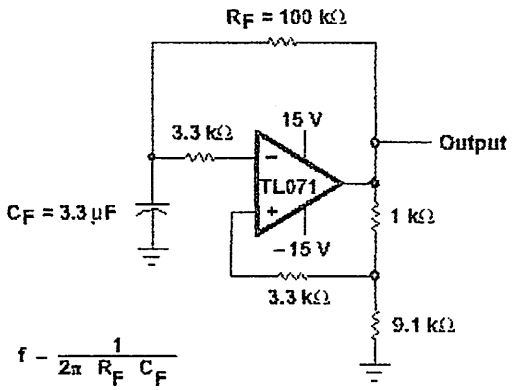


Figure 23. 0.5-Hz Square-Wave Oscillator

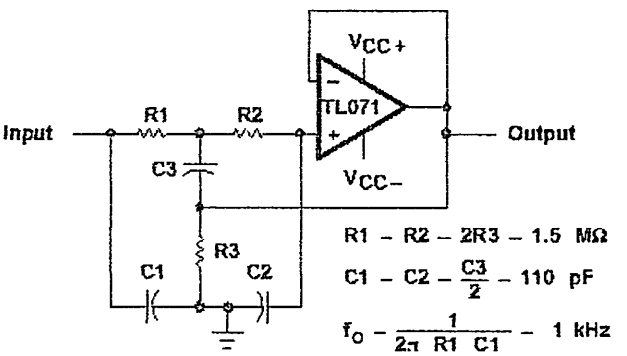


Figure 24. High-Q Notch Filter

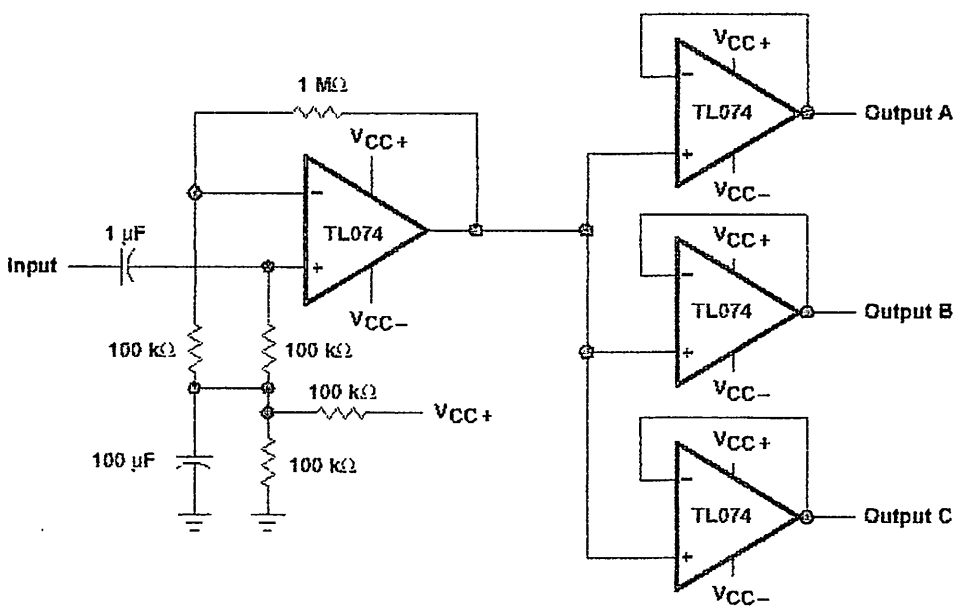
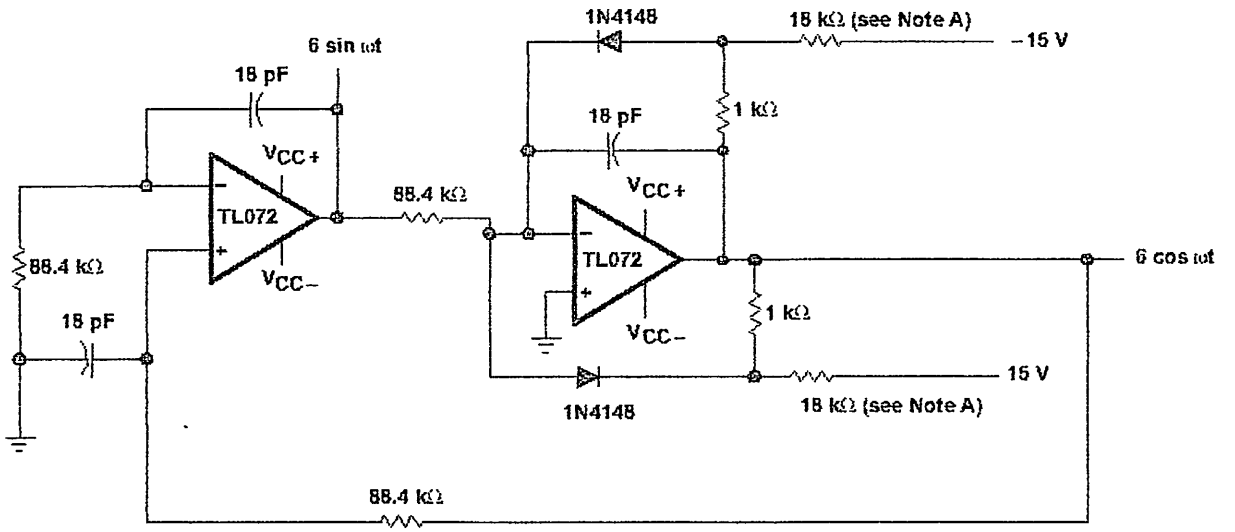


Figure 25. Audio-Distribution Amplifier

APPLICATION INFORMATION



NOTE A: These resistor values may be adjusted for a symmetrical output.

Figure 26. 100-kHz Quadrature Oscillator

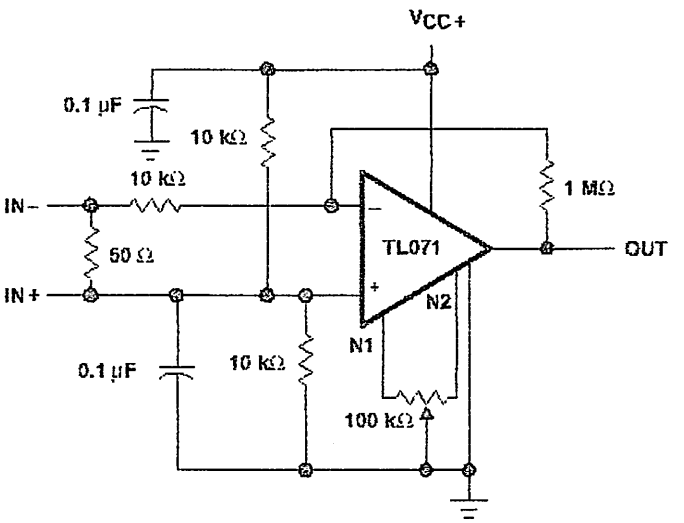


Figure 27. AC Amplifier

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National Semiconductor

December 1994

ADC0801/ADC0802/ADC0803/ADC0804/ADC0805
8-Bit µP Compatible A/D Converters

General Description

The ADC0801, ADC0802, ADC0803, ADC0804 and ADC0805 are CMOS 8-bit successive approximation A/D [illegible] similar to the 256R products. These converters are designed to allow operation with the NSC800 and INS8080A derivative control bus with TRI-STATE® output latches directly driving the data bus. These A/Ds appear like memory locations or I/O ports to the microprocessor and no interfacing logic is needed.

Differential analog voltage inputs allow increasing the common-mode rejection and offsetting the analog zero input voltage value. In addition, the voltage reference input can be adjusted to allow encoding any smaller analog voltage span to the full 8 bits of resolution.

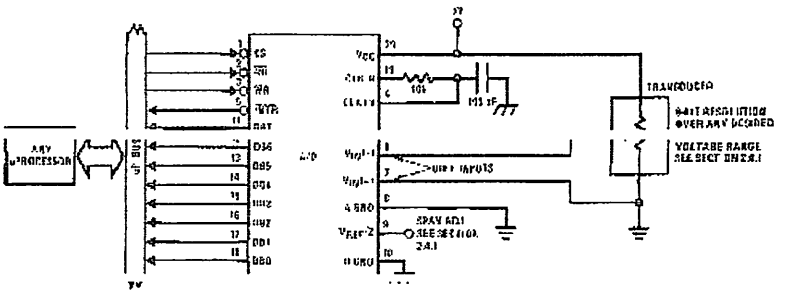
Features

- Compatible with 8080 µP derivatives—no interfacing logic needed - access time - 135 ns
- Easy interface to all microprocessors, or operates "stand alone"
- Differential analog voltage inputs
- Logic inputs and outputs meet both MOS and TTL voltage level specifications
- Works with 2.5V (LM336) voltage reference
- On-chip clock generator
- 0V to 5V analog input voltage range with single 5V supply
- No zero adjust required
- 0.3" standard width 20-pin DIP package
- 20-pin molded chip carrier or small outline package
- Operates ratiometrically or with 5 V_{DC}, 2.5 V_{DC}, or analog span adjusted voltage reference

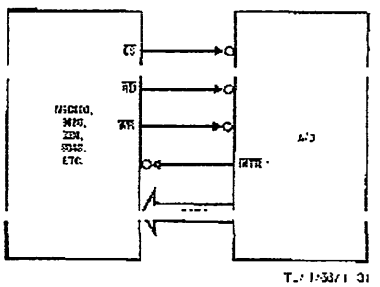
Key Specifications

- Resolution: 8 bits
- Total error: ±¼ LSB, ±½ LSB and ±1 LSB
- Conversion time: 100 µs

Typical Applications



8080 Interface



Part Number	Full-Scale Adjusted	Error Specification (Includes Full-Scale, Zero Error, and Non-Linearity) $V_{REF}/2 = 2.500\ V_{DC}$ (No Adjustments)	$V_{REF}/2$ = No Connection (No Adjustments)
ADC0801	±¼ LSB		
ADC0802		±½ LSB	
ADC0803	±½ LSB		
ADC0804		±1 LSB	
ADC0805			±1 LSB

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Z-80® is a registered trademark of Zilog Corp.

Absolute Maximum Ratings

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage (V_{CC}) (Note 3)	6.5V
Voltage	
Logic Control Inputs	−0.3V to +18V
At Other Input and Outputs	−0.3V to (V_{CC} +0.3V)
Lead Temp. (Soldering, 10 seconds)	
Dual-In-Line Package (plastic)	260°C
Dual-In-Line Package (ceramic)	300°C
Surface Mount Package	
Vapor Phase (60 seconds)	215°C
Infrared (15 seconds)	220°C
Storage Temperature Range	−65°C to +150°C
Package Dissipation at T_A = 25°C	875 mW
ESD Susceptibility (Note 10)	800V

Operating Ratings (Notes 1 & 2)

Temperature Range	$T_{MIN} \leq T_A \leq T_{MAX}$
ADC0801/02LJ, ADC0802LJ/883	−55°C ≤ T_A ≤ +125°C
ADC0801/02/03/04LCJ	−40°C ≤ T_A ≤ +85°C
ADC0801/02/03/05LCN	−40°C ≤ T_A ≤ +85°C
ADC0804LCN	0°C ≤ T_A ≤ +70°C
ADC0802/03/04LCV	0°C ≤ T_A ≤ +70°C
ADC0804LCWM	0°C ≤ T_A ≤ +70°C
Range of V_{CC}	4.5 V_{DC} to 6.3 V_{DC}

Electrical Characteristics

The following specifications apply for V_{CC} = 5 V_{DC}, $T_{MIN} \leq T_A \leq T_{MAX}$ and f_{CLK} = 640 kHz unless otherwise specified.

Parameter	Conditions	Min	Typ	Max	Units
ADC0801: Total Adjusted Error (Note 8)	With Full-Scale Adj. (See Section 2.5.2)			±¼	LSB
ADC0802: Total Unadjusted Error (Note 8)	$V_{REF}/2$ = 2.500 V_{DC}			±½	LSB
ADC0803: Total Adjusted Error (Note 8)	With Full-Scale Adj. (See Section 2.5.2)			±½	LSB
ADC0804: Total Unadjusted Error (Note 8)	$V_{REF}/2$ = 2.500 V_{DC}			±1	LSB
$V_{REF}/2$ Input Resistance (Pin 9)	ADC0801/02/03/05 ADC0804 (Note 9)	2.5 0.75	8.0 1.1		kΩ kΩ
Analog Input Voltage Range	(Note 4) V(−) or V(+)	Gnd−0.05		V_{CC} +0.05	V_{DC}
DC Common-Mode Error	Over Analog Input Voltage Range		±1/16	±1/8	LSB
Power Supply Sensitivity	V_{CC} = 5 V_{DC} ±10% Over Allowed $V_{IN}(-)$ and $V_{IN}(+)$ Voltage Range (Note 4)		±1/16	±1/8	LSB

AC Electrical Characteristics

The following specifications apply for V_{CC} = 5 V_{DC} and T_A = 25°C unless otherwise specified.

T_C	Conversion Time	f_{CLK} = 640 kHz (Note 6)	103		114	µs
T_C	Conversion Time	(Note 5, 6)	66		73	1/f_{CLK}
f_{CLK}	Clock Frequency Clock Duty Cycle	V_{CC} = 5V, (Note 5) (Note 5)	100 40	640	1460 60	kHz %
CR	Conversion Rate in Free-Running Mode	$\overline{INTR}$ tied to $\overline{WR}$ with $\overline{CS}$ = 0 V_{DC}, f_{CLK} = 640 kHz	8770		9708	conv/s
$t_{W(\overline{WR})L}$	Width of $\overline{WR}$ Input (Start Pulse Width)	$\overline{CS}$ = 0 V_{DC} (Note 7)	100			ns
t_{ACC}	Access Time (Delay from Falling Edge of $\overline{RD}$ to Output Data Valid)	C_L = 100 pF		135	200	ns
t_{1H}, t_{0H}	TRI-STATE Control (Delay from Rising Edge of $\overline{RD}$ to	C_L = 10 pF, R_L = 10k (See TRI-STATE Test		125	200	ns
t_{WI}, t_{RI}	Delay from Falling Edge of $\overline{WR}$ or $\overline{RD}$ to Reset of $\overline{INTR}$			300	450	ns
C_{IN}	Input Capacitance of Logic Control Inputs			5	7.5	pF
C_{OUT}	TRI-STATE Output Capacitance (Data Buffers)			5	7.5	pF
CONTROL INPUTS [Note: CLK IN (Pin 4) is the input of a Schmitt trigger circuit and is therefore specified separately]						
$V_{IN}(1)$	Logical "1" Input Voltage (Except Pin 4 CLK IN)	V_{CC} = 5.25 V_{DC}	2.0		15	V_{DC}

AC Electrical Characteristics (Continued)

The following specifications apply for V_{CC} = 5V_{DC} and $T_{MIN} \leq T_A \leq T_{MAX}$, unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Units
CONTROL INPUTS [Note: CLK IN (Pin 4) is the input of a Schmitt trigger circuit and is therefore specified separately]						
V_{IN} (0)	Logical "0" Input Voltage (Except Pin 4 CLK IN)	V_{CC}=4.75 V_{DC}			0.8	V_{DC}
I_{IN} (1)	Logical "1" Input Current (All Inputs)	V_{IN}=5 V_{DC}		0.005	1	μA_{DC}
I_{IN} (0)	Logical "0" Input Current (All Inputs)	V_{IN}=0 V_{DC}	−1	−0.005		μA_{DC}
CLOCK IN AND CLOCK R						
V_{T+}	CLK IN (Pin 4) Positive Going Threshold Voltage		2.7	3.1	3.5	V_{DC}
V_{T-}	CLK IN (Pin 4) Negative Going Threshold Voltage		1.5	1.8	2.1	V_{DC}
V_H	CLK IN (Pin 4) Hysteresis (V_{T+})−(V_{T-})		0.6	1.3	2.0	V_{DC}
V_{OUT} (0)	Logical "0" CLK R Output Voltage	I_O=360 µA V_{CC}=4.75 V_{DC}			0.4	V_{DC}
V_{OUT} (1)	Logical "1" CLK R Output Voltage	I_O=−360 µA V_{CC}=4.75 V_{DC}	2.4			V_{DC}
DATA OUTPUTS AND $\overline{INTR}$						
V_{OUT} (0)	Logical "0" Output Voltage Data Outputs $\overline{INTR}$ Output	 I_{OUT} = 1.6 mA, V_{CC}=4.75 V_{DC} I_{OUT} = 1.0 mA, V_{CC}=4.75 V_{DC}			 0.4 0.4	 V_{DC} V_{DC}
V_{OUT} (1)	Logical "1" Output Voltage	I_O=−360 µA, V_{CC}=4.75 V_{DC}	2.4			V_{DC}
V_{OUT} (1)	Logical "1" Output Voltage	I_O=−10 µA, V_{CC}=4.75 V_{DC}	4.5			V_{DC}
I_{OUT}	TRI-STATE Disabled Output Leakage (All Data Buffers)	V_{OUT}=0 V_{DC} V_{OUT}=5 V_{DC}	−3		 3	μA_{DC} μA_{DC}
I_{SOURCE}		V_{OUT} Short to Gnd, T_A=25°C	4.5	6		mA_{DC}
I_{SINK}		V_{OUT} Short to V_{CC}, T_A=25°C	9.0	16		mA_{DC}
POWER SUPPLY						
I_{CC}	Supply Current (Includes Ladder Current) ADC0801/02/03/04LCJ/05 ADC0804LCN/LCV/LCWM	f_{CLK}=640 kHz, V_{REF}/2=NC, T_A=25°C and $\overline{CS}$=5V		 1.1 1.9	 1.8 2.5	 mA mA

Note 1: Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. DC and AC electrical specifications do not apply when operating the device beyond its specified operating conditions.

Note 2: All voltages are measured with respect to Gnd, unless otherwise specified. The separate A Gnd point should always be wired to the D Gnd.

Note 3: A zener diode exists, internally, from V_{CC} to Gnd and has a typical breakdown voltage of 7 V_{DC}.

Note 4: For $V_{IN}(-) \geq V_{IN}(+)$ the digital output code will be 0000 0000. Two on-chip diodes are tied to each analog input (see block diagram) which will forward conduct for analog input voltages one diode drop below ground or one diode drop greater than the V_{CC} supply. Be careful, during testing at low V_{CC} levels (4.5V), [illegible] specs allows 50 mV forward bias of either diode. This means that as long as the analog V_{IN} does not exceed the supply voltage by more than 50 mV, the output code will be correct. To achieve an absolute 0 V_{DC} to 5 V_{DC} input voltage range will therefore require a minimum supply voltage of 4.950 V_{DC} over temperature variations, initial tolerance and loading.

Note 5: Accuracy is guaranteed at f_{CLK} = 640 kHz. At higher clock frequencies accuracy can degrade. For lower clock frequencies, the duty cycle limits can be extended so long as the minimum clock high time interval or minimum clock low time interval is no less than 275 ns.

Note 6: With an asynchronous start pulse, up to 8 clock periods may be required before the internal clock phases are proper to start the conversion process. The start request is internally latched, see *Figure 2* and section 2.0.

Note 7: The $\overline{CS}$ input is assumed to bracket the $\overline{WR}$ strobe input and therefore timing is dependent on the $\overline{WR}$ pulse width. An arbitrarily wide pulse width will hold the converter in a reset mode and the start of conversion is initiated by the low to high transition of the $\overline{WR}$ pulse (see timing diagrams).

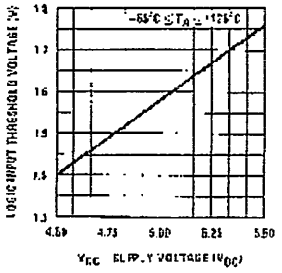
Note 8: None of these A/Ds requires a zero adjust (see section 2.5.1). To obtain zero code at other analog input voltages see section 2.5 and *Figure 5*.

Note 9: The V_{REF}/2 pin is the center point of a two-resistor divider connected from V_{CC} to ground. In all versions of the ADC0801, ADC0802, ADC0803, and ADC0805, and in the ADC0804LCJ, each resistor is typically 16 kΩ. In all versions of the ADC0804 except the ADC0804LCJ, each resistor is typically 2.2 kΩ.

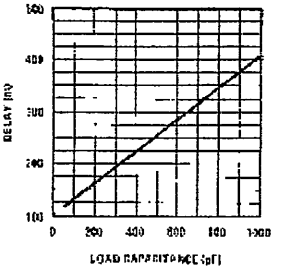
Note 10: Human body model, 100 pF discharged through a 1.5 kΩ resistor.

Typical Performance Characteristics

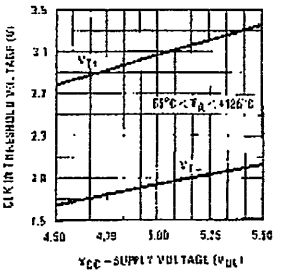
Logic Input Threshold Voltage vs. Supply Voltage



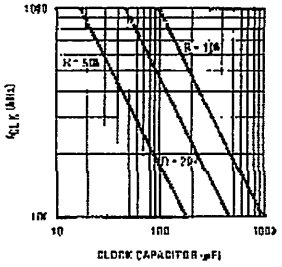
Delay From Falling Edge of $\overline{RD}$ to Output Data Valid vs. Load Capacitance



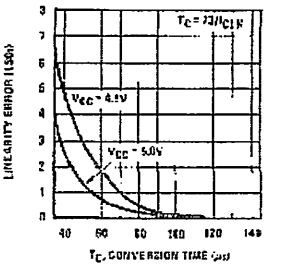
CLK IN Schmitt Trip Levels vs. Supply Voltage



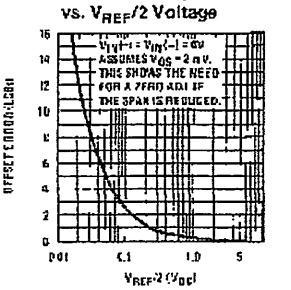
f_{CLK} vs. Clock Capacitor



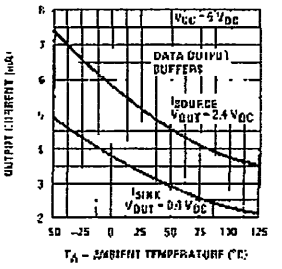
Full-Scale Error vs Conversion Time



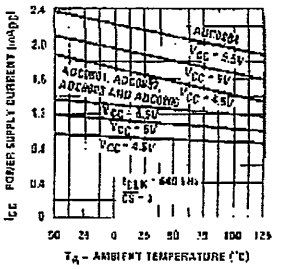
Effect of Unadjusted Offset Error vs. $V_{REF}/2$ Voltage



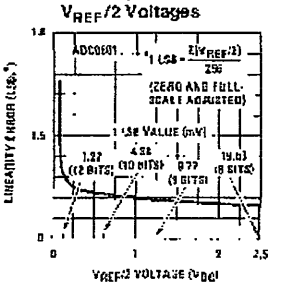
Output Current vs Temperature

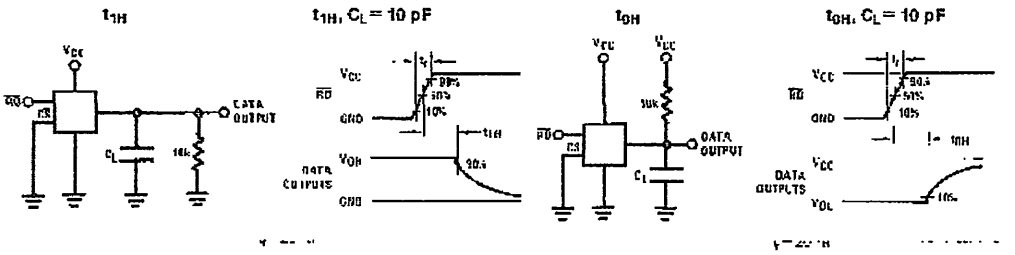


Power Supply Current vs Temperature (Note 9)

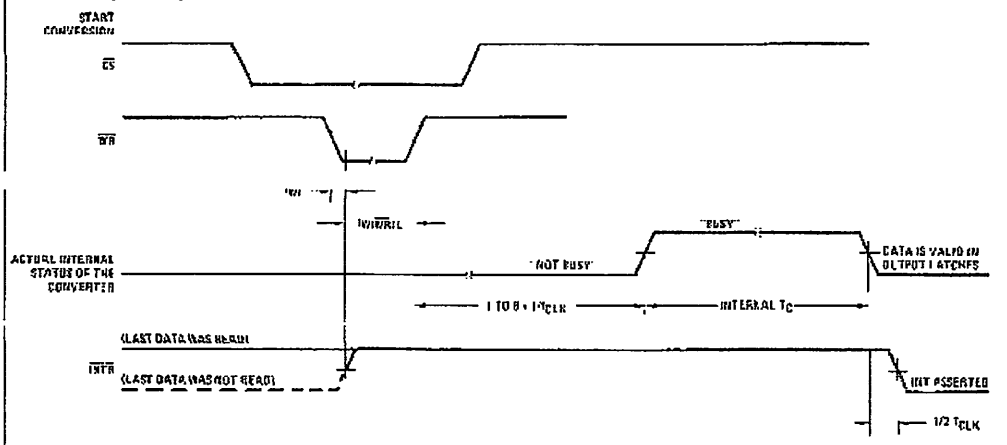


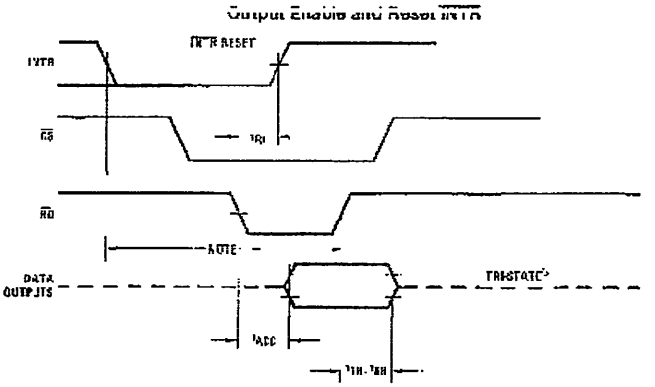
Linearity Error at Low $V_{REF}/2$ Voltages





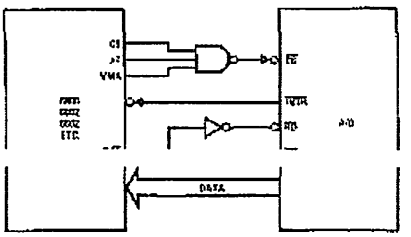
Timing Diagrams (All timing is measured from the 50% voltage points)



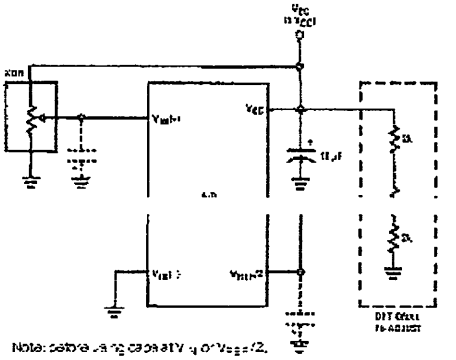


Note: Read strobe must occur 8 clock periods ($8/f_{CLK}$) after assertion of interrupt to guarantee reset of $\overline{INTR}$.

6800 Interface

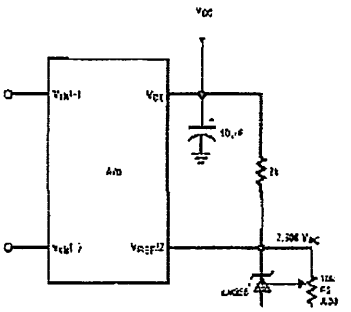


Ratiometric with Full-Scale Adjust



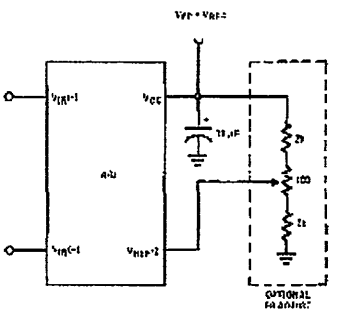
Note: Select R_1 and R_2 so that $1V < \frac{R_2}{R_1 + R_2} V_{REF} < 4V$, see section 2.0 for more details.

Absolute with a 2.500V Reference

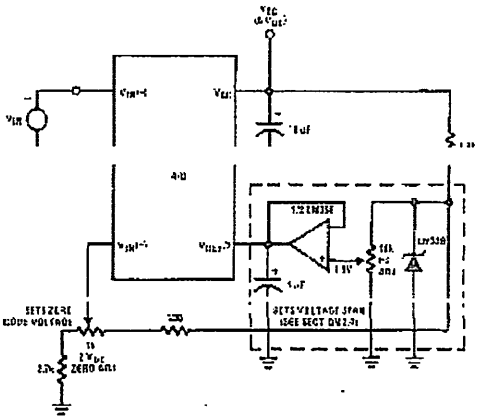


*For low power, see also LM385-2.5

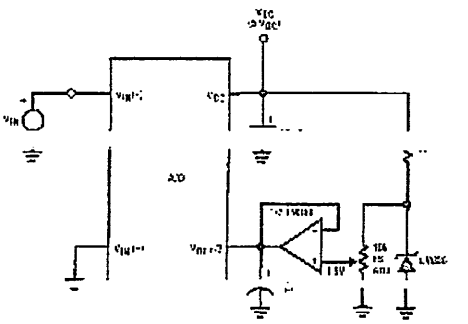
Absolute with a 5V Reference



Zero-Shift and Span Adjust: $2V \leq V_{IN} \leq 5V$

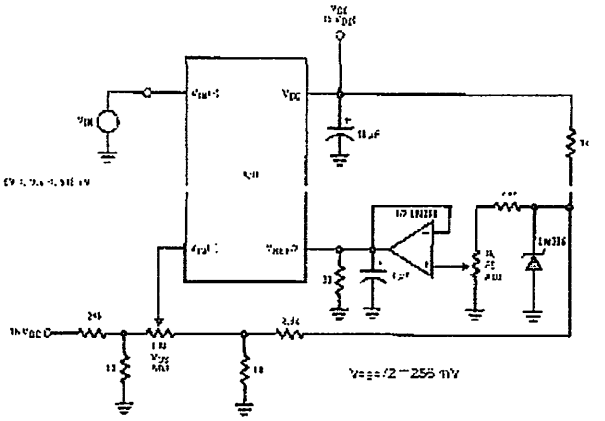


Span Adjust: $0V \leq V_{IN} \leq 3V$

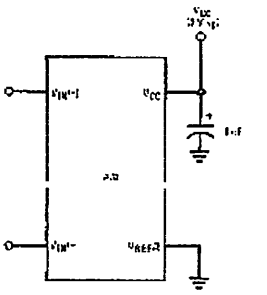


Typical Applications (Continued)

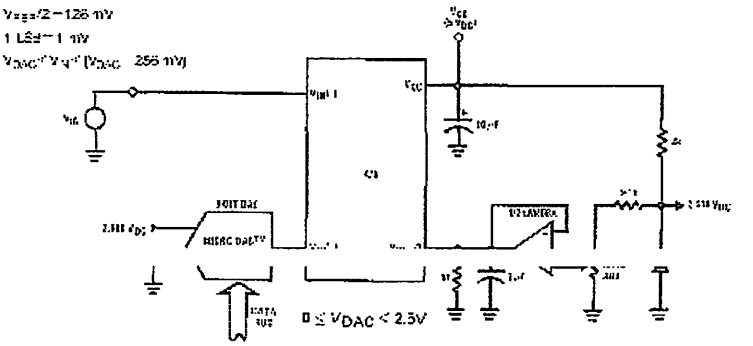
Directly Converting a Low-Level Signal



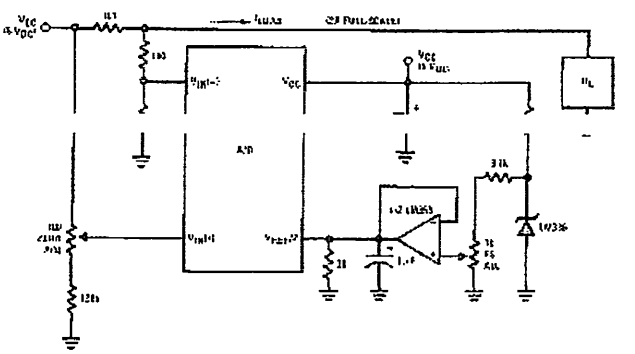
A µP Interfaced Comparator



1 mV Resolution with µP Controlled Range



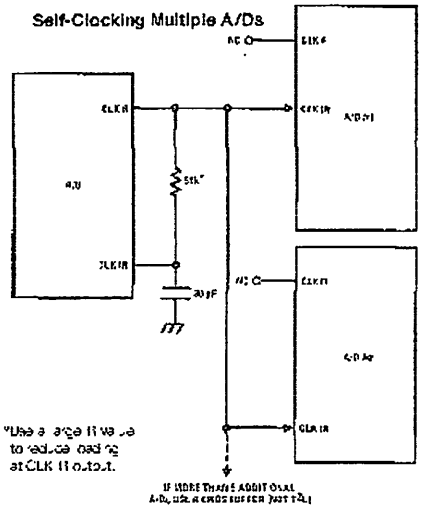
Digitizing a Current Flow



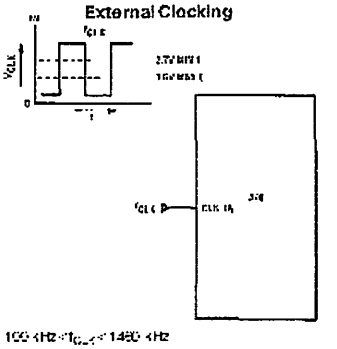
TL/H/5837/1-6

Typical Applications (Continued)

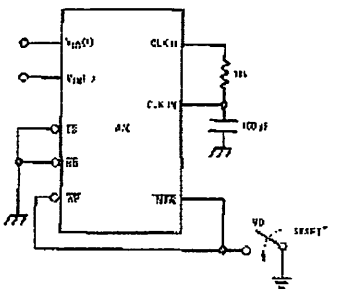
Self-Clocking Multiple A/Ds



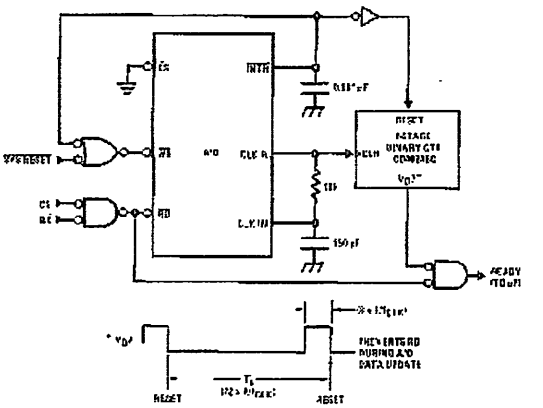
External Clocking



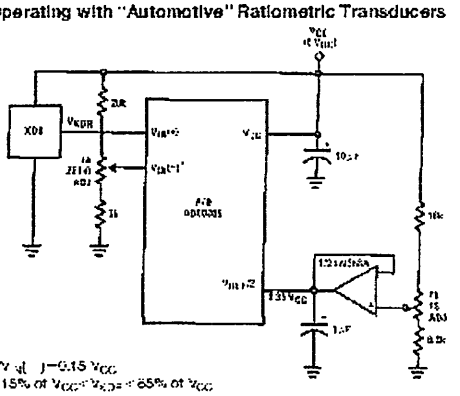
Self-Clocking in Free-Running Mode



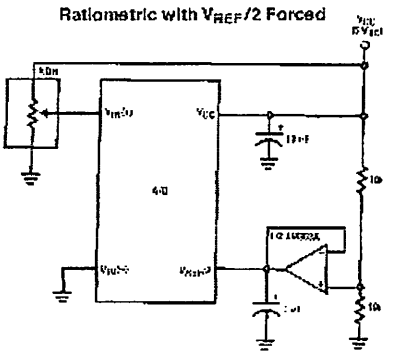
µP Interface for Free-Running A/D



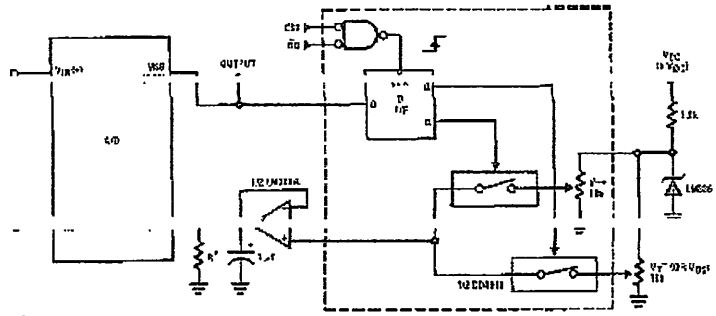
Operating with "Automotive" Ratiometric Transducers



Ratiometric with $V_{REF}/2$ Forced



µP Compatible Differential-Input Comparator with Pre-Set V_{OS} (with or without Hysteresis)

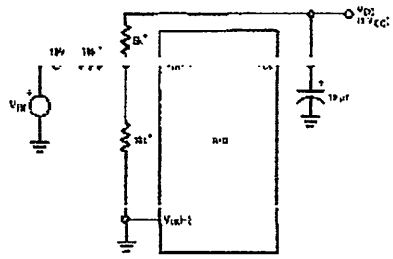


*See Figure 5 to select R value

DET = "1" for $V_{IN}(+) > V_{IN}(-)$ $(V_{REF}/2)$

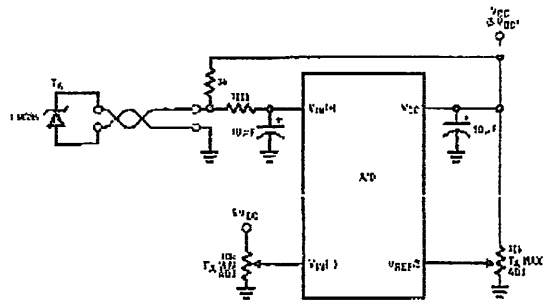
Hysteresis is not needed

Handling ± 10V Analog Inputs

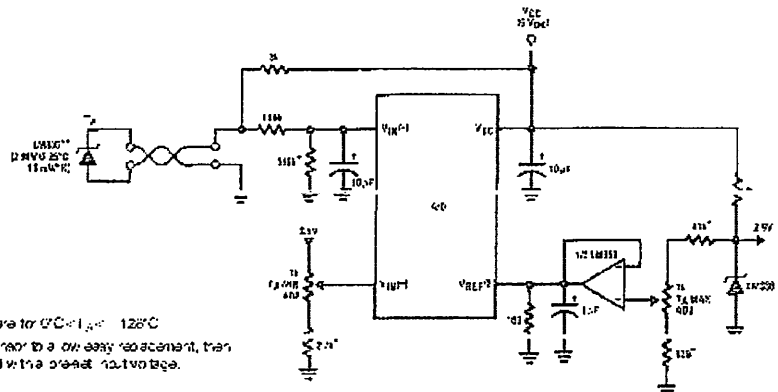


*Beckman Instruments 694G-R10K resistor array

Low-Cost, µP Interfaced, Temperature-to-Digital Converter



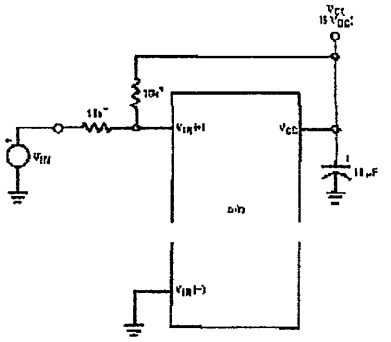
µP Interfaced Temperature-to-Digital Converter



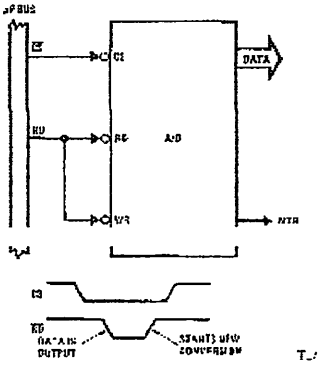
*Circuit is calibrated for 0°C ≤ T_A ≤ 125°C

**Since state each sensor is a one-step replacement, then A/D can be operated with a fixed reference.

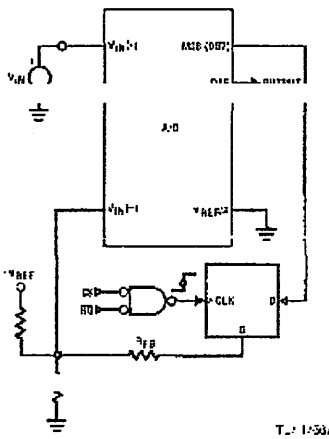
Handling ± 5V Analog Inputs



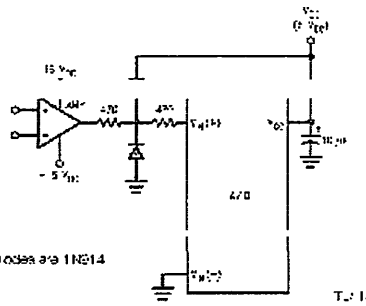
Read-Only Interface



µP Interfaced Comparator with Hysteresis

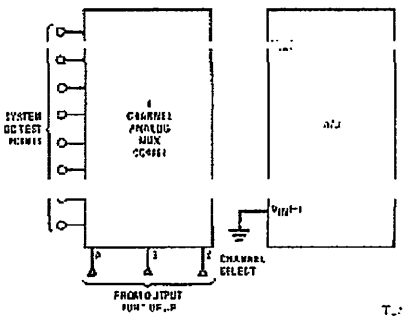


Protecting the Input

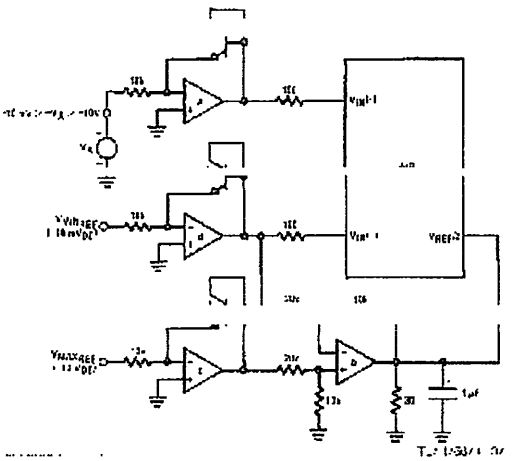


Diodes are 1N914

Analog Self-Test for a System



A Low-Cost, 3-Decade Logarithmic Converter

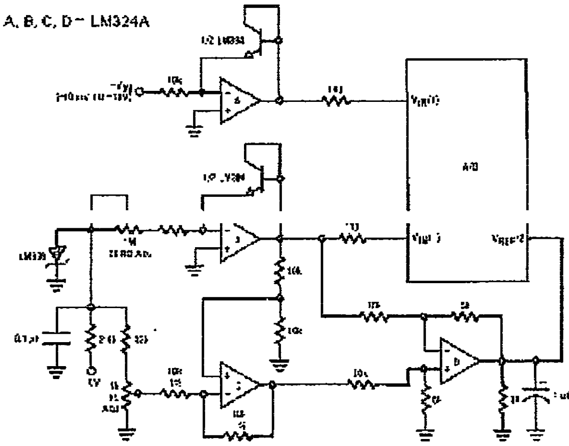


A, B, C, D = LM324A quad op amp

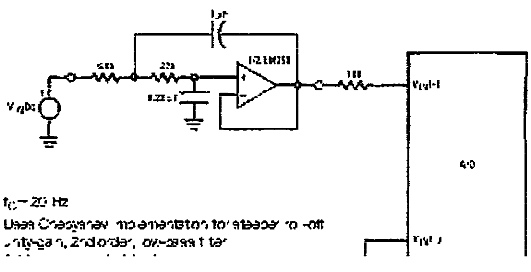
Typical Applications (Continued)

3-Decade Logarithmic A/D Converter

A, B, C, D = LM324A

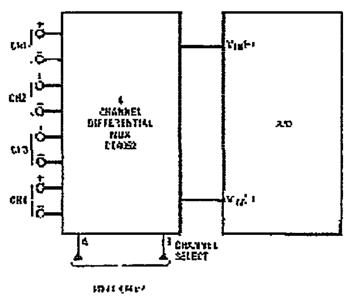


Filtering the Analog Input

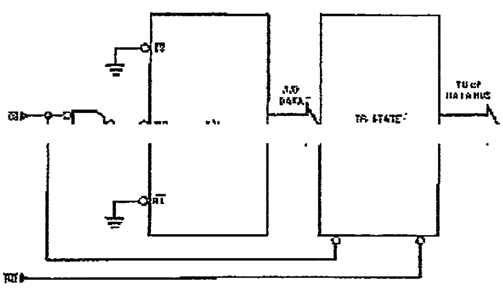


f_C = 20 Hz
Uses Chebyshev implementation for steeper roll-off unity-gain, 2nd order, low-pass filter
system response time if an analog input buffer is used

Multiplexing Differential Inputs

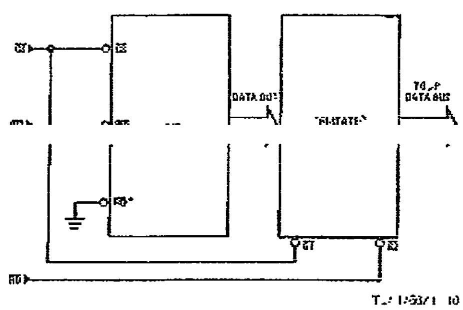


Output Buffers with A/D Data Enabled



*A/D output data is updated 1 CLK period prior to assertion of INTR

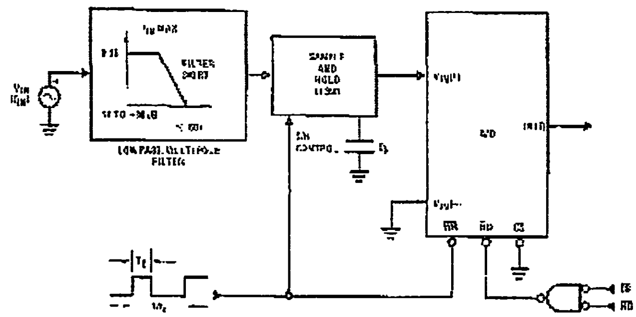
Increasing Bus Drive and/or Reducing Time on Bus



*Allows output data to set-up at falling edge of CS

Typical Applications (Continued)

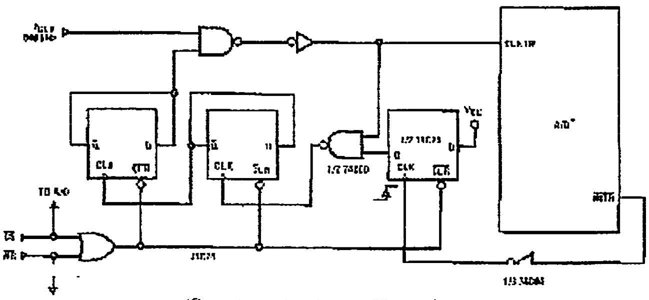
Sampling an AC Input Signal



Note 1: Oversample whenever possible [keep fs > 2f(−60)] to eliminate input frequency folding (aliasing) and to allow for the skirt response of the filter.

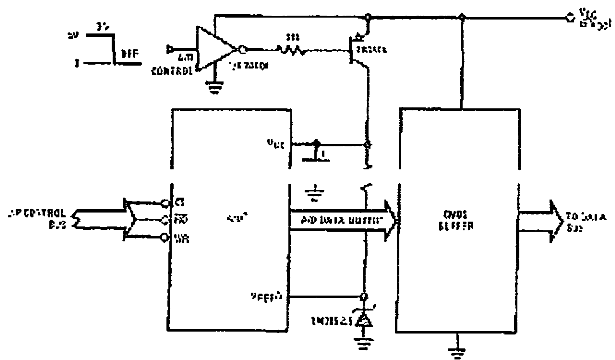
Note 2: Consider the amplitude errors which are introduced within the passband of the filter.

70% Power Savings by Clock Gating



(Complete shutdown takes ≈ 30 seconds.)

Power Savings by A/D and V_{REF} Shutdown



TL/H/5671–11

*Use ADC0801, 02, 03 or 05 for lowest power consumption.

Note: Logic inputs can be driven to V_{CC} with A/D supply at zero volts.

Buffer prevents data bus from overdriving output of A/D when in shutdown mode.

Functional Description

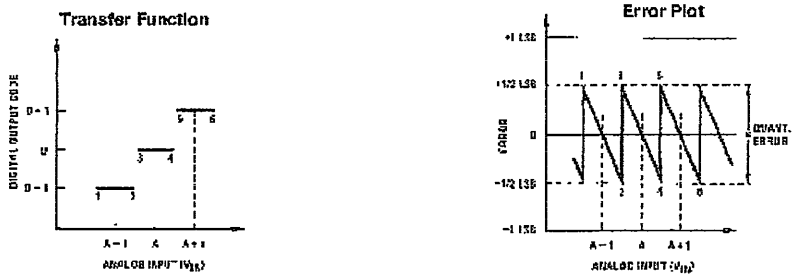
1.0 UNDERSTANDING A/D ERROR SPECS

A perfect A/D transfer characteristic (staircase waveform) is shown in *Figure 1a*. The horizontal scale is analog input voltage and the particular points labeled are in steps of 1 LSB (19.53 mV with 2.5V tied to the $V_{(+)}$/2 pin). The digital output codes that correspond to these inputs are shown as D 1, D, and D − 1. For the perfect A/D, not only will center-value (A 1, A, A − 1, ...) analog inputs produce the correct output digital codes, but also each riser (the transitions between adjacent output codes) will be located ± ½ LSB away from each center-value. As shown, the risers are ideal and have no width. Correct digital output codes will be provided for a range of analog input voltages that extend ± ½ LSB from the ideal center-values. Each tread (the range of analog input voltage that provides the same digital output code) is therefore 1 LSB wide.

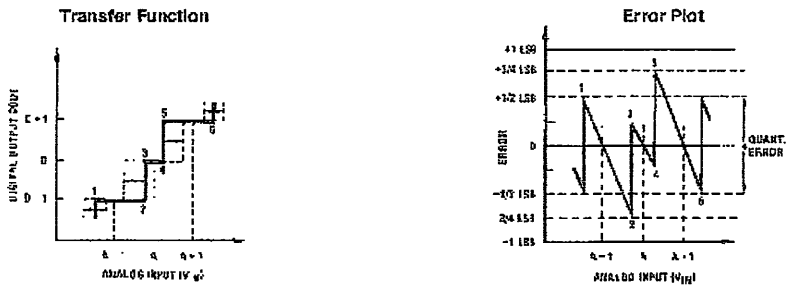
Figure 1b shows a worst case error plot for the ADC0801. All center-valued inputs are guaranteed to produce the correct output codes and the adjacent risers are guaranteed to be no closer to the center-value points than ± ½ LSB. In other words, if we apply an analog input equal to the center-value ± ½ LSB, *we guarantee* that the A/D will produce the correct digital code. The maximum range of the position of the code transition is indicated by the horizontal arrow and it is guaranteed to be no more than ½ LSB.

The error curve of *Figure 1c* shows a worst case error plot for the ADC0802. Here we guarantee that if we apply an analog input equal to the LSB analog voltage center-value the A/D will produce the correct digital code.

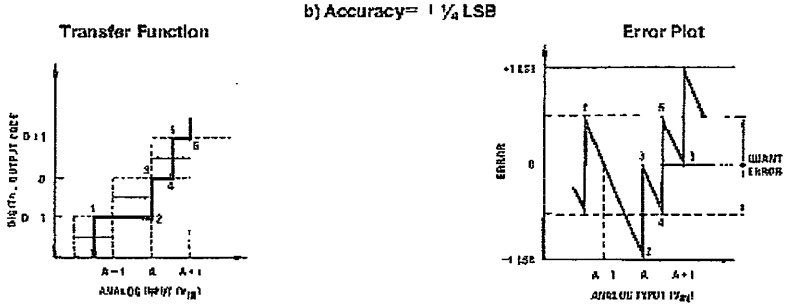
Next to each transfer function is shown the corresponding error plot. Many people may be more familiar with error plots than transfer functions. The analog input voltage to the A/D is provided by either a linear ramp or by the discrete output steps of a high resolution DAC. Notice that the error is continuously displayed and includes the quantization uncertainty of the A/D. For example the error at point 1 of *Figure 1a* is − ½ LSB because the digital code appeared ½ LSB in advance of the center-value of the tread. The error plots always have a constant negative slope and the abrupt upside steps are always 1 LSB in magnitude.



a) Accuracy = ± 0 LSB: A Perfect A/D



b) Accuracy = ± ¼ LSB



c) Accuracy = ± ½ LSB

FIGURE 1. Clarifying the Error Specs of an A/D Converter

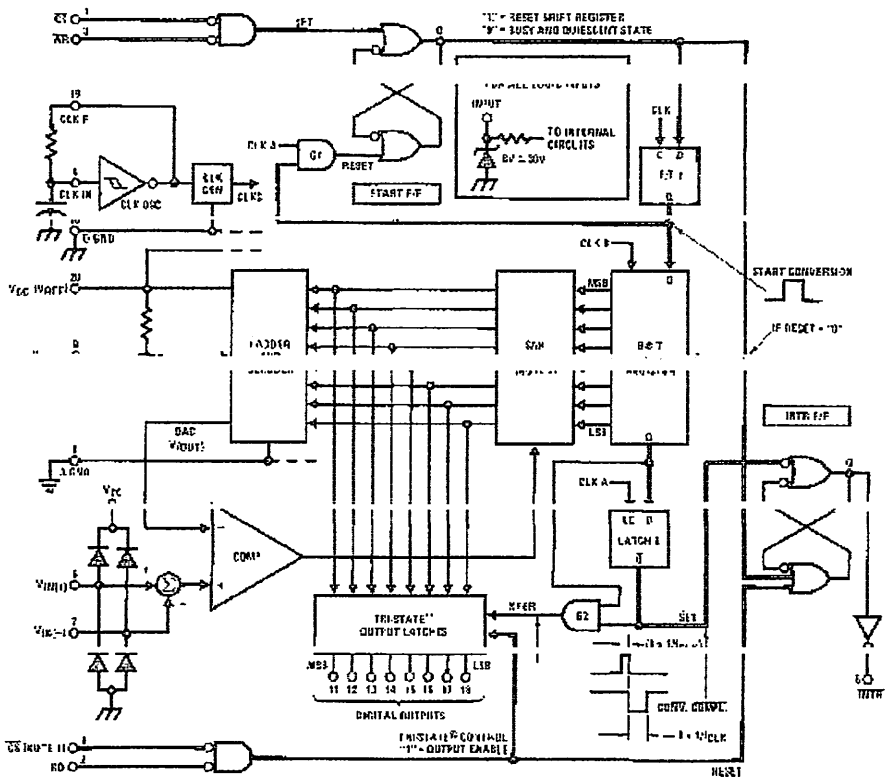
2.0 FUNCTIONAL DESCRIPTION

The ADC0801 series contains a circuit equivalent of the 256R network. Analog switches are sequenced by successive approximation logic to match the analog difference input voltage [$V_{IN}(-)$ $V_{IN}(+)$] to a corresponding tap on the R network. The most significant bit is tested first and after 8 comparisons (64 clock cycles) a digital 8-bit binary code (1111 1111 = full-scale) is transferred to an output latch and then an interrupt is asserted ($\overline{INTR}$ makes a high-to-low transition). A conversion in process can be interrupted by issuing a second start command. The device may be operated in the free-running mode by connecting $\overline{INTR}$ to the WR input with CS = 0. To ensure start-up under all possible conditions, an external $\overline{WR}$ pulse is required during the first power-up cycle.

On the high-to-low transition of the $\overline{WR}$ input the internal SAR latches and the shift register stages are reset. As long as the $\overline{CS}$ input and $\overline{WR}$ input remain low, the A/D will remain in a reset state. *Conversion will start from 1 to 8 clock periods after at least one of these inputs makes a low-to-high transition.*

A functional diagram of the A/D converter is shown in *Figure 2*. All of the package pinouts are shown and the major logic control paths are drawn in heavier weight lines.

The converter is started by having $\overline{CS}$ and $\overline{WR}$ simultaneously low. This sets the start flip-flop (F/F) and the resulting "1" level resets the 8-bit shift register, resets the Interrupt ($\overline{INTR}$) F/F and inputs a "1" to the D flop, F/F1, which is at the input end of the 8-bit shift register. Internal clock signals then transfer this "1" to the Q output of F/F1. The AND gate, G1, combines this "1" output with a clock signal to provide a reset signal to the start F/F. If the set signal is no longer present (either $\overline{WR}$ or $\overline{CS}$ is a "1") the start F/F is clocked in, which starts the conversion process. If the set signal were to still be present, this reset pulse would have no effect (both outputs of the start F/F would momentarily be at a "1" level) and the 8-bit shift register would continue to be held in the reset mode. This logic therefore allows for wide $\overline{CS}$ and $\overline{WR}$ signals and the converter will start after at least one of these signals returns high and the internal clocks again provide a reset signal for the start F/F.



Note 1: $\overline{CS}$ shown twice for clarity.

Note 2: SAR = Successive Approximation Register.

FIGURE 2. Block Diagram

After the "1" is clocked through the 8-bit shift register (which completes the SAR search) it appears as the input to the D-type latch, LATCH 1. As soon as this "1" is output from the shift register, the AND gate, G2, causes the new digital word to transfer to the TRI-STATE output latches. When LATCH 1 is subsequently enabled, the Q output makes a high-to-low transition which causes the INTR F/F to set. An inverting buffer then supplies the $\overline{\text{INTR}}$ input signal.

Note that this $\overline{\text{SET}}$ control of the INTR F/F remains low for 8 of the external clock periods (as the internal clocks run at 1/8 of the frequency of the external clock). If the data output

$\overline{\text{INTR}}$ output will still signal the end of conversion (by a high-to-low transition), because the $\overline{\text{SET}}$ input can control the Q output of the INTR F/F even though the RESET input is constantly at a "1" level in this operating mode. This $\overline{\text{INTR}}$ output will therefore stay low for the duration of the $\overline{\text{SET}}$ signal, which is 8 periods of the external clock frequency (assuming the A/D is not started during this interval).

When operating in the free-running or continuous conversion mode ($\overline{\text{INTR}}$ pin tied to $\overline{\text{WR}}$ and $\overline{\text{CS}}$ wired low—see also section 2.8), the START F/F is SET by the high-to-low transition of the $\overline{\text{INTR}}$ signal. This resets the SHIFT REGISTER which causes the input to the D-type latch, LATCH 1,

output will go high, which then allows the INTR F/F to be RESET. This reduces the width of the resulting $\overline{\text{INTR}}$ output pulse to only a few propagation delays (approximately 300 ns).

When data is to be read, the combination of both $\overline{\text{CS}}$ and $\overline{\text{RD}}$ being low will cause the INTR F/F to be reset and the TRI-STATE output latches will be enabled to provide the 8-bit digital outputs.

2.1 Digital Control Inputs

The digital control inputs ($\overline{\text{CS}}$, $\overline{\text{RD}}$, and $\overline{\text{WR}}$) meet standard T^2L logic voltage levels. These signals have been renamed when compared to the standard A/D Start and Output Enable labels. In addition, these inputs are active low to allow an easy interface to microprocessor control busses. For non-microprocessor based applications, the $\overline{\text{CS}}$ input (pin 1) can be grounded and the standard A/D Start function is obtained by an active low pulse applied at the $\overline{\text{WR}}$ input (pin 3) and the Output Enable function is caused by an active low pulse at the $\overline{\text{RD}}$ input (pin 2).

2.2 Analog Differential Voltage Inputs and Common-Mode Rejection

This A/D has additional applications flexibility due to the analog differential voltage input. The $V_{IN}(\ )$ input (pin 7) can be used to automatically subtract a fixed voltage value

4 mA–20 mA current loop conversion. In addition, common-mode noise can be reduced by use of the differential input.

The time interval between sampling $V_{IN}(-)$ and $V_{IN}(\ )$ is 4½ clock periods. The maximum error voltage due to this slight time difference between the input voltage samples is given by:

$$\Delta V_e(MAX) = (V_{pi})(2\pi f_{cm})\left(\frac{4.5}{f_{CLK}}\right).$$

where:

ΔV_e is the error voltage due to sampling delay

V_{pi} is the peak value of the common-mode voltage

f_{cm} is the common-mode frequency

As an example, to keep this error to ½ LSB (= 5 mV) when operating with a 60 Hz common-mode frequency, f_{cm}, and using a 640 kHz A/D clock, f_{CLK}, would allow a peak value of the common-mode voltage, V_{pi}, which is given by:

$$V_{pi} = \frac{[\Delta V_{e(MAX)}(f_{CLK})]}{(2\pi f_{cm})(4.5)}$$

or

$$V_{pi} = \frac{(5 \quad 10^{-3})(640 \quad 10^{3})}{(6.28)(60)(4.5)}$$

which gives

$V_{pi} = 1.9V$.

The allowed range of analog input voltages usually places more severe restrictions on input common-mode noise levels.

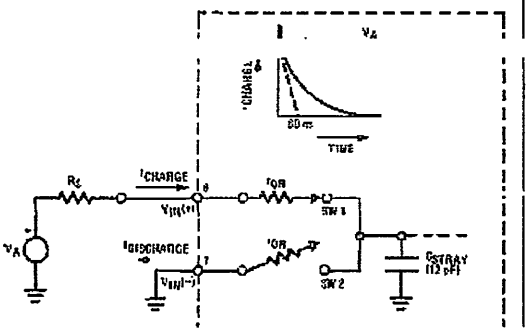
large zero offset can be handled easily by making use of the differential input (see section 2.4 Reference Voltage).

2.3 Analog Inputs

2.3.1 Input Current

Normal Mode

Due to the internal switching action, displacement currents will flow at the analog inputs. This is due to on-chip stray capacitance to ground as shown in *Figure 3*.



r_{ON} of SW 1 and SW 2 = 5 kΩ

$\tau = r_{ON} C_{STRAY} = 5\ k\Omega \times 12\ pF = 60\ ns$

FIGURE 3. Analog Input Impedance

The voltage on this capacitance is switched and will result in currents entering the $V_{IN}(-)$ input pin and leaving the $V_{IN}(\ )$ input which will depend on the analog differential input voltage levels. These current transients occur at the leading edge of the internal clocks. They rapidly decay and *do not cause errors* as the on-chip comparator is strobed at the end of the clock period.

Fault Mode

If the voltage source applied to the $V_{IN}(-)$ or $V_{IN}(\ )$ pin exceeds the allowed operating range of V_{CC} − 50 mV, large input currents can flow through a parasitic diode to the V_{CC} [illegible] spec, an external diode (1N914) should be added to bypass this current to the V_{CC} pin (with the current bypassed with this diode, the voltage at the $V_{IN}(-)$ pin can exceed the V_{CC} voltage by the forward voltage of this diode).

2.3.2 Input Bypass Capacitors

Bypass capacitors at the inputs will average these charges and cause a DC current to flow through the output resistances of the analog signal sources. This charge pumping action is worse for continuous conversions with the $V_{IN}(-)$ input voltage at full-scale. For continuous conversions with a 640 kHz clock frequency with the $V_{IN}(-)$ input at 5V, this DC current is at a maximum of approximately 5 μA. Therefore, *bypass capacitors should not be used at the analog inputs or the $V_{REF}/2$ pin* for high resistance sources (≥ 1 kΩ). If input bypass capacitors are necessary for noise filtering and high source resistance is desirable to minimize capacitor size, the detrimental effects of the voltage drop across this input resistance, which is due to the average value of the input current, can be eliminated with a full-scale adjustment while the given source resistor and input bypass capacitor are both in place. This is possible because the average value of the input current is a precise linear function of the differential input voltage.

2.3.3 Input Source Resistance

Large values of source resistance where an input bypass capacitor is not used, *will not cause errors* as the input currents settle out prior to the comparison time. If a low pass filter is required in the system, use a low valued series resistor (≤ 1 kΩ) for a passive RC section or add an op amp RC active low pass filter. For low source resistance applications, (≤ 1 kΩ), a 0.1 μF bypass capacitor at the inputs will prevent noise pickup due to series lead inductance of a long wire. A 100Ω series resistor can be used to isolate this capacitor—both the R and C are placed outside the feedback loop—from the output of an op amp, if used.

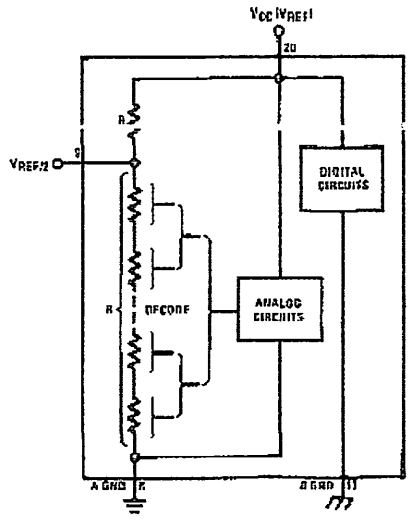
2.3.4 Noise

The leads to the analog inputs (pin 6 and 7) should be kept as short as possible to minimize input noise coupling. Both noise and undesired digital clock coupling to these inputs can cause system errors. The source resistance for these inputs should, in general, be kept below 5 kΩ. Larger values of source resistance can cause undesired system noise pickup. Input bypass capacitors, placed from the analog inputs to ground, will eliminate system noise pickup but can create analog scale errors as these capacitors will average the transient input switching currents of the A/D (see section 2.3.1.). This scale error depends on both a large source resistance and the use of an input bypass capacitor. This error can be eliminated by doing a full-scale adjustment of the A/D (adjust $V_{REF}/2$ for a proper full-scale reading—see section 2.5.2 on Full-Scale Adjustment) with the source resistance and input bypass capacitor in place.

2.4 Reference Voltage

2.4.1 Span Adjust

For maximum applications flexibility, these A/Ds have been designed to accommodate a 5 V_{DC}, 2.5 V_{DC} or an adjusted voltage reference. This has been achieved in the design of the IC as shown in *Figure 4*.



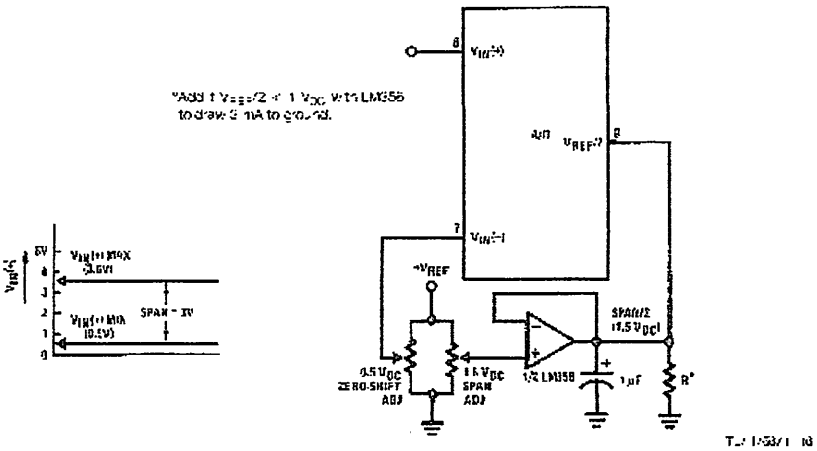
T-/ 1958/1 15

FIGURE 4. The $V_{REFERENCE}$ Design on the IC

Notice that the reference voltage for the IC is either ½ of the voltage applied to the V_{CC} supply pin, or is equal to the voltage that is externally forced at the $V_{REF}/2$ pin. This allows for a ratiometric voltage reference using the V_{CC} supply, a 5 V_{DC} reference voltage can be used for the V_{CC} supply or a voltage less than 2.5 V_{DC} can be applied to the $V_{REF}/2$ input for increased application flexibility. The internal gain to the $V_{REF}/2$ input is 2, making the full-scale differential input voltage twice the voltage at pin 9.

An example of the use of an adjusted reference voltage is to accommodate a reduced span—or dynamic voltage range of the analog input voltage. If the analog input voltage were to range from 0.5 V_{DC} to 3.5 V_{DC}, instead of 0V to 5 V_{DC}, the span would be 3V as shown in *Figure 5*. With 0.5 V_{DC} applied to the $V_{IN}(\ )$ pin to absorb the offset, the reference voltage can be made equal to ½ of the 3V span or 1.5 V_{DC}. The A/D now will encode the $V_{IN}(-)$ signal from 0.5V to 3.5 V with the 0.5V input corresponding to zero and the 3.5 V_{DC} input corresponding to full-scale. The full 8 bits of resolution are therefore applied over this reduced analog input voltage range.

Functional Description (Continued)



a) Analog Input Signal Example

b) Accommodating an Analog Input from 0.5V (Digital Out = = 00_{HEX}) to 3.5V (Digital Out = FF_{HEX})

FIGURE 5. Adapting the A/D Analog Input Voltages to Match an Arbitrary Input Signal Range

2.4.2 Reference Accuracy Requirements

The converter can be operated in a ratiometric mode or an absolute mode. In ratiometric converter applications, the magnitude of the reference voltage is a factor in both the output of the source transducer and the output of the A/D converter and therefore cancels out in the final digital output code. The ADC0805 is specified particularly for use in ratiometric applications with no adjustments required. In absolute conversion applications, both the initial value and the temperature stability of the reference voltage are important factors in the accuracy of the A/D converter. For $V_{REF}/2$ voltages of 2.4 V_{DC} nominal value, initial errors of 1 10 mV_{DC} will cause conversion errors of 1 1 LSB due to the gain of 2 of the $V_{REF}/2$ input. In reduced span applications, the initial value and the stability of the $V_{REF}/2$ input voltage become even more important. For example, if the span is reduced to 2.5V, the analog input LSB voltage value is correspondingly reduced from 20 mV (5V span) to 10 mV and 1 LSB at the $V_{REF}/2$ input becomes 5 mV. As can be seen, this reduces the allowed initial tolerance of the reference voltage and requires correspondingly less absolute change with temperature variations. Note that spans smaller than 2.5V place even tighter requirements on the initial accuracy and stability of the reference source.

In general, the magnitude of the reference voltage will require an initial adjustment. Errors due to an improper value of reference voltage appear as full-scale errors in the A/D transfer function. IC voltage regulators may be used for references if the ambient temperature changes are not excessive. The LM336B 2.5V IC reference diode (from National Semiconductor) has a temperature stability of 1.8 mV typ (6 mV max) over $0°C \leq T_A \leq -70°C$. Other temperature range parts are also available.

2.5 Errors and Reference Voltage Adjustments

2.5.1 Zero Error

The zero of the A/D does not require adjustment. If the minimum analog input voltage value, $V_{IN(MIN)}$, is not ground, a zero offset can be done. The converter can be made to output 0000 0000 digital code for this minimum input voltage by biasing the A/D $V_{IN}(\ )$ input at this $V_{IN(MIN)}$ value (see Applications section). This utilizes the differential mode operation of the A/D.

The zero error of the A/D converter relates to the location of the first riser of the transfer function and can be measured by grounding the $V_{IN}(+)$ input and applying a small magnitude positive voltage to the $V_{IN}(-)$ input. Zero error is the difference between the actual DC input voltage that is necessary to just cause an output digital code transition from 0000 0000 to 0000 0001 and the ideal ½ LSB value (½ LSB = 9.8 mV for $V_{REF}/2 = 2.500\ V_{DC}$).

2.5.2 Full-Scale

The full-scale adjustment can be made by applying a differential input voltage that is 1½ LSB less than the desired analog full-scale voltage range and then adjusting the magnitude of the $V_{REF}/2$ input (pin 9 or the V_{CC} supply if pin 9 is not used) for a digital output code that is just changing from 1111 1110 to 1111 1111.

Functional Description (Continued)

2.5.3 Adjusting for an Arbitrary Analog Input Voltage Range

If the analog zero voltage of the A/D is shifted away from ground (for example, to accommodate an analog input signal that does not go to ground) this new zero reference should be properly adjusted first. A $V_{IN}(-)$ voltage that equals this desired zero reference plus ½ LSB (where the LSB is calculated for the desired analog span, 1 LSB = analog span/256) is applied to pin 6 and the zero reference voltage at pin 7 should then be adjusted to just obtain the 00_{HEX} to 01_{HEX} code transition.

The full-scale adjustment should then be made (with the proper $V_{IN}(\ )$ voltage applied) by forcing a voltage to the $V_{IN}(-)$ input which is given by:

$$V_{IN}(-)\text{fs adj} = V_{MAX} - 1.5\left[\frac{(V_{MAX} - V_{MIN})}{256}\right],$$

where:

V_{MAX} = The high end of the analog input range

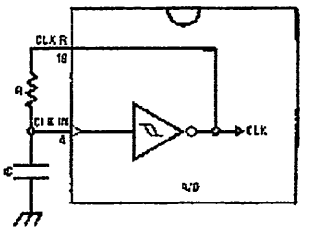
and

V_{MIN} = the low end (the offset zero) of the analog range. (Both are ground referenced.)

The $V_{REF}/2$ (or V_{CC}) voltage is then adjusted to provide a code change from FE_{HEX} to FF_{HEX}. This completes the adjustment procedure.

2.6 Clocking Option

The clock for the A/D can be derived from the CPU clock or an external RC can be added to provide self-clocking. The CLK IN (pin 4) makes use of a Schmitt trigger as shown in *Figure 6*.



$$f_{CLK} = \frac{1}{1.1\,RC}$$

$R = 10\ k\Omega$

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FIGURE 6. Self-Clocking the A/D

Heavy capacitive or DC loading of the clock R pin should be avoided as this will disturb normal converter operation. Loads less than 50 pF, such as driving up to 7 A/D converter clock inputs from a single clock R pin of 1 converter, are allowed. For larger clock line loading, a CMOS or low power TTL buffer or PNP input logic should be used to minimize the loading on the clock R pin (do not use a standard TTL buffer).

2.7 Restart During a Conversion

If the A/D is restarted ($\overline{CS}$ and $\overline{WR}$ go low and return high) during a conversion, the converter is reset and a new conversion is started. The output data latch is not updated if the conversion in process is not allowed to be completed, therefore the data of the previous conversion remains in this latch. The $\overline{INTR}$ output simply remains at the "1" level.

2.8 Continuous Conversions

For operation in the free-running mode an initializing pulse should be used, following power-up, to ensure circuit operation. In this application, the $\overline{CS}$ input is grounded and the $\overline{WR}$ input is tied to the $\overline{INTR}$ output. This $\overline{WR}$ and $\overline{INTR}$ node should be momentarily forced to logic low following a power-up cycle to guarantee operation.

2.9 Driving the Data Bus

This MOS A/D, like MOS microprocessors and memories, will require a bus driver when the total capacitance of the data bus gets large. Other circuitry, which is tied to the data bus, will add to the total capacitive loading, even in TRI-STATE (high impedance mode). Backplane bussing also greatly adds to the stray capacitance of the data bus.

There are some alternatives available to the designer to handle this problem. Basically, the capacitive loading of the data bus slows down the response time, even though DC specifications are still met. For systems operating with a relatively slow CPU clock frequency, more time is available in which to establish proper logic levels on the bus and therefore higher capacitive loads can be driven (see typical characteristics curves).

At higher CPU clock frequencies time can be extended for I/O reads (and/or writes) by inserting wait states (8080) or using clock extending circuits (6800).

Finally, if time is short and capacitive loading is high, external bus drivers must be used. These can be TRI-STATE buffers (low power Schottky such as the DM74LS240 series is recommended) or special higher drive current products which are designed as bus drivers. High current bipolar bus drivers with PNP inputs are recommended.

2.10 Power Supplies

Noise spikes on the V_{CC} supply line can cause conversion errors as the comparator will respond to this noise. A low inductance tantalum filter capacitor should be used close to the converter V_{CC} pin and values of 1 μF or greater are recommended. If an unregulated voltage is available in the system, a separate LM340LAZ-5.0, TO-92, 5V voltage regulator for the converter (and other analog circuitry) will greatly reduce digital noise on the V_{CC} supply.

2.11 Wiring and Hook-Up Precautions

Standard digital wire wrap sockets are not satisfactory for breadboarding this A/D converter. Sockets on PC boards can be used and all logic signal wires and leads should be grouped and kept as far away as possible from the analog signal leads. Exposed leads to the analog inputs can cause undesired digital noise and hum pickup, therefore shielded leads may be necessary in many applications.

Functional Description (Continued)

A single point analog ground that is separate from the logic ground points should be used. The power supply bypass capacitor and the self-clocking capacitor (if used) should both be returned to digital ground. Any $V_{REF}/2$ bypass capacitors, analog input filter capacitors, or input signal shielding should be returned to the analog ground point. A test for proper grounding is to measure the zero error of the A/D converter. Zero errors in excess of ½ LSB can usually be traced to improper board layout and wiring (see section 2.5.1 for measuring the zero error).

3.0 TESTING THE A/D CONVERTER

There are many degrees of complexity associated with testing an A/D converter. One of the simplest tests is to apply a known analog input voltage to the converter and use LEDs to display the resulting digital output code as shown in *Figure 7*.

For ease of testing, the $V_{REF}/2$ (pin 9) should be supplied with 2.560 V_{DC} and a V_{CC} supply voltage of 5.12 V_{DC} should be used. This provides an LSB value of 20 mV.

If a full-scale adjustment is to be made, an analog input voltage of 5.090 V_{DC} (5.120−1½ LSB) should be applied to the $V_{IN}(-)$ pin with the $V_{IN}(\ )$ pin grounded. The value of the $V_{REF}/2$ input voltage should then be adjusted until the digital output code is just changing from 1111 1110 to 1111 1111. This value of $V_{REF}/2$ should then be used for all the tests.

The digital output LED display can be decoded by dividing the 8 bits into 2 hex characters, the 4 most significant (MS) and the 4 least significant (LS). Table I shows the fractional binary equivalent of these two 4-bit groups. By adding the voltages obtained from the "VMS" and "VLS" columns in Table I, the nominal value of the digital display (when $V_{REF}/2$ = 2.560V) can be determined. For example, for an output LED display of 1011 0110 or B6 (in hex), the voltage values from the table are 3.520 + 0.120 or 3.640 V_{DC}. These voltage values represent the center-values of a perfect A/D converter. The effects of quantization error have to be accounted for in the interpretation of the test results.

For a higher speed test system, or to obtain plotted data, a digital-to-analog converter is needed for the test set-up. An accurate 10-bit DAC can serve as the precision voltage source for the A/D. Errors of the A/D under test can be expressed as either analog voltages or differences in 2 digital words.

A basic A/D tester that uses a DAC and provides the error as an analog output voltage is shown in *Figure 8*. The 2 op amps can be eliminated if a lab DVM with a numerical subtraction feature is available to read the difference voltage, "A−C", directly. The analog input voltage can be supplied by a low frequency ramp generator and an X-Y plotter can be used to provide analog error (Y axis) versus analog input (X axis).

For operation with a microprocessor or a computer-based test system, it is more convenient to present the errors digitally. This can be done with the circuit of *Figure 9*, where the output code transitions can be detected as the 10-bit DAC is incremented. This provides ½ LSB steps for the 8-bit A/D under test. If the results of this test are automatically plotted with the analog input on the X axis and the error (in LSB's) as the Y axis, a useful transfer function of the A/D under test results. For acceptance testing, the plot is not necessary and the testing speed can be increased by establishing internal limits on the allowed error for each code.

4.0 MICROPROCESSOR INTERFACING

To discuss the interface with 8080A and 6800 microprocessors, a common sample subroutine structure is used. The microprocessor starts the A/D, reads and stores the results of 16 successive conversions, then returns to the user's program. The 16 data bytes are stored in 16 successive memory locations. All Data and Addresses will be given in hexadecimal form. Software and hardware details are provided separately for each type of microprocessor.

4.1 Interfacing 8080 Microprocessor Derivatives (8048, 8085)

This converter has been designed to directly interface with derivatives of the 8080 microprocessor. The A/D can be mapped into memory space (using standard memory address decoding for $\overline{CS}$ and the $\overline{MEMR}$ and $\overline{MEMW}$ strobes) or it can be controlled as an I/O device by using the $\overline{I/O\ R}$ and $\overline{I/O\ W}$ strobes and decoding the address bits A0 → A7 (or address bits A8 → A15 as they will contain the same 8-bit address information) to obtain the $\overline{CS}$ input. Using the I/O space provides 256 additional addresses and may allow a simpler 8-bit address decoder but the data can only be input to the accumulator. To make use of the additional memory reference instructions, the A/D should be mapped into memory space. An example of an A/D in I/O space is shown in *Figure 10*.

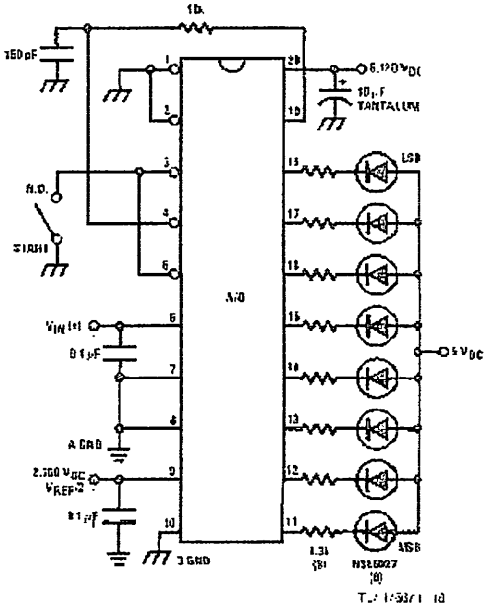

FIGURE 7. Basic A/D Tester

Functional Description (Continued)

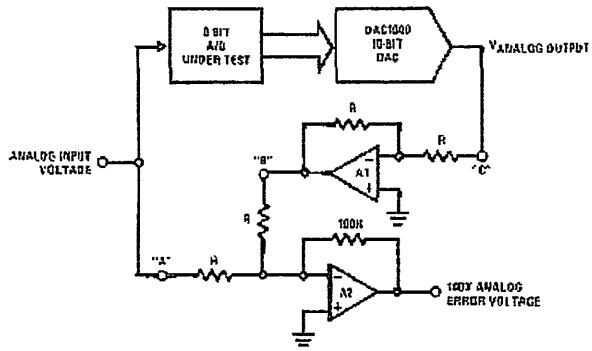

FIGURE 8. A/D Tester with Analog Error Output

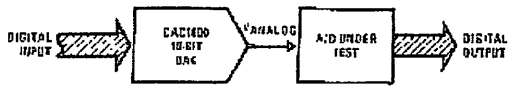

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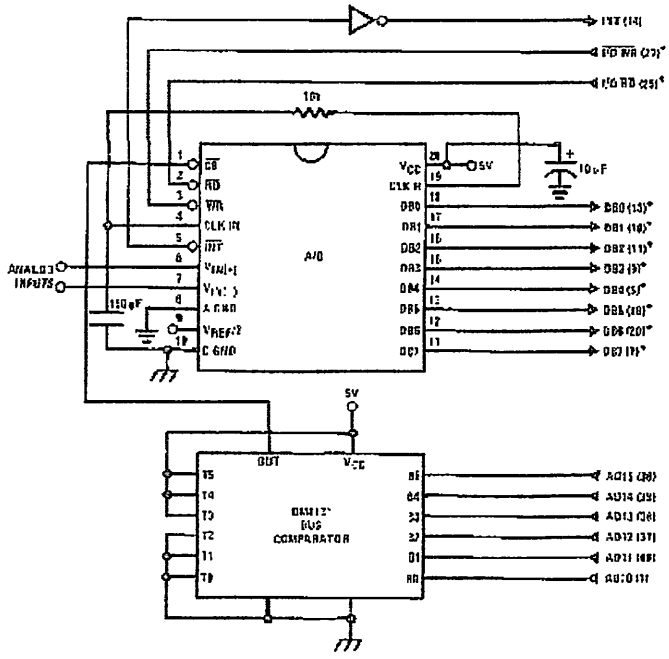
FIGURE 9. Basic "Digital" A/D Tester

TABLE I. DECODING THE DIGITAL OUTPUT LEDs

HEX	BINARY	FRACTIONAL BINARY VALUE FOR		OUTPUT VOLTAGE CENTER VALUES WITH $V_{REF}/2 = 2.560\ V_{DC}$	
		MS GROUP	LS GROUP	VMS GROUP*	VLS GROUP*
F	1 1 1 1	15/16	15/256	4.800	0.300
E	1 1 1 0	7/8	7/128	4.480	0.280
D	1 1 0 1	13/16	13/256	4.160	0.260
C	1 1 0 0	3/4	3/64	3.840	0.240
B	1 0 1 1	11/16	11/256	3.520	0.220
A	1 0 1 0	5/8	5/128	3.200	0.200
9	1 0 0 1	9/16	9/256	2.880	0.180
8	1 0 0 0	1/2	1/32	2.560	0.160
7	0 1 1 1	7/16	7/256	2.240	0.140
6	0 1 1 0	3/8	3/128	1.920	0.120
5	0 1 0 1	5/16	2/256	1.600	0.100
4	0 1 0 0	1/4	1/64	1.280	0.080
3	0 0 1 1	3/16	3/256	0.960	0.060
2	0 0 1 0	1/8	1/128	0.640	0.040
1	0 0 0 1	1/16	1/256	0.320	0.020
0	0 0 0 0			0	0

*Decay Output—VMS Group VLS Group

Functional Description (Continued)



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Note 1: "H" is necessary for the DP8228 system controller, others are INS8080A.

Note 2: Pin 28 of the INS8228 must be tied to +12V through a 1 kΩ resistor to generate the RST 7 instruction when an interrupt is acknowledged as required by the accompanying sample program.

FIGURE 10. ADC0801–INS8080A CPU Interface

SAMPLE PROGRAM FOR *FIGURE 10* ADC0801–INS8080A CPU INTERFACE

```
0038    C3 00 03    RST 7:      JMP     LD DATA
  •       •           •
  •       •           •
0100    21 00 02    START:      LXI H 0200H         ;HL pair will point to
                                                    ;data storage locations
0103    31 00 04    RETURN:     LXI SP 0400H        ;Initialize stack pointer (Note 1)
0106    7D                      MOV A, L            ;Test # of bytes entered
0107    FE 0F                   CPI 0FH             ;If # = 16, JMP to
0109    CA 13 01                JZ CONT             ;user program
010C    D3 E0                   OUT E0 H            ;Start A/D
010E    FB                      EI                  ;Enable interrupt
010F    00          LOOP:       NOP                 ;Loop until end of
0110    C3 0F 01                JMP LOOP            ;conversion
0113      •         CONT:         •
  •       •           •           •
  •       •         (User program to                •
  •       •         process data)                   •
  •       •           •           •
  •       •           •           •
0300    DB E0       LD DATA:    IN E0 H             ;Load data into accumulator
0302    77                      MOV M, A            ;Store data
0303    23                      INX H               ;Increment storage pointer
0304    C3 03 01                JMP RETURN
```

Note 1: The stack pointer must be initialized because a RST 7 instruction pushes the PC onto the stack.

Note 2: All address used were arbitrarily chosen.

Functional Description (Continued)

The standard control bus signals of the 8080 $\overline{CS}$, $\overline{RD}$ and $\overline{WR}$) can be directly wired to the digital control inputs of the A/D and the bus timing requirements are met to allow both starting the converter and outputting the data onto the data bus. A bus driver should be used for larger microprocessor systems where the data bus leaves the PC board and/or must drive capacitive loads larger than 100 pF.

4.1.1 Sample 8080A CPU Interfacing Circuitry and Program

The following sample program and associated hardware shown in *Figure 10* may be used to input data from the converter to the INS8080A CPU chip set (comprised of the INS8080A microprocessor, the INS8228 system controller and the INS8224 clock generator). For simplicity, the A/D is controlled as an I/O device, specifically an 8-bit bi-directional port located at an arbitrarily chosen port address, E0. The TRI-STATE output capability of the A/D eliminates the need for a peripheral interface device, however address decoding is still required to generate the appropriate $\overline{CS}$ for the converter.

It is important to note that in systems where the A/D converter is 1-of-8 or less I/O mapped devices, no address decoding circuitry is necessary. Each of the 8 address bits (A0 to A7) can be directly used as $\overline{CS}$ inputs—one for each I/O device.

4.1.2 INS8048 Interface

The INS8048 interface technique with the ADC0801 series (see *Figure 11*) is simpler than the 8080A CPU interface. There are 24 I/O lines and three test input lines in the 8048. With these extra I/O lines available, one of the I/O lines (bit 0 of port 1) is used as the chip select signal to the A/D, thus eliminating the use of an external address decoder. Bus control signals $\overline{RD}$, $\overline{WR}$ and $\overline{INT}$ of the 8048 are tied directly to the A/D. The 16 converted data words are stored at on-chip RAM locations from 20 to 2F (Hex). The $\overline{RD}$ and $\overline{WR}$ signals are generated by reading from and writing into a dummy address, respectively. A sample interface program is shown below.

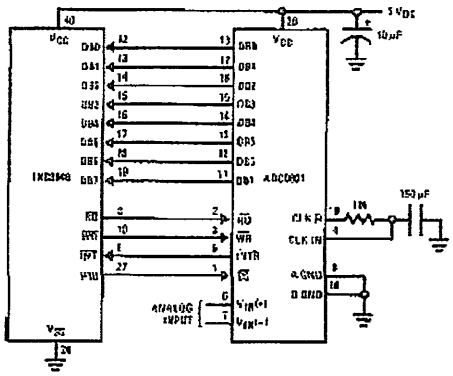

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FIGURE 11. INS8048 Interface

SAMPLE PROGRAM FOR *FIGURE 11* INS8048 INTERFACE

```
04 10              JMP     10H          ;Program starts at addr 10
                   ORG     3H
04 50              JMP     50H          ;Interrupt jump vector
                   ORG     10H          ;Main program
99 FE              ANL     P1,#0FEH     ;Chip select
81                 MOVX    A,@R1        ;Read in the 1st data
                                        ;to reset the intr
89 01      START:  ORL     P1,#1        ;Set port pin high
B8 20              MOV     R0,#20H      ;Data address
B9 FF              MOV     R1,#0FFH     ;Dummy address
BA 10              MOV     R2,#10H      ;Counter for 16 bytes
23 FF      AGAIN:  MOV     A,#0FFH      ;Set ACC for intr loop
99 FE              ANL     P1,#0FEH     ;Send CS (bit 0 of P1)
91                 MOVX    @R1,A        ;Send WR out
05                 EN      I            ;Enable interrupt
96 21      LOOP:   JNZ     LOOP         ;Wait for interrupt
EA 13              DJNZ    R2,AGAIN     ;If 16 bytes are read
00                 NOP                  ;go to user's program
00                 NOP
                   ORG     50H
81         INDATA: MOVX    A,@R1        ;Input data, CS still low
A0                 MOV     @R0,A        ;Store in memory
18                 INC     R0           ;Increment storage counter
89 01              ORL     P1,#1        ;Reset CS signal
27                 CLR     A            ;Clear ACC to get out of
93                 RETR                 ;the interrupt loop
```

Functional Description (Continued)

4.2 Interfacing the Z-80

The Z-80 control bus is slightly different from that of the 8080. General $\overline{RD}$ and $\overline{WR}$ strobes are provided and separate memory request, $\overline{MREQ}$, and I/O request, $\overline{IORQ}$, signals are used which have to be combined with the generalized strobes to provide the equivalent 8080 signals. An advantage of operating the A/D in I/O space with the Z-80 is that the CPU will automatically insert one wait state (the $\overline{RD}$ and $\overline{WR}$ strobes are extended one clock period) to allow more time for the I/O devices to respond. Logic to map the A/D in I/O space is shown in *Figure 13*.

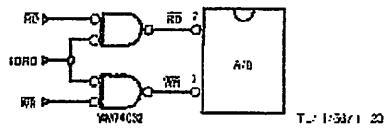


FIGURE 13. Mapping the A/D as an I/O Device for Use with the Z-80 CPU

Additional I/O advantages exist as software DMA routines are available and use can be made of the output data transfer which exists on the upper 8 address lines (A8 to A15) during I/O input instructions. For example, MUX channel selection for the A/D can be accomplished with this operating mode.

4.3 Interfacing 6800 Microprocessor Derivatives (6502, etc.)

The control bus for the 6800 microprocessor derivatives does not use the $\overline{RD}$ and $\overline{WR}$ strobe signals. Instead it employs a single R/$\overline{W}$ line and additional timing, if needed, can be derived fom the $\phi 2$ clock. All I/O devices are memory mapped in the 6800 system, and a special signal, VMA, indicates that the current address is valid. *Figure 14* shows an interface schematic where the A/D is memory mapped in the 6800 system. For simplicity, the $\overline{CS}$ decoding is shown using ½ DM8092. Note that in many 6800 systems, an already decoded $\overline{475}$ line is brought out to the common bus at pin 21. This can be tied directly to the $\overline{CS}$ pin of the A/D, provided that no other devices are addressed at HEX ADDR: 4XXX or 5XXX.

The following subroutine performs essentially the same function as in the case of the 8080A interface and it can be called from anywhere in the user's program.

In *Figure 15* the ADC0801 series is interfaced to the M6800 microprocessor through (the arbitrarily chosen) Port B of the MC6820 or MC6821 Peripheral Interface Adapter, (PIA). Here the $\overline{CS}$ pin of the A/D is grounded since the PIA is already memory mapped in the M6800 system and no $\overline{CS}$ decoding is necessary. Also notice that the A/D output data lines are connected to the microprocessor bus under program control through the PIA and therefore the A/D $\overline{RD}$ pin can be grounded.

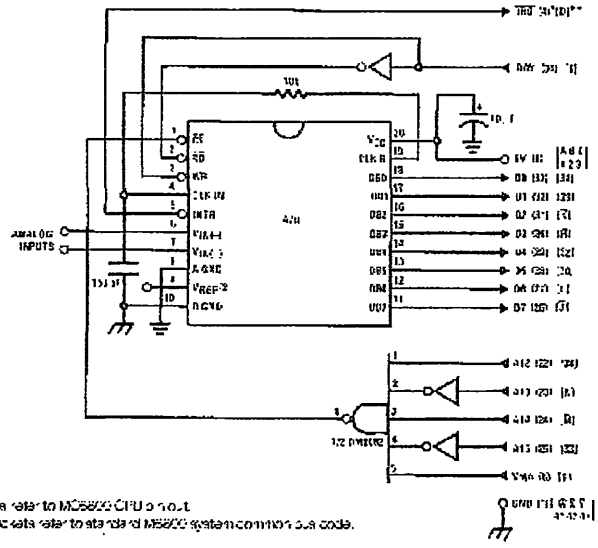
A sample interface program equivalent to the previous one is shown below *Figure 15*. The PIA Data and Control Registers of Port B are located at HEX addresses 8006 and 8007, respectively.

5.0 GENERAL APPLICATIONS

The following applications show some interesting uses for the A/D. The fact that one particular microprocessor is used is not meant to be restrictive. Each of these application circuits would have its counterpart using any microprocessor that is desired.

5.1 Multiple ADC0801 Series to MC6800 CPU Interface

To transfer analog data from several channels to a single microprocessor system, a multiple converter scheme presents several advantages over the conventional multiplexer single-converter approach. With the ADC0801 series, the differential inputs allow individual span adjustment for each channel. Furthermore, all analog input channels are sensed simultaneously, which essentially divides the microprocessor's total system servicing time by the number of channels, since all conversions occur simultaneously. This scheme is shown in *Figure 16*.



Note 1: Numbers in circles refer to MC6800 CPU pin out.
Note 2: Numbers or letters in circles refer to standard M6800 system common bus code.

FIGURE 14. ADC0801-MC6800 CPU Interface

Functional Description (Continued)

SAMPLE PROGRAM FOR *FIGURE 14* ADC0801-MC6800 CPU INTERFACE

```
0010  DF 36     DATAIN  STX   TEMP2   ;Save contents of X
0012  CE 00 2C        LDX   #$002C    ;Upon INT low CPU
0015  FF FF F8        STX   $FFF8     ;jumps to 002C
0018  B7 50 00        STAA  $5000     ;Start ADC0801
001B  0E              CLI
001C  3E        CONVRT  WAI           ;Wait for interrupt
001D  DE 34           LDX   TEMP1
001F  8C 02 0F        CPX   #$020F    ;Is final data stored?
0022  27 14           BEQ   ENDP
0024  B7 50 00        STAA  $5000     ;Restarts ADC0801
0027  08              INX
0028  DF 34           STX   TEMP1
002A  20 F0           BRA   CONVRT
002C  DE 34     INTRPT  LDX   TEMP1
002E  B6 50 00        LDAA  $5000     ;Read data
0031  A7 00           STAA  X         ;Store it at X
0033  3B              RTI
0034  02 00     TEMP1   FDB   $0200    ;Starting address for
                                      ;data storage
0036  00 00     TEMP2   FDB   $0000
0038  CE 02 00  ENDP    LDX   #$0200    ;Reinitialize TEMP1
003B  DF 34           STX   TEMP1
003D  DE 36           LDX   TEMP2
003F  39              RTS             ;Return from subroutine
                                      ;To user's program
```

Note 1: In order for the microprocessor to service subroutines and interrupts, the stack pointer must be determined in the user's program.

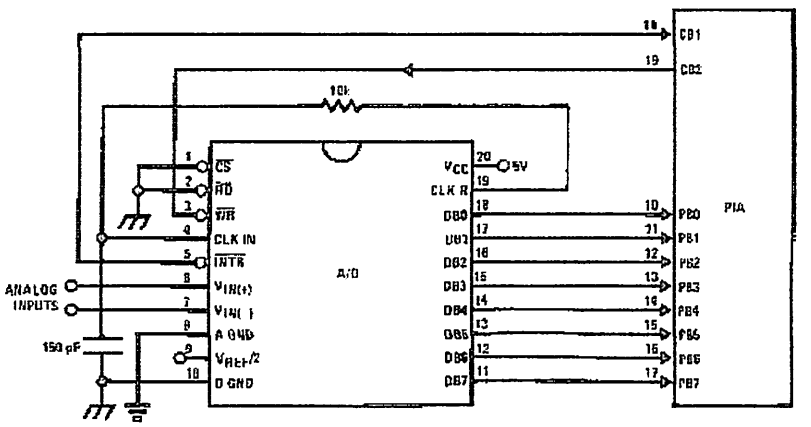


FIGURE 15. ADC0801–MC6820 PIA Interface

Functional Description (Continued)

SAMPLE PROGRAM FOR *FIGURE 15* ADC0801–MC6820 PIA INTERFACE

```
0010  CE 00 38     DATAIN   LDX   #$0038     ; Upon IRQ low CPU
0013  FF FF F8              STX   $FFF8      ; jumps to 0038
0016  B6 80 06              LDAA  PIAORB     ; Clear possible IRQ flags
0019  4F                    CLRA
001A  B7 80 07              STAA  PIACRB
001D  B7 80 06              STAA  PIAORB     ; Set Port B as input
0020  0E                    CLI
0021  C6 34                 LDAB  #$34
0023  86 3D                 LDAA  #$3D
0025  F7 80 07     CONVRT   STAB  PIACRB     ; Starts ADC0801
0028  B7 80 07              STAA  PIACRB
002B  3E                    WAI              ; Wait for interrupt
002C  DE 40                 LDX   TEMP1
002E  8C 02 0F              CPX   #$020F     ; Is final data stored?
0031  27 0F                 BEQ   END?
0033  08                    INX
0034  DF 40                 STX   TEMP1
0036  20 ED                 BRA   CONVRT
0038  DE 40        INTRPT   LDX   TEMP1
003A  B6 80 06              LDAA  PIAORB     ; Read data in
003D  A7 00                 STAA  X          ; Store it at X
003F  3B                    RTI
0040  02 00        TEMP1    FDB   $0200      ; Starting address for
                                             ; data storage
0042  CE 02 00     END?     LDX   #$0200     ; Reinitialize TEMP1
0045  DF 40                 STX   TEMP1
0047  39                    RTS              ; Return from subroutine
                   PIAORB   EQU   $8006      ; To user's program
                   PIACRB   EQU   $8007
```

The following schematic and sample subroutine (DATA IN) may be used to interface (up to) 8 ADC0801's directly to the MC6800 CPU. This scheme can easily be extended to allow the interface of more converters. In this configuration the converters are (arbitrarily) located at HEX address 8000 in the MC6800 memory space. To save components, the clock signal is derived from just one RC pair on the first converter. This output drives the other A/Ds.

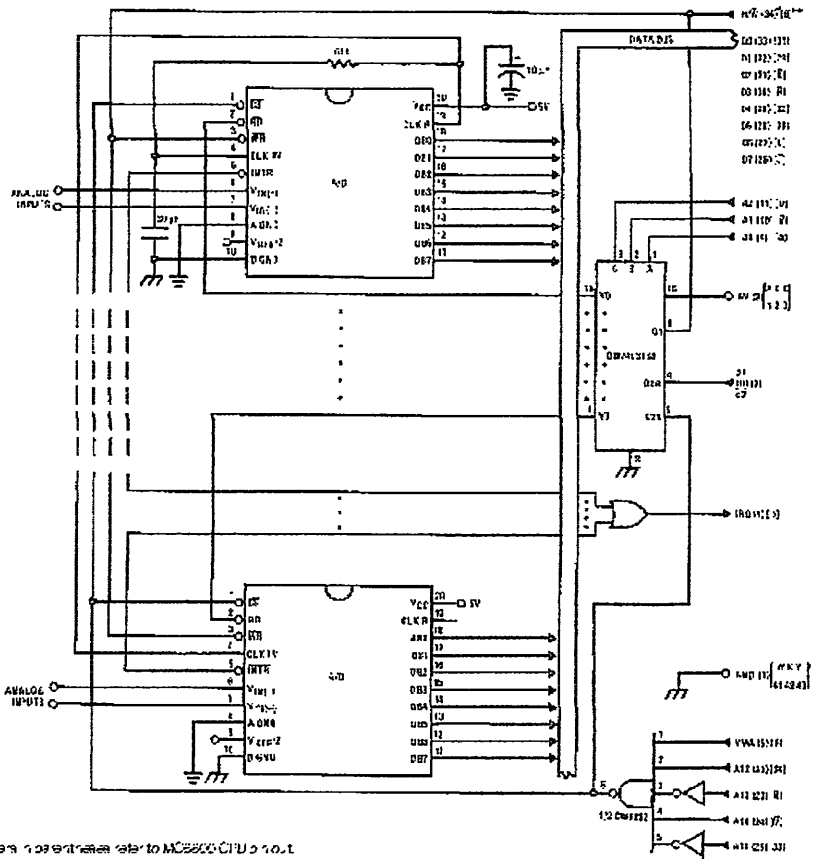
All the converters are started simultaneously with a STORE instruction at HEX address 8000. Note that any other HEX address of the form 8XXX will be decoded by the circuit, pulling all the $\overline{CS}$ inputs low. This can easily be avoided by using a more definitive address decoding scheme. All the interrupts are ORed together to insure that all A/Ds have completed their conversion before the microprocessor is interrupted.

The subroutine, DATA IN, may be called from anywhere in the user's program. Once called, this routine initializes the CPU, starts all the converters simultaneously and waits for the interrupt signal. Upon receiving the interrupt, it reads the converters (from HEX addresses 8000 through 8007) and stores the data successively at (arbitrarily chosen) HEX addresses 0200 to 0207, before returning to the user's program. All CPU registers then recover the original data they had before servicing DATA IN.

5.2 Auto-Zeroed Differential Transducer Amplifier and A/D Converter

The differential inputs of the ADC0801 series eliminate the need to perform a differential to single ended conversion for a differential transducer. Thus, one op amp can be eliminated since the differential to single ended conversion is provided by the differential input of the ADC0801 series. In general, a transducer preamp is required to take advantage of the full A/D converter input dynamic range.

Functional Description (Continued)



Note 1: N…

Note 2: N…

T…

FIGURE 16. Interfacing Multiple A/Ds in an MC6800 System

SAMPLE PROGRAM FOR *FIGURE 16* INTERFACING MULTIPLE A/Ds IN AN MC6800 SYSTEM

ADDRESS	HEX CODE		MNEMONICS		COMMENTS
0010	DF 44	DATAIN	STX	TEMP	;Save Contents of X
0012	CE 00 2A		LDX	#$002A	;Upon $\overline{IRQ}$ LOW CPU
0015	FF FF F8		STX	$FFF8	;Jumps to 002A
0018	B7 50 00		STAA	$5000	;Starts all A/D's
001B	0E		CLI		
001C	3E		WAI		;Wait for interrupt
001D	CE 50 00		LDX	#$5000	
0020	DF 40		STX	INDEX1	;Reset both INDEX
0022	CE 02 00		LDX	#$0200	;1 and 2 to starting
0025	DF 42		STX	INDEX2	;addresses
0027	DE 44		LDX	TEMP	
0029	39		RTS		;Return from Subroutine
002A	DE 40	INTRPT	LDX	INDEX1	;INDEX1 → X
002C	A6 00		LDAA	X	;Read data in from A/D at X
002E	08		INX		;Increment X by one
002F	DF 40		STX	INDEX1	;X → INDEX1
0031	DE 42		LDX	INDEX2	;INDEX2 → X

Functional Description (Continued)

SAMPLE PROGRAM FOR *FIGURE 16* INTERFACING MULTIPLE A/Ds IN AN MC6800 SYSTEM

ADDRESS	HEX CODE		MNEMONICS		COMMENTS
0033	A7 00		STAA	X	; Store data at X
0035	8C 02 07		CPX	#$0207	; Have all A/D's been read?
0038	27 05		BEQ	RETURN	; Yes: branch to RETURN
003A	08		INX		; No: increment X by one
003B	DF 42		STX	INDEX2	; X ⟶ INDEX2
003D	20 E3		BRA	INTRPT	; Branch to 002A
003F	3B	RETURN	RTI		
0040	50 00	INDEX1	FDB	$5000	; Starting address for A/D
0042	02 00	INDEX2	FDB	$0200	; Starting address for data storage
0044	00 00	TEMP	FDB	$0000	

Note 1: In order for the microprocessor to service subroutines and interrupts, the stack pointer must be dimensioned in the user's program.

For amplification of DC input signals, a major system error is the input offset voltage of the amplifiers used for the preamp. *Figure 17* is a gain of 100 differential preamp whose offset voltage errors will be cancelled by a zeroing subroutine which is performed by the INS8080A microprocessor system. The total allowable input offset voltage error for this preamp is only 50 μV for ½ LSB error. This would obviously require very precise amplifiers. The expression for the differential output voltage of the preamp is:

$$V_O = [V_{IN}(-) \quad V_{IN}(\ )]\left[1 - \frac{2R2}{R1}\right] -$$

SIGNAL GAIN

$$(V_{OS_2} \quad V_{OS_1} \quad V_{OS_3} \pm I_X R_X)\left(1 - \frac{2R2}{R1}\right)$$

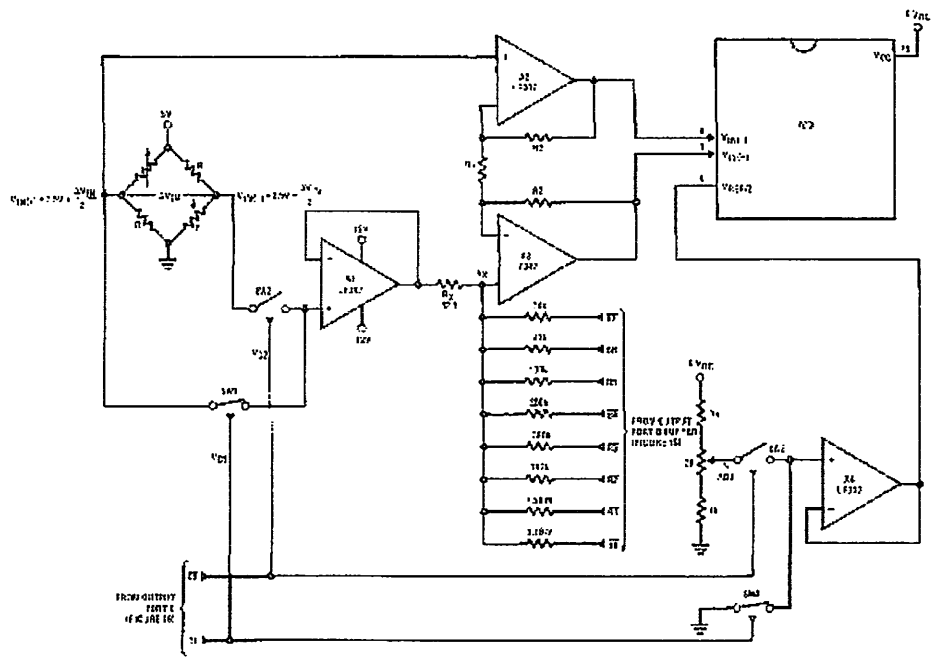
DC ERROR TERM GAIN

where I_X is the current through resistor R_X. All of the offset error terms can be cancelled by making $\pm I_X R_X = V_{OS1} - V_{OS3} \quad V_{OS2}$. This is the principle of this auto-zeroing scheme.

The INS8080A uses the 3 I/O ports of an INS8255 Programable Peripheral Interface (PPI) to control the auto zeroing and input data from the ADC0801 as shown in *Figure 18*. The PPI is programmed for basic I/O operation (mode 0) with Port A being an input port and Ports B and C being output ports. Two bits of Port C are used to alternately open or close the 2 switches at the input of the preamp. Switch SW1 is closed to force the preamp's differential input to be zero during the zeroing subroutine and then opened and SW2 is then closed for conversion of the actual differential input signal. Using 2 switches in this manner eliminates concern for the ON resistance of the switches as they must conduct only the input bias current of the input amplifiers.

Output Port B is used as a successive approximation register by the 8080 and the binary scaled resistors in series with each output bit create a D/A converter. During the zeroing subroutine, the voltage at V_X increases or decreases as required to make the differential output voltage equal to zero. This is accomplished by ensuring that the voltage at the output of A1 is approximately 2.5V so that a logic "1" (5V) on any output of Port B will source current into node V_X thus raising the voltage at V_X and making the output differential more negative. Conversely, a logic "0" (0V) will pull current out of node V_X and decrease the voltage, causing the differential output to become more positive. For the resistor values shown, V_X can move ± 12 mV with a resolution of 50 μV, which will null the offset error term to ½ LSB of full-scale for the ADC0801. It is important that the voltage levels that drive the auto-zero resistors be constant. Also, for symmetry, a logic swing of 0V to 5V is convenient. To achieve this, a CMOS buffer is used for the logic output signals of Port B and this CMOS package is powered with a stable 5V source. Buffer amplifier A1 is necessary so that it can source or sink the D/A output current.

Functional Description (Continued)



Note 1: R2 = 49.5 kΩ

Note 2: Switches are LMC13334 CMOS analog switches.

Note 3: The 5 resistors used in the sub-zero section can be ±5% tolerance.

FIGURE 17. Gain of 100 Differential Transducer Preamp

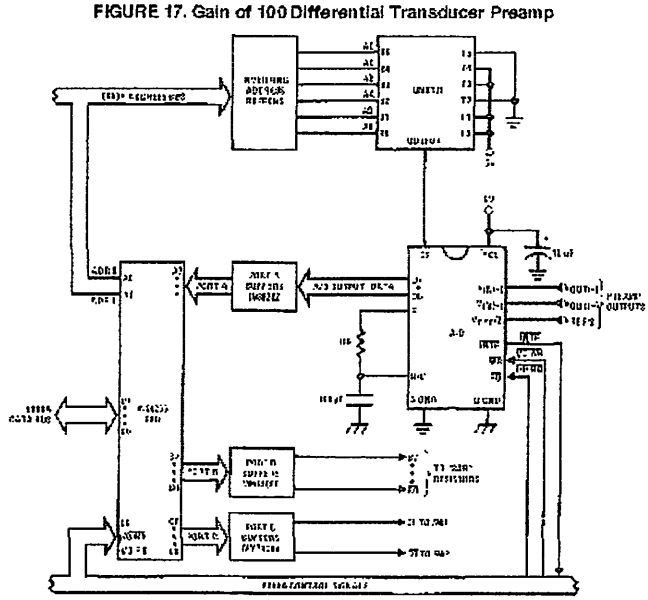


FIGURE 18. Microprocessor Interface Circuitry for Differential Preamp

A flow chart for the zeroing subroutine is shown in *Figure 19*. It must be noted that the ADC0801 series will output an all zero code when it converts a negative input [$V_{IN}(\ )$ ≤ $V_{IN}(-)$]. Also, a logic inversion exists as all of the I/O ports are buffered with inverting gates.

Basically, if the data read is zero, the differential output voltage is negative, so a bit in Port B is cleared to pull V_X more negative which will make the output more positive for the next conversion. If the data read is not zero, the output voltage is positive so a bit in Port B is set to make V_X more positive and the output more negative. This continues for 8 approximations and the differential output eventually converges to within 5 mV of zero.

The actual program is given in *Figure 20*. All addresses used are compatible with the BLC 80/10 microcomputer system. In particular:

Port A and the ADC0801 are at port address E4

Port B is at port address E5

Port C is at port address E6

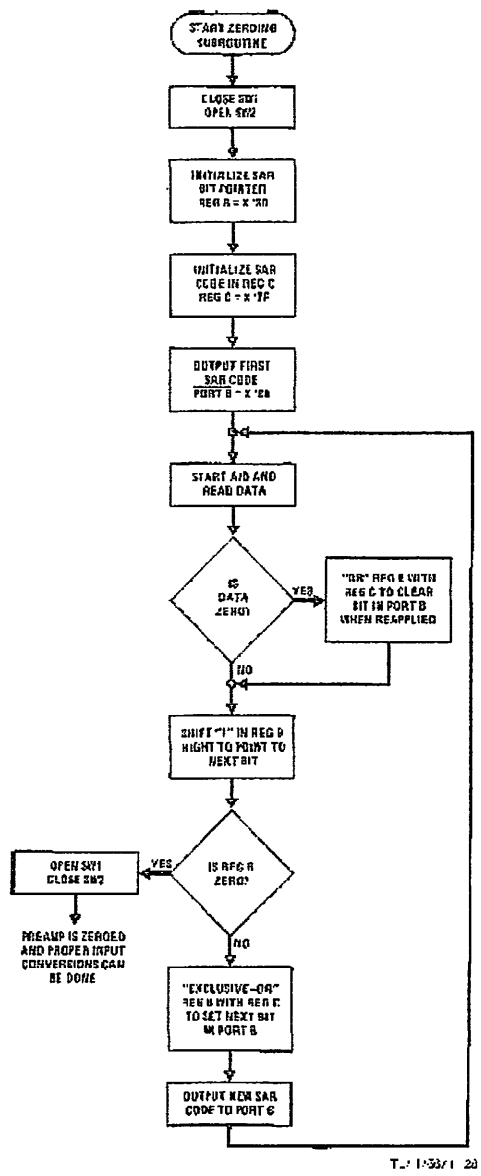
PPI control word port is at port address E7

Program Counter automatically goes to ADDR:3C3D upon acknowledgement of an interrupt from the ADC0801

5.3 Multiple A/D Converters in a Z-80 Interrupt Driven Mode

In data acquisition systems where more than one A/D converter (or other peripheral device) will be interrupting program execution of a microprocessor, there is obviously a need for the CPU to determine which device requires servicing. *Figure 21* and the accompanying software is a method of determining which of 7 ADC0801 converters has completed a conversion ($\overline{INTR}$ asserted) and is requesting an interrupt. This circuit allows starting the A/D converters in any sequence, but will input and store valid data from the converters with a priority sequence of A/D 1 being read first, A/D 2 second, etc., through A/D 7 which would have the lowest priority for data being read. Only the converters whose INT is asserted will be read.

The key to decoding circuitry is the DM74LS373, 8-bit D type flip-flop. When the Z-80 acknowledges the interrupt, the program is vectored to a data input Z-80 subroutine. This subroutine will read a peripheral status word from the DM74LS373 which contains the logic state of the $\overline{INTR}$ outputs of all the converters. Each converter which initiates an interrupt will place a logic "0" in a unique bit position in the status word and the subroutine will determine the identity of the converter and execute a data read. An identifier word (which indicates which A/D the data came from) is stored in the next sequential memory location above the location of the data so the program can keep track of the identity of the data entered.



TL/F/5371-28

FIGURE 19. Flow Chart for Auto-Zero Routine

```
3D00   3E90     MVI 90
3D02   D3E7     Out Control Port                    ;Program PPI
3D04   2601     MVI H 01          Auto-Zero Subroutine
3D06   7C       MOV A,H
3D07   D3E6     OUT C                              ;Close SW1 open SW2
3D09   0680     MVI B 80                           ;Initialize SAR bit pointer
3D0B   3E7F     MVI A 7F                           ;Initialize SAR code
3D0D   4F       MOV C,A           Return
3D0E   D3E5     OUT B                              ;Port B = SAR code
3D10   31AA3D   LXI SP 3DAA       Start            ;Dimension stack pointer
3D13   D3E4     OUT A                              ;Start A/D
3D15   FB       EI
3D16   00       NOP               Loop             ;Loop until INT asserted
3D17   C3163D   JMP Loop
3D1A   7A       MOV A,D           Auto-Zero
3D1B   C600     ADI 00
3D1D   CA2D3D   JZ Set C                           ;Test A/D output data for zero
3D20   78       MOV A,B           Shift B
3D21   F600     ORI 00                             ;Clear carry
3D23   1F       RAR                                ;Shift "1" in B right one place
3D24   F300     CPI 00                             ;Is B zero? If yes last
3D26   CA373D   JZ Done                            ;approximation has been made
3D29   47       MOV B,A
3D2A   C3333D   JMP New C
3D2D   79       MOV A,C           Set C
3D2E   B0       ORA B                              ;Set bit in C that is in same
3D2F   4F       MOV C,A                            ;position as "1" in B
3D30   C3203D   JMP Shift B
3D33   A9       XRA C             New C            ;Clear bit in C that is in
3D34   C30D3D   JMP Return                         ;same position as "1" in B
3D37   47       MOV B,A           Done             ;then output new SAR code.
3D38   7C       MOV A,H                            ;Open SW1, close SW2 then
3D39   EE03     XRI 03                             ;proceed with program. Preamp
3D3B   D3E6     OUT C                              ;is now zeroed.
3D3D            •                 Normal
                •
                •
                Program for processing
                proper data values
3C3D   D3E4     IN A              Read A/D Subroutine  ;Read A/D data
3C3F   EEFF     XRI FF                             ;Invert data
3C41   57       MOV D,A
3C42   78       MOV A,B                            ;Is B Reg = 0? If not stay
3C43   E6FF     ANI FF                             ;in auto zero subroutine
3C45   C21A3D   JNZ Auto-Zero
3C48   C33D3D   JMP Normal
```

Note: A numerical value are hexadecimal representations.

FIGURE 20. Software for Auto-Zeroed Differential A/D

5.3 Multiple A/D Converters in a Z-80® Interrupt Driven Mode (Continued)

The following notes apply:

1) It is assumed that the CPU automatically performs a RST 7 instruction when a valid interrupt is acknowledged (CPU is in interrupt mode 1). Hence, the subroutine starting address of X0038.

2) The address bus from the Z-80 and the data bus to the Z-80 are assumed to be inverted by bus drivers.

3) A/D data and identifying words will be stored in sequential memory locations starting at the arbitrarily chosen address X 3E00.

4) The stack pointer must be dimensioned in the main program as the RST 7 instruction automatically pushes the PC onto the stack and the subroutine uses an additional 6 stack addresses.

5) The peripherals of concern are mapped into I/O space with the following port assignments:

HEX PORT ADDRESS	PERIPHERAL
00	MM74C374 8-bit flip-flop
01	A/D 1
02	A/D 2
03	A/D 3
04	A/D 4
05	A/D 5
06	A/D 6
07	A/D 7

This port address also serves as the A/D identifying word in the program.

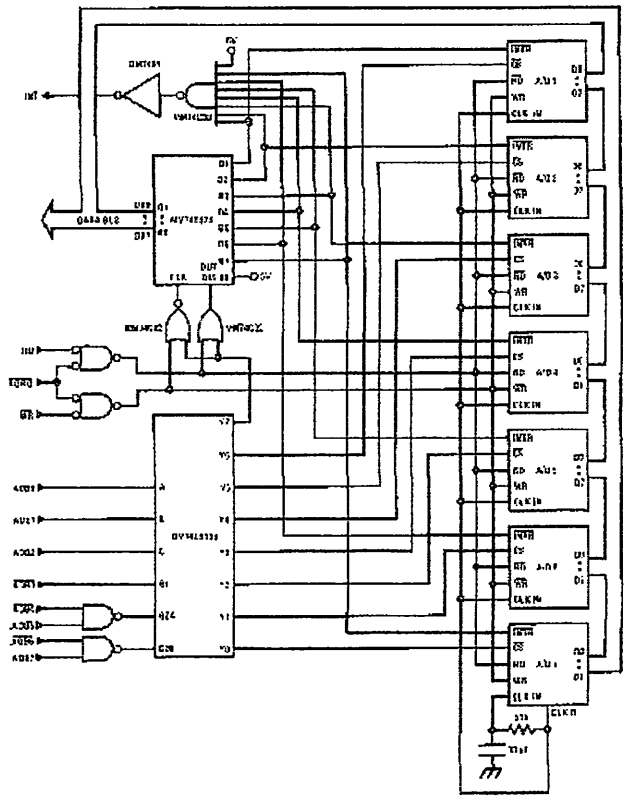


FIGURE 21. Multiple A/Ds with Z-80 Type Microprocessor

INTERRUPT SERVICING SUBROUTINE

LOC	OBJ CODE		SOURCE STATEMENT	COMMENT
0038	E5		PUSH HL	;Save contents of all registers effected by
0039	C5		PUSH BC	;this subroutine.
003A	F5		PUSH AF	;Assumed INT mode 1 earlier set.
003B	21 00 E0		LD (HL),XE000	;Initialize memory pointer where data will be stored.
003E	0E 01		LD C, X01	;C register will be port ADDR of A/D converters.
0040	D300		OUT X00, A	;Load peripheral status word into 8-bit latch.
0042	D300		IN A, X00	;Load status word into accumulator.
0044	47		LD B,A	;Save the status word.
0045	79	TEST	LD A,C	;Test to see if the status of all A/D's have
0046	FE 08		CP, X08	;been checked. If so, exit subroutine
0048	CA 60 00		JPZ, DONE	
004B	78		LD A,B	;Test a single bit in status word by looking for
004C	1F		RRA	;a "1" to be rotated into the CARRY (an $\overline{INT}$
004D	47		LD B,A	;is loaded as a "1"). If CARRY is set then load
004E	DA 5500		JPC, LOAD	;contents of A/D at port ADDR in C register.
0051	0C	NEXT	INC C	;If CARRY is not set, increment C register to point
0052	C3 4500		JP,TEST	;to next A/D, then test next bit in status word.
0055	ED 78	LOAD	IN A, (C)	;Read data from interrupting A/D and invert
0057	EE FF		XOR FF	;the data.
0059	77		LD (HL),A	;Store the data
005A	2C		INC L	
005B	71		LD (HL),C	;Store A/D identifier (A/D port ADDR).
005C	2C		INC L	
005D	C3 51 00		JP,NEXT	;Test next bit in status word.
0060	F1	DONE	POP AF	;Re-establish all registers as they were
0061	C1		POP BC	;before the interrupt.
0062	E1		POP HL	
0063	C9		RET	;Return to original program

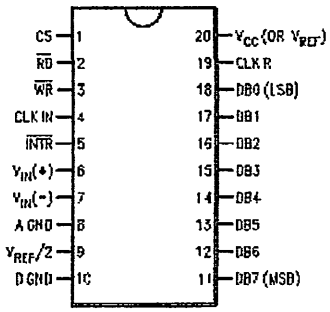
Ordering Information

TEMP RANGE		0°C TO 70°C	0°C TO 70°C	0°C TO 70°C	−40°C TO −85°C
ERROR	± ½ Bit Adjusted				ADC0801LCN
	± ½ Bit Unadjusted	ADC0802LCWM	ADC0802LCV		ADC0802LCN
	± ½ Bit Adjusted	ADC0803LCWM	ADC0803LCV		ADC0803LCN
	± 1Bit Unadjusted	ADC0804LCWM	ADC0804LCV	ADC0804LCN	ADC0805LCN
PACKAGE OUTLINE		M20B—Small Outline	V20A—Chip Carrier	N20A—Molded DIP	

TEMP RANGE		−40°C TO −85°C	−55°C TO −125°C
ERROR	± ½ Bit Adjusted	ADC0801LCJ	ADC0801LJ
	± ½ Bit Unadjusted	ADC0802LCJ	ADC0802LJ, ADC0802LJ/883
	± ½ Bit Adjusted	ADC0803LCJ	
	± 1Bit Unadjusted	ADC0804LCJ	
PACKAGE OUTLINE		J20A—Cavity DIP	J20A—Cavity DIP

Connection Diagrams

ADC080X
Dual-In-Line and Small Outline (SO) Packages



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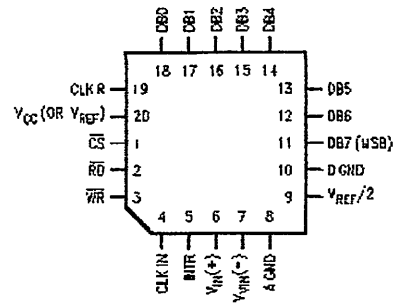
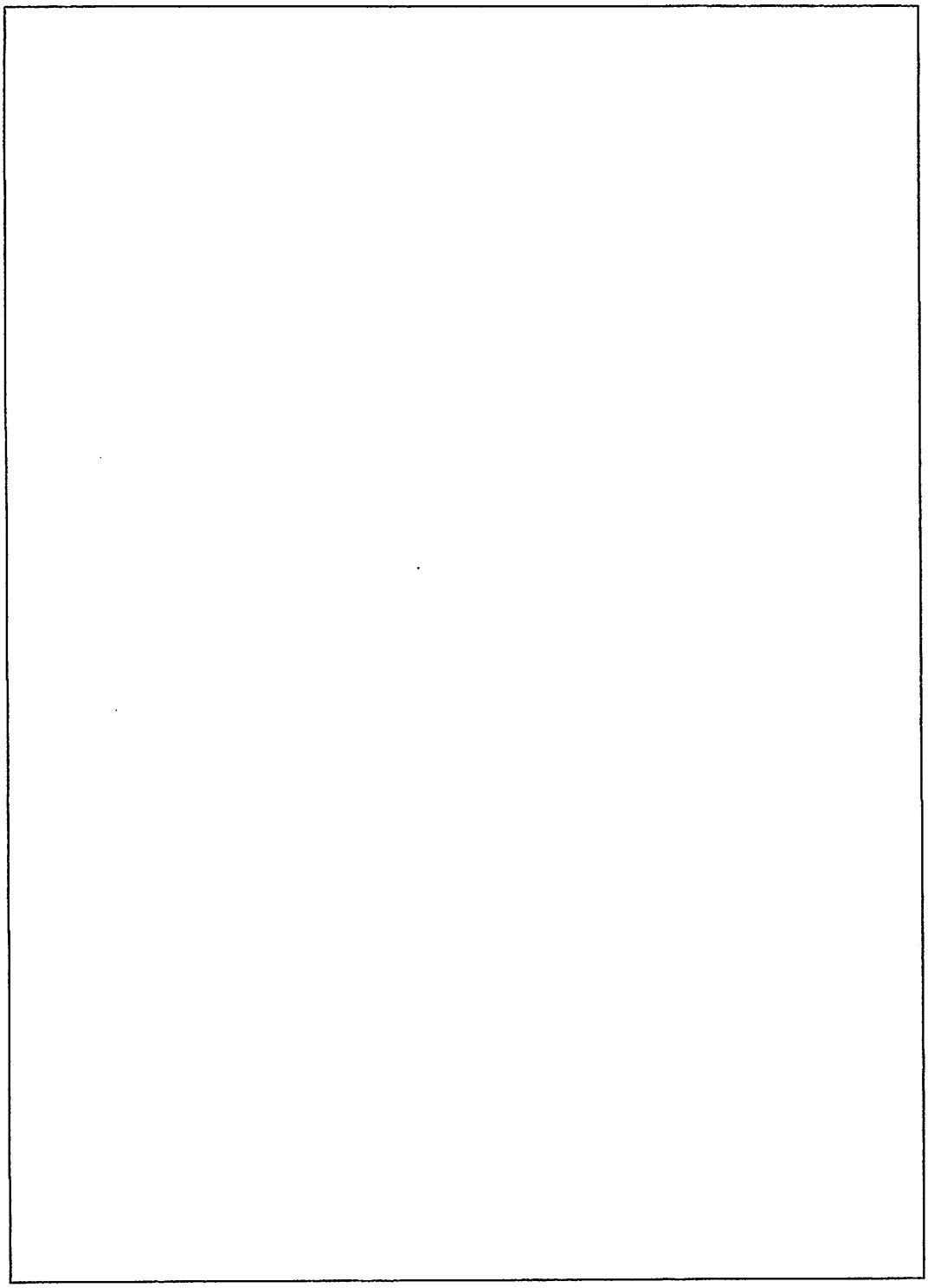
ADC080X
Molded Chip Carrier (PCC) Package

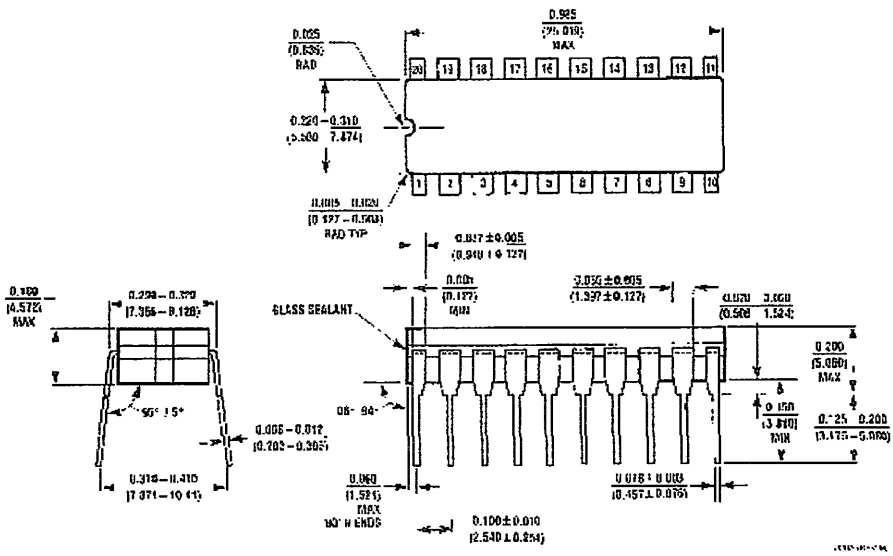


T-/ I-53/1 32

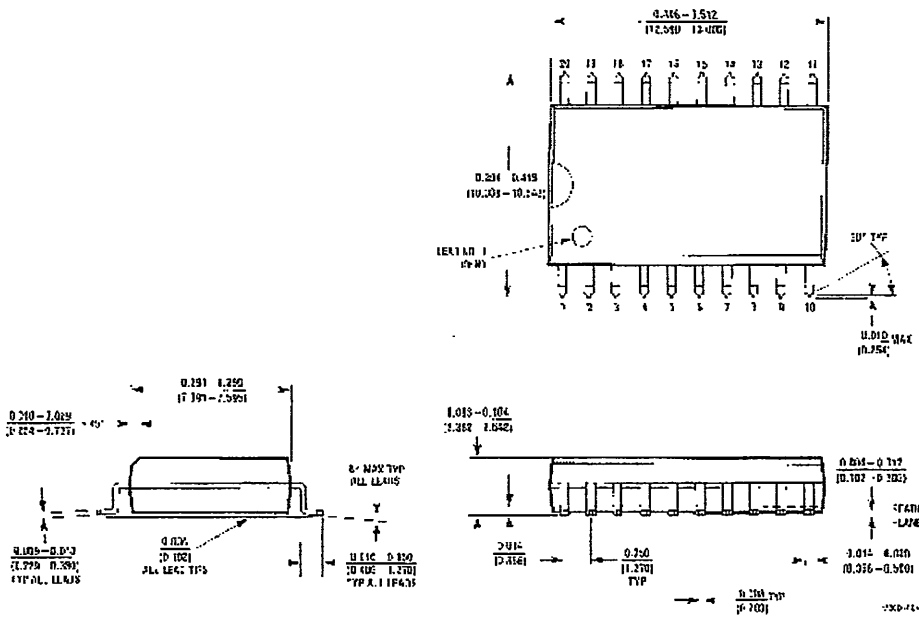
See Ordering Information



Physical Dimensions inches (millimeters)

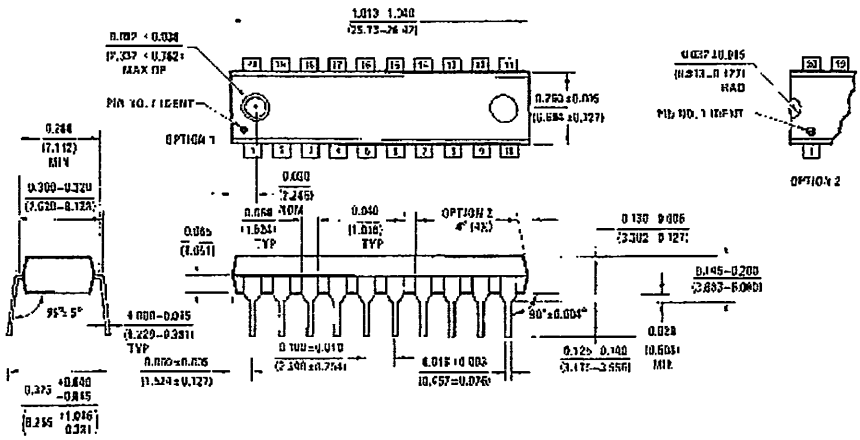


Dual-In-Line Package (J)
Order Number ADC0801LJ, ADC0802LJ, ADC0801LCJ,
ADC0802LCJ, ADC0803LCJ or ADC0804LCJ
ADC0802LJ/883 or 5962-9096601MRA
NS Package Number J20A



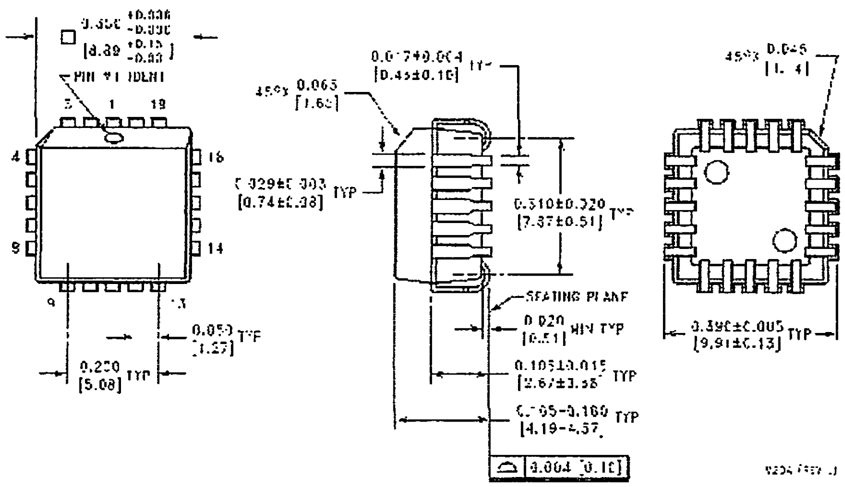
SO Package (M)
Order Number ADC0802LCWM, ADC0803LCWM or ADC0804LCWM
NS Package Number M20B

Physical Dimensions inches (millimeters) (Continued)



Molded Dual-In-Line Package (N)
Order Number ADC0801LCN, ADC0802LCN,
ADC0803LCN, ADC0804LCN or ADC0805LCN
NS Package Number N20A

Physical Dimensions inches (millimeters) (Continued)



Molded Chip Carrier Package (V)
Order Number ADC0802LCV, ADC0803LCV or ADC0804LCV
NS Package Number V20A

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