INSTITUT TEKNOLOGI NASIONAL MALANG
FAKULTAS TEKNOLOGI INDUSTRI
JURUSAN TEKNIK ELEKTRO S - 1
KONSENTRASI TEKNIK ELEKTRONIKA

SKRIPSI

PERENCANAAN DAN PEMBUATAN BEL SEKOLAH YANG BISA BERSUARA SECARA OTOMATIS DILENGKAPI DENGAN MATRIK LED SEBAGAI TAMPILAN BERBASIS MIKROKONTROLLER AT89S52

Disusun Oleh :

FILIP WONGSO WIBOWO
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APRIL 2005

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ISBN-13: 978-0-13-376220-2
ISBN-10: 0-13-376220-9

Library of Congress Control Number: 2013954111

LEMBAR PERSETUJUAN

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SKRIPSI

Disusun dan Diajukan untuk Melengkapi dan Memenuhi Syarat Guna Memperoleh Gelar Sarjana Teknik

Disusun Oleh :

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Hari	: Selasa
Tanggal	: 29 Maret 2005
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ABSTRAKSI

PERENCANAAN DAN PEMBUATAN BEL SEKOLAH YANG BISA BERSUARA SECARA OTOMATIS DILENGKAPI DENGAN MATRIK LED SEBAGAI TAMPILAN BERBASIS MIKROKONTROLLER AT89S52

(Filip Wongso Wibowo, 9917118, Teknik Elektro/Elektronika S-1, 84 halaman)

(Dosen Pembimbing : Joseph Dedy Irawan, ST, MT)

Kata Kunci : Mikrokontroller AT89S52, RTC DS 12C887, ISD 1420, LCD, Dot Matrik, Keypad Matrik 4x4

Teknologi dibuat dan diciptakan untuk membantu pekerjaan manusia atau untuk menjadikan suatu pekerjaan menjadi mudah dan efisien. Penerapan teknologi dimanfaatkan oleh semua bidang, salah satunya adalah bidang pendidikan, khususnya di sekolah – sekolah. Pada saat sekarang ini masih banyak sekolah – sekolah yang di dalam menggunakan bel untuk aktifitas sehari – hari masih menggunakan cara manual, seperti bel untuk membunyikan tanda masuk kelas, pergantian jam pelajaran, istirahat, maupun tanda pulang sekolah, cara ini dirasa kurang efektif dan kurang efisien.

Untuk merancang bel sekolah secara otomatis dapat memanfaatkan teknologi mikrokontroller/ teknologi lainnya. Salah satunya dapat menggunakan teknologi mikrokontroller AT89S52 dengan menambahkan komponen luar sebagai piranti pendukung yang dapat digunakan sebagai bel sekolah secara otomatis yang dapat memberikan informasi secara terjadwal. Salah satu dari komponen luar yang digunakan diantaranya adalah : RTC DS 12C887 yang merupakan jam yang sangat kompleks dan dapat menghitung dan menyimpan waktu (detik, menit, jam, hari, tanggal, bulan dan tahun yang mempunyai tingkat kepresisian/ keakuratan yang sangat tinggi) , ISD 1420, keypad matrik 4x4.

Prinsip kerja dari sistem ini adalah pertama – tama user memasukkan data waktu aktifitas sekolah melalui keypad, maka mikrokontroller AT89S52 akan mendeteksi/ mencocokkan waktu sekarang dengan waktu yang dimasukkan melalui keypad, jika waktu/ jamnya sama maka bel listrik dan ISD 1420 akan aktif dan mengaktifkan driver motor DC untuk menutup dan membuka pintu gerbang sebagai tanda dimulai/ selesainya aktifitas sekolah. Dengan demikian, dengan adanya bel sekolah secara otomatis ini diharapkan mampu meringankan tugas seorang operator.

Lembar Persembahan

- **Kegagalan** *bukan berarti* **Anda** *adalah orang yang gagal ..... ini berarti* **Anda** *masih belum berhasil*

- **Kegagalan** *bukan berarti* **Anda** *tidak mencapai apa – apa ..... ini berarti* **Anda** *telah mempelajari sesuatu*

- **Kegagalan** *bukan berarti* **Anda** *telah dipermalukan ..... ini berarti* **Anda** *telah mencoba*

- **Kegagalan** *bukan berarti* **Anda** *tidak memiliki kemampuan ..... ini berarti* **Anda** *harus melakukan hal itu dengan cara yang lain*

- **Kegagalan** *bukan berarti* **Anda** *telah menyia – nyiakan kehidupan* **Anda** *..... ini berarti* **Anda** *ada alasan lain untuk memulainya lagi*

- **Kegagalan** *bukan berarti* **Anda** *harus menyerah kalah ..... ini berarti* **Anda** *harus berusaha lebih keras lagi*

- **Kegagalan** *bukan berarti* **Anda** *tidak akan sukses ..... ini berarti* **Anda** *akan mengambil waktu lebih lama lagi*

- **Kegagalan** *bukan berarti* **Anda** *telah dihancurkan ..... ini berarti* **Anda** *mempunyai kesempatan untuk mencoba sesuatu yang baru*

Segala Puja Dan Puji Syukur Penulis Panjatkan Kehadirat Tuhan Yesus Kristus Yang Telah Melimpahkan Berkat dan Karunianya sehingga Penyusun dapat menyelesaikan Skripsi ini dengan baik dan tepat pada waktunya.
Pada Kesempatan Kali ini Penulis ingin Mengucapkan Terima Kasih yang Sebesar - besarnya Kepada :

- **Tuhan Yesus Kristus**, *Raja Di Atas Segala Raja Serta Raja Segala Ilmu Yang Ada Didunia ini. Terima Kasih Ya Tuhan Yang Telah Melimpahkan Berkat dan Karunianya Sehingga Penulis Dapat Menuntaskan Skripsi ini dengan Baik, Engkau Sungguh Allah yang Luar Biasa, Tak dapat Hambamu ini melupakan segala kebaikan dan Pemeliharaan - Mu*

- **Papaku** *Dan* **Mamaku** *, Berkat Doa dan Restu Engkau Berdualah, Ananda Berhasil menyelesaikan Semua ini. Ternyata Dibalik Kemarahanmu, Ketidaktegaanmu, Serta Cinta Kasihmu Telah Melahirkan Seorang Sarjana Ditengah Keluarga ini. Dalam Hati Yang Paling Dalam ini, Meskipun Didalam Keegoisanku , Keangkuhanku Tersimpan Jiwa Yang Selalu Menyayangimu.Ya... Sampai Kapanpun dan Sampai Selamanya Aku akan Sayang Engkau Berdua....*

- **Ketiga Kakakku** *dan* **Adikku** *Tercinta Terima Kasih Atas Segala Dukungannya Selama ini*

- **Pak Joseph** *selaku dosen pembimbing yang sudah membimbing dengan sabar dan penuh perhatian*

- *Temen2 Seperjuangan (* **Wahid , Natora , Dance , Cahyo , Indra , Gede , Heri , Cross** *)* **Congratulation.....** *I Hope We Are The Best Friendship Forever*

- *Temen2 Seperjuangan Kompree (* **Dodik , Yusuf , Gede , Anik , and Dwi** *) Makasih atas bantuan dan supportnya sehingga kita bisa lulus bareng – bareng .* **" We Are The Best Men "**

- *Untuk* **Budhi**, *Makasih yang udah ngebantuin nyolder. Makasih Yaa Bud. Tak Doain kamu cepet lulus jadi sarjana kayak Aku .....He He He*

- *Tak Lupa Makasih Buat* **Agoek** *yang ngebantuin bikin – bikin mekanik pintu gerbang. Mudah – mudahan kamu nanti bisa jadi tukang mekanik beneran Yaa*

- *Makasih juga buat* **Resti** *yang udah nyumbangin suaranya buat ngrekam ISD.*

- *Serta Semua Teman Yang Tidak Dapat Penulis Sebutkan , Makasih, Makasih Buangeet Atas Segala Doa Dan Supportnya.*

KATA PENGANTAR

Dengan mengucapkan puji syukur kepada Tuhan YME atas berkat bimbingan dan rahmat-Nya, sehingga penulis dapat menyelesaikan laporan skripsi yang berjudul *"Perencanaan dan Pembuatan Bel Sekolah Yang Bisa Bersuara Secara Otomatis Dilengkapi Dengan Matrik Led Sebagai Tampilan Berbasis Mikrokontroller AT 89S52"*.

Skripsi ini merupakan salah satu syarat yang harus dipenuhi oleh setiap mahasiswa untuk dapat memperoleh gelar sarjana di jurusan Teknik Elektro konsentrasi Elektronika Institut Teknologi Nasional Malang.

Pada kesempatan ini kami menyampaikan rasa hormat dan terima kasih yang sebesar – besarnya atas segala bantuan yang telah diberikan kepada kami terutama kepada :

1. Bapak Dr. Ir. Abraham Lomi, MSEE, selaku Rektor ITN Malang.
2. Bapak Ir. Mochtar Asroni, MSEE, selaku Dekan FTI.
3. Bapak Ir. Fx. Yudi Limpraptono, MT, selaku Ketua Jurusan Teknik Elektro S – 1.
4. Ibu Ir. Mimin Mustikawati, selaku Sekretaris Jurusan Teknik Elektro S – 1.
5. Bapak Joseph Dedy Irawan, ST, MT, selaku Dosen Pembimbing.
6. Untuk teman-teman seperjuangan : Wahid, Natora, Dance, Cahyo, Cros, Indra, Gede, Marse dan teman-teman lain yang tidak bisa saya

sebutkan satu per satu, terima kasih atas support yang diberikan selama ini.

7. Teman-teman angkatan 99 terutama Elka 3-4 terima kasih atas dukungannya serta semua pihak yang telah banyak membantu penulis dalam penyusunan Skripsi ini.

Penulis menyadari bahwa penulisan Skripsi ini mungkin masih banyak terdapat kekurangan, untuk itu penulis mengharapkan saran, kritik dari pembaca demi sempurnanya laporan Skripsi ini.

Akhir kata penulis mengharapkan semoga apa yang telah penulis lakukan dapat bermanfaat dan berguna bagi kita semua.

Malang, Maret 2005

Penyusun

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BAB I

PENDAHULUAN

1.1. Latar Belakang

Sampai saat ini, semua lembaga pendidikan (mulai tingkat TK sampai tingkat SMA) menggunakan bel sebagai tanda aktifitas sehari – harinya, seperti : masuk kelas, pergantian mata pelajaran, istirahat, pulang sekolah dan aktifitas pendidikan lainnya.

Jika dilihat pada waktu yang lalu lonceng digunakan sebagai tanda – tanda aktifitas di sekolah, namun beberapa saat kemudian fungsi lonceng digantikan dengan bel listrik. Semua alat yang digunakan dalam memberi tanda aktifitas di sekolah tersebut masih dilakukan secara manual, sehingga sering terjadi ketidaktepatan waktu dalam membunyikan bel dari waktu yang telah ditentukan.

Melihat kenyataan seperti di atas, maka penyusun ingin menerapkan teknologi di bidang elektronika dengan jalan mengendalikan bel dan pintu gerbang secara otomatis. Pengendali tersebut berupa mikrokontroller AT89S52 yang dapat mengendalikan bel dan pintu gerbang pada waktu – waktu tertentu dengan memberi informasi secara terjadwal pada suatu sekolah. Salah satu contohnya adalah pada saat masuk kelas pada pukul 07.00, maka bel sekolah akan berbunyi secara otomatis dan pintu gerbang akan menutup dengan sendirinya seiring bel masuk selesai berbunyi. Begitu juga pada saat pergantian jam pelajaran dan waktu istirahat, bel akan berbunyi secara otomatis, dan pada waktu pulang sekolah bel akan berbunyi diiringi dengan terbukanya pintu gerbang secara otomatis. Alat ini juga dilengkapi dengan tampilan suara sebagai tanda peringatan kalau jam menunjukkan waktu masuk, istirahat dan

pulang sekolah. Dengan adanya alat ini diharapkan akan membantu aktifitas pendidikan di sekolah, karena tidak akan ada lagi ketidaktepatan waktu di dalam membunyikan bel sekolah sekaligus meringankan tugas seorang operator di dalam mengoperasikan bel sekolah pada waktu – waktu tertentu, terutama pada saat masuk kelas, istirahat dan pulang sekolah.

1.2. Rumusan Masalah

Dalam Perencanaan dan Pembuatan Bel Sekolah yang Bisa Bersuara Secara Otomatis Berbasis Mikrokontroller AT89S52 dapat dirumuskan beberapa permasalahan seperti di bawah ini :

1. Bagaimana merancang dan membuat minimum sistem mikrokontroller AT89S52 sehingga membentuk sebuah bel otomatis.
2. Bagaimana cara membuat perangkat lunak (*software*) untuk mengontrol kerja sistem.
3. Bagaimana membuat pesan suara dan mengirim pesan suara ISD 1420.

1.3. Tujuan

Adapun tujuan dari perencanaan dan pembuatan alat ini antara lain adalah :

1. Mengaplikasikan teknologi mikrokontroller AT89S52 pada perencanaan dan pembuatan bel sekolah secara otomatis.
2. Mencegah terjadinya ketidaktepatan waktu di dalam membunyikan bel sekolah.
3. Meringankan tugas seorang operator di dalam mengendalikan bel sekolah.

1.4. Batasan Masalah

Sehubungan dengan permasalahan yang dibahas dalam pembuatan skripsi ini, permasalahan dibatasi dengan tujuan untuk mencegah terjadinya kemungkinan meluasnya masalah dari fokus permasalahan. Adapun batasan masalah pada skripsi ini antara lain adalah sebagai berikut :

1. Mikrokontroller AT89S52 adalah sebagai pusat pengendali utama.
2. Data waktu diambil dari RTC DS 12C887.
3. Data suara diambil dari ISD 1420.
4. Tidak membahas motor Dc yang digunakan secara mendetail.
5. Tidak membahas mengenai rangkaian catu daya/ power supply.
6. Untuk tampilan settingan waktu digunakan LCD dot matrik 16x2.

1.5. Metodologi

Dalam perancangan dan pembuatan bel sekolah secara otomatis berbasis mikrokontroller AT89S52, metode yang digunakan adalah sebagai berikut :

- **Study Literature**

  Dengan mempelajari teori serta aplikasi sistem kontrol menggunakan Mikrokontroller AT89S52.

- **Perencanaan dan Pembuatan Alat**

  Pada perencanaan dan pembuatan alat ini dibagi menjadi dua bagian yaitu terdiri atas perencanaan perangkat keras (*hardware*) dan perancangan perangkat lunak (*software*) yang mendukung sistem kerja pembuatan alat ini. Sesuai dengan rencana yang telah disusun sebagai perwujudan dari penyusunan Skripsi.

- **Pelaksanaan Pengujian Alat**

  Melakukan pengujian pada keypad, RTC DS 12C887, ISD 1420, driver bel listrik, driver motor dc dan dot matrik sebagai proses kerja alat yang telah dibuat apakah sudah sesuai dengan perencanaan dan pembuatan alat.

- **Penyusunan Laporan Hasil Kerja dari Pelaksanaan Skripsi**

1.6. Sistematika Penulisan

Adapun Sistematika dari Penyusunan Skripsi ini adalah :

BAB I. PENDAHULUAN

Berisi Latar belakang, rumusan masalah, tujuan, batasan masalah, metodologi serta sistematika penulisan.

BAB II. LANDASAN TEORI

Berisi tentang teori-teori dasar yang memiliki relevansi sebagai dasar perencanaan dan pembuatan.

BAB III. PERENCANAAN DAN PEMBUATAN ALAT

Berisi tentang perencanaan *hardware* dan *software*.

BAB IV. PENGUJIAN ALAT

Berisi tentang data hasil pengujian peralatan yang telah dibuat secara keseluruhan.

BAB V. PENUTUP

Berisi kesimpulan dari hasil pengujian alat dan saran.

BAB II

LANDASAN TEORI

Dalam bab II ini akan dibahas tentang landasan teori yang menunjang perencanaan dan pembuatan alat dalam penyusunan skripsi.

2.1. Mikrokontroller AT89S52

2.1.1. Umum

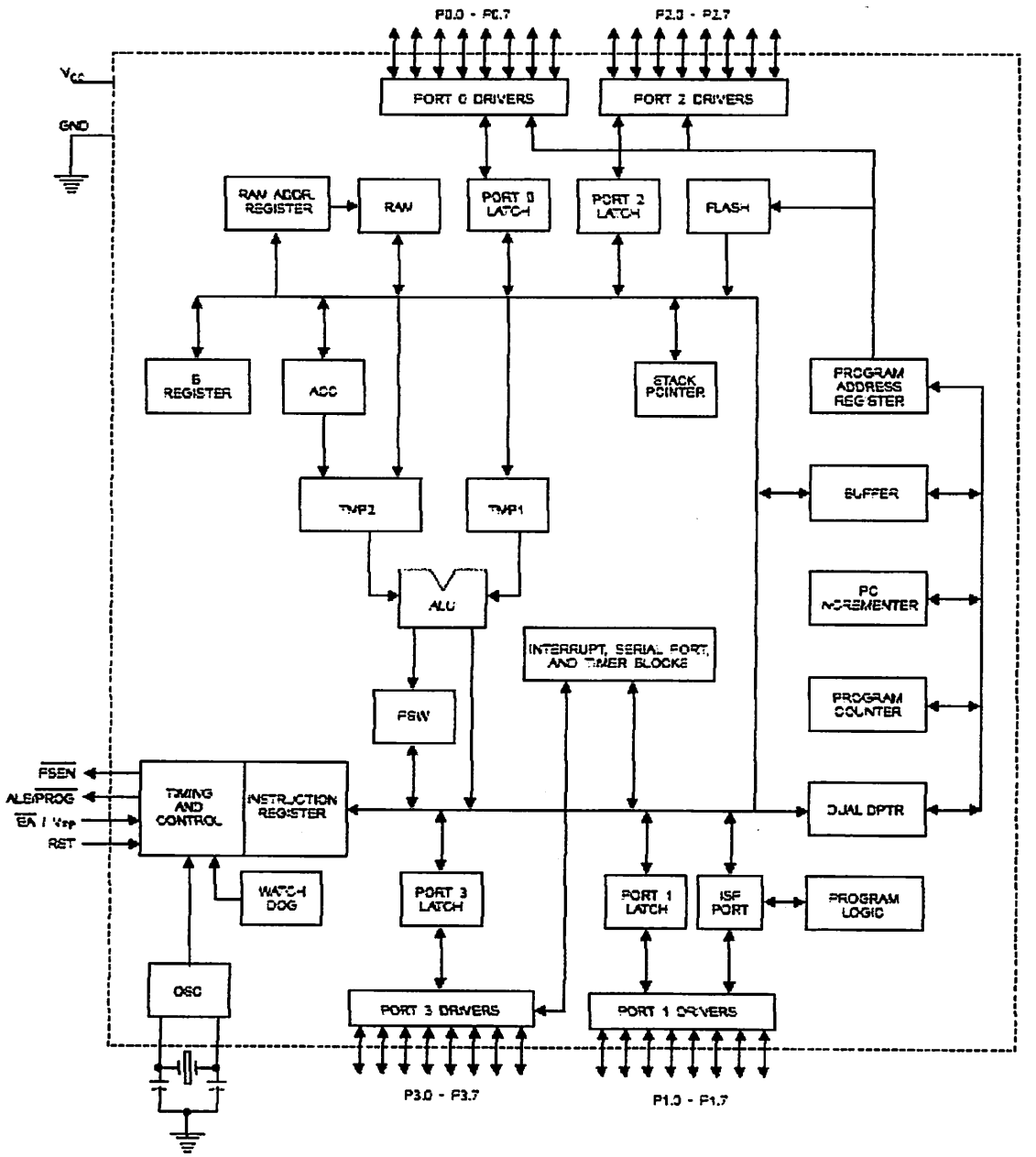
Perbedaan mendasar antara mikrokontroller dan mikroprosesor adalah mikrokontroller selain memiliki CPU, juga dilengkapi dengan memori dan I/ O yang merupakan kelengkapan sebagai sistem minimum mikrokontroller sehingga mikrokontroller dapat dikatakan sebagai mikrokomputer dalam keping tunggal yang dapat berdiri sendiri (*stand alone single chip microcomputer*).

Mikrokontroller AT89S52 adalah mikrokontroller keluaran atmel dengan 8K byte Flash PEROM (*Programmable and Erasable Read Only Memory*), AT89S52 merupakan memori dengan teknologi nonvolatile memori, artinya isi memori tersebut dapat diisi ulang ataupun dihapus berulang kali.

Memori ini biasa digunakan untuk menyimpan instruksi atau perintah berstandar MCS – 51 code sehingga memungkinkan mikrokontroller ini untuk bekerja dalam mode *Single Chip Operation* (Mode Operasi Keping Tunggal) yang tidak memerlukan *Eksternal Memori* (Memori luar) untuk menyimpan source code tersebut.

2.1.2. Perangkat Keras Mikrokontroller AT89S52

Blok diagram mikrokontroller AT89S52 adalah sebagai berikut :



Gambar 2.1 Blok Diagram AT89S52
Sumber : Data Sheet AT89S52

IC ATMEL AT89S52 menyediakan standart sebagai berikut :

⇒ 8K Bytes memori yang dapat diprogram ulang

⇒ 256 Bytes internal RAM

⇒ 32 jalur I/O (Input dan Output) yang dapat diprogram

⇒ 3 x 16 bit Timer dan Counter

⇒ Dual data Pointer (DPTR)

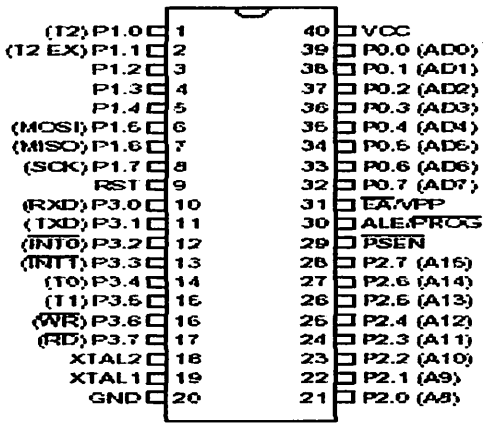
⇒ Watchdog Timer

⇒ ISP Port

⇒ Mendukung serial Port secara penuh

⇒ Waktu Pemrograman yang singkat

Sebagai tambahan AT89S52 dirancang menggunakan logika yang statis untuk mode pengoperasian yang menuju ke frekuensi dasar dan pendukungan terhadap dua *software*, serta dapat memilih model *Power Savingnya*. Mode idle akan berhenti ketika CPU sedang menjalankan *RAM, Timer/ Counter, Serial Port* dan *Interrupt Sistem* untuk terus melanjutkan fungsinya. Model power down akan menyimpan isi dari RAM tapi akan memberhentikan osilator dan akan menghentikan semua chip lain yang sedang berfungsi sampai terdapat adanya gangguan dari luar atau hardware di reset. Pin – pin dari mikrokontroller AT89S52 dapat dilihat pada gambar di bawah ini :



Gambar 2.2 Pin – Pin AT89S52
Sumber : Data Sheet AT89S52

2.1.3. Pin Deskripsi

VCC : Power Supply

GND : Ground

Port 0 : Port 0 berfungsi sebagai 8 bit I/O bertipe *open drain bi-directional.* Sebagai port keluaran, masing – masing pin dapat menyerap arus sebesar 8 masukan TTL (sekitar 3,8 mA). Ketika diberikan logika '1' pada pin port 0 ini maka pin – pin port 0 ini akan dapat digunakan sebagai inputan berimpedansi tinggi.

Port 0 juga dapat dikonfigurasikan sebagai bus alamat/ data bagian rendah (*low byte*) selama proses pengaksesan data memori dan program eksternal. Jika digunakan dalam mode ini port 0 memiliki internal Pull Up.

Port 0 juga menerima kode – kode data yang diberikan padanya selama proses pemrograman dan memberikan kode – kode selama proses

verifikasi program yang telah tersimpan di dalam flash memori. Dalam hal ini dibutuhkan *eksternal Pull Up* selama proses verifikasi program.

Port 1 : Port 1 berfungsi sebagai 8 bit I/O Bi-directional yang dilengkapi dengan *internal Pull Up*. Penyangga keluaran Port 1 mampu memberikan/ menyerap arus sebesar empat masukan TTL (sekitar 1,6 mA). Ketika diberikan logika '1' pada pin – pin port 1 ini, maka masing – masing pin akan di *Pulled High* dengan *pullup internal* sehingga dapat digunakan sebagai inputan. Sebagai inputan, jika pin – pin Port 1 ini dihubungkan ke ground (di-*Pulled Low*), maka masing – masing pin ini dapat menghantarkan arus karena di *Pulled High* secara internal. Port 1 juga menerima alamat bagian rendah (*Low Order Address Bytes*) selama melakukan pemrograman dan verifikasi flash.

Pada port 1 di AT89S52, pin ini mempunyai fungsi alternatif seperti pada tabel berikut ini :

Tabel 2.1 Fungsi – Fungsi Alternatif Port 1
Sumber : Data Sheet AT89S52

Port Pin	Alternate Functions
P1.0	T2 (external count input to Timer/ Counter 2). clock-out
P1.1	T2EX (Timer/ Counter 2 capture/ reload trigger and direction control
P1.5	MOSI (Master Output Slave Input). Used for In-System Programming.
P1.6	MISO (Master Input Slave Output). Used for In-System Programming.
P1.7	SCK (Serial Clock). Used for In- System Programming.

Port 2 : Port 2 berfungsi sebagai 8 bit I/O *Bi-directional* yang dilengkapi dengan *internal Pull Up*. Penyangga keluaran port 2 dapat memberikan atau menyerap arus empat masukan TTL (sekitar 1,6 mA).

Jika diberikan logika '1' pada pin – pin Port 2, maka masing – masing pin akan di *Pull High* secara internal sehingga dapat digunakan sebagai inputan. Sebagai inputan jika pin – pin Port 2 dihubungkan ke ground (di-*Pulled Low*), maka masing – masing pin dapat menghantarkan arus karena di *Pull High* secara internal.

Port 2 akan memberikan byte alamat bagian tinggi (*High Byte*) selama pengambilan instruksi dari memori program eksternal dan selama pengaksesan memori data eksternal yang menggunakan perintah dengan alamat 16 bit (misalnya : **MOVX@DPTR**). Dalam aplikasi ini , jika ingin mengirimkan '1', maka digunakan *Pull Up internal* yang sudah disediakan. Selama pengaksesan memori data eksternal yang menggunakan perintah dengan alamat 8 bit (misalnya **MOVX@Ri**), Port 2 akan mengirimkan isi dari **SFR P2** (***Special Function Register Port 2***). Port 2 juga menerima alamat bagian tinggi (*High Order Address Bytes*) selama pemrograman dan verifikasi flash.

Port 3 : Port 3 juga berfungsi sebagai 8 bit I/O *Bi-directional* yang dilengkapi dengan *Pull Up Internal*. Penyangga keluaran port 3 dapat memberikan atau menyerap arus empat masukan TTL (sekitar 1,6 mA).

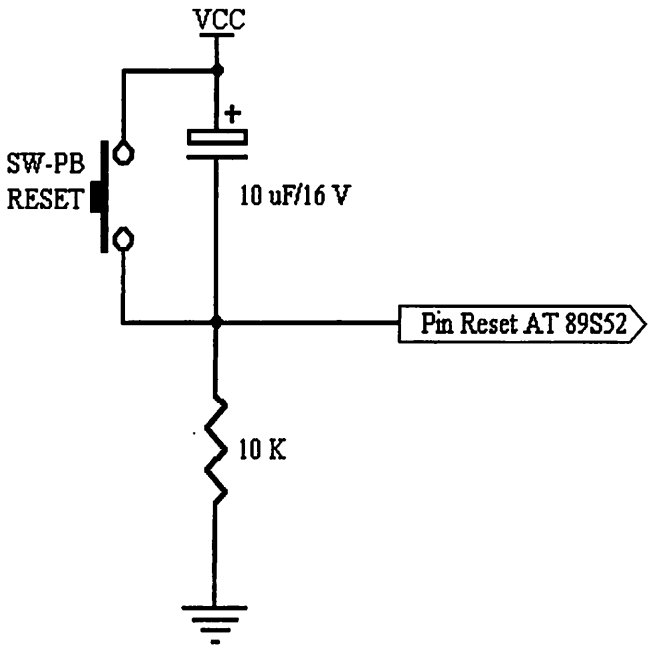
Jika diberikan logika '1' pada pin – pin Port 3, maka masing – masing pin akan di-Pulled High oleh Pull Up internal sehingga dapat digunakan sebagai inputan. Sebagai inputan, jika pin – pin Port 3 dihubungkan ke ground (di-*Pulled Low*), maka masing – masing kaki akan memberikan arus karena di *Pull High* secara internal.

Seperti halnya Port 1, Port 3 juga mempunyai fungsi – fungsi alternatif yang diberikan oleh AT89S52 seperti pada tabel 2.2 berikut ini :

Tabel 2.2 Fungsi – Fungsi Alternatif Port 3
Sumber : Data Sheet AT89S52

Port Pin	Fungsi Alternatif
P3.0	RxD (port masukan serial)
P3.1	TxD (port keluaran serial)
P3.2	$\overline{INT0}$ (sela eksternal 0)
P3.3	$\overline{INT1}$ (sela eksternal 1)
P3.4	T0 (masukan pewaktu eksternal 0)
P3.5	T1 (masukan pewaktu eksternal 1)
P3.6	WR (sinyal tulis memori data eksternal)
P3.7	RD (sinyal baca memori data eksternal)

Reset : Inputan Reset akan memberikan logika *High* (1) pada pin ini dengan jangka waktu yang ditentukan oleh lamanya pengosongan data muatan kapasitor. Jangka waktu minimal adalah 2 siklus mesin (24 periode frekuensi clock) ditambah waktu start On Osilator.



Gambar 2.3 Rangkaian Power On Reset
Sumber : Belajar Mikrokontroler AT89C51/52/55

ALE/ $\overline{PROG}$: Keluaran ALE (*Address Latch Enable*) menghasilkan pulsa - pulsa untuk menutup byte rendah (*Low Byte*) alamat selama mengakses memori eksternal. Pin ini juga berfungsi sebagai inputan pulsa program (*The Program Pulse Input*) atau $\overline{PROG}$ selama melakukan Flash Program. Pada operasi normal, ALE akan berpulsa dengan laju 1/6 dari frekuensi kristal dan dapat digunakan sebagai pewaktuan.

(*Timing*) atau pendetakan (*Clocking*) rangkaian eksternal. Sebagai catatan ada sebuah pulsa yang dilewati selama pengaksesan memori data eksternal. Jika dikehendaki operasi ALE dapat dinonaktifkan dengan cara mengatur bit 0 dari SFR (*Special Function Register*) lokasi 8Eh. Jika diberi logika '1' ALE hanya akan aktif selama

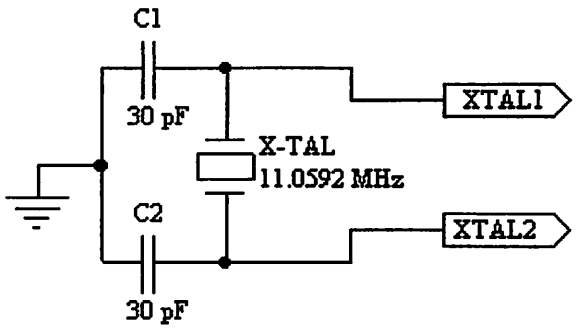
menemui instruksi **MOVX** atau **MOVC**. Selain itu, pin ini secara perlahan akan di Pull High. Mematikan bit ALE tidak akan ada efeknya jika mikrokontroller mengeksekusi program secara eksternal.

$\overline{PSEN}$: $\overline{PSEN}$ (*Program Store Enable*) merupakan sinyal baca untuk memori program eksternal. Ketika mikrokontroller AT89S52 menjalankan kode dari program eksternal, maka $\overline{PSEN}$ akan diaktifkan sebanyak 2 kali per siklusnya, kecuali dua aktivasi $\overline{PSEN}$ dilompati (diabaikan) saat mengakses memori data eksternal.

$\overline{EA}$ / **VPP** : $\overline{EA}$ / VPP (*External Access Enable*) harus selalu dihubungkan ke Ground jika digunakan untuk mengakses eksternal memori dengan lokasi 0000H sampai FFFFH. Catatan sekalipun bit '1' sudah terkunci dan terprogram, maka EA akan terkunci pada reset. $\overline{EA}$ juga harus dihubungkan ke Vcc untuk menjalankan program secara internal. Pada saat Flash Programming pin ini mendapatkan tegangan sebesar 12 Volt.

XTAL 1 : Merupakan input ke penguat pembalik osilator dan ke rangkaian operasi Clock internal.

XTAL 2 : Keluaran dari penguat pembalik osilator.



Gambar 2.4 Rangkaian Osilator
Sumber : Belajar Mikrokontroler AT89C51/52/55

Mikrokontroller AT89S52 memiliki rangkaian osilator internal dengan mengacu pada frekuensi referensi pada pin XTAL1 dan XTAL2.

Watchdog Timer (WDT) :

Fungsi dari WDT (*Watchdog Timer*) sebenarnya adalah untuk melakukan peresetan secara otomatis. Dimana dia akan mereset mikrokontroller jika mikrokontroller sedang hang. Oleh sebab itu user harus selalu mereset WDT sebelum WDT mereset mikrokontroller, jika WDT tidak direset oleh mikrokontroller dalam jangka waktu yang telah ditentukan maka secara otomatis WDT – lah yang akan mereset mikrokontroller. WDT terdiri dari suatu 14-bit counter dan Watchdog Timer Reset (WDTRST) SFR. WDT diset default untuk menonaktifkan reset yang ada. Tidak ada jalan lain untuk menonaktifkan WDT kecuali melalui Reset (baik Hardware reset atau WDT Overflow reset). Jika WDT Overflow, itu akan membuat suatu keluaran Reset High di Pin RST.

Untuk mengaktifkannya user harus menulis 01EH dan 0E1H di dalam daftar urutan WDTRST (alamat SFR-nya 0A6H). Ketika WDT aktif, pemakai harus mengisinya dengan menuliskan 01EH dan 0E1H ke WDTRST untuk menghindari

mengisinya dengan menuliskan 01EH dan 0E1H ke WDTRST untuk menghindari suatu WDT Overflow. 14-Bit Counter akan Overflow jika mencapai angka 16383 (3FFFH), dan ini akan mereset mikrokontroller. Disaat WDT aktif, dia akan menaikkan tiap-tiap siklus mesin ketika osilator sedang menjalankannya. Dan ini artinya pemakai harus mereset WDT sedikitnya tiap-tiap 16383 (3FFFH) siklus mesin. Untuk mereset WDT pemakai harus menulis 01EH dan 0E1H ke WDTRST, WDTRST adalah suatu write-only register. WDT counter tidak bisa dibaca atau ditulis. Ketika WDT Overflow, itu akan menghasilkan suatu keluaran RESET di pin RST. Jangka waktu Reset adalah 98 x Tosc, dimana Tosc = $\frac{1}{Fosc}$. Untuk membuat penggunaan terbaik dari WDT adalah user harus mengisikan bagian dari kode – kode itu yang akan mereset WDT sebelum WDT mereset mikrokontroller.

Dual DPTR (Data Pointer Register)

DPTR sebenarnya digunakan untuk melakukan transaksi dengan memori eksternal. Ini dikarenakan dalam keluarga MCS – 51 tidak dapat melakukan pemindahan data secara langsung dari RAM Internal dengan memori Eksternal. Pemindahan data semacam ini memerlukan DPTR untuk memberitahukan dimana alamat tepatnya data akan dipindahkan dari RAM Internal atau dari RAM Internal ke Memori Eksternal. Perbedaan antara AT89S52 dengan AT89C52 adalah bahwa AT89S52 diberikan Dual DPTR sedangkan di AT89C52 hanya sebuah, jadi untuk pengaksesan dari RAM Internal atau sebaliknya akan lebih cepat jika menggunakan AT89S52.

ISP Port : ISP Port digunakan untuk melakukan pemrograman secara langsung tanpa harus melepaskan IC dari tempatnya, cara ini digunakan agar lebih efisien pada waktu melakukan pemrograman, jika terjadi kesalahan maka kita tidak perlu melepaskan IC tersebut untuk kembali memprogramnya di Downloader AT89S52. Tapi kita hanya perlu memberikan akses pada pin – pin Port 1. Tepatnya pada pin P1.5 untuk MOSI, P1.6 untuk MISO dan P1.7 digunakan untuk SCK.

2.1.4. Register Fungsi Khusus

Register dengan fungsi khusus (Special Function Register) atau disebut juga SFR terletak pada 128 *byte* bagian atas memori data internal. Wilayah SFR ini terletak pada alamat 80H sampai FFH. Pengalamatannya harus diakses secara langsung baik per bit atau per *byte*. Secara perangkat keras, SFR ini dibedakan dengan memori data internal. Beberapa SFR yang digunakan dalam perancangan sistem penghitung waktu adalah :

- Accumulator

  Merupakan register untuk operasi penambahan dan pengurangan.

- PSW (Program Status Word)

  Terdiri dari beberapa bit status yang menggambarkan kejadian di accumulator sebelumnya. Terdiri dari *carry bit*, *auxiliary carry*, dua bit pemilih bank, bendera overflow, parity bit dan dua bendera yang dapat didefinisikan sendiri oleh pemakai.

- SP (Stack Pointer)

  Merupakan register 8 bit. Register SP dapat diletakkan pada alamat manapun pada RAM internal. Isi register ini ditambah sebelum data disimpan, selama instruksi PUSH dan CALL. Pada saat reset, register SP diinisialisasi pada alamat 07H sehingga stack akan dimulai pada lokasi 08H.

- DPTR (Data Pointer)

  Terdiri dari dua register, yaitu untuk byte tinggi (Data Pointer High) dan untuk byte rendah (Data Pointer Low). Fungsinya untuk menahan alamat 16 bit.

- Port 0 sampai Port 3

  Merupakan register yang berfungsi untuk membaca dan mengeluarkan data pada port 0, 1, 2 dan 3. Masing – masing register ini dapat dialamati secara per bit maupun per byte.

2.1.5. Metode Pengalamatan

Metode pengalamatan yang digunakan pada keluarga MCS – 51 adalah sebagai berikut :

a. Pengalamatan Tak Langsung

   Operasi pengalamatan tak langsung menuju ke sebuah register yang berisi lokasi alamat memori yang akan digunakan dalam operasi. Lokasi yang nyata tergantung dari isi register saat instruksi dijalankan. Untuk melaksanakan pengalamatan tak langsung digunakan simbol @.

Contoh :

ADD A, @R0; Tambahkan isi RAM pada register 0 ke akumulator.

DEC @R1; Kurangi dengan 1 isi RAM pada alamat R1.

b. Pengalamatan Langsung

Pengalamatan Langsung dilakukan dengan memberi nilai ke suatu register secara langsung. Untuk melaksanakan hal tersebut digunakan tanda #.

Contoh :

MOV A, # 01H; Isi akumulator dengan bilangan 01H.

MOV DPTR, # 19AB; Isi DPTR dengan bilangan 19ABH.

Pengalamatan data langsung dari 0 sampai 127 akan mengakses register perangkat keras.

Contoh :

MOV P3, A; Pindahkan isi akumulator ke alamat data B0H (alamat port 3)

INC 50; Naikkan lokasi 50 (desimal) dalam memori.

2.1.6. Bahasa Assembler

Bahasa Assembler merupakan tata cara untuk mewakili operasi CPU dalam format bahasa simbol yang disusun berurutan dalam pernyataan – pernyataan. Masing – masing pernyataan akan menterjemahkan ke dalam instruksi bahasa mesin atau operasi biner yang disebut operasi code/ OPCODE. Dalam penulisan bahasa mesin untuk program assembler umumnya, terdapat berbagai macam kelompok instruksi, diantaranya perpindahan data.

Instruksi ini memindahkan data antara register – register, memori – memori, register – memori, antara muka register dan antara muka memori.

Contoh :

MOV A, R0; Menyalin isi register R0 ke akumulator.

MOV A, @R0; Menyalin data di alamat yang ditunjukkan isi register R0 ke akumulator.

2.1.6.1. Operasi Aritmatik

Instruksi ini melaksanakan operasi aritmatik yang meliputi penjumlahan, pengurangan, perkalian maupun pembagian.

Contoh :

ADD A, #DATA; Menambah akumulator dengan data.

ADC A, #DATA; Menambah akumulator dan carry.

INC R4; Menambah isi R4 dengan 1.

DEC R4; Mengurangi isi R4 dengan 1.

MUL A, B; Mengalikan isi akumulator dengan isi register B.

DIV A, B; Membagi isi akumulator dengan isi register B.

2.1.6.2. Operasi Percabangan

Instruksi ini mengubah urutan normal pelaksanaan suatu program untuk melaksanakan program di lain tempat yang kita perlukan pada saat itu.

Contoh :

- CJNE (*Compare Memory to Accumulator*)

  Instruksi ini membandingkan isi lokasi memori tertentu dengan isi akumulator, jika sama instruksi selanjutnya akan dieksekusi. Jika tidak sama, eksekusi akan ke alamat kode.

- JB (*Jump if Bit Set*)

  Instruksi ini menguji suatu alamat bit. Jika berisi satu, eksekusi akan menuju ke alamat kode, jika tidak instruksi selanjutnya akan dieksekusi.

- JNB (*Jump if Bit Not Set*)

  Instruksi ini menguji alamat bit. Jika berisi 0 (nol), eksekusi akan menuju ke alamat kode. Jika berisi 1 (satu), instruksi selanjutnya yang akan dieksekusi.

2.2. Keypad

Keypad digunakan sebagai sarana memasukkan data ke minimum sistem. Untuk rangkaian keypad digunakan IC encoder jenis CMOS tipe MM 74C922. Dipilih 74C922 karena di dalam IC tersebut sudah memiliki beberapa kelengkapan, seperti misalnya rangkaian anti *debounching* yang hanya memerlukan satu kapasitor eksternal. Rangkaian internal register akan mengingat tombol terakhir yang ditekan meskipun tombol sudah dilepas. IC ini memiliki 4 bagian baris dan 4 bagian kolom sehingga dapat dipakai sebagai keypad 4x4.

Dengan penyemat X_1, X_2, X_3, X_4 untuk kolom dan Y_1, Y_2, Y_3, Y_4 untuk baris dapat dibuat keypad 4x4 sehingga keseluruhan ada 16 tombol. Tabel kebenaran

untuk ke-16 tombol tersebut terhadap logika keluaran pada penyemat A, B, C dan D dapat dilihat dalam Tabel 2.3.

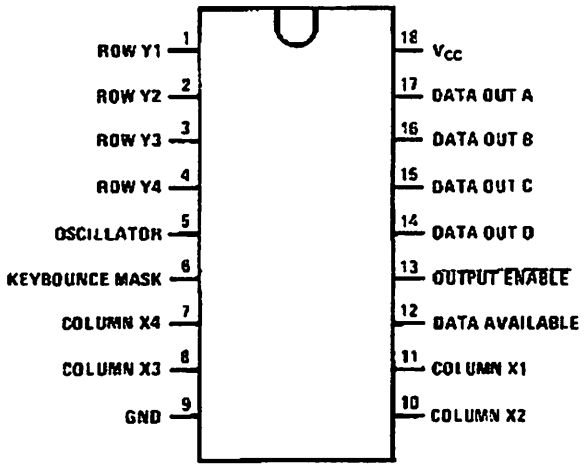
Tabel 2.3 Kombinasi Masukan Keypad Matrik 4x4 IC 74C922
Sumber : Data Sheet IC 74C922

P	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X
I	1	2	3	4	1	2	3	4	1	2	3	4	1	2	3	4
N	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y
	1	1	1	1	2	2	2	2	3	3	3	3	4	4	4	4
A	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1
B	0	0	1	1	0	0	1	1	0	0	1	1	0	0	1	1
C	0	0	0	0	1	1	1	1	0	0	0	0	1	1	1	1
D	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1

Posisi tombol terhadap kolom (Cn) dan barisnya (Bm) serta pin yang tersedia ditunjukkan dalam Gambar 2.5.

	C1	C2	C3	C4
B1	1	2	3	COR
B2	4	5	6	MEN
B3	7	8	9	UP
B4	CAN	0	ENT	DOWN

Gambar 2.5 Posisi tombol terhadap kolom (Cn) dan barisnya (Bm) serta pin yang tersedia n dan m nomor kolom dan baris
Sumber : Perancangan



Gambar 2.6 Konfigurasi Pin IC 74C922
Sumber : Data Sheet IC 74C922

Keterangan :

- Pin 1 – 4 (Row Y_1 - Row Y_4), sebagai input dari baris.
- Pin 5 (Oscillator), sebagai Clock Input.
- Pin 6 (Keybounce Mask), sebagai kunci input.
- Pin 7, 8, 10, 11 (X_4 , X_3 , X_2 , X_1), sebagai input dari kolom.
- Pin 9, sebagai ground untuk rangkaian yang dipakai.
- Pin 12, sebagai output data available.
- Pin 13, sebagai output enable.
- Pin 14 – 17, sebagai output data.
- Pin 18, Vcc.

2.3. LCD M 1632

Untuk tampilan dalam tugas akhir ini, digunakan LCD M 1632. Tampilan jenis ini tersusun dari dot matriks dan dikontrol oleh ROM/ RAM generator karakter dan RAM *data display*. Semua fungsi display dikontrol dengan instruksi dan LCD dapat dengan mudah diantarmukakan dengan mikroprosesor unit.

Adapun karakteristik dari LCD M 1632 adalah sebagai berikut :

- 16x2 karakter dengan 5x7 dot matriks.
- ROM generator karakter dengan 192 tipe karakter.
- RAM generator karakter dengan 8 tipe karakter (untuk program write).
- 80x8 bit RAM data *display* dengan 80 karakter maksimal.
- Dapat diantarmukakan dengan MPU 4 atau 8 bit.
- RAM data dan RAM generator karakter dapat dibaca dari MPU.
- Rangkaian oscilator terpadu.
- Catu daya tunggal +5 volt.
- Reset otomatis terpadu.
- Temperatur antara 0 °C sampai 50 °C.

Adapun untuk menampilkan karakter yang ada dilakukan dengan cara memberikan kode karakter untuk tiap-tiap karakter yang diinginkan pada bus data dan dengan menggunakan sinyal kontrol E, RS, dan R/$\overline{W}$.

Tabel 2.4 Konfigurasi Pena LCD M 1632

Sumber : LCD Module User Manual

Nama Sinyal	Jumlah Teminal	I/O	Tujuan	Fungsi
DB0 – DB3	4	I/O	MPU	4 bit bus data *lower tristate* dua arah, dapat dibaca/ ditulis terhadap MPU
DB4 – DB7	4	I/O	MPU	4 bit bus data *upper tristate* dua arah, dapat dibaca/ ditulis terhadap MPU, DB7 juga sebagai *busy flag*
$\overline{E}$	1	Input	MPU	Sinyal tanda mulai operasi yang berfungsi sebagai alat baca/ tulis
R/$\overline{W}$	1	Input	MPU	0 : Write 1 : Read

RS	1	Input	MPU	Sinyal seleksi register : 0 : Register Instruksi (tulis) 1 : Data Register (baca/ tulis)
V_{CC}	1	-	Power Supply	Untuk mengatur kontras pada LCD
V_{DD}	1	-	Power Supply	+5 V
V_{SS}	1	-	Power Supply	0 V (ground)

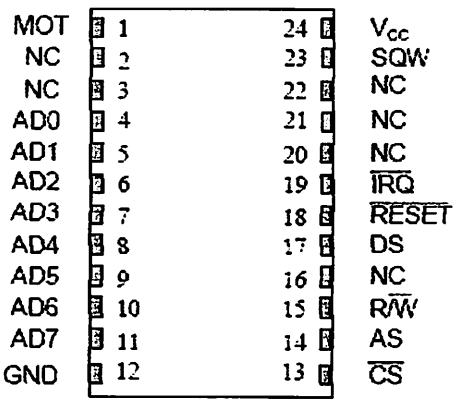
2.4. *Real Time Clock DS 12C887* (RTC DS 12C887)

Adapun karakteristik dari RTC DS 12C887 adalah sebagai berikut :

- Pengganti jam / kalender komputer IBM AT.
- PIN kompatibel / sesuai dengan MC 146818B dan DS 1287.
- Data tidak akan hilang maksimal sampai 10 tahun meskipun tidak ada daya.
- Subsistem tercakup sendiri meliputi lithium, kwarsa, dan rangkaian pendukung lainnya.
- Menghitung detik, menit, jam, hari, hari dalam seminggu, tanggal, bulan dan tahun dengan lompatan pergantian tahun.
- Data waktu, kalender atau alarm dapat dipresentasikan dalam format biner / BCD.
- *Clock* 12 atau 24 jam dengan *AM* dan *PM* dalam mode 12 jam-an.
- Pilihan waktu penyimpanan siang hari.
- *Timing bus* dapat dipilih antara Motorola dan Intel.
- Bus multipleks untuk efisiensi PIN.
- Interface dengan software dengan lokasi RAM 128 byte

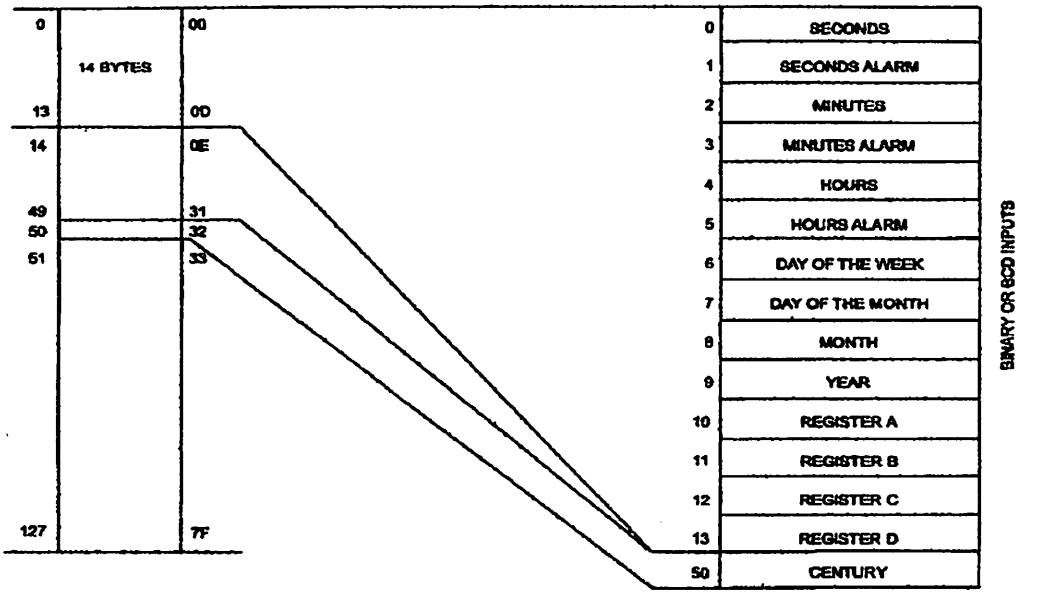
- 15 *byte clock* dan register kontrol
- 113 *byte* RAM untuk keperluan umum

- Tiga penyelaan terpisah dalam *software* yang dapat dilindungi dan dapat diuji
  - Waktu harian alarm sekali/ detik atau sekali/ hari.
  - Laju periodik dari 122 ms sampai 500 ms.
  - Akhir clock memperbaharui putaran.



Gambar 2.7 Konfigurasi PIN dari RTC DS 12C887
Sumber : Data Sheet RTC DS 12C887

RTC DS 12C887 buatan Dallas Semiconduktor ini selain menyediakan data – data mengenai waktu yang dapat ditampilkan dalam format biner atau BCD juga menyediakan RAM internal sebesar 128 *bytes*. RAM internal terdiri atas 15 *bytes* yang digunakan untuk *clock* dan register kontrol, sedangkan 115 *bytes* lainnya dapat digunakan oleh pemakai. Pembagian alamat RAM internal RTC DS 12C887 ditunjukkan dalam gambar 2.8.



Gambar 2.8 Pembagian Alamat RAM DS 12C887
Sumber : Data Sheet RTC DS 12C887

Tabel 2.5 Fungsi Penyemat RTC DS 12C887
Sumber : Data Sheet RTC DS 12C887

Penyemat	Fungsi
Vcc dan GND	Merupakan penyemat catu daya, Vcc dihubungkan pada catu daya positif dan GND pada ground. Tegangan catu daya adalah 5 Volt.
MOT (Motel)	Memilih mode diagram pewaktuan. Apabila dihubungkan pada Vcc berarti diagram pewaktuan Motorola yang dipakai, jika dihubungkan dengan ground berarti sistem pewaktuan lain yang dipakai (Intel).
SQW (Square Wave Output)	Mengeluarkan sebuah sinyal dari 15 periode yang ada. Besar frekuensi SQW dapat diubah dengan diprogram pada register A. Untuk mengaktifkan/ menonaktifkan sinyal SQW dipilih lewat bit SQW pada register B.
AD0 – AD7 (Address Data 0 – 7)	Bus data dan bus alamat yang masih termultipleks. Pengiriman data maupun alamat dilakukan melalui bus ini.
AS (Address Strobe)	Untuk memisahkan bus data dan bus alamat (ALE). Tepi turun dari ALE akan menyebabkan alamat ditahan 12C887 secara

	internal.
DS (Data Strobe)	Berfungsi sama dengan sinyal OE (Output Enable) pada komponen memori. Sinyal DS dihubungkan dengan sinyal RD yang berasal dari mikrokontroller untuk melakukan proses membaca data pada RAM internal RTC.
CS (Chip Select)	Mengaktifkan piranti RTC. Sinyal CS didapat dari dekoder alamat dengan alamat tertentu.
IRQ (Interrupt Request)	Untuk menginterupsi mikrokontroller. Untuk mereset IRQ, mikrokontroller memberikan program pada register C pada RTC. Saat tidak terdapat interupsi, penyemat ini dalam kondisi impedansi tinggi.
RESET	Untuk mereset beberapa flag menjadi nol tetapi tidak berpengaruh pada unjuk kerja clock, kalender dan fungsi RAM.
R/ W (Read/ Write)	Untuk membaca dan menulis data pada RTC.
RCLR (RAM clear)	Menghapus data – data pada RAM dengan cara menghubungkan penyemat atau RCLR dengan ground.

2.5. *Information Storage Device* 1420 (ISD 1420)

ISD (Information Storage Device) adalah rangkaian terpadu serpih tunggal yang mempunyai persamaan dengan CMOS LSI. Seri ISD 1420 Chip Corder merupakan peralatan yang dirancang untuk merekam dan memutar kembali suara atau bunyi dalam suatu chip. Suatu solusi yang tepat untuk merekam dan memutar kembali suatu pesan pendek atau suatu aplikasi tertentu.

IC ISD 1420 mempunyai perlengkapan di dalam antara lain : Osilator Internal, Microphone pre-amplifier, Gain kontrol otomatis, Filter perata dan Speaker amplifier (penguat speaker). Secara keseluruhan seri ISD 1420 dapat dilakukan sebuah perekam atau pemutar dengan komponen yang sederhana seperti microphone, speaker, beberapa komponen penunjang, dua buah saklar tekan dan sumber tegangan. Rekaman akan disimpan dalam sel memori yang tidak mudah hilang (non-volatile),

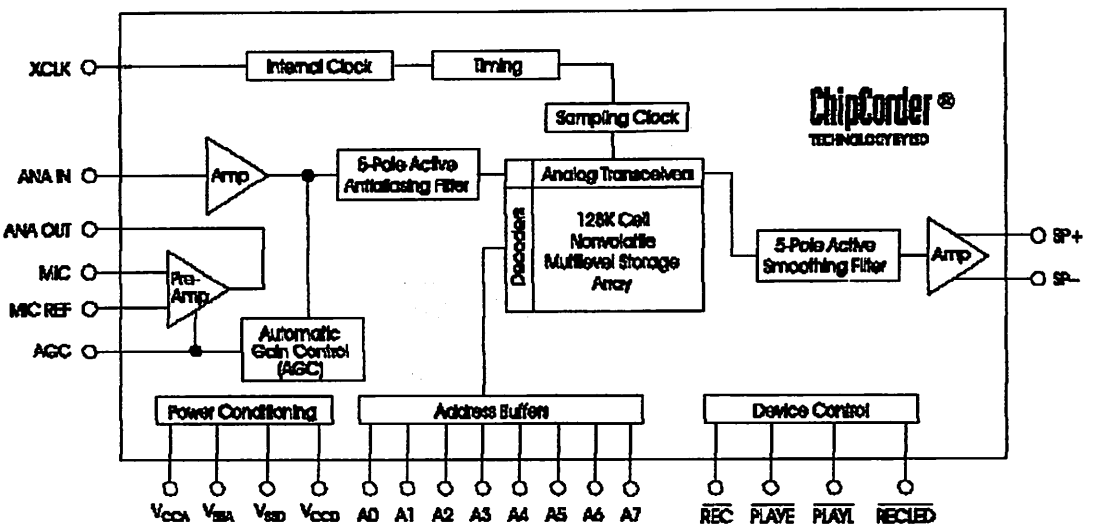
memberikan tempat penyimpanan yang masih kosong. Cara unik ini yang membuat ISD disebut Storage Direct Analog (DAST) atau teknik penyimpanan analog langsung, dengan jalan sinyal suara (voice) dan bunyi disimpan secara langsung dalam bentuk analog ke dalam memori EPROM.

Dalam penggunaannya, IC ini dalam menyimpan data sinyal suara dapat menggunakan static RAM atau ROM. Jika memakai static RAM data suara dapat diganti, data tetap ada selama catu daya masih diberikan, tetapi memori yang dipakai ROM/ EPROM, maka IC ini hanya berfungsi untuk produksi suara.

Penyimpanan analog langsung memungkinkan reproduksi suara secara alami dalam bentuk satu chip tunggal. Perekaman akan berhenti bila input REC tertekan HIGH. Tanda akhir dari pesan (end – message marker) akan otomatis tertekan sesudah itu, tanda ini juga berguna untuk memutuskan playback otomatis bila rekaman sudah habis. ISD akan langsung ke mode stanby bila REC dalam keadaan HIGH.

ISD 1420 mempunyai waktu penyimpanan suara selama 20 detik. Susunan ISD 1420 DAST adalah dalam 160 segmen dari alamat A0 sampai A7 yang menunjukkan akses setiap segmen dalam kesatuan untuk alamat pesan. Kemampuan pemberian atau penyediaan alamat yang berupa pesan yang disimpan dalam bentuk kalimat dan suara.

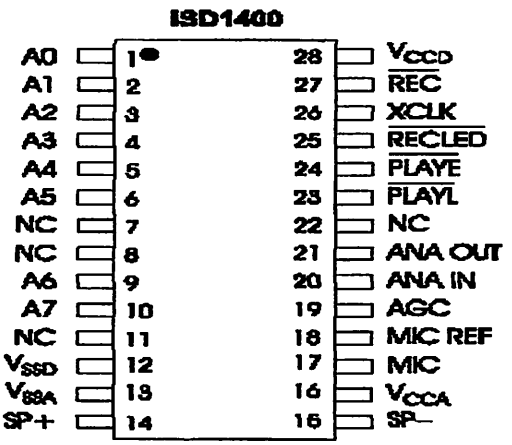
Tanda akhir pesan (*end – of message marker*) akan otomatis terekam sesudah itu. Tanda ini berguna untuk memutuskan playback secara otomatis bila rekaman sudah habis. ISD akan langsung ke stanby bila REC dalam keadaan HIGH. Blok diagram dari ISD 1420 dapat dilihat pada gambar 2.9 di bawah ini :



Gambar 2.9 Blok Diagram ISD 1420
Sumber : Data Sheet ISD 1420

2.5.1. Konfigurasi Pin – Pin ISD 1420

IC rekam atau ulang ISD 1420 mempunyai jumlah kaki atau pin 28 buah, seperti pada gambar 2.10.



Gambar 2.10 Konfigurasi PIN dari IC ISD 1420
Sumber : Data Sheet ISD 1420

Keterangan dan fungsi dari masing – masing PIN dapat dijelaskan sebagai berikut :

- Playback, edge – activated (PLAYE), pin 24 :

  Ketika sinyal akan berpindah menuju ke LOW (*low – going transition*) terdeteksi di input ini, maka PLAYE akan berjalan. Playback berjalan sampai tanda akhir dari pesan tercapai atau akhir dari ruang memori tercapai. Setelah menyelesaikan playback, ISD secara otomatis akan kembali ke mode stanby, menekan PLAYE ke HIGH pada waktu playback berjalan tidak akan menghentikan dari playback. Jadi playback akan berhenti bila mencapai akhir dari pesan atau ruang memori habis.

- Playback, level – activated (PLAYL), pin 23 :

  Ketika sinyal input ini berpindah dari high ke low, maka PLAYL akan berjalan. Playback akan berjalan sampai input ini tertekan high, tanda akhir dari pesan tercapai atau ruang memori sudah habis. ISD akan kembali ke mode stanby setelah playback ini terhenti.

- Record Led Output (RECLED), pin 25 :

  Output dari RECLED akan low selama perekaman, maka output ini biasanya digunakan untuk menjalankan sebuah LED yang berguna untuk mengetahui bahwa sedang terjadi proses perekaman. RECLED ini akan low sebentar ketika tanda akhir dari pesan tercapai pada saat Playback.

- Record (REC), pin 27 :

  Input sinyal akan aktif dalam keadaan low. ISD 1420 akan merekam bila REC dalam keadaan low, dan sinyal ini harus terus dalam keadaan low bila ingin terus merekam. Jika input REC ini tertekan low dalam keadaan

kita masih memutar ulang (playback), maka playback akan berhenti dan ISD akan merekam. Frekuensi rendah bila akhir dari suara (the low – frekuensi end of the voice panssband). Dalam perancangan dan pembuatan alat ini, harga kapasitor ditentukan sama dengan yang terdapat dalam data sheet ISD 1420.

- Automatic Gain Control (AGC), pin 19 :

  Kegunaan dari AGC adalah untuk menambah atau mengurangi secara otomatis penguatan (*gain*) dari pre-amplifier. Dan juga meluaskan batas dari sinyal input yang dapat digunakan oleh microphone tanpa terjadi distorsi. AGC ini dapat secara dinamis meluaskan batas dari suara bisikan sampai suara yang keras. Untuk menggunakan fasilitas AGC ini, resistor dan kapasitor luar (eksternal) harus dihubungkan secara paralel antara pin AGC dengan ground. Harga yang direkomendasikan adalah R = 470 kΩ dan C = 4,7 μF. Dalam perancangan alat ini digunakan juga harga seperti diatas, sesuai dengan yang terdapat pada data sheet ISD 1420.

- Speaker Output (SP+ dan SP-), pin 14 dan 15

  Pin SP (+) dan SP (-) digunakan untuk mengeluarkan suara yang telah direkam ke speaker atau ke device lainnya. Output ini mempunyai impedansi sebesar 16 Ω.

- Optimal Eksternal Clock (XCLK), pin 26 :

  Digunakan untuk menambahkan kristal clock bila dibutuhkan pewaktuan yang lebih besar dan presisi. Bila input ini tidak digunakan harus dihubungkan dengan ground.

- V_{CCA} dan V_{CCD}, pin 16 dan 28

Rangkaian Analog dan digital yang terdapat di dalam chip ISD 1420 menggunakan bus power yang terpisah untuk meminimalisasi noise. Pin power ini harus dihubungkan sedekat mungkin dengan sumber tegangan.

- V_{SSA} dan V_{SSD} (Ground), pin 13 dan 12 :

  Sama seperti V_{CCA} dan V_{CCD}, rangkaian analog dan digital di dalam ISD 1420 menggunakan bus ground yang terpisah untuk meminimalisasi noise. Pin ini harus dihubungkan sedekat mungkin dengan ground.

- Address Input (A0 – A7), pin 1-6 dan 9-10 :

  Input alamat ini mempunyai dua fungsi, tergantung pada level dari dua Most Significant Bits (MSB) dari alamat. Jika dua MSB ini kedua – duanya low, maka semua input digunakan sebagai bits pengalamatan (address bits) dan digunakan sebagai alamat untuk memulai (start address) dari perekam atau pemutaran ulang (playback). Kaki – kaki dari pengalamatan adalah hanya memasukkan dan bukan merupakan informasi keluaran pengalamatan internal (output internal address information) ketika proses operasi sedang berjalan.

  Ketika dua MSB ini kedua – duanya HIGH, maka sinyal input pengalamatan digunakan sebagai bits (mode bits). Pada saat ini mode operasi normal dan pengalamatan secara langsung tidak dapat digunakan secara langsung (*simultaneously*). Kedua MSB tersebut adalah pada kaki 9 dan 10 dari ISD 1420.

- Microphone – input (MIC), pin 17 :

  Kaki microphone ini terhubung dengan Vcc dengan microphone ground, maka tingkat noise selama perekaman dapat dikurangi. Noise ini

disebabkan oleh preamplifier yang terdapat di dalam chip. Bila pin ini digunakan maka tidak boleh dihubungkan dengan sinyal atau tegangan apapun, harus dalam keadaan terbukti.

- Analog Output (ANA OUT), pin 21 :

  Sinyal dari microphone dikuatkan dan dikeluarkan melalui ANA OUT pin. Penguatan tegangan dari pre-amp tergantung dari tingkat tegangan dari AGC (*Automatic Gain Control*) pin. Pre-amp ini mempunyai penguatan maksimum sekitar 24 dB untuk tingkat masukan sinyal kecil.

- Analog Input (ANA IN), pin 20 :

  Kapasitor eksternal menghubungkan antara ANA IN ke ANA OUT pin. Harga dari kapasitor luar bersama – sama dengan 3 kΩ input impedansi di ANA IN, dapat dipilih sendiri untuk memberikan keadaan cut-off (terputus).

2.5.2. Cara Perekaman Atau Pengisian Suara

Langkah – langkah yang dilakukan untuk memulai perekaman yang mengeset alamat atau durasi waktu yang dibutuhkan untuk perekaman. Pada saat memulai perekaman sinyal REC LOW, maka dengan demikian secara otomatis pin ANA-IN bekerja. Pada saat inilah dimasukkan suara yang akan direkam melalui microphone. Jika ruang sudah terisi penuh maka sinyal REC harus dikembalikan ke posisi HIGH. Tanda akhir dari pesan (*end – off – message merker*) akan otomatis terekam sesudah itu. Tanda ini berguna untuk memutuskan playback secara otomatis bila rekaman sudah habis. ISD 1420 akan langsung ke stanby bila REC dalam keadaan HIGH.

2.5.3. Mode Operasional

Mode operasional disini akan dibahas pada putar ulang. Pada perancangan disini diinginkan pengisyaratan pesan dapat sesuai dengan alamat pesan yang diinginkan. Yaitu setiap pemanggilan data pada alamat data dapat berlangsung secara acak dan tidak berurutan. Untuk mode operasional diatas dapat dipilih PLAYE atau PLAYL saja. PLAYL sebagai level activated untuk mencegah data melompat ke data berikutnya, pada kaki PLAYE diberi sinyal HIGH maka pointer akan mereset kembali data pesan. Untuk mode operasi seperti yang diinginkan di atas dengan jalan membuat kondisi REC menjadi LOW untuk selamanya. Sedangkan pada saat kaki PLAYE dan kaki PLAYL dijadikan satu dan diberi sinyal LOW maka proses putar akan berjalan dan pada saat kaki PLAYE dan PLAYL diberi sinyal HIGH, maka proses putar ulang akan berhenti sekaligus mereset kembali pointer data pesan.

2.6. Motor Arus Searah (Motor DC)

Motor arus searah (dc) adalah suatu mesin yang berfungsi mengubah tenaga listrik arus searah menjadi tenaga mekanik dimana tenaga gerak tersebut berupa putaran rotor. Dalam kehidupan sehari-hari motor arus searah sering dijumpai dimana-mana. Sebagai contoh adalah motor yang dipasang pada starter mobil, mainan anak-anak, tape recorder dan lain sebagainya. Sedangkan pada pabrik-pabrik, motor arus searah dapat dijumpai pada elevator, conveyor dan sebagainya.

2.6.1. Prinsip Dasar Motor Arus Searah (Motor DC)

Prinsip dasar dari motor arus searah adalah kalau sebuah kawat berarus diletakkan antara kutub magnet (U-S), maka pada kawat tersebut akan bekerja suatu

gaya yang akan menggerakkan kawat tersebut. Arah gerak dari kawat tersebut dapat ditentukan dengan " Kaidah Tangan Kiri " yang berbunyi sebagai berikut : " Apabila tangan kiri dibiarkan terbuka dan diletakkan diantara kutub utara dan kutub selatan, sehingga garis-garis gaya yang keluar dari kutub utara menembus telapak tangan kiri dan arus di dalam kawat mengalir searah dengan keempat jari, maka kawat tersebut akan mendapat gaya yang jatuhnya sesuai dengan ibu jari ", seperti pada gambar 2.11 di bawah ini. Adapun besarnya gaya yang bekerja pada kawat tersebut dapat dirumuskan sebagai berikut :

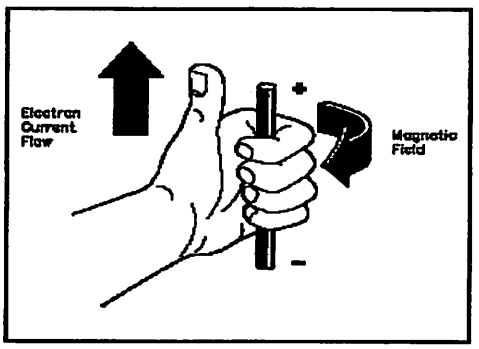
$F = B \times I \times L$ Newton

dimana :

B = kerapatan fluks magnet (Weber)

L = Panjang penghantar (meter)

I = Arus listrik (Ampere)



Gambar 2.11 Kaidah Tangan Kiri
Sumber : www. Google.com

2.7. Display Dot Matrik

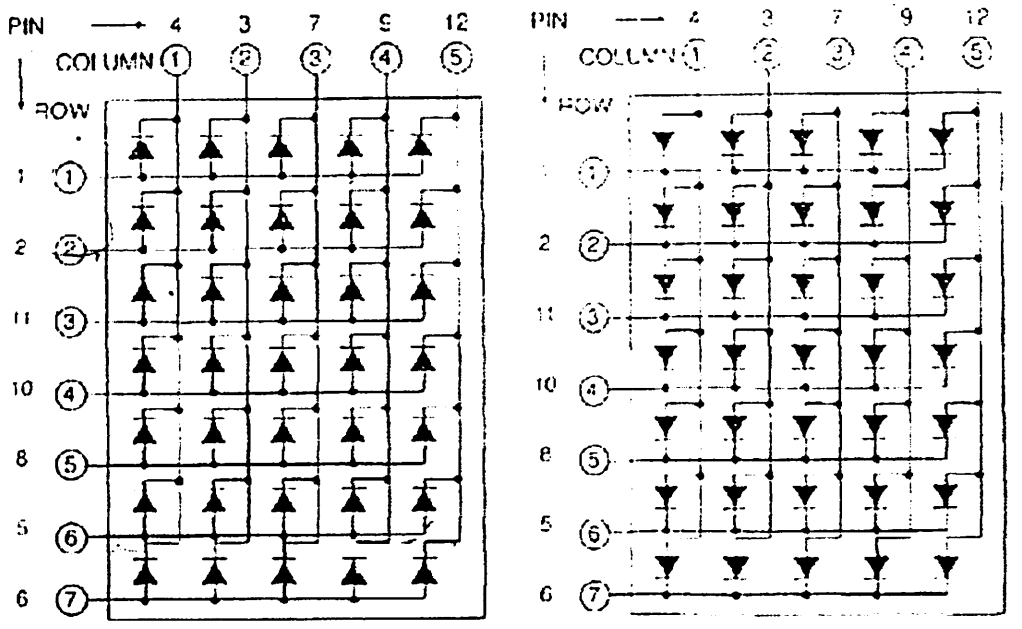
Display dot matrik merupakan sebuah chip yang berisi kumpulan dari beberapa led yang dikemas menjadi satu, kemasan led ini biasa disebut Led Dot Matrik.

Display dot matrik yang ada di pasaran disusun dengan berbagai komposisi, mulai 7x5, 8x5, 8x8 sampai 16x16. Angka pertama dari komposisi ini menunjukkan jumlah kaki anoda, sedangkan angka kedua merupakan jumlah kaki katoda.

Dalam tugas akhir ini dipakai rangkaian Led Dot Matrik 7x5, artinya dalam kemasan ini terdapat 35 buah led yang disusun menjadi 7 baris deretan led (kolom), setiap deretan led (baris) terdiri dari 5 buah led. Dengan demikian terminal yang keluar pada chip adalah 5 sambungan anoda dan 7 buah sambungan katoda.

Display dot matrik memiliki keistimewaan dibandingkan dengan tampilan yang lain, seperti : seven segment yaitu kemampuan untuk menampilkan karakter dan berbagai macam simbol.

Dot matrik merupakan kumpulan titik cahaya yang tersusun menjadi sejumlah kolom dan baris. Contohnya adalah matrik 7x5 yang ditunjukkan dalam gambar di bawah ini :



Gambar 2.12 Konfigurasi Dot Matrik
Sumber : Fairchild Semiconductor

Matrik LED ini terdiri dari 7 baris dan 5 kolom, ke 35 LED ini dapat menghasilkan berbagai macam dan bentuk karakter. Untuk menghidupkan satu LED dalam matrik ini dengan menerapkan tegangan ke anoda dan menghubungkan katodanya ke ground. Dengan menerapkan tegangan ke beberapa kolom tertentu dan menghubungkan beberapa baris tertentu ke ground. Setiap angka desimal, huruf, dan berbagai bentuk atau lambang lainnya dapat ditampilkan.

Untuk memperagakan karakter dengan tampilan matrik, LED yang diperlukan tidak dinyalakan secara bersamaan tetapi LED – LED ini diaktifkan baris demi baris dengan cepat. Proses ini diulangi untuk baris dan kolom – kolom berikutnya (scaning). Jadi sebenarnya hanya kolom – kolom pada satu baris tertentu yang menyala pada suatu saat. Tetapi karena proses dilakukan dengan cepat, mata menganggap bahwa LED – LED yang dimaksud menyala secara serentak.

2.8. Register Geser (Shift Register)

Register adalah kumpulan dari elemen – elemen memori yang bekerja bersama sebagai satu unit. Register yang paling sederhana tidak lebih dari sebuah penyimpanan kata biner, jenis lain dari register dapat mengubah kata yang tersimpan dengan menggeser bit – bitnya ke kiri atau ke kanan. Sebuah register geser dapat memindahkan bit – bit yang tersimpan ke kiri dan ke kanan.

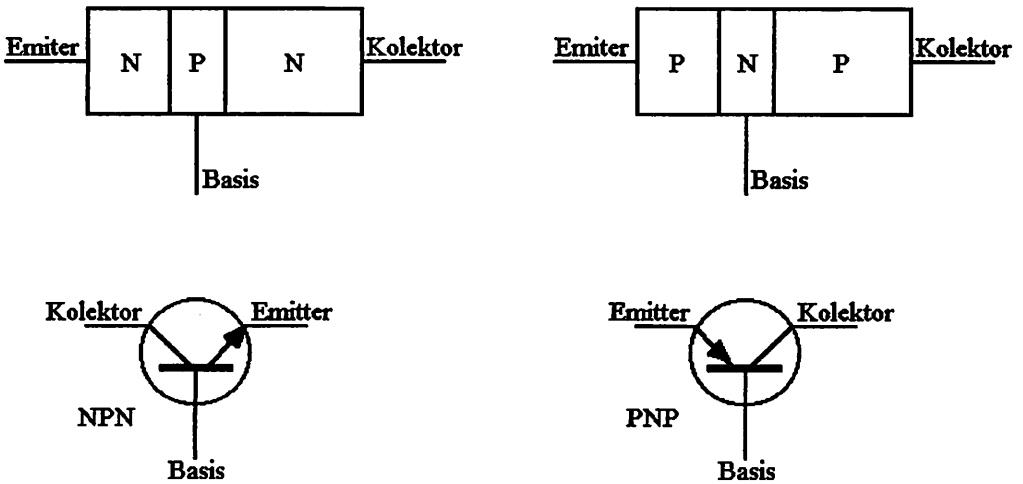
Rangkaian register geser (*Shift Register*) yang digunakan adalah IC 74LS164, yang berfungsi untuk menyimpan dan memindahkan data dari satu bagian ke bagian sistem yang lain. Prinsip kerjanya adalah masukan seri ke keluaran paralel (SIPO).

2.9. Transistor

Transistor merupakan salah satu komponen elektronika dengan terminal yang terdiri dari kolektor (C), Basis (B), dan Emitter (E). Setelah bahan semikonduktor dasar diolah, terbentuklah bahan semikonduktor jenis P dan N. Walaupun proses pembuatannya banyak, pada dasarnya transistor merupakan tiga lapis gabungan kedua jenis bahan tadi, yaitu NPN dan PNP.

Simbol sirkuit kedua jenis bahan tersebut hampir sama, perbedaannya hanya terletak pada arah panah di ujung emitter. Arah panah ini menunjukkan arah aliran arus konvensional yang berlawanan arah dalam kedua jenis tadi.

Adapun lambang komponen transistor NPN maupun PNP dapat dilihat pada gambar 2.13 di bawah ini.



Gambar 2.13 Lambang-lambang Transistor
Sumber : Malvino, Prinsip – Prinsip Elektronika

2.9.1. Transistor Sebagai Saklar

Suatu transistor dalam sistem kerjanya mengalami keadaan saturasi dan titik sumbat. Dengan demikian jika transistor digunakan sebagai saklar maka hubungan saklar ini terjadi antara kolektor dan emitor dari transistor tersebut. Sedangkan buka dan tutup saklar itu ditentukan oleh suatu tegangan yang diberikan pada basisnya.

- Saklar Terbuka

  Jika $V_B = 0$ Volt, $I_B = 0$ A, maka transistor dalam keadaan titik sumbat (cut-off) sehingga tidak ada arus yang mengalir dan saklar dalam keadaan terbuka.

- Saklar Tertutup

  Untuk mengembalikan saklar dalam keadaan tertutup maka harus diberikan tegangan input (Vin) pada V_b dan arus pada basis, sehingga keadaan transistor menjadi saturasi, dimana perpotongan dari garis beban dan kurva $I_B = I_{B(sat)}$. Keadaan ini seperti sebuah switch yang tertutup.

Jika transistor dikerjakan pada keadaan saturasi (Vce = 0,7 volt), maka antara kolektor dan emitor akan terhubung dengan cepat atau dengan kata lain saklar dalam keadaan tertutup. Adapun besarnya arus basis yang diperlukan untuk rangkaian ini dapat dicari melalui persamaan :

$$I_B = \frac{Ic}{\beta}$$

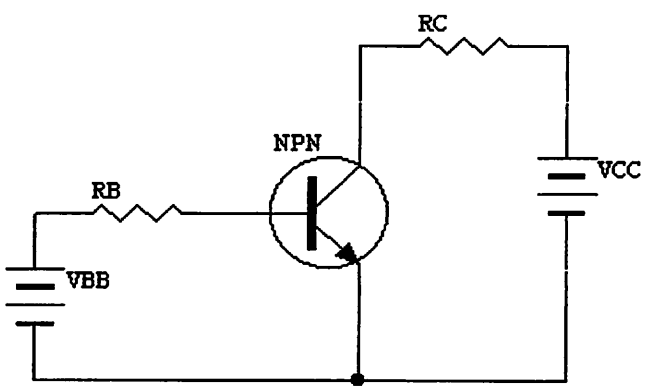
Maka nilai R_B dapat dicari sebagai berikut :

$$R_B = \frac{V_{bb} - V_{be}}{I_B}$$

Jika arus kolektor yang mengalir terlalu banyak, transistor akan menuju ke kondisi jenuh. Secara ideal terjadi suatu hubung singkat antara terminal kolektor dan emitor, dengan arus kolektor jenuh sebesar :

$$I_{c(sat)} \cong \frac{V_{cc}}{R_L}$$

Rangkaian transistor switch dapat dilihat pada gambar 2.14 di bawah ini.



Gambar 2.14 Transistor Sebagai Saklar
Sumber : Malvino, Prinsip – Prinsip Elektronika

2.10. Relay

Relay adalah switch/ saklar yang digerakkan secara elektronik. Kontak jenis ini adalah salah satu komponen bantu proses otomatisasi, walaupun kontak tersebut bersifat mekanis. Disini relay difungsikan untuk menghubungkan data yang ditransmisikan oleh mikrokontroller menuju bel listrik dan motor dc. Adapun karakteristik dari sebuah relay adalah sebagai berikut :

1. Tegangan Operasi, yaitu tegangan coil minimum yang diperlukan coil untuk dapat mengaktifkan kontak saklar relay dari posisi normal ke posisi operasi.
2. Tegangan lepas, adalah tegangan coil minimum yang diperlukan coil untuk dapat mengaktifkan kontak saklar relay dari posisi operasi ke posisi normal.
3. Tegangan maksimum, yaitu coil maksimum yang diperlukan coil untuk dapat bekerja tanpa merusak coilnya sendiri.
4. Tegangan normal, adalah tegangan kerja nominal sehingga coil dapat bekerja secara normal.

Adapun prinsip kerja dari relay yang kondisi normalnya Off (open) adalah :

a. Apabila lilitan terisolasi dari relay tersebut kita beri tegangan, maka akan timbul induksi.
b. Dengan adanya induksi maka besi (inti) yang diselubungi lilitan akan berubah sifatnya menjadi magnet yang bersifat sementara.

c. Karena besi tersebut menjadi bersifat magnet, maka akan dapat menarik besi lain yang berfungsi sebagai kontak sehingga relay menjadi On.

d. Jika tegangan pada lilitan dihilangkan, maka besi akan kembali seperti sifat semula sehingga relay menjadi Off.

BAB III

PERENCANAAN DAN PEMBUATAN ALAT

3.1. Penerapan Perangkat Keras (*Hardware*)

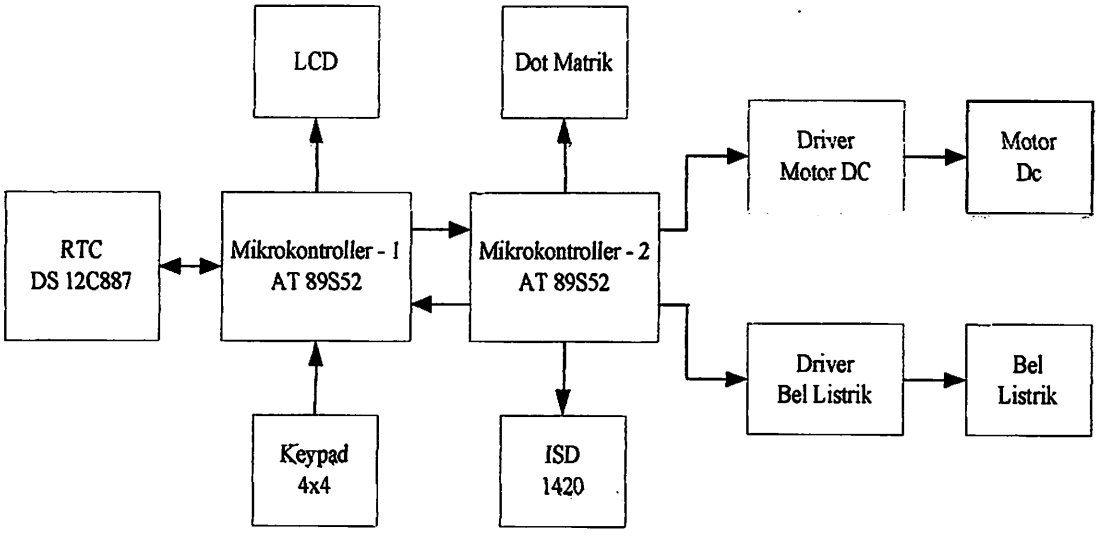
Dalam bab ini akan dijelaskan mengenai perancangan dan pembuatan bel sekolah otomatis yang dilengkapi dengan suara berbasis mikrokontroller AT89S52.

Pada perancangan alat ini secara keseluruhan dibagi menjadi dua bagian, yaitu :

1. Perancangan Perangkat Keras (*Hardware*)
2. Perancangan Perangkat Lunak (*Software*)

3.1.1. Diagram Blok

Diagram blok dari perangkat keras (*hardware*) yang direncanakan, diperlihatkan pada gambar 3.1.



Gambar 3.1 Diagram Blok Sistem

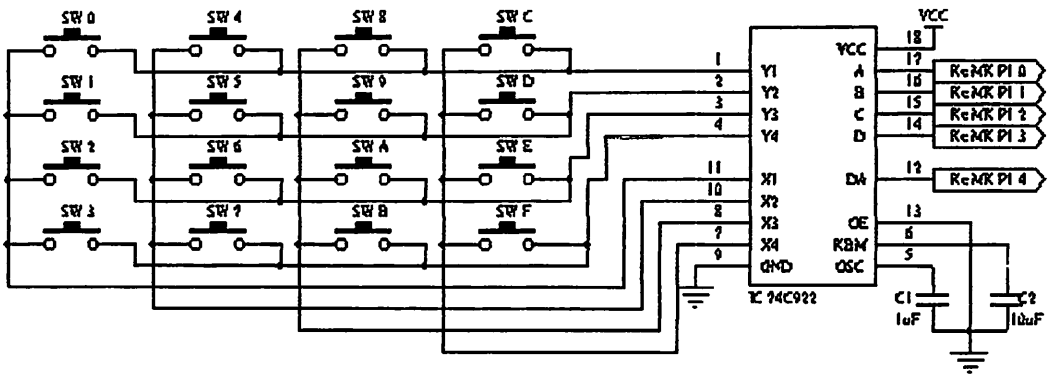
3.1.2. Cara Kerja Alat

Pertama kali user memasukkan waktu – waktu/ jam – jam tertentu sebagai ketentuan untuk masuk sekolah, istirahat dan waktu pulang sekolah melalui keypad ke dalam mikrokontroller AT89S52. Setelah itu mikrokontroller AT89S52 akan mendeteksi/ mencocokkan dengan waktu/ jam saat ini melalui RTC DS 12C887.

Jadi inputan mikrokontroller AT 89S52 berasal dari keypad dan RTC DS 12C887. Jika waktu inputan keypad tidak sama dengan waktu RTC DS 12C887, maka mikrokontroller AT89S52 akan mendeteksi atau mencocokkan secara terus menerus. Jika waktu inputan keypad sama dengan waktu RTC DS 12C887, maka akan muncul tampilan melalui display dot matrik. Dan pada saat itu pula mikrokontroller AT 89S52 akan mengaktifkan bel sekolah dan mengendalikan driver motor DC sebagai penggerak pintu gerbang sekaligus mengaktifkan driver ISD 1420 untuk memberikan informasi secara terjadwal.

3.1.3. Perencanaan dan Pembuatan Rangkaian Keypad

Untuk memasukkan waktu-waktu (jam-jam) tertentu yang terdiri dari waktu masuk sekolah, waktu istirahat maupun waktu pulang sekolah, maka dibutuhkan rangkaian keypad. Pada perencanaan dan pembuatan rangkaian keypad ini digunakan IC 74C922 dan keypad berukuran 4 x 4. Gambar 3.2 di bawah ini memperlihatkan suatu rangkaian keypad matrik 4 x 4 dengan IC 74C922.



Gambar 3.2 Keypad Matrik 4 x 4 dengan IC 74C922

Dari rangkaian di atas dapat diperoleh 16 kemungkinan output yang diperlihatkan pada Tabel 3.1.

Tabel 3.1 Kombinasi Output Keypad Matrik 4 x 4

Switch	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
Position	X1	X2	X3	X4	X1	X2	X3	X4	X1	X2	X3	X4	X1	X2	X3	X4
Output	Y1	Y1	Y1	Y1	Y2	Y2	Y2	Y2	Y3	Y3	Y3	Y3	Y4	Y4	Y4	Y4
A	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1
B	0	0	1	1	0	0	1	1	0	0	1	1	0	0	1	1
C	0	0	0	0	1	1	1	1	0	0	0	0	1	1	1	1
D	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1

Berdasarkan tabel di atas, kita dapat dengan mudah menyeleksi tombol angka mana yang ditekan pada rangkaian keypad yang dibuat. Keluaran tombol yang dipilih dihubungkan langsung pada port mikrokontroller AT89S52 dengan ketentuan port 1.0 untuk output A, port 1.1 untuk output B, port 1.2 untuk output C dan port 1.3

untuk output D sedangkan untuk strub masuk pada port 1.4 dan selanjutnya mikrokontroller AT89S52 akan mencocokkan/ mengkomper dengan RTC DS 12C887.

3.1.4. Perencanaan dan Pembuatan Rangkaian Mikrokontroller AT89S52

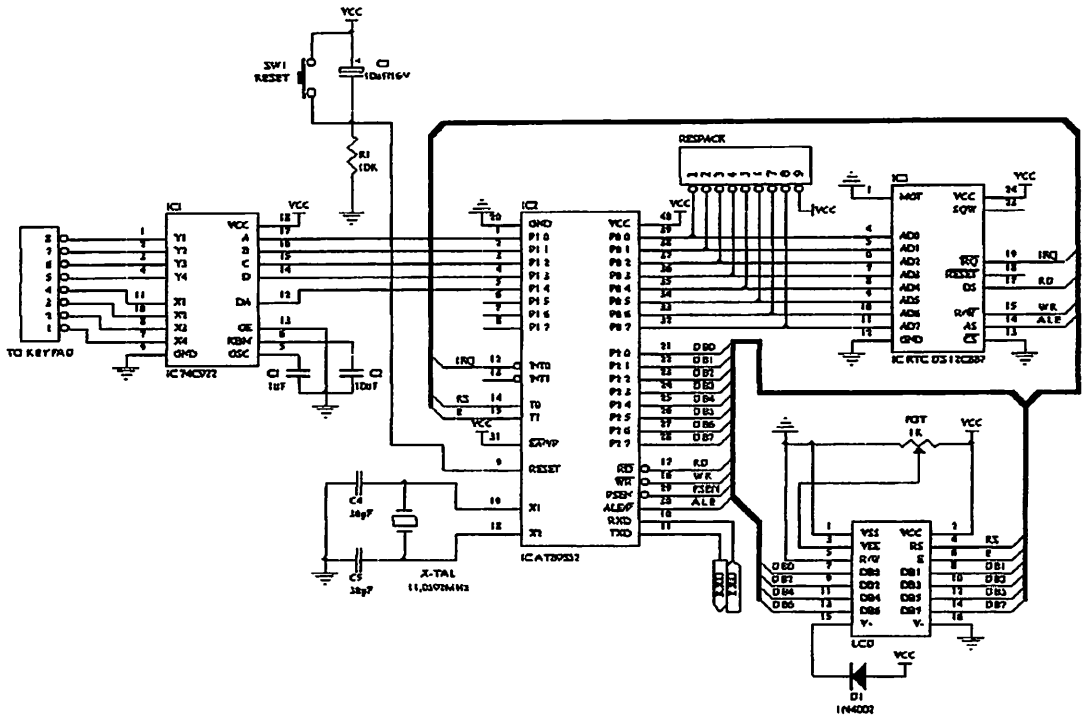
3.1.4.1. Rangkaian Mikrokontroller AT89S52

Mikrokontroller pada sistem ini berfungsi untuk mengolah data masukan dari keypad dan RTC DS 12C887 yang selanjutnya akan mengendalikan driver bel listrik, driver motor dc, driver ISD 1420 dan juga tampilan pada LCD serta tampilan pada dot matrik.

Mikrokontroller yang digunakan pada sistem ini adalah Mikrokontroller jenis AT89S52 yang merupakan IC CMOS 8 bit internal RAM, 40 pin dan 4 port I/ O.

Pada perencanaan dan pembuatan rangkaian mikrokontroller AT 89S52 ini dibagi menjadi dua bagian, yaitu : Rangkaian Mikrokontroller – 1 dan Rangkaian Mikrokontroller – 2, dimana pada rangkaian mikrokontroller – 1 digunakan sebagai masukan (inputan) dari keypad, RTC DS 12C887, serta tampilan pada LCD. Sedangkan pada mikrokontroller – 2 digunakan sebagai pengendali bel listrik, pengendali motor dc, pengendali ISD 1420, serta tampilan pada dot matrik.

Untuk lebih jelasnya Rangkaian Mikrokontroller – 1 dan Rangkaian Mikrokontroller – 2 dapat dilihat pada gambar 3.3 dan gambar 3.4 di bawah ini :

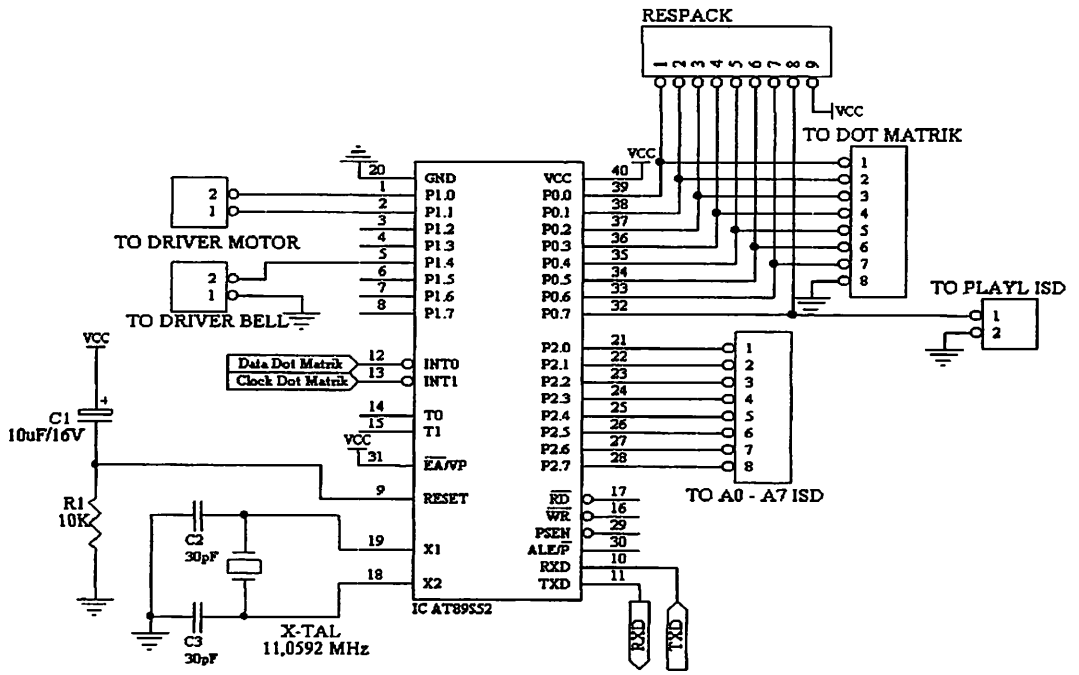


Gambar 3.3 Rangkaian Mikrokontroller – 1 AT89S52

Adapun fungsi dari masing-masing pin (kaki) dalam Mikrokontroller - 1 AT89S52 adalah sebagai berikut :

1. Pin 1 – Pin 5 (P1.0 – P1.4) merupakan port 1 mikrokontroller yang digunakan sebagai input bagi rangkaian keypad.
2. Pin 32 – Pin 39 (P0.0 – P0.7) merupakan port 0 mikrokontroller yang digunakan sebagai data untuk RTC DS 12C887
3. Pin 17 (P3.7) dihubungkan dengan pin 17 (DS) dari RTC DS 12C887.
4. Pin 16 (P3.6) dihubungkan dengan pin 15 (R/$\overline{W}$) dari RTC DS 12C887.
5. Pin 30 (ALE) dihubungkan dengan pin 14 (AS) dari RTC DS 12C887.
6. Pin 21 – Pin 28 (P2.0 – P2.7) digunakan sebagai data bus LCD.
7. Pin 14 (P3.4) digunakan untuk jalur RS pada LCD.

8. Pin 15 (P3.5) digunakan untuk jalur E pada LCD.
9. Pin 9 reset aktif high yang terhubung dengan rangkaian *Power On Reset* dan jika diaktifkan akan mereset mikrokontroller AT89S52.
10. Pin 10 (P3.0) digunakan untuk menerima data dari mikrokontroller – 2 AT89S52.
11. Pin 11 (P3.1) digunakan untuk mengirimkan data ke mikrokontroller – 2 AT89S52.
12. Pin 18 berfungsi sebagai output dari rangkaian pewaktu luar (X2).
13. Pin 19 berfungsi sebagai input dari rangkaian pewaktu luar (X1).
14. Pin 20 berfungsi sebagai ground (GND).
15. Pin 31 ($\overline{EA}$) dihubungkan dengan Vcc, karena mikrokontroller mengakses program secara internal.
16. Pin 40 berfungsi sebagai Vcc +5 Volt.

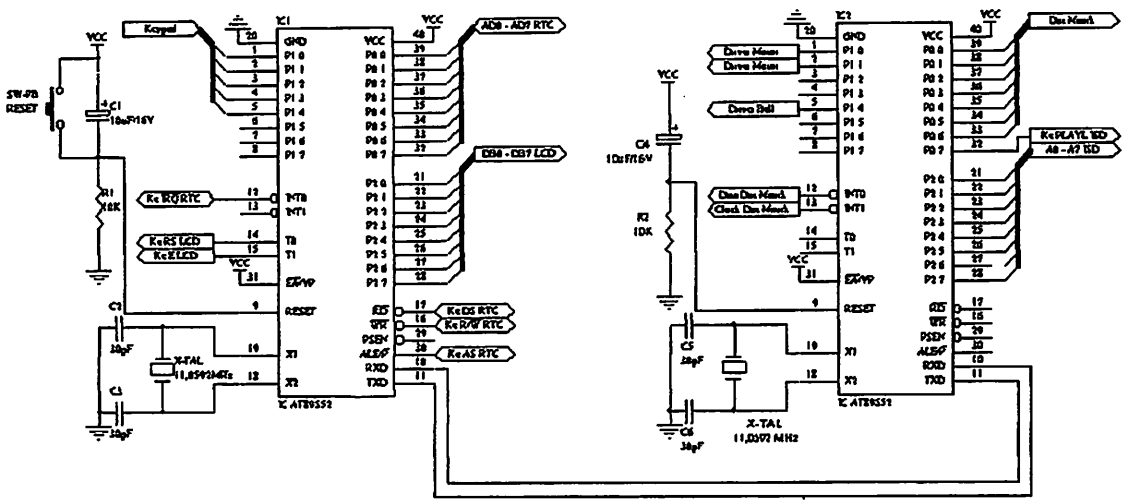


Gambar 3.4 Rangkaian Mikrokontroller – 2 AT89S52

Adapun fungsi dari masing-masing pin (kaki) dalam Mikrokontroller – 2 AT89S52 adalah sebagai berikut :

1. Pin 1 dan Pin 2 (P1.0 dan P1.1) digunakan untuk driver motor dc.
2. Pin 5 (P1.4) digunakan untuk driver bel listrik.
3. Pin 33 – Pin 39 (P0.0 – P0.6) digunakan sebagai data dot matrik.
4. Pin 12 dan Pin 13 (P3.2 dan P3.3) digunakan sebagai data dan clock dari dot matrik.
5. Pin 21 – Pin 28 (P2.0 – P2.7) digunakan sebagai alamat (A0 – A7) dari ISD 1420.
6. Pin 32 (P0.7) dihubungkan dengan PLAYL dari ISD 1420.
7. Pin 9 reset aktif high yang terhubung dengan rangkaian *Power On Reset* dan jika diaktifkan akan mereset mikrokontroller AT89S52.
8. Pin 10 (P3.0) digunakan untuk menerima data dari mikrokontroller – 1 AT89S52.
9. Pin 11 (P3.1) digunakan untuk mengirimkan data ke mikrokontroller – 1 AT89S52.
10. Pin 18 berfungsi sebagai output dari rangkaian pewaktu luar (X2).
11. Pin 19 berfungsi sebagai input dari rangkaian pewaktu luar (X1).
12. Pin 20 berfungsi sebagai ground (GND).
13. Pin 31 ($\overline{EA}$) dihubungkan dengan Vcc, karena mikrokontroller mengakses program secara internal.
14. Pin 40 berfungsi sebagai Vcc +5 Volt.

3.1.4.2. Komunikasi Serial Antar Mikrokontroller



Gambar 3.5 Rangkaian Komunikasi Serial Antar Mikrokontroller

Komunikasi serial antar mikrokontroller ditunjukkan pada gambar 3.5 di atas, dimana komunikasi serial yang digunakan adalah asinkron dengan mode 1, dimana data dikirim melalui P3.1 (TxD) dan diterima melalui P3.0 (RxD). Pada mode 1 ini data dikirim atau diterima 10 bit sekaligus, diawali dengan 1 bit start, disusul dengan 8 bit data yang dimulai dari bit yang bobotnya paling kecil (bit 0), diakhiri dengan 1 bit stop. Agar dapat mengirimkan data, maka perlu adanya inisialisasi komunikasi serial, dalam perancangan ini menentukan baud rate yang digunakan untuk kecepatan proses pengiriman data adalah 9600 dengan menggunakan rumus :

$$Baud\ Rate = \frac{FrekuensiOscilator}{32x12(256 - TH1)} \text{ x K}$$

Dimana K adalah konstanta dengan nilai : K = 1, jika SMOD = 0

K = 2, jika SMOD = 1

Dalam perancangan ini digunakan nilai SMOD = 0, jadi nilai K = 1, maka untuk menghitung nilai Timer TH1 adalah sebagai berikut :

$$TH1 = 256 - \frac{FrekuensiOscilator}{384xBaudRate} \text{ x K}$$

$$= 256 - \frac{11059200}{384x9600} \text{ x } 1$$

$$= 256 - 3$$

$$= 253$$

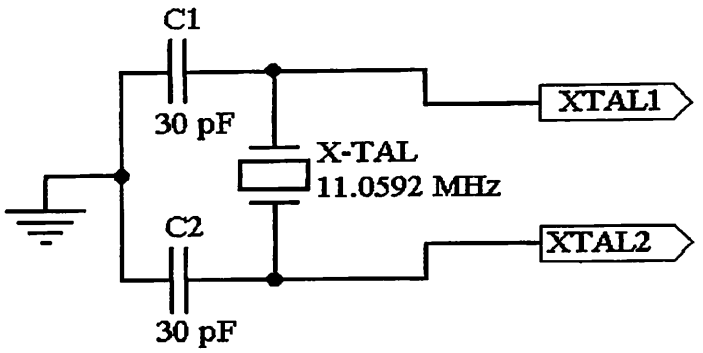
$$= FDH$$

3.1.4.3 Rangkaian Clock Minimum Sistem

Kecepatan proses pengolahan data pada mikrokontroller ditentukan oleh clock (pewaktu) yang dikendalikan oleh mikrokontroller tersebut. Pada mikrokontroller AT89S52 terdapat internal clock. Internal clock generator berfungsi sebagai sumber clock, tapi masih memerlukan rangkaian tambahan untuk membangkitkan clock yang diperlukan. Rangkaian clock ini terdiri dari dua buah kapasitor dan sebuah kristal yang dirangkai sedemikian rupa dan kemudian dihubungkan dengan Pin 18 dan 19 pada AT 89S52.

Dalam perancangan rangkaian ini menggunakan :

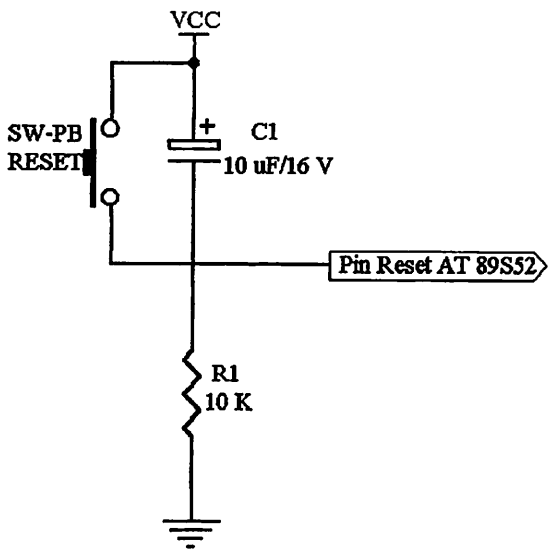
1. C = 30 pF. Penentuan besarnya kapasitansi disesuaikan dengan spesifikasi pada data sheet AT89S52.
2. Kristal 11,0592 MHZ (berdasarkan data sheet AT89S52). Adapun gambar rangkaian clock tampak seperti pada gambar 3.6.



Gambar 3.6 Rangkaian Clock Minimum Sistem

3.1.4.4. Rangkaian Reset

Reset pada Mikrokontroller merupakan masukan aktif High ' 1 '. Pulsa transisi dari rendah '0' ke tinggi '1' akan mereset Mikrokontroller menuju alamat 0000H. Pin reset dihubungkan dengan rangkaian power on reset seperti tampak pada gambar 3.7.



Gambar 3.7 Rangkaian Power On Reset

Rangkaian reset bertujuan agar mikrokontroller dapat menjalankan proses dari awal. Rangkaian reset untuk mikrokontroller dirancang agar mempunyai

kemampuan power on reset, yaitu reset yang terjadi pada saat sistem dinyalakan untuk pertama kalinya. Reset juga dapat dilakukan secara manual dengan menekan tombol reset yang berupa switch push button.

Rangkaian Reset terbentuk oleh komponen R dan C yang sudah baku (ditetapkan oleh perusahaan pembuat IC AT 89S52). Nilai R yang dipakai adalah 10 kΩ dan C =10 μF.

Sedangkan untuk mencari frekuensi dari reset tersebut dengan menggunakan rumus sebagai berikut :

$$fo = \frac{1}{1{,}1RC}$$

Sehingga dengan komponen resistor dengan nilai 10 kΩ serta kapasitor dengan nilai 10 μF akan dihasilkan frekuensi sebesar :

$$fo = \frac{1}{1{,}1x10.10^{3}x10.10^{-6}}$$

$$fo = 9{,}09Hz$$

Maka Periode Clock dapat dihitung sebagai berikut :

$$T = \frac{1}{fo}$$

$$T = \frac{1}{9{,}09}$$

$T = 0{,}11$ detik.

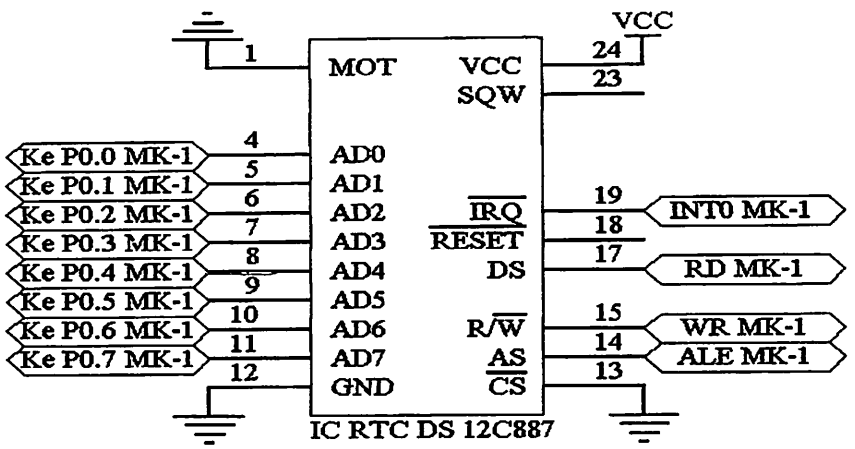
3.1.5. Perencanaan dan Pembuatan Rangkaian RTC DS 12C887

Dalam perencanaan dan pembuatan rangkaian RTC DS 12C887 ini berfungsi untuk mencocokkan/ mendeteksi dengan inputan keypad.

RTC DS 12C887 sejenis jam yang sangat kompleks, yang dapat menghitung detik, menit, jam, hari, tanggal, bulan dan tahun dengan lompatan pergantian tahun. RTC DS 12C887 ini mempunyai RAM internal sebesar 128 byte yang terdiri atas 14 byte untuk pewaktuan dan 114 byte untuk data yang bisa diprogram oleh pemakai. Hubungan penyemat untuk RTC DS 12C887 antara lain adalah sebagai berikut :

- AS (*Address Strobe*) dihubungkan dengan ALE mikrokontroller yang berfungsi untuk memisahkan saluran data dan saluran alamat yang termultipleks pada saluran AD0 – AD7.
- R/ $\overline{W}$ dihubungkan dengan WR mikrokontroller yang berfungsi sebagai kontrol untuk penulisan data pada RAM internal.
- DS (*Data Strobe*) dihubungkan dengan RD mikrokontroller yang berfungsi sebagai kontrol untuk pembacaan data pada RAM internal.
- MOT dihubungkan dengan ground untuk mendapatkan sistem pewaktuan bus intel.

Operasi pembacaan dan penulisan pada RAM internal RTC DS 12C887 ini sama dengan operasi baca tulis pada RAM. Gambar dari rangkaian RTC DS 12C887, diperlihatkan pada Gambar 3.8 di bawah ini :



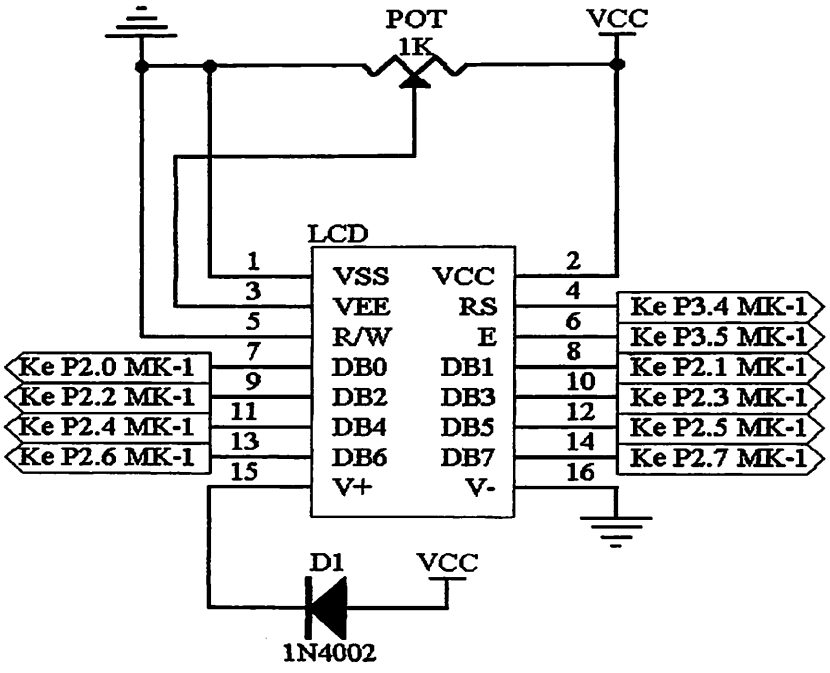
Gambar 3.8 Rangkaian RTC DS 12C887

3.1.6. Perencanaan dan Pembuatan Rangkaian LCD M 1632

Untuk tampilan dari keseluruhan waktu-waktu yang ada digunakan LCD jenis dot matriks *type* M 1632. LCD M 1632 dihubungkan dengan bus data mikrokontroller. Sinyal – sinyal yang dipergunakan oleh LCD adalah RS, R/W, dan E. Sinyal RS dihubungkan ke P3.4 dari mikrokontroller – 1, Sinyal RS diberikan ke LCD untuk membedakan sinyal antara instruksi program atau instruksi penulisan data. Sinyal E dihubungkan ke P3.5 dari mikrokontroller – 1 untuk mengaktifkan LCD, LCD akan aktif jika mikrokontroller memberikan instruksi tulis pada alamat LCD. Sedangkan pin R/W dihubungkan dengan ground, maka LCD difungsikan hanya untuk menuliskan program atau data ke display. Untuk mengambil data dari mikrokontroller maka pin – pin data dihubungkan dengan P2.0 – P2.7 yang merupakan pin – pin data dari mikrokontroller.

Dengan bantuan perangkat lunak yang dibuat, dapat ditampilkan karakter yang diinginkan pada layar tampilan, yaitu dengan mengendalikan pada pena E, R/W dan RS.

Gambar dari rangkaian LCD M 1632, diperlihatkan pada Gambar 3.9.



Gambar 3.9 Rangkaian LCD M 1632

VR1 pada pin 3 (VEE) digunakan untuk mengatur *contras* dari karakter yang ditampilkan, sedangkan pada pin 15 (V+) diberi sebuah diode gunanya adalah agar tegangan yang masuk sesuai dengan data sheet yaitu sebesar 4,5 volt maksimal.

Tegangan diode = 0,6 Volt

Vcc = 5 Volt

Jadi tegangan yang masuk = 5 – 0,6 = 4,4 Volt

3.1.7. Perencanaan dan Pembuatan Rangkaian Driver Bel Listrik

Kegunaan bel listrik disini adalah sebagai alarm, yaitu mengisyaratkan aktifitas sekolah. Bel listrik akan berbunyi jika waktu atau jam yang telah dimasukkan melalui keypad sama dengan waktu pada RTC DS 12C887. Rangkaian ini berfungsi untuk mengontrol bel listrik yang mempunyai catu daya AC 220 Volt.

Pada rangkaian driver bel listrik ini digunakan optotransistor dengan tipe 4N25 yang berfungsi sebagai osilator untuk mengisolasi IC mikrokontroller dengan rangkaian driver bel listrik, jika tegangan keluaran dari mikrokontroller sebesar 5 volt dan untuk membuat aktif optotransistor diperlukan arus forward If = 10 mA dan tegangan forward Vf = 1,5 volt, maka nilai R1 dapat dihitung sebagai berikut :

$$R1 = \frac{Vcc - Vf}{If}$$

$$= \frac{5 - 1{,}5}{10mA}$$

$$= \frac{5 - 1{,}5}{10x10^{-3}}$$

$$= 350\ \Omega$$

Karena nilai resistor 350 Ω tidak ada di pasaran maka digunakan resistor dengan nilai 330 Ω. Di dalam 4N25 terdapat transistor jenis NPN yang dapat dipicu oleh cahaya LED, transistor ini peka terhadap cahaya sehingga bisa disebut juga fototransistor. Bila LED menyala maka pada basis transistor akan terjadi loncatan elektron yang bisa menimbulkan adanya arus basis dan membuat arus kolektor (I_C) mengalir atau transistor menjadi saturasi. Untuk mengaktifkan relay diperlukan transistor NPN tipe BD139 sebagai saklar. Untuk melindungi transistor dari arus balik dipasang diode tipe 1N4001 sebagai pengamannya sehingga transistor tidak

akan rusak. Dari data sheet transistor BD139 diperoleh nilai h_{FE} = 25, V_{BE} = 0,7 Volt. Apabila V_{CC} = 12 Volt, R_{relay} = 360 Ω, maka besarnya R3 dapat dihitung sebagai berikut :

$$I_{relay} = \frac{V_{CC}}{R_{relay}}$$

$$= \frac{12}{360}$$

$$= 0{,}0333 \text{ A}$$

$$= 33{,}3 \text{ mA.}$$

$$I_B = \frac{Ic}{h_{FE}}$$

$$= \frac{33{,}3mA}{25}$$

$$= 1{,}332 \text{ mA.}$$

Maka besarnya nilai R2 dapat dihitung dengan persamaan :

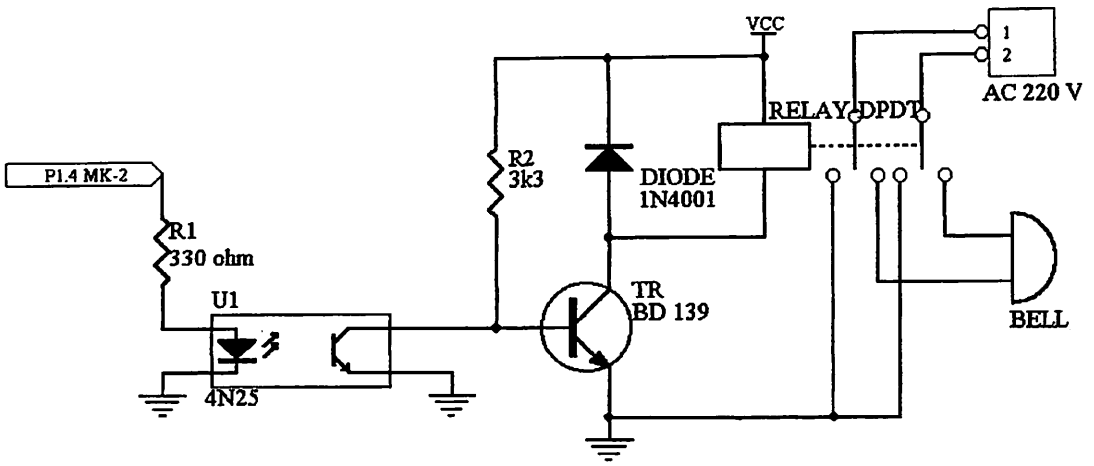
$$R2 = \frac{V_{BB} - V_{BE}}{I_B}$$

$$= \frac{5 - 0{,}7}{1{,}332mA}$$

$$= \frac{5 - 0{,}7}{1{,}332x10^{-3}}$$

$$= 3{,}23 \text{ k}\Omega$$

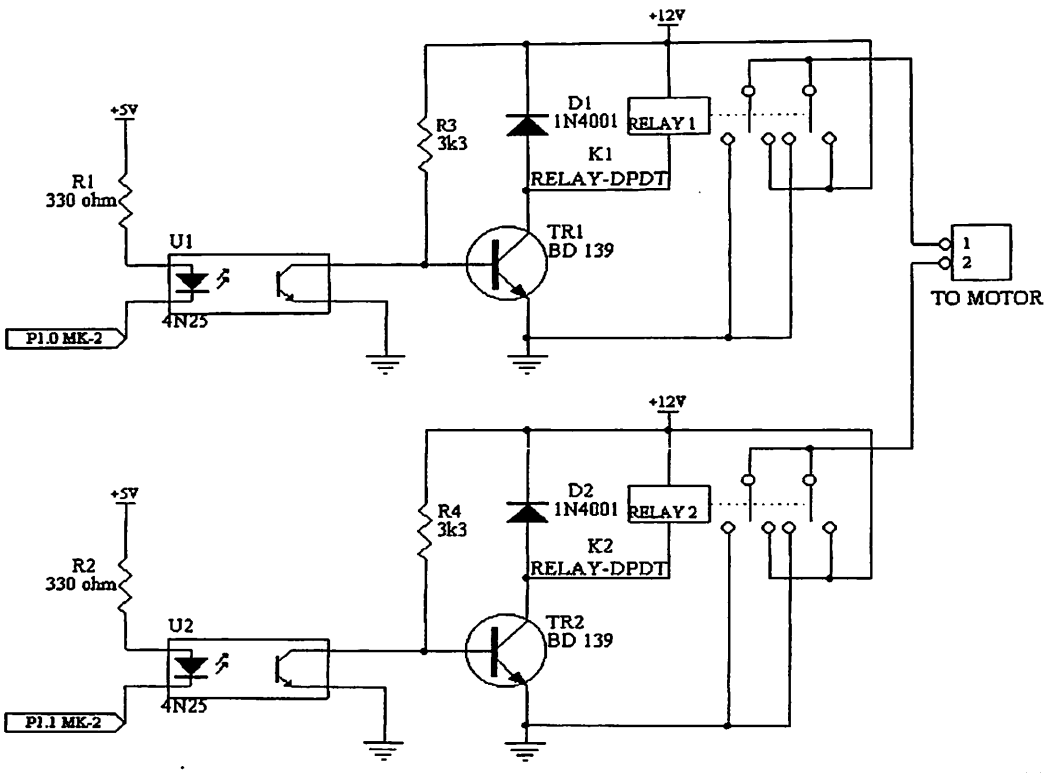
Karena nilai resistor sebesar 3,23 kΩ tidak ada di pasaran, maka digunakan resistor dengan nilai 3k3 Ω.



Gambar 3.10 Rangkaian Driver Bel Listrik

3.1.8. Perencanaan dan Pembuatan Rangkaian Driver Motor DC

Rangkaian driver motor DC pada perancangan ini digunakan sebagai pemicu atau penggerak motor DC yang nantinya digunakan untuk menggerakkan pintu gerbang. Prinsip dasar kerja dari motor DC ini adalah jika berputar ke kanan maka pintu gerbang akan tertutup dan jika berputar ke kiri maka pintu gerbang akan terbuka. Driver motor DC ini diperlukan karena tegangan dan arus output dari mikrokontroller sangat kecil sehingga tidak mampu untuk menggerakkan sebuah motor DC, maka diperlukan driver motor agar motor bisa berputar. Gambar dari rangkaian driver motor DC ditunjukkan pada Gambar 3.11.



Gambar 3.11 Rangkaian Driver Motor DC

Prinsip kerja dari rangkaian driver motor DC di atas adalah jika pada R1 diberi logika High dan R2 diberi logika Low maka motor akan berputar ke kanan dan jika pada R1 diberi logika Low dan R2 diberi logika High maka motor akan berputar ke kiri. Seperti halnya pada rangkaian driver bel listrik, rangkaian driver motor ini juga menggunakan optotransistor dengan tipe 4N25, untuk perhitungan nilai R1 atau R2 adalah sama dengan perhitungan nilai R1 pada rangkaian driver bel listrik yaitu 330 Ω.

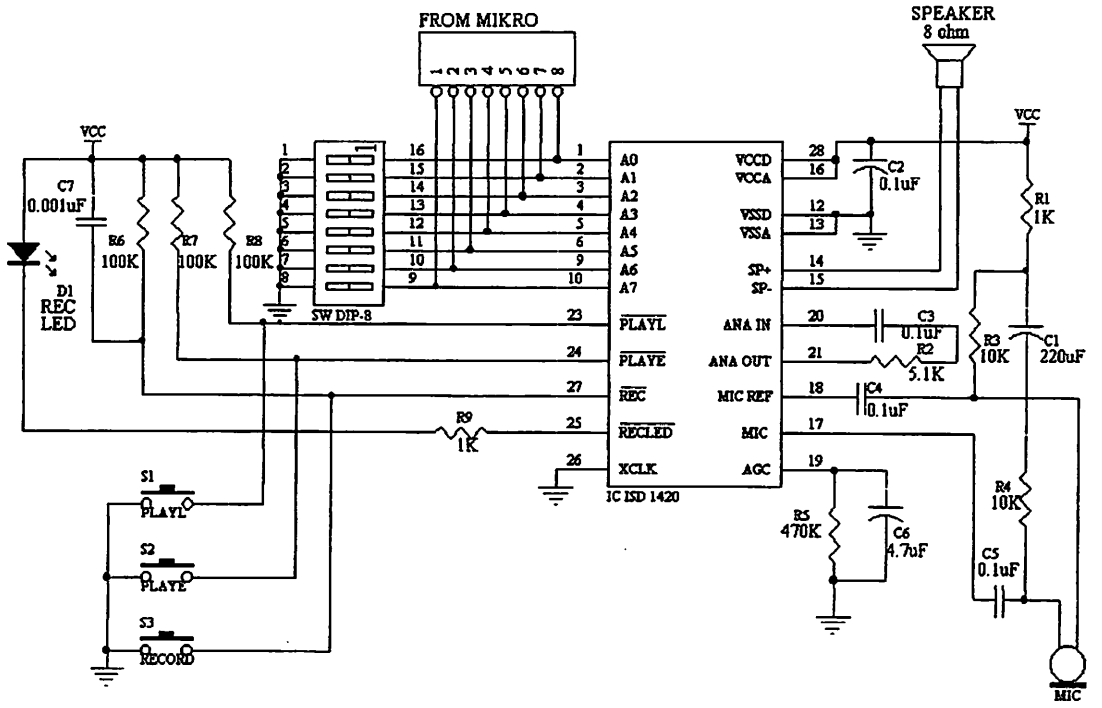
Sama halnya dengan rangkaian driver bel listrik, rangkaian driver motor dc ini juga menggunakan transistor NPN tipe BD 139 sebagai saklar, diode tipe 1N4001 sebagai pengaman dari arus balik relay sehingga transistor tidak akan rusak. Untuk

perhitungan nilai R3 dan R4 sama seperti perhitungan nilai R2 pada rangkaian driver bel listrik.

3.1.9. Perencanaan dan Pembuatan Rangkaian ISD 1420

Pada perencanaan dan pembuatan alat ini, suara yang direkam menggunakan *Voice Processor ISD 1420* yang disimpan dalam EPROM. Berdasarkan *datasheet* ISD 1420 mampu merekam suara dengan lama perekaman selama 20 detik.

Gambar dari rangkaian ISD 1420, diperlihatkan pada Gambar 3.12.

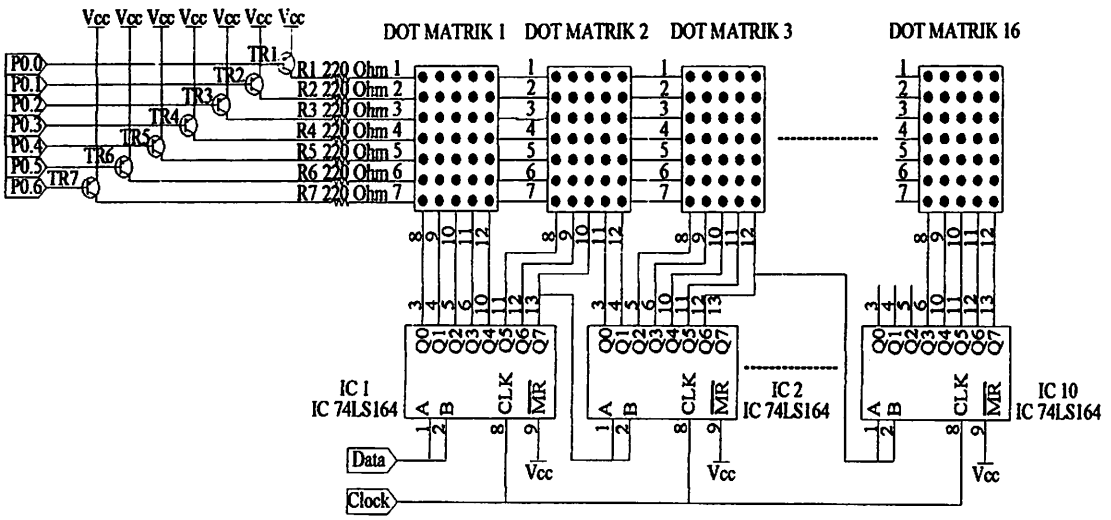


Gambar 3.12 Rangkaian ISD 1420

3.1.10. Perencanaan dan Pembuatan Rangkaian Display Dot Matrik

Display yang direncanakan adalah *dot matrik* dengan tipe *common anoda* yang mana data yang akan ditampilkan di driver oleh IC Latch 74LS164. Arus kerja dari masing – masing led dot matrik adalah sebesar 10 – 20 mA, sedangkan tegangan

kerja yang paling baik adalah antara 1,5 – 2,5 Volt. Pada led – led dot matrik perlu diberi tahanan untuk membatasi arus dan menjaga tegangan kerja seperti pada gambar 3.13 di bawah ini.



Gambar 3.13 Rangkaian Display Dot Matrik

Nilai resistansi dari tahanan – tahanan pembatas arus tersebut dapat dicari dengan menggunakan rumus :

$$R = \frac{Vcc - Vd}{Id}$$

$$= \frac{5 - 2{,}5}{10mA}$$

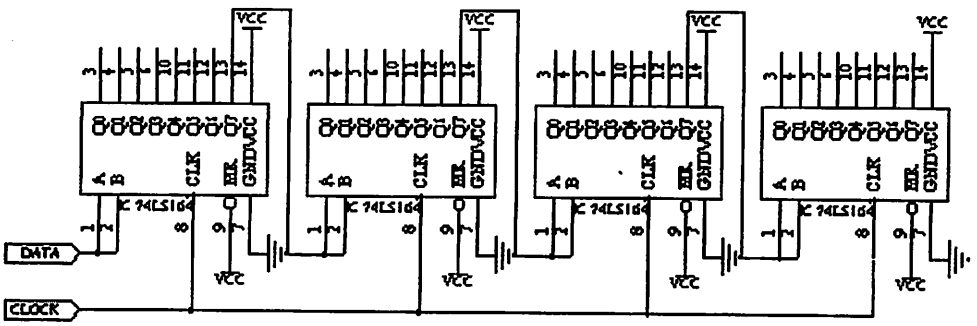
$$= \frac{2{,}5}{0{,}01}$$

$$= 250\ \Omega$$

Karena nilai tahanan sebesar 250 Ω tidak ada di pasaran, maka digunakan tahanan sebesar 220 Ω.

3.1.11. Perencanaan dan Pembuatan Rangkaian *Shift Register* (Register Geser)

Pada rangkaian *shift register* (register geser) menggunakan IC 74LS164, yang berfungsi untuk mengubah data *serial* dari rangkaian kontrol yaitu pada mikrokontroller port 3.7 untuk menjadi data *paralel* sebagai data kolom yang bergeser pada tiap bitnya seiring dengan diberikannya pulsa clock. Gambar dari rangkaian shift register (register geser) dapat dilihat pada gambar 3.14 di bawah ini.



Gambar 3.14 Rangkaian Shift Register (Register Geser)

Cara kerja dari rangkaian *shift register* (register geser) adalah sebagai berikut :

Sinyal scanning diatur oleh software dari program mikrokontroller AT89S52, bit pertama yang diterima oleh 74LS164 akan diteruskan ke pin Q0, dan pada saat bit kedua diterima maka bit tersebut juga diteruskan ke pin Q0, sedangkan data semula atau data yang pertama dari pin Q0 akan dipindahkan atau digeser ke pin Q1, demikian seterusnya. Pada saat bit ke 8 diterima maka data yang berada di pin Q7 langsung diteruskan ke 74LS164 yang berikutnya, dimana data tersebut dianggap sebagai bit pertama dan akan diteruskan ke pin Q0. Proses tersebut berlangsung secara terus – menerus sampai ke 80 data (bit) yang diinginkan sudah siap di pin Q0

sampai Q7 pada semua komponen 74LS164, setelah itu mikrokontroller AT89S52 akan mengirimkan sinyal sehingga data tersebut ditampilkan. Serta pada saat yang sama pula mikrokontroller mengirimkan *sinyal scanning* untuk baris pertama, kedua, sampai dengan baris ke tujuh. Karena kecepatan dari scanning sangat tinggi maka kita melihat seolah – olah tampilan yang ada pada *display dot matrik* tidak berkedip.

Bit – bit terus bergeser ke kanan dan data tersebut akan low (0) semua ketika pulsa clear diberikan. Pada rangkaian dot matrik ini didapatkan arus awal sebesar 23 mA yang didapat dengan rumus :

$$I = \frac{V}{R}$$

Dimana :

I = Arus dot matrik

V = Tegangan sumber / Vcc

R = Tahanan/ hambatan

Bila diketahui :

V = 5 Volt

R = 220 Ω

maka : $I = \frac{5}{220}$

I = 0,023 A

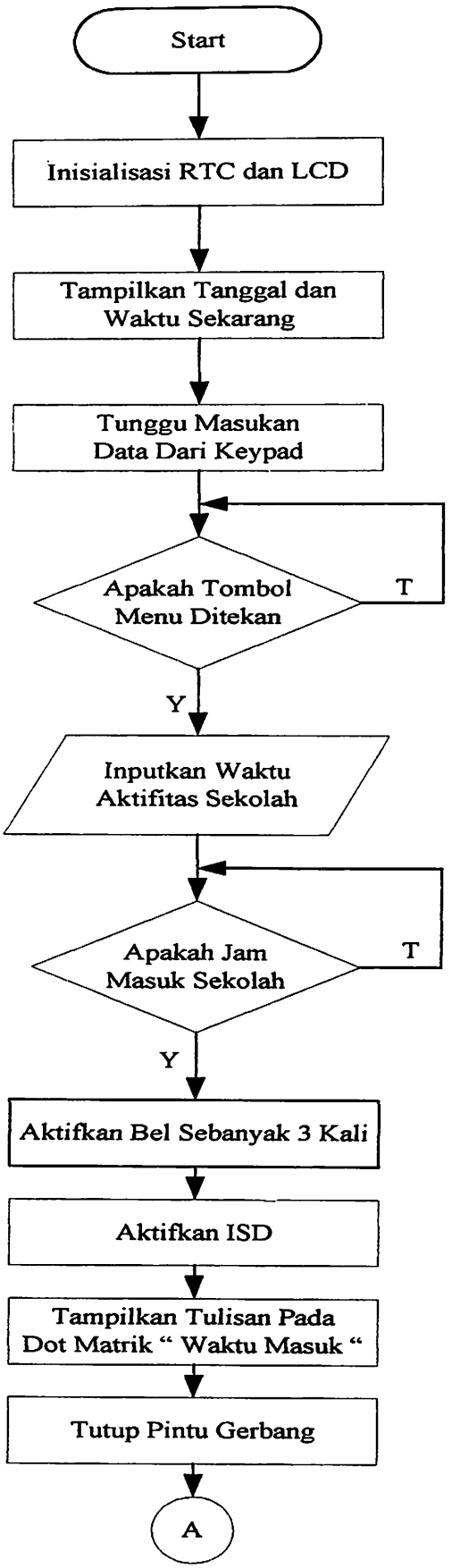
I = 23 mA

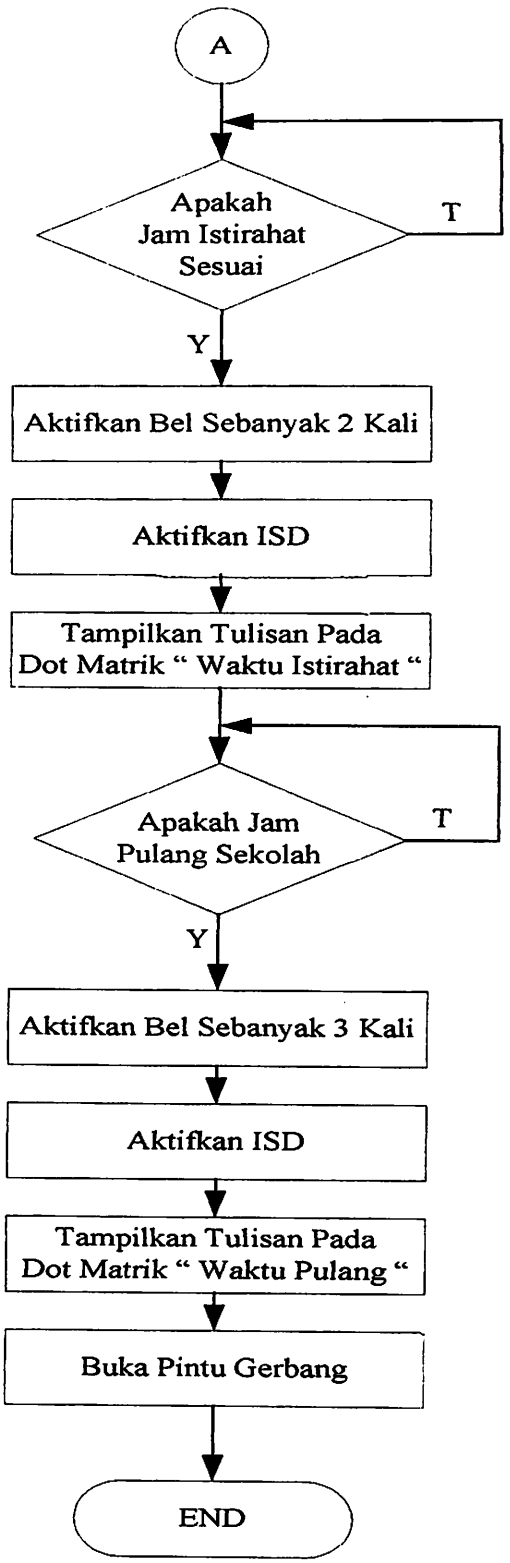
3.2. Perencanaan Perangkat Lunak (*Software*)

Untuk mendukung agar perangkat keras berfungsi sesuai dengan perencanaan, maka diperlukan perangkat lunak sebagai penunjangnya. Untuk mengatur dan mengendalikan keseluruhan sistem perangkat keras yang telah dibuat, harus dibantu dengan perangkat lunak. Perangkat lunak disini adalah susunan perintah – perintah (program) di dalam memori yang harus dilaksanakan oleh mikrokontroller. Sistem aplikasi mikrokontroller AT89S52 ini dapat mengatur dan mengendalikan keseluruhan sistem apabila ada urutan instruksi yang mendefinisikan secara jelas urutan tugas yang harus dikerjakannya.

Urutan instruksi ini sangat penting untuk didefinisikan, karena mikrokontroller bekerja secara pasti berdasarkan urutan instruksi ini. Susunan logika perancangan yang salah tidak dapat diketahui oleh mikrokontroller. Selama instruksi yang diterima sesuai dengan aturannya, mikrokontroller tetap mengerjakan instruksi tersebut. Kesalahan seperti ini baru diketahui ketika kerja sistem aplikasi tidak sesuai dengan spesifikasi awal. Oleh karena itu, perancangan perangkat keras sangat menentukan dalam keberhasilan pembuatan perangkat lunak, sama pentingnya dengan perancangan perangkat keras. Sebuah mikrokontroller tidak akan bekerja bila tidak diberikan program. Program tersebut memberitahukan apa yang harus dilakukan oleh mikrokontroller.

Perangkat lunak (*software*) dari perangkat keras (*hardware*) yang telah dibuat terdapat di bagian lampiran dan diagram alir (*flowchart*) dari perangkat keras tersebut adalah sebagai berikut :


Start
Inisialisasi RTC dan LCD
Tampilkan Tanggal dan Waktu Sekarang
Tunggu Masukan Data Dari Keypad
Apakah Tombol Menu Ditekan
T
Y
Inputkan Waktu Aktifitas Sekolah
Apakah Jam Masuk Sekolah
T
Y
Aktifkan Bel Sebanyak 3 Kali
Aktifkan ISD
Tampilkan Tulisan Pada Dot Matrik " Waktu Masuk "
Tutup Pintu Gerbang
A



Gambar 3.15 Diagram Alir (*Flowchart*) dari Perencanaan *Software*

BAB IV

PENGUJIAN ALAT

4.1. Umum

Setelah dilakukan perancangan diperlukan pengujian untuk mengetahui apakah peralatan yang telah dirancang bekerja sesuai dengan yang diharapkan.

Di dalam bab ini akan dilakukan pengujian yaitu mengamati masukan dan keluaran masing – masing blok serta untuk mengetahui kerja dari masing – masing sistem yang dibuat per blok, dan menguji rangkaian secara keseluruhan serta menganalisa apakah bentuk dan besarnya nilai masukan serta keluaran tersebut sudah sesuai dengan yang diharapkan, jika terjadi penyimpangan apa yang menyebabkan penyimpangan itu terjadi.

Secara umum tujuan dari pengujian alat ini adalah sebagai berikut :

1. Mengetahui proses kerja dari masing – masing rangkaian per blok.
2. Memudahkan pendataan spesifikasi alat.
3. Memudahkan perawatan dan perbaikan apabila sewaktu – waktu terjadi kerusakan.

Pengujian dilakukan secara berulang – ulang untuk mendapatkan hasil pengukuran yang tepat. Prosentase kesalahan antara hasil pengukuran dan perhitungan dapat dicari dengan rumus sebagai berikut :

$$\% \text{ kesalahan} = \left[\frac{Perhitungan - Pengukuran}{Perhitungan} \right] \text{x } 100\ \%$$

4.2. Pengujian Rangkaian Keypad

4.2.1. Tujuan Pengujian

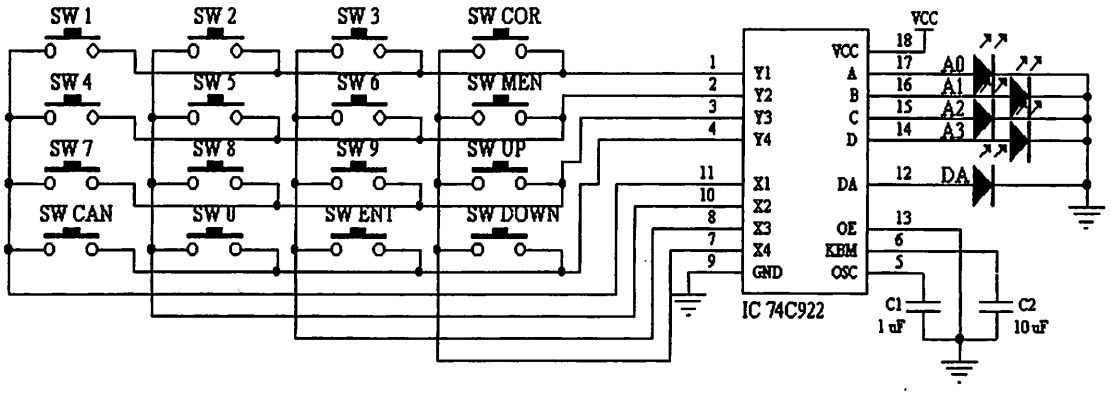
Untuk mengetahui apakah rangkaian keypad yang telah dibuat dapat bekerja sesuai dengan yang direncanakan.

4.2.2. Alat dan Bahan

1. Rangkaian keypad yang diuji
2. Catu daya 5 volt dc
3. LED peraga output keypad

4.2.3. Pelaksanaan Pengujian

1. Merangkai rangkaian keypad seperti pada gambar 4.1.
2. Menghubungkan rangkaian keypad ke catu daya.
3. Menghubungkan output rangkaian keypad dengan LED peraga.



Gambar 4.1. Rangkaian Pengujian Keypad 4x4 dengan IC 74C922

4.2.4. Analisa Hasil Pengujian

Encoder keypad untuk mendeteksi penekanan tombol keypad dan menterjemahkan ke dalam kode – kode biner 4 bit. Dalam perencanaan dan pembuatan alat ini menggunakan keypad 4 x 4 dan IC 74C922, dimana IC ini

berfungsi untuk mengeluarkan data dalam bentuk bilangan biner 4 bit, sehingga data – data yang dikeluarkan oleh keypad dapat diterjemahkan oleh mikrokontroller. Adapun kombinasi output dari keypad dengan IC 74C922 yang diperoleh dari hasil pengujian adalah sebagai berikut :

Tabel 4.1 Hasil Pengujian Keypad 4x4 dengan IC 74C922

Switch Ditekan	D	C	B	A	HEX
1	0	0	0	0	0
2	0	0	0	1	1
3	0	0	1	0	2
COR	0	0	1	1	3
4	0	1	0	0	4
5	0	1	0	1	5
6	0	1	1	0	6
MEN	0	1	1	1	7
7	1	0	0	0	8
8	1	0	0	1	9
9	1	0	1	0	A
UP	1	0	1	1	B
CAN	1	1	0	0	C
0	1	1	0	1	D
ENT	1	1	1	0	E
DOWN	1	1	1	1	F

4.3. Pengujian LCD

4.3.1. Tujuan Pengujian

Untuk mengetahui apakah rangkaian LCD yang telah dibuat dapat bekerja sesuai dengan yang direncanakan.

4.3.2. Alat dan Bahan

1. Rangkaian LCD
2. Rangkaian Mikrokontroller AT89S52
3. Catu daya 5 volt dc
4. Membuat program untuk inisialisasi LCD
5. Memprogram IC mikrokontroller kemudian menjalankannya

4.3.3. Langkah – Langkah Pengujian

1. Mengisi IC mikrokontroller dengan software, dengan program yang dapat ditampilkan pada layar LCD berupa tulisan – tulisan.
2. Bila pada layar LCD tampak tulisan berupa angka dan huruf, maka LCD tersebut siap untuk digunakan.

Adapun cara pengujian dapat dilihat pada blok pengujian LCD M 1632 di bawah ini.

Gambar 4.2 Blok Diagram Pengujian LCD

4.3.4. Analisa Hasil Pengujian

Untuk bisa sebuah mikrokontroller mengirim data ke LCD, terlebih dahulu mikrokontroller diprogram software inisialisasi sebuah LCD. Adapun potongan program inisialisasi LCD dapat dilihat di bawah ini :

```
void menu_utama(void){
uchar buf_select;
uchar buf_list;
if (data_key == menu){
        list=1;
        select=1;
        lcd_gotoxy(0,0);
        lcd_puts("SET JAM MASUK          ");
        lcd_gotoxy(0,1);
        lcd_puts("SET JAM ISTIRHT ");
        cek_select(select);
        while(data_key != cancel){
                if (list==1){
                        while(data_key != cancel){
                                lcd_gotoxy(0,0);
                                lcd_puts("SET JAM MASUK  ");
                                lcd_gotoxy(0,1);
                                lcd_puts("SET JAM ISTIRHT ");
                                cek_select(select);
                                get_noC();
                                data_key=getC();
                                if(up_down_atas(5))break;
                                if(data_key==enter){
                                        buf_select=select;
                                        buf_list=list;
                                        data_key=0;
                                    lcd_gotoxy(0,1);
                                    lcd_puts("  00:00:00    ");
                                      lcd_gotoxy(0,0);
                                      if(select==1){
                                         lcd_puts("SET JAM MASUK  ");
                                         load_jam_setting(jam_masuk);
                                         menu_edit_jam();
                                         save_jam_setting(jam_masuk);
                                      }
                                      else{
                                         lcd_puts("SET JAM ISTIRHT ");
                                         load_jam_setting(jam_istirahat);
                                         menu_edit_jam();
```

4.4. Pengujian Driver Motor Dc

4.4.1. Tujuan Pengujian

Tujuan dari pengujian driver motor DC ini adalah untuk mengetahui apakah driver motor yang dirancang dapat bekerja dengan baik. Pengujian rangkaian driver motor dilakukan dengan mengukur arus pada kaki kolektor dan kaki basis transistor BD 139.

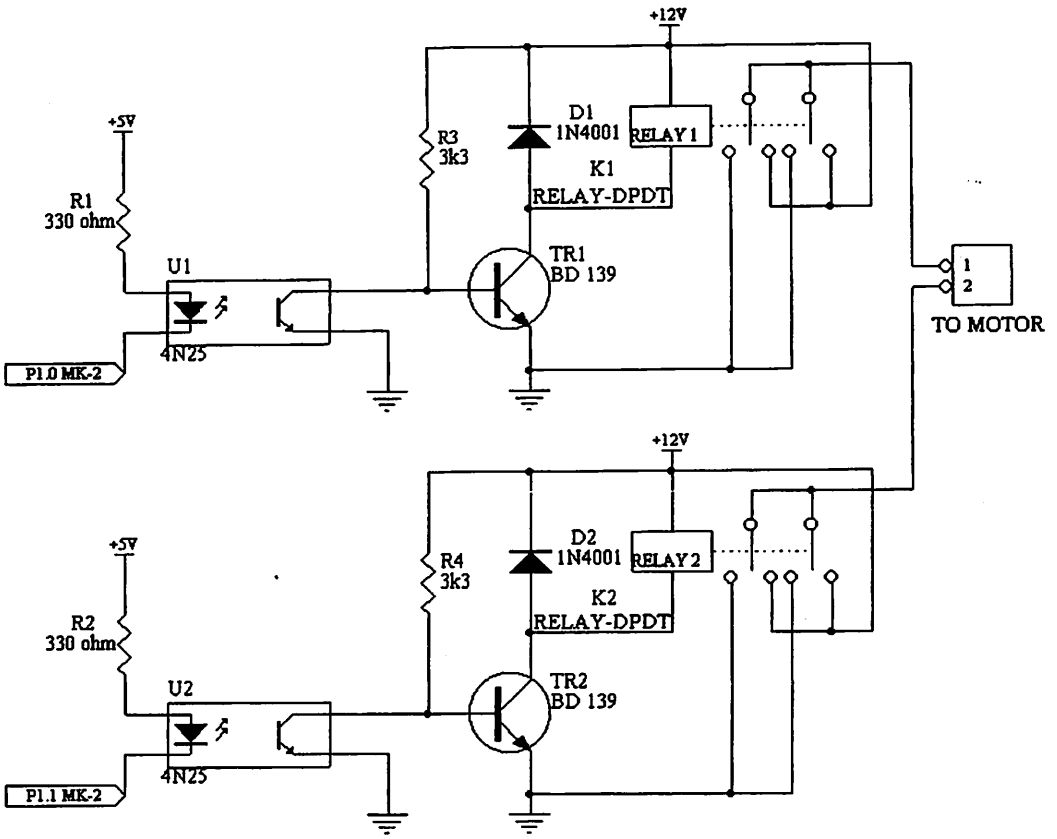
4.4.2. Alat dan Bahan

1. Dua Avometer digital merk DT830B
2. Power Supply dengan catu daya 5 Volt dan 12 Volt.

4.4.3. Langkah – Langkah Pengujian

1. Menyusun rangkaian seperti pada gambar 4.3
2. Menghubungkan rangkaian driver motor dengan catu daya 5 Volt dan 12 Volt.
3. Memasukkan hasil pengukuran pada tabel 4.2 dan 4.3.

Rangkaian driver motor DC berfungsi sebagai penggerak motor DC, jika pada R1 diberi logika HIGH (1) dan R2 diberi logika LOW (0) maka motor akan berputar ke kanan, dan sebaliknya apabila pada R1 diberi logika LOW (0) dan R2 diberi logika HIGH (1) maka motor akan berputar ke kiri. Optotransistor tipe 4N25 berfungsi sebagai isolator untuk mengisolasi IC mikrokontroller dengan rangkaian driver motor. Agar transistor saturasi maka perlu adanya masukan berlogika HIGH (1) sehingga relay akan aktif dan motor akan berputar.



Gambar 4.3 Rangkaian Driver Motor DC

Tabel 4.2 Pengukuran Arus Pada Optotransistor 4N25

Hasil Pengukuran	Hasil Perhitungan	% Kesalahan
I_f = 10,68 mA	I_f = 10 mA	6,8

Tabel 4.3 Pengukuran Arus Pada Transistor BD 139

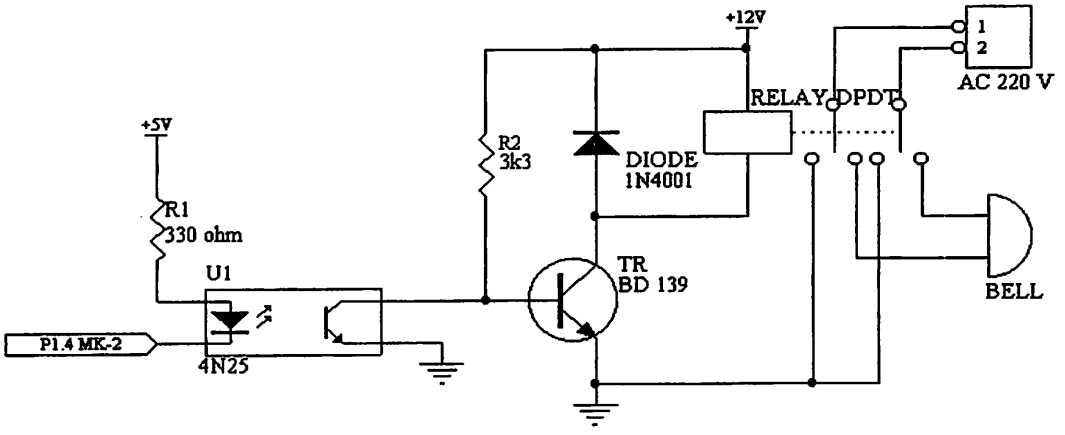
Hasil Pengukuran	Hasil Perhitungan	% Kesalahan
Ic = 31,24 mA	Ic = 33,3 mA	6,2
I_B = 1,21 mA	I_B = 1,332 mA	9,2

4.4.4. Analisa Hasil Pengujian

Dari hasil pengujian driver motor didapatkan hasil pengujian pada rangkaian driver motor yaitu pada transistor yang digunakan.

4.5. Pengujian Driver Bel Listrik

Untuk pengujian driver bel listrik ini sama dengan pengujian yang dilakukan pada rangkaian driver motor dc yaitu mengukur arus pada optotransistor 4N25 dan arus pada transistor BD139. Gambar dari rangkaian driver bel listrik dapat dilihat pada gambar 4.4.



Gambar 4.4 Rangkaian Driver Bel Listrik

4.6. Pengujian RTC DS 12C887

4.6.1. Tujuan Pengujian

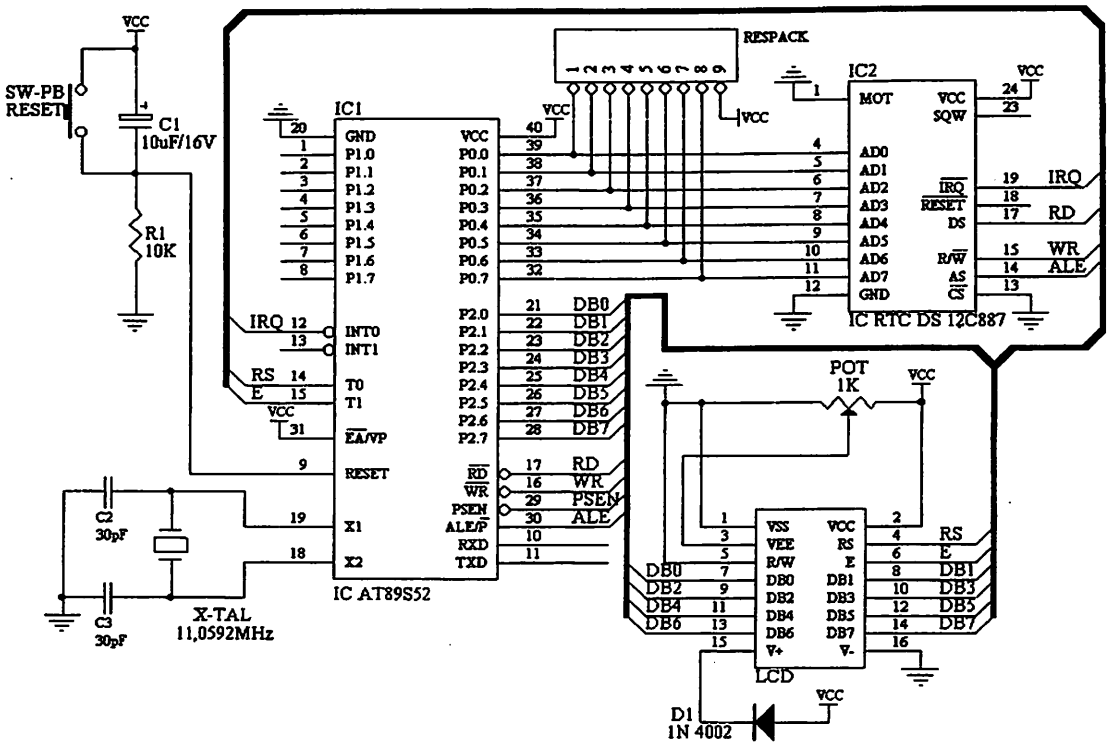
Tujuan Pengujian dari rangkaian RTC DS 12C887 adalah untuk mengetahui apakah rangkaian ini dapat bekerja menjadi basis pewaktuan. Perangkat lunak yang digunakan untuk menguji kerja rangkaian RTC adalah sebuah program simulasi jam digital dengan memanfaatkan modul penampil LCD.

4.6.2. Peralatan yang Digunakan

1. RTC Dallas 12C887
2. Mikrokontroller AT89S52
3. LCD 16x2
4. Power Supply Sistem

4.6.3. Pelaksanaan Pengujian

1. Merangkai rangkaian RTC seperti pada gambar 4.5.
2. Membuat perangkat lunak pengujian rangkaian pewaktu Real Time Clock (RTC). Program ini berisi inisialisasi mikrokontroller Real Time Clock (RTC) dan penampil kristal cair (LCD). Program kemudian mengirimkan data karakter berupa jam, menit dan detik ke rangkaian penampil kristal cair (LCD).
3. Mengaktifkan catu daya.
4. Mengoperasikan program. Hasil keluaran akan ditunjukkan pada layar penampil kristal cair (LCD).



Gambar 4.5 Rangkaian Pengujian Pewaktu RTC DS 12C887

4.6.4. Analisa Hasil Pengujian

Dari pengujian diperoleh hasil bahwa pada modul penampil kristal cair terlihat informasi waktu berupa jam, menit, detik dengan tampilan detik yang berubah setiap detik. Dengan demikian rangkaian Real Time Clock (RTC) dapat berfungsi dan dapat diakses oleh perangkat lunak. Adapun potongan software untuk inisialisasi RTC adalah sebagai berikut :

```
        void clear_buf_serial(void){
        i_rd=0;
        i_wr=0;
        buf_per=0;
        }
        uchar cekC_serial (void){
        uchar data=0;
        if(i_wr != i_rd)data=1;
return  data;
}
```

```
void tx_hex_serial(uchar data){
        n = data/16;
        if(n<=9)txC_serial(n|0x30);
        else txC_serial(n-10+0x41);
        n = data % 16;
        if(n<=9)txC_serial(n|0x30);
        else txC_serial(n-10+0x41);
}
```

4.7. Pengujian IC Penyimpan Suara (ISD 1420)

4.7.1. Tujuan Pengujian

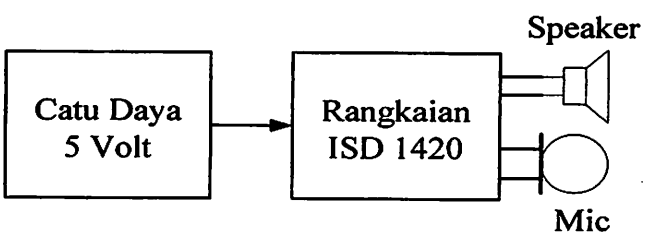
Pengujian ini bertujuan untuk mengetahui bekerja tidaknya rangkaian ISD.

4.7.2. Peralatan yang Digunakan

1. Rangkaian ISD 1420
2. Catu Daya 5 Volt Dc
3. Speaker
4. Microphone kondensor

4.7.3. Pelaksanaan Pengujian

Prosedur pengujian keluaran ISD ditunjukkan pada gambar blok diagram di bawah ini :



Gambar 4.6 Blok Diagram Pengujian ISD 1420

Langkah – langkah pengujian adalah sebagai berikut :

1. Rangkaian ISD diberi input tegangan 5 Volt DC.
2. Pada pin 27 (REC) diberi logika rendah fungsinya untuk melakukan perekaman suara, setelah proses perekaman suara selesai, pin yang dibuat berlogika rendah (pin 27) dikembalikan lagi pada posisi HIGH (berlogika '1').
3. Untuk memutar ulang suara yang direkam maka posisi pin 23 (PLAYL) diberi logika rendah sedangkan untuk pin 27 (REC) tetap posisinya pada logika HIGH.

4.7.4. Analisa Hasil Pengujian

Dalam perencanaan dan pembuatan rangkaian ISD membutuhkan tegangan 5 Volt DC dan mendapat input kontrol dari mikrokontroller. Dari hasil pengujian didapat data bahwa rangkaian ISD 1420 dapat merekam suara dan dapat pula memutar ulang suara tersebut.

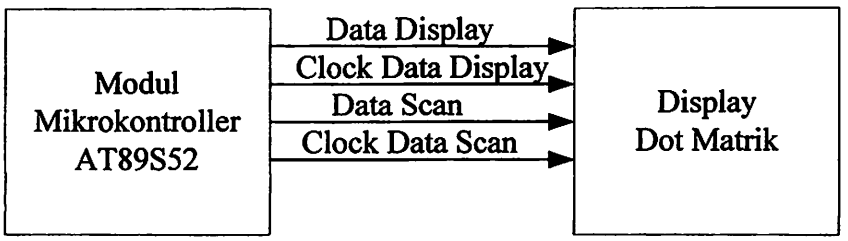
4.8. Pengujian Rangkaian Display Dot Matrik

Pengujian display dot matrik dilakukan untuk mengetahui nilai arus yang masuk dan keluar dari dot matrik serta membandingkan dengan hasil perhitungan. Untuk nilai arus keluaran dot matrik selalu berubah -- ubah berdasarkan input. Sedangkan untuk nilai arus inputan dot matrik dapat dilihat pada tabel 4.4.

Tabel 4.4 Hasil Pengukuran dan Perhitungan Arus Inputan Dot Matrik

Hasil Pengukuran	Hasil Perhitungan	% Kesalahan
20,27 mA	23 mA	11,9

Diketahui Vcc = 5 Volt, R = 220 Ω



Gambar 4.7 Blok Diagram Pengujian Display Dot Matrik

Tabel 4.5 Hasil Pengujian Dot Matrik

Clock	Data Scan	Data Baris	LED1	LED2	LED3	LED4	LED5	LED6	LED7
↑	0	0	1	0	0	0	0	0	0
↑	0	0	1	1	0	0	0	0	0
↑	0	0	1	1	1	0	0	0	0
↑	0	0	1	1	1	1	0	0	0
↑	0	0	1	1	1	1	1	0	0
↑	0	0	1	1	1	1	1	1	0
↑	0	0	1	1	1	1	1	1	1
↑	1	1	0	1	1	1	1	1	1
↑	1	1	0	0	1	1	1	1	1

↑	1	1	0	0	0	1	1	1	1
↑	1	1	0	0	0	0	1	1	1
↑	1	1	0	0	0	0	0	1	1
↑	1	1	0	0	0	0	0	0	1
↑	1	1	0	0	0	0	0	0	0

Tabel 4.5 menunjukkan hasil pengujian dot matrik. Pada tabel hasil pengujian diberikan data sebanyak 14 bit terbukti bahwa pada 7 bit pertama led dot matrik terus – menerus menyala. Selanjutnya pada 7 bit terakhir led dot matrik terus – menerus mati satu – persatu mengikuti detak clock yang diberikan. Pada percobaan display dot matrik ini hanya ingin menguji apakah seluruh led dot matrik dapat bekerja dengan baik atau tidak. Karena display ini disambungkan atau discan melalui register geser (*shift register*), jika diberikan logika 0 (switching transistor aktif low) pada data baris dan logika 0 pada data scan dengan clock terus – menerus diberikan, maka display akan menyala satu – persatu bergeser ke kiri. Sebaliknya pada saat data scan diberikan logika 1 sedang data baris berlogika 1 maka led dot matrik akan mati satu – persatu.

BAB V

PENUTUP

5.1. Kesimpulan

Dari Perencanaan dan Pembuatan bel sekolah yang bisa bersuara secara otomatis, maka dapat ditarik beberapa kesimpulan antara lain :

1. Digunakannya RTC DS12C887 dalam alat ini karena mempunyai beberapa kelebihan diantaranya adalah RTC DS12C887 dapat menghitung detik, menit, jam, hari, tanggal, bulan, dan tahun serta dapat menyimpan data yang digunakan untuk keperluan lain, misalnya data jadwal aktifitas sekolah.
2. Bel listrik akan aktif pada saat masukan berlogika "1" (high) karena terdapat tegangan masukan sebesar 4,98 volt, sedangkan bel listrik tidak akan aktif pada saat masukan berlogika "0" (low).
3. Pada rangkaian driver motor DC jika pada R1 diberi logika high dan R2 diberi logika low maka motor akan berputar ke kanan, sedangkan jika pada R1 diberi logika low dan R2 diberi logika high maka motor akan berputar ke kiri. Driver motor DC ini berfungsi untuk menutup atau membuka pintu gerbang sebagai tanda dimulai atau selesainya aktifitas sekolah.
4. Seluruh sistem apabila telah dirangkai akan menjadi sebuah alat pengendali bel sekolah sehingga dapat mempermudah tugas seorang operator bel sekolah.

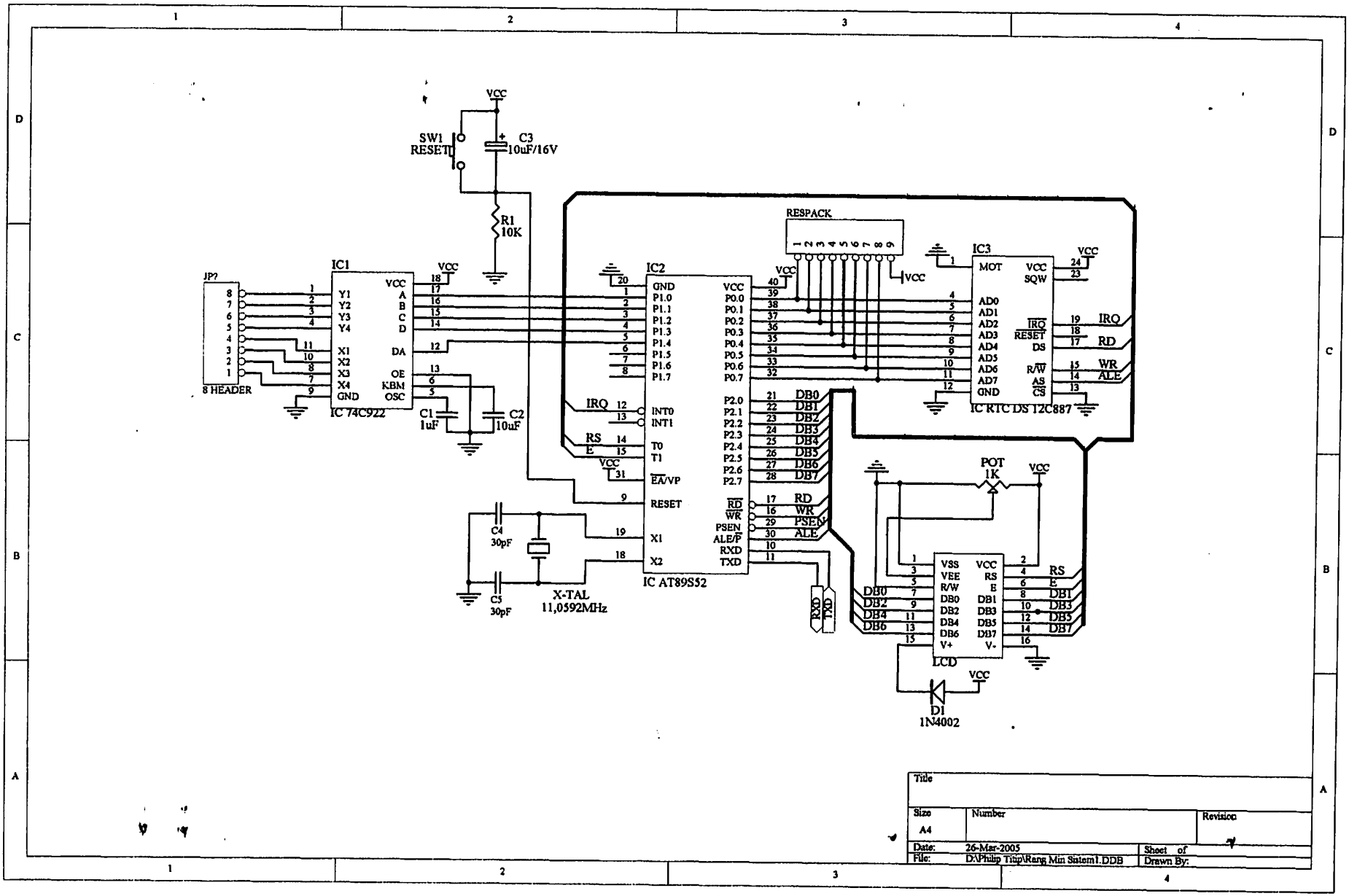
5.2. Saran – Saran

1. Bel sekolah secara otomatis sebaiknya dikembangkan lebih lanjut dengan menggunakan teknologi terbaru, misalnya Fuzzy Logic atau VHDL.
2. Direalisasikan bel sekolah secara otomatis tersebut diharapkan dapat meningkatkan disiplin waktu untuk para siswa di sekolah.
3. Driver motor yang digunakan untuk menggerakkan pintu gerbang ini hanya berupa simulasi/ prototype, apabila diterapkan dalam kondisi yang sebenarnya driver motor harus disesuaikan.
4. Apabila menginginkan tampilan yang lebih besar, maka dot matrik 7x5 yang berukuran kecil dapat diganti dengan ukuran yang lebih besar.
5. Apabila menginginkan suara yang lebih besar, maka bisa ditambahkan rangkaian penguat pada ISD 1420.

DAFTAR PUSTAKA

1. Malvino, **PRINSIP – PRINSIP ELEKTRONIKA,** Edisi Kedua, Penerbit Erlangga, Jakarta, 1999
2. **Belajar Mikrokontroler AT89C51/ 52/ 55,** Penerbit Gava Media
3. **Belajar Mikroprosesor – Mikrokontroler,** Penerbit PT. Elex Media Komputindo, Jakarta
4. **Bereksperimen Dengan Mikrokontroler 8031,** Penerbit PT. Elex Media Komputindo, Jakarta
5. Wasito S., **VADEMEKUM ELEKTRONIKA,** Edisi Kedua, Penerbit PT Gramedia Pustaka Utama, Jakarta, 1995

LAMPIRAN


VCC
SW1
RESET
C3
10uF/16V
R1
10K
RESPACK
JP?
8 HEADER
IC1
IC 74C922
C1
1uF
C2
10uF
IC2
IC AT89S52
C4
30pF
C5
30pF
X-TAL
11,0592MHz
IC3
IC RTC DS 12C887
POT
1K
LCD
D1
1N4002
IRQ
RD
WR
ALE
RS
DB0
DB1
DB2
DB3
DB4
DB5
DB6
DB7
RXD
TXD
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26-Mar-2005
Sheet of
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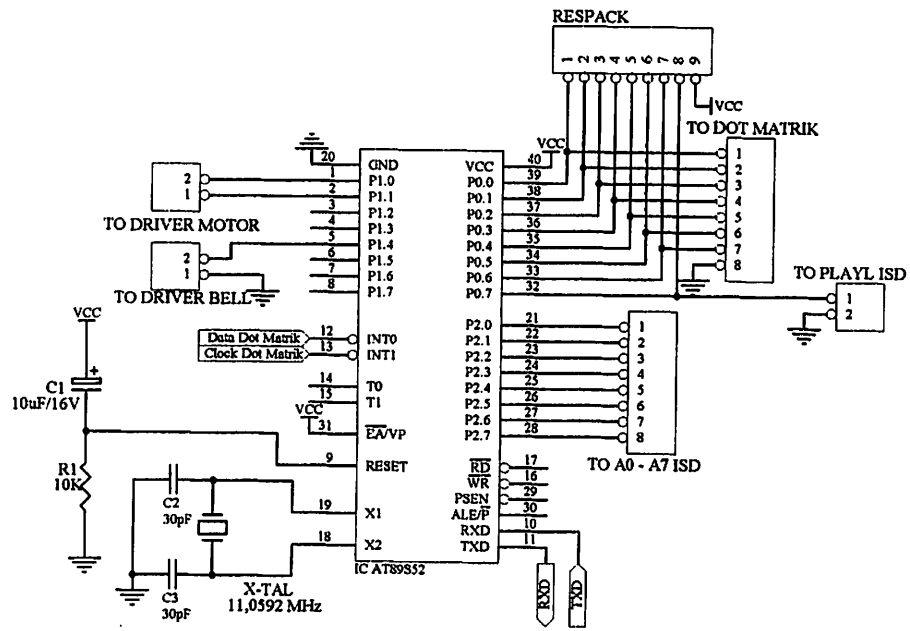
Drawn By:



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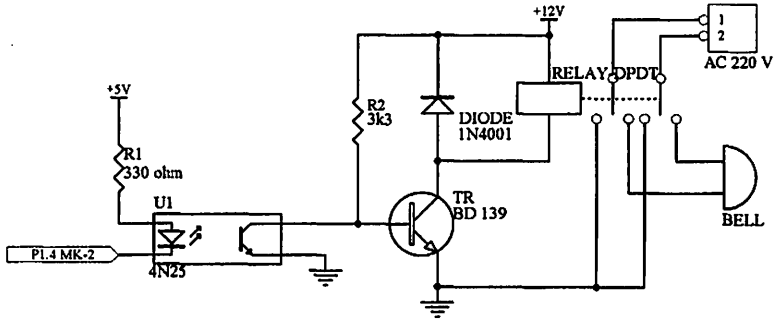

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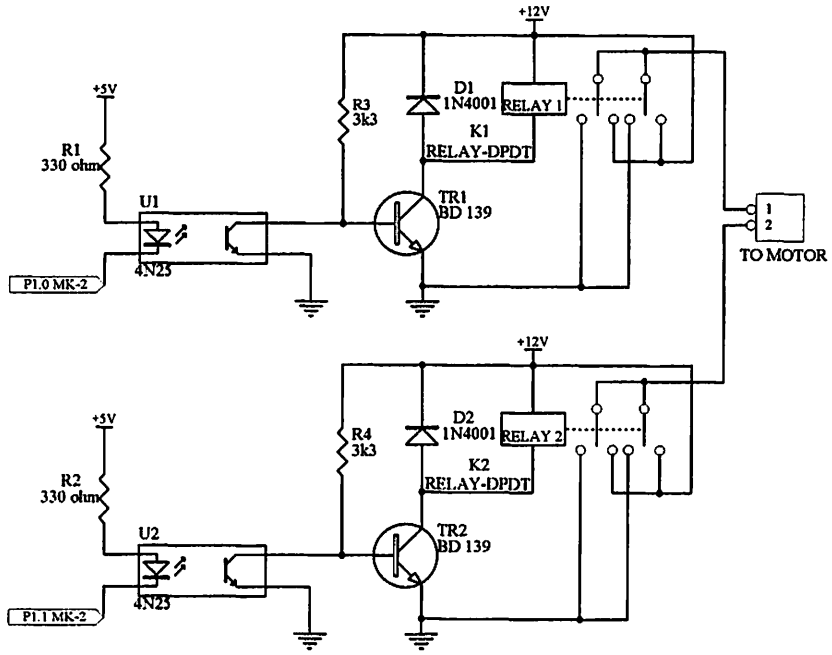
Size: A4	Number		Revision
Date: 26-Mar-2005		Sheet of	
File: D:\Philip Titip\Rang Driver Bel Listrik.DDB		Drawn By:	



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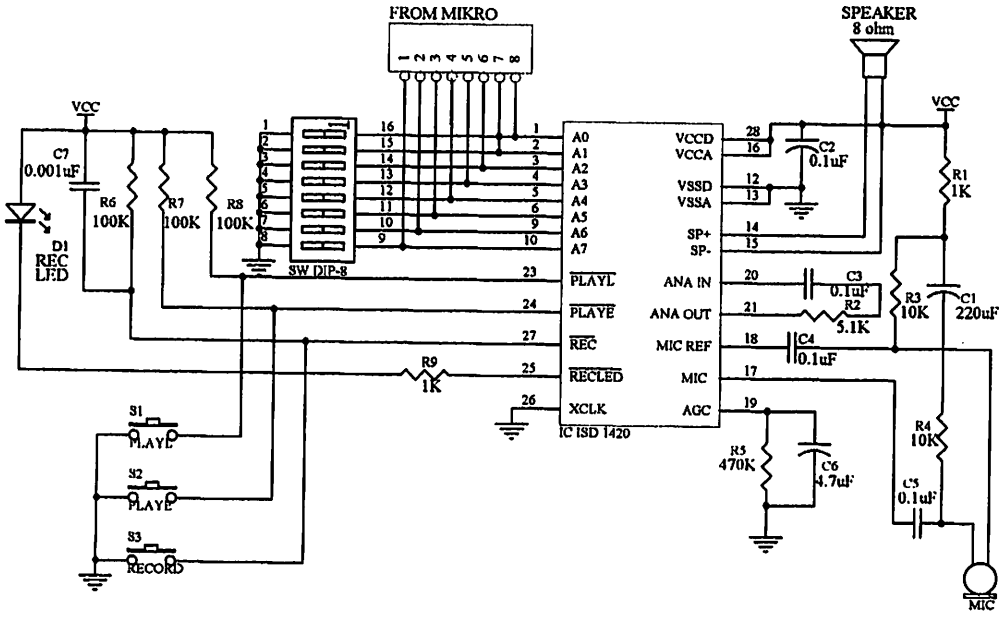
Date:	26-Mar-2005	Sheet of	
File:	D:\Philip Titip\Rang Driver Motor Dc.DDB	Drawn By:	



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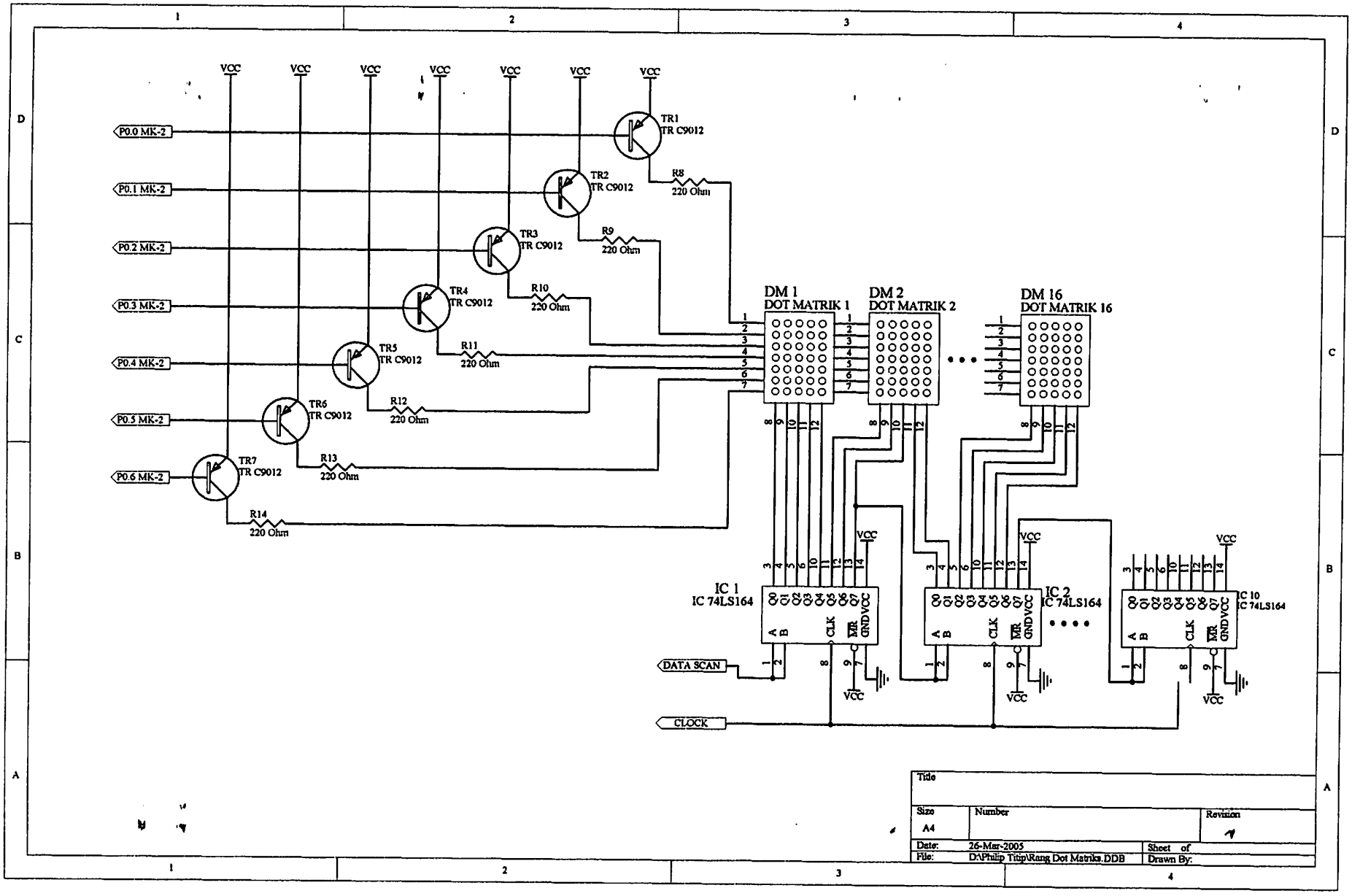
Date: 26-Mar-2005		Sheet of	
File: D:\Philip Titip\ISD 14201.DDB		Drawn By:	


VCC
P0.0 MK-2
P0.1 MK-2
P0.2 MK-2
P0.3 MK-2
P0.4 MK-2
P0.5 MK-2
P0.6 MK-2
TR1 TR C9012
TR2 TR C9012
TR3 TR C9012
TR4 TR C9012
TR5 TR C9012
TR6 TR C9012
TR7 TR C9012
R8 220 Ohm
R9 220 Ohm
R10 220 Ohm
R11 220 Ohm
R12 220 Ohm
R13 220 Ohm
R14 220 Ohm
DM 1 DOT MATRIK 1
DM 2 DOT MATRIK 2
DM 16 DOT MATRIK 16
IC 1 IC 74LS164
IC 2 IC 74LS164
IC 10 IC 74LS164
DATA SCAN
CLOCK
Title
Size A4
Number
Revision
Date: 26-Mar-2005
File: D:\Philip Titip\Rang Dot Matrika.DDB
Sheet of
Drawn By:

```
/*************************************************************
* Program CONTROL BELL SEKOLAH DENGAN SUARA
* Program ini Berpasangan dengan ITN_PLP2.C
*************************************************************/

#include <stdio.h>
#include <reg51.h>
#include <irq52.h>
#include <sys51.h>
#include <string.h>
#include <math.h>
#include "ds12887.h"
#include "keypad3.h"
#include "lcd_4bit.h"

#define enter  'B'
#define cancel 'A'
#define corect 'C'
#define menu   'D'
#define up     'E'
#define down   'F'

#define FCPU 12000000
#define frek_x 1000  //hz 8khz 0.125ms
#define prescaler  (65536-((FCPU/12)/frek_x))
#define baud_rate 9600
#define baud_rate_TH 253 //(256-((1*FCPU)/(32*12*baud_rate))) //253 //10592 251
//f18432  //252 //1481318//
#define jml_buf 10

const char baris1[]="PERENCANAAN DAN ";
const char baris2[]="PEMBUATAN BEL SE";
const char baris3[]="KOLAH YANG BISA ";
const char baris4[]="BERSUARA SECARA ";
const char baris5[]="OTOMATIS BERBA  ";
const char baris6[]="SIS   MICROCON ";
const char baris7[]="TROLLER AT89S52.";
const char baris8[]="                ";

inear uchar buf_serial[jml_buf];
near uchar ascl_des[4];
inear uchar buffer_key[4];
inear uchar jam_masuk[4];
inear uchar jam_istirahat[4];
inear uchar jam_msk_istirahat[4];
inear uchar jam_pulang[4];
near uchar  i_rd=0;
near uchar  i_wr=0;
```

```
near uchar buf_per,buf_jam,buf_menit,buf_detik=0;
near uchar buf_jam_rtc,buf_menit_rtc,buf_detik_rtc;
near uchar buf_jam2,buf_menit2,buf_detik2=0;
near uchar gsr,pjg,buf1,buf2,buf3,n,n2,data_key=0;
near uchar tunggu1,tunggu2,tunggu3,status,sts;
near uchar list=1;
near uchar select=1;
near uchar i,no_scrn,lama;
near uchar time_out,buf_prclr1,buf_prclr2=0;
near uint  cnt_down=1000;


//============== KERNEL SERIAL ==========================

void wr_mem (far char* name_mem,char data){
        *name_mem = data;
}

//=================== INTERUPSI SERIAL ===================

IRQ_VECTOR(kernel_serial,SERIAL)
void kernel_serial (void) interrupt  {
        RI = 0;
        wr_mem(buf_serial+i_wr,SBUF);
        if(++i_wr==jml_buf)i_wr=0;
}

//=================== INTERUPSI TIMER0 ===================


IRQ_VECTOR(timer0int,TIMER0)
void timer0int (void) interrupt  {
 TR0 =0;
 TH0 = buf_prclr1;
 TL0 = buf_prclr2;
 TR0 =1;
 if(!--cnt_down){
        cnt_down=1000;
        if(time_out)time_out--;
        else TR0=0;
 }
}

//=================== serial ===================

uchar rd_mem (far char* name_mem){
uchar data;
        data=*name_mem ;
```

```
return data;
}
void txC_serial(uchar data){
        EA=0;
        TI=0;
        SBUF=data;
        while(!TI);
        TI=0;
        EA=1;
}

uchar getC_serial (void){
uchar data;
        time_out=2;
        TR0=1;
        while(i_wr == i_rd)
                if(!time_out)break;
        data=rd_mem(buf_serial+i_rd);
        if(++i_rd==jml_buf)i_rd=0;
return  data;
}

void txS_serial(uchar *string){
uchar index;
        for(index=0;string[index] !=0; index++)
                txC_serial(string[index]);
}

uchar cek_Ok(void){
data_key=0;
        while(data_key != 'K'){
                data_key=getC_serial();  //OK
                if(!time_out)break;
        }
return  time_out;
}

void pesan_pop_up(uchar *line1,uchar *line2){
        lcd_gotoxy(0,0);
        lcd_puts(line1);
        lcd_gotoxy(0,1);
        lcd_puts(line2);
}
```

```
//=========================== INTERUPSI RTC ===========================

IRQ_VECTOR(int_0,IRQ_INT0)
void int_0 (void) interrupt  {
        EX0    = 0;
        _wait_ms(1);
        buf_jam_rtc=(uchar)get_rtc_jam();
        buf_menit_rtc=(uchar)get_rtc_menit();
        buf_detik_rtc=(uchar)get_rtc_detik();
        txS_serial("JM");
        txC_serial(buf_jam_rtc);
        txC_serial(buf_menit_rtc);
        txC_serial(buf_detik_rtc);
   no_scrn ++;
   if(no_scrn >=6)no_scrn = 0;
        EX0    = 1;
}

//=============================RUTIN SERIAL ============================
void clear_buf_serial(void){
        i_rd=0;
        i_wr=0;
        buf_per=0;
}

uchar cekC_serial (void){
uchar data=0;
        if(i_wr != i_rd)data=1;
return  data;
}

void tx_hex_serial(uchar data){
        n = data/16;
        if(n<=9)txC_serial(n|0x30);
        else txC_serial(n-10+0x41);
        n = data % 16;
        if(n<=9)txC_serial(n|0x30);
        else txC_serial(n-10+0x41);
}

//=========================== KONVERSI HEXA to ASCL ===========================
```

```
const char ascl[]={'0','1','2','3','4','5','6','7','8','9'};


void konvert_hex_to_ascl(uchar hex){
        ascl_des[0] = ascl [hex /100];
        hex = hex % 100;
        ascl_des[1] = ascl [hex /10];
        hex = hex % 10;
        ascl_des[2] = ascl [hex];
        ascl_des[3] = 0;
}

void tampil_lcd(uchar hexnya){
        konvert_hex_to_ascl(hexnya);
        lcd_puts(ascl_des);
}


void konvert_hex_to_ascl2(uchar hex){
        ascl_des[0] = ascl [hex /10];
        hex = hex % 10;
        ascl_des[1] = ascl [hex];
        ascl_des[2] = 0;
}

void tampil_lcd2(uchar hexnya){
        konvert_hex_to_ascl2(hexnya);
        lcd_puts(ascl_des);
}

uchar konvert_ascl_nilai(uchar data_keya,uchar col){

uchar hargaa;
data_keya -= 48;   //nilai ascl ke nilai sesungguhnya
        if(col==3)hargaa = (100 * data_keya);
        if(col==2)hargaa = (10 * data_keya);
        if(col==1)hargaa = (1 * data_keya);
return hargaa;
}


uchar save_mem(void){
uchar col,i,hex;
        hex=0;
        col=strlen(buffer_key);
        i=0;
        while(col>0){
                data_key=rd_mem(buffer_key+(i));
```

```
                hex += konvert_ascl_nilai(data_key,col);
                col--;
                i++;
        }
return hex;
}

//================ RUTIN UNTUK TAMPILAN MENU ==========

void cek_select(uchar select){
        if(select==1)
          lcd_gotoxy(15,0);
        else
          lcd_gotoxy(15,1);
        lcd_puts("< ");
}

uchar up_down_atas(uchar max){
uchar to_break=0;
        if(data_key==down){
         if(select==1)
           select=2;
         else{
           list ++;
           to_break=1;
         }
        }
        if(data_key==up){
         if(select==2)
           select=1;
         else{
           list=max;
           to_break=1;
         }
        }
return to_break;
}

uchar up_down_tengah(void){
uchar to_break=0;
        if(data_key==down){
         if(select==1)
           select=2;
         else{
           list ++;
           to_break=1;
         }
```

```
        }
        if(data_key==up){
         if(select==2)
           select=1;
         else{
           list--;
           to_break=1;
         }
        }
return to_break;
}

uchar up_down_bawah(void){
uchar to_break=0;
        if(data_key==down){
         if(select==1)
           select=2;
         else{
           list=1;
           to_break=1;
         }
        }
        if(data_key==up){
         if(select==2)
           select=1;
         else{
           list--;
           to_break=1;
         }
        }
return to_break;
}

uchar baca_key_nilai(uchar xpos,uchar jml_max,uchar buf_nil){
                konvert_hex_to_ascl2(buf_nil);
                strcpy(buffer_key,ascl_des);
                if((data_key >= 48) && (data_key <= 57)){
                        if(i<jml_max){
                                wr_mem((buffer_key+(i)),data_key);
                                i++;
                        }
                }
                if(data_key==corect){
                        if (i){
                                lcd_back();
                                i--;
                                lcd_gotoxy(xpos+i,1); //supaya no error loncat
                        }
```

```
                }
return  save_mem();
}

uchar baca_key_up_down(uchar batas_bawah,uchar batas_atas,uchar buf_hasil){
                if(data_key==up){
                        if(buf_hasil<batas_atas)
                                buf_hasil++;
                }
                if(data_key==down){
                        if(buf_hasil>batas_bawah)
                                buf_hasil--;
                }

return buf_hasil;
}

void menu_edit_jam(void){
        lcd_gotoxy(3,1);
        tampil_lcd2(buf_jam);
        lcd_gotoxy(6,1);
        tampil_lcd2(buf_menit);
        lcd_gotoxy(9,1);
        tampil_lcd2(buf_detik);
        i=0;
jam:    while(i<2){
                lcd_gotoxy(3+i,1);
                get_noC();
                data_key=getC();
                if (data_key==enter)break;
                if (data_key==cancel)goto gakjadi;
                if ((data_key==up)||(data_key==down))
                        buf_jam=baca_key_up_down(1,24,buf_jam);
                else
                        buf_jam=baca_key_nilai(3,2,buf_jam);
                if(buf_jam>23)buf_jam=23;
                lcd_gotoxy(3,1);
                tampil_lcd2(buf_jam);
        }
        i=0;
menit:  while(i<2){
                lcd_gotoxy(6+i,1);
                get_noC();
                data_key=getC();
                if (data_key==enter)break;
                if (data_key==cancel)goto gakjadi;
                if ((data_key==corect)&&(i==0)){
                                i=1;
```

```
                        goto jam;
                }
                if ((data_key==up)||(data_key==down))
                        buf_menit=baca_key_up_down(1,60,buf_menit);
                else
                        buf_menit=baca_key_nilai(3,2,buf_menit);
                if(buf_menit>59)buf_menit=59;
                lcd_gotoxy(6,1);
                tampil_lcd2(buf_menit);
        }
        i=0;
        while(1){
                lcd_gotoxy(9+i,1);
                get_noC();
                data_key=getC();
                if (data_key==enter)break;
                if (data_key==cancel)goto gakjadi;
                if ((data_key==corect)&&(i==0)){
                        i=1;
                        goto menit;
                }
                if ((data_key==up)||(data_key==down))
                        buf_detik=baca_key_up_down(1,60,buf_detik);
                else
                        buf_detik=baca_key_nilai(3,2,buf_detik);
                if(buf_detik>59)buf_detik=59;
                lcd_gotoxy(9,1);
                tampil_lcd2(buf_detik);
                if(i==2)i=1;
        }
gakjadi:data_key=0; ;
}

//========================= RUTIN RTC ==========================

void set_time_rtc(void){
        stop_update();
        rtc_write(4,buf_jam);
        rtc_write(2,buf_menit);
        rtc_write(0,buf_detik);
        init_rtc();
}

void save_rtc_setting(void){
        rtc_write(20,jam_masuk[0]);
        rtc_write(21,jam_masuk[1]);
        rtc_write(22,jam_masuk[2]);
```

```
        rtc_write(23,jam_istirahat[0]);
        rtc_write(24,jam_istirahat[1]);
        rtc_write(25,jam_istirahat[2]);
        rtc_write(26,jam_pulang[0]);
        rtc_write(27,jam_pulang[1]);
        rtc_write(28,jam_pulang[2]);
        rtc_write(29,jam_msk_istirahat[0]);
        rtc_write(30,jam_msk_istirahat[1]);
        rtc_write(31,jam_msk_istirahat[2]);
}

void load_rtc_setting(void){
        jam_masuk[0]=rtc_read(20);
        jam_masuk[1]=rtc_read(21);
        jam_masuk[2]=rtc_read(22);
        jam_masuk[3]=0;
        jam_istirahat[0]=rtc_read(23);
        jam_istirahat[1]=rtc_read(24);
        jam_istirahat[2]=rtc_read(25);
        jam_istirahat[3]=0;
        jam_pulang[0]=rtc_read(26);
        jam_pulang[1]=rtc_read(27);
        jam_pulang[2]=rtc_read(28);
        jam_pulang[3]=0;
        jam_msk_istirahat[0]=rtc_read(29);
        jam_msk_istirahat[1]=rtc_read(30);
        jam_msk_istirahat[2]=rtc_read(31);
        jam_msk_istirahat[3]=0;

}

void load_jam_setting(char* jam_set){
        buf_jam=jam_set[0];
        buf_menit=jam_set[1];
        buf_detik=jam_set[2];
}

void save_jam_setting(char* jam_set){
        jam_set[0]=buf_jam;
        jam_set[1]=buf_menit;
        jam_set[2]=buf_detik;
}

void menu_utama(void){
uchar buf_select;
uchar buf_list;
if (data_key == menu){
        list=1;
```

```
select=1;
lcd_gotoxy(0,0);
lcd_puts("SET JAM MASUK          ");
lcd_gotoxy(0,1);
lcd_puts("SET JAM ISTIRHT ");
cek_select(select);
while(data_key != cancel){
        if (list==1){
                while(data_key != cancel){
                        lcd_gotoxy(0,0);
                        lcd_puts("SET JAM MASUK   ");
                        lcd_gotoxy(0,1);
                        lcd_puts("SET JAM ISTIRHT ");
                        cek_select(select);
                        get_noC();
                        data_key=getC();
                        if(up_down_atas(5))break;
                        if(data_key==enter){
                                buf_select=select;
                                buf_list=list;
                                data_key=0;
                            lcd_gotoxy(0,1);
                            lcd_puts("  00:00:00    ");
                              lcd_gotoxy(0,0);
                              if(select==1){
                                 lcd_puts("SET JAM MASUK   ");
                                 load_jam_setting(jam_masuk);
                                 menu_edit_jam();
                                 save_jam_setting(jam_masuk);
                              }
                              else{
                                 lcd_puts("SET JAM ISTIRHT ");
                                 load_jam_setting(jam_istirahat);
                                 menu_edit_jam();
                                 save_jam_setting(jam_istirahat);
                              }
                            save_rtc_setting();
                              select=buf_select;
                              list=buf_list;
                        }
                }
        }
        if (list==2){
                while(data_key != cancel){
                        lcd_gotoxy(0,0);
                        lcd_puts("SET JAM ISTIRHT ");
                        lcd_gotoxy(0,1);
                        lcd_puts("SET JAM MSK IST ");
```

```
                    cek_select(select);
                    get_noC();
                    data_key=getC();
                    if(up_down_atas(4))break;
                    if(data_key==enter){
                            buf_select=select;
                            buf_list=list;
                            data_key=0;
                        lcd_gotoxy(0,1);
                        lcd_puts("  00:00:00    ");
                          lcd_gotoxy(0,0);
                          if(select==1){
                             lcd_puts("SET JAM ISTIRHT ");
                             load_jam_setting(jam_istirahat);
                             menu_edit_jam();
                             save_jam_setting(jam_istirahat);
                          }
                          else{
                             lcd_puts("SET JAM MSK IST ");
                             load_jam_setting(jam_msk_istirahat);
                             menu_edit_jam();
                             save_jam_setting(jam_msk_istirahat);
                          }
                        save_rtc_setting();
                          select=buf_select;
                          list=buf_list;
                    }
            }
}
if (list==3){
        while(data_key != cancel){
                    lcd_gotoxy(0,0);
                    lcd_puts("SET JAM MSK IST ");
                    lcd_gotoxy(0,1);
                    lcd_puts("SET JAM PULANG  ");
                    cek_select(select);
                    get_noC();
                    data_key=getC();
                    if(up_down_tengah())break;
                    if(data_key==enter){
                            buf_select=select;
                        buf_list=list;
                          data_key=0;
                        lcd_gotoxy(0,1);
                        lcd_puts("  00:00:00    ");
                          lcd_gotoxy(0,0);
                        if(select==1){
                              lcd_puts("SET JAM MSK IST ");
```

```
                        load_jam_setting(jam_msk_istirahat);
                        menu_edit_jam();
                        save_jam_setting(jam_msk_istirahat);
                    }
                else{
                        lcd_puts("SET JAM PULANG  ");
                        load_jam_setting(jam_pulang);
                        menu_edit_jam();
                        save_jam_setting(jam_pulang);
                    }
                save_rtc_setting();
                select=buf_select;
                list=buf_list;
            }
        }
}
if (list==4){
        while(data_key != cancel){
            lcd_gotoxy(0,0);
            lcd_puts("SET JAM PULANG  ");
            lcd_gotoxy(0,1);
            lcd_puts("SET JAM SYSTEM  ");
            cek_select(select);
            get_noC();
            data_key=getC();
            if(up_down_tengah())break;
            if(data_key==enter){
                buf_select=select;
                buf_list=list;
                data_key=0;
                lcd_gotoxy(0,1);
                lcd_puts("  00:00:00    ");
                lcd_gotoxy(0,0);
                if(select==1){
                    lcd_puts("SET JAM PULANG  ");
                    load_jam_setting(jam_pulang);
                    menu_edit_jam();
                    save_jam_setting(jam_pulang);
                    save_rtc_setting();
                }
                else{
                    lcd_puts("SET JAM SYSTEM  ");
                    buf_jam=buf_jam_rtc;
                    buf_menit=buf_menit_rtc;
                    buf_detik=buf_detik_rtc;
                    menu_edit_jam();
                    set_time_rtc();
                }
```

```
                    select=buf_select;
                    list=buf_list;
                }
            }
        }
        if (list==5){
            while(data_key != cancel){
                lcd_gotoxy(0,0);
                lcd_puts("SET JAM SYSTEM  ");
                lcd_gotoxy(0,1);
                lcd_puts("SET JAM MASUK   ");
                cek_select(select);
                get_noC();
                data_key=getC();
                if(up_down_bawah())break;
                if(data_key==enter){
                    buf_select=select;
                  buf_list=list;
                    data_key=0;
                  lcd_gotoxy(0,1);
                    lcd_puts("  00:00:00    ");
                    lcd_gotoxy(0,0);
                  if(select==1){
                      lcd_puts("SET JAM SYSTEM  ");
                      buf_jam=buf_jam_rtc;
                      buf_menit=buf_menit_rtc;
                      buf_detik=buf_detik_rtc;
                      menu_edit_jam();
                      set_time_rtc();
                    }
                  else{
                      lcd_puts("SET JAM MASUK   ");
                      load_jam_setting(jam_masuk);
                      menu_edit_jam();
                      save_jam_setting(jam_masuk);
                      save_rtc_setting();
                    }
                  select=buf_select;
                  list=buf_list;
                }
            }
        }

    }
  }
}

void tampil_jam(void){
```

```
        lcd_gotoxy(4,1);
        tampil_lcd2(buf_jam_rtc);
        lcd_gotoxy(7,1);
        tampil_lcd2(buf_menit_rtc);
        lcd_gotoxy(10,1);
        tampil_lcd2(buf_detik_rtc);
        lcd_kursor_out();
}

void bell_masuk_aktif(void){
        EX0  = 1;
        lcd_clear();
        lcd_gotoxy(0,0);
        lcd_puts("  BELL MASUK  ");
        lcd_gotoxy(0,1);
        lcd_puts("    AKTIF     ");
        clear_buf_serial();
        txS_serial("BM");
        if(!cek_Ok())pesan_pop_up("Pembacaan serial","   Gagal!!    ");
        _wait_ms(2000);
        EX0  = 1;
}

void bell_keluar_aktif(void){
  EX0  = 1;
  lcd_clear();
  lcd_gotoxy(0,0);
  lcd_puts(" BELL PULANG  ");
  lcd_gotoxy(0,1);
  lcd_puts("    AKTIF     ");
  clear_buf_serial();
  txS_serial("BK");
  if(!cek_Ok())pesan_pop_up("Pembacaan serial","   Gagal!!    ");
  _wait_ms(2000);
  EX0  = 1;
}

void bell_istirahat_aktif(void){
        EX0 = 0;
        lcd_clear();
        lcd_gotoxy(0,0);
        lcd_puts(" BELL ISTIRAHAT ");
        lcd_gotoxy(0,1);
        lcd_puts("    AKTIF     ");
        clear_buf_serial();
        txS_serial("BI");
        if(!cek_Ok())pesan_pop_up("Pembacaan serial","   Gagal!!    ");
        _wait_ms(2000);
```

```
        EX0    = 1;
}

void bell_aktif(void){
   EX0 = 0;
   lcd_clear();
   lcd_gotoxy(0,0);
   lcd_puts("    BELL     ");
   lcd_gotoxy(0,1);
   lcd_puts("    AKTIF    ");
   clear_buf_serial();
   txS_serial("BL");
   if(!cek_Ok())pesan_pop_up("Pembacaan serial","   Gagal!!    ");
   _wait_ms(2000);
   EX0    = 1;
}

void gerbang_buka(void){
        EX0    = 0;
        lcd_clear();
        lcd_gotoxy(0,0);
        lcd_puts(" GERBANG BUKA  ");
        lcd_gotoxy(0,1);
        lcd_puts("    AKTIF    ");
        clear_buf_serial();
        txS_serial("GO");
        if(!cek_Ok())pesan_pop_up("Pembacaan serial","   Gagal!!    ");
        _wait_ms(2000);
        EX0    = 1;

}


void gerbang_tutup(void){
   EX0    = 0;
   lcd_clear();
   lcd_gotoxy(0,0);
   lcd_puts(" GERBANG TUTUP  ");
   lcd_gotoxy(0,1);
   lcd_puts("    AKTIF    ");
   clear_buf_serial();
   txS_serial("GC");
   if(!cek_Ok())pesan_pop_up("Pembacaan serial","   Gagal!!    ");
   _wait_ms(2000);
   EX0    = 1;

}
```

```
void gerbang_bell_buka(void){
   EX0    = 0;
   lcd_clear();
   lcd_gotoxy(0,0);
   lcd_puts("BEL GERBANG BUKA");
   lcd_gotoxy(0,1);
   lcd_puts("    AKTIF     ");
   clear_buf_serial();
   txS_serial("GL");
   if(!cek_Ok())pesan_pop_up("Pembacaan serial","   Gagal!!    ");
   _wait_ms(2000);
   EX0    = 1;

}

void controller(void){
        if(jam_masuk[0]==buf_jam_rtc){
                if(jam_masuk[1]==buf_menit_rtc){
                        if(jam_masuk[2]==buf_detik_rtc){
                        bell_masuk_aktif();
                        }
                }
        }
        if(jam_istirahat[0]==buf_jam_rtc){
                if(jam_istirahat[1]==buf_menit_rtc){
                        if(jam_istirahat[2]==buf_detik_rtc){
                        bell_istirahat_aktif();
                        }
                }
        }
        if(jam_msk_istirahat[0]==buf_jam_rtc){
                if(jam_msk_istirahat[1]==buf_menit_rtc){
                        if(jam_msk_istirahat[2]==buf_detik_rtc){
                        bell_masuk_aktif();
                        }
                }
        }
        if(jam_pulang[0]==buf_jam_rtc){
                if(jam_pulang[1]==buf_menit_rtc){
                        if(jam_pulang[2]==buf_detik_rtc){
                        bell_keluar_aktif();
                        }
                }
        }
}

void screen(void){
   if(lama != no_scrn){
```

```
        lama = no_scrn;
        lcd_gotoxy(0,0);
        lcd_puts(baris1+(no_scrn * 17));
        lcd_gotoxy(0,1);
        lcd_puts(baris2+(no_scrn * 17));
    }
}

void main(void){
        EA    = 0;
        TMOD  = 0;
        TMOD  &= 0xF0;   // TMOD Timer 0:
        TMOD  |= 0x01;        // 16 Bit Mode 1 16 bit counter
        TMOD  |= 0x20;   //timer1 mode2 outo reload
        TH0 = (uchar)((prescaler+30)>>8);
        TL0 = (uchar)(prescaler+30);  //+30 waktu buat set TH dan TL
        buf_prclr1=(uchar)((prescaler+62)>>8);
        buf_prclr2=(uchar)(prescaler+62);
        TH1   = baud_rate_TH;
        TL1   = baud_rate_TH;
        TR1   = 1;
        TR0   = 0;
        SCON = 0x50;
        EX0   = 1;
        ES    = 1;   //enable serial
        ET0   = 1;    //enable timer0
        IP   =0x10;   //prioriti int serial
        lcd_init();
        lcd_gotoxy(0,0);
        lcd_puts("FILIP WONGSO W.   ITN MALANG  ");
        lcd_gotoxy(0,1);
        lcd_puts(" [99,17,118]   T.ELEKTRONIKA ");
        _wait_ms(3000);
        lcd_geser_kiri(16,100);
        _wait_ms(3000);
 lcd_clear();
        lcd_gotoxy(0,0);
        lcd_puts("  ITN MALANG  ");
        lcd_gotoxy(0,1);
        lcd_puts(" T.ELEKTRONIKA ");
        _wait_ms(3000);
        EA =1;
        init_rtc();
        load_rtc_setting();
 no_scrn = 0;
        while(1){
    screen();
    controller();
```

```
            if(cekC()){
                    data_key=getC();
                    if(data_key==menu){
                            lcd_clear();
                            menu_utama();
                    }
                    if(data_key=='1'){
    bell_aktif();
                    }
                    if(data_key=='2'){
    gerbang_buka();
                    }
                    if(data_key=='3'){
    gerbang_bell_buka();
                    }
    if(data_key=='5'){
      gerbang_tutup();
    }
            }
    }
}
```

```
/*********************************************************************
*

*********************************************************************
/
#include <stdio.h>
#include <reg51.h>
#include <sys51.h>
#include <irq52.h>
#include "dotmatrk.h"

#define FCPU 12000000
#define baud_rate 9600
#define baud_rate_TH 253 // (256-((1*FCPU)/(32*12*baud_rate))) //253 //10592
251 //f18432  //252 //1481318//
#define jml_buf 10
#define motor_relay1 P1_B0
#define motor_relay2 P1_B1
#define sensor_tutup P1_B5
#define sensor_buka P1_B6
#define bell_aktif  P1_B4
#define adrs_isd P2
#define playl  P0_B7

near uchar  buf_serial[jml_buf];
near uchar i_rd=0;
near uchar i_wr=0;
near uchar perintah;
near uchar jam,menit,detik;
near uchar ascl_des[3];

void wr_mem (far char* name_mem,char data){
        *name_mem = data;
}

IRQ_VECTOR(kernel_serial,SERIAL)
void kernel_serial (void) interrupt  {
        RI = 0;
        wr_mem(buf_serial+i_wr,SBUF);
        if(++i_wr==jml_buf)i_wr=0;
}


uchar rd_mem (far char* name_mem){
uchar data;
        data=*name_mem ;
return data;
```

```
}

uchar cekC_serial (void){
uchar data=0;
        if(i_wr != i_rd)data=1;
return  data;
}

uchar getC_serial (void){
uchar data;
        while(i_wr == i_rd);
        data=rd_mem(buf_serial+i_rd);
        if(++i_rd==jml_buf)i_rd=0;
return  data;
}

void txC_serial(uchar data){
        EA=0;
        TI=0;
        SBUF=data;
        while(!TI);
        TI=0;
        EA=1;
}

void txS_serial(uchar *string){
uchar index;
        for(index=0;string[index] !=0; index++)
                txC_serial(string[index]);
}

void kirim_ok(void){
        txC_serial('O');
        txC_serial('K');
}

const char ascl[]={'0','1','2','3','4','5','6','7','8','9'};

void konvert_hex_to_ascl2(uchar hex){
        ascl_des[0] = ascl [hex /10];
        hex = hex % 10;
        ascl_des[1] = ascl [hex];
        ascl_des[2] = 0;
}

void tampil_jam(void){
        konvert_hex_to_ascl2(jam);
```

```
        Dot_mtrk_xpos(7);
        Dot_mtrk_puts(ascl_des);
        konvert_hex_to_ascl2(menit);
        Dot_mtrk_xpos(25);
        Dot_mtrk_puts(ascl_des);
        konvert_hex_to_ascl2(detik);
        Dot_mtrk_xpos(43);
        Dot_mtrk_puts(ascl_des);
}

void bell_bunyi(void){
        bell_aktif=0;
        _wait_ms(200);
        bell_aktif=1;
        _wait_ms(200);
        bell_aktif=0;
        _wait_ms(200);
        bell_aktif=1;
        _wait_ms(200);
        bell_aktif=0;
        _wait_ms(200);
        bell_aktif=1;
}

void bell_bunyi2(void){
  bell_aktif=0;
  _wait_ms(200);
  bell_aktif=1;
  _wait_ms(200);
  bell_aktif=0;
  _wait_ms(200);
  bell_aktif=1;
}

void bell_bunyi3(void){
  bell_aktif=0;
  _wait_ms(200);
  bell_aktif=1;
}

void suara_masuk(void){
        playl=1;
        adrs_isd=0x00;
        _wait_ms(1);
        playl=0;
}
void suara_istirahat(void){
```

```
        playl =1;
        adrs_isd =0x30;
        _wait_ms(1);
        playl =0;
}
void suara_pulang(void){
        playl =1;
        adrs_isd =0x68;
        _wait_ms(1);
        playl =0;
}

void stop_suara(void){
        playl =1;
}

void Pagar_tutup(void){
        motor_relay1=0;
        motor_relay2=1;
}

void Pagar_buka(void){
        motor_relay1=1;
        motor_relay2=0;
}

void cek_max_buka(void){
        if(!sensor_buka){
                motor_relay1=0;
                motor_relay2=0;
        }
}

void cek_max_tutup(void){
        if(!sensor_tutup){
                motor_relay1=0;
                motor_relay2=0;
        }
}

void main(void){
        EA  = 0;
        TMOD = 0;
        Dot_mtrk_init();
        TMOD |= 0x20;  //timer1 mode2 outo reload
        TH1  = baud_rate_TH;
        TL1  = baud_rate_TH;
```

```
        ES  =1;    //enableint serial
        IP  |=0x10; //prioriti serial
        TR1  = 1;
        SCON = 0x50;
        EA   = 1;
        bell_aktif=1;
        playl =1;
        motor_relay1=0;
        motor_relay2=0;
        Dot_mtrk_puts_geser_kiri("FILIP WONGSO WIBOW");
        Dot_mtrk_puts_geser_kiri("O 99.17.118  TEKNI");
        Dot_mtrk_puts_geser_kiri("K ELEKTRONIKA INST");
        Dot_mtrk_puts_geser_kiri("ITUT TEKNOLOGI NAS");
        Dot_mtrk_puts_geser_kiri("IONAL MALANG  ");
        Dot_mtrk_puts_geser_kiri(" 00:00:00 WIB     ");
        kirim_ok();
        while(1){
                tampil_jam();
                if(cekC_serial()){
                                perintah=getC_serial();
                                switch(perintah){
                                case 'B':perintah=getC_serial();
                                        if('M'==perintah){
                                                kirim_ok();
                                                bell_bunyi();
                                                _wait_ms(500);
                                                Pagar_tutup();
                                                cek_max_tutup();

                                                suara_masuk();
                                                Dot_mtrk_puts_geser_kiri(" WAKTU
MASUK     ");
                                                Dot_mtrk_putar_kiri();
                                                while(sensor_tutup)playl ^=1;
                                                playl =1;
                                                cek_max_tutup();
                                                playl =0;
                                                _wait_ms(1000);
                                                stop_suara();
                                                Dot_mtrk_stop_putar();
                                                Dot_mtrk_puts_geser_kiri(" 00:00:00
WIB     ");
                                                break;
                                        }
                                        if('I'==perintah){
                                                kirim_ok();
                                                bell_bunyi2();
```

```
                                        _wait_ms(500);
                                        suara_istirahat();
                                        Dot_mtrk_puts_geser_kiri("WAKTU
    ISTIRAHAT  ");
                                        playl =1;
                                        Dot_mtrk_putar_kiri();
                                        playl =0;
                                        _wait_ms(1000);
                                        stop_suara();
                                        Dot_mtrk_stop_putar();
                                        Dot_mtrk_puts_geser_kiri(" 00:00:00
    WIB    ");
                                    break;
                                    }
                                    if('K'==perintah){
                                        kirim_ok();
                                        bell_bunyi();
                                        _wait_ms(500);

                                        Pagar_buka();
            cek_max_buka();
                                        suara_pulang();
                                        Dot_mtrk_puts_geser_kiri(" WAKTU
    PULANG    ");
                                        Dot_mtrk_putar_kiri();
                                        while(sensor_buka)playl ^=1;
                                        playl =1;
                                        cek_max_buka();
                                        playl =0;
                                        _wait_ms(1000);
                                        stop_suara();
                                        Dot_mtrk_stop_putar();
                                        Dot_mtrk_puts_geser_kiri(" 00:00:00
    WIB    ");
                                    break;
                                    }
            if('L'==perintah){
              kirim_ok();
              bell_bunyi3();
              break;
            }
                        case 'J':perintah=getC_serial();
                            if('M'==perintah){
                                kirim_ok();
                                jam=getC_serial();
                                menit=getC_serial();
                                detik=getC_serial();
```

```
                                                    break;
                                                }
                case 'G':perintah=getC_serial();
                    if('C'==perintah){
                        kirim_ok();
                        Pagar_tutup();
                        while(sensor_tutup);
                        cek_max_tutup();
                        break;
                    }
                    if('O'==perintah){
                        kirim_ok();
                        Pagar_buka();
                        while(sensor_buka);
                        cek_max_buka();
                        break;
                    }
                    if('L'==perintah){
                        kirim_ok();
                        bell_bunyi();
                        _wait_ms(200);
                        Pagar_buka();
                        while(sensor_buka);
                        cek_max_buka();
                        break;
                    }
                default :txC_serial(perintah);
                                    }
                            }
                    _wait_ms(50);
            }
    }

    // END
```

INSTITUT TEKNOLOGI NASIONAL
Jl. Bendungan Sigura-gura No. 2
MALANG

LEMBAR BIMBINGAN SKRIPSI

1.	Nama	: Filip Wongso Wibowo
2.	NIM	: 9917118
3.	Jurusan	: Teknik Elektro S-1
4.	Konsentrasi	: Teknik Elektronika
5.	Judul Skripsi	: Perencanaan dan Pembuatan Bel Sekolah yang Bisa Bersuara Secara Otomatis Dilengkapi Dengan Matrik Led Sebagai Tampilan Berbasis Mikrokontroller AT 89S52
6.	Tanggal Pengajuan Skripsi	: 24 April 2004
7.	Selesai Menulis Skripsi	: 26 Maret 2005
8.	Dosen Pembimbing	: Joseph Dedy Irawan, ST, MT
9.	Telah Dievaluasi Dengan Nilai	: 90 (Sembilan Puluh)

Malang, April 2005

Mengetahui,	Diperiksa dan Disetujui
Ketua Jurusan Teknik Elektro S – 1	Dosen Pembimbing
Ir. F. Yudi Limpraptono, MT	Joseph Dedy Irawan, ST, MT
NIP. Y. 103 950 0274	NIP. P. 103 980 0324

INSTITUT TEKNOLOGI NASIONAL MALANG
JL. Bendungan Sigura-gura No.2
Malang

FORMULIR PERBAIKAN SKRIPSI

Dari hasil ujian skripsi Jenjang Strata Satu (S-1) Jurusan Teknik Elektro Konsentrasi Teknik Elektronika yang diselenggarakan pada :

Hari : Selasa

Tanggal : 29 Maret 2005

Telah dilakukan perbaikan skripsi oleh :

1. Nama : Filip Wongso Wibowo
2. NIM : 99.17.118
3. Jurusan : Teknik Elektro S – 1
4. Konsentrasi : Teknik Elektronika
5. Judul Skripsi : **PERENCANAAN DAN PEMBUATAN BEL SEKOLAH YANG BISA BERSUARA SECARA OTOMATIS DILENGKAPI DENGAN MATRIK LED SEBAGAI TAMPILAN BERBASIS MIKROKONTROLLER AT 89S52**

Perbaikan meliputi :

No	Materi Perbaikan	Keterangan
1	Tata Tulis	

Dosen Pembimbing

Joseph Dédy Irawan, ST, MT
NIP. P. 103 980 0324

Anggota Penguji

Penguji Pertama

Ir. F. Yudi Limpraptono, MT
NIP. Y. 103 950 0274

Penguji Kedua

Ir. Erfan. A. Dahlan
NIP. 131 124 663

INSTITUT TEKNOLOGI NASIONAL MALANG
FAKULTAS TEKNOLOGI INDUSTRI
JURUSAN TEKNIK ELEKTRO

Formulir Perbaikan Ujian Skripsi

Dalam pelaksanaan Ujian Skripsi Janjang Strata 1 Jurusan Teknik Elektro Konsentrasi T. Energi Listrik / T. Elektronika, maka perlu adanya perbaikan skripsi untuk mahasiswa :

NAMA : Filip Wonyo W.
N I M :
Perbaikan meliputi :

Malang, 30/3 200[illegible]

(_____)

INSTITUT TEKNOLOGI NASIONAL MALANG
FAKULTAS TEKNOLOGI INDUSTRI
JURUSAN TEKNIK ELEKTRO

Formulir Perbaikan Ujian Skripsi

Dalam pelaksanaan Ujian Skripsi Janjang Strata 1 Jurusan Tekrik Elektro Konsentrasi T. Energi Listrik / T. Elektronika, maka perlu adanya perbaikan skripsi untuk mahasiswa :

NAMA :
N I M :
Perbaikan meliputi :

Malang, 200

(_____)

PERKUMPULAN PENGELOLA PENDIDIKAN UMUM DAN TEKNOLOGI NASIONAL MALANG
INSTITUT TEKNOLOGI NASIONAL MALANG
FAKULTAS TEKNOLOGI INDUSTRI
FAKULTAS TEKNIK SIPIL DAN PERENCANAAN
PROGRAM PASCASARJANA MAGISTER TEKNIK

T. BNI (PERSERO) MALANG
BANK NIAGA MALANG

Kampus I : Jl. Bendungan Sigura-gura No. 2 Telp. (0341) 551431 (Hunting) Fax. (0341) 553015 Malang 65145
Kampus II : Jl. Raya Karanglo, Km 2 Telp. (0341) 417636 Fax. (0341) 417634 Malang

Nomor : ITN-394/7/TA.GNP/2004
Lampiran :
Perihal : ***Bimbingan Skripsi***

Malang, 24-Apr-2004

Kepada : Yth. **Joseph Dedy Irawan, ST, MT**
Dosen Institut Teknologi Nasional
M a l a n g

Dengan hormat,
Sesuai dengan permohonan dan persetujuan dalam proposal skripsi untuk Mahasiswa :

N a m a	: Filip Wongso Wibowo
N i m	: 9917118
Semester	: X
Fakultas	: Teknologi Industri
Jurusan	: Teknik Elektro S-1
Konsentrasi	: Elektronika

Maka dengan ini pembimbingan Skripsi tersebut kami serahkan sepenuhnya kepada Saudara/i selama masa waktu 6 (enam) bulan, terhitung mulai tanggal :

24-Apr-2004 s/d 25-Oct-2004

Sebagai satu syarat untuk menempuh Ujian Akhir Sarjana.
Demikian agar maklum, atas perhatian dan bantuannya kami ucapkan banyak terima kasih.

Ketua
Jurusan Teknik Elektro

Ir. I Made Wartana, MT
NIP 131 991 182

Tembusan Kepada Yth :
1. Mahasiswa yang bersangkutan
2. Arsip

INSTITUT TEKNOLOGI NASIONAL
Jl. Bendungan Sigura-gura No. 2
M A L A N G

FORMULIR BIMBINGAN SKRIPSI

Nama : Filip Wongso Wibowo
Nim : 9917118
Masa Bimbingan : 24-Apr-2004 s\d 25-Oct-2004
Judul Skripsi : Perencanaan dan pembuatan bel sekolah yang bisa bersuara secara otomatis di lengkapi dengan Matrik Led sebagai tampilan berbasis Mikrokontroller AT89S51

No	Tanggal	Uraian	Paraf Pembimbing
1.	17-11-2004	Konsultasi Rangkaian Min. Sistem	
2.	21-12-2004	Acc Rangkaian Minimum Sistem	
3.	6-1-2005	Acc Bab I, II, III	
4.	8-2-2005	Revisi judul dari AT 89S51 menjadi AT 89S52	
5.	26-2-2005	Acc Makalah Seminar	
6.	26-3-2005	Revisi Penulisan dan Sumber	
7.	26-3-2005	Acc Laporan Skripsi	
8.			
9.			
10.			

Malang, 26-3-2005
Dosen Pembimbing

Joseph Dedy Irawan, ST, MT

eatures

- Compatible with MCS-51® Products
- 8K Bytes of In-System Programmable (ISP) Flash Memory
  - Endurance: 1000 Write/Erase Cycles
- 4.0V to 5.5V Operating Range
- Fully Static Operation: 0 Hz to 33 MHz
- Three-level Program Memory Lock
- 256 x 8-bit Internal RAM
- 32 Programmable I/O Lines
- Three 16-bit Timer/Counters
- Eight Interrupt Sources
- Full Duplex UART Serial Channel
- Low-power Idle and Power-down Modes
- Interrupt Recovery from Power-down Mode
- Watchdog Timer
- Dual Data Pointer
- Power-off Flag

escription

ne AT89S52 is a low-power, high-performance CMOS 8-bit microcontroller with 8K ytes of in-system programmable Flash memory. The device is manufactured using tmel's high-density nonvolatile memory technology and is compatible with the indus-y-standard 80C51 instruction set and pinout. The on-chip Flash allows the program emory to be reprogrammed in-system or by a conventional nonvolatile memory pro-ammer. By combining a versatile 8-bit CPU with in-system programmable Flash on monolithic chip, the Atmel AT89S52 is a powerful microcontroller which provides a ghly-flexible and cost-effective solution to many embedded control applications.

ne AT89S52 provides the following standard features: 8K bytes of Flash, 256 bytes RAM, 32 I/O lines, Watchdog timer, two data pointers, three 16-bit timer/counters, a x-vector two-level interrupt architecture, a full duplex serial port, on-chip oscillator, id clock circuitry. In addition, the AT89S52 is designed with static logic for operation wn to zero frequency and supports two software selectable power saving modes. ne Idle Mode stops the CPU while allowing the RAM, timer/counters, serial port, and terrupt system to continue functioning. The Power-down mode saves the RAM con-nts but freezes the oscillator, disabling all other chip functions until the next interrupt hardware reset.

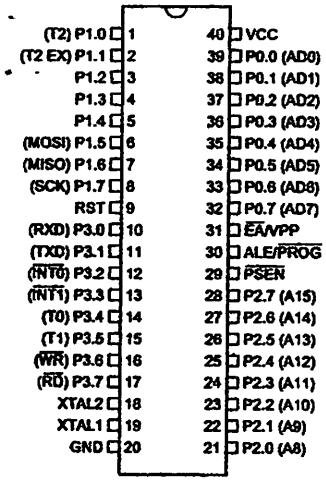
8-bit Microcontroller with 8K Bytes In-System Programmable Flash

AT89S52

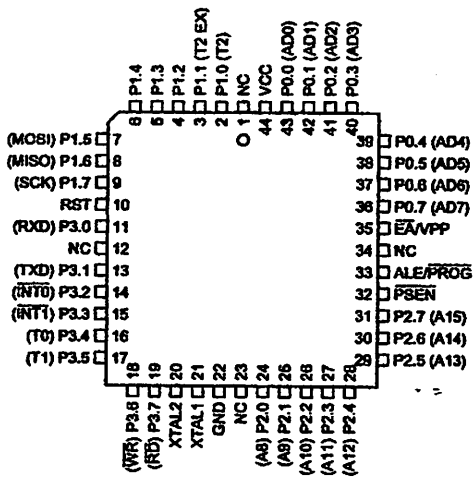
Rev. 1919A-07/01

Pin Configurations

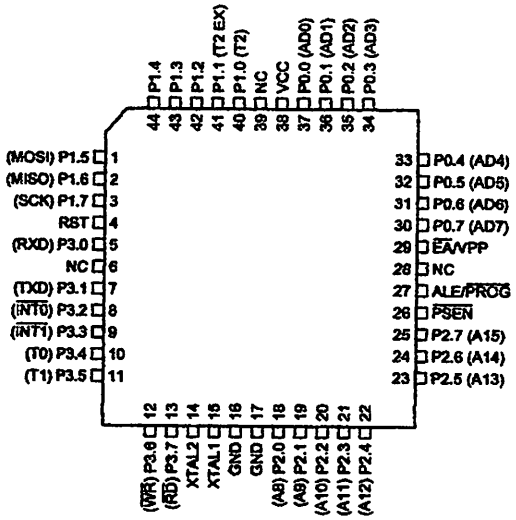
PDIP



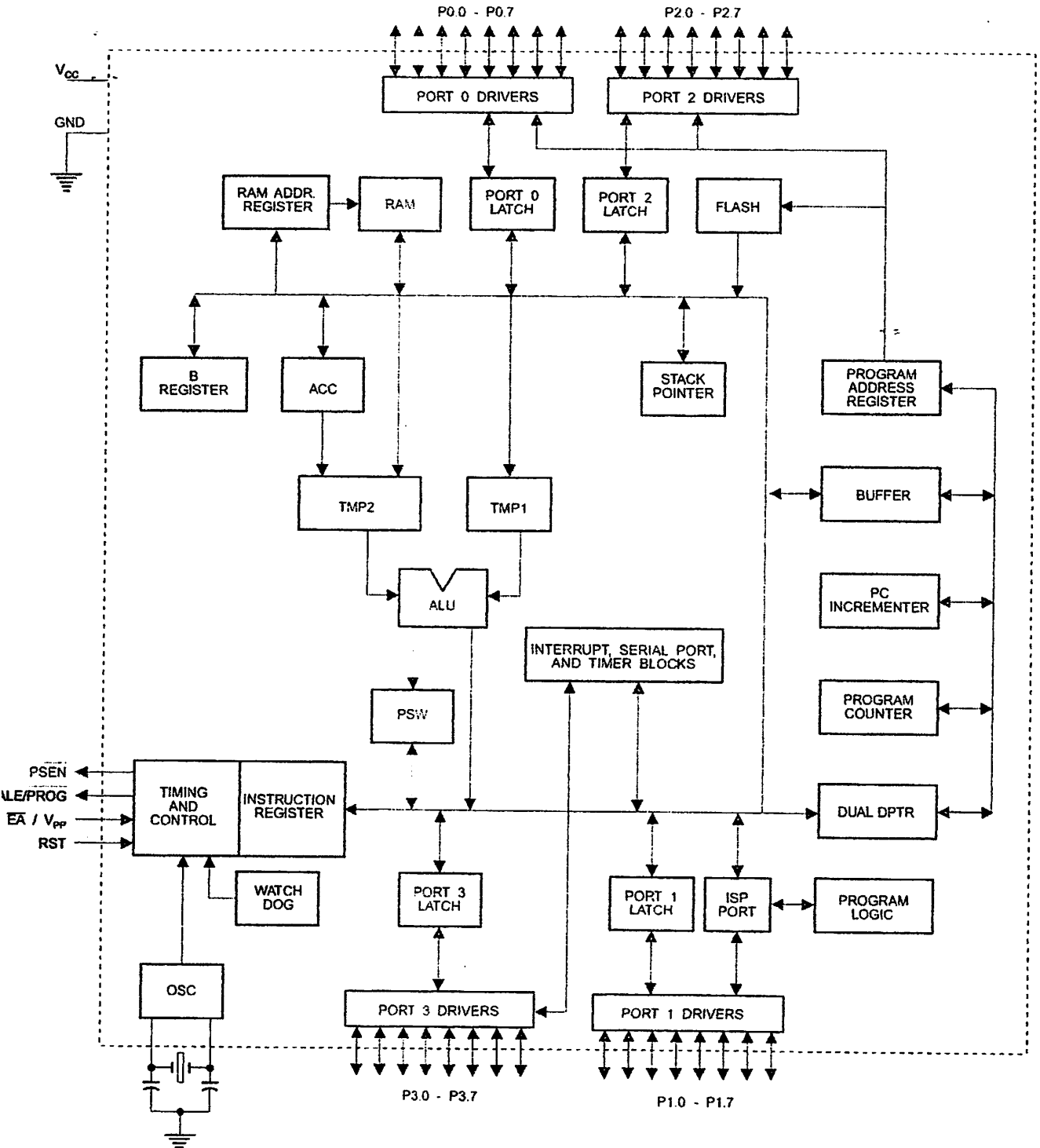
PLCC



TQFP



Block Diagram



Pin Description

VCC
Supply voltage.

GND
Ground.

Port 0
Port 0 is an 8-bit open drain bidirectional I/O port. As an output port, each pin can sink eight TTL inputs. When 1s are written to port 0 pins, the pins can be used as high-impedance inputs.

Port 0 can also be configured to be the multiplexed low-order address/data bus during accesses to external program and data memory. In this mode, P0 has internal pullups.

Port 0 also receives the code bytes during Flash programming and outputs the code bytes during program verification. External pullups are required during program verification.

Port 1
Port 1 is an 8-bit bidirectional I/O port with internal pullups. The Port 1 output buffers can sink/source four TTL inputs. When 1s are written to Port 1 pins, they are pulled high by the internal pullups and can be used as inputs. As inputs, Port 1 pins that are externally being pulled low will source current (I_{IL}) because of the internal pullups.

In addition, P1.0 and P1.1 can be configured to be the timer/counter 2 external count input (P1.0/T2) and the timer/counter 2 trigger input (P1.1/T2EX), respectively, as shown in the following table.

Port 1 also receives the low-order address bytes during Flash programming and verification.

Port Pin	Alternate Functions
P1.0	T2 (external count input to Timer/Counter 2), clock-out
P1.1	T2EX (Timer/Counter 2 capture/reload trigger and direction control)
P1.5	MOSI (used for In-System Programming)
P1.6	MISO (used for In-System Programming)
P1.7	SCK (used for In-System Programming)

Port 2
Port 2 is an 8-bit bidirectional I/O port with internal pullups. The Port 2 output buffers can sink/source four TTL inputs. When 1s are written to Port 2 pins, they are pulled high by the internal pullups and can be used as inputs. As inputs, Port 2 pins that are externally being pulled low will source current (I_{IL}) because of the internal pullups.

Port 2 emits the high-order address byte during fetches from external program memory and during accesses to external data memory that use 16-bit addresses (MOVX @ DPTR). In this application, Port 2 uses strong internal pullups when emitting 1s. During accesses to external data memory that use 8-bit addresses (MOVX @ RI), Port 2 emits the contents of the P2 Special Function Register.

Port 2 also receives the high-order address bits and some control signals during Flash programming and verification.

Port 3
Port 3 is an 8-bit bidirectional I/O port with internal pullups. The Port 3 output buffers can sink/source four TTL inputs. When 1s are written to Port 3 pins, they are pulled high by the internal pullups and can be used as inputs. As inputs, Port 3 pins that are externally being pulled low will source current (I_{IL}) because of the pullups.

Port 3 also serves the functions of various special features of the AT89S52, as shown in the following table.

Port 3 also receives some control signals for Flash programming and verification.

Port Pin	Alternate Functions
P3.0	RXD (serial input port)
P3.1	TXD (serial output port)
P3.2	$\overline{INT0}$ (external interrupt 0)
P3.3	$\overline{INT1}$ (external interrupt 1)
P3.4	T0 (timer 0 external input)
P3.5	T1 (timer 1 external input)
P3.6	$\overline{WR}$ (external data memory write strobe)
P3.7	$\overline{RD}$ (external data memory read strobe)

RST
Reset input. A high on this pin for two machine cycles while the oscillator is running resets the device. This pin drives High for 96 oscillator periods after the Watchdog times out. The DISRTO bit in SFR AUXR (address 8EH) can be used to disable this feature. In the default state of bit DISRTO, the RESET HIGH out feature is enabled.

ALE/$\overline{PROG}$
Address Latch Enable (ALE) is an output pulse for latching the low byte of the address during accesses to external memory. This pin is also the program pulse input ($\overline{PROG}$) during Flash programming.

In normal operation, ALE is emitted at a constant rate of 1/6 the oscillator frequency and may be used for external timing or clocking purposes. Note, however, that one ALE pulse is skipped during each access to external data memory.

If desired, ALE operation can be disabled by setting bit 0 of SFR location 8EH. With the bit set, ALE is active only during a MOVX or MOVC instruction. Otherwise, the pin is

eakly pulled high. Setting the ALE-disable bit has no ffect if the microcontroller is in external execution mode.

SEN

rogram Store Enable ($\overline{PSEN}$) is the read strobe to exter-al program memory.

hen the AT89S52 is executing code from external pro-ram memory, $\overline{PSEN}$ is activated twice each machine ycle, except that two $\overline{PSEN}$ activations are skipped during ach access to external data memory.

A/VPP

xternal Access Enable. $\overline{EA}$ must be strapped to GND in rder to enable the device to fetch code from external pro-ram memory locations starting at 0000H up to FFFFH. Note, however, that if lock bit 1 is programmed, $\overline{EA}$ will be internally latched on reset.

$\overline{EA}$ should be strapped to V_{CC} for internal program executions.

This pin also receives the 12-volt programming enable voltage (V_{PP}) during Flash programming.

XTAL1

Input to the inverting oscillator amplifier and input to the internal clock operating circuit.

XTAL2

Output from the inverting oscillator amplifier.

able 1. AT89S52 SFR Map and Reset Values

0F8H								0FFH
0F0H	B 00000000							0F7H
0E8H								0EFH
0E0H	ACC 00000000							0E7H
0D8H								0DFH
0D0H	PSW 00000000							0D7H
0C8H	T2CON 00000000	T2MOD XXXXXX00	RCAP2L 00000000	RCAP2H 00000000	TL2 00000000	TH2 00000000		0CFH
0C0H								0C7H
0B8H	IP XX000000							0BFH
0B0H	P3 11111111							0B7H
0A8H	IE 0X000000							0AFH
0A0H	P2 11111111		AUXR1 XXXXXXX0				WDTRST XXXXXXXX	0A7H
98H	SCON 00000000	SBUF XXXXXXXX						9FH
90H	P1 11111111							97H
88H	TCON 00000000	TMOD 00000000	TL0 00000000	TL1 00000000	TH0 00000000	TH1 00000000	AUXR XXX00XX0	8FH
80H	P0 11111111	SP 00000111	DP0L 00000000	DP0H 00000000	DP1L 00000000	DP1H 00000000	PCON 0XXX0000	87H

Special Function Registers

A map of the on-chip memory area called the Special Function Register (SFR) space is shown in Table 1.

Note that not all of the addresses are occupied, and unoccupied addresses may not be implemented on the chip. Read accesses to these addresses will in general return random data, and write accesses will have an indeterminate effect.

User software should not write 1s to these unlisted locations, since they may be used in future products to invoke new features. In that case, the reset or inactive values of the new bits will always be 0.

Timer 2 Registers: Control and status bits are contained in registers T2CON (shown in Table 2) and T2MOD (shown in Table 3) for Timer 2. The register pair (RCAP2H, RCAP2L) are the Capture/Reload registers for Timer 2 in 16-bit capture mode or 16-bit auto-reload mode.

Interrupt Registers: The individual interrupt enable bits are in the IE register. Two priorities can be set for each of the six interrupt sources in the IP register.

Table 2. T2CON – Timer/Counter 2 Control Register

T2CON Address = 0C8H — Reset Value = 0000 0000B

Bit Addressable

Bit	TF2	EXF2	RCLK	TCLK	EXEN2	TR2	C/$\overline{T2}$	CP/$\overline{RL2}$
	7	6	5	4	3	2	1	0

Symbol	Function
TF2	Timer 2 overflow flag set by a Timer 2 overflow and must be cleared by software. TF2 will not be set when either RCLK = 1 or TCLK = 1.
EXF2	Timer 2 external flag set when either a capture or reload is caused by a negative transition on T2EX and EXEN2 = 1. When Timer 2 interrupt is enabled, EXF2 = 1 will cause the CPU to vector to the Timer 2 interrupt routine. EXF2 must be cleared by software. EXF2 does not cause an interrupt in up/down counter mode (DCEN = 1).
RCLK	Receive clock enable. When set, causes the serial port to use Timer 2 overflow pulses for its receive clock in serial port Modes 1 and 3. RCLK = 0 causes Timer 1 overflow to be used for the receive clock.
TCLK	Transmit clock enable. When set, causes the serial port to use Timer 2 overflow pulses for its transmit clock in serial port Modes 1 and 3. TCLK = 0 causes Timer 1 overflows to be used for the transmit clock.
EXEN2	Timer 2 external enable. When set, allows a capture or reload to occur as a result of a negative transition on T2EX if Timer 2 is not being used to clock the serial port. EXEN2 = 0 causes Timer 2 to ignore events at T2EX.
TR2	Start/Stop control for Timer 2. TR2 = 1 starts the timer.
C/$\overline{T2}$	Timer or counter select for Timer 2. C/$\overline{T2}$ = 0 for timer function. C/$\overline{T2}$ = 1 for external event counter (falling edge triggered).
CP/$\overline{RL2}$	Capture/Reload select. CP/$\overline{RL2}$ = 1 causes captures to occur on negative transitions at T2EX if EXEN2 = 1. CP/$\overline{RL2}$ = 0 causes automatic reloads to occur when Timer 2 overflows or negative transitions occur at T2EX when EXEN2 = 1. When either RCLK or TCLK = 1, this bit is ignored and the timer is forced to auto-reload on Timer 2 overflow.

Table 3a. AUXR: Auxiliary Register

AUXR — Address = 8EH — Reset Value = XXX00XX0B

Not Bit Addressable

Bit	7	6	5	4	3	2	1	0
	–	–	–	WDIDLE	DISRTO	–	–	DISALE

–: Reserved for future expansion

DISALE: Disable/Enable ALE

DISALE	Operating Mode
0	ALE is emitted at a constant rate of 1/6 the oscillator frequency
1	ALE is active only during a MOVX or MOVC instruction

DISRTO: Disable/Enable Reset out

DISRTO	
0	Reset pin is driven High after WDT times out
1	Reset pin is input only

WDIDLE: Disable/Enable WDT in IDLE mode

WDIDLE	
0	WDT continues to count in IDLE mode
1	WDT halts counting in IDLE mode

ual Data Pointer Registers: To facilitate accessing both ıternal and external data memory, two banks of 16-bit ata Pointer Registers are provided: DP0 at SFR address ıcations 82H-83H and DP1 at 84H-85H. Bit DPS = 0 SFR AUXR1 selects DP0 and DPS = 1 selects DP1. he user should always initialize the DPS bit to the appropriate value before accessing the respective Data Pointer Register.

Power Off Flag: The Power Off Flag (POF) is located at bit 4 (PCON.4) in the PCON SFR. POF is set to "1" during power up. It can be set and rest under software control and is not affected by reset.

ıble 3b. AUXR1: Auxiliary Register 1

AUXR1 — Address = A2H — Reset Value = XXXXXXX0B

Not Bit Addressable

Bit	7	6	5	4	3	2	1	0
	–	–	–	–	–	–	–	DPS

-: Reserved for future expansion

)PS: Data Pointer Register Select

DPS	
0	Selects DPTR Registers DP0L, DP0H
1	Selects DPTR Registers DP1L, DP1H

Memory Organization

MCS-51 devices have a separate address space for Program and Data Memory. Up to 64K bytes each of external Program and Data Memory can be addressed.

Program Memory

If the $\overline{EA}$ pin is connected to GND, all program fetches are directed to external memory.

On the AT89S52, if $\overline{EA}$ is connected to V_{CC}, program fetches to addresses 0000H through 1FFFH are directed to internal memory and fetches to addresses 2000H through FFFFH are to external memory.

Data Memory

The AT89S52 implements 256 bytes of on-chip RAM. The upper 128 bytes occupy a parallel address space to the Special Function Registers. This means that the upper 128 bytes have the same addresses as the SFR space but are physically separate from SFR space.

When an instruction accesses an internal location above address 7FH, the address mode used in the instruction specifies whether the CPU accesses the upper 128 bytes of RAM or the SFR space. Instructions which use direct addressing access of the SFR space.

For example, the following direct addressing instruction accesses the SFR at location 0A0H (which is P2).

```
MOV 0A0H, #data
```

Instructions that use indirect addressing access the upper 128 bytes of RAM. For example, the following indirect addressing instruction, where R0 contains 0A0H, accesses the data byte at address 0A0H, rather than P2 (whose address is 0A0H).

```
MOV @R0, #data
```

Note that stack operations are examples of indirect addressing, so the upper 128 bytes of data RAM are available as stack space.

Watchdog Timer (One-time Enabled with Reset-out)

The WDT is intended as a recovery method in situations where the CPU may be subjected to software upsets. The WDT consists of a 13-bit counter and the Watchdog Timer Reset (WDTRST) SFR. The WDT is defaulted to disable from exiting reset. To enable the WDT, a user must write 01EH and 0E1H in sequence to the WDTRST register (SFR location 0A6H). When the WDT is enabled, it will increment every machine cycle while the oscillator is running. The WDT timeout period is dependent on the external clock frequency. There is no way to disable the WDT except through reset (either hardware reset or WDT overflow reset). When WDT overflows, it will drive an output RESET HIGH pulse at the RST pin.

Using the WDT

To enable the WDT, a user must write 01EH and 0E1H in sequence to the WDTRST register (SFR location 0A6H). When the WDT is enabled, the user needs to service it by writing 01EH and 0E1H to WDTRST to avoid a WDT overflow. The 13-bit counter overflows when it reaches 8191 (1FFFH), and this will reset the device. When the WDT is enabled, it will increment every machine cycle while the oscillator is running. This means the user must reset the WDT at least every 8191 machine cycles. To reset the WDT the user must write 01EH and 0E1H to WDTRST. WDTRST is a write-only register. The WDT counter cannot be read or written. When WDT overflows, it will generate an output RESET pulse at the RST pin. The RESET pulse duration is 96xTOSC, where TOSC=1/FOSC. To make the best use of the WDT, it should be serviced in those sections of code that will periodically be executed within the time required to prevent a WDT reset.

WDT During Power-down and Idle

In Power-down mode the oscillator stops, which means the WDT also stops. While in Power-down mode, the user does not need to service the WDT. There are two methods of exiting Power-down mode: by a hardware reset or via a level-activated external interrupt which is enabled prior to entering Power-down mode. When Power-down is exited with hardware reset, servicing the WDT should occur as it normally does whenever the AT89S52 is reset. Exiting Power-down with an interrupt is significantly different. The interrupt is held low long enough for the oscillator to stabilize. When the interrupt is brought high, the interrupt is serviced. To prevent the WDT from resetting the device while the interrupt pin is held low, the WDT is not started until the interrupt is pulled high. It is suggested that the WDT be reset during the interrupt service for the interrupt used to exit Power-down mode.

To ensure that the WDT does not overflow within a few states of exiting Power-down, it is best to reset the WDT just before entering Power-down mode.

Before going into the IDLE mode, the WDIDLE bit in SFR AUXR is used to determine whether the WDT continues to count if enabled. The WDT keeps counting during IDLE (WDIDLE bit = 0) as the default state. To prevent the WDT from resetting the AT89S52 while in IDLE mode, the user should always set up a timer that will periodically exit IDLE, service the WDT, and reenter IDLE mode.

With WDIDLE bit enabled, the WDT will stop to count in IDLE mode and resumes the count upon exit from IDLE.

UART

The UART in the AT89S52 operates the same way as the UART in the AT89C51 and AT89C52. For further information on the UART operation, refer to the ATMEL Web site (http://www.atmel.com). From the home page, select 'Products', then '8051-Architecture Flash Microcontroller', then 'Product Overview'.

Timer 0 and 1

Timer 0 and Timer 1 in the AT89S52 operate the same way as Timer 0 and Timer 1 in the AT89C51 and AT89C52. For further information on the timers' operation, refer to the ATMEL Web site (http://www.atmel.com). From the home page, select 'Products', then '8051-Architecture Flash Microcontroller', then 'Product Overview'.

Timer 2

Timer 2 is a 16-bit Timer/Counter that can operate as either a timer or an event counter. The type of operation is selected by bit C/$\overline{T2}$ in the SFR T2CON (shown in Table 2). Timer 2 has three operating modes: capture, auto-reload (up or down counting), and baud rate generator. The modes are selected by bits in T2CON, as shown in Table 3. Timer 2 consists of two 8-bit registers, TH2 and TL2. In the Timer function, the TL2 register is incremented every machine cycle. Since a machine cycle consists of 12 oscillator periods, the count rate is 1/12 of the oscillator frequency.

Table 3. Timer 2 Operating Modes

RCLK +TCLK	CP/$\overline{RL2}$	TR2	MODE
0	0	1	16-bit Auto-reload
0	1	1	16-bit Capture
1	X	1	Baud Rate Generator
X	X	0	(Off)

the Counter function, the register is incremented in sponse to a 1-to-0 transition at its corresponding external iput pin, T2. In this function, the external input is sampled uring S5P2 of every machine cycle. When the samples how a high in one cycle and a low in the next cycle, the ount is incremented. The new count value appears in the gister during S3P1 of the cycle following the one in which ie transition was detected. Since two machine cycles (24 scillator periods) are required to recognize a 1-to-0 transi-on, the maximum count rate is 1/24 of the oscillator fre-uency. To ensure that a given level is sampled at least nce before it changes, the level should be held for at least ne full machine cycle.

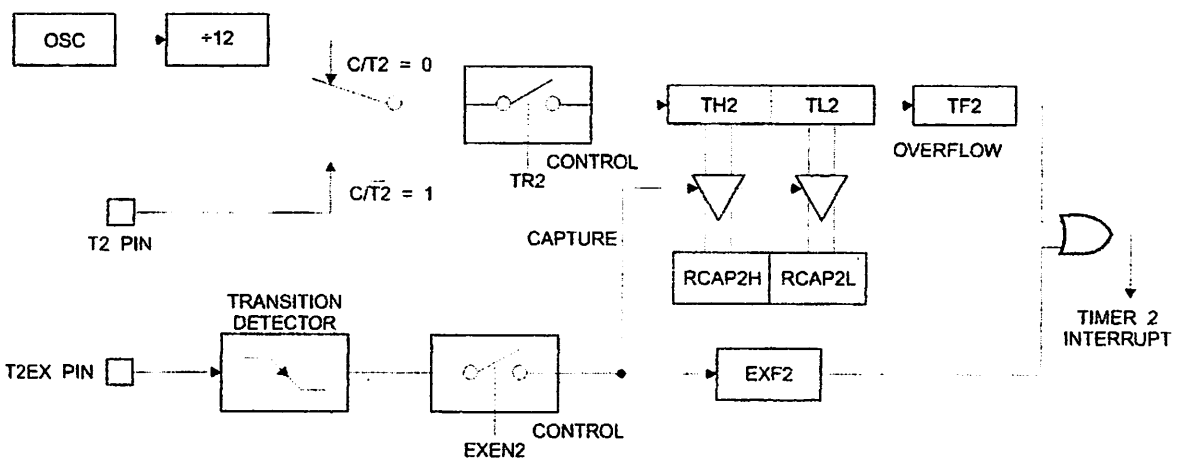
apture Mode

the capture mode, two options are selected by bit XEN2 in T2CON. If EXEN2 = 0, Timer 2 is a 16-bit timer r counter which upon overflow sets bit TF2 in T2CON. This bit can then be used to generate an interrupt. If EXEN2 = 1, Timer 2 performs the same operation, but a 1-to-0 transition at external input T2EX also causes the current value in TH2 and TL2 to be captured into RCAP2H and RCAP2L, respectively. In addition, the transition at T2EX causes bit EXF2 in T2CON to be set. The EXF2 bit, like TF2, can generate an interrupt. The capture mode is illustrated in Figure 5.

Auto-reload (Up or Down Counter)

Timer 2 can be programmed to count up or down when configured in its 16-bit auto-reload mode. This feature is invoked by the DCEN (Down Counter Enable) bit located in the SFR T2MOD (see Table 4). Upon reset, the DCEN bit is set to 0 so that timer 2 will default to count up. When DCEN is set, Timer 2 can count up or down, depending on the value of the T2EX pin.

igure 5. Timer in Capture Mode



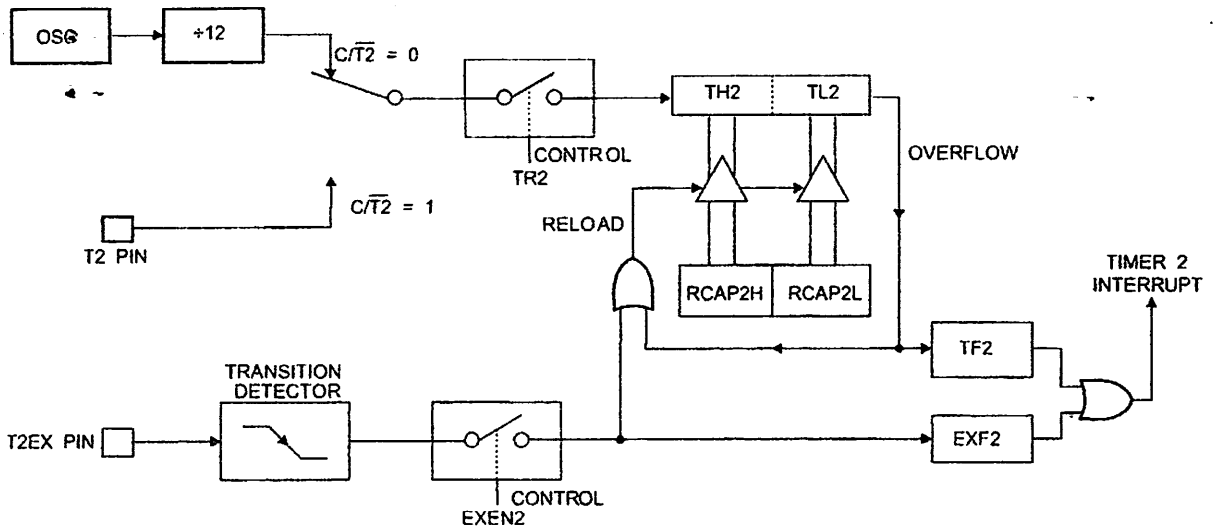
gure 6 shows Timer 2 automatically counting up when CEN=0. In this mode, two options are selected by bit XEN2 in T2CON. If EXEN2 = 0, Timer 2 counts up to FFFFH and then sets the TF2 bit upon overflow. The verflow also causes the timer registers to be reloaded with e 16-bit value in RCAP2H and RCAP2L. The values in mer in Capture ModeRCAP2H and RCAP2L are preset software. If EXEN2 = 1, a 16-bit reload can be triggered ther by an overflow or by a 1-to-0 transition at external put T2EX. This transition also sets the EXF2 bit. Both the F2 and EXF2 bits can generate an interrupt if enabled.

etting the DCEN bit enables Timer 2 to count up or down, shown in Figure 6. In this mode, the T2EX pin controls the direction of the count. A logic 1 at T2EX makes Timer 2 count up. The timer will overflow at 0FFFFH and set the TF2 bit. This overflow also causes the 16-bit value in RCAP2H and RCAP2L to be reloaded into the timer registers, TH2 and TL2, respectively.

A logic 0 at T2EX makes Timer 2 count down. The timer underflows when TH2 and TL2 equal the values stored in RCAP2H and RCAP2L. The underflow sets the TF2 bit and causes 0FFFFH to be reloaded into the timer registers.

The EXF2 bit toggles whenever Timer 2 overflows or underflows and can be used as a 17th bit of resolution. In this operating mode, EXF2 does not flag an interrupt.

gure 6. Timer 2 Auto Reload Mode (DCEN = 0)



ble 4. T2MOD – Timer 2 Mode Control Register

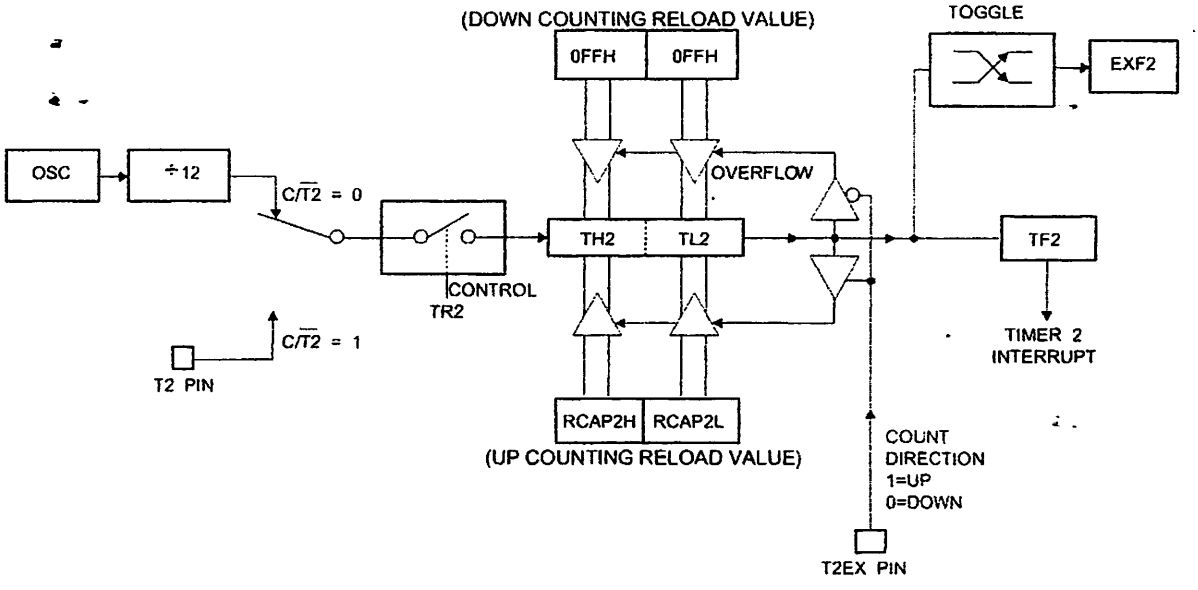
T2MOD Address = 0C9H — Reset Value = XXXX XX00B

Not Bit Addressable

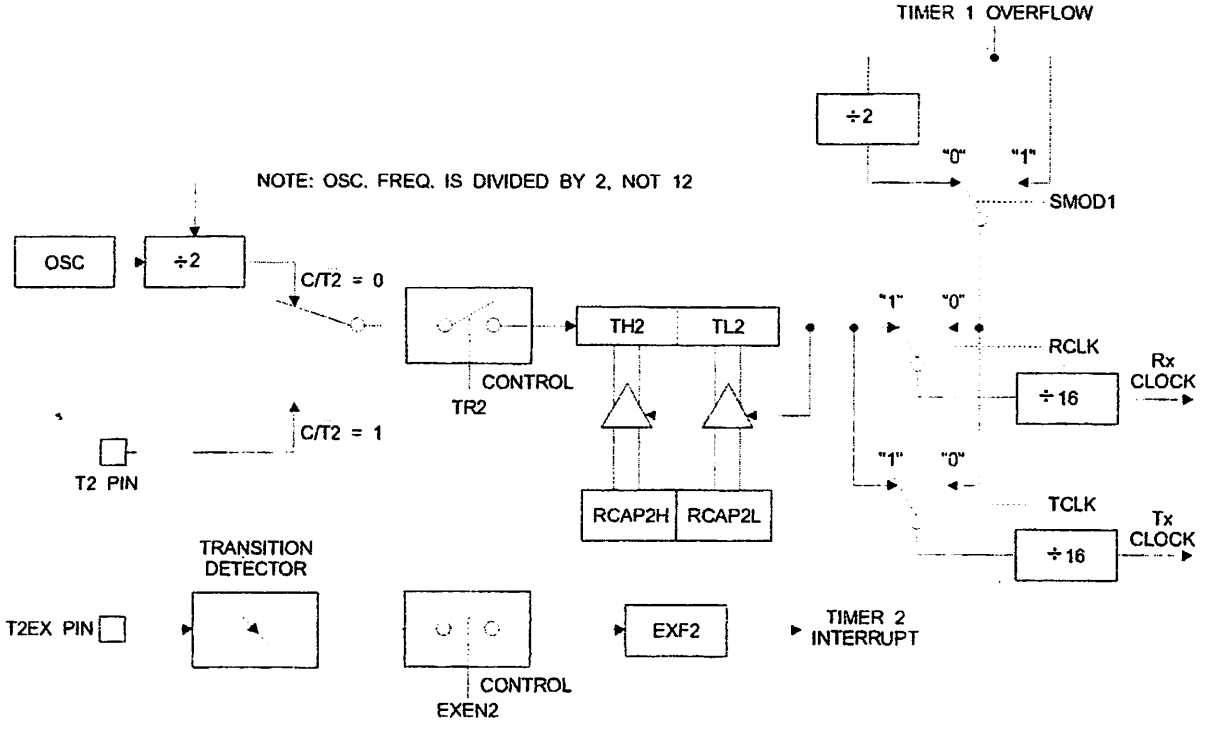
	–	–	–	–	–	–	T2OE	DCEN
Bit	7	6	5	4	3	2	1	0

ymbol	Function
	Not implemented, reserved for future
2OE	Timer 2 Output Enable bit
CEN	When set, this bit allows Timer 2 to be configured as an up/down counter

gure 7. Timer 2 Auto Reload Mode (DCEN = 1)



gure 8. Timer 2 in Baud Rate Generator Mode



Programmable Clock Out

A 50% duty cycle clock can be programmed to come out on P1.0, as shown in Figure 9. This pin, besides being a regular I/O pin, has two alternate functions. It can be programmed to input the external clock for Timer/Counter 2 or to output a 50% duty cycle clock ranging from 61 Hz to 4 MHz at a 16 MHz operating frequency.

To configure the Timer/Counter 2 as a clock generator, bit C/$\overline{T2}$ (T2CON.1) must be cleared and bit T2OE (T2MOD.1) must be set. Bit TR2 (T2CON.2) starts and stops the timer.

The clock-out frequency depends on the oscillator frequency and the reload value of Timer 2 capture registers (RCAP2H, RCAP2L), as shown in the following equation.

$$\text{Clock-Out Frequency} = \frac{\text{Oscillator Frequency}}{4 \times [65536-(\text{RCAP2H,RCAP2L})]}$$

In the clock-out mode, Timer 2 roll-overs will not generate an interrupt. This behavior is similar to when Timer 2 is used as a baud-rate generator. It is possible to use Timer 2 as a baud-rate generator and a clock generator simultaneously. Note, however, that the baud-rate and clock-out frequencies cannot be determined independently from one another since they both use RCAP2H and RCAP2L.

Interrupts

The AT89S52 has a total of six interrupt vectors: two external interrupts ($\overline{INT0}$ and $\overline{INT1}$), three timer interrupts (Timers 0, 1, and 2), and the serial port interrupt. These interrupts are all shown in Figure 10.

Each of these interrupt sources can be individually enabled or disabled by setting or clearing a bit in Special Function Register IE. IE also contains a global disable bit, EA, which disables all interrupts at once.

Note that Table 5 shows that bit position IE.6 is unimplemented. In the AT89S52, bit position IE.5 is also unimplemented. User software should not write 1s to these bit positions, since they may be used in future AT89 products.

Timer 2 interrupt is generated by the logical OR of bits TF2 and EXF2 in register T2CON. Neither of these flags is cleared by hardware when the service routine is vectored to. In fact, the service routine may have to determine whether it was TF2 or EXF2 that generated the interrupt, and that bit will have to be cleared in software.

The Timer 0 and Timer 1 flags, TF0 and TF1, are set at S5P2 of the cycle in which the timers overflow. The values are then polled by the circuitry in the next cycle. However, the Timer 2 flag, TF2, is set at S2P2 and is polled in the same cycle in which the timer overflows.

Table 5. Interrupt Enable (IE) Register

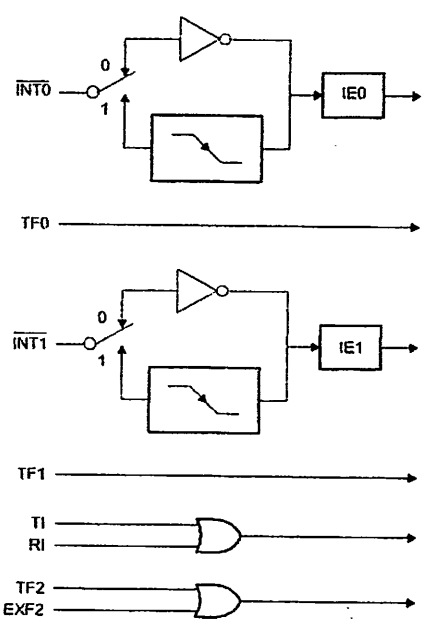
(MSB)							(LSB)
EA	–	ET2	ES	ET1	EX1	ET0	EX0

Enable Bit = 1 enables the interrupt.

Enable Bit = 0 disables the interrupt.

Symbol	Position	Function
EA	IE.7	Disables all interrupts. If EA = 0, no interrupt is acknowledged. If EA = 1, each interrupt source is individually enabled or disabled by setting or clearing its enable bit.
–	IE.6	Reserved.
ET2	IE.5	Timer 2 interrupt enable bit.
ES	IE.4	Serial Port interrupt enable bit.
ET1	IE.3	Timer 1 interrupt enable bit.
EX1	IE.2	External interrupt 1 enable bit.
ET0	IE.1	Timer 0 interrupt enable bit.
EX0	IE.0	External interrupt 0 enable bit.
User software should never write 1s to unimplemented bits, because they may be used in future AT89 products.		

Figure 10. Interrupt Sources



)scillator Characteristics

TAL1 and XTAL2 are the input and output, respectively, ' an inverting amplifier that can be configured for use as ı on-chip oscillator, as shown in Figure 11. Either a quartz ystal or ceramic resonator may be used. To drive the ɜvice from an external clock source, XTAL2 should be left ıconnected while XTAL1 is driven, as shown in Figure 12. ıere are no requirements on the duty cycle of the external ɔck signal, since the input to the internal clocking circuitry through a divide-by-two flip-flop, but minimum and maxium voltage high and low time specifications must be ɜserved.

lle Mode

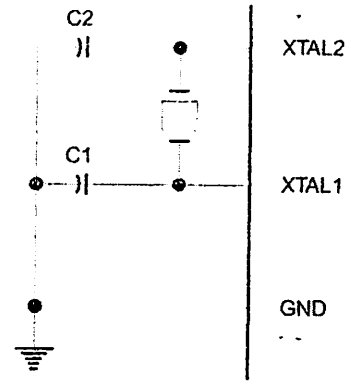
idle mode, the CPU puts itself to sleep while all the on-ip peripherals remain active. The mode is invoked by ftware. The content of the on-chip RAM and all the spe-al functions registers remain unchanged during this ɔde. The idle mode can be terminated by any enabled errupt or by a hardware reset.

ɔte that when idle mode is terminated by a hardware set, the device normally resumes program execution ım where it left off, up to two machine cycles before the ernal reset algorithm takes control. On-chip hardware iibits access to internal RAM in this event, but access to port pins is not inhibited. To eliminate the possibility of unexpected write to a port pin when idle mode is termited by a reset, the instruction following the one that okes idle mode should not write to a port pin or to exter-memory.

ɔwer-down Mode

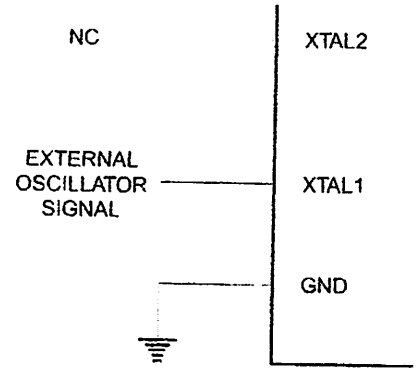
he Power-down mode, the oscillator is stopped, and the truction that invokes Power-down is the last instruction ɜcuted. The on-chip RAM and Special Function Regis-ɜ retain their values until the Power-down mode is termi-ed. Exit from Power-down mode can be initiated either a hardware reset or by an enabled external interrupt. ɜet redefines the SFRs but does not change the on-chip M. The reset should not be activated before V_{CC} is tored to its normal operating level and must be held active long enough to allow the oscillator to restart and stabilize.

Figure 11. Oscillator Connections



Note: C1, C2 = 30 pF ± 10 pF for Crystals
= 40 pF ± 10 pF for Ceramic Resonators

Figure 12. External Clock Drive Configuration



ıle 6. Status of External Pins During Idle and Power-down Modes

ɔde	Program Memory	ALE	$\overline{PSEN}$	PORT0	PORT1	PORT2	PORT3
e	Internal	1	1	Data	Data	Data	Data
e	External	1	1	Float	Data	Address	Data
wer-down	Internal	0	0	Data	Data	Data	Data
wer-down	External	0	0	Float	Data	Data	Data

'rogram Memory Lock Bits

he AT89S52 has three lock bits that can be left unpro-rammed (U) or can be programmed (P) to obtain the addi-)nal features listed in the following table.

able 7. Lock Bit Protection Modes

Program Lock Bits				
	LB1	LB2	LB3	Protection Type
1	U	U	U	No program lock features
2	P	U	U	MOVC instructions executed from external program memory are disabled from fetching code bytes from internal memory, $\overline{EA}$ is sampled and latched on reset, and further programming of the Flash memory is disabled
3	P	P	U	Same as mode 2, but verify is also disabled
4	P	P	P	Same as mode 3, but external execution is also disabled

hen lock bit 1 is programmed, the logic level at the $\overline{EA}$ pin sampled and latched during reset. If the device is pow-ed up without a reset, the latch initializes to a random lue and holds that value until reset is activated. The ched value of $\overline{EA}$ must agree with the current logic level that pin in order for the device to function properly.

rogramming the Flash – Parallel Mode

e AT89S52 is shipped with the on-chip Flash memory ay ready to be programmed. The programming interface eds a high-voltage (12-volt) program enable signal and compatible with conventional third-party Flash or ROM programmers.

e AT89S52 code memory array is programmed byte-by-e.

)gramming Algorithm: Before programming the 39S52, the address, data, and control signals should be up according to the Flash programming mode table and ures 13 and 14. To program the AT89S52, take the fol-ing steps:

Input the desired memory location on the address lines.

Input the appropriate data byte on the data lines.

Activate the correct combination of control signals.

Raise $\overline{EA}/V_{PP}$ to 12V.

Pulse ALE/$\overline{PROG}$ once to program a byte in the Flash array or the lock bits. The byte-write cycle is self-timed and typically takes no more than 50 µs.

Repeat steps 1 through 5, changing the address and data for the entire array or until the end of the object file is reached.

$\overline{Data}$ Polling: The AT89S52 features $\overline{Data}$ Polling to indicate the end of a byte write cycle. During a write cycle, an attempted read of the last byte written will result in the complement of the written data on P0.7. Once the write cycle has been completed, true data is valid on all outputs, and the next cycle may begin. $\overline{Data}$ Polling may begin any time after a write cycle has been initiated.

Ready/$\overline{Busy}$: The progress of byte programming can also be monitored by the RDY/$\overline{BSY}$ output signal. P3.0 is pulled low after ALE goes high during programming to indicate $\overline{BUSY}$. P3.0 is pulled high again when programming is done to indicate READY.

Program Verify: If lock bits LB1 and LB2 have not been programmed, the programmed code data can be read back via the address and data lines for verification. The status of the individual lock bits can be verified directly by reading them back.

Reading the Signature Bytes: The signature bytes are read by the same procedure as a normal verification of locations 000H, 100H, and 200H, except that P3.6 and P3.7 must be pulled to a logic low. The values returned are as follows.

(000H) = 1EH indicates manufactured by Atmel
(100H) = 52H indicates 89S52
(200H) = 06H

Chip Erase: In the parallel programming mode, a chip erase operation is initiated by using the proper combination of control signals and by pulsing ALE/$\overline{PROG}$ low for a duration of 200 ns - 500 ns.

In the serial programming mode, a chip erase operation is initiated by issuing the Chip Erase instruction. In this mode, chip erase is self-timed and takes about 500 ms.

During chip erase, a serial read from any address location will return 00H at the data output.

Programming the Flash – Serial Mode

The Code memory array can be programmed using the serial ISP interface while RST is pulled to V_{CC}. The serial interface consists of pins SCK, MOSI (input) and MISO (output). After RST is set high, the Programming Enable instruction needs to be executed first before other operations can be executed. Before a reprogramming sequence can occur, a Chip Erase operation is required.

The Chip Erase operation turns the content of every memory location in the Code array into FFH.

Either an external system clock can be supplied at pin XTAL1 or a crystal needs to be connected across pins XTAL1 and XTAL2. The maximum serial clock (SCK)

equency should be less than 1/16 of the crystal frequency. With a 33 MHz oscillator clock, the maximum SCK equency is 2 MHz.

erial Programming Algorithm

program and verify the AT89S52 in the serial programming mode, the following sequence is recommended:

Power-up sequence:

Apply power between VCC and GND pins.

Set RST pin to "H".

If a crystal is not connected across pins XTAL1 and XTAL2, apply a 3 MHz to 33 MHz clock to XTAL1 pin and wait for at least 10 milliseconds.

Enable serial programming by sending the Programming Enable serial instruction to pin MOSI/P1.5. The frequency of the shift clock supplied at pin SCK/P1.7 needs to be less than the CPU clock at XTAL1 divided by 16.

The Code array is programmed one byte at a time by supplying the address and data together with the appropriate Write instruction. The write cycle is self-timed and typically takes less than 1 ms at 5V.

4. Any memory location can be verified by using the Read instruction which returns the content at the selected address at serial output MISO/P1.6.
5. At the end of a programming session, RST can be set low to commence normal device operation.

Power-off sequence (if needed):

Set XTAL1 to "L" (if a crystal is not used).

Set RST to "L".

Turn V_{CC} power off.

$\overline{\text{Data}}$ Polling: The $\overline{\text{Data}}$ Polling feature is also available in the serial mode. In this mode, during a write cycle an attempted read of the last byte written will result in the complement of the MSB of the serial output byte on MISO.

Serial Programming Instruction Set

The Instruction Set for Serial Programming follows a 4-byte protocol and is shown in Table 10.

Programming Interface – Parallel Mode

Every code byte in the Flash array can be programmed by using the appropriate combination of control signals. The write operation cycle is self-timed and once initiated, will automatically time itself to completion.

All major programming vendors offer worldwide support for the Atmel microcontroller series. Please contact your local programming vendor for the appropriate software revision.

Table 8. Flash Programming Modes

Mode	V_{CC}	RST	$\overline{PSEN}$	ALE/ $\overline{PROG}$	$\overline{EA}$/ V_{PP}	P2.6	P2.7	P3.3	P3.6	P3.7	P0.7-0 Data	P2.4-0 Address	P1.7-0 Address
Write Code Data	5V	H	L	(2)	12V	L	H	H	H	H	D_{IN}	A12-8	A7-0
Read Code Data	5V	H	L	H	H	L	L	L	H	H	D_{OUT}	A12-8	A7-0
Write Lock Bit 1	5V	H	L	(3)	12V	H	H	H	H	H	X	X	X
Write Lock Bit 2	5V	H	L	(3)	12V	H	H	H	L	L	X	X	X
Write Lock Bit 3	5V	H	L	(3)	12V	H	L	H	H	L	X	X	X
Read Lock Bits 1, 2, 3	5V	H	L	H	H	H	H	L	H	L	P0.2, P0.3, P0.4	X	X
Chip Erase	5V	H	L	(1)	12V	H	L	H	L	L	X	X	X
Read Atmel ID	5V	H	L	H	H	L	L	L	L	L	1EH	X 0000	00H
Read Device ID	5V	H	L	H	H	L	L	L	L	L	52H	X 0001	00H
Read Device ID	5V	H	L	H	H	L	L	L	L	L	06H	X 0010	00H

Notes:
1. Each $\overline{PROG}$ pulse is 200 ns - 500 ns for Chip Erase.
2. Each $\overline{PROG}$ pulse is 200 ns - 500 ns for Write Code Data.
3. Each $\overline{PROG}$ pulse is 200 ns - 500 ns for Write Lock Bits.
4. RDY/$\overline{BSY}$ signal is output on P3.0 during programming.
5. X = don't care.

Figure 13. Programming the Flash Memory (Parallel Mode)

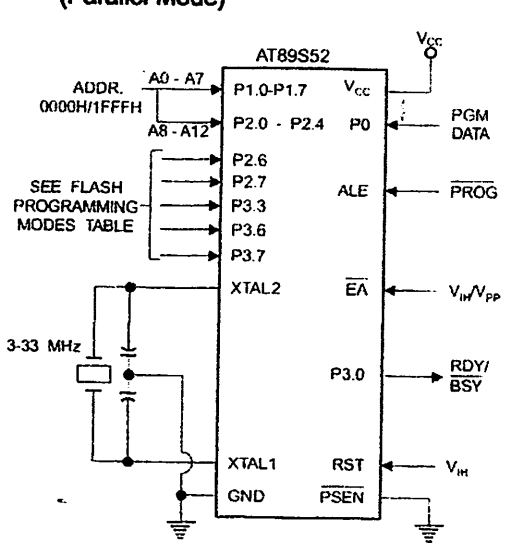
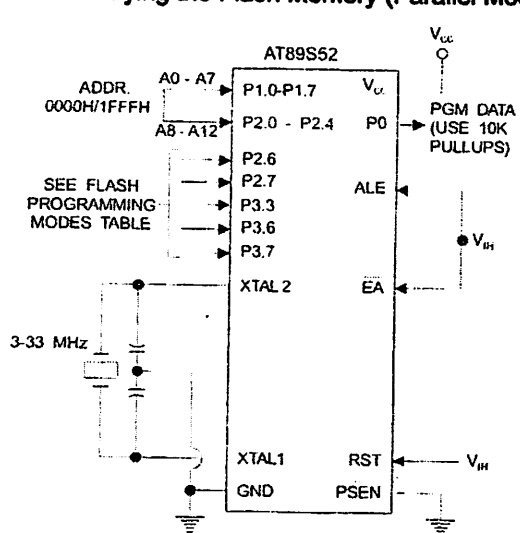


Figure 14. Verifying the Flash Memory (Parallel Mode)

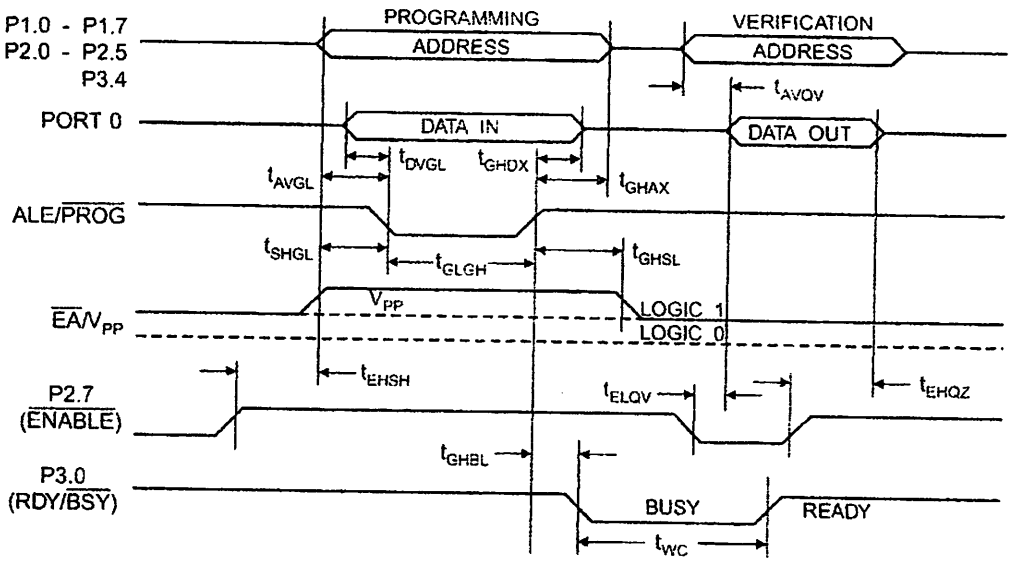


lash Programming and Verification Characteristics (Parallel Mode)

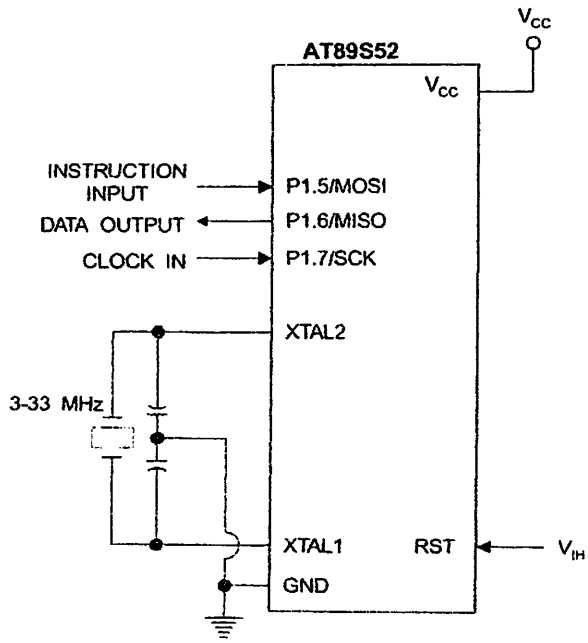
$_A$ = 20°C to 30°C, V_{CC} = 4.5 to 5.5V

Symbol	Parameter	Min	Max	Units
$/_{PP}$	Programming Supply Voltage	11.5	12.5	V
PP	Programming Supply Current		10	mA
CC	V_{CC} Supply Current		30	mA
$1/t_{CLCL}$	Oscillator Frequency	3	33	MHz
AVGL	Address Setup to $\overline{PROG}$ Low	$48t_{CLCL}$		
GHAX	Address Hold After $\overline{PROG}$	$48t_{CLCL}$		
DVGL	Data Setup to $\overline{PROG}$ Low	$48t_{CLCL}$		
GHDX	Data Hold After $\overline{PROG}$	$48t_{CLCL}$		
EHSH	P2.7 ($\overline{ENABLE}$) High to V_{PP}	$48t_{CLCL}$		
SHGL	V_{PP} Setup to $\overline{PROG}$ Low	10		µs
GHSL	V_{PP} Hold After $\overline{PROG}$	10		µs
GLGH	$\overline{PROG}$ Width	0.2	1	µs
AVQV	Address to Data Valid		$48t_{CLCL}$	
ELQV	$\overline{ENABLE}$ Low to Data Valid		$48t_{CLCL}$	
EHQZ	Data Float After $\overline{ENABLE}$	0	$48t_{CLCL}$	
GHBL	$\overline{PROG}$ High to $\overline{BUSY}$ Low		1.0	µs
WC	Byte Write Cycle Time		50	µs

jure 15. Flash Programming and Verification Waveforms – Parallel Mode

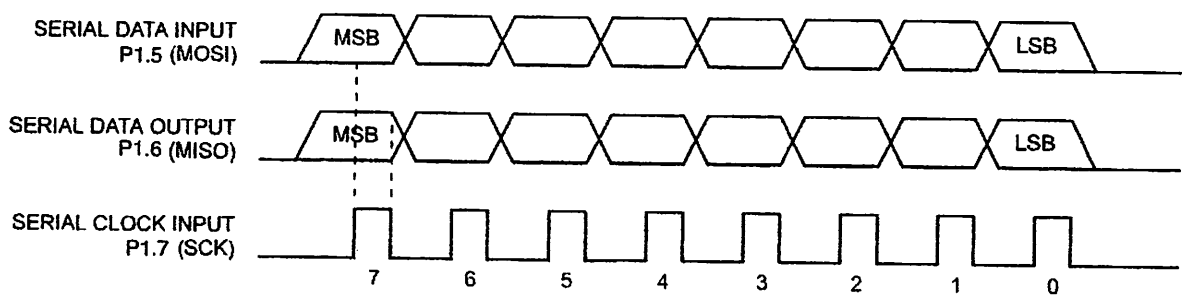


igure 16. Flash Memory Serial Downloading



lash Programming and Verification Waveforms – Serial Mode

gure 17. Serial Programming Waveforms



able 9. Serial Programming Instruction Set

Instruction	Instruction Format Byte 1	Byte 2	Byte 3	Byte 4	Operation
Programming Enable	1010 1100	0101 0011	xxxx xxxx	xxxx xxxx 0110 1001 (Output)	Enable Serial Programming while RST is high
Chip Erase	1010 1100	100x xxxx	xxxx xxxx	xxxx xxxx	Chip Erase Flash memory array
Read Program Memory (Byte Mode)	0010 0000	xxx A12 A11 A10 A9 A8	A7 A6 A5 A4 A3 A2 A1 A0	D7 D6 D5 D4 D3-D0	Read data from Program memory in the byte mode
Write Program Memory (Byte Mode)	0100 0000	xxx A12 A11 A10 A9 A8	A7 A6 A5 A4 A3 A2 A1 A0	D7 D6 D5 D4 D3-D0	Write data to Program memory in the byte mode
Write Lock Bits[2]	1010 1100	1110 00 B1 B2	xxxx xxxx	xxxx xxxx	Write Lock bits. See Note (2).
Read Lock Bits	0010 0100	xxxx xxxx	xxxx xxxx	xx LB3 LB2 LB1 xx	Read back current status of the lock bits (a programmed lock bit reads back as a '1')
Read Signature Bytes[1]	0010 1000	xxx A5 A4 A3 A2 A1 A0	xxx xxxx	Signature Byte	Read Signature Byte
Read Program Memory (Page Mode)	0011 0000	xxx A12 A11 A10 A9 A8	Byte 0	Byte 1... Byte 255	Read data from Program memory in the Page Mode (256 bytes)
Write Program Memory (Page Mode)	0101 0000	xxx A12 A11 A10 A9 A8	Byte 0	Byte 1... Byte 255	Write data to Program memory in the Page Mode (256 bytes)

otes: 1. The signature bytes are not readable in Lock Bit Modes 3 and 4.

2. B1 = 0, B2 = 0 —> Mode 1, no lock protection
   B1 = 0, B2 = 1 —> Mode 2, lock bit 1 activated
   B1 = 1, B2 = 0 —> Mode 3, lock bit 2 activated
   B1 = 1, B1 = 1 —> Mode 4, lock bit 3 activated

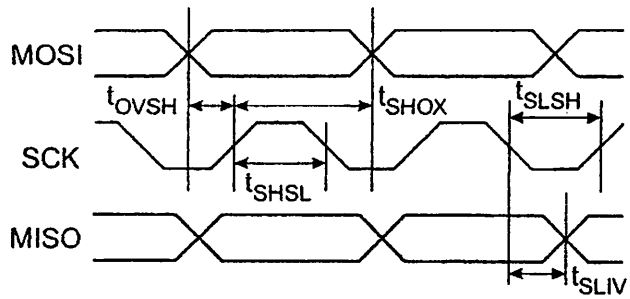
   } Each of the lock bits needs to be activated sequentially before Mode 4 can be executed.

ter Reset signal is high, SCK should be low for at least 64 stem clocks before it goes high to clock in the enable ta bytes. No pulsing of Reset signal is necessary. SCK ould be no faster than 1/16 of the system clock at AL1.

For Page Read/Write, the data always starts from byte 0 to 255. After the command byte and upper address byte are latched, each byte thereafter is treated as data until all 256 bytes are shifted in/out. Then the next instruction will be ready to be decoded.

erial Programming Characteristics

igure 18. Serial Programming Timing



able 10. Serial Programming Characteristics, T_A = -40° C to 85° C, V_{CC} = 4.0 - 5.5V (Unless otherwise noted)

Symbol	Parameter	Min	Typ	Max	Units
$1/t_{CLCL}$	Oscillator Frequency	0		33	MHz
t_{CLCL}	Oscillator Period	30			ns
t_{SHSL}	SCK Pulse Width High	$2\ t_{CLCL}$			ns
t_{SLSH}	SCK Pulse Width Low	$2\ t_{CLCL}$			ns
t_{OVSH}	MOSI Setup to SCK High	t_{CLCL}			ns
t_{SHOX}	MOSI Hold after SCK High	$2\ t_{CLCL}$			ns
t_{SLIV}	SCK Low to MISO Valid	10	16	32	ns
t_{ERASE}	Chip Erase Instruction Cycle Time			500	ms
t_{SWC}	Serial Byte Write Cycle Time			$64\ t_{CLCL} + 400$	µs

Absolute Maximum Ratings*

Operating Temperature	-55°C to +125°C
Storage Temperature	-65°C to +150°C
Voltage on Any Pin with Respect to Ground	-1.0V to +7.0V
Maximum Operating Voltage	6.6V
DC Output Current	15.0 mA

*NOTICE: Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC Characteristics

The values shown in this table are valid for T_A = -40°C to 85°C and V_{CC} = 4.0V to 5.5V, unless otherwise noted.

Symbol	Parameter	Condition	Min	Max	Units
V_{IL}	Input Low Voltage	(Except $\overline{EA}$)	-0.5	0.2 V_{CC}-0.1	V
V_{IL1}	Input Low Voltage ($\overline{EA}$)		-0.5	0.2 V_{CC}-0.3	V
V_{IH}	Input High Voltage	(Except XTAL1, RST)	0.2 V_{CC}+0.9	V_{CC}+0.5	V
V_{IH1}	Input High Voltage	(XTAL1, RST)	0.7 V_{CC}	V_{CC}+0.5	V
V_{OL}	Output Low Voltage[1] (Ports 1,2,3)	I_{OL} = 1.6 mA		0.45	V
V_{OL1}	Output Low Voltage[1] (Port 0, ALE, $\overline{PSEN}$)	I_{OL} = 3.2 mA		0.45	V
V_{OH}	Output High Voltage (Ports 1,2,3, ALE, $\overline{PSEN}$)	I_{OH} = -60 µA, V_{CC} = 5V ±10%	2.4		V
		I_{OH} = -25 µA	0.75 V_{CC}		V
		I_{OH} = -10 µA	0.9 V_{CC}		V
V_{OH1}	Output High Voltage (Port 0 in External Bus Mode)	I_{OH} = -800 µA, V_{CC} = 5V ±10%	2.4		V
		I_{OH} = -300 µA	0.75 V_{CC}		V
		I_{OH} = -80 µA	0.9 V_{CC}		V
I_{IL}	Logical 0 Input Current (Ports 1,2,3)	V_{IN} = 0.45V		-50	µA
I_{TL}	Logical 1 to 0 Transition Current (Ports 1,2,3)	V_{IN} = 2V, V_{CC} = 5V ±10%		-650	µA
I_{LI}	Input Leakage Current (Port 0, $\overline{EA}$)	0.45 < V_{IN} < V_{CC}		±10	µA
R_{RST}	Reset Pulldown Resistor		10	30	KΩ
C_{IO}	Pin Capacitance	Test Freq. = 1 MHz, T_A = 25°C		10	pF
I_{CC}	Power Supply Current	Active Mode, 12 MHz		25	mA
		Idle Mode, 12 MHz		6.5	mA
	Power-down Mode[1]	V_{CC} = 5.5V		50	µA

Notes:
1. Under steady state (non-transient) conditions, I_{OL} must be externally limited as follows:
   Maximum I_{OL} per port pin: 10 mA
   Maximum I_{OL} per 8-bit port:
   Port 0: 26 mA Ports 1, 2, 3: 15 mA
   Maximum total I_{OL} for all output pins: 71 mA
   If I_{OL} exceeds the test condition, V_{OL} may exceed the related specification. Pins are not guaranteed to sink current greater than the listed test conditions.
2. Minimum V_{CC} for Power-down is 2V.

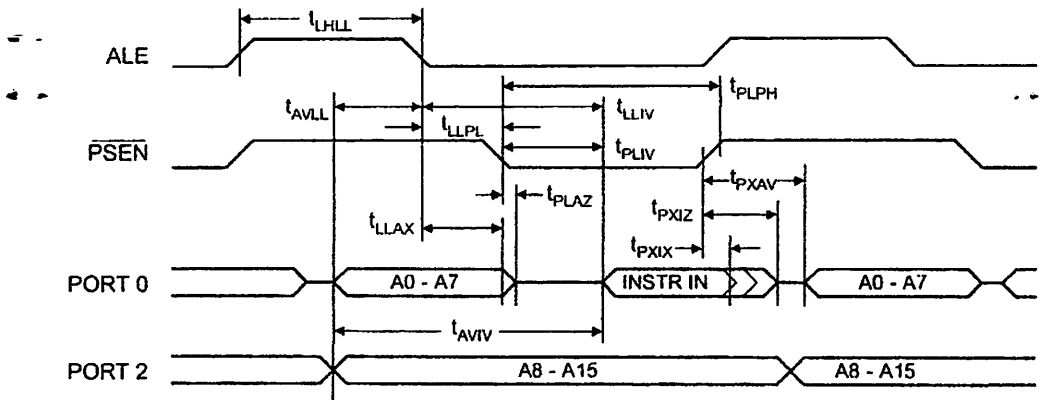
C Characteristics

ıder operating conditions, load capacitance for Port 0, ALE/$\overline{PROG}$, and $\overline{PSEN}$ = 100 pF; load capacitance for all other ıtputs = 80 pF.

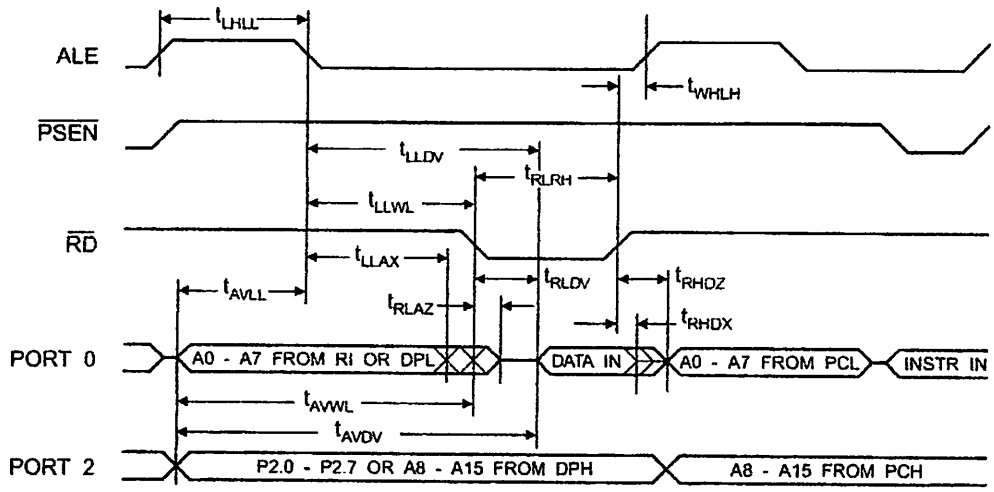
xternal Program and Data Memory Characteristics

ymbol	Parameter	12 MHz Oscillator		Variable Oscillator		Units
		Min	Max	Min	Max	
$1/t_{CLCL}$	Oscillator Frequency			0	33	MHz
LHLL	ALE Pulse Width	127		$2t_{CLCL}$-40		ns
AVLL	Address Valid to ALE Low	43		t_{CLCL}-25		ns
LAX	Address Hold After ALE Low	48		t_{CLCL}-25		ns
LIV	ALE Low to Valid Instruction In		233		$4t_{CLCL}$-65	ns
LPL	ALE Low to $\overline{PSEN}$ Low	43		t_{CLCL}-25		ns
PLPH	$\overline{PSEN}$ Pulse Width	205		$3t_{CLCL}$-45		ns
PLIV	$\overline{PSEN}$ Low to Valid Instruction In		145		$3t_{CLCL}$-60	ns
PXIX	Input Instruction Hold After $\overline{PSEN}$	0		0		ns
PXIZ	Input Instruction Float After $\overline{PSEN}$		59		t_{CLCL}-25	ns
PXAV	$\overline{PSEN}$ to Address Valid	75		t_{CLCL}-8		ns
AVIV	Address to Valid Instruction In		312		$5t_{CLCL}$-80	ns
PLAZ	$\overline{PSEN}$ Low to Address Float		10		10	ns
RLRH	$\overline{RD}$ Pulse Width	400		$6t_{CLCL}$-100		ns
WLWH	$\overline{WR}$ Pulse Width	400		$6t_{CLCL}$-100		ns
RLDV	$\overline{RD}$ Low to Valid Data In		252		$5t_{CLCL}$-90	ns
RHDX	Data Hold After $\overline{RD}$	0		0		ns
RHDZ	Data Float After $\overline{RD}$		97		$2t_{CLCL}$-28	ns
LDV	ALE Low to Valid Data In		517		$8t_{CLCL}$-150	ns
AVDV	Address to Valid Data In		585		$9t_{CLCL}$-165	ns
LWL	ALE Low to $\overline{RD}$ or $\overline{WR}$ Low	200	300	$3t_{CLCL}$-50	$3t_{CLCL}$+50	ns
AVWL	Address to $\overline{RD}$ or $\overline{WR}$ Low	203		$4t_{CLCL}$-75		ns
QVWX	Data Valid to $\overline{WR}$ Transition	23		t_{CLCL}-30		ns
QVWH	Data Valid to $\overline{WR}$ High	433		$7t_{CLCL}$-130		ns
WHQX	Data Hold After $\overline{WR}$	33		t_{CLCL}-25		ns
RLAZ	$\overline{RD}$ Low to Address Float		0		0	ns
WHLH	$\overline{RD}$ or $\overline{WR}$ High to ALE High	43	123	t_{CLCL}-25	t_{CLCL}+25	ns

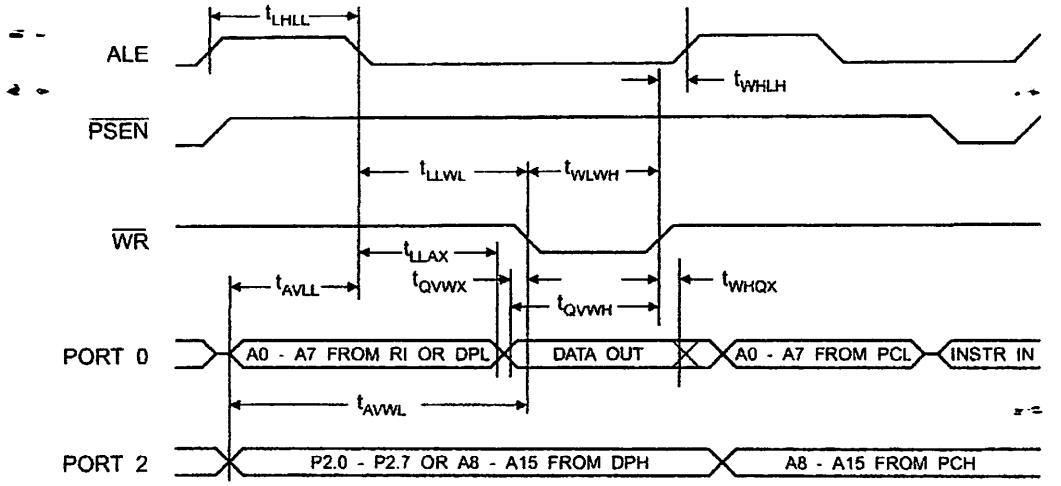
xternal Program Memory Read Cycle



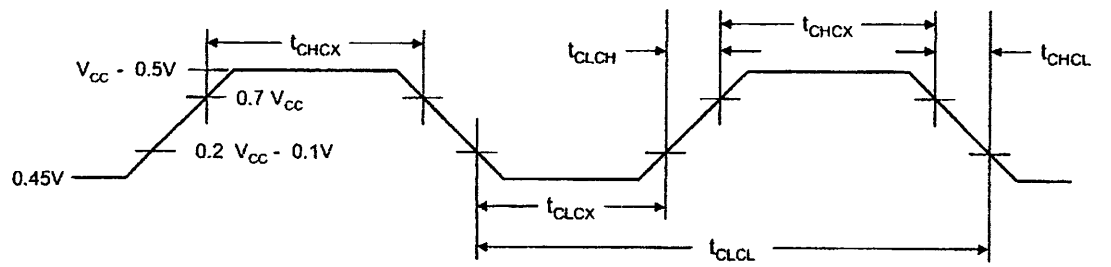
xternal Data Memory Read Cycle



xternal Data Memory Write Cycle



xternal Clock Drive Waveforms



xternal Clock Drive

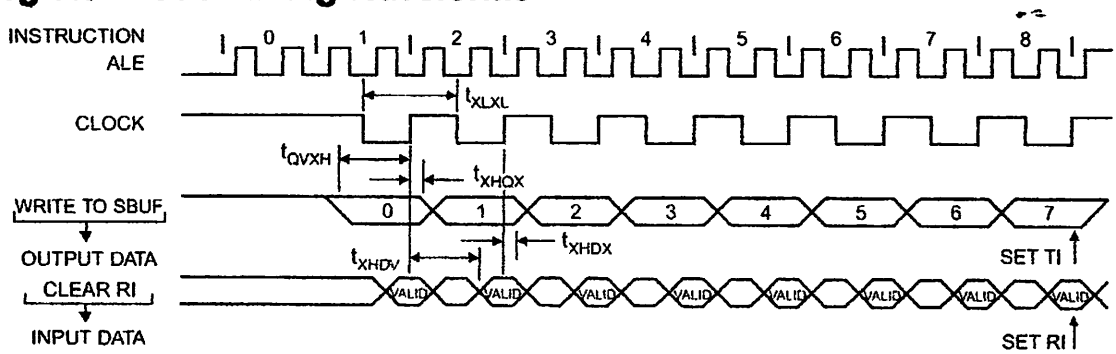
ymbol	Parameter	Min	Max	Units
t_{CLCL}	Oscillator Frequency	0	33	MHz
LCL	Clock Period	30		ns
HCX	High Time	12		ns
LCX	Low Time	12		ns
LCH	Rise Time		5	ns
HCL	Fall Time		5	ns

ierial Port Timing: Shift Register Mode Test Conditions

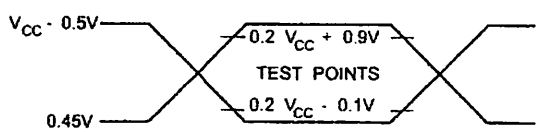
he values in this table are valid for V_{CC} = 4.0V to 5.5V and Load Capacitance = 80 pF.

Symbol	Parameter	12 MHz Osc		Variable Oscillator		Units
		Min	Max	Min	Max	
t_{XLXL}	Serial Port Clock Cycle Time	1.0		$12t_{CLCL}$		µs
t_{QVXH}	Output Data Setup to Clock Rising Edge	700		$10t_{CLCL}$-133		ns
t_{XHQX}	Output Data Hold After Clock Rising Edge	50		$2t_{CLCL}$-80		ns
t_{XHDX}	Input Data Hold After Clock Rising Edge	0		0		ns
t_{XHDV}	Clock Rising Edge to Input Data Valid		700		$10t_{CLCL}$-133	ns

ihift Register Mode Timing Waveforms

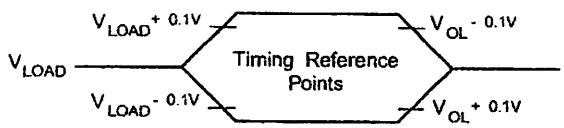


AC Testing Input/Output Waveforms[1]



Note: 1. AC Inputs during testing are driven at V_{CC} - 0.5V for a logic 1 and 0.45V for a logic 0. Timing measurements are made at V_{IH} min. for a logic 1 and V_{IL} max. for a logic 0.

Float Waveforms[1]



Note: 1. For timing purposes, a port pin is no longer floating when a 100 mV change from load voltage occurs. A port pin begins to float when a 100 mV change from the loaded V_{OH}/V_{OL} level occurs.

Ordering Information

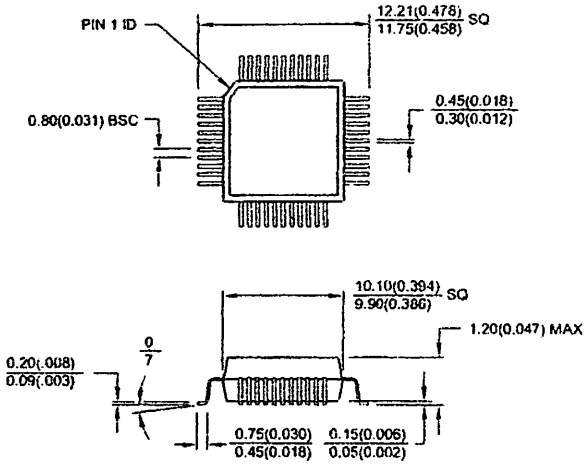
Speed (MHz)	Power Supply	Ordering Code	Package	Operation Range
24	4.0V to 5.5V	AT89S52-24AC AT89S52-24JC AT89S52-24PC	44A 44J 40P6	Commercial (0°C to 70°C)
		AT89S52-24AI AT89S52-24JI AT89S52-24PI	44A 44J 40P6	Industrial (-40°C to 85°C)
33	4.5V to 5.5V	AT89S52-33AC AT89S52-33JC AT89S52-33PC	44A 44J 40P6	Commercial (0°C to 70°C)

= Preliminary Availability

	Package Type
44A	44-lead, Thin Plastic Gull Wing Quad Flatpack (TQFP)
44J	44-lead, Plastic J-leaded Chip Carrier (PLCC)
40P6	40-pin, 0.600" Wide, Plastic Dual Inline Package (PDIP)

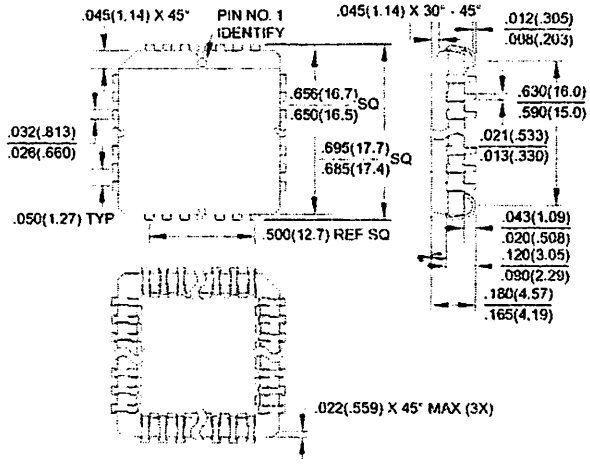
ackaging Information

44A, 44-lead, Thin (1.0 mm) Plastic Gull Wing Quad Flat Package (TQFP)
Dimensions in Millimeters and (Inches)*

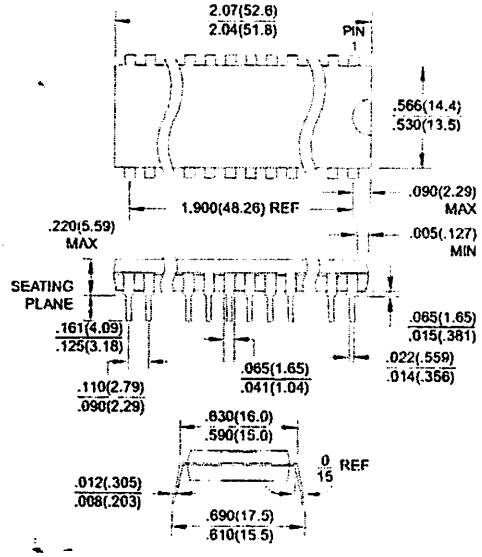


*Controlling dimension: millimeters

44J, 44-lead, Plastic J-leaded Chip Carrier (PLCC)
Dimensions in Inches and (Millimeters)



40P6, 40-pin, 0.600" Wide, Plastic Dual Inline Package (PDIP)
Dimensions in Inches and (Millimeters)
JEDEC STANDARD MS-011 AC



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Rev.1919A-07/01/xM

DALLAS SEMICONDUCTOR

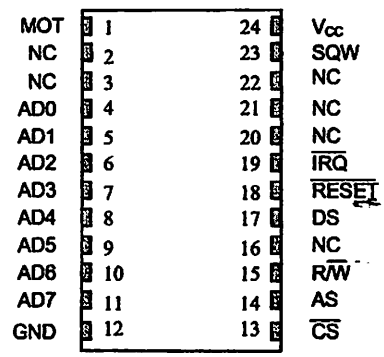
DS12C887
Real Time Clock

www.dalsemi.com

FEATURES

- Drop-in replacement for IBM AT computer clock/calendar
- Pin compatible with the MC146818B and DS1287
- Totally nonvolatile with over 10 years of operation in the absence of power
- Self-contained subsystem includes lithium, quartz, and support circuitry.
- Counts seconds, minutes, hours, days, day of the week, date, month, and year with leap year compensation valid up to 2100
- Binary or BCD representation of time, calendar, and alarm
- 12– or 24–hour clock with AM and PM in 12–hour mode
- Daylight Savings Time option
- Selectable between Motorola and Intel bus timing
- Multiplex bus for pin efficiency
- Interfaced with software as 128 RAM locations
  - 15 bytes of clock and control registers
  - 113 bytes of general purpose RAM
- Programmable square wave output signal
- Bus–compatible interrupt signals (IRQ)
- Three interrupts are separately software maskable and testable
  - Time–of–day alarm once/second to once/day
  - Periodic rates from 122 ms to 500 ms
  - End of clock update cycle
- Century register

PIN ASSIGNMENT



DS12C887 24-Pin
ENCAPSULATED PACKAGE

PIN DESCRIPTION

AD0-AD7	-	Multiplexed Address/Data Bus
NC	-	No Connect
MOT	-	Bus Type Selection
$\overline{CS}$	-	RTC Chip Select Input
AS	-	Address Strobe
R/$\overline{W}$	-	Read/Write Input
DS	-	Data Strobe
$\overline{RESET}$	-	Reset Input
$\overline{IRQ}$	-	Interrupt Request Output
SQW	-	Square Wave Output
V_{CC}	-	+5 Volt Main Supply
GND	-	Ground

DESCRIPTION

The DS12C887 Real Time Clock plus RAM is designed as a direct upgrade replacement for the DS12887 in existing IBM compatible personal computers to add hardware year 2000 compliance. A century byte was added to memory location 50, 32h, as called out by the PC AT specification. A lithium energy source, quartz crystal, and write-protection circuitry are contained within a 24–pin dual in-line package. As such, the DS12C887 is a complete subsystem replacing 16 components in a typical application. The functions include a nonvolatile time-of-day clock, an alarm, a one-hundred-year calendar, programmable interrupt, square wave generator, and 113 bytes of nonvolatile static RAM. The real time clock is distinctive in that time-of-day and memory are maintained even in the absence of power.

)PERATION

'he block diagram in Figure 1 shows the pin connections with the major internal functions of the)S12C887. The following paragraphs describe the function of each pin.

;IGNAL DESCRIPTIONS

;ND, V_{CC} -DC power is provided to the device on these pins. V_{CC} is the +5 volt input. When 5 volts are pplied within normal limits, the device is fully accessible and data can be written and read. When V_{CC} is elow 4.25 volts typical, reads and writes are inhibited. However, the timekeeping function continues naffected by the lower input voltage. As V_{CC} falls below 3 volts typical, the RAM and timekeeper are witched over to an internal lithium energy source. The timekeeping function maintains an accuracy of ±1 ıinute per month at 25°C regardless of the voltage input on the V_{CC} pin.

1OT (Mode Select) – The MOT pin offers the flexibility to choose between two bus types. When onnected to V_{CC}, Motorola bus timing is selected. When connected to GND or left disconnected, Intel us timing is selected. The pin has an internal pull-down resistance of approximately 20KΩ.

QW (Square Wave Output) – The SQW pin can output a signal from one of 13 taps provided by the 5 internal divider stages of the Real Time Clock. The frequency of the SQW pin can be changed by rogramming Register A as shown in Table 1. The SQW signal can be turned on and off using the SQWE it in Register B. The SQW signal is not available when V_{CC} is less than 4.25 volts typical.

.D0-AD7 (Multiplexed Bidirectional Address/Data Bus) – Multiplexed buses save pins because ddress information and data information time share the same signal paths. The addresses are present uring the first portion of the bus cycle and the same pins and signal paths are used for data in the second ortion of the cycle. Address/data multiplexing does not slow the access time of the DS12C887 since the us change from address to data occurs during the internal RAM access time. Addresses must be valid rior to the falling edge of AS/ALE, at which time the DS12C887 latches the address from AD0 to AD6. 'alid write data must be present and held stable during the latter portion of the DS or WR pulses. In a ;ad cycle the DS12C887 outputs 8 bits of data during the latter portion of the DS or RD pulses. The read ycle is terminated and the bus returns to a high impedance state as DS transitions low in the case of lotorola timing or as RD transitions high in the case of Intel timing.

.S (Address Strobe Input) – A positive going address strobe pulse serves to demultiplex the bus. The illing edge of AS/ALE causes the address to be latched within the DS12C887. The next rising edge that :curs on the AS bus will clear the address regardless of whether $\overline{CS}$ is asserted. Access commands ıould be sent in pairs.

'S (Data Strobe or Read Input) – The DS/RD pin has two modes of operation depending on the level f the MOT pin. When the MOT pin is connected to V_{CC}, Motorola bus timing is selected. In this mode 'S is a positive pulse during the latter portion of the bus cycle and is called Data Strobe. During read /cles, DS signifies the time that the DS12C887 is to drive the bidirectional bus. In write cycles the ailing edge of DS causes the DS12C887 to latch the written data. When the MOT pin is connected to ND, Intel bus timing is selected. In this mode the DS pin is called Read(RD). RD identifies the time :riod when the DS12C887 drives the bus with read data. The RD signal is the same definition as the utput Enable (OE) signal on a typical memory.

/$\overline{W}$ (Read/Write Input) – The R/$\overline{W}$ pin also has two modes of operation. When the MOT pin is onnected to V_{CC} for Motorola timing, R/W is at a level which indicates whether the current cycle is a ead or write. A read cycle is indicated with a high level on R/W while DS is high. A write cycle is idicated when R/$\overline{W}$ is low during DS. When the MOT pin is connected to GND for Intel timing, the /$\overline{W}$ signal is an active low signal called WR. In this mode the R/$\overline{W}$ pin has the same meaning as the /rite Enable signal (WE) on generic RAMs.

$\overline{S}$ (Chip Select Input) – The Chip Select signal must be asserted low for a bus cycle in the DS12C887) be accessed. $\overline{CS}$ must be kept in the active state during DS and AS for Motorola timing and during RD nd WR for Intel timing. Bus cycles which take place without asserting $\overline{CS}$ will latch addresses but no ccess will occur. When V_{CC} is below 4.25 volts, the DS12C887 internally inhibits access cycles by ternally disabling the $\overline{CS}$ input. This action protects both the real time clock data and RAM data during ower outages.

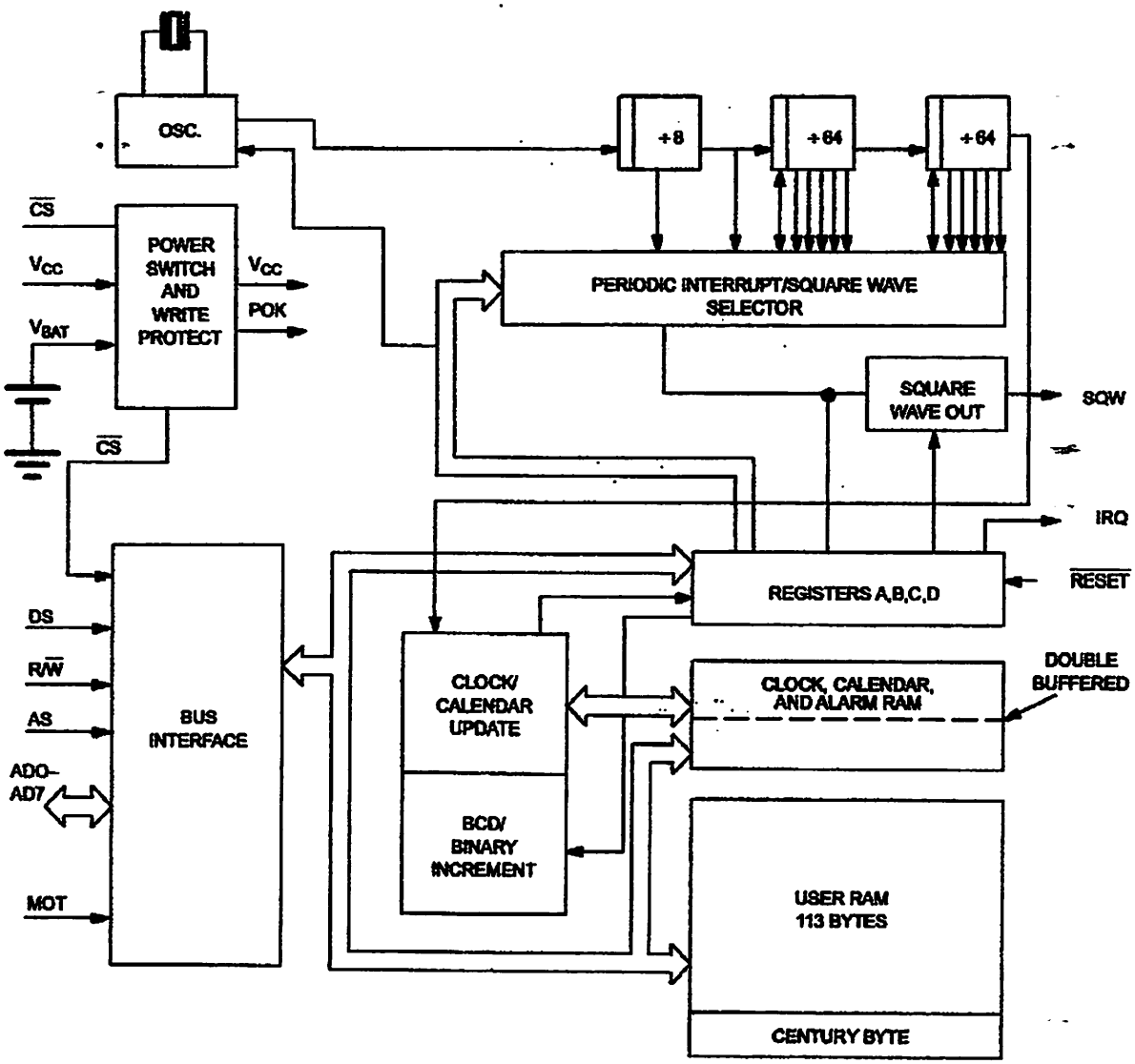
$\overline{RQ}$ (Interrupt Request Output) - The $\overline{IRQ}$ pin is an active low output of the DS12C887 that can be sed as an interrupt input to a processor. The $\overline{IRQ}$ output remains low as long as the status bit causing the nterrupt is present and the corresponding interrupt-enable bit is set. To clear the $\overline{IRQ}$ pin the processor rogram normally reads the C register. The RESET pin also clears pending interrupts. When no interrupt onditions are present, the $\overline{IRQ}$ level is in the high impedance state. Multiple interrupting devices can be onnected to an $\overline{IRQ}$ bus. The IRQ bus is an open drain output and requires an external pull-up resistor.

$\overline{ESET}$ (Reset Input) – The $\overline{RESET}$ pin has no effect on the clock, calendar, or RAM. On power-up the $\overline{ESET}$ pin can be held low for a time in order to allow the power supply to stabilize. The amount of me that $\overline{RESET}$ is held low is dependent on the application. However, if $\overline{RESET}$ is used on power–up, ie time $\overline{RESET}$ is low should exceed 200 ms to make sure that the internal timer that controls the)S12C887 on power-up has timed out. When $\overline{RESET}$ is low and V_{CC} is above 4.25 volts, the following ccurs:

A. Periodic Interrupt Enable (PEI) bit is cleared to zero.
B. Alarm Interrupt Enable (AIE) bit is cleared to zero.
C. Update Ended Interrupt Flag (UF) bit is cleared to zero.
D. Interrupt Request Status Flag (IRQF) bit is cleared to zero.
E. Periodic Interrupt Flag (PF) bit is cleared to zero.
F. The device is not accessible until $\overline{RESET}$ is returned high.
G. Alarm Interrupt Flag (AF) bit is cleared to zero.
H. $\overline{IRQ}$ pin is in the high impedance state.
I. Square Wave Output Enable (SQWE) bit is cleared to zero.
J. Update Ended Interrupt Enable (UIE) is cleared to zero.

a typical application $\overline{RESET}$ can be connected to V_{CC} . This connection will allow the DS12C887 to) in and out of power fail without affecting any of the control registers.

DS12C887 BLOCK DIAGRAM Figure 1



OWER-DOWN/POWER-UP CONSIDERATIONS

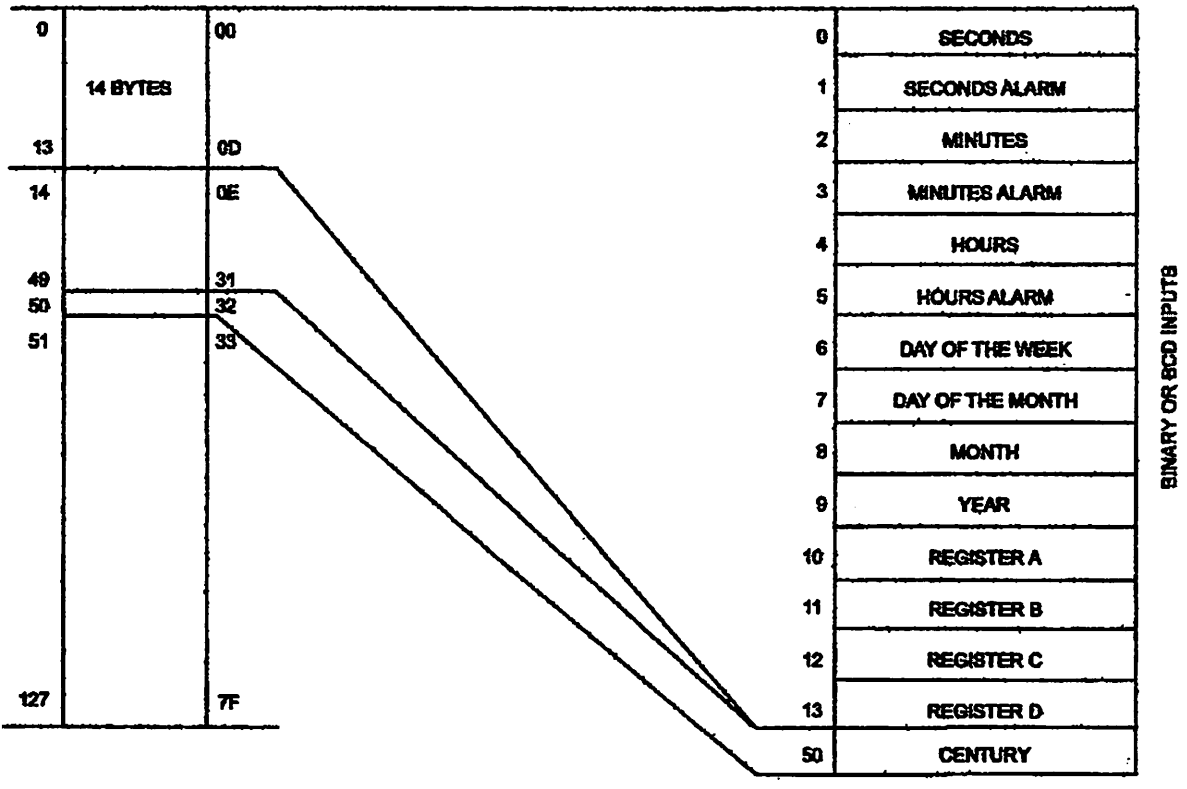
he Real Time Clock function will continue to operate and all of the RAM, time, calendar, and alarm emory locations remain nonvolatile regardless of the level of the V_{CC} input. When V_{CC} is applied to the S12C887 and reaches a level of greater than 4.25 volts, the device becomes accessible after 200 ms, ovided that the oscillator is running and the oscillator countdown chain is not in reset (see Register A). his time period allows the system to stabilize after power is applied. When V_{CC} falls below 4.25 volts, e chip select input is internally forced to an inactive level regardless of the value of $\overline{CS}$ at the input pin. he DS12C887 is, therefore, write-protected. When the DS12C887 is in a write-protected state, all inputs e ignored and all outputs are in a high impedance state. When V_{CC} falls below a level of approximately volts, the external V_{CC} supply is switched off and an internal lithium energy source supplies power to e Real Time Clock and the RAM memory.

TC ADDRESS MAP

he address map for the DS12C885 is shown in Figure 2. The address map consists of 113 bytes of user AM, 11 bytes of RAM that contain the RTC time, calendar, and alarm data, and 4 bytes which are used r control and status. All 128 bytes can be directly written or read except for the following:

1. Registers C and D are read-only.
2. Bit-7 of Register A is read-only.
3. The high order bit of the seconds byte is read-only.

S12C887 REAL TIME CLOCK ADDRESS MAP Figure 2



IME, CALENDAR AND ALARM LOCATIONS

he time and calendar information is obtained by reading the appropriate memory bytes. The time, ılendar, and alarm are set or initialized by writing the appropriate RAM bytes. The contents of the ten me, calendar, and alarm bytes can be either Binary or Binary-Coded Decimal (BCD) format. Before riting the internal time, calendar, and alarm registers, the SET bit in Register B should be written to a ıgic one to prevent updates from occurring while access is being attempted. In addition to writing the ten me, calendar, and alarm registers in a selected format (binary or BCD), the data mode bit (DM) of egister B must be set to the appropriate logic level. All ten time, calendar, and alarm bytes must use the ıme data mode. The set bit in Register B should be cleared after the data mode bit has been written to low the real time clock to update the time and calendar bytes. Once initialized, the real time clock ıakes all updates in the selected mode. The data mode cannot be changed without reinitializing the ten ıta bytes. Table 2 shows the binary and BCD formats of the ten time, calendar, and alarm locations. The 4–12 bit cannot be changed without reinitializing the hour locations. When the 12–hour format is ılected, the high order bit of the hours byte represents PM when it is a logic one. The time, calendar, ıd alarm bytes are always accessible because they are double buffered. Once per second the eleven bytes e advanced by one second and checked for an alarm condition. If a read of the time and calendar data ccurs during an update, a problem exists where seconds, minutes, hours, etc. may not correlate. The obability of reading incorrect time and calendar data is low. Several methods of avoiding any possible ıcorrect time and calendar reads are covered later in this text. The three alarm bytes can be used in two ays. First, when the alarm time is written in the appropriate hours, minutes, and seconds alarm ıcations, the alarm interrupt is initiated at the specified time each day if the alarm enable bit is high . The cond use condition is to insert a "don't care" state in one or more of the three alarm bytes. The "don't ıre" code is any hexadecimal value from C0 to FF. The two most significant bits of each byte set the lon't care" condition when at logic 1. An alarm will be generated each hour when the "don't care" bits e set in the hours byte. Similarly, an alarm is generated every minute with "don't care" codes in the ours and minute alarm bytes. The "don't care" codes in all three alarm bytes create an interrupt every cond.

IME, CALENDAR AND ALARM DATA MODES Table 1

ADDRESS LOCATION	FUNCTION	DECIMAL RANGE	RANGE	
			BINARY DATA MODE	BCD DATA MODE
0	Seconds	0-59	00-3B	00-59
1	Seconds Alarm	0-59	00-3B	00-59
2	Minutes	0-59	00-3B	00-59
3	Minutes Alarm	0-59	00-3B	00-59
4	Hours 12-hr, Mode	1-12	01-0C AM, 81-8C PM	01-12 AM, 81-92 PM
	Hours 24-hr, Mode	0-23	00-17	00-23
5	Hours Alarm 12-hr, Mode	1-12	01-0C AM, 81-8C PM	01-12 AM, 81-92 PM
	Hours Alarm 24-hr, Mode	0-23	00-17	00-23
6	Day of the week Sunday=1	1-7	01-07	01-07
7	Date of Month	1-31	01-1F	01-31
8	Month	1-12	01-0C	01-12
9	Year	0-99	00-63	00-99
50	Century	0-99	NA	19,20

REGISTER B

MSB **LSB**

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
SET	PIE	AIE	UIE	SQWE	DM	24/12	DSE

SET - When the SET bit is a 0, the update transfer functions normally by advancing the counts once per second. When the SET bit is written to a 1, any update transfer is inhibited and the program can initialize the time and calendar bytes without an update occurring in the midst of initializing. Read cycles can be executed in a similar manner. SET is a read/write bit and is not affected by $\overline{\text{RESET}}$ or internal functions of the DS12C887.

PIE - The Periodic Interrupt Enable bit is a read/write bit which allows the Periodic Interrupt Flag (PF) bit in Register C to drive the $\overline{\text{IRQ}}$ pin low. When the PIE bit is set to 1, periodic interrupts are generated by driving the $\overline{\text{IRQ}}$ pin low at a rate specified by the RS3-RS0 bits of Register A. A 0 in the PIE bit blocks the $\overline{\text{IRQ}}$ output from being driven by a periodic interrupt, but the Periodic Flag (PF) bit is still set at the periodic rate. PIE is not modified by any internal DS12C887 functions but is cleared to 0 on $\overline{\text{RESET}}$.

AIE - The Alarm Interrupt Enable (AIE) bit is a read/write bit which, when set to a 1, permits the Alarm Flag (AF) bit in register C to assert $\overline{\text{IRQ}}$. An alarm interrupt occurs for each second that the 3 time bytes equal the 3 alarm bytes including a "don't care" alarm code of binary 11XXXXXX. When the AIE bit is set to 0, the AF bit does not initiate the $\overline{\text{IRQ}}$ signal. The internal functions of the DS12C887 not affect the AIE bit.

UIE - The Update Ended Interrupt Enable (UIE) bit is a read/write bit that enables the Update End Flag (UF) bit in Register C to assert $\overline{\text{IRQ}}$. The $\overline{\text{RESET}}$ pin going low or the SET bit going high clears the UIE bit.

SQWE - When the Square Wave Enable (SQWE) bit is set to a 1, a square wave signal at the frequency set by the rate-selection bits RS3 through RS0 is driven out on the SQW pin. When the SQWE bit is set to 0, the SQW pin is held low. SQWE is a read/write bit and is cleared by $\overline{\text{RESET}}$. SQWE is set to a 1 when V_{CC} is powered up.

DM - The Data Mode (DM) bit indicates whether time and calendar information is in binary or BCD format. The DM bit is set by the program to the appropriate format and can be read as required. This bit is not modified by internal functions or $\overline{\text{RESET}}$. A 1 in DM signifies binary data while a 0 in DM specifies Binary Coded Decimal (BCD) data.

24/12 - The 24/12 control bit establishes the format of the hours byte. A 1 indicates the 24-hour mode and a 0 indicates the 12-hour mode. This bit is read/write and is not affected by internal functions or $\overline{\text{RESET}}$.

DSE - The Daylight Savings Enable (DSE) bit is a read/write bit which enables two special updates when DSE is set to 1. On the first Sunday in April the time increments from 1:59:59 AM to 3:00:00 AM. On the last Sunday in October when the time first reaches 1:59:59 AM it changes to 1:00:00 AM. These special updates do not occur when the DSE bit is a zero. This bit is not affected by internal functions or $\overline{\text{RESET}}$.

REGISTER C

MSB LSB

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
IRQF	PF	AF	UF	0	0	0	0

RQF - The Interrupt Request Flag (IRQF) bit is set to a 1 when one or more of the following are true:
'F = PIE = 1
AF = AIE = 1
JF = UIE = 1

e., IRQF = (PF • PIE) + (AF • AIE) + (UF • UIE)

ny time the IRQF bit is a 1, the $\overline{\text{IRQ}}$ pin is driven low. Flag bits PF, AF, and UF are cleared after egister C is read by the program or when the $\overline{\text{RESET}}$ pin is low.

F - The Periodic Interrupt Flag (PF) is a read-only bit which is set to a 1 when an edge is detected on the elected tap of the divider chain. The RS3 through RS0 bits establish the periodic rate. PF is set to a 1 ndependent of the state of the PIE bit. When both PF and PIE are 1's, the $\overline{\text{IRQ}}$ signal is active and will et the IRQF bit. The PF bit is cleared by a software read of Register C or a $\overline{\text{RESET}}$.

AF - A 1 in the Alarm Interrupt Flag (AF) bit indicates that the current time has matched the alarm time. f the AIE bit is also a 1, the $\overline{\text{IRQ}}$ pin will go low and a 1 will appear in the IRQF bit. A $\overline{\text{RESET}}$ or a read f Register C will clear AF.

UF - The Update Ended Interrupt Flag (UF) bit is set after each update cycle. When the UIE bit is set to , the 1 in UF causes the IRQF bit to be a 1, which will assert the $\overline{\text{IRQ}}$ pin. UF is cleared by reading egister C or a $\overline{\text{RESET}}$.

BIT 3 THROUGH BIT 0 - These are unused bits of the status Register C. These bits always read 0 and annot be written.

REGISTER D

MSB LSB

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
VRT	0	0	0	0	0	0	0

VRT - The Valid RAM and Time (VRT) bit indicates the condition of the battery connected to the V_{BAT} in. This bit is not writeable and should always be a 1 when read. If a 0 is ever present, an exhausted nternal lithium energy source is indicated and both the contents of the RTC data and RAM data are uestionable. This bit is unaffected by $\overline{\text{RESET}}$.

BIT 6 THROUGH BIT 0 - The remaining bits of Register D are not usable. They cannot be written and, hen read, they will always read 0.

CENTURY REGISTER

The century register at location 32h, is a BCD register designed to automatically load the BCD value 20 as the year register changes from 99 to 00. The MSB of this register will not be affected when the load of 20 occurs and will remain at the value written by the user.

NONVOLATILE RAM

The 113 general purpose nonvolatile RAM bytes are not dedicated to any special function within the DS12C887. They can be used by the processor program as nonvolatile memory and are fully available during the update cycle.

INTERRUPTS

The RTC plus RAM includes three separate, fully automatic sources of interrupt for a processor. The alarm interrupt can be programmed to occur at rates from once per second to once per day. The periodic interrupt can be selected for rates from 500ms to 122µs. The update-ended interrupt can be used to indicate to the program that an update cycle is complete. Each of these independent interrupt conditions is described in greater detail in other sections of this text.

The processor program can select which interrupts, if any, are going to be used. Three bits in Register B enable the interrupts. Writing a logic 1 to an interrupt-enable bit permits that interrupt to be initiated when the event occurs. A zero in an interrupt-enable bit prohibits the $\overline{IRQ}$ pin from being asserted from that interrupt condition. If an interrupt flag is already set when an interrupt is enabled, $\overline{IRQ}$ is immediately set at an active level, although the interrupt initiating the event may have occurred much earlier. As a result, there are cases where the program should clear such earlier initiated interrupts before first enabling new interrupts.

When an interrupt event occurs, the relating flag bit is set to logic 1 in Register C. These flag bits are set independent of the state of the corresponding enable bit in Register B. The flag bit can be used in a polling mode without enabling the corresponding enable bits. The interrupt flag bit is a status bit which software can interrogate as necessary. When a flag is set, an indication is given to software that an interrupt event has occurred since the flag bit was last read; however, care should be taken when using the flag bits as they are cleared each time Register C is read. Double latching is included with Register C so that bits which are set remain stable throughout the read cycle. All bits which are set (high) are cleared when read and new interrupts which are pending during the read cycle are held until after the cycle is completed. One, two, or three bits can be set when reading Register C. Each utilized flag bit should be examined when read to ensure that no interrupts are lost.

The second flag bit usage method is with fully enabled interrupts. When an interrupt flag bit is set and the corresponding interrupt enable bit is also set, the $\overline{IRQ}$ pin is asserted low. $\overline{IRQ}$ is asserted as long as at least one of the three interrupt sources has its flag and enable bits both set. The IRQF bit in Register C is a one whenever the $\overline{IRQ}$ pin is being driven low. Determination that the RTC initiated an interrupt is accomplished by reading Register C. A logic one in bit 7 (IRQF bit) indicates that one or more interrupts have been initiated by the DS12C887. The act of reading Register C clears all active flag bits and the IRQF bit.

OSCILLATOR CONTROL BITS

When the DS12C887 is shipped from the factory, the internal oscillator is turned off. This feature prevents the lithium energy cell from being used until it is installed in a system. A pattern of 010 in bits 4 through 6 of Register A will turn the oscillator on and enable the countdown chain. A pattern of 11X will turn the oscillator on, but holds the countdown chain of the oscillator in reset. All other combinations of bits 4 through 6 keep the oscillator off.

SQUARE WAVE OUTPUT SELECTION

Thirteen of the 15 divider taps are made available to a 1-of-15 selector, as shown in the block diagram of Figure 1. The first purpose of selecting a divider tap is to generate a square wave output signal on the SQW pin. The RS0–RS3 bits in Register A establish the square wave output frequency. These frequencies are listed in Table 1. The SQW frequency selection shares its 1-of-15 selector with the periodic interrupt generator. Once the frequency is selected, the output of the SQW pin can be turned on and off under program control with the square wave enable bit (SQWE).

PERIODIC INTERRUPT SELECTION

The periodic interrupt will cause the $\overline{IRQ}$ pin to go to an active state from once every 500ms to once every 122µs. This function is separate from the alarm interrupt which can be output from once per second to once per day. The periodic interrupt rate is selected using the same Register A bits which select the square wave frequency (see Table 1). Changing the Register A bits affects both the square wave frequency and the periodic interrupt output. However, each function has a separate enable bit in Register B. The SQWE bit controls the square wave output. Similarly, the periodic interrupt is enabled by the PIE bit in Register B. The periodic interrupt can be used with software counters to measure inputs, create output intervals, or await the next needed software function.

PERIODIC INTERRUPT RATE AND SQUARE WAVE OUTPUT FREQUENCY

Table 2

EXT. REG. B	SELECT BITS REGISTER A				t_{PI} PERIODIC INTERRUPT RATE	SQW OUTPUT FREQUENCY
E32K	RS3	RS2	RS1	RS0		
0	0	0	0	0	None	None
0	0	0	0	1	3.90625 ms	256 Hz
0	0	0	1	0	7.8125 ms	128 Hz
0	0	0	1	1	122.070 µs	8.192 kHz
0	0	1	0	0	244.141 µs	4.096 kHz
0	0	1	0	1	488.281 µs	2.048 kHz
0	0	1	1	0	976.5625 µs	1.024 kHz
0	0	1	1	1	1.953125 ms	512 Hz
0	1	0	0	0	3.90625 ms	256 Hz
0	1	0	0	1	7.8125 ms	128 Hz
0	1	0	1	0	15.625 ms	64 Hz
0	1	0	1	1	31.25 ms	32 Hz
0	1	1	0	0	62.5 ms	16 Hz
0	1	1	0	1	125 ms	8 Hz
0	1	1	1	0	250 ms	4 Hz
0	1	1	1	1	500 ms	2 Hz

UPDATE CYCLE

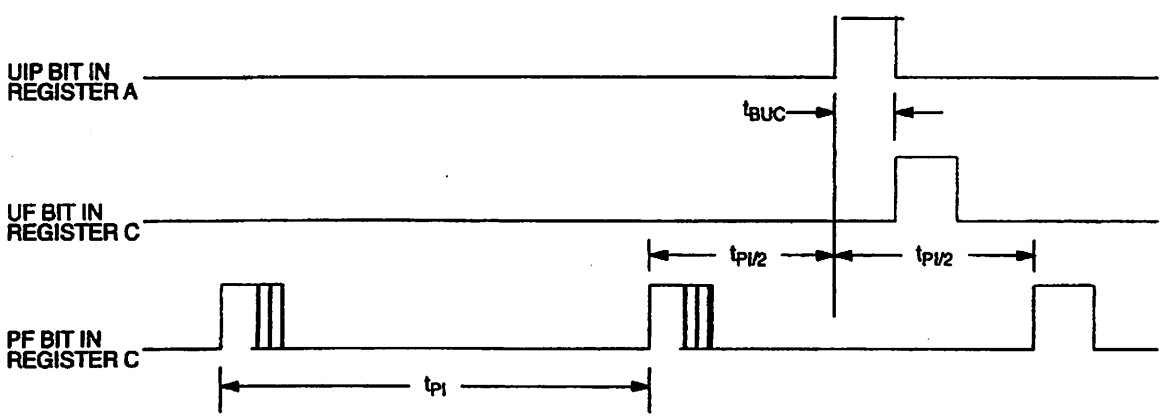
The DS12C887 executes an update cycle once per second regardless of the SET bit in Register B. When the SET bit in Register B is set to one, the user copy of the double buffered time, calendar, and alarm bytes is frozen and will not update as the time increments. However, the time countdown chain continues to update the internal copy of the buffer. This feature allows time to maintain accuracy independent of reading or writing the time, calendar, and alarm buffers and also guarantees that time and calendar information is consistent. The update cycle also compares each alarm byte with the corresponding time byte and issues an alarm if a match or if a "don't care" code is present in all three positions.

There are three methods that can handle access of the real time clock that avoid any possibility of accessing inconsistent time and calendar data. The first method uses the update-ended interrupt. If enabled, an interrupt occurs after every up date cycle that indicates that over 999 ms are available to read valid time and date information. If this interrupt is used, the IRQF bit in Register C should be cleared before leaving the interrupt routine.

A second method uses the update-in-progress bit (UIP) in Register A to determine if the update cycle is in progress. The UIP bit will pulse once per second. After the UIP bit goes high, the update transfer occurs 244µs later. If a low is read on the UIP bit, the user has at least 244µs before the time/calendar data will be changed. Therefore, the user should avoid interrupt service routines that would cause the time needed to read valid time/calendar data to exceed 244µs.

The third method uses a periodic interrupt to determine if an update cycle is in progress. The UIP bit in Register A is set high between the setting of the PF bit in Register C (see Figure 3). Periodic interrupts that occur at a rate of greater than t_{BUC} allow valid time and date information to be reached at each occurrence of the periodic interrupt. The reads should be complete within 1 ($t_{PI/2} + t_{BUC}$) to ensure that data is not read during the update cycle.

UPDATE-ENDED AND PERIODIC INTERRUPT RELATIONSHIP Figure 3



t_{PI} = PERIODIC INTERRUPT TIME INTERNAL PER TABLE 1
t_{BUC} = DELAY TIME BEFORE UPDATE CYCLE = 244 µs

ABSOLUTE MAXIMUM RATINGS*

Voltage on Any Pin Relative to Ground	-0.3V to +7.0V
Operating Temperature	0° to 70°C
Storage Temperature	-40°C to +70°C
Soldering Temperature	260°C for 10 seconds (See Note 7)

* This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operation sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect reliability.

RECOMMENDED DC OPERATING CONDITIONS (0°C to 70°C)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Power Supply Voltage	V_{CC}	4.5	5.0	5.5	V	1
Input Logic 1	V_{IH}	2.3		V_{CC}+0.3	V	1
Input Logic 0	V_{IL}	-0.3		0.8	V	1

DC ELECTRICAL CHARACTERISTICS (0°C to 70°C; VCC = 5.0V ± 10%)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Average V_{CC} Power Supply Current	I_{CC1}		7	15	mA	2
Input Leakage	I_{IL}	-1.0		+1.0	µA	3
I/O Leakage	I_{OL}	-1.0		+1.0	µA	4
Input Current	I_{MOT}	-1.0		+500	µA	3
Output @ 2.4V	I_{OH}	-1.0			mA	1,5
Output @ 0.4V	I_{OL}			4.0	mA	1
Write Protect Voltage	V_{TP}	4.0	4.25	4.5	V	

CAPACITANCE (tA = 25°C)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Input Capacitance	C_{IN}			5	pF	
Output Capacitance	C_{OUT}			7	pF	

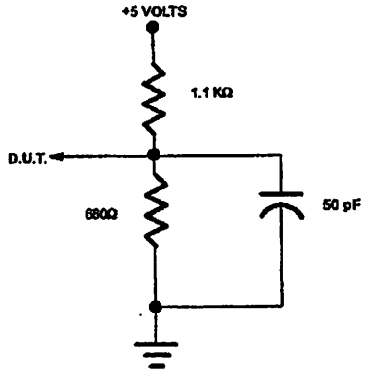
AC ELECTRICAL CHARACTERISTICS (0°C to 70°C; VCC = 5.0V ± 10%)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Cycle Time	t_{CYC}	385		DC	ns	
Pulse Width, DS/E Low or RD/$\overline{WR}$ High	PW_{EL}	150			ns	
Pulse Width, DS/E High or RD/$\overline{WR}$ Low	PW_{RH}	125			ns	
Input Rise and Fall	t_R, t_F			30	ns	
R/$\overline{W}$ Hold Time	t_{RWH}	10			ns	
R/$\overline{W}$ Setup Time Before DS/E	t_{RWS}	50			ns	
Chip Select Setup Time Before DS, $\overline{WR}$, or $\overline{RD}$	t_{CS}	20			ns	
Chip Select Hold Time	t_{CH}	0			ns	
Read Data Hold Time	t_{DHR}	10		80	ns	
Write Data Hold Time	t_{DHW}	0			ns	
Mux'ed Address Valid Time to ALE Fall	t_{ASL}	30			ns	
Mused Address Hold Time to ALE Fall	t_{AHL}	10			ns	
Delay Time DS/E to AS/ALE Rise	t_{ASD}	20			ns	
Pulse Width AS/ALE High	PW_{ASH}	60			ns	
Delay Time, AS/ALE to DS/E Rise	t_{ASED}	40			ns	
Output Data Delay Time from DS/E or $\overline{RD}$	t_{DDR}	20		120	ns	6
Data Setup Time	t_{DSW}	100			ns	
Reset Pulse Width	t_{RWL}	5			µs	
$\overline{IRQ}$ Release from DS	t_{IRDS}			2	µs	
$\overline{IRQ}$ Release from $\overline{RESET}$	t_{IRR}			2	µs	

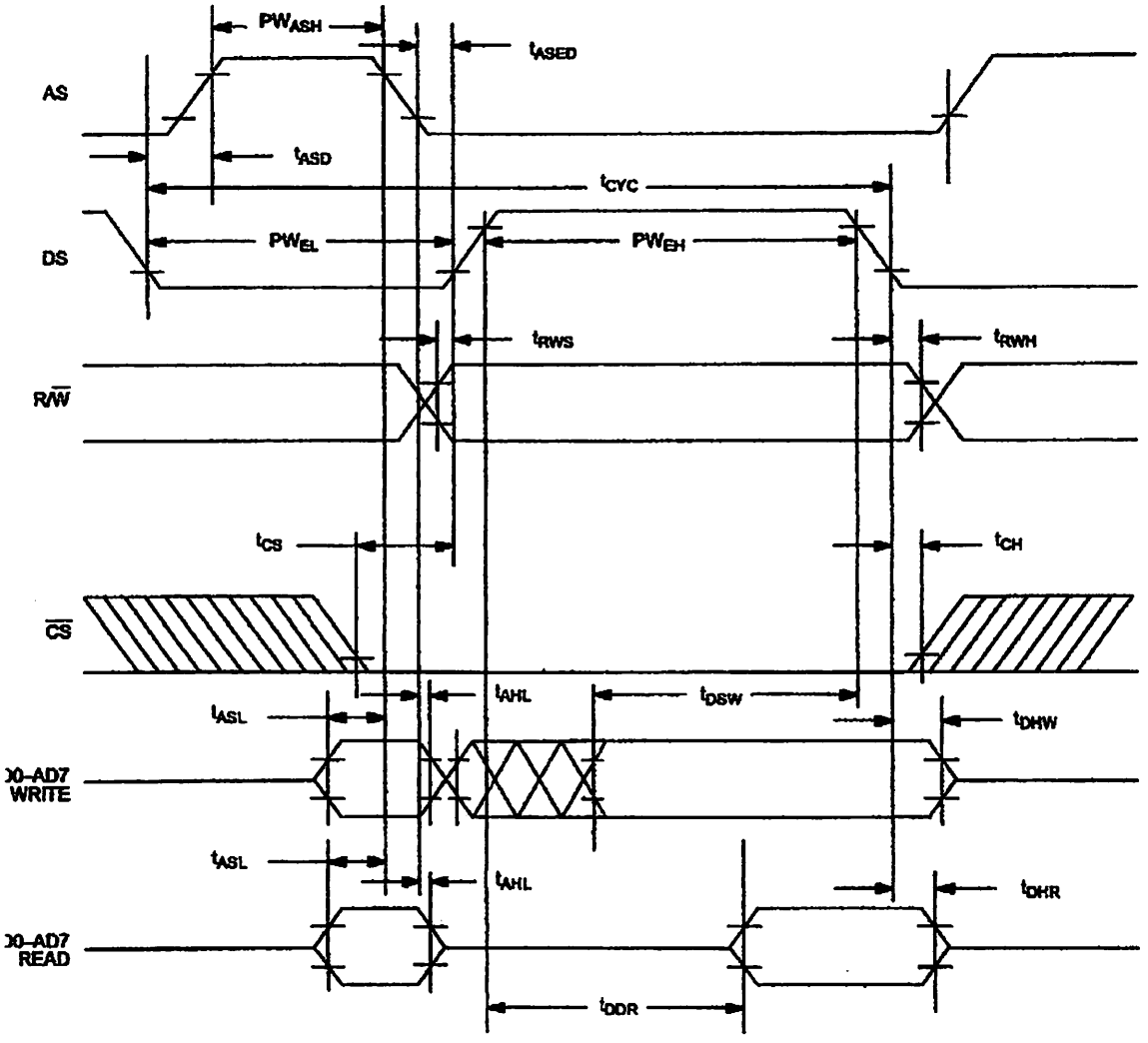
NOTES:

1. All voltages are referenced to ground.
2. All Outputs are open.
3. The MOT pin has an internal pull-down of 20KΩ.
4. Applies to the AD0-AD7 pins, the $\overline{IRQ}$ pin, and the SQW pin when each is in a high impedance state.
5. The $\overline{IRQ}$ pin is open drain.
6. Measured with a load as shown in Figure 4.
7. Real-Time Clock Modules can be successfully processed through conventional wave-soldering techniques as long as temperature exposure to the lithium energy source contained within does not exceed +85°C. Post solder cleaning with water washing techniques is acceptable, provided that ultrasonic vibration is not used. Such cleaning can damage the crystal.

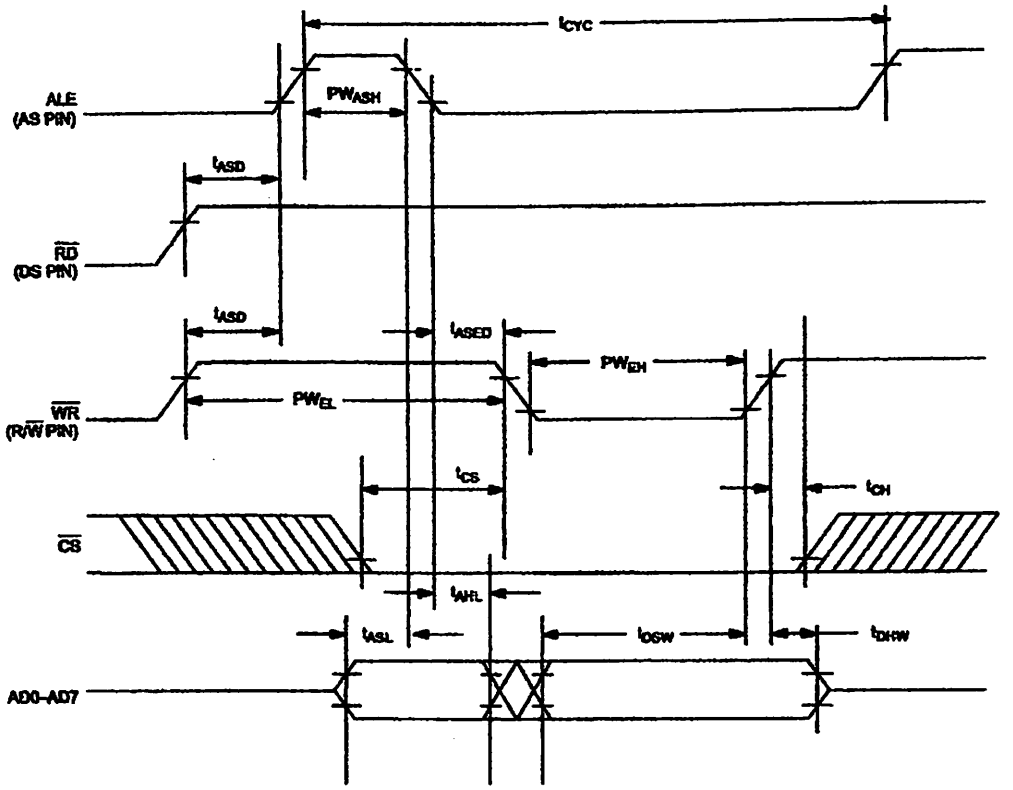
TPUT LOAD Figure 4



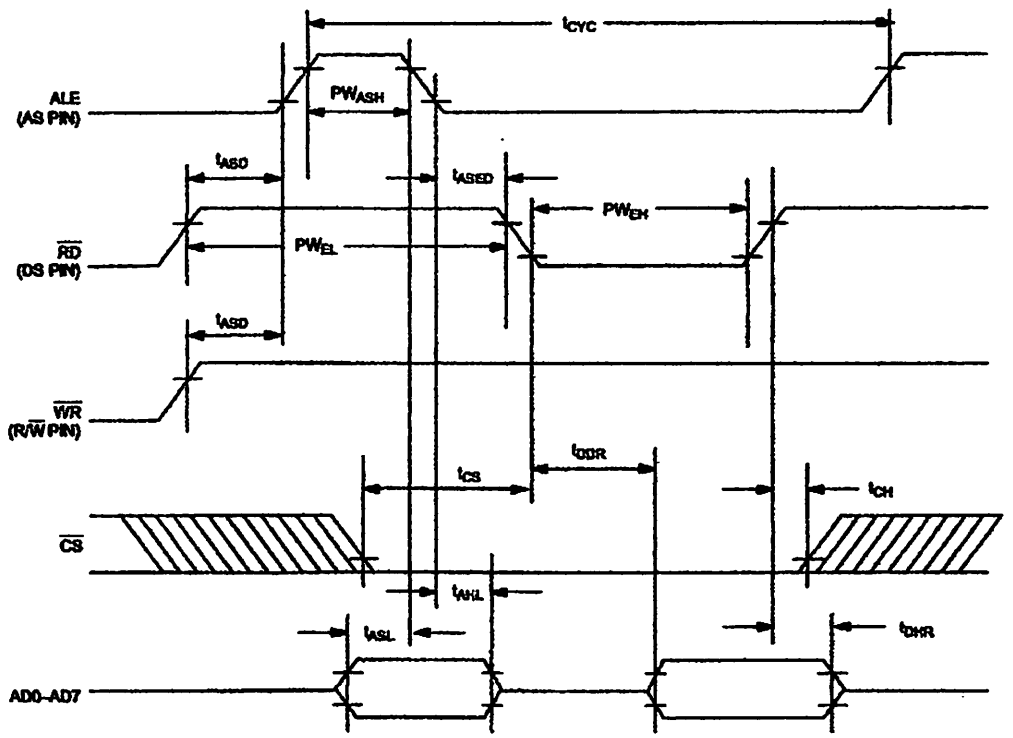
12C887 BUS TIMING FOR MOTOROLA INTERFACE



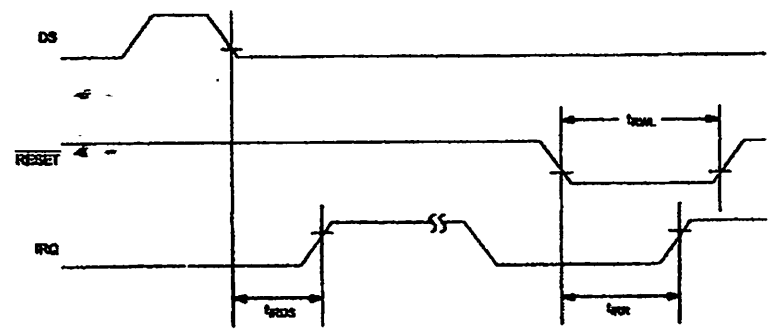
DS12C887 BUS TIMING FOR INTEL INTERFACE WRITE CYCLE



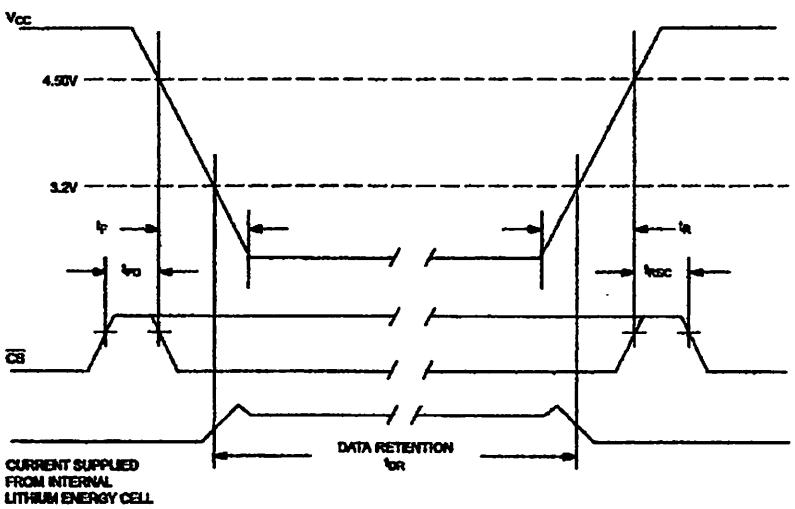
DS12C887 BUS TIMING FOR INTEL INTERFACE READ CYCLE



DS12C887 IRQ RELEASE DELAY TIMING



POWER DOWN / POWER UP TIMING



POWER DOWN / POWER UP TIMING

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
$\overline{CS}$ at V_{IH} before Power-Down	t_{PD}			0	µs	
V_{CC} slew from 4.5V to 0V ($\overline{CS}$ at V_{IH})	t_F $4.0 \le V_{CC} \le 4.5V$	300			µs	
V_{CC} slew from 0V to 4.5V ($\overline{CS}$ at V_{IH})	t_R	100			µs	
$\overline{CS}$ at V_{IH} after Power-Up	t_{REC}	20		200	ms	
Expected Data Retention	t_{DR}	10			years	10,11

(tA=25°C)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Expected Data Retention	t_{DR}	10			years	10,11

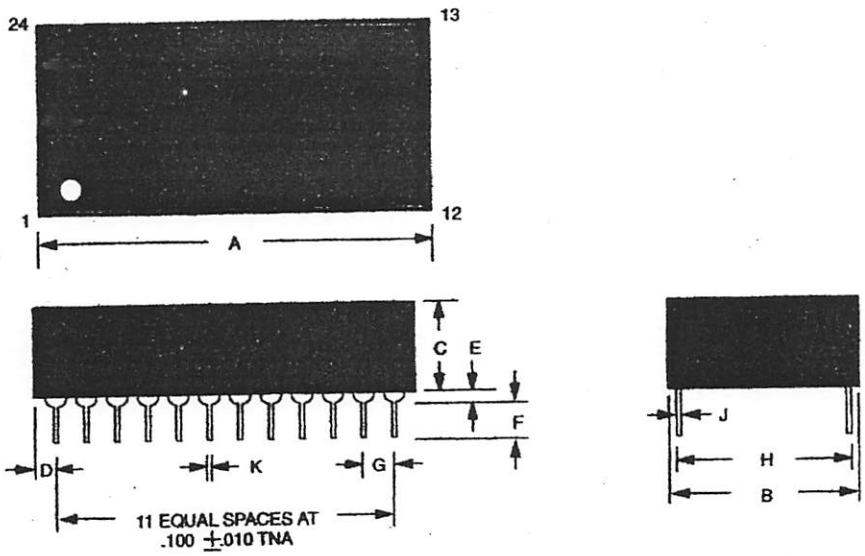
Note:

The real time clock will keep time to an accuracy of ±1 minute per month during data retention time for the period of t_{DR}.

Warning:

Under no circumstances are negative undershoots, of any amplitude, allowed when device is in battery back-up mode.

DS12C887 REAL TIME CLOCK PLUS RAM



NOTE:

Pins 2, 3, 16, 20, 21 and 22 are missing by design

PKG	24-PIN	
DIM	MIN	MAX
A IN	1.320	1.335
MM	33.53	33.91
B IN	0.675	0.700
MM	17.15	17.78
C IN	0.345	0.370
MM	8.76	9.40
D IN	0.100	0.130
MM	2.54	3.30
E IN	0.015	0.030
MM	0.38	0.76
F IN	0.110	0.140
MM	2.79	3.56
G IN	0.090	0.110
MM	2.29	2.79
H IN	0.590	0.630
MM	14.99	16.00
J IN	0.008	0.012
MM	0.20	0.30
K IN	0.015	0.021
MM	0.38	0.53

FAIRCHILD SEMICONDUCTOR™

October 1987
Revised January 1999

MM74C922 • MM74C923
16-Key Encoder • 20-Key Encoder

General Description

The MM74C922 and MM74C923 CMOS key encoders provide all the necessary logic to fully encode an array of SPST switches. The keyboard scan can be implemented by either an external clock or external capacitor. These encoders also have on-chip pull-up devices which permit switches with up to 50 kΩ on resistance to be used. No diodes in the switch array are needed to eliminate ghost switches. The internal debounce circuit needs only a single external capacitor and can be defeated by omitting the capacitor. A Data Available output goes to a high level when a valid keyboard entry has been made. The Data Available output returns to a low level when the entered key is released, even if another key is depressed. The Data Available will return high to indicate acceptance of the new key after a normal debounce period; this two-key roll-over is provided between any two switches.

An internal register remembers the last key pressed even after the key is released. The 3-STATE outputs provide for easy expansion and bus operation and are LPTTL compatible.

Features

- 50 kΩ maximum switch on resistance
- On or off chip clock
- On-chip row pull-up devices
- 2 key roll-over
- Keybounce elimination with single capacitor
- Last key register at outputs
- 3-STATE output LPTTL compatible
- Wide supply range: 3V to 15V
- Low power consumption

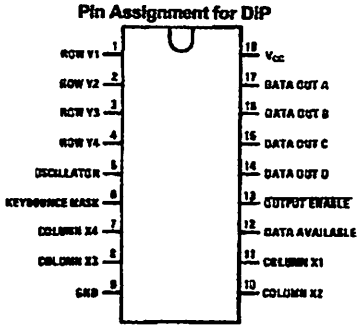
Ordering Code:

Order Number	Package Number	Package Description
MM74C922N	N18A	18-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300" Wide
MM74C922WM	M20B	20-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-013, 0.300" Wide
MM74C923WM	M20B	20-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-013, 0.300" Wide
MM74C923N	N20A	20-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300" Wide

Device also available in Tape and Reel. Specify by appending suffix letter "X" to the ordering code.

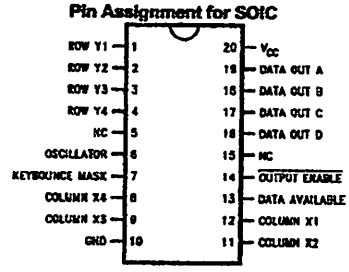
Connection Diagrams

Pin Assignment for DIP



Top View
MM94C922

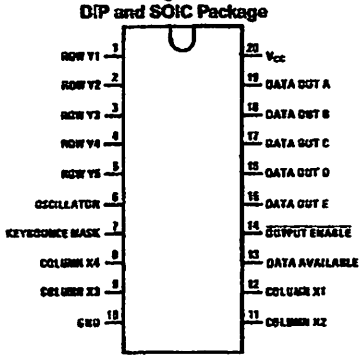
Pin Assignment for SOIC



Top View
MM74C922

Connection Diagrams (Continued)

Pin Assignment for
DIP and SOIC Package



Top View
MM74C923

Truth Tables

(Pins 0 through 11)

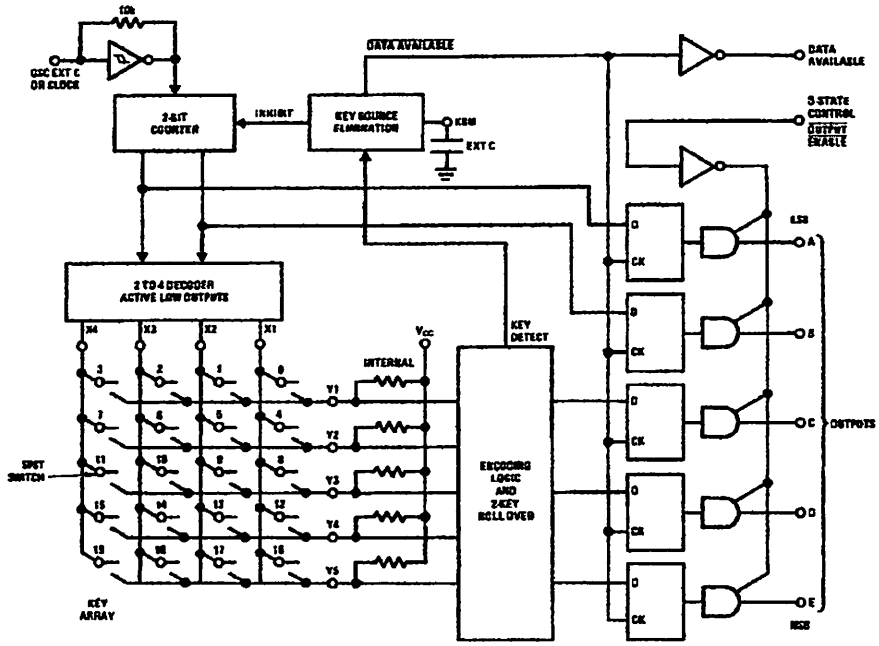
Switch Position		0 Y1,X1	1 Y1,X2	2 Y1,X3	3 Y1,X4	4 Y2,X1	5 Y2,X2	6 Y2,X3	7 Y2,X4	8 Y3,X1	9 Y3,X2	10 Y3,X3	11 Y3,X4
DATA OUT	A	0	1	0	1	0	1	0	1	0	1	0	1
	B	0	0	1	1	0	0	1	1	0	0	1	1
	C	0	0	0	0	1	1	1	1	0	0	0	0
	D	0	0	0	0	0	0	0	0	1	1	1	1
	E (Note 1)	0	0	0	0	0	0	0	0	0	0	0	0

(Pins 12 through 19)

Switch Position		12 Y4,X1	13 Y4,X2	14 Y4,X3	15 Y4,X4	16 Y5(Note 1), X1	17 Y5 (Note 1), X2	18 Y5 (Note 1), X3	19 Y5 (Note 1), X4
DATA OUT	A	0	1	0	1	0	1	0	1
	B	0	0	1	1	0	0	1	1
	C	1	1	1	1	0	0	0	0
	D	1	1	1	1	0	0	0	0
	E (Note 1)	0	0	0	0	1	1	1	1

Note 1: Omit for MM74C922

Block Diagram



Absolute Maximum Ratings (Note 2)

Voltage at Any Pin	V_{CC} − 0.3V to V_{CC} + 0.3V
Operating Temperature Range	
MM74C922, MM74C923	−40°C to +85°C
Storage Temperature Range	−65°C to +150°C
Power Dissipation (P_D)	
Dual-In-Line	700 mW
Small Outline	500 mW
Operating V_{CC} Range	3V to 15V
V_{CC}	18V
Lead Temperature	
(Soldering, 10 seconds)	260°C

Note 2: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Temperature Range" they are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

DC Electrical Characteristics

Min/Max limits apply across temperature range unless otherwise specified

Symbol	Parameter	Conditions	Min	Typ	Max	Units
CMOS TO CMOS						
V_{T+}	Positive-Going Threshold Voltage at Osc and KBM Inputs	V_{CC} = 5V, $I_{IN} \geq$ 0.7 mA	3.0	3.6	4.3	V
		V_{CC} = 10V, $I_{IN} \geq$ 1.4 mA	6.0	6.8	8.6	V
		V_{CC} = 15V, $I_{IN} \geq$ 2.1 mA	9.0	10	12.9	V
V_{T-}	Negative-Going Threshold Voltage at Osc and KBM Inputs	V_{CC} = 5V, $I_{IN} \geq$ 0.7 mA	0.7	1.4	2.0	V
		V_{CC} = 10V, $I_{IN} \geq$ 1.4 mA	1.4	3.2	4.0	V
		V_{CC} = 15V, $I_{IN} \geq$ 2.1 mA	2.1	5	6.0	V
$V_{IN(1)}$	Logical "1" Input Voltage, Except Osc and KBM Inputs	V_{CC} = 5V	3.5	4.5		V
		V_{CC} = 10V	8.0	9		V
		V_{CC} = 15V	12.5	13.5		V
$V_{IN(0)}$	Logical "0" Input Voltage, Except Osc and KBM Inputs	V_{CC} = 5V		0.5	1.5	V
		V_{CC} = 10V		1	2	V
		V_{CC} = 15V		1.5	2.5	V
I_{tp}	Row Pull-Up Current at Y1, Y2, Y3, Y4 and Y5 Inputs	V_{CC} = 5V, V_{IN} = 0.1 V_{CC}		−2	−5	μA
		V_{CC} = 10V		−10	−20	μA
		V_{CC} = 15V		−22	−45	μA
$V_{OUT(1)}$	Logical "1" Output Voltage	V_{CC} = 5V, I_O = −10 μA	4.5			V
		V_{CC} = 10V, I_O = −10 μA	9			V
		V_{CC} = 15V, I_O = −10 μA	13.5			V
$V_{OUT(0)}$	Logical "0" Output Voltage	V_{CC} = 5V, I_O = 10 μA			0.5	V
		V_{CC} = 10V, I_O = 10 μA			1	V
		V_{CC} = 15V, I_O = 10 μA			1.5	V
R_{oc}	Column "ON" Resistance at X1, X2, X3 and X4 Outputs	V_{CC} = 5V, V_O = 0.5V		500	1400	Ω
		V_{CC} = 10V, V_O = 1V		300	700	Ω
		V_{CC} = 15V, V_O = 1.5V		200	500	Ω
I_{CC}	Supply Current Osc at 0V, (one Y low)	V_{CC} = 5V		0.55	1.1	mA
		V_{CC} = 10V		1.1	1.9	mA
		V_{CC} = 15V		1.7	2.6	mA
$I_{IN(1)}$	Logical "1" Input Current at Output Enable	V_{CC} = 15V, V_{IN} = 15V		0.005	1.0	μA
$I_{IN(0)}$	Logical "0" Input Current at Output Enable	V_{CC} = 15V, V_{IN} = 0V	−1.0	−0.005		μA
CMOS/LPTTL INTERFACE						
$V_{IN(1)}$	Except Osc and KBM Inputs	V_{CC} = 4.75V	V_{CC} − 1.5			V
$V_{IN(0)}$	Except Osc and KBM Inputs	V_{CC} = 4.75V			0.8	V
$V_{OUT(1)}$	Logical "1" Output Voltage	I_O = −360 μA, V_{CC} = 4.75V, I_O = −360 μA	2.4			V
$V_{OUT(0)}$	Logical "0" Output Voltage	I_O = −360 μA, V_{CC} = 4.75V, I_O = −360 μA			0.4	V

DC Electrical Characteristics (Continued)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
OUTPUT DRIVE (See Family Characteristics Data Sheet) (Short Circuit Current)						
I_{SOURCE}	Output Source Current (P-Channel)	$V_{CC} = 5V$, $V_{OUT} = 0V$, $T_A = 25°C$	−1.75	−3.3		mA
I_{SOURCE}	Output Source Current (P-Channel)	$V_{CC} = 10V$, $V_{OUT} = 0V$, $T_A = 25°C$	−8	−15		mA
I_{SINK}	Output Sink Current (N-Channel)	$V_{CC} = 5V$, $V_{OUT} = V_{CC}$, $T_A = 25°C$	1.75	3.6		mA
I_{SINK}	Output Sink Current (N-Channel)	$V_{CC} = 10V$, $V_{OUT} = V_{CC}$, $T_A = 25°C$	8	16		mA

AC Electrical Characteristics (Note 3)

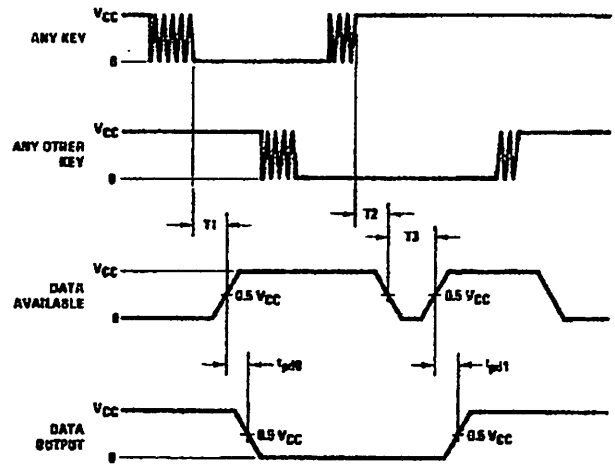
$T_A = 25°C$, $C_L = 50$ pF, unless otherwise noted

Symbol	Parameter	Conditions	Min	Typ	Max	Units
t_{pd0}, t_{pd1}	Propagation Delay Time to Logical "0" or Logical "1" from D.A.	$C_L = 50$ pF (Figure 1)				
		$V_{CC} = 5V$		60	150	ns
		$V_{CC} = 10V$		35	80	ns
		$V_{CC} = 15V$		25	60	ns
t_{0H}, t_{1H}	Propagation Delay Time from Logical "0" or Logical "1" into High Impedance State	$R_L = 10k$, $C_L = 10$ pF (Figure 2)				
		$V_{CC} = 5V$, $R_L = 10k$		80	200	ns
		$V_{CC} = 10V$, $C_L = 10$ pF		65	150	ns
		$V_{CC} = 15V$		50	110	ns
t_{H0}, t_{H1}	Propagation Delay Time from High Impedance State to a Logical "0" or Logical "1"	$R_L = 10k$, $C_L = 50$ pF (Figure 2)				
		$V_{CC} = 5V$, $R_L = 10k$		100	250	ns
		$V_{CC} = 10V$, $C_L = 50$ pF		55	125	ns
		$V_{CC} = 15V$		40	90	ns
C_{IN}	Input Capacitance	Any Input (Note 4)		5	7.5	pF
C_{OUT}	3-STATE Output Capacitance	Any Output (Note 4)		10		pF

Note 3: AC Parameters are guaranteed by DC correlated testing.

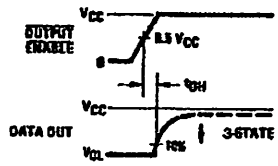
Note 4: Capacitance is guaranteed by periodic testing.

Switching Time Waveforms



T1 = T2 = RC, T3 = 0.7 RC, where R = 10k and C is external capacitor at KBM input.

FIGURE 1.



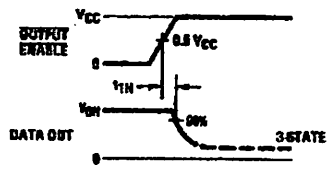
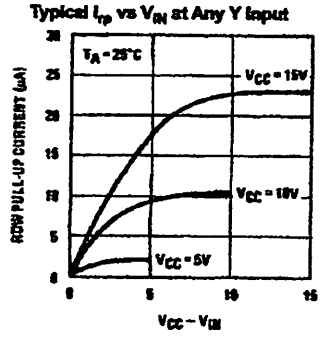


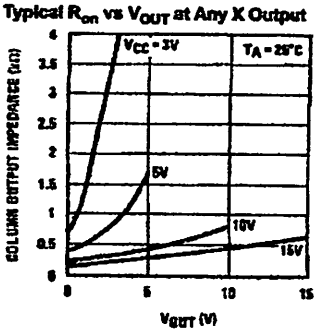
FIGURE 2.

Typical Performance Characteristics

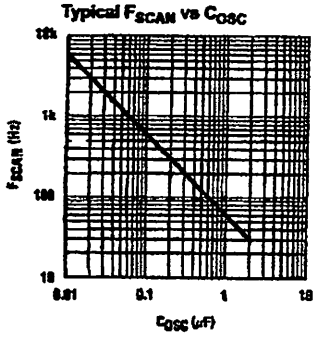
Typical I_{rp} vs V_{IN} at Any Y Input



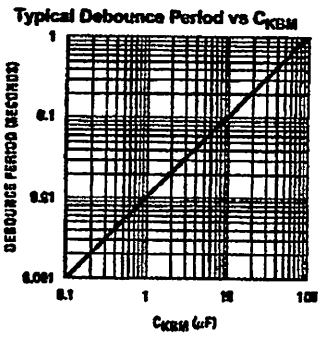
Typical R_{on} vs V_{OUT} at Any X Output



Typical F_{SCAN} vs C_{OSC}

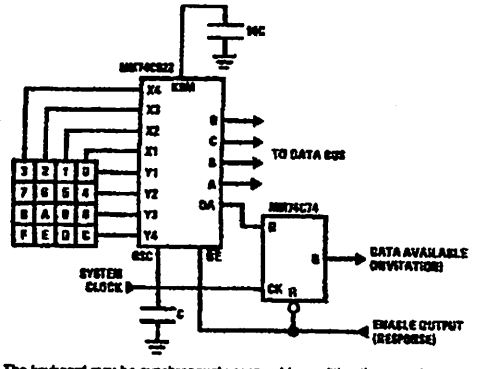


Typical Debounce Period vs C_{KBM}



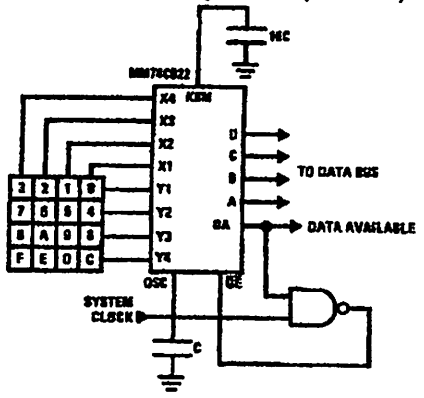
Typical Applications

Synchronous Handshake (MM74C922)



The keyboard may be synchronously scanned by omitting the capacitor at osc. and driving osc. directly if the system clock rate is lower than 10 kHz

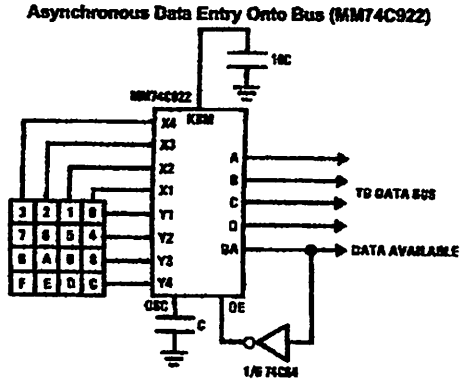
Synchronous Data Entry Onto Bus (MM74C922)



Outputs are enabled when valid entry is made and go into 3-STATE when key is released.

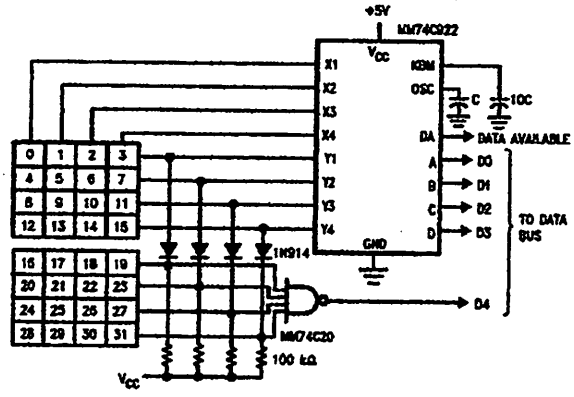
The keyboard may be synchronously scanned by omitting the capacitor at osc. and driving osc. directly if the system clock rate is lower than 10 kHz

Asynchronous Data Entry Onto Bus (MM74C922)



Outputs are in 3-STATE until key is pressed, then data is placed on bus. When key is released, outputs return to 3-STATE.

Expansion to 32 Key Encoder (MM74C922)



Theory of Operation

The MM74C922/MM74C923 Keyboard Encoders implement all the logic necessary to interface a 16 or 20 SPST key switch matrix to a digital system. The encoder will convert a key switch closer to a 4(MM74C922) or 5(MM74C923) bit nibble. The designer can control both the keyboard scan rate and the key debounce period by altering the oscillator capacitor, C_{OSE}, and the key bounce mask capacitor, C_{MSK}. Thus, the MM74C922/MM74C923's performance can be optimized for many keyboards.

The keyboard encoders connect to a switch matrix that is 4 rows by 4 columns (MM74C922) or 5 rows by 4 columns (MM74C923). When no keys are depressed, the row inputs are pulled high by internal pull-ups and the column outputs sequentially output a logic "0". These outputs are open drain and are therefore low for 25% of the time and otherwise off. The column scan rate is controlled by the oscillator input, which consists of a Schmitt trigger oscillator, a 2-bit counter, and a 2–4-bit decoder.

When a key is depressed, key 0, for example, nothing will happen when the X1 input is off, since Y1 will remain high. When the X1 column is scanned, X1 goes low and Y1 will go low. This disables the counter and keeps X1 low. Y1 going low also initiates the key bounce circuit timing and locks out the other Y inputs. The key code to be output is a combination of the frozen counter value and the decoded Y inputs. Once the key bounce circuit times out, the data is latched, and the Data Available (DAV) output goes high.

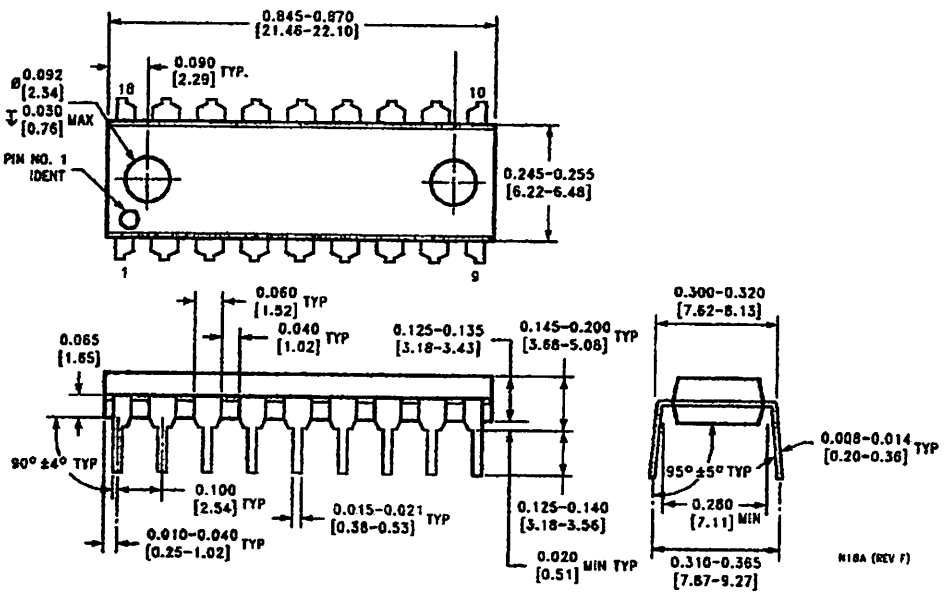
If, during the key closure the switch bounces, Y1 input will go high again, restarting the scan and resetting the key bounce circuitry. The key may bounce several times, but as soon as the switch stays low for a debounce period, the closure is assumed valid and the data is latched.

A key may also bounce when it is released. To ensure that the encoder does not recognize this bounce as another key closure, the debounce circuit must time out before another closure is recognized.

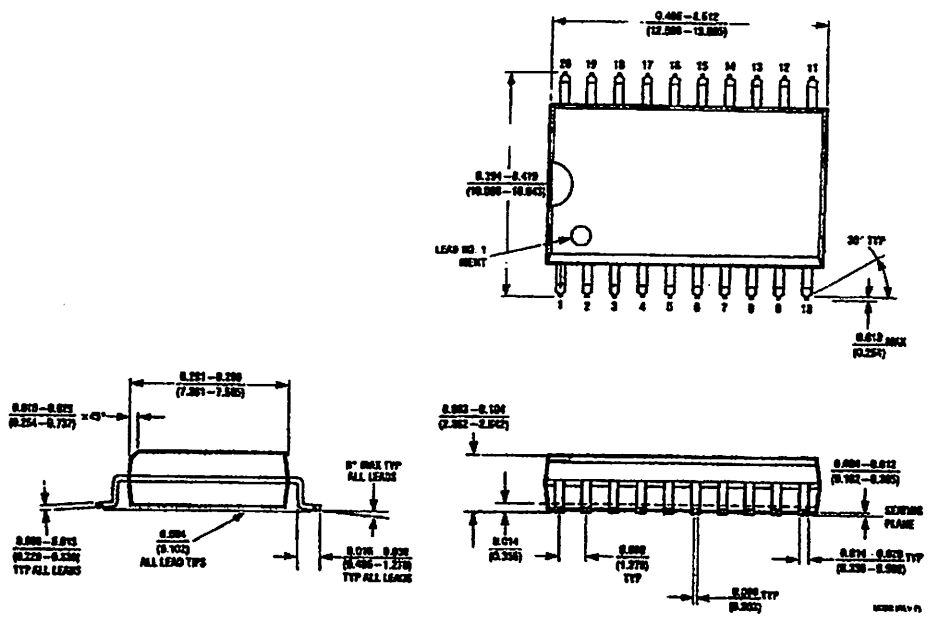
The two-key roll-over feature can be illustrated by assuming a key is depressed, and then a second key is depressed. Since all scanning has stopped, and all other Y inputs are disabled, the second key is not recognized until the first key is lifted and the key bounce circuitry has reset.

The output latches feed 3-STATE, which is enabled when the Output Enable ($\overline{OE}$) input is taken low.

Physical Dimensions inches (millimeters) unless otherwise noted

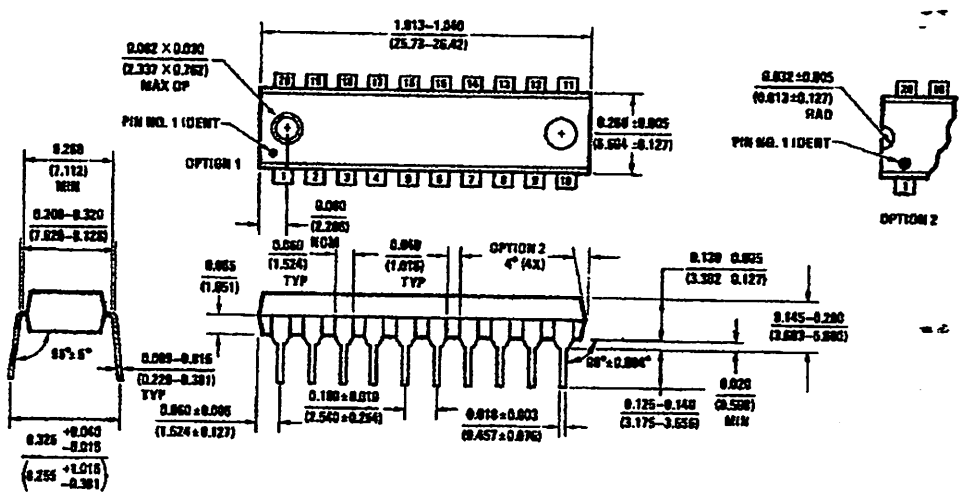


18-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300" Wide
Package Number N18A



20-Lead Plastic Small Outline I.C. Package (M)
Package Number M20B

Physical Dimensions inches (millimeters) unless otherwise noted (Continued)



20-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300" Wide
Package Number N20A

SN74LS164

Serial-In Parallel-Out Shift Register

The SN74LS164 is a high speed 8-Bit Serial-In Parallel-Out Shift Register. Serial data is entered through a 2-Input AND gate synchronous with the LOW to HIGH transition of the clock. The device features an asynchronous Master Reset which clears the register setting all outputs LOW independent of the clock. It utilizes the Schottky diode clamped process to achieve high speeds and is fully compatible with all ON Semiconductor TTL products.

- Typical Shift Frequency of 35 MHz
- Asynchronous Master Reset
- Gated Serial Data Input
- Fully Synchronous Data Transfers
- Input Clamp Diodes Limit High Speed Termination Effects
- ESD > 3500 Volts

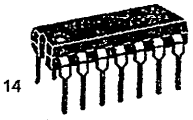
GUARANTEED OPERATING RANGES

Symbol	Parameter	Min	Typ	Max	Unit
V_{CC}	Supply Voltage	4.75	5.0	5.25	V
T_A	Operating Ambient Temperature Range	0	25	70	°C
I_{OH}	Output Current – High			–0.4	mA
I_{OL}	Output Current – Low			8.0	mA

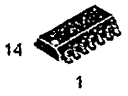
ON Semiconductor

http://onsemi.com

LOW POWER SCHOTTKY



PLASTIC
N SUFFIX
CASE 646

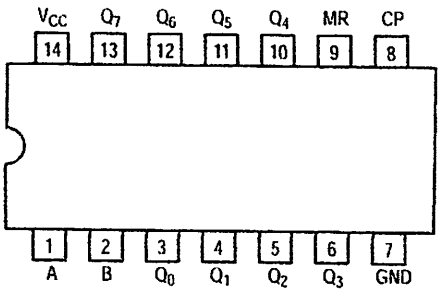


SOIC
D SUFFIX
CASE 751A

ORDERING INFORMATION

Device	Package	Shipping
SN74LS164N	14 Pin DIP	2000 Units/Box
SN74LS164D	14 Pin	2500/Tape & Reel

CONNECTION DIAGRAM DIP (TOP VIEW)

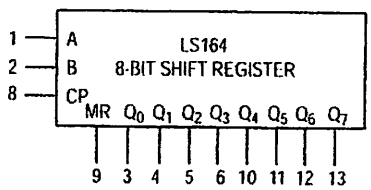


NOTE:
The Flatpak version has the same pinouts (Connection Diagram) as the Dual In-Line Package.

PIN NAMES		LOADING (Note a) HIGH	LOW
A, B	Data Inputs	0.5 U.L.	0.25 U.L.
CP	Clock (Active HIGH Going Edge) Input	0.5 U.L.	0.25 U.L.
$\overline{MR}$	Master Reset (Active LOW) Input	0.5 U.L.	0.25 U.L.
$Q_0 - Q_7$	Outputs	10 U.L.	5 U.L.

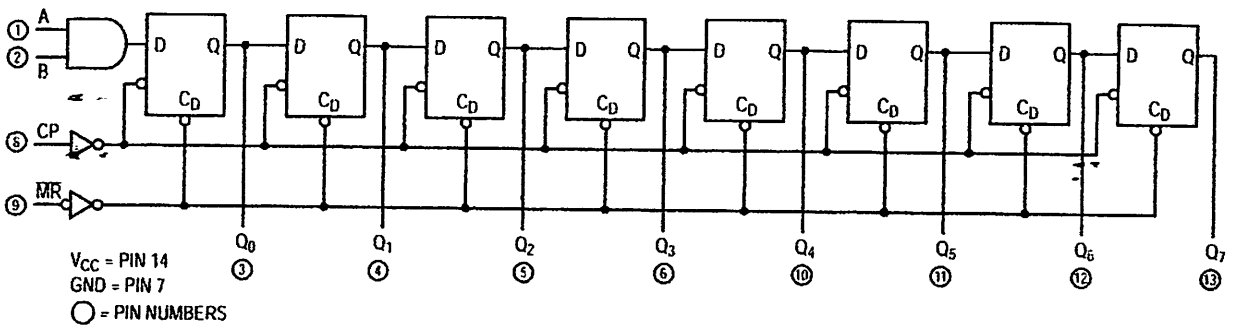
NOTES:
a) 1 TTL Unit Load (U.L.) = 40 μA HIGH/1.6 mA LOW.

LOGIC SYMBOL



V_{CC} = PIN 14
GND = PIN 7

LOGIC DIAGRAM



FUNCTIONAL DESCRIPTION

The LS164 is an edge-triggered 8-bit shift register with serial data entry and an output from each of the eight stages. Data is entered serially through one of two inputs (A or B); either of these inputs can be used as an active HIGH Enable for data entry through the other input. An unused input must be tied HIGH, or both inputs connected together.

Each LOW-to-HIGH transition on the Clock (CP) input shifts data one place to the right and enters into Q_0 the logical AND of the two data inputs (A•B) that existed before the rising clock edge. A LOW level on the Master Reset ($\overline{MR}$) input overrides all other inputs and clears the register asynchronously, forcing all Q outputs LOW.

MODE SELECT — TRUTH TABLE

OPERATING MODE	INPUTS			OUTPUTS	
	MR	A	B	Q_0	Q_1–Q_7
Reset (Clear)	L	X	X	L	L – L
Shift	H	l	l	L	$q_0 - q_6$
	H	l	h	L	$q_0 - q_6$
	H	h	l	L	$q_0 - q_6$
	H	h	h	H	$q_0 - q_6$

L (l) = LOW Voltage Levels
H (h) = HIGH Voltage Levels
X = Don't Care
q_n = Lower case letters indicate the state of the referenced input or output one set-up time prior to the LOW to HIGH clock transition.

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

Symbol	Parameter	Limits Min	Typ	Max	Unit	Test Conditions	
V_{IH}	Input HIGH Voltage	2.0			V	Guaranteed Input HIGH Voltage for All Inputs	
V_{IL}	Input LOW Voltage			0.8	V	Guaranteed Input LOW Voltage for All Inputs	
V_{IK}	Input Clamp Diode Voltage		−0.65	−1.5	V	V_{CC} = MIN, I_{IN} = −18 mA	
V_{OH}	Output HIGH Voltage	2.7	3.5		V	V_{CC} = MIN, I_{OH} = MAX, V_{IN} = V_{IH} or V_{IL} per Truth Table	
V_{OL}	Output LOW Voltage		0.25	0.4	V	I_{OL} = 4.0 mA	V_{CC} = V_{CC} MIN, V_{IN} = V_{IH} or V_{IL} per Truth Table
			0.35	0.5	V	I_{OL} = 8.0 mA	
I_{IH}	Input HIGH Current			20	μA	V_{CC} = MAX, V_{IN} = 2.7 V	
				0.1	mA	V_{CC} = MAX, V_{IN} = 7.0 V	
I_{IL}	Input LOW Current			−0.4	mA	V_{CC} = MAX, V_{IN} = 0.4 V	
I_{OS}	Short Circuit Current (Note 1)	−20		−100	mA	V_{CC} = MAX	
I_{CC}	Power Supply Current			27	mA	V_{CC} = MAX	

Note 1: Not more than one output should be shorted at a time, nor for more than 1 second.

AC CHARACTERISTICS (T_A = 25°C)

Symbol	Parameter	Limits Min	Typ	Max	Unit	Test Conditions
f_{MAX}	Maximum Clock Frequency	25	36		MHz	V_{CC} = 5.0 V C_L = 15 pF
t_{PHL}	Propagation Delay $\overline{MR}$ to Output Q		24	36	ns	
t_{PLH} t_{PHL}	Propagation Delay Clock to Output Q		17 21	27 32	ns	

AC SETUP REQUIREMENTS (T_A = 25°C)

Symbol	Parameter	Limits Min	Typ	Max	Unit	Test Conditions
t_w	CP, $\overline{MR}$ Pulse Width	20			ns	V_{CC} = 5.0 V
t_s	Data Setup Time	15			ns	
t_h	Data Hold Time	5.0			ns	
t_{rec}	$\overline{MR}$ to Clock Recovery Time	20			ns	

AC WAVEFORMS

*The shaded areas indicate when the input is permitted to change for predictable output performance.

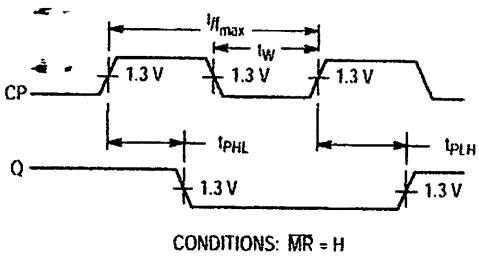


Figure 1. Clock to Output Delays and Clock Pulse Width

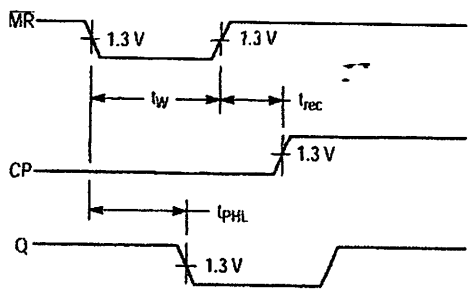


Figure 2. Master Reset Pulse Width, Master Reset to Output Delay and Master Reset to Clock Recovery Time

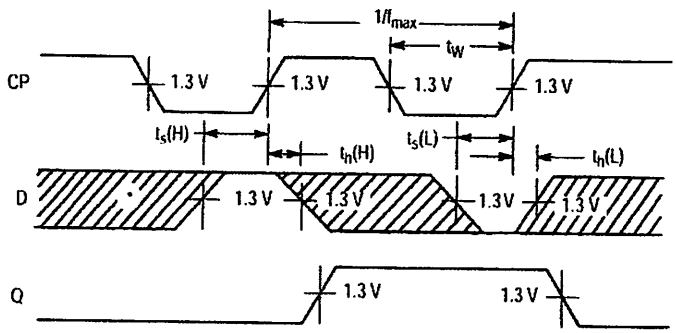
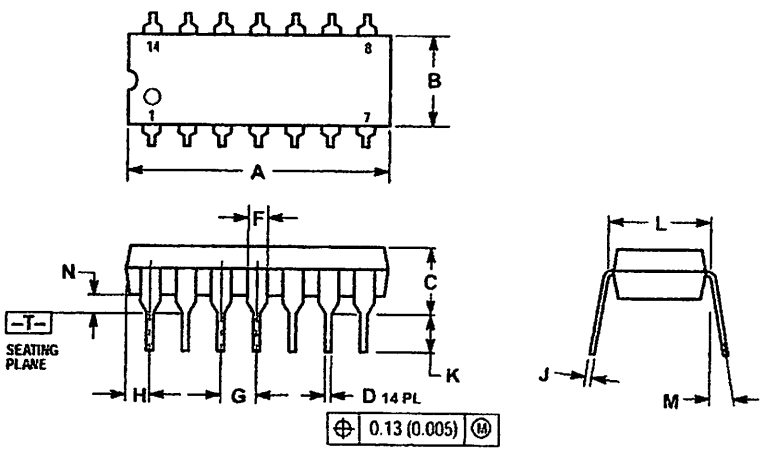


Figure 3. Data Setup and Hold Times

PACKAGE DIMENSIONS

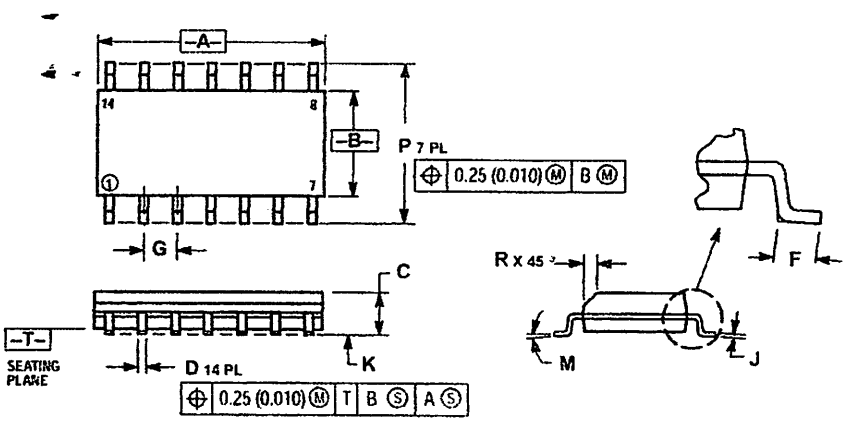
N SUFFIX
PLASTIC PACKAGE
CASE 646–06
ISSUE M



NOTES.
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. DIMENSION L TO CENTER OF LEADS WHEN FORMED PARALLEL.
4. DIMENSION B DOES NOT INCLUDE MOLD FLASH.
5. ROUNDED CORNERS OPTIONAL.

	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	0.715	0.770	18.16	18.80
B	0.240	0.260	6.10	6.60
C	0.145	0.185	3.69	4.69
D	0.015	0.021	0.38	0.53
F	0.040	0.070	1.02	1.78
G	0.100 BSC		2.54 BSC	
H	0.052	0.095	1.32	2.41
J	0.008	0.015	0.20	0.38
K	0.115	0.135	2.92	3.43
L	0.290	0.310	7.37	7.87
M	---	10°	---	10°
N	0.015	0.039	0.38	1.01

D SUFFIX
PLASTIC SOIC PACKAGE
CASE 751A–03
ISSUE F



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSIONS A AND B DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
5. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127 (0.005) TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	8.55	8.75	0.337	0.344
B	3.80	4.00	0.150	0.157
C	1.35	1.75	0.054	0.068
D	0.35	0.49	0.014	0.019
F	0.40	1.25	0.016	0.049
G	1.27 BSC		0.050 BSC	
J	0.19	0.25	0.008	0.009
K	0.10	0.25	0.004	0.009
M	0°	7°	0°	7°
P	5.80	6.20	0.228	0.244
R	0.25	0.50	0.010	0.019

PUBLICATION ORDERING INFORMATION

North America Literature Fulfillment:
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Email: r14153@onsemi.com

Fax Response Line: 303–675–2167
800–344–3810 Toll Free USA/Canada

ON Semiconductor Website: http://onsemi.com

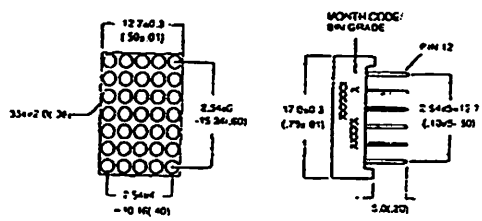
For additional information, please contact your local
Sales Representative.

FAIRCHILD
SEMICONDUCTOR

0.7" 5×7 DOT MATRIX DISPLAYS

HER GMA7175C GMC7175C
YELLOW GMA7475C GMC7475C
GREEN GMA7975C GMC7975C

PACKAGE DIMENSIONS



ST2618

NOTES:
1. ALL PINS ARE ø0.5 (.02).
2. DIMENSION IN MILLIMETERS (INCH). TOLERANCE IS 0.25 (.01) UNLESS OTHERWISE NOTED.

DESCRIPTION

The GMX7X75C series are 0.7" (17.2mm) matrix height 5 X 7 dot matrix displays. All these parts are available in grey face and white dot color.

The X in GMX denotes row anode or row cathode.

FEATURES

- 0.7" (17.8mm) matrix height
- Choice of 3 colors — green, yellow and HER
- Low power consumption
- 5×7 array with X-Y select
- Stackable vertically and horizontally
- Choice of 2 matrix orientation cathode column or anode column
- Easy mounting on PCB or socket
- Categorized for luminous intensity

ABSOLUTE MAXIMUM RATING (Ta=25°C unless otherwise specified)

	YELLOW	HER	GREEN	UNITS
Power dissipation per dot	60	70	75	mW
Peak forward current per dot (Duty cycle 1/10, 10KHz)	80	100	100	mA
Continuous I, per dot	20	25	25	mA
Reverse voltage per dot	5	5	5	V
Operating and operating temperature range				−25°C to +85°C
Soldering time at 260°C (1/16 inch below seating plane)				3 sec

FAIRCHILD
SEMICONDUCTOR

0.7" 5×7
DOT MATRIX DISPLAYS

ELECTRICAL/OPTICAL CHARACTERISTICS (T_A=25°C unless otherwise specified)

PARAMETER	MIN	TYP	MAX	UNITS	TEST CONDITIONS
Average luminous intensity		3000		µcd	I_F=20 mA
Peak emission wavelength		635		nm	I_F=20 mA
Spectral line half-width		40		nm	I_F=20 mA
Forward voltage, any dot		2.1	2.8	V	I_F=20 mA
Reverse voltage, any dot			100	µA	V_R=5V

TYPICAL ELECTRICAL/OPTICAL CHARACTERISTIC CURVES
(T_A=25°C Unless otherwise specified)

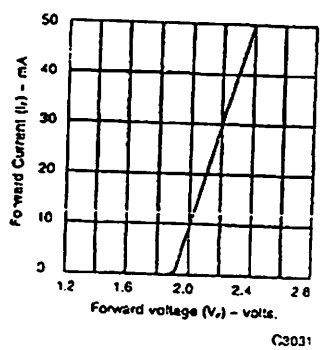


Fig. 1. Forward Current vs. Forward Voltage

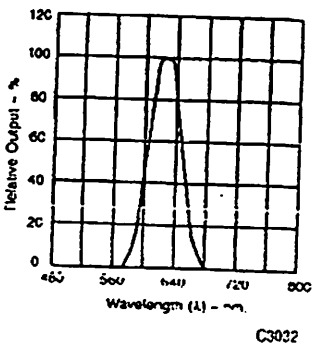


Fig. 2. Spectral Response

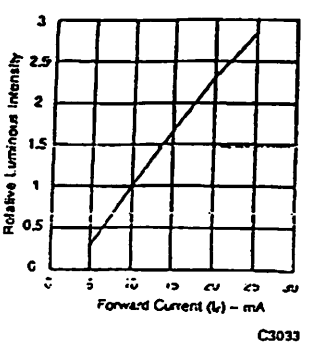


Fig. 3. Relative Luminous Intensity vs. Forward Current (Per Segment)

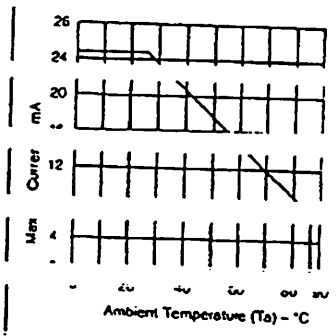


Fig. 4. Max. Forward Allowable DC Current Per Seg. vs.

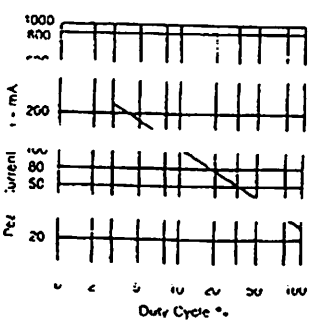


Fig. 5. Max. Peak Current vs. Duty Circle %

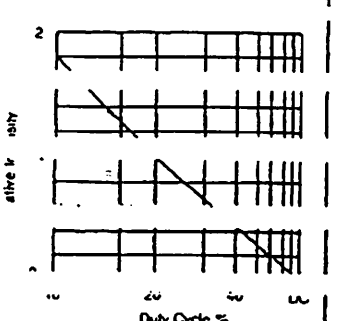


Fig. 6. Luminous Intensity vs. Duty Cycle %

FAIRCHILD
SEMICONDUCTOR

0.7" 5×7
DOT MATRIX DISPLAYS

ELECTRICAL/OPTICAL CHARACTERISTICS (T$_A$=25°C unless otherwise specified)
FLMX-7475C (RED)

PARAMETER	MIN	TYP	MAX	UNITS	TEST CONDITIONS
Average luminous intensity		3000		µcd	I_F=20 mA
Peak emission wavelength		585		nm	I_F=20 mA
Spectral line half-width		35		nm	I_F=20 mA
Forward voltage, any dot		2.1	2.8	V	I_F=20 mA
Reverse voltage, any dot			100	µA	V_R=5V

TYPICAL ELECTRICAL/OPTICAL CHARACTERISTIC CURVES

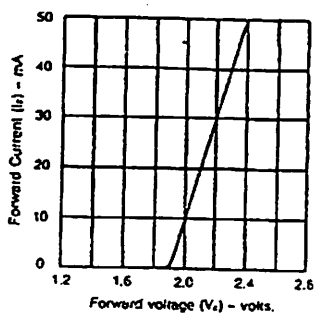


Fig. 1. Forward Current vs. Forward Voltage

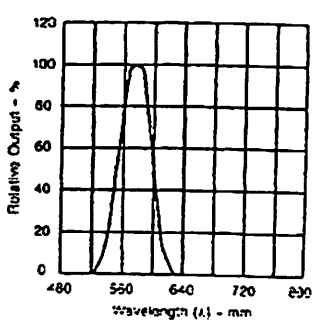


Fig. 2. Spectral Response

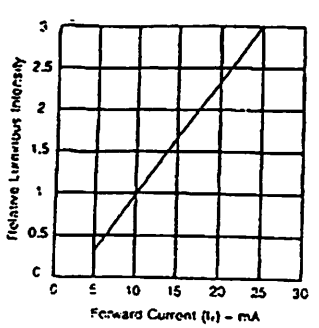


Fig. 3. Relative Luminous Intensity vs Forward Current (Per Segment)

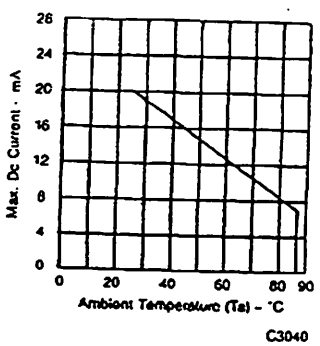


Fig. 4. Max. Forward Allowable DC Current Per Seg. vs. Ambient Temperature

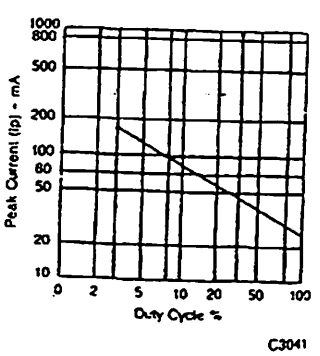


Fig. 5. Max. Peak Current vs. Duty Circle % (Refresh Rate – F = 1 KHz)

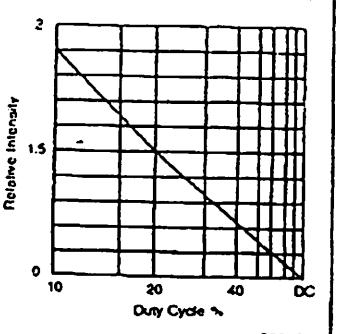


Fig. 6. Luminous Intensity vs. Duty Cycle % (Average I = 10 mA Per Seg.)

FAIRCHILD
SEMICONDUCTOR

0.7" 5x7 DOT MATRIX DISPLAYS

ELECTRICAL/OPTICAL CHARACTERISTICS (T_A=25°C Unless otherwise specified)
GMIX7975G (GREEN)

PARAMETER	MIN	TYP	MAX	UNITS	TEST CONDITIONS
Average luminous intensity		3000		µcd	I_F=20 mA
Peak emission wavelength		565		nm	I_F=20 mA
Spectral line half-width		30		nm	I_F=20 mA
Forward voltage, any dot		2.1	2.8	V	I_F=20 mA
Reverse voltage, any dot			100	µA	V_R=5V

TYPICAL ELECTRICAL/OPTICAL CHARACTERISTIC CURVES
(Ta=25°C Unless Otherwise Specified)

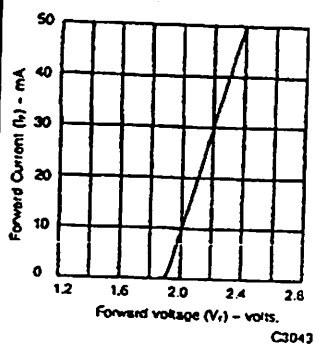


Fig. 1. Forward Current vs. Forward Voltage

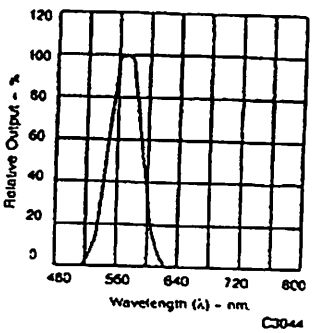


Fig. 2. Spectral Response

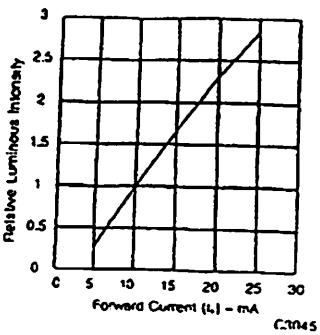


Fig. 3 Relative Luminous Intensity vs. Forward Current (Per Segment)

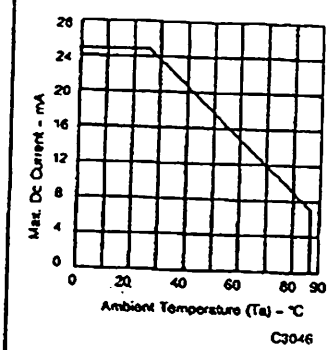


Fig. 4. Max. Forward Allowable DC Current Per Seg. vs. Ambient Temperature

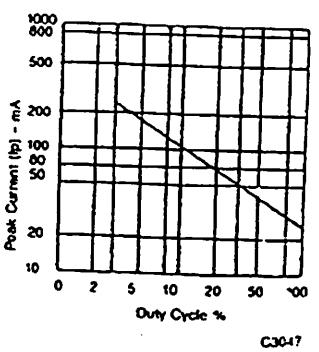


Fig. 5. Max. Peak Current vs. Duty Circle % (Refresh Rate=F=1 KHz)

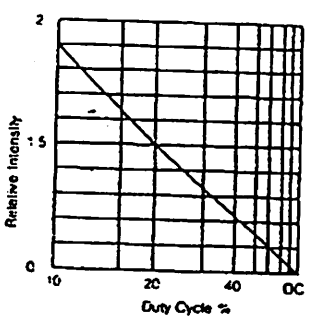


Fig. 6. Luminous Intensity vs. Duty Cycle % (Average I=10 mA Per Seg.)

FAIRCHILD
SEMICONDUCTOR

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2. A critical component in any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

FAIRCHILD
SEMICONDUCTOR™

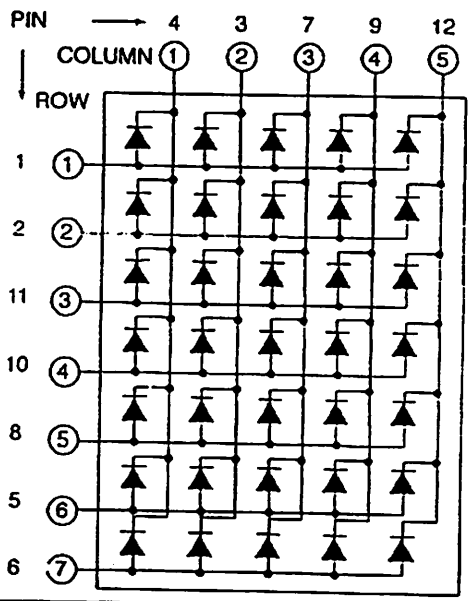
0.7" 5×7 DOT MATRIX DISPLAYS

PIN CONNECTION

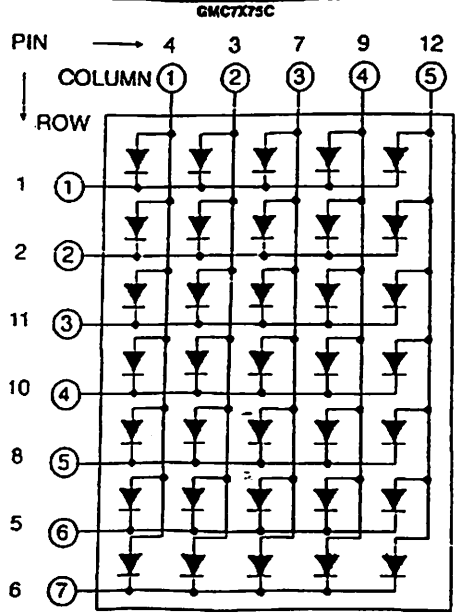
PIN NO.	GMA7X7SC	GMC7X7SC
1	Anode row 1	Cathode row 1
2	Anode row 2	Cathode row 2
3	Cathode column 2	Anode column 2
4	Cathode column 1	Anode column 1
5	Anode row 6	Cathode row 6
6	Anode row 7	Cathode row 7
7	Cathode column 3	Anode column 3
8	Anode row 5	Cathode row 5
9	Cathode column 4	Anode column 4
10	Anode row 4	Cathode row 4
11	Cathode row 3	Anode row 3
12	Cathode row 5	Anode row 5

INTERNAL CIRCUIT DIAGRAM

GMA7X7SC



GMC7X7SC



PRELIMINARY DATA SHEET

INFORMATION STORAGE DEVICES

ISD1200/1400 Series

Single-Chip Voice Record/Playback Devices 10-, 12, 16, and 20-Second Durations

GENERAL DESCRIPTION

Information Storage Devices' ISD1200/1400 ChipCorder™ Series provides high-quality, single-chip record/playback solutions to short duration messaging applications. The CMOS devices include an on-chip oscillator, microphone pre-amplifier, automatic gain control, antialiasing filter, smoothing filter, and speaker amplifier. A minimum record/playback subsystem can be configured with a microphone, a speaker, several passives, two push-buttons, and a power source.

Recordings are stored in nonvolatile memory cells, providing zero-power message storage. This unique solution is made possible through ISD's patented Direct Analog Storage Technology (DAST™), whereby voice and audio signals are stored directly, in their natural analog form, into EEPROM memory. Direct analog storage allows natural voice reproduction in a single-chip solid-state solution.

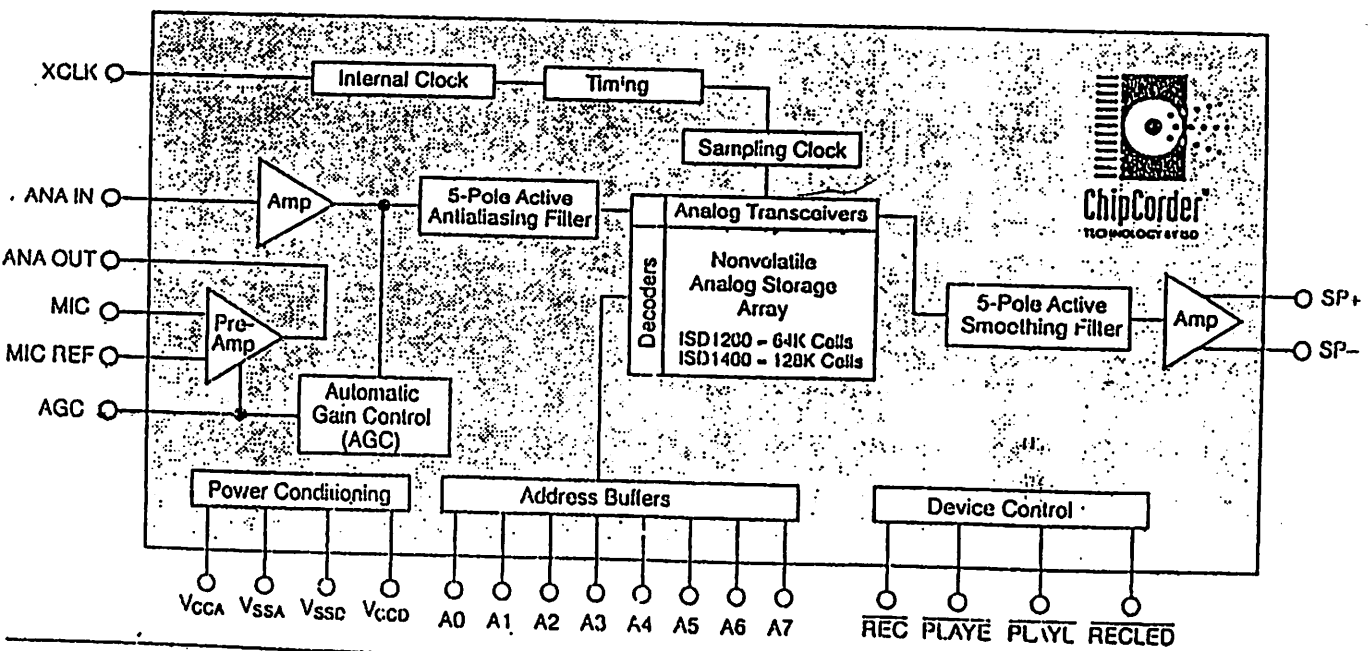
ISD1200/1400 SERIES SUMMARY

Part Number	Minimum Duration (Seconds)	Maximum Input Sample Rate (KHz)	Upper Pass Band (KHz)
ISD1210	10	6.4	2.7
ISD1212	12	5.3	2.3
ISD1416	16	8.0	3.4
ISD1420	20	6.4	2.7

FEATURES

- Easy-to-use single-chip voice record/playback solution
  - No external ICs required
  - Minimizes external components
- High-quality, natural voice/audio reproduction
- Push-button interface
  - Playback can be edge- or level-activated
- Zero-power message storage
  - Eliminates battery backup circuits
- 100-year message retention (typical)
- 100 K record cycles (typical)
- On-chip clock source
- No programmer or development system needed
- Fully addressable to handle multiple messages
- Automatic power-down mode
  - Enters standby mode immediately following a record or playback cycle
  - 0.5 uA standby current (typical)
- Single power supply
- Available in DIP, SOIC, and die form for Chip-on-Board (COB) Module assembly

ISD1200/1400 SERIES BLOCK DIAGRAM



DETAILED DESCRIPTION

Basic Operation

The ISD1200/1400 ChipCorder Series devices are controlled by a single signal, $\overline{REC}$, and either of two push-button control playback signals, $\overline{PLAYE}$ (edge-activated playback), and $\overline{PLAYL}$ (level-activated playback). The ISD1200/1400 parts are configured for simplicity of design in a single-message application. Using the address lines will allow multiple message applications. Device operation is explained on page 4.

Speech Quality

ISD's patented DAST technology provides natural record and playback. The input voice signals are stored directly in nonvolatile EEPROM cells, and reproduced without the synthetic effect often heard with digital solid-state speech solutions. A complete sample is stored in a single cell, minimizing the memory necessary to store a recording of a given duration.

Automatic Power-Down Mode

At the end of a playback or record cycle, the ISD1200/1400 Series devices automatically return to a low-power standby mode, consuming typically 0.5 µA. During a playback cycle, the device powers down automatically at the end of the message. During a record cycle, the device powers down immediately after $\overline{REC}$ is released HIGH.

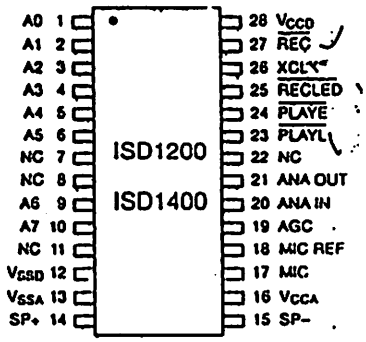
Addressing (optional)

In addition to providing simple message playback, the ISD1200/1400 Series provides a full addressing capability.

The ISD1200 Series storage array has 80 distinct addressable segments, while the ISD1400 Series storage array has 160 distinct addressable segments, providing the following resolutions.

Part Number	Resolution
ISD1210	125 ms
ISD1212	150 ms
ISD1416	100 ms
ISD1420	125 ms

ISD1200/1400 SERIES PINOUTS



Note: NC means Must Not Connect

PIN DESCRIPTIONS

Note: The $\overline{REC}$, $\overline{PLAYL}$, and $\overline{PLAYE}$ signals are all debounced for 50 ms. on the rising edge to prevent a false retriggering from a push-button switch.

Record ($\overline{REC}$)

The $\overline{REC}$ input is an active-LOW record signal. The device records whenever $\overline{REC}$ is LOW. This signal must remain LOW for the duration of the recording. $\overline{REC}$ takes precedence over either playback ($\overline{PLAYE}$ or $\overline{PLAYL}$) signal. If $\overline{REC}$ is pulled LOW during a playback cycle, the playback immediately ceases and recording begins.

A record cycle is completed when $\overline{REC}$ is pulled HIGH. An end-of-message marker is internally recorded, enabling a subsequent playback cycle to terminate appropriately. The device automatically powers down to standby mode when $\overline{REC}$ goes HIGH.

Playback, Edge-Activated ($\overline{PLAYE}$)

When a LOW-going transition is detected on this input signal, a playback cycle begins. Playback continues until an end-of-message marker is encountered or the end of the memory space is reached. Upon completion of the playback cycle, the device automatically powers down into standby mode. Taking $\overline{PLAYE}$ HIGH during a playback cycle will not terminate the current cycle.

Playback, Level-Activated ($\overline{PLAYL}$)

When this input signal transitions from HIGH to LOW, a playback cycle is initiated. Playback continues until $\overline{PLAYL}$ is pulled HIGH, an end-of-message marker is detected, or the end of the device space is reached. The device automatically powers down to standby mode upon completion of the playback cycle.

Note: In playback, if either $\overline{PLAYE}$ or $\overline{PLAYL}$ is held LOW during $\overline{EOM}$ or OVERFLOW, the device will still enter standby and the internal oscillator and timing generator

will stop. However, the rising edge of $\overline{\text{PLAYE}}$ and $\overline{\text{PLAYL}}$ will no longer be debounced and any subsequent falling edge present on the input pins will initiate another playback.

Record LED Output ($\overline{\text{RECLED}}$)

The output $\overline{\text{RECLED}}$ is LOW during a record cycle. It can be used to drive an LED to provide feedback that a record cycle is in progress. In addition, $\overline{\text{RECLED}}$ pulses LOW momentarily when an end-of-message marker is encountered in a playback cycle.

Microphone Input (MIC)

The microphone is usually AC-coupled to this pin via a series capacitor. The user-selectable value of the input series capacitor (together with the 10K ohm resistance internal to the chip) determines the low-frequency cutoff for the ISD1200/1400 Series passband.

Microphone Reference (MIC REF)

When MICREF is AC coupled to the microphone ground, the recorded noise level is significantly reduced. Ground noise is referenced to the preamplifier. If this pin is not used, it must NOT be connected to any signal or voltage. It must float.

Analog Output (ANA OUT)

The microphone signal is amplified and is output to the ANA OUT pin. The voltage gain of the preamp is determined by the voltage level at the Automatic Gain Control (AGC) pin. The preamplifier has a maximum gain of about 24 dB for small input signal levels.

Analog Input (ANA IN)

The external capacitor connects ANA IN to the ANA OUT pin. The value of the external capacitor, together with the 3 KΩ input impedance at ANA IN, can be chosen to give additional cutoff at the low-frequency end of the voice passband. The ANA IN pin may also be used to input alternative sources of analog signals (instead of the microphone signal) through a coupling capacitor.

Automatic Gain Control (AGC)

The purpose of the AGC is to dynamically adjust the preamplifier gain, and therefore extend the range of input signals which can be applied to the microphone input without causing distortion. The AGC can considerably extend the range of recordable sound from whispers to loud voices. To use the AGC feature, an external resistor and capacitor should be connected in parallel between the AGC pin and Ground. Recommended values are 470 KΩ and 4.7 µF. The "attack" time of the gain control is determined by the source resistance (5 KΩ) and the external capacitor. The "release" time is determined by the external resistor and capacitor. For AGC voltages of 1.5 Volts and below, the preamplifier is at its maximum gain of 24 dB. Reduction in preamplifier gain occurs for voltages of approximately 1.8 Volts. If the AGC function is not desired, the AGC pin can be tied to Ground and the preamplifier gain will be held at its highest level of approximately 24 dB.

If operating at voltages above 5.5 V, insert a 5.1 KΩ resistor in series with the capacitor from pin 20 to pin 21 to minimize distortion.

Speaker Outputs (SP+, SP–)

The SP+ and SP– pins provide direct drive for loudspeakers with impedances as low as 16 ohms. A single output may be used, but, for direct-drive loudspeakers, the two opposite-polarity outputs provide an improvement in output power of up to four times over a single-ended connection. Furthermore, when SP+ and SP– are used, a speaker-coupling capacitor is not required. A single-ended connection will require an AC-coupling capacitor between the SP pin and the speaker. The speaker outputs are in a high-impedance state during a record cycle, and held at V_{SSA} during Power Down.

Optional External Clock (XCLK)

This signal is normally tied to ground in applications circuits. If, however, greater timing precision is desired, (internal clock has ±2.5 % tolerance over temperature and voltage range), the chip can be externally clocked through this pin. If the XCLK is not used, this input should be connected to ground.

V_{CCA} and V_{CCD}

Analog and digital circuits internal to the ISD1200/1400 Series use separate power buses to minimize noise on the chip. These power buses are brought out to separate pins on the package and should be tied together as close to the supply as possible. It is important that the power supply be decoupled as close as possible to the package.

V_{SSA} and V_{SSD} (Ground)

Similar to V_{CCA} and V_{CCD}, the analog and digital circuits internal to the ISD1200/1400 Series use separate ground buses to minimize noise. These pins should be tied together as close as possible to the device.

TABLE 1. OPERATIONAL MODES

Address Ctrl. (HIGH)	Function	Typical Use	Jointly* Compatible
A0	Message cueing	Fast-forward through messages	A4
A1	Delete $\overline{EOM}$ markers	Position $\overline{EOM}$ marker at the end of the last message	A3, A4
A2	Unused		
A3	Looping	Continuous playback from Address 0	A1
A4	Consecutive addressing	Record/Play multiple consecutive messages	A0, A1
A5	Unused		

** Indicates additional operational modes which can be used simultaneously with the given mode.*

Address Inputs (A0-A7)

The Address Inputs have two functions, depending upon the level of the two Most Significant Bits (MSB) of the address.

If either of the two MSBs is LOW, the inputs are ALL interpreted as address bits and are used as the start address for the current Record or Playback cycle. The address pins are inputs only and do not output internal address information as the operation progresses. Address inputs are latched by the falling edge of $\overline{PLAYE}$, $\overline{PLAYL}$ or $\overline{REC}$.

OPERATIONAL MODES

The ISD1200/1400 Series is designed with several built-in operational modes provided to allow maximum functionality with a minimum of additional components, described in detail below. The operational modes use the address pins on the ISD1200/1400 devices, but are mapped outside the valid address range. When the two Most Significant Bits (MSBs) are HIGH, the remaining address signals are interpreted as mode bits and NOT as address bits. Therefore, operational modes and direct addressing are not compatible and cannot be used simultaneously.

There are two important considerations for using operational modes. First, all operations begin initially at address 0, which is the beginning of the ISD1200/1400 address space. Later operations can begin at other address locations, depending on the operational mode(s) chosen. In addition, the address pointer is reset to 0 when the device is changed from Record to Playback, Playback to Record, or when a Power-Down cycle is executed.

Second, an Operational Mode is executed when any of the control inputs, $\overline{PLAYE}$, $\overline{PLAYL}$, or $\overline{REC}$, go LOW and the two MSBs are HIGH. This Operational Mode remains in effect until the next LOW-going control input signal, at which point the current address/mode levels are sampled and executed.

(Note: The two MSBs are on pins 9 and 10 for each ISD1200/1400 Series member.)

OPERATIONAL MODE DESCRIPTIONS

The Operational Modes can be used in conjunction with a microcontroller, or they can be hard-wired to provide the desired system operation.

A0 — Message Cueing ($\overline{PLAYE}$ or $\overline{PLAYL}$ only)

Message Cueing allows the user to skip through messages, without knowing the actual physical addresses of each message. Each control input LOW pulse causes the internal address pointer to skip to the next message. This mode should be used for Playback only, and is typically used with the A4 Operational Mode.

A1 — Delete $\overline{EOM}$ Markers ($\overline{REC}$ only)

The A1 Operational Mode allows sequentially recorded messages to be concatenated into a single message with only one $\overline{EOM}$ marker set at the end of the combined message. When this operational mode is configured, messages recorded sequentially are played back as one continuous message.

A2 — Unused

A3 — Message Looping ($\overline{PLAYE}$ or $\overline{PLAYL}$ only)

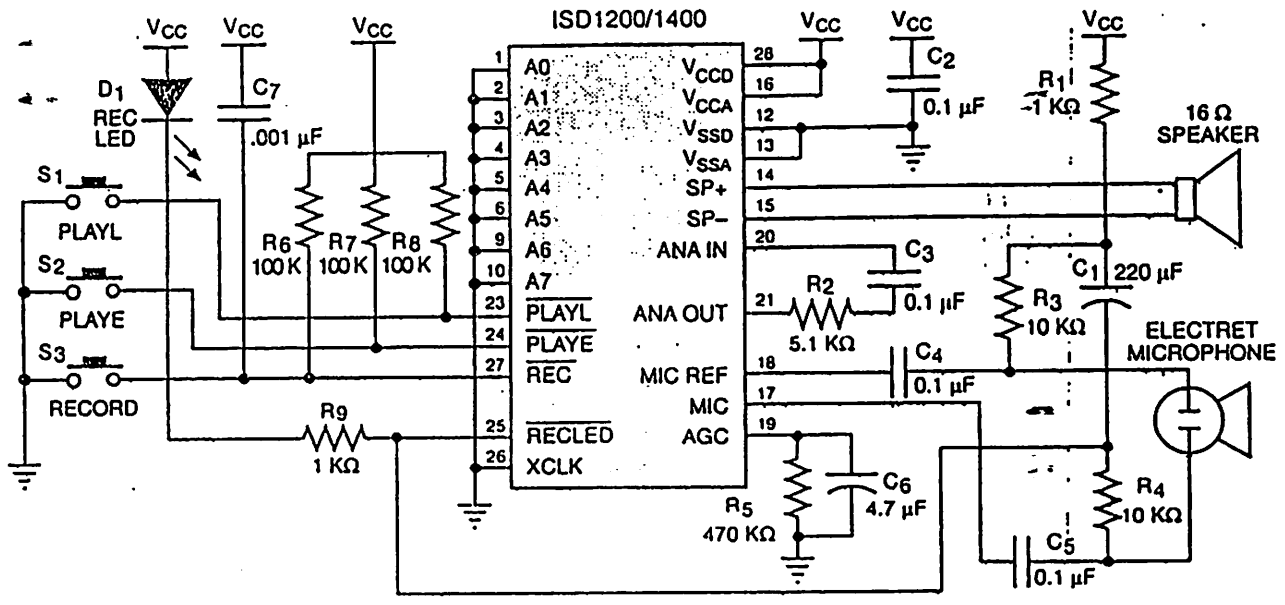
The A3 Operational Mode allows for the automatic, continuously repeated playback of the message located at the beginning of the address space. A message CAN completely fill the ISD1200/1400 device and will loop from beginning to end.

A4 — Consecutive Addressing

During normal operations, the address pointer will reset when a message is played through to an $\overline{EOM}$ marker. The A4 Operational Mode inhibits the address pointer reset, allowing messages to be played back consecutively.

A5 — Unused

APPLICATION SCHEMATIC



Note: ISD Application Notes and Design Manual available

FUNCTIONAL DESCRIPTION EXAMPLE

The following example operating sequence demonstrates the functionality of the ISD1200/1400 Series devices.

1. Record a message filling the address space.

Pulling the $\overline{\text{REC}}$ signal LOW initiates a record cycle from the beginning of the message space. If $\overline{\text{REC}}$ is held LOW, the recording continues until the message space has been filled. Once the message space is filled, recording ceases. The device will automatically power down after $\overline{\text{REC}}$ is pulled HIGH.

2. Edge-activated playback.

Pulling the $\overline{\text{PLAYE}}$ signal LOW initiates a playback cycle from the beginning of the message space. The rising edge of $\overline{\text{PLAYE}}$ has no effect on operation. If a recording has filled the message space, the entire message is played. When the device reaches the end of the message space, it automatically powers down. A subsequent falling edge on $\overline{\text{PLAYE}}$ initiates a new play cycle from the start address.

3. Level-activated playback.

Pulling the $\overline{\text{PLAYL}}$ signal LOW initiates a playback cycle from the beginning of the message space. If $\overline{\text{PLAYL}}$ remains LOW, the device plays through to the end of the message and subsequently enters the power-down mode.

4. Level-activated playback (truncated).

If $\overline{\text{PLAYL}}$ is pulled HIGH any time during the play- back cycle, the device stops playing and enters the power-down mode. A subsequent falling edge on $\overline{\text{PLAYL}}$ initiates a new play cycle from the start address.

5. Record (interrupting playback).

The $\overline{\text{REC}}$ signal takes precedence over other operations. Any LOW-going transition on $\overline{\text{REC}}$ initiates a new record operation from the beginning of the start address, regardless of any current operation in progress.

6. Record a message, partially filling the address space.

A record operation need not fill the entire message space. Releasing the $\overline{\text{REC}}$ signal HIGH before filling the message space causes the recording to stop and an end-of-message marker to be placed. The device powers down automatically.

7. Play back a message, partially filling the address space.

Pulling the $\overline{\text{PLAYE}}$ or $\overline{\text{PLAYL}}$ signal LOW initiates a playback cycle which is then completed when the end-of-message marker is encountered. Playback ceases and the device powers down.

8. $\overline{\text{RECLED}}$ operation.

The $\overline{\text{RECLED}}$ output pin provides an active-LOW signal which can be used to drive an LED as a "record in progress" indicator. It returns to a HIGH state when the $\overline{\text{REC}}$ pin is released HIGH or when the recording is completed due to the message space being filled.

APPLICATIONS NOTE

Some users may experience an unexpected recording taking place when their circuit is powered up, or the batteries are changed and V_{CC} rises faster than REC. This undesired recording prevents playback of the previously recorded message. A spurious End Of Message ($\overline{EOM}$) marker appears at the very beginning of the memory, preventing access to the original message, and nothing is played.

To prevent this occurrence, place a capacitor (approx. .001 µF) between the control pin ($\overline{REC}$) and V_{CC}. This pulls the control pin voltage up with V_{CC} as it rises. Once the voltage is HIGH, the pull-up device will keep the pin HIGH until intentionally pulled LOW, preventing the false $\overline{EOM}$ marker.

Since this anomaly is dependent upon factors such as the capacitance of the user's printed circuit board, not all circuit designs will exhibit the spurious marker. It is recommended, however, that the capacitor is included for design reliability. A more detailed explanation and resolution of this occurrence is described in the ISD Application Notes and Design Manual.

ABSOLUTE MAXIMUM RATINGS (ISD1200/1400 SERIES – PACKAGED)

Condition	Value
Temperature under bias	- 65° C to + 125° C
Storage temperature range	- 65° C to + 150° C
Voltage applied to any pin	(V_{SS} - 0.3 V) to (V_{CC} + 0.3 V)
Voltage applied to any pin (Input current limited to ± 20 mA)	(V_{SS} - 1.0 V) to (V_{CC} + 1.0 V)
Lead temperature (soldering - 10 seconds)	300° C
V_{CC} - V_{SS}	- 0.3 V to + 7.0 V

Stresses above those listed may cause permanent damage to the device. Exposure to the absolute maximum ratings may affect device reliability.

DC PARAMETERS (ISD1200/1400 SERIES – PACKAGED)

Operating Conditions: T_A = 0° to 70° C, V_{CC} = 4.5 V to 6.5 V (1), V_{SS} = 0 V (2); unless otherwise noted

Symbol	Parameters	Min	Typ (3)	Max	Units	Conditions
V_{IL}	Input Low Voltage			0.8	V	
V_{IH}	Input High Voltage	2.4			V	
V_{OL}	Output Low Voltage			.0.4	V	I_{OL} = 4.0 mA
V_{OH}	Output High Voltage	2.4			V	I_{OH} = - 1.6 mA
I_{CC}	V_{CC} Current (Operating)		15	30	mA	R_{EXT} = ∞ (4)
I_{SB}	V_{CC} Current (Standby)		0.5	2	µA	(4) (5)
I_{IL}	Input Leakage Current			±1	µA	(4) (5)
R_{EXT}	Output Load Impedance	16			Ω	Speaker Load
R_{MIC}	Preamp In Input Resistance		10		KΩ	Pins 17, 18
$R_{ANA\ In}$	Ana In Input Resistance		3		KΩ	
A_{PRE1}	Preamp Gain 1		24		dB	AGC = 0.0 V
A_{PRE2}	Preamp Gain 2		- 45	- 15	dB	AGC = 2.5 V
A_{ARP}	Ana In to SP+/-		22		dB	
R_{AGC}	AGC Output Resistance		5		KΩ	
I_{PREH}	Preamp Out Source		- 2		mA	@ V_{OUT} = 1.0 V
I_{PREL}	Preamp In Sink		0.5		mA	@ V_{OUT} = 2.0 V

Notes: 1. $V_{CC} = V_{CCA} = V_{CCD}$.
2. $V_{SS} = V_{SSA} = V_{SSD}$.
3. *Typical values @* T_A = 25° C *and 5.0 V.*
4. V_{CCA} *and* V_{CCD} *connected together.*
5. $\overline{REC}$, $\overline{PLAYL}$, *and* $\overline{PLAYE}$ *must be* V_{CCD}.

AC PARAMETERS (ISD1200/1400 SERIES – PACKAGED)

Operating Conditions: T_A = 0° to 70° C, V_{CC} = 4.5 V to 6.5 V [1], V_{SS} = 0 V [2]; unless otherwise noted

Symbol	Characteristic	Min	Typ [3]	Max	Units	Conditions
THD	Total Harmonic Distortion		1		%	@ 1 KHz
T_{LED1}	$\overline{\text{RECLED}}$ ON Delay		5		µsec	
T_{LED2}	$\overline{\text{RECLED}}$ OFF Delay		48.6		msec	
T_S	Loop Setup Time	300			nsec	
T_H	Loop Hold Time	0			nsec	
T_{RPUD}	Record Power-Up Delay		32		msec	
T_{RPDD}	Record Power-Down Delay		32		msec	
T_{PPUD}	Play Power-Up Delay		32		msec	
T_{PPDD}	Play Power-Down Delay		8.1		msec	
P_{OUT}	Speaker Output Power		12.2		mW	R_{EXT} = 16 Ω
V_{OUT}	Voltage Across Speaker Pins		1.25	2.5	V p-p	R_{EXT} = 600 Ω
V_{IN1}	MIC Input Voltage			20	mV	Peak-to-Peak [4]
V_{IN2}	ANA IN Input Voltage			50	mV	Peak-to-Peak

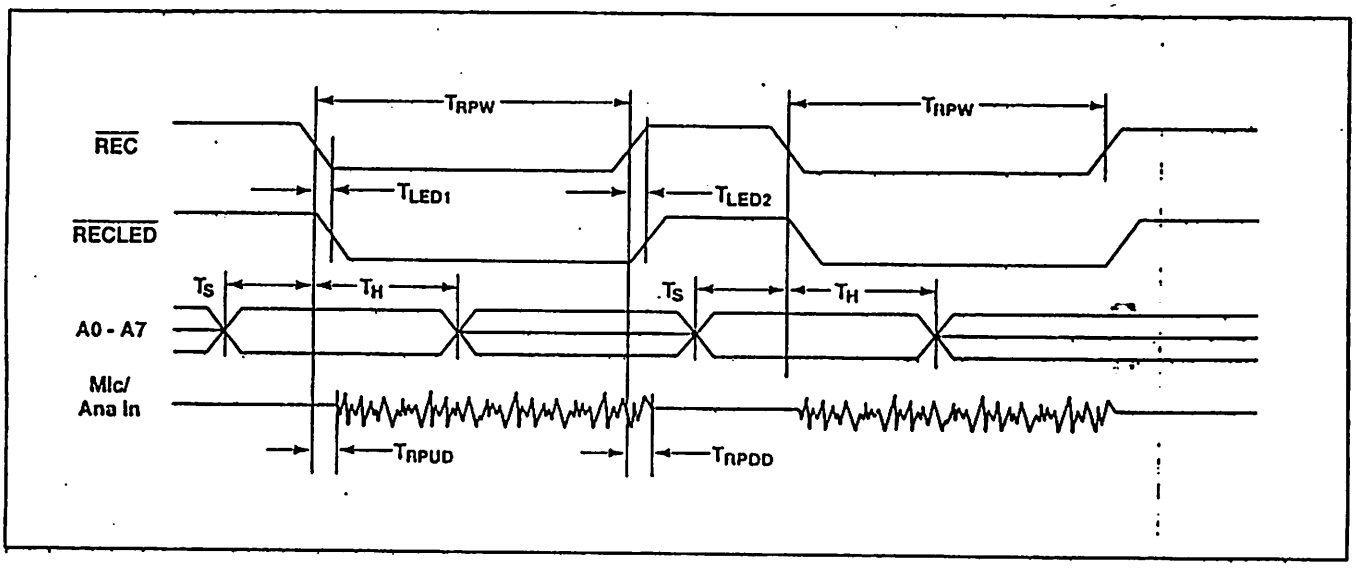
AC PARAMETERS

Symbol	Characteristic	ISD-1208	ISD-1210	ISD-1212	ISD-1416	ISD-1420	Units	Conditions
F_S	Sampling Frequency (max)	8	6.4	5.3	8	6.4	KHz	Internal Oscillator
BW	Bandwidth (max)	3.4	2.7	2.3	3.4	2.7	KHz	3 dB Roll-Off Point [5]
T_{RPW}	Record Pulse Width (max)	8	10	12	16	20	sec.	
T_{PLAY}	Playback Duration (min)	8	10	12	16	20	sec.	
T_{LED2}	$\overline{\text{RECLED}}$ OFF Delay	38.9	48.6	58.3	38.9	48.6	msec	[6]
T_{RPUD}	Rec. Power-Up Delay	26	32	39	26	32	msec	[6]
T_{RPDD}	Rec. Power-Down Delay	26	32	39	26	32	msec	[6]
T_{PPUD}	Play Power-Up Delay	26	32	39	26	32	msec	[6]
T_{PPDD}	Play Power-Down Delay	6.5	8.1	9.7	6.5	8.1	msec	[6]

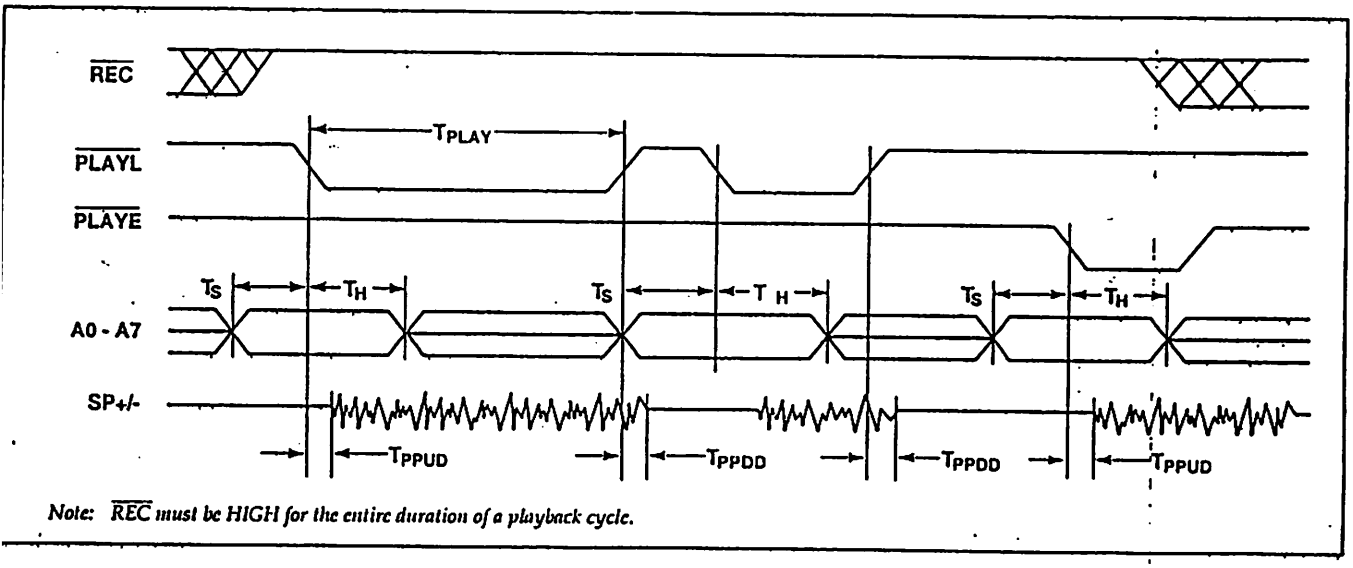
Notes: 1. $V_{CC} = V_{CCA} = V_{CCD}$.
2. $V_{SS} = V_{SSA} = V_{SSD}$.
3. *Typical values @ T_A = 25° C, 5.0 V, and 6.2 KHz sample rate.*
4. *With 12 KΩ series resistor at ANA IN.*
5. *Low-frequency cutoff depends upon value of external capacitors (see Pin Descriptions).*
6. *Typical values @ T_A = 25° C and 5.0 V.*

TIMING DIAGRAMS (ISD1200/1400 SERIES – PACKAGED)

RECORD



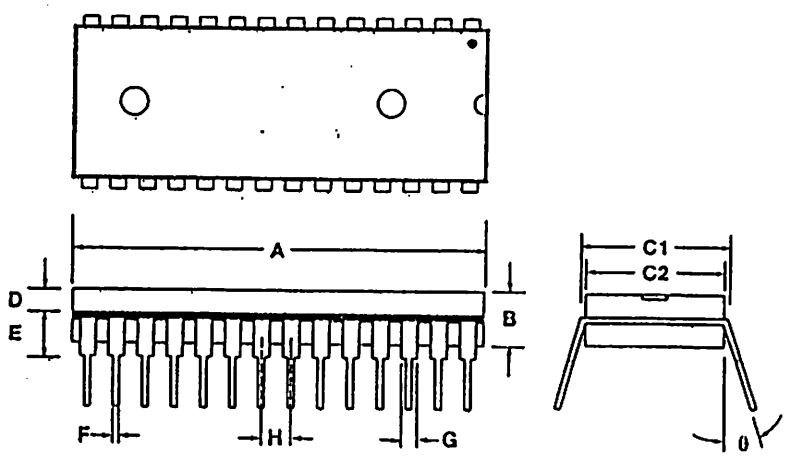
PLAYBACK



Note: $\overline{REC}$ must be HIGH for the entire duration of a playback cycle.

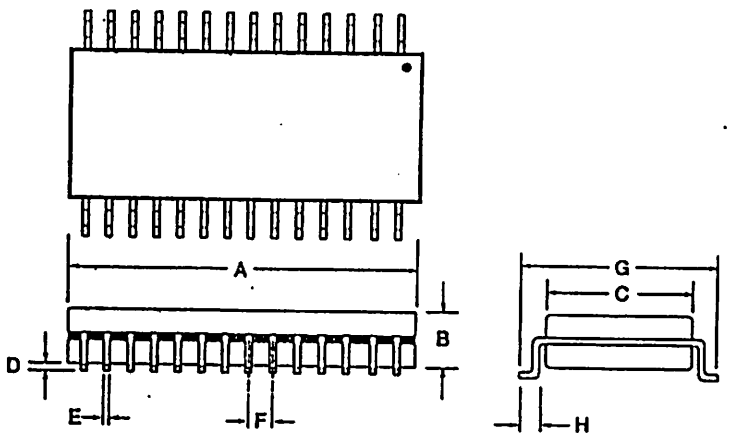
PACKAGE DIAGRAMS

28-Lead Plastic Dual In-Line Package (DIP) Type P



	INCHES			MILLIMETERS		
	Min	Nom	Max	Min	Nom	Max
A	1.445	1.450	1.455	36.7	36.83	36.95
B		.150			3.89	
C1	.600		.625	15.24		15.88
C2	.530	.540	.550	13.46	13.72	13.97
D	1.25	1.30	1.35	2.92	3.05	3.18
E	.125	.130	.135	3.18		3.43
F	.015	.018	.022	0.38	0.46	0.56
G	.055	.060	.065	1.40	1.52	1.65
H		.100			2.54	
θ	0°	7°	15°	0°	7°	15°

28-Lead Plastic Small Outline Package (SOIC) Type J



	INCHES			MILLIMETERS		
	Min	Nom	Max	Min	Nom	Max
A	.706	.714	.718	17.93	18.14	18.24
B	.086	.088	.090	2.18	2.24	2.29
C	.340	.346	.350	8.64	8.79	8.89
D	.004	.007	.010	.102	.178	.254
E	.014	.016	.020	.360	.410	.480
F		.050			1.27	
G	.463	.470	.477	11.76	12.00	12.12
H	.020	.031	.042	.510	.790	1.07

ABSOLUTE MAXIMUM RATINGS (ISD1200X/1400X SERIES - UNPACKAGED DIE)

Condition	Value
Storage temperature range	- 65°C to 150°C
Voltage applied to any pin	(V_{SS} - 0.3 V) to (V_{CC} + 0.3 V)
Voltage applied to any pin (Input current limited to ± 20 mA)	(V_{SS} - 1.0 V) to (V_{CC} + 1.0 V)
V_{CC} - V_{SS}	- 0.3 V to + 7.0 V

Stresses above those listed may cause permanent damage to the device. Exposure to the absolute maximum ratings may affect device reliability.

DC PARAMETERS (ISD1200X/1400X SERIES - UNPACKAGED DIE)

Operating Conditions: T_A = 0° to 50° C (ambient), V_{CC} = 4.5 V to 6.5 V (1), V_{SS} = 0 V (2); unless otherwise noted

Symbol	Parameters	Min	Typ (3)	Max	Units	Conditions
V_{IL}	Input Low Voltage			0.8	V	
V_{IH}	Input High Voltage	2.4			V	
V_{OL}	Output Low Voltage			0.4	V	I_{OL} = 4.0 mA
V_{OH}	Output High Voltage	2.4			V	I_{OH} = - 1.6 mA
I_{CC}	V_{CC} Current (Operating)		15	30	mA	R_{EXT} = ∞ (4)
I_{SB}	V_{CC} Current (Standby)		0.5	2	µA	(4) (5)
I_{IL}	Input Leakage Current			±1	µA	(4) (5)
R_{EXT}	Output Load Impedance	16			Ω	Speaker Load
R_{MIC}	Preamp In Input Resistance		10		KΩ	Pins 17, 18
$R_{ANA\ In}$	Ana In Input Resistance		3		KΩ	
A_{PRE1}	Preamp Gain 1		24		dB	AGC = 0.0 V
A_{PRE2}	Preamp Gain 2		- 45	- 15	dB	AGC = 2.5 V
A_{ARP}	Ana In to SP+/-		22		dB	
R_{AGC}	AGC Output Resistance		5		KΩ	
I_{PREH}	Preamp Out Source		- 2		mA	@ V_{OUT} = 1.0 V
I_{PREL}	Preamp In Sink		0.5		mA	@ V_{OUT} = 2.0 V

Notes: 1. $V_{CC} = V_{CCA} = V_{CCD}$.
2. $V_{SS} = V_{SSA} = V_{SSD}$.
3. *Typical values @* T_A = 25° C *and 5.0 V.*
4. V_{CCA} *and* V_{CCD} *connected together.*
5. $\overline{REC}$, $\overline{PLAYL}$, *and* $\overline{PLAYE}$ *must be* V_{CCD}.

AC PARAMETERS (ISD1200X/1400X SERIES – UNPACKAGED DIE)

Operating Conditions: T_A = 0° to 50° C (ambient), V_{CC} = 4.5 V to 6.5 V [1], V_{SS} = 0 V [2]; unless otherwise noted

Symbol	Characteristic	Min	Typ [3]	Max	Units	Conditions
THD	Total Harmonic Distortion		1		%	@1 KHz
T_{LED1}	$\overline{\text{RECLED}}$ ON Delay		5		µsec	
T_{LED2}	$\overline{\text{RECLED}}$ OFF Delay		48.6		msec	
T_S	Loop Setup Time	300			nsec	
T_H	Loop Hold Time	0			nsec	
T_{RPUD}	Record Power-Up Delay		32		msec	
T_{RPDD}	Record Power-Down Delay		32		msec	
T_{PPUD}	Play Power-Up Delay		32		msec	
T_{PPDD}	Play Power-Down Delay		8.1		msec	
P_{OUT}	Speaker Output Power		12.2		mW	R_{EXT} = 16 Ω
V_{OUT}	Voltage Across Speaker Pins		1.25	2.5	V p-p	R_{EXT} = 600 Ω
V_{IN1}	MIC Input Voltage			20	mV	Peak-to-Peak [4]
V_{IN2}	ANA IN Input Voltage			50	mV	Peak-to-Peak

AC PARAMETERS

Symbol	Characteristic	ISD-1210	ISD-1212	ISD-1416	ISD-1420	Units	Conditions
F_S	Sampling Frequency (max)	6.4	5.3	8	6.4	KHz	Internal Oscillator
BW	Bandwidth (max)	2.7	2.3	3.4	2.7	KHz	3 dB Roll-Off Point [5]
T_{RPW}	Record Pulse Width (max)	10	12	16	20	sec.	
T_{PLAY}	Playback Duration (min)	10	12	16	20	sec.	
T_{LED2}	$\overline{\text{RECLED}}$ OFF Delay	48.6	58.3	38.9	48.6	msec	[6]
T_{RPUD}	Rec. Power-Up Delay	32	39	26	32	msec	[6]
T_{RPDD}	Rec. Power-Down Delay	32	39	26	32	msec	[6]
T_{PPUD}	Play Power-Up Delay	32	39	26	32	msec	[6]
T_{PPDD}	Play Power-Down Delay	8.1	9.7	6.5	8.1	msec	[6]

Notes: 1. $V_{CC} = V_{CCA} = V_{CCD}$.
2. $V_{SS} = V_{SSA} = V_{SSD}$.
3. *Typical values @ T_A = 25° C, 5.0 V, and 6.2 KHz sample rate.*
4. *With 12 KΩ series resister at ANA IN.*
5. *Low-frequency cutoff depends upon value of external capacitors (see Pin Descriptions).*
6. *Typical values @ T_A = 25° C and 5.0 V.*

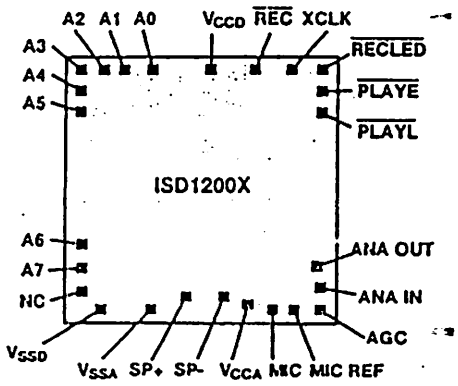
ISD1200X DIE BONDING PHYSICAL LAYOUT

ISD1200X

I. Die Dimensions
X: 172.2 ±1 mils
Y: 138.2 ±1 mils

II. Die Thickness
21 mils

III. Pad Opening(min)
88 x 112 microns
(3.46 x 4.41 mils)



ISD1200X PIN/PAD DESIGNATIONS, WITH RESPECT TO DIE CENTER (μm)

Pin	Pin Name	X Axis	Y Axis	Pin	Pin Name	X Axis	Y Axis
A0	Address 0	-1364	1589.6	V_{CCA}	V_{CC} Analog Power Supply	780	-1552.4
A1	Address 1	-1648.4	1589.6	MIC	Microphone Input	992	-1590
A2	Address 2	-1816.4	1589.6	MIC REF	Microphone Reference	1169.2	-1590
A3	Address 3	-2013.6	1515.6	AGC	Automatic Gain Control	1978.4	-1590
A4	Address 4	-2013.6	1337.6	ANA IN	Analog Input	2005.6	-1196.4
A5	Address 5	-2013.6	1129.6	ANA OUT	Analog Output	1991.2	-995.2
A6	Address 6	-2013.6	-831.2	$\overline{PLAYL}$	Level-Activated Playback	2014.4	1224.4
A7	Address 7	-2013.6	-1022	$\overline{PLAYE}$	Edge-Activated Playback	2014.4	1392.8
NC	No Connect	-2013.6	-1361.6	RECLED	Record LED Output	2012.4	1587.6
V_{SSD}	V_{SS} Digital Power Supply	-1893.6	-1588	XCLK	No Connect (optional)	1581.2	1589.6
V_{SSA}	V_{SS} Analog Power Supply	-357.6	-1588	$\overline{REC}$	Record	752.8	1589.6
SP+	Speaker Output +	-17.2	-1512.8	V_{CCD}	V_{CC} Digital Power Supply	-48	1545.2
SP–	Speaker Output –	412.4	-1512.8				

Note: Die dimensions and pin/pad positions may be subject to change. Please contact ISD Sales Offices or Representatives to verify current or future specifications.

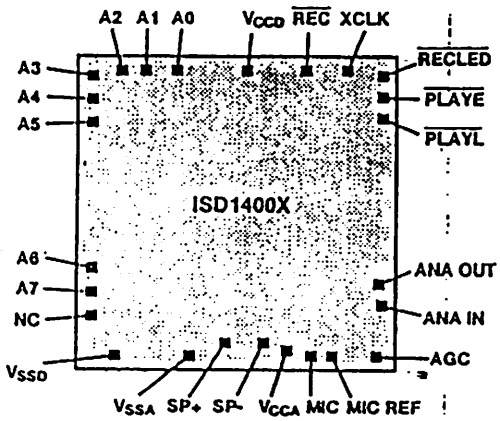
ISD1400X CURRENT DIE BONDING PHYSICAL LAYOUT

ISD1400X

I. Die Dimensions
X: 211 ±1 mils
Y: 207 ±1 mils

II. Die Thickness
21 mils

III. Pad Opening (min)
109 microns
(4.3 mils)



ISD1400X PIN/PAD DESIGNATIONS, WITH RESPECT TO DIE CENTER (μm)

Pin	Pin Name	X Axis	Y Axis	Pin	Pin Name	X Axis	Y Axis
A0	Address 0	-1712.5	2445.5	V_{CCA}	V_{CC} Analog Power Supply	952.2	-2412
A1	Address 1	-2068	2445.5	MIC	Microphone Input	1217.5	-2459
A2	Address 2	-2278	2445.5	MIC REF	Microphone Reference	1439	-2459
A3	Address 3	-2509.5	2368	AGC	Automatic Gain Control	2450.5	-2410
A4	Address 4	-2509.5	2145.5	ANA IN	Analog Input	2484.5	-1980.5
A5	Address 5	-2509.5	1885.5	ANA OUT	Analog Output	2466.5	-1715.5
A6	Address 6	-2509.5	-1525.5	$\overline{PLAYL}$	Level-Activated Playback	2495.5	1989
A7	Address 7	-2509.5	-1764	$\overline{PLAYE}$	Edge-Activated Playback	2495.5	2201
NC	No Connect	-2509.5	-2178.5	$\overline{RECLED}$	Record LED Output	2493	2443
V_{SSD}	V_{SS} Digital Power Supply	-2359.5	-2456.5	XCLK	No Connect (optional)	1970	2445.5
V_{SSA}	V_{SS} Analog Power Supply	-469.5	-2456.5	$\overline{REC}$	Record	900	2445.5
SP+	Speaker Output +	-29	-2362.5	V_{CCD}	V_{CC} Digital Power Supply	-52.5	2390
SP-	Speaker Output –	508	-2362.5				

Note: Die dimensions and pin/pad positions may be subject to change. Please contact ISD Sales Offices or Representatives to verify current or future specifications.

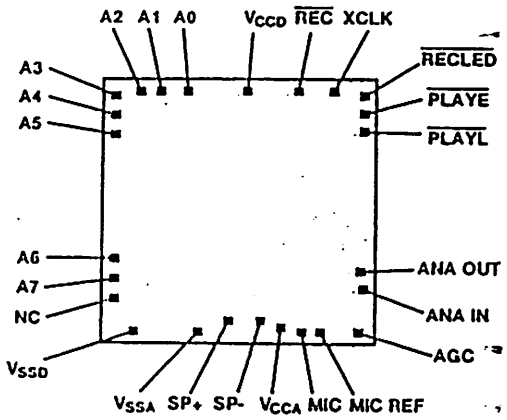
ISD1400X FUTURE DIE BONDING PHYSICAL LAYOUT

ISD1400X FUTURE

I. Die Dimensions
X: 206.9 +1 mils
Y: 202.3 +1 mils

II. Die Thickness
21 mils

III. Pad Opening (min)
88 x 112 microns
(3.6 x 4.4 mils)



ISD1400X FUTURE PIN/PAD DESIGNATIONS, WITH RESPECT TO DIE CENTER (µm)

Pin	Pin Name	X Axis	Y Axis	Pin	Pin Name	X Axis	Y Axis
A0	Address 0	-1332.5	1973.8	V_{CCA}	V_{CC} Analog Power Supply	779.5	-1936.2
A1	Address 1	-1628.9	1973.8	MIC	Microphone Input	991.5	-1973.8
A2	Address 2	-1808.9	1973.8	MIC REF	Microphone Reference	1168.7	-1973.8
A3	Address 3	-2014.1	1910.2	AGC	Automatic Gain Control	1977.9	-1910.6
A4	Address 4	-2014.1	1722.6	ANA IN	Analog Input	2005.1	-1580.2
A5	Address 5	-2014.1	1519.8	ANA OUT	Analog Output	1990.7	-1379
A6	Address 6	-2014.1	-1214.6	PLAYL	Level-Activated Playback	2013.9	1608.6
A7	Address 7	-2014.1	-1399.8	PLAYE	Edge-Activated Playback	2013.9	1777
NC	No Connect	-2014.1	-1745.4	RECLED	Record LED Output	2011.9	1971.8
V_{SSD}	V_{SS} Digital Power Supply	-1894.1	-1971.8	XCLK	No Connect (optional)	1580.7	1973.8
V_{SSA}	V_{SS} Analog Power Supply	-358.1	-1971.8	REC	Record	752.3	1973.8
SP+	Speaker Output +	-17.7	-1896.6	V_{CCD}	V_{CC} Digital Power Supply	-48.5	1929.4
SP–	Speaker Output –	411.9	-1896.6				

Note: Die dimensions and pin/pad positions may be subject to change. Please contact ISD Sales Offices or Representatives to verify current or future specifications.

ORDERING INFORMATION

When placing an order for the ISD1200/1400 Series devices, please refer to the following part numbers:

Part No.	Rec/Play Duration	Description
ISD1210P	10 sec.	28-pin plastic dual in-line package (DIP)
ISD1210G	10 sec.	28-lead small-outline integrated circuit (SOIC)
ISD1210X	10 sec.	Bare unpackaged die
ISD1212P	12 sec.	28-pin plastic dual in-line package (DIP)
ISD1212G	12 sec.	28-lead small-outline integrated circuit (SOIC)
ISD1212X	12 sec.	Bare unpackaged die
ISD1416P	16 sec.	28-pin plastic dual in-line package (DIP)
ISD1416G	16 sec.	28-lead small-outline integrated circuit (SOIC)
ISD1416X	16 sec.	Bare unpackaged die
ISD1420P	20 sec.	28-pin plastic dual in-line package (DIP)
ISD1420G	20 sec.	28-lead small-outline integrated circuit (SOIC)
ISD1420X	20 sec.	Bare unpackaged die