INSTITUT TEKNOLOGI NASIONAL MALANG
FAKULTAS TEKNOLOGI INDUSTRI
JURUSAN TEKNIK ELEKTRO S - 1
KONSENTRASI ELEKTRONIKA

SKRIPSI

PERENCANAAN DAN PEMBUATAN ALAT PENJERNIHAN AIR DENGAN MENGONTROL NILAI pH NORMAL BERBASIS ATmega8515

Oleh :

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LEMBAR PERSETUJUAN

PERENCANAAN DAN PEMBUATAN ALAT PENJERNIHAN AIR DENGAN MENGONTROL NILAI pH NORMAL BERBASIS AtMEGA 8515

SKRIPSI

Diajukan Sebagai Salah Satu Syarat Untuk Memperoleh Gelar Sarjana Teknik Pada Jurusan Teknik Elektro Strata Satu (S-1) Konsentrasi Elektronika

Disusun oleh :

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Judul Skripsi	:

" PERENCANAAN DAN PEMBUATAN ALAT PENJERNIHAN AIR DENGAN MENGONTROL NILAI pH NORMAL BERBASIS AtMEGA 8515 "

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ABSTRAKSI

PERENCANAAN DAN PEMBUATAN ALAT PENJERNIHAN AIR DENGAN MENGONTROLNILAI pH NORMAL BERBASIS MIKROKONTROLLER ATMEGA 8515

(Ronny Andriyanto, 99.17.102, Jurusan Teknik ElektroS-1/Elektronika)
(Dosen Pembimbing : Ir. F. Yudi Limpraptono, MT)

Kata Kunci : Mikrokontroller ATmega 8515, Transducer pH PE-03, ADC 0804, dan Transistor DB139.

Pesatnya perkembangan teknologi dewasa ini menyentuh kesemua bidang yang ada dimasyarakat, terlebih-lebih untuk teknologi elektronika atau penggunaan otomatisasi yang berdasarkan pada sistem mikrokontroller. Tapi untuk dikota-kota maju, kemajuan teknologi itu sendiri bisa dikatakan hampir menyentuh sendi-sendi kehidupan, berbeda dengan daerah-daerah yang masih belum maju dalam hal teknologi misalnya daerah di luar pulau jawa. Suatu misal untuk air yang dipakai umumnya diluar pulau Jawa air diambil dari pegunungan atau dari sumur yang digali yang kualitas air tersebut baik dan jernih bisa dikonsumsi oleh rumah tangga. Berbeda dengan apa yang terjadi diluar pulau Jawa. Misalnya di Kalimantan dimana air yang dikonsumsi untuk kebutuhan rumah tangga diambil dari air sungai yang banyak mengalir di Kalimantan.

Dan untuk dapat dikonsumsi oleh rumah tangga harus melewati masa pengendapan atau pemisahan antara air dan tanah yang terkandung dalam air dan waktu yang lama, lagi pula untuk sungai-sungai yang ada di Kalimantan saat ini banyak yang telah mengalami erosi sehingga mempengaruhi kualitas air yang akan dikonsumsi oleh masyarakat dan rumah tangga, yang mana dari tahun ke tahun tingkat kekeruhannya melewati ambang batas .

Didalam tugas akhir ini, dibahas tentang aplikasi mikrokontroller Atmega8515 dalam perencanaan dan pembuatan alat penjernihan air dengan mengontrol nilai pH normal berbasis Atmega 8515. Alat yang dibuat meliputi perencanaan perangkat keras dan perangkat lunak. Perencanaan perangkat keras meliputi: rangkaian sensor pH, rangkaian sensor kekeruhan, rangkaian *driver* relay, rangkaian ADC, rangkaian LCD, minimum sistem Mikrokontroller Atmega8515. Perencanaan perangkat lunak berupa *Flowchart* cara kerja sistem. Sensor kekeruhan berupa LDR segera memompa air menuju tangki penyaringan. Dan sensor pH akan bekerja mendeteksi tingkat pH air, dan menormalkan pH air. Mikrokontroller memberikan perintah untuk mengontrol pompa, motor DC, dan tranducer pH. Mikrokontroller mengolah data yang diterima dan LCD menampilkan sebagai informasi. Dari hasil pengujian diketahui memerlukan waktu yang cukup singkat untuk mengontrol tingkat kekeruhan air dan nilai pH air. Dari hasil pengujian diketahui rangkaian sensor dapat bekerja dengan baik. Ini dibuktikan dengan kecilnya prosentase *error*. *Error* pada rangkaian sensor suhu sebesar 0,89%.

KATA PENGANTAR

Dengan mengucapkan puji syukur kehadirat Tuhan Yang Maha Esa Penulis dapat menyelesaikan skripsi ini karena berkat rahmat-Nyalah Penulis dapat menyusun skripsi ini yang menjadi salah satu syarat akademik dalam menyelesaikan studi untuk menempuh gelar Sarjana S-1 di Fakultas Teknologi Industri Jurusan Teknik Elektro di Institut Teknologi Nasional Malang.

Skripsi ini disusun berdasarkan hasil-hasil percobaan beserta teori dasar dan beberapa jawaban pertanyaan dari permasalahan yang ada sehinga Penulis sekaligus Penyusun dapat menambah wawasan dan tidak hanya menguasai teori saja namun juga memahami pengetahuan tersebut secara teknis.

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Malang, Maret 2005

Penulis

DAFTAR ISI

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BAB I
PENDAHULUAN

1.1. LATAR BELAKANG MASALAH.

Semakin pesatnya perkembangan teknologi dewasa ini tidak menyentuh kesemua bidang yang ada di masyarakat, terlebih-lebih untuk teknologi elektronika atau penggunaan otomatisasi yang berdasarkan pada sistem mikrokontroler. Tapi untuk dikota-kota maju, kemajuan teknologi itu sendiri bisa dikatakan hampir menyentuh sendi-sendi kehidupan, berbeda dengan daerah-daerah yang masih belum maju dalam hal teknologi misalnya daerah yang berada diluar pulau Jawa. Suatu misal untuk air yang dipakai umumnya di pulau Jawa air diambil dari pegunungan atau dari sumur yang digali yang kwalitas air tersebut baik dan jernih yang sudah barang tentu tidak membutuhkan waktu lama untuk bisa dikonsunsi oleh rumah tangga. Berbeda dengan apa yang terjadi diluar pulau Jawa. Misalnya di Kalimantan dimana air yang dikonsumsi untuk kebutuhan rumah tangga diambil dari air sungai yang sudah barang tentu banyak mengalir di Kalimantan.

Dan untuk dapat dikonsumsi oleh rumah tangga air tersebut melewati masa pengendapan atau pemisahan antara air dan tanah yang terkandung dalam air tersebut yang membutuhkan waktu yang lama pula, lagi pula untuk sungai-sungai yang ada di Kalimantan saat ini banyak yang telah mengalami erosi sehingga mempengaruhi kwalitas air yang akan dikonsumsi oleh masyarakat dan runah tangga, yang mana dari tahun ketahun tingkat kekeruhannya sudah melewati ambang batas yang layak untuk dikonsumsi oleh manusia.

1.2. PERMASALAHAN.

- Bagaimana membuat alat untuk mengontrol tingkat kekeruhan dan keasaman air pada proses pengolahan air minum PDAM.

1.3. TUJUAN PENULISAN.

Tujuan penulisan skripsi ini adalah merencanakan dan membuat alat pengontrol tingkat kekeruhan dan tingkat keasaman air sebagai salah satu dari beberapa bagian dari proses pengolahan air minum.

1.4. BATASAN MASALAH.

Guna dapat tercapainya apa yang menjadi tujuan pembahasan skripsi ini, maka perlu kiranya diberikan batasan dalam pembahasannya yaitu:

- Digunakan mikrokontroller AT Mega 8515.
- Pembahasan hanya pada proses tingkat kekeruhan dan keasaman air.
- Pembahasan masing-masing instrumen sensor tidak terlampau menyeluruh.
- Konversi ADC (Analog to Digital Conversion).
- Driver menggunakan Transistor dan Relay.
- Rangkaian catu daya tidak dibahas.
- Penggunaan larutan pH yang digunakan tidak dibahas.
- Sensor pH yang dibahas pada sensor yang digunakan dan tidak membahas sensor pH jenis lain.
- Filter pada tangki penyaringan tidak dibahas.

1.5. METODOLOGI.

Untuk tercapainya sasaran yang sesuai dengan tujuan, maka digunakan metode metode sebagai berikut :

a. Studi Literatur.

   Pemanfaatan buku-buku sebagai referensi.

b. Perencanaan Dan Pembuatan Alat

   Melaksanakan perencanaan dan pembuatan sistem sesuai dengan rencana yang disusun.

c. Pelaksanaan Uji Coba Sistem.

   Menguji apakah sistem sudah sesuai dengan perencanaan dan perancangan.

d. Penyusunan Buku Laporan.

1.6. SISTEMATIKA PENULISAN.

Pada penulisan skripsi ini ditulis sedemikian rupa sehingga diperoleh hubungan yang jelas antara bagian yang satu dengan yang lainnya. Sistematikanya adalah sebagai berikut :

BAB I PENDAHULUAN

Berisikan latar belakang, permasalahan, tujuan, batasan masalah, metodelogi dan sistematika penulisan.

BAB IILANDASAN TEORI

Teori-teori yang menunjang dalam penyusunan skripsi.

BAB III PERENCANAAN DAN PEMBUATAN ALAT

Meliputi cara mendesain rangkaian serta membahas blok-blok diagram secara keseluruhan.

BAB IV PENGUJIAN ALAT

Mencakup pembahasan tentang proses pengujian alat yang terdiri dari peralatan yang digunakan, langkah kerja dan analisa hasil pengujian.

BAB V PENUTUP

Berisikan kesimpulan dan saran.

BAB II
LANDASAN TEORI

2.1. Tujuan Utama Pengolahan Air.

Tujuan utama dari suatu pengolahan air minum adalah menjadikan supaya air aman dalam pemakaian, konsumsi dan bersih. Aman berarti tidak memberikan efek negatif kepada konsumen, maupun terhadap sarana peralatan sistem penyediaan air minum baik dalam jangka waktu pendek maupun dalam jangka waktu panjang. Jadi kwalitas air harus memenuhi kriteria tertentu sesuai dengan standart air bersih.

Berbicara mengenai kwalitas air, ada 4 pokok permasalahan yang terkandung didalamnya yaitu :

1. Kwalitas fisika
2. Kwalitas kimia
3. kwalitas biologis, dan
4. kwalitas radiologis

Secara umum ke empat masalah tersebut dapat dilihat pada Standart Kwalitas Air Minum, yang di Indonesia dituangkan dalam surat Keputusan Menteri Kesehatan RI. Seperti telah kita maklumi bahwa air merupakan media penularan yang baik bagi beberapa sumber penyakit antara lain :

1. Bakteri
2. Protozoa
3. Cacing
4. Virus, dan

5. Jamur

Makin tinggi kekeruhan dari air, maka makin besar pula kemungkinan adanya penyebab penyakit dalam air, disamping makin banyak diperlukan zat desinfektan yang harus dibubuhkan sebagai pengamannya.

2.1.1.Kualitas Air Berdasarkan Tingkat Keasaman (pH).

Suatu larutan mempunyai kapasitas buffer tinggi apabila perubahan pH larutan hanya sedikit pada saat ditambahkan asam atau basa.

Sebagai contoh, penambahan 0,01 mmol HCL kedalam satu liter air murni mengubah pH air tersebut dari 7,0 menjadi 5,0. Jumlah yang sama ditambahkan kedalam satu liter air alam dengan pH 7,0 mengubah pH sebesar kurang dari 0,02 unit. Maka kapasitas buffer adalah suatu parameter yang menunjukkan ketahanan larutan terhadap perubahan pH.

- Kapasitas buffer tinggi berarti penambahan asam atau basa akan sedikit berpengaruh terhadap kenaikan atau penurunan pH larutan.
- Kapasitas buffer rendah berarti penambahan asam atau basa akan banyak berpengaruh terhadap perubahan pH larutan.

Untuk mengetahui besarnya kapasitas buffer suatu larutan, digunakan suatu angka yang disebut indeks buffer. Indeks buffer didapat berdasarkan pada percobaan di laboratorium, dimana larutan buffer dititrasi oleh asam atau basa yang bermuatan satu.

Jadi : indeks buffer adalah berapa banyak asam atau basa (1^+ atau 1^-) harus ditambahkan kedalam larutan buffer (dalam mmol/L) untuk menaikkan atau menurunkan pH sebesar 1 unit.

Semakin besar indeks buffer semakin besar pula kapasitas buffernya. Larutan buffer dapat dibuat dari campuran asam lemah dengan garamnya dari basa kuat. Atau dapat juga dibuat dari campuran basa lemah dengan garamnya dari asam kuat, misalnya campuran ammonium hidroksida dan ammonium khlorida.

2.1.2. Kualitas Air Berdasarkan Tingkat Kekeruhannya.

Turbidity atau kekeruhan dalam air dapat disebabkan oleh clay, pasir, zat-zat organik dan anorganik yang sangat halus, plankton dan mikroorganisme lainnya. Chlorinasi tidak akan efektif bila kadar kekeruhan tinggi karena merupakan habitat dari bakteri pathogen. Proses penurunan kadar kekeruhan adalah mahal.

2.2. MIKROKONTROLLER AVR Atmega 8515.

2.2.1. Teori Umum.

AVR merupakan seri mikrokontroler CMOS 8-bit buatan Atmel, berbasis arsitektur RISC (Reduced Instruction Set Computer). Hampir semua instruksi dieksekusi dalam satu siklus clock. AVR mempunyai 32 register general-purpose, timer/counter fleksibel dengan mode compare, interrupt internal dan eksternal, serial UART, programmable Watchdog Timer, dan mode power saving. Beberapa diantaranya mempunyai ADC dan PWM internal. AVR juga mempunyai In-System Programmable Flash on-chip yang mengijinkan memori program untuk diprogram ulang dalam sistem menggunakan hubungan serial SPI. Chip AVR yang digunakan adalah Atmega 8515.

Atmega 8515 adalah mikrokontroler CMOS 8-bit daya-rendah berbasis arsitektur RISC yang ditingkatkan. Kebanyakan instruksi dikerjakan pada satu siklus clock, Atmega 8515 mempunyai *throughput* mendekati 1 MIPS per MHz membuat disainer sistem untuk mengoptimasi komsumsi daya versus kecepatan proses.

Beberapa keistimewaan dari AVR Atmega 8515 antara lain:

- Advanced RISC Architecture
  - 130 Powerful Instructions – Most Single Clock Cycle Execution
  - 32 x 8 General Purpose Working Registers
  - Fully Static Operation
  - Up to 16 MIPS Throughput at 16 MHz
  - On-chip 2-cycle Multiplier
- Nonvolatile Program and Data Memories
  - 8K Bytes of In-System Self-Programmable Flash

    Endurance: 10,000 Write/Erase Cycles
  - Optional Boot Code Section with Independent Lock Bits

    In-System Programming by On-chip Boot Program

    True Read-While-Write Operation
  - 512 Bytes EEPROM

Endurance: 100,000 Write/Erase Cycles

- 512 Bytes Internal SRAM
- Up to 64K Bytes Optional External Memory Space
- Programming Lock for Software Security

• Peripheral Features

- One 8-bit Timer/Counters with Separate Prescalers and Compare Modes
- One 16-bit Timer/Counter with Separate Prescaler, Compare Mode, and Capture Mode
- Three PWM Channels
- Programmable Serial USART
- Master/Slave SPI Serial Interface
- Programmable Watchdog Timer with Separate On-chip Oscillator
- On-chip Analog Comparator

• Special Microcontroller Features

- Power-on Reset and Programmable Brown-out Detection
- Internal Calibrated RC Oscillator
- External and Internal Interrupt Sources
- Three Sleep Modes: Idle, Power-down and Standby

• I/O and Packages

- 32 Programmable I/O Lines
- 40-pin PDIP, 44-lead TQFP, 44-lead PLCC, and 44-pad MLF

• Operating Voltages

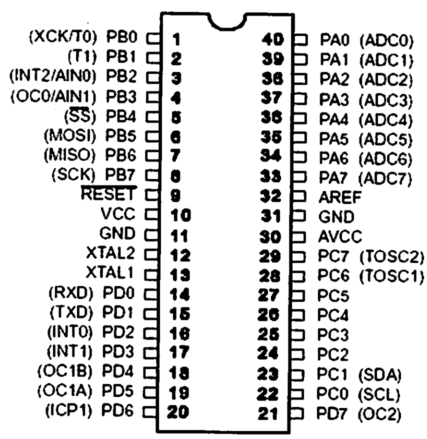
  • 2.7 - 5.5V for ATmega8515L

  • 4.5 - 5.5V for ATmega8515

• Speed Grades

  • 0 - 8 MHz for ATmega8515L

  • 0 - 16 MHz for ATmega8515



Gambar 2-1 Konfigurasi ATmega8515.

Pin-pin pada ATmega8515 dengan kemasan 40-pin DIP (dual in-line package) ditunjukkan dalam Gambar 2-1.

Guna memaksimalkan performa dan paralelisme, AVR menggunakan arsitektur Harvard dengan memori dan bus terpisah untuk program dan data. Arsitektur CPU dari AVR ditunjukkan dalam Gambar 2-1. Instruksi pada memori program dieksekusi dengan pipelining single level. Selagi sebuah instruksi sedang dikerjakan, instruksi berikutnya diambil dari memori program.

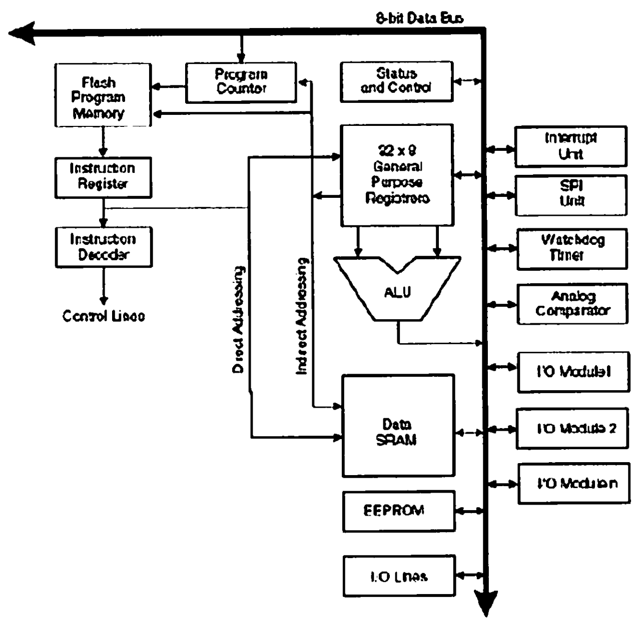
2.2.2.Sebagai Input/Output Digital.

Atmega 8515 mempunyai empat buah port yang bernama PortA, PortB, PortC, dan PortD. Keempat port tersebut merupakan jalur bi-directional dengan pilihan internal pull-up. Tiap port mempunyai tiga buah register bit, yaitu DDxn, PORTxn, dan PINxn. Huruf 'x' mewakili nama huruf dari port sedangkan huruf 'n' mewakili nomor bit. Bit DDxn terdapat pada I/O address DDRx, bit PORTxn terdapat pada I/O address PORTx, dan bit PINxn terdapat pada I/O address PINx.

Bit DDxn dalam regiter DDRx (Data Direction Register) menentukan arah pin. Bila DDxn diset 1 maka Px berfungsi sebagai pin output. Bila DDxn diset 0 maka Px berfungsi sebagai pin input. Bila PORTxn diset 1 pada saat pin terkonfigurasi sebagai pin input, maka resistor pull-up akan diaktifkan. Untuk mematikan resistor pull-up, PORTxn harus diset 0 atau pin dikonfigurasi sebagai pin output. Pin port adalah tri-state setelah kondisi reset.

Bila PORTxn diset 1 pada saat pin terkonfigurasi sebagai pin output maka pin port akan berlogika 1. Dan bila PORTxn diset 0 pada saat pin terkonfigurasi sebagai pin output maka pin port akan berlogika 0. Saat mengubah kondisi port dari kondisi *tri-state* (DDxn=0, PORTxn=0) ke kondisi *output high* (DDxn=1, PORTxn=1) maka harus ada kondisi peralihan apakah itu kondisi *pull-up enabled* (DDxn=0, PORTxn=1) atau kondisi *output low* (DDxn=1, PORTxn=0). Biasanya, kondisi pull-up enabled dapat diterima sepenuhnya, selama lingkungan impedansi tinggi tidak memperhatikan perbedaan antara sebuah *strong high driver* dengan sebuah pull-up. Jika ini bukan suatu masalah, maka bit PUD pada register SFIOR dapat diset 1 untuk mematikan semua pull-up dalam semua port.

Peralihan dari kondisi *input dengan pull-up* ke kondisi *output low* juga menimbulkan masalah yang sama. Kita harus menggunakan kondisi tri-state (DDxn=0, PORTxn=0) atau kondisi output high (DDxn=1, PORTxn=0) sebagai kondisi transisi. Lebih detil mengenai port ini dapat dilihat pada manual datasheet dari IC ATmega8515.



Gambar 2-2 Arsitektur CPU dari AVR.

Tabel 2.1 Konfigurasi Pin Port.

DDxn	PORTxn	PUD (in SFIOR)	I/O	Pull-up	Comment
0	0	X	Input	No	Tri-state (Hi-Z)
0	1	0	Input	Yes	Pxn will source current if ext. pulled low.
0	1	1	Input	No	Tri-state (Hi-Z)
1	0	X	Output	No	Output Low (Sink)
1	1	X	Output	No	Output High (Source)

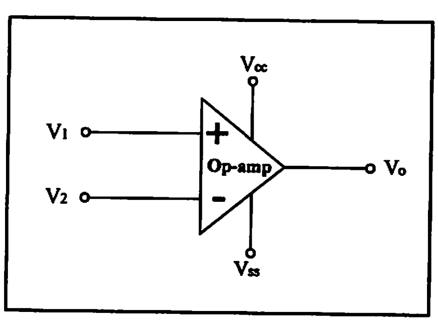
Bit	7	6	5	4	3	2	1	0	
	ADTS2	ADTS1	ADTS0	-	ACME	PUD	PSR2	PSR10	SFIOR
Read/Write	R/W	R/W	R/W	R	R/W	R/W	R/W	R/W	
Initial Value	0	0	0	0	0	0	0	0	

Bit 2 – PUD : Pull-up Disable

Bila bit diset bernilai 1 maka pull-up pada port I/O akan dimatikan walaupun register DDxn dan PORTxn dikonfigurasikan untuk menyalakan pull-up (DDxn=0, PORTxn=1).

2.3. Penguat Operasional.

Penguat operasional (op-amp) merupakan suatu komponen aktif yang terdiri dari rangkaian penguat gandengan langsung dengan penguatan tinggi yang dalam pengoperasiannya dilengkapi dengan umpan balik untuk memberikan tanggapan secara menyeluruh. Skematis dari op-amp diperlihatkan dalam Gambar 2-3.



Gambar 2-3. Penguat Operasional.

Penguat ini mempunyai lima buah terminal dasar, diantaranya dua terminal untuk mensupply daya, dua terminal untuk isyarat masukan, dan satu terminal keluaran. Kedua terminal isyarat masukan masing-masing terminal masukan pembalik (*inverting input* (-)), dan terminal masukan tak membalik (*non-inverting input* (+)).

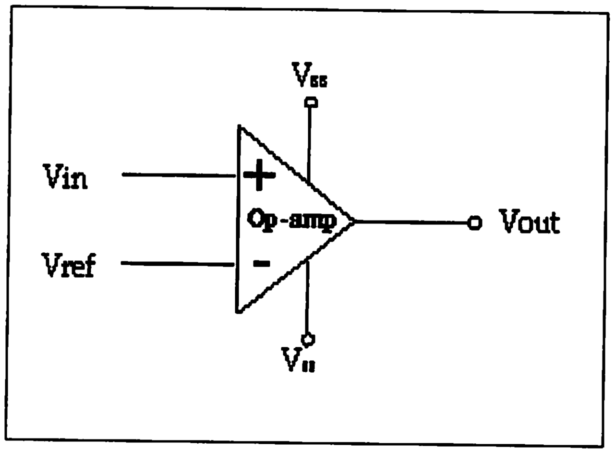
Jika pada kutub masukan tak membalik (V_1) diberi tegangan masukan, maka tegangan keluarannya akan sefasa dengan masukannya. Sebaliknya jika pada kutub masukan membalik (V_2) diberi tegangan masukan, maka tegangan keluarannya akan berlawan fasa dengan masukannya.

Suatu penguat operasional yang ideal mempunyai sifat-sifat sebagai berikut:

- Penguatnya terkopel langsung (*direct coupled*)
- Impedansi masukan (Zi) = ~ (tak berhingga)
- Impendasi keluaran (Zo) = 0 (nol)
- Penguatan (A) = ~ (tak berhingga)
- Tegangan keluaran bernilai 0 (nol), jika tegangan pada kedua terminal masukan bernilai 0 (nol)
- Tegangan keluaran dapat menganyun ke arah positif maupun ke arah negatif
- Lebar jalurnya (*band width*) tak berhingga lebarnya.

2.3.1.Op-Amp Sebagai Komparator.

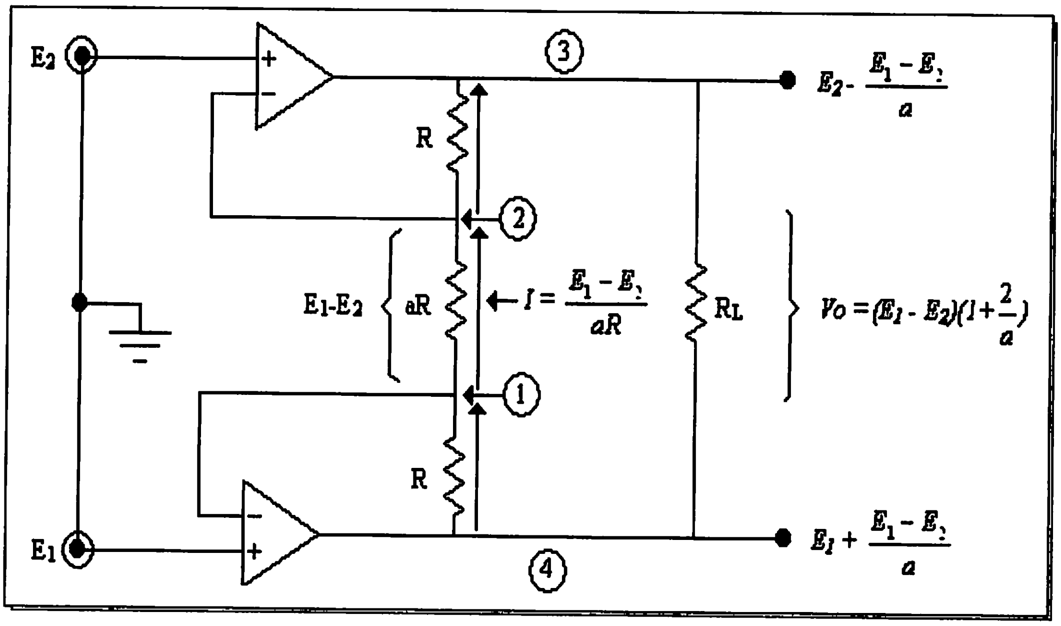
Komparator atau pembanding berfungsi membandingkan suatu sinyal tegangan dari satu *input* op-amp dengan suatu tegangan referensi yang sudah diketahui/ditetapkan pada *input* yang lain. Komparator merupakan contoh aplikasi op-amp yang sangat berguna. Bentuk sederhana dari komparator adalah op-amp dengan open loop, dengan dua *input* analog dan satu output digital, output bisa berupa tegangan saturasi (+) atau (-) tergantung *input* mana yang lebih besar. Komparator sederhan ditunjukkan dalam Gambar 2.4.



Gambar 2.4. Komparator Sederhana.

2.4. Penguat Instrumentasi.

Penguat instrumentasi terdiri dari 2 komponen penguat penyangga yang selanjutnya disebut penguat diferensial tersangga dan suatu penguat diferensial dasar. Penguat diferensial penyangga berfungsi memberi penguatan dan mencegah resistansi sensor mempengaruhi resistor di dalam rangkaian dan sebaliknya. Sebuah penguat diferensial tersangga ditunjukkan dalam Gambar 2.5.



Gambar 2.5 Penguat Diferensial Tersangga.

Tegangan di titik 1 (terhadap ground) sama dengan E1 dan di titik 2 (terhadap ground) sama dengan E2. Sedangkan pada saat terjadi pembebanan tegangan yang melintasi aR adalah E1-E2. Tahanan aR adalah sebuah resistor variabel yang digunakan untuk mengatur gainnya. Arus yang melalui aR adalah :

$$I = \frac{E_1 - E_2}{aR} \qquad (2.1)$$

Bila E1 lebih besar dari E2, maka arus I adalah seperti yang ditunjukkan dalam Gambar 2.5. Arus I mengalir melalui kedua tahanan yang bertanda R dan tegangan yang melintasi tiga tahanan seluruhnya menentukan harga Vo dalam bentuk persamaan :

$$Vo = (E_1 - E_2)(1 + \frac{2}{a}) \qquad (2.2)$$

Persamaan ini didapat dengan melihat pada titik 3 dalam Gambar 2.5, tegangan pada titik ini adalah :

$$E_2 - \frac{E_1 - E_2}{a} \quad \text{...} \quad (2.3)$$

Sedangkan pada titik 4 dalam Gambar 2.5, tegangannya adalah :

$$E_1 + \frac{E_1 - E_2}{a} \quad \text{...} \quad (2.4)$$

Sehingga Vo untuk rangkaian penyangga tersebut adalah beda tegangan antara titik 3 dan 4 yaitu :

$$Vo = (E_1 + \frac{E_1 - E_2}{a}) - (E_2 - \frac{E_1 - E_2}{a}) \quad \text{..................................} \quad (2.5)$$

$$Vo = (E_1 - E_2)(1 + \frac{2}{a}) \quad \text{..} \quad (2.6)$$

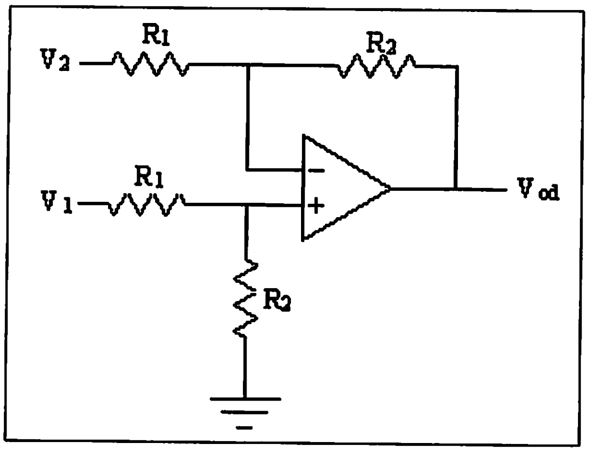
$$\frac{Vo}{(E_1 - E_2)} = (1 + \frac{2}{a}) = A_v \quad \text{...} \quad (2.7)$$

dimana : Vo = keluaran tegangan diferensial tersangga

$A_v = (1 + \frac{2}{a})$ adalah faktor penguatan

$a = \frac{aR}{R}$

Untuk mengatur gain penguatannya dapat dilakukan dengan mengubah tahanan aR saja. Tetapi penguat diferensial tersangga di atas hanya dapat menggerakkan beban mengambang saja (beban yang tak memiliki terminal yang dihubungkan ke ground). Untuk menggerakkan beban terground diperlukan rangkaian yang mengubah tegangan masukan diferensial menjadi suatu tegangan keluaran berujung tunggal. Rangkaian seperti itu adalah penguat diferensial dasar ditunjukkan dalam Gambar 2.6.



Gambar 2.6 Penguat Diferensial Dasar.

Penguat diferensial dasar ini mempunyai persamaan sebagai berikut :

$$V_{od} = (V_1 - V_2)\ \frac{R_2}{R_1} \quad \text{.......................} \quad (2.8)$$

Dimana : Vod = Keluaran tegangan diferensial dasar

(V1-V2) = Tegangan masukan diferensial dasar

Keluaran penguat ini merupakan keluaran penguat diferensial tersangga yang kemudian dikuatkan oleh penguat diferensial dasar.

Dari persamaan (2.6) dan (2.7) diketahui bahwa :

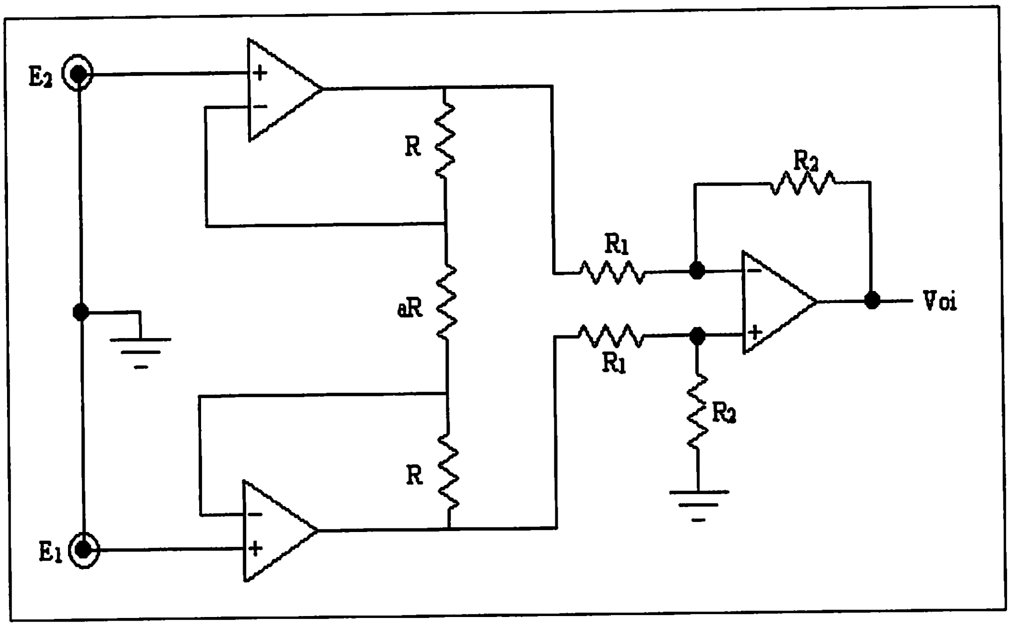
$$V_o = (E_1 - E_2)(1 + \frac{2}{a}) \quad \text{.......................} \quad (2.9)$$

$$V_{od} = (V1 - V2)\ \frac{R_2}{R_1} \quad \text{.......................} \quad (2.10)$$

Dimana : Vo = keluaran diferensial tersangga.

(V1-V2) = Tegangan masukan diferensial dasar.

ditunjukkan dalam Gambar 2.7.



Gambar 2.7 Penguat Instrumentasi.

2.5. ADC (*Analog to Digital Converter*).

Agar dapat mengolah suatu variable fisik yang umumnya adalah besaran analog amaka dibutuhkan suatu komponen yang dapat merubah besaran analog ke

Dengan memasukkan keluaran tegangan diferensial tersangga ke tegangan masukan diferensial dasar (keluaran tegangan diferensial tersangga menjadi masukan tegangan masukan diferensial dasar Vo=(V1-V2), maka didapatkan besar tegangan keluaran penguat instrumentasi :

$$V_{oi} = ((E_1 - E_2)\,(1+\frac{2}{a}))\,\frac{R_2}{R_1} \quad \text{...} \quad (2.11)$$

digital supaya dapat diolah oleh mikrokontroller. Konversi ini dilakukan oleh *converter* analog ke digital.

Resolusi (*Res*) ADC didefinisikan sebagai *voltage input* yang diperlukan untuk 1bit dan dapat dinyatakan dengan persamaan berikut:

$$\text{Res} = \frac{\text{E}}{2^n - 1} \quad \text{...} \quad (2.12)$$

Atau jika dinyatakan dalam % resolusi:

$$\%\text{Res} = \frac{\text{E}}{2^n - 1} x100\%$$

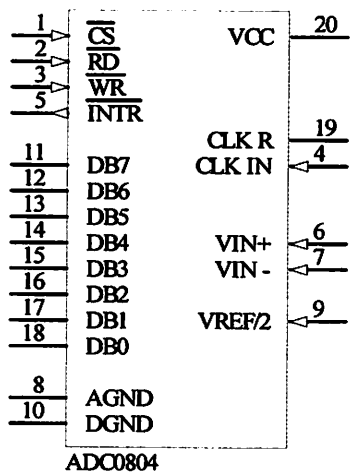
Resolusi ADC mengacu pada jumlah bit dalam keluaran biner ADC. Resolusi ADC 8 bit sama dengan (1/255) 100%. Spesifikasi penting lain selain ketelitian (akurasi) dan linearitas adalah waktu konversi (*Convertion time*). Waktu konversi ADC adalah waktu yang diperlukan ADC untuk menghasilkan kode biner yang valid untuk tegangan masukkan yang diberikan semakin pendek waktu konversi berarti kecepatan konversi semakin tinggi.

ADC yang paling banyak digunakan adalah:

1. *Counting and counter* ADC.
2. *Successive approximation* ADC (disingkat SAC).
3. *Paralel comparator* atau *flash* ADC.
4. *Dual slope* atau *ratimetrik* ADC.

Pada gambar 2-8 menunjukkan konfigurasi pin ADC 0804. Sehingga skripsi ini membahas salah satu dari keempat macam ADC tersebut, yaitu

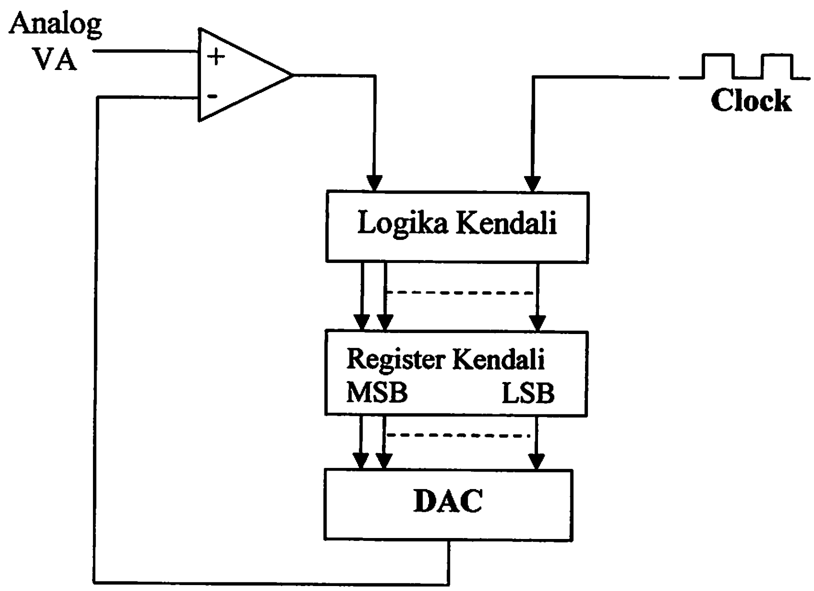
Successive Aproximation ADC sebagai ADC yang paling banyak digunakan karena memberikan prestasi yang paling baik untuk suatu rangkuman pemakaian yang luas dengan biaya yang pantas.



Gambar 2-8 Konfigurasi Pin ADC 0804.

2.5.1.ADC Pendekatan Bertingkat (*Successive Approximation* ADC).

ADC pendekatan bertingkat (*Successive Approximation* ADC disingkat SAC), adalah jenis ADC yang mungkin paling banyak digunakan, dibandingkan dengan counting ADC, waktu konversi SAC jauh lebih pendek dan selalu konstan, tidak tergantung pada nilai sinyal analog yang akan diubah. Pada gambar 2-9 menunjukkan blok diagram SAC yang disederhanakan.



Gambar 2-9 Blok Diagram SAC Yang Disederhanakan.

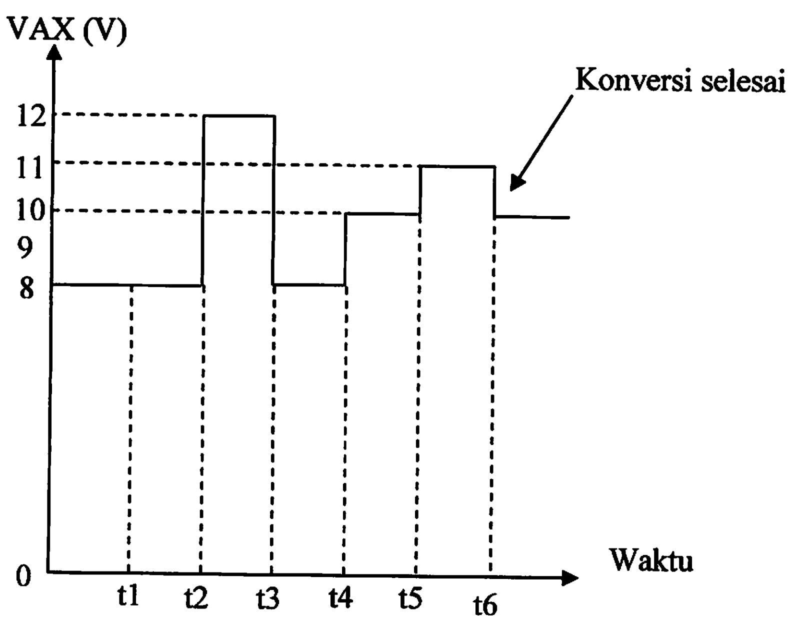
Cara kerjanya adalah sebagi berikut:

SAC tidak menggunakan pencacah, sebagai penggantinya digunakan register kontrol (*control register*, juga disebut *Successive Approximation Register*, SAR) yang isinya dapat diubah bit demi bit oleh suatu logika kendali. Proses konversi dimulai dengan memberikan pulsa start. Akibat pulsa start ini, logika kendali akan me-reset semua bit dalam register kontrol, sehingga keluaran register semuanya sama dengan 0 dan VAX = 0 volt. Karena itu VAX<VA, sehingga keluaran *komparator* akan tinggi. Karena logika 1 ini, logika kendali akan men-set MSB register kontrol menjadi logika 1, dengan demikian sekarang VAX akan sama dengan bobot MSB dikalikan step size DAC. Kalau sekarang ternyata VAX > VA, keluaran *komparator* akan berubah menjadi logika 0. Karena sinyal logika 0 ini, logika kendali akan me-reset MSB tadi kembali menjadi logika 0. Kemudian logika kendali akan men-set bit berikutnya (MSB kedua) menjadi logika 1.

Sebaliknya kalau tadi ternyata VAX < VA, keluaran *komparator* akan tetap tinggi. Karena sinyal tinggi ini, logika kendali akan membiarkan MSB tetap tinggi. Logika kendali kemudian akan men-set bit berikutnya (MSB kedua) menjadi tinggi.

Proses yang diuraikan diatas di-ulang sampai semua bit dicoba, dimulai dari MSB, kemudian MSB kedua, MSB ketiga, dan seterusnya sampai LSB. Setelah LSB selesai dicoba, proses konversi selesai, dan logika kendali akan mengeluarkan EOC (*end of conversion*). Setelah konversi selesai, *register control* berisi bilangan biner yang ekivalen dengan nilai sinyal *analog* VA.

Gambar 2-10 memperlihatkan bentuk sinyal VAX sebagai fungsi waktu untuk sebuah SAC 4 bit dengan VA= 10,4 volt, dan step size 1 volt.



Gambar 2-10 Contoh Keluaran Vax Untuk SAC 4 Bit Dengan Va=10,4 dan Step Size 1 Volt.

Dari uraian diatas dapat diambil kesimpulan sebagi berilut:

- Nilai keluaran digital SAC tidak dapat melebihi nilai sinyal analog yang akan diubah dengan nilai lebih dari tegangan ambang (*threshold*) VT dari *komparator* yang digunakan.
- Waktu konversi SAC selalu konstan, dan ditentukan oleh jumlah bit serta periode sinyal *clock* yang digunakan.

2.6. LCD (*Liquid Cristal Display*).

LCD Display Module M1632 buatan Seiko Instrument Inc. terdiri dari dua bagian, yang pertama merupakan panel LCD sebagai media penampil informasi dalam bentuk huruf / angka dua baris, masing-masing baris bisa menampung 16 huruf / angka.

Bagian kedua merupakan sebuah sistem yang dibentuk dengan mikrokontroler yang ditempelkan dibalik pada panel LCD, berfungsi mengatur tampilan informasi serta berfungsi mengatur komunikasi M1632 dengan *mikrokontroler* yang memakai tampilan LCD itu. Dengan demikian pemakaian M1632 menjadi sederhana, sistem lain yang M1632 cukup mengirimkan kode-kode ASCII dari informasi yang ditampilkan seperti layaknya memakai sebuah printer.

LCD M1632 mempunyai spesifikasi sebagai berikut :

1. Memiliki 16 karakter dan dua baris tampilan yang terdiri dari 5 x 7 dot matrik ditambah dengan kursor.

2. Pembangkit karakter ROM untuk 192 jenis karakter.

3. Pembangkit karakter RAM untuk 8 jenis karakter.

4. 80 x 8 display data RAM (max 80 karakter).

5. Isolator didalam modul.

6. Memerlukan catu daya ± volt

7. Otomatis reset saat catu daya dinyalakan.

LCD modul M1632 mempunyai 16 pin dengan fungsi dapat dilihat pada tabel 2-3.

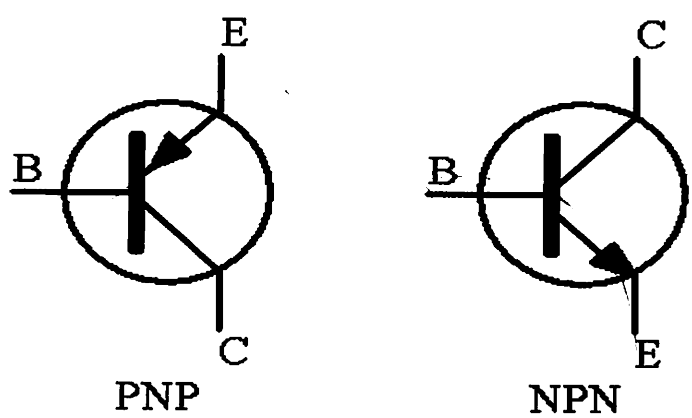
Tabel 2.2 Fungsi Pin – Pin LCD.

Pin No	Symbol	Level	Keterangan
1	VSS	-	Power Supply
2	Vcc		
3	Vee		
4	RS	H/L	H : Data Input L : Instruction Input
5	R/W	H/L	H : Read L : Write
6	E	H/L	H : Enable L : Disable
7	DB0	H/L	Data Bus
8	DB1	H/L	
9	DB2	H/L	
10	DB3	H/L	
11	DB4	H/L	
12	DB5	H/L	
13	DB6	H/L	
14	DB7	H/L	
15	V+BL	-	Back Light Supply
16	V-BL		

2.7. TRANSISTOR.

Untuk hubungan ke luar tiap lapis itu diberi penghantar, transistor adalah suatu mono kristal yang memiliki sifat kelistrikan *semikonduktor*, artinya : hantaran *(konduktivitas)* listriknya lebih rendah dari penghantar *(konduktor)*, tetapi lebih tinggi dari penyekat *(isolator)*. Bahan dasar transistor adalah *germanium (Ge)* atau *silikon (Si)*. Fungsi umum transistor sebagai penguat, memperkuat tegangan atau kuat arus listrik, atau dengan perkataan lain memperkuat daya listrik.

Berdasarkan susunan (lapis) bahannya terdapat dua jenis transistor, yaitu : Transistor *PNP* dan transistor *NPN*. Pada daerah tipe *N* mempunyai banyak *elektron* pita konduksi dan daerah *P* mempunyai banyak *hole*. Pada transistor *PNP* lapis *P* yang satu disebut *emitor*, lapis *P* yang lain disebut *kolektor*, sedang lapis *N*-nya disebut *basis*. Pada transistor *NPN* lapis *N* yang satu disebut *emitor*, lapis *N* yang lain disebut *kolektor*, sedangkan lapis *P*-nya disebut *basis*. mempunyai tiga buah kaki yaitu basis *(base)*, kolektor *(collector)*, emitor *(emitter)*.



Gambar 2-11. Simbol Transistor.

Pada perencanaan ini, menggunakan transistor *NPN* yang ditunjukkan pada gambar diatas yaitu arah perjalanan arus dari kaki *kolektor* menuju kaki *emitor* dimana transistor *NPN* akan on jika basis dari transistor diberi catu positif diatas 0,7 volt memiliki beberapa parameter antara lain *Ic, Ib,* dan *Hfe* dimana hubungan antara ketiganya dinyatakan dalam persamaan dibawah ini :

$$Ic = Hfe \times Ib \qquad (2.13)$$

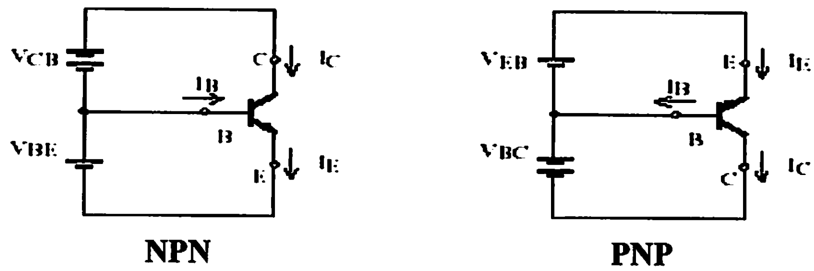
$$Ib = \frac{Ic}{Hfe} \qquad (2.14)$$

$$Hfe_{max} = \frac{Ic\max}{Ib\max} \qquad (2.15)$$

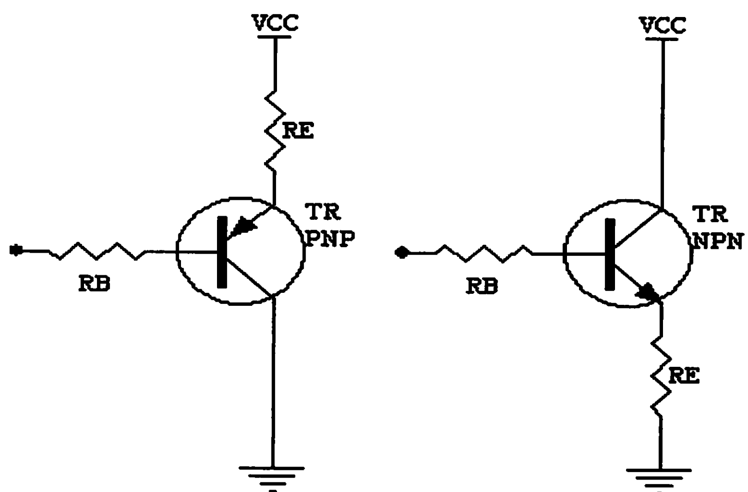
Hfe pada masing – masing transistor tidaklah sama, karena pada data sheet tertera spesifikasi *Ib*max dan *Ic*max yang berbeda. Semakin besar *Hfe* pada transistor, maka semakin baik pula transistor tersebut.

2.7.1.Transistor Sebagai Switch.

Transistor ini digunakan sebagai *switch*, artinya bahwa transistor dioperasikan pada salah satu dari *saturasi* / titik sumbat, tetapi tidak ditempat-tempat sepanjang garis beban(Albert Paul Malvino,1995:128)[5]. Pada kondisi on, tegangan gerbang sumber lain akan memindahkan titik operasi ke puncak dari garis beban, maka arus akan mengalir. Tegangan yang terdapat pada transistor dinamakan tegangan *saturasi.* Jika sebuah transistor berada pada keadaan *saturasi*, maka transistor tersebut bekerja sebagai *switch* yang tertutup dari *kolektor* ke *emitter.* Jika transistor tersumbat *(cutoff),* transistor bekerja seperti *switch* yang terbuka. Rangkaian transistor sebagai *switch* dapat dilihat pada gambar berikut:



Gambar 2-12. Polaritas Tegangan dan Arah Arus.



Gambar 2-13. Rangkaian Transistor Sebagai *switch.*

Persamaan yang dapat diperoleh dari rangkaian diatas :

$$Ib = \frac{Vbb - Vbe}{Rb} \quad \text{...} \quad (2.16)$$

$$Ic = \frac{Vcc}{Rc} \qquad \text{...} \qquad (2.17)$$

Transistor akan aktif bila hubungan *(junction) emitor-basis* dibias maju *(forward bias)* dan *kolektor-basis* diberi bias mundur *(reverse bias)*. Hubungan antara *Ic* dan *Vce* pada garis beban *dc* merupakan tempat kedudukan semua titik kerja *DC* dari transistor pada hambatan beban tertentu.

Garis beban *dc* tersebut mempunyai titik potong dengan sumbu tegak pada $Ic = \frac{Vcc}{Rc}$ untuk $Vce = 0$ dan titik potong dengan sumbu datar pada $Vce = Vcc$ untuk $Ic = 0$. Jika hubungan *emitor-basis* dan *kolektor-basis* diberi bias mundur, maka transistor akan berada pada keadaan *cutoff*, sedangkan jika hubungan *emitor-basis* dan *kolektor-basis* dibias maju, maka transistor menjadi jenuh *(saturasi)*.

Untuk saklar dalam posisi terbuka *(off)* transistor dalam keadaan *cutoff* dan untuk saklar dalam kondisi tertutup *(on)*, maka transisror dalam keadaan *saturasi*, sehingga arus *basis* dan arus *kolektor* dapat dicari dengan persamaan sebagai berikut :

$$Vbb - Ib \times Rb - Vbe = 0 \qquad \text{.......................................} \qquad (2.18)$$

$$Ib = \frac{Vbb - Vbe}{Rb} \qquad \text{.......................................} \qquad (2.19)$$

$$Ic = \beta \times Ib \qquad \text{.......................................} \qquad (2.20)$$

Arus *kolektor* akan menimbulkan tegangan sebesar *Ic x Rc* pada *resistor kolektor*. Karena itu, tegangan *kolektor* menjadi :

$$Vcc - Ic \times Rc - Vce = 0 \quad \ldots\ldots\ldots\ldots \quad (2.21)$$

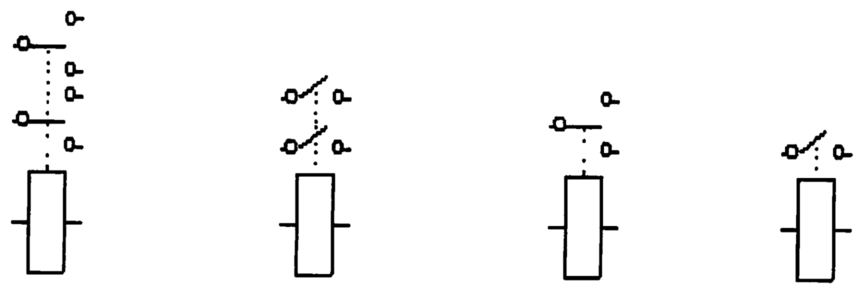
$$Vce = Vcc - Ic \times Rc \quad \ldots\ldots\ldots\ldots \quad (2.22)$$

2.8. RELAY.

Relay adalah suatu perangkat switch (saklar) yang dioperasikan oleh gaya elektromagnetik yang dihasilkan oleh kumparan yang berada didalamnya. Relay ini pada umumnya digunakan untuk menyambung dan memutuskan hubungan antara suatu bagian dengan bagian yang lain dalam suatu rangkaian elektronik, selain itu juga dimaksudkan untuk mengisolasi switching antara tegangan catu tinggi dengan tegangan catu rendah. Kerugian yang ditemui pada relay yaitu adanya tanggapan waktu (response time) saat on maupun off yang relatif lambat serta adanya efek induksi balik sesaat setelah relay off. Oleh sebab itu maka antara IC pengendali dan relay perlu diisolasi dengan suatu rangkaian isolasi.

Relay terdiri dari 4 jenis yaitu :

- DPDT (Double-Pole, Double-Throw)
- SPDT (Single-Pole, Double-Throw)
- DPST (Double-Pole, Single-Throw)
- SPST (Single-Pole, Single-Throw)
-



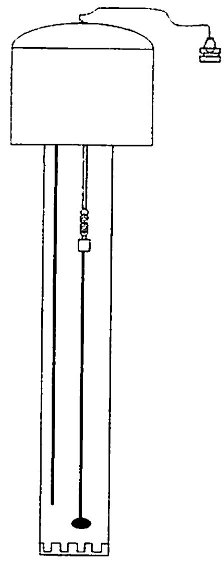
(a) DPDT (b) DPST (c) SPDT (d) SPST

Gambar 2-14. Jenis-Jenis Relay.

2.9. TRANDUSER pH.

Tranduser pH adalah tranduser yng digunakan untuk mengukur tingkat keasaman suatu larutan tertentu. Dalam pembuatan sistem ini digunakan elektrode kombinasi sebagai tranduser pH. Kombinasi ini merupakan elektroda gabungan antara elektroda pengukur dan elektroda referensi. Cara kerja dari elektroda ini secara prinsip sama dengan elektroda-elektroda yang lain yang terdapat dipasaran. Seperti elektroda tipe PE – 03 buatan Taiwan yang akan dipakai dalam pembuatan alat ini, yang mempunyai kriteria sebagai berikut :

- Batas suhunya 5 -60 °C (41 – 140 °F)
- Lebar daerah pengukuran dari pH 1 – 13
- Terbuat dari bahan *epoxy*
- Kabel BNC



Gambar 2-15. Elektrode type PE – 03.

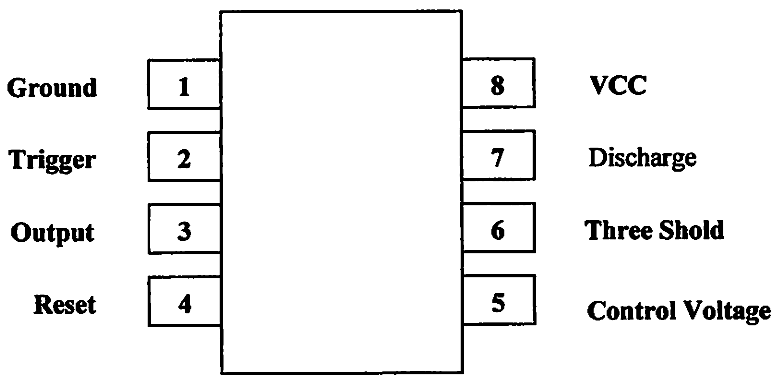
2.9.1.Tranducer pH Capasitif.

Rangkaian pewaktu monolit NE/SE 555 adalah pengatur yang mantap yang mampu membangkitkan tundaan waktu ataupun guncangan yang cermat. Ada terminal-terminal tambahan guna penyulutan atau pengkondisian ulang (reset), kalau diinginkan.

Dalam ragam operasi tundaan waktu, waktu dikemudikan dengan teliti dengan resistor dan kondensator ekstern. Untuk beroperasi tak mantap sebagai osilator, frekuensi bebas, dan daur aktif (duty cycle) dikemudikan dengan teliti oleh dua resistor dan satu kondensator ekstern.

Rangkaiannya akan dapat disulut dan direset pada bentuk gelombang yang sedang jatuh, dan susunan keluarannya akan dapat merupakan sumber ataupun benanan (sink) sampai 200mA ataupun dapat menggerakkan rangkaian TTL.

RC 555 dapat beroperasi dalam jelajahan suhu dari $0^{O}C$ hingga $+70^{O}C$. RM 555 tahan terhadap suhu lebih tinggi, dan beroperasi dalam $-55^{O}C$ hingga $+125^{O}C$.



Gambar 2-16. Diagram Koneksi.

Sifat-sifat :

- Waktu mati (off) kurang dari 12μ det.
- Frekuensi operasi tertinggi besar dari 500 KHz.
- Beroperasi dalam ragam tak stabil dan monostabil.
- Arus keluaran tinggi.
- Daur aktif (duty cycle) dapat disetting.
- Serba cocok dengan TTL.
- Kemantapan suhu 0,005% per ^{O}C.

Mono stabil :

$t \approx 1{,}1 \text{ X } R_A \text{ X } C$

Tak Stabil :

$t1 \approx 0{,}7 \text{ X } (R_A + R_B) \text{ X } C$

$t2 \approx 0{,}7 \text{ X } R_B \text{ X } C$

$T = t1 + t2$

Penerapan :

- Pewaktuan (timing) dengan cermat.
- Pembangkit denyut.
- Pewaktuan sekuensi.
- Pembangkitan tundaan waktu.
- Pemodulasian lebar denyut.
- Pemodulasian posisi denyut
- Detector denyut hilang.

Blok diagram untuk perancangan pengontrol tingkat keasaman tingkat kekeruhan pada sistem pengolahan air minum ini adalah untuk menjaga kestabilan untuk keasaman adalah antara 6.5 -7.5.

Fungsi dari setiap blok diagram yang ada pada gambar :

- Rangkaian single chip AT Mega 8515 mengolah data input untuk menjaga agar nilai keasaman yang ditampilkan oleh pH elektroda tetap antara 6.5 – 7.5.
- Sensor keasaman berfungsi untuk mengukur perubahan pH air, keluaran dari pH elektroda adalah berupa tegangan dan dapat bekerja pada skala antara pH 1 -14.
- Sensor kekeruhan berfungsi untuk mengukur perubahan dari tingkat kejernihan air yang diolah, dimana pada sensor kekeruhan bekerja berdasarkan LDR sebagai sensor penerima cahaya akan mendeteksi intensitas cahaya yang masuk ke LDR tersebut.
- Rangkaian Operasional Amplifier (penguat Op-Amp) menguatkan nilai keluaran dari masing masing sensor, yakni sensor keasaman dan sensor kekeruhan yang mempunyai nilai tegangan yang kecil. Penguat ini bertujuan untuk mengkondisikan input.
- Rangkaian ADC 0804 mengubah level tegangan analog menjad data digital.
- Rangkaian driver relay bertujuan untuk menyambungkan dan memutuskan arus yang mengalir pada motor penggerak katup dan motor pompa.
- Motor AC digunakan untuk mengaduk larutan dan juga untuk memompa air menuju penyaring.

- Rangkaian display digunakan untuk menampilkan nilai pH yang terdapat pada larutan.

3.2.2.Rangkaian Pengontrol Tingkat Keasaman dan Tingkat Kekeruhan Air.

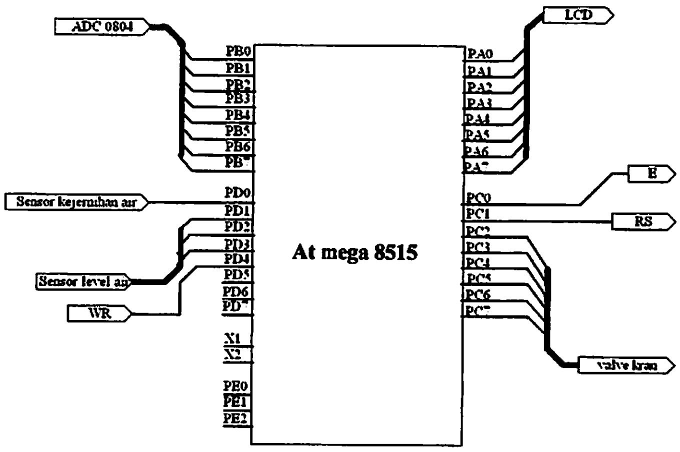
Perancangan rangkaian sebagai pengontrol terhadap nilai keasaman dan kekeruhan yang berubah pada sistem pengolahan air minum menggunakan beberapa komponen, yaitu pH elektroda, LDR, ADC 0804, penguat Op-Amp, transistor sebagai driver relay, valve asam dan valve basa, motor pengaduk dan pompa, dan LCD sebagai display.

3.3. Mikrokontroller AT Mega 8515.

3.3.1.Mikrokontroller AT Mega 8515.

Mikrokontroller AT Mega 8515 ini adalah suatu chip IC yang dirancang untuk dapat berdiri sendiri karena terdapat EEPROM, RAM serta port Input/Output dan perlengkapan lainnya dengan tujuan menambah kemudahan dalam aplikasinya juga dalam softwarenya.

Mikrokontroler yang digunakan pada sistem adalah mikrokontroler jenis AT Mega 8515 yang merupakan IC AVR 8 Bit Internal RAM, 40 Pin dan 35 Port I/O. Dalam perancangan sistem ini pin-pin yang dipergunakan adalah sebagai berikut:

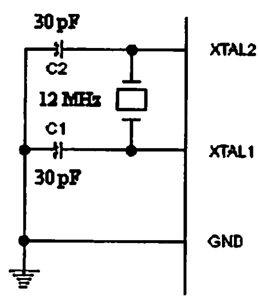


Gambar 3-2. Kedudukan Kaki-Kaki Mikrokontroler AT Mega 8515.

1. Pin PB0 sampai dengan pin PB7 adalah masukan dari ADC.
2. Pin PA0 sampai dengan pin PA7, pin PC0 dan pin PC1 adalah data untuk tampilan LCD.
3. Pin PD0 untuk input data dari LDR.
4. Pin X2 Untuk Clock Pada Mikrokontroler AT Mega 8515.
5. Pin X1 Untuk Clock Pada Mikrokontroler AT Mega 8515.
6. Pin 20 (GND) Untuk Vss Pada Mikrokontroler AT Mega 8515.
7. Pin PC2 sampai dengan pin PC7 untuk keluaran ke driver motor dan driver valve sumber air, kran asam, kran basa dan kran pembuangan air.
8. Pin 22 (P2.1) untuk keluaran ke driver valve asam.
9. Pin 23 (P2.2) untuk keluaran ke driver valve basa.
10. Pin PE1 (ALE/VPP) dihubungkan ke +Vcc untuk mengakses memori internal.
11. Pin 40 (Vcc) dihubungkan ke catu daya sebesar Vcc +5 Volt.
12. Pin 9 (Rst) jika diberi logika tinggi untuk reset sistem.

3.3.2.Pewaktuan CPU.

Mikrokontroler AT Mega 8515 memiliki Oscilator Internal (On Chip Osilator) yang dapat digunakan sebagai clock bagi CPU. Untuk menggunakan oscilator internal diperlukan sebuah kristal atau resonator keramik antara pin XTAL 1 dan XTAL 2 dan sebuah kapasitor ke ground seperti gambar 3-4. Untuk kristalnya dapat digunakan frekuensi dari 6-12 Mhz. Sedangkan untuk kapasitor bernilai antara 27 pF sampai 33 pF. Bila menggunakan clock eksternal, rangkaiannya dihubungkan seperti gambar 3-3.

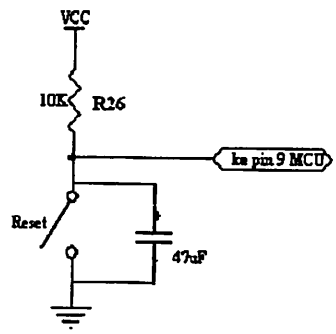


Gambar 3-3. Rangkaian Clock Minimum Sistem.

3.3.3.Rangkaian Reset.

Reset pada Mikrokontroler merupakan masukkan aktif high '1' pulsa transisi dari rendah '0' ke tinggi '1' akan mereset Mikrokontroler menuju alamat 0000H. Pin reset dihubungkan dengan rangkaian power on reset seperti pada gambar 3-4.

Rangkaian Reset bertujuan agar Mikrokontroler dapat menjalankan proses dari awal. Rangkaian reset untuk Mikrokontroler dirancang agar mempunyai kemampuan power on reset, yaitu reset yang terjadi pada saat sistem dinyalakan untuk pertama kalinya. Reset juga dapat dilakukan secara manual dengan menambahkan tombol reset yang berupa Swicth Push Button.



Gambar 3-4. Rangkaian Power On Reset.

3.3.4.Cara Kerja ATMEGA 8515

Cara kera MCU dalam mengontrol kran air dan menerima data pH adalah jika Kondisi dari larutan mempunyai pH yang tidak dinginkan maka data dari sensor akan dikonversi oleh ADC yang mana akan menjadi masukan dari MCU, setelah data yang diterima maka MCU akan mengkonversi data tersebut dan akan mengeluarkan data keluaran (kondisi *High*) pada pin-pin yang digunakan untuk mengontrol *driver* pompa sehingga pompa akan aktif, kondisi ini akan berlangsung terus-menerus sampai kondisi pH larutan sesuai dengan keinginan. Jika kondisi ini sudah terpenuhi maka data masukan dari sensor pH akan dikonversi oleh ADC dan keluaran dari ADC akan menjadi masukan dari MCU kemudian data ini akan dikonversi dan akan mengontrol *driver* pompa untuk me-nonaktifkan pompa.

3.4. Perancangan Pengkondisi Sinyal.

3.4.1.Perancangan komparator.

LDR merupakan tranduser yang merubah besaran cahaya menjadi besaran tegangan. Dalam intensitas cahaya normal, resistansi LDR akan rendah. LDR akan menghasilkan nilai resistensi yang besarnya sebanding dengan besarnya intensitas cahaya yang diterima.

Untuk pendeteksian kekeruhan suatu larutan digunakan sensor kekeruhan (LDR). Sesuai dengan karakteristik LDR dimana tegangan keluaran sebesar 2 volt.

Tegangan di titik A berbanding terbalik dengan nilai resistansi LDR, yaitu semakin rendah intensitas cahaya maka resistansi LDR semakin besar dan tegangan di titik A semakin kecil, sehingga tegangan di titik A digunakan sebagai masukkan *non inverting* pada komparator. Agar rangkaian aktif pada saat tegangan di titik A $\leq$ 2 volt, maka tegangan referensi pada kaki *inverting* diset sebesar 2 volt.

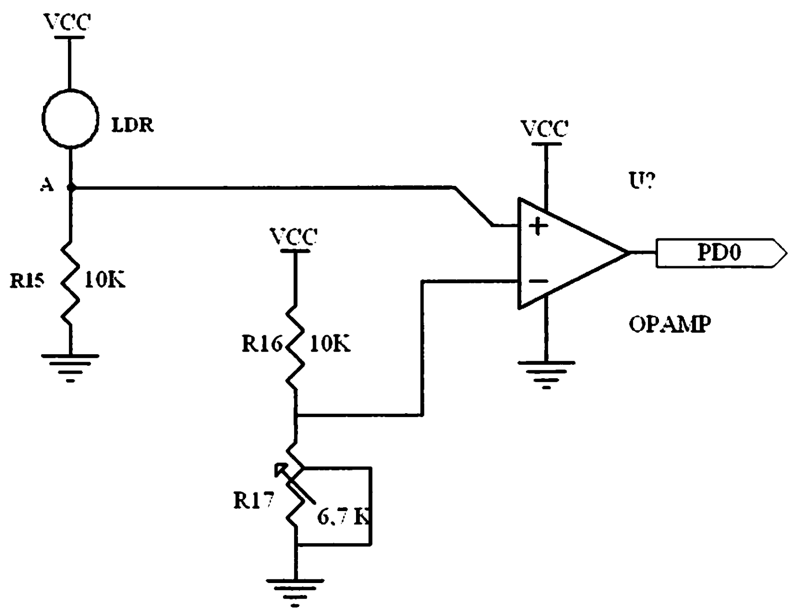
Karena nilai tegangan keluaran dari LDR sebesar 2 volt, maka tegangan referensi Vref (-) perlu diset pada tegangan 2 volt, sehingga pada saat mendeteksi air yang keruh maka komparator akan memberikan logika keluaran tinggi (5 volt). Pada perancangan ini R16 dan R17 diset untuk mendapatkan Vref sebesar 2 volt dengan menggunakan Persamaan:

$$R17 = \frac{Vref \times R16}{Vcc - Vref}$$

$$R17 = \frac{2 \times R16}{5 - 2}$$

$$R17 = \frac{2}{3} R16$$

Jika R16=10 kΩ, maka besar R17= 6,7 kΩ



Gambar 3-5. Rangkaian Komparator.

Cara kerja sensor kekeruhan :

LDR akan mengeluarkan tegangan bila terkena cahaya. Pada saat air keruh masuk maka LDR akan menerima sedikti sekali cahaya dan akan mengeluarkan tegangan yang kecil pula. Tegangan ini akan memicu mikrokontroller untuk menyalakan pompa menuju tabung penyaringan. Setelah beberapa kali penyaringan, maka air akan mulai terlihat jernih dan intensitas cahaya yang masuk menuju LDR akan besar dan menghasilkan tegangan yang besar pula. Bila tegangan keluaran dari LDR sesuai dengan inputan pada mikrokontroller maka pompa akan berhenti memompa secara otomatis.

Fungsi Tembaga dan besi :

Tembaga dan besi digunakan untuk memberikan respon kecepatan aliran arus listrik dimana pekat tidaknya suatu larutan menjadi bagian penting dalam menentukan kecepatan respon arus.

3.4.2.Perancangan Instrumentasi.

Penguat instrumentasi diperlukan untuk memperkuat output dari rangkaian sensor Asam basa yang merupakan besaran analog yang sangat kecil sehingga sesuai dengan level tegangan ADC sehingga dapat dikonversikan oleh ADC 0804.

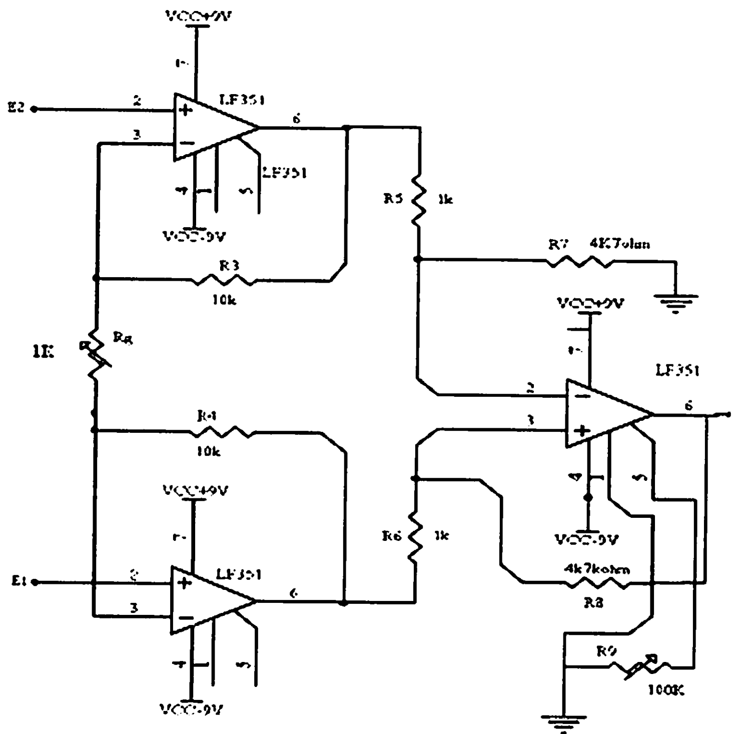
Penguat Instrumentasi yang digunakan dalam perancangan ini menggunakan IC penguat Operasional LF 351. IC ini dipilih karena dapat beroperasi pada tegangan catu + 12V.

Output dari rangkaian sensor asam/basa berkisar antara 1mV-50 mV,. Jika penguatan ditentukan sebesar 100 kali dan jika ditentukan besarnya tahanan R3=R4=10KΩ dan R5=R6= 1KΩ dan R7 dan R8 ditentukan sebesar 4,7 KΩ, maka nilai Rg sebesar :

$$\frac{Vo}{(E_2 - E_1)} = \left(1 + \frac{2R3}{Rg}\right)\left(\frac{R7}{R6}\right)$$

$$100 = \left(1 + \frac{2 \times 10K}{Rg}\right)\left(\frac{4,7K}{1K}\right)$$

Rg = 0,986 $K\Omega \cong 1K\Omega$



Gambar 3-6 Rangkaian Penguat Instrumentasi.

Fungsi dari penggunaan Op-amp Type LF 351 adalah sebagai penguat dimana dengan menggunakan type ini Penguatan yang didapat lebih besar dan *low noise.* Sehingga didapatkan hasil penguatan lebih baik yang sesuai dengan kebutuhan.

3.5. Perancangan Rangkaian ADC

Agar dapat diproses oleh mikrokontroler maka sinyal yang masuk kedalam mikrokontroler harus dikonversikan terlebih dahulu menjadi sinyal digital dengan menggunakan rangkaian ADC.

Rangkaian ADC ini mempunyai 8 bit keluaran (DB_0-DB_7) yang dihubungkan ke masukan mikrokontroller. Sedangkan masukannya adalah keluaran sensor asam/basa yang telah diperkuat, yang dihubungkan ke terminal Vin(+). Masukan dari ADC ini dibatasi antara 0 sampai 5 volt (*datasheet*).

ADC 0804 membutuhkan tegangan referensi per dua ($V_{ref}/2$) sebesar setengah dari jangkauan masukan analognya. Karena masukan tegangan analog yang direncanakan maksimum sebesar 5 volt maka dibutuhkan tegangan referensi 2,5 volt.

Tegangan ini didapat dengan meggunakan persamaan pembagi tegangan dimana ditentukan nilai resistansi dari R13=R19 sebesar 1KΩ yang terhubung paralel, sehingga digunakan persamaan pembagi tegangan, berikut ini adalah perhitungan tegangan referensi :

$$V_{\frac{ref}{2}} = \frac{R_{13} \times V_{ref}}{R_{13} + R_{14}} = \frac{1k\Omega \times 5V}{1k\Omega + 1k\Omega} = 2{,}5V$$

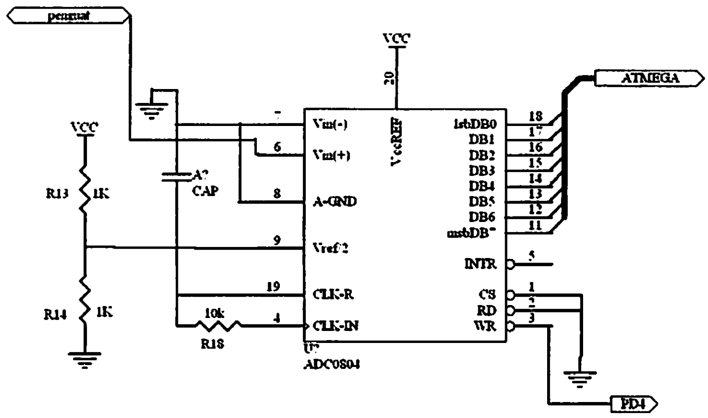
Besarnya tegangan setiap step atau Resolusi tegangan pada ADC adalah :

$$\text{Besarnya tegangan setiap step} = \frac{Vref}{2^n - 1}$$

$$= \frac{5V}{2^8 - 1}$$

$$= 19{,}6 \text{ mV}$$

Artinya keluaran biner ADC akan bertambah satu setiap kenaikan tegangan input sebesar 19,6 mV. Rangkaian ADC 0804 didalam perancangan sistem ini ditunjukkan dalam Gambar 3-7.



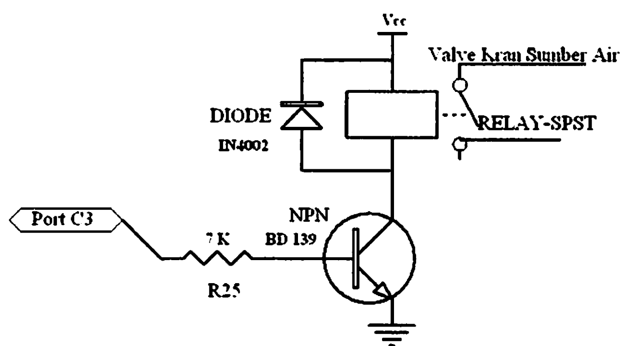
Gambar 3-7 Rangkaian ADC0804.

3.6. Perancangan Driver.

Perancangan driver ini memanfaatkan keluaran dari port PC2 – PC6, sebagai pemicu driver relay kali ini menggunakan transistor BD 139.

Pemasangan dioda digunakan untuk membalik arah arus dalam loop tertutup pada saat $I_B=0$ atau pada saat port C3 kondisi low. Dan jika port C3 kondisi high maka arus relay (I_{relay}) akan mengalir dan menimbulkan medan magnet sehingga besarnya tegangan pada induktansi adalah

$$V = \frac{-Ldi}{dt}$$



Gambar 3-8. Rangkaian Driver Motor dan Driver Valve.

Transistor *switching* berfungsi untuk mengkondisikan tegangan dari mikrokontroler secara *switching* dan difungsikan sebagai saklar untuk relay pompa.

Perhitungan dari rangkaian pompa dalam Gambar 3-8 terlebih dahulu harus dicari nilai R25=Rb. Data yang diperlukan untuk mencari besar resistansi Rb adalah sebagai berikut:

Data relai yang digunakan dalam perancangan adalah:

- Besar pengukuran tahanan dalam relai ($R_{relai\ II} = R_{c\ II}$) = 170 Ω.

Data transistor BD139 yang diperoleh dari datasheet (motorola *semiconductor*, 1995) adalah:

- V_{ce} saturasi = 0,5 volt.
- h_{fe} minimum = 40
- V_{be} Max = 1 volt.

Dengan resistansi relai sebesar 170 Ω, tegangan catu sebesar 5 V, dan V_{ce} saturasi sebesar 0,5 V maka besar arus I_{relai} adalah :

$$I_{relai} = \frac{Vcc - Vce}{R_{relai}}$$

$$I_{relai} = \frac{9V - 0{,}5V}{170\Omega} = 50 \text{ mA}$$

Dengan *hfe* minimum 40 maka digunakan persamaan sehingga besar arus basis

$$I_b = \frac{Ic}{hfe}$$

$$I_b = \frac{50mA}{40} = 1{,}25 \text{ mA}$$

Jika V_{OH} adalah tegangan keluaran dari mikrokontroler saat logika tinggi yaitu sebesar 2,4V dan *Vbe* yang digunakan dari nilai max dalam *datasheet* agar transistor berkerja dengan baik adalah *1 V* maka besar resistansi R25 adalah :

$$R25 \frac{V_{OH} - V_{be}}{Ib}$$

$$R25 \frac{2,4V - 1V}{0,2mA} = 7\ k\Omega$$

3.7. LCD (Liquid Crystal Display)

LCD display Module M1632 buatan Seiko Instrument Inc. Terdiri dari dua bagian, yang pertama merupakan panel LCD sebagai media penampil informasi dalam bentuk huruf/angka dua baris, masing-masing baris bisa menampung 16 huruf/angka.

Bagian kedua merupakan sebuah sistem yang dibentuk dengan mikrokontroler yang ditempelkan dibalik pada panel LCD, berfungsi mengatur tampilan informasi serta berfungsi mengatur komunikasi M1632 dengan mikrokontroler yang memakai tampilan LCD itu. Dengan demikian pemakaian M1632 menjadi sederhana, sistem lain yang M1632 cukup mengirimkan kode-kode ASCII dari informasi yang ditampilkan seperti layaknya memakai sebuah printer. LCD M1632 mempunyai spesifikasi sebagai berikut :

1. Memiliki 16 karakter dan dua baris tampiplan yang terdiri dari 5 x 7 dot matrik ditambah dengan kursor.
2. Pembangkit karakter ROM untuk 192 jenis karakter.
3. Pembangkit karakter RAM untuk 8 jenis karakter.

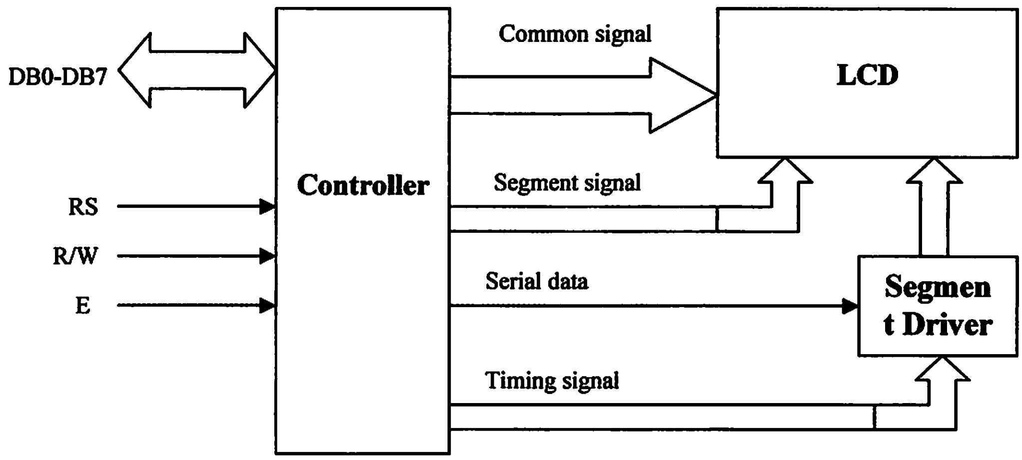
4. 80 x 8 display data RAM (max 80 karakter).

5. Isolator didalam modul.

6. Memerlukan catu daya ± 5 volt.

7. Otomatis reset saat catu daya dinyalakan.

Blok diagram LCD M1632 ditunjukkan dalam Gambar 3-10 dibawah ini :



Gambar 3-9. Blok Diagram LCD M1632.

LCD modul M1632 mempunyai 16 pin dengan fungsi sebagai berikut :

Tabel 3.1 Fungsi Pin-Pin LCD.

No. Pin	Nama Pin	Fungsi
1	**Vss**	Terminal Ground
2	**Vcc**	Tegangan Catu + 5 volt
3	**Vee**	Mengendalikan Kecerahan LCD
4	**RS**	Sinyal Pemilihan Register 0 = Tulis 1 = Baca
5	**R/W**	Sinyal Seleksi Tulis atau Baca 0 = Tulis 1 = Baca
6	**E**	Sinyal operasi awal yang mengaktifkan data tulis atau baca
7 – 14	**DB0 – DB7**	Merupakan saluran data berisi perintah data yang akan ditampilkan
15	**V + BL**	Back Light Supply 5 volt (volt)
16	**V - BL**	Back Light Supply 0 (Ground)

3.8. Perancangan Perangkat Lunak.

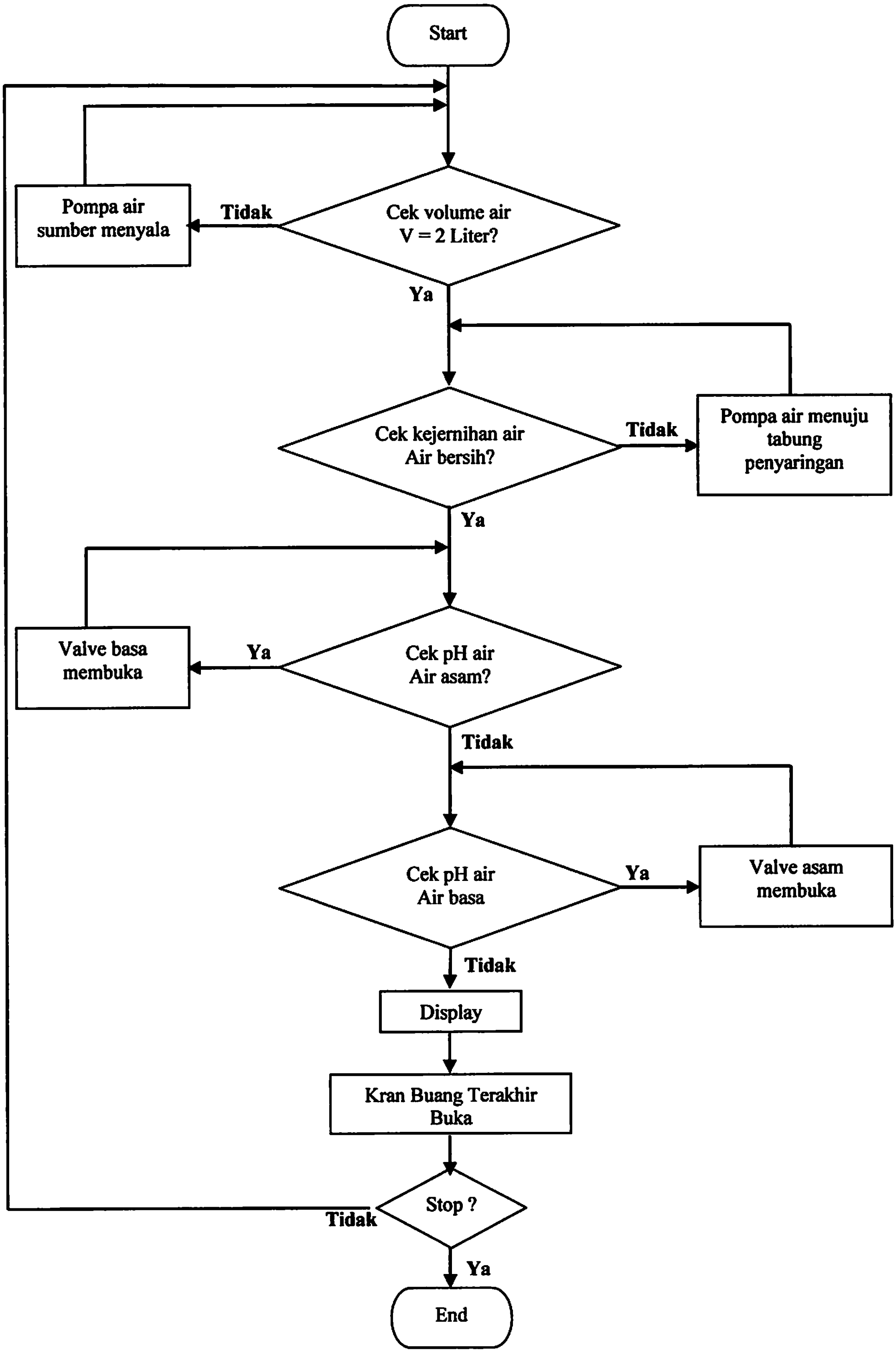
Untuk mengoperasikan alat yang telah dibuat dibutuhkan program dengan bahasa *assembler* yang telah dikompilasi menjadi data *binary* yang kemudian diisikan pada mikrokontroller

Adapun tiap tahap penyusun perangkat lunak untuk setiap bagian rangkaian adalah sebagai berikut :

1. Menyusun diagram alir (flow chart) program masing – masing rangkaian.
2. Membuat perangkat lunak berdasarkan diagram alir yang telah disusun dengan menggunakan bahasa asemmbly.
3. Perangkat lunak yang disusun, dikompile menggunakan sotware MCS – 51. Macroassembler V.2.2. Intel Corporation menjadi data file Object (.OBJ) dan list (.LST).
4. Apabila terjadi kesalahan, memeriksa kembali dengan membuka file yang berekstensi (.LST) untuk mengetahui pada bagian opcode yang mana telah terjadi kesalahan, dan mengulangi tahap b.
5. Bila sudah tidak terjadi kesalahan, mengkompile data file object (.OBJ) ke bentuk data file Hexadesimal (.Hex) dengan menggunakan software OH.1.0 Obj to Hex Intel Corporation.
6. Kemudian data file (.Hex) dikelompokkan menjadi data file Binary (.Bin) dengan menggunakan sotware H.V.2.2 Hex to Binary Converter Sunshine Elecrtonic.

7. Setelah semua proses selesai, program tersebut dimasukkan diisikan ke dalam PROM internal dari tiap mikrokontroller sesuai dengan tiap bagian rangkaian yang dibuat.

3.9. Diagram Flowchart Alat Penjernihan Air Dengan Mengontrol Nilai pH Normal Dengan Menggunakan Mikrokontroller AT Mega 8515.



BAB IV
ANALISA ALAT

4.1. Pendahuluan.

Pada bab ini akan dibahas pengujian dan pengukuran dari yang telah dibuat. Hal ini dilakukan untuk mengetahui kekurangan dan untuk kerja dari sistem yang telah dibuat. Pengujian tersebut meliputi pengujian sensor dan pengujian pengambilan data untuk masing-masing blok yang dipergunakan, sedangkan pengujian perangkat lunak dianggap ideal atau sesuai dengan yang diinginkan. Hasil pengujian selanjutnya dianalisa dengan membandingkan terhadap perancangan.

4.2. Pengujian Masing-Masing Blok.

Pada pengujian ini dilakukan dengan cara melakukan pengukuran terhadap rangkaian masing-masing penguat instrumentasi. Adapun untuk menunjang dilakukannya pengujian maka akan dilakukan langkah-langkah sebagai berikut :

1. Pengujian terhadap sensor pH.
2. Pengujian terhadap sensor kekeruhan.
3. Pengujian terhadap driver.

Dan untuk pengukuran, alat yang digunakan adalah sebagai berikut :

1. Multimeter.
2. Contoh larutan asam dan basa.

3. Contoh kondisi kekeruhan air.

4. Power supply.

4.2.1. Sensor pH.

4.2.1.1. Pengukuran Sensor pH.

Dalam pengujian dan pengukuran ini didapat keluaran tegangan sebesar 1 – 1.4V. Dari hasil perhitungan dan pengukuran sensor pH ini dapat dilihat dalam tabel dibawah ini :

Tabel 4.1 Hasil Pengukuran Dari Nilai pH.

Nilai pH	Kertas lakmus merah	Hasil Perhitungan (volt)	Hasil Pengukuran (volt)	Data output ADC
1	merah	0.1	0.25	$01_{(H)}$
2	merah	0,2	0,35	$0A_{(H)}$
3	merah	0,3	0,4	$35_{(H)}$
4	merah	0,4	0,47	$4A_{(H)}$
5	merah	0.5	0.509	$5C_{(H)}$
6	merah	0.6	0.57	$60_{(H)}$
7	merah	0.7	0.711	$80_{(H)}$
8	biru	0.8	0.78	$9A_{(H)}$
9	biru	0.9	0,85	$A5_{(H)}$
10	biru	1	1.08	$C4_{(H)}$
11	biru	1.1	1.12	$CA_{(H)}$
12	biru	1.2	1.25	$D5_{(H)}$
13	biru	1.3	1.35	$E0_{(H)}$
14	biru	1.35	1.4	$EC_{(H)}$

4.2.1.2.Analisa Data Sensor pH.

Diketahui : Vref = 0.7 V

1 Bit = Vin/2^8

Vref = ½ Vin max

pH_{min} = 1

pH_{max} = 14

VpH_{min}= 1 V

VpH_{max}= 1.4 V

Dicari data output ADC jika pH larutan adalah 7

Perhitungan :

$$K = \frac{pH\max}{VpH\max}$$

$$= \frac{14}{1.4}$$

$$= 10$$

$$VpHout = \frac{pH\max - nilaipH}{K}$$

$$= \frac{14-7}{10} = 0.7\text{ V}$$

VpHout = Vin ADC

$$1\text{ bit} = \frac{Vin}{2^8}$$

$$= \frac{1.4}{2^8}$$

$$= \frac{1.4}{255} = 0.0054902 = 0.0055\text{ mV}$$

$$\text{data ADC} = \frac{Vin}{1\,\text{LSB}}$$

$$= \frac{0.7}{0.0055}$$

$$= 127.27_{(D)} = 7F_{(H)}$$

4.2.2. Sensor Kekeruhan.

4.2.2.1.Pengukuran Sensor Kekeruhan.

Dalam pengukuran dan pengujian didapat keluaran tegangan untuk sensor kekeruhan adalah antara 0.3 – 3.8 Volt. Dari hasil perhitungan dan pengukuran sensor kekeruhan ini dapat dilihat dalam table dibawah ini :

Tabel 4.2 Hasil Pengukuran Sensor Kekeruhan.

Kondisi Air	Tegangan keluaran Pengukuran (Volt)	Kondisi keluaran Komparator
Keruh (air tanah)	0.3 – 0.9	*Low*
Agak keruh (60% air tanah & 40% sumber mata air)	1 – 1.99	*Low*
Agak jernih (40% air tanah & 60 % sumber mata air	2 – 2.99	*High*
Jernih (sumber mata air)	3 – 3.8	*High*

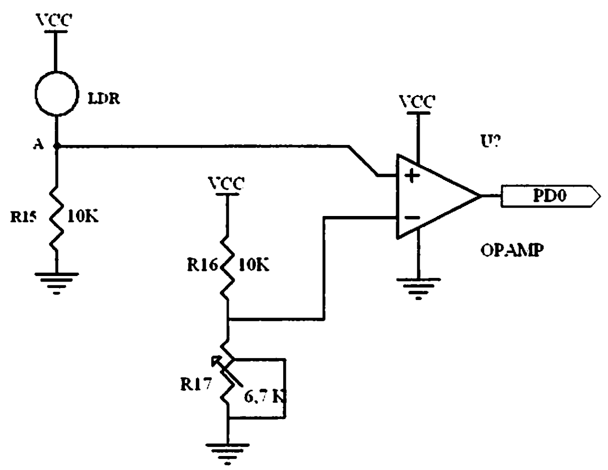
4.2.2.2.Analisa Data Sensor Kekeruhan.

Komparator akan memberikan logika keluaran tinggi (5 volt). Pada perancangan ini R16 dan R17 di set untuk mendapatkan Vref sebesar 2 volt dengan menggunakan persamaan :

$$R17 = \frac{Vref\ x\, R16}{Vcc - Vref}$$

$$R17 = \frac{2}{3} R16$$

Jika R16 = 10kΩ, maka besar R17 = 6,7 kΩ

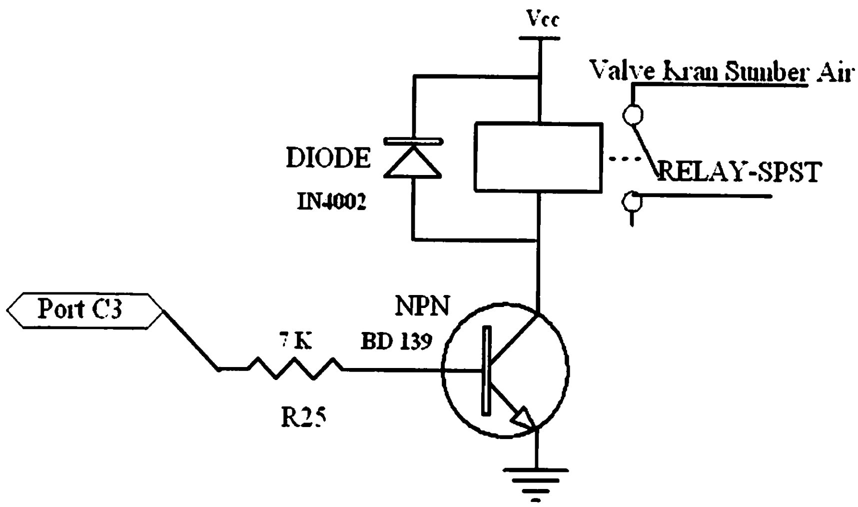


Gambar 4-1 Rangkaian Komparator.

4.2.2.3.Analisa Rangkaian Driver Relay.

Rangkaian pengendali relay pada alat ini digunakan untuk menghubungkan dan memutus hubungan dengan rangkaian dering. Relay yang digunakan dalam rangkaian penghubung dan pemutus ini adalah jenis DPDT

(*Dual Pole Dual Totem*) yang mempunyai resistansi sebesar 170Ω (hasil pengukuran) dan bekerja pada tegangan catu sebesar +5 volt.



Gambar 4-2 Rangkaian Driver relay

Tujuan pengujian rangkaian *driver* pompa adalah untuk mengetahui apakah kerja rangkaian *driver* pompa sesuai perencanaan.

Hasil pengujian *driver* motor ditunjukkan dalam Tabel 4.3. Dari data tersebut diperlihatkan hubungan antara tegangan masukan analog dan keluaran nyala lampu.

Data transistor BD139 yang diperoleh dari datasheet (motorola *semiconductor*, 1995) adalah:

- V_{ce} saturasi = 0,5 volt.
- h_{fe} minimum = 40
- V_{be} Max = 1 volt.

Dengan resistansi relai sebesar 170 Ω, tegangan catu sebesar 5 V, dan V_{ce} saturasi sebesar 0,5 V maka besar arus I_{relai} adalah :

$$I_{relai} = \frac{Vcc - Vce}{R_{relai}}$$

$$I_{relai} = \frac{9V - 0{,}5V}{170\Omega} = 50 \text{ mA}$$

Dengan *hfe* minimum 40 maka digunakan Persamaan (4.18) sehingga besar arus basis

$$I_b = \frac{Ic}{hfe}$$

$$I_b = \frac{50mA}{40} = 1{,}25 \text{ mA}$$

Jika V_{OH} adalah tegangan keluaran dari mikrokontroler saat logika tinggi yaitu sebesar 2,4V dan *Vbe* yang digunakan dari nilai max dalam ***datasheet*** agar transistor berkerja dengan baik adalah *1 V* maka besar resistansi R25 adalah :

$$R25 \; \frac{V_{OH} - V_{be}}{Ib}$$

$$R25 \; \frac{2{,}4V - 1V}{0{,}2mA} = 7 \text{ k}\Omega$$

Tabel 4.3 Hasil Pengujian *Driver* Pompa

Masukan	Lampu
5 volt 0 volt	On Off

Dalam Tabel 4.3 dapat dilihat bahwa hasil pengujian sesuai dengan yang direncanakan.

BAB V
PENUTUP

Bab ini berisi kesimpulan dan saran dari perencanaan dan pembuatan alat penjernihan air dengan mengontrol nilai pH normal berbasis mikrokontroller Atmega 8515.

5.1. Kesimpulan

Hasil dari perencanaan dan pembuatan alat penjernihan air dengan mengontrol nilai pH normal berbasis mikrokontroller atmega 8515. Diambil kesimpulan sebagai berikut:

1. Alat ini bekerja berdasarkan data dari sensor pH untuk mengukur kondisi larutan dalam keadaan asam atau basa dan sensor kejernihan air dengan menggunakan LDR, dimana dari kedua sensor ini akan dikonversi menjadi data digital oleh mikrokontroller Atmega 8515 dan hasil pengukuran ditampilkan oleh LCD. Sehingga jika terjadi kesalahan dalam pembacaan pengukuran maka motor valve akan bekerja mengatasi kondisi keadaan larutan.
2. Dari hasil pengujian alat ini diperoleh spesifikasi alat sebagai berikut:
   - Output dari pengukuran pH berupa tampilan LCD, dan sensor kejernihan digunakan sebagai untuk mengukur perubahan dari tingkat kejernihan air yang diolah, dimana pada sensor kekeruhan bekerja berdasarkan LDR sebagai sensor penerima cahaya akan mendeteksi intensitas cahaya yang masuk ke LDR tersebut.

- Pompa akan bekerja jika LDR mempunyai kondisi *Low* dengan tegangan 0,3 – 1,99 volt dan akan terus bekerja sampai kondisi dari air di tempat penyaringan semula berada pada kondisi normal dan pompa akan mati jika mempunyai pH sebesar 6,5 – 7,5 dan kondisi komparator berlogika *High* dengan tegangan 2-3,8 volt.
- Range pengukuran pH antara 1 – 14.

3. Kesalahan Output yang timbul pada alat ini antara lain diakibatkan oleh:
   - Pembacaan sensor pH dan LDR.
   - Tegangan *offset* op amp yang relatif cukup besar.
4. Hasil perancangan dan pembuatan telah sesuai dengan yang diinginkan.

5.2. Saran

Dari beberapa proses pengujian dan analisa ditemukan beberapa kelemahan yang masih membutuhkan pembenahan. Solusi dan saran yang dapat diberikan adalah :

- Dalam menentukan level volume sebesar 2 liter seharusnya menggunakan sensor untuk mendeteksi ketinggian larutan.
- Penggunaan sensor pH dan LDR yang lebih baik sehingga menghasilkan keluaran yang lebih presisi.

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Frederick W. Hughes. 1994. *Panduan Op-Amp*. Pt. Elex Media Komputindo. Jakarta.

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Peter H Beards. 1987. *Analog and Digital Elektronik* Prendice Hall.

Sergio Franco, *Operational Amplifiers And Analog Integrated Circuits*. Mc Graw Hill Book Co Singapore.

Sutanto.1997. *Rangkaian Elektronika Analog dan Terpadu*. Penerbit Universitas Indonesia.

Wasito S. 1997. *Data Sheet Book 1 (data IC Linier, TTL dan CMOS)*. PT. Elex Media Komputindo. Jakarta.

William D. Cooper. 1978. *Electronic Instrumentation And Measurement Techniques* 2nd Ed. Englewood Cliffs. N.J.. USA: Prentice-Hall.

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LAMPIRAN

INSTITUT TEKNOLOGI NASIONAL
JL. BENDUNGAN SIGUR-GURA 2
MALANG

FORMULIR BIMBINGAN SKRIPSI

Nama : Ronny Andriyanto
Nim : 9917102
Masa Bimbingan : 4-Mei-2006 s/d 4-November-2006
Judul Skripsi : Perencanaan dan Pembuatan Alat Penjernih Air Dengan Mengontrol Nilai pH Normal Berbasis Mikrokontroller AtMega 8515

NO	Tanggal	Uraian	Paraf Pembimbing
1.	5-10-06	Bab I & II Aprv.	[signature]
2.	6-10-06	Bab III	[signature]
3.	16-10-06	Bab III Flow chart belum.	[signature]
4.	17-10-06	Flow chart salah	[signature]
5.	1/3-07	Bab IV	[signature]
6.	14/3 07	Bab IV/V	[signature]
7.			
8.			
9.			
10			

Malang, 2006
Dosen Pembimbing

[signature]

Ir. F. Yudi Limpraptono, MT

Form.S-4a

INSTITUT TEKNOLOGI NASIONAL
FAKULTAS TEKNOLOGI INDUSTRI
JURUSAN TEKNIK ELEKTRO

Formulir Perbaikan Ujian Skripsi

Dalam pelaksanaan Ujian Skripsi Janjang Strata 1 Jurusan Teknik Elektro Konsentasi T. Energi Listrik / T. Elektronika, maka perlu adanya perbaikan skripsi untuk mahasiswa :

NAMA : Ronny A.
N I M : 9917102
Perbaikan meliputi :

1. Bpp volt keluaran pH meter utk pH 1 — 13.
2. Jelaskan fungsi LF351.
3. Jelaskan cara menghasilkan [illegible]
4. Jelaskan fungsi & mekanisme [illegible] dan [illegible] alat [illegible].
5. Jelaskan cara [illegible] ~~mengen~~ [illegible] menggunakan [illegible] air dan menerima data pH & pH meter.

(Jelaskan [illegible] dg membimbing utk kerja)

Malang,

(Ir. Cahyo [illegible])

6. Jelaskan materi [illegible] cara menghasilkan [illegible] sensor utk menyensor air jernih/keruh.

INSTITUT TEKNOLOGI NASIONAL
FAKULTAS TEKNOLOGI INDUSTRI
JURUSAN TEKNIK ELEKTRO

Formulir Perbaikan Ujian Skripsi

Dalam pelaksanaan Ujian Skripsi Janjang Strata 1 Jurusan Teknik Elektro Konsentasi T. Energi Listrik / T. Elektronika, maka perlu adanya perbaikan skripsi untuk mahasiswa :

NAMA : Ronny A.
N I M : 9917102
Perbaikan meliputi :

1) pembahasan Rangk. Non. Inverting!
2) perancangan di sesuaikan dgn Hard ware. !!
3) lihat 40 pin ke LCD.

Malang,

(R. Ronny S, ST. MT)

INSTITUT TEKNOLOGI NASIONAL MALANG
FAKULTAS TEKNOLOGI INDUSTRI
JURUSAN TEKNIK ELEKTRO S-1
KONSENTRASI TEKNIK ELEKTRONIKA

FORMULIR PERBAIKAN SKRIPSI

Nama : Ronny Andriyanto
NIM : 99.17.102
Masa Bimbingan : 4 November 2006 – 4 Mei 2007
Judul Skripsi :

" PERENCANAAN DAN PEMBUATAN ALAT PENJERNIHAN AIR DENGAN MENGONTROL NILAI pH NORMAL BERBASIS AtMEGA 8515 "

No	Tanggal	Uraian	Paraf
1	23 Maret 2007	Tegangan voltage keluaran pH meter untuk pH 1-14	
2		Fungsi LF 351	
3		Cara merangkai MC AtMega8515	
4		Fungsi dan mekanisme tembaga dan besi, dan skema akan MC	
5		Cara MC dalam mengontrol kran air dan menerima data pH dan pH meter	
6		Cara merangkai mekanik sensor untuk mensensor air jernih/keruh	

Mengetahui
Dosen Pembimbing

(Ir. F. Yudi Limpraptono, MT)

Diperiksa dan Disetujui
Penguji I

(Dr. Cahyo Chrysdian, MSc)

INSTITUT TEKNOLOGI NASIONAL MALANG
FAKULTAS TEKNOLOGI INDUSTRI
JURUSAN TEKNIK ELEKTRO S-1
KONSENTRASI TEKNIK ELEKTRONIKA

FORMULIR PERBAIKAN SKRIPSI

Nama : Ronny Andriyanto
NIM : 99.17.102
Masa Bimbingan : 4 November 2006 – 4 Mei 2007
Judul Skripsi :

" PERENCANAAN DAN PEMBUATAN ALAT PENJERNIHAN AIR DENGAN MENGONTROL NILAI pH NORMAL BERBASIS AtMEGA 8515 "

No	Tanggal	Uraian	Paraf
1	23 Maret 2007	Pembahasan Rangakaian Non-inverting	
2		Perancangan Sesuai Dengan Hardware	
3		Pin 15 LCd	

Mengetahui
Dosen Pembimbing

(Ir. F. Yudi Limpraptono, MT)

Diperiksa dan Disetujui
Penguji II

(I Komang Somawirata, ST, MT)

```
;==Setting asam basa PH 7 normal
; Project asam basah
.include "m8515def.inc"
.def    datalcd                    =R25
.def    dataalamat                     =R22
.def    data_adc                       =R24
;
.equu   satuan                =0x0060
.equ    puluhan               =0x0061
.equ    ratusan               =0x0062
.equU   SIMPAN                =0x0063


.EQU    ADC_WR                =PC0
.equ    lcdrs                 =PC6
.equ    lcde                  =PC7



.equ    R_kran_keluaran       =PC2
.equ    R_kran_sumber         =PD5
.equ    R_kran_asam                   =PD2
.equ    R_kran_basa                   =PD3
.equU   INDI_V_ASAM                   =PC1
.equU   INDI_V_BASA                   =PD0
.equU   INDI_V_PENAMPUNGAN    =PD1
.equ    sensor_keruh          =PC0
.equ    R_filter                      =PD6
.equ    tombol                        =PD7


.cseg
.org    $0
                ldi         r16,LOW(RAMEND)                     ;initialisasi
stack Pointer
            out     spL,r16     ;
            ldi     r16,HIGH(RAMEND)    ;
            out     spH,r16     ;
        rjmp    MULAI

;=====================================================================
==
INIALISIASA_LCD:
                ldi             r16,0b11111111  ;INIALISASI PORT SEBAGAI OUTPUT
                out             DDRA,r16
                ldi             r16,0b11111111          ;INIALISASI
                out             DDRB,r16
                ldi             r16,0b11111111          ;INIALISASI
                out             DDRC,r16
                ldi             r16,0b00000000          ;INIALISASI
                out             DDRD,r16
;
                ldi             datalcd,0x30            ; inisialisasi LCD
                rcall   write_inst
                ldi             datalcd,0x38
                rcall   write_inst
            ldi         datalcd,0x20
        rcall   write_inst
                ldi             datalcd,0x28
                rcall   write_inst
                ldi             datalcd,0x08
                rcall   write_inst
                ldi             datalcd,0x01
                rcall   write_inst
            ldi         datalcd,0x0E
        rcall   write_inst
                ldi             datalcd,0x06
```

```
            rcall   write_inst
            ldi             datalcd,0x0D
            rcall   write_inst
            ldi             datalcd,0x0C
            rcall   write_inst
            RET
;
write_inst:
            cbi             PORTC,lcdrs
write_LCD:
            out           PORTA,datalcd
        sbi         PORTC,lcde
            cbi         PORTC,lcde
            NOP
            NOP
            SWAP    DATALCD
            out         PORTA,datalcd
        sbi         PORTC,lcde
            cbi         PORTC,lcde
            rcall       delay
            ret

write_data:
            sbi             PORTC,lcdrs
            rjmp    write_LCD

delay:  ldi         r19,0
delay1: ldi         r20,0x25
dely1:  dec         r20
            brne    dely1
            dec             r19
            brne    delay1
            ret
ldelay:
            ldi             R21,0x15
ld1:    rcall   delay
            dec             R21
            brne    ld1
            ret

Mdelay:
            ldi             R21,0x60
ld3:    rcall   delay
            dec             R21
            brne    ld3
            ret

pldelay:
            ldi             R21,0x5
lp1:    rcall   delay
            dec             R21
            brne    lp1
            ret

barisa:
            ldi         datalcd,0x80                ; menulis di baris atas
tulis16:
            ldi         R17,0x16                ; sebanyak 16 character
            rcall       write_inst
tulis1: lpm
            mov         datalcd,r0
            rcall       write_data
            adiw    zl,1
            dec         r17
            brne        tulis1
            ret
barisb:
        ldi     datalcd,0xC0            ; menulis di baris bawah
```

```
            rjmp          tulis16

;================
AMBIL_ADC:
                CBI                PORTD,ADC_WR          ; start of conversion
                SBI                PORTD,ADC_WR
                RCALL     DELAY
                IN                 DATA_ADC,PORTD
                IN                 r16,PORTD
                RET

;================--------------------==============================
conversi:
                LDI                R30,9
                LDI                R21,$00
                LDI                R18,10                                  ;
                LDI                R20,$00                                 ;DATA
SISA PEMBAGIAN
                LDI                R17,9                                   ;R16 DATA
YANG AKAN DICONVERSI
                CP                 R17,R16
;MEMBANDINGKAN DATA APAKAH KURANG DARI 10
                BRCC      LANGSUL
;;LEBIH DARI 10
KKK:    LDI               R18,10                              ;
L_KUR:  DEC               R16
                DEC                R18

                BRNE      L_KUR
                INC                R21
;HASIL PEMBAGIAN
                cp                 r30,r16
                BRCC      kkX
                RJMP      KKK
KKX:    STS               SATUAN,R16
                CP                 R17,R21
                BRCC      LUNGSUL
                MOV                R16,R21
                LDI                R21,$00
DSF:    LDI               R18,10
KURR:   DEC               R16
                DEC                R18
                BRNE      KURR
                INC                R21
                CP                 R30,R16
                BRCC      HJF
                RJMP      DSF
HJF:    STS               PULUHAN,R16
                STS                RATUSAN,R21
                ret

LUNGSUL:
                LDI                R20,$00
                STS                PULUHAN,R21
                STS                RATUSAN,R20
                RET

LANGSUL:
                LDI                R20,$00
                STS                SATUAN,R16
                STS                PULUHAN,R20
                STS                RATUSAN,R20
                RET
;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;

tampilan_PH:
                ldi                dataalamat,0xc2
                lds                datalcd,satuan
```

```
                rcall   tampilan
                ldi             dataalamat,0xc1
                lds             datalcd,puluhan
                rcall   tampilan
                ldi             dataalamat,0xc0
                lds             datalcd,ratusan
                rcall   tampilan
                LDI             R18,00
                sts             satuan,r18
                sts             puluhan,r18
                sts             ratusan,r18
                ret
;==============
Tampilan:
                LDI             R17,00
                mov             r13,datalcd
                mov             datalcd,dataalamat
                RCALL   WRITE_INST
                ldi             zh,high(2*ANGKA)
                ldi             zl,low(2*ANGKA)
                lpm
                CP              R17,R13
                BRNE    LCDF
                RJMP    SSS
lcdf:   adiw    zl,1
                dec             r13
                brne    lcdf
                LPM
SSS:    MOV             DATALCD,R0
                RCALL   WRITE_DATA
                RET

;=====================
;====mulai program=====
;=====================
mulai:
            RCALL   INIALISIASA_LCD
                ldi             zh,high(2*set1)
                ldi             zl,low(2*set1)
                rcall   barisa
                ldi             zh,high(2*set2)
                ldi             zl,low(2*set2)
                rcall   barisB
                ldi             zh,high(2*set3)
                ldi             zl,low(2*set3)
                rcall   barisa
                ldi             zh,high(2*set4)
                ldi             zl,low(2*set4)
                rcall   barisB
                ldi             zh,high(2*set5)
                ldi             zl,low(2*set5)
                rcall   barisa
                ldi             zh,high(2*set6)
                ldi             zl,low(2*set6)
                rcall   barisB
                ldi             zh,high(2*kosong)
                ldi             zl,low(2*kosong)
                rcall   barisa
                ldi             zh,high(2*kosong)
                ldi             zl,low(2*kosong)
                rcall   barisB

        sbis    PIND,R_kran_basa                        ;melihat isi cairan basah
                rjmp    Liat_Tangki_asam
                ldi             zh,high(2*c_basa)
                ldi             zl,low(2*c_basa)
                rcall   barisa
                ldi             zh,high(2*abis)
```

```
                ldi             zl,low(2*abis)
                rcall   barisB
balik:
ke_1z:  sbic    PIND,R_kran_basa                        ;melihat isi cairan basah
                rjmp    ke_1z
Liat_Tangki_asam:
        sbis    PIND,R_kran_asam                        ;melihat isi cairan asam
                rjmp    ke_start
                ldi             zh,high(2*c_asam)
                ldi             zl,low(2*c_asam)
                rcall   barisa
                ldi             zh,high(2*abis)
                ldi             zl,low(2*abis)
                rcall   barisB
ke_2z:          sbic    PIND,R_kran_asam                        ;melihat isi
cairan asam
                rjmp    ke_2z

ke_start:
                sbi             portd,R_kran_sumber                     ;mengisi
air pada penampungan
ke_4z:  sbis    PIND,INDI_V_PENAMPUNGAN         ;sensor apa udah penuh
                rjmp    ke_4z
                cbi             portd,R_kran_sumber                     ;mengisi
air pada penampungan



        sbic    PINC,sensor_keruh                       ;air kotor
                rjmp    air_kotor
                ldi             zh,high(2*bersih)                       ;keadaan
air bersih
                ldi             zl,low(2*bersih)
                rcall   barisa
                ldi             zh,high(2*kosong)
                ldi             zl,low(2*kosong)
                rcall   barisB
                rcall   ldelay
                rcall   ldelay
                rcall   ldelay
                rjmp    pengukuran_asam_basa

air_kotor:
                ldi             zh,high(2*kotor)                        ;keadaan
air bersih
                ldi             zl,low(2*kotor)
                rcall   barisa
                ldi             zh,high(2*kosong)
                ldi             zl,low(2*kosong)
                rcall   barisB
                sbi             portD,R_filter
ke_5z:  sbic    PINC,sensor_keruh                       ;air kotor
                rjmp    ke_5z
                cbi             portD,R_filter

Pengukuran_asam_basa:                                   ;Pengukuran asam
basa dan
                ldi             zh,high(2*set7)                 ;tampilan asam
basa
                ldi             zl,low(2*set7)
                rcall   barisa
                ldi             zh,high(2*kosong)
                ldi             zl,low(2*kosong)
                rcall   barisB

                rcall   ambil_adc
;kalibrasi asam basa
                LDI             R17,10
```

```
          CP              R16,R17                    ;BRCC kanan lebih kecil
samadengan bercabang
          BRCC     ke_2                       ;R17 LEBIH BESAR TIDAK
BERCABANG/LEBIH KECIL BERCABANG
          ldi             r16,0                   ;JIKA R17=R16 BERCABANG
          rjmp     penampilan
ke_2:
          LDI             R17,41
          CP              R16,R17                    ;BRCC kanan lebih kecil
samadengan bercabang
          BRCC     ke_3                       ;R17 LEBIH BESAR TIDAK
BERCABANG/LEBIH KECIL BERCABANG
          ldi             r16,1                   ;JIKA R17=R16 BERCABANG
          rjmp     penampilan
ke_3:
          LDI             R17,45
          CP              R16,R17                    ;BRCC kanan lebih kecil
samadengan bercabang
          BRCC     ke_4                       ;R17 LEBIH BESAR TIDAK
BERCABANG/LEBIH KECIL BERCABANG
          ldi             r16,2                   ;JIKA R17=R16 BERCABANG
          rjmp     penampilan
ke_4:
          LDI             R17,46
          CP              R16,R17                    ;BRCC kanan lebih kecil
samadengan bercabang
          BRCC     ke_5                       ;R17 LEBIH BESAR TIDAK
BERCABANG/LEBIH KECIL BERCABANG
          ldi             r16,3                   ;JIKA R17=R16 BERCABANG
          rjmp     penampilan
ke_5:
          LDI             R17,47
          CP              R16,R17                    ;BRCC kanan lebih kecil
samadengan bercabang
          BRCC     ke_6                       ;R17 LEBIH BESAR TIDAK
BERCABANG/LEBIH KECIL BERCABANG
          ldi             r16,4                   ;JIKA R17=R16 BERCABANG
          rjmp     penampilan
ke_6:
          LDI             R17,48
          CP              R16,R17                    ;BRCC kanan lebih kecil
samadengan bercabang
          BRCC     ke_7                       ;R17 LEBIH BESAR TIDAK
BERCABANG/LEBIH KECIL BERCABANG
          ldi             r16,5                   ;JIKA R17=R16 BERCABANG
          rjmp     penampilan

ke_7:
          LDI             R17,49
          CP              R16,R17                    ;BRCC kanan lebih kecil
samadengan bercabang
          BRCC     ke_8                       ;R17 LEBIH BESAR TIDAK
BERCABANG/LEBIH KECIL BERCABANG
          ldi             r16,6                   ;JIKA R17=R16 BERCABANG
          rjmp     penampilan
ke_8:
          LDI             R17,54
          CP              R16,R17                    ;BRCC kanan lebih kecil
samadengan bercabang
          BRCC     ke_9                       ;R17 LEBIH BESAR TIDAK
BERCABANG/LEBIH KECIL BERCABANG
          ldi             r16,7                   ;JIKA R17=R16 BERCABANG
          rjmp     penampilan
ke_9:
          LDI             R17,56
          CP              R16,R17                    ;BRCC kanan lebih kecil
samadengan bercabang
          BRCC     ke_10                      ;R17 LEBIH BESAR TIDAK
```

```
BERCABANG/LEBIH KECIL BERCABANG
            ldi             r16,8                   ;JIKA R17=R16 BERCABANG
            rjmp    penampilan
ke_10:
            LDI             R17,58
            CP              R16,R17                     ;BRCC kanan lebih kecil
samadengan bercabang
            BRCC    ke_11                       ;R17 LEBIH BESAR TIDAK
BERCABANG/LEBIH KECIL BERCABANG
            ldi             r16,9                   ;JIKA R17=R16 BERCABANG
            rjmp    penampilan
ke_11:
            LDI             R17,60
            CP              R16,R17                     ;BRCC kanan lebih kecil
samadengan bercabang
            BRCC    ke_12                       ;R17 LEBIH BESAR TIDAK
BERCABANG/LEBIH KECIL BERCABANG
            ldi             r16,10                  ;JIKA R17=R16 BERCABANG
            rjmp    penampilan

ke_12:
            LDI             R17,66
            CP              R16,R17                     ;BRCC kanan lebih kecil
samadengan bercabang
            BRCC    ke_13                       ;R17 LEBIH BESAR TIDAK
BERCABANG/LEBIH KECIL BERCABANG
            ldi             r16,13                  ;JIKA R17=R16 BERCABANG
            rjmp    penampilan

ke_13:
            LDI             R17,70
            CP              R16,R17                     ;BRCC kanan lebih kecil
samadengan bercabang
            BRCC    ke_14                       ;R17 LEBIH BESAR TIDAK
BERCABANG/LEBIH KECIL BERCABANG
            ldi             r16,12                  ;JIKA R17=R16 BERCABANG
            rjmp    penampilan
ke_14:
            LDI             R17,90
            CP              R16,R17                     ;BRCC kanan lebih kecil
samadengan bercabang
            BRCC    ke_15                       ;R17 LEBIH BESAR TIDAK
BERCABANG/LEBIH KECIL BERCABANG
            ldi             r16,13                  ;JIKA R17=R16 BERCABANG
            rjmp    penampilan
ke_15:
            LDI             R17,94
            CP              R16,R17                     ;BRCC kanan lebih kecil
samadengan bercabang
            BRCC    ke_16                       ;R17 LEBIH BESAR TIDAK
BERCABANG/LEBIH KECIL BERCABANG
            ldi             r16,10                  ;JIKA R17=R16 BERCABANG
            rjmp    penampilan
ke_16:  ldi             r16,15
            rjmp    penampilan


Penampilan:
            mov             r26,r16
            rcall   conversi
            rcall   tampilan_ph
;
            ldi             R17,8
            CP              R26,R17                 ;BRCC kanan lebih kecil
samadengan bercabang
            BRCC    Kran_asam_nyala   ;R17 LEBIH BESAR TIDAK BERCABANG/LEBIH
KECIL BERCABANG
            ldi             R17,6
```

```
                CP              R17,R26                 ;BRCC kanan lebih kecil
samadengan bercabang
                BRCC    Kran_basa_nyala   ;R17 LEBIH BESAR TIDAK BERCABANG/LEBIH
KECIL BERCABANG
                cbi             portD,R_kran_asam
                cbi             portD,R_kran_basa

Kran_asam_nyala:
                sbi             portD,R_kran_asam
                rcall   ldelay
                rcall   ldelay
                rcall   ldelay
                rcall   ldelay
                cbi             portD,R_kran_asam
                rjmp    kran_penampung_buka

Kran_basa_nyala:
                sbi             portD,R_kran_basa
                rcall   ldelay
                rcall   ldelay
                rcall   ldelay
                rcall   ldelay
                cbi             portD,R_kran_basa
                rjmp    kran_penampung_buka

kran_penampung_buka:

                sbi             PortC,R_kran_keluaran
ke_a:   sbic    PIND,INDI_V_PENAMPUNGAN                 ;melihat isi penampungan
                rjmp    ke_a
                cbi             PortC,R_kran_keluaran

ke_ab:  sbic    PIND,Tombol                                             ;kembali
                rjmp    ke_ab
                rjmp    balik

set1:
.db             "RONNY ANDRIYANTO"
set2:
.db             " NIM.99.17.102  "
set3:
.db             "Penjernih Air   "
set4:
.db             "Dgn Mengontrol  "
set5:
.db             "Nilai PH berba- "
set6:
.db             "sis Atmega 8515L"


set7:
.db             "Indikator PH    "
KOSONG:
.db             "                "
BERSIH:
.db             "      CLEAR     "

KOTOR:
.db             "      DITRY     "

C_Basa:
.db     "  Cairan Basa    "

C_asam:
.db     "  Cairan Asam    "

abis:
.db             "     Kosong     "
```

```
Angka:
.db     "012345678900000-"


.exit
```

Features

- High-performance, Low-power AVR® 8-bit Microcontroller
- RISC Architecture
  - 130 Powerful Instructions – Most Single Clock Cycle Execution
  - 32 x 8 General Purpose Working Registers
  - Fully Static Operation
  - Up to 16 MIPS Throughput at 16 MHz
  - On-chip 2-cycle Multiplier
- Nonvolatile Program and Data Memories
  - 8K Bytes of In-System Self-programmable Flash
    Endurance: 10,000 Write/Erase Cycles
  - Optional Boot Code Section with Independent Lock bits
    In-System Programming by On-chip Boot Program
    True Read-While-Write Operation
  - 512 Bytes EEPROM
    Endurance: 100,000 Write/Erase Cycles
  - 512 Bytes Internal SRAM
  - Up to 64K Bytes Optional External Memory Space
  - Programming Lock for Software Security
- Peripheral Features
  - One 8-bit Timer/Counter with Separate Prescaler and Compare Mode
  - One 16-bit Timer/Counter with Separate Prescaler, Compare Mode, and Capture Mode
  - Three PWM Channels
  - Programmable Serial USART
  - Master/Slave SPI Serial Interface
  - Programmable Watchdog Timer with Separate On-chip Oscillator
  - On-chip Analog Comparator
- Special Microcontroller Features
  - Power-on Reset and Programmable Brown-out Detection
  - Internal Calibrated RC Oscillator
  - External and Internal Interrupt Sources
  - Three Sleep Modes: Idle, Power-down and Standby
- I/O and Packages
  - 35 Programmable I/O Lines
  - 40-pin PDIP, 44-lead TQFP, 44-lead PLCC, and 44-pad MLF
- Operating Voltages
  - 2.7 - 5.5V for ATmega8515L
  - 4.5 - 5.5V for ATmega8515
- Speed Grades
  - 0 - 8 MHz for ATmega8515L
  - 0 - 16 MHz for ATmega8515

8-bit AVR® Microcontroller with 8K Bytes In-System Programmable Flash

ATmega8515
ATmega8515L

Summary

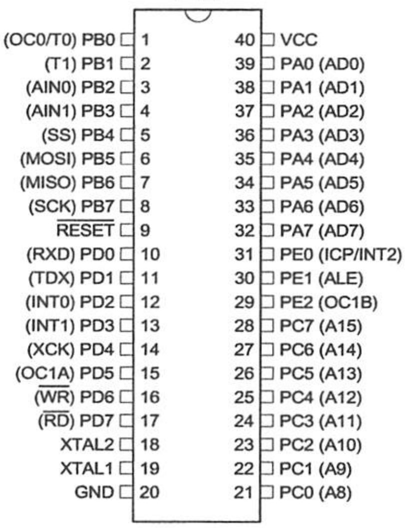
Rev. 2512FS–AVR–12/03

Note: This is a summary document. A complete document is available on our Web site at www.atmel.com.

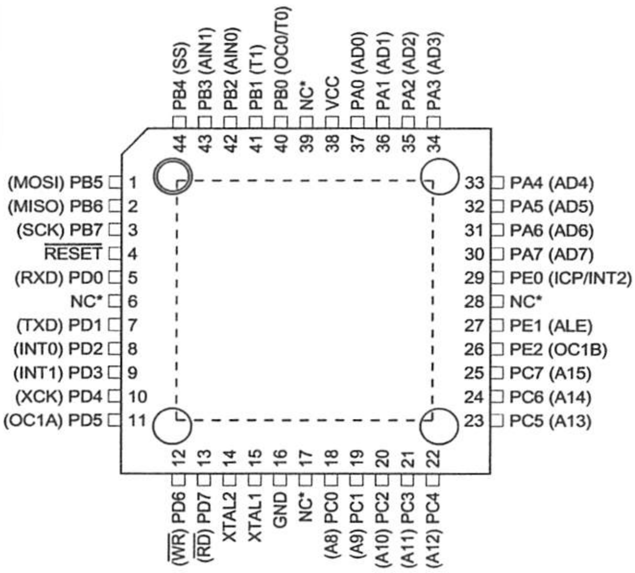
Pin Configurations

Figure 1. Pinout ATmega8515

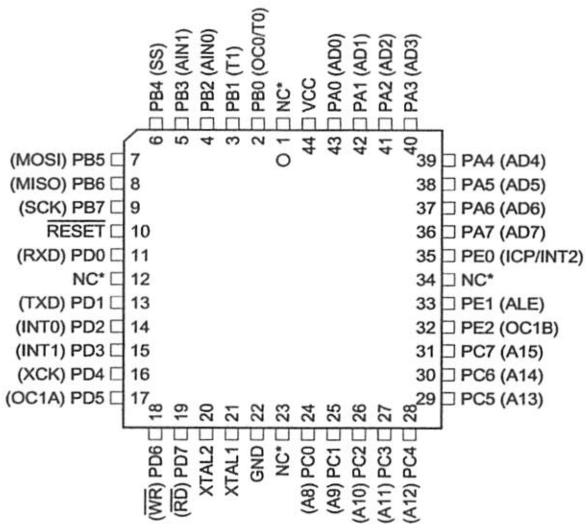
PDIP



TQFP/MLF



PLCC



NOTES:

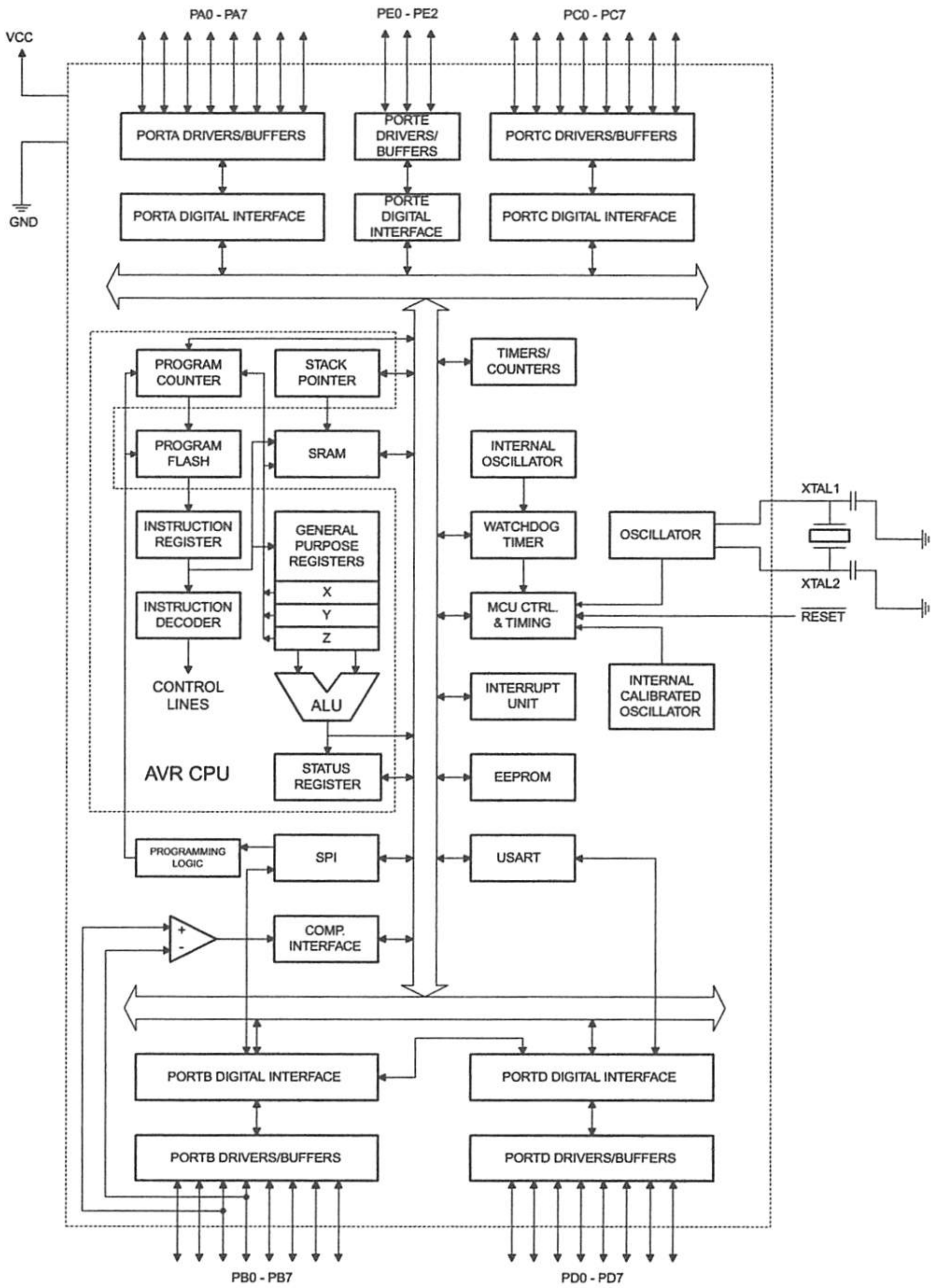
1. MLF bottom pad should be soldered to ground.
2. * NC = Do not connect (May be used in future devices)

Overview

The ATmega8515 is a low-power CMOS 8-bit microcontroller based on the AVR enhanced RISC architecture. By executing powerful instructions in a single clock cycle, the ATmega8515 achieves throughputs approaching 1 MIPS per MHz allowing the system designer to optimize power consumption versus processing speed.

Block Diagram

Figure 2. Block Diagram



The AVR core combines a rich instruction set with 32 general purpose working registers. All the 32 registers are directly connected to the Arithmetic Logic Unit (ALU), allowing two independent registers to be accessed in one single instruction executed in one clock cycle. The resulting architecture is more code efficient while achieving throughputs up to ten times faster than conventional CISC microcontrollers.

The ATmega8515 provides the following features: 8K bytes of In-System Programmable Flash with Read-While-Write capabilities, 512 bytes EEPROM, 512 bytes SRAM, an External memory interface, 35 general purpose I/O lines, 32 general purpose working registers, two flexible Timer/Counters with compare modes, Internal and External interrupts, a Serial Programmable USART, a programmable Watchdog Timer with internal Oscillator, a SPI serial port, and three software selectable power saving modes. The Idle mode stops the CPU while allowing the SRAM, Timer/Counters, SPI port, and Interrupt system to continue functioning. The Power-down mode saves the Register contents but freezes the Oscillator, disabling all other chip functions until the next interrupt or hardware reset. In Standby mode, the crystal/resonator Oscillator is running while the rest of the device is sleeping. This allows very fast start-up combined with low-power consumption.

The device is manufactured using Atmel's high density nonvolatile memory technology. The On-chip ISP Flash allows the Program memory to be reprogrammed In-System through an SPI serial interface, by a conventional nonvolatile memory programmer, or by an On-chip Boot program running on the AVR core. The boot program can use any interface to download the application program in the Application Flash memory. Software in the Boot Flash section will continue to run while the Application Flash section is updated, providing true Read-While-Write operation. By combining an 8-bit RISC CPU with In-System Self-programmable Flash on a monolithic chip, the Atmel ATmega8515 is a powerful microcontroller that provides a highly flexible and cost effective solution to many embedded control applications.

The ATmega8515 is supported with a full suite of program and system development tools including: C Compilers, Macro assemblers, Program debugger/simulators, In-circuit Emulators, and Evaluation kits.

Disclaimer

Typical values contained in this datasheet are based on simulations and characterization of other AVR microcontrollers manufactured on the same process technology. Min and Max values will be available after the device is characterized.

AT90S4414/8515 and ATmega8515 Compatibility

The ATmega8515 provides all the features of the AT90S4414/8515. In addition, several new features are added. The ATmega8515 is backward compatible with AT90S4414/8515 in most cases. However, some incompatibilities between the two microcontrollers exist. To solve this problem, an AT90S4414/8515 compatibility mode can be selected by programming the S8515C Fuse. ATmega8515 is 100% pin compatible with AT90S4414/8515, and can replace the AT90S4414/8515 on current printed circuit boards. However, the location of Fuse bits and the electrical characteristics differs between the two devices.

AT90S4414/8515 Compatibility Mode

Programming the S8515C Fuse will change the following functionality:

- The timed sequence for changing the Watchdog Time-out period is disabled. See "Timed Sequences for Changing the Configuration of the Watchdog Timer" on page 52 for details.
- The double buffering of the USART Receive Registers is disabled. See "AVR USART vs. AVR UART – Compatibility" on page 135 for details.
- PORTE(2:1) will be set as output, and PORTE0 will be set as input.

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- The double buffering of the USART Receive Registers is disabled. See "AVR USART vs. AVR UART – Compatibility" on page 135 for details.
- PORTE(2:1) will be set as output, and PORTE0 will be set as input.

Pin Descriptions

VCC Digital supply voltage.

GND Ground.

Port A (PA7..PA0) Port A is an 8-bit bi-directional I/O port with internal pull-up resistors (selected for each bit). The Port A output buffers have symmetrical drive characteristics with both high sink and source capability. When pins PA0 to PA7 are used as inputs and are externally pulled low, they will source current if the internal pull-up resistors are activated. The Port A pins are tri-stated when a reset condition becomes active, even if the clock is not running.

Port A also serves the functions of various special features of the ATmega8515 as listed on page 66.

Port B (PB7..PB0) Port B is an 8-bit bi-directional I/O port with internal pull-up resistors (selected for each bit). The Port B output buffers have symmetrical drive characteristics with both high sink and source capability. As inputs, Port B pins that are externally pulled low will source current if the pull-up resistors are activated. The Port B pins are tri-stated when a reset condition becomes active, even if the clock is not running.

Port B also serves the functions of various special features of the ATmega8515 as listed on page 66.

Port C (PC7..PC0) Port C is an 8-bit bi-directional I/O port with internal pull-up resistors (selected for each bit). The Port C output buffers have symmetrical drive characteristics with both high sink and source capability. As inputs, Port C pins that are externally pulled low will source current if the pull-up resistors are activated. The Port C pins are tri-stated when a reset condition becomes active, even if the clock is not running.

Port D (PD7..PD0) Port D is an 8-bit bi-directional I/O port with internal pull-up resistors (selected for each bit). The Port D output buffers have symmetrical drive characteristics with both high sink and source capability. As inputs, Port D pins that are externally pulled low will source current if the pull-up resistors are activated. The Port D pins are tri-stated when a reset condition becomes active, even if the clock is not running.

Port D also serves the functions of various special features of the ATmega8515 as listed on page 71.

Port E(PE2..PE0) Port E is an 3-bit bi-directional I/O port with internal pull-up resistors (selected for each bit). The Port E output buffers have symmetrical drive characteristics with both high sink and source capability. As inputs, Port E pins that are externally pulled low will source current if the pull-up resistors are activated. The Port E pins are tri-stated when a reset condition becomes active, even if the clock is not running.

Port E also serves the functions of various special features of the ATmega8515 as listed on page 73.

$\overline{\textbf{RESET}}$ Reset input. A low level on this pin for longer than the minimum pulse length will generate a reset, even if the clock is not running. The minimum pulse length is given in Table 18 on page 45. Shorter pulses are not guaranteed to generate a reset.

XTAL1 Input to the inverting Oscillator amplifier and input to the internal clock operating circuit.

XTAL2 Output from the inverting Oscillator amplifier.

Register Summary

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Page
$3F ($5F)	SREG	I	T	H	S	V	N	Z	C	9
$3E ($5E)	SPH	SP15	SP14	SP13	SP12	SP11	SP10	SP9	SP8	11
$3D ($5D)	SPL	SP7	SP6	SP5	SP4	SP3	SP2	SP1	SP0	11
$3C ($5C)	Reserved	-								
$3B ($5B)	GICR	INT1	INT0	INT2	-	-	-	IVSEL	IVCE	56, 77
$3A ($5A)	GIFR	INTF1	INTF0	INTF2	-	-	-	-	-	78
$39 ($59)	TIMSK	TOIE1	OCIE1A	OCIE1B	-	TICIE1	-	TOIE0	OCIE0	92, 123
$38 ($58)	TIFR	TOV1	OCF1A	OCF1B	-	ICF1	-	TOV0	OCF0	92, 124
$37 ($57)	SPMCR	SPMIE	RWWSB	-	RWWSRE	BLBSET	PGWRT	PGERS	SPMEN	168
$36 ($56)	EMCUCR	SM0	SRL2	SRL1	SRL0	SRW01	SRW00	SRW11	ISC2	28,41,77
$35 ($55)	MCUCR	SRE	SRW10	SE	SM1	ISC11	ISC10	ISC01	ISC00	28,40,76
$34 ($54)	MCUCSR	-	-	SM2	-	WDRF	BORF	EXTRF	PORF	40,48
$33 ($53)	TCCR0	FOC0	WGM00	COM01	COM00	WGM01	CS02	CS01	CS00	90
$32 ($52)	TCNT0	Timer/Counter0 (8 Bits)								92
$31 ($51)	OCR0	Timer/Counter0 Output Compare Register								92
$30 ($50)	SFIOR	-	XMBK	XMM2	XMM1	XMM0	PUD	-	PSR10	30,65,95
$2F ($4F)	TCCR1A	COM1A1	COM1A0	COM1B1	COM1B0	FOC1A	FOC1B	WGM11	WGM10	118
$2E ($4E)	TCCR1B	ICNC1	ICES1	-	WGM13	WGM12	CS12	CS11	CS10	121
$2D ($4D)	TCNT1H	Timer/Counter1 - Counter Register High Byte								122
$2C ($4C)	TCNT1L	Timer/Counter1 - Counter Register Low Byte								122
$2B ($4B)	OCR1AH	Timer/Counter1 - Output Compare Register A High Byte								122
$2A ($4A)	OCR1AL	Timer/Counter1 - Output Compare Register A Low Byte								122
$29 ($49)	OCR1BH	Timer/Counter1 - Output Compare Register B High Byte								122
$28 ($48)	OCR1BL	Timer/Counter1 - Output Compare Register B Low Byte								122
$27 ($47)	Reserved	-								-
$26 ($46)	Reserved	-								-
$25 ($45)	ICR1H	Timer/Counter1 - Input Capture Register High Byte								123
$24 ($44)	ICR1L	Timer/Counter1 - Input Capture Register Low Byte								123
$23 ($43)	Reserved	-								-
$22 ($42)	Reserved	-								-
$21 ($41)	WDTCR	-	-	-	WDCE	WDE	WDP2	WDP1	WDP0	50
$20(1) ($40)(1)	UBRRH	URSEL	-	-	-	UBRR[11:8]				157
	UCSRC	URSEL	UMSEL	UPM1	UPM0	USBS	UCSZ1	UCSZ0	UCPOL	155
$1F ($3F)	EEARH	-	-	-	-	-	-	-	EEAR8	18
$1E ($3E)	EEARL	EEPROM Address Register Low Byte								18
$1D ($3D)	EEDR	EEPROM Data Register								19
$1C ($3C)	EECR	-	-	-	-	EERIE	EEMWE	EEWE	EERE	19
$1B ($3B)	PORTA	PORTA7	PORTA6	PORTA5	PORTA4	PORTA3	PORTA2	PORTA1	PORTA0	74
$1A ($3A)	DDRA	DDA7	DDA6	DDA5	DDA4	DDA3	DDA2	DDA1	DDA0	74
$19 ($39)	PINA	PINA7	PINA6	PINA5	PINA4	PINA3	PINA2	PINA1	PINA0	74
$18 ($38)	PORTB	PORTB7	PORTB6	PORTB5	PORTB4	PORTB3	PORTB2	PORTB1	PORTB0	74
$17 ($37)	DDRB	DDB7	DDB6	DDB5	DDB4	DDB3	DDB2	DDB1	DDB0	74
$16 ($36)	PINB	PINB7	PINB6	PINB5	PINB4	PINB3	PINB2	PINB1	PINB0	74
$15 ($35)	PORTC	PORTC7	PORTC6	PORTC5	PORTC4	PORTC3	PORTC2	PORTC1	PORTC0	74
$14 ($34)	DDRC	DDC7	DDC6	DDC5	DDC4	DDC3	DDC2	DDC1	DDC0	74
$13 ($33)	PINC	PINC7	PINC6	PINC5	PINC4	PINC3	PINC2	PINC1	PINC0	75
$12 ($32)	PORTD	PORTD7	PORTD6	PORTD5	PORTD4	PORTD3	PORTD2	PORTD1	PORTD0	75
$11 ($31)	DDRD	DDD7	DDD6	DDD5	DDD4	DDD3	DDD2	DDD1	DDD0	75
$10 ($30)	PIND	PIND7	PIND6	PIND5	PIND4	PIND3	PIND2	PIND1	PIND0	75
$0F ($2F)	SPDR	SPI Data Register								131
$0E ($2E)	SPSR	SPIF	WCOL	-	-	-	-	-	SPI2X	131
$0D ($2D)	SPCR	SPIE	SPE	DORD	MSTR	CPOL	CPHA	SPR1	SPR0	129
$0C ($2C)	UDR	USART I/O Data Register								153
$0B ($2B)	UCSRA	RXC	TXC	UDRE	FE	DOR	PE	U2X	MPCM	153
$0A ($2A)	UCSRB	RXCIE	TXCIE	UDRIE	RXEN	TXEN	UCSZ2	RXB8	TXB8	154
$09 ($29)	UBRRL	USART Baud Rate Register Low Byte								157
$08 ($28)	ACSR	ACD	ACBG	ACO	ACI	ACIE	ACIC	ACIS1	ACIS0	162
$07 ($27)	PORTE	-	-	-	-	-	PORTE2	PORTE1	PORTE0	75
$06 ($26)	DDRE	-	-	-	-	-	DDE2	DDE1	DDE0	75
$05 ($25)	PINE	-	-	-	-	-	PINE2	PINE1	PINE0	75
$04 ($24)	OSCCAL	Oscillator Calibration Register								38

Notes: 1. Refer to the USART description for details on how to access UBRRH and UCSRC.

2. For compatibility with future devices, reserved bits should be written to zero if accessed. Reserved I/O memory addresses should never be written.

3. Some of the Status Flags are cleared by writing a logical one to them. Note that the CBI and SBI instructions will operate on all bits in the I/O Register, writing a one back into any flag read as set, thus clearing the flag. The CBI and SBI instructions work with registers $00 to $1F only.

Instruction Set Summary

Mnemonics	Operands	Description	Operation	Flags	#Clocks
ARITHMETIC AND LOGIC INSTRUCTIONS					
ADD	Rd, Rr	Add two Registers	Rd ← Rd + Rr	Z,C,N,V,H	1
ADC	Rd, Rr	Add with Carry two Registers	Rd ← Rd + Rr + C	Z,C,N,V,H	1
ADIW	Rdl,K	Add Immediate to Word	Rdh:Rdl ← Rdh:Rdl + K	Z,C,N,V,S	2
SUB	Rd, Rr	Subtract two Registers	Rd ← Rd - Rr	Z,C,N,V,H	1
SUBI	Rd, K	Subtract Constant from Register	Rd ← Rd - K	Z,C,N,V,H	1
SBC	Rd, Rr	Subtract with Carry two Registers	Rd ← Rd - Rr - C	Z,C,N,V,H	1
SBCI	Rd, K	Subtract with Carry Constant from Reg.	Rd ← Rd - K - C	Z,C,N,V,H	1
SBIW	Rdl,K	Subtract Immediate from Word	Rdh:Rdl ← Rdh:Rdl - K	Z,C,N,V,S	2
AND	Rd, Rr	Logical AND Registers	Rd ← Rd • Rr	Z,N,V	1
ANDI	Rd, K	Logical AND Register and Constant	Rd ← Rd • K	Z,N,V	1
OR	Rd, Rr	Logical OR Registers	Rd ← Rd v Rr	Z,N,V	1
ORI	Rd, K	Logical OR Register and Constant	Rd ← Rd v K	Z,N,V	1
EOR	Rd, Rr	Exclusive OR Registers	Rd ← Rd ⊕ Rr	Z,N,V	1
COM	Rd	One's Complement	Rd ← $FF – Rd	Z,C,N,V	1
NEG	Rd	Two's Complement	Rd ← $00 – Rd	Z,C,N,V,H	1
SBR	Rd,K	Set Bit(s) in Register	Rd ← Rd v K	Z,N,V	1
CBR	Rd,K	Clear Bit(s) in Register	Rd ← Rd • ($FF - K)	Z,N,V	1
INC	Rd	Increment	Rd ← Rd + 1	Z,N,V	1
DEC	Rd	Decrement	Rd ← Rd – 1	Z,N,V	1
TST	Rd	Test for Zero or Minus	Rd ← Rd • Rd	Z,N,V	1
CLR	Rd	Clear Register	Rd ← Rd ⊕ Rd	Z,N,V	1
SER	Rd	Set Register	Rd ← $FF	None	1
MUL	Rd, Rr	Multiply Unsigned	R1:R0 ← Rd x Rr	Z,C	2
MULS	Rd, Rr	Multiply Signed	R1:R0 ← Rd x Rr	Z,C	2
MULSU	Rd, Rr	Multiply Signed with Unsigned	R1:R0 ← Rd x Rr	Z,C	2
FMUL	Rd, Rr	Fractional Multiply Unsigned	R1:R0 ← (Rd x Rr) << 1	Z,C	2
FMULS	Rd, Rr	Fractional Multiply Signed	R1:R0 ← (Rd x Rr) << 1	Z,C	2
FMULSU	Rd, Rr	Fractional Multiply Signed with Unsigned	R1:R0 ← (Rd x Rr) << 1	Z,C	2
BRANCH INSTRUCTIONS					
RJMP	k	Relative Jump	PC ← PC + k + 1	None	2
IJMP		Indirect Jump to (Z)	PC ← Z	None	2
RCALL	k	Relative Subroutine Call	PC ← PC + k + 1	None	3
ICALL		Indirect Call to (Z)	PC ← Z	None	3
RET		Subroutine Return	PC ← STACK	None	4
RETI		Interrupt Return	PC ← STACK	I	4
CPSE	Rd,Rr	Compare, Skip if Equal	if (Rd = Rr) PC ← PC + 2 or 3	None	1/2/3
CP	Rd,Rr	Compare	Rd – Rr	Z, N,V,C,H	1
CPC	Rd,Rr	Compare with Carry	Rd – Rr – C	Z, N,V,C,H	1
CPI	Rd,K	Compare Register with Immediate	Rd – K	Z, N,V,C,H	1
SBRC	Rr, b	Skip if Bit in Register Cleared	if (Rr(b)=0) PC ← PC + 2 or 3	None	1/2/3
SBRS	Rr, b	Skip if Bit in Register is Set	if (Rr(b)=1) PC ← PC + 2 or 3	None	1/2/3
SBIC	P, b	Skip if Bit in I/O Register Cleared	if (P(b)=0) PC ← PC + 2 or 3	None	1/2/3
SBIS	P, b	Skip if Bit in I/O Register is Set	if (P(b)=1) PC ← PC + 2 or 3	None	1/2/3
BRBS	s, k	Branch if Status Flag Set	if (SREG(s) = 1) then PC←PC+k + 1	None	1/2
BRBC	s, k	Branch if Status Flag Cleared	if (SREG(s) = 0) then PC←PC+k + 1	None	1/2
BREQ	k	Branch if Equal	if (Z = 1) then PC ← PC + k + 1	None	1/2
BRNE	k	Branch if Not Equal	if (Z = 0) then PC ← PC + k + 1	None	1/2
BRCS	k	Branch if Carry Set	if (C = 1) then PC ← PC + k + 1	None	1/2
BRCC	k	Branch if Carry Cleared	if (C = 0) then PC ← PC + k + 1	None	1/2
BRSH	k	Branch if Same or Higher	if (C = 0) then PC ← PC + k + 1	None	1/2
BRLO	k	Branch if Lower	if (C = 1) then PC ← PC + k + 1	None	1/2
BRMI	k	Branch if Minus	if (N = 1) then PC ← PC + k + 1	None	1/2
BRPL	k	Branch if Plus	if (N = 0) then PC ← PC + k + 1	None	1/2
BRGE	k	Branch if Greater or Equal, Signed	if (N ⊕ V= 0) then PC ← PC + k + 1	None	1/2
BRLT	k	Branch if Less Than Zero, Signed	if (N ⊕ V= 1) then PC ← PC + k + 1	None	1/2
BRHS	k	Branch if Half Carry Flag Set	if (H = 1) then PC ← PC + k + 1	None	1/2
BRHC	k	Branch if Half Carry Flag Cleared	if (H = 0) then PC ← PC + k + 1	None	1/2
BRTS	k	Branch if T Flag Set	if (T = 1) then PC ← PC + k + 1	None	1/2
BRTC	k	Branch if T Flag Cleared	if (T = 0) then PC ← PC + k + 1	None	1/2
BRVS	k	Branch if Overflow Flag is Set	if (V = 1) then PC ← PC + k + 1	None	1/2
BRVC	k	Branch if Overflow Flag is Cleared	if (V = 0) then PC ← PC + k + 1	None	1/2
BRIE	k	Branch if Interrupt Enabled	if (I = 1) then PC ← PC + k + 1	None	1/2
BRID	k	Branch if Interrupt Disabled	if (I = 0) then PC ← PC + k + 1	None	1/2

Mnemonics	Operands	Description	Operation	Flags	#Clocks
DATA TRANSFER INSTRUCTIONS					
MOV	Rd, Rr	Move Between Registers	Rd ← Rr	None	1
MOVW	Rd, Rr	Copy Register Word	Rd+1:Rd ← Rr+1:Rr	None	1
LDI	Rd, K	Load Immediate	Rd ← K	None	1
LD	Rd, X	Load Indirect	Rd ← (X)	None	2
LD	Rd, X+	Load Indirect and Post-Inc.	Rd ← (X), X ← X + 1	None	2
LD	Rd, - X	Load Indirect and Pre-Dec.	X ← X - 1, Rd ← (X)	None	2
LD	Rd, Y	Load Indirect	Rd ← (Y)	None	2
LD	Rd, Y+	Load Indirect and Post-Inc.	Rd ← (Y), Y ← Y + 1	None	2
LD	Rd, - Y	Load Indirect and Pre-Dec.	Y ← Y - 1, Rd ← (Y)	None	2
LDD	Rd,Y+q	Load Indirect with Displacement	Rd ← (Y + q)	None	2
LD	Rd, Z	Load Indirect	Rd ← (Z)	None	2
LD	Rd, Z+	Load Indirect and Post-Inc.	Rd ← (Z), Z ← Z+1	None	2
LD	Rd, -Z	Load Indirect and Pre-Dec.	Z ← Z - 1, Rd ← (Z)	None	2
LDD	Rd, Z+q	Load Indirect with Displacement	Rd ← (Z + q)	None	2
LDS	Rd, k	Load Direct from SRAM	Rd ← (k)	None	2
ST	X, Rr	Store Indirect	(X) ← Rr	None	2
ST	X+, Rr	Store Indirect and Post-Inc.	(X) ← Rr, X ← X + 1	None	2
ST	- X, Rr	Store Indirect and Pre-Dec.	X ← X - 1, (X) ← Rr	None	2
ST	Y, Rr	Store Indirect	(Y) ← Rr	None	2
ST	Y+, Rr	Store Indirect and Post-Inc.	(Y) ← Rr, Y ← Y + 1	None	2
ST	- Y, Rr	Store Indirect and Pre-Dec.	Y ← Y - 1, (Y) ← Rr	None	2
STD	Y+q,Rr	Store Indirect with Displacement	(Y + q) ← Rr	None	2
ST	Z, Rr	Store Indirect	(Z) ← Rr	None	2
ST	Z+, Rr	Store Indirect and Post-Inc.	(Z) ← Rr, Z ← Z + 1	None	2
ST	-Z, Rr	Store Indirect and Pre-Dec.	Z ← Z - 1, (Z) ← Rr	None	2
STD	Z+q,Rr	Store Indirect with Displacement	(Z + q) ← Rr	None	2
STS	k, Rr	Store Direct to SRAM	(k) ← Rr	None	2
LPM		Load Program memory	R0 ← (Z)	None	3
LPM	Rd, Z	Load Program memory	Rd ← (Z)	None	3
LPM	Rd, Z+	Load Program memory and Post-Inc	Rd ← (Z), Z ← Z+1	None	3
SPM		Store Program memory	(Z) ← R1:R0	None	-
IN	Rd, P	In Port	Rd ← P	None	1
OUT	P, Rr	Out Port	P ← Rr	None	1
PUSH	Rr	Push Register on Stack	STACK ← Rr	None	2
POP	Rd	Pop Register from Stack	Rd ← STACK	None	2
BIT AND BIT-TEST INSTRUCTIONS					
SBI	P,b	Set Bit in I/O Register	I/O(P,b) ← 1	None	2
CBI	P,b	Clear Bit in I/O Register	I/O(P,b) ← 0	None	2
LSL	Rd	Logical Shift Left	Rd(n+1) ← Rd(n), Rd(0) ← 0	Z,C,N,V	1
LSR	Rd	Logical Shift Right	Rd(n) ← Rd(n+1), Rd(7) ← 0	Z,C,N,V	1
ROL	Rd	Rotate Left Through Carry	Rd(0)←C,Rd(n+1)← Rd(n),C←Rd(7)	Z,C,N,V	1
ROR	Rd	Rotate Right Through Carry	Rd(7)←C,Rd(n)← Rd(n+1),C←Rd(0)	Z,C,N,V	1
ASR	Rd	Arithmetic Shift Right	Rd(n) ← Rd(n+1), n=0..6	Z,C,N,V	1
SWAP	Rd	Swap Nibbles	Rd(3..0)←Rd(7..4),Rd(7..4)←Rd(3..0)	None	1
BSET	s	Flag Set	SREG(s) ← 1	SREG(s)	1
BCLR	s	Flag Clear	SREG(s) ← 0	SREG(s)	1
BST	Rr, b	Bit Store from Register to T	T ← Rr(b)	T	1
BLD	Rd, b	Bit load from T to Register	Rd(b) ← T	None	1
SEC		Set Carry	C ← 1	C	1
CLC		Clear Carry	C ← 0	C	1
SEN		Set Negative Flag	N ← 1	N	1
CLN		Clear Negative Flag	N ← 0	N	1
SEZ		Set Zero Flag	Z ← 1	Z	1
CLZ		Clear Zero Flag	Z ← 0	Z	1
SEI		Global Interrupt Enable	I ← 1	I	1
CLI		Global Interrupt Disable	I ← 0	I	1
SES		Set Signed Test Flag	S ← 1	S	1
CLS		Clear Signed Test Flag	S ← 0	S	1
SEV		Set Twos Complement Overflow.	V ← 1	V	1
CLV		Clear Twos Complement Overflow	V ← 0	V	1
SET		Set T in SREG	T ← 1	T	1
CLT		Clear T in SREG	T ← 0	T	1
SEH		Set Half Carry Flag in SREG	H ← 1	H	1
CLH		Clear Half Carry Flag in SREG	H ← 0	H	1
MCU CONTROL INSTRUCTIONS					

Mnemonics	Operands	Description	Operation	Flags	#Clocks
NOP		No Operation		None	1
SLEEP		Sleep	(see specific descr. for Sleep function)	None	1
WDR		Watchdog Reset	(see specific descr. for WDR/timer)	None	1

Ordering Information

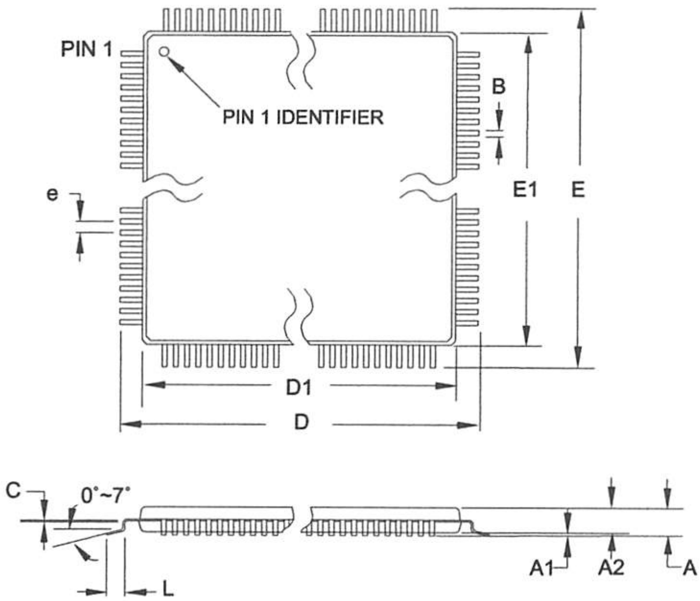
Speed (MHz)	Power Supply	Ordering Code	Package(1)	Operation Range
8	2.7 - 5.5V	ATmega8515L-8AC ATmega8515L-8PC ATmega8515L-8JC ATmega8515L-8MC	44A 40P6 44J 44M1	Commercial (0°C to 70°C)
		ATmega8515L-8AI ATmega8515L-8PI ATmega8515L-8JI ATmega8515L-8MI	44A 40P6 44J 44M1	Industrial (-40°C to 85°C)
16	4.5 - 5.5V	ATmega8515-16AC ATmega8515-16PC ATmega8515-16JC ATmega8515-16MC	44A 40P6 44J 44M1	Commercial (0°C to 70°C)
		ATmega8515-16AI ATmega8515-16PI ATmega8515-16JI ATmega8515-16MI	44A 40P6 44J 44M1	Industrial (-40°C to 85°C)

Note: 1. This device can also be supplied in wafer form. Please contact your local Atmel sales office for detailed ordering information and minimum quantities.

Package Type	
44A	44-lead, Thin (1.0 mm) Plastic Gull Wing Quad Flat Package (TQFP)
40P6	40-lead, 0.600" Wide, Plastic Dual Inline Package (PDIP)
44J	44-lead, Plastic J-Leaded Chip Carrier (PLCC)
44M1	44-pad, 7 x 7 x 1.0 mm body, lead pitch 0.50 mm, Micro Lead Frame Package (MLF)

Packaging Information

44A



COMMON DIMENSIONS
(Unit of Measure = mm)

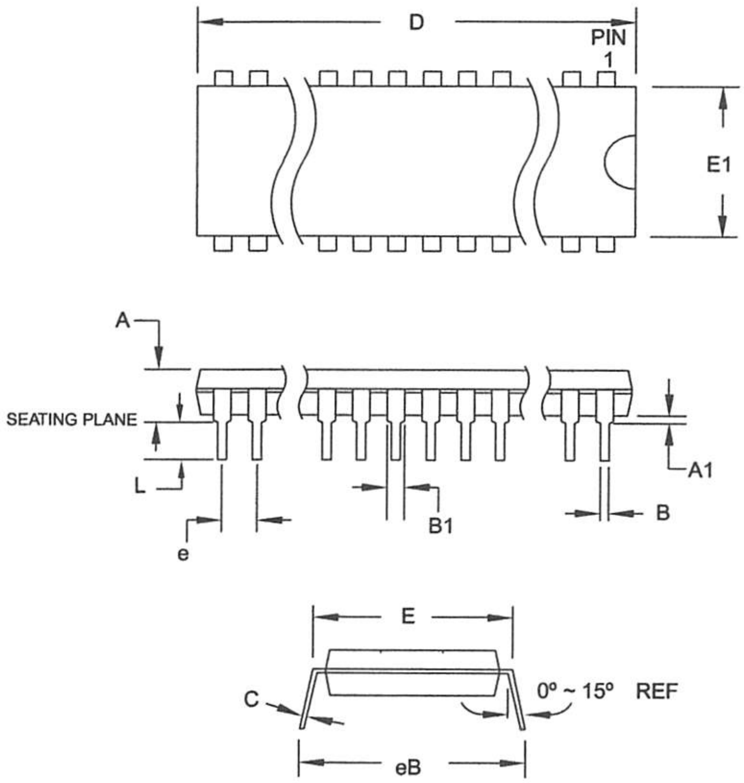
SYMBOL	MIN	NOM	MAX	NOTE
A	–	–	1.20	
A1	0.05	–	0.15	
A2	0.95	1.00	1.05	
D	11.75	12.00	12.25	
D1	9.90	10.00	10.10	Note 2
E	11.75	12.00	12.25	
E1	9.90	10.00	10.10	Note 2
B	0.30	–	0.45	
C	0.09	–	0.20	
L	0.45	–	0.75	
e	0.80 TYP			

Notes:
1. This package conforms to JEDEC reference MS-026, Variation ACB.
2. Dimensions D1 and E1 do not include mold protrusion. Allowable protrusion is 0.25 mm per side. Dimensions D1 and E1 are maximum plastic body size dimensions including mold mismatch.
3. Lead coplanarity is 0.10 mm maximum.

10/5/2001

	TITLE	DRAWING NO.	REV.
ATMEL 2325 Orchard Parkway San Jose, CA 95131	**44A,** 44-lead, 10 x 10 mm Body Size, 1.0 mm Body Thickness, 0.8 mm Lead Pitch, Thin Profile Plastic Quad Flat Package (TQFP)	44A	B

40P6



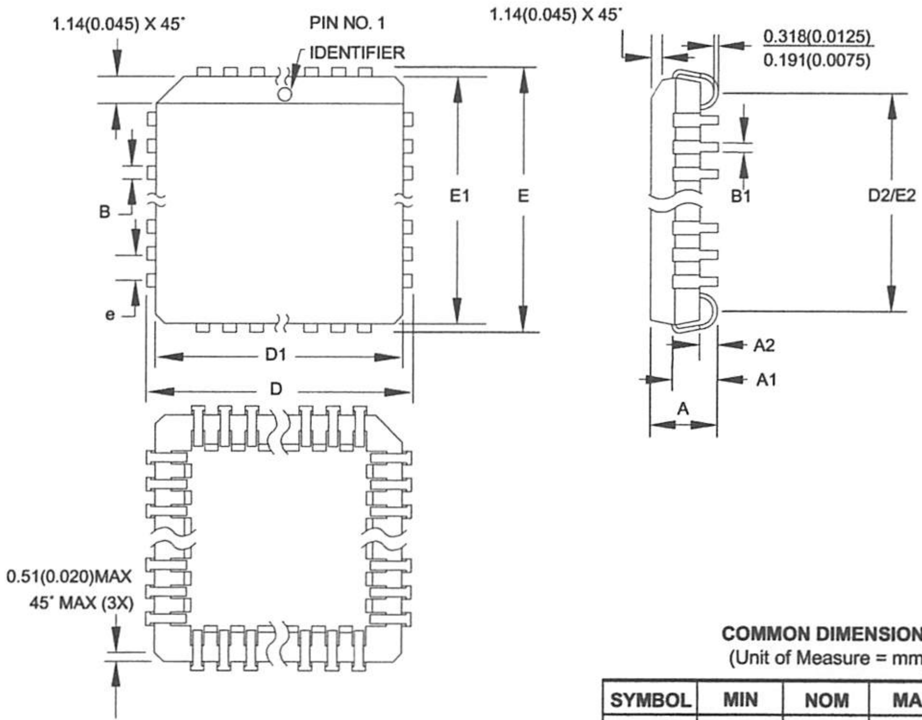
COMMON DIMENSIONS
(Unit of Measure = mm)

SYMBOL	MIN	NOM	MAX	NOTE
A	–	–	4.826	
A1	0.381	–	–	
D	52.070	–	52.578	Note 2
E	15.240	–	15.875	
E1	13.462	–	13.970	Note 2
B	0.356	–	0.559	
B1	1.041	–	1.651	
L	3.048	–	3.556	
C	0.203	–	0.381	
eB	15.494	–	17.526	
e	2.540 TYP			

Notes:
1. This package conforms to JEDEC reference MS-011, Variation AC.
2. Dimensions D and E1 do not include mold Flash or Protrusion. Mold Flash or Protrusion shall not exceed 0.25 mm (0.010").

09/28/01

	TITLE	DRAWING NO.	REV.
ATMEL 2325 Orchard Parkway San Jose, CA 95131	**40P6**, 40-lead (0.600"/15.24 mm Wide) Plastic Dual Inline Package (PDIP)	40P6	B



COMMON DIMENSIONS
(Unit of Measure = mm)

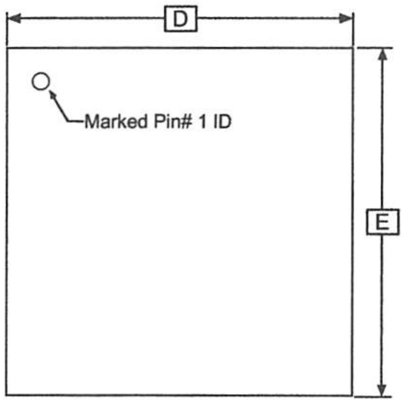
SYMBOL	MIN	NOM	MAX	NOTE
A	4.191	–	4.572	
A1	2.286	–	3.048	
A2	0.508	–	–	
D	17.399	–	17.653	
D1	16.510	–	16.662	Note 2
E	17.399	–	17.653	
E1	16.510	–	16.662	Note 2
D2/E2	14.986	–	16.002	
B	0.660	–	0.813	
B1	0.330	–	0.533	
e	1.270 TYP			

Notes:
1. This package conforms to JEDEC reference MS-018, Variation AC.
2. Dimensions D1 and E1 do not include mold protrusion. Allowable protrusion is .010"(0.254 mm) per side. Dimension D1 and E1 include mold mismatch and are measured at the extreme material condition at the upper or lower parting line.
3. Lead coplanarity is 0.004" (0.102 mm) maximum.

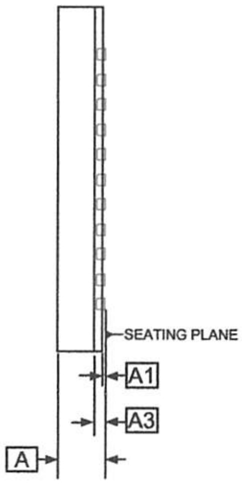
10/04/01

	TITLE	DRAWING NO.	REV.
2325 Orchard Parkway San Jose, CA 95131	**44J**, 44-lead, Plastic J-leaded Chip Carrier (PLCC)	44J	B

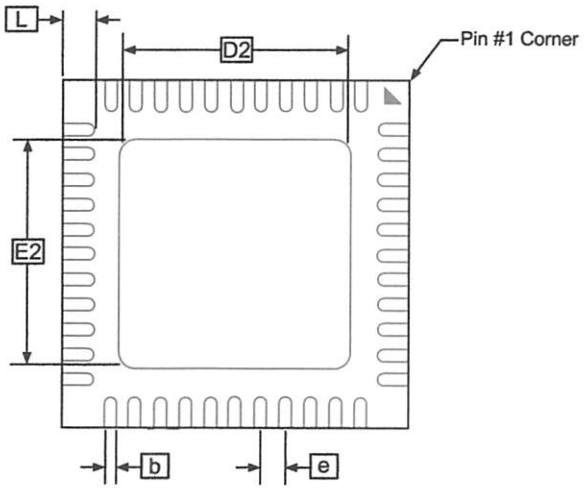
44M1



TOP VIEW



SIDE VIEW



BOTTOM VIEW

COMMON DIMENSIONS
(Unit of Measure = mm)

SYMBOL	MIN	NOM	MAX	NOTE
A	0.80	0.90	1.00	
A1	–	0.02	0.05	
A3		0.25 REF		
b	0.18	0.23	0.30	
D		7.00 BSC		
D2	5.00	5.20	5.40	
E		7.00 BSC		
E2	5.00	5.20	5.40	
e		0.50 BSC		
L	0.35	0.55	0.75	

Notes: 1. JEDEC Standard MO-220, Fig. 1 (SAW Singulation) VKKD-1.

01/15/03

	TITLE	DRAWING NO.	REV.
2325 Orchard Parkway San Jose, CA 95131	**44M1**, 44-pad, 7 x 7 x 1.0 mm Body, Lead Pitch 0.50 mm Micro Lead Frame Package (MLF)	44M1	C

Errata

The revision letter in this section refers to the revision of the ATmega8515 device.

ATmega8515(L) Rev. B

There are no errata for this revision of ATmega8515.

Errata

The revision letter in this section refers to the revision of the ATmega8515 device.

ATmega8515(L) Rev. B

There are no errata for this revision of ATmega8515.

Datasheet Change Log for ATmega8515

Please note that the referring page numbers in this section are referring to this document. The referring revision in this section are referring to the document revision.

Changes from Rev. 2512F-12/03 to Rev. 2512E-09/03

1. Updated "Calibrated Internal RC Oscillator" on page 38.

Changes from Rev. 2512D-02/03 to Rev. 2512E-09/03

1. Removed "Preliminary" from the datasheet.
2. Updated Table 18 on page 45 and "Absolute Maximum Ratings" and "DC Characteristics" in "Electrical Characteristics" on page 195.
3. Updated chapter "ATmega8515 Typical Characteristics" on page 205.

Changes from Rev. 2512C-10/02 to Rev. 2512D-02/03

1. Added "EEPROM Write During Power-down Sleep Mode" on page 22.
2. Improved the description in "Phase Correct PWM Mode" on page 87.
3. Corrected OCn waveforms in Figure 53 on page 110.
4. Added note under "Filling the Temporary Buffer (page loading)" on page 171 about writing to the EEPROM during an SPM page load.
5. Updated Table 93 on page 193.
6. Updated "Packaging Information" on page 12.

Changes from Rev. 2512B-09/02 to Rev. 2512C-10/02

1. Added "Using all Locations of External Memory Smaller than 64 KB" on page 30.
2. Removed all TBD.
3. Added description about calibration values for 2, 4, and 8 MHz.
4. Added variation in frequency of "External Clock" on page 39.
5. Added note about V_{BOT}, Table 18 on page 45.
6. Updated about "Unconnected pins" on page 63.
7. Updated "16-bit Timer/Counter1" on page 96, Table 51 on page 118 and Table 52 on page 119.
8. Updated "Enter Programming Mode" on page 182, "Chip Erase" on page 182, Figure 77 on page 185, and Figure 78 on page 186.
9. Updated "Electrical Characteristics" on page 195, "External Clock Drive" on page 197, Table 96 on page 197 and Table 97 on page 198, "SPI Timing Characteristics" on page 198 and Table 98 on page 200.
10. Added "Errata" on page 16.

ıanges from Rev. ;12A-04/02 to Rev. ;12B-09/02

1. **Changed the Endurance on the Flash to 10,000 Write/Erase Cycles.**

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SPC

SMART PERIPHERAL CONTROLLER

DC MOTOR

Quick Start

1. PENDAHULUAN

Smart Peripheral Controller / SPC DC MOTOR merupakan pengontrol motor DC yang menggunakan I²C-bus sebagai jalur penyampaian data sehingga dapat lebih menghemat dan mempermudah pengkabelan. SPC DC MOTOR ini dilengkapi dengan prosedur **input** sehingga dapat mengetahui kecepatan motor pada saat tertentu, juga dilengkapi dengan prosedur **brake** yang dapat menghentikan motor secara cepat. Selain itu SPC DC MOTOR dapat digunakan secara paralel. Contoh aplikasi dari SPC DC MOTOR adalah untuk robot, dan sumber gerak lainnya.

2. SPESIFIKASI EKSTERNAL SPC DC MOTOR

Spesifikasi Eksternal SPC DC MOTOR sebagai berikut :

- Kompatibel penuh dengan DT-51 Minimum System Ver 3.0.
- Hanya perlu 2 jalur kabel untuk interface dengan mikroprosesor / mikrokontroler lain.
- Mempunyai 2 buah pengontrol motor DC yang dapat bekerja secara bersama-sama.
- Masing-masing pengontrol motor DC dilengkapi dengan prosedur input dan brake.
- Dapat dikontrol secara I²C-bus maupun paralel.
- Pengaturan kecepatan motor menggunakan metode Pulse Width Modulation (PWM).
- Semua pin–pin kontrol paralel diakses dengan taraf logika TTL.
- Dilengkapi dengan jumper untuk setting alamat, sehingga bila menggunakan I²C bus dapat di-ekspan sampai 8 board (16 buah motor DC) tanpa tambahan perangkat keras.
- Tersedia prosedur siap pakai untuk aplikasi SPC DC MOTOR.

3. PENGALAMATAN

MSB **Address** LSB

1	1	1	0	A2	A1	A0	1/0
Alamat tetap				Alamat terprogram			$R/\overline{W}$

<u>Pengalamatan memanfaatkan register</u> : ***AddressI2C*** dengan alamat memory 2Fh

Semua penggunaan dari I²C-bus selalu diawali dengan pengalamatan. Pada pengalamatan itu sendiri dibedakan menjadi tiga bagian : alamat tetap, alamat terprogram, dan Read/$\overline{\text{Write}}$ ($R/\overline{W}$). SPC DC MOTOR selalu menggunakan alamat tetap dengan nilai "1110", sedangkan untuk alamat terprogram digunakan untuk memberikan alamat terhadap modul sesuai dengan kehendak pemakai. Alamat terprogram diatur dengan cara mengganti setting jumper (dapat dilihat pada **bagian 6.2**) sehingga pada jalur I²C yang sama dengan alamat tetap yang sama ("1110") dapat digunakan 8 buah modul secara bersamaan dengan membedakan alamat terprogram. Bagian Read/$\overline{\text{Write}}$ (R/$\overline{\text{W}}$) bernilai "1" jika Master I^2C (DT-51 MinSys / mikrokontroler lain) akan membaca data dari Slave I^2C (SPC DC Motor) dan bernilai "0" jika DT-51 MinSys / mikrokontroler lain akan menulis data ke SPC DC Motor.

4. Command

MSB — **Command** — LSB

m3	m2	m1	m0	X	X	X	X

(m3–m0: Mode)

m3	m2	m1	m0	x	x	x	x	Mode
0	0	0	0	X	X	X	X	*Tidak terpakai*
0	0	0	1	X	X	X	X	Command **GateTime**
0	0	1	0	X	X	X	X	Command **PWM1**
0	0	1	1	X	X	X	X	Command **PWM2**
0	1	0	0	X	X	X	X	Command **Control**
0	1	0	1	X	X	X	X	Command **Input**
0	1	1	0	X	X	X	X	*Tidak terpakai*
.	.	.	.	.	.	.	.	.
.	.	.	.	.	.	.	.	.
1	1	1	1	X	X	X	X	*Tidak terpakai*

Perintah command terdapat bagian utama yaitu Mode. Mode digunakan untuk memilih perintah selanjutnya yang akan diberikan pada device sesuai dengan pilihan mode yang diberikan. Pada command memiliki 16 kemungkinan mode, namun pada SPC DC MOTOR ini hanya digunakan 5 mode saja.

4.1. Command Control

MSB — **Control** — LSB

0	1	0	0	X	X	X	X

(bit 7–4: Mode)

Command Control memanfaatkan register : ***DCControl***
Memanfaatkan alamat memory 3Ch atau dengan nama lain *BufferOut4*

MSB — **DC Control** — LSB

IN 2	IN 1	X	X	Dir 2	Run 2	Dir 1	Run 1

DC Control	Setting (H/ $\overline{\text{L}}$)	Fungsi
Run 1	Stop/ $\overline{\text{Run}}$	Untuk menjalankan dan menghentikan motor DC 1 : *Stop beri logika '1' (high)* *Run beri logika '0' (low)*
Dir 1	CW / $\overline{\text{CCW}}$	Untuk arah putaran motor DC 1 : *CW (searah jarum jam) beri logika '1' (high)* *CCW (berlawanan arah jarum jam) beri logika '0' (low)*
Run 2	Stop / $\overline{\text{Run}}$	Untuk menjalankan dan menghentikan motor DC 2 : *Stop beri logika '1' (high)* *Run beri logika '0' (low)*
Dir 2	CW / $\overline{\text{CCW}}$	Untuk arah putaran motor DC 2 : *CW (searah jarum jam) beri logika '1' (high)* *CCW (berlawanan arah jarum jam) beri logika '0' (low)*

In 1	On / Off	Untuk mengaktifkan dan menon-aktifkan input motor DC 1 *Mengaktifkan beri logika '1' (high)* *Menon-aktifkan beri logika '0' (low)*
In 2	On / Off	Untuk mengaktifkan dan menon-aktifkan input motor DC 2 *Mengaktifkan beri logika '1' (high)* *Menon-aktifkan beri logika '0' (low)*

Pengiriman Command Control diikuti dengan pengiriman DCControl. Namun dalam Application Layer, user hanya perlu mengisi DCControl. Command Control akan ditambahkan secara otomatis. DCControl digunakan untuk mengatur semua kegiatan dari motor DC.

- Jika salah satu dari **IN 1 atau IN 2** aktif, maka SPC DC MOTOR akan menghitung pulsa kecepatan motor DC pada input yang aktif. Perhitungan ini akan diperbarui setiap periode (ditentukan oleh command **GateTime**) sampai input dinon-aktifkan.
- Jika **IN 1 dan IN 2** aktif secara bersamaan, maka SPC DC MOTOR akan menghitung pulsa kecepatan motor DC 1 dan pulsa kecepatan motor DC 2 secara bergantian.

Contoh Aplikasi :
Bila ingin menjalankan motor DC 1 dengan arah searah jarum jam dan ingin mengetahui kecepatan dari motor DC 1 maka register DCControl dapat diisi dengan nilai '01000110b atau setara dengan '46h'.
Bila ingin membuat motor DC berhenti maka Control Run 1 harus dibuat 'high', yaitu: '01000111b'.

4.2. Command PWM

PWM1 (MSB … LSB)

0	0	1	0	X	X	X	X

Mode

PWM2 (MSB … LSB)

0	0	1	1	X	X	X	X

Mode

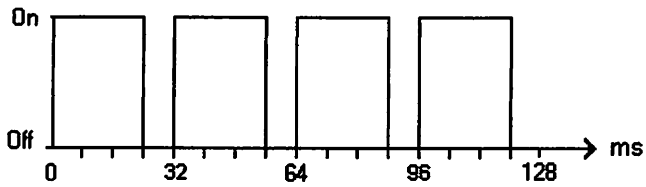
Command PWM1 memanfaatkan register : ***PWM1***
Memanfaatkan alamat memory 3Ah atau dengan nama lain *BufferOut2* untuk PWM1

Command PWM2 memanfaatkan register : ***PWM2***
Memanfaatkan alamat memory 3Bh atau dengan nama lain *BufferOut3* untuk PWM2

Pengiriman Command PWM diikuti dengan pengiriman PWM1 dan/atau PWM2. Namun dalam Application Layer, user hanya perlu mengisi PWM1 dan/atau PWM2. Command PWM akan ditambahkan secara otomatis. Nilai PWM1 dan PWM2 digunakan untuk mengatur kecepatan putaran motor DC, dengan cara menghidupkan dan mematikan motor DC secara bergantian dalam satu periode (32 ms) secara terus menerus. PWM hanya akan berfungsi jika motor DC dalam keadaan 'Run'.
Nilai dari PWM ini dapat diatur mulai dari 0 sampai 255 (FFh). Berikut ini adalah rumus perhitungan PWM dalam satu periode :

Ton = 32 ms **Toff** = 0 ms	Untuk	PWM = 0
Ton = (255 – PWM) * 0.125 ms **Toff** = 32 ms – **Ton**	Untuk	1 < PWM ≤ 255

Sebagai contoh, jika nilai PWM diset pada posisi 63d (3Fh), maka motor DC secara periodik berada pada posisi "On" selama 24 ms, dan pada posisi "Off" selama 8 ms.
Berikut ini adalah timing diagram dari nilai PWM 63d (3Fh).



Ada 2 buah register yang digunakan untuk mengatur setting PWM. Register **PWM1** digunakan untuk mengatur setting PWM motor DC 1 dan register **PWM2** digunakan untuk mengatur setting PWM motor DC 2.

Contoh Aplikasi :
Bila dikehendaki motor DC 1 berjalan dengan PWM 75% dan motor DC 2 berjalan dengan PWM 30%, maka perhitungannya sebagai berikut :

- Motor DC 1

  Ton = 75% * 32 ms
  = 24 ms

  Dari rumus di atas maka diperoleh

  24 ms = $(255 - PWM_1) * 0.125$ ms

  isi register PWM1 = **'63d'**

- Motor DC 2

  Ton = 30% * 32 ms
  = 9,6 ms

  Dari rumus di atas maka diperoleh

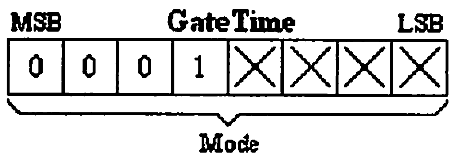
  9,6 ms = $(255 - PWM_2) * 0.125$ ms

  $PWM_2 = 178{,}2$

  Dibulatkan ke bilangan desimal terdekat maka

  isi register PWM2 = **'178d'**

4.3. Command GateTime



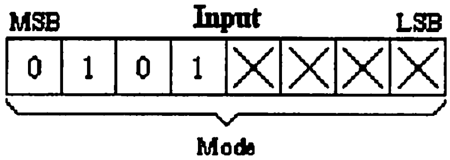
Command GateTime memanfaatkan register : ***GateTime***
Memanfaatkan alamat memory 39h atau dengan nama lain *BufferOut1*

GateTime	Time	Resolusi
80 H	2000 ms	0.5 Hz
40 H	1000 ms	1 Hz
20 H	500 ms	2 Hz
10 H	250 ms	4 Hz
08 H	125 ms	8 Hz
04 H	62.5 ms	16 Hz
02 H	31,25 ms	32 Hz
01 H	15,625 ms	64 Hz

Pengiriman Command GateTime diikuti dengan pengiriman GateTime. Namun dalam Application Layer, user hanya perlu mengisi GateTime. Command GateTime akan ditambahkan secara otomatis. GateTime digunakan untuk mengatur besarnya waktu yang dibutuhkan untuk menghitung banyaknya pulsa kecepatan motor DC setiap periode. Ada delapan nilai GateTime yang dapat digunakan, seperti yang terlihat pada tabel di atas. Semakin besar nilai GateTime, perhitungan pulsa kecepatan motor DC akan semakin akurat, namun waktu yang dibutuhkan untuk menghitung kecepatan dalam satu periode lebih lama. Default GateTime dari SPC DC MOTOR ini adalah '08h'.

Contoh :
Jika GateTime diberi nilai '20h', maka waktu yang dibutuhkan untuk menghitung pulsa kecepatan motor DC adalah 500 ms, dan kesalahan perhitungannya adalah ± 1 Hz.

4.4. Command Input

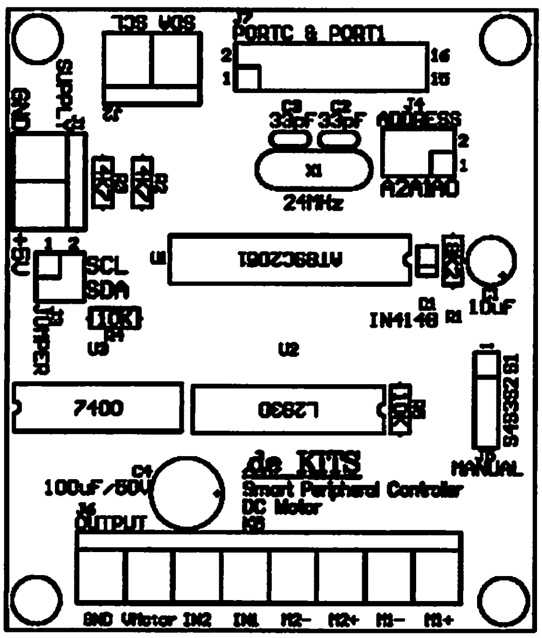


Command Input memanfaatkan register : ***InputH1, InputL1, InputH2, InputL2.***
Memanfaatkan alamat memory 30h atau dengan nama lain *BufferIn0* untuk InputH1
Memanfaatkan alamat memory 31h atau dengan nama lain *BufferIn1* untuk InputL1
Memanfaatkan alamat memory 32h atau dengan nama lain *BufferIn2* untuk InputH2
Memanfaatkan alamat memory 33h atau dengan nama lain *BufferIn3* untuk InputL2

Pengiriman Command Input diikuti dengan pembacaan InputH1 dan InputL1 dan/atau InputH2 dan InputL2. Namun dalam Application Layer, user hanya perlu membaca InputH1 dan InputL1 dan/atau InputH2 dan InputL2. Command Input akan ditambahkan secara otomatis. InputH1, InputL1, InputH2, dan InputL2 digunakan untuk menyimpan hasil perhitungan pulsa kecepatan putaran motor DC dalam satu detik. Command Input hanya dapat digunakan, jika motor DC dilengkapi dengan data input kecepatan putaran motor yang berupa pulsa TTL. Perhitungan dilakukan saat terjadi transisi dari high menjadi low dari data input kecepatan. Semakin cepat putaran motor, maka pulsa yang dihasilkan akan semakin tinggi frekuensinya. Sebuah motor DC dalam satu putaran bisa menghasilkan lebih dari satu pulsa tergantung dari spesifikasi motor DC tersebut.

Pada SPC DC MOTOR ini, pulsa maksimum yang dapat dihasilkan dalam satu detik adalah 65.535 (16 bit), yang disimpan didalam dua register yaitu **InputH1** (bit 8–15) dan **InputL1** (bit 0–7) untuk motor DC 1 dan **InputH2** (bit 8–15) dan **InputL2** (bit 0-7) untuk motor DC 2.

5. TATA LETAK KOMPONEN SPC DC MOTOR



6. SISTEM YANG DIANJURKAN

Perangkat keras :

- PC XT / AT Pentium™ IBM Compatible dengan port serial (COM 1/ COM2).
- Board DT-51 Minimum System.
- Floppy Disk 3.5" , kapasitas 1,44Mbytes atau CD-ROM Drive.
- Hard disk dengan kapasitas minimum 500Kbytes.

Perangkat lunak :

- Sistem operasi MS-DOS™ atau PC-DOS™.
- Assembler ASM51©
- File-file yang ada pada pada disket/CD program.

6.1. HUBUNGAN DT-51 MINIMUM SYSTEM DENGAN SPC DC MOTOR

SPC DC MOTOR merupakan suatu sistem yang '**Smart**'. Selain dapat dihubungkan dengan DT-51 Minimum System atau dengan sistem mikroprosesor / mikrokontroler yang lain, SPC DC MOTOR dapat juga difungsikan secara paralel (lihat **bagian 6.4**). Apabila Anda ingin menghubungkan SPC DC MOTOR dengan sistem yang lain kami sarankan untuk mempelajari skema SPC DC MOTOR.

Untuk menghubungkan SPC DC MOTOR dengan DT-51 Minimum System dianjurkan untuk menggunakan kabel pita (flat ribbon cable).

Hubungannya ditunjukkan pada tabel berikut :

I^2C Bus	DT-51 Minimum System PORT C & PORT 1	SPC DC MOTOR J7
SCL	Pin 15 (Port 1.6)	Pin 15 (Port 3.3)
SDA	Pin 16 (Port 1.7)	Pin 16 (Port 3.2)

Catu daya 5V DC dihubungkan dengan konektor J1 (Supply). Perhatikan polaritasnya jangan sampai terbalik, karena dapat mengakibatkan kerusakan.

Penting !

Referensi ground (GND) antara modul SPC DC MOTOR dengan DT-51 Minimum System harus sama.

6.2. SETTING JUMPER

Alamat terprogram setiap board SPC DC MOTOR ditentukan oleh setting jumper J4.

J4 (A2)	J4 (A1)	J4(A0)	Alamat Terprogram	
□	□	□	0	000
□	□		1	001
□		□	2	010
□			3	011
	□	□	4	100
	□		5	101
		□	6	110
			7 (default)	111
Keterangan :				
□ : jumper tersambung (ON)				

Jumper J3 (Pull up SCL/SDA) digunakan untuk resistor pull up SDA (I^2C bus data input / output) dan SCL (I^2C bus clock input). Apabila lebih dari satu board SPC DC MOTOR dihubungkan pada I^2C bus maka hanya perlu memasang jumper J3 pada salah satu board saja.

6.3. EKSPANSI SPC DC MOTOR

SPC DC MOTOR dapat di-ekspan sampai 8 board. Beberapa hal yang perlu diperhatikan apabila menggunakan lebih dari satu board SPC DC MOTOR :

- Setiap board harus mempunyai alamat terprogram yang berbeda, ditentukan oleh jumper

J4 (A0/A1/A2).

- Jumper J3 pada salah satu board saja yang dipasang.

6.4. PENGGUNAAN SPC DC MOTOR SECARA PARALEL

SPC DC MOTOR dapat digunakan secara paralel dengan cara mengatur pin–pin S1, S2, S3, dan S4 yang ada pada board SPC DC MOTOR.
Berikut adalah tabel kegunaan dari pin–pin tersebut:

Pin	Name	Setting	Fungsi
S1	Run 1	Stop / $\overline{Run}$	Untuk menjalankan atau mematikan motor DC 1 *Stop beri logika '1' (high)* *Run beri logika '0' (low)*
S2	Dir 1	CW / $\overline{CCW}$	Untuk arah putaran motor DC 1 *CW (searah jarum jam) beri logika '1' (high)* *CCW (berlawanan arah jarum jam) beri logika '0' (low)*
S3	Run 2	Stop / $\overline{Run}$	Untuk menjalankan atau mematikan motor DC 2 *Stop beri logika '1' (high)* *Run beri logika '0' (low)*
S4	Dir 2	CW / $\overline{CCW}$	Untuk arah putaran motor DC 2 *CW (searah jarum jam) beri logika '1' (high)* *CCW (berlawanan arah jarum jam) beri logika '0' (low)*

- Secara default jika pin–pin S1, S2, S3, dan S4 tersebut tidak dihubungkan (Floating/mengambang) maka akan selalu berlogika "high".
- Untuk dapat menjalankan SPC DC MOTOR secara paralel, setting kedua motor DC pada register **DCControl** harus dalam keadaan Stop.
- Apabila pada saat yang bersamaan terjadi pengaturan secara 'I^2C' dan 'Paralel' maka yang manjadi prioritas adalah I^2C, setelah perintah I^2C selesai dilaksanakan maka perintah paralel baru dapat dilaksanakan.
- Untuk pengaturan PWM secara paralel, dapat dilakukan dengan cara memberi pulsa secara periodik pada pin S1 atau S3 dengan frekuensi maksimal 10 KHz.

Contoh Aplikasi :
Bila diinginkan motor DC 1 dijalankan secara paralel dengan PWM 50% dan putaran searah jarum jam, maka pin S2 diberi logika '1' dan pin S1 diberi sinyal kotak dengan periode high dan periode low yang sama besarnya.

6.5. PENYAMBUNGAN SPC DC MOTOR DENGAN MOTOR DC

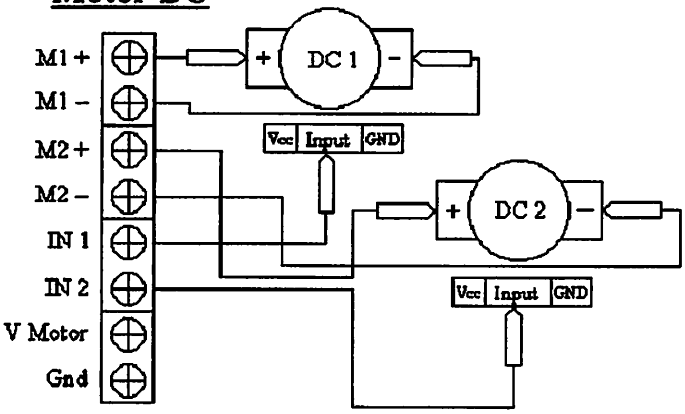
Dalam penyambungan motor DC dengan modul SPC DC MOTOR perlu diperhatikan tipe dari motor DC yang akan dipergunakan.
Modul SPC DC MOTOR dapat dipergunakan untuk dua buah motor DC yang mempunyai tegangan kerja yang sama. Modul SPC DC MOTOR ini dapat digunakan baik untuk motor DC yang mempunyai data input kecepatan maupun yang tidak mempunyai data input kecepatan. Untuk motor DC yang tidak mempunyai data input kecepatan, prosedur Input dan Brake yang terdapat pada SPC DC MOTOR ini tidak dapat digunakan.

Berikut adalah cara pemasangan dari kedua buah motor DC yang dilengkapi dengan data input.

- Modul SPC DC MOTOR dapat dipergunakan untuk motor DC dengan tegangan kerja dari 5 Volt sampai dengan 36 Volt.
- Arus RMS maksimum untuk modul SPC DC MOTOR adalah 600 mA.
- Arus impuls tak berulang maksimum untuk modul SPC DC MOTOR adalah 1.2 A.
- Sudah dilengkapi dioda clamp secara internal.
- Hubungkan catu daya positif (+) untuk motor DC pada V*motor* dan catu daya negatif (-) pada *GND.*
  Tegangannya harus sesuai dengan tegangan kerja motor.
- Untuk motor DC 1, sambungkan kutub positif motor DC pada M1+ dan kutub negatif motor DC pada M1- serta data input pada IN1 secara benar.
- Untuk motor DC 2, sambungkan kutub positif motor DC pada M2+ dan kutub negatif

motor DC pada M2- serta data input pada IN2 secara benar (lihat gambar).

Motor DC



6.6. MENCOBA SPC DC MOTOR DENGAN EXAMPLE.HEX

- Hubungkan DT-51 Minimum System dengan SPC DC MOTOR (lihat bagian 6.1)
- Hubungkan SPC DC MOTOR dengan motor DC (lihat bagian 6.5)
- Setting alamat SPC DC MOTOR pada alamat terprogram ke-7 (default)
- Download EXAMPLE.HEX yang terdapat pada disket/CD
- Motor DC 1 akan bergerak secara Clockwise (CW) dengan PWM 100 % dan input 1 aktif sedangkan motor DC 2 akan bergerak secara Counter Clockwise (CCW) dengan PWM 50 %.
  Setelah 5 detik, motor DC 1 dihentikan dengan menggunakan prosedur Brake sedangkan motor DC 2 dihentikan secara manual (tanpa prosedur Brake). Demikian seterusnya.

7. PERANGKAT LUNAK SPC DC MOTOR

7.1. DRIVER DAN RUTIN

SPC DC MOTOR dilengkapi dengan driver **DCMOTOR.INC** yang akan mempermudah user dalam pemrograman. **DCMOTOR.INC** menggunakan resource dari mikrokontroler 89C51 sebagai berikut :

- Internal RAM alamat 21h bit 0 dan 1
- Internal RAM dengan alamat 2Fh – 3Fh, dan 40h - 43h
- P1.6 dan P1.7

Sehingga tidak boleh dipakai oleh user untuk keperluan lain, kecuali user mampu melakukan modifikasi pengaturan memori dengan benar.

Driver ini menggunakan 13 buah register yang terdiri dari:

AddressI2C	GateTime	PWM1	PWM2	DCControl
InputH1	InputL1	InputH2	InputL2	
BrakeH1	BrakeL1	BrakeH2	BrakeL2	

Kegunaan dari register-register tersebut dapat dilihat pada **bagian 4**.
Dari register tersebut akan digunakan dalam 9 rutin penting berikut :

DCInit

Fungsi : Untuk menginisialisasi SPC DC Motor.
Input : AddressI2C, GateTime, PWM1, PWM2 dan DCControl
Output : Flag FAck
Keterangan :

- Rutin ini digunakan untuk memberikan nilai awal atau inisialisasi tanpa menjalankan motor DC, yaitu dengan memberi logika high '1' pada setting Run dari DCControl.
- Rutin ini dapat juga digunakan untuk menjalankan rutin SetGateTime, SetPWM1, SetPWM2 dan SetControl dalam satu buah rutin.

- ❖ Jika **Flag FAck** bernilai '1' maka SPC DC MOTOR siap untuk digunakan.

Metode : Isi register AddressI2C, GateTime, PWM1, PWM2 dan DCControl sesuai dengan kebutuhan kemudian panggil rutin DCInit.

SetGateTime

Fungsi : Mengatur besarnya waktu yang dibutuhkan untuk menghitung pulsa input kecepatan motor DC dalam satu periode.
Input : AddressI2C dan GateTime
Output : Flag FAck
Keterangan : Tabel pengaturan nilai register GateTime ini dapat dilihat pada **bagian 4.3.**
Metode : Isi register AddressI2C dan GateTime sesuai dengan kebutuhan kemudian panggil rutin SetGateTime.

SetPWM1

Fungsi : Mengatur kecepatan putaran motor DC 1
Input : AddressI2C dan PWM1
Output : Flag FAck
Keterangan : Perhitungan kecepatan putaran motor DC 1 dapat dilihat pada **bagian 4.2.**
Metode : Isi register AddressI2C dan PWM1 sesuai dengan kebutuhan kemudian panggil rutin SetPWM1.

SetPWM2

Fungsi : Mengatur kecepatan putaran motor DC 2
Input : AddressI2C dan PWM2
Output : Flag FAck
Keterangan : Perhitungan kecepatan putaran motor DC 2 dapat dilihat pada **bagian 4.2.**
Metode : Isi register AddressI2C dan PWM2 sesuai dengan kebutuhan kemudian panggil rutin SetPWM2.

SetControl

Fungsi : Untuk menjalankan atau menghentikan motor DC, mengubah arah putaran motor DC, dan mengaktifkan perhitungan pulsa input kecepatan pada motor DC.
Input : AddressI2C dan DCControl
Output : Flag FAck
Keterangan :

- ❖ Rutin ini digunakan untuk mengatur semua aktivitas dari SPC DC MOTOR.
- ❖ Tabel dari nilai register DCControl ini dapat dilihat pada **bagian 4.1.**

Metode : Isi register AddressI2C dan DCControl sesuai dengan kebutuhan kemudian panggil rutin SetControl.

GetInput1

Fungsi : Menyimpan hasil perhitungan pulsa input kecepatan motor DC 1.
Input : AddressI2C
Output : InputH1 dan InputL1
Keterangan : Hasil dari rutin ini disimpan pada register **InputH1** untuk bit 8-15 dan register **InputL1** untuk bit 0-7.
Metode : Isi register AddressI2C sesuai dengan alamat kemudian panggil rutin GetInput1.

GetInput2

Fungsi : Menyimpan hasil perhitungan pulsa input kecepatan motor DC 2.
Input : AddressI2C
Output : InputH2 dan InputL2
Keterangan : Hasil dari rutin ini disimpan pada register **InputH2** untuk bit 8-15 dan register **InputL2** untuk bit 0-7.

Metode : Isi register AddressI2C sesuai dengan alamat kemudian panggil rutin GetInput2.

Brake1

Fungsi : Untuk menghentikan motor DC 1 secara cepat.
Input : AddressI2C, BrakeH1 dan BrakeL1
Output : InputH1, InputL1
Keterangan :

- ❖ Fungsi ini hanya bisa digunakan, jika motor DC 1 dilengkapi dengan data input kecepatan putaran motor.
- ❖ Motor DC 1 akan berhenti jika pulsa input kecepatan lebih rendah dari input brake.
- ❖ Nilai pulsa input kecepatan terakhir sebelum motor DC 1 berhenti disimpan pada register InputH1 dan InputL1.

Metode : Isi register AddressI2C, **BrakeH1** untuk bit 8-15 dan **BrakeL1** untuk bit 0-7 sesuai dengan kebutuhan kemudian panggil rutin Brake1.

Brake2

Fungsi : Untuk menghentikan motor DC 2 secara cepat.
Input : AddressI2C, BrakeH2 dan BrakeL2
Output : InputH2, InputL2
Keterangan :

- ❖ Fungsi ini hanya bisa digunakan, jika motor DC 2 dilengkapi dengan data input kecepatan putaran motor.
- ❖ Motor DC 2 akan berhenti jika pulsa input kecepatan lebih rendah dari input brake.
- ❖ Nilai pulsa input kecepatan terakhir sebelum motor DC 2 berhenti disimpan pada register InputH2 dan InputL2.

Metode : Isi register AddressI2C, **BrakeH2** untuk bit 8-15 dan **BrakeL2** untuk bit 0-7 sesuai dengan kebutuhan kemudian panggil rutin Brake2.

7.2. CONTOH APLIKASI DAN PROGRAM

Bila dikehendaki modul SPC DC MOTOR dengan alamat terprogram ke-5 menjalankan motor DC 1 yang mempunyai input kecepatan dengan arah searah jarum jam (CW) dengan setting PWM 75% dan menjalankan motor DC 2 yang tidak mempunyai input kecepatan dengan arah berlawanan jarum jam (CCW) dengan PWM 50%.
Setelah 5 detik, arah motor DC 1 berubah menjadi berlawanan jarum jam (CCW) dengan PWM 25% dan arah motor DC 2 menjadi searah jarum jam (CW) dengan PWM 100%.
Lima detik kemudian motor DC 2 berhenti, dan 5 detik kemudian motor DC 1 juga berhenti.

<u>Listing program untuk kasus diatas:</u>

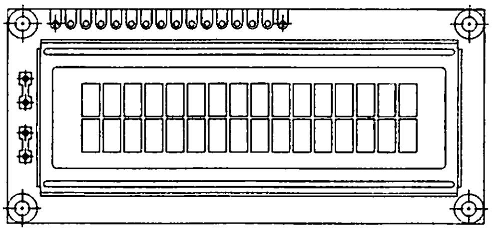
```
$MOD51
        CSEG
        ORG   4000H
        LJMP  Start

        ORG   4100H
        $INCLUDE(ENG_I2C.INC)         ;Driver untuk semua produk
                                      ;SPC I2C (HARUS DITULISKAN
                                      ;TERLEBIH DAHULU SEBELUM
                                      ;DCMOTOR.INC)
        $INCLUDE(DCMOTOR.INC)         ;Driver SPC DC MOTOR

Delay5s:
        MOV   R5,#28H
D1:     MOV   R6,#0FFH
D2:     MOV   R7,#0FFH
        DJNZ  R7,$
        DJNZ  R6,D2
        DJNZ  R5,D1
        RET
```

```
Start:
      MOV    SP, #50H
      MOV    AddressI2C,#11101010B    ;memasukkan alamat i2c
      MOV    DCControl,#01000010B     ;memasukkan nilai DCControl
      MOV    PWM1,#03FH               ;memasukkan PWM 1 = 75%
      MOV    PWM2,#07FH               ;memasukkan PWM 2 = 50%
      ACALL DCInit                    ;memanggil rutin DCInit
      ACALL Delay5s                   ;Delay 5 detik

      MOV    PWM1,#0BFH               ;memasukkan PWM 1 = 25%
      ACALL SetPWM1                   ;memanggil rutin SetPWM1
      MOV    PWM2,#00H                ;memasukkan PWM 2 = 100%
      ACALL SetPWM2                   ;memanggil rutin SetPWM2
      MOV    DCControl,#01001000B     ;memasukkan nilai DCControl
      ACALL SetControl                ;memanggil rutin SetControl
      ACALL Delay5s                   ;Delay 5 detik

      MOV    DCControl,#10001100B     ;memasukkan nilai DCControl
      ACALL SetControl                ;memanggil rutin SetControl
      ACALL Delay5s                   ;Delay 5 detik

      ACALL GetInput1                 ;memanggil rutin GetInput1
      MOV    BrakeH1,#20H             ;\memasukkan input Brake 1
      MOV    BrakeL1,#00H             ;/
      ACALL Brake1                    ;memanggil rutin Brake1
      END
```

Catatan :

- Bagi user yang ingin mempelajari lebih lanjut mengenai SPC DC MOTOR dapat membaca MANUAL SPC DC MOTOR.PDF serta contoh program EXAMPLE.ASM yang disertakan pada disket/CD.
- Technical Support : support@innovativeelectronics.com

16 x 2 Character LCD



FEATURES

- 5 x 8 dots with cursor
- Built-in controller (KS 0066 or Equivalent)
- + 5V power supply (Also available for + 3V)
- 1/16 duty cycle
- B/L to be driven by pin 1, pin 2 or pin 15, pin 16 or A.K (LED)
- N.V. optional for + 3V power supply

MECHANICAL DATA

ITEM	STANDARD VALUE	UNIT
Module Dimension	80.0 x 36.0	mm
Viewing Area	66.0 x 16.0	mm
Dot Size	0.56 x 0.66	mm
Character Size	2.96 x 5.56	mm

ABSOLUTE MAXIMUM RATING

ITEM	SYMBOL	STANDARD VALUE			UNIT
		MIN.	TYP.	MAX.	
Power Supply	VDD-VSS	- 0.3	–	7.0	V
Input Voltage	VI	- 0.3	–	VDD	V

NOTE: VSS = 0 Volt, VDD = 5.0 Volt

ELECTRICAL SPECIFICATIONS

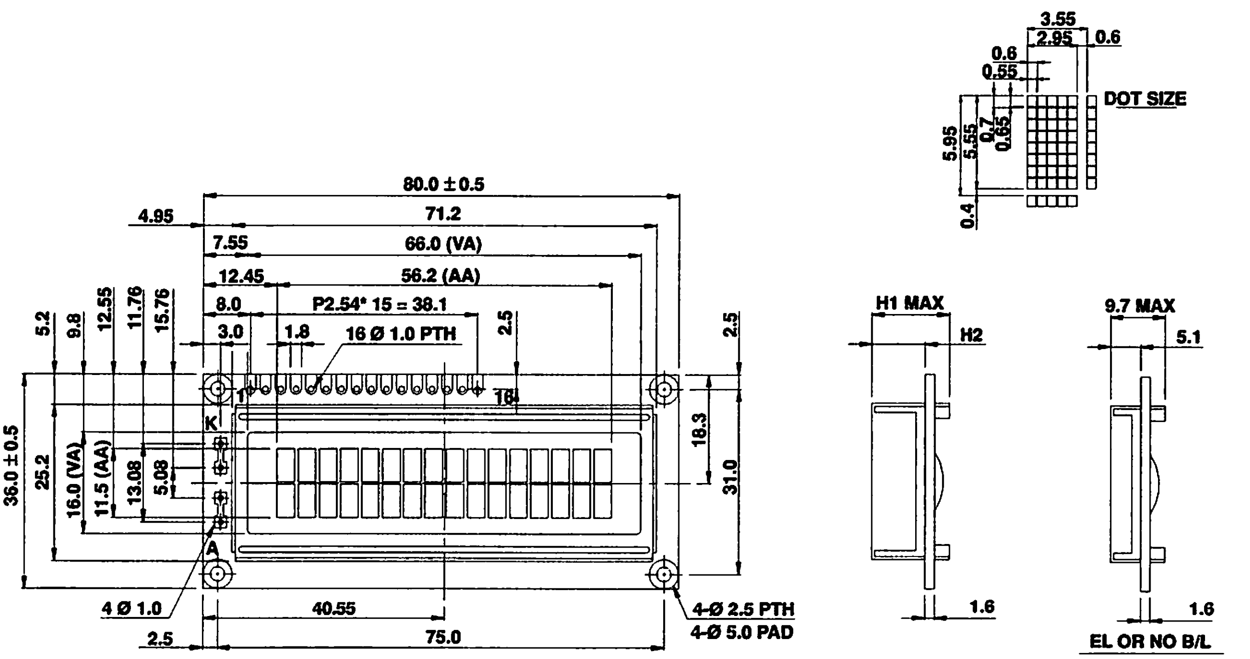
ITEM	SYMBOL	CONDITION		STANDARD VALUE			UNIT
				MIN.	TYP.	MAX.	
Input Voltage	VDD	VDD = + 5V		4.7	5.0	5.3	V
		VDD = + 3V		2.7	3.0	5.3	V
Supply Current	IDD	VDD = 5V		–	1.2	3.0	mA
Recommended LC Driving Voltage for Normal Temp. Version Module	VDD - V0	- 20 °C		–	–	–	V
		0°C		4.2	4.8	5.1	
		25°C		3.8	4.2	4.6	
		50°C		3.6	4.0	4.4	
		70°C		–	–	–	
LED Forward Voltage	VF	25°C		–	4.2	4.6	V
LED Forward Current	IF	25°C	Array	–	130	260	mA
			Edge	–	20	40	
EL Power Supply Current	IEL	Vel = 110VAC:400Hz		–	–	5.0	mA

DISPLAY CHARACTER ADDRESS CODE:

Display Position	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16
DD RAM Address	00	01														0F
DD RAM Address	40	41														4F

PIN NUMBER	SYMBOL	FUNCTION
1	Vss	GND
2	Vdd	+ 3V or + 5V
3	Vo	Contrast Adjustment
4	RS	H/L Register Select Signal
5	R/$\overline{W}$	H/L Read/Write Signal
6	E	H →L Enable Signal
7	DB0	H/L Data Bus Line
8	DB1	H/L Data Bus Line
9	DB2	H/L Data Bus Line
10	DB3	H/L Data Bus Line
11	DB4	H/L Data Bus Line
12	DB5	H/L Data Bus Line
13	DB6	H/L Data Bus Line
14	DB7	H/L Data Bus Line
15	A/Vee	+ 4.2V for LED/Negative Voltage Output
16	K	Power Supply for B/L (OV)

DIMENSIONS in millimeters



LED - H/L B/L	HIGH	LOW
H1	13.2	12.1
H2	8.6	7.5

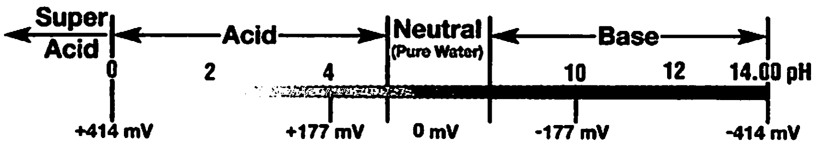
Introduction to pH and pH Measurement

Definition

The pH of a solution measures the degree of acidity or alkalinity relative to the ionization of water sample. Pure water dissociates to yield 10^{-7} M of $[H^+]$ and $[OH^-]$ at 25 °C; thus, the pH of water is neutral i.e. 7.

$$pH_{water} = -\log [H^+] = -\log 10^{-7} = 7$$

Most pH readings range from 0 to 14. Solutions with a higher $[H^+]$ than water (pH less than 7) are acidic; solutions with a lower $[H^+]$ than water (pH greater than 7) are basic or alkaline.



pH Measurement

Measuring pH involves comparing the potential of solutions with unknown $[H^+]$ to a known reference potential. pH meters convert the voltage ratio between a reference half-cell and a sensing half-cell to pH values.

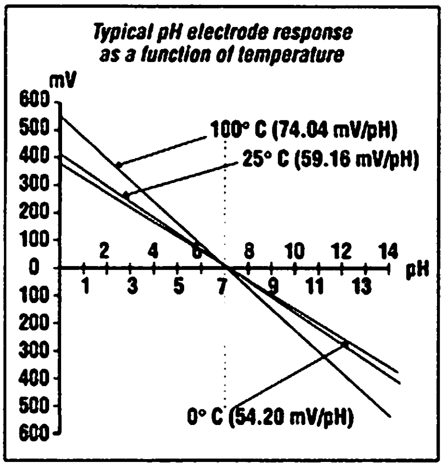
In acidic or alkaline solutions, the voltage on the outer membrane surface changes proportionally to changes in $[H^+]$. The pH meter detects the change in potential and determines $[H^+]$ of the unknown by the Nernst equation:

$$E = E^o + (2.3RT)/nF \log \{\text{unknown } [H^+]/\text{internal } [H^+]\}$$

where: E = total potential difference (measured in mV); E^o = reference potential; R = gas constant; T = temperature in Kelvin; n = number of electrons; F = Faraday's constant; $[H^+]$ = hydrogen ion concentration.

pH Temperature Compensation

The pH of any solution is a function of its temperature. Voltage output from the electrode changes linearly in relationship to changes in pH, and the temperature of the solution determines the slope of the graph. One pH unit corresponds to 59.16 mV at 25 °C, the standard voltage and temperature to which all calibrations are referenced. The electrode voltage decreases to 54.20 mV/pH unit at 0.0 °C and increases to 74.04 mV/pH unit at 100.0 °C.



Since pH values are temperature dependent, pH applications require some form of temperature compensation to ensure standardized pH values. Meters and controllers with automatic temperature compensation (ATC) receive a continuous signal from a temperature element and automatically correct the pH value based on the temperature of the solution. Manual temperature compensation requires the user to enter the temperature of the solution in order to correct pH readings for temperature. ATC is considered to be more practical for most pH applications.

pH System

A successful pH reading is dependent upon all components of the system being operational. Problems with any one of the three: electrode, meter or buffer will yield poor readings.

Electrodes: A pH electrode consists of two half-cells; an indicating electrode and a reference electrode. Most applications today use a combination electrode with both half cells in one body. Over 90% of pH measurement problems are related to the improper use, storage or selection of electrodes.

Meters: A pH meter is a sophisticated volt meter capable of reading small millivolt changes from the pH electrode system. The meter is seldom the source of problems for pH measurements. Today pH meters have temperature compensation (either automatic or manual) to correct for variations in slope caused by changes in temperature. Microprocessor technology has created many new convenience features for pH measurement; auto-buffer recognition, calculated slope and % efficiency, log tables for concentration of ions and more.

Buffers: These solutions of known pH value allow the user to adjust the system to read accurate measurements. For best accuracy:

- Standardization should be performed with fresh buffer solutions.
- Buffer used should frame the range of pH for the samples being tested.
- Buffers should be at the same temperature as the samples. (For example: if all your samples are at 50 °C, warm your buffers to 50 °C using a beaker in a warm bath.)

Buffer values are dependent upon temperature.

Frequently Asked Questions on pH

If I order a pH meter, what accessories do I need to use with it?

You need a pH electrode and at least two pH buffers, one at pH 7 and the other at either pH 4 or 10.

My co-worker is using an ORP (Redox) electrode to measure the same solution as I, but our readings are not even close. Could there be something wrong with my electrode?

No. Because ORP (Redox) is a relative measurement, it is almost impossible to compare two ORP electrodes directly. ORP electrodes come equipped with bands made up of platinum, gold, or hydrogen, for example. Each band type will give you a different reading in the same solution. Even if the electrodes are of the same band type, the leak rate through the reference junction will affect your readings.

Instead, simply measure two solutions and note the difference between the two electrodes. Once again, the difference between two solutions should compare. You should be looking for a change of state, rather than an absolute measurement. You can check your electrode using pH buffer and Quinhydrone.

Can I measure the pH of a gas?

The only way to measure the pH of a gas is to dissolve it into distilled water and measure the mixture. Technically, the pH of the distilled water/gas mixture will be that of the gas.

How should I store my electrode?

The best solution for electrode storage is 4M KCl. pH 4 buffer, pH 7 buffer, or tap water are also acceptable. Never store your electrode in distilled water.

What is the difference between a combination electrode and a sensing electrode with a reference cell?

A combination electrode is more convenient and requires a smaller sample container and volume. The sensing electrode with reference cell combination allows you to select the reference cell most compatible with your solution. You can select the double junction, calomel, or half cell. You will probably get better life from this combination, and can replace each cell individually.

How does one take soil pH measurements?

Prepare the sample by combining a 5 g soil sample with 5 g of distilled water, mixing thoroughly, and allowing the mixture to settle for 10 minutes. Carefully insert probe so bulb is in the soil part and the junction is in the supernatant. Allow reading to stabilize.

Why is a double junction electrode better than a single junction electrode?

A double junction electrode is less likely to become clogged because the second junction is located higher up in the probe out of contact with the fluid.

Is Automatic Temperature Compensation (ATC) really necessary?

The necessity of ATC depends on the required accuracy of a pH reading. pH readings vary with temperature. For example, a sample with a pH of 7 at 25°C, may have a pH of 7.08 at 5°C and a pH of 6.98 at 60°C.

When do you use a half cell?

When you are measuring a pressurized flow in a stream or pipe. The reference half cell would be mounted upstream, the measuring electrode would be mounted down stream.

How often should I calibrate my pH meter?

Before each use or set of uses.

How can you unclog a pH electrode? How can you restore a dry pH electrode?

First check the interior wire. If corrosion is evident, replace the electrode. If not, then soak the electrode in pH 4 buffer solution at 50 degrees C for 2-4 hours. Restore a dry electrode by soaking it in tap water after rinsing out the refill chamber with distilled water and refilling with the proper solution.

If measuring the entire range of pH what slope should be used?

The upper end or pH 10 buffer.

What is the difference between blue glass and amber glass, and what does that have to do with pH measurement?

The valance of Na^+ is much larger than H^+. Amber glass has a smaller pore size thus possibly discriminating between H^+ and Na^+ allowing only the smaller H^+ to enter the greatly eliminating Na^+ interference.

pH Electrode Selection Guide

The Electrode Pair

Sensing and reference half-cell electrodes must be used together to complete the pH circuit. Most of the electrodes in our catalog are combination electrodes that house both half-cells in a single probe.

Sensing Half-Cells

Sensing half-cells are the measuring portion of the electrode system and contain the pH-sensitive membrane.

Glass vs ISFET Sensors

The glass membrane or bulb of an electrode is constructed for use in specific conditions. Different types of glas membranes can strengthen the electrode, expand its temperature range, or prevent sodium error at high pH values.

- General-purpose glass: various pH ranges, temperatures to 100°C (212°F).
- Blue glass: pH 0-13, temperatures to 110°C (230°F)
- Amber glass: pH 0-14, temperatures to 110°C (230°F), low sodium (Na^+) error (In solutions with high Na^+ concentrations, Na^+ can be misread as H^+ at pH 12 and higher.)

The solid-state ISFET (ion-specific field effect transistor) electrodes have non-glass measuring surface won't break and wipes clean for dry storage—excellent for use in the food industry.

Glass vs Epoxy Body

Epoxy-body electrodes are impact resistant and ideal for rough handling, but should not be used at higher temperatures or for inorganics. Glass-body electrodes withstand high temperatures and highly corrosive materials or solvents.

Reference Half-Cells

Reference half-cells provide the reference potential needed for pH measurement. Our selection of electrodes includes a variety of reference cell options:

Single- vs Double-Junction

In combination electrodes, the reference junction allows H^+ ions to pass freely between the reference and sensing half-cells to complete the electrical circuit. Economical single-junction electrodes are ideal for general-purpose applications. Use double-junction electrodes with solutions that contain sulfides, heavy metals, or tris buffers to prevent contamination of the reference cell.

Although most reference cells feature a H^+-permeable glass junction, electrodes with reference junctions made of TEFLON® PTFE are also available—use with solutions that may clog conventional glass junctions.

Silver/Silver Chloride (Ag/AgCl) vs Calomel (Hg/Hg_2Cl_2)

Ag/AgCl is the most common internal element, suitable for almost all applications [temp limit: 80°C (176°F)]. Hg/Hg_2Cl_2 is recommended for use in solutions containing proteins, organics, or heavy metals that could react with silver and clog the reference junction [temp limit: 70°C (158°F)].

Refillable vs Sealed

Refillable electrodes have ports that allow you to refill the reference chamber with reference solution—they are economical and long-lasting. Sealed electrodes are rugged and require virtually no maintenance; however, they must be replaced when the fill-solution level is low.

TEFLON® is a registered trademark of DuPont.

AC Electrical Characteristics (Continued)

Note 7: The $\overline{CS}$ input is assumed to bracket the $\overline{WR}$ strobe input and therefore timing is dependent on the $\overline{WR}$ pulse width. An arbitrarily wide pulse width will hold the converter in a reset mode and the start of conversion is initiated by the low to high transition of the $\overline{WR}$ pulse (see timing diagrams).

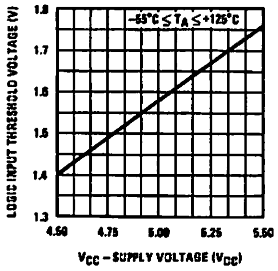
Note 8: None of these A/Ds requires a zero adjust (see section 2.5.1). To obtain zero code at other analog input voltages see section 2.5 and *Figure 7*.

Note 9: The $V_{REF}/2$ pin is the center point of a two-resistor divider connected from V_{CC} to ground. In all versions of the ADC0801, ADC0802, ADC0803, and ADC0805, and in the ADC0804LCJ, each resistor is typically 16 kΩ. In all versions of the ADC0804 except the ADC0804LCJ, each resistor is typically 2.2 kΩ.

Note 10: Human body model, 100 pF discharged through a 1.5 kΩ resistor.

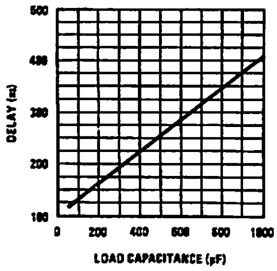
Typical Performance Characteristics

Logic Input Threshold Voltage vs. Supply Voltage



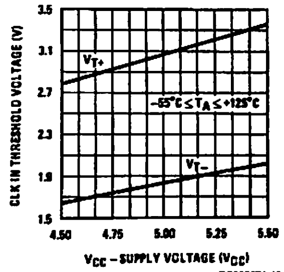
DS005671-38

Delay From Falling Edge of $\overline{RD}$ to Output Data Valid vs. Load Capacitance



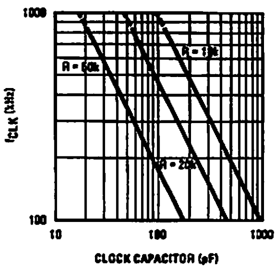
DS005671-39

CLK IN Schmitt Trip Levels vs. Supply Voltage



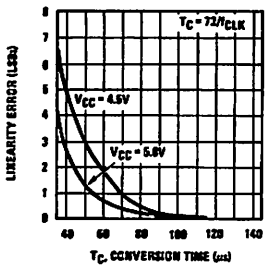
DS005671-40

f_{CLK} vs. Clock Capacitor



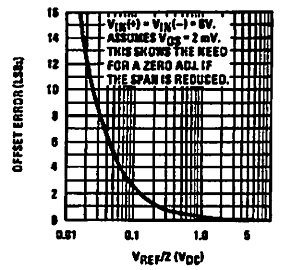
DS005671-41

Full-Scale Error vs Conversion Time



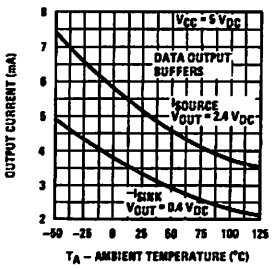
DS005671-42

Effect of Unadjusted Offset Error vs. $V_{REF}/2$ Voltage



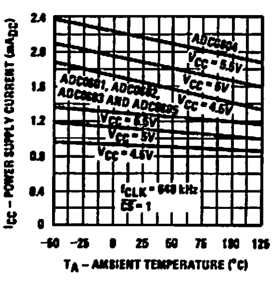
DS005671-43

Output Current vs Temperature



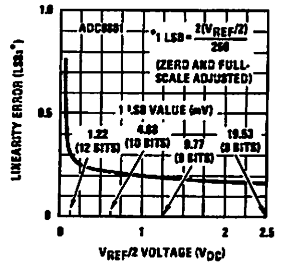
DS005671-44

Power Supply Current vs Temperature (Note 9)



DS005671-45

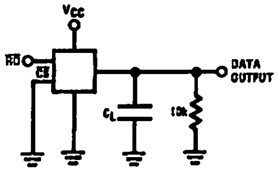
Linearity Error at Low $V_{REF}/2$ Voltages



DS005671-46

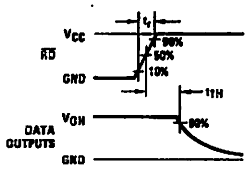
TRI-STATE Test Circuits and Waveforms

t_{1H}



DS005671-47

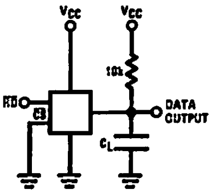
t_{1H}, C_L=10 pF



DS005671-48

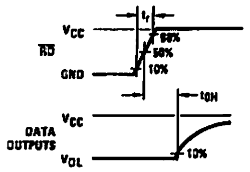
t_r=20 ns

t_{0H}



DS005671-49

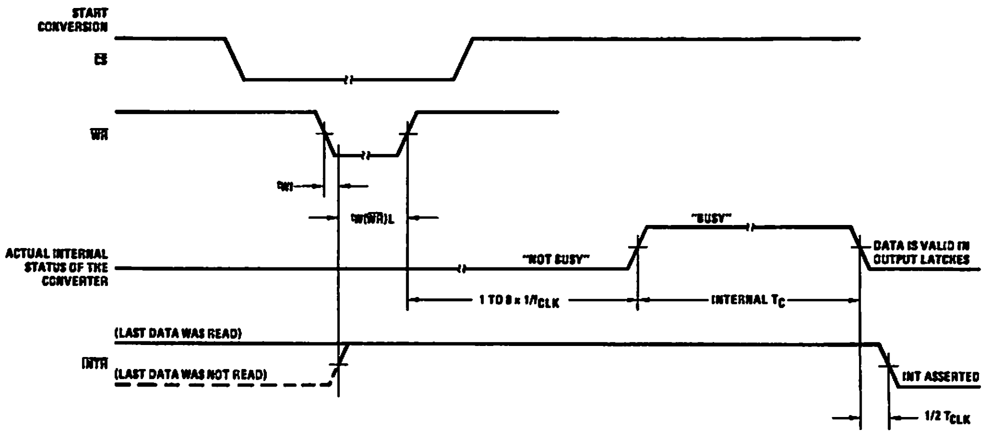
t_{0H}, C_L=10 pF



DS005671-50

t_r=20 ns

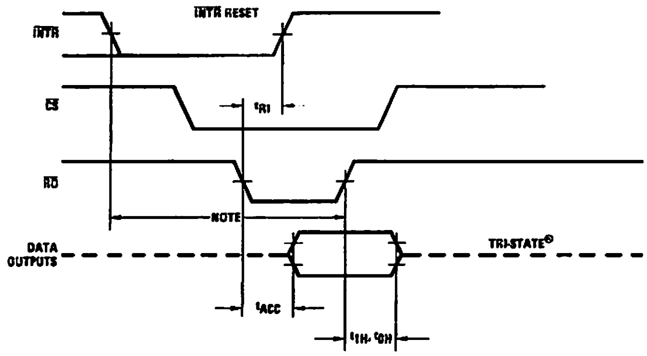
Timing Diagrams (All timing is measured from the 50% voltage points)



DS005671-51

Timing Diagrams (All timing is measured from the 50% voltage points) (Continued)

Output Enable and Reset with $\overline{INTR}$

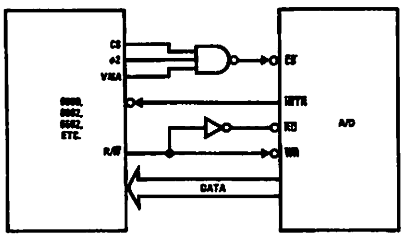


DS005671-52

Note: Read strobe must occur 8 clock periods ($8/f_{CLK}$) after assertion of interrupt to guarantee reset of $\overline{INTR}$.

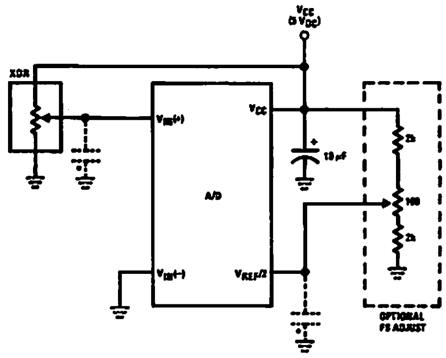
Typical Applications

6800 Interface



DS005671-53

Ratiometeric with Full-Scale Adjust

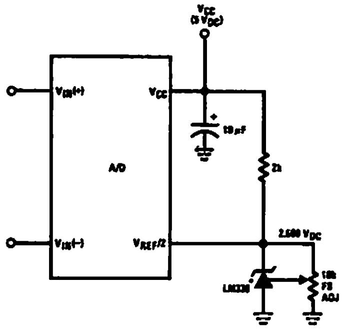


DS005671-54

Note: before using caps at V_{IN} or $V_{REF}/2$, see section 2.3.2 Input Bypass Capacitors.

Typical Applications (Continued)

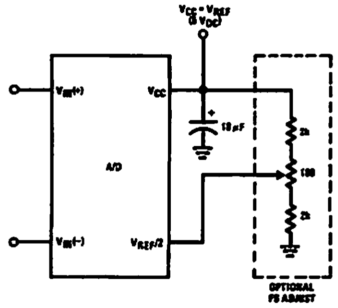
Absolute with a 2.500V Reference



DS005671-55

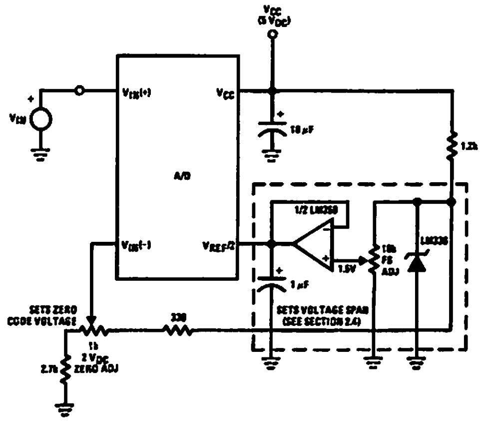
*For low power, see also LM385–2.5

Absolute with a 5V Reference



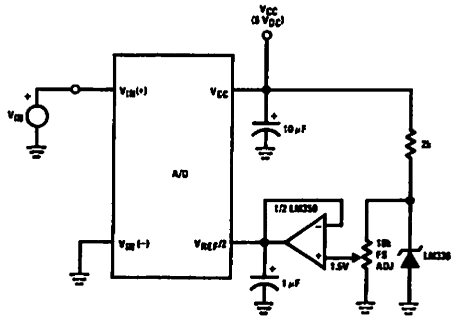
DS005671-56

Zero-Shift and Span Adjust: 2V ≤ V_{IN} ≤ 5V



DS005671-57

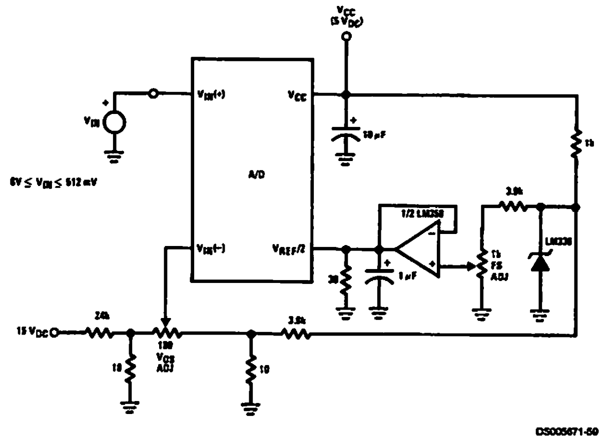
Span Adjust: 0V ≤ V_{IN} ≤ 3V



DS005671-58

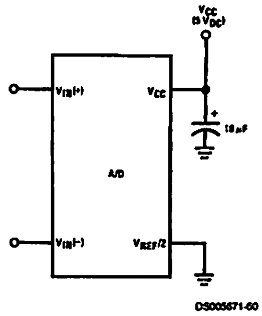
Typical Applications (Continued)

Directly Converting a Low-Level Signal



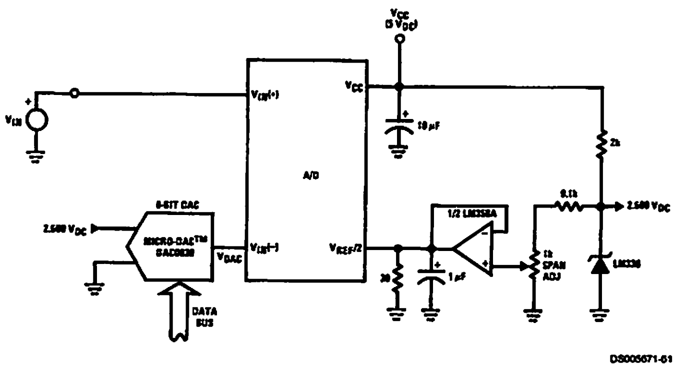
$V_{REF}/2=256$ mV

A µP Interfaced Comparator



For:
$V_{IN}(+)>V_{IN}(-)$
Output=FF_{HEX}
For:
$V_{IN}(+)<V_{IN}(-)$
Output=00_{HEX}

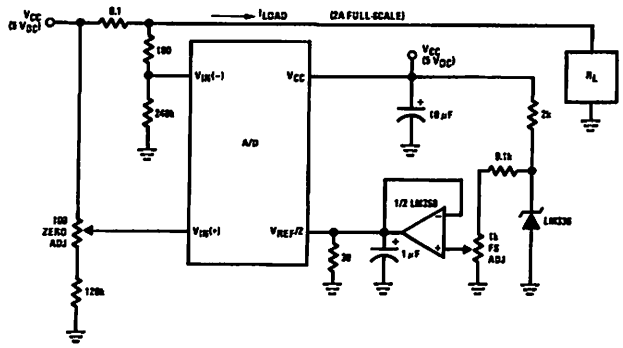
1 mV Resolution with µP Controlled Range



$V_{REF}/2=128$ mV
1 LSB=1 mV
$V_{DAC}\le V_{IN}\le(V_{DAC}+256$ mV)
$0\le V_{DAC}<2.5$V

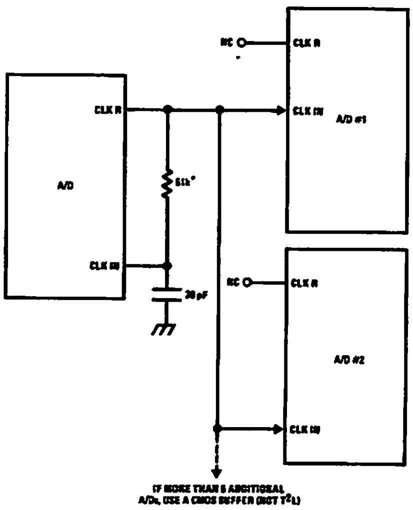
Typical Applications (Continued)

Digitizing a Current Flow



DS005671-62

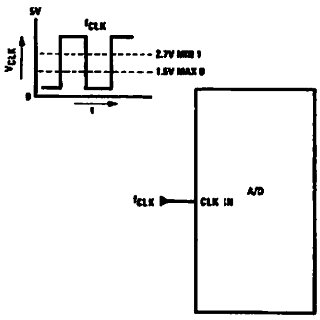
Self-Clocking Multiple A/Ds



DS005671-63

* Use a large R value to reduce loading at CLK R output.

External Clocking

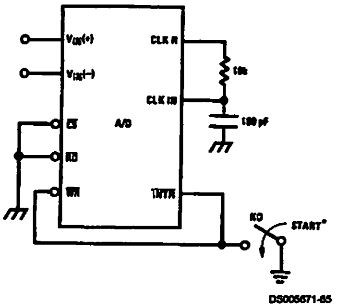


DS005671-64

100 kHz≤f_{CLK}≤1460 kHz

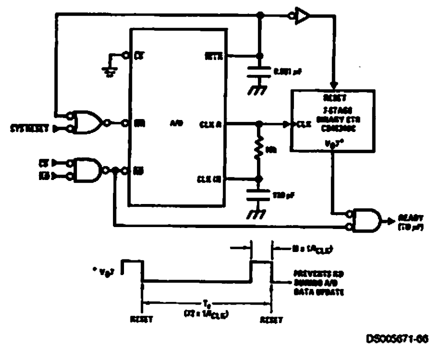
Typical Applications (Continued)

Self-Clocking in Free-Running Mode

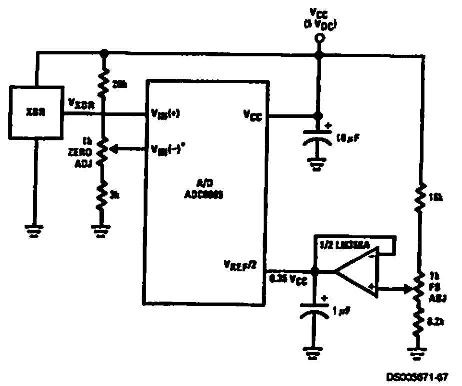


*After power-up, a momentary grounding of the $\overline{WR}$ input is needed to guarantee operation.

µP Interface for Free-Running A/D



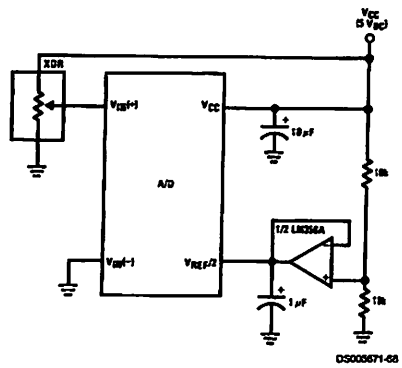
Operating with "Automotive" Ratiometric Transducers



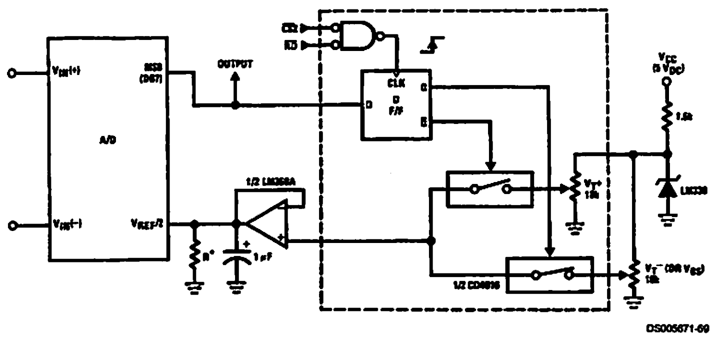
*$V_{IN}(-)=0.15\ V_{CC}$

15% of $V_{CC} \le V_{XDR} \le 85\%$ of V_{CC}

Ratiometric with $V_{REF}/2$ Forced



µP Compatible Differential-Input Comparator with Pre-Set V_{OS} (with or without Hysteresis)



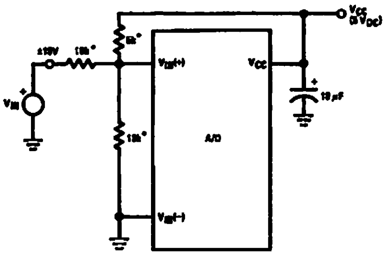
*See *Figure 5* to select R value

DB7="1" for $V_{IN}(+)>V_{IN}(-)+(V_{REF}/2)$

Omit circuitry within the dotted area if hysteresis is not needed

Typical Applications (Continued)

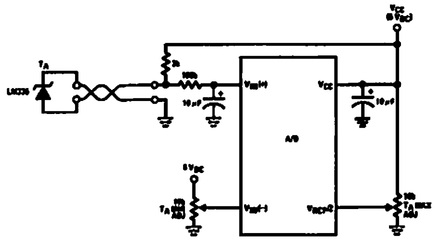
Handling ±10V Analog Inputs



DS005671-70

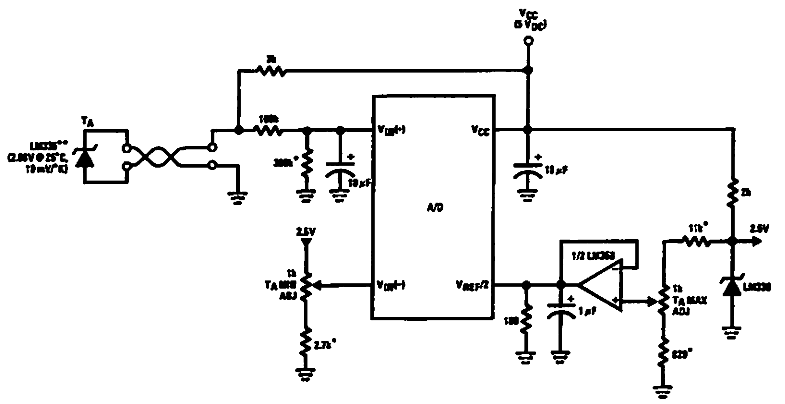
*Beckman Instruments #694-3-R10K resistor array

Low-Cost, µP Interfaced, Temperature-to-Digital Converter



DS005671-71

µP Interfaced Temperature-to-Digital Converter



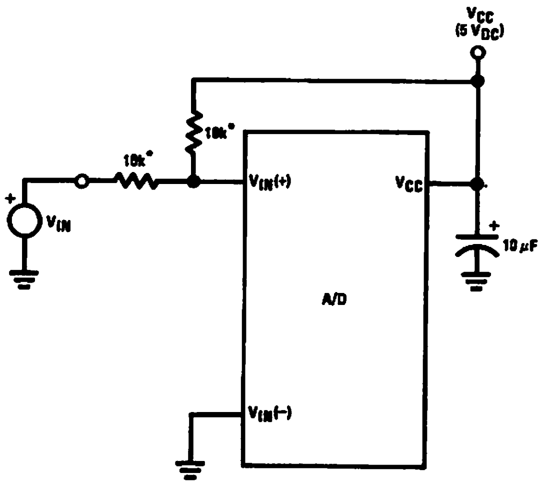
DS005671-72

*Circuit values shown are for 0°C≤T_A≤+128°C

***Can calibrate each sensor to allow easy replacement, then A/D can be calibrated with a pre-set input voltage.

Typical Applications (Continued)

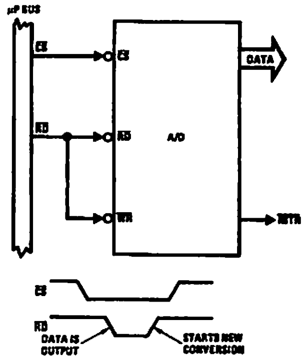
Handling ±5V Analog Inputs



DS005671-33

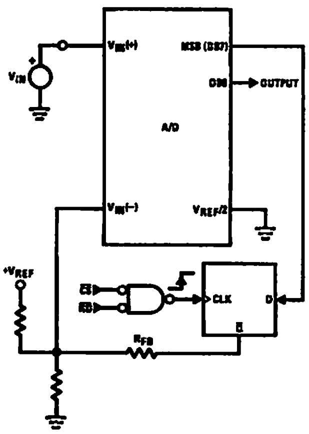
*Beckman Instruments #694-3-R10K resistor array

Read-Only Interface



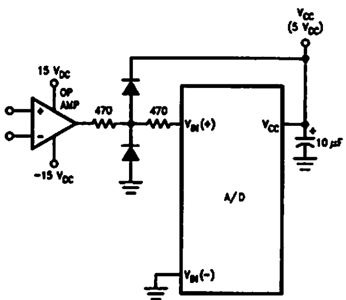
DS005671-34

µP Interfaced Comparator with Hysteresis



DS005671-35

Protecting the Input

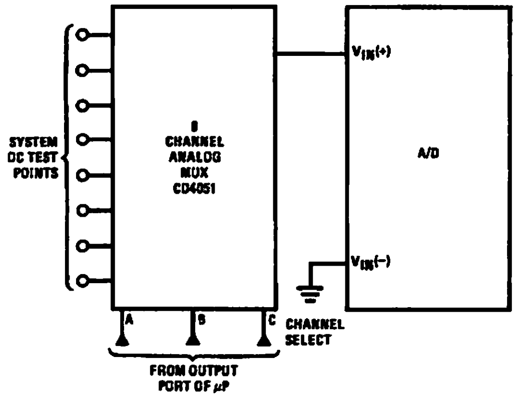


DS005671-9

Diodes are 1N914

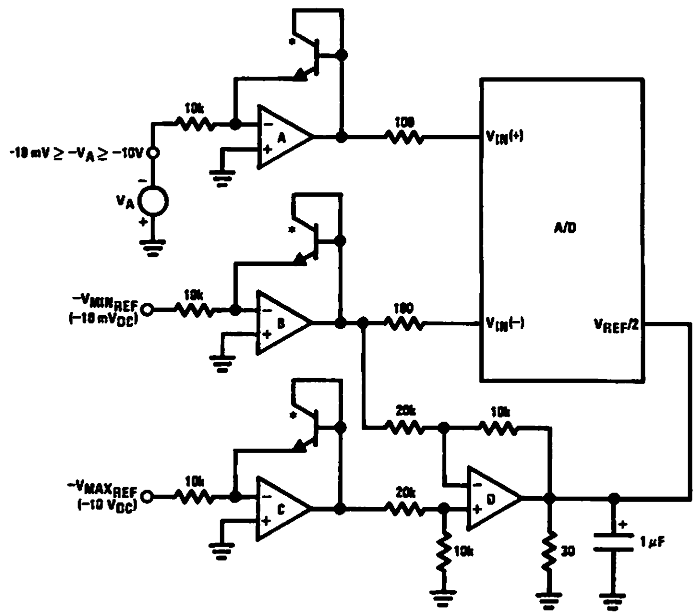
Typical Applications (Continued)

Analog Self-Test for a System



DS005671-36

A Low-Cost, 3-Decade Logarithmic Converter

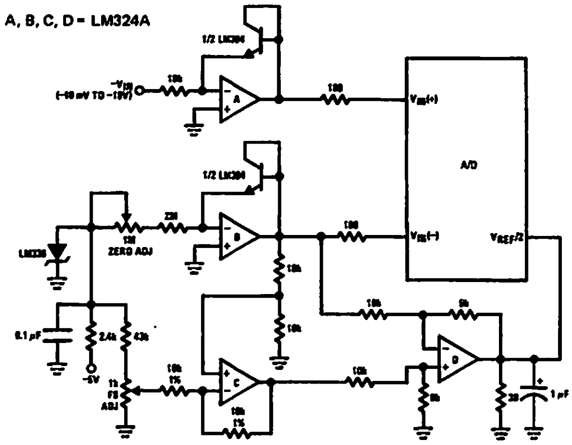


DS005671-37

*LM389 transistors
A, B, C, D = LM324A quad op amp

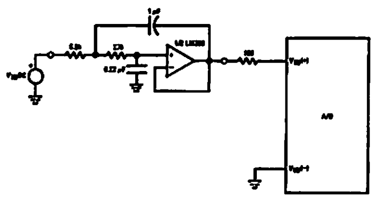
Typical Applications (Continued)

3-Decade Logarithmic A/D Converter



DS005671-73

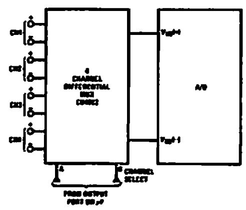
Noise Filtering the Analog Input



DS005671-74

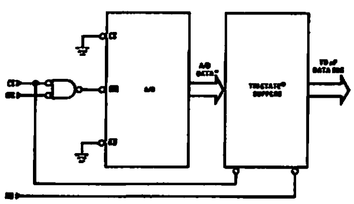
f_C=20 Hz
Uses Chebyshev implementation for steeper roll-off unity-gain, 2nd order, low-pass filter
Adding a separate filter for each channel increases system response time if an analog multiplexer is used

Multiplexing Differential Inputs



DS005671-75

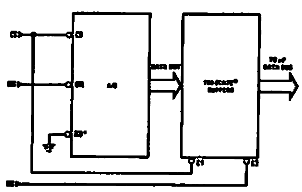
Output Buffers with A/D Data Enabled



DS005671-76

*A/D output data is updated 1 CLK period prior to assertion of $\overline{INTR}$

Increasing Bus Drive and/or Reducing Time on Bus

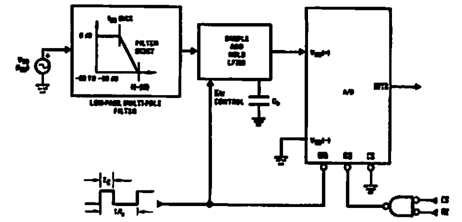


DS005671-77

*Allows output data to set-up at falling edge of $\overline{CS}$

Typical Applications (Continued)

Sampling an AC Input Signal

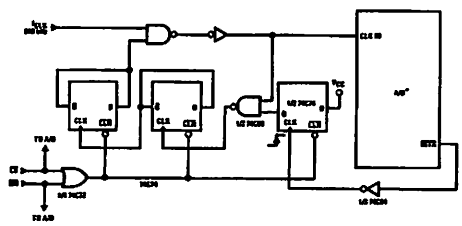


DS005671-78

Note 11: Oversample whenever possible [keep fs > 2f(−60)] to eliminate input frequency folding (aliasing) and to allow for the skirt response of the filter.

Note 12: Consider the amplitude errors which are introduced within the passband of the filter.

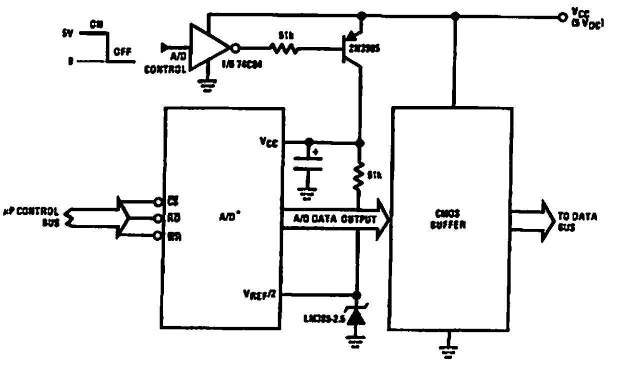
70% Power Savings by Clock Gating



DS005671-79

(Complete shutdown takes ≈ 30 seconds.)

Power Savings by A/D and V_{REF} Shutdown



DS005671-80

*Use ADC0801, 02, 03 or 05 for lowest power consumption.
Note: Logic inputs can be driven to V_{CC} with A/D supply at zero volts.
Buffer prevents data bus from overdriving output of A/D when in shutdown mode.

Functional Description

1.0 UNDERSTANDING A/D ERROR SPECS

A perfect A/D transfer characteristic (staircase waveform) is shown in *Figure 1*. The horizontal scale is analog input voltage and the particular points labeled are in steps of 1 LSB (19.53 mV with 2.5V tied to the $V_{REF}/2$ pin). The digital output codes that correspond to these inputs are shown as D−1, D, and D+1. For the perfect A/D, not only will center-value (A−1, A, A+1, ...) analog inputs produce the correct output digital codes, but also each riser (the transitions between adjacent output codes) will be located ±½ LSB away from each center-value. As shown, the risers are ideal and have no width. Correct digital output codes will be provided for a range of analog input voltages that extend ±½ LSB from the ideal center-values. Each tread (the range of analog input voltage that provides the same digital output code) is therefore 1 LSB wide.

Functional Description (Continued)

Figure 2 shows a worst case error plot for the ADC0801. All center-valued inputs are guaranteed to produce the correct output codes and the adjacent risers are guaranteed to be no closer to the center-value points than ±¼ LSB. In other words, if we apply an analog input equal to the center-value ±¼ LSB, *we guarantee* that the A/D will produce the correct digital code. The maximum range of the position of the code transition is indicated by the horizontal arrow and it is guaranteed to be no more than ½ LSB.

The error curve of *Figure 3* shows a worst case error plot for the ADC0802. Here we guarantee that if we apply an analog input equal to the LSB analog voltage center-value the A/D will produce the correct digital code.

Next to each transfer function is shown the corresponding error plot. Many people may be more familiar with error plots than transfer functions. The analog input voltage to the A/D is provided by either a linear ramp or by the discrete output steps of a high resolution DAC. Notice that the error is continuously displayed and includes the quantization uncertainty of the A/D. For example the error at point 1 of *Figure 1* is +½ LSB because the digital code appeared ½ LSB in advance of the center-value of the tread. The error plots always have a constant negative slope and the abrupt upside steps are always 1 LSB in magnitude.

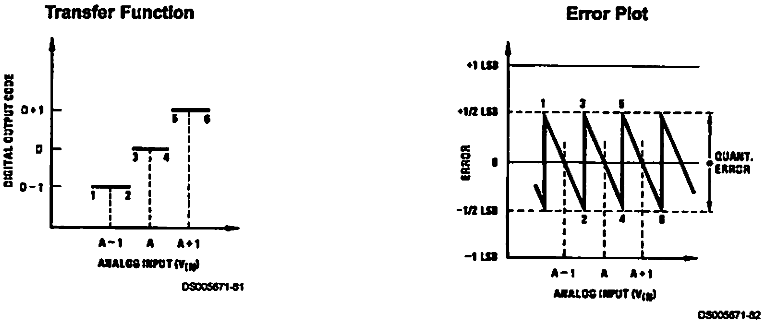


FIGURE 1. Clarifying the Error Specs of an A/D Converter Accuracy=±0 LSB: A Perfect A/D

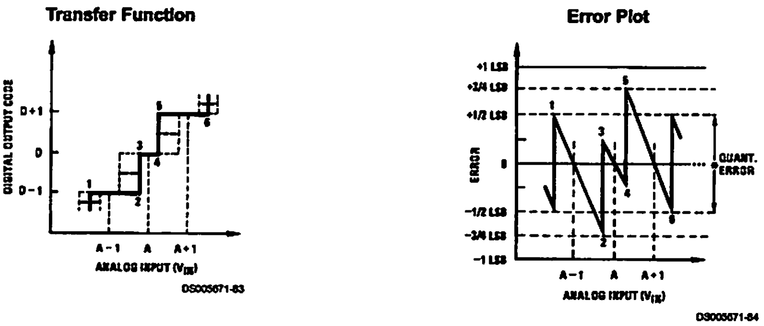
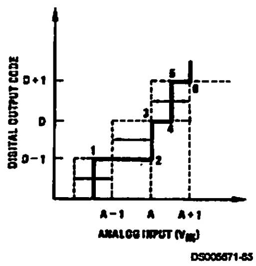


FIGURE 2. Clarifying the Error Specs of an A/D Converter Accuracy=±¼ LSB

Functional Description (Continued)

Transfer Function



Error Plot

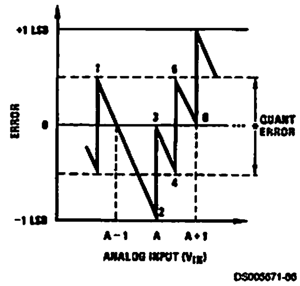


FIGURE 3. Clarifying the Error Specs of an A/D Converter Accuracy=±½ LSB

2.0 FUNCTIONAL DESCRIPTION

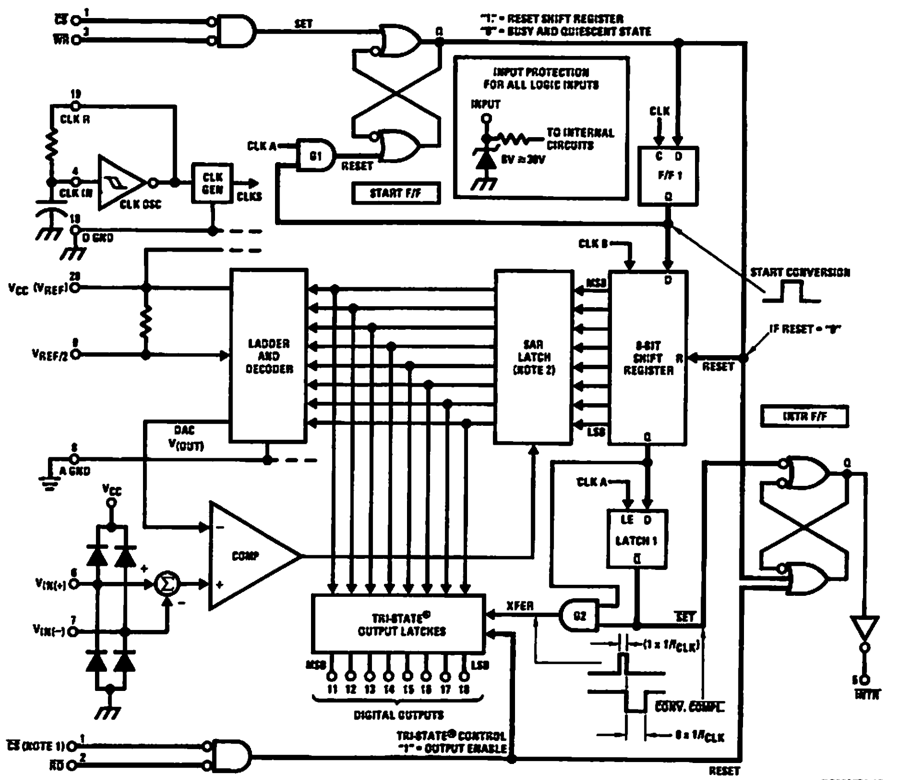
The ADC0801 series contains a circuit equivalent of the 256R network. Analog switches are sequenced by successive approximation logic to match the analog difference input voltage [$V_{IN}(+) - V_{IN}(-)$] to a corresponding tap on the R network. The most significant bit is tested first and after 8 comparisons (64 clock cycles) a digital 8-bit binary code (1111 1111 = full-scale) is transferred to an output latch and then an interrupt is asserted ($\overline{INTR}$ makes a high-to-low transition). A conversion in process can be interrupted by issuing a second start command. The device may be operated in the free-running mode by connecting $\overline{INTR}$ to the $\overline{WR}$ input with $\overline{CS}$ =0. To ensure start-up under all possible conditions, an external $\overline{WR}$ pulse is required during the first power-up cycle.

On the high-to-low transition of the $\overline{WR}$ input the internal SAR latches and the shift register stages are reset. As long as the $\overline{CS}$ input and $\overline{WR}$ input remain low, the A/D will remain in a reset state. *Conversion will start from 1 to 8 clock periods after at least one of these inputs makes a low-to-high transition.*

A functional diagram of the A/D converter is shown in *Figure 4*. All of the package pinouts are shown and the major logic control paths are drawn in heavier weight lines.

The converter is started by having $\overline{CS}$ and $\overline{WR}$ simultaneously low. This sets the start flip-flop (F/F) and the resulting "1" level resets the 8-bit shift register, resets the Interrupt (INTR) F/F and inputs a "1" to the D flop, F/F1, which is at the input end of the 8-bit shift register. Internal clock signals then transfer this "1" to the Q output of F/F1. The AND gate, G1, combines this "1" output with a clock signal to provide a reset signal to the start F/F. If the set signal is no longer present (either $\overline{WR}$ or $\overline{CS}$ is a "1") the start F/F is reset and the 8-bit shift register then can have the "1" clocked in, which starts the conversion process. If the set signal were to still be present, this reset pulse would have no effect (both outputs of the start F/F would momentarily be at a "1" level) and the 8-bit shift register would continue to be held in the reset mode. This logic therefore allows for wide $\overline{CS}$ and $\overline{WR}$ signals and the converter will start after at least one of these signals returns high and the internal clocks again provide a reset signal for the start F/F.

Functional Description (Continued)



Note 13: $\overline{CS}$ shown twice for clarity.

Note 14: SAR = Successive Approximation Register.

FIGURE 4. Block Diagram

After the "1" is clocked through the 8-bit shift register (which completes the SAR search) it appears as the input to the D-type latch, LATCH 1. As soon as this "1" is output from the shift register, the AND gate, G2, causes the new digital word to transfer to the TRI-STATE output latches. When LATCH 1 is subsequently enabled, the Q output makes a high-to-low transition which causes the INTR F/F to set. An inverting buffer then supplies the $\overline{INTR}$ input signal.

Note that this $\overline{SET}$ control of the INTR F/F remains low for 8 of the external clock periods (as the internal clocks run at ⅛ of the frequency of the external clock). If the data output is continuously enabled ($\overline{CS}$ and $\overline{RD}$ both held low), the $\overline{INTR}$ output will still signal the end of conversion (by a high-to-low transition), because the $\overline{SET}$ input can control the Q output of the INTR F/F even though the RESET input is constantly at a "1" level in this operating mode. This $\overline{INTR}$ output will therefore stay low for the duration of the $\overline{SET}$ signal, which is 8 periods of the external clock frequency (assuming the A/D is not started during this interval).

When operating in the free-running or continuous conversion mode ($\overline{INTR}$ pin tied to $\overline{WR}$ and $\overline{CS}$ wired low—see also section 2.8), the START F/F is SET by the high-to-low transition of the $\overline{INTR}$ signal. This resets the SHIFT REGISTER which causes the input to the D-type latch, LATCH 1, to go low. As the latch enable input is still present, the $\overline{Q}$ output will go high, which then allows the INTR F/F to be RESET. This reduces the width of the resulting $\overline{INTR}$ output pulse to only a few propagation delays (approximately 300 ns).

When data is to be read, the combination of both $\overline{CS}$ and $\overline{RD}$ being low will cause the INTR F/F to be reset and the TRI-STATE output latches will be enabled to provide the 8-bit digital outputs.

2.1 Digital Control Inputs

The digital control inputs ($\overline{CS}$, $\overline{RD}$, and $\overline{WR}$) meet standard T^2L logic voltage levels. These signals have been renamed when compared to the standard A/D Start and Output Enable labels. In addition, these inputs are active low to allow an easy interface to microprocessor control busses. For non-microprocessor based applications, the $\overline{CS}$ input (pin 1) can be grounded and the standard A/D Start function is obtained by an active low pulse applied at the $\overline{WR}$ input (pin 3) and the Output Enable function is caused by an active low pulse at the $\overline{RD}$ input (pin 2).

Functional Description (Continued)

2.2 Analog Differential Voltage Inputs and Common-Mode Rejection

This A/D has additional applications flexibility due to the analog differential voltage input. The $V_{IN}(-)$ input (pin 7) can be used to automatically subtract a fixed voltage value from the input reading (tare correction). This is also useful in 4 mA–20 mA current loop conversion. In addition, common-mode noise can be reduced by use of the differential input.

The time interval between sampling $V_{IN}(+)$ and $V_{IN}(-)$ is 4-½ clock periods. The maximum error voltage due to this slight time difference between the input voltage samples is given by:

$$\Delta V_e(MAX) = (V_P)(2\pi f_{cm})\left(\frac{4.5}{f_{CLK}}\right)$$

where:

ΔV_e is the error voltage due to sampling delay

V_P is the peak value of the common-mode voltage

f_{cm} is the common-mode frequency

As an example, to keep this error to ¼ LSB (~5 mV) when operating with a 60 Hz common-mode frequency, f_{cm}, and using a 640 kHz A/D clock, f_{CLK}, would allow a peak value of the common-mode voltage, V_P, which is given by:

$$V_P = \frac{[\Delta V_{e(MAX)}(f_{CLK})]}{(2\pi f_{cm})(4.5)}$$

or

$$V_P = \frac{(5 \times 10^{-3})(640 \times 10^{3})}{(6.28)(60)(4.5)}$$

which gives

$V_P \cong 1.9V$.

The allowed range of analog input voltages usually places more severe restrictions on input common-mode noise levels.

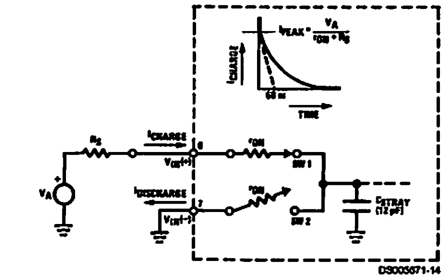
An analog input voltage with a reduced span and a relatively large zero offset can be handled easily by making use of the differential input (see section 2.4 Reference Voltage).

2.3 Analog Inputs

2.3 1 Input Current

Normal Mode

Due to the internal switching action, displacement currents will flow at the analog inputs. This is due to on-chip stray capacitance to ground as shown in *Figure 5.*



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r_{ON} of SW 1 and SW 2 ≅ 5 kΩ

$r = r_{ON}\, C_{STRAY}$ ≅ 5 kΩ x 12 pF = 60 ns

FIGURE 5. Analog Input Impedance

The voltage on this capacitance is switched and will result in currents entering the $V_{IN}(+)$ input pin and leaving the $V_{IN}(-)$ input which will depend on the analog differential input voltage levels. These current transients occur at the leading edge of the internal clocks. They rapidly decay and *do not cause errors* as the on-chip comparator is strobed at the end of the clock period.

Fault Mode

If the voltage source applied to the $V_{IN}(+)$ or $V_{IN}(-)$ pin exceeds the allowed operating range of V_{CC}+50 mV, large input currents can flow through a parasitic diode to the V_{CC} pin. If these currents can exceed the 1 mA max allowed spec, an external diode (1N914) should be added to bypass this current to the V_{CC} pin (with the current bypassed with this diode, the voltage at the $V_{IN}(+)$ pin can exceed the V_{CC} voltage by the forward voltage of this diode).

2.3.2 Input Bypass Capacitors

Bypass capacitors at the inputs will average these charges and cause a DC current to flow through the output resistances of the analog signal sources. This charge pumping action is worse for continuous conversions with the $V_{IN}(+)$ input voltage at full-scale. For continuous conversions with a 640 kHz clock frequency with the $V_{IN}(+)$ input at 5V, this DC current is at a maximum of approximately 5 µA. Therefore, ***bypass capacitors should not be used at the analog inputs or the $V_{REF}/2$ pin*** for high resistance sources (> 1 kΩ). If input bypass capacitors are necessary for noise filtering and high source resistance is desirable to minimize capacitor size, the detrimental effects of the voltage drop across this input resistance, which is due to the average value of the input current, can be eliminated with a full-scale adjustment while the given source resistor and input bypass capacitor are both in place. This is possible because the average value of the input current is a precise linear function of the differential input voltage.

2.3.3 Input Source Resistance

Large values of source resistance where an input bypass capacitor is not used, *will not cause errors* as the input currents settle out prior to the comparison time. If a low pass filter is required in the system, use a low valued series resistor (≤ 1 kΩ) for a passive RC section or add an op amp RC active low pass filter. For low source resistance applications, (≤ 1 kΩ), a 0.1 µF bypass capacitor at the inputs will prevent noise pickup due to series lead inductance of a long wire. A

Functional Description (Continued)

100Ω series resistor can be used to isolate this capacitor—both the R and C are placed outside the feedback loop—from the output of an op amp, if used.

2.3.4 Noise

The leads to the analog inputs (pins 6 and 7) should be kept as short as possible to minimize input noise coupling. Both noise and undesired digital clock coupling to these inputs can cause system errors. The source resistance for these inputs should, in general, be kept below 5 kΩ. Larger values of source resistance can cause undesired system noise pickup. Input bypass capacitors, placed from the analog inputs to ground, will eliminate system noise pickup but can create analog scale errors as these capacitors will average the transient input switching currents of the A/D (see section 2.3.1.). This scale error depends on both a large source resistance and the use of an input bypass capacitor. This error can be eliminated by doing a full-scale adjustment of the A/D (adjust $V_{REF}/2$ for a proper full-scale reading—see section 2.5.2 on Full-Scale Adjustment) with the source resistance and input bypass capacitor in place.

2.4 Reference Voltage

2.4.1 Span Adjust

For maximum applications flexibility, these A/Ds have been designed to accommodate a 5 V_{DC}, 2.5 V_{DC} or an adjusted voltage reference. This has been achieved in the design of the IC as shown in *Figure 6*.

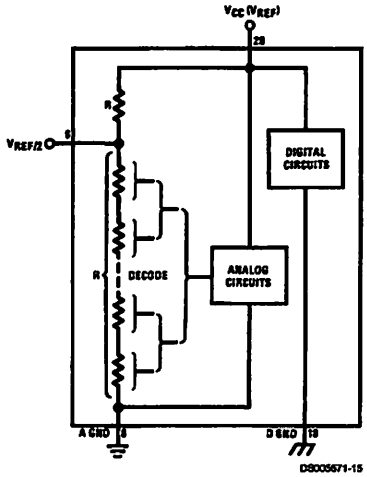


FIGURE 6. The $V_{REFERENCE}$ Design on the IC

Notice that the reference voltage for the IC is either ½ of the voltage applied to the V_{CC} supply pin, or is equal to the voltage that is externally forced at the $V_{REF}/2$ pin. This allows for a ratiometric voltage reference using the V_{CC} supply, a 5 V_{DC} reference voltage can be used for the V_{CC} supply or a voltage less than 2.5 V_{DC} can be applied to the $V_{REF}/2$ input for increased application flexibility. The internal gain to the $V_{REF}/2$ input is 2, making the full-scale differential input voltage twice the voltage at pin 9.

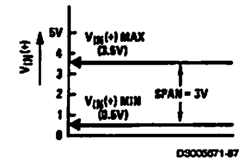
An example of the use of an adjusted reference voltage is to accommodate a reduced span—or dynamic voltage range of the analog input voltage. If the analog input voltage were to range from 0.5 V_{DC} to 3.5 V_{DC}, instead of 0V to 5 V_{DC}, the span would be 3V as shown in *Figure 7*. With 0.5 V_{DC} applied to the $V_{IN}(-)$ pin to absorb the offset, the reference voltage can be made equal to ½ of the 3V span or 1.5 V_{DC}. The A/D now will encode the $V_{IN}(+)$ signal from 0.5V to 3.5 V with the 0.5V input corresponding to zero and the 3.5 V_{DC} input corresponding to full-scale. The full 8 bits of resolution are therefore applied over this reduced analog input voltage range.

2.4.2 Reference Accuracy Requirements

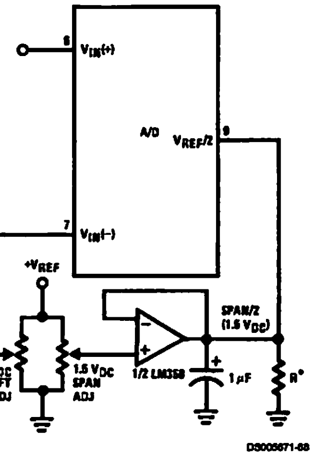
The converter can be operated in a ratiometric mode or an absolute mode. In ratiometric converter applications, the magnitude of the reference voltage is a factor in both the output of the source transducer and the output of the A/D converter and therefore cancels out in the final digital output code. The ADC0805 is specified particularly for use in ratiometric applications with no adjustments required. In absolute conversion applications, both the initial value and the temperature stability of the reference voltage are important factors in the accuracy of the A/D converter. For $V_{REF}/2$ voltages of 2.4 V_{DC} nominal value, initial errors of ±10 mV_{DC} will cause conversion errors of ±1 LSB due to the gain of 2 of the $V_{REF}/2$ input. In reduced span applications, the initial value and the stability of the $V_{REF}/2$ input voltage become even more important. For example, if the span is reduced to 2.5V, the analog input LSB voltage value is correspondingly reduced from 20 mV (5V span) to 10 mV and 1 LSB at the $V_{REF}/2$ input becomes 5 mV. As can be seen, this reduces the allowed initial tolerance of the reference voltage and requires correspondingly less absolute change with temperature variations. Note that spans smaller than 2.5V place even tighter requirements on the initial accuracy and stability of the reference source.

In general, the magnitude of the reference voltage will require an initial adjustment. Errors due to an improper value of reference voltage appear as full-scale errors in the A/D transfer function. IC voltage regulators may be used for references if the ambient temperature changes are not excessive. The LM336B 2.5V IC reference diode (from National Semiconductor) has a temperature stability of 1.8 mV typ (6 mV max) over $0°C \leq T_A \leq +70°C$. Other temperature range parts are also available.

Functional Description (Continued)



a) Analog Input Signal Example



*Add if $V_{REF}/2 \le 1$ V_{DC} with LM358 to draw 3 mA to ground.

b) Accommodating an Analog Input from 0.5V (Digital Out = 00_{HEX}) to 3.5V (Digital Out=FF_{HEX})

FIGURE 7. Adapting the A/D Analog Input Voltages to Match an Arbitrary Input Signal Range

2.5 Errors and Reference Voltage Adjustments

2.5.1 Zero Error

The zero of the A/D does not require adjustment. If the minimum analog input voltage value, $V_{IN(MIN)}$, is not ground, a zero offset can be done. The converter can be made to output 0000 0000 digital code for this minimum input voltage by biasing the A/D $V_{IN}(-)$ input at this $V_{IN(MIN)}$ value (see Applications section). This utilizes the differential mode operation of the A/D.

The zero error of the A/D converter relates to the location of the first riser of the transfer function and can be measured by grounding the V_{IN} (−) input and applying a small magnitude positive voltage to the V_{IN} (+) input. Zero error is the difference between the actual DC input voltage that is necessary to just cause an output digital code transition from 0000 0000 to 0000 0001 and the ideal ½ LSB value (½ LSB = 9.8 mV for $V_{REF}/2$=2.500 V_{DC}).

2.5.2 Full-Scale

The full-scale adjustment can be made by applying a differential input voltage that is 1½ LSB less than the desired analog full-scale voltage range and then adjusting the magnitude of the $V_{REF}/2$ input (pin 9 or the V_{CC} supply if pin 9 is not used) for a digital output code that is just changing from 1111 1110 to 1111 1111.

2.5.3 Adjusting for an Arbitrary Analog Input Voltage Range

If the analog zero voltage of the A/D is shifted away from ground (for example, to accommodate an analog input signal that does not go to ground) this new zero reference should be properly adjusted first. A $V_{IN}(+)$ voltage that equals this desired zero reference plus ½ LSB (where the LSB is calculated for the desired analog span, 1 LSB=analog span/256) is applied to pin 6 and the zero reference voltage at pin 7 should then be adjusted to just obtain the 00_{HEX} to 01_{HEX} code transition.

The full-scale adjustment should then be made (with the proper $V_{IN}(-)$ voltage applied) by forcing a voltage to the $V_{IN}(+)$ input which is given by:

$$V_{IN}(+)\ \text{fs adj} = V_{MAX} - 1.5\left[\frac{(V_{MAX} - V_{MIN})}{256}\right]$$

where:

V_{MAX}=The high end of the analog input range

and

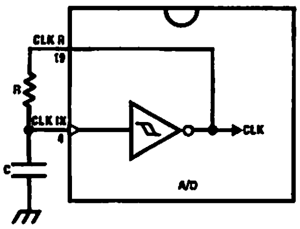
V_{MIN}=the low end (the offset zero) of the analog range. (Both are ground referenced.)

The $V_{REF}/2$ (or V_{CC}) voltage is then adjusted to provide a code change from FE_{HEX} to FF_{HEX}. This completes the adjustment procedure.

2.6 Clocking Option

The clock for the A/D can be derived from the CPU clock or an external RC can be added to provide self-clocking. The CLK IN (pin 4) makes use of a Schmitt trigger as shown in *Figure 8*.

Functional Description (Continued)



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$$f_{CLK} \cong \frac{1}{1.1\,RC}$$

$R \cong 10\ k\Omega$

FIGURE 8. Self-Clocking the A/D

Heavy capacitive or DC loading of the clock R pin should be avoided as this will disturb normal converter operation. Loads less than 50 pF, such as driving up to 7 A/D converter clock inputs from a single clock R pin of 1 converter, are allowed. For larger clock line loading, a CMOS or low power TTL buffer or PNP input logic should be used to minimize the loading on the clock R pin (do not use a standard TTL buffer).

2.7 Restart During a Conversion

If the A/D is restarted ($\overline{CS}$ and $\overline{WR}$ go low and return high) during a conversion, the converter is reset and a new conversion is started. The output data latch is not updated if the conversion in process is not allowed to be completed, therefore the data of the previous conversion remains in this latch. The $\overline{INTR}$ output simply remains at the "1" level.

2.8 Continuous Conversions

For operation in the free-running mode an initializing pulse should be used, following power-up, to ensure circuit operation. In this application, the $\overline{CS}$ input is grounded and the $\overline{WR}$ input is tied to the $\overline{INTR}$ output. This $\overline{WR}$ and $\overline{INTR}$ node should be momentarily forced to logic low following a power-up cycle to guarantee operation.

2.9 Driving the Data Bus

This MOS A/D, like MOS microprocessors and memories, will require a bus driver when the total capacitance of the data bus gets large. Other circuitry, which is tied to the data bus, will add to the total capacitive loading, even in TRI-STATE (high impedance mode). Backplane bussing also greatly adds to the stray capacitance of the data bus.

There are some alternatives available to the designer to handle this problem. Basically, the capacitive loading of the data bus slows down the response time, even though DC specifications are still met. For systems operating with a relatively slow CPU clock frequency, more time is available in which to establish proper logic levels on the bus and therefore higher capacitive loads can be driven (see typical characteristics curves).

At higher CPU clock frequencies time can be extended for I/O reads (and/or writes) by inserting wait states (8080) or using clock extending circuits (6800).

Finally, if time is short and capacitive loading is high, external bus drivers must be used. These can be TRI-STATE buffers (low power Schottky such as the DM74LS240 series is recommended) or special higher drive current products which are designed as bus drivers. High current bipolar bus drivers with PNP inputs are recommended.

2.10 Power Supplies

Noise spikes on the V_{CC} supply line can cause conversion errors as the comparator will respond to this noise. A low inductance tantalum filter capacitor should be used close to the converter V_{CC} pin and values of 1 µF or greater are recommended. If an unregulated voltage is available in the system, a separate LM340LAZ-5.0, TO-92, 5V voltage regulator for the converter (and other analog circuitry) will greatly reduce digital noise on the V_{CC} supply.

2.11 Wiring and Hook-Up Precautions

Standard digital wire wrap sockets are not satisfactory for breadboarding this A/D converter. Sockets on PC boards can be used and all logic signal wires and leads should be grouped and kept as far away as possible from the analog signal leads. Exposed leads to the analog inputs can cause undesired digital noise and hum pickup, therefore shielded leads may be necessary in many applications.

A single point analog ground that is separate from the logic ground points should be used. The power supply bypass capacitor and the self-clocking capacitor (if used) should both be returned to digital ground. Any $V_{REF}/2$ bypass capacitors, analog input filter capacitors, or input signal shielding should be returned to the analog ground point. A test for proper grounding is to measure the zero error of the A/D converter. Zero errors in excess of ¼ LSB can usually be traced to improper board layout and wiring (see section 2.5.1 for measuring the zero error).

3.0 TESTING THE A/D CONVERTER

There are many degrees of complexity associated with testing an A/D converter. One of the simplest tests is to apply a known analog input voltage to the converter and use LEDs to display the resulting digital output code as shown in *Figure 9*.

For ease of testing, the $V_{REF}/2$ (pin 9) should be supplied with 2.560 V_{DC} and a V_{CC} supply voltage of 5.12 V_{DC} should be used. This provides an LSB value of 20 mV.

If a full-scale adjustment is to be made, an analog input voltage of 5.090 V_{DC} (5.120–1½ LSB) should be applied to the $V_{IN}(+)$ pin with the $V_{IN}(-)$ pin grounded. The value of the $V_{REF}/2$ input voltage should then be adjusted until the digital output code is just changing from 1111 1110 to 1111 1111. This value of $V_{REF}/2$ should then be used for all the tests.

The digital output LED display can be decoded by dividing the 8 bits into 2 hex characters, the 4 most significant (MS) and the 4 least significant (LS). *Table 1* shows the fractional binary equivalent of these two 4-bit groups. By adding the voltages obtained from the "VMS" and "VLS" columns in *Table 1*, the nominal value of the digital display (when $V_{REF}/2$ = 2.560V) can be determined. For example, for an output LED display of 1011 0110 or B6 (in hex), the voltage values from the table are 3.520 + 0.120 or 3.640 V_{DC}. These voltage values represent the center-values of a perfect A/D converter. The effects of quantization error have to be accounted for in the interpretation of the test results.

Functional Description (Continued)

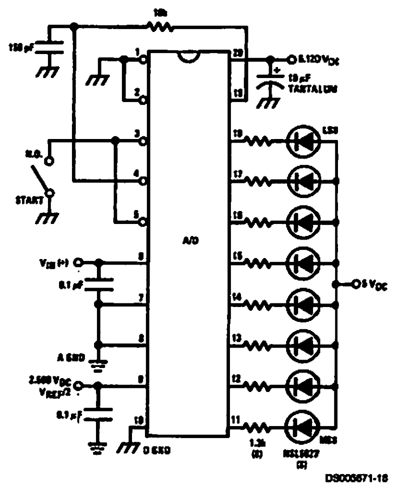

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FIGURE 9. Basic A/D Tester

For a higher speed test system, or to obtain plotted data, a digital-to-analog converter is needed for the test set-up. An accurate 10-bit DAC can serve as the precision voltage source for the A/D. Errors of the A/D under test can be expressed as either analog voltages or differences in 2 digital words.

A basic A/D tester that uses a DAC and provides the error as an analog output voltage is shown in *Figure 8*. The 2 op amps can be eliminated if a lab DVM with a numerical subtraction feature is available to read the difference voltage, "A–C", directly. The analog input voltage can be supplied by a low frequency ramp generator and an X-Y plotter can be used to provide analog error (Y axis) versus analog input (X axis).

For operation with a microprocessor or a computer-based test system, it is more convenient to present the errors digitally. This can be done with the circuit of *Figure 11*, where the output code transitions can be detected as the 10-bit DAC is incremented. This provides ¼ LSB steps for the 8-bit A/D under test. If the results of this test are automatically plotted with the analog input on the X axis and the error (in LSB's) as the Y axis, a useful transfer function of the A/D under test results. For acceptance testing, the plot is not necessary and the testing speed can be increased by establishing internal limits on the allowed error for each code.

4.0 MICROPROCESSOR INTERFACING

To dicuss the interface with 8080A and 6800 microprocessors, a common sample subroutine structure is used. The microprocessor starts the A/D, reads and stores the results of 16 successive conversions, then returns to the user's program. The 16 data bytes are stored in 16 successive memory locations. All Data and Addresses will be given in hexadecimal form. Software and hardware details are provided separately for each type of microprocessor.

4.1 Interfacing 8080 Microprocessor Derivatives (8048, 8085)

This converter has been designed to directly interface with derivatives of the 8080 microprocessor. The A/D can be mapped into memory space (using standard memory address decoding for $\overline{CS}$ and the $\overline{MEMR}$ and $\overline{MEMW}$ strobes) or it can be controlled as an I/O device by using the $\overline{I/O\ R}$ and $\overline{I/O\ W}$ strobes and decoding the address bits A0 → A7 (or address bits A8 → A15 as they will contain the same 8-bit address information) to obtain the $\overline{CS}$ input. Using the I/O space provides 256 additional addresses and may allow a simpler 8-bit address decoder but the data can only be input to the accumulator. To make use of the additional memory reference instructions, the A/D should be mapped into memory space. An example of an A/D in I/O space is shown in *Figure 12*.

Functional Description (Continued)

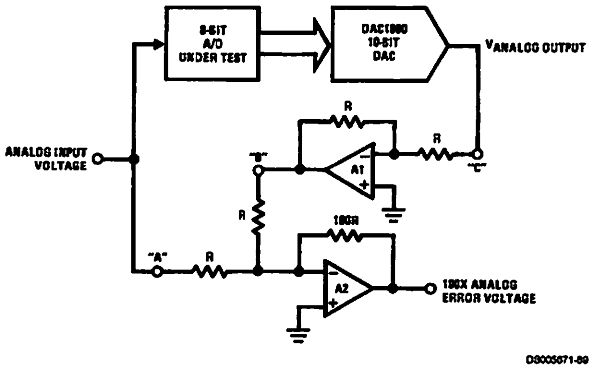


FIGURE 10. A/D Tester with Analog Error Output

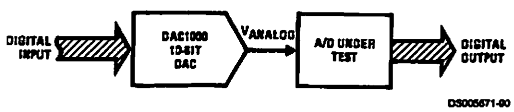


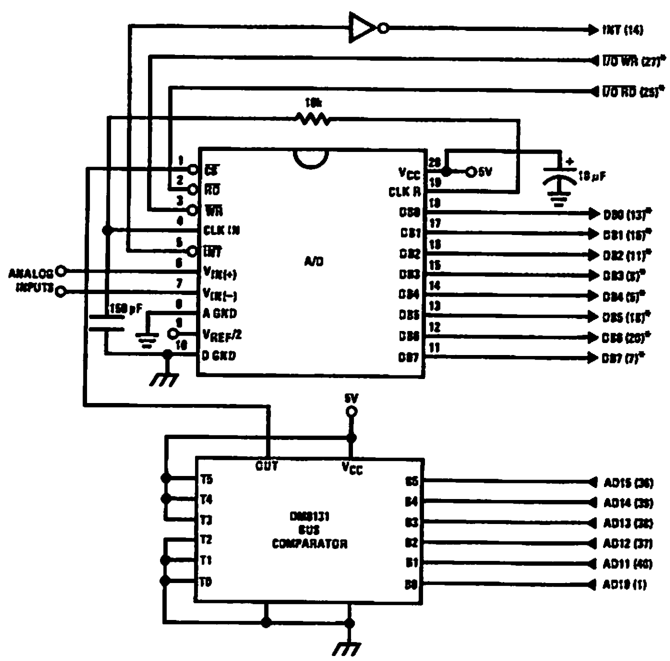
FIGURE 11. Basic "Digital" A/D Tester

TABLE 1. DECODING THE DIGITAL OUTPUT LEDs

HEX	BINARY				FRACTIONAL BINARY VALUE FOR		OUTPUT VOLTAGE CENTER VALUES WITH $V_{REF}/2=2.560\ V_{DC}$	
					MS GROUP	LS GROUP	VMS GROUP (Note 15)	VLS GROUP (Note 15)
F	1	1	1	1	15/16	15/256	4.800	0.300
E	1	1	1	0	7/8	7/128	4.480	0.280
D	1	1	0	1	13/16	13/256	4.160	0.260
C	1	1	0	0	3/4	3/64	3.840	0.240
B	1	0	1	1	11/16	11/256	3.520	0.220
A	1	0	1	0	5/8	5/128	3.200	0.200
9	1	0	0	1	9/16	9/256	2.880	0.180
8	1	0	0	0	1/2	1/32	2.560	0.160
7	0	1	1	1	7/16	7/256	2.240	0.140
6	0	1	1	0	3/8	3/128	1.920	0.120
5	0	1	0	1	5/16	2/256	1.600	0.100
4	0	1	0	0	1/4	1/64	1.280	0.080
3	0	0	1	1	3/16	3/256	0.960	0.060
2	0	0	1	0	1/8	1/128	0.640	0.040
1	0	0	0	1	1/16	1/256	0.320	0.020
0	0	0	0	0			0	0

Note 15: Display Output=VMS Group + VLS Group

Functional Description (Continued)



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Note 16: *Pin numbers for the DP8228 system controller, others are INS8080A.

Note 17: Pin 23 of the INS8228 must be tied to +12V through a 1 kΩ resistor to generate the RST 7 instruction when an interrupt is acknowledged as required by the accompanying sample program.

FIGURE 12. ADC0801_INS8080A CPU Interface

Functional Description (Continued)

SAMPLE PROGRAM FOR *Figure 12* ADC0801–INS8080A CPU INTERFACE

```
0038   C3 00 03   RST 7:               JMP  LD DATA
 •        •         •
 •        •         •
0100   21 00 02   START:               LXI H 0200H     ; HL pair will point to
                                                       ; data storage locations
0103   31 00 04   RETURN:              LXI SP 0400H    ; Initialize stack pointer (Note 1)
0106   7D                              MOV A, L        ; Test # of bytes entered
0107   FE 0F                           CPI 0F H        ; If # = 16. JMP to
0109   CA 13 01                        JZ CONT         ; user program
010C   D3 E0                           OUT E0 H        ; Start A/D
010E   FB                              EI              ; Enable interrupt
010F   00         LOOP:                NOP             ; Loop until end of
0110   C3 0F 01                        JMP LOOP        ; conversion
0113      •       CONT:                 •
 •        •         •                   •
 •        •       (User program to      •
 •        •       process data)         •
 •        •         •                   •
 •        •         •                   •
0300   DB E0      LD DATA:             IN E0 H         ; Load data into accumulator
0302   77                              MOV M, A        ; Store data
0303   23                              INX H           ; Increment storage pointer
0304   C3 03 01                        JMP RETURN
```

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Note 18: The stack pointer must be dimensioned because a RST 7 instruction pushes the PC onto the stack.

Note 19: All address used were arbitrarily chosen.

The standard control bus signals of the 8080 $\overline{CS}$, $\overline{RD}$ and $\overline{WR}$) can be directly wired to the digital control inputs of the A/D and the bus timing requirements are met to allow both starting the converter and outputting the data onto the data bus. A bus driver should be used for larger microprocessor systems where the data bus leaves the PC board and/or must drive capacitive loads larger than 100 pF.

4.1.1 Sample 8080A CPU Interfacing Circuitry and Program

The following sample program and associated hardware shown in *Figure 12* may be used to input data from the converter to the INS8080A CPU chip set (comprised of the INS8080A microprocessor, the INS8228 system controller and the INS8224 clock generator). For simplicity, the A/D is controlled as an I/O device, specifically an 8-bit bi-directional port located at an arbitrarily chosen port address, E0. The TRI-STATE output capability of the A/D eliminates the need for a peripheral interface device, however address decoding is still required to generate the appropriate $\overline{CS}$ for the converter.

It is important to note that in systems where the A/D converter is 1-of-8 or less I/O mapped devices, no address decoding circuitry is necessary. Each of the 8 address bits (A0 to A7) can be directly used as $\overline{CS}$ inputs—one for each I/O device.

4.1.2 INS8048 Interface

The INS8048 interface technique with the ADC0801 series (see *Figure 13*) is simpler than the 8080A CPU interface. There are 24 I/O lines and three test input lines in the 8048. With these extra I/O lines available, one of the I/O lines (bit 0 of port 1) is used as the chip select signal to the A/D, thus eliminating the use of an external address decoder. Bus control signals $\overline{RD}$, $\overline{WR}$ and $\overline{INT}$ of the 8048 are tied directly to the A/D. The 16 converted data words are stored at on-chip RAM locations from 20 to 2F (Hex). The $\overline{RD}$ and $\overline{WR}$ signals are generated by reading from and writing into a dummy address, respectively. A sample interface program is shown below.

Functional Description (Continued)

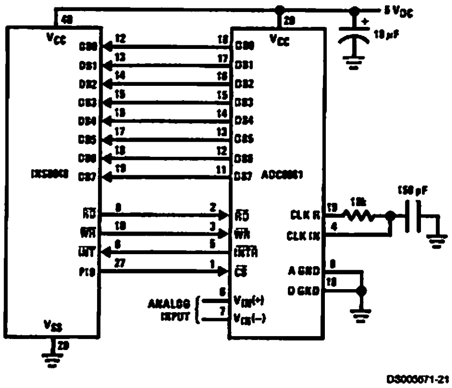

FIGURE 13. INS8048 Interface

SAMPLE PROGRAM FOR *Figure 13* INS8048 INTERFACE

04 10		JMP	10H	; Program starts at addr 10
		ORG	3H	
04 50		JMP	50H	; Interrupt jump vector
		ORG	10H	; Main program
99 FE		ANL	P1, #0FEH	; Chip select
81		MOVX	A, @R1	; Read in the 1st data
				; to reset the intr
89 01	START:	ORL	P1, #1	; Set port pin high
B8 20		MOV	R0, #20H	; Data address
B9 FF		MOV	R1, #0FFH	; Dummy address
BA 10		MOV	R2, #10H	; Counter for 16 bytes
23 FF	AGAIN:	MOV	A, #0FFH	; Set ACC for intr loop
99 FE		ANL	P1, #0FEH	; Send CS (bit 0 of P1)
91		MOVX	@R1, A	; Send WR out
05		EN	I	; Enable interrupt
96 21	LOOP:	JNZ	LOOP	; Wait for interrupt
EA 1B		DJNZ	R2, AGAIN	; If 16 bytes are read
00		NOP		; go to user's program
00		NOP		
		ORG	50H	
81	INDATA:	MOVX	A, @R1	; Input data, CS still low
A0		MOV	@R0, A	; Store in memory
18		INC	R0	; Increment storage counter
89 01		ORL	P1, #1	; Reset CS signal
27		CLR	A	; Clear ACC to get out of
93		RETR		; the interrupt loop

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4.2 Interfacing the Z-80

The Z-80 control bus is slightly different from that of the 8080. General $\overline{RD}$ and $\overline{WR}$ strobes are provided and separate memory request, $\overline{MREQ}$, and I/O request, $\overline{IORQ}$, signals are used which have to be combined with the generalized strobes to provide the equivalent 8080 signals. An advantage of operating the A/D in I/O space with the Z-80 is that the CPU will automatically insert one wait state (the $\overline{RD}$ and $\overline{WR}$ strobes are extended one clock period) to allow more time for the I/O devices to respond. Logic to map the A/D in I/O space is shown in *Figure 14*.

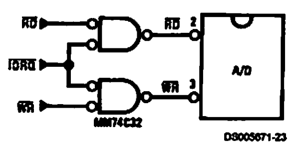


FIGURE 14. Mapping the A/D as an I/O Device for Use with the Z-80 CPU

Additional I/O advantages exist as software DMA routines are available and use can be made of the output data transfer which exists on the upper 8 address lines (A8 to A15) dur-

Functional Description (Continued)

ing I/O input instructions. For example, MUX channel selection for the A/D can be accomplished with this operating mode.

4.3 Interfacing 6800 Microprocessor Derivatives (6502, etc.)

The control bus for the 6800 microprocessor derivatives does not use the $\overline{RD}$ and $\overline{WR}$ strobe signals. Instead it employs a single R/$\overline{W}$ line and additional timing, if needed, can be derived fom the ϕ2 clock. All I/O devices are memory mapped in the 6800 system, and a special signal, VMA, indicates that the current address is valid. *Figure 15* shows an interface schematic where the A/D is memory mapped in the 6800 system. For simplicity, the $\overline{CS}$ decoding is shown using ½ DM8092. Note that in many 6800 systems, an already decoded $\overline{4/5}$ line is brought out to the common bus at pin 21. This can be tied directly to the $\overline{CS}$ pin of the A/D, provided that no other devices are addressed at HX ADDR: 4XXX or 5XXX.

The following subroutine performs essentially the same function as in the case of the 8080A interface and it can be called from anywhere in the user's program.

In *Figure 16* the ADC0801 series is interfaced to the M6800 microprocessor through (the arbitrarily chosen) Port B of the MC6820 or MC6821 Peripheral Interface Adapter, (PIA). Here the $\overline{CS}$ pin of the A/D is grounded since the PIA is already memory mapped in the M6800 system and no $\overline{CS}$ decoding is necessary. Also notice that the A/D output data lines are connected to the microprocessor bus under program control through the PIA and therefore the A/D $\overline{RD}$ pin can be grounded.

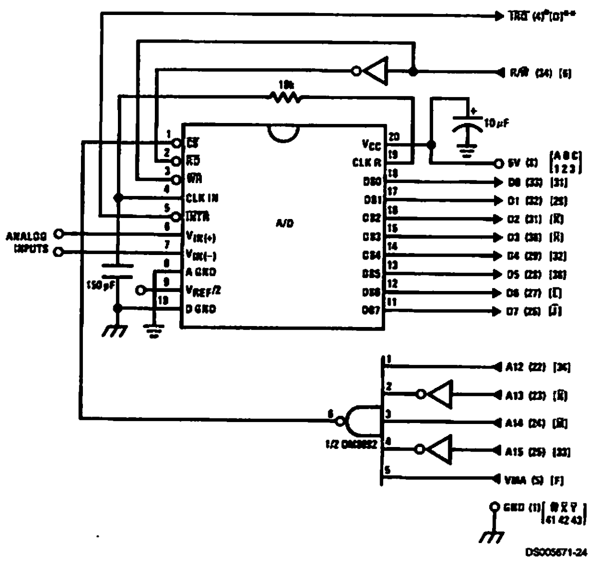
A sample interface program equivalent to the previous one is shown below *Figure 16.* The PIA Data and Control Registers of Port B are located at HEX addresses 8006 and 8007, respectively.

5.0 GENERAL APPLICATIONS

The following applications show some interesting uses for the A/D. The fact that one particular microprocessor is used is not meant to be restrictive. Each of these application circuits would have its counterpart using any microprocessor that is desired.

5.1 Multiple ADC0801 Series to MC6800 CPU Interface

To transfer analog data from several channels to a single microprocessor system, a multiple converter scheme presents several advantages over the conventional multiplexer single-converter approach. With the ADC0801 series, the differential inputs allow individual span adjustment for each channel. Furthermore, all analog input channels are sensed simultaneously, which essentially divides the microprocessor's total system servicing time by the number of channels, since all conversions occur simultaneously. This scheme is shown in *Figure 17.*



Note 20: Numbers in parentheses refer to MC6800 CPU pin out.

Note 21: Number or letters in brackets refer to standard M6800 system common bus code.

FIGURE 15. ADC0801-MC6800 CPU Interface

Functional Description (Continued)

SAMPLE PROGRAM FOR *Figure 15* ADC0801-MC6800 CPU INTERFACE

```
0010  DF 36      DATAIN  STX   TEMP2    ; Save contents of X
0012  CE 00 2C           LDX   #$002C   ; Upon IRQ low CPU
0015  FF FF F8           STX   $FFF8    ; jumps to 002C
0018  B7 50 00           STAA  $5000    ; Start ADC0801
001B  0E                 CLI
001C  3E         CONVRT  WAI            ; Wait for interrupt
001D  DE 34              LDX   TEMP1
001F  8C 02 0F           CPX   #$020F   ; Is final data stored?
0022  27 14              BEQ   ENDP
0024  B7 50 00           STAA  $5000    ; Restarts ADC0801
0027  08                 INX
0028  DF 34              STX   TEMP1
002A  20 F0              BRA   CONVRT
002C  DE 34      INTRPT  LDX   TEMP1
002E  B6 50 00           LDAA  $5000    ; Read data
0031  A7 00              STAA  X        ; Store it at X
0033  3B                 RTI
0034  02 00      TEMP1   FDB   $0200    ; Starting address for
                                        ; data storage
0036  00 00      TEMP2   FDB   $0000
0038  CE 02 00   ENDP    LDX   #$0200   ; Reinitialize TEMP1
003B  DF 34              STX   TEMP1
003D  DE 36              LDX   TEMP2
003F  39                 RTS            ; Return from subroutine
                                        ; To user's program
```

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Note 22: In order for the microprocessor to service subroutines and interrupts, the stack pointer must be dimensioned in the user's program.

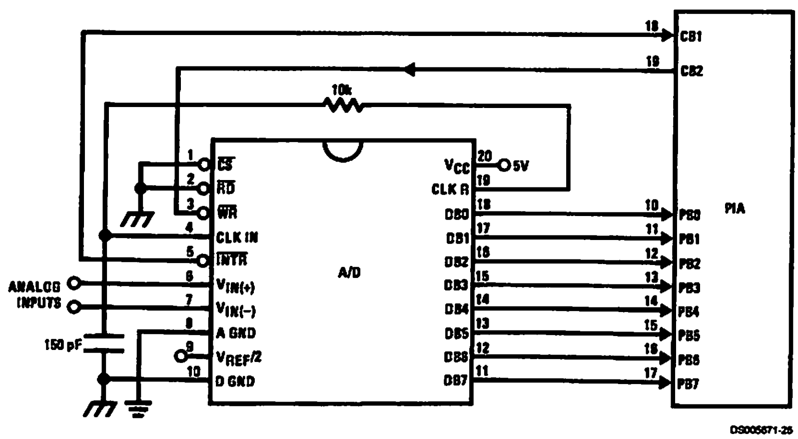

FIGURE 16. ADC0801–MC6820 PIA Interface

Functional Description (Continued)

SAMPLE PROGRAM FOR *Figure 16* ADC0801–MC6820 PIA INTERFACE

```
0010   CE 00 38    DATAIN   LDX    #$0038    ; Upon IRQ low CPU
0013   FF FF F8             STX    $FFF8     ; jumps to 0038
0016   B6 80 06             LDAA   PIAORB    ; Clear possible IRQ flags
0019   4F                   CLRA
001A   B7 80 07             STAA   PIACRB
001D   B7 80 06             STAA   PIAORB    ; Set Port B as input
0020   0E                   CLI
0021   C6 34                LDAB   #$34
0023   86 3D                LDAA   #$3D
0025   F7 80 07    CONVRT   STAB   PIACRB    ; Starts ADC0801
0028   B7 80 07             STAA   PIACRB
002B   3E                   WAI              ; Wait for interrupt
002C   DE 40                LDX    TEMP1
002E   8C 02 0F             CPX    #$020F    ; Is final data stored?
0031   27 0F                BEQ    ENDP
0033   08                   INX
0034   DF 40                STX    TEMP1
0036   20 ED                BRA    CONVRT
0038   DE 40       INTRPT   LDX    TEMP1
003A   B6 80 06             LDAA   PIAORB    ; Read data in
003D   A7 00                STAA   X         ; Store it at X
003F   3B                   RTI
0040   02 00       TEMP1    FDB    $0200     ; Starting address for
                                             ; data storage
0042   CE 02 00    ENDP     LDX    #$0200    ; Reinitialize TEMP1
0045   DF 40                STX    TEMP1
0047   39                   RTS              ; Return from subroutine
                   PIAORB   EQU    $8006     ; To user's program
                   PIACRB   EQU    $8007
```

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The following schematic and sample subroutine (DATA IN) may be used to interface (up to) 8 ADC0801's directly to the MC6800 CPU. This scheme can easily be extended to allow the interface of more converters. In this configuration the converters are (arbitrarily) located at HEX address 5000 in the MC6800 memory space. To save components, the clock signal is derived from just one RC pair on the first converter. This output drives the other A/Ds.

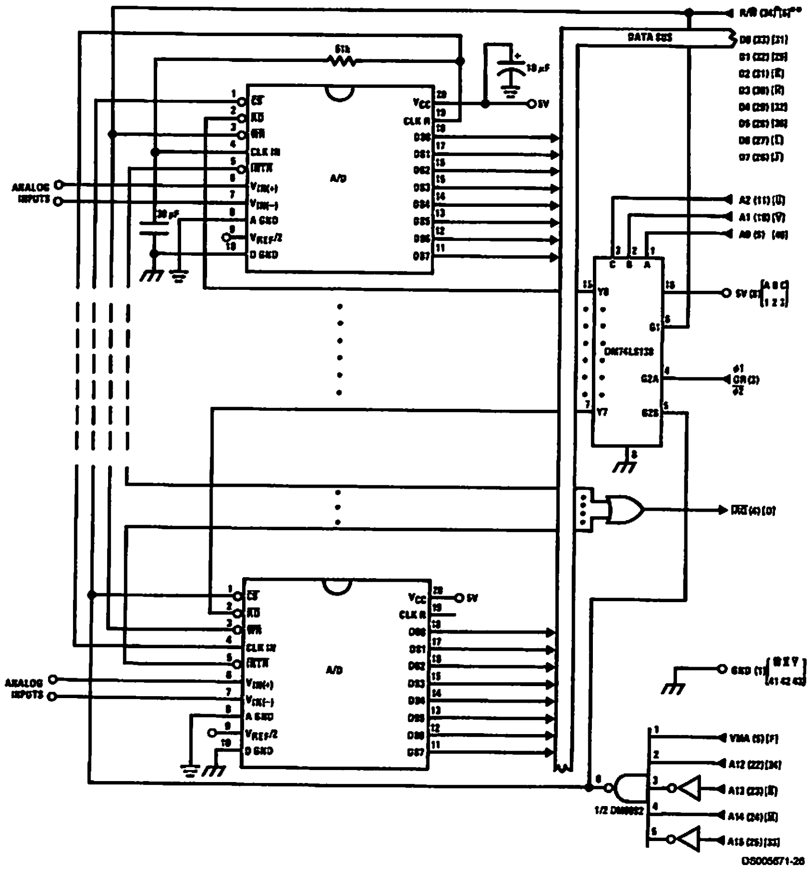
All the converters are started simultaneously with a STORE instruction at HEX address 5000. Note that any other HEX address of the form 5XXX will be decoded by the circuit, pulling all the $\overline{CS}$ inputs low. This can easily be avoided by using a more definitive address decoding scheme. All the interrupts are ORed together to insure that all A/Ds have completed their conversion before the microprocessor is interrupted.

The subroutine, DATA IN, may be called from anywhere in the user's program. Once called, this routine initializes the CPU, starts all the converters simultaneously and waits for the interrupt signal. Upon receiving the interrupt, it reads the converters (from HEX addresses 5000 through 5007) and stores the data successively at (arbitrarily chosen) HEX addresses 0200 to 0207, before returning to the user's program. All CPU registers then recover the original data they had before servicing DATA IN.

5.2 Auto-Zeroed Differential Transducer Amplifier and A/D Converter

The differential inputs of the ADC0801 series eliminate the need to perform a differential to single ended conversion for a differential transducer. Thus, one op amp can be eliminated since the differential to single ended conversion is provided by the differential input of the ADC0801 series. In general, a transducer preamp is required to take advantage of the full A/D converter input dynamic range.

Functional Description (Continued)



Note 23: Numbers in parentheses refer to MC6800 CPU pin out.

Note 24: Numbers of letters in brackets refer to standard M6800 system common bus code.

FIGURE 17. Interfacing Multiple A/Ds in an MC6800 System

Functional Description (Continued)

SAMPLE PROGRAM FOR *Figure 17* INTERFACING MULTIPLE A/D's IN AN MC6800 SYSTEM

ADDRESS	HEX CODE	MNEMONICS			COMMENTS
0010	DF 44	DATAIN	STX	TEMP	; Save Contents of X
0012	CE 00 2A		LDX	#$002A	; Upon $\overline{IRQ}$ LOW CPU
0015	FF FF F8		STX	$FFF8	; Jumps to 002A
0018	B7 50 00		STAA	$5000	; Starts all A/D's
001B	0E		CLI		
001C	3E		WAI		; Wait for interrupt
001D	CE 50 00		LDX	#$5000	
0020	DF 40		STX	INDEX1	; Reset both INDEX
0022	CE 02 00		LDX	#$0200	; 1 and 2 to starting
0025	DF 42		STX	INDEX2	; addresses
0027	DE 44		LDX	TEMP	
0029	39		RTS		; Return from subroutine
002A	DE 40	INTRPT	LDX	INDEX1	; INDEX1 → X
002C	A6 00		LDAA	X	; Read data in from A/D at X
002E	08		INX		; Increment X by one
002F	DF 40		STX	INDEX1	; X → INDEX1
0031	DE 42		LDX	INDEX2	; INDEX2 → X

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SAMPLE PROGRAM FOR *Figure 17* INTERFACING MULTIPLE A/D's IN AN MC6800 SYSTEM

ADDRESS	HEX CODE	MNEMONICS			COMMENTS
0033	A7 00		STAA	X	; Store data at X
0035	8C 02 07		CPX	#$0207	; Have all A/D's been read?
0038	27 05		BEQ	RETURN	; Yes: branch to RETURN
003A	08		INX		; No: increment X by one
003B	DF 42		STX	INDEX2	; X → INDEX2
003D	20 EB		BRA	INTRPT	; Branch to 002A
003F	3B	RETURN	RTI		
0040	50 00	INDEX1	FDB	$5000	; Starting address for A/D
0042	02 00	INDEX2	FDB	$0200	; Starting address for data storage
0044	00 00	TEMP	FDB	$0000	

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Note 25: In order for the microprocessor to service subroutines and interrupts, the stack pointer must be dimensioned in the user's program.

For amplification of DC input signals, a major system error is the input offset voltage of the amplifiers used for the preamp. *Figure 18* is a gain of 100 differential preamp whose offset voltage errors will be cancelled by a zeroing subroutine which is performed by the INS8080A microprocessor system. The total allowable input offset voltage error for this preamp is only 50 µV for ¼ LSB error. This would obviously require very precise amplifiers. The expression for the differential output voltage of the preamp is:

$$V_O = \underbrace{[V_{IN}(+) - V_{IN}(-)]}_{\text{SIGNAL}} \underbrace{\left[1 + \frac{2R2}{R1}\right]}_{\text{GAIN}} +$$

$$\underbrace{(V_{OS_2} - V_{OS_1} - V_{OS_3} \pm I_X R_X)}_{\text{DC ERROR TERM}} \underbrace{\left(1 + \frac{2R2}{R1}\right)}_{\text{GAIN}}$$

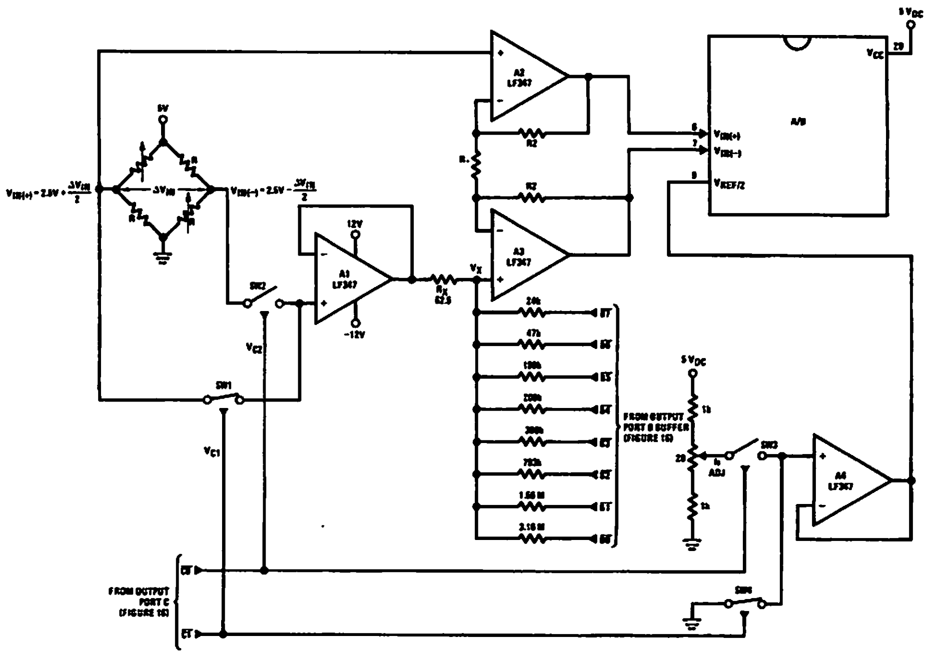
where I_X is the current through resistor R_X. All of the offset error terms can be cancelled by making $\pm I_X R_X = V_{OS1} + V_{OS3} - V_{OS2}$. This is the principle of this auto-zeroing scheme.

The INS8080A uses the 3 I/O ports of an INS8255 Programable Peripheral Interface (PPI) to control the auto zeroing and input data from the ADC0801 as shown in *Figure 19*. The PPI is programmed for basic I/O operation (mode 0) with Port A being an input port and Ports B and C being output ports. Two bits of Port C are used to alternately open or close the 2 switches at the input of the preamp. Switch SW1 is closed to force the preamp's differential input to be zero during the zeroing subroutine and then opened and SW2 is then closed for conversion of the actual differential input signal. Using 2 switches in this manner eliminates concern for the ON resistance of the switches as they must conduct only the input bias current of the input amplifiers.

Output Port B is used as a successive approximation register by the 8080 and the binary scaled resistors in series with each output bit create a D/A converter. During the zeroing subroutine, the voltage at V_x increases or decreases as required to make the differential output voltage equal to zero. This is accomplished by ensuring that the voltage at the output of A1 is approximately 2.5V so that a logic "1" (5V) on

Functional Description (Continued)

any output of Port B will source current into node V_X thus raising the voltage at V_X and making the output differential more negative. Conversely, a logic "0" (0V) will pull current out of node V_X and decrease the voltage, causing the differential output to become more positive. For the resistor values shown, V_X can move ±12 mV with a resolution of 50 µV, which will null the offset error term to ¼ LSB of full-scale for the ADC0801. It is important that the voltage levels that drive the auto-zero resistors be constant. Also, for symmetry, a logic swing of 0V to 5V is convenient. To achieve this, a CMOS buffer is used for the logic output signals of Port B and this CMOS package is powered with a stable 5V source. Buffer amplifier A1 is necessary so that it can source or sink the D/A output current.



Note 26: R2 = 49.5 R1

Note 27: Switches are LMC13334 CMOS analog switches.

Note 28: The 9 resistors used in the auto-zero section can be ±5% tolerance.

FIGURE 18. Gain of 100 Differential Transducer Preamp

Functional Description (Continued)

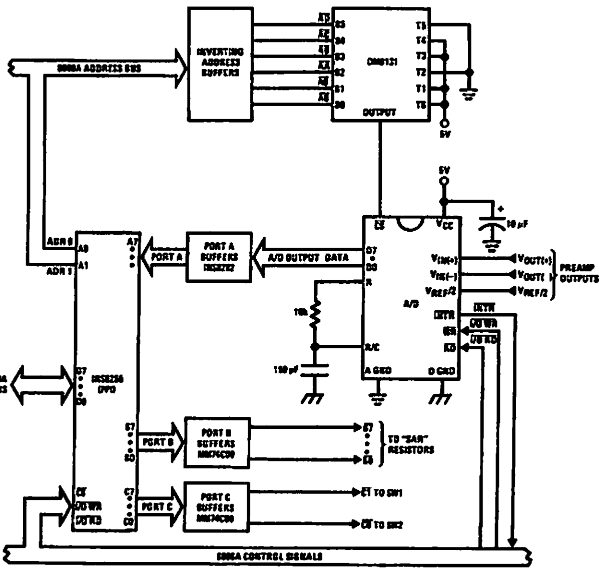


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FIGURE 19. Microprocessor Interface Circuitry for Differential Preamp

A flow chart for the zeroing subroutine is shown in *Figure 20*. It must be noted that the ADC0801 series will output an all zero code when it converts a negative input $[V_{IN}(-) \geq V_{IN}(+)]$. Also, a logic inversion exists as all of the I/O ports are buffered with inverting gates.

Basically, if the data read is zero, the differential output voltage is negative, so a bit in Port B is cleared to pull V_X more negative which will make the output more positive for the next conversion. If the data read is not zero, the output voltage is positive so a bit in Port B is set to make V_X more positive and the output more negative. This continues for 8 approximations and the differential output eventually converges to within 5 mV of zero.

The actual program is given in *Figure 21*. All addresses used are compatible with the BLC 80/10 microcomputer system. In particular:

Port A and the ADC0801 are at port address E4

Port B is at port address E5

Port C is at port address E6

PPI control word port is at port address E7

Program Counter automatically goes to ADDR:3C3D upon acknowledgement of an interrupt from the ADC0801

5.3 Multiple A/D Converters in a Z-80 Interrupt Driven Mode

In data acquisition systems where more than one A/D converter (or other peripheral device) will be interrupting program execution of a microprocessor, there is obviously a need for the CPU to determine which device requires servicing. *Figure 22* and the accompanying software is a method of determining which of 7 ADC0801 converters has completed a conversion ($\overline{INTR}$ asserted) and is requesting an interrupt. This circuit allows starting the A/D converters in any sequence, but will input and store valid data from the converters with a priority sequence of A/D 1 being read first, A/D 2 second, etc., through A/D 7 which would have the lowest priority for data being read. Only the converters whose INT is asserted will be read.

The key to decoding circuitry is the DM74LS373, 8-bit D type flip-flop. When the Z-80 acknowledges the interrupt, the program is vectored to a data input Z-80 subroutine. This subroutine will read a peripheral status word from the DM74LS373 which contains the logic state of the $\overline{INTR}$ outputs of all the converters. Each converter which initiates an interrupt will place a logic "0" in a unique bit position in the status word and the subroutine will determine the identity of the converter and execute a data read. An identifier word (which indicates which A/D the data came from) is stored in the next sequential memory location above the location of the data so the program can keep track of the identity of the data entered.

Functional Description (Continued)

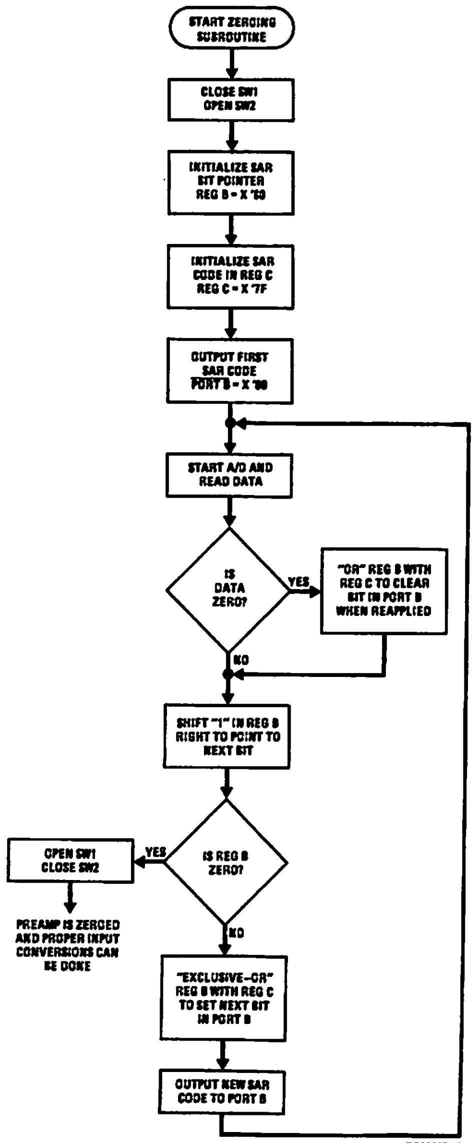

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FIGURE 20. Flow Chart for Auto-Zero Routine

Functional Description (Continued)

```
3D00  3E90     MVI 90
3D02  D3E7     Out Control Port                                      ; Program PPI
3D04  2601     MVI H 01               Auto-Zero Subroutine
3D06  7C       MOV A,H
3D07  D3E6     OUT C                                                 ; Close SW1 open SW2
3D09  0680     MVI B 80                                              ; Initialize SAR bit pointer
3D0B  3E7F     MVI A 7F                                              ; Initialize SAR code
3D0D  4F       MOV C,A                Return
3D0E  D3E5     OUT B                                                 ; Port B = SAR code
3D10  31AA3D   LXI SP 3DAA            Start                          ; Dimension stack pointer
3D13  D3E4     OUT A                                                 ; Start A/D
3D15  FB       IE
3D16  00       NOP                    Loop                           ; Loop until INT asserted
3D17  C3163D   JMP Loop
3D1A  7A       MOV A,D                Auto-Zero
3D1B  C600     ADI 00
3D1D  CA2D3D   JZ Set C                                              ; Test A/D output data for zero
3D20  78       MOV A,B                Shift B
3D21  F600     ORI 00                                                ; Clear carry
3D23  1F       RAR                                                   ; Shift "1" in B right one place
3D24  FE00     CPI 00                                                ; Is B zero? If yes last
3D26  CA373D   JZ Done                                               ; approximation has been made
3D29  47       MOV B,A
3D2A  C3333D   JMP New C
3D2D  79       MOV A,C                Set C
3D2E  B0       ORA B                                                 ; Set bit in C that is in same
3D2F  4F       MOV C,A                                               ; position as "1" in B
3D30  C3203D   JMP Shift B
3D33  A9       XRA C                  New C                          ; Clear bit in C that is in
3D34  C30D3D   JMP Return                                            ; same position as "1" in B
3D37  47       MOV B,A                Done                           ; then output new SAR code.
3D38  7C       MOV A,H                                               ; Open SW1, close SW2 then
3D39  EE03     XRI 03                                                ; proceed with program. Preamp
3D3B  D3E6     OUT C                                                 ; is now zeroed.
3D3D           •                      Normal
               •
               •
               Program for processing
               proper data values
3C3D  DBE4     IN A                   Read A/D Subroutine            ; Read A/D data
3C3F  EEFF     XRI FF                                                ; Invert data
3C41  57       MOV D,A
3C42  78       MOV A,B                                               ; Is B Reg = 0? If not stay
3C43  E6FF     ANI FF                                                ; in auto zero subroutine
3C45  C21A3D   JNZ Auto-Zero
3C48  C33D3D   JMP Normal
```

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Note 29: All numerical values are hexadecimal representations.

FIGURE 21. Software for Auto-Zeroed Differential A/D

5.3 Multiple A/D Converters in a Z-80 Interrupt Driven Mode (Continued)

The following notes apply:

- It is assumed that the CPU automatically performs a RST 7 instruction when a valid interrupt is acknowledged (CPU is in interrupt mode 1). Hence, the subroutine starting address of X0038.
- The address bus from the Z-80 and the data bus to the Z-80 are assumed to be inverted by bus drivers.
- A/D data and identifying words will be stored in sequential memory locations starting at the arbitrarily chosen address X 3E00.
- The stack pointer must be dimensioned in the main program as the RST 7 instruction automatically pushes the PC onto the stack and the subroutine uses an additional 6 stack addresses.
- The peripherals of concern are mapped into I/O space with the following port assignments:

Functional Description (Continued)

HEX PORT ADDRESS	PERIPHERAL
00	MM74C374 8-bit flip-flop
01	A/D 1
02	A/D 2
03	A/D 3
04	A/D 4
05	A/D 5
06	A/D 6
07	A/D 7

This port address also serves as the A/D identifying word in the program.

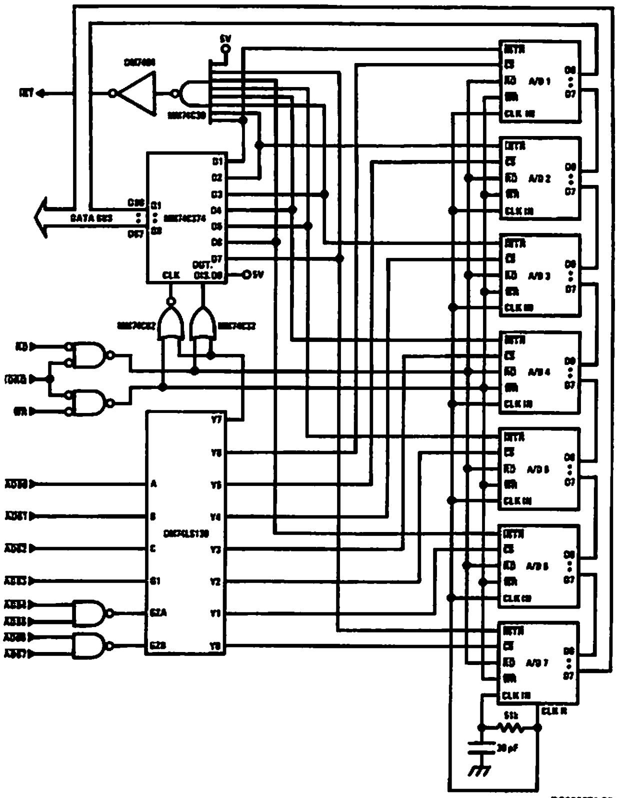

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FIGURE 22. Multiple A/Ds with Z-80 Type Microprocessor

Functional Description (Continued)

INTERRUPT SERVICING SUBROUTINE

LOC	OBJ CODE		SOURCE STATEMENT	COMMENT
0038	E5		PUSH HL	; Save contents of all registers affected by
0039	C5		PUSH BC	; this subroutine.
003A	F5		PUSH AF	; Assumed INT mode 1 earlier set.
003B	21 00 3E		LD (HL),X3E00	; Initialize memory pointer where data will be stored.
003E	0E 01		LD C, X01	; C register will be port ADDR of A/D converters.
0040	D300		OUT X00, A	; Load peripheral status word into 8-bit latch.
0042	DB00		IN A, X00	; Load status word into accumulator.
0044	47		LD B,A	; Save the status word.
0045	79	TEST	LD A,C	; Test to see if the status of all A/D's have
0046	FE 08		CP, X08	; been checked. If so, exit subroutine
0048	CA 60 00		JPZ, DONE	
004B	78		LD A,B	; Test a single bit in status word by looking for
004C	1F		RRA	; a "1" to be rotated into the CARRY (an INT
004D	47		LD B,A	; is loaded as a "1"). If CARRY is set then load
004E	DA 5500		JPC, LOAD	; contents of A/D at port ADDR in C register.
0051	0C	NEXT	INC C	; If CARRY is not set, increment C register to point
0052	C3 4500		JP,TEST	; to next A/D, then test next bit in status word.
0055	ED 78	LOAD	IN A, (C)	; Read data from interrupting A/D and invert
0057	EE FF		XOR FF	; the data.
0059	77		LD (HL),A	; Store the data
005A	2C		INC L	
005B	71		LD (HL),C	; Store A/D identifier (A/D port ADDR).
005C	2C		INC L	
005D	C3 51 00		JP,NEXT	; Test next bit in status word.
0060	F1	DONE	POP AF	; Re-establish all registers as they were
0061	C1		POP BC	; before the interrupt.
0062	E1		POP HL	
0063	C9		RET	; Return to original program

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Measurement of pH in the Biochemistry and Food Industries

The pH of food can be measured with the use of color indicators or electrochemically. In acid-base titration, indicators are used which change color at around pH 9.0. The pH values of foodstuffs which are not too highly colored can be readily determined by the use of pH indicator papers. These are now available in wide and narrow ranges of pH, enabling values to be measured within 0.5 or less units of pH.

Electrochemical measurements using pH meters are now simple and accurate. Micro-electronic components have made possible small portable high quality instruments with digital displays, some with built-in electrodes. These meters measure the potential difference between a glass electrode and a standard calomel electrode or silver/silver chloride electrode and are calibrated by the use of prepared or purchased buffer solutions of accurately known pH. There are also available other types of electrodes designed for special purposes, such as probe electrodes for the examination of carcass meat. Very accurate pH measurement, through seldom required in food analysis, is very susceptible to the temperature of the test solution. Temperature compensation devices are incorporated in pH meters to correct for known temperature deviations.

Some of the pH values of a number of biological materials are given below:

Material	pH value
Blood, normal limits	7.3 - 7.5
Blood, extreme limits	7.0 - 7.8
Enzymes, activity range of	
Amylopsin, optimum	7.0
Erepsin, optimum	7.8
Invertase, optimum	5.5
Lipase, optimum	7.0 - 8.0
Maltase, optimum	6.1 - 6.8
Pepsin, optimum	1.5 - 2.4
Trypsin, optimum	8.0 - 9.0
Fruit Juices	
Apple	3.8
Banana	4.6
Grapefruit	3.0 - 3.3
Orange	3.1 -4.1
Tomato	4.2
Gastric juice (adult)	0.9 - 1.6
Milk (cows)	6.2 - 7.3
Plants (extracted juice)	
Alfalfa tops	5.9
Carrot	5.2
Cucumber	5.2
Peas, field	6.8
Potato	6.1
Rhubarb, stalks	3.4
String beans	5.2
Sweat	4.5 - 7.1
Saliva	6.2 - 7.6
Urine (human)	4.2 - 8.0
Tears	7.2

Table A - pH Values of Representative Biological Materials, Elements of Food Biochemistry, William H. Peterson, Ph.D., John T. Skinner,

Measurement of pH in the Biochemistry and Food Industries

The pH of food can be measured with the use of color indicators or electrochemically. In acid-base titration, indicators are used which change color at around pH 9.0. The pH values of foodstuffs which are not too highly colored can be readily determined by the use of pH indicator papers. These are now available in wide and narrow ranges of pH, enabling values to be measured within 0.5 or less units of pH.

Electrochemical measurements using pH meters are now simple and accurate. Micro-electronic components have made possible small portable high quality instruments with digital displays, some with built-in electrodes. These meters measure the potential difference between a glass electrode and a standard calomel electrode or silver/silver chloride electrode and are calibrated by the use of prepared or purchased buffer solutions of accurately known pH. There are also available other types of electrodes designed for special purposes, such as probe electrodes for the examination of carcass meat. Very accurate pH measurement, through seldom required in food analysis, is very susceptible to the temperature of the test solution. Temperature compensation devices are incorporated in pH meters to correct for known temperature deviations.

Some of the pH values of a number of biological materials are given below:

Material	pH value
Blood, normal limits	7.3 - 7.5
Blood, extreme limits	7.0 - 7.8
Enzymes, activity range of	
Amylopsin, optimum	7.0
Erepsin, optimum	7.8
Invertase, optimum	5.5
Lipase, optimum	7.0 - 8.0
Maltase, optimum	6.1 - 6.8
Pepsin, optimum	1.5 - 2.4
Trypsin, optimum	8.0 - 9.0
Fruit Juices	
Apple	3.8
Banana	4.6
Grapefruit	3.0 - 3.3
Orange	3.1 -4.1
Tomato	4.2
Gastric juice (adult)	0.9 - 1.6
Milk (cows)	6.2 - 7.3
Plants (extracted juice)	
Alfalfa tops	5.9
Carrot	5.2
Cucumber	5.2
Peas, field	6.8
Potato	6.1
Rhubarb, stalks	3.4
String beans	5.2
Sweat	4.5 - 7.1
Saliva	6.2 - 7.6
Urine (human)	4.2 - 8.0
Tears	7.2

Table A - pH Values of Representative Biological Materials, Elements of Food Biochemistry, William H. Peterson, Ph.D., John T. Skinner,

Recommendations

Eutech's pHScan 1/2/3 and pHScan BNC/3BNC series is the ideal tool for quick testing the pH value. For discerning technologists and researchers, best to use a pH hand-held meter i.e. pH5/6/10/100 or bench meter i.e. pH510/1000/2500 for better accuracy and useful features. Note some models require separate specialized electrodes for different applications.

Electrode Type	Application
EC-FG73504-01B	General purpose application for aqueous pH measurement. Glass body 110mm (L) x 12mm (dia.)
EC-FG73905-01B	For tris buffers, clinical and biological media containing proteins, creams, fats and cosmetics. Also suitable for measurement in fruit juices, beer, milk and yogurt. Glass body 110mm (L) x 12mm (dia.)
EC-FG63511-01B	Sharp tip pH electrode for solid or semi-solid sample such as cheese, meats, fruits, bread or other similar samples
EC-FE13901-01B	Ideal for test tube measurements of fruit juices, beer, milk and yogurt. Epoxy body 155mm (L) x 9 mm (dia.)

pH ELECTRODE PERFORMANCE

By Mike Ross- Sensorex USA

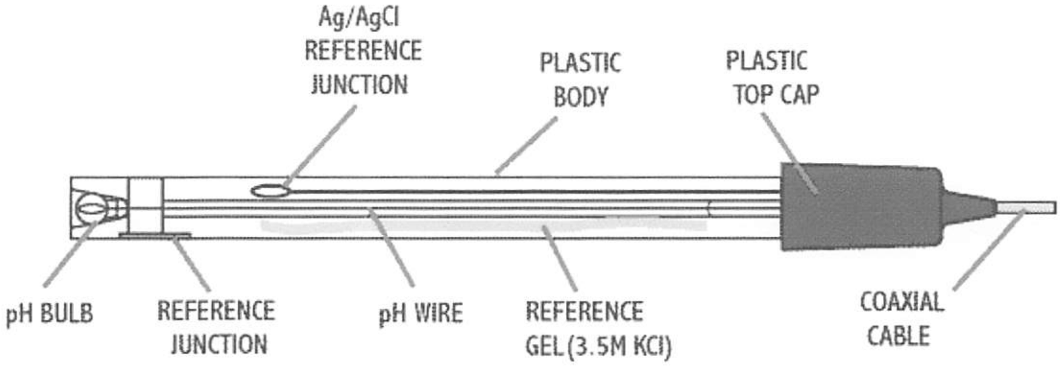
Preface

The purpose of this article is educational. The intent is to provide a practical explanation and general understanding of how to evaluate the performance of both new and used pH electrodes. Also discussed are some of the many factors which can affect pH electrode performance and to aid the reader in understanding what they may be able to do to increase performance and service life.

pH Electrodes

pH electrodes are electrochemical sensors used by many industries but are of particular importance to the water and wastewater industry. The sensor itself is similar to a battery. It generates a voltage output and has a useful service and shelf life. While there are many types of pH electrodes used in field, lab and process environments, we will concentrate on a basic design for this article.

Basic Construction of a pH electrode Fig 1



OFFSET - Theoretically, when placed in 7.00 buffer at 25°C a pH electrode produces zero millivolts which the pH meter reads as 7.00 pH. The difference between these perfect readings and the electrode's actual reading is called the offset error.

SPAN - A perfect pH electrode, at 25°C produces 59.12mV per pH unit. The difference between this perfect reading and the electrode's actual reading is called the span error.

These theoretical values are not always achieved, even with brand new electrodes. New pH electrode performance specifications should meet the following criteria:

TYPICAL SPECIFICATION - Offset: 7.00 +/- 0.2 pH (+/- 12mV) SPAN: Better than 95% of theory; i.e. between 56.2 and 59.2 mV

Normal Aging

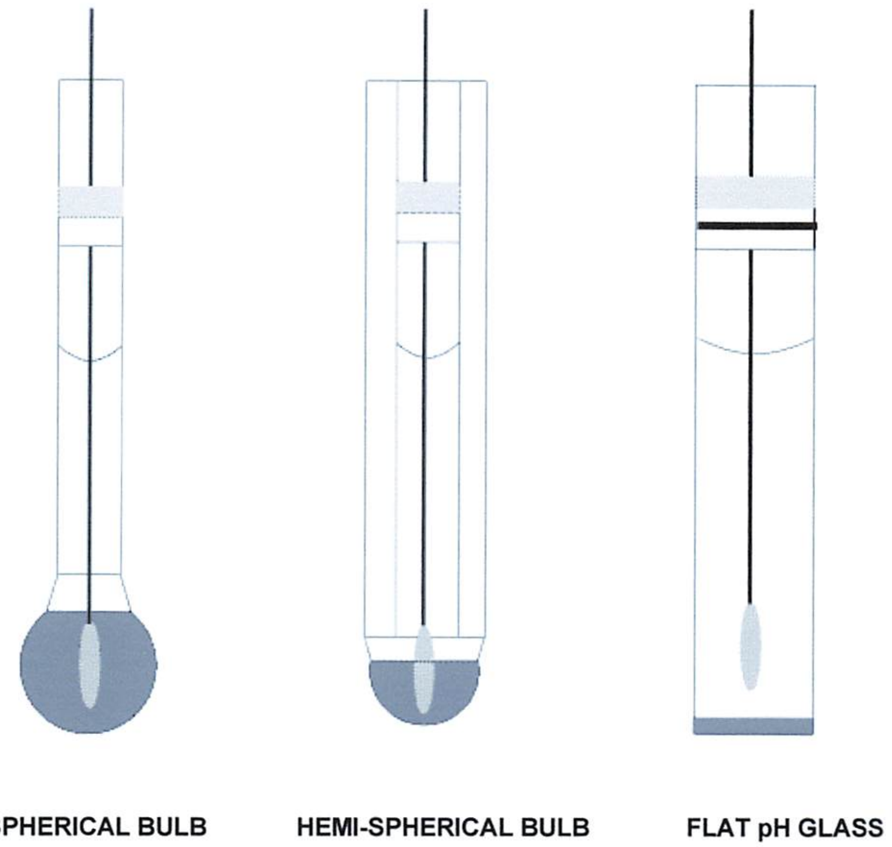
As electrodes are used or stored for long periods they will experience some shifts in these new electrode specifications. OFFSETS will change and SPAN error will increase; i.e., the span will become shorter. By using the calibration controls these errors can be corrected. If an electrode is able to be calibrated and it is stable and responsive, it is still a functional electrode and may be used in service even though it no longer meets "new" electrode specifications.

As described later in this article, an electrode's response time becomes longer as it ages. Even though the electrode can be calibrated, sluggish response can limit its life. Also, certain application conditions, elevated temperatures, for example, will cause electrodes to have shorter service lives.

Speed of Response

An electrode's speed of response is affected by several things; mainly, by the impedance (resistance) of the pH glass measuring surface and the condition of this surface. The type of pH responsive glass used and the size, shape and thickness of its surface all affect impedance characteristics. When selecting pH electrodes there are tradeoffs to consider. Here is a comparison of the three most common shapes:

Shapes of pH measuring Surfaces Fig 2



A spherical shaped bulb will provide 95% response in less than one second. It has low impedance and fast response but is relatively fragile. pH electrodes with spherical shaped surfaces are designed so that the bulb is recessed inside the electrode body. Such designs protect the glass bulb against breakage.

A hemispherical shaped bulb is a stronger shape mechanically and, as a result, it has a higher impedance and slightly slower response. These shapes are often used in a fully exposed manner.

A flat measuring surface is the most durable of all the shapes. It makes good sample contact, is easily cleaned, is very strong mechanically but has the highest impedance and the slowest speed of response-95% in less than 5 seconds.

Coatings can mimic a sluggish speed response problem; therefore a used pH glass measuring surface should be cleaned before assuming that the electrode is no longer functional. Normally, the electrode may be cleaned with whatever chemical the coating material is soluble in provided the chemical will not attack the electrode's materials of construction. The glass surface should never be cleaned in a manner that would scratch the glass surface. Scratches will result in a slow response and shorter working life. When wiping the surface always use clean, non abrasive materials and cloths.

Effects of Temperature

The impedance issue previously discussed is also a factor when measuring samples at temperatures other than 25°C. For every 10°C decrease in temperature the glass impedance will increase about 2.5 times. Therefore a spherical electrode (which has lower impedance) will offer better speed of response in lower temperatures than a flat electrode will.

Use of electrodes in elevated temperatures will cause pH electrodes to experience shorted service life than if used at ambient temperature. High temperatures accelerate both the natural aging of pH glass and chemical attack of the glass. These factors can cause impedance to increase and the surface to loose its ability to respond to hydrogen ion activity (which is what a pH electrode actually measures!).

High and Low pH Measurements

Very strong acidic or caustic solutions will accelerate aging of a pH electrode leading to shorter service life. Some of these solutions will actually etch the pH glass surface with a resulting loss of response to hydrogen ions. There are special formulations of glass which are available from some manufacturers to resist this degradation.

Low Ionic Strength Measurements

pH measurement in low ionic or low conductivity solutions may create several problems for standard pH electrodes. Typical difficulties include:

- Slow sluggish or drifting readings
- Unrepeatable readings
- Premature electrode failure

Special design electrodes have been developed and are often used in low ionic strength applications. They may feature:

Reference junctions- the porous material that contacts the sample- are made of porous materials so that there is a very large surface area where the junction contacts the sample.

The reference junction is peripheral; that is, it surrounds the glass stem onto which the pH bulb is blown. This design minimizes streaming current effects which can generate spurious reference junction potentials.

The built-in reference electrode is a double junction design. The inner chamber contains the usual high (3.0M or higher) salt concentration solutions or gels so that stable outputs are generated. The outer chamber, which contacts the sample through the porous reference junction, is filled with a low ionic solution or gel. This lower ionic strength material more closely matches that of the sample and further reduces spurious potentials.

Single vs. Double Junction References

For many applications, a single junction reference electrode is satisfactory. However, if samples contain proteins, sulfides, heavy metals or any other material which interacts with silver ions, unwanted side reactions may occur. These reactions can lead to erroneous reference signals or to precipitation at the reference junction leading to a short service life.

A double junction reference design affords a barrier of protection to combat the above interactions. When in doubt about using single or double junction designs, the safest approach is to use the double junction; they can be used anywhere a single junction design can be used. Conversely, single junction designs should not be used where double junction designs are needed. In most process applications, it is recommended to use double junction electrodes.

Electrical Ground Problems

When a pH system is unstable, erratic, has short electrode service life or the offset drifts, the most common problem is an electrical ground loop in the system, particularly if the tank and/or pipes are plastic. To verify this problem, remove the electrode and calibrate it in a known buffer in a beaker. Pull a sample of the solution from the process and verify meter reads sample correctly.

Electrical Ground Problem Fig 3

ELECTRODE CALIBRATES IN BUFFER AND READS SAMPLE OUTSIDE OF PROCESS

THEN

ELECTRODE READS HIGH OR OUT OF RANGE IN ROCESS

The sources of the ground loop could be any mixer motor, pump, conductivity probe, or other electrically powered device in the media with the pH electrode.

POSSIBLE SOLUTIONS

1. Check to see if any voltage producing sensor such as a conductivity or amperometric sensor is in the same solution or the meter to which they are attached is sharing same ground with your pH meter or controller. Power down that device and verify if the pH instrument is reading correctly.
2. Try placing a large (12 or 14 AWG) copper wire into the media and the other end to the meter or controller ground terminal to draw the ground loop away from the pH electrode.
3. Disconnect all devices connected to meter or controller. This includes all pumps, alarms, outputs, etc. If the problem solves, re-connect 1 item at a time to isolate the problem device.
4. A pH electrode with an internal differential amplifier and solution ground may provide a solution if all else fails. There are electrodes available with internal batteries, solution

grounds and differential amplifiers which will hook directly to your existing meter even though it was not designed to use this technology.

Storage/Shelf Life

Since pH electrodes have limited lives, it is important to keep one or more spare electrodes available for replacement. An important aspect of the performance of any spare pH electrode is that it will it work when you need it. Electrodes supplied in soaker storage bottles with special soaker solutions have longer shelf lives than those supplied dry, with small caps or dry stored after use. The special solution in soaker bottles provides an environment that maintains pH glass hydration in an acidic environment as well as keeping the reference junction wet and communicating. If the original solution is no longer available, the following are acceptable storage medias for pH electrodes in order of preference:

- 4.00 pH Buffer

- 7.00 pH Buffer

Note: Never store a pH electrode in de-ionized water. De- ionized water is only for rinsing.

Conclusion

I hope this article provided you with some insight into pH electrodes and the real world issues pertaining to their use and performance. Similar to batteries, they will have a useful service life and will require replacement. Understanding application use effects and the causes can assist you in the use, expense and performance of your pH operating system.

ABOUT THE AUTHOR

Mike Ross is the Director of Sales and Marketing for Sensorex in Garden Grove, California USA. He has spent over 25 years in the instrumentation and sensor industry. For questions or comments you may contact him at mike@sensorex.com

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National Semiconductor

November 1999

ADC0801/ADC0802/ADC0803/ADC0804/ADC0805 8-Bit µP Compatible A/D Converters

General Description

The ADC0801, ADC0802, ADC0803, ADC0804 and ADC0805 are CMOS 8-bit successive approximation A/D converters that use a differential potentiometric ladder—similar to the 256R products. These converters are designed to allow operation with the NSC800 and INS8080A derivative control bus with TRI-STATE® output latches directly driving the data bus. These A/Ds appear like memory locations or I/O ports to the microprocessor and no interfacing logic is needed.

Differential analog voltage inputs allow increasing the common-mode rejection and offsetting the analog zero input voltage value. In addition, the voltage reference input can be adjusted to allow encoding any smaller analog voltage span to the full 8 bits of resolution.

Features

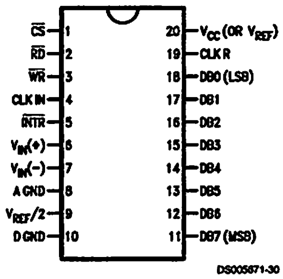
- Compatible with 8080 µP derivatives—no interfacing logic needed - access time - 135 ns
- Easy interface to all microprocessors, or operates "stand alone"
- Differential analog voltage inputs
- Logic inputs and outputs meet both MOS and TTL voltage level specifications
- Works with 2.5V (LM336) voltage reference
- On-chip clock generator
- 0V to 5V analog input voltage range with single 5V supply
- No zero adjust required
- 0.3" standard width 20-pin DIP package
- 20-pin molded chip carrier or small outline package
- Operates ratiometrically or with 5 V_{DC}, 2.5 V_{DC}, or analog span adjusted voltage reference

Key Specifications

- Resolution 8 bits
- Total error ±¼ LSB, ±½ LSB and ±1 LSB
- Conversion time 100 µs

Connection Diagram

ADC080X
Dual-In-Line and Small Outline (SO) Packages



See Ordering Information

Ordering Information

TEMP RANGE		0°C TO 70°C	0°C TO 70°C	−40°C TO +85°C
ERROR	±¼ Bit Adjusted			ADC0801LCN
	±½ Bit Unadjusted	ADC0802LCWM		ADC0802LCN
	±½ Bit Adjusted			ADC0803LCN
	±1Bit Unadjusted	ADC0804LCWM	ADC0804LCN	ADC0805LCN/ADC0804LCJ
PACKAGE OUTLINE		M20B—Small Outline	N20A—Molded DIP	

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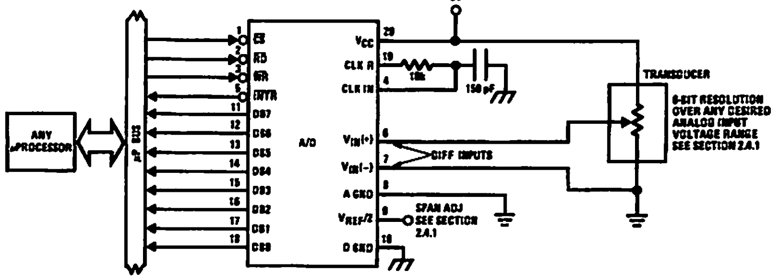
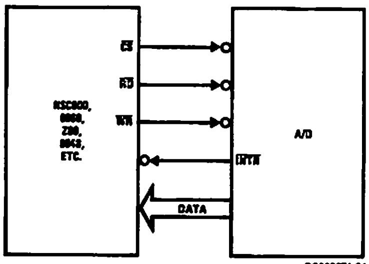
Z-80® is a registered trademark of Zilog Corp.

Typical Applications



DS005671-1

8080 Interface



DS005671-31

Error Specification (Includes Full-Scale, Zero Error, and Non-Linearity)			
Part Number	Full-Scale Adjusted	$V_{REF}/2=2.500\ V_{DC}$ (No Adjustments)	$V_{REF}/2$=No Connection (No Adjustments)
ADC0801	±¼ LSB		
ADC0802		±½ LSB	
ADC0803	±½ LSB		
ADC0804		±1 LSB	
ADC0805			±1 LSB

AC Electrical Characteristics (Continued)

The following specifications apply for V_{CC}=5 V_{DC} and $T_{MIN} \le T_A \le T_{MAX}$ unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Units
C_{OUT}	TRI-STATE Output Capacitance (Data Buffers)			5	7.5	pF
CONTROL INPUTS [Note: CLK IN (Pin 4) is the input of a Schmitt trigger circuit and is therefore specified separately]						
V_{IN} (1)	Logical "1" Input Voltage (Except Pin 4 CLK IN)	V_{CC}=5.25 V_{DC}	2.0		15	V_{DC}
V_{IN} (0)	Logical "0" Input Voltage (Except Pin 4 CLK IN)	V_{CC}=4.75 V_{DC}			0.8	V_{DC}
I_{IN} (1)	Logical "1" Input Current (All Inputs)	V_{IN}=5 V_{DC}		0.005	1	μA_{DC}
I_{IN} (0)	Logical "0" Input Current (All Inputs)	V_{IN}=0 V_{DC}	−1	−0.005		μA_{DC}
CLOCK IN AND CLOCK R						
V_T+	CLK IN (Pin 4) Positive Going Threshold Voltage		2.7	3.1	3.5	V_{DC}
V_T−	CLK IN (Pin 4) Negative Going Threshold Voltage		1.5	1.8	2.1	V_{DC}
V_H	CLK IN (Pin 4) Hysteresis (V_T+)−(V_T−)		0.6	1.3	2.0	V_{DC}
V_{OUT} (0)	Logical "0" CLK R Output Voltage	I_O=360 µA V_{CC}=4.75 V_{DC}			0.4	V_{DC}
V_{OUT} (1)	Logical "1" CLK R Output Voltage	I_O=−360 µA V_{CC}=4.75 V_{DC}	2.4			V_{DC}
DATA OUTPUTS AND $\overline{INTR}$						
V_{OUT} (0)	Logical "0" Output Voltage					
	Data Outputs	I_{OUT}=1.6 mA, V_{CC}=4.75 V_{DC}			0.4	V_{DC}
	$\overline{INTR}$ Output	I_{OUT}=1.0 mA, V_{CC}=4.75 V_{DC}			0.4	V_{DC}
V_{OUT} (1)	Logical "1" Output Voltage	I_O=−360 µA, V_{CC}=4.75 V_{DC}	2.4			V_{DC}
V_{OUT} (1)	Logical "1" Output Voltage	I_O=−10 µA, V_{CC}=4.75 V_{DC}	4.5			V_{DC}
I_{OUT}	TRI-STATE Disabled Output Leakage (All Data Buffers)	V_{OUT}=0 V_{DC}	−3			μA_{DC}
		V_{OUT}=5 V_{DC}			3	μA_{DC}
I_{SOURCE}		V_{OUT} Short to Gnd, T_A=25°C	4.5	6		mA_{DC}
I_{SINK}		V_{OUT} Short to V_{CC}, T_A=25°C	9.0	16		mA_{DC}
POWER SUPPLY						
I_{CC}	Supply Current (Includes Ladder Current)	f_{CLK}=640 kHz, V_{REF}/2=NC, T_A=25°C and $\overline{CS}$ =5V				
	ADC0801/02/03/04LCJ/05			1.1	1.8	mA
	ADC0804LCN/LCWM			1.9	2.5	mA

Note 1: Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. DC and AC electrical specifications do not apply when operating the device beyond its specified operating conditions.

Note 2: All voltages are measured with respect to Gnd, unless otherwise specified. The separate A Gnd point should always be wired to the D Gnd.

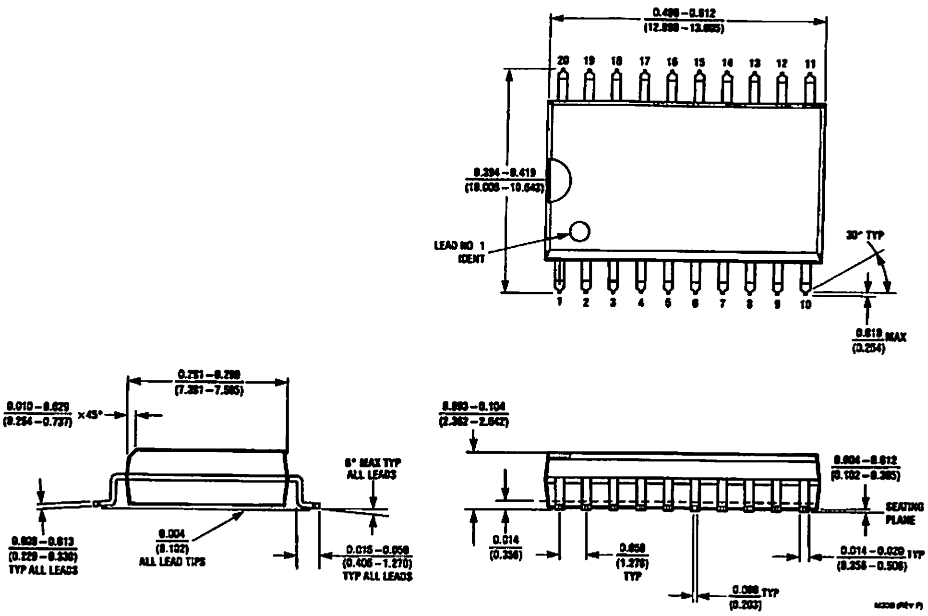
Note 3: A zener diode exists, internally, from V_{CC} to Gnd and has a typical breakdown voltage of 7 V_{DC}.

Note 4: For $V_{IN}(-) \ge V_{IN}(+)$ the digital output code will be 0000 0000. Two on-chip diodes are tied to each analog input (see block diagram) which will forward conduct for analog input voltages one diode drop below ground or one diode drop greater than the V_{CC} supply. Be careful, during testing at low V_{CC} levels (4.5V), as high level analog inputs (5V) can cause this input diode to conduct–especially at elevated temperatures, and cause errors for analog inputs near full-scale. The spec allows 50 mV forward bias of either diode. This means that as long as the analog V_{IN} does not exceed the supply voltage by more than 50 mV, the output code will be correct. To achieve an absolute 0 V_{DC} to 5 V_{DC} input voltage range will therefore require a minimum supply voltage of 4.950 V_{DC} over temperature variations, initial tolerance and loading.

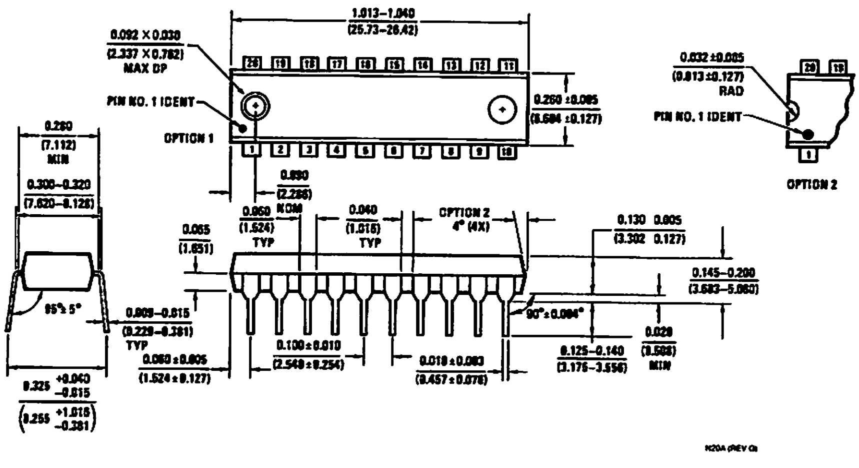
Note 5: Accuracy is guaranteed at f_{CLK} = 640 kHz. At higher clock frequencies accuracy can degrade. For lower clock frequencies, the duty cycle limits can be extended so long as the minimum clock high time interval or minimum clock low time interval is no less than 275 ns.

Note 6: With an asynchronous start pulse, up to 8 clock periods may be required before the internal clock phases are proper to start the conversion process. The start request is internally latched, see *Figure 4* and section 2.0.

Physical Dimensions inches (millimeters) unless otherwise noted



SO Package (M)
Order Number ADC0802LCWM or ADC0804LCWM
NS Package Number M20B



Molded Dual-In-Line Package (N)
Order Number ADC0801LCN, ADC0802LCN, ADC0803LCN, ADC0804LCN or ADC0805LCN
NS Package Number N20A

Notes

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FORMULIR PERBAIKAN SKRIPSI

1. Jelaskan cara merangkai MC AtMEGA :

   - Pin Vcc diberi tegangan (kaki 10) +5V.
   - Grnd diberi tegangan $\pm$ 0 V (kaki 11).
   - Xtal 1 dan 2 diberi tegangan kristal (0 – 8 Mhz).
   - Pin reset (kaki 9) diberi kondisi aktif High.
   - Pada program diberi inialisasi port input atau output.
   - Inialisasi line prom.
   - Menentukan port yang akan dikontrol.
   - LCD port A.
   - ADC port B.
   - Relay port C.
   - Sensor port D.

2. Jelaskan fungsi dan mekanisme tembaga dan besi dan skema akan MC :

   Tembaga diberi arus jika air mengenai tembaga dan besi akan menjadi penghantar.

3. Jelaskan cara MC dalam mengontrol kran air dan menerima data pH dari pH meter :

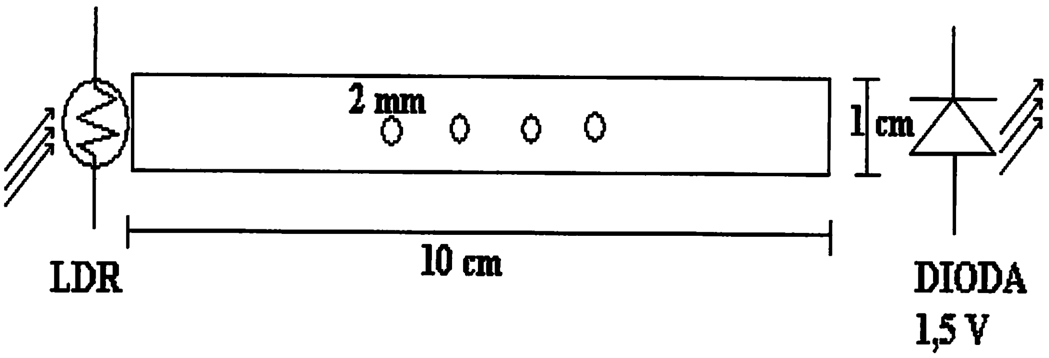
   - Cara MC dalam mengontrol pH :

   pH mengeluarkan tegangan kecil perlu dikuatkan atau dibuffer setelah masuk kedalam kedalam ADC setelah itu data diambil oleh MC dan diolah, tampil pada LCD. Tapi data tersebut masuk lock up table untuk dapat mengontrol pH tersebut.

- Cara MC dalam mengontrol kran air :

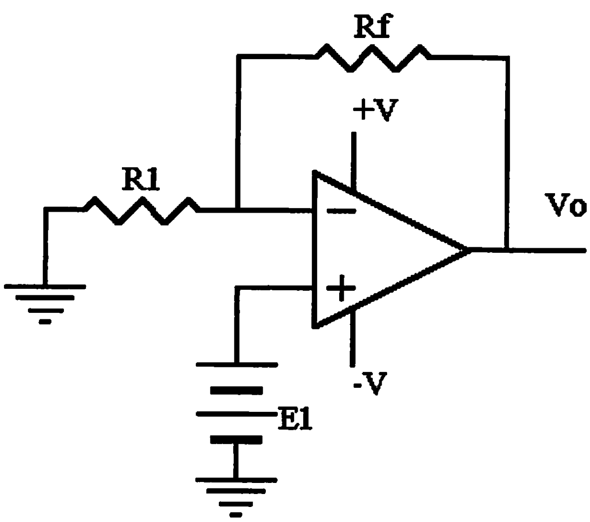
arena driver aktif low maka diberi bahasa pemrograman dan driver akan aktif high. Aktif low untuk kran aktif dan aktif high untuk kran mati.

4. Jelaskan cara merangkai mekanik sensor untuk menyensor air jernih atau keruh :



5. Penguat Tidak Membalik (Non Inverting Amplifier)

OP – Amp dapat di pakai sebagai penguat tak membalik, penguat tak membalik adalah penguat dimana tegangan *output* sefasa dengan tegangan *input*. Gambar 2.16 merupakan rangkaian dari penguat tak membalik.



Gambar 2.16 Rangkaian Penguat Tidak Membalik

Apabila tegangan antara terminal *input* (-) dengan terminal *input* (+) menunjukkan 0 (nol) volt pada gambar 2.16, maka besar tegangan *input* (-) sama dengan tegangan *input* (+) terhadap *ground* (GND) yaitu sebesar E1 volt. Arus yang melewati tahanan R1 sebesar :

$$I = \frac{E1}{R1} \text{ ampere}$$

Arah arus tergantung dari *polaritas* tegangan E1. Arus akan melewati tahanan umpan balik Rf, sehingga tegangan pada tahanan Rf diperoleh :

$$V_{RF} = I.\ Rf \text{ volt}$$

Dengan mensubstitusikannya persamaan (2.1) dan (2.2), maka didapatkan :

$$V_{RF} = \frac{E1}{R1}\ .\ Rf \text{ volt}$$

Tegangan *output* (Vo) diperoleh dari penjumlahan tegangan pada R1 dengan tegangan pada Rf, yaitu :

$$Vo = E1 + V_{RF}$$

$$Vo = E1 + \frac{Rf}{R1}\ .\ E1 \text{ volt}$$

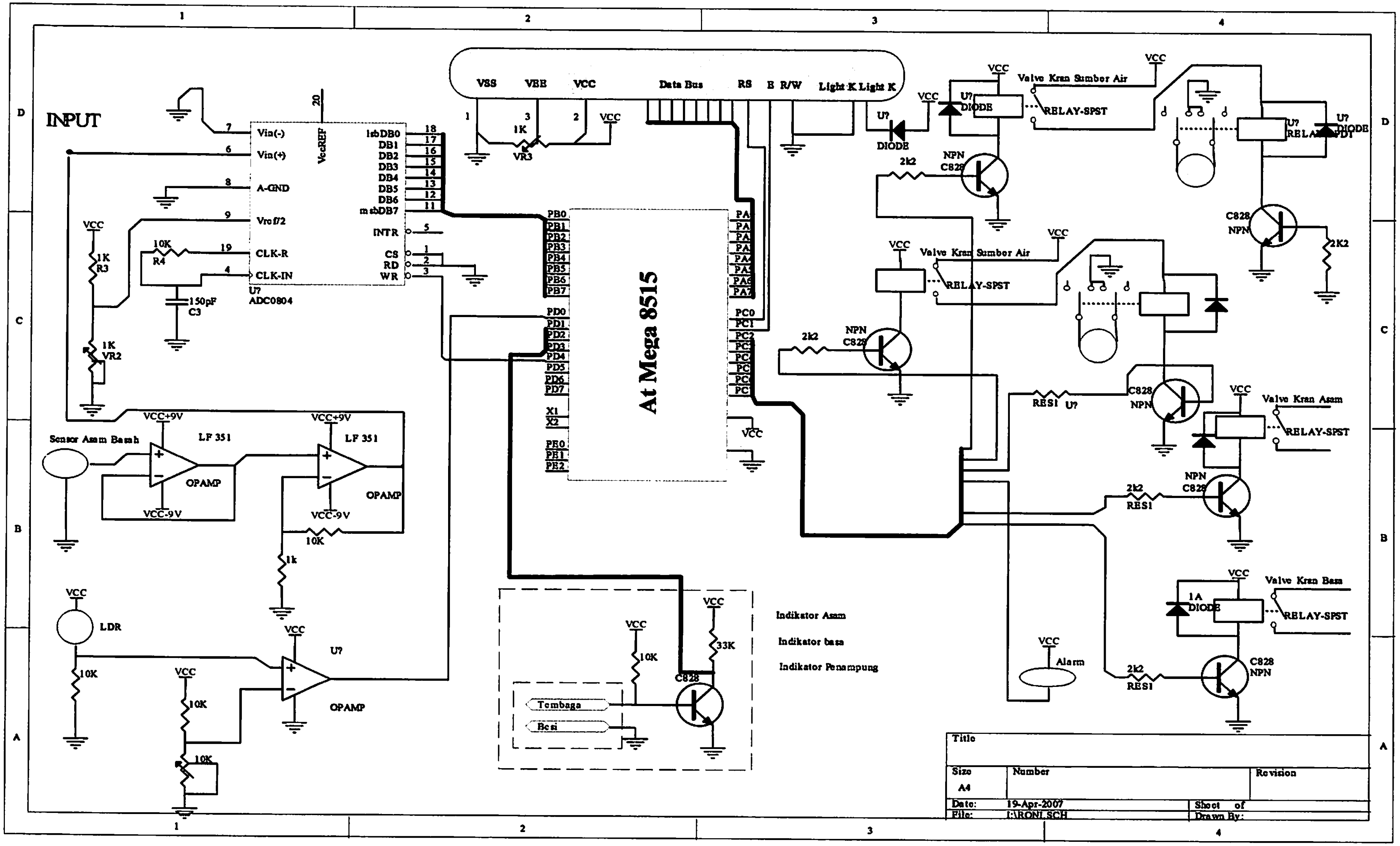
$$Vo = (\ 1 + \frac{Rf}{R1}\ )\ E1 \text{ volt}$$

Besar penguatan diperoleh dari tegangan *output* berbanding dengan tegangan *input,* dimana diperoleh :

$$Ao = \frac{Vo}{E1}$$

$$Ao = (\ 1 + \frac{Rf}{R1}\ )$$

6. Pin 15 LCD berfungsi untuk menebalkan dan menipiskan tulisan atau character pada LCD.


INPUT
Vin(-)
Vin(+)
A-GND
Vref/2
CLK-R
CLK-IN
VccREF
lsbDB0
DB1
DB2
DB3
DB4
DB5
DB6
msbDB7
INTR
CS
RD
WR
U?
ADC0804
10K
R4
150pF
C3
1K
R3
1K
VR2
VCC
VSS
VEE
Data Bus
RS
E
R/W
Light K
1K
VR3
At Mega 8515
X1
X2
Sensor Asam Basah
LF 351
VCC+9V
VCC-9V
OPAMP
10K
1k
LDR
U?
VCC
Tembaga
Besi
C828
33K
Indikator Asam
Indikator basa
Indikator Penampung
Valve Kran Sumber Air
RELAY-SPST
DIODE
NPN
2k2
2K2
RES1
Valve Kran Asam
Valve Kran Basa
1A
Alarm
Title
Size
A4
Number
Revision
Date:
19-Apr-2007
File:
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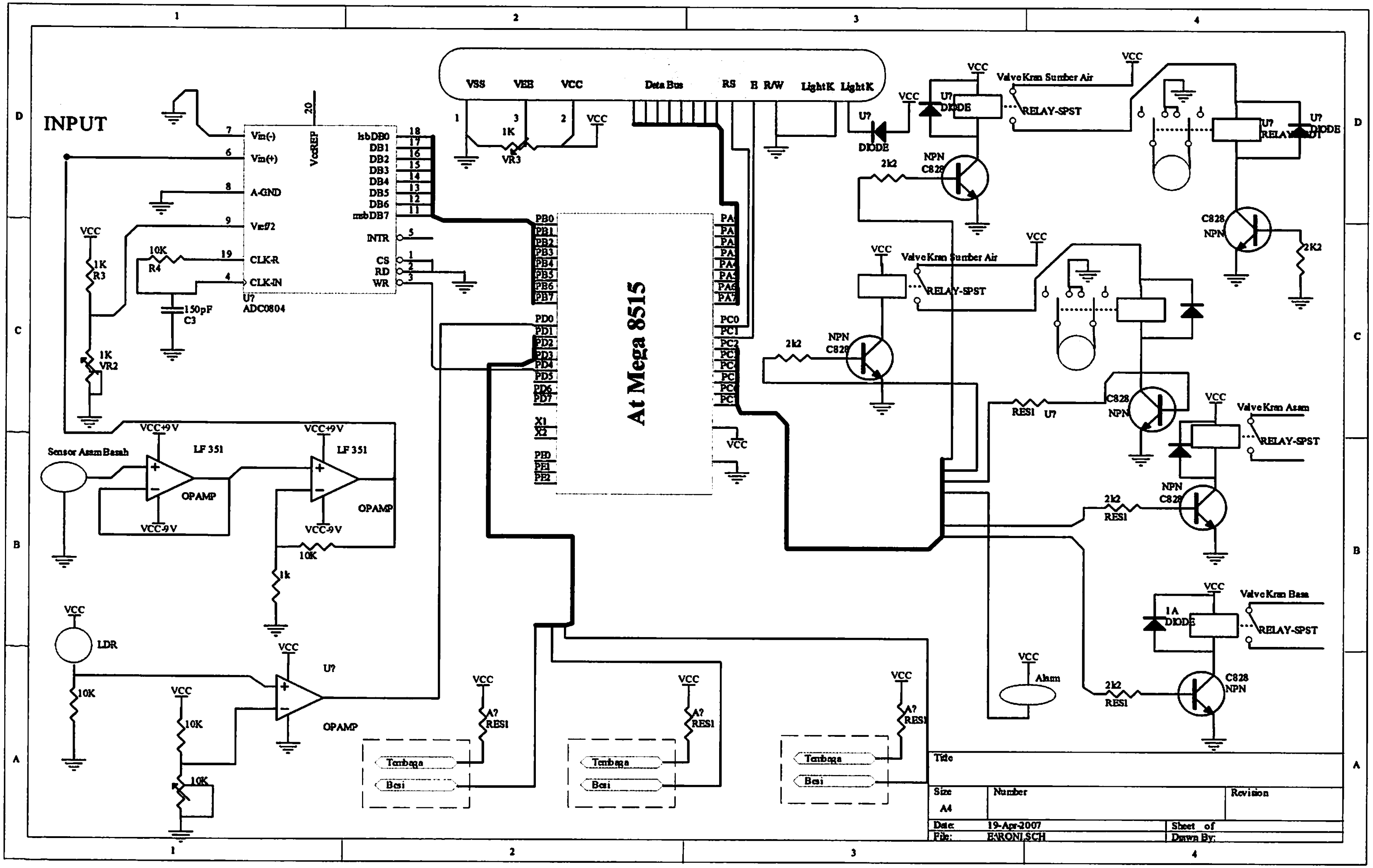
INPUT
Vin(-)
Vin(+)
A-GND
Vref/2
CLK-R
CLK-IN
VccREF
lsbDB0
DB1
DB2
DB3
DB4
DB5
DB6
msbDB7
INTR
CS
RD
WR
U?
ADC0804
10K
R4
150pF
C3
1K
R3
1K
VR2
VSS
VEE
VCC
Data Bus
RS
E
R/W
LightK
LightK
1K
VR3
At Mega 8515
PB0
PB1
PB2
PB3
PB4
PB5
PB6
PB7
PD0
PD1
PD2
PD3
PD4
PD5
PD6
PD7
X1
X2
PE0
PE1
PE2
PC0
PC1
PC2
VCC
Sensor Asam Basah
VCC+9V
VCC-9V
LF 351
OPAMP
10K
1k
LDR
10K
U?
Tembaga
Besi
A?
RES1
Valve Kran Sumber Air
RELAY-SPST
DIODE
NPN
C828
2k2
2K2
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