SKRIPSI

PERENCANAAN DAN PEMBUATAN ALAT PENCATAT DAN PENGANALISAAN KEBUTUHAN BAHAN BAKAR KENDARAAN BERBASIS MIKROKONTROLER AT89S8252

Disusun Oleh :

ANDI ANWAR
NIM 99.17.032

JURUSAN TEKNIK ELEKTRO S-1
KONSENTRASI TEKNIK ELEKTRONIKA
FAKULTAS TEKNOLOGI INDUSTRI
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LEMBAR PERSETUJUAN

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JURUSAN TEKNIK ELEKTRO
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ABSTRAKSI

JUDUL : PERENCANAAN DAN PEMBUATAN ALAT PENCATAT DAN PENGANALISAAN KEBUTUHAN BAHAN BAKAR KENDARAAN BERBASIS MIKROKONTROLER AT89S8252

Disusun oleh : Andi Anwar
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Kata kunci : Penganalisa Bahan Bakar, MC AT89S8252

Pesatnya perkembangan teknologi dewasa ini sangat membantu masyarakat. Dengan adanya teknologi khususnya teknologi di bidang elektronika akan mempermudah dan meringnkan pekerjaan-pekerjaan yang dilakukan manusia. Salah satu contoh system pengukuran secara manual yang masih banyak dilakukan dalam hal ini adalah pengukuran volume bahan bakar pada kendaraan bermotor.

Terkadang sering terjadi seorang pengemudi kehabisan bahan bakar dijalan, oleh karena itu dibutuhkan sebuah alat yang dapat memberikan informasi kapasitas bahan bakar pada kendaraan dan jarak tempuh berdasarkan bahan bakar yang tersisa pada tengki kendaraa sehingga pengemudi dapat merasakan kenyamanan berkendara tanpa rasa khawatir.

Didalam tugas akhir ini, dibahas tentang perencanaan dan pembuatan alat dan penganalisaan kebutuhan bahan bakar kendaraan bermotor berbasis mokrokontroler AT89S8252. Dengan alat ini pengguna kendaraan dapat mengetahui berapa banyak bahan bakar yang ada pada kendaraan dan jarak yang bias ditempuh dengan seven segment sebagai penampil data.

KATA PENGANTAR

Dengan mengucapkan puji syukur kehadirat Tuhan Yang Maha Esa Penulis dapat menyelesaikan skripsi ini karna berkat rahmat-Nyalah Penulis dapat menyusun skripsi ini menjadi salah satu syarat akademik dalam menyelesaikan studi untuk menempuh gelar Sarjana S-1 di Fakultas Teknologi Industri Jurusan Teknik Elektronika di Institut Teknologi Nasional Malang.

Sekripsi ini disusun berdasarkan hasil-hasil percobaan beserta teori dasar dan beberapa pertanyaan dari permasalahan yang ada sehingga Penulisan sekaligus Penyusun dapat menambah wawasan dan tidak hanya menguasai teori saja namun juga memahami pengetahuan tersebut secara teknis.

Tersusun skripsi ini karena adanya dorongan , masukan, juga fasilitas dari pihak-pihak yang berhubungan dengan pelaksanaan dan penyusun skripsi ini. Oleh karena itu penulisan mgucapakan terima kasih yang sebesar-besarnya kepada :

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Namun Penulis sadar bahwa isi dari sekripsi ini masih jauh dari sempurna. Oleh sebab itu kritik dan saran yang membangun sangat Penulis harapkan guna dalam perbakan pada periode mendatang serta sebagai kelanjutan pada studi Penulis *nantinya*.

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Malang, September 2007

Penulis

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BAB I

PENDAHULUAN

1.1 Latar Belakang

Pesatnya perkembangan teknologi dewasa ini sangat membantu masyarakat. Dengan adanya teknologi khususnya teknologi di bidang elektronika akan mempermudah dan meringnkan pekerjaan-pekerjaan yang dilakukan manusia. Teknologi di bidang elektronika telah banyak digunakan baik sebagai alat utama maupunsebagai alat bantu dalam penggerak maupun petunjuk atau indicator. Misalnya dalam bidang industri, perkantoran, alat-alat kedokteran dan peralatan rumah tangga.

Salah satu contoh system pengukuran secara manual yang masih banyak dilakukan dalam hal ini adalah pengukuran volume bahan bakar pada kendaraan bermotor. Pada pembacaan ini pengendara (pengemudi) kurang tahu persis banyaknya volume yang tersisa, karena petunjuk masih menggunakan kode atau batas-batas tertentu, buka nilai dalam jumlah angka yang tepat. Akibat dari permasalahan tersebut, pengendara juga kurang tahu persis berapa lagi jarak yang dapat ditempuh dengan kondisi bahan bakar tersisa pada tengki kendaraan, sehingga seringkali pengendara kehabisan bahan bakar ditengah perjalanan.

Melihat permasaln diatas penulis mencoba membuat suatu alat pengukur dengan petunjuk digital volume bahan bakar sekaligus jarak yang dapat ditempuh, dengan tampilan seven segment.

1.2 Rumusan Masalah

Melihat latar belakang tersebut, maka dapat dirumuskan beberapa permasalahan sebagai berikut:

1) Bagaimana membuat suatu alat sensor untuk mengukur volume bahan bakar dalam jarak yang linier.
2) Bagaimana memanfaatkan IC (Intergreted Circuit) control terprogram AT89S8252 sebagai pengolah dan petunjuk data sensor ke seven segment.
3) Bagaimana cara mengendalikan seven segment sebagai alat penampil karaktar dan dan data secara digital.
4) Bagaimana membuat perangkat lunak yang dapat mengelola data input dan mengeluarkan data output, untuk di tampilkan sebagai petunjuk kapasitas bahan bakar terhadap jarak tempuh yang mudah terbaca.

1.3 Batasan Masalah

Agar dalam pembahasan skripsi ini sesuai yang diharapkan dan tidak menyimpang jauh dari permasalahan, maka perlu adanya pembatasan masalah sebagai berikut:

1) Sensor volume menggunakan sensor yang sudah tersedia pada kendaraan dengan conventer menggunakan ADC (Analog to Digital Converter) 0804.
2) Sensor aliran bahan bakar ke karburator menggunakan sensor flow dengan pendektesian menggunakan optocoupler.
3) sensor kecepatan kendaraan menggunakan optocoupler, sedangkan pendektesiannya langsung pada kilometer (Km) kendaraan.

4) Sistem kontrol AT89S8252 sedangkan penampilan karakter menggunakan seven segment.
5) Mekanik didesain prototype dengan kalibrasi sesuai kondisi standar keadaan.
6) Tidak membahas system mekanik secara mendetail.
7) Bahan bakar yang dipakai adalah bensin.
8) Sensor aliran bahan bakar ke kalburator (sensor flow), modifikasi PDAM.

1.4 Tujuan

Tujuan pembuatan sekripsi ini adalah untuk mengubah sistem pengukurang yang sudah ada (manual), menjadi digital terprogram yang lebih presisi. Sehingga dapat memberikan informasi pada pengemudi, berapa jarak yang bisa ditempuh dari bahan bakar yang tersisa. Hal ini demi kenyamanan pengendara .

1.5 Metodologi

Untuk mencapai tujuan, Langkah-langkah yang dilakukan dalam penyusunan skripsi ini adalah:

1) Mempelajari teori-teori dari perpustakaan baik berupa buku-buku maupun dari tugas akhir dan literatur yang ada.
2) Merencanakan dan membuat alat yang telah direncanakan.
3) Menganalisa hasil perancangan dan mengambil data-data untuk dianalisa guna menentukan tingkat kepresisian alat.
4) Mengambil suatu kesimpulan tentang alat secara keseluruhan.

1.6 Sistematika Penulisan

BAB I PENDAHULUAN

Pendahuluan terdiri dari latar belakang, rumusan masalah, batasan masalah, tujuan, metodologi, sistematika penulisan.

BAB II TINJAUAN PUSTAKA

Bab yang akan membahas dasar-dasar teori yang berhubungan dengan komponen-komponenpada alat yang direncanakan.

BAB III PERENCANAAN DAN PEMBUATAN ALAT

Bab ini akan membahas tentang perencanaan dan proses pembuatan alat secara blok maupun keseluruhan.

BAB IV PENGUJIAN DAN ANALISA ALAT

Pada bab ini akan dibahas tentang pengujian dan analisa hasil perancangan.

BAB V PENUTUP

Penutup berisikan kesimpulan dan saran untuk perkembangan alat lebih lanjut.

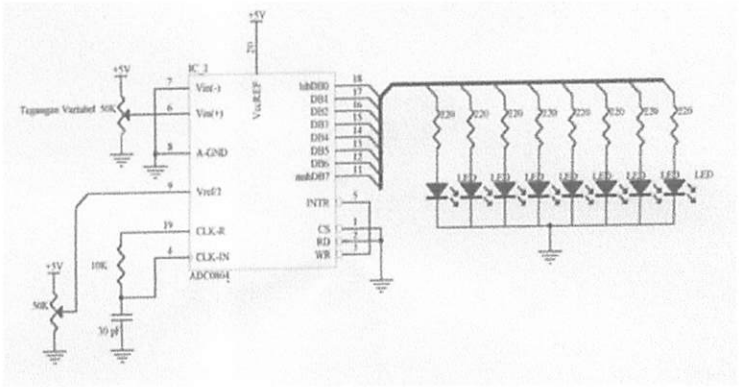
DAFTAR PUSTAKA

LAMPIRAN

b. Alat dan bahan:

- Catu daya +5VDC.
- *Volt* meter *analog.*
- Rangkaian pengujian ADC 0804 dan simulasi outpu*t* dengan LED.

c. Gambar cara pengujian rangkaian ADC 0804 dan LED:



Gambar 4.5. Pengujian Rangkaian ADC 0804

Sumber : Rangkaim pengujian

d. Data hasil pengujian:

Tabel 4.5.

Hasil Pengujian Rangkaian ADC 0804

No	Teg Input	LED1	LED2	LED3	LED4	LED5	LED6	LED7	LED8
1	0 Volt	OFF	OFF	OFF	OFF	OFF	OFF	OFF	OFF
2	1 Volt	OFF	OFF	**ON**	OFF	OFF	OFF	**ON**	OFF
3	2 Volt	OFF	**ON**	**ON**	OFF	OFF	**ON**	OFF	OFF
4	3 Volt	**ON**	OFF	OFF	ON	OFF	**ON**	**ON**	OFF
5	4 Volt	**ON**	**ON**	OFF	OFF	**ON**	OFF	OFF	OFF
6	5 Volt	**ON**	**ON**	**ON**	**ON**	**ON**	**ON**	**ON**	**ON**

Sumber: Data pengujian

e. Analisis:

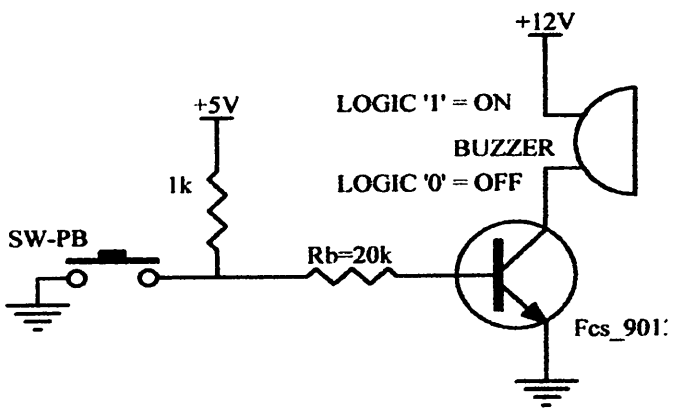
Dari rangkaian diatas dapat dianalisa sebagai berikut:

ADC 0804 dapat mengkonversi tegangan analog dari sensor *volume* bahan bakar, yang sebellumnya terlebih dahulu mengalarni penguatan tegangan

melaiui rangkaian penguatan tegangan. Hasil konversi menandakan, bahwa tiap kenaikan (19,5 mVolt) dari tegangan input, maka *output* ADC akan naik satu digit. Jadi bila. input desimalnya (analog = 5 *Volt),* maka terbentuk data *output* (5/0,0195-256) dengan rumus (2^n) didapat nilai Hex=FF atau 1111111 biner.

4.7 Pengujian *Driver Buzzer*

Pengujian *driver buzzer* sebagai sistem peringatan dini pada pengemudi, jika kondisi bahan bakar medekati habis Yang ditunjukkan pada *seven segment. Buzzer* berbunyi disaat bahan bakar lebeh kecil atau sebanding dengan 5liter dalam tangki. Rangkaian *driver* ini dalam mengoperasikannya seperti tingkah laku sebuah saklar onloff. Bila input basis transistor *driver* diberi masukan logic 'l' atau phus *button* di lepas, maka basis transistor mendapat arus maju, sehingga basis terpicu dan arus kolektor Yang lebuh besar mengalir menuju emitor. Dengan adanya arus mengalir sesuai membuat *buzzer* berbunyi. Kondisi lain jika diberi masukan logika '0' atau phus *button* di tekan pada *input* basis transistor, maka *buzzer* akan mati, hal ini dikarenakan arus kolektor tersumbat.



Gambar 4.6. Pengujian rangkaian driver Buzzer
Sumber: Rangkaian Pengujian

4.8. Pengujian Sistem Secara Keseluruhan Terhadap Objek

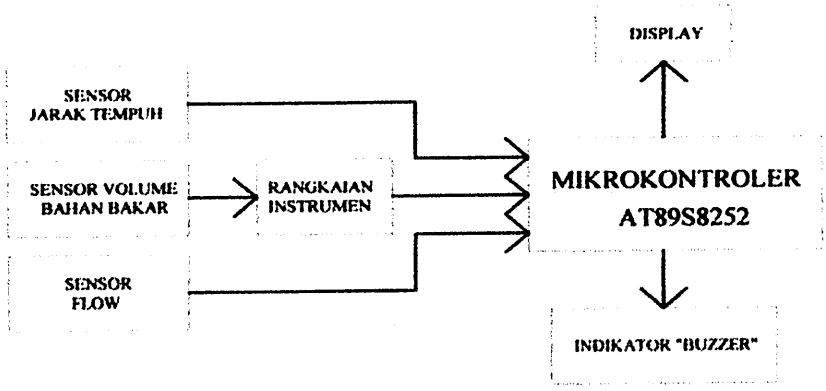
a. Tujuan:

Untuk mengetahui hasil unjuk kerja dari si4em pembaca baban bakar terhadap jarak tempuh, mulai dari blok sensor sampai ke display terhadap objek luar, yakni: sensor bahan bakar, sensor jarak tempuh dan sensorflow.

b. Alat dan bahan:

- Sumbertegangan+5VDCdan+12VDC.
- *Volt* meter *analog.*
- Obyek air sebagai simulasi bensin dan motor DC dilengkapi plat berbentuk piringan pipih dengan satu lubang sebagai simulasi roda motor.

c. Gambar pengujian dari blok rangkaian lengkap atau pengujian keseluruhan dari sistem terhadap objek:



Gambar 4.7. Pengujian Dari Seluruh Blok Rangkaian Terhadap Objek
Sumber: Rangkain Pengujian

BAB II

TINJAUAN PUSTAKA

Dalam bab ini akan dibahas mengenai dasar-dasar teori tiap komponen, yang mendukung dalam perencanaan sistem pengukur dan penunjuk *volume* bahan bakar terhadap jarak tempuh ini. Teori-teori dasar yang menyertainya langsung diambil dari *data sheet* maupun dari studi lapangan dan beberapa buku literatur lainnya.

2.1. Sensor

Sensor merupakan masukan pada kebanyakan sistem instrumentasi baik secara mekanik atau elektrik, hal ini untuk mendeteksi suatu perubahan besaran atau kondisi di lingkungan luarnya. Untuk menggunakan metode dan teknik listrik pada pengukuran, memanipulasi atau pengontrolan, besaran yang bukan listrik (mekanik) diubah menjadi suatu sinyal listrik. Secara sederhana sensor dapat diartikan sebagai alat yang berguna untuk mengubah besaran fisik menjadi besaran elektrik. Misal sensor putaran roda atau putaran sebuah mesin, hal ini berfungsi untuk mengetahui banyaknya sebuah putaran. Dimana putaran berguna sebagai referensi dalant penunjukkan jarak yang sudah ditempuh pada roda ban kendaraan, atau perputaran permenit pada sebuah mesin. Kondisi ini sangat penting dan perlu diketahui untuk meningkatkan efesiensi kendaraan.

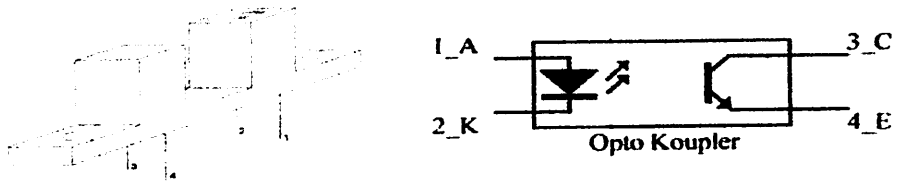
Berdasarkan prinsip kerjanya, macarn-macant sensor putaran dapat dikelornpokkan dalam 2 jenis, yaitu :

- Sensor putaran mekanik.
- Sensor putaran elektrik.

Dari keduanya memiliki persamaan sebagai alat bantu untuk mempermudah mengetahui banyaknya putaran pada sebuah objek (ban dan mesin), sedangkan dari keduanya memiliki perbedaan pembacaan yakni, untuk mekanik atau manual pembacaan dilakukan dengan cara menggunakan kawat putar yang dihubungkan dari objek (ban dan mesin) ke angka-angka penunjuk banyaknya putaran. Sedangkan sensor elektrik dilakukan dengan cara pendeteksian menggunakan sebuah komponen elektrik yang dapat merubah sebuah putaran mekanik, menjadi pulsa-pulsa elcktrik yang mewakili dari sebuah putaran. Sedangkan untuk membaca sinyal pulsa tersebut, digunakan sebuah sistem pengolah data yang menggunakan rangkaian isntrumentasi.

2.2. *Photointerrupter (Optocoupler 4N25)*

Photointernipter atau yang biasa disebut *oplocoupler* merupakan sebuah perangkat elektronik yang terdiri dari dua buah komponen, yaitu LED *(Light Emmiting Diode)* sebagai sumber cahaya *Infra Red* (IR) dan *photo transistor* sebagai penangkap cahaya *Infra Red.* Kekuatan cahaya yang dihasilkan LED tergantung dari arus yang mengalir pada LED tersebut. Sedangkan arus kolektor pada. transistorjuga ditentukan oleh kuat intensitas cahaya IR dari LED tersebut. Berikut ditunjukan bemuk fisik *photointerrupter optocoupler* pada gambar 2. 1.



(a) (b)

Gambar 2. 1. a). Kemasan *Photointerrupter/Optocoupler* 4N25
b). Skema Elektrik Dalam *Photointerrupter*
Sumber: HAMAMAI SU. *DalaSheel*, 2001 : 1

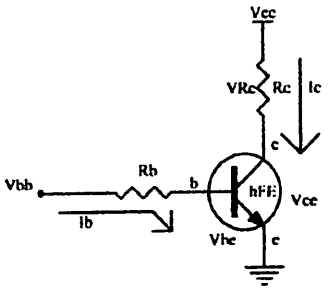
Dalam gambar 2.1. (a dan b) diatas dapat dilihat rangkaian dan bentuk kemasan dari optocompler. Penempatan antara LED dan phototransistor diberi celah udara. yang digunakan untuk melewatkan berkas cahaya dari LED ke photo transistor. Celah kosong ini berfungsi sebagai pendeteksi ada atau tidak-nya objek yang menghalangi cahaya IR ke photo transistor. Cara untuk menghalangi cahaya IR tersebut yaitu dengan memberikan sekat (objek) yang tidak tembus cahaya.

Adapun cara kerja dari optokoupler ini yaitu, bila cahaya dari LED terhalang maka photo transistor tidak dapat bekerja atau tersumbat (cutoff), sehingga arus kolektor tidak mengalir, Sebaliknya jika cahaya dari LED tidak terhalang maka transisitor akan bekerja (caturation) schingga akan mengalir arus kolektor. Sehingga tegangan V_{cc}, mendekati nol (± 0,2Volt) kondisi ini akan memberi interupsi pada sistem kontrol, sehingga oplocoupler ini juga disebut sebagai komponen photointerupter.

2.3. Transistor

Transistor merupakan salah satu dari komponen aktif yang sering sekali digunakan dalam setiap rangkaian elektronika. Beberapa fungsi transistor yaitu : dapat digunakan sebagai rangkaian *driver* ataupun sebagai saklar. Rangkaian

driver merupakan suatu rangkaian yang digunakan untuk menggerakkan suatu peralatan lain yang membutuhkan arus atau tegangan yang lebib besar. Dalam rangkaian *driver* ini kaki basis transistor dikontrol dengan memberi pulsa rendah dan pulsa tinggi. Rangkaian *driver* ditunjukkan dalarn garnbar 2.2:



Gambar 2.2. Transistor Sebagai Saklar
Sumber: Wasito S, Vademekum, 1984: 91

Dalam gambar terlihat V_{bb} akan memberi tegangan maju kepada dioda emitor melelui resistor R_b. Untuk sebuah transistor *silikon* memiliki tegangan hambat pada V_{be} sebesar 0,6 Volt, sedangkan transistor *germanium* V_{be} *0,7 Volt.* Arus basis dan *koleklor* (I_c) ditentukan dengan persamaan.

$$I_c = \frac{V_{cc} - V_{ce}}{R_c} (Ampere) \qquad (2\text{-}1)$$

$$I_b = \frac{V_{bb} - V_{be}}{R_b} = \frac{I_c}{h_{fe}} (Ampere) \qquad (2\text{-}2)$$

Dimana:

V_{bb} : Tegangan bias basis *(Volt)*

V_{be} : Tegangan basis emitor (Volt)

V_{ce} : Tegangan kolektor emitor *(Volt)*

V_{cc} : Tegangan sumber (Volt)

R_c : Resistor padakolektor (Ohm)

R_b : Resistor pada basis *(Ohm)*

I_c : Arus mengafir pada kolektor *(Ampere)*

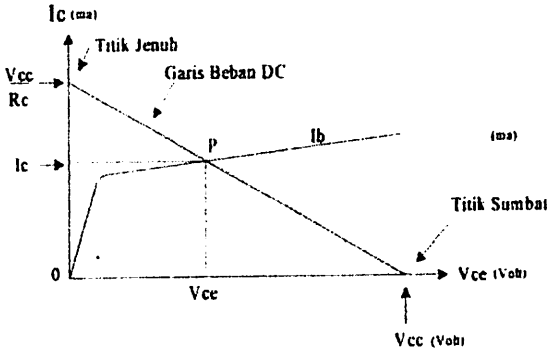
I_b : Arus mengalir pada basis *(Ampere)*

h_{fe} : Penguatan (kati/perkelipatan)

Arus kolektor yang mengalir pada resistor-nya akan menimbulkan tegangan sebesar I_c x R_c. Karena itu tegangan ernitor kolektor menjadi:

$$V_{ce} = V_{cc} - I_c \cdot R_c \text{ (Volt)} \qquad (2\text{-}3)$$

Hubungan antara I_c dan V_{ce} pada garis beban DC dari transistor pada hambatan beban tertentu ditunjukkan pada garnbar 2.3:



Gambar 2.3. Titik Potong Antara Garis Beban dan Arus Basis
Sumber: Wasito S, *Vademekum, 1984: 96*

Garis beban DC tersebut mempunyai titik potong dengan surnbu tegak pada 1. di titik V_{cc} / R_c dan mernotong surnbu V_{ce} pada titik V_{cc} Titik P merupakan titik potong antara garis beban dan arus beban. Pada garnbar diatas tampak bahwa titik potong antara garis beban DC dan kurva I_B pada daerah 0 atau pada sumbu V_{cc} dikenal sebagai titik cut off (sumbat), pada keadaan in i V_{ce}=V_{cc} Sedangkan untuk titik jenuh adalah titik potong kurva In pada ujung teratas pada garis beban DC pada V_{ce} - 0 atau pada sumbu I_c.

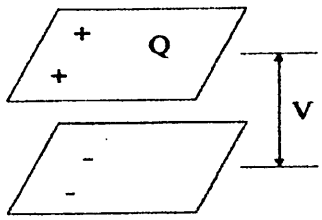
2.4. Kapasitor

Kapasitor adalah sebuah komponen elektrik yang dapat menyimpan sebuah muatan listrik dalam jumlah dan satuan tertentu. Kapasitor disusun dari dua buah lempeng logam yang diantara lempeng diberikan sebuah dielektrikum. Nama sebuah kapasitor ditentukan dari jenis diefektrikum yang di berikannya. Dengan kemampuannya sebagai penyimpan energi listrik, kapasitor dapat digunakan pada rangkaian elektrik sebagai penapisan *(filtering)* atau perata denyut pada sebuah rangkaian penyearah arus bolak-balik. Dapat juga digunakan sebagai penalaan *(tuning)* pada sebauah rangkaian RF *(Radio Frequency),* dan dapat juga sebagai pembagkit frekuensi bersama-sama komponen resistor dan induktor. Selain itu dapat digunakan sebagai pengkopelan sinyal dari suatu sirkuit ke sirkuit lainnya.

Berdasarkan bahan penyusun diantara kedua lempeng logam (dielektrikum) kapasitor dapat dibedakan antara lain

- Kapasitor elektrolit, disustin dari dielektrikum cairan elektrolit
- Kapasitor keramik, dari bahan keramik
- Kapasitor udara, dengan dielektrikum udara bebas

Kapasitor dengan rumus 'C' memiliki satuan terbesar *Farad* berturut-turut microfarad 'μF', nano farad 'nF' dan terkeeil pikofarad 'pF'. Nilai dari sebuah kapasitor ditun.iukkan pada badan komponen. Secara unturn bentuk kapasitor ditunjukkan pada gambar 2.4 berikut :



Gambar 2.4. Bentuk dan Lambang Dari Sebuah Kapasitor
Sumber: Wasito S. flademekum. 1984: 20

$$C = \frac{Q}{V} \text{ (farad)} \qquad (2\text{-}4)$$

dimana :

- Q = banyaknya muatan dalam *Coulomb*
- V = tegangan yang ada di antara keping-keping (Volt)
- C = farad

2.5. *Operational Amplifier (Op-A mp) LM324*

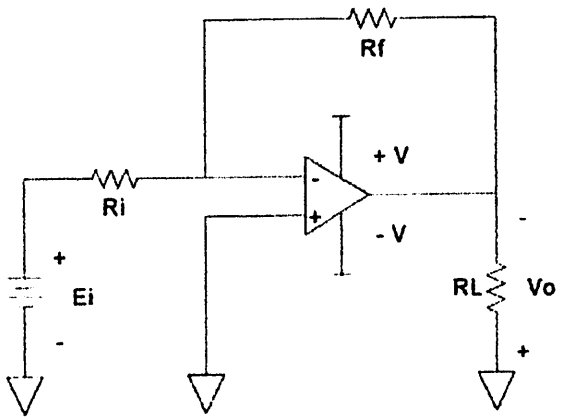
2.5.1. Penguat Pembalik (inverting)

LM 324 adalah,sebuah keping IC yang didalamnya terdapat empat buah gerbang Op-Amp yang masing-masing dapat dioperasikan sendiri. Komponen ini dapat disuplay dengan catu daya tunggal atau *double* tegangan, dari ±5V sampai +15V. Dalam pengoperasiannya Op-Amp dapat digunakan sebagai penguat pembalik, yakni sebuah penguat dengan tegangan keluaran (V_0) fidak sama dengan tegangan masukkannya (E_i), seperti yang diperlihatkan pada garnbar 2.5. Persarnaan tegangan keluaran dari penguat membalik adalah:

$$V_0 = \frac{R_f}{R_i} \text{ x } E_i \text{Volt} \qquad (2\text{-}5)$$

Sehingga diperoleh persarrutan penguatan *(gain)* tegangan adalah:

$$\text{Acl} = \frac{V_0}{E_i} = \frac{R_f}{R_i} \text{ kali} \qquad (2\text{-}6)$$



Gambar *2.5.* Tanggapan Tegangan Vo Terbal ik Terhadap Tegangan Masukan E_i
Sumber: Coughlin, Op-Amp, 1998: 102

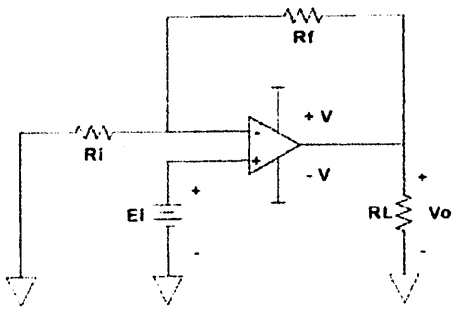
2.5.2. Penguat Tak Membalik (Non Inverting)

Penguat tak membalik adalah penguat yang tegangan keluaran V_0 mempunyai polaritas yang sama seperti tegangan masukannya E_i seperti yang diperlihatkan pada gambar 2.6. Persamaan tegangan keluaran dari penguat tak membalik adalah:

$$\left[1 + \frac{R_f}{R_i}\right] x\, E_i = V_0 \qquad (2\text{-}7)$$

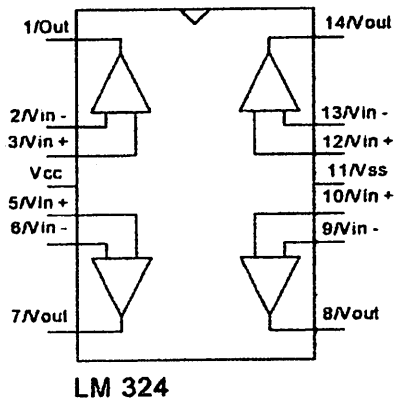
Untuk gain (Acl) adalah :

$$\text{Acl} = \frac{V_0}{E_i} \qquad (2\text{-}8)$$



Gambar 2.6. Tanggapan Tegangan V_0 Terbalik Terhadap Tegangan Masukan E_i
Sumber: Coughlin, Op-Amp, 1998:103

Deskripsi pin dari LM 324 seperti ditunjukkan pada gambar 2.7 berikut:



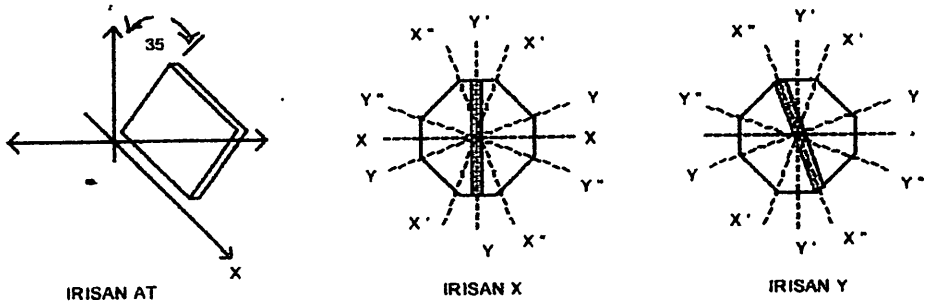
Gambar 2.7. Deskripsi Pin LM324
Sumber : National Data Sheet. 1995

2.6. Kristal

Kristal merupakan sebuah komponen pasif yang digunakan untuk membangkitkan guncangan atau getaran-getaran elektrik, yang dihasilkan dari pergetaran elektron dalam molekul kristal akibat aliran arus listrik. Garam *Rochelle* dan mempunyai aktivitas *piezo-elektrik* (getaran electron akibat aliran arus listrik) yang besar dan lebih kuat dari kwarsa maupun *tourmaline,* namun tourmaline lebih kuat secara fisik. Bentuk alarni dari pada kristal kwarsa adalah prisma, dengan 6 sumbunya diberi nama seperti yang ditunjukkan dalam gambar 2.8 dibawah ini. Untuk memenuhi keperluan kristal ini diris menurut

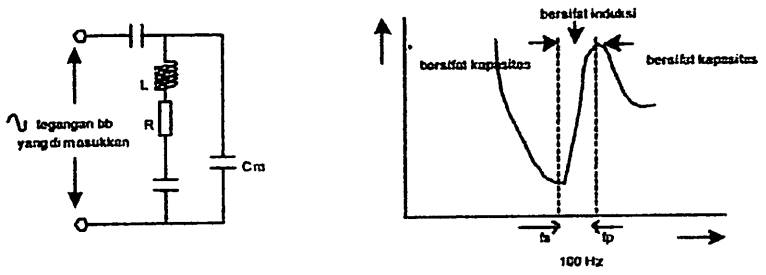
cara-cara tertentu, irisan dinamai irisan-X, irisan-Y, irisan-AT, irisan BT, dan sebagainya. Dimana setiap irisan mempunya karakteristik sendiri-sendiri yang berhubungan dengan frekuensi resonansi, koefisien suhu dan lain sebagainya. Frekuensi resonansi tertingi yang dapat dicapai ditentukan oleh bentuk irisan dan tebal irisan. Namun frekuensi resonansi tidak ter-pengaruh oleh beban. Untuk inenghindari perubahan frekuensi *(frequency drift)*, dipilihiah irisan dengan koefisien suhu nol.

Dalam resonansi, kristal bertingkah sebagai suatu sirkit ternala 'LC'. Oleh karena itu kristal berserta pembungkusnya dapat di ekivalenkan secara elektrik sebagai berikut :



Gambar 2.8. Bentuk Irisan Kristal
Sumber: Wasito S, Vademekum, 1984: 236

Untuk sebuah kristal diperlukan satu pembungkus yang dibuat dari logam dan diantara kristal diberikan logam sebagai kaki kristal untuk keperluan penyolderan.



Gambar 2.9. Rangkaian Ekivalen dari Sebuah Kiistal
Sumber : Wasito S, Tademekum, 1984 : 238

dimana:

- Cm = kapasitas penggenggaman *(mounting)*, dan seclang tidak bergerak
- Cg = kapasitas deeret yang efektif, antara celah udara dan kristal
- L,R,C = ekivalen listrik kristal, apabila seclang bergetar

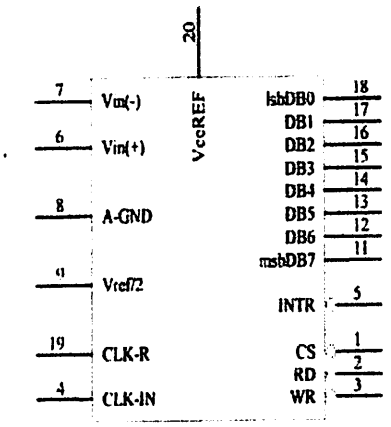
Oleh karena adanya kapasitas Cm yang berjajar dengan kristal, maka sirkit juga mempunyai frekuensi resonansi jajar 'fp'. Frekuensi resonansi deret fs' dan frekuensi jajar 'fp' sangat berdekatan, jaraknya kira-kira 100Hz. Lengkung yang melukiskan fs dan fp adalah sangat tajam, ini berarti sirkit mempunyai factor-Q sangat tinggi sekali saniapai satuan ribu hingga satu juta. Dikarenakan harga-Q tinggi ini maka kristal dapat dipakai sebagai sirkit LC konvensional, apabila diperlukan.

2.7. *Converter Analog to Digital (ADC 0804)*

Apabila dalam suatu sistem elektronik hanya dapat mengolah data dalam bentuk *biner* saja, atau sering disebut pemrosesan besaran *digital*, maka setiap data *analog* yang akan diproses oleh sistem tersebut harus diubah dahulu dalam bentuk kode-kode digital. Jadi untuk menghubungkan sistem *analog* dari kondisi alam luar (sensor) ke dalam sistem rangkaian *digital* dibutuhkan suatu pengubah *(converter)* sistem *analog* ke sistem *digital*, yang biasanya lebih dikenal dengan ADC *(Analog Digital Converter)*. Fungsi dasar dari sebuah *converter* A/D adalah mengubah tegangan *analog* ke dalam kode-kode *biner (digit)*, sehingga dapat diolah oleh system pemrograman.

Tegangan *analog* yang merupakan masukan bagi ADC yang berasal dari transduser melalui penguat operasional, yang *di-inputi* oleh. Tegangan listrik yang

dihasilkan oleh penguat operasional berubah-ubah sesuai dengan perubahaan tegangan pada tranduser. Tegangan *analog* inilah yang kemudian diubah oleh ADC menjadi bentuk *digital* yang sebanding dengan tegangan analog. Pengubah *analog* ke *digital* merupakan jamung dari sistern yang berfungsi umuk mengubah data ke dalam bentuk *digital* sehingga cocok untuk diproses dalam inikrokontroler AT89S8252. Deskripsi pin dari ADC 0804 ditunjukkan pada gambar 2. 10 :



Gambar 2. 10. Konfigurasi Pin ADC 0804
Sumber: National Data Sheet ADC/DAC, 1995: 2-208

Fungsi dari masing-masing pin adalah sebagi berikut:

- **Pin-6 & 7: Vin (+) dan (-)**

  Adalah *input analog* maksimall 5,1 Volt.

- **Pin-9: Vref**

  Tegangan *referensi* untuk menentukan kenaikan *bit* keluaran misalnya diberikan tegangan *referensi* 5,12 Volt, kombinasi yang mungkin dari 8 *bit* keluaran adalah 256d maka kenaikan tegangan per-bit = 256/5,12 = 50 mV, sehingga tegangan input yang bisa dideteksi adalah 50 mVolt dan keluaran digital 0000-000 1 B.

- **Pin_4 & 19 : Clock**

Pin clock tempat memberika pengaturan keserempakaan kerja dalain *internal* circuit ADC yang disarankan adaiah 600KHz dan maksimal 1280KHz.

- **Pin_1: Cs (Chip *Select)***

  Input chip selecl

- **Pin_2: RD *(Read)***

  *Strobe b*aca ekstemal

- **Pin_3: WR (Wilte)**

  Strobe tulis data eksternal

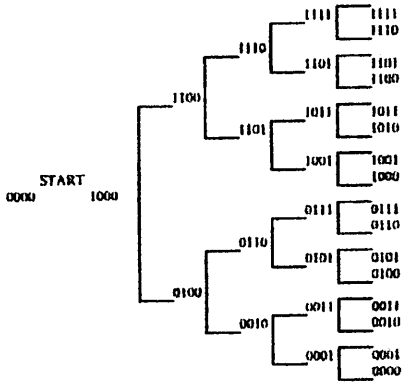
- **Pin_I 8 - 11: DBO - DB7**

  Jalur data *digital* 8 *bit* hasil *conversi* yang dihubungkan dengan data *bus.*

- **Pin_: 5INT**

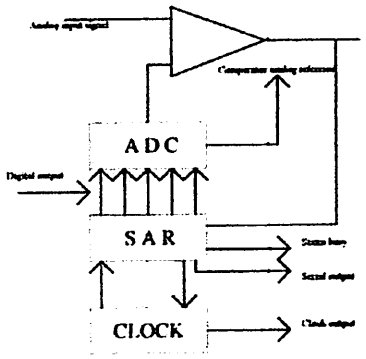
  Output internal.

ADC 0804 ini adalah jenis SAR *(Successive Approximation Regisfer)* memiliki rangkaian yang lebih kompleks dibandingkan dengan jenis ADC lainnya. Dikatakan demikian karena *coverter* jenis ini, untuk peralatan konversi tidak menggunkan *counter* untuk memberikan *input* blok *converter digital* ke analog yang mengontrol kerjanya sendiri. Keuntungan utama dari pemakaian SAR ini adalah dengan resolusi bitnya terletak pada selang waktu 'n' buah pulsa. *Clock* untuk konversi rangkaian utamanya terletak pada *register* yang mempunyai keluaran digilal seperti pada gambar 2.11:



Gambar 2.11. Sistem Operasi SAR
Sumber: Rangkaian Digital, 1995: 75

Pada awal *start* konversi akan aktif, di mana akan meng-*clear* data sebelumnya, pada saat MSB *(Most Sign~fican Bit)* "1" apabila kontrol register ini menyatakan keluaran kurang besar, maka bit yang di-set tetap, pada bit berikutya kentudian di-set. Sebaliknya apabila kontrol menyatakan keluaran terlalu besar, maka *bit* awal yang di-*set* akan di *reset* kembali dan *bit* berikutnya akan di-*set*. Urutan ini akan dikerJakan terus sampai urutan *bit* yang terakhir, hingga data digital yang paling sebanding dengan tegangan analog-nya.



Gambar 2.12. Blok Diagram Approximation Register
Sumber: William D cooper. 1993 : 45

Dari gambar 2.12. diatas dapat dianalisa, mula-mula dari register mempunyai harga digital tengah mempunyai keluaran MSB set =1 dan diberi ke

konverter digital ke analog yang mempunyai keluaran tegangan yang diumpankan pada komparator. Apabila tegangan ini lebih kecil dari komparator, maka keluarannya menjadi logic "1" yang akan mengontrol SAR supaya men-*set bit* berikutnya sehingga keluaran menjadi besar.

Dalam keadaan sebaliknya, keluaran komparator akan menjadi "0" yang akan mengontrol SAR supaya me-reset bit yang barn di-set, dan men-set bitberikutnya agar kekuaran konverter digital ke analog menjadi lebih keeil. Metode SAR memiliki keunggulan di bandingjenis ADC lain:

- Waktu konversi lebih cepat.
- Mempunyai waktu resolusi yang lebih tinggi untuk diatas 12 bit.
- Waktu konversi yang tetap tidak tergantung tegangan input.
- Masing-masing output tidak tergantung pada output sebelumnya, kondisi ini terjadi sebab *output* sebelumnya telah di-*clear*-kan atau di-*set* sebelumnya melakukan konversi baru. Semakin banyak jumlah *output*-nya, berarti makin baik resolusinya dan ketuampuan membedakan *level* tegangan makin baik. Untuk membedakan resolusi atau *persen* resolusi dari ADC dapat dicari dengan rumus:

$$\text{Re } solusi = \frac{1}{2^n} xE \qquad (2\text{-}9)$$

Dimana:

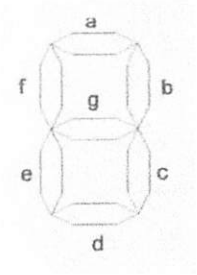
E = Tegangan *analog* skala penuh.

N = Jumlah bit *digital.*

Sedang prosentase resolusinya = $\frac{1}{2^n} x$ 100 %.

2.8. *Display Seven Segment*

Pada dasamya *display, seven segment* terdiri dari 7 (tujuh) dioda yang tersusun membentuk suatu konfigurasi angka. Terdapat dua macam *seven segment, y*aitu *common anoda* dan *common kaloda.* Pada *common anoda b*erarti anoda-anoda tersbut dihubungkan menjadi satu dan diberi tegangan *high,* sehingga untuk mengaktifkan dioda tersebut pada katodanya diberi tegangan low, Sebaliknya *common katoda* berarti katoda dari dioda-dioda *seven segmeHI* dihubungkan menjadi satu dan diberikan tegangan *high,* seperti pada table kebenaran, sedangkan konstruksi dari *sevenscgment* terlihat pada gamlbar 2.13:



Gambar 2.13. *Displqv Seven Segment*
Sumbcr : Dasar-Dasar Sistcm Digital

Tabel 2. 1. Konfigurasi *Displqy Seven Segment Common Anoda*

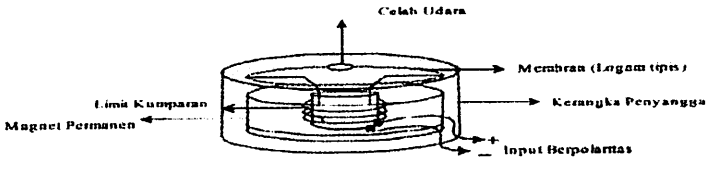
DEC	KONFIGURASI							HEX
	G	F	E	D	C	B	A	
0	1	0	0	0	0	0	0	40
1	1	1	1	1	0	0	1	79
2	0	1	0	0	1	0	0	24
3	0	1	1	0	0	0	0	30
4	0	0	1	1	0	0	1	19
5	0	0	1	0	0	1	0	12
6	0	0	0	0	0	1	0	02
7	1	1	1	1	0	0	0	78
8	0	0	0	0	0	0	0	00
9	0	0	1	0	0	0	0	10
Blank	1	1	1	1	1	1	1	7F

Sumber : Dasar-dasar Sistem digital

2.9. *Buzzer*

Buzzer adalah sebuah komponen yang digunakan untuk menghasilkan getaran suara (bunyi-bunyian) dengan frekuensi tinggi untuk pendengaran manusia. Dimana getaran suara ini dibasilkan dari getaran-getaran listrik yang diatirkan pada suatu kumparan yang diletakkan dalam suatu medan magnet permanen. Untuk menghasilkan suatu bunyi, kumparan direkatkan pada sebuah membran yang terbuat dari lembaran logam tipis yang melingkar. Dari getaran membran inilah udara akan bergetar sebanding dengan frekuensi arus listrik yang mengalir pada kumparan. Dimana getaran listrik disesuaikan dengan pendengaran manusia maksimal 20kHz (frekuensi audio), sehingga mampu didengar olch telinga manusia. Namun jika getaran listrik tersebut diatas getaran audio, maka getaran suara tersebut dinamakan getaran suara ultrasonik yang umumnya didegar oleh hewan tertentu.

Buzzer memiliki karakteristik yang berbeda-beda tergantung dari penggunaan. Karakteristik dari *buzzer* umunya dinyatakan dengan tegangan yang diterapkan padanya dalam satuan Volt, dan kuat frekuensi dalarn desibel (dB). *buzzer* memiliki polaritas (+ dan -) dalam pernasangannya, hal ini clikarenakan ada sebagaian buzzer didalamnya sudah diterapkan komponen pembangkit frekuensi. Gambar sistern *buzzer* secara umum seperti ditunJukkan dalam gambar 2.15 dibawah ini:



Gambar 2.15. Bentuk Fisik *Buzzer*
Sumber: Anonimous

2.10. Mikrokontroler AT89S8252

2.10.1. Pendahuluan

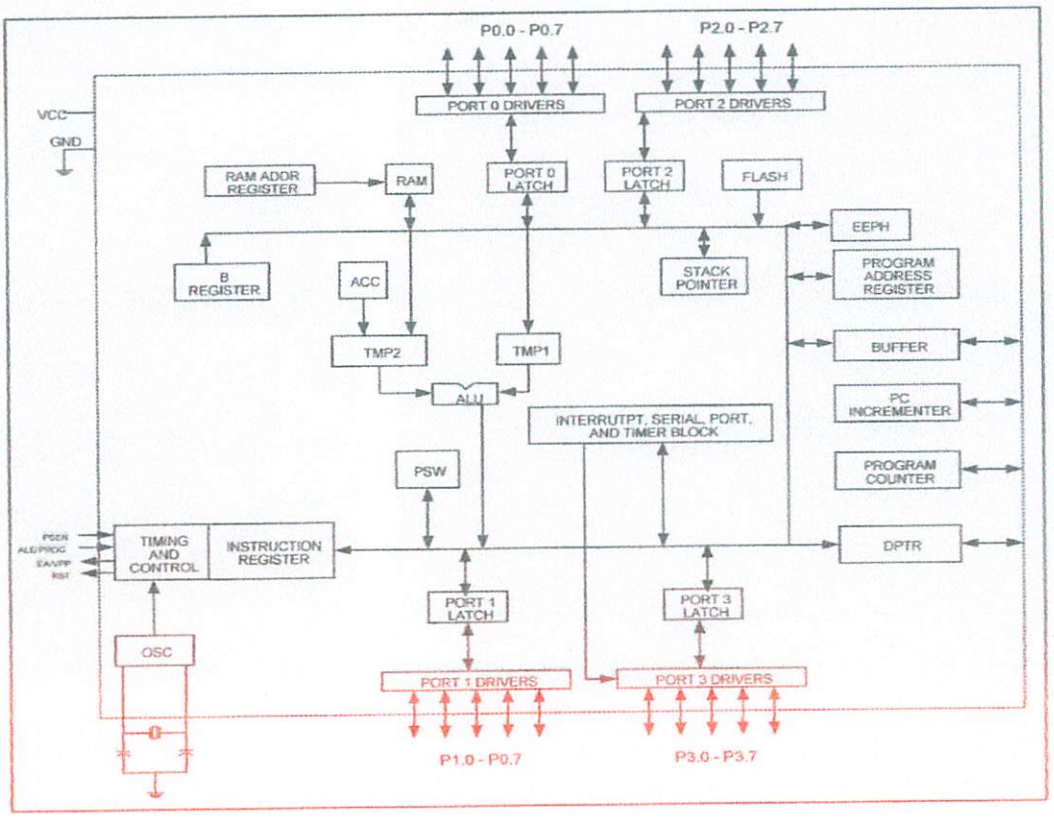
Perbedaan mendasar antara mikrokontroler dan milcroprosesor adalah jika mikrokontroler selain memiliki CPU *(Central Processing Unit)* juga dilengkapi dengan memori dan 1/0 *(Inpul/Output).* Maka mikrokontroler dapat dikatakan sebagai *microcomputer* dalam keping tunggal *(single chip microcomputer)* yang dapat berdiri sendiri.

Mikrokontroler AT89S8252 adalah mikrokontroler keluarga MCS-51 yan,g inembutuhkan daya rendah, memiliki kemampuan yang tinggi, dan merupakan mikrokomputer 8 bit yang dilengkapi 8K *byte Flash* PEROM *(Programmable and Erasable Read Only Memory)* yaitu ROM yang dapat ditulis uiang atau dihapus menggnakan sebuah perangkat *programmer.* Serta terdapat EPROM *internal* sebesar 2k *gvte.*

Flash PEROM dalam AT89S8252 menggunakan *Atmel's High-Density Non Volatile Technology* yang mempunyai kemampuan untuk ditulis ulang hingga 1000 kali dan berisikan perintah *standard* MCS-5 1. Selain itu juga dilengkapi RAM *internal* sebesar 256 *byte..* Dalam sistem Mikrokontroler terdapat dua hal yang mendasar, yaitu: perangkat keras dan perangkat Itmak yang keduanya saling terkait dan mendukung.

2.10.2. Perangkat Keras Mikrokontroler AT89S8252

Blok diagram mikrokontroler AT89S8252 secara umum seperti ditunjukkan dalam gambar16:



Gambar 2.16. Blok Diagram Mikrokontroler AT89S8252

Sumber: Paulus Andi Nalwan. 2003 : 2

- *CPU 8 bit*
- *8Kbyte FLASH PEROM*
- *2 Kbyte EEPROM*
- *Memory 256 x 8 bit Internal RAM*
- *32 Port I/O Lines*
- *3 Timer clan Counter 16 bit*
- *9 Sumber Interupsi*
- *SPI serial interface*
- *Oscillator dan clock maksintal 24MHz*
- *Programmable Watchdog Timer*
- *Programmable UART Serial Chanel*
- *Dual Data Pointer*

- *Power-Off Flag*

2.10.2.1. Arsitektur AT89SS252

Arsitektur Mikrokontroler AT89S8252 adalah sebagai berikut:

1). CPU (Central Processing Unit) 8 bit dengan register A (Accumulator) & B

2).16-bit Program Counter (PC) dan (Data Pointer) DTPR.

3).8-bit Program Status Word (PSW).

4).8-bit Stack Pointer (SP).

5).8 khyte Flash PEROM internal.

6).256 byte internal RAM.

- 4 bank register, masing-masing berisi 8 register.
- 16 kvte yang dapat dialamati pada bit-level.
- 208 byte general purpose memory data.

7).32 pin input-output tersusun atas P0-P3. masing-masing 8-bit.

8).3 buah timer (T0 & T1) dengan masing-masing 16-bit timerl counier.

9).Receive.rltrammiter data secara serial *full duplex*: Serial bqffer (SBUF).

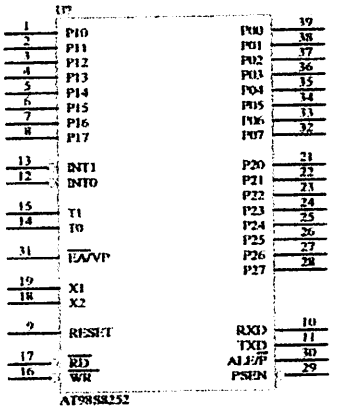
10). Control register: TCON, TMOD, SCON, PCON, I P & IE.

11). 9 buah sumber interupsi (4 sumber interupsi external dan 5 sumber internal

12). Oscillator dan clock internal.

2.10.2.2. Konfigurasi Pin Mikrokontroler AT89S8252

Konfigurasi kaki-kaki mikrokontroler terdiri dari 40 pena, seperti terlihat pada gambar 2.17:



Gambar 2.17. Diagram Pin Mikrokontroler AT89S8252
Sumber: Paulus Andi Nalwan, 2003: 90

Fungsi dari tiap-tiap pena adalah sebagai berikut:

- **Pin-40- Vcc** (sumber tegangan).
- **Pin-20:** GND *(Ground).*
- **Pin-32-39: Port-0: ***

  Merupakan port *input-output* dua arah dan dikonfigurasikan sebagai multipleks bus data dan alamat rendah (AO-A7) program dan data *external.*
- **Pin-1-8: Port-1:**

  Merupakan port *input-output* dua arah dengan *internal pull-up.*
- **Pin-21-28: Port-2:**

  Merupakan port *input-output* dengan *internal* pull-up. Mengeluarkan *address* tinggi selama pengambilan *(felching) program memory external.*
- **Pin-10-17: Port-3:**

  Port *input-output* dengan *internalpull-up,* dan memiliki fungsi khusus yaitu:

RXD (P3.0) Port *input serial.*

TXD (P3. I) Port *output serial.*

fNTO (P3.2) *Interrupt 0 external.*

INTI (P3.3) *Interrupt I external.*

TO (P3.4) *Input external timer 0.*

T I (P3.5) *Input external timer 1.*

T2 (P3.5) *Input external timer 2.*

WR (P3.6): *Strobe* tulis data *memory external.*

RD (P3.7) : Strobe baca data *memory external.*

- **Pin-9: RST *(Reset):***

  Input reset berfungsi *me-reset CPU* saat sumber tegangan dibidupkan.

- **Pin-30: ALE/PROG *(Addrcss Latch Enable)lPrograinming:***

  Pulsa ALE digunakan umuk *'latching' byte address low* selama pengaksesan ke *external memorv* dan memasukkan pulsa selama pemrograman.

- **Pin-29: PSEN *(Program Store Enable):***

  Merupakan *strobe* baca ke program *memory external.*

- **Pin-31: EA/VPP *(External Address):***

  EA low jika mengakses *memory external.*

  Untuk mengakses *memory internal* maka EA dihubungkan ke-Vcc (+5V).

- **Pin-18-19: XTALI dan XTAIL2:**

  Dihubungkan dengan kristal bila menggunakan *oscillator internal.* XTALI *input inverting oscillator amplifier,* XTAL2 merupakan *output inverting.*

2.10.2.3. Organisasi Mernori

Dalarn mikrokontroler AT89S8252 ruang alamat telah dibedakan untuk program memori dan data memori.

2.10.2.4. Perangkat Lunak Mikrokontroler AT89S8252

2.10.2.4.1. *Internal Program Memory*

Mikrokontroler AT89S8252 memiliki *program memory internal* sebesar 8Kbyte dengan ruang alamat 0000H-IF40H. Jika alamat-alamat program lebih tinggi dari pada. 1F40H dimana melebihi kapasitas ROM *internal,* menyebabkan AT89S8252 secara otornatis mengambil kode *byte* dari program memori *external.* Kode *byte* juga dapat diambil hanya dari *external memory* dengan alamat 0000H-FFFFH dengan cara menghubungkan pin EA ke *ground.*

2.10.2.4.2. *Internal Data Memory (RAM)*

Ruangan alamat memori data *internal* (RAM) dengan kapasitas 256 *byte* yaitu: 00H-FFH yang terbagi atas 3 daerah, yaitu:

1. *Bank regitler:*

   Setiap *bank* terdiri dari 8 *register* (R0-R7) sehingga. jum lah *register* untuk keempat *bank register* menjadi 32 buah *register* yang menempati ruang alamat 00H-IFH. Mengaktitkan salah satu *bank register* dapat dilakukan dengan mengatur RS0-RS I pada *ProgramStalus Word (PSW).*

2. *Bit Addrc ssable:*

   Terdiri dari 16 *byte* yang berada pada alamat 20H-2FH. Masing-masing bit dalam 232 *hit* yang lokasinya dapat dialamati secara langsung.

3. RAM *Generalpurpose*

   Terdiri atas 232 *byte* yang menempati alamat 30H-FFH, dan dapat dialamati secara langsung maupun tak langsung dalam penggunaan untuk keperluan umum *(general purpose).*

Tabel 2.2. Pengaturan RS0-RS I *Bank Register*

RSI	*RSO*	Selec Register Bank
1	*0*	*Bank 0*
0	*1*	*Bank I*
1	*0*	*Bank* 2
1	*1*	*Bank* 3

Sumber: Paulus Andi Nalwan, 2003 : 12

2.10.2.4.2.1. SIFR *(Special Function Register)*

Untuk operasi AT89S8252 yang tidak menggunakan alamat *internal* RAM (00H-FFH). Beberapa dari *register-register* ini juga mampu dengan pengalamatan *bit* sehingga dapat dioperasikan seperti yang ada pada RAM yang lokasinya dapat dialamati dengan pengalamatan *bit.*

2.10.2.4.2.2. *PSW (Program Status Word)*

Cara mendefinisikan *register PSW* ini menggunakan tabel 2.4 berikut:

Tabel 2.3. Pengaturan RS0-RS I *Bank Register*

Data	Simbol	Posisi	Fungsi /Arti
D0	P	PSW.0	*Parity flag*
DI	-	PSW.I	*Flag* didefinisikan oleh pemakai.
D2	OV	PSW.2	*Overflow,Flag*
D3	RS0	PSW.3	*Bit* pemilih *bank regisler*
D4	*RSI*	PSWA	*Bit* pemilih *bank register.*
D5	*F0*	PSW.5	*Flag 0*
D6	AC	PSW.6	*Auxiliary CarryFlag*
D7	*CY*	PSW.7	*Carry Hag*

Sumber: Paulus Andi Nalwan, 2003 : 12

2.10.2.4.2.3. PCON (Power Control)

Sedangkan cara untuk mendefinisikan *register* PCON ini menggunakan tabel 2.5 berikut:

Tabel 2.4. Skema Mendefinisikan PCON

Data	Simbol	Fungsi /Arti
D0	IDL	*Idle* mode *bil*
DI	PD	*Power Down bit*
D2	6F0	*Bit flag* serbaguna.
D3	GF1	Bit serbaguna.
D4	-	Tidak dipakai.
D5	-	Tidak dipakai.
D6		TWA dipakai.
D7	SMOD	Digunakan untuk menghasilkan *baudrate* dan SMOD_1,maka *baudrate* akan *double* baik mode 0, 1,2 atau 3.

sumber : Pauius Andi Nalwan, 2003 : 17

2.10.2.4.2.4. Sistem Interupsi

Mikrokontroler AT89S8252 mempunyai 5 buah sumber *inferrupt yang* dapat mengakibatkan permintaan *interrupt,* yaitu: INT0, FNT1, T0, T1, T2 dan *port serial.* Saat terjadi *-interrupt* mikrokontroler secara otomatis akan menuju ke *subrutin* pada alamat tersebut. Setelah *interrupt service* selesai dikerjakan, mikrokontroler akan mengerjakan program semula. Sumber *external interrupt* adalah INT0, INT1, dimana kedua interupsi *external* ini akan aktif pada transisi rendah selain itu juga ada *timer/counter* 0, *timer/counter* 0 dan interupsi dari port serial *(recivier).*

Interupsi serial dibangkitkan dengan melakukan operasi OR pada Rl dan T1. Tiap-tiap sumber interupsi dapat *di-enable atau di-disable* secara *software.*

Tingkat prioritas semua sumber interupsi dapat diprogram sendiri-sendiri dengan *set* atau *clear bit* pada SFR IP *(Interrupt Priority).*

Tabel 2.5. Alamat Sumber Interupsi

Sumber *Interrupt*	Alamat Awal
Power On Reset	0000h
interrupt luar 0 (INT 0)	0003h
Pewaktu/pencacah 0 (T0)	000Bh
Pewaktu/pencacah 1 (TI)	001Bh
Pewaktu/pencacah 2 (T2)	002Bh
Interrupt luar 1 (INT 1)	0013h
Port I/O *Serial*	0023h

Sumber :Paulus Andi Nalwan, 2003 : 53

Register yang berperan dalam mengatur akfif tidaknya interupsi adalah *interrupt enable register,* berikut tabel susunan dad *bit-bit* beserta kegunaannya:

Tabel 2.6. Kegunaan *Interrupt Enable Register*

Data	Simbol	Posisi	Fungsi /Arti
D0	EX-0	IE.0	Diatur secara *sqftware* untuk interupsi dari INT 1
Dl	ET0	IE.1	Diatur sccara *sqftware* untuk interupsi dari *limer1counler 1.*
D2	EXI	IE.2	Fi-atur secara *softwure* untuk interupsi dari INT 1.
D3	ET I	IE.3	Diatur secara *softwure* untuk interupsi dart *litner counter 1.*
D4	ES	1E.4	Untuk mengatur *enable* atau *disables* suatu interupsi R 1 /TL
D5	-	IE.5	Kosong
D6	-	IE.6	Kosong
D7	EA	IE.7	Jika diatur 0 maka semua interupsi *di-disable, jika* diatur 1 maka interupst diatur *di-disable atau di-emble* menurut masing-masing *bit.*

Sumber : Paulus Andi Nalwm, 2003 : 51

2.10.2.4.2.5. *Timer / Counter*

Pengendalian kerja dari *timer/counter* dilakukan dengan pengaturan *register* yang berhubungan dengan kerja dari *timer/counfer* yaitu melalui sebuah *timer/counter mode control.* Untuk mengaktitkan *timer/counter* yang meliputi penentuan fungsi sebagai *timer* atau sebagai *counter* serta pemilihan *mode* operasi dapat diatur melalui TMOD seperti ditunjukkan dalam label 2.8:

Tabel 2.7. *Register* TMOD

Data	Simbol	Posisi	Fungsi /Arti
D0	ITO	TCON.0	Interrulv 0 ope control bit.
D 1	IE0	TCON.1	External interrupt 0 *edge flag*
D2	ITI	TCON.2	Interrupt typel control bit. Diatur oleh software untuk menentukan akfif low alau high trigger dari external.
D3	IEI	17CON.3	External interrupt I edge flag. Diatur oleh hardware ketika external interrupt terdeteksi dan nol-kan melalui softtware ketika interrupt diproses.
D4	*TR0*	TCON.4	Timer 0 control bit. Diatur oleh soflawre ketika timer/ counter 0.
D5	TF0	TCON.5	Timer 0 *overflow plag* control bit. Diatur oleh *software* ketika *timer/counter 0 overflow*
D6	*TR 1*	TCON.6	Timer 1 control bit. Diatur oleh software ketika timer/ counter 0.
D7	TF1	TCON.7	Timer 1 overflow flag control bit. Diatur oleh software ketika timer1counter 0 oferflow.

Sumber : Paulus Andi Nalwan, 2003 : 13

Tabel *2.8. TimerlCounter Mode Control Register*

Data	Simbol	Fungsi /Arti
D0	Timer *0;* M0 (0)	Untuk rnemilih mode timer
D I	Timer 0; M 1 (0)	Untuk mmilih mode timer.
D2	Timer 0 ; C/T (0)	1 = Counter & 0 = Timer
D3	Timer 0; GATE (0)	Timer akan berjalan jika bit di set dan INT0 (untuk Timer 0) atau INT1 (untak Timer 1)
D4	Timer 1-2; M0 (1)	1 Intuk mernilih mode timer.
D5	Timer 1-2; M1 (1)	Untuk memilih mode timer.
D6	Timer 1-2; C/T (0)	1 = Counter & 0 = Timer
D7	Timer 1-2; GT (1)	Timer akan berjalan jika bit di set dan INT0 untuk Timer 0) atau INTI (untuk Timer 1)

Sumber: Paulus Andi Nalwan, 2003 : 32

Tabel *2. 9.. Mode Operasi TinterlCounter*

M 1	*M0*	*Operating Mode*
0	0	Timer 13 bit
0	1	Timer/Counter 16 bit
1	0	8 bit Auto reload Timer /Counter
1	1	TL0 dari Timer adalah 8 Bit Timer/Counter dikendalialan oleh control bit Timer 0. TH0 adalah 8 bit yang dikendalikan oleh Timer 1 control bit.

Sumber : Paulus Andi Nalwan, 2003 : 33

2.10.2.4.2.6. Metode Pengalamatan

1. Pengalamatan *bit (Direct Bit Addressing):*

   Pengalamatan langsung flap, *hit* hanya dilakukan pada lokasi RAM *internal* yaitu 20H-2FH, dan sebagian SFR yaitu: port 0, port 1, port 2 port 3, TCON *regisler,* SCON *register, IE rcgister, PSW regisfer, ACC* dan B *register.*

2. Pengalamatan tak langsung *(Indirect Bit Addressing) :*

   Pada pengalamatan tak langsung, instruksi menunjukkan suatu *register* yang isinya adalah alamat dari *operand, eksternal* dan *internal* RAM dapat alamati secara tidak langsung. *Register* alamat untuk data dengan lebar 8 *bit* dapat berupa R0 dan R1 yang digunakan untuk memilih angka *register* atau *slack pointer. Register* alamat untuk data dengan 16 *bit* untuk (DPTR).

3. Pengalamatan berindeks :

   Yang dapat diakses dengan pengalamatan berindeks hanya *memoryprogram.* Mode ini dimaksudkan untuk membaca look-up *table program-*

4. Konstanta *immediat :*

   Pengalamatan langsung dilakukan dengan memberikan nilai ke suatu *register* secara langsung, dilakukan dengan menggunakan tanda (#) contoh:

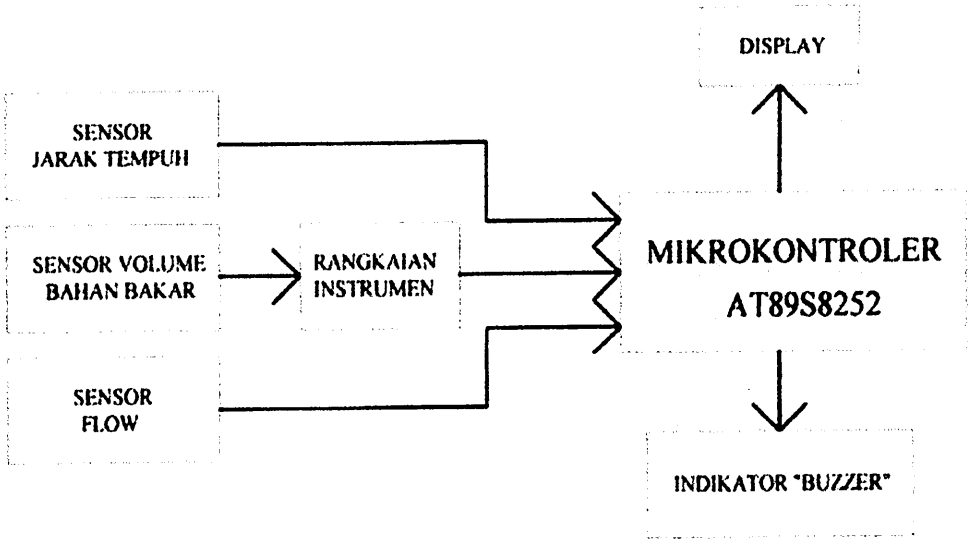
   Mov A,#OFFH ;copy data 255d, ke akumulator

BAB III

PERENCANAAN DAN PEMBUATAN ALAT

Dalam perancangan dan pembuatan alat ini berdasarkan beberapa teori penunjang yang telah dijelaskan pada bab II sebelumnya. Dalam pembahasan perencanaan pada perancangan perangkat keras penganalisa *volume* bahan bakar terhadap jarak yang dapat tempuh dari kondisi bahan bakar tersisa. Pembahasan ini dilakukan per-blok dari diagram sistem secara keseluruhan. Rangkaian yang akan dibahas meliputi, sensor *volume* bahan bakar, sensor jarak, sensor flow, *driver buzzer*, rangkaian ADC, rangkaian *display*, dan rangkaian kontrol.

Dimana rangkaian difungsikan sebagai pengolah data input dan outpul dengan menggunakan mikrokontroler AT89S8252. Disamping itu juga dibahas mengenai perancangan perangkat lunak *(software)* dan mekanik *(prototype)*. Blok diagram secara keseluruhan seperti ditunj ukkan pada gambar 3.1.



Gambar 3. 1. Blok Diagram Sistem Penganalisa Bahan Bakar Terhadap Jarak- Tempuh

Sumber: Perencanaan

3.1 Perencanaan Perangkat Keras *(Hardware)*

3.1.1 Sensor *Volume* Bahan Bakar

Pada bab I telah dijelaskan bahwa umuk mengetahui besarnya kapasitas bahan bakar didalant tangki, diperlukan sensor *volume.* Dalarn perencanaan alat ini digunakan sensor yang terdapat pada kendaraan umumnya. Schingga sensor tidak perlu mengalami perubahan atau modifikasi, dengan demikian sangat memungkinkan alat ini untuk dipasang pada semua jenis kendaraan bermotor. Untuk pemasangan pada jenis kendaraan sepeda motor perlu adanya penyesuaian dengan kapasitas tangki dan diameter roda kendaraan.

Sensor pada kendaran ini model resistansi geser dengan penggerak pelampung. Dimana nilai resistansi berbanding terbalik dengan *volume* bahan bakar. Jika *volume* naik maksimal = 50 liter, maka nilai resistansi sensor (Rs) akan turun sampai mendekati 0Ω, demikian sebaliknya dergan nilai *volume* minimal (kosong), maka resistansi pada kondisi ini maksimal sebesar Rs = 5000. Melihat nilai resistansi maksimal yang sangat keeil dapat dipastikan mengalir arus yang besar dengan sumber tegangan Vcc = +5 Volt.

Agar arus yang mengalir tidak terialu besar dan menyebabkan lilitan sensor panas, maka diperlukan resistansi tambahan yang dirangkai seri dengan sensor. Namun demikian dengan penambahan resitansi ini akan menyebabkan penurtman nilai tegangan output sensor, sehingga untuk menguatkan nilai tegangan output yang sesuaii dengan harga maksimal pada input ADC diperlukan penguat yang akan dibahas pada pembahasan penguat tegangan.

Resistansi (R_1) yang dipasang seri dengan sensor, seperti ditunjukan pada gambar 3.2. Untuk besar arus; yang mengalir ditetapkan sebesar = I mA saat Rs 500 Ω, maka dapat ditentukan resistansi pembatas arus dengan persarnaan 3-1:

$$R_{TOTAL} = \frac{V}{I} \qquad (3\text{-}1)$$

$$R_{TOTAL} = \frac{5V}{1mA}$$

$$= 5k\Omega$$

Maka besar nilai R_1, adalah:

$$R_{TOTAL} = R_1 + R_S \qquad (3\text{-}2)$$

$$R_1 = R_{TOTAL} - R_S \qquad (3\text{-}3)$$

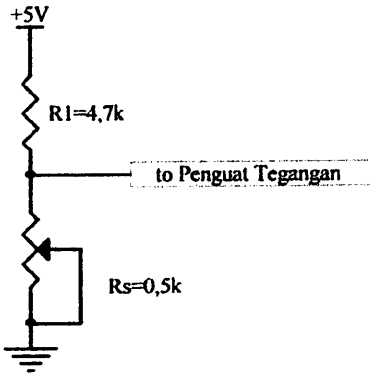
$$= 5k\Omega + 0{,}5k\Omega = 4{,}5k\Omega$$

Dalam perancangan ini agar mendapatkan nilai yang sesuai, maka akan digunakan resistor yaitu 4,7kD. Sedangkan untuk besar tegangan output maksimal atau tegangan pada sensor (Vs) saat bahan bakar kosong adalah

$$V_S = \frac{R_S}{R_1 + R_S} xVcc \qquad (3\text{-}4)$$

$$= \frac{0{,}5k\Omega}{4{,}7k\Omega + 0{,}5k\Omega} x5V = 0{,}48\,Volt$$

Rangkaian sensor *volume* bahan bakar seperti ditunjukkan pada gambar *3.2:*



Garnbar 3.2. Sensor *Volume* Bahan Bakar Model Resistansi Geser
Sumber: Perencanaan

3.1.2 Sensor Jarak Tempuh

Sensor jarak digunakan untuk mendeteksi jarak (km) yang telah ditempuh oleh suatu kendaraan saat berjalan. Untuk pendeteksian ini diambil dari PUtaran *speedo* meter yang ada pada, kendaraan dengan menambahkan piringan bercelah pada mekanik speedo meter. Dimana dari piringan bercelah ini dipasangkan dengan sebuah komponen jenis *optocoupler* cetah, hal ini untuk mendeteksi perputaran piringan melalui lubang atau celah tersebut.

Optocoupler disusun dari dua buah komponen yang berbeda, yaitu LED *(Light Enuniting Diode)* sebagai pembangkit sinar *Infta Red* (IR) dan *photo transistor* sebagai penerima *(receiver)* cahaya IR. Pada rangkaian ini, titik *colector* berada pada kondisi *open* kolektor, sehingga diperlukan resistor pull-up gUna membentuk data *logic T* saat *photo transistor cutoff* (tidak mendapat cahaya IR) atau pada kondisi celah terhalang oleh kepingan bundar. Sedangkan data logic '0' didapat saat celah *opto* mendapat cahaya dari LED-IR pada kondisi celah opto tidak terhalang oleh kepingan bundar tersebut.

Mikrokontroler akan mendeteksi roda kendaraan berputar satu kali, bila *optocoupler* niendeteksi setengan getap dan setengan terang atau mikrokontroler

mendapat *logic '1 & 0'* dengan perioda yang sama. Perhitungan jarak tempuh dipengarubi oleh diameter lingkaran roda depan pada kendaraan. Sedangkan untuk perhitungan jarak pada rancangan ini digunakan diameter 17". Nilaii ini sebagai komponen perhitungan didalam perencanaan perangkat hinak.

Pada *optocoupler* tertutupnya celah, berarti cahaya yang dibangkitkan dari LED IR tidak mengenahi *photo transistor.* Proses ini yang mengakibatkan arus colector tersumbat *(cutoff)* dan output pada colector akan berlogika finggi. Sebaliknya jika cahaya jatuh mengenai photo transistor, maka arus collector akan mengalir (caturation) dan transistor dikatakan dalam keadaan jenuh.

Dalam perencanaan ini besar arus colector saturation ditentukan *IC-sat* 2mA pada Vcc = +5V. Untuk LED-IR dibutuhkan arus 10 mA agar dapat menyala dalam keadaan nonnal, dengan tegangan 2,2Volt pada sumber tegangan Vcc = +5V. Dengan menggunkan persarnaan (3-1), dapat ditentukan resistansi LED (RLED), maka dengan persamaan (3-4) dapat dicari resistansi pembagi tegangan (R2), sedangkan untuk resistorpull-up pada colector (Rc) dengan persamaan 3-5:

$$R_{LED} = \frac{V}{I}$$

$$R_{LED} = \frac{2{,}2V}{10.10^{-3}A} = 220\Omega$$

$$V_{LED} = \frac{R_{LED}}{R_{LED} + R_2} xVcc$$

$$2{,}2\ V = \frac{220\Omega}{220\Omega + R_2} x5\ V$$

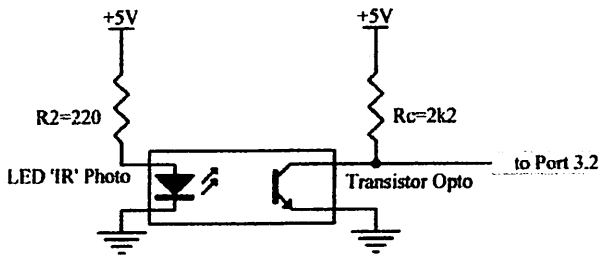
$$R_2 = 280\ \Omega$$

Nilai R_2 dicari yang mendekati ada dipasaran, yaitu 220Ω. Sedangkan untuk mencari besar nilai R_C adalah:

$$R_C = \frac{V_{CC} - V_{CE}}{I_C} \qquad (3\text{-}5)$$

$$R_C = \frac{5V - 0{,}3V}{2x10^{-3}A} 2350\Omega$$

Untuk R_C digunakan resistansi sebesar 2k2 Bentuk rangkaian dari sensor jarak dapat dilihat pada gambar 3.3:



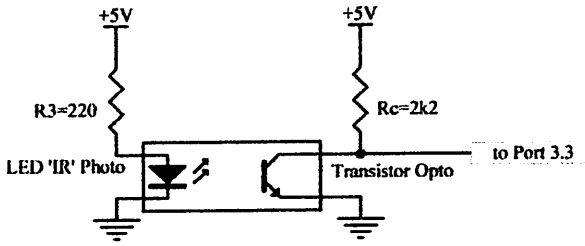
Gambar 3.3. Rangkaian Sensor Jarak Tempuh Menggunakan Optocoupler
Sumber : Perencanaan

3.1.3 Sensor Flow

Seperti halnya sensor jarak, pada sensorflow akan menggunakan prinsip yang sama dalam pembacaannya, yakni pendeteksian menggunakan piringan bercelah. Sensor flow digunakan untuk mendeteksi volume aliran bahan bakar perdetik (debit mm 3 /detik) yang diserap oleh karburator. Dimana volume aliran bahan bakar, berbanding lurus dengan jarak yang dapat ditempuh oleh suatu kendaraan bermotor. Pada perencanaan sensor ini unemiliki data yaitu, setiap satu putaran piringan atau optokoupler mencleteksi kondisi satu gelap clan satu terang. Dimana setiap satu putaran piringan sebanding dengan Imm 3 /detik aliran bahan bakar. Dalampencleteksiannya mikrokontroler dapat mengetahui volume aliran

dengan data frekuensi putaran piringan yang dikirimkan oleh optokoupler dalam bernuk pulsa. Diamana data dari sensorflow akan digunakan sebagai data pernbanding oleh mikrokontroler tehadap jarak dari bahan bakar yang tersisa. Untuk tiap kali konversi bahan bakar terhadap jarak, dibutuhkan referensi jarak, yaitu jarak yang sudah ditempuh ditetapkan sejauh 500m.

Rangkaian sensorflow kompetibel dengan rangkaian sensor jarak, seperti yang ditunjukkan dalam gambar 3.4 berikut ini:



Gambar 3.4. Rangkaian Elektrik Sensor Aliran Bahan Bakar (Flow)
Sumber: Perencanaan

3.1.4 Rangkaian Penguat Tegangan dengan IC LM324

Output tegangan yang dihasilkan dari rangkaian sensor volume bahan bakar, terlalu kecil untuk clapat dibaca sebagai data yang memiliki keakuratan finggi oleh ADC. Maka diperlukan rangkaian penguat guna mendapatkan nilai tegangan output maksimal sebesar 5 *Volt* saat kondisi bahan bakar habis. Hal ini mungkin akan terbaca terbalik saat data ditampilkan pada layar (fispplqv, agar fidak terjadi kesalahan dalarn pembacaannya, maka tegangan dari sensor akan diterapkan pada masukkan *Non Inverting* dari Op-Amp LM 324. Untuk mencari nilai penguatan (A) dan resistansi penguatan (R_f), maka terlebih dabulu menentukan nilai resistansi *input* (R_i) yaitu sebesar 10kΩ Pada perencanaan ini

tegangan *output* maksimal yang di ingginkan V_0 = +5Volt, maka dapat dicari besar (A dan R_f) dengan persamaan 3-6:

$$A = \frac{V_{out}}{V_{in}} \qquad (3\text{-}6)$$

$$A = \frac{5V}{0{,}48mV} = 10{,}41 \; kali$$

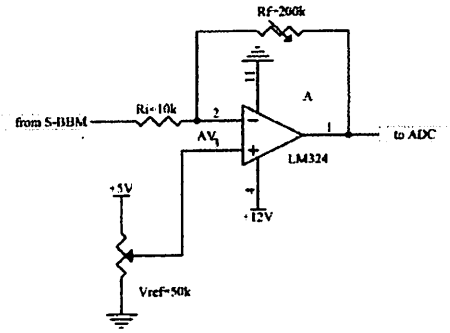
Dalam hal ini penguatan akan disesuaikan sebesar 10,4 kali, untuk mencari nilai Rf adalah:

$$A = \frac{R_f}{R_i} \qquad (3\text{-}7)$$

$$10{,}4 = \frac{R_f}{10k\Omega}$$

$$R_f = 104 \; k\Omega$$

Untuk mendapatkan nilai R_f yang sesuai, maka dalam perancangan ini digunakan resistansi varibel (trimpot) dengan harga maksimal 200ko. Rangkaian penguat tegangan ditunjukkan pada gambar 3.5:



Gambar 3.5. Rangkaian Penguat Tegangan Menggunakan IC LM 324
Sumber: Perencanaan

Penempatan resistor variable 50kΩ sebagai tegangan referensi pada masukan positip. Dimana tegangan referensi diatur sebanding dengan nilai

maksimal tegangan pada masukan negatipnya yaitu $V_{ref} = V_{in} = 0{,}48V$. Sehingga beda potensial antara. Kedua masukan (ΔV), yaitu:

$$\Delta V = V^{+} - V^{-} \qquad (3\text{-}8)$$

$$\Delta V = V_{ref} - V_{in}$$

$$= 0\ Volt$$

Dengan demikan saat bahan bakar kosong, nilai tegangan output sensor pada harga maksimal, yaitu 0,48 Volt, maka tegangan output penguat = 0 Volt dan keluaran hasil konversi ADC adalah $00H_{hex}$. Kondisi sebaliknya jika saat bahan bakar maksimal, tegangan output sensor (V_{in}) = 0 Volt, sehingga tegangan output penguat V_{out} menjadi:

$$\Delta V = 0{,}48V - 0V$$

$$= 0{,}48\ V$$

Maka

a V_{out} adalah:

$$V_{out} = \Delta V \times A \qquad (3\text{-}9)$$

$$= 0{,}48\ V \times 10{,}4$$

$$= 4{,}992\ Volt$$

3.1.5. Rangkaian Pengubah Analog ke Digital (ADC 0804)

Pada perencanaan alat konversi analog ke digital ini menggunakan ADC 0804. ADC ini merupakan jenis IC (Integral Cirrcuit) dengan keluaran/resolusi 8 bit dengan waktu pengubah cepat. ADC 0804 ini beroprasi pada daya standart +5Volt yang dapat mengkonversi tegangan analog dengan masukan berkisar

0Volt-5 Volt. Dalam merancang rangkaian *converter analog* ke digital ini, penulis mengutip langsung dari National Data *Sheet Application.* Untuk menentukan niliai resistor (R_t) dan capasitor (C_t) dihubungkan dengan masukan CLK-R dan CLK-IN. Penerapan hubungan pada rangkaian ini untuk menjangkitkan getaran gelornbang sinus, sehingga dapat membentuk gelornbang pulsa stabil pada *schimittriger* internal-nya.

Untuk melakukan proses konversi pertama-tama $\overline{CS}$ diberi input low kemudian pin $\overline{WR}$ dikondisikan low dan $\overline{RD}$ dipertahankan pada pulsa *high,* sehingga konversi analog ke digital akan terbentuk. Untuk tnernbaca data hasil konversi dengan cara meberi pulsa low pada pin $\overline{CS}$ dan $\overline{RD}$ dengan mempertahankan WR pada kondisi *high,* sehingga data 8 bit akan muncul pada saluran luar (D0-D7).

Apabila data analog yang terbaca adalah 4,992 Volt untuk kondisi bahan bakar maksimal, maka dengan ADC yang memiliki resolusi 8 bit dan bobot maksimal keluaran $11111111_b = 256_d$ untuk input analog maksimal 5 Volt, dengan demikian tiap kenaikan bit-nya adalah 5/256 = 19,5 Volt. Sehingga jika tegangan input 4,992V/1 9,5mV $= \pm 256_d$.

3.2.5.1 *Clock Pada ADC 0804*

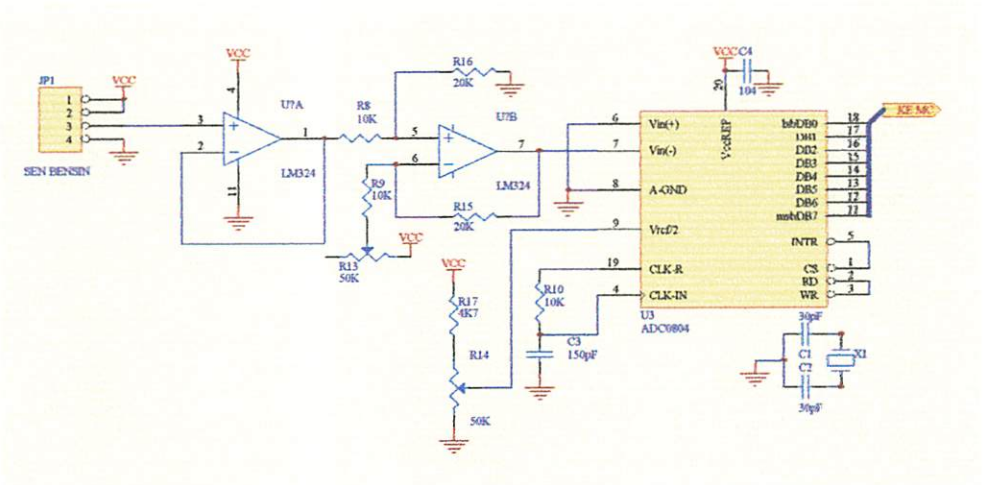
Clock dari ADC memiliki pembentuk pulsa internal, sehingga hanya dibutuhkan sebuah resistor dan capasitor yang dihubungkan pada jalur CLK-R (Pin 19) dan CLK-IN (pin 4). Dengan menetapkan nilai R_t= 10K dan C_t = 150pF maka diperoleh.frekuensi clock sebesar:

$$F_{CLK} = \frac{1}{1{,}1R_tC_t} \qquad (3\text{-}10)$$

$$F_{CLK} = \frac{1}{1{,}1x10x10^{3}x150x10^{-12}}$$

$$F_{CLK} = 606{,}06\ Khz$$

Frekuensi ini masih berada dalam batas yang ditentukan oleh data *sheet* ADC 0804 yaitu 100Khz sampai 1 MHz. Rangkaian ADC dan *clock* dapat dilihat pada gambar *3.6:*



Gambar *3.6.* Rangkaian ADC 0804 Beserta Pembangkit *Clock*
Sumber: Perencanaan

3.1.6 Rangkaian *Driver Buzzer*

Perancangan rangkaian *driver* ini untuk mengaktifkan sebuah *buzzer,* dimanajika *buzzer* berbunyi menandakan bahwa kondisi bahan bakar mendekati habis.Untuk pengontrolan bunyi *buzzer,* mikrokontroler masih membutuhkan sebuahrangkaian *driver.* Dimana rangkaian ini untuk menguatkan arus dan tegangan keluaran mikrokontrole agar sesuai dengan kebutuhan *buzzer* saat berbunyi, yain. 12V/20mA. Rangkaian *driver* disusun dari sebuah transistor silikon tipe FCS9013 dengan tegangan harnbat V_{BE}= 0,6V dan h_{FE} = 120kali.

Agar transistor tidak terlalu jenuh saat terpicu oleh mikrokontroler, maka diperlukan sebuah resistansi pembatas arus pada basisnya (R_b). Untuk menentukan besar resistor basis, terlebih dahulu harus diketahui arus beban IL dalam hal ini *buzzer*, yaitu sebesar 20mA dengan tegangan sumber +12V. Dimana arus beban sebanding dengan arus kolektor yaitu $I_L=I_c$, maka dengan menggunakan persamaan 3-11 dapat dicari besar resistansi Rb adalah:

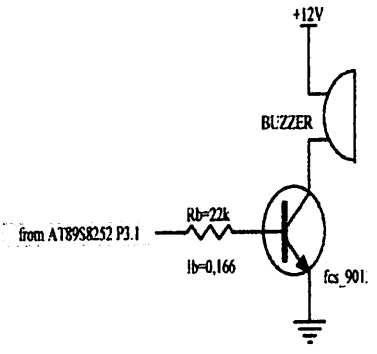
$$I_b = \frac{I_C}{h_{FE}} \qquad (3\text{-}11)$$

$$= \frac{20mA}{120} = 0{,}166mA$$

$$R_b = \frac{V_{BB} - V_{BE}}{I_B} \qquad (3\text{-}12)$$

$$= \frac{5V - 0{,}6}{0{,}166mA} = 26{,}4k\Omega$$

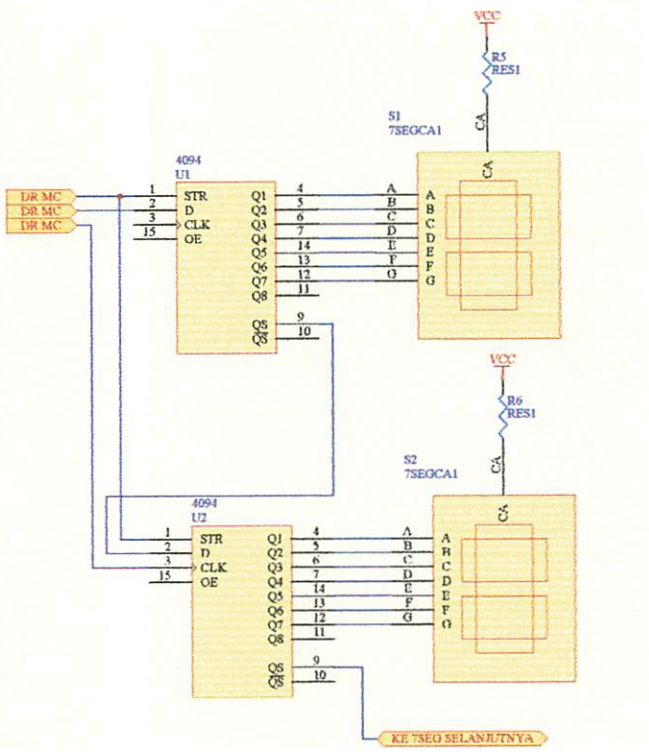
Nilai resistansi disesuaikan dengan yang ada dipasaran, yakni sebesar 22kΩ. Sedangkan rangkian *driver buzzer* ditunjukkan pada gambar 3.7.



Gambar 3.7. Rangkaian *Driver Buzzer*
Sumber : Perenemaan

3.1.7 Rangkaian *Driver Dispplay Seven Segment*

Rangkaian *driver dispplay seven segment* dirancang untuk membangkitkan arus keluaran lebih besar yang sesuai kebutuhan saat semua LED menyala yaitu *20mAx7segment--l40mA.* Pada perancangan disini menggunakan IC CD4094 BMS sebagai driver untuk mengatur nyala LED pada seven segment, IC CD4094BMS mengeluarkan data 7 bit tapi dengan cara bergeser.

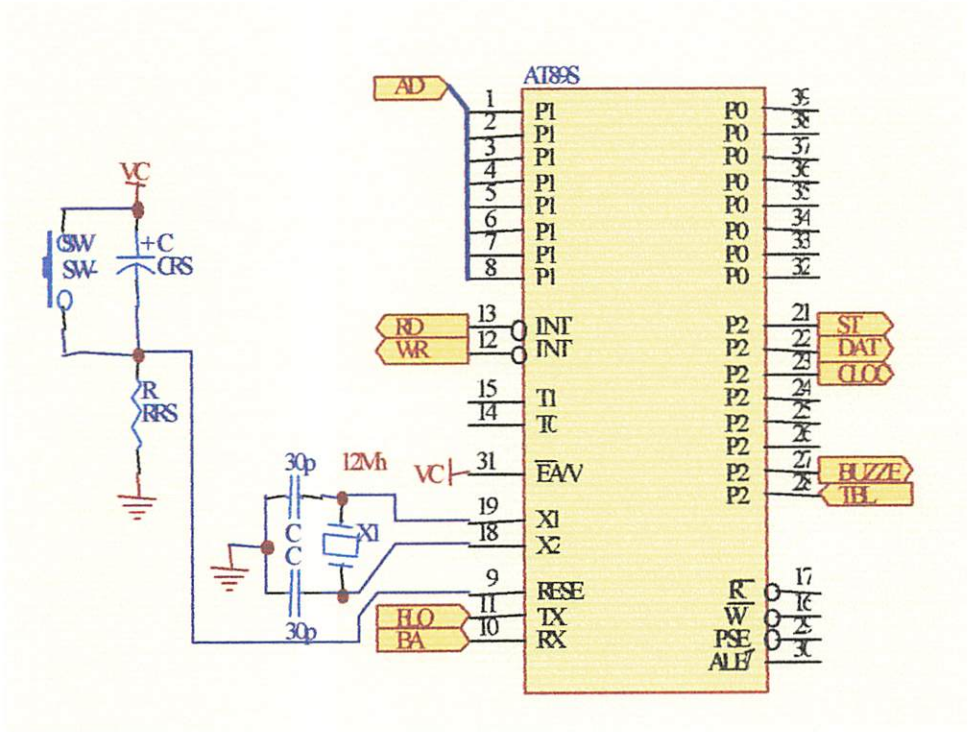


Gambar 3.8. Rangkaian *Dispplay Seven Segment*
Sumber : Perencanaan

3.1.8. Rangkaian Mikrokontroler AT89S8252

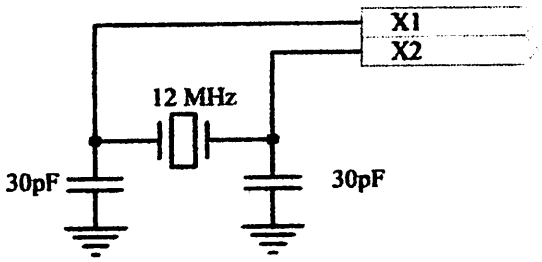
Rangkaian mikrokontroler AT89S8252 berfungsi sebagai pengolah data digital yang dihasilkan dari sensor maupun rangkaian insirumentasi (penguat tegangan) serta rangkaian ADC 0804. Pembacaan input data ADC pada mikrokontroler melalui port 0.0-0.7. Sedangkan hasil dari pengolahan data tersebut ditampilkan pada seven segment melalui port 1.0-1.7. Sedangkan untuk

pendeteksian Optocoupler dihubungkan dengan port 3.2 dan sendor flow pada port 3.3. Untuk hidup-mati buzzer dikontrol melalui port 3. 1. Port 2.0-2.7 dan port 3.0.. Rangkaianhubungan antara mikrokontroler dengan rangkaian pendukungnya ditunjukkan pada gambar 3.9:



Gambar 3.9. Minimum Sistem Mikrokontroler AT89S8252 dan Jalur *interface* dengan Rangkaian Instrument
Sumber : Perencanaan

Pada perancangan alat ini menggunakan clock sebesar 12Mhz. Mikrokontroler ini memiliki *internal clock generator* yang berfungsi sebagai sumber clock, tetapi masih diperlukan rangkaian tambahan umuk membangkitkan *clock* yang dibutuhkan oleh mikrokontroler. Rangkaian ini terdiri dari dua buah *capasitor (C I & C2* = 30Pf) dan sebuah *crystal (XTL – 12* Mhz). gambar 3. 10 dibawah ini adalah bentuk rangkaian sumber *clock* umuk mikrkontroler:



Gambar 3.10. Rangkaian *Clock Exsternal* Mikrokontroler
Sumber: *Data sheet A TMEL*

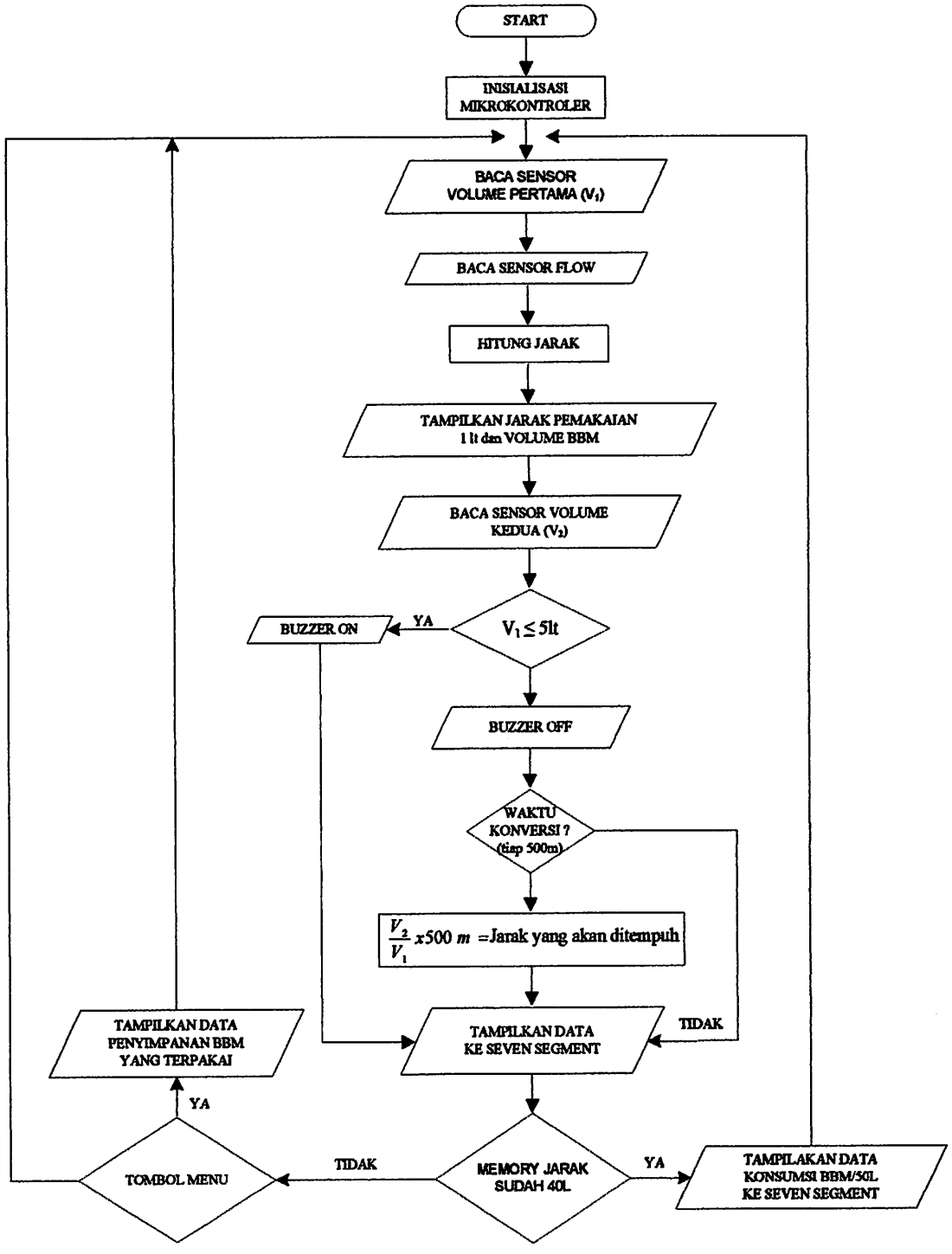
3.2 Perencanaan Perangkat Lunak *(Software)*

3.2.1 Mendesain flowchart

Pembuatan perangkat lunak pada tugas akhir ini adalah untuk mempermudah, dalam menentukan alur program yang akan dibuat pada mikrokontroler AT89S8252. Dalam sub bab ini akan dijelaskan mengenai alur pada program melalui bemuk gambar *(flowchart).*

Pada pernrograman mikrokontroler AT89S8252 ini digunakan bahasa assembler yaitu bahasa pemrograman tingkat sedang, masing-masing mikrokontroler mempunyai bahasa pernrograman sendiri-sendiri yang telah disesuaikan oleh produsen (pabrik). Salah satu program yang mudah diperoleh adalah ALDS *(Assembly Laguage Development System).*

3.2.2. *Flowchart*



Gambar 32.11. Flowchart Program Penganalisaan Bahan Bakar Terhadap jarak Tempuh
Sumber : Perencanaan

3.2.3 Analisis Flowchart

Penganalisaan *flowchart* ini akan memberikan pengertian mengenai pembacaan flowchart, hal ini akan lebih memudahkan terutama untuk masalah pembacaan dalam penerapan rumus-rumus yang digunakan didalainnya. Penerapan sistem penganalisa bahan bakar terhadap jarak khusus untuk kendaraan roda empat, penganlisaan ditumpukan pada pembacaan jarak yang sudah ditempuh, oleh karena yang digunakan mobil makan jarak yang sudah diternputh ini ditentakan oleh diameter roda *(veleg)* yang digunakan sebesar 17 *inch.* Maka dapat dihitung keliling lingkaran atau jarak minimal yang dapat ditempuh untuk satu kali putar adalah :

di mana keseluruhan adalah :

17 *inch* = 431,8 mm

D_{Total} = D_{Veleg} (cm) + Tebal $_{ban}$ (cm)

= 43,18 cm + 8 cm

= 51,18 cm

maka kehling roda ban:

Keliling = 2π. r

= 2 x 3,14 x 1/2 51.18

= 160,705 cm

Jadi jarak minimal yang dapat ditempuh adalab 1,60705 meter, hal ini dapat diketahui dari sensor dalam satu kali putaran. Maka jarak konversi maksimal 500meter dapat diwakili oleh jumlah putaran sebanyak (500/1,60705 = 311 kali putar roda).

Contoh : Aplikasi perhitungan

Pada saat inilah konversi jarak dilakukan dimana volume saat sebelum berangkat tercatat misal (V_1) 40L = 40000cc, maka setelah 311 putar atau ±500meter, terbaca oleh sensor V_2 39975cc, maka konsumsi bahan bakar yang digunakan (V_0) yang terbaca melalui sensor flow untuk menempuh jarak ±500meter atau 311 putaran roda adalah (250 ml = 25 cc).

Jadi jarak yang dapat ditempuh oleh kendaraan dengan baban bakar tersisa adalah:

$$Jarak\ kemudian = \frac{V_2}{V_o} x\ 500meter$$

$$= \frac{39975}{25} x\ 500meter$$

$$= 799500\ meter = 799{,}5\ km$$

Setelah melakakan pedalanan dengan mengbabiskan bahan bakar sebanyak 401iter, maka sistem kontrolakan memberitahukan jarak dan bahan bakar yang sudab ditempuh. Namun demikian sistem kontrol dapat diperintalikan memeberitahukan bahan bakar dan jarak yang sudab ditempuh, sebelum tercapai hal tersebut dengan cara menekan tombol menu.

BAB IV

PENGUJIAN DAN ANALISIS ALAT

4.1 Pendahuluan

Pengujian alat dilakukan untuk mengetahui apakah alat yang telah dibuat dapat bekerja seperti yang telah direncanakan pada bab III, tentang perencanaan pembuatan alat. Dalam pengujian ini ada beberapa sub sistem pengujian yaitu:

- Tiga blok rangkaian sensor *(volume,* jarak danflow).
- Rangkaian penguat tegangan.
- Rangkaian konverter *analog to digital* (ADC 0804).
- Rangkaian *driver buzzer.*
- Rangkaian control dan instrumentasi dengan program assembler.

4.2 Pengujian Rangkaian Sensor Volume Bahan Bakar

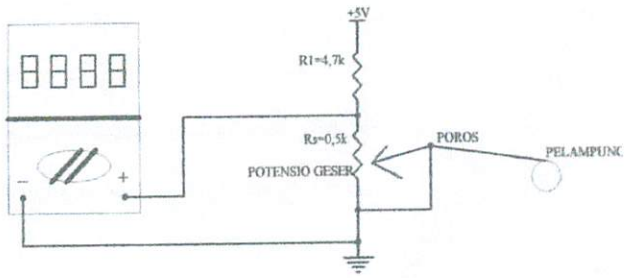
a. Tujuan:

   Untuk mengetahui linieritas dari kenaikkan bahan bakar, terhadap kenaikan tegangan output.

b. Alat dan bahan:

   - Sumber tegangan +5 VDC.
   - Volt meter *analog.*
   - Air dan tabung sebagai simulasi bahan bakar (bensin).
   - Rangkaian pengujian.

c. Gambar cara pengujian rangkaian sensor volume:



Gambar 4.1. Pengujian Rangkaian Sensor *Volume* Bahan Bakar
Sumber : Rangkaian pengujian

d. Data hasil pengujian:

Tabel 4.1.

Data tegangan Output Dari Sensor Volume Bahan Bakar

No	Volume (Liter)	V_{meter} (mV)	Keterangan
1	1	465	Output tegangan terbalik terhadap kenaikan volume bahan bakar, seperti dijelaskan pada bab III sebelumnya
2	5	432	
3	10	387	
4	15	341	
5	40	0	

Sumber : Data hasil pengujiian

e. Analisis:

Hasil dari pengarnatan dapat disimpulkan bahwa, saat *volume* bahan bakar naik-turun, kenaikan volume terhadap tinggi permukaan bahan bakar tidak sebanding. Kondisi ini dikarenakan bentuk tabung bahan bakar, sedangkan sensor memiliki pergerakan yang membernuk lingkaran.

4.3 Pengujian Rangkaian Sensor Jarak

a. Tujuan:

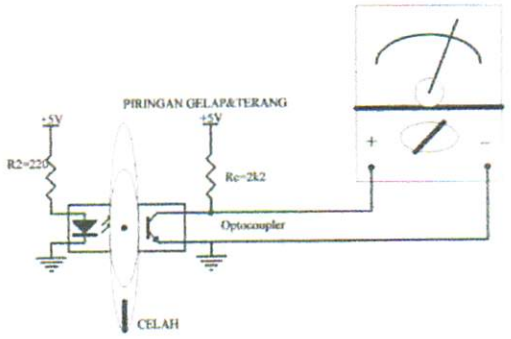
Pada pengujian ini bertujuan, untuk mengetahui bentuk tegangan output dari optokoupler terhadap hasil pernbacaan dari objek (piringan getap/terang).

b. Alat dan bahan :

- Sumber tegangan +5 VDC.

- *Volt* meter *analog.*
- Lingkaran gelap/terang sebagai objek penghalang.

c. Gambar cara pengujian rangkaian sensor jarak :



Gambar 4.2. pengujian Rangkaian Optocopler sebagai sensor jarak
Sumber : Rangkaian pengujian

d. Dari hasil pengujian

Tabel 4.2.

Data tegangan Output dari Sensor Jarak (Optocoupler).

No	Cahaya Infra Red	V_{meter} (Volt)	Logic	Keterangan
1	Terhalang	4,5	'1'	Transistor opto cut off (mati)
2	Tembus	0,1	'0'	Transiator opto saturation (bekerja)

Sumber : Data hasil pengujian

e. Analisis :

Dengan mengamati tingkah laku *optocoupler* maka, dapat disimpulkan bahwa saat cahaya *infra red* terhalang lingkaran gelap, maka *output* tegangan pada *colektor opto* berlogika *high* '1'dan sebaliknya. Jadi untuk mengetahui satu lingkaran noda depan mobil, mikrokontroller harus mendeteksi keadaan satu gelap dan satu terang atau logic (1 & 0) dari *optooupler.*

4.4. Pengujian Rangkaian Sensor Flow

a. Tujuan:

Pengujian sensor flow atau aliran bahan bakar yang menuju karburator bertujuan, untuk mengetahui konsumsi bahan bakar terhadap jarak yang sudah ditetapkan yakni tiap 500m. Dengan demikian dapat diketaui apakah kondisi jalan naik atau turun, hal ini akan digunakan sebagai data referensi mikrokontroler dalam menganalisa sisa bahan bakar terhadap jarak yang dapat ditempuh.

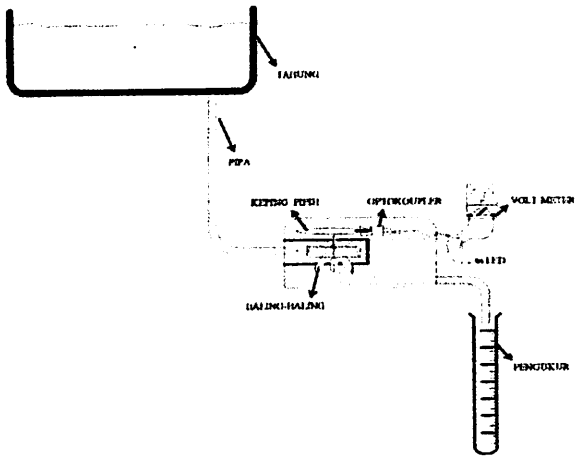
b. Alat dan bahan:

a. Sumber tegangan +5 VDC.

b. Air sebagai objek penganti bahan bakar.

c. Sensorflow.

c. Gambar cara pengujian rangkaian sensor flow:



Gambar 4.3. Pengujian Rangkaian Sensor Flow
Sumber: Rangkaian pengujian

d. Data basil pengujian:

Tabel 4.3

Data Tegangan Output Dari Sensor Flow

No	Jumlah Putaran	Output Volume	Keterangan
1	20	42	Data output rata-rata dipengaruhi oleh kepresisian putaran piringan jumlah aliran
2	40	84	
3	50	105	
4	100	210	

Sumber: Data hasil pengujian

e. Analisis :

Pada sensor flow ini hanya membaca putaran dari piringan bercelah untuk mengetahui debit suatu aliran. Melihat tabel bahwasanya setiap dua puluh putaran menghasilkan volume 44cc. Hal ini secara maternatis dapat dinyatakan bahwa setiap kali putaran kepingan menandakan volume bertambah sebesar 2,1cc.

4.5 Pengujian Rangkaian Penguat

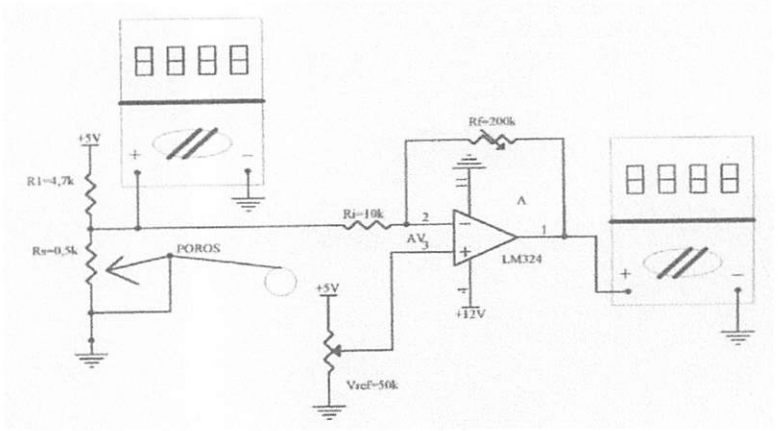
a. Tujuan:

Mengamati dan membandingkan data tegangan output hasil penguatan dari *Op-Amp* terhadap perhitungan.

b. Alat dan bahan:

- Sumber tegangan + 5V
- 2 buah Volt meter analog.
- Input tegangan (tegangan variable).

c. Gambar cara pengujian rangkaian penguat tegangan:



Gambar 4.4. Pengujian Rangkaian Penguat Tegangan
Sumber: Rangkaian pengujian

d. Dari hasil pengujian :

Tabel 4.4.

Data Hasil Pengamatan Pada Rangkaian Penguat Tegangan

No	$V_{meter-1}$ (m Volt)	Penguatan (A) kali	$V_{meter-2}$ (mVolt)	Perhitungan (m Volt)	Error
1	0	10,4	0	0	1,9%
2	50	10,4	541	520	
3	75	10,4	795	780	
4	100	10,4	1055	1040	
5	350	10,4	3664	3640	

Sumber : Data hasil pengujian

e. Analisis:

Data hasil pengujian yaitu, terbaca pada saat diberi *input* minimal *(0Volt)* , maka output *Op-Amp* tidak mampu menghasilkan tegangan OVolt, hal ini dikarenakan IC Op-Amp hanya menggunakan *single* tegangan (+12V dan 0V). Dimana Vce transistor dalam IC tidak mampu jenuh sampai mendekati 0 Volt

4.6. Pengujian Rangkaian ADC 0804

a. Tujuan:

Untuk mengetahui nilai hasil konversi tegangan analog ke digital tiap kenaikan I digit dari hasil konversi nilai tegangan input.

d. Data hasil pengujian:

Tabel 4.6.

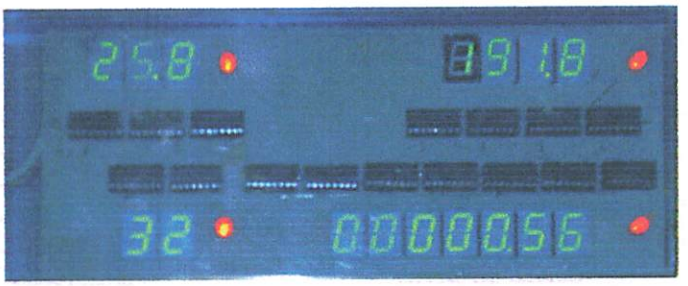
Data Hasil Pengukuran dan Pengamatan Pada Sistem Alat

No	Sensor	Tampilan Digit	Buzzer	Keterangan
1	Flow	35	-	Nilai hasil konversi dipengaruhi oleh kondisi secara fisik dari objek terdeteksi
2	Jarak	500 M	-	
3	Bahan Bakar	4,98 Liter	-	
4	Analisa	-	ON	
5	Flow	32	-	
6	Jarak	500 M	-	
7	Bahan Bakar	25,8 Liter	OFF	
8	Analisa	191,8 Km	-	

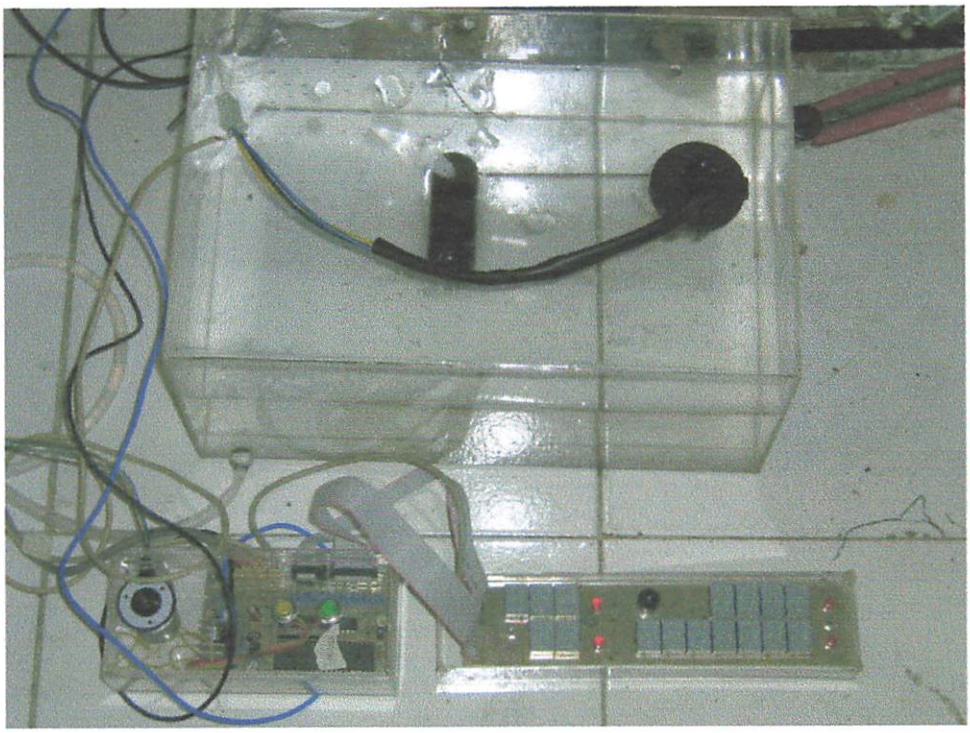
Sumber: Data pengujian

e. Analisis:

Dapat dianalisis pada blok keseluruhan dari sistem ini bahwa, alat dapat bekerja langsung pada alat peraga *volume* bahan bakar (bensin) dengan dinamo (motor DC 12V) sebagai simulasi roda berputar. Sedangkan tampilan pada *seven segment* sebagai penunjuk jarak yang telah ditempuh dan *volume* bahan bakar tersisa sekaligus kemungkinan jarak yang dapat ditempuh. Dari pengujian tersebut menunjukan nilai dari hasil pembacaan masing-masing sensor terhadap objek terbaca dengan kondisi yang tepat.



Gambar 4.8. Gambar Hasil Pengujian Alat



Gambar 4.9. Gambar Keseluruhan Alat

BAB V

KESIMPULAN DAN SARAN

5.1. Kesimpulan.

Berdasarkan perencanaan dan pengujian yang telah dilakukan, maka didapat kesimpulan sebagai berikut:

- Untuk sensor jarak, diameter roda (veleg) yang digunakan sebesar 17 inch dan ditambah oleh tebal ban luar 8 cm, maka setiap sekali putaran dapat menempuh jarak 1,60705 meter. Roda depan kendaraan adalah faktor penting dalam dalam menentukan perhitungan jarak.
- Untuk sensor aliran (flow) dalam sekali putaran menghasilkan keluaran sebesar 2,1 cc. flow jg merupakan sensor yang sangat penting untuk menentukan banyaknya bahan bakar yang dipakai.
- Dari hasil pengukuran dan perhitungan didapat nilai error sebesar 0,7%.
- Pembacaan volume bahan bakar juga dipengaruhi oleh kondisi luar yaitu pada saat jalan naik dan turun. Namun demikian pada alat ini sudah dilengkapi dengan sensor flow yang akan mengetahui aliran bahan bakar terhadap konsumsi kendaraan.

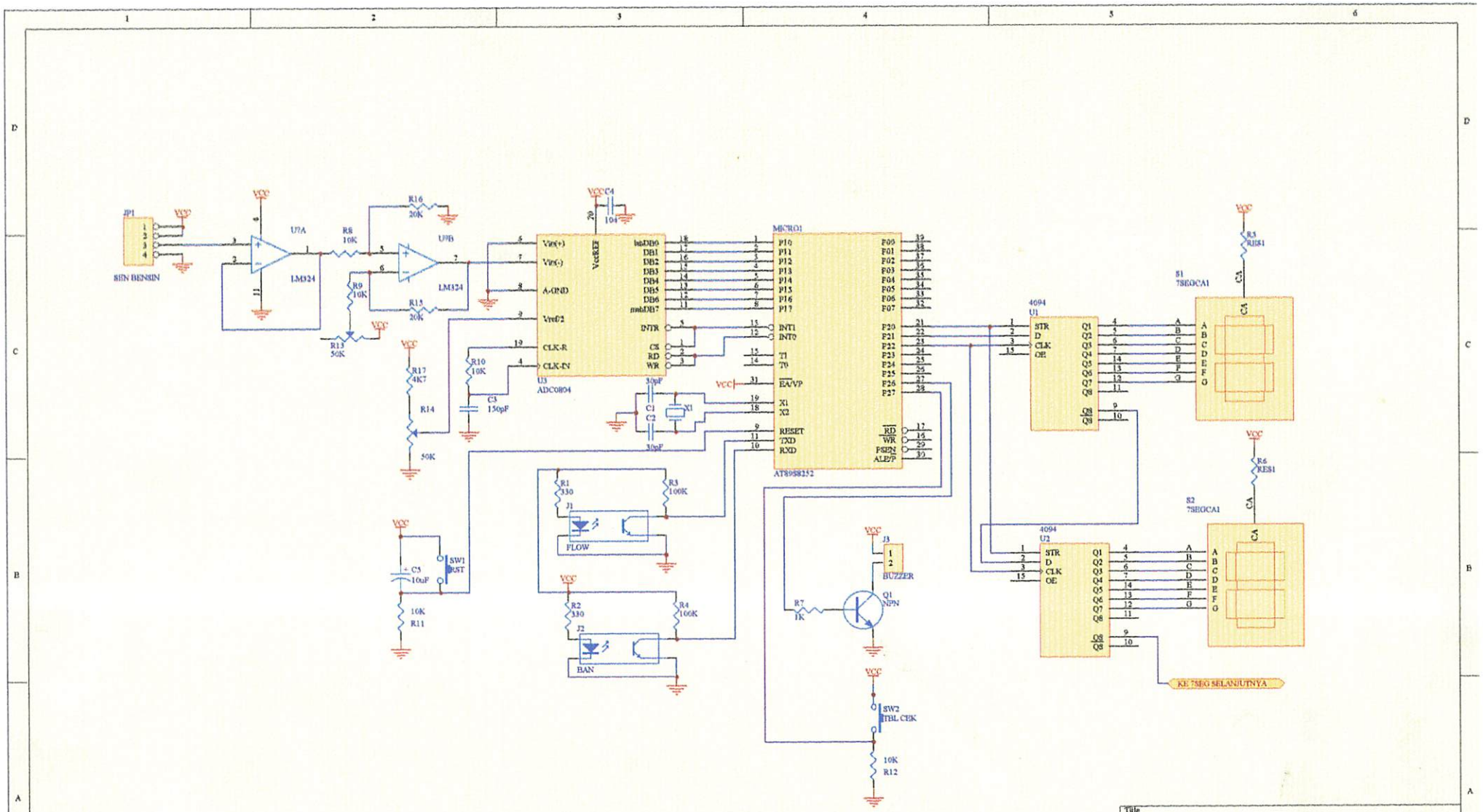
5.2. Saran-Saran

- Sensor optocoupler dalam penerapan yang sesungguhnya dapat dipengaruhi oleh air (hujan), debu maupun kotoran yang menempel/masuk pada celah-celah optocoupler, sehingga dapat mempengaruhi dalam pembacaan putaran.
- Untuk lebih lengkapnya sebaiknya juga menampilkan rotasi per-menit (Rpm).

- Sistem sebaiknya dilengkapi dengan pencatat kebutuhan bahan bakar dalam satu bulan terakhir.
- Untuk penempatan sensor jarak perlu diperhatikan, agar sensor terhindar dari kotoran.
- Khusus untuk penerapan kendaraan yangberkapasitas besar (truk), sebaiknya *software* disesuaikan dengan pembacaan sensor.

Daftar Pustaka

- Data sheet mikrokontroler AT89S8252
- Data sheet ADC 0804
- Data sheet optocoupler
- Data sheet LM 324, nasional semikonduktor
- MALIK, Mch. Ibnu, dan Anistradi, Belajar Mokrokontroler ATMEL AT89S8252, Gava Media, Yogyakarta, 2003
- ATMEL Data Sheet, 8-Bit Microcontroller White 8 Kbytes Flash, 1994, AT89C52, California, 1999.
- Malvino, Prinsip-Prinsip Elektronika, edisi kedua, ahli bahasa: Hanafi Gunawan, Erlangga, Jakarta, 1994.
- Mitel data sheet, Microelektronik Digital/Analog Comunication Handbook, Mitel semiconductor Corp, Canada, 1993.
- National Semiconductor Data Book, tssimshatsui HK, 1995.



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L E M B A R P E R S E M B A H A N

Puji syukur atas rahmat dan hidayah kepada Allah SWT dan junjungan hamba Muhammad SAW, sehingga terselesaikan penulisan skripsi ini.

Kupersembahkan karya ini walupun jauh dari kesempurnaan (karna kesempurnaan hanya milik Allah SWT) kepada :

Ayah dan Bunda : Terlalu banyak pengorbanan yang engkau berikan baik materi maupun perasaan, tiada hal yang paling anaknda inginkan kecuali membalas segala kabaikan ayahnda dan bunda, semoga niat dan cita-cita anaknda dikabulkan oleh SWT (Amin ya robbal allamin).

Kakak dan Adikku : Mas Andi + Mba Win terima kasih atas dukungan dan dorongannya selama ini, Mbak Nu2 semua yang tlah mbak berikan gak akan penah aku lupakan, Adikku Astri dan Anjar kalian adik2ku yang paling cantik.

My Friend : Anak-anak F 243 (Robby (rombeng), Taufik (Qumal), Apay (kentu) + tink (ayo buruan biar semester depan dah jadi ST), andre (uncle mbote), Andi + Lisa, Santos (saudara sebotol), Babe (Doel), Anton, yuli, Lisa, Mas Dody (ABFL), Adit. (Terima kasih atas segala bantuan kalian).

Special thanks : Wiwin (sayang terima kasih untuk semuanya gak kan pernah aku lupakan), Idha (terima kasih untuk semua yang dah kau berikan), Ka2 amin + ka2 Yuli sekeluarga (terima kasih atas bantuan dan doanya), Mas yuli + Mbak Nik sekeluarga, Mas Imam + Mba Lidya sekeluarga, Bang Erik + Mba Cantik sekeluarga.

Institut Teknologi Nasiaonal Malang
Fakultas Teknologo Industri
Jurusan Teknik Elektronika

Formulir Bimbingan Skripsi

Nama : **Andi Anwar**
Nim : **99.17.032**
Masa Bimbingan : **Tgl 10 Agustus 2006 Sampai 10 Februari 2007**
Judul : **Perencanaan Dan Pembuatan Alat Pencatat Dan Penganalisaan Kebutuhan Bahan Bakar Kendaraan Berbasis Mikrokontroler AT89S8252**

NO	Tanggal	Uraian	Paraf Pembimbing
1	20 - 08 - 2006	BAB I . ACC	
2	24 - 08 - 2006	BAB II . - Sensor - Kristal	
3	01 - 09 - 2006	BAB II . ACC	
4	18 - 09 - 2006	BAB III . - Blok Diagram - flowchart	
5	01 - 10 - 2006	BAB III ACC	
6	12 - 05 - 2007	Demo Alat	
7	10 - 08 - 2007	ACC Makalah Seminar	
8	12 - 08 - 2007	BAB IV. Cantumkan foto alat	
9	14 - 08 - 2007	BAB IV ACC	
10	01 - 09 - 2007	BAB V ACC + kompre	

Malang,

Dosen Pembimbing

(Eko Noercahyo)

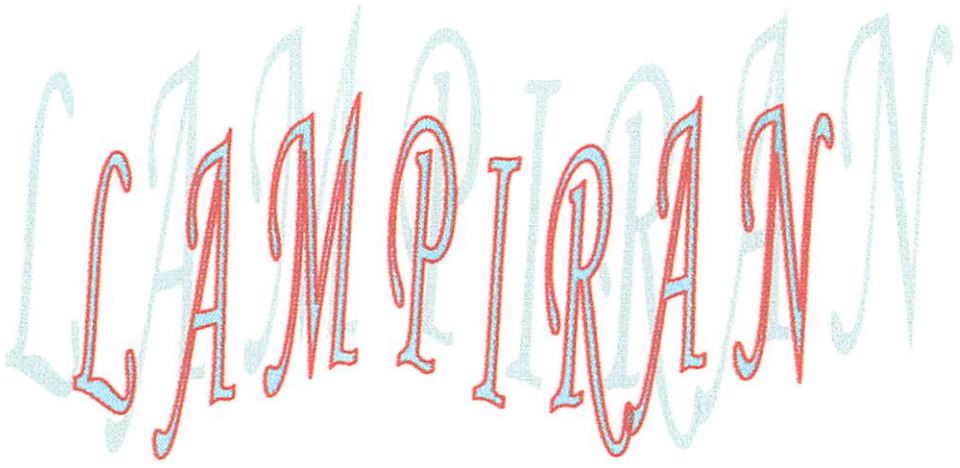
JURUSAN TEKNIK ELEKTRO S-1
FAKULTAS TEKNOLOGI INDUSTRI
INSTITUT TEKNOLOGI NASIONAL MALANG

FORMULIR PERBAIKAN SKRIPSI

ılam pelaksanaan Ujian Skripsi, perlu adanya perbaikan skripsi untuk mahasiswa :

lama	:	Andi Anwar	
IIM	:		
akultas	:	Teknologi Industri	
ırusan	:	Teknik Elektro S-1	
onsentrasi	:	1.	Teknik Energi Listrik *)
		2.	Teknik Elektronika *)
		3.	Tenik Komputer dan Informatika *)

rbaikan meliputi :


LAMPIRAN

'es

- tible with MCS®51 Products
- ɜs of In-System Reprogrammable Downloadable Flash Memory
- l Serial Interface for Program Downloading
- durance: 1,000 Write/Erase Cycles
- ɜs EEPROM
- durance: 100,000 Write/Erase Cycles
- V Operating Range
- tatic Operation: 0 Hz to 24 MHz
- evel Program Memory Lock
- -bit Internal RAM
- ɡrammable I/O Lines
- 16-bit Timer/Counters
- iterrupt Sources
- mmable UART Serial Channel
- rial Interface
- ɔwer Idle and Power-down Modes
- pt Recovery from Power-down
- mmable Watchdog Timer
- ata Pointer
- -off Flag

'iption

9S8252 is a low-power, high-performance CMOS 8-bit microcontroller with 8K downloadable Flash programmable and erasable read-only memory and 2K EEPROM. The device is manufactured using Atmel's high-density nonvolatile technology and is compatible with the industry-standard 80C51 instruction pinout. The on-chip downloadable Flash allows the program memory to be mmed In-System through an SPI serial interface or by a conventional nonvol-mory programmer. By combining a versatile 8-bit CPU with downloadable a monolithic chip, the Atmel AT89S8252 is a powerful microcontroller, which s a highly-flexible and cost-effective solution to many embedded control ons.

9S8252 provides the following standard features: 8K bytes of downloadable K bytes of EEPROM, 256 bytes of RAM, 32 I/O lines, programmable watchdog /o data pointers, three 16-bit timer/counters, a six-vector two-level interrupt ture, a full duplex serial port, on-chip oscillator, and clock circuitry. In addition, 9S8252 is designed with static logic for operation down to zero frequency and s two software selectable power saving modes. The Idle Mode stops the CPU owing the RAM, timer/counters, serial port, and interrupt system to continue ing. The Power-down mode saves the RAM contents but freezes the oscillator, g all other chip functions until the next external interrupt or hardware reset.

vnloadable Flash can be changed a single byte at a time and is accessible the SPI serial interface. Holding RESET active forces the SPI bus into a serial ming interface and allows the program memory to be written to or read from ɔck bits have been activated.

8-bit Microcontroller with 8K Bytes Flash

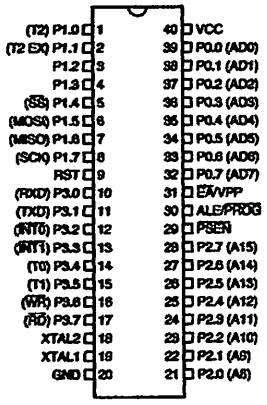
AT89S8252

Not Recommended for New Designs. Use AT89S8253.

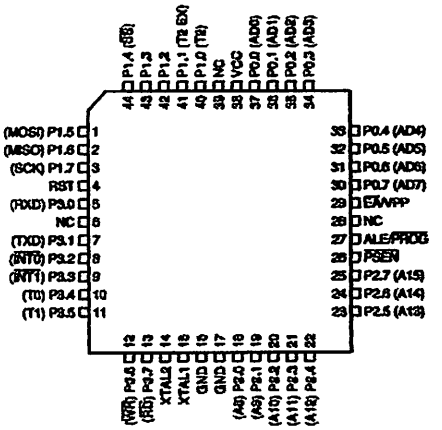
0401G–MICRO–3/06

onfigurations

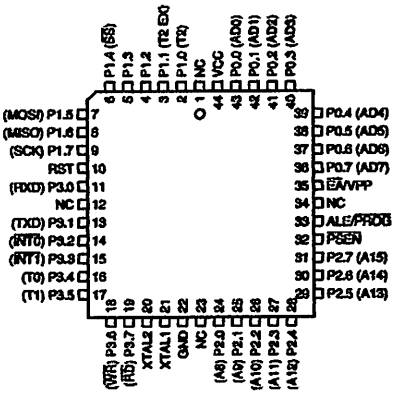
PDIP



TQFP



PLCC



escription

Supply voltage.

Ground.

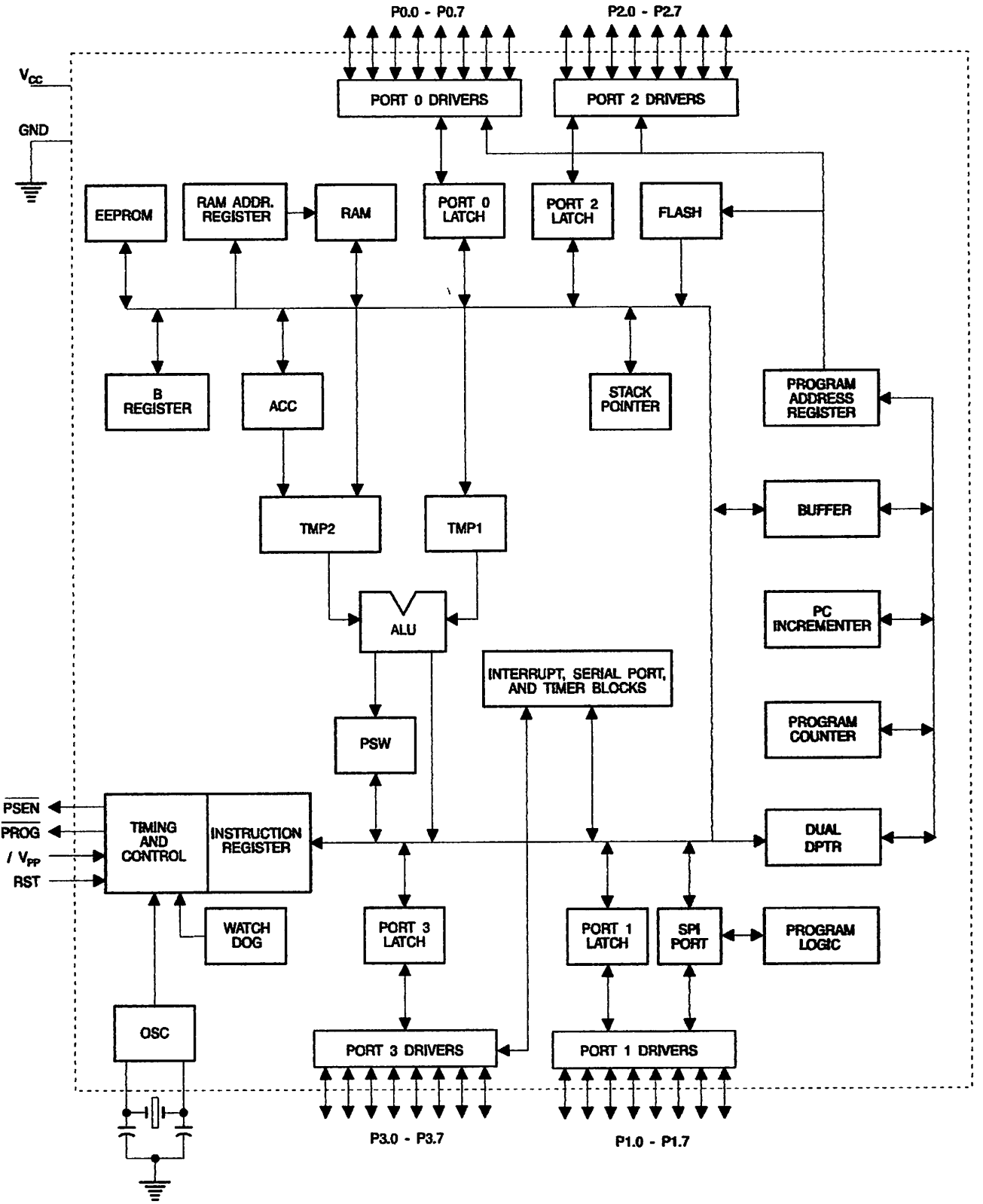
Port 0 is an 8-bit open drain bi-didirectional I/O port. As an output port, each pin can sink eight TTL inputs. When 1s are written to port 0 pins, the pins can be used as high-impedance inputs.

Port 0 can also be configured to be the multiplexed low-order address/data bus during accesses to external program and data memory. In this mode, P0 has internal pull-ups.

Port 0 also receives the code bytes during Flash programming and outputs the code bytes during program verification. External pull-ups are required during program verification.

Port 1 is an 8-bit bi-directional I/O port with internal pull-ups. The Port 1 output buffers can sink/source four TTL inputs. When 1s are written to Port 1 pins, they are pulled high by the internal pull-ups and can be used as inputs. As inputs, Port 1 pins that are externally being pulled low will source current (I_{IL}) because of the internal pull-ups.

Diagram


P0.0 - P0.7
P2.0 - P2.7
V_{CC}
GND
PORT 0 DRIVERS
PORT 2 DRIVERS
EEPROM
RAM ADDR. REGISTER
RAM
PORT 0 LATCH
PORT 2 LATCH
FLASH
B REGISTER
ACC
STACK POINTER
PROGRAM ADDRESS REGISTER
BUFFER
TMP2
TMP1
ALU
PC INCREMENTER
INTERRUPT, SERIAL PORT, AND TIMER BLOCKS
PROGRAM COUNTER
PSW
PSEN
PROG
/ V_{PP}
RST
TIMING AND CONTROL
INSTRUCTION REGISTER
DUAL DPTR
WATCH DOG
PORT 3 LATCH
PORT 1 LATCH
SPI PORT
PROGRAM LOGIC
OSC
PORT 3 DRIVERS
PORT 1 DRIVERS
P3.0 - P3.7
P1.0 - P1.7

Some Port 1 pins provide additional functions. P1.0 and P1.1 can be configured to be the timer/counter 2 external count input (P1.0/T2) and the timer/counter 2 trigger input (P1.1/T2EX), respectively.

Furthermore, P1.4, P1.5, P1.6, and P1.7 can be configured as the SPI slave port select, data input/output and shift clock input/output pins as shown in the following table.

Port Pin	Alternate Functions
P1.0	T2 (external count input to Timer/Counter 2), clock-out
P1.1	T2EX (Timer/Counter 2 capture/reload trigger and direction control)
P1.4	$\overline{SS}$ (Slave port select input)
P1.5	MOSI (Master data output, slave data input pin for SPI channel)
P1.6	MISO (Master data input, slave data output pin for SPI channel)
P1.7	SCK (Master clock output, slave clock input pin for SPI channel)

Port 1 also receives the low-order address bytes during Flash programming and verification.

Port 2 is an 8-bit bi-directional I/O port with internal pull-ups. The Port 2 output buffers can sink/source four TTL inputs. When 1s are written to Port 2 pins, they are pulled high by the internal pull-ups and can be used as inputs. As inputs, Port 2 pins that are externally being pulled low will source current (I_{IL}) because of the internal pull-ups.

Port 2 emits the high-order address byte during fetches from external program memory and during accesses to external data memory that use 16-bit addresses (MOVX @ DPTR). In this application, Port 2 uses strong internal pull-ups when emitting 1s. During accesses to external data memory that use 8-bit addresses (MOVX @ RI), Port 2 emits the contents of the P2 Special Function Register.

Port 2 also receives the high-order address bits and some control signals during Flash programming and verification.

Port 3 is an 8-bit bi-directional I/O port with internal pull-ups. The Port 3 output buffers can sink/source four TTL inputs. When 1s are written to Port 3 pins, they are pulled high by the internal pull-ups and can be used as inputs. As inputs, Port 3 pins that are externally being pulled low will source current (I_{IL}) because of the pull-ups.

Port 3 receives some control signals for Flash programming and verification.

Port 3 also serves the functions of various special features of the AT89S8252, as shown in the following table.

Port Pin	Alternate Functions
P3.0	RXD (serial input port)
P3.1	TXD (serial output port)
P3.2	$\overline{INT0}$ (external interrupt 0)
P3.3	$\overline{INT1}$ (external interrupt 1)
P3.4	T0 (timer 0 external input)
P3.5	T1 (timer 1 external input)
P3.6	$\overline{WR}$ (external data memory write strobe)
P3.7	$\overline{RD}$ (external data memory read strobe)

Reset input. A high on this pin for two machine cycles while the oscillator is running resets the device.

ROG

Address Latch Enable is an output pulse for latching the low byte of the address during accesses to external memory. This pin is also the program pulse input ($\overline{PROG}$) during Flash programming.

In normal operation, ALE is emitted at a constant rate of 1/6 the oscillator frequency and may be used for external timing or clocking purposes. Note, however, that one ALE pulse is skipped during each access to external data memory.

If desired, ALE operation can be disabled by setting bit 0 of SFR location 8EH. With the bit set, ALE is active only during a MOVX or MOVC instruction. Otherwise, the pin is weakly pulled high. Setting the ALE-disable bit has no effect if the microcontroller is in external execution mode.

Program Store Enable is the read strobe to external program memory.

When the AT89S8252 is executing code from external program memory, $\overline{PSEN}$ is activated twice each machine cycle, except that two $\overline{PSEN}$ activations are skipped during each access to external data memory.

P

External Access Enable. $\overline{EA}$ must be strapped to GND in order to enable the device to fetch code from external program memory locations starting at 0000H up to FFFFH. Note, however, that if lock bit 1 is programmed, $\overline{EA}$ will be internally latched on reset.

$\overline{EA}$ should be strapped to V_{CC} for internal program executions. This pin also receives the 12-volt programming enable voltage (V_{PP}) during Flash programming when 12-volt programming is selected.

Input to the inverting oscillator amplifier and input to the internal clock operating circuit.

Output from the inverting oscillator amplifier.

al Function ters

A map of the on-chip memory area called the Special Function Register (SFR) space is shown in Table 1.

Note that not all of the addresses are occupied, and unoccupied addresses may not be implemented on the chip. Read accesses to these addresses will in general return random data, and write accesses will have an indeterminate effect.

User software should not write 1s to these unlisted locations, since they may be used in future products to invoke new features. In that case, the reset or inactive values of the new bits will always be 0.

Timer 2 Registers Control and status bits are contained in registers T2CON (shown in Table 2) and T2MOD (shown in Table 9) for Timer 2. The register pair (RCAP2H, RCAP2L) are the Capture/Reload registers for Timer 2 in 16-bit capture mode or 16-bit auto-reload mode.

AT89S8252 SFR Map and Reset Values

								0FFH
B 00000000								0F7H
								0EFH
ACC 00000000								0E7H
								0DF H
PSW 00000000					SPCR 000001XX			0D7H
T2CON 00000000	T2MOD XXXXXX00	RCAP2L 00000000	RCAP2H 00000000	TL2 00000000	TH2 00000000			0CF H
								0C7H
IP XX000000								0BFH
P3 11111111								0B7H
IE 0X000000		SPSR 00XXXXXX						0AFH
P2 11111111								0A7H
SCON 00000000	SBUF XXXXXXXX							9FH
P1 11111111						WMCON 00000010		97H
TCON 00000000	TMOD 00000000	TL0 00000000	TL1 00000000	TH0 00000000	TH1 00000000			8FH
P0 11111111	SP 00000111	DP0L 00000000	DP0H 00000000	DP1L 00000000	DP1H 00000000	SPDR XXXXXXXX	PCON 0XXX0000	87H

T2CON – Timer/Counter 2 Control Register

Address = 0C8H Reset Value = 0000 0000B

ssable

TF2	EXF2	RCLK	TCLK	EXEN2	TR2	C/$\overline{T2}$	CP/$\overline{RL2}$
7	6	5	4	3	2	1	0

	Function
	Timer 2 overflow flag set by a Timer 2 overflow and must be cleared by software. TF2 will not be set when either RCLK = 1 or TCLK = 1.
	Timer 2 external flag set when either a capture or reload is caused by a negative transition on T2EX and EXEN2 = 1. When Timer 2 interrupt is enabled, EXF2 = 1 will cause the CPU to vector to the Timer 2 interrupt routine. EXF2 must be cleared by software. EXF2 does not cause an interrupt in up/down counter mode (DCEN = 1).
	Receive clock enable. When set, causes the serial port to use Timer 2 overflow pulses for its receive clock in serial port Modes 1 and 3. RCLK = 0 causes Timer 1 overflows to be used for the receive clock.
	Transmit clock enable. When set, causes the serial port to use Timer 2 overflow pulses for its transmit clock in serial port Modes 1 and 3. TCLK = 0 causes Timer 1 overflows to be used for the transmit clock.
	Timer 2 external enable. When set, allows a capture or reload to occur as a result of a negative transition on T2EX if Timer 2 is not being used to clock the serial port. EXEN2 = 0 causes Timer 2 to ignore events at T2EX.
	Start/Stop control for Timer 2. TR2 = 1 starts the timer.
	Timer or counter select for Timer 2. C/$\overline{T2}$ = 0 for timer function. C/$\overline{T2}$ = 1 for external event counter (falling edge triggered).
	Capture/Reload select. CP/$\overline{RL2}$ = 1 causes captures to occur on negative transitions at T2EX if EXEN2 = 1. CP/$\overline{RL2}$ = 0 causes automatic reloads to occur when Timer 2 overflows or negative transitions occur at T2EX when EXEN2 = 1. When either RCLK or TCLK = 1, this bit is ignored and the timer is forced to auto-reload on Timer 2 overflow.

g and Memory Control Register The WMCON register contains control bits for the Watchdog Timer (shown in The EEMEN and EEMWE bits are used to select the 2K bytes on-chip EEPROM, and to enable byte-write. The elects one of two DPTR registers available.

WMCON—Watchdog and Memory Control Register

l Address = 96H

Reset Value = 0000 0010B

PS2	PS1	PS0	EEMWE	EEMEN	DPS	WDTRST	WDTEN
7	6	5	4	3	2	1	0

	Function
	Prescaler Bits for the Watchdog Timer. When all three bits are set to "0", the watchdog timer has a nominal period of 16 ms. When all three bits are set to "1", the nominal period is 2048 ms.
	EEPROM Data Memory Write Enable Bit. Set this bit to "1" before initiating byte write to on-chip EEPROM with the MOVX instruction. User software should set this bit to "0" after EEPROM write is completed.
	Internal EEPROM Access Enable. When EEMEN = 1, the MOVX instruction with DPTR will access on-chip EEPROM instead of external data memory. When EEMEN = 0, MOVX with DPTR accesses external data memory.
	Data Pointer Register Select. DPS = 0 selects the first bank of Data Pointer Register, DP0, and DPS = 1 selects the second bank, DP1
T $\overline{Y}$	Watchdog Timer Reset and EEPROM Ready/$\overline{\text{Busy}}$ Flag. Each time this bit is set to "1" by user software, a pulse is generated to reset the watchdog timer. The WDTRST bit is then automatically reset to "0" in the next instruction cycle. The WDTRST bit is Write-Only. This bit also serves as the RDY/$\overline{\text{BSY}}$ flag in a Read-Only mode during EEPROM write. RDY/$\overline{\text{BSY}}$ = 1 means that the EEPROM is ready to be programmed. While programming operations are being executed, the RDY/$\overline{\text{BSY}}$ bit equals "0" and is automatically reset to "1" when programming is completed.
	Watchdog Timer Enable Bit. WDTEN = 1 enables the watchdog timer and WDTEN = 0 disables the watchdog timer.

SPI Registers Control and status bits for the Serial Peripheral Interface are contained in registers SPCR (shown in Table 4) and SPSR (shown in Table 5). The SPI data bits are contained in the SPDR register. Writing the SPI data register during serial data transfer sets the Write Collision bit, WCOL, in the SPSR register. The SPDR is double buffered for writing and the values in SPDR are not changed by Reset.

Interrupt Registers The global interrupt enable bit and the individual interrupt enable bits are in the IE register. In addition, the individual interrupt enable bit for the SPI is in the SPCR register. Two priorities can be set for each of the six interrupt sources in the IP register.

Dual Data Pointer Registers To facilitate accessing both internal EEPROM and external data memory, two banks of 16-bit Data Pointer Registers are provided: DP0 at SFR address locations 82H-83H and DP1 at 84H-85H. Bit DPS = 0 in SFR WMCON selects DP0 and DPS = 1 selects DP1. The user should **ALWAYS** initialize the DPS bit to the appropriate value before accessing the respective Data Pointer Register.

Power Off Flag The Power Off Flag (POF) is located at bit_4 (PCON.4) in the PCON SFR. POF is set to "1" during power up. It can be set and reset under software control and is not affected by RESET.

SPCR – SPI Control Register

ddress = D5H — Reset Value = 0000 01XXB

SPIE	SPE	DORD	MSTR	CPOL	CPHA	SPR1	SPR0
7	6	5	4	3	2	1	0

	Function
	SPI Interrupt Enable. This bit, in conjunction with the ES bit in the IE register, enables SPI interrupts: SPIE = 1 and ES = 1 enable SPI interrupts. SPIE = 0 disables SPI interrupts.
	SPI Enable. SPI = 1 enables the SPI channel and connects $\overline{SS}$, MOSI, MISO and SCK to pins P1.4, P1.5, P1.6, and P1.7. SPI = 0 disables the SPI channel.
	Data Order. DORD = 1 selects LSB first data transmission. DORD = 0 selects MSB first data transmission.
	Master/Slave Select. MSTR = 1 selects Master SPI mode. MSTR = 0 selects Slave SPI mode.
	Clock Polarity. When CPOL = 1, SCK is high when idle. When CPOL = 0, SCK of the master device is low when not transmitting. Please refer to figure on SPI Clock Phase and Polarity Control.
	Clock Phase. The CPHA bit together with the CPOL bit controls the clock and data relationship between master and slave. Please refer to figure on SPI Clock Phase and Polarity Control.
	SPI Clock Rate Select. These two bits control the SCK rate of the device configured as master. SPR1 and SPR0 have no effect on the slave. The relationship between SCK and the oscillator frequency, $F_{osc.}$, is as follows: SPR1 SPR0 SCK = $F_{osc.}$ divided by 0 0 4 0 1 16 1 0 64 1 1 128

SPSR – SPI Status Register

ddress = AAH — Reset Value = 00XX XXXXB

SPIF	WCOL	–	–	–	–	–	–
7	6	5	4	3	2	1	0

	Function
	SPI Interrupt Flag. When a serial transfer is complete, the SPIF bit is set and an interrupt is generated if SPIE = 1 and ES = 1. The SPIF bit is cleared by reading the SPI status register with SPIF and WCOL bits set, and then reading/writing the SPI data register.
	Write Collision Flag. The WCOL bit is set if the SPI data register is written during a data transfer. During data transfer, the result of reading the SPDR register may be incorrect, and writing to it has no effect. The WCOL bit (and the SPIF bit) are cleared by reading the SPI status register with SPIF and WCOL set, and then accessing the SPI data register.

SPDR – SPI Data Register

ddress = 86H — Reset Value = unchanged

SPD7	SPD6	SPD5	SPD4	SPD3	SPD2	SPD1	SPD0
7	6	5	4	3	2	1	0

Memory – OM and RAM

The AT89S8252 implements 2K bytes of on-chip EEPROM for data storage and 256 bytes of RAM. The upper 128 bytes of RAM occupy a parallel space to the Special Function Registers. That means the upper 128 bytes have the same addresses as the SFR space but are physically separate from SFR space.

When an instruction accesses an internal location above address 7FH, the address mode used in the instruction specifies whether the CPU accesses the upper 128 bytes of RAM or the SFR space. Instructions that use direct addressing access SFR space.

For example, the following direct addressing instruction accesses the SFR at location 0A0H (which is P2).

```
MOV 0A0H, #data
```

Instructions that use indirect addressing access the upper 128 bytes of RAM. For example, the following indirect addressing instruction, where R0 contains 0A0H, accesses the data byte at address 0A0H, rather than P2 (whose address is 0A0H).

```
MOV @R0, #data
```

Note that stack operations are examples of indirect addressing, so the upper 128 bytes of data RAM are available as stack space.

The on-chip EEPROM data memory is selected by setting the EEMEN bit in the WMCON register at SFR address location 96H. The EEPROM address range is from 000H to 7FFH. The MOVX instructions are used to access the EEPROM. To access off-chip data memory with the MOVX instructions, the EEMEN bit needs to be set to "0".

The EEMWE bit in the WMCON register needs to be set to "1" before any byte location in the EEPROM can be written. User software should reset EEMWE bit to "0" if no further EEPROM write is required. EEPROM write cycles in the serial programming mode are self-timed and typically take 2.5 ms. The progress of EEPROM write can be monitored by reading the RDY/$\overline{BSY}$ bit (read-only) in SFR WMCON. RDY/$\overline{BSY}$ = 0 means

programming is still in progress and RDY/$\overline{BSY}$ = 1 means EEPROM write cycle is completed and another write cycle can be initiated.

In addition, during EEPROM programming, an attempted read from the EEPROM will fetch the byte being written with the MSB complemented. Once the write cycle is completed, true data are valid at all bit locations.

ammable dog Timer

The programmable Watchdog Timer (WDT) operates from an independent internal oscillator. The prescaler bits, PS0, PS1 and PS2 in SFR WMCON are used to set the period of the Watchdog Timer from 16 ms to 2048 ms. The available timer periods are shown in the following table and the actual timer periods (at V_{CC} = 5V) are within ±30% of the nominal.

The WDT is disabled by Power-on Reset and during Power-down. It is enabled by setting the WDTEN bit in SFR WMCON (address = 96H). The WDT is reset by setting the WDTRST bit in WMCON. When the WDT times out without being reset or disabled, an internal RST pulse is generated to reset the CPU.

Table 7. Watchdog Timer Period Selection

WDT Prescaler Bits			Period (nominal)
PS2	PS1	PS0	
0	0	0	16 ms
0	0	1	32 ms
0	1	0	64 ms
0	1	1	128 ms
1	0	0	256 ms
1	0	1	512 ms
1	1	0	1024 ms
1	1	1	2048 ms

) and 1

Timer 0 and Timer 1 in the AT89S8252 operate the same way as Timer 0 and Timer 1 in the AT89C51 and AT89C52. For further information on the timers' operation, refer to the Atmel web site (http://www.atmel.com). From the home page, select "Products", then "Microcontrollers, then "8051-Architecture". Click on "Documentation", then on "Other Documents". Open the document "AT89 Series Hardware Description".

2

Timer 2 is a 16-bit Timer/Counter that can operate as either a timer or an event counter. The type of operation is selected by bit C/$\overline{T2}$ in the SFR T2CON (shown in Table 2). Timer 2 has three operating modes: capture, auto-reload (up or down counting), and baud rate generator. The modes are selected by bits in T2CON, as shown in Table 8.

Timer 2 consists of two 8-bit registers, TH2 and TL2. In the Timer function, the TL2 register is incremented every machine cycle. Since a machine cycle consists of 12 oscillator periods, the count rate is 1/12 of the oscillator frequency.

In the Counter function, the register is incremented in response to a 1-to-0 transition at its corresponding external input pin, T2. In this function, the external input is sampled during S5P2 of every machine cycle. When the samples show a high in one cycle and a low in the next cycle, the count is incremented. The new count value appears in the register during S3P1 of the cycle following the one in which the transition was detected.

Since two machine cycles (24 oscillator periods) are required to recognize a 1-to-0 transition, the maximum count rate is 1/24 of the oscillator frequency. To ensure that a given level is sampled at least once before it changes, the level should be held for at least one full machine cycle.

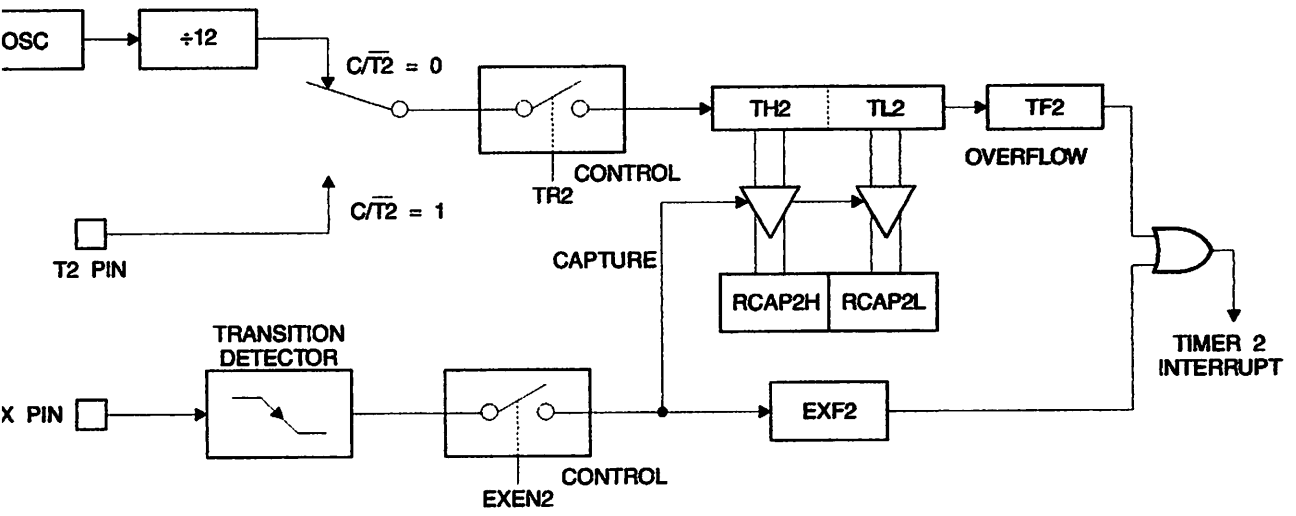
Table 8. Timer 2 Operating Modes

RCLK + TCLK	CP/$\overline{RL2}$	TR2	MODE
0	0	1	16-bit Auto-reload
0	1	1	16-bit Capture
1	X	1	Baud Rate Generator
X	X	0	(Off)

e Mode

In the capture mode, two options are selected by bit EXEN2 in T2CON. If EXEN2 = 0, Timer 2 is a 16-bit timer or counter which upon overflow sets bit TF2 in T2CON. This bit can then be used to generate an interrupt. If EXEN2 = 1, Timer 2 performs the same operation, but a l-to-0 transition at external input T2EX also causes the current value in TH2 and TL2 to be captured into RCAP2H and RCAP2L, respectively. In addition, the transition at T2EX causes bit EXF2 in T2CON to be set. The EXF2 bit, like TF2, can generate an interrupt. The capture mode is illustrated in Figure 1.

. Timer 2 in Capture Mode



load (Up or Down r)

Timer 2 can be programmed to count up or down when configured in its 16-bit auto-reload mode. This feature is invoked by the DCEN (Down Counter Enable) bit located in the SFR T2MOD (see Table 9). Upon reset, the DCEN bit is set to 0 so that timer 2 will default to count up. When DCEN is set, Timer 2 can count up or down, depending on the value of the T2EX pin.

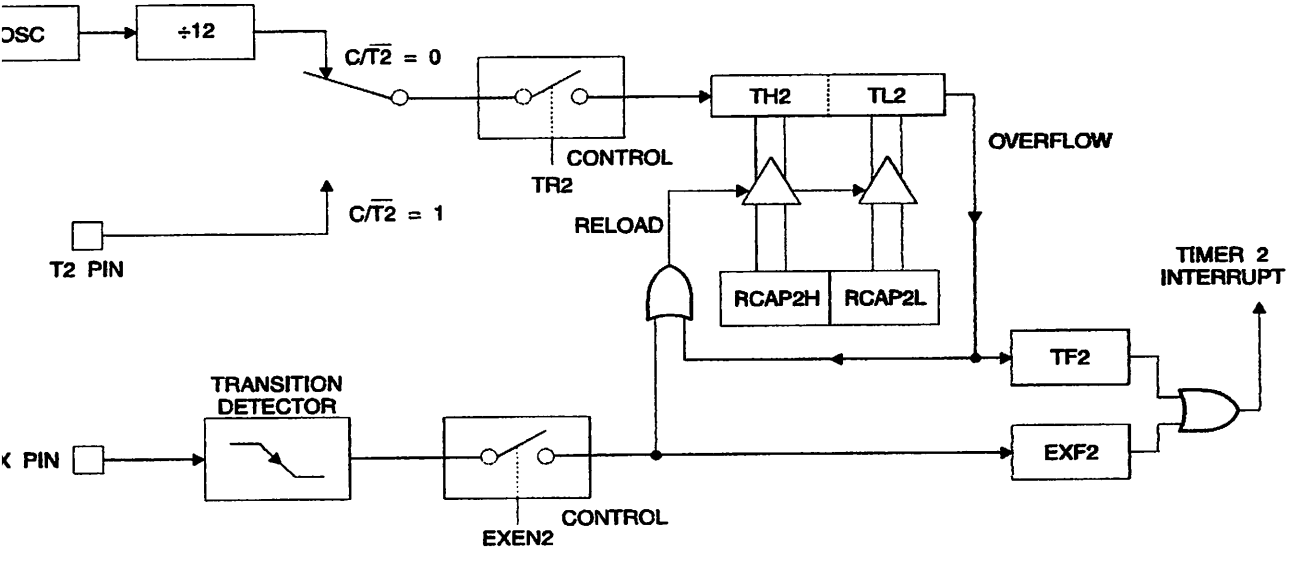
Figure 2 shows Timer 2 automatically counting up when DCEN = 0. In this mode, two options are selected by bit EXEN2 in T2CON. If EXEN2 = 0, Timer 2 counts up to 0FFFFH and then sets the TF2 bit upon overflow. The overflow also causes the timer registers to be reloaded with the 16-bit value in RCAP2H and RCAP2L. The values in RCAP2H and RCAP2L are preset by software. If EXEN2 = 1, a 16-bit reload can be triggered either by an overflow or by a 1-to-0 transition at external input T2EX. This transition also sets the EXF2 bit. Both the TF2 and EXF2 bits can generate an interrupt if enabled.

Setting the DCEN bit enables Timer 2 to count up or down, as shown in Figure 3. In this mode, the T2EX pin controls the direction of the count. A logic 1 at T2EX makes Timer 2 count up. The timer will overflow at 0FFFFH and set the TF2 bit. This overflow also causes the 16-bit value in RCAP2H and RCAP2L to be reloaded into the timer registers, TH2 and TL2, respectively.

A logic 0 at T2EX makes Timer 2 count down. The timer underflows when TH2 and TL2 equal the values stored in RCAP2H and RCAP2L. The underflow sets the TF2 bit and causes 0FFFFH to be reloaded into the timer registers.

The EXF2 bit toggles whenever Timer 2 overflows or underflows and can be used as a 17th bit of resolution. In this operating mode, EXF2 does not flag an interrupt.

. Timer 2 in Auto Reload Mode (DCEN = 0)



T2MOD – Timer 2 Mode Control Register

Address = 0C9H

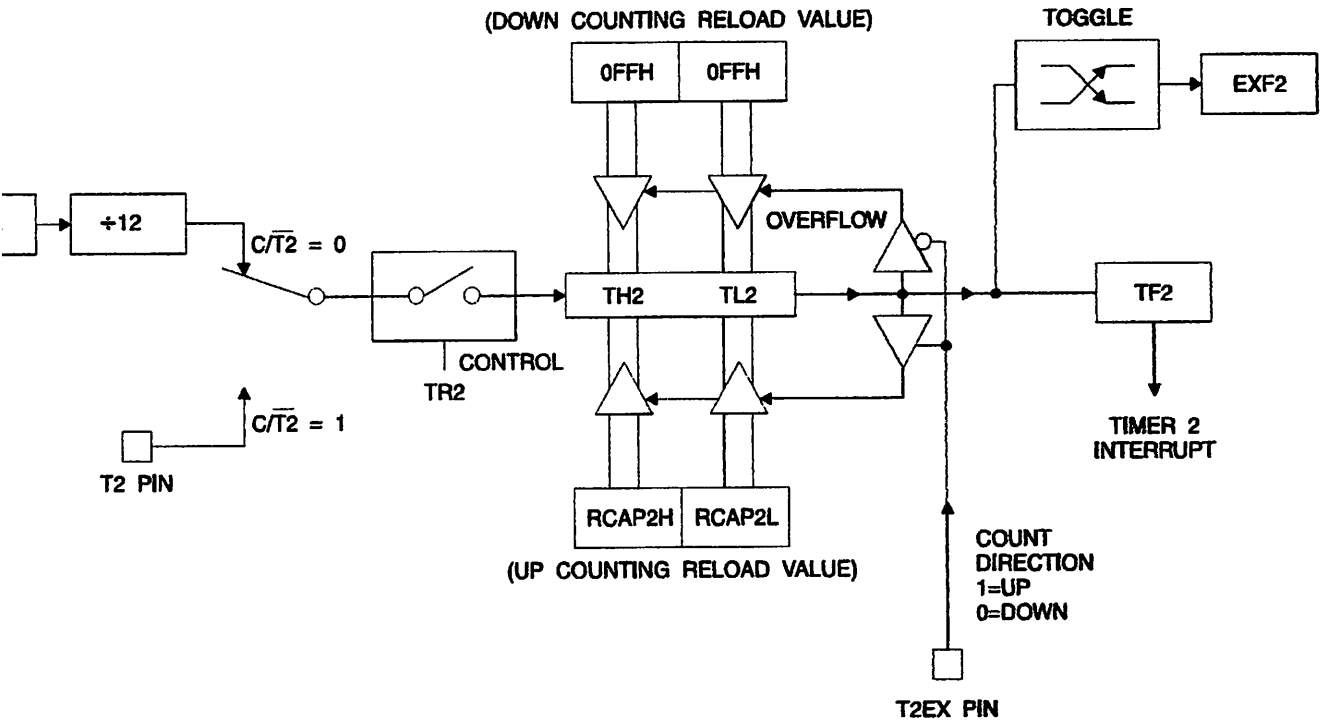
Reset Value = XXXX XX00B

ıddressable

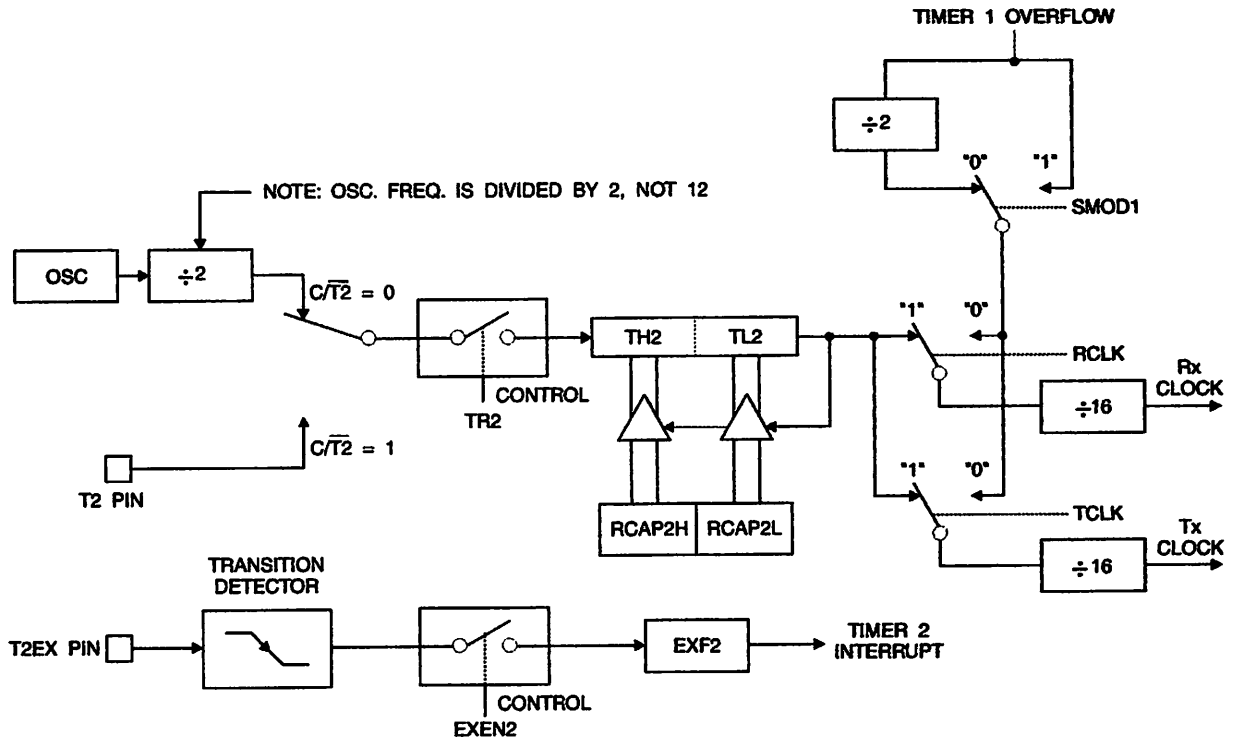
–	–	–	–	–	–	T2OE	DCEN
7	6	5	4	3	2	1	0

	Function
	Not implemented, reserved for future use.
	Timer 2 Output Enable bit.
	When set, this bit allows Timer 2 to be configured as an up/down counter.

. Timer 2 Auto Reload Mode (DCEN = 1)



. Timer 2 in Baud Rate Generator Mode



Rate Generator

Timer 2 is selected as the baud rate generator by setting TCLK and/or RCLK in T2CON (Table 2). Note that the baud rates for transmit and receive can be different if Timer 2 is used for the receiver or transmitter and Timer 1 is used for the other function. Setting RCLK and/or TCLK puts Timer 2 into its baud rate generator mode, as shown in Figure 4.

The baud rate generator mode is similar to the auto-reload mode, in that a rollover in TH2 causes the Timer 2 registers to be reloaded with the 16-bit value in registers RCAP2H and RCAP2L, which are preset by software.

The baud rates in Modes 1 and 3 are determined by Timer 2's overflow rate according to the following equation.

$$\text{Modes 1 and 3 Baud Rates} = \frac{\text{Timer 2 Overflow Rate}}{16}$$

The Timer can be configured for either timer or counter operation. In most applications, it is configured for timer operation ($CP/\overline{T2} = 0$). The timer operation is different for Timer 2 when it is used as a baud rate generator. Normally, as a timer, it increments every machine cycle (at 1/12 the oscillator frequency). As a baud rate generator, however, it increments every state time (at 1/2 the oscillator frequency). The baud rate formula is given below.

$$\frac{\text{Modes 1 and 3}}{\text{Baud Rate}} = \frac{\text{Oscillator Frequency}}{32 \times [65536 - (\text{RCAP2H,RCAP2L})]}$$

where (RCAP2H, RCAP2L) is the content of RCAP2H and RCAP2L taken as a 16-bit unsigned integer.

Timer 2 as a baud rate generator is shown in Figure 4. This figure is valid only if RCLK or TCLK = 1 in T2CON. Note that a rollover in TH2 does not set TF2 and will not generate an interrupt. Note too, that if EXEN2 is set, a 1-to-0 transition in T2EX will set EXF2 but will not cause a reload from (RCAP2H, RCAP2L) to (TH2, TL2). Thus when Timer 2 is in use as a baud rate generator, T2EX can be used as an extra external interrupt.

Note that when Timer 2 is running (TR2 = 1) as a timer in the baud rate generator mode, TH2 or TL2 should not be read from or written to. Under these conditions, the Timer is incremented every state time, and the results of a read or write may not be accurate. The RCAP2 registers may be read but should not be written to, because a write might overlap a reload and cause write and/or reload errors. The timer should be turned off (clear TR2) before accessing the Timer 2 or RCAP2 registers.

ammable Out

A 50% duty cycle clock can be programmed to come out on P1.0, as shown in Figure 5. This pin, besides being a regular I/O pin, has two alternate functions. It can be programmed to input the external clock for Timer/Counter 2 or to output a 50% duty cycle clock ranging from 61 Hz to 4 MHz (for a 16-MHz operating frequency).

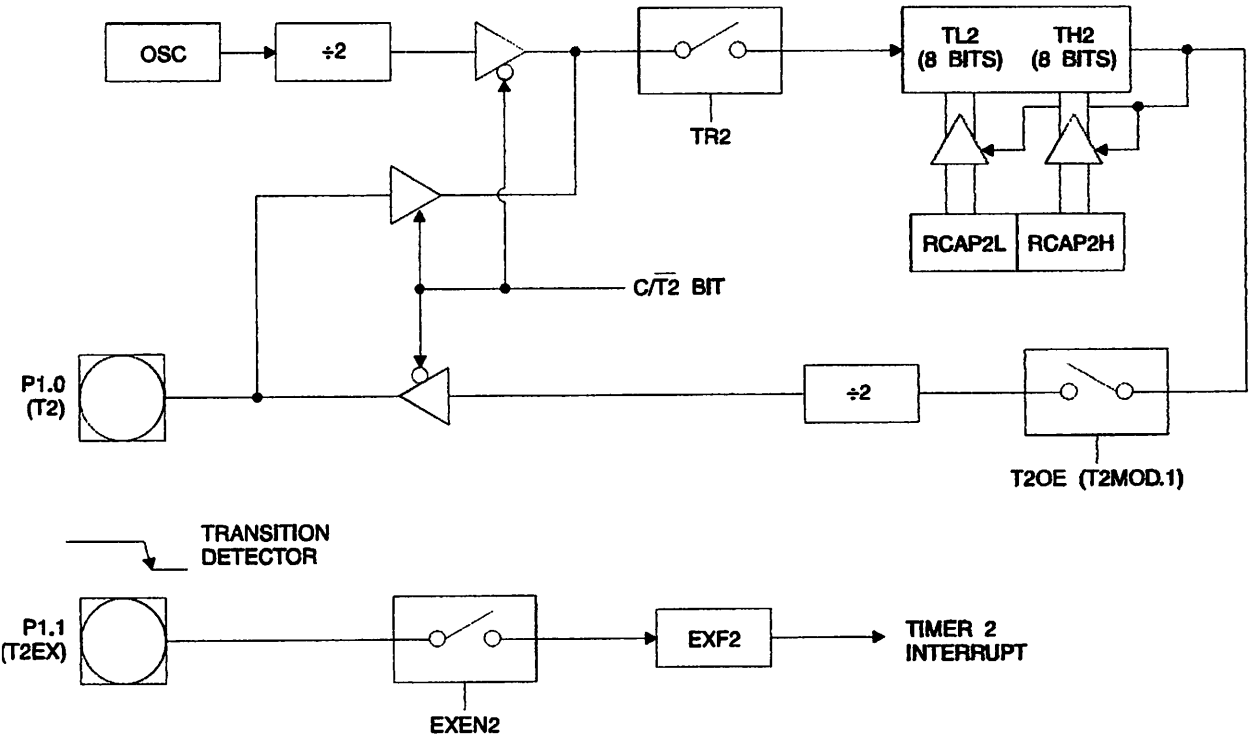
To configure the Timer/Counter 2 as a clock generator, bit $C/\overline{T2}$ (T2CON.1) must be cleared and bit T2OE (T2MOD.1) must be set. Bit TR2 (T2CON.2) starts and stops the timer.

The clock-out frequency depends on the oscillator frequency and the reload value of Timer 2 capture registers (RCAP2H, RCAP2L), as shown in the following equation.

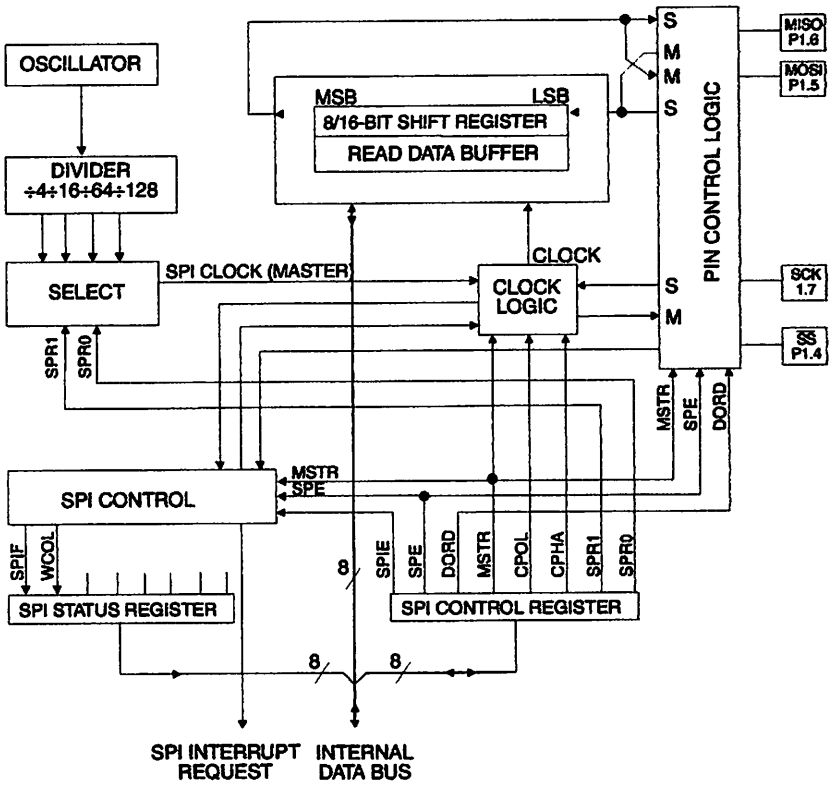
$$\text{Clock Out Frequency} = \frac{\text{Oscillator Frequency}}{4 \times [65536 - (\text{RCAP2H,RCAP2L})]}$$

In the clock-out mode, Timer 2 rollovers will not generate an interrupt. This behavior is similar to when Timer 2 is used as a baud-rate generator. It is possible to use Timer 2 as a baud-rate generator and a clock generator simultaneously. Note, however, that the baud-rate and clock-out frequencies cannot be determined independently from one another since they both use RCAP2H and RCAP2L.

. Timer 2 in Clock-out Mode



. SPI Block Diagram



The UART in the AT89S8252 operates the same way as the UART in the AT89C51 and AT89C52. For further information on the UART operation, refer to the Atmel web site (http://www.atmel.com). From the home page, select "Products", then "Microcontrollers, then "8051-Architecture". Click on "Documentation", then on "Other Documents". Open the document "AT89 Series Hardware Description".

Peripheral ıce

The serial peripheral interface (SPI) allows high-speed synchronous data transfer between the AT89S8252 and peripheral devices or between several AT89S8252 devices. The AT89S8252 SPI features include the following:

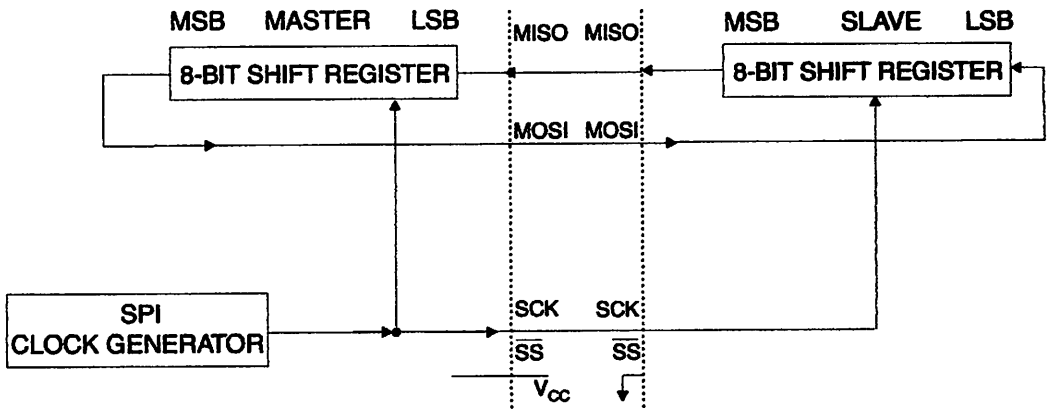
- Full-Duplex, 3-Wire Synchronous Data Transfer
- Master or Slave Operation
- 1.5 MHz Bit Frequency (max.)
- LSB First or MSB First Data Transfer
- Four Programmable Bit Rates
- End of Transmission Interrupt Flag
- Write Collision Flag Protection
- Wakeup from Idle Mode (Slave Mode Only)

The interconnection between master and slave CPUs with SPI is shown in the following figure. The SCK pin is the clock output in the master mode but is the clock input in the slave mode. Writing to the SPI data register of the master CPU starts the SPI clock generator, and the data written shifts out of the MOSI pin and into the MOSI pin of the slave CPU. After shifting one byte, the SPI clock generator stops, setting the end of transmission flag (SPIF). If both the SPI interrupt enable bit (SPIE) and the serial port interrupt enable bit (ES) are set, an interrupt is requested.

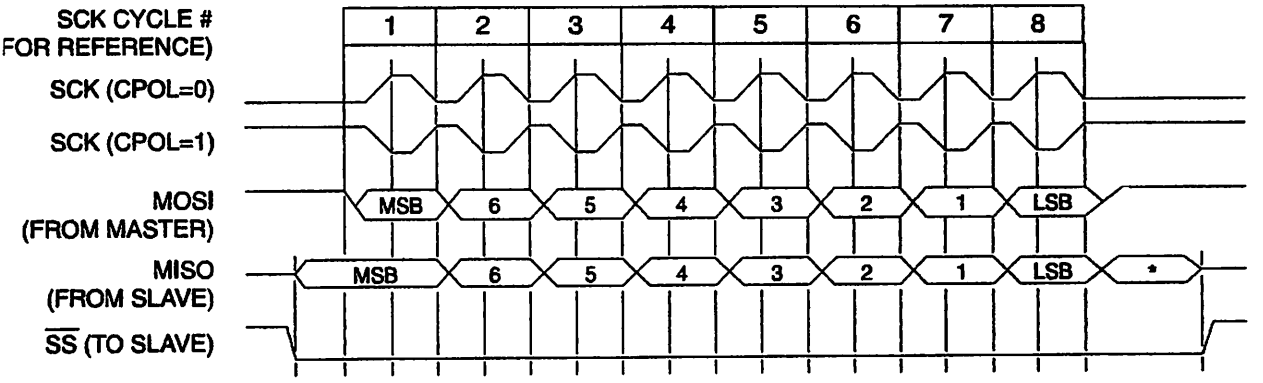
The Slave Select input, $\overline{SS}$/P1.4, is set low to select an individual SPI device as a slave. When $\overline{SS}$/P1.4 is set high, the SPI port is deactivated and the MOSI/P1.5 pin can be used as an input.

There are four combinations of SCK phase and polarity with respect to serial data, which are determined by control bits CPHA and CPOL. The SPI data transfer formats are shown in Figure 8 and Figure 9.

'. SPI Master-slave Interconnection

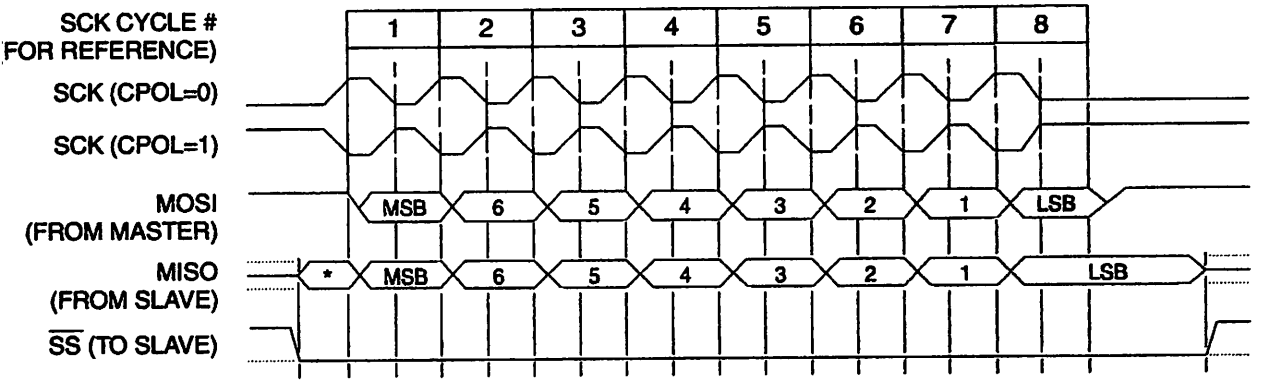


. SPI transfer Format with CPHA = 0



Not defined but normally MSB of character just received

. SPI Transfer Format with CPHA = 1



'Not defined but normally LSB of previously transmitted character.

upts

The AT89S8252 has a total of six interrupt vectors: two external interrupts ($\overline{INT0}$ and $\overline{INT1}$), three timer interrupts (Timers 0, 1, and 2), and the serial port interrupt. These interrupts are all shown in Figure 10.

Each of these interrupt sources can be individually enabled or disabled by setting or clearing a bit in Special Function Register IE. IE also contains a global disable bit, EA, which disables all interrupts at once.

Note that Table 10 shows that bit position IE.6 is unimplemented. In the AT89C51, bit position IE.5 is also unimplemented. User software should not write 1s to these bit positions, since they may be used in future AT89 products.

Timer 2 interrupt is generated by the logical OR of bits TF2 and EXF2 in register T2CON. Neither of these flags is cleared by hardware when the service routine is vectored to. In fact, the service routine may have to determine whether it was TF2 or EXF2 that generated the interrupt, and that bit will have to be cleared in software.

The Timer 0 and Timer 1 flags, TF0 and TF1, are set at S5P2 of the cycle in which the timers overflow. The values are then polled by the circuitry in the next cycle. However, the Timer 2 flag, TF2, is set at S2P2 and is polled in the same cycle in which the timer overflows.

. Interrupt Enable (IE) Register

SB)

EA	–	ET2	ES	ET1	EX1	ET0	EX0

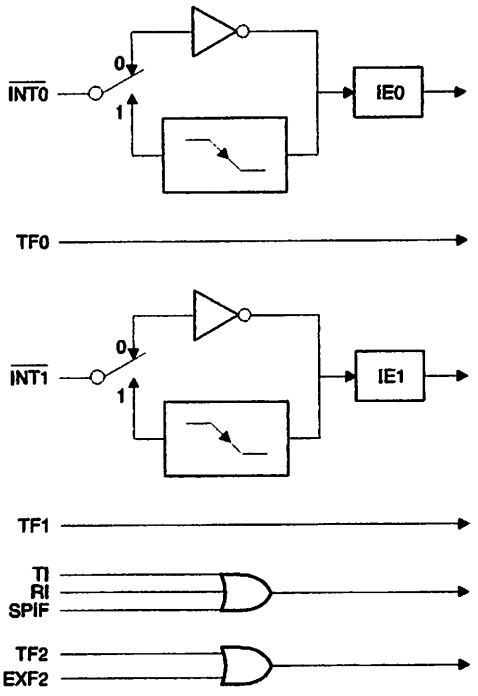
Enable Bit = 1 enables the interrupt.

Enable Bit = 0 disables the interrupt.

mbol	Position	Function
EA	IE.7	Disables all interrupts. If EA = 0, no interrupt is acknowledged. If EA = 1, each interrupt source is individually enabled or disabled by setting or clearing its enable bit.
–	IE.6	Reserved.
ET2	IE.5	Timer 2 interrupt enable bit.
ES	IE.4	SPI and UART interrupt enable bit.
ET1	IE.3	Timer 1 interrupt enable bit.
EX1	IE.2	External interrupt 1 enable bit.
ET0	IE.1	Timer 0 interrupt enable bit.
EX0	IE.0	External interrupt 0 enable bit.

tware should never write 1s to unimplemented bits, because they may be used in future AT89 products.

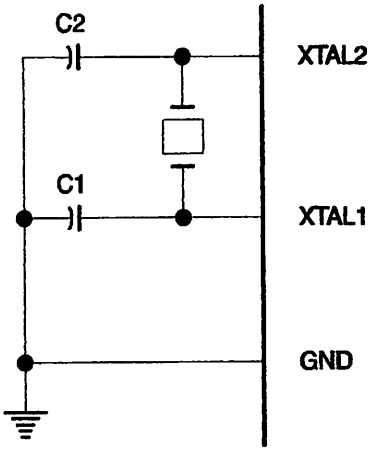
0. Interrupt Sources



ıtor cteristics

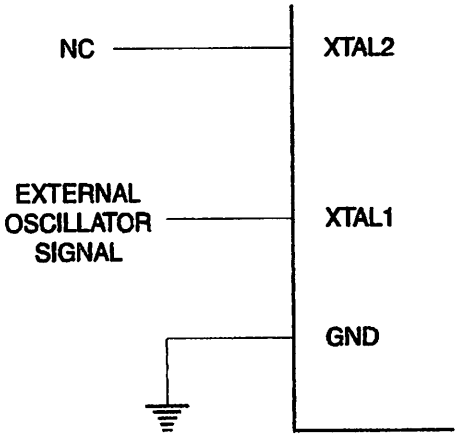
XTAL1 and XTAL2 are the input and output, respectively, of an inverting amplifier that can be configured for use as an on-chip oscillator, as shown in Figure 11. Either a quartz crystal or ceramic resonator may be used. To drive the device from an external clock source, XTAL2 should be left unconnected while XTAL1 is driven, as shown in Figure 12. There are no requirements on the duty cycle of the external clock signal, since the input to the internal clocking circuitry is through a divide-by-two flip-flop, but minimum and maximum voltage high and low time specifications must be observed.

Figure 11. Oscillator Connections



Note: C1, C2 = 30 pF ± 10 pF for Crystals
= 40 pF ± 10 pF for Ceramic Resonators

Figure 12. External Clock Drive Configuration



ode

In idle mode, the CPU puts itself to sleep while all the on-chip peripherals remain active. The mode is invoked by software. The content of the on-chip RAM and all the special functions registers remain unchanged during this mode. The idle mode can be terminated by any enabled interrupt or by a hardware reset.

Note that when idle mode is terminated by a hardware reset, the device normally resumes program execution from where it left off, up to two machine cycles before the internal reset algorithm takes control. On-chip hardware inhibits access to internal RAM in this event, but access to the port pins is not inhibited. To eliminate the possibility of an unexpected write to a port pin when idle mode is terminated by a reset, the instruction following the one that invokes idle mode should not write to a port pin or to external memory.

Status of External Pins During Idle and Power-down Modes

Mode	Program Memory	ALE	$\overline{PSEN}$	PORT0	PORT1	PORT2	PORT3
Idle	Internal	1	1	Data	Data	Data	Data
Idle	External	1	1	Float	Data	Address	Data
Power-down	Internal	0	0	Data	Data	Data	Data
Power-down	External	0	0	Float	Data	Data	Data

-down Mode

In the power-down mode, the oscillator is stopped and the instruction that invokes power-down is the last instruction executed. The on-chip RAM and Special Function Registers retain their values until the power-down mode is terminated. Exit from power-down can be initiated either by a hardware reset or by an enabled external interrupt. Reset redefines the SFRs but does not change the on-chip RAM. The reset should not be activated before V_{CC} is restored to its normal operating level and must be held active long enough to allow the oscillator to restart and stabilize.

To exit power-down via an interrupt, the external interrupt must be enabled as level sensitive before entering power-down. The interrupt service routine starts at 16 ms (nominal) after the enabled interrupt pin is activated.

am Memory Bits

The AT89S8252 has three lock bits that can be left unprogrammed (U) or can be programmed (P) to obtain the additional features listed in the following table.

When lock bit 1 is programmed, the logic level at the $\overline{EA}$ pin is sampled and latched during reset. If the device is powered up without a reset, the latch initializes to a random value and holds that value until reset is activated. The latched value of $\overline{EA}$ must agree with the current logic level at that pin in order for the device to function properly.

Once programmed, the lock bits can only be unprogrammed with the Chip Erase operations in either the parallel or serial modes.

it Protection Modes[1][2]

Program Lock Bits			
LB1	LB2	LB3	Protection Type
U	U	U	No internal memory lock feature.
P	U	U	MOVC instructions executed from external program memory are disabled from fetching code bytes from internal memory. $\overline{EA}$ is sampled and latched on reset and further programming of the Flash memory (parallel or serial mode) is disabled.
P	P	U	Same as Mode 2, but parallel or serial verify are also disabled.
P	P	P	Same as Mode 3, but external execution is also disabled.

1. U = Unprogrammed
2. P = Programmed

amming the and EEPROM

Atmel's AT89S8252 Flash Microcontroller offers 8K bytes of in-system reprogrammable Flash Code memory and 2K bytes of EEPROM Data memory.

The AT89S8252 is normally shipped with the on-chip Flash Code and EEPROM Data memory arrays in the erased state (i.e. contents = FFH) and ready to be programmed. This device supports a High-voltage (12-V V_{PP}) Parallel programming mode and a Low-voltage (5-V V_{CC}) Serial programming mode. The serial programming mode provides a convenient way to reprogram the AT89S8252 inside the user's system. The parallel programming mode is compatible with conventional third party Flash or EPROM programmers.

The Code and Data memory arrays are mapped via separate address spaces in the serial programming mode. In the parallel programming mode, the two arrays occupy one contiguous address space: 0000H to 1FFFH for the Code array and 2000H to 27FFH for the Data array.

The Code and Data memory arrays on the AT89S8252 are programmed byte-by-byte in either programming mode. An auto-erase cycle is provided with the self-timed programming operation in the serial programming mode. There is no need to perform the Chip Erase operation to reprogram any memory location in the serial programming mode unless any of the lock bits have been programmed.

In the parallel programming mode, there is no auto-erase cycle. To reprogram any non-blank byte, the user needs to use the Chip Erase operation first to erase both arrays.

Parallel Programming Algorithm: To program and verify the AT89S8252 in the parallel programming mode, the following sequence is recommended:

1. Power-up sequence:
   Apply power between V_{CC} and GND pins.
   Set RST pin to "H".
   Apply a 3 MHz to 24 MHz clock to XTAL1 pin and wait for at least 10 milliseconds.
2. Set $\overline{PSEN}$ pin to "L"
   ALE pin to "H"
   $\overline{EA}$ pin to "H" and all other pins to "H".
3. Apply the appropriate combination of "H" or "L" logic levels to pins P2.6, P2.7, P3.6, P3.7 to select one of the programming operations shown in the Flash Programming Modes table.
4. Apply the desired byte address to pins P1.0 to P1.7 and P2.0 to P2.5.
   Apply data to pins P0.0 to P0.7 for Write Code operation.
5. Raise $\overline{EA}/V_{PP}$ to 12V to enable Flash programming, erase or verification.
6. Pulse ALE/$\overline{PROG}$ once to program a byte in the Code memory array, the Data memory array or the lock bits. The byte-write cycle is self-timed and typically takes 1.5 ms.
7. To verify the byte just programmed, bring pin P2.7 to "L" and read the programmed data at pins P0.0 to P0.7.
8. Repeat steps 3 through 7 changing the address and data for the entire 2K or 8K bytes array or until the end of the object file is reached.
9. Power-off sequence:
   Set XTAL1 to "L".
   Set RST and $\overline{EA}$ pins to "L".
   Turn V_{CC} power off.

In the parallel programming mode, there is no auto-erase cycle and to reprogram any non-blank byte, the user needs to use the Chip Erase operation first to erase both arrays.

$\overline{\text{Data}}$ Polling: The AT89S8252 features $\overline{\text{DATA}}$ Polling to indicate the end of a byte write cycle. During a byte write cycle in the parallel or serial programming mode, an attempted read of the last byte written will result in the complement of the written datum on P0.7 (parallel mode), and on the MSB of the serial output byte on MISO (serial mode). Once the write cycle has been completed, true data are valid on all outputs, and the next cycle may begin. $\overline{\text{DATA}}$ Polling may begin any time after a write cycle has been initiated.

Ready/$\overline{\text{Busy}}$: The progress of byte programming in the parallel programming mode can also be monitored by the RDY/$\overline{\text{BSY}}$ output signal. Pin P3.4 is pulled Low after ALE goes High during programming to indicate $\overline{\text{BUSY}}$. P3.4 is pulled High again when programming is done to indicate READY.

Program Verify: If lock bits LB1 and LB2 have not been programmed, the programmed Code or Data byte can be read back via the address and data lines for verification. The state of the lock bits can also be verified directly in the parallel programming mode. In the serial programming mode, the state of the lock bits can only be verified indirectly by observing that the lock bit features are enabled.

Chip Erase: Both Flash and EEPROM arrays are erased electrically at the same time. In the parallel programming mode, chip erase is initiated by using the proper combination of control signals and by holding ALE/$\overline{\text{PROG}}$ low for 10 ms. The Code and Data arrays are written with all "1"s in the Chip Erase operation.

In the serial programming mode, a chip erase operation is initiated by issuing the Chip Erase instruction. In this mode, chip erase is self-timed and takes about 16 ms.

During chip erase, a serial read from any address location will return 00H at the data outputs.

Serial Programming Fuse: A programmable fuse is available to disable Serial Programming if the user needs maximum system security. The Serial Programming Fuse can only be programmed or erased in the Parallel Programming Mode.

The AT89S8252 is shipped with the Serial Programming Mode enabled.

Reading the Signature Bytes: The signature bytes are read by the same procedure as a normal verification of locations 030H and 031H, except that P3.6 and P3.7 must be pulled to a logic low. The values returned are as follows:

(030H) = 1EH indicates manufactured by Atmel
(031H) = 72H indicates 89S8252

amming ace

Every code byte in the Flash and EEPROM arrays can be written, and the entire array can be erased, by using the appropriate combination of control signals. The write operation cycle is self-timed and once initiated, will automatically time itself to completion.

Most worldwide major programming vendors offer support for the Atmel AT89 microcontroller series. Please contact your local programming vendor for the appropriate software revision.

Downloading

Both the Code and Data memory arrays can be programmed using the serial SPI bus while RST is pulled to V_{CC}. The serial interface consists of pins SCK, MOSI (input) and MISO (output). After RST is set high, the Programming Enable instruction needs to be executed first before program/erase operations can be executed.

An auto-erase cycle is built into the self-timed programming operation (in the serial mode ONLY) and there is no need to first execute the Chip Erase instruction unless any of the lock bits have been programmed. The Chip Erase operation turns the content of every memory location in both the Code and Data arrays into FFH.

The Code and Data memory arrays have separate address spaces:

0000H to 1FFFH for Code memory and 000H to 7FFH for Data memory.

Either an external system clock is supplied at pin XTAL1 or a crystal needs to be connected across pins XTAL1 and XTAL2. The maximum serial clock (SCK) frequency should be less than 1/40 of the crystal frequency. With a 24 MHz oscillator clock, the maximum SCK frequency is 600 kHz.

Programming hm

To program and verify the AT89S8252 in the serial programming mode, the following sequence is recommended:

1. Power-up sequence:

   Apply power between VCC and GND pins.

   Set RST pin to "H".

   If a crystal is not connected across pins XTAL1 and XTAL2, apply a 3 MHz to 24 MHz clock to XTAL1 pin and wait for at least 10 milliseconds.
2. Enable serial programming by sending the Programming Enable serial instruction to pin MOSI/P1.5. The frequency of the shift clock supplied at pin SCK/P1.7 needs to be less than the CPU clock at XTAL1 divided by 40.
3. The Code or Data array is programmed one byte at a time by supplying the address and data together with the appropriate Write instruction. The selected memory location is first automatically erased before new data is written. The write cycle is self-timed and typically takes less than 2.5 ms at 5V.
4. Any memory location can be verified by using the Read instruction which returns the content at the selected address at serial output MISO/P1.6.
5. At the end of a programming session, RST can be set low to commence normal operation.
6. Power-off sequence (if needed):

   Set XTAL1 to "L" (if a crystal is not used).

   Set RST to "L".

   Turn V_{CC} power off.

›rogramming tion

The Instruction Set for Serial Programming follows a 3-byte protocol and is shown in the following table:

on Set

ion	Input Format			Operation
	Byte 1	Byte 2	Byte 3	
ıming Enable	1010 1100	0101 0011	xxxx xxxx	Enable serial programming interface after RST goes high.
ıse	1010 1100	xxxx x100	xxxx xxxx	Chip erase both 8K & 2K memory arrays.
ɔde Memory	aaaa a001	low addr	xxxx xxxx	Read data from Code memory array at the selected address. The 5 MSBs of the first byte are the high order address bits. The low order address bits are in the second byte. Data are available at pin MISO during the third byte.
ɔde Memory	aaaa a010	low addr	data in	Write data to Code memory location at selected address. The address bits are the 5 MSBs of the first byte together with the second byte.
ata Memory	00aa a101	low addr	xxxx xxxx	Read data from Data memory array at selected address. Data are available at pin MISO during the third byte.
ata Memory	00aa a110	low addr	data in	Write data to Data memory location at selected address.
ɔck Bits	1010 1100	LB1 LB2 LB3 x x111	xxxx xxxx	Write lock bits. Set LB1, LB2 or LB3 = "0" to program lock bits.

1. DATA polling is used to indicate the end of a byte write cycle which typically takes less than 2.5 ms at 5V.
2. "aaaaa" = high order address.
3. "x" = don't care.

and EEPROM Parallel Programming Modes

	RST	PSEN	ALE/PROG	EA/V_{PP}	P2.6	P2.7	P3.6	P3.7	Data I/O P0.7:0	Address P2.5:0 P1.7:0
g. Modes	H	h[1]	h[1]	x						
e	H	L	(2)	12V	H	L	L	L	X	X
K bytes) Memory	H	L		12V	L	H	H	H	DIN	ADDR
K bytes) Memory	H	L	H	12V	L	L	H	H	DOUT	ADDR
k Bits:	H	L		12V	H	L	H	L	DIN	X
Bit - 1									P0.7 = 0	X
Bit - 2									P0.6 = 0	X
Bit - 3									P0.5 = 0	X
k Bits:	H	L	H	12V	H	H	L	L	DOUT	X
Bit - 1									@P0.2	X
Bit - 2									@P0.1	X
Bit - 3									@P0.0	X
nel Code	H	L	H	12V	L	L	L	L	DOUT	30H
vice Code	H	L	H	12V	L	L	L	L	DOUT	31H
g. Enable	H	L	(2)	12V	L	H	L	H	P0.0 = 0	X
g. Disable	H	L	(2)	12V	L	H	L	H	P0.0 = 1	X
rial Prog. Fuse	H	L	H	12V	H	H	L	H	@P0.0	X

1. "h" = weakly pulled "High" internally.
2. Chip Erase and Serial Programming Fuse require a 10 ms $\overline{\text{PROG}}$ pulse. Chip Erase needs to be performed first before reprogramming any byte with a content other than FFH.
3. P3.4 is pulled Low during programming to indicate RDY/$\overline{\text{BSY}}$.
4. "X" = don't care

3. Programming the Flash/EEPROM Memory

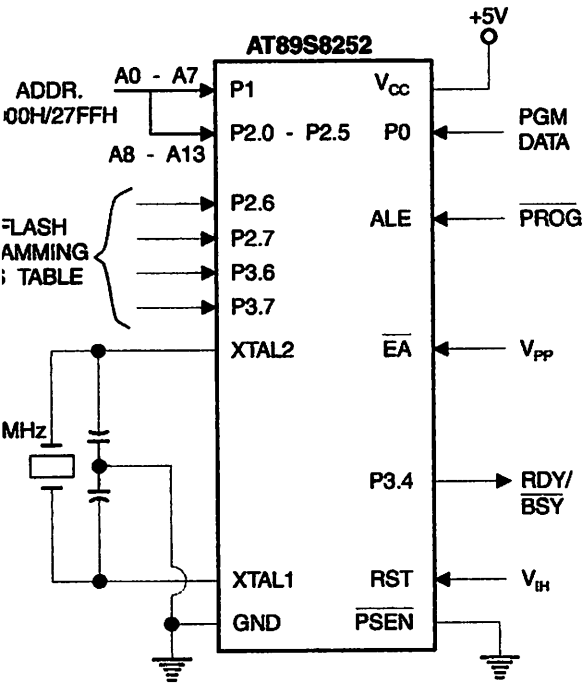
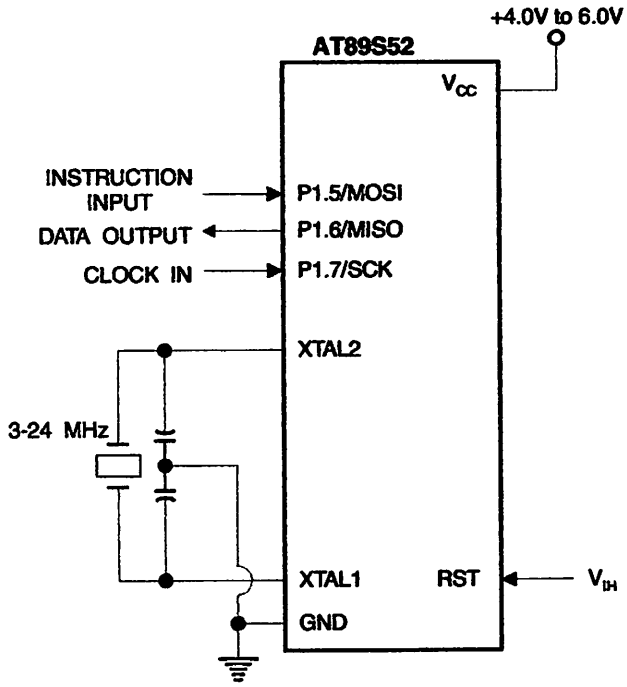
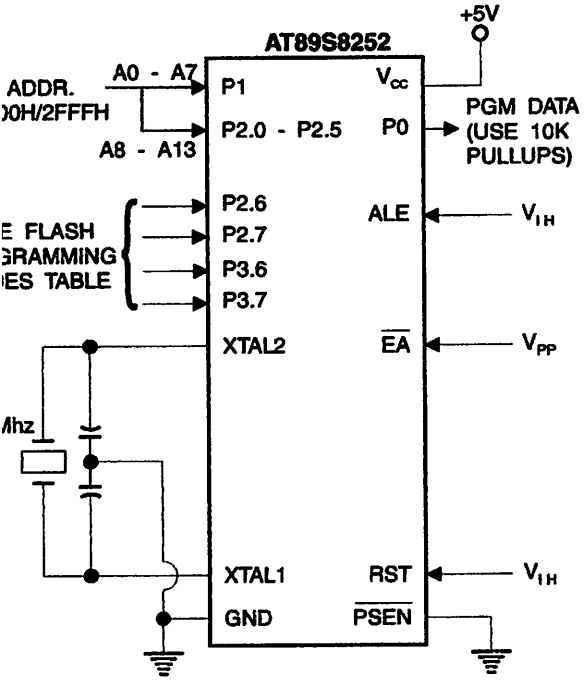


Figure 15. Flash/EEPROM Serial Downloading



4. Verifying the Flash/EEPROM Memory

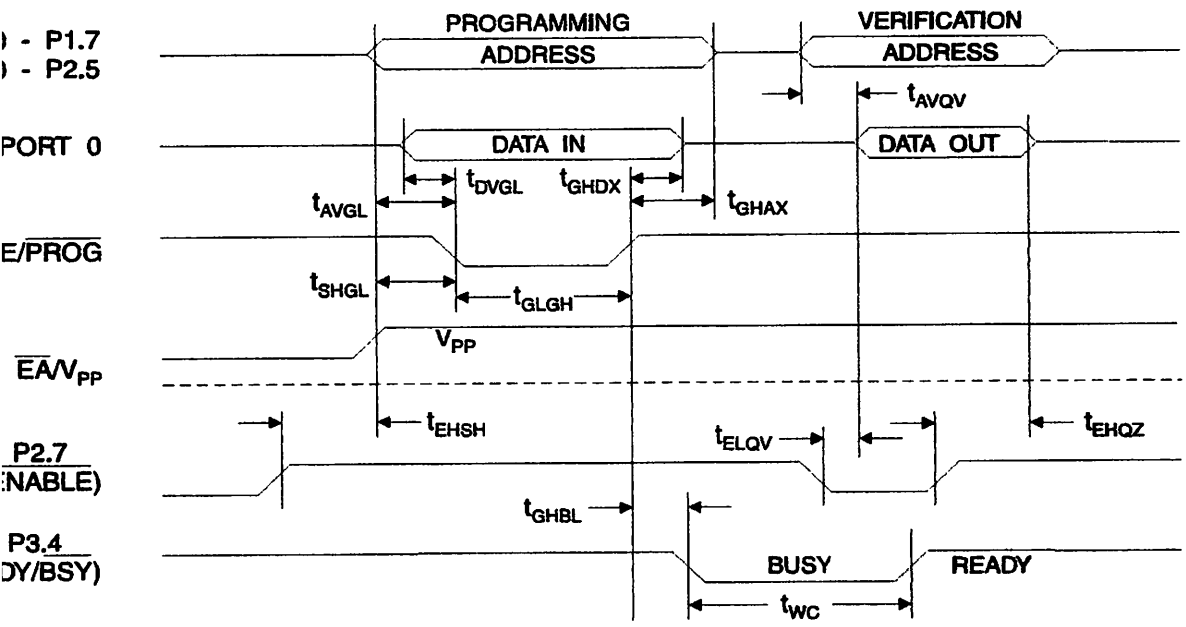


Programming and Verification Characteristics – Parallel Mode

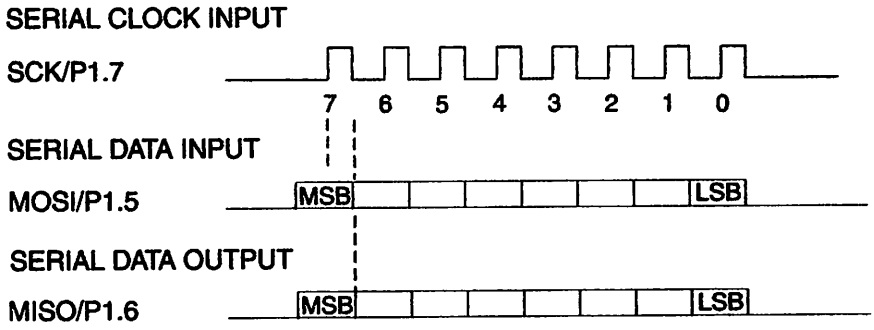
to 70°C, V_{CC} = 5.0V ± 10%

Parameter	Min	Max	Units
Programming Enable Voltage	11.5	12.5	V
Programming Enable Current		1.0	mA
Oscillator Frequency	3	24	MHz
Address Setup to $\overline{PROG}$ Low	$48t_{CLCL}$		
Address Hold after $\overline{PROG}$	$48t_{CLCL}$		
Data Setup to $\overline{PROG}$ Low	$48t_{CLCL}$		
Data Hold after $\overline{PROG}$	$48t_{CLCL}$		
P2.7 ($\overline{ENABLE}$) High to V_{PP}	$48t_{CLCL}$		
V_{PP} Setup to $\overline{PROG}$ Low	10		µs
$\overline{PROG}$ Width	1	110	µs
Address to Data Valid		$48t_{CLCL}$	
$\overline{ENABLE}$ Low to Data Valid		$48t_{CLCL}$	
Data Float after $\overline{ENABLE}$	0	$48t_{CLCL}$	
$\overline{PROG}$ High to $\overline{BUSY}$ Low		1.0	µs
Byte Write Cycle Time		2.0	ms

/EEPROM Programming and Verification Waveforms – Parallel Mode

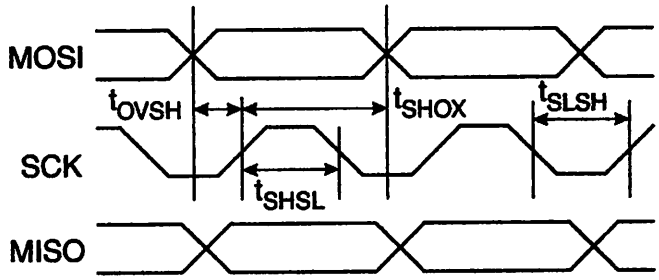


Downloading Waveforms



Programming Characteristics

6. Serial Programming Timing



. Serial Programming Characteristics, T_A = -40°C to 85°C, V_{CC} = 4.0 - 6.0V (Unless Otherwise Noted)

	Parameter	Min	Typ	Max	Units
	Oscillator Frequency	0		24	MHz
	Oscillator Period	41.6			ns
	SCK Pulse Width High	24 t_{CLCL}			ns
	SCK Pulse Width Low	24 t_{CLCL}			ns
	MOSI Setup to SCK High	t_{CLCL}			ns
	MOSI Hold after SCK High	2 t_{CLCL}			ns

ute Maximum Ratings*

g Temperature	-55°C to +125°C
Temperature	-65°C to +150°C
on Any Pin pect to Ground	-1.0V to +7.0V
n Operating Voltage	6.6V
ut Current	15.0 mA

*NOTICE: Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

haracteristics

es shown in this table are valid for T_A = -40°C to 85°C and V_{CC} = 5.0V ± 20%, unless otherwise noted.

	Parameter	Condition	Min	Max	Units
	Input Low-voltage	(Except $\overline{EA}$)	-0.5	0.2 V_{CC} - 0.1	V
	Input Low-voltage ($\overline{EA}$)		-0.5	0.2 V_{CC} - 0.3	V
	Input High-voltage	(Except XTAL1, RST)	0.2 V_{CC} + 0.9	V_{CC} + 0.5	V
	Input High-voltage	(XTAL1, RST)	0.7 V_{CC}	V_{CC} + 0.5	V
	Output Low-voltage (1) (Ports 1,2,3)	I_{OL} = 1.6 mA		0.5	V
	Output Low-voltage (1) (Port 0, ALE, $\overline{PSEN}$)	I_{OL} = 3.2 mA		0.5	V
	Output High-voltage (Ports 1,2,3, ALE, $\overline{PSEN}$)	I_{OH} = -60 µA, V_{CC} = 5V ± 10%	2.4		V
		I_{OH} = -25 µA	0.75 V_{CC}		V
		I_{OH} = -10 µA	0.9 V_{CC}		V
	Output High-voltage (Port 0 in External Bus Mode)	I_{OH} = -800 µA, V_{CC} = 5V ± 10%	2.4		V
		I_{OH} = -300 µA	0.75 V_{CC}		V
		I_{OH} = -80 µA	0.9 V_{CC}		V
	Logical 0 Input Current (Ports 1,2,3)	V_{IN} = 0.45V		-50	µA
	Logical 1 to 0 Transition Current (Ports 1,2,3)	V_{IN} = 2V, V_{CC} = 5V ± 10%		-650	µA
	Input Leakage Current (Port 0, $\overline{EA}$)	0.45 < V_{IN} < V_{CC}		±10	µA
	Reset Pull-down Resistor		50	300	KΩ
	Pin Capacitance	Test Freq. = 1 MHz, T_A = 25°C		10	pF
	Power Supply Current	Active Mode, 12 MHz		25	mA
		Idle Mode, 12 MHz		6.5	mA
	Power-down Mode (2)	V_{CC} = 6V		100	µA
		V_{CC} = 3V		40	µA

1. Under steady state (non-transient) conditions, I_{OL} must be externally limited as follows:
   Maximum I_{OL} per port pin: 10 mA
   Maximum I_{OL} per 8-bit port: Port 0: 26 mA; Ports 1, 2, 3: 15 mA
   Maximum total I_{OL} for all output pins: 71 mA
   If I_{OL} exceeds the test condition, V_{OL} may exceed the related specification. Pins are not guaranteed to sink current greater than the listed test conditions.
2. Minimum V_{CC} for Power-down is 2V

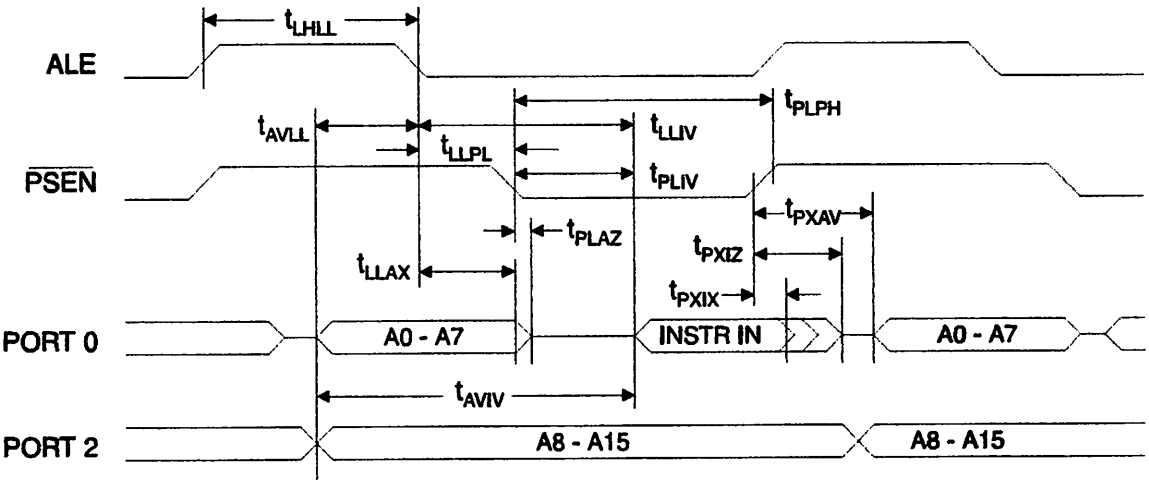
ıaracteristics

ıerating conditions, load capacitance for Port 0, ALE/$\overline{PROG}$, and $\overline{PSEN}$ = 100 pF; load capacitance for all other : 80 pF.

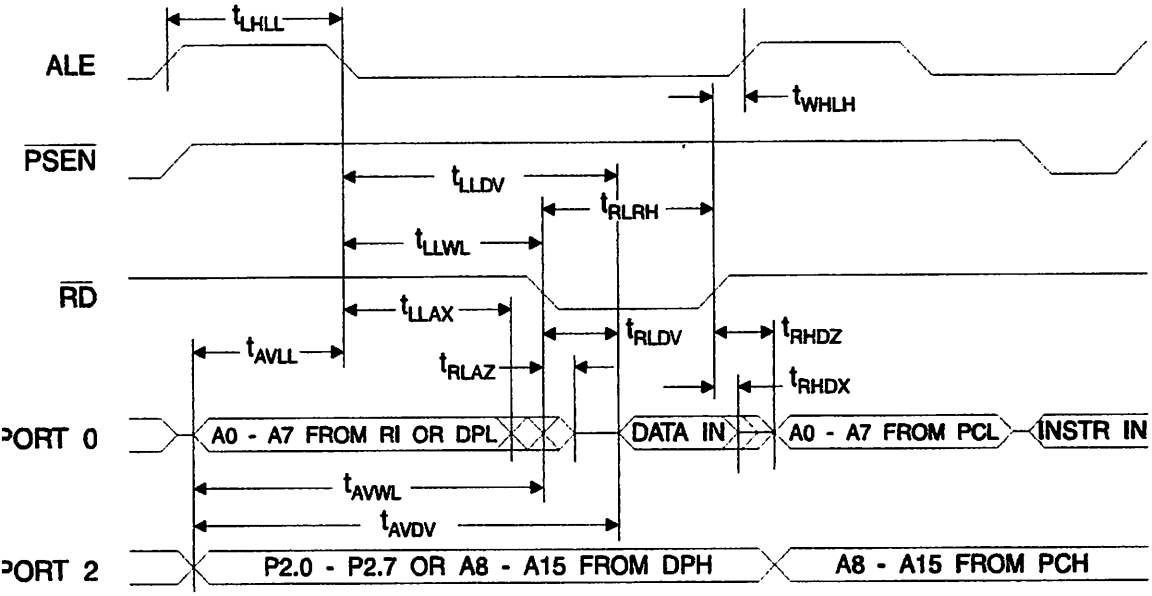
al Program and Data Memory Characteristics

Parameter	Variable Oscillator		Units
	Min	Max	
Oscillator Frequency	0	24	MHz
ALE Pulse Width	$2t_{CLCL}$ - 40		ns
Address Valid to ALE Low	t_{CLCL} - 13		ns
Address Hold after ALE Low	t_{CLCL} - 20		ns
ALE Low to Valid Instruction In		$4t_{CLCL}$ - 65	ns
ALE Low to $\overline{PSEN}$ Low	t_{CLCL} - 13		ns
$\overline{PSEN}$ Pulse Width	$3t_{CLCL}$ - 20		ns
$\overline{PSEN}$ Low to Valid Instruction In		$3t_{CLCL}$ - 45	ns
Input Instruction Hold after $\overline{PSEN}$	0		ns
Input Instruction Float after $\overline{PSEN}$		t_{CLCL} - 10	ns
$\overline{PSEN}$ to Address Valid	t_{CLCL} - 8		ns
Address to Valid Instruction In		$5t_{CLCL}$ - 55	ns
$\overline{PSEN}$ Low to Address Float		10	ns
$\overline{RD}$ Pulse Width	$6t_{CLCL}$ - 100		ns
$\overline{WR}$ Pulse Width	$6t_{CLCL}$ - 100		ns
$\overline{RD}$ Low to Valid Data In		$5t_{CLCL}$ - 90	ns
Data Hold after $\overline{RD}$	0		ns
Data Float after $\overline{RD}$		$2t_{CLCL}$ - 28	ns
ALE Low to Valid Data In		$8t_{CLCL}$ - 150	ns
Address to Valid Data In		$9t_{CLCL}$ - 165	ns
ALE Low to $\overline{RD}$ or $\overline{WR}$ Low	$3t_{CLCL}$ - 50	$3t_{CLCL}$ + 50	ns
Address to $\overline{RD}$ or $\overline{WR}$ Low	$4t_{CLCL}$ - 75		ns
Data Valid to $\overline{WR}$ Transition	t_{CLCL} - 20		ns
Data Valid to $\overline{WR}$ High	$7t_{CLCL}$ - 120		ns
Data Hold after $\overline{WR}$	t_{CLCL} - 20		ns
$\overline{RD}$ Low to Address Float		0	ns
$\overline{RD}$ or $\overline{WR}$ High to ALE High	t_{CLCL} - 20	t_{CLCL} + 25	ns

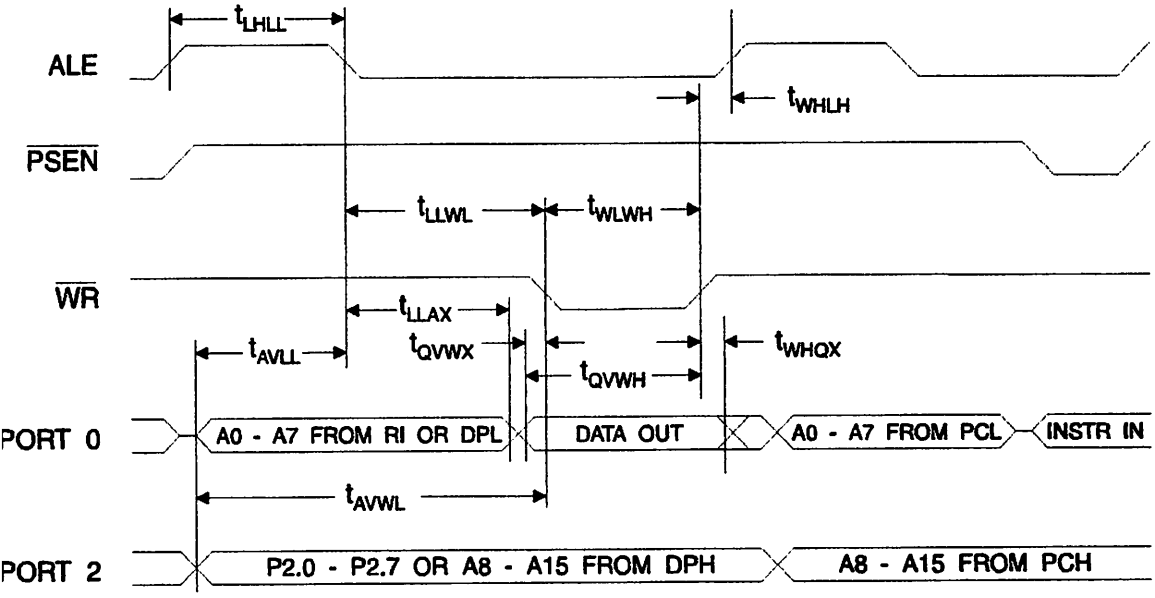
ıal Program Memory Read Cycle



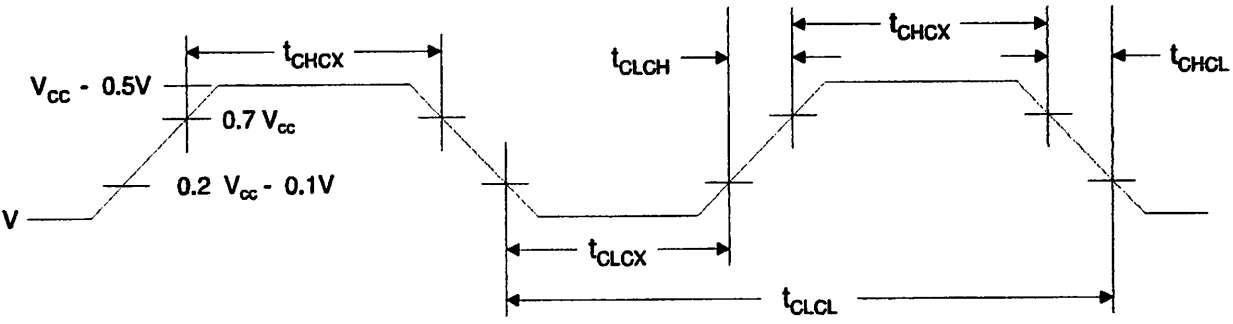
ıal Data Memory Read Cycle



ıal Data Memory Write Cycle



nal Clock Drive Waveforms



nal Clock Drive

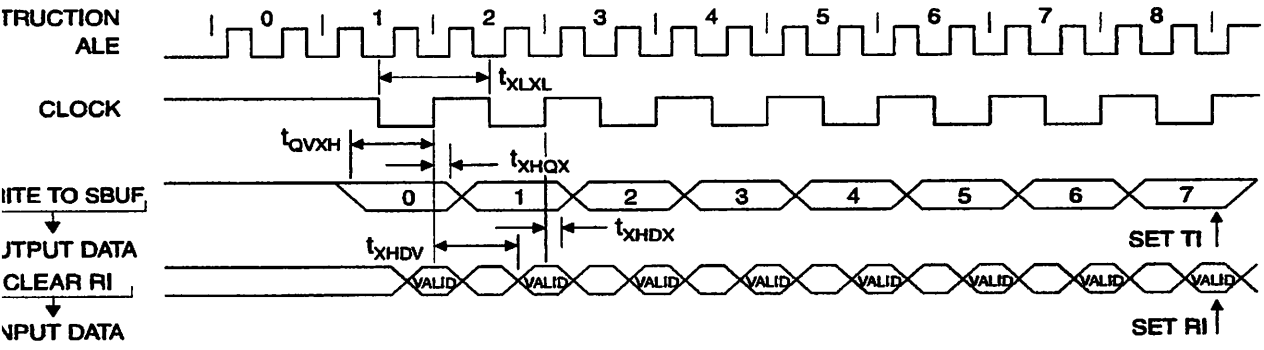
	Parameter	V_{CC} = 4.0V to 6.0V		Units
		Min	Max	
	Oscillator Frequency	0	24	MHz
	Clock Period	41.6		ns
	High Time	15		ns
	Low Time	15		ns
	Rise Time		20	ns
	Fall Time		20	ns

Port Timing: Shift Register Mode Test Conditions

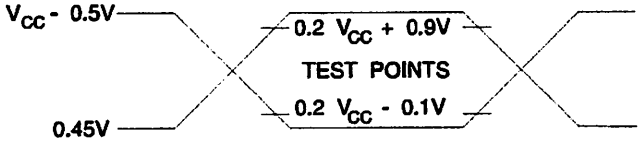
ɛs in this table are valid for V_{CC} = 4.0V to 6V and Load Capacitance = 80 pF.

Parameter	Variable Oscillator		Units
	Min	Max	
Serial Port Clock Cycle Time	$12t_{CLCL}$		µs
Output Data Setup to Clock Rising Edge	$10t_{CLCL}$ - 133		ns
Output Data Hold after Clock Rising Edge	$2t_{CLCL}$ - 117		ns
Input Data Hold after Clock Rising Edge	0		ns
Clock Rising Edge to Input Data Valid		$10t_{CLCL}$ - 133	ns

Register Mode Timing Waveforms

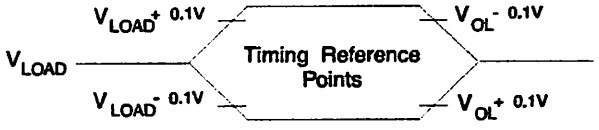


ɛsting Input/Output Waveforms(1)



1. AC Inputs during testing are driven at V_{CC} - 0.5V for a logic 1 and 0.45V for a logic 0. Timing measurements are made at V_{IH} min. for a logic 1 and V_{IL} max. for a logic 0.

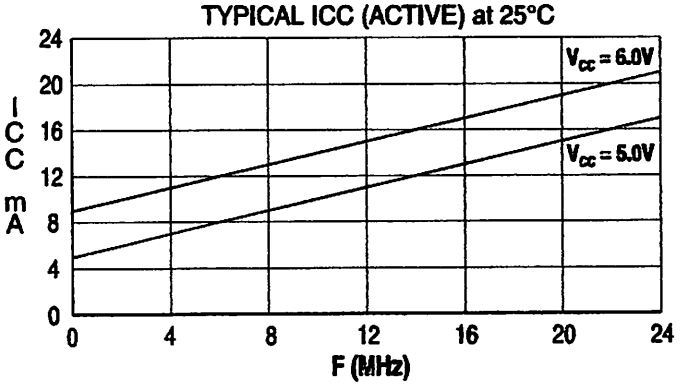
Waveforms(1)



1. For timing purposes, a port pin is no longer floating when a 100 mV change from load voltage occurs. A port pin begins to float when a 100 mV change from the loaded V_{OH}/V_{OL} level occurs.

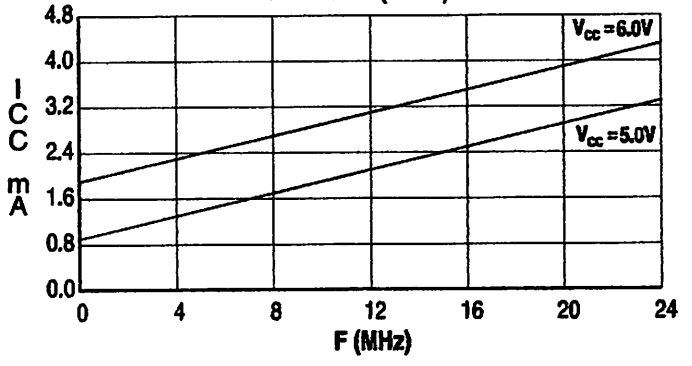
AT89S8252

TYPICAL ICC (ACTIVE) at 25°C



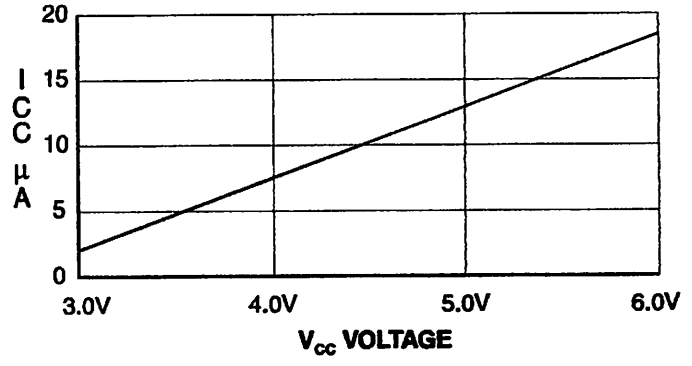
AT89S8252

TYPICAL ICC (IDLE) at 25°C



AT89S8252

TYPICAL ICC vs. VOLTAGE - POWER DOWN (85°C)



Notes: 1. XTAL1 tied to GND for Icc (power-down)
2. Lock bits programmed

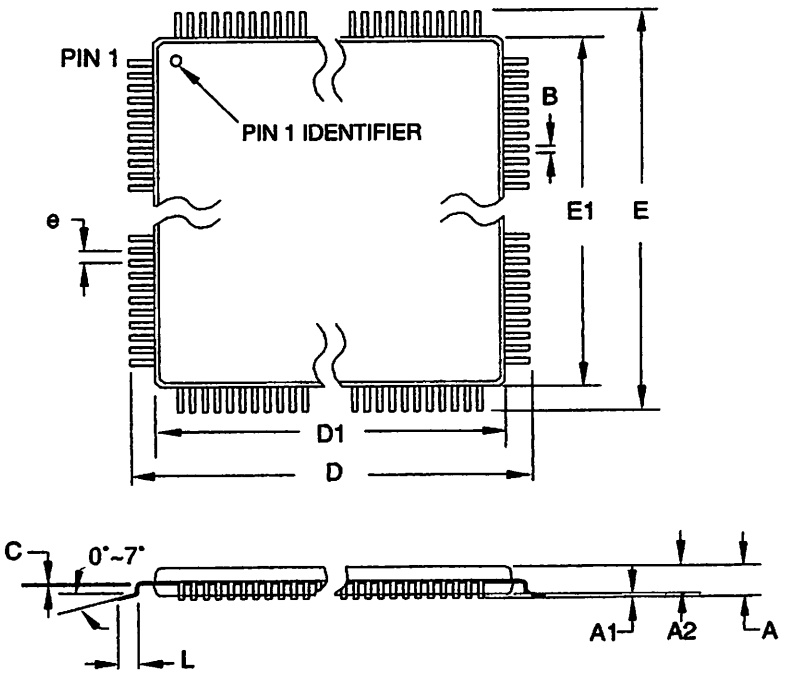
ing Information

	Power Supply	Ordering Code	Package	Operation Range
	4.0V to 6.0V	AT89S8252-24AC AT89S8252-24JC AT89S8252-24PC	44A 44J 40P6	Commercial (0°C to 70°C)
	4.0V to 6.0V	AT89S8252-24AI AT89S8252-24JI AT89S8252-24PI	44A 44J 40P6	Industrial (-40°C to 85°C)

	Package Type
	44-lead, Thin Plastic Gull Wing Quad Flatpack (TQFP)
	44-lead, Plastic J-leaded Chip Carrier (PLCC)
	40-lead, 0.600" Wide, Plastic Dual Inline Package (PDIP)

ging Information

'QFP



COMMON DIMENSIONS
(Unit of Measure = mm)

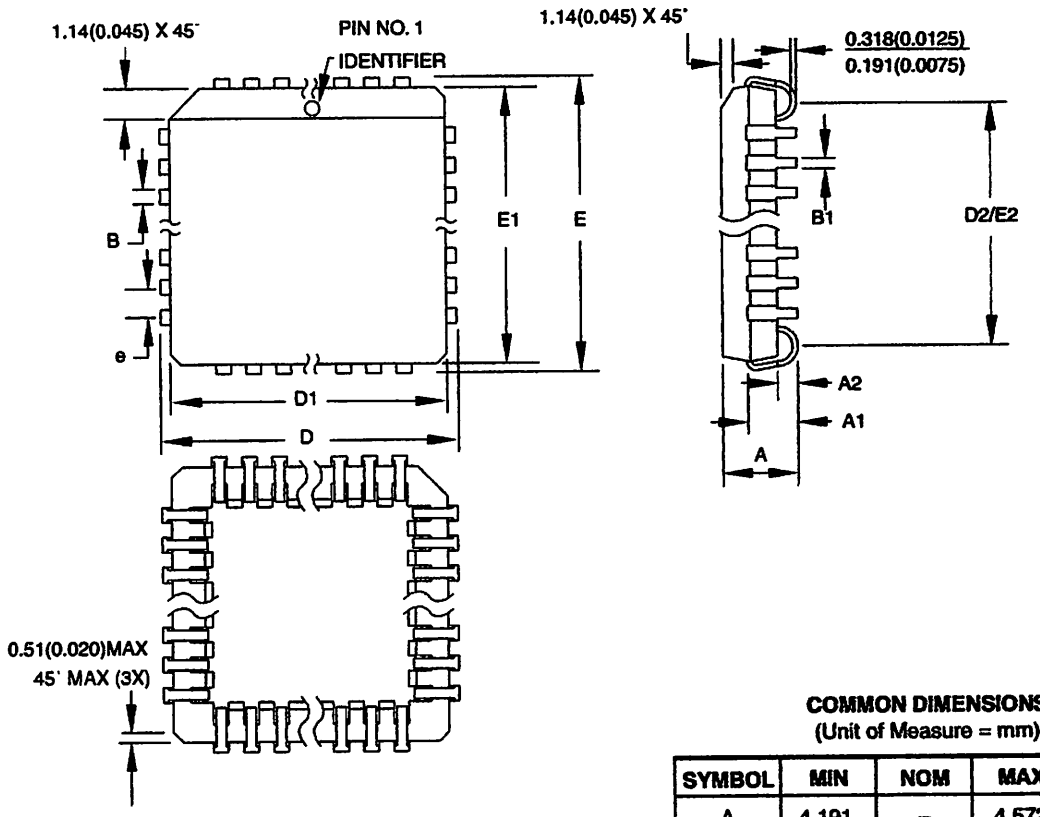
SYMBOL	MIN	NOM	MAX	NOTE
A	–	–	1.20	
A1	0.05	–	0.15	
A2	0.95	1.00	1.05	
D	11.75	12.00	12.25	
D1	9.90	10.00	10.10	Note 2
E	11.75	12.00	12.25	
E1	9.90	10.00	10.10	Note 2
B	0.30	–	0.45	
C	0.09	–	0.20	
L	0.45	–	0.75	
e	0.80 TYP			

es:
1. This package conforms to JEDEC reference MS-026, Variation ACB.
2. Dimensions D1 and E1 do not include mold protrusion. Allowable protrusion is 0.25 mm per side. Dimensions D1 and E1 are maximum plastic body size dimensions including mold mismatch.
3. Lead coplanarity is 0.10 mm maximum.

10/5/2001

	TITLE	DRAWING NO.	REV.
2325 Orchard Parkway San Jose, CA 95131	**44A**, 44-lead, 10 x 10 mm Body Size, 1.0 mm Body Thickness, 0.8 mm Lead Pitch, Thin Profile Plastic Quad Flat Package (TQFP)	44A	B

LCC



COMMON DIMENSIONS
(Unit of Measure = mm)

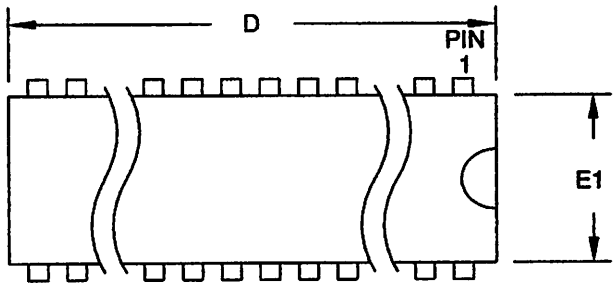
SYMBOL	MIN	NOM	MAX	NOTE
A	4.191	–	4.572	
A1	2.286	–	3.048	
A2	0.508	–	–	
D	17.399	–	17.653	
D1	16.510	–	16.662	Note 2
E	17.399	–	17.653	
E1	16.510	–	16.662	Note 2
D2/E2	14.986	–	16.002	
B	0.660	–	0.813	
B1	0.330	–	0.533	
e	1.270 TYP			

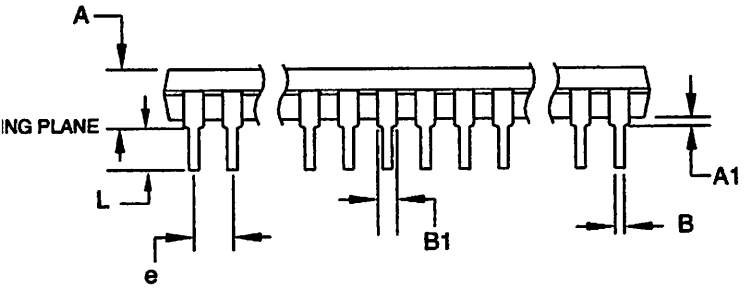
otes:
1. This package conforms to JEDEC reference MS-018, Variation AC.
2. Dimensions D1 and E1 do not include mold protrusion. Allowable protrusion is .010"(0.254 mm) per side. Dimension D1 and E1 include mold mismatch and are measured at the extreme material condition at the upper or lower parting line.
3. Lead coplanarity is 0.004" (0.102 mm) maximum.

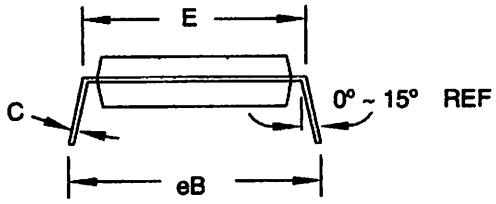
10/04/01

	TITLE	DRAWING NO.	REV.
2325 Orchard Parkway San Jose, CA 95131	**44J**, 44-lead, Plastic J-leaded Chip Carrier (PLCC)	44J	B

PDIP







COMMON DIMENSIONS
(Unit of Measure = mm)

SYMBOL	MIN	NOM	MAX	NOTE
A	–	–	4.826	
A1	0.381	–	–	
D	52.070	–	52.578	Note 2
E	15.240	–	15.875	
E1	13.462	–	13.970	Note 2
B	0.356	–	0.559	
B1	1.041	–	1.651	
L	3.048	–	3.556	
C	0.203	–	0.381	
eB	15.494	–	17.526	
e	2.540 TYP			

tes:
1. This package conforms to JEDEC reference MS-011, Variation AC.
2. Dimensions D and E1 do not include mold Flash or Protrusion. Mold Flash or Protrusion shall not exceed 0.25 mm (0.010").

09/28/01

	TITLE	DRAWING NO.	REV.
2325 Orchard Parkway San Jose, CA 95131	**40P6**, 40-lead (0.600"/15.24 mm Wide) Plastic Dual Inline Package (PDIP)	40P6	B

Corporation

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ose, CA 95131, USA
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l(408) 487-2600

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ı Kong
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)-ku, Tokyo 104-0033
n
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MOTOROLA

LM324, LM324A, LM224, LM2902, LM2902V

uad Low Power perational Amplifiers

The LM324 series are low–cost, quad operational amplifiers with true erential inputs. They have several distinct advantages over standard rational amplifier types in single supply applications. The quad amplifier operate at supply voltages as low as 3.0 V or as high as 32 V with escent currents about one–fifth of those associated with the MC1741 (on er amplifier basis). The common mode input range includes the negative ply, thereby eliminating the necessity for external biasing components in ny applications. The output voltage range also includes the negative wer supply voltage.

- Short Circuited Protected Outputs
- True Differential Input Stage
- Single Supply Operation: 3.0 V to 32 V
- Low Input Bias Currents: 100 nA Maximum (LM324A)
- Four Amplifiers Per Package
- Internally Compensated
- Common Mode Range Extends to Negative Supply
- Industry Standard Pinouts
- ESD Clamps on the Inputs Increase Ruggedness without Affecting Device Operation

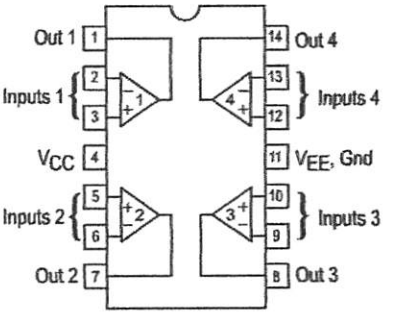
QUAD DIFFERENTIAL INPUT OPERATIONAL AMPLIFIERS

SEMICONDUCTOR TECHNICAL DATA

N SUFFIX
PLASTIC PACKAGE
CASE 646
(LM224, LM324, LM2902 Only)

D SUFFIX
PLASTIC PACKAGE
CASE 751A
(SO–14)

PIN CONNECTIONS



(Top View)

AXIMUM RATINGS (T_A = +25°C, unless otherwise noted.)

Rating	Symbol	LM224 LM324, LM324A	LM2902, LM2902V	Unit
ower Supply Voltages Single Supply Split Supplies	 V_{CC} V_{CC}, V_{EE}	 32 ±16	 26 ±13	Vdc
nput Differential Voltage Range (See Note 1)	V_{IDR}	±32	±26	Vdc
nput Common Mode Voltage Range	V_{ICR}	–0.3 to 32	–0.3 to 26	Vdc
Output Short Circuit Duration	t_{SC}	Continuous		
unction Temperature	T_J	150		°C
Storage Temperature Range	T_{stg}	–65 to +150		°C
Operating Ambient Temperature Range	T_A	–25 to +85 0 to +70	–40 to +105 –40 to +125	°C

OTE: 1. Split Power Supplies.

ORDERING INFORMATION

Device	Operating Temperature Range	Package
LM2902D	T_A = –40° to +105°C	SO–14
LM2902N		Plastic DIP
LM2902VD	T_A = –40° to +125°C	SO–14
LM2902VN		Plastic DIP
LM224D	T_A = –25° to +85°C	SO–14
LM224N		Plastic DIP
LM324AD	T_A = 0° to +70°C	SO–14
LM324AN		Plastic DIP
LM324D		SO–14
LM324N		Plastic DIP

ECTRICAL CHARACTERISTICS (V_{CC} = 5.0 V, V_{EE} = Gnd, T_A = 25°C, unless otherwise noted.)

Characteristics	Symbol	LM224			LM324A			LM324			LM2902			LM2902V			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
ıut Offset Voltage V_{CC} = 5.0 V to 30 V (26 V for LM2902, V), V_{ICR} = 0 V to V_{CC} −1.7 V, V_O = 1.4 V, R_S = 0 Ω	V_{IO}																mV
T_A = 25°C		–	2.0	5.0	–	2.0	3.0	–	2.0	7.0	–	2.0	7.0	–	2.0	7.0	
T_A = T_{high}(1)		–	–	7.0	–	–	5.0	–	–	9.0	–	–	10	–	–	13	
T_A = T_{low}(1)		–	–	7.0	–	–	5.0	–	–	9.0	–	–	10	–	–	10	
ɛrage Temperature Coefficient of Input Offset Voltage T_A = T_{high} to T_{low}(1)	$\Delta V_{IO}/\Delta T$	–	7.0	–	–	7.0	30	–	7.0	–	–	7.0	–	–	7.0	–	μV/°C
ɒut Offset Current	I_{IO}	–	3.0	30	–	5.0	30	–	5.0	50	–	5.0	50	–	5.0	50	nA
T_A = T_{high} to T_{low}(1)		–	–	100	–	–	75	–	–	150	–	–	200	–	–	200	
ɛrage Temperature Coefficient of Input Offset Current T_A = T_{high} to T_{low}(1)	$\Delta I_{IO}/\Delta T$	–	10	–	–	10	300	–	10	–	–	10	–	–	10	–	pA/°C
ɒut Bias Current	I_{IB}	–	−90	−150	–	−45	−100	–	−90	−250	–	−90	−250	–	−90	−250	nA
T_A = T_{high} to T_{low}(1)		–	–	−300	–	–	−200	–	–	−500	–	–	−500	–	–	−500	
ɒut Common Mode Voltage Range(2)	V_{ICR}																V
CC = 30 V (26 V for LM2902, V)		0	–	28.3	0	–	28.3	0	–	28.3	0	–	24.3	0	–	24.3	
CC = 30 V (26 V for LM2902, V), T_A = T_{high} to T_{low}		0	–	28	0	–	28	0	–	28	0	–	24	0	–	24	
ifferential Input Voltage Range	V_{IDR}	–	–	V_{CC}	–	–	V_{CC}	–	–	V_{CC}	–	–	V_{CC}	–	–	V_{CC}	V
ırge Signal Open Loop Voltage Gain	A_{VOL}																V/mV
R_L = 2.0 kΩ, V_{CC} = 15 V, for Large V_O Swing, T_A = T_{high} to T_{low}(1)		50 25	100 –	– –	25 15	100 –	– –	25 15	100 –	– –	25 15	100 –	– –	25 15	100 –	– –	
hannel Separation 10 kHz ≤ f ≤ 20 kHz, nput Referenced	CS	–	−120	–	–	−120	–	–	−120	–	–	−120	–	–	−120	–	dB
ɔmmon Mode Rejection, R_S ≤ 10 kΩ	CMR	70	85	–	65	70	–	65	70	–	50	70	–	50	70	–	dB
ɔwer Supply Rejection	PSR	65	100	–	65	100	–	65	100	–	50	100	–	50	100	–	dB
utput Voltage−High Limit (T_A = T_{high} to T_{low})(1)	V_{OH}																V
V_{CC} = 5.0 V, R_L = 2.0 kΩ, T_A = 25°C		3.3	3.5	–	3.3	3.5	–	3.3	3.5	–	3.3	3.5	–	3.3	3.5	–	
'CC = 30 V (26 V for LM2902, V), R_L = 2.0 kΩ		26	–	–	26	–	–	26	–	–	22	–	–	22	–	–	
'CC = 30 V (26 V for LM2902, V), R_L = 10 kΩ		27	28	–	27	28	–	27	28	–	23	24	–	23	24	–	

)TES: 1. T_{low} = −25°C for LM224 T_{high} = +85°C for LM224
= 0°C for LM324, A = +70°C for LM324, A
= −40°C for LM2902 = +105°C for LM2902
= −40°C for LM2902V = +125°C for LM2902V

2. The input common mode voltage or either input signal voltage should not be allowed to go negative by more than 0.3 V. The upper end of the common mode voltage range is V_{CC} −1.7 V.

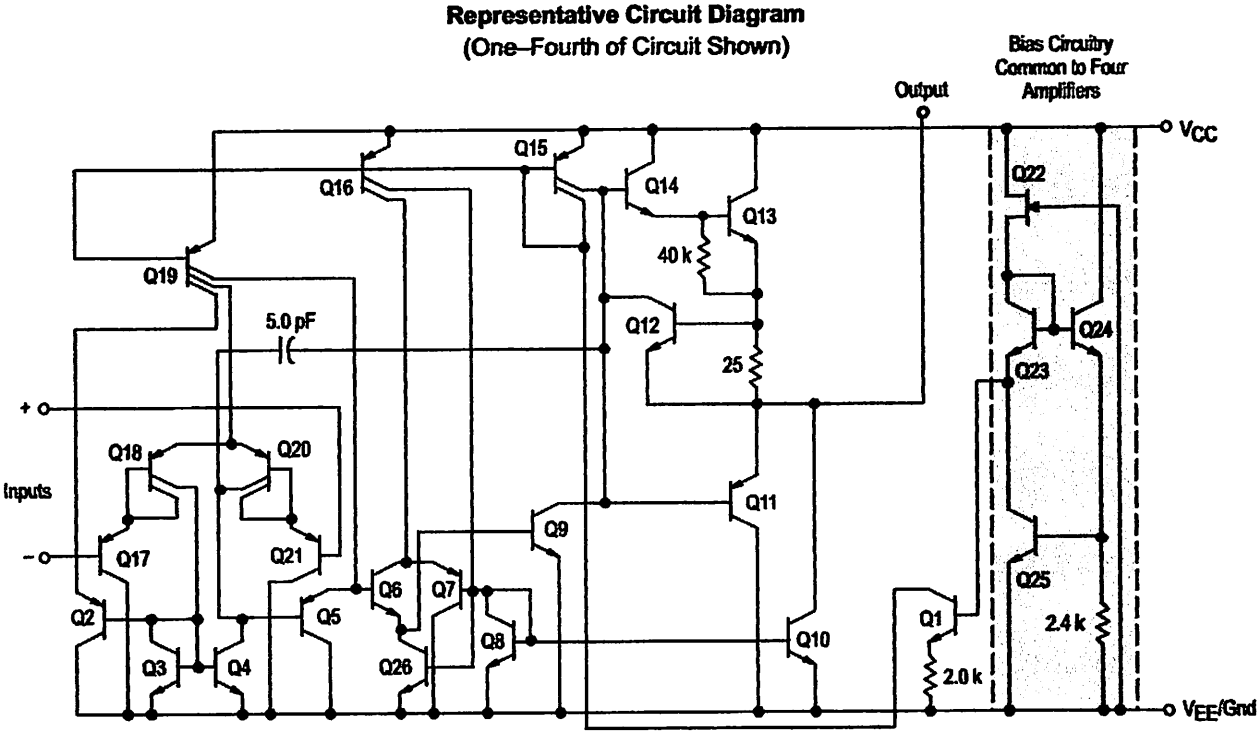
ECTRICAL CHARACTERISTICS (V_{CC} = 5.0 V, V_{EE} = Gnd, T_A = 25°C, unless otherwise noted.)

Characteristics	Symbol	LM224			LM324A			LM324			LM2902			LM2902V			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
itput Voltage – Low it, V_{CC} = 5.0 V, R_L 0 kΩ, T_A = T_{high} to low(1)	V_{OL}	–	5.0	20	–	5.0	20	–	5.0	20	–	5.0	100	–	5.0	100	mV
itput Source Current ID = +1.0 V, V_{CC} = 5 V)	I_{O+}																mA
T_A = 25°C		20	40	–	20	40	–	20	40	–	20	40	–	20	40	–	
T_A = T_{high} to T_{low}(1)		10	20	–	10	20	–	10	20	–	10	20	–	10	20	–	
itput Sink Current	I_{O-}																mA
/ID = –1.0 V, V_{CC} = 15 V) T_A = 25°C		10	20	–	10	20	–	10	20	–	10	20	–	10	20	–	
T_A = T_{high} to T_{low}(1)		5.0	8.0	–	5.0	8.0	–	5.0	8.0	–	5.0	8.0	–	5.0	8.0	–	
(V_{ID} = –1.0 V, V_O = 200 mV, T_A = 25°C)		12	50	–	12	50	–	12	50	–	–	–	–	–	–	–	µA
utput Short Circuit to Ground(3)	I_{SC}	–	40	60	–	40	60	–	40	60	–	40	60	–	40	60	mA
ower Supply Current A = T_{high} to T_{low})(1)	I_{CC}																mA
CC = 30 V (26 V for LM2902, V), V_O = 0 V, R_L = ∞		–	–	3.0	–	1.4	3.0	–	–	3.0	–	–	3.0	–	–	3.0	
V_{CC} = 5.0 V, V_O = 0 V, R_L = ∞		–	–	1.2	–	0.7	1.2	–	–	1.2	–	–	1.2	–	–	1.2	

TES: 1. T_{low} = –25°C for LM224 = 0°C for LM324, A = –40°C for LM2902 = –40°C for LM2902V
T_{high} = +85°C for LM224 = +70°C for LM324, A = +105°C for LM2902 = +125°C for LM2902V

2. The input common mode voltage or either input signal voltage should not be allowed to go negative by more than 0.3 V. The upper end of the common mode voltage range is V_{CC} –1.7 V.

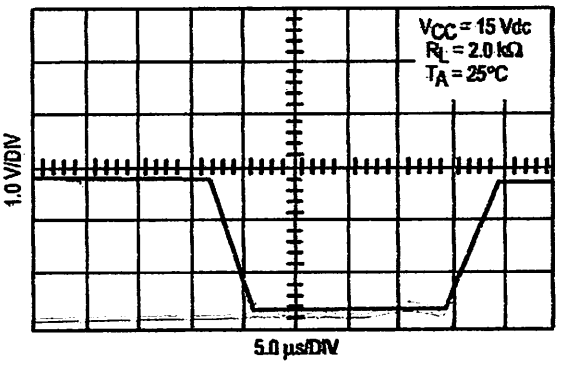
Representative Circuit Diagram
(One–Fourth of Circuit Shown)



CIRCUIT DESCRIPTION

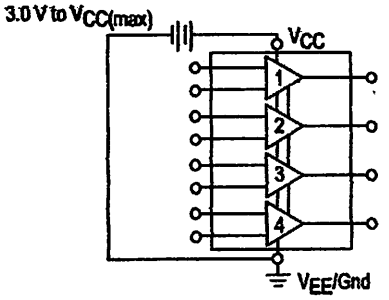
he LM324 series is made using four internally ıpensated, two–stage operational amplifiers. The first ıe of each consists of differential input devices Q20 and ı with input buffer transistors Q21 and Q17 and the ırential to single ended converter Q3 and Q4. The first ıe performs not only the first stage gain function but also orms the level shifting and transconductance reduction ctions. By reducing the transconductance, a smaller ıpensation capacitor (only 5.0 pF) can be employed, thus ing chip area. The transconductance reduction is omplished by splitting the collectors of Q20 and Q18. ther feature of this input stage is that the input common le range can include the negative supply or ground, in gle supply operation, without saturating either the input ices or the differential to single–ended converter. The ond stage consists of a standard current source load olifier stage.

Large Signal Voltage Follower Response



Each amplifier is biased from an internal–voltage regulator which has a low temperature coefficient thus giving each amplifier good temperature characteristics as well as excellent power supply rejection.

Single Supply



Split Supplies

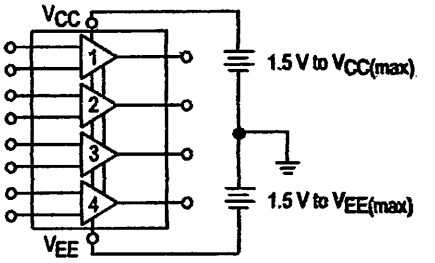


Figure 1. Input Voltage Range

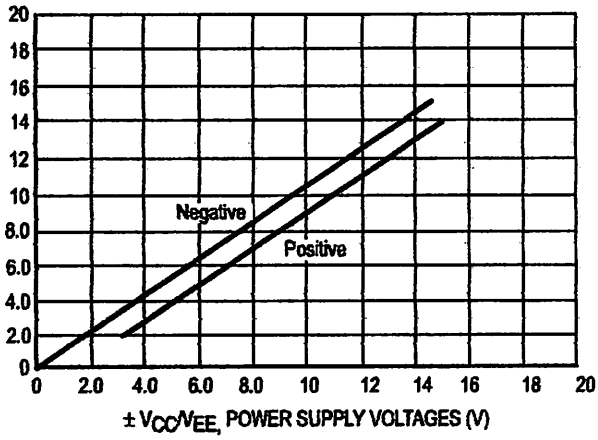


Figure 2. Open Loop Frequency

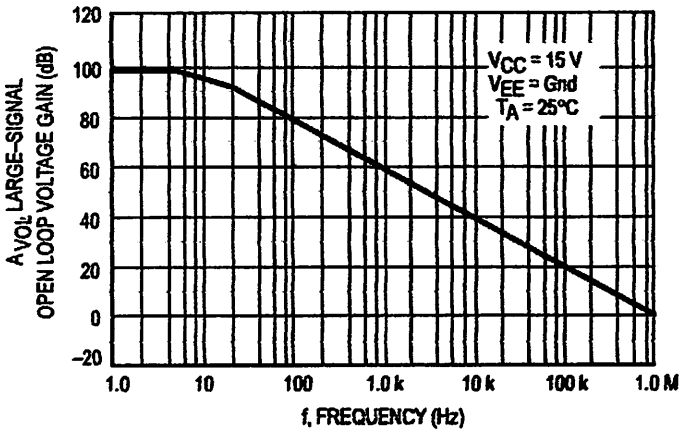


Figure 3. Large–Signal Frequency Response

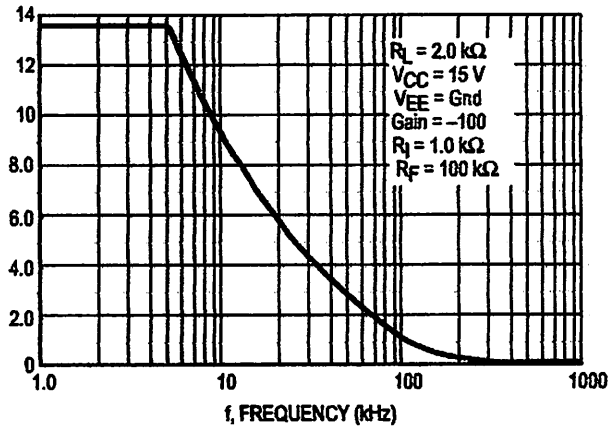


Figure 4. Small–Signal Voltage Follower Pulse Response (Noninverting)

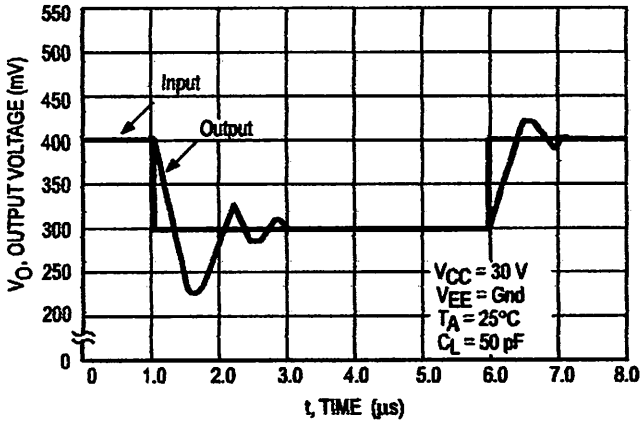


Figure 5. Power Supply Current versus Power Supply Voltage

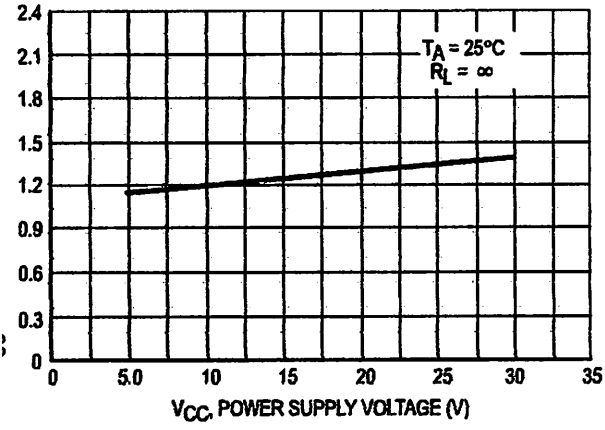


Figure 6. Input Bias Current versus Power Supply Voltage

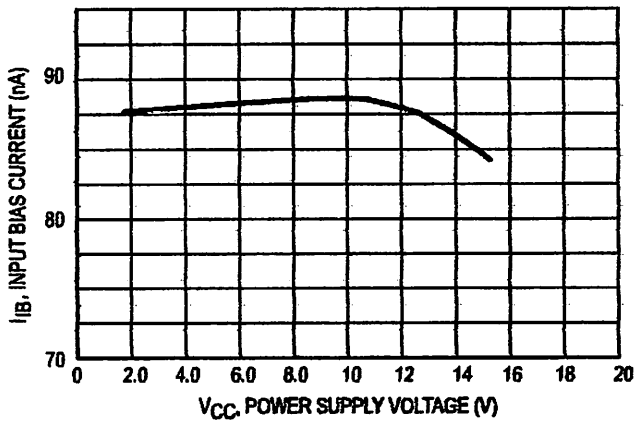
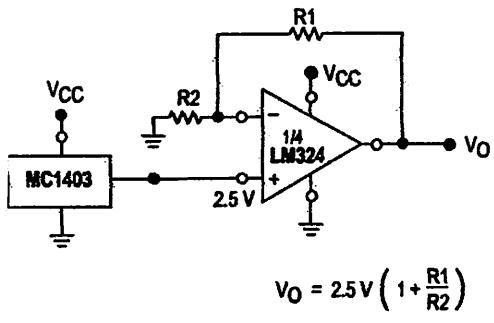


Figure 7. Voltage Reference



$$V_O = 2.5\,V\left(1+\frac{R1}{R2}\right)$$

Figure 8. Wien Bridge Oscillator

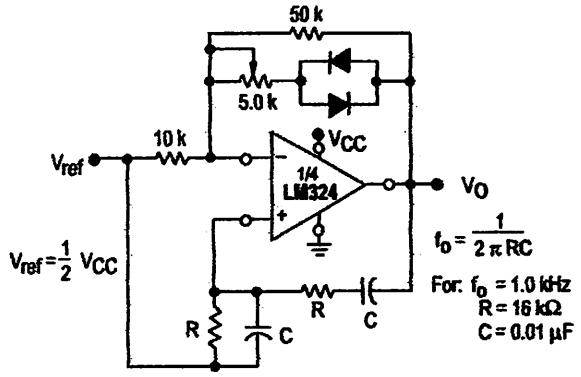
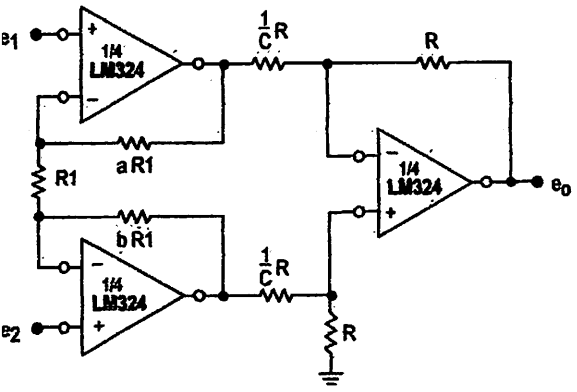
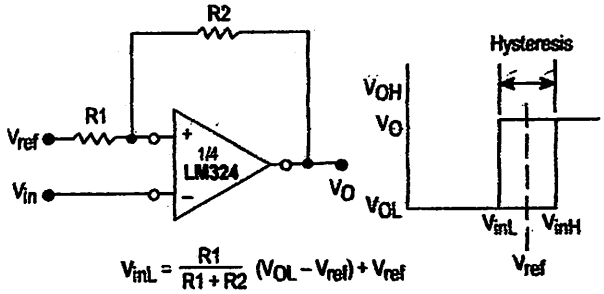


Figure 9. High Impedance Differential Amplifier



$$e_o = C(1+a+b)(e_2-e_1)$$

Figure 10. Comparator with Hysteresis



$$V_{inL} = \frac{R1}{R1+R2}(V_{OL}-V_{ref})+V_{ref}$$

$$V_{inH} = \frac{R1}{R1+R2}(V_{OH}-V_{ref})+V_{ref}$$

$$H = \frac{R1}{R1+R2}(V_{OH}-V_{OL})$$

Figure 11. Bi-Quad Filter

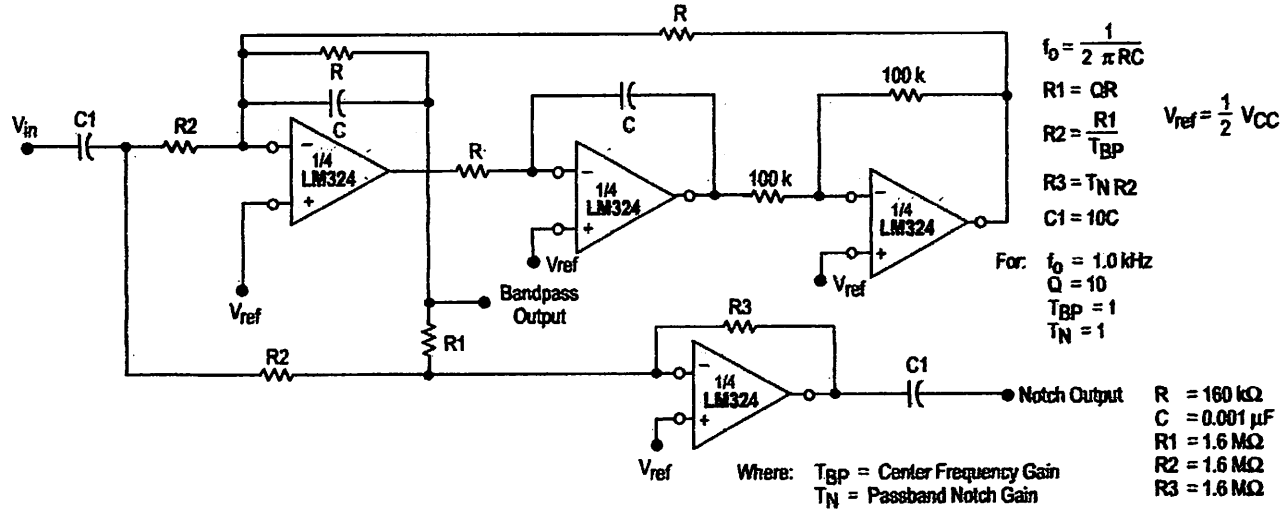
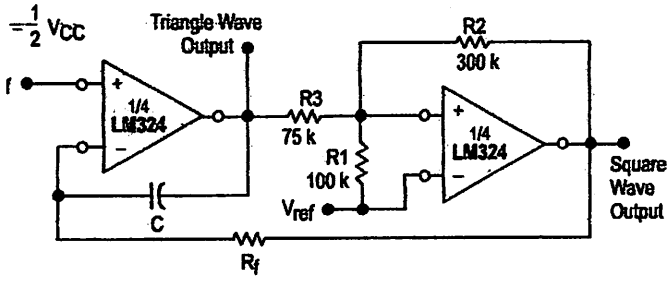
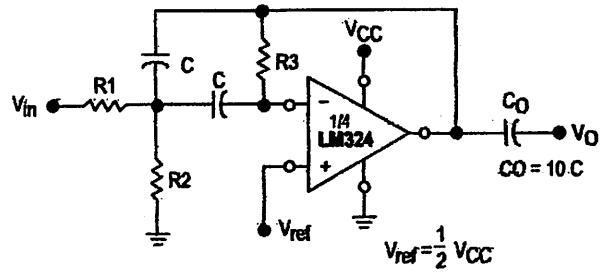


Figure 12. Function Generator



$$f = \frac{R1 + R_C}{4\,C R_f R1} \quad \text{if } R3 = \frac{R2\,R1}{R2 + R1}$$

Figure 13. Multiple Feedback Bandpass Filter



Given: f_0 = center frequency
$A(f_0)$ = gain at center frequency

Choose value f_0, C

Then: $R3 = \frac{Q}{\pi f_0 C}$

$$R1 = \frac{R3}{2\,A(f_0)}$$

$$R2 = \frac{R1\,R3}{4Q^2\,R1 - R3}$$

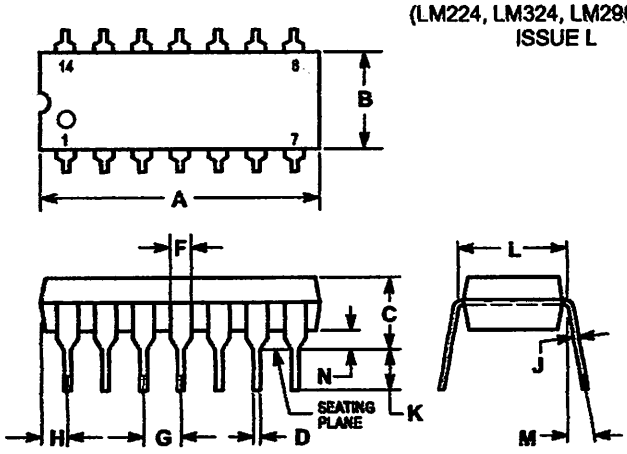
For less than 10% error from operational amplifier, $\frac{Q_0 f_0}{BW} < 0.1$

where f_0 and BW are expressed in Hz.

If source impedance varies, filter may be preceded with voltage follower buffer to stabilize filter parameters.

OUTLINE DIMENSIONS

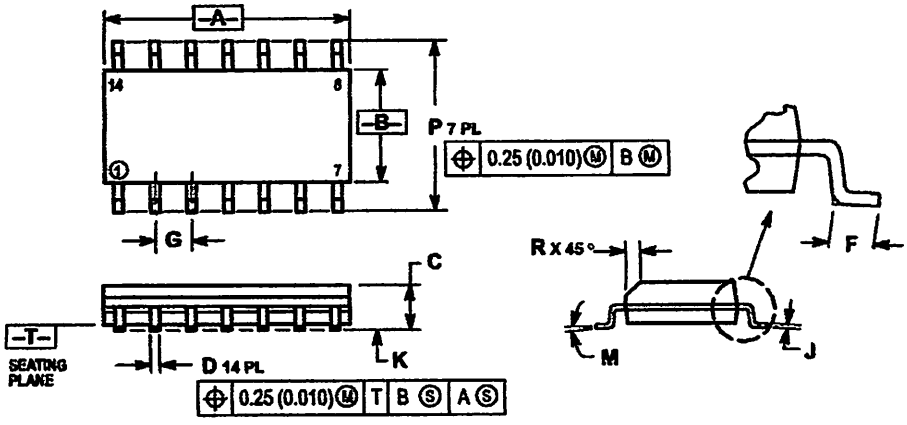
N SUFFIX
PLASTIC PACKAGE
CASE 646–06
(LM224, LM324, LM2902 Only)
ISSUE L



NOTES:
1. LEADS WITHIN 0.13 (0.005) RADIUS OF TRUE POSITION AT SEATING PLANE AT MAXIMUM MATERIAL CONDITION.
2. DIMENSION L TO CENTER OF LEADS WHEN FORMED PARALLEL.
3. DIMENSION B DOES NOT INCLUDE MOLD FLASH.
4. ROUNDED CORNERS OPTIONAL.

	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	0.715	0.770	18.16	19.56
B	0.240	0.260	6.10	6.60
C	0.145	0.185	3.69	4.69
D	0.015	0.021	0.38	0.53
F	0.040	0.070	1.02	1.78
G	0.100 BSC		2.54 BSC	
H	0.052	0.095	1.32	2.41
J	0.008	0.015	0.20	0.38
K	0.115	0.135	2.92	3.43
L	0.300 BSC		7.62 BSC	
M	0°	10°	0°	10°
N	0.015	0.039	0.39	1.01

D SUFFIX
PLASTIC PACKAGE
CASE 751A–03
(SO–14)
ISSUE F



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSIONS A AND B DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
5. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127 (0.005) TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	8.55	8.75	0.337	0.344
B	3.80	4.00	0.150	0.157
C	1.35	1.75	0.054	0.068
D	0.35	0.49	0.014	0.019
F	0.40	1.25	0.016	0.049
G	1.27 BSC		0.050 BSC	
J	0.19	0.25	0.008	0.009
K	0.10	0.25	0.004	0.009
M	0°	7°	0°	7°
P	5.80	6.20	0.228	0.244
R	0.25	0.50	0.010	0.019

low to reach us:
SA/EUROPE/Locations Not Listed: Motorola Literature Distribution;
O. Box 20912; Phoenix, Arizona 85036. 1–800–441–2447 or 602–303–5454

AX: RMFAX0@email.sps.mot.com – TOUCHTONE 602–244–6609
ITERNET: http://Design–NET.com

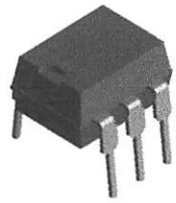
JAPAN: Nippon Motorola Ltd.; Tatsumi–SPD–JLDC, 6F Seibu–Butsuryu–Center, 3–14–2 Tatsumi Koto–Ku, Tokyo 135, Japan. 03–81–3521–8315

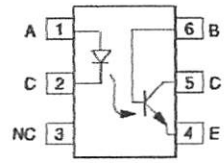
ASIA/PACIFIC: Motorola Semiconductors H.K. Ltd.; 8B Tai Ping Industrial Park, 51 Ting Kok Road, Tai Po, N.T., Hong Kong. 852–26629298

Optocoupler, Phototransistor Output, With Base Connection

Features

- Isolation Test Voltage 5300 V_{RMS}
- Interfaces with Common Logic Families
- Input-output Coupling Capacitance < 0.5 pF
- Industry Standard Dual-in-line 6-pin Package





i179004

Agency Approvals

- UL File #E52744 System Code H or J
- DIN EN 60747-5-2(VDE0884)
  DIN EN 60747-5-5 pending
  Available with Option 1

Applications

AC Mains Detection

Reed relay driving

Switch Mode Power Supply Feedback

Telephone Ring Detection

Logic Ground Isolation

Logic Coupling with High Frequency Noise Rejection

Description

The 4N25 family is an Industry Standard Single Channel Phototransistor Coupler.This family includes the 4N25/ 4N26/ 4N27/ 4N28. Each optocoupler consists of gallium arsenide infrared LED and a silicon NPN phototransistor.

These couplers are Underwriters Laboratories (UL) listed to comply with a 5300 V_{RMS} isolation test voltage. This isolation performance is accomplished through special Vishay manufacturing process.

Compliance to DIN EN 60747-5-2(VDE0884)/ DIN EN 60747-5-5 pending partial discharge isolation specification is available by ordering option1.

These isolation processes and the Vishay ISO9001 quality program results in the highest isolation performance available for a commercial plastic phototransistor optocoupler.

The devices are also available in lead formed configuration suitable for surface mounting and are available either on tape and reel, or in standard tube shipping containers.

Note:
For additional design information see Application Note 45 Normalized Curves

Order Information

Part	Remarks
4N25	CTR > 20 %, DIP-6
4N26	CTR > 20 %, DIP-6
4N27	CTR > 10 %, DIP-6
4N28	CTR > 10 %, DIP-6
4N25-Xxx6	CTR > 20 %, DIP-6 400 mil (option 6)
4N25-Xxx7	CTR > 20 %, SMD-6 (option 7)
4N25-Xxx9	CTR > 20 %, SMD-6 (option 9)
4N26-Xxx6	CTR > 20 %, DIP-6 400 mil (option 6)
4N26-Xxx7	CTR > 20 %, SMD-6 (option 7)
4N26-Xxx9	CTR > 20 %, SMD-6 (option 9)
4N27-Xxx7	CTR > 10 %, SMD-6 (option 7)
4N27-Xxx9	CTR > 10 %, SMD-6 (option 9)
4N28-Xxx9	CTR > 10 %, SMD-6 (option 9)

For additional option information and package dimensions see Option Section.

olute Maximum Ratings

25 °C, unless otherwise specified

ıs in excess of the absolute Maximum Ratings can cause permanent damage to the device. Functional operation of the device is ılied at these or any other conditions in excess of those given in the operational sections of this document. Exposure to absolute ım Rating for extended periods of the time can adversely affect reliability.

ıt

Parameter	Test condition	Symbol	Value	Unit
se voltage		V_R	6.0	V
ırd current		I_F	60	mA
) current	t < 10 µs	I_{FSM}	2.5	A
r dissipation		P_{diss}	100	mW

put

Parameter	Test condition	Symbol	Value	Unit
ctor-emitter breakdown voltage		V_{CEO}	70	V
er-base breakdown voltage		V_{EBO}	7.0	V
ctor current		I_C	50	mA
ctor current	t < 1.0 ms	I_C	100	mA
ır dissipation		P_{diss}	150	mW

ıpler

Parameter	Test condition	Symbol	Value	Unit
ion test voltage		V_{ISO}	5300	V_{RMS}
page			≥ 7.0	mm
ance			≥ 7.0	mm
ion thickness between er and detector			≥ 0.4	mm
parative tracking index	DIN IEC 112/VDE0303, part 1		175	
ion resistance	V_{IO} = 500 V, T_{amb} = 25 °C	R_{IO}	10^{12}	Ω
	V_{IO} = 500 V, T_{amb} = 100 °C	R_{IO}	10^{11}	Ω
ge temperature		T_{stg}	- 55 to + 150	°C
ating temperature		T_{amb}	- 55 to + 100	°C
ion temperature		T_j	100	°C
ering temperature	max.10 s, dip soldering: distance to seating plane ≥ 1.5 mm	T_{sld}	260	°C

Electrical Characteristics

T_{amb} = 25 °C, unless otherwise specified
Minimum and maximum values are testing requirements. Typical values are characteristics of the device and are the result of engineering evaluation. Typical values are for information only and are not part of the testing requirements.

Input

Parameter	Test condition	Symbol	Min	Typ.	Max	Unit
Forward voltage[1)]	I_F = 50 mA	V_F		1.3	1.5	V
Reverse current[1)]	V_R = 3.0 V	I_R		0.1	100	µA
Capacitance	V_R = 0 V	C_O		25		pF

[1)] Indicates JEDEC registered values

Output

Parameter	Test condition	Part	Symbol	Min	Typ.	Max	Unit
Collector-base breakdown voltage[1)]	I_C = 100 µA		BV_{CBO}	70			V
Collector-emitter breakdown voltage[1)]	I_C = 1.0 mA		BV_{CEO}	30			V
Emitter-collector breakdown voltage[1)]	I_E = 100 µA		BV_{ECO}	7.0			V
I_{CEO}(dark)[1)]	V_{CE} = 10 V, (base open)	4N25			5.0	50	nA
		4N26			5.0	50	nA
		4N27			5.0	50	nA
		4N28			10	100	nA
I_{CBO}(dark)[1)]	V_{CB} = 10 V, (emitter open)				2.0	20	nA
Collector-emitter capacitance	V_{CE} = 0		C_{CE}		6.0		pF

[1)] Indicates JEDEC registered values

Coupler

Parameter	Test condition	Part	Symbol	Min	Typ.	Max	Unit
Isolation voltage[1)]	Peak, 60 Hz	4N25	V_{IO}	2500			V
		4N26	V_{IO}	1500			V
		4N27	V_{IO}	1500			V
		4N28	V_{IO}	500			V
Saturation voltage, collector-emitter	I_{CE} = 2.0 mA, I_F = 50 mA		$V_{CE(sat)}$			0.5	V
Resistance, input output[1)]	V_{IO} = 500 V		R_{IO}	100			GΩ
Capacitance (input-output)	f = 1.0 MHz		C_{IO}		0.5		pF

[1)] Indicates JEDEC registered values

Current Transfer Ratio

Parameter	Test condition	Part	Symbol	Min	Typ.	Max	Unit
DC Current Transfer Ratio[1)]	V_{CE} = 10 V, I_F = 10 mA	4N25	CTR_{DC}	20	50		%
		4N26	CTR_{DC}	20	50		%
		4N27	CTR_{DC}	10	30		%
		4N28	CTR_{DC}	10	30		%

[1)] Indicates JEDEC registered value

ching Characteristics

arameter	Test condition	Symbol	Min	Typ.	Max	Unit
nd fall times	V_{CE} = 10 V, I_F = 10 mA, R_L = 100 Ω	t_r, t_f		2.0		µs

cal Characteristics (T_{amb} = 25 °C unless otherwise specified)

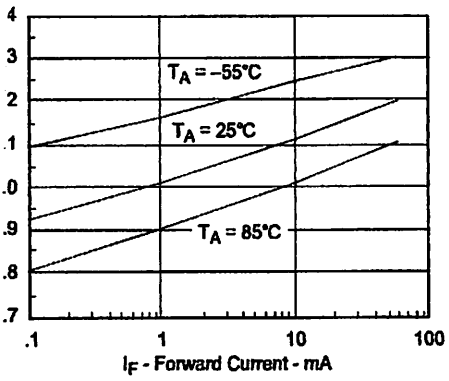
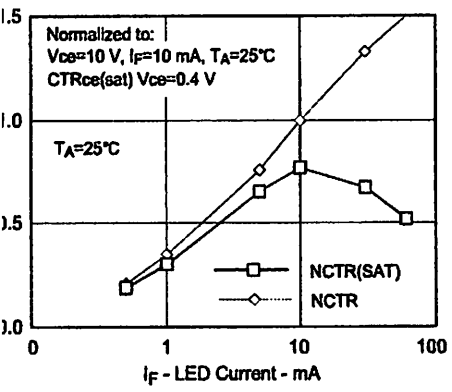


Figure 1. Forward Voltage vs. Forward Current



e 2. Normalized Non-saturated and Saturated CTR vs. LED Current

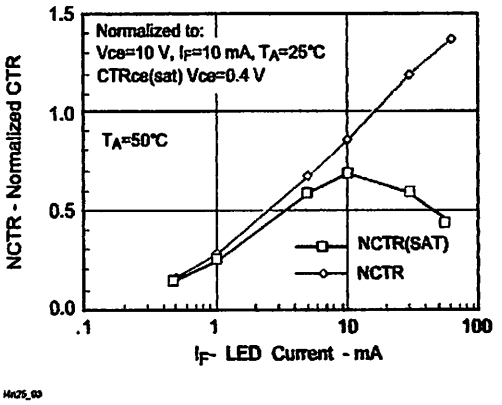


Figure 3. Normalized Non-saturated and Saturated CTR vs. LED Current

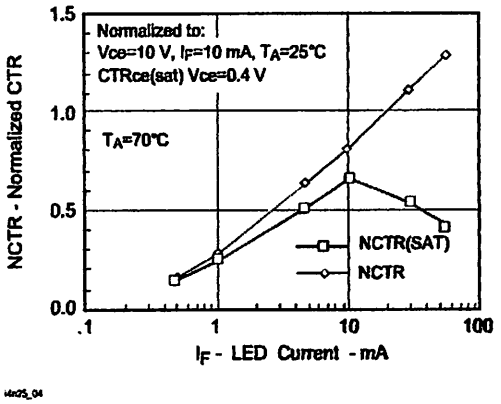


Figure 4. Normalized Non-saturated and saturated CTR vs. LED Current

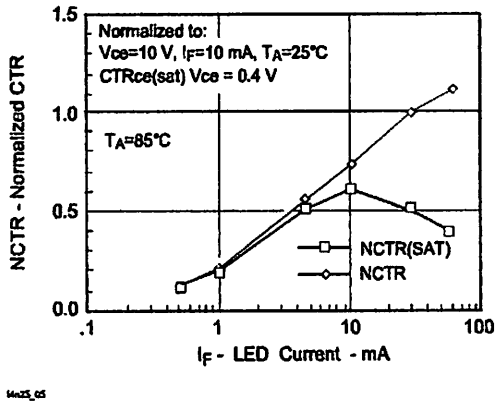


Figure 5. Normalized Non-saturated and saturated CTR vs. LED Current

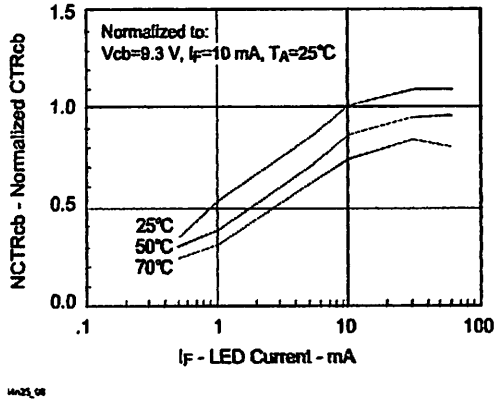


Figure 8. Normalized CTRcb vs. LED Current and Temp.

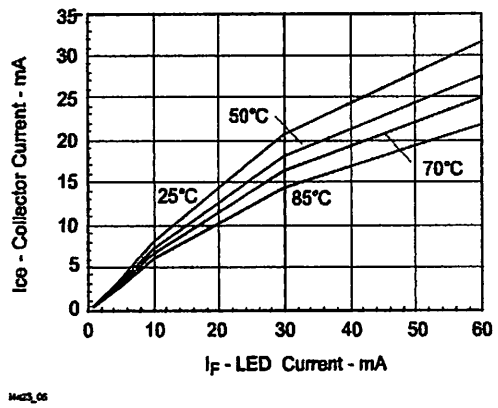


Figure 6. Collector-Emitter Current vs. Temperature and LED Current

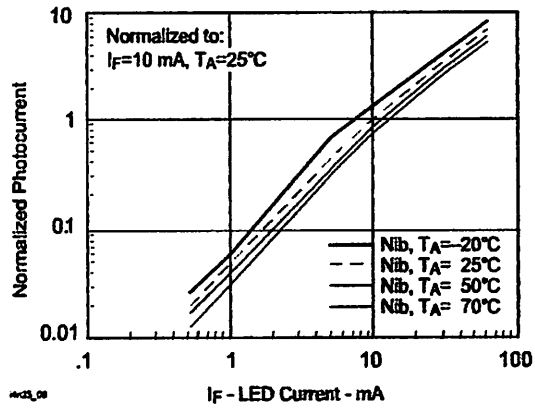


Figure 9. Normalized Photocurrent vs. I_F and Temp.

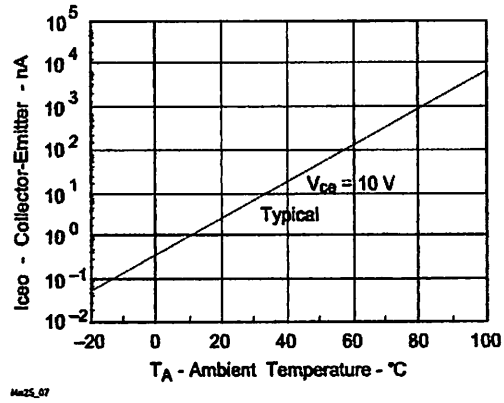


Figure 7. Collector-Emitter Leakage Current vs.Temp.

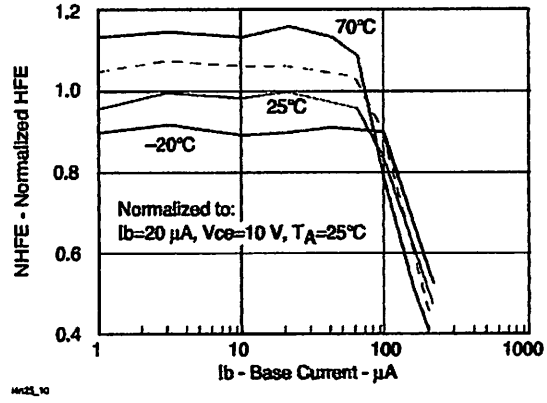
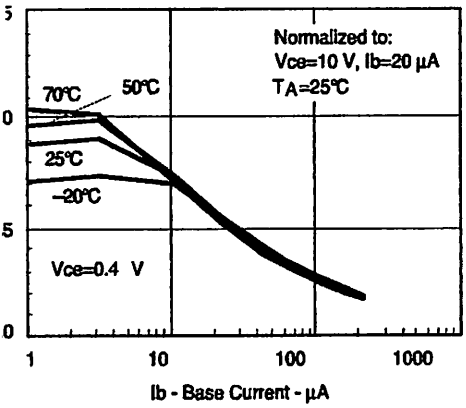


Figure 10. Normalized Non-saturated HFE vs. Base Current and Temperature



igure 11. Normalized HFE vs. Base Current and Temp.

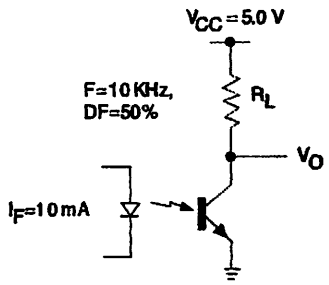
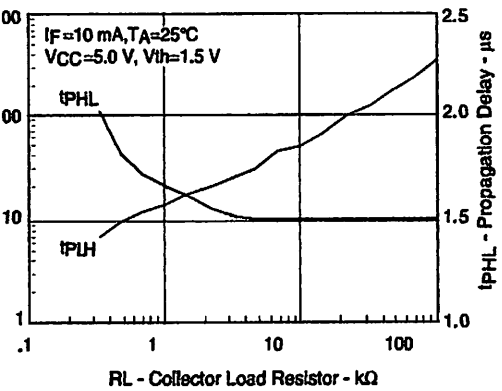


Figure 14. Switching Schematic



igure 12. Propagation Delay vs. Collector Load Resistor

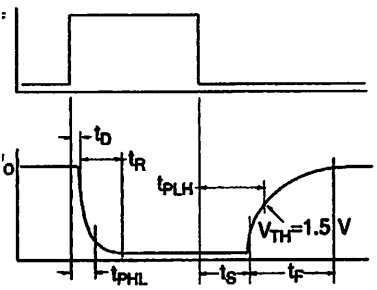
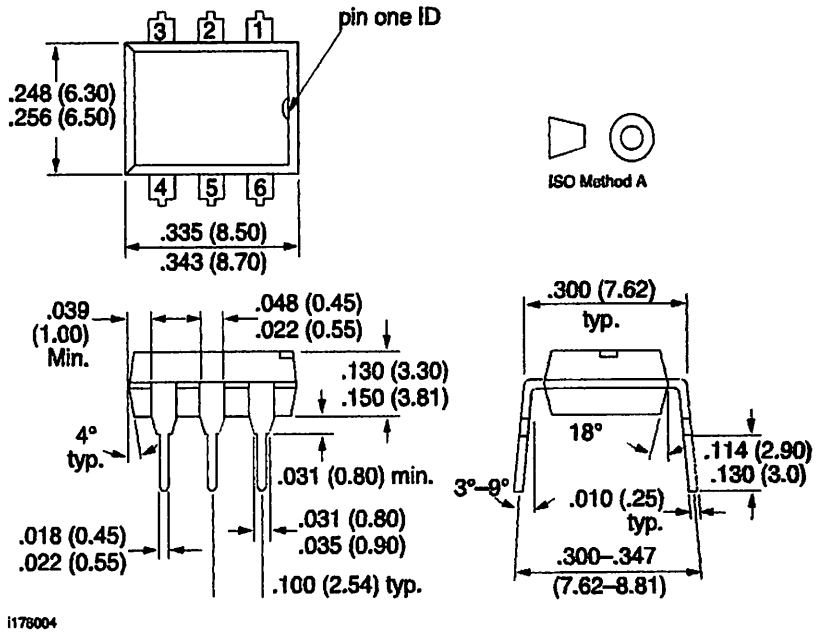
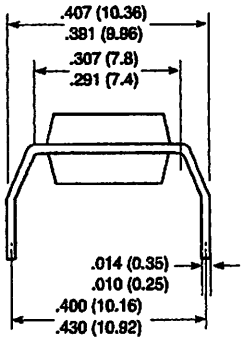


Figure 13. Switching Timing

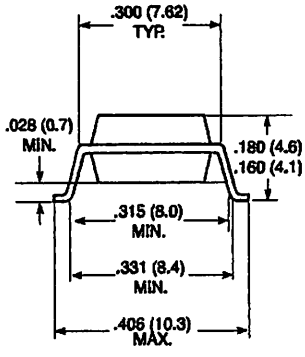
Package Dimensions in Inches (mm)



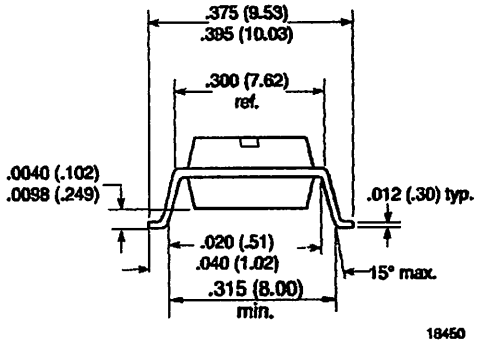
Option 6



Option 7



Option 9



ne Depleting Substances Policy Statement

ıe policy of **Vishay Semiconductor GmbH** to

eet all present and future national and international statutory requirements.

egularly and continuously improve the performance of our products, processes, distribution and eratingsystems with respect to their impact on the health and safety of our employees and the public, as ell as their impact on the environment.

ıarticular concern to control or eliminate releases of those substances into the atmosphere which are n as ozone depleting substances (ODSs).

Montreal Protocol (1987) and its London Amendments (1990) intend to severely restrict the use of ODSs orbid their use within the next ten years. Various national and international initiatives are pressing for an ır ban on these substances.

ay Semiconductor GmbH has been able to use its policy of continuous improvements to eliminate the ıf ODSs listed in the following documents.

nnex A, B and list of transitional substances of the Montreal Protocol and the London Amendments spectively

lass I and II ozone depleting substances in the Clean Air Act Amendments of 1990 by the Environmental rotection Agency (EPA) in the USA

ouncil Decision 88/540/EEC and 91/690/EEC Annex A, B and C (transitional substances) respectively.

ay Semiconductor GmbH can certify that our semiconductors are not manufactured with ozone depleting tances and do not contain such substances.

Vishay Semiconductor GmbH, P.O.B. 3535, D-74025 Heilbronn, Germany
Telephone: 49 (0)7131 67 2831, Fax number: 49 (0)7131 67 2423

University of California at Berkeley
Physics 111 Laboratory
Basic Semiconductor Circuits (BSC)

Lab 12

Analog-to-Digital (ADC) and Digital-to-Analog Conversion (DAC)

Reading:

Horowitz & Hill	Chapter 9.15-9.26
Haynes & Horowitz	Pages 406-415
Stubbins	Chapter 12 (see Appendix 2)
Higgins	Pages 258-285 (see Appendix 2)
Millman & Grabel	Chapter 16.4-16.5
Senturia & Wedlock	Chapter 18.3
Sedra & Smith	Chapter 10.9-10.11

In this week's lab you will learn the basics of digital circuits, including digital logic, (TTL) switches, flip-flops, and counters.

Pre-lab questions:

1. What is an ADC? DAC? How are these useful?
2. What is Shannon's sampling theorem? Give a short, plausible argument for this theorem.

General remarks: CMOS ADC and DAC chips are very sensitive to static electricity. Be sure to touch the conductive foam and the circuit ground before you remove the chips from the foam. Double Check your wiring carefully before turning on power. In particular, check that the ADC is connected to the +5 V supply, in contrast to the DAC, which needs +15 V and -15 V. Input signals for the ADC must always be in the range 0 to +5 V (**no negative inputs!**). Check input signals using the scope (set to DC) before connecting them to the ADC.

he lab:

conversion of voltage levels into digital numbers is important in the interface between digital essors (computers, transmission lines, etc.) and the real world. The integrated circuit ADC0804 layout is in Figure 12.1 and data sheet is in the Appendix) contains a complete 8-bit analog-to-al converter and the necessary circuitry to interface it to a microprocessor. Details about the ation can be obtained from the data sheets following this section. The ADC0804 is based on the essive-approximation principle (see, for example, Horowitz and Hill, p. 622). The following iections are available (also see list below).

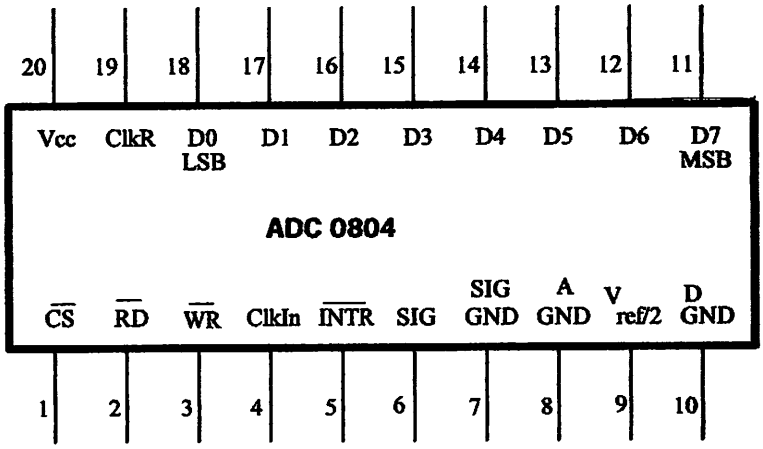


Figure 12.1 Pin assignment of ADC 0804 chip

cription of 20-pin-DIP ADC0804 chip

1 $\overline{CS}$ (chip select) : it activates the ADC when a '0' is at this input. The ADC will not pt read/write commands unless the chip is selected. This is very important when the ADC nnected to a computer data bus with many other devices (memory, other ADCs, DACs, I/O port, etc.).

2 $\overline{RD}$: a '0' at this input will cause the (digital) result to be applied to the output pins if chip is selected.

3 $\overline{WR}$: a '0' at this input will start the conversion process if the chip is selected.

4 ClkIn: input of the clock generator trigger circuit. It can be used for an external clock al.

5 $\overline{INTR}$: a '0' at this output signals the end of a conversion process.

Pins 6 & 7 Differential inputs. The voltage difference between these inputs is converted into an 8-bit number.

Pin 8 ADC ground.

Pin 9 Reference voltage. It determines the coefficient between the analog input and the digital output. The maximum digital output, 2^8-1, corresponds to twice the voltage of this pin.

Pin 10 Separate ground for the clock generator.

Pins 11-18 Digital outputs such that pin 11 corresponds to MSB (Most Significant Bit=2^7) and pin 18 is LSB(Least Significant Bit=2^0).

Pin 19 ClkR: output of the clock generator trigger circuit. Feedback of the trigger output to the input via an RC circuit causes the clock generator to oscillate.

Pin 20 V_{CC}: positive supply voltage (+5 V).

Normally, the ADC is interfaced to a microprocessor (μp) or computer as shown in Figure 12.2.

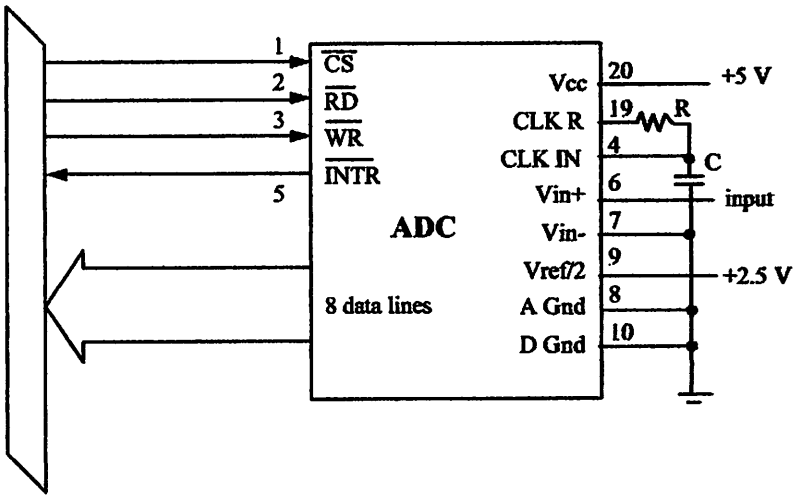


Figure 12.2 Connection of ADC0804 to a computer bus

The μp selects the ADC by asserting $\overline{CS}$, and sends a $\overline{WR}$ signal to start a conversion and then goes off to do something useful. After the ADC is finished with the conversion, it sends an interrupt ($\overline{INTR}$) get the μp's attention. Once the μp is ready to use the digitized output, it selects the ADC ($\overline{CS}$) and sends a $\overline{RD}$ signal to cause the result to be applied to the outputs at pins 11 to 18, which are connected to the data bus. The outputs are so-called tri-state outputs ('0'- '1' - 'inactive') which in their inactive mode ($\overline{RD}$ ='1') they don't influence the data bus. The latter feature allows the

uts to be connected directly to the bus; without the $\overline{RD}$ ='0' signal, they don't interfere with the ıal operation of the bus.

Since we do not want to bother with a µp, we operate the ADC in a simplified mode: the $\overline{WR}$ ıt is connected to the $\overline{INTR}$ output, and $\overline{CS}$ and $\overline{RD}$ are connected to '0.' As a result, when ADC is done with one conversion, it sets the digital outputs and starts the next conversion. ctly speaking, one has to provide a way to start the first conversion after power-up; usually, ısients due to the power-up will take care of this.

e: If your circuit is not working, it may be that the first conversion has not started. Look at $\overline{WR}$ he scope. There should be many small, quick spikes appearing on it. If not, you must signal the ; conversion To do this, momentarily short $\overline{WR}$ to ground with a second wire.

ital Voltmeter

l We can use the ADC to build a simple 2-digit DVM (Figure 12.3). Use the 25k potentiometer a DC input signal between 0 and 5 V.

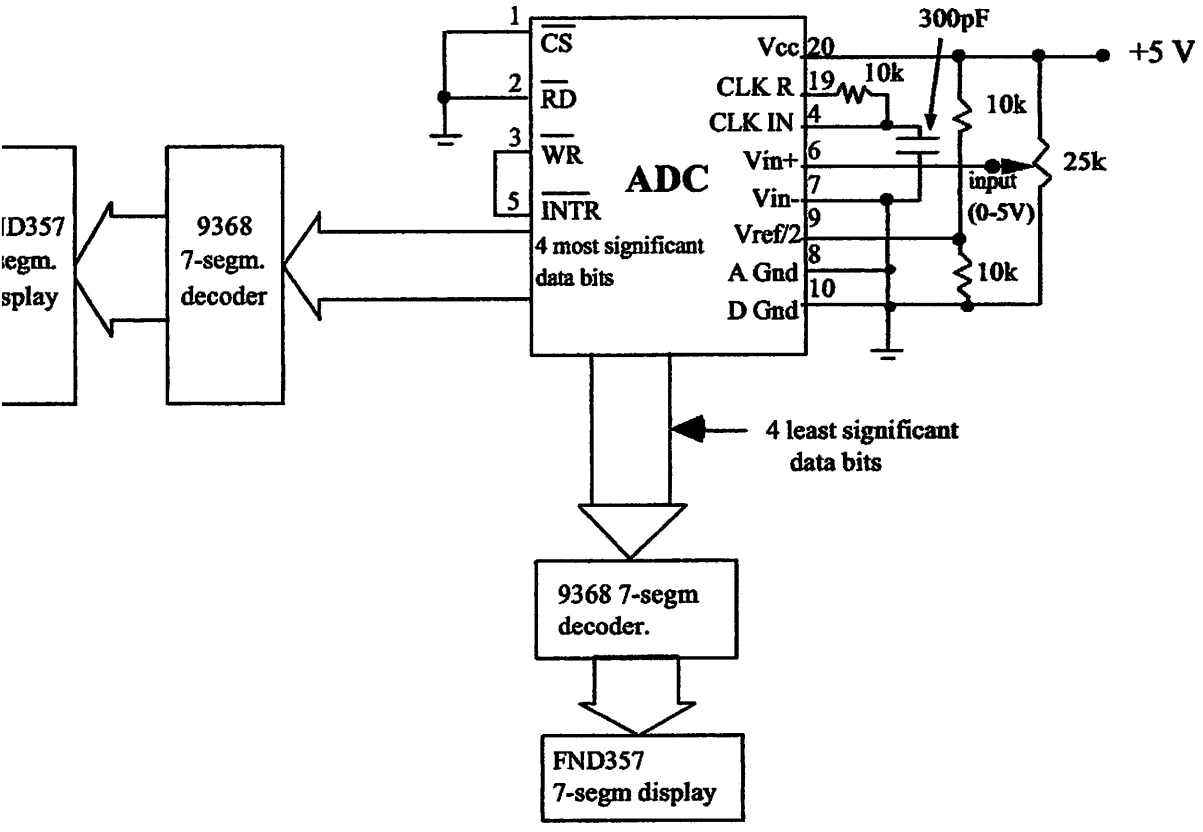


Figure 12.3 Circuit of a 2-digit DVM

Note that the display is hexadecimal; it shows 1,2,3...8,9,A,B,C,D,E,F.

Measure the clock frequency by examining the signal at pin 19. We advise that you use a *frequency-compensated probe* (a "10x probe"); the ordinary scope probe will disturb your measurement since the cable capacitance will alter the clock's capacitance. Measure the conversion time by connecting the scope to pin 5. Does the conversion time depend on the size of the input signal? Do you expect it to, given that the ADC is based on the successive-approximation principle? How many clock cycles does a conversion take? See data sheets for more information.

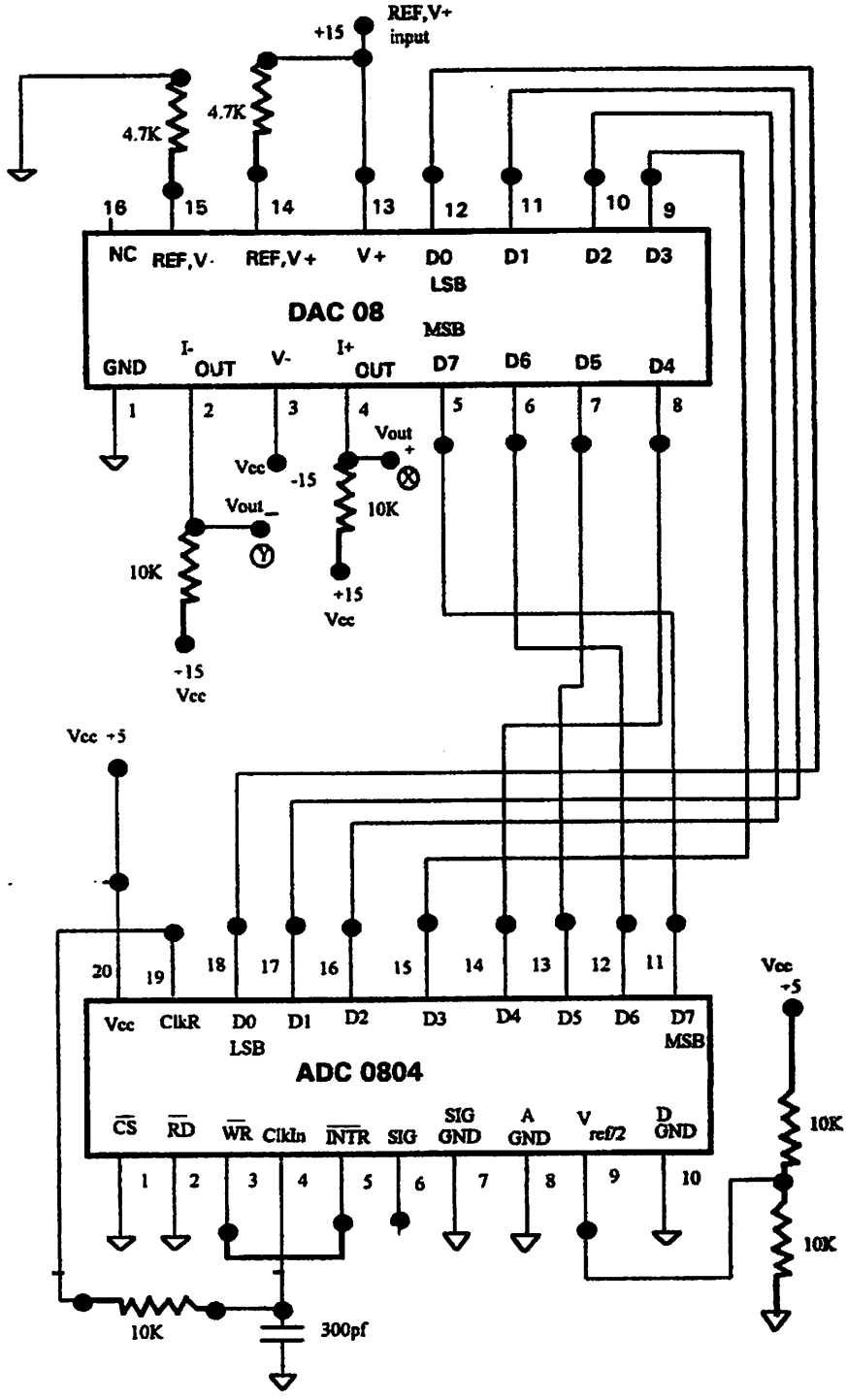
12.2 Determine precisely the input voltages corresponding to steps of 10_{hex} in the digital output, and plot the result. Is the ADC linear? From the data, calculate the conversion coefficient (counts/Volt). Does it agree with your expectations?

DAC and digital transmission

The currents from the analog outputs (pins 2 and 4) of the DAC08 (See Figure 12.4) correspond to the digital input number (pin 5=MSB to pin 12=LSB), with a conversion coefficient determined by the currents applied to the reference inputs (pins 14 and 15). Whenever the digital input is changed, the output settles to the new analog value within 100 ns. The DAC has two outputs (pins 4 and 2), a normal and an inverting one, which usually drive a differential amplifier. (See below, Section 12.3)

12.3 We are now ready to simulate a digital transmission chain, for example, used in modern phone systems or (with intermediate digital storage) in compact disc players. Build the circuit in Figure 12.4 and connect the digital outputs of the ADC to the inputs of the DAC and connect the scope to the DAC outputs. Connect V_{out} - to Y input on the scope, invert it, and V_{out} + to X input. Generate a 100 Hz, 1V p-p sine wave oscillating between about +2 and +3 V and apply it to the ADC input; you will need to use a DC level shifter. Readjust the offset and the amplitude of the signal generator such that the DAC output signal does not clip. Try different input signal shapes and frequencies and sketch how the DAC output tracks the ADC input.

Analog-to-Digital (ADC) and Digital-to-Analog Conversion (DAC)



Circuit for connecting ADC to DAC

Figure 12.4

12.4 Shannon's sampling theorem for minimal reproduction of a signal requires a sampling rate corresponding to twice the highest input frequency. This rate is often called the Nyquist frequency. Study this situation with your ADC/DAC system. What happens if the input signal is increased beyond half the sampling rate? Particularly interesting are the cases where the input frequency is close to a multiple of the sampling rate.

12.5 In practical applications, one usually wants to get rid of the steps in the output signal. This can be achieved by a low-pass filter to smooth the DAC output. Build the active filter circuit with an operational amplifier LF356 as shown in Figure 13.5 and measure its frequency response with sine waves. (Use the 10X scope probe.)

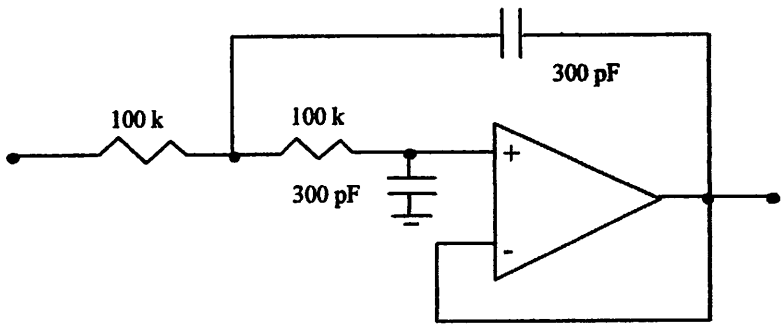


Figure 12.5 Active filter for smoothing the DAC output

(use a LF356 OpAmp)

Connect the filter to the DAC output and observe its effect. Measure the frequency response of the ADC/DAC/filter transmission chain by measuring the output voltage with the scope. Try again to increase the input frequency well above the sampling frequency — at certain frequencies, you will still observe significant output signals at a lower frequency than the input frequency. This is called "ghosting." To avoid this effect, real digital transmission systems have low-pass filters both in the inputs and outputs.

OPTIONAL: How about designing your own ADC? With your knowledge in analog and digital electronics, is shouldn't be too hard to build a 4-bit ADC. Start out with a home-made 4-bit DAC. The DAC resistors, if they are not too small, can be driven directly by any TTL output. Hook the DAC up to a 7490 counter driven by a gated clock signal (made using the 555), and add an opamp to compare DAC output and analog input. Now you need only a little logic circuit to stop the counter when the DAC output exceeds the input signal. Hint: switching transients from the DAC may be a problem - if necessary, add an appropriate RC low-pass filter at the DAC output. See the following diagram:

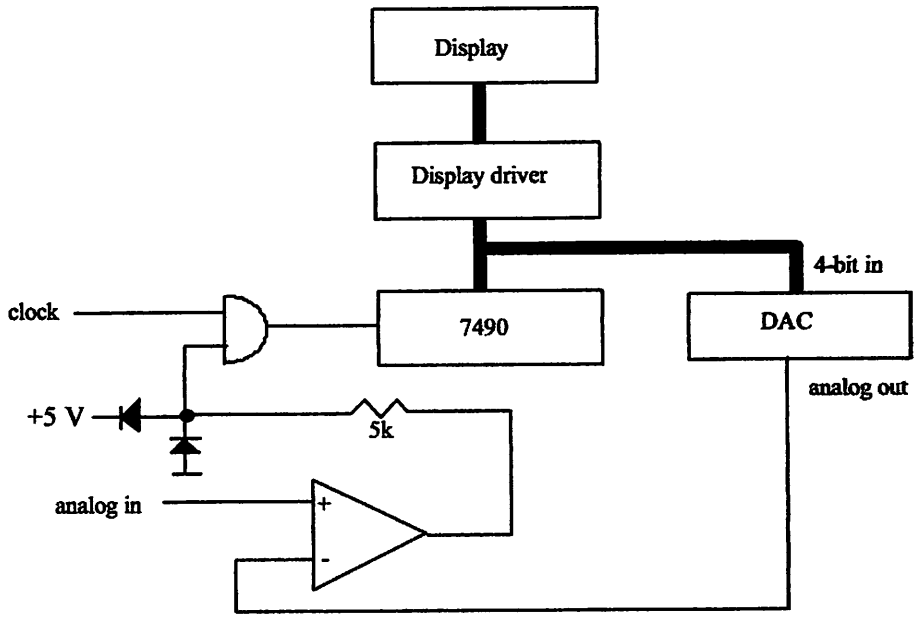


Figure 12.6 A simple ADC circuit

e that the opamp is running at full open-loop gain and is used as a voltage comparator. The stor-diode combination in its output limits the signal driving the gate. TTL gates don't like 15 V ıt signals.

ɜstions:

(See Section 12.5) Calculate the transfer function of the active filter as a function of the ıponent values R and C.

e the following pages for part of the data sheets on)C-0804 and the DAC 08

Appendix DAC-08 Motorola data sheet

Order this data sheet by DAC-08

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DAC-08

Specifications and Applications Information

HIGH SPEED 8-BIT MULTIPLYING D-TO-A CONVERTER

SILICON MONOLITHIC INTEGRATED CIRCUIT

HIGH SPEED 8-BIT MULTIPLYING D-TO-A CONVERTER

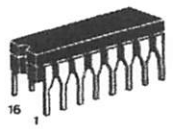
The DAC-08 series is a monolithic 8-bit high speed multiplying digital-to-analog converter, capable of settling to within 1/2 LSB (0.19%) in 85 ns. Monotonic multiplying performance is retained over a wide 40-to-1 reference current range. Full scale and reference currents are matched to within 1 LSB, therefore eliminating the need for full scale trim in most applications.

Dual complementry current outputs with high voltage compliance provide added versatility and allow differential mode of operation to effectively double the peak-to-peak output swing. In many applications, output current-to-voltage conversion can be accomplished without requiring an external op amp. Noise-immune inputs permit direct interface with TTL and DTL levels when the logic threshold control, V_{LC}, (Pin 1) is grounded. All other logic family thresholds are attainable by adjusting the voltage level of Pin 1. Performance characteristics are virtually unchanged over the entire ±4.5 V to ±18 V power supply range. Power consumption is typically 33 mW with ±5.0 V supplies.

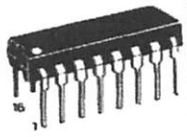
The DAC-08 is available in several versions, with nonlinearity as tight as ±0.1% (± 1/4 LSB) over temperature. All versions are guaranteed monotonic over 8 bits. For an extra margin of performance, Motorola utilizes thin-film resistors permitting very accurate resistive values which are extremely stable over temperature.

High performance characteristics along with low cost, make the DAC-08 an excellent selection for applications such as CRT displays, waveform generation, high-speed modems, and high-speed analog-to-digital converters.

- Fast Settling Time — 85 ns
- Full Scale Current Prematched to ±1 LSB
- Nonlinearity Over Temperature to ±0.1% Max
- Differential Current Outputs
- High Voltage Compliance Outputs 10 V to + 18 V
- Wide Range Multiplying Capability
- Inputs Compatable With TTL, DTL, CMOS, PMOS, ECL, HTL
- Low Full Scale Current Drift
- Wide Power Supply Range ±4.5 V to ±18 V
- Low Power Consumption
- Thin-Film Resistors
- Low Cost



Q SUFFIX
CERAMIC PACKAGE
CASE 620-02

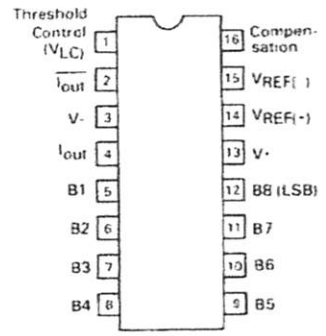


P SUFFIX
PLASTIC PACKAGE
CASE 648-06

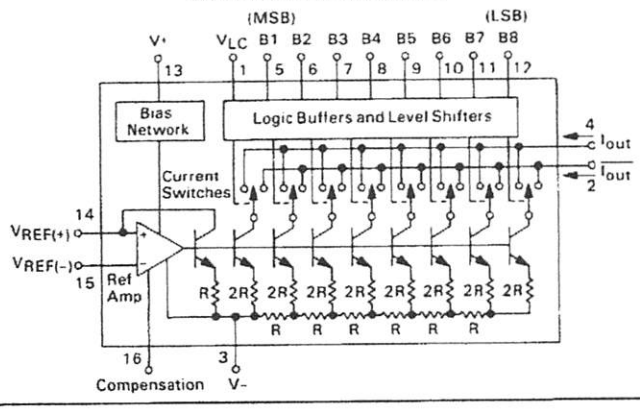
D SUFFIX
PLASTIC PACKAGE
CASE 751B-01
SO-16*

***Surface Mount pin-out is different than standard package pin-out for this device.**

PINOUT DIAGRAM



DAC-08 EQUIVALENT CIRCUIT



Device	Nonlinearity	Temperature Range	Package
DAC-08AQ	±0.1%	−55°C to +125°C	Ceramic
DAC-08Q	±0.19%		Ceramic
DAC-08HQ	±0.1%	0°C to +70°C	Ceramic
DAC-08EQ	±0.19%		Ceramic
DAC-08CQ	±0.39%		Ceramic
DAC-08CD	±0.39%		SO-16
DAC-08ED	±0.19%		SO-16
DAC-08HP	±0.1%		Plastic
DAC-08EP	±0.19%		Plastic
DAC-08CP	±0.39%		Plastic

Appendix DAC-08 Motorola data sheet

MAXIMUM RATINGS (T_A = 25°C unless otherwise noted)

Rating	Symbol	Value	Unit
V+ Supply to V-Supply	—	36	V
Logic Inputs	—	V- to V- Plus 36	V
Logic Threshold Control	V_{LC}	V- to V+	V
Analog Current Outputs	I_{out}	See Figure 7	mA
Reference Inputs (V14, V15)	V_{REF}	V- to V+	V
Reference Input Differential Voltage (V14 to V15)	$V_{REF(D)}$	±18	V
Reference Input Current (I14)	I_{REF}	5.0	mA
Operating Temperature Range DAC-08AQ, Q DAC-08HQ, EQ, CQ, HP, EP, CP, ED, CD	T_A	 -55 to +125 0 to +70	°C
Storage Temperature	T_A	-65 to +150	°C
Power Dissipation Derate above 100°C	P_D $R_{\theta JA}$	500 10	mW mW/°C

ELECTRICAL CHARACTERISTICS (V_S = ±15 V, I_{REF} = 2.0 mA, T_A = -55° C to +125° C, unless otherwise noted.)

Characteristic	Symbol	DAC-08A			DAC-08			Unit
		Min	Typ	Max	Min	Typ	Max	
Resolution	—	8	8	8	8	8	8	Bits
Monotonicity	—	8	8	8	8	8	8	Bits
Nonlinearity, T_A = 0°C to +70°C	NL	—	—	±0.1	—	—	±0.19	%FS
Settling Time to ±1/2 LSB, Figure 24 (All Bits Switched On or Off, T_A = 25°C)(Note 1)	t_s	—	85	135	—	85	150	ns
Propagation Delay, T_A = 25°C (Note 1) Each Bit All Bits Switched	 t_{PLH} t_{PHL}	 — —	 35 35	 60 60	 — —	 35 35	 60 60	ns
Full Scale Tempco	TCI_{FS}	—	±10	±50	—	±10	±80	ppm/°C
Output Voltage Compliance Full Scale Current Change < 1/2 LSB, R_{out} > 20 megohm typ.	V_{OC}	-10	—	+18	-10	—	+18	V
Full Range Current (V_{REF} = 10.000 V; R14, R15 = 5.000 kΩ, T_A = 25°C)	I_{FR4}	1.984	1.992	2.000	1.94	1.99	2.04	mA
Full Range Symmetry (I_{FR4} - I_{FR2})	I_{FRS}	—	±0.5	±4.0	—	±1.0	±8.0	µA
Zero Scale Current	I_{ZS}	—	0.1	1.0	—	0.2	2.0	µA
Output Current Range V- = -5.0 V V- = -8.0 V to -18 V	 I_{OR1} I_{OR2}	 0 0	 — —	 2.1 4.2	 0 0	 — —	 2.1 4.2	mA
Logic Input Levels (V_{LC} = 0 V) Logic "0" Logic "1"	 V_{IL} V_{IH}	 — 2.0	 — —	 0.8 —	 — 2.0	 — —	 0.8 —	V
Logic Input Current (V_{LC} = 0 V) Logic Input "0" (V_{in} = -10 V to +0.8 V) Logic Input "1" (V_{in} = +2.0 V to +18 V)	 I_{IL} I_{IH}	 — —	 -2.0 0.002	 -10 10	 — —	 -2.0 0.002	 -10 10	µA
Logic Input Swing, V- = -15 V	V_{IS}	-10	—	+18	-10	—	+18	V
Logic Threshold Range, V_S = ±15 V	V_{THR}	-10	—	+13.5	-10	—	+13.5	V
Reference Bias Current	I_{15}	—	-1.0	-3.0	—	-1.0	-3.0	µA
Reference Input Slew Rate Figure 19 (Note 1)	di/dt	4.0	8.0	—	4.0	8.0	—	mA/µs
Power Supply Sensitivity (I_{REF} = 1.0 mA) V+ = 4.5 V to 18 V V- = -4.5 V to -18 V	 $PSSI_{FS+}$ $PSSI_{FS-}$	 — —	 ±0.0003 ±0.002	 ±0.01 ±0.01	 — —	 ±0.0003 ±0.002	 ±0.01 ±0.01	%/%
Power Supply Current V_S = ±5.0 V, I_{REF} = 1.0 mA V_S = +5.0 V, -15 V, I_{REF} = 2.0 mA V_S = ±15 V, I_{REF} = 2.0 mA	 I+ I- I+ I- I+ I-	 — — — — — —	 2.3 -4.3 2.4 -6.4 2.5 -6.5	 3.8 -5.8 3.8 -7.8 3.8 -7.8	 — — — — — —	 2.3 -4.3 2.4 -6.4 2.5 -6.5	 3.8 -5.8 3.8 -7.8 3.8 -7.8	mA
Power Dissipation V_S = ±5.0 V, I_{REF} = 1.0 mA V_S = +5.0 V, -15 V, I_{REF} = 2.0 mA V_S = ±15 V, I_{REF} = 2.0 mA	P_D	 — — —	 33 103 135	 48 136 174	 — — —	 33 108 135	 48 136 174	mW

Note 1. Parameter is not 100% tested; guaranteed by design.

Appendix DAC-08 Motorola data sheet

ELECTRICAL CHARACTERISTICS (V_S = ±15 V, I_{REF} = 2.0 mA, T_A = 0°C to 70°C, unless otherwise noted.)

Characteristic	Symbol	DAC-08H			DAC-08E			DAC-08C			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
Resolution	—	8	8	8	8	8	8	8	8	8	Bits
Monotonicity	—	8	8	8	8	8	8	8	8	8	Bits
Nonlinearity, T_A = 0°C to +70°C	NL	—	—	±0.1	—	—	±0.19	—	—	±0.39	%FS
Settling Time to ±1/2 LSB (All Bits Switched On or Off, (T_A = 25°C) Figure 24 (Note 1)	t_s	—	85	135	—	85	150	—	85	150	ns
Propagation Delay, T_A = 25°C (Note 1)											ns
Each Bit	t_{PLH}	—	35	60	—	35	60	—	35	60	
All Bits Switched	t_{PHL}	—	35	60	—	35	60	—	35	60	
Full Scale Tempco	TCI_{FS}	—	±10	±50	—	±10	±50	—	±10	±80	ppm/°C
Output Voltage Compliance Full Scale Current Change < 1/2 LSB, R_{out} > 20 megohm typ.	V_{OC}	−10	—	+18	−10	—	+18	−10	—	+18	V
Full Range Current (V_{REF} = 10.000 V; R14, R15 = 5.000 kΩ) T_A = 25°C	I_{FR4}	1.984	1.992	2.000	1.94	1.99	2.04	1.94	1.99	2.04	mA
Full Range Symmetry (I_{FR4} - I_{FR2})	I_{FRS}	—	±0.5	±4.0	—	±1.0	±8.0	—	±2.0	±16.0	μA
Zero Scale Current	I_{ZS}	—	0.1	1.0	—	0.2	2.0	—	0.2	4.0	μA
Output Current Range											mA
V− = −5.0 V	I_{OR1}	0	—	2.1	0	—	2.1	0	—	2.1	
V− = −8.0 V to −18 V	I_{OR2}	0	—	4.2	0	—	4.2	0	—	4.2	
Logic Input Levels (V_{LC} = 0 V)											V
Logic "0"	V_{IL}	—	—	0.8	—	—	0.8	—	—	0.8	
Logic "1"	V_{IH}	2.0	—	—	2.0	—	—	2.0	—	—	
Logic Input Current (V_{LC} = 0 V)											μA
Logic Input "0" (V_{in} = −10 V to +0.8 V)	I_{IL}	—	−2.0	−10	—	−2.0	−10	—	−2.0	−10	
Logic Input "1" (V_{in} = +2.0 V to +18 V)	I_{IH}	—	0.002	10	—	0.002	10	—	0.002	10	
Logic Input Swing, V− = −15 V	V_{IS}	−10	—	+18	−10	—	+18	−10	—	+18	V
Logic Threshold Range, V_S = ±15 V	V_{THR}	−10	—	+13.5	−10	—	+13.5	−10	—	+13.5	V
Reference Bias Current	I_{15}	—	−1.0	−3.0	—	−1.0	−3.0	—	−1.0	−3.0	μA
Reference Input Slew Rate Figure 19 (Note 1)	dI/dt	4.0	8.0	—	4.0	8.0	—	4.0	8.0	—	mA/μs
Power Supply Sensitivity (I_{REF} = 1.0 mA)											%/%
V+ = 4.5 V to 18 V	$PSSI_{FS+}$	—	±0.0003	±0.01	—	±0.0003	±0.01	—	±0.0003	±0.01	
V− = −4.5 V to −18 V	$PSSI_{FS-}$	—	±0.002	±0.01	—	±0.002	±0.01	—	±0.002	±0.01	
Power Supply Current	I+	—	2.3	3.8	—	2.3	3.8	—	2.3	3.8	mA
V_S = ±5.0 V, I_{REF} = 1.0 mA	I−	—	−4.3	−5.8	—	−4.3	−25.8	—	−4.3	−5.8	
	I+	—	2.4	3.8	—	2.4	3.8	—	2.4	3.8	
V_S = +5.0 V, −15 V, I_{REF} = 2.0 mA	I−	—	−6.4	−7.8	—	−6.4	−7.8	—	−6.4	−7.8	
	I+	—	2.5	3.8	—	2.5	3.8	—	2.5	3.8	
V_S = ±15 V, I_{REF} = 2.0 mA	I−	—	−6.5	−7.8	—	−6.5	−7.8	—	−6.5	−7.8	
Power Dissipation	P_D										mW
V_S = ±5.0 V, I_{REF} = 1.0 mA		—	33	48	—	33	48	—	33	48	
V_S = +5.0 V, −15 V, I_{REF} = 2.0 mA		—	108	136	—	108	136	—	108	136	
V_S = ±15 V, I_{REF} = 2.0 mA		—	135	174	—	135	174	—	135	174	

Note 1. Parameter is not 100% tested; guaranteed by design.

National Semiconductor

December 1994

ADC0801/ADC0802/ADC0803/ADC0804/ADC0805 8-Bit μP Compatible A/D Converters

General Description

The ADC0801, ADC0802, ADC0803, ADC0804 and ADC0805 are CMOS 8-bit successive approximation A/D converters that use a differential potentiometric ladder—similar to the 256R products. These converters are designed to allow operation with the NSC800 and INS8080A derivative control bus with TRI-STATE® output latches directly driving the data bus. These A/Ds appear like memory locations or I/O ports to the microprocessor and no interfacing logic is needed.

Differential analog voltage inputs allow increasing the common-mode rejection and offsetting the analog zero input voltage value. In addition, the voltage reference input can be adjusted to allow encoding any smaller analog voltage span to the full 8 bits of resolution.

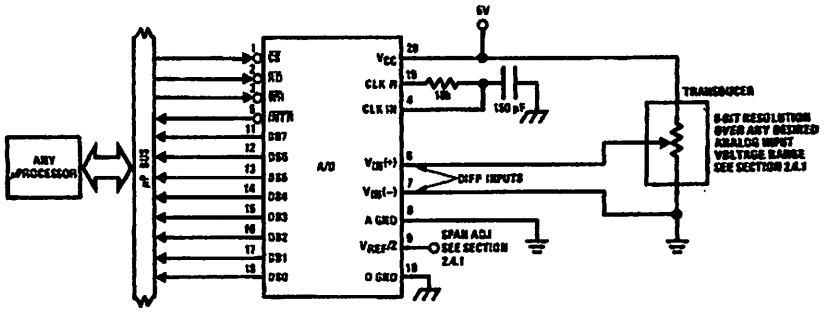
Features

- Compatible with 8080 μP derivatives—no interfacing logic needed - access time - 135 ns
- Easy interface to all microprocessors, or operates "stand alone"
- Differential analog voltage inputs
- Logic inputs and outputs meet both MOS and TTL voltage level specifications
- Works with 2.5V (LM336) voltage reference
- On-chip clock generator
- 0V to 5V analog input voltage range with single 5V supply
- No zero adjust required
- 0.3" standard width 20-pin DIP package
- 20-pin molded chip carrier or small outline package
- Operates ratiometrically or with 5 V_{DC}, 2.5 V_{DC}, or analog span adjusted voltage reference

Key Specifications

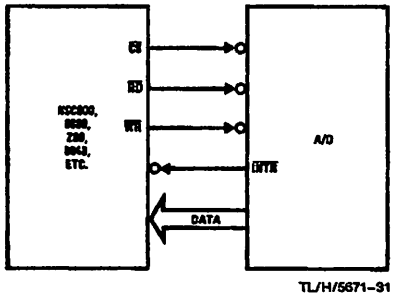
- Resolution: 8 bits
- Total error: ±¼ LSB, ±½ LSB and ±1 LSB
- Conversion time: 100 μs

Typical Applications



TL/H/5671–1

8080 Interface



TL/H/5671–31

Error Specification (Includes Full-Scale, Zero Error, and Non-Linearity)			
Part Number	Full-Scale Adjusted	$V_{REF}/2 = 2.500\ V_{DC}$ (No Adjustments)	$V_{REF}/2$ = No Connection (No Adjustments)
ADC0801	±¼ LSB		
ADC0802		±½ LSB	
ADC0803	±½ LSB		
ADC0804		±1 LSB	
ADC0805			±1 LSB

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Z-80® is a registered trademark of Zilog Corp.

RRD-B30M115/Printed in U. S. A.

Absolute Maximum Ratings (Notes 1 & 2)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage (V_{CC}) (Note 3)	6.5V
Voltage	
Logic Control Inputs	−0.3V to +18V
At Other Input and Outputs	−0.3V to (V_{CC} +0.3V)
Lead Temp. (Soldering, 10 seconds)	
Dual-In-Line Package (plastic)	260°C
Dual-In-Line Package (ceramic)	300°C
Surface Mount Package	
Vapor Phase (60 seconds)	215°C
Infrared (15 seconds)	220°C
Storage Temperature Range	−65°C to +150°C
Package Dissipation at T_A = 25°C	875 mW
ESD Susceptibility (Note 10)	800V

Operating Ratings (Notes 1 & 2)

Temperature Range	$T_{MIN} \le T_A \le T_{MAX}$
ADC0801/02LJ, ADC0802LJ/883	$-55°C \le T_A \le +125°C$
ADC0801/02/03/04LCJ	$-40°C \le T_A \le +85°C$
ADC0801/02/03/05LCN	$-40°C \le T_A \le +85°C$
ADC0804LCN	$0°C \le T_A \le +70°C$
ADC0802/03/04LCV	$0°C \le T_A \le +70°C$
ADC0802/03/04LCWM	$0°C \le T_A \le +70°C$
Range of V_{CC}	4.5 V_{DC} to 6.3 V_{DC}

Electrical Characteristics

The following specifications apply for V_{CC} = 5 V_{DC}, $T_{MIN} \le T_A \le T_{MAX}$ and f_{CLK} = 640 kHz unless otherwise specified.

Parameter	Conditions	Min	Typ	Max	Units
ADC0801: Total Adjusted Error (Note 8)	With Full-Scale Adj. (See Section 2.5.2)			±¼	LSB
ADC0802: Total Unadjusted Error (Note 8)	$V_{REF}/2$ = 2.500 V_{DC}			±½	LSB
ADC0803: Total Adjusted Error (Note 8)	With Full-Scale Adj. (See Section 2.5.2)			±½	LSB
ADC0804: Total Unadjusted Error (Note 8)	$V_{REF}/2$ = 2.500 V_{DC}			±1	LSB
ADC0805: Total Unadjusted Error (Note 8)	$V_{REF}/2$-No Connection			±1	LSB
$R_{VREF/2}$ Input Resistance (Pin 9)	ADC0801/02/03/05 ADC0804 (Note 9)	2.5 0.75	8.0 1.1		kΩ kΩ
Analog Input Voltage Range	(Note 4) V(+) or V(−)	Gnd−0.05		V_{CC} + 0.05	V_{DC}
DC Common-Mode Error	Over Analog Input Voltage Range		±1/16	±⅛	LSB
Power Supply Sensitivity	V_{CC} = 5 V_{DC} ±10% Over Allowed $V_{IN}(+)$ and $V_{IN}(-)$ Voltage Range (Note 4)		±1/16	±⅛	LSB

AC Electrical Characteristics

The following specifications apply for V_{CC} = 5 V_{DC} and T_A = 25°C unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Units
T_C	Conversion Time	f_{CLK} = 640 kHz (Note 6)	103		114	μs
T_C	Conversion Time	(Note 5, 6)	66		73	$1/f_{CLK}$
f_{CLK}	Clock Frequency Clock Duty Cycle	V_{CC} = 5V, (Note 5) (Note 5)	100 40	640	1460 60	kHz %
CR	Conversion Rate in Free-Running Mode	$\overline{INTR}$ tied to $\overline{WR}$ with $\overline{CS}$ = 0 V_{DC}, f_{CLK} = 640 kHz	8770		9708	conv/s
$t_{W(\overline{WR})L}$	Width of $\overline{WR}$ Input (Start Pulse Width)	$\overline{CS}$ = 0 V_{DC} (Note 7)	100			ns
t_{ACC}	Access Time (Delay from Falling Edge of $\overline{RD}$ to Output Data Valid)	C_L = 100 pF		135	200	ns
t_{1H}, t_{0H}	TRI-STATE Control (Delay from Rising Edge of $\overline{RD}$ to Hi-Z State)	C_L = 10 pF, R_L = 10k (See TRI-STATE Test Circuits)		125	200	ns
t_{WI}, t_{RI}	Delay from Falling Edge of $\overline{WR}$ or $\overline{RD}$ to Reset of $\overline{INTR}$			300	450	ns
C_{IN}	Input Capacitance of Logic Control Inputs			5	7.5	pF
C_{OUT}	TRI-STATE Output Capacitance (Data Buffers)			5	7.5	pF
CONTROL INPUTS [Note: CLK IN (Pin 4) is the input of a Schmitt trigger circuit and is therefore specified separately]						
V_{IN} (1)	Logical "1" Input Voltage (Except Pin 4 CLK IN)	V_{CC} = 5.25 V_{DC}	2.0		15	V_{DC}

AC Electrical Characteristics (Continued)

The following specifications apply for $V_{CC} = 5V_{DC}$ and $T_{MIN} \le T_A \le T_{MAX}$, unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Units
CONTROL INPUTS [Note: CLK IN (Pin 4) is the input of a Schmitt trigger circuit and is therefore specified separately]						
$V_{IN}(0)$	Logical "0" Input Voltage (Except Pin 4 CLK IN)	$V_{CC} = 4.75\ V_{DC}$			0.8	V_{DC}
$I_{IN}(1)$	Logical "1" Input Current (All Inputs)	$V_{IN} = 5\ V_{DC}$		0.005	1	μA_{DC}
$I_{IN}(0)$	Logical "0" Input Current (All Inputs)	$V_{IN} = 0\ V_{DC}$	−1	−0.005		μA_{DC}
CLOCK IN AND CLOCK R						
V_T+	CLK IN (Pin 4) Positive Going Threshold Voltage		2.7	3.1	3.5	V_{DC}
V_T-	CLK IN (Pin 4) Negative Going Threshold Voltage		1.5	1.8	2.1	V_{DC}
V_H	CLK IN (Pin 4) Hysteresis $(V_T+)-(V_T-)$		0.6	1.3	2.0	V_{DC}
$V_{OUT}(0)$	Logical "0" CLK R Output Voltage	$I_O = 360\ \mu A$ $V_{CC} = 4.75\ V_{DC}$			0.4	V_{DC}
$V_{OUT}(1)$	Logical "1" CLK R Output Voltage	$I_O = -360\ \mu A$ $V_{CC} = 4.75\ V_{DC}$	2.4			V_{DC}
DATA OUTPUTS AND $\overline{INTR}$						
$V_{OUT}(0)$	Logical "0" Output Voltage Data Outputs $\overline{INTR}$ Output	 $I_{OUT} = 1.6$ mA, $V_{CC} = 4.75\ V_{DC}$ $I_{OUT} = 1.0$ mA, $V_{CC} = 4.75\ V_{DC}$			 0.4 0.4	 V_{DC} V_{DC}
$V_{OUT}(1)$	Logical "1" Output Voltage	$I_O = -360\ \mu A$, $V_{CC} = 4.75\ V_{DC}$	2.4			V_{DC}
$V_{OUT}(1)$	Logical "1" Output Voltage	$I_O = -10\ \mu A$, $V_{CC} = 4.75\ V_{DC}$	4.5			V_{DC}
I_{OUT}	TRI-STATE Disabled Output Leakage (All Data Buffers)	$V_{OUT} = 0\ V_{DC}$ $V_{OUT} = 5\ V_{DC}$	−3		 3	μA_{DC} μA_{DC}
I_{SOURCE}		V_{OUT} Short to Gnd, $T_A = 25°C$	4.5	6		mA_{DC}
I_{SINK}		V_{OUT} Short to V_{CC}, $T_A = 25°C$	9.0	16		mA_{DC}
POWER SUPPLY						
I_{CC}	Supply Current (Includes Ladder Current) ADC0801/02/03/04LCJ/05 ADC0804LCN/LCV/LCWM	$f_{CLK} = 640$ kHz, $V_{REF}/2 = NC$, $T_A = 25°C$ and $\overline{CS} = 5V$		 1.1 1.9	 1.8 2.5	 mA mA

Note 1: Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. DC and AC electrical specifications do not apply when operating the device beyond its specified operating conditions.

Note 2: All voltages are measured with respect to Gnd, unless otherwise specified. The separate A Gnd point should always be wired to the D Gnd.

Note 3: A zener diode exists, internally, from V_{CC} to Gnd and has a typical breakdown voltage of 7 V_{DC}.

Note 4: For $V_{IN}(-) \ge V_{IN}(+)$ the digital output code will be 0000 0000. Two on-chip diodes are tied to each analog input (see block diagram) which will forward conduct for analog input voltages one diode drop below ground or one diode drop greater than the V_{CC} supply. Be careful, during testing at low V_{CC} levels (4.5V), as high level analog inputs (5V) can cause this input diode to conduct—especially at elevated temperatures, and cause errors for analog inputs near full-scale. The spec allows 50 mV forward bias of either diode. This means that as long as the analog V_{IN} does not exceed the supply voltage by more than 50 mV, the output code will be correct. To achieve an absolute 0 V_{DC} to 5 V_{DC} input voltage range will therefore require a minimum supply voltage of 4.950 V_{DC} over temperature variations, initial tolerance and loading.

Note 5: Accuracy is guaranteed at $f_{CLK} = 640$ kHz. At higher clock frequencies accuracy can degrade. For lower clock frequencies, the duty cycle limits can be extended so long as the minimum clock high time interval or minimum clock low time interval is no less than 275 ns.

Note 6: With an asynchronous start pulse, up to 8 clock periods may be required before the internal clock phases are proper to start the conversion process. The start request is internally latched, see *Figure 2* and section 2.0.

Note 7: The $\overline{CS}$ input is assumed to bracket the $\overline{WR}$ strobe input and therefore timing is dependent on the $\overline{WR}$ pulse width. An arbitrarily wide pulse width will hold the converter in a reset mode and the start of conversion is initiated by the low to high transition of the $\overline{WR}$ pulse (see timing diagrams).

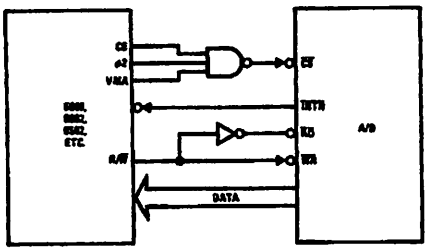
Note 8: None of these A/Ds requires a zero adjust (see section 2.5.1). To obtain zero code at other analog input voltages see section 2.5 and *Figure 5*.

Note 9: The $V_{REF}/2$ pin is the center point of a two-resistor divider connected from V_{CC} to ground. In all versions of the ADC0801, ADC0802, ADC0803, and ADC0805, and in the ADC0804LCJ, each resistor is typically 16 kΩ. In all versions of the ADC0804 except the ADC0804LCJ, each resistor is typically 2.2 kΩ.

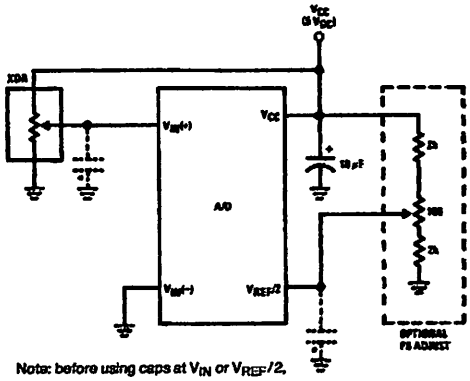
Note 10: Human body model, 100 pF discharged through a 1.5 kΩ resistor.

Typical Applications (Continued)

6800 Interface

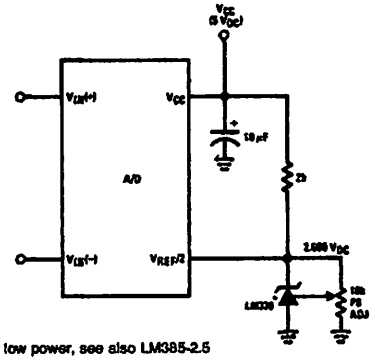


Ratiometric with Full-Scale Adjust



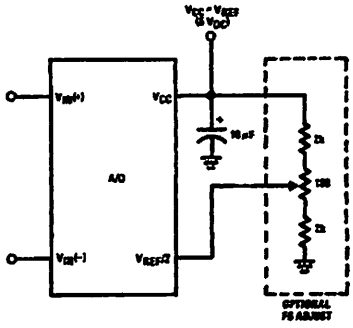
Note: before using caps at V_{IN} or $V_{REF}/2$, see section 2.3.2 Input Bypass Capacitors.

Absolute with a 2.500V Reference

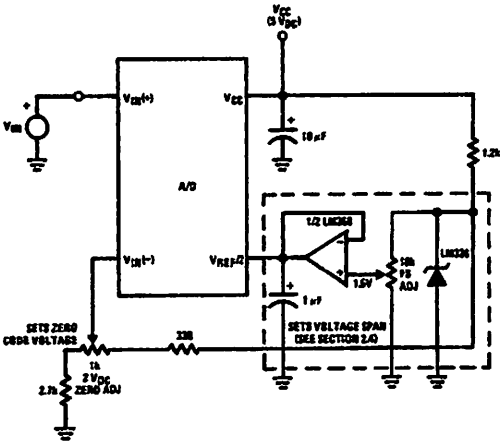


*For low power, see also LM385-2.5

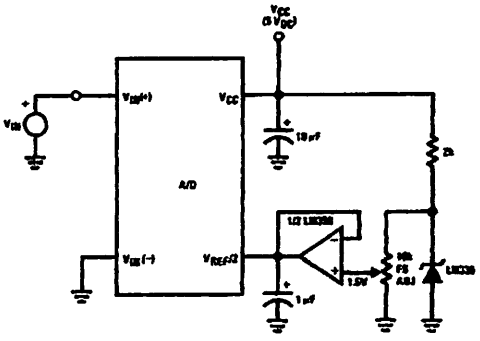
Absolute with a 5V Reference



Zero-Shift and Span Adjust: $2V \leq V_{IN} \leq 5V$



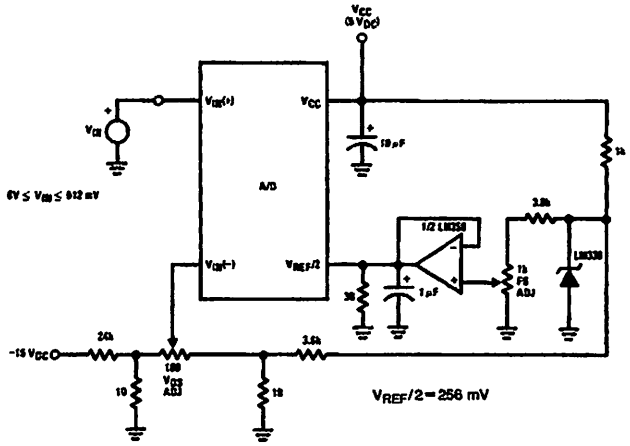
Span Adjust: $0V \leq V_{IN} \leq 3V$



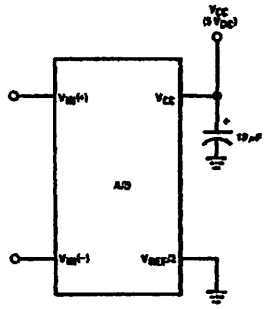
TL/H/5671–5

Typical Applications (Continued)

Directly Converting a Low-Level Signal



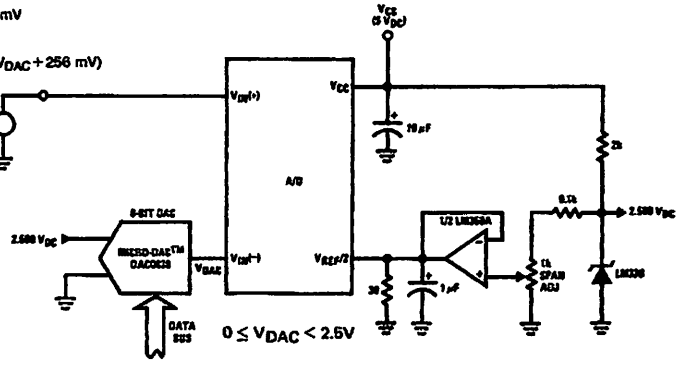
A µP Interfaced Comparator



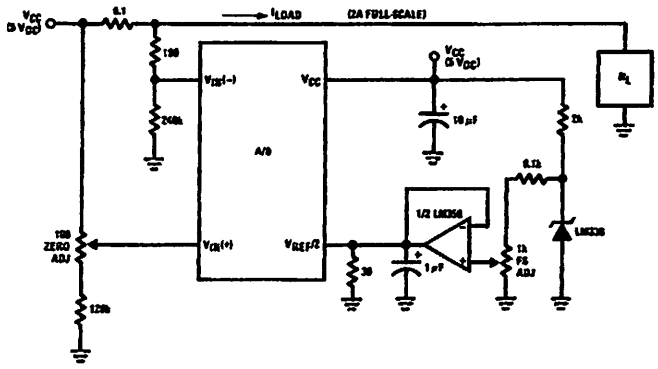
For: $V_{IN}(+) > V_{IN}(-)$
Output = FF_{HEX}
For: $V_{IN}(+) < V_{IN}(-)$
Output = 00_{HEX}

1 mV Resolution with µP Controlled Range

$V_{REF}/2 = 128$ mV
1 LSB = 1 mV
$V_{DAC} \leq V_{IN} \leq (V_{DAC} + 256$ mV)



Digitizing a Current Flow



TL/H/5671–6

HARRIS SEMICONDUCTOR

CD4094BMS

CMOS 8-Stage Shift-and-Store Bus Register

nber 1992

eatures

- ligh Voltage Type (20V Rating)
- -State Parallel Outputs for Connection to Common Bus
- Separate Serial Outputs Synchronous to Both Positive nd Negative Clock Edges for Cascading
- Medium Speed Operation - 5MHz at 10V (typ)
- Standardized Symmetrical Output Characteristics
- 100% Tested for Quiescent Current at 20V
- Maximum Input Current of 1μA at 18V Over Full Package Temperature Range; 100nA at 18V and +25°C
- Noise Margin (Over Full Package/Temperature Range)
  - 1V at VDD = 5V
  - 2V at VDD = 10V
  - 2.5V at VDD = 15V
- 5V, 10V and 15V Parametric Ratings
- Meets All Requirements of JEDEC Tentative Standard No. 13B, "Standard Specifications for Description of B' Series CMOS Devices"

pplications

- Serial-to-Parallel Data Conversion
- Remote Control Holding Register
- Dual-Rank Shift, Hold, and Bus Applications

escription

4094BMS is a 8-stage serial shift register having a storage ch associated with each stage for strobing data from the serial ut to parallel buffered 3-state outputs. The parallel outputs ay be connected directly to common bus lines. Data is shifted positive clock transitions. The data in each shift register stage ransferred to the storage register when the STROBE input is h. Data in the storage register appears at the outputs whener the OUTPUT-ENABLE signal is high.

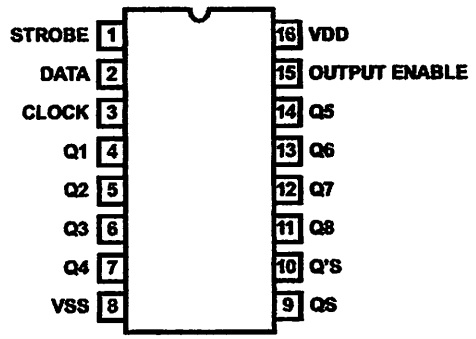
o serial outputs are available for cascading a number of 4094BMS devices. Data is available at the QS serial output minal on positive clock edges to allow for high-speed operan in cascaded systems in which the clock rise time is fast. The me serial information, available at the Q'S terminal on the next gative clock edge, provides a means for cascading 4094BMS devices when the clock rise time is slow.

e CD4094BMS is supplied in these 16 lead outline packages:

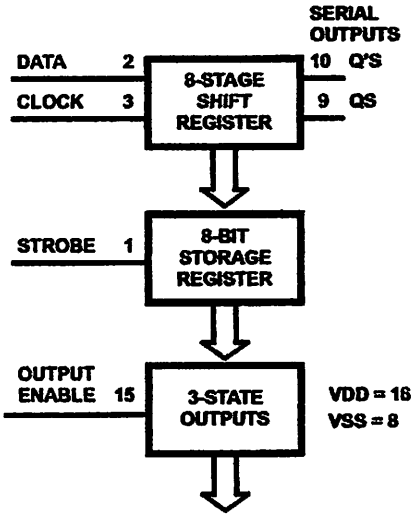
aze Seal DIP	H4X
t Seal DIP	H1F
ramic Flatpack	H6W

Pinout

CD4094BMS
TOP VIEW



Functional Diagram



PARALLEL OUTPUTS Q1 - Q8

(TERMINALS 4, 5, 6, 7, 14, 13, 12, 11, RESPECTIVELY)

ON: These devices are sensitive to electrostatic discharge. Users should follow proper I.C. Handling Procedures.

File Number 3194

solute Maximum Ratings

Supply Voltage Range, (VDD) ..... -0.5V to +20V
/oltage Referenced to VSS Terminals)
ıt Voltage Range, All Inputs .....-0.5V to VDD +0.5V
Input Current, Any One Input .....±10mA
ɔrating Temperature Range.....-55°C to +125°C
'ackage Types D, F, K, H
rage Temperature Range (TSTG).....-65°C to +150°C
d Temperature (During Soldering) ..... +265°C
t Distance 1/16 ± 1/32 Inch (1.59mm ± 0.79mm) from case for 0s Maximum

Reliability Information

	θ_{ja}	θ_{jc}
Thermal Resistance		
Ceramic DIP and FRIT Package.....	80°C/W	20°C/W
Flatpack Package	70°C/W	20°C/W

Maximum Package Power Dissipation (PD) at +125°C
For TA = -55°C to +100°C (Package Type D, F, K).....500mW
For TA = +100°C to +125°C (Package Type D, F, K) .....Derate Linearity at 12mW/°C to 200mW
Device Dissipation per Output Transistor 100mW
For TA = Full Package Temperature Range (All Package Types)
Junction Temperature .....+175°C

TABLE 1. DC ELECTRICAL PERFORMANCE CHARACTERISTICS

PARAMETER	SYMBOL	CONDITIONS (NOTE 1)		GROUP A SUBGROUPS	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
pply Current	IDD	VDD = 20V, VIN = VDD or GND		1	+25°C	-	10	µA
				2	+125°C	-	1000	µA
		VDD = 18V, VIN = VDD or GND		3	-55°C	-	10	µA
ıt Leakage Current	IIL	VIN = VDD or GND	VDD = 20	1	+25°C	-100	-	nA
				2	+125°C	-1000	-	nA
			VDD = 18V	3	-55°C	-100	-	nA
ıt Leakage Current	IIH	VIN = VDD or GND	VDD = 20	1	+25°C	-	100	nA
				2	+125°C	-	1000	nA
			VDD = 18V	3	-55°C	-	100	nA
tput Voltage	VOL15	VDD = 15V, No Load		1, 2, 3	+25°C, +125°C, -55°C	-	50	mV
tput Voltage	VOH15	VDD = 15V, No Load (Note 3)		1, 2, 3	+25°C, +125°C, -55°C	14.95	-	V
tput Current (Sink)	IOL5	VDD = 5V, VOUT = 0.4V		1	+25°C	0.53	-	mA
tput Current (Sink)	IOL10	VDD = 10V, VOUT = 0.5V		1	+25°C	1.4	-	mA
tput Current (Sink)	IOL15	VDD = 15V, VOUT = 1.5V		1	+25°C	3.5	-	mA
tput Current (Source)	IOH5A	VDD = 5V, VOUT = 4.6V		1	+25°C	-	-0.53	mA
tput Current (Source)	IOH5B	VDD = 5V, VOUT = 2.5V		1	+25°C	-	-1.8	mA
tput Current (Source)	IOH10	VDD = 10V, VOUT = 9.5V		1	+25°C	-	-1.4	mA
tput Current (Source)	IOH15	VDD = 15V, VOUT = 13.5V		1	+25°C	-	-3.5	mA
Threshold Voltage	VNTH	VDD = 10V, ISS = -10µA		1	+25°C	-2.8	-0.7	V
Threshold Voltage	VPTH	VSS = 0V, IDD = 10µA		1	+25°C	0.7	2.8	V
nctional	F	VDD = 2.8V, VIN = VDD or GND		7	+25°C	VOH > VDD/2	VOL < VDD/2	V
		VDD = 20V, VIN = VDD or GND		7	+25°C			
		VDD = 18V, VIN = VDD or GND		8A	+125°C			
		VDD = 3V, VIN = VDD or GND		8B	-55°C			
ıt Voltage Low ote 2)	VIL	VDD = 5V, VOH > 4.5V, VOL < 0.5V		1, 2, 3	+25°C, +125°C, -55°C	-	1.5	V
ıt Voltage High ote 2)	VIH	VDD = 5V, VOH > 4.5V, VOL < 0.5V		1, 2, 3	+25°C, +125°C, -55°C	3.5	-	V
ıt Voltage Low ote 2)	VIL	VDD = 15V, VOH > 13.5V, VOL < 1.5V		1, 2, 3	+25°C, +125°C, -55°C	-	4	V
ıt Voltage High ote 2)	VIH	VDD = 15V, VOH > 13.5V, VOL < 1.5V		1, 2, 3	+25°C, +125°C, -55°C	11	-	V
-State Output akage	IOZL	VIN = VDD or GND VOUT = 0V	VDD = 20V	1	+25°C	-0.4	-	µA
				2	+125°C	-12	-	µA
			VDD = 18V	3	-55°C	-0.4	-	µA
-State Output akage	IOZH	VIN = VDD or GND VOUT = VDD	VDD = 20V	1	+25°C	-	0.4	µA
				2	+125°C	-	12	µA
			VDD = 18V	3	-55°C	-	0.4	µA

OTES:
1. All voltages referenced to device GND, 100% testing being implemented.
2. Go/No Go test with limits applied to inputs.
3. For accuracy, voltage is measured differentially to VDD. Limit is 0.050V max.

TABLE 2. AC ELECTRICAL PERFORMANCE CHARACTERISTICS

PARAMETER	SYMBOL	CONDITIONS	GROUP A SUBGROUPS	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
ɔpagation Delay ɔck to Serial Output QS	TPHL1 TPLH1	VDD = 5V, VIN = VDD or GND (Note 1, 2)	9	+25°C	-	600	ns
			10, 11	+125°C, -55°C	-	810	ns
ɔpagation Delay ɔck to Serial Output S	TPHL2 TPLH2	VDD = 5V, VIN = VDD or GND (Note 1, 2)	9	+25°C	-	460	ns
			10, 11	+125°C, -55°C	-	621	ns
ɔpagation Delay ɔck to Parallel Output	TPHL3 TPLH3	VDD = 5V, VIN = VDD or GND (Note 1, 2)	9	+25°C	-	840	ns
			10, 11	+125°C, -55°C	-	1134	ns
ɔpagation Delay ʻobe to Parallel Output	TPHL4 TPLH4	VDD = 5V, VIN = VDD or GND (Note 1, 2)	9	+25°C	-	580	ns
			10, 11	+125°C, -55°C	-	783	ns
ɔpagation Delay ıtput Enable to Parallel ıtput	TPHZ TPZH	VDD = 5V, VIN = VDD or GND (Note 2, 3)	9	+25°C	-	280	ns
			10, 11	+125°C, -55°C	-	378	ns
ɔpagation Delay ıtput Enable to Parallel ıtput	TPLZ TPZL	VDD = 5V, VIN = VDD or GND (Note 2, 3)	9	+25°C	-	200	ns
			10, 11	+125°C, -55°C	-	270	ns
ansition Time	TTHL TTLH	VDD = 5V, VIN = VDD or GND (Note 1, 2)	9	+25°C	-	200	ns
			10, 11	+125°C, -55°C	-	270	ns
ıximum Clock Input equency	FCL	VDD = 5V, VIN = VDD or GND (Note 1, 2)	9	+25°C	1.25	-	MHz
			10, 11	+125°C, -55°C	.93	-	MHz

TES:

CL = 50pF, RL = 200K, Input TR, TF < 20ns.

-55°C and +125°C limits guaranteed, 100% testing being implemented.

CL = 50pF, RL = 1K, Input TR, TF < 20ns.

TABLE 3. ELECTRICAL PERFORMANCE CHARACTERISTICS

PARAMETER	SYMBOL	CONDITIONS	NOTES	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
ıpply Current	IDD	VDD = 5V, VIN = VDD or GND	1, 2	-55°C, +25°C	-	5	µA
				+125°C	-	150	µA
		VDD = 10V, VIN = VDD or GND	1, 2	-55°C, +25°C	-	10	µA
				+125°C	-	300	µA
		VDD = 15V, VIN = VDD or GND	1, 2	-55°C, +25°C	-	10	µA
				+125°C	-	600	µA
ıtput Voltage	VOL	VDD = 5V, No Load	1, 2	+25°C, +125°C, -55°C	-	50	mV
ıtput Voltage	VOL	VDD = 10V, No Load	1, 2	+25°C, +125°C, -55°C	-	50	mV
ıtput Voltage	VOH	VDD = 5V, No Load	1, 2	+25°C, +125°C, -55°C	4.95	-	V
ıtput Voltage	VOH	VDD = 10V, No Load	1, 2	+25°C, +125°C, -55°C	9.95	-	V
ıtput Current (Sink)	IOL5	VDD = 5V, VOUT = 0.4V	1, 2	+125°C	0.36	-	mA
				-55°C	0.64	-	mA
ıtput Current (Sink)	IOL10	VDD = 10V, VOUT = 0.5V	1, 2	+125°C	0.9	-	mA
				-55°C	1.6	-	mA
ıtput Current (Sink)	IOL15	VDD = 15V, VOUT = 1.5V	1, 2	+125°C	2.4	-	mA
				-55°C	4.2	-	mA

TABLE 3. ELECTRICAL PERFORMANCE CHARACTERISTICS (Continued)

PARAMETER	SYMBOL	CONDITIONS	NOTES	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
ıtput Current (Source)	IOH5A	VDD = 5V, VOUT = 4.6V	1, 2	+125°C	-	-0.36	mA
				-55°C	-	-0.64	mA
ıtput Current (Source)	IOH5B	VDD = 5V, VOUT = 2.5V	1, 2	+125°C	-	-1.1	mA
				-55°C	-	-2.0	mA
ıtput Current (Source)	IOH10	VDD = 10V, VOUT = 9.5V	1, 2	+125°C	-	-0.9	mA
				-55°C	-	-2.6	mA
ıtput Current (Source)	IOH15	VDD =15V, VOUT = 13.5V	1, 2	+125°C	-	-2.4	mA
				-55°C	-	-	mA
put Voltage Low	VIL	VDD = 10V, VOH > 9V, VOL < 1V	1, 2	+25°C, +125°C, -55°C	-	3	V
put Voltage High	VIH	VDD = 10V, VOH > 9V, VOL < 1V	1, 2	+25°C, +125°C, -55°C	7	-	V
opagation Delay ock to Serial Output Qs	TPHL1 TPLH1	VDD = 10V	1, 2, 3	+25°C	-	250	ns
		VDD = 15V	1, 2, 3	+25°C	-	190	ns
opagation Delay ock to Serial Output Q's	TPHL2 TPLH2	VDD = 10V	1, 2, 3	+25°C	-	220	ns
		VDD = 15V	1, 2, 3	+25°C	-	150	ns
opagation Delay ock to Parallel Output	TPHL3 TPLH3	VDD = 10V	1, 2, 3	+25°C	-	390	ns
		VDD = 15V	1, 2, 3	+25°C	-	270	ns
opagation Delay robe to Parallel Output	TPHL4 TPLH4	VDD = 10V	1, 2, 3	+25°C	-	290	ns
		VDD = 15V	1, 2, 3	+25°C	-	200	ns
opagation Delay utput Enable to Parallel utput	TPHZ TPZH	VDD = 10V	1, 2, 4	+25°C	-	120	ns
		VDD = 15V	1, 2, 4	+25°C	-	90	ns
opagation Delay utput Enable to Parallel utput	TPLZ TPZL	VDD = 10V	1, 2, 4	+25°C	-	100	ns
		VDD = 15V	1, 2, 4	+25°C	-	80	ns
ansition Time	TTLH TTHL	VDD = 10V	1, 2, 3	+25°C	-	100	ns
		VDD = 15V	1, 2, 3	+25°C	-	80	ns
aximum Clock Input equency	FCL	VDD = 10V	1, 2, 3	+25°C	2.5	-	MHz
		VDD = 15V	1, 2, 3	+25°C	3	-	MHz
inimum Data Setup me	TS	VDD = 5V	1, 2, 3	+25°C	-	125	ns
		VDD = 10V	1, 2, 3	+25°C	-	55	ns
		VDD = 15V	1, 2, 3	+25°C	-	35	ns
aximum Clock Input ise and Fall Time	TRCL TFCL	VDD = 5V	1, 2, 3, 5	+25°C	-	15	µs
		VDD = 10V	1, 2, 3, 5	+25°C	-	5	µs
		VDD = 15V	1, 2, 3, 5	+25°C	-	5	µs
inimum Clock Pulse idth	TW	VDD = 5V	1, 2, 3	+25°C	-	200	ns
		VDD = 10V	1, 2, 3	+25°C	-	100	ns
		VDD = 15V	1, 2, 3	+25°C	-	83	ns
inimum Strobe Pulse idth	TW	VDD = 5V	1, 2, 3	+25°C	-	200	ns
		VDD = 10V	1, 2, 3	+25°C	-	80	ns
		VDD = 15V	1, 2, 3	+25°C	-	70	ns
put Capacitance	CIN	Any Input	1, 2	+25°C	-	7.5	pF

TABLE 3. ELECTRICAL PERFORMANCE CHARACTERISTICS (Continued)

PARAMETER	SYMBOL	CONDITIONS	NOTES	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS

TES:

All voltages referenced to device GND.

The parameters listed on Table 3 are controlled via design or process and are not directly tested. These parameters are characterized on initial design release and upon design changes which would affect these characteristics.

CL = 50pF, RL = 200K, Input TR, TF < 20ns.

CL = 50pF, RL = 1K, Input TR, TF < 20ns.

If more than one unit is cascaded, TRCL should be made less than or equal to the sumof the transition time and the fixed propagation delay of the output of the driving stage for the estimated capacitive load.

TABLE 4. POST IRRADIATION ELECTRICAL PERFORMANCE CHARACTERISTICS

PARAMETER	SYMBOL	CONDITIONS	NOTES	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
ıpply Current	IDD	VDD = 20V, VIN = VDD or GND	1, 4	+25°C	-	25	µA
Threshold Voltage	VNTH	VDD = 10V, ISS = -10µA	1, 4	+25°C	-2.8	-0.2	V
Threshold Voltage ılta	ΔVTN	VDD = 10V, ISS = -10µA	1, 4	+25°C	-	±1	V
Threshold Voltage	VTP	VSS = 0V, IDD = 10µA	1, 4	+25°C	0.2	2.8	V
Threshold Voltage ılta	ΔVTP	VSS = 0V, IDD = 10µA	1, 4	+25°C	-	±1	V
ınctional	F	VDD = 18V, VIN = VDD or GND	1	+25°C	VOH > VDD/2	VOL < VDD/2	V
		VDD = 3V, VIN = VDD or GND					
opagation Delay Time	TPHL TPLH	VDD = 5V	1, 2, 3, 4	+25°C	-	1.35 x +25°C Limit	ns

)TES: 1. All voltages referenced to device GND.
2. CL = 50pF, RL = 200K, Input TR, TF < 20ns.
3. See Table 2 for +25°C limit.
4. Read and Record

TABLE 5. BURN-IN AND LIFE TEST DELTA PARAMETERS +25°C

PARAMETER	SYMBOL	DELTA LIMIT
Supply Current - MSI-2	IDD	± 1.0µA
Output Current (Sink)	IOL5	± 20% x Pre-Test Reading
Output Current (Source)	IOH5A	± 20% x Pre-Test Reading

TABLE 6. APPLICABLE SUBGROUPS

CONFORMANCE GROUP	MIL-STD-883 METHOD	GROUP A SUBGROUPS	READ AND RECORD
itial Test (Pre Burn-In)	100% 5004	1, 7, 9	IDD, IOL5, IOH5A
terim Test 1 (Post Burn-In)	100% 5004	1, 7, 9	IDD, IOL5, IOH5A
terim Test 2 (Post Burn-In)	100% 5004	1, 7, 9	IDD, IOL5, IOH5A
PDA (Note 1)	100% 5004	1, 7, 9, Deltas	
terim Test 3 (Post Burn-In)	100% 5004	1, 7, 9	IDD, IOL5, IOH5A

TABLE 6. APPLICABLE SUBGROUPS

CONFORMANCE GROUP		MIL-STD-883 METHOD	GROUP A SUBGROUPS	READ AND RECORD
PDA (Note 1)		100% 5004	1, 7, 9, Deltas	
ial Test		100% 5004	2, 3, 8A, 8B, 10, 11	
oup A		Sample 5005	1, 2, 3, 7, 8A, 8B, 9, 10, 11	
oup B	Subgroup B-5	Sample 5005	1, 2, 3, 7, 8A, 8B, 9, 10, 11, Deltas	Subgroups 1, 2, 3, 9, 10, 11
	Subgroup B-6	Sample 5005	1, 7, 9	
oup D		Sample 5005	1, 2, 3, 8A, 8B, 9	Subgroups 1, 2 3

TE: 1. 5% Parameteric, 3% Functional; Cumulative for Static 1 and 2.

TABLE 7. TOTAL DOSE IRRADIATION

CONFORMANCE GROUPS	MIL-STD-883 METHOD	TEST		READ AND RECORD	
		PRE-IRRAD	POST-IRRAD	PRE-IRRAD	POST-IRRAD
oup E Subgroup 2	5005	1, 7, 9	Table 4	1, 9	Table 4

TABLE 8. BURN-IN AND IRRADIATION TEST CONNECTIONS

FUNCTION	OPEN	GROUND	VDD	9V ± -0.5V	OSCILLATOR	
					50kHz	25kHz
atic Burn-In 1 ote 1)	4 - 7, 9 - 14	1 - 3, 8, 15	16			
atic Burn-In 2 ote 1)	4 - 7, 9 - 14	8	1 - 3, 15, 16			
namic Burn- (Note 1)	-	8	1, 15, 16	4 - 7, 9 - 14	3	2
adiation ote 2)	4 - 7, 9 - 14	8	1 - 3, 15, 16			

TES:

Each pin except VDD and GND will have a series resistor of 10K± 5%, VDD = 18V ± 0.5V

Each pin except VDD and GND will have a series resistor of 47K± 5%; Group E, Subgroup 2, sample size is 4 dice/wafer, 0 failures, VDD = 10V ± 0.5V

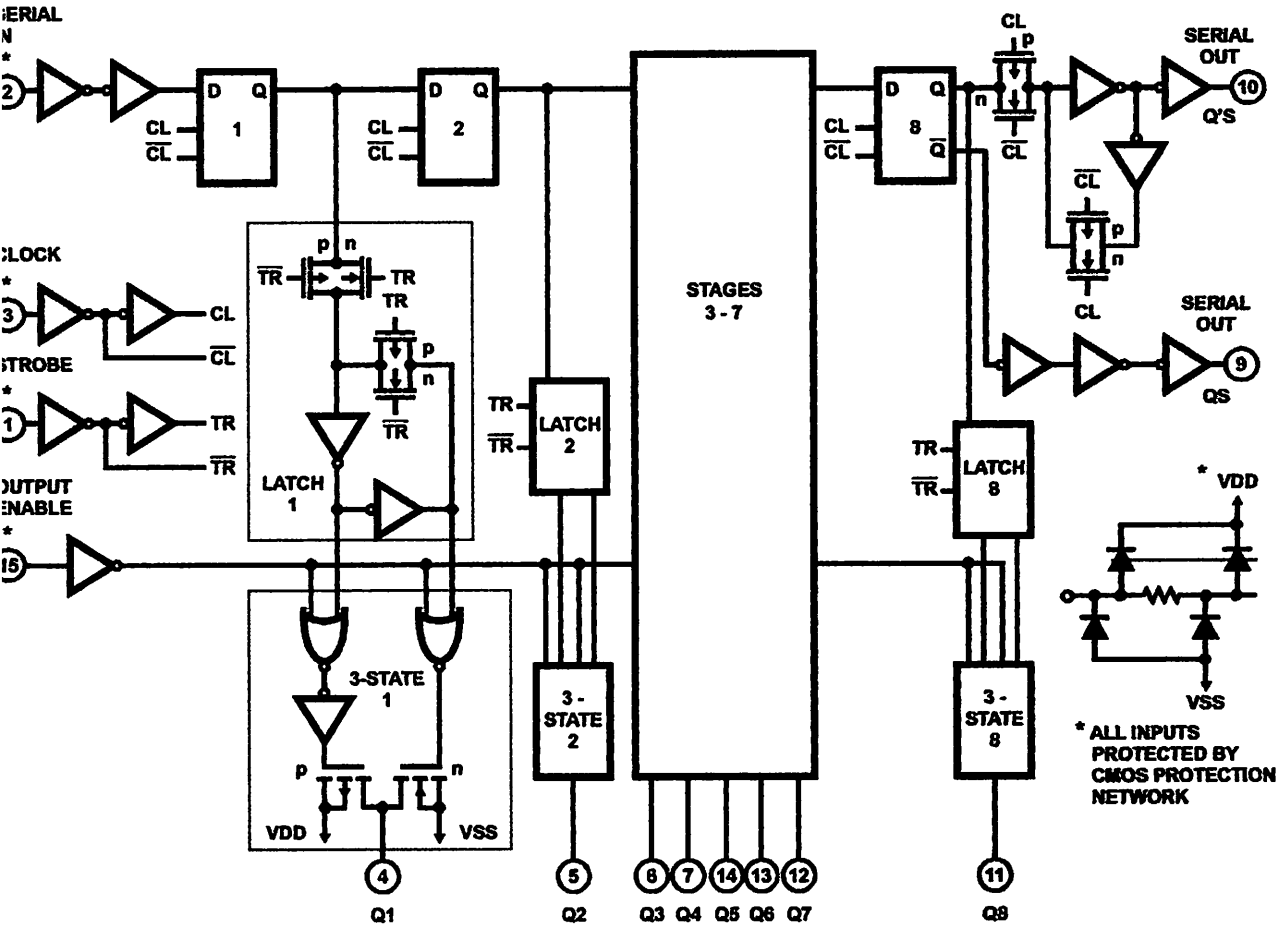


FIGURE 1. LOGIC DIAGRAM

TRUTH TABLE

CLΔ	OUTPUT ENABLE	STROBE	DATA	PARALLEL OUTPUTS		SERIAL OUTPUTS	
				Q1	QN	QS*	Q'S
↑	0	X	X	OC	OC	Q7	NC
↓	0	X	X	OC	OC	NC	Q7
↑	1	0	X	NC	NC	Q7	NC
↑	1	1	0	0	QN-1	Q7	NC
↑	1	1	1	1	QN-1	Q7	NC
↓	1	1	1	NC	NC	NC	Q7

Δ = Level Change

X = Don't Care

NC = No Change

OC = Open Circuit

Logic 1 = High

Logic 0 = Low

* At the positive clock edge information in the 7th shift register stage is transferred to the 8th register stage and the QS output

Typical Performance Characteristics

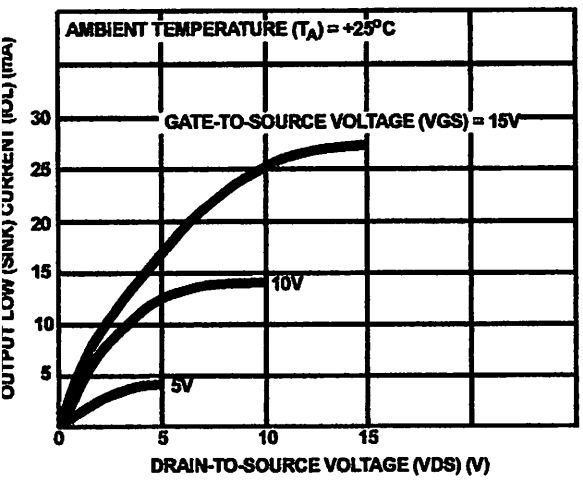


FIGURE 2. TYPICAL OUTPUT LOW (SINK) CURRENT TRANSFER CHARACTERISTICS

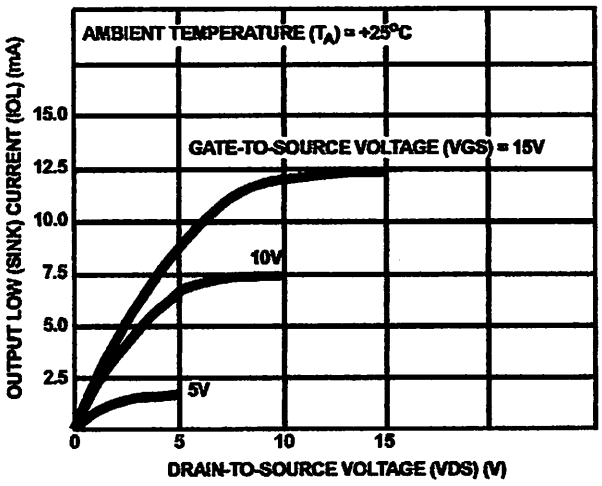


FIGURE 3. MINIMUM OUTPUT LOW (SINK) CURRENT CHARACTERISTICS

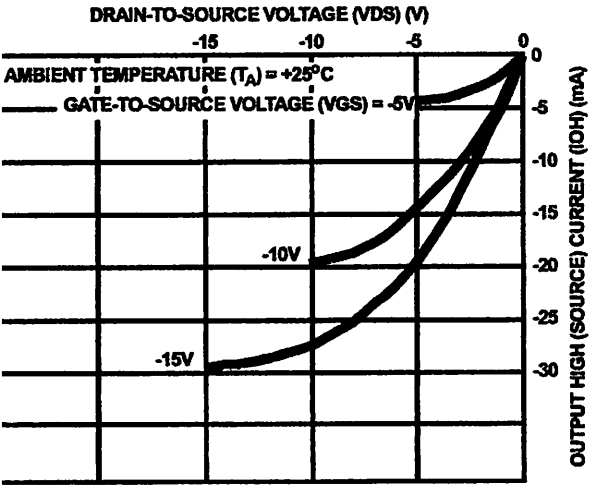


FIGURE 4. TYPICAL OUTPUT HIGH (SOURCE) CURRENT CHARACTERISTICS

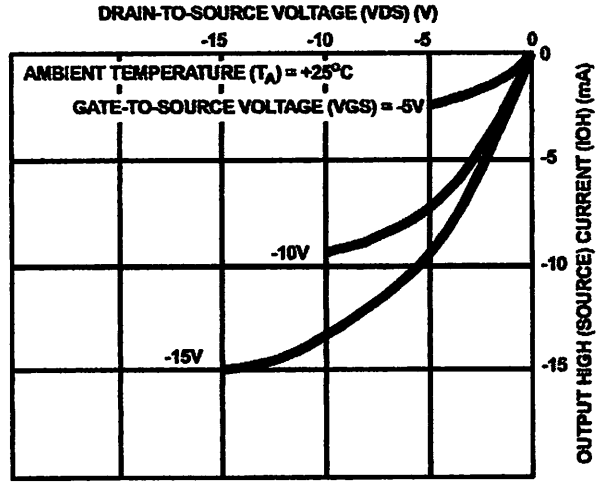


FIGURE 5. MINIMUM OUTPUT HIGH (SOURCE) CURRENT CHARACTERISTICS

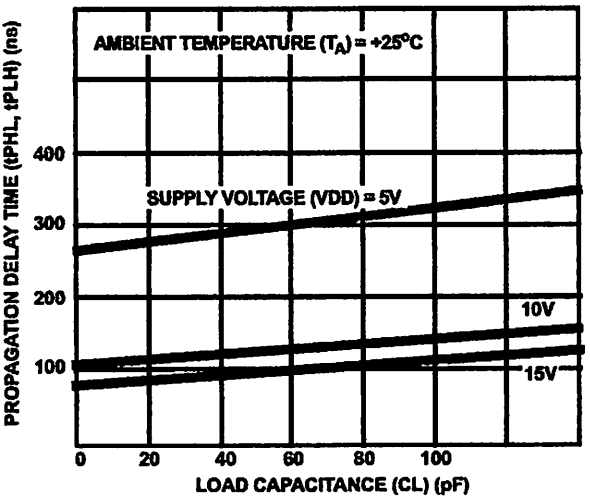


FIGURE 6. CLOCK-TO-SERIAL OUTPUT QS PROPAGATION DELAY vs CL

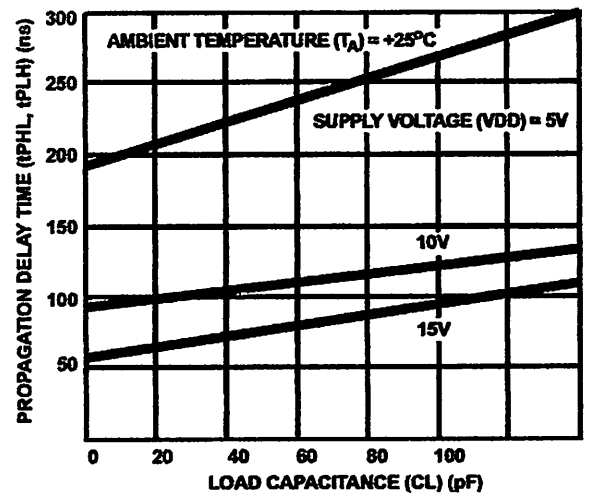
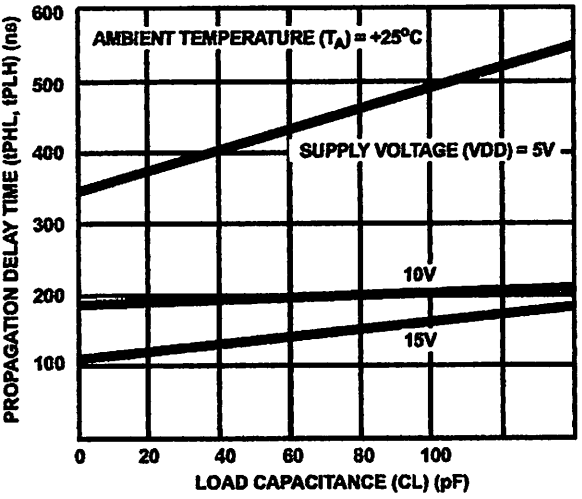


FIGURE 7. CLOCK-TO-SERIAL OUTPUT Q'S PROPAGATION DELAY vs CL

ypical Performance Characteristics (Continued)



IGURE 8. CLOCK-TO-PARALLEL OUTPUT PROPAGATION DELAY vs CL

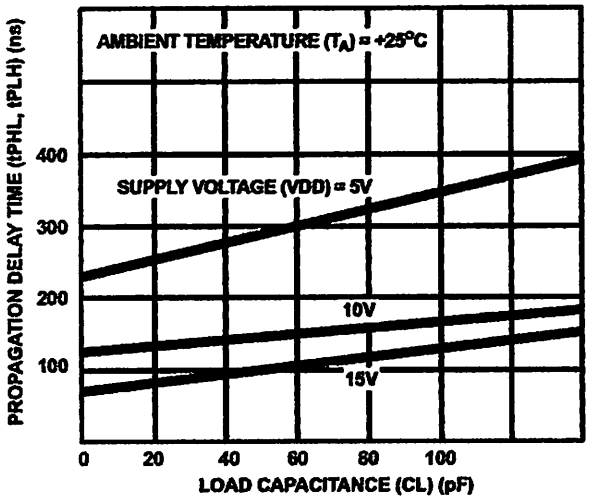
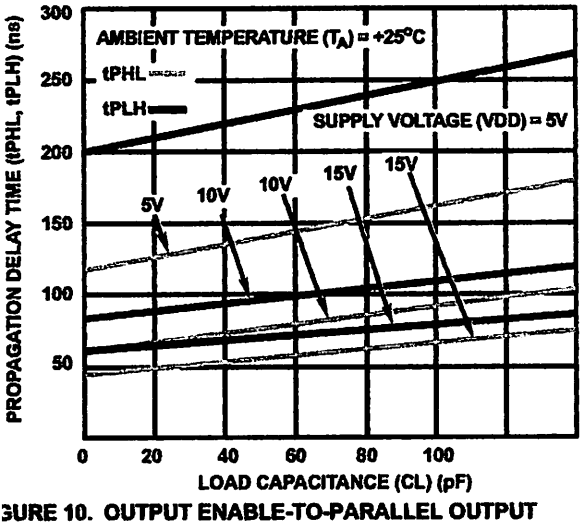


FIGURE 9. STROBE-TO-PARALLEL OUTPUT PROPAGATION DELAY vs CL



GURE 10. OUTPUT ENABLE-TO-PARALLEL OUTPUT PROPAGATION DELAY vs CL

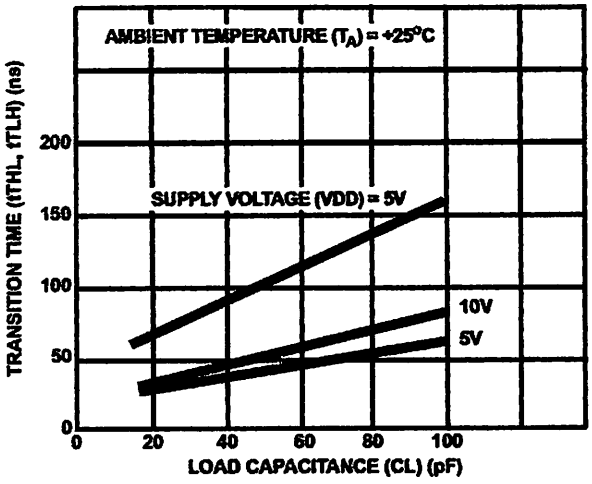


FIGURE 11. TYPICAL TRANSITION TIME vs LOAD CAPACITANCE

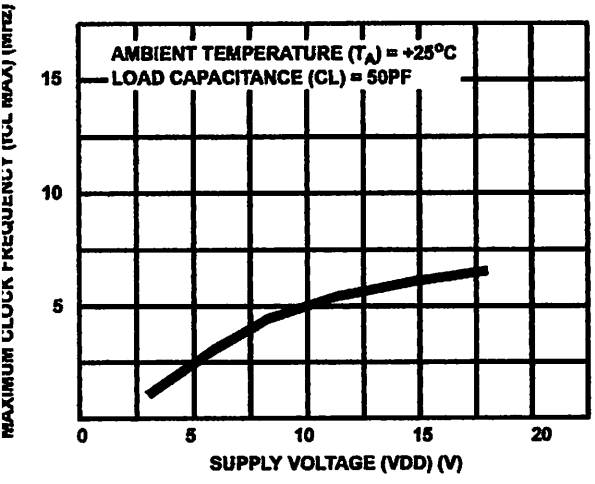


FIGURE 12. TYPICAL MAXIMUM-CLOCK-FREQUENCY vs SUPPLY VOLTAGE

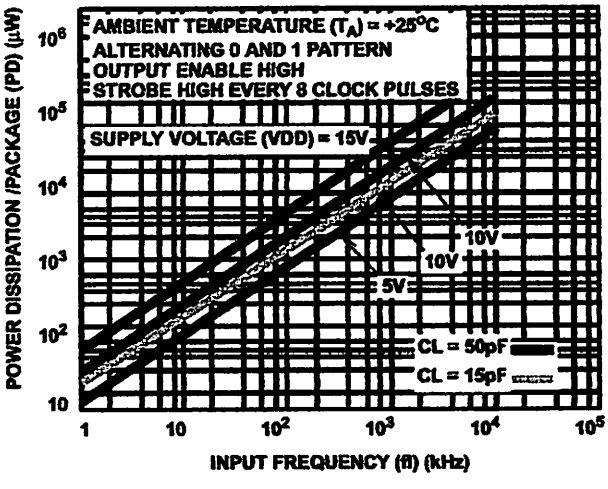


FIGURE 13. DYNAMIC POWER DISSIPATION vs INPUT CLOCK FREQUENCY

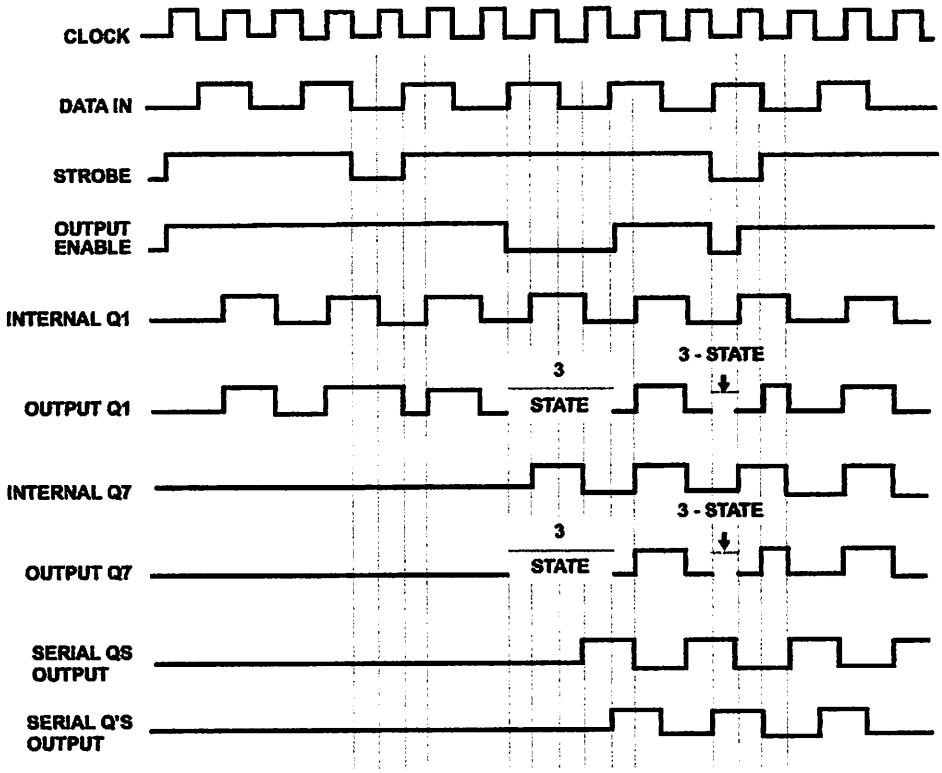


FIGURE 14. TIMING DIAGRAM

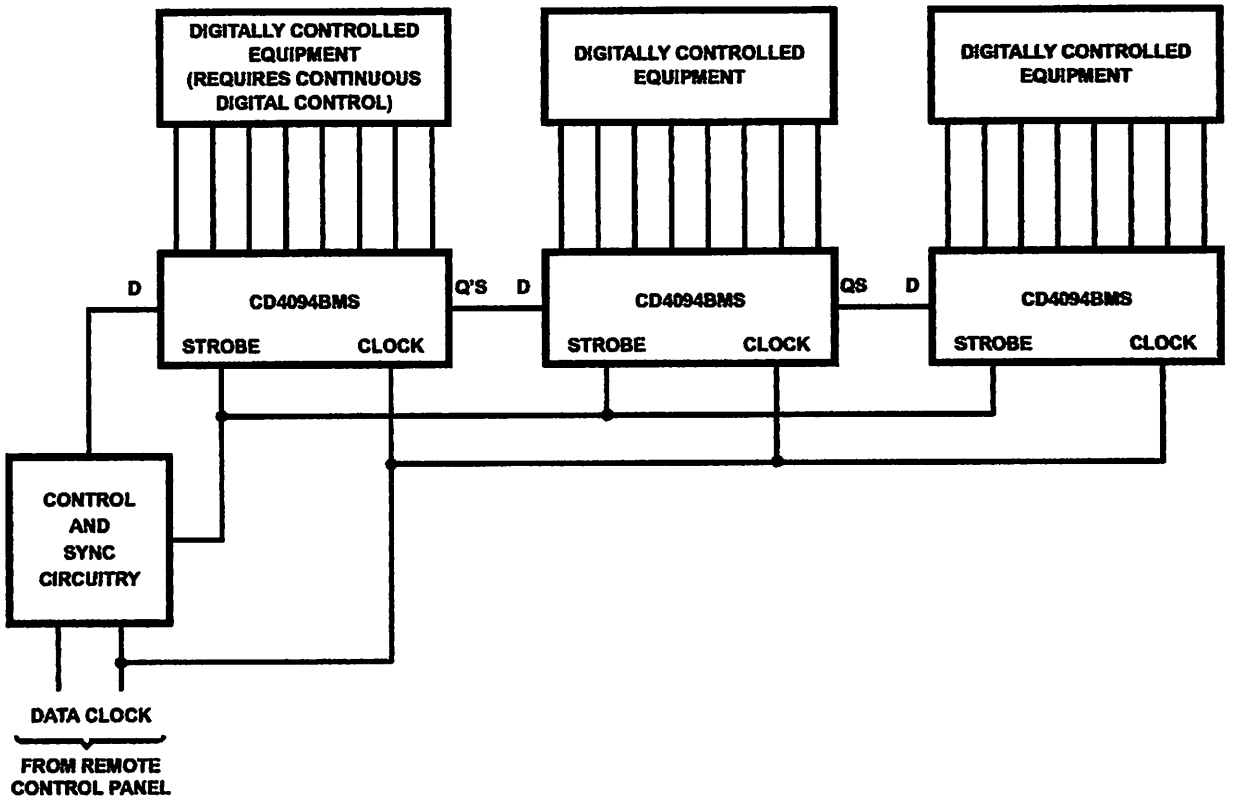
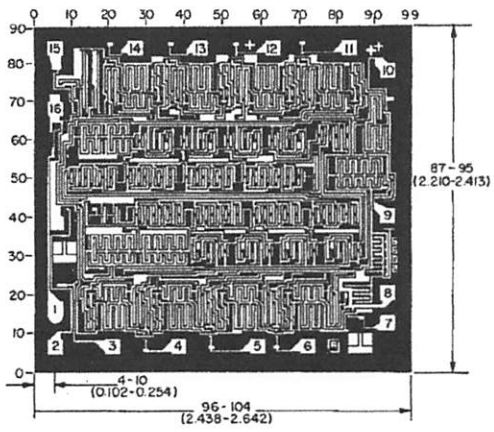


FIGURE 15. REMOTE CONTROL HOLDING REGISTER

hip Dimensions and Pad Layout



Dimensions in parenthesis are in millimeters and are derived from the basic inch dimensions as indicated. Grid graduations are in mils (10^{-3} inch).

METALLIZATION: Thickness: 11kÅ – 14kÅ, AL.

PASSIVATION: 10.4kÅ - 15.6kÅ, Silane

BOND PADS: 0.004 inches X 0.004 inches MIN

DIE THICKNESS: 0.0198 inches - 0.0218 inches

```
#include <c:\Gaza04X\FileH\reg51.h>
#include <c:\Gaza04X\FileH\DelayW.h>
#include <c:\Gaza04X\FileH\math.h>

sbit datc = P2^1;
sbit clkc = P2^0;
sbit strb = P2^2;

sbit jrk  = P3^0;
sbit tbl  = P3^2;
sbit flow = P3^3;
sbit cs   = P3^6;
sbit wr   = P3^7;
sbit bz   = P3^5;

sfr ad = 0x80;
unsigned char aa,a,bsn1,bsn2,bsn3,pjr1,pjr2,pjr3,pjr4;
unsigned char fl1,fl2,jr1,jr2,jr3,jr4,jr5,jr6,jr7;

unsigned int  bsn,bsnold,jr,pjr,fl,i,j,k;
unsigned int  jrold;

#include <c:\Gaza04X\FileH\7segadi.h>

main(){
     cs = 0;
     wr = 0;
     delayMSEC(10);
     bsn = (ad-4)*2;
     if (bsn >= 400) bsn = 400;
     if (bsn <= 1) bsn = 0;
     delayMSEC(10);
     cs = 1;
     wr = 1;

     while (1){
        for (j=0;j !=25;j++){
          cs = 0;
          wr = 0;
          delayMSEC(10);
          bsnold = (ad-4)*2;
          if (bsnold >= bsn) bsn = bsnold;
          if (bsn >= 400) bsn = 400;
          if (bsn <= 1) bsn = 0;
```

```
        delayMSEC(10);
        cs = 1;
        wr = 1;
        pjr = bsn*10;
        //fl++;
        for (k=0;k !=600;k++){
           if (jrk == 0){
              while (!jrk);
              jrold++;
              jr = jrold*0.16;
           }
           if (flow == 1){
              while (flow);
              fl++;
              i++;
           }
        }
        if (tbl == 1){
          bsn = 0;
          bsn = i*1.25/100;
          //pjr = i;
          tamp();
          while(tbl);
        }
        tamp();
        if (bsn <= 50) bz = 0;
        if (bsn >= 51) bz = 1;

      }
      bsn = 0;

   }
}
```