TUGAS AKHIR

PERENCANAAN DAN PEMBUATAN SCORE BOARD UNTUK BULU TANGKIS DENGAN MENGGUNAKAN REMOTE CONTROL BERBASIS MIKROKONTROLLER AT89C51

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KONSENTRASI TEKNIK ENERGI LISTRIK
JURUSAN TEKNIK ELEKTRO DIPLOMA III
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LEMBAR PERSETUJUAN

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TUGAS AKHIR

Diajukan sebagai Salah satu syarat Untuk memperoleh Gelar Diploma Tiga (DIII)
Pada Jurusan Elektro Studi Energi Listrik

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Penulis

ABSTRAKSI

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PERENCANAAN DAN PEMBUATAN SCORE BOARD UNTUK BULU TANGKIS DENGAN MENGGUNAKAN REMOTE CONTROL BERBASIS MIKROKONTROLLER AT89C51

Score Board adalah satu dari peralatan elektro yang berguna di dalam cabang Olah Raga. Khususnya dalam Bulu Tangkis, score board dapat menampilkan score atau nilai, pindah bola (service) dan set kemenangan dalam tiap pertandingan.

Dalam Perancangan alat Score Board Bulu Tangkis perlu adanya Rangkaian Pengontrol yang terdiri dari Rangkaian Remote Receiver, MCU, Driver Seven Segment dan Rangkaian Display Led yang menggunakan IC 74LS164 sebagai sift register dan ULN 2004 sebagai penguat led.

Pengujian perlu dilakukan didalam pembuatan Score Board tersebut, dengan cara memeriksa setiap komponen sudah berfungsi dengan baik atau belum, seperti pengujian Seven Segment yang akan aktif dalam kondisi low, pengujian inputan dan outputan Display Led dalam kondisi menyala atau mati dan juga jarak tempuh Remote Control dalam berbagai kondisi respon.

Kata Kunci : *Led, ULN 2004, 74LS164, Seven Segment*

DAFTAR ISI

DAFTAR TABEL

BAB I

PENDAHULUAN

1.1. Latar Belakang

Dalam perkembangan di dunia olah raga yang semakin pesat sekarang ini, banyak dibutuhkan peralatan yang dapat digunakan secara maksimal sesuai dengan kebutuhan. Oleh karena itu, dibutuhkan suatu peralatan mesin yang sudah ada dan dapat mempermudah kerja maupun proses kerjanya. Sebagai contoh adalah penggunaan dan pemanfaatan teknologi tepat guna, khususnya pada sektor olah raga bulu tangkis.

Perguruan tinggi, khususnya di bidang Elektro diharapkan mampu mengembangkan ketrampilan agar dapat meringankan beban manusia dalam menghadapi persaingan yang sangat ketat ini. Oleh karena itu, sangatlah tepat jika digalakkan suatu *device* elektro yang dapat mempermudah kinerja manusia untuk mendukung suatu perlombaan/ kejuaraan atau sebuah pertandingan biasa. Dalam hal ini, penulis akan mencoba merancang dan membuat sebuah alat yang bisa membantu para wasit untuk memimpin, sekaligus sebagai pengontrol *score*/ nilai pada olah raga bulu tangkis.

Penulis sangat terinspirasi untuk menciptakan produk yang bermanfaat bagi masyarakat, schingga dapat menyumbang pemikiran yang merupakan tantangan dalam dunia olah raga dan pendidikan.

1.2. Rumusan Masalah

Adapun rumusan masalah yang dibahas didalam pembuatan alat ini adalah sebagai berikut :

1. Bagaimana merencanakan dan membuat alat *Score Board* untuk Bulu Tangkis dengan menggunakan *Remote Control* Berbasis Mikrokontroller *AT89C51* ?
2. Bagaimana menampilkan program ke *Display Led* dan *Seven Segment* ?

1.3. Tujuan

Perencanaan dan Pembuatan *Score Board* untuk Bulu Tangkis dengan *Remote Control* Berbasis Mikrokontroller *AT89C51* yang ditampilkan ke *Display Led* dan *Seven Segment*.

1.4. Batasan Masalah

Agar permasalahan tidak terlalu luas, maka penulis membatasi hanya pada hal-hal berikut :

1. Jumlah perhitungan *score* dalam alat ini, dibatasi maksimal 2 (dua) digit, yaitu 99.
2. *Display* dalam alat ini hanya menampilkan informasi *score*, set kemenangan dan infomasi pindah bola saja.
3. Proses penambahan nilai/*score* masih dilakukan secara manual, dengan menggunakan *Remote Control*.
4. Menggunakan *Remote Sony* tipe Trinitron RM-827S.

1.5. Sistematika Penulisan Laporan

Sistematika pembahasan dalam proposal ini terdiri dari pokok pembahasan yang saling berkaitan antara satu dengan yang lainnya, yaitu :

BAB I : Merupakan pendahuluan yang berisikan tentang latar belakang, tujuan permasalahan, batasan masalah dan sistimatika pembahasan.

BAB II : Merupakan landasan teori dasar yang menunjang dalam perencanaan sistem kontrol ini.

BAB III : Merupakan pembahasan masalah yang berisikan perencanaan konstruksi alat dan perencanaan kontrol dari alat yang dibuat.

BAB IV : Pengujian Alat

BAB V : Merupakan bab penutup yang berisikan kesimpulan dan saran-saran.

1.6. Manfaat Alat

Alat ini dapat meminimalisasi kesalahan di dalam penghitungan score, proses kerja wasit dan menjaga konsentrasi pemain.

BAB II

TEORI DASAR

2.1. Mikrocontroller AT89C51

2.1.1. Hubungan dengan MCS-51

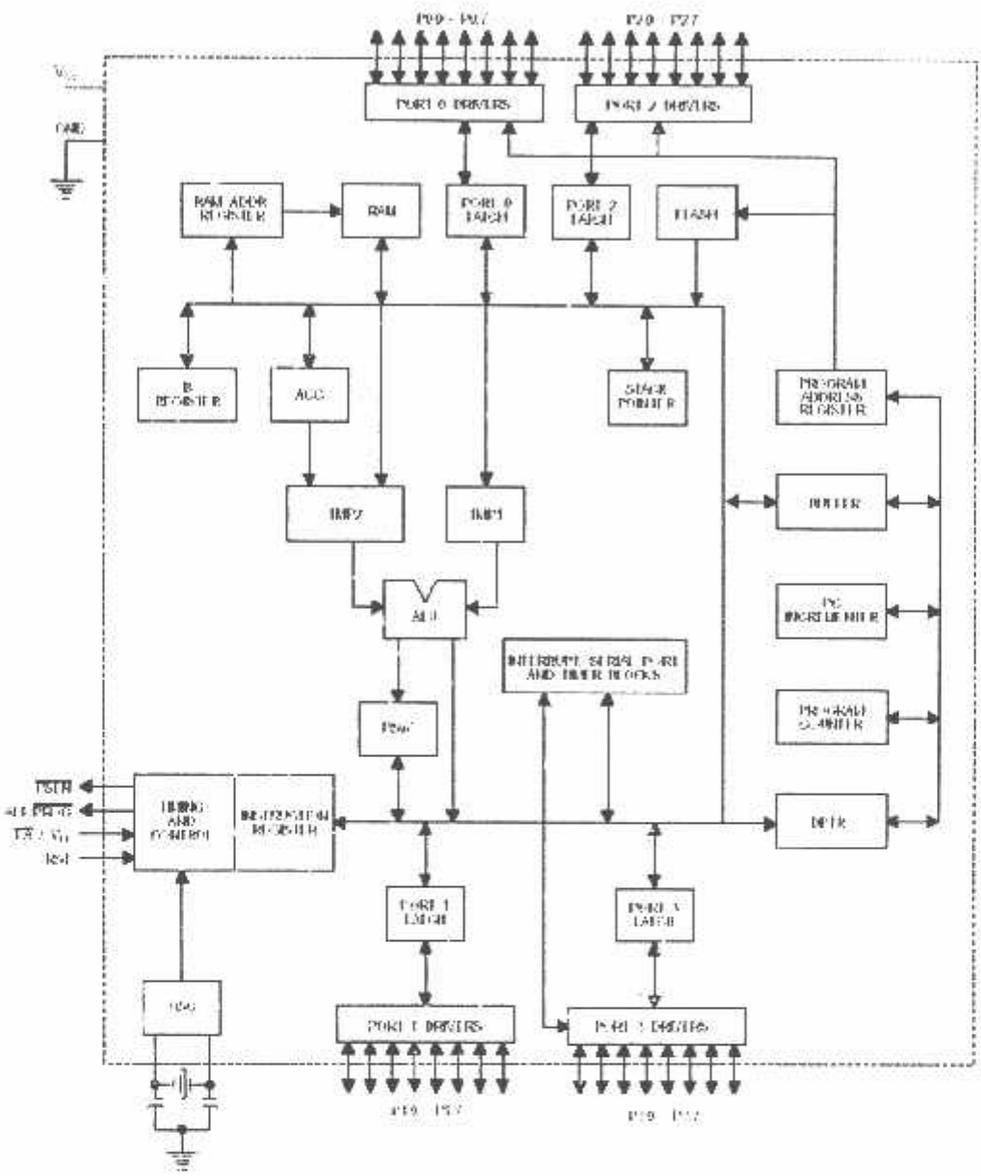
MCS-51 merupakan keluarga mikrokontroller 8 *bit* seperti ditunjukkan dalam tabel 1 berikut ini, yang kesemuanya mempunyai arsitektur MCS-51:

Tabel 2.1. MCS-51 *Family*[1]

Device	Internal Memori Program	Internal Memori Data	Timer/Even Counter	Interupt
8052AH	8K X 8 ROM	256 X 8 RAM	3 X 16 Bit	6
8051AH	4K X 8 ROM	128 X 8 RAM	2 X 16 Bit	5
8051	4K X 8 ROM	128 X 8 RAM	2 X 16 Bit	5
8032AH	NONE	256 X 8 RAM	3 X 16 Bit	6
8031AH	NONE	128 X 8 RAM	2 X 16 Bit	5
8031	4K X 8 EPROM	128 X 8 RAM	2 X 16 Bit	5
8751AH	4K X 8 EPROM	128 X 8 RAM	2 X 16 Bit	5
8751H12	4K X 8 EPROM	128 X 8 RAM	2 X 16 Bit	5
8751H88	4K X 8 EPROM	128 X 8 RAM	2 X 16 Bit	5
AT89C51	4K X 8 EPROM	128 X 8 RAM	2 X 16 Bit	5

Mikrokontroller *AT89C51* merupakan salah satu dari keluarga MCS-51 yang terbuat dari *CMOS* 8-*Bit* dengan 4K *Bytes Flash PEROM* dan merupakan produksi dari *ATMEL*. Dibandingkan dengan Mikrokontroller yang lain dalam *MCS*-51, Mikrokontroller *AT89C51* memiliki perbedaan yang terletak pada memori progam yang

digunakan yaitu menggunakan *EEPROM* yang merupakan versi *internal* dari 8051 yang memori progam *internalnya* dapat di progam dan di hapus secara elektrik. Sehingga di dalam penggunaanya, EEPROM lebih *fleksibel* dibandingkan dengai yang lain (PROM dan EPROM) dan harganya relatif murah. Secara umum arsitektur MCS-51 di tunjukkan pada gambar 2.1 berikut ini



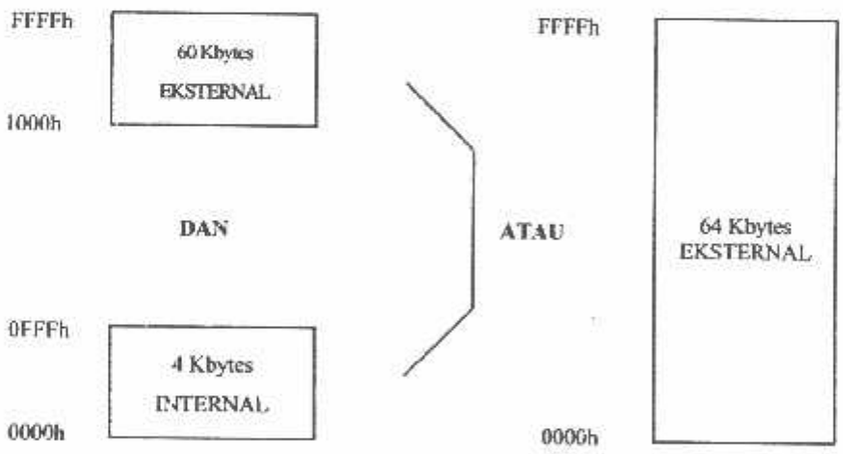
Gambar 2.1. Blok Diagram MCS -51 [3]

2.1.2. Organisasi Memori MCU AT89C51

MCS -51 mempunyai *space addres* yang terpisah antara progam memori (ROM) dan data memori (RAM). Pemisahan dilakukan secara logika, sehingga *CPU* dapat menggunakan lokasi *addres* untuk progam memori dan data memori.

2.1.3. Progam Memori

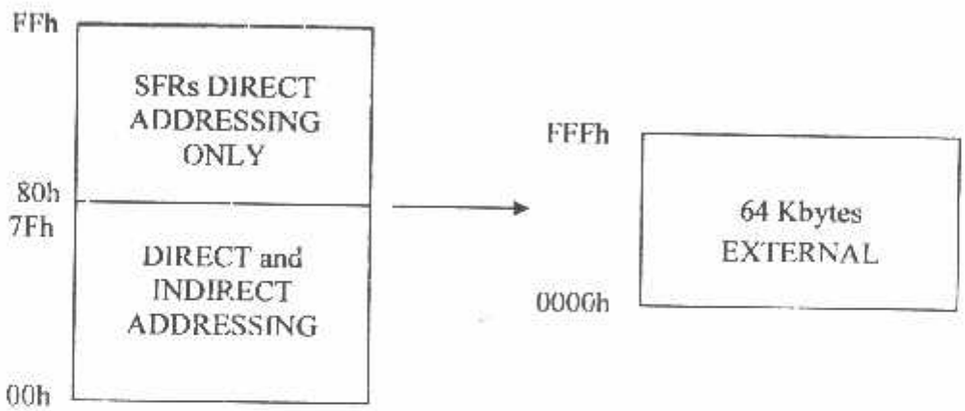
Progam memori menggunakan lokasi *addres* sepanjang 64K *Byte* dengan rician 4 K *Byte* memori *internal* (Addres 0000_H – $0FFF_H$) di tambah 60 *Kbyte* dari memori *eksternal*, atau dapat juga menggunakan 64 *Kbyte* memori *eksternal* penuh. *Addres* progam memori diatas $0FFF_H$ yang melebihi kapasitas *ROM internal* akan menyebabkan MCU AT89C51 secara otomatis akan mengambil *byte* kode dari progam memori *eksternal*.



Gambar 2.2. Blok Progam Memori[1]

2.1.4. Data Memori

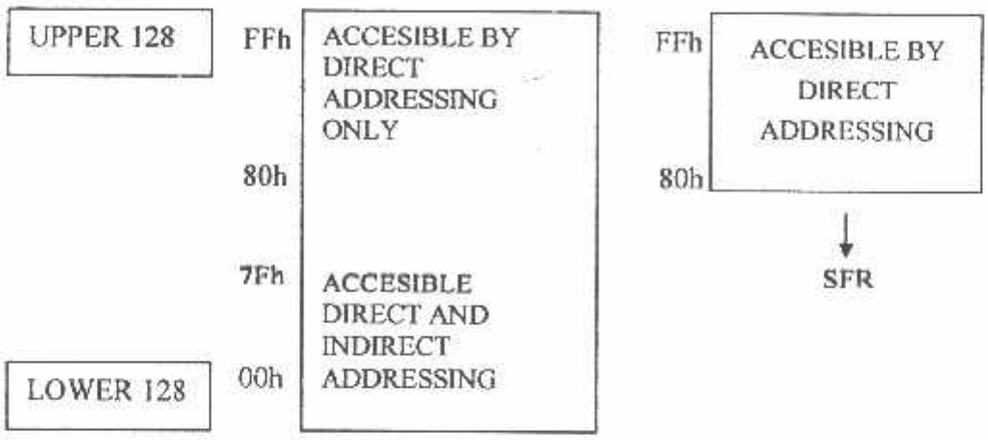
Data memori data yang dikenal dengan *RAM* (Random Acces Memori) menggunakan lokasi *addres* sepanjang 60 *Kbyte* yang didapat dari memori data *eksternal*. Untuk lebar *RAM internal* mempunyai 128 *byte* ditambah sejumlah *Register* Fungsi khusus atau *Special Function Register* (*SFRs*). *Register* ini menggunakan *addres* 80_H – FF_H, namun tidak semua *addres* ini digunakan untuk *SFRs*.



Gambar 2.3 Blok Diagram Data Memori [1]

2.1.5. Lokasi Pengalamatan (Addressing) Langsung Dan Tidak Langsung

Ruang memori data *internal* terbagi menjadi 3 *blok* seperti gambar dibawah ini :



Gambar 2.4. Ruang Memory Data Internal [1]

Sebanyak 128 *byte* bawah (*lower* 128) dari *RAM internal* dapat *diakses* baik dengan cara pengalamatan langsung maupun tidak langsung dan lokasi tersebut dibagi lagi menjadi 3 bagian, antara lain:

a. Register Bank 0-3

Lokasi *addres register bank* dimulai dari alamat 00_H-$1F_H$ atau sebanyak 32 *byte*. *Register* bank ini terdiri dari 4 *bit register*, masing-masing *register* bank berisi 8 *byte (byte 0-byte 7)* yang dapat dipilih melalui program status *word register* pada *software*. Namun pada saat *reset MCU*, program akan langsung diarahkan ke *register bank* 0.

b. Bit Addressable Area

Lokasi *addres*-nya dimulai dari alamat $20_H - 2F_H$ atau sebanyak 16 b*yte*. Masing-masing dari 16 byte (128 *bit*) lokasi ini dapat dialamati secara langsung yaitu dari

00_H-$7F_H$. *Bit-bit* ini dapat ditunjukkan dengan dua cara, yaitu yang pertama adalah dengan menunjukkan *addres*-nya dari alamat 00_H-$7F_H$, sedangkan cara kedua adalah dengan *referensi* ke alamat 20_H-$2F_H$. Dengan demikian *bit* ke 0 sampai *bit* ke 7 juga direferensikan sebagai *bit* 20.0 sampai 20.7, begitu seterusnya. Masing-masing dari 16 *byte* dapat juga dialamatkan sebagai sebagai sebuah *byte*.

c. **Scratch Pad Area**

Lokasi *addres*-nya dimulai dari alamat 30_H – $7F_H$ atau sebanyak 80 byte yang dapat digunakan sebagai data bagi *RAM*.

Pada 128 *byte* atas (upper 128) ditempati oleh suatu *register* yang memiliki fungsi khusus yang disebut dengan *Spesial Function Register* (*SFRs*) dengan ruang alamat 80_H – FF_H. Berikut ini adalah bagian dari *SFRs* :

1. **Accumulator**

Register ini digunakan untuk operasi perkalian dan pembagian.

2. **Program Status Word**

Register ini meliputi *bit-bit* : *CY* (*Carry*), *AC* (*Auxilliry* carry), *FO* (*sebagai* flag), *RS0* dan *RS1* (untuk pemilihan *register bank*), *OV* (Over *Flow*), dan *parity flag*.

3. **Stack Pointer**

Stack pointer adalah suatu *register* yang digunakan untuk petunjuk alamat yang berguna apabila *sub routine* digunakan pada program utama.

4. **Data Pointer High (DPH)Dan Data Pointer Low (DPL)**

DPH dan *DPL* adalah 2 buah *register* 8 *bit* yang digunakan untuk mengontrol *DPTR*, yaitu suatu *register* untuk pengalamatan tidak langsung. Fungsi *register* ini adalah untuk mengakses memori program baik *internal* maupun *eksternal*, juga untuk data *eksternal*.

5. **Port 0, Port 1, Port 2, Dan Port 3**

Pada keluarga 8051 masing-masing *port* dapat dialamati baik secara *bit* ataupun *byte*. Masing-masing *port* merupakan *port bidirectional* yang artinya dapat berfungsi sebagai *input* ataupun *output*. *Port* 0 dan *port* 2 digunakan sebagai pengalamatan memori dari luar, *port* 1 digunakan sebagai *port* I/O dari mikrokontroller, sedangkan *port* 3 berisi sinyal-sinyal kontrol seperti *interupt*, *serial*, *WR*, dan *RD*.

6. **Interupt Priority Register (IP)**

Merupakan *register* yang berisi *bit-bit* untuk mengaktifkan prioritas dari suatu *interupt* yang ada pada mikrokontroller pada taraf yang diinginkan.

7. **Interupt Enable Register (IE)**

Merupakan *register* yang berisi *bit-bit* untuk mengaktifkan maupun mematikan sumber *interupt*.

8. **Timer / Counter Register (TCON)**

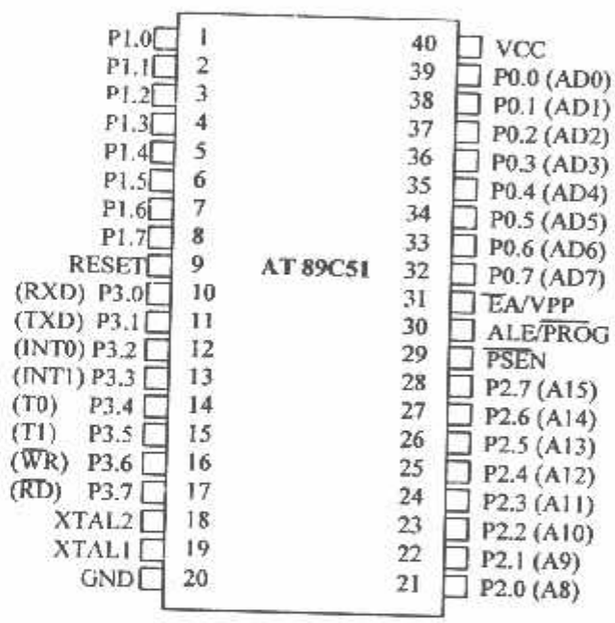
Register yang berisi *bit-bit*, berfungsi untuk memulai ataupun menghentikan pewaktu / pencacah.

9. **Serial Control Buffer (SBUF)**

Register ini digunakan untuk menampung data dari masukan(*SBUF-IN*) ataupun keluaran (*SBUF-OUT*) dari serial *port*.

2.1.6. Konfigurasi Pin-Pin Pada MCU AT89C51

Adapun fungsi dari masing-masing pin pada MCU AT89C51 dapat dilihat dari konfigurasi dan bentuk fisik berdasarkan gambar dibawah ini:



Gambar 2.5. Konfigurasi Pin MCU AT89C51 [1]

a. **VCC**

Merupakan *pin* catu daya dengan *level* tegangan +5 *volt*.

b. **GND**

Pin Ground.

c. **Port 0**

Port 0 merupakan Port I/O dengan 8 *bit directional* yang tidak mempunyai *pull-up internal*. Sebagai sebuah *port* keluaran, maka setiap *pin* dapat mengendalikan 8 beban *TTL*. Selain itu, *port* 0 juga dapat digunakan untuk *memultipleks addres bus* rendah dan data *memori* dengan mengunakan *pull-up internal*. *Port* 0 juga menerima kode mesin (dalam *byte*) selama pemrograman *EEPROM* dan mengeluarkan kode mesin selama program verifikasi dari *EEPROM*. Selama program *verifikasi* ini dibutuhkan *pull-up eksternal*. Pada *port* ini berlaku ketetapan yang berbeda dengan *port-port* yang lainnya, yaitu apa bila digunakan sebagai keluaran maka harus diberikan tambahan *resistor pull-up*.

d. **Port 1**

Port 1 merupakan *port* I/O dengan 8 *bit bidirectional* yang mempunyai *pull-up internal*. *Buffer* keluaran dari *port* 1 dapat mengendalikan 4 beban *TTL*. *Pin-pin* dari port 1 dapat digunakan sebagai input jika *dipull-high* oleh *pull-up internal* dan jika *dipull-low internal*. *Port* 1 menerima *addres bus* rendah (dalam *byte*) selama pemrograman *EEPROM* dan selama program *verifikasi* dari *EEPROM*.

e. **Port 2**

Port 2 merupakan port I/O dengan 8 *bit bidirectional* yang mempuyai *pull-up internal*. *Buffer* keluaran dari *port* 2 dapat mengendalikan 4 beban *TTL*. *Pin-pin* dari *port* 2 dapat digunakan sebagai input jika *dipull-high* oleh *pull-up internal* dan jika *dipull-low* secara *eksternal*, maka akan menghasilkan arus *IIL* yang disebabkan adanya *pull-up internal*. Port ini mengeluarkan *addres bus* tinggi (dalam *byte*) selama mengambil dari program memori *eksternal* dan selama

mengakses kedata memori *eksternal* yang menggunakan *addres16 bit* dan dengan menggunakan *pull-up internal*.

Selama mengakses kedata memori *eksternal* yang menggunakan *addres* 8 *bit*, maka *port* 2 mengijinkan isi dari *port* 2 yang merupakan *register* fungsi khusus atau *Special Function Register (SFRs)*. Port 2 ini menerima *addres bus* tinggi (dalam bit) selama pemrograman EEPROM dan selama program verifikasi dari EEPROM.

f. **Port 3**

Port 3 merupakan *Port* I/O dengan 8 *bit bidirectional* yang mempunyai *pull-up internal*. *Buffer* keluaran dari *Port* 3 dapat mengendalikan 4 beban TTL dan menghasilkan arus IIL karena adanya *pull-up internal*. Fungsi lain dari port 3 seperti tertera pada tabel 2.2 berikut :

Tabel 2.2 Fungsi lain Port[1]

Port Pin	Alternative Function
P 3.0	RXD (Serial Input Port)
P 3.1	TXD (Serial Output Port)
P 3.2	INT0 (External Interrupt 0)
P 3.3	INT1 (External Interrupt 1)
P 3.4	T0 (Timer 0 External Input)
P 3.5	T1 (Timer 1 External Input)
P 3.6	WR (External Data Memory Write Strobe)
P 3.7	RD (External Data Memory Read Strobe)

g. **RST (Reset)**

Pin reset aktif *high*, jika pin ini aktif *high* selama dua *siklus* mesin ketika *osilator* bekerja akan *mereset* peralatan.

h. **ALE/PROG (Addres Latch Enable/Program)**

Pin *ALE* (*aktif high*) mengeluarkan *pulsa* output untuk *melacth* (menahan)*1byte* alamat rendah selama mengakses kememori *eksternal*. *ALE* dapat mengendalikan 8 beban TTL dan juga merupakan input pulsa program yang aktif rendah selama pemrograman *flash EPROM*. Pada operasi normal, *ALE* dikeluarkan pada suatu kecepatan yang *konstan* yaitu 1/16 dari *frekwensi osilator*, dan juga dapat digunakan untuk pewaktu/*timing* atau pemberian *clock*.

i. **PSEN (Program Strobe Enable)**

Pin ini aktif *low* yang merupakan *strobe* pembacaan keprogram memori *eksternal*.

j. **XTAL 1**

Pin input kepenguat *osilator* pembalik dan *input internal clock* untuk operasi *system*/rangkaian

k. **XTAL 2**

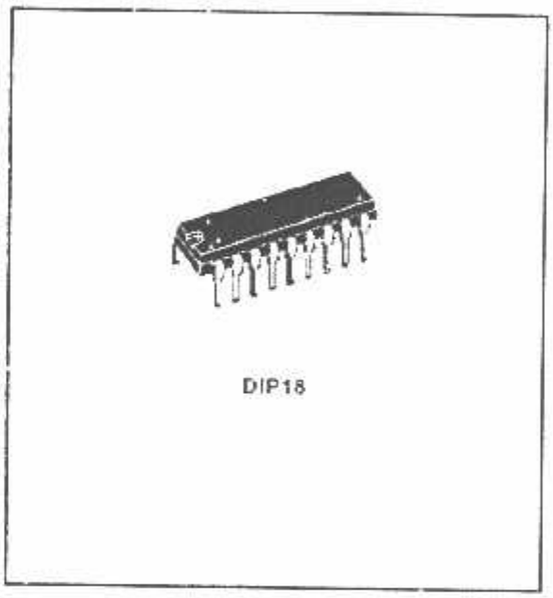
Pin *output* dari penguat *osilator* pembalik.

l. **EA/Vpp (External Acces/Program Supply Voltage)**

Pin EA harus di *hold* rendah secara *eksternal* atau dihubungkan ke *ground* agar AT89C51 dapat mengakses kode mesin dari program memori eksternal dengan lokasi *0000h* sampai *FFFFh*. Jika menggunakan *internal* program memori maka EA harus diberi *logic high*.

2.2. ULN 2004

Untuk rangkaian ULN 2004 sebagai driver led, dalam perancangan ini digunakan IC ULN 2004 dan sebagai sebagai kompenen utamanya, yang nantinya digunakan untuk mengaktifkan led. IC ULN 2004 diberikan logika tinggi dimana data sheet menyebutkan bahwa IC ULN 2004 dapat terpicu dengan tegangan 5 Volt dengan tegangan hubung.



Gambar 2.6. Gambar IC ULN 2004 [5]

2.3. Transformator

Transformator adalah suatu alat listrik yang dapat memindahkan dan mengubah energi listrik dari satu atau lebih rangkaian listrik yang lain, melalui suatu gandengan magnet dan berdasarkan *induksi elektromagnet*. *Transformator* digunakan secara luas, baik dalam bidang tenaga listrik maupun elektronika. Penggunaan *transformator* dalam sistem tenaga memungkinkan terpilihnya tegangan yang sesuai, dan *ekonomis* untuk tiap-tiap keperluan.

Dalam bidang elektronika, *transformator* digunakan antara lain sebagai gandengan *impedensi* antara sumber dan beban, untuk memisahkan satu rangkaian dari rangkaian lain dan membuat arus searah sambil tetap melakukan atau mengalirkan arus bolak balik antara rangkaian. Berdasarkan *frekuesi*, *tranformator* dapat dikelompokkan sebagai berikut :

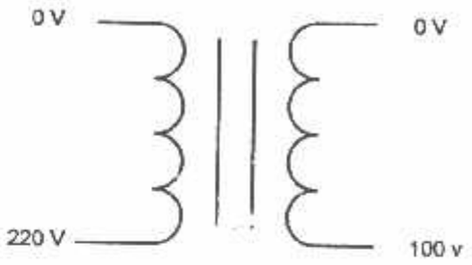
1. Frekuesi daya 50 – 60 c/s
2. Frekuensi pendengaran 50 c/s – 20 kc/s
3. Frekuensi radio diatas 30 kc/s

Dalam bidang tenaga listrik pemakaian transformator dikelompokkan menjadi :

1. Transformator daya
2. Transformator distribusi
3. transformator pengukuran yang terdiri atas tranfomator arus dan transormator tegangan.

Kerja transformator yang berdasarkan induksi *elektromagnet*, menghendaki adanya gandengan magnet antar rangkaian magnet antara rangkaian *primer* dan *sekunder*. Gandengan magnet inti besi tempat untuk melakukan *fluks* bersama.

Berdasarkan cara melilitkan kumparan pada inti, dikenal dua macam *tranformator*, yaitu tipe inti dan tipe cangkang.



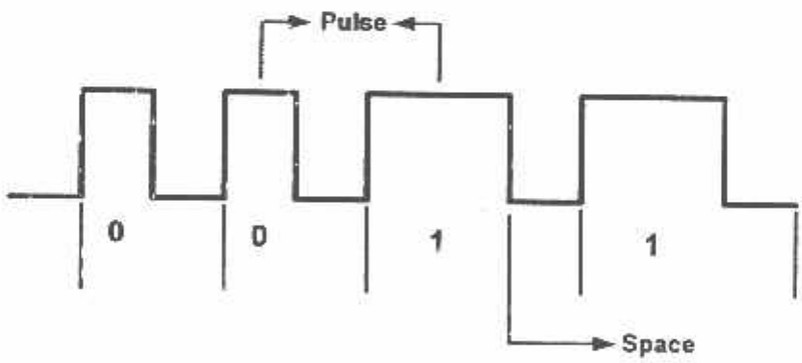
Gambar 2.7. Transformator Step down[11]

2.5. Remote Kontrol

Remote control *infra* merah menggunakan cahaya *infra* merah sebagai media dalam mengirimkan data ke penerima. Data yang dikirimkan berupa pulsa – pulsa cahaya dengan *modulasi frekwensi* 40 *Khz*. Sinyal yang dikirimkan berupa data – data *biner*. Untuk membentuk data – data *biner* tersebut, ada tiga metode yang digunakan yaitu pengubahan lebar pulsa, lebar jeda dan gabungan keduanya.

- *Pulse – Coded Signals*

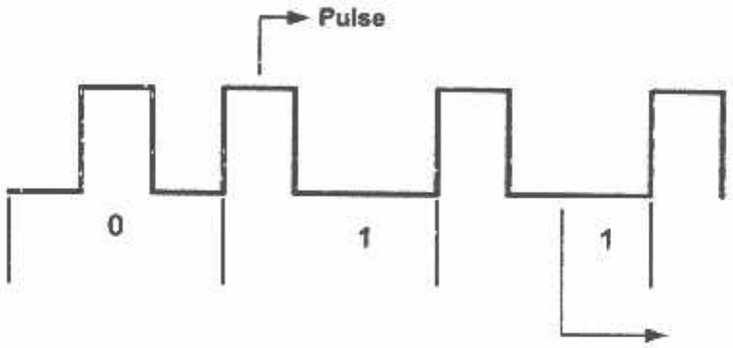
  Dalam mengirimkan kode, lebar jeda tetap yaitu t, sedangkan lebar pulsa adalah 2t, jika lebar pulsa dan lebar jeda adalah sama yaitu t, berarti yang dikirim adalah *bit* 0, jika lebar pulsa adalah 2t, dan lebar jeda adalah t, berarti yang dikirim adalah 1



Gambar 2.8.
Pengiriman kode dengan Type Pulse Coded Signals [8]

- *Space – Coded Signals*

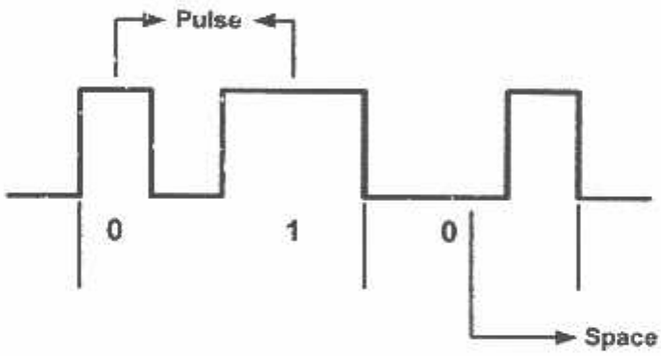
  Dalam mengirimkan *code remote control*, dilakukan dengan cara mengubah lebar jeda, sedangkan lebar pulsa tetap. Jika lebar pulsa dan lebar jeda asalah sama, yaitu t, berarti yang dikirim adalah 0. jika lebar jeda 3t, berarti data yang dikirim adalah 1.



Gambar 2.9.
Pengiriman kode dengan Type Space Coded Signals [8]

- *Shift – Code Signals*

  Tipe ini merupakan gabungan dari *tipe pulse* dan *space*, yaitu dalam mengirimkan *kode remote control*, dengan cara mengubah lebar pulsa dan lebar jeda. Jika lebar jeda adalah t, dan lebar pulsa adalh 2t, maka ini diartikan sebagai data 1. Jika lebar jeda adalah 2t dan lebar pulsa adalah t, maka ini diartikan sebagai data 0 (*low*)



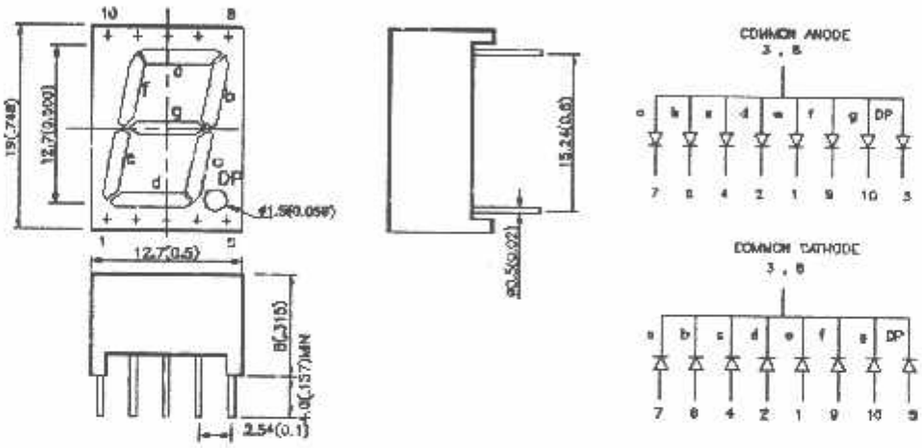
Gambar 2.10.
Pengiriman kode dengan Type Shift Coded Signals [8]

Sebelum kode dikirim, terlebih dahulu mengirimkan sinyal awal yang disebut sebagai header. Header adalah sinyal untuk mengaktifkan penerima. Header aelalu dikirimkan dengan lebar pulsa yang jauh, lebih panjang dari pada kode.

Setelah Header dikirimkan, baru kemudian kode remote control. Kode remote control dibagi menjadi 2 fungsi, yaitu fungsi pertama sebagai penunjuk alamat peralatan yang diaktifkan, fungsi kedua adalah sebagai command atau perintah untuk melaksanakan instruksi dari remote control.

2.6. Seven Segment

Bagian *display* adalah bagian yang berguna memberikan informasi hasil data *score* dari sebuah pertandingan bulu tangkis sehingga memudahkan para pemain, penonton dan wasit dengan melihat tampilan tersebut.Bagian ini terdiri dari beberapa blok yakni mikrokontroller AT89C51 sebagai pengendali utama, *seven segment* akan menampilkan huruf (tulisan) angka.



Gambar 2.11.
Seven Segment[9]

BAB III

PERENCANAAN ALAT

3.1. PENDAHULUAN

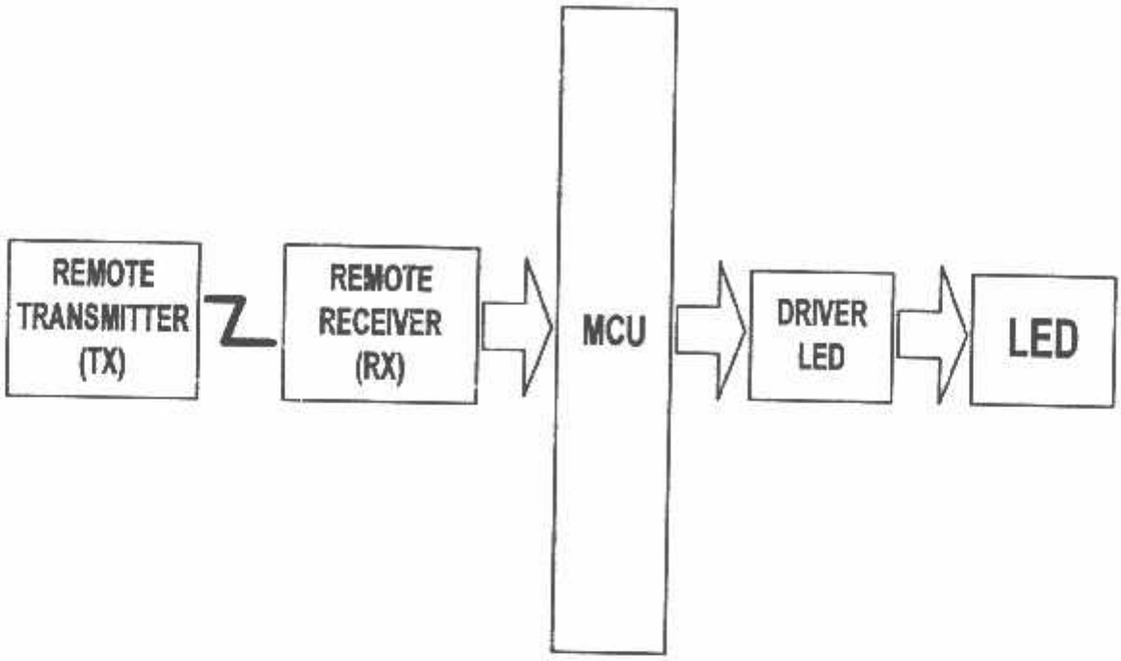
Dalam Bab ini akan dibahas pembuatan seluruh sistem perangkat yang ada pada alat Penyampaian Informasi *Score*, Pemenang *Set*, dan Pemegang *Servis* pada alat *Score Board* untuk olah raga Bulu Tangkis ini. Secara garis besar terdapat dua bagian perangkat yang ada yaitu:

1. Perencanaan perangkat keras
2. Perencanaan perangkat lunak

Pada perencanaan perangkat keras akan meliputi penjelasan dari perencanaan diagram blok sistem dan juga perencanaan minimum sistem Mikrokontroller ***AT89C51*** beserta *peripheral* yang digunakan pada perencanaan perangkat lunak yang juga digunakan pada minimum *sistem* Mikrokontroller *AT89C51*. Akan tetapi perangkat tersebut dalam kerjanya akan saling mendukung satu dengan lainnya sehingga alat yang direncanakan dapat berjalan sesuai dengan perencanaannya.

3.2. Perancangan Perangkat Keras

Dalam Tugas Akhir ini perencanaan dan pembuatan Alat *Score Board* berbasis Mikrokontroller *AT89C51* sebagai kontrol utama dan menggunakan komponen lain sebagai komponen pendukung. Sebelum membuat perangkat keras keras terlebih dahulu direncanakan blok diagram yang akan dibuat dan kemudian membahasnya sesuai dengan blok diagram tersebut. Adapun blok diagram alat tersebut adalah sebagai berikut:



Gambar 3.1
Blok Diagram Score Board Untuk Bulu Tangkis berbasis Mikrokontroller AT89C51

Gambar diatas adalah diagram blok dari rangkaian sistem. Rangkaian alat pengontrol tersebut terdiri dari rangkaian *Remote Receiver, MCU, Driver Seven Segment,* yang menggunakan *IC74LS164* dan *ULN 2004.*

3.3. Cara Kerja Alat

Pada kondisi awal, alat ini akan menampilkan *display* angka 00 pada sisi sebelah kiri dan kanan. Untuk display informasi pindah bola harus di*set* terlabih dahulu, sebab untuk olah raga bulu tangkis, yang melakukan *servis* pertama kali ditentukan oleh undian.

Setelah di*set* siapa/ sisi mana yang terlabih dahulu melakukan servis, maka tanda panah yang ada di bawah *display score* akan menyala, sebaliknya tanda yang satu lagi akan mati. Sebagai contoh, kita aktifkan sisi kiri yang pertama kali melakukan *servis*, maka tanda panah di sisi kiri akan menyala, sebaliknya tanda panah di sisi kanan akan mati.

Untuk penambahan *score*, pada alat ini kita masih menggunakan *sisitem* manual dengan cara menggunakan *Remote Control*. Kita hanya menekan tombol panah atas – bawah untuk *Display* sebelah kiri, dan tombol kiri – kanan untuk *Display* sebelah kanan. Mengapa hanya tombol tersebut yang dipergunakan, karena dalam olah raga bulu tangkis hanya membutuhkan penambahan nilai sampai *21 (rally point)*. Untuk menjaga kemungkinan *Deuce*, akan *diprogram* sampai *point 99 (max 2 digit)*.

Score board ini juga akan menampilkan informasi *set* yang telah dilalui. Apabila seorang pemain sudah mencapai nilai 21, maka *display* yang ada di atas display utama *(display score)* otomatis akan berubah juga. *Display* ini dibatasi sampai angka 2 (sesuai jumlah kemenangan pada olah raga ini yaitu mencari 2 set kemenangan)

3.4. Fungsi Komponen dari Rangkaian Sistem

Pada gambar *blok diagram* rangkaian keseluruhan diatas, dapat dilihat beberapa blok diagram yang masing-masing memiliki fungsi :

- *Mikrokontroller AT89C51*

  Digunakan sebagai kontrol utama untuk mengendalikan *system* dengan bantuan *software.*

- *Remote Transmitter*

  Berfungsi sebagai media pengirim data yang kita inginkan

- *Remote Receiver*

  Berfungsi sebagai media penerima data yang kita kirimkan melalui remote transmitter

- *ULN 2004*

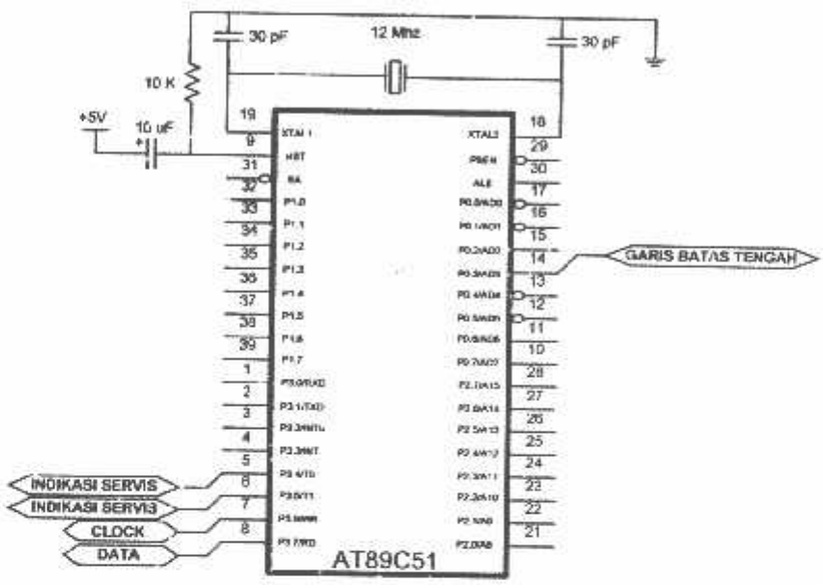
  Berfungsi sebagaipenguat *Led/ Seven Segment*

- *IC741s164*

  Berfungsi sebagai *Shift Register*

3.5. Perencanaan Rangkaian Minimum *Sistem MCU*

Rangkaian minimum *Mikrokontroller AT89C51* dan penyemat (pin) yang digunakan dalam perencanaan alat ini ditunjukkan pada gambar berikut ini:



Gambar 3.2.
Rangkaian Minimum Mikrokontroller AT89C51 [1]

Penyemat *X1* dan *X2* dihubungkan dengan *Kristal* yang berfungsi sebagai pembentuk sebuah *Isolator* bagi *Mikrokontroller*. *Kristal 12MHz* ini didukung dua *capasitor keramik C1* dan *C2* yang nilainya sama. Apabila terjadi beda potensial pada kedua *kapasitor* tersebut maka kristal akan *berosilasi*. *Pulsa* yang keluar adalah berbentuk gigi gergaji dan akan dikuatkan oleh rangkaian *internal* pembangkit rangkaian pulsa pada *mikrokontroller* sehingga akan berupa menjadi *pulsa clock*. Untuk pembagian dari *frekuensi internal mikrokontroller* itu sendiri yang *diinisialisasi* dengan program.

Penyemat *Reset* dihubungkan dengan *saklar* yang digunakan untuk *me-Reset mikrokontroller*. Karena kaki *reset* ini aktif *berlogic* tinggi maka diperlukan *Resistor R1 yang nilainya 10KΩ* yang dihubungkan dengan tegangan *0 Volt* untuk memastikan *penyemat Reset berlogic* rendah saat sistem ini bekerja. *Kapasitor C1=10μF* berfungsi untuk meredam adanya *pelentingan* akibat penekanan *saklar Reset*.

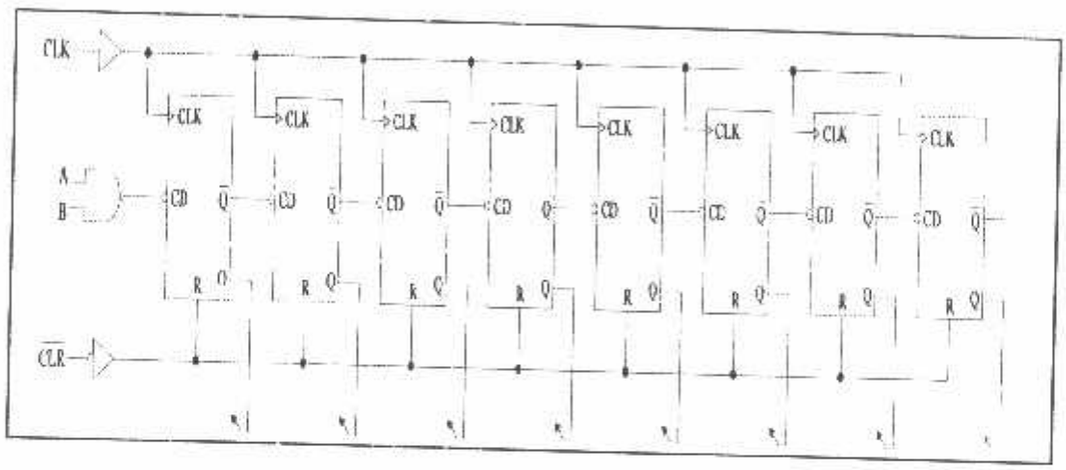
Port 3.6, dihubungkan dengan *IC74ls164* yang berfungsi sebagai *shift register (data)*, begitu pula untuk *Port 3.7* yang juga berfungsi sebagai sebagai *shift register (clock)*.

Port 3.4 dan 3.5 dihubungkan dengan rangkaian *Led* yang dalam perencanaan alat ini berfungsi sebagai penampil informasi pemegang servis.

Port 0.3 dihubungkan dengan rangkaian *Led* yang dalam perencanaan alat ini berfungsi sebagai penampil garis batas.

3.6. Rangkaian *Shift Register 8 bit*

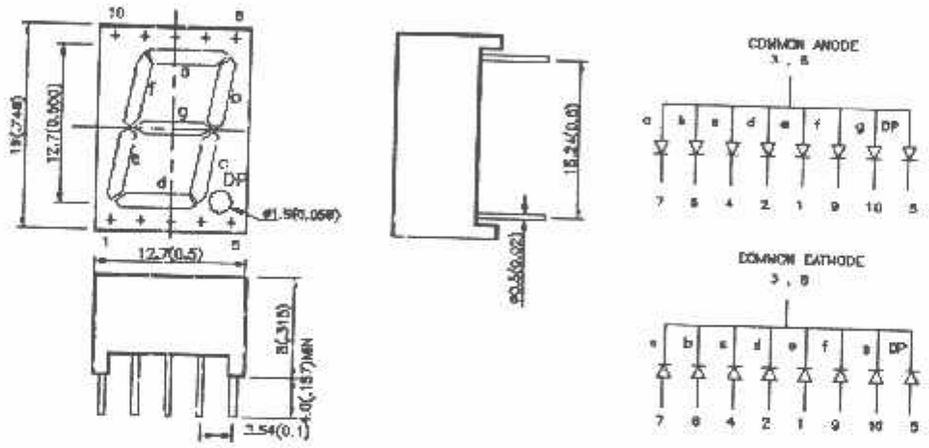
Rangkaian *shift register* digunakan untuk menggeser data masukan dari *MCU* yang berfungsi sebagai *scan* kolom pada LED *seven segment*. Masukan *register* geser *SN74LS164 (A, B, Clock)* berasal dari *Port* 3.6 – *Port* 3.7. Data yang keluar dari *output pararel register* geser digunakan pada proses *scanning* untuk pergeseran tampilan perkolom. Berikut ini gambar rangkaian dari *register* geser yang dirancang untuk menscan kolom *LED (seven segment)*



Gambar 3. 3.
Rangkaian Register geser untuk Scan kolom

3.7. Perencanaan Rangkaian *Display Seven Segment*

Bagian *display* adalah bagian yang berguna memberikan informasi hasil data *score* dari sebuah pertandingan bulu tangkis sehingga memudahkan para pemain, penonton dan wasit dengan melihat tampilan tersebut.Bagian ini terdiri dari beberapa blok yakni mikrokontroller AT89C51 sebagai pengendali utama, *seven segment* akan menampilkan huruf (tulisan) angka.



Gambar 3.4.
Seven Segment[2]

3.8. Perencanaan *Power Suplay*

Sebagaian besar rangkaian elektronika, membutuhkan tegangan *DC* untuk dapat bekerja dengan baik. Pada rangkaian *Power Suplay* ini, perencanaan menggunakan *transformator 3A* dan *Power Suplay* yang digunakan adalah *D 12 V*. rangkaian penyearah gelombang penuh biasanya menggunakan dua buah *dioda* atau empat buah *dioda*.

Tegangan *Output DC* (tegangan rata – rata) adalah:

Diketahui $Vef = 12\ V$

$Trafo = 3\ Ampere$

$Vm = \sqrt{2}\ x\ Vef$

$$VDC = \frac{2.Vm}{\pi} = 0.636.Vm$$

$$VDC = \frac{2.\sqrt{2x12}}{\pi}$$

$VDC = 0,725\ x\ 12$

$VDC = 8,700\ V$

Frekwensi Output :

$F\ out = 2.\ F\ in$

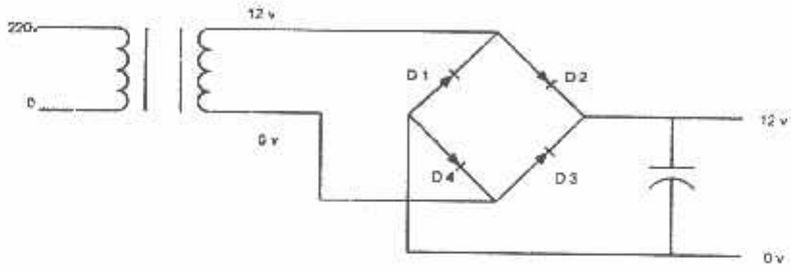
$F\ out = 2\ x\ 50\ Hz$

$F\ out = 100\ Hz$

Penyearah gelombang penuh setengah *siklus* tegangan *sekunder* yang positif, *dioda* (D1) mengalami *pra* tegangan maju dan *dioda* (D2) mengalami *pra* tegangan balik, sehingga arus mengalir melalui *dioda* (D1) tahanan beban. Tegangan beban mempunyai *polaritas* yang sama. Hal ini disebabkan karena arus mengalir melalui tahanan beban dari

arah yang sama tanpa memperhatikan *dioda* mana yang menghantar. Jadi tegangan beban berbentuk *sinyal* gelombang penuh.

Adapun gambar yang di *power supplay* yang ditunjukkan pada gambar di bawah ini :



Gambar 3.5. Rangkaian Power Supplay[11]

3.9. Perencanaan Rangkaian *Display Led*

Display utama yang akan digunakan adalah susunan dari *modul – modul Led* yang disusun menjadi sebuah *seven segment utama (besar).* Pada setiap *modul display anoda Led* dihubungkan semua schingga cuma terdapat *8 common anoda.* Sedangkan pada *katoda LED* dihubungkan pada keluaran *IC SN74LS164* yang berfungsi sebagai *shift register.* Dalam perencanaan rangkaian tampilan diperlukan rangkaian *driver* yang dihubungkan ke *port* 3.3 – *port* 3.7, dikarenakan arus yang keluar dari *port mikrokontroler* kecil. Dalam perancangan ini, digunakan *ULN 2004* sebagai penguat *Led.*

Dalam perancangan dan pembuatan alat ini, akan diberi tegangan sebesar *12 V DC,* karena karakteristik dari setiap *Led* akan aktif apabila dipicu oleh tegangan sebesar *1,5 20mA*, maka setiap *Led* akan membutuhkan tahanan agar *Led* tersebut tidak putus.

Di bawah ini adalah rumus untuk menentukan berapa besarnya tahanan agar *Led* bisa bekerja dengan baik sesuai perencanaan.

$$R = \frac{V - V_{LED}}{I_{IFD}}$$

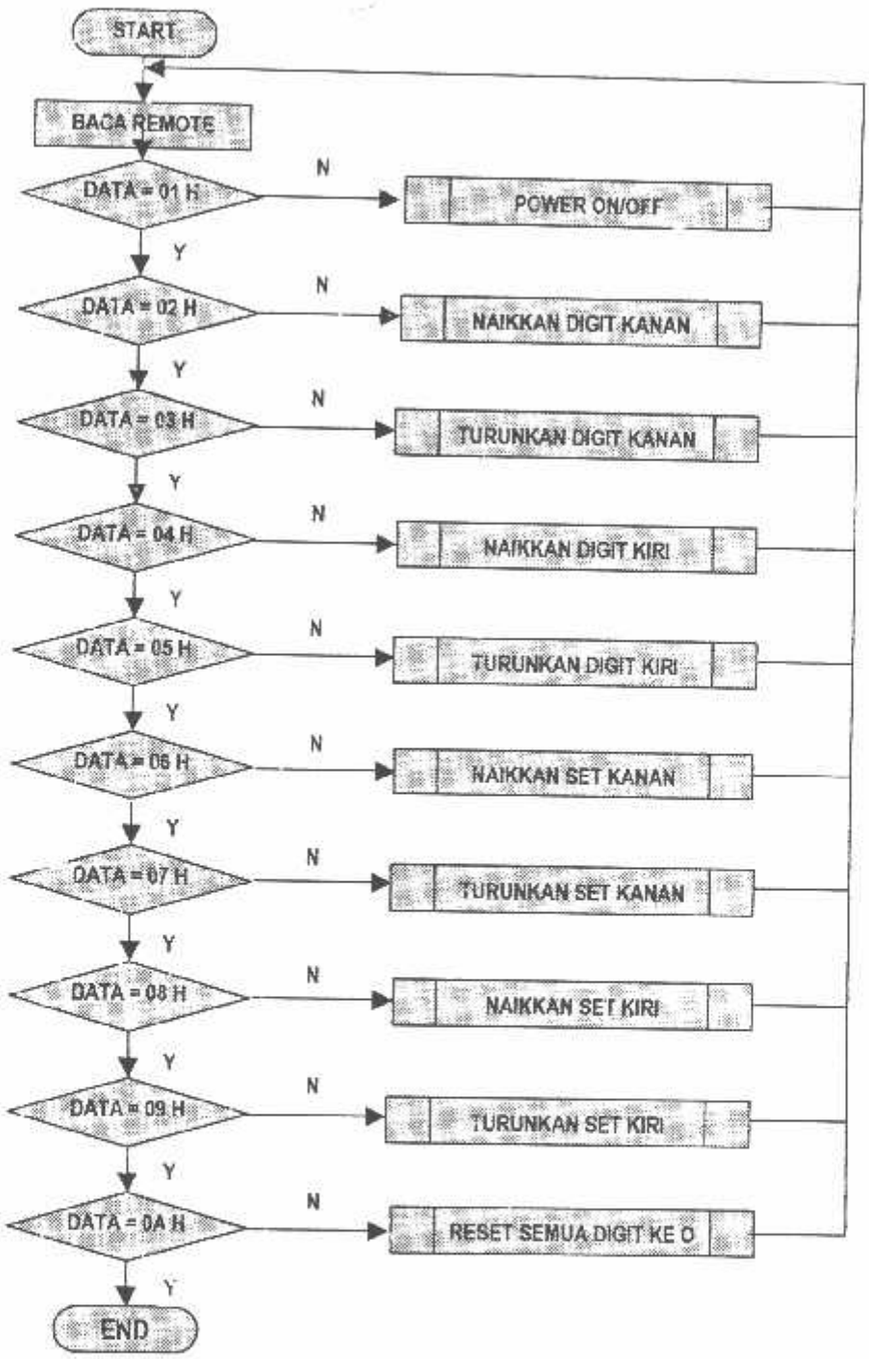
$$R = \frac{12 - 1{,}5}{20mA}$$

$$R = \frac{10{,}5}{20mA}$$

$$R = 0{,}525\ K\ atau\ 525\ \Omega$$

Jadi kita membutuhkan tahanan sebesar *525* Ω agar *Led* tidak putus. Karena tahanan tersebut sangat jarang tersedia di pasaran, dalam perancangan alat ini kami gunakan Tahanan bebas, asalkan tidak melebihi *2 KΩ*.

3.10. Perencanaan Perangkat Lunak *(Flow Chart)*



Gambar 3.6. Flow Chart Perencanaan Perangkat Lunak

BAB IV

PENGUJIAN ALAT

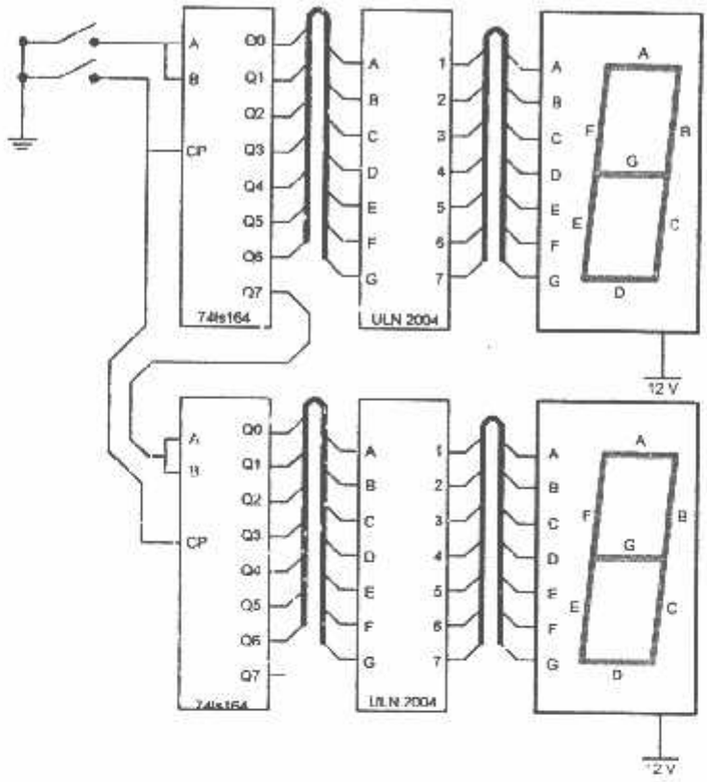
Tujuan pengujian adalah untuk mengetahui keadaan masukan atau keadaan keluaran dari tiap blok rangkaian yang direncanakan, sehingga dengan pengujian ini dapat diketahui apakah alat yang direncanakan dapat berfungsi dengan baik dan sesuai dengan yang diharapkan atau tidak. Untuk tujuan ini, pengujian dilakukan dengan urutan rangkaian sebagai berikut :

1. Pengujian *Seven Segment* sebagai penyampai informasi tampilan visual.
2. Pengujian Rangkaian *Minimum AT89C51*
3. Pengujian Rangkaian *Led* sebagai media penampil utama

4.1. Pengujian Rangkaian *Seven Segment*

Untuk mengetahui apakah rangkaian seven segment dapat bekerja sesuai dengan yang direncanakan, maka diperlukan pengujian. Dalam pengujian seven segment ini, alat yang diperlukan :

1. 1 buah *IC 74ls164*
2. 1 buah *Seven Segment*
3. 1 buah *deep switch 2 pin*
4. *power suplay 12 V & 5 V*



Gambar 4.1.
Pengujian Rangkaian Seven Segment

Semua komponen dirangkai sesuai dengan gambar diatas dan *deep switch dikonfigurasikan* dengan tabel di bawah, dan jika *output* juga sesuai dengan tabel maka rangkaian dapat dihubungkan dengan *MCU*.

Tabel 4.1.
Input dan Outputan pengujian Seven Segment

Input 1				Input 2				Output 1							Output 2							TAMPILAN
A	B	C	D	A	B	C	D	a	b	c	d	e	f	g	a	b	c	d	e	f	g	ANGKA
0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	1	0-0
0	0	0	1	0	0	0	1	1	0	0	1	1	1	1	1	0	0	1	1	1	1	1-1
0	0	1	0	0	0	1	0	0	0	1	0	0	1	0	0	0	1	0	0	1	0	2-2
0	0	1	1	0	0	1	1	0	0	0	0	1	1	0	0	0	0	0	1	1	0	3-3
0	1	0	0	0	1	0	0	1	0	0	1	1	0	0	1	0	0	1	1	0	0	4-4
0	1	0	1	0	1	0	1	0	1	0	0	1	0	0	0	1	0	0	1	0	0	5-5
0	1	1	0	0	1	1	0	1	1	0	0	0	0	0	1	1	0	0	0	0	0	6-6
0	1	1	1	0	1	1	1	0	0	0	1	1	1	1	0	0	0	1	1	1	1	7-7
1	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	8-8
1	0	0	1	1	0	0	1	0	0	0	1	1	0	0	0	0	0	1	1	0	0	9-9

Hasil pengujian rangkaian tersebut di atas dapat juga kita coba langsung dengan menggunakan program pada *MCU*.

Contah *Programnya* adalah sbb:

```
;--------------------------------
;       DEMO SEVEN SEGMENT
;--------------------------------
Togle  BIT    20H.0
DAT    BIT    P3.6
CLK    BIT    P3.7
RAM_1        EQU   22H
Ram_2EQU   23H
Ram_3EQU   24H
Ram_4EQU   25H
Ram_5EQU   26H
Ram_6EQU   27H
Kanan EQU   28H
Kiri    EQU   29H
Key    EQU   2AH
               ORG   0H
               JMP   Mulai
CLOCK:         NOP
               NOP
```

```
        NOP
        NOP
        CLR  CLK
        NOP
        NOP
        NOP
        NOP
        SETB CLK
        RET
Delay:  MOV  R4,#0FH
        DJNZ R4,$
        RET
Delay_L: MOV  R5,#02H
Jum_10:     CALL Delay
        DJNZ R5,Jum_10
        RET
Scan:   MOV  C,ACC.0
        MOV  DAT,C
        CALL CLOCK
        MOV  C,ACC.1
        MOV  DAT,C
        CALL CLOCK
        MOV  C,ACC.2
```

```
        MOV  DAT,C
        CALL CLOCK
        MOV  C,ACC.3
        MOV  DAT,C
        CALL CLOCK
        MOV  C,ACC.4
        MOV  DAT,C
        CALL CLOCK
        MOV  C,ACC.5
        MOV  DAT,C
        CALL CLOCK
        MOV  C,ACC.6
        MOV  DAT,C
        CALL CLOCK
        MOV  C,ACC.7
        MOV  DAT,C
        CALL CLOCK
        RET
Reset:  MOV  R2,#20H
        CLR  DAT
Jum_1:  CLR  CLK
        NOP
        NOP
```

```
        NOP
        SETB  CLK
        DJNZ  R2,Jum_1
        RET
Reset_0: MOV  Kanan,#00H
        MOV  A,Kanan
        CALL Tampil_BCD
        CALL BCD_1
        CALL T_Digit
        MOV  Kiri,#00H
        MOV  A,Kiri
        CALL Tampil_BCD
        CALL BCD_2
        CALL T_Digit
        RET
T_Digit: MOV  A,Ram_4
        MOV  DPTR,#Angka
        MOVC        A,@A+DPTR
        CALL Scan
        MOV  A,Ram_3
        MOV  DPTR,#Angka
        MOVC        A,@A+DPTR
        CALL Scan
```

```
        MOV  A,Ram_2
        MOV  DPTR,#Angka
        MOVC        A,@A+DPTR
        CALL Scan
        MOV  A,Ram_1
        MOV  DPTR,#Angka
        MOVC        A,@A+DPTR
        CALL Scan
        RET
;-------------------------------------------------------------
Banding:        CALL Baca_Key          ;Kanan UP
        MOV  A,Key
        CJNE A,#0aH,Jum_6
        INC  Kanan
        MOV  A,Kanan
        CJNE A,#63H,Jum_0B
        CALL Reset_0
Jum_0B:         CALL Tampil_BCD
        CALL BCD_1
        CALL T_Digit
        RET
Jum_6:  CJNE A,#02H,Jum_7          ;Kanan DOWN
        MOV  A,Kanan
```

```
                CJNE  A,#00H,Jum_0C
                JMP   Jum_0A
Jum_0C:         DEC   Kanan
                MOV   A,Kanan
                CALL  Tampil_BCD
                CALL BCD_1
                CALL T_Digit
                RET
Jum_7:          CJNE  A,#0cH,Jum_8          ;Kiri UP
                INC   Kiri
                MOV   A,Kiri
                CJNE  A,#63H,Jum_0D
                CALL Reset_0
Jum_0D:         CALL Tampil_BCD
                CALL BCD_2
                CALL T_Digit
                RET
Jum_8:          CJNE  A.#06H,Jum_9          ;Kiri DOWN
                JNB   P3.3,$
                MOV   A,Kiri
                CJNE  A,#00H,Jum_0E
                JMP   Jum_0A
Jum_0E:         DEC   Kiri
```

```
                MOV  A,Kiri
                CALL Tampil_BCD
                CALL BCD_2
                CALL T_Digit
                RET
Jum_9:          CJNE A,#0cH,Jum_0A
                CALL Reset_0
Jum_0A:         RET
;-------------------------------------------------------------
Power:          CALL Baca_Key
                MOV  A,Key
                CJNE A,#04H,Jum_B
                JNB  Togle,Jum_C
                CLR  Togle
                RET
Jum_C:          SETB Togle
Jum_B:          RET
;-------------------------------------------------------
Tampil_BCD: MOV  B,#0AH
            DIV  AB
            MOV  R0,B
            MOV  B,#0AH
            DIV  AB
```

```
        MOV  R1,B
        RET
BCD_1:  MOV  Ram_1,R0
        MOV  Ram_2,R1
        RET
BCD_2:  MOV  Ram_3,R0
        MOV  Ram_4,R1
        RET
Baca_Key: MOV  Key,#00H
        MOV  C,P3.0
        MOV  Key.3,C
        MOV  C,P3.1
        MOV  Key.2,C
        MOV  C,P3.2
        MOV  Key.1,C
        MOV  C,P3.3
        MOV  Key.0,C
        JNB  P3.0,baca_key
        JNB  P3.1,baca_key
        JNB  P3.2,baca_key
        JNB  P3.3,baca_key
;CALL Delay
        RET
```

```
;-------------------------------------------------------------

Mulai:      CALL Reset
mulai_1:        call    pOWER
            jb      togle,mulai_1
            CALL Reset_0
Jum_A:          CALL Banding
            call    power
            jnb     togle,jum_a
            JMP     mulai
;-------------------------------------------------------------
ANGKA:      DB      0FDH,0DH,0B7H,09FH,4FH,0DBH,0FBH,8DH,0FFH,0DFH
END
```

4.2. Pengujian Rangkaian *Minimum AT89C51*

4.2.1. Tujuan Pengujian.

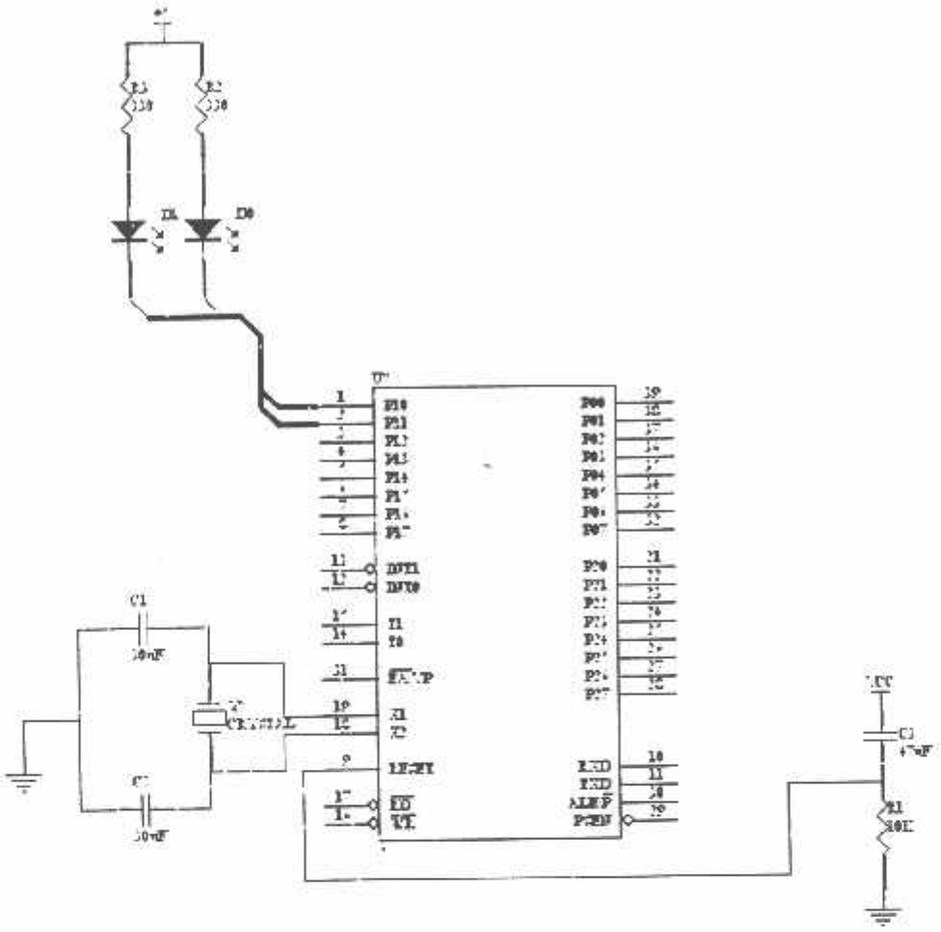
Pada pengujian ini dapat diketahui apakah rangkaian minimum dapat bekerja sesuai dengan program yang di masukan. Rangkaian minimum *AT89C51* di hubungkan ke *Led* melalui *port 1*. Adapun cara kerja dari program adalah menyalakan lampu secara bergantian gambar 4.2 adalah rangkaian *Led* dengan *MCU*.

4.2.2. Alat dan Bahan

1. Rangkaian *Mikrokontroller* yang akan diuji.
2. Catu Daya.
3. *Led* peraga output *Mikrokotroller*
4. *Programmer* dan *Evaluator Board*.

4.2.3. Pelaksanaan Pengujian.

1. Merangkai rangkaian *mikrokontroller* seperti gambar 4.2.
2. Menghubungkan rangkaian *mikrokontroller* ke catu daya.
3. Membuat Program *Software*.
4. Memprogaram *IC Mikrokontroller* kemudian menjalankannya.



Gambar 4.2. Gambar Rangkaian LED pada MCU 89C51 [1]

4.2.4. Analisa Hasil Pengujian

Agar sebuah *Mikrokontroller* dapat mengirim data , terlebih dahulu *Mikrokontroler* diprogram software *HB 2000*. Adapun potongan program inisialisasi *Mikrokontroller* dapat dilihat dibawah ini :

```
        ORG 00H
        JMP Mulai
Satu:   CLR  P1.0
        SETB P1.1
        RET
Dua:    CLR  P1.1
        SETB P1.0
        RET
Delay:  MOV  R2,#0FFH
JUM_1:  MOV  R3,#0FFH
        DJNZ R3,$
        DJNZ R2,JUM_1
        RET
Mulai:  CALL Satu
        CALL Delay
        CALL Dua
        CALL Delay
        JMP  Mulai
        END
```

4.3. Pengujian *Display Led*

4.3.1. Tujuan

Pengujian *Led* bertujuan apakah alat yang kita uji sudah sesuai dengan yang kita rancang.

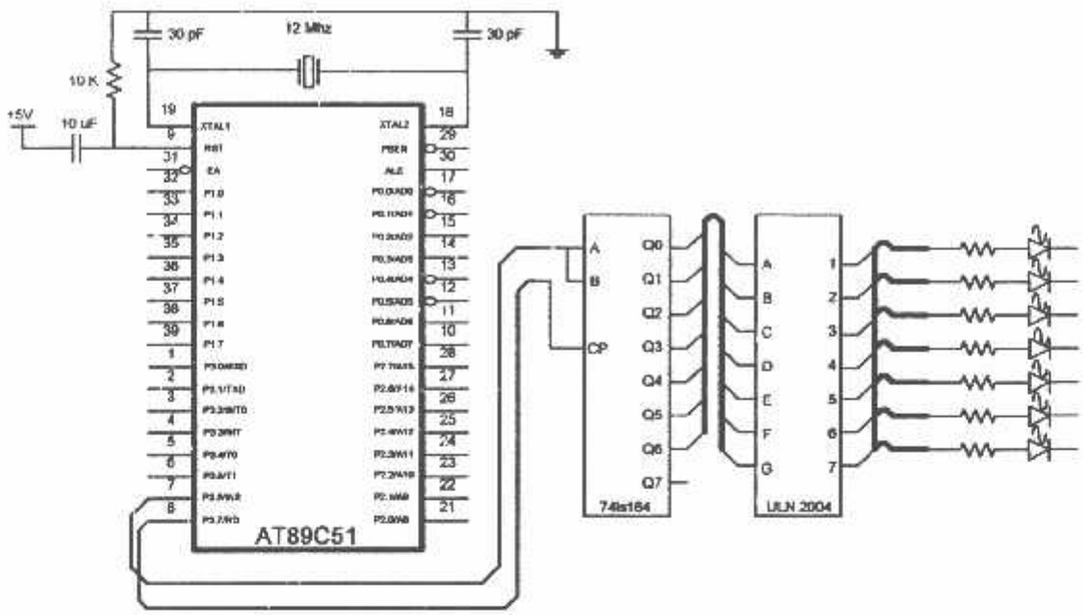
4.3.2. Peralatan Yang Digunakan

1. Rangkaian *Led*
2. Rangkaian minimum system *AT89C51* yang telalah terisi *program*
3. *Multimeter* digital

4.3.3. Langkah Pengujian

Langkah-langkah pengujian *Led* adalah sebagai berikut :

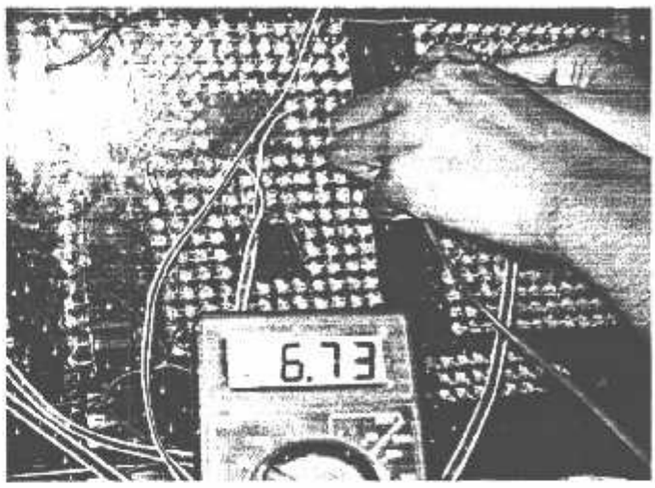
1. Menyusun rangkaian rangkaian *Led* seperti pada gambar 4.3.
2. Menghubungkan rangkaian susunan *Led port 3.6 – port 3.7 minimum system AT89C51*
3. Menghubungkan *multimeter* pada kaki *basis* dan kaki *colektor* driver *Led*



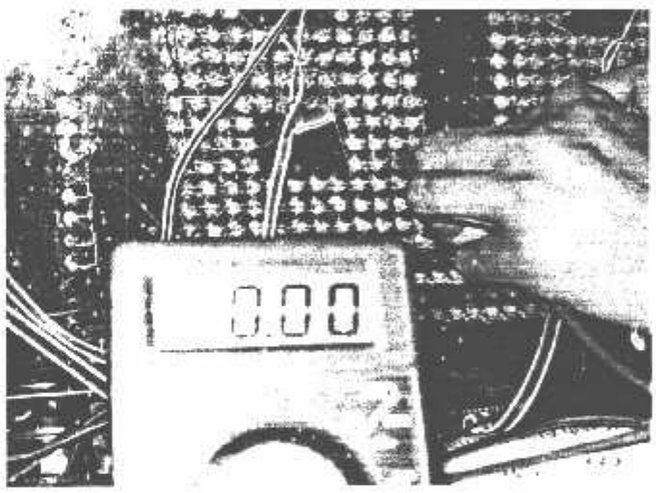
Gambar 4.3.
Gambar Pengujian Rangkaian LED sebagai display utama

Tabel 4.3. Tabel Hasil Pengujian Rangkaian Display Lcd

Kondisi */ segmen*	**Inpat (Volt)**	**Output (Volt)**
Aktif (Menyala) */ segmant*	**12**	**6,73**
Tidak Aktif (Mati) */ segmen*	**12**	**0**



Gambar 4.4.
Foto Hasil Pengujian Led pada saat Aktif (Menyala)



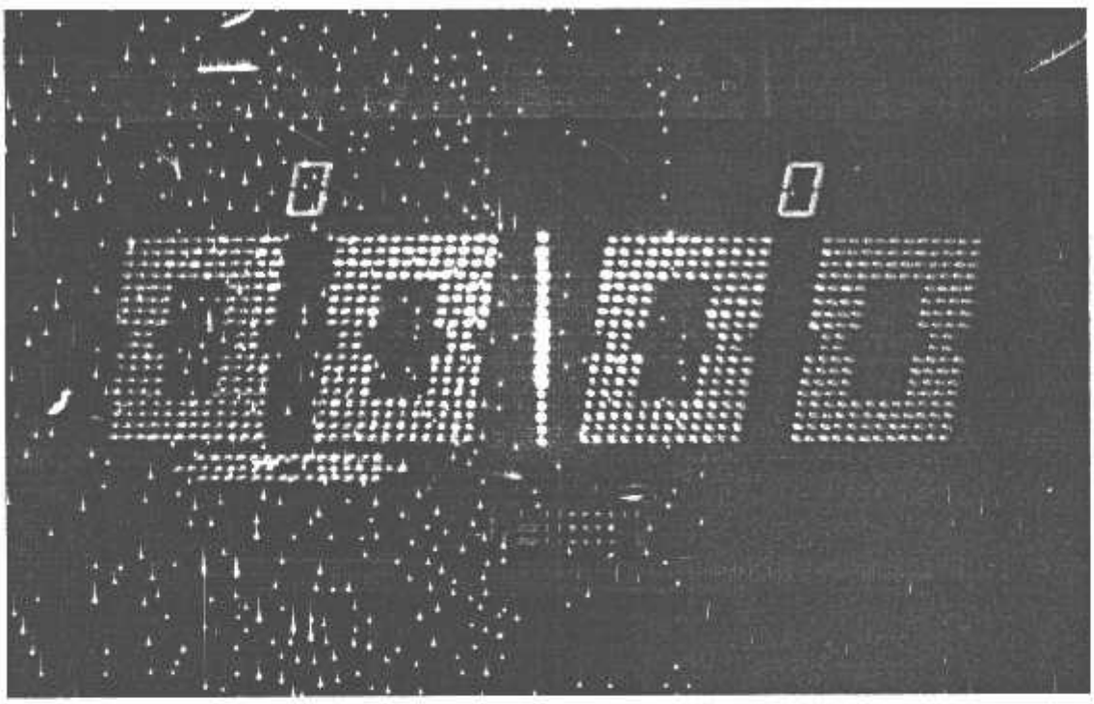
Gambar 4.5.
Foto Hasil Pengujian Led pada saat Tidak Aktif (Mati)

4.4. Pengujian Jarak Tempuh untuk Remote Control

Pengujian ini bertujuan untuk mengetahui berapa jarak maksimal remote control pada perencanaan dan pembuatan alat ini. Pengujian ini dilakukan secara bertahap mulai dari jarak 1 meter sampai jarak maksimal dimana *receiver remote control* tidak *responsive* terhadap data yang dikirimkan melalui *transmitter*.

Tabel 4.2. Hasil Pengujian Jarak Tempuh Remote

JARAK (Meter)	HASIL	KONDISI RESPON
1 meter	Sangat Baik	1 Kali Tekan Tombol Remote
1,5 meter	Sangat Baik	1 Kali Tekan Tombol Remote
2 meter	Sangat Baik	1 Kali Tekan Tombol Remote
2,5 meter	Sangat Baik	1 Kali Tekan Tombol Remote
3 meter	Baik	2 Kali Tekan Tombol Remote
3,5 meter	Baik	2 Kali Tekan Tombol Remote
4 meter	Baik	2 Kali Tekan Tombol Remote
4,5 meter	Cukup Baik	2-3 Kali Tekan Tombol Remote
5 meter	Kurang Baik	3 Kali Tekan Tombol Remote
5,5 meter	Kurang Baik	3 Kali Tekan Tombol Remote
6 meter	Tidak Merespon	Tidak Merespon



Gambar 4.6. Foto Alat Keseluruhan

BAB V

PENUTUP

Bab ini merupakan kesimpulan dari aplikasi *Mikrokontroller AT89C51* sebagai pengontrol utama pada alat *Score Board* untuk olah raga bulu tangkis. Bab ini juga diberikan saran yang mungkin bisa dilaksanakan untuk meningkatkan unjuk kerja piranti yang telah dibuat.

5.1. Kesimpulan

Setelah melalui beberapa tahap perencanaan alat yang kemudian dilanjutkan dengan pengujian alat untuk memberikan gambaran mengenai unjuk kerja alat yang telah dibuat. Dari hal pengujian dan analisis diperoleh kesimpulan sebagai berikut :

1. Hasil pengujian menunjukkan bahwa *resistor* / tahanan yang kita pasang sebagai bagian dari perancangan *display led* sebesar *525* Ω sesuai dengan yang dibutuhkan. *Display Led* terbukti bisa menyala dengan baik dan tidak ada satu *led* pun yang putus.
2. *IC74ls164* yang berfungsi sebagai *shift register* mampu berjalan dengan baik, terbukti bahwa data yang kita kirimkan melalui *remote transmitter* dapat diterima oleh *remotte receiver* dan ditampilkan dengan baik.
3. Pada saat aktif, tegangan *display led* sebesar 6,7 V. Pada saat tidak aktif tegangan *display lcd* sebesar 0 V
4. Perancangan Power Suplay sebesar 3 Ampere, 12 V DC ke alat ini, terbukti sesuai dengan kondisi alat yang mampu menyala dan bekerja dengan baik dengan menambahkan tahanan sebesar 525 Ω - 1K8 pada tiap –tiap led yang terpasang.

5.2. SARAN

1. Dalam rancang bangun suatu peralatan hendaknya direncanakan secara matang dengan memperhatikan keterbatasan pengetahuan, ketrampilan dan pengalaman yang dimiliki serta sarana dan prasarana yang dibutuhkan. *Observasi* di lapangan perlu dilakukan untuk melengkapi data-data yang dibutuhkan dan memperluas wawasan.
2. Bahan dan komponen yang digunakan dalam perancangan dipilih setepat mungkin dengan harga yang terjangkau tetapi masih memenuhi syarat-syarat kenyamanan dan keamanan.
3. Dalam pengoperasian alat, hendaknya diperhatikan cara pengoperasian yang benar karena akan memberikan hasil yang maksimal sesuai dengan yang diharapkan.

DAFTAR PUSTAKA

[1]. *Data Sheet* Mikrokontroller *AT89C51. Atmel Corp*

[2]. *Data Sheet Led*

[3]. ATMEL *Data Book*, 1999

[4]. MCS 51 *Microcontroller Family User's Manual* : I-18

[5]. *Data Sheet ULN 2004*

[6]. *Data Sheet 74LS164*

[7]. MV/DTMF *Componen Data Sheet*, USA, *MITEL Corporation*

[8]. *National Telekomunikasi Databook*, USA, *National semikonduktor Coporation*

[9]. *Data Sheet* Sevent Segment

[10]. *Design Protel 99Se*

[11]. Dasar Teknik Listrik, Zuhal

Lampiran

INSTITUT TEKNOLOGI NASIONAL
FAKULTAS TEKNOLOGI INDUSTRI
JURUSAN TEKNIK ELEKTRO D-III
PROGRAM STUDI TEKNIK ENERGI LISTRIK

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Program Studi : Teknik Energi Listrik

Dipertahankan dihadapan Team Penguji Tugas Akhir Jenjang Diploma (D-III)

Pada Hari : Sabtu

Tanggal : 22 September 2007

Dengan Nilai : A (83,70)

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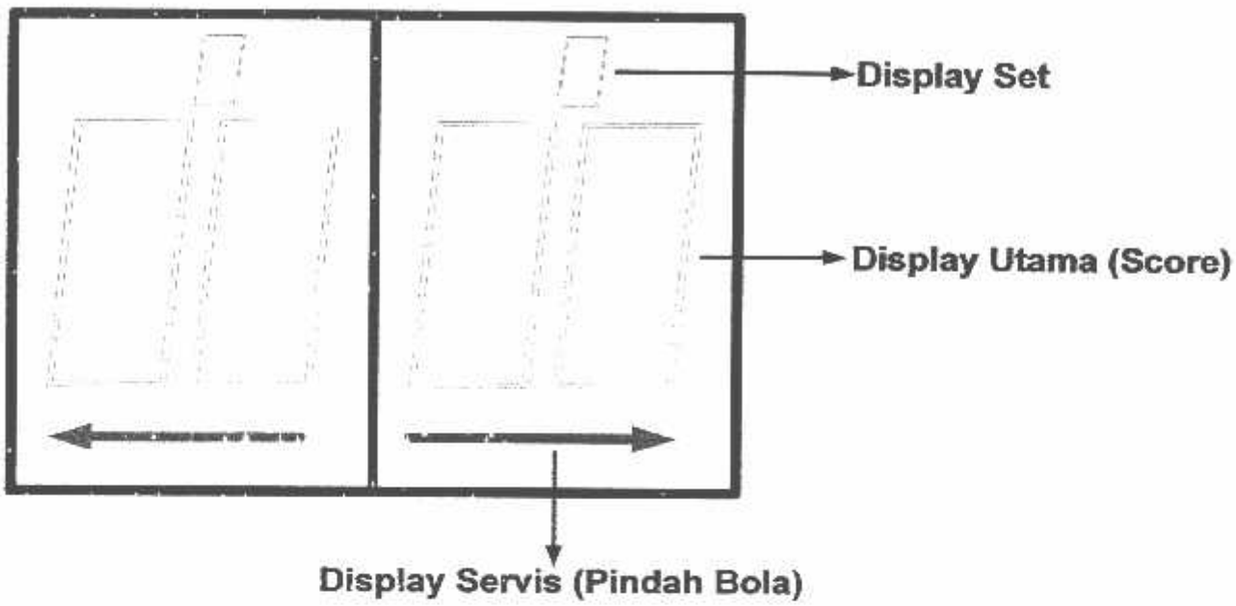
Dimensi Alat



Panjang : 70 cm

Lebar : 15 cm

Tinggi : 35 cm

```
$MOD51
;=============================================================
; PROGRAM DEMO HIR04 DENGAN MENGGUNAKAN
; REMOTE CONTROL TV MERK SONY SEBAGAI
; PENGHASIL KODE PULSA.
; KODE ASLI REMOTE DIKELUARKAN MELALUI PORT 2
; HASIL PENGOLAHAN DATA DITAMPILKAN MELALUI DISPLAY DOT MATRIX
; X-TAL = 12.000.000 HZ
;=============================================================
FLAG                    EQU     20H
HEAD                    BIT     20H.0
DATA_R                  BIT     20H.1
FINISH                  BIT     20H.2
KODE                    EQU     24H
COUNTER                 EQU     25H
LAMA                    EQU     26H
DEL1                    EQU     6EH
DEL2                    EQU     6FH
TEMP                    EQU     78H
VERTICAL        EQU     79H
;-------------------------------------------------------------
;       DEMO SEVEN SEGMENT
;-------------------------------------------------------------
DAT     BIT     P3.6
CLK     BIT     P3.7
RAM_1   EQU     30H
RAM_2   EQU     28H
RAM_3   EQU     29H
RAM_4   EQU     2AH
RAM_5   EQU     2BH
RAM_6   EQU     2CH
KANAN   EQU     2DH
KIRI    EQU     2EH
KEY     EQU     2FH
TOGLE   BIT     27H.0
BATAS   BIT     P3.0
; ---------------------------------------------
    ORG         0H
        JMP     MULAI0
;
        ORG     0BH
        CLR     TR0         ; STOP TIMER/COUNTER 0
        RETI
;
        ORG     13H
;*************************************
; ROUTINE INTERUPT IR RECEIVER MODULE
;*************************************
REMOTE: CLR     TR0
        CLR     EA
        JB      HEAD,PULSA_KEDUA_DST
        SETB    HEAD
        MOV     TH0,#0
        MOV     TL0,#0
        SETB    EA
        SETB    TR0         ; START TIMER/COUNTER 1
```

```
            RETI
;*************************************
; ROUTINE UNTUK TERJEMAHKAN REMOTE SONY
;*************************************
PULSA_KEDUA_DST:
            PUSH    ACC
            PUSH    PSW
            JB      DATA_R,DATA_REMOTE
            MOV     A,TH0
            CJNE    A,#0AH,N1
            SETB    DATA_R
            MOV     COUNTER,#7
            SJMP    TERUS
N1:         CJNE    A,#0BH,NOT_OK1
            SETB    DATA_R
            MOV     COUNTER,#7
            SJMP    TERUS
NOT_OK1:
            MOV     FLAG,#0
TERUS:      MOV     TH0,#0
            MOV     TL0,#0
            POP     PSW
            POP     ACC
            SETB    EA
            SETB    TR0         ; START TIMER/COUNTER 1
            RETI
;*****************************
; DATA REMOTE DIAMBIL 7 BIT
;*****************************
DATA_REMOTE:
            MOV     A,TH0
            CJNE    A,#4,REM0
            CLR     KODE.0
            SJMP    REMITT
REM0:       CJNE    A,#5,REM1
            CLR     KODE.0
            SJMP    REMITT
REM1:       CJNE    A,#6,REM3
            SETB    KODE.0
            SJMP    REMITT
REM3:       CJNE    A,#7,SALAH
            SETB    KODE.0
REMITT:     MOV     A,KODE
            RL      A
            MOV     KODE,A
            DJNZ    COUNTER,TERUS
            SETB    KODE.0
            SETB    FINISH
SALAH:      MOV     LAMA,KODE
            CLR     HEAD
            CLR     DATA_R
            SJMP    TERUS
;*************************************************************
;           START PROGRAM
;*************************************************************
MULAI0:     CLR     P3.5
```

```
        CLR     P3.4
        CLR     BATAS
        CALL    RESET
        MOV     SP,#30H
        MOV     TCON,#0
        SETB    TR0
        MOV     TMOD,#29H       ; 2UNTUK SERIAL MODE 2,UNTUK IR MODE 1
INT0
        SETB    PX1             ; PRIORITY
        SETB    IT1             ; SET EXT. INT.1 TO DOWN
        SETB    EX1             ; ENABLE EXT. INT.1
        SETB    ET0             ; ENABLE TIMER OVERFLOW INTERUP 1
        CALL    DELAY
        CALL    DELAY
;****************************************
;TUNGGU_DITEKAN: LOOP
;****************************************
MULAI:  MOV     DPTR,#NOL
ULANG:  SETB    EA              ; ENABLE ALL INTERUPT
        JB      FINISH,SDH_DITEKAN
        CALL    DISPLAY
        JMP     ULANG
SDH_DITEKAN:
        CLR     EA
;****************************************
; ROUTINE UNTUK MEMPROSES DATA RC SONY
;****************************************
PROGSONY:
        CLR     FINISH
        MOV     P2,A
        MOV     A,KODE
        CPL     A
        MOV     P2,A
        CALL    BANDING
        MOV     P2,#0FFH
        CPL     A
;=========================================
CARI_URUTAN_KODE:
        MOV     R2,#33          ; JML TOMBOL REMOTE SONY
        MOV     DPTR,#REM
LAGI_CARI:
        MOV     A,R2
        MOVC    A,@A+DPTR
        CJNE    A,KODE,TERUS_C
        JMP     TERUS_P
TERUS_C: DJNZ   R2,LAGI_CARI
        JMP     ULANG
TERUS_P:
        MOV     A,R2
        MOV     DPTR,#TS
        MOV     B,#6
        MUL     AB
        ADD     A,DPL
        MOV     DPL,A
        CLR     A
        ADDC    A,DPH
```

```
        MOV     DPH,A
        JMP     ULANG
;=============================
; UNTUK MENAMPILKAN DISPLAY
; DALAM 1 KALI SCANNING VERTICAL
; SEDERETAN DATA YANG TERLETAK
; DI DPTR INTERNAL
;=============================
DISPLAY:
        PUSH    DPH
        PUSH    DPL
        INC     DPTR
        MOV     TEMP,#5H
        MOV     VERTICAL,#01H
NEXTV:  CLR     A
        MOVC    A,@A+DPTR
        CPL     A
        MOV     P1,A
        MOV     P0,VERTICAL
        MOV     A,VERTICAL
        RL      A
        MOV     VERTICAL,A
        CALL    DELAY
        MOV     P1,#0FFH
        MOV     P0,#0H
        INC     DPTR
        DJNZ    TEMP,NEXTV
        POP     DPL
        POP     DPH
        RET
;=============
 SUB ROUTINE DELAY
;=============
DELAY:  MOV     R4,#00H
DELAY1: NOP
        DJNZ    R4,DELAY1
        RET
MDELAY: MOV     R4,#50
        JMP     DELAY1
DELAY_L:        MOV     R6,#0FFH
                DJNZ    R6,$
                RET
;-------------------------------------------------------------------------------
CLOCK:          NOP
                NOP
                NOP
                NOP
                CLR     CLK
                NOP
                NOP
                NOP
                NOP
                SETB    CLK
                RET
SCAN:           MOV     C,ACC.0
                MOV     DAT,C
```

```
        CALL    CLOCK
        MOV     C,ACC.1
        MOV     DAT,C
        CALL    CLOCK
        MOV     C,ACC.2
        MOV     DAT,C
        CALL    CLOCK
        MOV     C,ACC.3
        MOV     DAT,C
        CALL    CLOCK
        MOV     C,ACC.4
        MOV     DAT,C
        CALL    CLOCK
        MOV     C,ACC.5
        MOV     DAT,C
        CALL    CLOCK
        MOV     C,ACC.6
        MOV     DAT,C
        CALL    CLOCK
        MOV     C,ACC.7
        MOV     DAT,C
        CALL    CLOCK
        RET
RESET:  CLR     P3.4
        CLR     P3.5
        MOV     R2,#30H
        CLR     DAT
UM_1:   CLR     CLK
        NOP
        NOP
        NOP
        SETB    CLK
        DJNZ    R2,JUM_1
        RET
RESET_0:MOV     KANAN,#00H
        MOV     A,KANAN
        CALL    TAMPIL_BCD
        CALL    BCD_1
        CALL    T_DIGIT
        MOV     KIRI,#00H
        MOV     A,KIRI
        CALL    TAMPIL_BCD
        CALL    BCD_2
        CALL    T_DIGIT
        MOV     RAM_5,#00H
        CALL    T_DIGIT
        MOV     RAM_6,#00H
        CALL    T_DIGIT
        RET
T_DIGIT:MOV     A,RAM_6
        MOV     DPTR,#ANGKA
        MOVC    A,@A+DPTR
        CALL    SCAN
        MOV     A,RAM_5
        MOV     DPTR,#ANGKA
        MOVC    A,@A+DPTR
```

```
                CALL    SCAN
                MOV     A,RAM_1
                MOV     DPTR,#ANGKA
                MOVC    A,@A+DPTR
                CALL    SCAN
                MOV     A,RAM_2
                MOV     DPTR,#ANGKA
                MOVC    A,@A+DPTR
                CALL    SCAN
                MOV     A,RAM_3
                MOV     DPTR,#ANGKA
                MOVC    A,@A+DPTR
                CALL    SCAN
                MOV     A,RAM_4
                MOV     DPTR,#ANGKA
                MOVC    A,@A+DPTR
                CALL    SCAN
                RET
;-----------------------------------------------
BANDING:        CJNE    A,#0F6H,JUM_6           ;KANAN UP
                JB      TOGLE,JUM_001
                INC     KANAN
                SETB    P3.4
                CLR     P3.5
                MOV     A,KANAN
                CJNE    A,#63H,JUM_0B
                CALL    RESET_0
JUM_0B:         CALL    TAMPIL_BCD
                CALL    BCD_1
                CALL    T_DIGIT
JUM_001:        RET
JUM_6:          CJNE    A,#76H,JUM_7            ;KANAN DOWN
                JB      TOGLE,JUM_002
                MOV     A,KANAN
                CJNE    A,#00H,JUM_0C
                JMP     JUM_0A
JUM_0C:         DEC     KANAN
                MOV     A,KANAN
                CALL    TAMPIL_BCD
                CALL    BCD_1
                CALL    T_DIGIT
JUM_002:        RET
JUM_7:          CJNE    A,#0B6H,JUM_8           ;KIRI UP
                JB      TOGLE,JUM_003
                INC     KIRI
                SETB    P3.5
                CLR     P3.4
                MOV     A,KIRI
                CJNE    A,#63H,JUM_0D
                CALL    RESET_0
JUM_0D:         CALL    TAMPIL_BCD
                CALL    BCD_2
                CALL    T_DIGIT
JUM_003:        RET
JUM_8:          CJNE    A,#36H,JUM_9            ;KIRI DOWN
                JB      TOGLE,JUM_004
```

```
                MOV     A,KIRI
                CJNE    A,#00H,JUM_0E
                JMP     JUM_0A
JUM_0E:         DEC     KIRI
                MOV     A,KIRI
                CALL    TAMPIL_BCD
                CALL    BCD_2
                CALL    T_DIGIT
JUM_004:        RET
JUM_9:          CJNE    A,#5611,JUM_110         ;POWER
                JNB     TOGLE,JUM_009
                CLR     TOGLE
                SETB    BATAS
                CALL    RESET_0
                RET
JUM_009:        SETB    TOGLE
                CALL    RESET
                CLR     BATAS
                RET
JUM_110:        CJNE    A,#0D0H,JUM_111         ;KECIL KANAN UP
                INC     RAM_5
                CALL    T_DIGIT
                RET
UM_111:         CJNE    A,#50H,JUM_112          ;KECIL KANAN DOWN
                MOV     A,RAM_5
                CJNE    A,#00H,JUM_112A
                RET
UM_112A:        DEC     RAM_5
                CALL    T_DIGIT
                RET
UM_112:         CJNE    A,#92H,JUM_113          ;KECIL KIRI UP
                INC     RAM_6
                CALL    T_DIGIT
                RET
UM_113:         CJNE    A,#16H,JUM_10           ;KECIL KIRI DOWN
                MOV     A,RAM_6
                CJNE    A,#00H,JUM_113A
                RET
UM_113A:        DEC     RAM_6
                CALL    T_DIGIT
                RET
UM_10:          CJNE    A,#0D6H,JUM_0A          ;RESET
                JB      TOGLE,JUM_0A
                CALL    RESET_0
UM_0A:          RET
-------------------------------------------------
AMPIL_BCD:      MOV     B,#0AH
                DIV     AB
                MOV     R0,B
                MOV     B,#0AH
                DIV     AB
                MOV     R1,B
                RET
CD_1:           MOV     RAM_1,R0
                MOV     RAM_2,R1
                RET
```

```
                                GABUNG
BCD_2:          MOV     RAM_3,R0
                MOV     RAM_4,R1
                RET
;=============================================
; DATA AREA
;=============================================
REM:    DB      099H,001H,081H,041H,0C1H,021H,0A1H,061H,0E1H,011H
        DB      029H,05DH,0A9H,0FDH,0A5H,01DH,0D5H,02FH,03FH,0E9H
        DB      0AFH,087H,03DH,049H,009H,06DH,0C9H,089H,0B9H,091H
        DB      031H,0B1H,069H
TS:     DB      0,0,0,0,0,0             ; SPACE 20
        DB      0,0,21H,7FH,01,0        ; 1     31
        DB      0,23H,45H,49H,49H,31H           ; 2     32
        DB      0,42H,41H,49H,59H,66H           ; 3     33
        DB      0,0CH,14H,24H,7FH,04H           ; 4     34
        DB      0,72H,51H,51H,51H,4EH ; 5       35
        DB      0,1EH,29H,49H,49H,46H           ; 6     36
        DB      0,40H,47H,48H,50H,60H           ; 7     37
        DB      0,36H,49H,49H,49H,36H           ; 8     38
        DB      0,31H,49H,49H,4AH,3CH           ; 9     39
        DB      0,1FH,24H,44H,24H,1FH           ; A     41
        DB      0,7FH,49H,49H,49H,36H           ; B     42
        DB      0,3EH,41H,41H,41H,22H; C        43
        DB      0,7FH,41H,41H,41H,3EH; D        44
        DB      0,7FH,49H,49H,49H,41H           ; E     45
        DB      0,7FH,48H,48H,48H,40H           ; F     46
        DB      0,3EH,41H,41H,45H,47H; G        47
        DB      0,7FH,08H,08H,08H,7FH           ; H     48
        DB      0,00H,41H,7FH,41H,00H           ; I     49
        DB      0,02H,01H,01H,01H,7EH           ; J     4A
        DB      0,7FH,08H,14H,22H,41H           ; K     4B
        DB      0,7FH,01H,01H,01H,01H; L        4C
        DB      0,7FH,20H,18H,20H,7FH           ; M     4D
        DB      0,7FH,10H,08H,04H,7FH           ; N     4E
        DB      0,3EH,41H,41H,41H,3EH; O        4F
        DB      0,7FH,48H,48H,48H,30H           ; P     50
        DB      0,3EH,41H,45H,42H,3DH           ; Q     51
        DB      0,7FH,48H,4CH,4AH,31H           ; R     52
        DB      0,32H,49H,49H,49H,26H           ; S     53
NOL:    DB      0,3EH,45H,49H,51H,3EH; 0        30
        DB      0,20H,40H,4DH,50H,20H           ; ?     3F
        DB      0,3EH,41H,5DH,4DH,39H           ; @     40
        DB      0,41H,41H,41H,7FH,7FH; ]        5D
        DB      0,7FH,7FH,41H,41H,41H; [        5B
        DB      0,04H,08H,10H,08H,04H           ; ^     5E
ANGKA:  DB      0FDH,0DH,0B7H,09FH,4FH,0DBH,0FBH,8DH,0FFH,0DFH

        END
```

Teori dasar Format data Remote Control Sony

Sony mengambil standart pengkodean nama disesuaikan dengan nama perusahaannya Sony. ngkodeannya disebut Pengkodean Sony. Kode yang dikembangkan oleh perusahaan SONY ggunakan frekuensi *sub-carrier* 40 kHz dan selang waktu minimum antara 2 data – 25 ms. kasi selengkapnya adalah sebagai berikut :

Panjang data : *12 bits*

Header : 

Format data : H C_0 C_1 C_2 C_3 C_4 C_5 A_0 A_1 A_2 A_3 A_4 A_5

Jumlah kombinasi alamat = $2^6 = 64$

Jumlah kombinasi perintah = $2^6 = 64$

Keterangan : H = *Header* (awalan) data

C = *Command bits* (perintah) berjumlah 6

A = *Address bits* (alamat) berjumlah 6

Code SONY dapat mengalamati 64 jenis peralatan yang diwakili oleh kode alamat *(address* masing-masing peralatan dapat menggunakan maksimal 64 perintah yang diwakili oleh intah *(command bits).*

DÖNBERG ELECTRONICS®
TV, VIDEO AND AUDIO SPARES

Address

German
French

Sony Remote Controls in Dönberg's Warehouse

Order Code	Description	Net Price EURO
[illegible]	OUT OF PROGRAM-->N.L.A. REMOTE SONY SLV201	
[illegible]	SONY RM604 / RM605 / RM606 = IR 2140 / CP1627 MITSUBISHI	13.90
[illegible]	- IR 1481 SONY RM 613 / 613	13.90
[illegible]	SONY RM630-RM635 / RM615 / KV2066 KV2212 / KV2215 / KV188	9.90
[illegible]	Go To: RC 2484 REMOTE CONTROL SONY KVM1420U	
[illegible]	RC33 DECCA / TATUNG SONY RM615 = TPG802 REMOTE CONTROL	13.90
[illegible]	RM 689 SONY KVM1400 / KVM1400L = IR 2521 / KVA2512U / = R	13.94
[illegible]	Go To: RC 670 SONY KV211XMTU	
[illegible]	[illegible]	

IR 9123	**Go To: RC 670** RM670 / RM671 / RM672 / RM673 SONY	
9441	RM817 / RM826 SONY REMOTE KVE2522U / KVX2532U / KVC2941D	20.79
9452	REMOTE CONTROL SONY RM820 / RM694 / RM828 / RM834 / RM841	17.90
9871	REMOTE CONTROL SONY KV29X52 KV25X5L / RM836 / RM839 / RM8	16.90
140c	**Go To: RC 664** REMOTE SONY KV2092 CPC	
2484	RM686 / RM685 / 681 / RM694 / RM683 RM682 / RM681 / RM656	13.90
09/HQ	RM610 / RM610A / RM611 SONY KV2212 = IR 9243 REMOTE CONTR	14.90
19	RM832 REMOTE CONTROL SONY KVX2181D KVS3412 / KPS4112U / K	14.90
/HQ	RM833 REMOTE CONTROL SONY KVX2182U / KV25T1 / KV25F3 = RM	14.90
/HQ	REMOTE CONTROL SONY = RM842 / RM846 / RM864	12.90
34/HQ	REMOTE CONTROL SONY KV21X5L = RM883 = 147576511 = RM891 /	12.90
1	SONY REMOTE CONTROL TEXT RM664 / KV19XML / KV2092 / KV216	13.93
70	RM670 SONY REMOTE CONTROL = RC505 / HQ KVM2120L / KVM2131	13.93
/HQ	REMOTE CONTROL SONY VCR RMTV166 / RMTV166B / SLV210 = SLV	14.90
	147654512 ORIGINAL SONY REMOTE CONTROL	119.90
	SONY REMOTE CONTROL GENUINE	38.03
041	**Go To: RC 664** REMOTE CONTROL SONY KV2092	
367	**Go To: RC 522/HQ** REMOTE CONTROL SONY	

RM 661A	**Go To: RC 664** SONY 21XRL REMOTE GENUINE	
RM 670	**Go To: RC 670** SONY KVX25TL / KVM2151	
RM 671	**Go To: RC 670** SONY KV21XML / KV211XML	
RM 673	A1470844A REMOTE CONTROL SONY KVC27TD	124.90
RM 676	ORIGINAL SONY REMOTE	80.90
RM 677	SONY REMOTE CONTROL REPLACEMENT	12.99
RM 681	ORIGINAL REMOTE CONTROL SONY KVX2932U UNIVERSAL SONY	49.90
RM 687C	SONY REMOTE CONTROL REPLACEMENT	12.99
RM 68M	1465/9611 REMOTE CONTROL SONY KVX2132U / KVX2131A / KVX29	47.90
RM [illegible]	**Go To: IR 3650** REMOTE CONTROL SONY	
RM [illegible]	REMOTE CONTROL SONY GENUINE KVM2140L / KVM2141L = 9948009	63.90
RM [illegible]	**Go To: RC 519** SONY KVM2150U / KVM2150L / KVM2151U K	
RM [illegible]	SONY REMOTE CONTROL REPLACEMENT	12.99
RM [illegible]	REMOTE CONTROL SONY KVM112C = 994800915 / RMS04B	42.90
RM [illegible]	REMOTE CONTROL SONY GENUINE KVX2962U KVX2562 / KVB2913E =	44.90
RM [illegible]	146770611 REMOTE CONTROL SONY KVM2541 / KVX2582 / KVX2902	44.90
RM [illegible]	SONY REMOTE CONTROL REPLACEMENT	12.99
RM [illegible]	REMOTE CONTROL SONY KV32WS2U = 147369211 / KV32WF1U / KV2	58.90

RM 869	REMOTE CONTROL SONY REPLACEMENT = RM952 = 141816312	56.90
RM 877	141847623 REMOTE CONTROL SONY KV29LF35B	20.90
RM 887	141847611 REPLACEMENT REMOTE SONY KV32FX20A / KV21LT1B /	16.90
RM 889	REMOTE CONTROL SONY KV14LM1	24.90
RM 936	147717611 REMOTE CONTROL SONY KV32FQ80 / KV32FQ80B KV32FQ	79.90
RM 937	147715511 REMOTE CONTROL SONY KV32FX66B / 147715512	89.90
RM 938	147725912 REMOTE CONTROL SONY KV36FS76B / KV32FQ70 = 1477	44.90
RM 947	ORIGINAL SONY REMOTE CONTROL	19.99
RM 949	ORIGINAL SONY REMOTE CONTROL	19.99
RM PJM10	REMOTE CONTROL SONY VPL-CX11 PROJECTOR = 147674322	289.90
RM [illegible]	OUT OF PROGRAM-->N.L.A. REMOTE CONTROL SONY ST-S707ES 146	
RM [illegible]	ORIGINAL SONY UNIVERSAL MULTIBRAND REMOTE CONTROL, TEXT,	9.99
RMC 611	147536511 REMOTE CONTROL SONY KV21V6U	31.90
RMED 007	147984711 REMOTE CONTROL SONY KDF50E2010	12.90
RMJ 2	147655521 ORIGINAL REMOTE CONTROL SONY VPLCS3 / VPLCS4 PR	89.90
RMSS 373	141855411 REMOTE CONTROL SONY DHCMD373	60.90
RMST 1	REMOTE CONTROL SONY HCDT1 = 147327111	43.90
RMT 223	A6765943A REMOTE CONTROL SONY SLHF950ES	159.90

RMT 257	A6767794A REMOTE CONTROL SONY SLV 401	113.97
RMT 53A	A6768141A REMOTE CONTROL SONY SLV353UB	101.29
RMT 80?	891757090 REMOTE CONTROL SONY DSR200AP	120.03
RMT 81?	147581512 REMOTE CONTROL SONY DCRIP7E = 147764121	59.90
RMT 831	REMOTE CONTROL SONY DCRHC85E = 147849541 = DCRHC44E	39.90
RMT CD30	REMOTE CONTROL SONY CFDS33L = 891758590	18.92
RMT CD33A2	REMOTE CONTROL SONY CFDS33L = 891760390	63.36
RMT V10?	SONY REMOTE CONTROL SLV270 / 310	88.31
RMT V10?	REMOTE CONTROL SONY SLE15 GENUINE	53.02
?	146551411 REMOTE CONTROL SONY SLV373	126.85
?	146573911 REMOTE CONTROL SONY SLV315E	88.72
?	146573921 REMOTE CONTROL SONY VCR SLV325	75.90
RMTV 113	REMOTE SONY CONTROL SLV625 = RMTV168 = 147321712	119.90
RMTV 11?	146573931 REMOTE CONTROL SONY SLV225EI / SLV225UB	119.90
RMTV 11?	REMOTE CONTROL SONY SLVE7 146691811	101.58
RMTV 145A	145775731 REMOTE CONTROL SONY RS101P	98.90
RMTV 147A	147315521 REMOTE CONTROL SONY SLVE200EX	63.22
RMTV 197	REMOTE CONTROL SONY SLVE720 ORIGINAL / SLVE720B = RMTV197	59.90

[x]	RMTV 252A	146525231 REMOTE CONTROL SONY SLV255	31.58
[x]	RMTV 398K	141878211 REMOTE CONTROL SONY SLVSE700 ICEK	99.90
[x]	RMTV 402	REMOTE CONTRO, SONY = RMT-V402	89.90
[x]	RMTV 405	REMOTE CONTROL SONY SLVSE220	31.90
[x]	RMY 114A	OUT OF PROGRAM-->N.L.A. REMOTE CONTROL SONY KP61XBR28 = 1	
[x]	RMY 133	147322411 SONY 32KX1000 RMY133	120.00
[x]	RX 817	1466579711 REMOTE CONTROL SONY KVE2922U	84.95
[x]	RV-M2511	SONY REMOTE KV-M2511 GENUINE	43.81
[*]	REM 1	147369311 REPLACEMENT REMOTE CONTROL SONY KV29X1L = 14736	15.90
[*]	REM 9	Go To: SO REM 15 147613311 SONY REMOTE CONTROL MHCBX2	
[*]	REM 11	147650311 SONY REMOTE CONTROL RM-SR210 / MHCRG60	25.27
[x]	REM 12	147364811 REMOTE CONTROL SONY MHCV800 = RMV800	83.68
[x]	REM 13	891764690 REMOTE CONTROL SONY CMTSD1 / CMTSD3 / RMSSD1 M	120.90
[x]	REM 14	OUT OF PROGRAM-->N.L.A. SONY CMTCP1 141829911 REMOTE CONT	
[x]	REM 15	147618711 REMOTE CONTROL SONY MHCBX6AV = 147613311	89.90
[x]	REM 16	RM932 SONY REMOTE CONTROL KV28LS35 / KV29LS35B / KV32LS35	32.90
[x]	REM 17	RMU302 SONY REMOTE CONTROL STRDE225	70.90
[x]	REM 18	146712311 REMOTE CONTROL SONY CDPC365	41.90

[x]	REM 2	147348761 REMOTE CONTROL SONY SLVE710EX	63.90
[x]	REM 20	891759890 REMOTE CONTROL SONY PMCD307L / RMT-C305A	64.90
[x]	REM 21	147348711 REMOTE CONTROL SONY SLVE700UX = RMTV186	79.90
[x]	REM 22	141898821 REMOTE CONTROL SONY DVPS336 = RMTD115P	54.90
[x]	REM 23	147556321 SONY REMOTE CONTROL SLVE730 RMTV223A	81.90
[x]	REM 24	147640611 REMOTE CONTROL SONY SLVSE710 RMTV288	42.90
[x]	REM 25	147678411 REMOTE CONTROL SONY DAVS500 SOUND AROUND SYSTEM	86.90
[x]	REM 26	147651311 REMOTE CONTROL SONY MHCRG20 / HCDRG220 RM-SR2	42.90
[x]	REM 27	146534211 REMOTE CONTROL SONY MHC1500 / RMS100	44.90
[x]	REM 28	146724411 REMOTE CONTROL SONY CDPCX100	189.90
[x]	REM 29	891753090 REMOTE CONTROL SONY PMC303L RMTC303A	84.90
[x]	REM 3	REMOTE CONTROL SONY SLVE250EY = RMTV140P / 147316711 SLVE	73.51
[x]	REM 30	147716911 REMOTE CONTROL SONY DVPNS305 = RMT-D141P	20.90
[x]	REM 31	147734011 REMOTE CONTROL SONY DVPPQ1	28.90
[x]	REM 32	A4410091A REMOTE CONTROL SONY STJX520 TUNER = RMS520	189.90
[x]	REM 33	147651411 REMOTE CONTROL SONY RCDW3 CD RECORDER - RMR5C	69.90
[x]	REM 34	147655521 REMOTE SONY VPLCS4 DIGITAL PROJECTOR = RMPJ2	99.90
[x]			

[x]	REM 36	147737011 REMOTE CONTROL SONY HCDS550 DVD = RMSS880	42.99
[x]	REM 37	147780411 REMOTE CONTROL SONY RDRGX7 / RDRGX3 = RMT-D203P	115.00
[x]	REM 38	988504308 REMOTE CONTROL SONY SLVD950	57.90
[x]	REM 39	A3250959A REMOTE CONTROL SONY PMCR35L HI-FI	45.90
[x]	REM 4	146797711 REMOTE CONTROL SONY MHCC505	34.28
[x]	REM 40	147733211 REMOTE CONTROL SONY DAVS400 / HCDS400 = RMSS400	53.90
[x]	REM 41	147727111 REMOTE CONTROL SONY SLVSE7201	29.90
[x]	REM 42	147660511 REMOTE CONTROL SONY DVP-NS400D = RMTD128P	62.90
[x]	REM 43	988506939 REMOTE CONTROL SONY DAV SB100 HOME CINEAM SYSTE	74.90
[x]	REM 44	141800831 REMOTE CONTROL SONY SLVSE20	44.90
[x]	REM 45	147881511 REMOTE CONTROL SONY KLV30HR3 = RMY1108	15.90
[x]	REM 46	147789811 REMOTE CONTROL SONY TRV22BE	51.90
[x]	REM 47	147675411 REMOTE CONTROL SONY HCDCP500MD = RMSCP500	49.90
[x]	REM 48	147928911 REMOTE CONTROL SONY DVD RDX-HX710 / RDR-HX510 =	59.90
[x]	REM 49	147711014 REMOTE CONTROL SONY CDXM630 = 147711012 / 14771	27.90
[x]	REM 5	141849911 REMOTE CONTROL SONY MHCRXD6AV	59.90
[x]	REM 50	147727411 REMOTE CONTROL SONY VSLV-SE820B VIDEO RECORDER	29.90
[x]	REM 51	147636911 REMOTE CONTROL SONY SLVX831	26.90

[x]	147872221 REMOTE CONTROL SONY RDRGX3C0 = RMT-205P	44.90
[x]	147691711 REMOTE CONTROL SONY CMTEP50 / RMSEP50	88.90
[x]	147772211 REMOTE CONTROL SONY DVPNS330 DVD PLAYER = RMT-D	11.90
[x]	141029411 REMOTE CONTROL SONY STR-DE235 / RMU303	69.90
[x]	146535811 REMOTE CONTROL SONY RMS130	49.90
[x]	147861412 ORIGINAL REMOTE CONTROL SONY KV28HS15	15.90
[x]	79078083 REMOTE CONTROL SONY DVD SD9500 = SER0057	36.90
[x]	147936311 REMOTE CONTROL SONY RDRHXD710 DVD	89.90
[x]	994800913 REMOTE CONTROL SONY = RMS04 = RM862 / KV25F3 KV	57.14
[x]	147654611 REMOTE CONTROL SONY CDX-M670 = RMX111	44.90
[x]	RMX96 REMOTE CONTROL SONY = 141881271	69.90
[x]	147508631 REMOTE CONTROL SONY DVPS7000 = RMT-D100E	189.90
[x]	147066311 REMOTE CONTROL SONY CMTCP100	24.90
[x]	147654621 REMOTE CONTROL SONY WX7700	97.90
[x]	988509569 REMOTE CONTROL SONY RDRVX420 = RMT-D224P	68.90
[x]	147557211 REMOTE CONTROL SONY HCDRXD5	41.77
[x]	147527211 REMOTE CONTROL SONY CFDZW16CL ORMT-CZW200AD	49.90
[x]	146777711 REMOTE CONTROL SONY CDPCX151 / RMDX151	49.90

[x] SONY REM 02	147576751 REMOTE CONTROL SONY SLVF990N = RMTV240D	89.90
[x] UNI 02	PREPROGRAMMED UNIVERSAL REMOTE CONTROL FOR SONY TV'S TEXT	12.99
[x] US 201	SONY KV2202 REMOTE CONTROL - RTP22	21.94

156 types

Last update: 20 - Aug - 2007

eatures

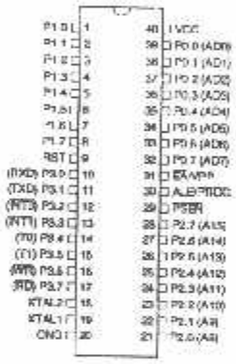
- Compatible with MCS-51™ Products
- K Bytes of In-System Reprogrammable Flash Memory
  - Endurance: 1,000 Write/Erase Cycles
- ully Static Operation: 0 Hz to 24 MHz
- hree-level Program Memory Lock
- 28 x 8-bit Internal RAM
- 2 Programmable I/O Lines
- wo 16-bit Timer/Counters
- ix Interrupt Sources
- rogrammable Serial Channel
- *ow-power Idle and Power-down Modes*

escription

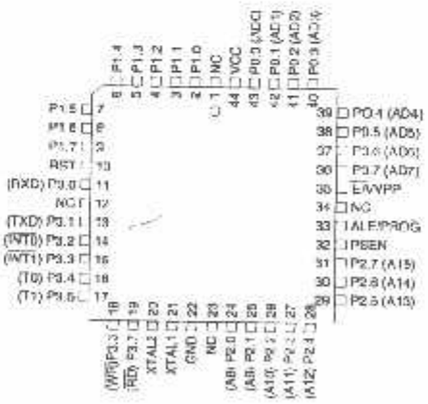
AT89C51 is a low-power, high-performance CMOS 8-bit microcomputer with 4K es of Flash programmable and erasable read only memory (PEROM). The device anufactured using Atmel's high-density nonvolatile memory technology and is patible with the industry-standard MCS-51 instruction set and pinout. The on-chip sh allows the program memory to be reprogrammed in-system or by a conven- al nonvolatile memory programmer. By combining a versatile 8-bit CPU with Flash monolithic chip, the Atmel AT89C51 is a powerful microcomputer which provides ghly-flexible and cost-effective solution to many embedded control applications.

Configurations

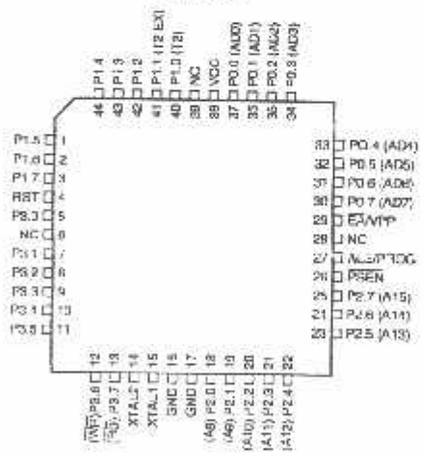
PDIP



PLCC



POFP/TQFP

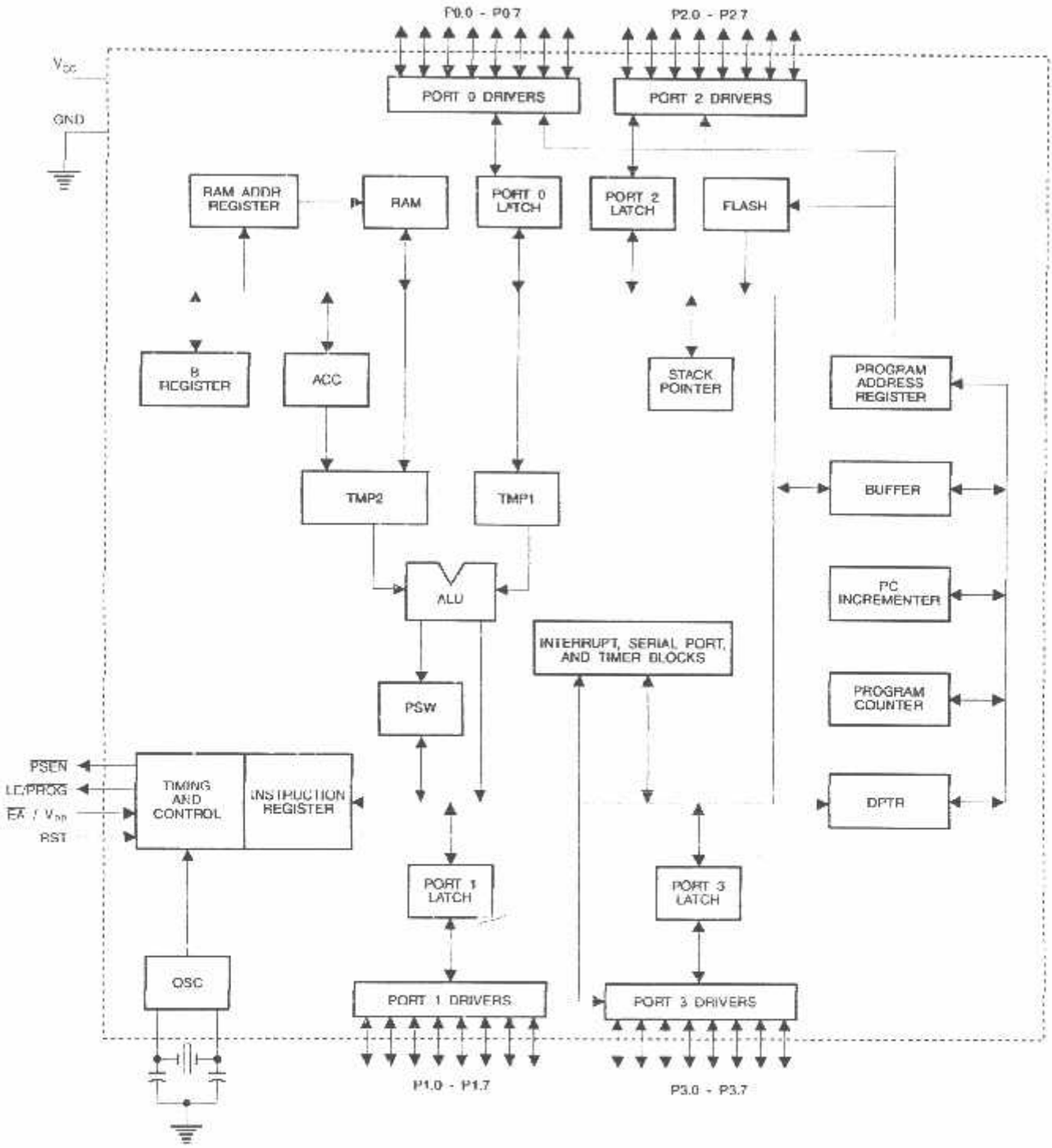


8-bit Microcontroller with 4K Bytes Flash

AT89C51

Rev. 0265G–02/00

Block Diagram



The AT89C51 provides the following standard features: 4K bytes of Flash, 128 bytes of RAM, 32 I/O lines, two 16-bit timer/counters, a five vector two-level interrupt architecture, a full duplex serial port, on-chip oscillator and clock circuitry. In addition, the AT89C51 is designed with static logic for operation down to zero frequency and supports two software selectable power saving modes. The Idle Mode stops the CPU while allowing the RAM, timer/counters, serial port and interrupt system to continue functioning. The Power-down Mode saves the RAM contents but freezes the oscillator disabling all other chip functions until the next hardware reset.

Pin Description

VCC

Supply voltage.

GND

Ground.

Port 0

Port 0 is an 8-bit open-drain bi-directional I/O port. As an output port, each pin can sink eight TTL inputs. When 1s are written to port 0 pins, the pins can be used as high-impedance inputs.

Port 0 may also be configured to be the multiplexed low-order address/data bus during accesses to external program and data memory. In this mode P0 has internal pullups.

Port 0 also receives the code bytes during Flash programming, and outputs the code bytes during program verification. External pullups are required during program verification.

Port 1

Port 1 is an 8-bit bi-directional I/O port with internal pullups. The Port 1 output buffers can sink/source four TTL inputs. When 1s are written to Port 1 pins they are pulled high by the internal pullups and can be used as inputs. As inputs, Port 1 pins that are externally being pulled low will source current (I_{IL}) because of the internal pullups.

Port 1 also receives the low-order address bytes during Flash programming and verification.

Port 2

Port 2 is an 8-bit bi-directional I/O port with internal pullups. The Port 2 output buffers can sink/source four TTL inputs. When 1s are written to Port 2 pins they are pulled high by the internal pullups and can be used as inputs. As inputs, Port 2 pins that are externally being pulled low will source current (I_{IL}) because of the internal pullups.

Port 2 emits the high-order address byte during fetches from external program memory and during accesses to external data memory that use 16-bit addresses (MOVX @ DPTR). In this application, it uses strong internal pullups when emitting 1s. During accesses to external data memory that use 8-bit addresses (MOVX @ RI), Port 2 emits the contents of the P2 Special Function Register.

Port 2 also receives the high-order address bits and some control signals during Flash programming and verification.

Port 3

Port 3 is an 8-bit bi-directional I/O port with internal pullups. The Port 3 output buffers can sink/source four TTL inputs. When 1s are written to Port 3 pins they are pulled high by the internal pullups and can be used as inputs. As inputs, Port 3 pins that are externally being pulled low will source current (I_{IL}) because of the pullups.

Port 3 also serves the functions of various special features of the AT89C51 as listed below:

Port Pin	Alternate Functions
P3.0	RXD (serial input port)
P3.1	TXD (serial output port)
P3.2	$\overline{INT0}$ (external interrupt 0)
P3.3	$\overline{INT1}$ (external interrupt 1)
P3.4	T0 (timer 0 external input)
P3.5	T1 (timer 1 external input)
P3.6	$\overline{WR}$ (external data memory write strobe)
P3.7	$\overline{RD}$ (external data memory read strobe)

Port 3 also receives some control signals for Flash programming and verification.

RST

Reset input. A high on this pin for two machine cycles while the oscillator is running resets the device.

ALE/$\overline{PROG}$

Address Latch Enable output pulse for latching the low byte of the address during accesses to external memory. This pin is also the program pulse input ($\overline{PROG}$) during Flash programming.

In normal operation ALE is emitted at a constant rate of 1/6 the oscillator frequency, and may be used for external timing or clocking purposes. Note, however, that one ALE

ılse is skipped during each access to external Data emory.

desired, ALE operation can be disabled by setting bit 0 of FR location 8EH. With the bit set, ALE is active only dur- g a MOVX or MOVC instruction. Otherwise, the pin is eakly pulled high. Setting the ALE-disable bit has no fect if the microcontroller is in external execution mode.

$\overline{\text{SEN}}$

ogram Store Enable is the read strobe to external pro- am memory.

hen the AT89C51 is executing code from external pro- am memory, $\overline{\text{PSEN}}$ is activated twice each machine cle, except that two $\overline{\text{PSEN}}$ activations are skipped during ch access to external data memory.

ı/VPP

ternal Access Enable. $\overline{\text{EA}}$ must be strapped to GND in ler to enable the device to fetch code from external pro- ım memory locations starting at 0000H up to FFFFH. te, however, that if lock bit 1 is programmed, $\overline{\text{EA}}$ will be rnally latched on reset.

should be strapped to V_{CC} for internal program cutions.

s pin also receives the 12-volt programming enable volt- e (V_{PP}) during Flash programming, for parts that require volt V_{PP}.

ıL1

ut to the inverting oscillator amplifier and input to the rnal clock operating circuit.

ıL2

put from the inverting oscillator amplifier.

cillator Characteristics

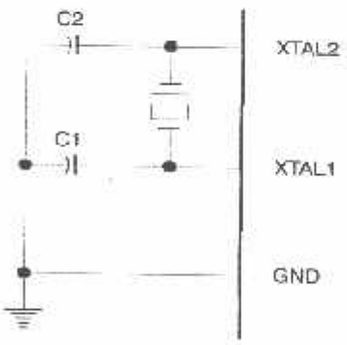
ıL1 and XTAL2 are the input and output, respectively, n inverting amplifier which can be configured for use as on-chip oscillator, as shown in Figure 1. Either a quartz tal or ceramic resonator may be used. To drive the ce from an external clock source, XTAL2 should be left unconnected while XTAL1 is driven as shown in Figure 2. There are no requirements on the duty cycle of the external clock signal, since the input to the internal clocking circuitry is through a divide-by-two flip-flop, but minimum and maximum voltage high and low time specifications must be observed.

Idle Mode

In idle mode, the CPU puts itself to sleep while all the on-chip peripherals remain active. The mode is invoked by software. The content of the on-chip RAM and all the special functions registers remain unchanged during this mode. The idle mode can be terminated by any enabled interrupt or by a hardware reset.

It should be noted that when idle is terminated by a hard ware reset, the device normally resumes program execution, from where it left off, up to two machine cycles before the internal reset algorithm takes control. On-chip hardware inhibits access to internal RAM in this event, but access to the port pins is not inhibited. To eliminate the possibility of an unexpected write to a port pin when Idle is terminated by reset, the instruction following the one that invokes Idle should not be one that writes to a port pin or to external memory.

Figure 1. Oscillator Connections

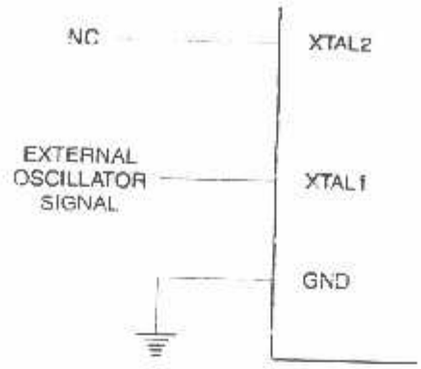


Note: C1, C2 = 30 pF ± 10 pF for Crystals
= 40 pF ± 10 pF for Ceramic Resonators

ıtus of External Pins During Idle and Power-down Modes

de	Program Memory	ALE	$\overline{\text{PSEN}}$	PORT0	PORT1	PORT2	PORT3
)	Internal	1	1	Data	Data	Data	Data
	External	1	1	Float	Data	Address	Data
ver-down	Internal	0	0	Data	Data	Data	Data
ver-down	External	0	0	Float	Data	Data	Data

Figure 2. External Clock Drive Configuration



Power-down Mode

In the power-down mode, the oscillator is stopped, and the instruction that invokes power-down is the last instruction executed. The on-chip RAM and Special Function Registers retain their values until the power-down mode is terminated. The only exit from power-down is a hardware reset. Reset redefines the SFRs but does not change the on-chip RAM. The reset should not be activated before V_{CC} is restored to its normal operating level and must be held active long enough to allow the oscillator to restart and stabilize.

Program Memory Lock Bits

On the chip are three lock bits which can be left unprogrammed (U) or can be programmed (P) to obtain the additional features listed in the table below.

When lock bit 1 is programmed, the logic level at the $\overline{EA}$ pin is sampled and latched during reset. If the device is powered up without a reset, the latch initializes to a random value, and holds that value until reset is activated. It is necessary that the latched value of $\overline{EA}$ be in agreement with the current logic level at that pin in order for the device to function properly.

Lock Bit Protection Modes

	Program Lock Bits			
	LB1	LB2	LB3	Protection Type
1	U	U	U	No program lock features
2	P	U	U	MOVC instructions executed from external program memory are disabled from fetching code bytes from internal memory, $\overline{EA}$ is sampled and latched on reset, and further programming of the Flash is disabled
3	P	P	U	Same as mode 2, also verify is disabled
4	P	P	P	Same as mode 3, also external execution is disabled

ogramming the Flash

AT89C51 is normally shipped with the on-chip Flash mory array in the erased state (that is, contents = FFH) l ready to be programmed. The programming interface epts either a high-voltage (12-volt) or a low-voltage c) program enable signal. The low-voltage program- g mode provides a convenient way to program the 89C51 inside the user's system, while the high-voltage gramming mode is compatible with conventional third- y Flash or EPROM programmers.

AT89C51 is shipped with either the high-voltage or -voltage programming mode enabled. The respective side marking and device signature codes are listed in following table.

	V_{PP} = 12V	V_{PP} = 5V
-Side Mark	AT89C51 xxxx yyww	AT89C51 xxxx-5 yyww
nature	(030H) = 1EH (031H) = 51H (032H) =F FH	(030H) = 1EH (031H) = 51H (032H) = 05H

AT89C51 code memory array is programmed byte-by- in either programming mode. *To program any non- k byte in the on-chip Flash Memory, the entire memory t be erased using the Chip Erase Mode.*

gramming Algorithm: Before programming the 3C51, the address, data and control signals should be p according to the Flash programming mode table and e 3 and Figure 4. To program the AT89C51, take the ving steps.

nput the desired memory location on the address nes.

nput the appropriate data byte on the data lines.

Activate the correct combination of control signals.

Raise $\overline{EA}/V_{PP}$ to 12V for the high-voltage program- ning mode.

Pulse ALE/$\overline{PROG}$ once to program a byte in the Flash array or the lock bits. The byte-write cycle is self-timed and typically takes no more than 1.5 ms. Repeat steps 1 through 5, changing the address and data for the entire array or until the end of the object file is reached.

Data Polling: The AT89C51 features $\overline{Data}$ Polling to indicate the end of a write cycle. During a write cycle, an attempted read of the last byte written will result in the complement of the written datum on PO.7. Once the write cycle has been completed, true data are valid on all outputs, and the next cycle may begin. $\overline{Data}$ Polling may begin any time after a write cycle has been initiated.

Ready/$\overline{Busy}$: The progress of byte programming can also be monitored by the RDY/$\overline{BSY}$ output signal. P3.4 is pulled low after ALE goes high during programming to indicate BUSY. P3.4 is pulled high again when programming is done to indicate READY.

Program Verify: If lock bits LB1 and LB2 have not been programmed, the programmed code data can be read back via the address and data lines for verification. The lock bits cannot be verified directly. Verification of the lock bits is achieved by observing that their features are enabled.

Chip Erase: The entire Flash array is erased electrically by using the proper combination of control signals and by holding ALE/$\overline{PROG}$ low for 10 ms. The code array is written with all "1"s. The chip erase operation must be executed before the code memory can be re-programmed.

Reading the Signature Bytes: The signature bytes are read by the same procedure as a normal verification of locations 030H, 031H, and 032H, except that P3.6 and P3.7 must be pulled to a logic low. The values returned are as follows.

(030H) = 1EH indicates manufactured by Atmel
(031H) = 51H indicates 89C51
(032H) = FFH indicates 12V programming
(032H) = 05H indicates 5V programming

Programming Interface

Every code byte in the Flash array can be written and the entire array can be erased by using the appropriate combination of control signals. The write operation cycle is self-timed and once initiated, will automatically time itself to completion.

All major programming vendors offer worldwide support for the Atmel microcontroller series. Please contact your local programming vendor for the appropriate software revision.

ash Programming Modes

ode		RST	PSEN	ALE/PROG	EA/V_{PP}	P2.6	P2.7	P3.6	P3.7
rite Code Data		H	L		H/12V	L	H	H	H
ead Code Data		H	L	H	H	L	L	H	H
rite Lock	Bit - 1	H	L		H/12V	H	H	H	H
	Bit - 2	H	L		H/12V	H	H	L	L
	Bit - 3	H	L		H/12V	H	L	H	L
ip Erase		H	L	(1)	H/12V	H	L	L	L
ad Signature Byte		H	L	H	H	L	L	L	L

e: 1. Chip Erase requires a 10 ms PROG pulse.

ure 3. Programming the Flash

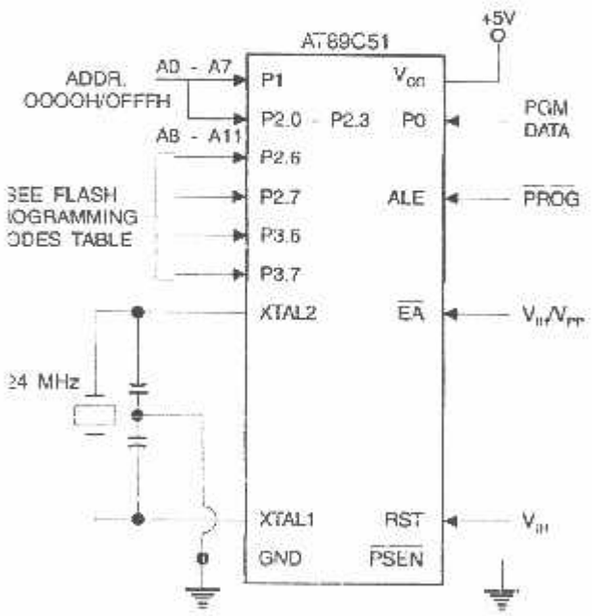
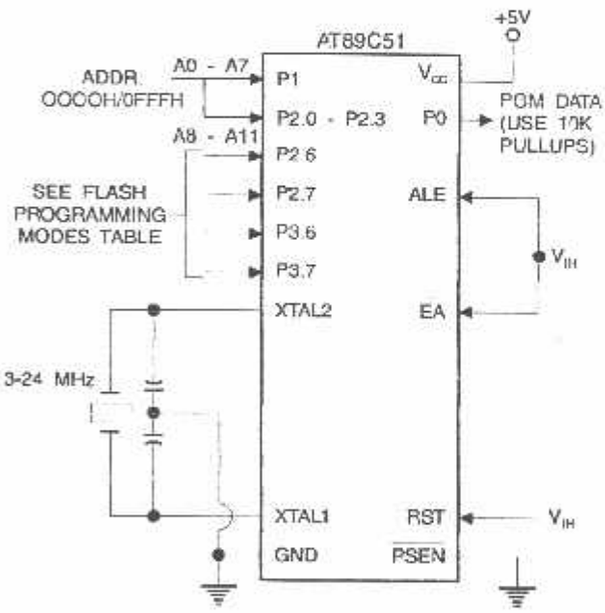
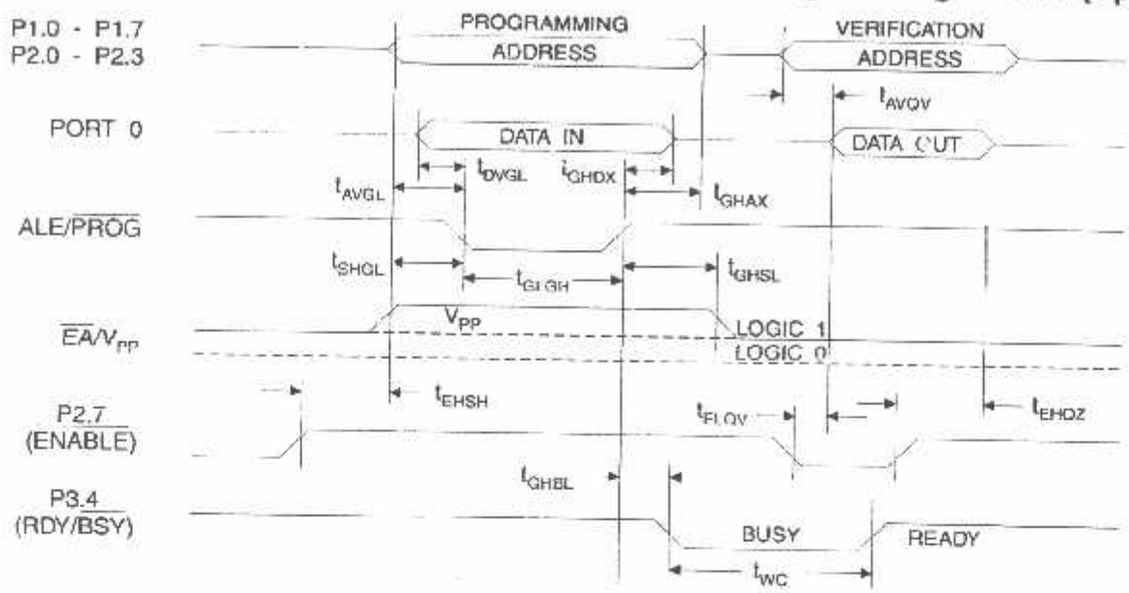


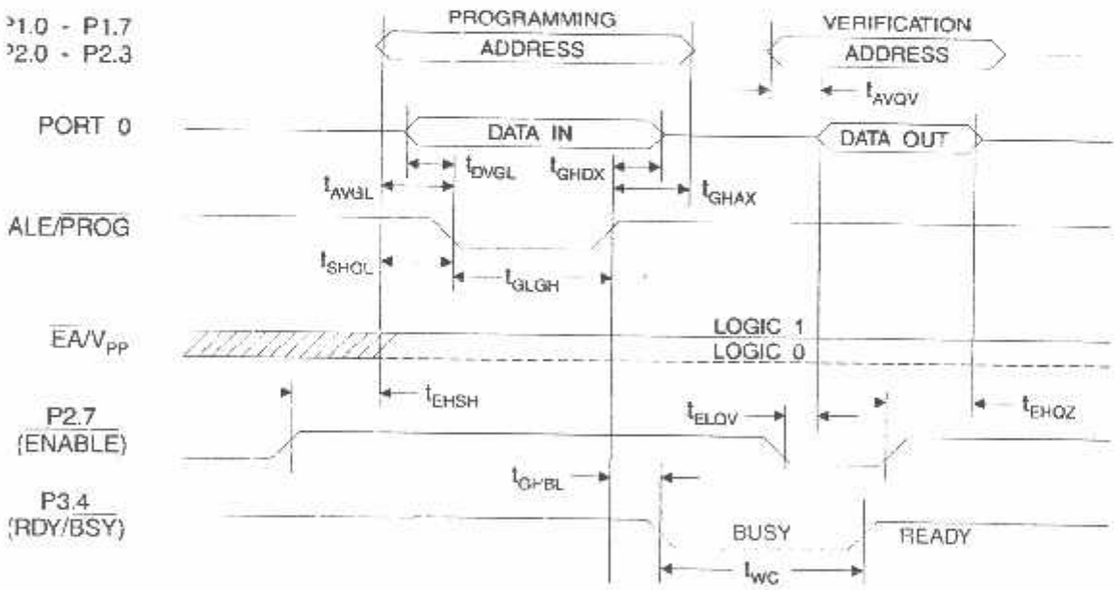
Figure 4. Verifying the Flash



ısh Programming and Verification Waveforms - High-voltage Mode (V_{PP} = 12V)



sh Programming and Verification Waveforms - Low-voltage Mode (V_{PP} = 5V)



ash Programming and Verification Characteristics

= 0°C to 70°C, V_{CC} = 5.0 ± 10%

ymbol	Parameter	Min	Max	Units
$_{PP}$[1]	Programming Enable Voltage	11.5	12.5	V
$_{P}$[1]	Programming Enable Current		1.0	mA
$_{CLCL}$	Oscillator Frequency	3	24	MHz
AVGL	Address Setup to PROG Low	$48t_{CLCL}$		
GHAX	Address Hold After PROG	$48t_{CLCL}$		
DVGL	Data Setup to PROG Low	$48t_{CLCL}$		
GHDX	Data Hold After PROG	$48t_{CLCL}$		
EHSH	P2.7 (ENABLE) High to V_{PP}	$48t_{CLCL}$		
SHGL	V_{PP} Setup to PROG Low	10		µs
GHSL[1]	V_{PP} Hold After PROG	10		µs
GLGH	PROG Width	1	110	µs
AVQV	Address to Data Valid		$48t_{CLCL}$	
ELQV	ENABLE Low to Data Valid		$48t_{CLCL}$	
EHQZ	Data Float After ENABLE	0	$48t_{CLCL}$	
GHBL	PROG High to BUSY Low		1.0	µs
	Byte Write Cycle Time		2.0	ms

1. Only used in 12-volt programming mode.

Absolute Maximum Ratings*

Operating Temperature	-55°C to +125°C
Storage Temperature	-65°C to +150°C
Voltage on Any Pin with Respect to Ground	-1.0V to +7.0V
Maximum Operating Voltage	6.6V
DC Output Current	15.0 mA

*NOTICE: Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and *functional* operation of the device at these or any other conditions beyond those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC Characteristics

T_A = -40°C to 85°C, V_{CC} = 5.0V ± 20% (unless otherwise noted)

Symbol	Parameter	Condition	Min	Max	Units
V_{IL}	Input Low-voltage	(Except $\overline{EA}$)	-0.5	0.2 V_{CC} - 0.1	V
V_{IL1}	Input Low-voltage ($\overline{EA}$)		-0.5	0.2 V_{CC} - 0.3	V
V_{IH}	Input High-voltage	(Except XTAL1, RST)	0.2 V_{CC} + 0.9	V_{CC} + 0.5	V
V_{IH1}	Input High-voltage	(XTAL1, RST)	0.7 V_{CC}	V_{CC} + 0.5	V
V_{OL}	Output Low-voltage[1] (Ports 1,2,3)	I_{OL} = 1.6 mA		0.45	V
V_{OL1}	Output Low-voltage[1] (Port 0, ALE, $\overline{PSEN}$)	I_{OL} = 3.2 mA		0.45	V
V_{OH}	Output High-voltage (Ports 1,2,3, ALE, $\overline{PSEN}$)	I_{OH} = -60 µA, V_{CC} = 5V ± 10%	2.4		V
		I_{OH} = -25 µA	0.75 V_{CC}		V
		I_{OH} = -10 µA	0.9 V_{CC}		V
V_{OH1}	Output High-voltage (Port 0 in External Bus Mode)	I_{OH} = -800 µA, V_{CC} = 5V ± 10%	2.4		V
		I_{OH} = -300 µA	0.75 V_{CC}		V
		I_{OH} = -80 µA	0.9 V_{CC}		V
I_{IL}	Logical 0 Input Current (Ports 1,2,3)	V_{IN} = 0.45V		-50	µA
I_{TL}	Logical 1 to 0 Transition Current (Ports 1,2,3)	V_{IN} = 2V VCC = 5V ± 10%		-650	µA
I_{LI}	Input Leakage Current (Port 0, $\overline{EA}$)	0.45 < V_{IN} < V_{CC}		±10	µA
R_{RST}	Reset Pull-down Resistor		50	300	KΩ
C_{IO}	Pin Capacitance	Test Freq. = 1 MHz, T_A = 25°C		10	pF
I_{CC}	Power Supply Current	Active Mode, 12 MHz		20	mA
		Idle Mode, 12 MHz		5	mA
	Power-down Mode[2]	V_{CC} = 6V		100	µA
		V_{CC} = 3V		40	µA

Notes:
1. Under steady state (non-transient) conditions, I_{OL} must be externally limited as follows:
   Maximum I_{OL} per port pin: 10 mA
   Maximum I_{OL} per 8-bit port: Port 0: 26 mA
   Ports 1, 2, 3: 15 mA
   Maximum total I_{OL} for all output pins: 71 mA
   If I_{OL} exceeds the test condition, V_{OL} may exceed the related specification. Pins are not guaranteed to sink current greater than the listed test conditions.
2. Minimum V_{CC} for Power-down is 2V.

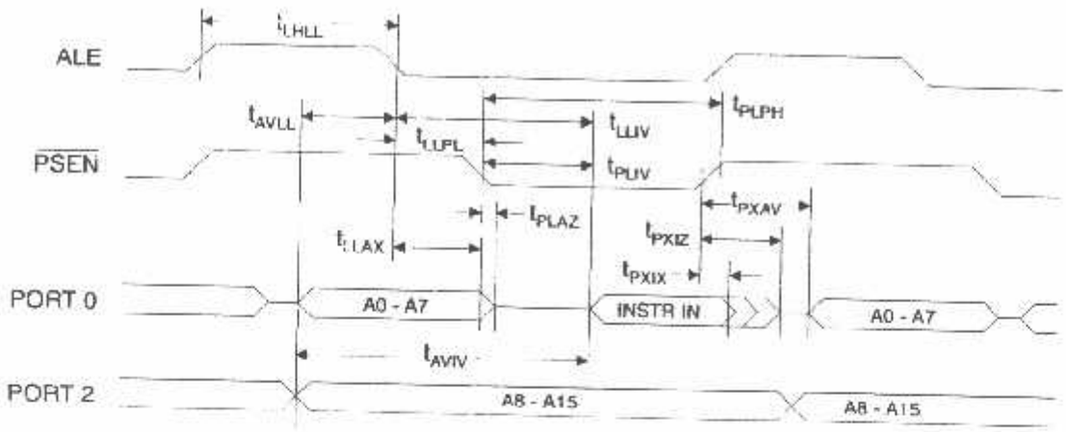
Characteristics

er operating conditions, load capacitance for Port 0, ALE/$\overline{PROG}$, and $\overline{PSEN}$ = 100 pF; load capacitance for all other uts = 80 pF.

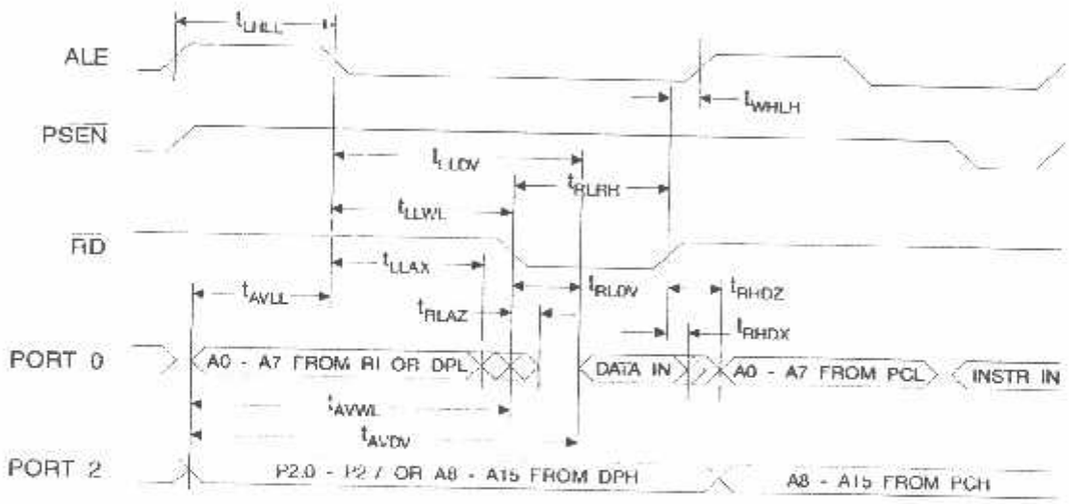
ternal Program and Data Memory Characteristics

mbol	Parameter	12 MHz Oscillator		16 to 24 MHz Oscillator		Units
		Min	Max	Min	Max	
CLCL	Oscillator Frequency			0	24	MHz
L	ALE Pulse Width	127		$2t_{CLCL}$-40		ns
L	Address Valid to ALE Low	43		t_{CLCL}-13		ns
X	Address Hold After ALE Low	48		t_{CLCL}-20		ns
	ALE Low to Valid Instruction In		233		$4t_{CLCL}$-65	ns
L	ALE Low to $\overline{PSEN}$ Low	43		t_{CLCL}-13		ns
H	$\overline{PSEN}$ Pulse Width	205		$3t_{CLCL}$-20		ns
	$\overline{PSEN}$ Low to Valid Instruction In		145		$3t_{CLCL}$-45	ns
	Input Instruction Hold After $\overline{PSEN}$	0		0		ns
	Input Instruction Float After $\overline{PSEN}$		59		t_{CLCL}-10	ns
V	$\overline{PSEN}$ to Address Valid	75		t_{CLCL}-8		ns
	Address to Valid Instruction In		312		$5t_{CLCL}$-55	ns
	$\overline{PSEN}$ Low to Address Float		10		10	ns
H	$\overline{RD}$ Pulse Width	400		$6t_{CLCL}$-100		ns
H	$\overline{WR}$ Pulse Width	400		$6t_{CLCL}$-100		ns
	$\overline{RD}$ Low to Valid Data In		252		$5t_{CLCL}$-90	ns
X	Data Hold After $\overline{RD}$	0		0		ns
Z	Data Float After $\overline{RD}$		97		$2t_{CLCL}$-28	ns
	ALE Low to Valid Data In		517		$8t_{CLCL}$-150	ns
V	Address to Valid Data In		585		$9t_{CLCL}$-165	ns
	ALE Low to $\overline{RD}$ or $\overline{WR}$ Low	200	300	$3t_{CLCL}$-50	$3t_{CLCL}$+50	ns
L	Address to RD or WR Low	203		$4t_{CLCL}$-75		ns
X	Data Valid to $\overline{WR}$ Transition	23		t_{CLCL}-20		ns
H	Data Valid to $\overline{WR}$ High	433		$7t_{CLCL}$-120		ns
X	Data Hold After $\overline{WR}$	33		t_{CLCL}-20		ns
Z	$\overline{RD}$ Low to Address Float		0		0	ns
H	$\overline{RD}$ or $\overline{WR}$ High to ALE High	43	123	t_{CLCL}-20	t_{CLCL}+25	ns

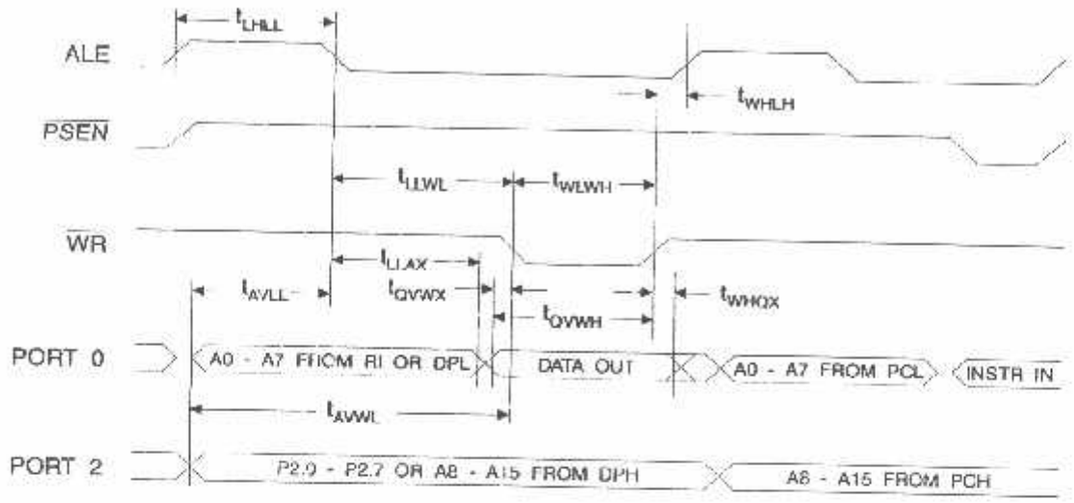
xternal Program Memory Read Cycle



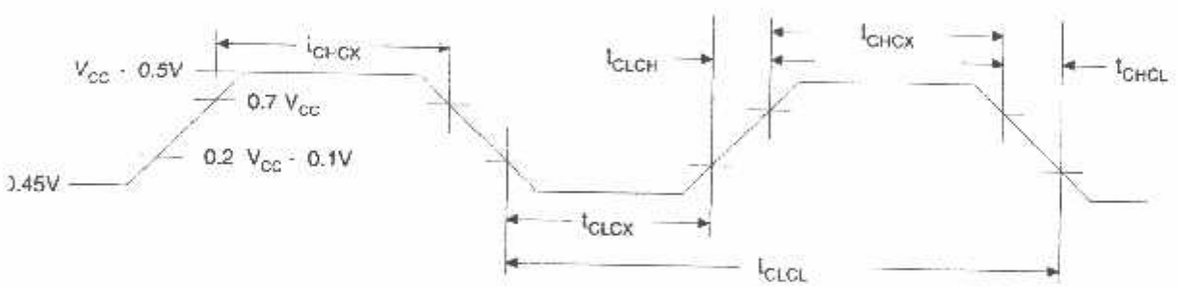
ternal Data Memory Read Cycle



xternal Data Memory Write Cycle



ternal Clock Drive Waveforms



ernal Clock Drive

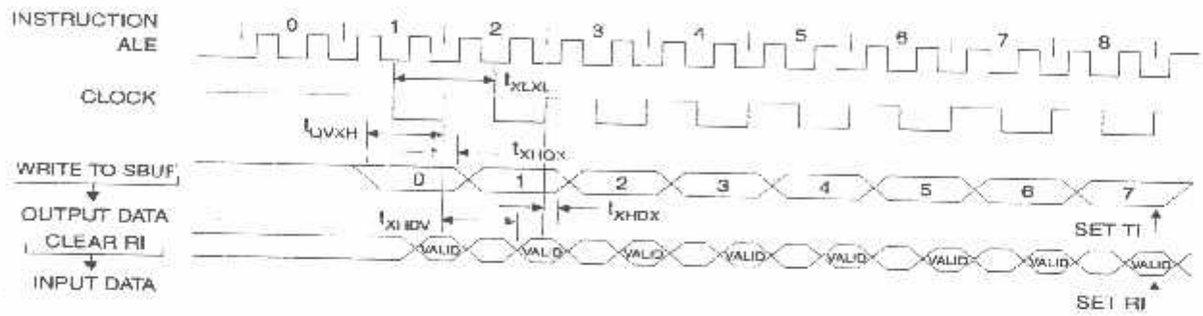
nbol	Parameter	Min	Max	Units
LCL	Oscillator Frequency	0	24	MHz
L	Clock Period	41.6		ns
X	High Time	15		ns
C	Low Time	15		ns
R	Rise Time		20	ns
F	Fall Time		20	ns

erial Port Timing: Shift Register Mode Test Conditions

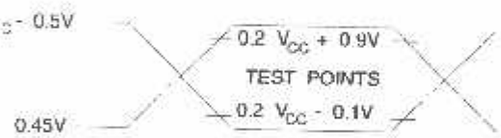
$_C$ = 5.0 V ± 20%; Load Capacitance = 80 pF)

mbol	Parameter	12 MHz Osc		Variable Oscillator		Units
		Min	Max	Min	Max	
XL	Serial Port Clock Cycle Time	1.0		$12t_{CLCL}$		µs
XH	Output Data Setup to Clock Rising Edge	700		$10t_{CLCL}$-133		ns
QX	Output Data Hold After Clock Rising Edge	50		$2t_{CLCL}$-117		ns
DX	Input Data Hold After Clock Rising Edge	0		0		ns
DV	Clock Rising Edge to Input Data Valid		700		$10t_{CLCL}$-133	ns

ift Register Mode Timing Waveforms

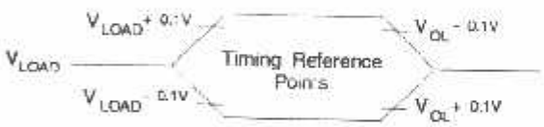


Testing Input/Output Waveforms(1)



1. AC Inputs during testing are driven at V_{CC} - 0.5V for a logic 1 and 0.45V for a logic 0. Timing measurements are made at V_{IH} min. for a logic 1 and V_{IL} max. for a logic 0.

Float Waveforms(1)



Note: 1. For timing purposes, a port pin is no longer floating when a 100 mV change from load voltage occurs. A port pin begins to float when 100 mV change from the loaded V_{OH}/V_{OL} level occurs.

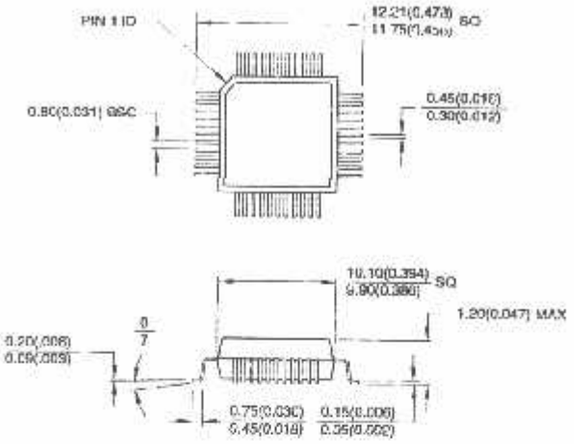
rdering Information

Speed (MHz)	Power Supply	Ordering Code	Package	Operation Range
12	5V ± 20%	AT89C51-12AC	44A	Commercial (0°C to 70°C)
		AT89C51-12JC	44J	
		AT89C51-12PC	40P6	
		AT89C51-12QC	44Q	
		AT89C51-12AI	44A	Industrial (-40°C to 85°C)
		AT89C51-12JI	44J	
		AT89C51-12PI	40P6	
		AT89C51-12QI	44Q	
16	5V ± 20%	AT89C51-16AC	44A	Commercial (0°C to 70°C)
		AT89C51-16JC	44J	
		AT89C51-16PC	40P6	
		AT89C51-16QC	44Q	
		AT89C51-16AI	44A	Industrial (-40°C to 85°C)
		AT89C51-16JI	44J	
		AT89C51-16PI	40P6	
		AT89C51-16QI	44Q	
20	5V ± 20%	AT89C51-20AC	44A	Commercial (0°C to 70°C)
		AT89C51-20JC	44J	
		AT89C51-20PC	40P6	
		AT89C51-20QC	44Q	
		AT89C51-20AI	44A	Industrial (-40°C to 85°C)
		AT89C51-20JI	44J	
		AT89C51-20PI	40P6	
		AT89C51-20QI	44Q	
24	5V ± 20%	AT89C51-24AC	44A	Commercial (0°C to 70°C)
		AT89C51-24JC	44J	
		AT89C51-24PC	40P6	
		AT89C51-24QC	44Q	
		AT89C51-24AI	44A	Industrial (-40°C to 85°C)
		AT89C51-24JI	44J	
		AT89C51-24PI	40P6	
		AT89C51-24QI	44Q	

	Package Type
	44-lead, Thin Plastic Gull Wing Quad Flatpack (TQFP)
	44-lead, Plastic J-leaded Chip Carrier (PLCC)
6	40-lead, 0.600" Wide, Plastic Dual Inline Package (PDIP)
	44-lead, Plastic Gull Wing Quad Flatpack (PQFP)

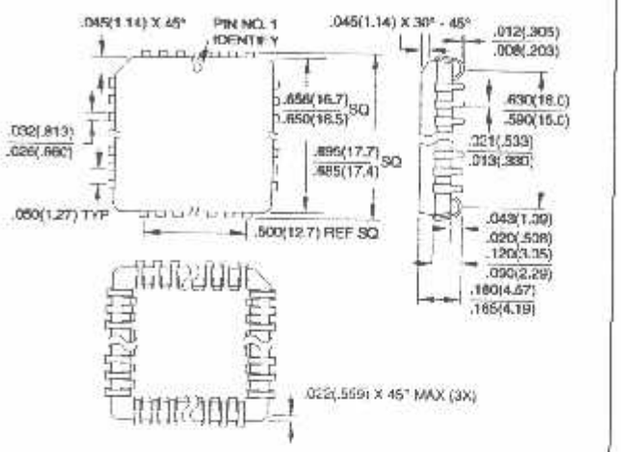
ıckaging Information

44A, 44-lead, Thin (1.0 mm) Plastic Gull Wing Quad Flatpack (TQFP)
*Dimensions in Millimeters and (Inches)**
JEDEC STANDARD MS-026 ACB

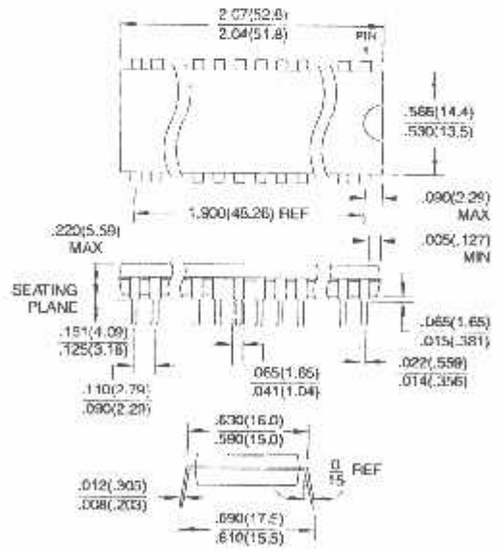


Controlling dimension: millimeters

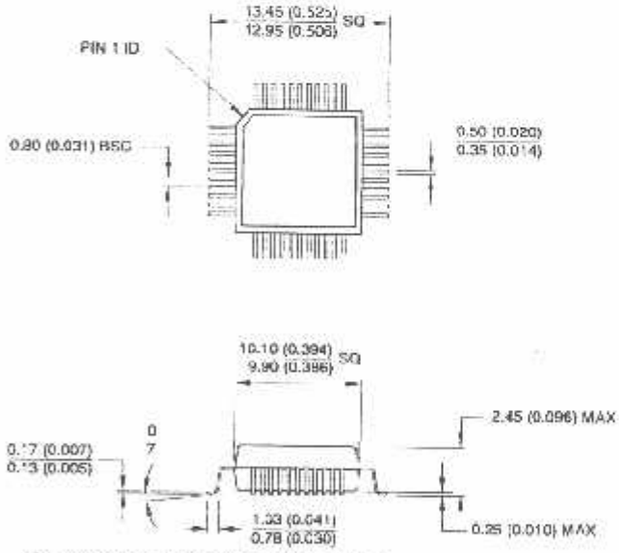
44J, 44-lead, Plastic J-leaded Chip Carrier (PLCC)
Dimensions in Inches and (Millimeters)
JEDEC STANDARD MS-018 AC



40P6, 40-lead, 0.600" Wide, Plastic Dual Inline Package (PDIP)
Dimensions in Inches and (Millimeters)



44Q, 44-lead, Plastic Quad Flat Package (PQFP)
Dimensions in Millimeters and (Inches)*
JEDEC STANDARD MS-022 AB



Controlling dimension: millimeters

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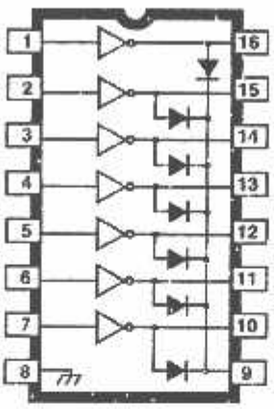
0265G–02/00/xM

2003 THRU 2024

Data Sheet 29304F

HIGH-VOLTAGE, HIGH-CURRENT DARLINGTON ARRAYS



Dwg. No. A-9594

Note that the ULN20xxA series (dual in-line package) and ULN20xxL series (small-outline IC package) are electrically identical and share a common terminal number assignment.

ABSOLUTE MAXIMUM RATINGS

Output Voltage, V_{CE}
(ULN200xA and ULN200xL) ..... **50 V**
(ULN202xA and ULN202xL) ..... **95 V**
Input Voltage, V_{IN} ..... **30 V**
Continuous Output Current,
I_C ..... **500 mA**
Continuous Input Current, I_{IN} ..... **25 mA**
Power Dissipation, P_D
(one Darlington pair) ..... **1.0 W**
(total package) ..... **See Graph**
Operating Temperature Range,
T_A ..... **-20°C to +85°C**
Storage Temperature Range,
T_S ..... **-55°C to +150°C**

Ideally suited for interfacing between low-level logic circuitry and multiple peripheral power loads, the Series ULN20xxA/L high-voltage, high-current Darlington arrays feature continuous load current ratings to 500 mA for each of the seven drivers. At an appropriate duty cycle depending on ambient temperature and number of drivers turned ON simultaneously, typical power loads totaling over 230 W (350 mA x 7, 95 V) can be controlled. Typical loads include relays, solenoids, stepping motors, magnetic print hammers, multiplexed LED and incandescent displays, and heaters. All devices feature open-collector outputs with integral clamp diodes.

The ULN2003A/L and ULN2023A/L have series input resistors selected for operation directly with 5 V TTL or CMOS. These devices will handle numerous interface needs — particularly those beyond the capabilities of standard logic buffers.

The ULN2004A/L and ULN2024A/L have series input resistors for operation directly from 6 to 15 V CMOS or PMOS logic outputs.

The ULN2003A/L and ULN2004A/L are the standard Darlington arrays. The outputs are capable of sinking 500 mA and will withstand at least 50 V in the OFF state. Outputs may be paralleled for higher load current capability. The ULN2023A/L and ULN2024A/L will withstand 95 V in the OFF state.

These Darlington arrays are furnished in 16-pin dual in-line plastic packages (suffix "A") and 16-lead surface-mountable SOICs (suffix "L"). All devices are pinned with outputs opposite inputs to facilitate ease of circuit board layout. All devices are rated for operation over the temperature range of -20°C to +85°C. Most (see matrix, next page) are also available for operation to -40°C; to order, change the prefix from "ULN" to "ULQ".

FEATURES

- TTL, DTL, PMOS, or CMOS-Compatible Inputs
- Output Current to 500 mA
- Output Voltage to 95 V
- Transient-Protected Outputs
- Dual In-Line Plastic Package or Small-Outline IC Package

x = digit to identify specific device. Characteristic shown applies to family of devices with remaining digits as shown. See matrix on next page.

2003 THRU 2024
HIGH-VOLTAGE, HIGH-CURRENT DARLINGTON ARRAYS

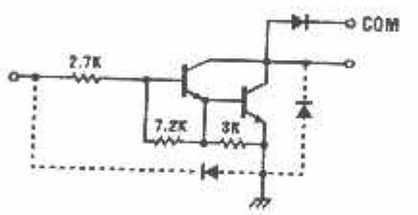
DEVICE PART NUMBER DESIGNATION

$V_{CE(MAX)}$	50 V	95 V
$I_{C(MAX)}$	500 mA	500 mA
Logic	**Part Number**	
5V TTL, CMOS	ULN2003A* ULN2003L*	ULN2023A* ULN2023L
6-15 V CMOS, PMOS	ULN2004A* ULN2004L*	ULN2024A ULN2024L

* Also available for operation between -40°C and +85°C. To order, change prefix from "ULN" to "ULQ".

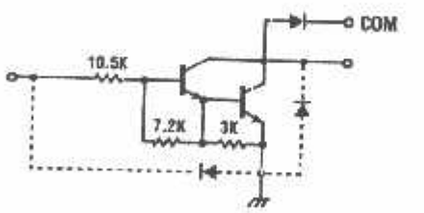
PARTIAL SCHEMATICS

ULN20x3A/L (Each Driver)

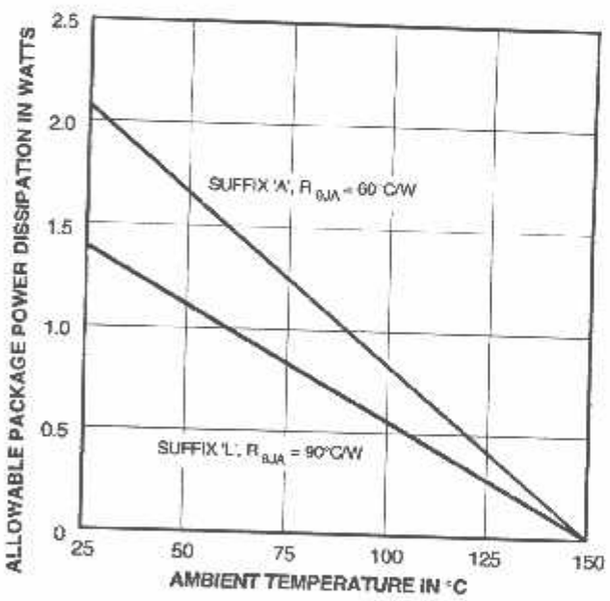


Dwg. No. A-9651

ULN20x4A/L (Each Driver)



Dwg. No. A-9998A



Dwg. GP-006A

X = Digit to identify specific device. Specification shown applies to family of devices with remaining digits as shown. See matrix above.

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pes ULN2003A, ULN2003L, ULN2004A, and ULN2004L
ECTRICAL CHARACTERISTICS at +25°C (unless otherwise noted).

aracteristic	Symbol	Test Fig.	Applicable Devices	Test Conditions	Limits			
					Min.	Typ.	Max.	Units
tput Leakage Current	I_{CEX}	1A	All	V_{CE} = 50 V, T_A = 25°C	—	< 1	50	µA
				V_{CE} = 50 V, T_A = 70°C	—	< 1	100	µA
		1B	ULN2004A/L	V_{CE} = 50 V, T_A = 70°C, V_{IN} = 1.0 V	—	< 5	500	µA
lector-Emitter uration Voltage	$V_{CE(SAT)}$	2	All	I_C = 100 mA, I_B = 250 µA	—	0.9	1.1	V
				I_C = 200 mA, I_B = 350 µA	—	1.1	1.3	V
				I_C = 350 mA, I_B = 500 µA	—	1.3	1.6	V
t Current	$I_{IN(ON)}$	3	ULN2003A/L	V_{IN} = 3.85 V	—	0.93	1.35	mA
			ULN2004A/L	V_{IN} = 5.0 V	—	0.35	0.5	mA
				V_{IN} = 12 V	—	1.0	1.45	mA
	$I_{IN(OFF)}$	4	All	I_C = 500 µA, T_A = 70°C	50	65	—	µA
t Voltage	$V_{IN(ON)}$	5	ULN2003A/L	V_{CE} = 2.0 V, I_C = 200 mA	—	—	2.4	V
				V_{CE} = 2.0 V, I_C = 250 mA	—	—	2.7	V
				V_{CE} = 2.0 V, I_C = 300 mA	—	—	3.0	V
			ULN2004A/L	V_{CE} = 2.0 V, I_C = 125 mA	—	—	5.0	V
				V_{CE} = 2.0 V, I_C = 200 mA	—	—	6.0	V
				V_{CE} = 2.0 V, I_C = 275 mA	—	—	7.0	V
				V_{CE} = 2.0 V, I_C = 350 mA	—	—	8.0	V
t Capacitance	C_{IN}	—	All		—	15	25	pF
-On Delay	t_{PLH}	8	All	0.5 E_{IN} to 0.5 E_{OUT}	—	0.25	1.0	µs
-Off Delay	t_{PHL}	8	All	0.5 E_{IN} to 0.5 E_{OUT}	—	0.25	1.0	µs
p Diode age Current	I_R	6	All	V_R = 50 V, T_A = 25°C	—	—	50	µA
				V_R = 50 V, T_A = 70°C	—	—	100	µA
p Diode ard Voltage	V_F	7	All	I_F = 350 mA	—	1.7	2.0	V

plete part number includes suffix to identify package style: A = DIP, L = SOIC.

03 THRU 2024
'GH-VOLTAGE,
'GH-CURRENT
\RLINGTON ARRAYS

s ULN2023A, ULN2023L, ULN2024A, and ULN2024L
:TRICAL CHARACTERISTICS at +25°C (unless otherwise noted).

acteristic	Symbol	Test Fig.	Applicable Devices	Test Conditions	Limits			
					Min.	Typ.	Max.	Units
t Leakage Current	I_{CEX}	1A	All	V_{CE} = 95 V, T_A = 25°C	—	< 1	50	µA
				V_{CE} = 95 V, T_A = 70°C	—	< 1	100	µA
		1B	ULN2024A/L	V_{CE} = 95 V, T_A = 70°C, V_{IN} = 1.0 V	—	< 5	500	µA
tor-Emitter ıtion Voltage	$V_{CE(SAT)}$	2	All	I_C = 100 mA, I_B = 250 µA	—	0.9	1.1	V
				I_C = 200 mA, I_B = 350 µA	—	1.1	1.3	V
				I_C = 350 mA, I_B = 500 µA	—	1.3	1.6	V
Current	$I_{IN(ON)}$	3	ULN2023A/L	V_{IN} = 3.85 V	—	0.93	1.35	mA
			ULN2024A/L	V_{IN} = 5.0 V	—	0.35	0.5	mA
				V_{IN} = 12 V	—	1.0	1.45	mA
	$I_{IN(OFF)}$	4	All	I_C = 500 µA, T_A = 70°C	50	65	—	µA
oltage	$V_{IN(ON)}$	5	ULN2023A/L	V_{CE} = 2.0 V, I_C = 200 mA	—	—	2.4	V
				V_{CE} = 2.0 V, I_C = 250 mA	—	—	2.7	V
				V_{CE} = 2.0 V, I_C = 300 mA	—	—	3.0	V
			ULN2024A/L	V_{CE} = 2.0 V, I_C = 125 mA	—	—	5.0	V
				V_{CE} = 2.0 V, I_C = 200 mA	—	—	6.0	V
				V_{CE} = 2.0 V, I_C = 275 mA	—	—	7.0	V
				V_{CE} = 2.0 V, I_C = 350 mA	—	—	8.0	V
apacitance	C_{IN}	—	All		—	15	25	pF
ı Delay	t_{PLH}	8	All	0.5 E_{IN} to 0.5 E_{OUT}	—	0.25	1.0	µs
f Delay	t_{PHL}	8	All	0.5 E_{IN} to 0.5 E_{OUT}	—	0.25	1.0	µs
Diode ı Current	I_R	6	All	V_R = 95 V, T_A = 25°C	—	—	50	µA
				V_R = 95 V, T_A = 70°C	—	—	100	µA
Diode Voltage	V_F	7	All	I_F = 350 mA	—	1.7	2.0	V

e part number includes suffix to identify package style: A = DIP, L = SOIC.

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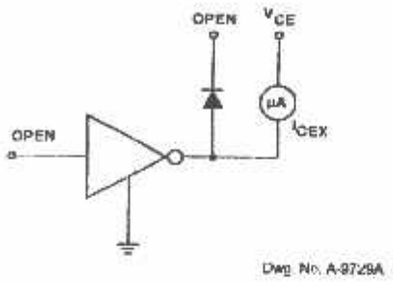
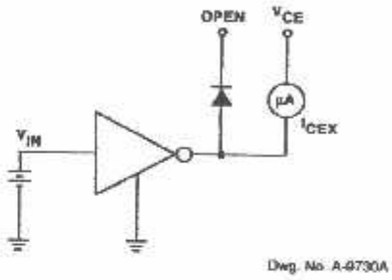
TEST FIGURES

FIGURE 1A



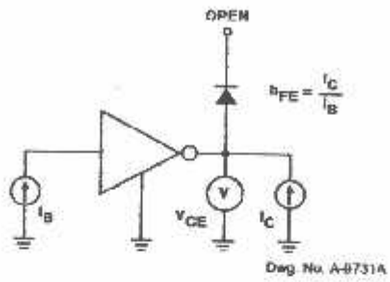
Dwg. No. A-9729A

FIGURE 1B



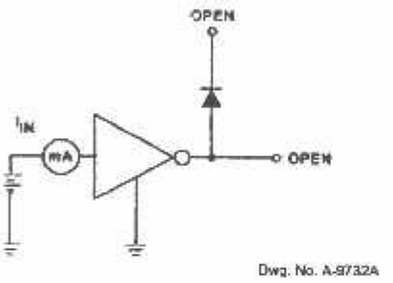
Dwg. No. A-9730A

FIGURE 2



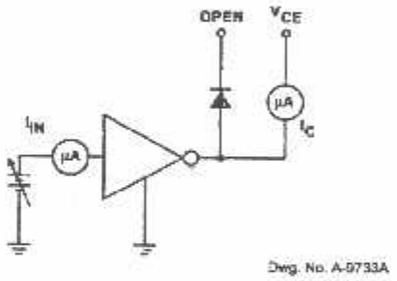
Dwg. No. A-9731A

FIGURE 3



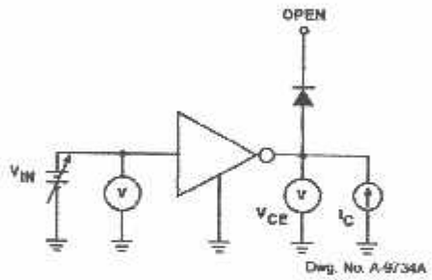
Dwg. No. A-9732A

FIGURE 4



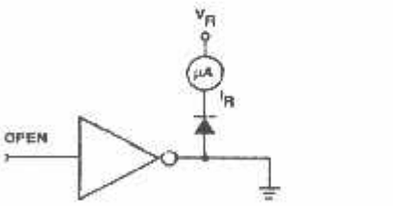
Dwg. No. A-9733A

FIGURE 5



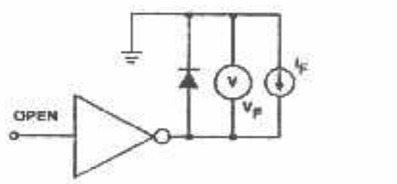
Dwg. No. A-9734A

FIGURE 6



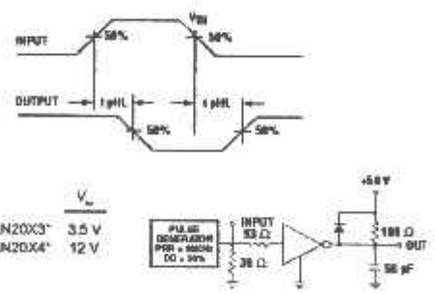
Dwg. No. A-9735A

FIGURE 7



Dwg. No. A-9736A

FIGURE 8

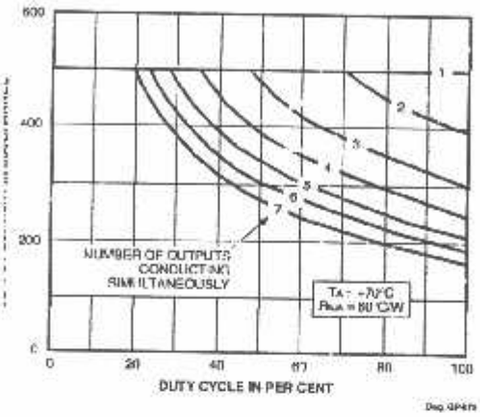


*Complete part number includes a final letter to indicate package.

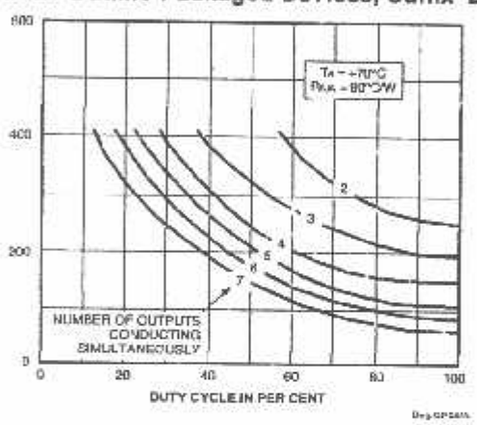
†Digit to identify specific device. Specification shown applies to family of devices with remaining digits as shown.

LLOWABLE COLLECTOR CURRENT AS A FUNCTION OF DUTY CYCLE

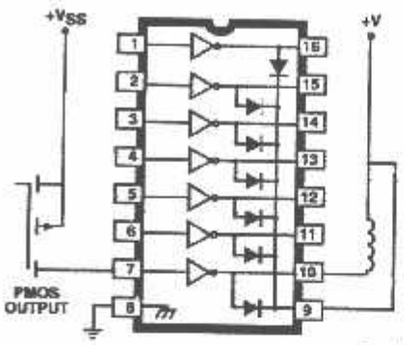
(Dual In-line-Packaged Devices, Suffix 'A')



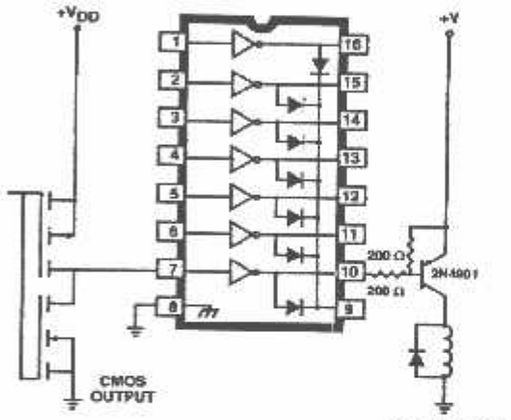
Small-Outline-Packaged Devices, Suffix 'L')



TYPICAL APPLICATIONS

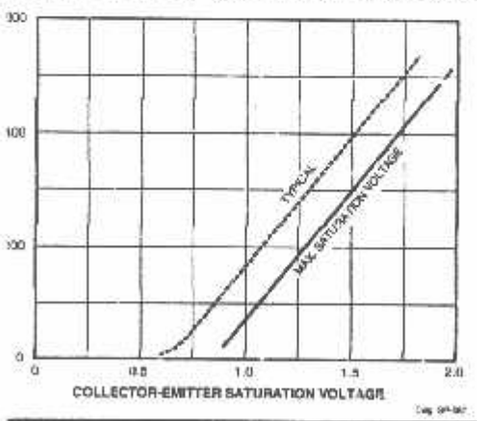


Dwg. No. A-9652

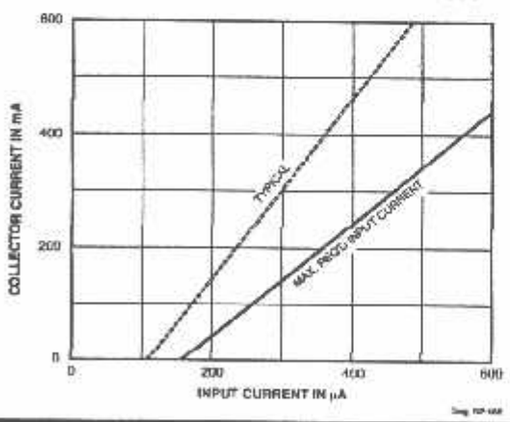


Dwg. No. A-9654A

SATURATION VOLTAGE FUNCTION OF COLLECTOR CURRENT



COLLECTOR CURRENT AS A FUNCTION OF INPUT CURRENT



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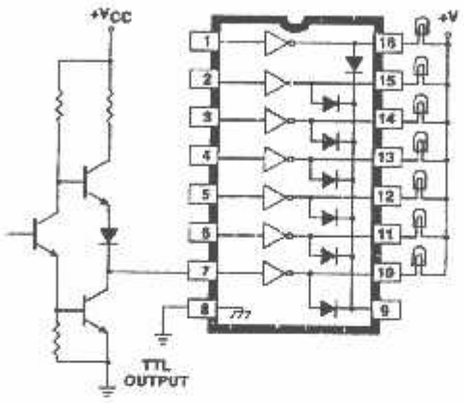
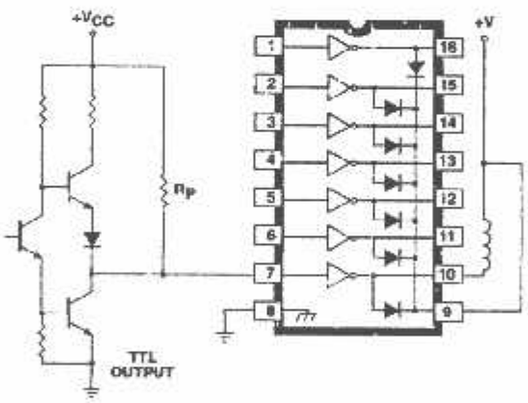
TYPICAL APPLICATIONS



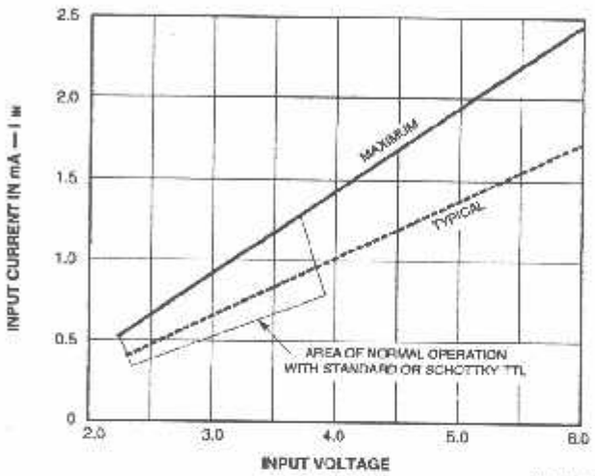
Dwg. No. A-9023A



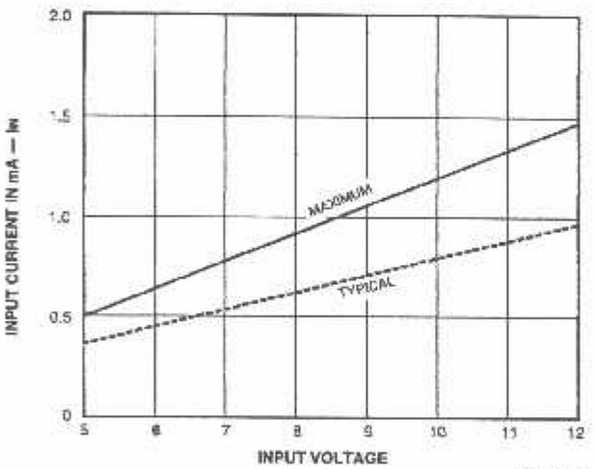
Dwg. No. A-10,175

INPUT CURRENT AS A FUNCTION OF INPUT VOLTAGE

Types ULN2003A, ULN2003L, ULN2023A, and ULN2023L

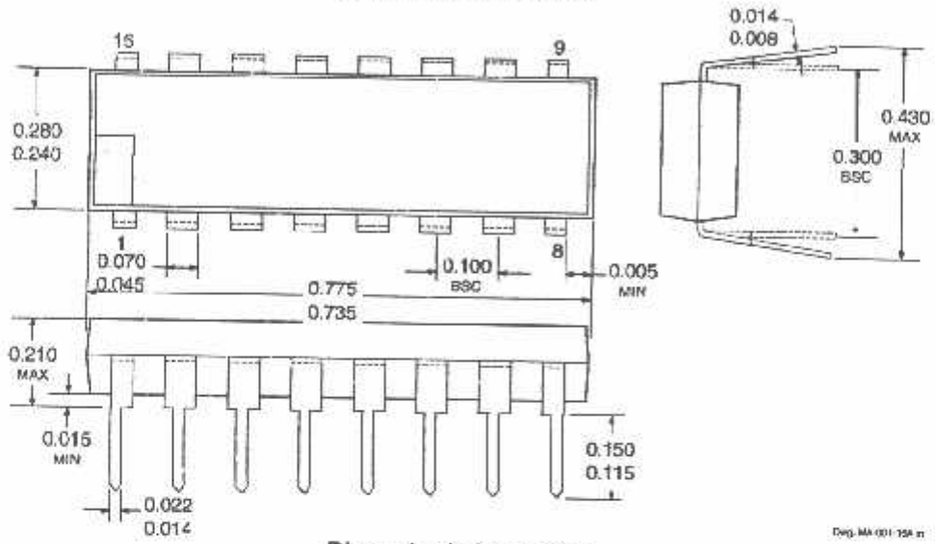


Types ULN2004A, ULN2004L, ULN2024A, and ULN2024L

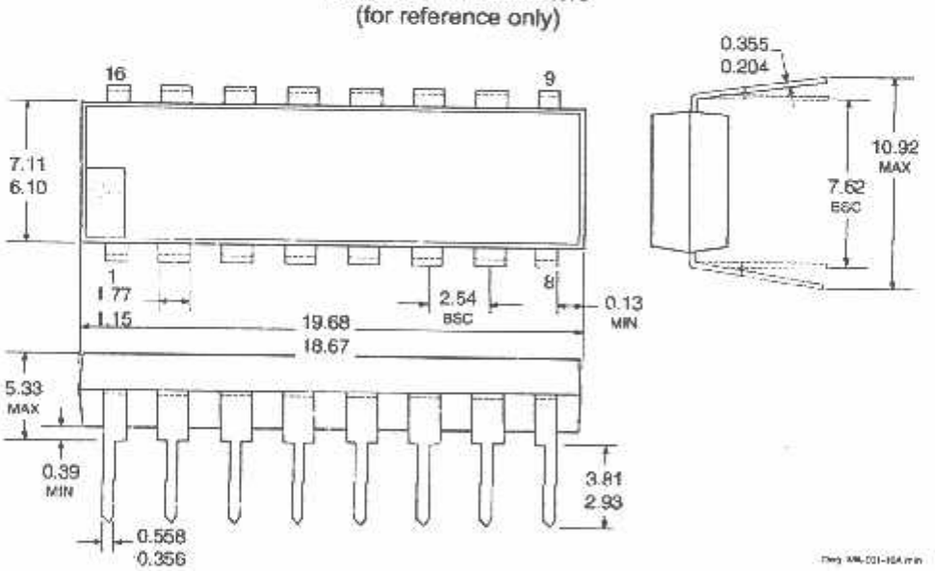


PACKAGE DESIGNATOR "A"

Dimensions in Inches
(controlling dimensions)



Dimension in Millimeters
(for reference only)



1. Leads 1, 8, 9, and 16 may be half leads at vendor's option.
2. Lead thickness is measured at seating plane or below.
3. Lead spacing tolerance is non-cumulative.
4. Exact body and lead configuration at vendor's option within limits shown.

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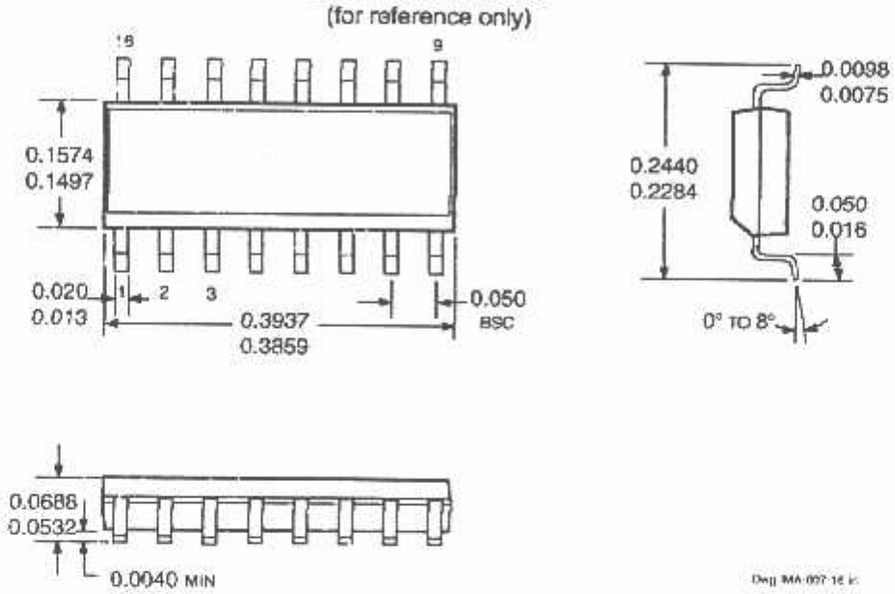
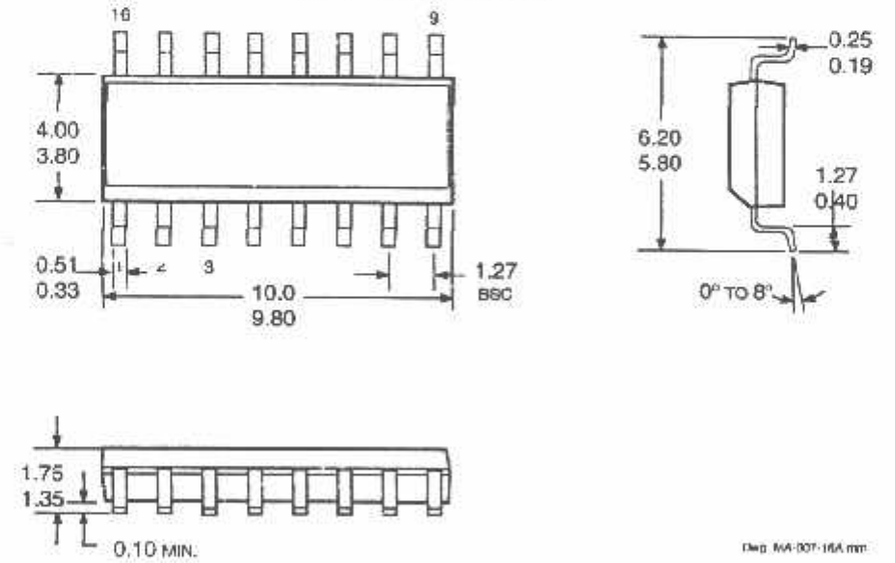
PACKAGE DESIGNATOR "L"

Dimensions in Inches
(for reference only)



Dwg. MA-007-16 in

Dimension in Millimeters
(controlling dimensions)



Dwg. MA-007-16A mm

ES: 1. Lead spacing tolerance is non-cumulative.
2. Exact body and lead configuration at vendor's option within limits shown.

)03 THRU 2024
IGH-VOLTAGE,
IGH-CURRENT
ARLINGTON ARRAYS

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Allegro MicroSystems, Inc.

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MOTOROLA

SERIAL-IN PARALLEL-OUT SHIFT REGISTER

SN54/74LS164

SERIAL-IN PARALLEL-OUT SHIFT REGISTER

LOW POWER SCHOTTKY

The SN54/74LS164 is a high speed 8-Bit Serial-In Parallel-Out Shift Register. Serial data is entered through a 2-input AND gate synchronous with the LOW to HIGH transition of the clock. The device features an asynchronous Master Reset which clears the register setting all outputs LOW independent of the clock. It utilizes the Schottky diode clamped process to achieve high speeds and is fully compatible with all Motorola TTL products.

- Typical Shift Frequency of 35 MHz
- Asynchronous Master Reset
- Gated Serial Data Input
- Fully Synchronous Data Transfers
- Input Clamp Diodes Limit High Speed Termination Effects
- ESD > 3500 Volts

J SUFFIX
CERAMIC
CASE 632-08

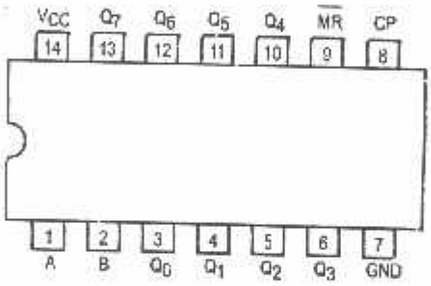
N SUFFIX
PLASTIC
CASE 646-06

D SUFFIX
SOIC
CASE 751A-02

ORDERING INFORMATION

SN54LSXXXJ	Ceramic
SN74LSXXXN	Plastic
SN74LSXXXD	SOIC

CONNECTION DIAGRAM DIP (TOP VIEW)



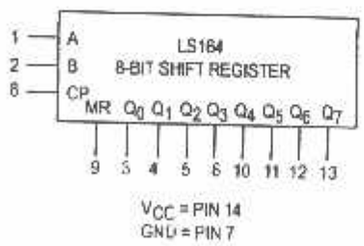
NOTE:
The Flatpak version has the same pinouts (Connection Diagram) as the Dual In-Line Package.

PIN NAMES

		LOADING (Note a) HIGH	LOW
A, B	Data Inputs	0.5 U.L.	0.25 U.L.
CP	Clock (Active HIGH Going Edge) Input	0.5 U.L.	0.25 U.L.
MR	Master Reset (Active LOW) Input	0.5 U.L.	0.25 U.L.
$Q_0 - Q_7$	Outputs (Note b)	10 U.L.	5 (2.5) U.L.

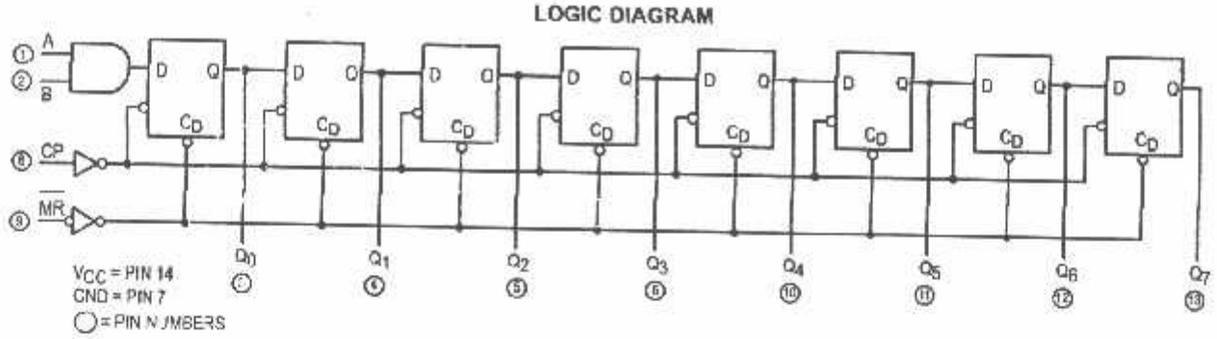
NOTES:
a. 1 TTL Unit Load (U.L.) = 40 µA HIGH/1.6 mA LOW.
b. The Output LOW drive factor is 2.5 U.L. for Military (54) and 5 U.L. for Commercial (74) Temperature Ranges.

LOGIC SYMBOL



V_{CC} = PIN 14
GND = PIN 7

LOGIC DIAGRAM



FUNCTIONAL DESCRIPTION

The LS164 is an edge-triggered 8-bit shift register with serial data entry and an output from each of the eight stages. Data is entered serially through one of two inputs (A or B); either of these inputs can be used as an active HIGH Enable for data entry through the other input. An unused input must be tied HIGH, or both inputs connected together.

Each LOW-to-HIGH transition on the Clock (CP) input shifts data one place to the right and enters into Q_0 the logical AND of the two data inputs (A•B) that existed before the rising clock edge. A LOW level on the Master Reset (MR) input overrides all other inputs and clears the register asynchronously, forcing all Q outputs LOW.

MODE SELECT — TRUTH TABLE

OPERATING MODE	INPUTS			OUTPUTS	
	MR	A	B	Q_0	Q_1–Q_7
Reset (Clear)	L	X	X	L	L – L
Shift:	H	l	l	L	$q_0 - q_6$
	H	l	h	L	$q_0 - q_6$
	H	h	l	L	$q_0 - q_6$
	H	h	h	H	$q_0 - q_6$

L (l) = LOW Voltage Levels
H (h) = HIGH Voltage Levels
X = Don't Care
q_n = Lower case letters indicate the state of the referenced input or output one set-up time prior to the LOW to HIGH clock transition.

GUARANTEED OPERATING RANGES

Symbol	Parameter		Min	Typ	Max	Unit
V_{CC}	Supply Voltage	54 74	4.5 4.75	5.0 5.0	5.5 5.25	V
T_A	Operating Ambient Temperature Range	54 74	–55 0	25 25	125 70	°C
I_{OH}	Output Current — High	54, 74			0.4	mA
I_{OL}	Output Current — Low	54 74			4.0 8.0	mA

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

Symbol	Parameter		Limits Min	Typ	Max	Unit	Test Conditions	
V_{IH}	Input HIGH Voltage		2.0			V	Guaranteed Input HIGH Voltage for All Inputs	
V_{IL}	Input LOW Voltage	54			0.7	V	Guaranteed Input LOW Voltage for All Inputs	
		74			0.8			
V_{IK}	Input Clamp Diode Voltage			−0.65	−1.5	V	V_{CC} = MIN, I_{IN} = −18 mA	
V_{OH}	Output HIGH Voltage	54	2.5	3.5		V	V_{CC} = MIN, I_{OH} = MAX, V_{IN} = V_{IH} or V_{IL} per Truth Table	
		74	2.7	3.5				
V_{OL}	Output LOW Voltage	54, 74		0.25	0.4	V	I_{OL} = 4.0 mA	V_{CC} = V_{CC} MIN, V_{IN} = V_{IH} or V_{IL} per Truth Table
		74		0.35	0.5	V	I_{OL} = 8.0 mA	
I_{IH}	Input HIGH Current				20	μA	V_{CC} = MAX, V_{IN} = 2.7 V	
					0.1	mA	V_{CC} = MAX, V_{IN} = 7.0 V	
I_{IL}	Input LOW Current				−0.4	mA	V_{CC} = MAX, V_{IN} = 0.4 V	
I_{OS}	Short Circuit Current (Note 1)		−20		−100	mA	V_{CC} = MAX	
I_{CC}	Power Supply Current				27	mA	V_{CC} = MAX	

Note 1: Not more than one output should be shorted at a time, nor for more than 1 second.

AC CHARACTERISTICS (T_A = 25°C)

Symbol	Parameter	Limits Min	Typ	Max	Unit	Test Conditions
f_{MAX}	Maximum Clock Frequency	25	36		MHz	V_{CC} = 5.0 V C_L = 15 pF
t_{PHL}	Propagation Delay MR to Output Q		24	36	ns	
t_{PLH} t_{PHL}	Propagation Delay Clock to Output Q		17 21	27 32	ns	

AC SETUP REQUIREMENTS (T_A = 25°C)

Symbol	Parameter	Limits Min	Typ	Max	Unit	Test Conditions
t_w	CP, MR Pulse Width	20			ns	V_{CC} = 5.0 V
t_s	Data Setup Time	15			ns	
t_h	Data Hold Time	5.0			ns	
t_{rec}	MR to Clock Recovery Time	20			ns	

AC WAVEFORMS

*The shaded areas indicate when the input is permitted to change for predictable output performance.

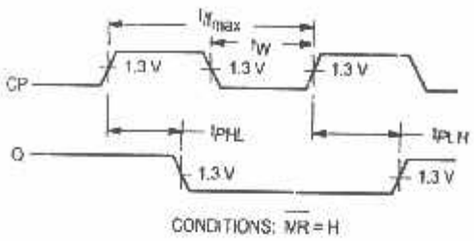


Figure 1. Clock to Output Delays and Clock Pulse Width

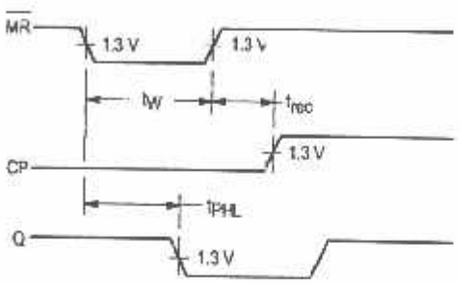


Figure 2. Master Reset Pulse Width, Master Reset to Output Delay and Master Reset to Clock Recovery Time

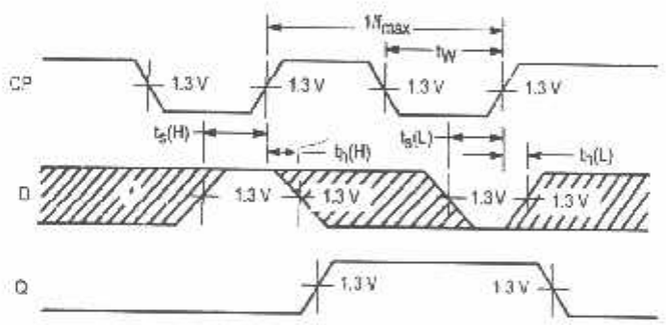


Figure 3. Data Setup and Hold Times

intersil

CA3161

August 1997

BCD to Seven Segment Decoder/Driver

Features

- TTL Compatible Input Logic Levels
- 25mA (Typ) Constant Current Segment Outputs
- Eliminates Need for Output Current Limiting Resistors
- Pin Compatible with Other Industry Standard Decoders
- Low Standby Power Dissipation . . . . . 18mW (Typ)

Description

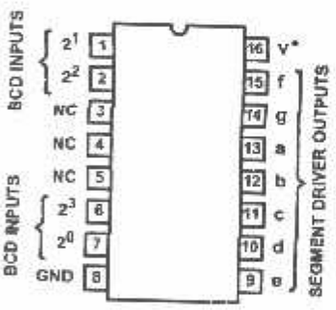
The CA3161E is a monolithic integrated circuit that performs the BCD to seven segment decoding function and features constant current segment drivers. When used with the CA3162E A/D Converter the CA3161E provides a complete digital readout system with a minimum number of external parts.

Ordering Information

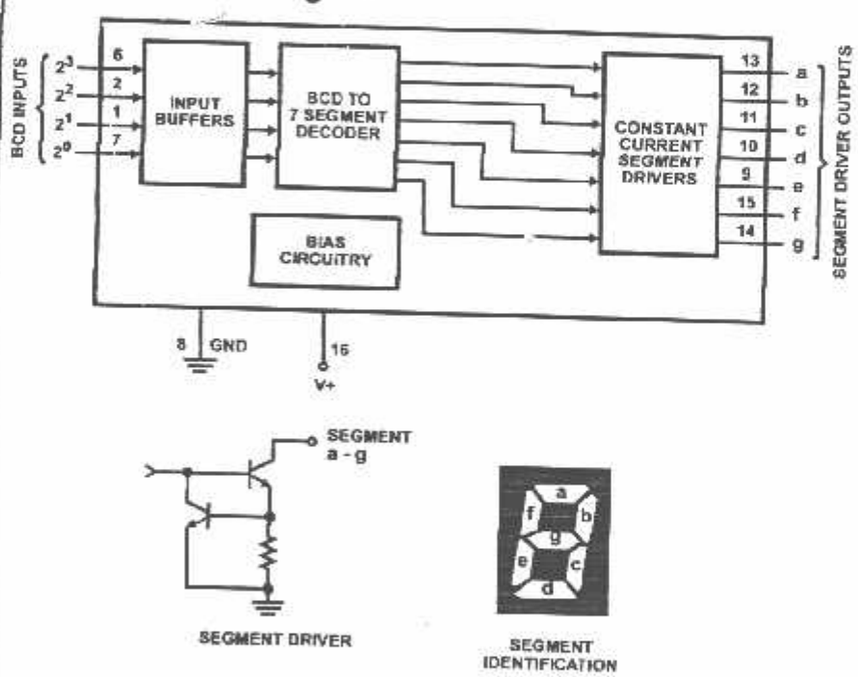
PART NUMBER	TEMP. RANGE (°C)	PACKAGE	PKG. NO.
CA3161E	0 to 70	16 Ld PDIP	E16.3

Pinout

CA3161
(PDIP)
TOP VIEW



Functional Block Diagram



SEGMENT DRIVER

SEGMENT IDENTIFICATION

File Number **1079.3**

Absolute Maximum Ratings

DC V_{SUPPLY} (Between Terminals 1 and 10) . . . . . +7.0V
Input Voltage (Terminals 1, 2, 6, 7) . . . . . +5.5V
Output Voltage
Output "Off" . . . . . +7V
Output "On" (Note 1) . . . . . +10V

Thermal Information

Thermal Resistance (Typical, Note 2) θ_{JA} (°C/W)
PDIP Package 100
Maximum Junction Temperature . . . . . 150°C
Maximum Storage Temperature Range . . . . . -65°C to 150°C
Maximum Lead Temperature (Soldering 10s) . . . . . 300°C

Operating Conditions

Temperature Range . . . . . 0°C to 75°C

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

NOTES:

1. This is the maximum output voltage for any single output. The output voltage must be consistent with the maximum dissipation and derating curve for worst case conditions. Example: All segments "ON", 100% duty cycle.
2. θ_{JA} is measured with the component mounted on an evaluation PC board in free air.

Electrical Specifications $T_A = 25°C$

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNITS
V_{SUPPLY} Operating Range, V*			4.5	5	5.5	V
Supply Current, I^+ (All Inputs High)			-	3.5	8	mA
Output Current Low (V_O = 2V)			18	25	32	mA
Output Current High (V_O = 5.5V)			-	-	250	µA
Input Voltage High (Logic "1" Level)			2	-	-	V
Input Voltage Low (Logic "0" Level)			-	-	0.8	V
nput Current High (Logic "1")		2V	-30	-	-	µA
nput Current Low (Logic "0")		0V	-40	-	-	µA
Propagation Delay Time,	t_{PHL}		-	2.6	-	µs
	t_{PLH}		-	1.4	-	µs

TRUTH TABLE

BINARY STATE	INPUTS				OUTPUTS							DISPLAY
	2^3	2^2	2^1	2^0	a	b	c	d	e	f	g	
0	L	L	L	L	L	L	L	L	L	L	H	0
1	L	L	L	H	H	L	L	H	H	H	H	1
2	L	L	H	L	L	L	H	L	L	H	L	2
3	L	L	H	H	L	L	L	L	H	H	L	3
4	L	H	L	L	H	L	L	H	H	L	L	4
5	L	H	L	H	L	H	L	L	H	L	L	5
6	L	H	H	L	L	H	L	L	L	L	L	6
7	L	H	H	H	L	L	L	H	H	H	H	7
8	H	L	L	L	L	L	L	L	L	L	L	8
9	H	L	L	H	L	L	L	L	H	L	L	9
10	H	L	H	L	H	H	H	H	H	H	L	-
11	H	L	H	H	L	H	H	L	L	L	L	E
12	H	H	L	L	H	L	L	H	L	L	L	H
13	H	H	L	H	H	H	H	L	L	L	H	L
14	H	H	H	L	L	L	H	H	L	L	L	P
15	H	H	H	H	H	H	H	H	H	H	H	BLANK

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'Infrared' Light-Emitting Diode Application Circuit

SERIAL CONNECTION AND PARALLEL CONNECTION

Figure 1 shows the most basic and commonly used circuits for driving light-emitting diodes.

In Figure 1(A), a constant voltage source (V_{CC}) is connected through a current limiting resistor (R) to an LED so that it is supplied with forward current (I_F). The I_F current flowing through the LED is expressed as $I_F = (V_{CC} - V_F)/R$, providing a radiant flux proportional to the I_F. The forward voltage (V_F) of the LED is dependent on the value of I_F, but it is approximated by a constant voltage when setting R.

Figures 1(B) and 1(C) show the circuits for driving LEDs in serial connection and parallel connection, respectively. In arrangement (B), the current flowing through the LED is expressed as $I_F = (V_{CC} - V_F \times N)/R$, while in arrangement (C), the current flowing through each LED is expressed as $I_F = (V_{CC} - V_F)/R$ and the total supply current is $N \times I_F$, where N is the number of LEDs.

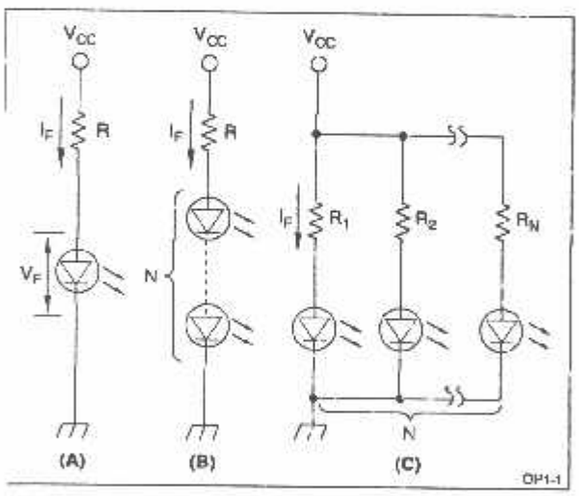

Figure 1. Driving Circuit of Light-Emitting Diode (LED)

The V_F of an LED has a temperature dependency of approximately -1.9 mV/°C. The operating point for the load R varies in response to the ambient temperature as shown in Figure 2.

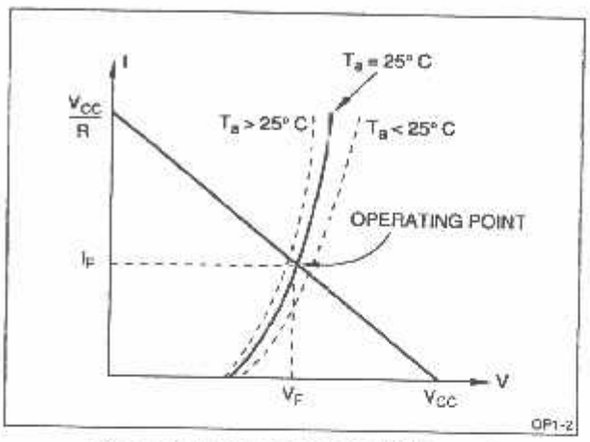

Figure 2. Current versus Voltage of Light-Emitting Diode (LED)

CONSTANT CURRENT DRIVE

To stabilize the radiant flux of the LED, the forward current (I_F) must be stabilized by using a constant current source. Figure 3 shows a circuit for constantly driving several LEDs using a transistor.

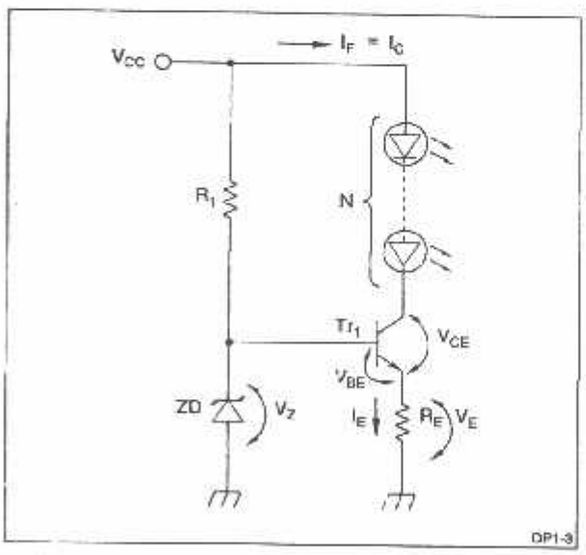

Figure 3. Constant Current Driving Circuit (1)

The transistor (Tr_1) is biased by a constant voltage supplied by a zener diode (ZD) so that the voltage across the emitter follower loaded by resistor R_E is constant, thereby making the collector current ($I_C = I_F$) constant. The I_C is given as $I_C = I_E = (V_Z = V_{BE})/R_E$. If too many LEDs are connected, the transistor enters the saturation region and does not operate as a constant current circuit. The number of LEDs (N) which can be connected in series is calculated by the following equations.

$V_{CC} - N \times V_F - V_E > V_{CE}$ (sat)

$V_E = V_Z - V_{BE}$

These equations give:

$N < (V_{CC} - V_Z + V_{BE} - V_{CE}(sat))/V_F$

Figures 4 and 5 show other constant current driving circuits that use diodes or transistors, instead of zener diodes.

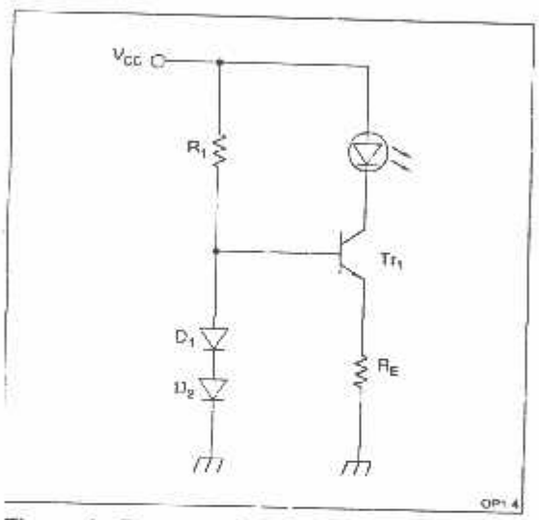

Figure 4. Constant Current Driving Circuit (2)

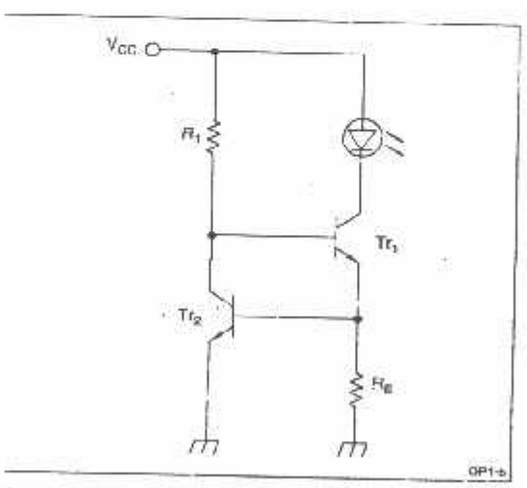

Figure 5. Constant Current Driving Circuit (3)

DRIVING CIRCUIT ACTIVATED BY A LOGIC IC

Figures 6 and 7 show LED driving circuits that operate in response to digital signals provided by TTL or CMOS circuits.

Figure 8 shows a driving circuit connected with a high level logic circuit.

In Figure 6, a high input signal V_{IN} from a TTL circuit makes the NPN transistor (Tr_1) conductive so that the forward current (I_F) flows through the LED. Accordingly, this circuit operates in the positive logic mode, in which a high input activates the LED.

In Figure 7, a low input signal V_{IN} from a TTL circuit makes the PNP transistor (Tr_1) conductive so that the forward current flows through the LED. This circuit operates in the negative logic mode, in which a low input activates the LED.

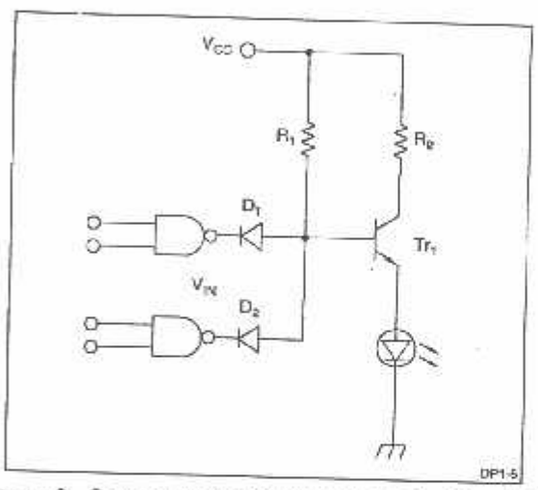

Figure 6. Connection with the TTL Logic Circuit (2)

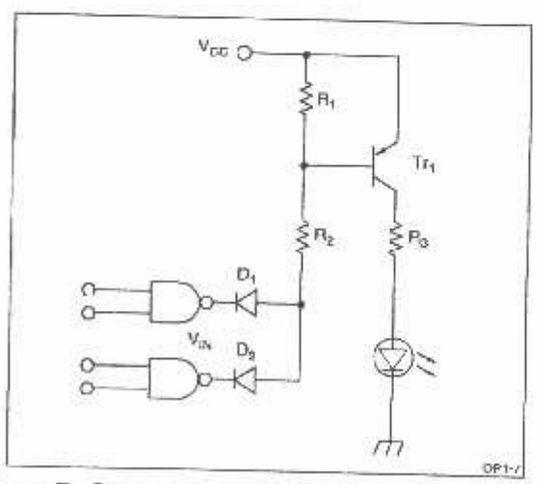

Figure 7. Connection with the TTL Logic Circuit (2)

In Figure 8, the circuit operates in the positive logic mode, and current I_F is stabilized by constant current driving so that the radiant flux of LED is stabilized against variations in the supply voltage (V_{CC}).

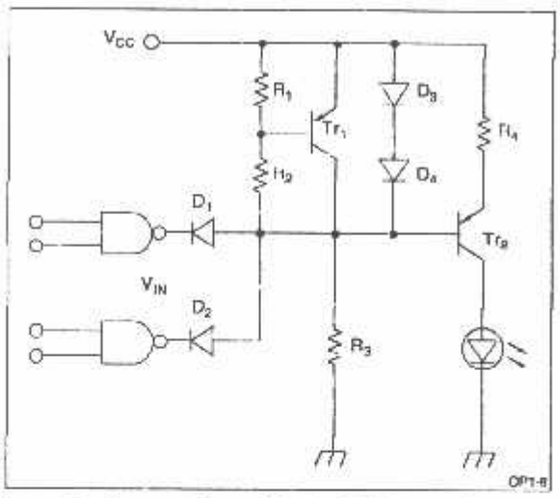

Figure 8. Connection with the TTL Logic Circuit (3)

DRIVING CIRCUIT WITH AN AC SIGNAL

Figure 9 (A) shows a circuit in which an AC power source supplies the forward current (I_{F1}) to an LED. A diode (D_1) in inverse parallel connection with the LED protects the LED against reverse voltage, suppressing the reverse voltage applied to the LED lower than V_{F2} by using a reverse voltage protection diode of an LED. The LED provides a radiant flux proportional to the applied AC current, (emitting only in half wave).

Figure 9 (B) shows the driving waveform of the AC power source.

Figure 10 (A) shows a driving circuit which modulates the radiant flux of LED in response to a sine wave or modulation signal. Figure 10 (B) shows modulation operation.

If an LED and light detector are used together in an environment of high intensity disturbing light, it is difficult for the light detector to detect the optical signal. In this case, modulating the LED drive signal alleviates the influence of disturbing light and facilitates signal detection.

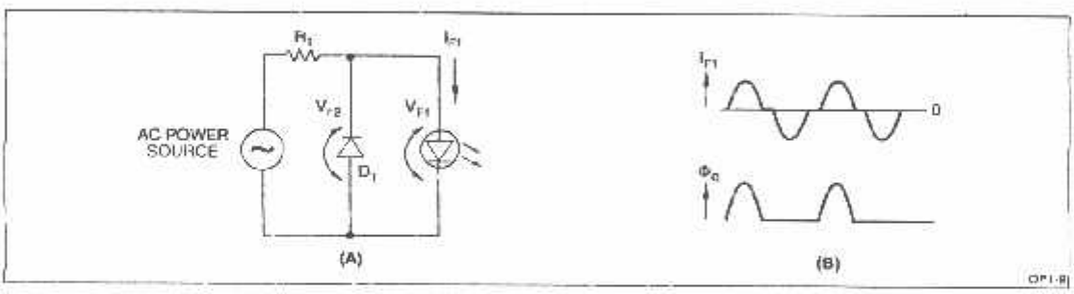

Figure 9. Driving Circuit with AC Power Source (A) and Driving Waveform (B)

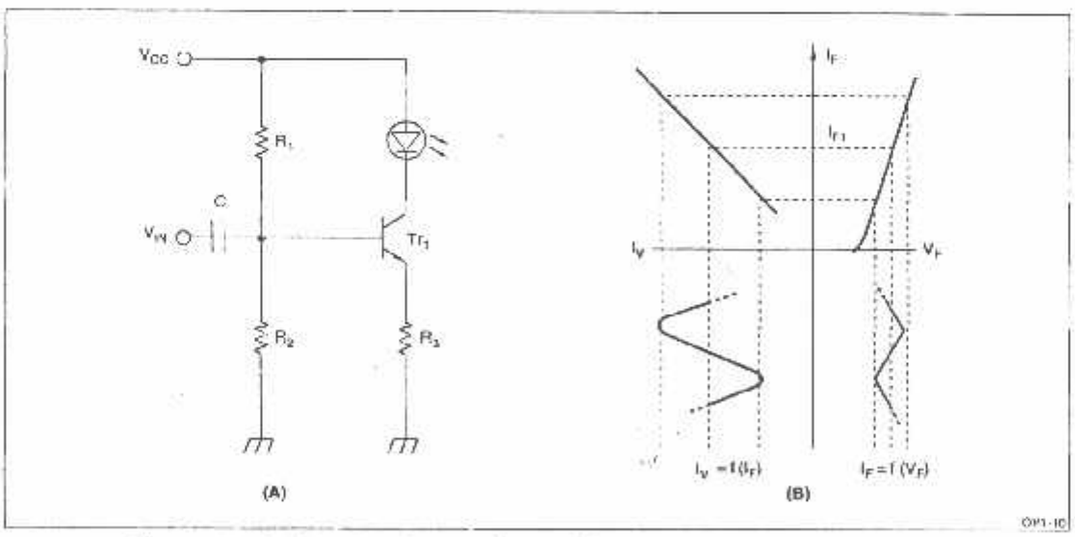

Figure 10. Modulation Driving Circuit (A) and Modulation Operation (B)

To drive an LED with a continuous modulation signal, it is necessary to operate the LED in the linear region of the light-emitting characteristics. In the arrangement of Figure 10, a fixed bias (I_{F1}) is applied to the LED using R_1 and R_2 so that the maximum amplitude of the modulation signal voltage (V_{IN}) lies within the linear portion of the LED characteristics. Moreover, to stabilize the radiant flux of the LED, it is driven by a constant current by the constant current driving circuit shown in Figure 3. The capacitor (C) used in Figure 10 (A) is a DC signal blocking capacitor.

PULSE DRIVING

LED driving systems fall into three categories: DC driving system, AC driving system (including modulation systems), and pulse driving system.

Features of the Pulse Driving System

Large radiant flux

Less influence of disturbing light

Information transmission

The radiant flux of the LED is proportional to its forward current (I_F), but in reality a large I_F heats up the LED by itself, causing the light-emitting efficiency to fall and thus saturating the radiant flux. In this circumstance, a relatively large I_F can be used with no risk of heating through the pulse drive of the LED. Consequently, a large radiant flux can be obtained.

When an LED is used in the outdoors where disturbing light is intense, the DC driving system or AC driving system which superimposes an AC signal on a fixed bias current provides low radiant flux, making it difficult to distinguish the signal (irradiation of LED) from disturbing light. In other words, the S/N ratio is small enough to reliably detect the signal. The pulse driving system provides high radiant flux and allows the detection of signal variations at the rising and falling edges of pulses, thereby enabling the use of LED-light detector where disturbing light is intense.

Transmission of information is possible by variations in pulse width or counting of the number of pulse used to encode the LED emission.

Figures 11 through 14 show typical pulse driving circuits. Figure 15 shows the pulse driving circuit used in the optical remote control. The circuit shown in Figure 11 uses an N-gate thyristor with voltage between the anode and cathode oscillated at a certain interval determined by the time constant of C x R so that the LED emits light pulse. To turn off the N-gate thyristor, resistor R_3 must be used so that the anode current is smaller than the holding current (I_H), i.e., $I_H > V_{CC}/R_3$. Therefore, R_3 has a large value, resulting in a large time constant ($\tau \pm C \times R_3$) and the circuit operates for a relatively long period to provide short pulse widths. The circuit shown in Figure 12 uses a type 555 timer IC to form an astable multi-vibrator to produce light pulses on the LED. The off-period (t_1) and the on-period (t_2) of the LED are calculated by the following equations.

$$t_1 = 1n2 \times (R_1 + R_2) \times C_1$$

$$t_2 = 1n2 \times R_2 \times C_1$$

The value of R1 is determined so that the rating of I_{IN} of a 555 timer IC is not exceeded, i.e. $S_1 > V_{CC}/I_{IN}$.

This pulse driving circuit uses a 555 timer IC to provide wide variable range in the oscillation period and light-on time. It is used extensively.

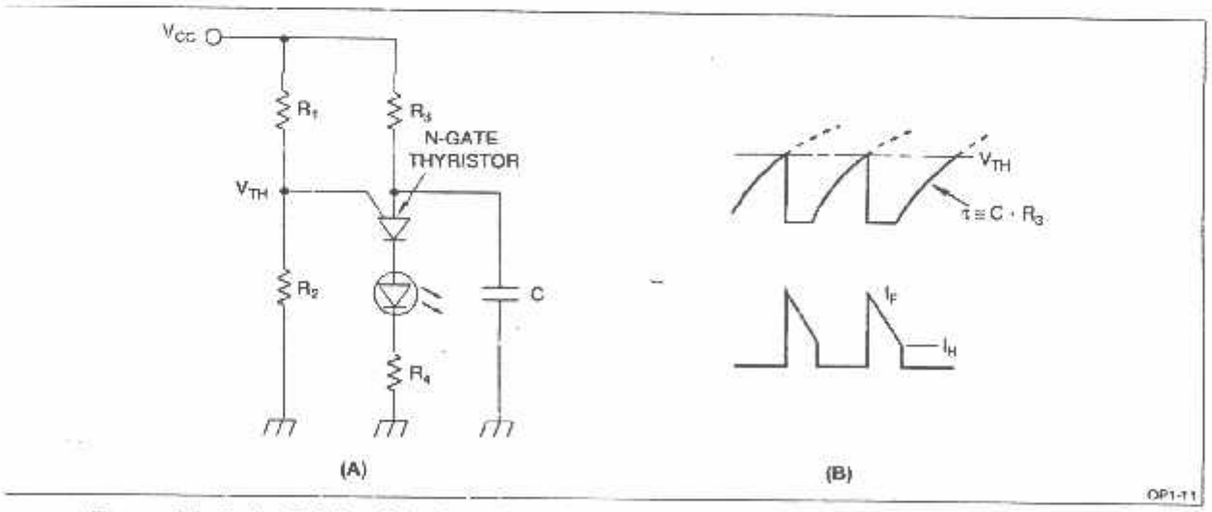

Figure 11. Pulse Driving Circuit using N-Gate Thyristor (A) and Operating Waveform (B)

The circuit shown in Figure 13 uses transistors to form an astable multi-vibrator for pulse driving an LED. The off-period (t_1) of the LED is given by $C_1 \times R_1$, while its on-period (t_2) is given by $C_2 \times R_2$. For oscillation of this circuit, resistors must be chosen so that the R_1/R_3 and R_2/R_5 ratios are large.

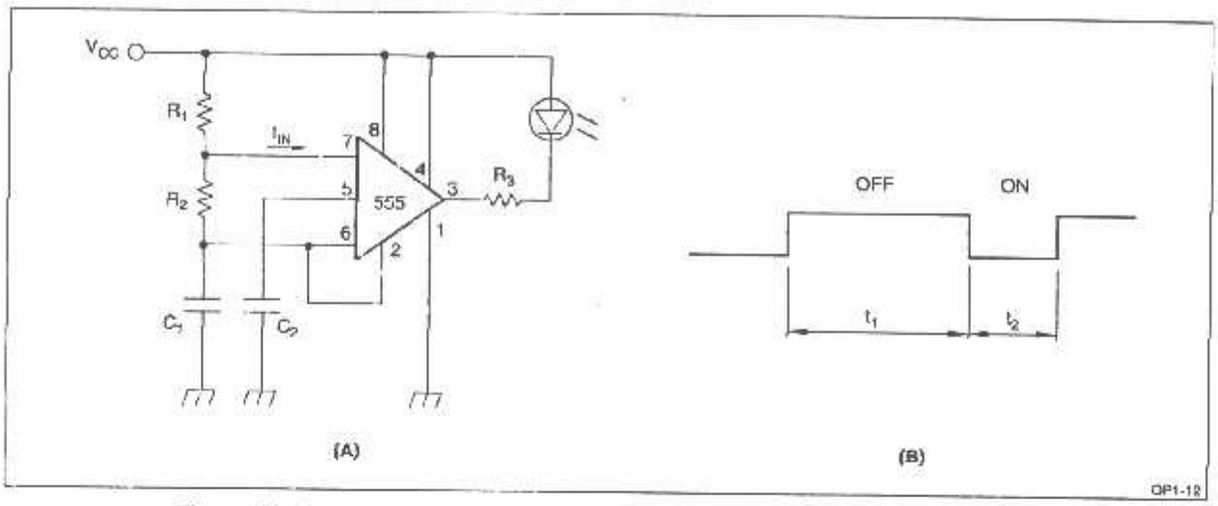

Figure 12. Pulse Driving using a 555 Timer IC (A) and Output Waveform (B)

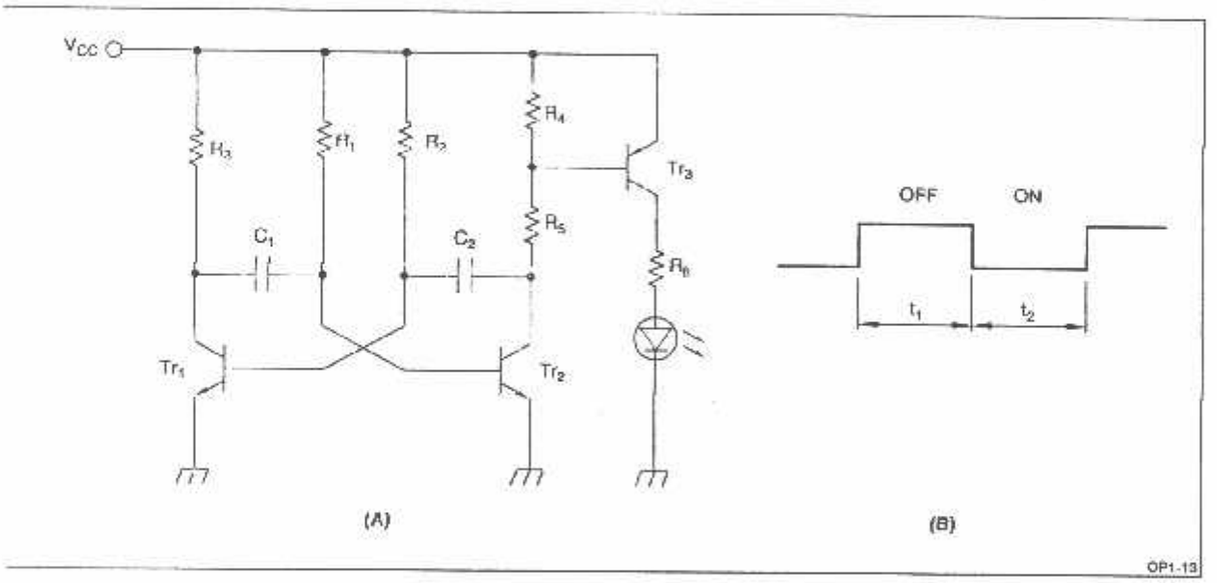

Figure 13. Pulse Driving Circuit using Astable Multi-vibrator (A) and Output Waveform (B)

The circuit shown in Figure 14 uses a CMOS logic IC (inverter) to form an oscillation circuit for pulse driving an LED. The pulse driving circuit using a logic IC provides a relatively short oscillation period with a 50% duty cycle.

Figure 15 (A) shows an LED pulse driving circuit used for the light projector of the optical remote control and optoelectronic switch. The circuit is arranged by combining two different oscillation circuits i.e., a long period oscillation (f_1) superimposed with a short period oscillation (f_2) as shown in Figure 15 (B). Frequencies f_1 and f_2 can be set independently.

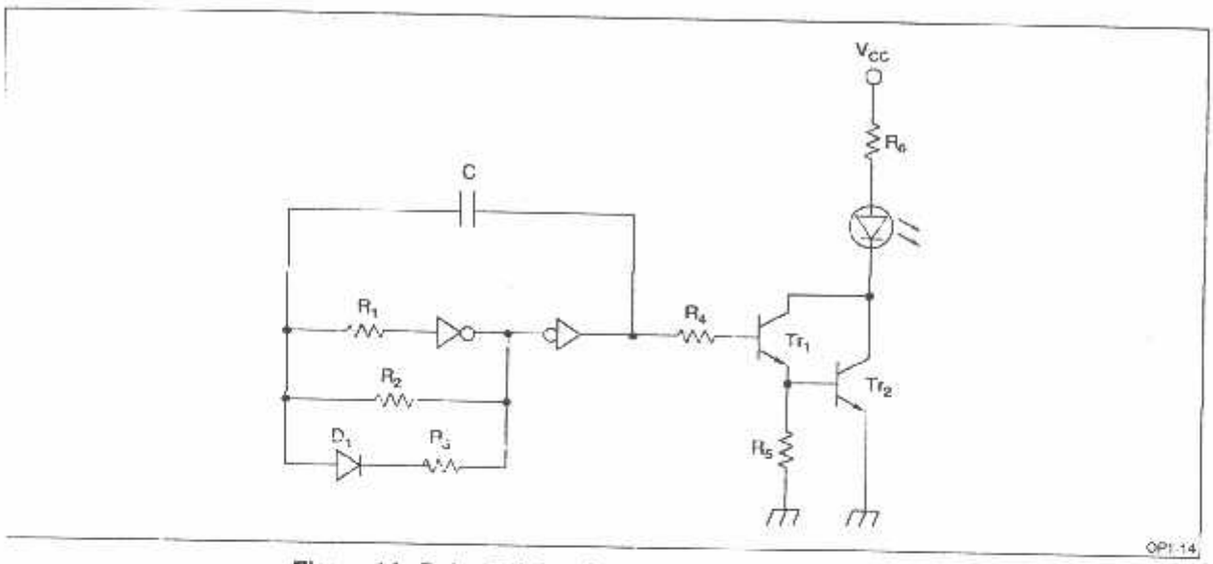

Figure 14. Pulse Driving Circuit using CMOS Logic IC

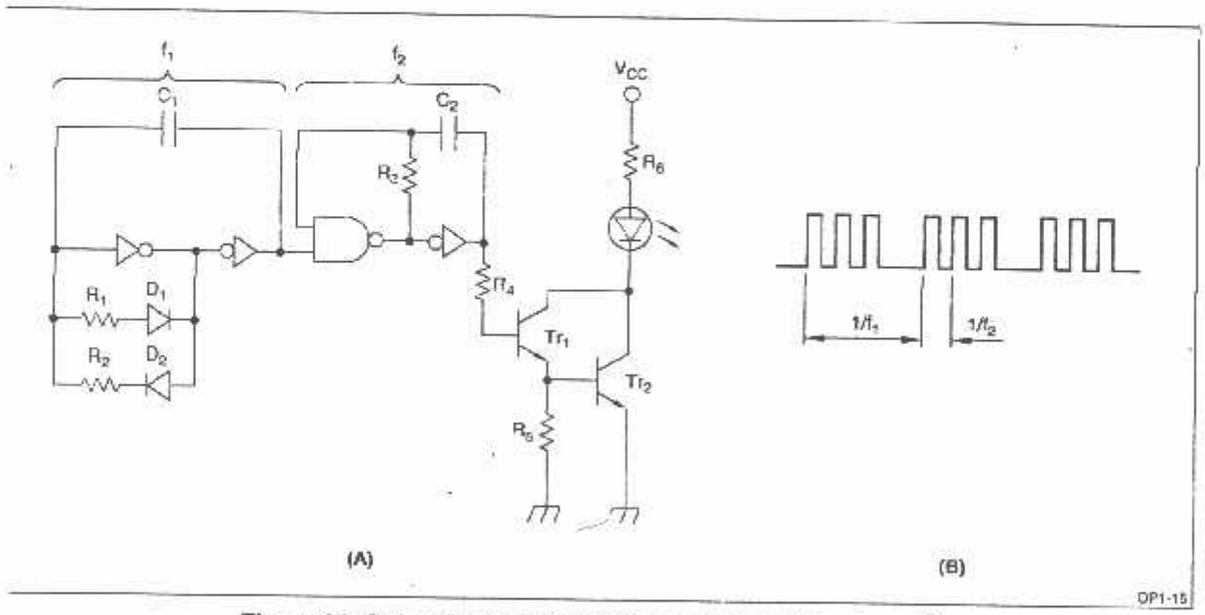

Figure 15. Pulse Driving Circuit (A) and Output Waveform (B)

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