INSTITUT TEKNOLOGI NASIONAL MALANG
FAKULTAS TEKNOLOGI INDUSTRI
JURUSAN TEKNIK ELEKTRO S-1
KONSENTRASI TEKNIK ELEKTRONIKA

PERANCANGAN DAN PEMBUATAN SISTEM KARTU PRABAYAR PADA SPBU MENGGUNAKAN TEKNOLOGI BERBASIS CPLD XS95 BOARD V1.3

SKRIPSI

Disusun Oleh :

ANDREW EKA YUSUF
NIM: 01.17.014

MARET 2006

LEMBAR PERSETUJUAN

PERANCANGAN DAN PEMBUATAN SISTEM KARTU PRABAYAR PADA SPBU MENGGUNAKAN TEKNOLOGI BERBASIS CPLD XS95 BOARD V1.3

SKRIPSI

Disusun Untuk Melengkapi dan Memenuhi Persyaratan
Guna Mencapai Gelar Sarjana Teknik Elektro Strata Satu (S-1)

Disusun Oleh :

ANDREW EKA YUSUF
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KONSENTRASI TEKNIK ELEKTRONIKA
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INSTITUT TEKNOLOGI NASIONAL MALANG
2006

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FAKULTAS TEKNOLOGI INDUSTRI
JURUSAN TEKNIK ELEKTRO S-1
KONSENTRASI TEKNIK ELEKTRONIKA

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Dipertahankan dihadapan Majelis Penguji Skripsi Jenjang Strata Satu (S-1) pada :

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بسم الله الرحمن الرحيم

Alhamdullillahirabbilalamin*Puji syukur kehadirat Allah SWT atas rahmat, taufik dan hidayahNya serta petunjuk pertolongan kemudahan dalam segala urusan serta berkah dan rahmat kepada setiap umatNya. Tak lupa Shalawat dan salam kepada junjungan besar Nabi Muhammad SAW semoga berkah dan Rahmat Allah selalu tercurah kepada beliau.*

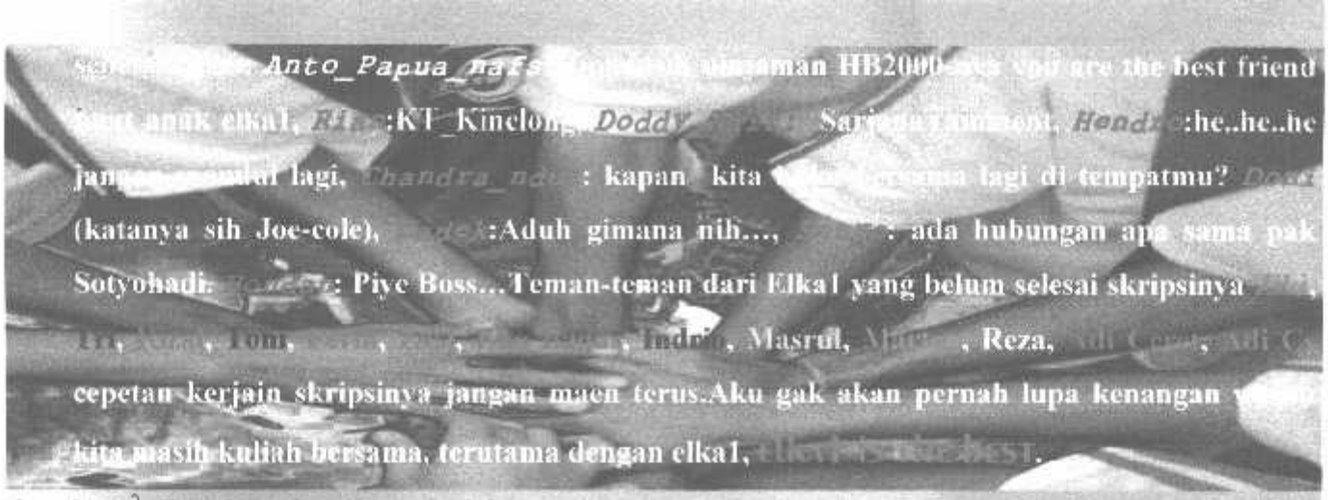
- *Skripsi ini saya persembahkan untuk ibunda* **Annara Sriwijayanti,Spd** *dan ayahanda* **Muhammad Sofyan,Spd**, *dua orang yang paling kusayangi yang ada di Balikpapan. Buat mama yang selalu ngingetin dan mendoakan serta memberikan dukungan hingga anakmu ini bisa menyelesaikan skripsinya serta papa yang selalu ngingetin untuk gak sombong dan selalu rendah hati. Gak lupa juga dukungan materi yang diberikan, maaf mas belum bisa menggantinya sekarang.*

- *Buat ketiga adikku Eva, Evi dan yang paling kecil Ade Ayu makasih ya atas dukungannya, tanpa kalian mas gak ada apa-apanya.* Buat *Ade Ayu* belajar yang bener biar pinter jangan nakal lagi ya awas kalo distrap guru lagi. Buat *Eva* jangan terlalu sibuk sama anak muridnya nanti kuliahnya ketinggalan. *Evi*...Doa dan Dukungan mas ada terus buat kamu.pokoknya gak usah takut selama masih ada mas...

- **Buat keluarga yang ada di Malang, keluarga** Bule' Gian **di Kepanjen makasih buat semuanya, n keluarga** Pakde Arif **dan** Bude Indra **makasih juga. Buat Keluarga** Om Wahyu **yang ada di Bontang,** Bule' Sus **n** Bule' Henny, Bu Ita, Om Didi **dan** Om Ed **di Balikpapan, terimakasih atas dukungannya. juga keluarga yang ada di Medan.**

- Buat **My Only One** yang selalu dihati, sebenarnya masih ada yang harus aku katakan kepadamu, aku berterima kasih atas semua dukungan, perhatian n semuanya deh yang udah kamu berikan padaku. gak tau gimana aku kalo gak ada kamu. ***You are my only, MyOnly one...***

- **Buat temen-temen elektronika angkatan 2001 terutama Elka1 mulai dari yang udah lulus seperti** *Ikhsan,ST* **(kalo ada kerjaan di Bpp hubungi aku bos).** *Gregorius,ST, Heri_77,ST* **(halo sodara, aku lulus juga),** *Khamid,ST, Aries Wahyudi,ST, Elbie Yusfianas,ST* **(makasih atas sablonannya) serta** *Kris,ST* **(the only girl) sekarang aku nyusul kalian. Temen-temen**



Anto_Papua_hati [illegible] simaman HB2000 yes you are the best friend [illegible] anak elka1, Fil[illegible]:KT_Kinelon, Doddy [illegible] Sariputra Simanjuntak, Hendr[illegible]:he..he..he jangan [illegible] lagi, Chandra_ndut : kapan kita [illegible] sama lagi di tempatmu? Dosa (katanya sih Joe-cole), [illegible]:Aduh gimana nih..., [illegible]: ada hubungan apa sama pak Sotyohadi. [illegible]: Piye Boss...Teman-teman dari Elka1 yang belum selesai skripsinya [illegible], Tri, [illegible], Toni, [illegible], [illegible], [illegible], Indri[illegible], Masrul, [illegible], Reza, [illegible], [illegible], Adi C[illegible], cepetan kerjain skripsinya jangan maen terus.Aku gak akan pernah lupa kenangan [illegible] kita masih kuliah bersama, terutama dengan elka1, [illegible] ELEKTRONIKA FOREVER BEST.

- Tmn[2] di Elektronika '01 yang lain sigit, nanang bokep sama bram makasih tumpangan tidur dikontrakkan kalian.**Rosi** (elka4) tanggal lahir jangan ikut2 dong. Si kembar oka-putra plus yoman sekalian joko-deny-yanu plus **david** (elka3) dan yang lainnya yang gak bisa disebutin satu persatu.
- Teman-teman di kost Poharin D-174A, [illegible] (maaf kalo bayarnya suka telat), **Rian Preman**, **Faisal**, **Yudha**, **Rhino**, **Surya_gundul**, [illegible] (Tiket ke Bpp berapa?) n **Lek Tajus** dan **Radit**. Teman sekaligus sahabatku **Abduh** [illegible] dan [illegible] (Kapan kita bisa sama2 lagi seperti waktu di SMA dulu).
- **Anak-anak crew Lab Elektronika digital Guntur (My Best Friend), Dian, Sulis mumun ama Cak Sundoro** (makasih pinjaman sepatunya). **trus ada Dodoy** (Gitu kau lah), **Fifi, Luppy, Nanang, Iskawan** (Makasih Boksnya) **gak lupa juga buat Mas Rido, mas Dani, mas Novan, Mas Yusup, Mas Ending, Mas Yogi ama Mas Andik,. Mbak Temi n Mas Kris yang selalu ngingetin, dan Mas Gentong yang selalu guyon maaf kalo Andrew suka bikin pakde jengkel.makasih atas semua dukungannya.**
- **Buat bapak-ibu Dosen Elektronika** [illegible], [illegible] **(Dosen pembimbingku), Pak Widodo (Dosen pembimbingku), Pak Sidik, B**[illegible] **dan dosen lain yang gak disebutkan namanya terima kasih telah membuat saya sedikit lebih pintar dari hari kemarin.**
- *Last but not least* makasih buat semuanya gak [illegible] kemana aja. Tukang [illegible], tuk warung [illegible] diperjalanan penulis serta mereka yang gak disebut [illegible] cuma bisa ucapin maaf dan makasih banyak atas [illegible] kebaikan anda.Terimakasih. *Wassalamu'alaikum.*

N-DREW 501

ABSTRAK

PERENCANAAN DAN PEMBUATAN SISTEM KARTU PRABAYAR PADA SPBU MENGGUNAKAN TEKNOLOGI BERBASIS CPLD XS95 BOARD V1.3

(Andrew Eka Yusuf,0117014,Teknik Elektro/Elektronika,61 Halaman)

(Dosen Pembimbing :Ir.Widodo Pudji Muljanto MT)

Kata Kunci: XS95 Board V1.3,AT89S51,EEPROM AT24C01A,Driver Motor AC, Xilinx Foundation 2.1i

Dengan semakin berkembangnya penggunaan alat-alat elektronika yang dapat bekerja secara otomatis sangat membantu manusia dalam memenuhi kebutuhan hidupnya.Dimana keakuratan,kestabilan serta nilai efektifitas suatu sistem operasi otomatisasi menjadi hal mutlak yang harus didapat.

Dengan menggunakan teknologi VHDL dan mikrokontroller dirancang suatu sistem yang bisa digunakan dalam pengambilan bahan bakar pada SPBU menggunakan kartu prabayar.Proses tersebut dilakukan oleh IC CPLD XC-95108PC84 sebagai pusat control.Mikrokontroller AT89S51 digunakan sebagai penampil LCD serta sebagai penulisan instruksi dan data pada EEPROM AT24C01A.

Perancangan alat ini menggunakan 2 *software* yaitu Xilinx Foundation 2.1i serta HB2000W.Program Xilinx digunakan untuk perancangan XS95 Board V1.3 dimana hasil akhir akan menghasilkan file *.svf yang kemudian didownloadkan menggunakan GXSLOAD.Sedangkan HB2000 digunakan untuk perancangan AT89S51 dan AT24C01 dimana hasil akhirnya akan menghasilkan file *.H51.Sistem ini dirancang untuk pengambilan BBM pada SPBU menggunakan kartu prabayar berupa EEPROM AT24C01 dengan driver motor AC sebagai penghasil outputan yang bisa diambil antara 1-9 liter.

KATA PENGANTAR

Dengan memanjatkan puji syukur kehadirat Allah SWT, atas limpahan Rahmat dan Hidayah-Nya, sehingga penyusun dapat menyelesaikan skripsi ini dengan judul :

"PERANCANGAN DAN PEMBUATAN SISTEM KARTU PRABAYAR PADA SPBU MENGGUNAKAN TEKNOLOGI BERBASIS CPLD XS95 BOARD V1.3 "

Skripsi ini disusun sebagai salah satu persyaratan dalam menyelesaikan studi program strata satu (S-1) Jurusan Teknik Elektro/Konsentrasi Teknik Elektronika, Fakultas Teknologi Industri, Institut Teknologi Nasional Malang.

Sebelum dan selama penyusunan skripsi ini, penyusun telah banyak mendapatkan bantuan dan bimbingan dari berbagai pihak. Untuk itu pada kesempatan ini penyusun menyampaikan terima kasih yang sebesar-besarnya kepada:

1. Bapak Dr. Ir. Abraham Lomi, MSEE, selaku Rektor Institut Teknologi Nasional Malang.
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7. Buat seseorang yang tetap dihati,terimakasih atas dukungan dan perhatiannya sehingga penulis bisa menyelesaikan skripsi.
8. Rekan-rekan di Jurusan teknik elektronika angkatan 2001 serta teman-teman di Laboratorium Elektronika Digital.
9. Semua pihak yang tidak dapat disebutkan satu per satu, yang telah membantu dalam penyelesaian skripsi ini.

Penyusun menyadari sepenuhnya akan segala kekurangan yang ada dalam penyusunan skripsi ini, maka dengan kerendahan hati penyusun mengharapkan kritik dan saran demi penyempurnaan skripsi ini.

Akhirnya penyusun berharap semoga dalam skripsi ini dapat membantu serta bermanfaat bagi rekan-rekan mahasiswa khususnya pada jurusan Teknik Elektro konsentrasi Teknik Elektronika.

Malang, Maret 2006

Andrew Eka Yusuf

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BAB I

PENDAHULUAN

1.1. Latar Belakang

Perkembangan ilmu pengetahuan dan teknologi pada saat ini semakin berkembang dengan pesat seiring dengan perkembangan zaman terutama dibidang elektronika. Salah satu perkembangan yang paling menonjol saat ini adalah perkembangan di bidang komputer selain itu adanya perkembangan teknologi *robotic*. Suatu sistem yang ditangani oleh komputer , semuanya akan terasa lebih cangih, lebih pintar, lebih otomatis dan lebih praktis serta efisien.

Sistem yang berkembang sekarang adalah sistem pengontrolan. .Salah satunya adalah teknologi VHsicHDL (*Very High Speed Integrated Circuit Hardware Description Language*).VHDL digunakan untuk menggambarkan perangkat keras untuk tujuan simulasi,pemodelan sistem dan tes perancangan dari suatu sistem digital sesuai dengan karakteristik yang diinginkan.Teknologi VHDL sekarang banyak digunakan dalam sistem pengontrolan terutama dibidang elektronika.

Penulis bermaksud membuat suatu sistem pembayaran atau pembelian BBM pada Stasiun Pengisian Bahan Bakar Umum (SPBU) dengan menggunakan kartu prabayar atau voucher yang diharapkan membantu petugas SPBU dalam hal menjalankan tugasnya untuk melakukan pengisian BBM sesuai yang diinginkan oleh konsumen dalam hal ini jenisnya yaitu Solar dan Premium (Bensin).Selain itu juga dapat menguntungkan dalam hal efisiensi waktu dimana setiap konsumen ingin membeli BBM yang diinginkan cukup memasukkan kartu dan melakukan pembayaran terlebih dahulu.

1.2. Tujuan

Penulisan skripsi ini bertujuan untuk merancang dan membuat sistem kartu prabayar/voucher yang digunakan di stasiun pengisian bahan bakar sehingga memungkinkan konsumen untuk memilih jenis BBM yang ingin dibeli.

1.3. Permasalahan

Berdasarkan latar belakang yang telah diuraikan pada bagian sebelumnya, maka permasalahannya adalah bagaimana merancang dan membuat sistem kartu prabayar pada SPBU untuk pengisian BBM menggunakan VHDL.

Sehubungan dengan hal itu, maka tugas akhir ini diberi judul

PERANCANGAN DAN PEMBUATAN SISTEM KARTU PRABAYAR PADA SPBU DENGAN MENGGUNAKAN TEKNOLOGI BERBASIS CPLD XS95 BOARD V1.3

1.4. Batasan Masalah

Dalam menyusun tugas akhir ini diperlukan suatu batasan masalah agar tidak menyimpang dari ruang lingkup yang akan dibahas. Adapun batasan masalahnya:

1. Unit pemroses utama yang digunakan adalah keypad 3x4 yang dihubungkan ke IC CPLD yaitu XS95 Board V1.3 dengan menggunakan software *Xilinx Foundation 2.1i.*
2. Sebagai penampil LCD digunakan IC mikrokontroller AT89S51.
3. Kartu yang dipakai adalah kartu berlubang memakai serial EEPROM tipe AT24C01.
4. Alat yang dibuat nantinya hanya berupa model dan simulasi.
5. Tidak membahas Power Supply.

1.5. Metodologi Penelitian

Metodologi penelitian yang dipakai dalam pembuatan tugas akhir ini adalah:

1. Study literatur
2. Perancangan dan Pembuatan alat
3. Pelaksanaan uji coba alat
4. Analisa Software dan Hardware
5. Penyusunan laporan tugas akhir

1.6. Sistematika Penulisan

Penulisan tugas akhir ini terbagi menjadi lima bab dengan sistematika sebagai berikut:

BAB I PENDAHULUAN

Berisi latar belakang, tujuan, permasalahan, batasan masalah, metodologi, dan sistematika penulisan.

BAB II TEORI PENUNJANG

Membahas teori dasar penunjang perancangan dan pembuatan alat.

BAB III PERANCANGAN DAN PEMBUATAN ALAT

Membahas tentang perancangan alat baik perangkat keras maupun perangkat lunak dan cara kerja blok diagram.

BAB IV PENGUJIAN ALAT

Mencakup pembahasan tentang proses pengujian alat yang terdiri dari peralatan yang digunakan, langkah kerja, dan analisa hasil pengujian.

BAB V PENUTUP

Berisi kesimpulan dan saran.

BAB II

DASAR TEORI

2.1 Latar Belakang VHDL

VHSIC HDL (*Very High Speed Integrated Circuit Hardware Description Language*) disingkat VHDL, VHDL adalah sebagai bahasa perangkat keras, bahasa ini dapat menyediakan format yang lengkap dan mempresentasikan fungsi secara detail, serta bisa digunakan untuk suatu simulasi, verifikasi desain, pemodelan test, perancangan dari sistem digital.

VHDL terdiri dari simbol sederhana dan notasi yang dapat menggantikan diagram skematik dari suatu rangkaian digital serta bisa berupa program simulasi yang bisa digunakan untuk verifikasi desain atau untuk membuktikan perangkat keras secara otomatis.

Dalam pencarian untuk program alat bantu dokumen dan desain standar VHSIC, Departement Pertahanan Amerika Serikat *(United States Departement of Defense, DoD)* pada musim panas 1981 mensponsori *workshop* untuk HDL di Woodnole, Massachusett. *Workshop* ini diatur oleh Institute for Defense Analysis (IDA) untuk mempelajari bermacam-macam metode deskripsi untuk hardware, keperluan standar bahasa, dan ciri-ciri yang diperlukan oleh bahasa standar tersebut.

Pada tahun 1983, Dod menetapkan bahasa VHDL, berdasarkan dari rekomendasi *workshop* di Wood hole tersebut. Ditahun 1986, VHDL diajukan sebagai standar IEEE. Setelah melalui berbagai revisi VHDL disetujui sebagai

standar IEEE 1076 pada desember 1987. Pada tahun 1988 Milsted 454 meminta agar semua ASIC dideskripsikan dalam VHDL, schingga pada tahun 1993, IEEE 1076 diperbaharui menjadi IEEE 1164 dan pada tahun 1996 menjadi IEEE 1076.3 standar sintesa VHDL.

2.1.1 Kelebihan Dan Fleksibilitas VHDL

Setiap simulasi didalam industri elektronika sudah scharusnya mempelajari VHDL untuk bisa berkompetisi dengan yang lain. Dengan perancangan VHDL, bisa membuat ribuan gerbang (*gate*) yang mana bila didesain dengan menggunakan skema atau persamaan *boole* membutuhkan waktu yang lama.

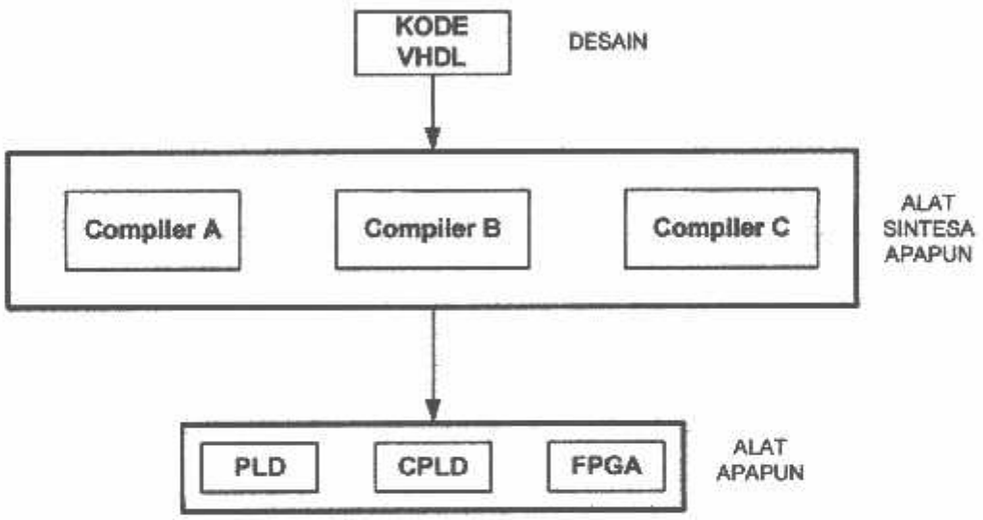
VHDL merupakan bahasa yang dapat digunakan untuk menuliskan kode deskripsi yang lebih efisien untuk mengontrol rangkaian logika schingga bisa lebih komplek. VHDL juga menyajikan pustaka desain (*design libraries*), yang dapat digunakan sebagai desain maupun simulasi.

2.1.2 Desain Alat Mandiri Dan Kecepatan Proses VHDL

VHDL memungkinkan untuk mendesain alat tanpa harus memilih terlebih dahulu pada alat apa yang akan didesain tersebut diimplementasikan, dengan demikian waktu yang ada dapat dikonsentrasikan pada desainnya. VHDL juga bisa untuk menggunakan berbagai macam deskripsi desain.

2.1.3 Portabilitas dan Kemampuan *Benchmark*

Karena VHDL merupakan standar dari setiap deskripsi desain sehingga dapat dipakai untuk berbagai macam simulasi dan sintesa. VHDL memungkinkan untuk mendesain alat dengan *architecture* alat maupun sintesa yang berbeda-beda tidak perlu memilih terlebih dahulu yang menggunakan CPLD atau FPGA. Desain dan sintesa dilakukan terlebih dahulu, baru dipilih IC. Sehingga IC-IC yang ada bisa saling dibandingkan untuk memperoleh IC yang paling tepat untuk desain.



Gambar 2-1 Portabilitas Antar Kompiler dan Desain

Dengan tingkat efisiensi yang dihasilkan oleh VHDL, maka setiap produk yang dibuat bisa memiliki fungsi seperti yang diharapkan, sehingga IC yang dibuat menjadi spesifik. Dengan VHDL maka kecepatan proses dapat ditingkatkan dan biaya untuk desain dapat ditekan. Sebuah IC PLD dapat menggantikan banyak IC logika biasa, bahkan IC pASIC dapat menggantikan sampai 100.000 buah gerbang (gate).

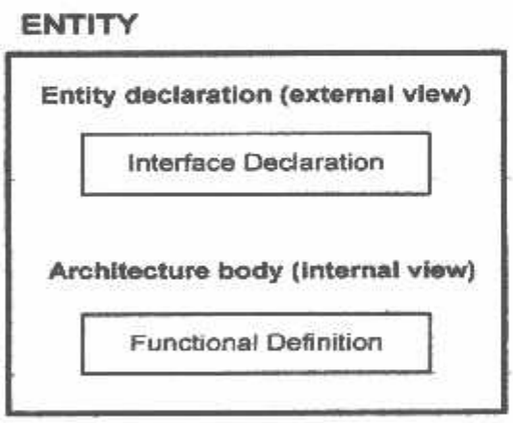
2.2 *Entity* dan *Architecture*

Dalam pembuatan desain VHDL, bergantung pada alat bantu (tools) yang digunakan, antara perusahaan satu dengan yang lain berbeda-beda, ada alat bantu yang dapat menghasilkan kode VHDL dari skema rangkaian ada juga yang tidak. Tetapi pada dasarnya, kode VHDL merupakan kode berbasis teks, yang bisa dibuat dengan menggunakan berbagai macam program kata (word processor) seperti notepad, edit, ws, dan ms word.

Azas bangunan dari desain entity VHDL terdiri dari 2 unsur, yaitu :

1. *Entity declaration*
2. *Architecture body*

Desain entity merupakan abstraksi dari suatu desain yang menggambarkan suatu sistem secara lengkap.



Gambar 2-2 Hubungan Antar Desain *Entity* dan *Architecture Body*

2.2.1 *Entity Declaration*

Entity declaration menggambarkan I/O dari desain *entity*. *Entity declaration* analog dengan skematik simbol yang menjelaskan hubungan komponen dalam

suatu desain. Signal I/O di Entity declaration didefinisikan sebagai port yang analog dengan pin dari skematik simbol.

Struktur penulisan *entity declaration* harus mengandung unsur *name* dan *port declaration*, sedangkan *port declaration* menjelaskan nama-nama pin I/O rangkaian digital dari suatu desain. *Direction* (*mode*) menjelaskan kondisi I/O dan data type menjelaskan tipe data yang digunakan (sesuai dengan standar IEEE 1076/1164).

Ada 4 macam direction (mode), yaitu ;

1. *IN* merupakan *Unidirection* data input (Aliran data berasal dari luar *entity* masuk kedalam *entity*).
2. *OUT* merupakan *Unidirection* data output (Aliran data berasal dari dalam *entity* keluar *entity*).
3. *BUFFER* merupakan data output dengan *internal feedback*. (Digunakan sebagai *port* dan *driver* dengan *architecture*, serupa dengan mode OUT tetapi juga berfungsi sebagai *internal feedback* bukan *Bidirection port*).
4. *INOUT* merupakan *Bidirection signal*. (Signal *driver* dapat berasal dari dalam atau luar *entity*, menggunakan mode INOUT ini untuk signal yang benar-benar *Bidirectional*, kalau tidak akan mengurangi kemampuan membaca kode sehingga sulit menentukan sumber signal).

Ada 2 macam Data type yang digunakan berdasarkan standar IEEE, yaitu :

1. Berdasarkan standar IEEE 1076/93, yaitu : *Boolean, Bit, Bit_vector* dan *Integer.*

2. Berdasarkan standar IEEE 1164, yaitu *Std_Ulogic, std_Logic* dan *std_Logic Vector.*

Structure penulisan *Entity Declaration*

Description
Entity entity_name is Port ([signal]{identifier{,identifier}:[mode] signal_type [signal]{identifier{,identifier}:[mode] signal_type}); End [Entity][Entity_name];

Aturan penulisan *identifier*, yaitu :

1. Karakter pertama harus *alphabetic* dan tidak boleh *numeric.*

2. Pada karakter terakhir tidak boleh tanda '_'.

3. Dua tanda '-' sebagai pemisah tidak diperbolehkan.

Signal adalah *wire* yang menghubungkan antar komponen dimana dapat berfungsi sebagai input atau output dan juga sebagai *state of memory element.*

2.2.2 *Architecture Body*

Architecture Body dalam sebuah *entity* berfungsi untuk mendeskripsikan apa yang akan dilakukan atau proses apa yang akan dikerjakan oleh perangkat keras yang didesain.

Architecture Body berhubungan erat dengan *Entity declaration* didalam desain *entity* VHDL. *Architecture body* menggambarkan fungsi dari *entity* yang sekaligus menjelaskan fungsi dari *entity* . Jika *entity declaration* ditampilkan sebagai kotak hitam yang mana input dan output itu diketahui

sedangkan apa yang ada didalam kotak itu tidak diketahui, maka *architecture body* itu adalah isi dari kotak hitam tersebut.

Sedangkan didalam *architecture body* ada beberapa jenis, anata lain :

1. *Structural description*
2. *Data flow description*
3. *Behavioral description*

Penjelasan dari masing-masing architecture body, yaitu :

1. Structural description

Perencanaan didasarkan pada pemakaian komponen (*logical gate*) pada *library* dan hubungan antar komponen-komponen tersebut (*a set of interconnected component*).

2. Data flow description

Perencanaan berdasarkan pada proses data *transfer* (dari *signal* atau dari input ke output tanpa *statement sequential*) yang merupakan sekumpulan dari *concurent assignment statement*. Perbedaan utama antara *data flow* dengan *behavioral* adalah yang satu menggunakan proses yang lain tidak. Penulisan persamaan pada data flow lebih ringkas dan mudah yaitu menggunakan *conditional signal assignment (when-else) statement*. Data flow menggunakan *concurent assignment* lebih disukai dari pada proses dan *sequential statement.*

3. Behavioral description

Perencanaan didasarkan pada proses pengerjaan *statement* antar input dan output secara *sequential*/berurutan/*step by step* dengan menggunakan

statement sequential (a set of sequential statement). Keuntungan dari *behavioral description* yang merupakan *high level description* adalah kita tidak perlu memfokuskan pada *gate level* pada desain implementasi tetapi kita fokuskan pada usaha mengakuratkan model fungsi. Proses *statement* dimulai dengan sebuah label yang diikuti dengan tanda ':' kemudian kata '*process*' dan *sensitivity list* dan dibawahnya diikuti dengan *sequential statement*, setelah bagian *sequential statement* selesai diakhiri dengan *'end process'* dan *label process*.

Yang termasuk *sequential statement*, antara lain :

a. *Process statement*
b. *If-then-else statement*
c. *Case-when statement*
d. *For-loop statement*
e. *While-loop statement*

Struktur penulisan *Architecture Body*

Description
Architecture architecture_name of entity_name is Type_declaration |signal_declaration |constan_declaration |alias_declaration |subprogram_declaratio begin {process_statement |concurent_signal_asignment_statement |component_instantion_statement |generate_statement} End [architecture][architecture_name];

2.2.3 *Declaration a Component*

Library adalah suatu tempat *directory* yang dipanggil pada saat kita mengkompile yang format desain unit kita mungkin sebuah *vendor specific format*. Kita biasanya menggunakan 2 macam *library* dalam desain kita yaitu :

- *IEEE library*
- *Work library*

IEEE Library tempat menyimpan desain unit IEEE standar seperti *package std_1164* dan *numeric_std*. Dalam perintahnya kita menggunakan *library clause : library IEEE; Work library* tempat menyimpan desain unit yang kita rancang, setelah kita merancang desain unit dan desain tersebut ingin di gunakan kembali maka kita dapat menempatkannya dalam *library work*, untuk keperluan desain yang lebih besar lagi.

Packages adalah desain unit yang dapat digunakan untuk membuat *type, component, function* dan declarasi lain untuk desain unit lain. Sebuah *package* terdiri dari sebuah *package declaration* dan *option package body*. Penulisannya adalah : **Use library_name. Package_name.item;**

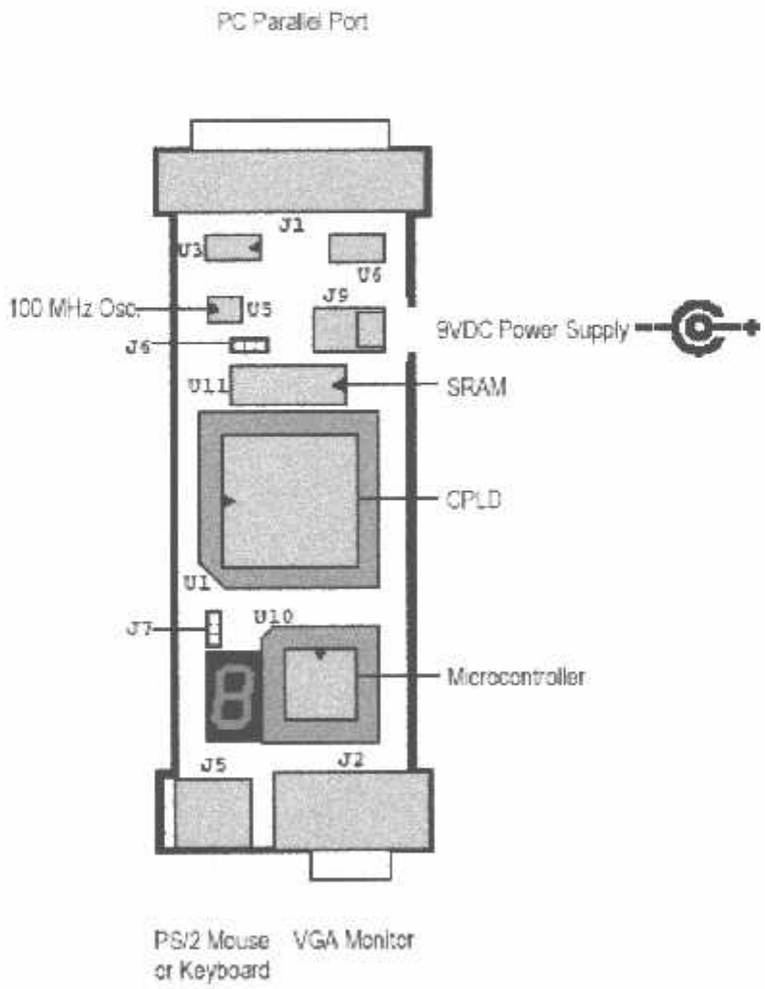
Package declaration digunakan untuk mendeklarasikan item-item seperti: ***Signal, type dan component.***

Signal menyatakan *wire-wire* yang menghubungkan antar komponen, *type* mendefinisikan *state* pada *state machine* dan *component* digunakan untuk memanggil *library component*. *Entity declaration*, *Architecture body* dan *package declaration* semuanya desain unit yang digabung dalam satu *file*. Karena *Entity*

declaration dan *package declaration* merupakan desain unit utama maka dipisah dalam *library* dan *use*.

2.3. XS95 Board V1.3

XS95 Board V1.3 adalah suatu *board* yang didalamnya terdiri dari sebuah IC CPLD XC95108-PC84 dan beberapa komponen pendukung lainnya. XS95 Board Versi 1.3 ini adalah produksi dari XESS Corporation. Berikut ini adalah gambar XS95 Board V1.3 :



Gambar 2-3 XS95 Board V1.3

2.3.1. IC CPLD XC95108-PC84

IC CPLD XC95108-PC84 adalah IC PLD buatan Xilinx, yang memiliki spesifikasi sebagai berikut :

- Delay waktu dari pin ke pin sebesar 7,5 nS dengan frekuensi maksimum125 MHz.
- Didalamnya terdapat 108 *macrocell* dengan 2400 *gate*.
- Tegangan catu daya sebesar 5 V sampai 7 V.
- Arus keluaran maksimum 24 mA.
- Memiliki dua mode tegangan I/O yaitu 3,3 V dan 5 V.
- Memiliki 84 pin yang terdiri dari :
  - 3 pin I/O/GCK adalah pin *Input/Output/Global Clock*
  - 2 pin I/O/GTS adalah pin *Input/Output/Global 3-State Control.*
  - 1 pin I/O/GSR adalah pin *Input/Output/Global Set-Reset.*
  - 3 pin V_{CCINT} 5V adalah pin input tegangan catu daya untuk *internal logic* dan *input buffer*.
  - 2 pin V_{CCIO} 3,3V/5V adalah pin input mode tegangan I/O.
  - 6 pin GND.
  - 4 pin JTAG adalah pin untuk pemrograman.
  - 69 pin I/O adalah pin Input/Output, 6 pin diantaranya termultipleks dengan pin GCK, GTS dan GSR.

2.3.2. DS1075Z100 - 100 MHz Osilator

XS95 Board V1.3 memiliki sebuah IC osilator pulsa kotak yang dapat diprogram. Frekuensi maksimum yang bisa dihasilkan oleh IC ini adalah 100MHz. Frekuensi ini bisa diturunkan dengan cara membagi dengan faktor 1,2,...sampai 2052 yang akan menghasilkan frekuensi dari 100 MHz, 50 MHz,...sampai 48,7 KHz. Untuk memprogram IC ini digunakan perangkat lunak GXSSETCLK.

2.3.3. Mikrokontroller 8031

Mikrokontroller yang ada didalam XS95 Board V1.3 adalah keluarga 8031 produksi Winbond. Mikrokontroller ini dimaksudkan untuk aplikasi desain yang menggabungkan dua teknologi dengan bahasa HDL *(Hardware Description Language)* dan SDL *(Software Description Language)* .

2.3.4. SRAM

SRAM *(Static Random Access Memory)* yang terpasang memiliki kapasitas sebesar 128Kb digunakan untuk mengirim dan menerima data dari dan ke mikrokontroller.

2.3.5. Seven Segment

Untuk kepentingan tertentu disediakan sebuah *seven segment common cathode* yang terhubung langsung dengan CPLD.

2.3.6. Konektor VGA/Monitor

Secara paralel 8 pin CPLD yang terhubung ke *seven segment* terhubung juga ke konektor VGA/Monitor. Konektor ini disediakan untuk kepentingan aplikasi yang berhubungan dengan pengendalian monitor.

2.3.7. Konektor PS/2

CPLD juga dapat mengakses *clock* dan data dari sebuah *keyboard* atau *mouse* melalui sebuah konektor PS/2.

2.3.8. Konektor PC Paralel Port

8 bit pin paralel port terhubung ke CPLD melalui konektor PC paralel port untuk kepentingan pemrograman XS95 Board V1.3 juga untuk mengakses 8 pin I/O CPLD

2.4. Mikrokontroler AT89S51

2.4.1. Pendahuluan

Perbedaan mendasar antara mikrokontroler dan mikroprosesor adalah mikrokontroler selain memiliki CPU juga dilengkapi memori dan input output yang merupakan kelengkapan sebagai sistem minimum mikrokomputer sehingga sebuah mikrokontroler dapat dikatakan sebagai mikrokomputer dalam keping tunggal *(Single Chip Microcomputer)* yang dapat berdiri sendiri.

Mikrokontroler AT89S51 adalah mikrokontroler ATMEL yang kompatibel penuh dengan mikrokontroler keluarga MCS – 51, membutuhkan daya rendah, memiliki performance yang tinggi dan merupakan mikrokomputer 8 bit yang dilengkapi 4 Kbyte EEPROM *(Electrical Erasable and Programmable Read Only Memory)* dan 128 Byte RAM internal. Program memory dapat diprogram berulang – ulang atau dengan menggunakan Programmer Nonvolatile Memory.

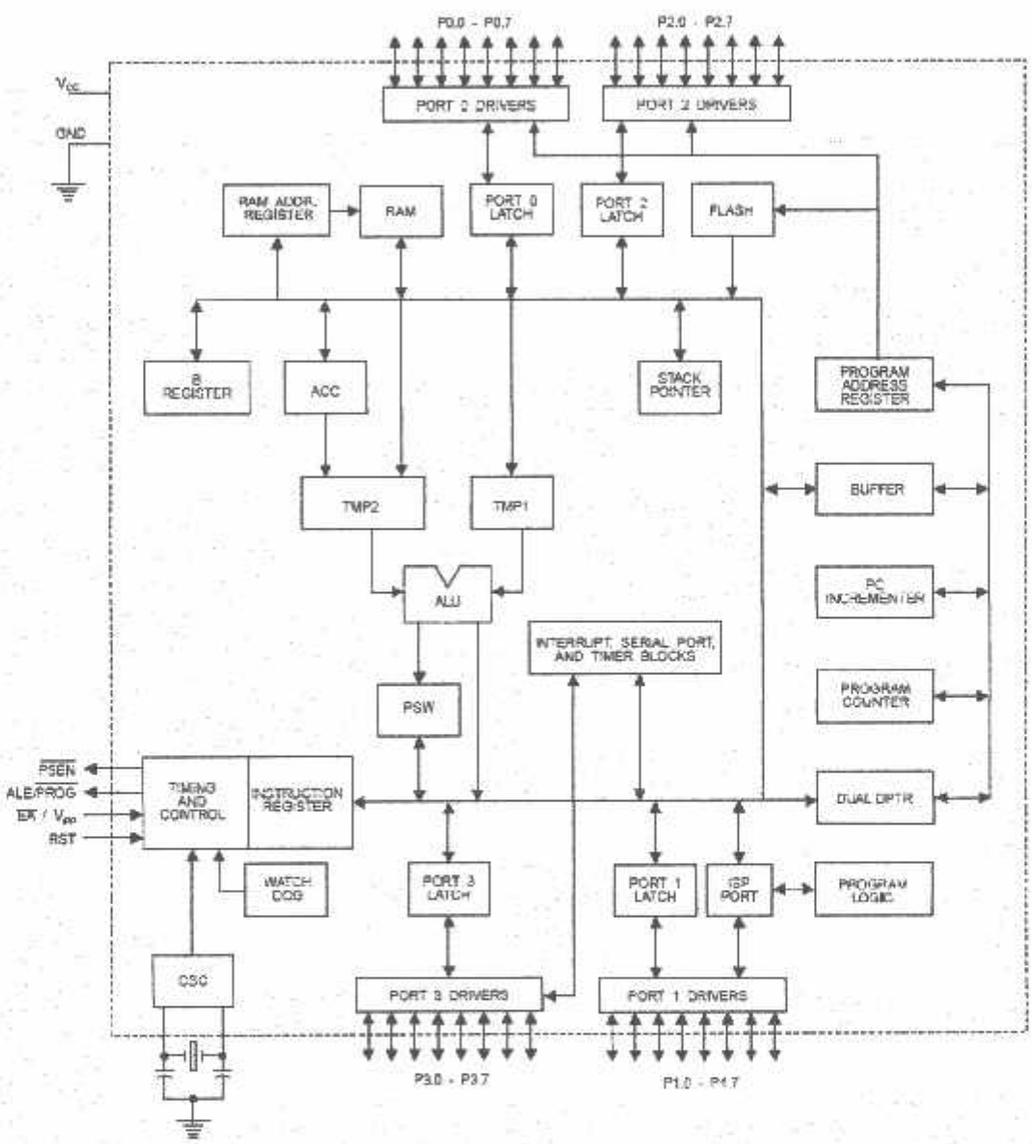
Dalam sistem mikrokontroler terdapat dua hal yang mendasar, yaitu: perangkat lunak dan perangkat keras yang keduanya saling terkait dan mendukung.

2.4.2. Perangkat keras mikrokontroler AT89S51

Secara umum Mikrokontroler AT89S51 memiliki :

- CPU 8 bit termasuk keluarga MCS-51
- 4 Kb Flash memory
- 128 byte Internal RAM
- 4 buah Port I/O, masing – masing terdiri atas 8 jalur I/O
- 2 Timer/ counter 16 bit
- 1 Serial Port Full Duplex
- Kecepatan pelaksanaan intruksi per siklus 1 us pada frekuensi clock 12 Mhz

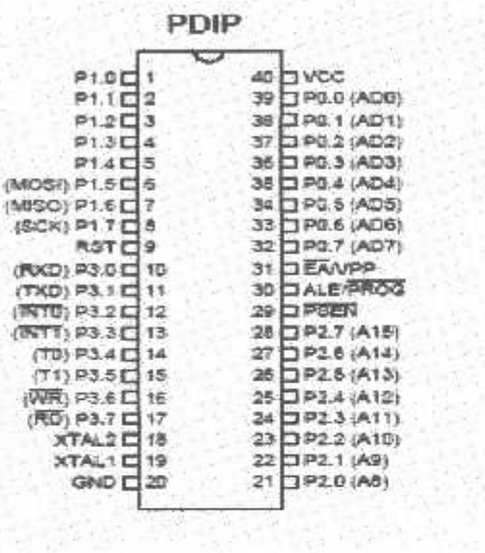
Dengan keistimewaan diatas pembuatan alat menggunakan AT89S51 menjadi lebih sederhana dan tidak memerlukan IC pendukung yang banyak. Adapun Blok Diagram dari Mikrokontroler AT89S51 adalah sebagai berikut:



Gambar 2-5 Blok Diagram Mikrokontroler AT89S51
Sumber: Data Sheet Atmel AT89S51

2.4.3. Konfigurasi Pin-Pin Mikrokontroler AT89S51

Mikrokontroler AT89S51 terdiri dari 40 pin dengan konfigurasi sebagai berikut:



Gambar 2-6 Konfigurasi Pin-Pin AT89S51
Sumber : Data Sheet Atmel AT89S51

Fungsi tiap pin-nya adalah sebagai berikut :

1. **GND** (Pin 20)

   Dihubungkan dengan Ground Rangkaian.

2. **VCC** (Pin 40)

   Dihubungkan dengan sumber tegangan +5V.

3. **Port 0** (Pin 32-39)

   Port 0 (P0.0 – P0.7) merupakan port I/O 8 bit dua arah. Port ini digunakan sebagai multipleks bus alamat rendah (A0 – A7) dan bus data selama pengaksesan ke memori eksternal.

4. **Port 1** (P1.0 – P1.7) (Pin 1-8)

   Merupakan port input – output dua arah dengan *pull-up*. Port ini berfungsi sebagai input atau output dan bekerja baik untuk operasi bit maupun byte, tergantung dari pengaturan software.

5. **Port 2** (P2.0 – P2.7) (Pin 21-28)

   Port 2 (P2.0 – P2.7) Merupakan input – output dua arah dengan *pull-up*. Port 2 mengeluarkan *high order address byte* selama pengambilan (*fetch*) program memori eksternal dan selama mengakses data memori eksternal. Port 2 juga menerima *high order address bit* dan beberapa sinyal kontrol selama pemrograman dan verifikasi.

6. **Port 3** (Pin 10-17)

   Merupakan port input-output dengan internal pull-up, dimana Port 3 juga memiliki fungsi khusus dan dapat dilihat pada tabel berikut ini:

Tabel 2-1 Fungsi Khusus Pada Port 3
Sumber : Data Sheet Atmel AT89S51

Pin Port	Fungsi Khusus
Port 3.0	RxD (Port masukan serial)
Port 3.1	TxD (Port keluaran Serial)
Port 3.2	$\overline{\text{INT0}}$ (Masukan Interupsi Eksternal 0)
Port 3.3	$\overline{\text{INT1}}$ (Masukan Interupsi Eksternal 1)
Port 3.4	T0 (Masukan Pewaktu Eksternal 0)
Port 3.5	T1 (Masukan Pewaktu Eksternal 1)
Port 3.6	$\overline{\text{WR}}$ (sinyal tulis memori data eksternal)
Port 3.7	$\overline{\text{RW}}$ (sinyal baca memori data eksternal)

7. **RST (Reset),** pin 9

   Input Reset merupakan reset master untuk AT89S51.

8. **ALE / Prog (Address Latch Enable),** pin 30

   Digunakan untuk menahan alamat memori eksternal selama pelaksanaan intruksi.

9. **PSEN (Program Strobe Enable),** pin 29

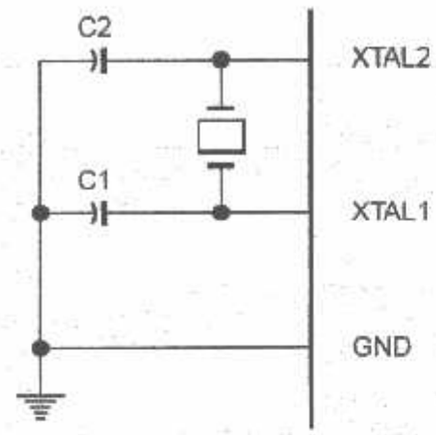
   Merupakan sinyal pengontrol yang memperbolehkan program memori eksternal masuk kedalam bus.

10. **EA / VPP (External Access),** pin 31

    Dapat diberikan logika rendah (Ground) atau logika tinggi (+5V). Jika diberikan logika tinggi maka mikrokontroler akan mengakses program dari ROM internal (EEPROM/Flash Memori), dan jika diberikan logika rendah maka mikrokontroler akan mengakses program dari memori eksternal.

11. **X-TAL 1 dan X-TAL 2,** pin 19, 18

    Pin ini dihubungkan dengan kristal bila menggunakan osilator internal. X-TAL 1 merupakan masukan ke rangkaian osilator internal sedangkan X-TAL 2 keluaran dari rangkaian osilator internal . Untuk keperluan ini diperlukan kapasitor penstabil sebesar 30pF. Dan nilai dari X-TAL tersebut antara 4 – 24 Mhz. Untuk lebih jelasnya dapat dilihat gambar pemasangan X-TAL serta kapasitor yang digunakannya.



Gambar 2-7 Osilator Eksternal AT89S51
Sumber : Data Sheet Atmel AT89S51

2.4.4. Organisasi Memory

Organisasi memori pada mikrokontroler AT89S51 dapat dibagi menjadi dua bagian besar yaitu memori program dan memori data. Pembagian tersebut didasarkan atas fungsi dari penyimpanan data maupun program. Memori program digunakan untuk menyimpan instruksi-instruksi yang akan dijalankan oleh mikrokontroler, sedangkan memori data digunakan sebagai tempat yang sedang diolah mikrokontroler.

Program mikrokontroler disimpan dalam memori program berupa ROM. Mikrokontroler 89S51 dilengkapi dengan ROM internal, sehingga untuk menyimpan program tidak digunakan ROM eksternal yang terpisah dari mikrokontroler. Agar tidak menggunakan memori program eksternal, penyemat $\overline{EA}$ dihubungkan dengan Vcc (logika 1).

Memori program mikrokontroler menggunakan alamat 16 bit mulai 0000_H-$0FFF_H$, sehingga kapasitas penyimpanan program maksimal adalah 4Kb.

Sinyal /PSEN (*Program Store Enable*) tidak digunakan jika digunakan memori program internal.

Selain program mikrokontroler 89S51 juga memiliki data internal 128 *byte* dan mampu mengakses memori data eksternal sebesar 64 Kb. Semua memori data internal dapat dialamati dengan data langsung atau tidak langsung. Ciri dari pengalamatan langsung adalah *operand* adalah alamat *register* yang berisi alamat data yang akan diolah. Sebagian memori tersebut dapat dialamati dengan pengalamatan register, dan sebagian lagi dapat dialamati dengan memori satu bit. Untuk membaca data digunakan sinyal $\overline{RD}$ sedangkan untuk menulis digunakan sinyal $\overline{WR}$.

2.4.5. SFR (Special Function Register)

Register Fungsi Khusus (*Special Function Register*) terletak pada 128 byte bagian atas memori data internal dan berisi register-register untuk pelayanan latch port, timer, program status words, control peripheral dan sebagainya. Alamat register fungsi khusus ditunjukkan pada tabel 2-2

Tabel 2-2 Special Function Register
Sumber : Bereksperimen Dengan Mikrokontroller 8031

Simbol	Nama Register	Alamat
ACC	Accumulator	$E0_H$
B	Register B	$F0_H$
PSW	Program Status Word	$D0_H$
SP	Stack Pointer	81_H
DPTR	Data Pointer 2 Byte	
DPL	Bit rendah	82_H
DPH	Bit Tinggi	83_H
P0	Port 0	80_H

P1	Port 1	90_H
P2	Port 2	$A0_H$
P3	Port 3	$B0_H$
IP	Interupt Periority Control	$D8_H$
IE	Interupt Enable Control	$A8_H$
TMOD	Timer/Counter Mode Control	89_H
TCON	Timer/Counter Control	88_H
TH0	Timer/Counter 0 High Control	$8C_H$
TL0	Timer/Counter 0 Low Control	$8A_H$
TH1	Timer/Counter 1 High Control	$8D_H$
TL1	Timer/Counter 1 Low Control	$8B_H$
SCON	Serial Control	98_H
SBUF	Serial Data Buffer	99_H
PCON	Power Control	87_H

Beberapa macam register fungsi khusus yang sering digunakan adalah sebagai berikut ini :

- *Accumulator* (ACC) merupakan register untuk penambahan dan pengurangan. Perintah *mnemonic* untuk mengakses akumulator disederhanakan sebagai A.
- *Register B* merupakan register khusus yang berfungsi melayani operasi perkalian dan pembagian.
- *Stack Pointer* (SP) merupakan register 8 bit yang dapat diletakkan di alamat manapun pada RAM internal.
- *Data Pointer* (DPTR) terdiri dari dua register, yaitu untuk byte tinggi (Data Pointer High, DPH) dan byte rendah (Data Pointer Low, DPL) yang berfungsi untuk mengunci alamat 16 bit.

- *Port 0* sampai *Port 3* merupakan register yang berfungsi untuk membaca dan mengeluarkan data pada port 0, 1, 2, 3. Masing-masing register ini dapat dialamati per-byte maupun per-bit.
- *Control Register* terdiri dari register yang mempunyai fungsi kontrol. Untuk mengontrol sistem interupsi, terdapat dua register khusus, yaitu register IP (*Interupt Priority*) dan register IE (*Interupt Enable*). Untuk mengontrol pelayanan timer/counter terdapat register khusus, yaitu register TCON (*timer/counter control*) serta pelayanan port serial menggunakan register SCON (*Serial Port Control*).

2.4.6. Sistem Interupsi

Mikrokontroler AT89S51 mempunyai 5 buah sumber interupsi yang dapat membangkitkan permintaan interupsi, yaitu INT0, INT1, T1, T2 dan Port Serial.

Saat terjadinya interupsi mikrokontroler secara otomatis akan menuju ke subrutin pada alamat tersebut. Setelah interupsi selesai dikerjakan, mikrokontroler akan mengerjakan program semula. Tiap-tiap sumber interupsi dapat enable atau disable secara software.

Tingkat prioritas semua sumber *interupt* dapat diprogram sendiri-sendiri dengan *set* atau *clear* bit pada (*Interupt Priority*). Jika dua permintaan interupsi dengan tingkat prioritas yang berbeda diterima secara bersamaan, permintaan interupsi dengan prioritas tertinggi yang akan dilayani. Jika permintaan interupsi

dengan prioritas yang sama diterima bersamaan, akan dilakukan polling untuk menentukan mana yang akan dilayani. Bit-bit pada IP adalah sebagai berikut:

-	-	-	PS	PT1	PX1	PT0	PX0

Priority bit = 1 menandakan prioritas tinggi

Priority bit = 0 menandakan prioritas rendah

Simbol	Posisi	Fungsi
-	IP.7	Kosong
-	IP.6	Kosong
-	IP.5	Kosong
PS	IP.4	Bit prioritas interupsi port serial
PT1	IP.3	Bit prioritas interupsi Timer 1
PX1	IP.2	Bit prioritas interupsi $\overline{INT1}$
PT0	IP.1	Bit prioritas interupsi Timer 0
PX0	IP.0	Bit prioritas interupsi $\overline{INT0}$

Tabel 2-3 Alamat Sumber Interupsi
Sumber : Bereksperimen Dengan Mikrokontroller 8031

Sumber interupsi	Alamat Awal
Interupt Luar 0 (INT 0)	03_H
Pewaktu / pencacah 0 (T0)	$0B_H$
Interupt Luar 1 (INT 0)	13_H
Pewaktu / pencacah 0 (T0)	$1B_H$
Port Serial	23_H

2.5. LCD (Liquid Crystal Display)

Liquid Crystal Display adalah modul tampilan yang mempunyai konsumsi daya yang relatif rendah dan terdapat sebuah controller CMOS didalamnya. Controller tersebut sebagai pembangkit ROM/RAM dan display data RAM. Semua fungsi tampilan di kontrol oleh suatu instruksi modul LCD dapat dengan mudah diinterfacekan dengan MPU. Ciri-ciri dari LCD M1632:

- Terdiri dari 32 karakter yang dibagi menjadi 2 baris dengan display dot matrik 5 X 7 ditambah cursor
- Karakter generator ROM dengan 192 karakter
- Karakter generator RAM dengan 8 tipe karakter
- 80 X 8 bit display data RAM
- Dapat diinterfacekan dengan MPU 8 atau 4 bit
- Dilengkapi fungsi tambahan : Display clear, cursor home, display ON/OFF, cursor ON/ OFF, display character blink, cursor shift dan display shift
- Internal data
- Internal otomatis dan reset pada power ON
- +5 V power supply tunggal

Berikut ini merupakan pin-pin LCD berserta konfigurasinya:

Tabel 2-4 Pin-Pin LCD Dan Konfigurasinya
Sumber : LCD Module User Manual

Nama pin	jumlah	I/O	Tujuan	Fungsi
DB0-DB3	4	I/O	MPU	Tri state bidirectional lower data bus: data dibaca dari modul ke MPU atau dari MPU ditulis ke modul melalui bus
DB4-DB7	4	I/O	MPU	Tri state bidirectional upper fourdata bus: data dibaca dari modul ke MPU atau dari MPU ditulis ke modul melalui bus
E	1	Input	MPU	Sinyal operasi dimulai: sinyal aktif baca/tulis
R/W	1	Input	MPU	Sinyalpilih data dan tulis (0:tulis,1:baca)
RS	1	-	Power supply	Sinyal pilih register 0: Instruction register (write) Busy flag dan addess counter (read) 1:Data register (write dan read)
VLC	1	-	Power supply	Penyetelan kontras pada tampilan LCD
VDD	1	-	Power supply	+ 5V
VSS	1	-	Power supply	Ground 0V

2.5.1. Register

Control LCD mempunyai 2 register 8 bit yaitu *Instruction register* (IR) dan *Data Register* (DR). Kedua register tersebut dipilih melalui *Register Select* (RS). IR menyimpan kode instruksi seperti Display clear dan cursor shift, dan alamat informasi dari Display Data RAM (DD RAM) dan character generator RAM (CG RAM)

DR menyimpan data sementara untuk ditulis ke DD RAM atau CG RAM, atau dibaca dari DD RAM atau CG RAM. Ketika data ditulis ke DD RAM atau CG RAM dari MPU, data di DR secara otomatis ditulis ke DD RAM atau CG RAM dengan operasi internal. Tetapi ketika data dibaca dari DD RAM atau CG RAM maka alamat data ditulis pada IR.Data tersebut akan dimasukkan ke DR dan MPU akan membaca data dari DR, Setelah operasi pembacaan, alamat berikutnya diset data dari DD RAM atau CG RAM pada alamat tersebut akan dimasukkan ke DR untuk operasi berikutnya.

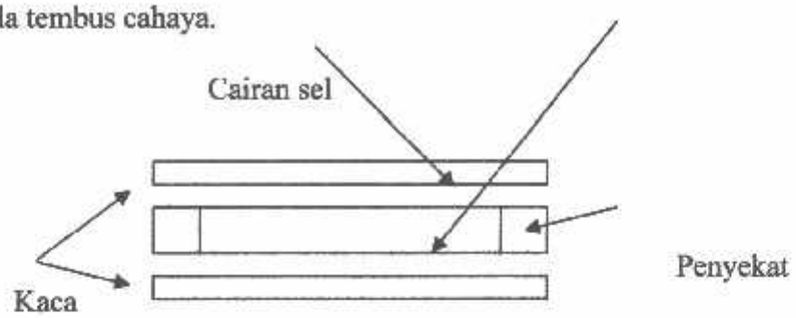
Display data RAM (DD RAM) mempunyai kapasitas area 80 X 8 bit. Beberapa area dari DDRAM yang tidak digunakan untuk display dapat digunakan sebagai General data RAM.

Pada LCD masing-masing pin mempunyai range alamat tersendiri, alamat itu diekspresikan dengan bilangan heksa. Untuk line 1 range alamat berkisar antara 00h-0Fh sedangkan untuk line 2 alamat berkisar antara 40h-4fh

2.5.2.Encoder

Informasi atau data ada kalanya dikodekan dalam bentuk kode. Untuk mengkode data digital tersebut digunakan suatu encoder. Salah satu contoh dari encoder adalah encoder 16 to 4 line yang digunakan untuk mengkode 16 saluran data desimal menjadi 4 saluran data BCD. Keluaran encoder merupakan kode dari salah satu input yang diaktifkan. Encoder mempunyai 2^n masukan dan n buah jalur keluaran.

Penggunaan encoder pada umumnya digunakan untuk mengkodekan Elektroda tembus cahaya.



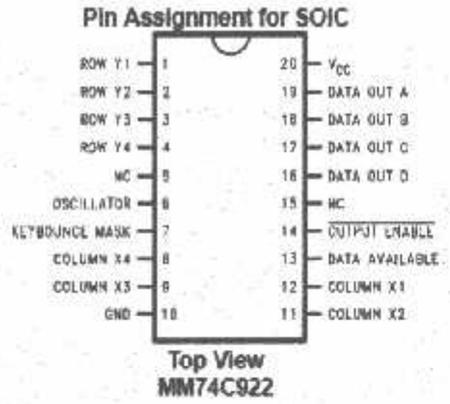
Gambar 2-8 Konstruksi dari Cairan Sel Kristal

Sumber : LCD Module User Manual

2.6. Keypad 4X3

Keypad digunakan sebagai sarana memasukan input data ke XS95108 PC84 yaitu sebagai tombol tekan guna pengoperasian dan pemilihan type bahan bakar yang akan dipilih. Untuk rangkaian keypad digunakan encoder jenis CMOS IC MM74C922. IC MM74C922 merupakan IC encoder 8 ke 4 jadi data yang menuju XS95108 merupakan data 4 bit. Dipilih jenis ini karena didalam IC tersebut sudah memiliki kelengkapan, seperti misalnya rangkaian anti dedouncing yang hanya memerlukan satu kapasitor eksternal. Rangkaian internal register akan mengingat data tombol terakhir yang ditekan, meskipun tombol sudah dilepas.

IC ini memiliki 4 bagian baris dan 4 bagian kolom sehingga dapat dipakai sebagai keypad 4x4. Konfigurasi dapat dilihat pada gambar dibawah ini.



Gambar 2-9 Konfigurasi Pin IC 74C922

Karateristik dari IC 74C922 adalah sebagai berikut:

- Saklar dengan resistansi maksimum 50 kΩ
- Clock chip on atau off
- Devais pull-up
- Roll-over 2 kunci
- Eliminasi keybounce dengan kapasitor tunggal
- Register kunci terakhir pada keluaran
- Jangkauan catu daya yang lebar 3V-15V
- Konsumsi daya rendah

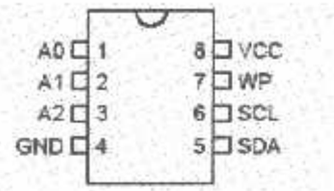
2.7. SERIAL EEPROM AT24C01

EEPROM merupakan salah satu terobosan baru dalam teknologi memori karena komponen ini merupakan perpaduan antara keunggulan memori RAM yang mampu dibaca maupun ditulis dengan mudah.Keunggulan memori EEPROM dapat menyimpan data secara permanen walaupun power supply yang terhubung kekomponen tersebut dimatikan.

Data ataupun program yang ada di dalam EEPROM hanya akan berubah jika terjadi penulisan kembali data atau program baru ke lokasi yang sama dalam komponen tersebut.Dengan digunakannya EEPROM pembuat program dengan mudah melakukan *update* atau perbaikan terhadap program yang telah tersimpan sebelumnya dalam memori tersebut hanya dengan menumpuk langsung program yang baru kedalamnya.

Oleh karena itu,EEPROM sangat sesuai pada sistem mikrokontroller berupa *Development System* ,yaitu sebuah sistem aplikasi yang dapat meng-update dan merevisi program yang ada didalamnya dengan mudah.

Serial EEPROM (*Erasable Electrical Programmable Read Only Memory*) digunakan sebagai penyimpan data tambahan dari Mikrokontroller AT89S51.Serial EEPROM AT24C01 digunakan sebagai penyimpan jumlah voucher pada kartu prabayar.Serial EEPROM AT24C01 memiliki ciri-ciri sebagai berikut:



Gambar 2-10 Konfigurasi Pin IC Serial EEPROM AT24C01

Berikut ini merupakan konfigurasi dari Pin-Pin Serial EEPROM AT24C01, adalah:

Tabel 2-5 Pin-Pin Serial EEPROM AT24C01 dan Konfigurasinya
Sumber : Data Sheet AT24C01

PIN Name	Fungsi
A0-A2	Address Inputs
SDA	Serial Data
SCL	Serial Clock Input
WP	Write Protect
NC	Not Connect

BAB III

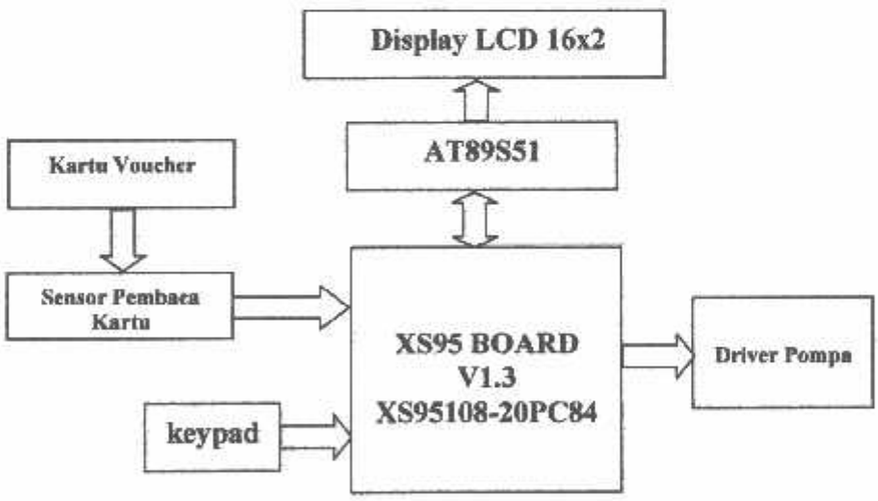
PERANCANGAN HARDWARE DAN SOFTWARE

Bab ini akan membahas tentang perencanaan dan perancangan alat yang meliputi perencanaan perangkat keras (Hardware) dan perangkat lunak (Software) dari Sistem kartu prabayar pada SPBU secara otomatis ini. Perancangan secara keseluruhan dapat dibagi menjadi dua bagian, yaitu :

1. Perancangan Hardware
2. Perancangan Software

3.1 PERANCANGAN HARDWARE

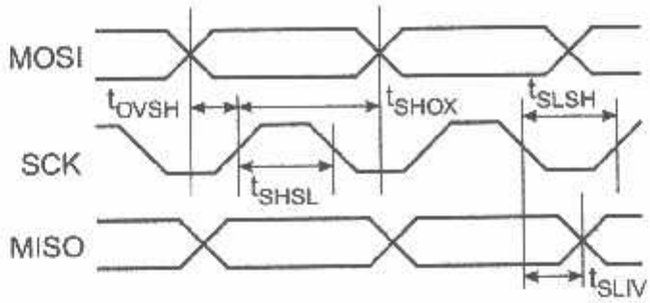
Blok diagram sistem sebagai berikut :



Gambar 3-1 Diagram Blok Sistem

ıl Programming Characteristics

ɜ 9. Serial Programming Timing



9. Serial Programming Characteristics, T_A = -40° C to 85° C, V_{CC} = 4.0 - 5.5V (Unless Otherwise Noted)

ɔol	Parameter	Min	Typ	Max	Units
:L	Oscillator Frequency	0		33	MHz
	Oscillator Period	30			ns
	SCK Pulse Width High	8 t_{CLCL}			ns
	SCK Pulse Width Low	8 t_{CLCL}			ns
	MOSI Setup to SCK High	t_{CLCL}			ns
	MOSI Hold after SCK High	2 t_{CLCL}			ns
	SCK Low to MISO Valid	10	16	32	ns
ɛ	Chip Erase Instruction Cycle Time			500	ms
	Serial Byte Write Cycle Time			64 t_{CLCL} + 400	µs

lute Maximum Ratings*

ng Temperature	-55°C to +125°C
Temperature	-65°C to +150°C
on Any Pin spect to Ground	-1.0V to +7.0V
m Operating Voltage	6.6V
put Current	15.0 mA

*NOTICE: Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

haracteristics

es shown in this table are valid for T_A = -40°C to 85°C and V_{CC} = 4.0V to 5.5V, unless otherwise noted.

	Parameter	Condition	Min	Max	Units
	Input Low Voltage	(Except $\overline{EA}$)	-0.5	0.2 V_{CC}-0.1	V
	Input Low Voltage ($\overline{EA}$)		-0.5	0.2 V_{CC}-0.3	V
	Input High Voltage	(Except XTAL1, RST)	0.2 V_{CC}+0.9	V_{CC}+0.5	V
	Input High Voltage	(XTAL1, RST)	0.7 V_{CC}	V_{CC}+0.5	V
	Output Low Voltage[1] (Ports 1,2,3)	I_{OL} = 1.6 mA		0.45	V
	Output Low Voltage[1] (Port 0, ALE, $\overline{PSEN}$)	I_{OL} = 3.2 mA		0.45	V
	Output High Voltage (Ports 1,2,3, ALE, $\overline{PSEN}$)	I_{OH} = -60 µA, V_{CC} = 5V ±10%	2.4		V
		I_{OH} = -25 µA	0.75 V_{CC}		V
		I_{OH} = -10 µA	0.9 V_{CC}		V
	Output High Voltage (Port 0 in External Bus Mode)	I_{OH} = -800 µA, V_{CC} = 5V ±10%	2.4		V
		I_{OH} = -300 µA	0.75 V_{CC}		V
		I_{OH} = -80 µA	0.9 V_{CC}		V
	Logical 0 Input Current (Ports 1,2,3)	V_{IN} = 0.45V		-50	µA
	Logical 1 to 0 Transition Current (Ports 1,2,3)	V_{IN} = 2V, V_{CC} = 5V ±10%		-650	µA
	Input Leakage Current (Port 0, $\overline{EA}$)	0.45 < V_{IN} < V_{CC}		±10	µA
	Reset Pulldown Resistor		50	300	KΩ
	Pin Capacitance	Test Freq. = 1 MHz, T_A = 25°C		10	pF
	Power Supply Current	Active Mode, 12 MHz		25	mA
		Idle Mode, 12 MHz		6.5	mA
	Power-down Mode[2]	V_{CC} = 5.5V		50	µA

1. Under steady state (non-transient) conditions, I_{OL} must be externally limited as follows:
   Maximum I_{OL} per port pin: 10 mA
   Maximum I_{OL} per 8-bit port:
   Port 0: 26 mA Ports 1, 2, 3: 15 mA
   Maximum total I_{OL} for all output pins: 71 mA
   If I_{OL} exceeds the test condition, V_{OL} may exceed the related specification. Pins are not guaranteed to sink current greater than the listed test conditions.
2. Minimum V_{CC} for Power-down is 2V.

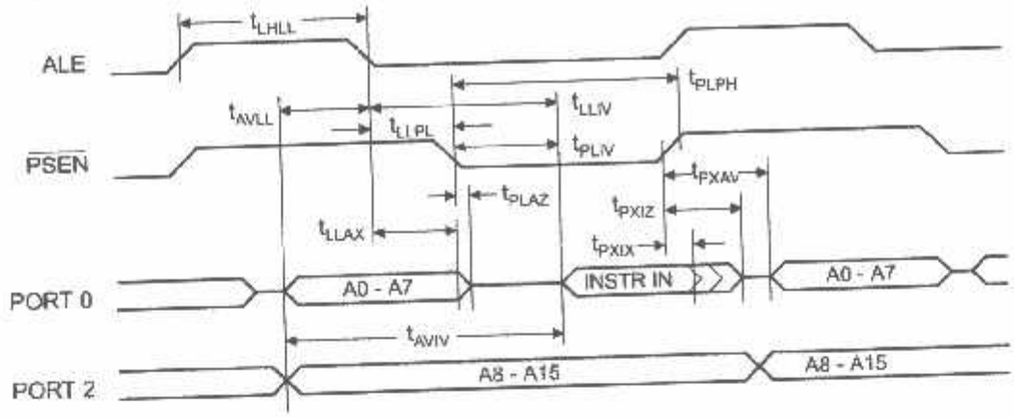
haracteristics

perating conditions, load capacitance for Port 0, ALE/$\overline{PROG}$, and $\overline{PSEN}$ = 100 pF; load capacitance for all other = 80 pF.

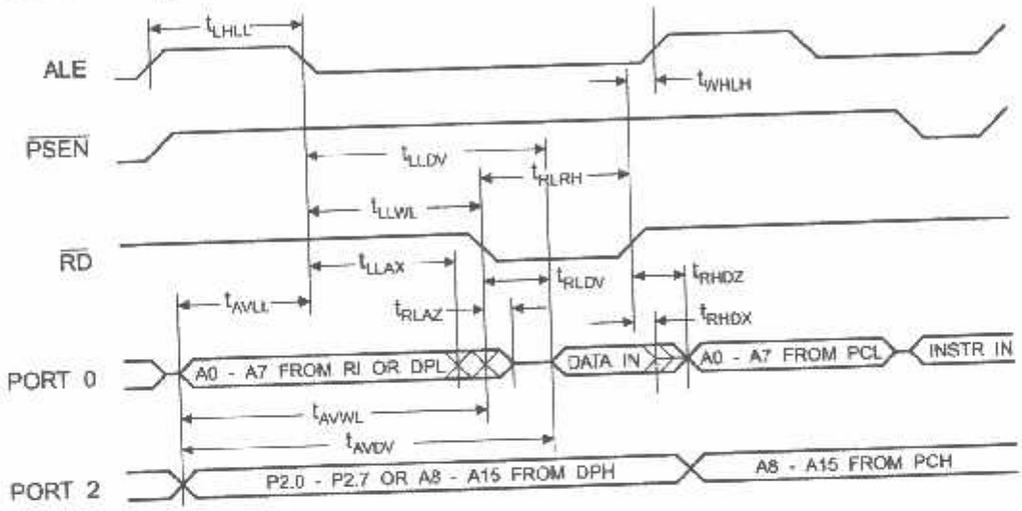
nal Program and Data Memory Characteristics

	12 MHz Oscillator		Variable Oscillator		
Parameter	Min	Max	Min	Max	Units
Oscillator Frequency			0	33	MHz
ALE Pulse Width	127		$2t_{CLCL}$-40		ns
Address Valid to ALE Low	43		t_{CLCL}-25		ns
Address Hold After ALE Low	48		t_{CLCL}-25		ns
ALE Low to Valid Instruction In		233		$4t_{CLCL}$-65	ns
ALE Low to $\overline{PSEN}$ Low	43		t_{CLCL}-25		ns
$\overline{PSEN}$ Pulse Width	205		$3t_{CLCL}$-45		ns
$\overline{PSEN}$ Low to Valid Instruction In		145		$3t_{CLCL}$-60	ns
Input Instruction Hold After $\overline{PSEN}$	0		0		ns
Input Instruction Float After $\overline{PSEN}$		59		t_{CLCL}-25	ns
$\overline{PSEN}$ to Address Valid	75		t_{CLCL}-8		ns
Address to Valid Instruction In		312		$5t_{CLCL}$-80	ns
$\overline{PSEN}$ Low to Address Float		10		10	ns
$\overline{RD}$ Pulse Width	400		$6t_{CLCL}$-100		ns
$\overline{WR}$ Pulse Width	400		$6t_{CLCL}$-100		ns
$\overline{RD}$ Low to Valid Data In		252		$5t_{CLCL}$-90	ns
Data Hold After $\overline{RD}$	0		0		ns
Data Float After $\overline{RD}$		97		$2t_{CLCL}$-28	ns
ALE Low to Valid Data In		517		$8t_{CLCL}$-150	ns
Address to Valid Data In		585		$9t_{CLCL}$-165	ns
ALE Low to $\overline{RD}$ or $\overline{WR}$ Low	200	300	$3t_{CLCL}$-50	$3t_{CLCL}$+50	ns
Address to $\overline{RD}$ or $\overline{WR}$ Low	203		$4t_{CLCL}$-75		ns
Data Valid to $\overline{WR}$ Transition	23		t_{CLCL}-30		ns
Data Valid to $\overline{WR}$ High	433		$7t_{CLCL}$-130		ns
Data Hold After $\overline{WR}$	33		t_{CLCL}-25		ns
$\overline{RD}$ Low to Address Float		0		0	ns
$\overline{RD}$ or $\overline{WR}$ High to ALE High	43	123	t_{CLCL}-25	t_{CLCL}+25	ns

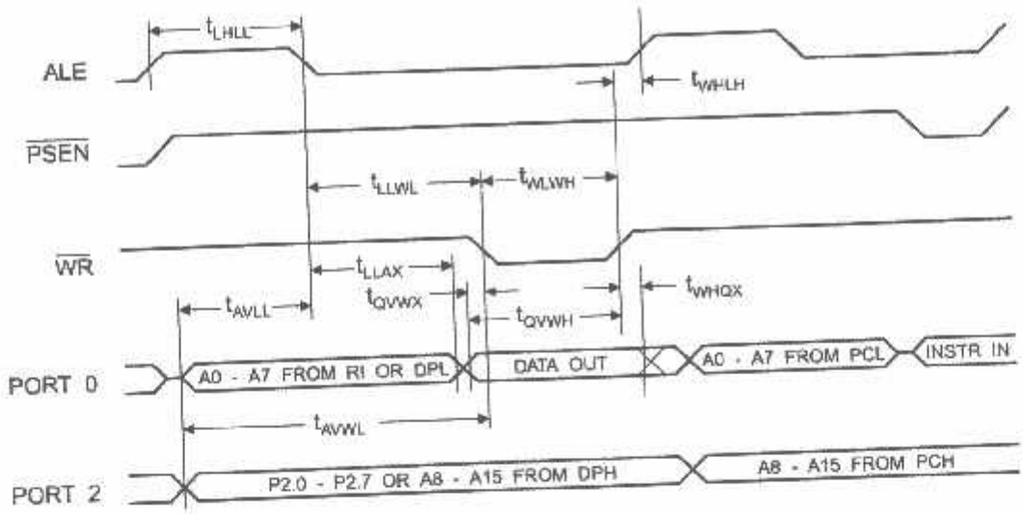
nal Program Memory Read Cycle



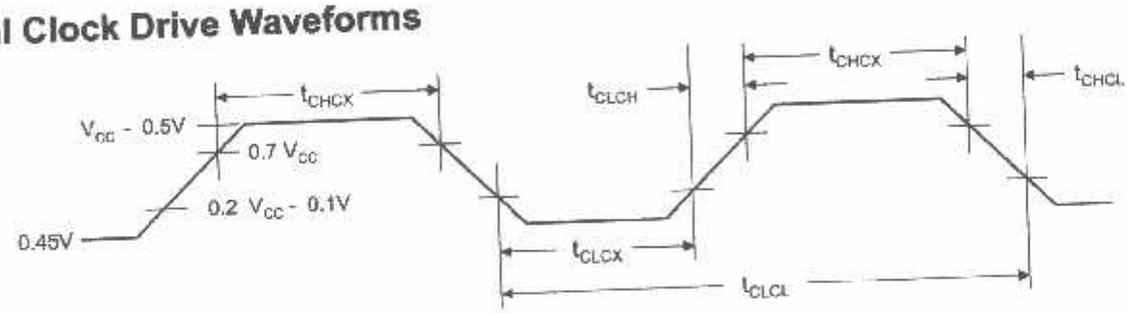
nal Data Memory Read Cycle



nal Data Memory Write Cycle



nal Clock Drive Waveforms



nal Clock Drive

	Parameter	Min	Max	Units
	Oscillator Frequency	0	33	MHz
	Clock Period	30		ns
	High Time	12		ns
	Low Time	12		ns
	Rise Time		5	ns
	Fall Time		5	ns

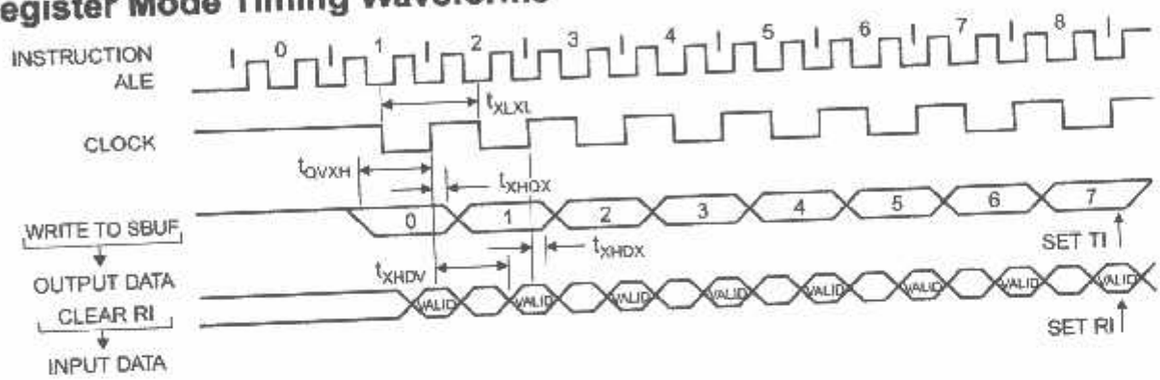
1

Port Timing: Shift Register Mode Test Conditions

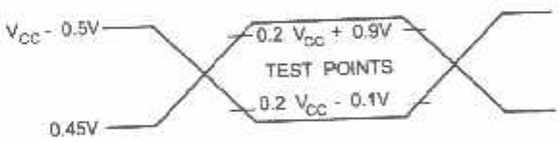
ies in this table are valid for V_{CC} = 4.0V to 5.5V and Load Capacitance = 80 pF.

	Parameter	12 MHz Osc		Variable Oscillator		Units
		Min	Max	Min	Max	
	Serial Port Clock Cycle Time	1.0		$12t_{CLCL}$		µs
	Output Data Setup to Clock Rising Edge	700		$10t_{CLCL}$-133		ns
	Output Data Hold After Clock Rising Edge	50		$2t_{CLCL}$-80		ns
	Input Data Hold After Clock Rising Edge	0		0		ns
	Clock Rising Edge to Input Data Valid		700		$10t_{CLCL}$-133	ns

Register Mode Timing Waveforms

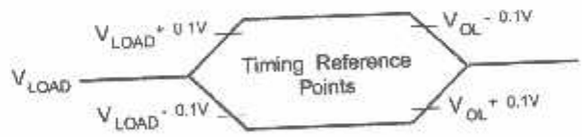


sting Input/Output Waveforms(1)



. AC Inputs during testing are driven at V_{CC} - 0.5V for a logic 1 and 0.45V for a logic 0. Timing measurements are made at V_{IH} min. for a logic 1 and V_{IL} max. for a logic 0.

Waveforms(1)



. For timing purposes, a port pin is no longer floating when a 100 mV change from load voltage occurs. A port pin begins to float when a 100 mV change from the loaded V_{OH}/V_{OL} level occurs.

ing Information

d)	Power Supply	Ordering Code	Package	Operation Range
	4.0V to 5.5V	AT89S51-24AC AT89S51-24JC AT89S51-24PC	44A 44J 40P6	Commercial (0° C to 70° C)
		AT89S51-24AI AT89S51-24JI AT89S51-24PI	44A 44J 40P6	Industrial (-40° C to 85° C)
	4.5V to 5.5V	AT89S51-33AC AT89S51-33JC AT89S51-33PC	44A 44J 40P6	Commercial (0° C to 70° C)

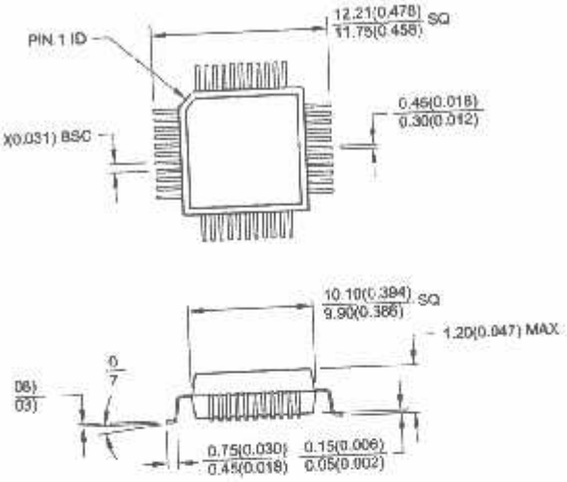
= Preliminary Availability

Package Type
44-lead, Thin Plastic Gull Wing Quad Flatpack (TQFP)
44-lead, Plastic J-leaded Chip Carrier (PLCC)
40-pin, 0.600" Wide, Plastic Dual Inline Package (PDIP)

1

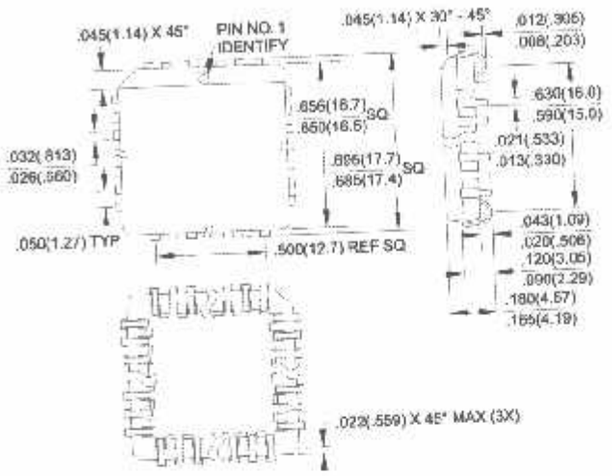
ıging Information

, 44-lead, Thin (1.0 mm) Plastic Gull Wing Quad Package (TQFP)
ensions in Millimeters and (Inches)*

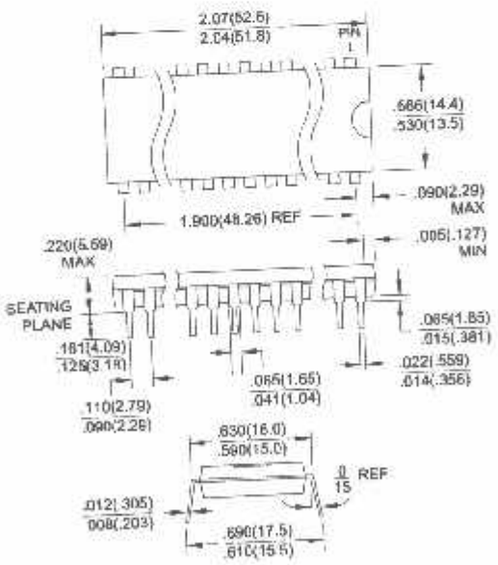


ıtrolling dimension: millimeters

44J, 44-lead, Plastic J-leaded Chip Carrier (PLCC)
Dimensions in Inches and (Millimeters)



ı, 40-pin, 0.600" Wide, Plastic Dual Inline
age (PDIP)
ensions in Inches and (Millimeters)
C STANDARD MS-011 AC



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2487A–10/01/xM

es

- ltage and Standard-Voltage Operation
- (V_{CC} = 4.5V to 5.5V)
- (V_{CC} = 2.7V to 5.5V)
- (V_{CC} = 2.5V to 5.5V)
- (V_{CC} = 1.8V to 5.5V)
- ly Organized 128 x 8 (1K), 256 x 8 (2K), 512 x 8 (4K), (8K) or 2048 x 8 (16K)
- erial Interface
- Trigger, Filtered Inputs for Noise Suppression
- ional Data Transfer Protocol
- (1.8V, 2.5V, 2.7V) and 400 kHz (5V) Compatibility
- otect Pin for Hardware Data Protection
- age (1K, 2K), 16-Byte Page (4K, 8K, 16K) Write Modes
- age Writes Are Allowed
- ed Write Cycle (10 ms max)
- liability
- lurance: 1 Million Write Cycles
- Retention: 100 Years
-) Protection: >3000V
- tive Grade and Extended Temperature Devices Available
- d 14-Pin JEDEC SOIC, 8-Pin PDIP, 8-Pin MSOP, and 8-Pin TSSOP Packages

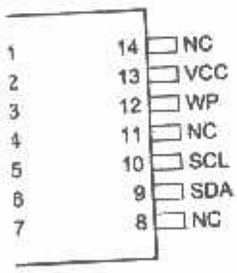
ption

C01A/02/04/08/16 provides 1024/2048/4096/8192/16384 bits of serial elec- asable and programmable read only memory (EEPROM) organized as 12/1024/2048 words of 8 bits each. The device is optimized for use in many and commercial applications where low power and low voltage operation are . The AT24C01A/02/04/08/16 is available in space saving 8-pin PDIP, 01A/02/04/08/16), 8-Pin MSOP (AT24C01A/02), 8-Pin TSSOP 01A/02/04/08/16), and 8-Pin and 14-Pin JEDEC SOIC 1A/02/04/08/16) packages and is accessed via a 2-wire serial interface. In he entire family is available in 5.0V (4.5V to 5.5V), 2.7V (2.7V to 5.5V), 2.5V .5V) and 1.8V (1.8V to 5.5V) versions.

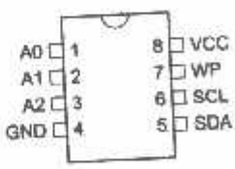
nfigurations

e	Function
	Address Inputs
	Serial Data
	Serial Clock Input
	Write Protect
	No Connect

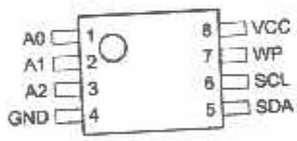
14-Pin SOIC



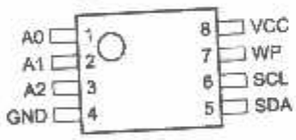
8-Pin PDIP



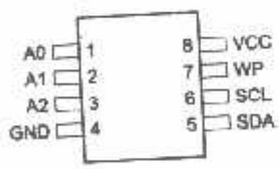
8-Pin TSSOP



8-Pin MSOP



8-Pin SOIC



2-Wire Serial EEPROM

1K (128 x 8)

2K (256 x 8)

4K (512 x 8)

8K (1024 x 8)

16K (2048 x 8)

AT24C01A
AT24C02
AT24C04
AT24C08
AT24C16

1 Kbyte = 1024 bit
= 128 x 8 bit

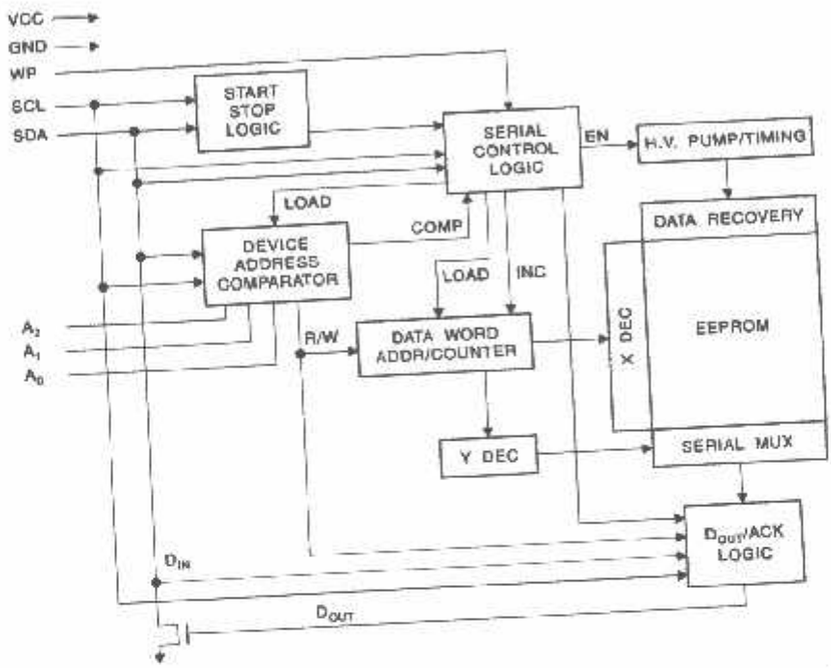
Rev. 0160D–10/98

ute Maximum Ratings

g Temperature	-55°C to +125°C
Temperature	-65°C to +150°C
n Any Pin pect to Ground	-1.0V to +7.0V
n Operating Voltage	6.25V
ut Current	5.0 mA

*NOTICE: Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Diagram



scription

CLOCK (SCL): The SCL input is used to positive k data into each EEPROM device and negative k data out of each device.

DATA (SDA): The SDA pin is bidirectional for a transfer. This pin is open-drain driven and may Red with any number of other open-drain or open devices.

PAGE ADDRESSES (A2, A1, A0): The A2, A1 ins are device address inputs that are hard wired T24C01A and the AT24C02. As many as eight vices may be addressed on a single bus system ddressing is discussed in detail under the Device ng section).

The AT24C04 uses the A2 and A1 inputs for hard wire addressing and a total of four 4K devices may be addressed on a single bus system. The A0 pin is a no connect.

The AT24C08 only uses the A2 input for hardwire addressing and a total of two 8K devices may be addressed on a single bus system. The A0 and A1 pins are no connects.

The AT24C16 does not use the device address pins which limits the number of devices on a single bus to one. The A0, A1 and A2 pins are no connects.

WRITE PROTECT (WP): The AT24C01A/02/04/16 has a Write Protect pin that provides hardware data protection. The Write Protect pin allows normal read/write operations when connected to ground (GND). When the Write Protect pin is connected to V_{CC}, the write protection feature is enabled and operates as shown in the following table.

Part of the Array Protected				
24C01A	24C02	24C04	24C08	24C16
Full (1K) Array	Full (2K) Array	Full (4K) Array	Normal Read/ Write Operation	Upper Half (8K) Array
Normal Read/Write Operations				

ry Organization

1A, 1K SERIAL EEPROM: Internally organized pages of 1-byte each, the 1K requires a 7-bit data ress for random word addressing.

AT24C02, 2K SERIAL EEPROM: Internally organized with 256 pages of 1-byte each, the 2K requires an 8-bit data word address for random word addressing.

AT24C04, 4K SERIAL EEPROM: The 4K is internally organized with 256 pages of 2 bytes each. Random word addressing Chip Number requires a 9-bit data word address.

AT24C08, 8K SERIAL EEPROM: The 8K is internally organized with 4 blocks of 256 pages of 4 bytes each. Random word addressing requires a 10-bit data word address.

AT24C16, 16K SERIAL EEPROM: The 16K is internally organized with 8 blocks of 256 pages of 8 bytes each. Random word addressing requires an 11-bit data word address.

ıpacitance(1)

e over recommended operating range from T_A = 25°C, f = 1.0 MHz, V_{CC} = +1.8V.

Test Condition	Max	Units	Conditions
Input/Output Capacitance (SDA)	8	pF	$V_{I/O}$ = 0V
Input Capacitance (A_0, A_1, A_2, SCL)	6	pF	V_{IN} = 0V

. This parameter is characterized and is not 100% tested.

ıaracteristics

le over recommended operating range from: T_{AI} = -40°C to +85°C, V_{CC} = +1.8V to +5.5V, T_{AC} = 0°C to +70°C, .8V to +5.5V (unless otherwise noted).

Parameter	Test Condition	Min	Typ	Max	Units
Supply Voltage		1.8		5.5	V
Supply Voltage		2.5		5.5	V
Supply Voltage		2.7		5.5	V
Supply Voltage		4.5		5.5	V
Supply Current V_{CC} = 5.0V	READ at 100 kHz		0.4	1.0	mA
Supply Current V_{CC} = 5.0V	WRITE at 100 kHz		2.0	3.0	mA
Standby Current V_{CC} = 1.8V	V_{IN} = V_{CC} or V_{SS}		0.6	3.0	µA
Standby Current V_{CC} = 2.5V	V_{IN} = V_{CC} or V_{SS}		1.4	4.0	µA
Standby Current V_{CC} = 2.7V	V_{IN} = V_{CC} or V_{SS}		1.6	4.0	µA
Standby Current V_{CC} = 5.0V	V_{IN} = V_{CC} or V_{SS}		8.0	18.0	µA
Input Leakage Current	V_{IN} = V_{CC} or V_{SS}		0.10	3.0	µA
Output Leakage Current	V_{OUT} = V_{CC} or V_{SS}		0.05	3.0	µA
Input Low Level(1)		-0.6		V_{CC} x 0.3	V
Input High Level(1)		V_{CC} x 0.7		V_{CC} + 0.5	V
Output Low Level V_{CC} = 3.0V	I_{OL} = 2.1 mA			0.4	V
Output Low Level V_{CC} = 1.8V	I_{OL} = 0.15 mA			0.2	V

. V_{IL} min and V_{IH} max are reference only and are not tested.

ıaracteristics

le over recommended operating range from T_A = -40°C to +85°C, V_{CC} = +1.8V to +5.5V, CL = 1 TTL Gate and nless otherwise noted).

	Parameter	2.7-, 2.5-, 1.8-volt		5.0-volt		Units
		Min	Max	Min	Max	
	Clock Frequency, SCL		100		400	kHz
	Clock Pulse Width Low	4.7		1.2		µs
	Clock Pulse Width High	4.0		0.6		µs
	Noise Suppression Time[1]		100		50	ns
	Clock Low to Data Out Valid	0.1	4.5	0.1	0.9	µs
	Time the bus must be free before a new transmission can start[1]	4.7		1.2		µs
	Start Hold Time	4.0		0.6		µs
	Start Set-up Time	4.7		0.6		µs
	Data In Hold Time	0		0		µs
	Data In Set-up Time	200		100		ns
	Inputs Rise Time[1]		1.0		0.3	µs
	Inputs Fall Time[1]		300		300	ns
	Stop Set-up Time	4.7		0.6		µs
	Data Out Hold Time	100		50		ns
	Write Cycle Time		10		10	ms
g[1]	5.0V, 25°C, Page Mode	1M		1M		Write Cycles

This parameter is characterized and is not 100% tested.

Operation

nd DATA TRANSITIONS: The SDA pin is nor- d high with an external device. Data on the SDA ıange only during SCL low time periods (refer to ity timing diagram). Data changes during SCL ds will indicate a start or stop condition as ow.

INDITION: A high-to-low transition of SDA with a start condition which must precede any other (refer to Start and Stop Definition timing dia-

IDITION: A low-to-high transition of SDA with s a stop condition. After a read sequence, the and will place the EEPROM in a standby power to Start and Stop Definition timing diagram).

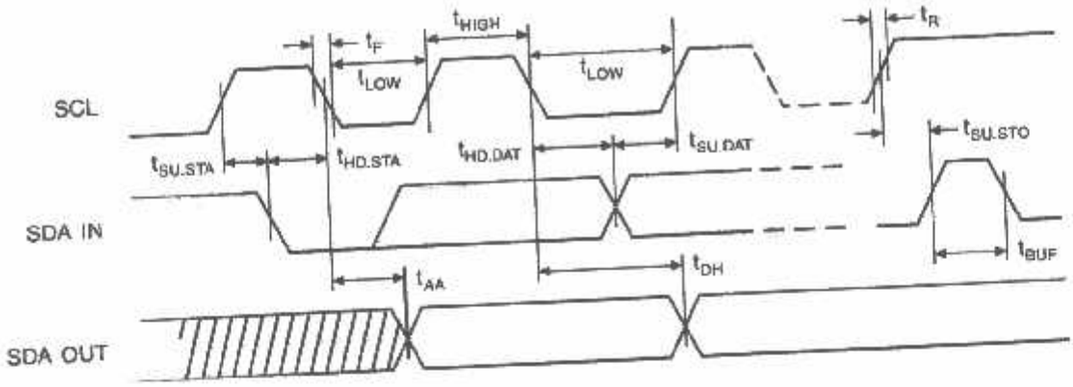
ACKNOWLEDGE: All addresses and data words are serially transmitted to and from the EEPROM in 8-bit words. The EEPROM sends a zero to acknowledge that it has received each word. This happens during the ninth clock cycle.

STANDBY MODE: The AT24C01A/02/04/08/16 features a low power standby mode which is enabled: (a) upon power-up and (b) after the receipt of the STOP bit and the completion of any internal operations.

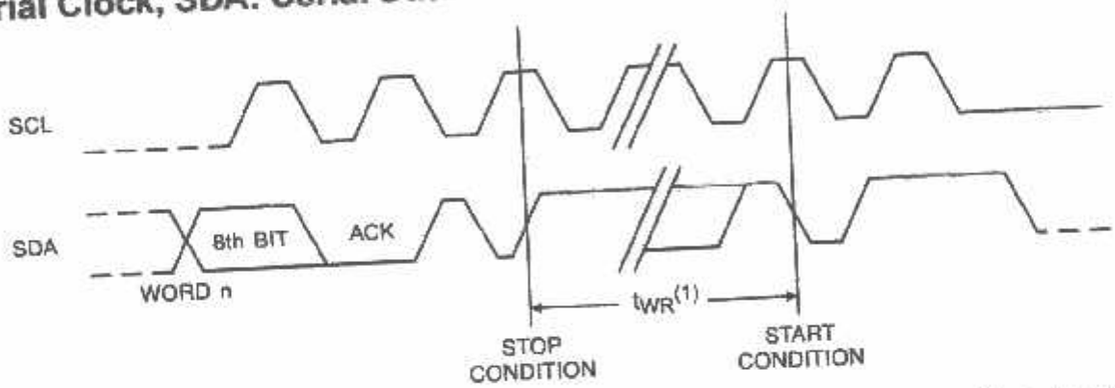
MEMORY RESET: After an interruption in protocol, power loss or system reset, any 2-wire part can be reset by following these steps:

1. Clock up to 9 cycles.
2. Look for SDA high in each cycle while SCL is high.
3. Create a start condition as SDA is high.

iming
Serial Clock, SDA: Serial Data I/O

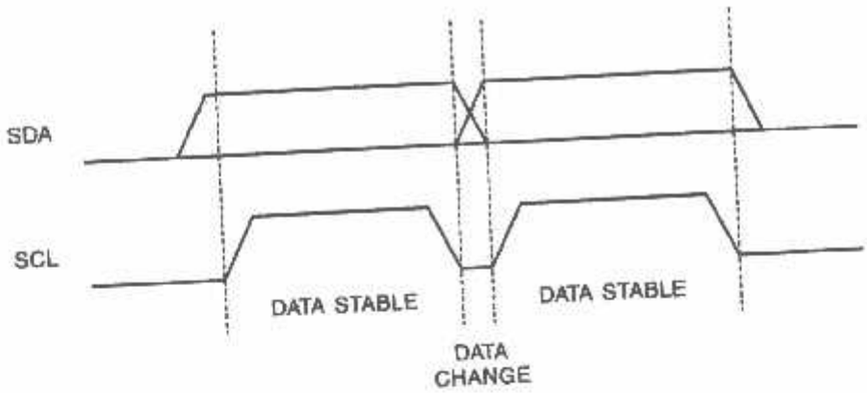


Cycle Timing
Serial Clock, SDA: Serial Data I/O

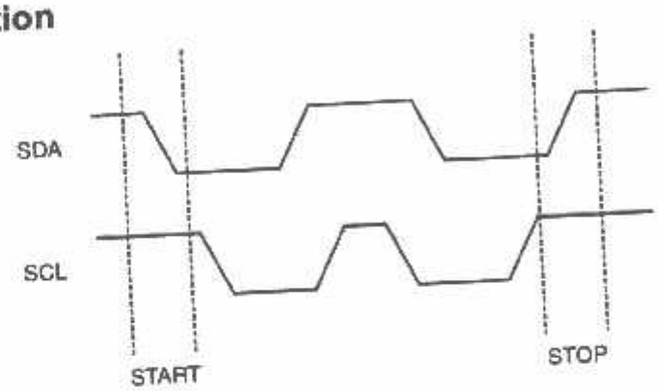


The write cycle time t_{WR} is the time from a valid stop condition of a write sequence to the end of the internal clear/write cycle.

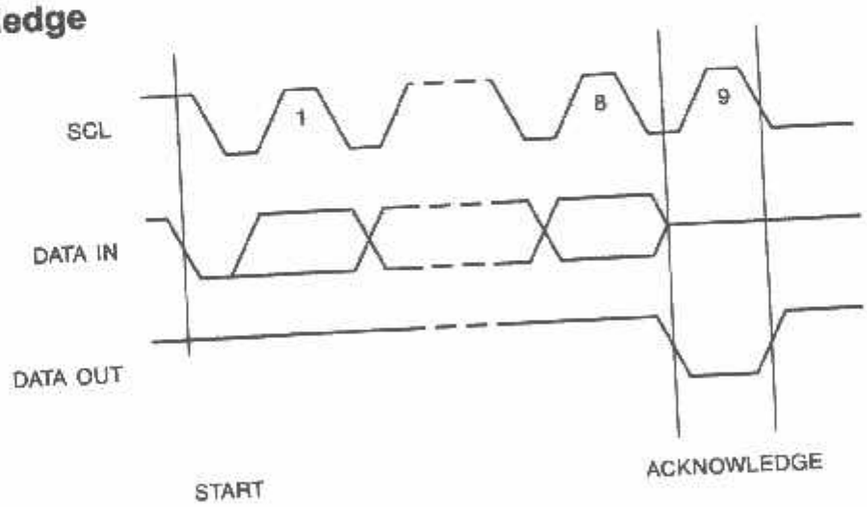
/alidity



ınd Stop Definition



t Acknowledge



e Addressing

2K, 4K, 8K and 16K EEPROM devices all require device address word following a start condition to ie chip for a read or write operation (refer to Figure

ice address word consists of a mandatory one, juence for the first four most significant bits as his is common to all the EEPROM devices.

3 bits are the A2, A1 and A0 device address bits K/2K EEPROM. These 3 bits must compare to esponding hard-wired input pins.

EPROM only uses the A2 and A1 device address he third bit being a memory page address bit. The e address bits must compare to their correspond- wired input pins. The A0 pin is no connect.

EPROM only uses the A2 device address bit with 2 bits being for memory page addressing. The A2 ompare to its corresponding hard-wired input pin. nd A0 pins are no connect.

does not use any device address bits but instead s are used for memory page addressing. These dressing bits on the 4K, 8K, and 16K devices e considered the most significant bits of the data ress which follows. The A0, A1 and A2 pins are no

h bit of the device address is the read/write opera- t bit. A read operation is initiated if this bit is high te operation is initiated if this bit is low.

ompare of the device address, the EEPROM will zero. If a compare is not made, the chip will return dby state.

Operations

RITE: A write operation requires an 8-bit data dress following the device address word and edgment. Upon receipt of this address, the will again respond with a zero and then clock in -bit data word. Following receipt of the 8-bit data EEPROM will output a zero and the addressing ch as a microcontroller, must terminate the write with a stop condition. At this time the EEPROM internally-timed write cycle, t_{WR}, to the nonvolatile All inputs are disabled during this write cycle and ROM will not respond until the write is complete Figure 2).

RITE: The 1K/2K EEPROM is capable of an 8- write, and the 4K, 8K and 16K devices are capa- byte page writes.

rite is initiated the same as a byte write, but the troller does not send a stop condition after the first rd is clocked in. Instead, after the EEPROM acknowledges receipt of the first data word, the microcontroller can transmit up to seven (1K/2K) or fifteen (4K, 8K, 16K) more data words. The EEPROM will respond with a zero after each data word received. The microcontroller must terminate the page write sequence with a stop condition (refer to Figure 3).

The data word address lower three (1K/2K) or four (4K, 8K, 16K) bits are internally incremented following the receipt of each data word. The higher data word address bits are not incremented, retaining the memory page row location. When the word address, internally generated, reaches the page boundary, the following byte is placed at the beginning of the same page. If more than eight (1K/2K) or sixteen (4K, 8K, 16K) data words are transmitted to the EEPROM, the data word address will "roll over" and previous data will be overwritten.

ACKNOWLEDGE POLLING: Once the internally-timed write cycle has started and the EEPROM inputs are disabled, acknowledge polling can be initiated. This involves sending a start condition followed by the device address word. The read/write bit is representative of the operation desired. Only if the internal write cycle has completed will the EEPROM respond with a zero allowing the read or write sequence to continue.

Read Operations

Read operations are initiated the same way as write operations with the exception that the read/write select bit in the device address word is set to one. There are three read operations: current address read, random address read and sequential read.

CURRENT ADDRESS READ: The internal data word address counter maintains the last address accessed during the last read or write operation, incremented by one. This address stays valid between operations as long as the chip power is maintained. The address "roll over" during read is from the last byte of the last memory page to the first byte of the first page. The address "roll over" during write is from the last byte of the current page to the first byte of the same page.

Once the device address with the read/write select bit set to one is clocked in and acknowledged by the EEPROM, the current address data word is serially clocked out. The microcontroller does not respond with an input zero but does generate a following stop condition (refer to Figure 4).

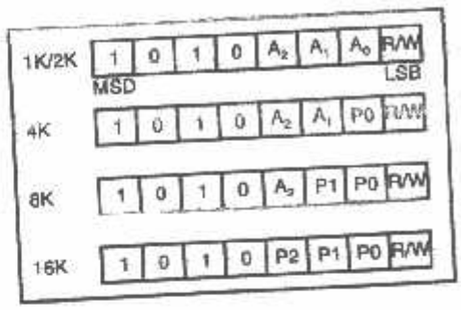
RANDOM READ: A random read requires a "dummy" byte write sequence to load in the data word address. Once the device address word and data word address are clocked in and acknowledged by the EEPROM, the microcontroller must generate another start condition. The microcontroller now initiates a current address read by sending a device address with the read/write select bit high. The EEPROM acknowledges the device address and serially clocks out

word. The microcontroller does not respond with a does generate a following stop condition (refer to

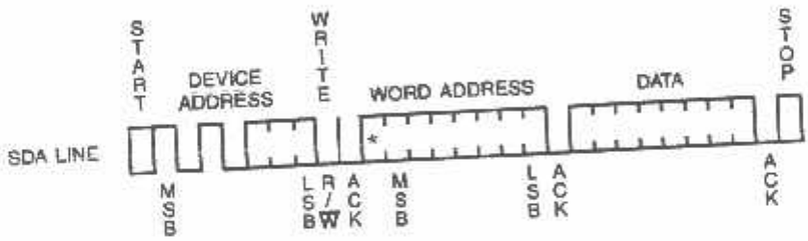
.

NTIAL READ: Sequential reads are initiated by current address read or a random address read. microcontroller receives a data word, it responds cknowledge. As long as the EEPROM receives an acknowledge, it will continue to increment the data word address and serially clock out sequential data words. When the memory address limit is reached, the data word address will "roll over" and the sequential read will continue. The sequential read operation is terminated when the microcontroller does not respond with a zero but does generate a following stop condition (refer to Figure 6).

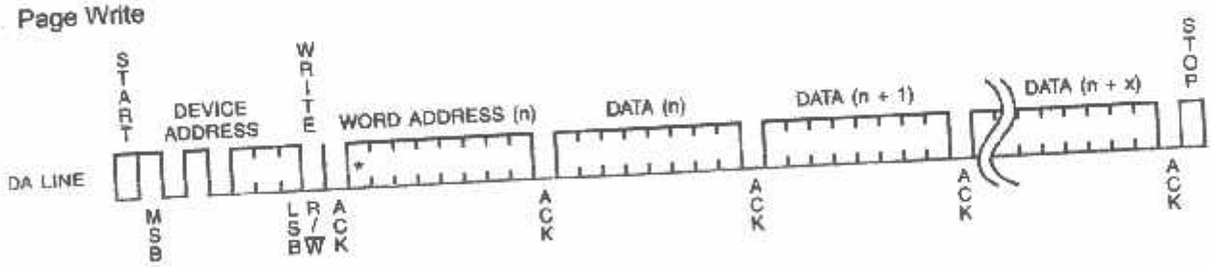
. Device Address



Byte Write

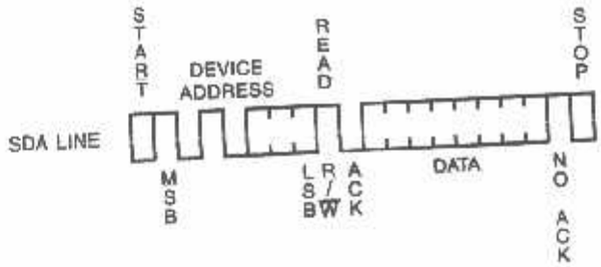


Page Write

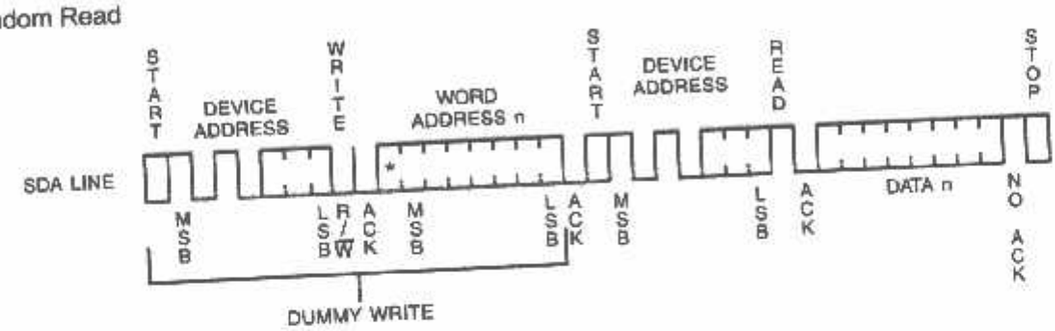


(* = DON'T CARE bit for 1K)

. Current Address Read

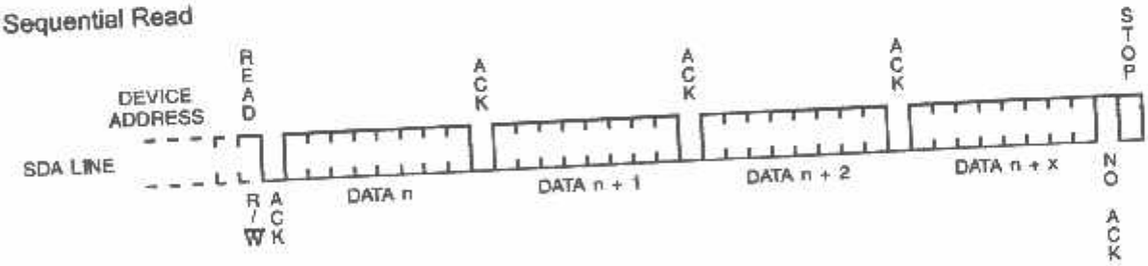


Random Read



(* = DON'T CARE bit for 1K)

Sequential Read



:01A Ordering Information

ix)	I_{CC} (max) (µA)	I_{SB} (max) (µA)	f_{MAX} (kHz)	Ordering Code	Package	Operation Range
	3000	18	400	AT24C01A-10PC AT24C01A-10SC AT24C01A-10MC AT24C01A-10TC	8P3 8S1 8M 8T	Commercial (0°C to 70°C)
	3000	18	400	AT24C01A-10PI AT24C01A-10SI AT24C01A-10MI AT24C01A-10TI	8P3 8S1 8M 8T	Industrial (-40°C to 85°C)
	1500	4	100	AT24C01A-10PC-2.7 AT24C01A-10SC-2.7 AT24C01A-10MC-2.7 AT24C01A-10TC-2.7	8P3 8S1 8M 8T	Commercial (0°C to 70°C)
	1500	4	100	AT24C01A-10PI-2.7 AT24C01A-10SI-2.7 AT24C01A-10MI-2.7 AT24C01A-10TI-2.7	8P3 8S1 8M 8T	Industrial (-40°C to 85°C)

	Package Type
	8-Lead, 0.118" Wide, Miniature Small Outline Package (MSOP)
	8-Lead, 0.300" Wide, Plastic Dual Inline Package (PDIP)
	8-Lead, 0.150" Wide, Plastic Gull Wing Small Outline (JEDEC SOIC)
	8-Lead, 0.170" Wide, Thin Shrink Small Outline Package (TSSOP)
	Options
	Standard Operation (4.5V to 5.5V)
	Low Voltage (2.7V to 5.5V)
	Low Voltage (2.5V to 5.5V)
	Low Voltage (1.8V to 5.5V)

:01A Ordering Information (Continued)

x)	I_{CC} (max) (µA)	I_{SB} (max) (µA)	f_{MAX} (kHz)	Ordering Code	Package	Operation Range
	1000	4	100	AT24C01A-10PC-2.5 AT24C01A-10SC-2.5 AT24C01A-10MC-2.5 AT24C01A-10TC-2.5	8P3 8S1 8M 8T	Commercial (0°C to 70°C)
	1000	4	100	AT24C01A-10PI-2.5 AT24C01A-10SI-2.5 AT24C01A-10MI-2.5 AT24C01A-10TI-2.5	8P3 8S1 8M 8T	Industrial (-40°C to 85°C)
	800	3	100	AT24C01A-10PC-1.8 AT24C01A-10SC-1.8 AT24C01A-10MC-1.8 AT24C01A-10TC-1.8	8P3 8S1 8M 8T	Commercial (0°C to 70°C)
	800	3	100	AT24C01A-10PI-1.8 AT24C01A-10SI-1.8 AT24C01A-10MI-1.8 AT24C01A-10TI-1.8	8P3 8S1 8M 8T	Industrial (-40°C to 85°C)

	Package Type
	8-Lead, 0.118" Wide, Miniature Small Outline Package (MSOP)
	8-Lead, 0.300" Wide, Plastic Dual Inline Package (PDIP)
	8-Lead, 0.150" Wide, Plastic Gull Wing Small Outline (JEDEC SOIC)
	8-Lead, 0.170" Wide, Thin Shrink Small Outline Package (TSSOP)
	Options
	Standard Operation (4.5V to 5.5V)
	Low Voltage (2.7V to 5.5V)
	Low Voltage (2.5V to 5.5V)
	Low Voltage (1.8V to 5.5V)

FAIRCHILD SEMICONDUCTOR IV

October 1987
Revised January 1999

MM74C922 • MM74C923
16-Key Encoder • 20-Key Encoder

General Description

The MM74C922 and MM74C923 CMOS key encoders provide all the necessary logic to fully encode an array of SPST switches. The keyboard scan can be implemented by either an external clock or external capacitor. These encoders also have on-chip pull-up devices which permit switches with up to 50 kΩ on resistance to be used. No diodes in the switch array are needed to eliminate ghost switches. The internal debounce circuit needs only a single external capacitor and can be defeated by omitting the capacitor. A Data Available output goes to a high level when a valid keyboard entry has been made. The Data Available output returns to a low level when the entered key is released, even if another key is depressed. The Data Available will return high to indicate acceptance of the new key after a normal debounce period; this two-key roll-over is provided between any two switches.

An internal register remembers the last key pressed even after the key is released. The 3-STATE outputs provide for easy expansion and bus operation and are LPTTL compatible.

Features

- 50 kΩ maximum switch on resistance
- On or off chip clock
- On-chip row pull-up devices
- 2 key roll-over
- Keybounce elimination with single capacitor
- Last key register at outputs
- 3-STATE output LPTTL compatible
- Wide supply range: 3V to 15V
- Low power consumption

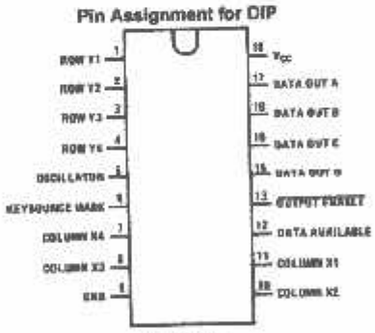
Ordering Code:

Order Number	Package Number	Package Description
MM74C922N	N18A	18-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300" Wide
MM74C922WM	M20B	20-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-013, 0.300" Wide
MM74C923WM	M20B	20-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-013, 0.300" Wide
MM74C923N	N20A	20-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300" Wide

Device also available in Tape and Reel. Specify by appending suffix letter "X" to the ordering code.

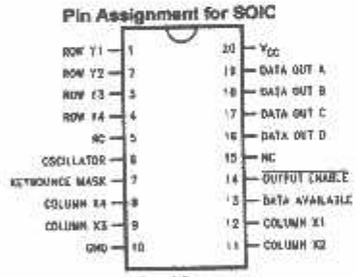
Connection Diagrams

Pin Assignment for DIP



Top View
MM74C922

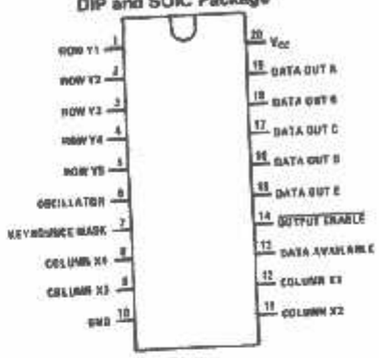
Pin Assignment for SOIC



Top View
MM74C922

Connection Diagrams (Continued)

Pin Assignment for DIP and SOIC Package



Top View
MM74C923

Truth Tables

(Pins 0 through 11)

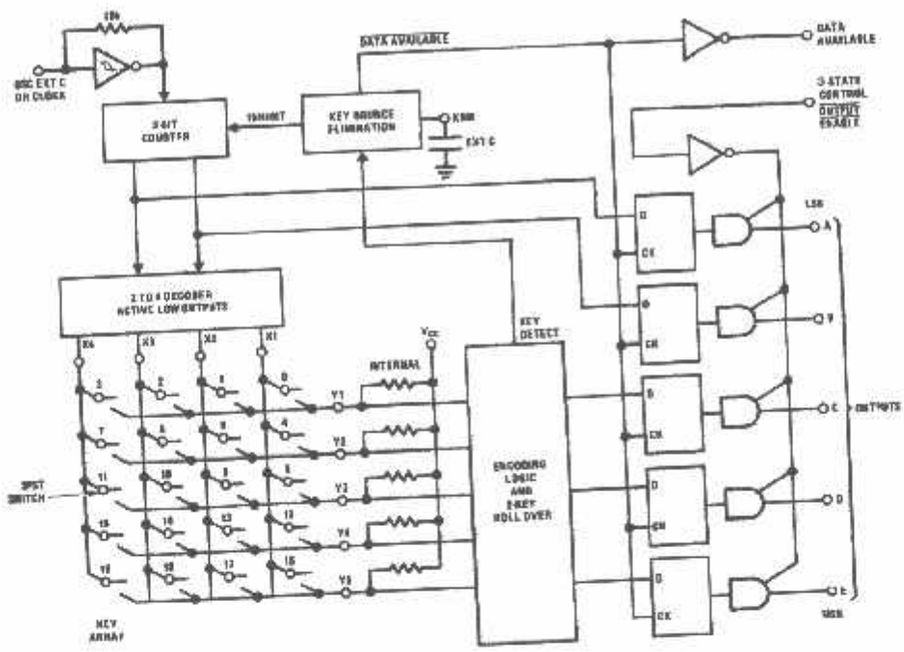
Switch Position	0 Y1,X1	1 Y1,X2	2 Y1,X3	3 Y1,X4	4 Y2,X1	5 Y2,X2	6 Y2,X3	7 Y2,X4	8 Y3,X1	9 Y3,X2	10 Y3,X3	11 Y3,X4
DATA A	0	1	0	1	0	1	0	1	0	1	0	1
DATA B	0	0	1	1	0	0	1	1	0	0	1	1
DATA C	0	0	0	0	1	1	1	1	0	0	0	0
DATA D	0	0	0	0	0	0	0	0	1	1	1	1
DATA E (Note 1)	0	0	0	0	0	0	0	0	0	0	0	0

(Pins 12 through 19)

Switch Position	12 Y4,X1	13 Y4,X2	14 Y4,X3	15 Y4,X4	16 Y5(Note 1), X1	17 Y5 (Note 1), X2	18 Y5 (Note 1), X3	19 Y5 (Note 1), X4
DATA A	0	1	0	1	0	1	0	1
DATA B	0	0	1	1	0	0	1	1
DATA C	1	1	1	1	0	0	0	0
DATA D	1	1	1	1	0	0	0	0
DATA E (Note 1)	0	0	0	0	1	1	1	1

Note 1: Omit for MM74C922

Block Diagram



Absolute Maximum Ratings (Note 2)

Voltage at Any Pin	V_{CC} − 0.3V to V_{CC} + 0.3V
Operating Temperature Range	
MM74C922, MM74C923	−40°C to +85°C
Storage Temperature Range	−65°C to +150°C
Power Dissipation (P_D)	
Dual-In-Line	700 mW
Small Outline	500 mW
Operating V_{CC} Range	3V to 15V
V_{CC}	18V
Lead Temperature	
(Soldering, 10 seconds)	260°C

Note 2: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Temperature Range" they are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

DC Electrical Characteristics

Min/Max limits apply across temperature range unless otherwise specified

Symbol	Parameter	Conditions	Min	Typ	Max	Units
CMOS TO CMOS						
V_{T+}	Positive-Going Threshold Voltage at Osc and KBM Inputs	V_{CC} = 5V, $I_{IN} \geq 0.7$ mA	3.0	3.8	4.3	V
		V_{CC} = 10V, $I_{IN} \geq 1.4$ mA	6.0	8.8	8.6	V
		V_{CC} = 15V, $I_{IN} \geq 2.1$ mA	9.0	10	12.9	V
V_{T-}	Negative-Going Threshold Voltage at Osc and KBM Inputs	V_{CC} = 5V, $I_{IN} \geq 0.7$ mA	0.7	1.4	2.0	V
		V_{CC} = 10V, $I_{IN} \geq 1.4$ mA	1.4	3.2	4.0	V
		V_{CC} = 15V, $I_{IN} \geq 2.1$ mA	2.1	5	6.0	V
$V_{IN(1)}$	Logical "1" Input Voltage, Except Osc and KBM Inputs	V_{CC} = 5V	3.5	4.5		V
		V_{CC} = 10V	8.0	9		V
		V_{CC} = 15V	12.5	13.5		V
$V_{IN(0)}$	Logical "0" Input Voltage, Except Osc and KBM Inputs	V_{CC} = 5V		0.5	1.5	V
		V_{CC} = 10V		1	2	V
		V_{CC} = 15V		1.5	2.5	V
I_{IR}	Row Pull-Up Current at Y1, Y2, Y3, Y4 and Y5 Inputs	V_{CC} = 5V, V_{IN} = 0.1 V_{CC}		−2	−5	μA
		V_{CC} = 10V		10	−20	μA
		V_{CC} = 15V		−22	−45	μA
$V_{OUT(1)}$	Logical "1" Output Voltage	V_{CC} = 5V, I_O = −10 μA	4.5			V
		V_{CC} = 10V, I_O = −10 μA	9			V
		V_{CC} = 15V, I_O = −10 μA	13.5			V
$V_{OUT(0)}$	Logical "0" Output Voltage	V_{CC} = 5V, I_O = 10 μA			0.5	V
		V_{CC} = 10V, I_O = 10 μA			1	V
		V_{CC} = 15V, I_O = 10 μA			1.5	V
R_{on}	Column "ON" Resistance at X1, X2, X3 and X4 Outputs	V_{CC} = 5V, V_O = 0.5V		500	1400	Ω
		V_{CC} = 10V, V_O = 1V		300	700	Ω
		V_{CC} = 15V, V_O = 1.5V		200	500	Ω
I_{CC}	Supply Current Osc at 0V, (one Y low)	V_{CC} = 5V		0.55	1.1	mA
		V_{CC} = 10V		1.1	1.9	mA
		V_{CC} = 15V		1.7	2.8	mA
$I_{IN(1)}$	Logical "1" Input Current at Output Enable	V_{CC} = 15V, V_{IN} = 15V		0.005	1.0	μA
$I_{IN(0)}$	Logical "0" Input Current at Output Enable	V_{CC} = 15V, V_{IN} = 0V	−1.0	−0.005		μA
CMOS/LPTTL INTERFACE						
$V_{IN(1)}$	Except Osc and KBM Inputs	V_{CC} = 4.75V	V_{CC} − 1.5			V
$V_{IN(0)}$	Except Osc and KBM Inputs	V_{CC} = 4.75V			0.8	V
$V_{OUT(1)}$	Logical "1" Output Voltage	I_O = −360 μA, V_{CC} = 4.75V	2.4			V
		I_O = −360 μA				
$V_{OUT(0)}$	Logical "0" Output Voltage	I_O = −360 μA, V_{CC} = 4.75V			0.4	V
		I_O = −360 μA				

DC Electrical Characteristics (Continued)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
OUTPUT DRIVE (See Family Characteristics Data Sheet) (Short Circuit Current)						
I_{SOURCE}	Output Source Current (P-Channel)	V_{CC} = 5V, V_{OUT} = 0V, T_A = 25°C	−1.75	−3.3		mA
I_{SOURCE}	Output Source Current (P-Channel)	V_{CC} = 10V, V_{OUT} = 0V, T_A = 25°C	−8	−15		mA
I_{SINK}	Output Sink Current (N-Channel)	V_{CC} = 5V, V_{OUT} = V_{CC}, T_A = 25°C	1.75	3.6		mA
I_{SINK}	Output Sink Current (N-Channel)	V_{CC} = 10V, V_{OUT} = V_{CC}, T_A = 25°C	8	16		mA

AC Electrical Characteristics (Note 3)

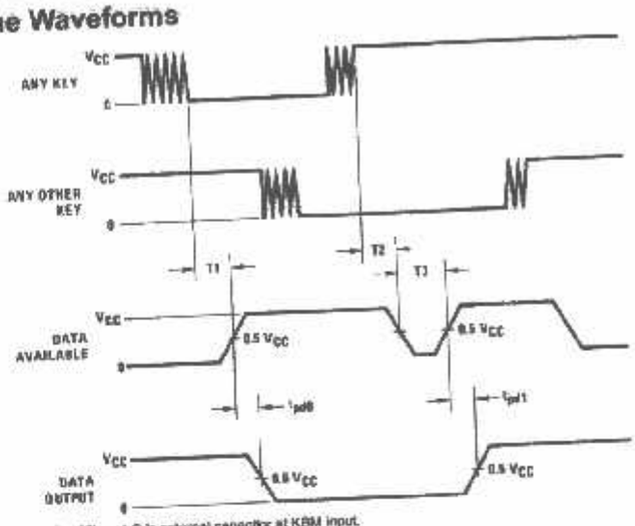
T_A = 25°C, C_L = 50 pF, unless otherwise noted

Symbol	Parameter	Conditions	Min	Typ	Max	Units
t_{PDO}, t_{PDH}	Propagation Delay Time to Logical "0" or Logical "1" from D,A	C_L = 50 pF (Figure 1) V_{CC} = 5V V_{CC} = 10V V_{CC} = 15V		60 35 25	150 80 60	ns ns ns
t_{HH}, t_{HH}	Propagation Delay Time from Logical "0" or Logical "1" into High Impedance State	R_L = 10k, C_L = 10 pF (Figure 2) V_{CC} = 5V, R_L = 10k V_{CC} = 10V, C_L = 10 pF V_{CC} = 15V		80 65 50	200 150 110	ns ns ns
t_{HD}, t_{HI}	Propagation Delay Time from High Impedance State to a Logical "0" or Logical "1"	R_L = 10k, C_L = 50 pF (Figure 2) V_{CC} = 5V, R_L = 10k V_{CC} = 10V, C_L = 50 pF V_{CC} = 15V		100 55 40	250 125 90	ns ns ns
C_{IN}	Input Capacitance	Any Input (Note 4)		5	7.5	pF
C_{OUT}	3-STATE Output Capacitance	Any Output (Note 4)		10		pF

Note 3: AC Parameters are guaranteed by DC correlated testing.

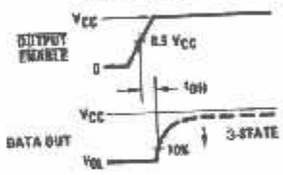
Note 4: Capacitance is guaranteed by periodic testing.

Switching Time Waveforms



T1 = T2 = RC, T3 = 0.7 RC, where R = 10K and C is external capacitor at KBM input.

FIGURE 1.



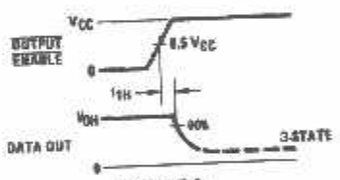
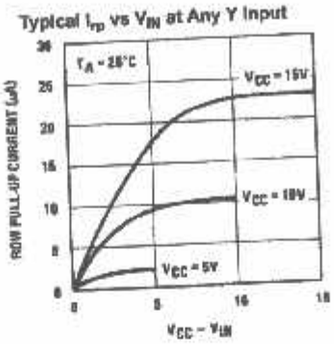


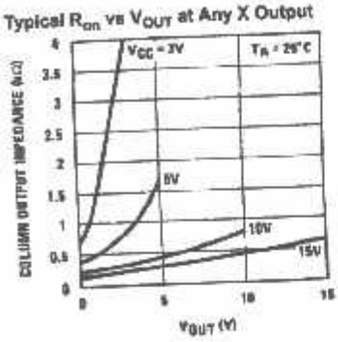
FIGURE 2.

Typical Performance Characteristics

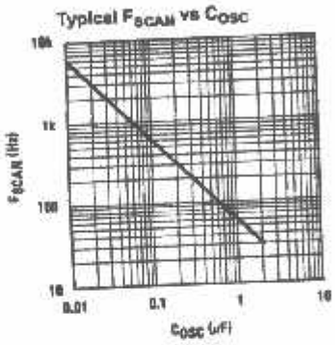
Typical I_{rp} vs V_{IN} at Any Y Input



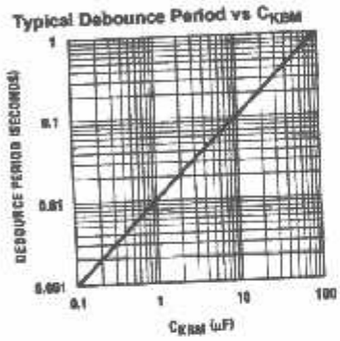
Typical R_{on} vs V_{OUT} at Any X Output



Typical F_{SCAN} vs C_{OSC}

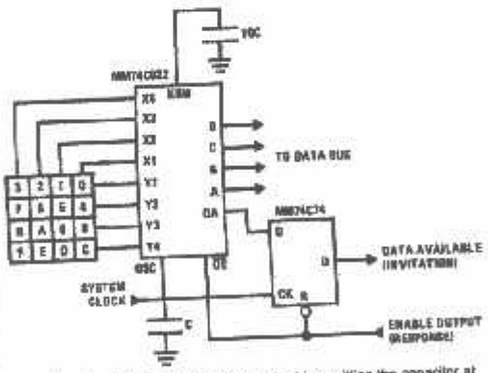


Typical Debounce Period vs C_{KBM}



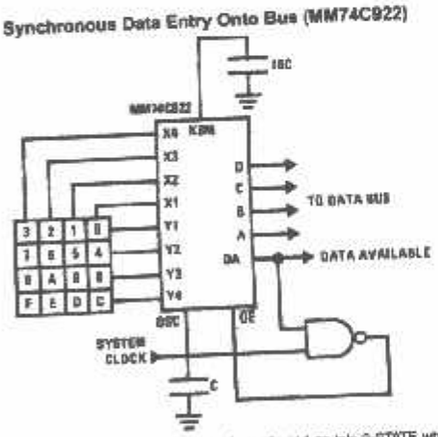
Typical Applications

Synchronous Handshake (MM74C922)



The keyboard may be synchronously scanned by omitting the capacitor at osc. and driving osc. directly if the system clock rate is lower than 10 kHz.

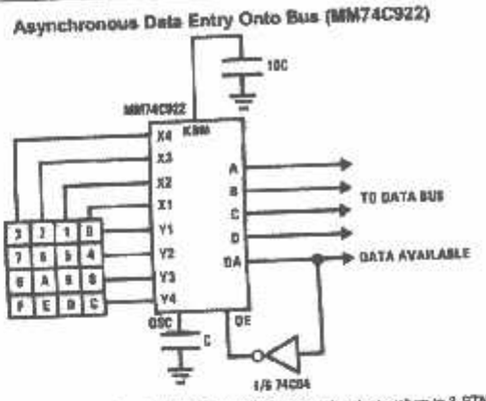
Synchronous Data Entry Onto Bus (MM74C922)



Outputs are enabled when valid entry is made and go into 3-STATE when key is released.

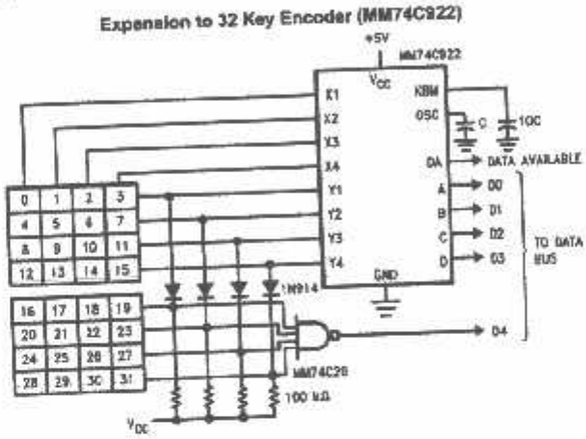
The keyboard may be synchronously scanned by omitting the capacitor at osc. and driving osc. directly if the system clock rate is lower than 10 kHz.

Asynchronous Data Entry Onto Bus (MM74C922)



Outputs are in 3-STATE until key is pressed, then data is placed on bus. When key is released, outputs return to 3-STATE.

Expansion to 32 Key Encoder (MM74C922)



Theory of Operation

The MM74C922/MM74C923 Keyboard Encoders implement all the logic necessary to interface a 16 or 20 SPST key switch matrix to a digital system. The encoder will convert a key switch closer to a 4(MM74C922) or 5(MM74C923) bit nibble. The designer can control both the keyboard scan rate and the key debounce period by altering the oscillator capacitor, C_{OSE}, and the key bounce mask capacitor, C_{MSK}. Thus, the MM74C922/MM74C923's performance can be optimized for many keyboards.

The keyboard encoders connect to a switch matrix that is 4 rows by 4 columns (MM74C922) or 5 rows by 4 columns (MM74C923). When no keys are depressed, the row inputs are pulled high by internal pull-ups and the column outputs sequentially output a logic "0". These outputs are open drain and are therefore low for 25% of the time and otherwise off. The column scan rate is controlled by the oscillator input, which consists of a Schmitt trigger oscillator, a 2-bit counter, and a 2–4-bit decoder.

When a key is depressed, key 0, for example, nothing will happen when the X1 input is off, since Y1 will remain high. When the X1 column is scanned, X1 goes low and Y1 will go low. This disables the counter and keeps X1 low. Y1 going low also initiates the key bounce circuit timing and locks out the other Y inputs. The key code to be output is a combination of the frozen counter value and the decoded Y inputs. Once the key bounce circuit times out, the data is latched, and the Data Available (DAV) output goes high.

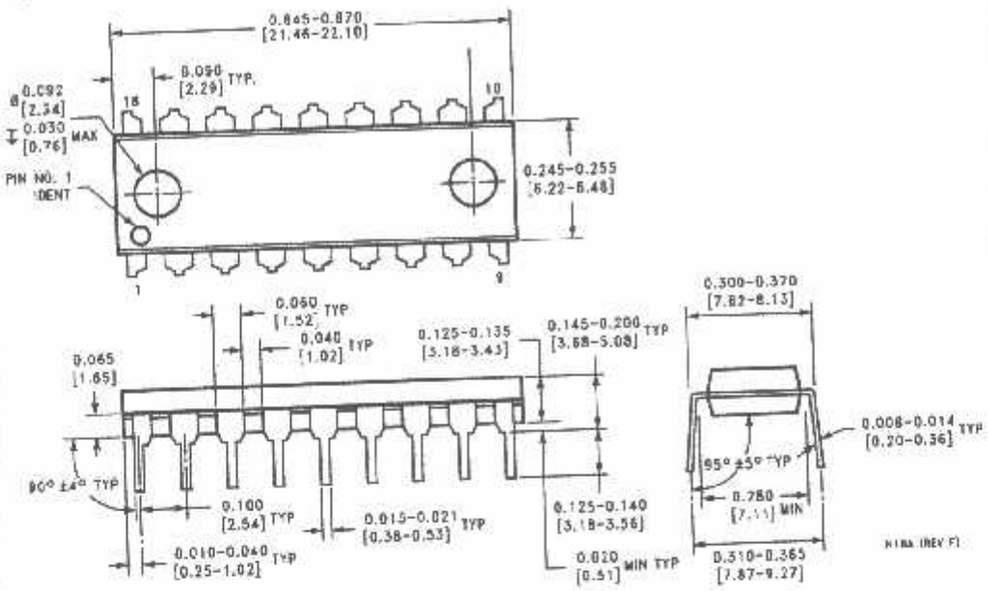
If, during the key closure the switch bounces, Y1 input will go high again, restarting the scan and resetting the key bounce circuitry. The key may bounce several times, but as soon as the switch stays low for a debounce period, the closure is assumed valid and the data is latched.

A key may also bounce when it is released. To ensure that the encoder does not recognize this bounce as another key closure, the debounce circuit must time out before another closure is recognized.

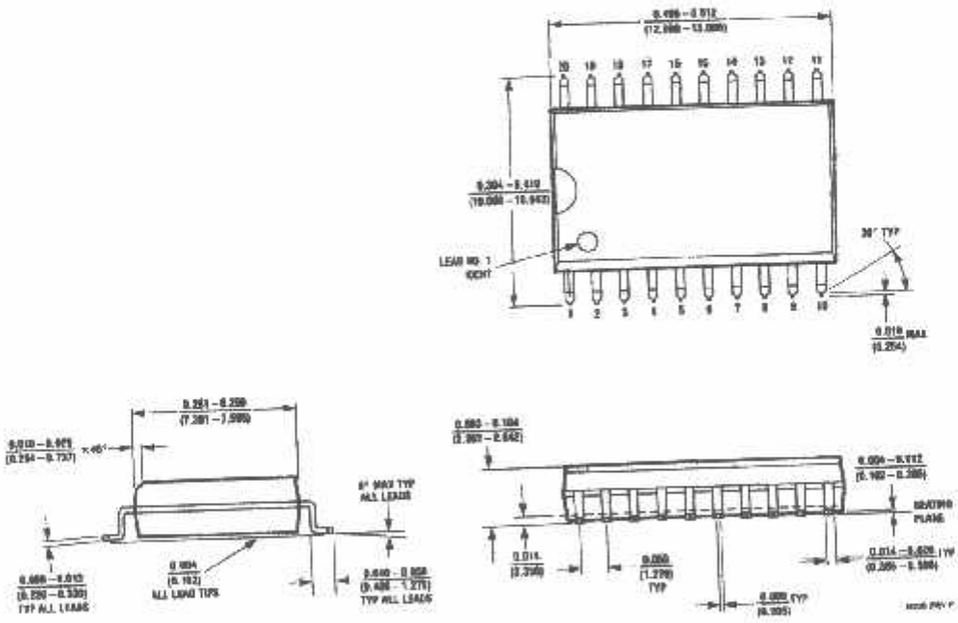
The two-key roll-over feature can be illustrated by assuming a key is depressed, and then a second key is depressed. Since all scanning has stopped, and all other Y inputs are disabled, the second key is not recognized until the first key is lifted and the key bounce circuitry has reset.

The output latches feed 3-STATE, which is enabled when the Output Enable ($\overline{OE}$) input is taken low.

Physical Dimensions inches (millimeters) unless otherwise noted

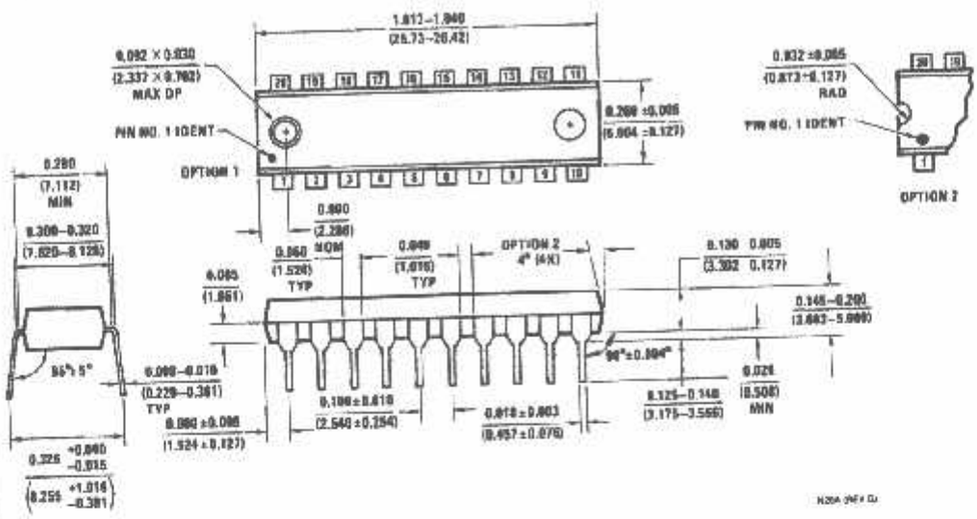


16-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300" Wide
Package Number N16A



20-Lead Plastic Small Outline I.C. Package (M)
Package Number M20B

Physical Dimensions inches (millimeters) unless otherwise noted (Continued)



20-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300" Wide
Package Number N20A

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AIRCHILD
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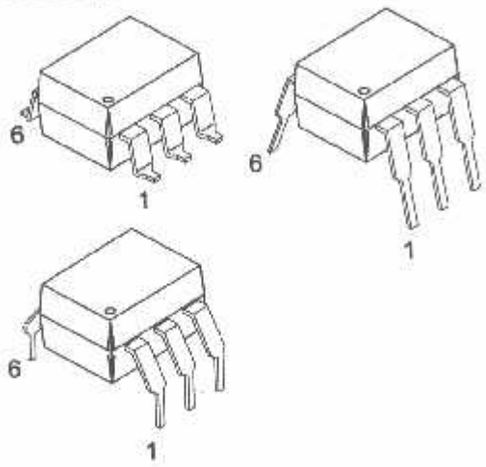
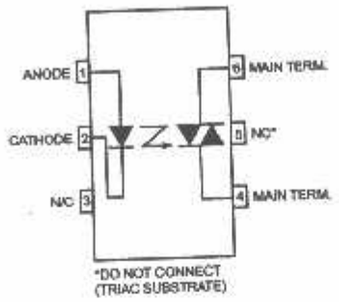
6-PIN DIP RANDOM-PHASE OPTOISOLATORS TRIAC DRIVER OUTPUT (250/400 VOLT PEAK)

3010M MOC3011M MOC3012M MOC3020M MOC3021M MOC3022M MOC3023M

PACKAGE



SCHEMATIC



:RIPTION

)C301XM and MOC302XM series are optically isolated triac driver devices. These devices contain a GaAs infrared ' diode and a light activated silicon bilateral switch, which functions like a triac. They are designed for interfacing between ilic controls and power triacs to control resistive and inductive loads for 115 VAC operations.

URES

llent I_{FT} stability—IR emitting diode has low degradation
isolation voltage—minimum 5300 VAC RMS
)rwriters Laboratory (UL) recognized—File #E90700
: blocking voltage
0V-MOC301XM
0V-MOC302XM
recognized (File #94766)
dering option V (e.g. MOC3023VM)

.ICATIONS

strial controls
c lights
ling machines
state relay
) ballasts

- Solenoid/valve controls
- Static AC power switch
- Incandescent lamp dimmers
- Motor control

OLUTE MAXIMUM RATINGS (T_A = 25°C unless otherwise noted)

ieters	Symbol	Device	Value	Units
L DEVICE				
je Temperature	T_{STG}	All	-40 to +150	°C
ting Temperature	T_{OPR}	All	-40 to +85	°C
Solder Temperature	T_{SOL}	All	260 for 10 sec	°C
on Temperature Range	T_J	All	-40 to +100	°C
on Surge Voltage[1] AC voltage, 60Hz, 1 sec duration)	V_{ISO}	All	7500	Vac(pk)
Device Power Dissipation @ 25°C	P_D	All	330	mW
above 25°C			4.4	mW/°C
ER				
uous Forward Current	I_F	All	60	mA
se Voltage	V_R	All	3	V
Power Dissipation 25°C Ambient	P_D	All	100	mW
above 25°C			1.33	mW/°C
CTOR				
ate Output Terminal Voltage	V_{DRM}	MOC3010M/1M/2M MOC3020M/1M/2M/3M	250 400	V
Repetitive Surge Current (PW = 1 ms, 120 pps)	I_{TSM}	All	1	A
Power Dissipation @ 25°C Ambient	P_D	All	300	mW
above 25°C			4	mW/°C

tion surge voltage, V_{ISO}, is an internal device dielectric breakdown rating. For this test, Pins 1 and 2 are common, and 4, 5 and 6 are common.

CTRICAL CHARACTERISTICS (T_A = 25°C Unless otherwise specified)

VIDUAL COMPONENT CHARACTERISTICS

Parameters	Test Conditions	Symbol	Device	Min	Typ	Max	Units
TER							
Forward Voltage	I_F = 10 mA	V_F	All		1.15	1.5	V
se Leakage Current	V_R = 3 V, T_A = 25°C	I_R	All		0.01	100	µA
CTOR							
Blocking Current,Either Direction	Rated V_{DRM}, I_F = 0 (note 1)	I_{DRM}	All		10	100	nA
On-State Voltage,Either Direction	I_{TM} = 100 mA peak, I_F = 0	V_{TM}	All		1.8	3	V

NSFER CHARACTERISTICS (T_A = 25°C Unless otherwise specified.)

haracteristics	Test Conditions	Symbol	Device	Min	Typ	Max	Units
rigger Current	Voltage = 3V (note 3)	I_{FT}	MOC3020M			30	mA
			MOC3010M			15	
			MOC3021M				
			MOC3011M			10	
			MOC3022M				
			MOC3012M			5	
			MOC3023M				
g Current, Either Direction		I_H	All		100		µA

voltage must be applied within dv/dt rating.

is static dv/dt. See Figure 5 for test circuit. Commutating dv/dt is a function of the load-driving thyristor(s) only.

evices are guaranteed to trigger at an I_F value less than or equal to max I_{FT}. Therefore, recommended operating I_F lies een max I_{FT} (30 mA for MOC3020M, 15 mA for MOC3010M and MOC3021M, 10 mA for MOC3011M and MOC3022M, \ for MOC3012M and MOC3023M) and absolute max I_F (60 mA).

Fig. 1 LED Forward Voltage vs. Forward Current

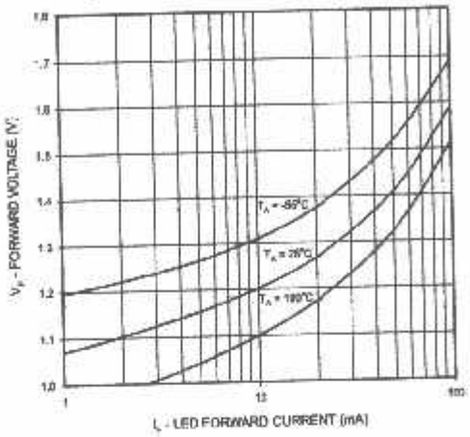


Fig. 2 On-State Characteristics

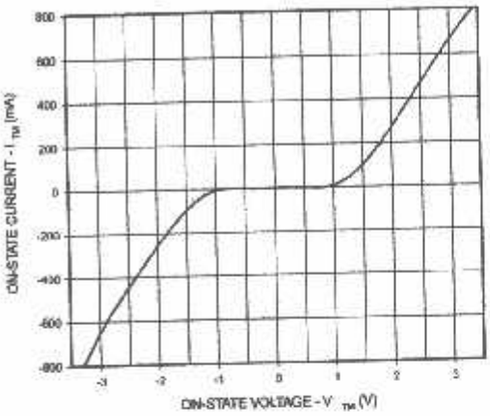


Fig. 3 Trigger Current vs. Ambient Temperature

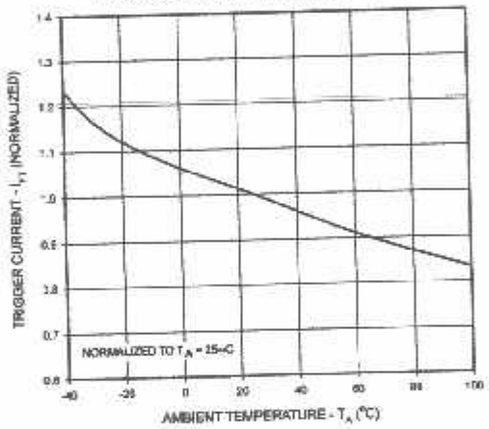


Fig. 4 LED Current Required to Trigger vs. LED Pulse Width

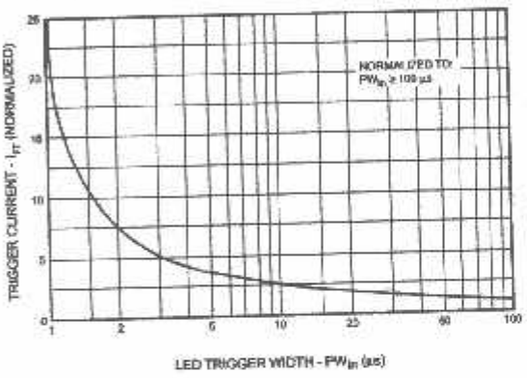


Fig. 5 dv/dt vs. Temperature

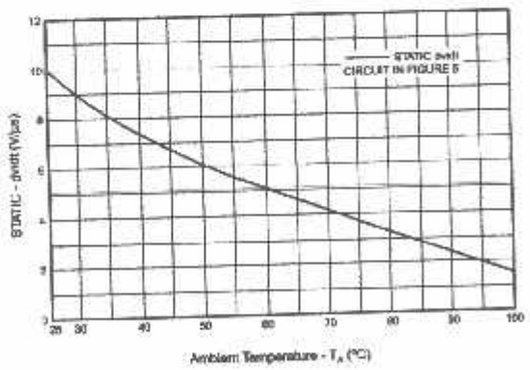
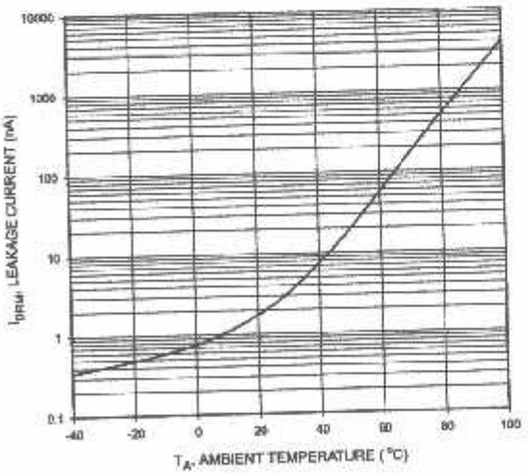
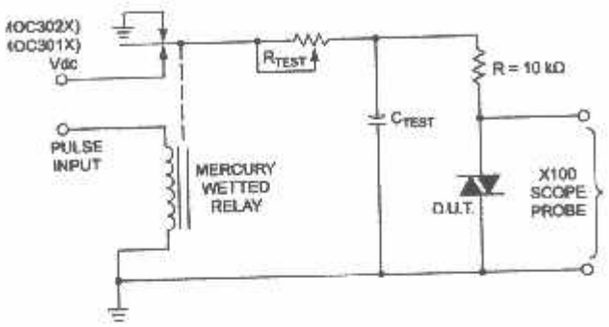


Fig. 6 Leakage Current, I_{DRM} vs. Temperature





1. The mercury wetted relay provides a high speed repeated pulse to the D.U.T.
2. 100x scope probes are used, to allow high speeds and voltages.
3. The worst-case condition for static dv/dt is established by triggering the D.U.T. with a normal LED input current, then removing the current. The variable R_{TEST} allows the dv/dt to be gradually increased until the D.U.T. continues to trigger in response to the applied voltage pulse, even after the LED current has been removed. The dv/dt is then decreased until the D.U.T. stops triggering. τ_{RC} is measured at this point and recorded.

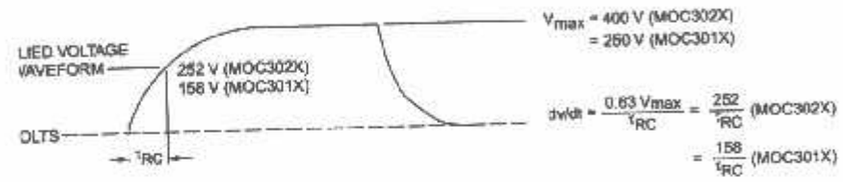


Figure 5. Static dv/dt Test Circuit

This optoisolator should not be used to drive a load directly. It is intended to be a trigger device only.

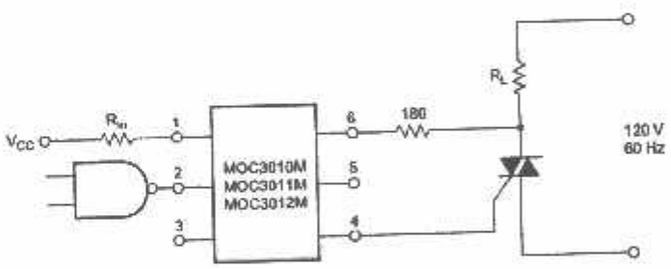


Figure 6. Resistive Load

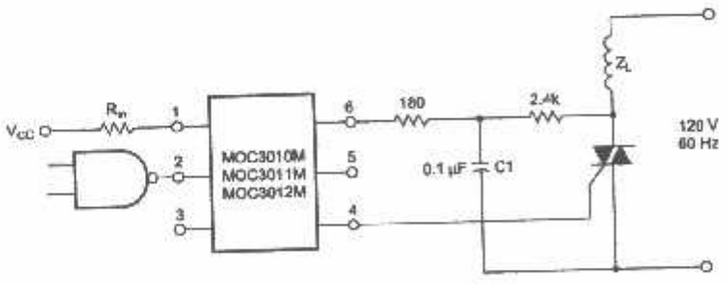


Figure 7. Inductive Load with Sensitive Gate Triac ($I_{GT} \leq 15$ mA)

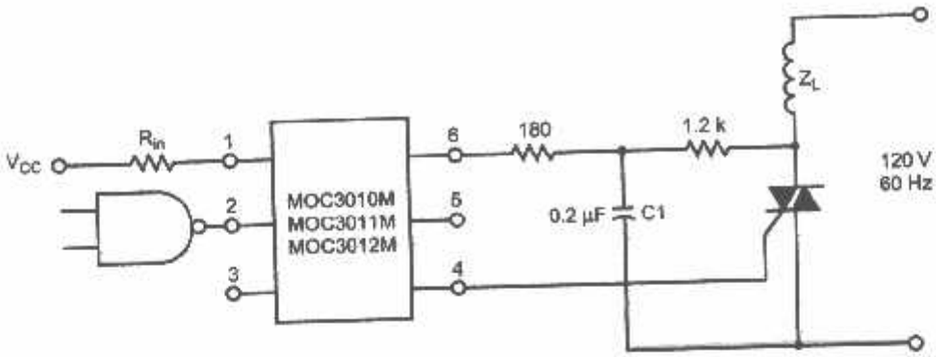
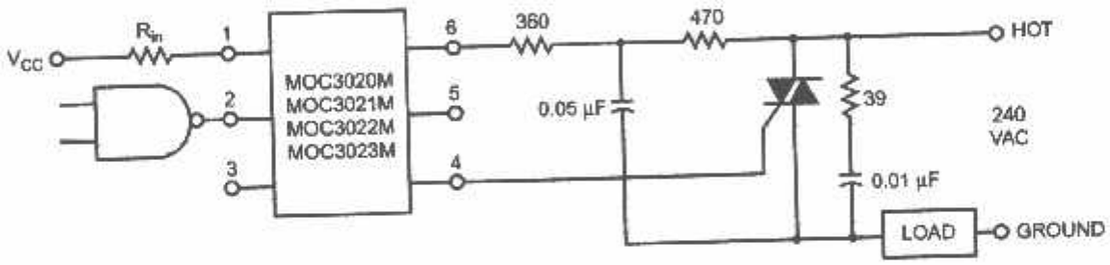


Figure 8. Inductive Load with Sensitive Gate Triac ($I_{GT} \leq 15$ mA)

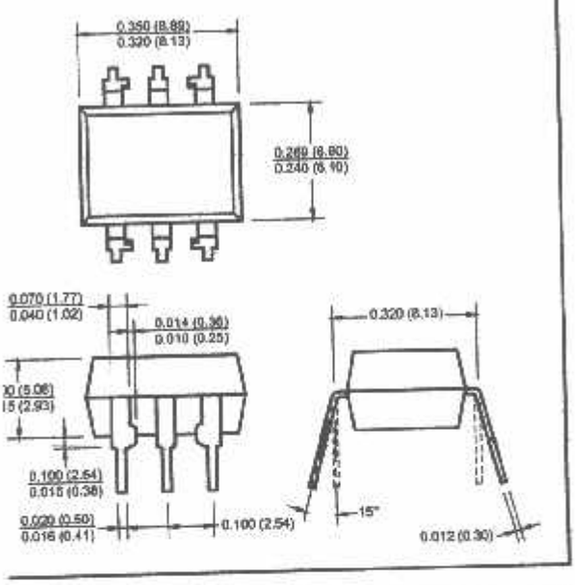


In this circuit the "hot" side of the line is switched and the load connected to the cold or ground side.

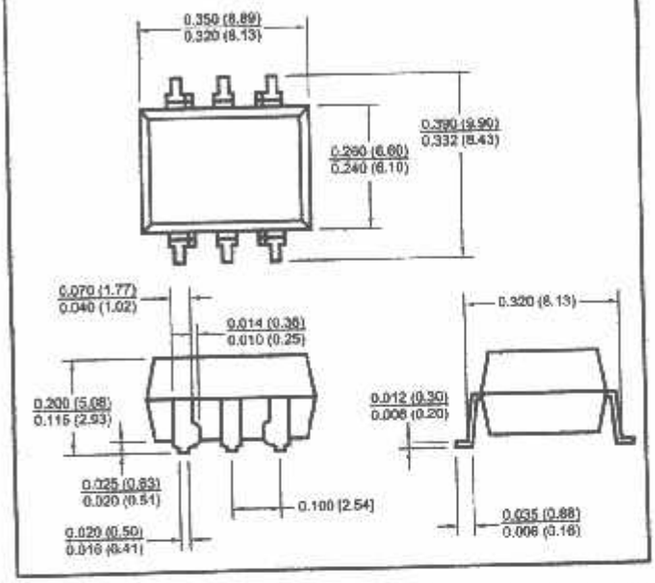
The 39 ohm resistor and 0.01µF capacitor are for snubbing of the triac, and the 470 ohm resistor and 0.05 µF capacitor are for snubbing the coupler. These components may or may not be necessary depending upon the particular and load used.

Figure 9. Typical Application Circuit

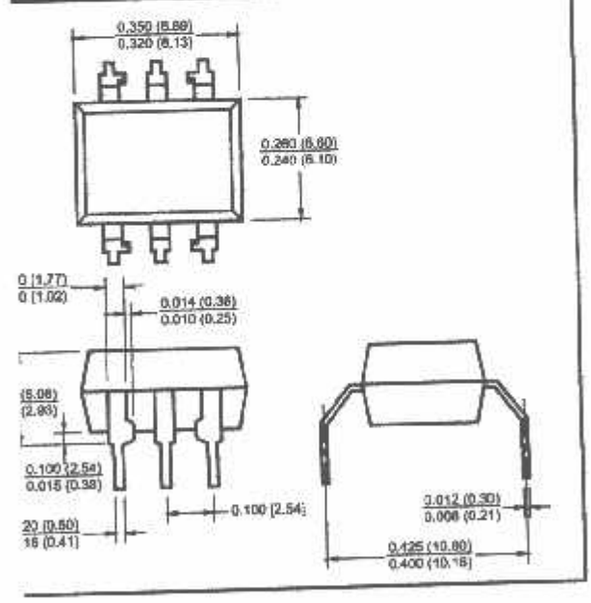
ackage Dimensions (Through Hole)



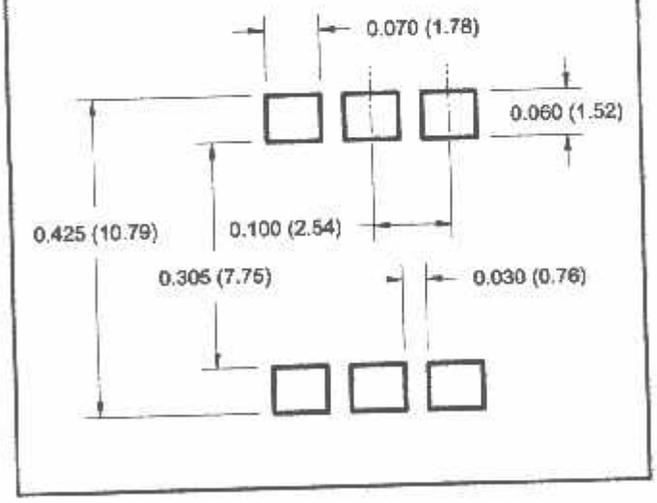
Package Dimensions (Surface Mount)



kage Dimensions (0.4" Lead Spacing)



Recommended Pad Layout for Surface Mount Leadform



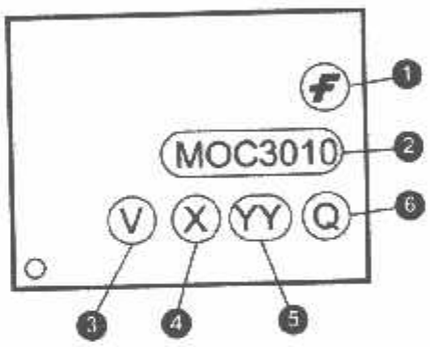
ensions are in inches (millimeters)

6-PIN DIP RANDOM-PHASE OPTOISOLATORS TRIAC DRIVER OUTPUT (250/400 VOLT PEAK)

ERING INFORMATION

on	Order Entry Identifier	Description
	S	Surface Mount Lead Bend
	SR2	Surface Mount; Tape and reel
	T	0.4" Lead Spacing
	V	VDE 0884
	TV	VDE 0884, 0.4" Lead Spacing
	SV	VDE 0884, Surface Mount
	SR2V	VDE 0884, Surface Mount, Tape & Reel

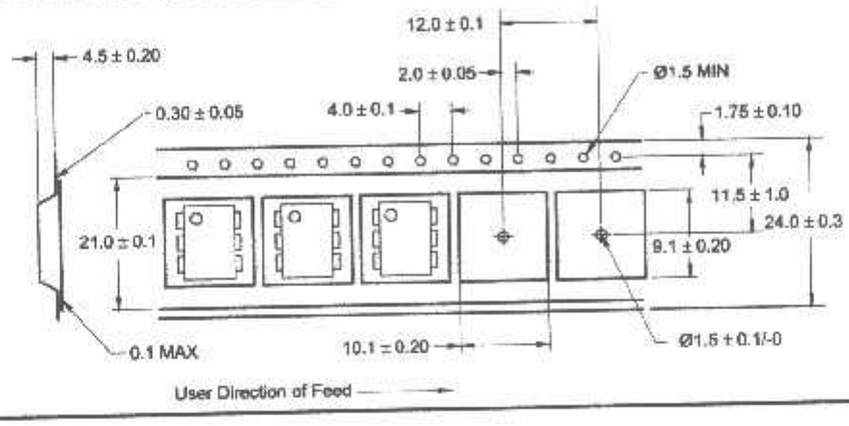
KING INFORMATION



Definitions	
1	Fairchild logo
2	Device number
3	VDE mark (Note: Only appears on parts ordered with VDE option – See order entry table)
4	One digit year code, e.g., '3'
5	Two digit work week ranging from '01' to '53'
6	Assembly package code

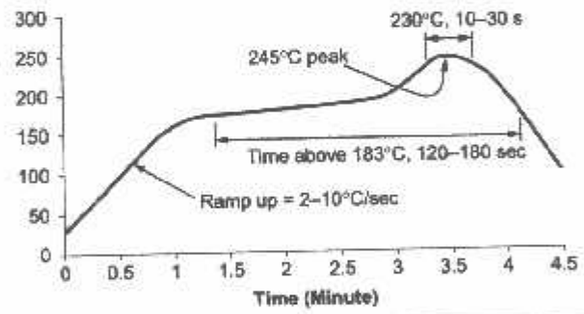
*Note – Parts that do not have the 'V' option (see definition 3 above) that are marked with date code '325' or earlier are marked in portrait format.

rier Tape Specifications



ensions are in inches (millimeters)

Profile (White Package, -M Suffix)



- Peak reflow temperature: 245°C (package surface temperature)
- Time of temperature higher than 183°C for 120–180 seconds
- One time soldering reflow is recommended

ERAL DESCRIPTION

ated triacs in a plastic envelope, ed for use in applications requiring idirectional transient and blocking capability and high thermal cycling mance. Typical applications include control, industrial and domestic ating and static switching.

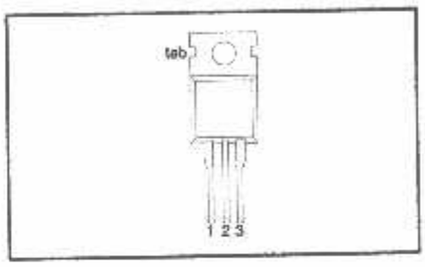
QUICK REFERENCE DATA

SYMBOL	PARAMETER	MAX.	UNIT
	BT136- BT136-	600 600F	
V_{DRM}	Repetitive peak off-state voltages	600	V
$I_{T(RMS)}$	RMS on-state current	4	A
I_{TSM}	Non-repetitive peak on-state current	25	A

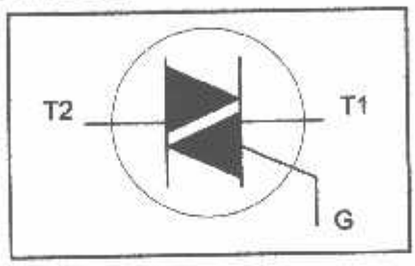
TO220AB

PIN	DESCRIPTION
1	main terminal 1
2	main terminal 2
3	gate
tab	main terminal 2

PIN CONFIGURATION



SYMBOL



TING VALUES

g values in accordance with the Absolute Maximum System (IEC 134).

BOL	PARAMETER	CONDITIONS				UNIT
	Repetitive peak off-state voltages			-	600[1]	V
	RMS on-state current	full sine wave; $T_{mb} \leq 107$ °C		-	4	A
	Non-repetitive peak on-state current	full sine wave; $T_j = 25$ °C prior to surge				
		t = 20 ms		-	25	A
		t = 16.7 ms		-	27	A
	I^2t for fusing	t = 10 ms		-	3.1	A^2s
	Repetitive rate of rise of on-state current after triggering	I_{TM} = 6 A; I_G = 0.2 A; dI_G/dt = 0.2 A/µs				
			T2+ G+	-	50	A/µs
			T2+ G-	-	50	A/µs
			T2- G-	-	50	A/µs
			T2- G+	-	10	A/µs
	Peak gate current			-	2	A
	Peak gate voltage			-	5	V
	Peak gate power			-	5	W
	Average gate					
	Storage temperature			-40	150	°C
	Operating temperature					°C

ough not recommended, off-state voltages up to 800V may be applied without damage, but the triac may to the on-state. The rate of rise of current should not exceed 3 A/µs.

RMAL RESISTANCES

IBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
R_{th}	Thermal resistance junction to mounting base	full cycle	-	-	3.0	K/W
		half cycle	-	-	3.7	K/W
R_{th}	Thermal resistance junction to ambient	in free air	-	60	-	K/W

TIC CHARACTERISTICS

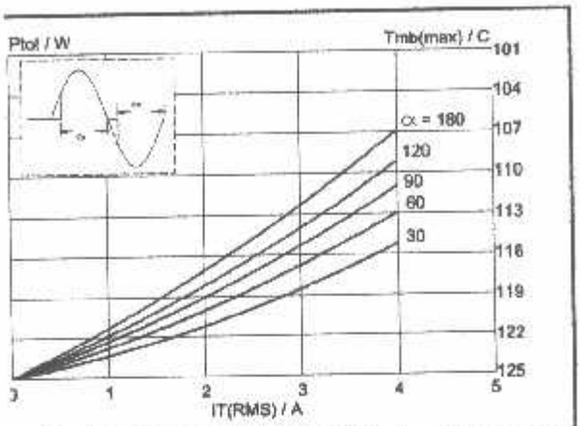
5 °C unless otherwise stated

IBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.		UNIT
		BT136-			...	...F	
	Gate trigger current	V_D = 12 V; I_T = 0.1 A					
		T2+ G+	-	5	35	25	mA
		T2+ G-	-	8	35	25	mA
		T2- G-	-	11	35	25	mA
		T2- G+	-	30	70	70	mA
	Latching current	V_D = 12 V; I_{GT} = 0.1 A					
		T2+ G+	-	7	20	20	mA
		T2+ G-	-	16	30	30	mA
		T2- G-	-	5	20	20	mA
		T2- G+	-	7	30	30	mA
	Holding current	V_D = 12 V; I_{GT} = 0.1 A	-	5	15	15	mA
	On-state voltage	I_T = 5 A	-	1.4	1.70		V
	Gate trigger voltage	V_D = 12 V; I_T = 0.1 A	-	0.7	1.5		V
		V_D = 400 V; I_T = 0.1 A; T_j = 125 °C	0.25	0.4	-		V
	Off-state leakage current	V_D = $V_{DRM(max)}$; T_j = 125 °C	-	0.1	0.5		mA

AMIC CHARACTERISTICS

5 °C unless otherwise stated

BOL	PARAMETER	CONDITIONS	MIN.		TYP.	MAX.	UNIT
		BT136-	...	...F			
dt	Critical rate of rise of off-state voltage	V_{DM} = 67% $V_{DRM(max)}$; T_j = 125 °C; exponential waveform; gate open circuit	100	50	250	-	V/µs
dV/dt	Critical rate of change of commutating voltage	V_{DM} = 400 V; T_j = 95 °C; $I_{T(RMS)}$ = 4 A; dI_{com}/dt = 1.8 A/ms; gate open circuit	-	-	50	-	V/µs
	Gate controlled turn-on time	I_{TM} = 6 A; V_D = $V_{DRM(max)}$; I_G = 0.1 A; dI_G/dt = 5 A/µs	-	-	2	-	µs



. Maximum on-state dissipation, P_{tot}, versus rms tate current, $I_{T(RMS)}$, where α = conduction angle.

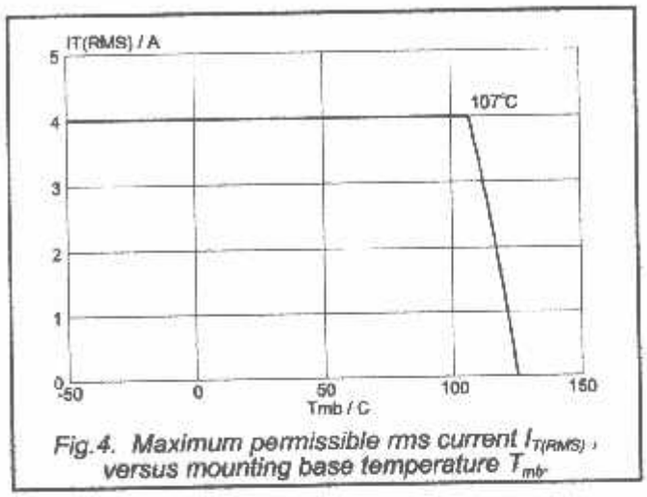
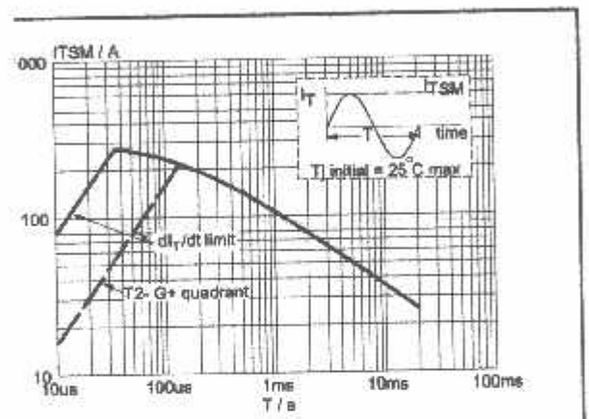


Fig.4. Maximum permissible rms current $I_{T(RMS)}$, versus mounting base temperature T_{mb}.



.2. Maximum permissible non-repetitive peak n-state current I_{TSM}, versus pulse width t_p, for sinusoidal currents, $t_p \leq 20ms$.

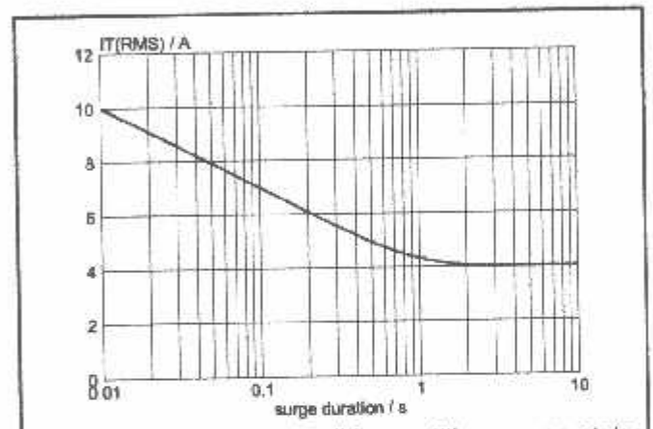
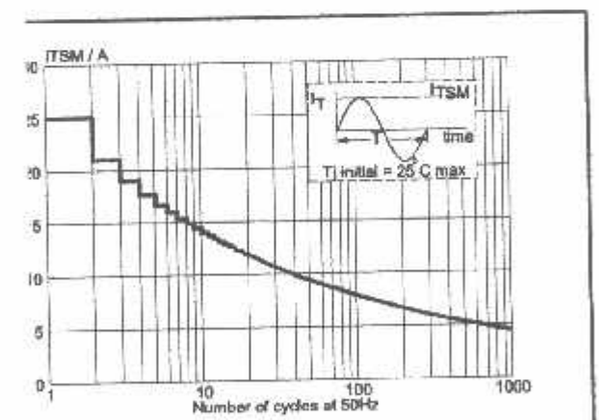


Fig.5. Maximum permissible repetitive rms on-state current $I_{T(RMS)}$, versus surge duration, for sinusoidal currents, $f = 50$ Hz; $T_{mb} \leq 107°C$.



.3. Maximum permissible non-repetitive peak -state current I_{TSM}, versus number of cycles, for sinusoidal currents, $f = 50$ Hz.

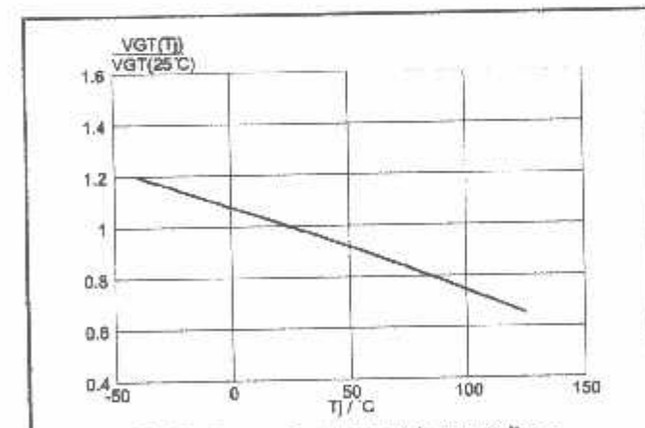


Fig.6. Normalised gate trigger voltage $V_{GT}(T_j)/ V_{GT}(25°C)$, versus junction temperature T_j.

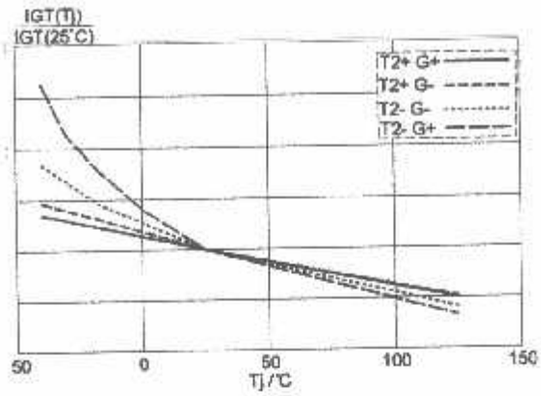


Fig.7. Normalised gate trigger current $I_{GT}(T_j)/I_{GT}(25°C)$, versus junction temperature T_j.

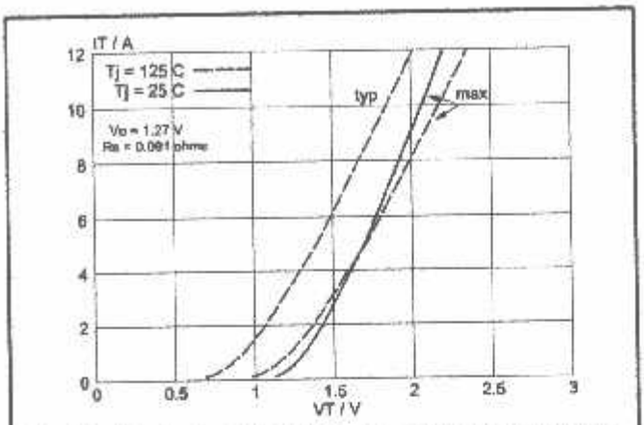
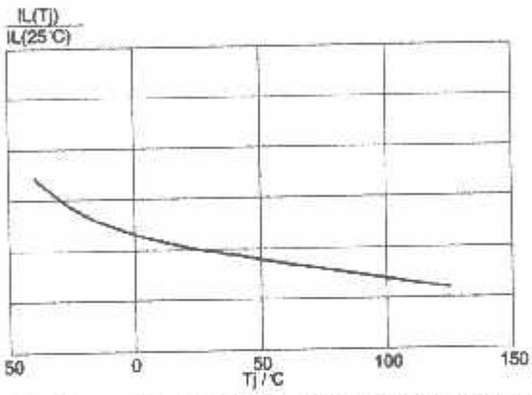


Fig.10. Typical and maximum on-state characteristic.



.8. Normalised latching current $I_L(T_j)/I_L(25°C)$, versus junction temperature T_j.

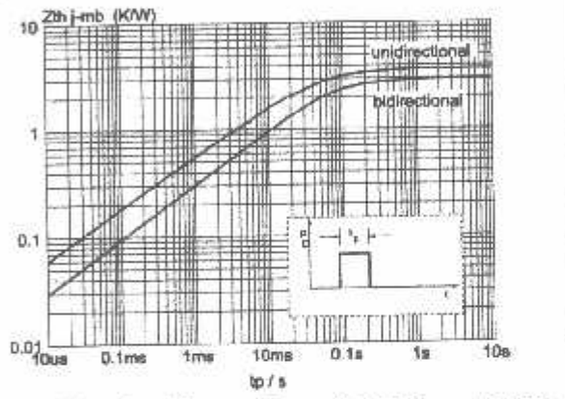
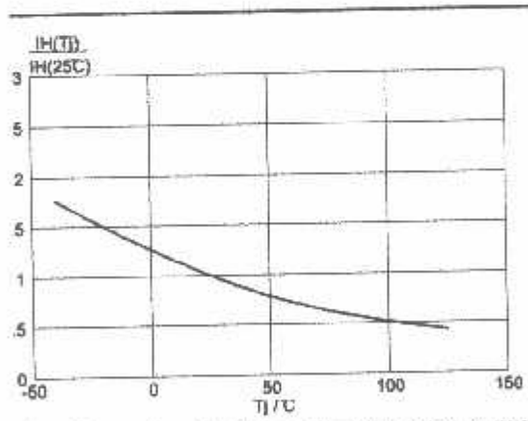


Fig.11. Transient thermal impedance $Z_{th\ j\text{-}mb}$ versus pulse width t_p.



.9. Normalised holding current $I_H(T_j)/I_H(25°C)$, versus junction temperature T_j.

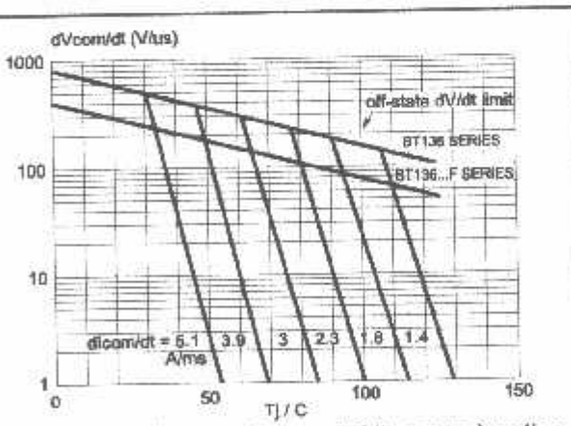


Fig.12. Typical commutation dV/dt versus junction temperature, parameter commutation dI_T/dt. The triac should commutate when the dV/dt is below the value on the appropriate curve for pre-commutation dI_T/dt.

HANICAL DATA

ensions in mm

Mass: 2 g

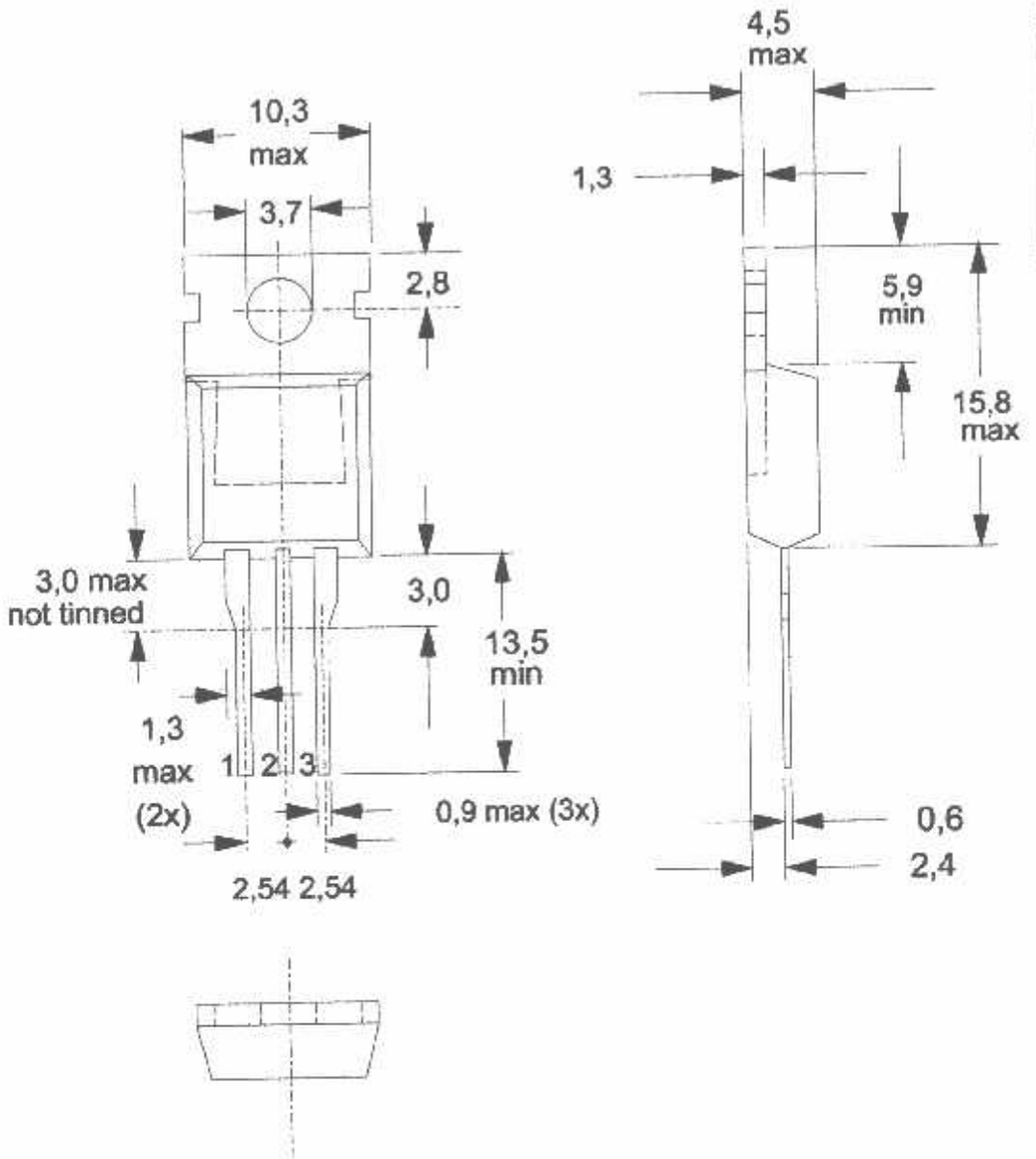


Fig.13. SOT78 (TO220AB). pin 2 connected to mounting base.

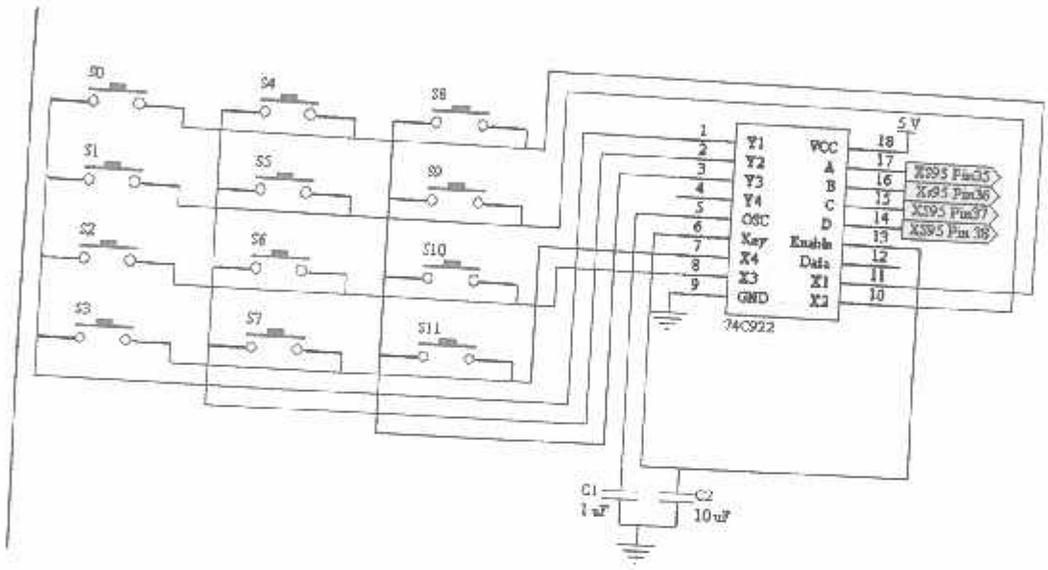
er to mounting instructions for SOT78 (TO220) envelopes.
xy meets UL94 V0 at 1/8".

Dari gambar blok diagram 3-1 dapat dijelaskan cara kerjanya sebagai berikut:

- Keypad sebagai inputan data 4 bit XS95108-20PC84 yang digunakan untuk tombol pengoperasian alat dan pemilihan jenis bahan bakar yang dipilih.
- Kartu Voucher berupa Serial EEPROM yang diisikan jumlah voucher untuk pengambilan bahan bakar yang diinginkan.
- Pada XS95 BOARD V1.3 terdapat XS95108-20PC84 yang telah diprogram untuk memberikan inputan pada IC Mikrokontroller.XS95108-PC84 juga digunakan sebagai penerima inputan dari keypad.
- Mikrokontroller AT89S51 sebagai pengontrol insialisasi, penulisan data dan instruksi pada LCD dan menerima data 4 bit dari XS95108-20PC84 guna penampilan jenis dan jumlah bahan bakar yang diambil .Mikrokontroller juga berfungsi sebagai reset global XS95108-20PC84.
- Display LCD sebagai penampil jenis bahan bakar yang dipilih.
- Driver Water Pump digunakan sebagai penghasil outputan yang diterima oleh AT89S51.

3.1.1 Perencanaan dan Pembuatan Rangkaian Keypad

Untuk memasukkan data pada XS95 board V1.3 sebagai pilihan bahan bakar maka dibutuhkan rangkaian keypad. Pada perencanaan dan pembuatan keypad ini menggunakan IC encoder MM74C922 dan keypad 3 x 4. Gambar 3-2 dihalaman berikut ini memperlihatkan suatu rangkaian keypad 3 x 4 dengan IC 74C922.



Gambar 3-2 Keypad Matrix 3 x 4 dengan IC MM74C922

Dari rangkaian di atas dapat diperoleh 12 kemungkinan output seperti pada tabel 3-1 berikut ini:

Tabel 3-1 Kombinasi Output Keypad Matrix 3 x 4

Switch	0	1	2	3	4	5	6	7	8	9	10	11
Position	X1	X2	X3	X4	X1	X2	X3	X4	X1	X2	X3	X4
Output	Y1	Y2	Y3	Y1	Y2	Y3	Y1	Y2	Y3	Y1	Y2	Y3
A	0	1	0	1	0	1	0	1	0	1	0	1
B	0	0	1	1	0	0	1	1	0	0	1	1
C	0	0	0	0	1	1	1	1	0	0	0	0
D	0	0	0	0	0	0	0	0	1	1	1	1

Berdasarkan data 4 bit pada tabel 2-1 maka dapat ditentukan fungsi dari setiap tombol. Keluaran data dari penekanan tombol dihubungkan langsung pada CPLD XS95108 -20 PC84 pada XS95 board V1.3 untuk menampilkan pilihan bahan bakar yang dibeli beserta jumlahnya. Sedangkan fungsi setiap tombol tersebut telah ditetapkan sebagai berikut:

- S0 berfungsi untuk pilihan Premium serta 1 liter dan data 4 bitnya "0000"
- S1 berfungsi untuk pilihan 4 liter dan data 4 bitnya "0001"
- S2 berfungsi untuk pilihan 7 liter dan data 4 bitnya "0010"
- S3 berfungsi untuk pilihan CLEAR(*) dan data 4 bitnya "0011"
- S4 berfungsi untuk pilihan Solar dan 2 liter dan data 4 bitnya "0100"

- S5 berfungsi untuk pilihan 5 liter dan data 4 bitnya "0101"
- S6 berfungsi untuk pilihan 8 liter dan data 4 bitnya "0110"
- S7 berfungsi untuk pilihan 0 liter dan data 4 bitnya "0111"
- S8 berfungsi untuk pilihan 3 liter dan data 4 bitnya "1000"
- S9 berfungsi untuk pilihan 6 liter dan data 4 bitnya "1001"
- S10 berfungsi untuk pilihan 9 liter dan data 4 bitnya "1010"
- S11 berfungsi untuk ENT (Enter) dan data 4 bitnya "1011"

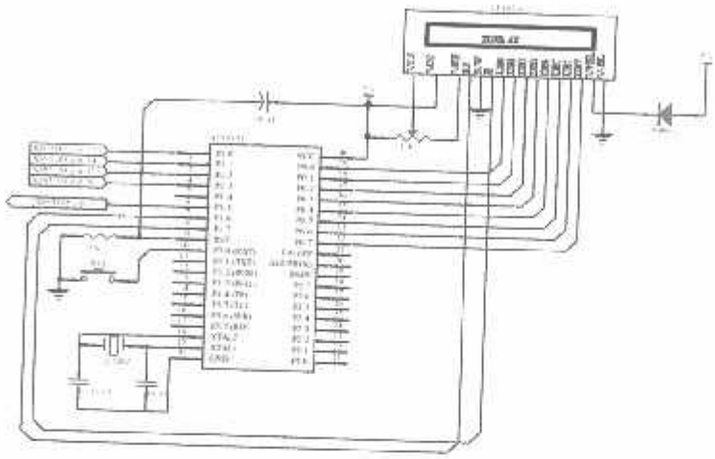
3.1.2 Rangkaian Mikrokontroller Dan Penampil LCD

Dalam perancangan ini digunakan mikrokontroller AT89S51 untuk pengiriman data dan intruksi pada LCD.Sebagai peraga digunakan LCD tipe YJ-162A dengan spesifikasi sebagai berikut:

- Dua baris dan karakter, tampilan LCD yang terdiri dari 5 x 7 dot matrik ditambah kursor.
- Pembangkit karakter ROM untuk 192 jenis karakter.
- Pembangkit karakter RAM untuk 8 jenis karakter.

Bus data LCD dihubungkan dengan port 0 mikrokontroller AT89S51. Sinyal kontrol E dihubungkan dengan pin P1.7 , RS dihubungkan dengan pin P1.6. Pin R/W

pada LCD dihubungkan ke GND sehingga mode LCD pada status tulis. Berikut ini adalah gambar rangkaian LCD yang terhubung dengan mikrokontroller.



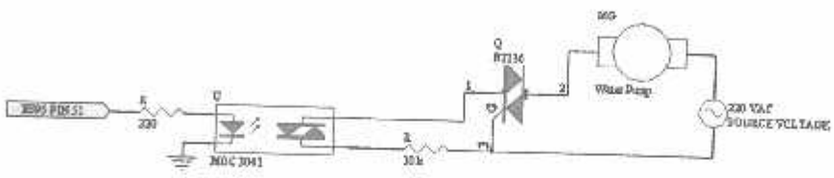
Gambar 3-3 Rangkaian Mikrokontroller Dan Penampil LCD

Mikrokontroller AT89S51 menerima data 4 bit dari XS95108 yang menerima data dari keypad sebagai identitas atau pengenalan data tampilan intruksi pengoperasian alat, tipe dan pemilihan jenis bahan bakar.

Port 3.0 mikrokontroller juga menerima inputan dari penekanan tombol push button yang dihubungkan ke Ground. Tombol ini berfungsi sebagai reset pada XS95108-20PC84.

3.1.3.Rangkaian Driver Water Pump

Untuk perancangan driver pompa digunakan Optotriac karena *Water pump* disini disupply dengan tegangan 220 VAC.



Gambar 3-4 Rangkaian Driver Pompa

Tegangan output maksimum dari XS95 adalah 5 V sedangkan untuk water pump memerlukan catu daya 220 VAC,maka diperlukan rangkaian driver untuk mengendalikannya.Rangkaian driver yang dipakai berupa optotriac MOC3041 dan triac type BT136,untuk analisa data yang digunakan.:

Vin = 5 V (Max)

Data sheet untuk mengaktifkan MOC 3041:

V_F (tegangan forward dioda) = 1,5 Volt

I_{FT} (Arus forward Trigger) = 15 mA

Maka untuk mengaktifkan optotriac R yang dipasang :

$$R=\frac{V_{in}-V_F}{I_{FT}}=\frac{5v-1,5v}{15mA}=\frac{3,5v}{15mA}=233\ \Omega$$

Nilai R yang mendekati dipasang 220 Ω

Kecepatan pompa yang dipakai pada rangkaian diatas adalah 1400 L /Jam sehingga bisa didapatkan waktu untuk per liternya dari pompa adalah:

$$\frac{1400L}{3600s}=0,39l/\det$$

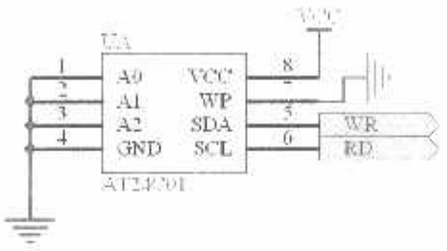
Sehingga didapatkan untuk pengisian 1 liter

$$\text{Waktu pengisian: } \frac{1liter}{0,39l/\det}=2,54\det \text{ atau dibulatkan menjadi 3 detik}$$

Untuk jumlah pengisian selanjutnya dibuat waktu pengisian kelipatan 3 detik.

3.1.4. Perencanaan Pembuatan Kartu Voucher

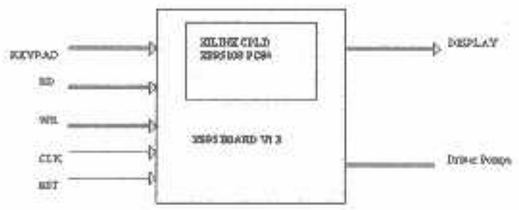
Untuk perancangan kartu voucher digunakan Serial EEPROM AT24C01A yang diisikan program berupa nilai voucher yang akan dibaca pada LCD.



Gambar 3-5 Konfigurasi Pin IC Serial EEPROM AT24C01

EEPROM disini dihubungkan dengan pin 32 dan pin 63 pada XS95 dimana pin tersebut merupakan $\overline{RD}$(P3.7) dan $\overline{WR}$(P3.6) pada mikrokontroller 8031 yang terdapat pada XS95 Board.Pin A0-A2 dihubungkan dengan Ground.pin SCL (Serial Clock) terhubung dengan pin 63 pada XS95 sedangkan pin SDA(Serial Data) dihubungkan dengan pin 32 pada XS95 sehingga pada mikrokontroller AT89S51 terbaca status EEPROM untuk ditampilkan pada LCD.

3.1.5 XS95 Board V1.3



Gambar 3-6 XS95 BOARD V1.3

Pada gambar diatas kaki-kaki yang dipakai pada XS95108-20 PC84 adalah:

- Kaki 33,34,35 dan 36 (Keypad) untuk inputan data 4 bit dari Keypad sebagai pemilihan jenis bahan bakar dan jumlah yang akan diambil.
- Kaki 9 (CLK) merupakan inputan untuk CLK (clock) XS95108-20PC84
- Kaki 11 (RST) merupakan inputan XS95108-20PC84 untuk RST (reset) yang dihubungkan dengan P1.5 pada mikrokontroller
- Kaki 45,46,47 dan 48 (MIKROKONTROLLER) merupakan outputan XS95108-20PC84 untuk input data mikrokontroller AT89S51.
- Kaki 14,15,17,18,19,21 dan 23 (S0-S6) merupakan outputan untuk seven segment pada XSBoard yang berkondisi active low.
- Kaki 49(GND) dan 78(VCC).

3.1.6 Perencanaan Clock

IC CPLD XS95108-20PC84 membutuhkan sinyal clock untuk berpindah dari satu kondisi ke kondisi yang lain, sebab dalam perancangan perangkat lunaknya perpindahan dari satu state ke state yang lain dieksekusi jika ada clock.

Perencanaan clock ini menggunakan DS1075Z100 - 100 MHz Osilator pada XS95 Board V1.3 yang dapat diprogram frekuensinya. Pemrograman clock mengunakan software GXSSETCLK dalam perencanaan alat ini clock diprogram pada 48,7 KHz.

3.2. Perancangan Software

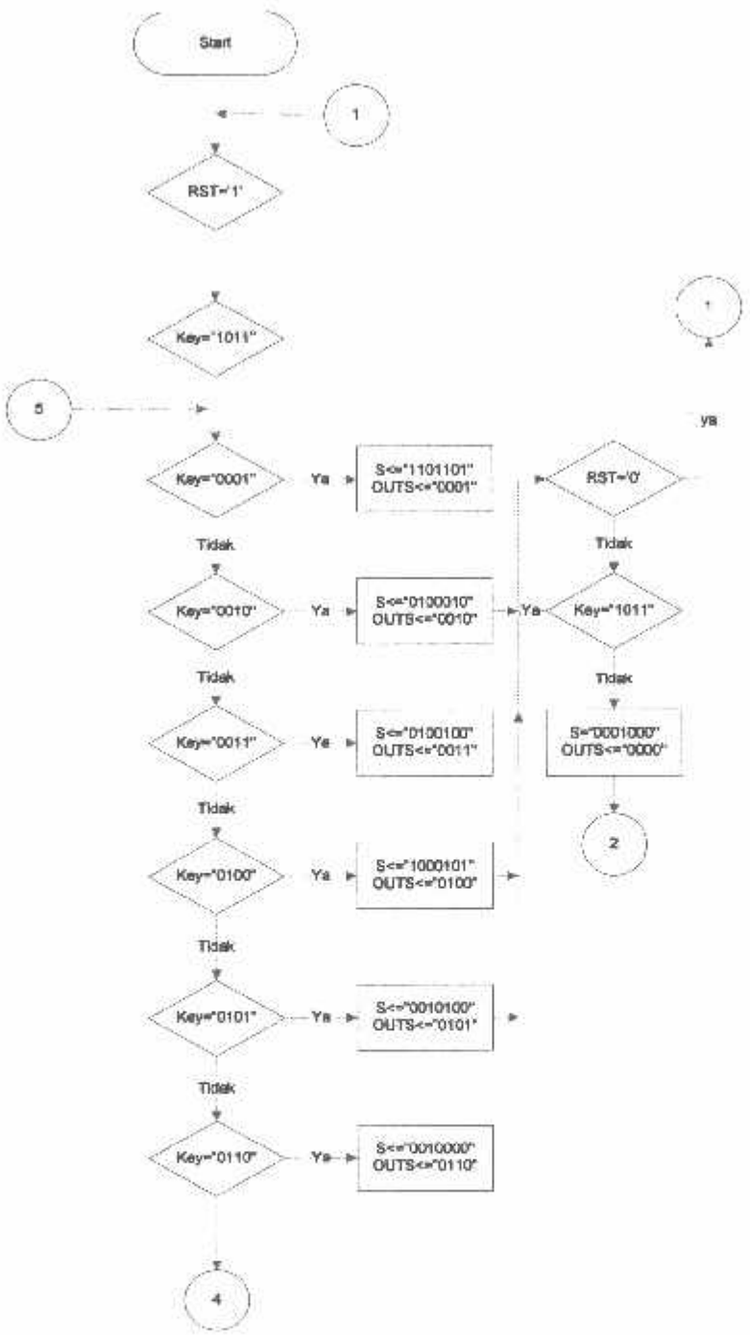
Untuk mengkonfigurasi IC CPLD XC95108-20-PC84 yang terdapat didalam XS95 Board V1.3, diperlukan sebuah file dengan ekstensi.svf. Untuk dapat menghasilkan file ini menggunakan software Xilinx Foundation Series 2.1i. Perancangan software ini menggunakan dua metode perancangan yaitu :

1. *Finite State Machine* (FSM)
2. *Schematic*

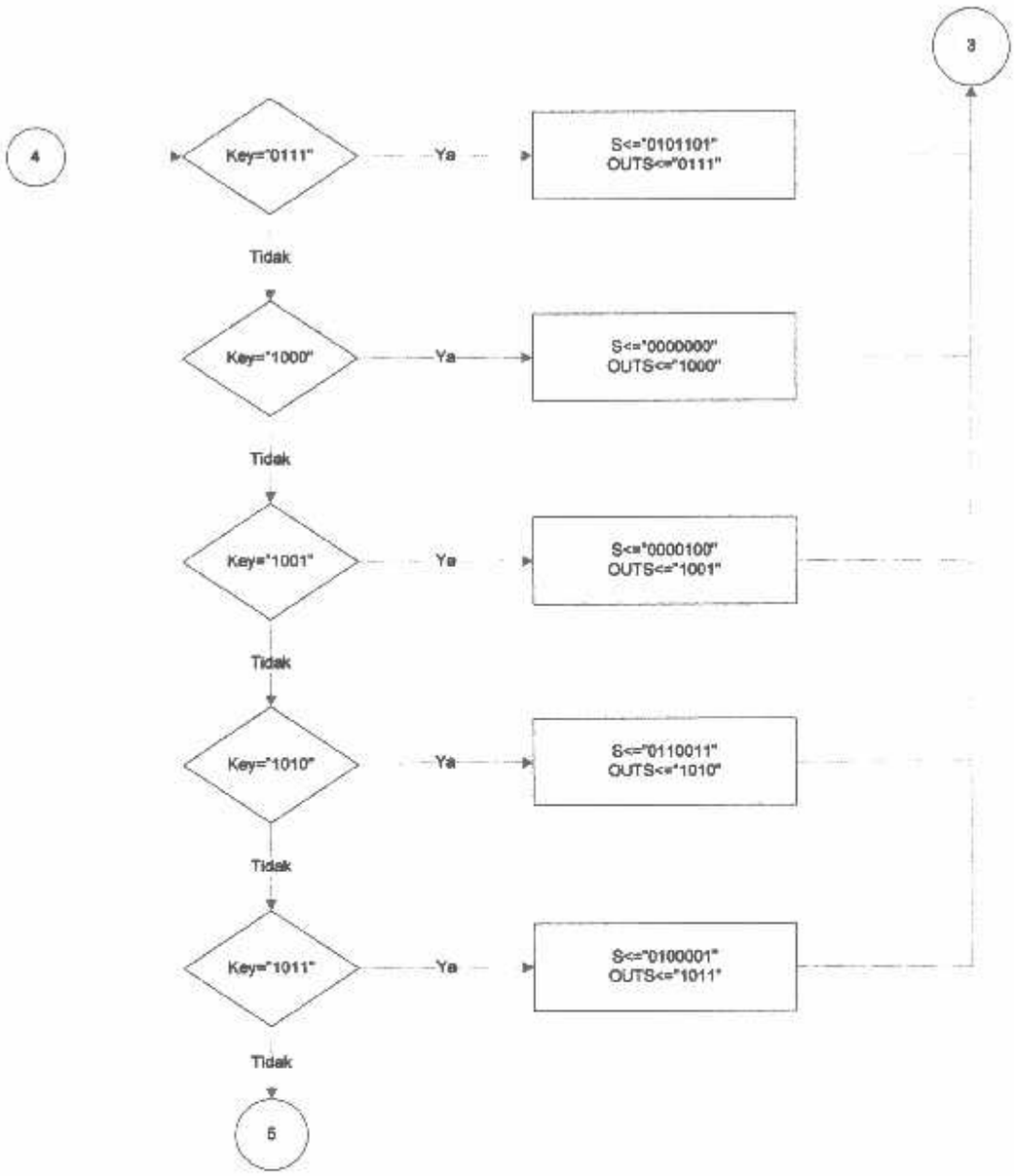
Kemudian desain tersebut akan disintesis, disimulasi dan kemudian akan dihasilkan file dengan ekstensi.sfv. File ini akan diimplementasikan ke IC CPLD XC95108-20-PC84 yang ada di dalam XS95 Board V1.3 dengan menggunakan

software GXSLOAD. Sedangkan untuk flowchart perancangan sofwarenya seperti pada gambar flowchart 3-7.

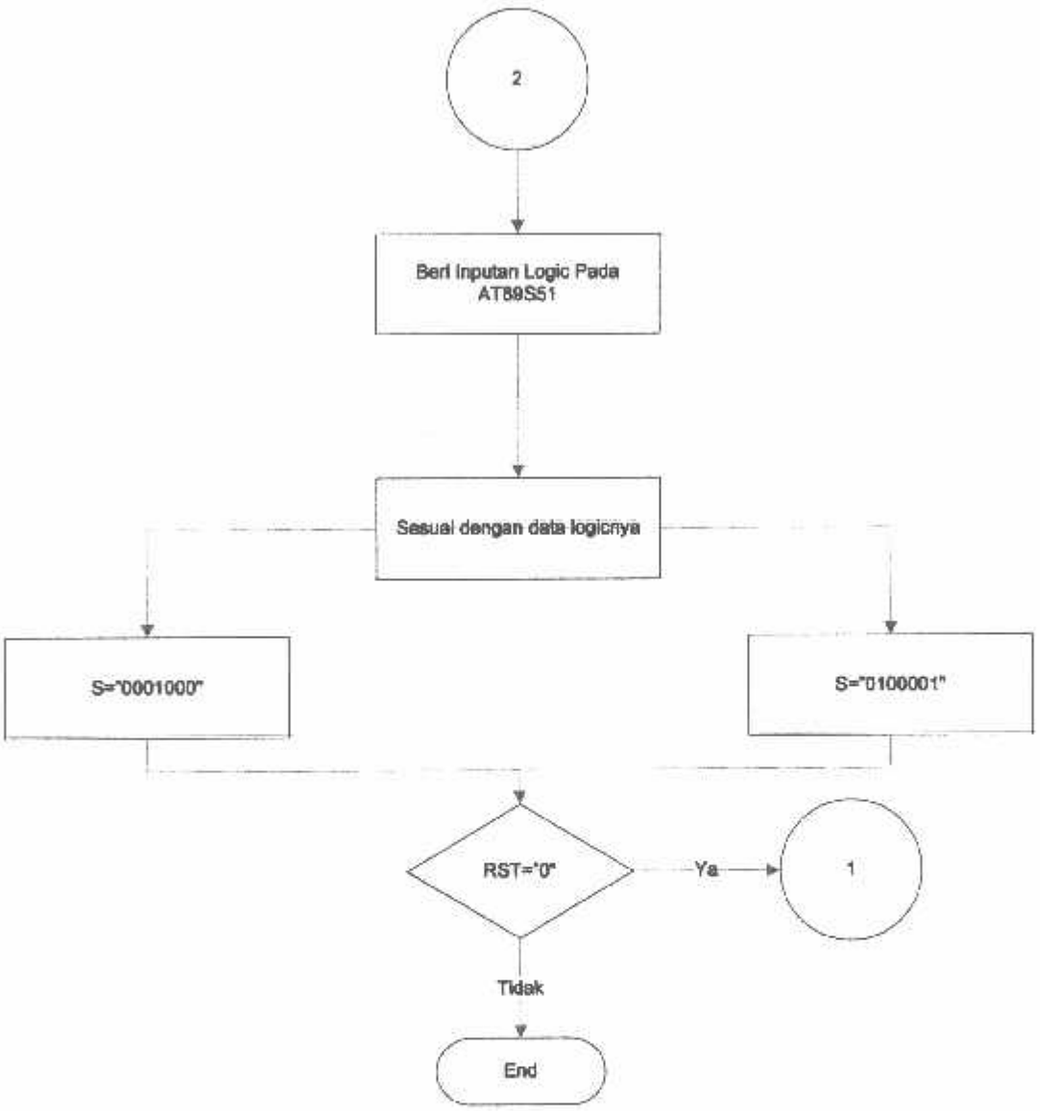
Sedangkan untuk pemprograman mikrokontroller AT89S51 digunakan bahasa assembler yang kemudian dikompilasi serta diubah ke dalam format heksa /biner dengan bantuan software HB2000W. Sedangkan untuk flowchart perancangan softwarenya seperti pada gambar 3-8.



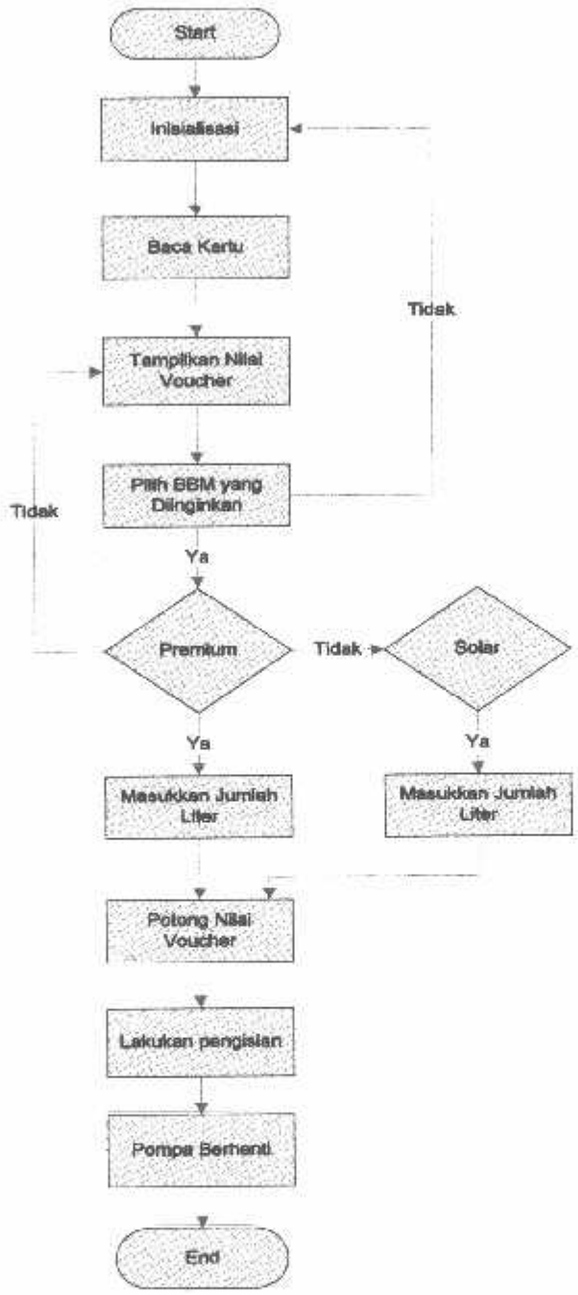
Gambar 3-7 (a) Flowchart Perangkat Lunak Xilinx Foundation Series 2.1i



Gambar 3-7 (b) Flowchart Perangkat Lunak Xilinx Foundation Series 2.1i



Gambar 3-7 (c) Flowchart Perangkat Lunak Xilinx Foundation Series 2.1i



Gambar 3-8 Flowchart sistem secara keseluruhan

BAB IV

PENGUJIAN DAN ANALISA

Pada bab ini membahas cara pegujian dan analisa dari alat yang dirancang, sehingga dapat diketahui apakah alat tersebut dapat bekerja sesuai dengan yang telah direncanakan. Dalam rangka pengujian alat tersebut diuraikan percobaan yang dilakukan untuk mengetahui respon dari keseluruhan alat yang telah dirancang.

Untuk mengetahui kemampuan alat dan sistem kerja sesuai dengan program yang telah dibuat maka dilakukan pengujian pada alat dan sistem kerja alat dengan prosedur pengujian sebagai berikut:

1. Pengujian perangkat keras
2. Pengujian perangkat lunak

4.1. Pengujian Perangkat Keras

Tujuan pengujian yang dilakukan terhadap sistem adalah sebagai berikut:

- Mengetahui unjuk kerja rangkaian Keypad
- Mengetahui unjuk kerja Motor AC
- Mengetahui unjuk kerja rangkaian clock
- Mengetahui unjuk kerja rangkaian mikrokontroller dengan display LCD
- Mengetahui tampilan seven segment pada XS95 Board V1.3.

4.1.1 Pengujian Rangkaian Keypad

➢ **Tujuan**

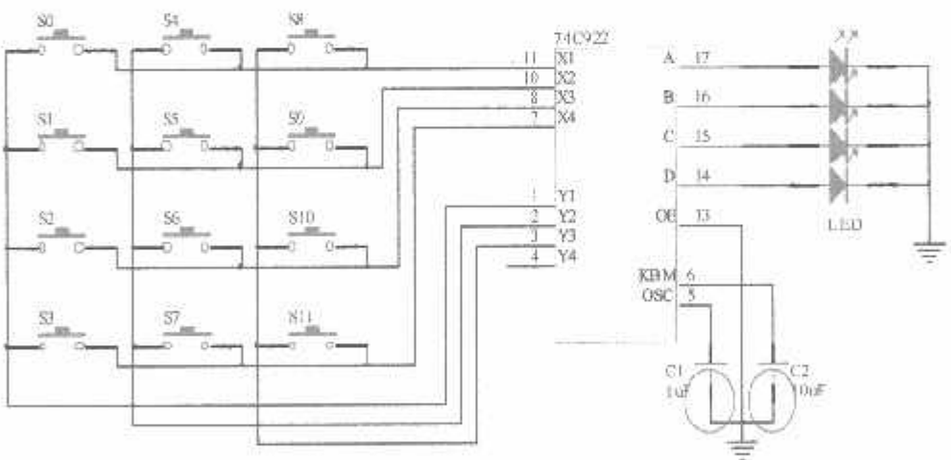
Pengujian rangkaian keypad ini bertujuan untuk mengetahui perubahan keluaran data 4 bit pada setiap penekanan tombol yang berbeda. Pengujian rangkaian keypad ini dilakukan sebagai berikut:

➢ **Peralatan yang digunakan**

1. Multimeter digital SANWA CD800
2. Rangkaian keypad yang akan diuji
3. Catu daya 5 Volt

➢ **Prosedur Pengujian**

1. Merangkai rangkaian keypad seperti pada gambar dibawah ini.



Gambar 4-1 Rangkaian Keypad

2. Menghubungkan rangkaian keypad dengan catu daya 5 Volt.

3. Melakukan pengukuran dan pengamatan output 4 bit (LED) sebagai inputan data XS95108-20PC84 terhadap penekanan setiap tombol, kemudian memasukan hasilnya berupa data 4 bit seperti pada tabel 4-1 dibawah ini.

Tabel 4-1 Data Output Rangkaian Keypad

INPUT		OUTPUT 4 BIT			
Tombol	Pilihan	D	C	B	A
S0	1 Liter	0	0	0	1
S1	4 Liter	0	1	0	0
S2	7 Liter	0	1	1	1
S3	CLEAR	1	0	1	0
S4	2 Liter	0	0	1	0
S5	5 liter	0	1	0	1
S6	8 Liter	1	0	0	0
S7	0 Liter	0	0	0	0
S8	3 Liter	0	0	1	1
S9	6 Liter	0	1	1	0
S10	9 liter	1	0	0	1
S11	ENTER	1	0	1	1

➢ **Analisa hasil pengujian**

Dari tabel 4-1 diatas maka dapat diketahui data 4 bit yang dikeluarkan IC encoder 74C922. Kemudian data tersebut dimasukan sebagai inputan data pada XS95108-20 PC84 untuk diproses sebagai pilihan jenis bahan bakar. Kemudian diikuti penekanan enter (1011) maka XS95108-20 PC84 menjalankan program tertentu untuk mengecek logikanya apakah sudah sesuai atau tidak.

Empat LED yang dipasang pada output A,B,C,D sebagai indikator logika 1 (high) atau 0 (low).Kondisi Led menyala sebagai logika high dan led padam sebagai kondisi low.

4.1.2. Pengujian Osilator DS1075Z100 - 100 MHz

- **Tujuan**

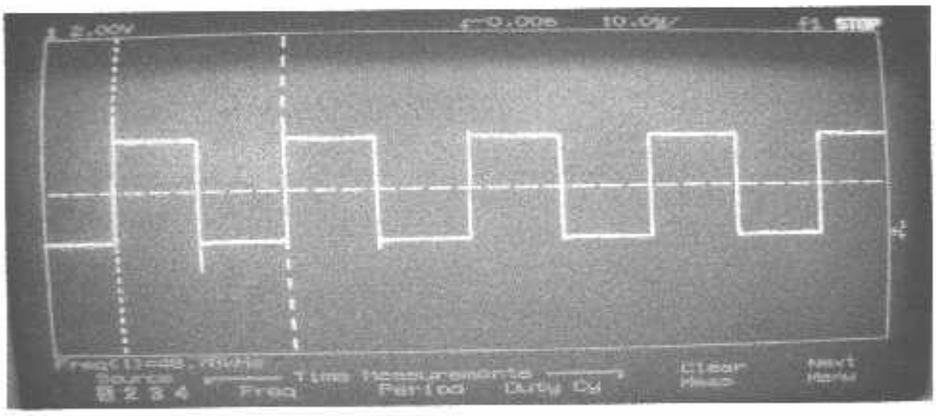
  Untuk mengetahui frekuensi yang dibangkitkan Osilator DS1075Z100 - 100 MHz guna perhitungan proses data XS95108-20PC84 dan sinkronisasi antar perangkat.

- **Peralatan yang digunakan**

  Satu buah Osciloscope HEWLETT PACKARD 54601A

- **Prosedur pengujian**

XS95 Board V1.3 memiliki sebuah IC osilator pulsa kotak yang dapat diprogram yaitu **DS1075Z100 - 100 MHz Osilator,** output pulsa osilator tersebut terhubung pada pin 9 dari XS95108-20PC84. Pada alat ini clock di setting pada 48,78 khz.



Gambar 4-2 Bentuk sinyal output DS1075Z100 - 100 MHz Osilator

Hasil pengujian yang terlihat pada osciloscope memastikan bahwa bentuk sinyal yang dihasilkan yaitu berupa pulsa kotak. Pada oscilloscope pembacaan frekuensi yang dihasilkan sebesar 49,15 KHz sedangkan sinyal yang direncanakan sebesar 48,78 KHz, maka terdapat persentase kesalahan yaitu:

$$\%kesalahan = \frac{selisihpengukurandanperencanaan}{nilaiperencanaan} x100\%$$

$$= \frac{49{,}15KHz - 48{,}78KHz}{48{,}78KHz} x100\%$$

$$= \frac{0{,}37KHz}{48{,}78KHz} x100\%$$

$$= 0{,}75\ \%$$

4.1.3 Pengujian Rangkaian Mikrokontroller AT89S51 Dengan Display LCD

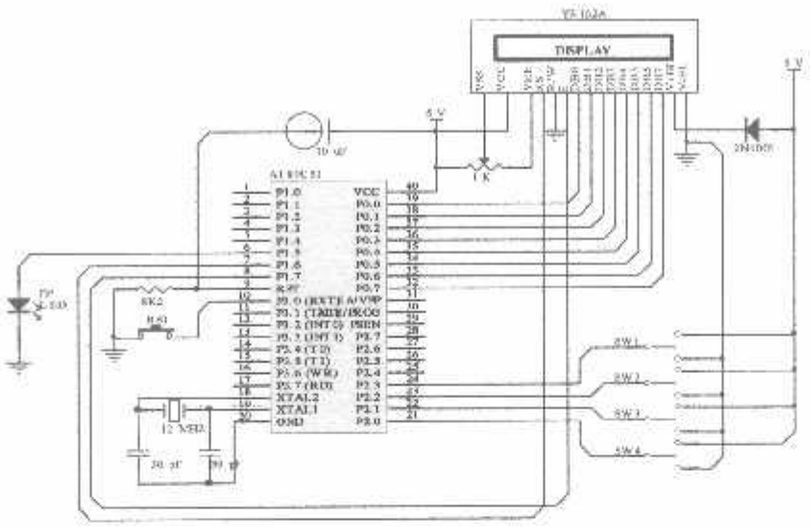
➢ **Tujuan**

1. Untuk mengetahui bentuk tampilan display LCD terhadap input data 4 bit yang berasal dari output XS95108-20PC84.
2. Untuk mengetahui output pada Port 2.5 mikrokontroller AT89S51 terhadap penekanan push button pada Port 3.0 mikrokontroller AT89S51.

➢ **Prosedur Pengujian**

Prosedur pengujian dilakukan berdasarkan alur listing program assembler yang telah dibuat. Untuk data inputan 4 bit digunakan 4 saklar yang dihubungkan dengan 5 V sebagai logika 1 dan ground (0 V) sebagai logika 0. Untuk inputan pada Port 3.0 digunakan push button yang dihubungkan dengan ground (0 V) dengan tujuan apabila ada penekanan maka Port 3.0 akan berlogika 0. Ketika Port 3.0 berlogika 0 maka output pada Port 2.5 akan berlogika 1 (led menyala) selama 0,0024 detik kemudian akan kembali berlogika 0 (led padam). Hal tersebut dilakukan sebagai reset global untuk XS95108-20PC84.

Pada gambar 4-4 pada halaman berikut ini merupakan skema rangkaian pengujian mikrokontroller AT89S51 dengan display LCD



Gambar 4-4 Pengujian Rangkaian Mikrokontroller AT89S51 Dengan Display LCD

4.1.4. Pengujian Driver Motor AC

- **Tujuan**

  Untuk mengetahui apakah driver ini dapat menggerakkan atau mengaktifkan motor AC dalam hal ini Pompa Air.

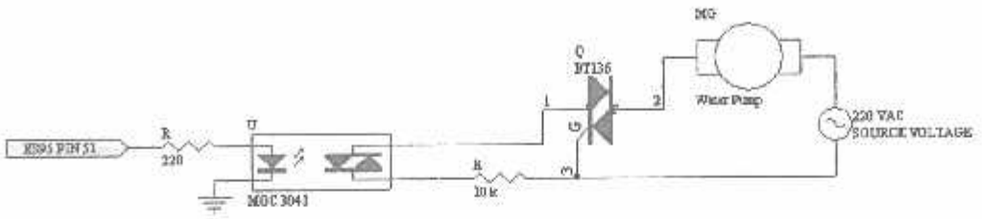
- **Peralatan Yang Digunakan**

  1.Multimeter Digital PROACE

  2.DC Adaptor 5 volt

➢ **Prosedur Pengujian**

1.Merangkai rangkaian driver seperti pada gambar dibawah ini:



Gambar 4-5 Pengujian Rangkaian driver Motor AC

2.Untuk inputan dari IC XS95 Board digantikan tegangan DC adaptor 5 V.

3.Melakukan pengukuran dan pengamatan.

4.Analisa hasil pengujian.

Dari pengukuran dan pengamatan,diuji apakah motor AC akan hidup apabila inputan diberi tegangan.

Tabel 4-2 Pengujian Driver Motor AC

Input Tegangan (DC)	Tegangan Input (AC)	Tegangan Pada Pompa (DC)	Arus pada Pompa (mA)	Kondisi Pompa
4,93	223	4,87	81,8	On (Hidup)
0	0	0	0	Off (Mati)

Diketahui Daya (P) pompa=18 Watt

Sehingga arus I pada saat pompa hidup adalah:

$$I = \frac{P}{V} = \frac{18}{223} = 0{,}08A \text{ atau } 80 \text{ mA}$$

Persentase kesalahan pada driver motor AC apabila diberi lamanya waktu pengisian per-liternya adalah 3 detik dan kelipatannya.

$$\%Kesalahan = \frac{waktusebenarnya}{waktupadaprogram} x100\%$$

$$= \frac{2.54 \det ik}{3 \det ik} x100\% = 0{,}847$$

Sehingga didapatkan error pada pengisian per-liternya adalah:

Jumlah liter x %kesalahan = 1 . 0,847=0,717 ml

4.1.4 Pengujian Tampilan Seven Segment pada XS95 Board V1.3

- **Tujuan**

  Untuk mengetahui apakah tampilan 7-segment pada XSBoard V1.3 sesuai dengan inputan dari keypad.

- **Prosedur Pengujian**

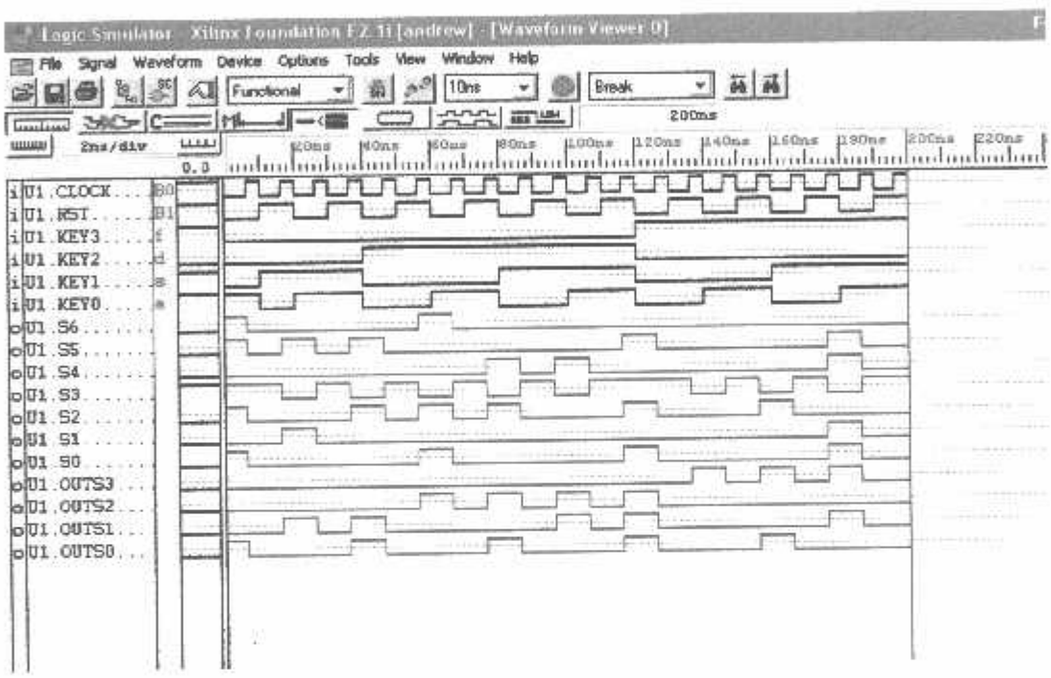
  Prosedur pengujian dilakukan berdasarkan outputan keypad DCBA yang masuk sebagai inputan ke XS95 Board untuk diproses kedalam AT89S51.data 4 bit yang masuk keXS95 board kemudian ditampilkan pada 7-segment yang berlogic low(active low common anoda) yang terdapat pada XS95 Board.

Tabel 4-3 hasil tampilan 7-segment pada XS95 Board V1.3

Clock	Input Keypad				Output S pada XS Board							Tampilan 7-segment
	Key0	Key1	Key2	Key3	G	F	B	A	E	C	D	
0	0	0	0	0	0	0	0	1	0	0	0	0
1	0	0	0	1	1	1	0	1	1	0	1	1
2	0	0	1	0	0	1	0	0	0	1	0	2
3	0	0	1	1	0	1	0	0	1	0	0	3
4	0	1	0	0	1	0	0	0	1	0	1	4
5	0	1	0	1	0	0	1	0	1	0	0	5
6	0	1	1	0	0	0	1	0	0	0	0	6
7	0	1	1	1	0	1	0	1	1	0	1	7
8	1	0	0	0	0	0	0	0	0	0	0	8
9	1	0	0	1	0	0	0	0	1	0	0	9
ENT	1	0	1	1	0	1	0	0	0	0	0	a
CLR	1	0	1	0	1	1	1	0	0	1	0	c

4.2. Pengujian Perangkat Lunak

Perangkat lunak yang telah dibuat dapat disimulasikan secara diagram waktu terlebih dahulu sebelum diimplementasikan ke perangkat keras. Dengan melalui simulasi diagram waktu ini dapat dilihat apakah perangkat lunak yang telah dibuat dapat merepresentasikan sistem yang dirancang atau belum. Berikut ini adalah gambar secara diagram waktu perangkat lunak yang dibuat.



Gambar 4-6 Hasil Simulasi Perangkat Lunak Xilinx Foundation 2.1i

BAB V

KESIMPULAN DAN SARAN

5.1 Kesimpulan

Berdasarkan perencanaan dan pembuatan sistem kartu prabayar pada SPBU menggunakan XS95 Board V1.3 dapat diambil kesimpulan sebagai berikut:

1. Sistem ini memakai kartu voucher jenis EEPROM AT24C01 yang diisikan data yang dapat dibaca oleh mikrokontroller untuk ditampilkan di LCD.
2. Mikrokontroller AT89S51 digunakan sebagai pemberi data ke LCD yang digunakan untuk menampilkan menu,jenis bahan bakar dan jumlah liter.
3. Pengendali driver motor AC menggunakan Optotriac MOC3041 dan TRIAC BT136 yang dihubungkan dengan pin 51 pada XS95 Board V1.3 dapat berfungsi dengan baik.
4. Jumlah liter yang bisa diambil adalah 1 – 9 liter berdasarkan nilai yang dihasilkan oleh keypad, dengan waktu pengisian tiap liternya adalah selama 3 detik serta kelipatannya sedangkan error pengisian tiap liternya adalah 0.8%.
5. Tampilan 7-segment pada XS95 Board V1.3 sesuai dengan data yang diberikan oleh keypad.
6. Sistem ini dapat menggantikan metode konvensional dalam pengisian di SPBU menjadi Self-service.

5.2 Saran

Tujuan utama dari penulisan adalah bagaimana membuat suatu sistem kartu prabayar untuk SPBU dimana konsumen dapat memilih jumlah liter sendiri.Saran-saran yang bisa digunakan untuk pengembangan alat ini secara lanjut antara lain:

1. Adanya peningkatan jumlah liter menjadi 2 digit sehingga memudahkan konsumen yang ingin membeli dalam jumlah besar.
2. Pengembangan dalam hal tampilan LCD yang langsung diaplikasikan dari XS95 Board V1.3 sendiri sehingga tidak perlu lagi memakai mikrokontroller AT89S51.
3. Pengembangan dalam hal pembuatan kartu voucher yang masih memakai serial EEPROM AT24C01A diganti dengan memakai RF ID,Barcode Reader dsb.

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LAMPIRAN

1.Lembar Bimbingan

2.Daftar Asistensi

3.Formulir Peminjaman Alat

3.Gambar-gambar Bukti Pembuatan Alat

4.Rancangan Perangkat Lunak

6.Data Sheet

- 6.1.Data Sheet Xilinx CPLD XC95108
- 6.2.Data Sheet AT89S51
- 6.3.Data Sheet Serial EEPROM AT24C01A
- 6.4.Data Sheet MM74C922
- 6.5.Data Sheet TRIAC BT136
- 6.6.Data Sheet OPTOTRIAC MOC3041

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LEMBAR PERSETUJUAN PERBAIKAN SKRIPSI

Dari hasil ujian skripsi jurusan Teknik Elektro jenjang strata satu (S-1), yang diselenggarakan pada:

Hari : Senin
Tanggal : 20 Maret 2006

Telah dilakukan perbaikan oleh:

Nama : ANDREW EKA YUSUF
N.I.M : 01.17.014
Jurusan : TEKNIK ELEKTRO S-1
Konsentrasi : ELEKTRONIKA
Judul Skripsi : **PERANCANGAN DAN PEMBUATAN SISTEM KARTU PRABAYAR PADA SPBU MENGGUNAKAN TEKNOLOGI BERBASIS CPLD XS95 BOARD V1.3**

Perbaikan meliputi:

No.	Materi Perbaikan	Keterangan
1.	Kesimpulan	
2.	Pengujian Driver Water Pump	

Diperiksa dan Disetujui,

Dosen Pembimbing

r.Widodo Pudji Muljanto,MT

Anggota Penguji

Penguji I

Ir.Sidik Noertjahjono,MT

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JURUSAN TEKNIK ELEKTRO
KONSENTRASI ELEKTRONIKA

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Judul Skripsi : **PERANCANGAN DAN PEMBUATAN SISTEM KARTU PRABAYAR PADA SPBU MENGGUNAKAN TEKNOLOGI BERBASIS CPLD XS95 BOARD V1.3**

Perbaikan meliputi:

No.	Materi Perbaikan	Keterangan
1.	Kesimpulan	25/'06

Diperiksa dan Disetujui,

Dosen Pembimbing

Ir.Widodo Pudji Muljanto,MT

Anggota Penguji

Penguji I

Sotyohadi,ST

INSTITUT TEKNOLOGI NASIONAL MALANG
FAKULTAS TEKNOLOGI INDUSTRI
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KONSENTRASI TEKNIK ELEKTRONIKA

LEMBAR BIMBINGAN SKRIPSI

Nama	: ANDREW EKA YUSUF
NIM	: 01.17.014
Jurusan	: Teknik Elektro S-1
Konsentrasi	: Teknik Elektronika
Judul Skripsi	: **PERANCANGAN DAN PEMBUATAN SISTEM KARTU PRABAYAR PADA SPBU MENGGUNAKAN TEKNOLOGI BERBASIS CPLD XS95 BOARD V1.3.**
Tanggal Mengajukan Skripsi	: 27 Juli 2005
Tanggal Menyelesaikan Skripsi	: 20 Maret 2006
Dosen Pembimbing	: Ir.Widodo Pudji Muljanto, MT
Telah dievaluasi dengan nilai	: 78 (tujuh puluh delapan)

Mengetahui
Ketua Jurusan Teknik Elektro

Ir. F. Yudi Limpraptono, MT
NIP.Y. 1039500274

Diperiksa dan Disetujui
Dosen Pembimbing

Ir.Widodo Pudji M, MT
NIP : 102 8700171

INSTITUT TEKNOLOGI NASIONAL
JL. BENDUNGAN SIGURA-GURA 2
MALANG

FORMULIR BIMBINGAN SKRIPSI

Nama : Andrew Eka Yusuf
Nim : 0117014
Masa Bimbingan : 27-Jul-2005 s/d 27-Jan-2006
Judul Skripsi : Perancangan dan pembuatan system kartu prabayar pada SPBU dengan menggunakan teknologi CPLD (IC XC95-108 PC84)

NO	Tanggal	Uraian	Paraf Pembimbing
1.	12/1 06	Konsultasi Bab I - IV	
2.	14/1 '06	Acc Bab I dan II	
3.	15/01 '06	Konsultasi Bab III	
4.	16/01 06	Revisi Diagram Blok	
5.	15/01 06	Revisi Gambar XC95	
6.	16/01 06	Konsultasi Bab IV	
7.	17/01 06	Acc Bab III dan IV	
8.	25/1 06	Acc Makalah Seminar	
9.		Demo Alat	
10		Kompre	

Malang, 2005
Dosen Pembimbing

Ir. Widodo Pudji M., MT

Form. S-4a

PERKUMPULAN PENGELOLA PENDIDIKAN UMUM DAN TEKNOLOGI NASIONAL MALANG
INSTITUT TEKNOLOGI NASIONAL MALANG
FAKULTAS TEKNOLOGI INDUSTRI
FAKULTAS TEKNIK SIPIL DAN PERENCANAAN
PROGRAM PASCASARJANA MAGISTER TEKNIK
(PERSERO) MALANG
NIAGA MALANG
Kampus I : Jl. Bendungan Sigura-gura No. 2 Telp. (0341) 551431 (Hunting) Fax. (0341) 553015 Malang 65145
Kampus II : Jl. Raya Karanglo, Km 2 Telp. (0341) 417636 Fax. (0341) 417634 Malang

Malang 27-Jul-2005

Nomor : ITN-683/7/TA.GNF/2005
Lampiran :
Perihal : *Bimbingan Skripsi*

Kepada : Yth. Sdr. **Ir. Widodo Pudji M., MT**
Dosen Pembimbing
Jurusan Teknik Elektro S-1
di
Malang

Dengan hormat,
Sesuai dengan permohonan dan persetujuan dalam proposal skipsi untuk mahasiswa:

Nama	: Andrew Eka Yusuf
Nim	: 0117014
Semester	: VIII
Fakultas	: Teknologi Industri
Jurusan	: Teknik Elektro S-1
Konsentrasi	: Teknik Elektronika

Maka dengan ini pembimbingan tersebut kami serahkan sepenuhnya kepada Saudara/i selama masa waktu 6 (enam) bulan, terhitung mulai tanggal:

27-Jul-2005 s/d 27-Jan-2006

Sebagai satu syarat untuk menempuh Ujian Akhir Sarjana.
Demikian agar maklum, atas perhatian dan bantuannya kami ucapkan banyak terima kasih.

Ketua Jurusan
Teknik Elektro S-1

Ir. F. Yudi Limpraptono, MT
NIP. P. 1039500274

Form S-1a

Perihal : Permohonan Peminjaman Alat

Kepada Yth :
Bapak Joseph Dedy Irawan.ST,MT
Kasie Laboratorium Elektronika Digital
Di tempat

Dengan hormat,

Sehubungan dengan pengajuan skripsi yang telah diprogram dan dalam hal ini saya merencanakan membuat sebuah alat sebagai syarat memperoleh gelar sarjana, maka saya :

Nama	: Andrew Eka Yusuf
Jurusan	: Teknik Elektro S1
Konsentrasi	: Teknik Elektronika
NIM	: 01.17.014

Bermaksud meminjam alat laboratorium untuk keperluan pengerjaan tugas akhir serta untuk pengujian dan analisa data dari alat yang saya rancang, oleh karena itu berkenan kiranya Bapak meminjamkan **XS95 Board V1.3** dengan waktu penggunaan alat selama satu minggu.

Demikian surat ini dibuat, atas perhatiannya saya ucapkan terima kasih.

Mengetahui,
Dosen Pembimbing

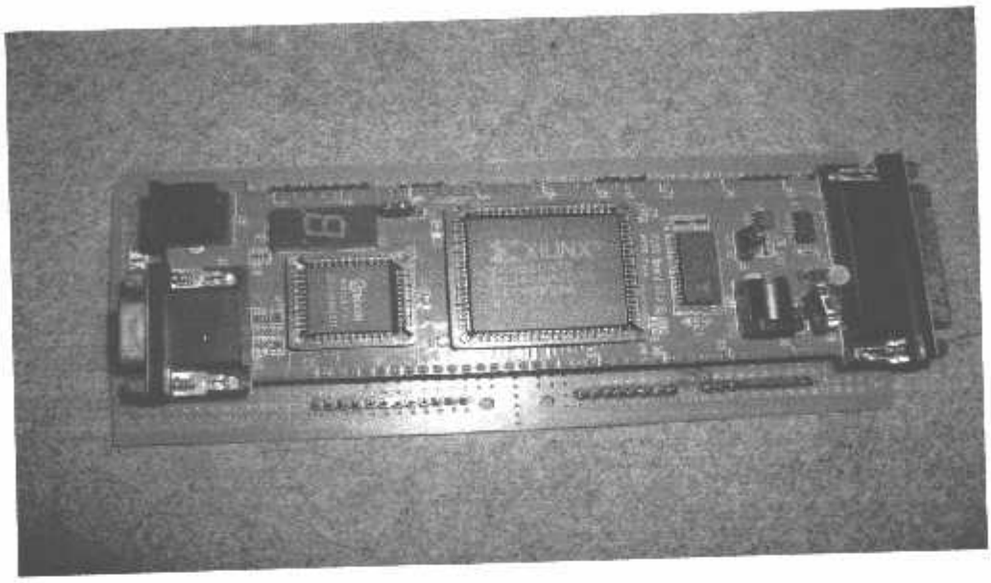
Ir.Widodo Pudji M,MT

Malang, Januari 2006
Pemohon,

Andrew Eka Yusuf
NIM 01.17.014

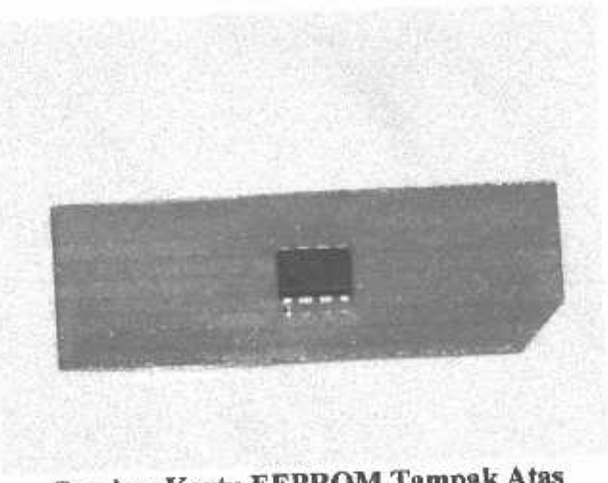
Mengetahui,
Kasie Lab.Elektronika Digital

Joseph Dedy Irawan,ST.MT

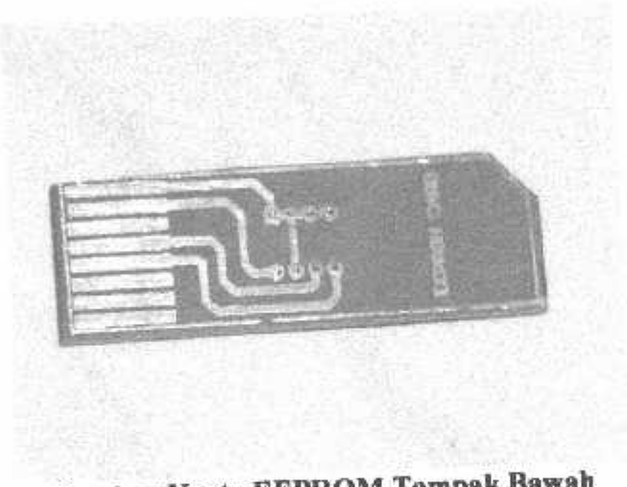


Gambar XS95 Board V1.3

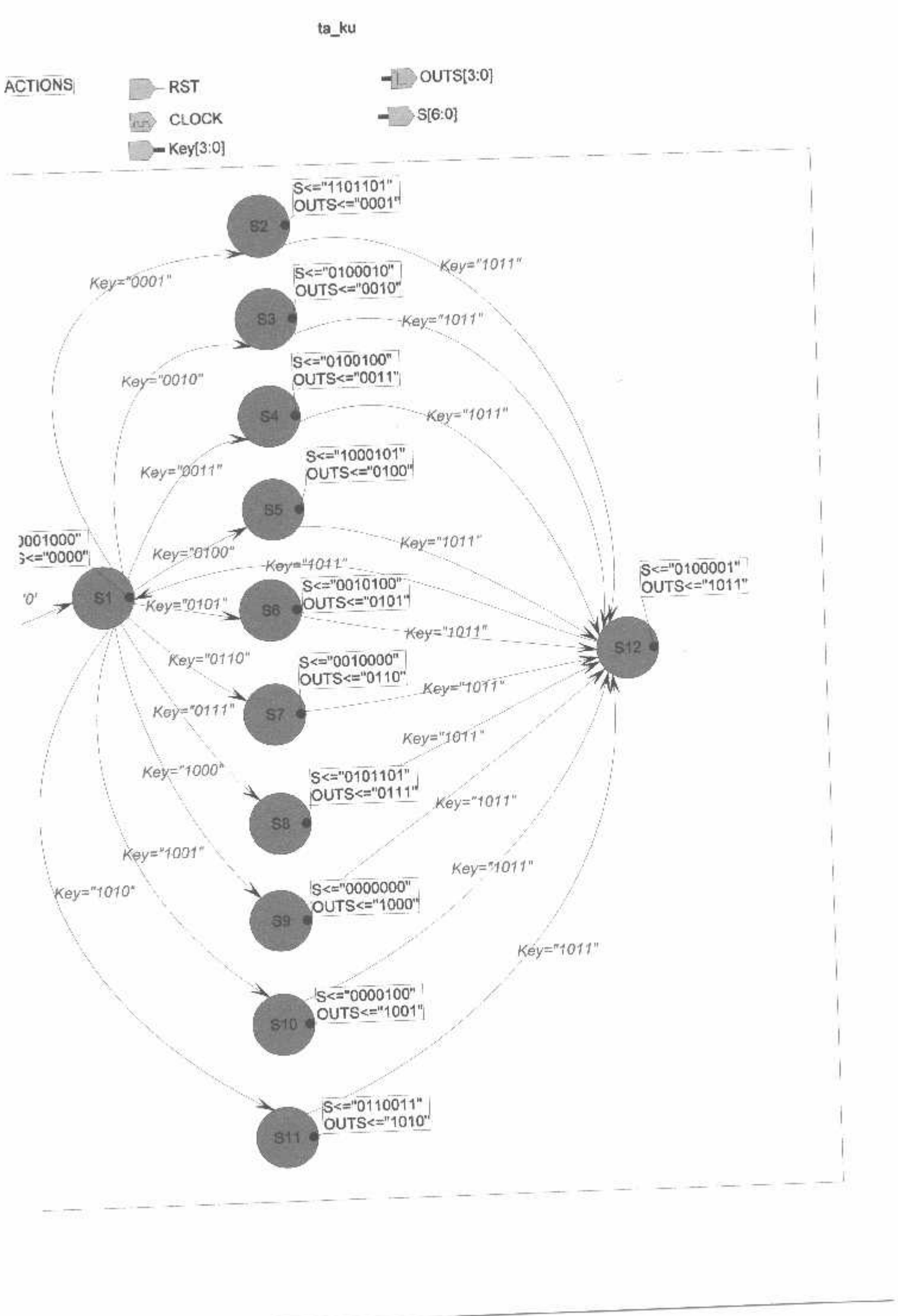
Gambar Alat Secara Keseluruhan



Gambar Kartu EEPROM Tampak Atas



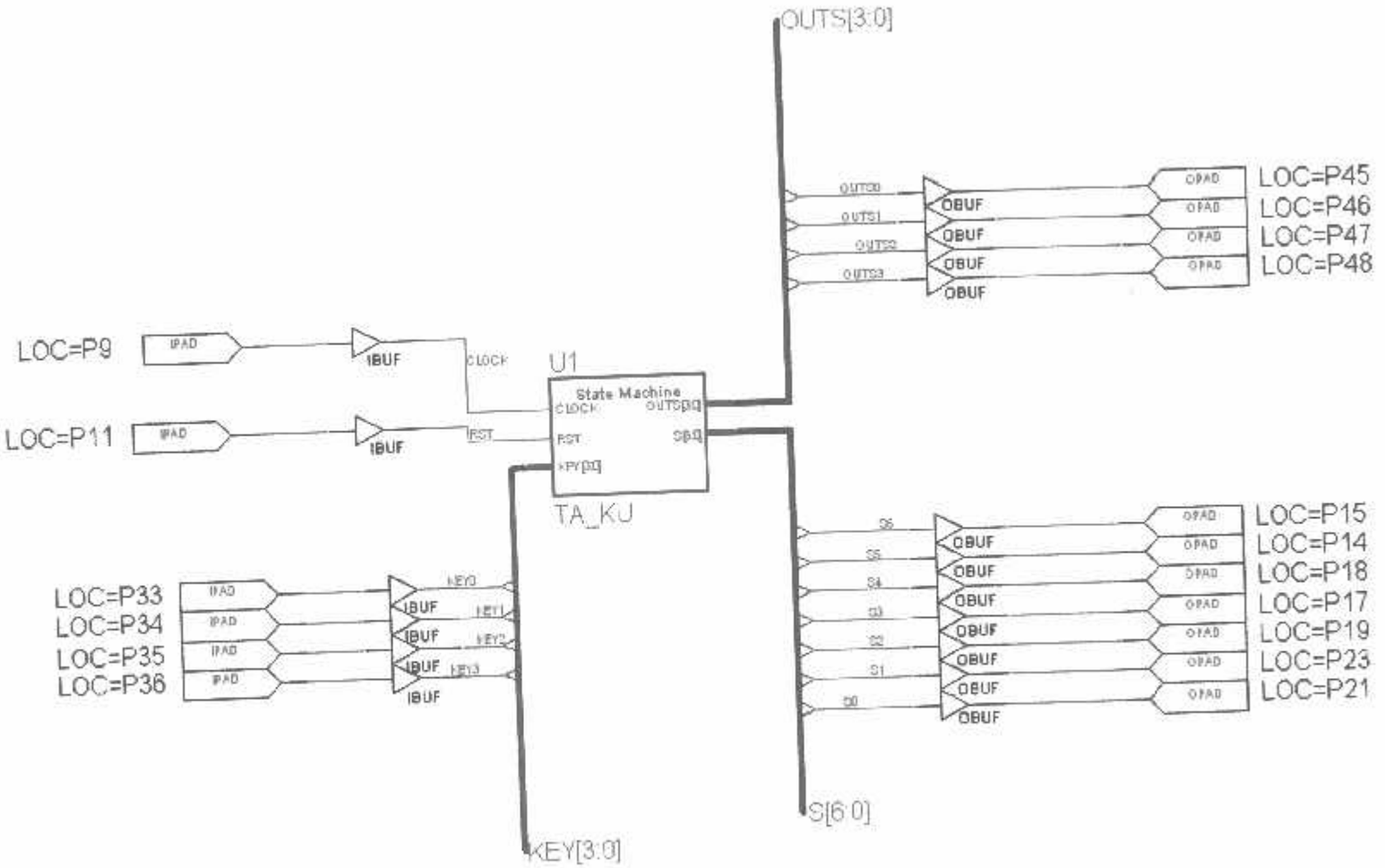
Gambar Kartu EEPROM Tampak Bawah


ta_ku
ACTIONS
RST
CLOCK
Key[3:0]
OUTS[3:0]
S[6:0]
S2
S<="1101101"
OUTS<="0001"
S3
S<="0100010"
OUTS<="0010"
S4
S<="0100100"
OUTS<="0011"
S5
S<="1000101"
OUTS<="0100"
S1
'0'
0001000"
S<="0000"
S6
S<="0010100"
OUTS<="0101"
S7
S<="0010000"
OUTS<="0110"
S8
S<="0101101"
OUTS<="0111"
S9
S<="0000000"
OUTS<="1000"
S10
S<="0000100"
OUTS<="1001"
S11
S<="0110011"
OUTS<="1010"
S12
S<="0100001"
OUTS<="1011"
Key="0001"
Key="0010"
Key="0011"
Key="0100"
Key="0101"
Key="0110"
Key="0111"
Key="1000"
Key="1001"
Key="1010"
Key="1011"

```
ile: D:\Fndtn\Active\Projects\yuli\ta_ku.vhd
eated: 03/17/06 15:38:45
om: 'D:\Fndtn\Active\Projects\yuli\ta_ku.ASF'
y fsm2hdl - version: 2.0.1.53

ıry IEEE;
IEEE.std_logic_1164.all;

IEEE.std_logic_arith.all;
IEEE.std_logic_unsigned.all;

ıry SYNOPSYS;
SYNOPSYS.attributes.all;

y ta_ku is
t (CLOCK: in STD_LOGIC;
Key: in STD_LOGIC_VECTOR (3 downto 0);
RST: in STD_LOGIC;
OUTS: out STD_LOGIC_VECTOR (3 downto 0);
S: out STD_LOGIC_VECTOR (6 downto 0));


itecture ta_ku_arch of ta_ku is


MBOLIC ENCODED state machine: Sreg0
Sreg0_type is (S1, S10, S11, S12, S2, S3, S4, S5, S6, S7, S8, S9);
al Sreg0: Sreg0_type;

n
ıcurrent signal assignments


0_machine: process (CLOCK)

n

OCK'event and CLOCK = '1' then
      if RST='0' then
                  Sreg0 <= S1;
                  OUTS<="0000";
      else
      case Sreg0 is
                  when S1 =>
                              OUTS<="0000";
                              if Key="0110" then
                                          Sreg0 <= S7;
                              elsif Key="0010" then
                                          Sreg0 <= S3;
                              elsif Key="0011" then
                                          Sreg0 <= S4;
                              elsif Key="0100" then
                                          Sreg0 <= S5;
                              elsif Key="0101" then
                                          Sreg0 <= S6;
                              elsif Key="0001" then
```

```
                    Sreg0 <= S2;
            elsif Key="0111" then
                    Sreg0 <= S8;
            elsif Key="1000" then
                    Sreg0 <= S9;
            elsif Key="1001" then
                    Sreg0 <= S10;
            elsif Key="1010" then
                    Sreg0 <= S11;
            end if;
when S10 =>
            OUTS<="1001";
            if Key="1011" then
                    Sreg0 <= S12;
            end if;
when S11 =>
            OUTS<="1010";
            if Key="1011" then
                    Sreg0 <= S12;
            end if;
when S12 =>
            OUTS<="1011";
            if Key="1011" then
                    Sreg0 <= S1;
            end if;
when S2 =>
            OUTS<="0001";
            if Key="1011" then
                    Sreg0 <= S12;
            end if;
when S3 =>
            OUTS<="0010";
            if Key="1011" then
                    Sreg0 <= S12;
            end if;
when S4 =>
            OUTS<="0011";
            if Key="1011" then
                    Sreg0 <= S12;
            end if;
when S5 =>
            OUTS<="0100";
            if Key="1011" then
                    Sreg0 <= S12;
            end if;
when S6 =>
            OUTS<="0101";
            if Key="1011" then
                    Sreg0 <= S12;
            end if;
when S7 =>
            OUTS<="0110";
            if Key="1011" then
                    Sreg0 <= S12;
            end if;
when S8 =>
            OUTS<="0111";
```

```
                    if Key="1011" then
                        Sreg0 <= S12;
                    end if;
                when S9 =>
                    OUTS<="1000";
                    if Key="1011" then
                        Sreg0 <= S12;
                    end if;
                when others =>
                    null;
        end case;
        end if;
if;
process;

inal assignment statements for combinatorial outputs
signment:
 "0000100" when (Sreg0 = S10) else
)110011" when (Sreg0 = S11) else
)100001" when (Sreg0 = S12) else
1101101" when (Sreg0 = S2) else
)100010" when (Sreg0 = S3) else
)100100" when (Sreg0 = S4) else
1000101" when (Sreg0 = S5) else
)010100" when (Sreg0 = S6) else
)010000" when (Sreg0 = S7) else
)101101" when (Sreg0 = S8) else
)000000" when (Sreg0 = S9) else
)001000";

ta_ku_arch;
```


OUTS[3:0]
LOC=P45
LOC=P46
LOC=P47
LOC=P48
OUTS0
OUTS1
OUTS2
OUTS3
OBUF
OPAD
LOC=P9
LOC=P11
IPAD
IBUF
CLOCK
RST
U1
State Machine
OUTS[3:0]
S[6:0]
KEY[3:0]
TA_KU
LOC=P33
LOC=P34
LOC=P35
LOC=P36
KEY0
KEY1
KEY2
KEY3
LOC=P15
LOC=P14
LOC=P18
LOC=P17
LOC=P19
LOC=P23
LOC=P21
S6
S5
S4
S3
S2
S1
S0

```
      BIT     P1.6
      BIT     P1.7
PA    BIT     P2.0

      BIT     P3.6
      BIT     P3.7

TUS   BIT     20H.0

ISAN  EQU     20
AH    EQU     -50000

S     EQU     30H
SI    EQU     R1
R     EQU     31H
R     EQU     32H
      EQU     33H
ANG   EQU     0DH
R     EQU     0EH

      ORG     00H
      LJMP    START

      ORG     100H
T:    CLR     POMPA
      MOV     TMOD,#01H
      call    Ldelay
      mov     A,#03Fh
      call    write_inst
      call    write_inst
      call    write_inst
      mov     A,#0Dh
      call    write_inst
      mov     A,#06h
      call    write_inst
      mov     A,#01h
      call    write_inst
      mov     A,#0Ch
      call    write_inst
      MOV     DPTR,#MENU1
      CALL    DISPLAY
      CALL    DISPLAY
      MOV     DPTR,#MENU3
      CALL    TAMPIL_ATAS
      CALL    TAMPIL_BAWAH
:     CALL    KEYPAD
      JB      STATUS,KEY1
      CJNE    A,#BINTANG,CEK1
      MOV     DPTR,#KREDIT
      CALL    TAMPIL_ATAS
      CALL    TAMPIL_BAWAH
      CALL    PANAH1
      MOV     POSISI,#1
      CALL    SCANMENU
      JB      STATUS,POM
      SJMP    KEY1
:     CJNE    A,#'1',CEK2
      MOV     DPTR,#MENU4
      CALL    TAMPIL_ATAS
      CALL    TAMPIL_BAWAH
      CALL    ISI_JUMLAH
      JB      STATUS,POM
      MOV     DPTR,#ISI
      CALL    TAMPIL_ATAS
      CALL    TAMPIL_BAWAH
      MOV     B,A             ;BACK UP DATA LITER
:     SETB    POMPA
      CALL    SELITER
```

WR setb

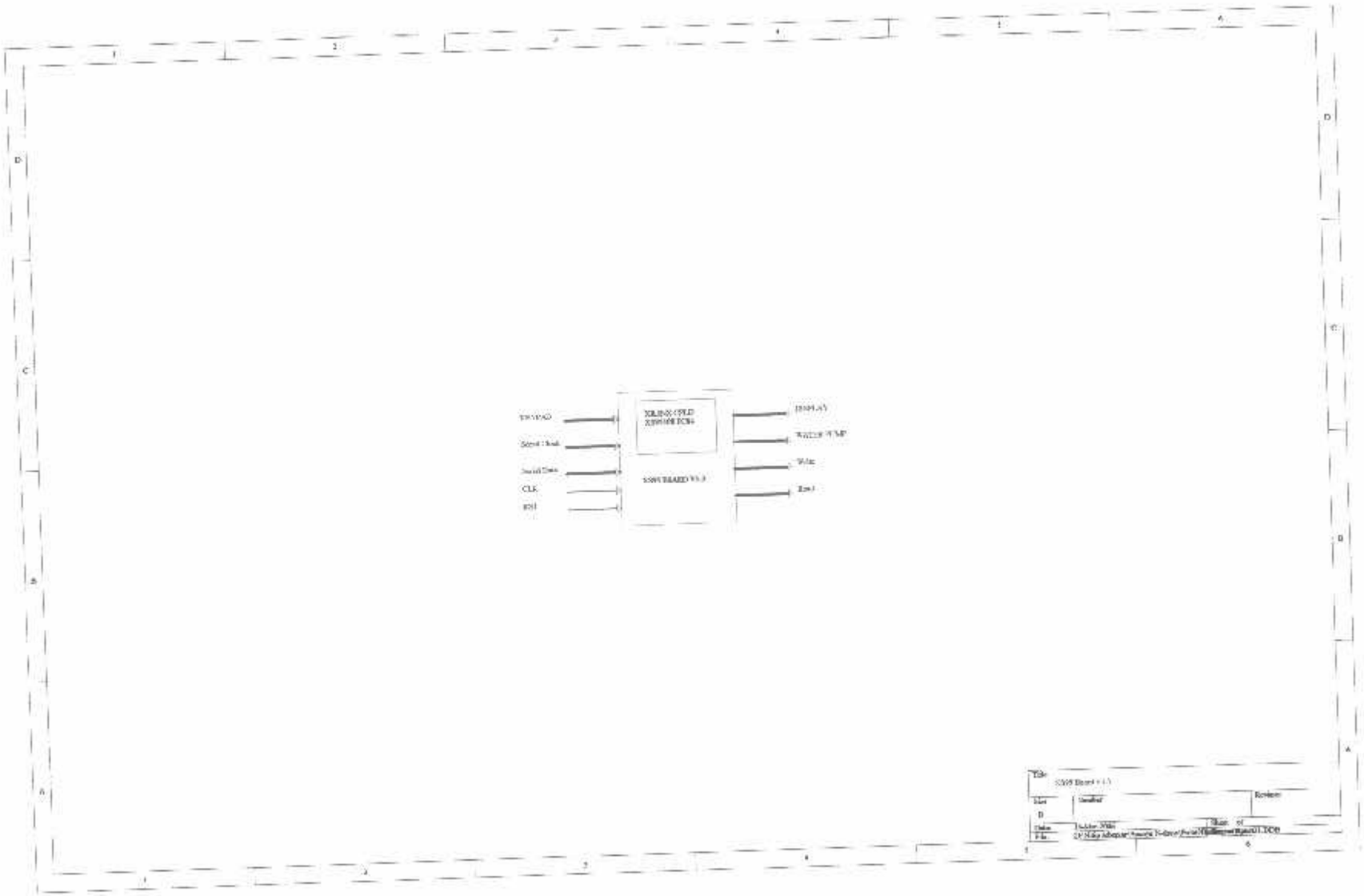
```
        DJNZ    LITER,LOP2
        CLR     POMPA
        MOV     DPTR,#THANKS
        CALL    DISPLAY
        SJMP    POM
2:      CJNE    A,#'2',CEK3
        MOV     DPTR,#MENU5
        CALL    TAMPIL_ATAS
        CALL    TAMPIL_BAWAH
        CALL    ISI_JUMLAH
        JB      STATUS,POM
        MOV     DPTR,#ISI
        CALL    TAMPIL_ATAS
        CALL    TAMPIL_BAWAH
        MOV     B,A             ;BACK UP DATA LITER
1:      SETB    POMPA
        CALL    SELITER
        DJNZ    LITER,LOP1
        CLR     POMPA
        MOV     DPTR,#THANKS
        CALL    DISPLAY
        JMP     POM
3:      CJNE    A,#BINTANG,KEY1
        JMP     POM

IMENU:
        CALL    KEYPAD
        JB      STATUS,SCANMENU
        CJNE    A,#'1',DT2
        CALL    PANAH1
        MOV     POSISI,#1
        CJNE    A,#'2',CEK_ENT
        CALL    PANAH2
        MOV     POSISI,#2
_ENT:CJNE       A,#PAGAR,GGL
        CLR     STATUS
        MOV     A,POSISI
        CJNE    A,#1,POS2
        CALL    BACA_I2C
        MOV     R0,#LAMA
        MOV     A,#80H
        CALL    WRITE_INST
        MOV     A,@R0
        CALL    WRITE_DATA
        INC     R0
        CJNE    R0,#LAMA+4,LLL
        RET
  :     CJNE    A,#2,GOUT
        MOV     DPTR,#0
        CALL    INISIAL_I2C
        MOV     DPTR,#0
        CALL    INISIAL_I2C
        MOV     A,#'4'
        CALL    WRITE_I2C
        MOV     A,#'5'
        CALL    WRITE_I2C
        MOV     A,#'0'
        CALL    WRITE_I2C
        MOV     A,#'0'
        CALL    WRITE_I2C
        CALL    STOP_I2C
  :     RET
        CJNE    A,#BINTANG,SCANMENU
        SETB    STATUS
        RET

JUMLAH:
```

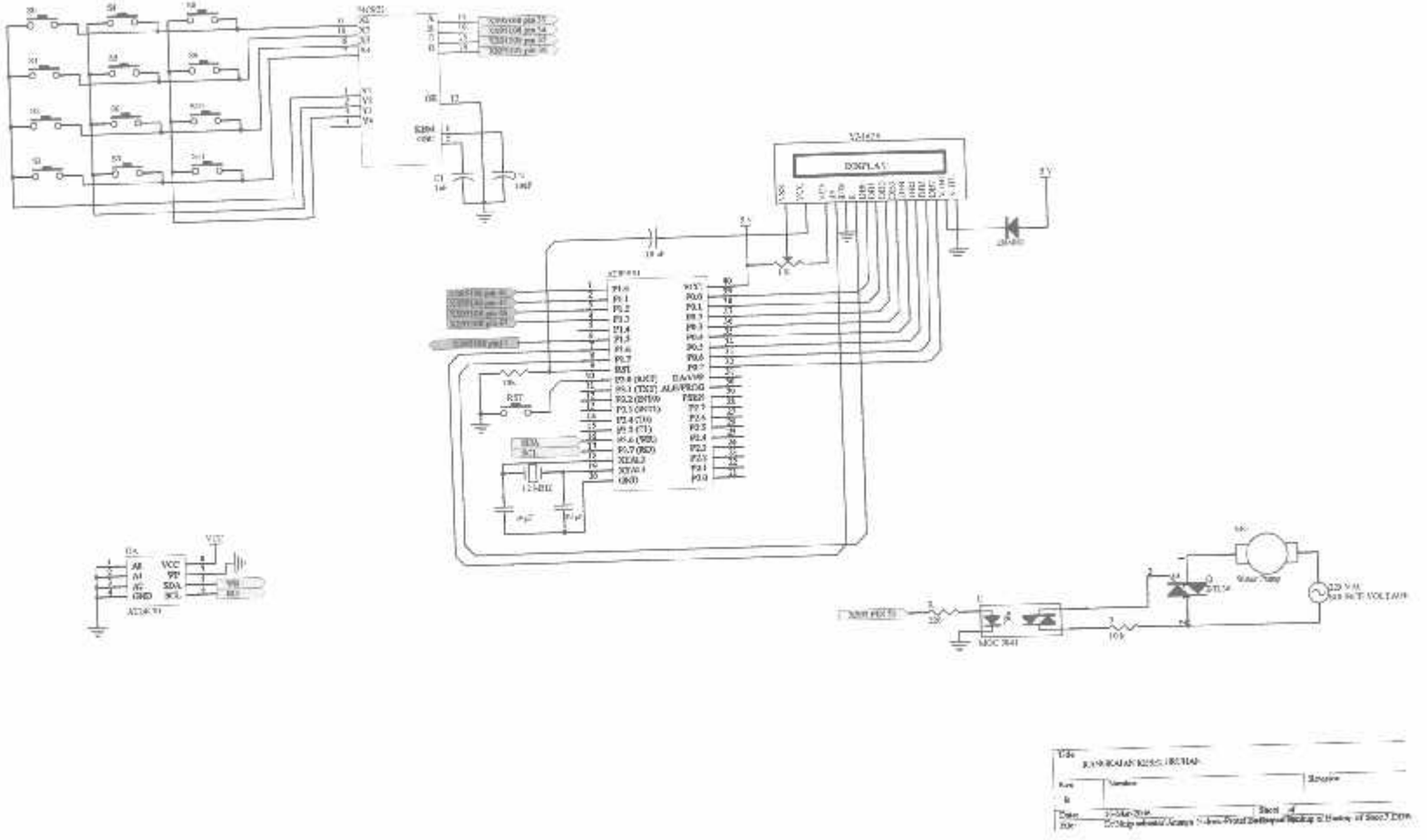
```
      MOV     A,#0C9H
      CALL    WRITE_INST
?:    CALL    KEYPAD
      JB      STATUS,KEY2
      CJNE    A,#BINTANG,CEK4
      SETB    STATUS
      RET
4:    CJNE    A,#PAGAR,CEK5
      CLR     STATUS
      RET
5:    CJNE    A,#'0',NORMAL
      JMP     KEY2
NAL:  CALL    WRITE_DATA
      ANL     A,#0FH
      MOV     LITER,A
      JMP     ISI_JUMLAH

H1:   MOV     A,#8FH
      CALL    WRITE_INST
      MOV     A,#7FH
      CALL    WRITE_DATA
      MOV     A,#0CFH
      CALL    WRITE_INST
      MOV     A,#' '
      CALL    WRITE_DATA
      RET

H2:   MOV     A,#0CFH
      CALL    WRITE_INST
      MOV     A,#7FH
      CALL    WRITE_DATA
      MOV     A,#8FH
      CALL    WRITE_INST
      MOV     A,#' '
      CALL    WRITE_DATA
      RET

AD:   SETB    STATUS
      JNB     P1.4,OUTK
      MOV     A,P1
      ANL     A,#0FH
      MOV     DPTR,#SCANKEY
      MOVC    A,@A+DPTR
      CLR     STATUS
      JB      P1.4,$
:     RET

TAL_I2C:
      CALL    START_I2C
      MOV     A,#10100000B
      CALL    WRITE_I2C
      MOV     A,DPL
      CALL    WRITE_I2C
      RET

_I2C:
      CALL    START_I2C
      MOV     A,#10100000B
      CALL    WRITE_I2C
      MOV     DPTR,#0000H
      MOV     A,DPH
      CALL    WRITE_I2C
      CALL    START_I2C
      MOV     A,#10100001B
      CALL    WRITE_I2C
      MOV     R0,#LAMA
N:    CALL    READ_I2C
      MOV     @R0,A
```

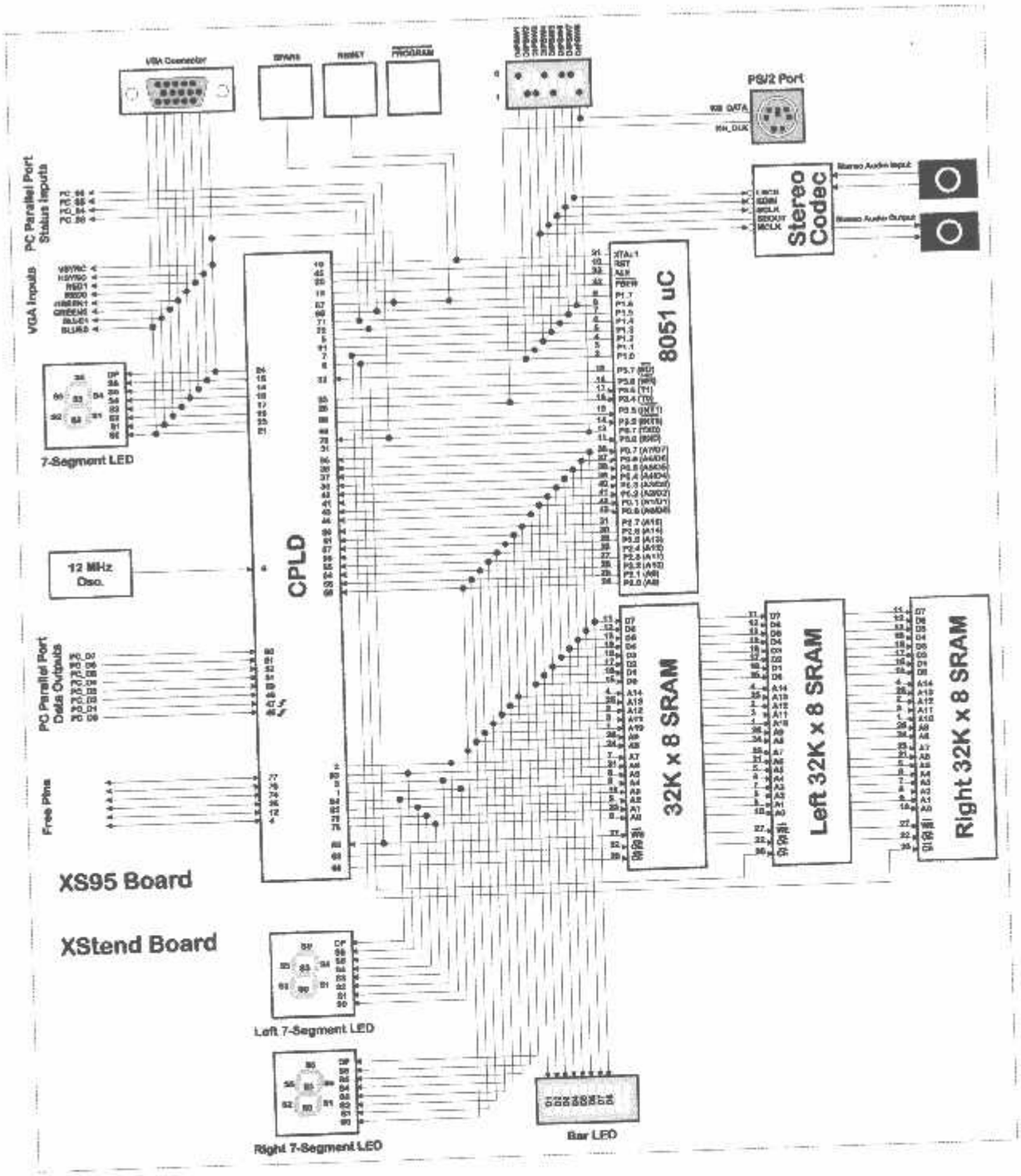
```
    INC     R0
    CJNE    R0,#LAMA+4,CEKIN
    CALL    NACK
    CALL    STOP_I2C
    RET


T_I2C:
    SETB    SDA
    SETB    SCL
    CALL    ROM_DELAY
    CLR     SDA
    CLR     SCL
    CALL    ROM_DELAY
    RET

_I2C:
    CLR     SDA
    SETB    SCL
    CALL    ROM_DELAY
    SETB    SDA
    CALL    ROM_DELAY
    CLR     SCL
    RET

E_I2C:
    MOV     B,A
    MOV     TULIS,#8
:   RLC     A
    MOV     SDA,C
    CALL    ROM_DELAY
    SETB    SCL
    CLR     SCL
    DJNZ    TULIS,OUTC
    SETB    SDA
    NOP
    SETB    SCL
    NOP
    NOP
    MOV     C,SDA
    CLR     SCL
    MOV     A,B
    RET

 _I2C:
    MOV     TULIS,#8
    SETB    SDA
    CALL    ROM_DELAY
    SETB    SCL
    NOP
    NOP
    MOV     C,SDA
    RLC     A
    CLR     SCL
    DJNZ    TULIS,IN
    CALL    ACK
    RET

    CLR     SDA
    CALL    ROM_DELAY
    SETB    SCL
    CLR     SCL
    RET

:   SETB    SDA
    CALL    ROM_DELAY
    SETB    SCL
    CLR     SCL
```

```
      RET

'IL_ATAS:
      MOV     TULIS,#16
      MOV     A,#80H
      CALL    WRITE_INST
'1:   CLR     A
      MOVC    A,@A+DPTR
      CALL    WRITE_DATA
      CALL    TDELAY
      INC     DPTR
      DJNZ    TULIS,LOOP1
      RET

'IL_BAWAH:
      MOV     TULIS,#16
      MOV     A,#0C0H
      CALL    WRITE_INST
      JMP     LOOP1

'LAY: CALL    TAMPIL_ATAS
      CALL    TAMPIL_BAWAH
      CALL    LDELAY
      RET

AY:   DJNZ    R7,$
      RET

DELAY:
      MOV     R7,#200
      DJNZ    R7,$
      RET

TER:  MOV     R7,#3
NE:   CALL    TUNDA
      DJNZ    R7,ENTENE
      RET

A:    MOV     TIMER,#RATUSAN
:     MOV     TH0,#HIGH CACAH
      MOV     TL0,#LOW CACAH
      SETB    TR0
GU:   JNB     TF0,TUNGGU
      CLR     TF0
      CLR     TR0
      DJNZ    TIMER,LAGI
      RET

AY:   MOV     R5,#25
      DJNZ R7,$
      DJNZ    R6,DEL
      DJNZ    R5,DEL
      RET

1:    DB      'N-DREW (0117014)'
      DB      '   ITN MALANG   '

2:    DB      '  SKRIPSI 2006  '
      DB      '   ITN MALANG   '

3:    DB      '1[Pre]    2[Sol]'
      DB      '*[Menu] #[Enter]'

4:    DB      'Masukkan Liter. '
      DB      'PREMIUM:   Liter'

5:    DB      'Masukkan Liter. '
      DB      'SOLAR  :   Liter'
```

```
)IT: DB       'CEK SALDO       '
     DB       'REFILL KREDIT   '

:    DB       'PENGISIAN SEDANG'
     DB       '  BERLANGSUNG   '

IKS: DB       'PROSES PENGISIAN'
     DB       'SELESAI........'

IKEY:       DB
'','2','3',0AH,'4','5','6',0BH,'7','8','9',0CH,BINTANG,'0',PAGAR,0FH

++++++++  menulis instruksi ke lcd
:e_inst:
     CLR     RS
     mov     P0,a
     setb    EN
     clr     EN
     MOV     R6,#10
'1:         DJNZ R7,$
     DJNZ    R6,WAIT1
     ret
++++++++  menulis data ke lcd
:e_data:
     SETB    RS
     mov     P0,a
     setb    EN
     clr     EN
    MOV      R6,#10
'2:         DJNZ R7,$
     DJNZ    R6,WAIT2
     ret
     end
```







• **Figure 6**: Programmer's model of the XS95/XStend Board combination.

• **Table 5:** Connections between the XS95 Board and the XStend Board resources.

XS95 Pins (J2)	Power/ GND	DIP Switch	Push-buttons	LEDs	VGA Interface	PS/2 Interface	RAMs	Stereo Codec	8051 Uc	PC Parallel Port	Oscillator	Function	UW-FPGA BOARD Pin
1				LSB0			A4					Left LED segment; RAM address line	P35
2				LSB1			A7					Left LED segment; RAM address line	P36
3				LSB2			A5					Left LED segment; RAM address line	P29
4								SDOUT	P1.3			Uncommitted XS95 I/O pin	
5		DIPSW4										DIP switch; codec serial data output; uC I/O	P24
6		DIPSW1					LCEB		P1.0			DIP switch; left RAM chip-enable; uC I/O port	P19
7		DIPSW2					RCEB		P1.1			DIP switch; right RAM chip-enable; uC I/O port	P20
9											CLK	XS Board oscillator	
10			RESET3						XTAL1			Pushbutton; uC clock	P56
11		DIPSW3						MCLK	P1.2			DIP switch; codec master clock; uC I/O port	P23
12												Uncommitted XS95 I/O pin	
13									PSENB			uC program store-enable	
14				S5	RED1							XS Board LED segment; VGA color signal	
15				S6	HSYNC0							XS Board LED segment; VGA horiz. sync.	
17				S3	GREEN1							XS Board LED segment; VGA color signal	
18				S4	RED0							XS Board LED segment; VGA color signal	
19				S2	GREEN0							XS Board LED segment; VGA color signal	
20									ALEB			uC address-latch-enable	
21				S0	BLUE0							XS Board LED segment; VGA color signal	
23				S1	BLUE1							XS Board LED segment; VGA color signal	
25						KB_CLK			P3.4 (T0)			Uncommitted XS95 I/O pin	
26												PS/2 keyboard clock; uC I/O port	
28												JTAG TDI; DIN	
29												JTAG TMS	
30									P3.0 (RXD)			JTAG TCK; CCLK	
31									P3.7 (RD_)			uC I/O port	
32									P3.5 (T1)			uC I/O port	
33									P2.7			uC I/O port	
34				RDPB					P0.7			Right LED decimal-point; RAM address line; uC I/O port	P41
35				DB8			D7		P0.6			LED; RAM data line; uC muxed address/data line	P61
36				DB7			D6		P0.5			LED; RAM data line; uC muxed address/data line	P62
37				DB6			D5		P0.4			LED; RAM data line; uC muxed address/data line	P65
39				DB5			D4		P0.3			LED; RAM data line; uC muxed address/data line	P66
40				DB4			D3		P0.2			LED; RAM data line; uC muxed address/data line	P57
41				DB3			D2		P0.1			LED; RAM data line; uC muxed address/data line	P58
43				DB2			D1		P0.0			LED; RAM data line; uC muxed address/data line	P59
44				DB1			D0		RST			LED; RAM data line; uC muxed address/data line	P60
45								CCLK		PC_D0		uC reset	
46								CDIN		PC_D1		Codec control line; PC parallel port data output	
47								CSB		PC_D2		Codec control line; PC parallel port data output	
48												Codec control line; PC parallel port data output	
49	GND									PC_D3		Power supply ground	
50										PC_D4		PC parallel port data output	
51										PC_D5		PC parallel port data output	
52												PC parallel port data output	
53				RSB4			A12		P2.4			Right LED segment; RAM address line; uC I/O port	P48
54				RSB2			A10		P2.2			Right LED segment; RAM address line; uC I/O port	P45
55				RSB3			A11		P2.3			Right LED segment; RAM address line; uC I/O port	P51
56				RSB1			A9		P2.1			Right LED segment; RAM address line; uC I/O port	P47
57				RSB5			A13		P2.5			Right LED segment; RAM address line; uC I/O port	P50
58				RSB0			A8		P2.0			Right LED segment; RAM address line; uC I/O port	P46
59												JTAG TDO; DOUT	
61				RSB6			A14		P2.6			Right LED segment; RAM address line; uC I/O port	P49
62							OEB					RAM output-enable	
63							WEB		P3.6 (WR_)			RAM write-enable; uC I/O port	
65							CEB					XS Board RAM chip-enable	
66								LRCK	P1.6	PC_S5		DIP switch; codec left-right channel select; uC I/O port; PC	P27
68		DIPSW7							P3.3 (INT1_)			uC I/O port	
69									P3.2 (INT0_)			uC I/O port	
70		DIPSW8					KB_DATA		P3.1 (TX	PC_S6		DIP switch; PS/2 keyboard serial data; uC I/O port; PC par	P28
71		DIPSW6						SDIN	P1.5	PC_S3		DIP switch; codec serial input data; uC I/O port; PC parall	P26
72		DIPSW5						SCLK	P1.4	PC_S4		DIP switch; codec serial clock; uC I/O port; PC parallel por	P25
74												Uncommitted XS95 I/O pin	
75				LSB3			A0					Left LED segment; RAM address line	P44
76												Uncommitted XS95 I/O pin	
77												Uncommitted XS95 I/O pin	
78	+5V											+5V power source	
79				LSB4			A1					Left LED segment; RAM address line	P38
80										PC_D7		PC parallel port data output	
81										PC_D6		PC parallel port data output	
82				LSB5			A2					Left LED segment; RAM address line	P40
83				LSB6			A6					Left LED segment; RAM address line	P39
84				LDP6			A3					Left LED segment; RAM address line	P37
24,67			SPAREEDP		VSYNC0				P1.7			Left LED decimal-point; RAM address line	P18
												Pushbutton; XS Board LED decimal-point; VGA horiz. sync	

XC95108 In-System Programmable CPLD

ember 4, 1998 (Version 3.0)

Product Specification

atures

.5 ns pin-to-pin logic delays on all pins
CNT to 125 MHz
08 macrocells with 2400 usable gates
lp to 108 user I/O pins
V in-system programmable (ISP)
  Endurance of 10,000 program/erase cycles
  Program/erase over full commercial voltage and temperature range
nhanced pin-locking architecture
lexible 36V18 Function Block
  90 product terms drive any or all of 18 macrocells within Function Block
  Global and product term clocks, output enables, set and reset signals
xtensive IEEE Std 1149.1 boundary-scan (JTAG) upport
rogrammable power reduction mode in each acrocell
lew rate control on individual outputs
ser programmable ground pin capability
xtended pattern security features for design protection
igh-drive 24 mA outputs
.3 V or 5 V I/O capability
dvanced CMOS 5V FastFLASH technology
upports parallel programming of more than one C9500 concurrently
vailable in 84-pin PLCC, 100-pin PQFP, 100-pin TQFP nd 160-pin PQFP packages

scription

XC95108 is a high-performance CPLD providing nced in-system programming and test capabilities for ral purpose logic integration. It is comprised of six 18 Function Blocks, providing 2,400 usable gates with agation delays of 7.5 ns. See Figure 2 for the architec- overview.

Power Management

Power dissipation can be reduced in the XC95108 by configuring macrocells to standard or low-power modes of operation. Unused macrocells are turned off to minimize power dissipation.

Operating current for each design can be approximated for specific operating conditions using the following equation:

I_{CC} (mA) =

MC_{HP} (1.7) + MC_{LP} (0.9) + MC (0.006 mA/MHz) f

Where:

MC_{HP} = Macrocells in high-performance mode

MC_{LP} = Macrocells in low-power mode

MC = Total number of macrocells used

f = Clock frequency (MHz)

Figure 1 shows a typical calculation for the XC95108 device.

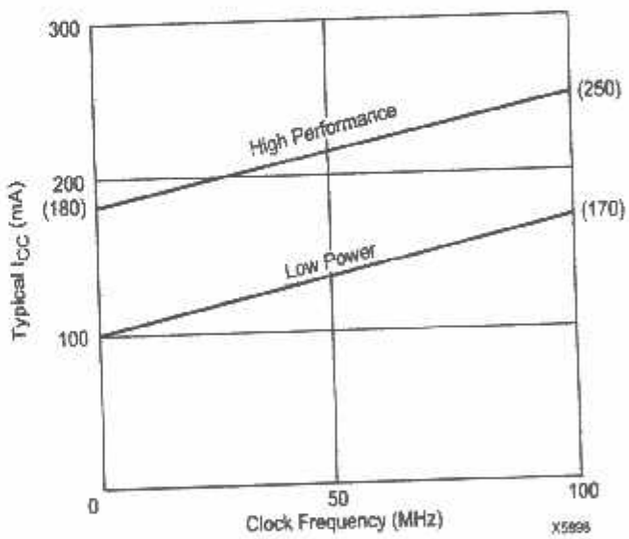
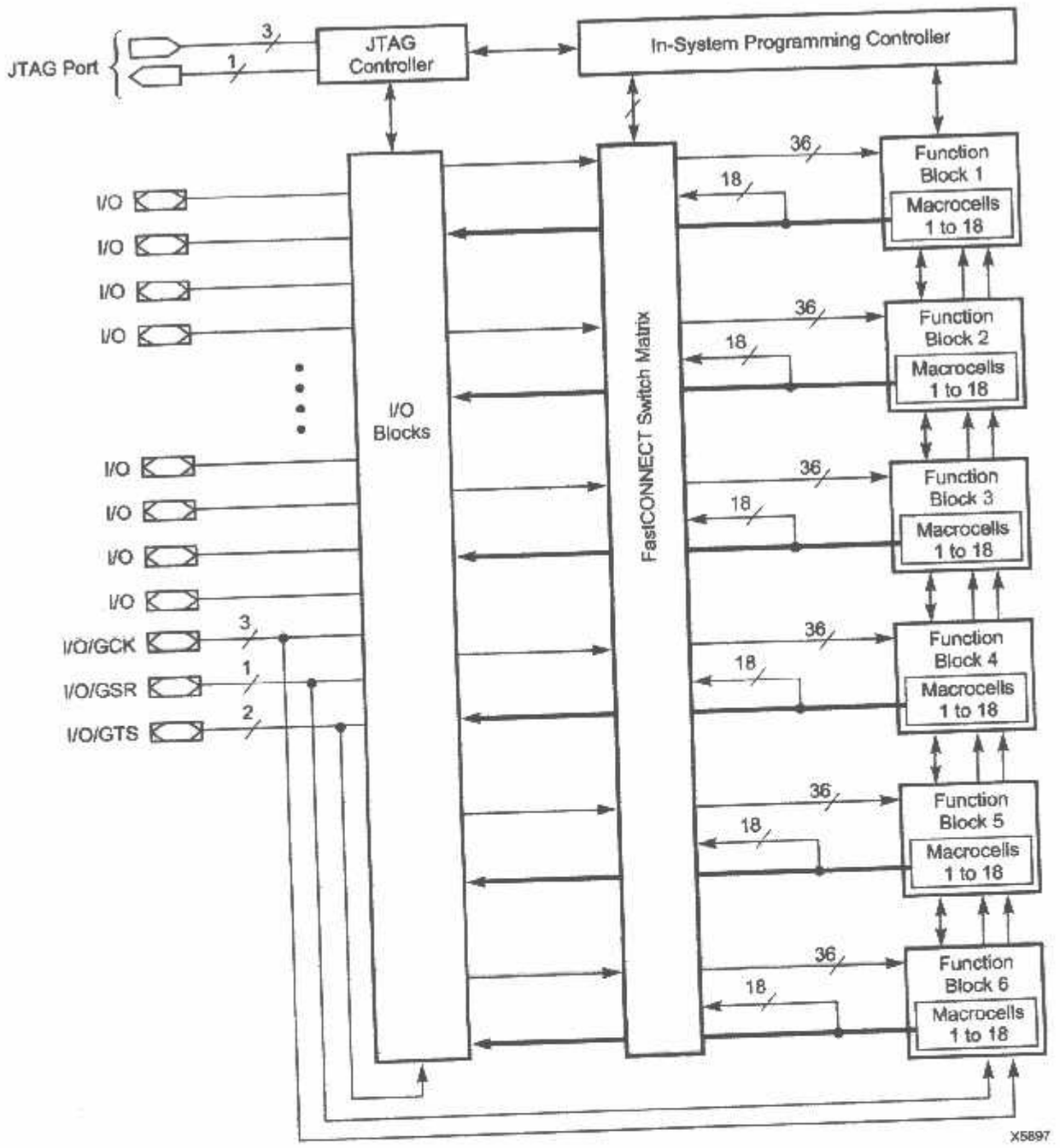


Figure 1: Typical I_{CC} vs. Frequency for XC95108



ıre 2: XC95108 Architecture

Note: Function Block outputs (indicated by the bold line) drive the I/O Blocks directly

ısolute Maximum Ratings

Symbol	Parameter	Value	Units
;	Supply voltage relative to GND	-0.5 to 7.0	V
	DC input voltage relative to GND	-0.5 to V_{CC} + 0.5	V
	Voltage applied to 3-state output with respect to GND	-0.5 to V_{CC} + 0.5	V
	Storage temperature	-65 to +150	°C
'G	Max soldering temperature (10 s @ 1/16 in = 1.5 mm)	+260	°C
)L			

ning: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, and functional oporation of the device at these or any other conditions beyond those listed under Recommended Operating Conditions is not implied. Exposure to Absolute Maximum Rating conditions for extended periods of time may affect device reliability.

commended Operation Conditions'

ymbol	Parameter	Min	Max	Units
:INT	Supply voltage for internal logic and input buffer	4.75 (4.5)	5.25 (5.5)	V
:IO	Supply voltage for output drivers for 5 V operation	4.75 (4.5)	5.25 (5.5)	V
	Supply voltage for output drivers for 3.3 V operation	3.0	3.6	V
	Low-level input voltage	0	0.80	V
	High-level input voltage	2.0	V_{CCINT} +0.5	V
	Output voltage	0	V_{CCIO}	V

): 1. Numbers in parenthesis are for industrial-temperature range versions.

durance Characteristics

ymbol	Parameter	Min	Max	Units
	Data Retention	20	-	Years
	Program/Erase Cycles	10,000	-	Cycles

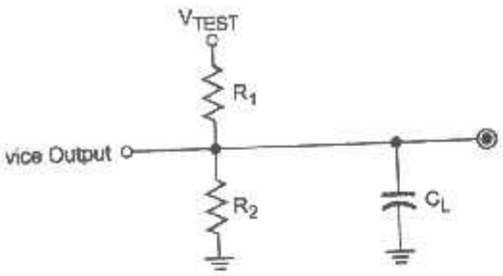
; Characteristics Over Recommended Operating Conditions

ymbol	Parameter	Test Conditions	Min	Max	Units
H	Output high voltage for 5 V operation	I_{OH} = -4.0 mA V_{CC} = Min	2.4		V
	Output high voltage for 3.3 V operation	I_{OH} = -3.2 mA V_{CC} = Min	2.4		V
	Output low voltage for 5 V operation	I_{OL} = 24 mA V_{CC} = Min		0.5	V
	Output low voltage for 3.3 V operation	I_{OL} = 10 mA V_{CC} = Min		0.4	V
	Input leakage current	V_{CC} = Max V_{IN} = GND or V_{CC}		±10.0	µA
	I/O high-Z leakage current	V_{CC} = Max V_{IN} = GND or V_{CC}		±10.0	µA
	I/O capacitance	V_{IN} = GND f = 1.0 MHz		10.0	pF
	Operating Supply Current (low power mode, active)	V_I = GND, No load f = 1.0 MHz	100 (Typ)		ma

; Characteristics

mbol	Parameter	XC95108-7		XC95108-10		XC95108-15		XC95108-20		Units
		Min	Max	Min	Max	Min	Max	Min	Max	
	I/O to output valid		7.5		10.0		15.0		20.0	ns
	I/O setup time before GCK	4.5		6.0		8.0		10.0		ns
	I/O hold time after GCK	0.0		0.0		0.0		0.0		ns
	GCK to output valid		4.5		6.0		8.0		10.0	ns
[1]	16-bit counter frequency	125.0		111.1		95.2		83.3		MHz
STEM [2]	Multiple FB internal operating frequency	83.3		66.7		55.6		50.0		MHz
J	I/O setup time before p-term clock input	0.5		2.0		4.0		4.0		ns
	I/O hold time after p-term clock input	4.0		4.0		4.0		6.0		ns
D	P-term clock to output valid		8.5		10.0		12.0		16.0	ns
	GTS to output valid		5.5		6.0		11.0		16.0	ns
	GTS to output disable		5.5		6.0		11.0		16.0	ns
E	Product term OE to output enabled		9.5		10.0		14.0		18.0	ns
D	Product term OE to output disabled		9.5		10.0		14.0		18.0	ns
H	GCK pulse width (High or Low)	4.0		4.5		5.5		5.5		ns

s: 1. f_{CNT} is the fastest 16-bit counter frequency available, using the local feedback when applicable.
f_{CNT} is also the Export Control Maximum flip-flop toggle rate, f_{TOG}.
2. f_{SYSTEM} is the internal operating frequency for general purpose system designs spanning multiple FBs.



Output Type	V_{CCIO}	V_{TEST}	R_1	R_2	C_L
	5.0 V	5.0 V	160 Ω	120 Ω	35 pF
	3.3 V	3.3 V	260 Ω	360 Ω	35 pF

X5906

ure 3: AC Load Circuit

ernal Timing Parameters

rmbol	Parameter	XC95108-7		XC95108-10		XC95108-15		XC95108-20		Units
		Min	Max	Min	Max	Min	Max	Min	Max	
fer Delays										
	Input buffer delay		2.5		3.5		4.5		6.5	ns
K	GCK buffer delay		1.5		2.5		3.0		3.0	ns
R	GSR buffer delay		4.5		6.0		7.5		9.5	ns
S	GTS buffer delay		5.5		6.0		11.0		16.0	ns
T	Output buffer delay		2.5		3.0		4.5		6.5	ns
	Output buffer enable/disable delay		0.0		0.0		0.0		0.0	ns
duct Term Control Delays										
CK	Product term clock delay		3.0		3.0		2.5		2.5	ns
SR	Product term set/reset delay		2.0		2.5		3.0		3.0	ns
TS	Product term 3-state delay		4.5		3.5		5.0		5.0	ns
rnal Register and Combinatorial delays										
	Combinatorial logic propagation delay		0.5		1.0		3.0		4.0	ns
	Register setup time	1.5		2.5		3.5		3.5		ns
	Register hold time	3.0		3.5		4.5		6.5		ns
	Register clock to output valid time		0.5		0.5		0.5		0.5	ns
	Register async. S/R to output delay		6.5		7.0		8.0		8.0	ns
	Register async. S/R recovery before clock	7.5		10.0		10.0		10.0		ns
	Internal logic delay		2.0		2.5		3.0		3.0	ns
SI	Internal low power logic delay		10.0		11.0		11.5		11.5	ns
SILP										
dback Delays										
	FastCONNECT matrix feedback delay		8.0		9.5		11.0		13.0	ns
	Function Block local feeback delay		4.0		3.5		3.5		5.0	ns
e Adders										
V^3	Incremental Product Term Allocator delay		1.0		1.0		1.0		1.5	ns
SW	Slew-rate limited delay		4.0		4.5		5.0		5.5	ns

e: 3. t_{PTA} is multiplied by the span of the function as defined in the family data sheet.

)5108 I/O Pins

tion ck	Macrocell	PC84	PQ100	TQ100	PQ160	BScan Order	Notes
	1	–	–	–	25	321	
	2	1	15	13	21	318	
	3	2	16	14	22	315	
	4	–	21	19	29	312	
	5	3	17	15	23	309	
	6	4	18	16	24	306	
	7	–	–	–	27	303	
	8	5	19	17	26	300	
	9	6	20	18	28	297	
	10	–	26	24	36	294	
	11	7	22	20	30	291	
	12	9	24	22	33	288	[1]
	13	–	–	–	34	285	
	14	10	25	23	35	282	[1]
	15	11	27	25	37	279	
	16	12	28	27	42	276	[1]
	17	13	30	28	44	273	
	18	–	–	–	43	270	
	1	–	–	–	153	267	
	2	71	98	96	154	264	
	3	72	99	97	156	261	
	4	–	4	2	4	258	
	5	74	1	99	159	255	[1]
	6	75	3	1	2	252	
	7	–	–	–	3	249	
	8	76	5	3	6	246	[1]
	9	77	6	4	8	243	[1]
	10	–	9	7	12	240	
	11	79	8	6	11	237	
	12	80	10	8	13	234	
	13	–	–	–	14	231	
	14	81	11	9	15	228	
	15	82	12	10	17	225	
	16	83	13	11	18	222	
	17	84	14	12	19	219	
	18	–	–	–	16	216	

Function Block	Macrocell	PC84	PQ100	TQ100	PQ160	BScan Order	Notes
3	1	–	–	–	45	213	
3	2	14	31	29	47	210	
3	3	15	32	30	49	207	
3	4	–	36	34	57	204	
3	5	17	34	32	54	201	
3	6	18	35	33	56	198	
3	7	–	–	–	50	195	
3	8	19	37	35	58	192	
3	9	20	38	36	59	189	
3	10	–	45	43	69	186	
3	11	21	39	37	60	183	
3	12	23	41	39	62	180	
3	13	–	–	–	52	177	
3	14	24	42	40	63	174	
3	15	25	43	41	64	171	
3	16	28	44	42	66	168	
3	17	31	51	49	77	165	
3	18	–	–	–	74	162	
4	1	–	–	–	123	159	
4	2	57	83	81	134	156	
4	3	58	84	82	135	153	
4	4	–	82	80	136	150	
4	5	61	87	85	138	147	
4	6	62	88	86	139	144	
4	7	–	–	–	128	141	
4	8	63	89	87	140	138	
4	9	65	91	89	142	135	
4	10	–	–	–	147	132	
4	11	66	92	90	143	129	
4	12	67	93	91	144	126	
4	13	–	–	–	153	123	
4	14	68	95	93	146	120	
4	15	69	96	94	148	117	
4	16	–	94	92	145	114	
4	17	70	97	95	152	111	
4	18	–	–	–	155	108	

s: (1) Global control pin

5108 I/O Pins (continued)

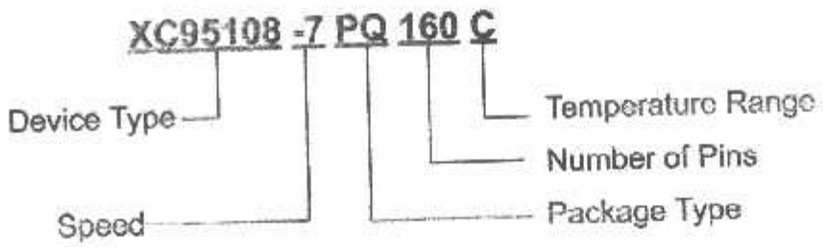
tion ck	Macrocell	PC84	PQ100	TQ100	PQ160	BScan Order	Notes
	1	–	–	–	76	105	
	2	32	52	50	79	102	
	3	33	54	52	82	99	
	4	–	48	46	72	96	
	5	34	55	53	86	93	
	6	35	56	54	88	90	
	7	–	–	–	78	87	
	8	36	57	55	90	84	
	9	37	59	56	92	81	
	10	–	–	–	84	78	
	11	39	60	58	95	75	
	12	40	62	60	97	72	
	13	–	–	–	87	69	
	14	41	63	61	98	66	
	15	43	65	63	101	63	
	16	–	61	59	96	60	
	17	44	66	64	102	57	
	18	–	–	–	99	54	

Function Block	Macrocell	PC84	PQ100	TQ100	PQ160	BScan Order	Notes
6	1	–	–	–	91	51	
6	2	45	67	65	103	48	
6	3	46	68	66	104	45	
6	4	–	75	73	116	42	
6	5	47	69	67	106	39	
6	6	48	70	68	108	36	
6	7	–	–	–	105	33	
6	8	50	72	70	111	30	
6	9	51	73	71	113	27	
6	10	–	–	–	107	24	
6	11	52	74	72	115	21	
6	12	53	76	74	117	18	
6	13	–	–	–	112	15	
6	14	54	78	76	122	12	
6	15	55	79	77	124	9	
6	16	–	81	79	129	6	
6	17	56	80	78	126	3	
6	18	–	–	–	114	0	

5108 Global, JTAG and Power Pins

Pin Type	PC84	PQ100	TQ100	PQ160
I/O/GCK1	9	24	22	33
I/O/GCK2	10	25	23	35
I/O/GCK3	12	29	27	42
I/O/GTS1	76	5	3	6
I/O/GTS2	77	6	4	8
I/O/GSR	74	1	99	159
TCK	30	50	48	75
TDI	28	47	45	71
TDO	59	85	83	136
TMS	29	49	47	73
CCINT 5 V	38,73,78	7,59,100	5,57,98	10,46,91,157
CIO 3.3 V/5 V	22,64	28,40,53,90	26,38,51,88	1,41,61,81,121,141
GND	8,16,27,42,49,60	2,23,33,46,64,71,77,86	100,21,31,44,62,69,75,84	20,31,40,51,70,80,99
GND	–	–	–	109,119,120,127,137
GND	–	–	–	160
o connects	–	–	–	3,5,7,32,38,39,48,53,55,6 5,66,67,83,85,93,109, 118,119,125,130,131, 132,149,150,151

lering Information



d Options

- 20 20 ns pin-to-pin delay
-15 15 ns pin-to-pin delay
-10 10 ns pin-to-pin delay
-7 7 ns pin-to-pin delay

Packaging Options

PC84 84-Pin Plastic Leaded Chip Carrier (PLCC)
PQ100 100-Pin Plastic Quad Flat Pack (PQFP)
TQ100 100-Pin Very Thin Quad Flat Pack (TQFP)
PQ160 160-Pin Plastic Quad Flat Pack (PQFP)

Temperature Options

C Commercial 0°C to +70°C
I Industrial –40°C to +85°C

nponent Availability

		84	100		160
		Plastic PLCC	Plastic PQFP	Plastic TQFP	Plastic PQFP
		PC84	PQ100	TQ100	PQ160
5108	–20	C(I)	C(I)	C(I)	C(I)
	–15	C(I)	C(I)	C(I)	C(I)
	10	C(I)	C(I)	C(I)	C(I)
	–7	C(I)	C(I)	C(I)	C(I)

ommercial = 0° to +70°C I = Industrial = –40° to +85°C

ision Control

Date	Revision
2/04/98	Update AC Characteristics and Internal Parameters

ıres

- ıatible with MCS-51® Products
- 'tes of In-System Programmable (ISP) Flash Memory
- ndurance: 1000 Write/Erase Cycles
- o 5.5V Operating Range
- Static Operation: 0 Hz to 33 MHz
- -level Program Memory Lock
- 8-bit Internal RAM
- ıgrammable I/O Lines
- 6-bit Timer/Counters
- ierrupt Sources
- uplex UART Serial Channel
- ıower Idle and Power-down Modes
- ıpt Recovery from Power-down Mode
- ıdog Timer
-)ata Pointer
- '-off Flag
- 'rogramming Time
- le ISP Programming (Byte and Page Mode)

ription

39S51 is a low-power, high-performance CMOS 8-bit microcontroller with 4K in-system programmable Flash memory. The device is manufactured using high-density nonvolatile memory technology and is compatible with the industdard 80C51 instruction set and pinout. The on-chip Flash allows the program to be reprogrammed in-system or by a conventional nonvolatile memory pro-r. By combining a versatile 8-bit CPU with in-system programmable Flash on a nic chip, the Atmel AT89S51 is a powerful microcontroller which provides a exible and cost-effective solution to many embedded control applications.

9S51 provides the following standard features: 4K bytes of Flash, 128 bytes of ? I/O lines, Watchdog timer, two data pointers, two 16-bit timer/counters, a five-vo-level interrupt architecture, a full duplex serial port, on-chip oscillator, and rcuitry. In addition, the AT89S51 is designed with static logic for operation zero frequency and supports two software selectable power saving modes. Mode stops the CPU while allowing the RAM, timer/counters, serial port, and system to continue functioning. The Power-down mode saves the RAM con-t freezes the oscillator, disabling all other chip functions until the next external or hardware reset.

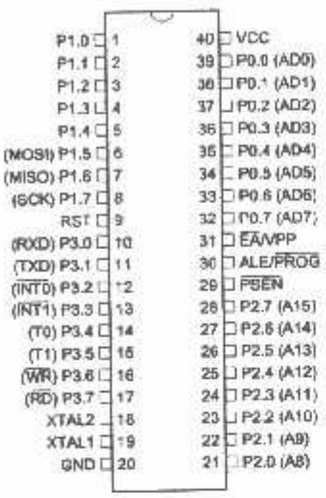
8-bit Microcontroller with 4K Bytes In-System Programmable Flash

AT89S51

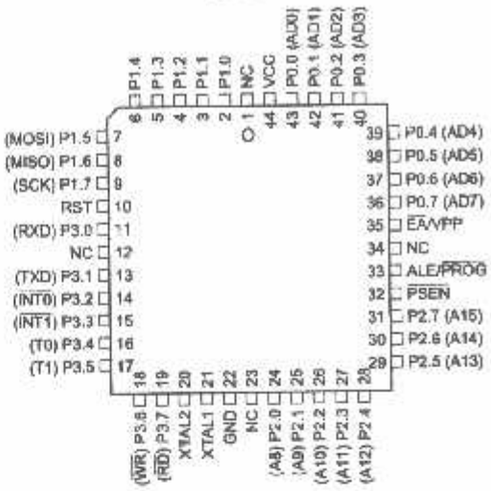
Rev. 2487A–10/01

Configurations

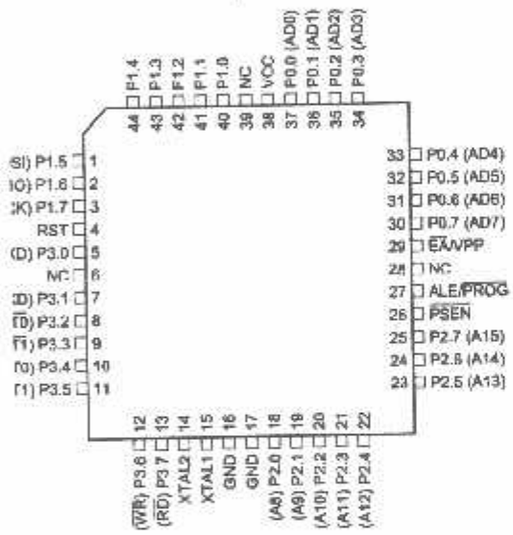
PDIP



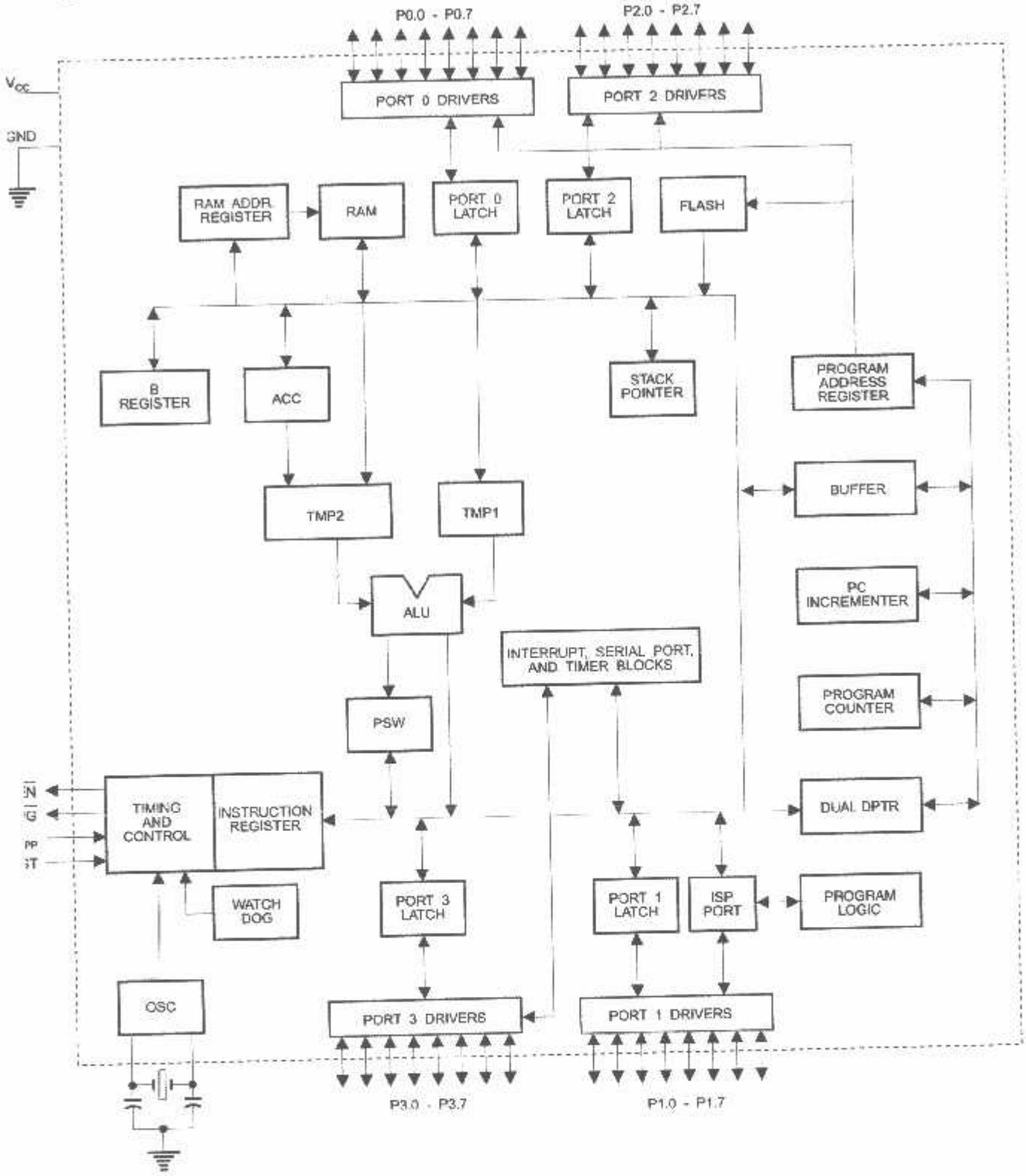
PLCC



TQFP



‹ Diagram


P0.0 - P0.7
P2.0 - P2.7
PORT 0 DRIVERS
PORT 2 DRIVERS
V_{CC}
GND
RAM ADDR. REGISTER
RAM
PORT 0 LATCH
PORT 2 LATCH
FLASH
B REGISTER
ACC
STACK POINTER
PROGRAM ADDRESS REGISTER
BUFFER
TMP2
TMP1
ALU
PC INCREMENTER
INTERRUPT, SERIAL PORT, AND TIMER BLOCKS
PROGRAM COUNTER
PSW
DUAL DPTR
TIMING AND CONTROL
INSTRUCTION REGISTER
WATCH DOG
PORT 3 LATCH
PORT 1 LATCH
ISP PORT
PROGRAM LOGIC
OSC
PORT 3 DRIVERS
PORT 1 DRIVERS
P3.0 - P3.7
P1.0 - P1.7

Description

Supply voltage.

Ground.

Port 0 is an 8-bit open drain bidirectional I/O port. As an output port, each pin can sink eight TTL inputs. When 1s are written to port 0 pins, the pins can be used as high-impedance inputs.

Port 0 can also be configured to be the multiplexed low-order address/data bus during accesses to external program and data memory. In this mode, P0 has internal pull-ups.

Port 0 also receives the code bytes during Flash programming and outputs the code bytes during program verification. **External pull-ups are required during program verification.**

Port 1 is an 8-bit bidirectional I/O port with internal pull-ups. The Port 1 output buffers can sink/source four TTL inputs. When 1s are written to Port 1 pins, they are pulled high by the internal pull-ups and can be used as inputs. As inputs, Port 1 pins that are externally being pulled low will source current (I_{IL}) because of the internal pull-ups.

Port 1 also receives the low-order address bytes during Flash programming and verification.

Port Pin	Alternate Functions
P1.5	MOSI (used for In-System Programming)
P1.6	MISO (used for In-System Programming)
P1.7	SCK (used for In-System Programming)

Port 2 is an 8-bit bidirectional I/O port with internal pull-ups. The Port 2 output buffers can sink/source four TTL inputs. When 1s are written to Port 2 pins, they are pulled high by the internal pull-ups and can be used as inputs. As inputs, Port 2 pins that are externally being pulled low will source current (I_{IL}) because of the internal pull-ups.

Port 2 emits the high-order address byte during fetches from external program memory and during accesses to external data memory that use 16-bit addresses (MOVX @ DPTR). In this application, Port 2 uses strong internal pull-ups when emitting 1s. During accesses to external data memory that use 8-bit addresses (MOVX @ RI), Port 2 emits the contents of the P2 Special Function Register.

Port 2 also receives the high-order address bits and some control signals during Flash programming and verification.

Port 3 is an 8-bit bidirectional I/O port with internal pull-ups. The Port 3 output buffers can sink/source four TTL inputs. When 1s are written to Port 3 pins, they are pulled high by the internal pull-ups and can be used as inputs. As inputs, Port 3 pins that are externally being pulled low will source current (I_{IL}) because of the pull-ups.

Port 3 receives some control signals for Flash programming and verification.

Port 3 also serves the functions of various special features of the AT89S51, as shown in the following table.

Port Pin	Alternate Functions
P3.0	RXD (serial input port)
P3.1	TXD (serial output port)
P3.2	$\overline{INT0}$ (external interrupt 0)
P3.3	$\overline{INT1}$ (external interrupt 1)
P3.4	T0 (timer 0 external input)
P3.5	T1 (timer 1 external input)
P3.6	$\overline{WR}$ (external data memory write strobe)
P3.7	$\overline{RD}$ (external data memory read strobe)

Reset input. A high on this pin for two machine cycles while the oscillator is running resets the device. This pin drives High for 98 oscillator periods after the Watchdog times out. The DISRTO bit in SFR AUXR (address 8EH) can be used to disable this feature. In the default state of bit DISRTO, the RESET HIGH out feature is enabled.

$\overline{ROG}$

Address Latch Enable (ALE) is an output pulse for latching the low byte of the address during accesses to external memory. This pin is also the program pulse input ($\overline{PROG}$) during Flash programming.

In normal operation, ALE is emitted at a constant rate of 1/6 the oscillator frequency and may be used for external timing or clocking purposes. Note, however, that one ALE pulse is skipped during each access to external data memory.

If desired, ALE operation can be disabled by setting bit 0 of SFR location 8EH. With the bit set, ALE is active only during a MOVX or MOVC instruction. Otherwise, the pin is weakly pulled high. Setting the ALE-disable bit has no effect if the microcontroller is in external execution mode.

Program Store Enable ($\overline{PSEN}$) is the read strobe to external program memory.

When the AT89S51 is executing code from external program memory, $\overline{PSEN}$ is activated twice each machine cycle, except that two $\overline{PSEN}$ activations are skipped during each access to external data memory.

P

External Access Enable. $\overline{EA}$ must be strapped to GND in order to enable the device to fetch code from external program memory locations starting at 0000H up to FFFFH. Note, however, that if lock bit 1 is programmed, $\overline{EA}$ will be internally latched on reset.

$\overline{EA}$ should be strapped to V_{CC} for internal program executions.

This pin also receives the 12-volt programming enable voltage (V_{PP}) during Flash programming.

Input to the inverting oscillator amplifier and input to the internal clock operating circuit.

Output from the inverting oscillator amplifier

ial tion sters

A map of the on-chip memory area called the Special Function Register (SFR) space is shown in Table 1.

Note that not all of the addresses are occupied, and unoccupied addresses may not be implemented on the chip. Read accesses to these addresses will in general return random data, and write accesses will have an indeterminate effect.

. AT89S51 SFR Map and Reset Values

								0FFH
B 00000000								0F7H
								0EFH
ACC 00000000								0E7H
								0DFH
PSW 00000000								0D7H
								0CFH
								0C7H
IP XX000000								0BFH
P3 11111111								0B7H
IE 0X000000								0AFH
P2 11111111		AUXR1 XXXXXXX0				WDTRST XXXXXXXX		0A7H
SCON 00000000	SBUF XXXXXXXX							9FH
P1 11111111								97H
TCON 00000000	TMOD 00000000	TL0 00000000	TL1 00000000	TH0 00000000	TH1 00000000	AUXR XXX00XX0		8FH
P0 11111111	SP 00000111	DP0L 00000000	DP0H 00000000	DP1L 00000000	DP1H 00000000		PCON 0XXX0000	87H

User software should not write 1s to these unlisted locations, since they may be used in future products to invoke new features. In that case, the reset or inactive values of the new bits will always be 0.

Interrupt Registers: The individual interrupt enable bits are in the IE register. Two priorities can be set for each of the five interrupt sources in the IP register.

Table 2. AUXR: Auxiliary Register

AUXR Address = 8EH Reset Value = XXX00XX0B

Not Bit Addressable

Bit	7	6	5	4	3	2	1	0
	–	–	–	WDIDLE	DISRTO	–	–	DISALE

– Reserved for future expansion

DISALE Disable/Enable ALE

DISALE Operating Mode

0 ALE is emitted at a constant rate of 1/6 the oscillator frequency

1 ALE is active only during a MOVX or MOVC instruction

DISRTO Disable/Enable Reset out

DISRTO

0 Reset pin is driven High after WDT times out

1 Reset pin is input only

WDIDLE Disable/Enable WDT in IDLE mode

WDIDLE

0 WDT continues to count in IDLE mode

1 WDT halts counting in IDLE mode

Dual Data Pointer Registers: To facilitate accessing both internal and external data memory, two banks of 16-bit Data Pointer Registers are provided: DP0 at SFR address locations 82H-83H and DP1 at 84H-85H. Bit DPS = 0 in SFR AUXR1 selects DP0 and DPS = 1 selects DP1. The user should always initialize the DPS bit to the appropriate value before accessing the respective Data Pointer Register.

Power Off Flag: The Power Off Flag (POF) is located at bit 4 (PCON.4) in the PCON SFR. POF is set to "1" during power up. It can be set and rest under software control and is not affected by reset.

Table 3. AUXR1: Auxiliary Register 1

AUXR1

Address = A2H

Reset Value = XXXXXXX0B

Not Bit Addressable

Bit	7	6	5	4	3	2	1	0
	–	–	–	–	–	–	–	DPS

– Reserved for future expansion

DPS Data Pointer Register Select

DPS	
0	Selects DPTR Registers DP0L, DP0H
1	Selects DPTR Registers DP1L, DP1H

ory
ization

MCS-51 devices have a separate address space for Program and Data Memory. Up to 64K bytes each of external Program and Data Memory can be addressed.

im Memory

If the $\overline{EA}$ pin is connected to GND, all program fetches are directed to external memory.

On the AT89S51, if $\overline{EA}$ is connected to V_{CC}, program fetches to addresses 0000H through FFFH are directed to internal memory and fetches to addresses 1000H through FFFFH are directed to external memory.

lemory

The AT89S51 implements 128 bytes of on chip RAM. The 128 bytes are accessible via direct and indirect addressing modes. Stack operations are examples of indirect addressing, so the 128 bytes of data RAM are available as stack space.

ıdog

time
ed with
:-out)

The WDT is intended as a recovery method in situations where the CPU may be subjected to software upsets. The WDT consists of a 14-bit counter and the Watchdog Timer Reset (WDTRST) SFR. The WDT is defaulted to disable from exiting reset. To enable the WDT, a user must write 01EH and 0E1H in sequence to the WDTRST register (SFR location 0A6H). When the WDT is enabled, it will increment every machine cycle while the oscillator is running. The WDT timeout period is dependent on the external clock frequency. There is no way to disable the WDT except through reset (either hardware reset or WDT overflow reset). When WDT overflows, it will drive an output RESET HIGH pulse at the RST pin.

| the WDT

To enable the WDT, a user must write 01EH and 0E1H in sequence to the WDTRST register (SFR location 0A6H). When the WDT is enabled, the user needs to service it by writing 01EH and 0E1H to WDTRST to avoid a WDT overflow. The 14-bit counter overflows when it reaches 16383 (3FFFH), and this will reset the device. When the WDT is enabled, it will increment every machine cycle while the oscillator is running. This means the user must reset the WDT at least every 16383 machine cycles. To reset the WDT the user must write 01EH and 0E1H to WDTRST. WDTRST is a write-only register. The WDT counter cannot be read or written. When WDT overflows, it will generate an output RESET pulse at the RST pin. The RESET pulse duration is 98xTOSC, where TOSC=1/FOSC. To make the best use of the WDT, it

should be serviced in those sections of code that will periodically be executed within the time required to prevent a WDT reset.

During r-down dle

In Power-down mode the oscillator stops, which means the WDT also stops. While in Power-down mode, the user does not need to service the WDT. There are two methods of exiting Power-down mode: by a hardware reset or via a level activated external interrupt, which is enabled prior to entering Power-down mode. When Power-down is exited with hardware reset, servicing the WDT should occur as it normally does whenever the AT89S51 is reset. Exiting Power-down with an interrupt is significantly different. The interrupt is held low long enough for the oscillator to stabilize. When the interrupt is brought high, the interrupt is serviced. To prevent the WDT from resetting the device while the interrupt pin is held low, the WDT is not started until the interrupt is pulled high. It is suggested that the WDT be reset during the interrupt service for the interrupt used to exit Power-down mode.

To ensure that the WDT does not overflow within a few states of exiting Power-down, it is best to reset the WDT just before entering Power-down mode.

Before going into the IDLE mode, the WDIDLE bit in SFR AUXR is used to determine whether the WDT continues to count if enabled. The WDT keeps counting during IDLE (WDIDLE bit = 0) as the default state. To prevent the WDT from resetting the AT89S51 while in IDLE mode, the user should always set up a timer that will periodically exit IDLE, service the WDT, and reenter IDLE mode.

With WDIDLE bit enabled, the WDT will stop to count in IDLE mode and resumes the count upon exit from IDLE.

The UART in the AT89S51 operates the same way as the UART in the AT89C51. For further information on the UART operation, refer to the ATMEL Web site (http://www.atmel.com). From the home page, select 'Products', then '8051-Architecture Flash Microcontroller', then 'Product Overview'.

0 and 1

Timer 0 and Timer 1 in the AT89S51 operate the same way as Timer 0 and Timer 1 in the AT89C51. For further information on the timers' operation, refer to the ATMEL Web site (http://www.atmel.com). From the home page, select 'Products', then '8051-Architecture Flash Microcontroller', then 'Product Overview'.

upts

The AT89C51 has a total of five interrupt vectors: two external interrupts ($\overline{INT0}$ and $\overline{INT1}$), two timer interrupts (Timers 0 and 1), and the serial port interrupt. These interrupts are all shown in Figure 1.

Each of these interrupt sources can be individually enabled or disabled by setting or clearing a bit in Special Function Register IE. IE also contains a global disable bit, EA, which disables all interrupts at once.

Note that Table 4 shows that bit position IE.6 is unimplemented. In the AT89S51, bit position IE.5 is also unimplemented. User software should not write 1s to these bit positions, since they may be used in future AT89 products.

The Timer 0 and Timer 1 flags, TF0 and TF1, are set at S5P2 of the cycle in which the timers overflow. The values are then polled by the circuitry in the next cycle

Table 4. Interrupt Enable (IE) Register

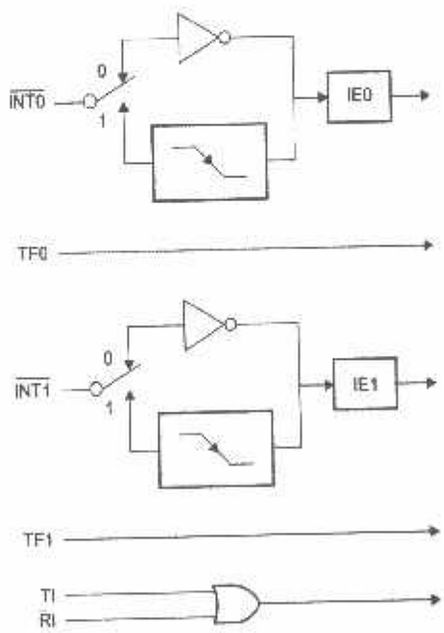
(MSB)							(LSB)
EA	–	–	ES	ET1	EX1	ET0	EX0

Enable Bit = 1 enables the interrupt.

Enable Bit = 0 disables the interrupt.

Symbol	Position	Function
EA	IE.7	Disables all interrupts. If EA = 0, no interrupt is acknowledged. If EA = 1, each interrupt source is individually enabled or disabled by setting or clearing its enable bit.
–	IE.6	Reserved
–	IE.5	Reserved
ES	IE.4	Serial Port interrupt enable bit
ET1	IE.3	Timer 1 interrupt enable bit
EX1	IE.2	External interrupt 1 enable bit
ET0	IE.1	Timer 0 interrupt enable bit
EX0	IE.0	External interrupt 0 enable bit
User software should never write 1s to reserved bits, because they may be used in future AT89 products.		

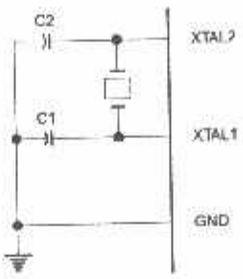
Figure 1. Interrupt Sources



lator acteristics

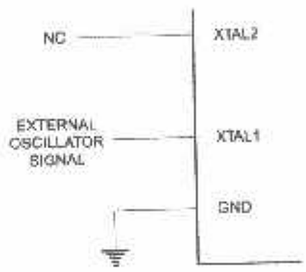
XTAL1 and XTAL2 are the input and output, respectively, of an inverting amplifier that can be configured for use as an on-chip oscillator, as shown in Figure 2. Either a quartz crystal or ceramic resonator may be used. To drive the device from an external clock source, XTAL2 should be left unconnected while XTAL1 is driven, as shown in Figure 3. There are no requirements on the duty cycle of the external clock signal, since the input to the internal clocking circuitry is through a divide-by-two flip-flop, but minimum and maximum voltage high and low time specifications must be observed.

Figure 2. Oscillator Connections



Note: C1, C2 = 30 pF ±10 pF for Crystals = 40 pF ±10 pF for Ceramic Resonators

Figure 3. External Clock Drive Configuration



lode

In idle mode, the CPU puts itself to sleep while all the on-chip peripherals remain active. The mode is invoked by software. The content of the on-chip RAM and all the special function registers remain unchanged during this mode. The idle mode can be terminated by any enabled interrupt or by a hardware reset.

Note that when idle mode is terminated by a hardware reset, the device normally resumes program execution from where it left off, up to two machine cycles before the internal reset algorithm takes control. On-chip hardware inhibits access to internal RAM in this event, but access to the port pins is not inhibited. To eliminate the possibility of an unexpected write to a port pin when idle mode is terminated by a reset, the instruction following the one that invokes idle mode should not write to a port pin or to external memory.

r-down

In the Power-down mode, the oscillator is stopped, and the instruction that invokes Power-down is the last instruction executed. The on-chip RAM and Special Function Registers retain their values until the Power-down mode is terminated. Exit from Power-down mode can be initiated either by a hardware reset or by activation of an enabled external interrupt into $\overline{INT0}$ or $\overline{INT1}$. Reset redefines the SFRs but does not change the on-chip RAM. The reset should not be activated before V_{CC} is restored to its normal operating level and must be held active long enough to allow the oscillator to restart and stabilize.

Table 5. Status of External Pins During Idle and Power-down Modes

Mode	Program Memory	ALE	$\overline{PSEN}$	PORT0	PORT1	PORT2	PORT3
Idle	Internal	1	1	Data	Data	Data	Data
Idle	External	1	1	Float	Data	Address	Data
Power-down	Internal	0	0	Data	Data	Data	Data
Power-down	External	0	0	Float	Data	Data	Data

ram ory Lock

The AT89S51 has three lock bits that can be left unprogrammed (U) or can be programmed (P) to obtain the additional features listed in the following table.

Table 6. Lock Bit Protection Modes

Program Lock Bits				Protection Type
	LB1	LB2	LB3	
1	U	U	U	No program lock features
2	P	U	U	MOVC instructions executed from external program memory are disabled from fetching code bytes from internal memory, $\overline{EA}$ is sampled and latched on reset, and further programming of the Flash memory is disabled
3	P	P	U	Same as mode 2, but verify is also disabled
4	P	P	P	Same as mode 3, but external execution is also disabled

When lock bit 1 is programmed, the logic level at the $\overline{EA}$ pin is sampled and latched during reset. If the device is powered up without a reset, the latch initializes to a random value and holds that value until reset is activated. The latched value of $\overline{EA}$ must agree with the current logic level at that pin in order for the device to function properly.

amming ash – el Mode

The AT89S51 is shipped with the on-chip Flash memory array ready to be programmed. The programming interface needs a high-voltage (12-volt) program enable signal and is compatible with conventional third-party Flash or EPROM programmers.

The AT89S51 code memory array is programmed byte-by-byte.

Programming Algorithm: Before programming the AT89S51, the address, data, and control signals should be set up according to the Flash programming mode table and Figures 13 and 14. To program the AT89S51, take the following steps:

1. Input the desired memory location on the address lines.
2. Input the appropriate data byte on the data lines.
3. Activate the correct combination of control signals.
4. Raise $\overline{EA}/V_{PP}$ to 12V.
5. Pulse ALE/$\overline{PROG}$ once to program a byte in the Flash array or the lock bits. The byte-write cycle is self-timed and typically takes no more than 50 µs. Repeat steps 1 through 5, changing the address and data for the entire array or until the end of the object file is reached.

$\overline{Data}$ Polling: The AT89S51 features $\overline{Data}$ Polling to indicate the end of a byte write cycle. During a write cycle, an attempted read of the last byte written will result in the complement of the written data on P0.7. Once the write cycle has been completed, true data is valid on all outputs, and the next cycle may begin. $\overline{Data}$ Polling may begin any time after a write cycle has been initiated.

Ready/Busy: The progress of byte programming can also be monitored by the RDY/BSY output signal. P3.0 is pulled low after ALE goes high during programming to indicate BUSY. P3.0 is pulled high again when programming is done to indicate READY.

Program Verify: If lock bits LB1 and LB2 have not been programmed, the programmed code data can be read back via the address and data lines for verification. The status of the individual lock bits can be verified directly by reading them back.

Reading the Signature Bytes: The signature bytes are read by the same procedure as a normal verification of locations 000H, 100H, and 200H, except that P3.6 and P3.7 must be pulled to a logic low. The values returned are as follows.

(000H) = 1EH indicates manufactured by Atmel
(100H) = 51H indicates 89S51
(200H) = 06H

Chip Erase: In the parallel programming mode, a chip erase operation is initiated by using the proper combination of control signals and by pulsing ALE/PROG low for a duration of 200 ns - 500 ns.

In the serial programming mode, a chip erase operation is initiated by issuing the Chip Erase instruction. In this mode, chip erase is self-timed and takes about 500 ms.

During chip erase, a serial read from any address location will return 00H at the data output.

amming ash – Mode

The Code memory array can be programmed using the serial ISP interface while RST is pulled to V_{CC}. The serial interface consists of pins SCK, MOSI (input) and MISO (output). After RST is set high, the Programming Enable instruction needs to be executed first before other operations can be executed. Before a reprogramming sequence can occur, a Chip Erase operation is required.

The Chip Erase operation turns the content of every memory location in the Code array into FFH.

Either an external system clock can be supplied at pin XTAL1 or a crystal needs to be connected across pins XTAL1 and XTAL2. The maximum serial clock (SCK) frequency should be less than 1/16 of the crystal frequency. With a 33 MHz oscillator clock, the maximum SCK frequency is 2 MHz.

imming hm

To program and verify the AT89S51 in the serial programming mode, the following sequence is recommended:

1. Power-up sequence:
   Apply power between VCC and GND pins.
   Set RST pin to "H".
   If a crystal is not connected across pins XTAL1 and XTAL2, apply a 3 MHz to 33 MHz clock to XTAL1 pin and wait for at least 10 milliseconds.
2. Enable serial programming by sending the Programming Enable serial instruction to pin MOSI/P1.5. The frequency of the shift clock supplied at pin SCK/P1.7 needs to be less than the CPU clock at XTAL1 divided by 16.
3. The Code array is programmed one byte at a time in either the Byte or Page mode. The write cycle is self-timed and typically takes less than 0.5 ms at 5V.
4. Any memory location can be verified by using the Read instruction that returns the content at the selected address at serial output MISO/P1.6.
5. At the end of a programming session, RST can be set low to commence normal device operation.

Power-off sequence (if needed):

Set XTAL1 to "L" (if a crystal is not used).

Set RST to "L".

Turn V_{CC} power off.

Data Polling: The Data Polling feature is also available in the serial mode. In this mode, during a write cycle an attempted read of the last byte written will result in the complement of the MSB of the serial output byte on MISO.

The Instruction Set for Serial Programming follows a 4-byte protocol and is shown in Table 8 on page 18.

ımming :tion Set

amming ace – ei Mode

Every code byte in the Flash array can be programmed by using the appropriate combination of control signals. The write operation cycle is self-timed and once initiated, will automatically time itself to completion.

All major programming vendors offer worldwide support for the Atmel microcontroller series. Please contact your local programming vendor for the appropriate software revision.

Flash Programming Modes

	V_{CC}	RST	PSEN	ALE/ PROG	EA/ V_{PP}	P2.6	P2.7	P3.3	P3.6	P3.7	P0.7-0 Data	P2.3-0	P1.7-0
												Address	
de Data	5V	H	L	(2)	12V	L	H	H	H	H	D_{IN}	A11-8	A7-0
de Data	5V	H	L	H	H	L	L	L	H	H	D_{OUT}	A11-8	A7-0
k Bit 1	5V	H	L	(3)	12V	H	H	H	H	H	X	X	X
k Bit 2	5V	H	L	(3)	12V	H	H	H	L	L	X	X	X
k Bit 3	5V	H	L	(3)	12V	H	L	H	H	L	X	X	X
k Bits	5V	H	L	H	H	H	H	L	H	L	P0.2, P0.3, P0.4	X	X
se	5V	H	L	(1)	12V	H	L	H	L	L	X	X	X
nel ID	5V	H	L	H	H	L	L	L	L	L	1EH	0000	00H
vice ID	5V	H	L	H	H	L	L	L	L	L	51H	0001	00H
vice ID	5V	H	L	H	H	L	L	L	L	L	06H	0010	00H

1. Each PROG pulse is 200 ns - 500 ns for Chip Erase.
2. Each PROG pulse is 200 ns - 500 ns for Write Code Data.
3. Each PROG pulse is 200 ns - 500 ns for Write Lock Bits.
4. RDY/BSY signal is output on P3.0 during programming.
5. X = don't care.

Figure 4. Programming the Flash Memory (Parallel Mode)

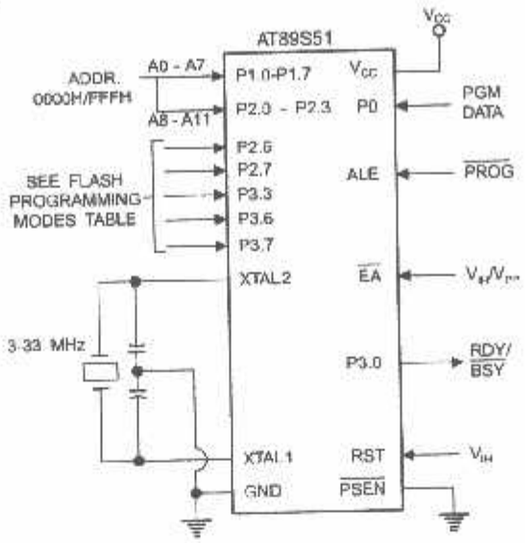
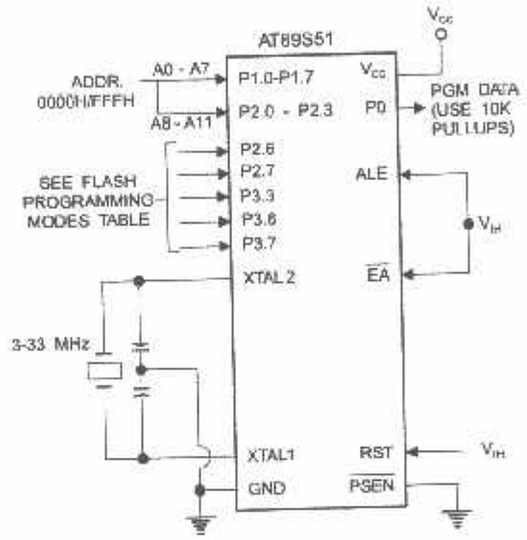


Figure 5. Verifying the Flash Memory (Parallel Mode)

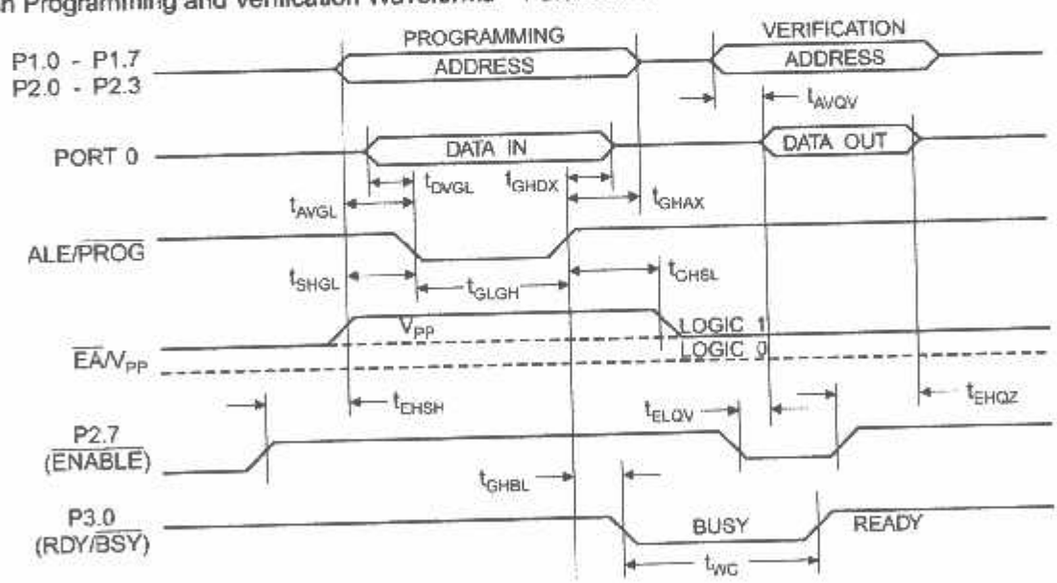


Programming and Verification Characteristics (Parallel Mode)

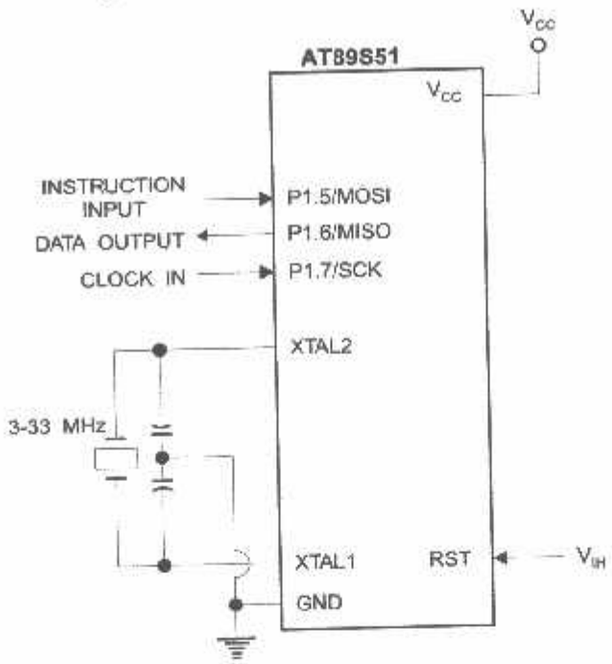
°C to 30°C, V_{CC} = 4.5 to 5.5V

	Parameter	Min	Max	Units
	Programming Supply Voltage	11.5	12.5	V
	Programming Supply Current		10	mA
	V_{CC} Supply Current		30	mA
	Oscillator Frequency	3	33	MHz
	Address Setup to $\overline{PROG}$ Low	$48t_{CLCL}$		
	Address Hold After $\overline{PROG}$	$48t_{CLCL}$		
	Data Setup to $\overline{PROG}$ Low	$48t_{CLCL}$		
	Data Hold After $\overline{PROG}$	$48t_{CLCL}$		
	P2.7 ($\overline{ENABLE}$) High to V_{PP}	$48t_{CLCL}$		
	V_{PP} Setup to $\overline{PROG}$ Low	10		µs
	V_{PP} Hold After $\overline{PROG}$	10		µs
	$\overline{PROG}$ Width	0.2	1	µs
	Address to Data Valid		$48t_{CLCL}$	
	$\overline{ENABLE}$ Low to Data Valid		$48t_{CLCL}$	
	Data Float After $\overline{ENABLE}$	0	$48t_{CLCL}$	
	$\overline{PROG}$ High to $\overline{BUSY}$ Low		1.0	µs
	Byte Write Cycle Time		50	µs

Flash Programming and Verification Waveforms – Parallel Mode

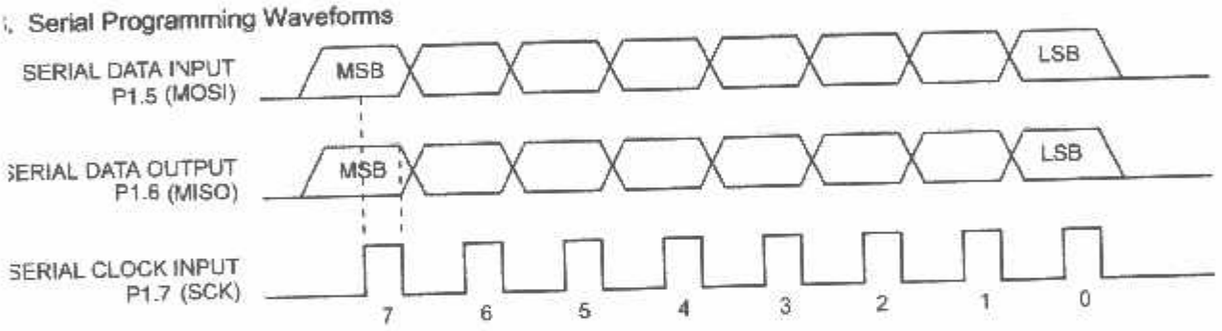


7. Flash Memory Serial Downloading



Programming and Verification Waveforms – Serial Mode

1. Serial Programming Waveforms



1

Serial Programming Instruction Set

tion	Instruction Format Byte 1	Byte 2	Byte 3	Byte 4	Operation
ıming Enable	1010 1100	0101 0011	xxxx xxxx	xxxx xxxx 0110 1001 (Output)	Enable Serial Programming while RST is high
ase	1010 1100	100x xxxx	xxxx xxxx	xxxx xxxx	Chip Erase Flash memory array
ogram Memory ode)	0010 0000	xxxx A11 A10 A9 A8	A7 A6 A5 A4 A3 A2 A1 A0	D7 D6 D5 D4 D3 D2 D1 D0	Read data from Program memory in the byte mode
ogram Memory ode)	0100 0000	xxxx A11 A10 A9 A8	A7 A6 A5 A4 A3 A2 A1 A0	D7 D6 D5 D4 D3 D2 D1 D0	Write data to Program memory in the byte mode
ck Bits[2]	1010 1100	1110 00 B1 B2	xxxx xxxx	xxxx xxxx	Write Lock bits. See Note (2).
ck Bits	0010 0100	xxxx xxxx	xxxx xxxx	xx LB3 LB2 LB1 xx	Read back current status of the lock bits (a programmed lock bit reads back as a "1")
gnature Bytes[1]	0010 1000	xxx A5 A4 A3 A2 A1	A0 xxx xxxx	Signature Byte	Read Signature Byte
ogram Memory lode)	0011 0000	xxxx A11 A10 A9 A8	Byte 0	Byte 1... Byte 255	Read data from Program memory in the Page Mode (256 bytes)
ogram Memory lode)	0101 0000	xxxx A11 A10 A9 A8	Byte 0	Byte 1... Byte 255	Write data to Program memory in the Page Mode (256 bytes)

1. The signature bytes are not readable in Lock Bit Modes 3 and 4.
2. B1 = 0, B2 = 0 → Mode 1, no lock protection
   B1 = 0, B2 = 1 → Mode 2, lock bit 1 activated
   B1 = 1, B2 = 0 → Mode 3, lock bit 2 activated
   B1 = 1, B1 = 1 → Mode 4, lock bit 3 activated

   } Each of the lock bits needs to be activated sequentially before Mode 4 can be executed.

After Reset signal is high, SCK should be low for at least 64 system clocks before it goes high to clock in the enable data bytes. No pulsing of Reset signal is necessary. SCK should be no faster than 1/16 of the system clock at XTAL1.

For Page Read/Write, the data always starts from byte 0 to 255. After the command byte and upper address byte are latched, each byte thereafter is treated as data until all 256 bytes are shifted in/out. Then the next instruction will be ready to be decoded.