SKRIPSI

PERENCANAAN DAN PEMBUATAN MASTER KONTROL LAB. BAHASA DELAPAN CHANNEL BERBASIS MIKROKONTROLLER AT89S8252

Disusun Oleh :

ISNAINI ROZAFI

NIM : 01.17.044

KONSENTRASI TEKNIK ELEKTRONIKA

JURUSAN TEKNIK ELEKTRO S-1

FAKULTAS TEKNOLOGI INDUSTRI

INSTITUT TEKNOLOGI NASIONAL

MALANG

2007

LEMBAR PERSETUJUAN

PERENCANAAN DAN PEMBUATAN MASTER KONTROL LAB. BAHASA DELAPAN CHANNEL BERBASIS MIKROKONTROLLER AT89S8252

SKRIPSI

Disusun dan Diajukan Untuk Melengkapi dan Memenuhi Syarat Guna Mencapai Gelar Sarjana Teknik

Disusun Oleh :

ISNAINI ROZAFI

NIM : 01.17.044

Mengetahui
Ketua Jurusan Teknik Elektro S-1

Ir. F. Yudi Limpraptono, MT.
NIP.Y. 1039500274

Diperiksa dan disetujui
Dosen Pembimbing

Joseph Dedi Irawan ST., MT
NIP.132315178

KONSENTRASI TEKNIK ELEKTRONIKA

JURUSAN TEKNIK ELEKTRO S-1

FAKULTAS TEKNOLOGI INDUSTRI

INSTITUT TEKNOLOGI NASIONAL MALANG

2007

INSTITUT TEKNOLOGI NASIONAL MALANG
FAKULTAS TEKNOLOGI INDUSTRI
JURUSAN TEKNIK ELEKTRO S-1
KONSENTRASI ELEKTRONIKA

BERITA ACARA UJIAN SKRIPSI
FAKULTAS TEKNOLOGI INDUSTRI

1. Nama : Isanaini Rozafi
2. NIM : 01.17.044
3. Jurusan : Teknik Elektro S-1
4. Konsentrasi : Elektronika
5. Judul Skripsi : Perencanaan dan Pembuatan Master Kontrol Lab. Bahasa Delapan Channel Berbasis Mikrokontroller AT89S8252

Dipertahankan dihadapan Majelis Penguji Skripsi Jenjang Strata Satu (S-1)

Pada :

Hari : Jum'at

Tanggal : 23 Maret 2007

Dengan Nilai : 82,5 (A)

Panitia Ujian Skripsi

Ketua

Ir. Mochtar Asroni, MSME
NIP.Y. 1018100036

Sekretaris

Ir. F. Yudi Limpraptono, MT.
NIP.Y. 1039500274

Anggota Penguji

Penguji I

Ir. Widodo Pudji M, MT.
NIP.Y. 1028700171

Penguji II

Dr. Cahyo Crysdian, MSC.
NIP. 1030400412

KATA PENGANTAR

بسم الله الرحمن الرحيم

AlhamdulillahiRobbil'Alamin, puji syukur hamba panjatkan kehadirat-Mu Ya Allah atas segala nikmat dan karunia-Mu. Sholawat serta salam semoga tercurah kepada Rasulullah SAW., keluarga, sahabat, dan para pengikutnya. Amin. Atas kehendak Allah SWT. sajalah kami dapat menyelesaikan skripsi yang berjudul **"PERENCANAAN DAN PEMBUATAN MASTER KONTROL LAB. BAHASA DELAPAN CHANNEL BERBASIS MIKROKONTROLLER AT89S8252"** ini dengan lancar. Skripsi ini merupakan persyaratan kelulusan studi di jurusan Teknik Elektro S-1 konsentrasi Elektronika ITN Malang dan untuk mencapai gelar Sarjana Teknik.

Keberhasilan penyelesaian laporan Skripsi ini tidak lepas dari dukungan dan bantuan berbagai pihak. Untuk itu penyusun menyampaikan terimakasih kepada :

1. Kedua orang tuaku yang telah memberikan do'a dan dukungannya.
2. Bapak Prof. Dr. Ir. Abraham Lomi, MSEE. selaku Rektor ITN Malang.
3. Bapak Ir. F. Yudi Limpraptono, MT. selaku Ketua Jurusan Teknik Elektro S-1.
4. Bapak Joseph Dedi Irawan ST., MT. selaku Dosen Pembimbing.
5. Teman-temanku, terimakasih atas dukungannya selama ini.
6. Berbagai pihak yang tidak bisa disebutkan satu persatu, yang telah banyak membantu hingga selesainya laporan ini.

Penyusun telah berusaha semaksimal mungkin dan menyadari sepenuhnya akan keterbatasan pengetahuan dalam menyelesaikan laporan ini. Untuk itu penyusun mengharapkan saran dan kritik yang membangun dari pembaca demi kesempurnaan laporan ini.

Harapan penyusun, semoga laporan Skripsi ini memberikan manfaat bagi perkembangan ilmu pengetahuan dan pembaca.

Malang, Maret 2007
Penyusun

Isnaini Rozafi

Laboratorium Bahasa sekarang ini banyak dibutuhkan oleh para pengajar, khususnya pada bidang bahasa, contohnya pada tempat kursusan, sekolahan, lembaga penelitian, kampus, kantor dan lain sebagainya. Maka dengan adanya latar belakang itu, maka penulis mencoba membuatnya dengan judul Perencanaan Dan Pembuatan Master Kontrol Lab. Bahasa Delapan Chanel Berbasis Mikrokontroller AT89S8252, disamping sebagai pembelajaran, penulis juga ingin cepat lulus kuliah karena pengajuan skripsi sebagai prasyarat lulus sarjana.

1.2 Rumusan Masalah

Permasalahan yang dihadapi saat ini ialah bagaimana cara membuat dan merancang alat Laboratorium Bahasa yang berbasis mikrokontroller AT89S8252, yang meliputi cara kerja sistem, perancangan *hardware* dan *software*-nya.

Dari perumusan masalah didapat beberapa rumusan masalah, antara lain :

- Bagaimana membuat atau merancang cara kerja sistem dari Laboratorium Bahasa.
- Bagaimana cara memanfaatkan mikrokontroller sebagai pemroses cara kerja dari sistem yang kita rancang.
- Bagaimana cara memanfaatkan relay yang diatur oleh mikrokontroller sesuai dengan cara kerja yang kita inginkan.

1.3 Tujuan

Tujuan dari pengerjaan skripsi ini ialah Perencanaan Dan Pembuatan Alat Master Kontrol Lab. Bahasa Delapan Chanel Berbasis Mikrokontroller AT89S8252 sesuai dengan cara kerja yang kita inginkan dengan memanfaatkan

mikrokontroller sebagai pengontrol alat yang akan dibuat dan dapat dimanfaatkan oleh masyarakat ataupun instansi terkait.

1.4 Batasan Masalah

Agar permasalahan dari pembuatan alat ini tidak meluas, maka perlu dibatasi pada hal-hal sebagai berikut :

- Pengontrol utama menggunakan Mikrokontroller AT89S8252.
- Tidak membahas catu daya.
- Tidak membahas audio amplifier.
- Hanya memakai sebuah rangkaian pengajar (Guru) dan delapan rangkaian murid.

1.5 Metodologi Penulisan

Dalam penulisan skripsi ini,langkah-langkah yang dilakukan sebagai berikut :

1. Studi Pustaka

   Dimana penulis dengan membaca, mengumpulkan bahan-bahan materi yang digunakan sebagai referensi dan acuan dalam penyusunan skripsi

2. Studi Lapangan

   Dalam hal ini, memperoleh data dengan cara praktek langsung dalam perencanaan alat.

3. Pengolahan Data

   Mengolah data dengan jalan membuat analisa dan menarik kesimpulan dari hasil data yang didapat.

4. Pengujian Alat

Menguji alat yang telah dibuat apakah sesuai dengan perencanaan atau belum

5. Penyusunan Buku

Menyusu laporan hasil dari pelaksanaan skripsi.

1.6 Sistematika Penulisan

Sistematika penulisan dan gambaran secukupnya yang terdapat dalam setiap bab sebagai berikut :

BAB I : PENDAHULUAN

Membahas tentang latar belakang, rumusan masalah, tujuan, batasan masalah, metodologi perencanaan dan sistematika penulisan.

BAB II : LANDASAN TEORI

Membahas teori beserta pustaka yang relevan dan menunjang perancangan dan pembuatan rangkaian yang digunakan.

BAB III : PERENCANAAN DAN PEMBUATAN ALAT

Membahas perancangan dan pembuatan perangkat keras dan perangkat lunak.

BAB IV : PENGUJIAN ALAT

Membahas tentang pengujian-pengujian terhadap system yang telah dibuat.

BAB V : PENUTUP

Merupakan bagian-bagian penutup yang berisi kesimpulan dan saran yang bermanfaat bagi pengembangan lebih lanjut.

BAB II
LANDASAN TEORI

Landasan teori ini sangat membantu untuk dapat memahami suatu sistem. Disamping itu dapat juga dijadikan sebagai bahan acuan didalam merencanakan suatu sistem. Dengan pertimbangan hal-hal tersebut maka landasan teori merupakan bagian yang harus dipahami untuk pembahasan selanjutnya.

2.1 Mikrokontroler AT89S8252

Mikrokontroler AT89S8252 merupakan mikrokontroler 8 bit kompatibel dengan Standar industri MCS-51™ baik atas segi pemrograman maupun kaki tiap pin. Mikrokontroler AT89S8252 menpunyai 8 *Kbyte (Flash Programmable and Read Only Memori*) pada dasarnya mikrokontrolcr adalah terdiri atas mikroprosesor, *timer*, dan *counter*, perangkat I/O dan internal memori. Mikrokontroler termasuk perangkat yang sudah didesain dalam *chip* tunggal.

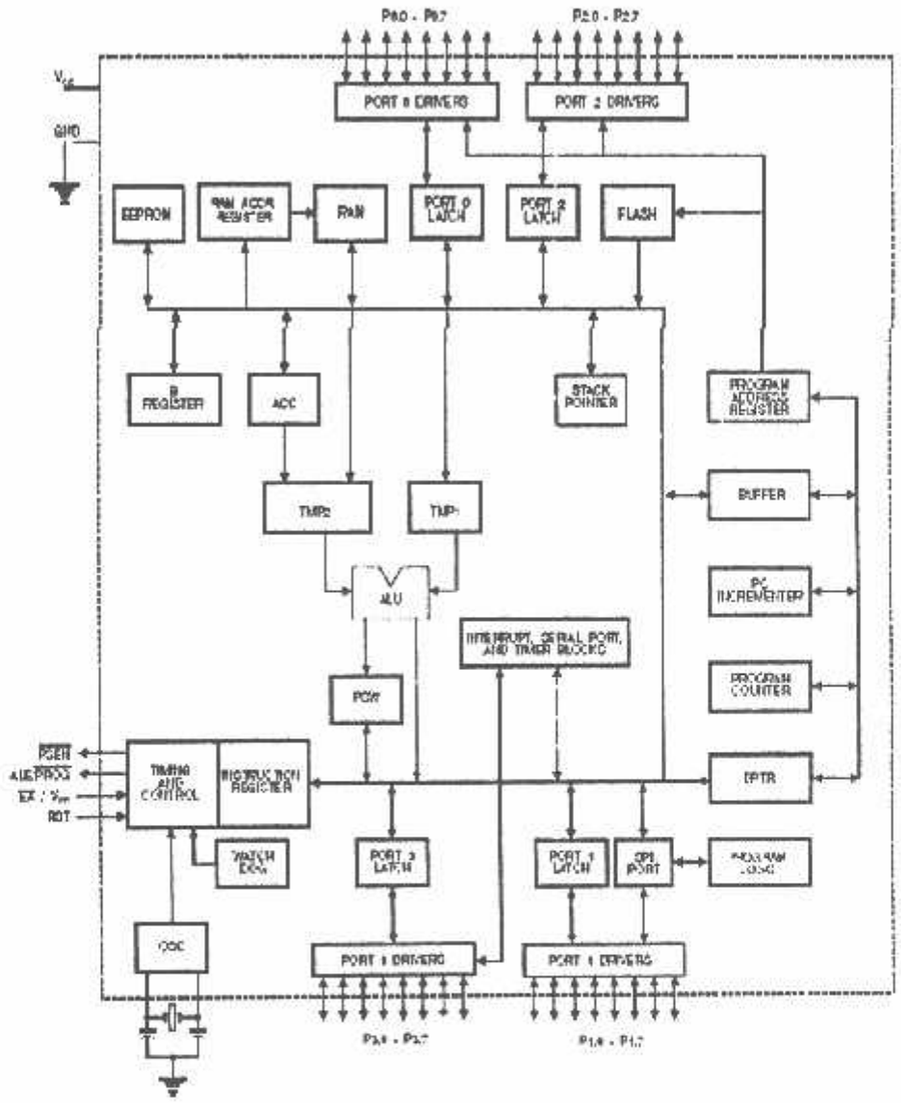
Pada dasarnya mikrokontroler mempunyai fungsi yang sama dengan mikroprosesor yaitu untuk mengontrol suatu kerja sistem. Selain itu mikrokontroler juga dikemas dalam satu *chip* (*single chip*). Didalam mikrokontroler juga terdapat CPU, ALU, PC, SP, dan register seperti dalam mikroprosesor, tetapi juga ditambah dengan perangkat-perangkat lain seperti ROM, RAM, PIO, SIO, *counter* dan sebuah rangkaian *clock*. Mikroprosesor didesain dengan intruksi-intruksi lebih luas dan 8 bit instruksi yang digunakan membaca data instruksi dari internal memori ke ALU. Sebagai suatu sistem control mikrokontroler bila dibandingkan dengan mikroprosesor memiliki kemampuan dan segi ekonomis yang bisa diandalkan karena dalam

mikrokontroler sudah terdapat RAM dan ROM. Sedangkan mikroprosesor didalamnya tidak terdapat keduanya. Terlihat bahwa mikrokontroler Atmel AT89S8252 memilki banyak fitur yang menguntungkan. Dipakainya Downloadable flash memori memungkinkan mikrokontroler ini bekerja sendiri tanpa diperlukan tambahan *chip* lainya. Sementara *Flash* memorinya mampu diprogram hingga seribu kali. Hal lain yang menguntungkan adalah system pemrograman menjadi lebih sederhana dan tidak memerlukan rangkaian yang rumit seperti rangkaian untuk memprogram produk Atmel lainya. Secara umum konfigurasi yang dimiliki mikrokontroler AT89S8252 adalah sebagai berikut :

- Sebuah CPU 8 bit dengan menggunakan teknologi dari Atmel.
- 8K byte Downloadable Flash Memori.
- 2K byte EEPROM
- Sebuah *port* serial dengan control *full duplex* UART (Universal Asynchronous Receiver Transmiter.
- 256 byte RAM internal.
- 32 I/O yang dapat dipakai semua.
- 3 buah Timer/Counter 16 bit .
- SPI Serial Interface.
- Programmable Watchdog Timer .
- Dual Data Pointer.
- Frekuensi kerja 0 sampai 24 MHz
- Tegangan operasi 2,7 Volt sampai 6Volt.

- Kemampuan melaksanakan operasi perkalian, pembagian, dan operasi *Bolean* (bit)

Sedangkan untuk blok diagram AT89S8252 diperlihatkan dalam gambar 2-1

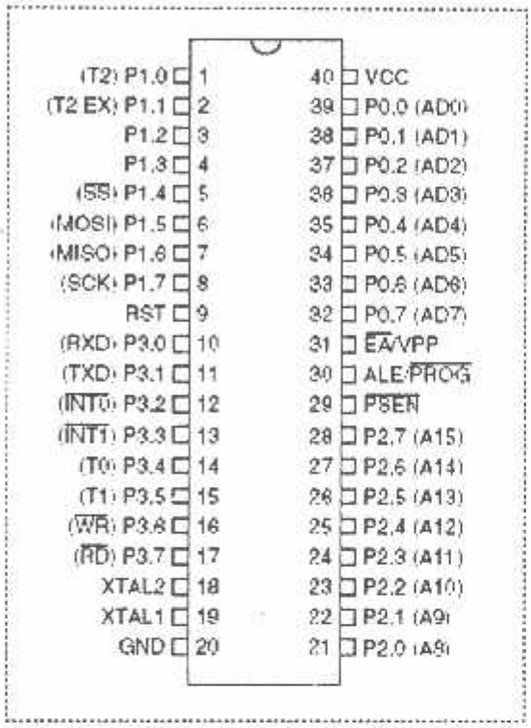


Gambar 2-1 Blok Diagram AT89S8252

Sumber : Data Sheet Mikrokontroller ATMEL AT89S8252

2.1.1. Penjelasan Fungsi Pin AT89S8252

Mikrokontroler AT89S8252 mempunyai 40 pin seperti yang ditunjukkan dalam gambar 2-2 Fungsi-fungsi pin dijelaskan sebagai berikut :



Gambar 2-2 Susunan Pin AT89S8252

Sumber : Data Sheet Mikrokontroller ATMEL AT89S8252

- Pin 1 sampai 8

  Port 1 yang terdiri atas pin 1 sampai 8 merupakan saluran masukan/keluaran dua arah.

- Pin 9

  RST merupakan saluran dua masukan untuk me*reset* mikrokontroler dengan cara memberi masukan logika tinggi.

- Pin 10 sampai 17

  Port 3 yang terdiri atas pin 10 sampai pin 17 merupakan saluran masukan/keluaran dua arah dan mempunyai fungsi khusus seperti yang terlihat dalam tabel 2-1

- Pin 18 dan 19

  $XTAL_1$ dan $XTAL_2$ merupakan saluran untuk mengatur pewktuan system. Untuk pewaktuan dapat menggunakan pewaktuan internal maupun eksternal .

- Pin 20

  Vss merupakan hubungan ke *ground* dari rangkaian.

- Pin 21 sampai 28

  Port 2 yang terdiri atas pin 21 sampai 28 merupakan saluran masukan/keluaran dua arah. *Port* ini mengeluarkan 8 bit bagian alamat tinggi (A8-A15) selama pengambilan instruksi dari memori program eksternal dan pengambilan data memori eksternal yang menggunakan mode pengalamatan 16 bit.

- Pin 29

  PSEN (*Program Store Enable*) merupakan sinyal baca untuk mengaktifkan memori program eksternal.

- Pin 30

  ALE/PROG (*Address Latch Enable*) merupakan pulsa yang berfungsi untuk menahan alamat rendah (A0-A7) dalam *port* 0, selama proses baca/tulis memori eksternal. Frekuensi ALE adalah 1/6 kali frekuensi

osilator, dan digunakan sebagai pewaktu. Pin ini juga berfungsi sebagai saluran program selama dilakukan pemrograman jika menggunakan memori program eksternal.

- Pin 31

  EA/VPP (*External Access Enable*) untuk mengatur penggunaan memori program eksternal dan internal. Pin ini harus dihubungkan dengan *ground* bila menggunakan memori program eksternal dan dihubungkan dengan VPP sebesar 12 Volt jika menggunakan memori program eksternal.

- Pin 32 sampai 39

  Port 0 yang terdiri atas pin 32 sampai 39 merupakan saluran masukan/keluaran. *Port* 0 merupakan saluran alamat rendah (A0-A7) yang dimultipleks dengan saluran *bus* data (D0-D7).

- Pin 40

  Vcc merupakan saluran masukan untuk catu daya positif sebesar 5 Volt DC dengan toleransi kurang lebih 10 %.

2.1.2. Masukan dan Keluaran

Untuk masukan dan keluaran terdapat 4 buah *port* yang masing-masing 8 bit. Saluran ini bersifat dua arah (*bidirectional*) yang berarti dapat difungsikan sebagai masukan atau keluaran, serta dapat dialamati per bit. *Port* 3 selain digunakan sebagai *port* masukan dan keluaran juga dapat digunakan sebagai fungsi pengganti sebagaimana yang terdapat dalam tabel 2-1.

Sedangkan AT89S8252 memiliki fitur tambahan yang terdapat pada *port 1* seperti pada tabel 2-2.

Tabel 2-1 Fungsi Pengganti *Port 3*

Port Pin	Alternate Functions
P3.0	RXD (serial input port)
P3.1	TXD (serial output port)
P3.2	$\overline{INT0}$ (external interrupt 0)
P3.3	$\overline{INT1}$ (external interrupt 1)
P3.4	T0 (timer 0 external input)
P3.5	T1 (timer 1 external input)
P3.6	$\overline{WR}$ (external data memory write strobe)
P3.7	$\overline{RD}$ (external data memory read strobe)

Sumber : Data Sheet Mikrokontroller ATMEL AT89S8252

Tabel 2-2 Fungsi khusus pada *port 1* AT89S8252

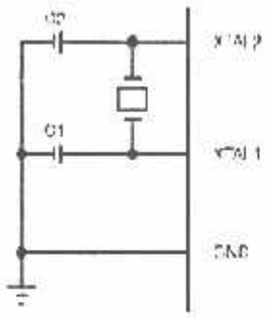
Port Pin	Alternate Functions
P1.0	T2 (external count input to Timer/Counter 2, clock-out
P1.1	T2EX (Timer/Counter 2 capture/reload trigger and direction control)
P1.4	$\overline{SS}$ (Slave port select input)
P1.5	MOSI (Master data output, slave data input pin for SPI channel)
P1.6	MISO (Master data input, slave data output pin for SPI channel)
P1.7	SCK (Master clock output, slave clock input pin for SPI channel)

Sumber : Data Sheet Mikrokontroller ATMEL AT89S8252

2.1.3. Osilator

Jantung dari AT89S8252 adalah rangkaian yang membangkitkan pulsa clock yang mesinkronkan semua operasi internal. Mikrokontroler AT89S8252 memiliki osilator internal (*on chip oscillator*) yang dapat digunakan sebagai sumber pewaktu (*clock*) bagi CPU. Untuk menggunakan internal diperlukan

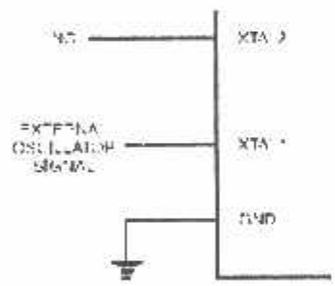
sebuah kristal atau resonator keramik antara pin XTAL1 dan pin XTAL2 dan sebuah kapasitor ke *ground*. Konfigurasinya dapat dilihat pada gambar berikut.



Gambar 2-3 Konfigurasi Osilator Menggunakan Kristal
Sumber : Data Sheet Mikrokontroller ATMEL AT89S8252

Nilai C1 dan C2 adalah 10 pF – 30 pF bila menggunakan kristal, dan bernilai 10 pF – 40 pF bila menggunakan resonator keramik.

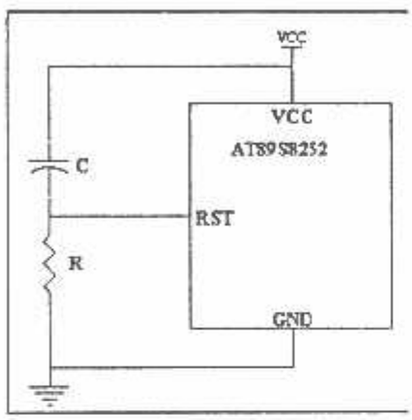
Untuk penggunaan dengan external clock, XTAL2 harus dibiarkan dalam kondisi tidak terhubung. Konfigurasinya dapat dilihat pada gambar berikut ini :



Gambar 2-4 Konfigurasi Osilator Menggunakan External Oscilator Signal
Sumber : Data Sheet Mikrokontroller ATMEL AT89S8252

2.1.4. Reset

Rangkaian *power on reset* diperlukan untuk me*reset* mikrokontroler secara otomatis setiap catu daya *on*. Gambar 2-5 menunjukkan rangkaian *power on reset*. Ketika catu daya diaktifkan, rangkaian *reset* menahan logika tinggi pin RST dengan jangka waktu yang ditentukan oleh besarnya pengisian muatan C.



Gambar 2-5 Rangkaian *Power On Reset*

Sumber : Data Sheet Mikrokontroller ATMEL AT89S8252

2.1.5. Data Memori (EEPROM) Dan RAM

Berbeda dengan mikrokontroler standard MCS-51, mikrokontroler Atmel AT89S8252 juga dilengkapi dengan data memori yang berupa EEPROM (*Electrically Erasable Programmable Read Only Memory*). EEPROM yang dimaksud ini besarnya 2 *kilo byte* (2K) dan dipakai untuk penyimpanan data.

EEPROM *on-chip* ini diakses dengan mengeset bit EEMEN pada register WMCON pada alamat 96H. Alamat EEPROM ini adalah 000H sampai 7FFH. Intruksi move digunakan untuk mengakses EEPROM internal ini. Bit EEMWE pada register WMCON harus diset ke-1 sebelum seberang lokasi pada EEPROM dapat ditulisi. Program pengguna harus *mereset* bit EEMWE ke '0'jika proses

ABSTRAKSI

PERENCANAAN DAN PEMBUATAN MASTER KONTROL LAB. BAHASA DELAPAN CHANNEL BERBASIS MIKROKONTROLLER AT89S8252

(Nama : Isnaini Rozafi, NIM : 01. 17. 044, Teknik Elektronika S1)
(Dosen Pembimbing : Joseph Dedi Irawan ST., MT.)

Pada perkembangan teknologi saat ini pada bidang pendidikan, sekarang ini sedang tren adanya Laboratorium Bahasa guna pembelajaran-pembelajaran bahasa, baik bahasa asing ataupun bahasa dalam negeri, maka dengan adanya Laboratorium Bahasa, seorang siswa atau pemakai dapat belajar lebih mudah dan fleksibel, guna memudahkan para pengajar dalam hal penyampaian pelajarannya.

Selain itu, dengan adanya Laboratorium Bahasa, suatu instansi baik instansi negeri ataupun instansi swasta dapat menambah bobot (pandangan atau gengsi), sehingga dengan adanya Laboratorium Bahasa diharapkan dapat menarik minat masyarakat, khususnya calon siswa.

Laboratorium Bahasa sekarang ini banyak dibutuhkan oleh para pengajar, khususnya pada bidang bahasa, seperti pada tempat kursusan, sekolahan, lembaga penelitian, kampus, kantor dan lain sebagainya. Maka dengan adanya latar belakang itu, maka penulis mencoba untuk mengajukannya dengan judul Perencanaan Dan Pembuatan Master Kontrol Lab. Bahasa Delapan Channel Berbasis Mikrokontroller AT89S8252, disamping sebagai pembelajaran, penulis juga ingin cepat lulus kuliah karena pengajuan skripsi sebagai prasyarat lulus sarjana.

DAFTAR ISI

LEMBAR PERSETUJUAN ..... **i**

KATA PENGANTAR ..... **ii**

ABSTRAKSI ..... **iv**

DAFTAR ISI ..... **v**

DAFTAR GAMBAR ..... **viii**

DAFTAR TABEL ..... **x**

BAB I PENDAHULUAN **1**

1.1. Latar Belakang 1

1.2. Rumusan Masalah 2

1.3. Tujuan Pembahasan 2

1.4. Metodologi 3

1.5. Batasan Masalah 3

1.6. Sistematika Penulisan 4

BAB II LANDASAN TEORI **5**

2.1. Mikrokontroller AT89S8252 5

2.1.1. Penjelasan Fungsi Pin 8

2.1.2. Masukan dan Keluaran 6

2.1.3. Osilator 7

2.1.4. Reset 13

2.1.5. Data Memori dan Ram 13

2.1.6. Spesial Function Register (SFR) 15

2.1.7. Timer dan Counter 17

2.1.8. Idle Mode 19

2.2. Relay 20

2.3. Op-Amp 21

2.3.1. Penguat Inverting 21

2.3.2. Rangkaia Summing Inverting 23
2.4. LM741 24
2.5. Switch Elektronik 25
BAB III PERENCANAAN DAN PEMBUATAN ALAT 26
3.1. Sistematik Secara Diagram Blok 26
3.2. Rangkaian Pre-Amp Mic 29
3.3. Mixer 29
3.4. Driver Relay 30
3.5. Mikrokontroller AT89S8252 32
3.6. Flowchart 33
BAB IV PENGUJIAN ALAT 35
4.1. Umum 35
4.2. Pengujian Rangkaian Pre-Amp Mic 35
4.3. Pengujian Rangkaian Mixer 38
4.4. Pengujian Seluruh Sistem 41
BAB V PENUTUP 46
5.1. Kesimpulan 46
5.2. Saran-saran 46
DAFTAR PUSTAKA
LAMPIRAN

DAFTAR GAMBAR

Gambar 2.1 Blok Diagram AT89S8252 7
Gambar 2.2 Susunan Pin AT89S8252 9
Gambar 2.3 Konfigurasi Osilator Menggunakan Kristal 12
Gambar 2.4 Konfigurasi Osilator Menggunakan External Osc. Kristal 12
Gambar 2.5 Rangkaian Power On Reset 13
Gambar 2.6 Memori Data Internal 14
Gambar 2.7 Rangkaian Relay 21
Gambar 2.8 Rangkaian Inverting 22
Gambar 2.9 Rangkaian Summing Inverting 23
Gambar 2.10 Konfigurasi Pin-pin I.M 741 24
Gambar 2.11 Konfigurasi Pin-pin 4049 25
Gambar 3.1 Blok Diagram Rangkaian 28
Gambar 3.2 Rangkaian Pre-Amp mic 29
Gambar 3.3 Rangkaian Mixer 30
Gambar 3.4 Rangkaian Mikrokontroller 32
Gambar 3.5 Flowchart 33
Gambar 4.1 Pengujian Rangkaian Pre-Amp mic 36
Gambar 4.2 Pengujian Rangkaian Mixer 39

DAFTAR TABEL

Tabel 2.1 Fungsi Pengganti port 3 11
Tabel 2.2 Fungsi Khusus pada Port 1 11
Tabel 2.3 Mode Operasi Timer/Counter 0 dan 1 17
Tabel 2.4 Mode Operasi Timer 2 18
Tabel 2.5 Alamat Sumber Interupsi 20
Tabel 2.6 Fungsi-fungsi pin-pin LM 741 25
Tabel 4.1 Hasil Pengukuran Pre-Amp Mic 38
Tabel 4.2 Hasil Pengukuran Rangkaian Mixer 40
Tabel 4.3 Hasil Pengujian Tombol Individu 42
Tabel 4.4 Hasil Penguian Tombol CALL 43
Tabel 4.5 Hasil Pengujian Tombol A (Ganjil) 44
Tabel 4.6 Hasil Pengujian Tombol B (Genap) 45

DAFTAR PUSTAKA

- Data Sheets AT89S8252 http://www.atmel.com
- Wasito S. Vademekum Elektronika Edisi Kedua, Penerbit PT. Gramedia Pustaka Utama, Jakarta, 2004
- Agfianto Eko Putra, Belajar Mikrokontroller AT89C51/52/55, Penerbit Gava Media, Yogyakarta

LAMPIRAN

BAB V
PENUTUP

5.1 Kesimpulan

Dari percobaan dan pengujian, didapatkan kesimpulan sebagai berikut :

- Penggunaan relay pada rangkaian *audio* yang dekat dengan *audio amplifier* dapat menghasilkan suara dengung (*noise*).
- Pada sistem *audio* sebaiknya menggunakan kabel jenis *scarm* untuk input dan output rangkaian *audio* guna meredam noise akibat *fluksi* dari trafo.
- untuk mendapatkan sistem *audio* yang bagus, sebaiknya sistem *ground* terhubung dengan baik pada bodi dan rangkaian serta pada kabel *power* sebaiknya menggunakan kabel besar, guna mendapatkan nilai *resistansi* yang lebih kecil.

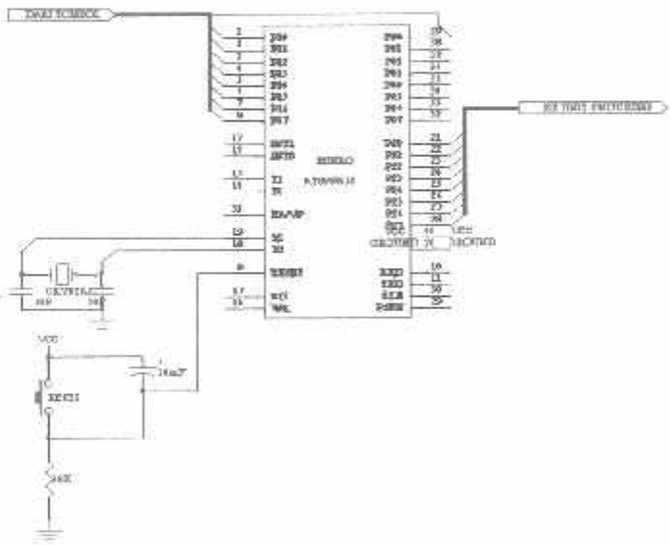
5.2. Saran-saran

1. Agar siswa dapat dengan mudah dalam menggunakannya, dapat ditambahkan suatu tampilan, seperti LCD ataupun dapat dihubungkan ke PC agar lebih canggih, mengikuti perkembangan zaman.
2. Guna pengembangan yang lebih lanjut, dapat ditambahkan beberapa fitur yang dapat membantu dalam pengoperasiannya seperti sistem kuis maupun pada ruang seminar agar lebih efisien.

3.5. Mikrokontroller AT89S8252

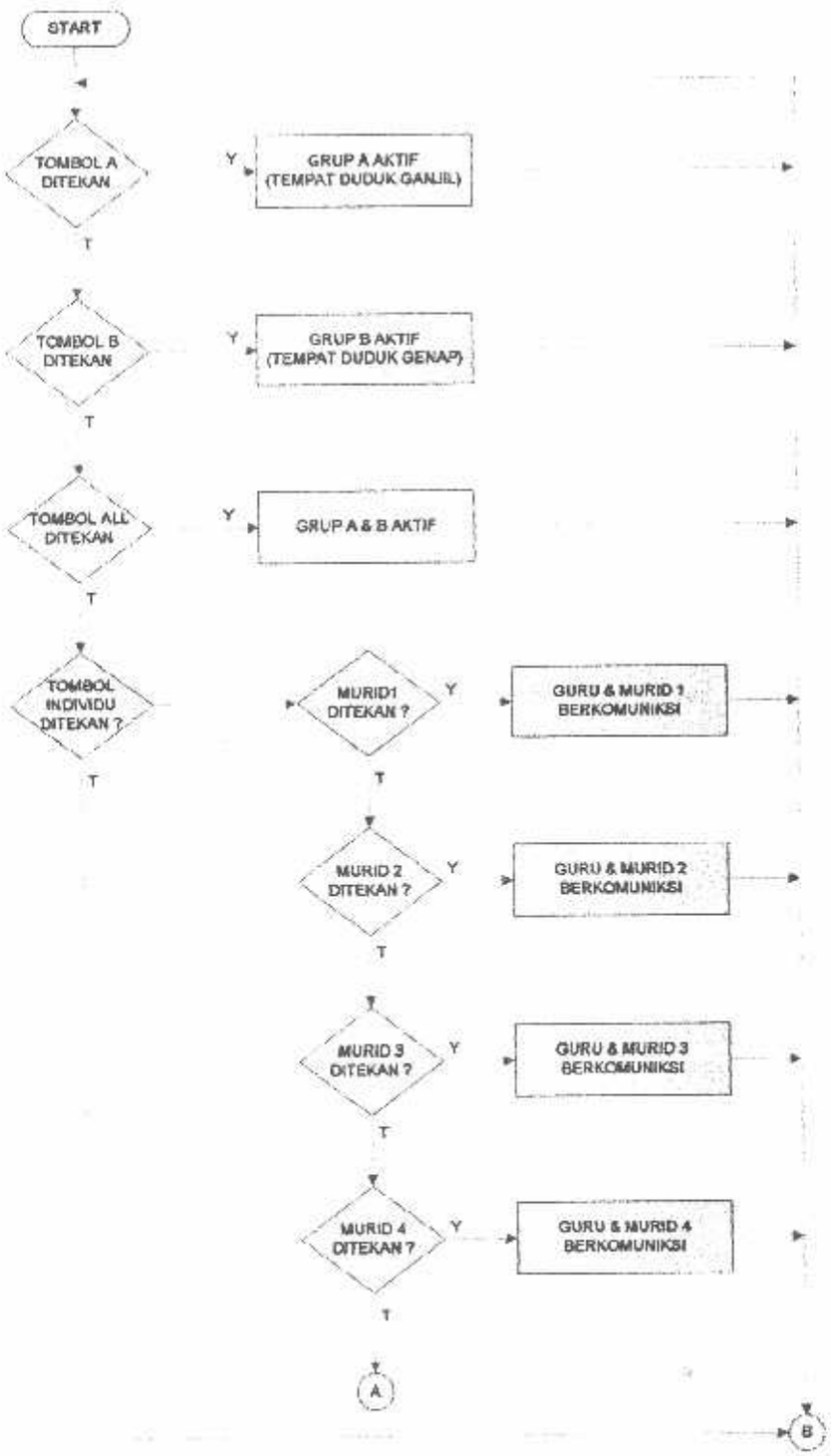
Disini rangkaian mikrokontroller berfungsi sebagai pengolah data dan pengendali alat agar sistem dapat bekerja dengan optimal, maka dalam perancangan alat ini pin-pin yang akan digunakan sebagai berikut :

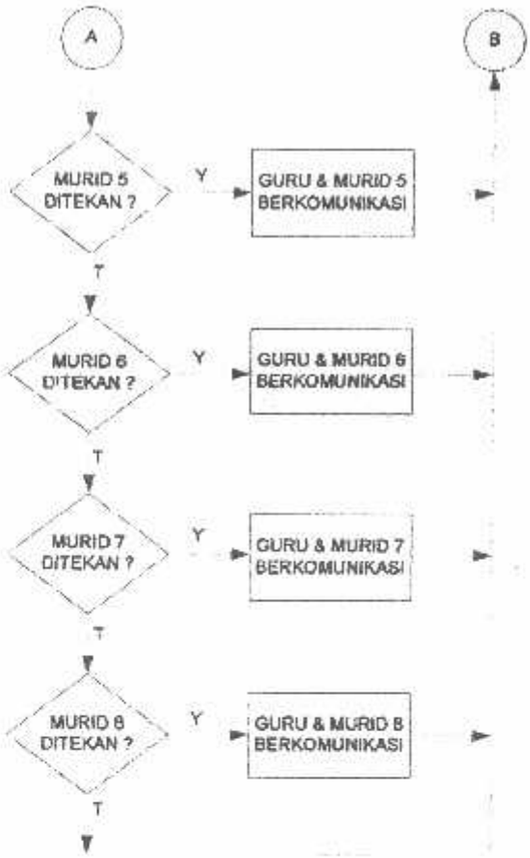
- Port 1.0-1.7 digunakan sebagai inputan dari tombol
- Port 0.0-0.7 digunakan sebagai outputan menuju relay
- Port 18 dan 19 sebagai rangkaian clock
- Port 9 sebagai reset



Gambar 3-4Rangkaian Mikrokontroller

3.6. Flowchart




A
B
MURID 5 DITEKAN ?
Y
GURU & MURID 5 BERKOMUNIKASI
T
MURID 6 DITEKAN ?
Y
GURU & MURID 6 BERKOMUNIKASI
T
MURID 7 DITEKAN ?
Y
GURU & MURID 7 BERKOMUNIKASI
T
MURID 8 DITEKAN ?
Y
GURU & MURID 8 BERKOMUNIKASI
T

BAB IV

PENGUJIAN ALAT

4.1. Umum

Dalam bab ini akan dibahas tentang pengujian alat yang telah dibuat berdasarkan perencanaan dan pembuatan. Maksud dan tujuan pengujian alat ini adalah untuk mengetahui apakah alat yang telah direncanakan dan dibuat dapat bekerja dengan baik.

Pengujian alat ini meliputi pengujian terhadap :

1. Pengujian rangkaian pre-amp mic
2. Pengujian rangkaian mixer
3. pengujian rangkaian IC switch
4. Pengujian seluruh sistem.

4.2. Pengujian Rangkaian Pre-amp mic.

Tujuan pengujian pre-amp mic adalah untuk mengetahui besarnya penguatan dengan cara mengukur Vout dari pre-amp mic. Penguatan telah ditentukan sebesar 50 kali.

Peralatan yang digunakan antara lain catu daya, multimeter digital dan variabel resistor. Pengujian penguatan dapat dilakukan dengan menggunakan multimeter digital yang berfungsi untuk mengetahui besarnya nilai Vout dari pre-amp

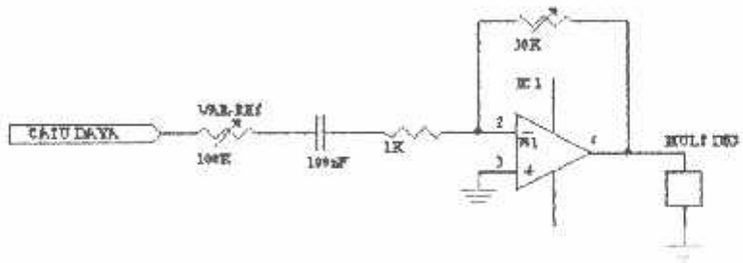
mic. Dengan menentukan besarnya penguatan sebesar 50 kali, maka Rf dapat dicari dengan rumus :

Vout = Av X Vin

Av = Rf/R1

50 = Rf/1K

Bila ditentukan R1 = 1K, maka Rf = 50K



Gambar 4.1.

Pengujian rangkaian pre-amp mic.

Langkah-langkah pengujian pre-amp mic dengan menggunakan multimeter digital adalah sebagai berikut :

1. menyiapkan rangkaian seperti gambar, serta memastikan bahwa catudaya telah terpasang dan hubungan rangkaian telah benar.
2. Setelah susunan dan hubungan antar rangkaian telah benar, aktifkan sumber tegangan
3. Gunakan multimeter digital untuk mengetahui tegangan pada Vout pre-amp mic.

Tabel 4-1

Hasil Pengukuran Pre-Amp Mic

Vin (mV)	Vout (V)	AV (kali)
20,45	0,95	46,89
31,66	1,50	47,51
40,80	2,03	49,79
52,30	2,57	49,32
61,68	3,07	49,83

Dari pengujian didapat hasil seperti dalam tabel 4-1, dari data telah ditentukan besarnya penguatan sebesar 50 kali, maka untuk melihat prosentase kesalahan dari penguatan digunakan rumus :

$$Error = \frac{perencanaan - pengukuran}{perencanaan} x100\%$$

$$Error1 = \frac{50 - 46,89}{50} x100\%$$

$$= 6,22\ \%$$

$$Error2 = \frac{50 - 47,51}{50} x100\%$$

$$= 4,98\ \%$$

$$Error3 = \frac{50 - 49{,}79}{50} x100\%$$

$$= 0{,}42\ \%$$

$$Error4 = \frac{50 - 49{,}32}{50} x100\%$$

$$= 1{,}36\ \%$$

$$Error5 = \frac{50 - 49{,}83}{50} x100\%$$

$$= 0{,}34\ \%$$

Dari data diatas idaatkan error rata-rata sebesar :

$$\frac{6{,}22 + 4{,}98 + 0{,}42 + 1{,}36 + 0{,}34}{5} = 2{,}66\%$$

dan penguatan rata-rata sebesar :

$$\frac{46{,}89 + 47{,}51 + 49{,}79 + 49{,}32 + 49{,}83}{5} = 48{,}66 \text{ kali}$$

4.3. Pengujian rangkaian mixer

Tujuan pengujian rangkaian mixer adalah untuk mengetahui besarnya penjumlahan dengan mengukur Vout dari mixer. Penjumlahan ditentukan untuk penguatan yang pertama sebesar 1 kali dan untuk penguatan yang kedua sebesar 5 kali.

Peralatan yang digunakan antara lain catu daya, variable resistor dan multimeter digital. Pengujian penguatan dapat dilakukan dengan cara menggunakan multimeter digital untuk mengetahui nilai Vout dari mixer. Dengan menentukan

besarnya penguatan pertama sebesar 1 kali dan penguatan yang kedua sebesar 5 kali, maka untuk penguatan yang pertama digunakan rumus :

$$Vout1 = - \frac{Vin1}{Rin1} xRf1$$

$$AV = - \frac{Rf1}{Rin1}$$

$$= \frac{Vout1}{Vin1}$$

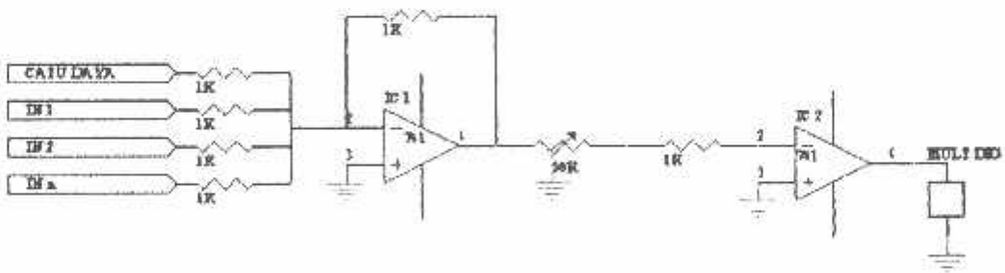
Bila ditentukan R1 = 1K, maka Rf = 1K

Sedangkan untuk penguatan yang kedua sebesar 5 kali menggunakan rumus :

$$Vout2 = - \frac{Vin2}{Rin2} xRf2$$

$$AV = - \frac{Rf2}{Rin2}$$

$$= \frac{Vout1}{Vin1}$$



Gambar 4.2.

Pengujian Rangkaian Mixer.

Tabel 4-2.

Hasil pengukuran rangkain mixer

Vin (mV)	Vout (mV)	AV (kali)
21,24	61,38	2,89
30,90	90,53	2,93
39,68	114,27	2,88
50,41	146,69	2,91
59,96	175,08	2,92

Dari pengujian didapat hasil seperti dalam tabel 4-2, dari data telah ditentukan besarnya penguatan sebesar 3 kali, maka untuk melihat prosentase kesalahan dari penguatan digunakan rumus :

$$Error = \frac{perencanaan - pengukuran}{perencanaan} x100\%$$

$$Error1 = \frac{3 - 2,89}{3} x100\%$$

$$= 3,6\ \%$$

$$Error2 = \frac{3 - 2,93}{3} x100\%$$

$$= 2,3\ \%$$

$$Error3 = \frac{3 - 2,88}{3} x100\%$$

$$= 4\ \%$$

$$Error4 = \frac{3 - 2,91}{3} x100\%$$

$$= 3\ \%$$

$$Error5 = \frac{3 - 2,92}{3} x100\%$$

$$= 2,6\ \%$$

Dari data diatas didapatkan error rata-rata sebesar :

$$\frac{3,6 + 2,3 + 4 + 3 + 2,6}{5} = 3,10\%$$

sedangkan penguatan rata-ratanya didapat :

$$\frac{2,89 + 2,93 + 2,88 + 2,91 + 2,92}{5} = 2,90 \text{ kali}$$

4.4. Pengujian seluruh sistem

Tujuan pengujian seluruh sistem adalah untuk mengetahui apakah sistem telah bekerja sesuai dengan apa yang diharapkan, langkah-langkah pengujian seluruh sistem adalah dengan mempersiapkan semua rangkaian, kemudian melihat hasil keluaran yang ditampilkan melalui lampu led maupun output audionya.

Tabel 4-3

Hasil pengujian tombol individu saat menu individu ON

IND	Kondisi Led							
	1	2	3	4	5	6	7	8
1	ON	OFF	OFF	OFF	OFF	OFF	OFF	OFF
2	OFF	ON	OFF	OFF	OFF	OFF	OFF	OFF
3	OFF	OFF	ON	OFF	OFF	OFF	OFF	OFF
4	OFF	OFF	OFF	ON	OFF	OFF	OFF	OFF
5	OFF	OFF	OFF	OFF	ON	OFF	OFF	OFF
6	OFF	OFF	OFF	OFF	OFF	ON	OFF	OFF
7	OFF	OFF	OFF	OFF	OFF	OFF	ON	OFF
8	OFF	OFF	OFF	OFF	OFF	OFF	OFF	ON

Tabel 4-4

Hasil pengujian tombol CALL

IND	Kondisi Led (berkedip)							
	1	2	3	4	5	6	7	8
1	ON	OFF	OFF	OFF	OFF	OFF	OFF	OFF
2	OFF	ON	OFF	OFF	OFF	OFF	OFF	OFF
3	OFF	OFF	ON	OFF	OFF	OFF	OFF	OFF
4	OFF	OFF	OFF	ON	OFF	OFF	OFF	OFF
5	OFF	OFF	OFF	OFF	ON	OFF	OFF	OFF
6	OFF	OFF	OFF	OFF	OFF	ON	OFF	OFF
7	OFF	OFF	OFF	OFF	OFF	OFF	ON	OFF
8	OFF	OFF	OFF	OFF	OFF	OFF	OFF	ON

Tabel 4-5

Hasil pengujian tombol A (ganjil)*

A	Kondisi Audio							
	1	2	3	4	5	6	7	8
1	ON	OFF	OFF	OFF	OFF	OFF	OFF	OFF
2	OFF	OFF	OFF	OFF	OFF	OFF	OFF	OFF
3	OFF	OFF	ON	OFF	OFF	OFF	OFF	OFF
4	OFF	OFF	OFF	OFF	OFF	OFF	OFF	OFF
5	OFF	OFF	OFF	OFF	ON	OFF	OFF	OFF
6	OFF	OFF	OFF	OFF	OFF	OFF	OFF	OFF
7	OFF	OFF	OFF	OFF	OFF	OFF	ON	OFF
8	OFF	OFF	OFF	OFF	OFF	OFF	OFF	OFF

Tabel 4-6

Hasil pengujian tombol B (genap)*

B	Kondisi Audio							
	1	2	3	4	5	6	7	8
1	OFF	OFF	OFF	OFF	OFF	OFF	OFF	OFF
2	OFF	ON	OFF	OFF	OFF	OFF	OFF	OFF
3	OFF	OFF	OFF	OFF	OFF	OFF	OFF	OFF
4	OFF	OFF	OFF	ON	OFF	OFF	OFF	OFF
5	OFF	OFF	OFF	OFF	OFF	OFF	OFF	OFF
6	OFF	OFF	OFF	OFF	OFF	ON	OFF	OFF
7	OFF	OFF	OFF	OFF	OFF	OFF	OFF	OFF
8	OFF	OFF	OFF	OFF	OFF	OFF	OFF	ON

*) ket : Untuk rangkaian tombol A dan B yang ON/OFF adalah sistem audionya, bukan masalah tentang lampu lednya.

Dari pengujian seluruh sistem apat disimpulkan bahwa sistem telah bekerja sesuai dengan yang diharapkan.

BAB III

PERENCANAAN DAN PEMBUATAN ALAT

Pada bab ini akan dibahas mengenai peralatan yang direncanakan dan akan direalisasikan sebagaimana fungsinya. Adapun perencanaan dan pembuatan alat meliputi: perencanaan dan pembuatan perangkat keras serta perencanaan dan pembuatan perangkat lunak secara garis besarnya.

3.1 Sistematik Secara Diagram Blok

Keterangan dari blok-blok diagram sebagai berikut :

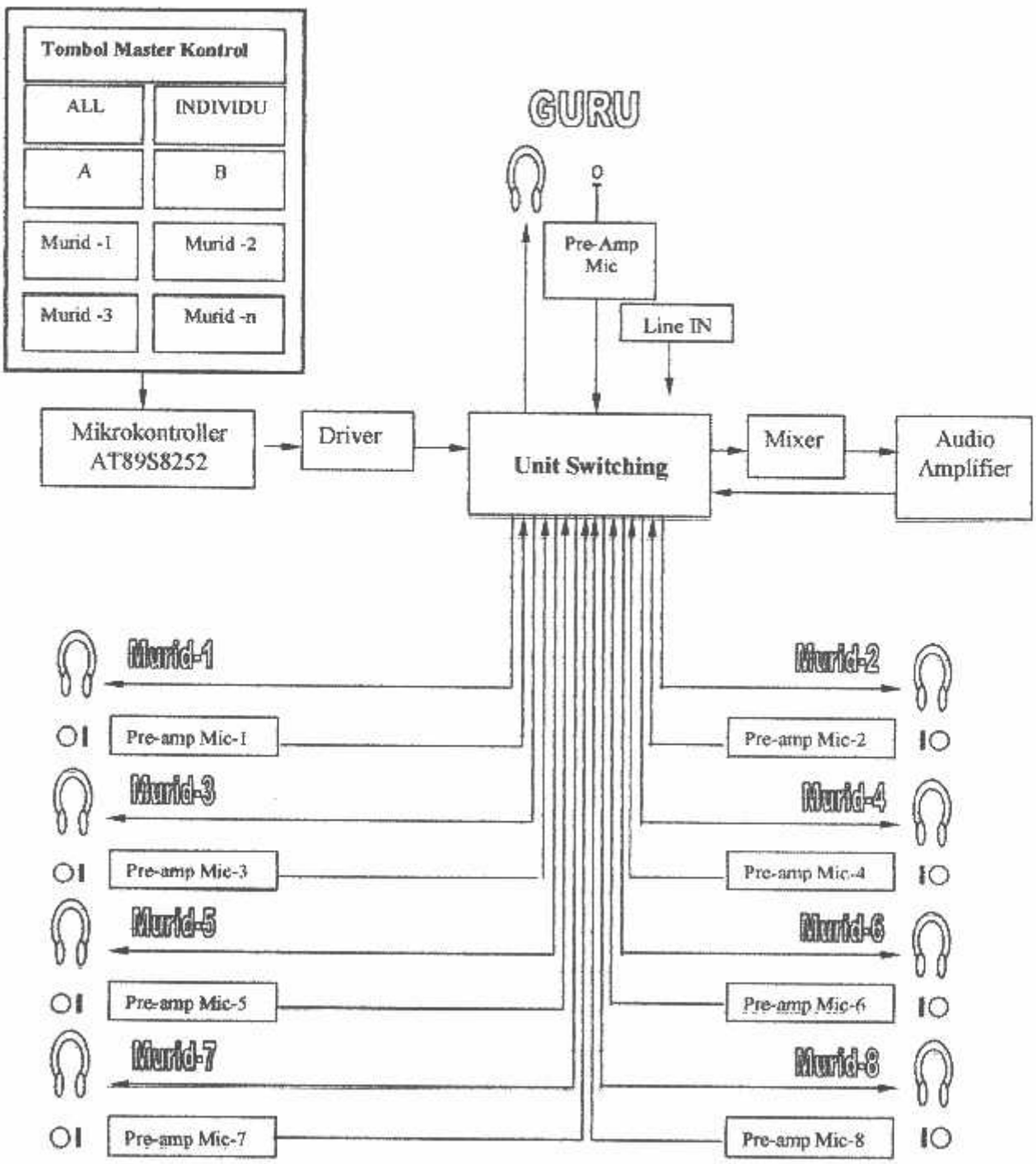
- Tombol Master Kontrol sebagai menjalankanataupun memadamkan suatu instruksi

Ada beberapa tombol yang terdapat pada panel master kontrol, diantaranya :

- Tombol Power sebagai menghidupkan ataupun mematikan master kontrol.
- Tombol All sebagai komunikasi antara guru dengan seluruh murid.
- Tombol Individu, guru dapat berkomunikasi dengan salah satu obyek, sesuai dengan keinginan sang guru.
- Tombol A, hanya murid yang mempunyai nomor/tempat duduk ganjil saja yang dapat berkomunikasi dengan guru.
- Tombol B, hanya murid yang mempunyai nomor/tempat duduk genap saja yang dapat berkomunikasi dengan guru.
- Tombol Murid, untuk komunikasi guru dengan murid sesuai dengan instruksi tombol yang sudah ada.

- Mikrokontroller sebagai pengendali keseluruhan sistem, mikrokontroller akan memproses data inputan sesuai dengan instruksi yang masuk serta mengendalikan output yang kita inginkan.
- Driver sebagai rangkaian penghubung antara mikrokontroller dengan unit switching.
- Unit Switching sebagai penghubung ataupun pemutus audio antara guru dengan murid sesuai dengan instruksi.
- Mixer sebagai pencampur audio dari guru dan murid.
- Audio Amplifier sebagai penguat suara.
- Line IN sebagai inputan dari tape recorder ataupun vcd.

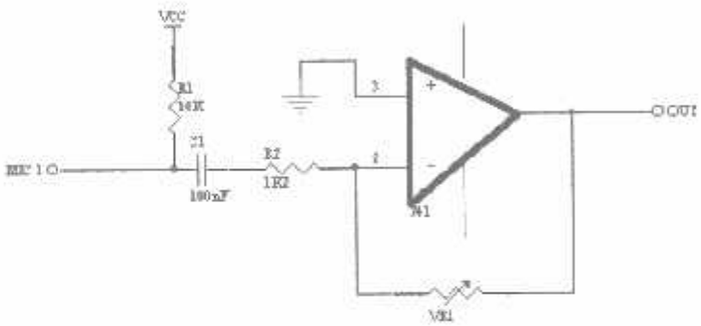
Adapun Blok Diagram dari alat sebagai berikut :



Gambar 3-1 Blok Diagram Ragkaian

3.2 Rangkaian Pre-Amp Mic

Pre-Amp Mic difungsikan sebagai penguat bagi mic condenser, rangkaian dasar pre-amp mic adalah rangkaian penguat inferting seperti gambar di bawah ini



Gambar 3-2 Rangkaian Pre-Amp Mic

Dari rangkaian diatas ditentukan besranya penguatan sebesar 50 kali dengan menggunakan rumus : $A = -(VR1/R2)$

$50 = -(VR1/1K)$

$VR1 = 50 \times 1K$

$= 50\ K$

3.2 Mixer

Mixer disini difungsikan sebagai pencampur semua masukan dari pre-amp mic. Rangkaian mixer mnggunakan penguat op-amp jenis *summing* yang dikaskadekan dengan penguat inverting, dimana dalam rangkain ini untuk penguatan op-amp yang pertama sebesar 1 kali dan untuk op-amp yang kedua sebesar 3 kali. Dan bila Ri1 ditentukan 1KΩ maka Rf dapat dicari melalui rumus, dapatlah ditentukan A_V 1 kali dan Ri sebesar 1 KΩ, maka untuk mencari Rf yaitu :

$A_V = Rf/Ri$

$Rf = A_V \times Ri$

$= 1 \times 1K, \quad = 1K\Omega$

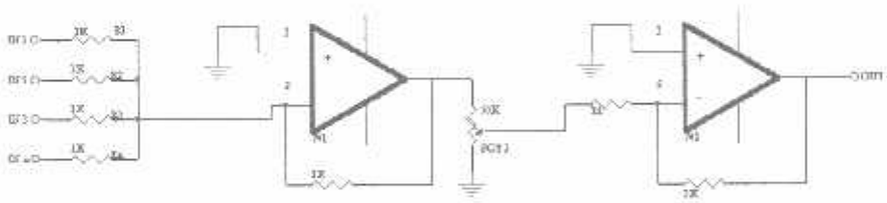
Sedangkan untuk A_{V2} ditentukan sebesar 3 kali dan Ri ditentukan 1KΩ, maka untuk mencari Rf adalah sebagai berikut :

$Rf \quad = A_V \times Ri$

$= 3 \times 1K$

$= 3K\Omega$

jadi untuk rangkaian mixer adalah sebagai berikut :



Gambar 3-3 Rangkaian Mixer

3.4. Driver Relay

Sebelum masuk ke relay diperlukan rangkaian pengendali relay yang berfungsi untuk mengendalikan posisi relay, dioda yang dipararel dengan relay berfungsi untuk mencegah timbulnya tegangan lebih pada transistor penerima pada saat transistor dalam keaaan tidak aktif. Transistor yang digunakan adalah BD 139 dengan datasheet sebagai berikut :

- BD 139
- hfe = 100
- VBE = 0,7 Volt

Agar relay dapat bekerja, transistor pada kondisi saturasi, sehingga apat dicari nilai Ic-nya, yaitu :

$$Ic = \frac{Vcc}{Rl(relay)}$$
$$= \frac{12}{360}$$
$$= 33{,}3mA$$

Maka pada saat jenuh (saturasi) besar arus Ib adalah :

$$Ib = \frac{Ic}{hfe}$$
$$= \frac{33{,}3mA}{100}$$
$$= 0{,}33mA$$

dengan demikian, harga RB dapat dicari jika nilai Vcc = 5 V0lt, Vbe = 0,7 Volt, yaitu :

$$RB = \frac{Vcc - Vbe}{Ib}$$
$$= \frac{5 - 0{,}7}{0{,}33mA}$$
$$= 13K$$

BAB I
PENDAHULUAN

1.1 Latar Belakang

Perkembangan ilmu di bidang teknologi, khususnya teknologi elektronika merupakan suatu kenyataan yang menunjukkan bahwa manusia didalam melakukan aktifitasnya. Sesuai dengan tuntutan jaman yang semakin modern telah membawa ide-ide ke arah teknologi yang lebih maju, lebih bermanfaat serta memiliki nilai ekonomis.

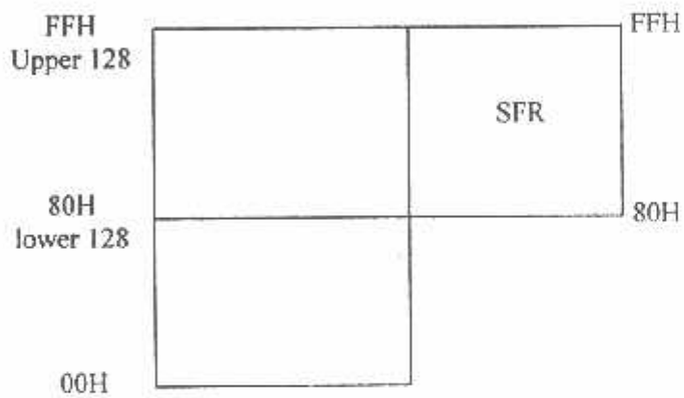
Oleh karena itu berbagai macam sebab perkembangan teknologi khususnya dibidang elektronika mempengaruhi pola kehidupan masyarakat yang dulunya memanfaatkan tenaga murni (tenaga manusia itu sendiri) kini berubah menggunakan suatu alat yang dapat bekerja sendiri yang hanya membutuhkan sedikit sentuhan tenaga manusia.

Seperti pada perkembangan teknologi saat ini pada bidang pendidikan, sekarang ini sedang tren adanya Laboratorium Bahasa guna pembelajaran-pembelajaran bahasa, seperti bahasa asing ataupun bahasa dalam negeri, sehingga dengan adanya Laboratorium Bahasa, seorang siswa atau pemakai dapat belajar lebih mudah dan fleksibel, guna memudahkan para pengajar dalam hal penyampaian pelajarannya.

Selain itu, dengan adanya Laboratorium Bahasa, suatu instansi baik instansi negeri ataupun instansi swasta, dapat menambah bobot (pandangan atau gengsi), maka dengan adanya Laboratorium Bahasa diharapkan dapat menarik minat masyarakat, khususnya calon siswa.

penulisan ke EEPROM tidak diperlukan lagi. Proses penulisan ke EEPROM dapat dilihat dengan membaca bit RDY/BSY pada SFR WMCON. Jika bit ini berlogika rendah maka berarti penulisan EEPROM sedang berlangsung, jika bit ini berlogika tinggi berarti penulisan sudah selesai dan penulisan lain dapat dimulai lagi.

Sedangkan RAM yang ada pada mikrokontroler AT89S8252 adalah berkapasitas 256 *byte* dan kompatibel dengan RAM yang ada pada mikrokontroler standard MCS-51.



Gambar 2-6. Memori Data *Internal* (RAM)
Sumber : Data Sheet Mikrokontroller ATMEL AT89S8252

Pada *lower* 128 lokasi memori dibagi menjadi 3 bagian :

1. Register bank 0 – 3

   Lokasi bank register dimulai dari alamat 00H – 1 H yang terdiri dari 32 *bytes*. Register bank ini terdiri dari 4 buah register 8 bit yang dapat dipilih melalui pengaturan *program status word* register.

2. Bit *Addressing*

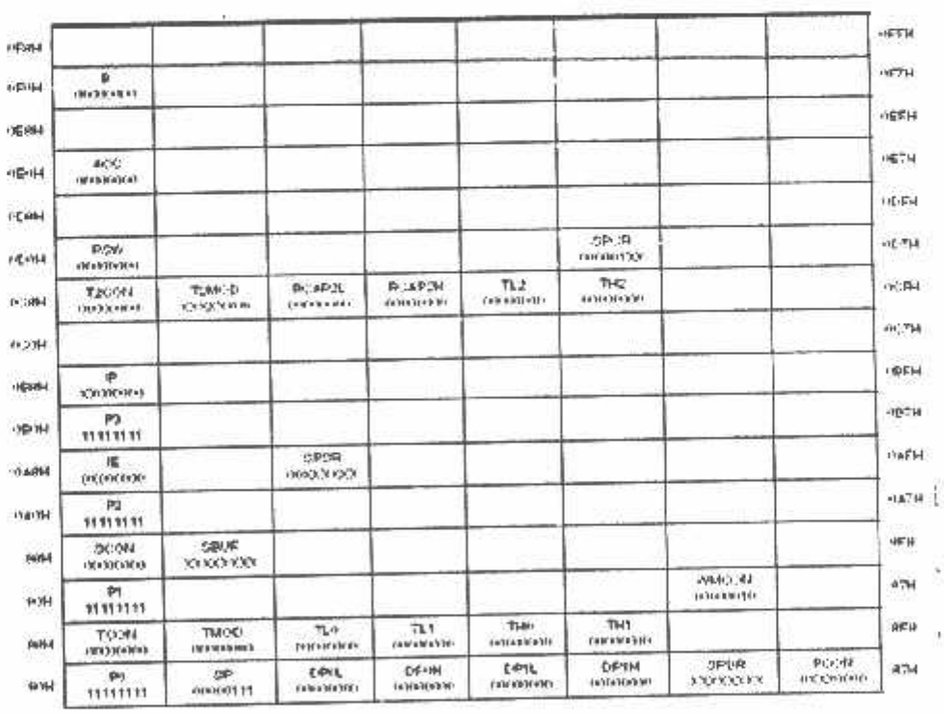
Terdiri dari 16 *bytes* yang dimulai dari 20H – 2FH. Masing-masing dari 128 bit lokasi ini dapat dialamati secara langsung yaitu dari 00H sampai 7FH.

3. *Scratch Pad Area*

Lokasi dari alamat 30H – 7FH atau sebanyak 80 *bytes* yang dapat digunakan sebagai alamat bagi RAM.

2.1.6. Special Function Register (SFR)

Special Function Register merupakan register dengan tugas khusus. SFR pada mikrokontroler AT89S8252 kompatibel dengan mikrokontroler keluarga MCS-51 dan memiliki alamat 80H - FFH sehingga terdapat 128 lokasi alamat untuk SFR. Namun demikian pada mikrokontroler ini tidak berarti memiliki SFR sebanyak 128 buah. Berikut ini adalah gambar letak dari lokasi alamat SFR.



T2MOD (Timer 2 Mode dengan alamat 0C9H), WMCON (*Watchdog and Memory Control* Register dengan alamat 96H), SPCR (SPI *Control* Register dengan alamat D5H), SPSR (SPI Status Register dengan alamat AAH), SPDR (SPI Data Register dengan alamat 86H).

- SFR untuk Timer 2

  Mikrokontroler AT89S8252 terdapat tambahan sebuah Timer/Counter yang diberi nama timer 2 (sehingga AT89S8252 memiliki 3 Timer /Counter yaitu Timer/Counter 0, Timer/Counter 1, Timer/Counter 2). Pada Timer/Counter 2 ini dikendalikan oleh *Special Function* Register yang bernama T2CON (Timer 2 Control), T2MOD (Timer @ MODE) dan sepasang register RCAP2H, RCAP2L merupakan register *capture/reload* untuk Timer 2 dalam 16 bit *capture mode/auto reload mode*.

- SFR untuk *Watchdog* Memori.

  Untuk menggunakan *Watchdog* timer atau memori, maka dapat dilakukan dengan mengatur SFR yang bernama WMCON dengan alamat 96H.

- SFR pengontrol SPI

  Berbeda dengan mikrokontroler MCS-51, AT89S8252 memiliki fasilitas SPI (*Serial Perpheral Interface*). Fasilitas ini memungkinkan transfer data kecepatan tinggi secara sinkron antara mikrokontroler dengan peripheral atau antar mikrokontroler AT89S8252. Fitur ini meliputi :

a. Full Duplek, 3 kawat dengan transfer data secara sinkron ,
b. Operasi Master atau Slave.
c. Frekuensi maksimum 6 MHz.

d. 4 bit rate terprogram.

2.1.7. Timer dan Counter

Dalam mikrokontroler AT89S8252 terdapat tiga buah pewaktu/pencacah (timer/counter 16) 16 bit yang dapat diatur melalui perangkat lunak, yaitu pewaktu / pencacah 0 dan pewaktu / pencacah 1. Timer/counter ini diatur oleh *special function* register yaitu Timer/Counter *Control* (TCON alamat 88H), dan Timer/Counter Mode *Control* (TMOD alamat 89H). Selain itu nilai byte bawah dan byte atas dari Timer/Counter disimpan dalam register TL dan TH.

Jika difungsikan sebagai Timer, maka akan menggunakan system clock sebagai sumber masukan pulsanya. Jika sebagai Counter (pencacah), maka akan menggunakan pulsa dari luar (eksternal) sebagai masukan pulsanya. Pada Port 3 terdapat fungsi khusus yaitu TO (masukan luar untuk Timer/Counter 0) dan T1 (masukan luar untuk Timer/Counter 1). Pemilihan mode Timer/Counter dikontrol oleh register TMOD. Dengan memberikan nilai tertentu pada register TMOD dapat dipilih mode operasi untuk Timer/Counter 0 dan Timer/Counter 1 seperti terlihat dalam Tabel 2-3.

Tabel 2-3 Mode Operasi Timer/Counter 0 dan 1

M2	M1	Mode	Keterangan
0	0	0	13 bit Timer
0	1	1	16 bit Timer
1	0	2	8 bit auto-reload
1	1	3	Split Mode

Pada mikrokontroler AT89S8252 terdapat tambahan Timer 2. Timer yang lain adalah Timer 0 dan Timer 1. Timer 2 ini merupakan Timer/Counter 16 bit dan memiliki 3 mode operasi yaitu *capture, auto reload* (*up down counting*) dan baud rate generator. Untuk memilih mode ini dilakukan dengan mengatur bit pada SFR T2CON (Timer 2 Control Register). Timer 2 ini terdiri dari 2 buah timer 8 bit register yaitu TH2 dan TL2. pada fungsi Timer, register TL2 dinaikkan (increment) tiap siklus mesin. Karena siklus mesin terdiri dari 12 periode osilasi, maka count rate menjadi 1/12 dari frekuensi osilator. Sedangkan pada fungsi Counter, register dinaikkan berdasarkan tanggapan adanya transisi tinggi ke rendah pada pena yang bersesuaian (dalam hal ini pin T2 atau P1.0). Tabel berikut menunjukkan mode operasi yang dapat dijalankan pada timer 2.

Tabel 2-4 Mode Operasi Timer 2

RCLK + TCLK	CP/$\overline{RL2}$	TR2	MODE
0	0	1	16-bit Auto-reload
0	1	1	16-bit Capture
1	X	1	Baud Rate Generator
X	X	0	(Off)

Sumber : Data Sheet Mikrokontroller ATMEL AT89S8252

RCLK = Receive clock enable. Jika diset menyebabkan serial port menggunakan pulsa overflow Timer 2 sebagai detak penerimaan pada serial port. Jika RCLK = 0 Timer 1 yang digunakan.

TCLK = Transmit clok enable. Jika diset menyebabkan serial port menggunakan pulsa overflow Timer 2 sebagai detak pengiriman. Jika TCLK = 0 pulsa overflow timer 1 yang digunakan.

CP/RL2 = Pemilihan capture/Reload. Jika diset maka proses capture yang terjadi sedangkan jika bit ini diclear maka proses reload.

TR2 = Bit untuk mengatur start/stop untuk timer 2 jika TR2 = 1 Timer akan aktif.

2.1.8. Idle Mode

Saat *Idle Mode* mikrokontroler tidak melakukan apa-apa. Tetapi peralatan lain yang terhubung tetap aktif. Kondisi ini dapat dihentikan dengan sebuah *interrupt* atau dengan me-*reset* sistem.

2.1.9. Sistem Interupt

Mikrokontroler AT89S8252 mempunyai 6 buah sumber interrupt yang dapat membangkitkan permintaan interrupt, yaitu INTO, INT1, T0, T1, T2 dan port serial.

Saat terjadinya interupt, mikrokontroler secara otomatis akan menuju ke *sub rutin* pada alamat tersebut. Setelah interrupt service selesai dikerjakan, mikrokontroler akan mengerjakan program semula. Dua sumber interrupt *external* adalah INTO dan INT1, dimana kedua interupsi eksternal akan aktif atau aktif transisi tergantung isi dari IT0 dan IT1 pada register TCON. Interupsi T0, T1, T2 aktif pada saat timer yang sesuai mengalami *roll over*, interupsi serial dibangkitkan dengan melakukan operasi OR pada R1 dan T1. Tiap-tiap sumber interupsi dapat *enable* atau *disable* secara otomatis.

Tingkat prioritas semua sumber interupsi dapat diprogram sendiri-sendiri dengan set atau *clear bit* pada SFRS IP (*interrupt Priority*).

Tabel 2-5 Alamat Sumber Interupsi

(MSB)(LSB)

EA	–	ET2	ES	ET1	EX1	ET0	EX0

Enable Bit = 1 enables the interrupt.

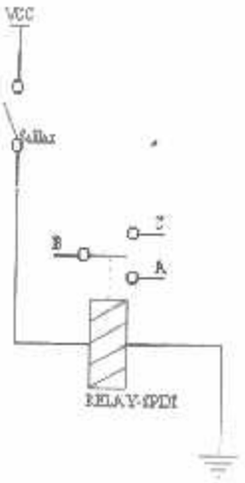
Enable Bit = 0 disables the interrupt.

Symbol	Position	Function
EA	IE.7	Disables all interrupts. If EA = 0, no interrupt is acknowledged. If EA = 1, each interrupt source is individually enabled or disabled by setting or clearing its enable bit.
–	IE.6	Reserved.
ET2	IE.5	Timer 2 interrupt enable bit.
ES	IE.4	SPI and UART interrupt enable bit.
ET1	IE.3	Timer 1 interrupt enable bit.
EX1	IE.2	External interrupt 1 enable bit.
ET0	IE.1	Timer 0 interrupt enable bit.
EX0	IE.0	External interrupt 0 enable bit.

Sumber : WWW.datasheet.atmel.com

2.2. Relay

Relay adalah salah satu dari komponen elektronika yang terdiri dari sebuah lilitan kawat(kumparan/koil) yang terlilit pada sebuah besi lunak. Jika kumparan dialiri arus listrik maka inti besi akan menjadi magnet dan dapat menarik pegas sehingga kontak BA terhubunh dan kontak BC terputus.



Gambar 2-7 Rangkaian Relay

Sumber : WWW.relay.com

Relay berfungsi untuk menghubungkan atau memutuskan aliran listrik yang dikontrol dengan memberikan tegangan dan arus tertentu pada koilnya. Dalam memutus atau menghubungkan kontak digerakkan oleh *fluksi* yang ditimbulkan dari adanya medan magnet listrik yang dihasilkan oleh kumparan yang melilit pada besi lunak.

2.3. Op-Amp.

2.3.1. Penguat Inverting

Rangkaian penguat inverting merupakan rangkaian Op-Amp yang paling luas digunakan, rangkaian ini merupakan penguat yang gainnya dari vi ke vo ditentukan oleh Rf dan Ri yang dapat memperkecil isyarat ac atau dc.

Tabel 2-6 Fungsi-fungsi pin-pin LM741

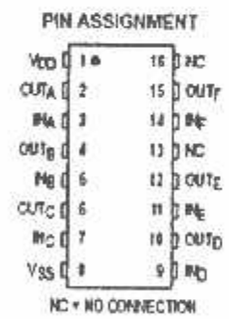
PIN	NAMA	KET
1.	BAL	OFFSET BALANCE
2.	- IN	INVERTING INPUT
3.	+ IN	NON INVERTING INPUT
4.	- V	GROUND
5.	BAL	OFFSET BALANCE
6.	OUT	OUTPUT SIGNAL
7.	+ V	POSITIF POWER SUPPLY
8.	NC	NO CONNECTION

Sumber : WWW.Datasheet.LM741.com

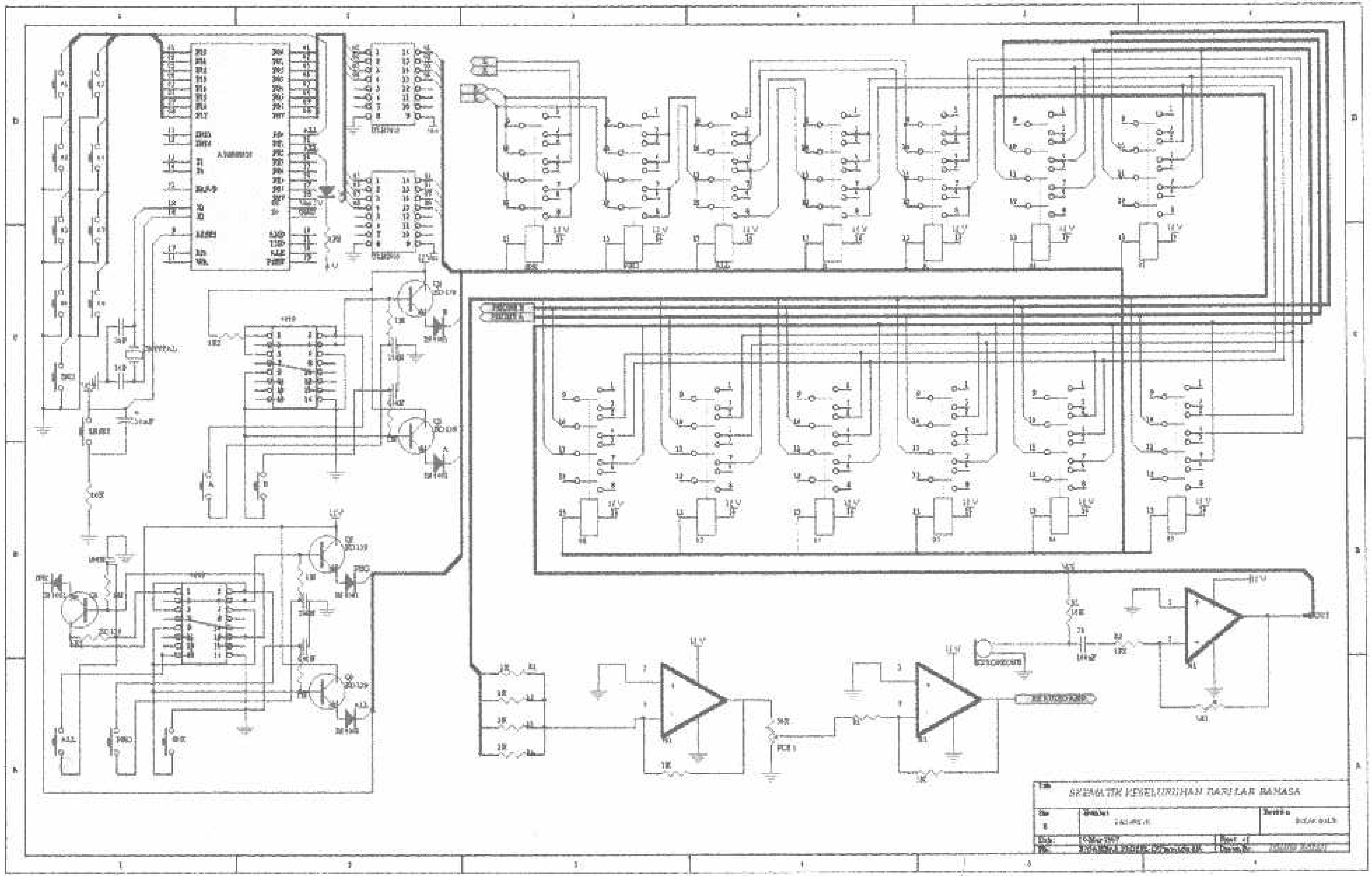
2.5. Switch Elektronik

Rangkaian switch elektronik yang digunakan adalah jenis ic cmos dengan tipe 4049, dimana ic ini akan aktif jika mendapat logic high dan jika logic low maka tidak aktif

Gambar 2-10 Konfigurasi Pin-pin 4049



Sumber : WWW.datasheet.4049.com


SKEMATIK KESELURUHAN DARI LAB BAHASA
AT89C51
ULN2803
4016
BD139
MICROPHONE
HEADPHONE
CRYSTAL
RESET
OUT

```
joto awal;


( == 1)

(P1 == 251)

( = 0;
MURID3 = 1;
goto awal;


X == 0)

(P1 == 251)

X = 1;
MURID3 = 0;
goto awal;


X == 1)

(P1 == 247)

X = 0;
MURID4 = 1;
goto awal;


X == 0)

(P1 == 247)
{
X = 1;
MURID4 = 0;
goto awal;


X == 1)

(P1 == 239)
{
X = 0;
MURID5 = 1;
goto awal;
}

(X == 0)

f (P1 == 239)
```

```
{
 X = 1;
 MURID5 = 0;
 goto awal;
 }
}

(X == 1)
{
if (P1 == 223)
 {
 X = 0;
 MURID6 = 1;
 goto awal;
 }

(X == 0)

if (P1 == 223)
 {
 X = 1;
 MURID6 = 0;
 goto awal;
 }


(X == 1)

f (P1 == 191)
{
 X = 0;
 MURID7 = 1;
 goto awal;
}


(X == 0)

(P1 == 191)
{
 X = 1;
 MURID7 = 0;
 goto awal;
}


 X == 1)

 (P1 == 127)

 X = 0;
 MURID8 = 1;
 goto awal;


 X == 0)
```

```
if (P1 == 127)
 {
  X = 1;
  MURID8 = 0;
  goto awal;
 }
}
 (P2 == 254)
{
 goto awal1;
}
oto awal;


al1:
 {
   X = 2;
          P2 = 251;
          if (Y == 1)
          {
           if (P1 == 254)
            {
             Y = 0;
             P2 = 254;
             goto awal1;
            }
          }

          if (Y == 0)
          {
           if (P1 == 254)
            {
             Y = 1;
             P2 = 255;
             goto awal1;
            }
          }

          if (Y == 1)
          {
           if (P1 == 253)
            {
             Y = 0;
             P2 = 255;
             P2 = 253;
             goto awal1;
            }
          }


          if (Y == 0)
          {
           if (P1 == 253)
            {
             Y = 1;
             P2 = 255;
             goto awal1;
            }
          }
```

```
if (Y == 1)
 {
  if (P1 == 251)
   {
    Y = 0;
    P2 = 255;
    P2 = 251;
    goto awal1;
   }
 }

if (Y == 0)
 {
  if (P1 == 251)
   {
    Y = 1;
    P2 = 255;
    goto awal1;
   }
 }
if (Y == 1)
 {
  if (P1 == 247)
   {
    Y = 0;
    P2 = 255;
    P2 = 247;
    goto awal1;
   }
 }

if (Y == 0)
 {
  if (P1 == 247)
   {
    Y = 1;
    P2 = 255;
    goto awal1;
   }
 }


if (Y == 1)
 {
  if (P1 == 239)
   {
    Y = 0;
    P2 = 255;
    P2 = 239;
    goto awal1;
   }
 }
```

```
    if (Y == 0)
     {
      if (P1 == 239)
       {
        Y = 1;
P2 = 255;
        goto awal1;
       }
     }

    if (Y == 1)
     {
      if (P1 == 223)
       {
        Y = 0;
P2 = 255;
        P2 = 223;
        goto awal1;
       }
     }


    if (Y == 0)
     {
      if (P1 == 223)
       {
        Y = 1;
        P2 = 255;
        goto awal1;
       }
     }

    if (Y == 1)
     {
      if (P1 == 191)
       {
        Y = 0;
P2 = 255;
        P2 = 191;
        goto awal1;
       }
     }


   if (Y == 0)
    {
     if (P1 == 191)
      {
       Y = 1;
       P2 = 255;
       goto awal1;
      }
    }

   if (Y == 1)
    {
     if (P1 == 127)
      {
       Y = 0;
```

INSTITUT TEKNOLOGI NASIONAL MALANG
FAKULTAS TEKNOLOGI INDUSTRI
JURUSAN TEKNIK ELEKTRO S-1
KONSENTRASI ELEKTRONIKA

LEMBAR PERSETUJUAN PERBAIKAN SKRIPSI

Dari hasil ujian skripsi Jurusan Teknik Elektro jenjang Strata Satu (S-1), yang diselenggarakan pada :

Hari : Jum'at

Tanggal : 23 maret 2007

Telah dilakukan perbaikan oleh :

Nama : Isnaini Rozafi

NIM : 01.17.044

Jurusan : Teknik Elektro S-1

Konsentrasi : Elektronika

Judul Skripsi : **Perencanaan dan Pembuatan Master Kontrol Lab.Bahasa Delapan Channel Berbasis Mikrokontroller AT89S8252**

Perbaikan meliputi :

No.	Materi Perbaikan	Keterangan	Paraf Penguji I
01.	Gambar Skema Lengkap	Harap disempurnakan	
02.	Gambar hal.36 dan 39	Diperbaiki	
03.	Hasil Pengujian hal.37	Diperbaiki	

Penguji I

Ir. Widodo Pudji M, MT.
NIP.Y. 1028700171

INSTITUT TEKNOLOGI NASIONAL MALANG
FAKULTAS TEKNOLOGI INDUSTRI
JURUSAN TEKNIK ELEKTRO S-1
KONSENTRASI ELEKTRONIKA

LEMBAR PERSETUJUAN PERBAIKAN SKRIPSI

Dari hasil ujian skripsi Jurusan Teknik Elektro jenjang Strata Satu (S-1), yang diselenggarakan pada :

Hari : Jum'at

Tanggal : 23 maret 2007

Telah dilakukan perbaikan oleh :

Nama : Isnaini Rozafi

NIM : 01.17.044

Jurusan : Teknik Elektro S-1

Konsentrasi : Elektronika

Judul Skripsi : **Perencanaan dan Pembuatan Master Kontrol Lab.Bahasa Delapan Channel Berbasis Mikrokontroller AT89S8252**

Perbaikan meliputi :

No.	Materi Perbaikan	Keterangan	Paraf Penguji II
01.	Gambar Skema Lengkap	Harap disempurnakan	

Penguji II

Dr. Cahyo Crysdian, MSC.
NIP. 1030400412

INSTITUT TEKNOLOGI NASIONAL
FAKULTAS TEKNOLOGI INDUSTRI
JURUSAN TEKNIK ELEKTRO

Formulir Perbaikan Ujian Skripsi

.m pelaksanaan Ujian Skripsi Janjang Strata 1 Jurusan Teknik Elektro Konsentasi T. Energi
k / T. Elektronika, maka perlu adanya perbaikan skripsi untuk mahasiswa :

IA : Isnaini R
I :
aikan meliputi :

Gambar skema lengkap supaya dicantumkan.

Gambar hal 36 & 39 harap dicantumkan.

) Hasil pengujian hal 37 harap dicantumkan.

Malang,

([signature])

INSTITUT TEKNOLOGI NASIONAL
FAKULTAS TEKNOLOGI INDUSTRI
JURUSAN TEKNIK ELEKTRO

Formulir Perbaikan Ujian Skripsi

Dalam pelaksanaan Ujian Skripsi Janjang Strata 1 Jurusan Teknik Elektro Konsentasi T. Energi Listrik / T. Elektronika, maka perlu adanya perbaikan skripsi untuk mahasiswa :

NAMA :
NIM :
Perbaikan meliputi :

1) Perbaiki ejaan tata tulis
(Buat detailnya)

Malang,

(_____)

TITUT TEKNOLOGI NASIONAL
l. Bendungan Sigura-gura No. 2
MALANG

FORMULIR BIMBINGAN SKRIPSI

l	: ISNAINI ROZAFI
	: 01.17.044
Bimbingan	: 10 Februari 2007 s/d 10 Agustus 2007
Skripsi	: Perencanaan dan Pembuatan Master Kontrol Lab. Bahasa 8 Channel Berbasis Mikrokontroller AT89S8252

Tanggal	Uraian	Paraf Pembimbing
10-2-07	Bab I & II	
10-2-07	Revisi Bab II	
18-02-07	Revisi Bab II	
21-02-07	Bab III & IV	
25-02-07	Revisi Bab IV	
28-02-07	Revisi Bab V	
8-3-07	Acc Seminar Hasil	
12-3-2007	Acc Lengkap	

Malang, 12-3-2007
Dosen Pembimbing

Joseph Dedy Irawan, ST., MT.
NIP. 132315178

Form S-4

eatures

- Compatible with MCS®51 Products
- 8K Bytes of In-System Reprogrammable Downloadable Flash Memory
  - SPI Serial Interface for Program Downloading
  - Endurance: 1,000 Write/Erase Cycles
- 2K Bytes EEPROM
  - Endurance: 100,000 Write/Erase Cycles
- V to 6V Operating Range
- Fully Static Operation: 0 Hz to 24 MHz
- Three-level Program Memory Lock
- 256 x 8-bit Internal RAM
- 32 Programmable I/O Lines
- Three 16-bit Timer/Counters
- Nine Interrupt Sources
- Programmable UART Serial Channel
- SPI Serial Interface
- Low-power Idle and Power-down Modes
- Interrupt Recovery from Power-down
- Programmable Watchdog Timer
- Dual Data Pointer
- Power-off Flag

escription

ie AT89S8252 is a low-power, high-performance CMOS 8-bit microcontroller with 8K tes of downloadable Flash programmable and erasable read-only memory and 2K tes of EEPROM. The device is manufactured using Atmel's high-density nonvolatile emory technology and is compatible with the industry-standard 80C51 instruction t and pinout. The on-chip downloadable Flash allows the program memory to be programmed In-System through an SPI serial interface or by a conventional nonvol-le memory programmer. By combining a versatile 8-bit CPU with downloadable ash on a monolithic chip, the Atmel AT89S8252 is a powerful microcontroller, which ovides a highly-flexible and cost-effective solution to many embedded control plications.

e AT89S8252 provides the following standard features: 8K bytes of downloadable ash, 2K bytes of EEPROM, 256 bytes of RAM, 32 I/O lines, programmable watchdog ner, two data pointers, three 16-bit timer/counters, a six-vector two-level interrupt chitecture, a full duplex serial port, on-chip oscillator, and clock circuitry. In addition, e AT89S8252 is designed with static logic for operation down to zero frequency and pports two software selectable power saving modes. The Idle Mode stops the CPU ile allowing the RAM, timer/counters, serial port, and interrupt system to continue nctioning. The Power-down mode saves the RAM contents but freezes the oscillator, abling all other chip functions until the next external interrupt or hardware reset.

e downloadable Flash can be changed a single byte at a time and is accessible ough the SPI serial interface. Holding RESET active forces the SPI bus into a serial gramming interface and allows the program memory to be written to or read from ess lock bits have been activated.

8-bit Microcontroller with 8K Bytes Flash

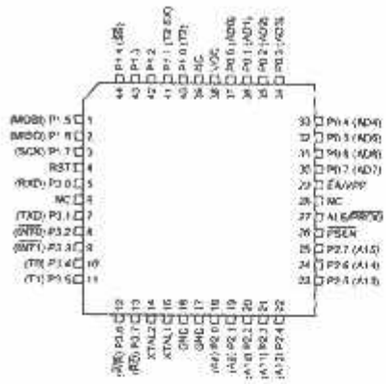
AT89S8252

0401F–MICRO–11/03

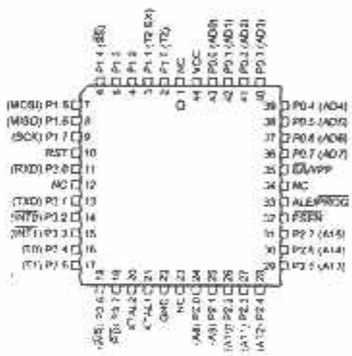
in Configurations

PDIP

TQFP



PLCC



in Description

:C Supply voltage.

ID Ground.

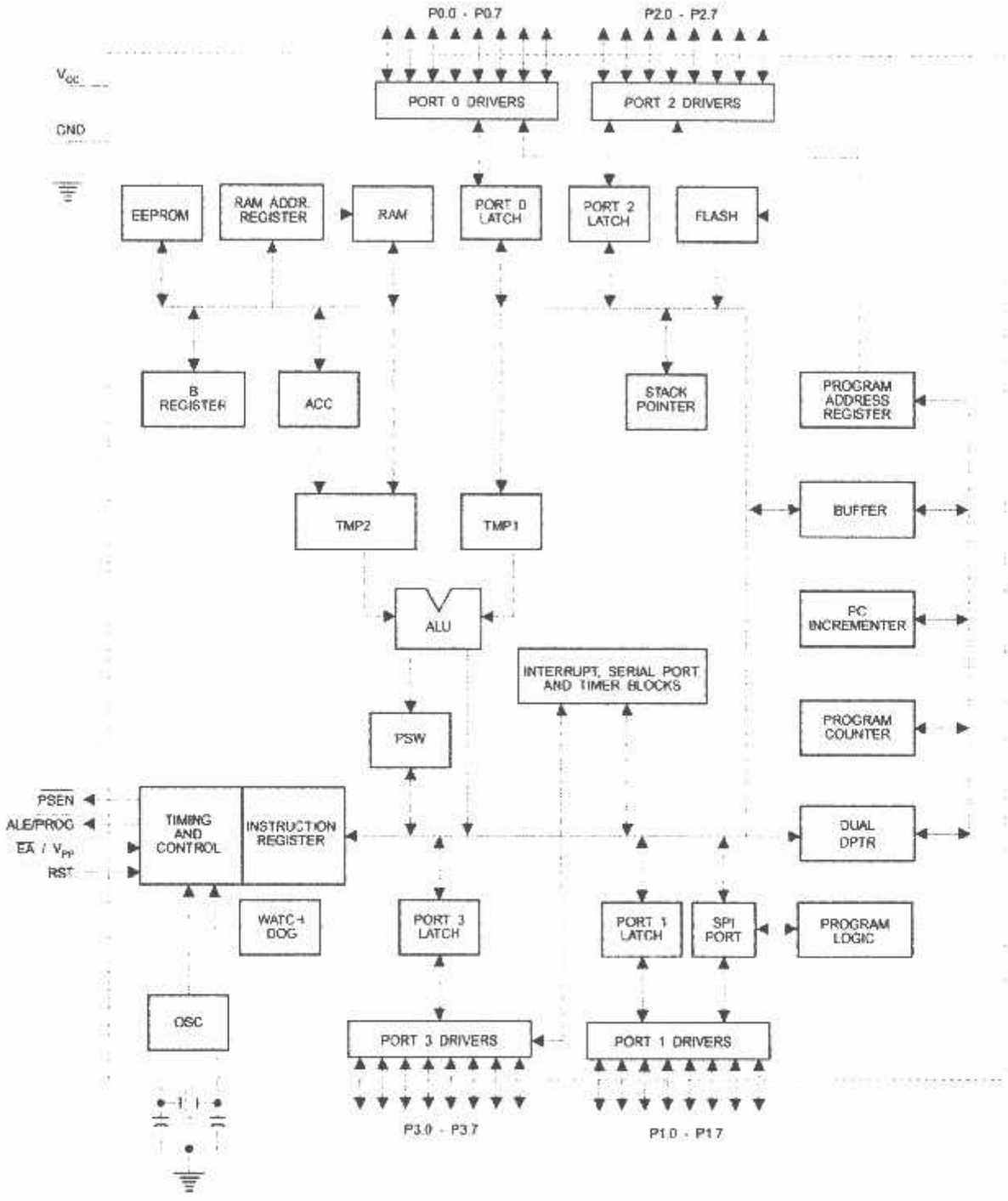
rt 0 Port 0 is an 8-bit open drain bi-didirectional I/O port. As an output port, each pin can sink eight TTL inputs. When 1s are written to port 0 pins, the pins can be used as high-impedance inputs.

Port 0 can also be configured to be the multiplexed low-order address/data bus during accesses to external program and data memory. In this mode, P0 has internal pull-ups.

Port 0 also receives the code bytes during Flash programming and outputs the code bytes during program verification. External pull-ups are required during program verification.

rt 1 Port 1 is an 8-bit bi-directional I/O port with internal pull-ups. The Port 1 output buffers can sink/source four TTL inputs. When 1s are written to Port 1 pins, they are pulled high by the internal pull-ups and can be used as inputs. As inputs, Port 1 pins that are externally being pulled low will source current (I_{IL}) because of the internal pull-ups.

ock Diagram


P0.0 - P0.7
P2.0 - P2.7
V_{CC}
GND
PORT 0 DRIVERS
PORT 2 DRIVERS
EEPROM
RAM ADDR. REGISTER
RAM
PORT 0 LATCH
PORT 2 LATCH
FLASH
B REGISTER
ACC
STACK POINTER
PROGRAM ADDRESS REGISTER
TMP2
TMP1
BUFFER
ALU
PC INCREMENTER
INTERRUPT, SERIAL PORT AND TIMER BLOCKS
PSW
PROGRAM COUNTER
PSEN
ALE/PROG
EA / V_{PP}
RST
TIMING AND CONTROL
INSTRUCTION REGISTER
DUAL DPTR
WATCH DOG
PORT 3 LATCH
PORT 1 LATCH
SPI PORT
PROGRAM LOGIC
OSC
PORT 3 DRIVERS
PORT 1 DRIVERS
P3.0 - P3.7
P1.0 - P1.7

Some Port 1 pins provide additional functions. P1.0 and P1.1 can be configured to be the timer/counter 2 external count input (P1.0/T2) and the timer/counter 2 trigger input (P1.1/T2EX), respectively.

Furthermore, P1.4, P1.5, P1.6, and P1.7 can be configured as the SPI slave port select, data input/output and shift clock input/output pins as shown in the following table.

Port Pin	Alternate Functions
P1.0	T2 (external count input to Timer/Counter 2), clock-out
P1.1	T2EX (Timer/Counter 2 capture/reload trigger and direction control)
P1.4	$\overline{SS}$ (Slave port select input)
P1.5	MOSI (Master data output, slave data input pin for SPI channel)
P1.6	MISO (Master data input, slave data output pin for SPI channel)
P1.7	SCK (Master clock output, slave clock input pin for SPI channel)

Port 1 also receives the low-order address bytes during Flash programming and verification.

ort 2

Port 2 is an 8-bit bi-directional I/O port with internal pull-ups. The Port 2 output buffers can sink/source four TTL inputs. When 1s are written to Port 2 pins, they are pulled high by the internal pull-ups and can be used as inputs. As inputs, Port 2 pins that are externally being pulled low will source current (I_{IL}) because of the internal pull-ups.

Port 2 emits the high-order address byte during fetches from external program memory and during accesses to external data memory that use 16-bit addresses (MOVX @ DPTR). In this application, Port 2 uses strong internal pull-ups when emitting 1s. During accesses to external data memory that use 8-bit addresses (MOVX @ RI), Port 2 emits the contents of the P2 Special Function Register.

Port 2 also receives the high-order address bits and some control signals during Flash programming and verification.

ort 3

Port 3 is an 8-bit bi-directional I/O port with internal pull-ups. The Port 3 output buffers can sink/source four TTL inputs. When 1s are written to Port 3 pins, they are pulled high by the internal pull-ups and can be used as inputs. As inputs, Port 3 pins that are externally being pulled low will source current (I_{IL}) because of the pull-ups.

Port 3 receives some control signals for Flash programming and verification.

Port 3 also serves the functions of various special features of the AT89S8252, as shown in the following table.

Port Pin	Alternate Functions
P3.0	RXD (serial input port)
P3.1	TXD (serial output port)
P3.2	$\overline{INT0}$ (external interrupt 0)
P3.3	$\overline{INT1}$ (external interrupt 1)
P3.4	T0 (timer 0 external input)
P3.5	T1 (timer 1 external input)
P3.6	$\overline{WR}$ (external data memory write strobe)
P3.7	$\overline{RD}$ (external data memory read strobe)

ST

Reset input. A high on this pin for two machine cycles while the oscillator is running resets the device.

LE/$\overline{PROG}$

Address Latch Enable is an output pulse for latching the low byte of the address during accesses to external memory. This pin is also the program pulse input ($\overline{PROG}$) during Flash programming.

In normal operation, ALE is emitted at a constant rate of 1/6 the oscillator frequency and may be used for external timing or clocking purposes. Note, however, that one ALE pulse is skipped during each access to external data memory.

If desired, ALE operation can be disabled by setting bit 0 of SFR location 8EH. With the bit set, ALE is active only during a MOVX or MOVC instruction. Otherwise, the pin is weakly pulled high. Setting the ALE-disable bit has no effect if the microcontroller is in external execution mode.

$\overline{SEN}$

Program Store Enable is the read strobe to external program memory.

When the AT89S8252 is executing code from external program memory, $\overline{PSEN}$ is activated twice each machine cycle, except that two $\overline{PSEN}$ activations are skipped during each access to external data memory.

$\overline{A}$/VPP

External Access Enable. $\overline{EA}$ must be strapped to GND in order to enable the device to fetch code from external program memory locations starting at 0000H up to FFFFH. Note, however, that if lock bit 1 is programmed, $\overline{EA}$ will be internally latched on reset.

$\overline{EA}$ should be strapped to V_{CC} for internal program executions. This pin also receives the 12-volt programming enable voltage (V_{PP}) during Flash programming when 12-volt programming is selected.

TAL1

Input to the inverting oscillator amplifier and input to the internal clock operating circuit.

TAL2

Output from the inverting oscillator amplifier.

:cial Function
jisters

A map of the on-chip memory area called the Special Function Register (SFR) space is shown in Table 1.

Note that not all of the addresses are occupied, and unoccupied addresses may not be implemented on the chip. Read accesses to these addresses will in general return random data, and write accesses will have an indeterminate effect.

User software should not write 1s to these unlisted locations, since they may be used in future products to invoke new features. In that case, the reset or inactive values of the new bits will always be 0.

Timer 2 Registers Control and status bits are contained in registers T2CON (shown in Table 2) and T2MOD (shown in Table 9) for Timer 2. The register pair (RCAP2H, RCAP2L) are the Capture/Reload registers for Timer 2 in 16-bit capture mode or 16-bit auto-reload mode.

ıle 1. AT89S8252 SFR Map and Reset Values

iF8H									0FFH
)F0H	B 00000000								0F7H
0E8H									0EFH
0E0H	ACC 00000000								0E7H
0D8H									0DF H
0D0H	PSW 00000000					SPCR 000001XX			0D7H
0C8H	T2CON 00000000	T2MOD XXXXXX00	RCAP2L 00000000	RCAP2H 00000000	TL2 00000000	TH2 00000000			0CF H
0C0H									0C7H
0B8H	IP XX000000								0BFH
0B0H	P3 11111111								0B7H
0A8H	IE 0X000000		SPSR 00XXXXXX						0AFH
0A0H	P2 11111111								0A7H
98H	SCON 00000000	SBUF XXXXXXXX							9FH
90H	P1 11111111						WMCON 00000010		97H
88H	TCON 00000000	TMOD 00000000	TL0 00000000	TL1 00000000	TH0 00000000	TH1 00000000			8FH
80H	P0 11111111	SP 00000111	DP0L 00000000	DP0H 00000000	DP1L 00000000	DP1H 00000000	SPDR XXXXXXXX	PCON 0XXX0000	87H

2. T2CON – Timer/Counter 2 Control Register

ON Address = 0C8H Reset Value = 0000 0000B

Addressable

TF2	EXF2	RCLK	TCLK	EXEN2	TR2	C/$\overline{T2}$	CP/$\overline{RL2}$
7	6	5	4	3	2	1	0

mbol	Function
2	Timer 2 overflow flag set by a Timer 2 overflow and must be cleared by software. TF2 will not be set when either RCLK = 1 or TCLK = 1.
F2	Timer 2 external flag set when either a capture or reload is caused by a negative transition on T2EX and EXEN2 = 1. When Timer 2 interrupt is enabled, EXF2 = 1 will cause the CPU to vector to the Timer 2 interrupt routine. EXF2 must be cleared by software. EXF2 does not cause an interrupt in up/down counter mode (DCEN = 1).
CLK	Receive clock enable. When set, causes the serial port to use Timer 2 overflow pulses for its receive clock in serial port Modes 1 and 3. RCLK = 0 causes Timer 1 overflows to be used for the receive clock.
CLK	Transmit clock enable. When set, causes the serial port to use Timer 2 overflow pulses for its transmit clock in serial port Modes 1 and 3. TCLK = 0 causes Timer 1 overflows to be used for the transmit clock.
XEN2	Timer 2 external enable. When set, allows a capture or reload to occur as a result of a negative transition on T2EX if Timer 2 is not being used to clock the serial port. EXEN2 = 0 causes Timer 2 to ignore events at T2EX.
R2	Start/Stop control for Timer 2. TR2 = 1 starts the timer.
/T2	Timer or counter select for Timer 2. C/$\overline{T2}$ = 0 for timer function. C/$\overline{T2}$ = 1 for external event counter (falling edge triggered).
P/RL2	Capture/Reload select. CP/$\overline{RL2}$ = 1 causes captures to occur on negative transitions at T2EX if EXEN2 = 1. CP/$\overline{RL2}$ = 0 causes automatic reloads to occur when Timer 2 overflows or negative transitions occur at T2EX when EXEN2 = 1. When either RCLK or TCLK = 1, this bit is ignored and the timer is forced to auto-reload on Timer 2 overflow.

:hdog and Memory Control Register The WMCON register contains control bits for the Watchdog Timer (shown in e 3). The EEMEN and EEMWE bits are used to select the 2K bytes on-chip EEPROM, and to enable byte-write. The bit selects one of two DPTR registers available.

e 3. WMCON—Watchdog and Memory Control Register

:CON Address = 96H — Reset Value = 0000 0010B

PS2	PS1	PS0	EEMWE	EEMEN	DPS	WDTRST	WDTEN
7	6	5	4	3	2	1	0

mbol	Function
32 31 S0	Prescaler Bits for the Watchdog Timer. When all three bits are set to "0", the watchdog timer has a nominal period of 16 ms. When all three bits are set to "1", the nominal period is 2048 ms.
EMWE	EEPROM Data Memory Write Enable Bit. Set this bit to "1" before initiating byte write to on-chip EEPROM with the MOVX instruction. User software should set this bit to "0" after EEPROM write is completed.
EEMEN	Internal EEPROM Access Enable. When EEMEN = 1, the MOVX instruction with DPTR will access on-chip EEPROM instead of external data memory. When EEMEN = 0, MOVX with DPTR accesses external data memory.
DPS	Data Pointer Register Select. DPS = 0 selects the first bank of Data Pointer Register, DP0, and DPS = 1 selects the second bank, DP1
WDTRST RDY/$\overline{BSY}$	Watchdog Timer Reset and EEPROM Ready/$\overline{Busy}$ Flag. Each time this bit is set to "1" by user software, a pulse is generated to reset the watchdog timer. The WDTRST bit is then automatically reset to "0" in the next instruction cycle. The WDTRST bit is Write-Only. This bit also serves as the RDY/$\overline{BSY}$ flag in a Read-Only mode during EEPROM write. RDY/$\overline{BSY}$ = 1 means that the EEPROM is ready to be programmed. While programming operations are being executed, the RDY/$\overline{BSY}$ bit equals "0" and is automatically reset to "1" when programming is completed.
WDTEN	Watchdog Timer Enable Bit. WDTEN = 1 enables the watchdog timer and WDTEN = 0 disables the watchdog timer.

SPI Registers Control and status bits for the Serial Peripheral Interface are contained in registers SPCR (shown in Table 4) and SPSR (shown in Table 5). The SPI data bits are contained in the SPDR register. Writing the SPI data register during serial data transfer sets the Write Collision bit, WCOL, in the SPSR register. The SPDR is double buffered for writing and the values in SPDR are not changed by Reset.

Interrupt Registers The global interrupt enable bit and the individual interrupt enable bits are in the IE register. In addition, the individual interrupt enable bit for the SPI is in the SPCR register. Two priorities can be set for each of the six interrupt sources in the IP register.

Dual Data Pointer Registers To facilitate accessing both internal EEPROM and external data memory, two banks of 16-bit Data Pointer Registers are provided: DP0 at SFR address locations 82H-83H and DP1 at 84H-85H. Bit DPS = 0 in SFR WMCON selects DP0 and DPS = 1 selects DP1. The user should **ALWAYS** initialize the DPS bit to the apropriate value before accessing the respective Data Pointer Register.

Power Off Flag The Power Off Flag (POF) is located at bit_4 (PCON.4) in the PCON SFR. POF is set to "1" during power up. It can be set and reset under software control and is not affected by RESET.

ble 4. SPCR – SPI Control Register

SPCR Address = D5H — Reset Value = 0000 01XXB

Bit	7	6	5	4	3	2	1	0
	SPIE	SPE	DORD	MSTR	CPOL	CPHA	SPR1	SPR0

ymbol	Function
PIE	SPI Interrupt Enable. This bit, in conjunction with the ES bit in the IE register, enables SPI interrupts: SPIE = 1 and ES = 1 enable SPI interrupts. SPIE = 0 disables SPI interrupts.
PE	SPI Enable. SPI = 1 enables the SPI channel and connects $\overline{SS}$, MOSI, MISO and SCK to pins P1.4, P1.5, P1.6, and P1.7. SPI = 0 disables the SPI channel.
ORD	Data Order. DORD = 1 selects LSB first data transmission. DORD = 0 selects MSB first data transmission.
STR	Master/Slave Select. MSTR = 1 selects Master SPI mode. MSTR = 0 selects Slave SPI mode.
POL	Clock Polarity. When CPOL = 1, SCK is high when idle. When CPOL = 0, SCK of the master device is low when not transmitting. Please refer to figure on SPI Clock Phase and Polarity Control.
PHA	Clock Phase. The CPHA bit together with the CPOL bit controls the clock and data relationship between master and slave. Please refer to figure on SPI Clock Phase and Polarity Control.
PR0 PR1	SPI Clock Rate Select. These two bits control the SCK rate of the device configured as master. SPR1 and SPR0 have no effect on the slave. The relationship between SCK and the oscillator frequency, F_{osc}, is as follows: SPR1 SPR0 SCK = F_{osc} divided by 0 0 4 0 1 16 1 0 64 1 1 128

: 5. SPSR – SPI Status Register

:R Address = AAH

Reset Value = 00XX XXXXB

SPIF	WCOL	–	–	–	–	–	–
7	6	5	4	3	2	1	0

ıbol	Function
F	SPI Interrupt Flag. When a serial transfer is complete, the SPIF bit is set and an interrupt is generated if SPIE = 1 and ES = 1. The SPIF bit is cleared by reading the SPI status register with SPIF and WCOL bits set, and then reading/writing the SPI data register.
:OL	Write Collision Flag. The WCOL bit is set if the SPI data register is written during a data transfer. During data transfer, the result of reading the SPDR register may be incorrect, and writing to it has no effect. The WCOL bit (and the SPIF bit) are cleared by reading the SPI status register with SPIF and WCOL set, and then accessing the SPI data register.

ıle 6. SPDR – SPI Data Register

'DR Address = 86H

Reset Value = unchanged

	SPD7	SPD6	SPD5	SPD4	SPD3	SPD2	SPD1	SPD0
Bit	7	6	5	4	3	2	1	0

ata Memory – EPROM and RAM

The AT89S8252 implements 2K bytes of on-chip EEPROM for data storage and 256 bytes of RAM. The upper 128 bytes of RAM occupy a parallel space to the Special Function Registers. That means the upper 128 bytes have the same addresses as the SFR space but are physically separate from SFR space.

When an instruction accesses an internal location above address 7FH, the address mode used in the instruction specifies whether the CPU accesses the upper 128 bytes of RAM or the SFR space. Instructions that use direct addressing access SFR space.

For example, the following direct addressing instruction accesses the SFR at location 0A0H (which is P2).

```
MOV 0A0H, #data
```

Instructions that use indirect addressing access the upper 128 bytes of RAM. For example, the following indirect addressing instruction, where R0 contains 0A0H, accesses the data byte at address 0A0H, rather than P2 (whose address is 0A0H).

```
MOV @R0, #data
```

Note that stack operations are examples of indirect addressing, so the upper 128 bytes of data RAM are available as stack space.

The on-chip EEPROM data memory is selected by setting the EEMEN bit in the WMCON register at SFR address location 96H. The EEPROM address range is from 000H to 7FFH. The MOVX instructions are used to access the EEPROM. To access off-chip data memory with the MOVX instructions, the EEMEN bit needs to be set to "0".

The EEMWE bit in the WMCON register needs to be set to "1" before any byte location in the EEPROM can be written. User software should reset EEMWE bit to "0" if no further EEPROM write is required. EEPROM write cycles in the serial programming mode are self-timed and typically take 2.5 ms. The progress of EEPROM write can be monitored by reading the RDY/$\overline{BSY}$ bit (read-only) in SFR WMCON. RDY/$\overline{BSY}$ = 0 means

programming is still in progress and RDY/$\overline{BSY}$ = 1 means EEPROM write cycle is completed and another write cycle can be initiated.

In addition, during EEPROM programming, an attempted read from the EEPROM will fetch the byte being written with the MSB complemented. Once the write cycle is completed, true data are valid at all bit locations.

grammable tchdog Timer

The programmable Watchdog Timer (WDT) operates from an independent internal oscillator. The prescaler bits, PS0, PS1 and PS2 in SFR WMCON are used to set the period of the Watchdog Timer from 16 ms to 2048 ms. The available timer periods are shown in the following table and the actual timer periods (at V_{CC} = 5V) are within ±30% of the nominal.

The WDT is disabled by Power-on Reset and during Power-down. It is enabled by setting the WDTEN bit in SFR WMCON (address = 96H). The WDT is reset by setting the WDTRST bit in WMCON. When the WDT times out without being reset or disabled, an internal RST pulse is generated to reset the CPU.

Table 7. Watchdog Timer Period Selection

WDT Prescaler Bits			
PS2	PS1	PS0	Period (nominal)
0	0	0	16 ms
0	0	1	32 ms
0	1	0	64 ms
0	1	1	128 ms
1	0	0	256 ms
1	0	1	512 ms
1	1	0	1024 ms
1	1	1	2048 ms

mer 0 and 1

Timer 0 and Timer 1 in the AT89S8252 operate the same way as Timer 0 and Timer 1 in the AT89C51 and AT89C52. For further information on the timers' operation, refer to the Atmel web site (http://www.atmel.com). From the home page, select "Products", then "Microcontrollers, then "8051-Architecture". Click on "Documentation", then on "Other Documents". Open the document "AT89 Series Hardware Description".

ner 2

Timer 2 is a 16-bit Timer/Counter that can operate as either a timer or an event counter. The type of operation is selected by bit C/$\overline{T2}$ in the SFR T2CON (shown in Table 2). Timer 2 has three operating modes: capture, auto-reload (up or down counting), and baud rate generator. The modes are selected by bits in T2CON, as shown in Table 8.

Timer 2 consists of two 8-bit registers, TH2 and TL2. In the Timer function, the TL2 register is incremented every machine cycle. Since a machine cycle consists of 12 oscillator periods, the count rate is 1/12 of the oscillator frequency.

In the Counter function, the register is incremented in response to a 1-to-0 transition at its corresponding external input pin, T2. In this function, the external input is sampled during S5P2 of every machine cycle. When the samples show a high in one cycle and a low in the next cycle, the count is incremented. The new count value appears in the register during S3P1 of the cycle following the one in which the transition was detected.

Since two machine cycles (24 oscillator periods) are required to recognize a 1-to-0 transition, the maximum count rate is 1/24 of the oscillator frequency. To ensure that a given level is sampled at least once before it changes, the level should be held for at least one full machine cycle.

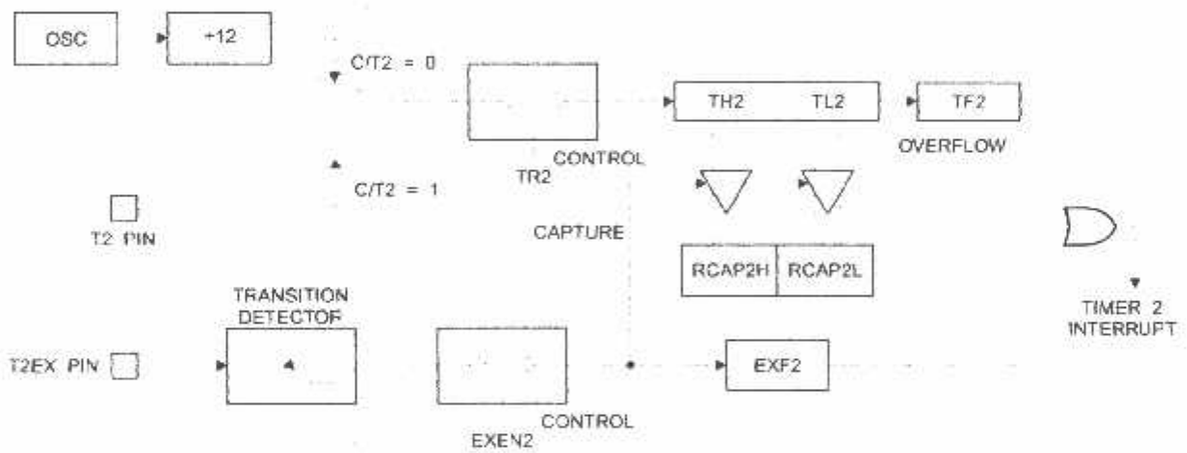
Table 8. Timer 2 Operating Modes

RCLK + TCLK	CP/$\overline{RL2}$	TR2	MODE
0	0	1	16-bit Auto-reload
0	1	1	16-bit Capture
1	X	1	Baud Rate Generator
X	X	0	(Off)

pture Mode

In the capture mode, two options are selected by bit EXEN2 in T2CON. If EXEN2 = 0, Timer 2 is a 16-bit timer or counter which upon overflow sets bit TF2 in T2CON. This bit can then be used to generate an interrupt. If EXEN2 = 1, Timer 2 performs the same operation, but a 1-to-0 transition at external input T2EX also causes the current value in TH2 and TL2 to be captured into RCAP2H and RCAP2L, respectively. In addition, the transition at T2EX causes bit EXF2 in T2CON to be set. The EXF2 bit, like TF2, can generate an interrupt. The capture mode is illustrated in Figure 1.

ure 1. Timer 2 in Capture Mode



to-reload (Up or Down unter)

Timer 2 can be programmed to count up or down when configured in its 16-bit auto-reload mode. This feature is invoked by the DCEN (Down Counter Enable) bit located in the SFR T2MOD (see Table 9). Upon reset, the DCEN bit is set to 0 so that timer 2 will default to count up. When DCEN is set, Timer 2 can count up or down, depending on the value of the T2EX pin.

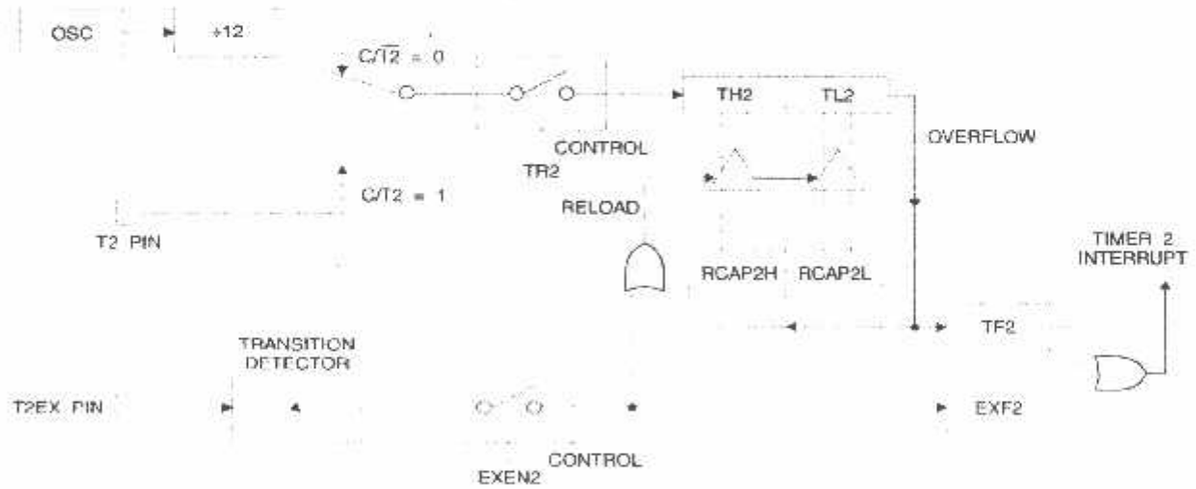
Figure 2 shows Timer 2 automatically counting up when DCEN = 0. In this mode, two options are selected by bit EXEN2 in T2CON. If EXEN2 = 0, Timer 2 counts up to 0FFFFH and then sets the TF2 bit upon overflow. The overflow also causes the timer registers to be reloaded with the 16-bit value in RCAP2H and RCAP2L. The values in RCAP2H and RCAP2L are preset by software. If EXEN2 = 1, a 16-bit reload can be triggered either by an overflow or by a 1-to-0 transition at external input T2EX. This transition also sets the EXF2 bit. Both the TF2 and EXF2 bits can generate an interrupt if enabled.

Setting the DCEN bit enables Timer 2 to count up or down, as shown in Figure 3. In this mode, the T2EX pin controls the direction of the count. A logic 1 at T2EX makes Timer 2 count up. The timer will overflow at 0FFFFH and set the TF2 bit. This overflow also causes the 16-bit value in RCAP2H and RCAP2L to be reloaded into the timer registers, TH2 and TL2, respectively.

A logic 0 at T2EX makes Timer 2 count down. The timer underflows when TH2 and TL2 equal the values stored in RCAP2H and RCAP2L. The underflow sets the TF2 bit and causes 0FFFFH to be reloaded into the timer registers.

The EXF2 bit toggles whenever Timer 2 overflows or underflows and can be used as a 17th bit of resolution. In this operating mode, EXF2 does not flag an interrupt.

ure 2. Timer 2 in Auto Reload Mode (DCEN = 0)



Lampiran

PIC16F87XA
Data Sheet

28/40/44-Pin Enhanced Flash Microcontrollers

MICROCHIP

PIC16F87XA

28/40/44-Pin Enhanced Flash Microcontrollers

Devices Included in this Data Sheet:

- PIC16F873A
- PIC16F874A
- PIC16F876A
- PIC16F877A

High-Performance RISC CPU:

- Only 35 single-word instructions to learn
- All single-cycle instructions except for program branches, which are two-cycle
- Operating speed: DC – 20 MHz clock input
  DC – 200 ns instruction cycle
- Up to 8K x 14 words of Flash Program Memory, Up to 368 x 8 bytes of Data Memory (RAM), Up to 256 x 8 bytes of EEPROM Data Memory
- Pinout compatible to other 28-pin or 40/44-pin PIC16CXXX and PIC16FXXX microcontrollers

Peripheral Features:

- Timer0: 8-bit timer/counter with 8-bit prescaler
- Timer1: 16-bit timer/counter with prescaler, can be incremented during Sleep via external crystal/clock
- Timer2: 8-bit timer/counter with 8-bit period register, prescaler and postscaler
- Two Capture, Compare, PWM modules
  - Capture is 16-bit, max. resolution is 12.5 ns
  - Compare is 16-bit, max. resolution is 200 ns
  - PWM max. resolution is 10-bit
- Synchronous Serial Port (SSP) with SPI™ (Master mode) and I^2C™ (Master/Slave)
- Universal Synchronous Asynchronous Receiver Transmitter (USART/SCI) with 9-bit address detection
- Parallel Slave Port (PSP) – 8 bits wide with external $\overline{RD}$, $\overline{WR}$ and $\overline{CS}$ controls (40/44-pin only)
- Brown-out detection circuitry for Brown-out Reset (BOR)

Analog Features:

- 10-bit, up to 8-channel Analog-to-Digital Converter (A/D)
- Brown-out Reset (BOR)
- Analog Comparator module with:
  - Two analog comparators
  - Programmable on-chip voltage reference (V_{REF}) module
  - Programmable input multiplexing from device inputs and internal voltage reference
  - Comparator outputs are externally accessible

Special Microcontroller Features:

- 100,000 erase/write cycle Enhanced Flash program memory typical
- 1,000,000 erase/write cycle Data EEPROM memory typical
- Data EEPROM Retention > 40 years
- Self-reprogrammable under software control
- In-Circuit Serial Programming™ (ICSP™) via two pins
- Single-supply 5V In-Circuit Serial Programming
- Watchdog Timer (WDT) with its own on-chip RC oscillator for reliable operation
- Programmable code protection
- Power saving Sleep mode
- Selectable oscillator options
- In-Circuit Debug (ICD) via two pins

CMOS Technology:

- Low-power, high-speed Flash/EEPROM technology
- Fully static design
- Wide operating voltage range (2.0V to 5.5V)
- Commercial and Industrial temperature ranges
- Low-power consumption

Device	Program Memory		Data SRAM (Bytes)	EEPROM (Bytes)	I/O	10-bit A/D (ch)	CCP (PWM)	MSSP		USART	Timers 8/16-bit	Comparators
	Bytes	# Single Word Instructions						SPI	Master I^2C			
PIC16F873A	7.2K	4096	192	128	22	5	2	Yes	Yes	Yes	2/1	2
PIC16F874A	7.2K	4096	192	128	33	8	2	Yes	Yes	Yes	2/1	2
PIC16F876A	14.3K	8192	368	256	22	5	2	Yes	Yes	Yes	2/1	2
PIC16F877A	14.3K	8192	368	256	33	8	2	Yes	Yes	Yes	2/1	2

Pin Diagrams (Continued)

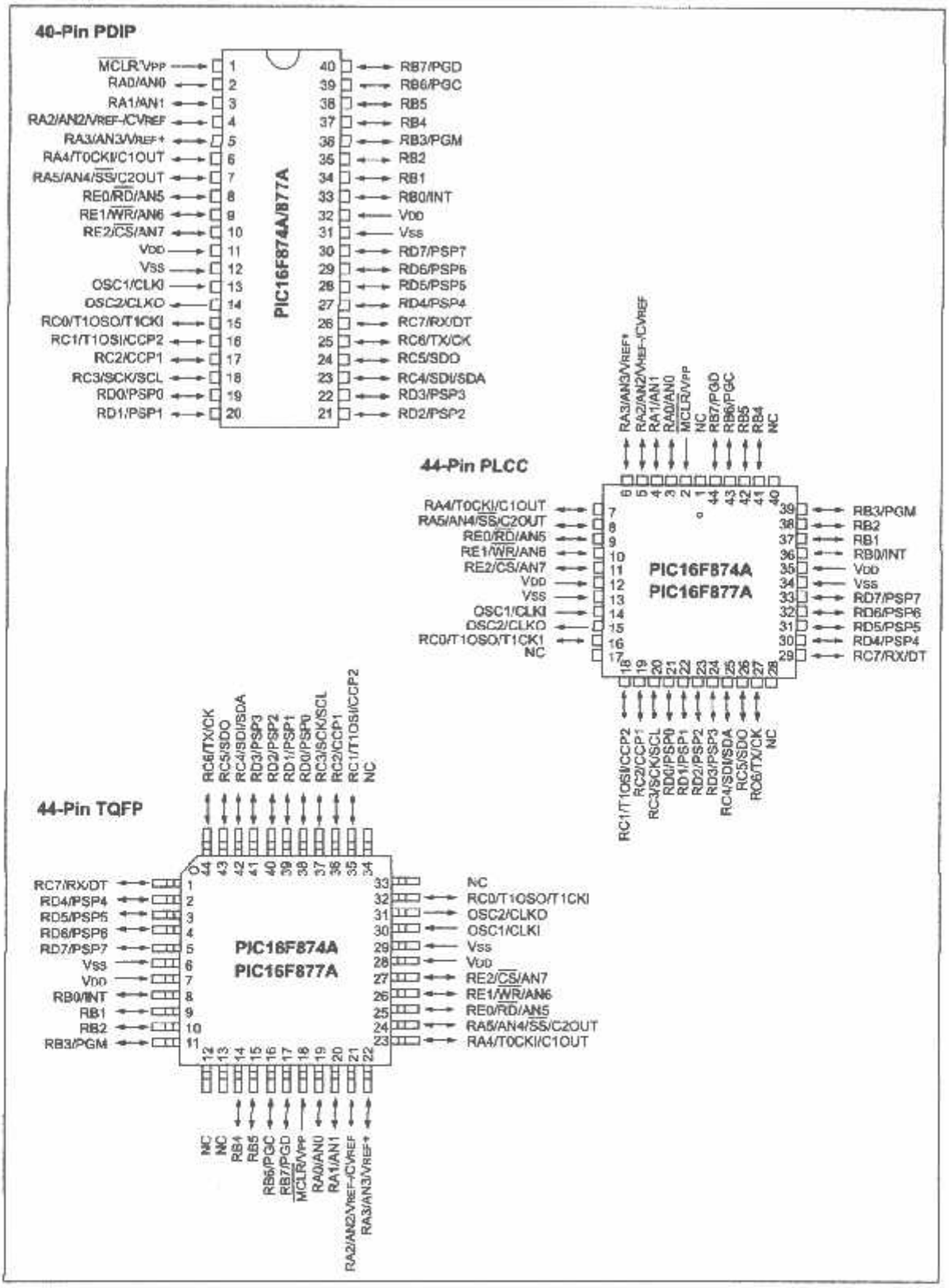
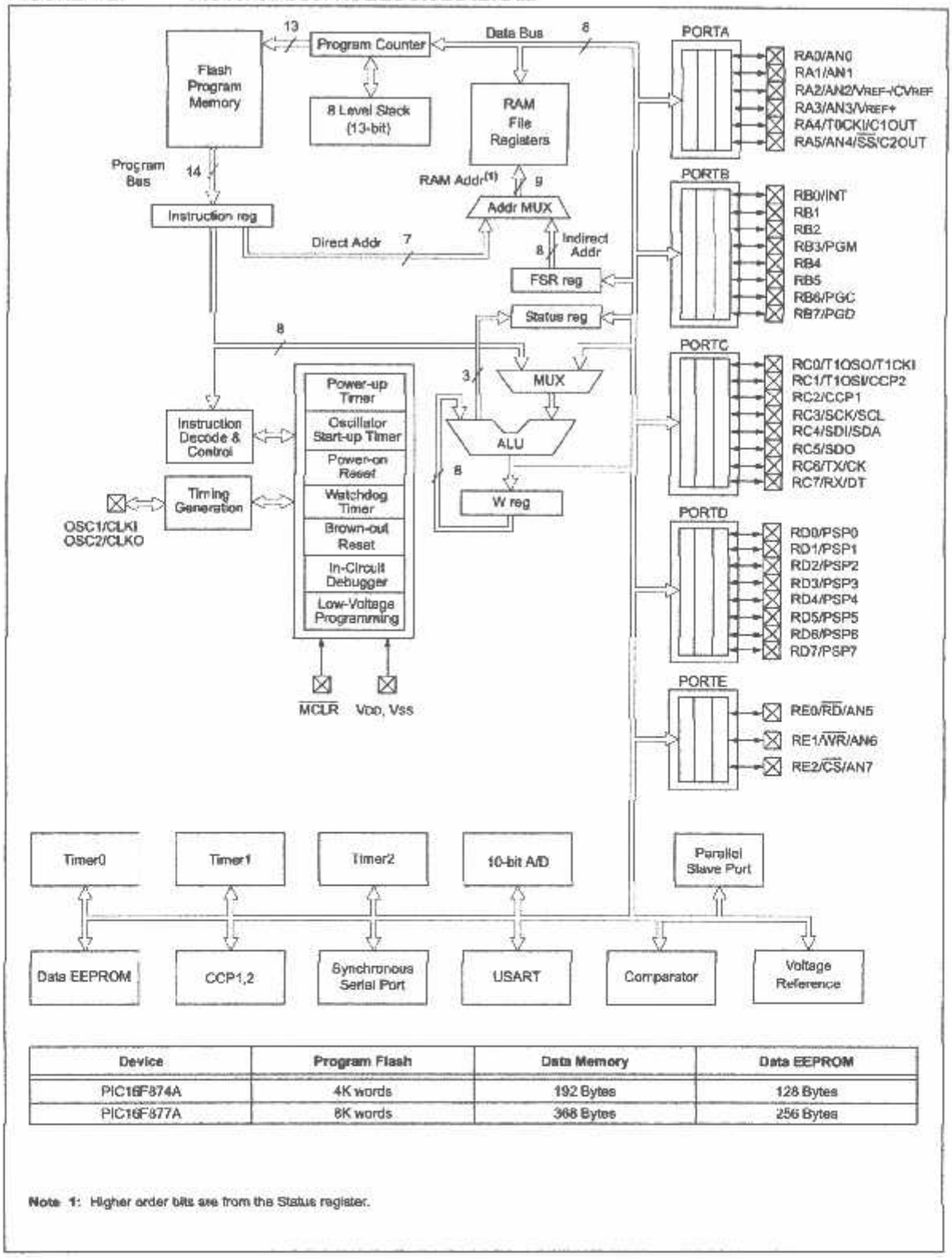


FIGURE 1-2: PIC16F874A/877A BLOCK DIAGRAM



Device	Program Flash	Data Memory	Data EEPROM
PIC16F874A	4K words	192 Bytes	128 Bytes
PIC16F877A	8K words	368 Bytes	256 Bytes

Note 1: Higher order bits are from the Status register.

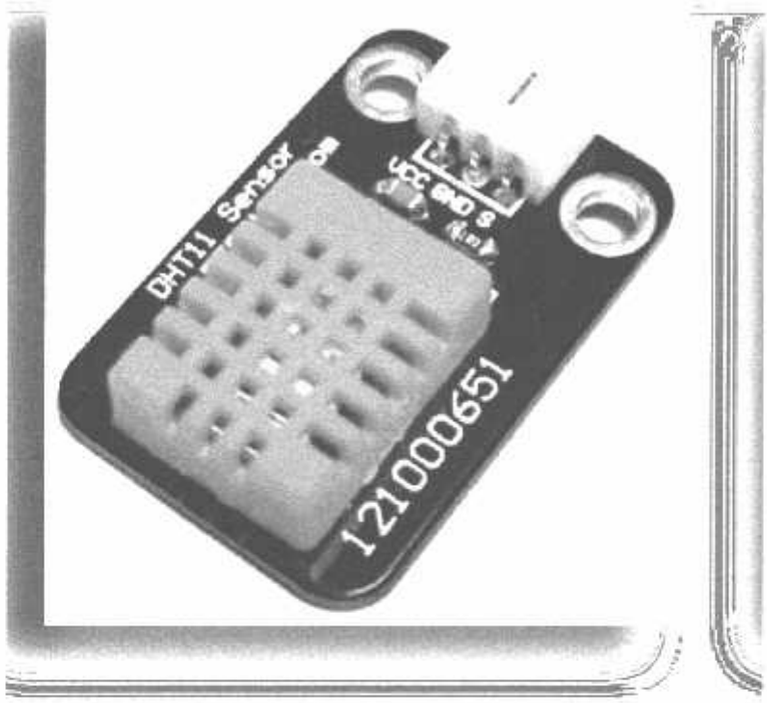
DHT11 Humidity & Temperature Sensor

D-Robotics UK (www.droboticsonline.com)

DHT11 Temperature & Humidity Sensor features a temperature & humidity sensor complex with a calibrated digital signal output.

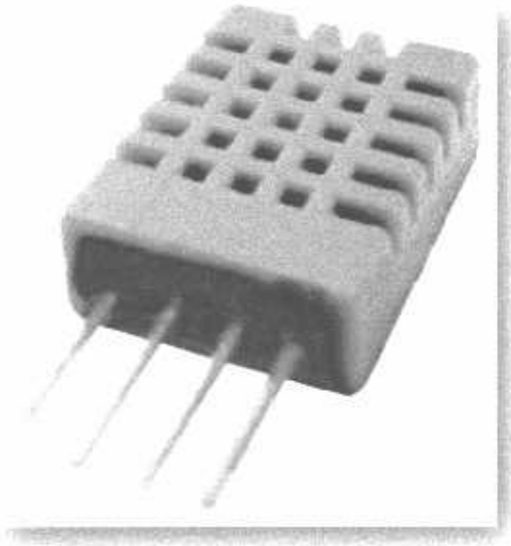
D-Robotics
7/30/2010

DHT 11 Humidity & Temperature Sensor



1. Introduction

This DFRobot DHT11 Temperature & Humidity Sensor features a temperature & humidity sensor complex with a calibrated digital signal output. By using the exclusive digital-signal-acquisition technique and temperature & humidity sensing technology, it ensures high reliability and excellent long-term stability. This sensor includes a resistive-type humidity measurement component and an NTC temperature measurement component, and connects to a high-performance 8-bit microcontroller, offering excellent quality, fast response, anti-interference ability and cost-effectiveness.



Each DHT11 element is strictly calibrated in the laboratory that is extremely accurate on humidity calibration. The calibration coefficients are stored as programmes in the OTP memory, which are used by the sensor's internal signal detecting process. The single-wire serial interface makes system integration quick and easy. Its small size, low power consumption and up-to-20 meter signal transmission making it the best choice for various applications, including those most demanding ones. The component is 4-pin single row pin package. It is convenient to connect and special packages can be provided according to users' request.

2. Technical Specifications:

Overview:

Item	Measurement Range	Humidity Accuracy	Temperature Accuracy	Resolution	Package
DHT11	20-90%RH 0-50 ℃	±5%RH	±2℃	1	4 Pin Single Row

Detailed Specifications:

Parameters	Conditions	Minimum	Typical	Maximum
Humidity				
Resolution		1%RH	1%RH	1%RH
			8 Bit	
Repeatability			±1%RH	
Accuracy	25℃		±4%RH	
	0-50℃			±5%RH
Interchangeability	Fully Interchangeable			
Measurement Range	0℃	30%RH		90%RH
	25℃	20%RH		90%RH
	50℃	20%RH		80%RH
Response Time (Seconds)	1/e(63%)25℃, 1m/s Air	6 S	10 S	15 S
Hysteresis			±1%RH	
Long-Term Stability	Typical		±1%RH/year	
Temperature				
Resolution		1℃	1℃	1℃
		8 Bit	8 Bit	8 Bit
Repeatability			±1℃	
Accuracy		±1℃		±2℃
Measurement Range		0℃		50℃
Response Time (Seconds)	1/e(63%)	6 S		30 S

3. Typical Application (Figure 1)

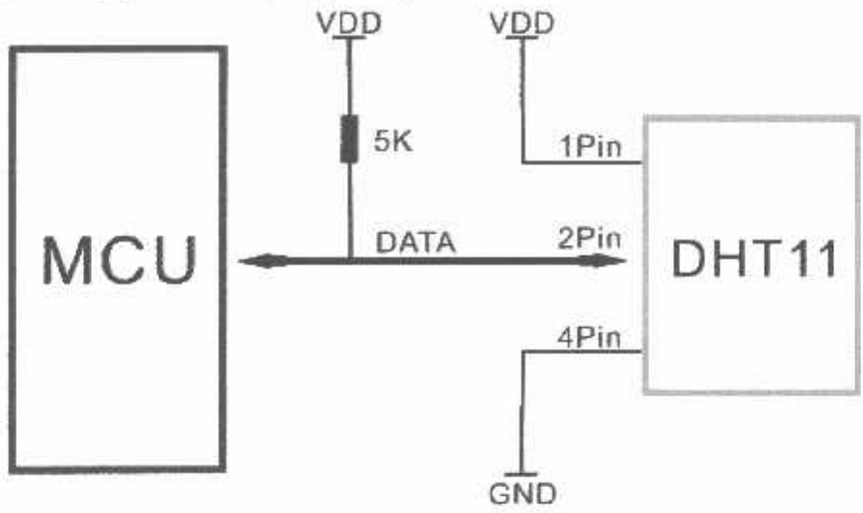


Figure 1 Typical Application

Note: 3Pin – Null; MCU = Micro-computer Unite or single chip Computer

When the connecting cable is shorter than 20 metres, a 5K pull-up resistor is recommended; when the connecting cable is longer than 20 metres, choose a appropriate pull-up resistor as needed.

4. Power and Pin

DHT11's power supply is 3-5.5V DC. When power is supplied to the sensor, do not send any instruction to the sensor in within one second in order to pass the unstable status. One capacitor valued 100nF can be added between VDD and GND for power filtering.

5. Communication Process: Serial Interface (Single-Wire Two-Way)

Single-bus data format is used for communication and synchronization between MCU and DHT11 sensor. One communication process is about 4ms.

Data consists of decimal and integral parts. A complete data transmission is **40bit**, and the sensor sends **higher data bit** first.

Data format: 8bit integral RH data + 8bit decimal RH data + 8bit integral T data + 8bit decimal T data + 8bit check sum. If the data transmission is right, the check-sum should be the last 8bit of "*8bit integral RH data + 8bit decimal RH data + 8bit integral T data + 8bit decimal T data*".

5.1 Overall Communication Process (Figure 2, below)

When MCU sends a start signal, DHT11 changes from the low-power-consumption mode to the running-mode, waiting for MCU completing the start signal. Once it is completed, DHT11 sends a response signal of 40-bit data that include the relative humidity and temperature information to MCU. Users can choose to collect (read) some data. Without the start signal from MCU, DHT11 will not give the response signal to MCU. Once data is collected, DHT11 will change to the low-power-consumption mode until it receives a start signal from MCU again.

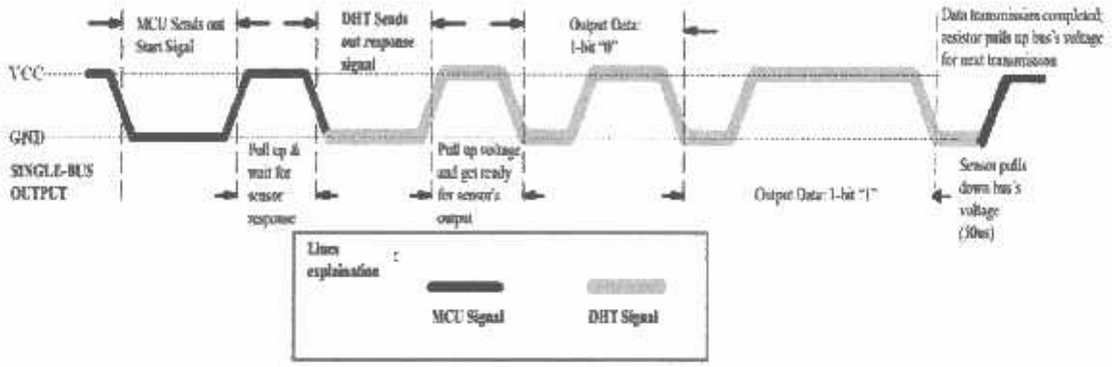


Figure 2 Overall Communication Process

5.2 MCU Sends out Start Signal to DHT (Figure 3, below)

Data Single-bus free status is at high voltage level. When the communication between MCU and DHT11 begins, the programme of MCU will set Data Single-bus voltage level from high to low and this process must take at least 18ms to ensure DHT's detection of MCU's signal, then MCU will pull up voltage and wait 20-40us for DHT's response.

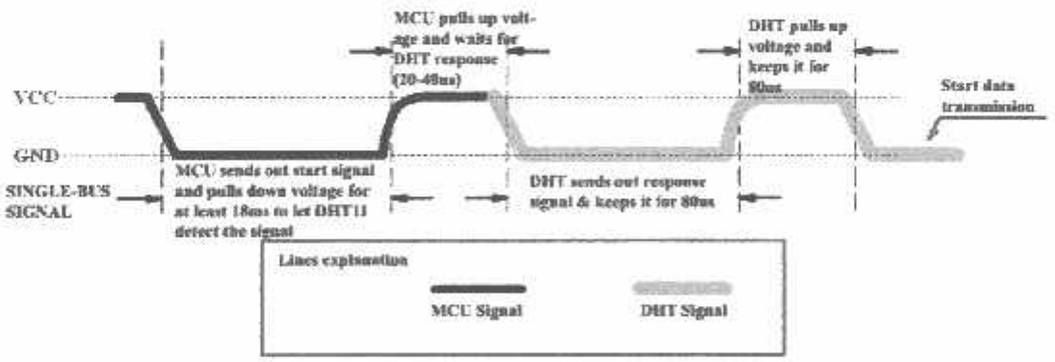


Figure 3 MCU Sends out Start Signal & DHT Responses

5.3 DHT Responses to MCU (Figure 3, above)

Once DHT detects the start signal, it will send out a low-voltage-level response signal, which lasts 80us. Then the programme of DHT sets Data Single-bus voltage level from low to high and keeps it for 80us for DHT's preparation for sending data.

When DATA Single-Bus is at the low voltage level, this means that DHT is sending the response signal. Once DHT sent out the response signal, it pulls up voltage and keeps it for 80us and prepares for data transmission.

When DHT is sending data to MCU, every bit of data begins with the 50us low-voltage-level and the length of the following high-voltage-level signal determines whether data bit is "0" or "1" (see Figures 4 and 5 below).

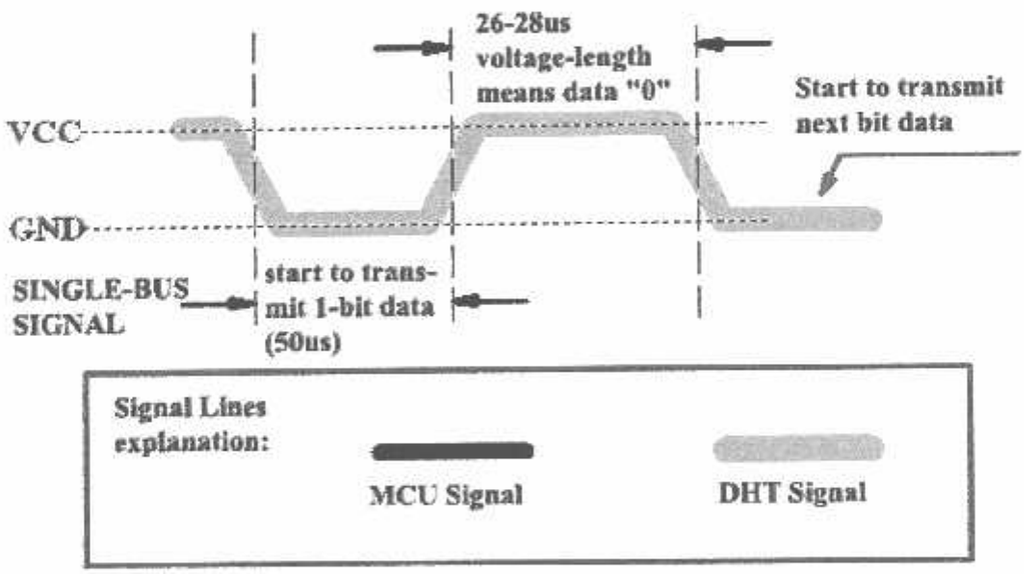


Figure 4 Data "0" Indication

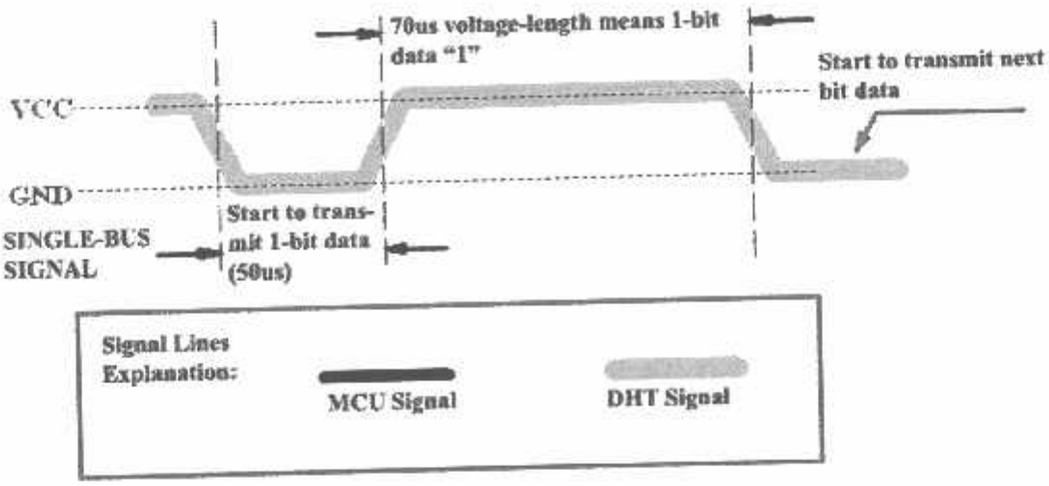


Figure 5 Data "1" Indication

If the response signal from DHT is always at high-voltage-level, it suggests that DHT is not responding properly and please check the connection. When the last bit data is transmitted, DHT11 pulls down the voltage level and keeps it for 50us. Then the Single-Bus voltage will be pulled up by the resistor to set it back to the free status.

6. Electrical Characteristics

VDD=5V, T = 25℃ (unless otherwise stated)

	Conditions	Minimum	Typical	Maximum
Power Supply	DC	3V	5V	5.5V
Current Supply	Measuring	0.5mA		2.5mA
	Average	0.2mA		1mA
	Standby	100uA		150uA
Sampling period	Second	1		

Note: Sampling period at intervals should be no less than 1 second.

7. Attentions of application

(1) Operating conditions

Applying the DHT11 sensor beyond its working range stated in this datasheet can result in 3%RH signal shift/discrepancy. The DHT11 sensor can recover to the calibrated status gradually when it gets back to the normal operating condition and works within its range. Please refer to (3) of

this section to accelerate its recovery. Please be aware that operating the DHT11 sensor in the non-normal working conditions will accelerate sensor's aging process.

(2) Attention to chemical materials

Vapor from chemical materials may interfere with DHT's sensitive-elements and debase its sensitivity. A high degree of chemical contamination can permanently damage the sensor.

(3) Restoration process when (1) & (2) happen

Step one: Keep the DHT sensor at the condition of Temperature 50~60Celsius, humidity <10%RH for 2 hours;
Step two:K keep the DHT sensor at the condition of Temperature 20~30Celsius, humidity >70%RH for 5 hours.

(4) Temperature Affect

Relative humidity largely depends on temperature. Although temperature compensation technology is used to ensure accurate measurement of RH, it is still strongly advised to keep the humidity and temperature sensors working under the same temperature. DHT11 should be mounted at the place as far as possible from parts that may generate heat.

(5) Light Affect

Long time exposure to strong sunlight and ultraviolet may debase DHT's performance.

(6) Connection wires

The quality of connection wires will affect the quality and distance of communication and high quality shielding-wire is recommended.

(7) Other attentions

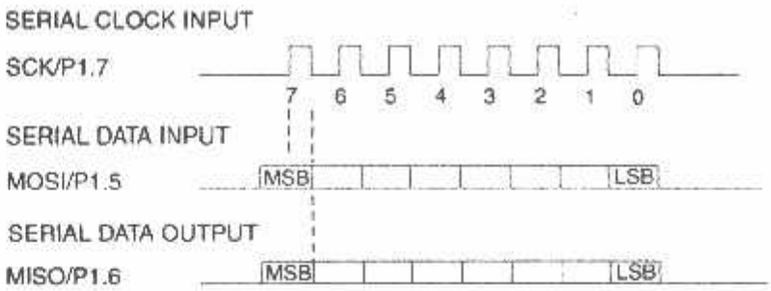
* Welding temperature should be bellow 260Celsius and contact should take less than 10 seconds.
* Avoid using the sensor under dew condition.
* Do not use this product in safety or emergency stop devices or any other occasion that failure of DHT11 may cause personal injury.
* Storage: Keep the sensor at temperature 10-40℃, humidity <60%RH.

Declaim:

D-Robotics: www.droboticsonline.com

Email contact: d_robotics@hotmail.co.uk

Serial Downloading Waveforms



Serial Programming Characteristics

Figure 16. Serial Programming Timing

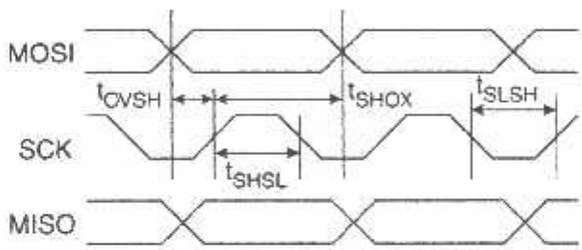


Table 11. Serial Programming Characteristics, T_A = -40°C to 85°C, V_{CC} = 4.0 - 6.0V (Unless Otherwise Noted)

Symbol	Parameter	Min	Typ	Max	Units
$1/t_{CLCL}$	Oscillator Frequency	0		24	MHz
t_{CLCL}	Oscillator Period	41.6			ns
t_{SHSL}	SCK Pulse Width High	24 t_{CLCL}			ns
t_{SLSH}	SCK Pulse Width Low	24 t_{CLCL}			ns
t_{OVSH}	MOSI Setup to SCK High	t_{CLCL}			ns
t_{SHOX}	MOSI Hold after SCK High	2 t_{CLCL}			ns

Absolute Maximum Ratings*

Operating Temperature	-55°C to +125°C
Storage Temperature	-65°C to +150°C
Voltage on Any Pin with Respect to Ground	-1.0V to +7.0V
Maximum Operating Voltage	6.6V
DC Output Current	15.0 mA

*NOTICE: Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC Characteristics

The values shown in this table are valid for T_A = -40°C to 85°C and V_{CC} = 5.0V ± 20%, unless otherwise noted.

Symbol	Parameter	Condition	Min	Max	Units
V_{IL}	Input Low-voltage	(Except $\overline{EA}$)	-0.5	0.2 V_{CC} - 0.1	V
V_{IL1}	Input Low-voltage ($\overline{EA}$)		0.5	0.2 V_{CC} 0.3	V
V_{IH}	Input High-voltage	(Except XTAL1, RST)	0.2 V_{CC} + 0.9	V_{CC} + 0.5	V
V_{IH1}	Input High-voltage	(XTAL1, RST)	0.7 V_{CC}	V_{CC} + 0.5	V
V_{OL}	Output Low-voltage (1) (Ports 1,2,3)	I_{OL} = 1.6 mA		0.5	V
V_{OL1}	Output Low-voltage (1) (Port 0, ALE, $\overline{PSEN}$)	I_{OL} = 3.2 mA		0.5	V
V_{OH}	Output High-voltage (Ports 1,2,3, ALE, $\overline{PSEN}$)	I_{OH} = -60 µA, V_{CC} = 5V ± 10%	2.4		V
		I_{OH} = -25 µA	0.75 V_{CC}		V
		I_{OH} = -10 µA	0.9 V_{CC}		V
V_{OH1}	Output High-voltage (Port 0 in External Bus Mode)	I_{OH} = -800 µA, V_{CC} = 5V ± 10%	2.4		V
		I_{OH} = -300 µA	0.75 V_{CC}		V
		I_{OH} = -80 µA	0.9 V_{CC}		V
I_{IL}	Logical 0 Input Current (Ports 1,2,3)	V_{IN} = 0.45V		-50	µA
I_{TL}	Logical 1 to 0 Transition Current (Ports 1,2,3)	V_{IN} = 2V, V_{CC} = 5V ± 10%		-650	µA
I_{LI}	Input Leakage Current (Port 0, $\overline{EA}$)	0.45 < V_{IN} < V_{CC}		±10	µA
RRST	Reset Pull-down Resistor		50	300	KΩ
C_{IO}	Pin Capacitance	Test Freq. = 1 MHz, T_A = 25°C		10	pF
I_{CC}	Power Supply Current	Active Mode, 12 MHz		25	mA
		Idle Mode, 12 MHz		6.5	mA
	Power-down Mode (2)	V_{CC} = 6V		100	µA
		V_{CC} = 3V		40	µA

Notes: 1. Under steady state (non-transient) conditions, I_{OL} must be externally limited as follows:
Maximum I_{OL} per port pin: 10 mA
Maximum I_{OL} per 8-bit port: Port 0: 26 mA; Ports 1, 2, 3: 15 mA
Maximum total I_{OL} for all output pins: 71 mA
If I_{OL} exceeds the test condition, V_{OL} may exceed the related specification. Pins are not guaranteed to sink current greater than the listed test conditions.
2. Minimum V_{CC} for Power-down is 2V

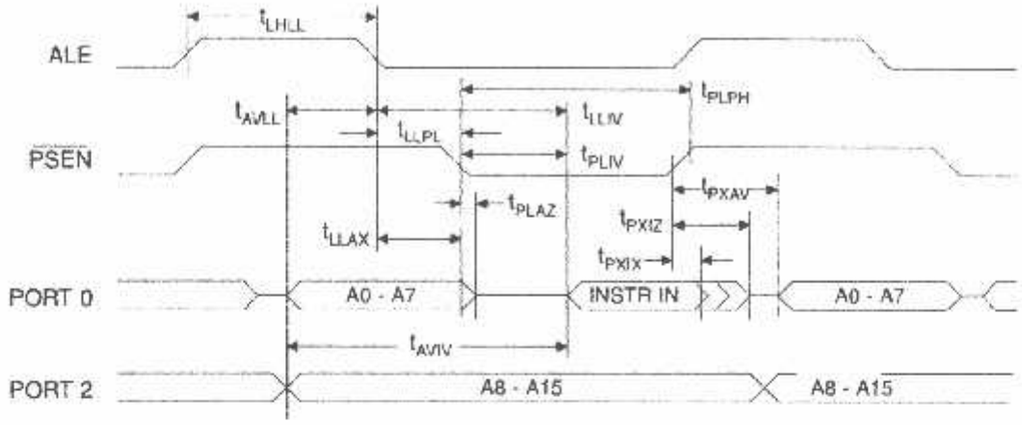
AC Characteristics

Under operating conditions, load capacitance for Port 0, ALE/$\overline{PROG}$, and $\overline{PSEN}$ = 100 pF; load capacitance for all other outputs = 80 pF.

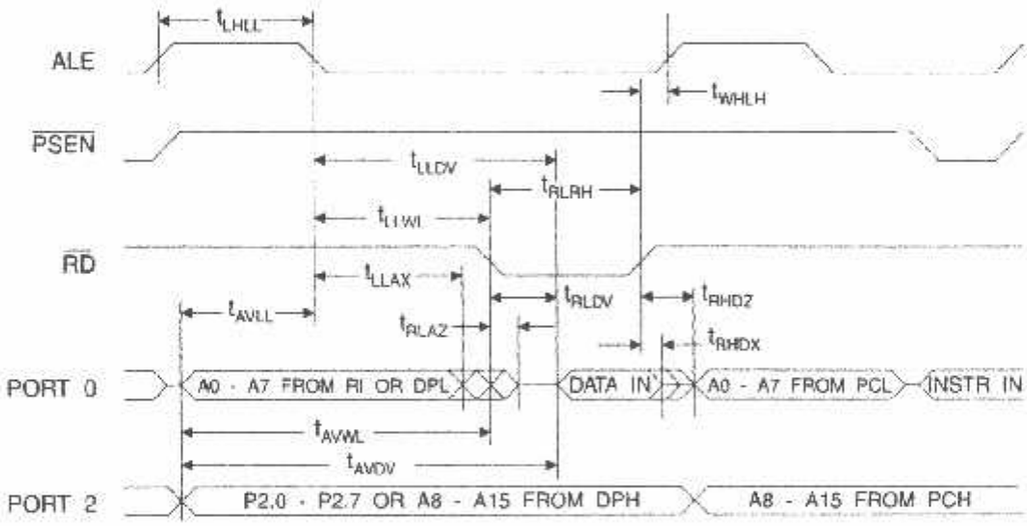
External Program and Data Memory Characteristics

Symbol	Parameter	Variable Oscillator		Units
		Min	Max	
$1/t_{CLCL}$	Oscillator Frequency	0	24	MHz
t_{LHLL}	ALE Pulse Width	$2t_{CLCL}$ - 40		ns
t_{AVLL}	Address Valid to ALE Low	t_{CLCL} - 13		ns
t_{LLAX}	Address Hold after ALE Low	t_{CLCL} - 20		ns
t_{LLIV}	ALE Low to Valid Instruction In		$4t_{CLCL}$ - 65	ns
t_{LLPL}	ALE Low to $\overline{PSEN}$ Low	t_{CLCL} - 13		ns
t_{PLPH}	$\overline{PSEN}$ Pulse Width	$3t_{CLCL}$ - 20		ns
t_{PLIV}	$\overline{PSEN}$ Low to Valid Instruction In		$3t_{CLCL}$ - 45	ns
t_{PXIX}	Input Instruction Hold after $\overline{PSEN}$	0		ns
t_{PXIZ}	Input Instruction Float after $\overline{PSEN}$		t_{CLCL} - 10	ns
t_{PXAV}	$\overline{PSEN}$ to Address Valid	t_{CLCL} - 8		ns
t_{AVIV}	Address to Valid Instruction In		$5t_{CLCL}$ - 55	ns
t_{PLAZ}	$\overline{PSEN}$ Low to Address Float		10	ns
t_{RLRH}	$\overline{RD}$ Pulse Width	$6t_{CLCL}$ - 100		ns
t_{WLWH}	$\overline{WR}$ Pulse Width	$6t_{CLCL}$ - 100		ns
t_{RLDV}	$\overline{RD}$ Low to Valid Data In		$5t_{CLCL}$ - 90	ns
t_{RHDX}	Data Hold after $\overline{RD}$	0		ns
t_{RHDZ}	Data Float after $\overline{RD}$		$2t_{CLCL}$ - 28	ns
t_{LLDV}	ALE Low to Valid Data In		$8t_{CLCL}$ - 150	ns
t_{AVDV}	Address to Valid Data In		$9t_{CLCL}$ - 165	ns
t_{LLWL}	ALE Low to $\overline{RD}$ or $\overline{WR}$ Low	$3t_{CLCL}$ - 50	$3t_{CLCL}$ + 50	ns
t_{AVWL}	Address to $\overline{RD}$ or $\overline{WR}$ Low	$4t_{CLCL}$ - 75		ns
t_{QVWX}	Data Valid to $\overline{WR}$ Transition	t_{CLCL} - 20		ns
t_{QVWH}	Data Valid to $\overline{WR}$ High	$7t_{CLCL}$ - 120		ns
t_{WHQX}	Data Hold after $\overline{WR}$	t_{CLCL} - 20		ns
t_{RLAZ}	$\overline{RD}$ Low to Address Float		0	ns
t_{WHLH}	$\overline{RD}$ or $\overline{WR}$ High to ALE High	t_{CLCL} - 20	t_{CLCL} + 25	ns

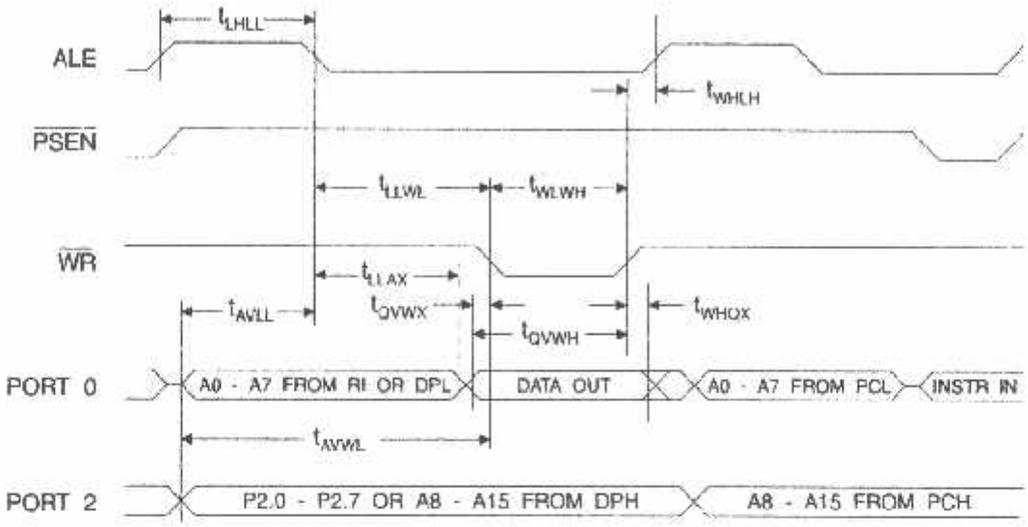
External Program Memory Read Cycle



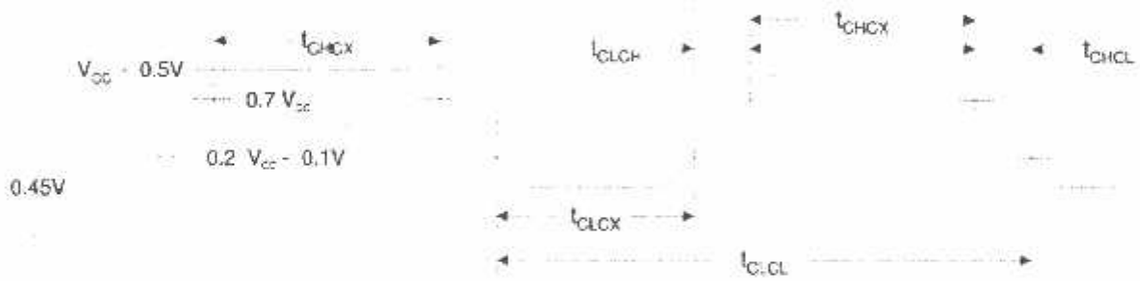
External Data Memory Read Cycle



External Data Memory Write Cycle



External Clock Drive Waveforms



External Clock Drive

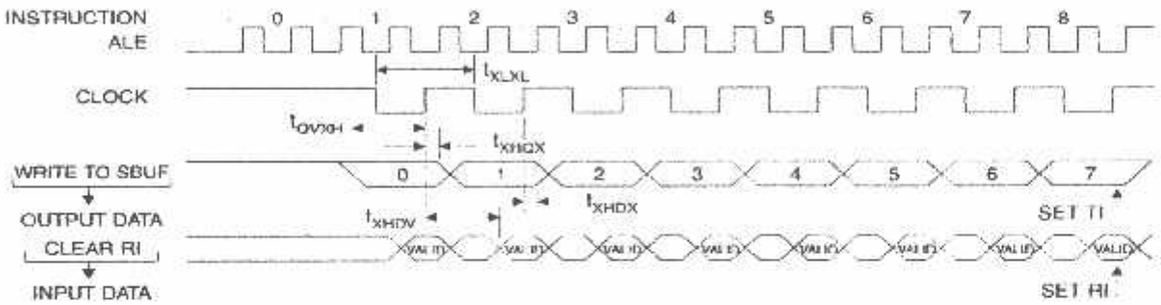
Symbol	Parameter	V_{CC} = 4.0V to 6.0V Min	Max	Units
$1/t_{CLCL}$	Oscillator Frequency	0	24	MHz
t_{CLCL}	Clock Period	41.6		ns
t_{CHCX}	High Time	15		ns
t_{CLCX}	Low Time	15		ns
t_{CLCH}	Rise Time		20	ns
t_{CHCL}	Fall Time		20	ns

Serial Port Timing: Shift Register Mode Test Conditions

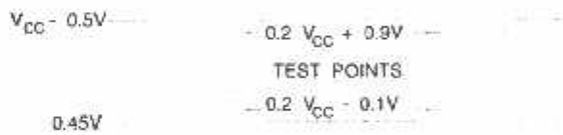
The values in this table are valid for V_{CC} = 4.0V to 6V and Load Capacitance = 80 pF.

Symbol	Parameter	Variable Oscillator		Units
		Min	Max	
t_{XLXL}	Serial Port Clock Cycle Time	$12t_{CLCL}$		µs
t_{QVXH}	Output Data Setup to Clock Rising Edge	$10t_{CLCL}$ - 133		ns
t_{XHQX}	Output Data Hold after Clock Rising Edge	$2t_{CLCL}$ - 117		ns
t_{XHDX}	Input Data Hold after Clock Rising Edge	0		ns
t_{XHDV}	Clock Rising Edge to Input Data Valid		$10t_{CLCL}$ - 133	ns

Shift Register Mode Timing Waveforms



AC Testing Input/Output Waveforms[1]



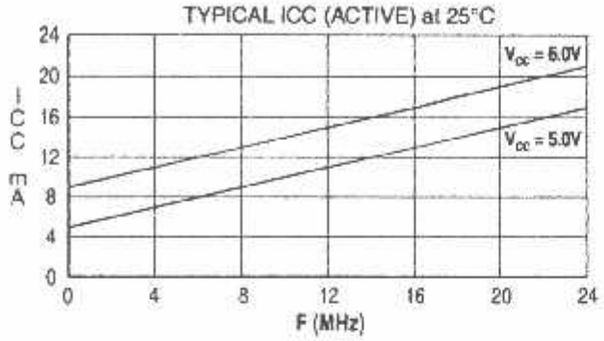
Note: 1. AC inputs during testing are driven at V_{CC} - 0.5V for a logic 1 and 0.45V for a logic 0. Timing measurements are made at V_{IH} min. for a logic 1 and V_{IL} max. for a logic 0.

Float Waveforms[1]

Note: 1. For timing purposes, a port pin is no longer floating when a 100 mV change from load voltage occurs. A port pin begins to float when a 100 mV change from the loaded V_{OH}/V_{OL} level occurs.

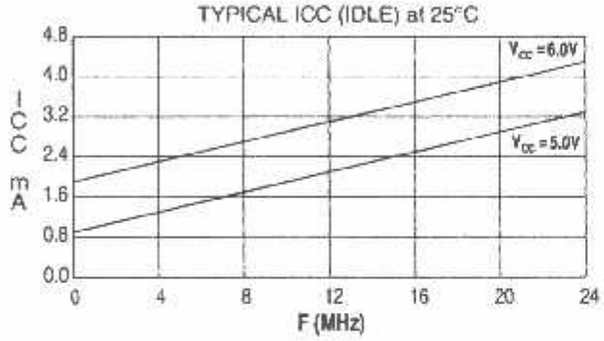
AT89S8252

TYPICAL ICC (ACTIVE) at 25°C



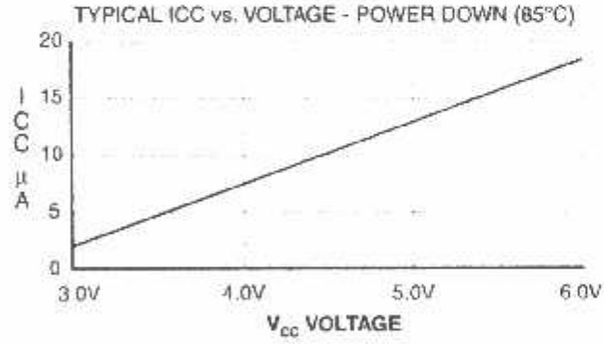
AT89S8252

TYPICAL ICC (IDLE) at 25°C



AT89S8252

TYPICAL ICC vs. VOLTAGE - POWER DOWN (85°C)



Notes: 1. XTAL1 tied to GND for Icc (power-down)
2. Lock bits programmed

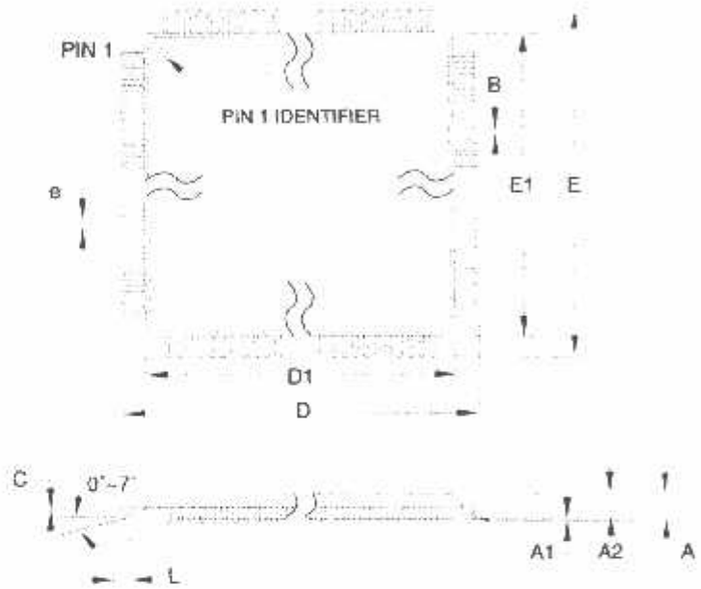
Ordering Information

Speed (MHz)	Power Supply	Ordering Code	Package	Operation Range
24	4.0V to 6.0V	AT89S8252-24AC	44A	Commercial (0°C to 70°C)
		AT89S8252-24JC	44J	
		AT89S8252-24PC	40P6	
	4.0V to 6.0V	AT89S8252-24AI	44A	Industrial (-40°C to 85°C)
		AT89S8252-24JI	44J	
		AT89S8252-24PI	40P6	

Package Type	
4A	44-lead, Thin Plastic Gull Wing Quad Flatpack (TQFP)
J	44-lead, Plastic J-leaded Chip Carrier (PLCC)
P6	40-lead, 0.600" Wide, Plastic Dual Inline Package (PDIP)

Packaging Information

44A – TQFP



COMMON DIMENSIONS
(Unit of Measure = mm)

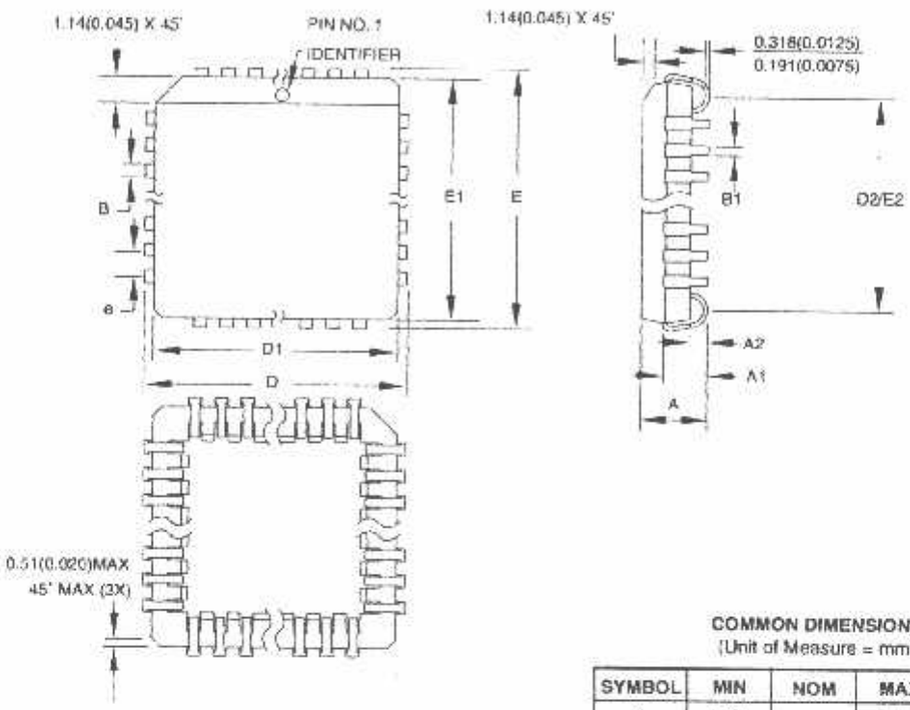
SYMBOL	MIN	NOM	MAX	NOTE
A	–	–	1.20	
A1	0.05	–	0.15	
A2	0.95	1.00	1.05	
D	11.75	12.00	12.25	
D1	9.90	10.00	10.10	Note 2
E	11.75	12.00	12.25	
E1	9.90	10.00	10.10	Note 2
B	0.30	–	0.45	
C	0.09	–	0.20	
L	0.45	–	0.75	
e	0.80 TYP			

Notes.
1. This package conforms to JEDEC reference MS-026, Variation ACB.
2. Dimensions D1 and E1 do not include mold protrusion. Allowable protrusion is 0.25 mm per side. Dimensions D1 and E1 are maximum plastic body size dimensions including mold mismatch.
3. Lead coplanarity is 0.10 mm maximum.

10/5/2001

	TITLE	DRAWING NO.	REV.
2325 Orchard Parkway San Jose, CA 95131	**44A**, 44-lead, 10 x 10 mm Body Size, 1.0 mm Body Thickness, 0.8 mm Lead Pitch, Thin Profile Plastic Quad Flat Package (TQFP)	44A	B

44J – PLCC



COMMON DIMENSIONS
(Unit of Measure = mm)

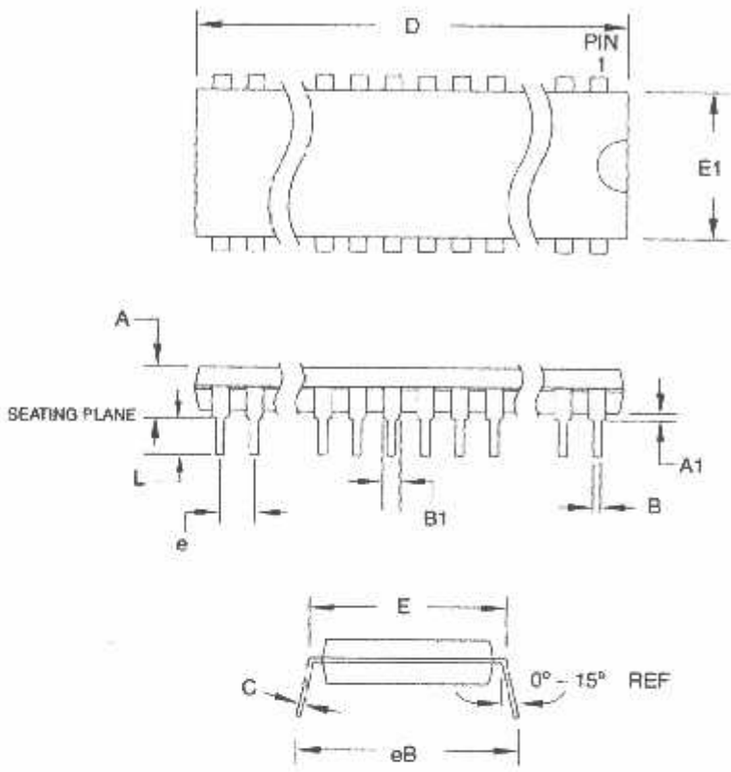
SYMBOL	MIN	NOM	MAX	NOTE
A	4.191	–	4.572	
A1	2.286	–	3.048	
A2	0.508	–	–	
D	17.399	–	17.653	
D1	16.510	–	16.662	Note 2
E	17.399	–	17.653	
E1	16.510	–	16.662	Note 2
D2/E2	14.986	–	16.002	
B	0.660	–	0.813	
B1	0.330	–	0.533	
e	1.270 TYP			

Notes:
1. This package conforms to JEDEC reference MS-016, Variation AC.
2. Dimensions D1 and E1 do not include mold protrusion. Allowable protrusion is .010"(0.254 mm) per side. Dimension D1 and E1 include mold mismatch and are measured at the extreme material condition at the upper or lower parting line.
3. Lead coplanarity is 0.004" (0.102 mm) maximum.

10/04/01

	TITLE	DRAWING NO.	REV.
2325 Orchard Parkway San Jose, CA 95131	44J, 44-lead, Plastic J-leaded Chip Carrier (PLCC)	44J	B

40P6 – PDIP



COMMON DIMENSIONS
(Unit of Measure = mm)

SYMBOL	MIN	NOM	MAX	NOTE
A	–	–	4.826	
A1	0.381	–	–	
D	52.070	–	52.578	Note 2
E	15.240	–	15.875	
E1	13.462	–	13.970	Note 2
B	0.356	–	0.559	
B1	1.041	–	1.651	
L	3.048	–	3.556	
C	0.203	–	0.381	
eB	15.494	–	17.526	
e	2.540 TYP			

Notes:
1. This package conforms to JEDEC reference MS-011, Variation AC.
2. Dimensions D and E1 do not include mold Flash or Protrusion. Mold Flash or Protrusion shall not exceed 0.25 mm (0.010").

09/28/01

	TITLE	DRAWING NO.	REV.
2325 Orchard Parkway San Jose, CA 95131	**40P6**, 40-lead (0.600"/15.24 mm Wide) Plastic Dual Inline Package (PDIP)	40P6	B

Atmel Corporation

2325 Orchard Parkway
San Jose, CA 95131, USA
Tel: 1(408) 441-0311
Fax: 1(408) 487-2600

Regional Headquarters

Europe
Atmel Sarl
Route des Arsenaux 41
Case Postale 80
CH-1705 Fribourg
Switzerland
Tel: (41) 26-426-5555
Fax: (41) 26-426-5500

Asia
Room 1219
Chinachem Golden Plaza
77 Mody Road Tsimshatsui
East Kowloon
Hong Kong
Tel: (852) 2721-9778
Fax: (852) 2722-1369

Japan
9F, Tonetsu Shinkawa Bldg.
1-24-8 Shinkawa
Chuo-ku, Tokyo 104-0033
Japan
Tel: (81) 3-3523-3551
Fax: (81) 3-3523-7581

Atmel Operations

Memory
2325 Orchard Parkway
San Jose, CA 95131, USA
Tel: 1(408) 441-0311
Fax: 1(408) 436-4314

Microcontrollers
2325 Orchard Parkway
San Jose, CA 95131, USA
Tel: 1(408) 441-0311
Fax: 1(408) 436-4314

La Chantrerie
BP 70602
44306 Nantes Cedex 3, France
Tel: (33) 2-40-18-18-18
Fax: (33) 2-40-18-19-60

ASIC/ASSP/Smart Cards
Zone Industrielle
13106 Rousset Cedex, France
Tel: (33) 4-42-53-60-00
Fax: (33) 4-42-53-60-01

1150 East Cheyenne Mtn. Blvd.
Colorado Springs, CO 80906, USA
Tel: 1(719) 576-3300
Fax: 1(719) 540-1759

Scottish Enterprise Technology Park
Maxwell Building
East Kilbride G75 0QR, Scotland
Tel: (44) 1355-803-000
Fax: (44) 1355-242-743

RF/Automotive
Theresienstrasse 2
Postfach 3535
74025 Heilbronn, Germany
Tel: (49) 71-31-67-0
Fax: (49) 71-31-67-2340

1150 East Cheyenne Mtn. Blvd.
Colorado Springs, CO 80906, USA
Tel: 1(719) 576-3300
Fax: 1(719) 540-1759

Biometrics/Imaging/Hi-Rel MPU/
High-Speed Converters/RF Datacom
Avenue de Rochepleine
BP 123
38521 Saint-Egreve Cedex, France
Tel: (33) 4-76-58-30-00
Fax: (33) 4-76-58-34-80

Literature Requests
www.atmel.com/literature

0401G–MICRO–3/06 xM

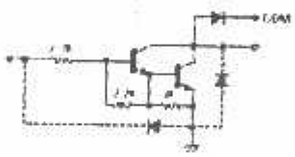
de KITS Application Note

AN1 - Relay Board

Oleh: Tim IE

Hardware

Relay merupakan salah satu komponen output yang paling sering digunakan baik pada industri, otomotif, ataupun peralatan elektronika lainnya. Relay berfungsi untuk menghubungkan atau memutus aliran arus listrik yang dikontrol dengan memberikan tegangan dan arus tertentu pada koilnya. Ada 2 macam relay berdasarkan tegangan untuk menggerakkan koilnya yaitu AC dan DC. Pada relay board ini digunakan relay DC dengan tegangan koil 12V DC,arus yang diperlukan sekitar 20-30mA. Karena itu pada umumnya kita tidak bisa langsung menghubungkan output suatu IC logic (TTL/CMOS) atau peripheral lain seperti µC 89C51 , PPI 82C55 dengan relay karena I_{OHmax} (arus maximum yang dikeluarkan pada saat logic '1') atau I_{OLmax} (arus maximum yang mampu dibenamkan pada saat logic '0') tidak cukup besar. Karena itu perlu digunakan driver untuk penguat arus yang biasanya berupa transistor, di sini digunakan "Darlington Array" ULN 2803A yang merupakan sekumpulan transistor dengan konfigurasi Darlington sehingga mempunyai β (penguatan arus) yang besar (lihat gambar 1).



Gambar 1. Konfigurasi Output ULN2803A

etiap output pada ULN 2803A dapat dibebani sampai 00mA, serta dilengkapi dengan 'supression diode'. iode ini berfungsi untuk mencegah 'kickback' yaitu ansient yang
rjadi pada koil relay (beban induktif) saat relay matikan . Fenomena ini bisa dianalisa dari rumus rikut :

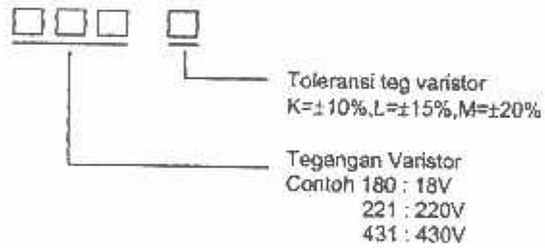
$$V = -L\frac{di}{dt}$$

yangkan bila terjadi perubahan arus yang cukup besar lam satuan waktu yang sangat cepat dt = 0 maka angan balik ini menjadi sangat besar, dan dapat ngakibatkan kerusakan pada transistor. Problem lain ng sering terjadi pada kontak relay adalah loncatan nga api listrik yang dapat memperpendek umur kontak. nga api ini terutama terjadi pada beban induktif seperti itor, solenoid, dll. Untuk mencegah hal ini digunakan OV (Metallic Oxide Varistor) yang dipasang secara

paralel dengan kontak. Varistor bersifat seperti resistor dengan nilai resistansinya tergantung pada tegangan. Ketika kontak
terbuka, beban induktif menghasilkan tegangan balik yang cukup besar akibat perubahan medan magnet. Pada saat ini ('protective state') nilai resistansi varistor menjadi sangat kecil dan arus akan mengalir melalui MOV, sehingga transient dapat diredam. Pada saat keadaan normal resistansi MOV sangat besar dan hanya menarik arus yang sangat kecil, bunga api juga menyebabkan sinyal Radio Frequency Interference (RFI) yang dapat mengganggu peralatan – peralatan sensitif. Karena itu komponen peredam transient seperti MOV sangat diperlukan terutama pada beban induktif.
Parameter-parameter penting Varistor :

- Tegangan Varistor (tegangan breakdown) :
  Tegangan pada varistor yang diukur pada arus tertentu (0,1 mA atau 1 mA) selama waktu tertentu
- Tegangan maksimum yang diperbolehkan :
  Tegangan maksimum pada varistor agar tetap pada keadaan normal ('rest state')

Cara membaca kode varistor pada umumnya

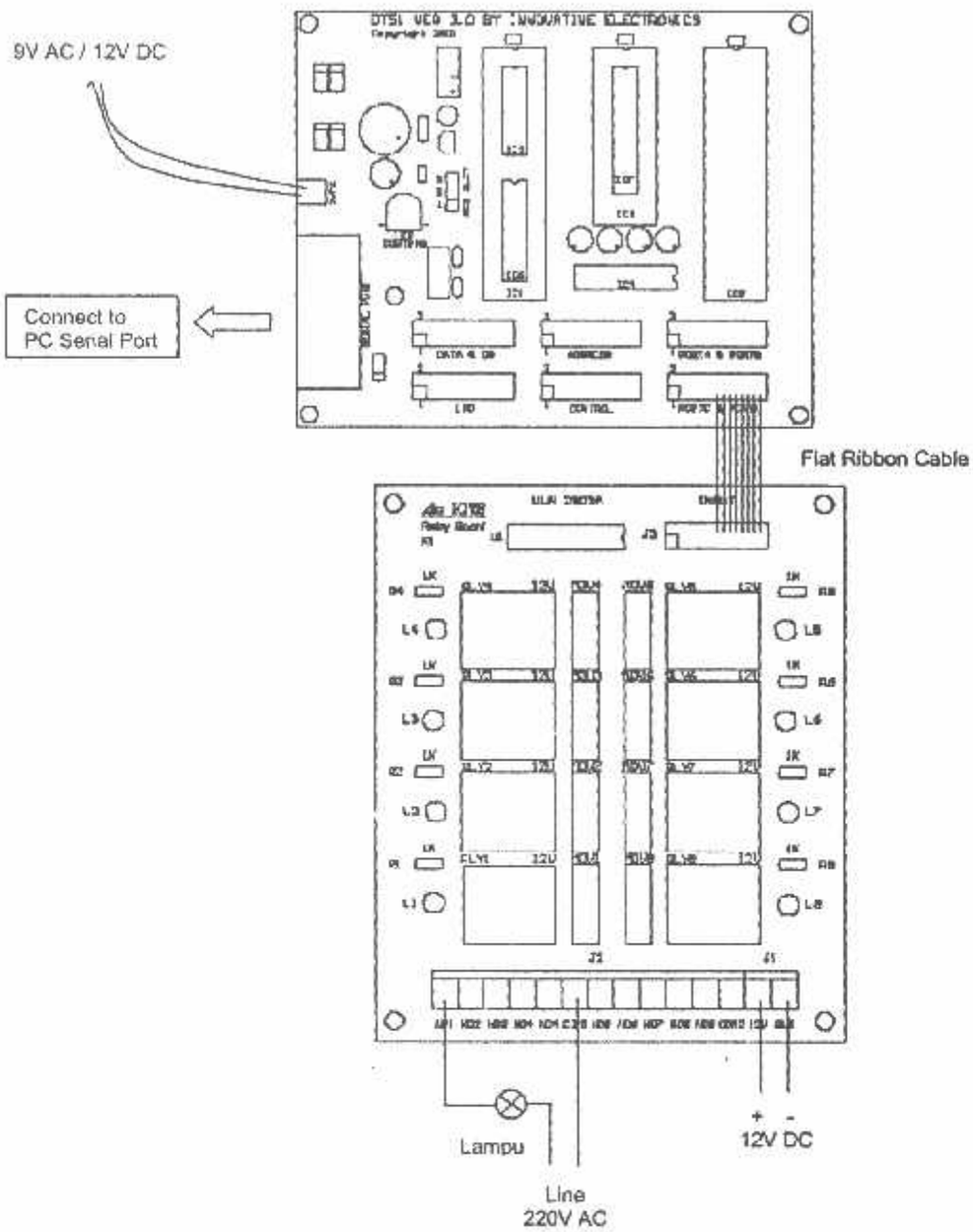


Pemilihan tegangan varistor tergantung pada tegangan beban yang dihubungkan pada relay.
Contoh :

Tegangan Supply	Tipe Varistor
12V DC	220K
24V DC	390K
110V AC	201K, 221K
220V AC	431K, 471K

Software

Pemrograman untuk mengendalikan relay board ini sangat sederhana. Bila menggunakan DT-51® Development Tools kita bisa memilih apakah menggunakan Port 1 (P1.0 ~ P1.7) atau Port A, B, dan C dari PPI (Programmable Peripheral Interface).
Pada gambar 2 ditunjukkan salah satu contoh aplikasi relay board, yaitu untuk mematikan dan menghidupkan lampu bohlam 220V AC. Input Relay Board (IN1-IN8) dihubungkan dengan Port 1 DT-51® Development Tools (P1.0-P1.7).



Gambar 2. Hubungan DT-51 MinSys Ver 3.0 dengan Relay Board

sting Program

erikut ini listing program (dengan Assembler ASM51)
tuk menyalakan lampu bohlam selama ± 15 detik,
mudian padam ± 15 detik secara periodik.

```
$TITLE(Demo RELAY BOARD dengan lampu bohlam)
$MOD51
                CSEG
```

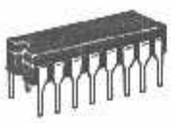
```
                ORG             4000H
                LJMP            Start
                ORG             4100H

Delay:          PUSH            06H
                PUSH            07H
                PUSH            05H
                PUSH            04H

                MOV             R4,#01H
DelayOutsLoop:  MOV             R5,#0AAH
DelayOutLoop:   MOV             R6,#0BBH
DelayOuterLoop: MOV             R7,#0CCH
DelayInnerLoop: DJNZ            R7,$
                DJNZ            R6,DelayOuterLoop
                DJNZ            R5,DelayOutLoop
                DJNZ            R4,DelayOutsLoop

                POP             04H
                POP             05H
                POP             07H
                POP             06H
                RET

Start:          SETB            P1.0
                ACALL           Delay
                CLR             P1.0
                ACALL           Delay
                AJMP            Start
                END
```

MC14049UB

ex Buffers

'he MC14049UB hex inverter/buffer is constructed with MOS P–channel
J N–channel enhancement mode devices in a single monolithic structure.
s complementary MOS device finds primary use where low power
sipation and/or high noise immunity is desired. This device provides
c–level conversion using only one supply voltage, V_{DD}. The input–signal
h level (V_{IH}) can exceed the V_{DD} supply voltage for logic–level
iversions. Two TTL/DTL Loads can be driven when the device is used as
OS–to–TTL/DTL converters (V_{DD} = 5.0 V, $V_{OL} \leq$ 0.4 V, $I_{OL} \geq$ 3.2 mA).
:e that pins 13 and 16 are not connected internally on this device;
:sequently connections to these terminals will not affect circuit operation.

- High Source and Sink Currents
- High–to–Low Level Converter
- Supply Voltage Range = 3.0 V to 18 V
- Meets JEDEC UB Specifications
- V_{IN} can exceed V_{DD}
- Improved ESD Protection on All Inputs



L SUFFIX
CERAMIC
CASE 620

P SUFFIX
PLASTIC
CASE 648

D SUFFIX
SOIC
CASE 751B

ORDERING INFORMATION

MC14XXXBCP	Plastic
MC14XXXBCL	Ceramic
MC14XXXBD	SOIC

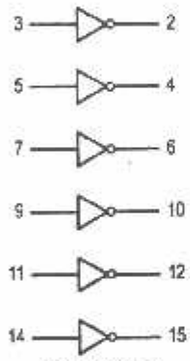
T_A = – 55° to 125°C for all packages.

AXIMUM RATINGS* (Voltages Referenced to V_{SS})

Rating	Symbol	Value	Unit
)C Supply Voltage	V_{DD}	– 0.5 to + 18	V
nput Voltage (DC or Transient)	V_{in}	– 0.5 to + 18	V
Output Voltage (DC or Transient)	V_{out}	– 0.5 to V_{DD} + 0.5	V
nput Current (DC or Transient), per Pin	I_{in}	± 10	mA
Output Current (DC or Transient), per Pin	I_{out}	+ 45	mA
Power Dissipation, per Package† Plastic/Ceramic SOIC	P_D	825 740	mW
Storage Temperature	T_{stg}	– 65 to + 150	°C
.ead Temperature (8–Second Soldering)	T_L	260	°C

Maximum Ratings are those values beyond which damage to the device may occur.
Temperature Derating: All Packages: See Figure 4.

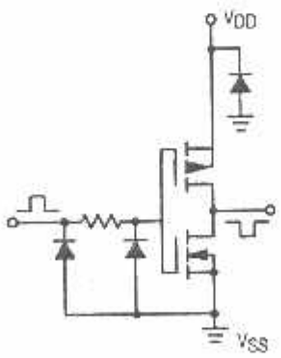
LOGIC DIAGRAM
MC14049UB



NC = PIN 13, 16
V_{SS} = PIN 8
V_{DD} = PIN 1

CIRCUIT SCHEMATIC
(1/6 OF CIRCUIT SHOWN)

MC14049UB



.ECTRICAL CHARACTERISTICS (Voltages Referenced to V_{SS})

Characteristic	Symbol	V_{DD} Vdc	−55°C Min	−55°C Max	25°C Min	25°C Typ	25°C Max	125°C Min	125°C Max	Unit
ıtput Voltage "0" Level V_{in} = V_{DD} or 0	V_{OL}	5.0 10 15	— — —	0.05 0.05 0.05	— — —	0 0 0	0.05 0.05 0.05	— — —	0.05 0.05 0.05	Vdc
"1" Level V_{in} = 0 or V_{DD}	V_{OH}	5.0 10 15	4.95 9.95 14.95	— — —	4.95 9.95 14.95	5.0 10 15	— — —	4.95 9.95 14.95	— — —	Vdc
ıput Voltage "0" Level (V_O = 4.5 Vdc) (V_O = 9.0 Vdc) (V_O = 13.5 Vdc)	V_{IL}	5.0 10 15	— — —	1.0 2.0 2.5	— — —	2.25 4.50 6.75	1.0 2.0 2.5	— — —	1.0 2.0 2.5	Vdc
"1" Level (V_O = 0.5 Vdc) (V_O = 1.0 Vdc) (V_O = 1.5 Vdc)	V_{IH}	5.0 10 15	4.0 9.0 12.5	— — —	4.0 8.0 12.5	2.75 5.50 8.25	— — —	4.0 8.0 12.5	— — —	Vdc
ıutput Drive Current (V_{OH} = 2.5 Vdc) Source (V_{OH} = 9.5 Vdc) (V_{OH} = 13.5 Vdc)	I_{OH}	5.0 10 15	−1.6 −1.6 −4.7	— — —	−1.25 −1.3 −3.75	−2.5 −2.6 −10	— — —	−1.0 −1.0 −3.0	— — —	mAdc
(V_{OL} = 0.4 Vdc) Sink (V_{OL} = 0.5 Vdc) (V_{OL} = 1.5 Vdc)	I_{OL}	5.0 10 15	3.75 10 30	— — —	3.2 8.0 24	6.0 16 40	— — —	2.6 6.6 19	— — —	mAdc
Input Current	I_{in}	15	—	±0.1	—	±0.00001	±0.1	—	±1.0	µAdc
Input Capacitance (V_{in} = 0)	C_{in}	--	—	—	—	10	20	—	—	pF
Quiescent Current (Per Package)	I_{DD}	5.0 10 15	— — —	1.0 2.0 4.0	— — —	0.002 0.004 0.006	1.0 2.0 4.0	— — —	30 60 120	µAdc
Total Supply Current**† (Dynamic plus Quiescent, Per Package) (C_L = 50 pF on all outputs, all buffers switching)	I_T	5.0 10 15	I_T = (1.8 µA/kHz) f + I_{DD} I_T = (3.5 µA/kHz) f + I_{DD} I_T = (5.3 µA/kHz) f + I_{DD}							µAdc

Data labelled "Typ" is not to be used for design purposes but is intended as an indication of the IC's potential performance.

* The formulas given are for the typical characteristics only at 25°C.

To calculate total supply current at loads other than 50 pF:

$$I_T(C_L) = I_T(50\ pF) + (C_L - 50)\ Vfk$$

where: I_T is in µA (per package), C_L in pF, V = (V_{DD} − V_{SS}) in volts, f in kHz is input frequency, and k = 0.002.

ITCHING CHARACTERISTICS* (C_L = 50 pF, T_A = 25°C)

Characteristic	Symbol	V_{DD} Vdc	Min	Typ #	Max	Unit
tput Rise Time	t_{TLH}					ns
t_{TLH} = (0.8 ns/pF) C_L + 60 ns		5.0	—	100	160	
t_{TLH} = (0.3 ns/pF) C_L + 35 ns		10	—	50	100	
t_{TLH} = (0.27 ns/pF) C_L + 26.5 ns		15	—	40	60	
tput Fall Time	t_{THL}					ns
t_{THL} = (0.3 ns/pF) C_L + 25 ns		5.0	—	40	60	
t_{THL} = (0.12 ns/pF) C_L + 14 ns		10	—	20	40	
t_{THL} = (0.1 ns/pF) C_L + 10 ns		15	—	15	30	
opagation Delay Time	t_{PLH}					ns
t_{PLH} = (0.38 ns/pF) C_L + 61 ns		5.0	—	80	120	
t_{PLH} = (0.20 ns/pF) C_L + 30 ns		10	—	40	65	
t_{PLH} = (0.11 ns/pF) C_L + 24.5 ns		15	—	30	50	
opagation Delay Time	t_{PHL}					ns
t_{PHL} = (0.38 ns/pF) C_L + 11 ns		5.0	—	30	60	
t_{PHL} = (0.12 ns/PF) C_L + 9 ns		10	—	15	30	
t_{PHL} = (0.11 ns/pF) C_L + 4.5 ns		15	—	10	20	

he formulas given are for the typical characteristics only at 25°C.
ata labelled "Typ" is not to be used for design purposes but is intended as an indication of the IC's potential performance.

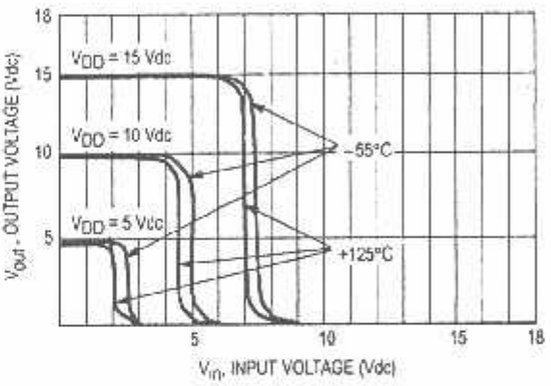


Figure 1. Typical Voltage Transfer Characteristics versus Temperature

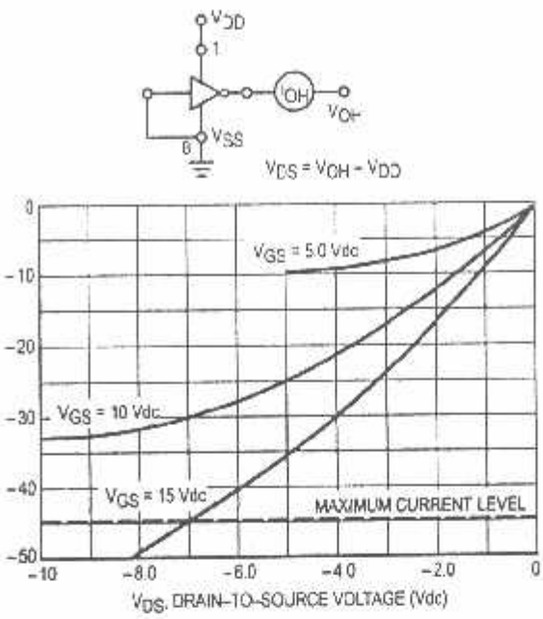


Figure 2. Typical Output Source Characteristics

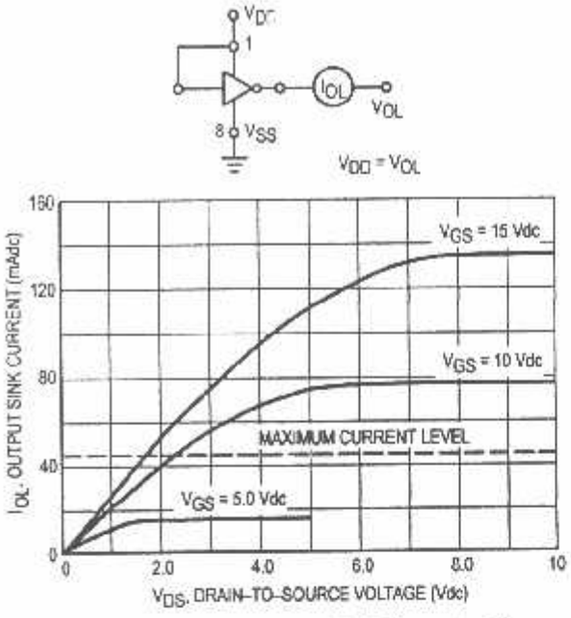


Figure 3. Typical Output Sink Characteristics

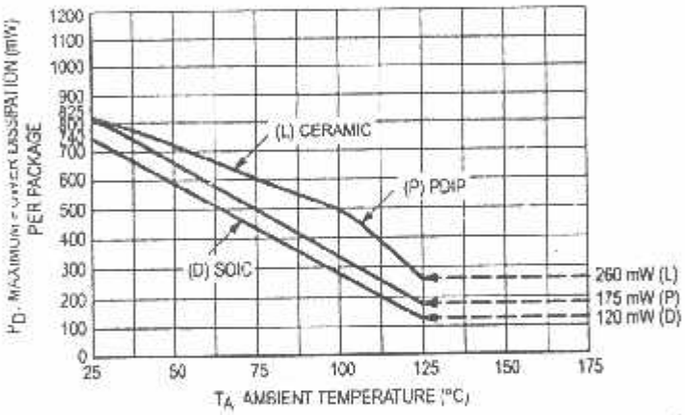


Figure 4. Ambient Temperature Power Derating

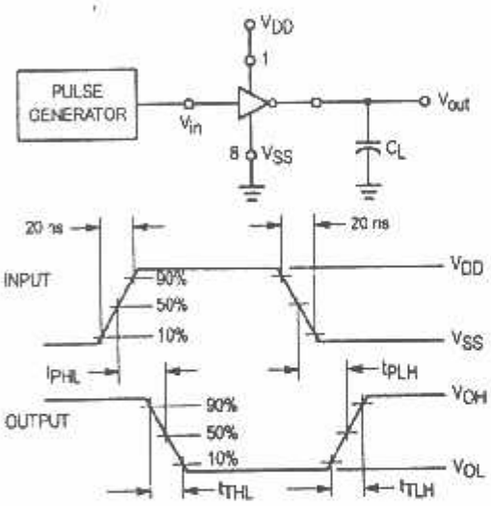
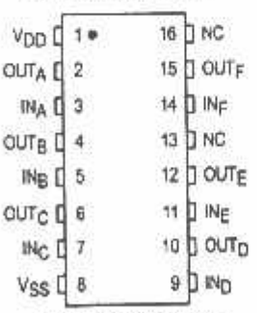


Figure 5. Switching Time Test Circuit and Waveforms

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields referenced to the V_{SS} pin, only. Extra precautions must be taken to avoid applications of any voltage higher than the maximum rated voltages to this high-impedance circuit. For proper operation, the ranges $V_{SS} \le V_{in} \le 18V$ and $V_{SS} \le V_{out} \le V_{DD}$ are recommended.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either V_{SS} or V_{DD}). Unused outputs must be left open.

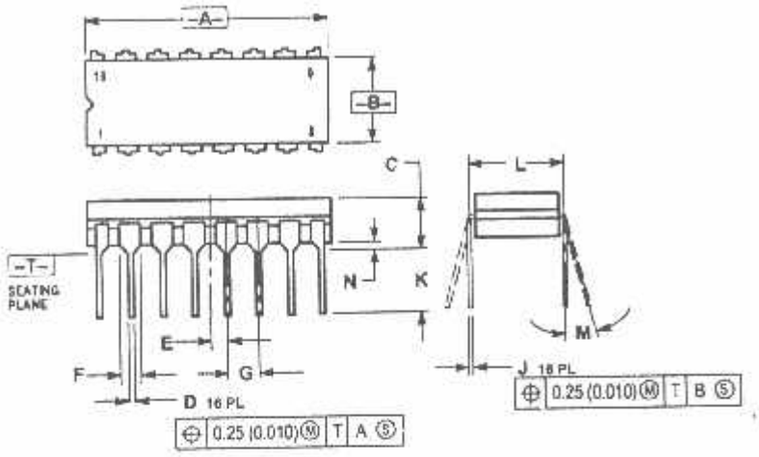
PIN ASSIGNMENT



NC = NO CONNECTION

OUTLINE DIMENSIONS

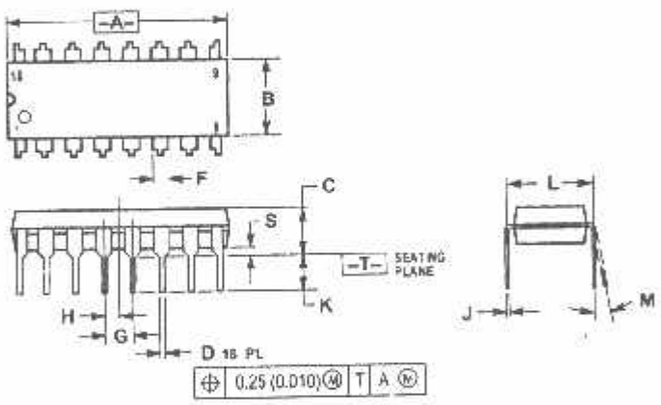
L SUFFIX
CERAMIC DIP PACKAGE
CASE 620–10
ISSUE V



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. DIMENSION L TO CENTER OF LEAD WHEN FORMED PARALLEL.
4. DIMENSION F MAY NARROW TO 0.76 (0.030) WHERE THE LEAD ENTERS THE CERAMIC BODY.

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.750	0.785	19.05	19.93
B	0.240	0.295	6.10	7.49
C	—	0.200	—	5.08
D	0.015	0.020	0.39	0.50
E	0.050 BSC		1.27 BSC	
F	0.055	0.065	1.40	1.65
G	0.100 BSC		2.54 BSC	
H	0.008	0.015	0.21	0.38
K	0.125	0.170	3.18	4.31
L	0.300 BSC		7.62 BSC	
M	0°	15°	0°	15°
N	0.020	0.040	0.51	1.01

P SUFFIX
PLASTIC DIP PACKAGE
CASE 648–08
ISSUE R

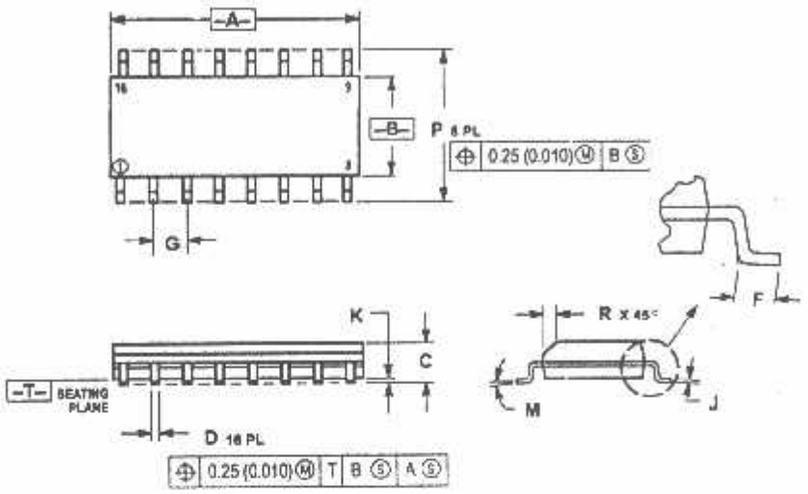


NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. DIMENSION L TO CENTER OF LEADS WHEN FORMED PARALLEL.
4. DIMENSION B DOES NOT INCLUDE MOLD FLASH.
5. ROUNDED CORNERS OPTIONAL.

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.740	0.770	18.80	19.55
B	0.250	0.270	6.35	6.85
C	0.145	0.175	3.69	4.44
D	0.015	0.021	0.39	0.53
F	0.040	0.70	1.02	1.77
G	0.100 BSC		2.54 BSC	
H	0.05 BSC		1.27 BSC	
J	0.008	0.015	0.21	0.38
K	0.110	0.130	2.80	3.30
L	0.295	0.305	7.50	7.74
M	0°	10°	0°	10°
S	0.020	0.040	0.51	1.01

OUTLINE DIMENSIONS

D SUFFIX
PLASTIC SOIC PACKAGE
CASE 751B–05
ISSUE J



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSIONS A AND B DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
5. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127 (0.005) TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	9.80	10.00	0.386	0.393
B	3.80	4.00	0.150	0.157
C	1.35	1.75	0.054	0.068
D	0.35	0.49	0.014	0.019
F	0.40	1.25	0.016	0.049
G	1.27 BSC		0.050 BSC	
J	0.19	0.25	0.008	0.009
K	0.10	0.25	0.004	0.009
M	0°	7°	0°	7°
P	5.80	6.20	0.229	0.244
R	0.25	0.50	0.010	0.019

How to reach us:
USA/EUROPE/Locations Not Listed: Motorola Literature Distribution; P.O. Box 20912; Phoenix, Arizona 85036. 1–800–441–2447 or 602–303–5454

MFAX: RMFAX0@email.sps.mot.com – TOUCHTONE 602–244–6609
INTERNET: http://Design–NET.com

JAPAN: Nippon Motorola Ltd.; Tatsumi–SPD–JLDC, 6F Seibu–Butsuryu–Center, 3–14–2 Tatsumi Koto–Ku, Tokyo 135, Japan. 03–81–3521–8315

ASIA/PACIFIC: Motorola Semiconductors H.K. Ltd.; 8B Tai Ping Industrial Park, 51 Ting Kok Road, Tai Po, N.T., Hong Kong. 852–26629298

MOTOROLA ◊

August 2000

National Semiconductor

LM741
Operational Amplifier

General Description

The LM741 series are general purpose operational amplifiers which feature improved performance over industry standards like the LM709. They are direct, plug-in replacements for the 709C, LM201, MC1439 and 748 in most applications.

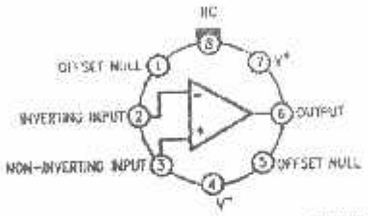
The amplifiers offer many features which make their application nearly foolproof: overload protection on the input and output, no latch-up when the common mode range is exceeded, as well as freedom from oscillations.

The LM741C is identical to the LM741/LM741A except that the LM741C has their performance guaranteed over a 0°C to +70°C temperature range, instead of −55°C to +125°C.

Features

Connection Diagrams

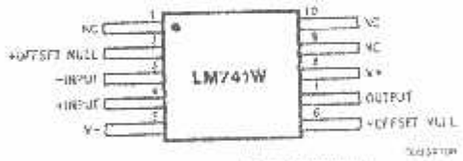
Metal Can Package



Note 1: LM741H is available per JM38510/10101

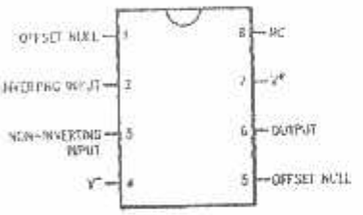
Order Number LM741H, LM741H/883 (Note 1), LM741AH/883 or LM741CH
See NS Package Number H08C

Ceramic Flatpak



Order Number LM741W/883
See NS Package Number W10A

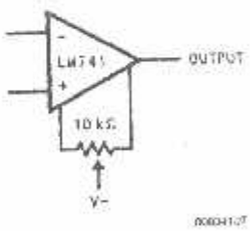
Dual-In-Line or S.O. Package



Order Number LM741J, LM741J/883, LM741CN
See NS Package Number J08A, M08A or NC8E

Typical Application

Offset Nulling Circuit



Absolute Maximum Ratings (Note 2)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

(Note 7)

	LM741A	LM741	LM741C
Supply Voltage	±22V	±22V	±18V
Power Dissipation (Note 3)	500 mW	500 mW	500 mW
Differential Input Voltage	±30V	±30V	±30V
Input Voltage (Note 4)	±15V	±15V	±15V
Output Short Circuit Duration	Continuous	Continuous	Continuous
Operating Temperature Range	−55°C to +125°C	−55°C to +125°C	0°C to +70°C
Storage Temperature Range	−65°C to +150°C	−65°C to +150°C	−65°C to +150°C
Junction Temperature	150°C	150°C	100°C
Soldering Information			
N-Package (10 seconds)	260°C	260°C	260°C
J- or H-Package (10 seconds)	300°C	300°C	300°C
M-Package			
Vapor Phase (60 seconds)	215°C	215°C	215°C
Infrared (15 seconds)	215°C	215°C	215°C
See AN-450 "Surface Mounting Methods and Their Effect on Product Reliability" for other methods of soldering surface mount devices.			
ESD Tolerance (Note 8)	400V	400V	400V

Electrical Characteristics (Note 5)

Parameter	Conditions	LM741A			LM741			LM741C			Units
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
Input Offset Voltage	$T_A = 25°C$ $R_S \le 10\ k\Omega$ $R_S \le 50\Omega$		0.8	3.0		1.0	5.0		2.0	6.0	mV mV
	$T_{AMIN} \le T_A \le T_{AMAX}$ $R_S \le 50\Omega$ $R_S \le 10\ k\Omega$			4.0			6.0			7.5	mV mV
Average Input Offset Voltage Drift				15							µV/°C
Input Offset Voltage Adjustment Range	$T_A = 25°C$, $V_S = \pm 20V$	±10				±15			±15		mV
Input Offset Current	$T_A = 25°C$		3.0	30		20	200		20	200	nA
	$T_{AMIN} \le T_A \le T_{AMAX}$			70		85	500			300	nA
Average Input Offset Current Drift				0.5							nA/°C
Input Bias Current	$T_A = 25°C$		30	80		80	500		80	500	nA
	$T_{AMIN} \le T_A \le T_{AMAX}$			0.210			1.5			0.8	µA
Input Resistance	$T_A = 25°C$, $V_S = \pm 20V$	1.0	6.0		0.3	2.0		0.3	2.0		MΩ
	$T_{AMIN} \le T_A \le T_{AMAX}$, $V_S = \pm 20V$	0.5									MΩ
Input Voltage Range	$T_A = 25°C$							±12	±13		V
	$T_{AMIN} \le T_A \le T_{AMAX}$				±12	±13					V

Electrical Characteristics (Note 5) (Continued)

Parameter	Conditions	LM741A			LM741			LM741C			Units
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
ge Signal Voltage Gain	T_A = 25°C, $R_L \geq 2$ kΩ										
	V_S = ±20V, V_O = ±15V	50									V/mV
	V_S = ±15V, V_O = ±10V				50	200		20	200		V/mV
	$T_{AMIN} \leq T_A \leq T_{AMAX}$, $R_L \geq 2$ kΩ,										
	V_S = ±20V, V_O = ±15V	32									V/mV
	V_S = ±15V, V_O = ±10V				25			15			V/mV
	V_S = ±5V, V_O = ±2V	10									V/mV
utput Voltage Swing	V_S = ±20V										
	$R_L \geq 10$ kΩ	±16									V
	$R_L \geq 2$ kΩ	±15									V
	V_S = ±15V										
	$R_L \geq 10$ kΩ				±12	±14		±12	±14		V
	$R_L \geq 2$ kΩ				±10	±13		±10	±13		V
Output Short Circuit	T_A = 25°C	10	25	35		25			25		mA
Current	$T_{AMIN} \leq T_A \leq T_{AMAX}$	10		40							mA
Common-Mode	$T_{AMIN} \leq T_A \leq T_{AMAX}$										
Rejection Ratio	$R_S \leq 10$ kΩ, V_{CM} = ±12V				70	90		70	90		dB
	$R_S \leq 50$Ω, V_{CM} = ±12V	80	95								dB
Supply Voltage Rejection	$T_{AMIN} \leq T_A \leq T_{AMAX}$,										
Ratio	V_S = ±20V to V_S = ±5V										
	$R_S \leq 50$Ω	86	96								dB
	$R_S \leq 10$ kΩ				77	96		77	96		dB
Transient Response	T_A = 25°C, Unity Gain										
Rise Time			0.25	0.8		0.3			0.3		µs
Overshoot			6.0	20		5			5		%
Bandwidth (Note 6)	T_A = 25°C	0.437	1.5								MHz
Slew Rate	T_A = 25°C, Unity Gain	0.3	0.7			0.5			0.5		V/µs
Supply Current	T_A = 25°C					1.7	2.8		1.7	2.8	mA
Power Consumption	T_A = 25°C										
	V_S = ±20V		80	150							mW
	V_S = ±15V					50	85		50	85	mW
LM741A	V_S = ±20V										
	$T_A = T_{AMIN}$			165							mW
	$T_A = T_{AMAX}$			135							mW
LM741	V_S = ±15V										
	$T_A = T_{AMIN}$					60	100				mW
	$T_A = T_{AMAX}$					45	75				mW

Note 2: "Absolute Maximum Ratings" indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is functional, but do not guarantee specific performance limits.

Electrical Characteristics (Note 5) (Continued)

Note 3: For operation at elevated temperatures, these devices must be derated based on thermal resistance, and T_j max. (listed under "Absolute Maximum Ratings"). $T_j = T_A + (\theta_{jA} P_D)$.

Thermal Resistance	Cerdip (J)	DIP (N)	HO8 (H)	SO-8 (M)
θ_{jA} (Junction to Ambient)	100°C/W	100°C/W	170°C/W	195°C/W
θ_{jC} (Junction to Case)	N/A	N/A	25°C/W	N/A

Note 4: For supply voltages less than ±15V, the absolute maximum input voltage is equal to the supply voltage.

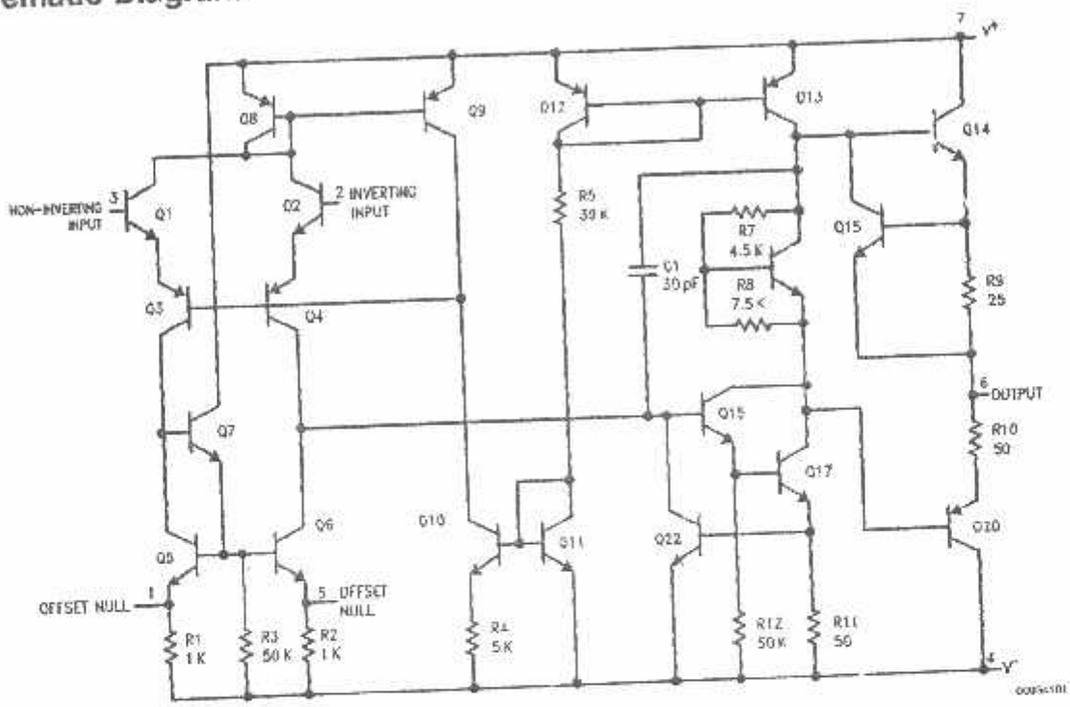
Note 5: Unless otherwise specified, these specifications apply for V_S = ±15V, −55°C ≤ T_A ≤ +125°C (LM741/LM741A). For the LM741C/LM741E, these specifications are limited to 0°C ≤ T_A ≤ +70°C.

Note 6: Calculated value from: BW (MHz) = 0.35/Rise Time(μs).

Note 7: For military specifications see RETS741X for LM741 and RETS741AX for LM741A.

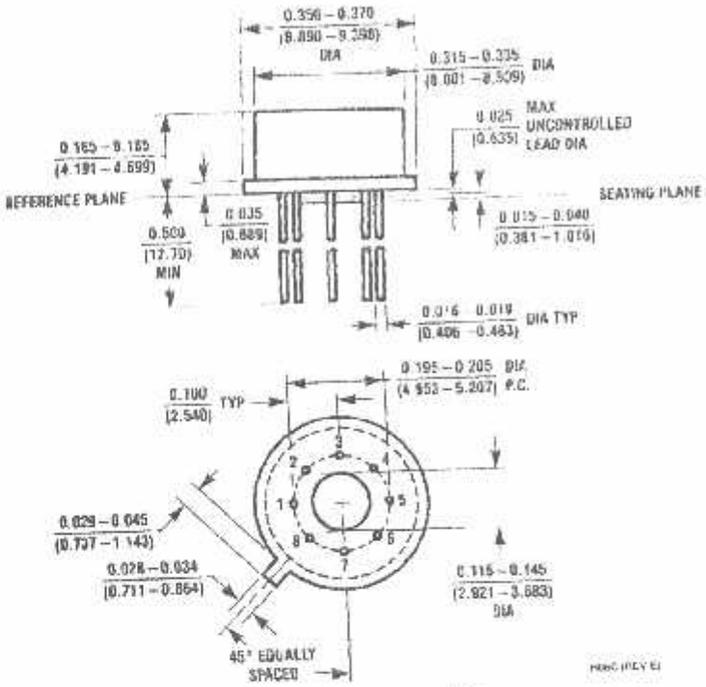
Note 8: Human body model, 1.5 kΩ in series with 100 pF.

Schematic Diagram



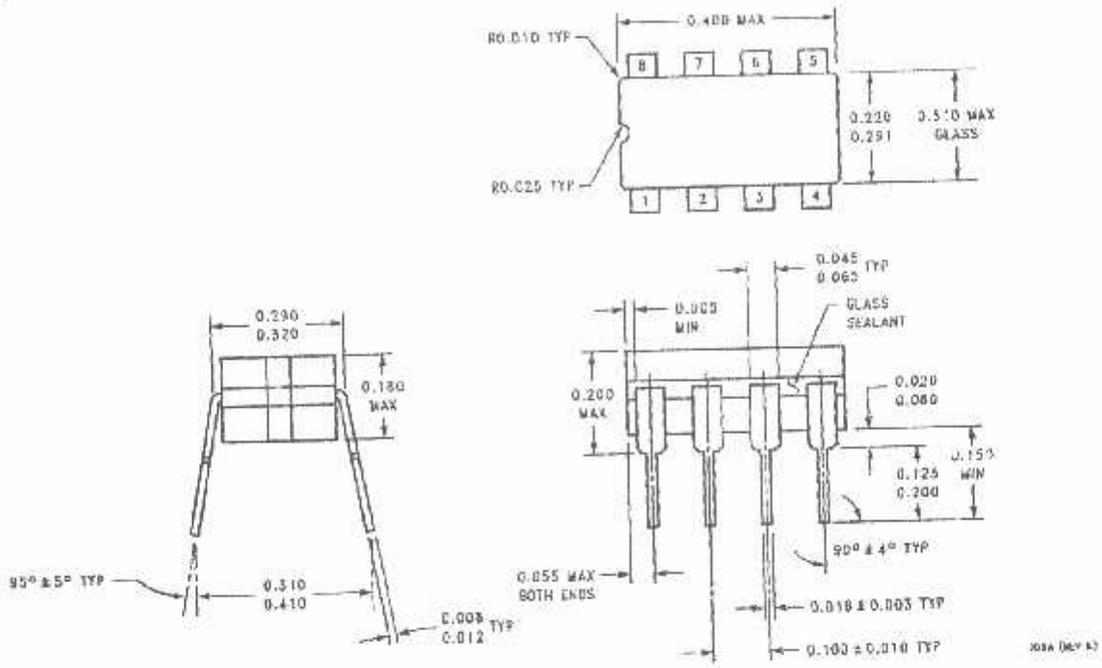
Physical Dimensions inches (millimeters)

unless otherwise noted

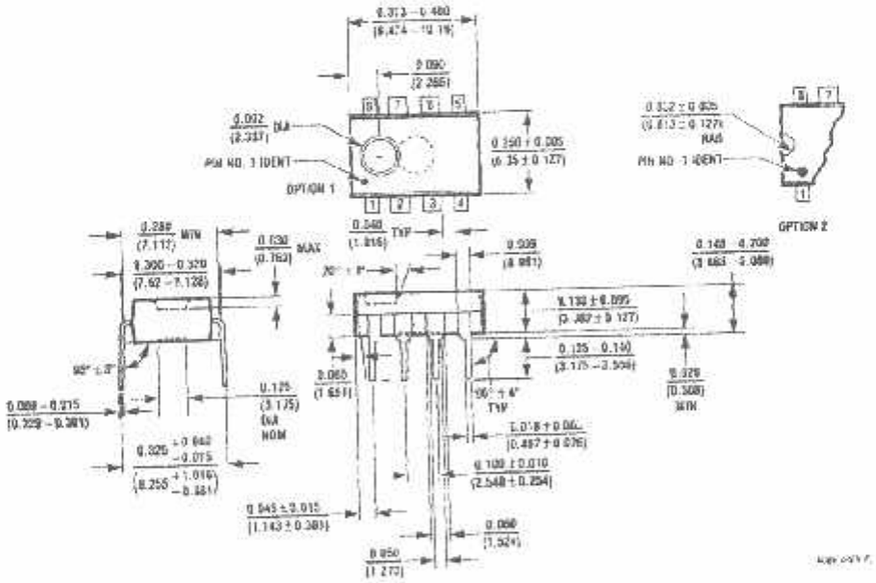


Metal Can Package (H)
Order Number LM741H, LM741H/883, LM741AH/883, LM741AH-MIL or LM741CH
NS Package Number H08C

Physical Dimensions inches (millimeters) unless otherwise noted (Continued)

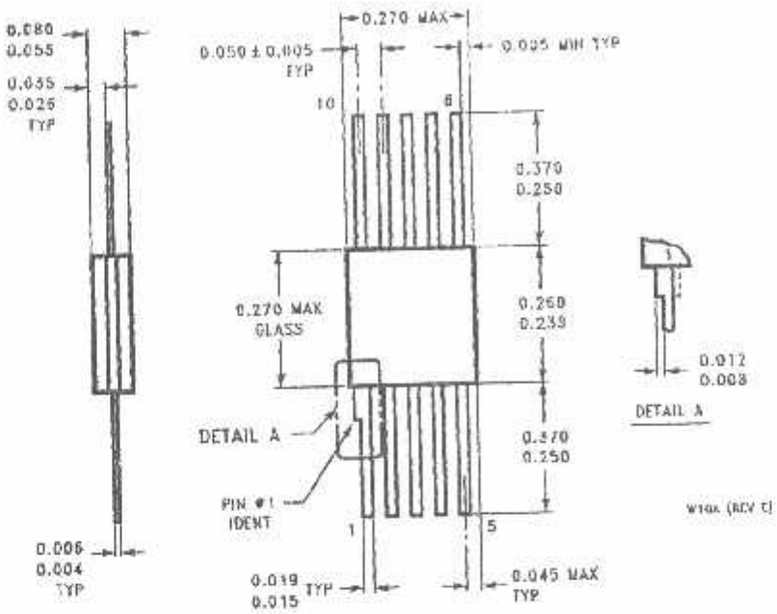


Ceramic Dual-In-Line Package (J)
Order Number LM741J/883
NS Package Number J08A



Dual-In-Line Package (N)
Order Number LM741CN
NS Package Number N08E

Physical Dimensions inches (millimeters) unless otherwise noted (Continued)



10-Lead Ceramic Flatpak (W)
Order Number LM741W/883, LM741WG-MPR or LM741W/G/883
NS Package Number W10A

TITUT TEKNOLOGI NASIONAL
Jl. Bendungan Sigura-gura No. 2
MALANG

FORMULIR BIMBINGAN SKRIPSI

ma : ISNAINI ROZAFI
M : 01.17.044
sa Bimbingan : 10 Februari 2007 s/d 10 Agustus 2007
ul Skripsi : Perencanaan dan Pembuatan Master Kontrol Lab. Bahasa 8 Channel Berbasis Mikrokontroller AT89S8252

	Tanggal	Uraian	Paraf Pembimbing
	10-2-07	Bab I & II	
	10-2-07	Revisi Bab II	
	18-02-07	Revisi Bab II	
	21-02-07	Bab III & IV	
	25-02-07	Revisi Bab IV	
	28-02-07	Revisi Bab V	
	8-3-07	Acc seminar hasil	
	12-3-2007	Acc lompre	

Malang, 12-3-2007
Dosen Pembimbing

Joseph Dedy Irawan, ST., MT.
NIP. 132315178

Form S-4

e 9. T2MOD – Timer 2 Mode Control Register

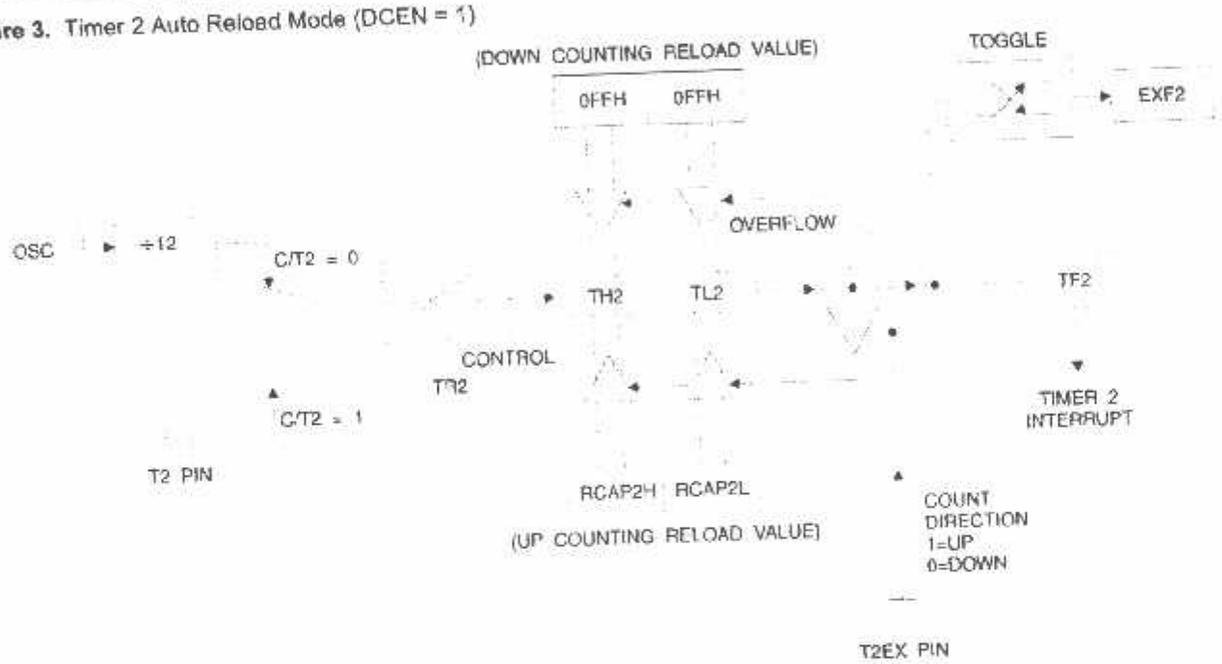
MOD Address = 0C9H — Reset Value = XXXX XX00B

Bit Addressable

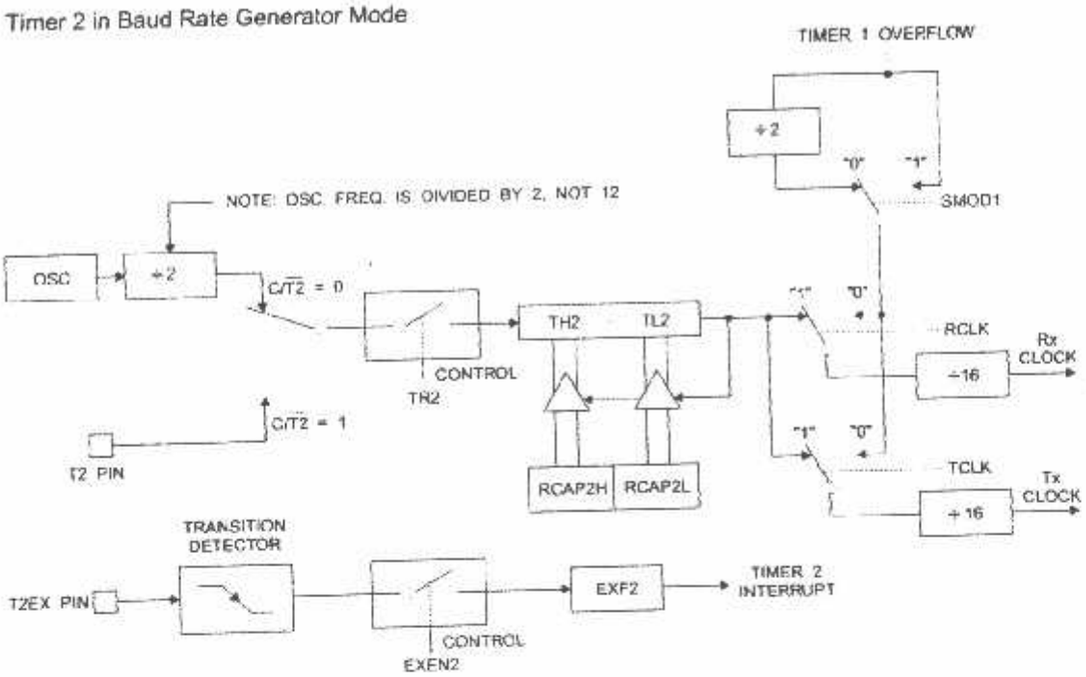
–	–	–	–	–	–	T2OE	DCEN
7	6	5	4	3	2	1	0

mbol	Function
	Not implemented, reserved for future use.
OE	Timer 2 Output Enable bit.
EN	When set, this bit allows Timer 2 to be configured as an up/down counter.

ıre 3. Timer 2 Auto Reload Mode (DCEN = 1)



ıre 4. Timer 2 in Baud Rate Generator Mode



ud Rate Generator

Timer 2 is selected as the baud rate generator by setting TCLK and/or RCLK in T2CON (Table 2). Note that the baud rates for transmit and receive can be different if Timer 2 is used for the receiver or transmitter and Timer 1 is used for the other function. Setting RCLK and/or TCLK puts Timer 2 into its baud rate generator mode, as shown in Figure 4.

The baud rate generator mode is similar to the auto-reload mode, in that a rollover in TH2 causes the Timer 2 registers to be reloaded with the 16-bit value in registers RCAP2H and RCAP2L, which are preset by software.

The baud rates in Modes 1 and 3 are determined by Timer 2's overflow rate according to the following equation.

$$\text{Modes 1 and 3 Baud Rates} = \frac{\text{Timer 2 Overflow Rate}}{16}$$

The Timer can be configured for either timer or counter operation. In most applications, it is configured for timer operation ($CP/\overline{T2} = 0$). The timer operation is different for Timer 2 when it is used as a baud rate generator. Normally, as a timer, it increments every machine cycle (at 1/12 the oscillator frequency). As a baud rate generator, however, it increments every state time (at 1/2 the oscillator frequency). The baud rate formula is given below.

$$\frac{\text{Modes 1 and 3}}{\text{Baud Rate}} = \frac{\text{Oscillator Frequency}}{32 \times [65536 - (\text{RCAP2H,RCAP2L})]}$$

where (RCAP2H, RCAP2L) is the content of RCAP2H and RCAP2L taken as a 16-bit unsigned integer.

Timer 2 as a baud rate generator is shown in Figure 4. This figure is valid only if RCLK or TCLK = 1 in T2CON. Note that a rollover in TH2 does not set TF2 and will not generate an interrupt. Note too, that if EXEN2 is set, a 1-to-0 transition in T2EX will set EXF2 but will not cause a reload from (RCAP2H, RCAP2L) to (TH2, TL2). Thus when Timer 2 is in use as a baud rate generator, T2EX can be used as an extra external interrupt.

Note that when Timer 2 is running (TR2 = 1) as a timer in the baud rate generator mode, TH2 or TL2 should not be read from or written to. Under these conditions, the Timer is incremented every state time, and the results of a read or write may not be accurate. The RCAP2 registers may be read but should not be written to, because a write might overlap a reload and cause write and/or reload errors. The timer should be turned off (clear TR2) before accessing the Timer 2 or RCAP2 registers.

·ogrammable ·ock Out

A 50% duty cycle clock can be programmed to come out on P1.0, as shown in Figure 5. This pin, besides being a regular I/O pin, has two alternate functions. It can be programmed to input the external clock for Timer/Counter 2 or to output a 50% duty cycle clock ranging from 61 Hz to 4 MHz (for a 16-MHz operating frequency).

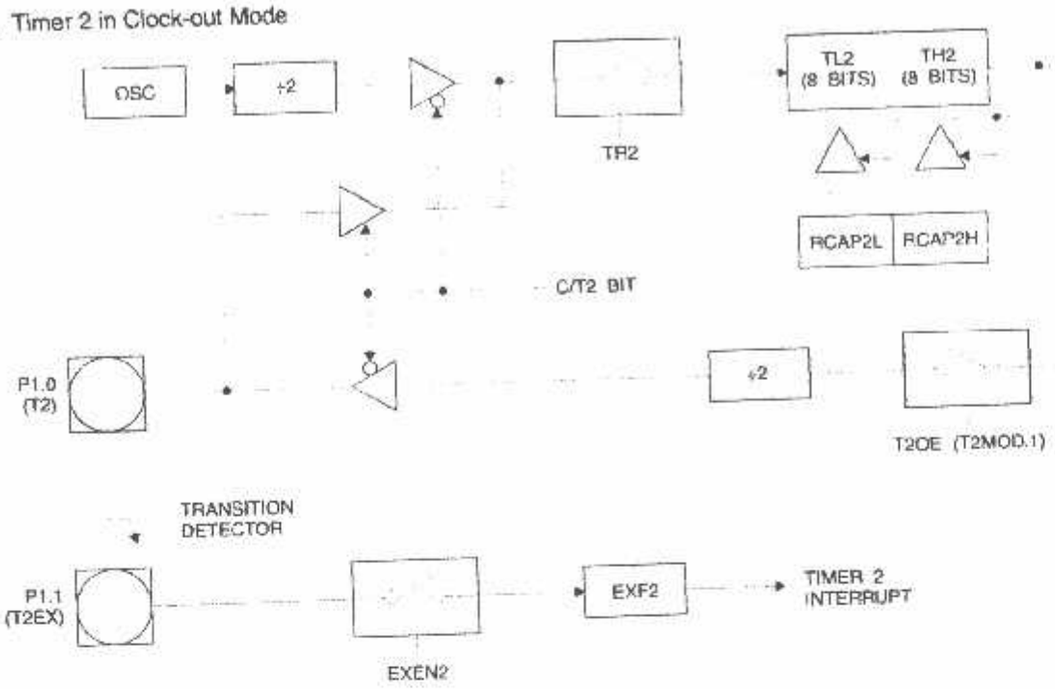
To configure the Timer/Counter 2 as a clock generator, bit C/$\overline{T2}$ (T2CON.1) must be cleared and bit T2OE (T2MOD.1) must be set. Bit TR2 (T2CON.2) starts and stops the timer.

The clock-out frequency depends on the oscillator frequency and the reload value of Timer 2 capture registers (RCAP2H, RCAP2L), as shown in the following equation.

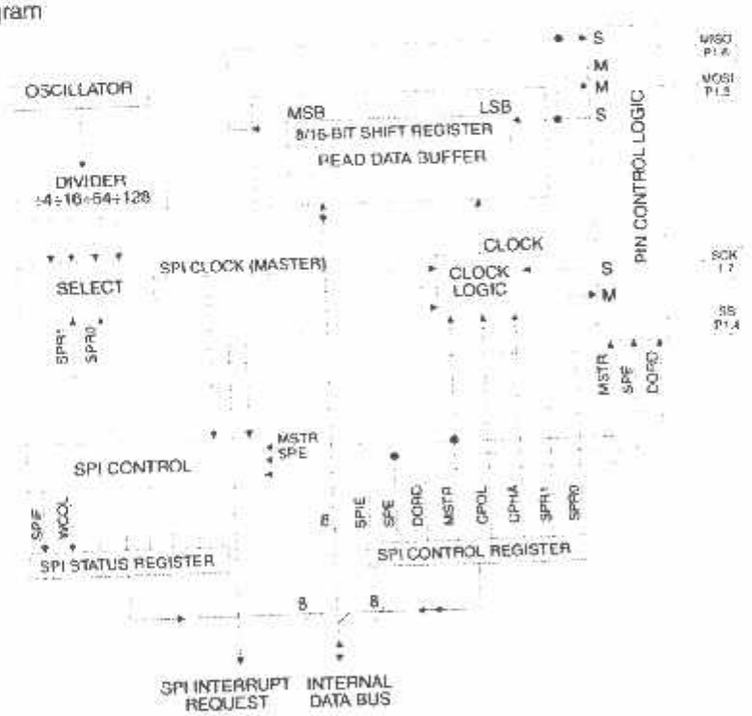
$$\text{Clock Out Frequency} = \frac{\text{Oscillator Frequency}}{4 \times [65536 - (\text{RCAP2H,RCAP2L})]}$$

In the clock-out mode, Timer 2 rollovers will not generate an interrupt. This behavior is similar to when Timer 2 is used as a baud-rate generator. It is possible to use Timer 2 as a baud-rate generator and a clock generator simultaneously. Note, however, that the baud-rate and clock-out frequencies cannot be determined independently from one another since they both use RCAP2H and RCAP2L.

re 5. Timer 2 in Clock-out Mode



igure 6. SPI Block Diagram



.RT

The UART in the AT89S8252 operates the same way as the UART in the AT89C51 and AT89C52. For further information on the UART operation, refer to the Atmel web site (http://www.atmel.com). From the home page, select "Products", then "Microcontrollers, then "8051-Architecture". Click on "Documentation", then on "Other Documents". Open the document "AT89 Series Hardware Description".

ɛrial Peripheral terface

The serial peripheral interface (SPI) allows high-speed synchronous data transfer between the AT89S8252 and peripheral devices or between several AT89S8252 devices. The AT89S8252 SPI features include the following:

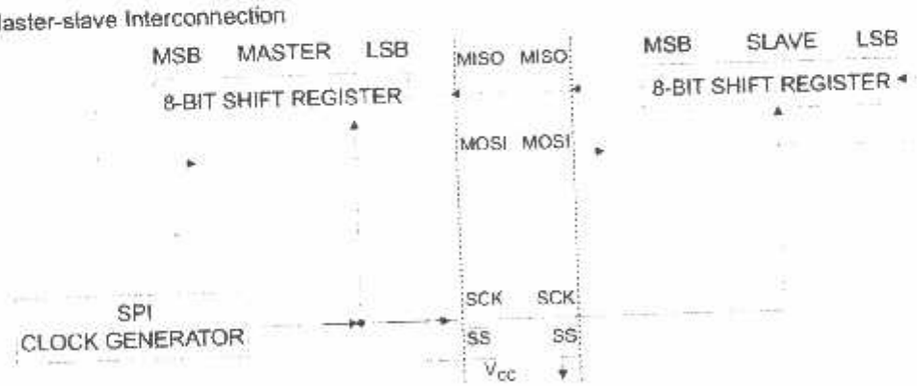
- Full-Duplex, 3-Wire Synchronous Data Transfer
- Master or Slave Operation
- 1.5 MHz Bit Frequency (max.)
- LSB First or MSB First Data Transfer
- Four Programmable Bit Rates
- End of Transmission Interrupt Flag
- Write Collision Flag Protection
- Wakeup from Idle Mode (Slave Mode Only)

The interconnection between master and slave CPUs with SPI is shown in the following figure. The SCK pin is the clock output in the master mode but is the clock input in the slave mode. Writing to the SPI data register of the master CPU starts the SPI clock generator, and the data written shifts out of the MOSI pin and into the MOSI pin of the slave CPU. After shifting one byte, the SPI clock generator stops, setting the end of transmission flag (SPIF). If both the SPI interrupt enable bit (SPIE) and the serial port interrupt enable bit (ES) are set, an interrupt is requested.

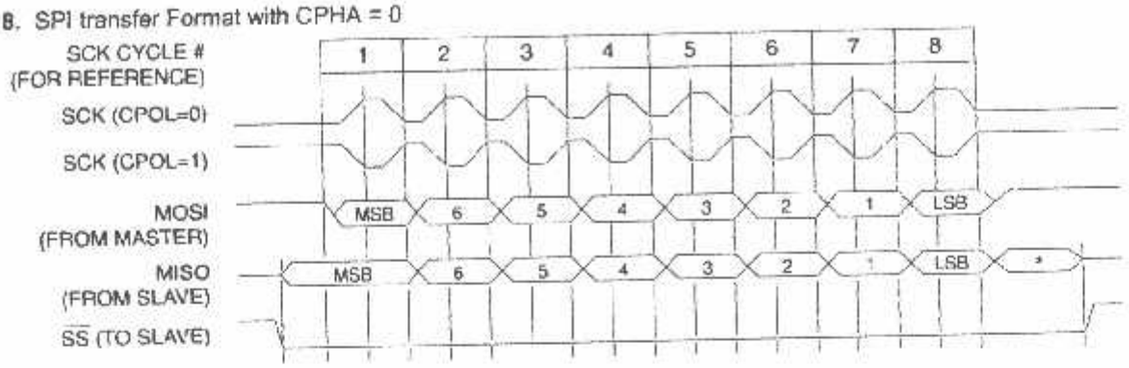
The Slave Select input, $\overline{SS}$/P1.4, is set low to select an individual SPI device as a slave. When $\overline{SS}$/P1.4 is set high, the SPI port is deactivated and the MOSI/P1.5 pin can be used as an input.

There are four combinations of SCK phase and polarity with respect to serial data, which are determined by control bits CPHA and CPOL. The SPI data transfer formats are shown in Figure 8 and Figure 9.

igure 7. SPI Master-slave Interconnection

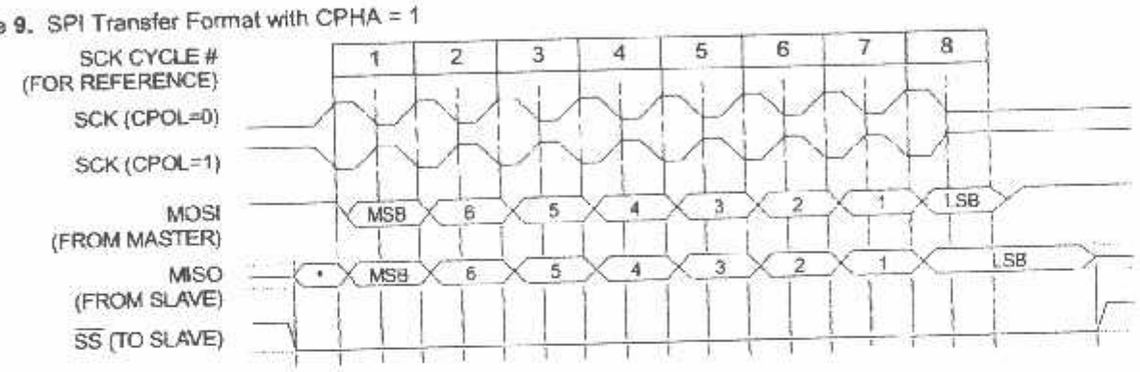


ıre 8. SPI transfer Format with CPHA = 0



ıe: *Not defined but normally MSB of character just received

ıure 9. SPI Transfer Format with CPHA = 1



Note: *Not defined but normally LSB of previously transmitted character.

nterrupts

The AT89S8252 has a total of six interrupt vectors: two external interrupts ($\overline{INT0}$ and $\overline{INT1}$), three timer interrupts (Timers 0, 1, and 2), and the serial port interrupt. These interrupts are all shown in Figure 10.

Each of these interrupt sources can be individually enabled or disabled by setting or clearing a bit in Special Function Register IE. IE also contains a global disable bit, EA, which disables all interrupts at once.

Note that Table 10 shows that bit position IE.6 is unimplemented. In the AT89C51, bit position IE.5 is also unimplemented. User software should not write 1s to these bit positions, since they may be used in future AT89 products.

Timer 2 interrupt is generated by the logical OR of bits TF2 and EXF2 in register T2CON. Neither of these flags is cleared by hardware when the service routine is vectored to. In fact, the service routine may have to determine whether it was TF2 or EXF2 that generated the interrupt, and that bit will have to be cleared in software.

The Timer 0 and Timer 1 flags, TF0 and TF1, are set at S5P2 of the cycle in which the timers overflow. The values are then polled by the circuitry in the next cycle. However, the Timer 2 flag, TF2, is set at S2P2 and is polled in the same cycle in which the timer overflows.

e 10. Interrupt Enable (IE) Register

(SB)(LSB)

EA	–	ET2	ES	ET1	EX1	ET0	EX0

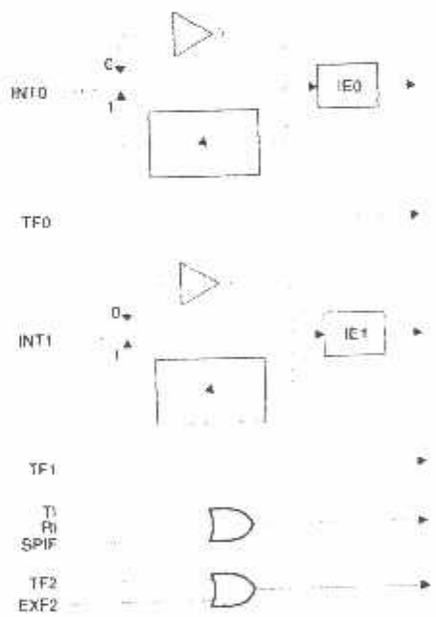
Enable Bit = 1 enables the interrupt.

Enable Bit = 0 disables the interrupt.

Symbol	Position	Function
EA	IE.7	Disables all interrupts. If EA = 0, no interrupt is acknowledged. If EA = 1, each interrupt source is individually enabled or disabled by setting or clearing its enable bit.
–	IE.6	Reserved.
ET2	IE.5	Timer 2 interrupt enable bit.
ES	IE.4	SPI and UART interrupt enable bit.
ET1	IE.3	Timer 1 interrupt enable bit.
EX1	IE.2	External interrupt 1 enable bit.
ET0	IE.1	Timer 0 interrupt enable bit.
EX0	IE.0	External interrupt 0 enable bit.

User software should never write 1s to unimplemented bits, because they may be used in future AT89 products.

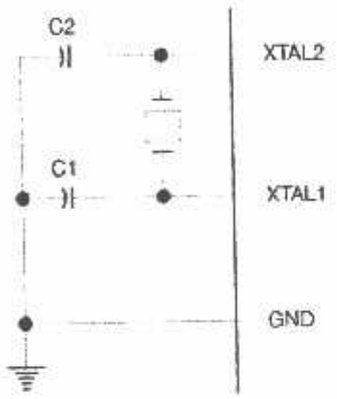
=igure 10. Interrupt Sources



cillator
ıaracteristics

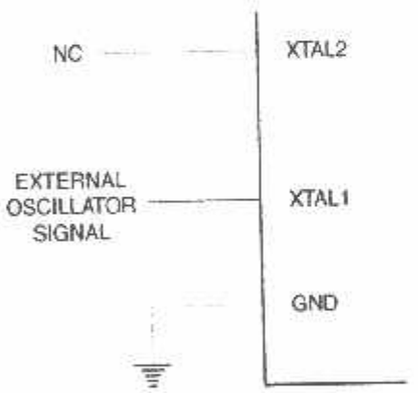
XTAL1 and XTAL2 are the input and output, respectively, of an inverting amplifier that can be configured for use as an on-chip oscillator, as shown in Figure 11. Either a quartz crystal or ceramic resonator may be used. To drive the device from an external clock source, XTAL2 should be left unconnected while XTAL1 is driven, as shown in Figure 12. There are no requirements on the duty cycle of the external clock signal, since the input to the internal clocking circuitry is through a divide-by-two flip-flop, but minimum and maximum voltage high and low time specifications must be observed.

Figure 11. Oscillator Connections



Note: C1, C2 = 30 pF ± 10 pF for Crystals
= 40 pF ± 10 pF for Ceramic Resonators

Figure 12. External Clock Drive Configuration



: Mode

In idle mode, the CPU puts itself to sleep while all the on-chip peripherals remain active. The mode is invoked by software. The content of the on-chip RAM and all the special functions registers remain unchanged during this mode. The idle mode can be terminated by any enabled interrupt or by a hardware reset.

Note that when idle mode is terminated by a hardware reset, the device normally resumes program execution from where it left off, up to two machine cycles before the internal reset algorithm takes control. On-chip hardware inhibits access to internal RAM in this event, but access to the port pins is not inhibited. To eliminate the possibility of an unexpected write to a port pin when idle mode is terminated by a reset, the instruction following the one that invokes idle mode should not write to a port pin or to external memory.

Status of External Pins During Idle and Power-down Modes

Mode	Program Memory	ALE	$\overline{PSEN}$	PORT0	PORT1	PORT2	PORT3
Idle	Internal	1	1	Data	Data	Data	Data
Idle	External	1	1	Float	Data	Address	Data
Power-down	Internal	0	0	Data	Data	Data	Data
Power-down	External	0	0	Float	Data	Data	Data

Power-down Mode

In the power-down mode, the oscillator is stopped and the instruction that invokes power-down is the last instruction executed. The on-chip RAM and Special Function Registers retain their values until the power-down mode is terminated. Exit from power-down can be initiated either by a hardware reset or by an enabled external interrupt. Reset redefines the SFRs but does not change the on-chip RAM. The reset should not be activated before V_{CC} is restored to its normal operating level and must be held active long enough to allow the oscillator to restart and stabilize.

To exit power-down via an interrupt, the external interrupt must be enabled as level sensitive before entering power-down. The interrupt service routine starts at 16 ms (nominal) after the enabled interrupt pin is activated.

Program Memory Lock Bits

The AT89S8252 has three lock bits that can be left unprogrammed (U) or can be programmed (P) to obtain the additional features listed in the following table.

When lock bit 1 is programmed, the logic level at the $\overline{EA}$ pin is sampled and latched during reset. If the device is powered up without a reset, the latch initializes to a random value and holds that value until reset is activated. The latched value of $\overline{EA}$ must agree with the current logic level at that pin in order for the device to function properly.

Once programmed, the lock bits can only be unprogrammed with the Chip Erase operations in either the parallel or serial modes.

.ock Bit Protection Modes[1][2]

	Program Lock Bits			
	LB1	LB2	LB3	Protection Type
1	U	U	U	No internal memory lock feature.
2	P	U	U	MOVC instructions executed from external program memory are disabled from fetching code bytes from internal memory. $\overline{EA}$ is sampled and latched on reset and further programming of the Flash memory (parallel or serial mode) is disabled.
3	P	P	U	Same as Mode 2, but parallel or serial verify are also disabled.
4	P	P	P	Same as Mode 3, but external execution is also disabled.

otes: 1. U = Unprogrammed
2. P = Programmed

›gramming the ash and EEPROM

Atmel's AT89S8252 Flash Microcontroller offers 8K bytes of in-system reprogrammable Flash Code memory and 2K bytes of EEPROM Data memory.

The AT89S8252 is normally shipped with the on-chip Flash Code and EEPROM Data memory arrays in the erased state (i.e. contents = FFH) and ready to be programmed. This device supports a High-voltage (12-V V_{PP}) Parallel programming mode and a Low-voltage (5-V V_{CC}) Serial programming mode. The serial programming mode provides a convenient way to reprogram the AT89S8252 inside the user's system. The parallel programming mode is compatible with conventional third party Flash or EPROM programmers.

The Code and Data memory arrays are mapped via separate address spaces in the serial programming mode. In the parallel programming mode, the two arrays occupy one contiguous address space: 0000H to 1FFFH for the Code array and 2000H to 27FFH for the Data array.

The Code and Data memory arrays on the AT89S8252 are programmed byte-by-byte in either programming mode. An auto-erase cycle is provided with the self-timed programming operation in the serial programming mode. There is no need to perform the Chip Erase operation to reprogram any memory location in the serial programming mode unless any of the lock bits have been programmed.

In the parallel programming mode, there is no auto-erase cycle. To reprogram any non-blank byte, the user needs to use the Chip Erase operation first to erase both arrays.

Parallel Programming Algorithm: To program and verify the AT89S8252 in the parallel programming mode, the following sequence is recommended:

1. Power-up sequence:
   Apply power between V_{CC} and GND pins.
   Set RST pin to "H".
   Apply a 3 MHz to 24 MHz clock to XTAL1 pin and wait for at least 10 milliseconds.
2. Set $\overline{PSEN}$ pin to "L"
   ALE pin to "H"
   $\overline{EA}$ pin to "H" and all other pins to "H".
3. Apply the appropriate combination of "H" or "L" logic levels to pins P2.6, P2.7, P3.6, P3.7 to select one of the programming operations shown in the Flash Programming Modes table.
4. Apply the desired byte address to pins P1.0 to P1.7 and P2.0 to P2.5.
   Apply data to pins P0.0 to P0.7 for Write Code operation.
5. Raise $\overline{EA}/V_{pp}$ to 12V to enable Flash programming, erase or verification.
6. Pulse ALE/$\overline{PROG}$ once to program a byte in the Code memory array, the Data memory array or the lock bits. The byte-write cycle is self-timed and typically takes 1.5 ms.
7. To verify the byte just programmed, bring pin P2.7 to "L" and read the programmed data at pins P0.0 to P0.7.
8. Repeat steps 3 through 7 changing the address and data for the entire 2K or 8K bytes array or until the end of the object file is reached.
9. Power-off sequence:
   Set XTAL1 to "L".
   Set RST and $\overline{EA}$ pins to "L".
   Turn V_{CC} power off.

In the parallel programming mode, there is no auto-erase cycle and to reprogram any non-blank byte, the user needs to use the Chip Erase operation first to erase both arrays.

Data Polling: The AT89S8252 features DATA Polling to indicate the end of a byte write cycle. During a byte write cycle in the parallel or serial programming mode, an attempted read of the last byte written will result in the complement of the written datum on P0.7 (parallel mode), and on the MSB of the serial output byte on MISO (serial mode). Once the write cycle has been completed, true data are valid on all outputs, and the next cycle may begin. DATA Polling may begin any time after a write cycle has been initiated.

Ready/Busy: The progress of byte programming in the parallel programming mode can also be monitored by the RDY/BSY output signal. Pin P3.4 is pulled Low after ALE goes High during programming to indicate BUSY. P3.4 is pulled High again when programming is done to indicate READY.

Program Verify: If lock bits LB1 and LB2 have not been programmed, the programmed Code or Data byte can be read back via the address and data lines for verification. The state of the lock bits can also be verified directly in the parallel programming mode. In the serial programming mode, the state of the lock bits can only be verified indirectly by observing that the lock bit features are enabled.

Chip Erase: Both Flash and EEPROM arrays are erased electrically at the same time. In the parallel programming mode, chip erase is initiated by using the proper combination of control signals and by holding ALE/PROG low for 10 ms. The Code and Data arrays are written with all "1"s in the Chip Erase operation.

In the serial programming mode, a chip erase operation is initiated by issuing the Chip Erase instruction. In this mode, chip erase is self-timed and takes about 16 ms.

During chip erase, a serial read from any address location will return 00H at the data outputs.

Serial Programming Fuse: A programmable fuse is available to disable Serial Programming if the user needs maximum system security. The Serial Programming Fuse can only be programmed or erased in the Parallel Programming Mode.

The AT89S8252 is shipped with the Serial Programming Mode enabled.

Reading the Signature Bytes: The signature bytes are read by the same procedure as a normal verification of locations 030H and 031H, except that P3.6 and P3.7 must be pulled to a logic low. The values returned are as follows:

(030H) = 1EH indicates manufactured by Atmel
(031H) = 72H indicates 89S8252

Programming Interface

Every code byte in the Flash and EEPROM arrays can be written, and the entire array can be erased, by using the appropriate combination of control signals. The write operation cycle is self-timed and once initiated, will automatically time itself to completion.

Most worldwide major programming vendors offer support for the Atmel AT89 microcontroller series. Please contact your local programming vendor for the appropriate software revision.

Serial Programming Instruction

The Instruction Set for Serial Programming follows a 3-byte protocol and is shown in the following table:

Instruction Set

Instruction	Input Format			Operation
	Byte 1	Byte 2	Byte 3	
Programming Enable	1010 1100	0101 0011	xxxx xxxx	Enable serial programming interface after RST goes high.
Chip Erase	1010 1100	xxxx x100	xxxx xxxx	Chip erase both 8K & 2K memory arrays.
Read Code Memory	aaaa a001	low addr	xxxx xxxx	Read data from Code memory array at the selected address. The 5 MSBs of the first byte are the high order address bits. The low order address bits are in the second byte. Data are available at pin MISO during the third byte.
Write Code Memory	aaaa a010	low addr	data in	Write data to Code memory location at selected address. The address bits are the 5 MSBs of the first byte together with the second byte.
Read Data Memory	00aa a101	low addr	xxxx xxxx	Read data from Data memory array at selected address. Data are available at pin MISO during the third byte.
Write Data Memory	00aa a110	low addr	data in	Write data to Data memory location at selected address.
Write Lock Bits	1010 1100	LB1 LB2 LB3 x x111	xxxx xxxx	Write lock bits. Set LB1, LB2 or LB3 = "0" to program lock bits.

Notes:
1. DATA polling is used to indicate the end of a byte write cycle which typically takes less than 2.5 ms at 5V.
2. "aaaaa" = high order address.
3. "x" = don't care.

Flash and EEPROM Parallel Programming Modes

Mode	RST	PSEN	ALE/PROG	EA/V_{PP}	P2.6	P2.7	P3.6	P3.7	Data I/O P0.7:0	Address P2.5:0 P1.7:0
Serial Prog. Modes	H	h[1]	h[1]	x						
Chip Erase	H	L	(2)	12V	H	L	L	L	X	X
Write (10K bytes) Memory	H	L		12V	L	H	H	H	DIN	ADDR
Read (10K bytes) Memory	H	L	H	12V	L	L	H	H	DOUT	ADDR
Write Lock Bits:	H	L		12V	H	L	H	L	DIN	X
Bit - 1									P0.7 = 0	X
Bit - 2									P0.6 = 0	X
Bit - 3									P0.5 = 0	X
Read Lock Bits:	H	L	H	12V	H	H	L	L	DOUT	X
Bit - 1									@P0.2	X
Bit - 2									@P0.1	X
Bit - 3									@P0.0	X
Read Atmel Code	H	L	H	12V	L	L	L	L	DOUT	30H
Read Device Code	H	L	H	12V	L	L	L	L	DOUT	31H
Serial Prog. Enable	H	L	(2)	12V	L	H	L	H	P0.0 = 0	X
Serial Prog. Disable	H	L	(2)	12V	L	H	L	H	P0.0 = 1	X
Read Serial Prog. Fuse	H	L	H	12V	H	H	L	H	@P0.0	X

Notes:
1. "h" = weakly pulled "High" internally.
2. Chip Erase and Serial Programming Fuse require a 10 ms $\overline{PROG}$ pulse. Chip Erase needs to be performed first before reprogramming any byte with a content other than FFH.
3. P3.4 is pulled Low during programming to indicate RDY/$\overline{BSY}$.
4. "X" = don't care

Figure 13. Programming the Flash/EEPROM Memory

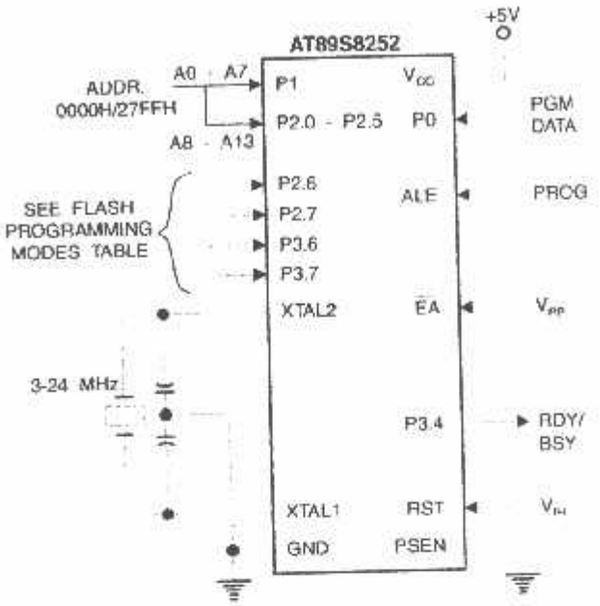


Figure 14. Verifying the Flash/EEPROM Memory

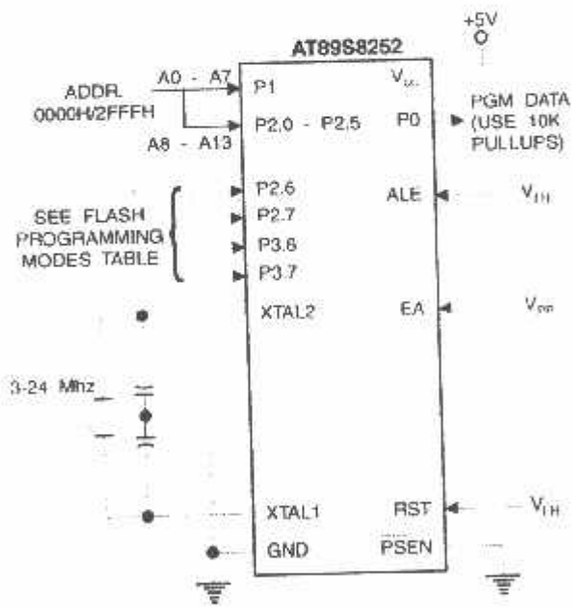
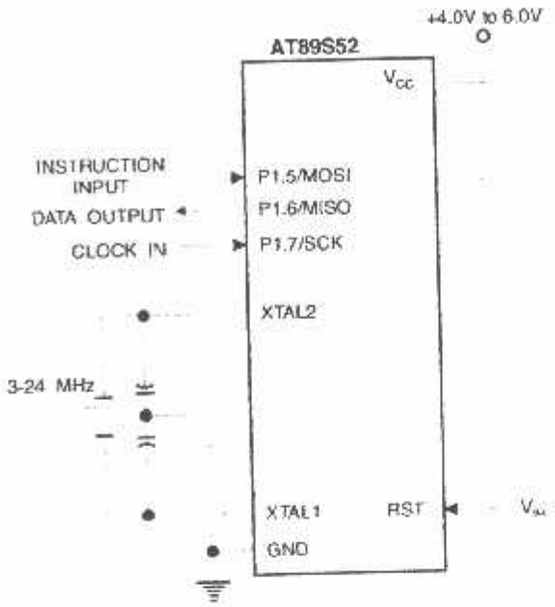


Figure 15. Flash/EEPROM Serial Downloading



Flash Programming and Verification Characteristics – Parallel Mode

T_A = 0°C to 70°C, V_{CC} = 5.0V ± 10%

Symbol	Parameter	Min	Max	Units
V_{PP}	Programming Enable Voltage	11.5	12.5	V
I_{PP}	Programming Enable Current		1.0	mA
$1/t_{CLCL}$	Oscillator Frequency	3	24	MHz
t_{AVGL}	Address Setup to $\overline{PROG}$ Low	$48t_{CLCL}$		
t_{GHAX}	Address Hold after $\overline{PROG}$	$48t_{CLCL}$		
t_{DVGL}	Data Setup to $\overline{PROG}$ Low	$48t_{CLCL}$		
t_{GHDX}	Data Hold after $\overline{PROG}$	$48t_{CLCL}$		
t_{EHSH}	P2.7 ($\overline{ENABLE}$) High to V_{PP}	$48t_{CLCL}$		
t_{SHGL}	V_{PP} Setup to $\overline{PROG}$ Low	10		µs
t_{GLGH}	$\overline{PROG}$ Width	1	110	µs
t_{AVQV}	Address to Data Valid		$48t_{CLCL}$	
t_{ELQV}	$\overline{ENABLE}$ Low to Data Valid		$48t_{CLCL}$	
t_{EHQZ}	Data Float after $\overline{ENABLE}$	0	$48t_{CLCL}$	
t_{GHBL}	$\overline{PROG}$ High to $\overline{BUSY}$ Low		1.0	µs
t_{WC}	Byte Write Cycle Time		2.0	ms

Flash/EEPROM Programming and Verification Waveforms – Parallel Mode