INSTITUT TEKNOLOGI NASIONAL MALANG
FAKULTAS TEKNOLOGI INDUSTRI
JURUSAN TEKNIK ELEKTRO S-1
KONSENTRASI TEKNIK ELEKTRONIKA

PERANCANGAN DAN PEMBUATAN ALAT PENCATAT PEMAKAIAN AIR PELANGGAN PDAM DAN DITRANSMISIKAN MELALUI RADIO PAKET YANG DIHUBUNGKAN DENGAN PC PDAM BERBASIS MIKROKONTROLLER AT89S8252

SKRIPSI

Disusun Oleh :

DAVID AFIANTO

01.17.054

MARET 2006

LEMBAR PERSETUJUAN

PERANCANGAN DAN PEMBUATAN ALAT PENCATAT PEMAKAIAN AIR PELANGGAN PDAM DAN DITRANSMISIKAN MELALUI RADIO PAKET YANG DIHUBUNGKAN DENGAN PC PDAM BERBASIS MIKROKONTROLLER AT89S8252

Disusun dan Diajukan untuk Melengkapi dan Memenuhi Syarat Guna Mencapai Gelar Sarjana Teknik Elektro Strata Satu (S-1)

Disusun Oleh :

DAVID AFIANTO

01.17.054

Diperiksa dan Disetujui,

Dosen Pembimbing I	Dosen Pembimbing II
(Ir. F. Yudi Limpraptono, MT)	(Ir. Mimien Mustikawati)
NIP. Y. 1039500274	NIP. P. 1030000352

Mengetahui,

Ketua Jurusan T. Elektro

(Ir. F. Yudi Limpraptono, MT)

NIP.Y. 1039500274

JURUSAN TEKNIK ELEKTRO S-1

KONSENTRASI TEKNIK ELEKTRONIKA

FAKULTAS TEKNOLOGI INDUSTRI

INSTITUT TEKNOLOGI NASIONAL MALANG

INSTITUT TEKNOLOGI NASIONAL
FAKULTAS TEKNOLOGI INDUSTRI
JURUSAN TEKNIK ELEKTRO S-1
KONSENTRASI TEKNIK ELEKTRONIKA

BERITA ACARA UJIAN SKRIPSI
FAKULTAS TEKNOLOGI INDUSTRI

Nama	: DAVID AFIANTO
Nim	: 01.17.054
Jurusan	: Teknik Elektro S-1
Konsentrasi	: Teknik Elektronika
Judul Skripsi	: Perancangan dan Pembuatan Alat Pencatat Pemakaian Air Pelanggan PDAM dan Ditransmisikan Melalui Radio Paket yang Dihubungkan dengan PC PDAM Berbasis Mikrokontroller AT89S8252

Dipertahankan di hadapan majelis penguji Skripsi jenjang Strata satu (S-1) pada :

Hari	: Rabu
Tanggal	: 22 Maret 2006
Dengan Nilai	: 87,5 (A)

Panitia Ujian Skripsi

Ketua

(Ir. Mochtar Asroni, MSME)
NIP. Y. 1018100036

Sekretaris

(Ir. F. Yudi Limpraptono, MT)
NIP. Y. 1039500274

Anggota Penguji

Penguji I

(M. Ibrahim Ashari, ST)
NIP. Y. 1030100358

Penguji II

(Irmalia Suryani F, ST)
NIP. Y. 1030100365

بسم الله الرحمن الرحيم

Kupersembahkan Karya Ini Untuk :

- Ayah dan Ibunda tercinta terima kasih atas kasih sayang, perhatian dorongan dan do'a yang tulus untukku.
- Kakakku yang selalu memberikan perhatian dan semangat untukku.
- Seseorang yang selalu memberiku perhatian "Lulut Wijayanti" serta selalu menemaniku disaat suka maupun duka, Honey I Love You So Much.
- Keponakan-keponakanku yang selalu mewarnai dalam hidupku.
- Serta tak lupa buat Best Friend "Agus" thanx's for your support & sorry I always late if we have promise go to campus & for Lk-2 Childrens love & peace for you.
- Serta tak lupa juga buat anak-anak C-332, aku harap persahabatan kita tidak berakhir sampai disini, I love you all & thank's for your support.
- For ex my band, I hope you can continue we struggle.

بسم الله الرحمن الرحيم

Motto :

- *Hidup adalah sebuah Perjuangan yang harus kita menangkan.*
- *Hari esok harus lebih baik dari hari sekarang.*
- *Kasih sayang dan cinta adalah anugrah dari yang Maha Kuasa sepatutnyalah kita menjaganya dan merawatnya dengan tulus hati.*
- *Do'a dan semangat adalah kunci keberhasilan dalam cita dan cinta.*

DAFTAR ISI

HALAMAN JUDUL i

LEMBAR PERSETUJUAN ii

BERITA ACARA SKRIPSI iii

LEMBAR PERSEMBAHAN iv

ABSTRAKSI vi

KATA PENGANTAR vii

DAFTAR ISI viii

DAFTAR TABEL xi

DAFTAR GAMBAR xii

BAB I PENDAHULUAN

1.1. Latar Belakang Masalah 1

1.2. Rumusan Masalah 2

1.3. Batasan Masalah 2

1.4. Tujuan 3

1.5. Metodologi Penulisan 3

1.6. Sistematika Penulisan 4

BAB II LANDASAN TEORI

2.1. Mikrokontroller AT89S51 5

2.1.1. Teori umum 5

2.1.2. Konfigurasi Pin Pada Mikrokontroller AT89S8252 .. 9

2.1.3. Masukan dan Keluaran 13

2.1.4 Organisasi Memori 13

2.1.4.1. Data Memori (EEPROM) dan RAM 13

2.1.4.2. SFR (*Special Function Register*) 16

2.1.4.2.1. SFR untuk Timer 2 18

2.1.4.2.2. SFR untuk Watchdog & memori 19

2.1.4.2.3. SFR pengontrol SPI 19

2.1.5. Osilator 20
2.1.6. Timer dan Counter 21
2.1.7. Sistem Interrupt 23
2.1.8. Reset 24
2.2. LCD (*Liquid Cristal Display*) 24
2.2.1 Instruksi Operasi 27
2.2.2. Operasi Dasar 28
2.3. Papan Tombol (*Keypad*) 30
2.4. Modulasi FSK 32
2.4.1. Modulator FSK XR2206 33
2.4.2. Demodulator FSK XR2211 36
2.5. Perangkat Komunikasi Data 38
2.5.1. Serial Interface RS-232 38
2.5.2. Max 232 39
2.6. Transmisi Data Asinkron 40

BAB III PERANCANGAN DAN PEMBUATAN ALAT

3.1. Gambaran Umum Sistem 42
3.2. Diagram Blok 42
3.3. Rangkaian Interface RS-232 45
3.4. Perancangan Perangkat Keras Modulator Demodulator 46
3.4.1. FSK XR2206 (Modulator FSK) 46
3.4.2. FSK XR2211 (Demodulator FSK) 48
3.5. Perancangan Sistem Mikrokontroler 51
3.6. Mikrokontroler AT89S8252 51
3.7. Papan Tombol (*Keypad*) 53
3.8. LCD (*Liquid Cristal Display*) 54
3.9. Perancangan Perangkat Lunak 55

BAB IV ANALISISA DAN PENGUJIAN ALAT

4.1. Tujuan 58
4.2. Pengujian Sistem Mikrokontroler 58

4.3. Pengujian Komunikasi Serial 61
4.4. Pengujian Rangkaian IC XR2206 dan IC XR2211 63
4.5. Pengujian Rangkaian Keypad 66
4.6. Pengujian LCD 68
4.7. Pengujian secara keseluruhan 69

BAB V PENUTUP

5.1. Kesimpulan 73
5.2. Saran 74

DAFTAR PUSTAKA

LAMPIRAN

DAFTAR TABEL

Tabel 2-1. Fungsi Alternatif Port 1 10
Tabel 2-2. Fungsi Alternatif Port 3 11
Tabel 2-3. Pengaturan RS0-RS1 untuk Select Register Bank 15
Tabel 2-4. 128 Byte Special Function Register 16
Tabel 2-5. Mode Operasi Timer/Counter 0 dan 1 21
Tabel 2-6. Mode Operasi Timer 2 22
Tabel 2-7. Fungsi Tiap Pin LCD 27
Tabel 2-8. Instruksi Pada LCD 27
Tabel 2-9. Pemilihan Register Pada LCD 28
Tabel 2-10. Konfigurasi Pin dan Fungsi Pin RS232 dengan DB9 Conector 39
Tabel 4-1. Hasil Pengujian Sistem Mikrokontroller 60
Tabel 4-2. Hasil Pengujian Transfer data serial 63
Tabel 4-3. Hasil Pengujian TX XR2206 dan RX XR2211 pada PC 64
Tabel 4-4. Hasil Pengujian pengkode papan tombol (*keypad*) 67

BAB I

PENDAHULUAN

1.1. Latar Belakang

Seiring dengan perkembangan pembangunan, teknologi elektronika mengalami kemajuan yang begitu cepat, menyebabkan manusia tidak akan lepas dari penggunaan berbagai macam peralatan elektronika yang ada, baik itu penggunaan peralatan yang menggunakan perangkat keras maupun perangkat lunak elektronika.

Pada perkembangannya teknologi elektronika menuntut manusia untuk merekayasa suatu peralatan elektronika yang praktis.

Dari uraian diatas salah satu peralatan elektronika yang berkembang dewasa ini banyak menggunakan suatu perangkat lunak yang akan menjalankan suatu peralatan elektronika. Dengan menggunakan peralatan yang diprogram oleh suatu perangkat lunak maka akan diperoleh kemudahan dalam pembuatan peralatan elektronika yang akan dirancang. Dengan adanya peralatan pencatat pemakaian air yang dikontrol oleh sebuah software, maka akan mempermudah bagi petugas pencatat pemakaian air dan ini akan meminimalkan kesalahan pada saat pencatatan.

Salah satu perangkat yang digunakan pada alat ini adalah IC mikrokontroller AT89S8252, yang merupakan mikrokontroller dengan memori internal yang mampu menyimpan berbagai data untuk penggunaan bermacam-macam aplikasi peralatan elektronika.

Didasari oleh latar belakang tersebut, maka dalam skripsi ini akan dibuat suatu peralatan elektronika yang dijalankan oleh perangkat lunak yang nantinya digunakan untuk mempermudah dalam pencatatan pemakaian air.

1.2. Rumusan Masalah

Rumusan masalah dalam penyusunan skripsi ini menekankan pada bagaimana memberikan kemudahan bagi pencatat meteran air. Dengan banyaknya data yang akan dicatat, maka akan mempersulit bagi petugas pencatat meteran air dan akan cenderung mengambil data secara acak misalnya 3 bulan sekali, data acak ini sering kali akan merugikan pelanggan, maka alat ini dibuat untuk memberikan kemudahan bagi petugas pencatat meteran air, karena alat ini berfungsi untuk menyimpan dan menampilkan no. pelanggan, serta biaya pada bulan ini yang harus dibayar oleh pelanggan ke kantor PDAM.

1.3. Batasan Masalah

Agar permasalahan tidak meluas, maka dalam skripsi ini penulis membatasi hanya pada hal-hal berikut :

- Menggunakan mikrokontroller AT89S8252
- Tidak membahas radio paket
- Modem yaitu sebagai modulator IC XR2206 dan demodulator IC XR2211
- Pada PC menggunakan perangkat lunak Visual Basic 6
- Tidak membahas perangkat keras pada PC
- Tidak membahas perancangan dan pembuatan catu daya
- Sebagai simulasi pelanggan air PDAM ada 5 rumah

1.4. Tujuan

Tujuan dari penulisan skripsi ini adalah untuk merencanakan dan membuat suatu alat untuk menyimpan dan menampilkan nomor pelanggan, serta biaya pada bulan ini yang harus dibayar oleh pelanggan ke kantor PDAM, dan membuat program perangkat lunak sebagai pengendali dari peralatan yang akan dibuat.

1.5. Metodologi

Metodologi yang digunakan dalam penyusunan tugas skripsi ini adalah sebagai berikut :

1. Studi literature, meliputi :

   Melakukan kajian dari buku, majalah atau hasil penelitian dilaboratorium.

2. Perancangan tiap blok diagram

   Perancangan ini dilakukan berhubungan dengan kerja alat yang digunakan.

3. Pengujian alat

   Pengujian alat dilakukan perblok sistem dan keseluruhan sistem yang telah disusun sehingga disimpulkan suatu efektifitas penggunaan suatu alat.

4. Analisa

   Merupakan analisa data dari hasil pengujian alat yang telah dilakukan.

1.6. Sistematika penulisan

Sistematika penulisan dari tugas akhir ini adalah sebagai berikut :

- BAB I : Pendahuluan

  Membahas tentang latar belakang permasalahan, rumusan masalah, batasan masalah, tujuan, metodologi, dan sistematika penulisan.

- BAB II : Landasan Teori

  Membahas teori penunjang dalam perencanaan dan pembuatan alat yang akan dibuat.

- BAB III : Perancangan dan pembuatan program dan alat, membahas tentang perancangan alat dan program yang digunakan, mulai dari pembuatan hardware dan software sampai dengan cara kerja alat.

- BAB IV : Pengujian Alat dan Analisa

  Membahas pengujian dari alat yang telah selesai dengan menjalankan program tersebut serta menganalisa hasilnya.

- BAB V : Penutup

  Membahas tentang kesimpulan dan saran dari hasil perancangan dan pembuatan alat pencatat pemakaian air pelanggan PDAM dan ditransmisikan melalui radio paket yang dihubungkan dengan PC PDAM berbasis mikrokontroller AT89S8252.


INSTITUT TEKNOLOGI NASIONAL
ITN
MALANG

BAB II

LANDASAN TEORI

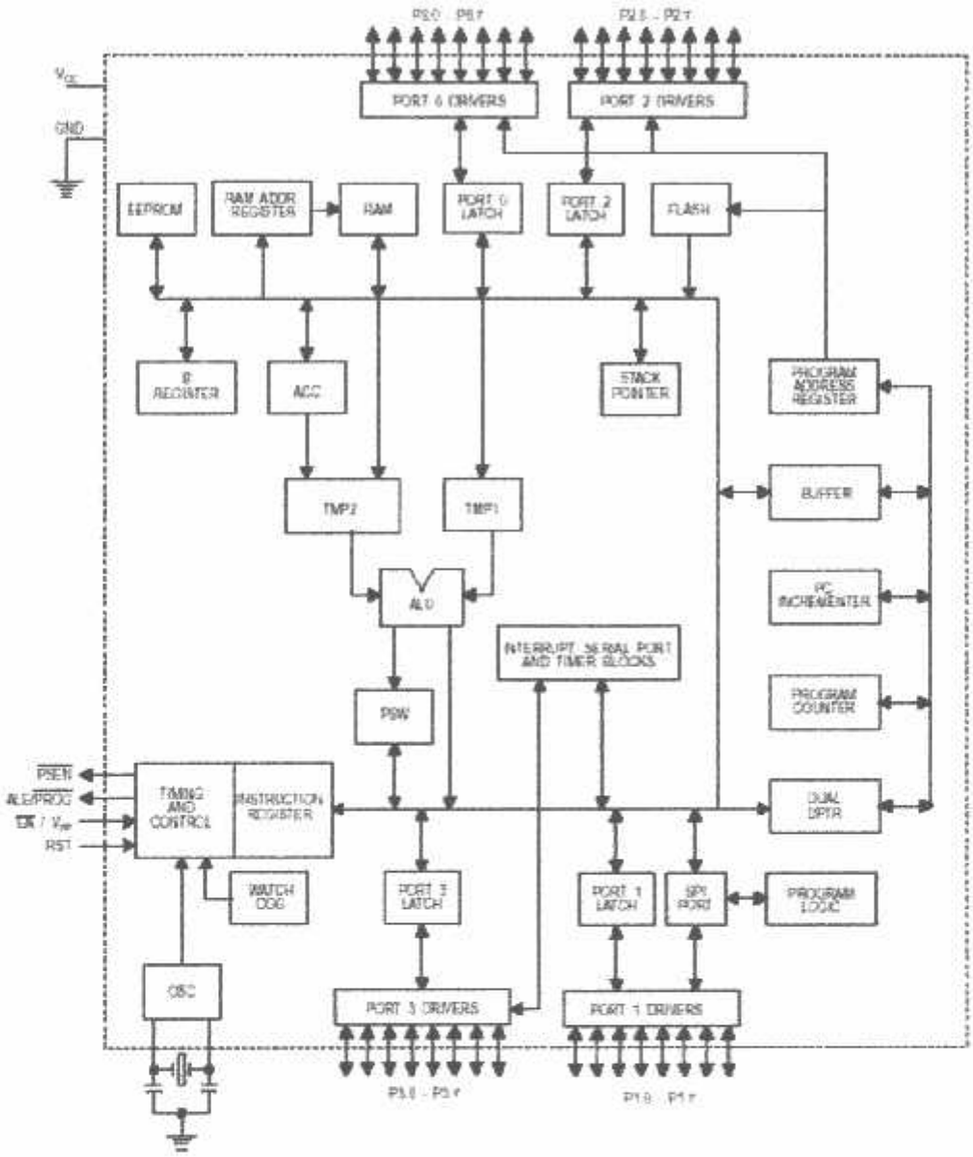
2.1. Mikrokontroler AT89S8252

2.1.1. Teori Umum

SCM (*single on-chip*) adalah suatu mikrokontroler lengkap yang dibuat dalam sebuah IC yang mempunyai struktur seperti CPU, Osilator, Timer, RAM, EPROM dan Buffer (alamat, data dan input-output). Mikrokontroler AT89S8252 merupakan mikrokontroler 8-bit kompatibel dengan standar industri *MCS-51*™ baik dari segi pemprograman maupun kaki tiap pin. Mikrokontroler AT89S8252 mempunyai 8 Kbyte PEROM (*Programmable and Erasable Read Only Memory*).

Pada dasarnya mikrokontroler terdiri atas mikroprosesor, timer, counter, perangkat I/O dan internal memori. Mikrokontroler termasuk perangkat yang mudah didesain dalam bentuk chip tunggal (*single chip*). Pada dasarnya mikrokontroler mempunyai fungsi yang sama dengan mikroprosesor yaitu untuk mengontrol suatu kerja sistem.

Diagram blok dari IC AT89S8252 seperti gambar 2.1. dibawah ini.



Gambar 2.1. Diagram Blok AT89S8252[1]

Di dalam mikrokontroller juga terdapat CPU, ALU, PC, SP dan register seperti dalam mikroprosesor, tetapi juga ditambah dengan perangkat-perangkat lain seperti RAM, ROM, PIO, SIO, Counter dan sebuah rangkaian Clock.

RAM pada dasarnya merupakan suatu flip-flop yang dapat diset/direset, sifat ini membuat RAM dapat dibaca atau ditulis. Karena transistor yang menyusun flip-flop membutuhkan suatu tegangan DC agar tetap aktif, maka sel RAM akan kehilangan datanya bila power dimatikan. Hal ini dalam dunia komputer disebut bersifat *volatile*. Sedangkan ROM memiliki beberapa tipe diantaranya yaitu *Mask Programmable* ROM, *Fusible Link* PROM, *UV Light Erasable* PROM (EPROM) dan EEPROM. Tidak seperti RAM, data yang ada didalam ROM tidak akan hilang bila power dimatikan. Hal ini disebut bersifat *non-volatile*, suatu pemrogram khusus yang diperlukan untuk menulis data ke ROM. Karena non-volatilitasnya maka ROM sering dipetakan ke alamat reset dari mikrokontroler, dalam hal ini sangat diperlukan pada saat melakukan *booting*.

Mikrokontroler didesain dengan instruksi-instruksi lebih luas dan 8-bit instruksi yang digunakan untuk membaca data instruksi dari internal memori ke ALU. Sebagai suatu sistem kontrol, mikrokontroler bila dibandingkan dengan mikroprosesor memiliki kemampuan dan segi ekonomis yang bisa diandalkan karena dalam mikrokontroler sudah terdapat RAM dan ROM sedangkan mikroprosesor didalamnya tidak terdapat keduanya. Terlihat bahwa mikrokontroler Atmel AT89S8252 memiliki banyak fitur yang menguntungkan. Dipakainya *downloadable flash memory* memungkinkan mikrokontroler ini bekerja sendiri tanpa diperlukan tambahan chip lainnya. Sementara flash memorinya mampu diprogram hingga seribu kali. Hal lain yang menguntungkan adalah sistem pemrograman menjadi lebih sederhana dan tidak memerlukan rangkaian yang rumit seperti rangkaian untuk memprogram produk Atmel

lainnya. Di samping itu pula mikrokontroler AT89S8252 membutuhkan daya rendah dan memiliki performen yang tinggi.

AT89S8252 juga mempunyai 2 buah *Power Saving Mode* yang dapat diatur melalui *software*, yaitu IDE Mode yang akan menghentikan CPU sebagai RAM, dimana Timer/Counter, Serial Port dan Interrupt Sistem tetap berfungsi. Sedangkan *Power Down Mode* yang akan menyimpan data di RAM dan akan menahan osilator untuk tidak mengaktifkan chip yang lain sampai terjadi reset secara *hardware*.

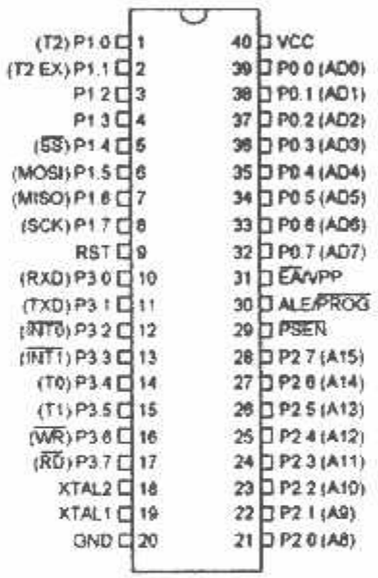
Adapun secara umum, konfigurasi yang dimiliki mikrokontroler AT89S8252[1] adalah sebagai berikut :

- Sebuah CPU 8-bit dengan menggunakan teknologi dari Atmel
- 8 Kbyte *Downloadable Flash Memory*
- 2 Kbyte EEPROM
- Sebuah port serial dengan kontrol *full duplex* UART (*Universal Asynchronous Receiver Transmitter*)
- 256 byte RAM internal
- 32 I/O yang dapat dipakai semuanya
- 3 buah Timer/Counter 16-bit
- 6 Sumber Interrupt
- SPI Serial Interface
- *Programmable Watchdog Timer*
- *Dual data pointer*
- Frekuensi kerja 0 – 24 MHz

- Tegangan operasi 2,7 V sampai 6 V
- *Power-of flag*
- Kemampuan melaksanakan operasi perkalian, pembagian dan operasi Boolean (bit)

2.1.2. Konfigurasi Pin Pada Mikrokontroller AT89S8252

Konfigurasi kaki-kaki mikrokontroler AT89S8252 terdiri dari 40 pin seperti yang terlihat pada gambar berikut ini.



Gambar 2.2. Konfigurasi Pin-Pin AT89S8252[1]

Adapun fungsi dari tiap pin akan dijelaskan sebagai berikut :

- Pin 1 – 8

  Port 1 yang terdiri atas pin 1 – 8 merupakan saluran masukan/keluaran dua arah dengan internal *pull-up* dan mempunyai fungsi khusus seperti yang terlihat pada tabel

Tabel 2.1. Fungsi Alternatif Port 1

Port Pin	Fungsi
P1.0	T2 (masukan eksternal untuk Timer/Counter 2)
P1.1	T2EX (Timer/Counter 2 capture/reload trigger dan kontrol arah
P1.2	-
P1.3	-
P1.4	SS (slave port select input)
P1.5	MOSI (master data output, slave data input untuk chanel SPI)
P1.6	MISO (maser data input, slave data output untuk chanel SPI)
P1.7	SCK (master clock output, slave clock input untuk chanel SPI)

- Pin 9

  RST merupakan saluran 2 masukan untuk mereset mikrokontroler dengan cara memberi masukan logika tinggi

- Pin 10 – 17

  Port 3 yang terdiri atas pin 10 – 17 merupakan saluran masukan/keluaran dua arah dengan internal *pull-up* dan mempunyai fungsi khusus seperti yang terlihat pada tabel

Tabel 2.2. Fungsi Alternatif Port 3

Port Pin	Fungsi
P3.0	RXD (port serial input)
P3.1	TXD (port serial output)
P3.2	INT0 (interrupt eksternal 0)
P3.3	INT1 (interrupt eksternal 1)
P3.4	T0 (input eksternal timer 0)
P3.5	T1 (input eksternal timer 1)
P3.6	WR (menulis data ke memori eksternal)
P3.7	RD (membaca data dari memory eksternal)

- Pin 18 – 19

  $XTAL_1$ dan $XTAL_2$ merupakan saluran untuk mengatur pewaktuan sistem. Untuk pewaktuan dapat menggunakan pewaktuan internal maupun eksternal. Pin ini dihubungkan dengan kristal bila menggunakan osilator internal. $XTAL_1$ merupakan masukan ke rangkaian osilator internal sedangkan $XTAL_2$ merupakan keluaran dari rangkaian osilator internal

- Pin 20

  V_{SS} merupakan hubungan ke ground dari rangkaian

- Pin 21 – 28

  Port 2 yang terdiri atas pin 21 – 28 merupakan saluran masukan/keluaran dua arah dengan internal *pull-up*. Port ini mengeluarkan 8-bit bagian alamat tinggi (A_8 – A_{15}) selama pengambilan instruksi dari memori

program eksternal dan pengambilan data memori eksternal menggunakan mode pengalamatan 16-bit

- Pin 29

  PSEN (*Program Store Enable*) merupakan sinyal baca untuk mengaktifkan memori program eksternal

- Pin 30

  ALE/PROG (*Address Latch Enable*) merupakan pulsa yang berfungsi untuk mengeluarkan alamat rendah ($A_0 - A_7$) dalam port 0, selama proses baca/tulis memori eksternal. Frekuensi ALE adalah 1/6 kali frekuensi osilator dan dapat digunakan sebagai pewaktu. Pin ini juga berfungsi sebagai saluran program selama dilakukan pemrograman jika menggunakan memori program internal

- Pin 31

  EA/VPP (*External Access Enable*) untuk mengatur penggunaan memori program eksternal dan internal. Pin ini harus dihubungkan dengan ground bila menggunakan memori program eksternal dan dihubungkan dengan VPP sebesar 12 V jika menggunakan memori program internal. Dapat diberikan logika rendah (ground) atau logika tinggi (+5V), jika diberikan logika tinggi maka mikrokontroler akan mengakses program dari ROM internal (EEPROM/*Flash Memory*), dan jika diberikan logika rendah maka mikrokontroler akan mengakses program dari memori eksternal

- Pin 32 – 39

  Port 0 yang terdiri atas pin 32 – 39 merupakan saluran masukan/keluaran dua arah tanpa internal *pull-up*. Port 0 merupakan saluran alamat rendah ($A_0 - A_7$) yang dimultipleks dengan saluran bus data ($D_0 - D_7$)

- Pin 40

  V_{CC} merupakan saluran masukan untuk catu daya positif sebesar 5 volt DC dengan toleransi kurang lebih 1 %

2.1.3. Masukan dan Keluaran

Untuk saluran masukan dan keluaran terdapat 4 buah port yang masing-masing 8-bit. Saluran ini bersifat dua arah (*bidirectional*) yang berarti dapat difungsikan sebagai masukan/keluaran, serta dapat dialamati per bit. Port 3 selain digunakan sebagai port masukan dan keluaran juga dapat digunakan sebagai fungsi pengganti sebagaimana yang terdapat dalam tabel 2.2. AT89S8252 juga memiliki fitur tambahan yang terdapat pada port 1 seperti dalam tabel 2.1.

2.1.4. Organisasi Memori

2.1.4.1. Data Memori (EEPROM) dan RAM

Berbeda dengan mikrokontroler standar MCS-51, untuk AT89S8252 terdapat 2 Kbytes dalam EEPROM untuk penyimpanan data dan 256 byte untuk RAM. Dibagian atas 128 byte RAM ditempati paralel untuk SFR. Bagian atas 128 byte mempunyai alamat sama dengan SFR, tetapi secara fisik terpisah dari SFR.

EEPROM on-chip ini diakses dengan mengeset bit EEMEN pada register WMCON pada alamat 96_H. Alamat EEPROM ini adalah 000_H sampai $7FF_H$. Dan

selama EEPROM memprogram, yang dibaca dari EEPROM akan mengambil byte yang sedang ditulis dengan melengkapi MSB. Instruksi *movx* digunakan untuk mengakses EEPROM internal ini. Bit EEMWE pada register WMCON harus diset ke "1" sebelum sembarang lokasi pada EEPROM dapat ditulisi. Program pengguna harus mereset bit EEMWE ke "0" jika proses penulisan ke EEPROM tidak diperlukan lagi. Proses penulisan ke EEPROM dapat dilihat dengan membaca bit RDY/BSY pada SFR WMCON. Jika bit ini berlogika rendah maka berarti penulisan EEPROM sedang berlangsung, tapi jika bit ini berlogika tinggi berarti penulisan sudah selesai dan penulisan lain dapat dimulai lagi.

Sedangkan RAM yang ada pada mikrokontroler AT89S8252 berkapasitas 256 byte dan kompatibel dengan RAM yang ada pada mikrokontroler standar MCS-51. Pada lower 128-bit lokasi memori dapat dibagi menjadi 3 bagian, yaitu :

1. Empat Bank Register

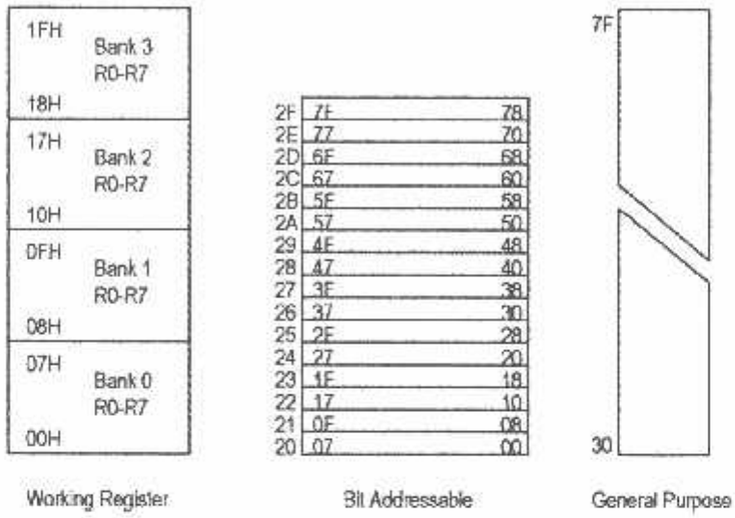
   Setiap bank terdiri dari 8 register (R0-R7), sehingga jumlah register untuk keempat bank register (bank 0 – bank 3) menjadi 32 buah register yang menempati ruang alamat 00_H – $1F_H$. Untuk mengaktifkan salah satu bank register dapat dilakukan dengan mengatur RS0-RS1 melalui pengaturan pada PSW (*Program Status Word*)

2. Bit Addressable

   Terdiri dari 16-bit yang berada pada alamat 20_H – $2F_H$. Masing- masing dari 128-bit lokasi ini dapat dialamati secara langsung yaitu dari 00_H – $7F_H$

3. Scratch Pad Area

Terdiri dari 80-byte yang menempati alamat 30_H – $7F_H$ yang dapat dialamati secara langsung dan dapat digunakan untuk keperluan umum (*General Purpose* RAM). Misalnya digunakan untuk lokasi *stack*.



Gambar 2.3. Organisasi RAM Internal[2]

Tabel 2.3. Pengaturan RS0-RS1 Untuk Select Register Bank[2]

RS1	RS0	Select Register Bank
0	0	Bank 0
0	1	Bank 1
1	0	Bank 2
1	1	Bank 3

2.1.4.2. SFR (*Special Function Register*)

Area memori AT89S8252 disebut dengan SFR (*Special Function Register*) yang merupakan register dengan tugas khusus. Tidak semua address digunakan sebagai SFR, hanya addres tertentu seperti yang dijelaskan oleh tabel 2.4 berikut ini.

Tabel 2.4. 128 Byte Special Function Register[2]

SYMBOL	NAME	ADDRESS
ACC	ACCUMULATOR	0E0H
B	B REGISTER	0F0H
PSW	PROGRAM STATUS WORD	0D0H
SP	STACK POINTER	81H
DPTR	DATA POINTER 2 BYTE	
DPL	LOW BYTE	82H
DPH	HIGH BYTE	83H
P0	PORT 0	80H
P1	PORT 1	90H
P2	PORT 2	0A0H
P3	PORT 3	080H
IP	INTERRUPT PERIORITY CONTROL	088H
IE	INTERRUPT ENABLE CONTROL	0ABH
TMOD	TIMER/COUNTER MODE CONTROL	89H
TCON	TIMER/COUNTER CONTROL	88H

+TCON	TIMER/COUNTER 2 CONTROL	0CBH
TH0	TIMER/COUNTER 0 HIGH CONTROL	8CH
TL0	TIMER/COUNTER 0 LOW CONTROL	8DH
TH1	TIMER/COUNTER 1 HIGH CONTROL	8DH
TL1	TIMER/COUNTER 1 LOW CONTROL	8CH
TH2	TIMER/COUNTER 2 HIGH CONTROL	0CDH
TL2	TIMER/COUNTER 2 LOW CONTROL	0CCH
RCAP2H	T/C 2 CAPTURE REG. HIGH BYTE	0CBH
+RCAP2L	T/C 2 CAPTURE REG. LOW BYTE	0CAH
SCON	SERIAL CONTROL	98H
SBUF	SERIAL DATA BUFFER	99H
PCON	POWER CONTROL	87H

Akses pembacaan dari semua address akan diwujudkan dalam bentuk random data dan penulisan akses diwujudkan dalam bentuk (efek) tidak tentu. SFR pada mikrokontroler AT89S8252 kompatibel dengan mikrokontroler keluarga MCS-51 dan memiliki alamat 80_H sampai FF_H sehingga terdapat 128-bit lokasi alamat untuk SFR. Namun demikian, pada mikrokontroler ini tidak berarti memiliki SFR sebanyak 128 buah.

Selain itu mikrokontroler AT89S8252 memiliki tambahan SFR. Hal ini tak lain adalah karena terdapatnya tambahan fitur pada mikrokontroler ini. SFR tambahan ini meliputi T2CON (Timer 2 Control dengan alamat $0C8_H$), T2MOD (Timer 2 Mode dengan alamat $0C9_H$), WMCON (*Watchdog and Memory Control*

Register dengan alamat 96_H), SPCR (SPI Control Register dengan alamat $D5_H$), SPSR (SPI Status Register dengan alamat AA_H), SPDR (SPI Data Register dengan alamat 86_H). Gambar berikut akan menjelaskan letak masing-masing SFR.

0F8H								0FFH
0F0H	B 00000000							0F7H
0E8H								0EFH
0E0H	ACC 00000000							0E7H
0D8H								0DFH
0D0H	PSW 00000000					SPCR 00000XX		0D7H
0C8H	T2CON 00000000	T2MOD XXXXXX00	RCAP2L 00000000	RCAP2H 00000000	TL2 00000000	TH2 00000000		0CFH
0C0H								0C7H
0B8H	IP XX000000							0BFH
0B0H	P3 11111111							0B7H
0A8H	IE 0X000000		SPSR 00XXXXXX					0AFH
0A0H	P2 11111111							0A7H
98H	SCON 00000000	SBUF XXXXXXXX						9FH
90H	P1 11111111						WMCON 00000010	97H
88H	TCON 00000000	TMOD 00000000	TL0 00000000	TL1 00000000	TH0 00000000	TH1 00000000		8FH
80H	P0 11111111	SP 00000111	DPOL 00000000	DP0H 00000000	DP1L 00000000	DP1H 00000000	SPDR XXXXXXXX	PCON 00X10000	87H

Gambar 2.4. Peta Letak SFR Pada Mikrokontroller AT89S8252[1]

2.1.4.2.1. SFR untuk Timer 2

Mikrokontroler AT89S8252 terdapat tambahan sebuah Timer/Counter yang diberi nama Timer 2 (sehingga AT89S8252 memiliki 3 Timer/Counter yaitu Timer/Counter 0, Timer/Counter 1, Timer/Counter 2). Pada Timer/Counter 2 ini dikendalikan oleh SFR yang bernama T2CON (Timer 2 Control), T2MOD (Timer 2 Mode) dan sepasang register RCAP2H, RCAP2L yang merupakan register *capture/reload* untuk Timer 2 dalam 16-bit *capture mode/auto-reload mode*.

2.1.4.2.2. SFR untuk Watchdog dan Memori

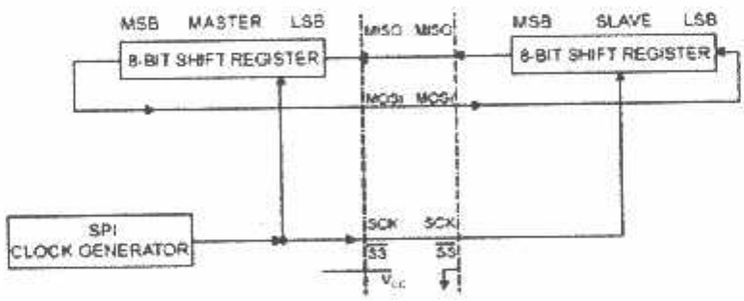
Untuk menggunakan Watchdog Timer/Memori, maka dapat dilakukan dengan mengatur SFR yang bernama WMCON dengan alamat 96_{H}.

2.1.4.2.3. SFR pengontrol SPI

Berbeda dengan mikrokontroler MCS-51, AT89S8252 memiliki fasilitas SPI (*Serial Peripheral Interface*). Fasilitas ini memungkinkan transfer data kecepatan tinggi secara sinkron antara mikrokontroler dengan peripheral atau antar mikrokontroler AT89S8252. Fitur ini meliputi :

a. *Full Duplex*, 3 kawat dengan transfer data secara sinkron
b. Operasi Master atau Slave
c. Frekuensi maksimum 6 MHz
d. 4-bit rate terprogram
e. Sistem data transfer MSB dahulu atau LSB
f. Write Collision Flag Protection

Gambar berikut menunjukkan hubungan antara CPU master dan slave.



Gambar 2.5. Koneksi SPI Master dan Slave[6]

2.1.5. Osilator

Jantung dari AT89S8252 adalah rangkaian yang membangkitkan pulsa clock yang mensinkronkan semua operasi internal. Mikrokontroler AT89S8252 memiliki osilator internal (*on-chip oscilator*) yang dapat digunakan sebagai sumber pewaktu (clock) bagi CPU. Untuk menggunakan osilator internal diperlukan sebuah kristal atau resonator keramik antara pin $XTAL_1$ dan $XTAL_2$ dan sebuah kapasitor ke ground. $XTAL_2$ dan $XTAL_1$ secara berurutan merupakan input dan output dari sebuah inverting amplifier yang dapat dikonfigurasikan penggunaannya sebagai *on-chip oscillator* seperti yang ditunjukkan pada gambar 2.6a.

Untuk memberikan IC AT89S8252 sumber clock eksternal, maka pin $XTAL_2$ dibiarkan tidak berhubungan dengan sumber clock eksternal dan $XTAL_1$ dihubungkan dengan sumber clock eksternal seperti pada gambar 2.6b.

a). *Oscillator Connector* b). *External Clock Drive Configuration*

Gambar 2.6. Karakteristik Osilator[1]

2.1.6. Timer dan Counter

Dalam mikrokontroler AT89S8252 terdapat 3 buah pewaktu/pencacah (Timer/Counter) 16-bit yang dapat diatur melalui perangkat lunak, yaitu pewaktu/pencacah 0 dan pewaktu/pencacah 1. Timer/Counter ini diatur oleh SFR (*Special Function Register*) yaitu Timer/Counter Control (TCON dengan alamat 88_{H}) dan Timer/Counter Mode Control (TMOD dengan alamat 89_{H}). Selain itu nilai byte bawah dan byte atas dari Timer/Counter disimpan dalam register TL dan TH.

Jika difungsikan sebagai Timer, maka akan menggunakan sistem clock sebagai sumber masukan pulsanya. Jika sebagai Counter (pencacah), maka akan menggunakan pulsa dari luar (eksternal) sebagai masukan pulsanya. Pada port 3 terdapat fungsi khusus yaitu T0 (masukan luar untuk Timer/Counter 0) dan T1 (masukan luar untuk Timer/Counter 1). Pemilihan mode Timer/Counter dikontrol oleh register TMOD. Dengan memberikan nilai tertentu pada regiater TMOD, dapat dipilih mode operasi untuk Timer/Counter 0 dan Timer/Counter 1 seperti terlihat dalam tabel.

Tabel 2.5. Mode Operasi Timer/Counter 0 dan 1[3]

Mode	Timer/Counter 0	Timer/Counter 1
0	13-bit Timer	13-bit Timer
1	16-bit Timer	16-bit Timer
2	8-bit auto-reload	8-bit auto-reload
3	Dua 8-bit Timer	Tidak bekerja

Pada mikrokontroler terdapat tambahan Timer 2. Timer yang lain adalah Timer 0 dan Timer 1. Timer 2 ini merupakan Timer/Counter 16-bit dan memiliki 3 mode operasi yaitu *capture, auto-reload* (*up-down counting*) dan *baund rate generator*. Untuk memilih mode ini dilakukan dengan mengatur bit pada SFR T2CON (Timer 2 Control Register). Timer 2 ini terdiri dari 2 buah Timer 8-bit register yaitu TH2 dan TL2. Pada fungsi Timer, register TL2 dinaikkan (*increament*) tiap siklus mesin. Karena siklus mesin terdiri dari 12 periode osilasi, maka *count rate* menjadi 1/12 dari frekuensi osilator. Sedangkan pada fungsi Counter, register dinaikkan berdasarkan tanggapan adanya transisi tinggi ke rendah pada pin yang bersesuaian (dalam hal ini pin T2 atau P1.0). Tabel berikut menunjukkan mode operasi yang dapat dijalankan pada Timer 2.

Tabel 2.6. Mode Operasi Timer 2[1]

RCLK + TCLK	CP/RL2	TR2	MODE
0	0	1	16-bit auto-reload
0	1	1	16-bit capture
1	X	1	Baund Rate Generator
X	X	0	Off

Keterangan[1] :

RCLK = *Receive Clock Enable*. Jika dieset menyebabkan serial port menggunakan pulsa *overflow* Timer 2 sebagai detak penerimaan pada serial port. Jika RCLK = 0, maka Timer 1 yang digunakan

TCLK = *Transmit Clock Enable*. Jika diset menyebabkan serial port menggunakan pulsa overflow Timer 2 sebagai detak pengiriman. Jika TCLK = 0, maka pulsa *overflow* Timer 1 yang digunakan

CP/RL2 = Pemilihan *Capture/Reload*. Jika diset maka proses *capture* yang terjadi sedangkan jika bit ini diclear maka proses *reload*

2.1.7. Sistem Interrupt

AT89S8252 memiliki 6 buah sumber interupsi, 2 eksternal interupsi (INT0 dan INT1), 3 Timer interupsi (Timer 0,1 dan 2) dan satu serial port interupsi.

INT0 = interrupt pada P3.2 (kaki 12)

INT1 = interrupt pada P3.3 (kaki 13)

Timer 0 = Timer pada P3.4 (kaki 14)

Timer 1 = Timer pada P3.5 (kaki15)

Port serial = jika pengiriman/penerimaan suatu frame telah lengkap

Saat terjadinya interupsi, mikrokontroler secara otomatis akan menuju *subroutine* pada alamat tersebut. Setelah interupsi servis selesai dikerjakan, mikrokontroler akan mengerjakan program semula. Dua sumber eksternal adalah INT0 dan INT1, kedua interupsi eksternal akan aktif, transisi tergantung isi IT0 dan IT1 pada register TCON. Interrupt T0 dan T1 aktif pada saat Timer yang sesuai mengalami *roll over*. Interupsi serial akan dibangkitkan dengan melakukan operasi OR pada R1 dan T1 tiap-tiap sumber interupsi dapat *enable* atau *disable* secara *software*. Tingkat prioritas semua sumber interupsi dapat diprogram sendiri-sendiri dengan set atau *clear bit* pada SFR IP (*interrupt priority*). Register

yang akan berperan dalam mengatur aktif tidaknya interupsi adalah Interrupt Enable Register.

2.1.8. Reset

Rangkaian power on reset diperlukan untuk mereset mikrokontroler secara otomatis setiap catu daya. Ketika catu daya diaktifkan, rangkaian reset menahan logika tinggi pin RST dengan jangka waktu yang ditentukan oleh besarnya pengisian muatan C.

2.2. LCD (*Liquid Crystal Display*)

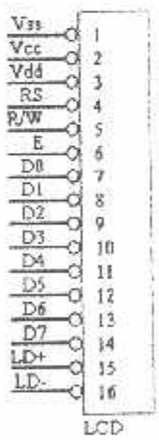
Liquid Crystal Display atau LCD merupakan komponen optoelektronik yaitu komponen yang bekerja atau dipengaruhi oleh sinar (optolistrik), komponen pembangkit cahaya (light emiting) dan komponen-komponen yang akan mengubah sinar. LCD terbuat dari bahan kristal cair yang merupakan suatu komponen organik dan mempunyai sifat optik seperti benda padat meskipun bahan tetap cair.

Sel kristal cair terdiri dari selapis bahan kristal cair yang diapit antara dua kaca tipis yang transparan. Antara dua lembar kaca tersebut diberi bahan kristal cair (*liquid crystal)* yang tembus cahaya. Permukaan luar dari masing-masing keping kaca mempunyai lapisan penghantar tembus cahaya seperti oxida timah (*tin oxide)* atau oxida indium (*indium oxide)*. Sel mempunyai ketebalan sekitar 1×10^{-5} meter dan diisi dengan kristal cair.

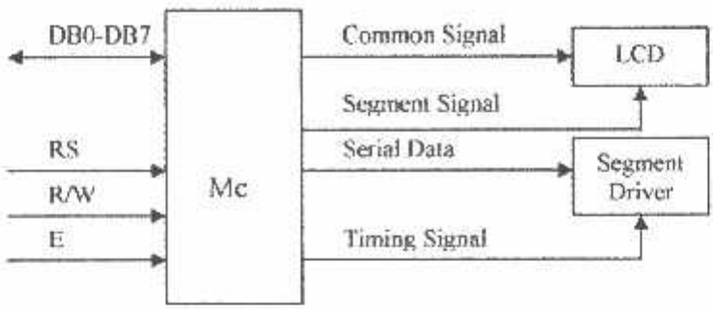
Karena sel-sel kristal cair merefleksikan cahaya dan bukan membangkitkan cahaya maka konsumsi daya yang dibutuhkan relatif rendah.

Energi yang dipergunakan hanya untuk mengaktifkan kristal cair. Pada dasarnya LCD bekerja pada tegangan rendah (3 – 15 Vrms), frekuensi rendah (25 – 60 Hz) sinyal AC dan memakai arus listrik yang sangat kecil (25 - 300 μA). LCD seringkali ditata sebagai tampilan *seven segment* untuk menampilkan angka tetapi juga memiliki keistimewaan lain, yaitu kemampuan untuk menampilkan karakter dan berbagai macam simbol.

Salah satu jenis LCD diantaranya adalah LCD M1632, suatu jenis piranti dengan konsumsi daya yang rendah, disusun dari dot matrik dan dikontrol oleh ROM atau RAM generator karakter dan RAM data display. Pengontrolan utamanya adalah pada ROM generator dan display data RAM yang menghasilkan kode ASCII jika padanya diberikan input ASCII. Untuk dapat difungsikan dengan baik maka perlu diperhatikan proses analisasi yang telah ditentukan oleh pabrik pembuatnya. Timing penganalisasian sangat dipertimbangkan, karena jika meleset sampai ordo *milisecon* maka dapat dipastikan LCD tidak dapat berfungsi.



Gambar 2.7. Konfigurasi Kaki LCD [4]



Gambar 2.8. Blok Diagram LCD [4]

Adapun karakteristik dari LCD M1632 antara lain :

- Dengan 16 karakter – 2 baris dalam bentuk dotmatrik 5x7 dan cursor
- *Duty ratio* 1/16
- Memiliki ROM pembangkitan karakter untuk 192 jenis karakter
- RAM untuk data display sebanyak 80x8 bit
- Dapat dirangkai dengan MPU 8 bit/4 bit
- RAM data display dan RAM pembangkit karakter dapat dibaca oleh MPU
- Memiliki fungsi instruksi antara lain *display on/off, Cursor on/off, display* karakter *blink, cursor shift* dan *display shift*
- Memiliki rangkaian osilator sendiri
- Catu tegangan tunggal yaitu ± 5 V
- Memiliki rangkaian reset otomatis pada catu daya yang dihidupkan
- Temperatur operasi 0^0 - 50^0

LCD memiliki 16 pin yang masing-masing mempunyai fungsi sebagai berikut :

Tabel 2.7. Fungsi Tiap Pin LCD[4]

No. Pin	Simbol	Level	Fungsi	
1	V_{SS}	-	Power Supply	0 V (GND)
2	V_{CC}	-		5 V ± 10%
3	V_{DD}	-		For LCD Drive
4	RS	H/L	Sinyal seleksi register H ; Data Input [register data (write/read)] L ; Instruction Input [register instruksi (write), busy flag dan address counter (read)]	
5	R/W	H/L	H ; Read L ; Write	
6	E	H	Enable Signal [sinyal penanda mulai operasi, aktif saat operasi write atau read]	
7	DB0	H/L	4 bit bus data lower 2 arah, dapat dibaca atau ditulis terhadap mikrokontroler	
8	DB1	H/L		
9	DB2	H/L		
10	DB3	H/L		
11	DB4	H/L	4 bit bus data upper 2 arah, dapat dibaca atau ditulis terhadap mikrokontroler. DB7 juga sebagai busy flag	
12	DB5	H/L		
13	DB6	H/L		
14	DB7	H/L		
15	V+BL	-	Back Light Supply	4 - 4,2 V 50 – 200 mA
16	V-BL	-		0 V (GND)

2.2.1. Instruksi Operasi

Tabel 2.8. Instruksi Pada LCD [4]

Instruksi	RS	RW	D7	D6	D5	D4	D3	D2	D1	D0
Display Clear	0	0	0	0	0	0	0	0	0	1
Cursor Home	0	0	0	0	0	0	0	0	1	*
Entry Mode Set	0	0	0	0	0	0	0	1	I/D	S
Display On/Off	0	0	0	0	0	0	1	D	C	B
Cursor Display Shift	0	0	0	0	0	1	S/C	R/L	*	*
Function Set	0	0	0	0	1	DL	1	*	*	*
CG RAM Address Set	0	0	0	1	A_{CG}					
DD RAM Address Set	0	0	1	A_{DD}						
BF/Address Read	0	1	BF	AC						
Data Write to CG RAM	1	0	Write Data							
Data Read from CG RAM	1	1	Read Data							

*Invalid Bit
A_{CG} ; CG RAM Address
A_{DD} ; DD RAM Address

2.2.2. Operasi Dasar

- Register

  Kontrol dari LCD memiliki 2 buah register 8 bit yaitu register instruksi (IR) dan register data (DR). IR memiliki instruksi seperti display, clear, cursor shift dan display data (DD RAM) serta karakter (CG RAM). DR menyimpan data untuk ditulis ke DD RAM ataupun membaca data dari DD RAM dan CG RAM. Ketika data ditulis ke DD RAM atau CG RAM maka DR secara otomatis menulis data ke DD RAM atau CG RAM. Ketika data pada CG RAM atau DD RAM akan dibaca maka alamat data ditulis pada IR. Sedangkan data akan dimasukkan melalui DR sehingga dapat dibaca oleh mikrokontroler.

Tabel 2.9. Pemilihan Register Pada LCD [4]

RS	RW	Operasi
0	0	Seleksi IR, IR Write Display Clear
0	1	Busy Flag (DB7), @ Counter (DB0-DB7) Read
1	0	Seleksi DR, DR Write
1	1	Seleksi DR, DR Read

- Busy Flag

  Busy Flag menunjukkan bahwa modul siap untuk menerima instruksi selanjutnya sebagaimana terlihat pada tabel diatas. Register seleksi sinyal akan melalui DB7 jika RS=0 dan R/W=1. Jika bernilai 1 maka sedang melakukan kerja internal dan instruksi tidak akan dapat diterima, oleh karena itu status dari flag harus diperiksa sebelum melaksanakan instruksi selanjutnya.

- Address Counter (AC)

  AC menunjukkan lokasi memori dalam modul LCD. Pemilihan lokasi alamat lewat Ac diberikan lewat register instruksi (IR) ketika data pada A, maka AC secara otomatis menaikkan atau menurunkan alamat tergantung dari Entry Mode Set.

- Display Data RAM

  Pada LCD, masing-masing line memiliki range alamat tersendiri. Alamat itu diekspresikan dengan bilangan hexadesimal. Untuk line 1 range alamat berkisar antara 40_H-$4F_H$.

- Character Generator ROM (CG ROM)

  CG ROM memiliki tipe dot matrik 5x7, dimana pada LCD telah tersedian ROM sebagai pembangkit karakter dalam kode ASCII.

- Character Generator RAM (CG RAM)

  CG RAM dipakai untuk pembuatan karakter tersendiri melalui program.

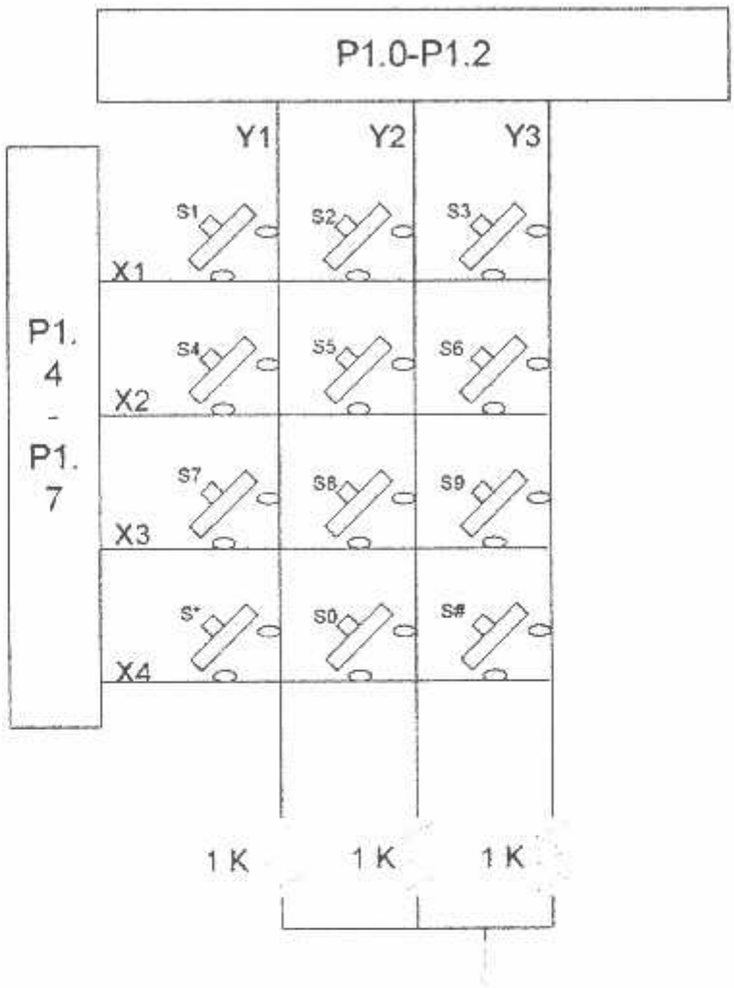
  Adapun bentuk fsik dari LCD M1632 adalah pada gambar berikut :

Gambar 2.9. Liquid Crystal Display [4]

2.3. Papan Tombol (*Keypad*)

Papan tombol ini digunakan untuk memasukkan data referensi dan mengubah data bila diinginkan. Untuk menterjemahkan informasi yang diterima dari papan tombol, maka *keypad* dihubungkan dengan *port* 1.

Papan tombol tersebut mempunyai matrik 4 baris dan 3 kolom. Deretan baris dan kolom dari papan tombol dihubungkan dengan *port* 1 yang difungsikan sebagai masukan dan keluaran. Deretan kolom dihubungkan dengan *ground* (berlogika 0) dan *port* 1 (P1.0-P1.2) yang difungsikan sebagai *input* mikrokontroler. Sedangkan deretan baris dihubungkan ke *port* 1 (P1.4-P1.7) yang telah diberi data 0001 dan secara kontinyu data tersebut bergeser satu bit ke kiri. Pergeseran data satu bit ini dimaksudkan untuk menentukan posisi tombol yang ditekan dalam satu kolom. *Port* ini difungsikan sebagai *output* dari mikrokontroler. Dengan demikian kalau tombol tidak ditekan maka masukan *port* 1 (P1.0-P1.2) di pin yang terhubung tombol tersebut berlogika 0 dan bila tombol ditekan akan berlogika 1. Rangkaian papan tombol tersebut dapat dilihat dalam Gambar 2.10.

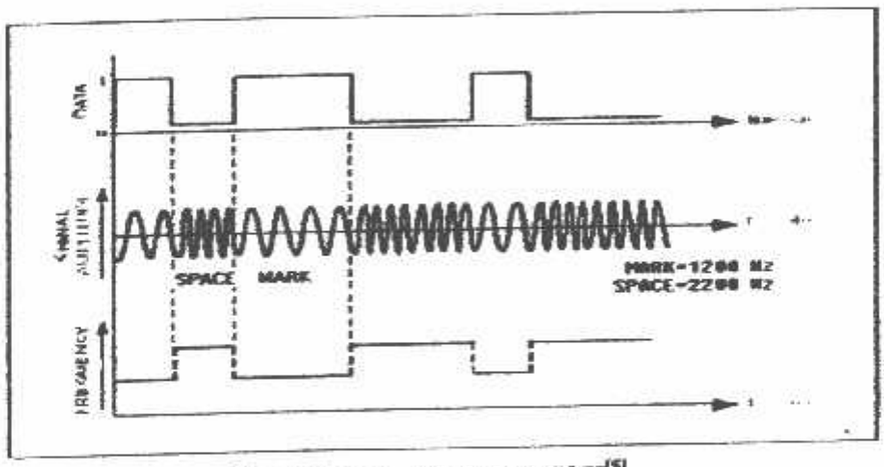


Gambar 2.10. Rangkaian *Keypad*

2.4. Modulasi FSK

Modulasi merupakan proses pengubahan informasi menjadi bentuk yang sesuai dengan media transmisi. Modulasi FSK (*frequency shift keying*) merupakan teknik modulasi yang biasa digunakan untuk mengirim informasi digital melalui jalur analog.

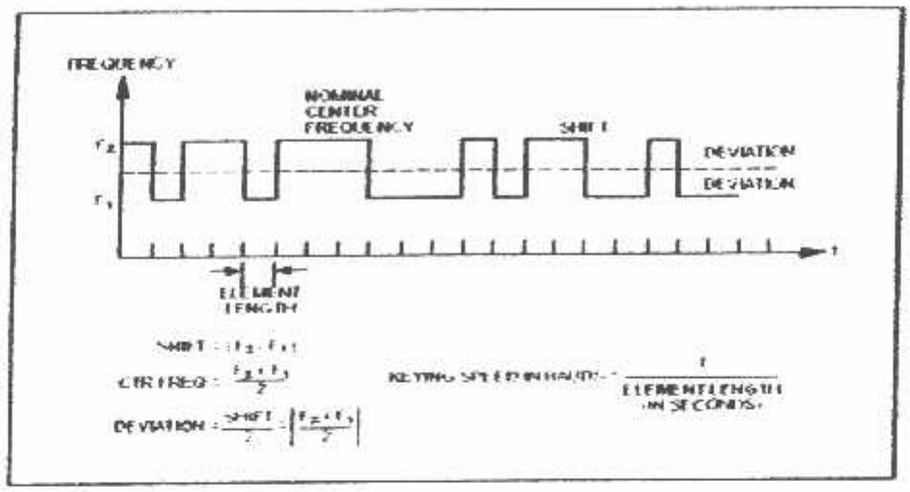
Modulasi FSK (*frequency shift keying*) menyatakan sinyal digital '1' sebagai nilai tegangan dengan frekuensi tertentu misalnya : 1200 Hz sementara sinyal digital '0' dinyatakan sebagai suatu nilai tegangan dengan frekuensi tertentu yang berbeda misalnya : 2200 Hz.



Gambar 2.11. Modulasi FSK[5]

Frekuensi mark dan frekuensi space mengarah kepada nilai logika biner '1' dan logika biner '0'. Gambar 2.11. menunjukkan hubungan antara data dan sinyal yang dikirimkan.

Sejumlah istilah yang sering digunakan dalam mendeskripsikan sinyal FSK, diperlihatkan pada gambar berikut :



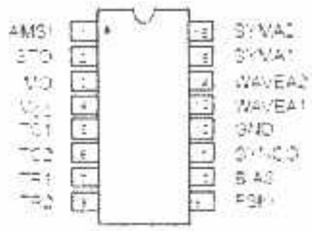
Gambar 2.12. Komponen Modulasi FSK[5]

Durasi kecil dari Mark atau Space disebut sebagai *element length*. Frekuensi yang diukur dari sebuah sinyal FSK adalah "shift" dan "center frequency". Shift adalah perbedaan frekuensi antara frekuensi mark dan frekuensi space, shift atau pergeseran biasanya berada pada jangkauan 50 Hz sampai 1000 Hz. Sedangkan nilai nominal dari "center frequency" adalah setengah dari frekuensi mark dan frekuensi space.

2.4.1. Modulator FSK XR 2206

XR 2206 adalah suatu *function generator* berbentuk rangkaian terintegrasi yang mampu dalam memproduksi gelombang sinus, square, triangle, ramp dengan stabilitas dan keakurasian tinggi. Frekuensi operasi dapat dipilih secara eksternal dalam jangkauan 0.01 Hz sampai lebih dari 1 MHz.

Rangkaian ini dapat digunakan sebagai aplikasi komunikasi, instrumentasi yang membutuhkan gelombang sinusoida, AM, FM, atau generator FSK.

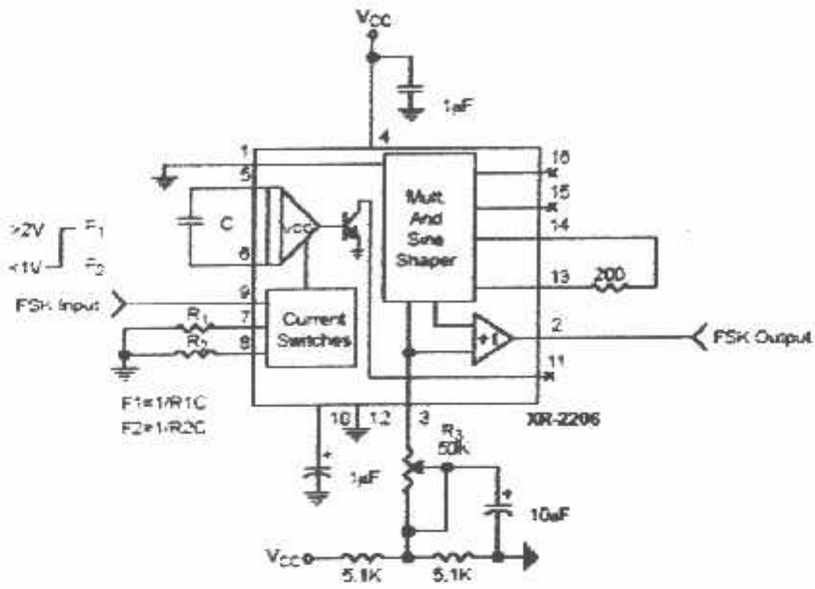


Gambar 2.13. Konfigurasi Pin XR 2206[6]

Dalam XR 2206 terdapat VCO (*voltage controlled oscillator*) yang menghasilkan suatu frekuensi keluaran sebanding dengan arus masukan, yang diatur oleh resistor dari timing terminal ke ground. Dengan dua timing pin (TR1 dan TR2), dua frekuensi keluaran yang berbeda dapat dihasilkan untuk aplikasi generator FSK.

XR 2206 dapat dioperasikan dengan dua timing resistor terpisah, R1 dan R2 terhubung dengan timing pin 7 dan timing pin 8. bergantung pada polaritas dari sinyal logika pada pin 9, 9 (FSK input), hanya satu dari timing resistor yang diaktifkan. Jika pin 9 dalam keadaan tidak terhubung atau terhubung dengan tegangan 2V, maka timing resistor R1 menjadi aktif. Begitu pula apabila pin 9 terhubung dengan tegangan 1V maka timing resistor R2 yang aktif. Output frekuensi dapat dirubah diantara dua tingkat frekuensi yaitu F1 dan F2 yang mengikuti formula berikut :

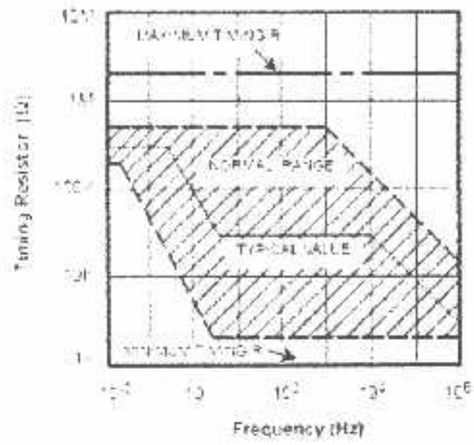
$F1 = 1/R_1C$ dan $F2 = 1/R_2C$



Gambar 2.14. Rangkaian FSK Generator dengan XR 2206[6]

Gambar 2.14. menunjukkan rangkaian generator FSK. Mark dan Space frekuensi dapat diatur secara terpisah dengan pemilihan nilai R1 dan R2. output frekuensi bersifat *phase continous* selama masa pergeseran dari mark ke space maupun sebaliknya.

Nilai R yang disarankan untuk berbagai tingkat frekuensi diperlihatkan pada gambar 2.15. Temperatur optimal yang stabil didapatkan diantara nilai resistor $4k\Omega<R<200k\Omega$. Nilai C yang disarankan adalah 1000 pF sampai 100 µF.



Gambar 2.15. Nilai R Yang Disarankan Untuk Berbagai Frekuensi[6]

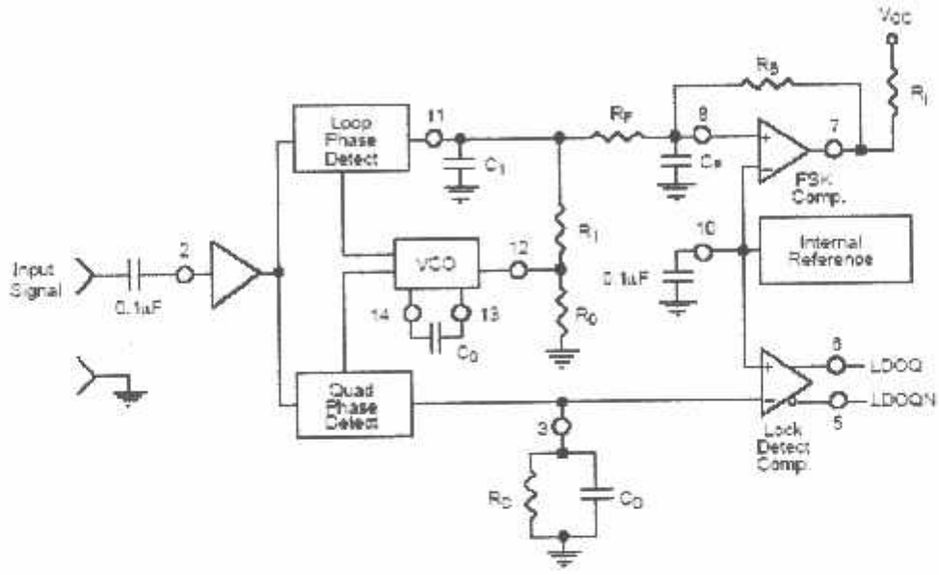
2.4.2. Demodulator FSK XR 2211

XR 2211 adalah monolithic PLL (*phase locked loop*) yang didesain untuk aplikasi komunikasi data, yang khususnya tepat digunakan pada aplikasi FSK modem.

Gambar 2.16. Konfigurasi Pin XR 2211[7]

Perangkat demodulator menggunakan IC Demodulator FSK XR 2211 dapat digunakan untuk beragam aplikasi decoding FSK dengan menentukan nilai dari lima komponen eksternalnya, yaitu : R_0, R_1, C_0, C_1, C_F. Komponen eksternal dipergunakan secara terpisah untuk menentukan center frequency, bandwidth dan output delay.

Mengacu pada gambar 2.17. dibawah, fungsi dari komponen eksternal ditentukan sebagai berikut, R_0 dan C_0 menentukan PLL center frequency, R_1 menentukan bandwidth sistem.



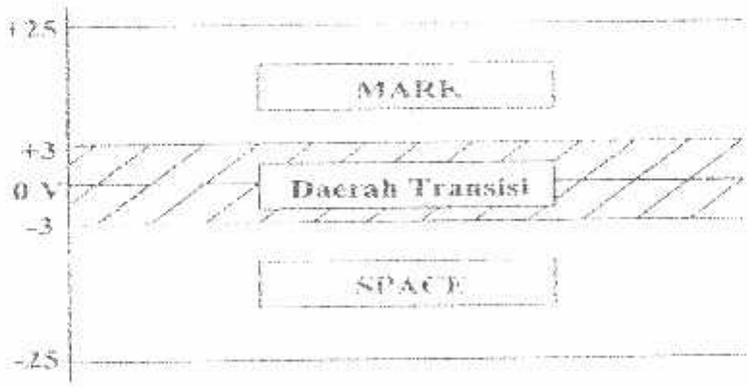
Gambar 2.17. Rangkaian Demodulator FSK XR 2211[7]

2.5. Perangkat Komunikasi Data

2.5.1. Serial Interface RS 232

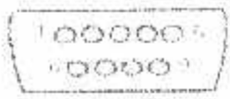
Interface EIA-232, atau yang juga dikenal sebagai RS-232. merupakan suatu interface yang menghubungkan antara terminal data dari suatu peralatan dan peralatan komunikasi data yang menjalankan suatu pertukaran data biner secara serial.

Karakteristik elektris yang dimiliki oleh EIA-232 menspesifikasikan tegangan positif antara +3 sampai +25 V. pada tegangan ini, isyarat dikenal sebagai biner 0 atau space. Sedangkan tegangan -3 sampai -25 V menyatakan biner 1 dan keadaan off atau Mark. Sedangkan tegangan antara -3 sampai dengan +3 disebut sebagai daerah transisi yang besaran tegangannya tidak berlaku atau *in valid*



Gambar 2.18. Karakteristik Elektris RS-232[8]

Berikut ini akan dibahas mengenai jenis sinyal dan konfigurasi pin RS-232. Spesifikasi mekanik untuk EIA-232 diilustrasikan pada gambar 2.19.



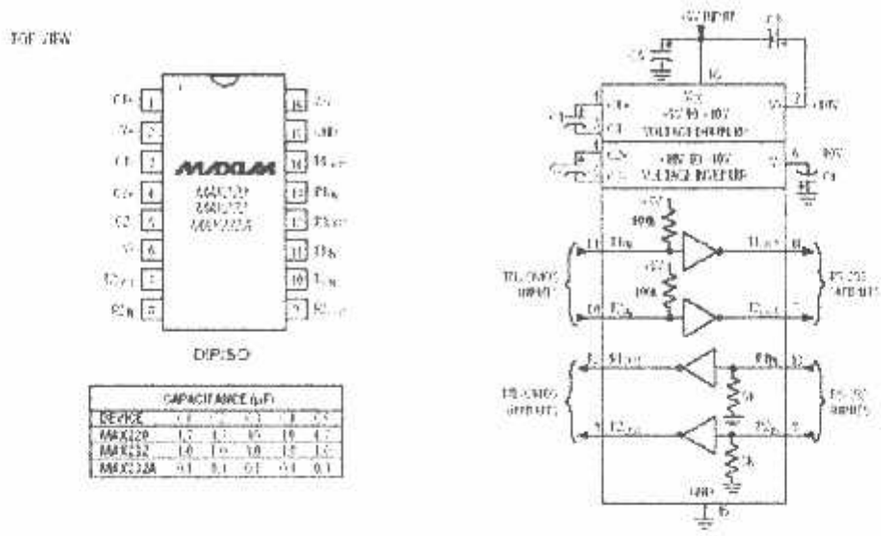
Gambar 2.19. Port RS-232 dengan DB-9 connector[9]

Tabel 2.10. Konfigurasi Pin dan Fungsi Pin RS-232 dengan DB-9 Connector

Pin	Nama	Arah	Fungsi
Pin 1	**CD** *Carrier Detect*	1	Mendeteksi sinyal adanya pembawa modem
Pin 2	**RD** *Receive Data*	1	Input data serial
Pin 3	**TD** *Transmit Data*	0	Output data serial
Pin 4	**DTR** *Data Terminal Ready*	0	Memberitahu modem bahwa UART siap digunakan
Pin 5	**SG** *Signal Ground*	-	Ground
Pin 6	**DSR** *Data Set Ready*		Membaca sinyal bahwa modem telah siap dipergunakan
Pin 7	**RTS** *Request To Send*	0	Mengindikasikan bahwa UART akan mengirim data
Pin 8	**CTS** *Clear To Send*	1	Membaca indikasi bahwa modem telah siap menerima data
Pin 9	**RI** *Ring Indikator*	1	Memberitahukan adanya sinyal dering pada modem

2.5.2. Max 232

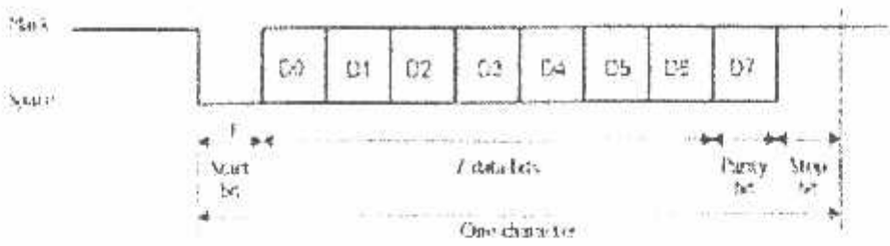
IC Max 232 ini adalah IC yang dirancang sebagai interface untuk merubah level tegangan RS-232 ke level tegangan TTL / CMOS sehingga bias dipakai untuk berkomunikasi dengan rangkaian digital dengan level tegangan 5 volt. Demikian juga sebaliknya IC ini juga bisa dipakai untuk merubah level tegangan TTL / CMOS ke level tegangan RS-232.



Gambar 2.20. IC Max 232[10]

2.6. Transmisi Data Asinkron

Salah satu pendekatan yang paling umum untuk mencapai sinkronisasi yang diharapkan adalah transmisi asynchronous. Strategi dalam skema ini adalah menghindari problem yang berkaitan dengan waktu dengan cara tidak mengirimkan deretan bit yang panjang dan tidak putus-putus. Jadi, data ditransmisikan satu karakter sekaligus, dimana setiap karakter panjangnya lima sampai delapan bit. Waktu atau sinkronisasi harus dipertahankan hanya didalam setiap karakter, receiver memiliki peluang melakukan sinkronisasi pada permulaan setiap karakter baru.



Gambar 2.21. Komponen Modulasi FSK[11]

Gambar 2.21. menunjukkan bentuk sinyal digital sebuah karakter data 7 bit. Dalam transmisi serial asinkron, clock dari transmitter dan receiver yang bertanggung jawab untuk membagi aliran data kedalam bit tidak disinkronkan. Output dari transmitter dalam keadaan mark logika 1 apabila data tidak dikirimkan.

Ketika transmitter akan mengirim sebuah karakter, jalur transmisi berubah menjadi logika 0 (space) selama satu periode bit yang disebut sebagai start bit, maka receiver menganggap sejumlah bit selanjutnya sebagai bit data.

Setelah jumlah bit data terpenuhi, selanjutnya diikuti dengan bit parity. Apabila receiver menemukan bahwa parity bit tidak sesuai dengan perhitungan, maka karakter tersebut akan ditolak. Parity bit digunakan sebagai error protection, sehingga tidak harus dikirimkan.


INSTITUT TEKNOLOGI NASIONAL
ITN
MALANG

BAB III

PERENCANAAN DAN PEMBUATAN ALAT

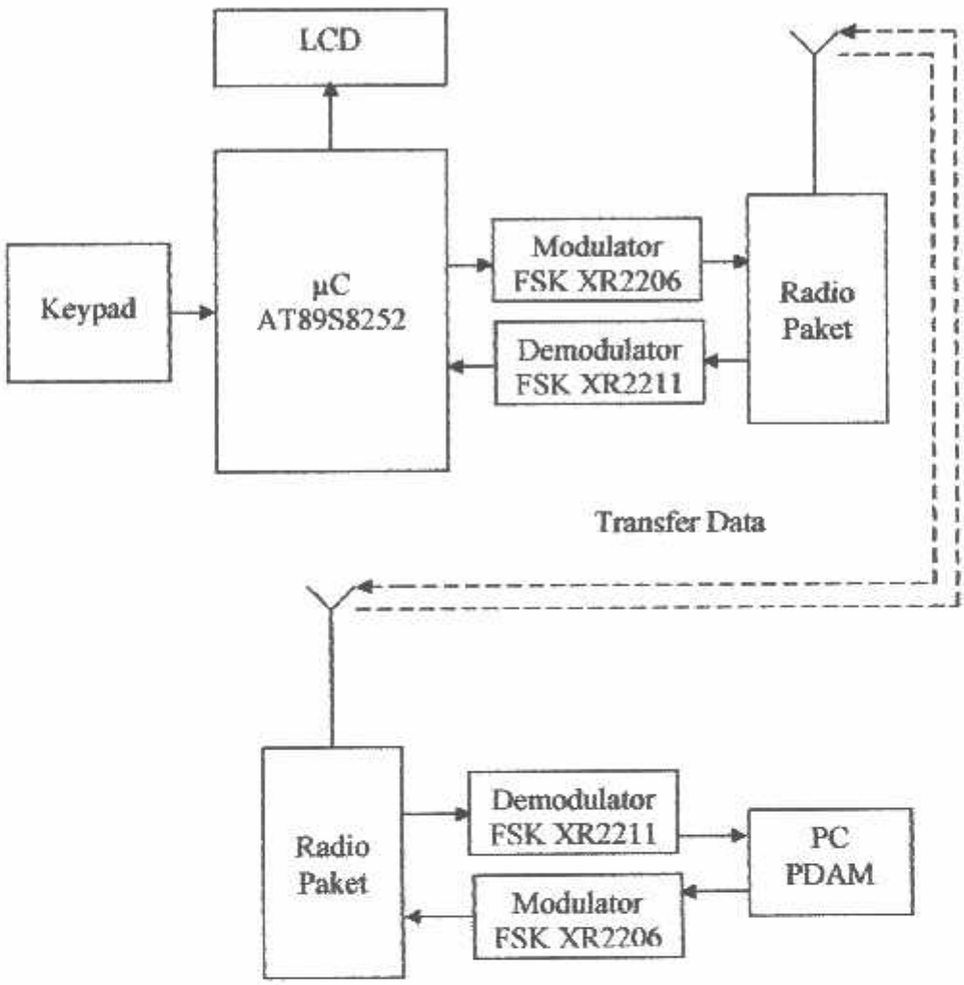
Dalam bab ini akan dijelaskan perencanaan dan pembuatan alat yang meliputi pembuatan perangkat keras dan perangkat lunak. Untuk memudahkan pemahaman pembuatan perangkat keras akan dimulai dengan menjelaskan secara blok diagram terlebih dahulu baru detail dari masing-masing peralatan.

3.1. Gambaran Umum Sistem.

Sistem yang dibuat adalah untuk diaplikasikan pada alat pencatat pemakaian air pelanggan PDAM agar petugas yang berada dilapangan bisa melakukan pekerjaan dengan mudah dimanapun dia berada asal masih dalam jangkauan radio komunikasi pada alat yang digunakan. Kemudian akan dikirimkan ke PC (*Personal Computer*) yang berada di kantor PDAM untuk proses pengolahan data.

3.2. Blok Diagram

Berikut ini adalah gambar blok perancangan sistem secara keseluruhan :



Gambar 3.1. Blok Diagram Sistem

Awalnya petugas melihat meteran pada kran PDAM yang berada di rumah-rumah pelanggan, kemudian dengan menggunakan keypad petugas memasukkan nomor pelanggan dan masukan juga digit-digit angka yang ada pada meteran air pelanggan, kemudian data yang masuk oleh mikrokontroller AT89S8252 disimpan di RAM pada mikrokontroller AT89S8252. Setelah pencatatan dari satu pelanggan selesai, kemudian data diteruskan ke modulator IC FSK XR2206 kemudian oleh FSK XR2206 data digital dirubah menjadi sinyal

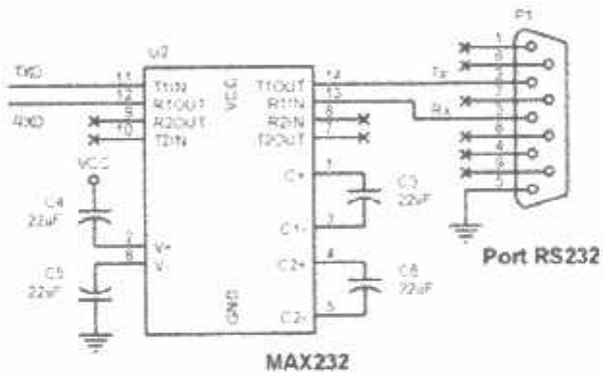
analog, setelah itu masuk ke dalam radio paket half duplex yang berfungsi sebagai pentransfer data dengan kecepatan pengiriman data 1200 bps, setelah data ditransfer, disisi penerima ada radio paket half duplex lagi yang berfungsi sebagai penerima kemudian diteruskan ke demodulator IC FSK XR2211 untuk dirubah dari sinyal analog menjadi data digital dan kemudian data masuk ke PC PDAM. Didalam PC PDAM data yang baru diterima kemudian diproses sehingga hasil dari pemprosesan data yaitu berupa nomor pelanggan dan biaya pelanggan pada bulan ini kemudian ditampilkan di LCD. Dari proses tersebut pelanggan akan mengerti berapa tagihan yang harus dibayar pada bulan ini.

Fungsi dari masing-masing blok adalah :

1. Minimum sistem AT89S8252 digunakan sebagai penyimpan data yang disimpan di RAM.
2. Keypad berfungsi untuk memasukkan data berupa : nomor pelanggan dan digit-digit angka yang ada pada meteran air yang berada di rumah pelanggan.
3. Tampilan LCD digunakan sebagai penampil informasi nomor pelanggan dan biaya yang harus dibayar pada tiap-tiap bulannya.
4. Modem atau modulator IC XR2206 dan demodulator IC XR2211 yaitu sebagai pengubah data digital ke frekuensi dan sebaliknya.
5. Radio paket half duplex digunakan sebagai pentransfer data yang berasal dari modulator dan demodulator.
6. PC PDAM merupakan alat yang digunakan sebagai tempat pemprosesan data.

3.3 Rangkaian Interface RS-232

Pada perencanaan hubungan antara komputer dengan modem adalah dipergunakan komunikasi data secara serial yaitu port 1 atau yang sering dikenal dengan COM 1. Adapun kaki atau pin-pin yang dipakai adalah pada pin nomor 2 yang berfungsi untuk sambungan *receive data*, pin nomor 3 untuk sambungan *transmit data* yang berguna sebagai input data pada modem FSK yang sebelumnya telah disesuaikan dulu level tegangannya dari RS-232 ke level tegangan TTL melalui sebuah IC MAX 232, dan pin nomor 5 untuk *signal ground*. Rangkaian interface RS-232 diperlihatkan pada gambar 3.2.



Gambar 3.2. Rangkaian Interface RS-232

Data biner yang berasal dari komputer mempunyai level tegangan antara +3V sampai +15V dan -3V sampai -15V, sebelum masuk pada rangkaian modulator demodulator terlebih dahulu tegangannya melalui sebuah IC MAX 232 dan diubah menjadi tegangan TTL sebesar 0V sampai 5V yang sesuai dengan tegangan untuk mencatu kerja rangkaian modulator demodulator tersebut.

3.4. Perencanaan Perangkat Keras Modulator Demodulator

Dalam perencanaan perangkat keras modulator demodulator atau yang sering dikenal dengan istilah modem ini dipergunakan suatu rangkaian dengan memakai komponen jenis FSK XR2206 untuk modulator dan FSK XR2211 untuk demodulator.

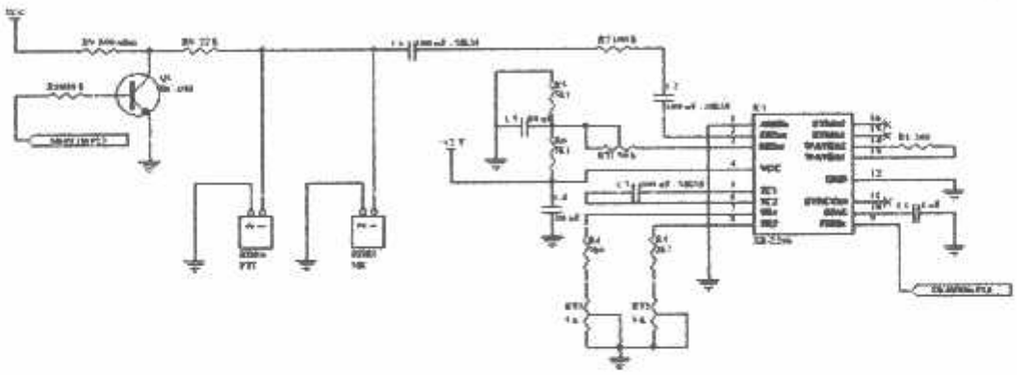
Untuk proses modulasi, data biner yang berasal dari komputer atau minimum sistem dimasukkan pada pin nomor 9 (*Data Input*) pada IC FSK XR2206, kemudian data tersebut dimudulasi, keluaran hasil modulasi yang berupa sinyal FSK dilewatkan pada pin nomor 2 (*FSK Output*). Keluaran sinyal FSK dari pin nomor 2 dihubungkan pada HT (*microphone*) untuk ditransmisikan melalui gelombang radio.

Untuk proses demodulasi berlaku sebaliknya, sinyal informasi yang berupa sinyal analog yang berasal dari HT (*speaker*) dihubungkan pada pin nomor 2 (*FSK Input*) di dalam IC FSK XR2211 yang berfungsi sebagai masukan demodulator. Setelah terjadi proses demodulasi keluaran sinyal dilewatkan pada pin nomor 7 (*Data Output*). Untuk dihubungkan pada komputer atau minimum sistem. Dari hasil demodulasi sinyal sudah berupa data biner.

3.4.1. FSK XR2206 (Modulator FSK)

Rangkaian untuk membangkitkan FSK (*FSK Generator*) ditunjukkan dalam gambar 3.3. FSK XR2206 dapat bekerja dengan dua buah *timing resistor* R_4 dan R_3 yang dihubungkan pada pin nomor 7 dan pin nomor 8, dan ditentukan oleh pemilihan kapasitor eksternal yang dihubungkan antara pin nomor 5 dan pin nomor 6. *Timing resistor* ini bekerja bergantian sesuai dengan level tegangan pada

pin nomor 9. jika pin nomor 9 diberi tegangan bias ≥ 2 V (logika 1), maka hanya R_4 yang bekerja. Sebaliknya jika pin nomor 9 diberi tegangan ≤ 1 V (logika 0), maka hanya R_3 yang bekerja. Sehingga frekuensi keluaran (pin no.2) berubah-ubah diantara dua frekuensi f1 dan f2. Besarnya f1 dan f2 dapat ditentukan dengan persamaan : $f1 = 1/R_1.C$, $f2 = 1/R_2.C$



Gambar 3.3. Rangkaian Modulator FSK XR2206

Frekuensi osilasi f_0, ditentukan oleh timing kapasitor yang terhubung dengan pin nomor 5 dan pin nomor 6 serta oleh timing resistor R_4 dan R_3 yang terhubung dengan pin nomor 7 dan pin nomor 8, dengan ketentuan

$$f_0 = 1/RC \text{ Hz}$$

Mempertimbangkan nilai R yang disarankan antara 4KΩ–200KΩ, diinginkan agar nilai timing resistor R_4 dan R_3 dengan frekuensi biner 1 (*mark*) pada $f_1 = 1200$ Hz dan frekuensi biner 0 (*space*) pada $f_2 = 2200$ Hz. Nilai kapasitor C diperoleh setelah memasukkan nilai-nilai variabel yang telah diketahui yaitu R_4, R_3, dan f, dengan mempertimbangkan nilai komponen kapasitor yang disarankan pada datasheet dan nilai komponen standar.

Adapun perhitungan untuk menentukan nilai komponen eksternal dari modulator FSK sebagai berikut :

Untuk nilai R_4 = 8,3 kΩ dan f1 = 1200 Hz

$$f_1 = \frac{1}{R_4.C}$$

$$C = \frac{1}{f1.R_4} = \frac{1}{1200.8{,}3k} = 1{,}004016064.10^{-7}\ \text{Farad} = 100\ \text{nF}$$

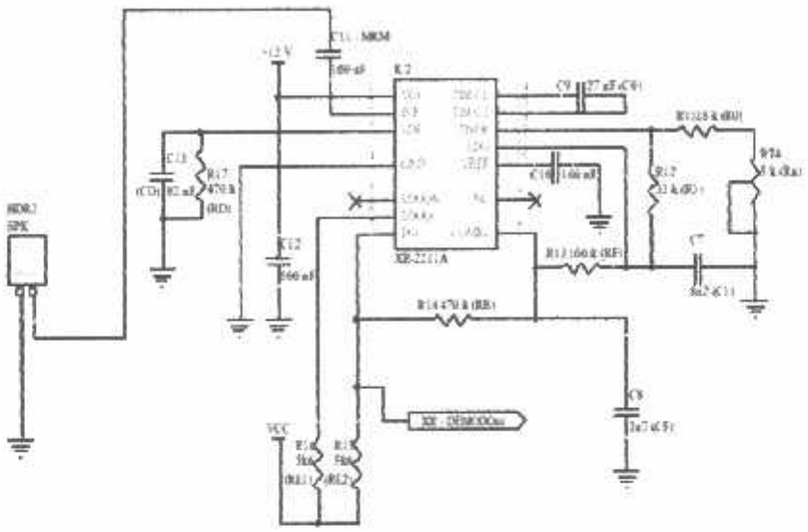
Setelah memperoleh komponen C dengan f_2 = 2200 Hz dapat menentukan nilai R_3 sebagai berikut :

$$R_3 = \frac{1}{f2.C} = \frac{1}{2200.100nF} = 4545{,}45\ \text{Ohm} \approx 5\ \text{kOhm}$$

Dari hasil perhitungan diatas, digunakan nilai timing kapasitor C sebesar 100 nF, karena merupakan nilai standart dan umum dipakai dipasaran. Sedangkan nilai R_4 dan R_3 yang berada pada jangkauan 4KΩ – 200KΩ digunakan komponen variabel resistor 5kΩ.

3.4.2. FSK XR2211 (Demodulator FSK)

Rangkaian demodulator berfungsi mengubah sinyal FSK yang diterima radio paket menjadi data biner. Untuk mendemodulasikan sinyal FSK tersebut digunakan IC FSK XR2211. FSK XR2211 adalah sebuah IC *monolithic phase locked loop* (PLL) yang dirancang untuk komunikasi data khususnya aplikasi modem FSK.



Gambar 3.4. Rangkaian Demodulator FSK XR2211

Demodulator FSK dirancang untuk mendemodulasi sinyal FSK dengan frekuensi biner 1 (*mark*) 1200 Hz dan biner 0 (*space*) 2200 Hz dengan kecepatan 1200 bps. Untuk mendemodulasi sinyal FSK dengan frekuensi tersebut maka pemilihan nilai-nilai komponen eksternal antara lain : R_0, R_1, C_0, C_1, C_F.

Penentuan nilai kelima komponen eksternal yaitu R_0, R_1, C_0, C_1, C_F. Untuk nilai f1 = 1200 Hz dan f2 = 2200 Hz dapat diperhitungkan mengacu pada desain instruksi perhitungan yang diberikan pada datasheet.

Adapun perhitungan untuk sistem demodulator yang akan dibuat dikemukakan dalam perhitungan sebagai berikut :

1. Menetukan PLL center frekuensi

$$f_0 = \sqrt{f1.f2} = \sqrt{1200.2200}$$

$$= 1624 \text{ Hz}$$

2. Menghitung timing resistor dengan Ro = 18k dan VR Rx = 5k

$$R_T = Ro + \frac{Rx}{2} = 18 + \frac{5}{2}$$

$$= 20{,}5 \text{ kOhm}$$

3. Menghitung nilai C_0

$$C_0 = \frac{1}{R_T . f_0} = \frac{1}{20{,}5k.1624}$$

$$= 30 \text{ nF} \approx 27 \text{ nF}$$

4. Menghitung nilai R1

$$R1 = \frac{18000.1624.2}{(2200-1200)}$$

$$= 58{,}484 \text{ Ohm}$$

$$\approx 33 \text{ kOhm}$$

5. menghitung nilai C1

$$C_1 = \frac{1250.Co}{R1.0{,}5^2} = \frac{1250.27nF}{33000.0{,}5^2}$$

$$= 4{,}09 \text{ nF} \approx 8{,}2 \text{ nF}$$

6. Menghitung nilai Rf (paling sedikit 5 kali nilai R1)

$$Rf = 33000 . 5 = 165000 \text{ Ohm}$$

$$= 165 \text{ kOhm} \approx 100 \text{ kOhm}$$

7. Menghitung nilai R_B (nilainya paling sedikit 5 kali nilai Rf)

$$R_B = 100000 . 5$$

$$= 500 \text{ kOhm} \approx 470 \text{ kOhm}$$

8. Menghitung Rsum

$$R_{SUM} = \frac{(Rf + Rl).Rb}{(Rf + Rl + Rb)}$$

$$= \frac{(100k + 33k)470k}{(100k + 33k + 470k)} = 103{,}665 \text{ kOhm}$$

9. Menghitung nilai C_F

$$C_F = \frac{0{,}25.}{(Rsum.Boudrate)}$$

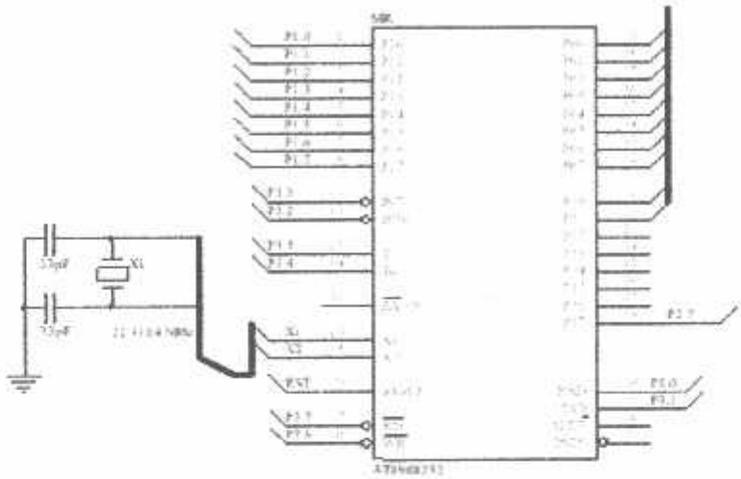
$$= \frac{0{,}25}{103665.1200} = 2 \text{ nF} \approx 2{,}7 \text{ nF}$$

3.4. Perancangan Sistem Mikrokontroller

Sistem mikrokontroller terdiri atas mikrokontroler dan komponen-komponen pendukung agar sistem dapat bekerja dengan optimal. Komponen pendukung pada perancangan sistem ini adalah RAM, PPI, latch dan dekoder.

3.5. Mikrokontroler AT89S8252

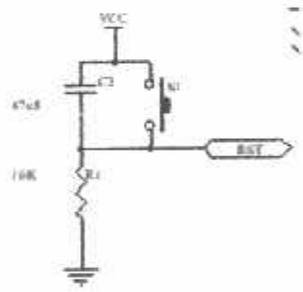
Mikrokontroller AT89S8252 harus didukung oleh beberapa rangkaian lain agar dapat melakukan prosesnya, yaitu berupa rangkaian clock dan reset. Selain itu juga harus ditentukan penggunaan port-portnya dan sinyal-sinyal yang digunakan untuk mendukung proses yang akan dilakukan.



Gambar 3.5. Rangkaian Osilator Internal

Mikrokontroller AT89S8252 memiliki rangkaian osilator internal yang dapat digunakan sebagai sumber clock bagi CPU. Osilator internal dirancang dengan dua buah kapasitor dan satu kristal, sesuai dengan spesifikasi AT89S8252. Gambar 3.5. menunjukkan rangkaian mikrokontroller dengan osilator internal.

- Rangkaan clock dan reset



Gambar 3.6. Rangkaian *Power-On Reset*

Rangkaian *power-on reset* dipergunakan untuk mereset mikrokontroller secara otomatis setiap awal catu daya dihidupkan. Saat catu daya diaktifkan, rangkaian reset akan menahan logika tinggi dari pin RST dengan jangka waktu

tertentu hingga kapasitor terisi muatan hingga jenuh. Saat kapasitor jenuh, pin RST akan berlogika rendah, dan mikrokontroller telah mengalami proses reset.

- Pembagian port

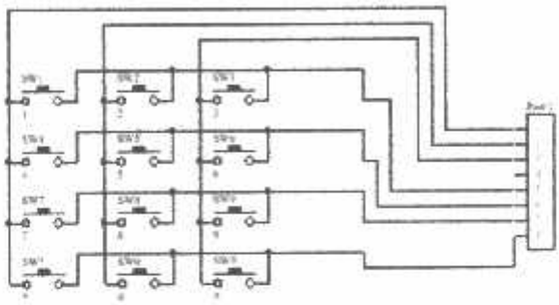
Dalam sistem mikrokontroller AT89S8252 ini direncanakan menggunakan port-port yang tersedia. Port 0 digunakan untuk saluran data ke LCD yaitu port P0.0-P0.7 dan P2.0 ; P2.1. Untuk port 1 digunakan sebagai inputan yang berasal dari keypad, port-port yang digunakan antara lain port P1.0-P1.2 sebagai kolom dan P1.4-P1.7 sebagai baris. Untuk port P3.0 (RXD) digunakan sebagai inputan ke FSK XR2206 dan untuk port P3.1 (TXD) juga digunakan sebagai inputan yaitu ke FSK XR2211.

3.6. Papan Tombol (*Keypad*)

Papan tombol ini digunakan untuk memasukkan data referensi dan mengubah data bila diinginkan. Untuk menterjemahkan informasi yang diterima dari papan tombol, maka *keypad* dihubungkan dengan *port* 1.

Papan tombol tersebut mempunyai matrik 4 baris dan 3 kolom. Deretan baris dan kolom dari papan tombol dihubungkan dengan *port* 1 yang difungsikan sebagai masukan dan keluaran. Deretan kolom dihubungkan dengan *ground* (berlogika 0) dan *port* 1 (P1.0-P1.2) yang difungsikan sebagai *input* mikrokontroller. Sedangkan deretan baris dihubungkan ke *port* 1 (P1.4-P1.7) yang telah diberi data 0001 dan secara kontinyu data tersebut bergeser satu bit ke kiri. Pergeseran data satu bit ini dimaksudkan untuk menentukan posisi tombol yang ditekan dalam satu kolom. *Port* ini difungsikan sebagai *output* dari mikrokontroller. Dengan demikian kalau tombol tidak ditekan maka masukan *port*

1 (P1.0-P1.2) di pin yang terhubung tombol tersebut berlogika 0 dan bila tombol ditekan akan berlogika 1. Rangkaian papan tombol tersebut dapat dilihat dalam Gambar 3.7.

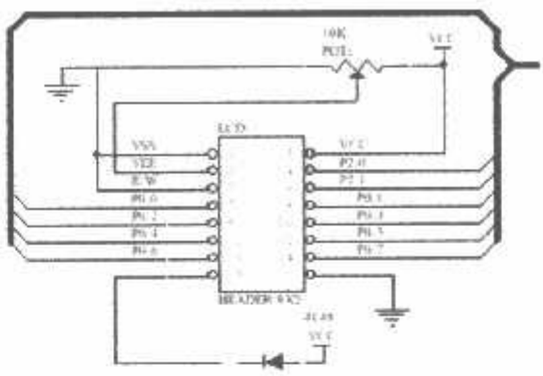


Gambar 3.7 Rangkaian *Keypad*

3.7. LCD

Pada sistem yang direncanakan akan digunakan LCD (*Liquid Crystal Display*) sebagai tampilan. LCD yang digunakan adalah jenis TM1632ABC yang merupakan LCD dua baris dengan tiap barisnya terdiri dari 16 karakter.

LCD ini membutuhkan 3 sinyal kontrol, R/W (*read/write*) untuk menentukan apakah data akan dibaca atau ditulis, E (*Enable*) yang merupakan sinyal untuk meng-enable-kan dan RS (*Register Select*) untuk memilih register yang diakses. LCD TM1632ABC memiliki 2 register yaitu register data dan register instruksi.

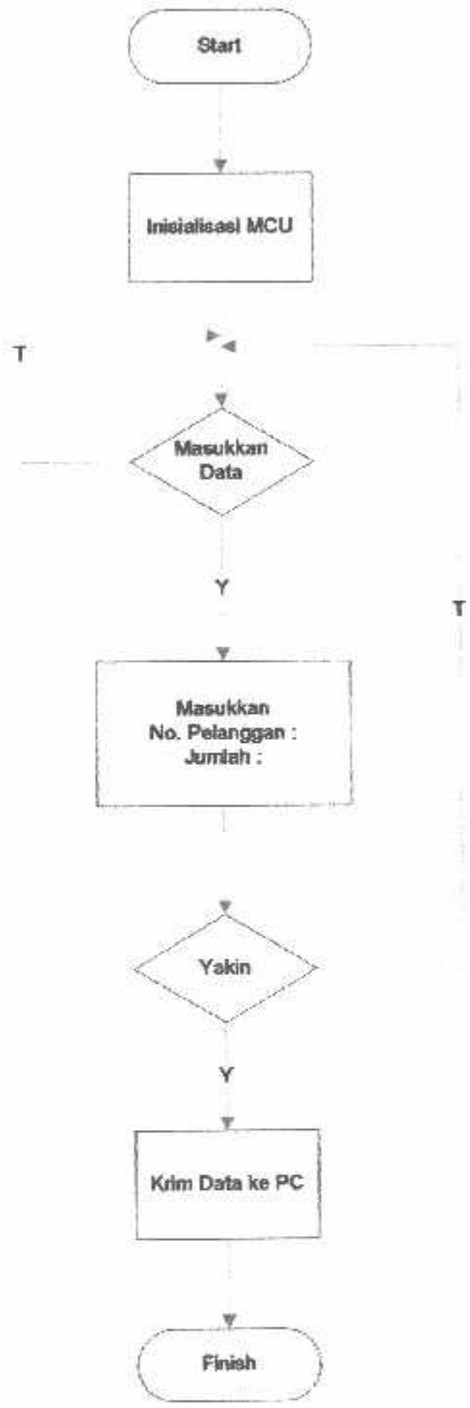


Gambar 3.8. Rangkaian LCD

3.8. Perancangan Perangkat Lunak

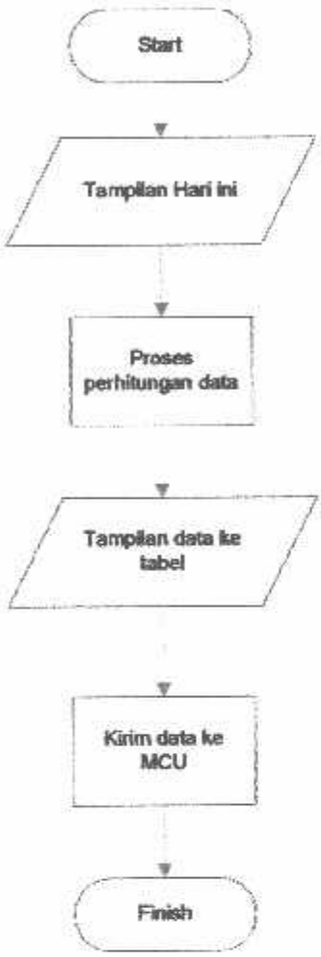
Karena digunakan komponen AT89S8252 sebagai CPU-nya maka program yang digunakan untuk mengontrol prosesnya menggunakan mnemonic mikrokontroller AT89S8252. Dan pada pengolahan data pada waktu pengambilan datanya diperlukan metode tertentu juga. Oleh karena itu diperlukan urutan-urutan kerja yang digambarkan pada flowchart berikut, sedangkan untuk bahasa pemrogramannya terletak dibagian lampiran.

- **Flowchart MCU**



Gambar 3.9. Flowchart MCU

- **Flowchart VB6**



Gambar 3.10. Flowchart VB 6

➢ **Hasil pengujian dan analisis**

Hasil pengujian dan pengamatan rangkaian *keypad* ditunjukkan dalam tabel 4.4. berikut :

Tabel 4.4. Hasil pengujian pengkode papan tombol (*keypad*)

Tombol	L_4	L_3	L_2	L_1	L_0
0	1	0	0	0	0
1	1	0	0	0	1
2	1	0	0	1	0
3	1	0	0	1	1
4	1	0	1	0	0
5	1	0	1	0	1
6	1	0	1	1	0
7	1	0	1	1	1
8	1	1	0	0	0
9	1	1	0	0	1
*	1	1	0	1	0
#	1	1	0	1	1

Berdasarkan hasil pengujian dapat dilihat bahwa L_4 yang dihubungkan ke pin *data available* berlogika high (ON) jika ada tombol ditekan, sedangkan L_3-L_0 menunjukkan data keluaran yang dihasilkan. Dengan demikian maka rangkaian pengkode papan tombol dapat bekerja dengan baik sesuai perencanaan.

4.6. Pengujian LCD

1. Tujuan

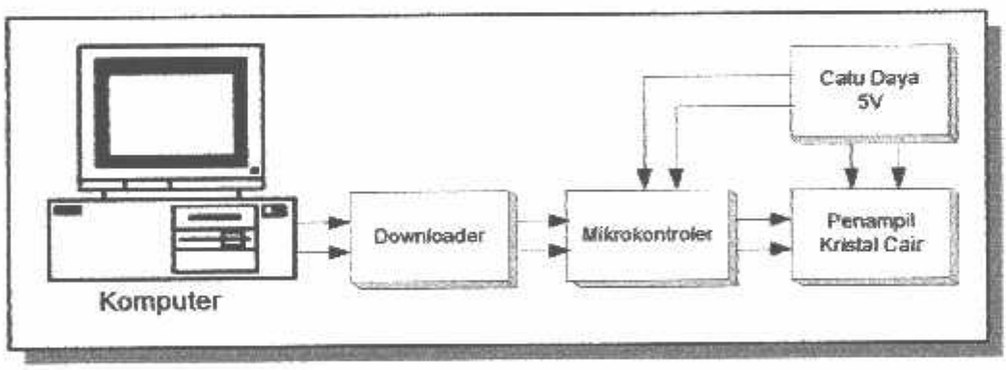
   Mengetahui apakah rangkaian LCD dapat menampilkan data karakter sesuai dengan yang dikirimkan oleh Downloader.

2. Peralatan yang digunakan

   - Downloader.
   - Komputer.
   - Minimum sistem mikrokontroller AT89S8252.
   - Catu daya 5V DC

3. Prosedur Pengujian

   - Merangkai peralatan seperti dalam Gambar 4.9.
   - Membuat perangkat lunak pengujian rangkaian LCD.
   - Mengaktifkan catu daya
   - Mengoperasikan program dengan bantuan Downloader. Hasil keluaran akan ditunjukkan pada layar penampil kristal cair.

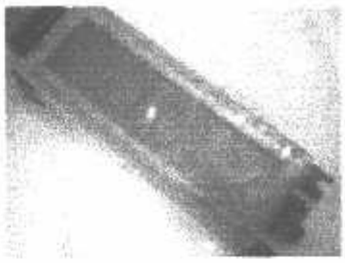


Gambar 4.9. Blok Pengujian LCD

4. Hasil Pengujian dan Analisis

   Dari hasil pengujian didapatkan bahwa rangkaian LCD dapat menampilkan karakter-karakter, sesuai dengan data yang dikirimkan oleh

mikrokontroller. Tampilan penampil kristal cair terdiri atas 2 baris yang masing-masing mempunyai 16 karakter.



Gambar 4.10. Hasil Pengujian LCD

4.7. Pengujian Secara Keseluruhan

Pengujian ini dapat dilakukan setelah semua tahap pengujian perbagian telah dilakukan dengan baik. Adapun prosedur pengujian secara keseluruhan dapat dijelaskan sebagai berikut :

1. Pasang semua piranti perangkat keras.
2. Nyalakan piranti pada bagian petugas yang berada dilapangan.
3. Masukan data-data yang diperlukan melalui keypad. Data meliputi nomor pelanggan dan digit-digit meteran pelanggan yang berada pada alat PDAM yang terpasang dirumah-rumah pelanggan.
4. Buka program aplikasi di komputer.
5. Lakukan setting pada port serial.
6. Ambil data
7. Simpan data.
8. Data diproses di komputer yang berada di kantor PDAM.

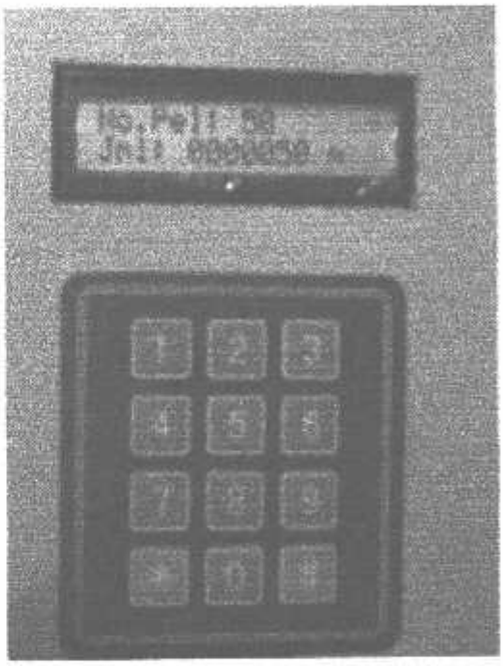
9. Data diterima oleh petugas yang berada dilapangan yaitu berupa nomor pelanggan dan biaya yang harus dibayar pelanggan pada bulan tersebut.

Jika semua langkah telah dilakukan dan tidak terdapat kesalahan maka pengujian secara keseluruhan telah dapat dilakukan dengan baik.

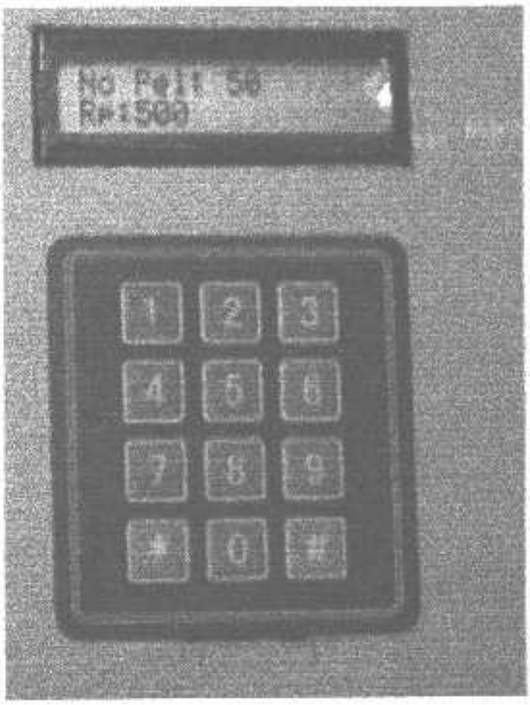
- **Berikut merupakan hasil pengujian alat secara keseluruhan yang penulis lakukan sebanyak 50 kali percobaan.**

1. Percobaan ke 50, Nomor pelanggan : 50

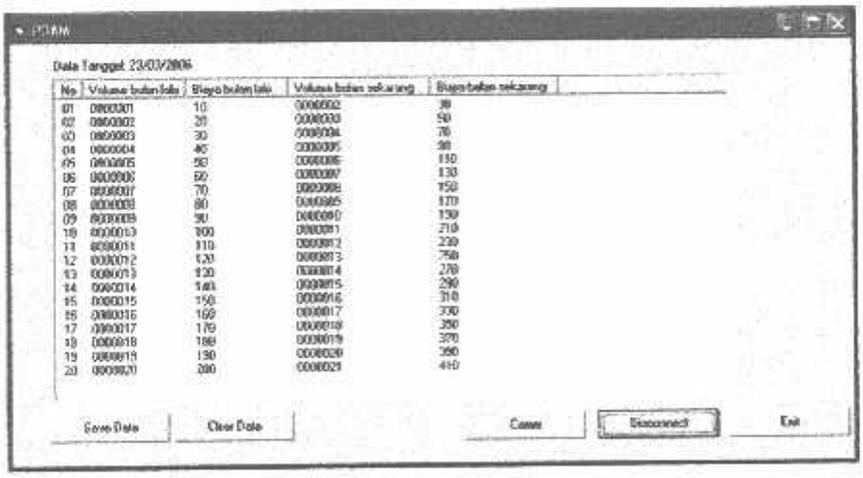
   Jumlah : 0000050 m^3

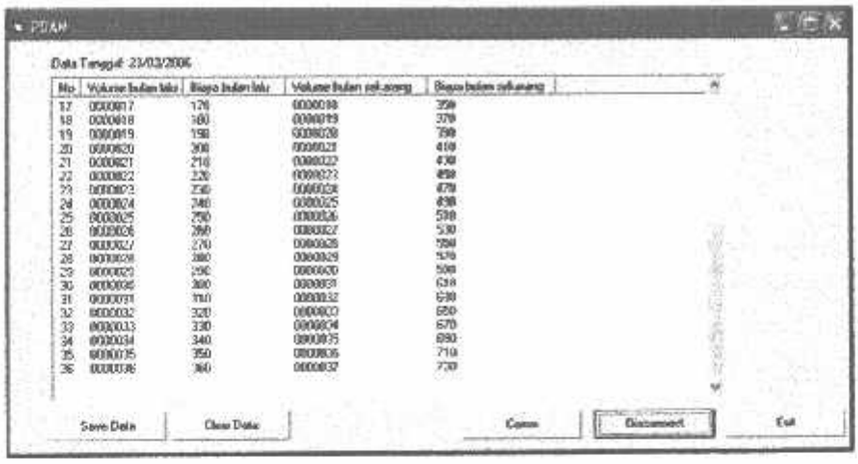


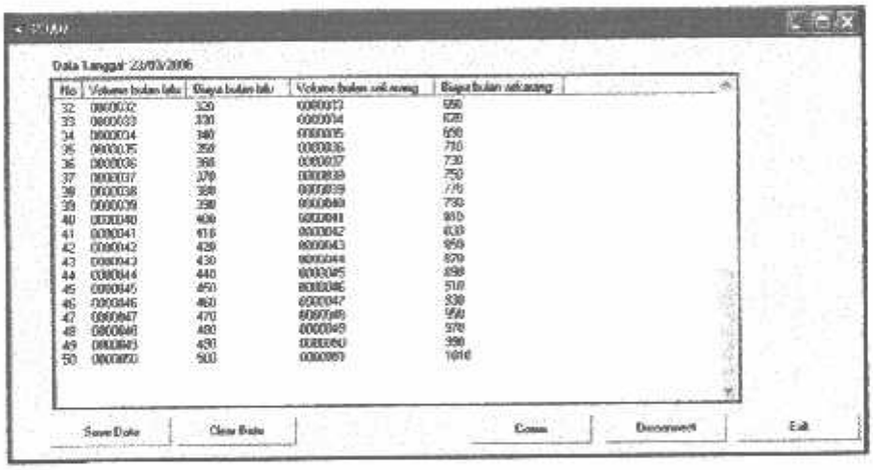
2. Berikut merupakan hasil data yang telah diproses oleh software visual Basic 6 dan diterima oleh petugas yang berada di lapangan :



3. Berikut merupakan data hasil percobaan yang penulis lalukan selama 50 kali, data ini merupakan data yang berada di Data Base VB 6 :







- **Analisa Hasil Pengujian**

Hasil pengujian diatas menunjukkan bahwa proses pengiriman data serial telah benar dan stabil. Oleh karena yang dikirim berupa data maka tidak boleh ada *error*, jadi data tersebut *valid*.

BAB V

PENUTUP

5.1. Kesimpulan

Berdasarkan analisis dan pengujian alat yang telah dilakukan maka didapatkan kesimpulan sebagai berikut :

1. Dari hasil pengujian mikrokontroller pada tabel 4.1. terlihat bahwa pada port 1 memberikan logika $0F_H$ dan $F0_H$ secara bergantian sesuai dengan isi program. Jadi mikrokontroller sudah berkerja dengan baik sesuai dengan perencanaan.
2. Dari hasil pengujian komunikasi serial pada table 4.2. menunjukkan bahwa proses pengiriman data serial dengan menggunakan RS-232 ke alat telah benar.
3. Dari hasil pengujian dalam Tabel 4.3. menunjukkan bahwa proses pengiriman data serial dari TX XR2206 ke RX XR2211 telah benar dan stabil.
4. Dari hasil pengujian dan pengamatan rangkaian *keypad* yang ditunjukkan pada tabel 4.4. maka rangkaian papan tombol dapat bekerja dengan baik sesuai dengan perencanaan.
5. Dari hasil pengujian LCD didapatkan bahwa rangkaian LCD dapat menampilkan karakter-karakter sesuai dengan data yang dikirimkan oleh mikrokontroller.

6. Dari hasil pengujian secara menyeluruh menunjukkan bahwa proses pengiriman data serial telah benar dan stabil. Oleh karena yang dikirim berupa data maka tidak boleh ada *error*, jadi data tersebut *valid* adanya.
7. Hasil pengujian secara menyeluruh menunjukkan bahwa proses pengiriman data serial telah benar dan stabil serta dapat menyimpan, menampilkan nomor pelanggan dan juga biaya yang harus dibayar oleh pelanggan ke kantor PDAM.

5.2. Saran-saran

Berdasarkan kesimpulan dari hasil analisis dan pengujian alat, maka penulis dapat memberikan saran sebagai berikut :

1. Karena proses transfer data menggunakan radio paket dan menggunakan antena pendek, maka dalam pengiriman datanya hanya terbatas pada jangkauan radio paket saja yaitu kurang lebih 500 m. Oleh karena itu diperlukan media lain agar pengiriman data dapat lebih jauh.
2. Karena alat ini merupakan simulasi, maka perlu adanya penyempurnaan pada perancangan software baik pada pemrograman perangkat keras maupun perangkat lunak. Hal ini dimaksudkan untuk lebih memberikan kepuasan kepada pelanggan PDAM.
3. Pada alat ini frekuensi yang digunakan merupakan frekuensi yang tidak sedang digunakan. Agar dalam proses transfer data tidak mengalami gangguan, maka perlu adanya frekuensi yang terdaftar atau *legal frequency* .

DAFTAR PUSTAKA

1. www.atmel.com, AT89S8252 datasheet archieves.
2. Andi Nalwan, Paulus, *Teknik Antarmuka dan Pemrograman AT89C51*, PT. Elekmedia Komputindo, Jakarta, 2003.
3. MCS-51 Microcontroller User's Manual.
4. Liquid Cristal Display Module M1632 User Manual.
5. FSK Signal and Demodulation, WJ Communication Inc.
6. XR2206 datasheet, Exar Corp.
7. XR2211 datasheet, Exar Corp.
8. Teguh Wahyono, *Prinsip Dasar Teknologi Komunikasi Data*, PT. Elekmedia Komputindo, Jakarta, 1996.
9. Interfacing The Serial RS232 Port, http:/www.senet.com.au.
10. Datasheet, http:/www.lookrs232.com.
11. Asyncronous Serial Transmission, http:/www.howstuffworks.com.

LAMPIRAN

INSTITUT TEKNOLOGI NASIONAL MALANG
FAKULTAS TEKNOLOGI INDUSTRI
JURUSAN TEKNIK ELEKTRO

FORMULIR BIMBINGAN SKRIPSI

Nama : DAVID AFIANTO
Nim : 0117054
Masa Bimbingan : 9 Desember 2005 – 9 Mei 2006
Judul Skripsi : PERANCANGAN DAN PEMBUATAN ALAT PENCATAT PEMAKAIAN AIR PELANGGAN PDAM DAN DITRANSMISIKAN MELALUI RADIO PAKET YANG DIHUBUNGKAN DENGAN PC PDAM BERBASIS MIKROKONTROLLER AT89S8252

No.	Tanggal	Uraian	Paraf Pembimbing
1.	25/11 06	Bab I	
2.	3/2 06	Bab II	
3.	26/2 06	Revisi	
4.	1/3 06	Bab IV	
5.	2/3 06	Bab V + Melabel Skripsi	
6.	15/3 06	Bab I – Bab V	
7.			
8.			
9.			
10.			

Malang,
Dosen Pembimbing

Ir. F. Yudi Limpraptono, MT
NIP. P. 1039500274

INSTITUT TEKNOLOGI NASIONAL MALANG
FAKULTAS TEKNOLOGI INDUSTRI
JURUSAN TEKNIK ELEKTRO

FORMULIR BIMBINGAN SKRIPSI

Nama : DAVID AFIANTO
Nim : 0117054
Masa Bimbingan : 9 Desember 2005 – 9 Mei 2006
Judul Skripsi : PERANCANGAN DAN PEMBUATAN ALAT PENCATAT PEMAKAIAN AIR PELANGGAN PDAM DAN DITRANSMISIKAN MELALUI RADIO PAKET YANG DIHUBUNGKAN DENGAN PC PDAM BERBASIS MIKROKONTROLLER AT89S8252

No.	Tanggal	Uraian	Paraf Pembimbing
1.	25/1 06	Bab I	
2.		Bab III revisi	
3		Bab II ok	
4.		Bab IV ok	
5.		Bab V + sequi nyuan	
6.		Seminar hasil	
7.		Kompre	
8.			
9.			
10.			

Malang,
Dosen Pembimbing

Ir. Mimien Mustikawati
NIP. P. 1030000352

INSTITUT TEKNOLOGI NASIONAL
FAKULTAS TEKNOLOGI INDUSTRI
JURUSAN TEKNIK ELEKTRO S-1
KONSENTRASI TEKNIK ELEKTRONIKA

LEMBAR BIMBINGAN SKRIPSI

Nama	: DAVID AFIANTO
NIM	: 01.17.054
Jurusan	: Teknik Elektro S-1
Konsentrasi	: Teknik Elektronika
Judul Skripsi	: Perancangan dan Pembuatan Alat Pencatat Pemakaian Air Pelanggan PDAM dan Ditransmisikan Melalui Radio Paket yang Dihubungkan dengan PC PDAM Berbasis Mikrokontroller AT89S8252
Mulai Bimbingan Skripsi	: 09 Desember 2005
Selesai Bimbingan Skripsi	: 09 Mei 2006
Dosen Pembimbing	: Ir. F. Yudi Limpraptono, MT. Pembimbing I
	: Ir. Mimien Mustikawati. Pembimbing II
Telah Dievaluasi Dengan Nilai	: 95

Diperiksa dan Disetujui,

Dosen Pembimbing I

(Ir. F. Yudi Limpraptono, MT)
NIP. Y. 1039500274

Dosen Pembimbing II

(Ir. Mimien Mustikawati)
NIP. P. 1030000352

Mengetahui,
Ketua Jurusan T. Elektro S-1

(Ir. F. Yudi Limpraptono, MT)
NIP. Y. 1039500274

INSTITUT TEKNOLOGI NASIONAL
FAKULTAS TEKNOLOGI INDUSTRI
JURUSAN TEKNIK ELEKTRO

Formulir Perbaikan Ujian Skripsi

Dalam pelaksanaan Ujian Skripsi Janjang Strata 1 Jurusan Teknik Elektro Konsentasi T. Energi Listrik / T. Elektronika, maka perlu adanya perbaikan skripsi untuk mahasiswa :

NAMA : Daud Afianto
N I M : 0117054
Perbaikan meliputi :

Penggujian.
Pembahasan.

Malang, 22 Maret 2006

(M. Ibrahim A, ST)

INSTITUT TEKNOLOGI NASIONAL
FAKULTAS TEKNOLOGI INDUSTRI
JURUSAN TEKNIK ELEKTRO S-1
KONSENTRASI TEKNIK ELEKTRONIKA

FORMULIR PERBAIKAN SKRIPSI

Nama : DAVID AFIANTO

NIM : 01.17.054

Masa Bimbingan : 09 Desember 2005 s/d 09 Mei 2006

Judul : Perancangan dan Pembuatan Alat Pencatat Pemakaian Air Pelanggan PDAM dan Ditransmisikan Melalui Radio Paket yang Dihubungkan dengan PC PDAM Berbasis Mikrokontroller AT89S8252

No	Tanggal	Uraian	Paraf
1	22 Maret 2006	- Perencanaan	
2	22 Maret 2006	- Pengujian	

Disetujui,

Penguji I

(M. Ibrahim Ashari, ST)
NIP. Y. 1030100358

Penguji II

(Irmalia Suryani. F, ST)
NIP. Y. 1030100365

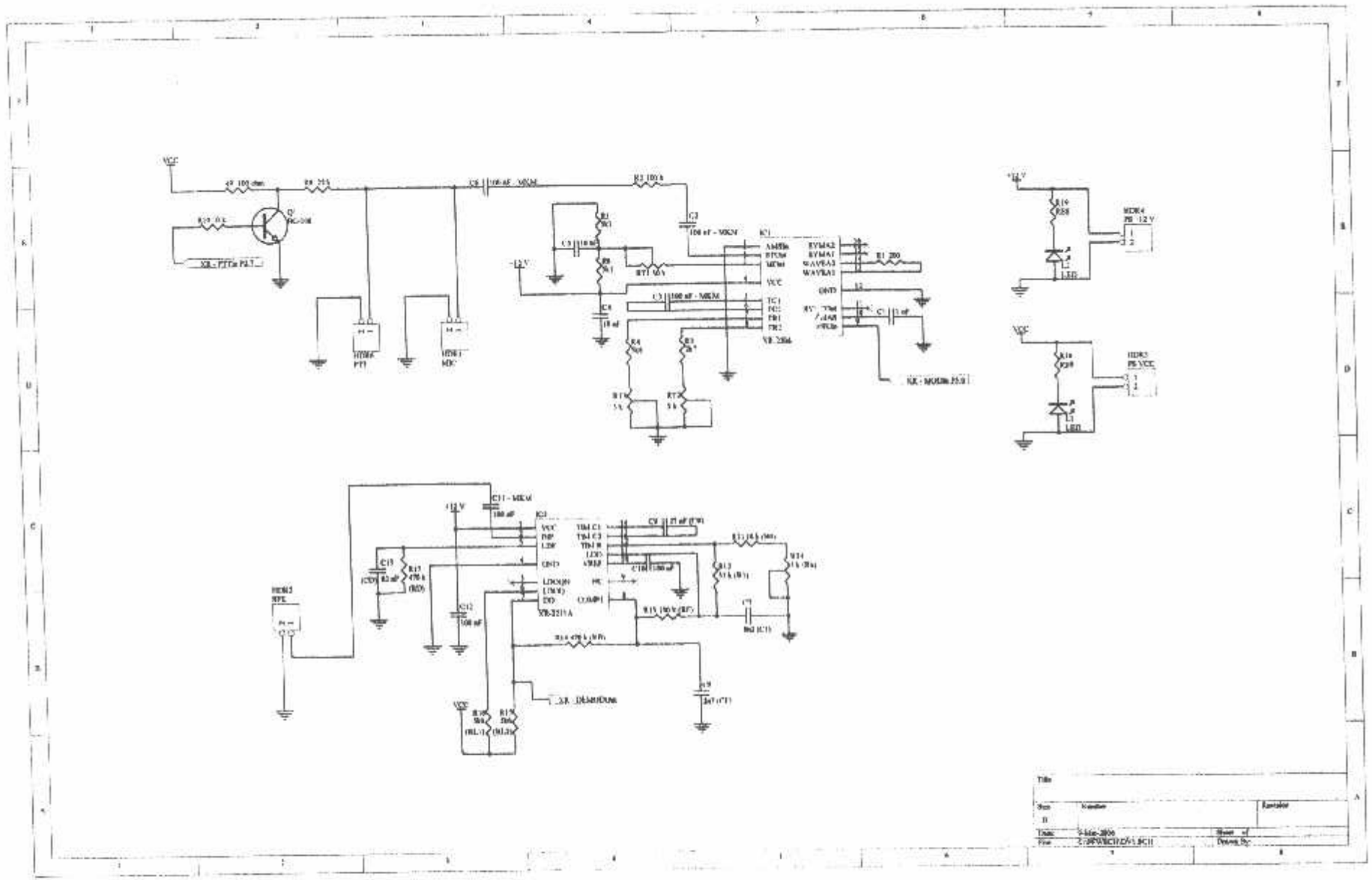
Mengetahui,

Dosen Pembimbing I

(Ir. F. Yudi Limpraptono, MT)
NIP. Y. 1039500274

Dosen Pembimbing II

(Ir. Mimien Mustikawati)
NIP. P. 1030000352



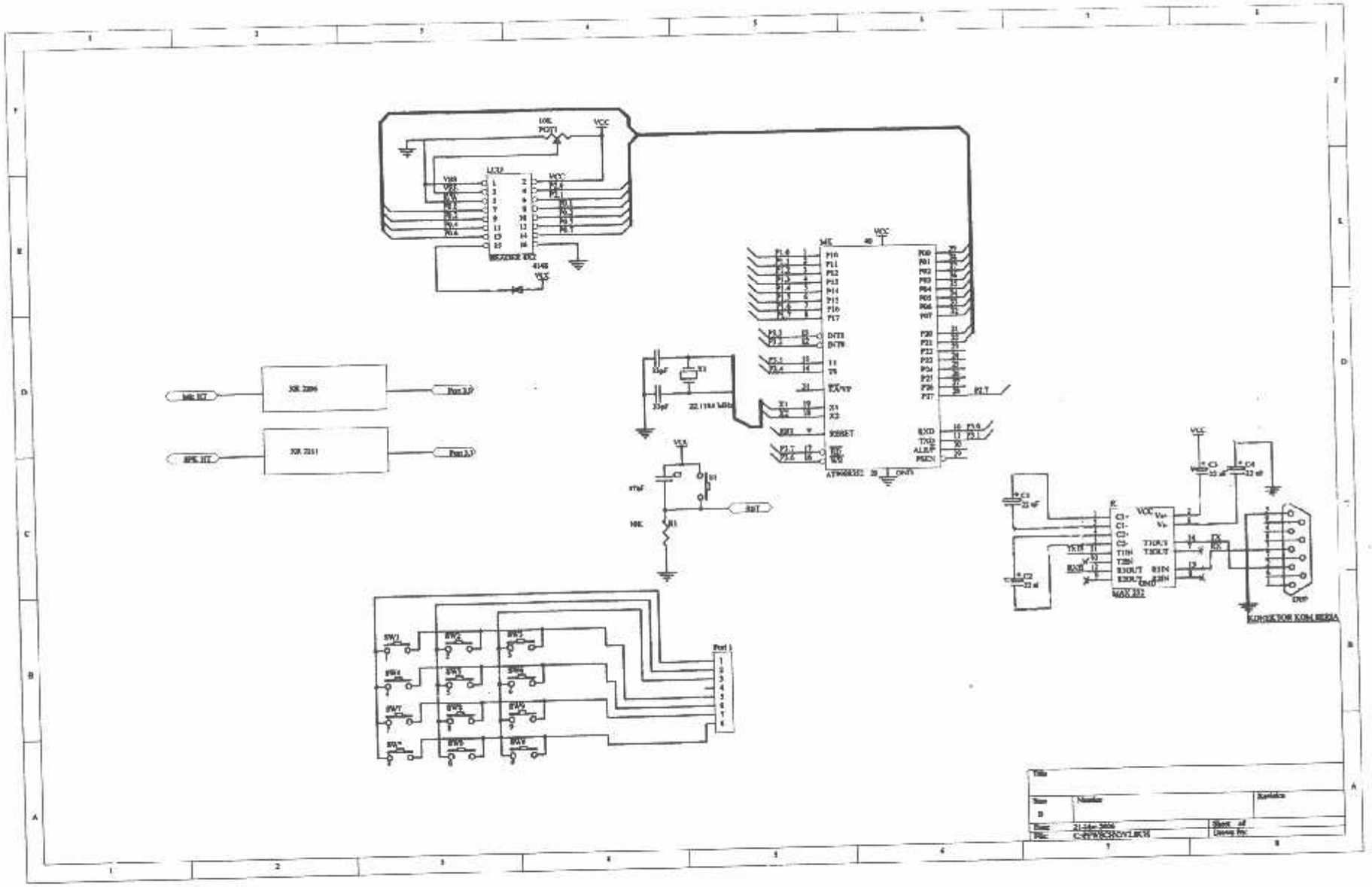

VCC
LCD
4148
MAX 232
KONEKTOR KOM.RS232A

FOTO ALAT

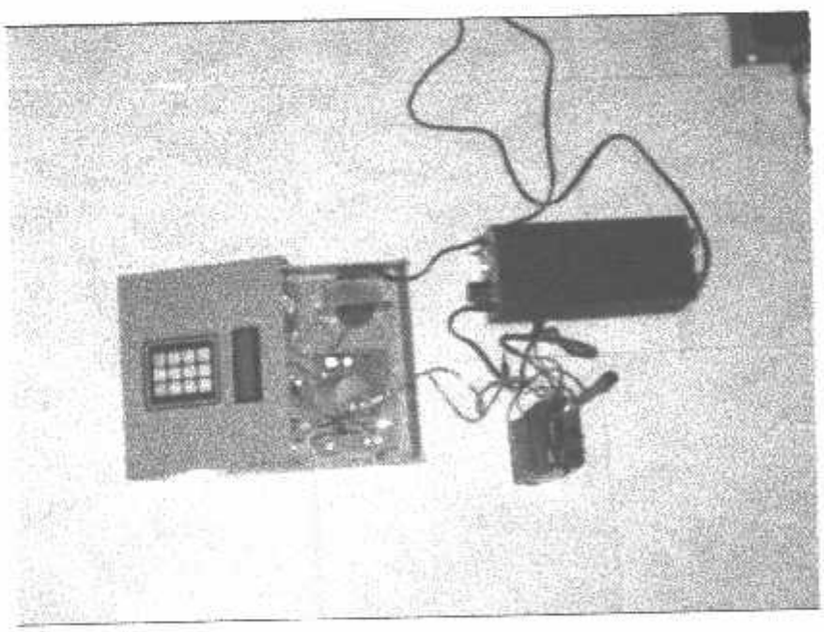
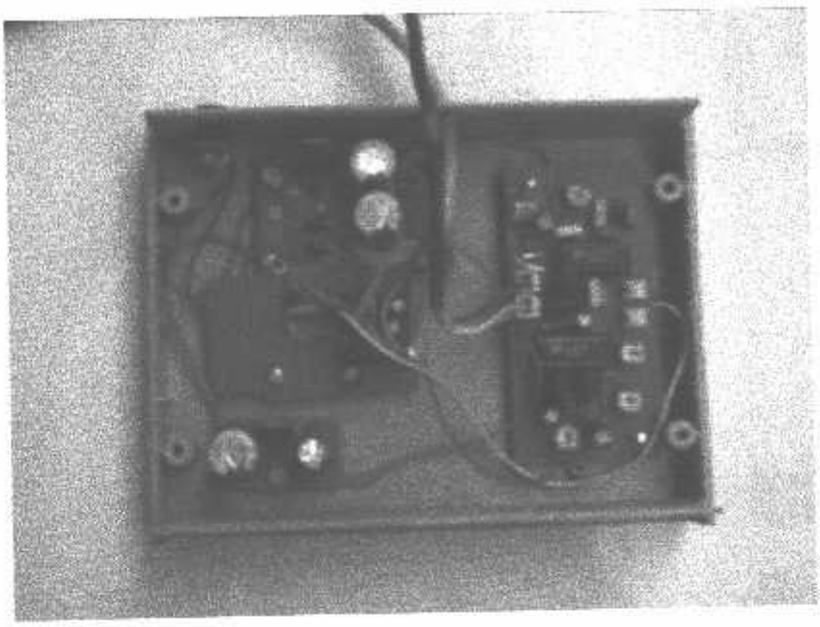
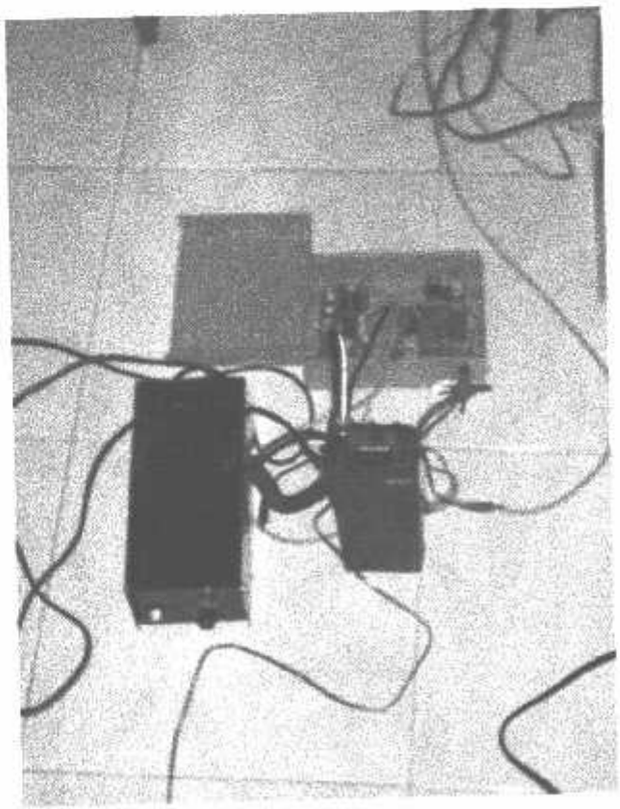


FOTO ALAT





LISTING PROGRAM

```
kolom1      Bit   P1.4          ; kiri (1,4,7,redial)
kolom2      Bit   P1.5          ;      (2,5,8,0)
kolom3      Bit   P1.6          ;      (3,3,9,#
kolom4      Bit   P1.7

baris1      Bit   P1.0          ; atas (1,2,3)
baris2      Bit   P1.1          ;      (4,5,6)
baris3      Bit   P1.2          ;      (7,8,9)
baris4      Bit   P1.3          ;      (*,0,#)
;
keyport     Data  P1
Relay       Bit   P2.5
keydata     Data  22h
temp        Data  21h

FlagKey     Data  24h

;tekantombol data  30h          30-46// 47,48=stack
Tmpnilai1   Data  50h          ; 50-56

        Clr   EA
        Mov   SP,#80h
start:
        Call  LCD_Inisialisasi
        Call  Serial_Initialization

ULANG:
        Clr   Relay
KeyInGetmatrix1:
        Clr   kolom3
        Jnb   baris4,KeyInGetmatrix0

        Jnb   RI,KeyInGetmatrix1

        Call  Serial_Receive

        Cjne  A,#'R',KeyInGetmatrix1

        Call  Serial_Receive

        Cjne  A,#'E',KeyInGetmatrix1

        Call  Serial_Receive
```

```
        Cjne  A,#'S',KeyInGetmatrix1

        Mov   R0,#60h
Ulang1xx:
        Call  Serial_Receive
Cek_Abjat:
        Cjne  A,#'1',nex_cek
        Jmp   Langsung1
nex_cek:
        Cjne  A,#'2',nex_cek1
        Jmp   Langsung1
nex_cek1:
        Cjne  A,#'3',nex_cek2
        Jmp   Langsung1
nex_cek2:
        Cjne  A,#'4',nex_cek3
        Jmp   Langsung1
nex_cek3:
        Cjne  A,#'5',nex_cek4
        Jmp   Langsung1
nex_cek4:
        Cjne  A,#'6',nex_cek5
        Jmp   Langsung1
nex_cek5:
        Cjne  A,#'7',nex_cek6
        Jmp   Langsung1
nex_cek6:
        Cjne  A,#'8',nex_cek7
        Jmp   Langsung1
nex_cek7:
        Cjne  A,#'9',nex_cek8
        Jmp   Langsung1
nex_cek8:
        Cjne  A,#'0',nex_cek9
        Jmp   Langsung1
nex_cek9:
        Cjne  A,#'&',nex_cek10
        Jmp   Langsung1
nex_cek10:
        Cjne  A,#'$',nex_cek11

        Jmp   Langsung1
nex_cek11:
        Jmp   Ulang1xx
Langsung1:
        Mov   @R0,A
```

```
        Mov   A,@R0
        Cjne  A,#'$',Tampilkandataxx

        Inc   R0
        Mov   @R0,#'$'
        Jmp   Lanjut

Tampilkandataxx:

        Inc   R0
        Jmp   Ulang1xx
KeyInGetmatrix0:
        Jmp   Key_masukan
;=============================
Lanjut:
        Call  LCD_Clear
        Call  lcd_line_1
        Mov   DPTR,#txt_no
        Call  LCD_TampilKata

        Mov   A,#88h
        Call  LCD_Tulis_Inst
        Call  Tampilkan_no

        Call  LCD_Line_2
        Mov   DPTR,#txt_rp
        Call  LCD_TampilKata

        Mov   A,#0C3h
        Call  LCD_Tulis_Inst

        Call  Tampilkan_Lcd
        Call  Delay_Fix_1s

        Call  Keypad_KeyIn

        Jmp   start

Key_masukan:
        Call  Delay_Fix_1s
;-------------------------------
SetRupiah:
        Call  LCD_Clear
        Call  lcd_line_1
        Mov   DPTR,#txt_setRP
        Call  LCD_TampilKata
```

```
        Call   LCD_Line_2
        Mov    DPTR,#txt_setRP1
        Call   LCD_TampilKata

        Call   LCD_Blink_On
        Mov    A,#88h
        Call   LCD_Tulis_Inst

        Mov    R0,#25h

        Mov    @R0,#'N'
        Inc    R0
        Mov    @R0,#'M'
        Inc    R0
INPUTKAN:
        Mov    FlagKey,#0
        Call   Keypad_KeyIn
        Cjne   A,#'#',SIMPANLAGI
        Jmp    INPUTKAN
SIMPANLAGI:
        Mov    @R0,A
        Inc    R0

        Mov    FlagKey,#0
        Call   Keypad_KeyIn
        Mov    @R0,A
        Inc    R0

        Mov    A,#0c5h
        Call   LCD_Tulis_Inst

        Mov    @R0,#'&'
        Inc    R0

        Mov    FlagKey,#0
        Call   Keypad_KeyIn
        Mov    @R0,A
        Inc    R0

        Mov    FlagKey,#0
        Call   Keypad_KeyIn
        Mov    @R0,A
        Inc    R0
        Mov    FlagKey,#0
        Call   Keypad_KeyIn
        Mov    @R0,A
```

```
        Inc     R0

        Mov     FlagKey,#0
        Call    Keypad_KeyIn
        Mov     @R0,A
        Inc     R0

        Mov     FlagKey,#0
        Call    Keypad_KeyIn
        Mov     @R0,A
        Inc     R0

        Mov     FlagKey,#0
        Call    Keypad_KeyIn
        Mov     @R0,A
        Inc     R0

        Mov     FlagKey,#0
        Call    Keypad_KeyIn
        Mov     @R0,A
        Inc     R0

        Mov     @R0,#'$'

        Call    LCD_Blink_Off

        Call    Delay_Fix_1s

yakin1cx:
        Call    LCD_Blink_Off
        Call    Delay_Fix_1s

        Call    LCD_Clear
        Call    lcd_line_1
        Mov     DPTR,#txt_menuyakin
        Call    LCD_TampilKata

        Call    LCD_Line_2
        Mov     DPTR,#txt_menuyakin1
        Call    LCD_TampilKata
Yakin1C:
        Mov     FlagKey,#0
        Call    Keypad_KeyIn
        Cjne    A,#'1',Yakin2C
        Call    Simpan_data1
        Setb    Relay
```

```
        Call   Delay_Fix_1s
        Call   Delay_Fix_1s
        Call   Delay_Fix_1s
        Call   Delay_Fix_1s

        Call   Outxx
        Clr    Relay

        Call   Delay_Fix_1s
        Call   Delay_Fix_1s
        Call   LCD_Clear
        Jmp    start

Yakin2C:
        Cjne   A,#'2',Yakin1C
        Call   LCD_Clear
        Jmp    start

Subroutine Outxx:

        Mov    R0,#52h
Ulang1:
        Mov    A,@R0
        Cjne   A,#'$',Tampilkandata
        Call   Serial_Transmit

        Ret
Tampilkandata:
        Call   Serial_Transmit
        Inc    R0
        Jmp    Ulang1
EndSub

;=============================================================
Subroutine Simpan_data1:

        Call   LCD_Clear
        Call   lcd_line_1
        Mov    DPTR,#txt_simpan
        Call   LCD_TampilKata
        Call   Delay_Fix_1s
        Mov    47h,#25h
        Mov    48h,#52h
Simpandata2:
        Mov    R0,47h                ; r0=30h // r0=31h
        Mov    A,@R0                 ; a=30h  // a=31h
```

```
        Cjne   A,#'$',SimpanData3
        Mov    R0,48h              ; r0=52h // r0=53h
        Mov    @R0,A               ; 52h<=30h //53h<=31h

        Ret                        ; start
SimpanData3:
        Inc    R0                  ; r0=31h //r0=32h
        Mov    47h,R0              ; 40h=31h //40h=32h
        Mov    R0,48h              ; r0=52h // r0=53h
        Mov    @R0,A               ; 52h<=30h //53h<=31h
        Inc    R0                  ; r0=53  // r0=54h
        Mov    48h,R0              ; 41h=53 //41=54h

        Jmp    Simpandata2
EndSub
Subroutine Tampilkan_No:
        Mov    R0,#60h
Ulang1a:

        Mov    A,@R0
        Cjne   A,#'&',Tampilkandataa
        ;Call  Serial_Transmit
        Ret

Tampilkandataa:
        Call   LCD_Tulis_Data
        Inc    R0
        Jmp    Ulang1a

EndSub

Subroutine Tampilkan_Lcd:

        Mov    R0,#60h
Ulang1xxx:
        Mov    A,@R0
        Cjne   A,#'&',TampilkandataB
        Inc    R0
Ulang1b:
        Mov    A,@R0
        Cjne   A,#'$',Tampilkandataxxx
        ;Call  Serial_Transmit
        Ret

Tampilkandataxxx:
        Call   LCD_Tulis_Data
```

```
        Inc     R0
        Jmp     Ulang1b
TampilkandataB:
        Inc     R0
        Jmp     Ulang1xxx
EndSub

;=============================================
Subroutine Keypad_KeyIn:
        Push    B                       ; amankan register B
KeyInGet1:
        Call    Keypad3x4               ; scan keypad
        Mov     A,keydata               ; isi keydata = data di rutin keypad
        Cjne    A,#0FFh,KeyInGet0       ; jk isi a # 0ffh ==>lompat
        Jmp     KeyInGet1
KeyInGet0:
        Mov     B,A                     ; simpan isi a to b
KeyInGet:
        Call    Keypad3x4
        Mov     A,keydata
        Cjne    A,B,KeyInOut            ; jk isi A # B lompat
        Jmp     KeyInGet
KeyInOut:
        Cjne    A,#0,KeyInOut1
        Mov     A,B
        Call    LCD_Tulis_Data
        Pop     B
        Ret
KeyInOut1:
        Mov     A,B
        Pop     B                       ; idem
EndSub
;=============================================
; routine u/ baca keypad 3x4
; output pd keydata(0-9,E=redial,F=#)
;=============================================
Subroutine Keypad3x4:

        Mov     keyport,#0FFh
        Clr     kolom1                  ;
;-----------
ul1:
        Jb      baris1,key1
        Mov     keydata,#'1'
        Ret
key1:
```

```
        Jb      baris2,key2
        Mov     keydata,#'4'
        Ret
key2:
        Jb      baris3,key3
        Mov     keydata,#'7'
        Ret
key3:
        ;Jb     baris4,key4
        ;Mov    keydata,#'*'
        ;Ret
;--------------
key4:
        Setb    kolom1
        Clr     kolom2
        ;--------------
        Jb      baris1,key5
        Mov     keydata,#'2'
        Ret
key5:
        Jb      baris2,key6
        Mov     keydata,#'5'
        Ret
key6:
        Jb      baris3,key7
        Mov     keydata,#'8'
        Ret
key7:
        Jb      baris4,key8
        Mov     keydata,#'0'
        Ret
;--------------
key8:
        Setb    kolom2
        Clr     kolom3
        ;--------------
        Jb      baris1,key9
        Mov     keydata,#'3'
        Ret
key9:
        Jb      baris2,key10
        Mov     keydata,#'6'
        Ret
key10:
        Jb      baris3,key11
        Mov     keydata,#'9'
```

```
        Ret
key11:
        Jb      baris4,key12
        Mov     keydata,#'#'
        Ret
key12:
        Mov     keydata,#0FFh

EndSub

Subroutine Cek_Tbl_Key:

EndSub

Subroutine Serial_Receive:
        Jnb     RI,$
        Clr     RI
        Mov     A,SBUF
        Clr     RI
EndSub
Subroutine Serial_Transmit:
        Mov     SBUF,A
        Jnb     TI,$
        Clr     TI

        Ret
EndSub
Subroutine Serial_Initialization:
        Mov     SCON,#50h
        Mov     TH1,#208            ; BAUDRATE 1200
        Mov     87h,#00h            ; PCON
        Mov     TMOD,#21h
        Mov     TCON,#01010000B     ; RUN T1 AND T0
        ;Mov    IE,#10000010B
        ;Mov    IP,#00001000B
EndSub

Subroutine LCD_Clear:
        Mov     A,#01h
        Call    LCD_Tulis_Inst
EndSub
Subroutine LCD_Blink_Off:
        Push    ACC
        Mov     A,#00001100b        ;
        Lcall   LCD_Tulis_Inst
        Pop     ACC
```

```
EndSub
Subroutine LCD_Blink_On:
        Push  ACC
        Mov   A,#00001101b        ;
        Lcall LCD_Tulis_Inst
        Pop   ACC
EndSub
Subroutine lcd_line_1:
        Mov   A,#80h
        Call  LCD_Tulis_Inst
EndSub
Subroutine LCD_Line_2:
        Mov   A,#0C0h
        Call  LCD_Tulis_Inst
EndSub
Subroutine LCD_Cursor_Position:
        Push  ACC
        Mov   A,R0                ;15   26
        Anl   A,#0F0h             ;10   20
        Cjne  A,#10h,lcd_cursor_position1
        Mov   A,R0  ;15
        Call  LCD_Tulis_Inst
        Jmp   lcd_cursor_position_end
 lcd_cursor_position1:
        Cjne  A,#20h,lcd_cursor_position_end
        Mov   A,R0                ; 26
        Call  LCD_Tulis_Inst
 lcd_cursor_position_end:
        Pop   ACC
 EndSub
 Subroutine LCD_TampilKata:
        Push  ACC
        Push  DPL
        Push  DPH
 TampilKata1:
        Clr   A
        Movc  A,@A+DPTR
        Cjne  A,#0,TampilKata2    ; intinya
        Jmp   out
 TampilKata2:
        Inc   DPTR
        Call  LCD_Tulis_Data
        Jmp   TampilKata1
 out:
        Pop   DPH
        Pop   DPL
```

```
        Pop   ACC
EndSub

Subroutine LCD_Inisialisasi:
        ;Call  delayL
        Mov   A,#3Fh
        Call   LCD_Tulis_Inst
        Mov   A,#0Ch
        Call   LCD_Tulis_Inst
        Mov   A,#06h
        Call   LCD_Tulis_Inst
        Mov   A,#1Ch
        Call   LCD_Tulis_Inst
        Mov   A,#01h
        Call   LCD_Tulis_Inst
 EndSub
 Subroutine LCD_Tulis_Inst:
        Clr    P2.7
        Mov   P0,A
        Setb   P2.6
        Clr    P2.6
 EndSub
 Subroutine LCD_Tulis_Data:
        Setb   P2.7
        Mov   P0,A
        Setb   P2.6
        Clr    P2.6
 EndSub
 Subroutine LCD_Hexa:
        Push  07h
        Push  ACC

        Mov   7,A
        Anl    A,#0F0h
        Swap  A
        Orl    A,#30h
        Lcall  tes_huruf_
        Call   LCD_Tulis_Data
        Mov   A,7
        Anl    A,#0Fh
        Orl    A,#30h
        Lcall  tes_huruf_
        Lcall  LCD_Tulis_Data

        Pop    ACC
        Pop    07h
```

```
        Ret

EndSub
;=================== DELAY ==========================
Subroutine Delay_Var_1ms:
        Call   Delay_Fix_1ms
        Djnz   R0,Delay_Var_1ms
EndSub
Subroutine Delay_Var_10ms:
        Call   Delay_Fix_10ms
        Djnz   R0,Delay_Var_10ms
EndSub
Subroutine Delay_Var_100ms:
        Call   Delay_Fix_1ms
        Djnz   R0,Delay_Var_100ms
EndSub
Subroutine Delay_Var_1s:
        Call   Delay_Fix_1s
        Djnz   R0,Delay_Var_1s
EndSub
Subroutine Delay_Var_10s:
        Call   Delay_Fix_10s
        Djnz   R0,Delay_Var_10s
EndSub
Subroutine Delay_Var_10us:
        Call   Delay_Fix_10us
        Djnz   R0,Delay_Var_10us
EndSub
Subroutine Delay_Fix_10us:
        Push   1
        Mov    1,#20
        Djnz   1,$
        Pop    1
EndSub
Subroutine Delay_Fix_10s:
        Push   1
        Mov    1,#100
delay_fix_10s_1:
        Call   Delay_Fix_100ms
        Djnz   1,delay_fix_10s_1
        Pop    1
EndSub
Subroutine Delay_Fix_1s:
        Push   1
        Mov    1,#100
delay_fix_1000ms_1:
```

```
        Call   Delay_Fix_10ms
        Djnz   1,delay_fix_1000ms_1
        Pop    1
EndSub
Subroutine Delay_Fix_100ms:
        Push   1
        Mov    1,#10
delay_fix_100ms_1:
        Call   Delay_Fix_10ms
        Djnz   1,delay_fix_100ms_1
        Pop    1
EndSub
Subroutine Delay_Fix_10ms:
        Mov    TMOD,#00000001b  ; Timer 1 bekerja pada mode 1
        Mov    TL0,#3Dh         ; siapkan waktu tunda 50 mili-detik
        Mov    TH0,#0B0h
        Clr    TF0              ; me-nol-kan bit limpahan
        Setb   TR0              ; timer mulai bekerja
        Jnb    TF0,$            ; tunggu di sini sampai melimpah
        Clr    TR0              ; timer berhenti kerja
        Ret
EndSub
Subroutine Delay_Fix_1ms:
        Mov    TMOD,#00000001b  ; Timer 1 bekerja pada mode 1
        Mov    TL0,#0EDh        ; siapkan waktu tunda 50 mili-detik
        Mov    TH0,#78h
        Clr    TF0              ; me-nol-kan bit limpahan
        Setb   TR0              ; timer mulai bekerja
        Jnb    TF0,$            ; tunggu di sini sampai melimpah
        Clr    TR0              ; timer berhenti kerja
        Ret
EndSub                          ;'1234567890abcdef'

txt_setRP:      Db    'No.Pel:',0
txt_setRP1:     Db    'Jml:      m',0
txt_menuyakin:  Db    'Yakin ?',0
txt_menuyakin1: Db    '   Y-1,T-2',0
txt_simpan:     Db    'simpan data',0
txt_no:         Db    'No Pel:',0
txt_rp:         Db    'Rp:',0
```

LISTING PROGRAM

frmProperties (FRMPROPS.FRM)

```
Private iFlow As Integer, iTempEcho As Boolean


Sub LoadPropertySettings()
Dim i As Integer, Settings As String, Offset As Integer

' Load Port Settings
For i = 1 To 16
   cboPort.AddItem "Com" & Trim$(Str$(i))
Next i

' Load Speed Settings
cboSpeed.AddItem "110"
cboSpeed.AddItem "300"
cboSpeed.AddItem "600"
cboSpeed.AddItem "1200"
cboSpeed.AddItem "2400"
cboSpeed.AddItem "4800"
cboSpeed.AddItem "9600"
cboSpeed.AddItem "14400"
cboSpeed.AddItem "19200"
cboSpeed.AddItem "28800"
cboSpeed.AddItem "38400"
cboSpeed.AddItem "56000"
cboSpeed.AddItem "57600"
cboSpeed.AddItem "115200"
cboSpeed.AddItem "128000"
cboSpeed.AddItem "256000"

' Load Data Bit Settings
cboDataBits.AddItem "4"
cboDataBits.AddItem "5"
cboDataBits.AddItem "6"
cboDataBits.AddItem "7"
cboDataBits.AddItem "8"

' Load Parity Settings
cboParity.AddItem "Even"
cboParity.AddItem "Odd"
cboParity.AddItem "None"
cboParity.AddItem "Mark"
cboParity.AddItem "Space"
```

```
' Load Stop Bit Settings
cboStopBits.AddItem "1"
cboStopBits.AddItem "1.5"
cboStopBits.AddItem "2"

' Set Default Settings

Settings = frmTerminal.MSComm1.Settings

' In all cases the right most part of Settings will be 1 character
' except when there are 1.5 stop bits.
If InStr(Settings, ".") > 0 Then
   Offset = 2
Else
   Offset = 0
End If

cboSpeed.Text = Left$(Settings, Len(Settings) - 6 - Offset)
Select Case Mid$(Settings, Len(Settings) - 4 - Offset, 1)
Case "e"
   cboParity.ListIndex = 0
Case "m"
   cboParity.ListIndex = 1
Case "n"
   cboParity.ListIndex = 2
Case "o"
   cboParity.ListIndex = 3
Case "s"
   cboParity.ListIndex = 4
End Select

cboDataBits.Text = Mid$(Settings, Len(Settings) - 2 - Offset, 1)
cboStopBits.Text = Right$(Settings, 1 + Offset)

cboPort.ListIndex = frmTerminal.MSComm1.CommPort - 1

optFlow(frmTerminal.MSComm1.Handshaking).Value = True
If Echo Then
   optEcho(1).Value = True
Else
   optEcho(0).Value = True
End If

End Sub
```

```
Private Sub cmdCancel_Click()
Unload Me
End Sub

Private Sub cmdOK_Click()
Dim OldPort As Integer, ReOpen As Boolean

On Error Resume Next

Echo = iTempEcho
OldPort = frmTerminal.MSComm1.CommPort
NewPort = cboPort.ListIndex + 1

If NewPort <> OldPort Then                ' If the port number changes, close the
old port.
   If frmTerminal.MSComm1.PortOpen Then
      frmTerminal.MSComm1.PortOpen = False
      ReOpen = True
   End If

   frmTerminal.MSComm1.CommPort = NewPort        ' Set the new port
number.

   If Err = 0 Then
      If ReOpen Then
         frmTerminal.MSComm1.PortOpen = True
      End If
   End If

   If Err Then
      MsgBox Error$, 48
      frmTerminal.MSComm1.CommPort = OldPort
      Exit Sub
   End If
  End If


  frmTerminal.MSComm1.Settings = Trim$(cboSpecd.Text) & "," &
  Left$(cboParity.Text, 1) _
    & "," & Trim$(cboDataBits.Text) & "," & Trim$(cboStopBits.Text)

  If Err Then
     MsgBox Error$, 48
     Exit Sub
  End If
```

```
frmTerminal.MSComm1.Handshaking = iFlow
If Err Then
   MsgBox Error$, 48
   Exit Sub
End If

SaveSetting App.Title, "Properties", "Settings", frmTerminal.MSComm1.Settings
SaveSetting App.Title, "Properties", "CommPort",
frmTerminal.MSComm1.CommPort
SaveSetting App.Title, "Properties", "Handshaking",
frmTerminal.MSComm1.Handshaking
SaveSetting App.Title, "Properties", "Echo", Echo

Unload Me

End Sub

Private Sub Form_Load()

' Set the form's size
Me.Left = (Screen.Width - Me.Width) / 2
Me.Top = (Screen.Height - Me.Height) / 2

' Size the frame to fit in the tabstrip control
fraSettings.Move tabSettings.ClientLeft, tabSettings.ClientTop

' Make sure the frame is the top most control
fraSettings.ZOrder

' Load current property settings
LoadPropertySettings

End Sub

Private Sub optEcho_Click(Index As Integer)
If Index = 1 Then
   iTempEcho = True
Else
   iTempEcho = False
End If
End Sub

Private Sub optFlow_Click(Index As Integer)
iFlow = Index
End Sub
```

frmTerminal (Form1.frm)

```
Option Explicit


Dim FileName As String
Dim FileName1 As String

Private Sub cmdAmbilData_Click()
Dim a, b, c, d, e, f, g, h, i, j, k, l, m, n, o, p, q, r, s, t, u, v, w, x, y, z
Dim s0, s1, s2, s3, s4, s5, s6, s7, s8, s9
Dim s10, s11, s12, s13, s14, s15, s16, s17, s18, s19
Dim s20, s21, s22, s23, s24, s25, s26, s27, s28, s29
Dim s30, s31, s32, s33, s34, s35, s36, s37, s38, s39
Dim EA As Variant
Dim Rupiah As Long
Dim Km As Long
Dim Waktu As Long
Dim Taxi As Integer

    FileName1 = App.Path & "\" & Replace(DTP1.Value, "/", "_") & ".txt"
    If Dir(FileName1) = "" Then
       MsgBox "Data tidak ditemukan", vbCritical, "Error"
       LV2.ListItems.Clear
       Exit Sub
    End If

    CM1.OpenFile FileName1

    LV2.ListItems.Clear
    If CM1.Text = "" Then Exit Sub

    For i = 0 To CM1.LineCount - 2
       a = CM1.GetLine(i)
       EA = Split(a, ";")
       LV2.ListItems.Add , "A" & Date & Time & i, LV2.ListItems.Count + 1
       LV2.ListItems(LV2.ListItems.Count).SubItems(1) = EA(0)
    Next i

End Sub

Private Sub cmdClearData_Click()
   LV1.ListItems.Clear
End Sub

Private Sub cmdComm_Click()
```

```
  frmProperties.Show vbModal
End Sub

Private Sub cmdConnect_Click()
  If cmdConnect.Caption = "Connect" Then
    MSComm1.PortOpen = True
    cmdConnect.Caption = "Disconnect"
    Proses = Awal
  Else
    MSComm1.PortOpen = False
    cmdConnect.Caption = "Connect"
  End If
End Sub


Private Sub cmdExit_Click()
  Unload Me
End Sub

Private Sub cmdGetData_Click()

  If MSComm1.PortOpen = False Then
    MsgBox "Komunikasi belum diaktifkan", vbCritical, "Error "
    Exit Sub
  End If

  txtTerm.Text = ""
    MSComm1.DTREnable = True
    Sleep 7000
  'Do
    MSComm1.Output = "RES"
    'DoEvents
    'If txtTerm.Text <> "" Then Exit Do
    Sleep 100
    MSComm1.Output = "RES"
    Sleep 500
  'Loop
  MSComm1.DTREnable = False

End Sub

Private Sub cmdSave_Click()
Dim a, b, c, d, e, f, g, h, i, j, k, l, m, n, o, p, q, r, s, t, u, v, w, x, y, z
Dim s0, s1, s2, s3, s4, s5, s6, s7, s8, s9
Dim s10, s11, s12, s13, s14, s15, s16, s17, s18, s19
Dim s20, s21, s22, s23, s24, s25, s26, s27, s28, s29
```

```
Dim s30, s31, s32, s33, s34, s35, s36, s37, s38, s39

  If LV1.ListItems.Count = 0 Then
     If MsgBox("Anda yakin menyimpan data kosong?", vbOKCancel,
"Perhatian") = vbCancel Then Exit Sub
  End If

  s30 = App.Path & "\" & Replace(lblTanggal.Caption, "/", "_") & ".txt"

  CM1.Text = ""
  For i = 1 To LV1.ListItems.Count
     a = LV1.ListItems(i).Text & ";"
     a = a & LV1.ListItems(i).SubItems(1) & ";"
     a = a & LV1.ListItems(i).SubItems(2) & ";"
     a = a & LV1.ListItems(i).SubItems(3) & ";"
     a = a & LV1.ListItems(i).SubItems(4) & ";"
     CM1.Text = CM1.Text & a & vbCrLf
   Next i

   CM1.SaveFile s30, True
   a = a
End Sub


Private Sub Form_Load()
Dim a, b, c, d, e, f, g, h, i, j, k, l, m, n, o, p, q, r, s, t, u, v, w, x, y, z
Dim s0, s1, s2, s3, s4, s5, s6, s7, s8, s9
Dim s10, s11, s12, s13, s14, s15, s16, s17, s18, s19
Dim s20, s21, s22, s23, s24, s25, s26, s27, s28, s29
Dim s30, s31, s32, s33, s34, s35, s36, s37, s38, s39
Dim EA As Variant
Dim Str1 As String


    Dim CommPort As String, Handshaking As String, Settings As String

    lblTanggal.Caption = Date

    FileName1 = App.Path & "\data.txt"
    If Dir(FileName1) = "" Then
       LV1.ListItems.Clear
       Exit Sub
    End If

    CM1.OpenFile FileName1
```

```
LV1.ListItems.Clear
If CM1.Text = "" Then Exit Sub

For i = 0 To CM1.LineCount - 2
   a = CM1.GetLine(i)
   EA = Split(a, ";")
   LV1.ListItems.Add , "A" & Date & Time & i, EA(0)
   LV1.ListItems(LV1.ListItems.Count).SubItems(1) = EA(1)
   LV1.ListItems(LV1.ListItems.Count).SubItems(2) = EA(2)
   LV1.ListItems(LV1.ListItems.Count).SubItems(3) = EA(3)
   LV1.ListItems(LV1.ListItems.Count).SubItems(4) = EA(4)
 Next i

End Sub

Private Sub MSComm1_OnComm()
  Dim EVMsg$
  Dim ERMsg$

  ' Branch according to the CommEvent property.
  Select Case MSComm1.CommEvent
    ' Event messages.
    Case comEvReceive
      Dim Buffer As Variant
      Buffer = MSComm1.Input
      Debug.Print "Receive - " & StrConv(Buffer, vbUnicode)
      ShowData txtTerm, (StrConv(Buffer, vbUnicode))
    Case comEvSend
    Case comEvCTS
      EVMsg$ = "Change in CTS Detected"
    Case comEvDSR
      EVMsg$ = "Change in DSR Detected"
    Case comEvCD
      EVMsg$ = "Change in CD Detected"
    Case comEvRing
      EVMsg$ = "The Phone is Ringing"
    Case comEvEOF
      EVMsg$ = "End of File Detected"
    GoTo x1
    ' Error messages.
'   Case comBreak
'     ERMsg$ = "Break Received"
'   Case comCDTO
'     ERMsg$ = "Carrier Detect Timeout"
'   Case comCTSTO
'     ERMsg$ = "CTS Timeout"
```

```
'     Case comDCB
'       ERMsg$ = "Error retrieving DCB"
'     Case comDSRTO
'       ERMsg$ = "DSR Timeout"
'     Case comFrame
'       'ERMsg$ = "Framing Error"
'     Case comOverrun
'       ERMsg$ = "Overrun Error"
'     Case comRxOver
'       ERMsg$ = "Receive Buffer Overflow"
'     Case comRxParity
'       ERMsg$ = "Parity Error"
'     Case comTxFull
'       ERMsg$ = "Transmit Buffer Full"
x1:
      Case Else
        Err.Clear
        'ERMsg$ = "Unknown error or event"
    End Select

End Sub
Private Static Sub ShowData(Term As Control, Data As String)
    On Error GoTo Handler
    Const MAXTERMSIZE = 16000
    Dim TermSize As Long, i

    ' Make sure the existing text doesn't get too large.
    TermSize = Len(Term.Text)
    If TermSize > MAXTERMSIZE Then
      Term.Text = Mid$(Term.Text, 4097)
      TermSize = Len(Term.Text)
    End If

    ' Point to the end of Term's data.
    Term.SelStart = TermSize

    ' Filter/handle BACKSPACE characters.
    Do
      i = InStr(Data, Chr$(8))
      If i Then
        If i = 1 Then
          Term.SelStart = TermSize - 1
          Term.SelLength = 1
          Data = Mid$(Data, i + 1)
        Else
          Data = Left$(Data, i - 2) & Mid$(Data, i + 1)
```

```
    End If
  End If
Loop While i

' Eliminate line feeds.
Do
  i = InStr(Data, Chr$(10))
  If i Then
    Data = Left$(Data, i - 1) & Mid$(Data, i + 1)
  End If
Loop While i

' Make sure all carriage returns have a line feed.
i = 1
Do
  i = InStr(i, Data, Chr$(13))
  If i Then
    Data = Left$(Data, i) & Chr$(10) & Mid$(Data, i + 1)
    i = i + 1
  End If
Loop While i

' Add the filtered data to the SelText property.
Term.SelText = Data

' Log data to file if requested.
Term.SelStart = Len(Term.Text)
Exit Sub

Handler:
  MsgBox Error$
  Resume Next
End Sub

Private Sub txtTerm_Change()
Dim a, b, c, d, e, f, g, h, i, j, k, l, m, n, o, p, q, r, s, t, u, v, w, x, y, z
Dim s0, s1, s2, s3, s4, s5, s6, s7, s8, s9
Dim s10, s11, s12, s13, s14, s15, s16, s17, s18, s19
Dim s20, s21, s22, s23, s24, s25, s26, s27, s28, s29
Dim s30, s31, s32, s33, s34, s35, s36, s37, s38, s39
Dim Rupiah As Long
Dim Volume As Single
Dim NoPelanggan As String
Dim IsKetemu As Boolean

    If txtTerm.Text = "" Then Exit Sub
```

```
a = InStr(1, txtTerm.Text, "$")
If a <> 0 Then
   b = InStrRev(txtTerm.Text, "&", -1, vbTextCompare)
   If b = 0 Then Exit Sub
   c = InStr(b, txtTerm.Text, "$", vbTextCompare)
   If c = 0 Then Exit Sub
   v = Mid(txtTerm.Text, b + 1, c - b - 1)

   b = InStrRev(txtTerm.Text, "&", -1, vbTextCompare)
   If b = 0 Then Exit Sub
   c = InStrRev(txtTerm.Text, "NM", b - 1, vbTextCompare)
   If c = 0 Then Exit Sub
   n = Mid(txtTerm.Text, c + 2, b - c - 2)

   '----------

   For i = 1 To LV1.ListItems.Count
      If LV1.ListItems(i).Text = n Then
         If LV1.ListItems(i).SubItems(3) = "" Then
            LV1.ListItems(i).SubItems(1) = 0
            LV1.ListItems(i).SubItems(2) = 0
            LV1.ListItems(i).SubItems(3) = v
            LV1.ListItems(i).SubItems(4) = Val(v) * 10
            Call KirimHarga(LV1.ListItems(i).SubItems(0),
LV1.ListItems(i).SubItems(4))
         Else
            LV1.ListItems(i).SubItems(1) = LV1.ListItems(i).SubItems(3)
            LV1.ListItems(i).SubItems(2) = LV1.ListItems(i).SubItems(4)
            LV1.ListItems(i).SubItems(3) = v
            LV1.ListItems(i).SubItems(4) = (Val(v) -
Val(LV1.ListItems(i).SubItems(1))) * 10
            Call KirimHarga(LV1.ListItems(i).Text,
LV1.ListItems(i).SubItems(4))
         End If
         IsKetemu = True
         Exit For
      End If
   Next i

   If IsKetemu = False Then
      a = a
      LV1.ListItems.Add , "A" & Date & Time & LV1.ListItems.Count, n
      LV1.ListItems(LV1.ListItems.Count).SubItems(1) = 0
      LV1.ListItems(LV1.ListItems.Count).SubItems(2) = 0
      LV1.ListItems(LV1.ListItems.Count).SubItems(3) = v
      LV1.ListItems(LV1.ListItems.Count).SubItems(4) = Val(v) * 10
```

Features

- Compatible with MCS®51 Products
- 8K Bytes of In-System Reprogrammable Downloadable Flash Memory
  - SPI Serial Interface for Program Downloading
  - Endurance: 1,000 Write/Erase Cycles
- 2K Bytes EEPROM
  - Endurance: 100,000 Write/Erase Cycles
- 4V to 6V Operating Range
- Fully Static Operation: 0 Hz to 24 MHz
- Three-level Program Memory Lock
- 256 x 8-bit Internal RAM
- 32 Programmable I/O Lines
- Three 16-bit Timer/Counters
- Nine Interrupt Sources
- Programmable UART Serial Channel
- SPI Serial Interface
- Low-power Idle and Power-down Modes
- Interrupt Recovery from Power-down
- Programmable Watchdog Timer
- Dual Data Pointer
- Power-off Flag

Description

The AT89S8252 is a low-power, high-performance CMOS 8-bit microcontroller with 8K bytes of downloadable Flash programmable and erasable read-only memory and 2K bytes of EEPROM. The device is manufactured using Atmel's high-density nonvolatile memory technology and is compatible with the industry-standard 80C51 instruction set and pinout. The on-chip downloadable Flash allows the program memory to be reprogrammed In-System through an SPI serial interface or by a conventional nonvolatile memory programmer. By combining a versatile 8-bit CPU with downloadable Flash on a monolithic chip, the Atmel AT89S8252 is a powerful microcontroller, which provides a highly-flexible and cost-effective solution to many embedded control applications.

The AT89S8252 provides the following standard features: 8K bytes of downloadable Flash, 2K bytes of EEPROM, 256 bytes of RAM, 32 I/O lines, programmable watchdog timer, two data pointers, three 16-bit timer/counters, a six-vector two-level interrupt architecture, a full duplex serial port, on-chip oscillator, and clock circuitry. In addition, the AT89S8252 is designed with static logic for operation down to zero frequency and supports two software selectable power saving modes. The Idle Mode stops the CPU while allowing the RAM, timer/counters, serial port, and interrupt system to continue functioning. The Power-down mode saves the RAM contents but freezes the oscillator, disabling all other chip functions until the next external interrupt or hardware reset.

The downloadable Flash can be changed a single byte at a time and is accessible through the SPI serial interface. Holding RESET active forces the SPI bus into a serial programming interface and allows the program memory to be written to or read from unless lock bits have been activated.

8-bit Microcontroller with 8K Bytes Flash

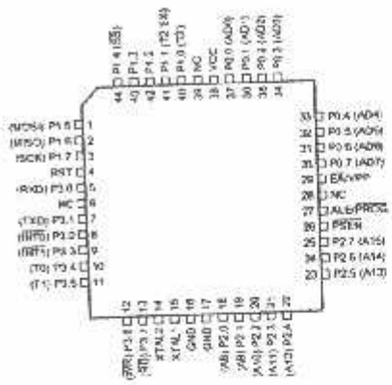
AT89S8252

0401F–MICRO–11/03

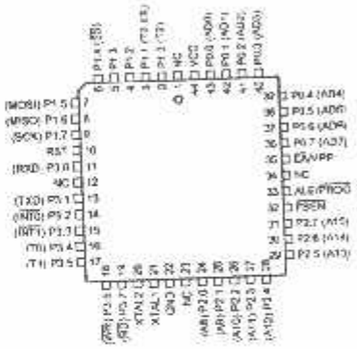
Pin Configurations

PDIP

TQFP



PLCC



Pin Description

VCC

Supply voltage.

GND

Ground.

Port 0

Port 0 is an 8-bit open drain bi-didirectional I/O port. As an output port, each pin can sink eight TTL inputs. When 1s are written to port 0 pins, the pins can be used as high-impedance inputs.

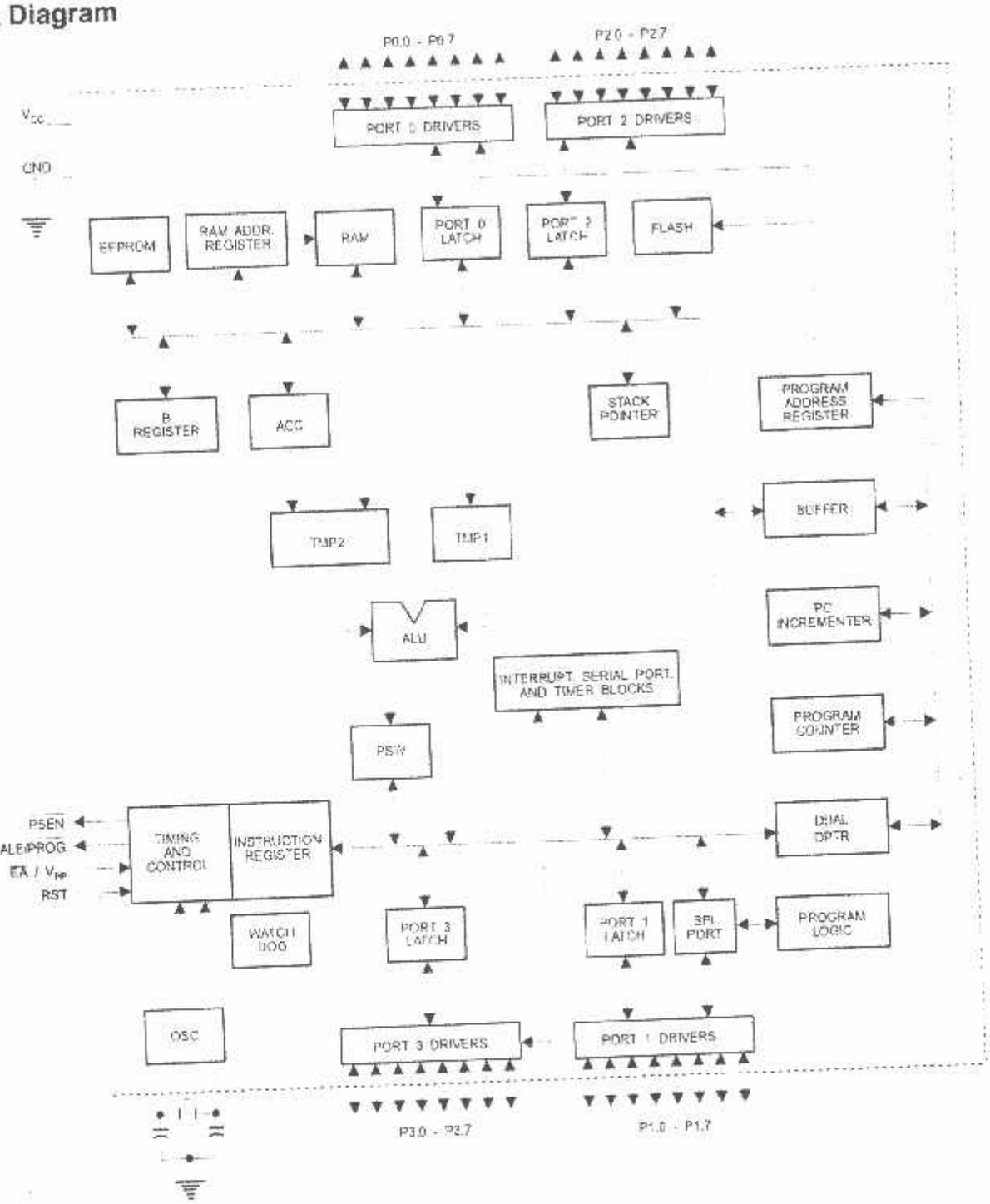
Port 0 can also be configured to be the multiplexed low-order address/data bus during accesses to external program and data memory. In this mode, P0 has internal pull-ups.

Port 0 also receives the code bytes during Flash programming and outputs the code bytes during program verification. External pull-ups are required during program verification.

Port 1

Port 1 is an 8-bit bi-directional I/O port with internal pull-ups. The Port 1 output buffers can sink/source four TTL inputs. When 1s are written to Port 1 pins, they are pulled high by the internal pull-ups and can be used as inputs. As inputs, Port 1 pins that are externally being pulled low will source current (I_{IL}) because of the internal pull-ups.

Block Diagram



Some Port 1 pins provide additional functions. P1.0 and P1.1 can be configured to be the timer/counter 2 external count input (P1.0/T2) and the timer/counter 2 trigger input (P1.1/T2EX), respectively.

Furthermore, P1.4, P1.5, P1.6, and P1.7 can be configured as the SPI slave port select, data input/output and shift clock input/output pins as shown in the following table.

Port Pin	Alternate Functions
P1.0	T2 (external count input to Timer/Counter 2), clock-out
P1.1	T2EX (Timer/Counter 2 capture/reload trigger and direction control)
P1.4	$\overline{SS}$ (Slave port select input)
P1.5	MOSI (Master data output, slave data input pin for SPI channel)
P1.6	MISO (Master data input, slave data output pin for SPI channel)
P1.7	SCK (Master clock output, slave clock input pin for SPI channel)

Port 1 also receives the low-order address bytes during Flash programming and verification.

Port 2

Port 2 is an 8-bit bi-directional I/O port with internal pull-ups. The Port 2 output buffers can sink/source four TTL inputs. When 1s are written to Port 2 pins, they are pulled high by the internal pull-ups and can be used as inputs. As inputs, Port 2 pins that are externally being pulled low will source current (I_{IL}) because of the internal pull-ups.

Port 2 emits the high-order address byte during fetches from external program memory and during accesses to external data memory that use 16-bit addresses (MOVX @ DPTR). In this application, Port 2 uses strong internal pull-ups when emitting 1s. During accesses to external data memory that use 8-bit addresses (MOVX @ RI), Port 2 emits the contents of the P2 Special Function Register.

Port 2 also receives the high-order address bits and some control signals during Flash programming and verification.

Port 3

Port 3 is an 8-bit bi-directional I/O port with internal pull-ups. The Port 3 output buffers can sink/source four TTL inputs. When 1s are written to Port 3 pins, they are pulled high by the internal pull-ups and can be used as inputs. As inputs, Port 3 pins that are externally being pulled low will source current (I_{IL}) because of the pull-ups.

Port 3 receives some control signals for Flash programming and verification.

Port 3 also serves the functions of various special features of the AT89S8252, as shown in the following table.

Port Pin	Alternate Functions
P3.0	RXD (serial input port)
P3.1	TXD (serial output port)
P3.2	$\overline{INT0}$ (external interrupt 0)
P3.3	$\overline{INT1}$ (external interrupt 1)
P3.4	T0 (timer 0 external input)
P3.5	T1 (timer 1 external input)
P3.6	$\overline{WR}$ (external data memory write strobe)
P3.7	$\overline{RD}$ (external data memory read strobe)

RST

Reset Input. A high on this pin for two machine cycles while the oscillator is running resets the device.

ALE/$\overline{PROG}$

Address Latch Enable is an output pulse for latching the low byte of the address during accesses to external memory. This pin is also the program pulse input ($\overline{PROG}$) during Flash programming.

In normal operation, ALE is emitted at a constant rate of 1/6 the oscillator frequency and may be used for external timing or clocking purposes. Note, however, that one ALE pulse is skipped during each access to external data memory.

If desired, ALE operation can be disabled by setting bit 0 of SFR location 8EH. With the bit set, ALE is active only during a MOVX or MOVC instruction. Otherwise, the pin is weakly pulled high. Setting the ALE-disable bit has no effect if the microcontroller is in external execution mode.

$\overline{PSEN}$

Program Store Enable is the read strobe to external program memory.

When the AT89S8252 is executing code from external program memory, $\overline{PSEN}$ is activated twice each machine cycle, except that two $\overline{PSEN}$ activations are skipped during each access to external data memory.

$\overline{EA}$/VPP

External Access Enable. $\overline{EA}$ must be strapped to GND in order to enable the device to fetch code from external program memory locations starting at 0000H up to FFFFH. Note, however, that if lock bit 1 is programmed, $\overline{EA}$ will be internally latched on reset.

$\overline{EA}$ should be strapped to V_{CC} for internal program executions. This pin also receives the 12-volt programming enable voltage (V_{PP}) during Flash programming when 12-volt programming is selected.

XTAL1

Input to the inverting oscillator amplifier and input to the internal clock operating circuit.

XTAL2

Output from the inverting oscillator amplifier.

Special Function Registers

A map of the on-chip memory area called the Special Function Register (SFR) space is shown in Table 1.

Note that not all of the addresses are occupied, and unoccupied addresses may not be implemented on the chip. Read accesses to these addresses will in general return random data, and write accesses will have an indeterminate effect.

User software should not write 1s to these unlisted locations, since they may be used in future products to invoke new features. In that case, the reset or inactive values of the new bits will always be 0.

Timer 2 Registers Control and status bits are contained in registers T2CON (shown in Table 2) and T2MOD (shown in Table 9) for Timer 2. The register pair (RCAP2H, RCAP2L) are the Capture/Reload registers for Timer 2 in 16-bit capture mode or 16-bit auto-reload mode.

Table 1. AT89S8252 SFR Map and Reset Values

0F8H								0FFH
0F0H	B 00000000							0F7H
0E8H								0EFH
0E0H	ACC 00000000							0E7H
0D8H								0DFH
0D0H	PSW 00000000					SPCR 00000100		0D7H
0C8H	T2CON 00000000	T2MOD XXXXXX00	RCAP2L 00000000	RCAP2H 00000000	TL2 00000000	TH2 00000000		0CFH
0C0H								0C7H
0B8H	IP XX000000							0BFH
0B0H	P3 11111111							0B7H
0A8H	IE 0X000000		SPSR 00XXXXXX					0AFH
0A0H	P2 11111111							0A7H
98H	SCON 00000000	SBUF XXXXXXXX						9FH
90H	P1 11111111						WMCON 00000010	97H
88H	TCON 00000000	TMOD 00000000	TL0 00000000	TL1 00000000	TH0 00000000	TH1 00000000		8FH
80H	P0 11111111	SP 00000111	DP0L 00000000	DP0H 00000000	DP1L 00000000	DP1H 00000000	SPDR XXXXXXXX	PCON 0XXX0000
								87H

Table 2. T2CON – Timer/Counter 2 Control Register

T2CON Address = 0C8H — Reset Value = 0000 0000B

Bit Addressable

Bit	TF2	EXF2	RCLK	TCLK	EXEN2	TR2	C/$\overline{T2}$	CP/$\overline{RL2}$
	7	6	5	4	3	2	1	0

Symbol	Function
TF2	Timer 2 overflow flag set by a Timer 2 overflow and must be cleared by software. TF2 will not be set when either RCLK = 1 or TCLK = 1.
EXF2	Timer 2 external flag set when either a capture or reload is caused by a negative transition on T2EX and EXEN2 = 1. When Timer 2 interrupt is enabled, EXF2 = 1 will cause the CPU to vector to the Timer 2 interrupt routine. EXF2 must be cleared by software. EXF2 does not cause an interrupt in up/down counter mode (DCEN = 1).
RCLK	Receive clock enable. When set, causes the serial port to use Timer 2 overflow pulses for its receive clock in serial port Modes 1 and 3. RCLK = 0 causes Timer 1 overflows to be used for the receive clock.
TCLK	Transmit clock enable. When set, causes the serial port to use Timer 2 overflow pulses for its transmit clock in serial port Modes 1 and 3. TCLK = 0 causes Timer 1 overflows to be used for the transmit clock.
EXEN2	Timer 2 external enable. When set, allows a capture or reload to occur as a result of a negative transition on T2EX if Timer 2 is not being used to clock the serial port. EXEN2 = 0 causes Timer 2 to ignore events at T2EX.
TR2	Start/Stop control for Timer 2. TR2 = 1 starts the timer.
C/$\overline{T2}$	Timer or counter select for Timer 2. C/$\overline{T2}$ = 0 for timer function. C/$\overline{T2}$ = 1 for external event counter (falling edge triggered).
CP/$\overline{RL2}$	Capture/Reload select. CP/$\overline{RL2}$ = 1 causes captures to occur on negative transitions at T2EX if EXEN2 = 1. CP/$\overline{RL2}$ = 0 causes automatic reloads to occur when Timer 2 overflows or negative transitions occur at T2EX when EXEN2 = 1. When either RCLK or TCLK = 1, this bit is ignored and the timer is forced to auto-reload on Timer 2 overflow.

Watchdog and Memory Control Register The WMCON register contains control bits for the Watchdog Timer (shown in Table 3). The EEMEN and EEMWE bits are used to select the 2K bytes on-chip EEPROM, and to enable byte-write. The DPS bit selects one of two DPTR registers available.

Table 3. WMCON—Watchdog and Memory Control Register

WMCON Address = 96H — Reset Value = 0000 0010B

Bit	PS2	PS1	PS0	EEMWE	EEMEN	DPS	WDTRST	WDTEN
	7	6	5	4	3	2	1	0

Symbol	Function
PS2 PS1 PS0	Prescaler Bits for the Watchdog Timer. When all three bits are set to "0", the watchdog timer has a nominal period of 16 ms. When all three bits are set to "1", the nominal period is 2048 ms.
EEMWE	EEPROM Data Memory Write Enable Bit. Set this bit to "1" before initiating byte write to on-chip EEPROM with the MOVX instruction. User software should set this bit to "0" after EEPROM write is completed.
EEMEN	Internal EEPROM Access Enable. When EEMEN = 1, the MOVX instruction with DPTR will access on-chip EEPROM instead of external data memory. When EEMEN = 0, MOVX with DPTR accesses external data memory.
DPS	Data Pointer Register Select. DPS = 0 selects the first bank of Data Pointer Register, DP0, and DPS = 1 selects the second bank, DP1
WDTRST RDY/$\overline{BSY}$	Watchdog Timer Reset and EEPROM Ready/$\overline{Busy}$ Flag. Each time this bit is set to "1" by user software, a pulse is generated to reset the watchdog timer. The WDTRST bit is then automatically reset to "0" in the next instruction cycle. The WDTRST bit is Write-Only. This bit also serves as the RDY/$\overline{BSY}$ flag in a Read-Only mode during EEPROM write. RDY/$\overline{BSY}$ = 1 means that the EEPROM is ready to be programmed. While programming operations are being executed, the RDY/$\overline{BSY}$ bit equals "0" and is automatically reset to "1" when programming is completed.
WDTEN	Watchdog Timer Enable Bit. WDTEN = 1 enables the watchdog timer and WDTEN = 0 disables the watchdog timer.

SPI Registers Control and status bits for the Serial Peripheral Interface are contained in registers SPCR (shown in Table 4) and SPSR (shown in Table 5). The SPI data bits are contained in the SPDR register. Writing the SPI data register during serial data transfer sets the Write Collision bit, WCOL, in the SPSR register. The SPDR is double buffered for writing and the values in SPDR are not changed by Reset.

Interrupt Registers The global interrupt enable bit and the individual interrupt enable bits are in the IE register. In addition, the individual interrupt enable bit for the SPI is in the SPCR register. Two priorities can be set for each of the six interrupt sources in the IP register.

Dual Data Pointer Registers To facilitate accessing both internal EEPROM and external data memory, two banks of 16-bit Data Pointer Registers are provided: DP0 at SFR address locations 82H-83H and DP1 at 84H-85H. Bit DPS = 0 in SFR WMCON selects DP0 and DPS = 1 selects DP1. The user should **ALWAYS** initialize the DPS bit to the appropriate value before accessing the respective Data Pointer Register.

Power Off Flag The Power Off Flag (POF) is located at bit_4 (PCON.4) in the PCON SFR. POF is set to "1" during power up. It can be set and reset under software control and is not affected by RESET.

Table 4. SPCR – SPI Control Register

SPCR Address = D5H — Reset Value = 0000 01XXB

Bit	7	6	5	4	3	2	1	0
	SPIE	SPE	DORD	MSTR	CPOL	CPHA	SPR1	SPR0

Symbol	Function
SPIE	SPI Interrupt Enable. This bit, in conjunction with the ES bit in the IE register, enables SPI interrupts: SPIE = 1 and ES = 1 enable SPI interrupts. SPIE = 0 disables SPI interrupts.
SPE	SPI Enable. SPI = 1 enables the SPI channel and connects $\overline{SS}$, MOSI, MISO and SCK to pins P1.4, P1.5, P1.6, and P1.7. SPI = 0 disables the SPI channel.
DORD	Data Order. DORD = 1 selects LSB first data transmission. DORD = 0 selects MSB first data transmission.
MSTR	Master/Slave Select. MSTR = 1 selects Master SPI mode. MSTR = 0 selects Slave SPI mode.
CPOL	Clock Polarity. When CPOL = 1, SCK is high when idle. When CPOL = 0, SCK of the master device is low when not transmitting. Please refer to figure on SPI Clock Phase and Polarity Control.
CPHA	Clock Phase. The CPHA bit together with the CPOL bit controls the clock and data relationship between master and slave. Please refer to figure on SPI Clock Phase and Polarity Control.
SPR0 SPR1	SPI Clock Rate Select. These two bits control the SCK rate of the device configured as master. SPR1 and SPR0 have no effect on the slave. The relationship between SCK and the oscillator frequency, F_{osc}, is as follows: SPR1 SPR0 SCK = F_{osc} divided by 0 0 4 0 1 16 1 0 64 1 1 128

Table 5. SPSR – SPI Status Register

SPSR Address = AAH — Reset Value = 00XX XXXXB

Bit	7	6	5	4	3	2	1	0
	SPIF	WCOL	–	–	–	–	–	–

Symbol	Function
SPIF	SPI Interrupt Flag. When a serial transfer is complete, the SPIF bit is set and an interrupt is generated if SPIE = 1 and ES = 1. The SPIF bit is cleared by reading the SPI status register with SPIF and WCOL bits set, and then reading/writing the SPI data register.
WCOL	Write Collision Flag. The WCOL bit is set if the SPI data register is written during a data transfer. During data transfer, the result of reading the SPDR register may be incorrect, and writing to it has no effect. The WCOL bit (and the SPIF bit) are cleared by reading the SPI status register with SPIF and WCOL set, and then accessing the SPI data register.

Table 6. SPDR – SPI Data Register

SPDR Address = 86H — Reset Value = unchanged

Bit	7	6	5	4	3	2	1	0
	SPD7	SPD6	SPD5	SPD4	SPD3	SPD2	SPD1	SPD0

Data Memory – EEPROM and RAM

The AT89S8252 implements 2K bytes of on-chip EEPROM for data storage and 256 bytes of RAM. The upper 128 bytes of RAM occupy a parallel space to the Special Function Registers. That means the upper 128 bytes have the same addresses as the SFR space but are physically separate from SFR space.

When an instruction accesses an internal location above address 7FH, the address mode used in the instruction specifies whether the CPU accesses the upper 128 bytes of RAM or the SFR space. Instructions that use direct addressing access SFR space.

For example, the following direct addressing instruction accesses the SFR at location 0A0H (which is P2).

```
MOV 0A0H, #data
```

Instructions that use indirect addressing access the upper 128 bytes of RAM. For example, the following indirect addressing instruction, where R0 contains 0A0H, accesses the data byte at address 0A0H, rather than P2 (whose address is 0A0H).

```
MOV @R0, #data
```

Note that stack operations are examples of indirect addressing, so the upper 128 bytes of data RAM are available as stack space.

The on-chip EEPROM data memory is selected by setting the EEMEN bit in the WMCON register at SFR address location 96H. The EEPROM address range is from 000H to 7FFH. The MOVX instructions are used to access the EEPROM. To access off-chip data memory with the MOVX instructions, the EEMEN bit needs to be set to "0".

The EEMWE bit in the WMCON register needs to be set to "1" before any byte location in the EEPROM can be written. User software should reset EEMWE bit to "0" if no further EEPROM write is required. EEPROM write cycles in the serial programming mode are self-timed and typically take 2.5 ms. The progress of EEPROM write can be monitored by reading the RDY/$\overline{BSY}$ bit (read-only) in SFR WMCON. RDY/$\overline{BSY}$ = 0 means

programming is still in progress and RDY/$\overline{BSY}$ = 1 means EEPROM write cycle is completed and another write cycle can be initiated.

In addition, during EEPROM programming, an attempted read from the EEPROM will fetch the byte being written with the MSB complemented. Once the write cycle is completed, true data are valid at all bit locations.

Programmable Watchdog Timer

The programmable Watchdog Timer (WDT) operates from an independent internal oscillator. The prescaler bits, PS0, PS1 and PS2 in SFR WMCON are used to set the period of the Watchdog Timer from 16 ms to 2048 ms. The available timer periods are shown in the following table and the actual timer periods (at V_{CC} = 5V) are within ±30% of the nominal.

The WDT is disabled by Power-on Reset and during Power-down. It is enabled by setting the WDTEN bit in SFR WMCON (address = 96H). The WDT is reset by setting the WDTRST bit in WMCON. When the WDT times out without being reset or disabled, an internal RST pulse is generated to reset the CPU.

Table 7. Watchdog Timer Period Selection

WDT Prescaler Bits			Period (nominal)
PS2	PS1	PS0	
0	0	0	16 ms
0	0	1	32 ms
0	1	0	64 ms
0	1	1	128 ms
1	0	0	256 ms
1	0	1	512 ms
1	1	0	1024 ms
1	1	1	2048 ms

Timer 0 and 1

Timer 0 and Timer 1 in the AT89S8252 operate the same way as Timer 0 and Timer 1 in the AT89C51 and AT89C52. For further information on the timers' operation, refer to the Atmel web site (http://www.atmel.com). From the home page, select "Products", then "Microcontrollers, then "8051-Architecture". Click on "Documentation", then on "Other Documents". Open the document "AT89 Series Hardware Description".

Timer 2

Timer 2 is a 16-bit Timer/Counter that can operate as either a timer or an event counter. The type of operation is selected by bit C/$\overline{T2}$ in the SFR T2CON (shown in Table 2). Timer 2 has three operating modes: capture, auto-reload (up or down counting), and baud rate generator. The modes are selected by bits in T2CON, as shown in Table 8.

Timer 2 consists of two 8-bit registers, TH2 and TL2. In the Timer function, the TL2 register is incremented every machine cycle. Since a machine cycle consists of 12 oscillator periods, the count rate is 1/12 of the oscillator frequency.

In the Counter function, the register is incremented in response to a 1-to-0 transition at its corresponding external input pin, T2. In this function, the external input is sampled during S5P2 of every machine cycle. When the samples show a high in one cycle and a low in the next cycle, the count is incremented. The new count value appears in the register during S3P1 of the cycle following the one in which the transition was detected.

Since two machine cycles (24 oscillator periods) are required to recognize a 1-to-0 transition, the maximum count rate is 1/24 of the oscillator frequency. To ensure that a given level is sampled at least once before it changes, the level should be held for at least one full machine cycle.

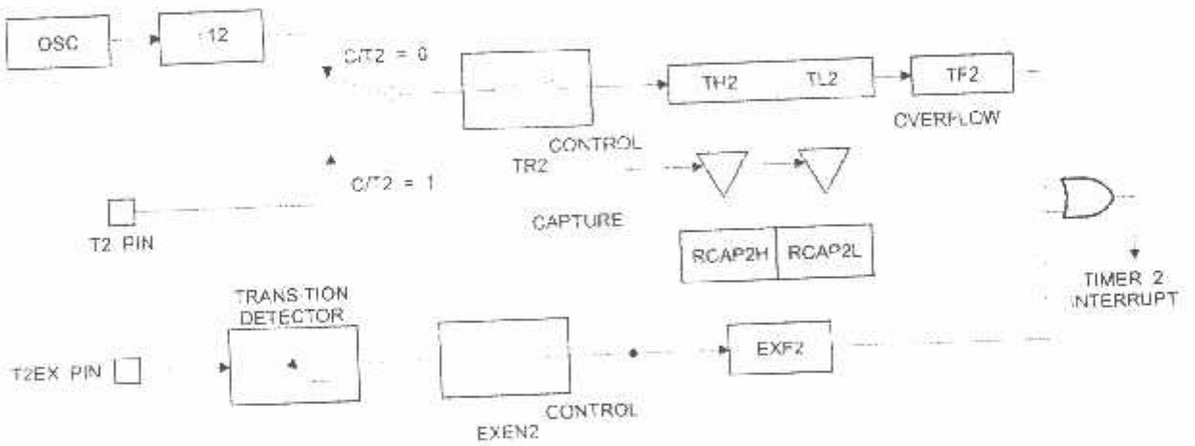
Table 8. Timer 2 Operating Modes

RCLK + TCLK	CP/$\overline{RL2}$	TR2	MODE
0	0	1	16-bit Auto-reload
0	1	1	16-bit Capture
1	X	1	Baud Rate Generator
X	X	0	(Off)

Capture Mode

In the capture mode, two options are selected by bit EXEN2 in T2CON. If EXEN2 = 0, Timer 2 is a 16-bit timer or counter which upon overflow sets bit TF2 in T2CON. This bit can then be used to generate an interrupt. If EXEN2 = 1, Timer 2 performs the same operation, but a 1-to-0 transition at external input T2EX also causes the current value in TH2 and TL2 to be captured into RCAP2H and RCAP2L, respectively. In addition, the transition at T2EX causes bit EXF2 in T2CON to be set. The EXF2 bit, like TF2, can generate an interrupt. The capture mode is illustrated in Figure 1.

Figure 1. Timer 2 in Capture Mode



Auto-reload (Up or Down Counter)

Timer 2 can be programmed to count up or down when configured in its 16-bit auto-reload mode. This feature is invoked by the DCEN (Down Counter Enable) bit located in the SFR T2MOD (see Table 9). Upon reset, the DCEN bit is set to 0 so that timer 2 will default to count up. When DCEN is set, Timer 2 can count up or down, depending on the value of the T2EX pin.

Figure 2 shows Timer 2 automatically counting up when DCEN = 0. In this mode, two options are selected by bit EXEN2 in T2CON. If EXEN2 = 0, Timer 2 counts up to 0FFFFH and then sets the TF2 bit upon overflow. The overflow also causes the timer registers to be reloaded with the 16-bit value in RCAP2H and RCAP2L. The values in RCAP2H and RCAP2L are preset by software. If EXEN2 = 1, a 16-bit reload can be triggered either by an overflow or by a 1-to-0 transition at external input T2EX. This transition also sets the EXF2 bit. Both the TF2 and EXF2 bits can generate an interrupt if enabled.

Setting the DCEN bit enables Timer 2 to count up or down, as shown in Figure 3. In this mode, the T2EX pin controls the direction of the count. A logic 1 at T2EX makes Timer 2 count up. The timer will overflow at 0FFFFH and set the TF2 bit. This overflow also causes the 16-bit value in RCAP2H and RCAP2L to be reloaded into the timer registers, TH2 and TL2, respectively.

A logic 0 at T2EX makes Timer 2 count down. The timer underflows when TH2 and TL2 equal the values stored in RCAP2H and RCAP2L. The underflow sets the TF2 bit and causes 0FFFFH to be reloaded into the timer registers.

The EXF2 bit toggles whenever Timer 2 overflows or underflows and can be used as a 17th bit of resolution. In this operating mode, EXF2 does not flag an interrupt.

Figure 2. Timer 2 in Auto Reload Mode (DCEN = 0)

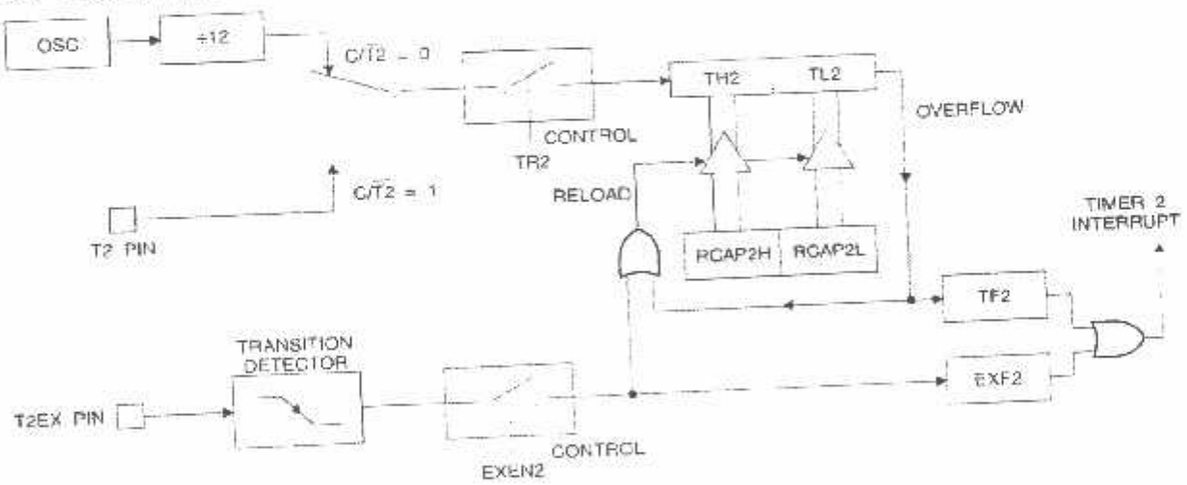


Table 9. T2MOD – Timer 2 Mode Control Register

T2MOD Address = 0C9H — Reset Value = XXXX XX00B

Not Bit Addressable

Bit	7	6	5	4	3	2	1	0
	–	–	–	–	–	–	T2OE	DCEN

Symbol	Function
–	Not implemented, reserved for future use.
T2OE	Timer 2 Output Enable bit.
DCEN	When set, this bit allows Timer 2 to be configured as an up/down counter.

Figure 3. Timer 2 Auto Reload Mode (DCEN = 1)

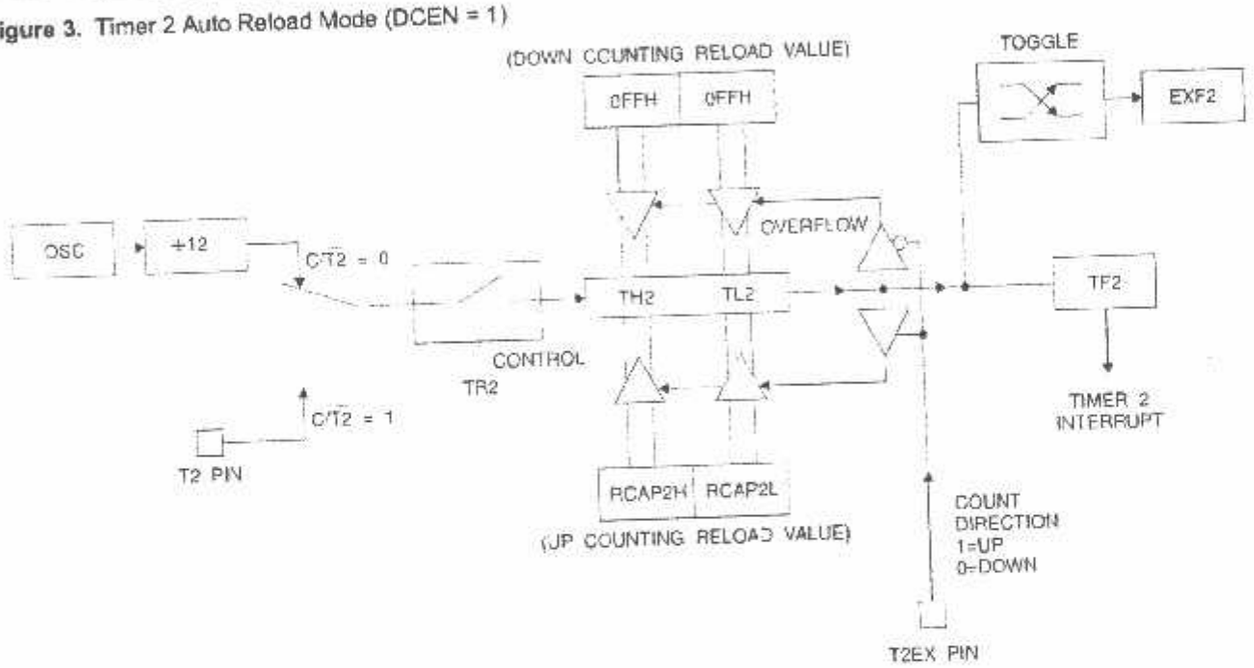
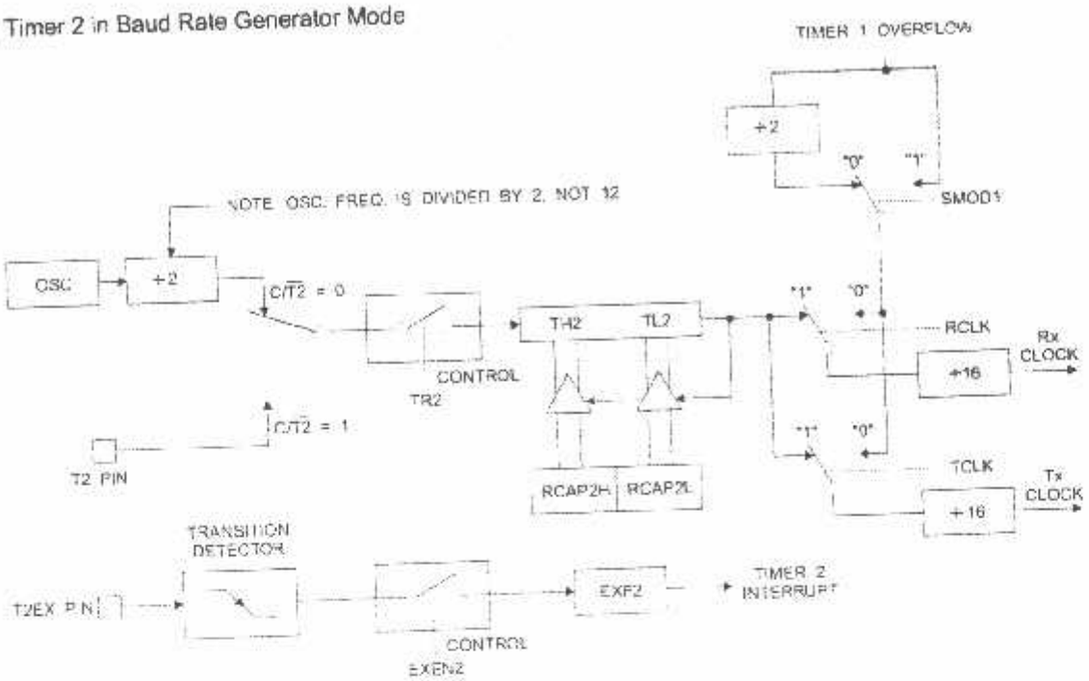


Figure 4. Timer 2 in Baud Rate Generator Mode



Baud Rate Generator

Timer 2 is selected as the baud rate generator by setting TCLK and/or RCLK in T2CON (Table 2). Note that the baud rates for transmit and receive can be different if Timer 2 is used for the receiver or transmitter and Timer 1 is used for the other function. Setting RCLK and/or TCLK puts Timer 2 into its baud rate generator mode, as shown in Figure 4.

The baud rate generator mode is similar to the auto-reload mode, in that a rollover in TH2 causes the Timer 2 registers to be reloaded with the 16-bit value in registers RCAP2H and RCAP2L, which are preset by software.

The baud rates in Modes 1 and 3 are determined by Timer 2's overflow rate according to the following equation.

$$\text{Modes 1 and 3 Baud Rates} = \frac{\text{Timer 2 Overflow Rate}}{16}$$

The Timer can be configured for either timer or counter operation. In most applications, it is configured for timer operation ($C/\overline{T2} = 0$). The timer operation is different for Timer 2 when it is used as a baud rate generator. Normally, as a timer, it increments every machine cycle (at 1/12 the oscillator frequency). As a baud rate generator, however, it increments every state time (at 1/2 the oscillator frequency). The baud rate formula is given below.

$$\frac{\text{Modes 1 and 3}}{\text{Baud Rate}} = \frac{\text{Oscillator Frequency}}{32 \times [65536 - (\text{RCAP2H,RCAP2L})]}$$

where (RCAP2H, RCAP2L) is the content of RCAP2H and RCAP2L taken as a 16-bit unsigned integer.

Timer 2 as a baud rate generator is shown in Figure 4. This figure is valid only if RCLK or TCLK = 1 in T2CON. Note that a rollover in TH2 does not set TF2 and will not generate an interrupt. Note too, that if EXEN2 is set, a 1-to-0 transition in T2EX will set EXF2 but will not cause a reload from (RCAP2H, RCAP2L) to (TH2, TL2). Thus when Timer 2 is in use as a baud rate generator, T2EX can be used as an extra external interrupt.

Note that when Timer 2 is running (TR2 = 1) as a timer in the baud rate generator mode, TH2 or TL2 should not be read from or written to. Under these conditions, the Timer is incremented every state time, and the results of a read or write may not be accurate. The RCAP2 registers may be read but should not be written to, because a write might overlap a reload and cause write and/or reload errors. The timer should be turned off (clear TR2) before accessing the Timer 2 or RCAP2 registers.

Programmable Clock Out

A 50% duty cycle clock can be programmed to come out on P1.0, as shown in Figure 5. This pin, besides being a regular I/O pin, has two alternate functions. It can be programmed to input the external clock for Timer/Counter 2 or to output a 50% duty cycle clock ranging from 61 Hz to 4 MHz (for a 16-MHz operating frequency).

To configure the Timer/Counter 2 as a clock generator, bit C/$\overline{T2}$ (T2CON.1) must be cleared and bit T2OE (T2MOD.1) must be set. Bit TR2 (T2CON.2) starts and stops the timer.

The clock-out frequency depends on the oscillator frequency and the reload value of Timer 2 capture registers (RCAP2H, RCAP2L), as shown in the following equation.

$$\text{Clock Out Frequency} = \frac{\text{Oscillator Frequency}}{4 \times [65536 - (\text{RCAP2H,RCAP2L})]}$$

In the clock-out mode, Timer 2 rollovers will not generate an interrupt. This behavior is similar to when Timer 2 is used as a baud-rate generator. It is possible to use Timer 2 as a baud-rate generator and a clock generator simultaneously. Note, however, that the baud-rate and clock-out frequencies cannot be determined independently from one another since they both use RCAP2H and RCAP2L.

Figure 5. Timer 2 in Clock-out Mode

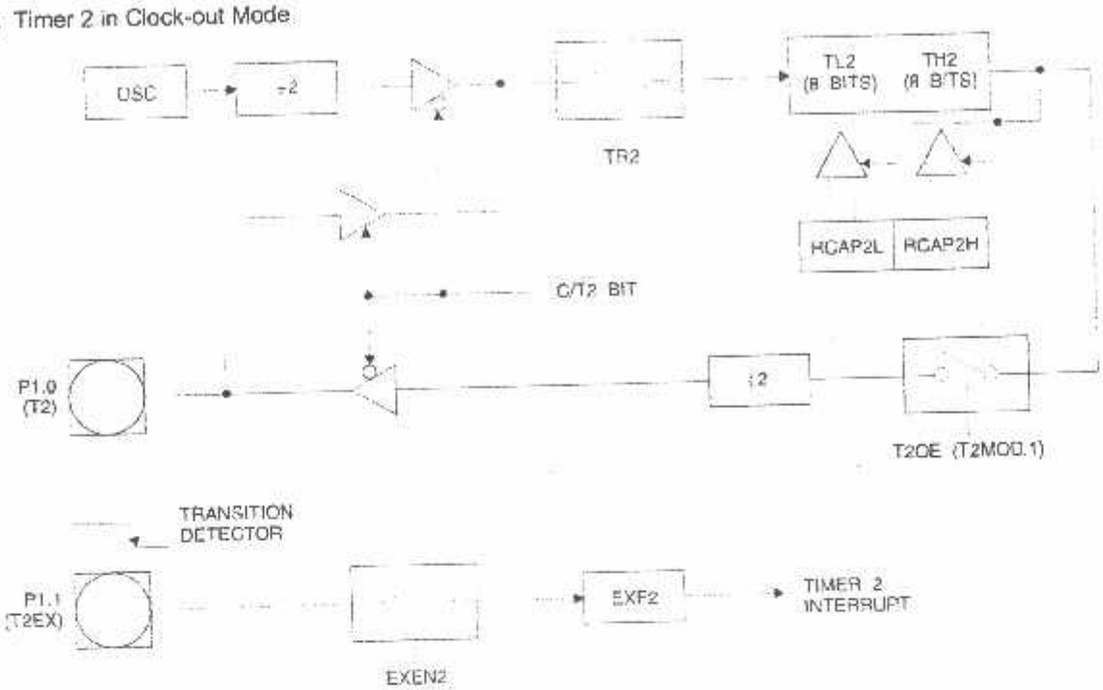
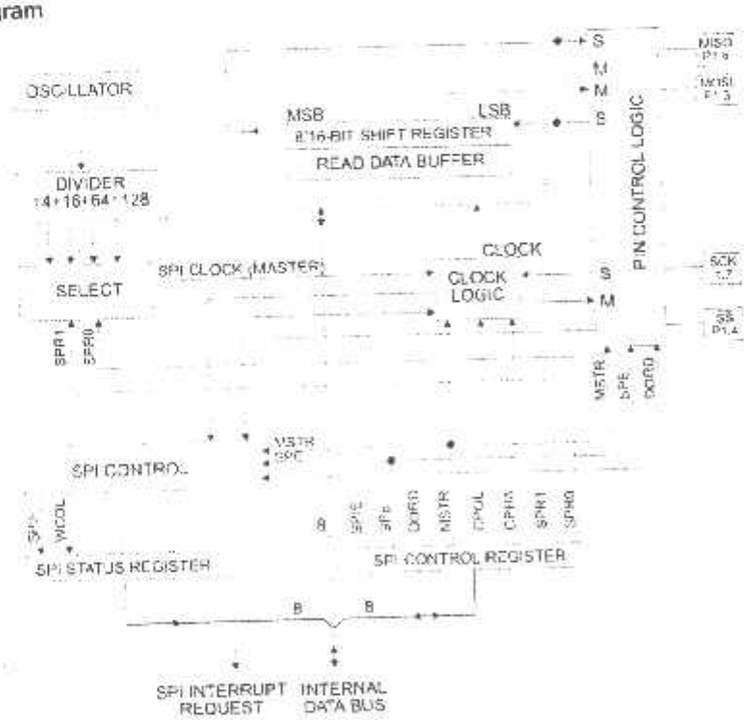


Figure 6. SPI Block Diagram



JART

The UART in the AT89S8252 operates the same way as the UART in the AT89C51 and AT89C52. For further information on the UART operation, refer to the Atmel web site (http://www.atmel.com). From the home page, select "Products", then "Microcontrollers, then "8051-Architecture". Click on "Documentation", then on "Other Documents". Open the document "AT89 Series Hardware Description".

Serial Peripheral nterface

The serial peripheral interface (SPI) allows high-speed synchronous data transfer between the AT89S8252 and peripheral devices or between several AT89S8252 devices. The AT89S8252 SPI features include the following:

- Full-Duplex, 3-Wire Synchronous Data Transfer
- Master or Slave Operation
- 1.5 MHz Bit Frequency (max.)
- LSB First or MSB First Data Transfer
- Four Programmable Bit Rates
- End of Transmission Interrupt Flag
- Write Collision Flag Protection
- Wakeup from Idle Mode (Slave Mode Only)

The interconnection between master and slave CPUs with SPI is shown in the following figure. The SCK pin is the clock output in the master mode but is the clock input in the slave mode. Writing to the SPI data register of the master CPU starts the SPI clock generator, and the data written shifts out of the MOSI pin and into the MOSI pin of the slave CPU. After shifting one byte, the SPI clock generator stops, setting the end of transmission flag (SPIF). If both the SPI interrupt enable bit (SPIE) and the serial port interrupt enable bit (ES) are set, an interrupt is requested.

The Slave Select input, $\overline{SS}$/P1.4, is set low to select an individual SPI device as a slave. When $\overline{SS}$/P1.4 is set high, the SPI port is deactivated and the MOSI/P1.5 pin can be used as an input.

There are four combinations of SCK phase and polarity with respect to serial data which are determined by control bits CPHA and CPOL. The SPI data transfer formats are shown in Figure 8 and Figure 9.

Figure 7. SPI Master-slave Interconnection

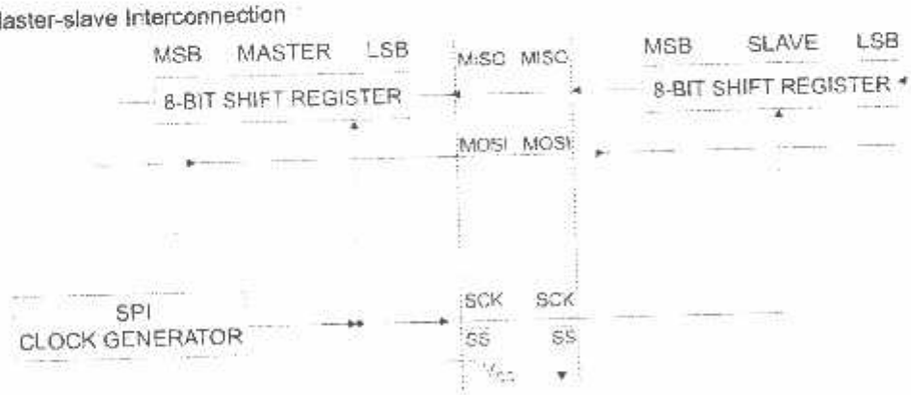
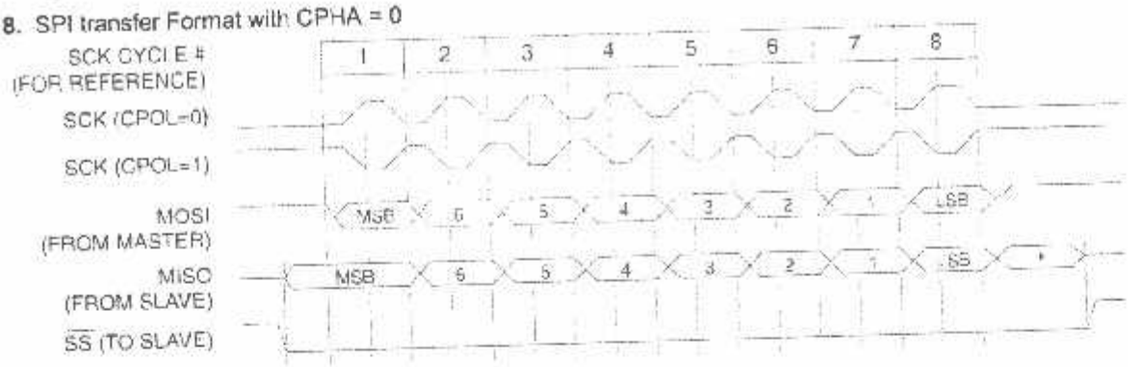
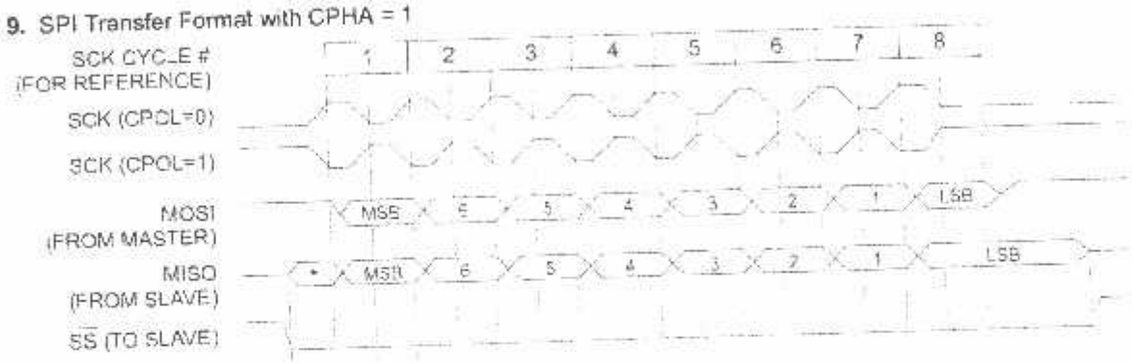


Figure 8. SPI transfer Format with CPHA = 0



Note: *Not defined but normally MSB of character just received

Figure 9. SPI Transfer Format with CPHA = 1



Note: *Not defined but normally LSB of previously transmitted character.

nterrupts

The AT89S8252 has a total of six interrupt vectors: two external interrupts ($\overline{INT0}$ and $\overline{INT1}$), three timer interrupts (Timers 0, 1, and 2), and the serial port interrupt. These interrupts are all shown in Figure 10.

Each of these interrupt sources can be individually enabled or disabled by setting or clearing a bit in Special Function Register IE. IE also contains a global disable bit, EA, which disables all interrupts at once.

Note that Table 10 shows that bit position IE.6 is unimplemented. In the AT89C51, bit position IE.5 is also unimplemented. User software should not write 1s to these bit positions, since they may be used in future AT89 products.

Timer 2 interrupt is generated by the logical OR of bits TF2 and EXF2 in register T2CON. Neither of these flags is cleared by hardware when the service routine is vectored to. In fact, the service routine may have to determine whether it was TF2 or EXF2 that generated the interrupt, and that bit will have to be cleared in software.

The Timer 0 and Timer 1 flags, TF0 and TF1, are set at S5P2 of the cycle in which the timers overflow. The values are then polled by the circuitry in the next cycle. However, the Timer 2 flag, TF2, is set at S2P2 and is polled in the same cycle in which the timer overflows.

Table 10. Interrupt Enable (IE) Register

(MSB)(LSB)

EA	-	ET2	ES	ET1	EX1	ET0	EX0

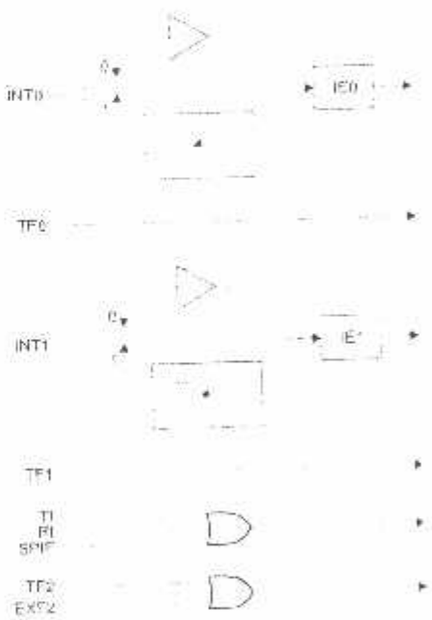
Enable Bit = 1 enables the interrupt.

Enable Bit = 0 disables the Interrupt.

Symbol	Position	Function
EA	IE.7	Disables all interrupts. If EA = 0, no interrupt is acknowledged. If EA = 1, each interrupt source is individually enabled or disabled by setting or clearing its enable bit.
-	IE.6	Reserved.
ET2	IE.5	Timer 2 interrupt enable bit.
ES	IE.4	SPI and UART interrupt enable bit.
ET1	IE.3	Timer 1 interrupt enable bit.
EX1	IE.2	External interrupt 1 enable bit.
ET0	IE.1	Timer 0 interrupt enable bit.
EX0	IE.0	External interrupt 0 enable bit.

User software should never write 1s to unimplemented bits, because they may be used in future AT89 products.

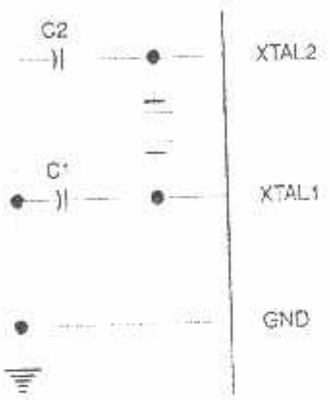
Figure 10. Interrupt Sources



Oscillator Characteristics

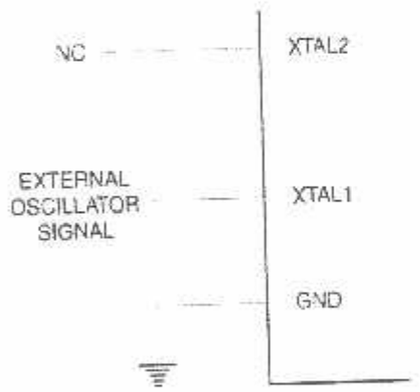
XTAL1 and XTAL2 are the input and output, respectively, of an inverting amplifier that can be configured for use as an on-chip oscillator, as shown in Figure 11. Either a quartz crystal or ceramic resonator may be used. To drive the device from an external clock source, XTAL2 should be left unconnected while XTAL1 is driven, as shown in Figure 12. There are no requirements on the duty cycle of the external clock signal, since the input to the internal clocking circuitry is through a divide-by-two flip-flop, but minimum and maximum voltage high and low time specifications must be observed.

Figure 11. Oscillator Connections



Note: C1, C2 = 30 pF ± 10 pF for Crystals
= 40 pF ± 10 pF for Ceramic Resonators

Figure 12. External Clock Drive Configuration



BAB IV

ANALISA DAN PENGUJIAN ALAT

4.1. Tujuan

Bab ini membahas tentang analisis dan pengujian alat yang telah dibuat. Secara umum, pengujian ini bertujuan untuk mengetahui apakah alat yang telah direalisasikan dapat bekerja sesuai dengan spesifikasi perencanaan yang telah ditetapkan. Pengujian alat ini meliputi pengujian perangkat keras dan pengujian perangkat lunak. Pengujian dilakukan pada masing-masing blok terlebih dahulu, yang selanjutnya dilakukan pengujian untuk sistem secara keseluruhan. Adapun pengujian terhadap perangkat keras meliputi pengujian terhadap mikrokontroller, RS232, IC FSK XR2206 dan FSK XR2211, LCD dan keypad.

4.2. Pengujian Sistem Mikrokontroller.

- **Tujuan**

  Untuk mengetahui kondisi awal dari mikrokontroller apakah sudah sesuai dengan yang telah direncanakan.

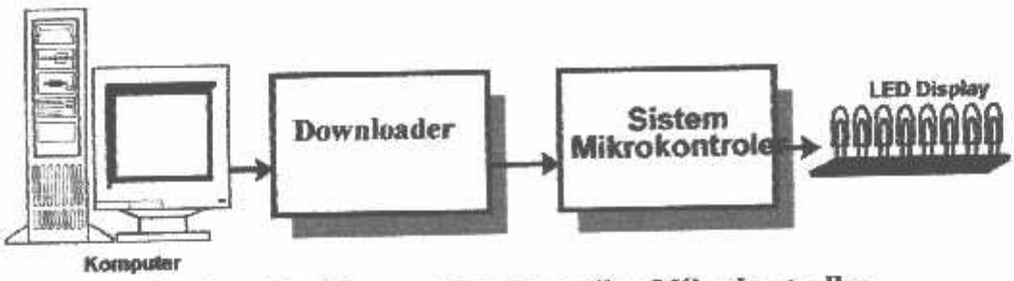
- **Prosedur Pengujian**

1. Membuat program yang digunakan dalam pengujian mikrokontroller.

   Program yang digunakan dalam pengujian mikrokontroller ini merupakan program sederhana yang meletakkan $0F_H$ dan $F0_H$ pada ACC secara bergantian kemudian memindahkannya pada *Port* 1 AT89S8252. Program yang dibuat adalah sebagai berikut :

```
        ORG     0000H
        JMP     START
START:  MOV     A,#0FH
        MOV     P1,A
        CALL    TUNDA
        MOV     A,#F0H
        MOV     P1,A
        JMP     START
TUNDA:  MOV     R3,#0FFH
TUNDA1: MOV     R2,#0FFH
        DJNZ    R2,$
        MOV     R1,#0FH
        DJNZ    R1,$
        DJNZ    R3,TUNDA1
        RET
        END
```

2. Rangkaian dibuat seperti Gambar 4.1.
3. Memasang catu daya rangkaian sebesar 5 Volt DC
4. Download program diatas.
5. Mengamati keluaran pada LED Display .



Gambar 4.1. Diagram blok Pengujian Mikrokontroller

➢ **Hasil Pengujian**

Hasil pengujian pada sistem mikrokontroller ditunjukkan dalam Tabel 4.1. dibawah ini :

Tabel 4.1. Hasil Pengujian Sistem Mikrokontroller

Kondisi	Keluaran pada LED Display							
	Bit 0	Bit 1	Bit 2	Bit 3	Bit 4	Bit 5	Bit 6	Bit 7
Satu	1	1	1	1	0	0	0	0
Dua	0	0	0	0	1	1	1	1

➢ **Analisis Pengujian**

Dari hasil pengujian dalam tabel 4.1. dapat dilihat bahwa *port* 1 memberikan logika $0F_H$ dan $F0_H$ secara bergantian sesuai dengan isi program.

4.3. Pengujian Komunikasi Serial

➢ **Tujuan**

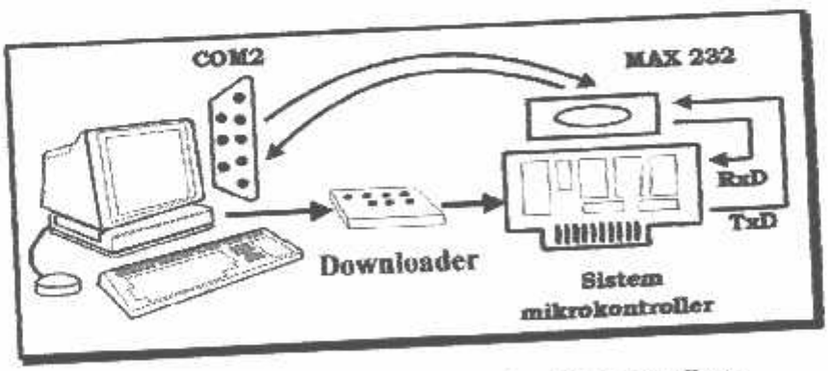
Untuk mengetahui apakah data yang dikirim dari MCU ke *PC* dapat diterima dengan benar dengan melakukan simulasi pada komputer.

➢ **Peralatan yang digunakan**

- Komputer
- Sistem mikrokontroller dengan antarmuka RS-232.

➢ **Prosedur pengujian**

1. Menyusun rangkaian seperti pada Gambar 4.2.
2. Membuat program transfer data pada sistem mikrokontroller seperti yang ditunjukkan dalam Gambar 4.3. dan Gambar 4.4. Dengan program tersebut komputer mengirim data '1234567890' ke alat dan oleh alat akan dikembalikan lagi ke komputer.
3. Download program ke mikrokontroller dan eksekusi program.
4. Mencatat hasil yang terlihat dalam layar komputer.



Gambar 4.2. Rangkaian Pengujian Transfer Data

```
PCON    EQU   87H
        ORG   0000H
        JMP   MULAI
        ORG   0023H
MULAI:
        CALL  INIT232
        CALL  SERIAL
        JMP   MULAI
SERIAL: JBC   TI,OUT232
        PUSH  ACC
        MOV   A,SBUF
        MOV   SBUF,A
        POP   ACC
OUT232: CLR   TI
        CLR   RI
        RETI
INIT232: MOV  TH1,#B1200
        MOV   TMOD,#22H
        ANL   PCON,#7FH
        MOV   SCON,#50H
        SETB  PS
        SETB  ES
```

Gambar 4.3. Program Uji Komunikasi Data di Mikrokontroller

```
' Cuplikan program uji komunikasi data di komputer menggunakan program
VB 6.0

MSComm1.Output = '1234567890'

Text1.Text = MSComm1.Input
```

Gambar 4.4. Program Uji Komunikasi Data di Komputer

➢ **Hasil Pengujian**

Hasil pengujian transfer data serial ini ditunjukkan Tabel 4.2. dibawah ini :

Tabel 4.2. Hasil Pengujian Transfer Data Serial

Data yang dikirim komputer	Data yang diterima komputer
1234567890	1234567890

➢ **Analisis Hasil Pengujian**

Hasil pengujian dalam Tabel 4.2. menunjukkan bahwa proses pengiriman data serial dengan menggunakan RS-232 ke alat telah benar.

4.4. Pengujian Rangkaian IC FSK XR2206 dan IC FSK XR 2211

➢ **Tujuan**

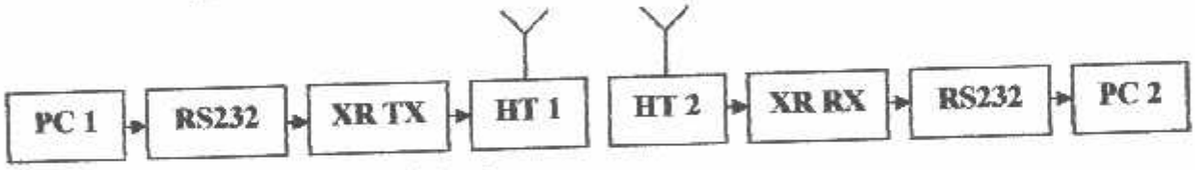
- Untuk mengetahui frekuensi TX pada IC XR2206
- Untuk mengetahui RX pada IC XR2211 bisa menerima data dari TX XR2206.

➢ **Peralatan yang digunakan**

- Obeng untuk pengesetan frekuensi
- Frekuensi Counter
- Komputer 1 dan komputer 2
- Catu daya 5 Volt DC untuk RS232
  dan 12 Volt DC untuk XR2206 dan XR2211

➢ **Prosedur Pengujian**

1. Setting tegangan pada XR2206 TX pada frekuensi 1200 Hz untuk High dan frekuensi 2200 Hz untuk Low.
2. Input XR TX dihubungkan dengan RS232 TX.
3. Output XR TX dihubungkan dengan terminal Mic HT.
4. Input XR RX dihubungkan dengan RS232 RX.
5. Output XR RX dihubungkan dengan terminal Speak pada HT.
6. RS232 dihubungkan ke masing-masing komputer.
7. Kirim data dari MSCOMM dengan BoudRate 1200 bps pada PC 1.
8. Set XR2211 RX sampai bisa terima data yang sesuai dengan data yang dikirim oleh PC 1.



Keterangan : PC 1 sebagai Kirim dan

PC 2 sebagai Terima

Gambar 4.5. Diagram blok pengujian TX XR2206 dan RX XR2211

➢ **Hasil Pengujian**

Hasil pengujian TX XR2206 dan RX XR2211 ini ditunjukkan Tabel 4.2. dibawah ini :

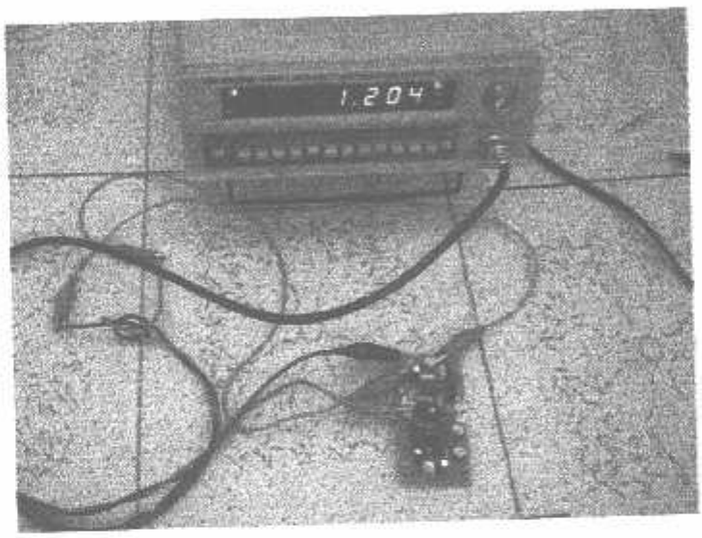
Tabel 4.3. Hasil Pengujian TX XR2206 dan RX XR2211 pada PC

Data yang dikirim komputer	Data yang diterima komputer
1234567890	1234567890

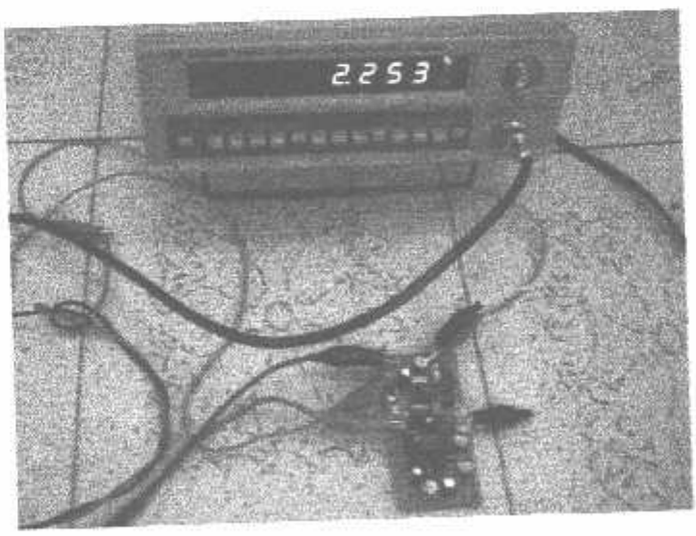
- **Analisis Hasil Pengujian**

  Hasil pengujian dalam Tabel 4.3. menunjukkan bahwa proses pengiriman data serial dari TX XR2206 ke RX XR2211 telah benar dan stabil.

- **Berikut merupakan gambar dari hasil pengujian frekuensi 1200 Hz dan frekuensi 2200 Hz :**



Gambar 4.6. Pengujian Frekuensi 1200 Hz atau High "1".



Gambar 4.7. Pengujian Frekuensi 2200 Hz atau Low "0".

4.5. Pengujian Rangkaian Papan Tombol (*Keypad*)

➢ **Tujuan**

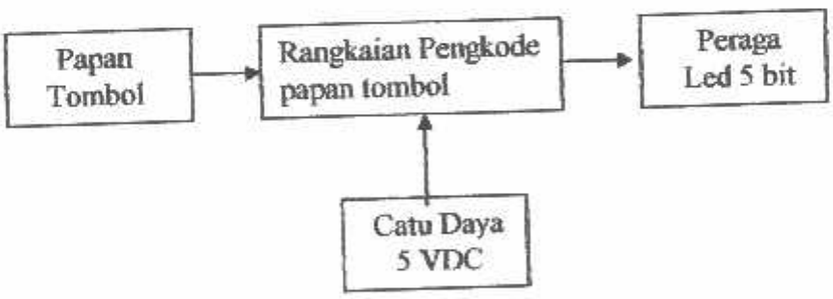
Untuk mengetahui apakah rangkaian ini dapat mengkodekan tombol-tombol input keypad yang ditekan menjadi data 4 bit yang bersesuaian.

➢ **Peralatan yang digunakan**

- Papan Tombol (*keypad* 3x4)
- Rangkaian pengkode *keypad*
- Peraga led 5 bit
- Catu daya 5 Volt DC

➢ **Prosedur Pengujian**

1. Peralatan dirangkai seperti pada gambar 4.8.
2. Menekan tombol pada papan tombol, mengamati dan mencatat keluaran yang ditampilkan ke peraga led 5 bit



Gambar 4.8. Diagram blok pengujian pengkode papan tombol (*keypad*)

Idle Mode

In idle mode, the CPU puts itself to sleep while all the on-chip peripherals remain active. The mode is invoked by software. The content of the on-chip RAM and all the special functions registers remain unchanged during this mode. The idle mode can be terminated by any enabled interrupt or by a hardware reset.

Note that when idle mode is terminated by a hardware reset, the device normally resumes program execution from where it left off, up to two machine cycles before the internal reset algorithm takes control. On-chip hardware inhibits access to internal RAM in this event, but access to the port pins is not inhibited. To eliminate the possibility of an unexpected write to a port pin when idle mode is terminated by a reset, the instruction following the one that invokes idle mode should not write to a port pin or to external memory.

Status of External Pins During Idle and Power-down Modes

Mode	Program Memory	ALE	PSEN	PORT0	PORT1	PORT2	PORT3
Idle	Internal	1	1	Data	Data	Data	Data
Idle	External	1	1	Float	Data	Address	Data
Power-down	Internal	0	0	Data	Data	Data	Data
Power-down	External	0	0	Float	Data	Data	Data

Power-down Mode

In the power-down mode, the oscillator is stopped and the instruction that invokes power-down is the last instruction executed. The on-chip RAM and Special Function Registers retain their values until the power-down mode is terminated. Exit from power-down can be initiated either by a hardware reset or by an enabled external interrupt. Reset redefines the SFRs but does not change the on-chip RAM. The reset should not be activated before V_{CC} is restored to its normal operating level and must be held active long enough to allow the oscillator to restart and stabilize.

To exit power-down via an interrupt, the external interrupt must be enabled as level sensitive before entering power-down. The interrupt service routine starts at 16 ms (nominal) after the enabled interrupt pin is activated.

Program Memory Lock Bits

The AT89S8252 has three lock bits that can be left unprogrammed (U) or can be programmed (P) to obtain the additional features listed in the following table.

When lock bit 1 is programmed, the logic level at the $\overline{EA}$ pin is sampled and latched during reset. If the device is powered up without a reset, the latch initializes to a random value and holds that value until reset is activated. The latched value of $\overline{EA}$ must agree with the current logic level at that pin in order for the device to function properly.

Once programmed, the lock bits can only be unprogrammed with the Chip Erase operations in either the parallel or serial modes.

Lock Bit Protection Modes[1,2]

	Program Lock Bits			
	LB1	LB2	LB3	Protection Type
1	U	U	U	No internal memory lock feature.
2	P	U	U	MOVC instructions executed from external program memory are disabled from fetching code bytes from internal memory. $\overline{EA}$ is sampled and latched on reset and further programming of the Flash memory (parallel or serial mode) is disabled.
3	P	P	U	Same as Mode 2, but parallel or serial verify are also disabled.
4	P	P	P	Same as Mode 3, but external execution is also disabled.

Notes: 1. U = Unprogrammed
2. P = Programmed

Programming the Flash and EEPROM

Atmel's AT89S8252 Flash Microcontroller offers 8K bytes of in-system reprogrammable Flash Code memory and 2K bytes of EEPROM Data memory.

The AT89S8252 is normally shipped with the on-chip Flash Code and EEPROM Data memory arrays in the erased state (i.e. contents = FFH) and ready to be programmed. This device supports a High-voltage (12-V V_{PP}) Parallel programming mode and a Low-voltage (5-V V_{CC}) Serial programming mode. The serial programming mode provides a convenient way to reprogram the AT89S8252 inside the user's system. The parallel programming mode is compatible with conventional third party Flash or EPROM programmers.

The Code and Data memory arrays are mapped via separate address spaces in the serial programming mode. In the parallel programming mode, the two arrays occupy one contiguous address space: 0000H to 1FFFH for the Code array and 2000H to 27FFH for the Data array.

The Code and Data memory arrays on the AT89S8252 are programmed byte-by-byte in either programming mode. An auto-erase cycle is provided with the self-timed programming operation in the serial programming mode. There is no need to perform the Chip Erase operation to reprogram any memory location in the serial programming mode unless any of the lock bits have been programmed.

In the parallel programming mode, there is no auto-erase cycle. To reprogram any non-blank byte, the user needs to use the Chip Erase operation first to erase both arrays.

Parallel Programming Algorithm: To program and verify the AT89S8252 in the parallel programming mode, the following sequence is recommended:

1. Power-up sequence:
   Apply power between V_{CC} and GND pins.
   Set RST pin to "H".
   Apply a 3 MHz to 24 MHz clock to XTAL1 pin and wait for at least 10 milliseconds.
2. Set $\overline{PSEN}$ pin to "L"
   ALE pin to "H"
   $\overline{EA}$ pin to "H" and all other pins to "H".
3. Apply the appropriate combination of "H" or "L" logic levels to pins P2.6, P2.7, P3.6, P3.7 to select one of the programming operations shown in the Flash Programming Modes table.
4. Apply the desired byte address to pins P1.0 to P1.7 and P2.0 to P2.5.
   Apply data to pins P0.0 to P0.7 for Write Code operation.
5. Raise $\overline{EA}/V_{PP}$ to 12V to enable Flash programming, erase or verification.
6. Pulse ALE/$\overline{PROG}$ once to program a byte in the Code memory array, the Data memory array or the lock bits. The byte-write cycle is self-timed and typically takes 1.5 ms.
7. To verify the byte just programmed, bring pin P2.7 to "L" and read the programmed data at pins P0.0 to P0.7.
8. Repeat steps 3 through 7 changing the address and data for the entire 2K or 8K bytes array or until the end of the object file is reached.
9. Power-off sequence:
   Set XTAL1 to "L".
   Set RST and $\overline{EA}$ pins to "L".
   Turn V_{CC} power off.

In the parallel programming mode, there is no auto-erase cycle and to reprogram any non-blank byte, the user needs to use the Chip Erase operation first to erase both arrays.

Data Polling: The AT89S8252 features DATA Polling to indicate the end of a byte write cycle. During a byte write cycle in the parallel or serial programming mode, an attempted read of the last byte written will result in the complement of the written datum on P0.7 (parallel mode), and on the MSB of the serial output byte on MISO (serial mode). Once the write cycle has been completed, true data are valid on all outputs, and the next cycle may begin. DATA Polling may begin any time after a write cycle has been initiated.

Ready/Busy: The progress of byte programming in the parallel programming mode can also be monitored by the RDY/BSY output signal. Pin P3.4 is pulled Low after ALE goes High during programming to indicate BUSY. P3.4 is pulled High again when programming is done to indicate READY.

Program Verify: If lock bits LB1 and LB2 have not been programmed, the programmed Code or Data byte can be read back via the address and data lines for verification. The state of the lock bits can also be verified directly in the parallel programming mode. In the serial programming mode, the state of the lock bits can only be verified indirectly by observing that the lock bit features are enabled.

Chip Erase: Both Flash and EEPROM arrays are erased electrically at the same time. In the parallel programming mode, chip erase is initiated by using the proper combination of control signals and by holding ALE/PROG low for 10 ms. The Code and Data arrays are written with all "1"s in the Chip Erase operation.

In the serial programming mode, a chip erase operation is initiated by issuing the Chip Erase instruction. In this mode, chip erase is self-timed and takes about 16 ms.

During chip erase, a serial read from any address location will return 00H at the data outputs.

Serial Programming Fuse: A programmable fuse is available to disable Serial Programming if the user needs maximum system security. The Serial Programming Fuse can only be programmed or erased in the Parallel Programming Mode.

The AT89S8252 is shipped with the Serial Programming Mode enabled.

Reading the Signature Bytes: The signature bytes are read by the same procedure as a normal verification of locations 030H and 031H, except that P3.6 and P3.7 must be pulled to a logic low. The values returned are as follows:

(030H) = 1EH indicates manufactured by Atmel
(031H) = 72H indicates 89S8252

Programming Interface

Every code byte in the Flash and EEPROM arrays can be written, and the entire array can be erased, by using the appropriate combination of control signals. The write operation cycle is self-timed and once initiated, will automatically time itself to completion.

Most worldwide major programming vendors offer support for the Atmel AT89 microcontroller series. Please contact your local programming vendor for the appropriate software revision.

Serial Downloading

Both the Code and Data memory arrays can be programmed using the serial SPI bus while RST is pulled to V_{CC}. The serial interface consists of pins SCK, MOSI (input) and MISO (output). After RST is set high, the Programming Enable instruction needs to be executed first before program/erase operations can be executed.

An auto-erase cycle is built into the self-timed programming operation (in the serial mode ONLY) and there is no need to first execute the Chip Erase instruction unless any of the lock bits have been programmed. The Chip Erase operation turns the content of every memory location in both the Code and Data arrays into FFH.

The Code and Data memory arrays have separate address spaces:

0000H to 1FFFH for Code memory and 000H to 7FFH for Data memory.

Either an external system clock is supplied at pin XTAL1 or a crystal needs to be connected across pins XTAL1 and XTAL2. The maximum serial clock (SCK) frequency should be less than 1/40 of the crystal frequency. With a 24 MHz oscillator clock, the maximum SCK frequency is 600 kHz.

Serial Programming Algorithm

To program and verify the AT89S8252 in the serial programming mode, the following sequence is recommended:

1. Power-up sequence:

   Apply power between VCC and GND pins.

   Set RST pin to "H".

   If a crystal is not connected across pins XTAL1 and XTAL2, apply a 3 MHz to 24 MHz clock to XTAL1 pin and wait for at least 10 milliseconds.
2. Enable serial programming by sending the Programming Enable serial instruction to pin MOSI/P1.5. The frequency of the shift clock supplied at pin SCK/P1.7 needs to be less than the CPU clock at XTAL1 divided by 40.
3. The Code or Data array is programmed one byte at a time by supplying the address and data together with the appropriate Write instruction. The selected memory location is first automatically erased before new data is written. The write cycle is self-timed and typically takes less than 2.5 ms at 5V.
4. Any memory location can be verified by using the Read instruction which returns the content at the selected address at serial output MISO/P1.6.
5. At the end of a programming session, RST can be set low to commence normal operation.
6. Power-off sequence (if needed):

   Set XTAL1 to "L" (if a crystal is not used).

   Set RST to "L".

   Turn V_{CC} power off.

Serial Programming Instruction

The Instruction Set for Serial Programming follows a 3-byte protocol and is shown in the following table.

Instruction Set

Instruction	Input Format			Operation
	Byte 1	Byte 2	Byte 3	
Programming Enable	1010 1100	0101 0011	xxxx xxxx	Enable serial programming interface after RST goes high.
Chip Erase	1010 1100	xxxx x100	xxxx xxxx	Chip erase both 8K & 2K memory arrays.
Read Code Memory	aaaa a001	low addr	xxxx xxxx	Read data from Code memory array at the selected address. The 5 MSBs of the first byte are the high order address bits. The low order address bits are in the second byte. Data are available at pin MISO during the third byte.
Write Code Memory	aaaa a010	low addr	data in	Write data to Code memory location at selected address. The address bits are the 5 MSBs of the first byte together with the second byte.
Read Data Memory	00aa a101	low addr	xxxx xxxx	Read data from Data memory array at selected address. Data are available at pin MISO during the third byte.
Write Data Memory	00aa a110	low addr	data in	Write data to Data memory location at selected address.
Write Lock Bits	1010 1100	LB1 LB2 LB3 x x111	xxxx xxxx	Write lock bits. Set LB1, LB2 or LB3 = "0" to program lock bits.

Notes:
1. DATA polling is used to indicate the end of a byte write cycle which typically takes less than 2.5 ms at 5V.
2. "aaaaa" = high order address.
3. "x" = don't care.

Flash and EEPROM Parallel Programming Modes

Mode	RST	$\overline{PSEN}$	ALE/$\overline{PROG}$	$\overline{EA}/V_{PP}$	P2.6	P2.7	P3.6	P3.7	Data I/O P0.7:0	Address P2.5:0 P1.7:0
Serial Prog. Modes	H	h(1)	h(1)	x						
Chip Erase	H	L	⌐‾⌐ (2)	12V	H	L	L	L	X	X
Write (10K bytes) Memory	H	L	⌐‾⌐	12V	L	H	H	H	DIN	ADDR
Read (10K bytes) Memory	H	L	H	12V	L	L	H	H	DOUT	ADDR
Write Lock Bits:	H	L	⌐‾⌐	12V	H	H	H	L	DIN	X
Bit - 1									P0.7 = 0	X
Bit - 2									P0.6 = 0	X
Bit - 3									P0.5 = 0	X
Read Lock Bits:	H	L	H	12V	H	H	L	L	DOUT	X
Bit - 1									@P0.2	X
Bit - 2									@P0.1	X
Bit - 3									@P0.0	X
Read Atmel Code	H	L	H	12V	L	L	L	L	DOUT	30H
Read Device Code	H	L	H	12V	L	L	L	L	DOUT	31H
Serial Prog. Enable	H	L	⌐‾⌐ (2)	12V	L	H	L	H	P0.0 = 0	X
Serial Prog. Disable	H	L	⌐‾⌐ (2)	12V	L	H	L	H	P0.0 = 1	X
Read Serial Prog. Fuse	H	L	H	12V	H	H	L	H	@P0.0	X

Notes:
1. "h" = weakly pulled "High" internally.
2. Chip Erase and Serial Programming Fuse require a 10 ms $\overline{PROG}$ pulse. Chip Erase needs to be performed first before reprogramming any byte with a content other than FFH.
3. P3.4 is pulled Low during programming to indicate RDY/$\overline{BSY}$.
4. "X" = don't care

Figure 13. Programming the Flash/EEPROM Memory

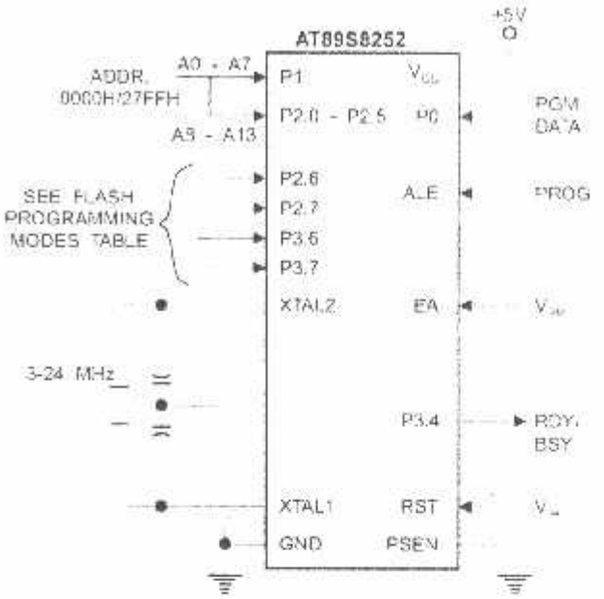


Figure 14. Verifying the Flash/EEPROM Memory

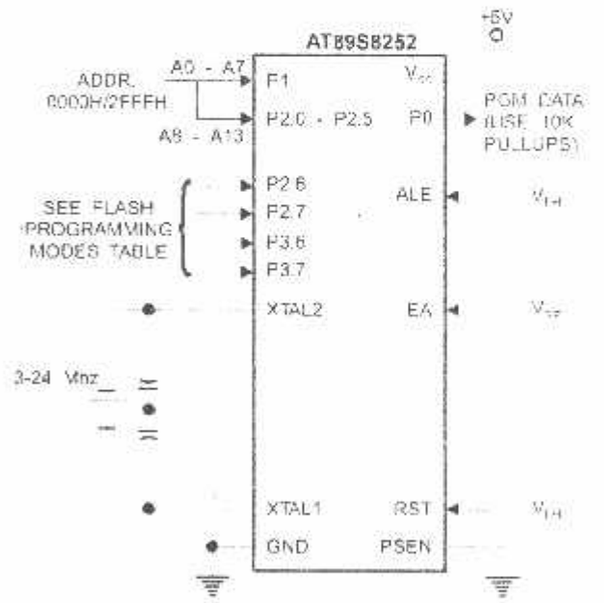
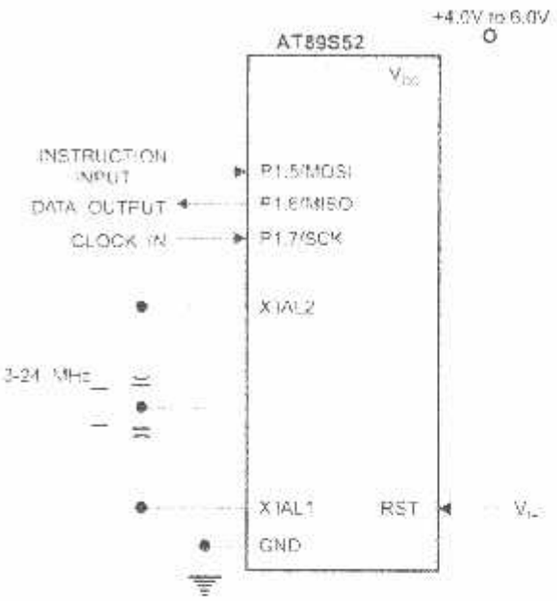


Figure 15. Flash/EEPROM Serial Downloading

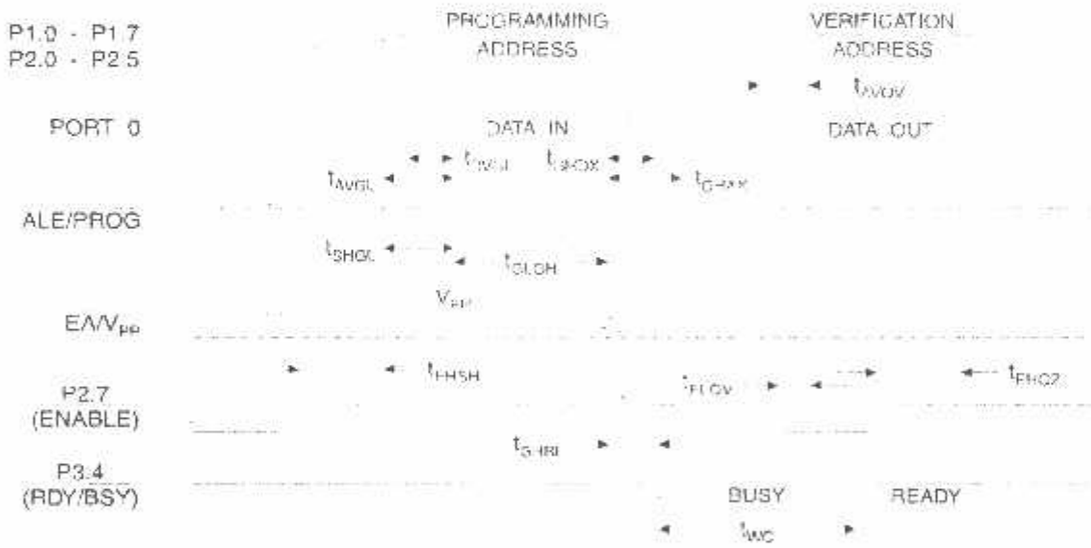


Flash Programming and Verification Characteristics – Parallel Mode

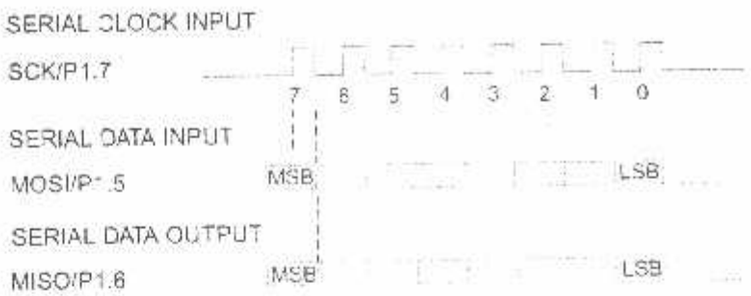
T_A = 0°C to 70°C, V_{CC} = 5.0V ±10%

Symbol	Parameter	Min	Max	Units
V_{PP}	Programming Enable Voltage	11.5	12.5	V
I_{PP}	Programming Enable Current		1.0	mA
$1/t_{CLCL}$	Oscillator Frequency	3	24	MHz
t_{AVGL}	Address Setup to $\overline{PROG}$ Low	$48t_{CLCL}$		
t_{GHAX}	Address Hold after $\overline{PROG}$	$48t_{CLCL}$		
t_{DVGL}	Data Setup to $\overline{PROG}$ Low	$48t_{CLCL}$		
t_{GHDX}	Data Hold after $\overline{PROG}$	$48t_{CLCL}$		
t_{EHSH}	P2.7 ($\overline{ENABLE}$) High to V_{PP}	$48t_{CLCL}$		
t_{SHGL}	V_{PP} Setup to $\overline{PROG}$ Low	10		µs
t_{GLGH}	$\overline{PROG}$ Width	1	110	µs
t_{AVQV}	Address to Data Valid		$48t_{CLCL}$	
t_{ELQV}	$\overline{ENABLE}$ Low to Data Valid		$48t_{CLCL}$	
t_{EHQZ}	Data Float after $\overline{ENABLE}$	0	$48t_{CLCL}$	
t_{GHBL}	$\overline{PROG}$ High to $\overline{BUSY}$ Low		1.0	µs
t_{WC}	Byte Write Cycle Time		2.0	ms

Flash/EEPROM Programming and Verification Waveforms – Parallel Mode



Serial Downloading Waveforms



Serial Programming Characteristics

Figure 16. Serial Programming Timing

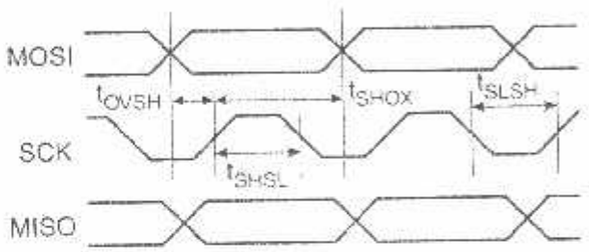


Table 11. Serial Programming Characteristics, T_A = -40° C to 85° C, V_{CC} = 4.0 - 6.0V (Unless Otherwise Noted)

Symbol	Parameter	Min	Typ	Max	Units
$1/t_{CLCL}$	Oscillator Frequency	0		24	MHz
t_{CLCL}	Oscillator Period	41.6			ns
t_{SHSL}	SCK Pulse Width High	24 t_{CLCL}			ns
t_{SLSH}	SCK Pulse Width Low	24 t_{CLCL}			ns
t_{OVSH}	MOSI Setup to SCK High	t_{CLCL}			ns
t_{SHOX}	MOSI Hold after SCK High	2 t_{CLCL}			ns

Absolute Maximum Ratings*

Operating Temperature	-55°C to +125°C
Storage Temperature	-65°C to +150°C
Voltage on Any Pin with Respect to Ground	-1.0V to +7.0V
Maximum Operating Voltage	6.6V
DC Output Current	15.0 mA

*NOTICE: Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC Characteristics

The values shown in this table are valid for T_A = -40°C to 85°C and V_{CC} = 5.0V ± 20%, unless otherwise noted.

Symbol	Parameter	Condition	Min	Max	Units
V_{IL}	Input Low-voltage	(Except $\overline{EA}$)	-0.5	0.2 V_{CC} - 0.1	V
V_{IL1}	Input Low-voltage ($\overline{EA}$)		-0.5	0.2 V_{CC} - 0.3	V
V_{IH}	Input High-voltage	(Except XTAL1, RST)	0.2 V_{CC} + 0.9	V_{CC} + 0.5	V
V_{IH1}	Input High-voltage	(XTAL1, RST)	0.7 V_{CC}	V_{CC} + 0.5	V
V_{OL}	Output Low-voltage (1) (Ports 1,2,3)	I_{OL} = 1.6 mA		0.5	V
V_{OL1}	Output Low-voltage (1) (Port 0, ALE, $\overline{PSEN}$)	I_{OL} = 3.2 mA		0.5	V
V_{OH}	Output High-voltage (Ports 1,2,3, ALE, $\overline{PSEN}$)	I_{OH} = -60 µA, V_{CC} = 5V ±10%	2.4		V
		I_{OH} = -25 µA	0.75 V_{CC}		V
		I_{OH} = -10 µA	0.9 V_{CC}		V
V_{OH1}	Output High-voltage (Port 0 in External Bus Mode)	I_{OH} = -800 µA, V_{CC} = 5V ± 10%	2.4		V
		I_{OH} = -300 µA	0.75 V_{CC}		V
		I_{OH} = -80 µA	0.9 V_{CC}		V
I_{IL}	Logical 0 Input Current (Ports 1,2,3)	V_{IN} = 0.45V		-50	µA
I_{TL}	Logical 1 to 0 Transition Current (Ports 1,2,3)	V_{IN} = 2V, V_{CC} = 5V ± 10%		-650	µA
I_{LI}	Input Leakage Current (Port 0, $\overline{EA}$)	0.45 < V_{IN} < V_{CC}		±10	µA
RRST	Reset Pull-down Resistor		50	300	KΩ
C_{IO}	Pin Capacitance	Test Freq. = 1 MHz, T_A = 25°C		10	pF
I_{CC}	Power Supply Current	Active Mode, 12 MHz		25	mA
		Idle Mode, 12 MHz		6.5	mA
	Power-down Mode (2)	V_{CC} = 6V		100	µA
		V_{CC} = 3V		40	µA

Notes:
1. Under steady state (non-transient) conditions, I_{OL} must be externally limited as follows:
   Maximum I_{OL} per port pin: 10 mA
   Maximum I_{OL} per 8-bit port: Port 0: 26 mA; Ports 1, 2, 3: 15 mA
   Maximum total I_{OL} for all output pins: 71 mA
   If I_{OL} exceeds the test condition, V_{OL} may exceed the related specification. Pins are not guaranteed to sink current greater than the listed test conditions.
2. Minimum V_{CC} for Power-down is 2V

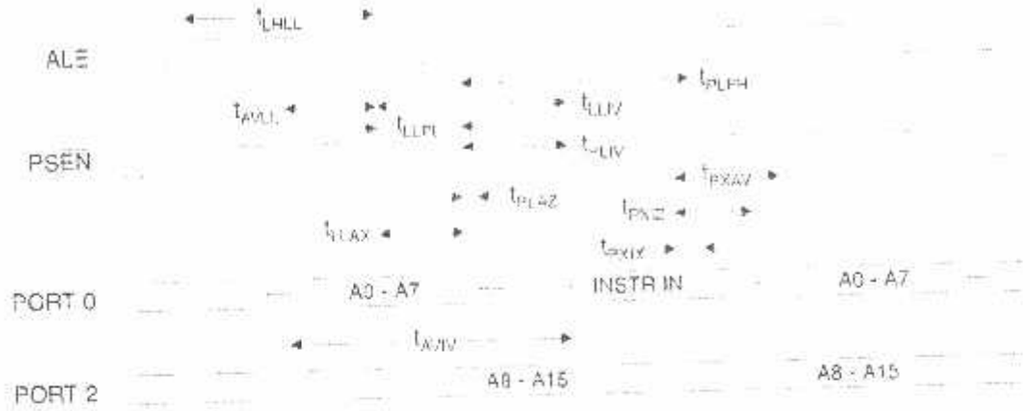
AC Characteristics

Under operating conditions, load capacitance for Port 0, ALE/$\overline{PROG}$, and $\overline{PSEN}$ = 100 pF; load capacitance for all other outputs = 80 pF.

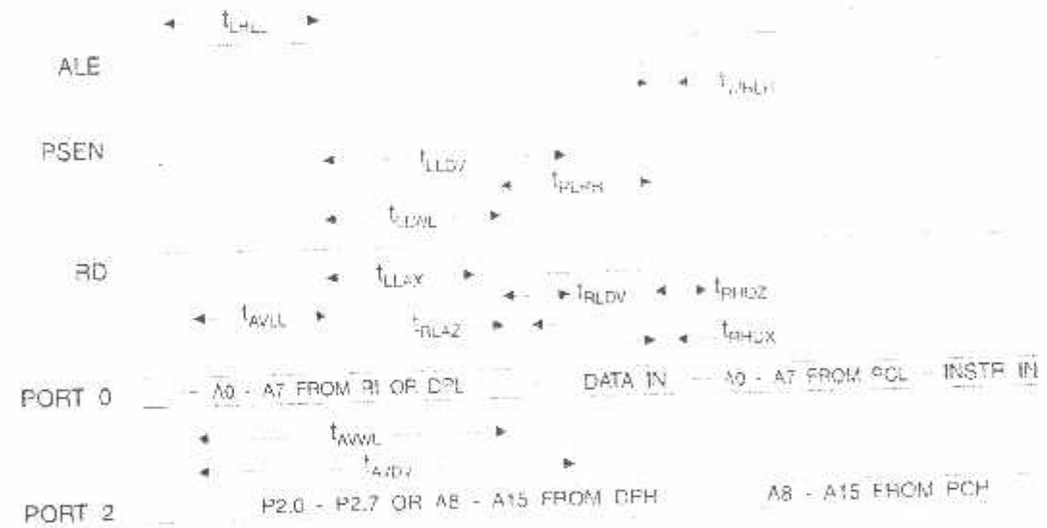
External Program and Data Memory Characteristics

Symbol	Parameter	Variable Oscillator		Units
		Min	Max	
$1/t_{CLCL}$	Oscillator Frequency	0	24	MHz
t_{LHLL}	ALE Pulse Width	$2t_{CLCL}$ - 40		ns
t_{AVLL}	Address Valid to ALE Low	t_{CLCL} - 13		ns
t_{LLAX}	Address Hold after ALE Low	t_{CLCL} - 20		ns
t_{LLIV}	ALE Low to Valid Instruction In		$4t_{CLCL}$ - 65	ns
t_{LLPL}	ALE Low to $\overline{PSEN}$ Low	t_{CLCL} - 13		ns
t_{PLPH}	$\overline{PSEN}$ Pulse Width	$3t_{CLCL}$ - 20		ns
t_{PLIV}	$\overline{PSEN}$ Low to Valid Instruction In		$3t_{CLCL}$ - 45	ns
t_{PXIX}	Input Instruction Hold after $\overline{PSEN}$	0		ns
t_{PXIZ}	Input Instruction Float after $\overline{PSEN}$		t_{CLCL} - 10	ns
t_{PXAV}	$\overline{PSEN}$ to Address Valid	t_{CLCL} - 8		ns
t_{AVIV}	Address to Valid Instruction In		$5t_{CLCL}$ - 55	ns
t_{PLAZ}	$\overline{PSEN}$ Low to Address Float		10	ns
t_{RLRH}	$\overline{RD}$ Pulse Width	$6t_{CLCL}$ - 100		ns
t_{WLWH}	$\overline{WR}$ Pulse Width	$6t_{CLCL}$ - 100		ns
t_{RLDV}	$\overline{RD}$ Low to Valid Data In		$5t_{CLCL}$ - 90	ns
t_{RHDX}	Data Hold after $\overline{RD}$	0		ns
t_{RHDZ}	Data Float after $\overline{RD}$		$2t_{CLCL}$ - 28	ns
t_{LLDV}	ALE Low to Valid Data In		$8t_{CLCL}$ - 150	ns
t_{AVDV}	Address to Valid Data In		$9t_{CLCL}$ - 165	ns
t_{LLWL}	ALE Low to $\overline{RD}$ or $\overline{WR}$ Low	$3t_{CLCL}$ - 50	$3t_{CLCL}$ + 50	ns
t_{AVWL}	Address to $\overline{RD}$ or $\overline{WR}$ Low	$4t_{CLCL}$ - 75		ns
t_{QVWX}	Data Valid to $\overline{WR}$ Transition	t_{CLCL} - 20		ns
t_{QVWH}	Data Valid to $\overline{WR}$ High	$7t_{CLCL}$ - 120		ns
t_{WHQX}	Data Hold after $\overline{WR}$	t_{CLCL} - 20		ns
t_{RLAZ}	$\overline{RD}$ Low to Address Float		0	ns
t_{WHLH}	$\overline{RD}$ or $\overline{WR}$ High to ALE High	t_{CLCL} - 20	t_{CLCL} + 25	ns

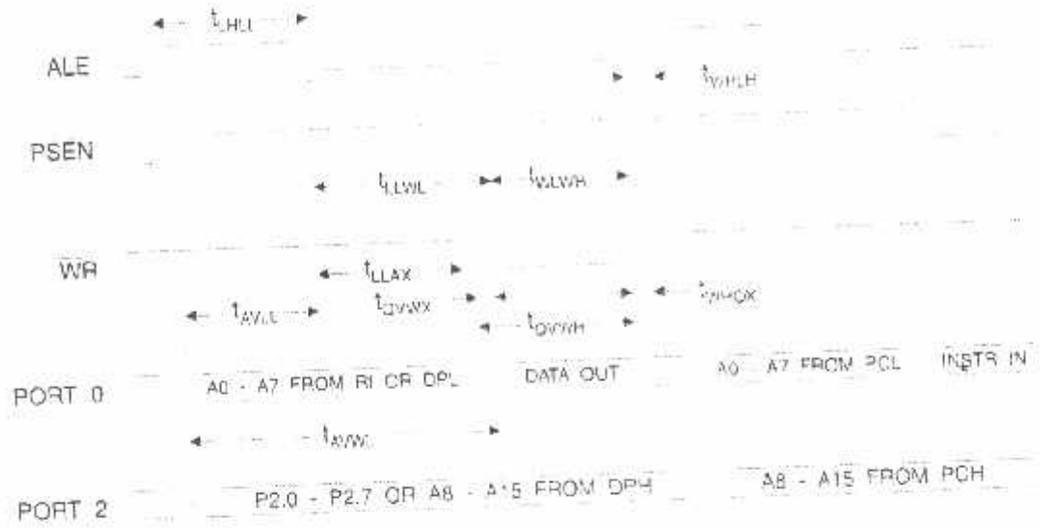
External Program Memory Read Cycle



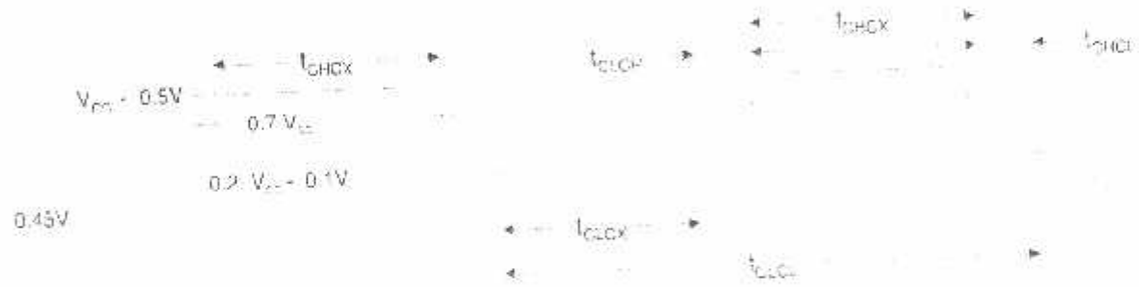
External Data Memory Read Cycle



External Data Memory Write Cycle



External Clock Drive Waveforms



External Clock Drive

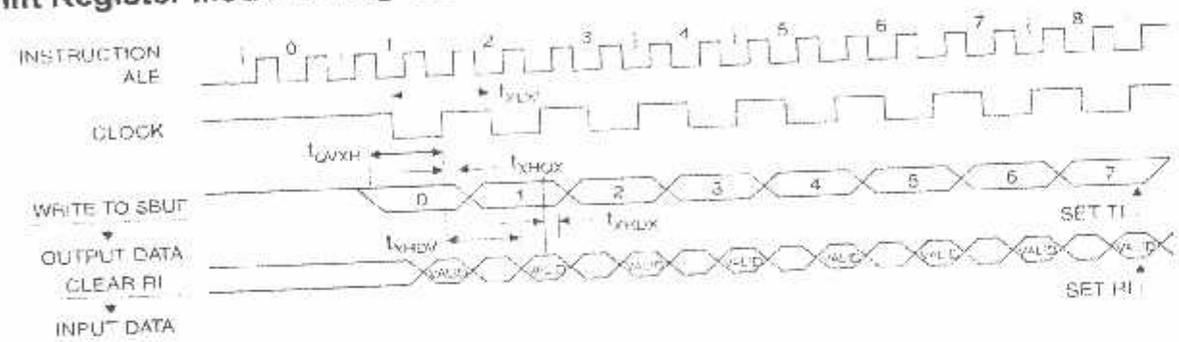
Symbol	Parameter	V_{CC} = 4.0V to 6.0V		Units
		Min	Max	
$1/t_{CLCL}$	Oscillator Frequency	0	24	MHz
t_{CLCL}	Clock Period	41.6		ns
t_{CHCX}	High Time	15		ns
t_{CLCX}	Low Time	15		ns
t_{CLCH}	Rise Time		20	ns
t_{CHCL}	Fall Time		20	ns

Serial Port Timing: Shift Register Mode Test Conditions

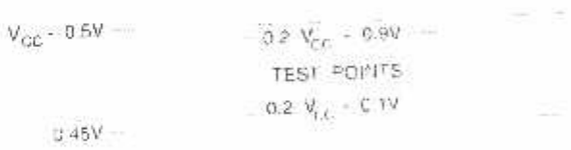
The values in this table are valid for V_{CC} = 4.0V to 6V and Load Capacitance = 80 pF.

Symbol	Parameter	Variable Oscillator		Units
		Min	Max	
t_{XLXL}	Serial Port Clock Cycle Time	$12t_{CLCL}$		µs
t_{QVXH}	Output Data Setup to Clock Rising Edge	$10t_{CLCL}$ - 133		ns
t_{XHQX}	Output Data Hold after Clock Rising Edge	$2t_{CLCL}$ - 117		ns
t_{XHDX}	Input Data Hold after Clock Rising Edge	0		ns
t_{XHDV}	Clock Rising Edge to Input Data Valid		$10t_{CLCL}$ - 133	ns

Shift Register Mode Timing Waveforms



AC Testing Input/Output Waveforms[1]



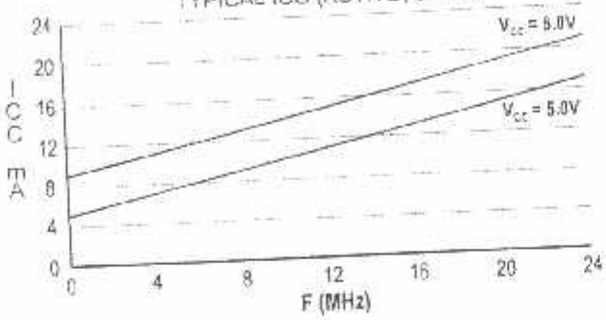
Note: 1. AC Inputs during testing are driven at V_{CC} - 0.5V for a logic 1 and 0.45V for a logic 0. Timing measurements are made at V_{IH} min. for a logic 1 and V_{IL} max. for a logic 0.

Float Waveforms[1]

Note: 1. For timing purposes, a port pin is no longer floating when a 100 mV change from load voltage occurs. A port pin begins to float when a 100 mV change from the loaded V_{OH}/V_{OL} level occurs.

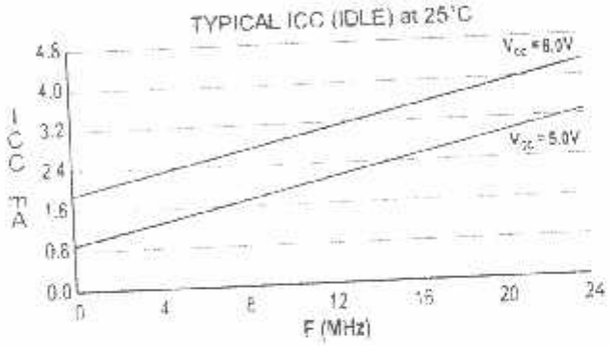
AT89S8252

TYPICAL ICC (ACTIVE) at 25°C



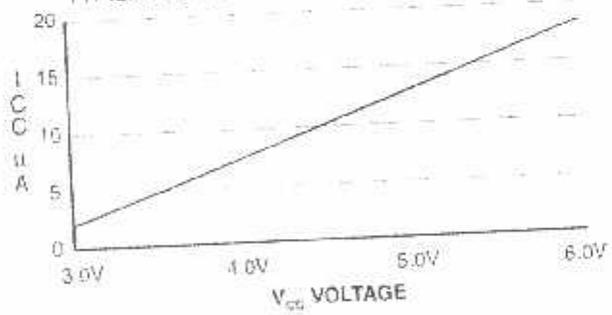
AT89S8252

TYPICAL ICC (IDLE) at 25°C



AT89S8252

TYPICAL ICC vs. VOLTAGE - POWER DOWN (85°C)



Notes: 1. XTAL1 tied to GND for Icc (power-down)
2. Lock bits programmed

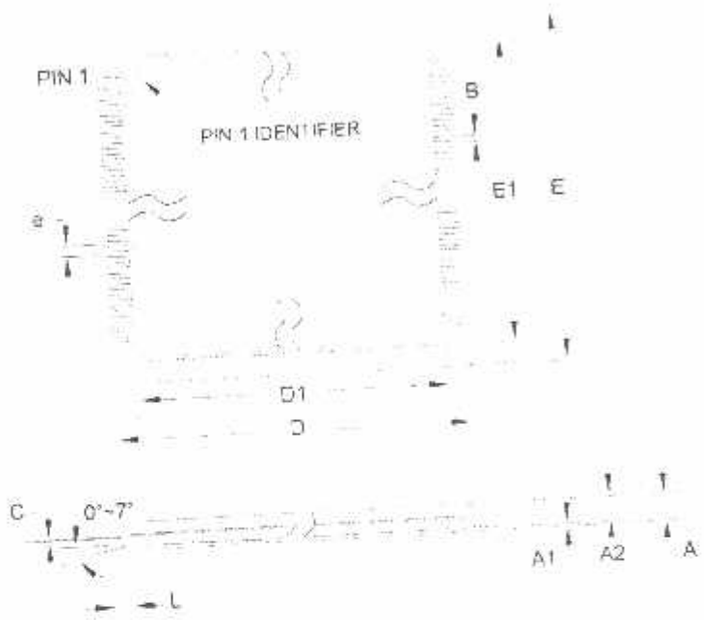
Ordering Information

Speed (MHz)	Power Supply	Ordering Code	Package	Operation Range
24	4.0V to 6.0V	AT89S8252-24AC AT89S8252-24JC AT89S8252-24PC	44A 44J 40P6	Commercial (0°C to 70°C)
	4.0V to 6.0V	AT89S8252-24AI AT89S8252-24JI AT89S8252-24PI	44A 44J 40P6	Industrial (-40°C to 85°C)

Package Type	
44A	44-lead, Thin Plastic Gull Wing Quad Flatpack (TQFP)
44J	44-lead, Plastic J-leaded Chip Carrier (PLCC)
40P6	40-lead, 0.600" Wide, Plastic Dual Inline Package (PDIP)

Packaging Information

44A – TQFP



COMMON DIMENSIONS
(Unit of Measure = mm)

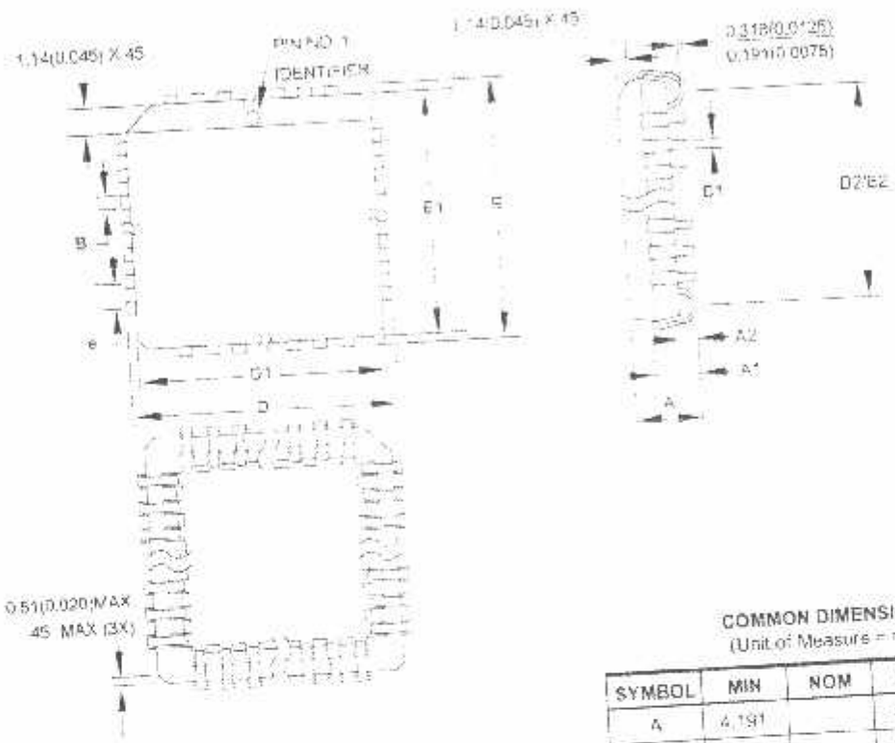
SYMBOL	MIN	NOM	MAX	NOTE
A	–	–	1.20	
A1	0.05	–	0.15	
A2	0.95	1.00	1.05	
D	11.75	12.00	12.25	
D1	9.90	10.00	10.10	Note 2
E	11.75	12.00	12.25	
E1	9.90	10.00	10.10	Note 2
B	0.30	–	0.45	
C	0.09	–	0.20	
L	0.45	–	0.75	
e	0.80 TYP			

Notes
1. This package conforms to JEDEC reference MS-026, Variation ACB.
2. Dimensions D1 and E1 do not include mold protrusion. Allowable protrusion is 0.25 mm per side. Dimensions D1 and E1 are maximum plastic body size dimensions including mold mismatch.
3. Lead coplanarity is 0.10 mm maximum.

10/5/2001

	TITLE	DRAWING NO.	REV.
2325 Orchard Parkway San Jose, CA 95131	44A, 44-lead, 10 x 10 mm Body Size, 1.0 mm Body Thickness, 0.8 mm Lead Pitch, Thin Profile Plastic Quad Flat Package (TQFP)	44A	B

4J – PLCC



COMMON DIMENSIONS
(Unit of Measure = mm)

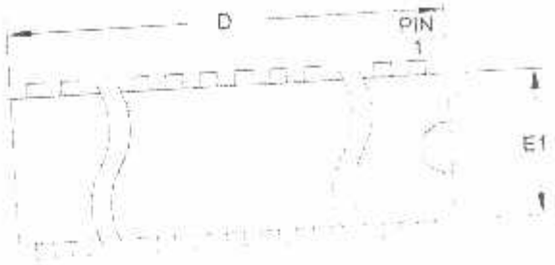
SYMBOL	MIN	NOM	MAX	NOTE
A	4.191		4.572	
A1	2.286		3.048	
A2	0.508	–	–	
D	17.399	–	17.653	
D1	16.510		16.662	Note 2
E	17.399	–	17.653	
E1	16.510	–	16.662	Note 2
D2/E2	14.986		16.002	
B	0.660	–	0.813	
B1	0.330		0.533	
e	1.270 TYP			

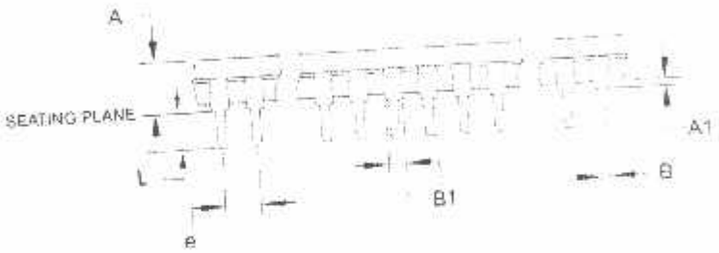
Notes:
1. This package conforms to JEDEC reference MS-016, Variation AC.
2. Dimensions D1 and E1 do not include mold protrusion. Allowable protrusion is .010"(0.254 mm) per side. Dimension D1 and E1 include mold mismatch and are measured at the extreme material condition at the upper or lower parting line.
3. Lead coplanarity is 0.004" (0.102 mm) maximum.

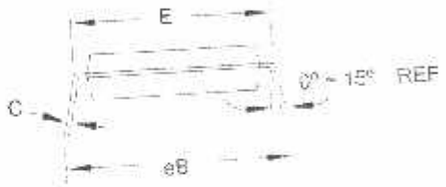
10/04/01

	TITLE	DRAWING NO.	REV.
2325 Orchard Parkway San Jose, CA 95131	44J, 44-lead, Plastic J-leaded Chip Carrier (PLCC)	44J	B

40P6 – PDIP







COMMON DIMENSIONS
(Unit of Measure = mm)

SYMBOL	MIN	NOM	MAX	NOTE
A	–		4.826	
A1	0.381	–	–	
D	52.070	–	52.578	Note 2
E	15.240	–	15.875	
E1	13.462	–	13.970	Note 2
B	0.356	–	0.559	
B1	1.041	–	1.651	
L	3.048	–	3.556	
C	0.203		0.381	
eB	15.494	–	17.526	
e	2.540 TYP			

Notes:
1. This package conforms to JEDEC reference MS-011, Variation AC.
2. Dimensions D and E1 do not include mold Flash or Protrusion. Mold Flash or Protrusion shall not exceed 0.25 mm (0.010").

09/28/01

	TITLE	DRAWING NO.	REV.
2325 Orchard Parkway San Jose, CA 95131	**40P6**, 40-lead (0.600"/15.24 mm Wide) Plastic Dual Inline Package (PDIP)	40P6	B

Atmel Corporation

2325 Orchard Parkway
San Jose, CA 95131, USA
Tel: 1(408) 441-0311
Fax: 1(408) 487-2600

Regional Headquarters

Europe
Atmel Sarl
Route des Arsenaux 41
Case Postale 80
CH-1705 Fribourg
Switzerland
Tel: (41) 26-426-5555
Fax: (41) 26-426-5500

Asia
Room 1219
Chinachem Golden Plaza
77 Mody Road Tsimshatsui
East Kowloon
Hong Kong
Tel: (852) 2721-9778
Fax: (852) 2722-1369

Japan
9F, Tonetsu Shinkawa Bldg.
1-24-8 Shinkawa
Chuo-ku, Tokyo 104-0033
Japan
Tel: (81) 3-3523-3551
Fax: (81) 3-3523-7581

Atmel Operations

Memory
2325 Orchard Parkway
San Jose, CA 95131, USA
Tel: 1(408) 441-0311
Fax: 1(408) 436-4314

Microcontrollers
2325 Orchard Parkway
San Jose, CA 95131, USA
Tel: 1(408) 441-0311
Fax: 1(408) 436-4314

La Chantrerie
BP 70602
44306 Nantes Cedex 3, France
Tel: (33) 2-40-18-18-18
Fax: (33) 2-40-18-19-60

ASIC/ASSP/Smart Cards
Zone Industrielle
13106 Rousset Cedex, France
Tel: (33) 4-42-53-60-00
Fax: (33) 4-42-53-60-01

1150 East Cheyenne Mtn. Blvd.
Colorado Springs, CO 80906, USA
Tel: 1(719) 576-3300
Fax: 1(719) 540-1759

Scottish Enterprise Technology Park
Maxwell Building
East Kilbride G75 0QR, Scotland
Tel: (44) 1355-803-000
Fax: (44) 1355-242-743

RF/Automotive
Theresienstrasse 2
Postfach 3535
74025 Heilbronn, Germany
Tel: (49) 71-31-67-0
Fax: (49) 71-31-67-2340

1150 East Cheyenne Mtn. Blvd.
Colorado Springs, CO 80906, USA
Tel: 1(719) 576-3300
Fax: 1(719) 540-1759

Biometrics/Imaging/Hi-Rel MPU/
High Speed Converters/RF Datacom
Avenue de Rochepleine
BP 123
38521 Saint-Egreve Cedex, France
Tel: (33) 4-76-58-30-00
Fax: (33) 4-76-58-34-80

Literature Requests
www.atmel.com/literature

0481F-MICRO-11/03 xM

XR-2206

Monolithic
Function Generator

EXAR ...the analog plus company™

June 1997-3

FEATURES

- Low-Sine Wave Distortion, 0.5%, Typical
- Excellent Temperature Stability, 20ppm/°C, Typ.
- Wide Sweep Range, 2000:1, Typical
- Low-Supply Sensitivity, 0.01%V, Typ.
- Linear Amplitude Modulation
- TTL Compatible FSK Controls
- Wide Supply Range, 10V to 26V
- Adjustable Duty Cycle, 1% TO 99%

APPLICATIONS

- Waveform Generation
- Sweep Generation
- AM/FM Generation
- V/F Conversion
- FSK Generation
- Phase-Locked Loops (VCO)

GENERAL DESCRIPTION

The XR-2206 is a monolithic function generator integrated circuit capable of producing high quality sine, square, triangle, ramp, and pulse waveforms of high-stability and accuracy. The output waveforms can be both amplitude and frequency modulated by an external voltage. Frequency of operation can be selected externally over a range of 0.01Hz to more than 1MHz.

The circuit is ideally suited for communications, instrumentation, and function generator applications requiring sinusoidal tone, AM, FM, or FSK generation. It has a typical drift specification of 20ppm/°C. The oscillator frequency can be linearly swept over a 2000:1 frequency range with an external control voltage, while maintaining low distortion.

ORDERING INFORMATION

Part No.	Package	Operating Temperature Range
XR-2206M	16 Lead 300 Mil CDIP	-55°C to +125°C
XR-2206P	16 Lead 300 Mil PDIP	-40°C to +85°C
XR-2206CP	16 Lead 300 Mil PDIP	0°C to +70°C
XR-2206D	16 Lead 300 Mil JEDEC SOIC	0°C to +70°C

TQM™

EXAR Corporation, 48720 Kato Road, Fremont, CA 94538 ◆ (510) 668-7000 ◆ (510) 668-7017

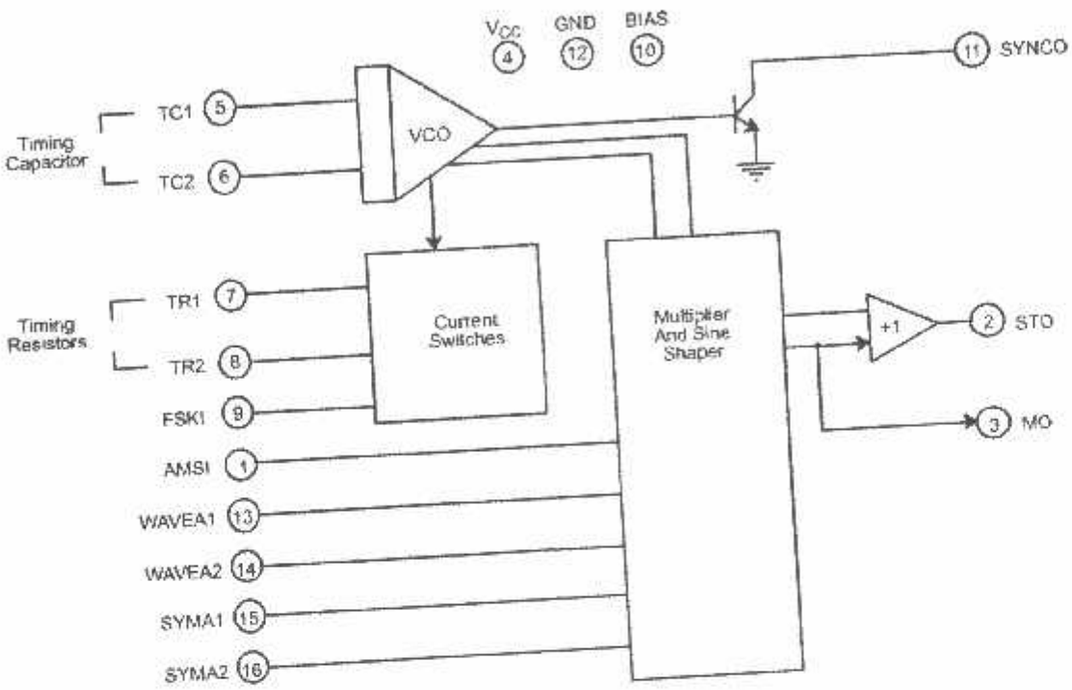
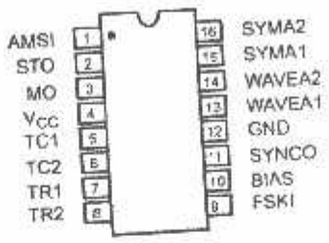
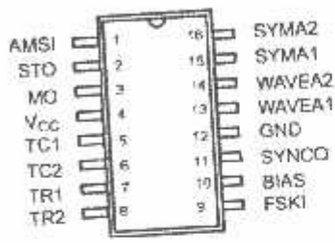


Figure 1. XR-2206 Block Diagram



16 Lead PDIP, CDIP (0.300")



16 Lead SOIC (Jedec, 0.300")

PIN DESCRIPTION

Pin #	Symbol	Type	Description
1	AMSI	I	**Amplitude Modulating Signal Input.**
2	STO	O	**Sine or Triangle Wave Output.**
3	MO	O	**Multiplier Output.**
4	V_{CC}		**Positive Power Supply.**
5	TC1	I	**Timing Capacitor Input.**
6	TC2	I	**Timing Capacitor Input.**
7	TR1	O	**Timing Resistor 1 Output.**
8	TR2	O	**Timing Resistor 2 Output.**
9	FSKI	I	**Frequency Shift Keying Input.**
10	BIAS	O	**Internal Voltage Reference.**
11	SYNCO	O	**Sync Output.** This output is a open collector and needs a pull up resistor to V_{CC}.
12	GND		**Ground pin.**
13	WAVEA1	I	**Wave Form Adjust Input 1.**
14	WAVEA2	I	**Wave Form Adjust Input 2.**
15	SYMA1	I	**Wave Symetry Adjust 1.**
16	SYMA2	I	**Wave Symetry Adjust 2.**

DC ELECTRICAL CHARACTERISTICS

Test Conditions: Test Circuit of *Figure 2* V_{CC} = 12V, T_A = 25°C, C = 0.01µF, R_1 = 100kΩ, R_2 = 10kΩ, R_3 = 25kΩ
Unless Otherwise Specified, S_1 open for triangle, closed for sine wave.

Parameters	XR-2206M/P			XR-2206CP/D			Units	Conditions
	Min.	Typ.	Max.	Min.	Typ.	Max.		
General Characteristics								
Single Supply Voltage	**10**		**26**	10		26	V	
Split-Supply Voltage	**±5**		**±13**	±5		±13	V	
Supply Current		12	17		14	20	mA	$R_1 \geq 10k\Omega$
Oscillator Section								
Max. Operating Frequency	0.5	1		0.5	1		MHz	C = 1000pF, R_1 = 1kΩ
Lowest Practical Frequency		0.01			0.01		Hz	C = 50µF, R_1 = 2MΩ
Frequency Accuracy		±1	**±4**		±2		% of f_o	$f_o = 1/R_1C$
Temperature Stability		±10	**±50**		±20		ppm/°C	0°C ≤ T_A ≤ 70°C $R_1 = R_2$ = 20kΩ
Frequency								
Sine Wave Amplitude Stability[2]		4800			4800		ppm/°C	
Supply Sensitivity		0.01	**0.1**		0.01		%/V	V_{LOW} = 10V, V_{HIGH} = 20V, $R_1 = R_2$ = 20kΩ
Sweep Range	1000:1	2000:1			2000:1		$f_H = f_L$	f_H @ R_1 = 1kΩ f_L @ R_1 = 2MΩ
Sweep Linearity								
10:1 Sweep		2			2		%	f_L = 1kHz, f_H = 10kHz
1000:1 Sweep		8			8		%	f_L = 100Hz, f_H = 100kHz
FM Distortion		0.1			0.1		%	±10% Deviation
Recommended Timing Components								
Timing Capacitor: C	**0.001**		100	0.001		100	µF	*Figure 5*
Timing Resistors: R_1 & R_2	**1**		2000	1		2000	kΩ	*Figure 3*
Triangle Sine Wave Output[1]								
Triangle Amplitude		160			160		mV/kΩ	*Figure 2*, S_1 Open
Sine Wave Amplitude	**40**	60	80		60		mV/kΩ	*Figure 2*, S_1 Closed
Max. Output Swing		6			6		Vp-p	
Output Impedance		600			600		Ω	
Triangle Linearity		1			1		%	
Amplitude Stability		0.5			0.5		dB	For 1000:1 Sweep
Sine Wave Distortion								
Without Adjustment		2.5			2.5		%	R_1 = 30kΩ
With Adjustment		0.4	**1.0**		0.5	1.5	%	See *Figure 7* and *Figure 8*

Notes
[1] Output amplitude is directly proportional to the resistance, R_3, on Pin 3. See Figure 3.
[2] For maximum amplitude stability, R_3 should be a positive temperature coefficient resistor.
***Bold face parameters** are covered by production test and guaranteed over operating temperature range.*

EXAR

DC ELECTRICAL CHARACTERISTICS (CONT'D)

Parameters	XR-2206M/P			XR-2206CP/D			Units	Conditions
	Min.	Typ.	Max.	Min.	Typ.	Max.		
Amplitude Modulation								
Input Impedance	50	100		50	100		kΩ	
Modulation Range		100			100		%	
Carrier Suppression		55			55		dB	
Linearity		2			2		%	For 95% modulation
Square-Wave Output								
Amplitude		12			12		Vp-p	Measured at Pin 11.
Rise Time		250			250		ns	C_L = 10pF
Fall Time		50			50		ns	C_L = 10pF
Saturation Voltage		0.2	0.4		0.2	0.6	V	I_L = 2mA
Leakage Current		0.1	20		0.1	100	µA	V_{CC} = 26V
FSK Keying Level (Pin 9)	0.8	1.4	2.4	0.8	1.4	2.4	V	See section on circuit controls
Reference Bypass Voltage	2.9	3.1	3.3	2.5	3	3.5	V	Measured at Pin 10.

Notes
[1] Output amplitude is directly proportional to the resistance, R_3, on Pin 3. See Figure 3.
[2] For maximum amplitude stability, R_3 should be a positive temperature coefficient resistor.
***Bold face parameters** are covered by production test and guaranteed over operating temperature range*

Specifications are subject to change without notice

ABSOLUTE MAXIMUM RATINGS

Power Supply 26V
Power Dissipation 750mW
Derate Above 25°C ..... 5mW/°C
Total Timing Current 6mA
Storage Temperature ..... -65°C to +150°C

SYSTEM DESCRIPTION

The XR-2206 is comprised of four functional blocks: a voltage-controlled oscillator (VCO), an analog multiplier and sine-shaper; a unity gain buffer amplifier; and a set of current switches.

The VCO produces an output frequency proportional to an input current, which is set by a resistor from the timing terminals to ground. With two timing pins, two discrete output frequencies can be independently produced for FSK generation applications by using the FSK input control pin. This input controls the current switches which select one of the timing resistor currents, and routes it to the VCO.

TQM™

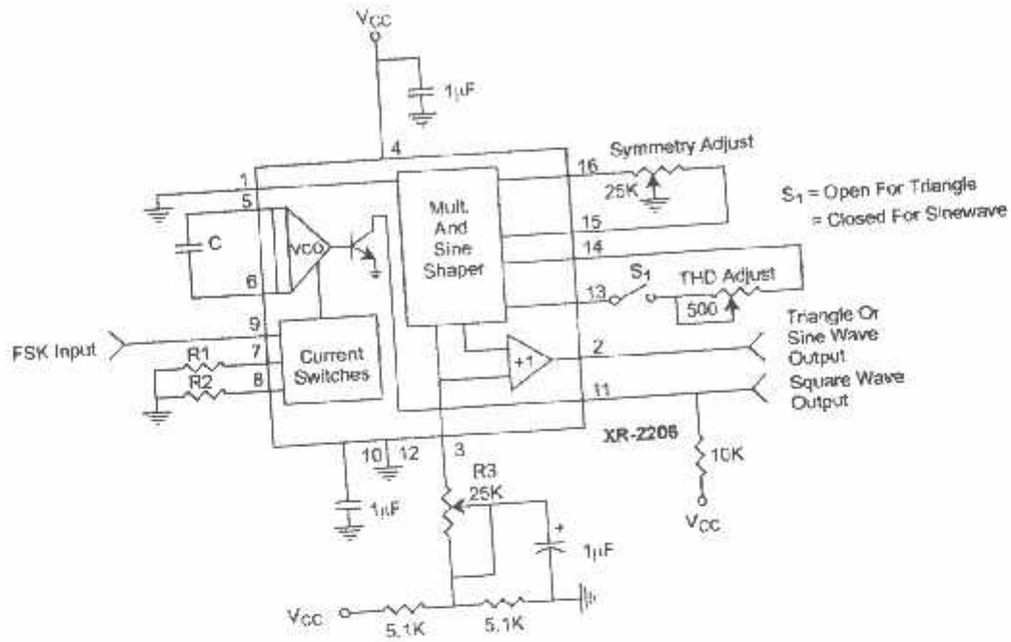


Figure 2. Basic Test Circuit

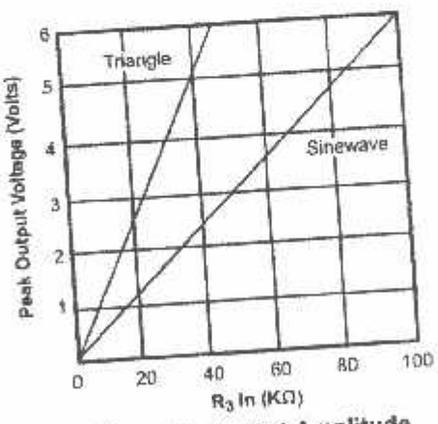


Figure 3. Output Amplitude as a Function of the Resistor, R3, at Pin 3

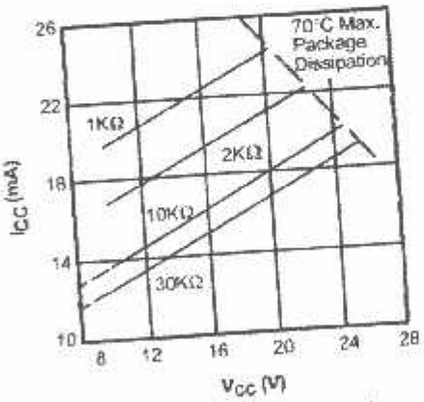


Figure 4. Supply Current vs Supply Voltage, Timing, R

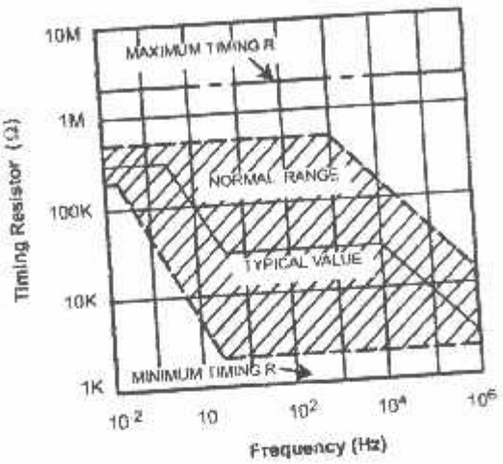


Figure 5. R versus Oscillation Frequency.

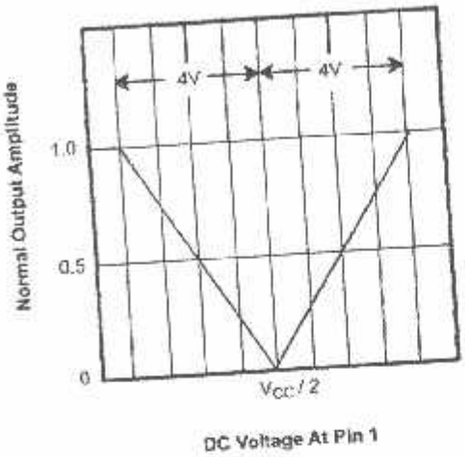


Figure 6. Normalized Output Amplitude versus DC Bias at AM Input (Pin 1)

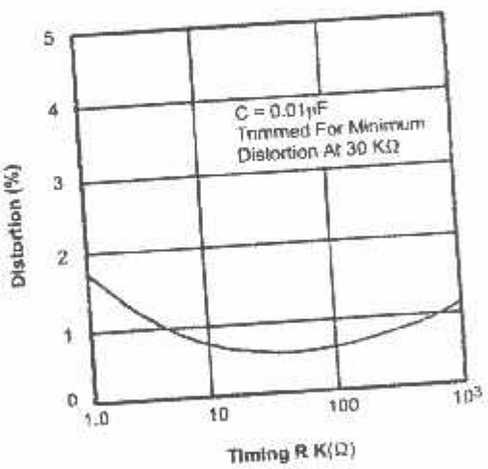


Figure 7. Trimmed Distortion versus Timing Resistor.

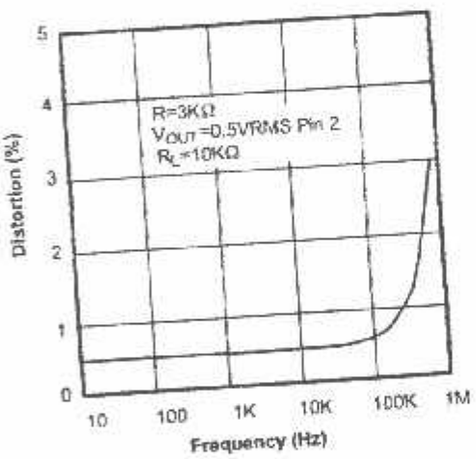


Figure 8. Sine Wave Distortion versus Operating Frequency with Timing Capacitors Varied.

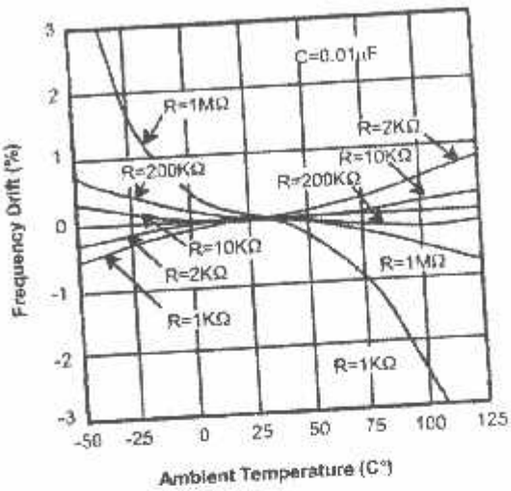


Figure 9. Frequency Drift versus Temperature.

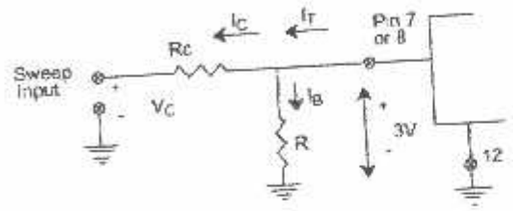


Figure 10. Circuit Connection for Frequency Sweep.

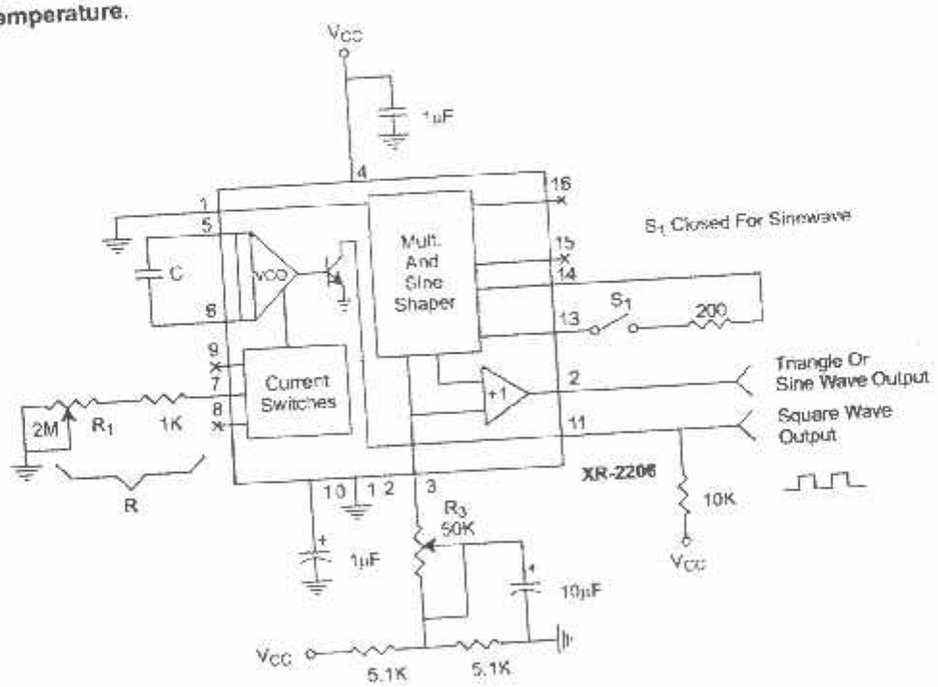


Figure 11. Circuit tor Sine Wave Generation without External Adjustment. (See *Figure 3* for Choice of R_3)

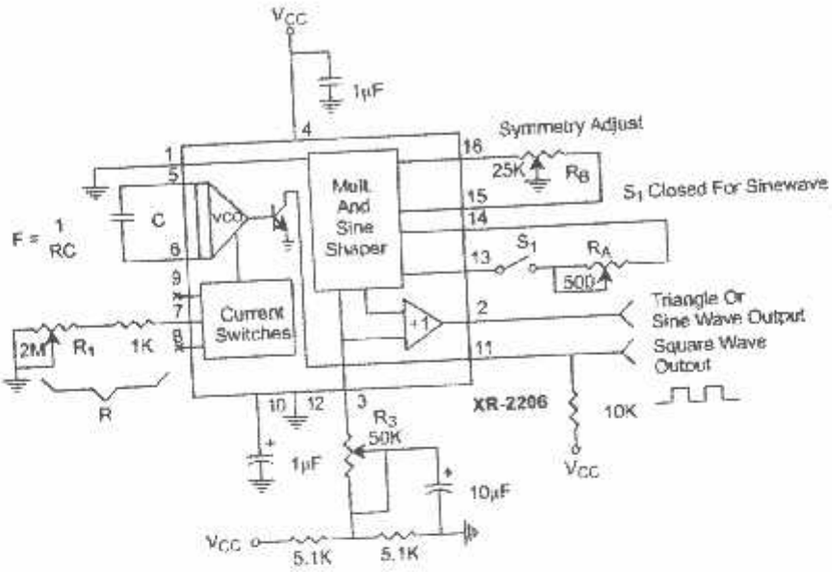


Figure 12. Circuit for Sine Wave Generation with Minimum Harmonic Distortion. (R_3 Determines Output Swing - See *Figure 3*)

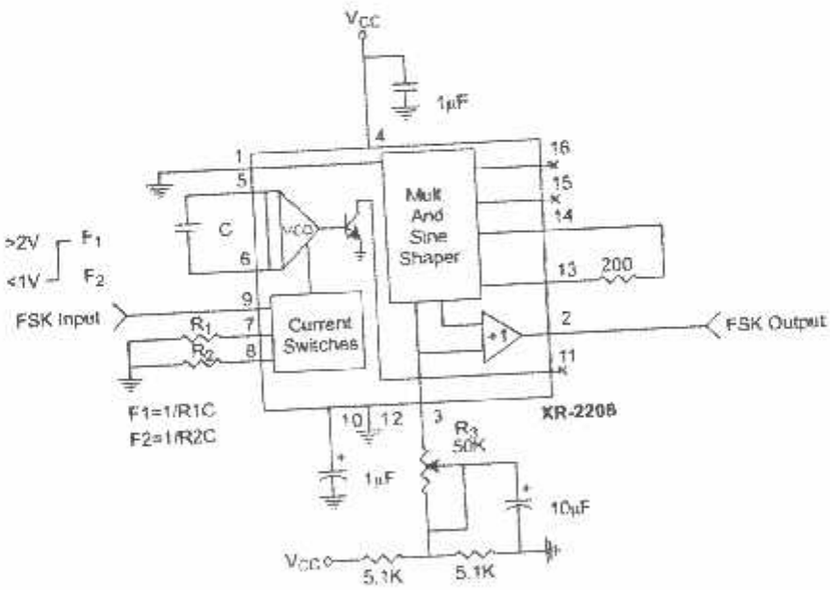


Figure 13. Sinusoidal FSK Generator

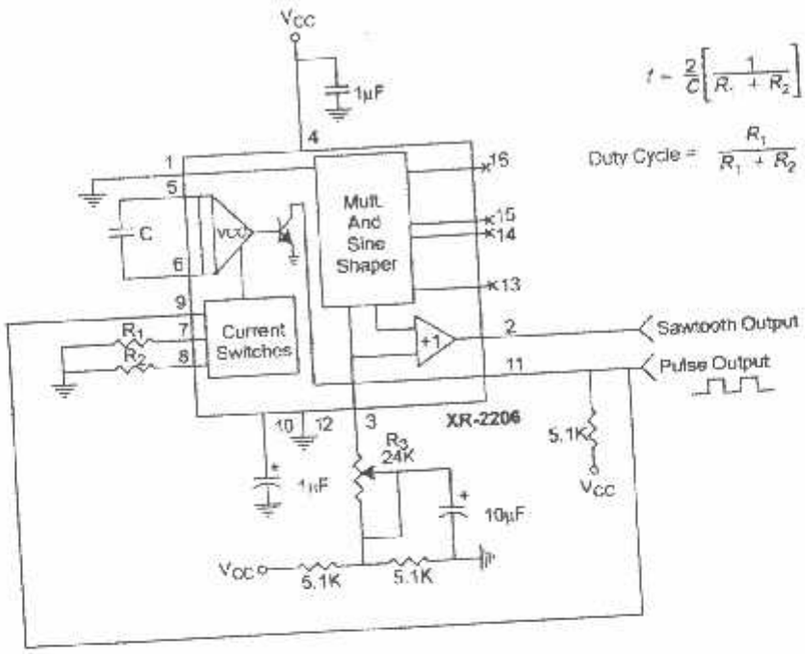


Figure 14. Circuit for Pulse and Ramp Generation.

APPLICATIONS INFORMATION

Frequency-Shift Keying

The XR-2206 can be operated with two separate timing resistors, R_1 and R_2, connected to the timing Pin 7 and 8, respectively, as shown in *Figure 13*. Depending on the polarity of the logic signal at Pin 9, either one or the other of these timing resistors is activated. If Pin 9 is open-circuited or connected to a bias voltage $\geq$ 2V, only R_1 is activated. Similarly, if the voltage level at Pin 9 is $\leq$1V, only R_2 is activated. Thus, the output frequency can be keyed between two levels. f_1 and f_2, as:

$f_1 = 1/R_1C$ and $f_2 = 1/R_2C$

For split-supply operation, the keying voltage at Pin 9 is referenced to V^-.

Output DC Level Control

The dc level at the output (Pin 2) is approximately the same as the dc bias at Pin 3. In *Figure 11*, *Figure 12* and *Figure 13*, Pin 3 is biased midway between V+ and ground, to give an output dc level of $\approx V^+/2$.

Sine Wave Generation

Without External Adjustment

Figure 11 shows the circuit connection for generating a sinusoidal output from the XR-2206. The potentiometer, R_1 at Pin 7, provides the desired frequency tuning. The maximum output swing is greater than $V^+/2$, and the typical distortion (THD) is < 2.5%. If lower sine wave distortion is desired, additional adjustments can be provided as described in the following section.

The circuit of *Figure 11* can be converted to split-supply operation, simply by replacing all ground connections with V^-. For split-supply operation, R_3 can be directly connected to ground.

With External Adjustment:

The harmonic content of sinusoidal output can be reduced to ~0.5% by additional adjustments as shown in *Figure 12*. The potentiometer, R_A, adjusts the sine-shaping resistor, and R_B provides the fine adjustment for the waveform symmetry. The adjustment procedure is as follows:

1. Set R_B at midpoint and adjust R_A for minimum distortion.
2. With R_A set as above, adjust R_B to further reduce distortion.

Triangle Wave Generation

The circuits of *Figure 11* and *Figure 12* can be converted to triangle wave generation, by simply open-circuiting Pin 13 and 14 (i.e., S_1 open). Amplitude of the triangle is approximately twice the sine wave output.

FSK Generation

Figure 13 shows the circuit connection for sinusoidal FSK signal operation. Mark and space frequencies can be independently adjusted by the choice of timing resistors, R_1 and R_2; the output is phase-continuous during transitions. The keying signal is applied to Pin 9. The circuit can be converted to split-supply operation by simply replacing ground with V⁻.

Pulse and Ramp Generation

Figure 14 shows the circuit for pulse and ramp waveform generation. In this mode of operation, the FSK keying terminal (Pin 9) is shorted to the square-wave output (Pin 11), and the circuit automatically frequency-shift keys itself between two separate frequencies during the positive-going and negative-going output waveforms. The pulse width and duty cycle can be adjusted from 1% to 99% by the choice of R_1 and R_2. The values of R_1 and R_2 should be in the range of 1kΩ to 2MΩ.

PRINCIPLES OF OPERATION

Description of Controls

Frequency of Operation:

The frequency of oscillation, f_o, is determined by the external timing capacitor, C, across Pin 5 and 6, and by the timing resistor, R, connected to either Pin 7 or 8. The frequency is given as:

$$f_o = \frac{1}{RC}\ Hz$$

and can be adjusted by varying either R or C. The recommended values of R, for a given frequency range, as shown in *Figure 5*. Temperature stability is optimum for $4k\Omega < R < 200k\Omega$. Recommended values of C are from 1000pF to 100μF.

Frequency Sweep and Modulation:

Frequency of oscillation is proportional to the total timing current, I_T, drawn from Pin 7 or 8:

$$f = \frac{320 I_T(mA)}{C(\mu F)}\ Hz$$

Timing terminals (Pin 7 or 8) are low-impedance points, and are internally biased at +3V, with respect to Pin 12. Frequency varies linearly with IT, over a wide range of current values, from 1μA to 3mA. The frequency can be controlled by applying a control voltage, V_C, to the activated timing pin as shown in *Figure 10*. The frequency of oscillation is related to VC as:

$$f = \frac{1}{RC}\left(1 + \frac{R}{R_C}\left(1 - \frac{V_C}{3}\right)\right) Hz$$

where V_C is in volts. The voltage-to-frequency conversion gain, K, is given as:

$$K = \partial f / \partial V_C = -\frac{0.32}{R_C C}\ \ Hz/V$$

CAUTION: *For safety operation of the circuit, I_T should be limited to ≤ 3mA.*

Output Amplitude:

Maximum output amplitude is inversely proportional to the external resistor, R_3, connected to Pin 3 (see *Figure 3*). For sine wave output, amplitude is approximately 60mV peak per kΩ of R_3; for triangle, the peak amplitude is approximately 160mV peak per kΩ of R_3. Thus, for example, R_3 = 50kΩ would produce approximately 13V sinusoidal output amplitude.

Amplitude Modulation:

Output amplitude can be modulated by applying a dc bias and a modulating signal to Pin 1. The internal impedance at Pin 1 is approximately 100kΩ. Output amplitude varies linearly with the applied voltage at Pin 1, for values of dc bias at this pin, within 14 volts of $V_{CC}/2$ as shown in *Figure 6*. As this bias level approaches $V_{CC}/2$, the phase of the output signal is reversed, and the amplitude goes through zero. This property is suitable for phase-shift keying and suppressed-carrier AM generation. Total dynamic range of amplitude modulation is approximately 55dB.

CAUTION: *AM control must be used in conjunction with a well-regulated supply, since the output amplitude now becomes a function of* V_{CC}.

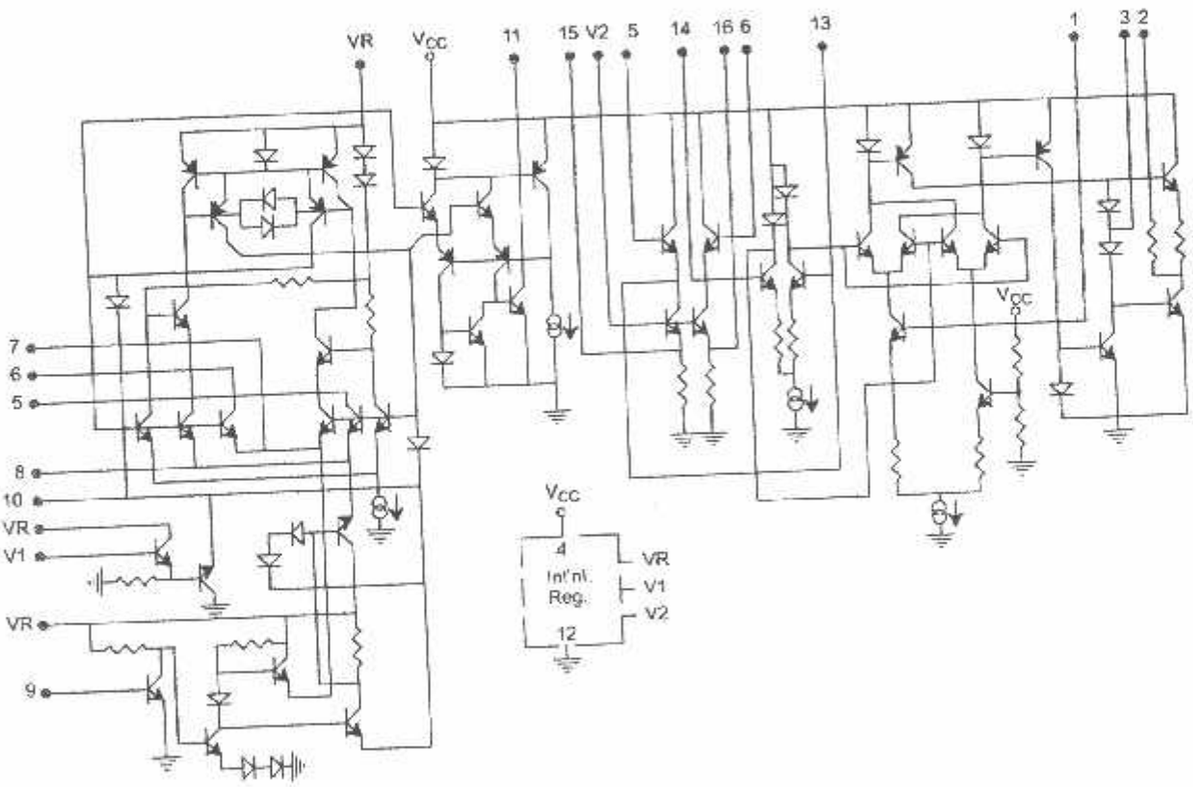
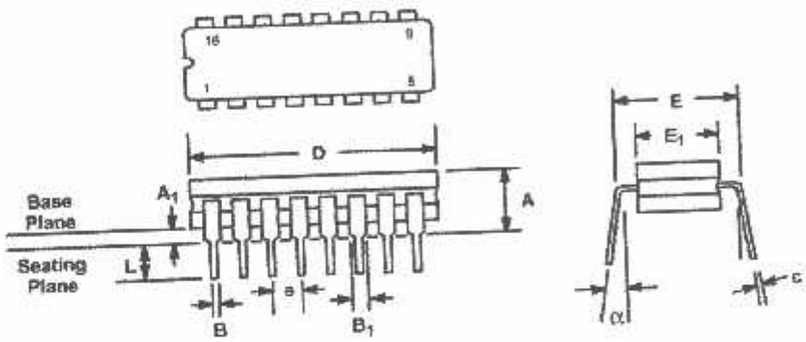


Figure 15. Equivalent Schematic Diagram

16 LEAD CERAMIC DUAL-IN-LINE (300 MIL CDIP)

Rev. 1.00

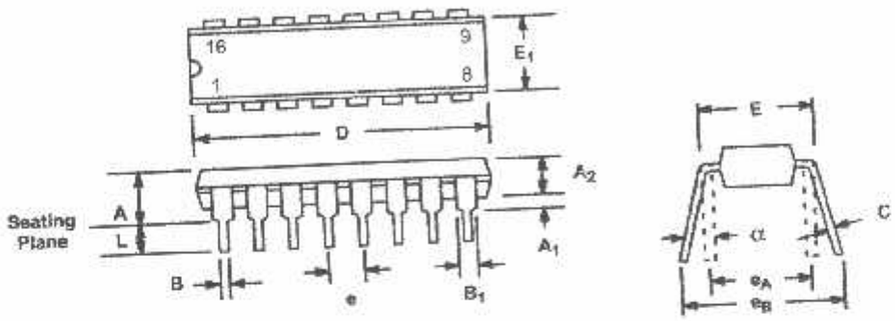


SYMBOL	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.100	0.200	2.54	5.08
A_1	0.015	0.060	0.38	1.52
B	0.014	0.026	0.36	0.66
B_1	0.045	0.065	1.14	1.65
c	0.008	0.018	0.20	0.46
D	0.740	0.840	18.80	21.34
E_1	0.250	0.310	6.35	7.87
E	0.300 BSC		7.62 BSC	
e	0.100 BSC		2.54 BSC	
L	0.125	0.200	3.18	5.08
α	0°	15°	0°	15°

Note: The control dimension is the inch column

16 LEAD PLASTIC DUAL-IN-LINE (300 MIL PDIP)

Rev. 1.00



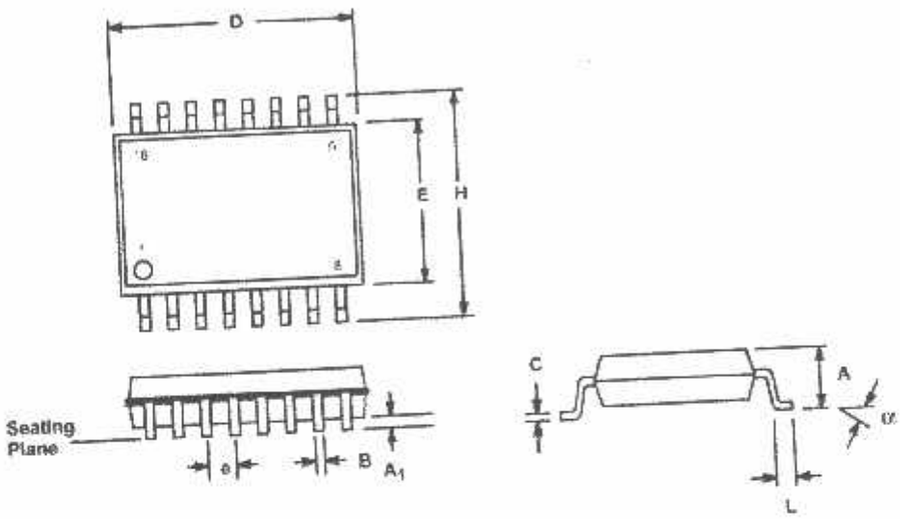
SYMBOL	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.145	0.210	3.68	5.33
A_1	0.015	0.070	0.38	1.78
A_2	0.115	0.195	2.92	4.95
B	0.014	0.024	0.36	0.56
B_1	0.030	0.070	0.76	1.78
C	0.008	0.014	0.20	0.36
D	0.745	0.840	18.92	21.34
E	0.300	0.325	7.62	8.26
E_1	0.240	0.280	6.10	7.11
e	0.100 BSC		2.54 BSC	
e_A	0.300 BSC		7.62 BSC	
e_B	0.310	0.430	7.87	10.92
L	0.115	0.160	2.92	4.06
α	0°	15°	0°	15°

Note: The control dimension is the inch column

EXAR

16 LEAD SMALL OUTLINE (300 MIL JEDEC SOIC)

Rev. 1.00



SYMBOL	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.093	0.104	2.35	2.65
A_1	0.004	0.012	0.10	0.30
B	0.013	0.020	0.33	0.51
C	0.009	0.013	0.23	0.32
D	0.398	0.413	10.10	10.50
E	0.291	0.299	7.40	7.60
e	0.050 BSC		1.27 BSC	
H	0.394	0.419	10.00	10.65
L	0.016	0.050	0.40	1.27
α	0°	8°	0°	8°

Note: The control dimension is the millimeter column

NOTICE

EXAR Corporation reserves the right to make changes to the products contained in this publication in order to improve design, performance or reliability. EXAR Corporation assumes no responsibility for the use of any circuits described herein, conveys no license under any patent or other right, and makes no representation that the circuits are free of patent infringement. Charts and schedules contained here in are only for illustration purposes and may vary depending upon a user's specific application. While the information in this publication has been carefully checked; no responsibility, however, is assumed for inaccuracies.

EXAR Corporation does not recommend the use of any of its products in life support applications where the failure or malfunction of the product can reasonably be expected to cause failure of the life support system or to significantly affect its safety or effectiveness. Products are not authorized for use in such applications unless EXAR Corporation receives, in writing, assurances to its satisfaction that: (a) the risk of injury or damage has been minimized; (b) the user assumes all such risks; (c) potential liability of EXAR Corporation is adequately protected under the circumstances.

Datasheet June 1997

XR-2211

FSK Demodulator/ Tone Decoder

EXAR ...the analog plus company™

June 1997-3

FEATURES

- Wide Frequency Range, 0.01Hz to 300kHz
- Wide Supply Voltage Range, 4.5V to 20V
- HCMOS/TTL/Logic Compatibility
- FSK Demodulation, with Carrier Detection
- Wide Dynamic Range, 10mV to 3V rms
- Adjustable Tracking Range, ±1% to 80%
- Excellent Temp. Stability, ±50ppm/°C, max.

APPLICATIONS

- Caller Identification Delivery
- FSK Demodulation
- Data Synchronization
- Tone Decoding
- FM Detection
- Carrier Detection

GENERAL DESCRIPTION

The XR-2211 is a monolithic phase-locked loop (PLL) system especially designed for data communications applications. It is particularly suited for FSK modem applications. It operates over a wide supply voltage range of 4.5 to 20V and a wide frequency range of 0.01Hz to 300kHz. It can accommodate analog signals between 10mV and 3V, and can interface with conventional DTL, TTL, and ECL logic families. The circuit consists of a basic PLL for tracking an input signal within the pass band, a quadrature phase detector which provides carrier detection, and an FSK voltage comparator which provides FSK demodulation. External components are used to independently set center frequency, bandwidth, and output delay. An internal voltage reference proportional to the power supply is provided at an output pin.

The XR-2211 is available in 14 pin packages specified for military and industrial temperature ranges.

ORDERING INFORMATION

Part No.	Package	Operating Temperature Range
XR-2211M	14 Pin CDIP (0.300")	-55°C to +125°C
XR-2211N	14 Pin CDIP (0.300")	-40°C to +85°C
XR-2211P	14 Pin PDIP (0.300")	-40°C to +85°C
XR-2211D	14 Lead SOIC (Jedec, 0.150")	-40°C to +85°C

TQM™

EXAR Corporation, 48720 Kato Road, Fremont, CA 94538 ◆ (510) 668-7000 ◆ FAX (510) 668-7017

BLOCK DIAGRAM

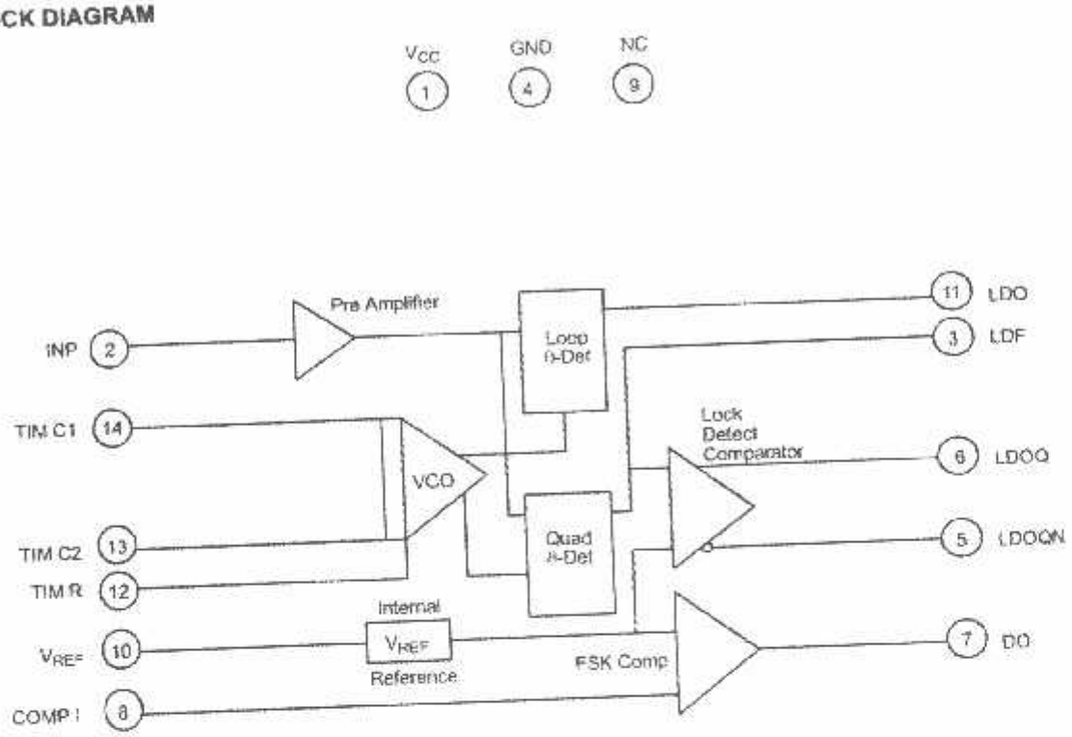
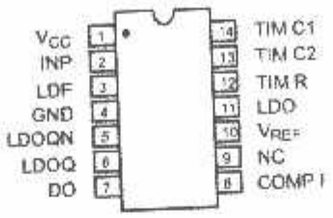
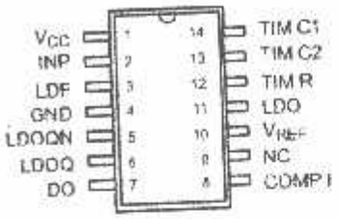


Figure 1. XR-2211 Block Diagram

PIN CONFIGURATION



14 Lead CDIP, PDIP (0.300")



14 Lead SOIC (Jedec, 0.150")

PIN DESCRIPTION

Pin #	Symbol	Type	Description
1	V_{CC}		**Positive Power Supply.**
2	INP	I	**Receive Analog Input.**
3	LDF	O	**Lock Detect Filter.**
4	GND		**Ground Pin.**
5	LDOQN	O	**Lock Detect Output Not.** This output will be low if the VCO is in the capture range.
6	LDOQ	O	**Lock Detect Output.** This output will be high if the VCO is in the capture range.
7	DO	O	**Data Output.** Decoded FSK output.
8	COMP I	I	**FSK Comparator Input.**
9	NC		**Not Connected.**
10	V_{REF}	O	**Internal Voltage Reference.** The value of V_{REF} is $V_{CC}/2$ - 650mV.
11	LDO	O	**Loop Detect Output.** This output provides the result of the quadrature phase detection.
12	TIM R	I	**Timing Resistor Input.** This pin connects to the timing resistor of the VCO.
13	TIM C2	I	**Timing Capacitor Input.** The timing capacitor connects between this pin and pin 14.
14	TIM C1	I	**Timing Capacitor Input.** The timing capacitor connects between this pin and pin 13.

ELECTRICAL CHARACTERISTICS

Test Conditions: V_{CC} = 12V, T_A = +25°C, R_O = 30KΩ, C_O = 0.033μF, unless otherwise specified.

Parameter	Min.	Typ.	Max.	Unit	Conditions
General					
Supply Voltage	**4.5**		**20**	V	
Supply Current		4	7	mA	$R_0 \geq$ 10KΩ. See *Figure 4.*
Oscillator Section					
Frequency Accuracy		±1	±3	%	Deviation from $f_O = 1/R_0 C_0$
Frequency Stability					
Temperature		±20	±50	ppm/°C	See *Figure 8.*
Power Supply		0.05	**0.5**	%/V	V_{CC} = 12 ±1V. See *Figure 7.*
		0.2		%/V	V_{CC} = ± 5V. See *Figure 7.*
Upper Frequency Limit	**100**	300		kHz	R_0 = 8.2KΩ, C_0 = 400pF
Lowest Practical Operating Frequency			0.01	Hz	R_0 = 2MΩ, C_0 = 50μF
Timing Resistor, R_0 - See *Figure 5*					
Operating Range	**5**		2000	KΩ	
Recommended Range	5			KΩ	See *Figure 7* and *Figure 8.*
Loop Phase Dectector Section					
Peak Output Current	**±150**	±200	**±300**	μA	Measured at Pin 11
Output Offset Current		1		μA	
Output Impedance		1		MΩ	
Maximum Swing	**+4**	± 5		V	Referenced to Pin 10
Quadrature Phase Detector					Measured at Pin 3
Peak Output Current	**100**	300		μA	
Output Impedance		1		MΩ	
Maximum Swing		11		V_{PP}	
Input Preampt Section					Measured at Pin 2
Input Impedance		20		KΩ	
Input Signal					
Voltage Required to Cause Limiting		2	10	mV rms	

Notes
Parameters are guaranteed over the recommended operating conditions, but are not 100% tested in production.
***Bold face parameters** are covered by production test and guaranteed over operating temperature range.*

DC ELECTRICAL CHARACTERISTICS (CONT'D)

Test Conditions: V_{CC} = 12V, T_A = +25°C, R_O = 30KΩ, C_O = 0.033μF, unless otherwise specified.

Parameter	Min.	Typ.	Max.	Unit	Conditions
Voltage Comparator Section					
Input Impedance		2		MΩ	Measured at Pins 3 and 8
Input Bias Current		100		nA	
Voltage Gain	55	70		dB	R_L = 5.1KΩ
Output Voltage Low		300	500	mV	I_C = 3mA
Output Leakage Current		0.01	10	μA	V_O = 20V
Internal Reference					
Voltage Level	4.9	5.3	5.7	V	Measured at Pin 10
Output Impedance		100		Ω	AC Small Signal
Maximum Source Current		80		μA	

Notes
Parameters are guaranteed over the recommended operating conditions, but are not 100% tested in production
***Bold face parameters** are covered by production test and guaranteed over operating temperature range.*

Specifications are subject to change without notice

ABSOLUTE MAXIMUM RATINGS

Power Supply 20V
Input Signal Level ..... 3V rms
Power Dissipation 900mW

Package Power Dissipation Ratings
CDIP 750mW
Derate Above T_A = 25°C ..... 8mW/°C
PDIP 800mW
Derate Above T_A = 25°C ..... 60mW/°C
SOIC 390mW
Derate Above T_A = 25°C ..... 5mW/°C

SYSTEM DESCRIPTION

The main PLL within the XR-2211 is constructed from an input preamplifier, analog multiplier used as a phase detector and a precision voltage controlled oscillator (VCO). The preamplifier is used as a limiter such that input signals above typically 10mV rms are amplified to a constant high level signal. The multiplying-type phase detector acts as a digital exclusive or gate. Its output (unfiltered) produces sum and difference frequencies of the input and the VCO output. The VCO is actually a current controlled oscillator with its normal input current (f_O) set by a resistor (R_0) to ground and its driving current with a resistor (R_1) from the phase detector.

The output of the phase detector produces sum and difference of the input and the VCO frequencies (internally connected). When in lock, these frequencies are $f_{IN} + f_{VCO}$ (2 times f_{IN} when in lock) and $f_{IN} - f_{VCO}$ (0Hz when lock). By adding a capacitor to the phase detector output, the 2 times f_{IN} component is reduced, leaving a DC voltage that represents the phase difference between the two frequencies. This closes the loop and allows the VCO to track the input frequency.

The FSK comparator is used to determine if the VCO is driven above or below the center frequency (FSK comparator). This will produce both active high and active low outputs to indicate when the main PLL is in lock (quadrature phase detector and lock detector comparator).

PRINCIPLES OF OPERATION

Signal Input (Pin 2): Signal is AC coupled to this terminal. The internal impedance at pin 2 is 20KΩ. Recommended input signal level is in the range of 10mV rms to 3V rms.

Quadrature Phase Detector Output (Pin 3): This is the high impedance output of quadrature phase detector and is internally connected to the input of lock detect voltage comparator. In tone detection applications, pin 3 is connected to ground through a parallel combination of R_D and C_D (see *Figure 3*) to eliminate the chatter at lock detect outputs. If the tone detect section is not used, pin 3 can be left open.

Lock Detect Output, Q (Pin 6): The output at pin 6 is at "low" state when the PLL is out of lock and goes to "high" state when the PLL is locked. It is an open collector type output and requires a pull-up resistor, R_L, to V_{CC} for proper operation. At "low" state, it can sink up to 5mA of load current.

Lock Detect Complement, (Pin 5): The output at pin 5 is the logic complement of the lock detect output at pin 6. This output is also an open collector type stage which can sink 5mA of load current at low or "on" state.

FSK Data Output (Pin 7): This output is an open collector logic stage which requires a pull-up resistor, R_L, to V_{CC} for proper operation. It can sink 5mA of load current. When decoding FSK signals, FSK data output is at "high" or "off" state for low input frequency, and at "low" or "on" state for high input frequency. If no input signal is present, the logic state at pin 7 is indeterminate.

FSK Comparator Input (Pin 8): This is the high impedance input to the FSK voltage comparator. Normally, an FSK post-detection or data filter is connected between this terminal and the PLL phase detector output (pin 11). This data filter is formed by R_F and C_F (see *Figure 3*.) The threshold voltage of the comparator is set by the internal reference voltage, V_{REF}, available at pin 10.

Reference Voltage, V_{REF} (Pin 10): This pin is internally biased at the reference voltage level, V_{REF}: $V_{REF} = V_{CC}/2 - 650mV$. The DC voltage level at this pin forms an internal reference for the voltage levels at pins 5, 8, 11 and 12. Pin 10 must be bypassed to ground with a 0.1μF capacitor for proper operation of the circuit.

Loop Phase Detector Output (Pin 11): This terminal provides a high impedance output for the loop phase detector. The PLL loop filter is formed by R_1 and C_1 connected to pin 11 (see *Figure 3*.) With no input signal, or with no phase error within the PLL, the DC level at pin 11 is very nearly equal to V_{REF}. The peak to peak voltage swing available at the phase detector output is equal to $2 \times V_{REF}$.

VCO Control Input (Pin 12): VCO free-running frequency is determined by external timing resistor, R_0, connected from this terminal to ground. The VCO free-running frequency, f_0, is:

$$f_o = \frac{1}{R_0 \cdot C_0} \; Hz$$

where C_0 is the timing capacitor across pins 13 and 14. For optimum temperature stability, R_0 must be in the range of 10KΩ to 100KΩ (see *Figure 9*.)

This terminal is a low impedance point, and is internally biased at a DC level equal to V_{REF}. The maximum timing current drawn from pin 12 must be limited to ≤ 3mA for proper operation of the circuit.

VCO Timing Capacitor (Pins 13 and 14): VCO frequency is inversely proportional to the external timing capacitor, C_0, connected across these terminals (see *Figure 6*.) C_0 must be non-polar, and in the range of 200pF to 10μF.

VCO Frequency Adjustment: VCO can be fine-tuned by connecting a potentiometer, R_X, in series with R_0 at pin 12 (see *Figure 10*.)

VCO Free-Running Frequency, f_0: XR-2211 does not have a separate VCO output terminal. Instead, the VCO outputs are internally connected to the phase detector sections of the circuit. For set-up or adjustment purposes, the VCO free-running frequency can be tuned by using the generalized circuit in *Figure 3*, and applying an alternating bit pattern of 0's and 1's at the known mark and space frequencies. By adjusting R_0, the VCO can then be tuned to obtain a 50% duty cycle on the FSK output (pin 7). This will ensure that the VCO f_0 value is accurately referenced to the mark and space frequencies.

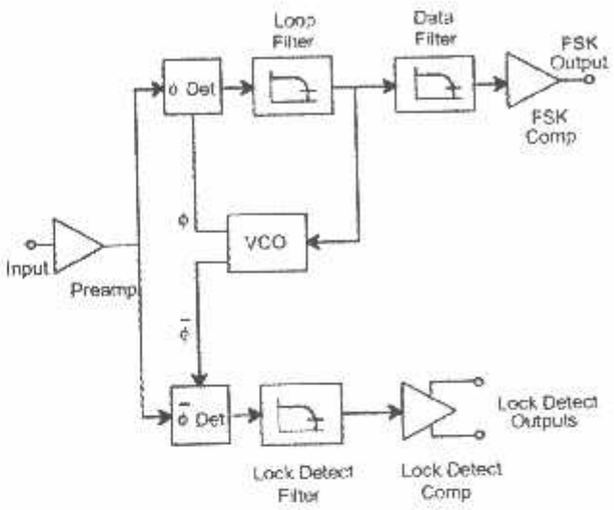


Figure 2. Functional Block Diagram of a Tone and FSK Decoding System Using XR-2211

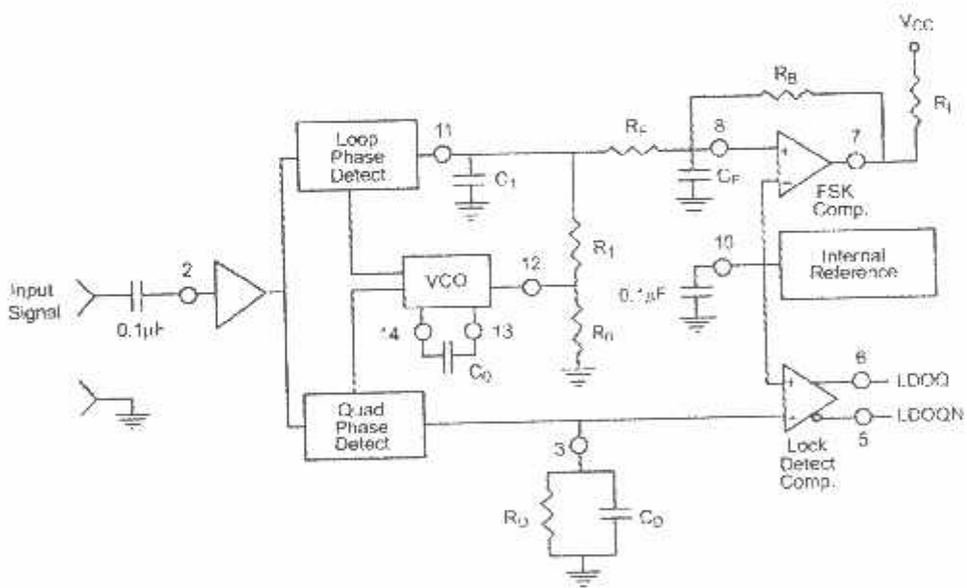


Figure 3. Generalized Circuit Connection for FSK and Tone Detection

DESIGN EQUATIONS

(All resistance in Ω, all frequency in Hz and all capacitance in farads, unless otherwise specified)

(See *Figure 3* for definition of components)

1. VCO Center Frequency, f_O:

$$f_o = \frac{1}{R_0 \cdot C_0}$$

2. Internal Reference Voltage, V_{REF} (measured at pin 10):

$$V_{REF} \approx \left(\frac{V_{cc}}{2}\right) - 650mV \text{ in volts}$$

3. Loop Low-Pass Filter Time Constant, τ:

$$\tau = C_1 \cdot R_{pp} \text{ (seconds)}$$

where:

$$R_{pp} = \left(\frac{R_1 \cdot R_F}{R_1 + R_F}\right)$$

if R_F is ∞ or C_F reactance is ∞, then $R_{pp} = R1$

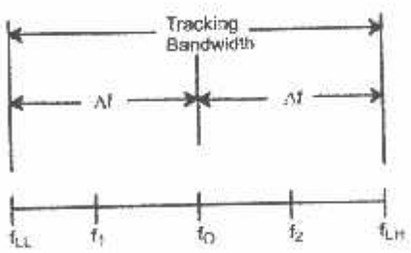
4. Loop Damping, ζ:

$$\zeta = \sqrt{\left(\frac{1250 \cdot C_0}{R_1 \cdot C_1}\right)}$$

Note: *For derivation/explanation of this equation, please see TAN-011.*

5. Loop-tracking bandwidth, $\pm = \frac{\Delta f}{f_o}$

$$\frac{\Delta f}{f_o} = \frac{R_0}{R_1}$$



6. FSK Data filter time constant, tF:

$$\tau_F = \frac{R_B \cdot R_F}{(R_B + R_F)} \cdot C_F \ (seconds)$$

7. Loop phase detector conversion gain, Kd: (Kd is the differential DC voltage across pin 10 and pin11, per unit of phase error at phase detector input):

$$K_d = \frac{V_{REF} \cdot R_1}{10,000 \cdot \pi} \left[\frac{volt}{radian}\right]$$

Note: *For derivation/explanation of this equation, please see TAN-011.*

8. VCO conversion gain, Ko: (Ko is the amount of change in VCO frequency, per unit of DC voltage change at pin 11):

$$K_o = \frac{-2\pi}{V_{REF} \cdot C_0 \cdot R_1} = \left(\frac{radian/second}{volt}\right)$$

9. The filter transfer function:

$$F(s) = \frac{1}{1 + SR_1 \cdot C_1} \text{ at 0 Hz.} \qquad S = j\omega \text{ and } \omega = 0$$

10. Total loop gain, K_T:

$$K_T = K_O \cdot K_d \cdot F(s) = \left(\frac{R_F}{5,000 \cdot C_0 \cdot (R_1 + R_F)}\right)\left[\frac{1}{seconds}\right]$$

11. Peak detector current I_A:

$$I_A = \frac{V_{REF}}{20,000} \ (V_{REF} \text{ in volts and } I_A \text{ in amps})$$

Note: *For derivation/explanation of this equation, please see TAN-011.*

APPLICATIONS INFORMATION

FSK Decoding

Figure 10 shows the basic circuit connection for FSK decoding. With reference to *Figure 3* and *Figure 10*, the functions of external components are defined as follows: R_0 and C_0 set the PLL center frequency, R_1 sets the system bandwidth, and C_1 sets the loop filter time constant and the loop damping factor. C_F and R_F form a one-pole post-detection filter for the FSK data output. The resistor R_B from pin 7 to pin 8 introduces positive feedback across the FSK comparator to facilitate rapid transition between output logic states.

Design Instructions:

The circuit of *Figure 10* can be tailored for any FSK decoding application by the choice of five key circuit components: R_0, R_1, C_0, C_1 and C_F. For a given set of FSK mark and space frequencies, f_0 and f_1, these parameters can be calculated as follows:

(All resistance in Ω's, all frequency in Hz and all capacitance in farads, unless otherwise specified)

a) Calculate PLL center frequency, f_0:

$$f_o = \sqrt{F_1 \cdot F_2}$$

b) Choose value of timing resistor R_0, to be in the range of 10KΩ to 100KΩ. This choice is arbitrary. The recommended value is R_0 = 20KΩ. The final value of R_0 is normally fine-tuned with the series potentiometer, R_X.

$$R_o = R_o + \frac{R_X}{2}$$

c) Calculate value of C0 from design equation (1) or from *Figure 7*:

$$C_o = \frac{1}{R_o \cdot f_o}$$

d) Calculate R1 to give the desired tracking bandwidth (See design equation 5).

$$R_1 = \frac{R_o \cdot f_o}{(f_1 - f_2)} \cdot 2$$

e) Calculate C1 to set loop damping. (See design equation 4):

Normally, $\varsigma = 0.5$ is recommended.

$$C_1 = \frac{1250 \cdot C_o}{R_1 \cdot \varsigma^2}$$

f) The input to the XR-2211 may sometimes be too sensitive to noise conditions on the input line. *Figure 4* illustrates a method of de-sensitizing the XR-2211 from such noisy line conditions by the use of a resistor, Rx, connected from pin 2 to ground. The value of Rx is chosen by the equation and the desired minimum signal threshold level.

$$V_{IN}\ minimum\ (peak) = V_a - V_b = \Delta V \pm 2.8mV\ offset = V_{REF}\frac{20,000}{(20,000 + R_x)}\ or\ R_x = 20,000\left(\frac{V_{REF}}{\Delta V} - 1\right)$$

V_{IN} minimum (peak) input voltage must exceed this value to be detected (equivalent to adjusting V threshold)

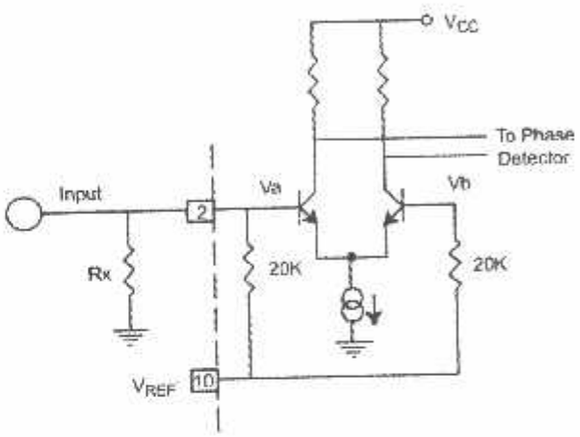


Figure 4. Desensitizing Input Stage

g) Calculate Data Filter Capacitance, C_F:

$$R_{sum} = \frac{(R_e + R_1)\cdot R_\theta}{(R_1 + R_e + R_\theta)}$$

$$C_f = \frac{0.25}{(R_{sum}\cdot Baud\ Rate)} \qquad Baud\ rate\ in\ \frac{1}{seconds}$$

Note: *All values except R_0 can be rounded to nearest standard value.*

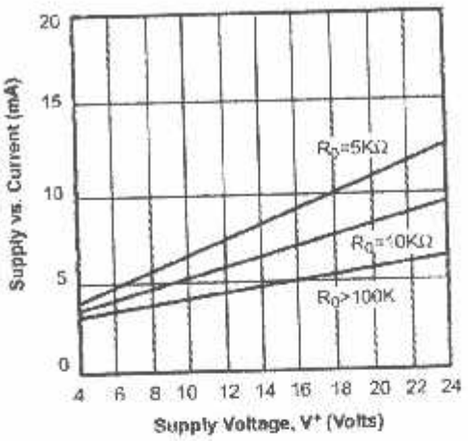


Figure 5. Typical Supply Current vs. V+ (Logic Outputs Open Circuited)

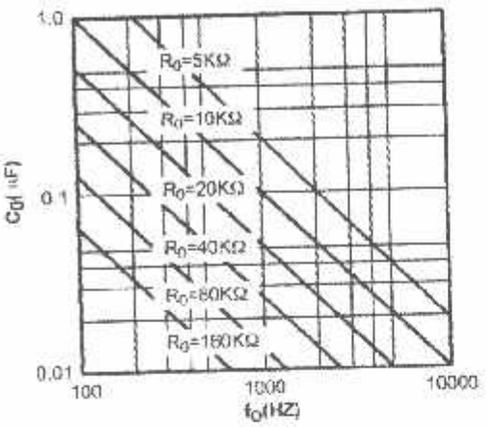


Figure 6. VCO Frequency vs. Timing Resistor

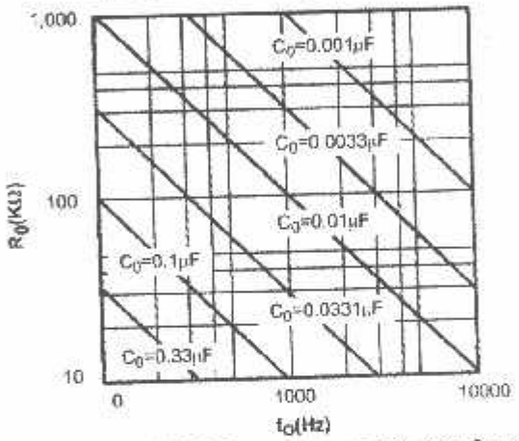


Figure 7. VCO Frequency vs. Timing Capacitor

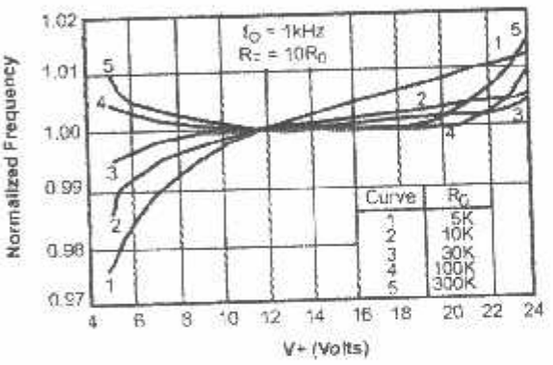


Figure 8. Typical f_O vs. Power Supply Characteristics

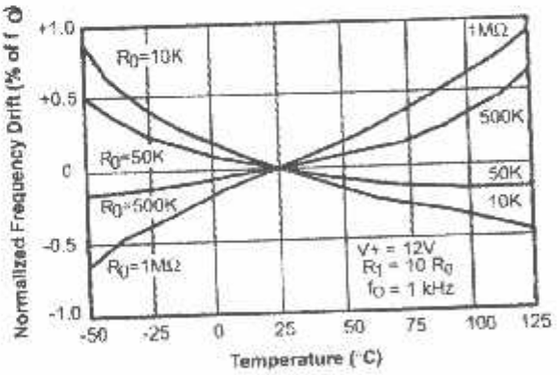


Figure 9. Typical Center Frequency Drift vs. Temperature

Design Example:

1200 Baud FSK demodulator with mark and space frequencies of 1200/2200.

Step 1: Calculate f_O: from design instructions

(a) $f_o = \sqrt{1200 \cdot 2200} = 1624$

Step 2: Calculate R_0 : R_0 =10K with a potentiometer of 10K. (See design instructions (b))

(b) $R_T = 10 + \left(\frac{10}{2}\right) = 15K$

Step 3: Calculate C_0 from design instructions

(c) $C_0 = \frac{1}{15000 \cdot 1624} = 39nF$

Step 4: Calculate R_1 : from design instructions

(d) $R_1 = \frac{20000 \cdot 1624 \cdot 2}{(2200-1200)} = 51,000$

Step 5: Calculate C_1 : from design instructions

(e) $C_1 = \frac{1250 \cdot 39nF}{51000 \cdot 0.5^2} = 3.9nF$

Step 6: Calculate R_F : R_F should be at least five times R_1, $R_F = 51,000 \cdot 5 = 255\ K\Omega$

Step 7: Calculate R_B : R_B should be at least five times R_F, $R_B = 255,000 \cdot 5 = 1.2\ M\Omega$

Step 8: Calculate R_{SUM} :

$$R_{SUM} = \frac{(R_F + R_1) \cdot R_B}{(R_F + R_1 + R_B)} = 240K\Omega$$

Step 9: Calculate C_F :

$$C_F = \frac{0.25}{(R_{SUM} \cdot Baud\ Rate)} = 1nF$$

Note: *All values except R_0 can be rounded to nearest standard value.*

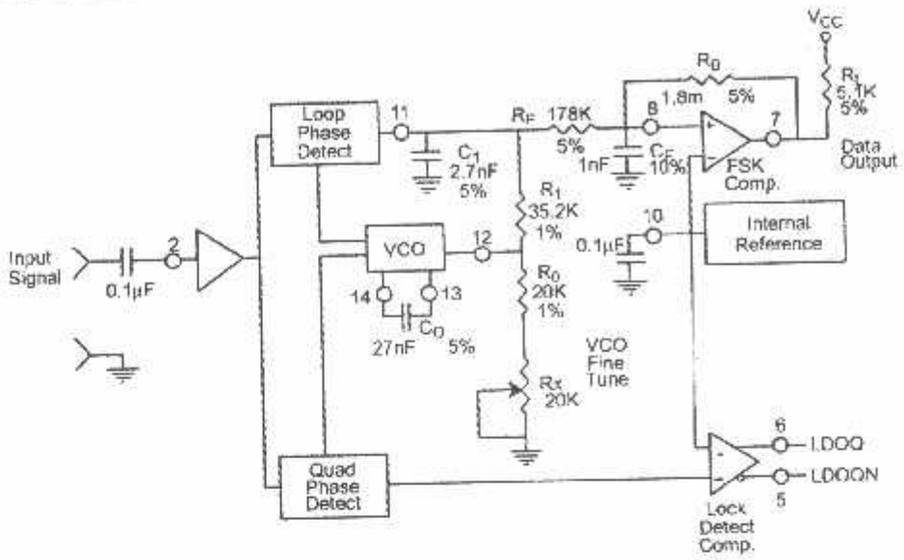


Figure 10. Circuit Connection for FSK Decoding of Caller Identification Signals (Bell 202 Format)

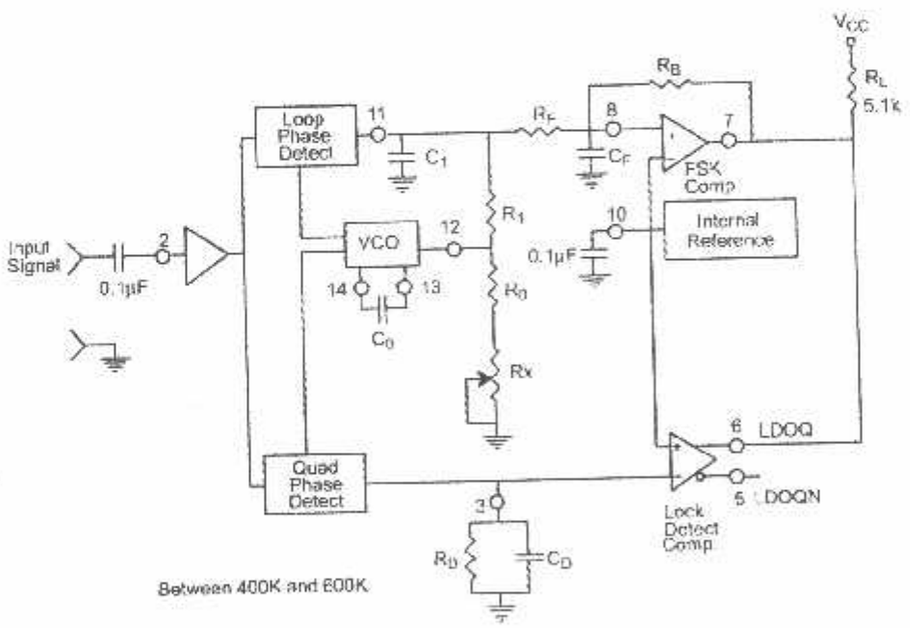


Figure 11. External Connectors for FSK Demodulation with Carrier Detect Capability

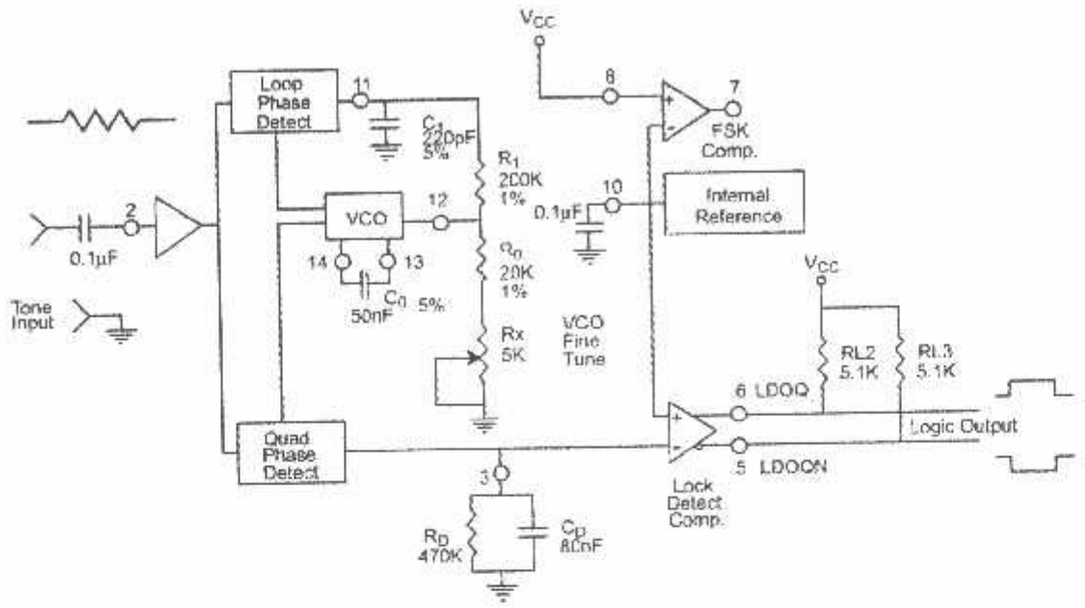


Figure 12. Circuit Connection for Tone Detection

FSK Decoding with Carrier Detect

The lock detect section of XR-2211 can be used as a carrier detect option for FSK decoding. The recommended circuit connection for this application is shown in *Figure 11*. The open collector lock detect output, pin 6, is shorted to data output (pin 7). Thus, data output will be disabled at "low" state, until there is a carrier within the detection band of the PLL and the pin 6 output goes "high" to enable the data output.

***Note:** Data Output is "Low" When No Carrier is Present.*

The minimum value of the lock detect filter capacitance C_D is inversely proportional to the capture range, $\pm\Delta fc$. This is the range of incoming frequencies over which the loop can acquire lock and is always less than the tracking range. It is further limited by C_1. For most applications, $\Delta fc > \Delta f/2$. For $R_D = 470K\Omega$, the approximate minimum value of C_D can be determined by:

$$C_D > \frac{16}{\Delta f} \quad C \text{ in } \mu F \text{ and } f \text{ in Hz.}$$

C in µF and f in Hz.

With values of C_D that are too small, chatter can be observed on the lock detect output as an incoming signal frequency approaches the capture bandwidth. Excessively large values of C_D will slow the response time of the lock detect output. For Caller I.D. applications choose $C_D = 0.1\mu F$.

Tone Detection

Figure 12 shows the generalized circuit connection for tone detection. The logic outputs, LDOQN and LDOQ at pins 5 and 6 are normally at "high" and "low" logic states, respectively. When a tone is present within the detection band of the PLL, the logic state at these outputs become reversed for the duration of the input tone. Each logic output can sink 5mA of load current.

Both outputs at pins 5 and 6 are open collector type stages, and require external pull-up resistors R_{L2} and R_{L3}, as shown in *Figure 12*.

With reference to *Figure 3* and *Figure 12*, the functions of the external circuit components can be explained as follows. R_0 and C_0 set VCO center frequency; R_1 sets the detection bandwidth; C_1 sets the low pass-loop filter time constant and the loop damping factor.

Design Instructions:

The circuit of *Figure 12* can be optimized for any tone detection application by the choice of the 5 key circuit components: R_0, R_1, C_0, C_1 and C_D. For a given input, the tone frequency, f_S, these parameters are calculated as follows:

(All resistance in Ω's, all frequency in Hz and all capacitance in farads, unless otherwise specified)

a) Choose value of timing resistor R_0 to be in the range of 10KΩ to 50KΩ. This choice is dictated by the max./min. current that the internal voltage reference can deliver. The recommended value is R_0 = 20KΩ. The final value of R_0 is normally fine-tuned with the series potentiometer, R_X.

b) Calculate value of C_0 from design equation (1) or from *Figure 7* $f_S = f_O$:

$$C_0 = \frac{1}{R_0 \cdot fs}$$

c) Calculate R_1 to set the bandwidth $\pm\Delta f$ (See design equation 5):

$$R_1 = \frac{R_0 \cdot f_0 \cdot 2}{\Delta f}$$

***Note:** The total detection bandwidth covers the frequency range of $f_O \pm \Delta f$*

d) Calculate value of C_1 for a given loop damping factor:

Normally, $\varsigma = 0.5$ is recommended.

$$C_1 = \frac{1250 \cdot C_0}{R_1 \cdot \varsigma^2}$$

Increasing C_1 improves the out-of-band signal rejection, but increases the PLL capture time.

e) Calculate value of the filter capacitor C_D. To avoid chatter at the logic output, with R_D = 470KΩ, C_D must be:

$$C_D > \frac{16}{\Delta f} \quad C \text{ in } \mu F$$

Increasing C_D slows down the logic output response time.

Design Examples:

Tone detector with a detection band of ± 100Hz:

a) Choose value of timing resistor R_0 to be in the range of 10KΩ to 50KΩ. This choice is dictated by the max./min. current that the internal voltage reference can deliver. The recommended value is R_0 = 20 KΩ. The final value of R_0 is normally fine-tuned with the series potentiometer, R_X.

b) Calculate value of C_0 from design equation (1) or from *Figure 6* $f_S = f_O$:

$$C_0 = \frac{1}{R_0 \cdot f_s} = \frac{1}{20,000 \cdot 1,000} = 50nF$$

c) Calculate R_1 to set the bandwidth $\pm\Delta f$ (See design equation 5):

$$R_1 = \frac{R_0 \cdot f_0 \cdot 2}{\Delta f} = \frac{20,000 \cdot 1,000 \cdot 2}{100} = 400K$$

Note: *The total detection bandwidth covers the frequency range of $f_0 \pm \Delta f$*

d) Calculate value of C_0 for a given loop damping factor:

Normally, $\zeta = 0.5$ is recommended.

$$C_1 = \frac{1250 \cdot C_D}{R_1 \cdot \zeta^2} = \frac{1250 \cdot 50 \cdot 10^{-6}}{400,000 \cdot 0.5^2} = 6.25pF$$

Increasing C_1 improves the out-of-band signal rejection, but increases the PLL capture time.

e) Calculate value of the filter capacitor C_D . To avoid chatter at the logic output, with R_D = 470KΩ, C_D must be:

$$C_D = \frac{16}{\Delta f} \geq \frac{16}{200} \geq 80nF$$

Increasing C_D slows down the logic output response time.

f) Fine tune center frequency with 5KΩ potentiometer, R_X.

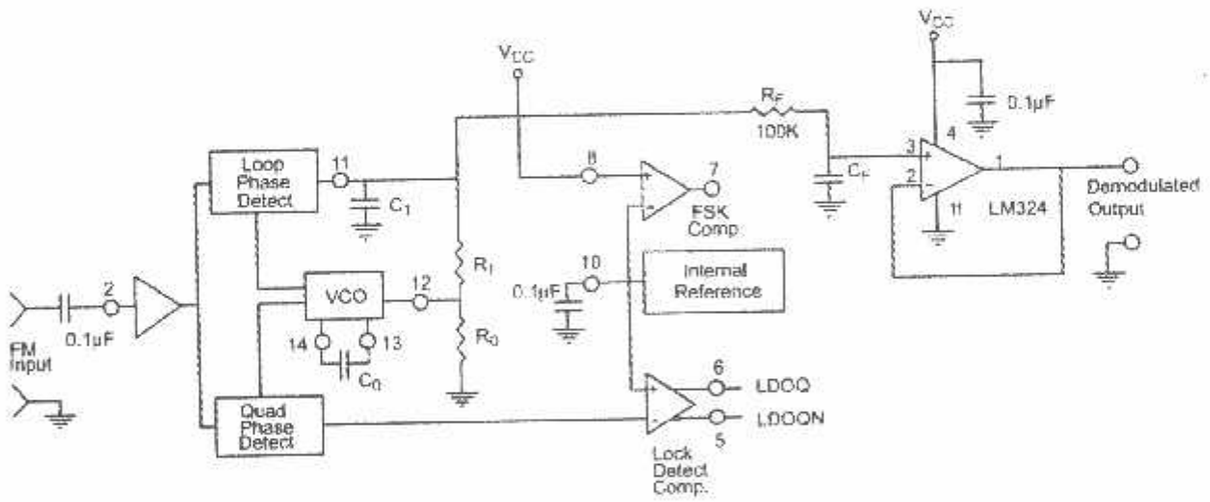


Figure 13. Linear FM Detector Using XR-2211 and an External Op Amp. (See Section on Design Equation for Component Values.)

Linear FM Detection

XR-2211 can be used as a linear FM detector for a wide range of analog communications and telemetry applications. The recommended circuit connection for this application is shown in *Figure 13*. The demodulated output is taken from the loop phase detector output (pin 11), through a post-detection filter made up of R_F and C_F and an external buffer amplifier. This buffer amplifier is necessary because of the high impedance output at pin 11. Normally, a non-inverting unity gain op amp can be used as a buffer amplifier, as shown in *Figure 13*.

The FM detector gain, i.e., the output voltage change per unit of FM deviation can be given as:

$$V_{OUT} = \frac{R_1 \cdot V_{REF}}{100 \cdot R_0}$$

where VR is the internal reference voltage ($V_{REF} = V_{CC}/2 - 650mV$). For the choice of external components R_1, R_0, C_D, C_1 and C_F, see the section on design equations.

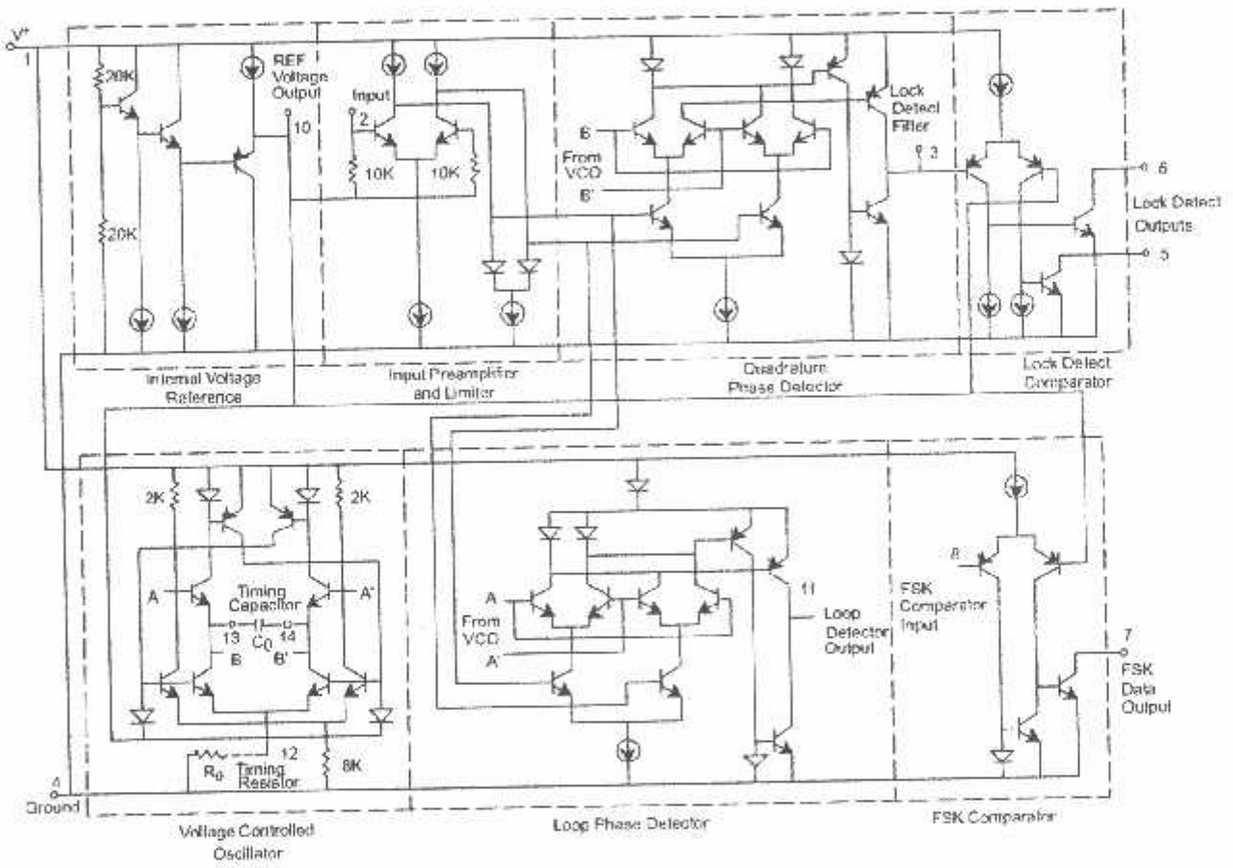
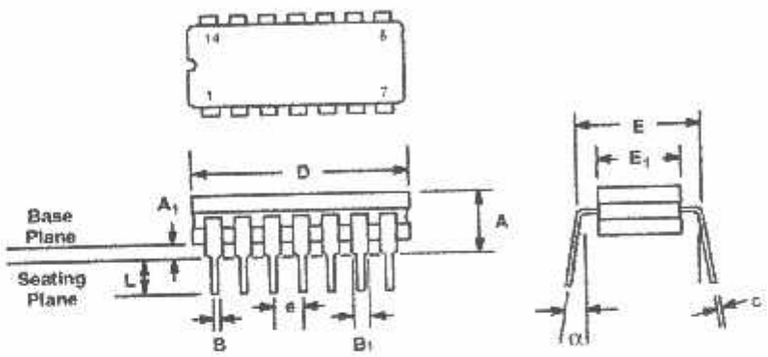


Figure 14. Equivalent Schematic Diagram

14 LEAD CERAMIC DUAL-IN-LINE (300 MIL CDIP)

Rev. 1.00

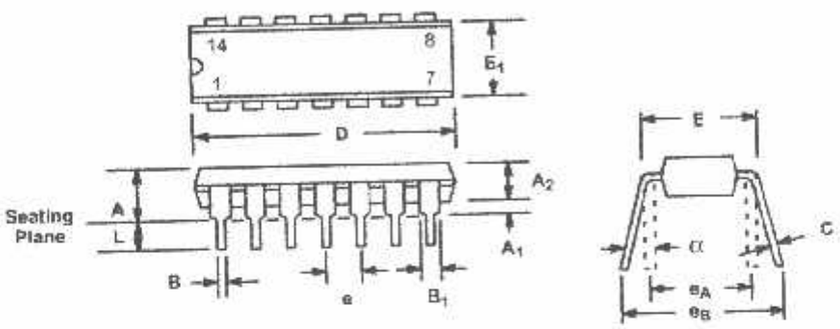


SYMBOL	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.100	0.200	2.54	5.08
A_1	0.015	0.060	0.38	1.52
B	0.014	0.026	0.36	0.66
B_1	0.045	0.065	1.14	1.65
c	0.008	0.018	0.20	0.46
D	0.685	0.785	17.40	19.94
E_1	0.250	0.310	6.35	7.87
E	0.300 BSC		7.62 BSC	
e	0.100 BSC		2.54 BSC	
L	0.125	0.200	3.18	5.08
α	0°	15°	0°	15°

Note: The control dimension is the inch column

14 LEAD PLASTIC DUAL-IN-LINE (300 MIL PDIP)

Rev. 1.00

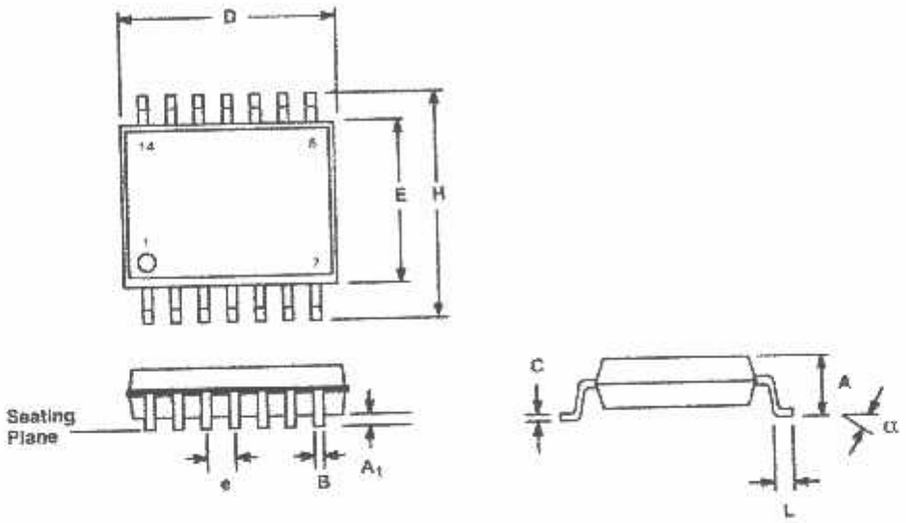


SYMBOL	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.145	0.210	3.68	5.33
A_1	0.015	0.070	0.38	1.78
A_2	0.115	0.195	2.92	4.95
B	0.014	0.024	0.36	0.56
B_1	0.030	0.070	0.76	1.78
C	0.008	0.014	0.20	0.38
D	0.725	0.795	18.42	20.19
E	0.300	0.325	7.62	8.26
E_1	0.240	0.280	6.10	7.11
e	0.100 BSC		2.54 BSC	
e_A	0.300 BSC		7.62 BSC	
e_B	0.310	0.430	7.87	10.92
L	0.115	0.160	2.92	4.06
α	0°	15°	0°	15°

Note: The control dimension is the inch column

14 LEAD SMALL OUTLINE (150 MIL JEDEC SOIC)

Rev. 1.00



SYMBOL	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.053	0.069	1.35	1.75
A_1	0.004	0.010	0.10	0.25
B	0.013	0.020	0.33	0.51
C	0.007	0.010	0.19	0.25
D	0.337	0.344	8.55	8.75
E	0.150	0.157	3.80	4.00
e	0.050 BSC		1.27 BSC	
H	0.226	0.244	5.80	6.20
L	0.016	0.050	0.40	1.27
α	0°	8°	0°	8°

Note: The control dimension is the millimeter column

Notes

Notes

NOTICE

EXAR Corporation reserves the right to make changes to the products contained in this publication in order to improve design, performance or reliability. EXAR Corporation assumes no responsibility for the use of any circuits described herein, conveys no license under any patent or other right, and makes no representation that the circuits are free of patent infringement. Charts and schedules contained here in are only for illustration purposes and may vary depending upon a user's specific application. While the information in this publication has been carefully checked; no responsibility, however, is assumed for inaccuracies.

EXAR Corporation does not recommend the use of any of its products in life support applications where the failure or malfunction of the product can reasonably be expected to cause failure of the life support system or to significantly affect its safety or effectiveness. Products are not authorized for use in such applications unless EXAR Corporation receives, in writing, assurances to its satisfaction that: (a) the risk of injury or damage has been minimized; (b) the user assumes all such risks; (c) potential liability of EXAR Corporation is adequately protected under the circumstances.

MAXIM

+5V-Powered, Multichannel RS-232 Drivers/Receivers

General Description

The MAX220–MAX249 family of line drivers/receivers is intended for all EIA/TIA-232E and V.28/V.24 communications interfaces, particularly applications where ±12V is not available.

These parts are especially useful in battery-powered systems, since their low-power shutdown mode reduces power dissipation to less than 5µW. The MAX225, MAX233, MAX235, and MAX245/MAX246/MAX247 use no external components and are recommended for applications where printed circuit board space is critical.

Applications

Portable Computers

Low-Power Modems

Interface Translation

Battery-Powered RS-232 Systems

Multi-Drop RS-232 Networks

Features

Superior to Bipolar

- Operate from Single +5V Power Supply (+5V and +12V—MAX231/MAX239)
- Low-Power Receive Mode in Shutdown (MAX223/MAX242)
- Meet All EIA/TIA-232E and V.28 Specifications
- Multiple Drivers and Receivers
- 3-State Driver and Receiver Outputs
- Open-Line Detection (MAX243)

Ordering Information

PART	TEMP. RANGE	PIN-PACKAGE
MAX220CPE	0°C to +70°C	16 Plastic DIP
MAX220CSE	0°C to +70°C	16 Narrow SO
MAX220CWE	0°C to +70°C	16 Wide SO
MAX220C/D	0°C to +70°C	Dice*
MAX220EPE	-40°C to +85°C	16 Plastic DIP
MAX220ESE	-40°C to +85°C	16 Narrow SO
MAX220EWE	-40°C to +85°C	16 Wide SO
MAX220EJE	-40°C to +85°C	16 CERDIP
MAX220MJE	-55°C to +125°C	16 CERDIP

Ordering Information continued at end of data sheet.

Contact factory for dice specifications.

Selection Table

Part Number	Power Supply (V)	No. of RS-232 Drivers/Rx	No. of Ext. Caps	Nominal Cap. Value (µF)	SHDN & Three-State	Rx Active in SHDN	Data Rate (kbps)	Features
MAX220	+5	2/2	4	0.1	No	No	120	
MAX222	+5	2/2	4	0.1	No	Yes	120	
MAX223 (MAX213)	+5	4/5	4	0.1	Yes	Yes	120	
MAX225	+5	5/5	0	—	Yes	No	120	
MAX230 (MAX200)	+5	5/0	4	0.1	Yes	No	120	
MAX231 (MAX201)	+5 and +12 to +15	2/2	2	1.0	No	No	120	
MAX232 (MAX202)	+5	2/2	4	0.1	No	No	120	
MAX233	+5	2/2	0	—	No	No	120	
MAX234 (MAX204)	+5	4/0	0	—	No	No	120	
MAX235	+5	5/5	0	—	Yes	No	120	
MAX236 (MAX206)	+5	4/3	0	—	Yes	No	120	
MAX237 (MAX207)	+5	5/3	0	—	No	No	120	
MAX238 (MAX208)	+5	4/4	0	—	No	No	120	
MAX239 (MAX209)	+5 and +12 to +15	4/5	2	1.0	Yes	No	120	
MAX240	+5	5/5	4	0.1	Yes	No	120	
MAX241 (MAX211)	+5 and +12 to +15	4/5	4	0.1	Yes	Yes	120	
MAX242	+5	2/2	4	0.1	Yes	Yes	120	
MAX243	+5	2/2	4	0.1	No	Yes	120	
MAX244	+5	8/10	0	—	Yes	No	120	
MAX245	+5	8/10	0	—	Yes	Yes	120	
MAX246	+5	8/10	0	—	Yes	Yes	120	
MAX247	+5	8/9	4	0.1	Yes	Yes	120	
MAX248	+5	8/8	4	0.1	Yes	Yes	120	
MAX249	+5	6/10	4	0.1	Yes	Yes	120	

ABSOLUTE MAXIMUM RATINGS—MAX220/222/232A/233A/242/243

Supply Voltage (Vcc) ..... 0.3V to +6V

Input Voltages

T_IN ..... -0.3V to (Vcc + 0.3V)

R_IN ..... ±30V

T_OUT (Note 1) ..... ±15V

Output Voltages

T_OUT ..... ±15V

R_OUT ..... -0.3V to (Vcc + 0.3V)

Driver/Receiver Output Short Circuited to GND ..... Continuous

Continuous Power Dissipation (T_A = +70°C)

16-Pin Plastic DIP (derate 10.53mW/°C above +70°C) 842mW

16-Pin Wide SO (derate 9.52mW/°C above +70°C) 762mW

18-Pin Plastic DIP (derate 11.11mW/°C above +70°C) 889mW

20-Pin Wide SO (derate 10.00mW/°C above +70°C) 800mW

20-Pin SSOP (derate 8.00mW/°C above +70°C) 640mW

20-Pin CERDIP (derate 11.11mW/°C above +70°C) 889mW

24-Pin CERDIP (derate 12.50mW/°C above +70°C) 1000mW

Operating Temperature Ranges

MAX2_ _AC_ / MAX2_ _C_ _ ..... 0°C to +70°C

MAX2_ _AE_ _ / MAX2_ _E_ _ ..... -40°C to +85°C

MAX2_ _AM_ / MAX2_ _M ..... -55°C to +125°C

Storage Temperature Range ..... -65°C to +160°C

Lead Temperature (soldering, 10sec) ..... +300°C

Note 1: Input voltage measured with T_OUT in high-impedance state, SHDN or Vcc = 0V.

ELECTRICAL CHARACTERISTICS—MAX220/222/232A/233A/242/243

(Vcc = +5V ±10%, C1–C4 = 0.1µF, T_A = T_{MIN} to T_{MAX}, unless otherwise noted.)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
RS-232 TRANSMITTERS					
Output Voltage Swing	All transmitter outputs loaded with 3kΩ to GND	±5	±8		V
Input Logic Threshold Low			1.4	0.8	V
Input Logic Threshold High		2	1.4		V
Logic Pull-Up Input Current	Normal operation		5	40	µA
	SHDN = 0V (MAX223/MAX242 only)		±0.01	±1	
Output Leakage Current	Vcc = +5V or 0V, SHDN = 0V, V_OUT = ±15V, MAX222/242		±0.05	±10	µA
	MAX223, SHDN = 0V, V_OUT = ±15V		±0.05	±10	
Data Rate	All except MAX220, normal operation		22	20	kbps
	MAX220		1		Mbps
Transmitter Output Resistance	Vcc = V+ = V- = 0V, V_OUT = ±2V	300	10M		Ω
Output Short-Circuit Current	V_OUT = 0V		±7	±22	mA
RS-232 RECEIVERS					
RS-232 Input Voltage Operating Range				±30	V
RS-232 Input Threshold Low	Vcc = 5V	All except MAX243 R2	0.8	1.3	V
		MAX243 R2 (Note 2)	1	1.5	
RS-232 Input Threshold High	Vcc = 5V	All except MAX243 R2		1.8	2.4
		MAX243 R2 (Note 2)		0.5	0.8
RS-232 Input Hysteresis	All except MAX243, Vcc = 5V, no hysteresis in shdn		0.5	1.0	V
	MAX243		0.15		
RS-232 Input Resistance		3	5	7	kΩ
TTL/CMOS Output Voltage Low	I_OUT = 1.6mA		0.2	0.4	V
TTL/CMOS Output Voltage High	I_OUT = -1.0mA	3.5	Vcc - 0.2		V
TTL/CMOS Output Short-Circuit Current	Sourcing V_OUT = GND		-2	-10	mA
	Sinking V_OUT = Vcc		10	30	
TTL/CMOS Output Leakage Current	SHDN = Vcc or 0V, 5V < V_OUT < 5.5V		±0.05	±10	µA

ELECTRICAL CHARACTERISTICS—MAX220/222/232A/233A/242/243 (continued)

(VCC = +5V ±10%, C1–C4 = 0.1µF, T_A = T_{MIN} to T_{MAX}, unless otherwise noted.)

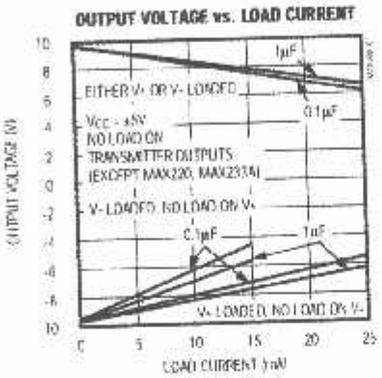
PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
EN Input Threshold Low	MAX242			1.4	0.8	V
EN Input Threshold High	MAX242		2.0	1.4		V
Operating Supply Voltage			4.5		5.5	V
VCC Supply Current (SHDN = VCC) Figures 5, 6, 7, 10	No load	MAX220		0.5	2	mA
		MAX222/232A/233A/242/243		4	10	
	3kΩ load both inputs	MAX220		12		
		MAX222/232A/233A/242/243		15		
Shutdown Supply Current	MAX222/242	T_A = +25°C		0.1	10	µA
		T_A = 0°C to +70°C		2	50	
		T_A = -40°C to +85°C		2	50	
		T_A = -55°C to +125°C		35	100	
SHDN Input Leakage Current	MAX222/242				±1	µA
SHDN Threshold Low	MAX222/242			1.4	0.8	V
SHDN Threshold High	MAX222/242		2.0	1.4		V
Transition Slew Rate	C_L = 50pF to 2500pF, R_L = 3kΩ to 7kΩ, VCC = 5V, T_A = +25°C, measured from +3V to -3V or -3V to +3V	MAX222/232A/233A/242/243	6	12	30	V/µs
		MAX223	1.5	3	30	
Transmitter Propagation Delay TLL to RS-232 (normal operation), Figure 1	t_{PHL}	MAX222/232A/233A/242/243		1.3	3.5	µs
		MAX220		4	10	
	t_{PLH}	MAX222/232A/233A/242/243		1.5	3.5	
		MAX220		5	10	
Receiver Propagation Delay RS-232 to TTL (normal operation) Figure 2	t_{PHLR}	MAX222/232A/233A/242/243		0.5	1	µs
		MAX220		0.6	3	
	t_{PLHR}	MAX222/232A/233A/242/243		0.6	1	
		MAX220		0.8	3	
Receiver Propagation Delay RS-232 to TTL (shutdown), Figure 2	t_{PHLS}	MAX242		3.5	10	µs
	t_{PLHS}	MAX242		2.5	10	
Receiver-Output Enable Time, Figure 3	t_{ER}	MAX242		125	500	ns
Receiver-Output Disable Time, Figure 3	t_{DR}	MAX242		160	500	ns
Transmitter-Output Enable Time (SHDN goes high), Figure 4	t_{ET}	MAX222/242, 0.1µF caps (includes charge-pump start-up)		250		µs
Transmitter-Output Disable Time (SHDN goes low), Figure 4	t_{DT}	MAX222/242, 0.1µF caps		500		ns
Transmitter + to - Propagation Delay Difference (normal operation)	t_{PHLT} - t_{PLHT}	MAX222/232A/233A/242/243		300		ns
		MAX220		2000		
Receiver + to - Propagation Delay Difference (normal operation)	t_{PHLR} - t_{PLHR}	MAX222/232A/233A/242/243		100		ns
		MAX220		225		

Note 2: MAX243 $R2_{OUT}$ is guaranteed to be low when $R2_{IN}$ is ≥ 0V or is floating.

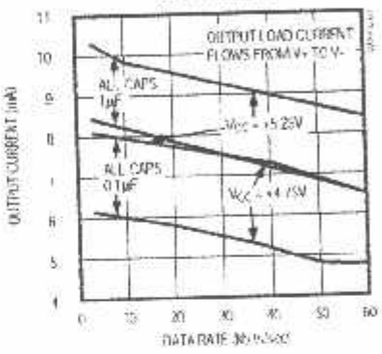
Typical Operating Characteristics

MAX220/MAX222/MAX232A/MAX233A/MAX242/MAX243

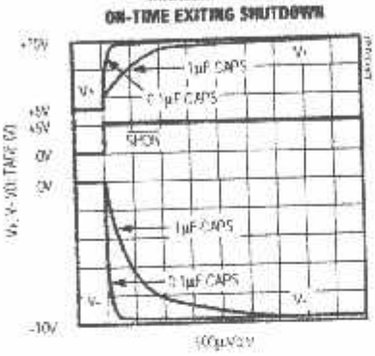
OUTPUT VOLTAGE vs. LOAD CURRENT



AVAILABLE OUTPUT CURRENT vs. DATA RATE



MAX222/MAX242 ON-TIME EXITING SHUTDOWN



ABSOLUTE MAXIMUM RATINGS—MAX223/MAX230–MAX241

V_{CC} ..... -0.3V to +6V
V+ ..... (V_{CC} - 0.3V) to +14V
V- ..... +0.3V to -14V
Input Voltages
T_{IN} ..... -0.3V to (V_{CC} + 0.3V)
R_{IN} ..... ±30V
Output Voltages
T_{OUT} ..... (V+ + 0.3V) to (V- - 0.3V)
R_{OUT} ..... -0.3V to (V_{CC} + 0.3V)
Short-Circuit Duration, T_{OUT} ..... Continuous
Continuous Power Dissipation (T_A = +70°C)
14-Pin Plastic DIP (derate 10.00mW/°C above +70°C) 800mW
16-Pin Plastic DIP (derate 10.53mW/°C above +70°C) 842mW
20-Pin Plastic DIP (derate 11.11mW/°C above +70°C) 889mW
24-Pin Narrow Plastic DIP (derate 13.33mW/°C above +70°C) 1.07W
24-Pin Plastic DIP (derate 9.09mW/°C above +70°C) 500mW
16-Pin Wide SO (derate 9.52mW/°C above +70°C) 762mW
20-Pin Wide SO (derate 10.00mW/°C above +70°C) 800mW
24-Pin Wide SO (derate 11.76mW/°C above +70°C) 941mW
28-Pin Wide SO (derate 12.50mW/°C above +70°C) 1W
44-Pin Plastic FP (derate 11.11mW/°C above +70°C) 889mW
14-Pin CERDIP (derate 9.09mW/°C above +70°C) 727mW
16-Pin CERDIP (derate 10.00mW/°C above +70°C) 800mW
20-Pin CERDIP (derate 11.11mW/°C above +70°C) 889mW
24-Pin Narrow CERDIP (derate 12.50mW/°C above +70°C) 1W
24-Pin Sidebraze (derate 20.0mW/°C above +70°C) 1.6W
28-Pin SSOP (derate 9.52mW/°C above +70°C) 762mW
Operating Temperature Ranges
MAX2__C__ ..... 0°C to +70°C
MAX2__E__ ..... -40°C to +85°C
MAX2__M__ ..... -55°C to +125°C
Storage Temperature Range ..... -65°C to +160°C
Lead Temperature (soldering, 10sec) ..... +300°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS—MAX223/MAX230–MAX241

(MAX223/230/232/234/236/237/238/240/241, V_{CC} = +5V ±10%; MAX233/MAX235, V_{CC} = 5V ±5%; C1–C4 = 1.0µF; MAX231/MAX239, V_{CC} = 5V ±10%; V+ = 7.5V to 13.2V; T_A = T_{MIN} to T_{MAX}, unless otherwise noted.)

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Output Voltage Swing	All transmitter outputs loaded with 3kΩ to ground		±5.0	±7.3		V
V_{CC} Power-Supply Current	No load, T_A = +25°C	MAX232/233		5	10	mA
		MAX223/230/234–238/240/241		7	15	
		MAX231/239		0.4	1	
V+ Power-Supply Current		MAX231		1.8	5	mA
		MAX239		5	15	
Shutdown Supply Current	T_A = +25°C	MAX223		15	50	µA
		MAX230/235/236/240/241		1	10	
Input Logic Threshold Low	T_{IN}; EN, SHDN (MAX233); $\overline{EN}$, SHDN (MAX230/235–241)				0.8	V
Input Logic Threshold High	T_{IN}		2.0			V
	EN, SHDN (MAX223); $\overline{EN}$, SHDN (MAX230/235/236/240/241)		2.4			
Logic Pull-Up Current	T_{IN} = 0V			1.5	200	µA
Receiver Input Voltage Operating Range			-30		30	V

ELECTRICAL CHARACTERISTICS—MAX223/MAX230–MAX241 (continued)

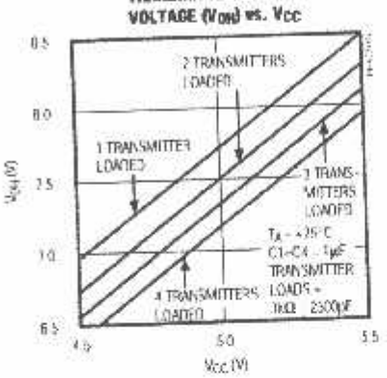
(MAX223/230/232/234/236/237/238/240/241, V_{CC} = +5V ±10; MAX233/MAX235, V_{CC} = 5V ±5%, C1–C4 = 1.0µF; MAX231/MAX239, V_{CC} = 5V ±10%; V+ = 7.5V to 13.2V; T_A = T_{MIN} to T_{MAX}; unless otherwise noted.)

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
RS-232 Input Threshold Low	T_A = +25°C, V_{CC} = 5V	Normal operation $\overline{SHDN}$ = 5V (MAX223) SHDN = 0V (MAX235/236/240/241)	0.8	1.2		V
		Shutdown (MAX223) $\overline{SHDN}$ = 0V, $\overline{EN}$ = 5V ($R4_{IN}$, $R5_{IN}$)	0.6	1.5		
RS-232 Input Threshold High	T_A = +25°C, V_{CC} = 5V	Normal operation $\overline{SHDN}$ = 5V (MAX223) SHDN = 0V (MAX235/236/240/241)		1.7	2.4	V
		Shutdown (MAX223) $\overline{SHDN}$ = 0V, $\overline{EN}$ = 5V ($R4_{IN}$, $R5_{IN}$)		1.5	2.4	
RS-232 Input Hysteresis	V_{CC} = 5V, no hysteresis in shutdown		0.2	0.5	1.0	V
RS-232 Input Resistance	T_A = +25°C, V_{CC} = 5V		3	5	7	kΩ
TTL/CMOS Output Voltage Low	I_{OUT} = 1.6mA (MAX231/232/233 I_{OUT} = 3.2mA)				0.4	V
TTL/CMOS Output Voltage High	I_{OUT} = -1mA		3.5	V_{CC} - 0.4		V
TTL/CMOS Output Leakage Current	0V ≤ R_{OUT} ≤ V_{CC}; $\overline{EN}$ = 0V (MAX223); $\overline{EN}$ = V_{CC} (MAX233–241)			0.05	±10	µA
Receiver Output Enable Time	Normal operation	MAX223		600		ns
		MAX235/236/239/240/241		400		
Receiver Output Disable Time	Normal operation	MAX223		900		ns
		MAX235/236/239/240/241		250		
Propagation Delay	RS-232 IN to TTL/CMOS OUT, C_L = 150pF	Normal operation		0.5	10	µs
		$\overline{SHDN}$ = 0V (MAX223) t_{PHLS}		4	40	
		t_{PLHS}		6	40	
Transition Region Slew Rate	MAX223/MAX230/MAX234–241, T_A = +25°C, V_{CC} = 5V, R_L = 3kΩ to 7kΩ, C_L = 50pF to 2500pF, measured from +3V to -3V or -3V to +3V		3	5.1	30	V/µs
	MAX231/MAX232/MAX233, T_A = +25°C, V_{CC} = 5V, R_L = 3kΩ to 7kΩ, C_L = 50pF to 2500pF, measured from +3V to -3V or -3V to +3V			4	30	
Transmitter Output Resistance	V_{CC} = V+ = V- = 0V, V_{OUT} = ±2V		300			Ω
Transmitter Output Short-Circuit Current				±10		mA

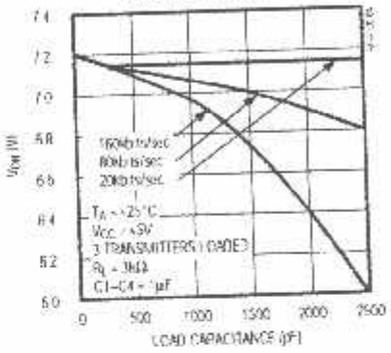
Typical Operating Characteristics

MAX223/MAX230–MAX241

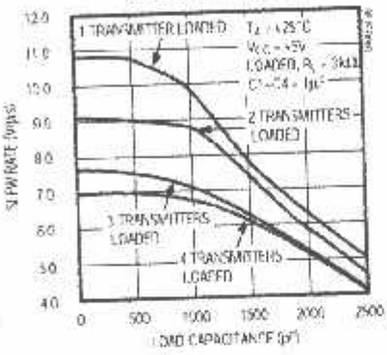
TRANSMITTER OUTPUT VOLTAGE (V_{OH}) vs. V_{CC}



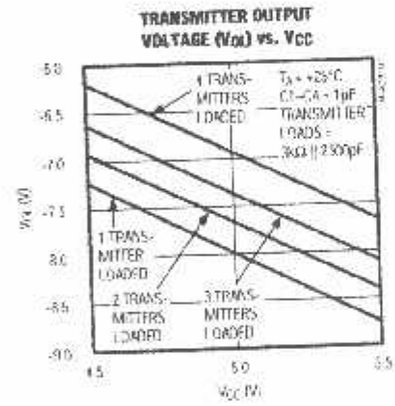
TRANSMITTER OUTPUT VOLTAGE (V_{OH}) vs. LOAD CAPACITANCE AT DIFFERENT DATA RATES



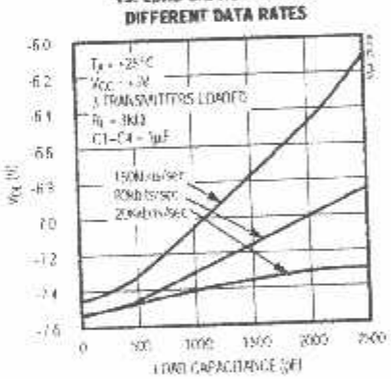
TRANSMITTER SLEW RATE vs. LOAD CAPACITANCE



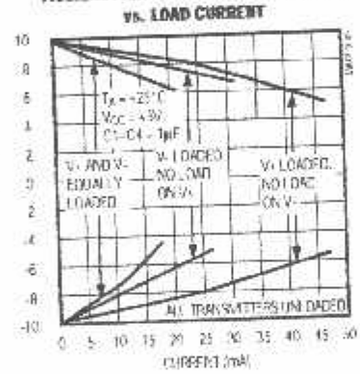
TRANSMITTER OUTPUT VOLTAGE (V_{OL}) vs. V_{CC}



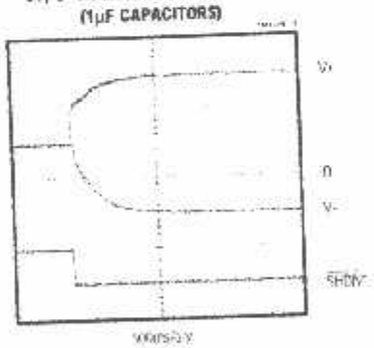
TRANSMITTER OUTPUT VOLTAGE (V_{OL}) vs. LOAD CAPACITANCE AT DIFFERENT DATA RATES



TRANSMITTER OUTPUT VOLTAGE (V+, V-) vs. LOAD CURRENT



V+, V- WHEN EXITING SHUTDOWN (1µF CAPACITORS)



*SHUTDOWN POLARITY IS REVERSED FOR NON-MAX241 PARTS.

+5V-Powered, Multichannel RS-232 Drivers/Receivers

ABSOLUTE MAXIMUM RATINGS—MAX225/MAX244–MAX249

Supply Voltage (V_{CC}) ..... -0.3V to +6V
Input Voltages
T_{IN}, $\overline{ENA}$, ENB, $\overline{ENR}$, ENT, $\overline{ENRA}$, $\overline{ENRB}$, $\overline{ENTA}$, $\overline{ENTB}$ ..... -0.3V to (V_{CC} + 0.3V)
R_{IN} ..... ±25V
T_{OUT} (Note 3) ..... +15V
R_{OUT} ..... -0.3V to (V_{CC} + 0.3V)
Short Circuit (one output at a time)
T_{OUT} to GND ..... Continuous
R_{OUT} to GND ..... Continuous

Continuous Power Dissipation (T_A = +70°C)
28-Pin Wide SO (derate 12.50mW/°C above +70°C) 1W
40-Pin Plastic DIP (derate 11.11mW/°C above +70°C) 611mW
44-Pin PLCC (derate 13.33mW/°C above +70°C) 1.07W
Operating Temperature Ranges
MAX225C_ _, MAX24_C_ _ ..... 0°C to +70°C
MAX225E_ _, MAX24_E_ _ ..... -40°C to +85°C
Storage Temperature Range ..... -65°C to +160°C
Lead Temperature (soldering, 10sec) ..... +300°C

Note 3: Input voltage measured with transmitter output in a high-impedance state, shutdown, or V_{CC} = 0V.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS—MAX225/MAX244–MAX249

(MAX225, V_{CC} = 5.0V ±5%; MAX244–MAX249, V_{CC} = +5.0V ±10%, external capacitors C1–C4 = 1µF; T_A = T_{MIN} to T_{MAX}, unless otherwise noted.)

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
RS-232 TRANSMITTERS						
Input Logic Threshold Low				1.4	0.8	V
Input Logic Threshold High			2	1.4		V
Logic Pull-Up/Input Current	Tables 1a–1d	Normal operation		10	50	µA
		Shutdown		±0.01	±1	
Data Rate	Tables 1a–1d, normal operation			120	64	kbits/sec
Output Voltage Swing	All transmitter outputs loaded with 3kΩ to GND		±5	±7.5		V
Output Leakage Current (shutdown)	Tables 1a–1d	$\overline{ENA}$, ENB, $\overline{ENT}$, $\overline{ENTA}$, $\overline{ENTB}$ = V_{CC}, V_{OUT} = ±15V		±0.01	±25	µA
		V_{CC} = 0V, V_{OUT} = ±15V		±0.01	±25	
Transmitter Output Resistance	V_{CC} = V+ = V- = 0V, V_{OUT} = ±2V (Note 4)		300	10M		Ω
Output Short-Circuit Current	V_{OUT} = 0V		±7	±30		mA
RS-232 RECEIVERS						
RS-232 Input Voltage Operating Range					±25	V
RS-232 Input Threshold Low	V_{CC} = 5V		0.8	1.3		V
RS-232 Input Threshold High	V_{CC} = 5V			1.8	2.4	V
RS-232 Input Hysteresis	V_{CC} = 5V		0.2	0.5	1.0	V
RS-232 Input Resistance			3	5	7	kΩ
TTL/CMOS Output Voltage Low	I_{OUT} = 3.2mA			0.2	0.4	V
TTL/CMOS Output Voltage High	I_{OUT} = -1.0mA		3.5	V_{CC} - 0.2		V
TTL/CMOS Output Short-Circuit Current	Sourcing V_{OUT} = GND		-2	-10		mA
	Shrinking V_{OUT} = V_{CC}		10	30		
TTL/CMOS Output Leakage Current	Normal operation, outputs disabled. Tables 1a–1d, 0V ≤ V_{OUT} ≤ V_{CC}, $\overline{ENR}$_ = V_{CC}			±0.05	±0.10	µA

ELECTRICAL CHARACTERISTICS—MAX225/MAX244–MAX249 (continued)

(MAX225, V_{CC} = 5.0V ±5%; MAX244–MAX249, V_{CC} = +5.0V ±10%, external capacitors C1–C4 = 1µF; T_A = T_{MIN} to T_{MAX}, unless otherwise noted.)

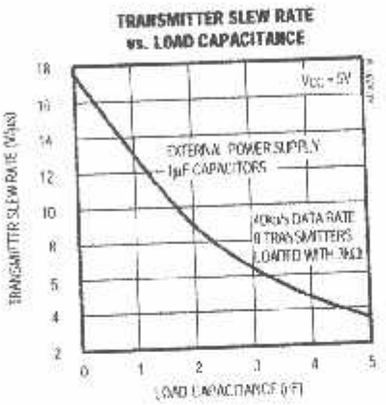
PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
POWER SUPPLY AND CONTROL LOGIC						
Operating Supply Voltage		MAX225	4.75		5.25	V
		MAX244–MAX249	4.5		5.5	
V_{CC} Supply Current (normal operation)	No load	MAX225		10	20	mA
		MAX244–MAX249		11	30	
	3kΩ loads on all outputs	MAX225		40		
		MAX244–MAX249		57		
Shutdown Supply Current	T_A = +25°C			8	25	µA
	T_A = T_{MIN} to T_{MAX}				50	
Control Input	Leakage current				±1	µA
	Threshold low			1.4	0.8	V
	Threshold high		2.4	1.4		
AC CHARACTERISTICS						
Transition Slew Rate	C_L = 50pF to 2500pF, R_L = 3kΩ to 7kΩ, V_{CC} = 5V, T_A = +25°C, measured from +3V to -3V or -3V to +3V		5	10	30	V/µs
Transmitter Propagation Delay TTL to RS-232 (normal operation), Figure 1	t_{PHLT}			1.3	3.5	µs
	t_{PLHT}			1.5	3.5	
Receiver Propagation Delay TTL to RS-232 (normal operation), Figure 2	t_{PHLR}			0.6	1.5	µs
	t_{PLHR}			0.6	1.5	
Receiver Propagation Delay TTL to RS-232 (low-power mode), Figure 2	t_{PHLS}			0.6	10	µs
	t_{PLHS}			3.0	10	
Transmitter + to - Propagation Delay Difference (normal operation)	t_{PHLT} - t_{PLHT}			300		ns
Receiver + to - Propagation Delay Difference (normal operation)	t_{PHLR} - t_{PLHR}			350		ns
Receiver-Output Enable Time, Figure 3	t_{ER}			100	500	ns
Receiver-Output Disable Time, Figure 3	t_{DR}			100	500	ns
Transmitter Enable Time	t_{ET}	MAX240–MAX249 (excludes charge-pump start up)		5		µs
		MAX225/MAX245–MAX249 (includes charge-pump start up)		10		ms
Transmitter Disable Time, Figure 4	t_{DT}			100		ns

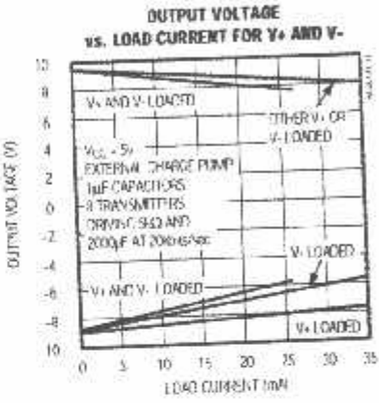
Note 4: The 300Ω minimum specification complies with EIA/TIA-232E, but the actual resistance when in shutdown mode at V_{CC} = 0V is 10MΩ, as is implied by the leakage specification.

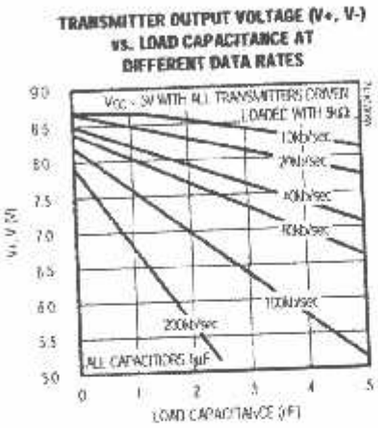
+5V-Powered, Multichannel RS-232 Drivers/Receivers

Typical Operating Characteristics

MAX225/MAX244–MAX249







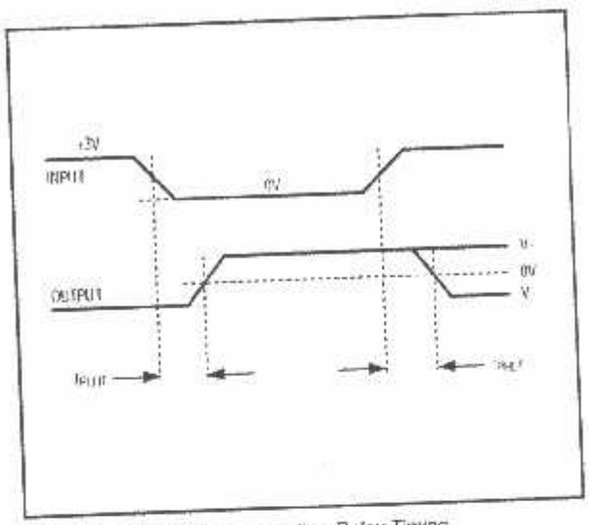


Figure 1. Transmitter Propagation-Delay Timing

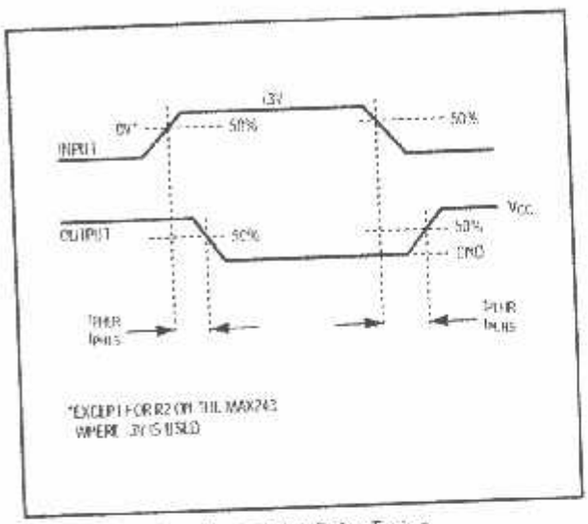


Figure 2. Receiver Propagation-Delay Timing

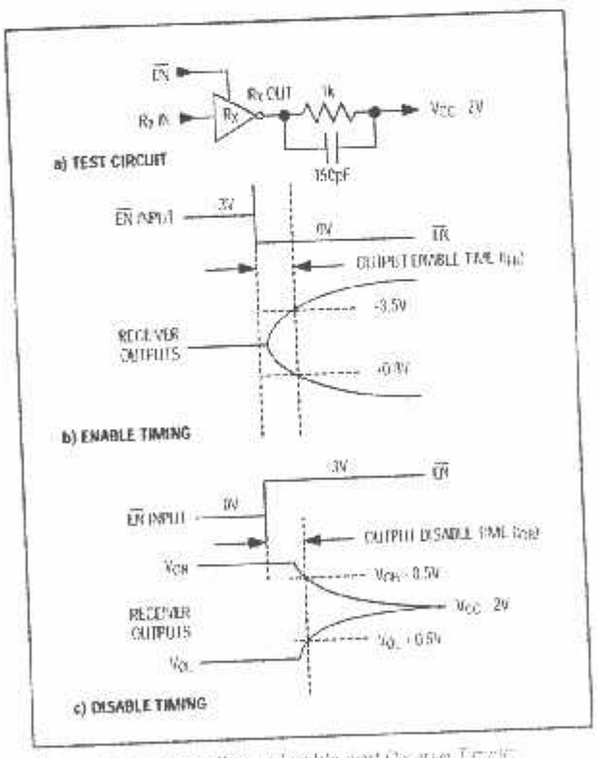


Figure 3. Receiver Output Enable and Disable Timing

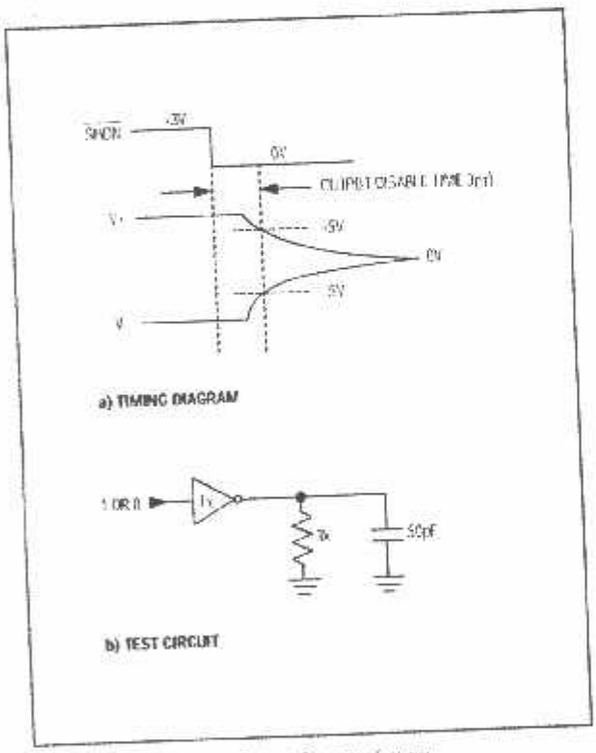


Figure 4. Transmitter Output Enable Timing

Table 1a. MAX245 Control Pin Configurations

$\overline{ENT}$	$\overline{ENR}$	OPERATION STATUS	TRANSMITTERS	RECEIVERS
0	0	Normal Operation	All Active	All Active
0	1	Normal Operation	All Active	All 3-State
1	0	Shutdown	All 3-State	All Low-Power Receive Mode
1	1	Shutdown	All 3-State	All 3-State

Table 1b. MAX245 Control Pin Configurations

$\overline{ENT}$	$\overline{ENR}$	OPERATION STATUS	TRANSMITTERS		RECEIVERS	
			TA1–TA4	TB1–TB4	RA1–RA5	RB1–RB5
0	0	Normal Operation	All Active	All Active	All Active	All Active
0	1	Normal Operation	All Active	All Active	RA1–RA4 3-State RA5 Active	RB1–RB4 3-State RB5 Active
1	0	Shutdown	All 3-State	All 3-State	All Low-Power Receive Mode	All Low-Power Receive Mode
1	1	Shutdown	All 3-State	All 3-State	RA1–RA4 3-State RA5 Low-Power Receive Mode	RB1–RB4 3-State RB5 Low-Power Receive Mode

Table 1c. MAX246 Control Pin Configurations

$\overline{ENA}$	$\overline{ENB}$	OPERATION STATUS	TRANSMITTERS		RECEIVERS	
			TA1–TA4	TB1–TB4	RA1–RA5	RB1–RB5
0	0	Normal Operation	All Active	All Active	All Active	All Active
0	1	Normal Operation	All Active	All 3-State	All Active	RB1–RB4 3-State RB5 Active
1	0	Shutdown	All 3-State	All Active	RA1–RA4 3-State RA5 Active	All Active
1	1	Shutdown	All 3-State	All 3-State	RA1–RA4 3-State RA5 Low-Power Receive Mode	RB1–RB4 3-State RB5 Low-Power Receive Mode

Table 1d. MAX247/MAX248/MAX249 Control Pin Configurations

$\overline{ENTA}$	$\overline{ENTB}$	$\overline{ENRA}$	$\overline{ENRB}$	OPERATION STATUS		TRANSMITTERS		RECEIVERS	
					MAX247	TA1–TA4	TB1–TB4	RA1–RA4	RB1–RB5
					MAX248	TA1–TA4	TB1–TB4	RA1–RA4	RB1–RB4
					MAX249	TA1–TA3	TB1–TB3	RA1–RA5	RB1–RB5
0	0	0	0	Normal Operation		All Active	All Active	All Active	All Active
0	0	0	1	Normal Operation		All Active	All Active	All Active	All 3-State, except RB5 stays active on MAX247
0	0	1	0	Normal Operation		All Active	All Active	All 3-State	All Active
0	0	1	1	Normal Operation		All Active	All Active	All 3-State	All 3-State, except RB5 stays active on MAX247
0	1	0	0	Normal Operation		All Active	All 3-State	All Active	All Active
0	1	0	1	Normal Operation		All Active	All 3-State	All Active	All 3-State, except RB5 stays active on MAX247
0	1	1	0	Normal Operation		All Active	All 3-State	All 3-State	All Active
0	1	1	1	Normal Operation		All Active	All 3-State	All 3-State	All 3-State, except B5 stays active on MAX247
1	0	0	0	Normal Operation		All 3-State	All Active	All Active	All Active
1	0	0	1	Normal Operation		All 3-State	All Active	All Active	All 3-State, except RB5 stays active on MAX247
1	0	1	0	Normal Operation		All 3-State	All Active	All 3-State	All Active
1	0	1	1	Normal Operation		All 3-State	All Active	All 3-State	All 3-State, except RB5 stays active on MAX247
1	1	0	0	Shutdown		All 3-State	All 3-State	Low-Power Receive Mode	Low-Power Receive Mode
1	1	0	1	Shutdown		All 3-State	All 3-State	Low-Power Receive Mode	All 3-State, except RB5 stays active on MAX247
1	1	1	0	Shutdown		All 3-State	All 3-State	All 3-State	Low-Power Receive Mode
1	1	1	1	Shutdown		All 3-State	All 3-State	All 3-State	All 3-State, except RB5 stays active on MAX247

+5V-Powered, Multichannel RS-232 Drivers/Receivers

Detailed Description

The MAX220–MAX249 contain four sections: dual charge-pump DC-DC voltage converters, RS-232 drivers, RS-232 receivers, and receiver and transmitter enable control inputs.

Dual Charge-Pump Voltage Converter

The MAX220–MAX249 have two internal charge-pumps that convert +5V to ±10V (unloaded) for RS-232 driver operation. The first converter uses capacitor C1 to double the +5V input to +10V on C3 at the V+ output. The second converter uses capacitor C2 to invert +10V to -10V on C4 at the V- output.

A small amount of power may be drawn from the +10V (V+) and -10V (V-) outputs to power external circuitry (see the *Typical Operating Characteristics* section) except on the MAX225 and MAX245–MAX247, where these pins are not available. V+ and V- are not regulated, so the output voltage drops with increasing load current. Do not load V+ and V- to a point that violates the minimum ±5V EIA/TIA-232E driver output voltage when sourcing current from V+ and V- to external circuitry.

When using the shutdown feature in the MAX222, MAX225, MAX230, MAX235, MAX236, MAX240, MAX241, and MAX245–MAX249, avoid using V+ and V- to power external circuitry. When these parts are shutdown, V- falls to 0V, and V+ falls to +5V. For applications where a +10V external supply is applied to the V+ pin (instead of using the internal charge pump to generate +10V), the C1 capacitor must not be installed and the $\overline{SHDN}$ pin must be tied to V_{CC}. This is because V+ is internally connected to V_{CC} in shutdown mode.

RS-232 Drivers

The typical driver output voltage swing is ±8V when loaded with a nominal 5kΩ RS-232 receiver and V_{CC} = +5V. Output swing is guaranteed to meet the EIA/TIA-232E and V.28 specification, which calls for ±5V minimum driver output levels under worst-case conditions. These include a minimum 3kΩ load, V_{CC} = +4.5V, and maximum operating temperature. Unloaded driver output voltage ranges from (V+ -1.3V) to (V- +0.5V).

Input thresholds are both TTL and CMOS compatible. The inputs of unused drivers can be left unconnected since 400kΩ input pull-up resistors to V_{CC} are built in. The pull-up resistors force the outputs of unused drivers low because all drivers invert. The internal input pull-up resistors typically source 12µA, except in shutdown mode where the pull-ups are disabled. Driver outputs turn off and enter a high-impedance state—where leakage current is typically microamperes (maximum 25µA)—when in shutdown mode, in three-state mode, or when device power is removed. Outputs can be driven to ±15V. The power-supply current typically drops to 8µA in shutdown mode.

The MAX239 has a receiver three-state control line, and the MAX223, MAX225, MAX235, MAX236, MAX240, and MAX241 have both a receiver three-state control line and a low-power shutdown control. Table 2 shows the effects of the shutdown control and receiver three-state control on the receiver outputs.

The receiver TTL/CMOS outputs are in a high-impedance, three-state mode whenever the three-state enable line is high (for the MAX225/MAX235/MAX236/MAX239–MAX241), and are also high-impedance whenever the shutdown control line is high.

When in low-power shutdown mode, the driver outputs are turned off and their leakage current is less than 1µA with the driver output pulled to ground. The driver output leakage remains less than 1µA, even if the transmitter output is backdriven between 0V and (V_{CC} + 6V). Below -0.5V, the transmitter is diode clamped to ground with 1kΩ series impedance. The transmitter is also zener clamped to approximately V_{CC} + 6V, with a series impedance of 1kΩ.

The driver output slew rate is limited to less than 30V/µs as required by the EIA/TIA-232E and V.28 specifications. Typical slew rates are 24V/µs unloaded and 10V/µs loaded with 3Ω and 2500pF.

RS-232 Receivers

EIA/TIA-232E and V.28 specifications define a voltage level greater than 3V as a logic 0, so all receivers invert. Input thresholds are set at 0.8V and 2.4V, so receivers respond to TTL level inputs as well as EIA/TIA-232E and V.28 levels.

The receiver inputs withstand an input overvoltage up to ±25V and provide input terminating resistors with nominal 5kΩ values. The receivers implement Type 1 interpretation of the fault conditions of V.28 and EIA/TIA 232E.

Table 2. Three-State Control of Receivers

PART	SHDN	SHDN	EN	EN(R)	RECEIVERS
MAX223	—	Low	X	—	High Impedance
		High	Low		Active
		High	High		High Impedance
MAX225	—	—	—	Low	High Impedance
				High	Active
MAX235	Low	—	—	Low	High Impedance
MAX236	High			High	Active
MAX240	High			X	High Impedance

The receiver input hysteresis is typically 0.5V with a guaranteed minimum of 0.2V. This produces clean output transitions with slow-moving input signals, even with moderate amounts of noise and ringing. The receiver propagation delay is typically 600ns and is independent of input swing direction.

Low-Power Receive Mode

The low-power receive-mode feature of the MAX223, MAX242, and MAX245–MAX249 puts the IC into shutdown mode but still allows it to receive information. This is important for applications where systems are periodically awakened to look for activity. Using low-power receive mode, the system can still receive a signal that will activate it on command and prepare it for communication at faster data rates. This operation conserves system power.

Negative Threshold—MAX243

The MAX243 is pin compatible with the MAX232A, differing only in that RS-232 cable fault protection is removed on one of the two receiver inputs. This means that control lines such as CTS and RTS can either be driven or left floating without interrupting communication. Different cables are not needed to interface with different pieces of equipment.

The input threshold of the receiver without cable fault protection is -0.8V rather than +1.4V. Its output goes positive only if the input is connected to a control line that is actively driven negative. If not driven, it defaults to the 0 or "OK to send" state. Normally, the MAX243's other receiver (+1.4V threshold) is used for the data line (TD or RD), while the negative threshold receiver is connected to the control line (DTR, DTS, CTS, RTS, etc.).

Other members of the RS-232 family implement the optional cable fault protection as specified by EIA/TIA-232E specifications. This means a receiver output goes high whenever its input is driven negative, left floating, or shorted to ground. The high output tells the serial communications IC to stop sending data. To avoid this, the control lines must either be driven or connected with jumpers to an appropriate positive voltage level.

Shutdown—MAX222–MAX242

On the MAX222, MAX235, MAX236, MAX240, and MAX241, all receivers are disabled during shutdown. On the MAX223 and MAX242, two receivers continue to operate in a reduced power mode when the chip is in shutdown. Under these conditions, the propagation delay increases to about 2.5µs for a high-to-low input transition. When in shutdown, the receiver acts as a CMOS inverter with no hysteresis. The MAX223 and MAX242 also have a receiver output enable input ($\overline{EN}$ for the MAX242 and EN for the MAX223) that allows receiver output control independent of $\overline{SHDN}$ (SHDN for MAX241). With all other devices, $\overline{SHDN}$ (SHDN for MAX241) also disables the receiver outputs.

The MAX225 provides five transmitters and five receivers, while the MAX245 provides ten receivers and eight transmitters. Both devices have separate receiver and transmitter-enable controls. The charge pumps turn off and the devices shut down when a logic high is applied to the ENT input. In this state, the supply current drops to less than 25µA and the receivers continue to operate in a low-power receive mode. Driver outputs enter a high-impedance state (three-state mode). On the MAX225, all five receivers are controlled by the $\overline{ENR}$ input. On the MAX245, eight of the receiver outputs are controlled by the $\overline{ENR}$ input, while the remaining two receivers (RA5 and RB5) are always active. RA1–RA4 and RB1–RB4 are put in a three-state mode when $\overline{ENR}$ is a logic high.

Receiver and Transmitter Enable Control Inputs

The MAX225 and MAX245–MAX249 feature transmitter and receiver enable controls.

The receivers have three modes of operation: full-speed receive (normal active), three-state (disabled), and low-power receive (enabled receivers continue to function at lower data rates). The receiver enable inputs control the full-speed receive and three-state modes. The transmitters have two modes of operation: full-speed transmit (normal active) and three-state (disabled). The transmitter enable inputs also control the shutdown mode. The device enters shutdown mode when all transmitters are disabled. Enabled receivers function in the low-power receive mode when in shutdown.

Tables 1a–1d define the control states. The MAX244 has no control pins and is not included in these tables.

The MAX246 has ten receivers and eight drivers with two control pins, each controlling one side of the device. A logic high at the A-side control input ($\overline{ENA}$) causes the four A-side receivers and drivers to go into a three-state mode. Similarly, the B-side control input ($\overline{ENB}$) causes the four B-side drivers and receivers to go into a three-state mode. As in the MAX245, one A-side and one B-side receiver (RA5 and RB5) remain active at all times. The entire device is put into shutdown mode when both the A and B sides are disabled ($\overline{ENA}$ = $\overline{ENB}$ = +5V).

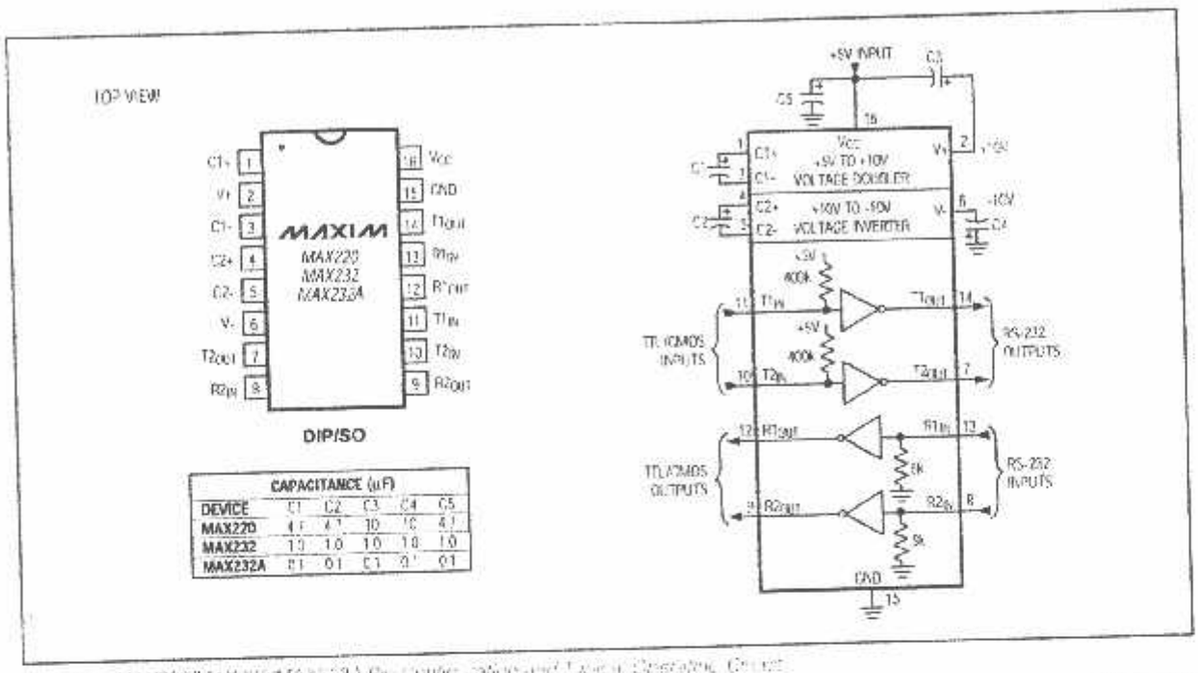
The MAX247 provides nine receivers and eight drivers with four control pins. The $\overline{ENRA}$ and $\overline{ENRB}$ receiver enable inputs each control four receiver outputs. The $\overline{ENTA}$ and $\overline{ENTB}$ transmitter enable inputs each control four drivers. The ninth receiver (RB5) is always active. The device enters shutdown mode with a logic high on both $\overline{ENTA}$ and $\overline{ENTB}$.

The MAX248 provides eight receivers and eight drivers with four control pins. The $\overline{ENRA}$ and $\overline{ENRB}$ receiver enable inputs each control four receiver outputs. The $\overline{ENTA}$ and $\overline{ENTB}$ transmitter enable inputs control four drivers each. This part does not have an always-active receiver. The device enters shutdown mode and transmitters go into a three-state mode with a logic high on both $\overline{ENTA}$ and $\overline{ENTB}$.

The MAX249 provides ten receivers and six drivers with four control pins. The $\overline{ENRA}$ and $\overline{ENRB}$ receiver enable inputs each control five receiver outputs. The $\overline{ENTA}$ and $\overline{ENTB}$ transmitter enable inputs control three drivers each. There is no always-active receiver. The device enters shutdown mode and transmitters go into a three-state mode with a logic high on both $\overline{ENTA}$ and $\overline{ENTB}$. In shutdown mode, active receivers operate in a low-power receive mode at data rates up to 20kbits/sec.

Applications Information

Figures 5 through 25 show pin configurations and typical operating circuits. In applications that are sensitive to power-supply noise, VCC should be decoupled to ground with a capacitor of the same value as C1 and C2 connected as close as possible to the device.



CAPACITANCE (µF)					
DEVICE	C1	C2	C3	C4	C5
MAX220	4.7	4.7	10	10	4.7
MAX232	1.0	1.0	1.0	1.0	1.0
MAX232A	0.1	0.1	0.1	0.1	0.1

Figure 5. MAX220/MAX232/MAX232A Pin Configuration and Typical Operating Circuit

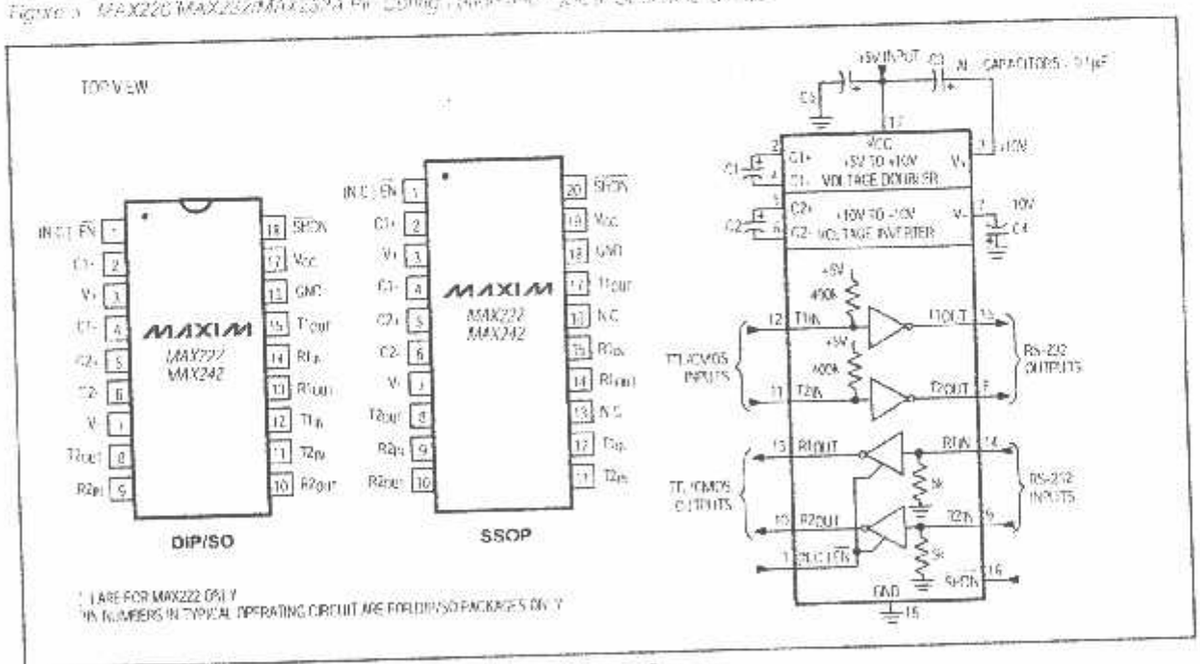


Figure 6. MAX222/MAX242 Pin Configurations and Typical Operating Circuit

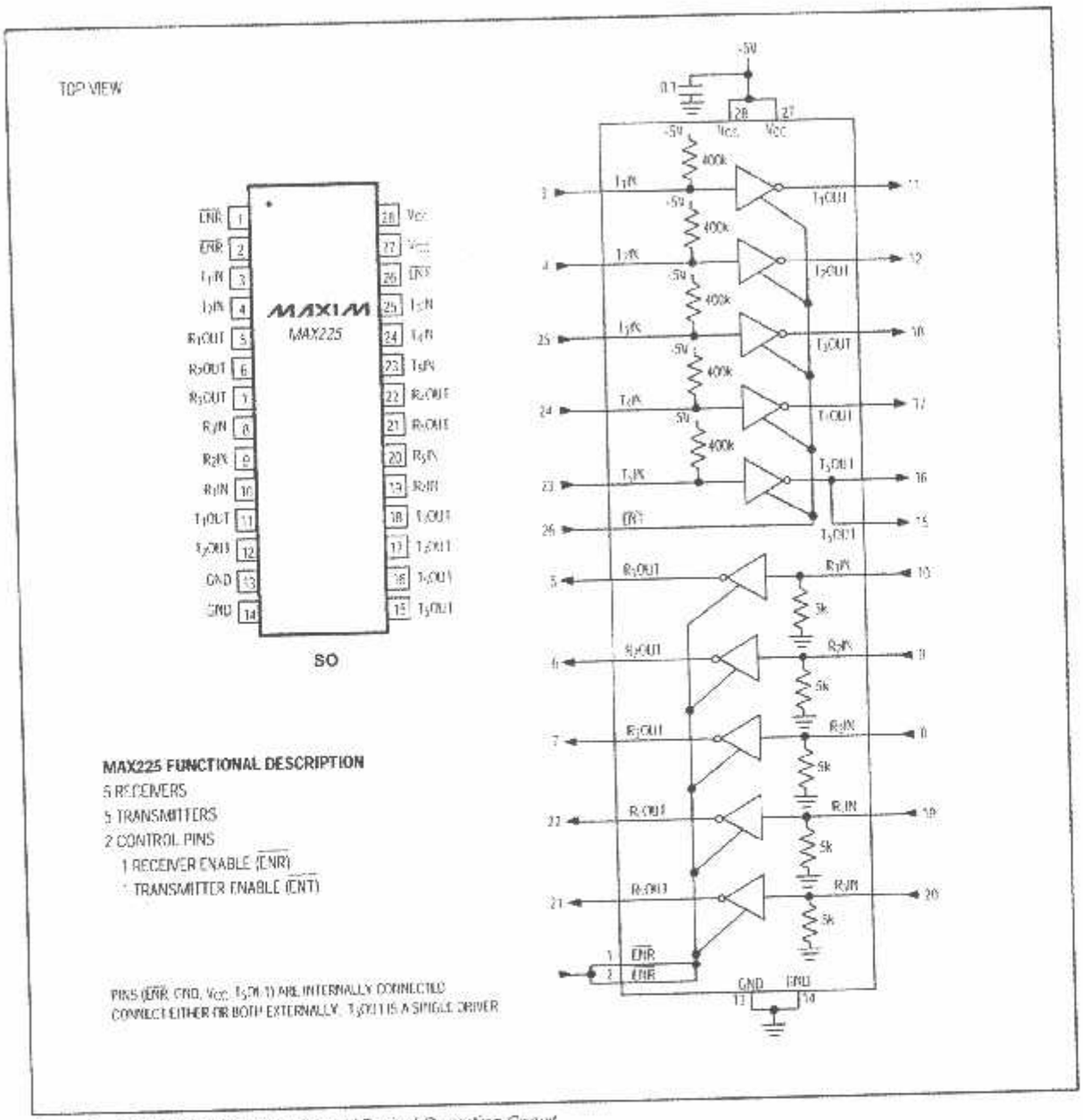


Figure 7. MAX225 Pin Configuration and Typical Operating Circuit

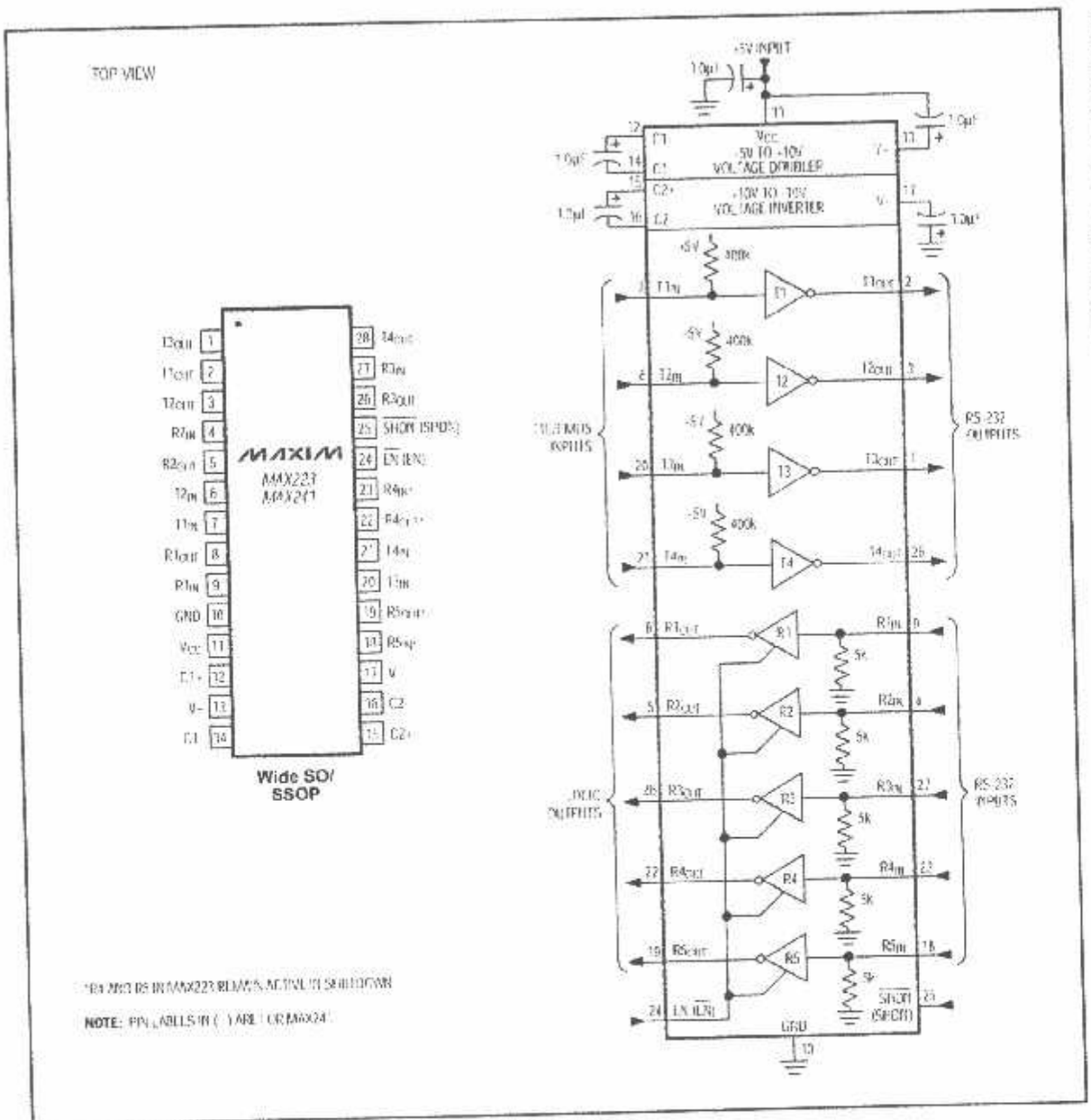


Figure 8. MAX223/MAX241 Pin Configuration and Typical Operating Circuit

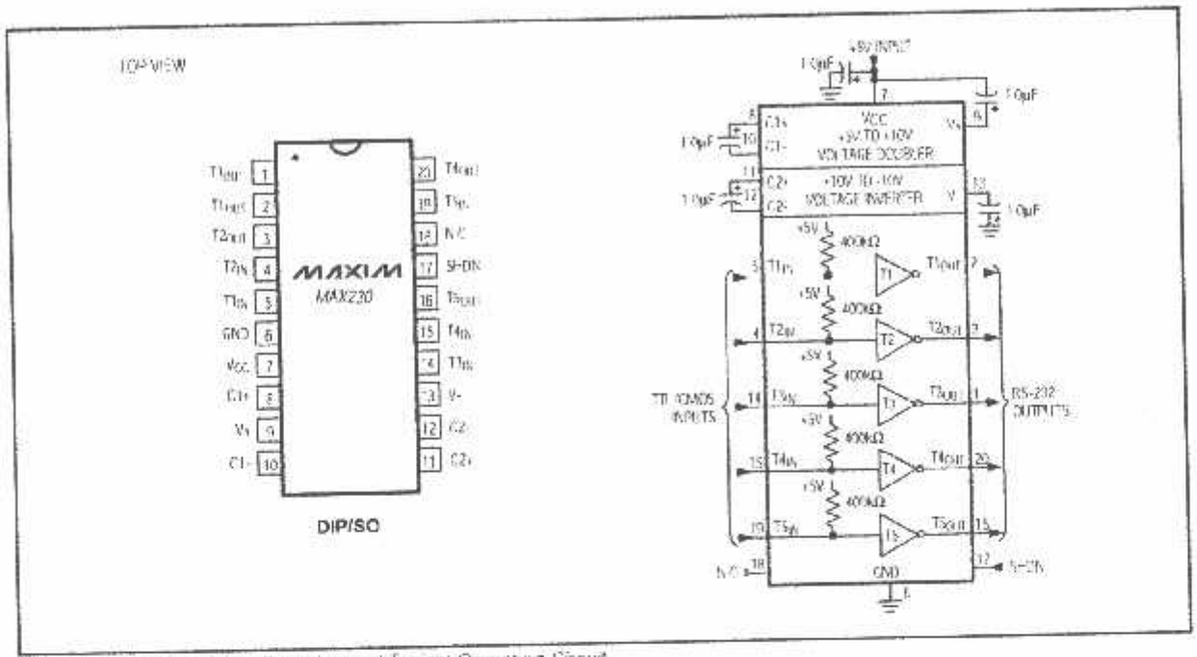


Figure 9. MAX230 Pin Configuration and Typical Operating Circuit

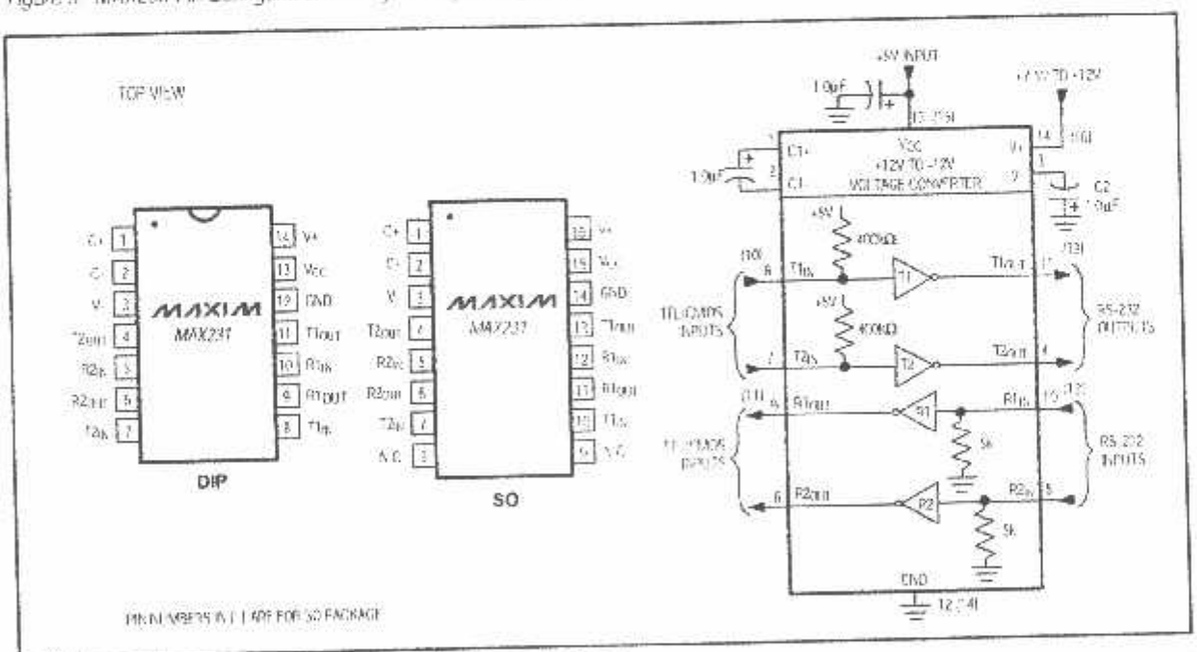


Figure 10. MAX231 Pin Configurations and Typical Operating Circuit

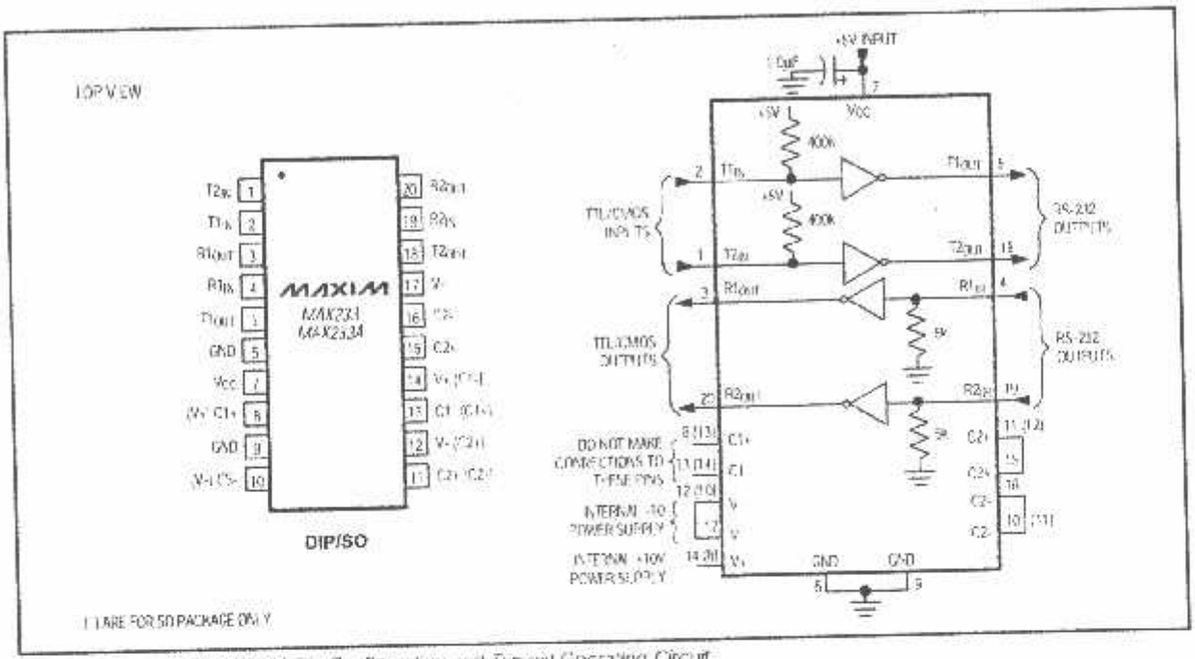


Figure 11. MAX233/MAX233A Pin Configuration and Typical Operating Circuit

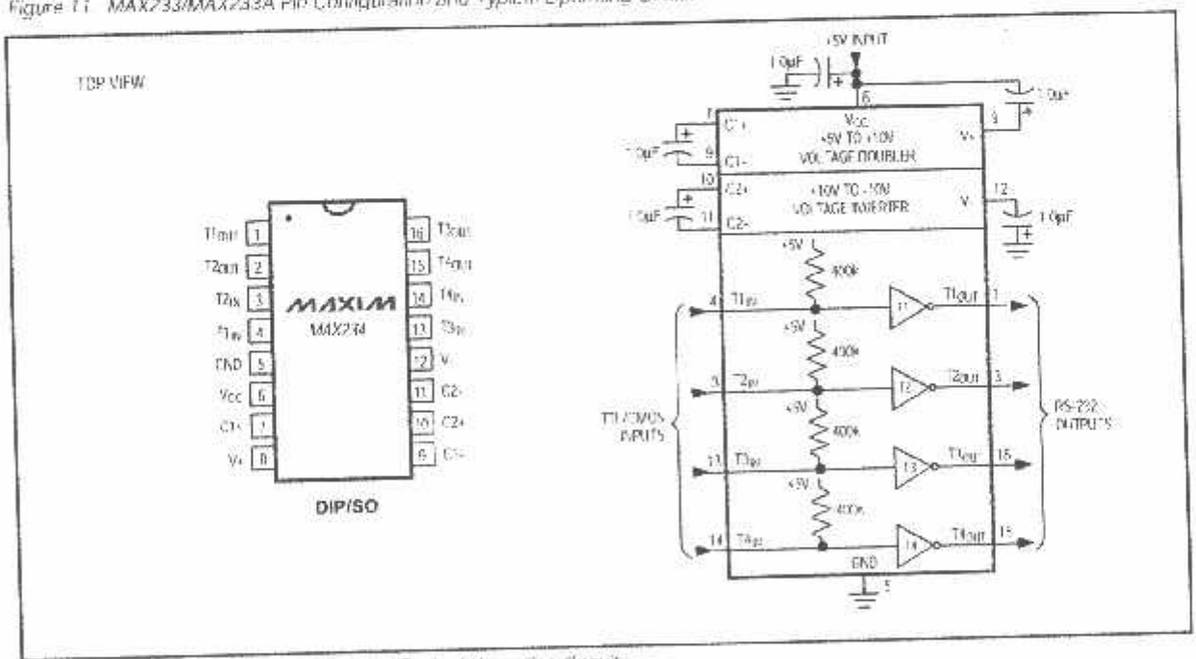


Figure 12. MAX234 Pin Configuration and Typical Operating Circuit

+5V-Powered, Multichannel RS-232 Drivers/Receivers

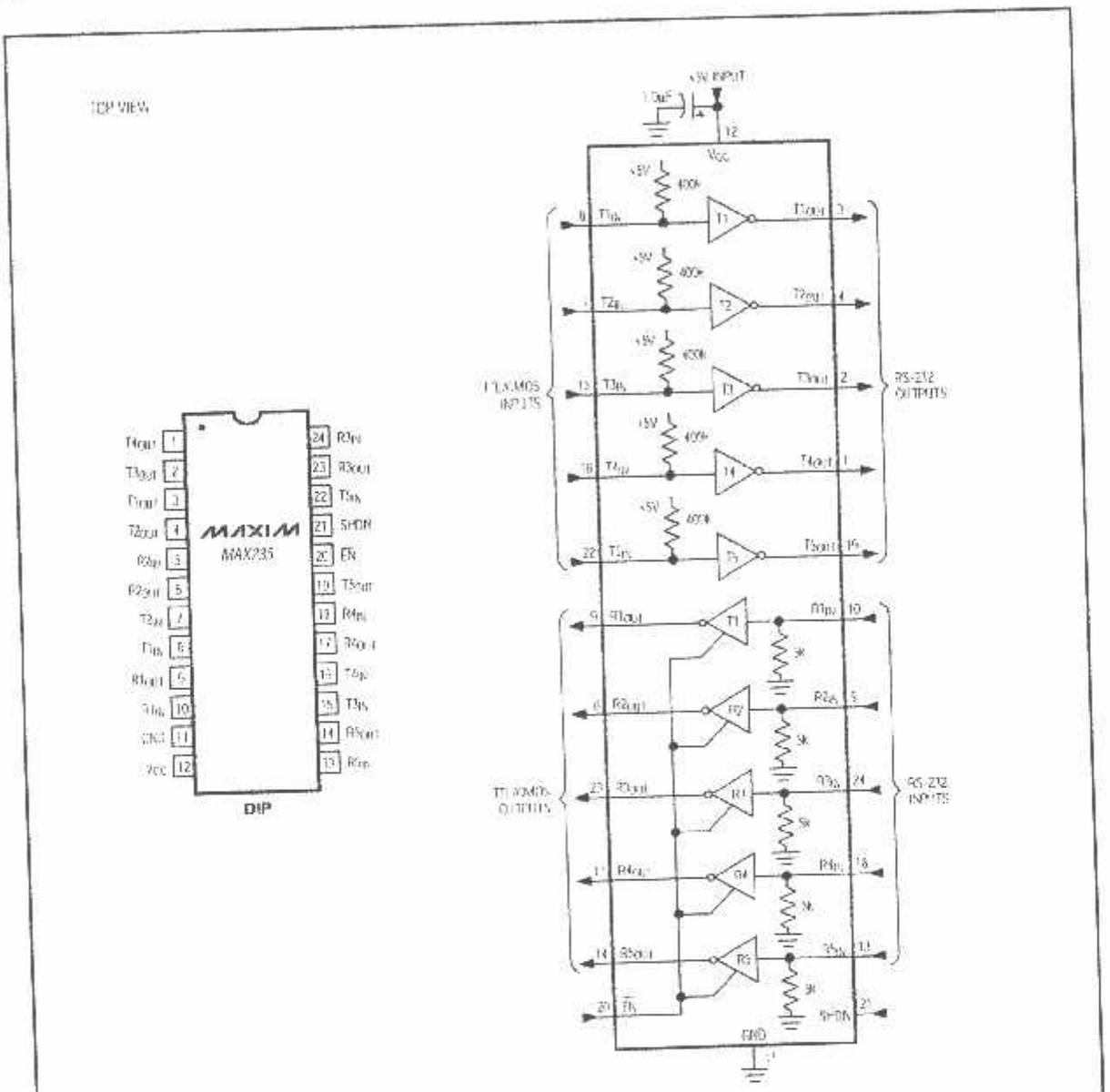


Figure 13. MAX235 Pin Configuration and Typical Operating Circuit

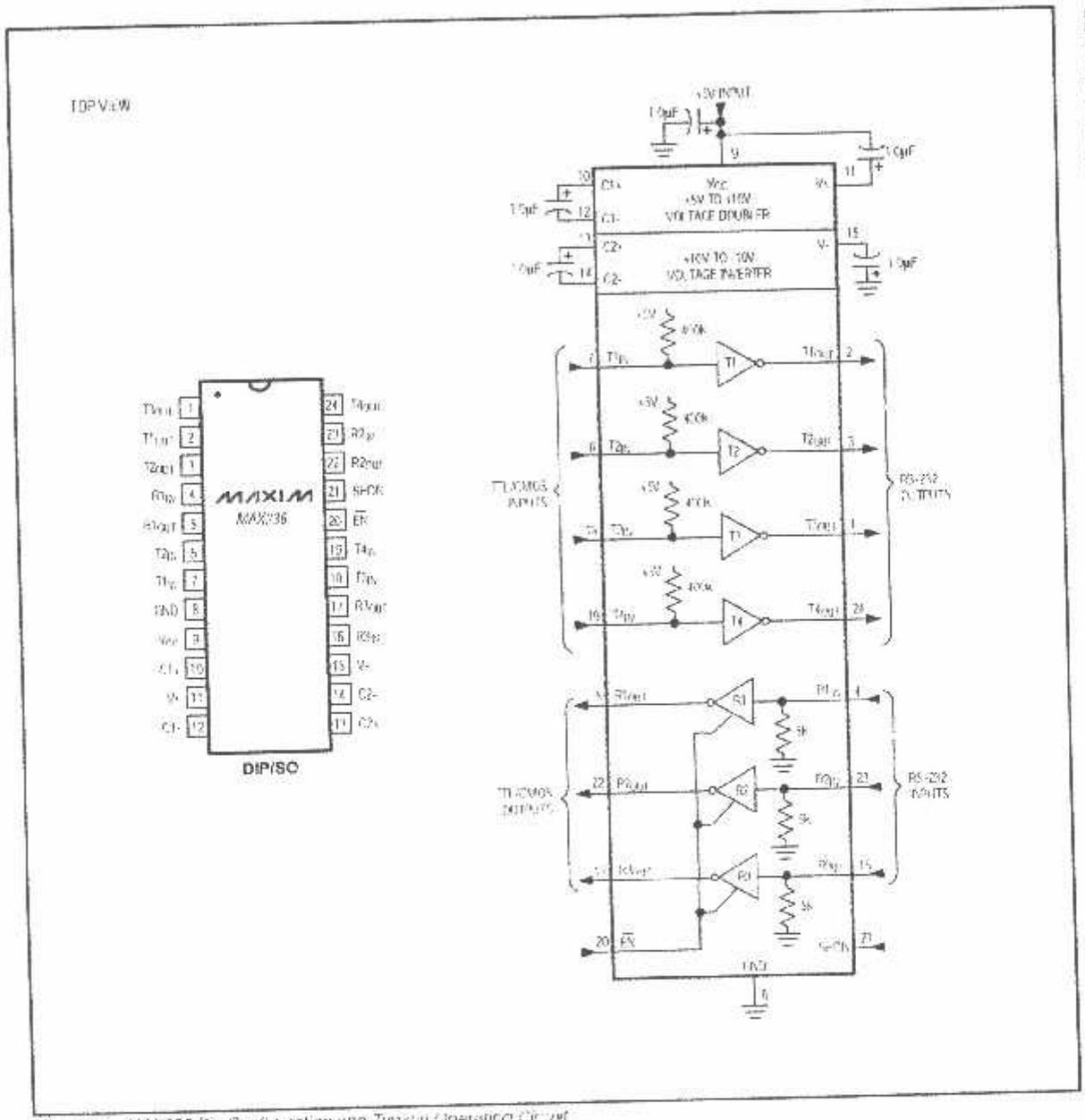


Figure 14. MAX236 Pin Configuration and Typical Operating Circuit

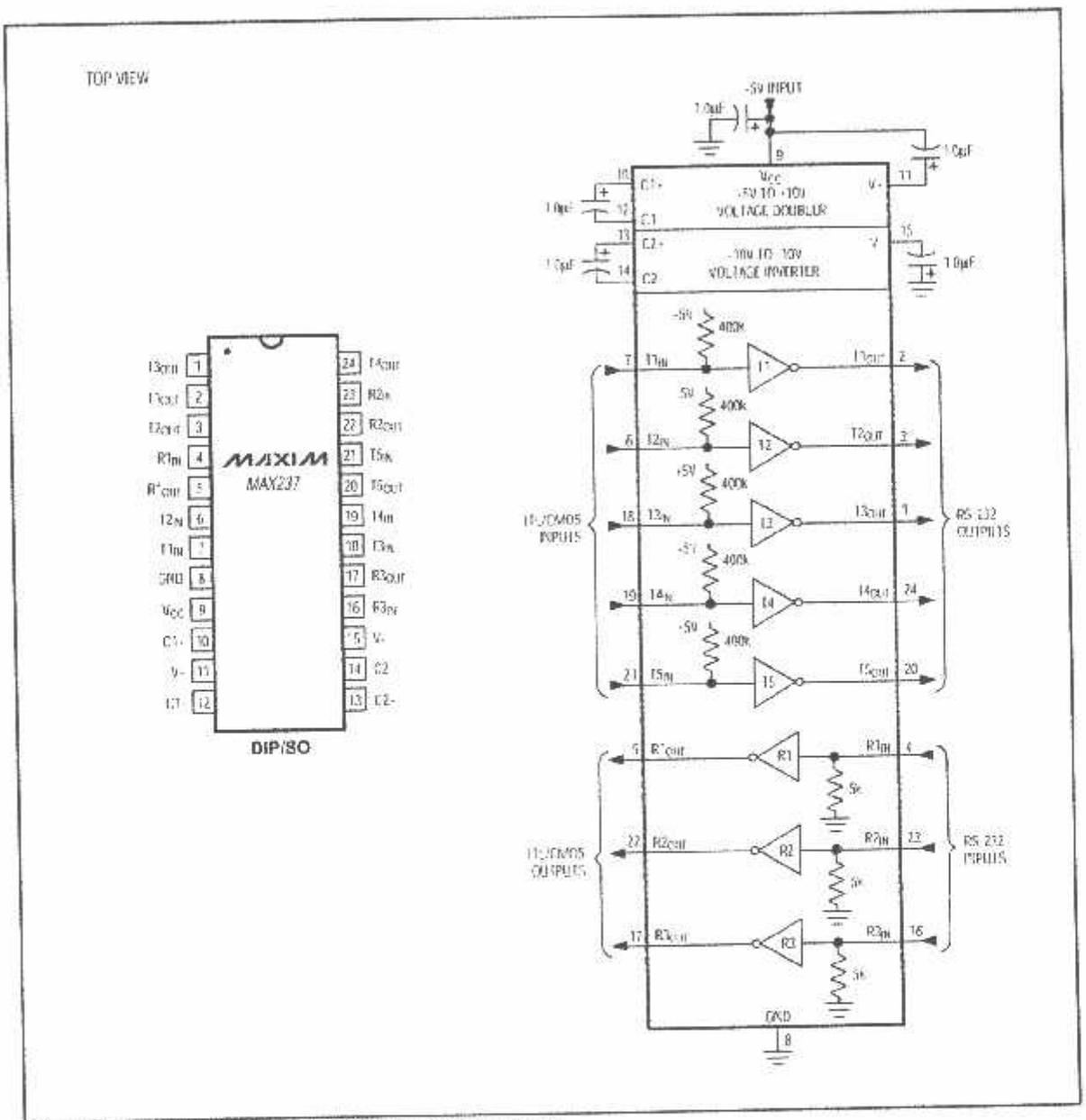


Figure 15. MAX237 Pin Configuration and Typical Operating Circuit

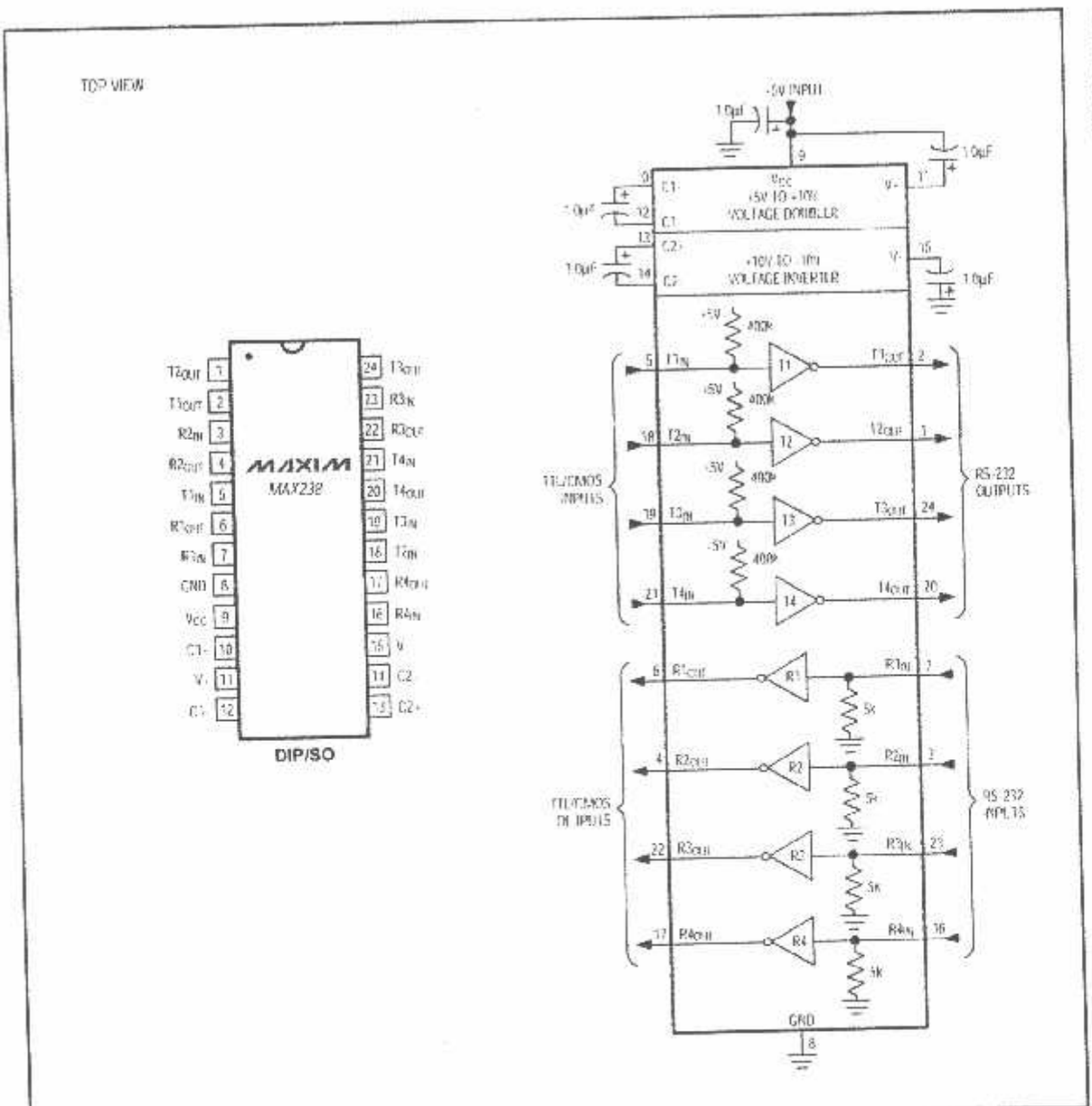


Figure 16. MAX238 Pin Configuration and Typical Operating Circuit

+5V-Powered, Multichannel RS-232 Drivers/Receivers

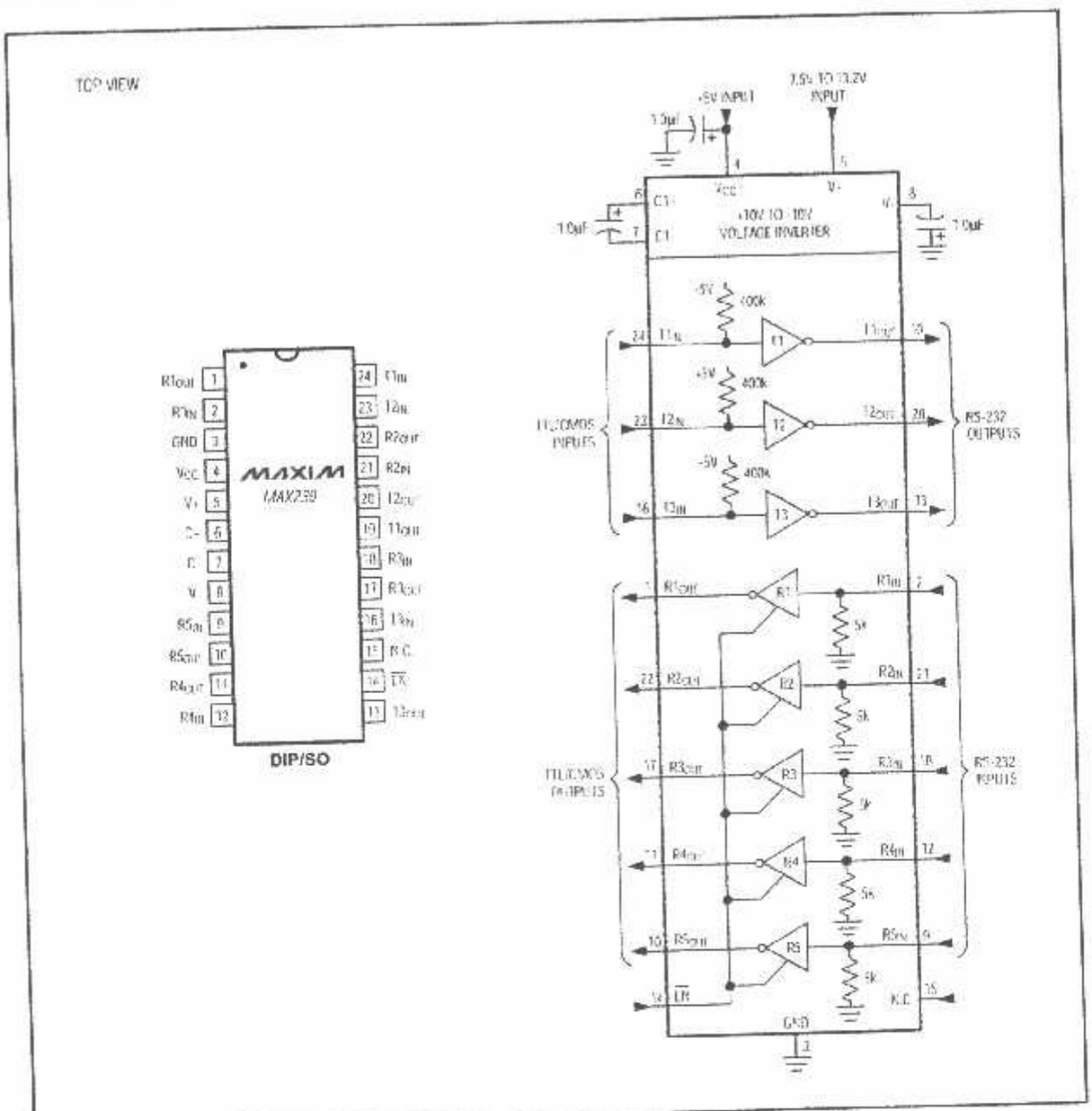


Figure 17. MAX239 Pin Configuration and Typical Operating Circuit

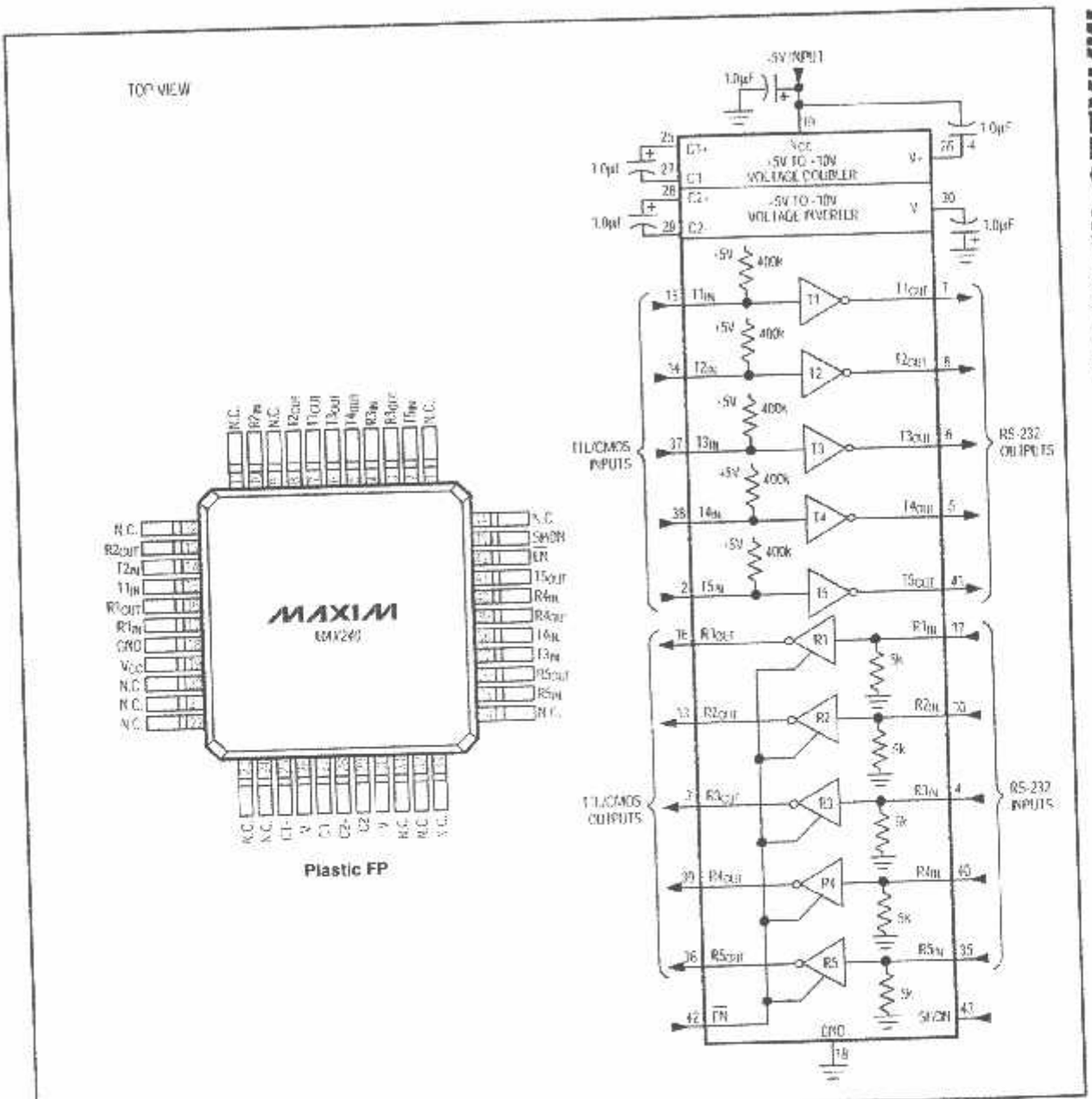
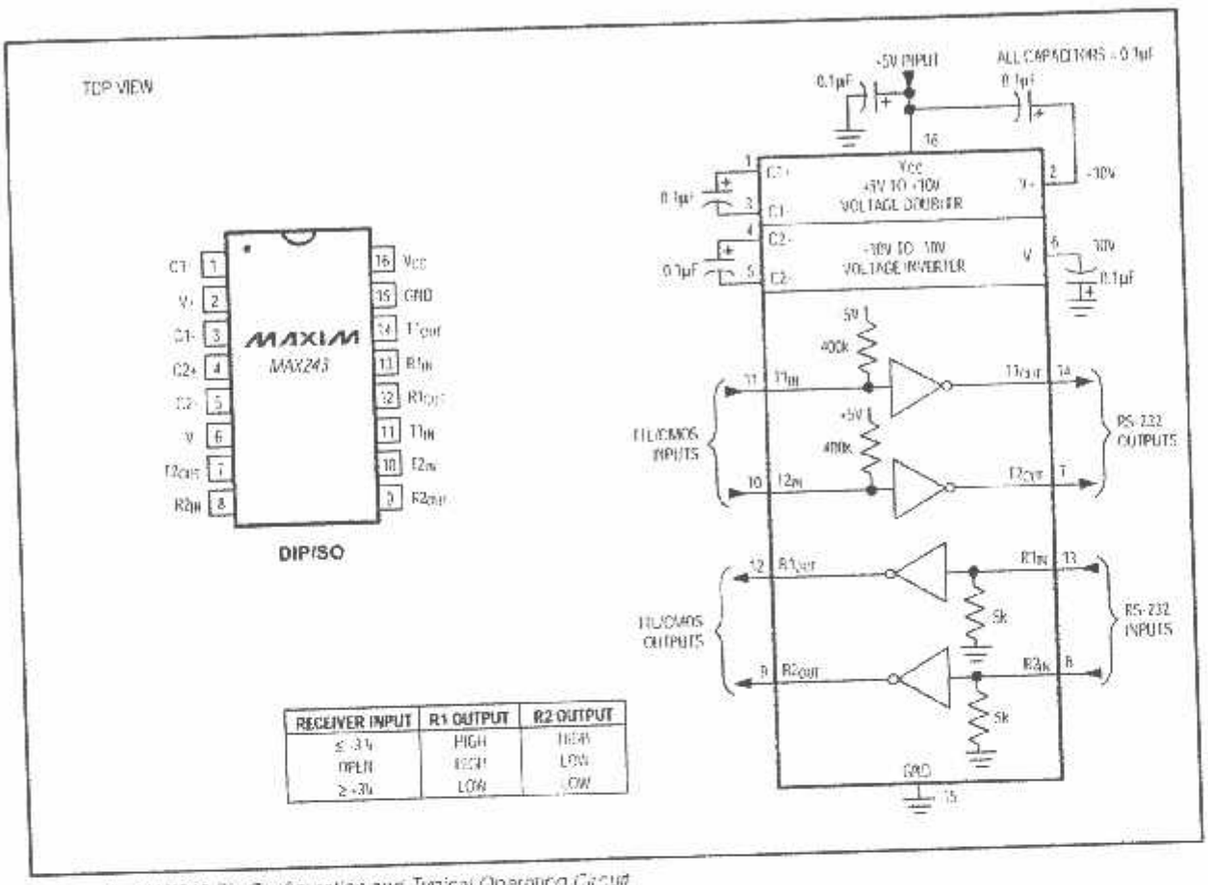


Figure 18. MAX240 Pin Configuration and Typical Operating Circuit

+5V-Powered, Multichannel RS-232 Drivers/Receivers



RECEIVER INPUT	R1 OUTPUT	R2 OUTPUT
≤ -3V	HIGH	HIGH
OPEN	HIGH	LOW
≥ +3V	LOW	LOW

Figure 19. MAX243 Pin Configuration and Typical Operating Circuit

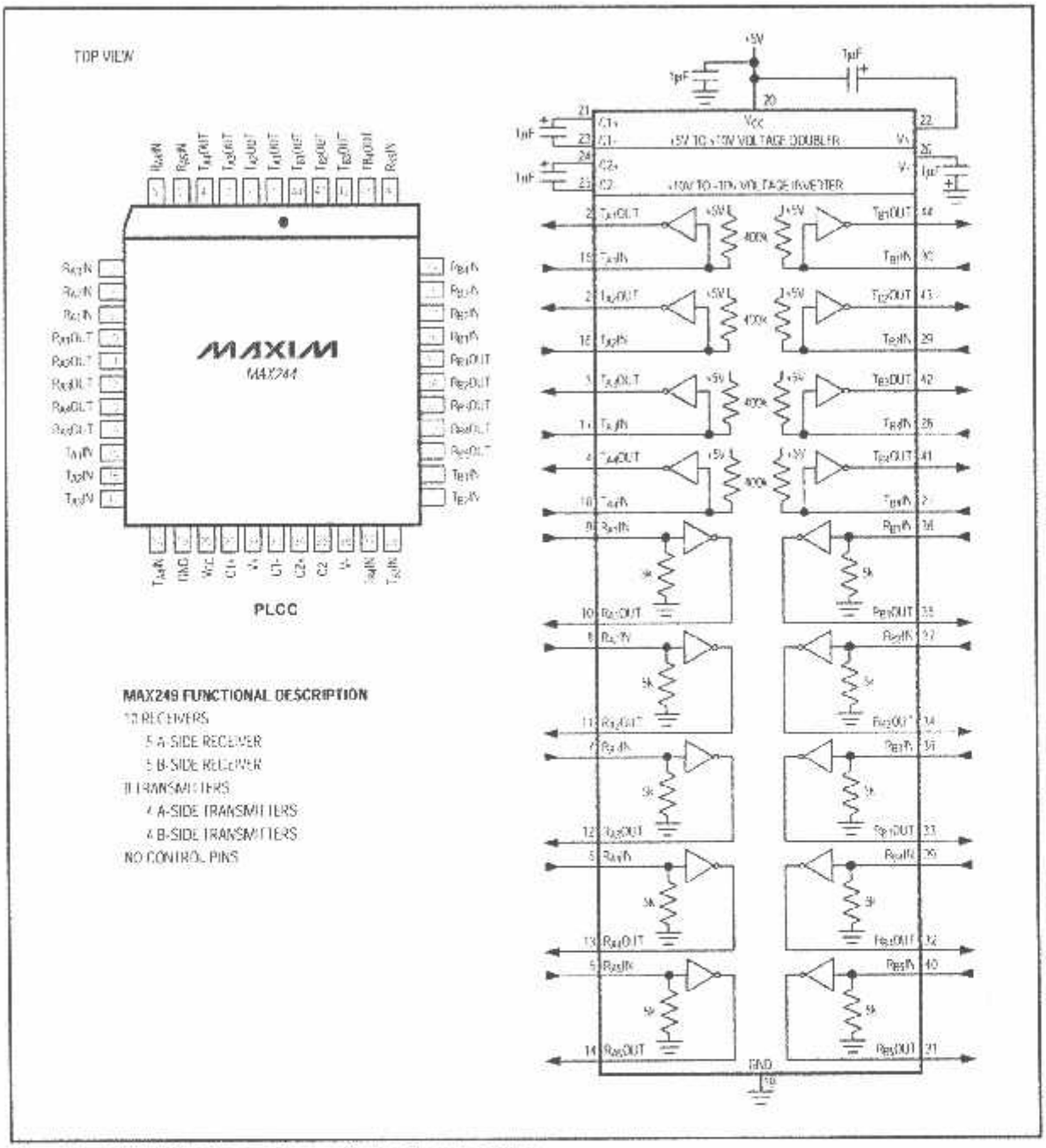


Figure 20. MAX244 Pin Configuration and Typical Operating Circuit

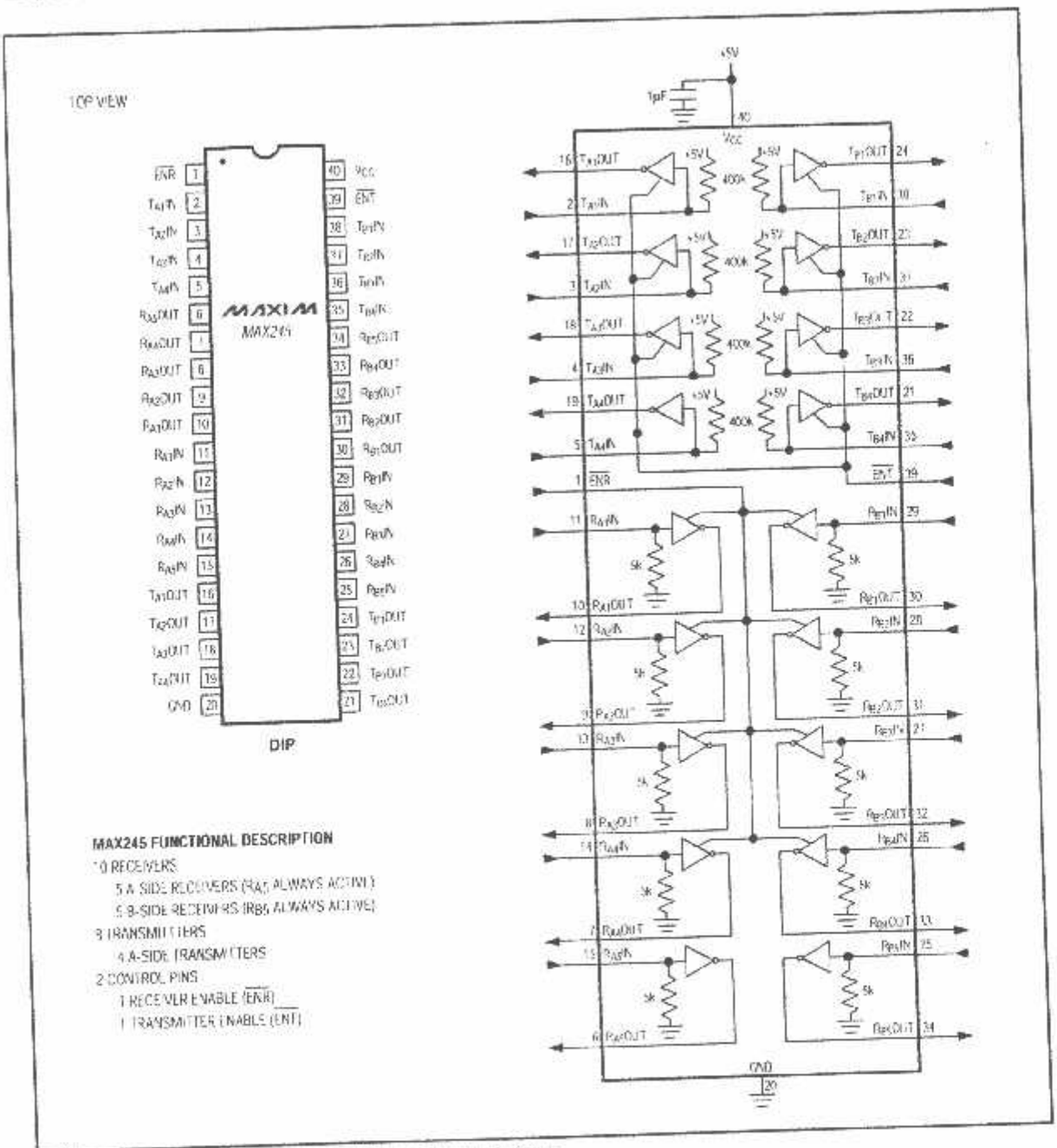
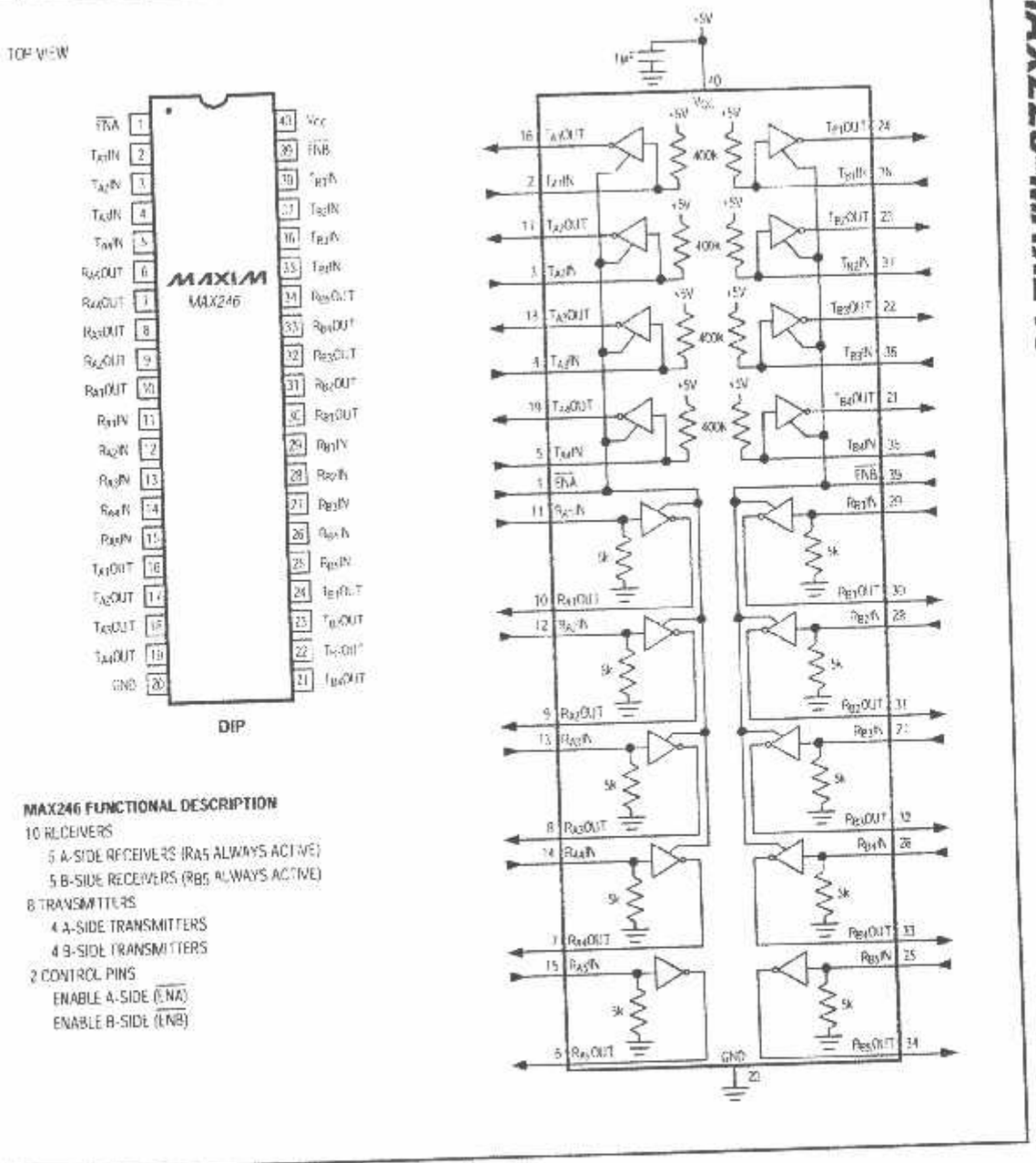


Figure 21. MAX245 Pin Configuration and Typical Operating Circuit



MAX246 FUNCTIONAL DESCRIPTION

10 RECEIVERS
- 5 A-SIDE RECEIVERS (RA5 ALWAYS ACTIVE)
- 5 B-SIDE RECEIVERS (RB5 ALWAYS ACTIVE)

8 TRANSMITTERS
- 4 A-SIDE TRANSMITTERS
- 4 B-SIDE TRANSMITTERS

2 CONTROL PINS
- ENABLE A-SIDE ($\overline{ENA}$)
- ENABLE B-SIDE ($\overline{ENB}$)

Figure 22. MAX246 Pin Configuration and Typical Operating Circuit

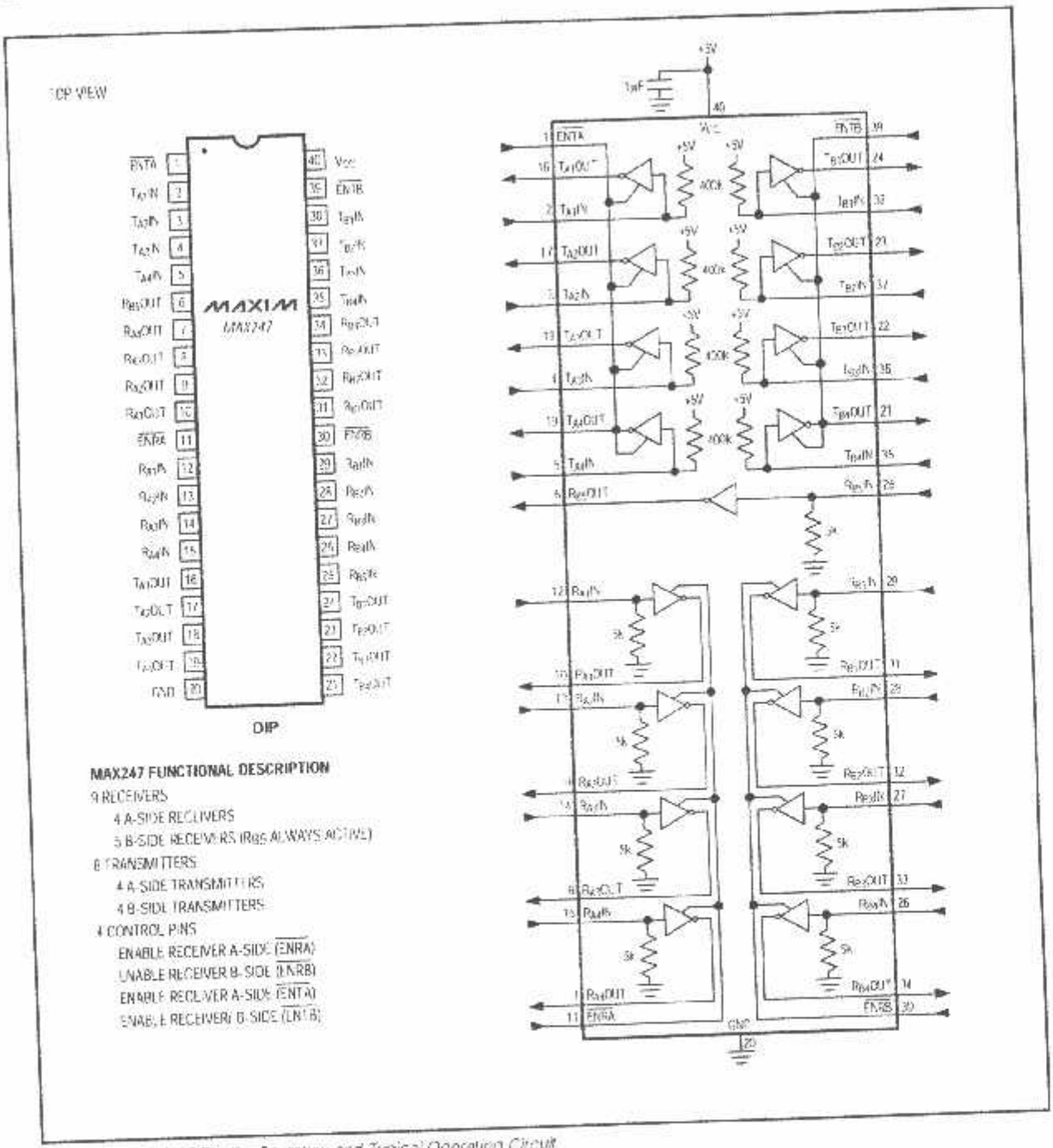
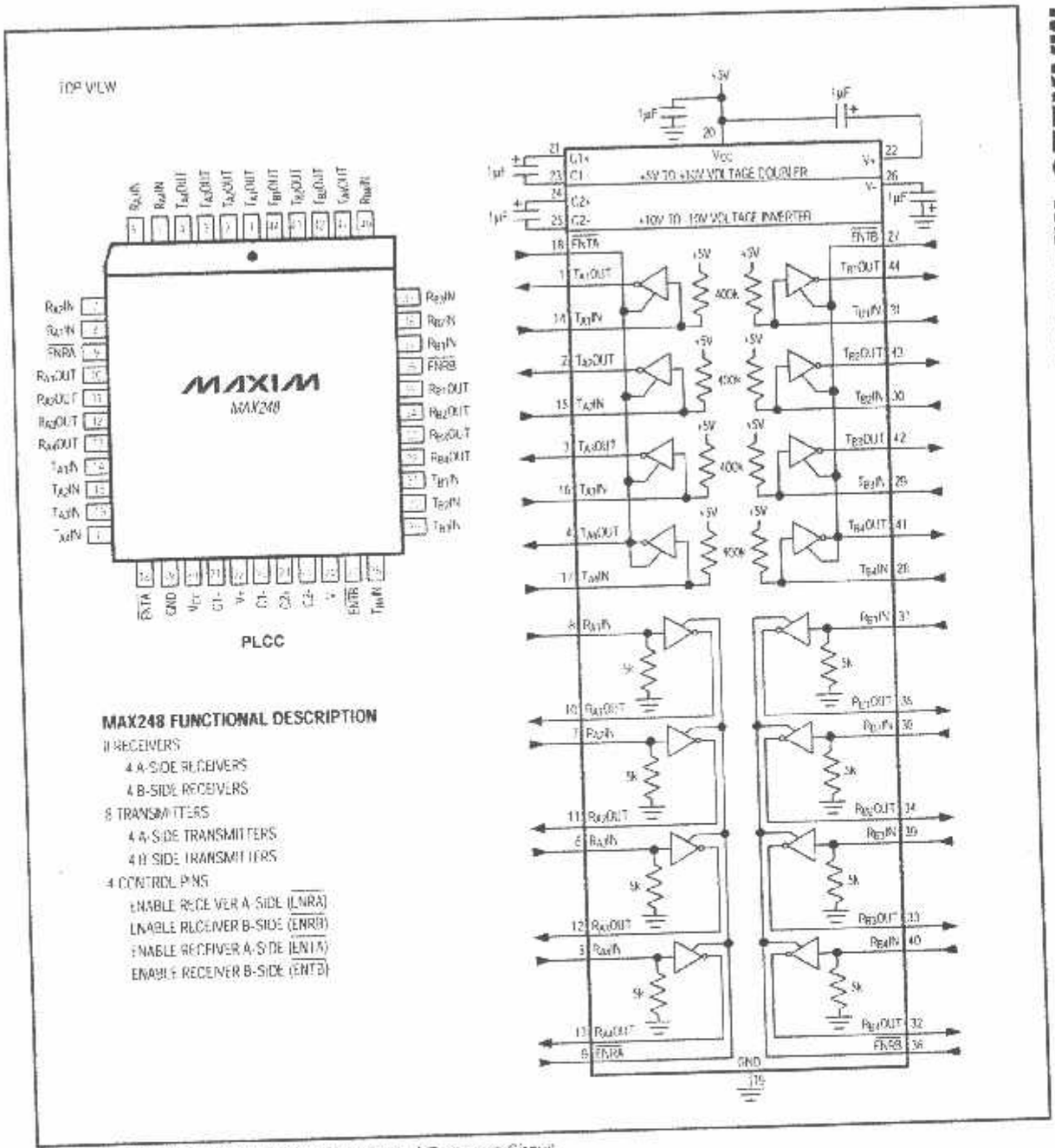


Figure 23. MAX247 Pin Configuration and Typical Operating Circuit



MAX248 FUNCTIONAL DESCRIPTION

8 RECEIVERS
- 4 A-SIDE RECEIVERS
- 4 B-SIDE RECEIVERS

8 TRANSMITTERS
- 4 A-SIDE TRANSMITTERS
- 4 B-SIDE TRANSMITTERS

4 CONTROL PINS
- ENABLE RECEIVER A-SIDE ($\overline{ENRA}$)
- ENABLE RECEIVER B-SIDE ($\overline{ENRB}$)
- ENABLE RECEIVER A-SIDE ($\overline{EN1A}$)
- ENABLE RECEIVER B-SIDE ($\overline{EN1B}$)

Figure 24. MAX248 Pin Configuration and Typical Operating Circuit

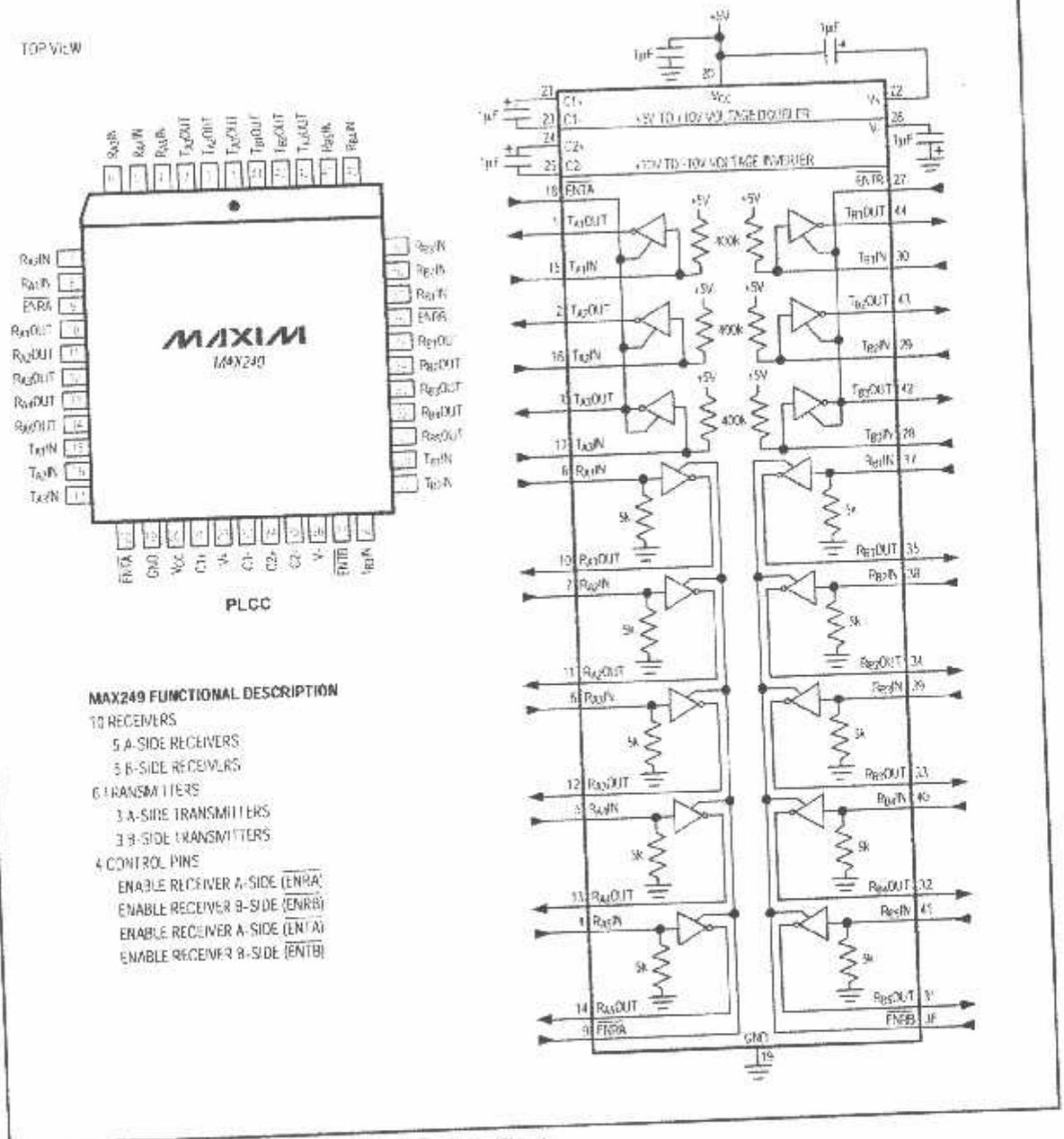


Figure 25. MAX249 Pin Configuration and Typical Operating Circuit

Ordering Information (continued)

PART	TEMP. RANGE	PIN-PACKAGE
MAX222CPN	0°C to +70°C	18 Plastic DIP
MAX222CWN	0°C to +70°C	18 Wide SO
MAX222C/D	0°C to +70°C	Dice*
MAX222EPN	-40°C to +85°C	18 Plastic DIP
MAX222EWN	-40°C to +85°C	18 Wide SO
MAX222EJN	-40°C to +85°C	18 CERDIP
MAX222MJN	-55°C to +125°C	18 CERDIP
MAX223CAI	0°C to +70°C	28 SSOP
MAX223CWI	0°C to +70°C	28 Wide SO
MAX223C/D	0°C to +70°C	Dice*
MAX223EAI	-40°C to +85°C	28 SSOP
MAX223EWI	-40°C to +85°C	28 Wide SO
MAX225CWI	0°C to +70°C	28 Wide SO
MAX225EWI	-40°C to +85°C	28 Wide SO
MAX230CPP	0°C to +70°C	20 Plastic DIP
MAX230CWP	0°C to +70°C	20 Wide SO
MAX230C/D	0°C to +70°C	Dice*
MAX230EPP	40°C to +85°C	20 Plastic DIP
MAX230EWP	-40°C to +85°C	20 Wide SO
MAX230EJP	-40°C to +85°C	20 CERDIP
MAX230MJP	-55°C to +125°C	20 CERDIP
MAX231CPD	0°C to +70°C	14 Plastic DIP
MAX231CWE	0°C to +70°C	16 Wide SO
MAX231CJD	0°C to +70°C	14 CERDIP
MAX231C/D	0°C to +70°C	Dice*
MAX231EPD	-40°C to +85°C	14 Plastic DIP
MAX231EWE	40°C to +85°C	16 Wide SO
MAX231EJD	-40°C to +85°C	14 CERDIP
MAX231MJD	-55°C to +125°C	14 CERDIP
MAX232CPE	0°C to +70°C	16 Plastic DIP
MAX232CSE	0°C to +70°C	16 Narrow SO
MAX232CWE	0°C to +70°C	16 Wide SO
MAX232C/D	0°C to +70°C	Dice*
MAX232EPE	-40°C to +85°C	16 Plastic DIP
MAX232ESE	-40°C to +85°C	16 Narrow SO
MAX232EWE	40°C to +85°C	16 Wide SO
MAX232EJE	-40°C to +85°C	16 CERDIP
MAX232MJE	-55°C to +125°C	16 CERDIP
MAX232MLP	-55°C to +125°C	20 LCC
MAX232ACPE	0°C to +70°C	16 Plastic DIP
MAX232ACSE	0°C to +70°C	16 Narrow SO
MAX232ACWE	0°C to +70°C	16 Wide SO
MAX232AC/D	0°C to +70°C	Dice*
MAX232AEPE	-40°C to +85°C	16 Plastic DIP
MAX232AESE	-40°C to +85°C	16 Narrow SO
MAX232AEWE	-40°C to +85°C	16 Wide SO
MAX232AEJE	-40°C to +85°C	16 CERDIP
MAX232AMJE	-55°C to +125°C	16 CERDIP
MAX232AMLP	-55°C to +125°C	20 LCC
MAX233CPP	0°C to +70°C	20 Plastic DIP
MAX233EPP	-40°C to +85°C	20 Plastic DIP
MAX233ACPP	0°C to +70°C	20 Plastic DIP
MAX233ACWP	0°C to +70°C	20 Wide SO
MAX233AEPP	-40°C to +85°C	20 Plastic DIP
MAX233AEWP	-40°C to +85°C	20 Wide SO
MAX234CPE	0°C to +70°C	16 Plastic DIP
MAX234CWE	0°C to +70°C	16 Wide SO
MAX234C/D	0°C to +70°C	Dice*
MAX234EPE	-40°C to +85°C	16 Plastic DIP
MAX234EWE	-40°C to +85°C	16 Wide SO
MAX234EJE	-40°C to +85°C	16 CERDIP
MAX234MJE	-55°C to +125°C	16 CERDIP
MAX235CPG	0°C to +70°C	24 Wide Plastic DIP
MAX235EPG	-40°C to +85°C	24 Wide Plastic DIP
MAX235EDG	40°C to +85°C	24 Ceramic SB
MAX235MDG	-55°C to +125°C	24 Ceramic SB
MAX236CNG	0°C to +70°C	24 Narrow Plastic DIP
MAX236CWG	0°C to +70°C	24 Wide SO
MAX236C/D	0°C to +70°C	Dice*
MAX236ENG	-40°C to +85°C	24 Narrow Plastic DIP
MAX236EWG	-40°C to +85°C	24 Wide SO
MAX236ERG	-40°C to +85°C	24 Narrow CERDIP
MAX236MRG	-55°C to +125°C	24 Narrow CERDIP
MAX237CNG	0°C to +70°C	24 Narrow Plastic DIP
MAX237CWG	0°C to +70°C	24 Wide SO
MAX237C/D	0°C to +70°C	Dice*
MAX237ENG	-40°C to +85°C	24 Narrow Plastic DIP
MAX237EWG	-40°C to +85°C	24 Wide SO
MAX237ERG	-40°C to +85°C	24 Narrow CERDIP
MAX237MRG	-55°C to +125°C	24 Narrow CERDIP
MAX238CNG	0°C to +70°C	24 Narrow Plastic DIP
MAX238CWG	0°C to +70°C	24 Wide SO
MAX238C/D	0°C to +70°C	Dice*
MAX238ENG	-40°C to +85°C	24 Narrow Plastic DIP

*Contact factory for dice specifications