INSTITUT TEKNOLOGI NASIONAL MALANG
FAKULTAS TEKNOLOGI INDUSTRI
JURUSAN TEKNIK ELEKTRO S - 1
KONSENTRASI TEKNIK ELEKTRONIKA

SKRIPSI

PERENCANAAN DAN PEMBUATAN ROBOT CERDAS PEMADAM API BERBASIS MIKROKONTROLLER

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MARET 2007

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PERENCANAAN DAN PEMBUATAN ROBOT CERDAS PEMADAM API BERBASIS MIKROKONTROLLER

SKRIPSI

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2007

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ABSTRAKSI

PERANCANGAN DAN PEMBUATAN ROBOT CERDAS PEMADAM API BERBASIS MIKROKONTROLLER

(Hijriyah Irawan, 02 17 012, Teknik Elektro / Elektronika S-1)

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Kata Kunci : Robot, Pemadam, Api

Alat yang dirancang merupakan robot pencari api pada ruangan, yaitu robot bergerak ke beberapa ruangan untuk mencari letak api dan memadamkanya tanpa bantuan kabel atau remot control.

Robot bergerak dan tetap pada jalurnya di karenakan adanya sensor yang terpasan di samping kanan dan kiri serta di depan serta belakang, robot ini dapat mendeteksi sumber api berupa lilin pada jarak 40cm dengan menggunakan Detektor *Flame* UVtron.

Setelah proses pengujian, didapatkan dari beberapa kali pengujian robot tidak dapat mendeteksi api dan memedamkan api sebanyak 1 kali.

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Syukur alhamdulillah kepada Allah SWT yang telah memberikan rahmat taufiq serta hidayah-Nya kepada kita semua atas segala-galanya sehingga penyusun dapat menyelesaikan tugas akhir yang berjudul :

" PERANCANGAN DAN PEMBUATAN ROBOT CERDAS PEMADAM API BERBASIS MIKROKONTROLLER"

Pembuatan tugas akhir ini disusun guna memenuhi syarat akhir kelulusan pendidikan jenjang Strata-1 di Institut Teknologi Nasional Malang. Selama pembuatan tugas akhir ini telah melewatkan waktu yang sangat berharga. Inti dari pembuatan tugas akhir adalah sebagai wujud tanggung jawab atas ilmu yang diperoleh selama kuliah.

Penyusun menyadari bahwa penyelesaian skripsi ini tidak terlepas dari bantuan, bimbingan dan dukungan dari berbagai pihak. Oleh karena itu pada kesempatan ini penulis ingin menyapaikan rasa terima kasih, khususnya kepada :

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Penyusun juga menyadari bahwa dalam laporan ini tentu masih ada kekuranganya, oleh karena itu penyusun mengharapkan adanya masukan demi penyempurnaannya.

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Malang, Maret 2007

Penyusun

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BAB I

PENDAHULUAN

1.1. Latar Belakang

Api sangat bermanfaat bagi kehidupan mausia semua sifat api bisa di manfaatkan oleh manusia, seperti panas api bisa di pakai untuk memasak makanan sehari-hari, serta sinar api menjadi pelita di desa yang belum terjangkau listrik dan juga memberi keindahan pada rangkaian lilin yang membuat pesta menjadi lebih syahdu, tetapi api juga dapat menjadi bencana kebakaran bila sudah di luar kendali manusia. Kita tahu bahwa setiap kebakaran selalu diawali dengan kebakaran kecil, yang bila kita tahu dan bila kita mau , api kecil itu bias langsung di padamkan dengan mudah.

Sejalan dengan perkembangan teknologi di bidang elektronika, maka penulis mencoba menerapkan teknologi elektronika dalam membantu manusia untuk meminimalisai kemungkinan terjadinya kebakaran. Hal itu di lakukan dengan menerapkan otomatisasi pada robot mekatronika yang mampu mendeteksi adanya api pada ruangan dan memadamkanya.

1.2. Tujuan

Penulisan skripsi ini bertujuan untuk merancang dan membuat Robot Cerdas pemadam api berbasis Mikrokontroler dengan sistem Robot otomatis atau mengenali warna, panas (api) dan ruang.

1.3. Rumusan Masalah

Berdasarkan latar belakang yang telah diuraikan pada bagian sebelumnya, maka dapat diuraikan beberapa masalah yang akan dibahas yaitu :

1. Merancang dan membuat hardware robot otomatis dalam ruang untuk memadamkan api dengan teknologi Mikrokontroller.
2. Merancang suatu sistem untuk mengenali panas, warna dan ruang.

1.4. Batasan Masalah

Dalam penyusunan skripsi ini diperlukan suatu batasan masalah agar tidak menyimpang dari ruang lingkup yang akan dibahas, batasan masalah meliputi :

1. Robot hanya mengenal dan mendeteksi panas (api), warna putih dan ruang.
2. Pengujian hanya dibatasi 4 ruang (starcase, sound dan white line)
3. Tidak membahas model robot.
4. Model bangunan hanya dalam 1 lantai
5. Sistem yang dibuat adalah sebatas simulasi yang diserupakan dengan keadaan sebenarnya dilapangan.
6. Tidak membahas tentang sudut.
7. Tidak membahas ruang mana yang akan dimasuki lebih dulu.
8. Dalam ruangan hanya terdapat 1 robot dan 1 titik api atau lilin.

1.5. Metodologi

Metodologi penulisan yang digunakan penulisan dalam penyelesaian penulisan skripsi ini adalah :

1. *Study* Pustaka

   Untuk mendapatkan bahan referensi yang mendukung penulisan skripsi ini, yaitu dengan mempelajari beberapa perpustakaan, baik keputusan tentang perangkat keras, perangkat lunak, teori dasar yang mendukung maupun tentang perangkat pendukung lainya.

2. Perancangan Dan Pembuatan *Hardware* beserta *Software*

   Dari permasalahan yang ada, kemudian dirancang suatu sistem untuk mengurangi pemrosesan mulai dalam mendeteksi suatu api.

3. Pengujian Dan Analisa

   Setelah semua sistem selesai dibuat maka diadakan pengujian dan penganalisaan untuk mendapat keakuratan dari sistem yang di rancang.

4. Penyusunan Laporan

   Penyusunan laporan skripsi dibuat sesuai dengan sistematik pembahasan yang telah ditetapkan.

1.6. Sistematika Penulisan

Kerangka penjelasan untuk penyusunan laporan perancangan dan pembuatan robot cerdas pemadam api ini meliputi beberapa pokok bahasan yang terbagi dalam beberapa bab, sebagai berikut :

BAB I PENDAHULUAN

Pada bab ini membahas mengenai Latar Belakang, Rumusan Masalah, Tujuan, Batasan Masalah, Metodologi serta Sistematika Penulisan.

BAB II LANDASAN TEORI

Pada bab ini membahas mengenai teori-teori dasar yang mendukung dalam perancangan sistem yang dibuat. Selain itu digunakan untuk memberikan bahan penunjang untuk memahami dari keseluruhan sistem yang dirancang.

BAB III PERANCANGAN DAN PEMBUATAN ALAT

Pada bab ini membahas tentang perancangan dan pembuatan minimum sistem sebagai robot pemadam api yang meliputi perancangan rangkaian minimum sistem, mekanisme kerja minimum sistem skematik rangkaian dari minimum sistemnya.

BAB IV PERANCANGAN DAN PEMBUATAN ALAT

Pada bab ini membahas tentang uji coba alat, pengamatan, pengukuran dan analisa dari system yang dibuat.

BAB V PENUTUP

Pada bab ini membahas tentang kesimpulan yang dapat diambil dari perancangan dan pembuatan sistem serta saran-saran untuk perbaikan dan untuk pengembangan lebih lanjut.

BAB II

LANDASAN TEORI

2.1. Pendahuluan

Untuk dapat memahami alat yang akan dirancang, maka dalam bab ini akan dijelaskan mengenai teori dasar yang akan berkaitan dengan sistem yang digunakan pada perancangan dan pembuatan alat.

2.2. Mikrokontroler AT89S8252

2.2.1. Fitur Mikrokontroler AT89S8252

Perbedaan mendasar antara mikrokontroler dan mikroprosesor adalah mikrokontroler selain memiliki CPU juga dilengkapi memori dan input output yang merupakan kelengkapan sebagai sistem minimum mikrokomputer sehingga sebuah mikrokontroler dapat dikatakan sebagai mikrokomputer dalam keeping tunggal (*Single Chip Microcomputer*) yang dapat berdiri sendiri.

Mikrokontroler AT89S8252 adalah mikrokontroler ATMEL yang kompatibel penuh dengan Mikrokontroler keluarga MCS-51, membutuhkan daya rendah, memiliki performance yang tinggi dan merupakan mikrokomputer 8 bit yang dilengkapi dengan *8* Kilo*byte Flash* memori untuk program, *2* Kilo*byte EEPROM (Electrical Eraseable And Programmable Read Only Memory)* dan 256 *Byte* RAM *internal*. Program memori yang dapat diprogram ulang dalam sistem atau menggunakan programmer nonvolative memori konvensional. Dalam sistem mikrokontroler terdapat dua hal mendasar yaitu : perangkat lunak dan perangkat keras yang keduanya saling terkait dan mendukung.

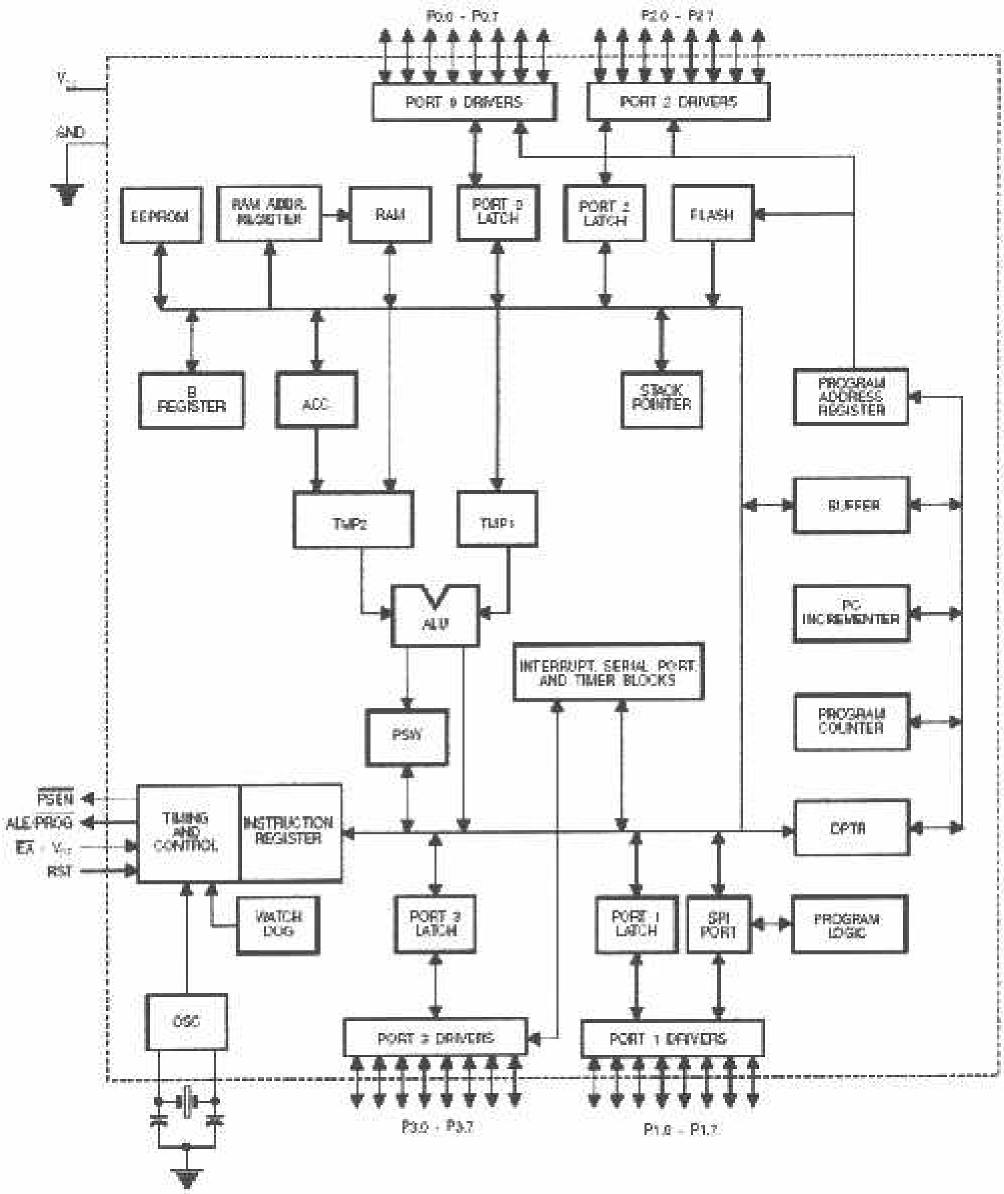
2.2.2. Arsitektur Mikrokontroler AT89S8252

Secara umum Mikrokontroler AT89S8252 memiliki :

- CPU 8 bit termasuk keluarga MCS-51.
- 8 Kbyte *Flash* Memori.
- 256 Byte *Internal* Memori.
- 32 Port I/O, masing-masing terdiri atas 6 jalur I/O.
- 3 *Timer/Counter* 16 Bit.
- 2 Serial Port *Full Duplex*.
- Kecepatan pelaksanaan instruksi per siklus 1 μS pada frekuensi *clock* 12 MHz.
- 2 DPTR (Data *Pointer*).
- *Watchdog time.r*
- *Fleksibel* ISP *Programing*.

Dengan keistimewaan diatas pembuatan alat menggunakan AT89S8252 menjadi lebih sederhana dan tidak memerlukan IC pendukung yang banyak.

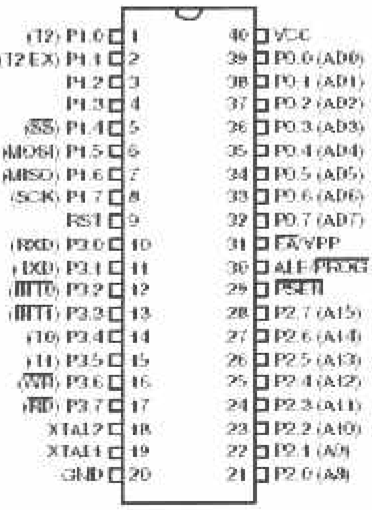
Adapun blok diagram dari Mikrokontroler AT89S8252 adalah sebagai berikut :



Gambar 2-1 Diagram Blok Mikrokontroler AT89S8252

2.2.3. Konfigurasi Pin - Pin Mikrokontroler AT89S8252

Mikrokontroler AT89S8252 terdiri dari 40 pin dengan konfigurasi sebagai berikut:



Gambar 2-2. Konfigurasi Pin-Pin AT89s8252

Fungsi-fungsi tiap pinnya adalah sebagai berikut :

- Pin 40 sebagai sumber tegangan (Vcc)
- Pin 20 sebagai Ground
- Port 0 pada pin 32 - 39

  Merupakan port input-output dua arah, tanpa internal *pull-up* dan konfigurasi sebagai multipleks bus alamat rendah (A_0-A_7) dan data selain pengaksesan program memori dan data memori eksternal.
- Port 1 pada pin 1 - 8

  Merupakan port input-output dua arah dengan internal *pull-up*.

- Port 2 pada pin 21 - 28

  Merupakan port input-output dengan internal *pull-up*. Mengeluarkan alamat tinggi selama pengambilan program memori eksternal.

- Port 3 pada pin 10 - 17

  Merupakan port input-output dengan internal *pull-up*, dimana port 3 juga memiliki fungsi khusus dan dapat dilihat pada tabel berikut :

Tabel 2-1. Fungsi Khusus Pada Port 3

Identitas Port	Fungsi Khusus
Port 3.0	RxD (Port Masukan khusus)
Port 3.1	TxD (Port Keluaran Khusus)
Port 3.2	/INT0 (Masukan Interupsi Eksternal 0)
Port 3.3	/INT1 (Masukan Interupsi Eksternal 1)
Port 3.4	T0 (Masukan Pewaktu Eksternal 0)
Port 3.5	T1(Masukan Pewaktu Eksternal 1)
Port 3.6	/WR (Sinyal Tulis Memori Data Eksternal)
Port 3.7	/RD (Sinyal Baca Memori Data Eksternal)

- RST (Reset) pada pin 9

  Input reset merupakan reset master untuk AT89S8252

- ALE /Prog (*Address Lacth Enable*) pada pin 30

  Digunakan untuk menahan alamat memori eksternal selama pelaksanaan intruksi.

- PSEN *(Program Store Enable)* pada pin 29

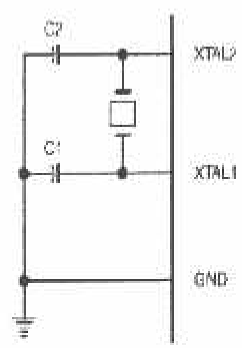
Merupakan sinyal pengontrol yang memperbolehkan program memori eksternal masuk ke dalam bus.

- EA/VPP *(External Access)*, pin 31

Dapat diberikan logika rendah (Ground) atau logika tinggi (+5 Volt). Jika diberikan logika tinggi maka mikrokontroler akan mengakses program dari ROM internal (EEPROM/*Flash* Memori), dan jika diberikan logika rendah maka mikrokontroler akan mengakses program dari memori eksternal.

- X-TAL 1 dan X-TAL 2 pada pin 18 dan 19

Pin ini dihubungkan dengan kristal bila menggunakan osilator internal. X-TAL 1 merupakan masukan ke rangkaian osilator internal sedangkan X-TAL 2 keluaran dari rangkaian osilator internal. Untuk keperluan ini diperlukan kapasitor penstabil sebesar 30 pF. Dan nilai dari X-TAL tersebut antara 4 - 24 Mhz. untuk lebih jelasnya dapat dilihat gambar pemasangan X-TAL serta kapasitor yang digunakannya.



Gambar 2-3. Osilator Eksternal AT89S8252

2.2.4. Organisasi Memory

Organisasi memori pada mikrokontroler AT89S8252 dapat dibagi menjadi dua bagian besar yaitu memori program dan memori data. Pembagian tersebut didasarkan atas fungsi dari penyimpanan data maupun program. Memori program digunakan untuk menyimpan instruksi-instruksi yang akan dijalankan oleh mikrokontroler, sedangkan memori data digunakan sebagai tempat yang sedang diolah mikrokontroler.

Program mikrokontroler disimpan dalam memori program berupa ROM. Mikrokontroler AT89S8252 dilengkapi dengan ROM internal, sehingga untuk menyimpan program tidak digunakan ROM eksternal yang terpisah dari mikrokontroler. Agar tidak menggunakan memori program eksternal, pin EA dihubungkan dengan Vcc (logika 1).

Memori program mikrokontroler menggunakan alamat 16 Bit mulai dari 0000_H – $0FFF_H$ sehingga kapasitas penyimpanan program maksimal adalah 4 Kbyte. Sinyal / PSEN *(Program Store Enable)* tidak digunakan jika menggunakan memori program internal.

Selain program mikrokontroler AT89S8252 juga memiliki data internal sebesar 128 Byte dan mampu mengakses memori data eksternal sebear 64 Kbyte. Semua memori data internal dapat dialamati dengan data langsung atau tidak langsung. Ciri dari pengalamatan langsung *operand* adalah alamat register yang berisi alamat data yang akan diolah. Sebagian memori tersebut dapat dialamati dengan pengalamatan register, dan sebagian lagi dapat dialamati dengan memori satu bit. Untuk membaca data digunakan sinyal / RD sedangkan untuk menulis digunakan sinyal / WR.

2.2.5. SFR *(Special Fuction Register)*

Register Fungsi Khusus *(Special fuction Register)* terletak pada 128 byte bagian atas memori data internal dan berisi register-register untuk pelayanan latch port, timer, program status word (PSW), control peripheral dan sebagainya.

Beberapa macam register fungsi khusus yang sering digunakan adalah sebagai berikut :

- *Accumulator* (ACC) merupakan register untuk penambahan dan pengurangan, perintah Mneumonic untuk mengakses akumulator disederhanakan sebagai A.
- *Register B* merupakan register khusus yang berfungsi melayani operasi perkalian dan pembagian.
- *Stack Pointer* (SP) merupakan register 8 bit yang dapat diletakkan di alamat manapun pada RAM internal.
- *2 Data Pointer* (DPTR) terdiri atas dua register yaitu untuk byte tinggi (*data pointer high*, DPH) dan byte rendah (*data Pointer Low*, DPL) yang berfungsi untuk mengunci alamat 16 bit.
- *Port 0 sampai port 3* merupakan register yang berfungsi untuk membaca dan mengeluarkan data pada port 0, 1, 2, dan 3. Masing-masing register ini dapat dialamati per-*byte* maupun per-bit.
- *Control Register* terdiri dari register yang mempunyai fungsi kontrol. Untuk mengontrol sistem interupsi, terdapat dua register khusus yaitu register IP (*Interrupt Priority*) dan register IE *(Interupt Enable*). Untuk mengontrol pelayanan timer/counter terdapat register khusus yaitu register TCON (*Timer/Counter Control*) serta pelayanan port serial menggunakan register SCON (*Serial Port Control)*.

Tabel 2-2. ***Special Fuction Register*** **AT89S8252 SFR Map dan Reset Values**

0F8H									0FFH
0F0H	B 00000000								0F7H
0E8H									0EFH
0E0H	ACC 00000000								0E7H
0D8H									0DFH
0D0H	PSW 00000000					SPCR 000001XX			0D7H
0C8H	T2CON 00000000	T2MOD XXXXXX00	RCAP2L 00000000	RCAP2H 00000000	TL2 00000000	TH2 00000000			0CFH
0C0H									0C7H
0B8H	IP XX000000								0BFH
0B0H	P3 11111111								0B7H
0A8H	IE 0X000000		SPSR 00XXXXXX						0AFH
0A0H	P2 11111111								0A7H
98H	SCON 00000000	SBUF XXXXXXXX							9FH
90H	P1 11111111						WMCON 00000010		97H
88H	TCON 00000000	TMOD 00000000	TL0 00000000	TL1 00000000	TH0 00000000	TH1 00000000			8FH
80H	P0 11111111	SP 00000111	DP0L 00000000	DP0H 00000000	DP1L 00000000	DP1H 00000000	SPDR XXXXXXXX	PCON 0XXX0000	87H

2.2.6. Sistem Interupsi

Mikrokontroler AT89S8252 mempunyai 5 buah sumber interupsi yang dapat membangkitkan permintaan yaitu INT0, INT1, T1, T2 dan Port Serial.

Saat terjadinya interupsi mikrokontroler secara otomatis akan menuju ke subrutin pada alamat tersebut. Setelah interupsi selesai dikerjakan, mikrokontroler akan mengerjakan program semula. Tiap-tiap sumber interupsi dapat *enable* atau *disable* secara software.

Tingkat prioritas semua sumber interrupt dapat diprogram sendiri-sendiri dengan set atau *clear* bit pada (*interrupt priority*). Jika dua permintaan interupsi dengan tingkat prioritas yang berbeda diterima secara bersamaan akan dilakukan polling untuk menentukan mana yang akan dilayani.

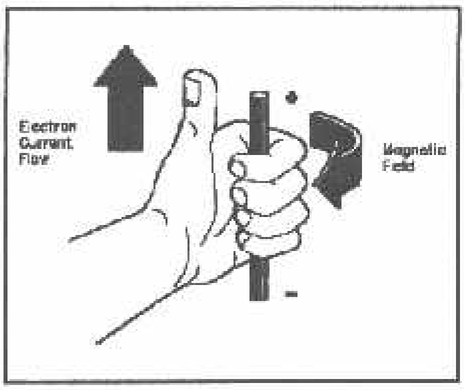
Tabel 2-3. Alamat Sumber Interupsi

Sumber Interupsi	Alamat Awal
Interupt Luar 0 (INT 0)	03_H
Pewaktu/Pencacah 0 (T0)	$0B_H$
Interrupt Luar 1 (INT 0)	13_H
Pewaktu/Pencacah 0 (T0)	$1B_H$
Port Serial	23_H

2.3. Pengendali Arah Putaran Motor DC

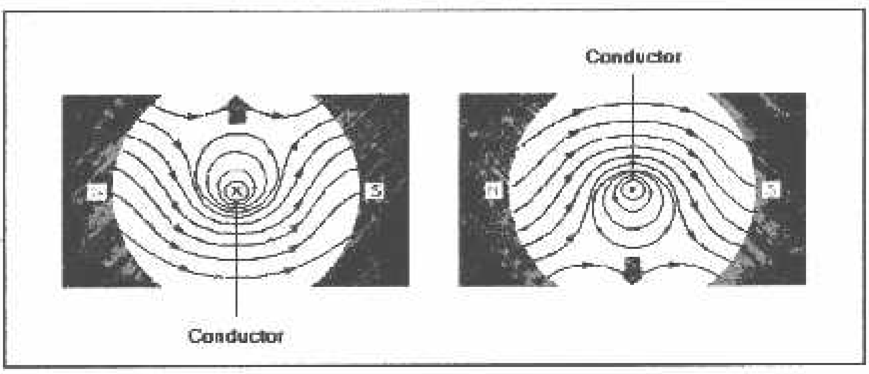
2.3.1. Teori Dasar Motor DC

Setiap arus yang mengalir melalui sebuah konduktor akan menimbulkan medan magnet. Arah medan magnet dapat ditentukan dengan kaidah tangan kiri. Ibu jari tangan menunjukkan arah aliran arus listrik sedangkan jari-jari yang lain menunjukkan arah medan magnet yang timbul, seperti yang ditunjukkan oleh gambar 2-4 berikut ini.



Gambar 2-4. Kaidah Tangan Kiri

Jika suatu konduktor yang dialiri arus listrik ditempatkan dalam sebuah medan magnet, kombinasi medan magnet akan ditunjukkan oleh gambar 2-8. Arah aliran arus listrik dalam konduktor ditunjukkan dengan tanda "x" atau ".". Tanda "x" menunjukkan arah arus listrik mengalir menjauhi pembaca gambar, tanda "." menunjukkan arah arus listrik mengalir mendekati pembaca gambar.



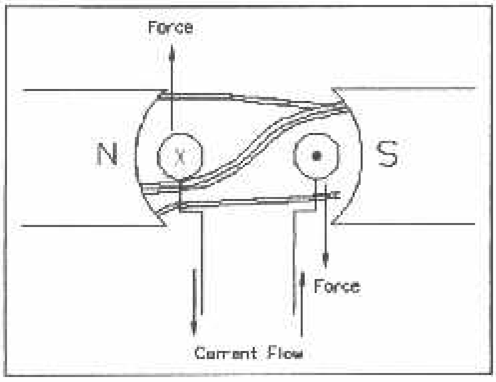
Gambar 2-5. Konduktor Berarus Listrik Dalam Medan Magnet

Pada gambar sebelah kiri, arah medan magnet pada sisi atas yang dihasilkan oleh konduktor berlawanan dengan arah medan magnet yang dihasilkan oleh magnet permanen. Sementara pada sisi sebelah bawah, arah medan magnet yang dihasilkan oleh konduktor searah dengan arah medan magnet yang dihasilkan oleh magnet permanen. Dengan kata lain, pada sisi sebelah atas kerapatan fluks magnet lebih sedikit dari pada sisi sebelah bawah. Sebuah gaya dorong akan menyebabkan konduktor bergerak ke sisi sebelah atas.

Pada gambar sebelah kanan, arah medan magnet pada sisi atas yang dihasilkan oleh konduktor searah dengan arah medan magnet yang dihasilkan oleh magnet permanen. Sementara pada sisi sebelah bawah, arah medan magnet yang dihasilkan oleh konduktor berlawanan dengan arah medan magnet yang dihasilkan oleh magnet permanen. Dengan kata lain, pada sisi sebelah bawah kerapatan fluks magnet lebih sedikit dari pada sisi sebelah atas. Sebuah gaya dorong akan menyebabkan konduktor bergerak ke sisi sebelah bawah.

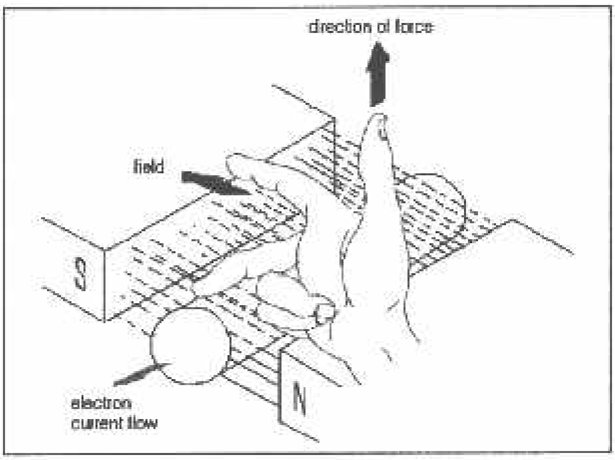
Pada sebuah motor DC, konduktor dibentuk menjadi sebuah loop sehingga ada dua bagian konduktor yang berada didalam medan magnet pada saat yang sama, seperti diperlihatkan pada gambar 2-9.

Konfigurasi konduktor seperti ini akan menghasilkan distorsi pada medan magnet utama dan menghasilkan gaya dorong pada masing-masing konduktor. Pada saat konduktor di tempatkan pada rotor, gaya dorong yang timbul akan menyebabkan rotor berputar searah dengan jarum jam, seperti diperlihatkan pada gambar 2-9.



Gambar 2-6. Bergeraknya Sebuah Motor

Sebuah cara lagi untuk menunjukkan hubungan antara arus listrik yang mengalir didalam sebuah konduktor, medan magnet dan arah gerak, adalah kaidah tangan kanan untuk motor seperti yang diperlihatkan pada gambar 2-10.



Gambar 2-7. Kaidah Tangan Kanan Untuk Motor

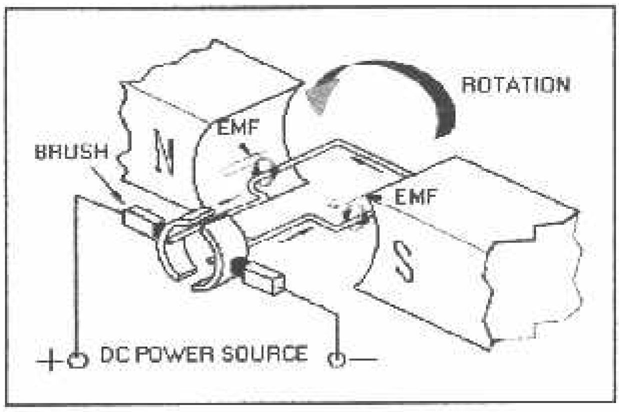
Kaidah tangan kanan untuk motor menunjukkan arah arus yang mengalir didalam sebuah konduktor yang berada dalam medan magnet. Jari tengah menunjukkan arah arus yang mengalir pada konduktor, jari telunjuk menunjukkan arah medan magnet dan ibu jari menunjukkan arah gaya putar. Adapun besarnya gaya yang bekerja pada konduktor tersebut dapat dirumuskan dengan :

F = B.L.I (Newton)

Dimana : B = kerapatan fluks magnet (weber)

L = panjang konduktor (meter)

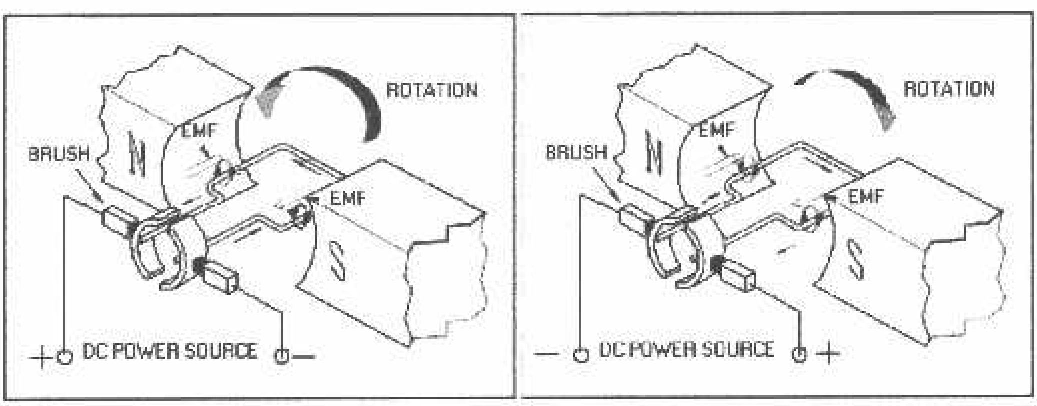
I = arus listrik (ampere)



Gambar 2-8. Konstruksi Dasar Motor DC

Pada gambar 2-11 diatas tampak sebuah konstruksi dasar motor dc, pada gambar diatas terlihat bahwa pada saat terminal motor diberi tegangan dc, maka arus elektron akan mengalir melalui konduktor dari terminal negatif menuju ke terminal positif. Karena konduktor berada diantara medan magnet, maka akan timbul medan magnet juga pada konduktor yang arahnya seperti terlihat pada gambar 2-11. diatas. Arah garis gaya medan magnet yang dihasilkan oleh magnet permanen adalah dari kutub utara menuju ke selatan. Sementara pada konduktor yang dekat dengan kutub selatan, arah garis gaya magnet disisi sebelah bawah searah dengan garis gaya magnet permanen sedangkan di sisi sebelah atas arah garis gaya magnet berlawanan arah dengan garis gaya magnet permanen. Ini menyebabkan medan magnet disisi sebelah bawah lebih rapat daripada sisi sebelah atas. Dengan demikian konduktor akan terdorong ke arah atas. Sementara pada konduktor yang dekat dengan kutub utara, arah garis gaya magnet disisi sebelah atas searah dengan garis gaya magnet permanen sedangkan di sisi sebelah bawah arah garis gaya magnet berlawanan arah dengan garis gaya magnet permanen. Ini menyebabkan medan magnet disisi sebelah atas lebih rapat daripada sisi sebelah bawah. Dengan demikian konduktor akan terdorong ke arah bawah. Pada akhirnya konduktor akan membentuk gerakan berputar berlawanan dengan jarum jam seperti terlihat pada gambar 2-11diatas.

2.3.2. Pengendalian Arah Putaran Motor DC



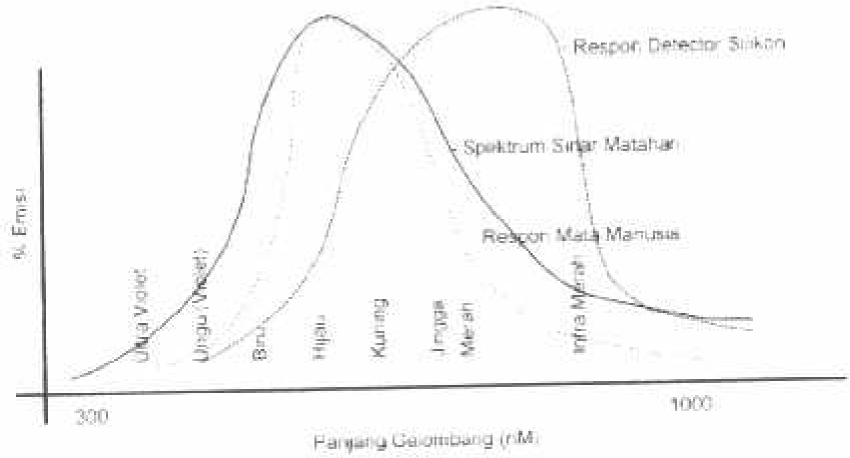
Gambar 2-9. Arah Putaran Motor DC

Dari gambar 2-12 diatas, agar arah putaran motor DC berubah, maka polaritas tegangan pada terminal motor harus dibalik.

2.4. Dioda Infra Merah

Cahaya infra merah merupakan cahaya yang tidak tampak. Jika dilihat dengan dengan *spektroskop* cahaya maka radiasi cahaya infra merah akan nampak pada spektrum elektromagnet dengan panjang gelombang di atas panjang gelombang cahaya merah. Dengan panjang gelombang ini maka cahaya infra merah ini akan tidak tampak oleh mata namun radiasi panas yang ditimbulkannya masih terasa/dideteksi.

Pada dasarnya komponen yang menghasilkan panas juga menghasilkan radiasi infra merah termasuk tubuh manusia maupun tubuh binatang. Cahaya infra merah, walaupun mempunyai panjang gelombang yang sangat panjang tetap tidak dapat menembus bahan-bahan yang tidak dapat melewatkan cahaya yang nampak sehingga cahaya infra merah tetap mempunyai karakteristik seperti halnya cahaya yang nampak oleh mata.



Gambar 2-10. Spektrum Cahaya dan Respon Mata Manusia

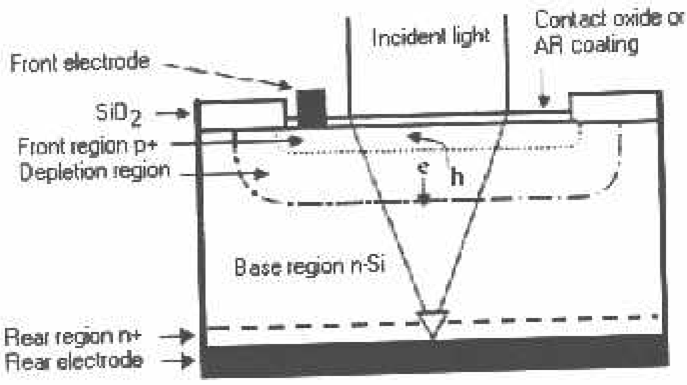
Komponen elektronik yang bisa menghasilkan cahaya infra merah adalah dioda infra merah.

(a) Bentuk Fisik (b) Simbol Elektronika

Gambar 2-11. Dioda Infra Merah

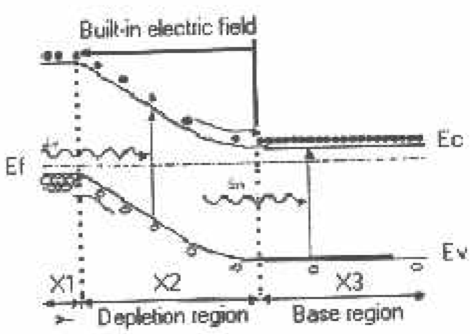
2.4.1 Photodioda

Photodioda merupakan sambungan substrat tipe N dan substrat tipe P yang dirancang untuk beroperasi bila dibiaskan dalam arah terbalik.



Gambar 2-12. Struktur Photodioda

Ketika energi cahaya *(photon)* yang jatuh pada sambungan photodioda lebih besar dari tegangan barrier silikon yaitu 1,12eV, energi cahaya ini dapat menyebabkan elektron keluar dari pita valensi *(valence band)* dan masuk ke pita konduksi *(conduction band)* dan meninggalkan hole pada pita konduksi, dengan kata lain energi cahaya yang jatuh pada sambungan photodioda akan menghasilkan aliran arus *elektron-hole*.



Gambar 2-13. Diagram Pita Konduksi Photodioda

Gambar 2-16. menunjukkan struktur dari photodioda, dimana terdapat *substrat* silikon tipe N , yang diatasnya doping dengan substrat tipe P, seperti *Boron*, dengan penumbuhan secara ion, sebagai suatu cara untuk menghasilkan sebuah sambungan *(junction)*. Pada bagian bawah *wafer (Base Region)* didoping dengan bahan tipe N yang peka cahaya seperti *Phosphorous.*

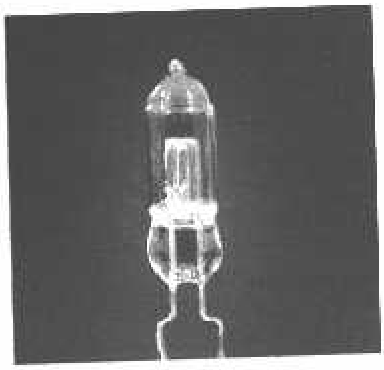
Daerah sambungan *(depletion region)* dibentuk oleh medan elektromagnetik, yang timbul akibat adanya beda potensial sambungan *(junction)*. Daerah sambungan ini sangat menentukan kemampuan kerja photodioda dalam merespon dan mengubah energi cahaya menjadi arus *elektron-hole*. Memperluas daerah sambungan adalah suatu cara untuk meningkatkan kemampuan kerja photodioda. Ini bisa dicapai dengan menerapkan tegangan bias terbalik pada sambungan P-N atau memilih *substrat* silikon tipe N yang lebih sensitif terhadap cahaya dan menebalkan *substrat* P.

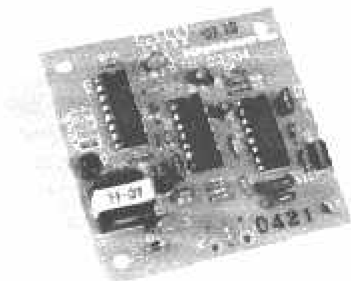
(a) Bentuk fisik (b) Simbol elektronika

Gambar 2-14. Photodioda

2.5. Hamamatsu UVtron Flame Detector

Hamamatsu UVTron Flame Detector dan rangkaian driver dapat mendeteksi api dari lilin atau puntung rokok dalam jarak 5 meter. Biasanya digunakan sebagai alat untuk mendeteksi sumber api seperti lilin, yang beroperasi pada panjang spectral antara 185 hingga 160 nm.





Gambar 2-15. UVtron Flame Detector

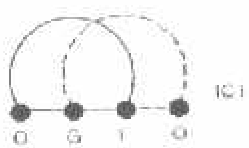
2.5.1. Menghubungkan UVtron dengan papan PCB

Untuk menggerakan papan rangkaian tabung UVtron membutukan solder yang dapat secara langsung dengan gelombang sebelah kanan di atas papan atau anda dapat menambahkan kawat atau kabel sepanjang 5 cm dari posisi tabung Uvtron di tempat lain. Melindungi tabung UVtron yang ada pada papan rangkaian. Kaki kawat katoda adalah kaki kawat yang (pendek), masukan kaki tersebut ke dalam tanda "K" di atas papan penggerak atau pada papan (PCB) dan untuk kaki anoda adalah (kaki kawat yang panjang) di letakan ke dalam lubang yang bertanda "A" pada papan (PCB) ketika ingin menyolder tabung UVtron harus menjaga kestabilan panas sebab sensitife dengan panas yang lebih dari solder besi.

2.5.2. Mengatur Daya Tegangan +5 Volt

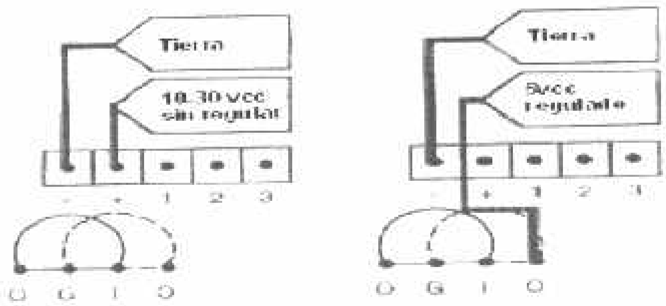
Pada rangkaian penggerak mempunyai spesifikasi tegangan input 10 – 30 Vdc untuk menghindari beban yang berlebihan maka dapat mengatur tegangan agar dapat bekerja. Untuk menggerakan UVtron hannya membutukan arus sebesar 3 mAmpere dengan arus rata-rata tidak menjadi penghalang pada persoalan arusnya.

Yang kita lakukan pada papan penggerak (PCB) tidak merubah tegangan input +5 Volt . Sangat aman apabila kita menggunakan pengaturan tegangan yang kecil. Pada papan (PCB) pengaturan tegangan di beri tanda IC1 yang terdiri dari 4 lubang (3 lubang yang digunakan) dan masing masing lubang di beri tanda 0, G , I dan 0 yang masing masing lubang mempunyai nama / fungsi sebagai output, grond, input, output



Gambar 2-16 . Pengatut Tegangan +5 Volt

Dari empat lubang di atas papan (PCB) tanda "0" tidak digunakan dan 3 lubang lain yang dapat digunakan diberi pengaturan tegangan +5 Volt yang mampu bekerja pada arus 30mV atau menjadi arus puncak. Langkah selanjutnya mengatur tegangan yang lengkap pada papan (PCB) selanjutnya akan ditunjukan 2 pilihan dena diagram dari power supply (penyedia tegangan).



Gambar 2- 17. Dena Diagram *Power Supply*

2.5.3. Keterangan Output / Keluaran

Rangkaian penggerak UVtron menawarkan 3 pilihan output dan pemberian nomer 1, 2, dan 3 yang di pisah-pisahkan dengan heder yang di tunjukan pada gambar di atas disini dijelaskan secara detail dari 3 output :

1. Keluaran dari *cmos* ini cocok dibuat keluaran. Dalam keadaan tidak bergerak rendah / low dan untuk keadan *high* dengan 10ms akan mendeteksi/ menemukan pulsa.
2. Keluaran ini kebalikan dari output nomor 1. dalam keadaan tidak bergerak dia mempunyai kondisi *high* (tinggi) dan untuk keadan yang turun *low* pada setiap 10ms akan mendeteksi / menemukan pulsa.
3. Pada nomor ini mempunyai fungsi membuka keluaran *collector* pada transistor maksudnya dia dapat menggerakan perbedaan tegangan (pada keluaran nomer 1 dan 2 hanya dengan tegangan 0 atau +5Volt) jadi dapat

juga mengemudikan atau menurunkan arus diatas 50ma. Keluaran ini membutuikan resistor fungsi pemberhentian.

Lebar pulsa dari semua 3 output pilihan masing-masing 10ms. Dengan penambahan pada papan (PCB) di dalam lubang yang bertanda CX akan dapat membuat pulsa menjadi tambah panjang. Kapasitor memerlukan / membutukan bentuk gelombang pulsa dengan mengatur polaritas dan memasang ke lubang dengan tanda yang tepat. Contohnya jika 1μF kapasitor yang digunakan maka gelombang pulsa merenggang / memperluas selama 1 detik dan jika 10 μF kapasitor yang digunakan, maka luas pulsa akan sampai 10 detik jika kita membutukan pulsa yang dapat merenggangkan / memperluas lebih kira-kira bisa mencapai lamanya 100 detik.

2.5.4. Yang Melatar Belakangi Penyesuaian dari Pembatalan

Yang melatar belakangi terjadinya pembatalan untuk membiarkan UVtron menjalankan atau menggerakan rangkaian masing jumper di sisi kiri di atas papan (PCB) dengan tanda 3, 5 dan 7 dengan untuk pulsa. Pengaturan 3 pulsa untuk tidak muncul pengaturan perhitungan dari nomor pulsa diterima dalam 2 detik jika pengaturan perhitungan turun kebawah maka pulsa akan mengabaikan untuk mengatasi pengaturan nilai tersebut setiap 2 detik maka pulsa akan mencatatnya.

Beberapa latar belakang untuk merubah pengaturan UVtron untuk memberi cahaya di lingkungan sekitarnya yaitu dengan memberi jumper pada nomor kaki yang di lingkari secara bebas anda dapat menyolder 2 x di tempat pemisah (heider) dan dengan menggunakan jumper untuk mengatur pengaturan.

2.5.5. Cara Pengoperasian

Gelombang UVtron benar-benar sangat sederhana. Ketika sinar-sinar ultraviolet terlindungi oleh katoda (dari lilin), dari photo electron memancarkan katoda yang di berikan akibat oleh photo elektronik kemudian anoda dipancarkan terhadap medan listrik. Ketika pada saat memekai tegangan menjadi tinggi dan medan listrik kuat, maka energi kinetik dari elektron menjadi molekul menginisialisasi cukup besar dari tubrukan gas tertutup di dalam tabung elektron yang di pancarkan dapat menimbulkan ionisasi, yang memungkinkan molekul lain mengionisai sebelum menjangkau anoda dan teori yang lain, dengan mempercapat ion positif terhadap katoda dan bertubrukan dengan yang lain, yang menimbulkan elektron sekunder. Menyebabkan arus yang besar turun seperti salju yang turun diantara molekul yang akan mengalir ke suatu tempat.

Pengaturanya terjadi hanya sekali. tabung yang penuh terisi dengan elektron dan ion.tegangan yang menurun diantara anoda dan katoda dapat mengurangi dari sumbernya. Kemampuan ini mempunyai keadan / sifat tanpa menurunkan tegangan anoda di ujung bawah titik jenuh.

Untuk menciptakan atau membuat rangkaian yang berjalan di perlukan perbedaan tegangan di dalam tabung yang di dalamnya memperoleh proses seperti salju turun ketika memberikan sinar-sinar ultra ungu menjadi arus keluaran dari rangkaian tabung yang ketika terjadi proses salju turun, maka membuat arus mengalir, sekali terjadi pengaliran, tegangan anoda itu akan dikurangi oleh rangkaian yang berbentuk atau memperbolekan gelombang "reset"setiap waktu turun atau drop dan terjadi proses pengaliran yang dikeluarkan pulsa oleh rangkaian itu dengan kondisi untuk beberapa latar belakang.

2.5.6. Prosedur penggunaan

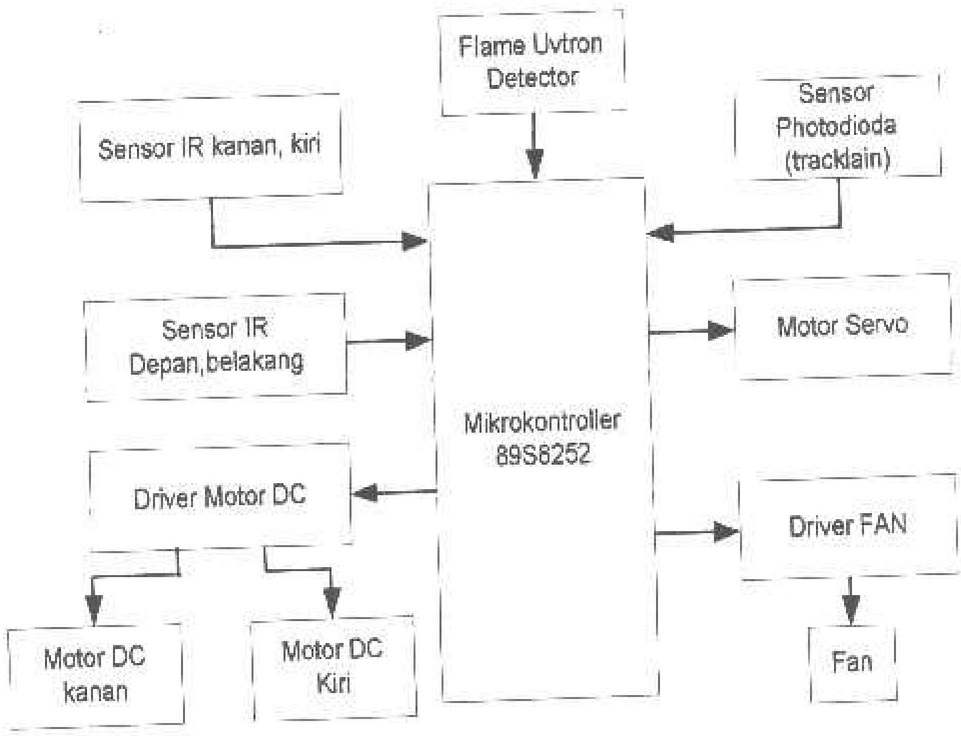
1. Memperlihatkan detector dari medan yang jalanya hampir menutupi bola yang terdapat di dalam gelombang UVtron. Hati-hati dalam meletakan posisinya.
2. Menjaga tabung gelas dari kotoran, debu dan jari-jari yang menempel akan mengurangi keefektifan dari sensor tersebut.
3. Sumbar dari UVtron mungkin akan memberikan cahaya pada di sekitar lingkungan. Memasukkan cahaya halogen di rumah dengan tegangan cahaya yang rendah, cahaya obor, dan lebih penting itu cahaya dari video kamera dengan begitu pembacaan tidak akan salah ketika melakukan percobaan menemukan nyala api.
4. Menjaga hubungan sangat pendek dari gelombang dengan rangkaian penggerak dalam teori, hati-hati memasang atau menyolder tabung UVtron secara langsung pada rangkaian (PCB) kawat yang digunakan di perpanjang hanya 5 cm.
5. Cahaya lembayung ultra (sinar ultrafiolet) melambung sama seperti cahaya lain. Baik untuk keperluan UVtron di butuhkan langsung untuk memperlihatkan penemuanya.

BAB III

PERENCANAAN DAN PEMBUATAN ALAT

3.1. Perancangan Perangkat Keras (Hardware)

Blok diagram sistem dapat dilihat pada gambar dibawah ini:



Gambar 3-1. Diagram Blok Sistem

3.1.1. Perancangan Rangkaian Clock

Rangkaian sistem minimum dari mikrokontroller AT89S8252 salah satunya terdiri dari rangkaian clock. Rangkaian tersebut tersusun dari komponen-komponen 2 buah capasitor, 1 buah IC mikrokontroller, sebuah resistor dan sebuah kristal atau *resonator* keramik. Rangkaian capasitor dan kristal atau *resonator* keramik digunakan sebagai rangkaian pembangkit *internal clock generator* yang terdapat pada AT89S8252. Nilai kapasitansi ditentukan sesuai dengan jenis oscilator yang digunakan, yaitu:

C1 dan C2 = 20pF – 40pF untuk kristal

C1 dan C2 = 30pF – 50pF untuk resonator keramik.

Karena dalam perancangan digunakan oscilator kristal maka nilai capasitor yang dipakai dalam perancangan adalah sebesar 30pF.

Mikrokontroller AT89S8252 mempunyai *frekwensi* maksimal 12 MHz, dimana 1 siklus mesin = 12 clock. Dalam rangkaian digunakan kristal dengan harga 11,0592 MHz, maka program akan dijalankan pada setiap langkahnya selama 1,085 μs. Siklus tersebut diambil berdasarkan ketentuan mikrokontroller AT89S8252 yaitu 12 *clock* = 1 siklus mesin, sedangkan *frekwensi* yang digunakan 12 MHz, maka waktu yang dipakai dalam setiap 1 siklus mesin adalah 1μs. Dengan demikian perhitungannya dapat dilihat sebagai berikut:

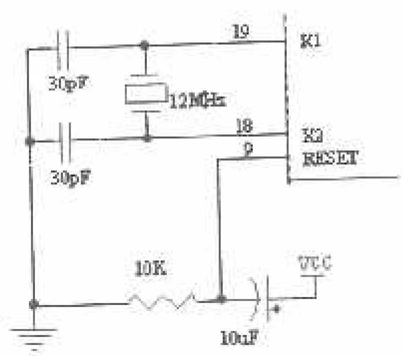
f= 11,0592 MHz

$$T = \frac{1}{f}$$

$$T = \frac{1}{11{,}0592 \times 10^6}$$

Karena 1 siklus mesin = 12T maka,

$$1 \text{ siklus mesin} = 12 \times \frac{1}{11{,}0592 \times 10^6} = 1{,}085\ \mu s.$$



Gambar 3-2. Gambar Rangkaian Clock dari AT89S8252

3.1.2. Sensor Photo dioda (Sensor *Trackline*)

Sensor untuk membedakan warna gelap dan warna terang dari jalur (track) digunakan pasangan diode infra merah dan photodioda. Dioda infra merah akan

Karena dipasaran tidak ada maka diambil nilai terdekatnya yaitu 220 Ω. Sedangkan untuk menentukan nilai resistor *pull up* pada photodioda adalah sebagai berikut :

Diketahui arus pada photodioda *(I_{PD})*sebesar 0,5 mA

$$R_2 = \frac{Vcc}{I_{PD}}$$

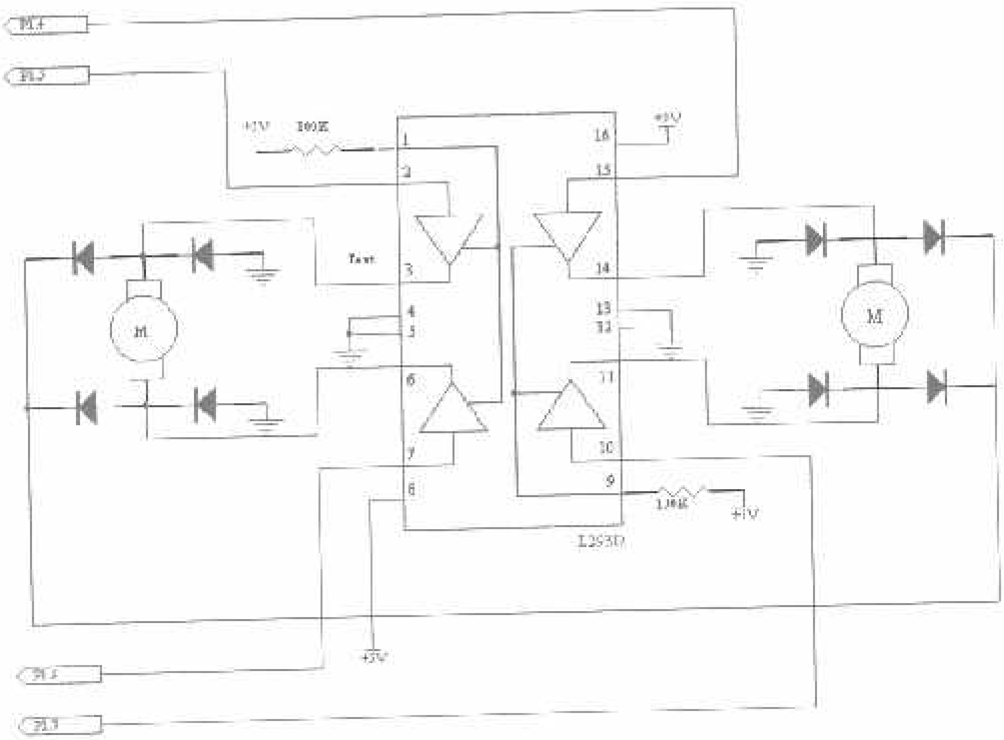
$$R_2 = \frac{5}{0{,}5x10^{-3}}$$

$$R_2 = 10\,K\Omega$$

Pada rangkaian diatas memanfaatkan inverter schmitt trigger yang terdapat pada IC 74LS14. Gerbang ini merupakan fungsi not yang akan membalik kondisi logika input menjadi kebalikannya. Misalnya jika inputnya berlogika "0" maka outputnya akan berlogika "1" atau sebaliknya. Selain itu juga berfungsi untuk mengubah taraf tegangan masukan menjadi taraf tegangan TTL pada keluarannya. Rangkaian sensor infra merah ini dibuat 4 buah dengan nilai komponen yang sama.

3.1.3 Driver Motor DC

Berikut ini adalah gambar skema dari rangkaian penggerak motor dc :



Gambar 3.4 Driver Motor DC

Komponen utama rangkaian penggerak motor dc ini adalah IC L293D yang merupakan IC yang dirancang khusus untuk keperluan pengendalian motor dc. IC L293D didalamnya terdapat empat penggerak push-pull yang dapat mengalirkan arus pada keluarannya sampai sebesar 2A tiap jalurnya. Masing-masing jalur dikendalikan oleh sebuah sebuah TTL yang kompatibel. Tegangan yang bisa dikendalikan untuk supply motor mencapai 36 V.

Pada skema rangkaian terlihat ada 8 buah dioda 2A (1N2002) yang dipasang dengan konfigurasi jembatan dioda pada tiap motor dc. Maksud dari pemasangan jembatan dioda ini adalah menghilangkan gelombang osilasi yang timbul akibat adanya beban induktif yaitu kumparan motor.

Pada kaki 1 dan 8 adalah kaki *Sensing Voltage*. Kaki ini akan mengendalikan besarnya arus beban. Dalam keadaan tidak terhubung ke ground, *tegangan sensing* ($V_{sensing}$) pada kaki ini sebesar 3 Volt. Agar motor dapat berputar, tegangan pada kaki 1 dan 8 harus sebesar 1 Volt sampai 2 Volt. Apabila diinginkan arus yang mengalir pada beban sebesar 2A (dari baterai 12V/3Ah), maka :

$$I = \frac{V_{sensing}}{Rs}$$

$$3 = \frac{2}{Rs}$$

$$Rs = \frac{2}{3}$$

$$Rs = 0{,}67\Omega$$

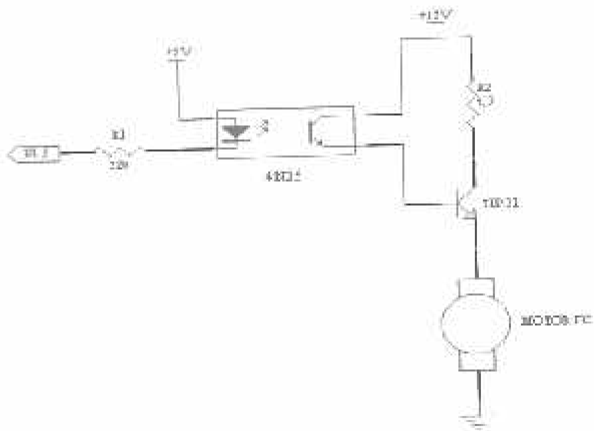
Tabel 3.1 Tabel Kebenaran IC L293D

INPUT		FUNGSI MOTOR
$VINH_2$ = H	A = H ; B = L	Motor 1 Berputar ke kanan
	A = L ; B = H	Motor 1 Berputar ke kiri
	A = B	Motor 1 Berhenti dengan cepat
$VINH_2$ = L	A = X ; B = X	Motor 1 Berhenti tanpa ada pengereman
$VINH_1$ = H	C = H ; D = L	Motor 2 Berputar ke kanan
	C = L ; D = H	Motor 2 Berputar ke kiri
	C = D	Motor 2 Berhenti dengan cepat
$VINH_1$ = L	A = X ; B = X	Motor 1 Berhenti tanpa ada pengereman

Keterangan :
H = High
L = Low
X = Don't Care

3.1.4. Rangkaian Driver Fan

Untuk perancangan driver Fan digunakan Optocoupler karena Fan disini disupply dengan tegangan 12V DC.



Gambar 3-5. Rangkaian Fan

Tegangan output maksimum dari Mikro adalah 5 V sedangkan untuk water pump memerlukan catu daya 12V DC,maka diperlukan rangkaian driver untuk mengendalikannya.Rangkaian driver yang dipakai berupa optocoupler 4N25 dan transistor type TIP31,untuk analisa data yang digunakan.:

Vin = 5 V (Max)

Data sheet untuk mengaktifkan 4N25:

V_F (tegangan forward dioda) = 1,5 Volt

I_{FT} (Arus forward Trigger) = 15 mA

Maka untuk mengaktifkan optocoupler R yang dipasang :

$$R = \frac{V_{in} - V_F}{I_{FT}}$$

$$R = \frac{5v - 1{,}5v}{15mA}$$

$$R = \frac{3{,}5v}{15mA}$$

$$R = 233\ \Omega$$

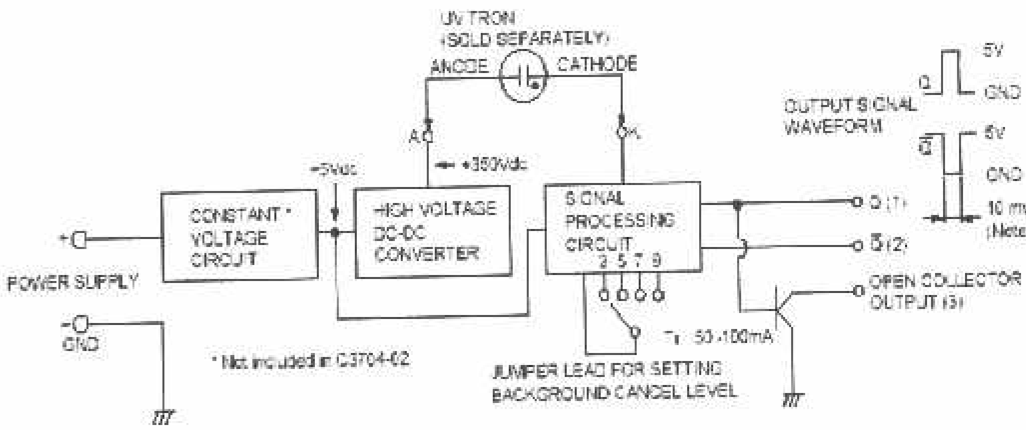
Nilai R yang mendekati dipasang 220 Ω

3.1.6. Detektor *Flame* UVtron

Tabung UVTron merupakan tabung yang bekerja ketika katoda diberikan sinyal ultraviolet, dimana fotoelektronakan dipancarkan darikatoda oleh efek fotoelektrik dan dipercepatke anoda menggunakan medan listrik. Ketika tegangan diberikan menyebabkansemakin meningkatnya dan medan listrik semakin besar, dan energi di tabung untuk bertubrukan. Elektron yang di bangkitkan oleh ionisasi dipercepat, menyebabkan mampu mengionisasi molekul lainya sebelum mencapai anoda. Ion positif yang dipercepat ke kejadian ini menyebabkan arus yang cukup besar diantara elektroda dan terjadi pembuangan muatan. Ketika terjadi pelepasan, tabung diisi dengan electron dan ion.

Pengaliranya terjadi hanya sekali, tabung yang dipenuhi atau di isi elektron dan ion. Tegangan yang menurun di antara anoda dan katoda dapat mengurangi sekali dari sumbernya. Kemampuan ini mempunyai keadaan dan sifat tanpa menurunkan tegangan anoda di ujung bawah titik jenuh.

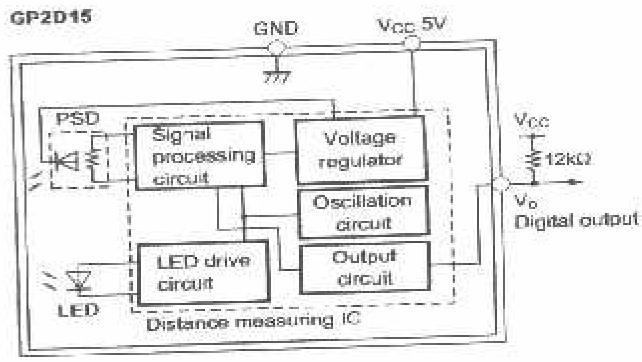
Untuk menciptakan atau membuat rangkaian yang berjalan berbeda tegangan diprlukan di dalam tabung yang di dalamnya memperbolekan proses pembuangan muatan ketika memberikan sinar ultrafiolet, menjaga arus keluaran dari rangkaian tabung dan ketika terjadi proses pembuangan muatan, maka membuat arus mengalir. Sekali terjadi pengaliran, tegangan anoda itu akan dikurangi oleh rangkaian yang berbentuk atau memperbolekan gelombang reset setiap waktu turun atau drop dan terjadi pengaliran atau yang dikeluarkan pulsa oleh rangkaian.



Gambar 3-6. Rangkaian detektor *Flame* UVtron

3.1.7 Sensor Infrared GP2D15

Sensor infrared GP2D15 adalah sensor jarak secara terus menerus, jarak yang di ukur di keluarkan sebagai suatu level logika. Ketika tidak ada jarak yang diukur atau tidak ada objek level outputan akan menunjukan logika low dan akan menjadi logika high ketika ada jarak yang diukur atau ada objek yang di deteksi dimana sensor ini diseting untuk range antara 5cm – 20cm.

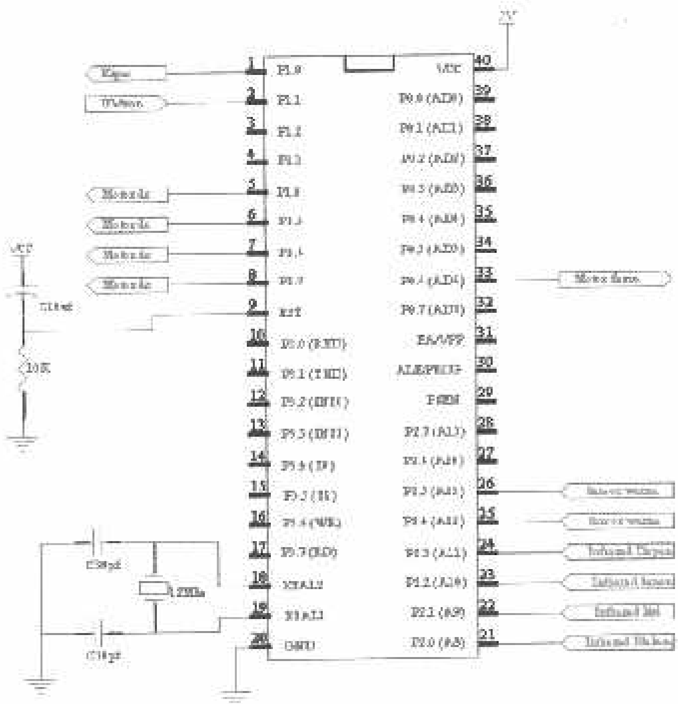


Gambar 3-7. Rangkaian Infrared GP2D15

Output dari sensor GP2D15 adalah *open collector* output ini berarti untuk mendapatkan logika yang dapat dideteksi ketika di hubungkan pada pin mikrokontroller perlu di tambahkan sebuah resisto pull up resistor ini harus berada pada range 10K – 20K.

3.1.8 Mikrokontroller (AT89S8252)

Mikrokontroler AT89S8252 digunakan sebagai Kontrol kerja dari system, masukan dari sensor diolah oleh mikrokontroller dan mikrokontroller mengatur kerjadari outputan, yaitu:



Gambar 3-8. Rangkaian Mikrokontroller Sistem

- P1.4 - P1.7 digunakan sebagai outputan mikrokontroller yaitu motor dc
- P0.6 digunakan sebagai outputan mikrokontroler untuk menggerakan motor servo.

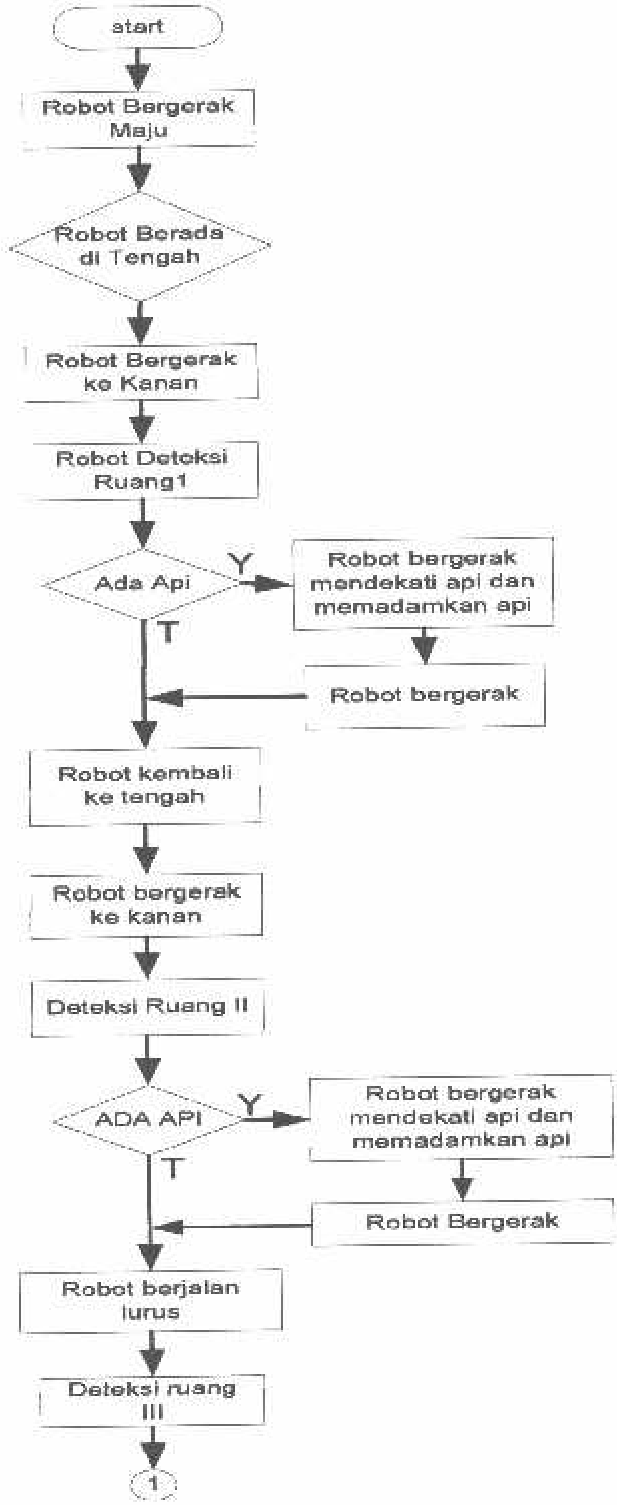
- P1.0 digunakan sebagai outputan untuk menjalankan FAN untuk memedamkan lilin.
- P1.1 digunakan sebagai inputan mikrokontroler yaitu sensorDetektor *Flame* Uvtron.
- P2.0 digunakan sebagai inputan mikrokontroler yaitu sensor infrared GP2D15 belakang.
- P2.1 digunakan sebagai inputan mikrokontroller yaitu sensor infrared GP2D15 kiri.
- P2.2 digunakan sebagai inputan mikrokontroller yaitu sensor infrared GP2D15 kanan.
- P2.3 digunakan sebagai inputan mikrokontroller yaitu sensor infrared GP2D15 depan
- P2.4 – P2.5 digunakan sebagai inputan mikrokontroller yaitu Sensor Infra merah (Sensor *Trackline*).

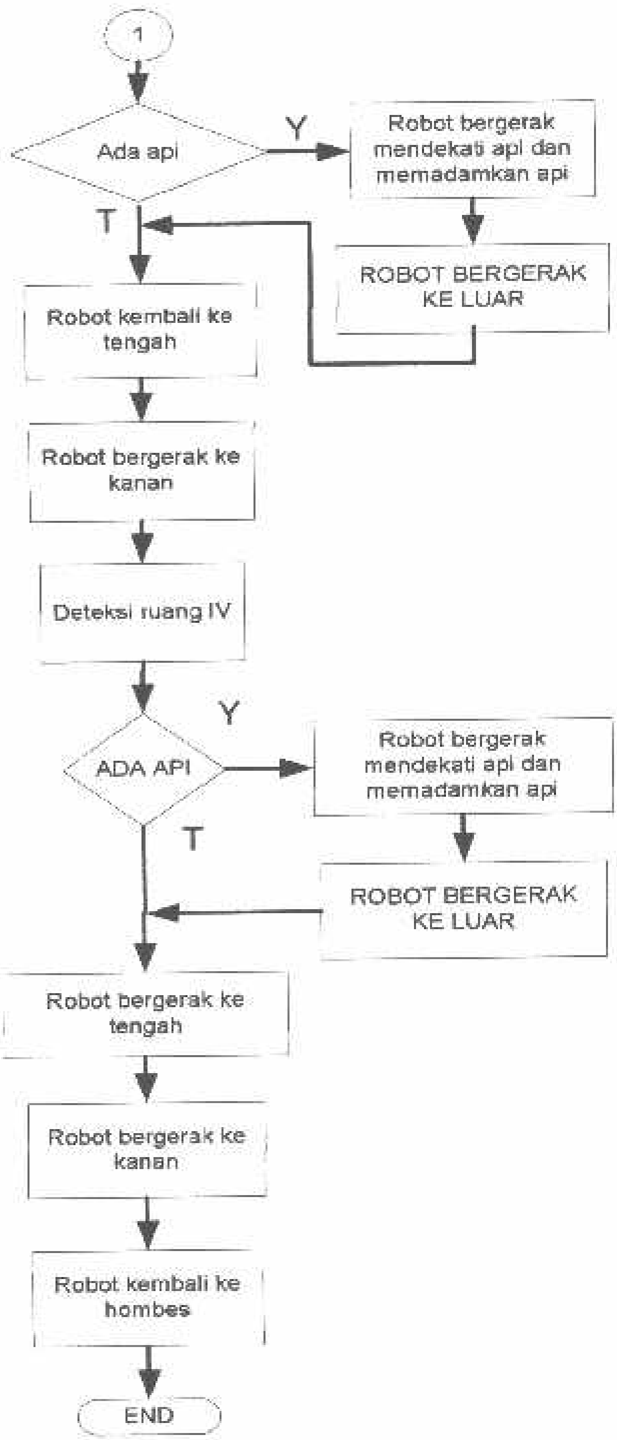
3.2. Perencanaan Perangkat Lunak (*Software*)

Untuk mendukung hardware yang sudah dibuat, maka dibutuhkan perangkat lunak (software) supaya perangkat keras tersebut bias berjalan sesuai dengan tujuan. Mikrokontroler dapat mengendalikan seluruh system apabila ada untaian instruksi yang mendefinisikan secara jelas urutan kerja yang harus dilaksanakan. Dalam perancangan alat ini perangkat lunak yang digunakan adalah bahasa pemrograman *assembler*.

Sebelum membuat perangkat lunak, terlebih dahulu dibuat diagram alir (*flowchart*) dari proses yang akan dibuat supaya memudahkan dalam pembuatan perangkat lunak (*software*).

3.2.1. Flowchart Sistem


start
Robot Bergerak Maju
Robot Berada di Tengah
Robot Bergerak ke Kanan
Robot Deteksi Ruang1
Ada Api
Y
T
Robot bergerak mendekati api dan memadamkan api
Robot bergerak
Robot kembali ke tengah
Robot bergerak ke kanan
Deteksi Ruang II
ADA API
Y
T
Robot bergerak mendekati api dan memadamkan api
Robot Bergerak
Robot berjalan lurus
Deteksi ruang III
1



Gambar 3.9. FlowChart Sistem

BAB IV

PENUJIAN ALAT

Dalam bab ini akan di bahas mengenai pengujian alat yang telah dibuat. Hal ini dapat dilakukan untuk mengetahui kekurangan kerja sistem yang telah dibuat, sehingga dapat diketahui apakah alat tersebut dapat bekerja sesuai dengan yang telah di rencanakan. Dalam rangka pengujian alat tersebut diuraikan percobaan yang telah di lakukan untuk mengetahui respon dari keseluruan alat yang telah dirancang.

4.1. Tujuan Pengujian

Tujuan pengujian yang dilakukan terhadap sistem aplikasi ini adalah sebagai berikut :

- Mengetahui unjuk kerja rangkaian sensor infra merah GP2D15
- Mengetahui unjuk kerja rangkaian driver motor DC.
- Mengetahui unjuk kerja rangkaian sensor Detektor Flame UVtron
- Mengetahui unjuk kerja rangkaian Photodioda (sensor trackline)

4.2. Alat-alat untuk pengujian

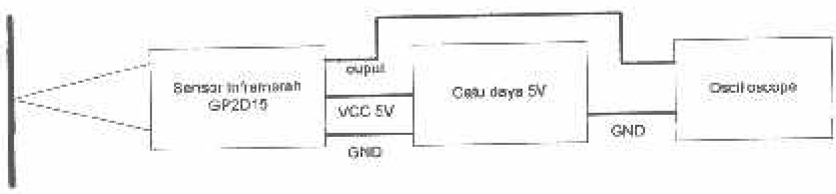
Alat-alat yang digunakan dalam pengujian adalah :

1. Oscilloscope
2. Multimeter Digital
3. Power suplay +5 Volt dan +12 Volt

4.3. Pengujian dan Pengukuran

4.3.1.Sensor Infra merah GP2D15

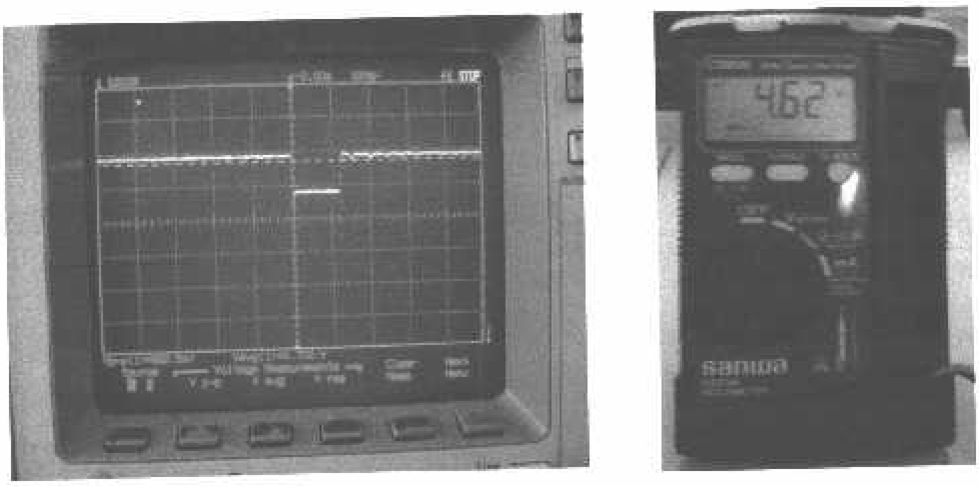
Metode pengujian dilakukan dengan cara memberikan tegangan pada sensor sebesar +5 Volt, dekatkan sensor pada dinding dan ukur jarak pancar sensor, kemudian ukur tegangan dan sinyal yang dihasilkan oleh sensor.



Gambar 4-1 Metode Pengujian Sensor GP2D15

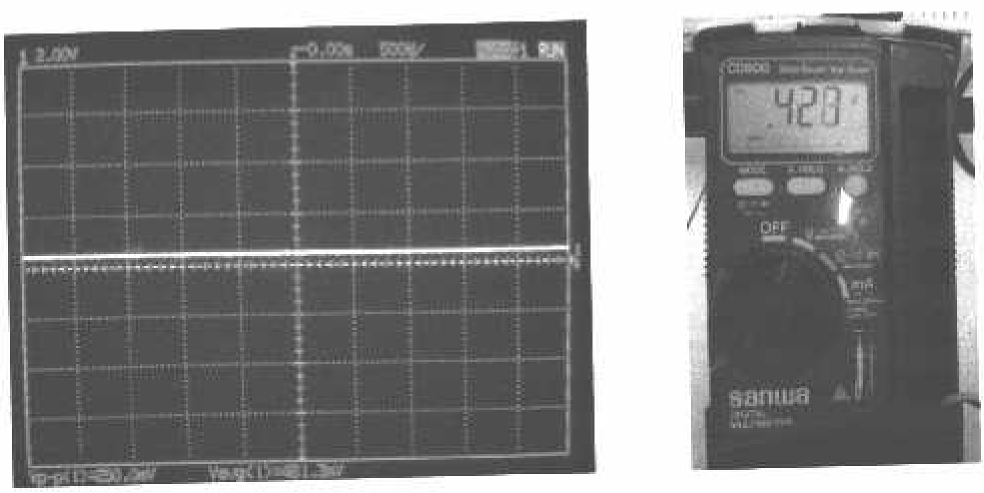
Jarak yang diukur sebagai suatu logika. Ketika tidak ada jarak yang diukur (tidak ada objek) level logika menunjukkan logika low dan akan menjadi logika high ketika ada jarak yang diukur (ada objek yang dideteksi) dimana dapat diseting pada range 5 – 20 cm.

Ouput dari GP2D15 adalah *open collector* output ini berarti untuk mendapatkan logika yang dapat dideteksi ketika dihubungkan pada pin mikrokontroler perlu di tambahkan sebuah resistor *pull up* resistor ini harus berada pada range 10 K – 20 K.



Gambar 4-2. Ouputan Sensor pada saat Terhalang

Ouputan sensor Inframerah pada saat terhalang akan mengeluarkan logika high dan ouput tegangan 4,6 Volt.

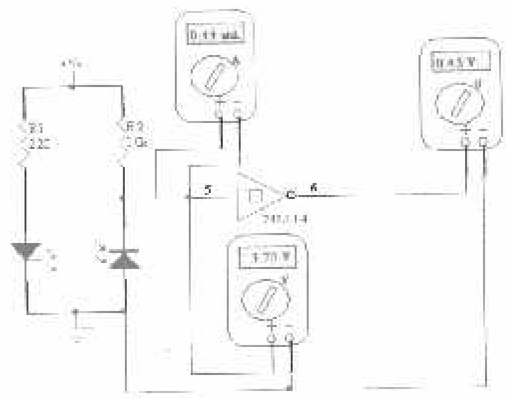


Gambar 4-3. Ouput Sensor Pada Saat tak Terhalang

Ouput sensor infra merah pada saat tak terhalang akan menghasilkan logika low dan output tegangan 0,42 Volt.

4.3.2.Pengujian Rangkaian Sensor Photodioda

Pengujian dilakukan dengan menghadapkan dioda infrared dan photodioda ke garis lintasan putih dahulu dengan jarak kira-kira 1,5 cm atau diatur lebih lanjut jaraknya sampai tegangan yang dihasilkan pada kaki katoda photodioda mendekati 4 Volt. Kemudian mencatat nilai tegangan dan arus pada masing-masing titik uji pada tabel. Pengujian dilakukan dengan cara yang sama pada garis lintasan berwarna hitam.



Gambar 4-4. Rangkaian Pengujian Sensor Photodioda

Tabel 4-1. Hasil Pengujian Tegangan Pada Garis Lintasan Putih

Tegangan (Volt)							
Photodioda 1		**Photodioda 2**		**Photodioda 3**		**Photodioda 4**	
Kaki Katoda	Output Inverter	Kaki Katoda	Output Inverter	Kaki Katoda	Output Inverter	Kaki Katoda	Output Inverter
0,98	5,15	0,31	5,15	0,96	5,15	0,89	5,15

Tabel 4-2. Hasil Pengujian Tegangan Pada Warna Hitam

Tegangan (Volt)							
Photodioda 1		Photodioda 2		Photodioda 3		Photodioda 4	
Kaki Katoda	Output Inverter	Kaki Katoda	Output Inverter	Kaki Katoda	Output Inverter	Kaki Katoda	Output Inverter
3,68	0,33	3,77	0,33	3,85	0,33	3,86	0,33

Tabel 4-3. Hasil Pengujian Arus Pada Garis Lintasan Hitam

Arus (mA)							
Photodioda 1		Photodioda 2		Photodioda 3		Photodioda 4	
Kaki Katoda	Output Inverter	Kaki Katoda	Output Inverter	Kaki Katoda	Output Inverter	Kaki Katoda	Output Inverter
0,44	0,01	0,45	0,01	0,43	0,01	0,43	0,01

Tabel 4-4. Hasil Pengujian Arus Pada Warna Hitam

Arus (mA)							
Photodioda 1		Photodioda 2		Photodioda 3		Photodioda 4	
Kaki Katoda	Output Inverter	Kaki Katoda	Output Inverter	Kaki Katoda	Output Inverter	Kaki Katoda	Output Inverter
0,198	0,482	0,221	0,496	0,220	0,487	0,237	0,488

Dari hasil pengukuran seperti pada gambar 4-1 dan gambar 4-2, dapat dianalisa besarnya tegangan keluaran pada photodioda 1 pada garis lintasan putih dengan menggunakan persamaan sebagai berikut :

$$Vcc = I_{PD}.R + Vout$$

$$5V = (0,44.10^{-3} * 10.10^{3}) + Vout$$

$$V_{OUT} = 5 - 4,44$$

$$Vout = 0,56Volt$$

Untuk pengujian sensor infra merah pada garis lintasan hitam seperti pada gambar 4-1 dan gambar 4-3, tegangan keluaran dapat dihitung dengan persamaan:

$$Vcc = I_{PD}.R + Vout$$

$$5V = (0,198.10^{-3} * 10.10^{3}) + Vout$$

$$V_{OUT} = 5 - 1,98$$

$$Vout = 3,02Volt$$

Dari *datasheet* tegangan keluaran dari *inverter schmitt trigger* akan mengeluarkan tegangan sebesar 3,4 volt jika tegangan pada inputnya sebesar 0,6 volt sampai 1,1 volt. Dan akan mengeluarkan tegangan sebesar 0,25 volt jika tegangan pada inputnya sebesar 1,5 volt sampai 2 volt.

Untuk perhitungan pada photodioda 2, photodioda 3 dan photodioda 4 dengan menggunakan persamaan yang sama akan didapatkan hasil perhitungan yang sama dengan hasil perhitungan pada photodioda 1. Berikut ini adalah tabel hasil perhitungan.

Tabel 4-5. Hasil Perhitungan Tegangan Pada Garis lintasan putih

Tegangan (Volt)							
Photodioda 1		Photodioda 2		Photodioda 3		Photodioda 4	
Kaki Katoda	Output Inverter	Kaki Katoda	Output Inverter	Kaki Katoda	Output Inverter	Kaki Katoda	Output Inverter
0,56	5	0,50	5	0,70	5	0,70	5

Tabel 4-6. Hasil Perhitungan Tegangan Pada Media Berwarna Gelap

Tegangan (Volt)							
Photodioda 1		Photodioda 2		Photodioda 3		Photodioda 4	
Kaki Katoda	Output Inverter	Kaki Katoda	Output Inverter	Kaki Katoda	Output Inverter	Kaki Katoda	Output Inverter
3,02	0	2,79	0	2,78	0	2,63	0

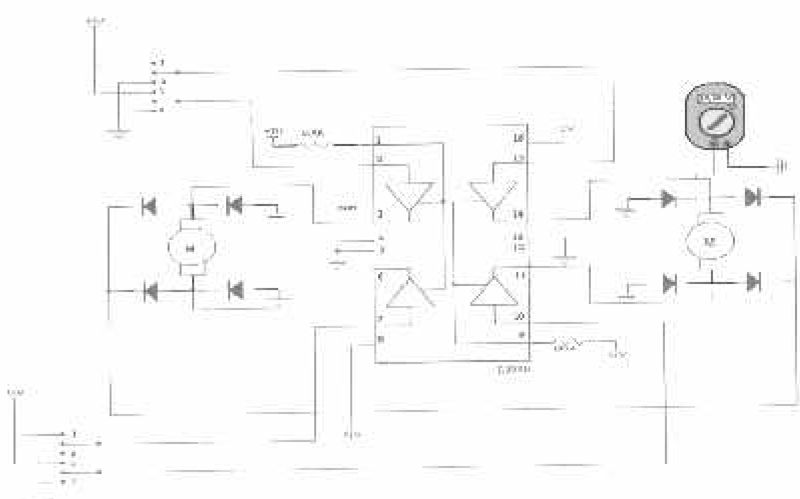
4.3.3.Pengujian Rangkaian Driver Motor

Pengujian rangkaian driver motor ini bertujuan untuk mengetahui apakah rangkaian ini dapat bekerja sebagaimana mestinya, yaitu dapat menggerakkan motor dengan arah yang bersesuaian dengan kombinasi masukannya.

Metode pengujian dilakukan seperti pada gambar. Pengujian dilakukan dengan memberi kombinasi logika pada inputan driver dan mengamati arah putaran motor DC pada keluarannya, serta mengukur tegangan pada keluaran driver.

Gambar 4.5 Metode Pengujian Rangkaian Driver Motor DC

Kombinasi logika diberikan pada masukan driver pada pin 2, 7, 10, 15. Pada masukan *Enable A* dan *Enable B* dihubungkan langsung ke +5 Volt. Kemudian diukur tegangan keluaran pada pin 3, 6, 11, 14, dan diamati arah putaran dari motor DC, lalu memasukkan hasil pengamatan pada tabel.



Gambar 4-6. Rangkaian Pengujian Driver Motor

Tabel 4-7. Hasil Pengujian Rangkaian Driver Motor

No.	INPUT						OUTPUT				UNIT
	A	B	C	D	VINH1	VINH2	Out 1	Out 2	Out 3	Out 4	
1.	0	0	0	0	1	0	0,76	0,78	-	-	V
2.	0	1	0	1	1	0	0,75	10,31	-	-	V
3.	1	0	1	0	1	0	10,31	0,78	-	-	V
4.	1	1	1	1	1	0	10,30	10,30	-	-	V
5.	0	0	0	0	0	1	-	-	0,78	0,77	V
6.	0	1	0	1	0	1	-	-	0,79	10,31	V
7.	1	0	1	0	0	1	-	-	10,31	0,78	V
8.	1	1	1	1	0	1	-	-	10,30	10,30	V

Keterangan :

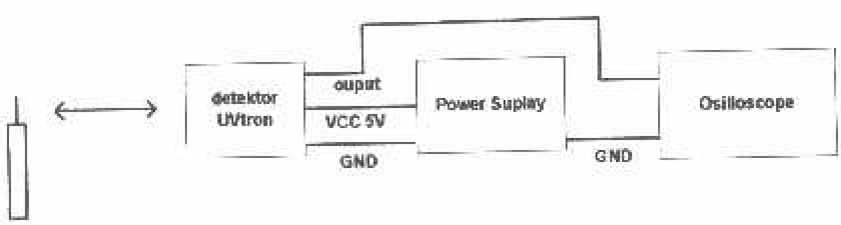
0 = *Low*

1 = *High*

- = Tidak ada tegangan

4.3.4.Pengujian Rangkaian Detektor *Flame* UVtron

Pengujian rangkaian Detektor *flame* UVtron ini bertujuan untuk mengetahui apakah rangkaian ini dapat bekerja sebagaimana mestinya, yaitu dapat mendeteksi nyala api lilin pada jarak yang diinginkan.

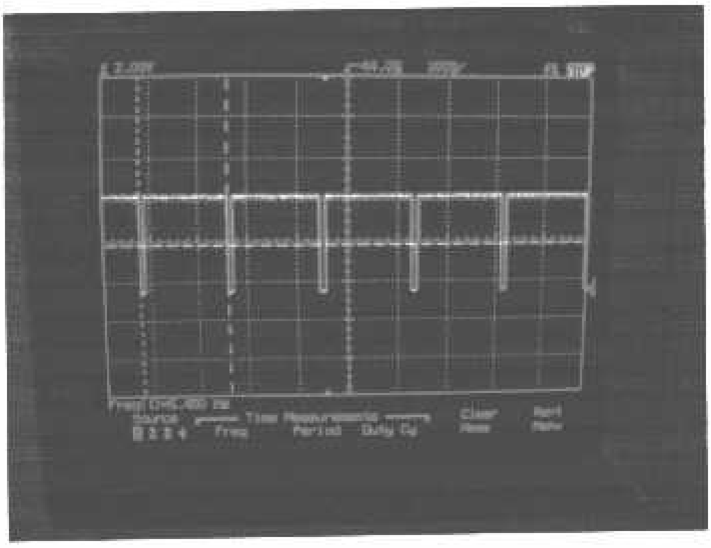


Gambar 4-7. Metode Pengujian Detektor *Flame* UVtron

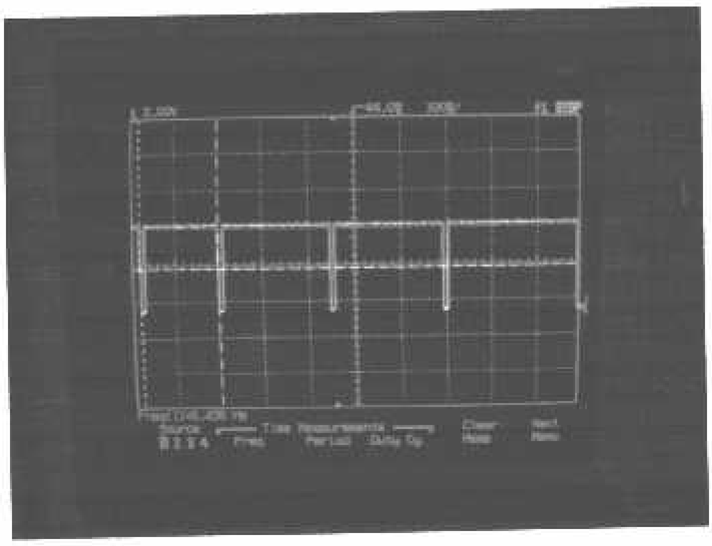
Pengujian dilakukan dengan cara memberikan tegangan +5 Volt pada modul rangkaian, dekatkan UVtron tersebut pada nyala lilin, lalu lihat outputan atau keluaran dari UVtron tersebut dengan menggunakan osilloscope lihat sinyal yang di hasilkan oleh UVtron tersebut, akan mengalami perubahan pada saat kita dekatkan UVtron tersebut dengan nyala api pada lilin. Dari hasil pengujian di dapatkan bahwa hasil ouputan UVtron adalah berupa Frekuensi yang mengikuti perubahan jarak cahaya api.

Tabel 4-8 Hasil Pengujian Rangkaian Detektor *Flame* UVtron

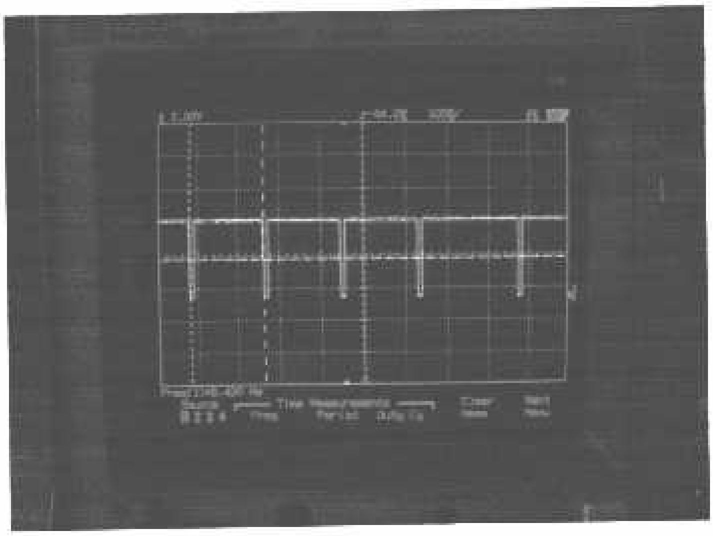
No	Jarak	Freg (HZ)
1	5 cm	5,450
2	10 cm	5,435
3	15 cm	5,420
4	20 cm	5,362
5	25 cm	5,319
6	30 cm	4,149
7	35 cm	4,132
8	40 cm	4,115
9	45 cm	4,090
10	50 cm	4,082
11	55 cm	4,073
12	60 cm	4,065
13	65 cm	4,040
14	70 cm	4,016
15	75 cm	3,527
16	80 cm	3,413
17	85 cm	3,311
18	90 cm	3,226
19	95 cm	3,180
20	1 m	3,145
21	1,5 m	2,721
22	2 m	2,328
23	2,5 m	2,006
24	3 m	1,972
25	3,5 m	1,671
26	4 m	1,571



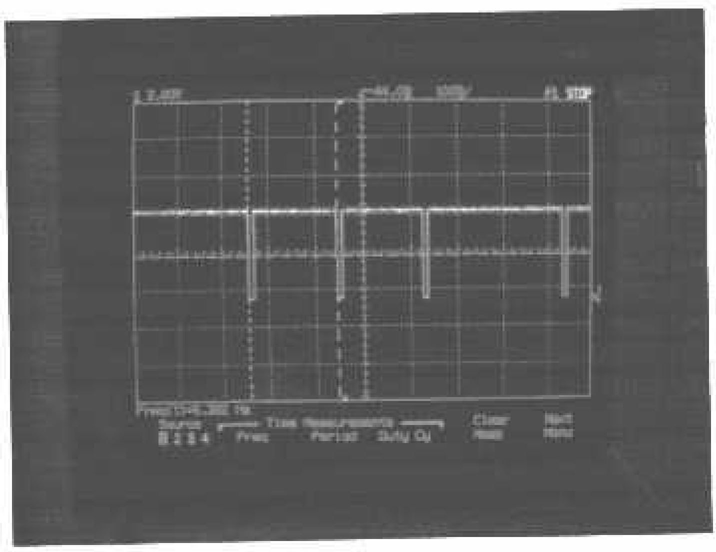
Gambar 4-8. Hasil Pengujian UVtron pada Jarak 5cm



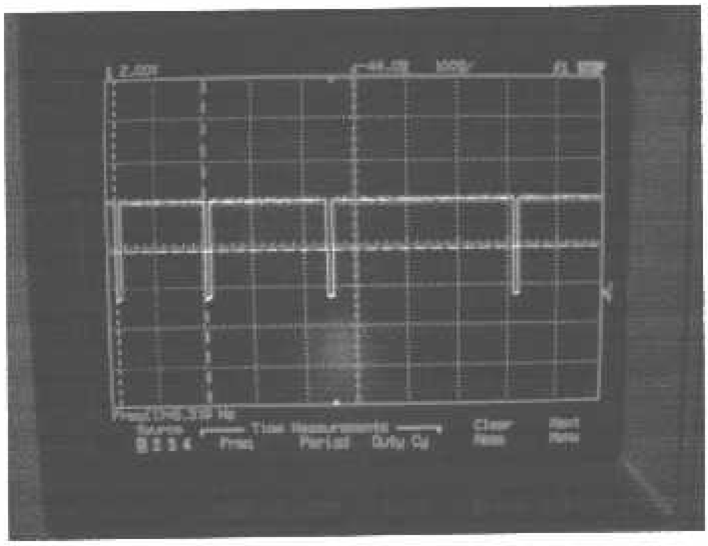
Gambar 4-9. Hasil Pengujian UVtron pada Jarak 10cm



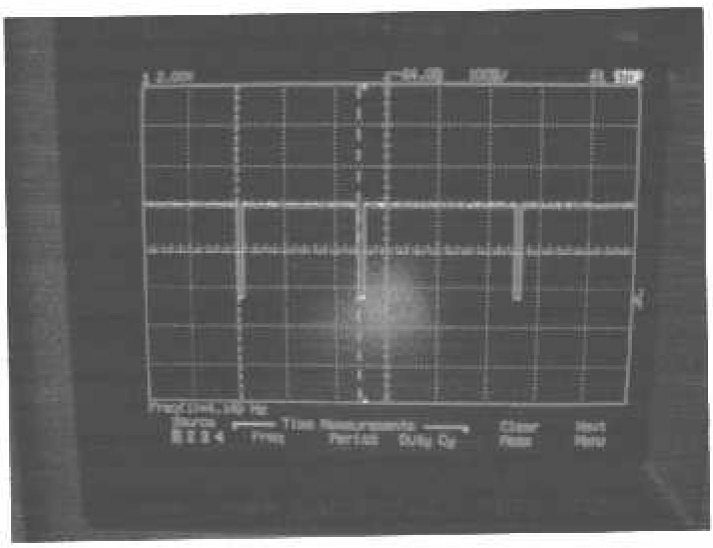
Gambar 4-10. Hasil Pengujian UVtron pada Jarak 15cm



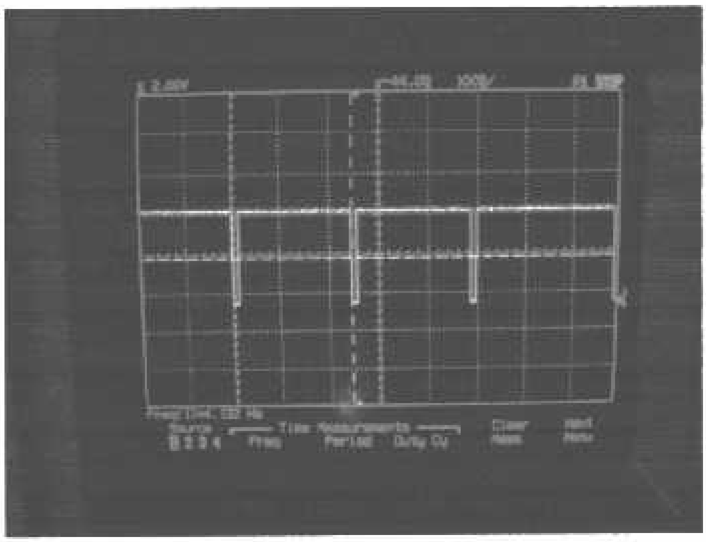
Gambar 4-11.Hasil Pengujian UVtron pada Jarak 20cm



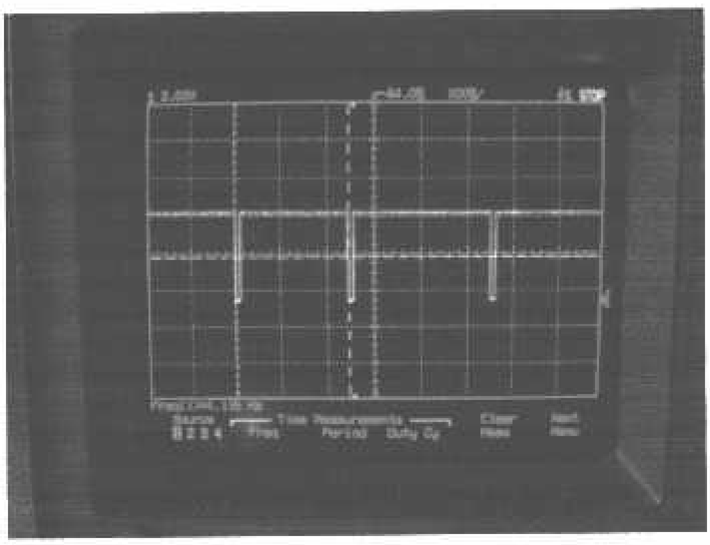
Gambar 4-12.Hasil Pengujian UVtron pada Jarak 25cm



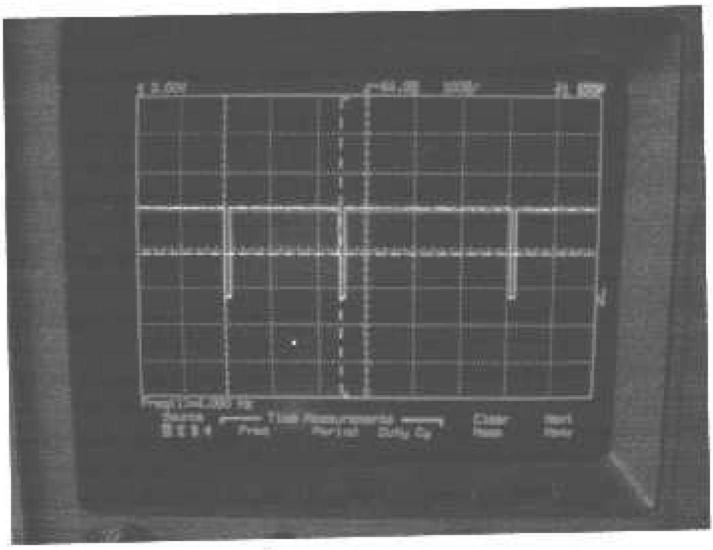
Gambar 4-13. Hasil Pengujian UVtron pada Jarak 30cm



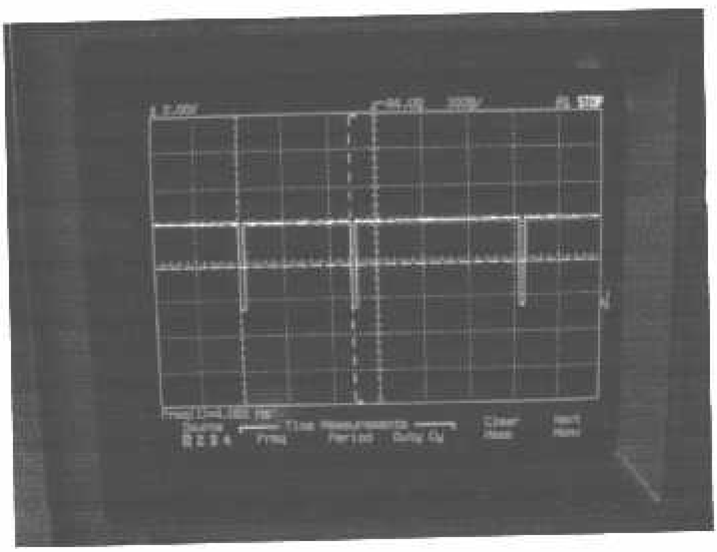
Gambar 4-14. Hasil Pengujian UVtron pada Jarak 35cm



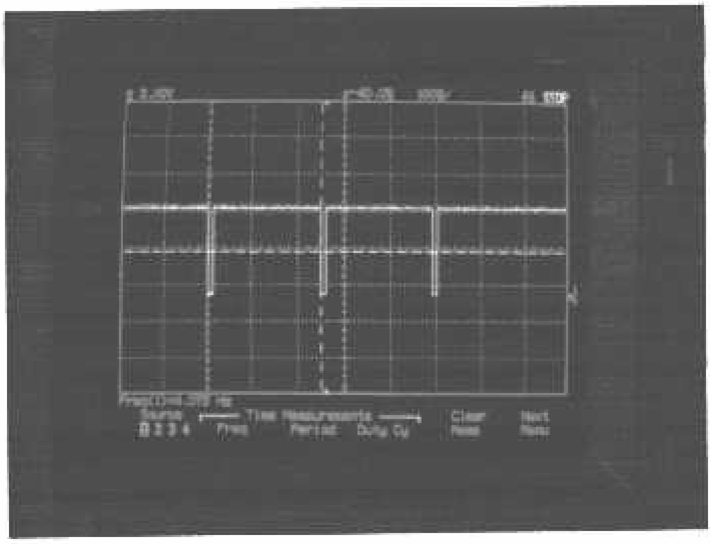
Gambar 4-15.Hasil Pengujian UVtron pada Jarak 40cm



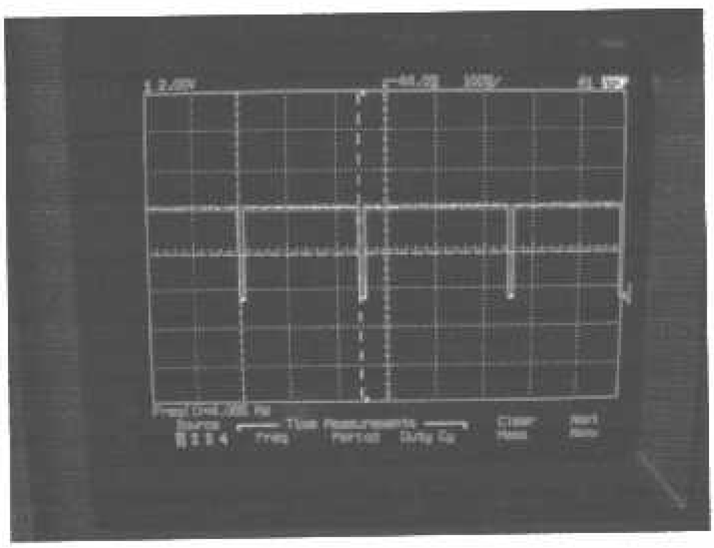
Gambar 4-16. Hasil Pengujian UVtron Pada Jarak 45cm



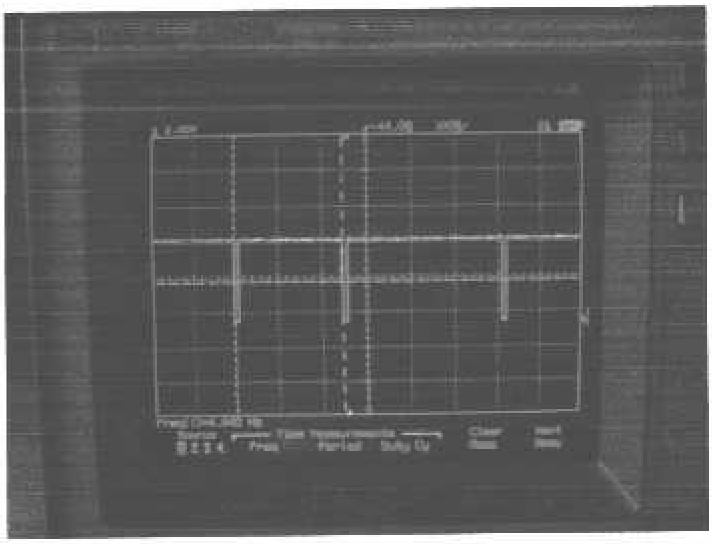
Gambar 4-17. Hasil Pengujian UVtron Pada Jarak 50cm



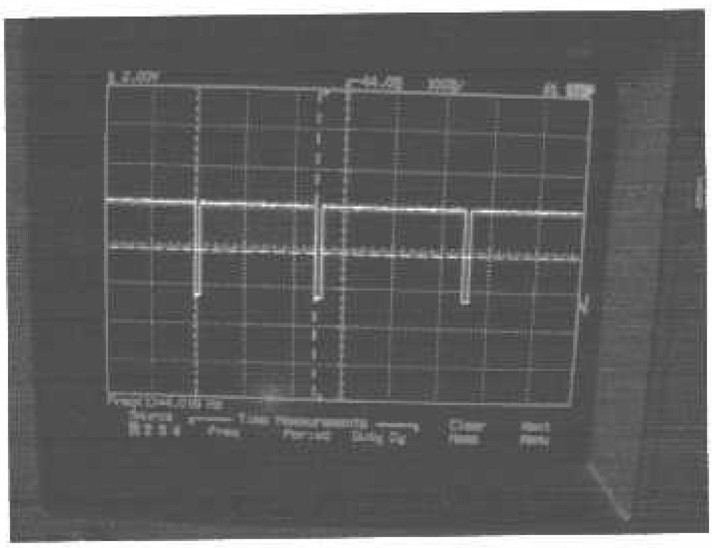
Gambar 4-18. Hasil Pengujian UVtron Pada Jarak 55cm



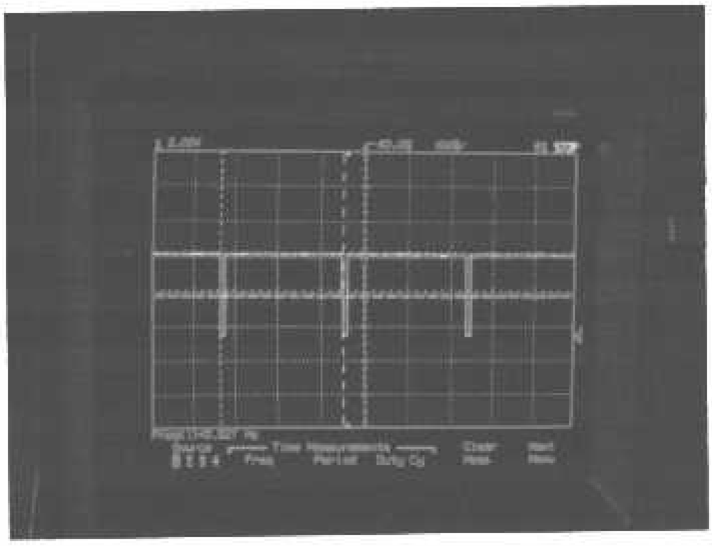
Gambar 4-19. Hasil Pengujian UVtron Pada Jarak 60cm



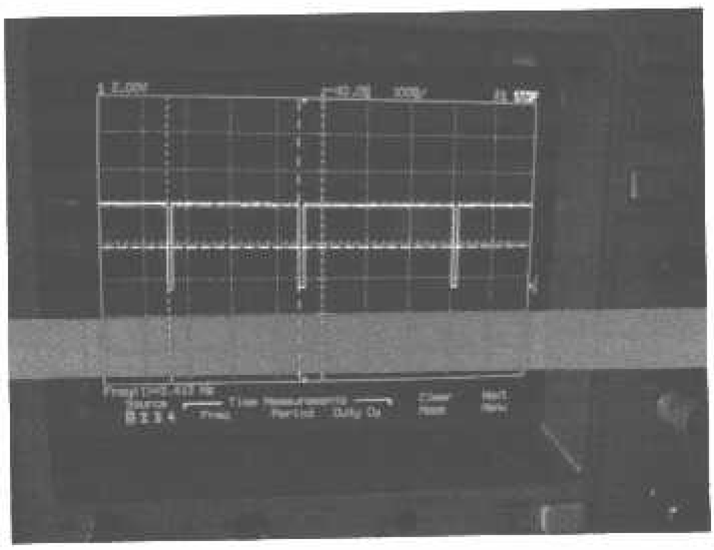
Gambar 4-20. Hasil Pengujian UVtron Pada Jarak 65cm



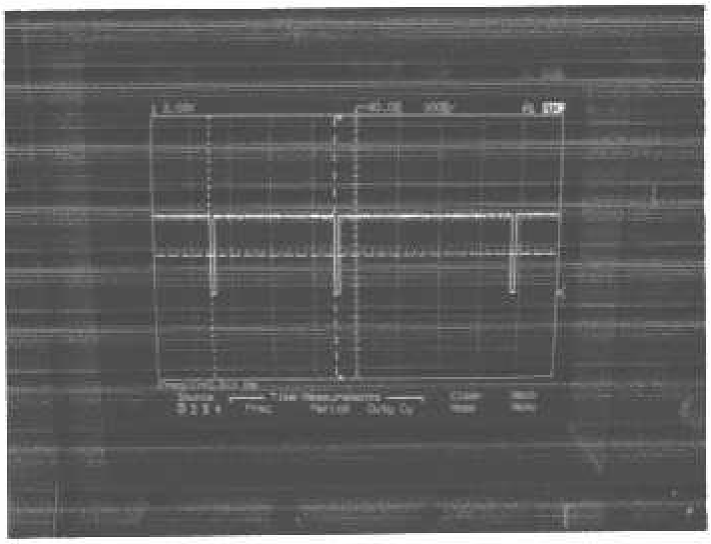
Gambar 4-21. Hasil Pengujian UVtron Pada Jarak 70cm



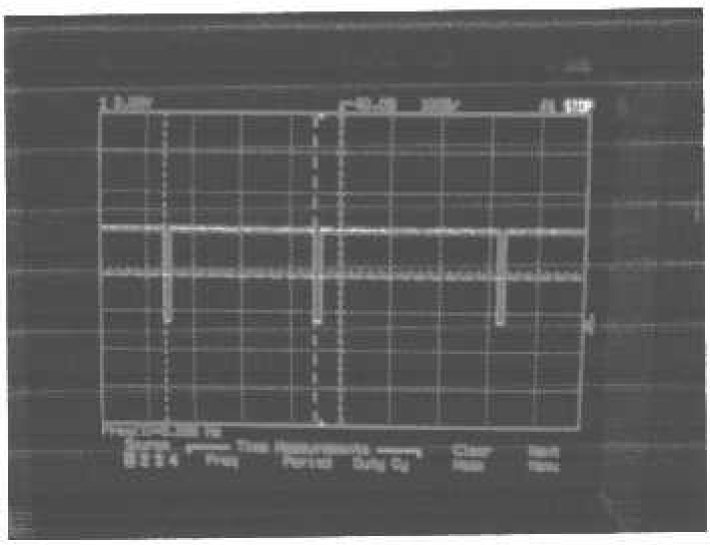
Gambar 4-22. Hasil Pengujian UVtron Pada Jarak 75cm



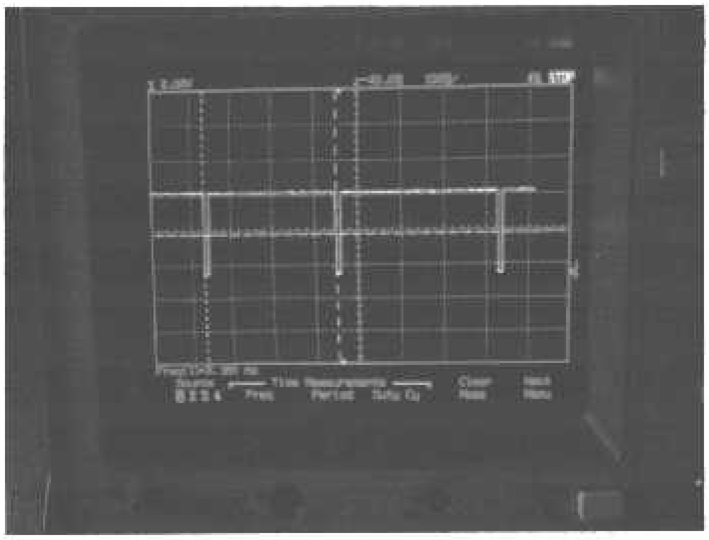
Gambar 4-23. Hasil Pengujian UVtron Pada Jarak 80cm



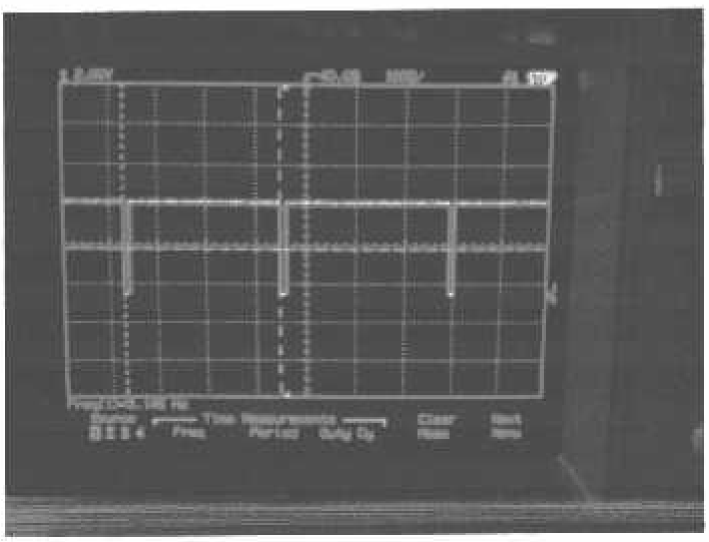
Gambar 4-24. Hasil Pengujian UVtron Pada Jarak 85cm



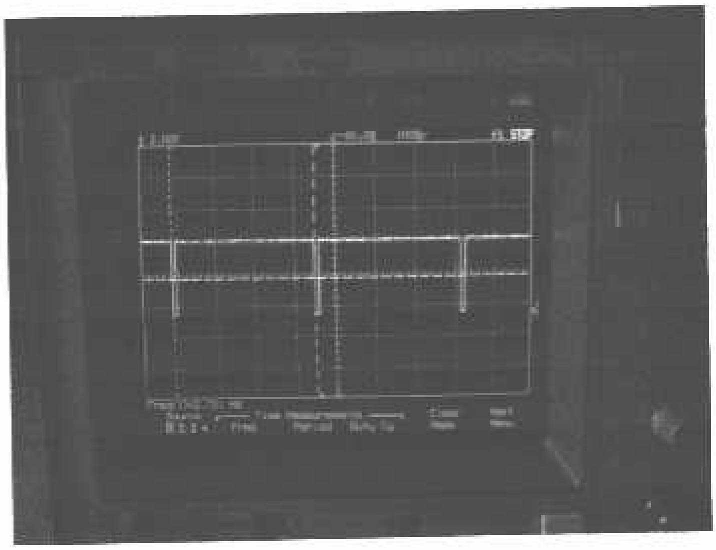
Gambar 4-25. Hasil Pengujian UVtron Pada Jarak 90cm



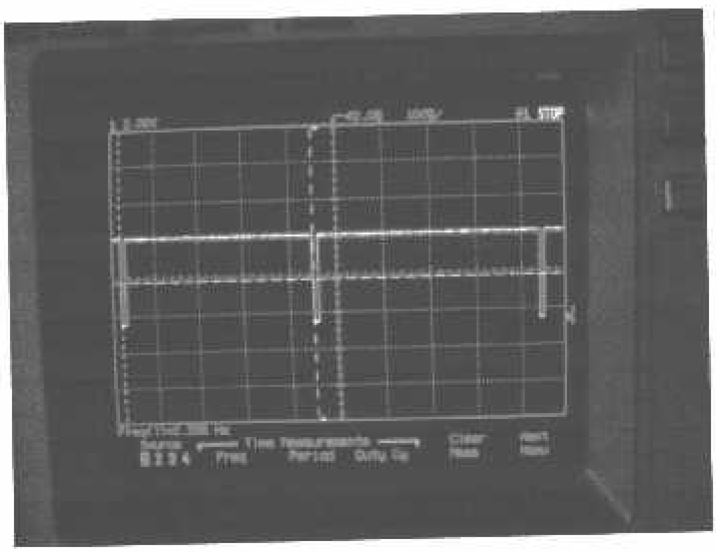
Gambar 4-26. Hasil Pengujian UVtron Pada Jarak 95cm



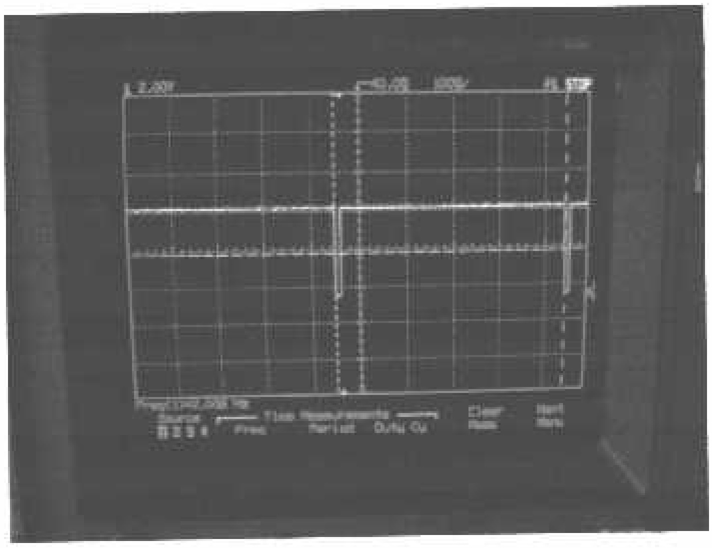
Gambar 4-27. Hasil Pengujian UVtron Pada Jarak 1M



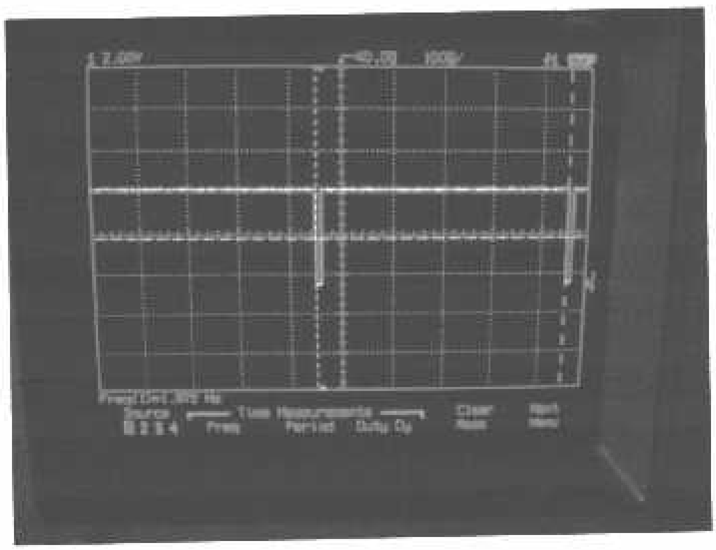
Gambar 4-28. Hasil Pengujian UVtron Pada Jarak 1,5M



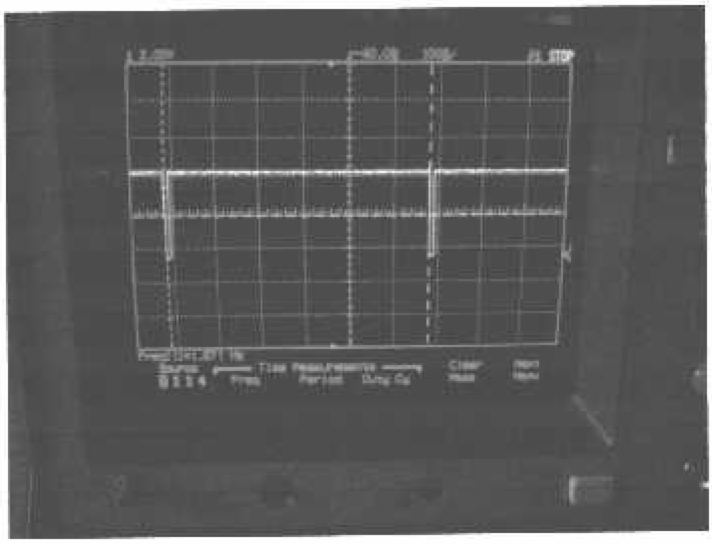
Gambar 4-29. Hasil Pengujian UVtron Pada Jarak 2M



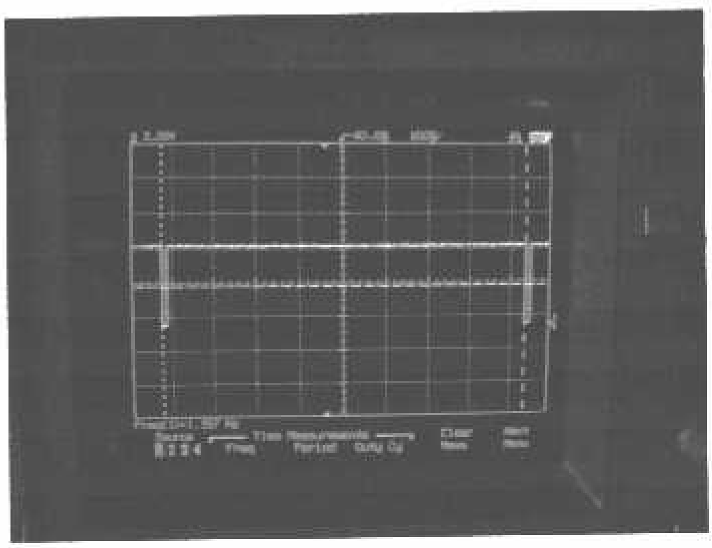
Gambar 4-30. Hasil Pengujian UVtron Pada Jarak 2,5M



Gambar 4-31. Hasil Pengujian UVtron Pada Jarak 3M



Gambar 4-32. Hasil Pengujian UVtron Pada Jarak 3,5M



Gambar 4-33. Hasil Pengujian UVtron Pada Jarak 4M

BAB V

PENUTUP

5.1 Kesimpulan

Selama dalam perencanaan dan pengujian dari keseluruhan sistem yang telah di buat maka dapat ditarik beberapa kesimpulan antara lain:

1. Dari hasil pengujian, dengan menggunakan batrai sebesar 300ma dengan tegangan 12 dan 5V mampu menjalankan robot dari start berjalan mencari api dan memadamkan, pada ruangan sampai kembali ke start lagi catudaya ini bertahan selama 10 menit.
2. Waktu yang diperlukan robot untuk memadamkan api pada saat sensor menemukan sumber api selama 10 detik
3. Dari hasil pengujian, dengan menggunakan sensor infrared object detector GP2D15 sebagai sensor jarak, robot mampu melewati lorong tanpa tanpa menyentu atau menabrak dinding tembok.
4. Dar hasil pengujian, dengan menggunakan Detector FlameUVtron.UVtron ini mampu mendeteksi api pada lilin sejauh 4 meter, dari UVtron hingga ke pusat titik api
5. Dari 20 kali percobaan ada 1 kali robot tidak dapat memadamkan api dikarenakan kurangnya tegangan, karena konsomsi daya potensial degan ukuran waktu (mAH).

5.2. Saran – Saran

Untuk meningkatkan kepresisian dari alat yang dibuat serta mencapai hasil yang mendekati sempurna hendaknya perlu di tambahkan sensor kompas agar robot dapat menentukan sudut yang di inginkan. Dan bisa tambahkan sensor suara agar robot dapat mendeteksi suara pada ruangan, kemudian bisa dikembangkan lagi misalnya dengan memperbanyak titik api pada ruangan.

DAFTAR PUSTAKA

- Sharp Data Sheet, http:// www.sharpusa.com
- Hamamatsu Corp., http:// www.hamamatsu.com
- Fairchild Data Sheet, http:// www.fairchildsemi.com
- Trinity College Home Fire Fighting Robot Hompage:

  http:// www.trincoll.edu/events/robot
- JAMECO Elcktronic, http://www.jameco.com
- www.digi_ware.com
- Mikrokontroler Data Sheet, http:// www.data sheet.com
- Widodo Budiharto, BELAJAR SENDIRI MEMBUAT

  ROBOT CERDAS, Penerbit PT Elex media komputindo
- http://www.Delta–electronic.com

FORMULIR PERBAIKAN SKRIPSI

Dalam pelaksanaan Ujian Skripsi Jenjang Strata Satu (S-1) Jurusan Teknik Elektro Konsentrasi Teknik Elektronika, maka perlu adanya perbaikan skripsi untuk mahasiswa :

Nama : Hijriyah Irawan
NIM : 02 17 012
Jurusan : Teknik Elektro S-1
Konsentrasi : Teknik Elektronika
Masa Bimbingan : 5 Oktober 2006 s/d 5 Aprel 2007
Judul Skripsi : Perencanaan Dan Pembuatan Robot Cerdas Pemadam Api Berbasis Mikrokontroller.

Tanggal	Uraian	Paraf
17 Maret 2007	❖ Buat Skema Rangkaian Lengkap	
	❖ Jelaskan Mekanisme Mikro dalam Menangkap data UVtron	
	❖ Buat Pengujian Tentang Intensitas Api Terhadap Keluaran UVtron	
	❖ Jelaskan Lup Api Mengeluarkan UV	

Mengetahui,

Dosen Pembimbing I

(Ir. Sidik Noertjahjono, MT)
NIP.1028700167

Dosen Pembimbing II

(M.Ashar, ST , MT)
NIP.

Dosen Penguji,

(DR. Cahyo Crysdian, Msc)
NIP.1030400412

INSTITUT TEKNOLOGI NASIONAL
FAKULTAS TEKNOLOGI INDUSTRI
JURUSAN TEKNIK ELEKTRO S-1
Jl. Karanglo KM. 2 Malang

FORMULIR PERBAIKAN SKRIPSI

Dalam pelaksanaan Ujian Skripsi Jenjang Strata Satu (S-1) Jurusan Teknik Elektro Konsentrasi Teknik Elektronika, maka perlu adanya perbaikan skripsi untuk mahasiswa :

Nama : Hijriyah Irawan
NIM : 02 17 012
Jurusan : Teknik Elektro S-1
Konsentrasi : Teknik Elektronika
Masa Bimbingan : 5 Oktober 2006 s/d 5 Aprel 2007
Judul Skripsi : Perencanaan Dan Pembuatan Robot Cerdas Pemadam Api Berbasis Mikrokontroller.

Tanggal	Uraian	Paraf
17 Maret 2007	❖ FlowChart	
	❖ Rangkaian Sekematik Lengkap	
	❖ Analisa Lagi UVtron Bukan PWM Melainkan Intensitas Cahaya UV Mengikuti Perubahan Frekuensi	

Mengetahui,

Dosen Pembimbing I

(Ir. Sidik Noertjahjono, MT)
NIP.1028700167

Dosen Pembimbing II

(M.Ashar, ST , MT)
NIP.

Dosen Penguji,

(I Komang Somawirata, ST, MT)
NIP.P.1030100361

LAMPIRAN

INSTITUT TEKNOLOGI NASIONAL MALANG
FAKULTAS TEKNOLOGI INDUSTRI
JURUSAN TEKNIK ELEKTRO

FORMULIR BIMBINGAN SKRIPSI

Nama : HIJRIYAH IRAWAN
Nim : 02.17.012
Masa Bimbingan : 5 Oktober 2006 s/d 5 April 2007
Judul Skripsi : **PERENCANAAN DAN PEMBUATAN ROBOT CERDAS PEMADAM API BERBASIS MIKROKONTROLLER ATmega32**

No.	Tanggal	Uraian	Paraf
1.	24/9 06.	Konsultasi judul, siapkan rancangan berupa blok diagram	[signature]
2.	2/10 06.	Rencanakan agar tepat sensor panas (utk api saja) yg. digunakan.	[signature]
3.	10/10 06.	Ukur kepastian sensor panas berupa UVtron, jarak & suhunya.	[signature]
4.	22/10 06	Bab IV, dari rancangan lakukan pengukuran² pd. response sensor²	[signature]
5.	29/10 06.	Bab IV, ukur kemampuan software dlm. fungsi sbg. kecerdasan buatan.	[signature]
6.	12/11 06	Bab V, simpulkan apakah benar Robot yg. dibuat bg. kecerdasan.	[signature]
7.	24/11 06.	Bab III, dlm. perancangan, pertegas fungsi kecerdasan buatan.	[signature]
8.	2/12 06	Bab II, Bahasan ttg sensor panas dipertegas hanya pd. panas api!	[signature]
9.	29/2 07	Bab I, Permasalah & batasan masalah di perjelas	[signature]
10.	5/3 07.	Lap. skripsi disetujui, siapkan ujian komprehensive.	[signature]

Malang,
Dosen Pembimbing I

[signature] 10/3 07.

Ir. Sidik Noertjahjono, MT
NIP. 1028700167

Form.S-4b

INSTITUT TEKNOLOGI NASIONAL
FAKULTAS TEKNOLOGI INDUSTRI
JURUSAN TEKNIK ELEKTRO

Formulir Perbaikan Ujian Skripsi

Dalam pelaksanaan Ujian Skripsi Janjang Strata 1 Jurusan Teknik Elektro Konsentasi T. Energi Listrik / T. Elektronika, maka perlu adanya perbaikan skripsi untuk mahasiswa :

NAMA : HIJRIYAH IRAWAN
NIM : 02.17.012
Perbaikan meliputi :

1) Flow Chart

2) Rangkaian Schematic Lengkap.

3) Analisa Logic LED dan Sensor. antara PWM melakukan intensitas cahaya LED ~~[illegible]~~ mengikuti perubahan frekuensi

Malang, 13/3 - '07

[illegible] S.MT.

INSTITUT TEKNOLOGI NASIONAL
FAKULTAS TEKNOLOGI INDUSTRI
JURUSAN TEKNIK ELEKTRO

Formulir Perbaikan Ujian Skripsi

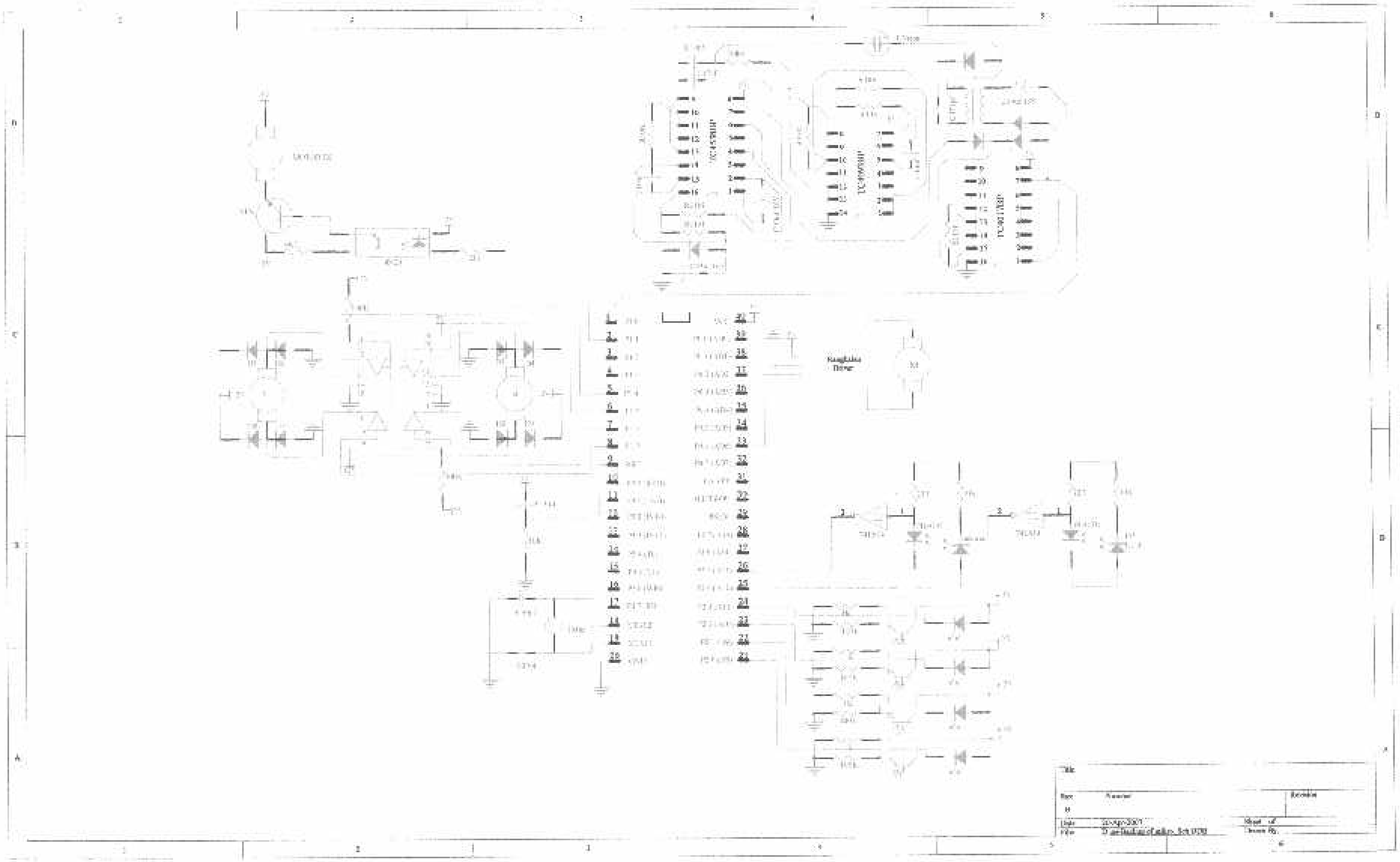
Dalam pelaksanaan Ujian Skripsi Janjang Strata 1 Jurusan Teknik Elektro Konsentasi T. Energi Listrik / T. Elektronika, maka perlu adanya perbaikan skripsi untuk mahasiswa :

NAMA : HIJRIYAH IRAWAN
N I M :
Perbaikan meliputi :

1) Buat skema rangkaian lengkap.
2) Jelaskan mekanisme alat dlm mengukur data UV & UV [illegible]
3) Buat pengujian ttg [illegible] cepat thd sensor UV.
4) Jelaskan [illegible] api mengeluarkan UV.

Malang,

(Dr. Cahyo Crysdian, MSc.)



Title
Size
Number
Revision
Date
File
Sheet of
Drawn By

2. Jelaskan mekanisme mikrokontroller dalam menangkap data UV dari Uvtron adalah:

Tabung UVTron merupakan tabung yang bekerja ketika katoda diberikan sinyal ultraviolet, dimana fotoelektronakan dipancarkan dari katoda oleh efek fotoelektrik dan dipercepatke anoda menggunakan medan listrik. Ketika tegangan diberikan menyebabkan semakin meningkatnya dan medan listrik semakin besar, dan energi di tabung untuk bertubrukan. Elektron yang di bangkitkan oleh ionisasi dipercepat, menyebabkan mampu mengionisasi molekul lainya sebelum mencapai anoda. ion positif yang dipercepat ke kejadian ini menyebabkan arus yang cukup besar diantara elektroda dan terjadi pembuangan muatan. Ketika terjadi pelepasan, tabung diisi dengan electron dan ion.

Pengaliranya terjadi hanya sekali, tabung yang dipenuhi atau di isi elektron dan ion. Tegangan yang menurun di antara anoda dan katoda dapat mengurangi sekali dari sumbernya. Kemampuan ini mempunyai keadaan dan sifat tanpa menurunkan tegangan anoda di ujung bawah titik jenuh.

Untuk menciptakan atau membuat rangkaian yang berjalan berbeda tegangan diprlukan di dalam tabung yang di dalamnya memperbolekan proses pembuangan muatan ketika memberikan sinar ultrafiolet, menjaga arus keluaran dari rangkaian tabung dan ketika terjadi proses pembuangan muatan, maka membuat arus mengalir. Sekali terjadi pengaliran, tegangan anoda itu akan dikurangi oleh rangkaian yang berbentuk atau memperbolekan gelombang reset setiap waktu turun atau drop dan terjadi pengaliran atau yang dikeluarkan pulsa digital oleh rangkaian.

Outputan yang dihasilkan rangkaian Uvtron berupa pulsa digital ouputan tersebut dimasukan ke mikrokontroller pada port P1.0.sinyal yang diterima mikrokontroller akan di counter:

Tunggu logika Uvtron : Low

Jika Logic : Low maka tunggu logika Uvtron : high

Jika logic : high

Cek Logic : Low, jika tidak ulang

Pulsa selama high : jika ya, keluar

Banding data : tiup (nyalakan kipas) atau tidak tiup (matikan kipas)

Cara membandikan :

Mov A , # Counter

Mov B , A

Div AB

Contoh program untuk menjalankan Uvtron :

```
bc_sns:  mov     Cnt0,#255         ;set counter maximum
         mov     Cnt1,#0           ; reset counter
         mov     Tmot,#255         ;\
bcsns0:  jb      Uvtr,bcsns1       ; | set time out
         sjmp    bcsns2            ; |tunggu sensor low
bcsns1:  acall   jeda
         djnz    Tmot,bcsns0       ; |tidak low-lompat
         sjmp    bcsns6            ;/
bcsns2:  jnb     Uvtr,$            ; tunggu sensor high
         mov     Tmot,#255         ;\
bcsns3:  acall   dlyuvt            ;   |delay   counter
uvtron
         inc     Cnt1              ; |
         jb      Uvtr,bcsns4       ; | set time out
         sjmp    bcsns7            ; |tunggu sensor low
bcsns4:  djnz    Tmot,bcsns5         |tidak low-lompat
         sjmp    bcsns6            ;/
bcsns5:  djnz    Cnt0,bcsns3
bcsns6:  mov     Cnt1,#255
bcsns7:  acall   cekbts
```

```
        ret
;
cekbts: mov     A,Cntl
        mov     B,#150 ; batas minimum peniupan 65
        div     AB
        cjne    A,#0,ckbts
        acall   meniup
ckbts:  setb    Tfin
        ret
;
meniup: clr     Tfin
        acall   delayl
        ret
```

4. proses api mengeluarkan sinar UV atau ultraviolet :

- **Teori Api**

  Api adalah reaksi kimia eksotermik yang disertai timbulnya panas atau kalor, cahaya (nyala), asap dan gas dan bahan yang terbakar. Proses ini dinamakan reaksi pembakaran.

- **Reaksi pembakaran di klasifikasikan sebagai:**

  Reaksi pembakaran kimia, termasuk senyawa organic (senyawa yang mengandung gugus karbon)

- **Senyawa Karbon + O2 – CO2 + H2O + panas + cahaya**

  Reaksi sederhana ataus empurna; misalnya antara gas methan (CH4) dengan oksigen, menghasilkan air dan karbon dioksida. Reaksi ini disebut sempurna karena satu molekul methane memerlukan 2 molekul oksigen (tercukupi)

  CH4 + O2 – CO2 + 2H20 + panas + cahaya.

- **Reaksi Pembakaran Tidak Sempurna Karena Oksigen tidak Tercukupi:**

  Senyawa karbon + O2 – CO2 + CO + C + H2O + panas + cahaya.

  Terjadinya Api Memerlukan tiga (3) Unsur Pembakaran Api Yaitu Bahan Bakar, Panas dan oksigen.

  1. **Bahan Bakar:**

     Bahan baker adalah materi atau zat yang selurunya atau sebagaian mengalami perubahan kimia dan fisika bila terbakar. Dapat berentuk padat, cair atau gas.

2. **Panas :**

Panas merupakan tingkatan energi bahan untuk terbakar pada suhu bakarnya, yakni suhu terendah saat bahan mulai terbakar. Disebut juga sebagai temperatur penyulutan *(ignition temperature)*.

3. **Oksigen :**

Oksigen adalah unsure kimia pembakaran (± 20% dari udara).

- **Reaksi Rantai Pembakaran**

Reaksi rantai menunjukkan suatu proses pembakaran yang berkesinambungan. Api yang timbul pada saat bahan baker akan memanaskan dan menaikan suhu baker pada bahan lainnya, sehingga menyebabkan benda – benda disekitarnya turut terbakar.

- **Ultraviolet**

Sinar ultraviolet adalah termasuk cahaya monokromatis yang tidak tampak oleh mata manusia. Spektrum frekuensi cahaya secara umum dibagi menjadi empat bagian yaitu :

a. *Ultraviolet*

b. Cahaya tampak (*visible light*)

c. Inframerah

d. *Microwaves*

Gambar Letak Spektrum Gelombang Ultraviolet

Gelombang elektromagnetik merupakan penyusun dari cahaya yang berada dalam spektrum elektromagnetik yang mempunyai jangkauan sangat lebar. Pada jarak yang sama, seluruh spektrum elektomagnetik tersebut mempunyai kecepatan yang sama tetapi frekuensinya berbeda sesuai dengan panjang gelombangnya.

Dalam hal ini berlaku :

$$c = \lambda . f$$

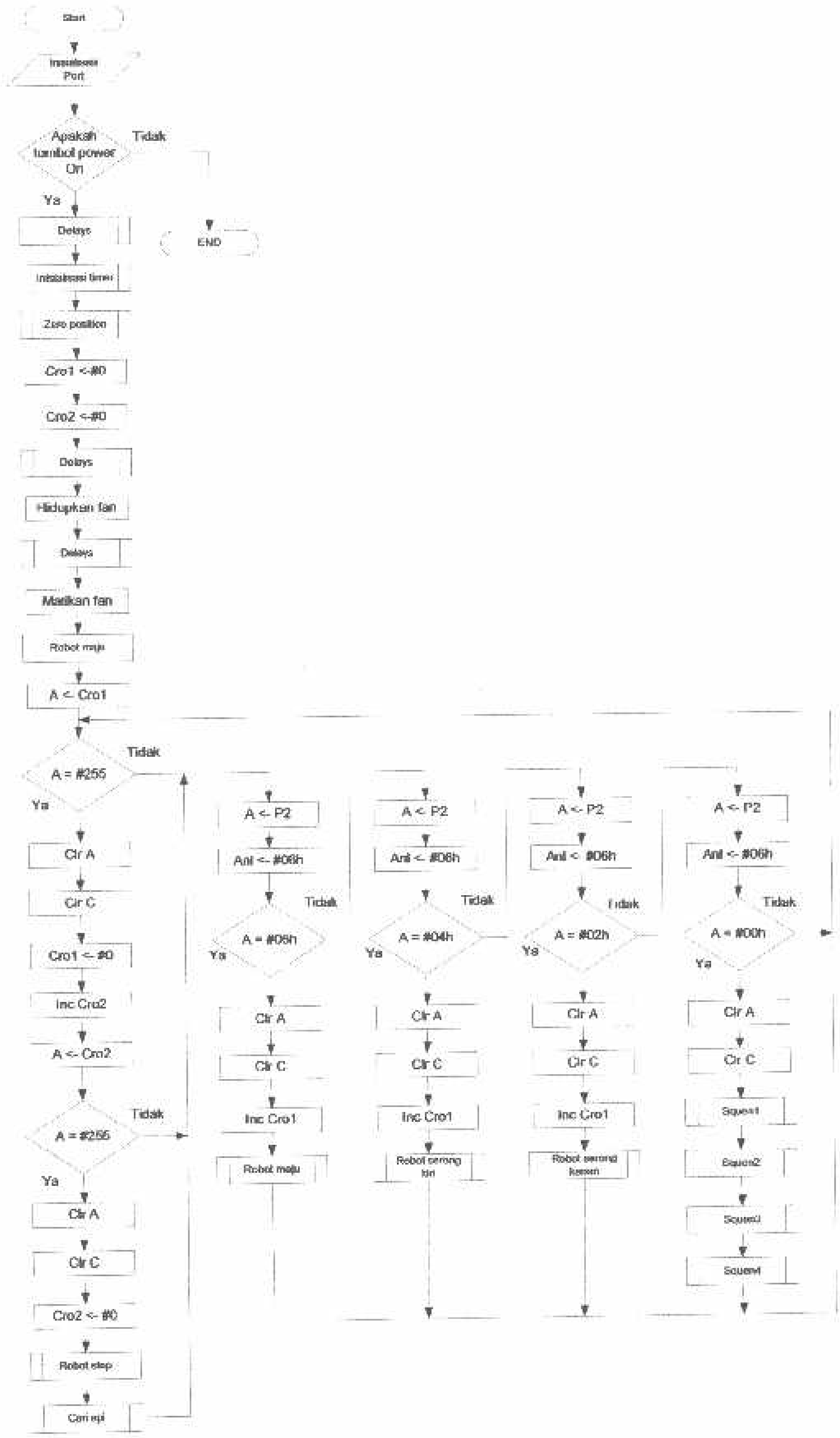
dengan : c = kecepatan cahaya (m/s)

λ = panjang gelombang (m)

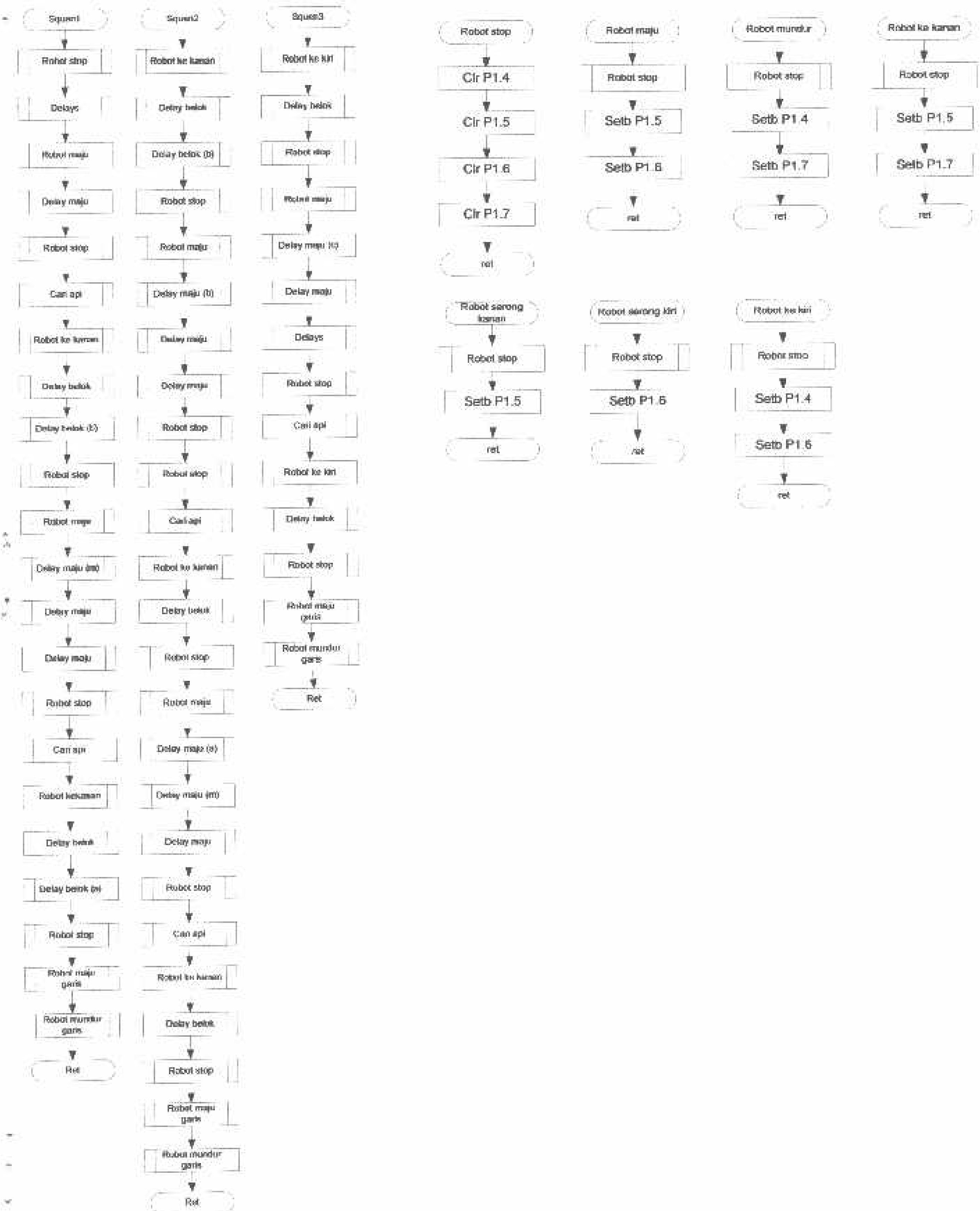
f = frekuensi (Hz)

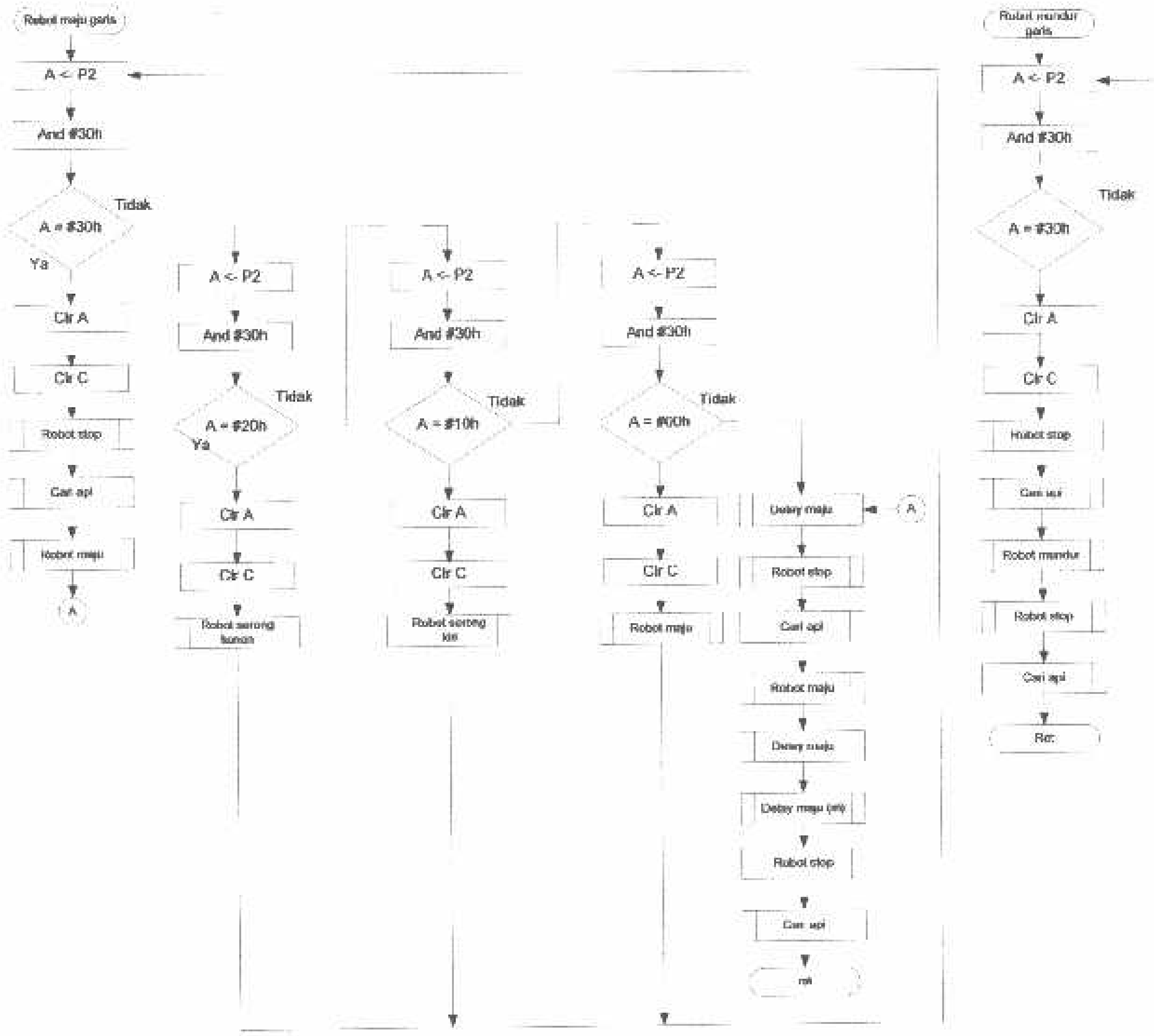
Suatu spektrum frekuensi cahaya disebut Inframerah jika panjang gelombangnya 0,1 μm – 100 μm.

Flowchart program utama:

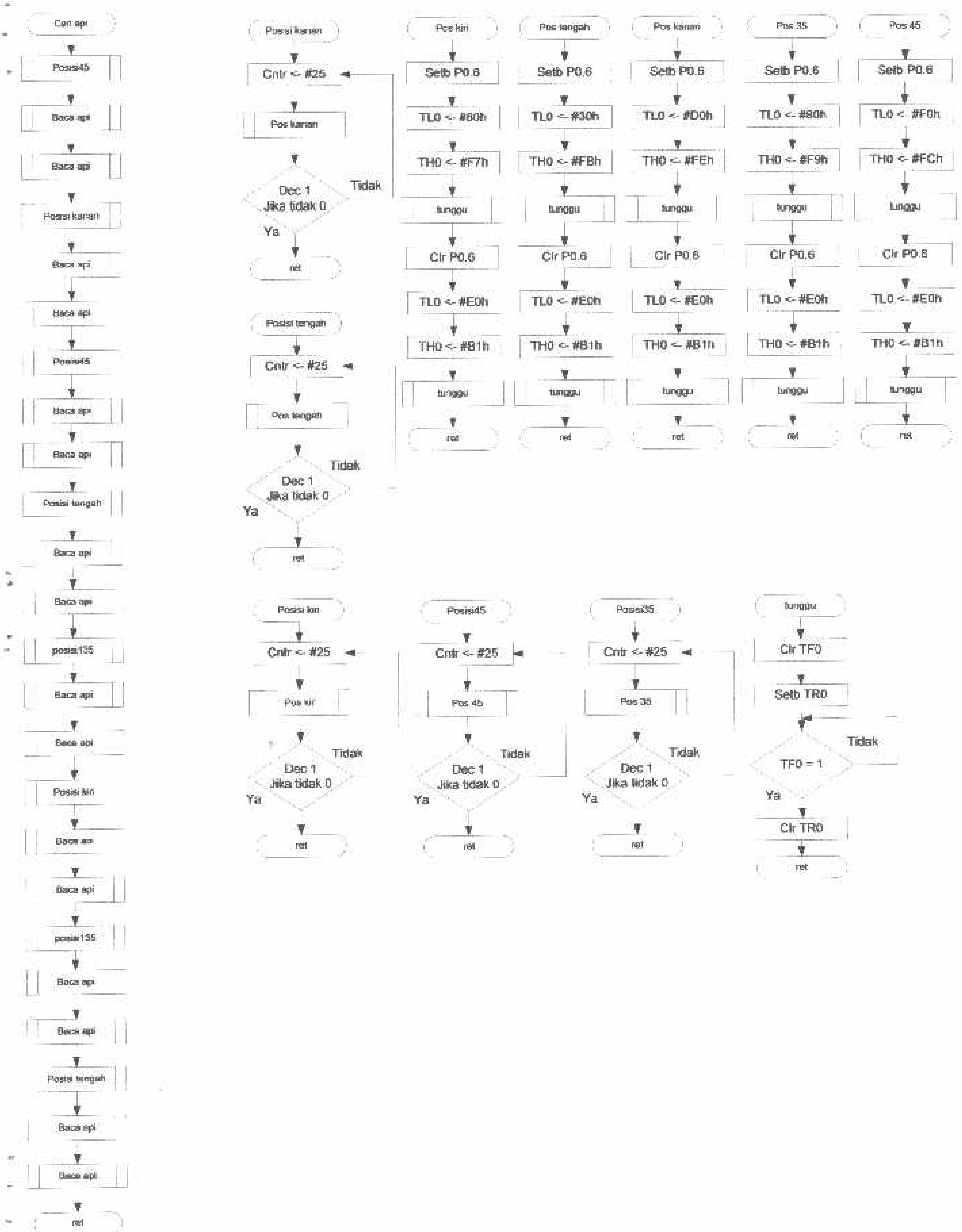


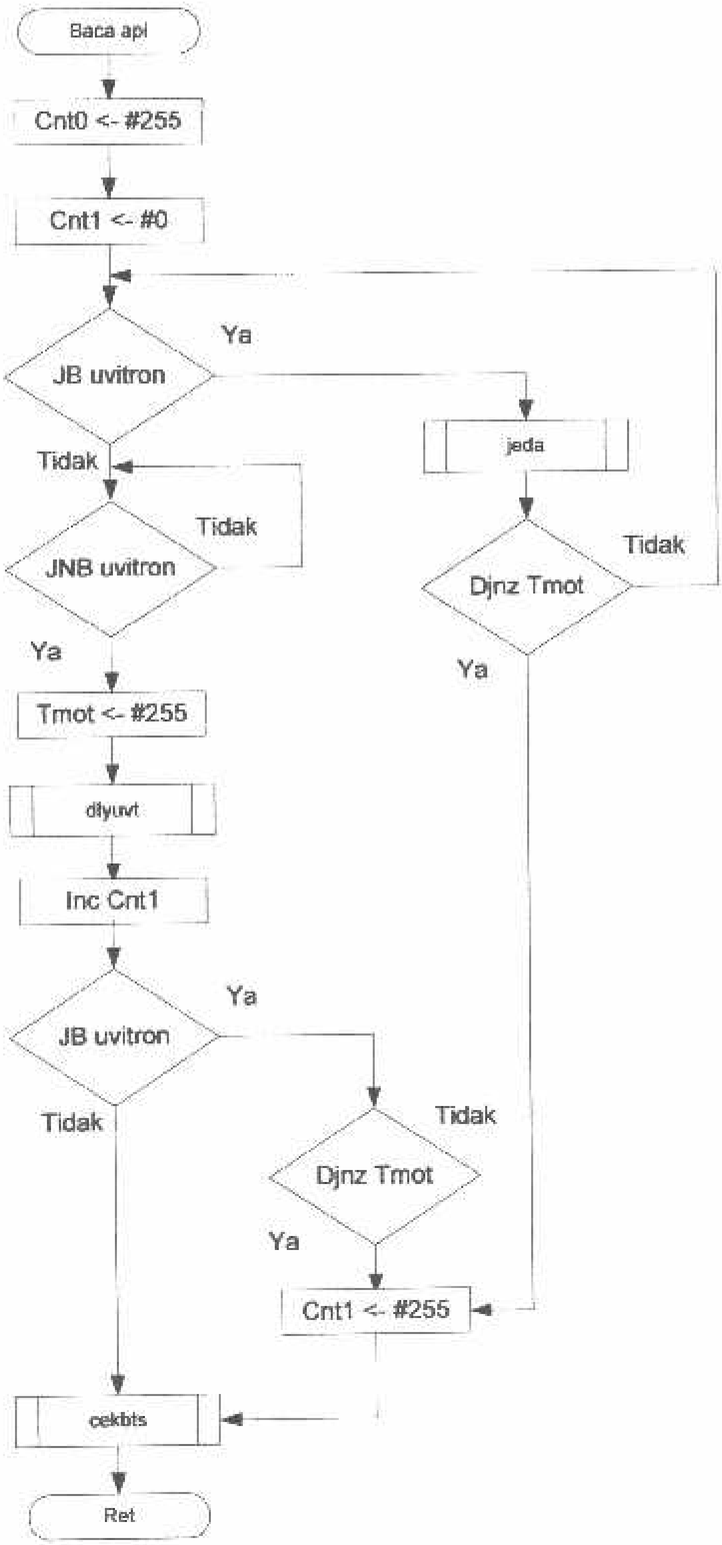
Flowchart program bagian:

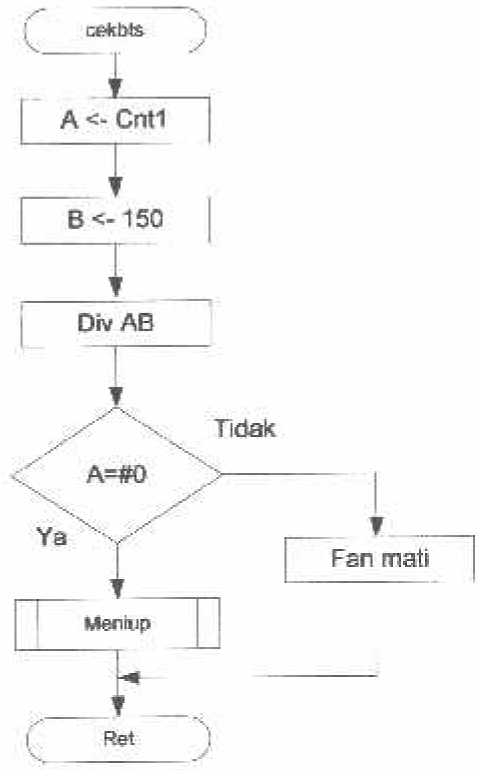


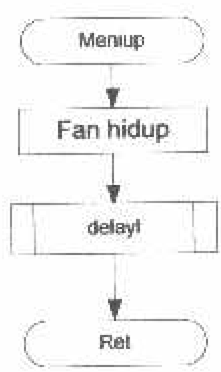


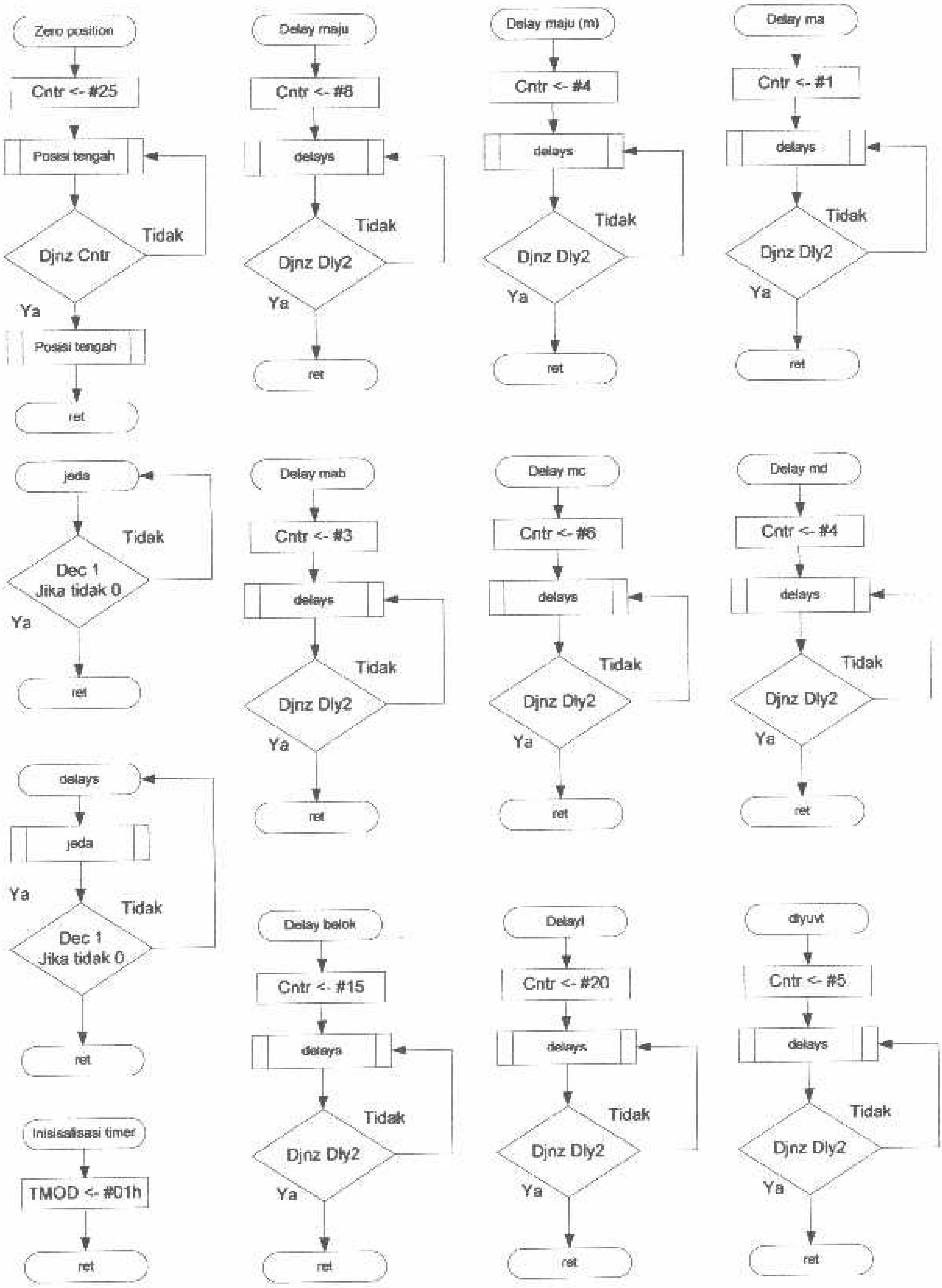
Robot maju garis
A <- P2
And #30h
Tidak
A = #30h
Ya
Clr A
Clr C
Robot stop
Cari api
Robot maju
A
A <- P2
And #30h
Tidak
A = #20h
Ya
Clr A
Clr C
Robot serong kanan
A <- P2
And #30h
Tidak
A = #10h
Clr A
Clr C
Robot serong kiri
A <- P2
And #30h
Tidak
A = #00h
Clr A
Clr C
Robot maju
Delay maju
A
Robot stop
Cari api
Robot maju
Delay maju
Robot stop
Cari api
ret
Robot mundur garis
A <- P2
And #30h
Tidak
A = #30h
Clr A
Clr C
Robot stop
Cari api
Robot mundur
Robot stop
Cari api
Ret


Cari api
Posisi45
Baca api
Baca api
Posisi kanan
Baca api
Baca api
Posisi45
Baca api
Baca api
Posisi tengah
Baca api
Baca api
posisi135
Baca api
Baca api
Posisi kiri
Baca api
Baca api
posisi135
Baca api
Baca api
Posisi tengah
Baca api
Baca api
ret
Posisi kanan
Cntr <- #25
Pos kanan
Dec 1
Jika tidak 0
Tidak
Ya
ret
Posisi tengah
Cntr <- #25
Pos tengah
Dec 1
Jika tidak 0
Tidak
Ya
ret
Pos kiri
Setb P0.6
TL0 <- #80h
TH0 <- #F7h
tunggu
Clr P0.6
TL0 <- #E0h
TH0 <- #B1h
tunggu
ret
Pos tengah
Setb P0.6
TL0 <- #30h
TH0 <- #FBh
tunggu
Clr P0.6
TL0 <- #E0h
TH0 <- #B1h
tunggu
ret
Pos kanan
Setb P0.6
TL0 <- #D0h
TH0 <- #FEh
tunggu
Clr P0.6
TL0 <- #E0h
TH0 <- #B1h
tunggu
ret
Pos 35
Setb P0.6
TL0 <- #80h
TH0 <- #F9h
tunggu
Clr P0.6
TL0 <- #E0h
TH0 <- #B1h
tunggu
ret
Pos 45
Setb P0.6
TL0 <- #F0h
TH0 <- #FCh
tunggu
Clr P0.6
TL0 <- #E0h
TH0 <- #B1h
tunggu
ret
Posisi kiri
Cntr <- #25
Pos kiri
Dec 1
Jika tidak 0
Tidak
Ya
ret
Posisi45
Cntr <- #25
Pos 45
Dec 1
Jika tidak 0
Tidak
Ya
ret
Posisi35
Cntr <- #25
Pos 35
Dec 1
Jika tidak 0
Tidak
Ya
ret
tunggu
Clr TF0
Setb TR0
TF0 = 1
Tidak
Ya
Clr TR0
ret


Baca api
Cnt0 <- #255
Cnt1 <- #0
JB uvitron
Ya
Tidak
jeda
Djnz Tmot
Tidak
Ya
JNB uvitron
Tidak
Ya
Tmot <- #255
dlyuvt
Inc Cnt1
JB uvitron
Ya
Tidak
Djnz Tmot
Tidak
Ya
Cnt1 <- #255
cekbts
Ret


cekbts
A <- Cnt1
B <- 150
Div AB
A=#0
Tidak
Ya
Fan mati
Meniup
Ret


Meniup
Fan hidup
delayf
Ret


Zero position
Cntr <- #25
Posisi tengah
Djnz Cntr
Tidak
Ya
Posisi tengah
ret
Delay maju
Cntr <- #8
delays
Djnz Dly2
Tidak
Ya
ret
Delay maju (m)
Cntr <- #4
delays
Djnz Dly2
Tidak
Ya
ret
Delay ma
Cntr <- #1
delays
Djnz Dly2
Tidak
Ya
ret
jeda
Dec 1
Jika tidak 0
Tidak
Ya
ret
Delay mab
Cntr <- #3
delays
Djnz Dly2
Tidak
Ya
ret
Delay mc
Cntr <- #6
delays
Djnz Dly2
Tidak
Ya
ret
Delay md
Cntr <- #4
delays
Djnz Dly2
Tidak
Ya
ret
delays
jeda
Dec 1
Jika tidak 0
Tidak
Ya
ret
Inisialisasi timer
TMOD <- #01h
ret
Delay belok
Cntr <- #15
delays
Djnz Dly2
Tidak
Ya
ret
Delayl
Cntr <- #20
delays
Djnz Dly2
Tidak
Ya
ret
dlyuvt
Cntr <- #5
delays
Djnz Dly2
Tidak
Ya
ret

Program pada mikrokontroler AT89S8252:

```
        Org     0h
;
        PwSv    Bit P0.6
        Ovtr    Bit P1.0
        Tfin    Bit P1.1
        MkrL    Bit P1.4
        MkrR    Bit P1.5
        MknR    Bit P1.6
        MknL    Bit P1.7
        Snbl    Bit P2.0
        Snkr    Bit P2.1
        Snkn    Bit P2.2
        Sndp    Bit P2.3
        Snb0    Bit P2.4
        Snb1    Bit P2.5
;
        Cnt0    Equ 30h
        Cnt1    Equ 31h
        Cntr    Equ 32h
        Cro1    Equ 33h
        Cro2    Equ 34h
        Crln    Equ 35h
        Tmot    Equ 36h
;
        Dly0    Equ 41h
        Dly1    Equ 42h
        Dly2    Equ 43h
        Dly3    Equ 44h
;
init:   acall   delays
        acall   tmr_in
        acall   zero
;
        Mov     Cro1,#0
        Mov     Cro2,#0
;
        acall   delays
        clr     Tfin
        acall   delays
        acall   delays
        setb    Tfin
        acall   rbtmj
;______________________________________
jalan:  mov     A,Cro
        cjne    A,#255,jln0
        clr     A
        clr     C
        mov     Cro1,#0
        inc     Cro2
        mov     A,Cro2
        cjne    A,#255,jln0
        clr     A
        clr     C
        mov     Cro2,#0
        acall   rbtst
        acall   carapi
jln0:   mov     A,P2
        anl     A,#00000110b
        cjne    A,#00000110b,jln1
        clr     A
        clr     C
        inc     Cro1
        acall   rbtmj
        sjmp    jalan
jln1:   mov     A,P2
        anl     A,#00000110b
        cjne    A,#00000100b,jln2
        clr     A
        clr     C
        inc     Cro1
        acall   rbtsl
        sjmp    jalan
jln2:   mov     A,P2
        anl     A,#00000110b
```

```
        cjne    A,#00000010b,jln3
        clr     A
        clr     C
        inc     Cro1
        acall   rbtor
        sjmp    jalan
jln3:   mov     A,P2
        anl     A,#00000110b
        cjne    A,#00000000b,jln4
        clr     A
        clr     C
        acall   squen1
        acall   squen2
        acall   squen3
        acall   squen4
jln4:   ljmp    jalan
;_________________________________
squen1: acall   rbtst
        acall   delays
        acall   rbtmj
        acall   delmj           ; delay maju P1
        acall   rbtst
        acall   carapi
;
        acall   rbtkn
        acall   delbe
;       acall   delmb
        acall   rbtst
        acall   rbtmj
        acall   delmm
        acall   delmj
        acall   delmj           ; delay maju P2
        acall   rbtst
;
        acall   carapi
        acall   rbtkn
        acall   delbe
;       acall   delma
        acall   rbtst
        acall   rbtgrs
        acall   rbtmdr
        ret
;
squen2: acall   rbtkn
        acall   delbe
        acall   delmb
        acall   rbtst
        acall   rbtmj
        acall   delmb
        acall   delmj
        acall   delmj           ; delay maju P3
        acall   rbtst
        acall   carapi
;
        acall   rbtkn
        acall   delbe
        acall   rbtst
        acall   rbtmj
        acall   delma           ; delay maju P4
        acall   delmm
        acall   delmj
        acall   rbtst
        acall   carapi
;
        acall   rbtkn
        acall   delbe
        acall   rbtst
;
        acall   rbtgrs
        acall   rbtmdr
        ret
;
squen3: acall   rbtkr
        acall   delbe
        acall   rbtst
        acall   rbtmj
        acall   delmc           ; delay maju P5
```

```
        acall   delmj
        acall   delays
        acall   rbtst
        acall   carapi
;
        acall   rbtkr
        acall   delbe
        acall   rbtst
        acall   rbtgrs
        acall   rbtmdr
        ret
;
squen4: acall   rbtkr
        acall   delbe
        acall   rbtst
        acall   rbtmj
        acall   delmj           ; delay maju P6
        acall   rbtst
        acall   carapi
        acall   rbtmj
        acall   delmj           ; delay maju P7
        acall   delmj
        acall   delmm
        acall   rbtst
        acall   carapi
        acall   rbtkn
        acall   delbe
        acall   rbtst
        sjmp    $
;________________________________
rbtmj:  acall   rbtst
        setb    MkrR
        setb    MknR
        ret
;
rbtmd:  acall   rbtst
        setb    MkrL
        setb    MknL
        ret
;
rbtkr:  acall   rbtst
        setb    MkrL
        setb    MknR
        ret
;
rbtkn:  acall   rbtst
        setb    MkrR
        setb    MknL
        ret
;
rbtsr:  acall   rbtst
        setb    MkrR
        ret
;
rbtsl:  acall   rbtst
        setb    MknR
        ret
;
rbtst:  clr     MkrR
        clr     MkrL
        clr     MknR
        clr     MknL
        ret
;
rbtgrs: acall   rbtmj
rbtgr:  mov     A,P2
        anl     A,#00110000b
        cjne    A,#00110000b,lop11
        clr     A
        clr     C
        acall   rbtst
        acall   carapi
        acall   rbtmj
        sjmp    lop15
lop11:  mov     A,P2
        anl     A,#00110000b
        cjne    A,#00100000b,lop12
```

```
        clr     A
        clr     C
        acall   rbtsr
        sjmp    rbtgr
lop12:  mov     A,P2
        anl     A,#00110000b
        cjne    A,#00010000b,lop13
        clr     A
        clr     C
        acall   rbtsl
        sjmp    rbtgr
lop13:  mov     A,P2
        anl     A,#00110000b
        cjne    A,#00000000b,lop14
        clr     A
        clr     C
        acall   rbtmj
lop14:  sjmp    rbtgr
lop15:  acall   delmj           ; delay maju P
        acall   rbtst
        acall   carapi
        acall   rbtmj
        acall   delmj
        acall   delmm           ; delay maju P
        acall   rbtst
        acall   carapi
        ret
;
rbtmdr: acall   rbtmd
lop16:  mov     A,P2
        anl     A,#00110000b
        cjne    A,#00110000b,lop16
        clr     A
        clr     C
        acall   rbtst
        acall   carapi
        acall   rbtmd
        acall   delmd           ; delay mundur P
        acall   rbtst
        acall   carapi
        ret
;
zero:   mov     Cntr,#25
zer:    acall   serte
        djnz    Cntr,zer
        acall   rbtmj
        ret
;
carapi: acall   posi45
        acall   bc_sns
        acall   bc_sns
        acall   posika
        acall   bc_sns
        acall   bc_sns
        acall   posi45
        acall   bc_sns
        acall   bc_sns
        acall   posite
        acall   bc_sns
        acall   bc_sns
        acall   posi35
        acall   bc_sns
        acall   bc_sns
        acall   posiki
        acall   bc_sns
        acall   bc_sns
        acall   posi35
        acall   bc_sns
        acall   bc_sns
        acall   posite
        acall   bc_sns
        acall   bc_sns
        ret
;
posika: mov     Cntr,#25
pos0:   acall   serka
        djnz    Cntr,pos0
```

```
        ret
posite: mov     Cntr,#25
pos1:   acall   serte
        djnz    Cntr,pos1
        ret
posiki: mov     Cntr,#25
pos2:   acall   serki
        djnz    Cntr,pos2
        ret
;
posi45: mov     Cntr,#25
pos3:   acall   ser45
        djnz    Cntr,pos3
        ret
;
posi35: mov     Cntr,#25
pos4:   acall   ser35
        djnz    Cntr,pos4
        ret
;
serki:  setb    PwSv
        mov     TL0,#000h
        mov     TH0,#0F7h
        acall   tnggu
        clr     PwSv
        mov     TL0,#0E0h
        mov     TH0,#0B1h
        acall   tnggu
        ret
;
ser35:  setb    PwSv
        mov     TL0,#080h
        mov     TH0,#0F9h
        acall   tnggu
        clr     PwSv
        mov     TL0,#0E0h
        mov     TH0,#0B1h
        acall   tnggu
        ret
;
serte:  setb    PwSv
        mov     TL0,#030h
        mov     TH0,#0FBh
        acall   tnggu
        clr     PwSv
        mov     TL0,#0E0h
        mov     TH0,#0B1h
        acall   tnggu
        ret
;
ser45:  setb    PwSv
        mov     TL0,#0F0h
        mov     TH0,#0FCh
        acall   tnggu
        clr     PwSv
        mov     TL0,#0E0h
        mov     TH0,#0B1h
        acall   tnggu
        ret
;
serka:  setb    PwSv
        mov     TL0,#0D0h
        mov     TH0,#0FEh
        acall   tnggu
        clr     PwSv
        mov     TL0,#0E0h
        mov     TH0,#0B1h
        acall   tnggu
        ret
;
tnggu:  clr     TF0
        setb    TR0
        jnb     TF0,$
        clr     TR0
        ret
;
bc_sns: mov     Cnt0,#255               ; set counter maximum
```

```
        mov     Cnt1,#0                    ; reset counter
        mov     Tmot,#255                 ;\
bcsns0: jb      Uvtr,bcsns1               ; | set time out
        sjmp    bcsns2                    ; | tunggu sensor low
bcsns1: acall   jeda
        djnz    Tmot,bcsns0               ; | tidak low - lompat
        sjmp    bcsns6                    ;/
bcsns2: jnb     Uvtr,$                    ; tunggu sensor high
        mov     Tmot,#255                 ;\
bcsns3: acall   dlyuvt                    ; | delay counter uvtron
        inc     Cnt1                      ; |
        jb      Uvtr,bcsns4               ; | set time out
        sjmp    bcsns7                    ; | tunggu sensor low
bcsns4: djnz    Tmot,bcsns5               ; | tidak low - lompat
        sjmp    bcsns6                    ;/
bcsns5: djnz    Cnt0,bcsns3
bcsns6: mov     Cnt1,#255
bcsns7: acall   cekbts
        ret
;
cekbts: mov     A,Cnt1
        mov     B,#150                    ; batas minimum peniupan 65
        div     AB
        cjne    A,#0,ckbts
        acall   meniup
ckbts:  setb    Tfin
        ret
;
meniup: clr     Tfin
        acall   delay1
        ret
;
tmr_in: mov     TMOD,#01h
        ret
;
jeda:   djnz    Dly0,$
        ret
;
delays: acall   jeda
        djnz    Dly1,delays
        ret
;
delmj:  mov     Dly2,#8           ; setting lama maju 00
delm1:  acall   delays
        djnz    Dly2,delm1
        ret
;
delmm:  mov     Dly2,#4           ; setting lama maju 00
delm2:  acall   delays
        djnz    Dly2,delm2
        ret
;
delma:  mov     Dly2,#1           ; setting lama maju P2
delm3:  acall   delays
        djnz    Dly2,delm3
        ret
;
delmb:  mov     Dly2,#3           ; setting lama maju P4
delm4:  acall   delays
        djnz    Dly2,delm4
        ret
;
delmc:  mov     Dly2,#6           ; setting lama maju P5
delm5:  acall   delays
        djnz    Dly2,delm5
        ret
;
delmd:  mov     Dly2,#4           ; setting lama mundur 00
delm6:  acall   delays
        djnz    Dly2,delm6
        ret
;
delbe:  mov     Dly2,#15          ; setting belok 90 derajat
delb1:  acall   delays
        djnz    Dly2,delb1
        ret
;
```

```
delayl: mov     Dly2,#20
dlyl:   acall   delays
        djnz    Dly2,dlyl
        ret
;
dlyuvt: mov     Dly3,#5
dlyuv:  acall   joda
        djnz    Dly3,dlyuv
        ret
;
        end
```

TIP31, TIP31A, TIP31B, TIP31C, (NPN), TIP32, TIP32A, TIP32B, TIP32C, (PNP)

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Complementary Silicon Plastic Power Transistors

Designed for use in general purpose amplifier and switching applications.

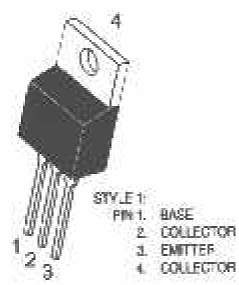
- Collector-Emitter Saturation Voltage -
  $V_{CE(sat)}$ = 1.2 Vdc (Max) @ I_C = 3.0 Adc
- Collector-Emitter Sustaining Voltage -
  $V_{CEO(sus)}$ = 40 Vdc (Min) - TIP31, TIP32
  = 60 Vdc (Min) - TIP31A, TIP32A
  = 80 Vdc (Min) - TIP31B, TIP32B
  = 100 Vdc (Min) - TIP31C, TIP32C
- High Current Gain - Bandwidth Product
  f_T = 3.0 MHz (Min) @ I_C = 500 mAdc
- Compact TO-220 AB Package

3 AMPERE
POWER TRANSISTORS
COMPLEMENTARY
SILICON
40-60-80-100 VOLTS
40 WATTS

MAXIMUM RATINGS

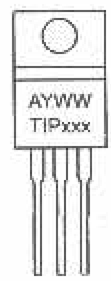
Rating	Symbol	Value	Unit
Collector-Emitter Voltage TIP31, TIP32 TIP31A, TIP32A TIP31B, TIP32B TIP31C, TIP32C	V_{CEO}	40 60 80 100	Vdc
Collector-Base Voltage TIP31, TIP32 TIP31A, TIP32A TIP31B, TIP32B TIP31C, TIP32C	V_{CB}	40 60 80 100	Vdc
Emitter-Base Voltage	V_{EB}	5.0	Vdc
Collector Current Continuous Peak	I_C	3.0 5.0	Adc
Base Current	I_B	1.0	Adc
Total Power Dissipation @ T_C = 25°C Derate above 25°C	P_D	40 0.32	Watts W/°C
Total Power Dissipation @ T_A = 25°C Derate above 25°C	P_D	2.0 0.016	Watts W/°C
Unclamped Inductive Load Energy (Note 1)	E	32	mJ
Operating and Storage Junction Temperature Range	T_J, T_{stg}	−65 to +150	°C

1. I_C = 1.8 A, L = 20 mH, P.R.F. = 10 Hz, V_{CC} = 10 V, R_{BE} = 100 Ω.



TO-220AB
CASE 221A-09
STYLE 1

MARKING DIAGRAM



xxx = Specific Device Code:
31, 31A, 31B, 31C, 32, 32A, 32B, 32C
A = Assembly Location
Y = Year
WW = Work Week

ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 6 of this data sheet.

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Ambient	$R_{\theta JA}$	62.5	°C/W
Thermal Resistance, Junction to Case	$R_{\theta JC}$	3.125	°C/W

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic		Symbol	Min	Max	Unit
OFF CHARACTERISTICS					
Collector-Emitter Sustaining Voltage (Note 2) (I_C = 30 mAdc, I_B = 0)	TIP31, TIP32	$V_{CEO(sus)}$	40	-	Vdc
	TIP31A, TIP32A		60	-	
	TIP31B, TIP32B		80	-	
	TIP31C, TIP32C		100	-	
Collector Cutoff Current (V_{CE} = 30 Vdc, I_B = 0)	TIP31, TIP32, TIP31A, TIP32A	I_{CEO}	-	0.3	mAdc
(V_{CE} = 60 Vdc, I_B = 0)	TIP31B, TIP31C, TIP32B, TIP32C		-	0.3	
Collector Cutoff Current		I_{CES}			μAdc
(V_{CE} = 40 Vdc, V_{EB} = 0)	TIP31, TIP32		-	200	
(V_{CE} = 60 Vdc, V_{EB} = 0)	TIP31A, TIP32A		-	200	
(V_{CE} = 80 Vdc, V_{EB} = 0)	TIP31B, TIP32B		-	200	
(V_{CE} = 100 Vdc, V_{EB} = 0)	TIP31C, TIP32C		-	200	
Emitter Cutoff Current (V_{BE} = 5.0 Vdc, I_C = 0)		I_{EBO}	-	1.0	mAdc
ON CHARACTERISTICS (Note 2)					
DC Current Gain (I_C = 1.0 Adc, V_{CE} = 4.0 Vdc)		h_{FE}	25	-	-
(I_C = 3.0 Adc, V_{CE} = 4.0 Vdc)			10	50	
Collector-Emitter Saturation Voltage (I_C = 3.0 Adc, I_B = 375 mAdc)		$V_{CE(sat)}$	-	1.2	Vdc
Base-Emitter On Voltage (I_C = 3.0 Adc, V_{CE} = 4.0 Vdc)		$V_{BE(on)}$	-	1.8	Vdc
DYNAMIC CHARACTERISTICS					
Current-Gain - Bandwidth Product (I_C = 500 mAdc, V_{CE} = 10 Vdc, f_{test} = 1.0 MHz)		f_T	3.0	-	MHz
Small-Signal Current Gain (I_C = 0.5 Adc, V_{CE} = 10 Vdc, f = 1.0 kHz)		h_{fe}	20	-	-

2. Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2.0%.

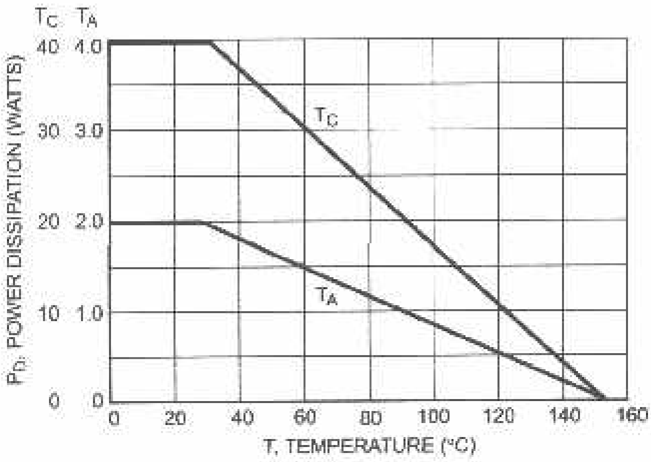


Figure 1. Power Derating

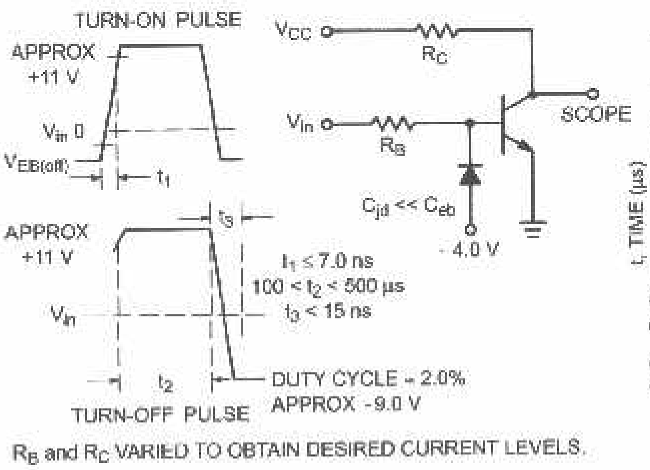


Figure 2. Switching Time Equivalent Circuit

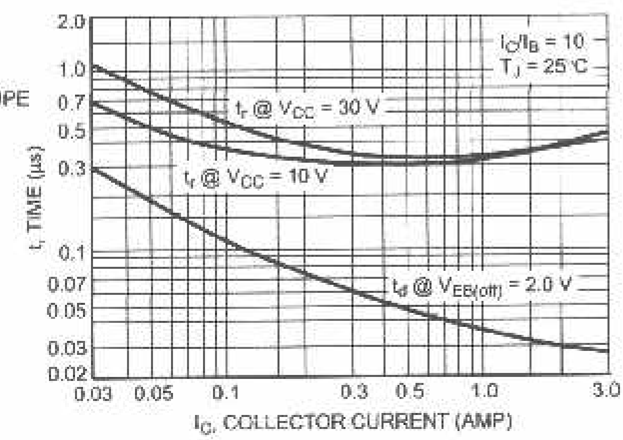


Figure 3. Turn-On Time

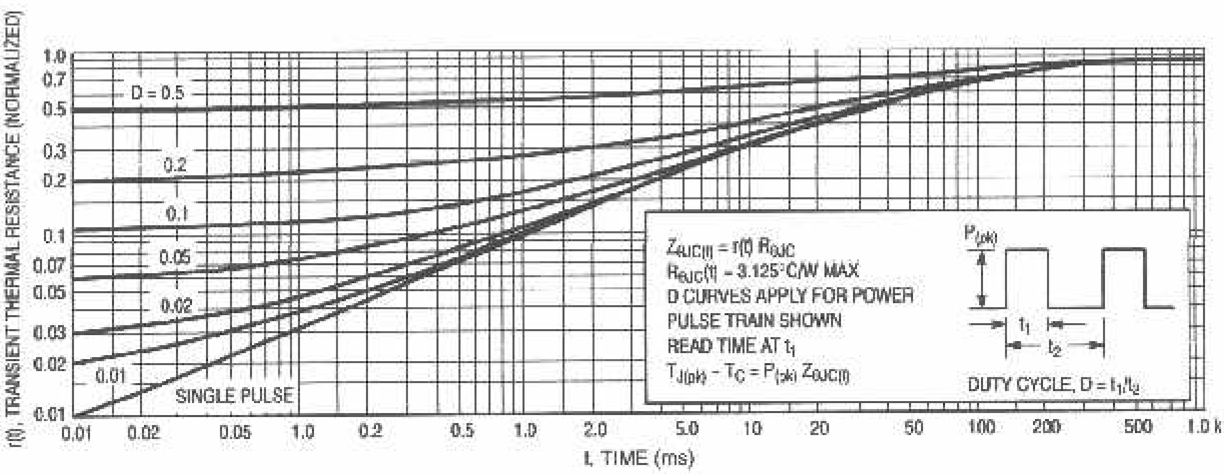


Figure 4. Thermal Response

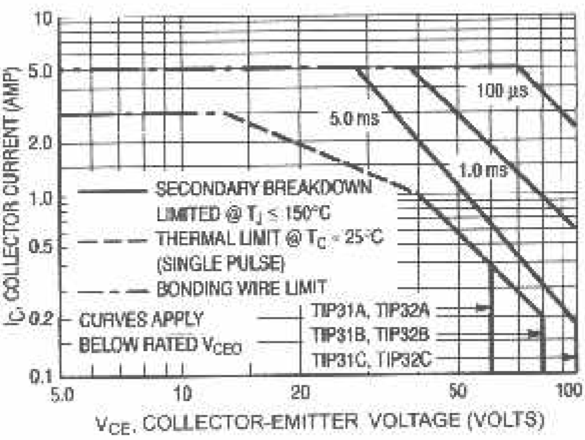


Figure 5. Active Region Safe Operating Area

There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate I_C - V_{CE} limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 5 is based on $T_{J(pk)} = 150°C$; T_C is variable depending on conditions. Second breakdown pulse limits are valid for duty cycles to 10% provided $T_{J(pk)} \le 150°C$. $T_{J(pk)}$ may be calculated from the data in Figure 4. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown.

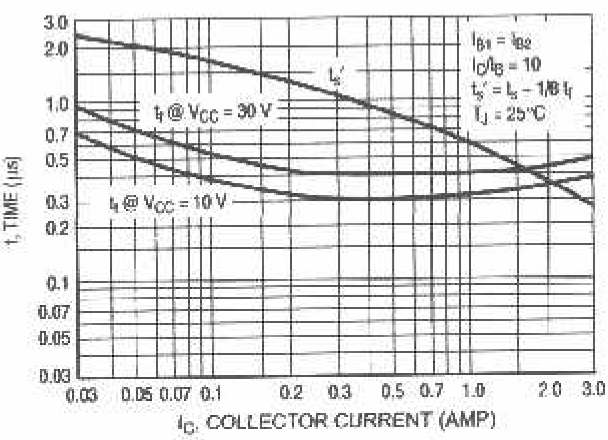


Figure 6. Turn-Off Time

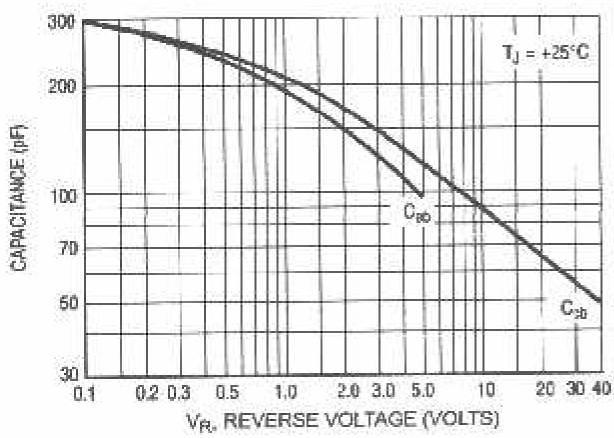


Figure 7. Capacitance

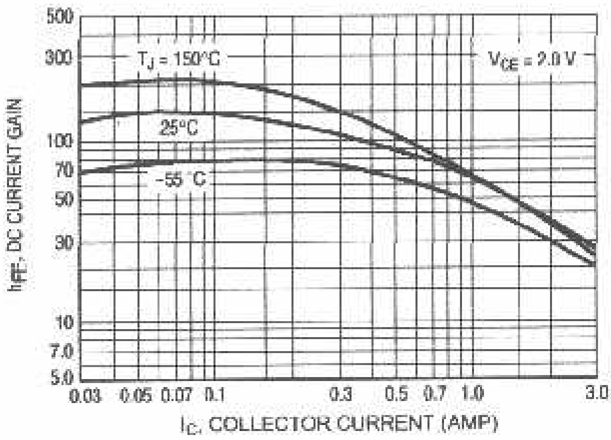


Figure 8. DC Current Gain

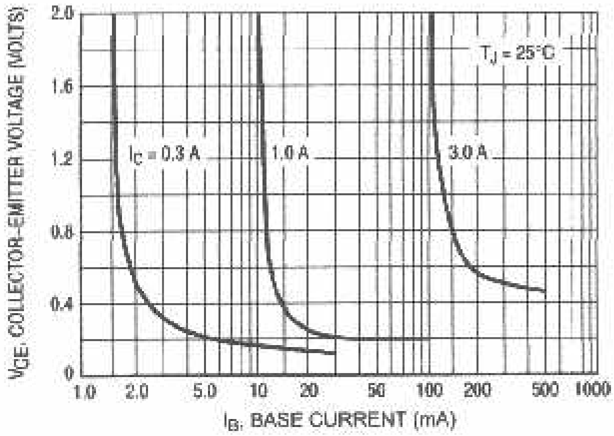


Figure 9. Collector Saturation Region

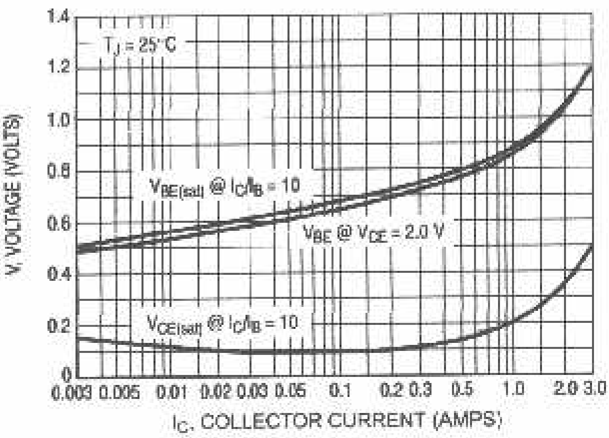


Figure 10. "On" Voltages

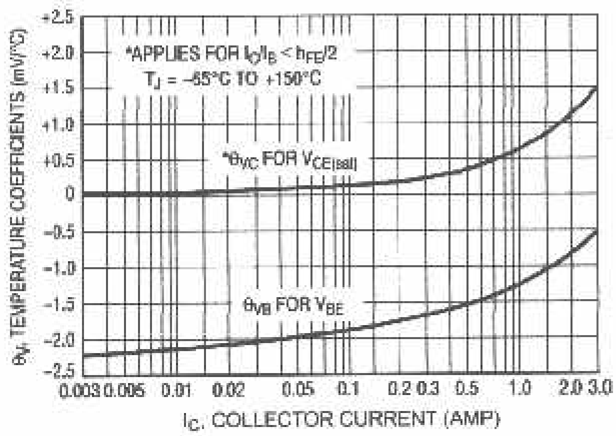


Figure 11. Temperature Coefficients

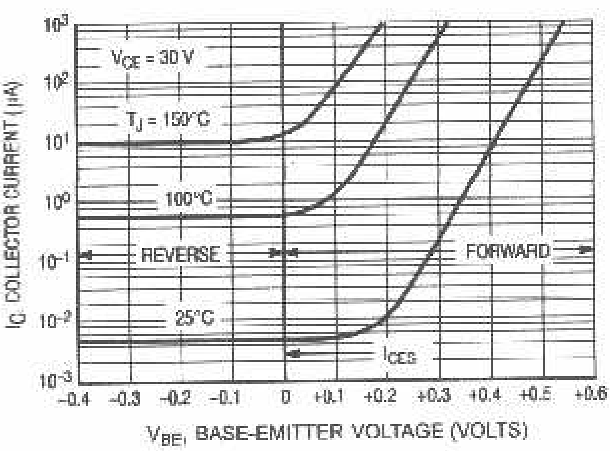


Figure 12. Collector Cut-Off Region

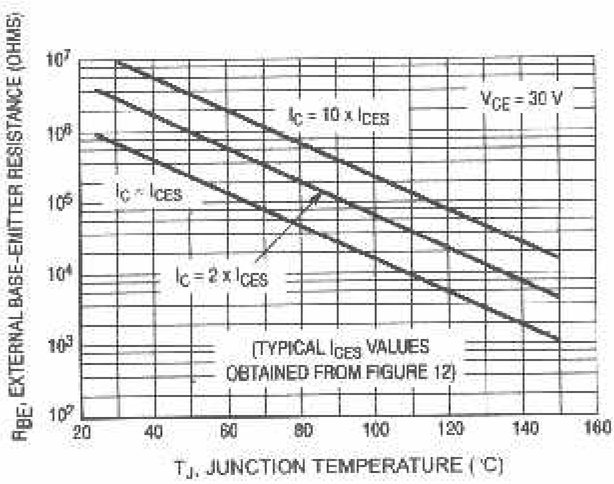


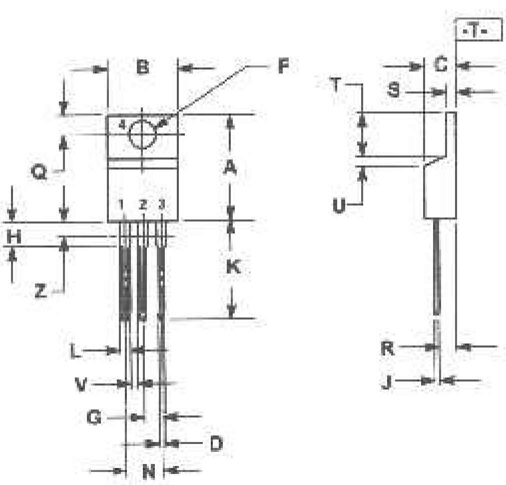
Figure 13. Effects of Base-Emitter Resistance

ORDERING INFORMATION

Device	Package	Shipping
TIP31	TO-220AB	50 Units/Rail
TIP31A	TO-220AB	50 Units/Rail
TIP31B	TO-220AB	50 Units/Rail
TIP31C	TO-220AB	50 Units/Rail
TIP32	TO-220AB	50 Units/Rail
TIP32A	TO-220AB	50 Units/Rail
TIP32B	TO-220AB	50 Units/Rail
TIP32C	TO-220AB	50 Units/Rail

PACKAGE DIMENSIONS

TO-220AB
CASE 221A-09
ISSUE AA



STYLE 1:
PIN 1. BASE
2. COLLECTOR
3. EMITTER
4. COLLECTOR

NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. DIMENSION Z DEFINES A ZONE WHERE ALL BODY AND LEAD IRREGULARITIES ARE ALLOWED.

	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	0.570	0.620	14.48	15.75
B	0.380	0.405	9.66	10.28
C	0.160	0.190	4.07	4.82
D	0.025	0.035	0.64	0.88
F	0.142	0.147	3.61	3.73
G	0.095	0.105	2.42	2.66
H	0.110	0.155	2.80	3.93
J	0.018	0.025	0.46	0.64
K	0.500	0.562	12.70	14.27
L	0.045	0.060	1.15	1.52
N	0.190	0.210	4.83	5.33
Q	0.100	0.120	2.54	3.04
R	0.080	0.110	2.04	2.79
S	0.045	0.055	1.15	1.39
T	0.235	0.255	5.97	6.47
U	0.000	0.050	0.00	1.27
V	0.045		1.15	—
Z	—	0.080	—	2.04

PUBLICATION ORDERING INFORMATION

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FAIRCHILD
SEMICONDUCTOR ™

March 1998

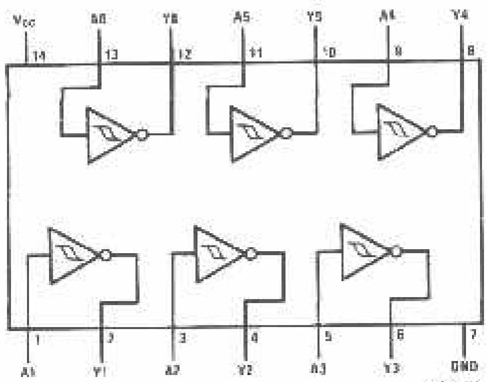
DM74LS14
Hex Inverters with Schmitt Trigger Inputs

General Description

This device contains six independent gates each of which performs the logic INVERT function. Each input has hysteresis which increases the noise immunity and transforms a slowly changing input signal to a fast changing, jitter free output.

Connection Diagram

Dual-In-Line Package



Order Number 54LS14DMQB, 54LS14FMQB, 54LS14LMQB, DM74LS14M or DM74LS14N
See Package Number E20A, J14A, M14A, N14A or W14B

Function Table

$Y = \overline{A}$

Input	Output
A	Y
L	H
H	L

H = High Logic Level
L = Low Logic Level

Absolute Maximum Ratings (Note 1)

Supply Voltage	7V
Input Voltage	7V
Operating Free Air Temperature Range	
54LS	−55°C to +125°C
DM74LS	0°C to +70°C
Storage Temperature Range	−65°C to +150°C

Recommended Operating Conditions

Symbol	Parameter	54LS14			DM74LS14			Units
		Min	Nom	Max	Min	Nom	Max	
V_{CC}	Supply Voltage	4.5	5	5.5	4.75	5	5.25	V
V_{T+}	Positive-Going Input Threshold Voltage (Note 2)	1.5	1.6	2.0	1.4	1.6	1.9	V
V_{T-}	Negative-Going Input Threshold Voltage (Note 2)	0.6	0.8	1.1	0.5	0.8	1	V
HYS	Input Hysteresis (Note 2)	0.4	0.8		0.4	0.8		V
I_{OH}	High Level Output Current			−0.4			−0.4	mA
I_{OL}	Low Level Output Current			4			8	mA
T_A	Free Air Operating Temperature	−55		125	0		70	°C

Note 1: *The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.*

Electrical Characteristics

over recommended operating free air temperature range (unless otherwise noted)

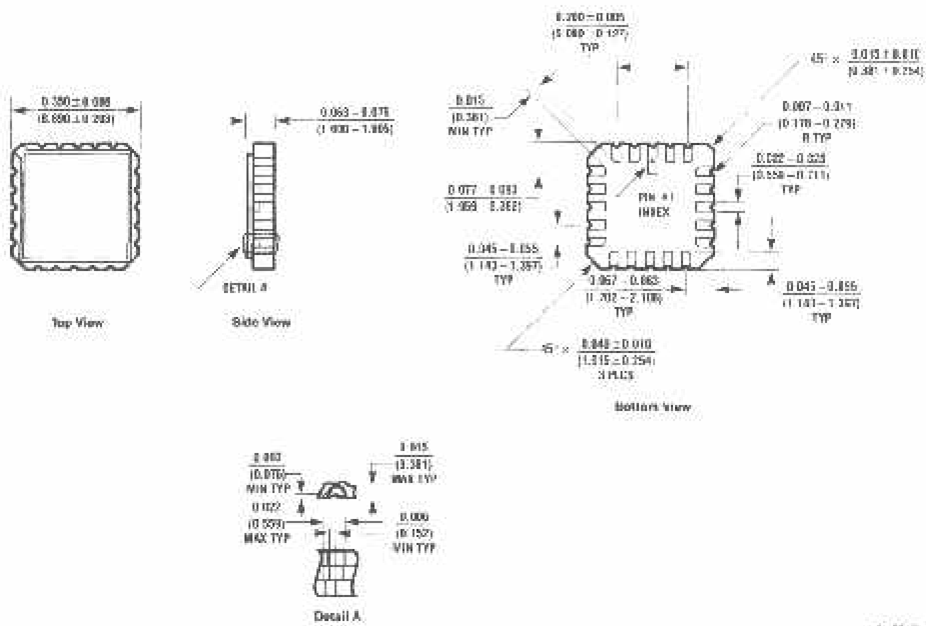
Symbol	Parameter	Conditions		Min	Typ (Note 3)	Max	Units
V_I	Input Clamp Voltage	V_{CC} = Min, I_I = −18 mA				−1.5	V
V_{OH}	High Level Output Voltage	V_{CC} = Min, I_{OH} = Max	54LS	2.5	3.4		V
		V_{IL} = Max	DM74	2.7	3.4		
V_{OL}	Low Level Output Voltage	V_{CC} = Min, I_{OL} = Max	54LS		0.25	0.4	V
		V_{IH} = Min	DM74		0.35	0.5	
		V_{CC} = Min, I_{OL} = 4 mA	DM74		0.25	0.4	
I_{T+}	Input Current at Positive-Going Threshold	V_{CC} = 5V, V_I = V_{T+}	DM74		−0.14		mA
I_{T-}	Input Current at Negative-Going Threshold	V_{CC} = 5V, V_I = V_{T-}	DM74		−0.18		mA
I_I	Input Current @ Max Input Voltage	V_{CC} = Max, V_I = 7V	DM74			0.1	mA
		V_{CC} = Max, V_I = 10.0V	54LS				
I_{IH}	High Level Input Current	V_{CC} = Max, V_I = 2.7V				20	µA
I_{IL}	Low Level Input Current	V_{CC} = Max, V_I = 0.4V				−0.4	mA
I_{OS}	Short Circuit Output Current	V_{CC} = Max	54LS	−20		−100	mA
		(Note 4)	DM74	−20		−100	
I_{CCH}	Supply Current with Outputs High	V_{CC} = Max			8.6	16	mA
I_{CCL}	Supply Current with Outputs Low	V_{CC} = Max			12	21	mA

Note 2: V_{CC} = 5V.

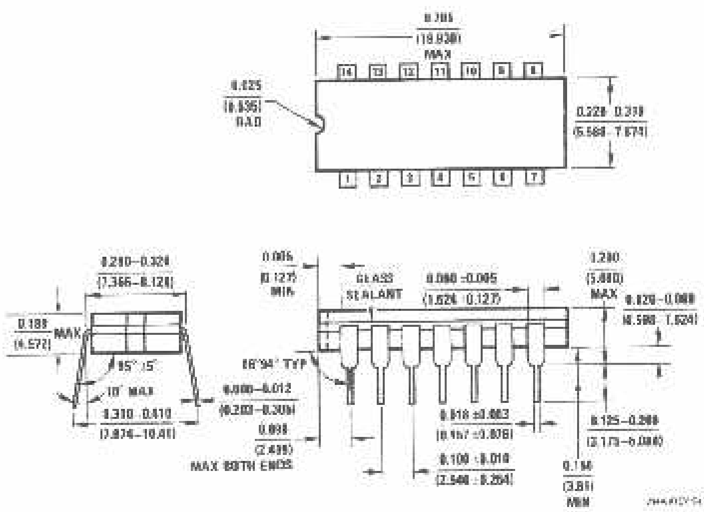
Note 3: All typicals are at V_{CC} = 5V, T_A = 25°C.

Note 4: Not more than one output should be shorted at a time, and the duration should not exceed one second.

Physical Dimensions inches (millimeters) unless otherwise noted

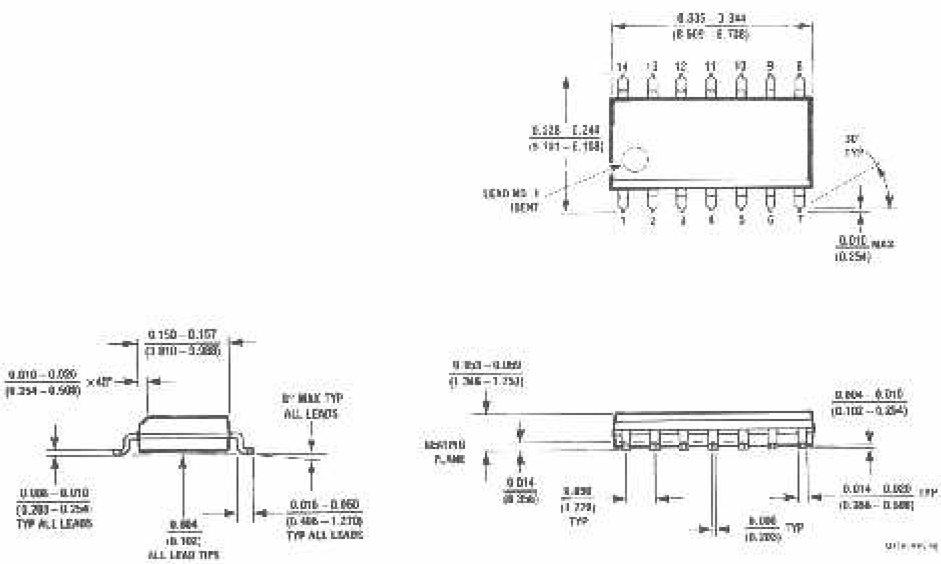


Ceramic Leadless Chip Carrier (E)
Order Number 54LS14LMQB
Package Number E20A

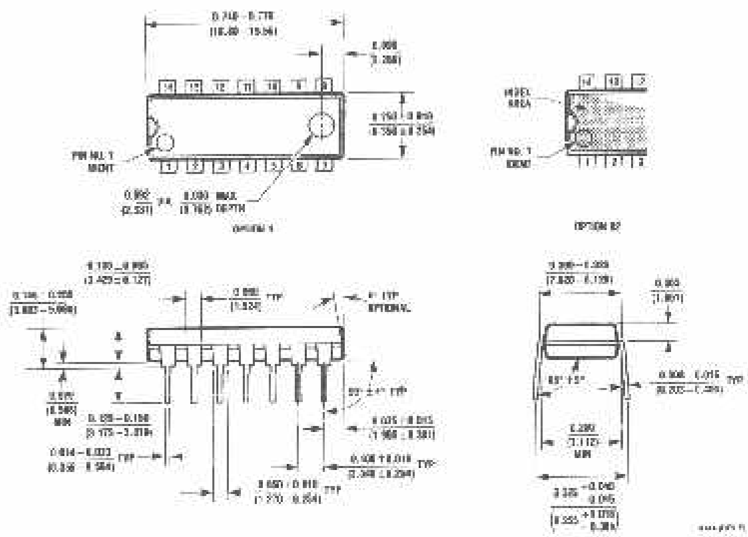


14-Lead Ceramic Dual-In-Line Package (J)
Order Number 54LS14DMQB
Package Number J14A

Physical Dimensions inches (millimeters) unless otherwise noted (Continued)

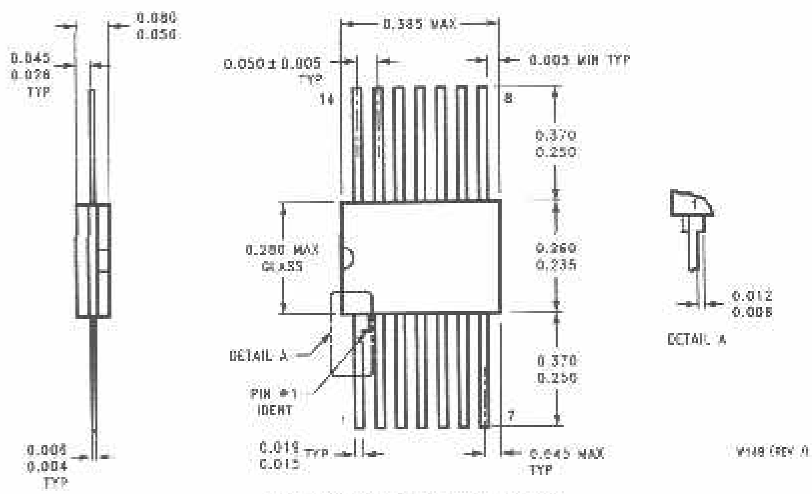


14-Lead Small Outline Molded Package (M)
Order Number DM74LS14M
Package Number M14A



14-Lead Molded Dual-In-Line Package (N)
Order Number DM74LS14N
Package Number N14A

Physical Dimensions inches (millimeters) unless otherwise noted (Continued)



14-Lead Ceramic Flat Package (W)
Order Number 54LS14FMQB
Package Number W14B

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GlobalOptoisolator™

6-Pin DIP Optoisolators Transistor Output

The 4N25/A, 4N26, 4N27 and 4N28 devices consist of a gallium arsenide infrared emitting diode optically coupled to a monolithic silicon phototransistor detector.

- Most Economical Optoisolator Choice for Medium Speed, Switching Applications
- Meets or Exceeds All JEDEC Registered Specifications
- ***To order devices that are tested and marked per VDE 0884 requirements, the suffix "V" must be included at end of part number. VDE 0884 is a test option.***

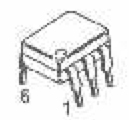
Applications

- General Purpose Switching Circuits
- Interfacing and coupling systems of different potentials and impedances
- I/O Interfacing
- Solid State Relays

4N25*
4N25A*
4N26*
[CTR = 20% Min]
4N27
4N28
[CTR = 10% Min]

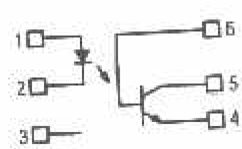
*Motorola Preferred Devices

STYLE 1 PLASTIC



STANDARD THRU HOLE CASE 730A–04

SCHEMATIC



PIN 1. LED ANODE
2. LED CATHODE
3. N.C.
4. EMITTER
5. COLLECTOR
6. BASE

MAXIMUM RATINGS (T_A = 25°C unless otherwise noted)

Rating	Symbol	Value	Unit
INPUT LED			
Reverse Voltage	V_R	3	Volts
Forward Current — Continuous	I_F	60	mA
LED Power Dissipation @ T_A = 25°C with Negligible Power in Output Detector	P_D	120	mW
Derate above 25°C		1.41	mW/°C
OUTPUT TRANSISTOR			
Collector–Emitter Voltage	V_{CEO}	30	Volts
Emitter–Collector Voltage	V_{ECO}	7	Volts
Collector–Base Voltage	V_{CBO}	70	Volts
Collector Current — Continuous	I_C	150	mA
Detector Power Dissipation @ T_A = 25°C with Negligible Power in Input LED	P_D	150	mW
Derate above 25°C		1.76	mW/°C
TOTAL DEVICE			
Isolation Surge Voltage(1) (Peak ac Voltage, 60 Hz, 1 sec Duration)	V_{ISO}	7500	Vac(pk)
Total Device Power Dissipation @ T_A = 25°C Derate above 25°C	P_D	250 2.94	mW mW/°C
Ambient Operating Temperature Range(2)	T_A	–55 to +100	°C
Storage Temperature Range(2)	T_{stg}	–55 to +150	°C
Soldering Temperature (10 sec, 1/16" from case)	T_L	260	°C

1. Isolation surge voltage is an internal device dielectric breakdown rating. For this test, Pins 1 and 2 are common, and Pins 4, 5 and 6 are common.
2. Refer to Quality and Reliability Section in Opto Data Book for information on test conditions.

Preferred devices are Motorola recommended choices for future use and best overall value.
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REV 5

MOTOROLA

ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise noted)(1)

Characteristic		Symbol	Min	Typ(1)	Max	Unit
INPUT LED						
Forward Voltage (I_F = 10 mA)	T_A = 25°C T_A = –55°C T_A = 100°C	V_F	— — —	1.15 1.3 1.05	1.5 — —	Volts
Reverse Leakage Current (V_R = 3 V)		I_R	—	—	100	µA
Capacitance (V = 0 V, f = 1 MHz)		C_J	—	18	—	pF
OUTPUT TRANSISTOR						
Collector–Emitter Dark Current (V_{CE} = 10 V, T_A = 25°C	4N25,25A,26,27 4N28	I_{CEO}	— —	1 1	50 100	nA
(V_{CE} = 10 V, T_A = 100°C)	All Devices	I_{CEO}	—	1	—	µA
Collector–Base Dark Current (V_{CB} = 10 V)		I_{CBO}	—	0.2	—	nA
Collector–Emitter Breakdown Voltage (I_C = 1 mA)		$V_{(BR)CEO}$	30	45	—	Volts
Collector–Base Breakdown Voltage (I_C = 100 µA)		$V_{(BR)CBO}$	70	100	—	Volts
Emitter–Collector Breakdown Voltage (I_E = 100 µA)		$V_{(BR)ECO}$	7	7.8	—	Volts
DC Current Gain (I_C = 2 mA, V_{CE} = 5 V)		h_{FE}	—	500	—	—
Collector–Emitter Capacitance (f = 1 MHz, V_{CE} = 0)		C_{CE}	—	7	—	pF
Collector–Base Capacitance (f = 1 MHz, V_{CB} = 0)		C_{CB}	—	19	—	pF
Emitter–Base Capacitance (f = 1 MHz, V_{EB} = 0)		C_{EB}	—	9	—	pF
COUPLED						
Output Collector Current (I_F = 10 mA, V_{CE} = 10 V)	4N25,25A,26 4N27,28	I_C (CTR)(2)	2 (20) 1 (10)	7 (70) 5 (50)	— —	mA (%)
Collector–Emitter Saturation Voltage (I_C = 2 mA, I_F = 50 mA)		$V_{CE(sat)}$	—	0.15	0.5	Volts
Turn–On Time (I_F = 10 mA, V_{CC} = 10 V, R_L = 100 Ω)(3)		t_{on}	—	2.8	—	µs
Turn–Off Time (I_F = 10 mA, V_{CC} = 10 V, R_L = 100 Ω)(3)		t_{off}	—	4.5	—	µs
Rise Time (I_F = 10 mA, V_{CC} = 10 V, R_L = 100 Ω)(3)		t_r	—	1.2	—	µs
Fall Time (I_F = 10 mA, V_{CC} = 10 V, R_L = 100 Ω)(3)		t_f	—	1.3	—	µs
Isolation Voltage (f = 60 Hz, t = 1 sec)(4)		V_{ISO}	7500	—	—	Vac(pk)
Isolation Resistance (V = 500 V)(4)		R_{ISO}	10^{11}	—	—	Ω
Isolation Capacitance (V = 0 V, f = 1 MHz)(4)		C_{ISO}	—	0.2	—	pF

1. Always design to the specified minimum/maximum electrical limits (where applicable).
2. Current Transfer Ratio (CTR) = I_C/I_F x 100%.
3. For test circuit setup and waveforms, refer to Figure 11.
4. For this test, Pins 1 and 2 are common, and Pins 4, 5 and 6 are common.

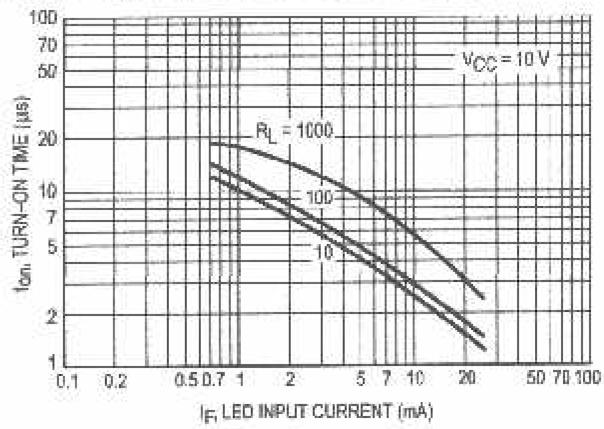


Figure 7. Turn–On Switching Times (Typical Values)

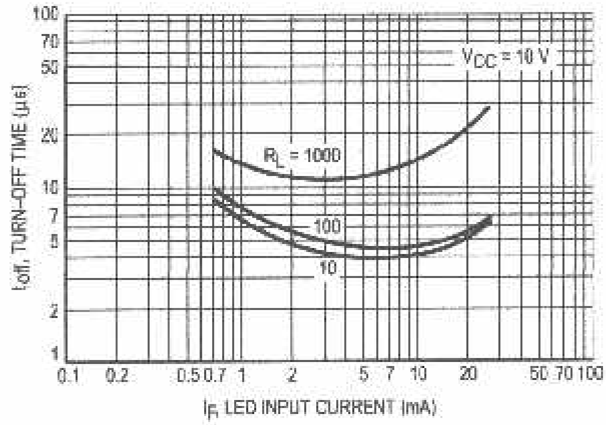


Figure 8. Turn–Off Switching Times (Typical Values)

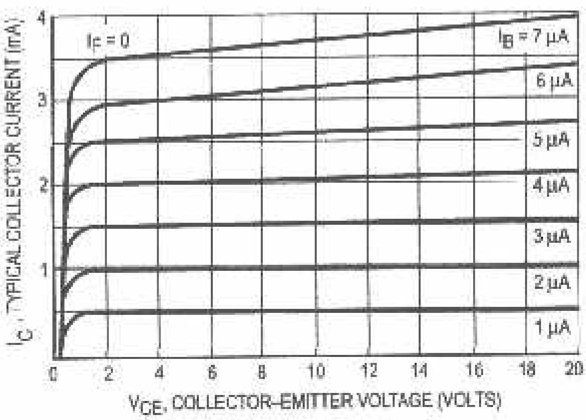


Figure 9. DC Current Gain (Detector Only)

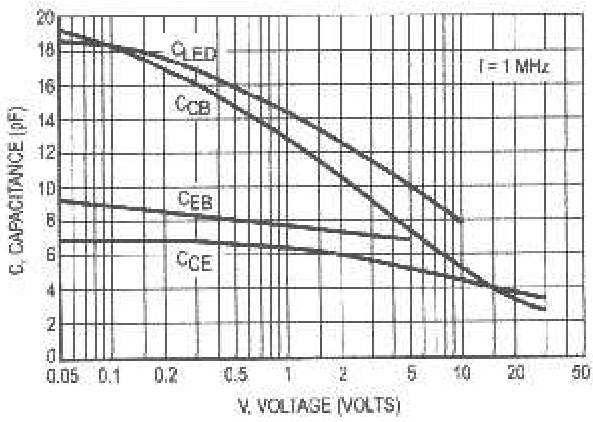


Figure 10. Capacitances versus Voltage

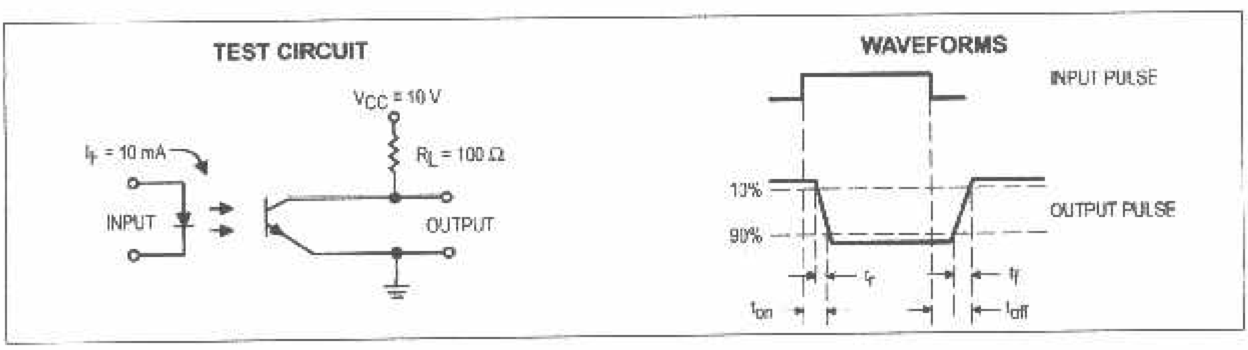


Figure 11. Switching Time Test Circuit and Waveforms

Special Function Registers

A map of the on-chip memory area called the Special Function Register (SFR) space is shown in Table 1.

Note that not all of the addresses are occupied, and unoccupied addresses may not be implemented on the chip. Read accesses to these addresses will in general return random data, and write accesses will have an indeterminate effect.

User software should not write 1s to these unlisted locations, since they may be used in future products to invoke new features. In that case, the reset or inactive values of the new bits will always be 0.

Timer 2 Registers Control and status bits are contained in registers T2CON (shown in Table 2) and T2MOD (shown in Table 9) for Timer 2. The register pair (RCAP2H, RCAP2L) are the Capture/Reload registers for Timer 2 in 16 bit capture mode or 16-bit auto-reload mode.

Table 2. T2CON—Timer/Counter 2 Control Register

T2CON Address = 0C8H Reset Value = 0000 0000B

Bit Addressable

	TF2	EXF2	RCLK	TCLK	EXEN2	TR2	$C/\overline{T2}$	$CP/\overline{RL2}$
Bit	7	6	5	4	3	2	1	0

Symbol	Function
TF2	Timer 2 overflow flag set by a Timer 2 overflow and must be cleared by software. TF2 will not be set when either RCLK = 1 or TCLK = 1.
EXF2	Timer 2 external flag set when either a capture or reload is caused by a negative transition on T2EX and EXEN2 = 1. When Timer 2 interrupt is enabled, EXF2 = 1 will cause the CPU to vector to the Timer 2 interrupt routine. EXF2 must be cleared by software. EXF2 does not cause an interrupt in up/down counter mode (DCEN = 1).
RCLK	Receive clock enable. When set, causes the serial port to use Timer 2 overflow pulses for its receive clock in serial port Modes 1 and 3. RCLK = 0 causes Timer 1 overflows to be used for the receive clock.
TCLK	Transmit clock enable. When set, causes the serial port to use Timer 2 overflow pulses for its transmit clock in serial port Modes 1 and 3. TCLK = 0 causes Timer 1 overflows to be used for the transmit clock.
EXEN2	Timer 2 external enable. When set, allows a capture or reload to occur as a result of a negative transition on T2EX if Timer 2 is not being used to clock the serial port. EXEN2 = 0 causes Timer 2 to ignore events at T2EX.
TR2	Start/Stop control for Timer 2. TR2 = 1 starts the timer.
$C/\overline{T2}$	*Timer or counter select for Timer 2. $C/\overline{T2}$ = 0 for timer function. $C/\overline{T2}$ = 1 for external event counter (falling edge triggered).*
$CP/\overline{RL2}$	Capture/Reload select. $CP/\overline{RL2}$ = 1 causes captures to occur on negative transitions at T2EX if EXEN2 = 1. $CP/\overline{RL2}$ = 0 causes automatic reloads to occur when Timer 2 overflows or negative transitions occur at T2EX when EXEN2 = 1. When either RCLK or TCLK = 1, this bit is ignored and the timer is forced to auto-reload on Timer 2 overflow.

Watchdog and Memory Control Register The WMCON register contains control bits for the Watchdog Timer (shown in Table 3). The EEMEN and EEMWE bits are used to select the 2K bytes on-chip EEPROM, and to enable byte-write. The DPS bit selects one of two DPTR registers available.

Table 3. WMCON—Watchdog and Memory Control Register

WMCON Address = 96H Reset Value = 0000 0010B

	PS2	PS1	PS0	EEMWE	EEMEN	DPS	WDTRST	WDTEN
Bit	7	6	5	4	3	2	1	0

Symbol	Function
PS2 PS1 PS0	Prescaler Bits for the Watchdog Timer. When all three bits are set to "0", the watchdog timer has a nominal period of 16 ms. When all three bits are set to "1", the nominal period is 2048 ms.
EEMWE	EEPROM Data Memory Write Enable Bit. Set this bit to "1" before initiating byte write to on-chip EEPROM with the MOVX instruction. User software should set this bit to "0" after EEPROM write is completed.
EEMEN	Internal EEPROM Access Enable. When EEMEN = 1, the MOVX instruction with DPTR will access on-chip EEPROM instead of external data memory. When EEMEN = 0, MOVX with DPTR accesses external data memory.
DPS	Data Pointer Register Select. DPS = 0 selects the first bank of Data Pointer Register, DP0, and DPS = 1 selects the second bank, DP1
WDTRST RDY/$\overline{BSY}$	Watchdog Timer Reset and EEPROM Ready/$\overline{Busy}$ Flag. Each time this bit is set to "1" by user software, a pulse is generated to reset the watchdog timer. The WDTRST bit is then automatically reset to "0" in the next instruction cycle. The WDTRST bit is Write-Only. This bit also serves as the RDY/$\overline{BSY}$ flag in a Read-Only mode during EEPROM write. RDY/$\overline{BSY}$ = 1 means that the EEPROM is ready to be programmed. While programming operations are being executed, the RDY/$\overline{BSY}$ bit equals "0" and is automatically reset to "1" when programming is completed.
WDTEN	Watchdog Timer Enable Bit. WDTEN = 1 enables the watchdog timer and WDTEN = 0 disables the watchdog timer.

SPI Registers Control and status bits for the Serial Peripheral Interface are contained in registers SPCR (shown in Table 4) and SPSR (shown in Table 5). The SPI data bits are contained in the SPDR register. Writing the SPI data register during serial data transfer sets the Write Collision bit, WCOL, in the SPSR register. The SPDR is double buffered for writing and the values in SPDR are not changed by Reset.

Interrupt Registers The global interrupt enable bit and the individual interrupt enable bits are in the IE register. In addition, the individual interrupt enable bit for the SPI is in the SPCR register. Two priorities can be set for each of the six interrupt sources in the IP register.

Dual Data Pointer Registers To facilitate accessing both internal EEPROM and external data memory, two banks of 16 bit Data Pointer Registers are provided: DP0 at SFR address locations 82H-83H and DP1 at 84H-85H. Bit DPS = 0 in SFR WMCON selects DP0 and DPS = 1 selects DP1. The user should always initialize the DPS bit to the appropriate value before accessing the respective Data Pointer Register.

Power Off Flag The Power Off Flag (POF) is located at bit_4 (PCON.4) in the PCON SFR. POF is set to "1" during power up. It can be set and reset under software control and is not affected by RESET.

Table 4. SPCR—SPI Control Register

SPCR Address = D5H Reset Value = 0000 01XXB

	SPIE	SPE	DORD	MSTR	CPOL	CPHA	SPR1	SPR0
Bit	7	6	5	4	3	2	1	0

Symbol	Function
SPIE	SPI Interrupt Enable. This bit, in conjunction with the ES bit in the IE register, enables SPI interrupts: SPIE = 1 and ES = 1 enable SPI interrupts. SPIE = 0 disables SPI interrupts.
SPE	SPI Enable. SPI = 1 enables the SPI channel and connects $\overline{SS}$, MOSI, MISO and SCK to pins P1.4, P1.5, P1.6, and P1.7. SPI = 0 disables the SPI channel.
DORD	Data Order. DORD = 1 selects LSB first data transmission. DORD = 0 selects MSB first data transmission.
MSTR	Master/Slave Select. MSTR = 1 selects Master SPI mode. MSTR = 0 selects Slave SPI mode.
CPOL	Clock Polarity. When CPOL = 1, SCK is high when idle. When CPOL = 0, SCK of the master device is low when not transmitting. Please refer to figure on SPI Clock Phase and Polarity Control.
CPHA	Clock Phase. The CPHA bit together with the CPOL bit controls the clock and data relationship between master and slave. Please refer to figure on SPI Clock Phase and Polarity Control.
SPR0 SPR1	SPI Clock Rate Select. These two bits control the SCK rate of the device configured as master. SPR1 and SPR0 have no effect on the slave. The relationship between SCK and the oscillator frequency, F_{OSC}, is as follows: SPR1 SPR0 SCK = F_{OSC} divided by 0 0 4 0 1 16 1 0 64 1 1 128

Table 5. SPSR – SPI Status Register

SPSR Address = AAH Reset Value = 00XX XXXXB

	SPIF	WCOL	–	–	–	–	–	–
Bit	7	6	5	4	3	2	1	0

Symbol	Function
SPIF	SPI Interrupt Flag. When a serial transfer is complete, the SPIF bit is set and an interrupt is generated if SPIE = 1 and ES = 1. The SPIF bit is cleared by reading the SPI status register with SPIF and WCOL bits set, and then accessing the SPI data register.
WCOL	Write Collision Flag. The WCOL bit is set if the SPI data register is written during a data transfer. During data transfer, the result of reading the SPDR register may be incorrect, and writing to it has no effect. The WCOL bit (and the SPIF bit) are cleared by reading the SPI status register with SPIF and WCOL set, and then accessing the SPI data register.

Table 6. SPDR – SPI Data Register

SPDR Address = 86H Reset Value = unchanged

	SPD7	SPD6	SPD5	SPD4	SPD3	SPD2	SPD1	SPD0
Bit	7	6	5	4	3	2	1	0

Data Memory – EEPROM and RAM

The AT89S8252 implements 2K bytes of on-chip EEPROM for data storage and 256 bytes of RAM. The upper 128 bytes of RAM occupy a parallel space to the Special Function Registers. That means the upper 128 bytes have the same addresses as the SFR space but are physically separate from SFR space.

When an instruction accesses an internal location above address 7FH, the address mode used in the instruction specifies whether the CPU accesses the upper 128 bytes of RAM or the SFR space. Instructions that use direct addressing access SFR space.

For example, the following direct addressing instruction accesses the SFR at location 0A0H (which is P2).

```
MOV 0A0H, #data
```

Instructions that use indirect addressing access the upper 128 bytes of RAM. For example, the following indirect addressing instruction, where R0 contains 0A0H, accesses the data byte at address 0A0H, rather than P2 (whose address is 0A0H).

```
MOV @R0, #data
```

Note that stack operations are examples of indirect addressing, so the upper 128 bytes of data RAM are available as stack space.

The on-chip EEPROM data memory is selected by setting the EEMEN bit in the WMCON register at SFR address location 96H. The EEPROM address range is from 000H to 7FFH. The MOVX instructions are used to access the EEPROM. To access off-chip data memory with the MOVX instructions, the EEMEN bit needs to be set to "0".

The EEMWE bit in the WMCON register needs to be set to "1" before any byte location in the EEPROM can be written. User software should reset EEMWE bit to "0" if no further EEPROM write is required. EEPROM write cycles in the serial programming mode are self-timed and typically take 2.5 ms. The progress of EEPROM write can be monitored by reading the RDY/$\overline{BSY}$ bit (read-only) in SFR WMCON. RDY/$\overline{BSY}$ = 0 means programming is still in progress and RDY/$\overline{BSY}$ = 1 means EEPROM write cycle is completed and another write cycle can be initiated.

In addition, during EEPROM programming, an attempted read from the EEPROM will fetch the byte being written with the MSB complemented. Once the write cycle is completed, true data are valid at all bit locations.

Programmable Watchdog Timer

The programmable Watchdog Timer (WDT) operates from an independent oscillator. The prescaler bits, PS0, PS1 and PS2 in SFR WMCON are used to set the period of the Watchdog Timer from 16 ms to 2048 ms. The available timer periods are shown in the following table and the actual timer periods (at V_{CC} = 5V) are within ±30% of the nominal.

The WDT is disabled by Power-on Reset and during Power-down. It is enabled by setting the WDTEN bit in SFR WMCON (address = 96H). The WDT is reset by setting the WDTRST bit in WMCON. When the WDT times out without being reset or disabled, an internal RST pulse is generated to reset the CPU.

Table 7. Watchdog Timer Period Selection

WDT Prescaler Bits			
PS2	PS1	PS0	Period (nominal)
0	0	0	16 ms
0	0	1	32 ms
0	1	0	64 ms
0	1	1	128 ms
1	0	0	256 ms
1	0	1	512 ms
1	1	0	1024 ms
1	1	1	2048 ms

Timer 0 and 1

Timer 0 and Timer 1 in the AT89S8252 operate the same way as Timer 0 and Timer 1 in the AT89C51, AT89C52 and AT89C55. For further information, see the October 1995 Microcontroller Data Book, page 2-45, section titled, "Timer/Counters."

Timer 2

Timer 2 is a 16 bit Timer/Counter that can operate as either a timer or an event counter. The type of operation is selected by bit C/$\overline{T2}$ in the SFR T2CON (shown in Table 2). Timer 2 has three operating modes: capture, auto-reload (up or down counting), and baud rate generator. The modes are selected by bits in T2CON, as shown in Table 8.

Timer 2 consists of two 8-bit registers, TH2 and TL2. In the Timer function, the TL2 register is incremented every machine cycle. Since a machine cycle consists of 12 oscillator periods, the count rate is 1/12 of the oscillator frequency.

In the Counter function, the register is incremented in response to a 1-to-0 transition at its corresponding external input pin, T2. In this function, the external input is sampled during S5P2 of every machine cycle. When the samples show a high in one cycle and a low in the next cycle, the count is incremented. The new count value appears in the register during S3P1 of the cycle following the one in which the transition was detected. Since two machine cycles (24 oscillator periods) are required to recognize a 1-to-0 transition, the maximum count rate is 1/24 of the oscillator frequency. To ensure that a given level is sampled at least once before it changes, the level should be held for at least one full machine cycle.

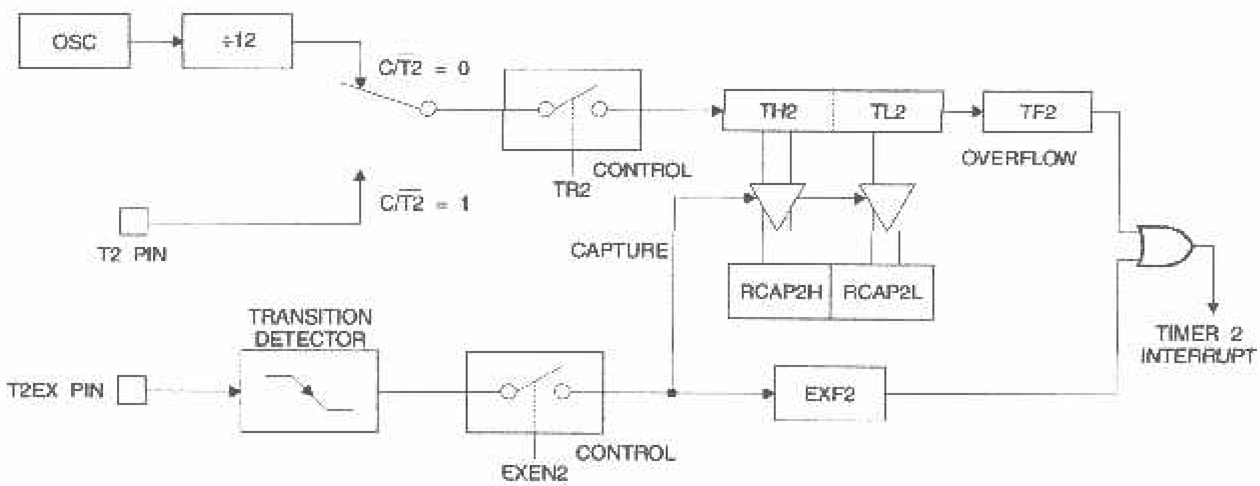
Table 8. Timer 2 Operating Modes

RCLK + TCLK	CP/$\overline{RL2}$	TR2	MODE
0	0	1	16-bit Auto-reload
0	1	1	16-bit Capture
1	X	1	Baud Rate Generator
X	X	0	(Off)

Capture Mode

In the capture mode, two options are selected by bit EXEN2 in T2CON. If EXEN2 = 0, Timer 2 is a 16 bit timer or counter which upon overflow sets bit TF2 in T2CON. This bit can then be used to generate an interrupt. If EXEN2 = 1, Timer 2 performs the same operation, but a 1-to-0 transition at external input T2EX also causes the current value in TH2 and TL2 to be captured into RCAP2H and RCAP2L, respectively. In addition, the transition at T2EX causes bit EXF2 in T2CON to be set. The EXF2 bit, like TF2, can generate an interrupt. The capture mode is illustrated in Figure 1.

Figure 1. Timer 2 in Capture Mode



Auto-reload (Up or Down Counter)

Timer 2 can be programmed to count up or down when configured in its 16 bit auto-reload mode. This feature is invoked by the DCEN (Down Counter Enable) bit located in the SFR T2MOD (see Table 9). Upon reset, the DCEN bit is set to 0 so that timer 2 will default to count up. When DCEN is set, Timer 2 can count up or down, depending on the value of the T2EX pin.

Figure 2 shows Timer 2 automatically counting up when DCEN = 0. In this mode, two options are selected by bit EXEN2 in T2CON. If EXEN2 = 0, Timer 2 counts up to 0FFFFH and then sets the TF2 bit upon overflow. The overflow also causes the timer registers to be reloaded with the 16 bit value in RCAP2H and RCAP2L. The values in RCAP2H and RCAP2L are preset by software. If EXEN2 = 1, a 16 bit reload can be triggered either by an overflow or by a 1-to-0 transition at external input T2EX. This transition also sets the EXF2 bit. Both the TF2 and EXF2 bits can generate an interrupt if enabled.

Setting the DCEN bit enables Timer 2 to count up or down, as shown in Figure 3. In this mode, the T2EX pin controls the direction of the count. A logic 1 at T2EX makes Timer 2 count up. The timer will overflow at 0FFFFH and set the TF2 bit. This overflow also causes the 16 bit value in RCAP2H and RCAP2L to be reloaded into the timer registers, TH2 and TL2, respectively.

A logic 0 at T2EX makes Timer 2 count down. The timer underflows when TH2 and TL2 equal the values stored in RCAP2H and RCAP2L. The underflow sets the TF2 bit and causes 0FFFFH to be reloaded into the timer registers.

The EXF2 bit toggles whenever Timer 2 overflows or underflows and can be used as a 17th bit of resolution. In this operating mode, EXF2 does not flag an interrupt.

Figure 2. Timer 2 in Auto Reload Mode (DCEN = 0)

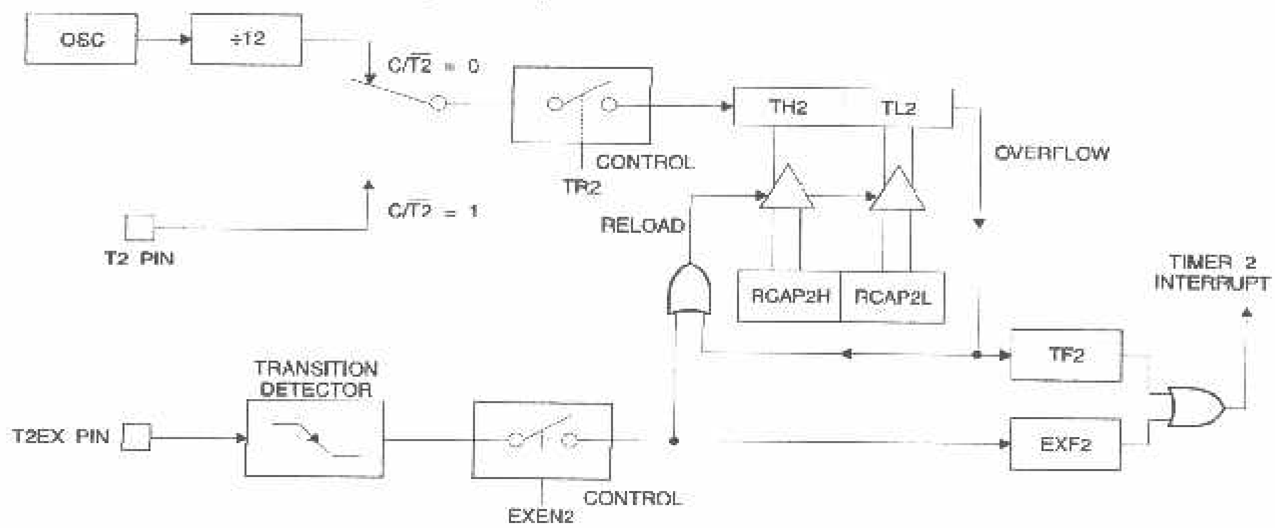


Table 9. T2MOD – Timer 2 Mode Control Register

T2MOD Address = 0C9H								Reset Value = XXXX XX00B
Not Bit Addressable								
	–	–	–	–	–	–	T2OE	DCEN
Bit	7	6	5	4	3	2	1	0

Symbol	Function
–	Not implemented, reserved for future use.
T2OE	Timer 2 Output Enable bit.
DCEN	When set, this bit allows Timer 2 to be configured as an up/down counter.

Figure 3. Timer 2 Auto Reload Mode (DCEN = 1)

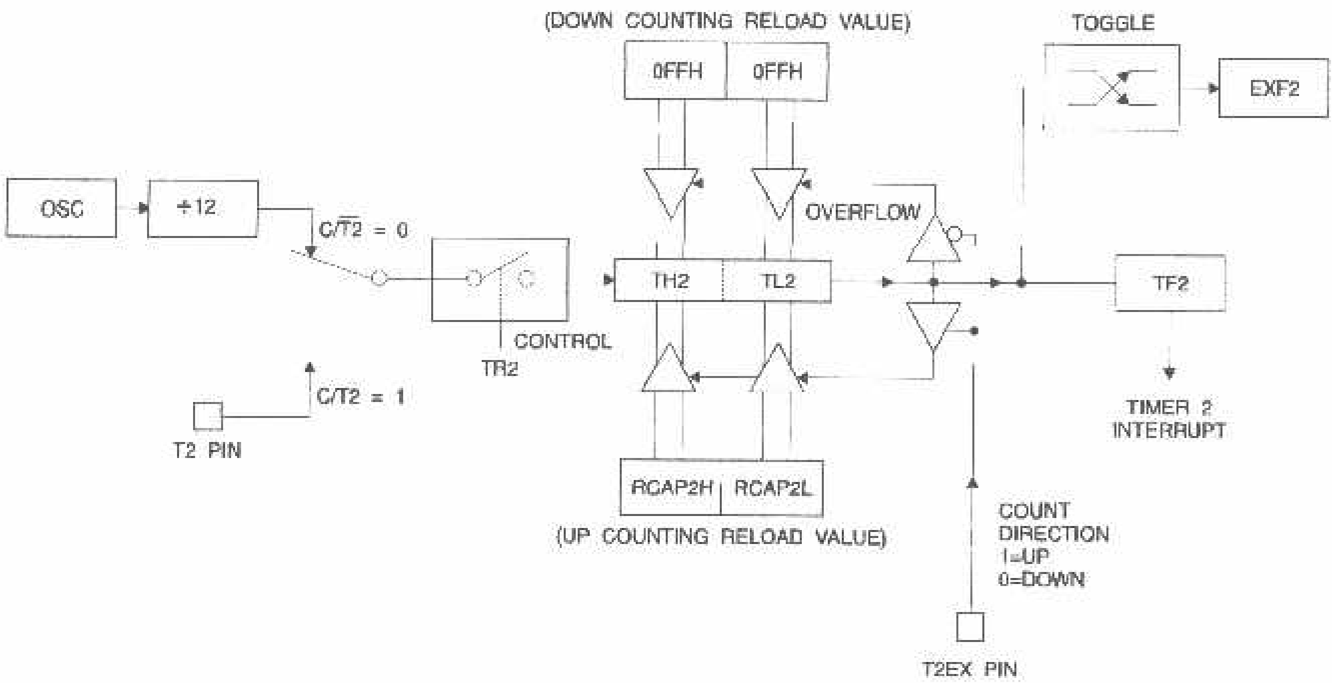
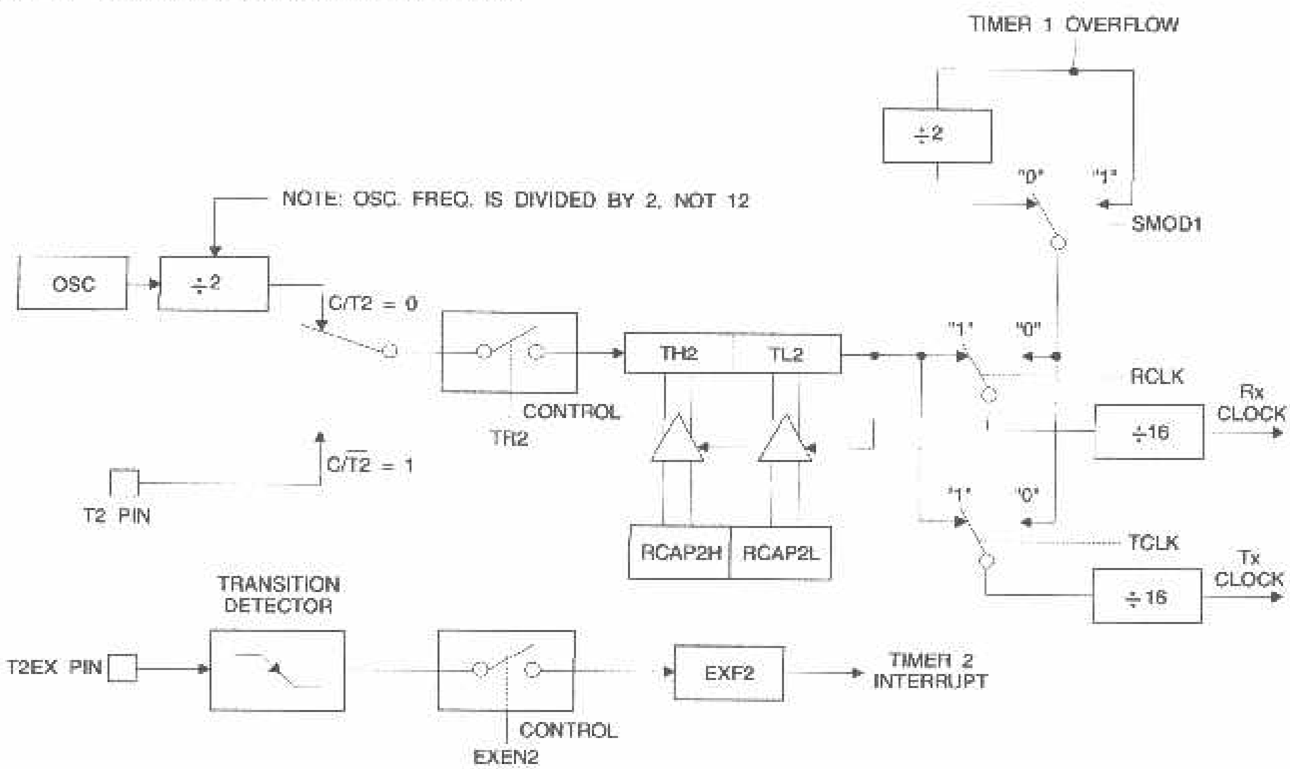


Figure 4. Timer 2 in Baud Rate Generator Mode



Baud Rate Generator

Timer 2 is selected as the baud rate generator by setting TCLK and/or RCLK in T2CON (Table 2). Note that the baud rates for transmit and receive can be different if Timer 2 is used for the receiver or transmitter and Timer 1 is used for the other function. Setting RCLK and/or TCLK puts Timer 2 into its baud rate generator mode, as shown in Figure 4.

The baud rate generator mode is similar to the auto-reload mode, in that a rollover in TH2 causes the Timer 2 registers to be reloaded with the 16 bit value in registers RCAP2H and RCAP2L, which are preset by software.

The baud rates in Modes 1 and 3 are determined by Timer 2's overflow rate according to the following equation.

$$\text{Modes 1 and 3 Baud Rates} = \frac{\text{Timer 2 Overflow Rate}}{16}$$

The Timer can be configured for either timer or counter operation. In most applications, it is configured for timer operation ($CP/\overline{T2} = 0$). The timer operation is different for Timer 2 when it is used as a baud rate generator. Normally, as a timer, it increments every machine cycle (at 1/12 the oscillator frequency). As a baud rate generator, however, it increments every state time (at 1/2 the oscillator frequency). The baud rate formula is given below.

$$\frac{\text{Modes 1 and 3}}{\text{Baud Rate}} = \frac{\text{Oscillator Frequency}}{32 \times [65536 - (\text{RCAP2H,RCAP2L})]}$$

where (RCAP2H, RCAP2L) is the content of RCAP2H and RCAP2L taken as a 16 bit unsigned integer.

Timer 2 as a baud rate generator is shown in Figure 4. This figure is valid only if RCLK or TCLK = 1 in T2CON. Note that a rollover in TH2 does not set TF2 and will not generate an interrupt. Note too, that if EXEN2 is set, a 1-to-0 transition in T2EX will set EXF2 but will not cause a reload from (RCAP2H, RCAP2L) to (TH2, TL2). Thus when Timer 2 is in use as a baud rate generator, T2EX can be used as an extra external interrupt.

Note that when Timer 2 is running (TR2 = 1) as a timer in the baud rate generator mode, TH2 or TL2 should not be read from or written to. Under these conditions, the Timer is incremented every state time, and the results of a read or write may not be accurate. The RCAP2 registers may be read but should not be written to, because a write might overlap a reload and cause write and/or reload errors. The timer should be turned off (clear TR2) before accessing the Timer 2 or RCAP2 registers.

Programmable Clock Out

A 50% duty cycle clock can be programmed to come out on P1.0, as shown in Figure 5. This pin, besides being a regular I/O pin, has two alternate functions. It can be programmed to input the external clock for Timer/Counter 2 or to output a 50% duty cycle clock ranging from 61 Hz to 4 MHz at a 16 MHz operating frequency.

To configure the Timer/Counter 2 as a clock generator, bit $C/\overline{T2}$ (T2CON.1) must be cleared and bit T2OE (T2MOD.1) must be set. Bit TR2 (T2CON.2) starts and stops the timer.

The clock-out frequency depends on the oscillator frequency and the reload value of Timer 2 capture registers (RCAP2H, RCAP2L), as shown in the following equation.

$$\text{Clock Out Frequency} = \frac{\text{Oscillator Frequency}}{4 \times [65536 - (\text{RCAP2H,RCAP2L})]}$$

In the clock-out mode, Timer 2 rollovers will not generate an interrupt. This behavior is similar to when Timer 2 is used as a baud-rate generator. It is possible to use Timer 2 as a baud-rate generator and a clock generator simultaneously. Note, however, that the baud-rate and clock-out frequencies cannot be determined independently from one another since they both use RCAP2H and RCAP2L.

Figure 5. Timer 2 in Clock-out Mode

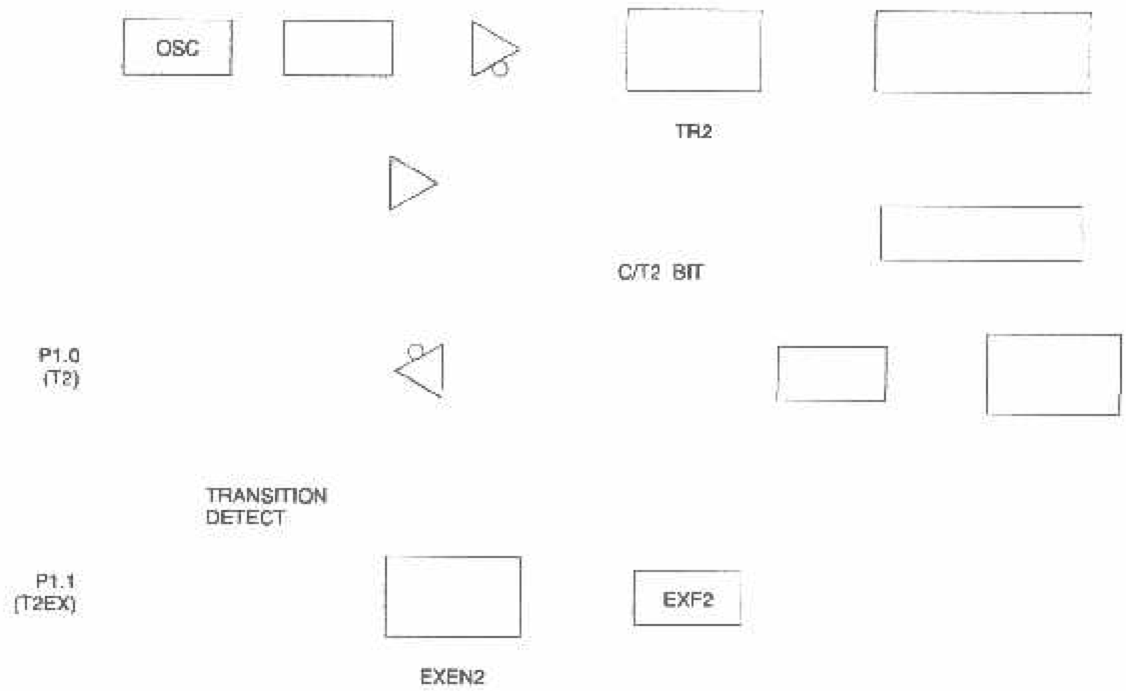


Figure 6. SPI Block Diagram

UART

The UART in the AT89S8252 operates the same way as the UART in the AT89C51, AT89C52 and AT89C55. For further information, see the October 1995 Microcontroller Data Book, page 2-49, section titled, "Serial Interface."

Serial Peripheral Interface

The serial peripheral interface (SPI) allows high-speed synchronous data transfer between the AT89S8252 and peripheral devices or between several AT89S8252 devices. The AT89S8252 SPI features include the following:

- Full-Duplex, 3-Wire Synchronous Data Transfer
- Master or Slave Operation
- 1.5 MHz Bit Frequency (max.)
- LSB First or MSB First Data Transfer
- Four Programmable Bit Rates
- End of Transmission Interrupt Flag
- Write Collision Flag Protection
- Wakeup from Idle Mode (Slave Mode Only)

The interconnection between master and slave CPUs with SPI is shown in the following figure. The SCK pin is the clock output in the master mode but is the clock input in the slave mode. Writing to the SPI data register of the master CPU starts the SPI clock generator, and the data written shifts out of the MOSI pin and into the MOSI pin of the slave CPU. After shifting one byte, the SPI clock generator stops, setting the end of transmission flag (SPIF). If both the SPI interrupt enable bit (SPIE) and the serial port interrupt enable bit (ES) are set, an interrupt is requested.

The Slave Select input, $\overline{SS}$/P1.4, is set low to select an individual SPI device as a slave. When $\overline{SS}$/P1.4 is set high, the SPI port is deactivated and the MOSI/P1.5 pin can be used as an input.

There are four combinations of SCK phase and polarity with respect to serial data, which are determined by control bits CPHA and CPOL. The SPI data transfer formats are shown in Figure 8 and Figure 9.

Figure 7. SPI Master-slave Interconnection

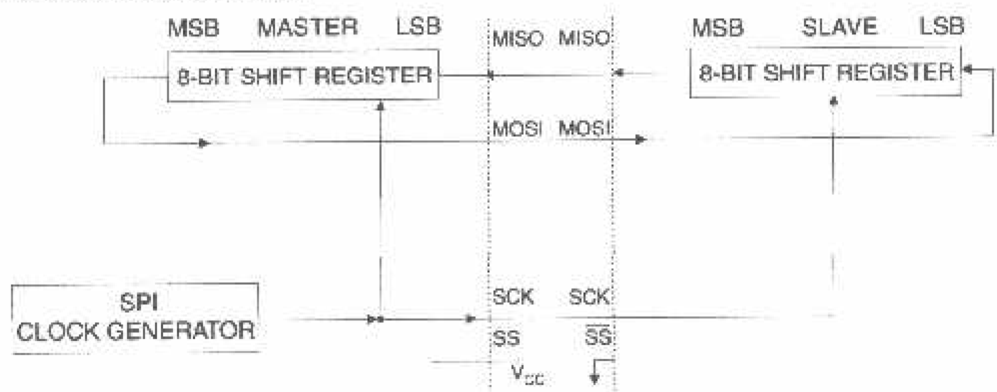
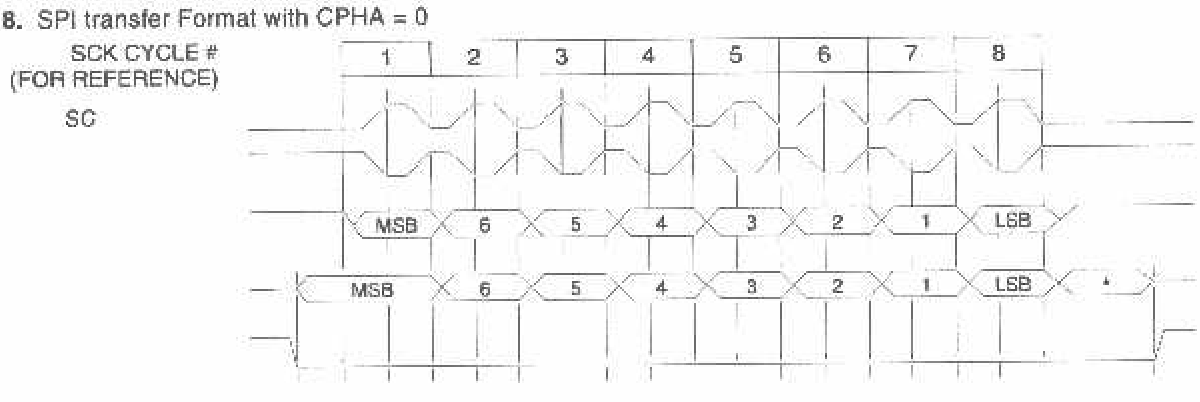
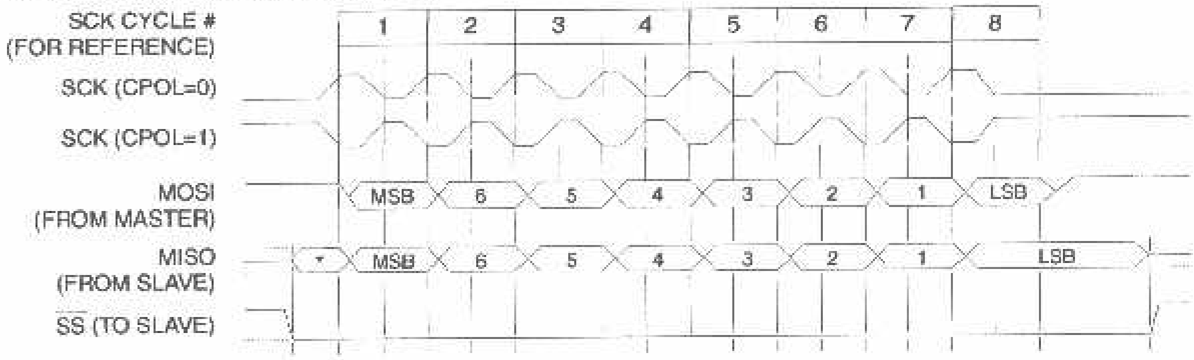


Figure 8. SPI transfer Format with CPHA = 0



*Not defined but normally MSB of character just received

Figure 9. SPI Transfer Format with CPHA = 1



*Not defined but normally LSB of previously transmitted character

Interrupts

The AT89S8252 has a total of six interrupt vectors: two external interrupts ($\overline{INT0}$ and $\overline{INT1}$), three timer interrupts (Timers 0, 1, and 2), and the serial port interrupt. These interrupts are all shown in Figure 10.

Each of these interrupt sources can be individually enabled or disabled by setting or clearing a bit in Special Function Register IE. IE also contains a global disable bit, EA, which disables all interrupts at once.

Note that Table 10 shows that bit position IE.6 is unimplemented. In the AT89C51, bit position IE.5 is also unimplemented. User software should not write 1s to these bit positions, since they may be used in future AT89 products.

Timer 2 interrupt is generated by the logical OR of bits TF2 and EXF2 in register T2CON. Neither of these flags is cleared by hardware when the service routine is vectored to. In fact, the service routine may have to determine whether it was TF2 or EXF2 that generated the interrupt, and that bit will have to be cleared in software.

The Timer 0 and Timer 1 flags, TF0 and TF1, are set at S5P2 of the cycle in which the timers overflow. The values are then polled by the circuitry in the next cycle. However, the Timer 2 flag, TF2, is set at S2P2 and is polled in the same cycle in which the timer overflows.

Table 10. Interrupt Enable (IE) Register

(MSB)(LSB)

EA	–	ET2	ES	ET1	EX1	ET0	EX0

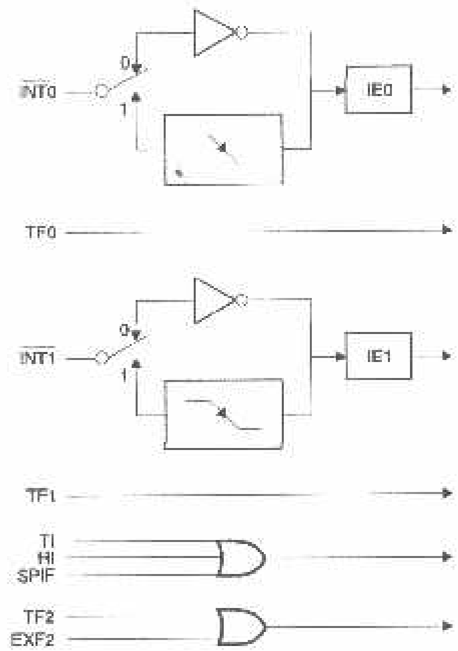
Enable Bit = 1 enables the interrupt.

Enable Bit = 0 disables the interrupt.

Symbol	Position	Function
EA	IE.7	Disables all interrupts. If EA = 0, no interrupt is acknowledged. If EA = 1, each interrupt source is individually enabled or disabled by setting or clearing its enable bit.
–	IE.6	Reserved.
ET2	IE.5	Timer 2 interrupt enable bit.
ES	IE.4	SPI and UART interrupt enable bit.
ET1	IE.3	Timer 1 interrupt enable bit.
EX1	IE.2	External interrupt 1 enable bit.
ET0	IE.1	Timer 0 interrupt enable bit.
EX0	IE.0	External interrupt 0 enable bit.

User software should never write 1s to unimplemented bits, because they may be used in future AT89 products.

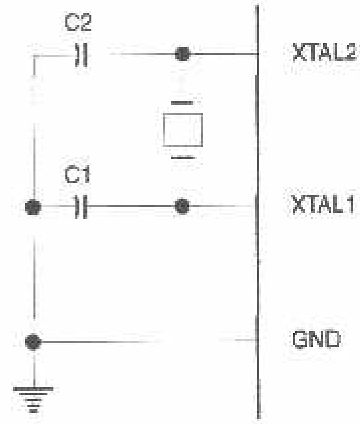
Figure 10. Interrupt Sources



Oscillator Characteristics

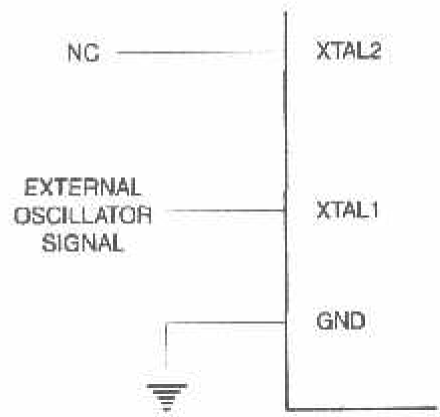
XTAL1 and XTAL2 are the input and output, respectively, of an inverting amplifier that can be configured for use as an on-chip oscillator, as shown in Figure 11. Either a quartz crystal or ceramic resonator may be used. To drive the device from an external clock source, XTAL2 should be left unconnected while XTAL1 is driven, as shown in Figure 12. There are no requirements on the duty cycle of the external clock signal, since the input to the internal clocking circuitry is through a divide-by-two flip-flop, but minimum and maximum voltage high and low time specifications must be observed.

Figure 11. Oscillator Connections



Note: Note: C1, C2 = 30 pF ± 10 pF for Crystals
= 40 pF ± 10 pF for Ceramic Resonators

Figure 12. External Clock Drive Configuration



Idle Mode

In idle mode, the CPU puts itself to sleep while all the on-chip peripherals remain active. The mode is invoked by software. The content of the on-chip RAM and all the special functions registers remain unchanged during this mode. The idle mode can be terminated by any enabled interrupt or by a hardware reset.

Note that when idle mode is terminated by a hardware reset, the device normally resumes program execution from where it left off, up to two machine cycles before the internal reset algorithm takes control. On-chip hardware inhibits access to internal RAM in this event, but access to the port pins is not inhibited. To eliminate the possibility of an unexpected write to a port pin when idle mode is terminated by a reset, the instruction following the one that invokes idle mode should not write to a port pin or to external memory.

Status of External Pins During Idle and Power-down Modes

Mode	Program Memory	ALE	$\overline{PSEN}$	PORT0	PORT1	PORT2	PORT3
Idle	Internal	1	1	Data	Data	Data	Data
Idle	External	1	1	Float	Data	Address	Data
Power-down	Internal	0	0	Data	Data	Data	Data
Power-down	External	0	0	Float	Data	Data	Data

Power-down Mode

In the power-down mode, the oscillator is stopped and the instruction that invokes power-down is the last instruction executed. The on-chip RAM and Special Function Registers retain their values until the power-down mode is terminated. Exit from power-down can be initiated either by a hardware reset or by an enabled external interrupt. Reset redefines the SFRs but does not change the on-chip RAM. The reset should not be activated before V_{CC} is restored to its normal operating level and must be held active long enough to allow the oscillator to restart and stabilize.

To exit power-down via an interrupt, the external interrupt must be enabled as level sensitive before entering power-down. The interrupt service routine starts at 16 ms (nominal) after the enabled interrupt pin is activated.

Program Memory Lock Bits

The AT89S8252 has three lock bits that can be left unprogrammed (U) or can be programmed (P) to obtain the additional features listed in the following table.

When lock bit 1 is programmed, the logic level at the $\overline{EA}$ pin is sampled and latched during reset. If the device is powered up without a reset, the latch initializes to a random value and holds that value until reset is activated. The latched value of $\overline{EA}$ must agree with the current logic level at that pin in order for the device to function properly.

Once programmed, the lock bits can only be unprogrammed with the Chip Erase operations in either the parallel or serial modes.

Lock Bit Protection Modes[1][2]

	Program Lock Bits			
	LB1	LB2	LB3	Protection Type
1	U	U	U	No internal memory lock feature.
2	P	U	U	MOVC instructions executed from external program memory are disabled from fetching code bytes from internal memory. $\overline{EA}$ is sampled and latched on reset and further programming of the Flash memory (parallel or serial mode) is disabled.
3	P	P	U	Same as Mode 2, but parallel or serial verify are also disabled.
4	P	P	P	Same as Mode 3, but external execution is also disabled.

Notes: 1. U = Unprogrammed
2. P = Programmed

Programming the Flash and EEPROM

Atmel's AT89S8252 Flash Microcontroller offers 8K bytes of in-system reprogrammable Flash Code memory and 2K bytes of EEPROM Data memory.

The AT89S8252 is normally shipped with the on-chip Flash Code and EEPROM Data memory arrays in the erased state (i.e. contents = FFH) and ready to be programmed. This device supports a High-voltage (12V) Parallel programming mode and a Low-voltage (5V) Serial programming mode. The serial programming mode provides a convenient way to download the AT89S8252 inside the user's system. The parallel programming mode is compatible with conventional third party Flash or EPROM programmers.

The Code and Data memory arrays are mapped via separate address spaces in the serial programming mode. In the parallel programming mode, the two arrays occupy one contiguous address space: 0000H to 1FFFH for the Code array and 2000H to 27FFH for the Data array.

The Code and Data memory arrays on the AT89S8252 are programmed byte-by-byte in either programming mode. An auto-erase cycle is provided with the self-timed programming operation in the serial programming mode. There is no need to perform the Chip Erase operation to reprogram any memory location in the serial programming mode unless any of the lock bits have been programmed.

In the parallel programming mode, there is no auto-erase cycle. To reprogram any non-blank byte, the user needs to use the Chip Erase operation first to erase both arrays.

Parallel Programming Algorithm: To program and verify the AT89S8252 in the parallel programming mode, the following sequence is recommended:

1. Power-up sequence:

   Apply power between V_{CC} and GND pins.

   Set RST pin to "H".

   Apply a 3 MHz to 24 MHz clock to XTAL1 pin and wait for at least 10 milliseconds.

2. Set $\overline{\text{PSEN}}$ pin to "L"

   ALE pin to "H"

   $\overline{\text{EA}}$ pin to "H" and all other pins to "H".

3. Apply the appropriate combination of "H" or "L" logic levels to pins P2.6, P2.7, P3.6, P3.7 to select one of the programming operations shown in the Flash Programming Modes table.

4. Apply the desired byte address to pins P1.0 to P1.7 and P2.0 to P2.5.

   Apply data to pins P0.0 to P0.7 for Write Code operation.

5. Raise $\overline{\text{EA}}/V_{PP}$ to 12V to enable Flash programming, erase or verification.

6. Pulse ALE/$\overline{\text{PROG}}$ once to program a byte in the Code memory array, the Data memory array or the lock bits. The byte-write cycle is self-timed and typically takes 1.5 ms.

7. To verify the byte just programmed, bring pin P2.7 to "L" and read the programmed data at pins P0.0 to P0.7.

8. Repeat steps 3 through 7 changing the address and data for the entire 2K or 8K bytes array or until the end of the object file is reached.

9. Power-off sequence:

   Set XTAL1 to "L".

   Set RST and $\overline{\text{EA}}$ pins to "L".

   Turn V_{CC} power off.

In the parallel programming mode, there is no auto-erase cycle and to reprogram any non-blank byte, the user needs to use the Chip Erase operation first to erase both arrays.

Data Polling: The AT89S8252 features $\overline{\text{DATA}}$ Polling to indicate the end of a write cycle. During a write cycle in the parallel or serial programming mode, an attempted read of the last byte written will result in the complement of the written datum on P0.7 (parallel mode), and on the MSB of the serial output byte on MISO (serial mode). Once the write cycle has been completed, true data are valid on all outputs, and the next cycle may begin. $\overline{\text{DATA}}$ Polling may begin any time after a write cycle has been initiated.

Ready/$\overline{\text{Busy}}$: The progress of byte programming in the parallel programming mode can also be monitored by the RDY/$\overline{\text{BSY}}$ output signal. Pin P3.4 is pulled Low after ALE goes High during programming to indicate $\overline{\text{BUSY}}$. P3.4 is pulled High again when programming is done to indicate READY.

Program Verify: If lock bits LB1 and LB2 have not been programmed, the programmed Code or Data byte can be read back via the address and data lines for verification. The state of the lock bits can also be verified directly in the parallel programming mode. In the serial programming mode, the state of the lock bits can only be verified indirectly by observing that the lock bit features are enabled.

Chip Erase: Both Flash and EEPROM arrays are erased electrically at the same time. In the parallel programming mode, chip erase is initiated by using the proper combination of control signals and by holding ALE/$\overline{\text{PROG}}$ low for 10 ms. The Code and Data arrays are written with all "1"s in the Chip Erase operation.

In the serial programming mode, a chip erase operation is initiated by issuing the Chip Erase instruction. In this mode, chip erase is self-timed and takes about 16 ms.

During chip erase, a serial read from any address location will return 00H at the data outputs.

Serial Programming Fuse: A programmable fuse is available to disable Serial Programming if the user needs maximum system security. The Serial Programming Fuse can only be programmed or erased in the Parallel Programming Mode.

The AT89S8252 is shipped with the Serial Programming Mode enabled.

Reading the Signature Bytes: The signature bytes are read by the same procedure as a normal verification of locations 030H and 031H, except that P3.6 and P3.7 must be pulled to a logic low. The values returned are as follows:

(030H) = 1EH indicates manufactured by Atmel
(031H) = 72H indicates 89S8252

Programming Interface

Every code byte in the Flash and EEPROM arrays can be written, and the entire array can be erased, by using the appropriate combination of control signals. The write operation cycle is self-timed and once initiated, will automatically time itself to completion.

All major programming vendors offer worldwide support for the Atmel microcontroller series. Please contact your local programming vendor for the appropriate software revision.

Serial Downloading

Both the Code and Data memory arrays can be programmed using the serial SPI bus while RST is pulled to V_{CC}. The serial interface consists of pins SCK, MOSI (input) and MISO (output). After RST is set high, the Programming Enable instruction needs to be executed first before program/erase operations can be executed.

An auto-erase cycle is built into the self-timed programming operation (in the serial mode ONLY) and there is no need to first execute the Chip Erase instruction unless any of the lock bits have been programmed. The Chip Erase operation turns the content of every memory location in both the Code and Data arrays into FFH.

The Code and Data memory arrays have separate address spaces:

0000H to 1FFFH for Code memory and 000H to 7FFH for Data memory.

Either an external system clock is supplied at pin XTAL1 or a crystal needs to be connected across pins XTAL1 and XTAL2. The maximum serial clock (SCK) frequency should be less than 1/40 of the crystal frequency. With a 24 MHz oscillator clock, the maximum SCK frequency is 600 kHz.

Serial Programming Algorithm

To program and verify the AT89S8252 in the serial programming mode, the following sequence is recommended:

1. Power-up sequence:

   Apply power between VCC and GND pins.

   Set RST pin to "H".

   If a crystal is not connected across pins XTAL1 and XTAL2, apply a 3 MHz to 24 MHz clock to XTAL1 pin and wait for at least 10 milliseconds.

2. Enable serial programming by sending the Programming Enable serial instruction to pin MOSI/P1.5. The frequency of the shift clock supplied at pin SCK/P1.7 needs to be less than the CPU clock at XTAL1 divided by 40.

3. The Code or Data array is programmed one byte at a time by supplying the address and data together with the appropriate Write instruction. The selected memory location is first automatically erased before new data is written. The write cycle is self-timed and typically takes less than 2.5 ms at 5V.

4. Any memory location can be verified by using the Read instruction which returns the content at the selected address at serial output MISO/P1.6.

5. At the end of a programming session, RST can be set low to commence normal operation.

Power-off sequence (*if needed*):

Set XTAL1 to "L" (if a crystal is not used).

Set RST to "L".

Turn V_{CC} power off.

Serial Programming Instruction

The Instruction Set for Serial Programming follows a 3-byte protocol and is shown in the following table:

Instruction Set

Instruction	Input Format			Operation
	Byte 1	Byte 2	Byte 3	
Programming Enable	1010 1100	0101 0011	xxxx xxxx	Enable serial programming interface after RST goes high.
Chip Erase	1010 1100	xxxx x100	xxxx xxxx	Chip erase both 8K & 2K memory arrays.
Read Code Memory	aaaa a001	low addr	xxxx xxxx	Read data from Code memory array at the selected address. The 5 MSBs of the first byte are the high order address bits. The low order address bits are in the second byte. Data are available at pin MISO during the third byte.
Write Code Memory	aaaa a010	low addr	data in	Write data to Code memory location at selected address. The address bits are the 5 MSBs of the first byte together with the second byte.
Read Data Memory	00aa a101	low addr	xxxx xxxx	Read data from Data memory array at selected address. Data are available at pin MISO during the third byte.
Write Data Memory	00aa a110	low addr	data in	Write data to Data memory location at selected address.
Write Lock Bits	1010 1100	x x111	xxxx xxxx	Write lock bits. *Set LB1, LB2 or LB3 = "0" to program lock bits.*

Note: 1. DATA polling is used to indicate the end of a write cycle which typically takes less than 2.5 ms at 5V.
2. "aaaaa" = high order address.
3. "x" = don't care.

Flash and EEPROM Parallel Programming Modes

Mode	RST	PSEN	ALE/PROG	EA/V_{PP}	P2.6	P2.7	P3.6	P3.7	Data I/O P0.7:0	Address P2.5:0 P1.7:0
Serial Prog. Modes	H	h[1]	h[1]	x						
Chip Erase	H	L	‾_/‾ (2)	12V	H	L	L	L	X	X
Write (10K bytes) Memory	H	L	‾_/‾	12V	L	H	H	H	DIN	ADDR
Read (10K bytes) Memory	H	L	H	12V	L	L	H	H	DOUT	ADDR
Write Lock Bits:	H	L	‾_/‾	12V	H	L	H	L	DIN	X
Bit - 1									P0.7 = 0	X
Bit - 2									P0.6 = 0	X
Bit - 3									P0.5 = 0	X
Read Lock Bits:	H	L	H	12V	H	H	L	L	DOUT	X
Bit - 1									@P0.2	X
Bit - 2									@P0.1	X
Bit - 3									@P0.0	X
Read Atmel Code	H	L	H	12V	L	L	L	L	DOUT	30H
Read Device Code	H	L	H	12V	L	L	L	L	DOUT	31H
Serial Prog. Enable	H	L	‾_/‾ (2)	12V	L	H	L	H	P0.0 = 0	X
Serial Prog. Disable	H	L	‾_/‾ (2)	12V	L	H	L	H	P0.0 = 1	X
Read Serial Prog. Fuse	H	L	H	12V	H	H	L	H	@P0.0	X

Notes:
1. "h" = weakly pulled "High" internally.
2. Chip Erase and Serial Programming Fuse require a 10 ms PROG pulse. Chip Erase needs to be performed first before reprogramming any byte with a content other than FFH.
3. P3.4 is pulled Low during programming to indicate RDY/BSY.
4. "X" = don't care

Figure 13. Programming the Flash/EEPROM Memory

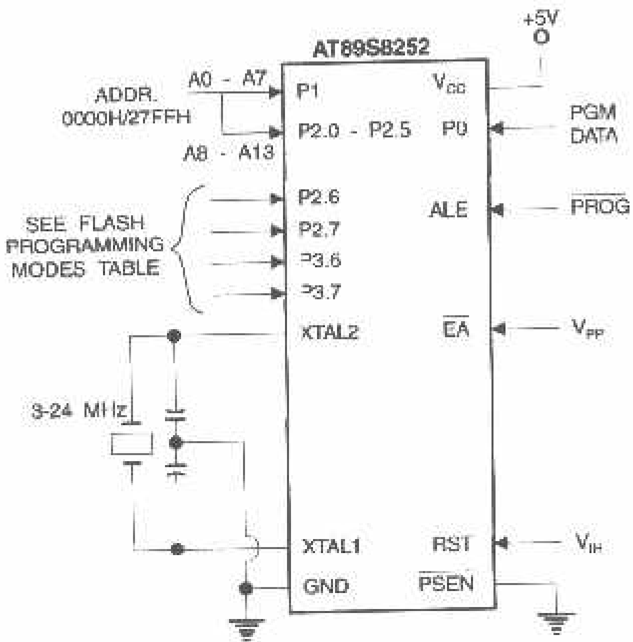


Figure 14. Verifying the Flash/EEPROM Memory

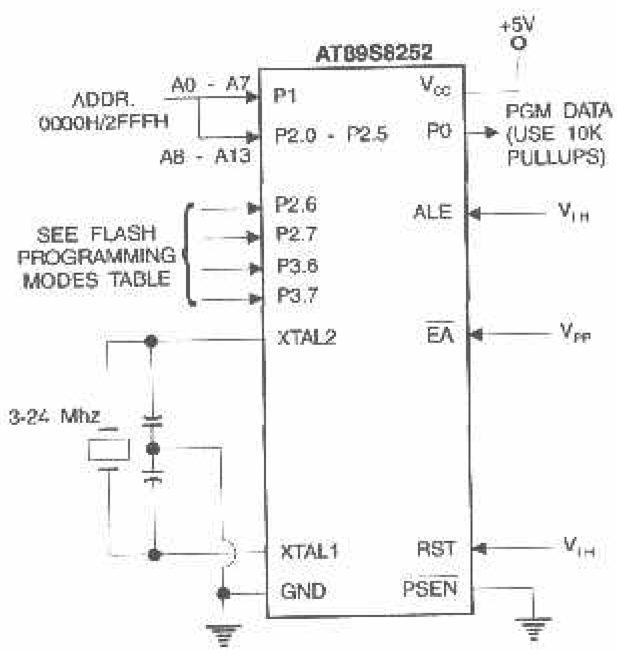
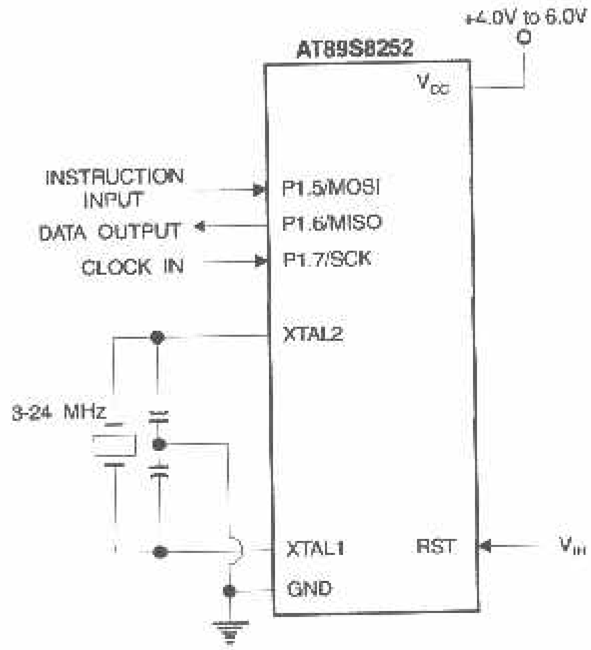


Figure 15. Flash/EEPROM Serial Downloading

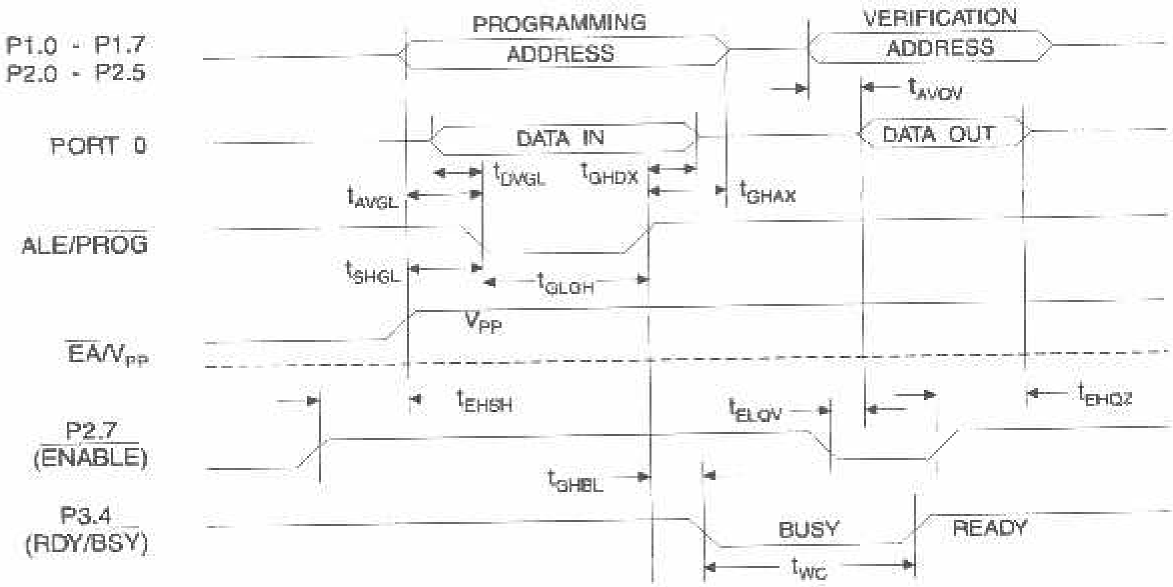


Flash Programming and Verification Characteristics – Parallel Mode

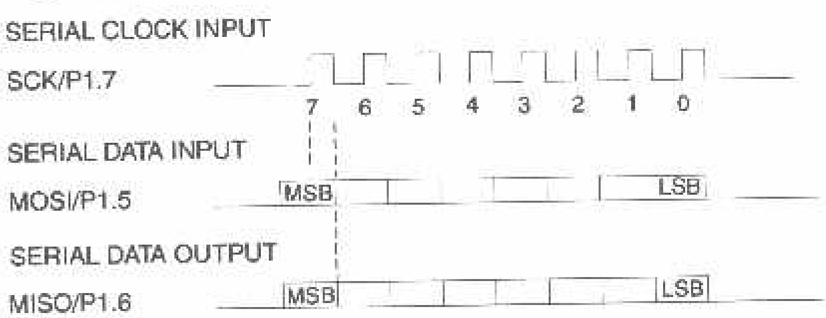
T_A = 0°C to 70°C, V_{CC} = 5.0V ± 10%

Symbol	Parameter	Min	Max	Units
V_{PP}	Programming Enable Voltage	11.5	12.5	V
I_{PP}	Programming Enable Current		1.0	mA
$1/t_{CLCL}$	Oscillator Frequency	3	24	MHz
t_{AVGL}	Address Setup to $\overline{PROG}$ Low	$48t_{CLCL}$		
t_{GHAX}	Address Hold after $\overline{PROG}$	$48t_{CLCL}$		
t_{DVGL}	Data Setup to $\overline{PROG}$ Low	$48t_{CLCL}$		
t_{GHDX}	Data Hold after $\overline{PROG}$	$48t_{CLCL}$		
t_{EHSH}	P2.7 ($\overline{ENABLE}$) High to V_{PP}	$48t_{CLCL}$		
t_{SHGL}	V_{PP} Setup to $\overline{PROG}$ Low	10		µs
t_{GLGH}	$\overline{PROG}$ Width	1	110	µs
t_{AVQV}	Address to Data Valid		$48t_{CLCL}$	
t_{ELQV}	$\overline{ENABLE}$ Low to Data Valid		$48t_{CLCL}$	
t_{EHQZ}	Data Float after $\overline{ENABLE}$	0	$48t_{CLCL}$	
t_{GHBL}	$\overline{PROG}$ High to $\overline{BUSY}$ Low		1.0	µs
t_{WC}	Byte Write Cycle Time		2.0	ms

Flash/EEPROM Programming and Verification Waveforms – Parallel Mode



Serial Downloading Waveforms



Absolute Maximum Ratings*

Operating Temperature	-55°C to +125°C
Storage Temperature	-65°C to +150°C
Voltage on Any Pin with Respect to Ground	-1.0V to +7.0V
Maximum Operating Voltage	6.6V
DC Output Current	15.0 mA

*NOTICE: Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC Characteristics

The values shown in this table are valid for T_A = -40°C to 85°C and V_{CC} = 5.0V ± 20%, unless otherwise noted.

Symbol	Parameter	Condition	Min	Max	Units
V_{IL}	Input Low-voltage	(Except $\overline{EA}$)	-0.5	0.2 V_{CC} - 0.1	V
V_{IL1}	Input Low-voltage ($\overline{EA}$)		-0.5	0.2 V_{CC} - 0.3	V
V_{IH}	Input Hifh-voltage	(Except XTAL1, RST)	0.2 V_{CC} + 0.9	V_{CC} + 0.5	V
V_{IH1}	Input Hifh-voltage	(XTAL1, RST)	0.7 V_{CC}	V_{CC} + 0.5	V
V_{OL}	Output Low-voltage [1] (Ports 1,2,3)	I_{OL} = 1.6 mA		0.5	V
V_{OL1}	Output Low-voltage [1] (Port 0, ALE, $\overline{PSEN}$)	I_{OL} = 3.2 mA		0.5	V
V_{OH}	Output Hifh-voltage (Ports 1,2,3, ALE, $\overline{PSEN}$)	I_{OH} = -60 µA, V_{CC} = 5V ± 10%	2.4		V
		I_{OH} = -25 µA	0.75 V_{CC}		V
		I_{OH} = -10 µA	0.9 V_{CC}		V
V_{OH1}	Output Hifh-voltage (Port 0 in External Bus Mode)	I_{OH} = -800 µA, V_{CC} = 5V ± 10%	2.4		V
		I_{OH} = -300 µA	0.75 V_{CC}		V
		I_{OH} = -80 µA	0.9 V_{CC}		V
I_{IL}	Logical 0 Input Current (Ports 1,2,3)	V_{IN} = 0.45V		-50	µA
I_{TL}	Logical 1 to 0 Transition Current (Ports 1,2,3)	V_{IN} = 2V, V_{CC} = 5V ± 10%		-650	µA
I_{LI}	Input Leakage Current (Port 0, $\overline{EA}$)	0.45 < V_{IN} < V_{CC}		±10	µA
RRST	Reset Pull-down Resistor		50	300	KΩ
C_{IO}	Pin Capacitance	Test Freq. = 1 MHz, T_A = 25°C		10	pF
I_{CC}	Power Supply Current	Active Mode, 12 MHz		25	mA
		Idle Mode, 12 MHz		6.5	mA
	Power-down Mode [2]	V_{CC} = 6V		100	µA
		V_{CC} = 3V		40	µA

Notes: 1. Under steady state (non-transient) conditions, I_{OL} must be externally limited as follows:
Maximum I_{OL} per port pin: 10 mA
Maximum I_{OL} per 8-bit port:
Port 0: 26 mA
Ports 1, 2, 3: 15 mA
Maximum total I_{OL} for all output pins: 71 mA
If I_{OL} exceeds the test condition, V_{OL} may exceed the related specification. Pins are not guaranteed to sink current greater than the listed test conditions.
2. Minimum V_{CC} for Power-down is 2V

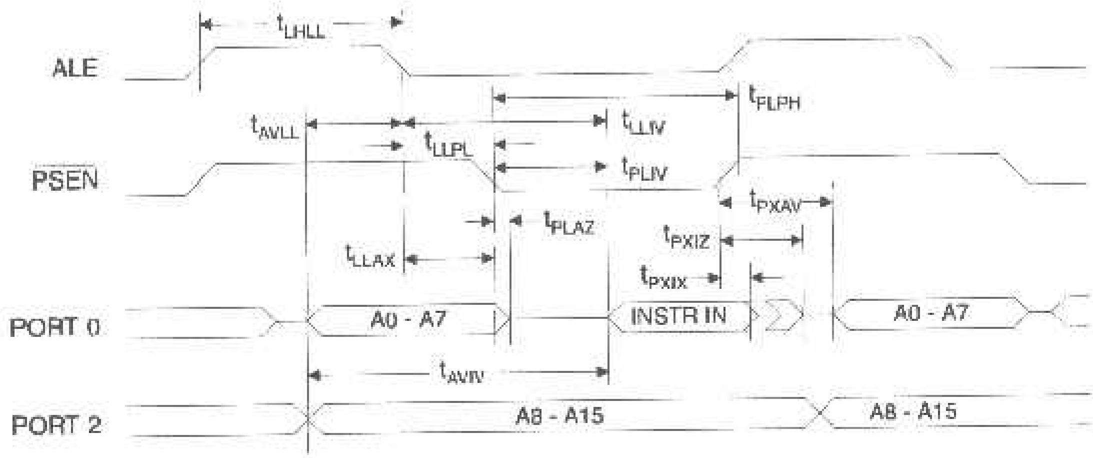
AC Characteristics

Under operating conditions, load capacitance for Port 0, ALE/$\overline{PROG}$, and $\overline{PSEN}$ = 100 pF; load capacitance for all other outputs = 80 pF.

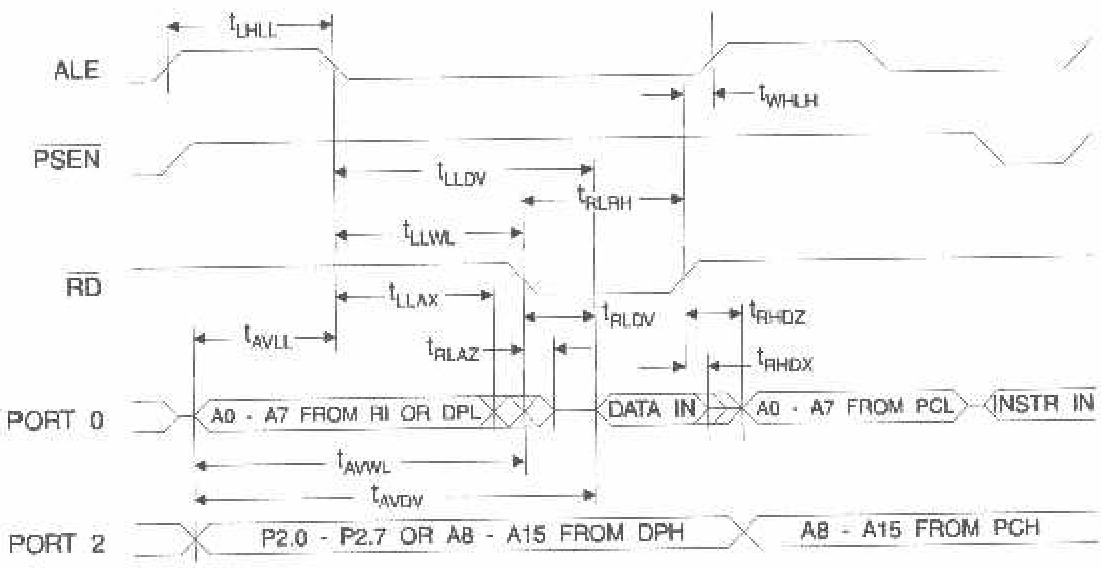
External Program and Data Memory Characteristics

Symbol	Parameter	Variable Oscillator		Units
		Min	Max	
$1/t_{CLCL}$	Oscillator Frequency	0	24	MHz
t_{LHLL}	ALE Pulse Width	$2t_{CLCL}$ - 40		ns
t_{AVLL}	Address Valid to ALE Low	t_{CLCL} - 13		ns
t_{LLAX}	Address Hold after ALE Low	t_{CLCL} - 20		ns
t_{LLIV}	ALE Low to Valid Instruction In		$4t_{CLCL}$ - 65	ns
t_{LLPL}	ALE Low to $\overline{PSEN}$ Low	t_{CLCL} - 13		ns
t_{PLPH}	$\overline{PSEN}$ Pulse Width	$3t_{CLCL}$ - 20		ns
t_{PLIV}	$\overline{PSEN}$ Low to Valid Instruction In		$3t_{CLCL}$ - 45	ns
t_{PXIX}	Input Instruction Hold after $\overline{PSEN}$	0		ns
t_{PXIZ}	Input Instruction Float after $\overline{PSEN}$		t_{CLCL} - 10	ns
t_{PXAV}	$\overline{PSEN}$ to Address Valid	t_{CLCL} - 8		ns
t_{AVIV}	Address to Valid Instruction In		$5t_{CLCL}$ - 55	ns
t_{PLAZ}	$\overline{PSEN}$ Low to Address Float		10	ns
t_{RLRH}	$\overline{RD}$ Pulse Width	$6t_{CLCL}$ - 100		ns
t_{WLWH}	$\overline{WR}$ Pulse Width	$6t_{CLCL}$ - 100		ns
t_{RLDV}	$\overline{RD}$ Low to Valid Data In		$5t_{CLCL}$ - 90	ns
t_{RHDX}	Data Hold after $\overline{RD}$	0		ns
t_{RHDZ}	Data Float after $\overline{RD}$		$2t_{CLCL}$ - 28	ns
t_{LLDV}	ALE Low to Valid Data In		$8t_{CLCL}$ - 150	ns
t_{AVDV}	Address to Valid Data In		$9t_{CLCL}$ - 165	ns
t_{LLWL}	ALE Low to $\overline{RD}$ or $\overline{WR}$ Low	$3t_{CLCL}$ - 50	$3t_{CLCL}$ + 50	ns
t_{AVWL}	Address to $\overline{RD}$ or $\overline{WR}$ Low	$4t_{CLCL}$ - 75		ns
t_{QVWX}	Data Valid to $\overline{WR}$ Transition	t_{CLCL} - 20		ns
t_{QVWH}	Data Valid to $\overline{WR}$ High	$7t_{CLCL}$ - 120		ns
t_{WHQX}	Data Hold after $\overline{WR}$	t_{CLCL} - 20		ns
t_{RLAZ}	$\overline{RD}$ Low to Address Float		0	ns
t_{WHLH}	$\overline{RD}$ or $\overline{WR}$ High to ALE High	t_{CLCL} - 20	t_{CLCL} + 25	ns

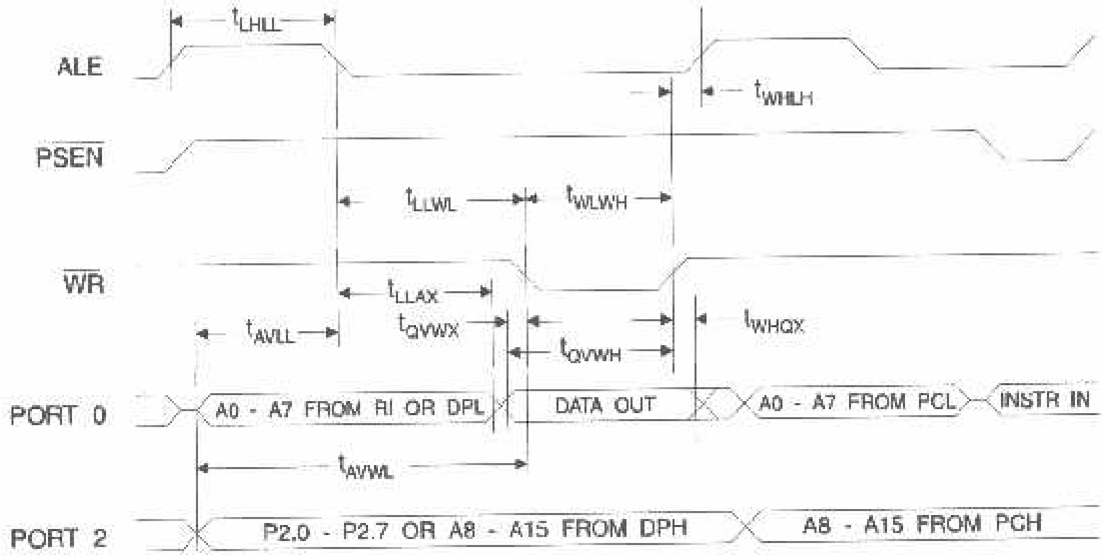
External Program Memory Read Cycle



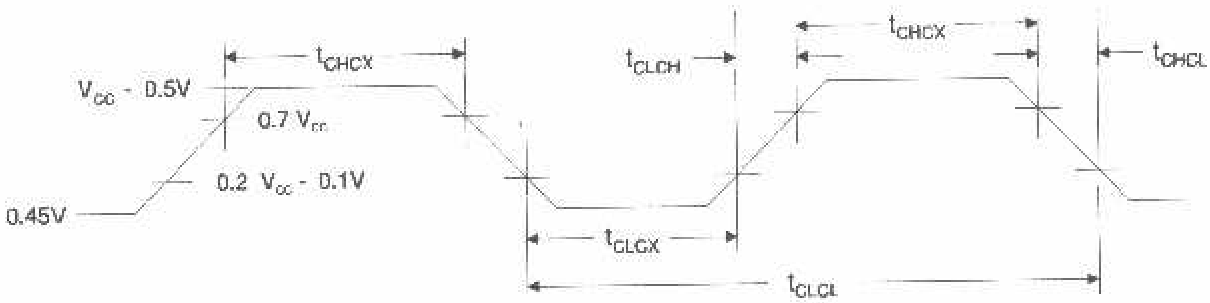
External Data Memory Read Cycle



External Data Memory Write Cycle



External Clock Drive Waveforms



External Clock Drive

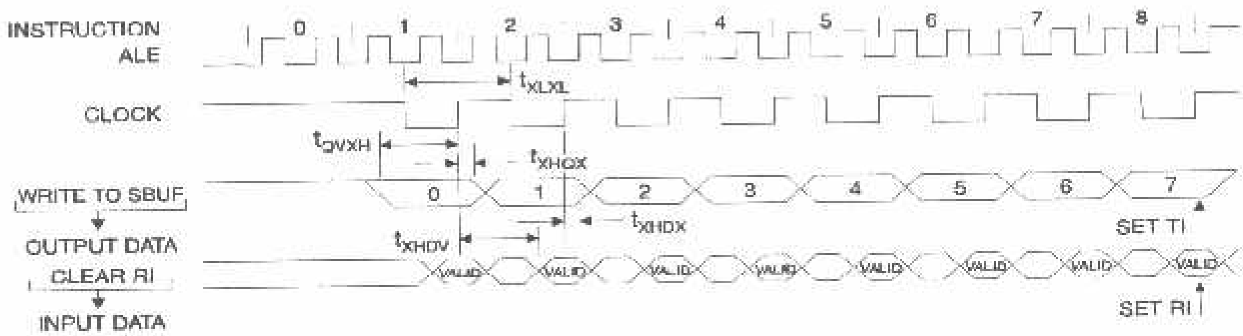
Symbol	Parameter	V_{CC} = 4.0V to 6.0V		Units
		Min	Max	
$1/t_{CLCL}$	Oscillator Frequency	0	24	MHz
t_{CLCL}	Clock Period	41.6		ns
t_{CHCX}	High Time	15		ns
t_{CLCX}	Low Time	15		ns
t_{CLCH}	Rise Time		20	ns
t_{CHCL}	Fall Time		20	ns

Serial Port Timing: Shift Register Mode Test Conditions

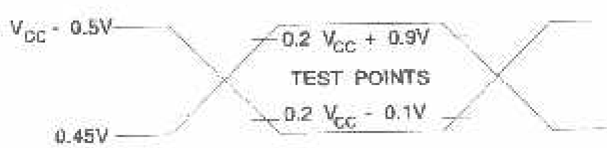
The values in this table are valid for V_{CC} = 4.0V to 6V and Load Capacitance = 80 pF.

Symbol	Parameter	Variable Oscillator		Units
		Min	Max	
t_{XLXL}	Serial Port Clock Cycle Time	$12t_{CLCL}$		µs
t_{QVXH}	Output Data Setup to Clock Rising Edge	$10t_{CLCL}$ - 133		ns
t_{XHQX}	Output Data Hold after Clock Rising Edge	$2t_{CLCL}$ - 117		ns
t_{XHDX}	Input Data Hold after Clock Rising Edge	0		ns
t_{XHDV}	Clock Rising Edge to Input Data Valid		$10t_{CLCL}$ - 133	ns

Shift Register Mode Timing Waveforms



AC Testing Input/Output Waveforms(1)



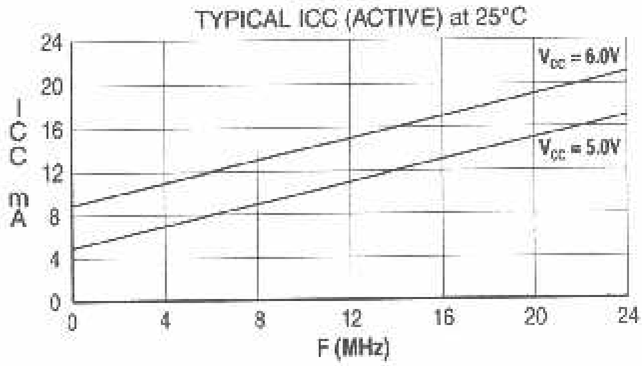
Notes: 1. AC Inputs during testing are driven at V_{CC} - 0.5V for a logic 1 and 0.45V for a logic 0. Timing measurements are made at V_{IH} min. for a logic 1 and V_{IL} max. for a logic 0.

Float Waveforms(1)

Notes: 1. For timing purposes, a port pin is no longer floating when a 100 mV change from load voltage occurs. A port pin begins to float when a 100 mV change from the loaded V_{OH}/V_{OL} level occurs.

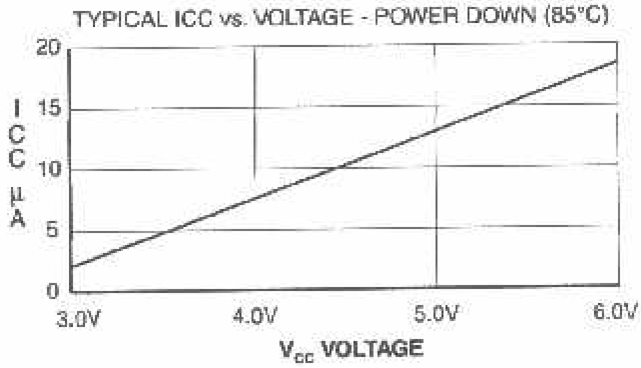
AT89S8252

TYPICAL ICC (ACTIVE) at 25°C



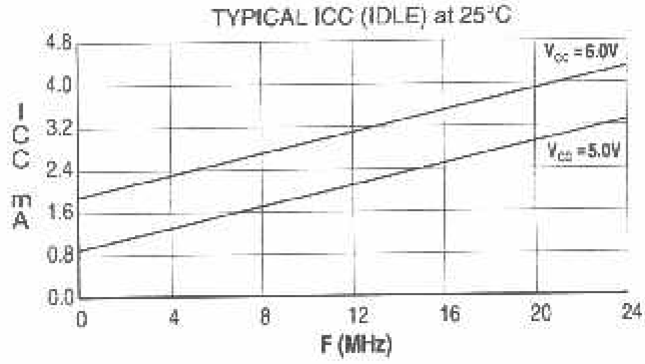
AT89S8252

TYPICAL ICC vs. VOLTAGE - POWER DOWN (85°C)



AT89S8252

TYPICAL ICC (IDLE) at 25°C



Notes:
1. XTAL1 tied to GND for Icc (power-down)
2. Lock bits programmed

Ordering Information

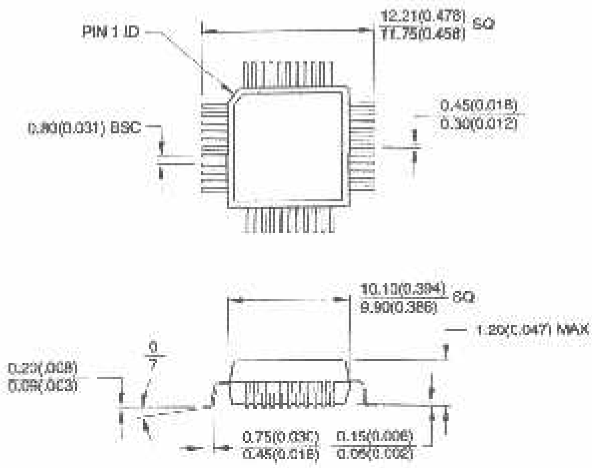
Speed (MHz)	Power Supply	Ordering Code	Package	Operation Range
24	4.0V to 6.0V	AT89S8252-24AC AT89S8252-24JC AT89S8252-24PC AT89S8252-24QC	44A 44J 40P6 44Q	Commercial (0°C to 70°C)
	4.0V to 6.0V	AT89S8252-24AI AT89S8252-24JI AT89S8252-24PI AT89S8252-24QI	44A 44J 40P6 44Q	Industrial (-40°C to 85°C)
33	4.5V to 5.5V	AT89S8252-33AC AT89S8252-33JC AT89S8252-33PC AT89S8252-33QC	44A 44J 40P6 44Q	Commercial (0°C to 70°C)

= Preliminary Information

Package Type	
44A	44-lead, Thin Plastic Gull Wing Quad Flatpack (TQFP)
44J	44-lead, Plastic J-leaded Chip Carrier (PLCC)
40P6	40-lead, 0.600" Wide, Plastic Dual Inline Package (PDIP)
44Q	44-lead, Plastic Gull Wing Quad Flatpack (PQFP)

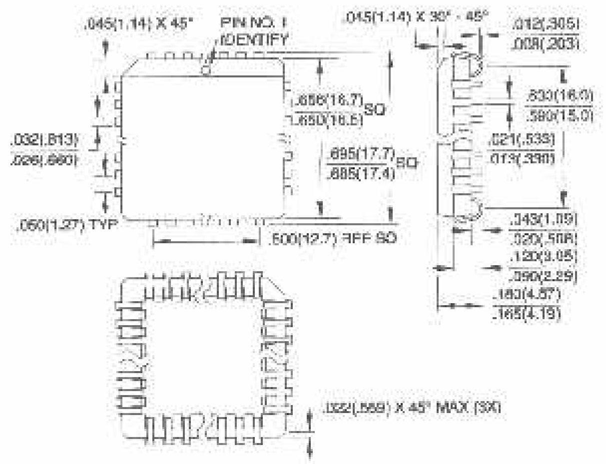
Packaging Information

44A, 44-lead, Thin (1.0 mm) Plastic Gull Wing Quad Flatpack (TQFP)
Dimensions in Millimeters and (Inches)*
JEDEC STANDARD MS-026 ACB

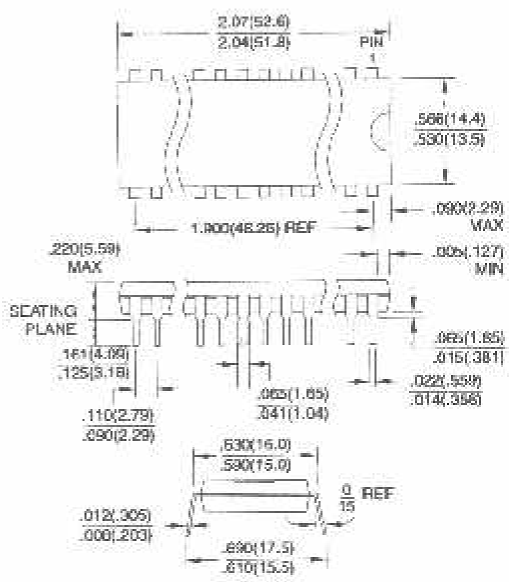


Controlling dimension: millimeters

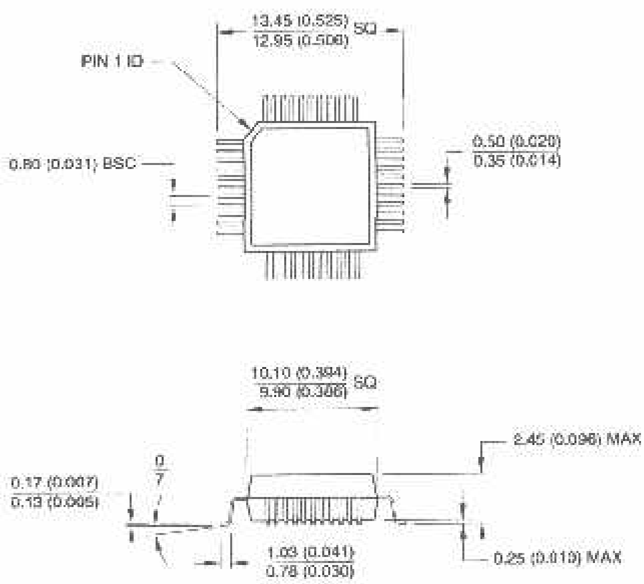
44J, 44-lead, Plastic J-leaded Chip Carrier (PLCC)
Dimensions in Inches and (Millimeters)
JEDEC STANDARD MS-018 AC



40P6, 40-lead, 0.600" Wide, Plastic Dual Inline Package (PDIP)
Dimensions in Inches and (Millimeters)



44Q, 44-lead, Plastic Quad Flat Package (PQFP)
Dimensions in Millimeters and (Inches)*
JEDEC STANDARD MS-022 AB



Controlling dimension: millimeters

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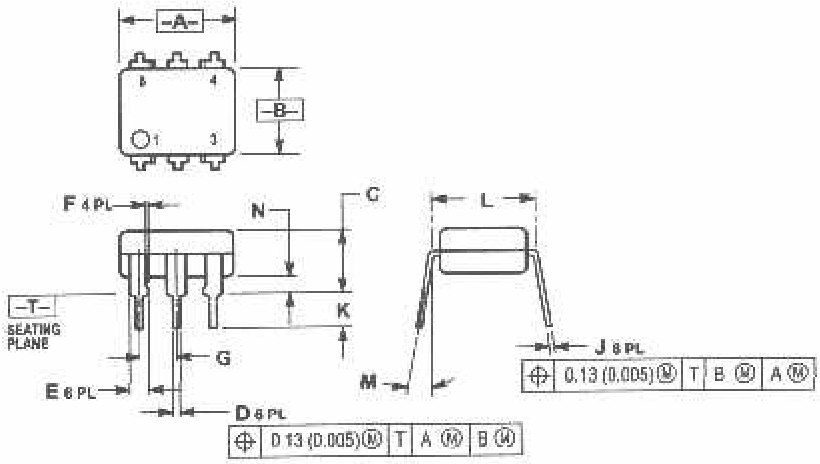
PACKAGE DIMENSIONS

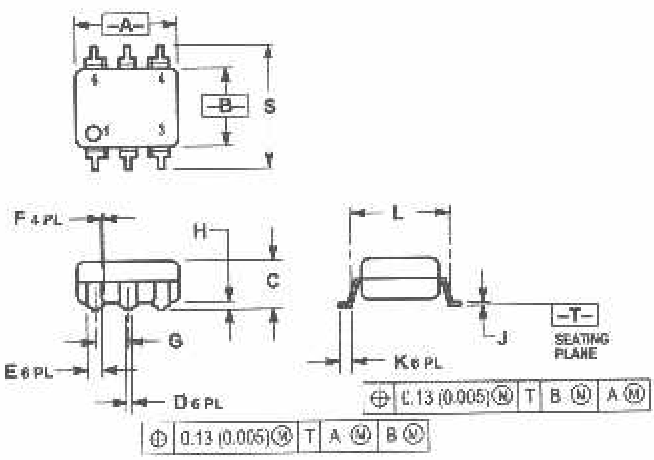


NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. DIMENSION L TO CENTER OF LEAD WHEN FORMED PARALLEL.

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.320	0.350	8.13	8.89
B	0.240	0.260	6.10	6.60
C	0.115	0.200	2.93	5.08
D	0.016	0.020	0.41	0.50
E	0.040	0.070	1.02	1.77
F	0.010	0.014	0.25	0.36
G	0.100 BSC		2.54 BSC	
J	0.008	0.012	0.21	0.30
K	0.100	0.150	2.54	3.81
L	0.300 BSC		7.62 BSC	
M	0°	15°	0°	15°
N	0.015	0.100	0.38	2.54

STYLE 1:
PIN 1. ANODE
2. CATHODE
3. NC
4. EMITTER
5. COLLECTOR
6. BASE

CASE 730A–04
ISSUE G

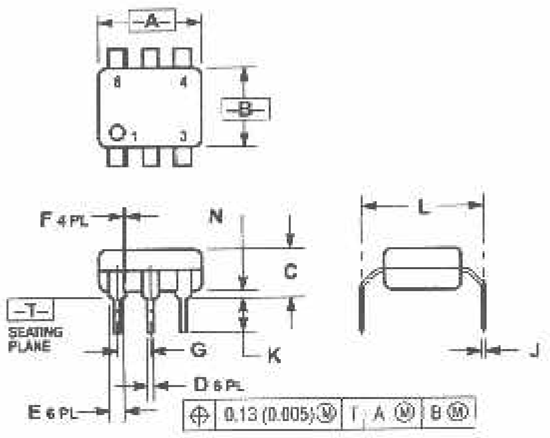


NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.320	0.350	8.13	8.89
B	0.240	0.260	6.10	6.60
C	0.115	0.200	2.93	5.08
D	0.016	0.020	0.41	0.50
E	0.040	0.070	1.02	1.77
F	0.010	0.014	0.25	0.36
G	0.100 BSC		2.54 BSC	
H	0.020	0.025	0.51	0.63
J	0.008	0.012	0.20	0.30
K	0.006	0.035	0.16	0.88
L	0.320 BSC		8.13 BSC	
S	0.332	0.390	8.43	9.90

***Consult factory for leadform option availability**

CASE 730C–04
ISSUE D



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. DIMENSION L TO CENTER OF LEAD WHEN FORMED PARALLEL.

DIM	INCHES MIN	INCHES MAX	MILLIMETERS MIN	MILLIMETERS MAX
A	0.320	0.350	8.13	8.89
B	0.240	0.260	6.10	6.60
C	0.115	0.200	2.93	5.08
D	0.016	0.020	0.41	0.50
E	0.040	0.070	1.02	1.77
F	0.010	0.014	0.25	0.36
G	0.100 BSC		2.54 BSC	
J	0.008	0.012	0.21	0.30
K	0.100	0.150	2.54	3.81
L	0.400	0.425	10.16	10.80
N	0.015	0.040	0.38	1.02

***Consult factory for leadform option availability**

CASE 730D–05
ISSUE D

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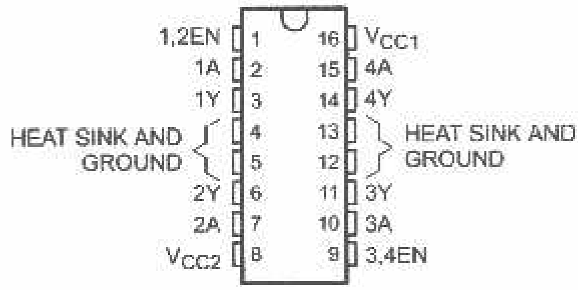
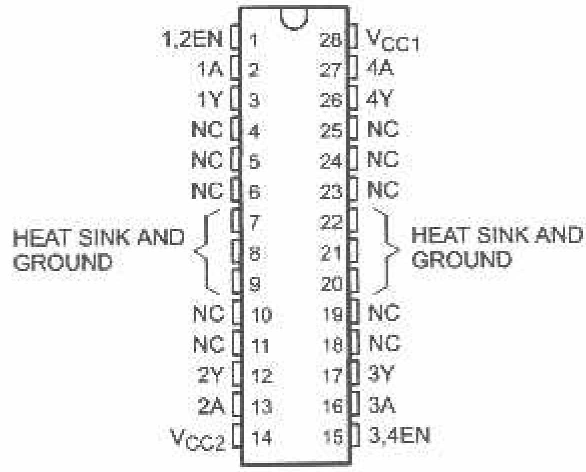
- **Featuring Unitrode L293 and L293D Products Now From Texas Instruments**
- **Wide Supply-Voltage Range: 4.5 V to 36 V**
- **Separate Input-Logic Supply**
- **Internal ESD Protection**
- **Thermal Shutdown**
- **High-Noise-Immunity Inputs**
- **Functional Replacements for SGS L293 and SGS L293D**
- **Output Current 1 A Per Channel (600 mA for L293D)**
- **Peak Output Current 2 A Per Channel (1.2 A for L293D)**
- **Output Clamp Diodes for Inductive Transient Suppression (L293D)**

N, NE PACKAGE (TOP VIEW)



DWP PACKAGE (TOP VIEW)



description

The L293 and L293D are quadruple high-current half-H drivers. The L293 is designed to provide bidirectional drive currents of up to 1 A at voltages from 4.5 V to 36 V. The L293D is designed to provide bidirectional drive currents of up to 600-mA at voltages from 4.5 V to 36 V. Both devices are designed to drive inductive loads such as relays, solenoids, dc and bipolar stepping motors, as well as other high-current/high-voltage loads in positive-supply applications.

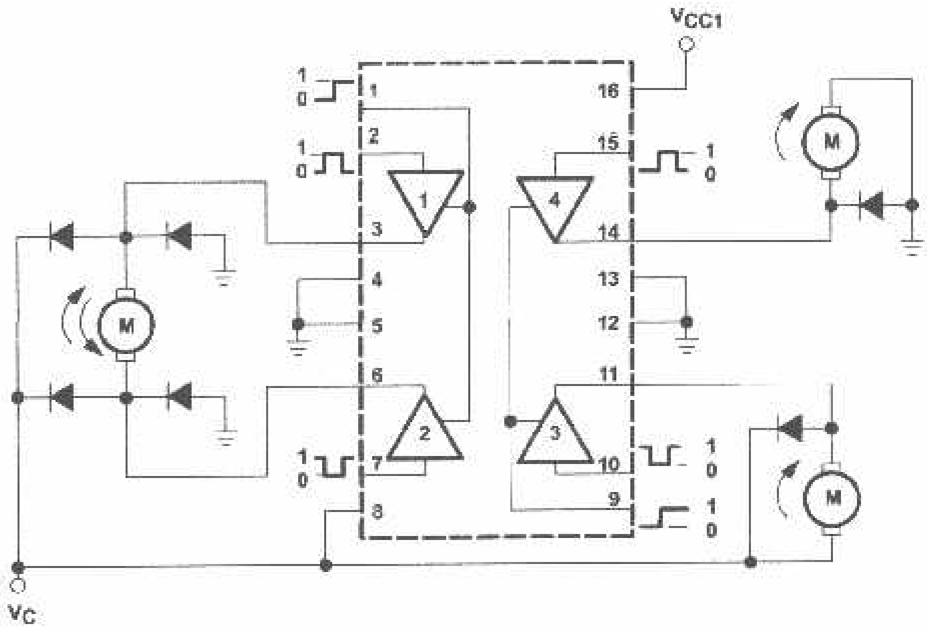
All inputs are TTL compatible. Each output is a complete totem-pole drive circuit, with a Darlington transistor sink and a pseudo-Darlington source. Drivers are enabled in pairs, with drivers 1 and 2 enabled by 1,2EN and drivers 3 and 4 enabled by 3,4EN. When an enable input is high, the associated drivers are enabled and their outputs are active and in phase with their inputs. When the enable input is low, those drivers are disabled and their outputs are off and in the high-impedance state. With the proper data inputs, each pair of drivers forms a full-H (or bridge) reversible drive suitable for solenoid or motor applications.

On the L293, external high-speed output clamp diodes should be used for inductive transient suppression.

A V_{CC1} terminal, separate from V_{CC2}, is provided for the logic inputs to minimize device power dissipation.

The L293and L293D are characterized for operation from 0°C to 70°C.

block diagram



NOTE: Output diodes are internal in L293D.

TEXAS INSTRUMENTS
AVAILABLE OPTIONS

T_A	PACKAGE PLASTIC DIP (NE)
0°C to 70°C	L293NE L293DNE

Unitrode Products from Texas Instruments
AVAILABLE OPTIONS

T_A	PACKAGED DEVICES	
	SMALL OUTLINE (DWP)	PLASTIC DIP (N)
0°C to 70°C	L293DWP L293DDWP	L293N L293DN

The DWP package is available taped and reeled. Add the suffix TR to device type (e.g., L293DWPTR).

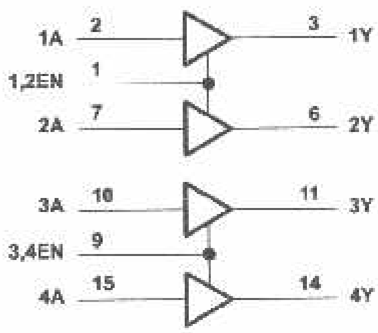
FUNCTION TABLE
(each driver)

INPUTS†		OUTPUT
A	EN	Y
H	H	H
L	H	L
X	L	Z

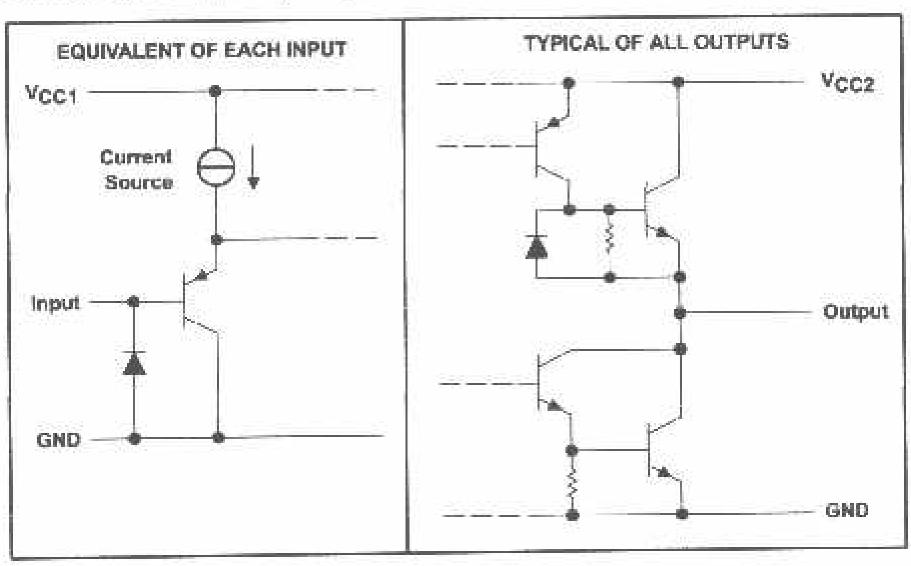
H = high level, L = low level, X = irrelevant, Z = high impedance (off)

† In the thermal shutdown mode, the output is in the high-impedance state, regardless of the input levels.

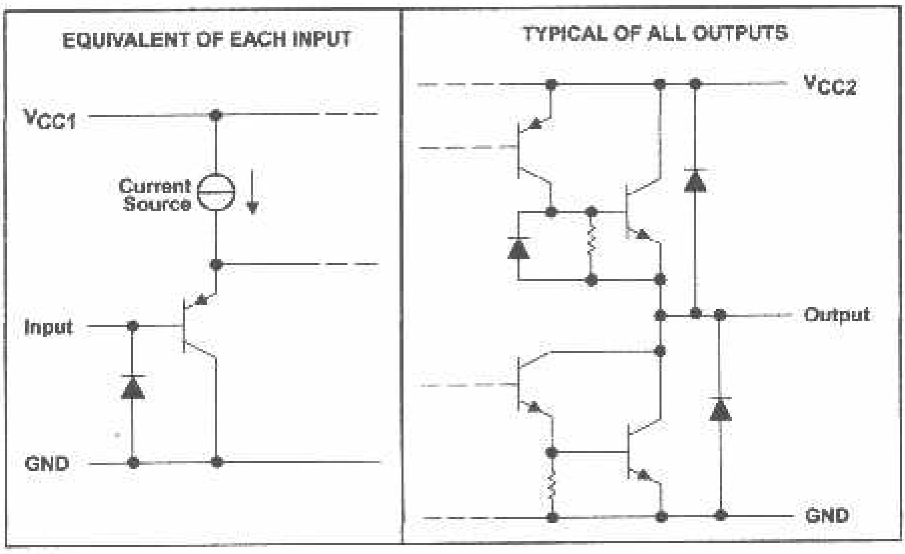
logic diagram



schematics of inputs and outputs (L293)



schematics of inputs and outputs (L293D)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage, V_{CC1} (see Note 1)	36 V
Output supply voltage, V_{CC2}	36 V
Input voltage, V_I	7 V
Output voltage range, V_O	–3 V to V_{CC2} + 3 V
Peak output current, I_O (nonrepetitive, $t \leq 5$ ms): L293	±2 A
Peak output current, I_O (nonrepetitive, $t \leq 100$ µs): L293D	±1.2 A
Continuous output current, I_O: L293	±1 A
Continuous output current, I_O: L293D	±600 mA
Continuous total dissipation at (or below) 25°C free-air temperature (see Notes 2 and 3)	2075 mW
Continuous total dissipation at 80°C case temperature (see Note 3)	5000 mW
Maximum junction temperature, T_J	150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds	260°C
Storage temperature range, T_{stg}	–65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. All voltage values are with respect to the network ground terminal.
2. For operation above 25°C free-air temperature, derate linearly at the rate of 16.6 mW/°C.
3. For operation above 25°C case temperature, derate linearly at the rate of 71.4 mW/°C. Due to variations in individual device electrical characteristics and thermal resistance, the built-in thermal overload protection may be activated at power levels slightly above or below the rated dissipation.

recommended operating conditions

			MIN	MAX	UNIT
	Supply voltage	V_{CC1}	4.5	7	V
		V_{CC2}	V_{CC1}	36	
V_{IH}	High-level input voltage	$V_{CC1} \le 7$ V	2.3	V_{CC1}	V
		$V_{CC1} \ge 7$ V	2.3	7	V
V_{IL}	Low-level output voltage		–0.3†	1.5	V
T_A	Operating free-air temperature		0	70	°C

† The algebraic convention, in which the least positive (most negative) designated minimum, is used in this data sheet for logic voltage levels.

electrical characteristics, V_{CC1} = 5 V, V_{CC2} = 24 V, T_A = 25°C

PARAMETER			TEST CONDITIONS		MIN	TYP	MAX	UNIT
V_{OH}	High-level output voltage		L293: I_{OH} = –1 A L293D: I_{OH} = –0.6 A		V_{CC2}–1.8	V_{CC2}–1.4		V
V_{OL}	Low-level output voltage		L293: I_{OL} = 1 A L293D: I_{OL} = 0.6 A			1.2	1.8	V
V_{OKH}	High-level output clamp voltage		L293D: I_{OK} = –0.6 A			V_{CC2} + 1.3		V
V_{OKL}	Low-level output clamp voltage		L293D: I_{OK} = 0.6 A			1.3		V
I_{IH}	High-level input current	A	V_I = 7 V			0.2	100	µA
		EN				0.2	10	
I_{IL}	Low-level input current	A	V_I = 0			–3	–10	µA
		EN				–2	–100	
I_{CC1}	Logic supply current		I_O = 0	All outputs at high level		13	22	mA
				All outputs at low level		35	60	
				All outputs at high impedance		8	24	
I_{CC2}	Output supply current		I_O = 0	All outputs at high level		14	24	mA
				All outputs at low level		2	6	
				All outputs at high impedance		2	4	

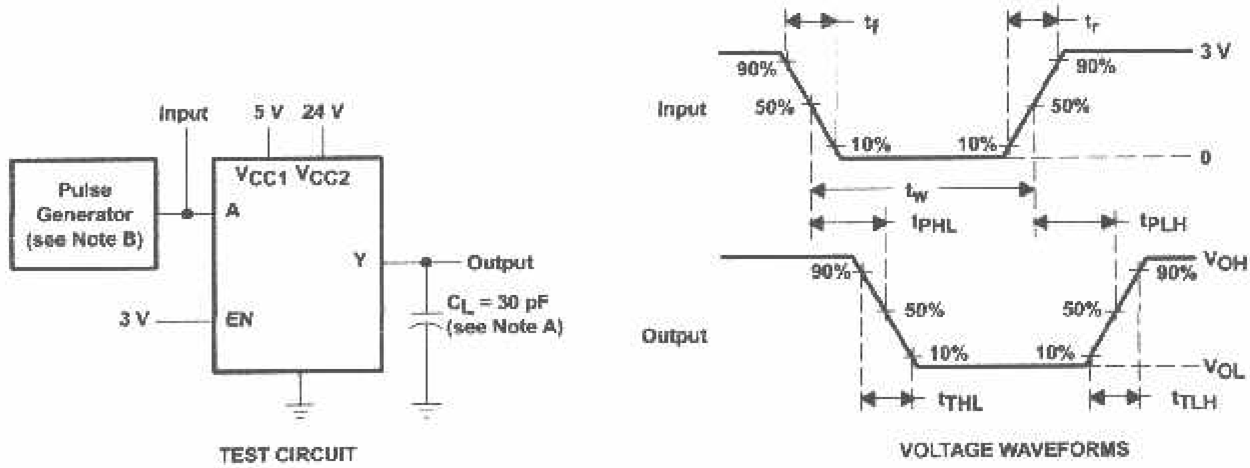
switching characteristics, V_{CC1} = 5 V, V_{CC2} = 24 V, T_A = 25°C

PARAMETER		TEST CONDITIONS	L293NE, L293DNE			UNIT
			MIN	TYP	MAX	
t_{PLH}	Propagation delay time, low-to-high-level output from A input	C_L = 30 pF, See Figure 1		800		ns
t_{PHL}	Propagation delay time, high-to-low-level output from A input			400		ns
t_{TLH}	Transition time, low-to-high-level output			300		ns
t_{THL}	Transition time, high-to-low-level output			300		ns

switching characteristics, V_{CC1} = 5 V, V_{CC2} = 24 V, T_A = 25°C

PARAMETER		TEST CONDITIONS	L293DWP, L293N L293DDWP, L293DN			UNIT
			MIN	TYP	MAX	
t_{PLH}	Propagation delay time, low-to-high-level output from A input	C_L = 30 pF, See Figure 1		750		ns
t_{PHL}	Propagation delay time, high-to-low-level output from A input			200		ns
t_{TLH}	Transition time, low-to-high-level output			100		ns
t_{THL}	Transition time, high-to-low-level output			350		ns

PARAMETER MEASUREMENT INFORMATION



NOTES: A. C_L includes probe and jig capacitance.
B. The pulse generator has the following characteristics: $t_r \leq 10$ ns, $t_f \leq 10$ ns, $t_w = 10\ \mu s$, PRR = 5 kHz, $Z_O = 50\ \Omega$.

Figure 1. Test Circuit and Voltage Waveforms

APPLICATION INFORMATION

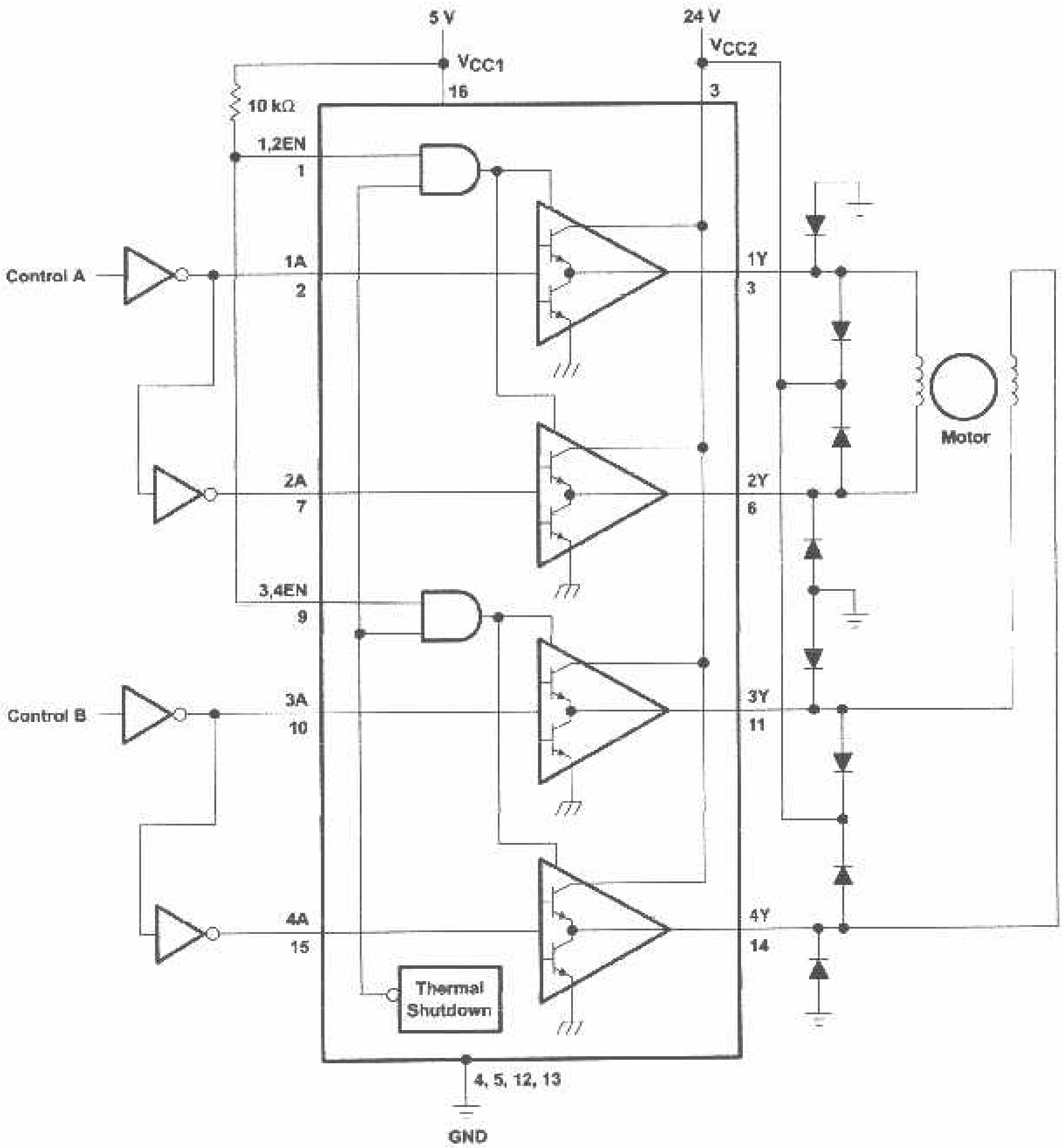


Figure 2. Two-Phase Motor Driver (L293)

APPLICATION INFORMATION

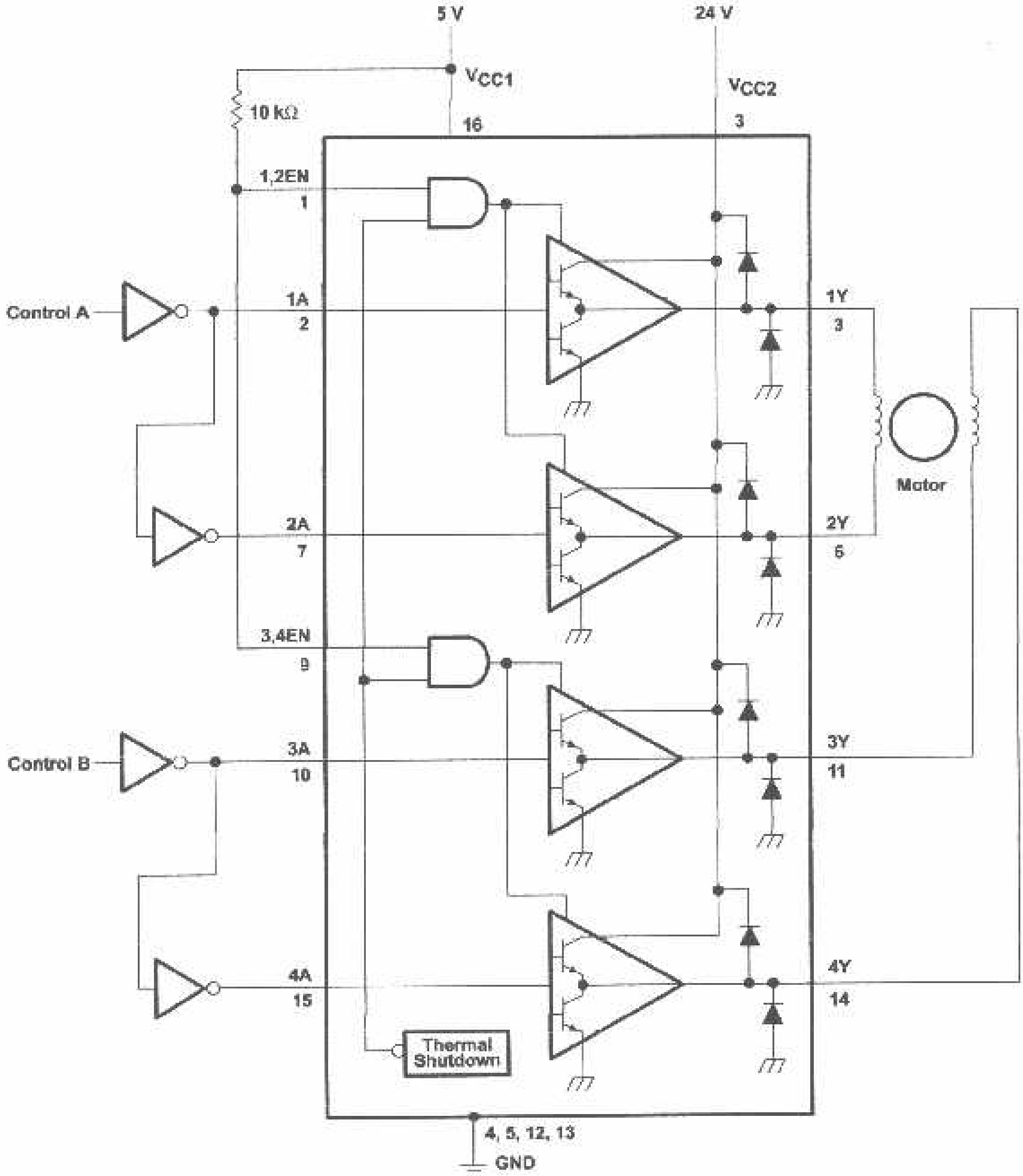


Figure 3. Two-Phase Motor Driver (L293D)

APPLICATION INFORMATION

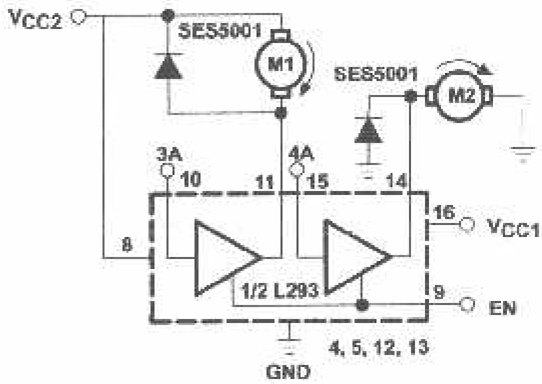


Figure 4. DC Motor Controls (connections to ground and to supply voltage)

EN	3A	M1	4A	M2
H	H	Fast motor stop	H	Run
H	L	Run	L	Fast motor stop
L	X	Free-running motor stop	X	Free-running motor stop

L = low, H = high, X = don't care

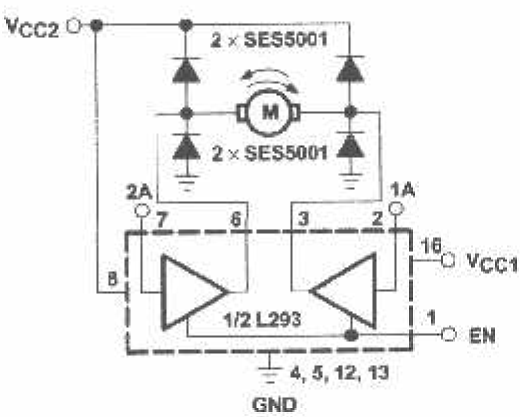


Figure 5. Bidirectional DC Motor Control

EN	1A	2A	FUNCTION
H	L	H	Turn right
H	H	L	Turn left
H	L	L	Fast motor stop
H	H	H	Fast motor stop
L	X	X	Fast motor stop

L = low, H = high, X = don't care

APPLICATION INFORMATION

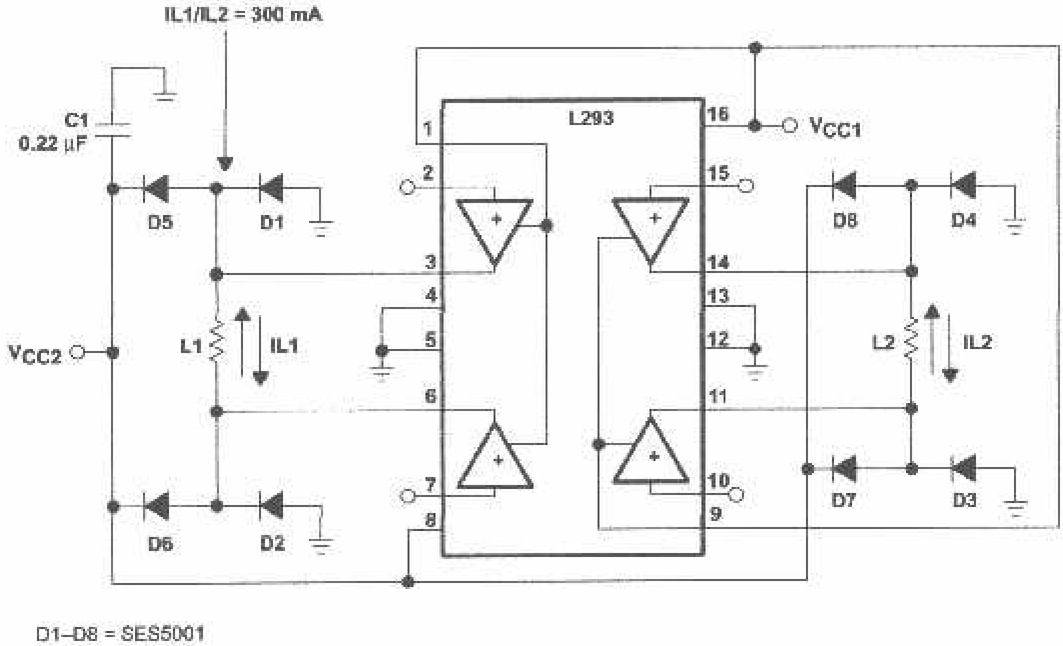


Figure 6. Bipolar Stepping-Motor Control

mounting instructions

The Rthj-amp of the L293 can be reduced by soldering the GND pins to a suitable copper area of the printed circuit board or to an external heatsink.

Figure 9 shows the maximum package power P_{TOT} and the θ_{JA} as a function of the side ℓ of two equal square copper areas having a thickness of 35 μm (see Figure 7). In addition, an external heat sink can be used (see Figure 8).

During soldering, the pin temperature must not exceed 260°C, and the soldering time must not be longer than 12 seconds.

The external heatsink or printed circuit copper area must be connected to electrical ground.

APPLICATION INFORMATION

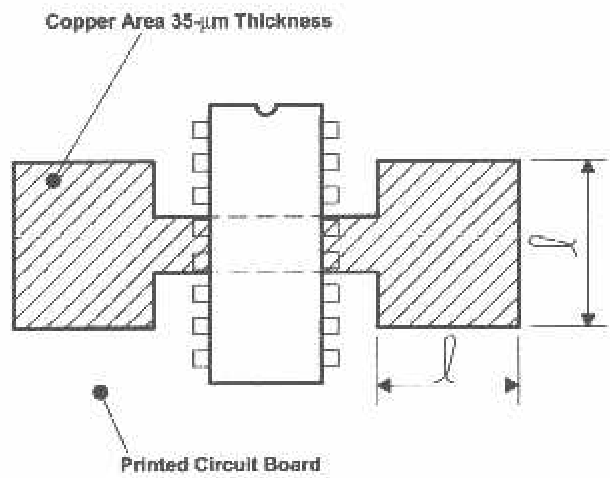


Figure 7. Example of Printed Circuit Board Copper Area
(used as heat sink)

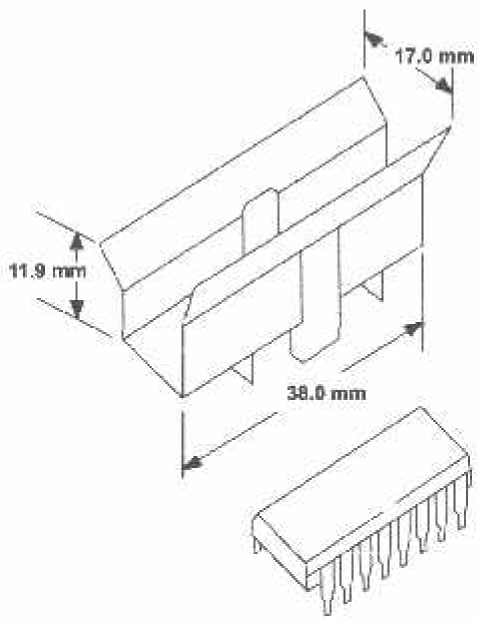


Figure 8. External Heat Sink Mounting Example
(θ_{JA} = 25°C/W)

APPLICATION INFORMATION

MAXIMUM POWER AND JUNCTION
vs
THERMAL RESISTANCE

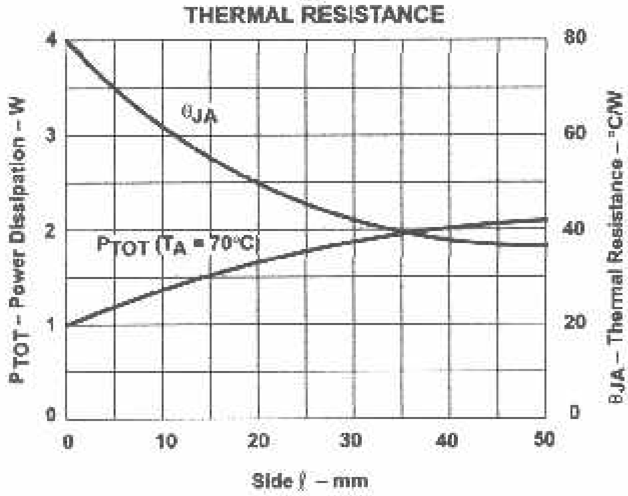


Figure 9

MAXIMUM POWER DISSIPATION
vs
AMBIENT TEMPERATURE

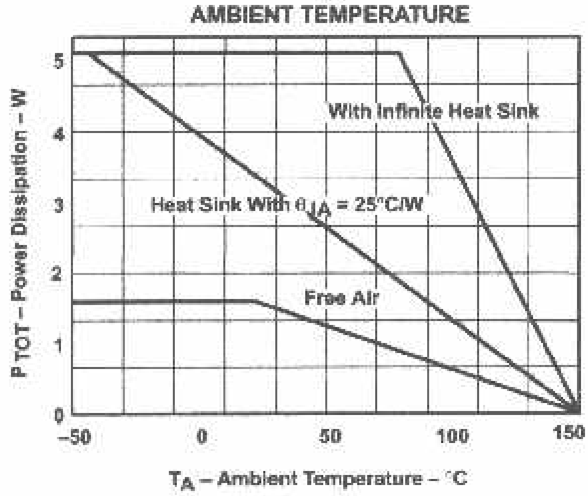


Figure 10

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GP2D12/GP2D15

General Purpose Type Distance Measuring Sensors

■ Features

1. Less influence on the color of reflective objects, reflectivity
2. Line-up of distance output/distance judgement type
   Distance output type (analog voltage) : **GP2D12**
   Detecting distance : 10 to 80cm
   Distance judgement type : **GP2D15**
   Judgement distance : 24cm
   (Adjustable within the range of 10 to 80cm)
3. External control circuit is unnecessary
4. Low cost

■ Applications

1. TVs
2. Personal computers
3. Cars
4. Copiers

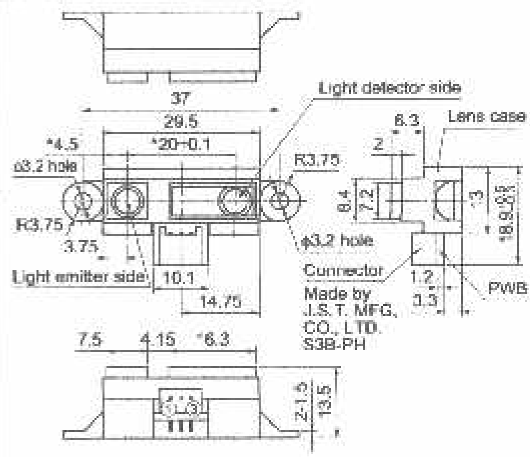
■ Absolute Maximum Ratings

(Ta=25°C, Vcc=5V)

Parameter	Symbol	Rating	Unit
Supply voltage	V_{CC}	−0.3 to +7	V
Output terminal voltage	V_O	−0.3 to Vcc+0.3	V
Operating temperature	T_{opr}	−10 to +60	°C
Storage temperature	T_{stg}	−40 to +70	°C

■ Outline Dimensions

(Unit : mm)



Terminal connection
① V_O
② GND
③ V_{CC}

- The dimensions marked * are described the dimensions of lens center position.
- Unspecified tolerance : ±0.3mm

■ Recommended Operating Conditions

Parameter	Symbol	Rating	Unit
Operating supply voltage	V_{CC}	4.5 to +5.5	V

■ Electro-optical Characteristics

(T_a=25°C, V_{CC}=5V)

Parameter		Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Distance measuring range		ΔL	*1 *3	10	–	80	cm
Output terminal voltage	GP2D12	V_O	L=80cm *1	0.25	0.4	0.55	V
	GP2D15	V_{OH}	Output voltage at High *1	V_{CC} −0.3	–	–	V
		V_{OL}	Output voltage at Low *1	–	–	0.6	V
Difference of output voltage	GP2D12	ΔV_O	Output change at L=80cm to 10cm *1	1.75	2.0	2.25	V
Distance characteristics of output	GP2D15	V_O	*1 *2 *4	21	24	27	cm
Average Dissipation current		I_{CC}	L=80cm *1	–	33	50	mA

Note: L : Distance to reflective object.

*1 Using reflective object : White paper (Made by Kodak Co. Ltd. gray cards R-27 · white face, reflective ratio ; 90%).
*2 We ship the device after the following adjustment : Output switching distance L=24cm±1cm must be measured by the sensor.
*3 Distance measuring range of the optical sensor system.
*4 Output switching has a hysteresis width. The distance specified by Vo should be the one with which the output L switches to the output H.

Fig.1 Internal Block Diagram

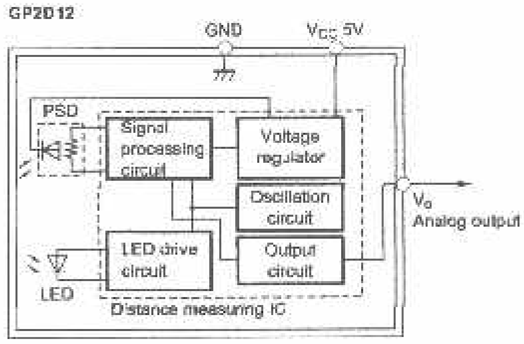


Fig.2 Internal Block Diagram

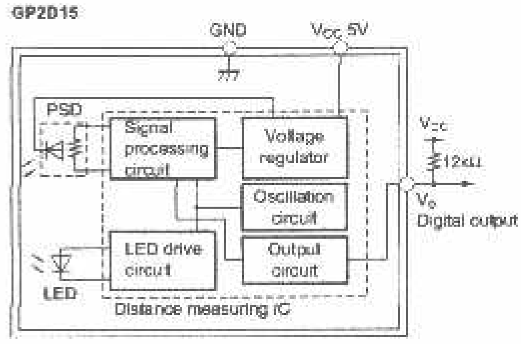


Fig.3 Timing Chart

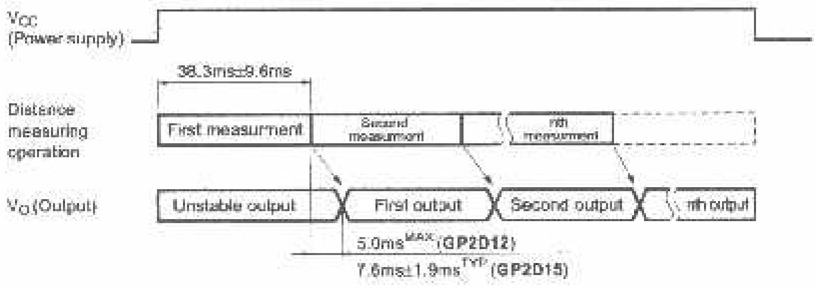


Fig.4 Distance Characteristics

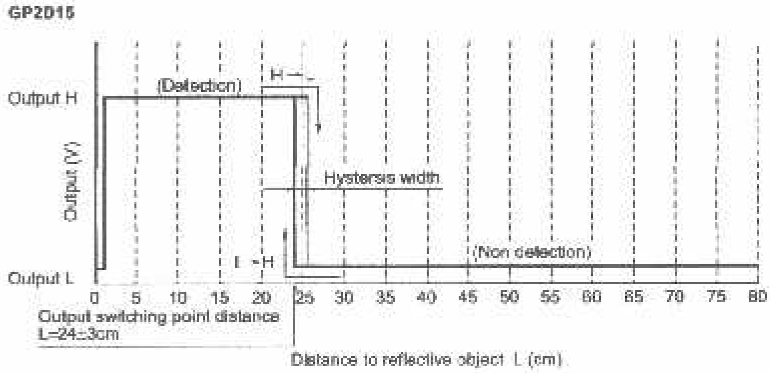


Fig.5 Analog Output Voltage vs. Surface Illuminance of Reflective Object

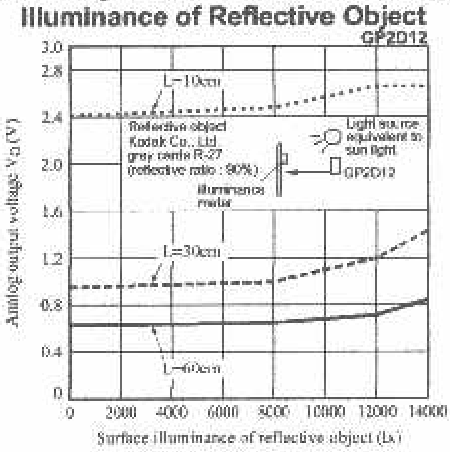


Fig.6 Analog Output Voltage vs.Distance to Reflective Object

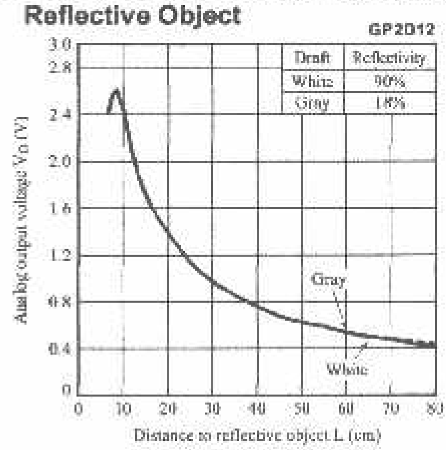


Fig.7 Analog Output Voltage vs.Ambient Temperature

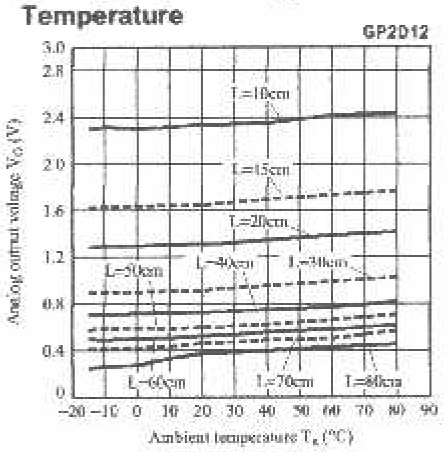
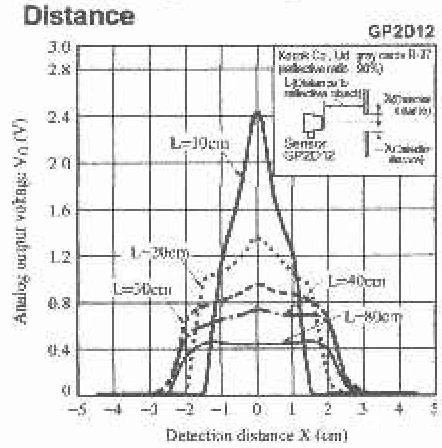


Fig.8 Analog Output Voltage vs.Detection Distance



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– Test and measurement equipment
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– Consumer electronics

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– Gas leakage sensor breakers
– Alarm equipment
– Various safety devices, etc.

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Features

- Compatible with MCS-51™ Products
- 8K Bytes of In-System Reprogrammable Downloadable Flash Memory
  - SPI Serial Interface for Program Downloading
  - Endurance: 1,000 Write/Erase Cycles
- 2K Bytes EEPROM
  - Endurance: 100,000 Write/Erase Cycles
- 4V to 6V Operating Range
- Fully Static Operation: 0 Hz to 24 MHz
- Three-level Program Memory Lock
- 256 x 8-bit Internal RAM
- 32 Programmable I/O Lines
- Three 16-bit Timer/Counters
- Nine Interrupt Sources
- Programmable UART Serial Channel
- SPI Serial Interface
- Low-power Idle and Power-down Modes
- Interrupt Recovery From Power-down
- Programmable Watchdog Timer
- Dual Data Pointer
- Power-off Flag

8-bit Microcontroller with 8K Bytes Flash

AT89S8252

Description

The AT89S8252 is a low-power, high-performance CMOS 8-bit microcomputer with 8K bytes of downloadable Flash programmable and erasable read only memory and 2K bytes of EEPROM. The device is manufactured using Atmel's high-density nonvolatile memory technology and is compatible with the industry-standard 80C51 instruction set and pinout. The on-chip downloadable Flash allows the program memory to be reprogrammed in-system through an SPI serial interface or by a conventional nonvolatile memory programmer. By combining a versatile 8-bit CPU with downloadable Flash on a monolithic chip, the Atmel AT89S8252 is a powerful microcomputer which provides a highly-flexible and cost-effective solution to many embedded control applications.

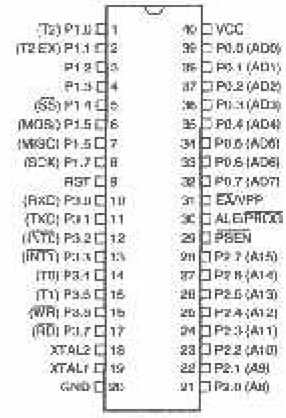
The AT89S8252 provides the following standard features: 8K bytes of downloadable Flash, 2K bytes of EEPROM, 256 bytes of RAM, 32 I/O lines, programmable watchdog timer, two data pointers, three 16-bit timer/counters, a six-vector two-level interrupt architecture, a full duplex serial port, on-chip oscillator, and clock circuitry. In addition, the AT89S8252 is designed with static logic for operation down to zero frequency and supports two software selectable power saving modes. The Idle Mode stops the CPU while allowing the RAM, timer/counters, serial port, and interrupt system to continue functioning. The Power-down mode saves the RAM contents but freezes the oscillator, disabling all other chip functions until the next interrupt or hardware reset.

The downloadable Flash can be changed a single byte at a time and is accessible through the SPI serial interface. Holding RESET active forces the SPI bus into a serial programming interface and allows the program memory to be written to or read from unless Lock Bit 2 has been activated.

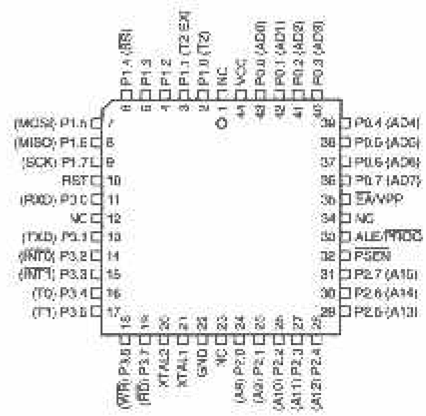
Rev. 0401E–02/00

Pin Configurations

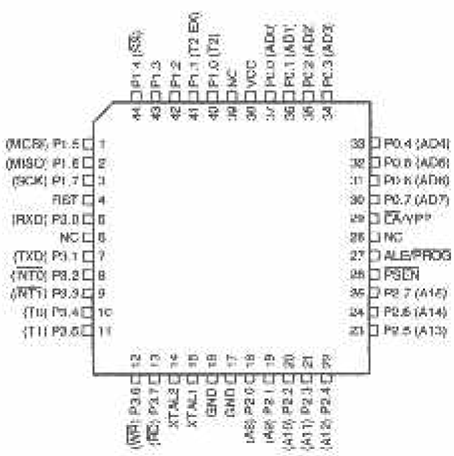
PDIP



PLCC



PQFP/TQFP



Pin Description

VCC

Supply voltage.

GND

Ground.

Port 0

Port 0 is an 8-bit open drain bbi-didirectional I/O port. As an output port, each pin can sink eight TTL inputs. When 1s are written to port 0 pins, the pins can be used as high-impedance inputs.

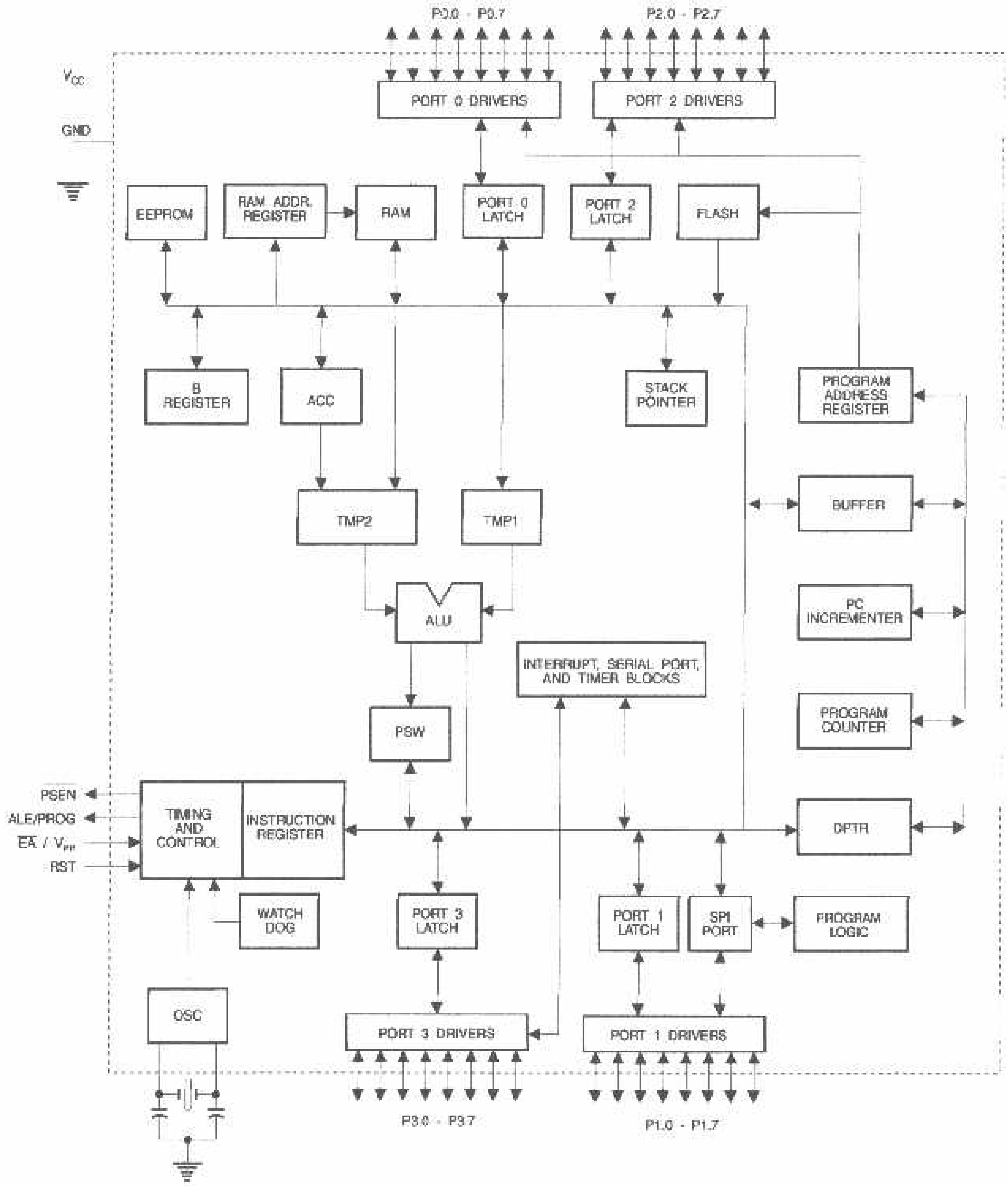
Port 0 can also be configured to be the multiplexed low-order address/data bus during accesses to external program and data memory. In this mode, P0 has internal pullups.

Port 0 also receives the code bytes during Flash programming and outputs the code bytes during program verification. External pullups are required during program verification.

Port 1

Port 1 is an 8-bit bi-directional I/O port with internal pullups. The Port 1 output buffers can sink/source four TTL inputs. When 1s are written to Port 1 pins, they are pulled high by the internal pullups and can be used as inputs. As inputs, Port 1 pins that are externally being pulled low will source current (I_{IL}) because of the internal pullups.

Block Diagram



Some Port 1 pins provide additional functions. P1.0 and P1.1 can be configured to be the timer/counter 2 external count input (P1.0/T2) and the timer/counter 2 trigger input (P1.1/T2EX), respectively.

Pin Description

Furthermore, P1.4, P1.5, P1.6, and P1.7 can be configured as the SPI slave port select, data input/output and shift clock input/output pins as shown in the following table.

Port Pin	Alternate Functions
P1.0	T2 (external count input to Timer/Counter 2), clock-out
P1.1	T2EX (Timer/Counter 2 capture/reload trigger and direction control)
P1.4	$\overline{SS}$ (Slave port select input)
P1.5	MOSI (Master data output, slave data input pin for SPI channel)
P1.6	MISO (Master data input, slave data output pin for SPI channel)
P1.7	SCK (Master clock output, slave clock input pin for SPI channel)

Port 1 also receives the low-order address bytes during Flash programming and verification.

Port 2

Port 2 is an 8-bit bi-directional I/O port with internal pullups. The Port 2 output buffers can sink/source four TTL inputs. When 1s are written to Port 2 pins, they are pulled high by the internal pullups and can be used as inputs. As inputs, Port 2 pins that are externally being pulled low will source current (I_{IL}) because of the internal pullups.

Port 2 emits the high-order address byte during fetches from external program memory and during accesses to external data memory that use 16-bit addresses (MOVX @ DPTR). In this application, Port 2 uses strong internal pullups when emitting 1s. During accesses to external data memory that use 8-bit addresses (MOVX @ RI), Port 2 emits the contents of the P2 Special Function Register.

Port 2 also receives the high-order address bits and some control signals during Flash programming and verification.

Port 3

Port 3 is an 8 bit bi-directional I/O port with internal pullups. The Port 3 output buffers can sink/source four TTL inputs. When 1s are written to Port 3 pins, they are pulled high by the internal pullups and can be used as inputs. As inputs, Port 3 pins that are externally being pulled low will source current (I_{IL}) because of the pullups.

Port 3 also serves the functions of various special features of the AT89S8252, as shown in the following table.

Port 3 also receives some control signals for Flash programming and verification.

Port Pin	Alternate Functions
P3.0	RXD (serial input port)
P3.1	TXD (serial output port)
P3.2	$\overline{INT0}$ (external interrupt 0)
P3.3	$\overline{INT1}$ (external interrupt 1)
P3.4	T0 (timer 0 external input)
P3.5	T1 (timer 1 external input)
P3.6	$\overline{WR}$ (external data memory write strobe)
P3.7	$\overline{RD}$ (external data memory read strobe)

RST

Reset input. A high on this pin for two machine cycles while the oscillator is running resets the device.

ALE/$\overline{PROG}$

Address Latch Enable is an output pulse for latching the low byte of the address during accesses to external memory. This pin is also the program pulse input ($\overline{PROG}$) during Flash programming.

In normal operation, ALE is emitted at a constant rate of 1/6 the oscillator frequency and may be used for external timing or clocking purposes. Note, however, that one ALE pulse is skipped during each access to external data memory.

If desired, ALE operation can be disabled by setting bit 0 of SFR location 8EH. With the bit set, ALE is active only during a MOVX or MOVC instruction. Otherwise, the pin is weakly pulled high. Setting the ALE-disable bit has no effect if the microcontroller is in external execution mode.

$\overline{PSEN}$

Program Store Enable is the read strobe to external program memory.

When the AT89S8252 is executing code from external program memory, $\overline{PSEN}$ is activated twice each machine cycle, except that two $\overline{PSEN}$ activations are skipped during each access to external data memory.

$\overline{EA}$/VPP

External Access Enable. $\overline{EA}$ must be strapped to GND in order to enable the device to fetch code from external program memory locations starting at 0000H up to FFFFH. Note, however, that if lock bit 1 is programmed, EA will be internally latched on reset.

$\overline{EA}$ should be strapped to V_{CC} for internal program executions. This pin also receives the 12-volt programming enable voltage (V_{PP}) during Flash programming when 12-volt programming is selected.

XTAL1

Input to the inverting oscillator amplifier and input to the internal clock operating circuit.

XTAL2

Output from the inverting oscillator amplifier.

Table 1. AT89S8252 SFR Map and Reset Values

0F8H									0FFH
0F0H	B 00000000								0F7H
0E8H									0EFH
0E0H	ACC 00000000								0E7H
0D8H									0DFH
0D0H	PSW 00000000					SPCR 000001XX			0D7H
0C8H	T2CON 00000000	T2MOD XXXXXX00	RCAP2L 00000000	RCAP2H 00000000	TL2 00000000	TH2 00000000			0CFH
0C0H									0C7H
0B8H	IP XX000000								0BFH
0B0H	P3 11111111								0B7H
0A8H	IE 0X000000		SPSR 00XXXXXX						0AFH
0A0H	P2 11111111								0A7H
98H	SCON 00000000	SBUF XXXXXXXX							9FH
90H	P1 11111111						WMCON 00000010		97H
88H	TCON 00000000	TMOD 00000000	TL0 00000000	TL1 00000000	TH0 00000000	TH1 00000000			8FH
80H	P0 11111111	SP 00000111	DP0L 00000000	DP0H 00000000	DP1L 00000000	DP1H 00000000	SPDR XXXXXXXX	PCON 0XXX0000	87H