SKRIPSI

PERENCANAAN DAN PEMBUATAN ALAT PEMADAM BAHAYA KEBAKARAN *(FIRE ALARM)* DENGAN APLIKASI SENSOR ASAP, SENSOR SUHU DAN SENSOR AIR YANG DILENGKAPI INFORMASI SUARA BERBASIS MIKROKONTROLLER AT89S8252

Disusun Oleh :

RADHITHYA PURBO SANTIKO

NIM : 02.17.068

JURUSAN TEKNIK ELEKTRO S-1

KONSENTRASI TEKNIK ELEKTRONIKA

FAKULTAS TEKNOLOGI INDUSTRI

INSTITUT TEKNOLOGI NASIONAL MALANG

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LEMBAR PERSETUJUAN

PERENCANAAN DAN PEMBUATAN ALAT PEMADAM BAHAYA KEBAKARAN(*FIRE ALARM*) DENGAN APLIKASI SENSOR ASAP, SENSOR SUHU DAN SENSOR AIR YANG DILENGKAPI INFORMASI SUARA BERBASIS MIKROKONTROLLER AT89S8252

SKRIPSI

Disusun Dan Diajukan Sebagai Salah Satu Syarat Untuk Memperoleh Gelar Sarjana Teknik Elektronika Strata Satu(S-1)

Disusun oleh:

RADHITHYA PURBO SANTIKO
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2007

INSTITUT TEKNOLOGI NASIONAL MALANG
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"Ada Kemauan Ketekunan dan Itikad Yang Baik Pasti Allah S.W.T Berikan Jalan Dan Orang Yang Sukses Ialah Orang yang Tak Menunda-nunda Pekerjaanya...Aku Sangat Menghormati dan Menghargai Sang Waktu..."

Penulis

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BAB I

PENDAHULUAN

1.1. LATAR BELAKANG

Sehubungan dengan perkembangan pola pikir manusia ilmu pengetahuan dan tekonologi ternyata mengalami kemajuan secara terus-menerus. Perbaikan terhadap teknologi yang sudah ada terus dilakukan agar lebih menjadi lebih mudah. Salah satu bidang tekonologi yang mengalami perkembangan lebih pesat adalah teknologi kontrol otomatis yang berkembang pesat seiring dengan perkembangan jaman. Telah banyak kontrol otomatis yang dibuat dan diaplikasikan untuk keperluan industri, layanan umum maupun untuk penelitian.

Dewasa ini perkembangan khususnya dibidang pembangunan gedung – gedung bertingkat semakin pesat, sehingga dapat menimbulkan persoalan yang komplek terhadap kerawanan terjadinya kebakaran. Kebakaran merupakan suatu bencana yang sangat merugikan. Dalam penanggulangan masalah kebakaran banyak sekali ditemukan kesulitan-kesulitan seperti sukarnya ditemukan sumber api secara dini dan sumber air yang jauh sehingga api akan terus membesar dan menjalar ketempat lain dan kerugianpun akan semakin besar.

Mengacu hal tersebut sudah sepantasnya faktor jaminan keamanan merupakan hal yang sangat penting, untuk mengatasi hal tersebut diperlukan suatu alat yang mampu untuk mendeteksi secara dini dan memperkecil kemungkinan meluasnya api. Secara konvensional biasanya digunakan suatu detektor (sensor) yang dihubungkan

secara langsung dengan alarm sehingga bila terjadi kebakaran akan langsung berbunyi dan lampu sirene akan menyala.

Melihat kenyataan tersebut diatas maka dalam penyusunan tugas akhir ini, penyusun mengaplikasikan pengamanan kebakaran secara otomatis dengan menggunakan mikrokontroller sebagai sentral dari aplikasi kinerja semua *system* yang bekerja melalui instruksi-instruksi program.

1.2. RUMUSAN MASALAH

Sehubungan dengan latar belakang diatas maka yang menjadi rumusan masalah adalah:

"Bagaimana merencanaan dan membuat alat pendeteksi serta pengaman bahaya kebakaran (*fire alarm*) dengan aplikasi sensor asap, sensor suhu dan sensor air yang dilengkapi informasi suara berbasis Mikrokontroller AT 89S8252."

1.3. BATASAN MASALAH

Agar lebih mudah memahami pokok bahasan, maka masalah yang ada dalam perencanaan dan pembuatan alat ini akan dibatasi pada hal-hal sebagai berikut:

a. Menggunakan Mikrokontroller AT 89S8252.
b. Sensor yang digunakan berupa sensor suhu LM35, sensor asap tipe AF 30 dan sensor air.
c. Tidak membahas catu daya
d. Perangkat keras yang digunakan dibahas secara umum

1.4. TUJUAN

Tujuan dari tugas akhir ini adalah merancang dan membuat alat yang efektif dan efisien yang mampu untuk mendeteksi api secara dini dan memperkecil kemungkinan meluasnya api serta dilakukan tindakan awal untuk penanggulangannya.

1.5. METODOLOGI PENELITIAN

Untuk menyelesaikan semua permasalahan dan mencapai tujuan seperti tersebut diatas maka metodologi penulisan yang diambil adalah:

1. Kajian Pustaka: dimaksudkan untuk mengumpulkan semua literatur yang mendukung tentang perencanaan dan pembuatan alat.
2. Perancangan dan pembuatan alat: bertujuan untuk mempermudah dalam melakukan perancangan dan pembuatan alat sesuai dengan rencana yang disusun.
3. Studi analisis alat: studi ini dimaksudkan untuk mengetahui apakah alat yang telah dibuat berfungsi sesuai dengan apa yang kita rencanakan.

1.6. SISTIMATIKA PENULISAN

Tugas akhir ini disusun berdasarkan beberapa teori penunjang serta bagian-bagian dari perencanaan alat yang menjadikan tugas akhir ini dibagi menjadi lima bab dan beberapa sub bab. Inti dari penyusunan tugas akhir ini dapat diuraikan sebagai berikut:

BAB I : PENDAHULUAN

Berisi pendahuluan yang meliputi latar belakang , tujuan, rumusan permasalahan, ruang lingkup masalah, metodologi penelitian dan sistimatika penulisan.

BAB II : TEORI PENUNJANG

Berisi dasar teori yang akan digunakan pada perencanaan dan pembuatan alat.

BAB III : PERENCANAAN DAN PEMBUATAN ALAT

Menguraikan mengenai perencanaan, meliputi perancangan *hardware* dan *software* dari keseluruhan alat.

BAB IV : PENGUJIAN ALAT

Melaporkan hasil pengujian dan pembuatan dari hasil perancangan dan pembuatan alat.

BAB V : PENUTUP

Pada bab ini akan disampaikan kesimpulan dari perancangan dan pembuatan sistem ini.

BAB II

TEORI DASAR

2.1. Pendahuluan

Pada bab ini akan dibahas mengenai teori penunjang dari peralatan yang direncanakan. Teori penunjang ini akan membahas tentang komponen dan peralatan pendukung pada alat yang dibuat. Pokok pembahasan pada bab ini adalah :

1. Karbon Monoksida
2. Sensor Karbon Monoksida
3. Sensor Suhu
4. ADC 0808
5. Komunikasi data serial RS 485
6. *Information Storage Device* (ISD 1420)
7. *Liquid Crystal Display* (LCD) M1632
8. Mikrokontroler AT89S8252 dan
9. Mikrokontroler AT89S52

2.2. Karbon Monoksida (CO)

Karbon monoksida (CO) adalah suatu komponen tidak berwarna, tidak berbau dan tidak mempunyai rasa yang terdapat dalam bentuk gas pada suhu diatas -192 °C. Komponen yang mempunyai berat sebesar 96,5% dari berat air dan tidak larut didalam air. Karbon monoksida (CO) yang terdapat dialam terbentuk dari salah satu proses seperti berikut:

1. Pembakaran tidak lengkap terhadap karbon (C) atau komponen yang mengandung karbon.
2. Reaksi antara karbon dioksida (CO_2) dan komponen yang mengandung karbon pada suhu tinggi.
3. Pada suhu tinggi, karbon dioksida (CO_2) terurai menjadi karbon monoksida (CO) dan oksida (O).

Oksidasi tidak lengkap terhadap karbon atau komponen yang mengandung karbon terjadi jika jumlah oksigen yang tersedia kurang dari jumlah yang dibutuhkan untuk pembakaran sempurna dimana dihasilkan karbon dioksida (CO_2). Pembentukan karbon monoksida (CO) hanya terjadi jika reaktan yang ada terdiri atas karbon (C) dan oksigen (O_2) murni. Jika yang terjadi adalah pembakaran komponen yang mengandung karbon diudara, prosesnya lebih kompleks dan terdiri dari beberapa tahap reaksi. Reaksi ini sering terjadi pada suhu tinggi yang umumnya terdapat pada industri.

Berbagai proses alam juga memproduksi karbon monoksida (CO), misalnya aktivitas vulkanik, emisi gas alami, dan lain-lain. Tetapi kontribusi karbon monoksida ke atmosfer yang disebabkan oleh proses alam tersebut relatif kecil, sedangkan aktivitas manusia yang menghasilkan karbon monoksida (CO) dan melepas ke atmosfer lebih banyak dan nyata, misalnya transportasi dan proses industri.

Pada umumnya konsentrasi karbon monoksida (CO) di udara kurang dari 110 ppm. Jika terjadi kontak antara manusia dengan karbon monoksida (CO) pada konsentrasi tinggi dapat menyebabkan kematian, sedangkan pada konsentrasi yang relatif rendah (110 ppm atau kurang) dapat mengganggu kesehatan. Faktor penting yang menentukan pengaruh karbon monoksida (CO) terhadap manusia adalah konsentrasi COHb yang

terdapat dalam darah, dimana semakin tinggi persentasi hemoglobin (Hb) yang terikat dalam bentuk COHb, semakin parah pengaruhnya terhadap kesehatan manusia. Hubungan antar konsentrasi COHb didalam darah dan pengaruhnya terhadap kesehatan dapat dilihat pada tabel 2-1.

Tabel 2-1. Pengaruh Konsentrasi COHb di Dalam Darah[1]

Jumlah Gas CO Dalam darah(%)	Gejala-gejala (akibatnya)
0-5	Tidak ada gejala (normal)
5-10	Aliran darah meningkat sakit kepala ringan
10-20	Tegang daerah dahi, sakit kepala, penglihatan agak terganggu
20-30	Sakit kepala sedang, berdenyut-denyut, dahi, wajah merah dan mual.
30-40	Sakit kepala berat, mual, muntah, lemas, mudah terganggu pingsan pada saat bekerja.
40-50	Sakit kepala hebat, badan lemas, pandangan kabur, mual, muntah, jatuh dan pingsan, denyut nadi dan pernafasan bertambah.
50-60	Sinkope, pernafasan dan denyut nadi bertambah, koma dengan sebentar kejang-kejang.
60-70	Koma dengan kejang-kejang, kerja jantung dan pernafasan tertekan dan bisa mati.
70-80	Denyut jantung sangat lemah, pernafasan lambat, kegagalan pernafasan dan menyebabkan kematian.

2.3. Sensor Karbon Monoksida (AF-30)

Fungsi dari sensor adalah menerima beberapa aksi dari fenomena tunggal dari subyek yang diukur dan mengubahnya menjadi fenomena fisik yang dapat dilihat secara mudah. Fenomena yang mendukung subyek yang diukur dinamakan sinyal masukan dan fenomena setelah perubahan disebut sinyal keluaran. Perbandingan sinyal keluaran terhadap sinyal masukan disebut transmisi atau gain. Fungsi dari sensor adalah sebagai

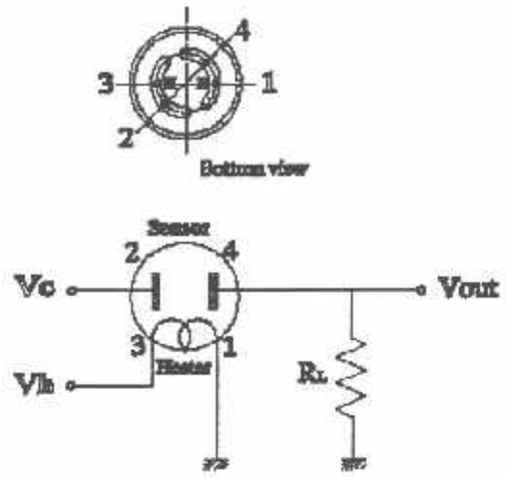
pengkonversi, hasil konversi berupa sinyal keluaran yang akan digunakan untuk mendukung rangkaian tahap berikutnya.

Diharapkan sebuah sensor mampu mendeteksi terjadinya perubahan kuantitas dari subyek yang diukur, sehingga sensor perlu mempunyai sifat-sifat sebagai berikut:

1. *Non Interference*, yang berarti keluaran dari sensor tak berubah oleh adanya faktor lain yang mempengaruhi subyek yang diukur. Proses konversi yang dilakukan oleh sensor seperti ini disebut pengukuran secara langsung. Proses konversi dimana kuantitas pengukuran masih perlu dilakukan perhitungan dari sinyal keluaran yang dihasilkan oleh sensor dinamakan pengukuran secara tidak langsung.
2. *High Sensivity*, jumlah perubahan sinyal keluaran yang dihasilkan oleh karena adanya perubahan pada sejumlah kuantitas masukan yang diukur harus dapat dideteksi, ini berarti sensor harus memiliki gain sebesar mungkin.
3. *Small Measurement Pressure*, ini berarti sensor tidak terganggu oleh kondisi fisik dari subyek yang diukur. Dari gambaran ini maka konversi metode modulasi mempunyai prioritas yang baik untuk pengukuran secara langsung.
4. *High Speed*, ini berarti sensor harus mempunyai kecepatan yang cukup tinggi untuk berubah sinyal keluarannya bila terjadi perubahan pada kuantitas yang diukur.
5. *Low Noise*, ini berarti noise internal yang dibangkitkan oleh sensor harus sekecil mungkin.
6. *Robustness*, sensor harus tahan terhadap kondisi lingkungan pemakaiannya dan noise dari luar serta mudah pemakainnya.

Dalam skripsi ini sensor yang digunakan adalah sensor gas seri AF (Scimarec) tipe 30 yang terbuat dari bahan semikonduktor yang memiliki kinerja, kualitas dan ketahanan jangka panjang. Elemen semikonduktor yang memiliki kinerja, kualitas dan ketahanan jangka panjang. Elemen semi konduktor yang mendeteksi gas dipanaskan pada salah satu sisi bahan keramik, selanjutnya ditutup dengan keramik film untuk melindungi terhadap debu. Sebuah *microheater* dipasang pada bagian belakang lapisan, dengan demikian cepat memanaskan element pendeteksi gas pada suhu operasi yang diinginkan.

Elemen yang merasakan gas adalah suatu semikonduktor oksida yang dipanaskan sampai 350 °C. Jika berhadapan dengan gas yang sesuai, oksigen dipermukaan akan diserap untuk digunakan dan tahanannya akan menurun. Penurunan tahanan ini mengikuti pola yang dapat diprediksi dan berulang-ulang. Dimana keluaran sensor tersebut adalah berupa selisih tegangan, yaitu saat sensor dipengaruhi oleh gas Karbon Monoksida (CO) tegangan tersebut akan naik sesuai dengan banyaknya gas Karbon Monoksida (CO) yang diterima olch sensor. Sensor gas CO ini mempunyai 4 pin dimana pin 3 dan 1 berfungsi sebagai *heater* sedangkan pin 2 dan 4 berfungsi sebagai sensor Karbon Monoksida (CO).



Gambar 2-1. Konfigurasi pin-pin AF-30[2]

Sensor gas ini dirancang untuk beroperasi dengan tegangan 5V. Ketika sensor mendeteksi gas, tahanan sensor akan menurun. Tahanan sensor (RS) ini dihitung dari tegangan keluaran (Vout) dengan menggunakan rumus sebagai berikut :

$$RS = \frac{Vc - Vout}{Vout} xRLoad \quad \text{.....(1)}$$

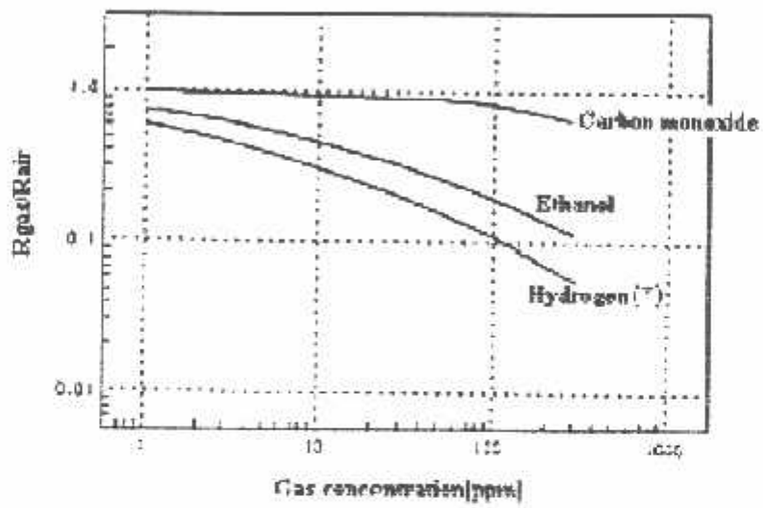
Sensivitas menunjukkan rasio (R_{GAS}/R_{UDARA}) dari tahanan sensor yang diperoleh dalam udara yang berisi gas (R_{GAS}) untuk tahanan sensor yang diperoleh di udara bersih tanpa pencemaran gas (R_{UDARA}).

Satuan dari kadar gas Karbon Monoksida (CO) adalah ppm *(part per million)* yaitu banyaknya kadar gas CO dalam satu milimeter kubik, yang didefinisikan sebagai berikut :

$$1\ ppm = \frac{1\ volume\ gas\ pencemar}{10^6\ volume\ (udara + pencemar)}$$

atau 0.0001 persen volume = 1 ppm.

Maka pada grafik berikut menunjukkan hubungan antara perubahan resistansi sensor dengan konsentrasi gas karbon monoksida (CO). Sumbu Y menunjukkan perbandingan dari resistansi gas (R_{GAS}) dengan resistansi atmosphere (R_{AIR}).



Grafik 2-1. Respon Sensor Terhadap Gas CO[3]

2.4. Sensor Suhu LM35

Sensor suhu merupakan suatu komponen yang mudah untuk mengalami perubahan tegangan dan arus. Apabila terjadi perubahan suhu pada suatu kondisi tertentu. Sensor suhu yang dipakai adalah IC LM35 yang nilai hambatannya berubah terhadap perubahan suhu.

Tegangan output pada IC LM35 adalah sebanding dengan derajad(^{0}) temperature serta menghasilkan kenaikan tegangan sekitar 10 mv pada setiap kenaikan suhu 1^0C.

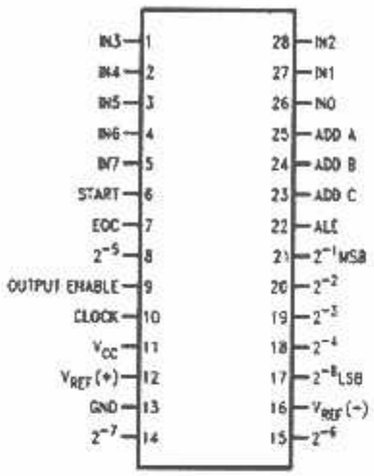
LM35 mempunyai keuntungan lebih linier dari sensor temperature yang disesuaikan pada ^{0}K sehingga penggunaannya tidak diharuskan untuk mengurangi besar tegangan konstan dari output yang mendapatkan skala tetap. Adapun kelebihan lain dari jenis IC ini, tidak memerlukan banyak pengkalibrasian khusus pada temperature ruang 1/4 ^{0}C dan 3/4^{0}C lebih besar.

2.5. ADC 0808

Agar dapat mengukur atau mengubah suatu besaran fisik yang umumnya dalam bentuk analog dengan piranti digital, variabel tersebut harus terlebih dahulu diubah menjadi variable digital yang nilainya proporsional dengan nilai variable yang akan diukur/diolah tersebut. Proses konversi ini dilakukan oleh konverter analog ke digital (*Analog Digital To Conversion*).

Spesifikasi penting lain selain ketelitian (akurasi) dan linieritas adalah waktu konversi (*confersion time*). Waktu konversi ADC adalah waktu yang diperlukan untuk menghasilkan kode biner yang valid untuk tegangan masukan yang diberikan. Semakin pendek waktu konversi berarti kecepatan konversi semakin tinggi.

Dalam pembuatan alat ini digunakan ADC jenis 0808 yang mempunyai 8 bit *channel multiplekser* dan menggunakan metode pendekatan *Succesive Approximation Register* (SAR). Waktu konversi (*conversion time*) ADC ini adalah 100µs dengan rentangan input sebesar 0 sampai dengan 8 V dan supply sebesar 5 V.



Gambar 2-2. Konfigursi Pin-pin ADC0808[4]

2.6. RS 485

2.6.1. Sistem Komunikasi RS485

Standar RS485 diterapkan oleh *Electronic Industry Association* (EIA) dan *Telekomunikasi Industry Association* (TIA) pada tahun 1983. Standar RS485 hanya membicarakan karakteristik sinyal dalam transmisi data secara *Balanced Digital Multipoint System*. Jadi jauh lebih sederhana dibanding dengan standar RS232 yang mencakup ketentuan tentang karakteristik sinyal, macam-macam sinyal dan konektor yang dipakai maupun konfigurasi sinyal pada kaki-kaki konektor beserta tata cara pertukaran informasi antara komputer dan alat-alat pelengkapnya.

RS485 merupakan kabel komunikasi serial yang bisa mencapai jarak 4000 yard dengan kecepatan lebih dari 1 Megabit/detik, dan pada jarak yang lebih pendek kecepatan transmisi RS484 sekitar 10 Megabit/detik.

Pada RS485 menggunakan saluran ganda (*Differential* atau *Unbalanced Transmission*). Transmisi ini memakai satu pasang kabel untuk mengirim satu sinyal, informasi logika ditafsirkan dari beda tegangan antara dua utas kabel saluran. Tegangan

pada kedua utas kabel saluran selalu berlawanan, saat satu kabel bertegangan tinggi maka kabel yang lain bertegangan rendah, demikian pula sebaliknya, Rangkaian penerima sinyal membandingkan tegangan kedua kabel saluran, level logika pada bagian output ditentukan oleh kabel mana yang lebih positif. Meskipun demikian, saluran ganda tidak dipakai untuk transmisi yang memerlukan banyak saluran mengingat RS485 memakai kabel jauh lebih banyak sehingga mahal. Untuk penghematan kabel, bahkan saluran ganda sering dipakai untuk saluran *Half Duplex* yaitu saluran dua arah secara bergantian yang hanya menggunakan satu pasang kabel, bisa dipakai untuk menghubungkan line generator dan banyak line receiver menjadi satu, sistem ini disebut sebagai komunikasi multidrop (*Multipoint Communication*).

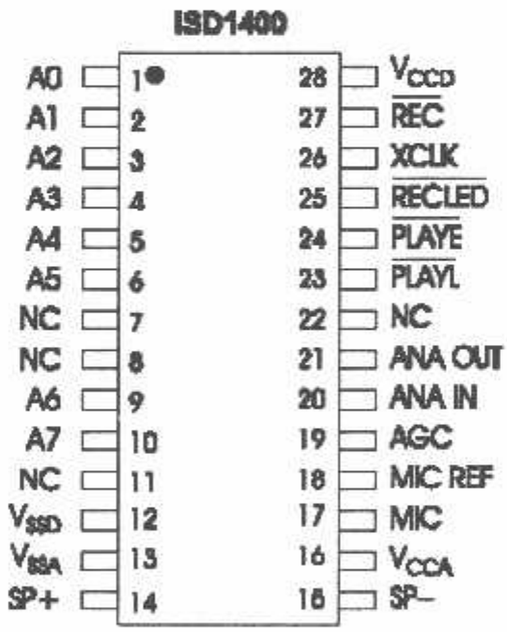
RS485 mempunyai keuntungan dibanding dengan RS232 dimana ratio tegangan operasionalnya cukup rendah yaitu -7 Volt sampai dengan +7 Volt dibandingkan dengan RS232 yaitu -13 Volt sampai dengan +13 Volt. Dengan tegangan operasi setinggi itu kemungkinan akan dapat mempengaruhi bahkan dapat mengakibatkan kerusakan perangkat lain yang tersambung dengannya.

2.7. IC Penyimpan Suara (ISD 1420)

IC penyimpan suara yang digunakan merupakan jenis EEPROM (*Electrically Erasable Programable Read Only Memory*) yaitu ROM yang dapat diprogram, dihapus dan diprogram ulang secara elektrik dengan arus listrik, bukan sinar ultraviolet. IC ISD yang dipakai yaitu ISD 1420 (*Information Strorage Device*), IC dapat merekam pesan maksimal 20 detik dan dapat dikaskade sehingga pesan yang disimpan dapat diperpanjang sesuai dengan keinginan kita dengan 160 alamat yang berbeda.

Rekaman akan disimpan dalam sel memori yang tidak mudah hilang (*non volztile*), memberikan tempat penyimpanan yang masih kosong. Cara unik ini yang membuat ISD disebut *Stroge Technolgi Direct Analog* (DAST) atau teknik penyimpanan analog langsung, dengan jalan sinyal suara (*voice*) dan bunyi disimpan secara langung dalam bentuk analog, kedalam memori EPROM. Penyimpanan analog langsung memungkinkan reproduksi suara secara alami dalam satu chip tunggal.

Susunan ISD 1420 DAST adalah dikelompokkan dalam 160 segmen dari alamat A0 sampai A7 yang menunjukkan akses tips segmen dalam kesatuan untuk alamat pesan. Kemampuan pemberian atau penyediaan alamat yang berupa pesan yang disimpan dalam bentuk kalimat dan suara.



Gambar 2-3 Struktur Pin IC ISD 1420[5]

Keterangan :

- **Address Input (A0-A7) Pin 1-6 Dan 9-10**

  Input alamat ini mempunyai dua fungsi,tergantung dari level dari dua *Most Significant Bits* (MSB) dari alamat. Jika dua MSB ini keduanya *low*, maka semua input digunakan sebagai bit pengalamatan (*Address Bits*) dan digunakan sebagai alamat untuk memulai (*Start Address*) dai perekaman atau pemutaran ulang (*Play Back*). Kaki-kaki dari pengalamat hanya meupakan masukan dan bukan merupakan informasi keluaran pengalamatan internal (*Output Internal Address Information*). Ketika proses operasional sedang berjalan dan pada saat kedua MSB ini high, maka sinyal input pengalamatan digunakan sebagai bits mode (*Mode Bit*) yang membuat mode operasi normal dan pengalamatan secara tidak langsung (*Simultanously*).

- **Vssd dan Vssa (Ground) Pin 12 dan 13**

  Sama seperti Vccd dan Vcca, analog input dan digital sirkuit didalam ISD1420 menggunakan bus ground yang terpisah untuk meminimalisasi noice. Pin ini harus dihubungkan sedekat mungkin dengan ground.

- **Speaker Output (SP +, SP -) Pin 14 dan 15**

  Pin SP + dan SP –digunakan untuk mengeluarkan suara yang telah direkam ke speaker atau ke *device* lainnya. Output ini mempunyai impedansi sebesar 16 Ohm.

- **Microphone Input (mic) Pin 17**

  Kaki mikropon ini terhubung dengan Vcc melalui beberapa kapasitor yang terhubung secara seri, bersamaan dengan resistor 10KΩ yang berada didalam chip (*internal*). Harga dari kapasitor dari dalam perancangan tugas akhir ini menggunakan harga kapasitor sesuai dengan yang tertera dalam rangkaian data sheet ISD 1420.

- **Microphone Reference (MIC REF) Pin 18**

  Ketika MIC REF menghubungkan antara Vcc dengan mikropon Ground, maka tingkat *noice* selama perekaman dapat dikurangi. *Noise* itu disebabkan oleh preamplifier yang terdapat didalam chip. Bila pin ini tidak digunakan, maka tidak boleh dihubungkan dengan sinyal atau dengan tegangan apapun, harus dalam keadaan terbuka.

- **Automatik Gain Control (AGC) Pin 19**

  Kegunaan dari AGC adalah untuk menambah atau mengurangi secara otomatis penguatan (*Gain*) dari preamplifier yang juga meluaskan batas dari sinyal input yang dapat digunakan oleh mikropon tampa terjadi *distorsi*. AGC ini dapat secara dinamis meluaskan batas dari suara yang terekam baik itu suara bisikan sampai suara yang keras. Untuk menggunakan fasilitas AGC ini, resistor dan kapasitor luar (*Eksternal*) harus dihubungkan secara paralel antara pin AGC dengan ground. Harga yang direkomendasikan adalah R = 470 KΩ dan C = 4,7 µF (Dalam perancangan tugas akhir ini juga dipakai harga seperti diatas sama dengan data sheet ISD).

- **Analog Input (ANA IN) Pin 20**

  Kapasitor eksternal (luar) menghubungkan antara ANA IN ke ANA OUT pin harga-harga dari kapasitor luar bersama dengan 3 KΩ input impedansi di ANA IN dapat dipilih sendiri untuk memberikan keadaan *cut off* (terputus) pada frekuensi rendah sampai pada pass band suara. ANA IN juga dapat digunakan pada input sumber alternative dari sinyal analog pada sinyal mikropon terus ke kapasitor kopling.

- **Analog Output (ANA OUT) Pin 21**

  Sinyal dari mikropon dikuatkan dan dikeluarkan melalui ANA OUT pin. Penguatan tegangan dari preamp tergantung dari tingkat tegangan AGC (*Automatik Gain Control*) pin. Preamplifier ini mempunyai penguatan maksimum sekitar 24 dB untuk tingkat masukan kecil.

- **Playback, Level – Aktivated (PLAY L) Pin 23**

  Ketika sinyal ini berpindah dari *high* ke *low*, maka PLAY L akan berjalan. *Playback* akan berjalan sampai input ini tertekan *high*, tanda akhir dari pesan tercapai atau ruang memori sudah habis. ISD akan kembali ke mode *standby* setelah *playback* ini berhenti.

- **Playback,Edge-Aktivated (PLAY E) Pin 24**

  Ketika sinyal akan bepindah menuju *low* (*low-going transition*) terdeteksi di input ini, maka PLAY E akan berjalan. *Playback* berjalan sampai tanda akhir dari pesan tercapai (Akhir dari ruang memori tercapai). Setelah menyelesaikan *playback*, ISD secara otomatis akan kembali ke mode *standby*, menekan PLAY E ke *high* pada waktu *playback* berjalan tidak

akan menghentikan *playback*. Jadi *playback* akan berhenti bila mencapai akhir dari pesan atau ruang memori habis.

- **Record LED Output (RECLED) Pin 25**

  Selama proses perekaman output RECLED akan *low*. Maka output ini bisa digunakan untuk menjalankan sebuah led bergunanya untuk mengetahui bahwa terjadi proses perekaman. Ketika tanda akhir dari pesan tercapai pada saat playback, maka RECLED akan *low* sebentar.

- **Optimal External Clock (XCLK) Pin 26**

  Digunakan untuk penambahan kristal clock bila dibutuhkan pewaktuan yang lebih besar dan presisi. Bila input ini tidak digunakan, harus dihubungkan dengan ground.

- **Record (REC) Pin 27**

  Input sinyal REC akan aktif dalam kondisi *low*. ISD 1420 akan merekam bila REC dalam keadaan *low*, dan sinyal ini harus terus dalam keadaan *low* bila ingin terus merekam. Jika input REC ini tertekan *low* dalam keadaan masih memutar ulang pesan (*playback*), maka *playback* akan berhenti dan ISD akan merekam.

- **VCCA Dan VCCD Pin 16 Dan 28**

  Analog dan digital sirkuit yang terdapat didalam chip ISD 1420 menggunakan bus power yang terpisah untuk meminimalisasi *noise*. Pin power ini harus dihubungkan sedekat mungkin dengan sumber tegangan.

2.8. LCD *(Liquid Crystal Display) M1632*

LCD *(Liquid Cristal Display)* adalah suatu jenis piranti *output* yang menggunakan daya rendah dengan pengontrol kontras dan kecerahan. Pengontrol utamanya dan karakter ada pada ROM *(Read Only Memory) generator* dan *display* data RAM *(Random Access Memory)* yang akan menghasilkan *extended key codes* (kode tombol keyboard standart *international* dalam Hexsa) jika padanya diberikan inputan. Untuk dapat memfungsikan dengan baik maka perlu diperhatikan proses inisialisasi yang telah ditentukan oleh pabrik pembuatnya. *Timing* penginisialisasian sangat perlu dipertimbangkan, karena jika meleset sampai orde *secon,* maka dapat dipastikan LCD itu tidak dapat berfungsi.

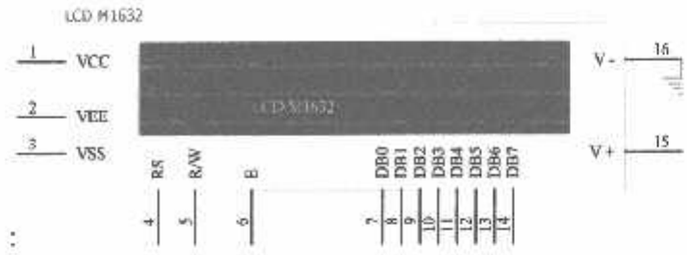
Ada dua jenis *register* yang terdapat dalam LCD M1632 ini, yaitu *data register dan instruction register.* Dengan menggunakan pin RS *(Register Select)* pada LCD, pemakaian kedua *register* dapat dipilih. Pemilihan *register* pada LCD ditunjukkan dalam tabel 2.9 berikut ini

Tabel 2.2
Pemilihan *Register* Pada LCD M I632

Nama Sinyal	No. Terminal	I/O	Tujuan	Keterangan Sinyal
RS	4	Input	MPU	0 : Instruction Register 1 : Data Register

Jika bagian yang dipilih adalah *instruction register* maka output yang dihasilkan adalah meliputi operasional dari LCD, misalnya fungsi *display clear, cursor home, entry mode set, display on/off, cursor shift* dan sejenisnva. Sebaliknya jika bagian yang dipilih adalah *data register, output* yang dihasilkan adalah meliputi karakter yang tabelnya terdapat pada lampiran.

Berikut adalah gambar dari LCD dengan pin-pin yang akan terhubung dengan mikrokontroller AT89S8252 :



Gambar 2.4 Rangkaian LCD M1632[6]

LCD M1632 mempunyai spesifikasi sebagai berikut :

- 16 karakter 2 bans dalam bentuk *dot matrik 5 x* 7 dan kursor.
- *Duty ratio* 1/16.
- Memiliki ROM pembangkit karakter untuk 192 jenis karakter.
- RAM untuk data *display* sebanyak 80 x 8 bit (80 karakter maksimum).
- Dapat dirangkai dengan MPU *(Microprocesor Unit) 8* bit atau 4 bit.
- RAM data *display* dan RAM pembangkit karakter dibaca oleh *MPU.*
- Memiliki fungsi instruksi : display ON/OFF, cursor ON/OFF, *display character blink, cursor shift* dan *display shift.*
- Memiliki rangkaian *oscillator* sendiri.
- Sumber tegangan tunggal *+5* Volt.
- Memiliki rangkaian *reset* otomatis pada saat catu daya dihidupkan.
- Temperatur operasi 0° – *50°.*

LCD modul M1632 mempunyai 16 pin sebagai berikut :

Table 2.3
Fungsi pin-pin LCD M1632

No Pin	Nama Pin	Fungsi
1	Vss	Terminal Ground
2	Vcc	Tegangan catu 5 Volt
3	Vcc	Mengendalikan kecerahan LCD
4	RS	Sinyal pemilihan Register 0= Tulis 1= Baca
5	R/W	Sinyal Seleksi atau baca 0= Tulis 1= Baca
6	E	Sinyal operasi awal yang mengaktifkan data tulis atau baca
7-14	DB0-DB7	Merupakan saluran data berisi perintah data yang akan ditampilkan
15	V+BL	Back Light Supply 5Volt
16	V-BL	Back Light Supply Ground

Pada LCD juga terdapat instruksi – instruksi sebagai berikut :

1. *Display clear*: membersihkan tampilan yang ada pada LCD serta menyimpan, sedangkan kursor kembali ke posisi semula.
2. *Cursor home* : hanya membersihkan tampilan dan kursor kembali ke semula.
3. *Empty mode Set* : layar beraksi sebagai tampilan tulis.

   S : 1/0 = menggeser layar.

   1/0 : 1 = kursor bergerak ke kanan dan layar bergerak ke kiri.

   1/0 : 0 = kursor bergerak ke kiri dan layar bergerak ke kanan
4. Display On/Off kontrol.

D : 1 = layar on

D : 0 = layar off

C : 1 = kursor on

C : 0 = kursor off

B : 1 = kursor berkedip-kedip

B : 0 kursor tidak berkedip – kedip

5. *Cursor Display Shift*

S/C : 1 = LCD diidentifikasikan sebagai layar

S/C : 0 = LCD diidentifikasikan sebagai kursor

R/L : 1 = menggeser satu spasi ke kanan

R/L : 0 = menggeser satu spasi ke kiri

6. *Fuction Set*

DL : 1 – panjang data LCD pada 8 bit

DL : 0 = panjang data LCD pada 4 bit

Bit upper ditransfer terlebih dahulu kemudian diikuti dengan 4 bit lower.

N : 1/0 = LCD menggunakan 2 atau 1 baris karakter

P : 1/0 = LCD menggunakan 5 x 10 dot matrik

7. CG RAM *address set* : menulis alamat RAM ke karakter

8. DD RAM *address set* : menulis alamat RAM ke tampilan

9. BF/*address set* : BF = 1/0, LCD dalam keadaan sibuk atau tidak sibuk.

10. Data *write* to CG RAM or DD RAM : membaca byte dari alamat terakhir RAM yang dipilih.

2.9. Mikrokontroller AT89S8252

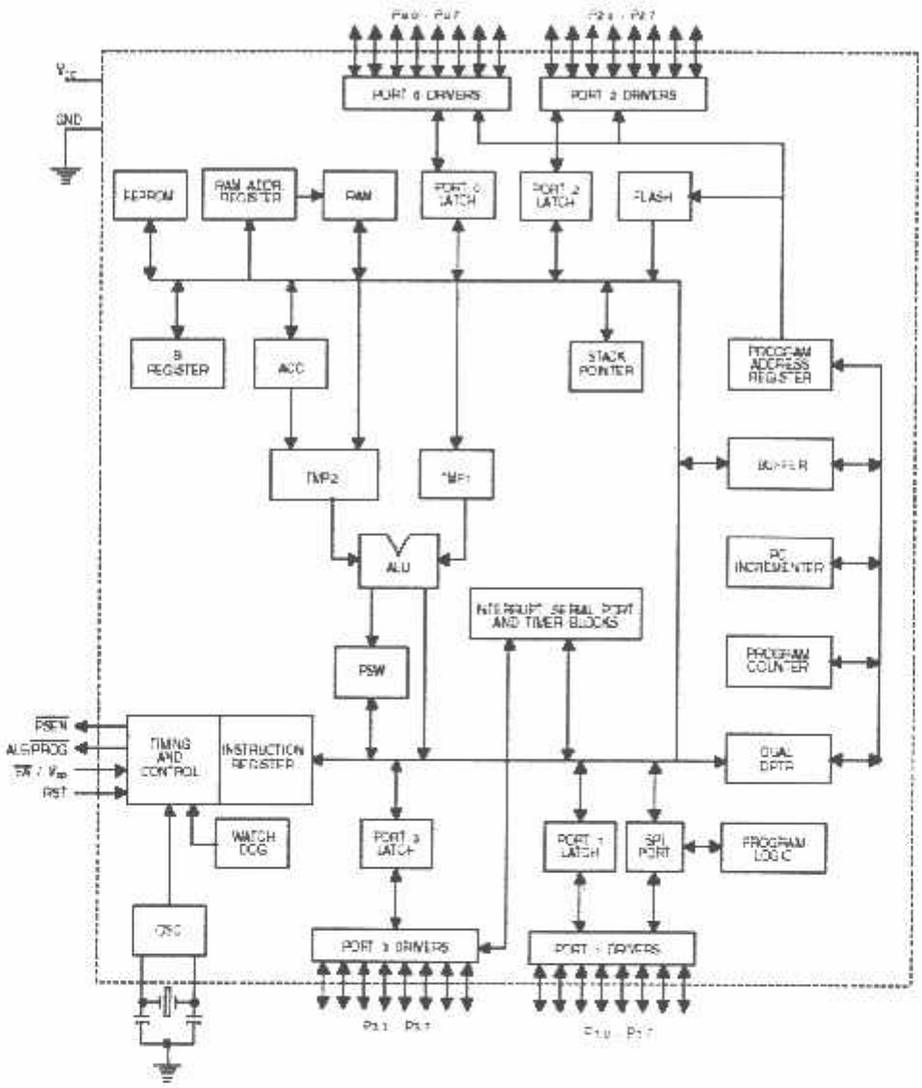
2.9.1 Pendahuluan

Perbedaan mendasar antara mikrokontroller dan mikroprosesor adalah jika mikrokontroller selain memiliki CPU *(Central Processing Unit)* juga dilengkapi dengan memori dan I/O *(Input/Output)*. Maka mikrokontroller dapat dikatakan sebagai *microcomputer* dalam keping tunggal *(single chip microcomputer) yang* dapat berdiri sendiri.

Mikrokontroller AT89S8252 adalah mikrokontroller keluarga MCS-51 yang membutuhkan daya rendah, memiliki kemampuan yang tinggi, dan merupakan mikrokomputer 8 bit yang dilengkapi 8K *byte Flash* PEROM *(Programmable and Erasable Read Only Memory)* yaitu ROM yang dapat ditulis ulang atau dihapus menggunakan sebuah perangkat *programmer*. Serta terdapat EEPROM *internal* sebesar 2k *Byte*.

Flash PEROM dalam AT89S8252 menggunakan *Atmel 's High-Density Non Volatile Technology* yang mempunyai kemampuan untuk ditulis ulang hingga 1000 kali dan berisikan perintah *standard* MCS-51. Selain itu juga dilengkapi RAM *internal* sebesar 256 *byte*. Dalam sistem Mikrokontroller terdapat dua hal yang mendasar, yaitu: perangkat keras dan perangkat lunak yang keduanya saling terkait dan mendukung.

2.9.2 Perangkat Keras Mikrokontroller AT89S8252



Gambar 2.5
Blok Diagram Mikrokontroller AT89S8252[7]

Mikrokontroller AT89S8252 secara umum memiliki:

- CPU 8 bit
- 8Kbyte FLASH PEROM
- 2 Kbyte EEPROM

- Memory 256 x 8 bit Internal RAM
- 32 Port I/O *Lines*
- 3 *Timer* dan *Counter* 16 bit
- 9 Sumber Interupsi
- SPI *serial interface*
- Oscillator dan clock maksimal 24 MHz
- *Programmable Watchdog Timer*
- *Programmable UART Serial Chanel*
- *Dual Data Pointer*
- *Power-Off Flag*

2.9.3. Arsitektur AT89S8252

Arsitektur Mikrokontroller AT89S8252 adalah sebagai berikut:

1. CPU *(Central Processing Unit)* 8 bit dengan *register A (Accumulator)* & B.
2. 16-bit *Program Counter* (PC) dan *(Data Pointer)* DTPR.
3. 8-bit *Program Status Word (PSW).*
4. 8-bit *Stack Pointer (SP)*
5. 8 *kbyte* Flash PEROM *internal*
6. 256 *byte internal* RAM.
    - bank *register,* masing-masing berisi *8 register*
    - 16 *byte* yang dapat dialamati pada *bit-level.*
    - 208 byte *general purpose memory data.*
7. 32 pin *input-output* tersusun atas PO-P3. masing-masing 8-bit.
8. 3 buah *timer (TO & T1)* dengan masing-masing 16-bit *timer/ counter.*

9. *Receiver/transmiter data* secara *serial full duplex: Serial buffer* (SBUF).

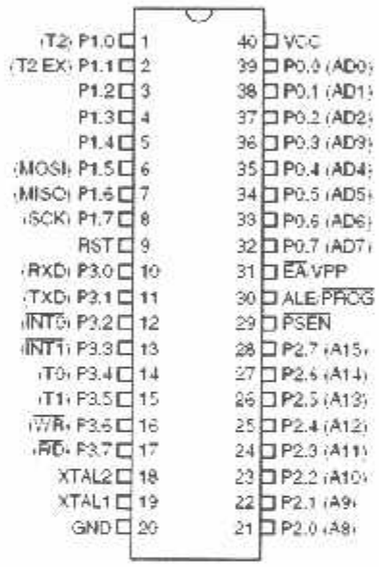
10. *Control register : TCON,* TMOD, SCON, PCON, IP & IE.

11. 9 buah *sumber* interupsi (4 buah sumber interupsi *external dan 5* buah sumber interupsi *internal).*

12. *Oscillator* dan *clock internal.*

2.9.4. Konfigurasi Pin Mikrokontroller AT89S8252

Konfigurasi kaki-kaki mikrokontroller terdiri dari 40 pin, seperti terlihat pada gambar 2.2 berikut ini :



Gambar 2.6 Konfigurasi Pin-Pin AT89S8252[8]

Fungsi dari tiap-tiap pin adalah sebagai berikut:

- **Pin 40: Vcc** (sumber tegangan).
- **Pin 20: GND** *(Ground)*
- **Pin 32-39:**

  Port 0: Merupakan port *input-output* dua arah multipleks dan dua *bus* alamat

rendah (A0-A7) serta data selama pengaksesan program dan data memori *external.*

- **Pin 1-8: Port 1:**

  Merupakan port *input-output* dua arah dengan *internal pull-up.*

- **Pin 21-28: Port 2:**

  Merupakan port *input-output* dengan *internal pull-up.* Mengeluarkan *address* tinggi selama pengambilan *(fetching) program memory external.* Seama pengaksesan ke *external data memory,* port 2 mengeluarkan isi P2 SFR *(Special Function Register).* Menerima *address* dan beberapa sinyal control selama pemrograman dan verifikasi.

- **Pin 10-17: Port 3:**

  Merupakan port *input-output* dengan *internal pull-up.* Port 3 juga memiliki fungsi khusus, yaitu:

  1. RXD (P3.0) : Port *serial input.*
  2. TXD (P3.1) : Port *serial output.*
  3. INTO (P3.2) : *external interrupt 0.*
  4. INT1 (P3.3) : *external interrupt 1.*
  5. TO (P3.4) : *Input external timer 0.*
  6. T1 (P3.5) : *Input external timer 1.*
  7. WR (P3.6) : *Strobe* tulis data memori *external.*
  8. RD (P3.7) : *Strobe* baca data memori *external.*

- **Pin 9: RST *(Reset):***

  Input reset berfungsi *me-reset* CPU saat tegangan dihidupkan.

- **Pin 30: ALE/PROG *(Address Latch Enable)/Programming:***

  Pulsa *output* ALE digunakan untuk proses *latching byte address* rendah (A0-A7) selama pengaksesan ke memori *external*. Pin ini juga digunakan untuk memasukkan pulsa program selama pemrograman.

- **Pin 29: PSEN *(Program Store Enable):***

  Merupakan *strobe* baca ke program memori *external*.

- **Pin 31: *EA/VPP (External Address):***

  EA *low* jika mengakses memori *external*. Untuk mengakses memori *internal* maka EA dihubungkan ke-Vcc (+5V).

- **Pin 18-19: *XTAL1* dan *XTAL2:***

  Kaki ini dihubungkan dengan kristal bila menggunakan *Oscillator internal*. XTAL1 merupakan *input inverting Oscillator amplifier* sedangkan XTAL2 merupakan *output inverting oscillator amplifier*.

2.9.5. Organisasi Memori

Dalam mikrokontroller AT89S8252 ruang alamat telah dibedakan untuk program memori dan data memori.

2.9.5.1. *Internal Program Memory*

Mikrokontroller AT89S8252 memiliki program memori *internal* sebesar 8 Kbyte dengan ruang alamat 0000H-0FA0H. Jika alamat-alamat program lebih tinggi dari pada 0FA0H dimana melebihi kapasitas ROM *internal*, menyebabkan AT89S8252 secara otomatis mengambil kode byte dari program memori *external*. Kode *byte* juga dapat diambil hanya dari memori *external* dengan alamat 0000HFFFFH dengan cara menghubungkan pin EA ke *ground*.

2.9.5.2. *Random Acsses Memory* (RAM)

Ruangan alamat memory data *internal* (RAM) dengan kapasitas 256 *byte* yaitu: 00H-FFH yang terbagi atas 3 daerah, yaitu:

1. Empat *bank register*

   Setiap *bank* terdiri dari *8 register* (R0-R7) sehingga jumlah *register* untuk keempat *bank register* menjadi 32 buah *register* yang menempati ruang alamat 00H-1FH. Mengaktifkan salah satu *bank register* dapat dilakukan dengan mengatur RS O-RS 1 pada *Program Status Word (PSW).*

2. Bit *Addressable*

   Terdiri dari *16 byte* yang berada pada alamat 20H-2FH. Masing-masing bit dalam 208 bit yang lokasinya dapat dialamati secara langsung.

3. RAM Keperluan Umum

   Terdiri atas 208 *byte* yang menempati alamat 30H-FFH, dan dapat dialamati secara langsung maupun tak langsung dalam penggunaan untuk keperluan umum *(general purpose).*

Table 2.4
Pengaturan RS0-RS1 *Bank Register*

RS1	RS0	Register Bank Select Bits
0	0	Bank 0
0	1	Bank 1
1	0	Bank 2
1	1	Bank 3

2.9.5.3. Sistem Interupsi

Mikrokontroller AT89S8252 mempunyai 9 buah sumber interupsi yang dapat mengakibatkan permintaan interupsi, yaitu: INTO, INT1, TO, TI port serial dan beberapa

port lainnya. Saat terjadi interupsi mikrokontroller secara otomatis akan menuju ke *subrutin* pada alamat tersebut. Setelah interupsi *service selesai* dikerjakan, Mikrokontroller akan mengerjakan program semula. Sumber interupsi *external* adalah INTO, INTl, dimana kedua interupsi *external* ini akan aktif pada transisi rendah selain itu juga ada *Timer/Counter 0, Timer/Counter 0 dan* interupsi dari port serial *(receiver).* Interupsi serial dibangkitkan dengan melakukan operasi OR pada RI dan TI. Tiap-tiap sumber interupsi dapat *di-enable* atau *di-disable* secara *software.* Tingkat prioritas semua sumber interupsi dapat diprogram sendiri-sendiri dengan *set* atau *clear* bit pada SFRS IP *(Interrupt Priority).*

Tabel 2.5
Alamat Sumber Interupsi

Sumber Interupsi	Alamat Awal
Power On Reset	0000h
Interrupt luar 0 (INT 0)	0003h
Pewaktu/ pencacah 0 (TO)	000Bh
Interrupt luar 1 (INT 1)	0013h
Pewaktu/ pencacah 1 (T I)	001 Bh
Port 110 *Serial*	0023h

Register yang berperan dalam mengatur aktif tidaknya interupsi adalah *interrupt enable register.* susunan dari bit-bit beserta kegunaannya adalah:

Tabel 2.6
Kegunaan *Interrupt Enable Register*

Data	Simbol	Posisi	Fungsi /Arti
DO	EXO	1E.0	Diatur secara *software* untuk interupsi dari INTL.
DI	ETO	1E. 1	Diatur secara *software* untuk interupsi dari *timer/counter* 1.
D2	EX I	IE.2	Diatur secara *software* untuk interupsi dari INT 1.
D3	ETI	IE.3	Diatur secara *software* untuk interupsi dari *timer/counter 1.*

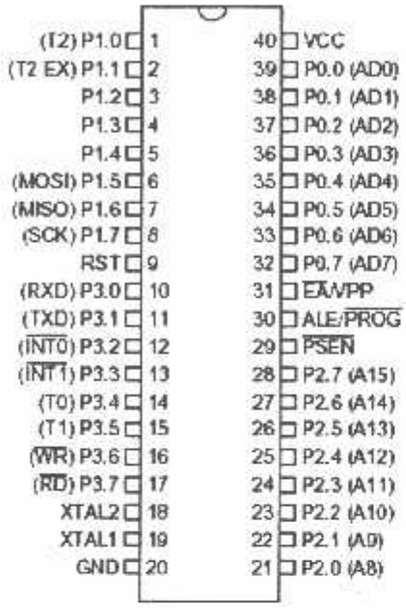
D4	ES	IE.4	Untuk mengatur *enable* atau *disables* satu interupsi RI/TI.
D5	-	IE.5	Kosong
D6	-	IE.6	Kosong
D7	EA	IE.7	Jika diatur 0 maka semua interupsi *di-disable*. jika diatur 1 maka interupsi diatur *di-disable* atau *di-enable* menurut masing-masing bit.

2.10. Mikrokontroller AT89S52

Mikrokontroller AT89S52 merupakan salah satu anggota keluarga dari MCS-51, yaitu suatu komponen produksi ATMEL, yang berorientasi *control* (microcontroller). Intel mengklarifikasikan dalam kelompok *embedded microcontroller*, yang artinya adalah mikrokontroller yang dapat diprogram ulang (*reprogrammable*).Didalam chip mikrokontroller AT89S52 ini sudah tersedia berbagai macam peralatan pendukung mikroprosesor seperti RAM, serial port, bus-bus datadan lainnya yang membuat pemakai chip ini dapat menekan penambahan komponen pendukung. Spesifikasi perangkat keras dari mikrokontroller AT89S52 adalah sebagai berikut:

- CPU (*Central Processing Unit*) dengan lebar data 8 bit
- Prosesor Boolean untuk operasi logika 1 bit
- Pembangkit clock *internal*
- Tiga buah *timer/counter* 16 bit
- Dua buah saluran *interupsi eksternal*
- Jalur I/O dua arah 32 buah
- Memori program terpisah dari memori data
- Memori data *internal* 256 byte
- Alamat memori program *eksternal* 64 Kilobyte
- Alamat memori data *eksternal* 64 Kilobyte

- Memori program *internal* sebesar 8 Kilobyte



Gambar 2.7 Konfigurasi Pin-Pin AT89S52[9]

Berikut ini adalah penjelasan dari masing-masing pin mikrokontroller AT89S52:

- **Pin 1 sampai 8**

  Port 1: Merupakan 8 bit saluran masukan/keluaran dua arah. Setiap saluran mampu melayani 4 masukan.

- **Pin 9**

  RST: Merupakan masukan reset. Logika *high* yang akan membuat mikrokontroller AT89S52 menjalankan rutin *reset*.

- **Pin 10-17**

  Port 3: Port 3 terdiri dari 8 saluran masukan/keluaran dua arah. Setiap saluran mampu melayani 4 masukan.Selain itu masukan/keluaran port 3 juga mempunyai fungsi-fungsi khusus yang dimiliki oleh keluaran MCS-51. Fungsi tersebut dapat

dilihat dalam table2.14

- **Pin 18-19**

  X1 (XTAL) & X2 (XTAL2):Jika dikonfigurasikan bersama sebuah kristal akan membentuk rangkaian osilator on-chip pada mikrokontroller.

- **Pin 20-27**

  Port 2 : Port 2 terdiri dari 8saluran masukan/keluaran dua arah,setiap salurannya mampu melayani 4 masukan. Port 2 mengeluarkan alamat bagian tinggi (A8-A15),selama pengambilan intruksi dari memori program *eksternal* dan pengambilan data dari memory data *eksternal* yang menggunakan mode pengalamatan 16 bit (dengan perintah MOV @DPTR).

- **Pin 29**

  $\overline{PSEN}$: *Program Store Enable* merupakan sinyal baca yang mengesekusi memori program *eksternal*.

- **Pin 30**

  ALE/ $\overline{PROG}$:*Address Latch Enable* merupakan pulsa yang berfungsi menahan alamat rendah (A0-A7) pada port 0, selama dilakukan proses baca atau tulis memori *eksternal*. Pin ini juga berfungsi sebagai masukan pulsa program ($\overline{PROG}$),selama dilakukan pemrogaman pada EEPROM *eksternal*.

- **Pin 31**

  $\overline{EA}$ /VPP: *Eksternal Access*. $\overline{EA}$ dihubungkan dengan VSS untuk memungkinkan pengambilan instruksi pada pengambilan intruksi pada memori program *eksternal* yang berlokasi 0000h-FFFFh. Jika diinginkan menggunakan memori program *internal* maka $\overline{EA}$ dihubungkan VCC.

- **Pin 32 -39**

  Port 0: Port 0 terdiri dari 8 saluran masukan / keluaran dua arah,setiap saluran mampu melayani 8 masukan. Port 0 merupakan saluran alamat bagian rendah (A0-A7), yang di*multiplekser* saluran bus data (D0-D7), yang digunakan pada saat mengakses memori data *eksternal* dan memori program *eksternal*.

- **Pin 40**

  VCC: Merupakan masukan catu daya 5V, dengan toleransi kurang lebih 10%.

2.10.1. Organisasi Memori

Organisasi memori pada mikrokontroller AT89S52 dapat dibagi menjadi dua bagian besar yaitu memori program dan memori data. Pembagian tersebut didasarkan atas fungsi dari penyimpanan data maupun program. Memori program digunakan untuk menyimpan instruksi-instruksi yang akan dijalankan oleh mikrokontroller,sedangkan memori data digunakan sebagai tempat penyimpanan data yang sedang diolah mikrokontroller.

Program mikrokontroller disimpan dalam memori program berupa ROM. Mikrokontroller AT89S52 dilengkapi dengan ROM internal namun untuk program yang besar digunakan ROM *eksternal* yang terpisah dari mikrokontroller. Untuk dapat menggunakan memori program *eksternal* ini penyemat / $\overline{EA}$ dihubungkan dengan penyemat V_{SS}(logika 0).

Memori program mikrokontroller alamat 16 bit mulai 0000_H-$FFFF_H$, sehingga kapasitas penyimpanan program maksimal 2^{16} *byte* atau 64 Kb. Sinyal yang digunakan unutuk membaca program *eksternal* adalah sinyal $\overline{PSEN}$ (*Program Store Enable*).

Selain memori program mikrokontroller AT89S52 juga memiliki memori data internal berkapasitas 256 byte dan mampu mengakses memori data *eksternal* sebesar 64 Kb. Semua memori data *internal* dapat dialamati dengan pengalamatan langsung atau tidak langsung. Ciri dari pengalamatan langsung adalah operand berisi data yang diolah. Sedangkan ciri dari pengalamatan tidak langsung adalah operand alamat register yang berisi alamat data yang akan diolah. Untuk membaca data digunakan sinyal / $\overline{RD}$, sedangkan untuk menulis data digunakan sinyal / $\overline{WR}$.

2.10.2. Register Fungsi Khusus

Register fungsi khusus (*Special Function Register*) terletak pada 128 *byte* bagian atas memori data internal dan berisi register-register untuk pelayanan *latch port*, *timer,program status words,control peripheral* dan sebagainya. Alamat *register* fungsi khusus ditunjukkan pada table 2-6.

Register-register ini hanya dapat diakses dengan pengalamatan langsung. Enam belas alamat pada register fungsi khusus dapat dialamati perbit maupun per*byte* dan terletak pada alamat 80_H-FF_H. Secara perangkat keras, register fungsi khusus ini dibedakan dengan memori data internal.

Tabel 2-7. Nama dan Alamat Register pada Register fungsi Khusus[10]

Simbol	Nama Register	Nilai pada saat reset	Alamat
ACC	*Accumulator*	00_H	$0E0_H$
B	*Register B*	00H	0F0H
PSW	*Program Status Word*	00H	0D0H
SP	*Stack Pointer*	07H	81H
DPTR	*Data Pointer 2bytes*		
DPL	*Low Bytes*	0000H	82H
DPH	High bytes	0000H	83H
P0	Port 0	FFH	80H
P1	Port 1	FFH	90H
P2	Port 2	FFH	0A0H
P3	Port 3	FFH	0B0H
IP	*Interrupt priority control*	XXX00000B	0B8H
IE	*Intrrupt enable control*	0XX00000B	0A8H
TMOD	*Timer/counter mode control*	00H	89H
TCON	*Timer/counter control*	00H	88H
TH0	*Timer/counter 0 high bytes*	00H	8CH
TL0	*Timer/counter 0 low bytes*	00H	8AH
TH1	*Timer/counter 1high bytes*	00H	8DH
TL1	*Timer/counter 1low bytes*	00H	8BH
SCON	*Serial control*	00H	98H
SBUF	*Serial Data Buffer*	Independen	99H

Beberapa macam register fungsi khusus yang sering digunakan, dijelaskan sebagai berikut (Modul Pelatihan MCS-51,14-15):

- *Accumulator* (ACC) merupakan *register* untuk penambahan dan pengurangan. Perintah *Mnemonic* untuk mengakses akumulator disederhanakan sebagai A.
- *Register* B merupakan *register* khusus yang berfungsi melayani operasi perkalian dan pembagian.
- *Program Status Word* (PSW) terdiri dari beberapa bit status yang menggambarkan kejadian diakumulator sebelumnya. Yaitu *carry bit*, *auxiliary*

carry, dua bit pemilih bank, bendera *overflow*, *parity bit*,dan dua bendera yang dapat didefenisikan sendiri oleh pemakai.

- *Stack Pointer* (SP)merupakan *register* 8 bit yang hanya dapat diletakkan di alamat manapun pada RAM internal. Isi *register* ini ditambah sebelum data disimpan, selama instruksi PUSH dan CALL. Pada saat *reset*,*register* SP diinisialisasi pada alamat 07H, sehingga *stack* akan dimulai pada lokasi 08H.
- *Data Pointer* (DPTR) terdiri dari dua register, yaitu untuk *byte* tinggi (*Data pointer high*,DPH) dan *byte* rendah (*Data pointer low*,DPL)yang berfungsi untuk pengalamatan alamat 16 bit.
- *Port* 0 sampai *port* 3 merupakan *register* yang berfungsi untuk membaca dan mengeluarkan data pada *port* 0,1,2,3. Masing-masing *register* ini dapat dialamati per-*byte* maupun per-*bit*.
- *Serial Data Buffer* (SBUF) merupakan dua *register* yang terpisah, *register buffer* pengirim dan sebuah *register buffer* penerima. Meletakkan data pada SBUF berarti meletakkan pada *buffer* pengirim yang akan mengirimkan data melalui transmisi serial. Membaca data SBUF berarti menerima data dari *buffer* penerima.
- *Control register* terdiri dari *register* yang mempunyai fungsi *control*. Untuk mengontrol system interupsi, terdapat dua register khusus, yaitu register IP (*Interrupt priority*) dan register IE (*Interrupt enable*). Untuk mengontrol pelayanan *timer/counter* terdapat *register* khusus, yaitu *register* TCON(*timer/counter control*) serta untuk pelayanan port serial menggunakan register SCON(*serialport control*).

2.10.3. Port Masukan dan Keluaran

Mikrokontroller AT89S52 mempunyai 4 port dan masing-masing port terdiri dari 8 saluran bit. Ke empat ini bersifat bidirectional yaitu dapat digunakan sebagai masukan atau keluaran.

Port 0 digunakan sebagai saluran data yang dimultipleks dengan saluran alamat rendah untuk mengakses memori *eksternal*,baikmemori program maupun memori data. Port 2 mengeluarkan bagian alamat tinggi untuk mode pengalamatan memori16 bit. Port 1dan port 3 berfungsi sebagai saluran masukan dan keluaran multi fungsi. Jika dibutuhkan port 3 mempunyai fungsi khusus seperti ditunjukkan pada tablc 2-14.

Tabel 2.8. Fungsi Khusus port 3

Nama Port	Fungsi Khusus
Port 3.0	RxD (port masukan serial)
Port 3.1	TxD (port keluaran serial)
Port 3.2	/INT0 (masukan interupsi *eksternal* 0)
Port 3.3	/INT1 (masukan interupsi)
Port 3.4	TO (masukan pewaktu *eksternal* 0)
Port 3.5	T1 (masukan pewaktu *eksternal* 1)
Port 3.6	/WR (sinyal tulis memori data *eksternal*)
Port 3.7	/RD (sinyal baca memori data *eksternal*)

BAB III

PERANCANGAN DAN PEMBUATAN ALAT

3.1. Pendahuluan

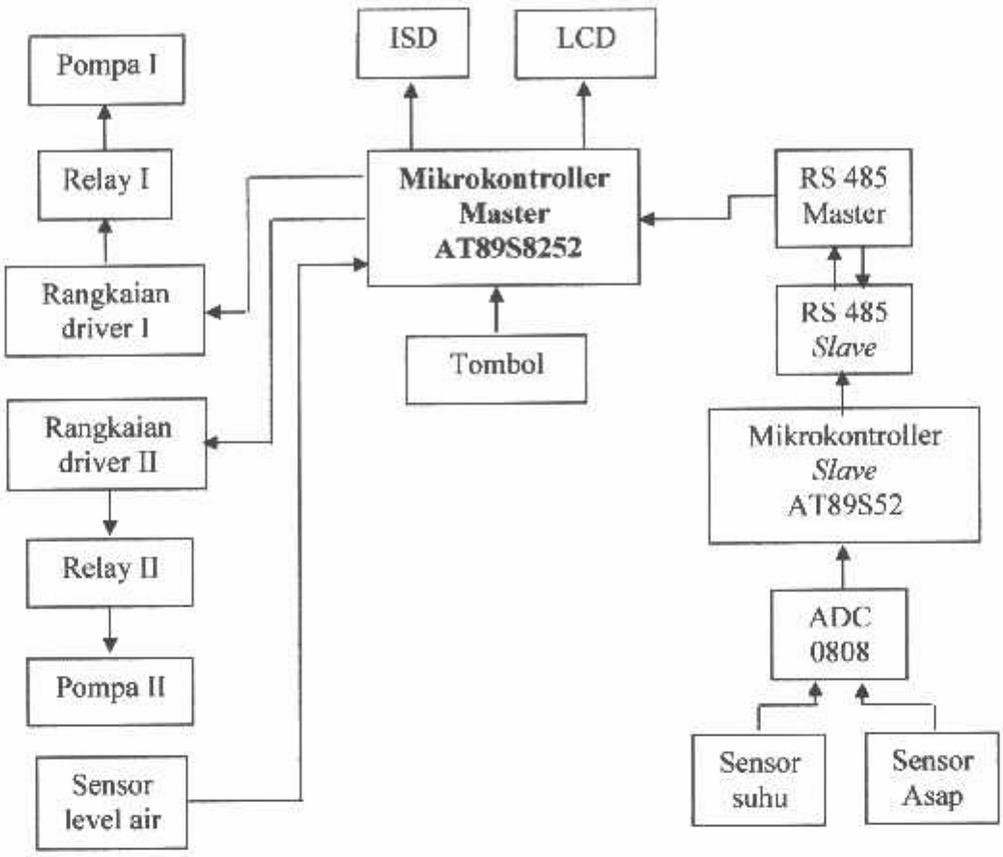
Dalam bab ini akan dibahas perancangan dan pembuatan alat. Pembahasan akan dilakukan pada setiap blok rangkaian, cara kerja masing-masing blok rangkaian, perhitungan dan fungsi masing-masing blok rangkaian tersebut. Secara garis besar terdapat dua bagian perangkat yang ada yaitu :

- Perancangan perangkat keras *(Hardware)*.
- Perancangan perangkat lunak *(Software)*.

Pada perancangan perangkat keras akan meliputi seluruh *peripheral* yang digunakan pada sistem ini. Pada perancangan perangkat lunak akan meliputi diagram alir dan software secara umum. Akan tetapi kedua perangkat ini dalam kerjanya akan saling menunjang satu sama lain.

3.1.1. Blok Diagram Keseluruhan Sistem

Mikrokontroler dalam diagram blok terdapat 2 bagian yaitu mikrokontroler *Master* AT89S8252,dan mikrokontroler *Slave 1* AT89S52, yang bekerja saling berhubungan satu dengan yang lainnya, mikrokontroler *Master* disini bertugas sebagai pengendali utama dari keseluruhan sistem. Gambar dibawah ini menunjukkan blok diagram dari keseluruhan sistem.



Gambar 3.1. Diagram Blok Keseluruhan Sistem

Secara umum sistem kerja dari keseluruhan sistem ini adalah kita setting suhu dan asap sesuai dengan ketentuan, untuk suhu normal ruangan 28° jadi suhu disetting diatas suhu normal ruangan (misalnya 40°) dengan menggunakan tombol lalu tekan Enter. Untuk setting kadar asap disesuaikan dengan intensitas yang dikategorikan kebakaran menggunakan satuan ppm (*part per million*). Bila besar temperature dalam ruangan tersebut mencapai 40°C dan intensitas asap mencapai intensitas yang telah ditentukan, maka mikrokontroller *Slave* akan memberikan sinyal berupa tegangan yang ditunjukkan pada rangkaian RS 485 yang berfungsi sebagai pengirim dan penerima data secara serial, kemudian diterima oleh mikrokontroller *Master* yang akan mengaktifkan rangkaian

driver relay II sehingga akan mengaktifkan pompa II dan air akan menyemprot melalui pipa dan alarm akan berbunyi berupa informasi yang disampaikan melalui suara terpogram,tampilan pada LCD berupa besar suhu dan asap yang diinginkan. Berikut penjelasan secara umum masing-masing blok:

- **Sensor Gas CO (Karbon Monoksida) AF 30.**

  Mendeteksi kadar asap pada gas CO (Karbon Monoksida) dan mengubahnya dalam bentuk fluktuasi tegangan. Kadar asap pada gas CO disini diukur dalam *part per million* (ppm). Semakin besar kadar gas CO-nya tegangan pada sensor semakin besar pula, demikian juga sebaliknya. Fluktuasi tegangan inilah dapat diolah dan diproses oleh mikrokontroler yang diubah dalam bentuk besaran digital terlebih dahulu.

- **Sensor Suhu LM 35.**

  Sensor suhu yang dipakai adalah IC LM35 yang nilai hambatannya berubah terhadap perubahan suhu.Tegangan output pada IC LM35 adalah sebanding dengan derajad(^{0}) temperature serta menghasilkan kenaikan tegangan sekitar 10 mV pada setiap kenaikan suhu 1^{0}C.

- **ADC 0808.**

  Mengubah besaran analog ke besaran digital 8 bit data, disini menggunakan ADC 0808, 8 input analog dan 1 output data digital. Besaran analog yang dimasukkan pada ADC, adalah besaran analog dari sensor CO yaitu AF 30 dan sensor suhu LM35.

- **Mikrokontroller *Slave* AT89S52 (Sensor Asap dan Suhu)**

  Mikrokontroller ini menerima masukan dari ADC 0808 yang membawa data dari sensor CO AF30 dan sensor suhu LM35 yang kemudian mengirimkan data ke mikrokontroller Master melalui RS 485.

- **RS 485**

  RS485 merupakan kabel komunikasi serial yang bisa mencapai jarak 4000 yard dengan kecepatan lebih dari 1 Megabit/detik, dan pada jarak yang lebih pendek kecepatan transmisi RS 485 sekitar 10 Megabit/detik. RS485 juga berfungsi sebagai pengirim dan penerima data.

- **Mikrokontroller *Master* AT89S8252**

  Mikrokontroller ini merupakan mikrokontroller pengendali utama yaitu menerima masukan dari tombol setting yang berfungsi untuk mengeset besarnya suhu dan kadar asap dalam bentuk ppm yang diinginkan yang akan ditampilkan pada LCD. Apabila terjadi kebakaran dimana besarnya suhu dan asap sesuai dengan yang disetting maka mikrokontroller *Slave* 1 akan mengirimkan data ke mikrokontroller *Master* untuk diproses dan diolah yang akan mengaktifkan rangkaian driver relay II sehingga akan mengaktifkan pompa II dan air akan menyemprot melalui pipa dan alarm akan berbunyi.

- **ISD 1420**

  Sebagai memori suara terprogram yang dapat menyimpan suara dalam bentuk data-data digital dan dapat dipanggil dan mengubahnya kembali menjadi data suara audio. *Peripheral* ISD 1420 ini mempunyai waktu bicara sepanjang 20 detik. Fungsi dari bagian ini adalah sebagai alarm apabila terjadi kebakaran.

- **LCD M1632.**

  Menampilkan data-data dari masukan untuk dibaca oleh *user*/pengguna, dalam sistem ini menampilkan besarnya settingan suhu dan asap.

- **Tombol**

  Tombol ini terdapat enam pilihan utama diantaranya adalah: Menu, Select,Cancel Enter, Cek Baca Sensor dan Cek Pompa Penyemprot. Tombol disini berfungsi untuk mengeset besarnya suhu dan asap yang diinginkan kemudian membaca suhu dan asap pada ruangan tersebut dan mengecek apakah pompa penyemprot bisa menyemprot atau tidak.

- **Rangkaian driver**

  Driver-driver ini merupakan driver *relay* yang menerima data-data digital dari mikrokontroler untuk mengaktifkan relay I yang berfungsi sebagai penghubung ke pompa I yang bertugas mengisi tandon jika air habis dan sebagai pemutus ke pompa I jika air dalam tandon penuh dan mengaktifkan relay II berfungsi sebagai penghubung ke pompa II jika terjadi kebakaran dan sebagai pemutus ke pompa II bila api padam.

- **Relay I**

  Berfungsi sebagai penghubung ke pompa I yang bertugas mengisi tandon jika air habis dan sebagai pemutus ke pompa I jika air dalam tandon penuh.

- **Pompa I**

  Berfungsi untuk mengisi tandon jika air habis.

- **Relay II**

  Berfungsi sebagai penghubung ke pompa II jika terjadi kebakaran dan sebagai pemutus ke pompa II bila api padam.

- **Pompa II**

  Berfungsi untuk memadamkan kebakaran.

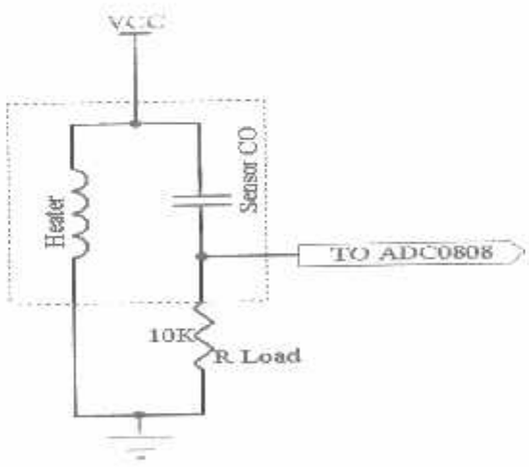
3.2. Perancangan Perangkat Keras

Perancangan perangkat keras terdiri dari beberapa bagian secara umum dapat dibagi menjadi 3 bagian utama yaitu :

- Bagian masukan yang terdiri dari sensor-sensor,keypad.
- Bagian pemroses data yaitu mikrokontroler.
- Bagian keluaran yang terdiri dari driver-driver, LCD dan ISD.

3.2.1. Perancangan Sensor Asap AF30

Pada perancangan ini sensor digunakan untuk mendeteksi adanya kadar gas karbon monoksida (CO) disuatu ruangan. Sensor yang digunakan adalah type AF-30 yang dapat bekerja pada temperatur -10-55 °C. Dari sensor ini bisa diketahui besarnya kadar CO sesuai dengan ouput yang dihasilkan berupa tegangan. Sensor gas ini dirancang untuk beroperasi dengan tegangan 5V. Ketika sensor mendeteksi gas, tahanan sensor akan menurun.Berikut adalah gambar rangkaian sensor gas AF30.



Gambar 3.2. Rangkaian Sensor Gas *CO AF-30*

Besarnya tahanan sensor (Rs) dapat diketahui dengan persamaan sebagai berikut:

$$Rs = \frac{Vc - Vout}{Vout}.RL$$

Maka dari situ kita dapat mencari besarnya daya yang dibutuhkan sensor (Ps) dengan rumus: $Ps = \frac{Vc^2 - Rs}{(Rs + Rl)^2}$

Dimana:

Rs = Tahanan sensor

R_L = Tahanan beban (Variabel)

Vc = Tegangan kerja pada rangkaian

Vout = Tegangan keluaran (Vo)

Ps – Daya yang di butuhkan oleh sensor (Ps≤ 15 mw)

Sebagai contoh:

1. Diketahui hasil pengukuran diperoleh kadar CO adalah 1120 ppm, R_L= 10KΩ,Vout =2,10 V tahanan sensornya (Rs) adalah:

$$Rs = \frac{Vc - Vout}{Vout}.RL$$

$$Rs = \frac{5 - 2{,}10}{2{,}10}10K = 13{,}81K\Omega$$

2. Diketahui hasil pengukuran diperoleh kadar CO adalah 990 ppm, R_L=10KΩ , Vout – 1,94 V, tahanan sensornya (Rs) adalah:

$$Rs = \frac{Vc - Vout}{Vout}.$$

$$Rs = \frac{5 - 1{,}94}{1{,}94}.10K = 15{,}77K\Omega$$

3.2.2. Perancangan Sensor Suhu LM35

Pada dasarnya sensor suhu pada alat ini adalah untuk mengetahui suhu yang ada didalam ruangan. Pada perancangan dan pembuatan alat ini menggunakan sensor LM35 yang memiliki kelebihan pada outputnya yang linier yaitu tegangan output sebesar 10mV setiap kenaikan 1^0C sehingga memudahkan dalam pengolahan datanya, untuk menghitung tegangan output dari sensor ini pada saat membaca temperature adalah:

Vout – Temp x 10mV/^{0}C

Dimana :

Vout = Tegangan output dari sensor LM35 (V)

Temp = Besarnya suhu yang dibaca sensor (^{0}C)

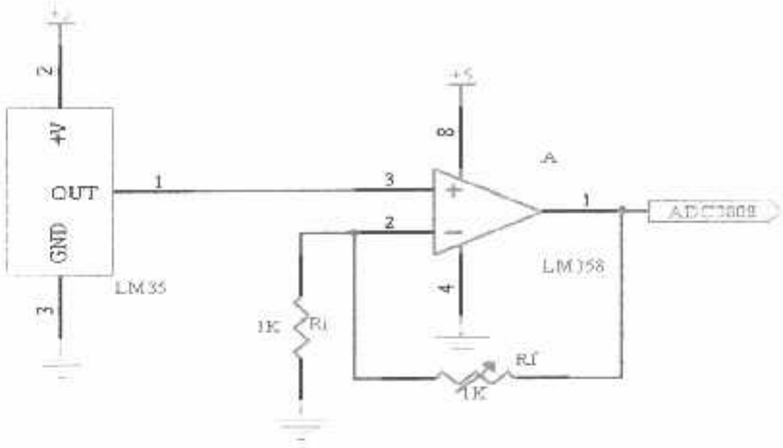
Sebagai contoh:

Jika suhu yang diukur 40^0C maka tegangan output sensor LM35 adalah:

Vout = 40^0C x 10mV/^{0}C

Vout = 400mV

Untuk menaikkan resolusi pembacaan data suhu maka output dari sensor diumpankan ke suatu rangkaian penguat non inverting dengan menggunakan IC *Op-Amp* LM358. Untuk lebih jelasnya dapat dilihat pada rangkaian dibawah ini:



Gambar 3.3.Rangkaian Sensor Suhu dan Pengkondisi Sinyal

Persamaan yang digunakan adalah:

$$A = \left(1 + \frac{Rf}{Ri}\right)$$

Dari rumus tersebut dapat kita hitung besarnya penguatan dari ouput sensor LM35.

Diatas diketahui : Ri = 1K, Rf= 1K maka penguatannya:

$$A = \left(1 + \frac{Rf}{Ri}\right)$$

$$A = \left(1 + \frac{1K}{1K}\right) = 2kali$$

Jadi dari perhitungan diatas diketahui penguatannya adalah 2 kali. Dipilih penguatan sebesar 2 kali karena menyamakan resolusi dari ADC 0808.

3.2.3. Perancangan *Analog Digital Counter* (ADC) 0808

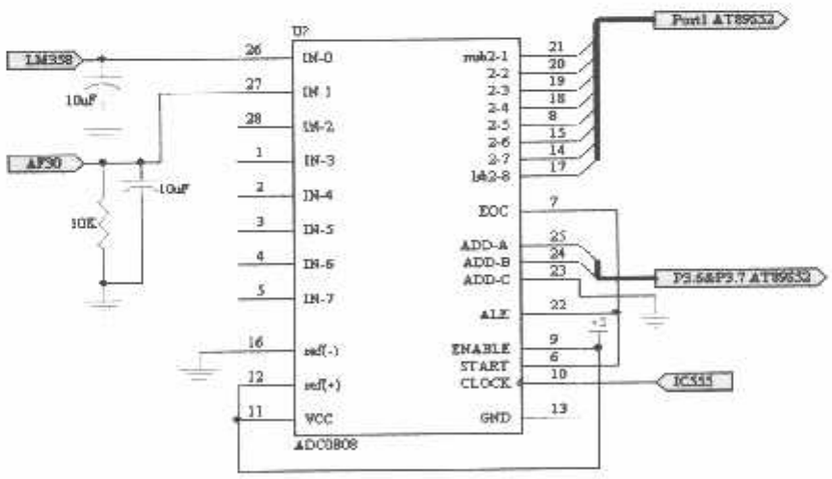
Dalam pembuatan alat ini juga dibutuhkan pengubah sinyal analog menjadi digital atau disebut *Analog to Digital Converter* (ADC) hal ini disebabkan karena sinyal-sinyal yang didapat dari sensor suhu dan sensor CO adalah berupa sinyal analog sedangkan rangkaian kontrolnya menggunakan system digital sehingga membutuhkan input berupa

sinyal digital. Jenis ADC yang digunakan adalah ADC 0808 yang memiliki kelebihan yaitu dapat menerima hingga 8 inputan. Pada alat ini hanya menggunakan 2 inputan saja yaitu IN-0 (pin 26) sebagai inputan dari pengkondisi sinyal sensor suhu, sedangkan IN-1(pin 27) sebagai inputan dari sensor asap. Untuk lebih jelasnya dapat kita lihat pada table dibawah ini:

Tabel 3.1. *Address Decoder* ADC 0808

Selected Analog Channel	*Address Line*		
	C	B	A
IN0	L	L	L
IN1	L	L	H
IN2	L	H	L
IN3	L	H	H
IN4	H	L	L
IN5	H	L	H
IN6	H	H	L
IN7	H	H	H

Berikut adalah gambar dari rangkaian ADC 0808:

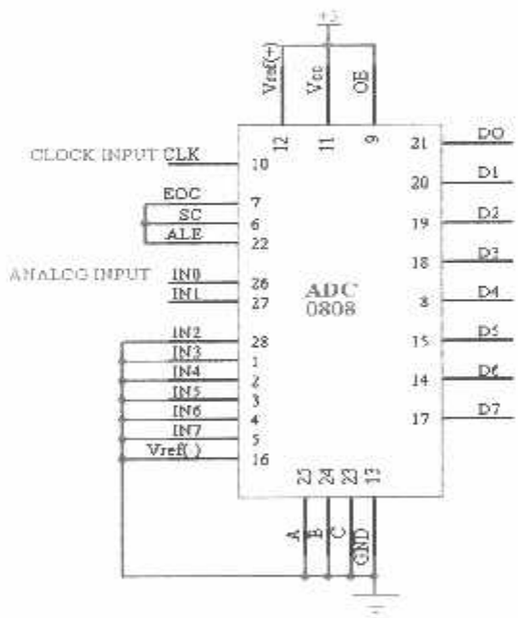


Gambar 3.4. Rangkaian ADC 0808

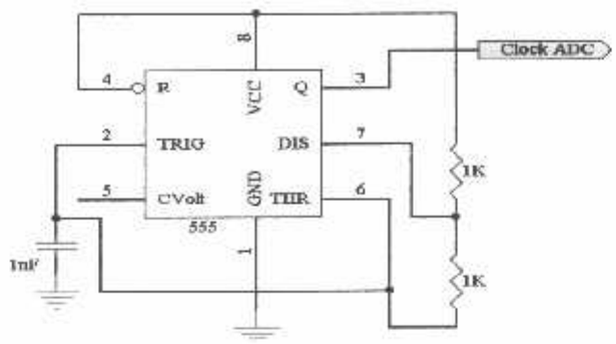
Penjelasan dari gambar diatas:

1. IN-0 (pin 26) merupakan inputan yang berupa analog dari pengkondisi sinyal sensor suhu LM35, IN1 (pin 27) merupakan inputan yang berupa sinyal analog dari sensor CO (AF30).
2. D0-D7 digunakan untuk mengirim data digital ke mikrokontroller.
3. ADD A dan ADD B digunakan untuk mengirim sinyal dari mikrokontroller untuk memilih data antara sensor suhu/sensor CO.

Dalam perancangan alat ini menggunakan ADC mode *free running* artinya ia akan konversi terus-menerus sinyal input yang masuk dengan cara menghubungkan pin EOC (*End of Conversion*) ke SC (*Start Conversion*).



Pada ADC 0808 tidak memiliki clock internal sehingga untuk mengaktifkannya diperlukan clock eksternal. Dalam hal ini menggunakan IC 555 berikut ini adalah gambar dari rangkaian clock eksternal ADC 0808.



Gambar 3.5. Rangkaian Clock Eksternal ADC 0808

Dari gambar rangkaian diatas dapat kita hitung besarnya frekuensi yang dihasilkan adalah sebagai berikut:

$$f = \frac{1,44}{(R1 + 2R2)C}$$

$$f = \frac{1,44}{(1.10^{3} + 2.1.10^{3})1.10^{-9}}$$

$$f = \frac{1,44}{2.10^{6}.1.10^{-9}}$$

$$f = 480 \text{ KHz}$$

Berdasarkan perhitungan diatas dapat diketahui frekuensi yang dihasilkan oleh rangkaian clock eksternal adalah 480 KHz. 480 KHz dipilih karena frekuensi sebesar itu sudah cukup memenuhi dengan proses frekuensi yang dibutuhkan oleh ADC. Jadi jika dilihat data sheet pada ADC0808 frekuensi clock yang dibutuhkan oleh ADC 0808 adalah antara 10-1280 KHz, sehingga frekuensi yang dihasilkan oleh rangkaian clock eksternal ini sudah memenuhi syarat.

Pada ADC 0808 Vref diset pada kondisi *Full Range* yaitu Vref (-) diset pada 0 Volt,sedangkan untuk Vref (+) diset pada 5 volt.pada saat 0Volt yaitu pada 0 sedangkan pada 5 Volt pada 255, karena kondisi tersebut maka Vref-nya dapat diketahui yaitu sebesar 5 Volt.Dari data Vref tersebut dapat dicari output dari ADC dengan persamaan sebagai berikut:

Vref = 5Volt

$$\text{Resolusi perbit} = \frac{Vref}{2^8} = \frac{5}{255} = 19{,}6mV$$

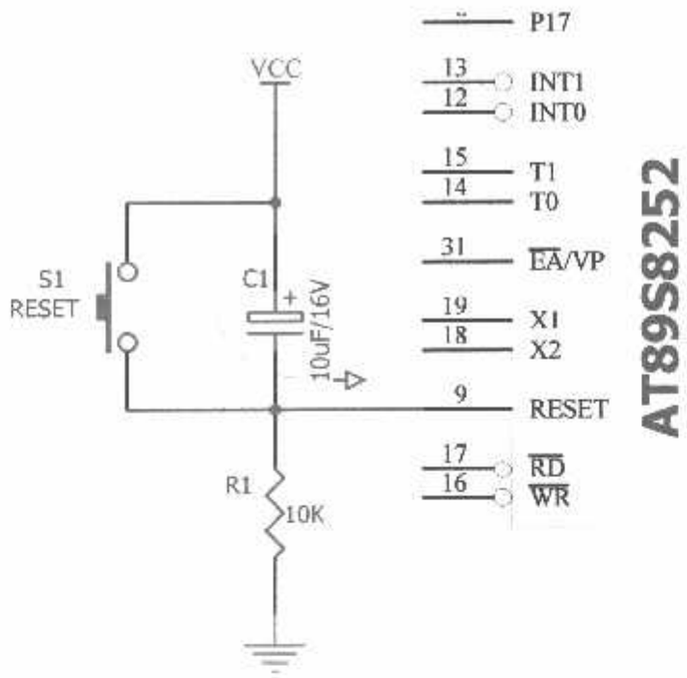
Contoh:

Vanalog = 0,5V

$$\text{Data ADC} = \frac{Vana\log}{resolusi} = \frac{0{,}5}{19{,}6mV} = 25_{(10)}$$

3.2.4. Perancangan Rangkaian Reset

Untuk m*ereset* mikrokontroler AT89S8252, maka pin RST diberi logika tinggi selama sekurangnya dua siklus mesin (24 periode osilator). Untuk membangkitkan sinyal *reset* kapasitor dihubungkan dengan Vcc dan sebuah resistor yang dihubungkan ke *ground*. Rangkaian *reset* ditunjukkan dalam gambar 3-5 sebagai berikut :



Gambar 3.6. Perancangan Rangkaian Reset

Karena kristal yang digunakan mempunyai frekuensi sebesar 11,0592 MHz, maka satu periode membutuhkan waktu sebesar :

$$T = \frac{1}{f_{XTAL}} = \frac{1}{11{,}0592\,MHz}\,S = 9{,}042\times10^{-8}\,s$$

Sehingga waktu minimal logika tinggi yang dibutuhkan untuk *mereset* mikrokontroler adalah :

reset(min) = T × periode yang dibutuhkan

= 9,042 × 10^{-8} × 24 = 2,17 µs

Jadi mikrokontroler membutuhkan waktu minimal 2,17 µs untuk *mereset*. Waktu minimal inilah yang dijadikan pedoman untuk menentukan nilai R dan C. Dengan menentukan nilai R = 8,2 kΩ dan C = 10 µF, maka :

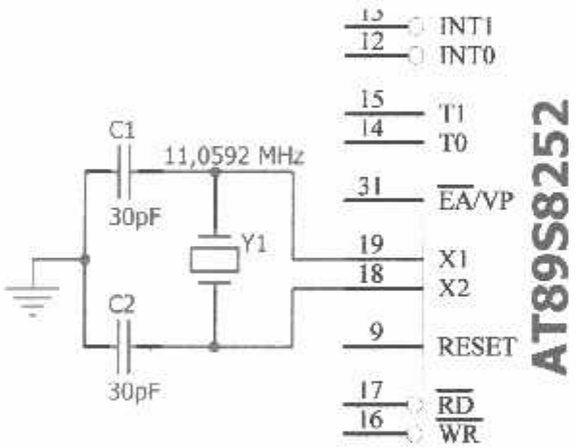
t = 0,357 R.C = 0,357 × 8200Ω × 10.10^{-6} = 29,274 ms

Jadi dengan nilai komponen R = 8,2 kΩ dan C = 10μF dapat memenuhi syarat minimal untuk waktu yang dibutuhkan oleh mikrokontroler.

3.2.5. Perancangan Clock

Kecepatan proses yang dilakukan oleh mikrokontroler ditentukan oleh sumber *clock* yang mengendalikan mikrokontroler tersebut. Sistem yang dirancang ini menggunakan osilator internal yang telah tersedia dalam *chip* AT89S8252. Untuk menentukan frekuensi osilatornya cukup dengan menghubungkan kristal dalam pin 19 (X_1) dan pin 18 (X_2) serta dua buah kapasitor ke *ground*.

Besarnya kapasitansinya disesuaikan dengan spesifikasi dalam lembar data AT89S8252 yaitu 30 pF. Kristal yang digunakan adalah 11,0592 MHz. Gambar 3.6 memperlihatkan rangkaian *clock* yang dirancang.

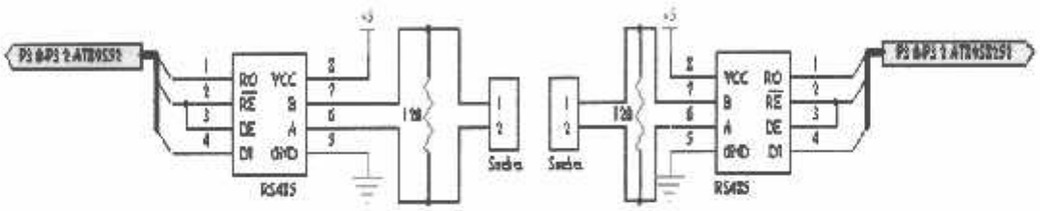


Gambar 3.7. Perancangan Rangkaian *Clock*

3.2.6. Perencanaan rangkaian RS485

Rangkaian RS 485 ini menggunakan IC MAX 485 yang sama dengan rangkaian dalam konveter RS 232 ke RS 485.Untuk pin RE dan DE dihubung singkat sehingga dapat berfungsi sebagai penerima dan pengirim data.

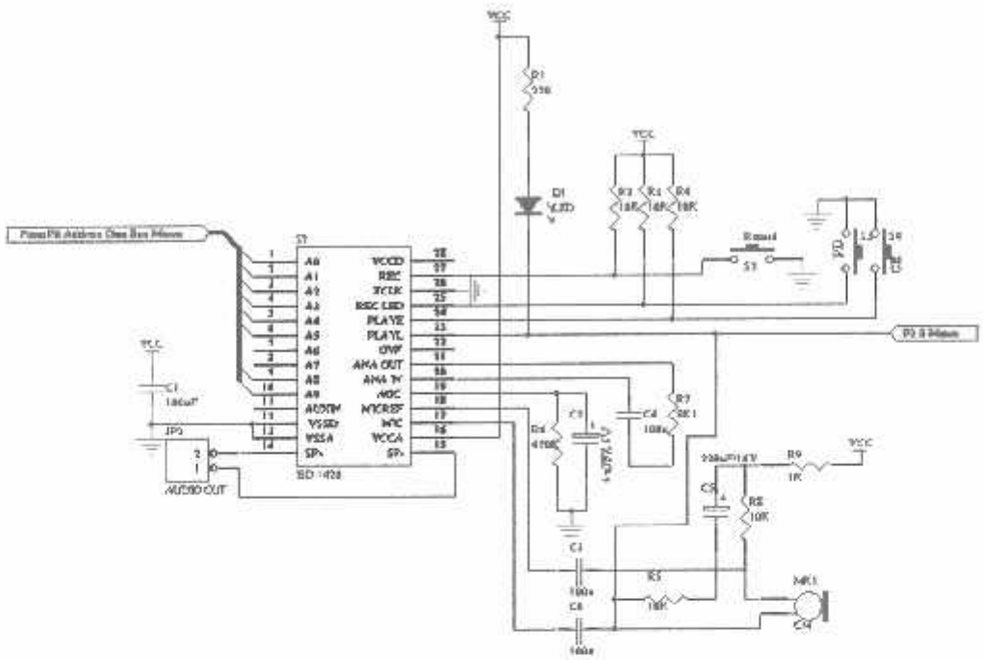
Untuk pin 1 dihubungkan dengan port 3.0/RXD pada mikrokontroller, pin 2 dan 3 dihubungkan pada port 3.2/INT0, pin 4 dihubungkan pada port 3.1/TXD, pin 5 dihubungkan dengan tegangan *supply ground*, pin 5 dan pin 6 masing-masing dihubungkan dengan resistor sebesar 120Ω dan pin 8 dihubungkan dengan tegangan *supply* +5 Volt.



Gambar 3.8. Rangkaian RS485

3.2.7. Perancangan Rangkaian *Information Storage Device* (ISD 1420)

Pada rangkaian ini suara yang di rekam menggunakan *Information Storage Device* ISD 1420 yang disimpan dalam EEPROM. Berdasarkan data sheet, ISD 1420 ini mampu merekam suara dengan lama perekaman 20 detik dengan alamat yang berbeda. Rangkaian ISD 1420 ditunjukkan pada gambar 3.7. Pin *address* data menerima masukan 8 bit dari mikrokontroler *Master* pada Port 0. Alamat-alamat ini akan memilih data suara yang mana yang akan dipanggil. Kemudian untuk pin *Chip Enable* (CE) berfungsi sebagai pengaktifan (*Enabled*), secara aktif *low* yang terkoneksi dengan *Port* 2.0.



Gambar 3.9.Rangkaian ISD 1420

Untuk memberikan peringatan kepada orang yang berada dalam ruangan bahwa sedang terjadi kebakaran menggunakan IC ISD 1420. Sinyal suara merupakan bentuk sinyal analog kemudian diubah menjadi bentuk digital untuk disimpan ke dalam *memory*. Data-data digital yang sudah tersimpan yang berasal dari data analog (suara) dapat dipanggil kembali dengan memanggil alamat penyimpanan datanya. Proses perekaman pada ISD 1420 adalah sebagai berikut :

- Pin *PlayE* pin 23 mendapat logika *low*.
- Memberikan alamat dengan mengatur dip *switch*.
- Kemudian Pin *Playback/Record* pin 27 mendapat logika *low*.
- Perekaman dimulai dengan memasukkan data suara pada mikrofon.
- Pin *Playback/Record* mendapat logika *high* kembali.

- Mencari alamat terakhir yang ditandai pada *REC LED* pin 25 terjadi pulsa *low* sesaat kemudian *high* kembali.
- Demikian seterusnya, untuk melanjutkan perekaman alamat terkhir dari sebelumnya diberikan spasi dan memulai perekaman kembali sampai batas waktu dari kemampuan ISDnya.

Kemudian untuk prosedur pemanggilan data-data suara yang telah direkam adalah sebagai berikut :

- Pin *PlayE* pin 23 mendapat logika *low*.
- Memanggil alamat suara yang diinginkan, pada waktu perekaman tadi.
- Kemudian Pin memberikan logika *low* pada *Playback/Record* pin 27, yang berarti pemanggilan suara dimulai.
- Menunggu pada *REC LED* pin 25 terdapat pulsa logika *low* sesaat.
- Bila sudah terdapat pulsa logika *low* sesaat pada *REC LED*, segera diberikan logika *high* pada pin *PlayE*, ini menandakan akhir dari data suara pada alamat itu.
- Demikian seterusnya pada alamat-alamat selanjutnya, sesuai dengan data suara yang diinginkan.

Tabel 3.2. Data Hasil Perekaman dan Alamatnya Pada ISD 1420

Data Suara yang Direkam	**Alamat Data Suara dalam Biner 8 bit**	**Alamat Data Suara dalam Desimal**
" Kebakaran"	0000 0000	0
"Putus"	0011 0010	50

Dengan memanggil alamat-alamat data yang diinginkan maka terbetuk kalimat-kalimat dari penggalan-penggalan kata-kata yang sudah dialamati.

Dengan memanggil alamat-alamat data yang diinginkan maka terbetuk kalimat-kalimat dari penggalan-penggalan kata-kata yang sudah dialamati.

3.2.8. Rangkaian LCD M1632

LCD Display Module M1632 buatan Seiko Instrument Inc. adalah komponen *display* yang paling umum digunakan saat ini. LCD M1632 merupakan panel LCD sebagai media penampil informasi dalam bentuk huruf/angka dua baris, masing-masing baris bisa menampung 16 huruf/angka.

Untuk berhubungan dengan mikrokontroller, pemakai LCD M1632 dilengkapi dengan 8 jalur data (**DB0..DB7**) yang dipakai untuk menyalurkan kode ASCII maupun perintah pengatur kerjanya M1632. Selain itu dilengkapi pula dengan **E**, **R/W*** dan **RS** seperti layaknya komponen yang kompatibel dengan mikroprosesor.

RS, singkatan dari *Register Select*, dipakai untuk membedakan jenis data yang dikirim ke M1632, kalau **RS=0** data yang dikirim adalah perintah untuk mengatur kerja M1632, sebaliknya kalau **RS=1** data yang dikirim adalah kode ASCII yang ditampilkan.

Demikian pula saat pengambilan data, saat **RS=0** data yang diambil dari M1632 merupakan data status yang mewakili aktivitas M1632, dan saat **RS=1** maka data yang diambil merupakan kode ASCII dari data yang ditampilkan.

Proses mengirim/mengambil data ke/dari M1632 bisa dijabarkan sebagai berikut :

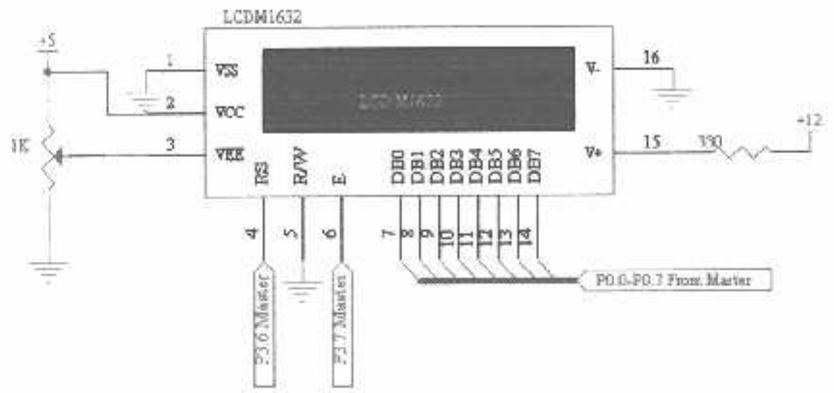
- **RS** harus dipersiapkan dulu, untuk menentukan jenis data seperti yang telah dibicarakan di atas.
- **R/W*** di-nol-kan untuk menandakan akan diadakan pengiriman data ke M1632. Data yang akan dikirim disiapkan di **DB0..DB7**, sesaat kemudian sinyal **E** di-satu-kan dan di-nol-kan kembali. Sinyal **E** merupakan sinyal

sinkronisasi, saat **E** berubah dari 1 menjadi 0 data di **DB0 .. DB7** diterima oleh M1632.

- Untuk mengambil data dari M1632 sinyal **R/W*** di-satu-kan, menyusul sinyal E di-satu-kan. Pada saat **E** menjadi 1, M1632 akan meletakkan datanya di **DB0 .. DB7**, data ini harus diambil sebelum sinyal E di-nol-kan kembali.

M1632 mempunyai seperangkat perintah untuk mengatur tata kerjanya, perangkat perintah tersebut meliputi perintah untuk menghapus tampilan, meletakkan kembali cursor pada baris huruf pertama baris pertama, menghidup/matikan tampilan dan lain sebagainya, semua itu dibahas secara terperinci dalam Lembar Data M1632.

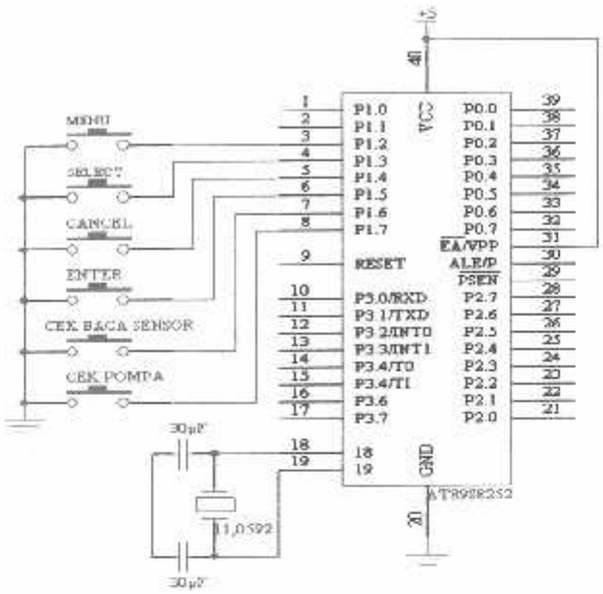
Untuk tampilan dipergunakan LCD Dot Matrik 2 x 16 karakter. Sinyal-sinyal yang diperlukan oleh LCD adalah RS dan *Enable*, sinyal RS dan *Enable* dipergunakan sebagai input yang outputnya dipakai untuk mengaktifkan LCD. LCD akan aktif apabila mikrokontroller memberikan instruksi tulis pada LCD. Saat kondisi RS *don't care* dan *Enable* 0 maka LCD tetap pada kondisi semula, pengiriman data ke LCD dilakukan saat RS berlogika 1 dan *enable* berlogika 1. Instruksi dikirim pada LCD bila keadaan RS 0 dan *Enable* 1. Pin LCD ini untuk data terkoneksi pada *Port 0* mikrokontoller. Kemudian untuk RS dihubungkan pada *Port 3.6 Master*, tulis/baca (*Read/Write)* diberikan logika *low* karena disini LCD bersifat menulis data, dan yang terakhir *Enable* (E) dikendalikan dengan *Port* 3.7 *Master*.Gambar rangkaian LCD ditunjukkan pada gambar 3.8 sebagai berikut :



Gambar 3.10. Perancangan Rangkaian *Liquid Crystal Display* (LCD)

3.2.9 Rangkaian Keypad

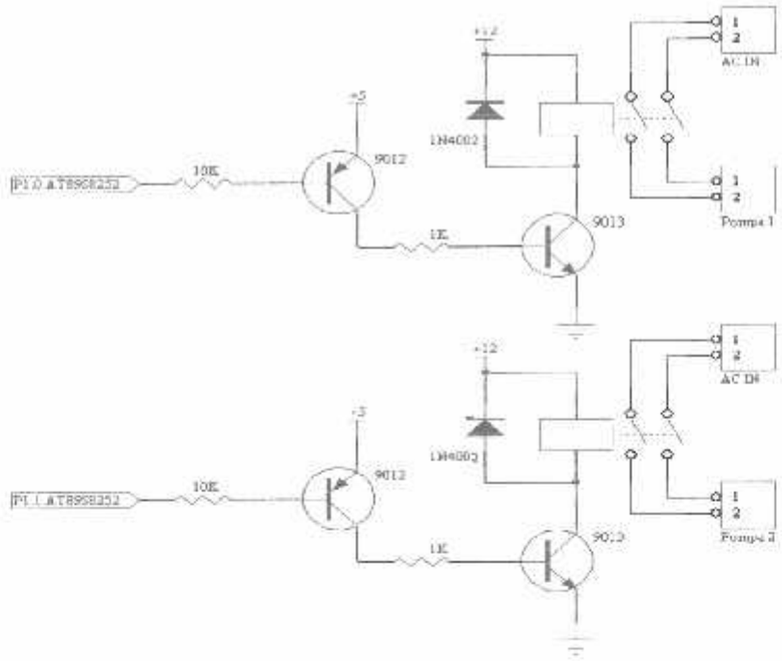
Rangkaian *keypad* dalam perencanaan ini menggunakan *keypad matrik push button.* Tombol disini berfungsi untuk mengeset besarnya suhu dan asap sesuai dengan yang diinginkan. Tombol pada perencanaan alat ini terdiri dari 6 pilihan utama diantaranya: Menu, Select, Cancel, Enter, Cek Baca Sensor dan Cek Pompa Penyemprot. Pada tombol ini terletak pada mikrokontroller *Master* pada port P1.2, P1.3, P1.4, P1.5, P1.6 dan P1.7. Mikrokontroller *Master* akan aktif apabila salah satu tombol ditekan dengan memberikan logika 0 pada salah satu port. Gambar rangkaian keypad ditunjukkan pada gambar 3.9 sebagai berikut.



Gambar 3.11. Rangkaian *Keypad Matriks*

3.2.10. Perancangan Rangkaian Driver Pompa air

Perancangan rangkaian driver yang digunakan untuk menggerakkan relay yang terhubung dengan pompa yang terdiri dari transistor NPN 9013 dan transistor PNP 9012 yang difungsikan sebagai transistor *switching*. Relay yang dihubungkan dengan pompa diberi dioda yang dirangkai paralel dengan relay dengan tujuan untuk menghindari tegangan mundur yang dibangkitkan oleh relay sehingga tidak merusak transistor juga untuk mencegah arus balik yang ditimbulkan dari L(induktor) setelah mengalami perubahan dari saturasi ke cutoff. Gambar rangkaian driver pompa air ditunjukkan pada gambar 3.10 sebagai berikut.



Gambar 3.12. Rangkaian *Driver* Pompa air

Diketahui dari data sheet transistor 9012 besarnya I_C=80mA, hfe = 120, V_{BE} = 0,7 Volt, sehingga:

$I_C = I_B * hfe$

$$I_B = \frac{I_C}{hfe}$$

$$I_B = \frac{50mA}{120} = 0{,}416mA$$

Maka R_B adalah:

$$R_B = \frac{V_{CC} - Vbe}{I_B}$$

$$R_B = \frac{5 - 0{,}7}{0{,}416mA}$$

$$= \frac{4{,}3}{0{,}416mA} = 10{,}33.10^3$$

Jadi dari hasil perhitungan diatas diperoleh nilai R_B sebesar $10{,}33.10^3\Omega$ atau disederhanakan menjadi $10K\Omega$.

Sedangkan dari data sheet transistor 9013 besarnya I_C = 180mA, hfe =50, V_{BE} = 0,7 Volt ,sehingga:

$$I_B = \frac{180mA}{50} = 3{,}6mA$$

Maka R_B adalah:

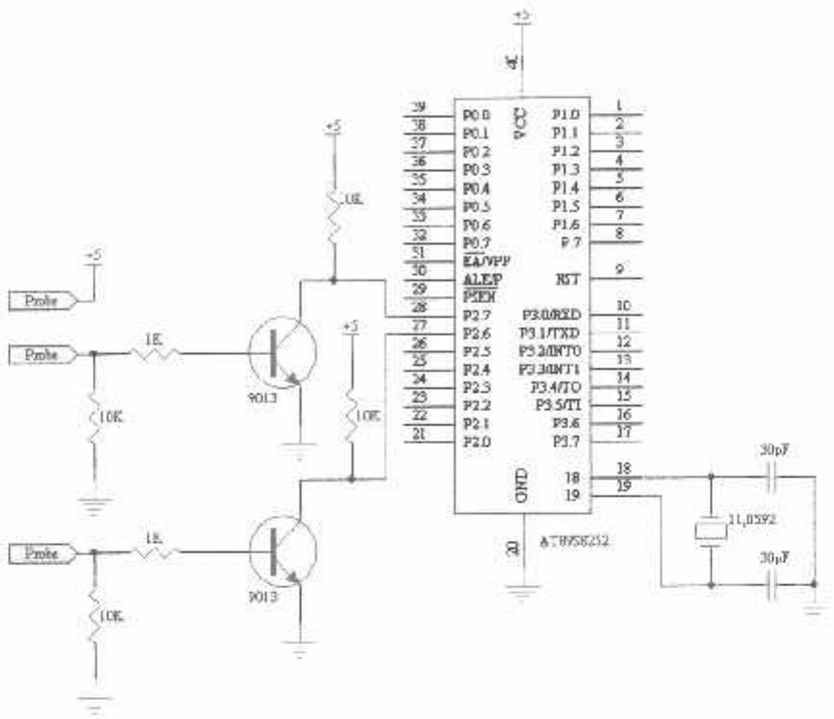
$$R_B = \frac{5 - 0{,}7}{3{,}6mA}$$

$$= \frac{4{,}3}{3{,}6mA} = 1{,}2.10^3\Omega$$

Jadi dari hasil perhitungan diatas diperoleh nilai R_B sebesar $1{,}2.10^3\ \Omega$, tetapi dalam perancangan ini kami pakai $1K\Omega$

3.2.11. Perencanaan Rangkaian Sensor Level Air

Sensor air berfungsi untuk mendeteksi level air. Sensor air yang digunakan pada perancangan alat ini adalah sensor air yang terdiri dari logam-logam yang berbentuk stick yang terdiri dari tiga buah logam. Sensor ini bekerja bila sensor level bawah sudah tidak menyentuh air dan level atas menyentuh air. Dengan prinsip kerja jika dua stick logam yang panjang (anoda) menyentuh air, maka air akan bermuatan positif, proses ini akan berjalan sampai air menyentuh stick logam yang pendek (katoda). Ketika air menyentuh katoda maka akan terjadi hubung singkat yang memberikan instruksi logika 1 kepada relay untuk mematikan pompa. Gambar rangkaian sensor air ditunjukkan pada gambar 3.11 sebagai berikut.

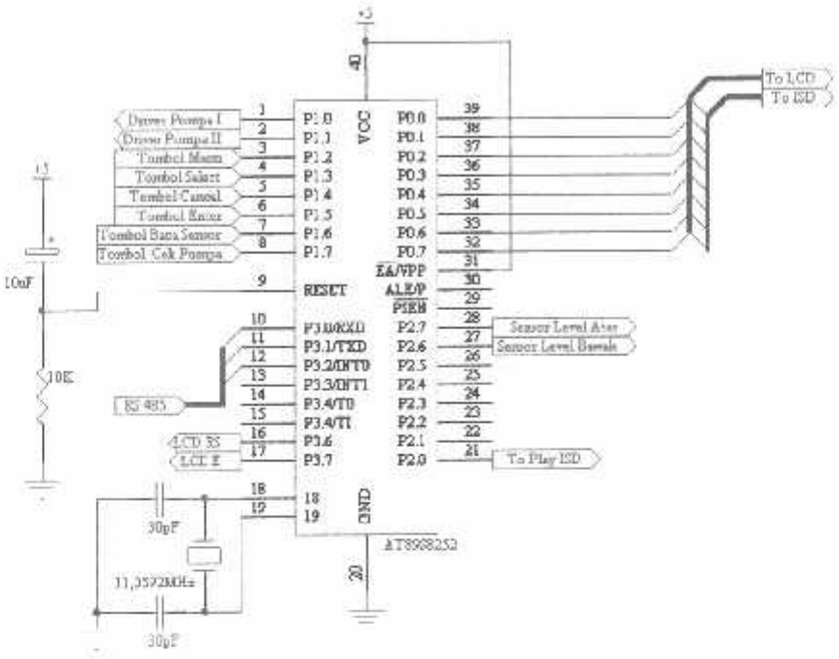


Gambar 3.13. Rangkaian Sensor Level Air

3.2.12. Perancangan Minimum System Mikrokontroller Master AT89S8252

Mikrokontroller *Master* merupakan pengendali utama,dalam hal ini menggunakan mikrokontroller AT89S8252. Rangkaian mikrokontroller AT89S8252 berfungsi sebagai pengolah data yang dihasilkan oleh penekanan keypad yang berfungsi sebagai inputan dan menampilkan data tersebut ke dalam LCD dan ISD1420 yang berfungsi sebagai output.

Pengaturan jalur *input* dan *output* pada rangkaian mikrokontroller untuk sebuah rancangan terpogram, sangat berkaitan erat dengan progam yang kita buat. Dalam mikrokontroller menyediakan jalur-jalur 32 input-output yang dapat digunakan secara bersamaan untuk tiap kelompok terisi 8 bit. Adapun rangkaiannya ditunjukkan seperti pada gambar 3.12 dibawah ini:



Gambar 3.14. Rangkaian Mikrokontroller *Master* AT89S8252

Berikut adalah fungsi dari pin-pin mikrokontroller *master*:

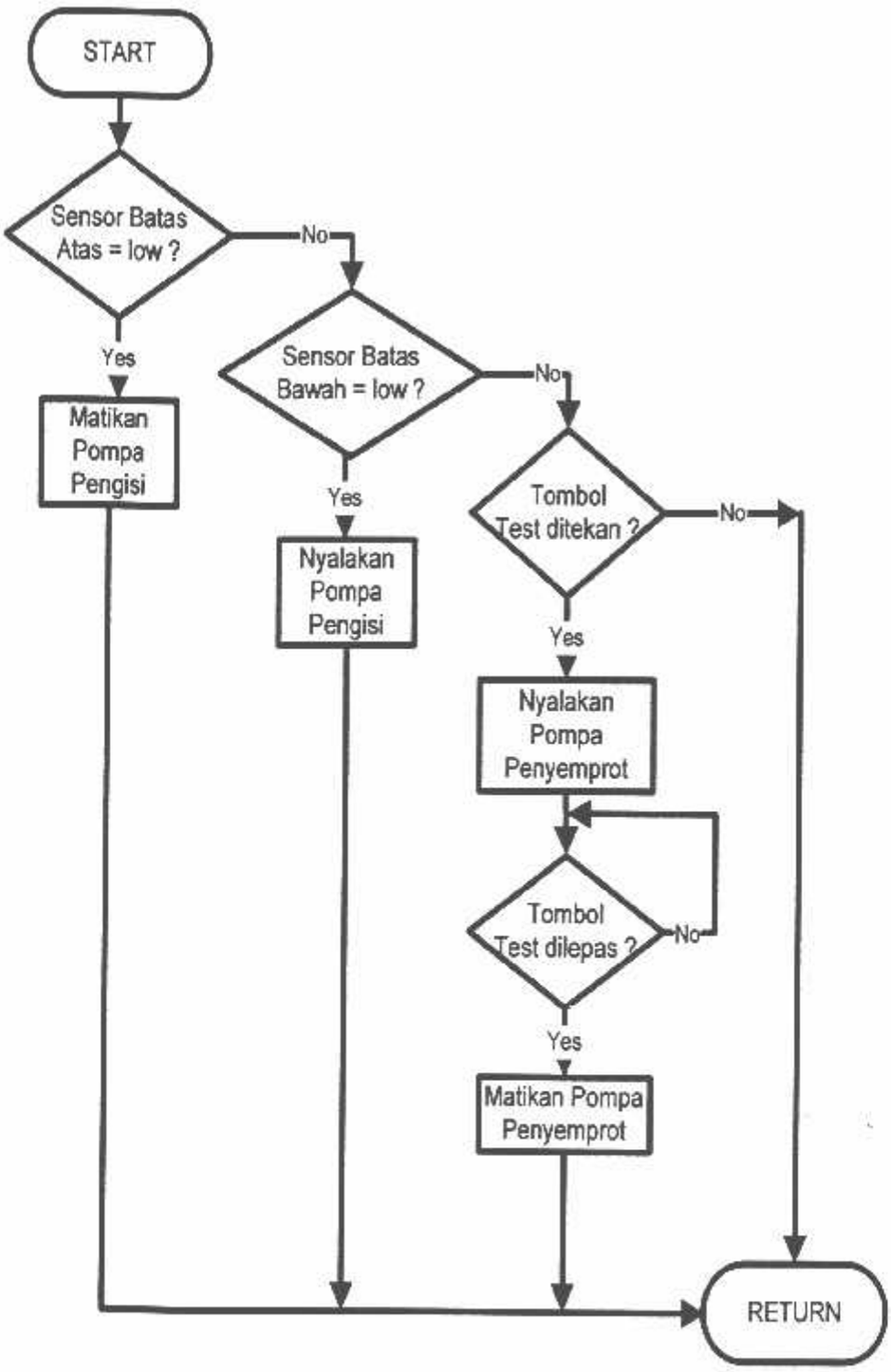
1. Port 1.0 digunakan untuk mengaktifkan rangkaian driver relay I jika air pada tandon habis maka pompa I akan nyala dan ketika air pada tandon penuh maka pompa I akan berhenti.
2. Port 1.1 digunakan untuk mengaktifkan rangkaian *driver* relay II apabila terjadi kebakaran sehingga akan mengaktifkan pompa II dan air akan menyemprot.
3. Port 1.2 berfungsi sebagai inputan dari tombol Menu yang berisi batas suhu dan batas asap.
4. Port 1.3 berfungsi sebagai inputan dari tombol Select yang berisi pilihan apakah memilih setting suhu atau asap dan memilih *range* yang diinginkan.
5. Port 1.4 berfungsi sebagai inputan dari tombol Cancel apabila ingin kembali ke menu semula.

6. Port 1.5 berfungsi sebagai inputan dari tombol Enter yaitu masuk ke menu yang diinginkan.
7. Port 1.6 berfungsi sebagai inputan dari tombol Cek Baca Sensor yaitu mengetahui sensor tesebut mendeteksi asap dan gas pada ruangan.
8. Port 1.7 berfungsi sebagai inputan dari tombol Cek Pompa apakah pompa tersebut bisa menyemprot atai tidak.
9. Port 0.0-0.7 berfungsi sebagai output data ke LCD dan ISD.
10. Port 2.0 berfungsi untuk mengaktifkan ISD.
11. Port 2.7 berfungsi sebagai sensor level atas.
12. Port 2.6 berfungsi sebagai sensor level bawah
13. Port 3.6 memberikan pulsa ke RS pada LCD.
14. Port 3.7 memberikan pulsa ke E(enable) pada LCD.
15. Port 3.0-3.2 berfungsi untuk menerima data dari RS 485.

3.2.13. Perancangan Mikrokontroller *Slave* Untuk Sensor Suhu dan Asap

Mikrokontroler *Slave 1* menggunakan mikokontroler AT89S52. Mikrokontroler ini bertugas menerima masukan dari sensor gas CO AF-30 dan sensor suhu LM35 kemudian mengirimkan data ke mikrokontroller *Master*. Berikut ini adalah konfigurasi pin-pin yang digunakan :

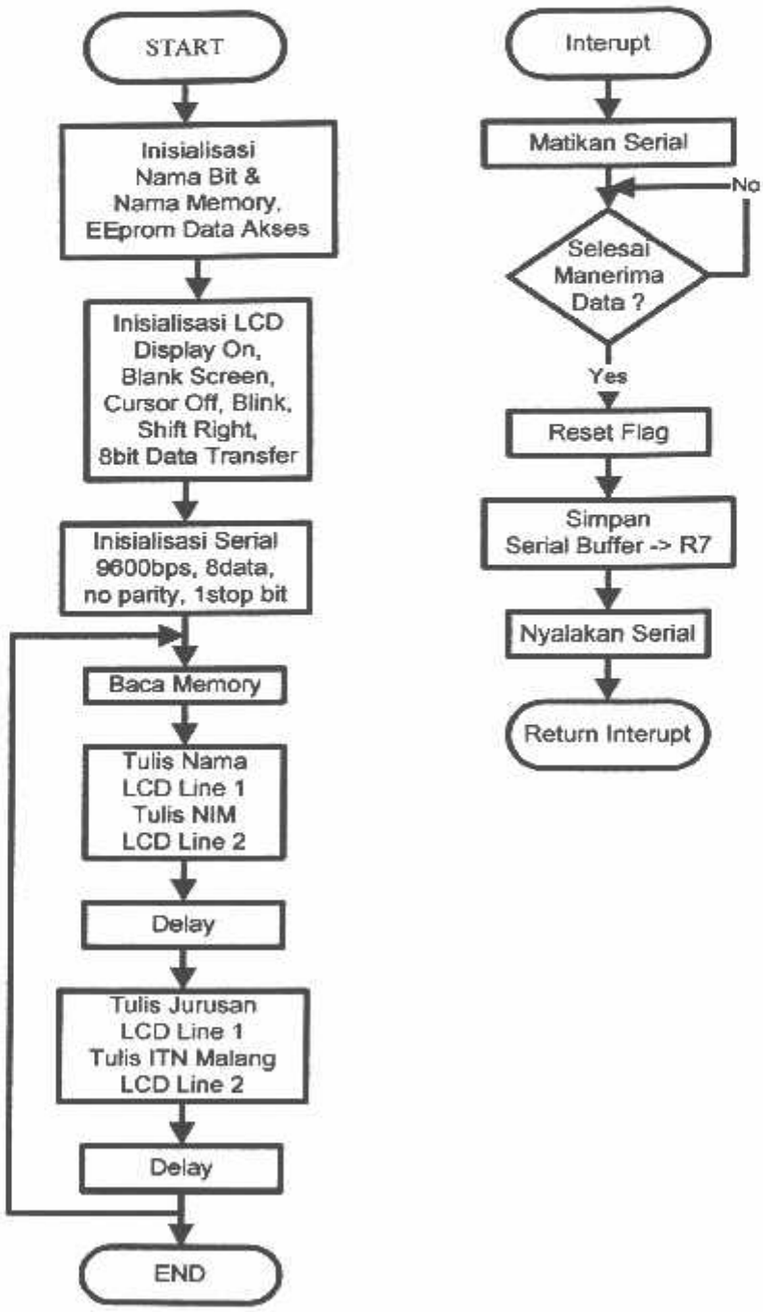
3.3.2. *Flowchart* Untuk Cek Tandon



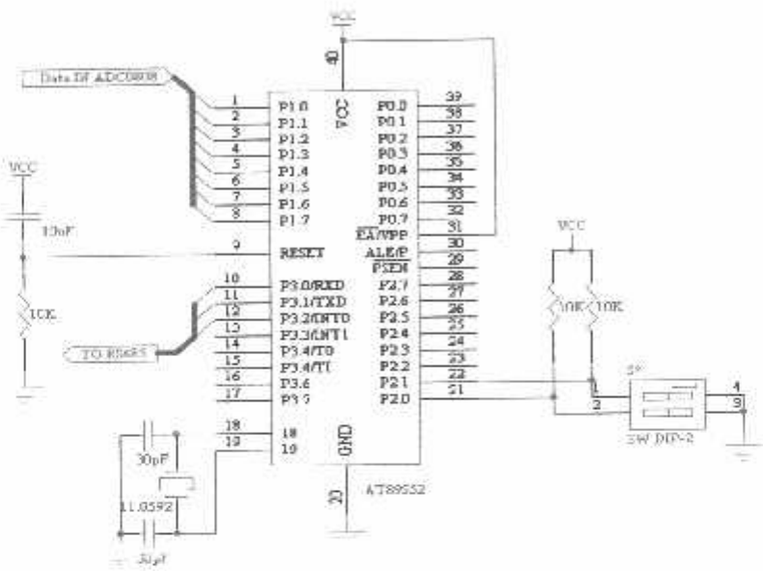
Gambar 3.17. *Flowchart* Cek Tandon

dengan apa yang direncanakan. Mikrokontroller AT89S8252 menggunakan bahasa *assembly* MCS-51 karena mikrokontroller ini adalah masih keluarga MCS-51.

3.3.1. *Flowchart* Pada Mikrokontroller Master



Gambar 3.16. *Flowchart* Mikrokontroller Master AT89S8252



Gambar 3.15. Rangkaian Mikrokontroller *Slave* AT89S52

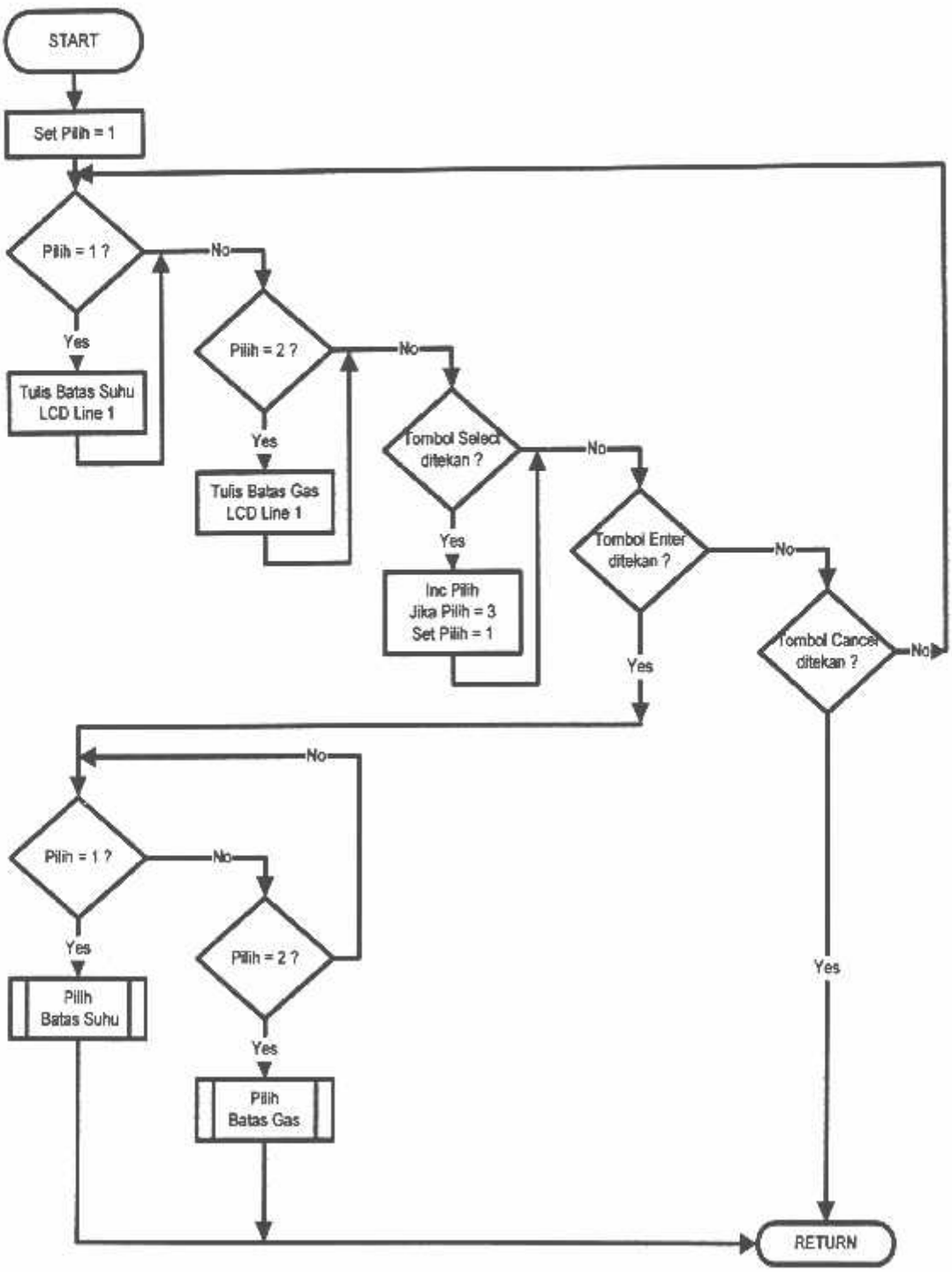
Berikut penjelasan dari gambar diatas:

1. Port 1 menerima masukan dari data ADC 0808 dimana mikrokontroller *Slave* ini memproses masukan data dari ADC yang berupa sensor suhu dan asap.
2. Port 3: P3.0-P3.2 sebagai output dari mikrokontroller *Slave* yang akan diterima RS485 yang berfungsi sebagai komunikasi serial yang akan mengirimkan data ke mikrokontroller *Master*.
3. Port 2: P2.0-P2.1 sebagai alamat address data mikrokontroller *Slave*.

3.3. Perancangan Perangkat Lunak (*Software*)

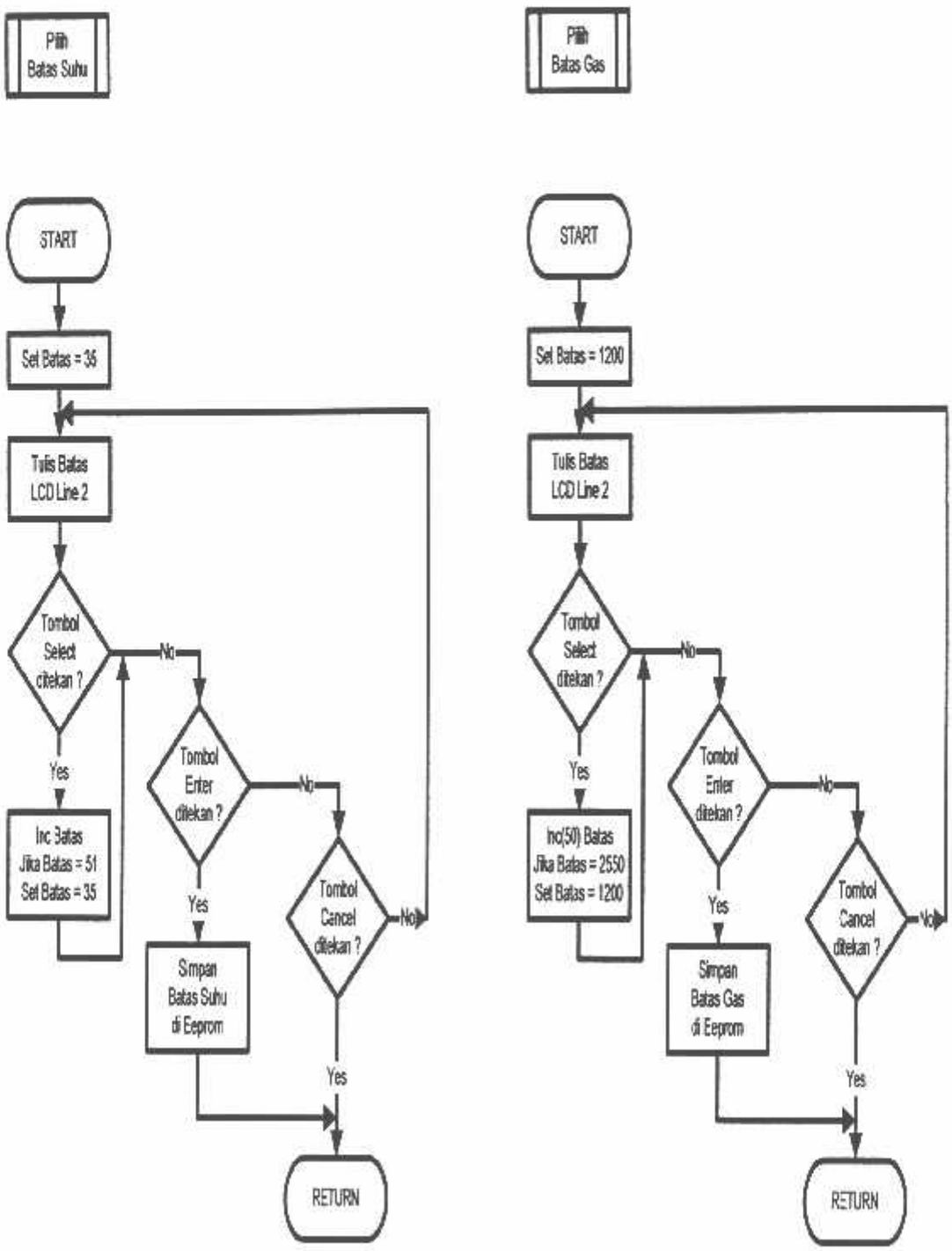
Perancangan perangkat lunak (*software*) sangat diperlukan oleh *programmer* dalam mempermudah menentukan langkah-langkah atau alur dari program. Selain mempermudah langkah-langkah pemrograman, diagram alir juga difungsikan supaya program sesuai dan sinkron dengan kerja perangkat keras (*hardware*), sehingga sesuai

3.3.3. *Flowchart* Tampilan LCD Untuk Pilih Batas Suhu Dan Gas



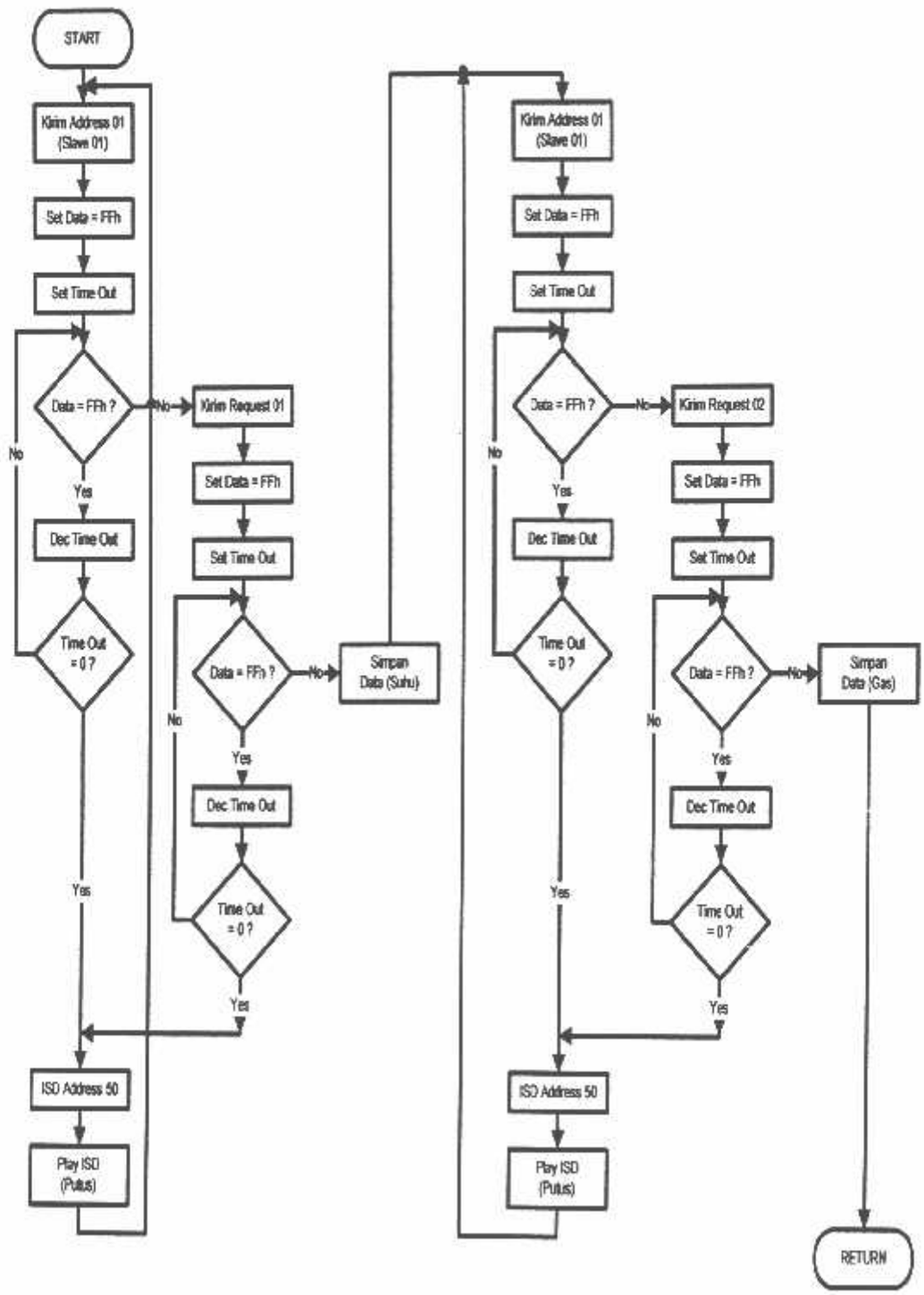
Gambar 3.18. *Flowchart* Tampilan LCD Pilih Batas Suhu dan Gas

3.3.4. *Flowchart* Pilih Batas Suhu Dan Pilih Batas Gas



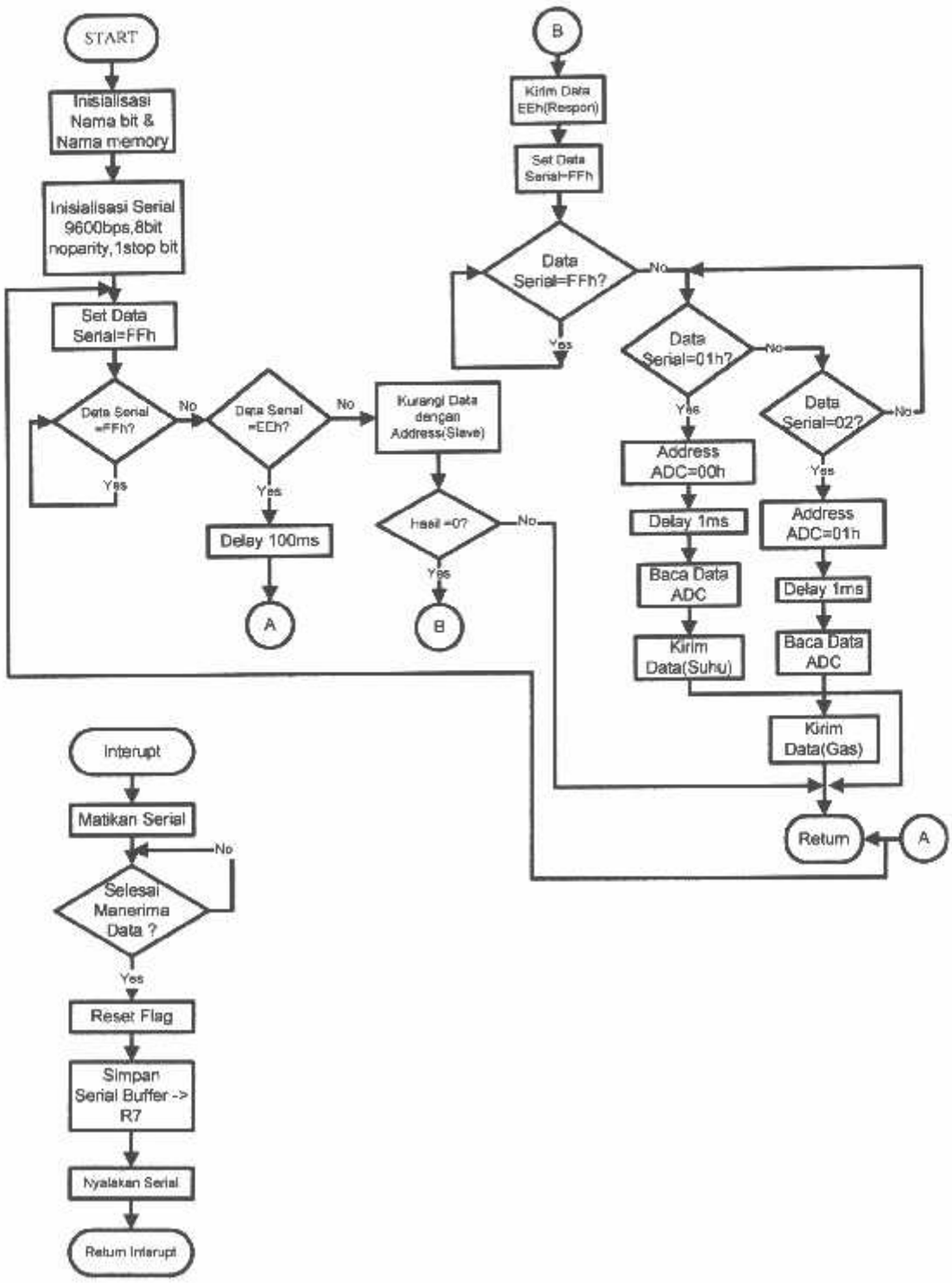
Gambar 3.19.*Flowchart* Pilih Batas Suhu Dan Pilih Batas Gas

3.3.5. *Flowchart* Baca Sensor



Gambar 3.20. *Flowchart* Baca Sensor

3.3.6. *Flowchart* Pada Mikokontroller *Slave*



Gambar 3.21. *Flowchart* Mikokontroller *Slave* AT89S52

BAB IV

PENGUJIAN DAN PERCOBAAN ALAT

4.1. Pendahuluan

Dalam bab ini akan dibahas tentang pengujian alat yang telah dirancang dan dibuat secara keseluruhan. Adapun tujuan dari pengujian alat adalah untuk mengetahui apakah alat yang sudah direncanakan dan dibuat dapat bekerja dengan baik sesuai dengan perencanaan.

4.2. Pengujian Sensor Suhu

Pada pengujian sensor suhu dilakukan pada suhu ruangan menggunakan thermometer air raksa. Tujuan dilakukan percobaan ini adalah untuk mengetahui sensor suhu sesuai dengan tegangan keluaran sensor suhu yaitu 10mV/^{0}C.Untuk menaikkan resolusi pembacaan data suhu, maka output dari sensor diumpankan ke suatu rangkaian penguat *non-inverting*. Pada pengujian sensor suhu ada beberapa pengukuran yang harus dilakukan antara lain sebagai berikut:

4.2.1.Pengukuran Untuk Mencari Besarnya Penguatan Vout Sensor Suhu

Untuk mengetahui penguatan dari penguat non-inverting dapat dicari dengan membandingkan antara jumlah Vout *Op-Amp* dan Vout sensor.

Berikut ini persamaan untuk mengetahui penguatan rata-rata dari output sensor beserta hasilnya:

$$A_{rata\text{-}rata} = \frac{\Sigma V_{out}}{\Sigma V_{in}} = \frac{\Sigma V_{op-amp}}{\Sigma V_{out-sensor}}$$

Tabel 4.1 Pengukuran Vout Sensor dan Vout *Op-Amp*

Temperatur (^{0}C)	Vout Sensor (mV)	Vout Op-Amp (mV)
25	250	517
30	300	575
35	350	680
40	400	780
45	450	890
50	500	1004
Jumlah	2250	4451
Penguatan(A) rata-rata	1.98 kali	

4.2.2. Pengujian Untuk Mencari Kesalahan Rata-rata Dari Vout Sensor

Pada pengujian ini untuk mencari kesalahan Vout sensor yaitu dengan menggunakan persamaan sebagai berikut:

$$\Delta\% = \left| \frac{Vout\_sensor(pengukuran) - Vout\_sensor(datasheet)}{Vout\_sensor(datasheet)} x100\% \right|$$

$$\text{Kesalahan rata-rata} = \left| \frac{\Sigma\Delta\%}{\Sigma pengukuran} \right|$$

Tabel 4.2 Perbandingan Vout Sensor Data Sheet Dengan Vout Sensor Pengukuran

Temperatur (^{0}C)	Vout Sensor (mV)		Δ%
	Data Sheet	Pengukuran	
25	250	253	1,2
30	300	304	1,3
35	350	352	0,7
40	400	402	0,5
45	450	454	0,8
50	500	503	0,6
Kesalahan Rata-rata (*error*)			0,85 %

4.2.3. PengujianUntuk Mencari Kesalahan Rata-rata Vout *Op-Amp*

Pada pengujian ini untuk mencari kesalahan Vout *Op-Amp* yaitu dengan persamaan sebagai berikut:

$$\Delta\% = \left| \frac{Vout\_Op-Amp(pengukuran) - Vout\_Op-Amp(perhitungan)}{Vout\_Op-Amp(perhitungan)} x100\% \right|$$

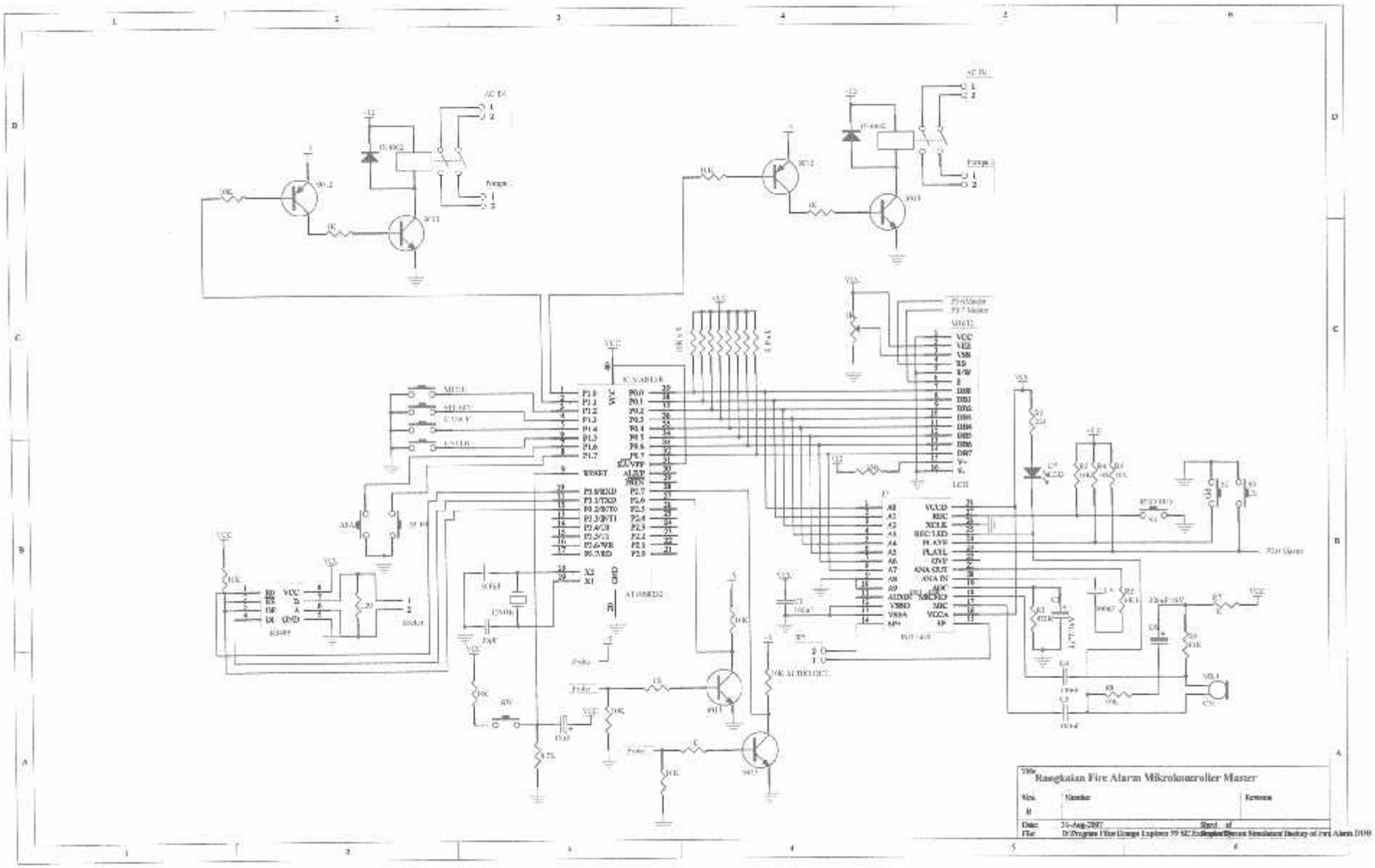
$$\text{Kesalahan Rata-rata} = \left| \frac{\Sigma\Delta\%}{\Sigma pengukuran} \right|$$

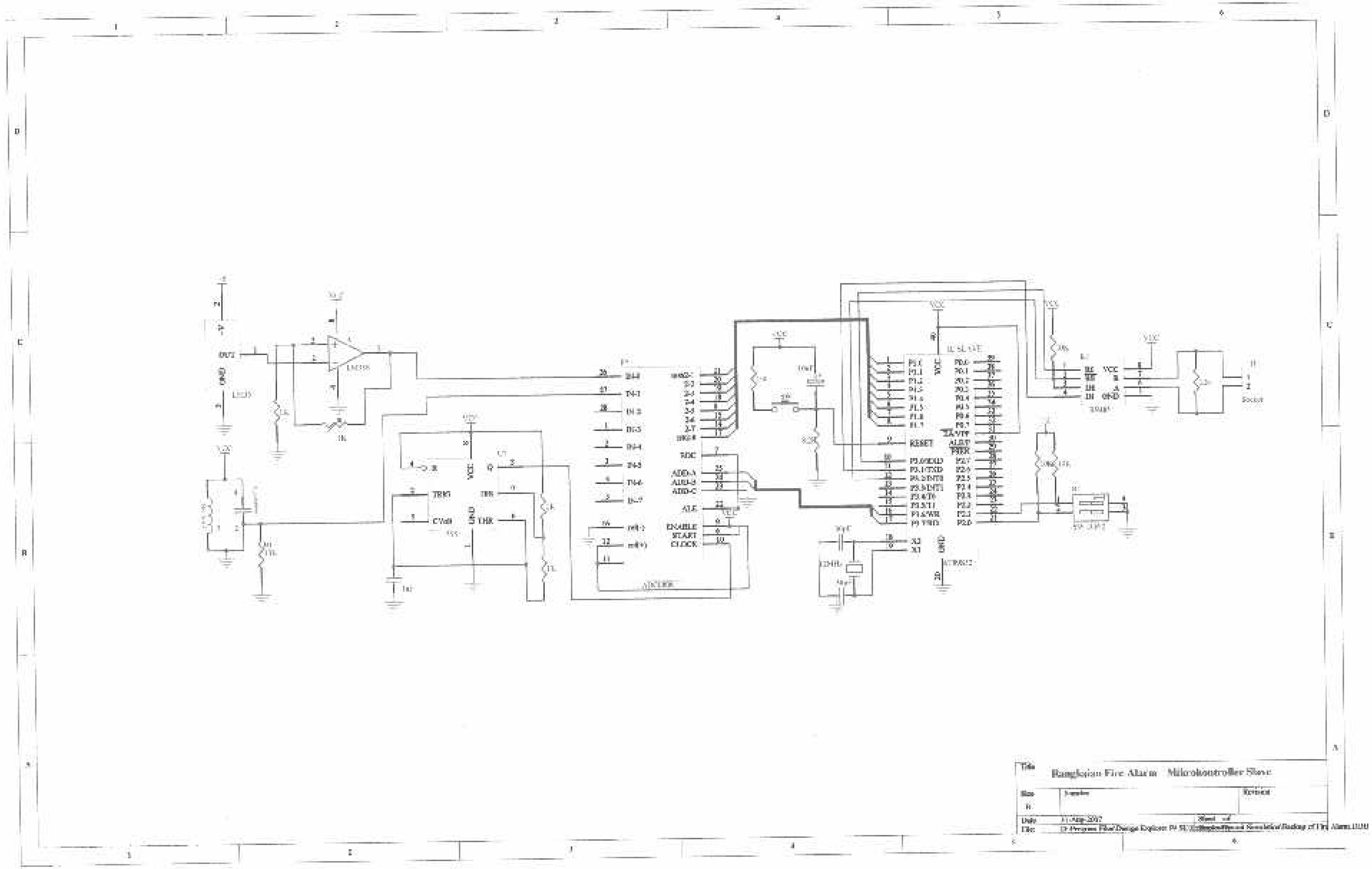
Tabel 4.3 Perbandingan Vout *Op-Amp* Perhitungan Dengan Vout *Op-Amp* Pengukuran

Temperatur (^{O}C)	Vout Op-Amp (mV)		Δ%
	Perhitungan	Pengukuran	
25	500	517	3,4
30	600	575	4,2
35	700	680	2,86
40	800	780	2,5
45	900	890	1,1
50	1000	1004	0,4
Kesalahan Rata-Rata (*error*)			2,41%

4.3. Pengujian Sensor Asap

Dari hasil pengujian dengan menggunakan voltmeter digital didapat bahwa resistansi load resistor untuk menghasilkan teganagan ouput yang dapat mengaktifkan sensor adalah 10KΩ dengan nilai tegangan antara 0,22 - 4,78V, nilai ouput maksimal bagi ADC 0808 adalah 5 volt, hal ini disebabkan Vref ADC 0808 sebesar 5V.


Rangkaian Fire Alarm Mikrokontroller Master
Rev
Number
Revision
Date:
Sheet of
File:



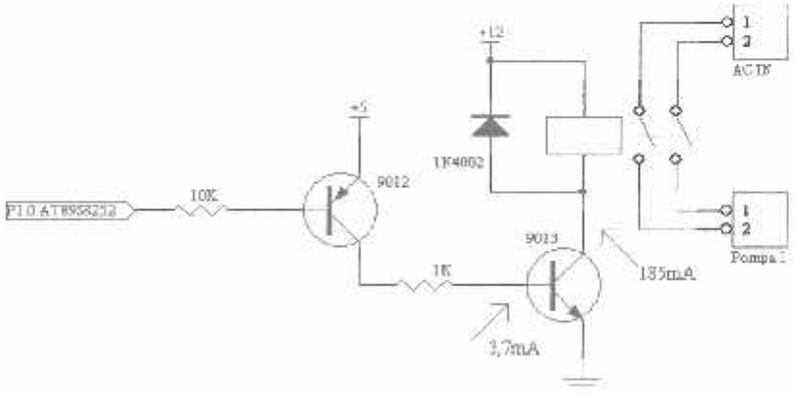
LM358
ADC0808
AT89S52
RESET
ENABLE
START
CLOCK
ALE
EOC
ADD-A
ADD-B
ADD-C
VCC
GND
TRIG
THR
Socket
Title
Rangkaian Fire Alarm Mikrokontroller Slave
Size
Number
Revision
Date
File
Sheet of

4.5. Pengujian *Driver* Relay

Pada pengujian *driver* relay ini berfungsi untuk menguji apakah rangkaian *driver* relay bisa bekerja sesuai dengan yang direncanakan. Dalam alat ini menggunakan dua rangkaian *driver* relay yaitu: Rangkaian *driver* relay I yang bertugas mengisi tandon jika air habis dan sebagai pemutus ke pompa I jika air dalam tandon penuh dan relay II berfungsi sebagai penghubung ke pompa II jika terjadi kebakaran dan sebagai pemutus ke pompa II bila api padam. Berikut ini hasil pengujian dari *driver* relay.

Tabel 4.6 Hasil Pengujian *Driver* Relay

Logic	Vlogic	Vdriver	Vrelay(V)	Keterangan
0	0,02	0,3	11,4	Aktif
1	4,87	11,72	0,38	Tidak Aktif



Perhitungan mencari besarnya Ib pada transistor 9013 yaitu:

$$Ib = \frac{Vcc}{Rb}$$

$$Ib = \frac{3,7}{1K} = 3,7mA$$

Ic = Ib x Hfe

LAMPIRAN

```
        org     0h
        ljmp    init

        org     23h
        clr     ES
        jnb     RI,$
        clr     RI
        mov     R7,SBUF
        setb    ES
        reti

        Wmcn    Data 96h                ; data write memory control
        Eemn    Equ 00001000b           ; data eeprom enable (read)
        Eemw    Equ 00010000b           ; data eeprom write
        Wtdg    Equ 00000010b           ; data watchdog
        Rly0    Bit P1.0                ; relay 0
        Rly1    Bit P1.1                ; relay 1
        Tbl0    Bit P1.2                ; tombol menu
        Tbl1    Bit P1.3                ; tombol select
        Tbl2    Bit P1.4                ; tombol cancel
        Tbl3    Bit P1.5                ; tombol enter
        Tbl4    Bit P1.6                ; tombol reset suhu
        Tbl5    Bit P1.7                ; tombol reset asap
        Ply1    Bit P2.0                ; play ISD
        Adr0    Bit P2.1                ; dip-switch address 0
        Adr1    Bit P2.2                ; dip-switch address 1
        Lev0    Bit P2.6                ; level air 0
        Lev1    Bit P2.7                ; level air 1
        Slct    Bit P3.2                ; select sensor suhu / gas
        Rest    Bit P3.6                ; reset LCD
        Enbl    Bit P3.7                ; enable LCD
        Dta0    Equ 30h                 ;\
        Dta1    Equ 31h                 ; | data suhu
        Dta2    Equ 32h                 ; | cacah data suhu
        Dta3    Equ 33h                 ;/
        Dta4    Equ 34h                 ;\
        Dta5    Equ 35h                 ; | data gas
        Dta6    Equ 36h                 ; | cacah data gas
        Dta7    Equ 37h                 ;/
        Stsh    Equ 38h                 ; setting suhu
        Stgs    Equ 39h                 ; setting gas
        Buf0    Equ 3Ah                 ; buffer pilih 0
        Buf1    Equ 3Bh                 ; buffer pilih 1
        Sshu    Equ 3Ch                 ; status suhu
        Sgas    Equ 3Dh                 ; status gas
        Hurf    Equ 40h                 ; character LCD
        Cntr    Equ 41h                 ; counter
        Tmt0    Equ 42h                 ; timeout 0
        Tmt1    Equ 43h                 ; timeout 1
        Dly0    Equ 44h                 ; delay 0
        Dly1    Equ 45h                 ; delay 1
        Dly2    Equ 46h                 ; delay 2
        Dly3    Equ 47h                 ; delay 3

iit:    acall   lcd_in                  ; inisialisasi LCD
        acall   srl_in                  ; inisialisasi serial
        acall   rd_mem

lai:    mov     DPTR,#nama
        acall   line1
        mov     Hurf,#16
        acall   tulis
        acall   line2
        mov     Hurf,#16
        acall   tulis
        acall   delay1
        mov     DPTR,#jrusan
        acall   line1
```

```
          mov     Hurf,#16
          acall   tulis
          acall   line2
          mov     Hurf,#16
          acall   tulis
          acall   delay1
          sjmp    mulai

iamenu:   jnb     Tb10,$                ; tunggu lepas tombol menu
          acall   rd_mem
ienu00:   cjne    R0,#0,menu01
          mov     DPTR,#stgshu
ienu01:   cjne    R0,#1,menu02
          mov     DPTR,#stggas
ienu02:   acall   line1
          mov     Hurf,#16
          acall   tulis
          mov     DPTR,#kosong
          acall   line2
          mov     Hurf,#16
          acall   tulis
ienu03:   mov     DPTR,#angka
          cjne    R0,#0,menu04
          mov     P0,#0C6h
          acall   w_ins
          mov     A,Stsh
          mov     B,#10
          div     AB
          acall   wr_chr
          mov     A,B
          acall   wr_chr
          mov     P0,#0DFh
          acall   w_chr
          mov     P0,#'C'
          acall   w_chr
          mov     P0,#0D0h              ; buang cursor
          acall   w_ins
          sjmp    menu05
ienu04:   mov     P0,#0C4h
          acall   w_ins
          mov     A,Stgs
          mov     B,#100
          div     AB
          acall   wr_chr
          mov     A,B
          mov     B,#10
          div     AB
          acall   wr_chr
          mov     A,B
          acall   wr_chr
          mov     P0,#'0'
          acall   w_chr
          mov     P0,#'p'
          acall   w_chr
          mov     P0,#'p'
          acall   w_chr
          mov     P0,#'m'
          acall   w_chr
          mov     P0,#0D0h              ; buang cursor
          acall   w_ins
ienu05:   jnb     Tb11,$                ; tunggu lepas tombol select
ienu06:   acall   jeda
          jb      Tb11,menu08           ; cek tekan tombol select
          inc     R0
          cjne    R0,#2,menu07
          mov     R0,#0
ienu07:   ljmp    menu00
ienu08:   jb      Tb12,menu09
```

```
        mov     SP,#07h                 ; reset RAM
        ljmp    mulai
enu09:  jb      Tbl3,menu06
        jnb     Tbl3,$                  ; tunggu lepas tombol enter
        mov     DPTR,#plhbts
        acall   line1
        mov     Hurf,#16
        acall   tulis

bmn00:  cjne    R0,#0,sbmn10            ; cek pilih sub menu suhu
        mov     Buf0,#35                ; awal set batas suhu
        mov     DPTR,#angka
bmn01:  mov     P0,#0C6h
        acall   w_ins
        mov     A,Buf0
        mov     B,#10
        div     AB
        acall   wr_chr
        mov     A,B
        acall   wr_chr
        mov     P0,#0DFh
        acall   w_chr
        mov     P0,#'C'
        acall   w_chr
        mov     P0,#0D0h                ; buang cursor
        acall   w_ins
        jnb     Tbl1,$                  ; tunggu lepas tombol select
bmn02:  acall   jeda
        jb      Tbl1,sbmn04             ; cek tekan tombol select
        inc     Buf0
        mov     A,Buf0
        cjne    A,#51,sbmn03
        mov     Buf0,#35
bmn03:  sjmp    sbmn01
bmn04:  jb      Tbl2,sbmn05
        mov     SP,#07h                 ; reset RAM
        ljmp    mulai
bmn05:  jb      Tbl3,sbmn02
        mov     Stsh,Buf0
        acall   wr_mem
        mov     SP,#07h                 ; reset RAM
        ljmp    mulai

bmn10:  mov     Buf1,#120               ; awal set batas gas
        mov     DPTR,#angka
bmn11:  mov     P0,#0C4h
        acall   w_ins
        mov     A,Buf1
        mov     B,#100
        div     AB
        acall   wr_chr
        mov     A,B
        mov     B,#10
        div     AB
        acall   wr_chr
        mov     A,B
        acall   wr_chr
        mov     P0,#'0'
        acall   w_chr
        mov     P0,#'p'
        acall   w_chr
        mov     P0,#'p'
        acall   w_chr
        mov     P0,#'m'
        acall   w_chr
        mov     P0,#0D0h                ; buang cursor
        acall   w_ins
        jnb     Tbl1,$                  ; tunggu lepas tombol select
```

```
;bmn12: acall   jeda
        jb      Tb11,sbmn14             ; cek tekan tombol select
        inc     Buf1
        inc     Buf1
        inc     Buf1
        inc     Buf1
        inc     Buf1
        mov     A,Buf1
        cjne    A,#255,sbmn13
        mov     Buf1,#120
;bmn13: sjmp    sbmn11
;bmn14: jb      Tb12,sbmn15
        mov     SP,#07h                 ; reset RAM
        ljmp    mulai
;bmn15: jb      Tb13,sbmn12
        mov     Stgs,Buf1
        acall   wr_mem
        mov     SP,#07h                 ; reset RAM
        ljmp    mulai
;
;c_dts: mov     A,#1                    ; data address for slave 1
        acall   kr_srl                  ; kirim ke serial
        acall   tgrspn                  ; tunggu respon
        mov     A,#1                    ; data address suhu
        acall   kr_srl                  ; kirim ke serial
        acall   rstcmd
;g_dts: cjne    R7,#0FFh,ad_dts
        sjmp    tg_dts
;d_dts: mov     A,R7
        mov     Dta0,A
        mov     B,#100
        div     AB
        mov     Dta1,A
        mov     A,B
        mov     B,#10
        div     AB
        mov     Dta2,A
        mov     Dta3,B
dshps0: mov     A,Dta1
        cjne    A,#0,dshps1
        mov     Dta1,#10
dshps1: mov     A,Dta2
        cjne    A,#0,dshps2
        mov     A,Dta1
        cjne    A,#10,dshps2
        mov     Dta2,#10
dshps2: acall   delays
        ret
;
;c_dtg: mov     A,#1                    ; data address for slave 1
        acall   kr_srl                  ; kirim ke serial
        acall   tgrspn                  ; tunggu respon
        mov     A,#2                    ; data adrress gas
        acall   kr_srl                  ; kirim ke serial
        acall   rstcmd
tg_dtg: cjne    R7,#0FFh,ad_dtg
        sjmp    tg_dtg
;d_dtg: mov     A,R7
        mov     Dta4,A
        mov     B,#100
        div     AB
        mov     Dta5,A
        mov     A,B
        mov     B,#10
        div     AB
        mov     Dta6,A
        mov     Dta7,B
dghps0: mov     A,Dta5
```

```
        cjne    A,#0,dghps1
        mov     Dta5,#10
dghps1: mov     A,Dta6
        cjne    A,#0,dghps2
        mov     A,Dta5
        cjne    A,#10,dghps2
        mov     Dta6,#10
dghps2: acall   delays
        ret
;
bc_sns: mov     DPTR,#shugas
        acall   line1
        mov     Hurf,#16
        acall   tulis
        acall   line2
        mov     Hurf,#16
        acall   tulis
bcsns:  acall   bc_dts                  ; baca data suhu
        acall   bc_dtg                  ; baca data gas
        mov     DPTR,#angka
        mov     P0,#0C1h
        acall   w_ins
        mov     A,Dta1
        acall   wr_chr
        mov     A,Dta2
        acall   wr_chr
        mov     A,Dta3
        acall   wr_chr
        mov     P0,#'0'
        acall   w_chr
        mov     P0,#0CAh
        acall   w_ins
        mov     A,Dta5
        acall   wr_chr
        mov     A,Dta6
        acall   wr_chr
        mov     A,Dta7
        acall   wr_chr
        mov     P0,#0DFh
        acall   w_chr
        mov     P0,#0D0h                ; buang cursor
        acall   w_ins
        jb      Tb12,bcsns
        mov     SP,#07h                 ; reset RAM
        ljmp    mulai
;
ck_bts: acall   bc_dts                  ; baca data suhu
        acall   bc_dtg                  ; baca data gas
        mov     A,Dta4                  ;\
        mov     B,Stsh                  ; | bagi data suhu dg
        div     AB                      ; | data batas suhu
        cjne    A,#0,ckbts0             ;/
        mov     Sshu,#0                 ; jika hasil=0 -> status suhu=0
        sjmp    ckbts1
ckbts0: mov     Sshu,#1                 ; jika hasil=1 -> status suhu=1
ckbts1: mov     A,Dta0                  ;\
        mov     B,Stgs                  ; | bagi data gas dg
        div     AB                      ; | data batas gas
        cjne    A,#0,ckbts2             ;/
        mov     Sgas,#0                 ; jika hasil=0 -> status gas=0
        sjmp    ckbts3
ckbts2: mov     Sgas,#1                 ; jika hasil=1 -> status gas=1
ckbts3: mov     A,Sshu
        cjne    A,#1,ckbts4
        mov     A,Sgas
        cjne    A,#1,ckbts4
        clr     Rly0
        acall   bahaya
```

```
        sjmp    ckbts5
ckbts4: setb    Rly0
ckbts5: ret
;
line1:  mov     P0,#080h
        acall   w_ins
        ret
;
line2:  mov     P0,#0C0h
        acall   w_ins
        ret
;
tulis:  clr     A
        movc    A,@A+DPTR
        mov     P0,A
        inc     DPTR
        acall   w_chr
        djnz    Hurf,tulis
        ret
;
wr_chr: movc    A,@A+DPTR
        mov     P0,A
        acall   w_chr
        ret
;
w_ins:  clr     Enbl
        clr     Rest
        acall   jeda
        setb    Enbl
        clr     Enbl
        acall   jeda
        ret
;
w_chr:  clr     Enbl
        setb    Rest
        acall   jeda
        setb    Enbl
        clr     Enbl
        acall   jeda
        ret
;
lcd_in: acall   delays
        acall   delays
        mov     P0,#03Fh
        acall   w_ins
        acall   w_ins
        mov     P0,#0Dh
        acall   w_ins
        mov     P0,#06h
        acall   w_ins
        mov     P0,#01h
        acall   w_ins
        mov     P0,#0Ch
        acall   w_ins
        acall   delays
        ret
;
srl_in: acall   delays
        setb    EA
        mov     TMOD,#20h
        mov     TH1,#0FDh
        mov     SCON,#50h
        setb    TR1
        setb    ES
        clr     Slct                    ; select RS485 receive
        acall   delays
        ret
;
```

```
kr_srl: setb    Slct                    ; select RS485 transmit
        acall   jeda
        clr     ES
        mov     SBUF,A
        jnb     TI,$
        clr     TI
        setb    ES
        clr     Slct                    ; select RS485 receive
        ret
;
rstcmd: mov     R7,#0FFh                ; reset data command
        ret
;
tgrspn: mov     Tmt0,#0
        mov     Tmt1,#0
        acall   rstcmd
tg_rsp: cjne    R7,#0FFh,ad_rsp
        djnz    Tmt0,tg_rsp
        djnz    Tmt1,tg_rsp
        acall   jrgpts
        mov     SP,#07h                 ; reset RAM
        ljmp    mulai
ad_rsp: ret
;
wt_wr:  mov     A,Wmcn
        anl     A,#wtdg
        jz      wt_wr
        ret
;
stwrmm: orl     Wmcn,#Eemn              ; 00011000b
        orl     Wmcn,#Eemw
        ret
;
enwrmm: xrl     Wmcn,#Eemw              ; 00000000b
        xrl     Wmcn,#Eemn
        ret
;
strdmm: orl     Wmcn,#Eemn              ; 00001000b
        ret
;
enrdmm: xrl     Wmcn,#Eemn              ; 00000000b
        ret
;
wr_mem: lcall   stwrmm
        mov     DPTR,#00h
        mov     A,Stsh
        movx    @DPTR,A
        lcall   wt_wr
        mov     DPTR,#01h
        mov     A,Stgs
        movx    @DPTR,A
        lcall   wt_wr
        lcall   enwrmm
        ret

rd_mem: acall   strdmm
        mov     DPTR,#00h
        movx    A,@DPTR
        mov     Stsh,A
        mov     DPTR,#01h
        movx    A,@DPTR
        mov     Stgs,A
        acall   enrdmm
        ret

tandon: jb      Lev0,tndon
        jb      Lev1,tndon
        setb    Rly1
```

```
        sjmp    tandn
tndon:  clr     Rly1
tandn:  ret
;
bahaya: mov     P0,#00
        acall   jeda
        clr     Plyl
        mov     Dly3,#20
        acall   bicara
        setb    Plyl
        ret
;
jrgpts: mov     P0,#50
        acall   jeda
        clr     Plyl
        mov     Dly3,#15
        acall   bicara
        setb    Plyl
        ret
;
jeda:   djnz    Dly0,$
        ret
;
delays: acall   jeda
        jb      Tbl0,dlys0              ; cek tekan tombol menu
        mov     R0,#0                   ; reset status main-menu
        mov     R1,#0                   ; reset status sub-menu suhu
        mov     R2,#0                   ; reset status sub-menu gas
        ljmp    mamenu
dlys0:  jb      Tbl5,dlys1              ; cek tekan tombol menu
        jnb     Tbl5,$                  ; tunggu lepas tombol kalibrasi
        ljmp    bc_sns
dlys1:  djnz    Dly1,delays
        ret
;
delayl: mov     Dly2,#20
        acall   rd_mem                  ; baca memory
dlyl:   acall   delays
        acall   ck_bts                  ; cek batas
        acall   tandon                  ; cek tandon
        djnz    Dly2,dlyl
        ret
;
bicara: acall   delays
        djnz    Dly3,bicara
        ret
;
nama:   DB      ' Radhitya Purbo '
        DB      '    0217068     '
jrusan: DB      ' Teknik Elektro '
        DB      '   ITN Malang   '
stgshu: DB      '   Batas Suhu   '
stggas: DB      '   Batas Gas    '
plhbts: DB      '  Pilih Batas   '
shugas: DB      '   Gas     Suhu '
clcppm: DB      '     ppm      C '
angka:  DB      '0123456789      '
kosong: DB      '                '
;
        end
```

```
        org     0h
        ljmp    init

        org     23h
        clr     ES
        jnb     RI,$
        clr     RI
        mov     R7,SBUF
        setb    ES
        reti

        Add0    Bit P2.0
        Add1    Bit P2.1
        Slct    Bit P3.2
        AddA    Bit P3.7
        AddB    Bit P3.6
        Addr    Equ 30h
        Dly0    Equ 31h
        Dly1    Equ 32h
        Dly2    Equ 33h

iit:    acall   srl_in          ; inisialisasi serial
        acall   rstcmd          ; reset data command

ulai:   cjne    R7,#0FFh,cek00  ; cek command = FF
        sjmp    mulai           ; yes->kembali, no->samakan address
ek00:   acall   scnadr          ; scaning address
        clr     C               ; clear flag
        mov     A,Addr          ; kurangi data address
        mov     B,R7            ; dengan data command
        subb    A,B             ; jika data sama
        cjne    A,#0,cek01      ; maka
        acall   respon          ; respon
        acall   rstcmd          ; reset data command
        sjmp    cek02           ; cek command selanjutnya
ek01:   acall   rstcmd          ; jika data tidak sama
        sjmp    mulai           ; reset data command & kembali

ek02:   cjne    R7,#01h,cek03   ; cek command = 01
        acall   rstcmd          ; reset data command
        acall   bc_shu          ; yes -> baca suhu, no -> cek ulang
        acall   kr_srl          ; kirim ke serial
        sjmp    mulai           ; kembali
ek03:   cjne    R7,#02h,cek02   ; cek command = 02
        acall   rstcmd          ; reset data command
        acall   bc_gas          ; yes -> baca gas, no -> cek ulang
        acall   kr_srl          ; kirim serial
        sjmp    mulai           ; kembali

c_shu:  clr     AddA
        clr     AddB
        acall   jeda
        mov     A,P1
        acall   jeda
        ret

c_gas:  setb    AddA
        clr     AddB
        acall   jeda
        mov     A,P1
        acall   jeda
        ret

rl_in:  acall   delays
        acall   delays
        setb    EA
        mov     TMOD,#20h
        mov     TH1,#0FDh
```

```
        mov     SCON,#50h
        setb    TR1
        setb    ES
        clr     Slct                    ; select RS485 receive
        acall   delays
        ret

-_srl:  setb    Slct                    ; select RS485 transmit
        acall   jeda
        clr     ES
        mov     SBUF,A
        jnb     TI,$
        clr     TI
        setb    ES
        clr     Slct                    ; select RS485 receive
        ret

espon:  acall   jeda
        mov     A,#0EEh                 ; data respon
        acall   kr_srl
        ret

stcmd:  mov     R7,#0FFh                ; reset data command
        ret

cnadr:  jb      Add0,scnad0
        jb      Add1,scnad0
        mov     Addr,#0
cnad0:  jnb     Add0,scnad1
        jb      Add1,scnad1
        mov     Addr,#1
cnad1:  jb      Add0,scnad2
        jnb     Add1,scnad2
        mov     Addr,#2
cnad2:  jnb     Add0,scnad3
        jnb     Add1,scnad3
        mov     Addr,#3
cnad3:  ret

eda:    djnz    Dly0,$
        ret

elays:  acall   jeda
        djnz    Dly1,delays
        ret

elay1:  mov     Dly2,#20
ly1:    acall   delays
        djnz    Dly2,dly1
        ret

        end
```

GAS SENSORS : TYPE AF30

CIGARETTE SMOKE SENSOR

DESCRIPTION:

Gas sensor made with thick film element.

FEATURES:

- Constant heater voltage
- Tight resistance tolerance
- High sensitivity
- Typical applications include air purifier

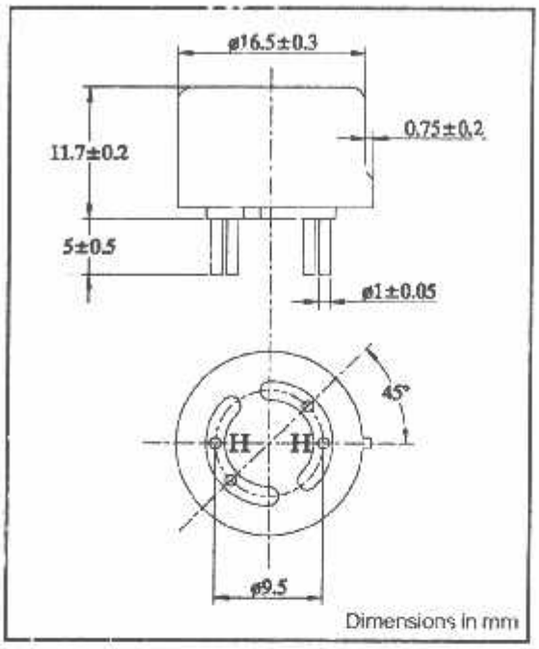
DATA:

Operating conditions:
Operating temperature ..... -10 to +55°C
Storage temperature ..... -30 to +60°C
Load Resistor R_L ..... Variable
Heater resistance ..... 27Ω (nom)
Rated power consumption P_s ..... <15mW
Rated working voltage of circuit V_c .....
..... 5V d.c. or 5V rms a.c. (max 12V)
Rated working voltage of heater .....
..... 5 ±0.2V d.c.
..... 5 ±0.2 V rms a.c.
Parts and material:
Sensing element ..... Semi-conducting oxide
Thick film heater ..... Platinum
Case ..... Nylon 66
Pin ..... Nickel alloy
Flame arrestor .....
... Double 100-mesh stainless gauze (SUS316)

Sensitivity characteristics:

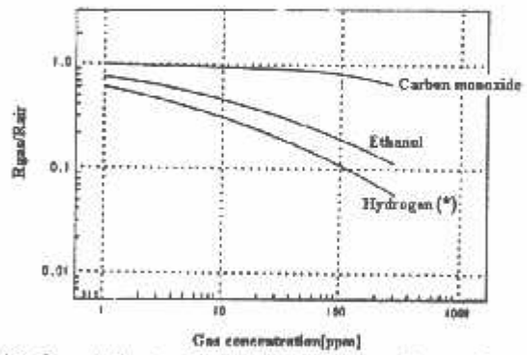
	Specification	Conditions
Sensor resistance Rgas	15k to 35k Ω	In clean air
Gas sensitivity Rgas/Rair	0.2 to 0.4	Resistance ratio at 10ppm H_2 to clean air (*)
Power consumption	535mW (max)	

DIMENSIONS:



Dimensions in mm

Typical gas sensitivity:



(*) Correlation between H_2 and cigarette smoke

Mechanical characteristics:

Test	Condition		Performance
Vibration	Frequency:	10 - 500 Hz	Should satisfy the specifications shown in the sensitivity characteristics
	Amplitude (10 - 50Hz):	2 mm	
	Acceleration (50 - 500 Hz)	10G	
	Recipricol scanning time:	5 min	
	Test time: 2 hours each for X, Y and Z directions		
Shock	Acceleration:	100G	
	Number of impacts:	5	

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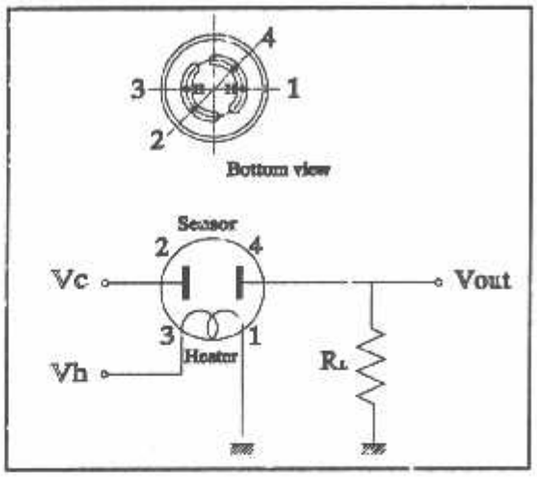
GAS SENSORS : TYPE AF30

SMOKE SENSOR

NOTES:

Pin allocation and standard test circuit:



Test conditions:

Atmosphere

Clean air at 25± 2°C and 50±5% RH without noise gas.

Circuit condition

Vc (circuit voltage)..... 5±0.05V
Vh (heater voltage)..... 5±0.05V
Preheat time..... 48 hours

Test gas

Hydrogen..... 10ppm

WARNING:

Do not use if the case or wire netting is damaged, otherwise built-in heater may cause explosions or fires.
Do not disassemble or change any parts.
Use only within specified conditions.

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National Semiconductor

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LM35
Precision Centigrade Temperature Sensors

General Description

The LM35 series are precision integrated-circuit temperature sensors, whose output voltage is linearly proportional to the Celsius (Centigrade) temperature. The LM35 thus has an advantage over linear temperature sensors calibrated in ° Kelvin, as the user is not required to subtract a large constant voltage from its output to obtain convenient Centigrade scaling. The LM35 does not require any external calibration or trimming to provide typical accuracies of ±¼°C at room temperature and ±¾°C over a full −55 to +150°C temperature range. Low cost is assured by trimming and calibration at the wafer level. The LM35's low output impedance, linear output, and precise inherent calibration make interfacing to readout or control circuitry especially easy. It can be used with single power supplies, or with plus and minus supplies. As it draws only 60 µA from its supply, it has very low self-heating, less than 0.1°C in still air. The LM35 is rated to operate over a −55° to +150°C temperature range, while the LM35C is rated for a −40° to +110°C range (−10° with improved accuracy). The LM35 series is available packaged in hermetic TO-46 transistor packages, while the LM35C, LM35CA, and LM35D are also available in the plastic TO-92 transistor package. The LM35D is also available in an 8-lead surface mount small outline package and a plastic TO-220 package.

Features

- Calibrated directly in ° Celsius (Centigrade)
- Linear + 10.0 mV/°C scale factor
- 0.5°C accuracy guaranteeable (at +25°C)
- Rated for full −55° to +150°C range
- Suitable for remote applications
- Low cost due to wafer-level trimming
- Operates from 4 to 30 volts
- Less than 60 µA current drain
- Low self-heating, 0.08°C in still air
- Nonlinearity only ±¼°C typical
- Low impedance output, 0.1 Ω for 1 mA load

Typical Applications

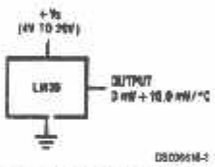
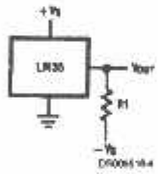


FIGURE 1. Basic Centigrade Temperature Sensor (+2°C to +150°C)



Choose $R_1 = -V_S/50\ \mu A$
$V_{OUT} = +1,500$ mV at +150°C
= +250 mV at +25°C
= −550 mV at −55°C

FIGURE 2. Full-Range Centigrade Temperature Sensor

TRI-STATE® is a registered trademark of National Semiconductor Corporation.

Connection Diagrams

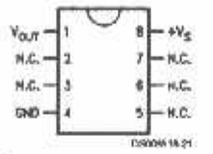
TO-46
Metal Can Package*

BOTTOM VIEW
DS006516-1

*Case is connected to negative pin (GND)

Order Number LM35H, LM35AH, LM35CH, LM35CAH or LM35DH
See NS Package Number H03H

SO-8
Small Outline Molded Package



DS006516-21

N.C. = No Connection

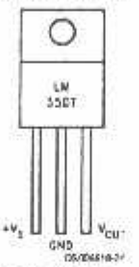
Top View
Order Number LM35DM
See NS Package Number M08A

TO-92
Plastic Package

BOTTOM VIEW
DS006516-2

Order Number LM35CZ, LM35CAZ or LM35DZ
See NS Package Number Z03A

TO-220
Plastic Package*



DS006516-24

*Tab is connected to the negative pin (GND).
Note: The LM35DT pinout is different than the discontinued LM350P.

Order Number LM35DT
See NS Package Number TA03F

Absolute Maximum Ratings (Note 10)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Supply Voltage	+35V to −0.2V
Output Voltage	+6V to −1.0V
Output Current	10 mA
Storage Temp.;	
TO-46 Package,	−60°C to +180°C
TO-92 Package,	−60°C to +150°C
SO-8 Package,	−65°C to +150°C
TO-220 Package,	−65°C to +150°C
Lead Temp.:	
TO-46 Package, (Soldering, 10 seconds)	300°C
TO-92 and TO-220 Package, (Soldering, 10 seconds)	260°C
SO Package (Note 12)	
Vapor Phase (60 seconds)	215°C
Infrared (15 seconds)	220°C
ESD Susceptibility (Note 11)	2500V
Specified Operating Temperature Range: T_{MIN} to T_{MAX} (Note 2)	
LM35, LM35A	−55°C to +150°C
LM35C, LM35CA	−40°C to +110°C
LM35D	0°C to +100°C

Electrical Characteristics

(Notes 1, 6)

Parameter	Conditions	LM35A			LM35CA			Units (Max.)
		Typical	Tested Limit (Note 4)	Design Limit (Note 5)	Typical	Tested Limit (Note 4)	Design Limit (Note 5)	
Accuracy (Note 7)	T_A=+25°C	±0.2	±0.5		±0.2	±0.5		°C
	T_A=−10°C	±0.3			±0.3		±1.0	°C
	T_A=T_{MAX}	±0.4	±1.0		±0.4	±1.0		°C
	T_A=T_{MIN}	±0.4	±1.0		±0.4		±1.5	°C
Nonlinearity (Note 8)	T_{MIN}≤T_A≤T_{MAX}	±0.18		±0.35	±0.15		±0.3	°C
Sensor Gain (Average Slope)	T_{MIN}≤T_A≤T_{MAX}	+10.0	+9.9, +10.1		+10.0		+9.9, +10.1	mV/°C
Load Regulation (Note 3) 0≤I_L≤1 mA	T_A=+25°C	±0.4	±1.0		±0.4	±1.0		mV/mA
	T_{MIN}≤T_A≤T_{MAX}	±0.5		±3.0	±0.5		±3.0	mV/mA
Line Regulation (Note 3)	T_A=+25°C	±0.01	±0.05		±0.01	±0.05		mV/V
	4V≤V_S≤30V	±0.02		±0.1	±0.02		±0.1	mV/V
Quiescent Current (Note 9)	V_S=+5V, +25°C	56	67		56	67		µA
	V_S=+5V	105		131	91		114	µA
	V_S=+30V, +25°C	56.2	68		56.2	68		µA
	V_S=+30V	105.5		133	91.5		116	µA
Change of Quiescent Current (Note 3)	4V≤V_S≤30V, +25°C	0.2	1.0		0.2	1.0		µA
	4V≤V_S≤30V	0.5		2.0	0.5		2.0	µA
Temperature Coefficient of Quiescent Current		+0.39		+0.5	+0.39		+0.5	µA/°C
Minimum Temperature for Rated Accuracy	In circuit of *Figure 1*, I_L=0	+1.5		+2.0	+1.5		+2.0	°C
Long Term Stability	T_J=T_{MAX}, for 1000 hours	±0.08			±0.08			°C

Electrical Characteristics

(Notes 1, 6)

Parameter	Conditions	LM35			LM35C, LM35D			Units (Max.)
		Typical	Tested Limit (Note 4)	Design Limit (Note 5)	Typical	Tested Limit (Note 4)	Design Limit (Note 5)	
Accuracy,	T_A=+25°C	±0.4	±1.0		±0.4	±1.0		°C
LM35, LM35C	T_A=−10°C	±0.5			±0.5		±1.5	°C
(Note 7)	T_A=T_{MAX}	±0.8	±1.5		±0.8		±1.5	°C
	T_A=T_{MIN}	±0.8		±1.5	±0.8		±2.0	°C
Accuracy, LM35D	T_A=+25°C				±0.8	±1.5		°C
(Note 7)	T_A=T_{MAX}				±0.9		±2.0	°C
	T_A=T_{MIN}				±0.9		±2.0	°C
Nonlinearity	T_{MIN}≤T_A≤T_{MAX}	**±0.3**		**±0.5**	**±0.2**		**±0.5**	°C
(Note 8)								
Sensor Gain	T_{MIN}≤T_A≤T_{MAX}	**+10.0**	**+9.8, +10.2**		**+10.0**		**+9.8, +10.2**	mV/°C
(Average Slope)								
Load Regulation	T_A=+25°C	±0.4	±2.0		±0.4	±2.0		mV/mA
(Note 3) 0≤I_L≤1 mA	T_{MIN}≤T_A≤T_{MAX}	**±0.5**		**±5.0**	**±0.5**		**±5.0**	mV/mA
Line Regulation	T_A=+25°C	±0.01	±0.1		±0.01	±0.1		mV/V
(Note 3)	4V≤V_S≤30V	**±0.02**		**±0.2**	**±0.02**		**±0.2**	mV/V
Quiescent Current	V_S=+5V, +25°C	56	80		56	80		µA
(Note 9)	V_S=+5V	**105**		**158**	**91**		**138**	µA
	V_S=+30V, +25°C	56.2	82		56.2	82		µA
	V_S=+30V	**105.5**		**161**	**91.5**		**141**	µA
Change of	4V≤V_S≤30V, +25°C	0.2	2.0		0.2	2.0		µA
Quiescent Current	4V≤V_S≤30V	**0.5**		**3.0**	**0.5**		**3.0**	µA
(Note 3)								
Temperature		**+0.39**		**+0.7**	**+0.39**		**+0.7**	µA/°C
Coefficient of								
Quiescent Current								
Minimum Temperature	In circuit of	+1.5		+2.0	+1.5		+2.0	°C
for Rated Accuracy	*Figure 1*, I_L=0							
Long Term Stability	T_J=T_{MAX}, for	±0.08			±0.08			°C
	1000 hours							

Note 1: Unless otherwise noted, these specifications apply: −55°C≤T_J≤150°C for the LM35 and LM35A; −40°≤T_J≤110°C for the LM35C and LM35CA; and 0°≤T_J≤100°C for the LM35D. V_S=+5Vdc and I_{LOAD}=50 µA, in the circuit of *Figure 2*. These specifications also apply from +2°C to T_{MAX} in the circuit of *Figure 1*. Specifications in **boldface** apply over the full rated temperature range.

Note 2: Thermal resistance of the TO-46 package is 400°C/W, junction to ambient, and 24°C/W junction to case. Thermal resistance of the TO-92 package is 180°C/W junction to ambient. Thermal resistance of the small outline molded package is 220°C/W junction to ambient. Thermal resistance of the TO-220 package is 90°C/W junction to ambient. For additional thermal resistance information see table in the Applications section.

Note 3: Regulation is measured at constant junction temperature, using pulse testing with a low duty cycle. Changes in output due to heating effects can be computed by multiplying the internal dissipation by the thermal resistance.

Note 4: Tested Limits are guaranteed and 100% tested in production.

Note 5: Design Limits are guaranteed (but not 100% production tested) over the indicated temperature and supply voltage ranges. These limits are not used to calculate outgoing quality levels.

Note 6: Specifications in **boldface** apply over the full rated temperature range.

Note 7: Accuracy is defined as the error between the output voltage and 10mV/°C times the device's case temperature, at specified conditions of voltage, current, and temperature (expressed in °C).

Note 8: Nonlinearity is defined as the deviation of the output-voltage-versus-temperature curve from the best-fit straight line, over the device's rated temperature range.

Note 9: Quiescent current is defined in the circuit of *Figure 1*.

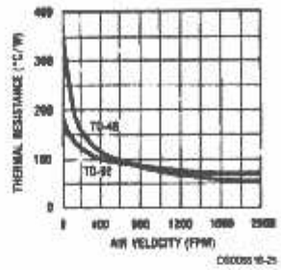
Note 10: Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. DC and AC electrical specifications do not apply when operating the device beyond its rated operating conditions. See Note 1.

Note 11: Human body model, 100 pF discharged through a 1.5 kΩ resistor.

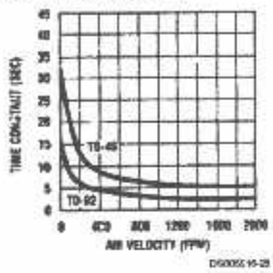
Note 12: See AN-450 "Surface Mounting Methods and Their Effect on Product Reliability" or the section titled "Surface Mount" found in a current National Semiconductor Linear Data Book for other methods of soldering surface mount devices.

Typical Performance Characteristics

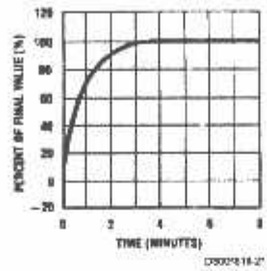
Thermal Resistance Junction to Air



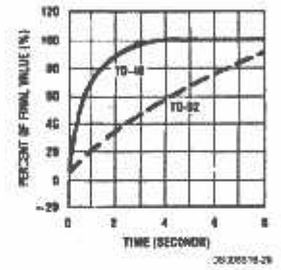
Thermal Time Constant



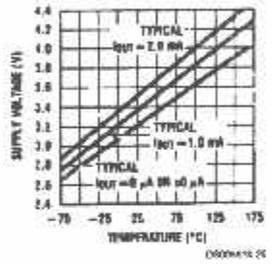
Thermal Response in Still Air



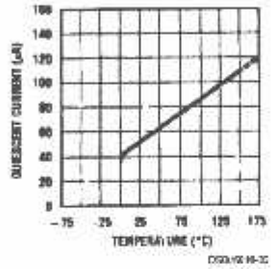
Thermal Response in Stirred Oil Bath



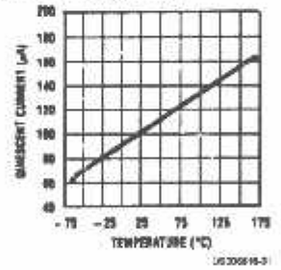
Minimum Supply Voltage vs. Temperature



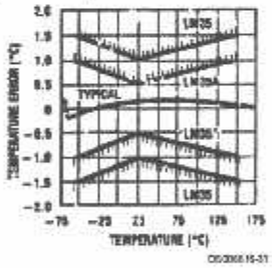
Quiescent Current vs. Temperature (In Circuit of *Figure 1.*)



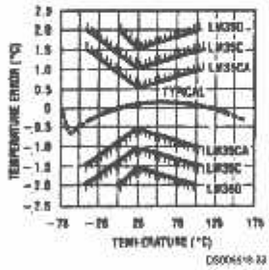
Quiescent Current vs. Temperature (In Circuit of *Figure 2.*)



Accuracy vs. Temperature (Guaranteed)

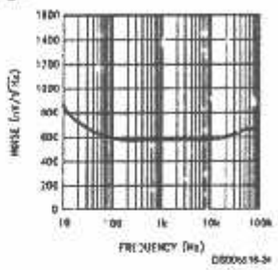


Accuracy vs. Temperature (Guaranteed)

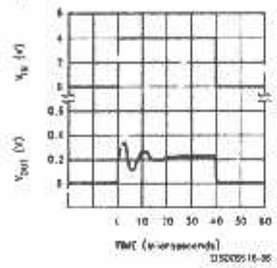


Typical Performance Characteristics (Continued)

Noise Voltage



Start-Up Response



Applications

The LM35 can be applied easily in the same way as other integrated-circuit temperature sensors. It can be glued or cemented to a surface and its temperature will be within about 0.01°C of the surface temperature.

This presumes that the ambient air temperature is almost the same as the surface temperature; if the air temperature were much higher or lower than the surface temperature, the actual temperature of the LM35 die would be at an intermediate temperature between the surface temperature and the air temperature. This is especially true for the TO-92 plastic package, where the copper leads are the principal thermal path to carry heat into the device, so its temperature might be closer to the air temperature than to the surface temperature.

To minimize this problem, be sure that the wiring to the LM35, as it leaves the device, is held at the same temperature as the surface of interest. The easiest way to do this is to cover up these wires with a bead of epoxy which will insure that the leads and wires are all at the same temperature as the surface, and that the LM35 die's temperature will not be affected by the air temperature.

The TO-46 metal package can also be soldered to a metal surface or pipe without damage. Of course, in that case the V− terminal of the circuit will be grounded to that metal. Alternatively, the LM35 can be mounted inside a sealed-end metal tube, and can then be dipped into a bath or screwed into a threaded hole in a tank. As with any IC, the LM35 and accompanying wiring and circuits must be kept insulated and dry, to avoid leakage and corrosion. This is especially true if the circuit may operate at cold temperatures where condensation can occur. Printed-circuit coatings and varnishes such as Humiseal and epoxy paints or dips are often used to insure that moisture cannot corrode the LM35 or its connections.

These devices are sometimes soldered to a small light-weight heat fin, to decrease the thermal time constant and speed up the response in slowly-moving air. On the other hand, a small thermal mass may be added to the sensor, to give the steadiest reading despite small deviations in the air temperature.

Temperature Rise of LM35 Due To Self-heating (Thermal Resistance, θ_{JA})

	TO-46, no heat sink	TO-46*, small heat fin	TO-92, no heat sink	TO-92**, small heat fin	SO-8 no heat sink	SO-8** small heat fin	TO-220 no heat sink
Still air	400°C/W	100°C/W	180°C/W	140°C/W	220°C/W	110°C/W	90°C/W
Moving air	100°C/W	40°C/W	90°C/W	70°C/W	105°C/W	90°C/W	26°C/W
Still oil	100°C/W	40°C/W	90°C/W	70°C/W			
Stirred oil	50°C/W	30°C/W	45°C/W	40°C/W			
(Clamped to metal, infinite heat sink)	(24°C/W)				(55°C/W)		

*Wakefield type 201, or 1" disc of 0.020" sheet brass, soldered to case, or similar.
**TO-92 and SO-8 package glued and leads soldered to 1" square of 1/16" printed circuit board with 2 oz. foil or similar.

Typical Applications

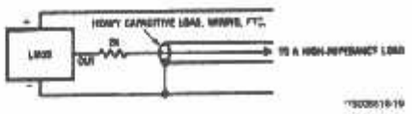


FIGURE 3. LM35 with Decoupling from Capacitive Load

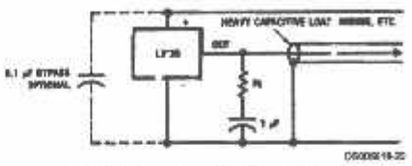


FIGURE 4. LM35 with R-C Damper

CAPACITIVE LOADS

Like most micropower circuits, the LM35 has a limited ability to drive heavy capacitive loads. The LM35 by itself is able to drive 50 pF without special precautions. If heavier loads are anticipated, it is easy to isolate or decouple the load with a resistor; see *Figure 3*. Or you can improve the tolerance of capacitance with a series R-C damper from output to ground; see *Figure 4*.

When the LM35 is applied with a 200Ω load resistor as shown in *Figure 5*, *Figure 6* or *Figure 8* it is relatively immune to wiring capacitance because the capacitance forms a bypass from ground to input, not on the output. However, as with any linear circuit connected to wires in a hostile environment, its performance can be affected adversely by intense electromagnetic sources such as relays, radio transmitters, motors with arcing brushes, SCR transients, etc, as its wiring can act as a receiving antenna and its internal junctions can act as rectifiers. For best results in such cases, a bypass capacitor from V_{IN} to ground and a series R-C damper such as 75Ω in series with 0.2 or 1 µF from output to ground are often useful. These are shown in *Figure 13*, *Figure 14*, and *Figure 16*.

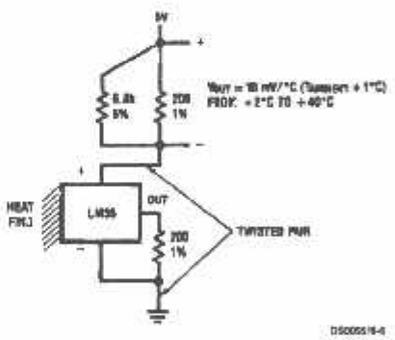


FIGURE 5. Two-Wire Remote Temperature Sensor (Grounded Sensor)

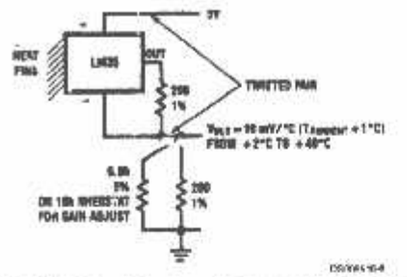


FIGURE 6. Two-Wire Remote Temperature Sensor (Output Referred to Ground)

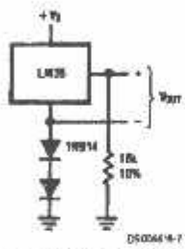


FIGURE 7. Temperature Sensor, Single Supply, −55° to +150°C

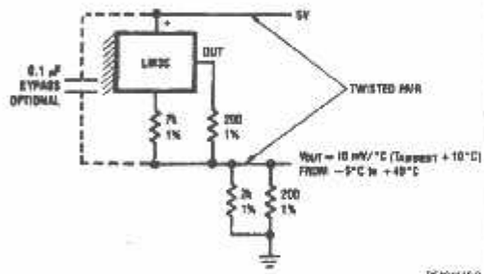


FIGURE 8. Two-Wire Remote Temperature Sensor (Output Referred to Ground)

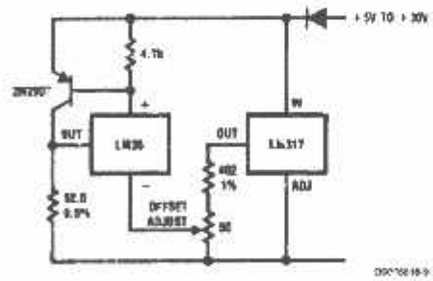


FIGURE 9. 4-To-20 mA Current Source (0°C to +100°C)

Typical Applications (Continued)

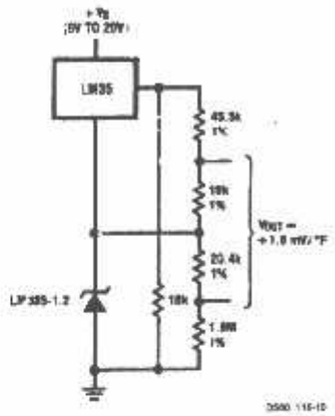


FIGURE 10. Fahrenheit Thermometer

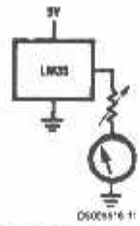


FIGURE 11. Centigrade Thermometer (Analog Meter)

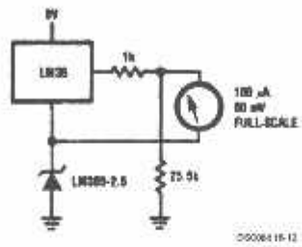


FIGURE 12. Fahrenheit ThermometerExpanded Scale Thermometer
(50° to 80° Fahrenheit, for Example Shown)

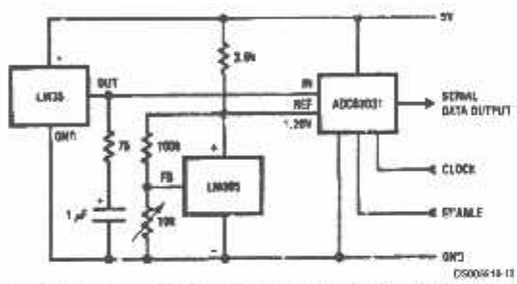


FIGURE 13. Temperature To Digital Converter (Serial Output) (+128°C Full Scale)

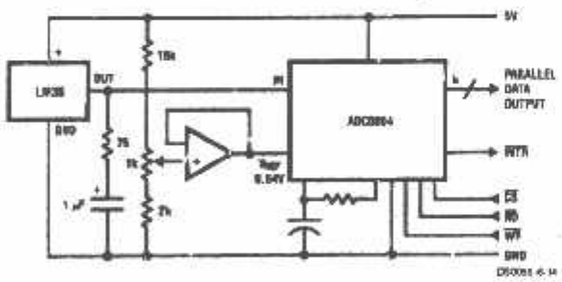
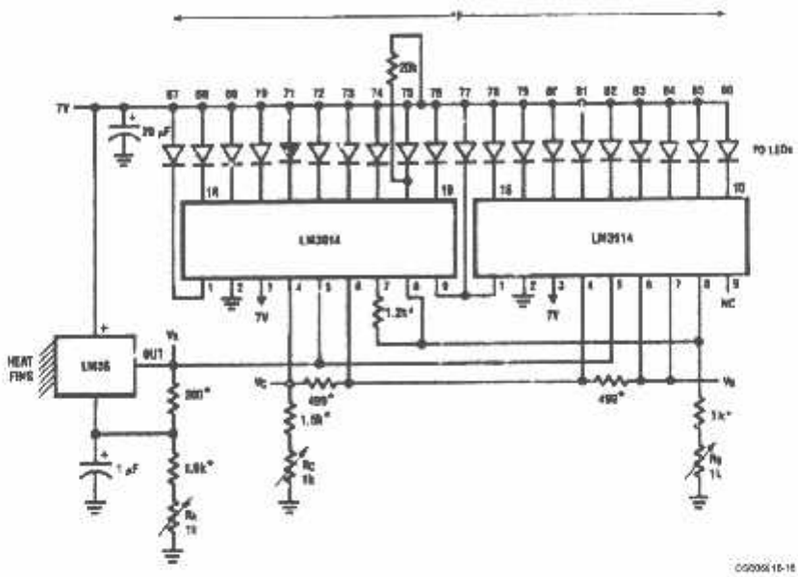


FIGURE 14. Temperature To Digital Converter (Parallel TRI-STATE™ Outputs for Standard Data Bus to µP Interface) (128°C Full Scale)

Typical Applications (Continued)



*= 1% or 2% film resistor
Trim R_B for V_B=3.075V
Trim R_C for V_C=1.965V
Trim R_A for V_A=0.075V + 100mV/°C x $T_{ambient}$
Example, V_A=2.275V at 22°C

FIGURE 15. Bar-Graph Temperature Display (Dot Mode)

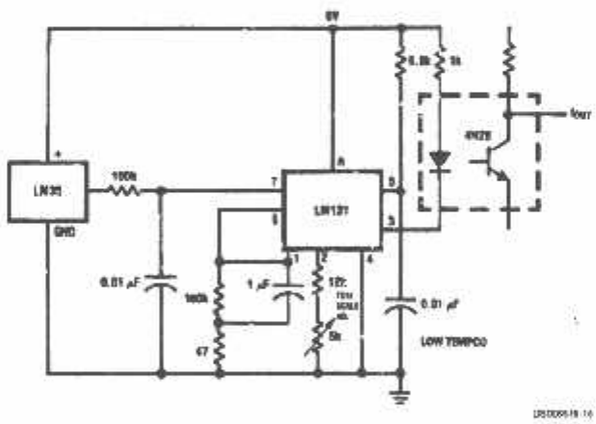
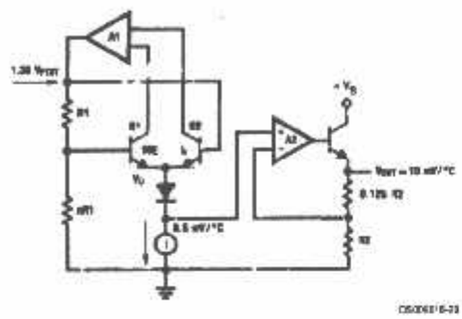
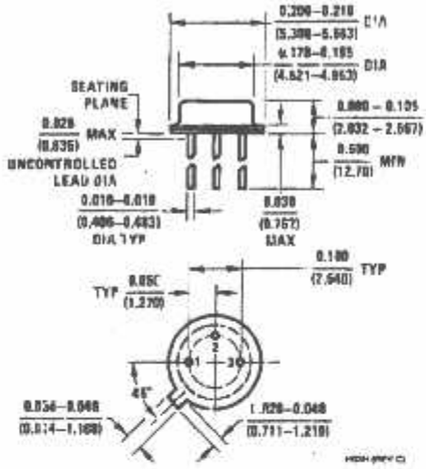


FIGURE 16. LM35 With Voltage-To-Frequency Converter And Isolated Output (2°C to +150°C; 20 Hz to 1500 Hz)

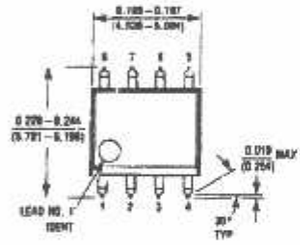
Block Diagram

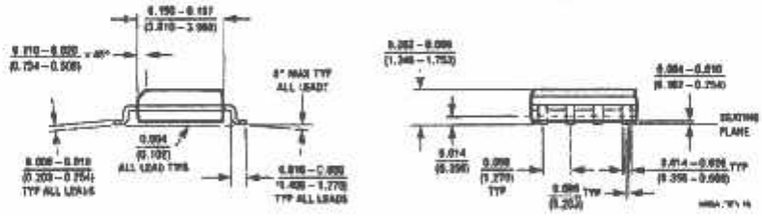


Physical Dimensions Inches (millimeters) unless otherwise noted



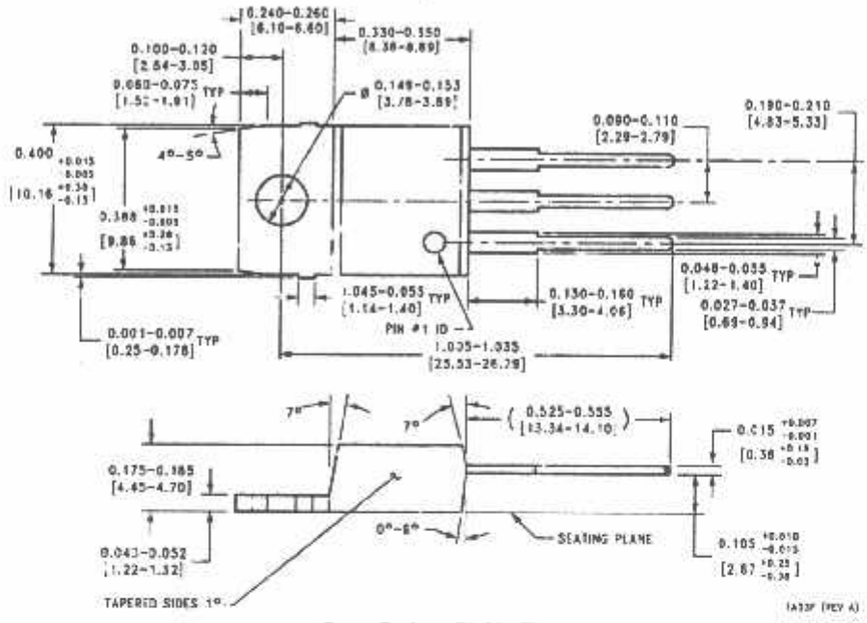
TO-46 Metal Can Package (H)
Order Number LM35AH, LM35CH, LM35CAH, or LM35DH
NS Package Number H03H



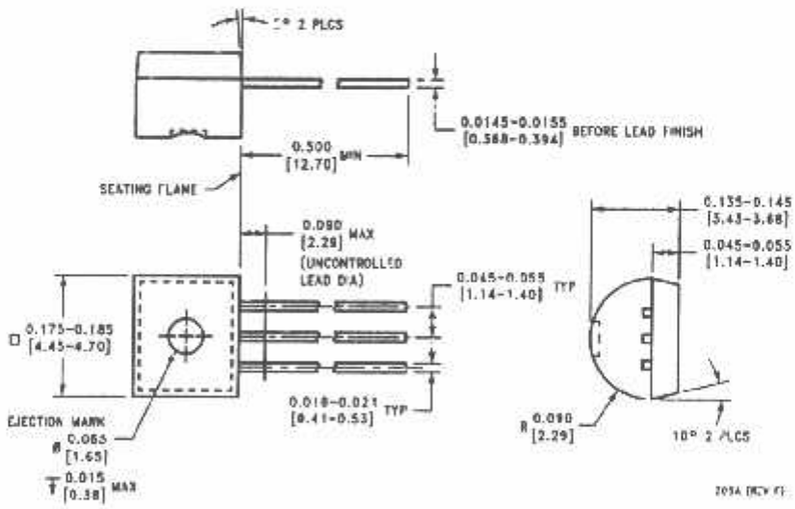


SO-8 Molded Small Outline Package (M)
Order Number LM35DM
NS Package Number M08A

Physical Dimensions inches (millimeters) unless otherwise noted (Continued)



Power Package TO-220 (T)
Order Number LM35DT
NS Package Number TA03F



TO-92 Plastic Package (Z)
Order Number LM35CZ, LM35CAZ or LM35DZ
NS Package Number Z03A

Notes

LIFE SUPPORT POLICY

NATIONAL'S PRODUCTS ARE NOT AUTHORIZED FOR USE AS CRITICAL COMPONENTS IN LIFE SUPPORT DEVICES OR SYSTEMS WITHOUT THE EXPRESS WRITTEN APPROVAL OF THE PRESIDENT AND GENERAL COUNSEL OF NATIONAL SEMICONDUCTOR CORPORATION. As used herein:

1. Life support devices or systems are devices or systems which, (a) are intended for surgical implant into the body, or (b) support or sustain life, and whose failure to perform when properly used in accordance with instructions for use provided in the labeling, can be reasonably expected to result in a significant injury to the user.
2. A critical component is any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

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19-0122; Rev 6; 10/01

MAXIM

Low-Power, Slew-Rate-Limited RS-485/RS-422 Transceivers

General Description

The MAX481, MAX483, MAX485, MAX487–MAX491, and MAX1487 are low-power transceivers for RS-485 and RS-422 communication. Each part contains one driver and one receiver. The MAX483, MAX487, MAX488, and MAX489 feature reduced slew-rate drivers that minimize EMI and reduce reflections caused by improperly terminated cables, thus allowing error-free data transmission up to 250kbps. The driver slew rates of the MAX481, MAX485, MAX490, MAX491, and MAX1487 are not limited, allowing them to transmit up to 2.5Mbps.

These transceivers draw between 120µA and 500µA of supply current when unloaded or fully loaded with disabled drivers. Additionally, the MAX481, MAX483, and MAX487 have a low-current shutdown mode in which they consume only 0.1µA. All parts operate from a single 5V supply.

Drivers are short-circuit current limited and are protected against excessive power dissipation by thermal shutdown circuitry that places the driver outputs into a high-impedance state. The receiver input has a fail-safe feature that guarantees a logic-high output if the input is open circuit.

The MAX487 and MAX1487 feature quarter-unit-load receiver input impedance, allowing up to 128 MAX487/MAX1487 transceivers on the bus. Full-duplex communications are obtained using the MAX488–MAX491, while the MAX481, MAX483, MAX485, MAX487, and MAX1487 are designed for half-duplex applications.

Applications

Low-Power RS-485 Transceivers

Low-Power RS-422 Transceivers

Level Translators

Transceivers for EMI-Sensitive Applications

Industrial-Control Local Area Networks

Features

- **In µMAX Package: Smallest 8-Pin SO**
- **Slew-Rate Limited for Error-Free Data Transmission (MAX483/487/488/489)**
- **0.1µALow-Current Shutdown Mode (MAX481/483/487)**
- **Low Quiescent Current:**
  120µA (MAX483/487/488/489)
  230µA (MAX1487)
  300µA (MAX481/485/490/491)
- **-7V to +12V Common-Mode Input Voltage Range**
- **Three-State Outputs**
- **30ns Propagation Delays, 5ns Skew (MAX481/485/490/491/1487)**
- **Full-Duplex and Half-Duplex Versions Available**
- **Operate from a Single 5V Supply**
- **Allows up to 128 Transceivers on the Bus (MAX487/MAX1487)**
- **Current-Limiting and Thermal Shutdown for Driver Overload Protection**

Ordering Information

PART	TEMP. RANGE	PIN-PACKAGE
MAX481CPA	0°C to +70°C	8 Plastic DIP
MAX481CSA	0°C to +70°C	8 SO
MAX481CUA	0°C to +70°C	8 µMAX
MAX481C/D	0°C to +70°C	Dice*

Ordering Information continued at end of data sheet.

**Contact factory for dice specifications.*

Selection Table

PART NUMBER	HALF/FULL DUPLEX	DATA RATE (Mbps)	SLEW-RATE LIMITED	LOW-POWER SHUTDOWN	RECEIVER/ DRIVER ENABLE	QUIESCENT CURRENT (µA)	NUMBER OF TRANSMITTERS ON BUS	PIN COUNT
MAX481	Half	2.5	No	Yes	Yes	300	32	8
MAX483	Half	0.25	Yes	Yes	Yes	120	32	8
MAX485	Half	2.5	No	No	Yes	300	32	8
MAX487	Half	0.25	Yes	Yes	Yes	120	128	8
MAX488	Full	0.25	Yes	No	No	120	32	8
MAX489	Full	0.25	Yes	No	Yes	120	32	14
MAX490	Full	2.5	No	No	No	300	32	8
MAX491	Full	2.5	No	No	Yes	300	32	14
MAX1487	Half	2.5	No	No	Yes	230	128	8

Low-Power, Slew-Rate-Limited RS-485/RS-422 Transceivers

ABSOLUTE MAXIMUM RATINGS

Supply Voltage (V_{CC}) 12V
Control Input Voltage ($\overline{RE}$, DE) ..... -0.5V to (V_{CC} + 0.5V)
Driver Input Voltage (DI) ..... -0.5V to (V_{CC} + 0.5V)
Driver Output Voltage (A, B) ..... -8V to +12.5V
Receiver Input Voltage (A, B) ..... -8V to +12.5V
Receiver Output Voltage (RO) ..... -0.5V to (V_{CC} +0.5V)
Continuous Power Dissipation (T_A = +70°C)
8-Pin Plastic DIP (derate 9.09mW/°C above +70°C) 727mW
14-Pin Plastic DIP (derate 10.00mW/°C above +70°C) ..800mW
8-Pin SO (derate 5.88mW/°C above +70°C) 471mW
14-Pin SO (derate 8.33mW/°C above +70°C) 667mW
8-Pin µMAX (derate 4.10mW/°C above +70°C) 830mW
8-Pin CERDIP (derate 8.00mW/°C above +70°C) 640mW
14-Pin CERDIP (derate 9.09mW/°C above +70°C) 727mW
Operating Temperature Ranges
MAX4_ _C_ _/MAX1487C_A ..... 0°C to +70°C
MAX4_ _E_ _/MAX1487E_A ..... -40°C to +85°C
MAX4_ _MJ_/MAX1487MJA ..... -55°C to +125°C
Storage Temperature Range ..... -65°C to +160°C
Lead Temperature (soldering, 10sec) ..... +300°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC ELECTRICAL CHARACTERISTICS

(V_{CC} = 5V ±5%, T_A = T_{MIN} to T_{MAX}, unless otherwise noted.) (Notes 1, 2)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Differential Driver Output (no load)	V_{OD1}					5	V
Differential Driver Output (with load)	V_{OD2}	R = 50Ω (RS-422)		2			V
		R = 27Ω (RS-485), Figure 4		1.5		5	
Change in Magnitude of Driver Differential Output Voltage for Complementary Output States	ΔV_{OD}	R = 27Ω or 50Ω, Figure 4				0.2	V
Driver Common-Mode Output Voltage	V_{OC}	R = 27Ω or 50Ω, Figure 4				3	V
Change in Magnitude of Driver Common-Mode Output Voltage for Complementary Output States	ΔV_{OD}	R = 27Ω or 50Ω, Figure 4				0.2	V
Input High Voltage	V_{IH}	DE, DI, $\overline{RE}$		2.0			V
Input Low Voltage	V_{IL}	DE, DI, $\overline{RE}$				0.8	V
Input Current	I_{IN1}	DE, DI, $\overline{RE}$				±2	µA
Input Current (A, B)	I_{IN2}	DE = 0V; V_{CC} = 0V or 5.25V, all devices except MAX487/MAX1487	V_{IN} = 12V			1.0	mA
			V_{IN} = -7V			-0.8	
		MAX487/MAX1487, DE = 0V, V_{CC} = 0V or 5.25V	V_{IN} = 12V			0.25	mA
			V_{IN} = -7V			-0.2	
Receiver Differential Threshold Voltage	V_{TH}	-7V ≤ V_{CM} ≤ 12V		-0.2		0.2	V
Receiver Input Hysteresis	ΔV_{TH}	V_{CM} = 0V			70		mV
Receiver Output High Voltage	V_{OH}	I_O = -4mA, V_{ID} = 200mV		3.5			V
Receiver Output Low Voltage	V_{OL}	I_O = 4mA, V_{ID} = -200mV				0.4	V
Three-State (high impedance) Output Current at Receiver	I_{OZR}	0.4V ≤ V_O ≤ 2.4V				±1	µA
Receiver Input Resistance	R_{IN}	-7V ≤ V_{CM} ≤ 12V, all devices except MAX487/MAX1487		12			kΩ
		-7V ≤ V_{CM} ≤ 12V, MAX487/MAX1487		48			kΩ

DC ELECTRICAL CHARACTERISTICS (continued)

(V_{CC} = 5V ±5%, T_A = T_{MIN} to T_{MAX}, unless otherwise noted) (Notes 1, 2)

PARAMETER	SYMBOL	CONDITIONS			MIN	TYP	MAX	UNITS
No-Load Supply Current (Note 3)	I_{CC}	MAX488/MAX489, DE, DI, $\overline{RE}$ = 0V or V_{CC}				120	250	µA
		MAX490/MAX491, DE, DI, $\overline{RE}$ = 0V or V_{CC}				300	500	
		MAX481/MAX485, $\overline{RE}$ = 0V or V_{CC}	DE = V_{CC}			500	900	
			DE = 0V			300	500	
		MAX1487, $\overline{RE}$ = 0V or V_{CC}	DE = V_{CC}			300	500	
			DE = 0V			230	400	
		MAX483/MAX487, $\overline{RE}$ = 0V or V_{CC}	DE = 5V	MAX483		350	650	
				MAX487		250	400	
			DE = 0V			120	250	
Supply Current in Shutdown	I_{SHDN}	MAX481/483/487, DE = 0V, $\overline{RE}$ = V_{CC}				0.1	10	µA
Driver Short-Circuit Current, V_O = High	I_{OSD1}	-7V ≤ V_O ≤12V (Note 4)			35		250	mA
Driver Short-Circuit Current, V_O = Low	I_{OSD2}	-7V ≤ V_O ≤12V (Note 4)			35		250	mA
Receiver Short-Circuit Current	I_{OSR}	0V ≤ V_O ≤ V_{CC}			7		95	mA

SWITCHING CHARACTERISTICS—MAX481/MAX485, MAX490/MAX491, MAX1487

(V_{CC} = 5V ±5%, T_A = T_{MIN} to T_{MAX}, unless otherwise noted.) (Notes 1, 2)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Driver Input to Output	t_{PLH}	Figures 6 and 8, R_{DIFF} = 54Ω, C_{L1} = C_{L2} = 100pF		10	30	60	ns
	t_{PHL}			10	30	60	
Driver Output Skew to Output	t_{SKEW}	Figures 6 and 8, R_{DIFF} = 54Ω, C_{L1} = C_{L2} = 100pF			5	10	ns
Driver Rise or Fall Time	t_R, t_F	Figures 6 and 8, R_{DIFF} = 54Ω, C_{L1} = C_{L2} = 100pF	MAX481, MAX485, MAX1487	3	15	40	ns
			MAX490C/E, MAX491C/E	5	15	25	
			MAX490M, MAX491M	3	15	40	
Driver Enable to Output High	t_{ZH}	Figures 7 and 9, C_L = 100pF, S2 closed			40	70	ns
Driver Enable to Output Low	t_{ZL}	Figures 7 and 9, C_L = 100pF, S1 closed			40	70	ns
Driver Disable Time from Low	t_{LZ}	Figures 7 and 9, C_L = 15pF, S1 closed			40	70	ns
Driver Disable Time from High	t_{HZ}	Figures 7 and 9, C_L = 15pF, S2 closed			40	70	ns
Receiver Input to Output	t_{PLH}, t_{PHL}	Figures 6 and 10, R_{DIFF} = 54Ω, C_{L1} = C_{L2} = 100pF	MAX481, MAX485, MAX1487	20	90	200	ns
			MAX490C/E, MAX491C/E	20	90	150	
			MAX490M, MAX491M	20	90	200	
$\lvert t_{PLH} - t_{PHL} \rvert$ Differential Receiver Skew	t_{SKD}	Figures 6 and 10, R_{DIFF} = 54Ω, C_{L1} = C_{L2} = 100pF			13		ns
Receiver Enable to Output Low	t_{ZL}	Figures 5 and 11, C_{RL} = 15pF, S1 closed			20	50	ns
Receiver Enable to Output High	t_{ZH}	Figures 5 and 11, C_{RL} = 15pF, S2 closed			20	50	ns
Receiver Disable Time from Low	t_{LZ}	Figures 5 and 11, C_{RL} = 15pF, S1 closed			20	50	ns
Receiver Disable Time from High	t_{HZ}	Figures 5 and 11, C_{RL} = 15pF, S2 closed			20	50	ns
Maximum Data Rate	f_{MAX}			2.5			Mbps
Time to Shutdown	t_{SHDN}	MAX481 (Note 5)		50	200	600	ns

Low-Power, Slew-Rate-Limited RS-485/RS-422 Transceivers

SWITCHING CHARACTERISTICS—MAX481/MAX485, MAX490/MAX491, MAX1487 (continued)

(V_{CC} = 5V ±5%, T_A = T_{MIN} to T_{MAX}, unless otherwise noted.) (Notes 1, 2)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Driver Enable from Shutdown to Output High (MAX481)	$t_{ZH(SHDN)}$	Figures 7 and 9, C_L = 100pF, S2 closed		40	100	ns
Driver Enable from Shutdown to Output Low (MAX481)	$t_{ZL(SHDN)}$	Figures 7 and 9, C_L = 100pF, S1 closed		40	100	ns
Receiver Enable from Shutdown to Output High (MAX481)	$t_{ZH(SHDN)}$	Figures 5 and 11, C_L = 15pF, S2 closed, A - B = 2V		300	1000	ns
Receiver Enable from Shutdown to Output Low (MAX481)	$t_{ZL(SHDN)}$	Figures 5 and 11, C_L = 15pF, S1 closed, B - A = 2V		300	1000	ns

SWITCHING CHARACTERISTICS—MAX483, MAX487/MAX488/MAX489

(V_{CC} = 5V ±5%, T_A = T_{MIN} to T_{MAX}, unless otherwise noted.) (Notes 1, 2)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Driver Input to Output	t_{PLH}	Figures 6 and 8, R_{DIFF} = 54Ω, C_{L1} = C_{L2} = 100pF	250	800	2000	ns
	t_{PHL}		250	800	2000	
Driver Output Skew to Output	t_{SKEW}	Figures 6 and 8, R_{DIFF} = 54Ω, C_{L1} = C_{L2} = 100pF		100	800	ns
Driver Rise or Fall Time	t_R, t_F	Figures 6 and 8, R_{DIFF} = 54Ω, C_{L1} = C_{L2} = 100pF	250		2000	ns
Driver Enable to Output High	t_{ZH}	Figures 7 and 9, C_L = 100pF, S2 closed	250		2000	ns
Driver Enable to Output Low	t_{ZL}	Figures 7 and 9, C_L = 100pF, S1 closed	250		2000	ns
Driver Disable Time from Low	t_{LZ}	Figures 7 and 9, C_L = 15pF, S1 closed	300		3000	ns
Driver Disable Time from High	t_{HZ}	Figures 7 and 9, C_L = 15pF, S2 closed	300		3000	ns
Receiver Input to Output	t_{PLH}	Figures 6 and 10, R_{DIFF} = 54Ω, C_{L1} = C_{L2} = 100pF	250		2000	ns
	t_{PHL}		250		2000	
$\lvert t_{PLH} - t_{PHL} \rvert$ Differential Receiver Skew	t_{SKD}	Figures 6 and 10, R_{DIFF} = 54Ω, C_{L1} = C_{L2} = 100pF		100		ns
Receiver Enable to Output Low	t_{ZL}	Figures 5 and 11, C_{RL} = 15pF, S1 closed		20	50	ns
Receiver Enable to Output High	t_{ZH}	Figures 5 and 11, C_{RL} = 15pF, S2 closed		20	50	ns
Receiver Disable Time from Low	t_{LZ}	Figures 5 and 11, C_{RL} = 15pF, S1 closed		20	50	ns
Receiver Disable Time from High	t_{HZ}	Figures 5 and 11, C_{RL} = 15pF, S2 closed		20	50	ns
Maximum Data Rate	f_{MAX}	t_{PLH}, t_{PHL} < 50% of data period	250			kbps
Time to Shutdown	t_{SHDN}	MAX483/MAX487 (Note 5)	50	200	600	ns
Driver Enable from Shutdown to Output High	$t_{ZH(SHDN)}$	MAX483/MAX487, Figures 7 and 9, C_L = 100pF, S2 closed			2000	ns
Driver Enable from Shutdown to Output Low	$t_{ZL(SHDN)}$	MAX483/MAX487, Figures 7 and 9, C_L = 100pF, S1 closed			2000	ns
Receiver Enable from Shutdown to Output High	$t_{ZH(SHDN)}$	MAX483/MAX487, Figures 5 and 11, C_L = 15pF, S2 closed			2500	ns
Receiver Enable from Shutdown to Output Low	$t_{ZL(SHDN)}$	MAX483/MAX487, Figures 5 and 11, C_L = 15pF, S1 closed			2500	ns

NOTES FOR ELECTRICAL/SWITCHING CHARACTERISTICS

Note 1: All currents into device pins are positive; all currents out of device pins are negative. All voltages are referenced to device ground unless otherwise specified.

Note 2: All typical specifications are given for V_{CC} = 5V and T_A = +25°C.

Note 3: Supply current specification is valid for loaded transmitters when DE = 0V.

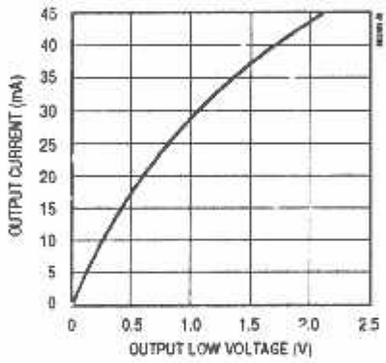
Note 4: Applies to peak current. See *Typical Operating Characteristics*.

Note 5: The MAX481/MAX483/MAX487 are put into shutdown by bringing $\overline{RE}$ high and DE low. If the inputs are in this state for less than 50ns, the parts are guaranteed not to enter shutdown. If the inputs are in this state for at least 600ns, the parts are guaranteed to have entered shutdown. See *Low-Power Shutdown Mode* section.

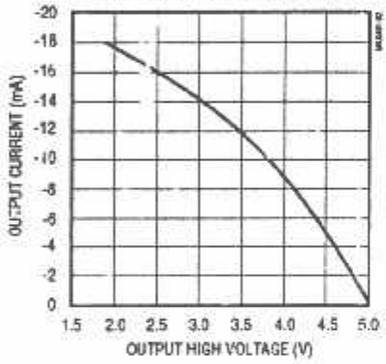
Typical Operating Characteristics

(V_{CC} = 5V, T_A = +25°C, unless otherwise noted.)

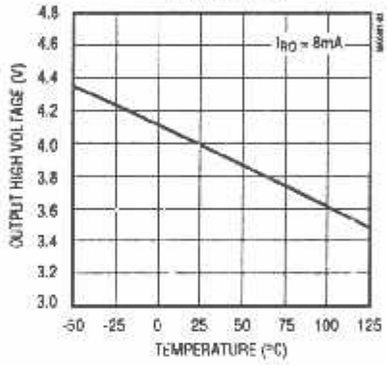
OUTPUT CURRENT vs. RECEIVER OUTPUT LOW VOLTAGE



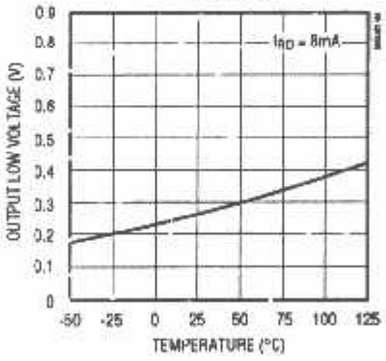
OUTPUT CURRENT vs. RECEIVER OUTPUT HIGH VOLTAGE



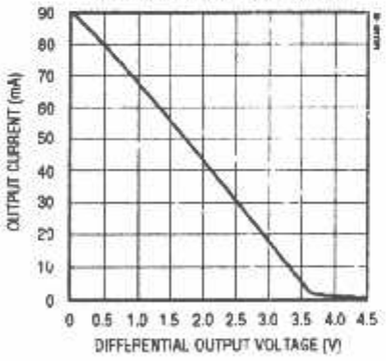
RECEIVER OUTPUT HIGH VOLTAGE vs. TEMPERATURE



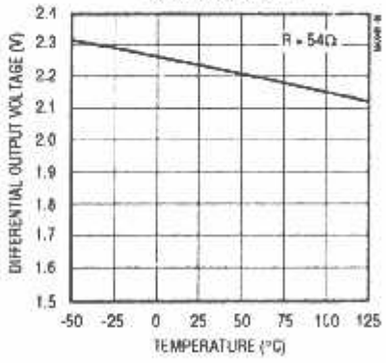
RECEIVER OUTPUT LOW VOLTAGE vs. TEMPERATURE



DRIVER OUTPUT CURRENT vs. DIFFERENTIAL OUTPUT VOLTAGE



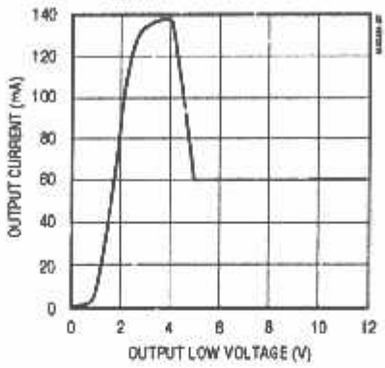
DRIVER DIFFERENTIAL OUTPUT VOLTAGE vs. TEMPERATURE



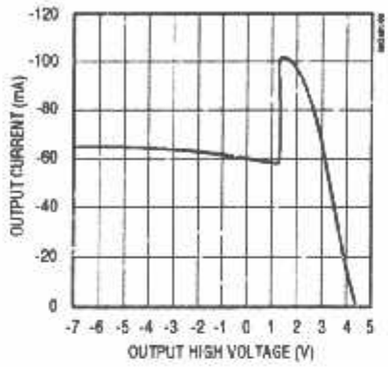
Typical Operating Characteristics (continued)

(V_{CC} = 5V, T_A = +25°C, unless otherwise noted.)

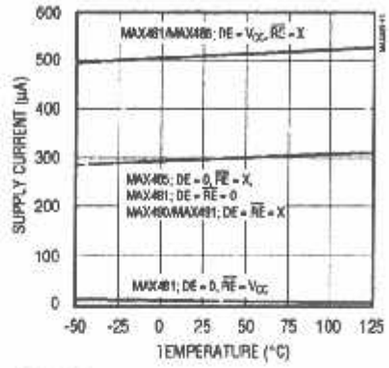
OUTPUT CURRENT vs. DRIVER OUTPUT LOW VOLTAGE



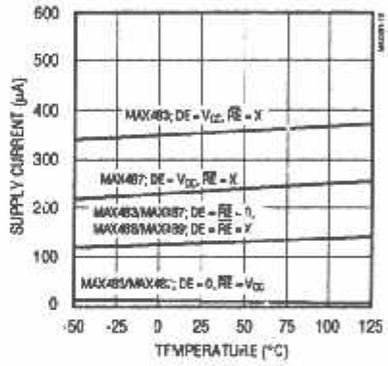
OUTPUT CURRENT vs. DRIVER OUTPUT HIGH VOLTAGE



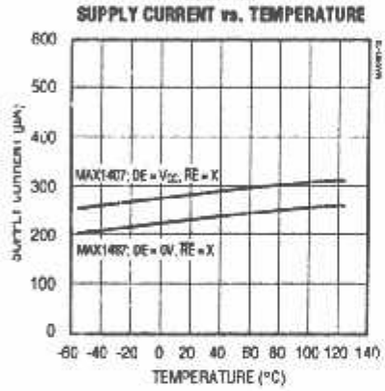
MAX481/MAX485/MAX490/MAX491 SUPPLY CURRENT vs. TEMPERATURE



MAX483/MAX487–MAX489 SUPPLY CURRENT vs. TEMPERATURE



MAX1487 SUPPLY CURRENT vs. TEMPERATURE



Pin Description

PIN					NAME	FUNCTION
MAX481/MAX483/ MAX485/MAX487/ MAX1487		MAX488/ MAX490		MAX489/ MAX491		
DIP/SO	µMAX	DIP/SO	µMAX	DIP/SO		
1	3	2	4	2	RO	Receiver Output: If A > B by 200mV, RO will be high; If A < B by 200mV, RO will be low.
2	4	—	—	3	$\overline{RE}$	Receiver Output Enable. RO is enabled when $\overline{RE}$ is low; RO is high impedance when $\overline{RE}$ is high.
3	5	—	—	4	DE	Driver Output Enable. The driver outputs, Y and Z, are enabled by bringing DE high. They are high impedance when DE is low. If the driver outputs are enabled, the parts function as line drivers. While they are high impedance, they function as line receivers if $\overline{RE}$ is low.
4	6	3	5	5	DI	Driver Input. A low on DI forces output Y low and output Z high. Similarly, a high on DI forces output Y high and output Z low.
5	7	4	6	6, 7	GND	Ground
—	—	5	7	9	Y	Noninverting Driver Output
—	—	6	8	10	Z	Inverting Driver Output
6	8	—	—	—	A	Noninverting Receiver Input and Noninverting Driver Output
—	—	8	2	12	A	Noninverting Receiver Input
7	1	—	—	—	B	Inverting Receiver Input and Inverting Driver Output
—	—	7	1	11	B	Inverting Receiver Input
8	2	1	3	14	V_{CC}	Positive Supply: 4.75V ≤ V_{CC} ≤ 5.25V
—	—	—	—	1, 8, 13	N.C.	No Connect—not internally connected

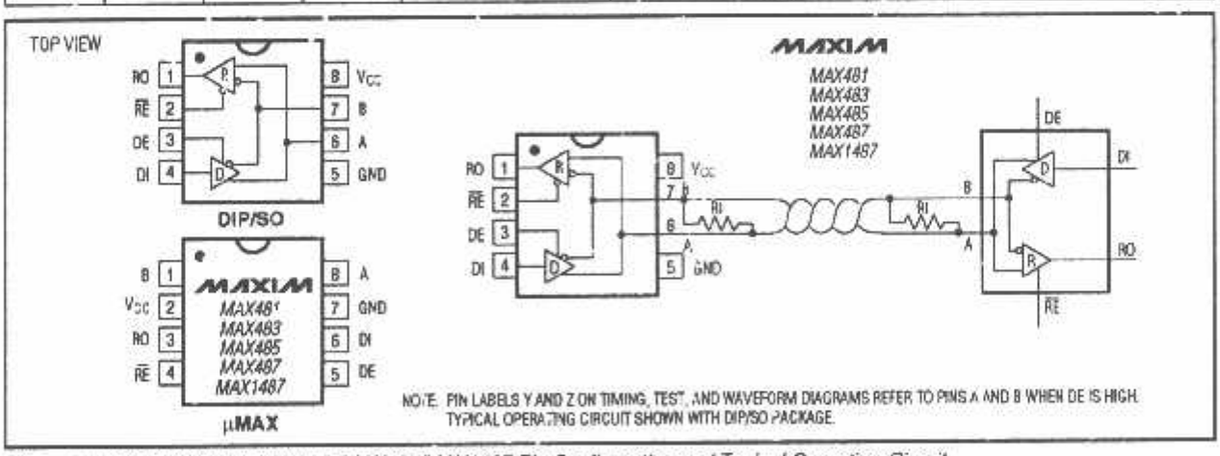


Figure 1. MAX481/MAX483/MAX485/MAX487/MAX1487 Pin Configuration and Typical Operating Circuit

Low-Power, Slew-Rate-Limited RS-485/RS-422 Transceivers

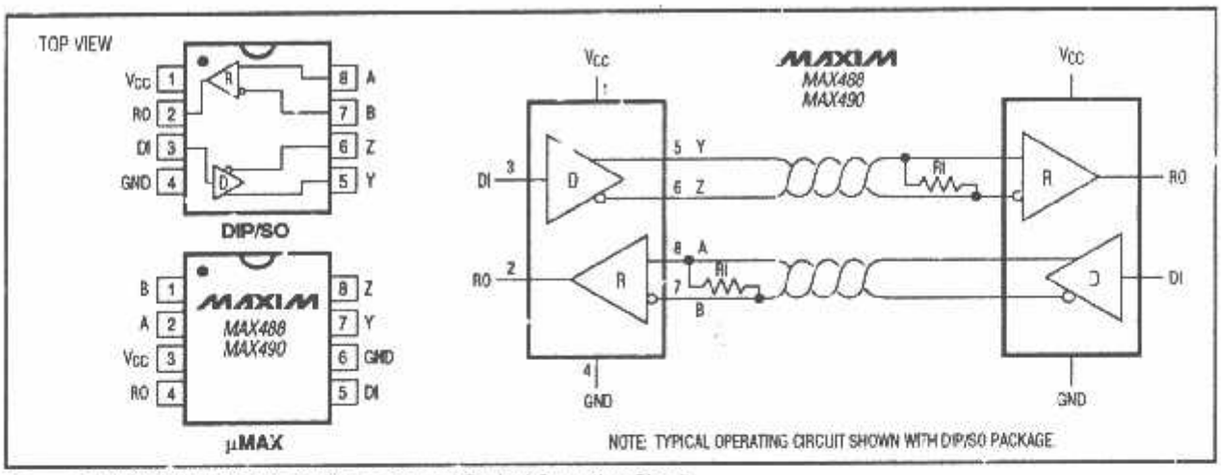


Figure 2. MAX488/MAX490 Pin Configuration and Typical Operating Circuit

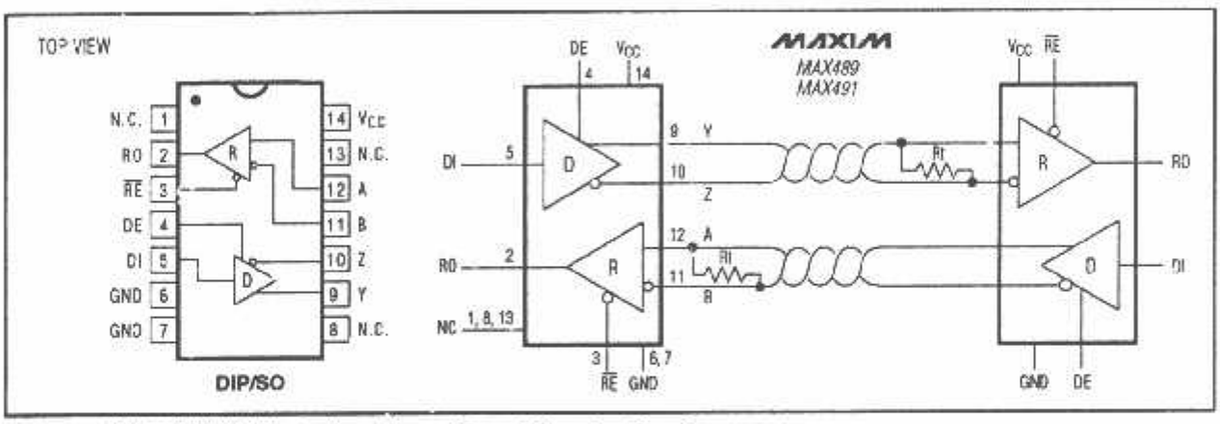


Figure 3. MAX489/MAX491 Pin Configuration and Typical Operating Circuit

Applications Information

The MAX481/MAX483/MAX485/MAX487–MAX491 and MAX1487 are low-power transceivers for RS-485 and RS-422 communications. The MAX481, MAX485, MAX490, MAX491, and MAX1487 can transmit and receive at data rates up to 2.5Mbps, while the MAX483, MAX487, MAX488, and MAX489 are specified for data rates up to 250kbps. The MAX488–MAX491 are full-duplex transceivers while the MAX481, MAX483, MAX485, MAX487, and MAX1487 are half-duplex. In addition, Driver Enable (DE) and Receiver Enable (RE) pins are included on the MAX481, MAX483, MAX485, MAX487, MAX489, MAX491, and MAX1487. When disabled, the driver and receiver outputs are high impedance.

MAX487/MAX1487: 128 Transceivers on the Bus

The 48kΩ, 1/4-unit-load receiver input impedance of the MAX487 and MAX1487 allows up to 128 transceivers on a bus, compared to the 1-unit load (12kΩ input impedance) of standard RS-485 drivers (32 transceivers maximum). Any combination of MAX487/MAX1487 and other RS-485 transceivers with a total of 32 unit loads or less can be put on the bus. The MAX481/MAX483/MAX485 and MAX488–MAX491 have standard 12kΩ Receiver Input impedance.

Test Circuits

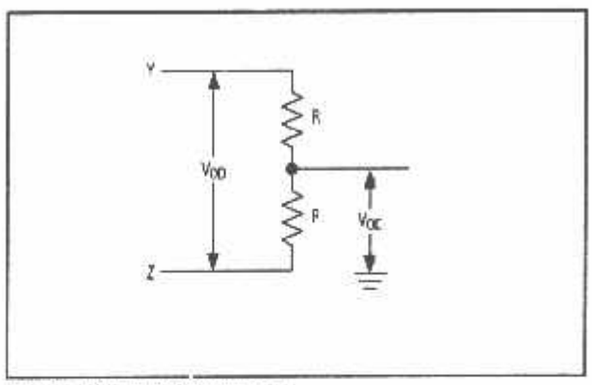


Figure 4. Driver DC Test Load

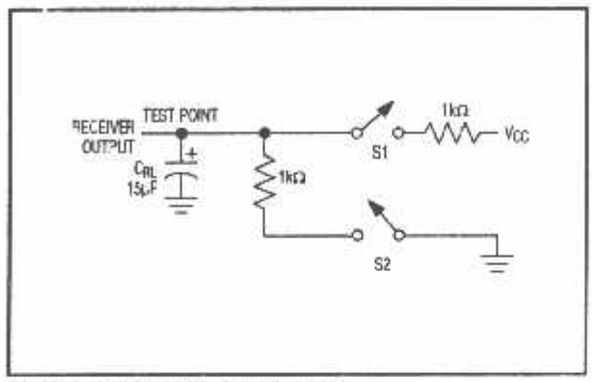


Figure 5. Receiver Timing Test Load

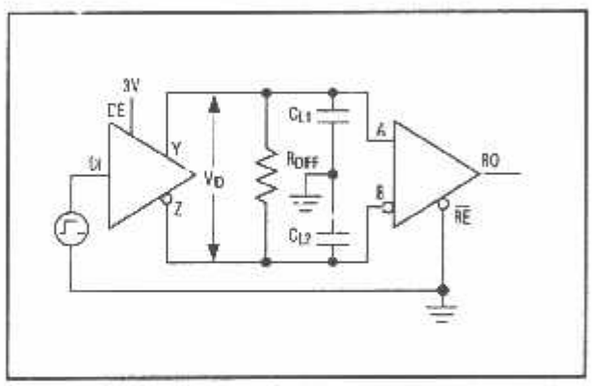


Figure 6. Driver/Receiver Timing Test Circuit

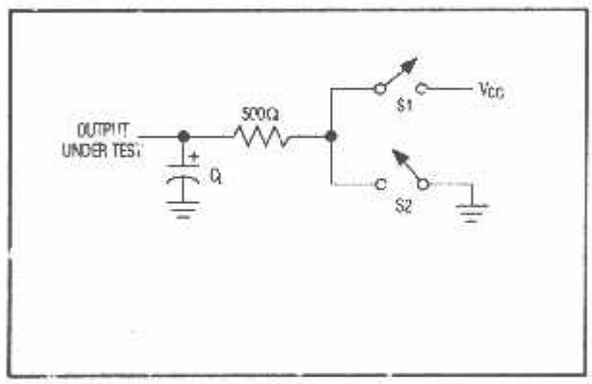


Figure 7. Driver Timing Test Load

MAX483/MAX487/MAX488/MAX489: Reduced EMI and Reflections

The MAX483 and MAX487–MAX489 are slew-rate limited, minimizing EMI and reducing reflections caused by improperly terminated cables. Figure 12 shows the driver output waveform and its Fourier analysis of a 150kHz signal transmitted by a MAX481, MAX485, MAX490, MAX491, or MAX1487. High-frequency harmonics with large amplitudes are evident. Figure 13 shows the same information displayed for a MAX483, MAX487, MAX488, or MAX489 transmitting under the same conditions. Figure 13's high-frequency harmonics have much lower amplitudes, and the potential for EMI is significantly reduced.

Low-Power, Slew-Rate-Limited RS-485/RS-422 Transceivers

Switching Waveforms

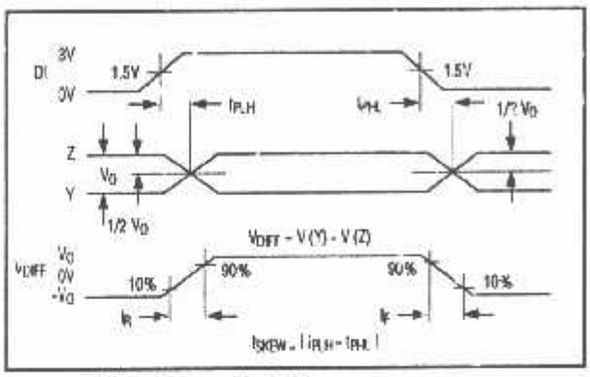


Figure 9. Driver Propagation Delays

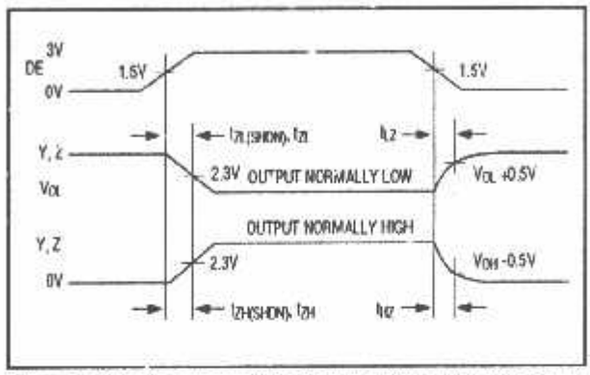


Figure 9. Driver Enable and Disable Times (except MAX488 and MAX490)

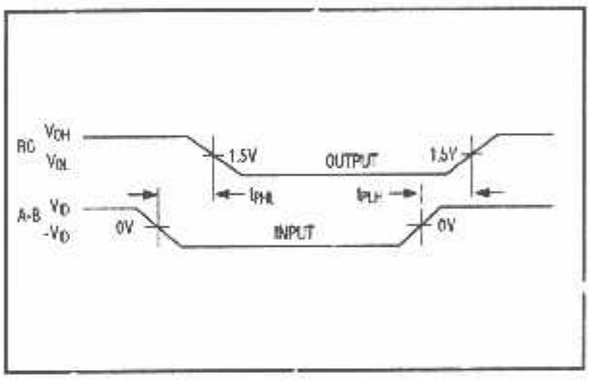


Figure 10. Receiver Propagation Delays

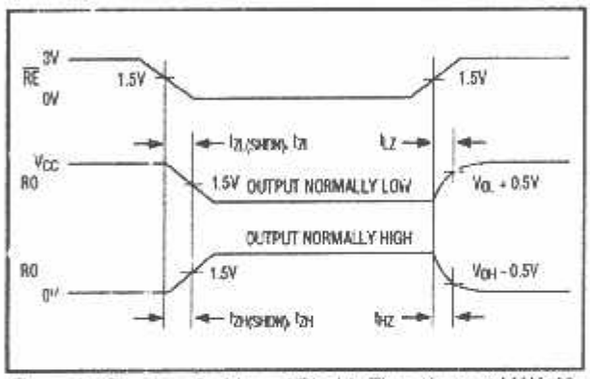


Figure 11. Receiver Enable and Disable Times (except MAX488 and MAX490)

Function Tables (MAX481/MAX483/MAX485/MAX487/MAX1487)

Table 1. Transmitting

INPUTS			OUTPUTS	
$\overline{RE}$	DE	DI	Z	Y
X	1	1	0	1
X	1	0	1	0
0	0	X	High-Z	High-Z
1	0	X	High-Z*	High-Z*

X = Don't care
High-Z = High impedance
* Shutdown mode for MAX481/MAX483/MAX487

Table 2. Receiving

INPUTS			OUTPUT
$\overline{RE}$	DE	A-B	RO
0	0	≥ +0.2V	1
0	0	≤ -0.2V	0
0	0	Inputs open	1
1	0	X	High-Z*

X = Don't care
High-Z = High impedance
* Shutdown mode for MAX481/MAX483/MAX487

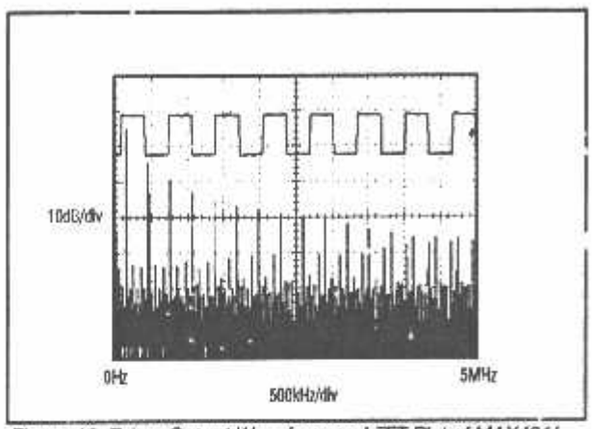


Figure 12. Driver Output Waveform and FFT Plot of MAX481/MAX485/MAX490/MAX491/MAX1487 Transmitting a 150kHz Signal

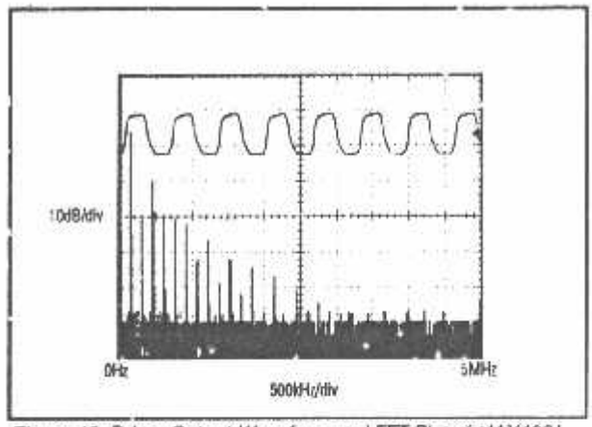


Figure 13. Driver Output Waveform and FFT Plot of MAX483/MAX487–MAX489 Transmitting a 150kHz Signal

Low-Power Shutdown Mode (MAX481/MAX483/MAX487)

A low-power shutdown mode is initiated by bringing both $\overline{RE}$ high and DE low. The devices will not shut down unless both the driver and receiver are disabled. In shutdown, the devices typically draw only 0.1µA of supply current.

$\overline{RE}$ and DE may be driven simultaneously; the parts are guaranteed not to enter shutdown if $\overline{RE}$ is high and DE is low for less than 50ns. If the inputs are in this state for at least 600ns, the parts are guaranteed to enter shutdown.

For the MAX481, MAX483, and MAX487, the t_{ZH} and t_{ZL} enable times assume the part was not in the low-power shutdown state (the MAX485/MAX488–MAX491 and MAX1487 can not be shut down). The $t_{ZH(SHDN)}$ and $t_{ZL(SHDN)}$ enable times assume the parts were shut down (see *Electrical Characteristics*).

It takes the drivers and receivers longer to become enabled from the low-power shutdown state ($t_{ZH(SHDN)}$, $t_{ZL(SHDN)}$) than from the operating mode (t_{ZH}, t_{ZL}). (The parts are in operating mode if the $\overline{RE}$, DE inputs equal a logical 0,1 or 1,1 or 0, 0.)

Driver Output Protection

Excessive output current and power dissipation caused by faults or by bus contention are prevented by two mechanisms. A foldback current limit on the output stage provides immediate protection against short circuits over the whole common-mode voltage range (see *Typical Operating Characteristics*). In addition, a thermal shutdown circuit forces the driver outputs into a high-impedance state if the die temperature rises excessively.

Propagation Delay

Many digital encoding schemes depend on the difference between the driver and receiver propagation delay times. Typical propagation delays are shown in Figures 15–18 using Figure 14's test circuit.

The difference in receiver delay times, $|t_{PLH} - t_{PHL}|$, is typically under 13ns for the MAX481, MAX485, MAX490, MAX491, and MAX1487 and is typically less than 100ns for the MAX483 and MAX487–MAX489.

The driver skew times are typically 5ns (10ns max) for the MAX481, MAX485, MAX490, MAX491, and MAX1487, and are typically 100ns (800ns max) for the MAX483 and MAX487–MAX489.

Low-Power, Slew-Rate-Limited RS-485/RS-422 Transceivers

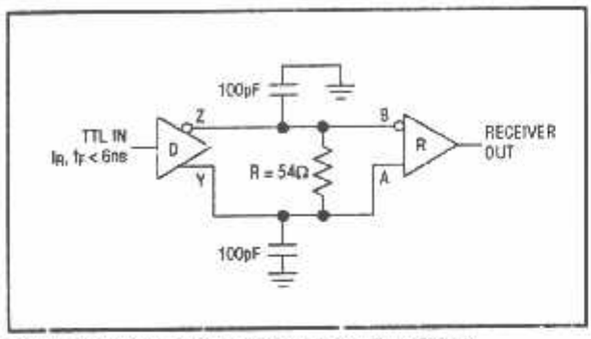


Figure 14. Receiver Propagation Delay Test Circuit

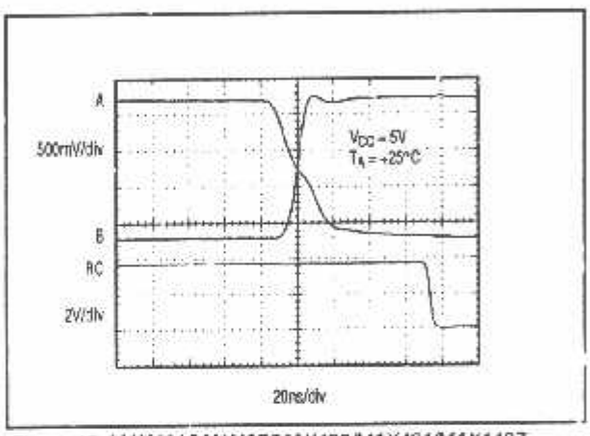


Figure 15. MAX481/MAX485/MAX490/MAX491/MAX1487 Receiver tPHL

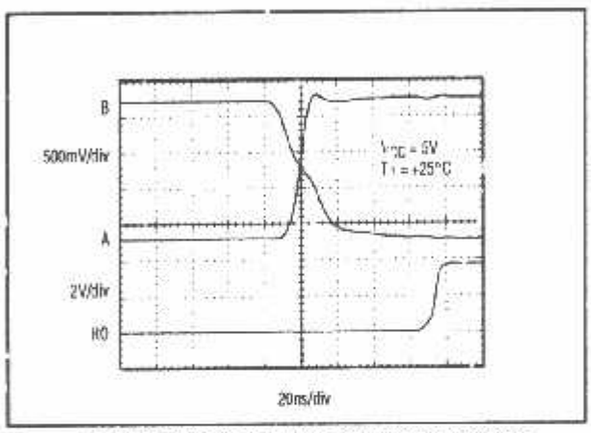


Figure 16. MAX481/MAX485/MAX490/MAX491/MAX1487 Receiver tPLH

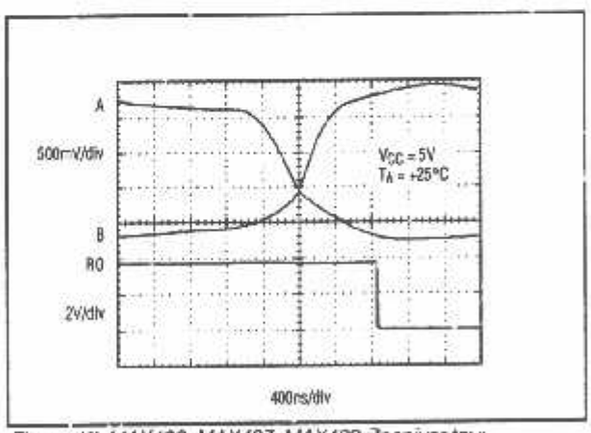


Figure 17. MAX483, MAX487–MAX489 Receiver tPHL

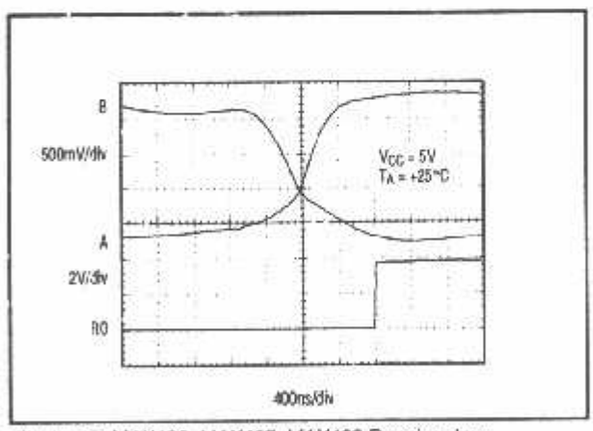


Figure 18. MAX483, MAX487–MAX489 Receiver tPLH

Line Length vs. Data Rate

The RS-485/RS-422 standard covers line lengths up to 4000 feet. For line lengths greater than 4000 feet, see Figure 23.

Figures 19 and 20 show the system differential voltage for the parts driving 4000 feet of 26AWG twisted-pair wire at 110kHz into 120Ω loads.

Typical Applications

The MAX481, MAX483, MAX485, MAX487–MAX491, and MAX1487 transceivers are designed for bidirectional data communications on multipoint bus transmission lines.

Figures 21 and 22 show typical network applications circuits. These parts can also be used as line repeaters, with cable lengths longer than 4000 feet, as shown in Figure 23.

To minimize reflections, the line should be terminated at both ends in its characteristic impedance, and stub lengths off the main line should be kept as short as possible. The slew-rate-limited MAX483 and MAX487–MAX489 are more tolerant of imperfect termination.

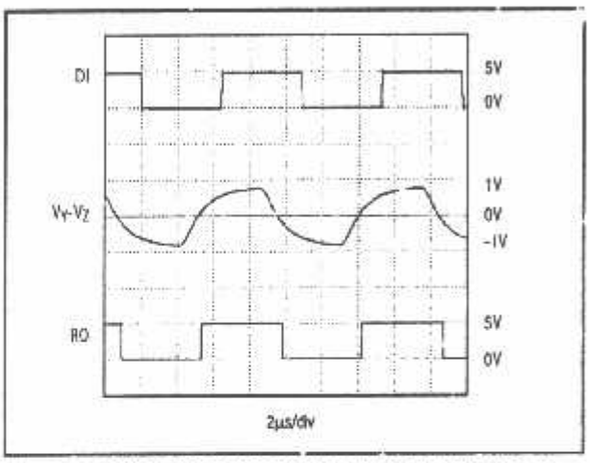


Figure 19. MAX481/MAX485/MAX490/MAX491/MAX1487 System Differential Voltage at 110kHz Driving 4000ft of Cable

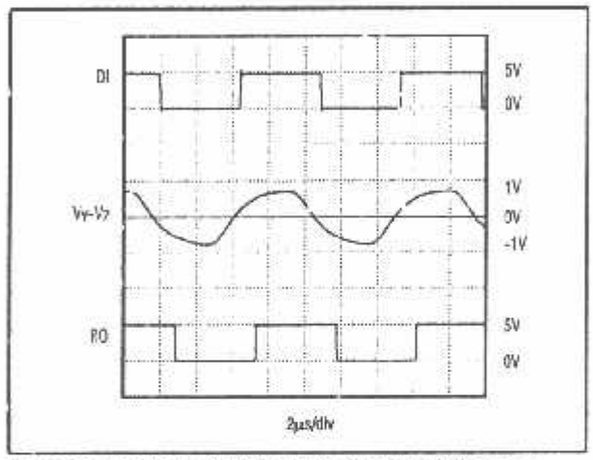


Figure 20. MAX483, MAX487–MAX489 System Differential Voltage at 110kHz Driving 4000ft of Cable

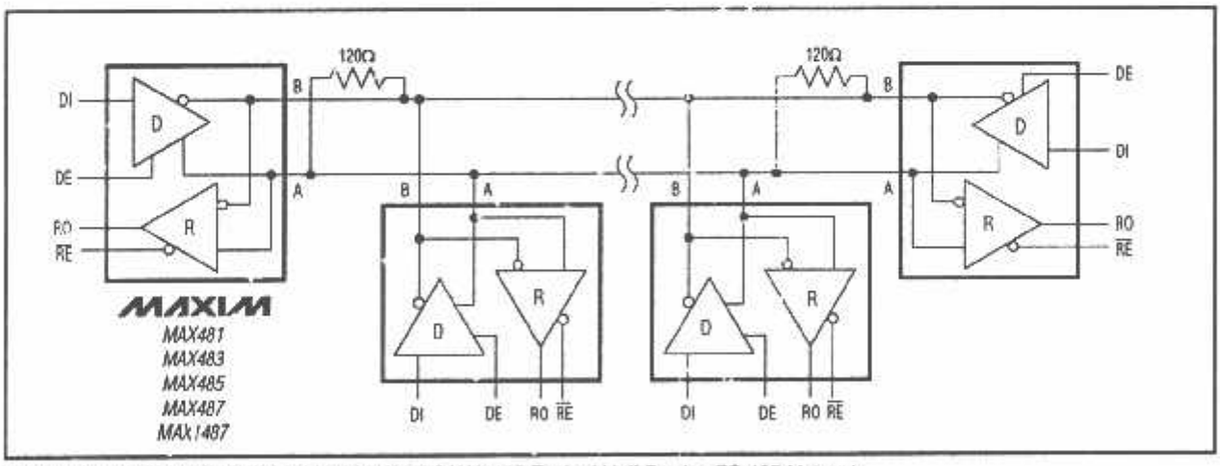


Figure 21. MAX481/MAX483/MAX485/MAX487/MAX1487 Typical Half-Duplex RS-485 Network

Low-Power, Slew-Rate-Limited RS-485/RS-422 Transceivers

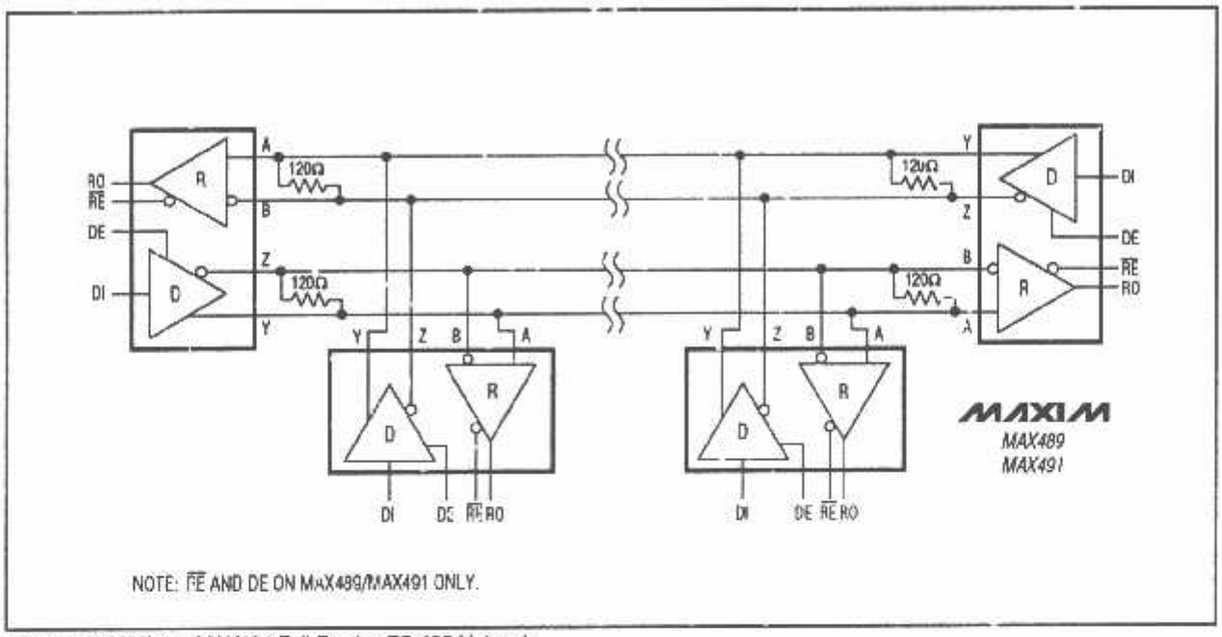


Figure 22. MAX488–MAX491 Full-Duplex RS-485 Network

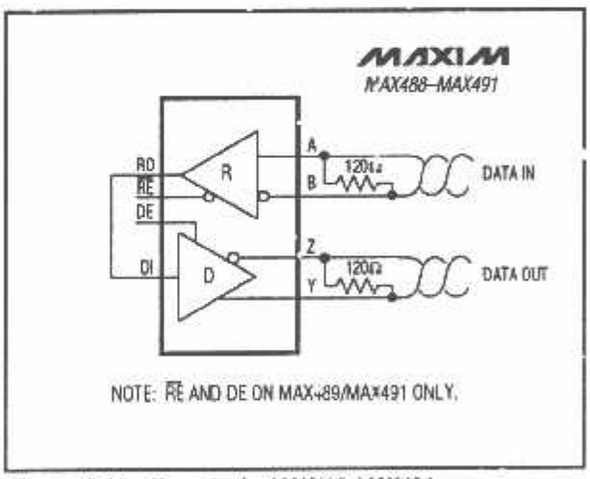


Figure 23. Line Repeater for MAX488–MAX491

Isolated RS-485

For isolated RS-485 applications, see the MAX253 and MAX1480 data sheets.

Ordering Information (continued)

PART	TEMP. RANGE	PIN-PACKAGE
MAX481EPA	-40°C to +85°C	8 Plastic DIP
MAX481ESA	-40°C to +85°C	8 SO
MAX481MJA	-55°C to +125°C	8 CERDIP
MAX483CPA	0°C to +70°C	8 Plastic DIP
MAX483CSA	0°C to +70°C	8 SO
MAX483CUA	0°C to +70°C	8 µMAX
MAX483C/D	0°C to +70°C	Dice*
MAX483EPA	-40°C to +85°C	8 Plastic DIP
MAX483ESA	-40°C to +85°C	8 SO
MAX483MJA	-55°C to +125°C	8 CERDIP
MAX485CPA	0°C to +70°C	8 Plastic DIP
MAX485CSA	0°C to +70°C	8 SO
MAX485CUA	0°C to +70°C	8 µMAX
MAX485C/D	0°C to +70°C	Dice*
MAX485EPA	-40°C to +85°C	8 Plastic DIP
MAX485ESA	-40°C to +85°C	8 SO
MAX485MJA	-55°C to +125°C	8 CERDIP
MAX487CPA	0°C to +70°C	8 Plastic DIP
MAX487CSA	0°C to +70°C	8 SO
MAX487CUA	0°C to +70°C	8 µMAX
MAX487C/D	0°C to +70°C	Dice*
MAX487EPA	-40°C to +85°C	8 Plastic DIP
MAX487ESA	-40°C to +85°C	8 SO
MAX487MJA	-55°C to +125°C	8 CERDIP
MAX488CPA	0°C to +70°C	8 Plastic DIP
MAX488CSA	0°C to +70°C	8 SO
MAX488CUA	0°C to +70°C	8 µMAX
MAX488C/D	0°C to +70°C	Dice*
MAX488EPA	-40°C to +85°C	8 Plastic DIP
MAX488ESA	-40°C to +85°C	8 SO
MAX488MJA	-55°C to +125°C	8 CERDIP
MAX489CPD	0°C to +70°C	14 Plastic DIP
MAX489CSD	0°C to +70°C	14 SO
MAX489C/D	0°C to +70°C	Dice*
MAX489EPD	-40°C to +85°C	14 Plastic DIP
MAX489ESD	-40°C to +85°C	14 SO
MAX489MJD	-55°C to +125°C	14 CERDIP

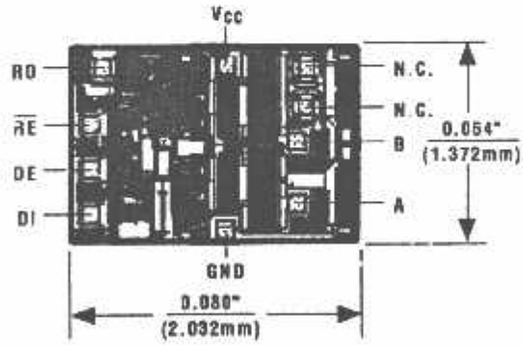
Ordering Information (continued)

PART	TEMP. RANGE	PIN-PACKAGE
MAX490CPA	0°C to +70°C	8 Plastic DIP
MAX490CSA	0°C to +70°C	8 SO
MAX490CUA	0°C to +70°C	8 µMAX
MAX490C/D	0°C to +70°C	Dice*
MAX490EPA	-40°C to +85°C	8 Plastic DIP
MAX490ESA	-40°C to +85°C	8 SO
MAX490MJA	-55°C to +125°C	8 CERDIP
MAX491CPD	0°C to +70°C	14 Plastic DIP
MAX491CSD	0°C to +70°C	14 SO
MAX491C/D	0°C to +70°C	Dice*
MAX491EPD	-40°C to +85°C	14 Plastic DIP
MAX491ESD	-40°C to +85°C	14 SO
MAX491MJD	-55°C to +125°C	14 CERDIP
MAX1487CPA	0°C to +70°C	8 Plastic DIP
MAX1487CSA	0°C to +70°C	8 SO
MAX1487CUA	0°C to +70°C	8 µMAX
MAX1487C/D	0°C to +70°C	Dice*
MAX1487EPA	-40°C to +85°C	8 Plastic DIP
MAX1487ESA	-40°C to +85°C	8 SO
MAX1487MJA	-55°C to +125°C	8 CERDIP

* *Contact factory for dice specifications.*

Chip Topographies

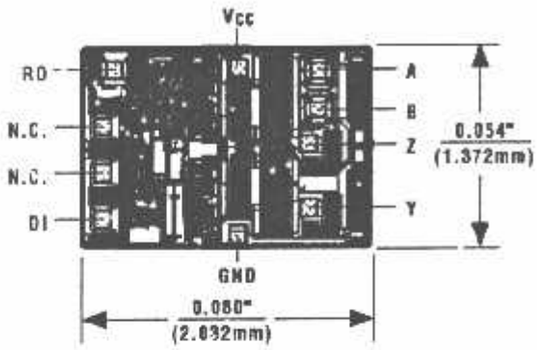
MAX481/MAX483/MAX485/MAX487/MAX1487



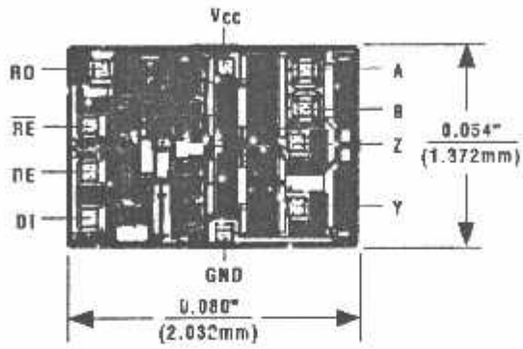
Low-Power, Slew-Rate-Limited RS-485/RS-422 Transceivers

Chip Topographies (continued)

MAX488/MAX490

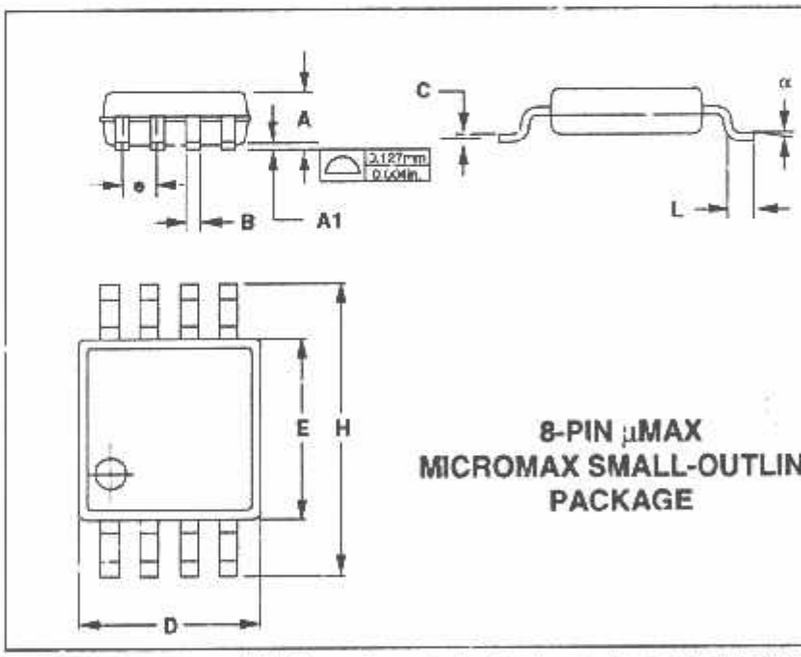


MAX489/MAX491



TRANSISTOR COUNT: 248
SUBSTRATE CONNECTED TO GND

Package Information



DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.053	0.069	1.35	1.75
A1	0.004	0.010	0.10	0.25
B	0.014	0.019	0.35	0.49
C	0.007	0.010	0.19	0.25
D	0.189	0.197	4.80	5.00
E	0.150	0.157	3.80	4.00
e	0.050 BSC		1.27 BSC	
H	0.228	0.244	5.80	6.20
h	0.010	0.020	0.25	0.50
L	0.016	0.050	0.40	1.27
α	0°	8°	0°	8°

21-325A

8-PIN µMAX MICROMAX SMALL-OUTLINE PACKAGE

October 1999

National Semiconductor

ADC0808/ADC0809
8-Bit µP Compatible A/D Converters with 8-Channel Multiplexer

General Description

The ADC0808, ADC0809 data acquisition component is a monolithic CMOS device with an 8-bit analog-to-digital converter, 8-channel multiplexer and microprocessor compatible control logic. The 8-bit A/D converter uses successive approximation as the conversion technique. The converter features a high impedance chopper stabilized comparator, a 256R voltage divider with analog switch tree and a successive approximation register. The 8-channel multiplexer can directly access any of 8-single-ended analog signals.

The device eliminates the need for external zero and full-scale adjustments. Easy interfacing to microprocessors is provided by the latched and decoded multiplexer address inputs and latched TTL TRI-STATE® outputs.

The design of the ADC0808, ADC0809 has been optimized by incorporating the most desirable aspects of several A/D conversion techniques. The ADC0808, ADC0809 offers high speed, high accuracy, minimal temperature dependence, excellent long-term accuracy and repeatability, and consumes minimal power. These features make this device ideally suited to applications from process and machine control to consumer and automotive applications. For 16-channel multiplexer with common output (sample/hold port) see ADC0816 data sheet. (See AN-247 for more information.)

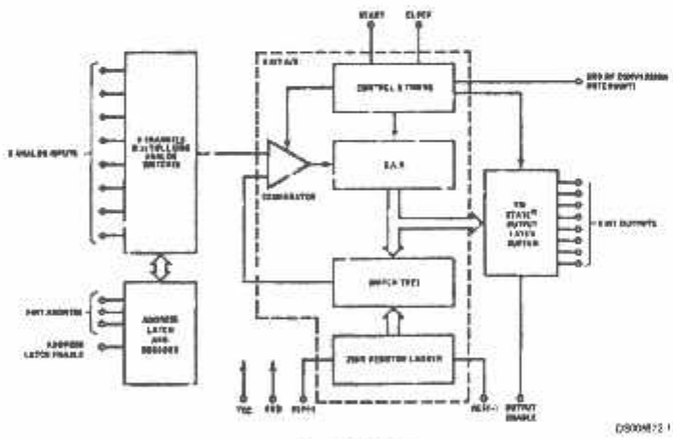
Features

- Easy interface to all microprocessors
- Operates ratiometrically or with 5 V_{DC} or analog span adjusted voltage reference
- No zero or full-scale adjust required
- 8-channel multiplexer with address logic
- 0V to 5V input range with single 5V power supply
- Outputs meet TTL voltage level specifications
- Standard hermetic or molded 28-pin DIP package
- 28-pin molded chip carrier package
- ADC0808 equivalent to MM74C949
- ADC0809 equivalent to MM74C949-1

Key Specifications

Resolution	8 Bits
Total Unadjusted Error	±½ LSB and ±1 LSB
Single Supply	5 V_{DC}
Low Power	15 mW
Conversion Time	100 µs

Block Diagram



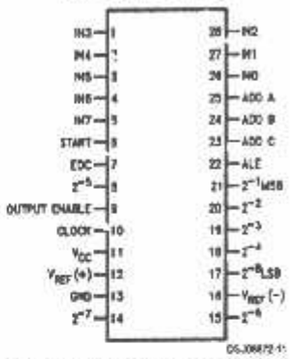
See Ordering Information

TRI-STATE® is a registered trademark of National Semiconductor Corp.

 DS005672

Connection Diagrams

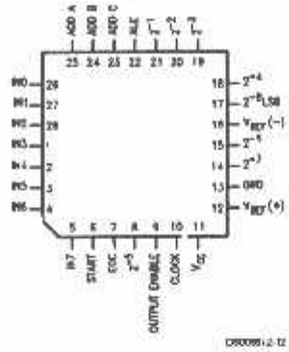
Dual-In-Line Package



TL/H/5671-1

Order Number ADC0808CCN or ADC0809CCN
See NS Package J28A or N28A

Molded Chip Carrier Package



D80080-2-12

Order Number ADC0808CCV or ADC0809CCV
See NS Package V28A

Ordering Information

TEMPERATURE RANGE		−40°C to +85°C			−55°C to +125°C
Error	±½ LSB Unadjusted	ADC0808CCN	ADC0808CCV	ADC0808CCJ	ADC0808CJ
	±1 LSB Unadjusted	ADC0809CCN	ADC0809CCV		
Package Outline		N28A Molded DIP	V28A Molded Chip Carrier	J28A Ceramic DIP	J28A Ceramic DIP

Absolute Maximum Ratings (Notes 2, 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Supply Voltage (V_{CC}) (Note 3)	6.5V
Voltage at Any Pin Except Control Inputs	−0.3V to (V_{CC}+0.3V)
Voltage at Control Inputs (START, OE, CLOCK, ALE, ADD A, ADD B, ADD C)	−0.3V to +15V
Storage Temperature Range	−65°C to +150°C
Package Dissipation at T_A=25°C	875 mW
Lead Temp. (Soldering, 10 seconds)	
Dual-In-Line Package (plastic)	260°C
Dual-In-Line Package (ceramic)	300°C
Molded Chip Carrier Package	
Vapor Phase (60 seconds)	215°C
Infrared (15 seconds)	220°C
ESD Susceptibility (Note 8)	400V

Operating Conditions (Notes 1, 2)

Temperature Range (Note 1)	$T_{MIN} \le T_A \le T_{MAX}$
ADC0808CCN,ADC0809CCN	−40°C≤T_A≤+85°C
ADC0808CCV, ADC0809CCV	−40°C ≤ T_A ≤ +85°C
Range of V_{CC} (Note 1)	4.5 V_{DC} to 6.0 V_{DC}

Electrical Characteristics

Converter Specifications: V_{CC}=5 V_{DC}=V_{REF+}, $V_{REF(-)}$=GND, $T_{MIN} \le T_A \le T_{MAX}$ and f_{CLK}=640 kHz unless otherwise stated.

Symbol	Parameter	Conditions	Min	Typ	Max	Units
	ADC0808					
	Total Unadjusted Error	25°C			±½	LSB
	(Note 5)	T_{MIN} to T_{MAX}			±¾	LSB
	ADC0809					
	Total Unadjusted Error	0°C to 70°C			±1	LSB
	(Note 5)	T_{MIN} to T_{MAX}			±1¼	LSB
	Input Resistance	From Ref(+) to Ref(−)	1.0	2.5		kΩ
	Analog Input Voltage Range	(Note 4) V(+) or V(−)	GND−0.10		V_{CC}+0.10	V_{DC}
$V_{REF(+)}$	Voltage, Top of Ladder	Measured at Ref(+)		V_{CC}	V_{CC}+0.1	V
$\frac{V_{REF(+)}+V_{REF(-)}}{2}$	Voltage, Center of Ladder		V_{CC}/2-0.1	V_{CC}/2	V_{CC}/2+0.1	V
$V_{REF(-)}$	Voltage, Bottom of Ladder	Measured at Ref(−)	−0.1	0		V
I_{IN}	Comparator Input Current	f_c=640 kHz, (Note 6)	−2	±0.5	2	µA

Electrical Characteristics

Digital Levels and DC Specifications: ADC0808CCN, ADC0808CCV, ADC0809CCN and ADC0809CCV, 4.75≤V_{CC}≤5.25V, −40°C≤T_A≤+85°C unless otherwise noted

Symbol	Parameter	Conditions	Min	Typ	Max	Units
ANALOG MULTIPLEXER						
$I_{OFF(+)}$	OFF Channel Leakage Current	V_{CC}=5V, V_{IN}=5V,				
		T_A=25°C		10	200	nA
		T_{MIN} to T_{MAX}			1.0	µA
$I_{OFF(-)}$	OFF Channel Leakage Current	V_{CC}=5V, V_{IN}=0,				
		T_A=25°C	−200	−10		nA
		T_{MIN} to T_{MAX}	−1.0			µA
CONTROL INPUTS						
$V_{IN(1)}$	Logical "1" Input Voltage		V_{CC}−1.5			V
$V_{IN(0)}$	Logical "0" Input Voltage				1.5	V
$I_{IN(1)}$	Logical "1" Input Current (The Control Inputs)	V_{IN}=15V			1.0	µA
$I_{IN(0)}$	Logical "0" Input Current (The Control Inputs)	V_{IN}=0	−1.0			µA
I_{CC}	Supply Current	f_{CLK}=640 kHz		0.3	3.0	mA

Electrical Characteristics (Continued)

Digital Levels and DC Specifications: ADC0808CCN, ADC0808CCV, ADC0809CCN and ADC0809CCV, $4.75 \le V_{CC} \le 5.25V$, $-40^{\circ}C \le T_A \le +85^{\circ}C$ unless otherwise noted

Symbol	Parameter	Conditions	Min	Typ	Max	Units
DATA OUTPUTS AND EOC (INTERRUPT)						
$V_{OUT(1)}$	Logical "1" Output Voltage	V_{CC} = 4.75V I_{OUT} = −360µA I_{OUT} = −10µA		2.4 4.5		V(min) V(min)
$V_{OUT(0)}$	Logical "0" Output Voltage	I_O=1.6 mA			0.45	V
$V_{OUT(0)}$	Logical "0" Output Voltage EOC	I_O=1.2 mA			0.45	V
I_{OUT}	TRI-STATE Output Current	V_O=5V V_O=0	 −3		3	µA µA

Electrical Characteristics

Timing Specifications $V_{CC}=V_{REF(+)}=5V$, $V_{REF(-)}=GND$, $t_r=t_f=20$ ns and $T_A=25^{\circ}C$ unless otherwise noted.

Symbol	Parameter	Conditions	Min	Typ	Max	Units
t_{WS}	Minimum Start Pulse Width	(*Figure 5*)		100	200	ns
t_{WALE}	Minimum ALE Pulse Width	(*Figure 5*)		100	200	ns
t_s	Minimum Address Set-Up Time	(*Figure 5*)		25	50	ns
t_H	Minimum Address Hold Time	(*Figure 5*)		25	50	ns
t_D	Analog MUX Delay Time From ALE	R_S=0Ω (*Figure 5*)		1	2.5	µs
t_{H1}, t_{H0}	OE Control to Q Logic State	C_L=50 pF, R_L=10k (*Figure 8*)		125	250	ns
t_{1H}, t_{0H}	OE Control to HI-Z	C_L=10 pF, R_L=10k (*Figure 8*)		125	250	ns
t_C	Conversion Time	f_c=640 kHz, (*Figure 5*) (Note 7)	90	100	116	µs
f_c	Clock Frequency		10	640	1280	kHz
t_{EOC}	EOC Delay Time	(*Figure 5*)	0		8+2 µS	Clock Periods
C_{IN}	Input Capacitance	At Control Inputs		10	15	pF
C_{OUT}	TRI-STATE Output Capacitance	At TRI-STATE Outputs		10	15	pF

Note 1: Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. DC and AC electrical specifications do not apply when operating the device beyond its specified operating conditions.

Note 2: All voltages are measured with respect to GND, unless otherwise specified.

Note 3: A zener diode exists, internally, from V_{CC} to GND and has a typical breakdown voltage of 7 V_{DC}.

Note 4: Two on-chip diodes are tied to each analog input which will forward conduct for analog input voltages one diode drop below ground or one diode drop greater than the V_{CC} supply. The spec allows 100 mV forward bias of either diode. This means that as long as the analog V_{IN} does not exceed the supply voltage by more than 100 mV, the output code will be correct. To achieve an absolute $0V_{DC}$ to $5V_{DC}$ input voltage range will therefore require a minimum supply voltage of 4.900 V_{DC} over temperature variations, initial tolerance and loading.

Note 5: Total unadjusted error includes offset, full-scale, linearity, and multiplexer errors. See *Figure 3*. None of these A/Ds requires a zero or full-scale adjust. However, if an all zero code is desired for an analog input other than 0.0V, or if a narrow full-scale span exists (for example: 0.5V to 4.5V full-scale) the reference voltages can be adjusted to achieve this. See *Figure 13*.

Note 6: Comparator input current is a bias current into or out of the chopper stabilized comparator. The bias current varies directly with clock frequency and has little temperature dependence (*Figure 6*). See paragraph 4.0.

Note 7: The outputs of the data register are updated one clock cycle before the rising edge of EOC.

Note 8: Human body model, 100 pF discharged through a 1.5 kΩ resistor.

Functional Description

Multiplexer. The device contains an 8-channel single-ended analog signal multiplexer. A particular input channel is selected by using the address decoder. *Table 1* shows the input states for the address lines to select any channel. The address is latched into the decoder on the low-to-high transition of the address latch enable signal.

TABLE 1.

SELECTED ANALOG CHANNEL	ADDRESS LINE		
	C	B	A
IN0	L	L	L
IN1	L	L	H
IN2	L	H	L
IN3	L	H	H
IN4	H	L	L
IN5	H	L	H
IN6	H	H	L
IN7	H	H	H

CONVERTER CHARACTERISTICS

The Converter

The heart of this single chip data acquisition system is its 8-bit analog-to-digital converter. The converter is designed to give fast, accurate, and repeatable conversions over a wide range of temperatures. The converter is partitioned into 3 major sections: the 256R ladder network, the successive approximation register, and the comparator. The converter's digital outputs are positive true.

The 256R ladder network approach (*Figure 1*) was chosen over the conventional R/2R ladder because of its inherent monotonicity, which guarantees no missing digital codes. Monotonicity is particularly important in closed loop feedback control systems. A non-monotonic relationship can cause oscillations that will be catastrophic for the system. Additionally, the 256R network does not cause load variations on the reference voltage.

The bottom resistor and the top resistor of the ladder network in *Figure 1* are not the same value as the remainder of the network. The difference in these resistors causes the output characteristic to be symmetrical with the zero and full-scale points of the transfer curve. The first output transition occurs when the analog signal has reached +½ LSB and succeeding output transitions occur every 1 LSB later up to full-scale.

The successive approximation register (SAR) performs 8 iterations to approximate the input voltage. For any SAR type converter, n-iterations are required for an n-bit converter. *Figure 2* shows a typical example of a 3-bit converter. In the ADC0808, ADC0809, the approximation technique is extended to 8 bits using the 256R network.

The A/D converter's successive approximation register (SAR) is reset on the positive edge of the start conversion (SC) pulse. The conversion is begun on the falling edge of the start conversion pulse. A conversion in process will be interrupted by receipt of a new start conversion pulse. Continuous conversion may be accomplished by tying the end-of-conversion (EOC) output to the SC input. If used in this mode, an external start conversion pulse should be applied after power up. End-of-conversion will go low between 0 and 8 clock pulses after the rising edge of start conversion.

The most important section of the A/D converter is the comparator. It is this section which is responsible for the ultimate accuracy of the entire converter. It is also the comparator drift which has the greatest influence on the repeatability of the device. A chopper-stabilized comparator provides the most effective method of satisfying all the converter requirements.

The chopper-stabilized comparator converts the DC input signal into an AC signal. This signal is then fed through a high gain AC amplifier and has the DC level restored. This technique limits the drift component of the amplifier since the drift is a DC component which is not passed by the AC amplifier. This makes the entire A/D converter extremely insensitive to temperature, long term drift and input offset errors.

Figure 4 shows a typical error curve for the ADC0808 as measured using the procedures outlined in AN-179.

Functional Description (Continued)

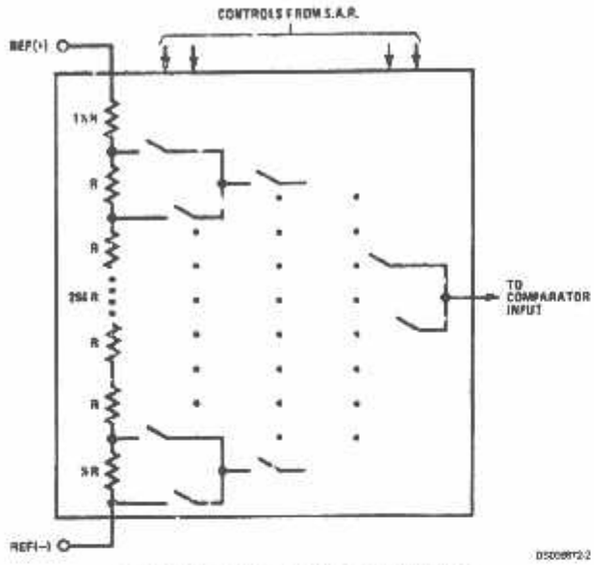


FIGURE 1. Resistor Ladder and Switch Tree

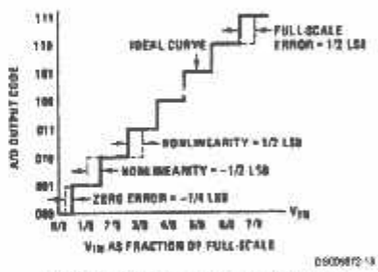


FIGURE 2. 3-Bit A/D Transfer Curve

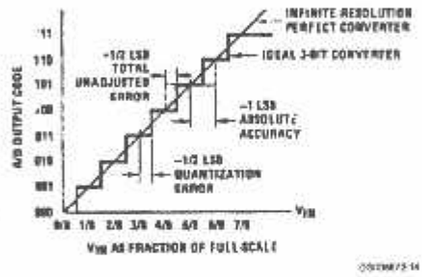


FIGURE 3. 3-Bit A/D Absolute Accuracy Curve

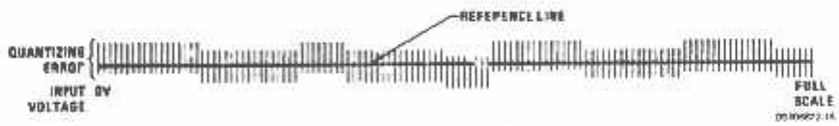


FIGURE 4. Typical Error Curve

Timing Diagram

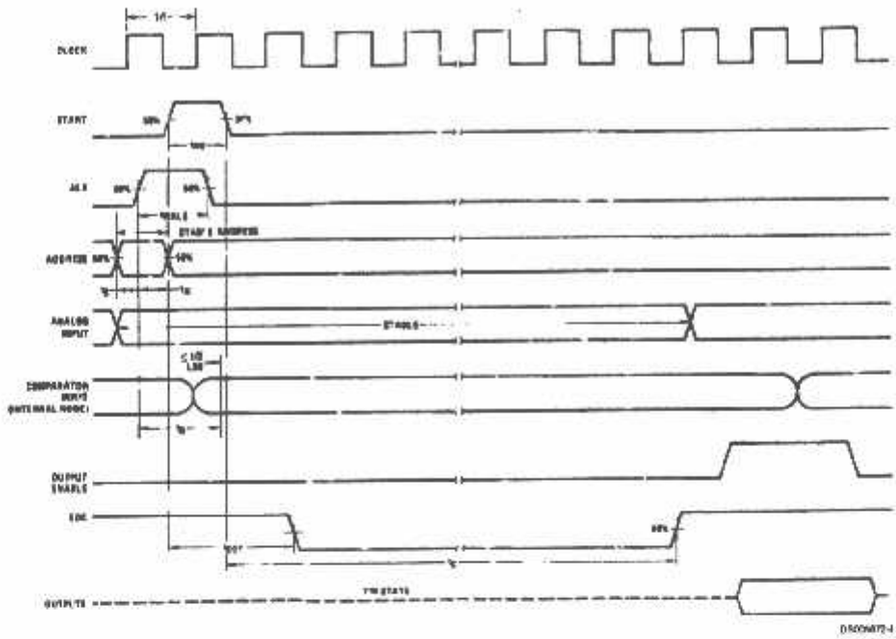


FIGURE 5.

Typical Performance Characteristics

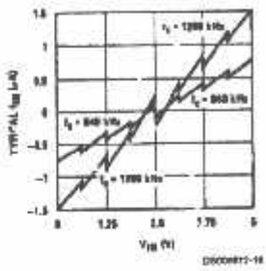


FIGURE 6. Comparator I_{IN} vs V_{IN} ($V_{CC}=V_{REF}=5V$)

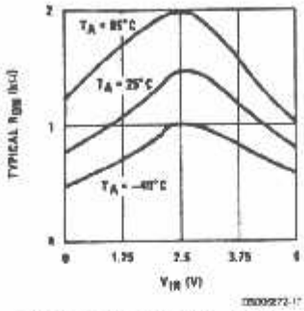


FIGURE 7. Multiplexer R_{ON} vs V_{IN} ($V_{CC}=V_{REF}=5V$)

TRI-STATE Test Circuits and Timing Diagrams

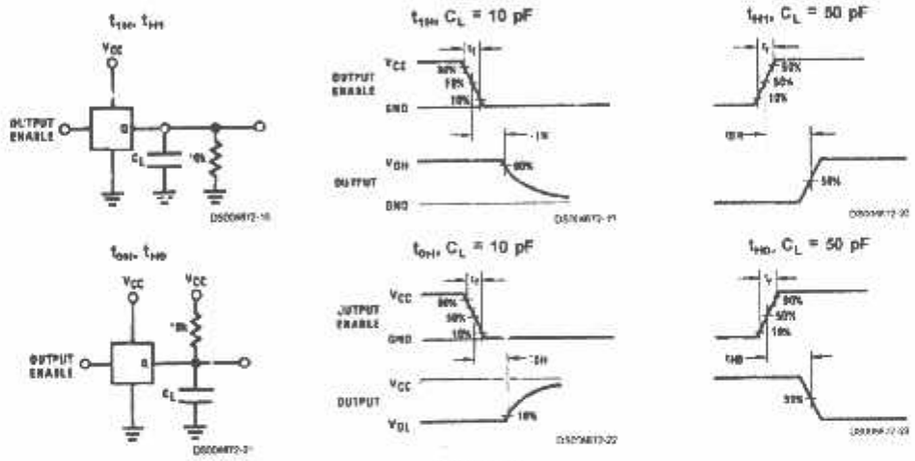


FIGURE 8.

Applications Information

OPERATION

1.0 RATIOMETRIC CONVERSION

The ADC0808, ADC0809 is designed as a complete Data Acquisition System (DAS) for ratiometric conversion systems. In ratiometric systems, the physical variable being measured is expressed as a percentage of full-scale which is not necessarily related to an absolute standard. The voltage input to the ADC0808 is expressed by the equation

$$\frac{V_{IN}}{V_{fs}-V_Z}=\frac{D_X}{D_{MAX}-D_{MIN}} \qquad (1)$$

V_{IN}=Input voltage into the ADC0809

V_{fs}=Full-scale voltage

V_Z=Zero voltage

D_X=Data point being measured

D_{MAX}=Maximum data limit

D_{MIN}=Minimum data limit

A good example of a ratiometric transducer is a potentiometer used as a position sensor. The position of the wiper is directly proportional to the output voltage which is a ratio of the full-scale voltage across it. Since the data is represented as a proportion of full-scale, reference requirements are greatly reduced, eliminating a large source of error and cost for many applications. A major advantage of the ADC0808, ADC0809 is that the input voltage range is equal to the supply range so the transducers can be connected directly across the supply and their outputs connected directly into the multiplexer inputs, (*Figure 9*).

Ratiometric transducers such as potentiometers, strain gauges, thermistor bridges, pressure transducers, etc., are suitable for measuring proportional relationships; however, many types of measurements must be referred to an absolute standard such as voltage or current. This means a sys-

Applications Information (Continued)

tem reference must be used which related the full-scale voltage to the standard volt. For example, if $V_{CC}=V_{REF}=5.12V$, then the full-scale range is divided into 256 standard steps. The smallest standard step is 1 LSB which is then 20 mV.

2.0 RESISTOR LADDER LIMITATIONS

The voltages from the resistor ladder are compared to the selected into 8 times in a conversion. These voltages are coupled to the comparator via an analog switch tree which is referenced to the supply. The voltages at the top, center and bottom of the ladder must be controlled to maintain proper operation.

The top of the ladder, Ref(+), should not be more positive than the supply, and the bottom of the ladder, Ref(−), should not be more negative than ground. The center of the ladder voltage must also be near the center of the supply because the analog switch tree changes from N-channel switches to P-channel switches. These limitations are automatically satisfied in ratiometric systems and can be easily met in ground referenced systems.

Figure 10 shows a ground referenced system with a separate supply and reference. In this system, the supply must be trimmed to match the reference voltage. For instance, if a 5.12V is used, the supply should be adjusted to the same voltage within 0.1V.

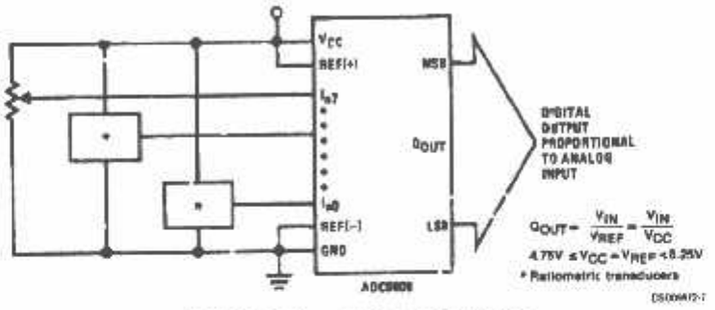
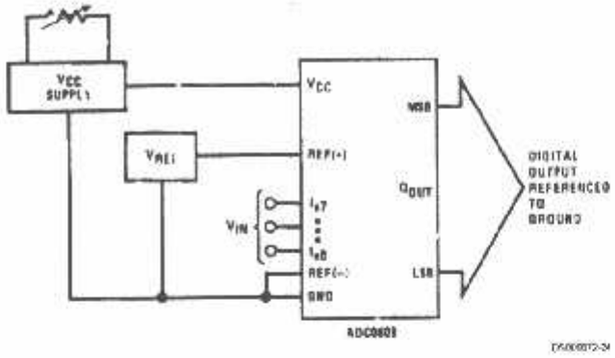


FIGURE 9. Ratiometric Conversion System

The ADC0808 needs less than a milliamp of supply current so developing the supply from the reference is readily accomplished. In *Figure 11* a ground referenced system is shown which generates the supply from the reference. The buffer shown can be an op amp of sufficient drive to supply the milliamp of supply current and the desired bus drive, or if a capacitive bus is driven by the outputs a large capacitor will supply the transient supply current as seen in *Figure 12*. The LM301 is overcompensated to insure stability when loaded by the 10 µF output capacitor.

The top and bottom ladder voltages cannot exceed V_{CC} and ground, respectively, but they can be symmetrically less than V_{CC} and greater than ground. The center of the ladder voltage should always be near the center of the supply. The sensitivity of the converter can be increased, (i.e., size of the LSB steps decreased) by using a symmetrical reference system. In *Figure 13*, a 2.5V reference is symmetrically centered about $V_{CC}/2$ since the same current flows in identical resistors. This system with a 2.5V reference allows the LSB bit to be half the size of a 5V reference system.

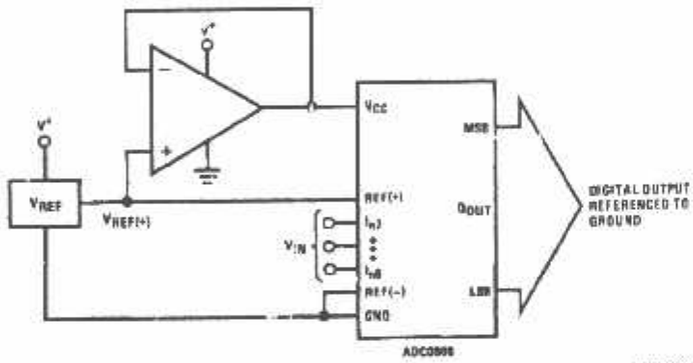
Applications Information (Continued)



$$Q_{OUT} = \frac{V_{IN}}{V_{REF}}$$

$4.75V \leq V_{CC} = V_{REF} \leq 5.25V$

FIGURE 10. Ground Referenced Conversion System Using Trimmed Supply



$$Q_{OUT} = \frac{V_{IN}}{V_{REF}}$$

$4.75V \leq V_{CC} = V_{REF} \leq 5.25V$

FIGURE 11. Ground Referenced Conversion System with Reference Generating V_{CC} Supply

Applications Information (Continued)

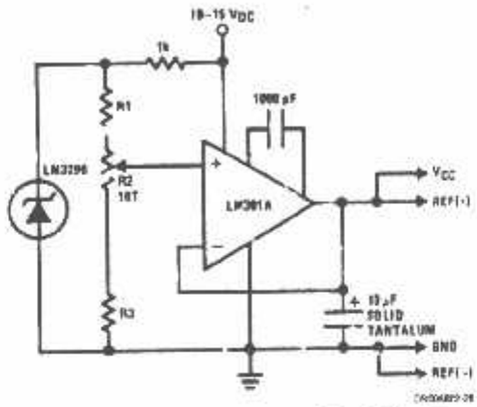
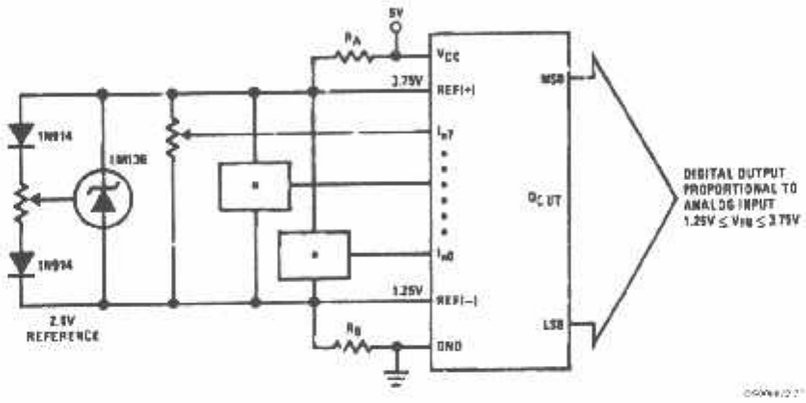


FIGURE 12. Typical Reference and Supply Circuit



$R_A = R_B$

*Ratiometric transducers

FIGURE 13. Symmetrically Centered Reference

3.0 CONVERTER EQUATIONS

The transition between adjacent codes N and N+1 is given by:

$$V_{IN} = \left[(V_{REF(+)} - V_{REF(-)}) \left[\frac{N}{256} + \frac{1}{512} \right] \pm V_{TUE} \right] + V_{REF(-)} \quad (2)$$

The center of an output code N is given by:

$$V_{IN} \left[(V_{REF(+)} - V_{REF(-)}) \left[\frac{N}{256} \right] \pm V_{TUE} \right] + V_{REF(-)} \quad (3)$$

The output code N for an arbitrary input are the integers within the range:

$$N = \frac{V_{IN} - V_{REF(-)}}{V_{REF(+)} - V_{REF(-)}} \times 256 \pm \text{Absolute Accuracy} \quad (4)$$

Where: V_{IN} = Voltage at comparator input
$V_{REF(+)}$ = Voltage at Ref(+)
$V_{REF(-)}$ = Voltage at Ref(−)
V_{TUE} = Total unadjusted error voltage (typically $V_{REF(+)} \cdot 512$)

Applications Information (Continued)

4.0 ANALOG COMPARATOR INPUTS

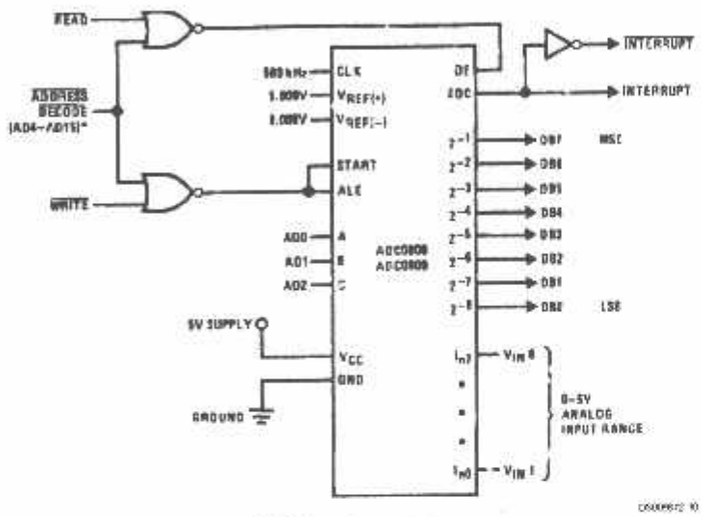
The dynamic comparator input current is caused by the periodic switching of on-chip stray capacitances. These are connected alternately to the output of the resistor ladder/switch tree network and to the comparator input as part of the operation of the chopper stabilized comparator.

The average value of the comparator input current varies directly with clock frequency and with V_{IN} as shown in *Figure 6*.

If no filter capacitors are used at the analog inputs and the signal source impedances are low, the comparator input current should not introduce converter errors, as the transient created by the capacitance discharge will die out before the comparator output is strobed.

If input filter capacitors are desired for noise reduction and signal conditioning they will tend to average out the dynamic comparator input current. It will then take on the characteristics of a DC bias current whose effect can be predicted conventionally.

Typical Application

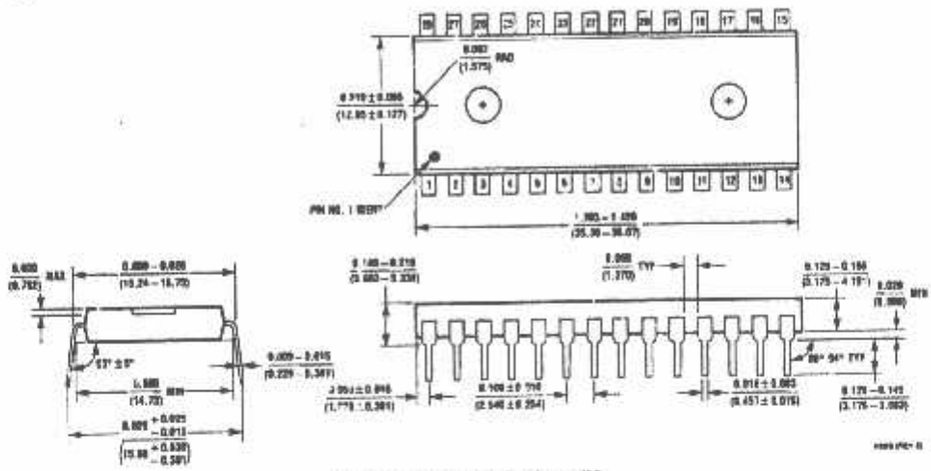


*Address latches needed for 8085 and SC/MP interfacing the ADC0808 to a microprocessor

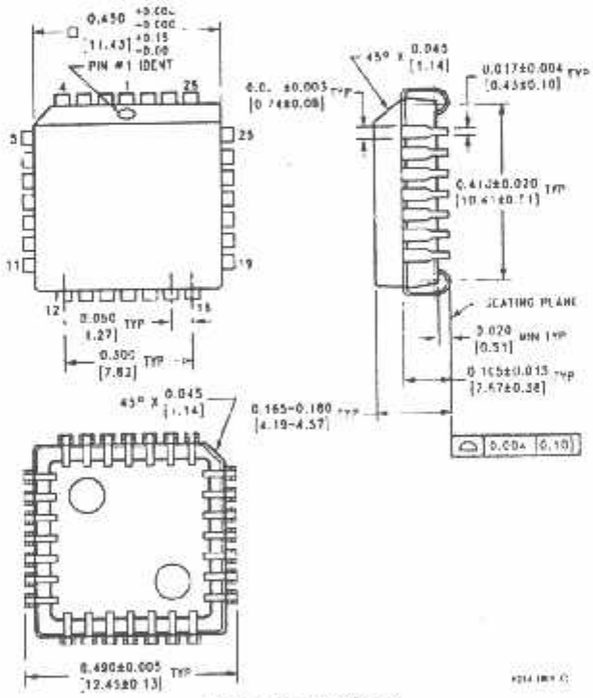
TABLE 2. Microprocessor Interface Table

PROCESSOR	$\overline{\text{READ}}$	$\overline{\text{WRITE}}$	INTERRUPT (COMMENT)
8080	$\overline{\text{MEMR}}$	$\overline{\text{MEMW}}$	INTR (Thru RST Circuit)
8085	$\overline{\text{RD}}$	$\overline{\text{WR}}$	INTR (Thru RST Circuit)
Z-80	$\overline{\text{RD}}$	$\overline{\text{WR}}$	$\overline{\text{INT}}$ (Thru RST Circuit, Mode 0)
SC/MP	NRDS	NWDS	SA (Thru Sense A)
6800	VMA•Φ2•R/W	VMA•Φ•$\overline{\text{R/W}}$	$\overline{\text{IRQA}}$ or $\overline{\text{IRQB}}$ (Thru PIA)

Physical Dimensions inches (millimeters) unless otherwise noted



Molded Dual-In-Line Package (N)
Order Number ADC0808CCN or ADC0809CCN
NS Package Number N28B



Molded Chip Carrier (V)
Order Number ADC0808CCV or ADC0809CCV
NS Package Number V28A

Notes

LIFE SUPPORT POLICY

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DETAILED DESCRIPTION

SPEECH/SOUND QUALITY

The ISD1400 series includes devices offered at 6.4 and 8.0 KHz sampling frequencies, allowing the user a choice of speech quality options. The speech samples are stored directly into on-chip nonvolatile memory without the digitization and compression associated with other solutions. Direct analog storage provides a very true, natural sounding reproduction of voice, music, tones, and sound effects not available with most solid-state digital solutions.

DURATION

To meet end system requirements, the ISD1400 series offers single-chip solutions at 16 and 20 seconds.

EEPROM STORAGE

One of the benefits of ISD's ChipCorder technology is the use of on-chip nonvolatile memory, providing zero-power message storage. The message is retained for up to 100 years typically without power. In addition, the device can be re-recorded typically over 100,000 times.

BASIC OPERATION

The ISD1400 ChipCorder series devices are controlled by a single record signal, $\overline{REC}$, and either of two push-button control playback signals, $\overline{PLAYE}$ (edge-activated playback), and $\overline{PLAYL}$ (level-activated playback). The ISD1400 parts are configured for simplicity of design in a single-message application. Using the address lines will allow multiple message applications. Device operation is explained on page 15.

AUTOMATIC POWER-DOWN MODE

At the end of a playback or record cycle, the ISD1400 series devices automatically return to a low-power standby mode, consuming typically 0.5 μA. During a playback cycle, the device powers down automatically at the end of the message. During a record cycle, the device powers down immediately after $\overline{REC}$ is released HIGH.

ADDRESSING (OPTIONAL)

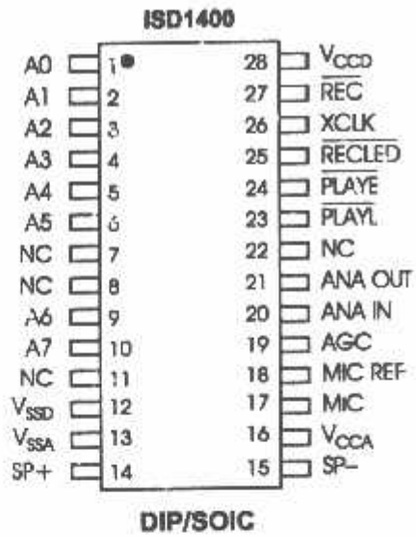
In addition to providing simple message playback, the ISD1400 series provides a full addressing capability.

The ISD1400 series storage array has 160 distinct addressable segments, providing the following resolutions. See Application Information for ISD1400 address tables.

Table 1: Device Playback/Record Durations

Part Number	Minimum Duration (Seconds)
ISD1416	100 ms
ISD1420	125 ms

Figure 1: ISD1400 Series Pinouts



NOTE: *NC means must Not Connect.*

PIN DESCRIPTION

NOTE *The $\overline{REC}$ signal is debounced for 50 ms on the rising edge to prevent a false retriggering from a push-button switch.*

VOLTAGE INPUTS (V_{CCA}, V_{CCD})

Analog and digital circuits internal to the ISD1400 series use separate power buses to minimize noise on the chip. These power buses are brought out to separate pins on the package and should be tied together as close to the supply as possible. It is important that the power supply be decoupled as close as possible to the package.

GROUND INPUTS (V_{SSA}, V_{SSD})

Similar to V_{CCA} and V_{CCD}, the analog and digital circuits internal to the ISD1400 series use separate ground buses to minimize noise. These pins should be tied together as close as possible to the device.

RECORD ($\overline{REC}$)

The $\overline{REC}$ input is an active-LOW record signal. The device records whenever $\overline{REC}$ is LOW. This signal must remain LOW for the duration of the recording. $\overline{REC}$ takes precedence over either playback ($\overline{PLAYE}$ or PLAYL) signal. If $\overline{REC}$ is pulled LOW during a playback cycle, the playback immediately ceases and recording begins.

A record cycle is completed when $\overline{REC}$ is pulled HIGH or the memory space is filled.

An end-of-message marker (EOM) is internally recorded, enabling a subsequent playback cycle to terminate appropriately. The device automatically powers down to standby mode when $\overline{REC}$ goes HIGH.

PLAYBACK, EDGE-ACTIVATED ($\overline{PLAYE}$)

When a LOW-going transition is detected on this input signal, a playback cycle begins. Playback continues until an EOM is encountered or the end of the memory space is reached. Upon completion of the playback cycle, the device automatically powers down into standby mode. Taking $\overline{PLAYE}$ HIGH during a playback cycle will not terminate the current cycle.

PLAYBACK, LEVEL-ACTIVATED (PLAYL)

When this input signal transitions from HIGH to LOW, a playback cycle is initiated. Playback continues until PLAYL is pulled HIGH, an EOM marker is detected, or the end of the memory space is reached. The device automatically powers down to standby mode upon completion of the playback cycle.

NOTE *In playback, if either $\overline{PLAYE}$ or PLAYL is held LOW during EOM or OVF, the device will still enter standby and the internal oscillator and timing generator will stop. However, the rising edge of $\overline{PLAYE}$ and PLAYL are not debounced and any subsequent falling edge (particularly switch bounce) present on the input pins will initiate another playback.*

RECORD LED OUTPUT ($\overline{\text{RECLED}}$)

The output $\overline{\text{RECLED}}$ is LOW during a record cycle. It can be used to drive an LED to provide feedback that a record cycle is in progress. In addition, $\overline{\text{RECLED}}$ pulses LOW momentarily when an EOM is encountered in a playback cycle.

MICROPHONE INPUT (MIC)

The microphone input transfers its signal to the on-chip preamplifier. An on-chip Automatic Gain Control (AGC) circuit controls the gain of this preamplifier from –15 to 24 dB. An external microphone should be AC coupled to this pin via a series capacitor. The capacitor value, together with the internal 10 KΩ resistance on this pin, determine the low-frequency cutoff for the ISD1400 series passband. See Application Information for additional information on low-frequency cutoff calculations.

MICROPHONE REFERENCE (MIC REF)

The MIC REF input is the inverting input to the microphone preamplifier. This provides a noise-canceling or common-mode rejection input to the device when connected differentially to a microphone.

AUTOMATIC GAIN CONTROL (AGC)

The AGC dynamically adjusts the gain of the preamplifier to compensate for the wide range of microphone input levels. The AGC allows the full range of sound, from whispers to loud sounds, to be recorded with minimal distortion. The "attack" time is determined by the time constant of a 5 KΩ internal resistance and an external capacitor (C6 on the schematic in Figure 4) connected from the AGC pin to V_{SSA} analog ground. The "release" time is determined by the time constant of an external resistor (R5) and an external capacitor (C6) connected in parallel between the AGC Pin and V_{SSA} analog ground. Nominal values of 470 KΩ and 4.7 µF give satisfactory results in most cases.

ANALOG OUTPUT (ANA OUT)

This pin provides the preamplifier output to the user. The voltage gain of the preamplifier is determined by the voltage level at the AGC pin.

ANALOG INPUT (ANA IN)

The ANA IN pin transfers the input signal to the chip for recording. For microphone inputs, the ANA OUT pin should be connected via an external capacitor to the ANA IN pin. This capacitor value, together with the 3.0 KΩ input impedance of ANA IN, is selected to give additional cutoff at the low-frequency end of the voice passband. If the desired input is derived from a source other than a microphone, the signal can be fed, capacitively coupled, into the ANA IN pin directly.

EXTERNAL CLOCK INPUT (XCLK)

The external clock input for the ISD1400 devices has an internal pull-down device. The ISD1400 is configured at the factory with an internal sampling clock frequency that guarantees its minimum nominal record/playback time. For instance, an ISD1420 operating within specification will be observed to always have a minimum of 20 seconds of recording time. The sampling frequency is then maintained to a variation of ±2.25 percent over the commercial temperature and operating voltage ranges, while still maintaining the minimum specified recording duration. This will result in some devices having a few percent more than nominal recording time.

The internal clock has a ±5 percent tolerance over the industrial temperature and voltage range. A regulated power supply is recommended for industrial temperature parts. If greater precision is required, the device can be clocked through the XCLK pin as follows:

Table 2: External Clock Sample Rates

Part Number	Sample Rate	Required Clock
ISD1416	8.0 KHz	1024 KHz
ISD1420	6.4 KHz	819.2 KHz

These recommended clock rates should not be varied because the antialiasing and smoothing filters are fixed, and aliasing problems can occur if the sample rate differs from the one recommended. The duty cycle on the input clock is not critical, as the clock is immediately divided by two internally. **If the XCLK is not used, this input should be connected to ground.**

SPEAKER OUTPUTS (SP+, SP–)

The SP+ and SP– pins provide direct drive for loudspeakers with impedances as low as 16 Ω. A single output may be used, but, for direct-drive loudspeakers, the two opposite-polarity outputs provide an improvement in output power of up to four times over a single-ended connection. Furthermore, when SP+ and SP– are used, a speaker-coupling capacitor is not required. A single-ended connection will require an AC-coupling capacitor between the SP pin and the speaker. The speaker outputs are in a high-impedance state during a record cycle, and held at V_{SSA} during power down.

ADDRESS INPUTS (A0–A7)

The Address inputs have two functions, depending upon the level of the two Most Significant Bits (MSB) of the address.

If either of the two MSBs is LOW, the inputs are all interpreted as address bits and are used as the start address for the current record or playback cycle. The address pins are inputs only and do not output internal address information as the operation progresses. Address inputs are latched by the falling edge of PLAYE, PLAYL, or REC.

OPERATIONAL MODES

The ISD1400 series is designed with several built-in operational modes provided to allow maximum functionality with a minimum of additional components, described in detail below. The operational modes use the address pins on the ISD1400 devices, but are mapped outside the valid address range. When the two Most Significant Bits (MSBs) are HIGH (A6 and A7), the remaining address signals are interpreted as mode bits and not as address bits. Therefore, operational modes and direct addressing are not compatible and cannot be used simultaneously.

There are two important considerations for using operational modes. First, all operations begin initially at address 0, which is the beginning of the ISD1400 address space. Later operations can begin at other address locations, depending on the operational mode(s) chosen. In addition, the address pointer is reset to 0 when the device is changed from record to playback but not from playback to record when A4 is HIGH in Operational Mode.

Second, an Operational Mode is executed when any of the control inputs, PLAYE, PLAYL, or REC, go LOW and the two MSBs are HIGH. This Operational Mode remains in effect until the next LOW-going control input signal, at which point the current address/mode levels are sampled and executed.

NOTE *The two MSBs are on pins 9 and 10 for each ISD1400 series device.*

OPERATIONAL MODES DESCRIPTION

The Operational Modes can be used in conjunction with a microcontroller, or they can be hard-wired to provide the desired system operation.

A0 — MESSAGE CUEING

Message Cueing allows the user to skip through messages, without knowing the actual physical addresses of each message. Each control input LOW pulse causes the internal address pointer to skip to the next message. This mode should be used for playback only, and is typically used with the A4 Operational Mode.

A1 — DELETE $\overline{\text{EOM}}$ MARKERS

The A1 Operational Mode allows sequentially recorded messages to be combined into a single message with only one EOM marker set at the end of the final message. When this operational mode is configured, messages recorded sequentially are played back as one continuous message.

A2 — UNUSED

A3 — MESSAGE LOOPING

The A3 Operational Mode allows for the automatic, continuously repeated playback of the message located at the beginning of the address space.

A message can completely fill the ISD1400 device and will loop from beginning to end. Pulsing $\overline{\text{PLAYE}}$ will start the playback and pulsing $\overline{\text{PLAYL}}$ will end the playback.

A4 — CONSECUTIVE ADDRESSING

During normal operations, the address pointer will reset when a message is played through to an EOM marker. The A4 Operational Mode inhibits the address pointer reset, allowing messages to be recorded or played back consecutively. When the device is in a static state; i.e., not recording or playing back, momentarily taking this pin LOW will reset the address counter to zero.

A5 — UNUSED

Table 3: Operational Modes Table

Address Ctrl. (HIGH)	Function	Typical Use	Jointly Compatible[1]
A0	Message cueing	Fast-forward through messages	A4
A1	Delete EOM markers	Position EOM marker at the end of the last message	A3, A4
A2	Unused		
A3	Looping	Continuous playback from Address 0	A1
A4	Consecutive addressing	Record/play multiple consecutive messages	A0, A1
A5	Unused		

1. *Additional operational modes can be used simultaneously with the given mode.*

TIMING DIAGRAMS

Figure 2: Record

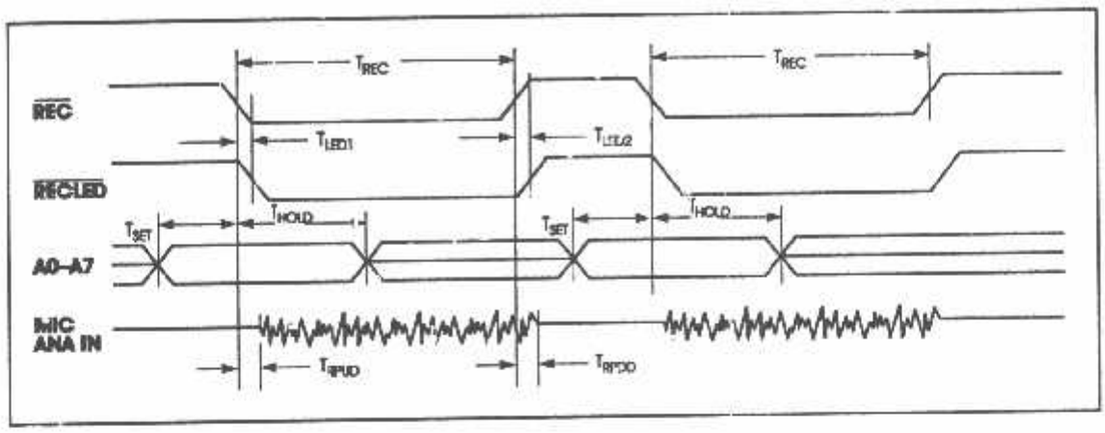
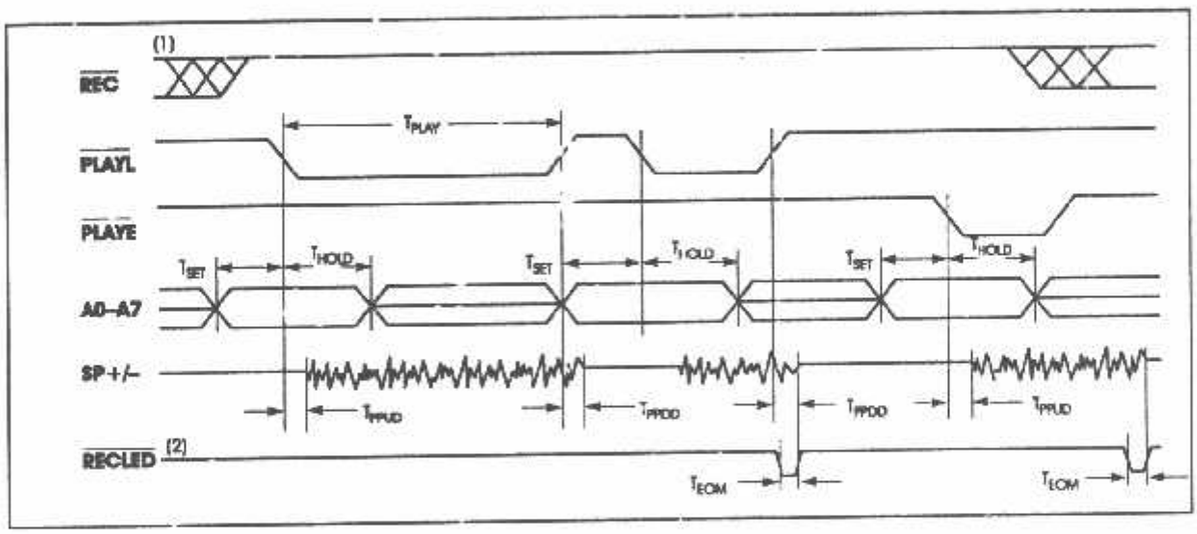


Figure 3: Playback



1. *REC must be HIGH for the entire duration of a playback cycle.*
2. *RECLED functions as an EOM during playback.*

Table 4: Absolute Maximum Ratings (Packaged Parts)[1]

Condition	Value
Junction temperature	150°C
Storage temperature range	–65°C to +150°C
Voltage applied to any pin	(V_{SS} – 0.3 V) to (V_{CC} + 0.3 V)
Voltage applied to any pin (input current limited to ±20 mA)	(V_{SS} – 1.0 V) to (V_{CC} + 1.0 V)
Lead temperature (soldering – 10 seconds)	300°C
$V_{CC} - V_{SS}$	–0.3 V to +7.1 V

1. *Stresses above those listed may cause permanent damage to the device. Exposure to the absolute maximum ratings may affect device reliability. Functional operation is not implied at these conditions.*

Table 5: Operating Conditions (Packaged Parts)

Condition	Value
Commercial operating temperature range[1]	0°C to +70°C
Industrial operating temperature[1]	–40°C to +85°C
Supply voltage (V_{CC})[2]	+4.5 V to +5.5 V
Ground voltage (V_{SS})[3]	0 V

1. *Case temperature.*
2. $V_{CC} = V_{CCA} = V_{CCD}$
3. $V_{SS} = V_{SSA} = V_{SSD}$

Table 6: DC Parameters (Packaged Parts)

Symbol	Parameters	Min[2]	Typ[1]	Max[2]	Units	Conditions
V_{IL}	Input Low Voltage			0.8	V	
V_{IH}	Input High Voltage	2.4			V	
V_{OL}	Output Low Voltage			0.4	V	I_{OL} = 4.0 mA
V_{OH}	Output High Voltage	2.4			V	I_{OH} = –1.6 mA
I_{CC}	V_{CC} Current (Operating)		15	30	mA	V_{CC} = 5.5 V[3], R_{EXT} = ∞
I_{SB}	V_{CC} Current (Standby)		0.5	10	µA	[3] [4]
I_{IL}	Input Leakage Current			±1	µA	
I_{ILPD}	Input Current HIGH w/Pull Down			130	µA	Force V_{CC}[5]
R_{EXT}	Output Load Impedance	16			Ω	Speaker Load
R_{MIC}	Preamp In Input Resistance	4	9	17	KΩ	Pins 17, 18
$R_{ANA\ IN}$	ANA IN Input Resistance	2.5	3	5	KΩ	
A_{PRE1}	Preamp Gain 1	20	23	26	dB	AGC = 0.0 V
A_{PRE2}	Preamp Gain 2		–45	–15	dB	AGC = 2.5 V

Table 6: DC Parameters (Packaged Parts)

Symbol	Parameters	Min(2)	Typ (1)	Max(2)	Units	Conditions
A_{ARP}	ANA IN to SP+/– Gain	20	22	25	dB	
R_{AGC}	AGC Output Resistance	2.5	5	9.5	KΩ	
I_{PREH}	Preamp Out Source		–2		mA	@ V_{OUT} = 1.0 V
I_{PREL}	Preamp In Sink		0.5		mA	@ V_{OUT} = 2.0 V

1. *Typical values @ T_A = 25°C and 5.0 V.*
2. *All Min/Max limits are guaranteed by ISD via electrical testing or characterization. Not all specifications are 100 percent tested.*
3. *V_{CCA} and V_{CCD} connected together.*
4. *$\overline{REC}$, $\overline{PLAYL}$, and $\overline{PLAYE}$ must be at V_{CCD}.*
5. *XCLK pin.*

Table 7: AC Parameters (Packaged Parts)

Symbol	Characteristic		Min(2)	Typ (1)	Max(2)	Units	Conditions
F_S	Sampling Frequency	ISD1416 ISD1420			8 6.4	KHz KHz	(5) (5)
F_{CF}	Filter Pass Band	ISD1416 ISD1420		3.3 2.6		KHz KHz	3 dB Roll-Off Point (3)(6) 3 dB Roll-Off Point (3)(6)
T_{REC}	Record Duration	ISD1416 ISD1420	16 20			sec sec	
T_{PLAY}	Playback Duration	ISD1416 ISD1420	16 20			sec sec	(5) (5)
T_{LED1}	$\overline{RECLED}$ ON Delay			5		msec	
T_{LED2}	$\overline{RECLED}$ OFF Delay	ISD1416 ISD1420	30 40	38.9 48.6	95 110	msec msec	
T_{SET}	Address Setup Time		300			nsec	
T_{HOLD}	Address Hold Time		0			nsec	
T_{RPUD}	Record Power-Up Delay	ISD1416 ISD1420		26 32		msec msec	
T_{RPDD}	Record Power-Down Delay	ISD1416 ISD1420		26 32		msec msec	
T_{PPUD}	Play Power-Up Delay	ISD1416 ISD1420		26 32		msec msec	

Table 7: AC Parameters (Packaged Parts)

Symbol	Characteristic		Min[2]	Typ [1]	Max[2]	Units	Conditions
T_{PDD}	Play Power-Down Delay	ISD1416 ISD1420		6.5 8.1		msec msec	
T_{EOM}	EOM Pulse Width	ISD1416 ISD1420		12.5 15.625		msec msec	
THD	Total Harmonic Distortion			1	3	%	@ 1 KHz
P_{OUT}	Speaker Output Power			12.2		mW	R_{EXT} = 16 Ω
V_{OUT}	Voltage Across Speaker Pins			1.25	2.5	V p-p	R_{EXT} = 600 Ω
V_{IN1}	MIC Input Voltage				20	mV	Peak-to-Peak [4]
V_{IN2}	ANA IN Input Voltage				50	mV	Peak-to-Peak

1. *Typical values @ T_A = 25°C and 5.0 V.*
2. *All Min/Max limits are guaranteed by ISD via electrical testing or characterization. Not all specifications are 100 percent tested.*
3. *Low-frequency cutoff depends upon value of external capacitors (see Pin Descriptions).*
4. *With 5.1 KΩ series resistor at ANA IN.*
5. *Sampling frequency and playback duration will vary as much as ±2.25 percent over the commercial temperature and voltage ranges. It may vary as much as ±5 percent over the industrial temperature and voltage ranges. All devices will meet the maximum sampling frequency and minimum playback duration parameters. For greater stability, an external clock can be utilized (see Pin Descriptions).*
6. *Filter specification applies to the antialiasing filter and to the smoothing filter.*

TYPICAL PARAMETER VARIATION WITH VOLTAGE AND TEMPERATURE (PACKAGED PARTS)

Chart 1: Record Mode Operating Current (I_{CC})

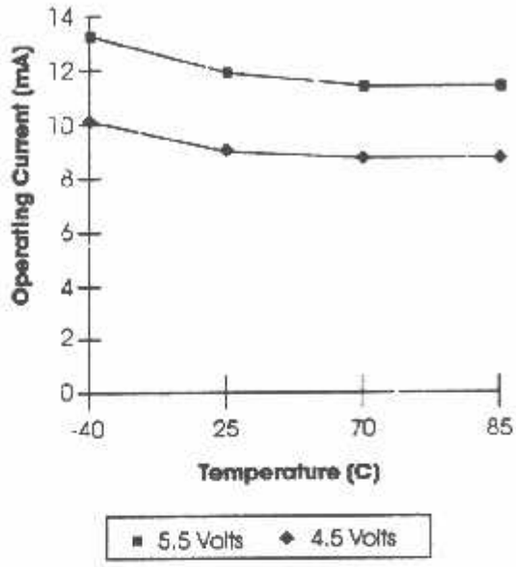


Chart 2: Total Harmonic Distortion

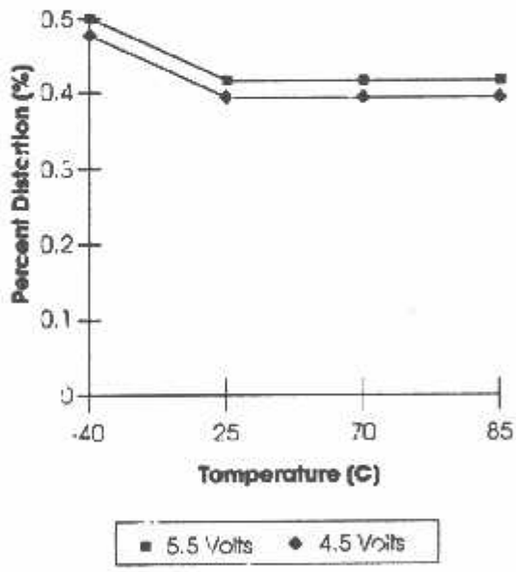


Chart 3: Standby Current (I_{SB})

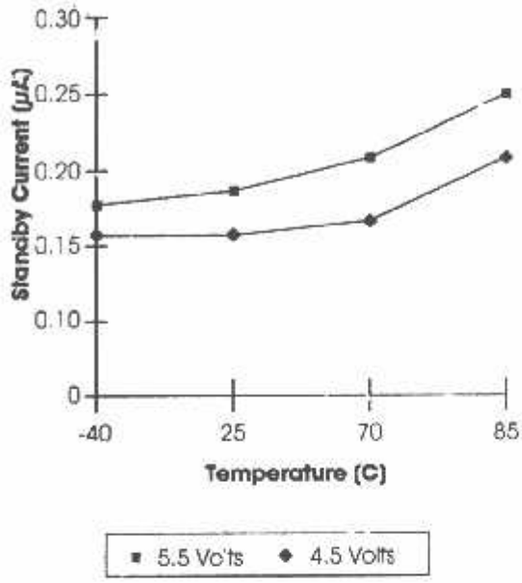
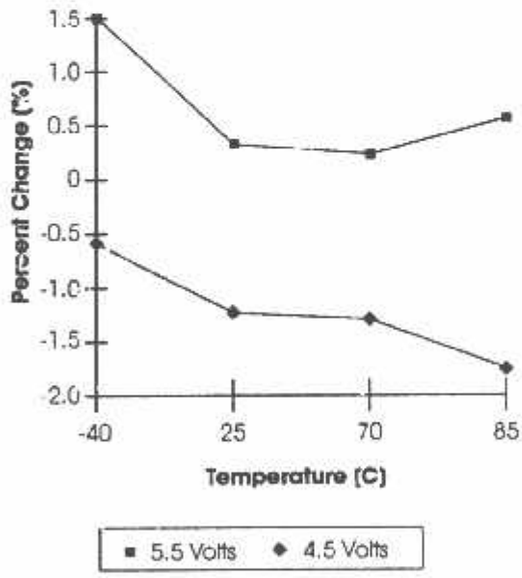


Chart 4: Oscillator Stability



Features

- Compatible with MCS®51 Products
- 8K Bytes of In-System Reprogrammable Downloadable Flash Memory
  - SPI Serial Interface for Program Downloading
  - Endurance: 1,000 Write/Erase Cycles
- 2K Bytes EEPROM
  - Endurance: 100,000 Write/Erase Cycles
- 4V to 6V Operating Range
- Fully Static Operation: 0 Hz to 24 MHz
- Three-level Program Memory Lock
- 256 x 8-bit Internal RAM
- 32 Programmable I/O Lines
- Three 16-bit Timer/Counters
- Nine Interrupt Sources
- Programmable UART Serial Channel
- SPI Serial Interface
- Low-power Idle and Power-down Modes
- Interrupt Recovery from Power-down
- Programmable Watchdog Timer
- Dual Data Pointer
- Power-off Flag

Description

The AT89S8252 is a low-power, high-performance CMOS 8-bit microcontroller with 8K bytes of downloadable Flash programmable and erasable read-only memory and 2K bytes of EEPROM. The device is manufactured using Atmel's high-density nonvolatile memory technology and is compatible with the industry-standard 80C51 instruction set and pinout. The on-chip downloadable Flash allows the program memory to be reprogrammed In-System through an SPI serial interface or by a conventional nonvolatile memory programmer. By combining a versatile 8-bit CPU with downloadable Flash on a monolithic chip, the Atmel AT89S8252 is a powerful microcontroller, which provides a highly-flexible and cost-effective solution to many embedded control applications.

The AT89S8252 provides the following standard features: 8K bytes of downloadable Flash, 2K bytes of EEPROM, 256 bytes of RAM, 32 I/O lines, programmable watchdog timer, two data pointers, three 16-bit timer/counters, a six-vector two-level interrupt architecture, a full duplex serial port, on-chip oscillator, and clock circuitry. In addition, the AT89S8252 is designed with static logic for operation down to zero frequency and supports two software selectable power saving modes. The Idle Mode stops the CPU while allowing the RAM, timer/counters, serial port, and interrupt system to continue functioning. The Power-down mode saves the RAM contents but freezes the oscillator, disabling all other chip functions until the next external interrupt or hardware reset.

The downloadable Flash can be changed a single byte at a time and is accessible through the SPI serial interface. Holding RESET active forces the SPI bus into a serial programming interface and allows the program memory to be written to or read from unless lock bits have been activated.

8-bit Microcontroller with 8K Bytes Flash

AT89S8252

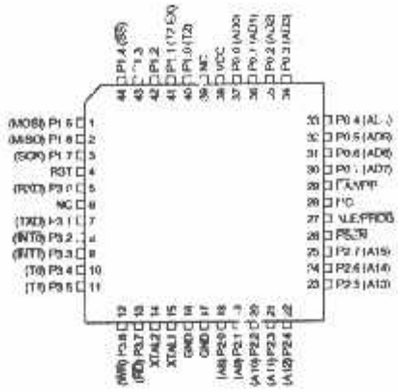
Not Recommended for New Designs. Use AT89S8253.

0401G–MICRO–3/06

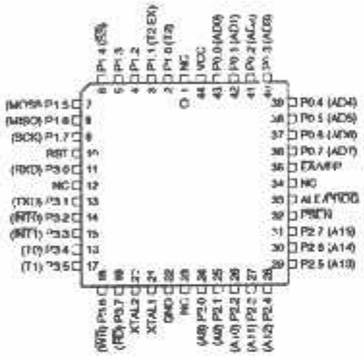
Pin Configurations

PDIP

TQFP



PLCC



Pin Description

VCC Supply voltage.

GND Ground.

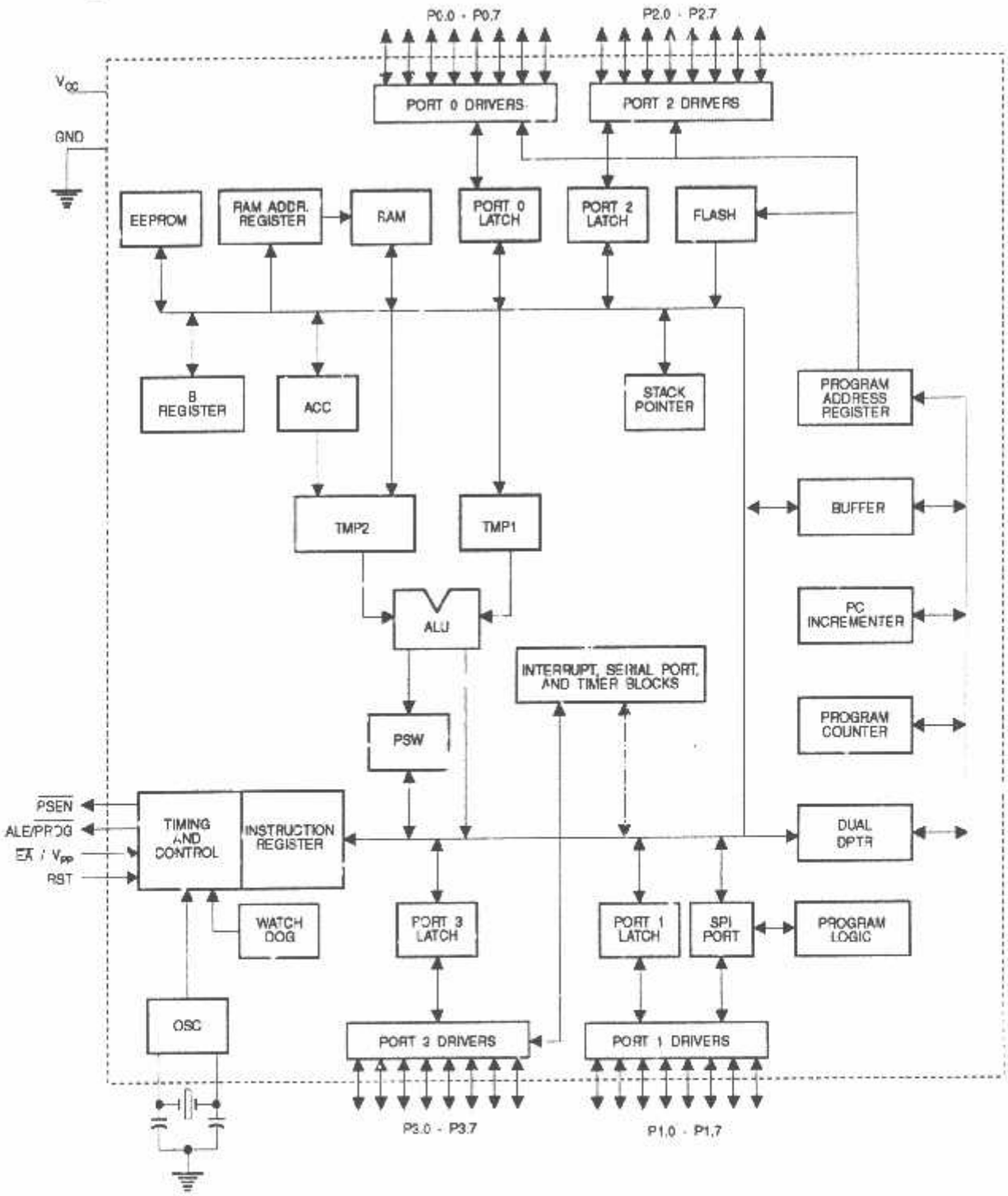
Port 0 Port 0 is an 8-bit open drain bi-didirectional I/O port. As an output port, each pin can sink eight TTL inputs. When 1s are written to port 0 pins, the pins can be used as high-impedance inputs.

Port 0 can also be configured to be the multiplexed low-order address/data bus during accesses to external program and data memory. In this mode, P0 has internal pull-ups.

Port 0 also receives the code bytes during Flash programming and outputs the code bytes during program verification. External pull-ups are required during program verification.

Port 1 Port 1 is an 8-bit bi-directional I/O port with internal pull-ups. The Port 1 output buffers can sink/source four TTL inputs. When 1s are written to Port 1 pins, they are pulled high by the internal pull-ups and can be used as inputs. As inputs, Port 1 pins that are externally being pulled low will source current (I_{IL}) because of the internal pull-ups.

Block Diagram



Some Port 1 pins provide additional functions. P1.0 and P1.1 can be configured to be the timer/counter 2 external count input (P1.0/T2) and the timer/counter 2 trigger input (P1.1/T2EX), respectively.

Furthermore, P1.4, P1.5, P1.6, and P1.7 can be configured as the SPI slave port select, data input/output and shift clock input/output pins as shown in the following table.

Port Pin	Alternate Functions
P1.0	T2 (external count input to Timer/Counter 2), clock-out
P1.1	T2EX (Timer/Counter 2 capture/reload trigger and direction control)
P1.4	$\overline{SS}$ (Slave port select input)
P1.5	MOSI (Master data output, slave data input pin for SPI channel)
P1.6	MISO (Master data input, slave data output pin for SPI channel)
P1.7	SCK (Master clock output, slave clock input pin for SPI channel)

Port 1 also receives the low-order address bytes during Flash programming and verification.

Port 2

Port 2 is an 8-bit bi-directional I/O port with internal pull-ups. The Port 2 output buffers can sink/source four TTL inputs. When 1s are written to Port 2 pins, they are pulled high by the internal pull-ups and can be used as inputs. As inputs, Port 2 pins that are externally being pulled low will source current (I_{IL}) because of the internal pull-ups.

Port 2 emits the high-order address byte during fetches from external program memory and during accesses to external data memory that use 16-bit addresses (MOVX @ DPTR). In this application, Port 2 uses strong internal pull-ups when emitting 1s. During accesses to external data memory that use 8-bit addresses (MOVX @ RI), Port 2 emits the contents of the P2 Special Function Register.

Port 2 also receives the high-order address bits and some control signals during Flash programming and verification.

Port 3

Port 3 is an 8-bit bi-directional I/O port with internal pull-ups. The Port 3 output buffers can sink/source four TTL inputs. When 1s are written to Port 3 pins, they are pulled high by the internal pull-ups and can be used as inputs. As inputs, Port 3 pins that are externally being pulled low will source current (I_{IL}) because of the pull-ups.

Port 3 receives some control signals for Flash programming and verification.

Port 3 also serves the functions of various special features of the AT89S8252, as shown in the following table.

Port Pin	Alternate Functions
P3.0	RXD (serial input port)
P3.1	TXD (serial output port)
P3.2	$\overline{INT0}$ (external interrupt 0)
P3.3	$\overline{INT1}$ (external interrupt 1)
P3.4	T0 (timer 0 external input)
P3.5	T1 (timer 1 external input)
P3.6	$\overline{WR}$ (external data memory write strobe)
P3.7	$\overline{RD}$ (external data memory read strobe)

RST

Reset input. A high on this pin for two machine cycles while the oscillator is running resets the device.

ALE/$\overline{PROG}$

Address Latch Enable is an output pulse for latching the low byte of the address during accesses to external memory. This pin is also the program pulse input ($\overline{PROG}$) during Flash programming.

In normal operation, ALE is emitted at a constant rate of 1/6 the oscillator frequency and may be used for external timing or clocking purposes. Note, however, that one ALE pulse is skipped during each access to external data memory.

If desired, ALE operation can be disabled by setting bit 0 of SFR location 8EH. With the bit set, ALE is active only during a MOVX or MOVC instruction. Otherwise, the pin is weakly pulled high. Setting the ALE-disable bit has no effect if the microcontroller is in external execution mode.

$\overline{PSEN}$

Program Store Enable is the read strobe to external program memory.

When the AT89S8252 is executing code from external program memory, $\overline{PSEN}$ is activated twice each machine cycle, except that two $\overline{PSEN}$ activations are skipped during each access to external data memory.

$\overline{EA}$/VPP

External Access Enable. $\overline{EA}$ must be strapped to GND in order to enable the device to fetch code from external program memory locations starting at 0000H up to FFFFH. Note, however, that if lock bit 1 is programmed, $\overline{EA}$ will be internally latched on reset.

$\overline{EA}$ should be strapped to V_{CC} for internal program executions. This pin also receives the 12-volt programming enable voltage (V_{PP}) during Flash programming when 12-volt programming is selected.

XTAL1

Input to the inverting oscillator amplifier and input to the internal clock operating circuit.

XTAL2

Output from the inverting oscillator amplifier.

Special Function Registers

A map of the on-chip memory area called the Special Function Register (SFR) space is shown in Table 1.

Note that not all of the addresses are occupied, and unoccupied addresses may not be implemented on the chip. Read accesses to these addresses will in general return random data, and write accesses will have an indeterminate effect.

User software should not write 1s to these unlisted locations, since they may be used in future products to invoke new features. In that case, the reset or inactive values of the new bits will always be 0.

Timer 2 Registers Control and status bits are contained in registers T2CON (shown in Table 2) and T2MOD (shown in Table 9) for Timer 2. The register pair (RCAP2H, RCAP2L) are the Capture/Reload registers for Timer 2 in 16-bit capture mode or 16-bit auto-reload mode.

Table 1. AT89S8252 SFR Map and Reset Values

0F8H									0FFH
0F0H	B 00000000								0F7H
0E8H									0EFH
0E0H	ACC 00000000								0E7H
0D8H									0DFH
0D0H	PSW 00000000					SPCR 000001XX			0D7H
0C8H	T2CON 00000000	T2MOD XXXXXX00	RCAP2L 00000000	RCAP2H 00000000	TL2 00000000	TH2 00000000			0CFH
0C0H									0C7H
0B8H	IP XX000000								0BFH
0B0H	P3 11111111								0B7H
0A8H	IE 0X000000		SPSR 00XXXXXX						0AFH
0A0H	P2 11111111								0A7H
98H	SCON 00000000	SBUF XXXXXXXX							9FH
90H	P1 11111111						WMCON 00000010		97H
88H	TCON 00000000	TMOD 00000000	TL0 00000000	TL1 00000000	TH0 00000000	TH1 00000000			8FH
80H	P0 11111111	SP 00000111	DP0L 00000000	DP0H 00000000	DP1L 00000000	DP1H 00000000	SPDR XXXXXXXX	PCON 00XX0000	87H

Table 2. T2CON – Timer/Counter 2 Control Register

T2CON Address = 0C8H — Reset Value = 0000 0000B

Bit Addressable

Bit	TF2	EXF2	RCLK	TCLK	EXEN2	TR2	C/$\overline{T2}$	CP/$\overline{RL2}$
	7	6	5	4	3	2	1	0

Symbol	Function
TF2	Timer 2 overflow flag set by a Timer 2 overflow and must be cleared by software. TF2 will not be set when either RCLK = 1 or TCLK = 1.
EXF2	Timer 2 external flag set when either a capture or reload is caused by a negative transition on T2EX and EXEN2 = 1. When Timer 2 interrupt is enabled, EXF2 = 1 will cause the CPU to vector to the Timer 2 interrupt routine. EXF2 must be cleared by software. EXF2 does not cause an interrupt in up/down counter mode (DCEN = 1).
RCLK	Receive clock enable. When set, causes the serial port to use Timer 2 overflow pulses for its receive clock in serial port Modes 1 and 3. RCLK = 0 causes Timer 1 overflows to be used for the receive clock.
TCLK	Transmit clock enable. When set, causes the serial port to use Timer 2 overflow pulses for its transmit clock in serial port Modes 1 and 3. TCLK = 0 causes Timer 1 overflows to be used for the transmit clock.
EXEN2	Timer 2 external enable. When set, allows a capture or reload to occur as a result of a negative transition on T2EX if Timer 2 is not being used to clock the serial port. EXEN2 = 0 causes Timer 2 to ignore events at T2EX.
TR2	Start/Stop control for Timer 2. TR2 = 1 starts the timer.
C/$\overline{T2}$	Timer or counter select for Timer 2. C/$\overline{T2}$ = 0 for timer function. C/$\overline{T2}$ = 1 for external event counter (falling edge triggered).
CP/$\overline{RL2}$	Capture/Reload select. CP/$\overline{RL2}$ = 1 causes captures to occur on negative transitions at T2EX if EXEN2 = 1. CP/$\overline{RL2}$ = 0 causes automatic reloads to occur when Timer 2 overflows or negative transitions occur at T2EX when EXEN2 = 1. When either RCLK or TCLK = 1, this bit is ignored and the timer is forced to auto-reload on Timer 2 overflow.

Watchdog and Memory Control Register The WMCON register contains control bits for the Watchdog Timer (shown in Table 3). The EEMEN and EEMWE bits are used to select the 2K bytes on-chip EEPROM, and to enable byte-write. The DPS bit selects one of two DPTR registers available.

Table 3. WMCON—Watchdog and Memory Control Register

WMCON Address = 96H — Reset Value = 0000 0010B

	PS2	PS1	PS0	EEMWE	EEMEN	DPS	WDTRST	WDTEN
Bit	7	6	5	4	3	2	1	0

Symbol	Function
PS2 PS1 PS0	Prescaler Bits for the Watchdog Timer. When all three bits are set to "0", the watchdog timer has a nominal period of 16 ms. When all three bits are set to "1", the nominal period is 2048 ms.
EEMWE	EEPROM Data Memory Write Enable Bit. Set this bit to "1" before initiating byte write to on-chip EEPROM with the MOVX instruction. User software should set this bit to "0" after EEPROM write is completed.
EEMEN	Internal EEPROM Access Enable. When EEMEN = 1, the MOVX instruction with DPTR will access on-chip EEPROM instead of external data memory. When EEMEN = 0, MOVX with DPTR accesses external data memory.
DPS	Data Pointer Register Select. DPS = 0 selects the first bank of Data Pointer Register, DP0, and DPS = 1 selects the second bank, DP1
WDTRST RDY/$\overline{BSY}$	Watchdog Timer Reset and EEPROM Ready/$\overline{Busy}$ Flag. Each time this bit is set to "1" by user software, a pulse is generated to reset the watchdog timer. The WDTRST bit is then automatically reset to "0" in the next instruction cycle. The WDTRST bit is Write-Only. This bit also serves as the RDY/$\overline{BSY}$ flag in a Read-Only mode during EEPROM write. RDY/$\overline{BSY}$ = 1 means that the EEPROM is ready to be programmed. While programming operations are being executed, the RDY/$\overline{BSY}$ bit equals "0" and is automatically reset to "1" when programming is completed.
WDTEN	Watchdog Timer Enable Bit. WDTEN = 1 enables the watchdog timer and WDTEN = 0 disables the watchdog timer.

SPI Registers Control and status bits for the Serial Peripheral Interface are contained in registers SPCR (shown in Table 4) and SPSR (shown in Table 5). The SPI data bits are contained in the SPDR register. Writing the SPI data register during serial data transfer sets the Write Collision bit, WCOL, in the SPSR register. The SPDR is double buffered for writing and the values in SPDR are not changed by Reset.

Interrupt Registers The global interrupt enable bit and the individual interrupt enable bits are in the IE register. In addition, the individual interrupt enable bit for the SPI is in the SPCR register. Two priorities can be set for each of the six interrupt sources in the IP register.

Dual Data Pointer Registers To facilitate accessing both internal EEPROM and external data memory, two banks of 16-bit Data Pointer Registers are provided: DP0 at SFR address locations 82H-83H and DP1 at 84H-85H. Bit DPS = 0 in SFR WMCON selects DP0 and DPS = 1 selects DP1. The user should **ALWAYS** initialize the DPS bit to the appropriate value before accessing the respective Data Pointer Register.

Power Off Flag The Power Off Flag (POF) is located at bit_4 (PCON.4) in the PCON SFR. POF is set to "1" during power up. It can be set and reset under software control and is not affected by RESET.

Table 4. SPCR – SPI Control Register

SPCR Address = D5H — Reset Value = 0000 01XXB

Bit	SPIE	SPE	DORD	MSTR	CPOL	CPHA	SPR1	SPR0
	7	6	5	4	3	2	1	0

Symbol	Function
SPIE	SPI Interrupt Enable. This bit, in conjunction with the ES bit in the IE register, enables SPI interrupts: SPIE = 1 and ES = 1 enable SPI interrupts. SPIE = 0 disables SPI interrupts.
SPE	SPI Enable. SPI = 1 enables the SPI channel and connects $\overline{SS}$, MOSI, MISO and SCK to pins P1.4, P1.5, P1.6, and P1.7. SPI = 0 disables the SPI channel.
DORD	Data Order. DORD = 1 selects LSB first data transmission. DORD = 0 selects MSB first data transmission.
MSTR	Master/Slave Select. MSTR = 1 selects Master SPI mode. MSTR = 0 selects Slave SPI mode.
CPOL	Clock Polarity. When CPOL = 1, SCK is high when idle. When CPOL = 0, SCK of the master device is low when not transmitting. Please refer to figure on SPI Clock Phase and Polarity Control.
CPHA	Clock Phase. The CPHA bit together with the CPOL bit controls the clock and data relationship between master and slave. Please refer to figure on SPI Clock Phase and Polarity Control.
SPR0 SPR1	SPI Clock Rate Select. These two bits control the SCK rate of the device configured as master. SPR1 and SPR0 have no effect on the slave. The relationship between SCK and the oscillator frequency, F_{osc}, is as follows: SPR1 SPR0 SCK = F_{osc} divided by 0 0 4 0 1 16 1 0 64 1 1 128

Table 5. SPSR – SPI Status Register

SPSR Address = AAH — Reset Value = 00XX XXXXB

Bit	7	6	5	4	3	2	1	0
	SPIF	WCOL	–	–	–	–	–	–

Symbol	Function
SPIF	SPI Interrupt Flag. When a serial transfer is complete, the SPIF bit is set and an interrupt is generated if SPIE = 1 and ES = 1. The SPIF bit is cleared by reading the SPI status register with SPIF and WCOL bits set, and then reading/writing the SPI data register.
WCOL	Write Collision Flag. The WCOL bit is set if the SPI data register is written during a data transfer. During data transfer, the result of reading the SPDR register may be incorrect, and writing to it has no effect. The WCOL bit (and the SPIF bit) are cleared by reading the SPI status register with SPIF and WCOL set, and then accessing the SPI data register.

Table 6. SPDR – SPI Data Register

SPDR Address = 86H — Reset Value = unchanged

Bit	7	6	5	4	3	2	1	0
	SPD7	SPD6	SPD5	SPD4	SPD3	SPD2	SPD1	SPD0

Data Memory – EEPROM and RAM

The AT89S8252 implements 2K bytes of on-chip EEPROM for data storage and 256 bytes of RAM. The upper 128 bytes of RAM occupy a parallel space to the Special Function Registers. That means the upper 128 bytes have the same addresses as the SFR space but are physically separate from SFR space.

When an instruction accesses an internal location above address 7FH, the address mode used in the instruction specifies whether the CPU accesses the upper 128 bytes of RAM or the SFR space. Instructions that use direct addressing access SFR space.

For example, the following direct addressing instruction accesses the SFR at location 0A0H (which is P2).

```
MOV 0A0H, #data
```

Instructions that use indirect addressing access the upper 128 bytes of RAM. For example, the following indirect addressing instruction, where R0 contains 0A0H, accesses the data byte at address 0A0H, rather than P2 (whose address is 0A0H).

```
MOV @R0, #data
```

Note that stack operations are examples of indirect addressing, so the upper 128 bytes of data RAM are available as stack space.

The on-chip EEPROM data memory is selected by setting the EEMEN bit in the WMCON register at SFR address location 96H. The EEPROM address range is from 000H to 7FFH. The MOVX instructions are used to access the EEPROM. To access off-chip data memory with the MOVX instructions, the EEMEN bit needs to be set to "0".

The EEMWE bit in the WMCON register needs to be set to "1" before any byte location in the EEPROM can be written. User software should reset EEMWE bit to "0" if no further EEPROM write is required. EEPROM write cycles in the serial programming mode are self-timed and typically take 2.5 ms. The progress of EEPROM write can be monitored by reading the RDY/$\overline{BSY}$ bit (read-only) in SFR WMCON. RDY/$\overline{BSY}$ = 0 means

programming is still in progress and RDY/$\overline{BSY}$ = 1 means EEPROM write cycle is completed and another write cycle can be initiated.

In addition, during EEPROM programming, an attempted read from the EEPROM will fetch the byte being written with the MSB complemented. Once the write cycle is completed, true data are valid at all bit locations.

Programmable Watchdog Timer

The programmable Watchdog Timer (WDT) operates from an independent internal oscillator. The prescaler bits, PS0, PS1 and PS2 in SFR WMCON are used to set the period of the Watchdog Timer from 16 ms to 2048 ms. The available timer periods are shown in the following table and the actual timer periods (at V_{CC} = 5V) are within ±30% of the nominal.

The WDT is disabled by Power-on Reset and during Power-down. It is enabled by setting the WDTEN bit in SFR WMCON (address = 96H). The WDT is reset by setting the WDTRST bit in WMCON. When the WDT times out without being reset or disabled, an internal RST pulse is generated to reset the CPU.

Table 7. Watchdog Timer Period Selection

WDT Prescaler Bits			Period (nominal)
PS2	PS1	PS0	
0	0	0	16 ms
0	0	1	32 ms
0	1	0	64 ms
0	1	1	128 ms
1	0	0	256 ms
1	0	1	512 ms
1	1	0	1024 ms
1	1	1	2048 ms

Timer 0 and 1

Timer 0 and Timer 1 in the AT89S8252 operate the same way as Timer 0 and Timer 1 in the AT89C51 and AT89C52. For further information on the timers' operation, refer to the Atmel web site (http://www.atmel.com). From the home page, select "Products", then "Microcontrollers, then "8051-Architecture". Click on "Documentation", then on "Other Documents". Open the document "AT89 Series Hardware Description".

Timer 2

Timer 2 is a 16-bit Timer/Counter that can operate as either a timer or an event counter. The type of operation is selected by bit C/$\overline{T2}$ in the SFR T2CON (shown in Table 2). Timer 2 has three operating modes: capture, auto-reload (up or down counting), and baud rate generator. The modes are selected by bits in T2CON, as shown in Table 8.

Timer 2 consists of two 8-bit registers, TH2 and TL2. In the Timer function, the TL2 register is incremented every machine cycle. Since a machine cycle consists of 12 oscillator periods, the count rate is 1/12 of the oscillator frequency.

In the Counter function, the register is incremented in response to a 1-to-0 transition at its corresponding external input pin, T2. In this function, the external input is sampled during S5P2 of every machine cycle. When the samples show a high in one cycle and a low in the next cycle, the count is incremented. The new count value appears in the register during S3P1 of the cycle following the one in which the transition was detected.

Since two machine cycles (24 oscillator periods) are required to recognize a 1-to-0 transition, the maximum count rate is 1/24 of the oscillator frequency. To ensure that a given level is sampled at least once before it changes, the level should be held for at least one full machine cycle.

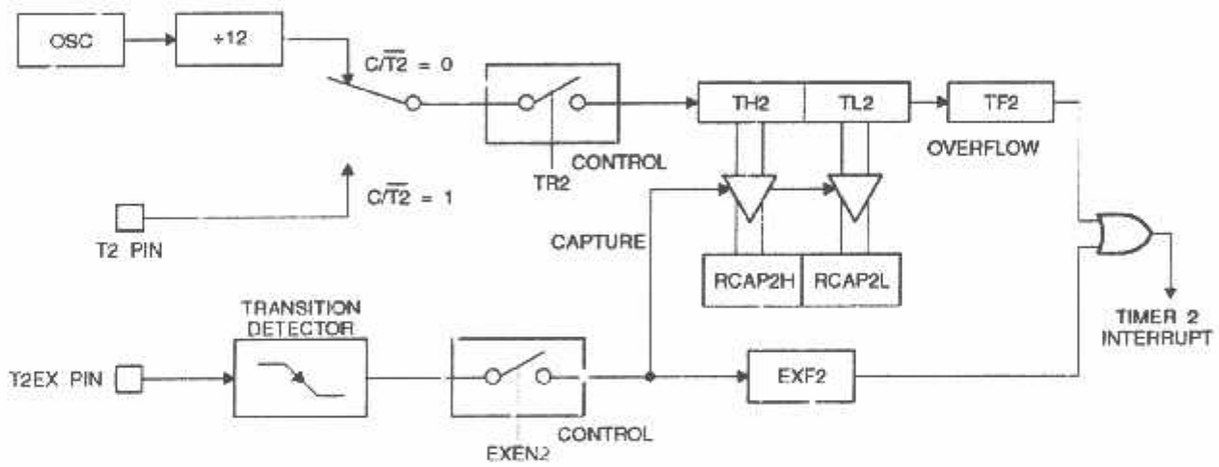
Table 8. Timer 2 Operating Modes

RCLK + TCLK	CP/$\overline{RL2}$	TR2	MODE
0	0	1	16-bit Auto-reload
0	1	1	16-bit Capture
1	X	1	Baud Rate Generator
X	X	0	(Off)

Capture Mode

In the capture mode, two options are selected by bit EXEN2 in T2CON. If EXEN2 = 0, Timer 2 is a 16-bit timer or counter which upon overflow sets bit TF2 in T2CON. This bit can then be used to generate an interrupt. If EXEN2 = 1, Timer 2 performs the same operation, but a 1-to-0 transition at external input T2EX also causes the current value in TH2 and TL2 to be captured into RCAP2H and RCAP2L, respectively. In addition, the transition at T2EX causes bit EXF2 in T2CON to be set. The EXF2 bit, like TF2, can generate an interrupt. The capture mode is illustrated in Figure 1.

Figure 1. Timer 2 in Capture Mode



Auto-reload (Up or Down Counter)

Timer 2 can be programmed to count up or down when configured in its 16-bit auto-reload mode. This feature is invoked by the DCEN (Down Counter Enable) bit located in the SFR T2MOD (see Table 9). Upon reset, the DCEN bit is set to 0 so that timer 2 will default to count up. When DCEN is set, Timer 2 can count up or down, depending on the value of the T2EX pin.

Figure 2 shows Timer 2 automatically counting up when DCEN = 0. In this mode, two options are selected by bit EXEN2 in T2CON. If EXEN2 = 0, Timer 2 counts up to 0FFFFH and then sets the TF2 bit upon overflow. The overflow also causes the timer registers to be reloaded with the 16-bit value in RCAP2H and RCAP2L. The values in RCAP2H and RCAP2L are preset by software. If EXEN2 = 1, a 16-bit reload can be triggered either by an overflow or by a 1-to-0 transition at external input T2EX. This transition also sets the EXF2 bit. Both the TF2 and EXF2 bits can generate an interrupt if enabled.

Setting the DCEN bit enables Timer 2 to count up or down, as shown in Figure 3. In this mode, the T2EX pin controls the direction of the count. A logic 1 at T2EX makes Timer 2 count up. The timer will overflow at 0FFFFH and set the TF2 bit. This overflow also causes the 16-bit value in RCAP2H and RCAP2L to be reloaded into the timer registers, TH2 and TL2, respectively.

A logic 0 at T2EX makes Timer 2 count down. The timer underflows when TH2 and TL2 equal the values stored in RCAP2H and RCAP2L. The underflow sets the TF2 bit and causes 0FFFFH to be reloaded into the timer registers.

The EXF2 bit toggles whenever Timer 2 overflows or underflows and can be used as a 17th bit of resolution. In this operating mode, EXF2 does not flag an interrupt.

Figure 2. Timer 2 in Auto Reload Mode (DCEN = 0)

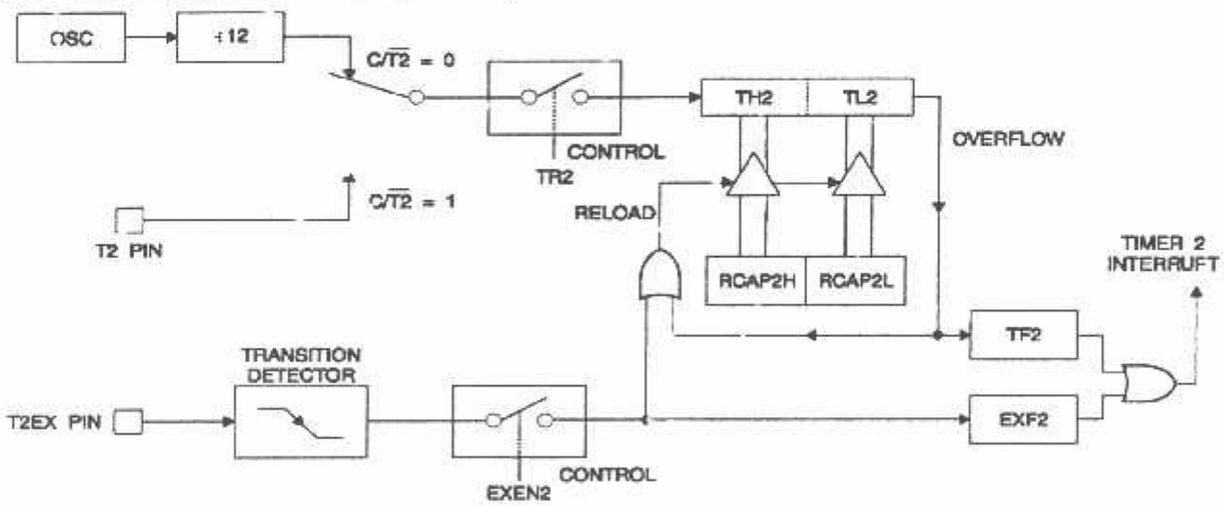


Table 9. T2MOD – Timer 2 Mode Control Register

T2MOD Address = 0C9H — Reset Value = XXXX XX00B

Not Bit Addressable

Bit	7	6	5	4	3	2	1	0
	–	–	–	–	–	–	T2OE	DCEN

Symbol	Function
–	Not implemented, reserved for future use.
T2OE	Timer 2 Output Enable bit.
DCEN	When set, this bit allows Timer 2 to be configured as an up/down counter.

Figure 3. Timer 2 Auto Reload Mode (DCEN = 1)

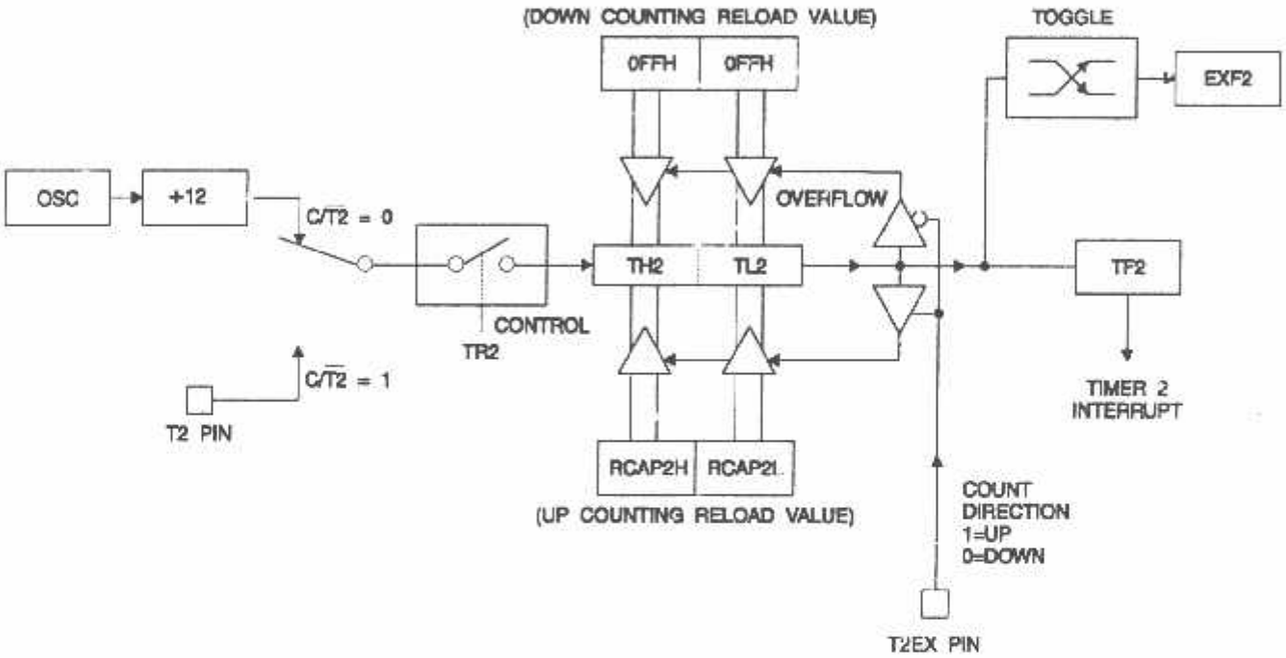
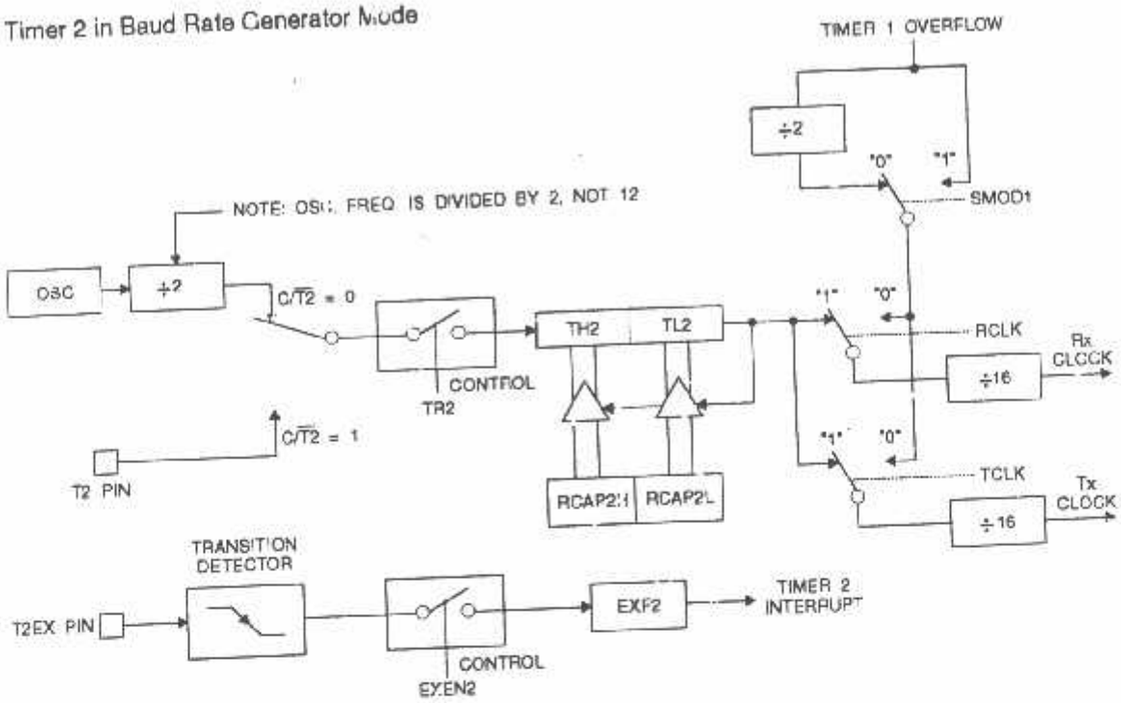


Figure 4. Timer 2 in Baud Rate Generator Mode



Baud Rate Generator

Timer 2 is selected as the baud rate generator by setting TCLK and/or RCLK in T2CON (Table 2). Note that the baud rates for transmit and receive can be different if Timer 2 is used for the receiver or transmitter and Timer 1 is used for the other function. Setting RCLK and/or TCLK puts Timer 2 into its baud rate generator mode, as shown in Figure 4.

The baud rate generator mode is similar to the auto-reload mode, in that a rollover in TH2 causes the Timer 2 registers to be reloaded with the 16-bit value in registers RCAP2H and RCAP2L, which are preset by software.

The baud rates in Modes 1 and 3 are determined by Timer 2's overflow rate according to the following equation.

$$\text{Modes 1 and 3 Baud Rates} = \frac{\text{Timer 2 Overflow Rate}}{16}$$

The Timer can be configured for either timer or counter operation. In most applications, it is configured for timer operation ($C/\overline{T2} = 0$). The timer operation is different for Timer 2 when it is used as a baud rate generator. Normally, as a timer, it increments every machine cycle (at 1/12 the oscillator frequency). As a baud rate generator, however, it increments every state time (at 1/2 the oscillator frequency). The baud rate formula is given below.

$$\frac{\text{Modes 1 and 3}}{\text{Baud Rate}} = \frac{\text{Oscillator Frequency}}{32 \times [65536 - (\text{RCAP2H,RCAP2L})]}$$

where (RCAP2H, RCAP2L) is the content of RCAP2H and RCAP2L taken as a 16-bit unsigned integer.

Timer 2 as a baud rate generator is shown in Figure 4. This figure is valid only if RCLK or TCLK = 1 in T2CON. Note that a rollover in TH2 does not set TF2 and will not generate an interrupt. Note too, that if EXEN2 is set, a 1-to-0 transition in T2EX will set EXF2 but will not cause a reload from (RCAP2H, RCAP2L) to (TH2, TL2). Thus when Timer 2 is in use as a baud rate generator, T2EX can be used as an extra external interrupt.

Note that when Timer 2 is running (TR2 = 1) as a timer in the baud rate generator mode, TH2 or TL2 should not be read from or written to. Under these conditions, the Timer is incremented every state time, and the results of a read or write may not be accurate. The RCAP2 registers may be read but should not be written to, because a write might overlap a reload and cause write and/or reload errors. The timer should be turned off (clear TR2) before accessing the Timer 2 or RCAP2 registers.

Programmable Clock Out

A 50% duty cycle clock can be programmed to come out on P1.0, as shown in Figure 5. This pin, besides being a regular I/O pin, has two alternate functions. It can be programmed to input the external clock for Timer/Counter 2 or to output a 50% duty cycle clock ranging from 61 Hz to 4 MHz (for a 16-MHz operating frequency).

To configure the Timer/Counter 2 as a clock generator, bit C/$\overline{T2}$ (T2CON.1) must be cleared and bit T2OE (T2MOD.1) must be set. Bit TR2 (T2CON.2) starts and stops the timer.

The clock-out frequency depends on the oscillator frequency and the reload value of Timer 2 capture registers (RCAP2H, RCAP2L), as shown in the following equation.

$$\text{Clock Out Frequency} = \frac{\text{Oscillator Frequency}}{4 \times [65536 - (\text{RCAP2H,RCAP2L})]}$$

In the clock-out mode, Timer 2 rollovers will not generate an interrupt. This behavior is similar to when Timer 2 is used as a baud-rate generator. It is possible to use Timer 2 as a baud-rate generator and a clock generator simultaneously. Note, however, that the baud-rate and clock-out frequencies cannot be determined independently from one another since they both use RCAP2H and RCAP2L.

Figure 5. Timer 2 in Clock-out Mode

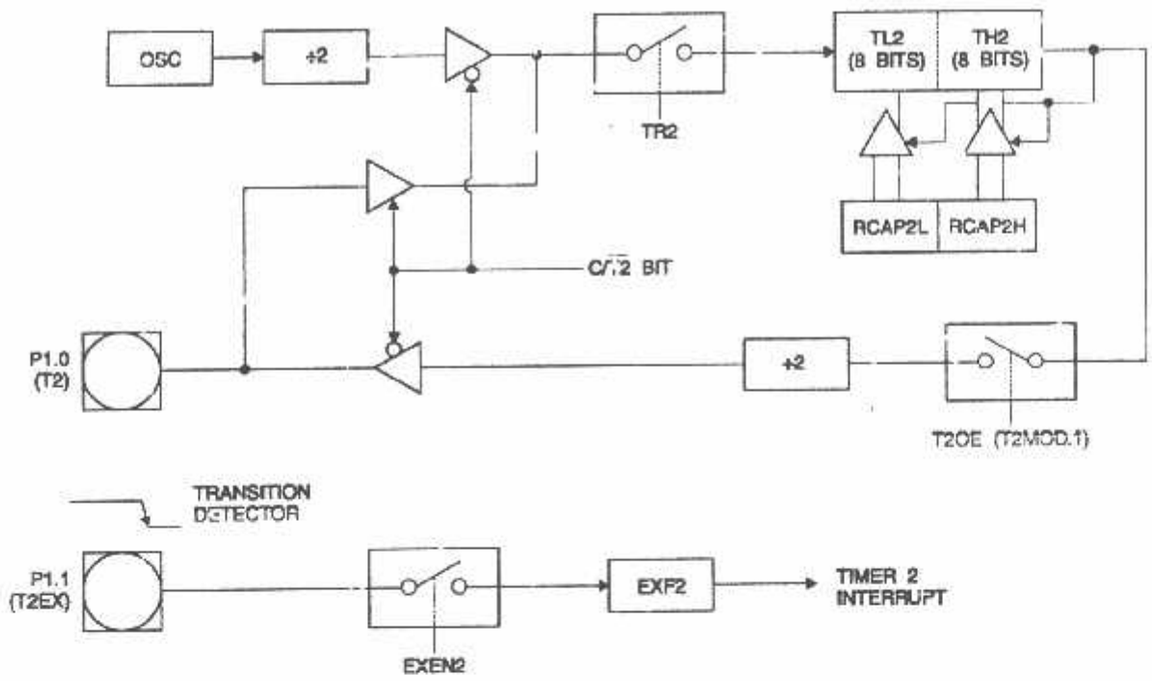
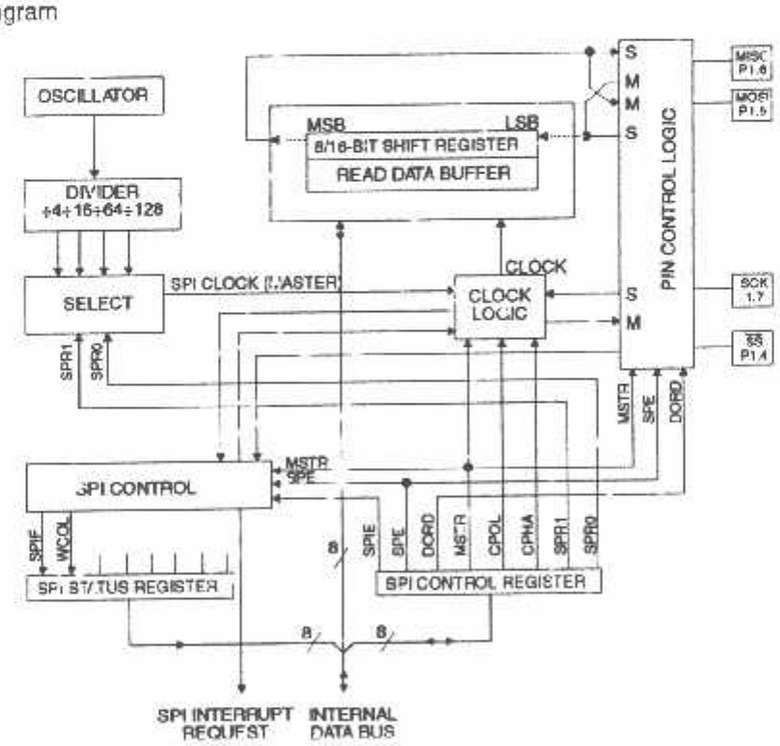


Figure 6. SPI Block Diagram



UART

The UART in the AT89S8252 operates the same way as the UART in the AT89C51 and AT89C52. For further information on the UART operation, refer to the Atmel web site (http://www.atmel.com). From the home page, select "Products", then "Microcontrollers, then "8051-Architecture". Click on "Documentation", then on "Other Documents". Open the document "AT89 Series Hardware Description".

Serial Peripheral Interface

The serial peripheral interface (SPI) allows high-speed synchronous data transfer between the AT89S8252 and peripheral devices or between several AT89S8252 devices. The AT89S8252 SPI features include the following:

- Full-Duplex, 3-Wire Synchronous Data Transfer
- Master or Slave Operation
- 1.5 MHz Bit Frequency (max.)
- LSB First or MSB First Data Transfer
- Four Programmable Bit Rates
- End of Transmission Interrupt Flag
- Write Collision Flag Protection
- Wakeup from Idle Mode (Slave Mode Only)

The interconnection between master and slave CPUs with SPI is shown in the following figure. The SCK pin is the clock output in the master mode but is the clock input in the slave mode. Writing to the SPI data register of the master CPU starts the SPI clock generator, and the data written shifts out of the MOSI pin and into the MOSI pin of the slave CPU. After shifting one byte, the SPI clock generator stops, setting the end of transmission flag (SPIF). If both the SPI interrupt enable bit (SPIE) and the serial port interrupt enable bit (ES) are set, an interrupt is requested.

The Slave Select input, $\overline{SS}$/P1.4, is set low to select an individual SPI device as a slave. When $\overline{SS}$/P1.4 is set high, the SPI port is deactivated and the MOSI/P1.5 pin can be used as an input.

There are four combinations of SCK phase and polarity with respect to serial data, which are determined by control bits CPHA and CPOL. The SPI data transfer formats are shown in Figure 8 and Figure 9.

Figure 7. SPI Master-slave Interconnection

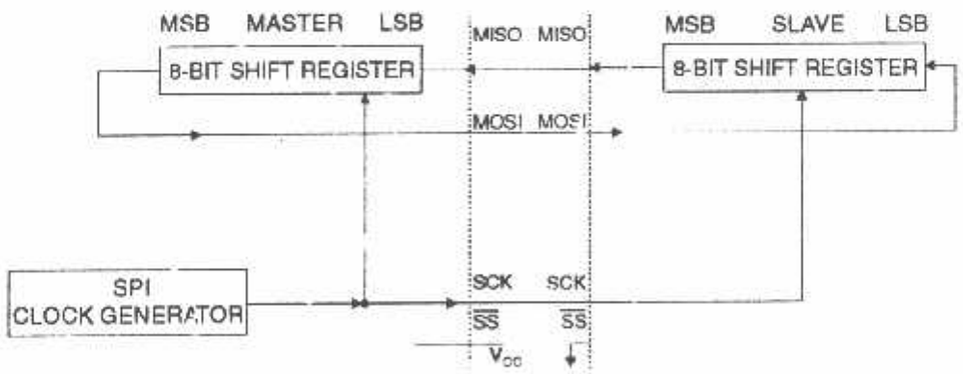
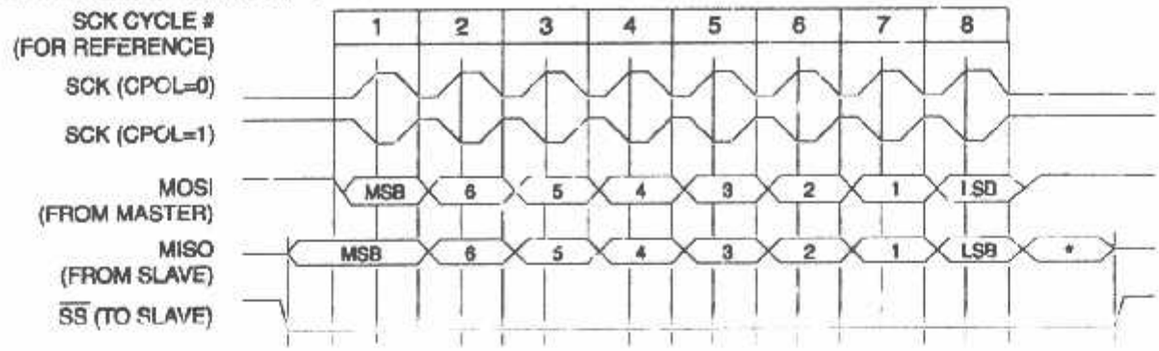
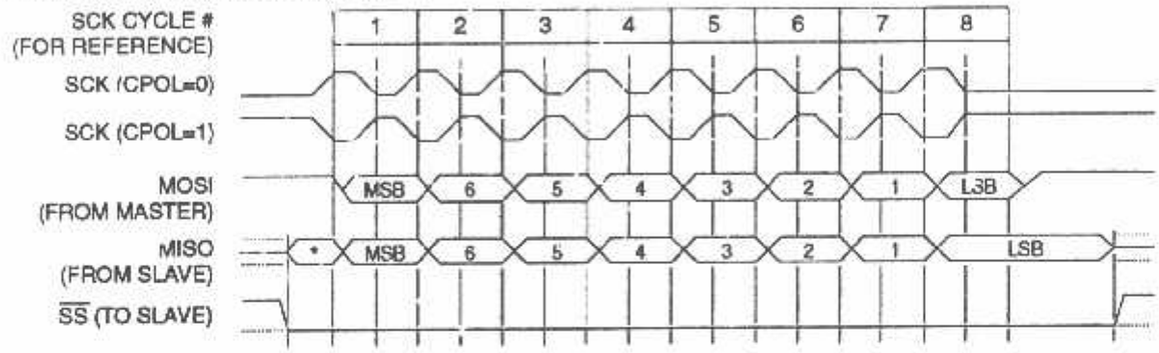


Figure 8. SPI transfer Format with CPHA = 0



Note: *Not defined but normally MSB of character just received

Figure 9. SPI Transfer Format with CPHA = 1



Note: *Not defined but normally LSB of previously transmitted character.

Interrupts

The AT89S8252 has a total of six interrupt vectors: two external interrupts ($\overline{INT0}$ and $\overline{INT1}$), three timer interrupts (Timers 0, 1, and 2), and the serial port interrupt. These interrupts are all shown in Figure 10.

Each of these interrupt sources can be individually enabled or disabled by setting or clearing a bit in Special Function Register IE. IE also contains a global disable bit, EA, which disables all interrupts at once.

Note that Table 10 shows that bit position IE.6 is unimplemented. In the AT89C51, bit position IE.5 is also unimplemented. User software should not write 1s to these bit positions, since they may be used in future AT89 products.

Timer 2 interrupt is generated by the logical OR of bits TF2 and EXF2 in register T2CON. Neither of these flags is cleared by hardware when the service routine is vectored to. In fact, the service routine may have to determine whether it was TF2 or EXF2 that generated the interrupt, and that bit will have to be cleared in software.

The Timer 0 and Timer 1 flags, TF0 and TF1, are set at S5F2 of the cycle in which the timers overflow. The values are then polled by the circuitry in the next cycle. However, the Timer 2 flag, TF2, is set at S2P2 and is polled in the same cycle in which the timer overflows.

Table 10. Interrupt Enable (IE) Register

(MSB)(LSB)

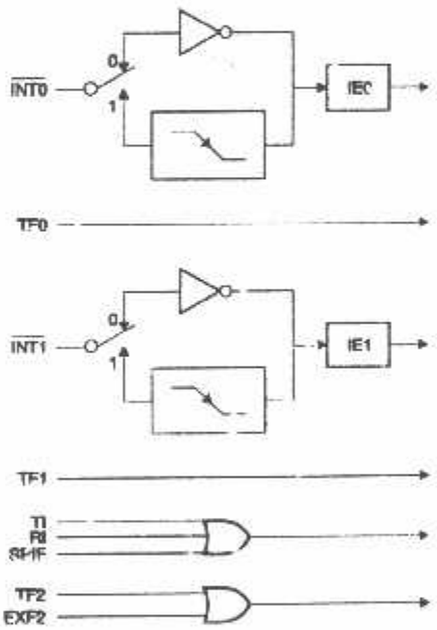
EA	–	ET2	ES	ET1	EX1	ET0	EX0

Enable Bit = 1 enables the interrupt.

Enable Bit = 0 disables the interrupt.

Symbol	Position	Function
EA	IE.7	Disables all interrupts. If EA = 0, no interrupt is acknowledged. If EA = 1, each interrupt source is individually enabled or disabled by setting or clearing its enable bit.
–	IE.6	Reserved.
ET2	IE.5	Timer 2 interrupt enable bit.
ES	IE.4	SPI and UART interrupt enable bit.
ET1	IE.3	Timer 1 interrupt enable bit.
EX1	IE.2	External interrupt 1 enable bit.
ET0	IE.1	Timer 0 interrupt enable bit.
EX0	IE.0	External interrupt 0 enable bit.
User software should never write 1s to unimplemented bits, because they may be used in future AT89 products.		

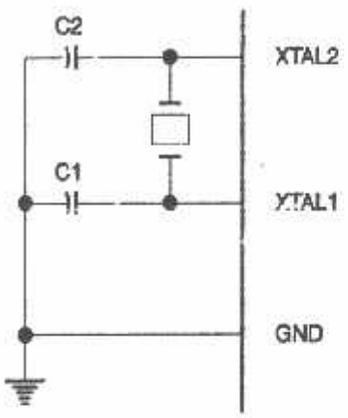
Figure 10. Interrupt Sources



Oscillator Characteristics

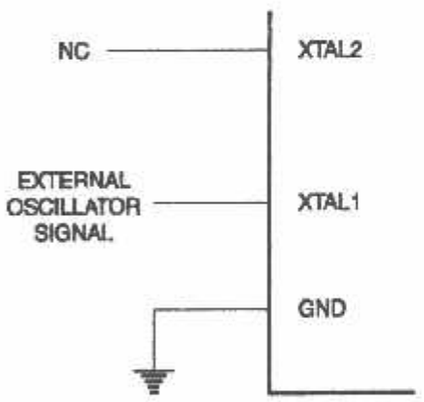
XTAL1 and XTAL2 are the input and output, respectively, of an inverting amplifier that can be configured for use as an on-chip oscillator, as shown in Figure 11. Either a quartz crystal or ceramic resonator may be used. To drive the device from an external clock source, XTAL2 should be left unconnected while XTAL1 is driven, as shown in Figure 12. There are no requirements on the duty cycle of the external clock signal, since the input to the internal clocking circuitry is through a divide-by-two flip-flop, but minimum and maximum voltage high and low time specifications must be observed.

Figure 11. Oscillator Connections



Note: C1, C2 = 30 pF ± 10 pF for Crystals
= 40 pF ± 10 pF for Ceramic Resonators

Figure 12. External Clock Drive Configuration



Idle Mode

In idle mode, the CPU puts itself to sleep while all the on-chip peripherals remain active. The mode is invoked by software. The content of the on-chip RAM and all the special functions registers remain unchanged during this mode. The idle mode can be terminated by any enabled interrupt or by a hardware reset.

Note that when idle mode is terminated by a hardware reset, the device normally resumes program execution from where it left off, up to two machine cycles before the internal reset algorithm takes control. On-chip hardware inhibits access to internal RAM in this event but access to the port pins is not inhibited. To eliminate the possibility of an unexpected write to a port pin when idle mode is terminated by a reset, the instruction following the one that invokes idle mode should not write to a port pin or to external memory.

Status of External Pins During Idle and Power-down Modes

Mode	Program Memory	ALE	$\overline{PSEN}$	PORT0	PORT1	PORT2	PORT3
Idle	Internal	1	1	Data	Data	Data	Data
Idle	External	1	1	Float	Data	Address	Data
Power-down	Internal	0	0	Data	Data	Data	Data
Power-down	External	0	0	Float	Data	Data	Data

Power-down Mode

In the power-down mode, the oscillator is stopped and the instruction that invokes power-down is the last instruction executed. The on-chip RAM and Special Function Registers retain their values until the power-down mode is terminated. Exit from power-down can be initiated either by a hardware reset or by an enabled external interrupt. Reset redefines the SFRs but does not change the on-chip RAM. The reset should not be activated before V_{CC} is restored to its normal operating level and must be held active long enough to allow the oscillator to restart and stabilize.

To exit power-down via an interrupt, the external interrupt must be enabled as level sensitive before entering power-down. The interrupt service routine starts at 16 ms (nominal) after the enabled interrupt pin is activated.

Program Memory Lock Bits

The AT89S8252 has three lock bits that can be left unprogrammed (U) or can be programmed (P) to obtain the additional features listed in the following table.

When lock bit 1 is programmed, the logic level at the $\overline{EA}$ pin is sampled and latched during reset. If the device is powered up without a reset, the latch initializes to a random value and holds that value until reset is activated. The latched value of $\overline{EA}$ must agree with the current logic level at that pin in order for the device to function properly.

Once programmed, the lock bits can only be unprogrammed with the Chip Erase operations in either the parallel or serial modes.

Lock Bit Protection Modes[1][2]

	Program Lock Bits			
	LB1	LB2	LB3	Protection Type
1	U	U	U	No internal memory lock feature.
2	P	U	U	MOVC instructions executed from external program memory are disabled from fetching code bytes from internal memory. $\overline{EA}$ is sampled and latched on reset and further programming of the Flash memory (parallel or serial mode) is disabled.
3	P	P	U	Same as Mode 2, but parallel or serial verify are also disabled.
4	P	P	P	Same as Mode 3, but external execution is also disabled.

Notes: 1. U = Unprogrammed
2. P = Programmed

Programming the Flash and EEPROM

Atmel's AT89S8252 Flash Microcontroller offers 8K bytes of in-system reprogrammable Flash Code memory and 2K bytes of EEPROM Data memory.

The AT89S8252 is normally shipped with the on-chip Flash Code and EEPROM Data memory arrays in the erased state (i.e. contents = FFH) and ready to be programmed. This device supports a High-voltage (12-V V_{PP}) Parallel programming mode and a Low-voltage (5-V V_{CC}) Serial programming mode. The serial programming mode provides a convenient way to reprogram the AT89S8252 inside the user's system. The parallel programming mode is compatible with conventional third party Flash or EPROM programmers.

The Code and Data memory arrays are mapped via separate address spaces in the serial programming mode. In the parallel programming mode, the two arrays occupy one contiguous address space: 0000H to 1FFFH for the Code array and 2000H to 27FFH for the Data array.

The Code and Data memory arrays on the AT89S8252 are programmed byte-by-byte in either programming mode. An auto-erase cycle is provided with the self-timed programming operation in the serial programming mode. There is no need to perform the Chip Erase operation to reprogram any memory location in the serial programming mode unless any of the lock bits have been programmed.

In the parallel programming mode, there is no auto-erase cycle. To reprogram any non-blank byte, the user needs to use the Chip Erase operation first to erase both arrays.

Parallel Programming Algorithm: To program and verify the AT89S8252 in the parallel programming mode, the following sequence is recommended:

1. Power-up sequence:
   Apply power between V_{CC} and GND pins.
   Set RST pin to "H".
   Apply a 3 MHz to 24 MHz clock to XTAL1 pin and wait for at least 10 milliseconds.
2. Set $\overline{PSEN}$ pin to "L"
   ALE pin to "H"
   $\overline{EA}$ pin to "H" and all other pins to "H".
3. Apply the appropriate combination of "H" or "L" logic levels to pins P2.6, P2.7, P3.6, P3.7 to select one of the programming operations shown in the Flash Programming Modes table.
4. Apply the desired byte address to pins P1.0 to P1.7 and P2.0 to P2.5.
   Apply data to pins P0.0 to P0.7 for Write Code operation.
5. Raise $\overline{EA}/V_{PP}$ to 12V to enable Flash programming, erase or verification.
6. Pulse ALE/$\overline{PROG}$ once to program a byte in the Code memory array, the Data memory array or the lock bits. The byte-write cycle is self-timed and typically takes 1.5 ms.
7. To verify the byte just programmed, bring pin P2.7 to "L" and read the programmed data at pins P0.0 to P0.7.
8. Repeat steps 3 through 7 changing the address and data for the entire 2K or 8K bytes array or until the end of the object file is reached.
9. Power-off sequence:
   Set XTAL1 to "L".
   Set RST and $\overline{EA}$ pins to "L".
   Turn V_{CC} power off.

In the parallel programming mode, there is no auto-erase cycle and to reprogram any non-blank byte, the user needs to use the Chip Erase operation first to erase both arrays.

Data Polling: The AT89S8252 features DATA Polling to indicate the end of a byte write cycle. During a byte write cycle in the parallel or serial programming mode, an attempted read of the last byte written will result in the complement of the written datum on P0.7 (parallel mode), and on the MSB of the serial output byte on MISO (serial mode). Once the write cycle has been completed, true data are valid on all outputs, and the next cycle may begin. DATA Polling may begin any time after a write cycle has been initiated.

Ready/Busy: The progress of byte programming in the parallel programming mode can also be monitored by the RDY/BSY output signal. Pin P3.4 is pulled Low after ALE goes High during programming to indicate BUSY. P3.4 is pulled High again when programming is done to indicate READY.

Program Verify: If lock bits LB1 and LB2 have not been programmed, the programmed Code or Data byte can be read back via the address and data lines for verification. The state of the lock bits can also be verified directly in the parallel programming mode. In the serial programming mode, the state of the lock bits can only be verified indirectly by observing that the lock bit features are enabled.

Chip Erase: Both Flash and EEPROM arrays are erased electrically at the same time. In the parallel programming mode, chip erase is initiated by using the proper combination of control signals and by holding ALE/PROG low for 10 ms. The Code and Data arrays are written with all "1"s in the Chip Erase operation.

In the serial programming mode, a chip erase operation is initiated by issuing the Chip Erase instruction. In this mode, chip erase is self-timed and takes about 16 ms.

During chip erase, a serial read from any address location will return 00H at the data outputs.

Serial Programming Fuse: A programmable fuse is available to disable Serial Programming if the user needs maximum system security. The Serial Programming Fuse can only be programmed or erased in the Parallel Programming Mode.

The AT89S8252 is shipped with the Serial Programming Mode enabled.

Reading the Signature Bytes: The signature bytes are read by the same procedure as a normal verification of locations 030H and 031H, except that P3.6 and P3.7 must be pulled to a logic low. The values returned are as follows:

(030H) = 1EH indicates manufactured by Atmel
(031H) = 72H indicates 89S8252

Programming Interface

Every code byte in the Flash and EEPROM arrays can be written, and the entire array can be erased, by using the appropriate combination of control signals. The write operation cycle is self-timed and once initiated, will automatically time itself to completion.

Most worldwide major programming vendors offer support for the Atmel AT89 microcontroller series. Please contact your local programming vendor for the appropriate software revision.

Serial Downloading

Both the Code and Data memory arrays can be programmed using the serial SPI bus while RST is pulled to V_{CC}. The serial interface consists of pins SCK, MOSI (input) and MISO (output). After RST is set high, the Programming Enable instruction needs to be executed first before program/erase operations can be executed.

An auto-erase cycle is built into the self-timed programming operation (in the serial mode ONLY) and there is no need to first execute the Chip Erase instruction unless any of the lock bits have been programmed. The Chip Erase operation turns the content of every memory location in both the Code and Data arrays into FFH.

The Code and Data memory arrays have separate address spaces:

0000H to 1FFFH for Code memory and 000H to 7FFH for Data memory.

Either an external system clock is supplied at pin XTAL1 or a crystal needs to be connected across pins XTAL1 and XTAL2. The maximum serial clock (SCK) frequency should be less than 1/40 of the crystal frequency. With a 24 MHz oscillator clock, the maximum SCK frequency is 600 kHz.

Serial Programming Algorithm

To program and verify the AT89S8252 in the serial programming mode, the following sequence is recommended:

1. Power-up sequence:

   Apply power between VCC and GND pins.

   Set RST pin to "H".

   If a crystal is not connected across pins XTAL1 and XTAL2, apply a 3 MHz to 24 MHz clock to XTAL1 pin and wait for at least 10 milliseconds
2. Enable serial programming by sending the Programming Enable serial instruction to pin MOSI/P1.5. The frequency of the shift clock supplied at pin SCK/P1.7 needs to be less than the CPU clock at XTAL1 divided by 40.
3. The Code or Data array is programmed one byte at a time by supplying the address and data together with the appropriate Write instruction. The selected memory location is first automatically erased before new data is written. The write cycle is self-timed and typically takes less than 2.5 ms at 5V.
4. Any memory location can be verified by using the Read instruction which returns the content at the selected address at serial output MISO/P1.6.
5. At the end of a programming session, RST can be set low to commence normal operation.
6. Power-off sequence (if needed):

   Set XTAL1 to "L" (if a crystal is not used).

   Set RST to "L".

   Turn V_{CC} power off.

Serial Programming Instruction

The Instruction Set for Serial Programming follows a 3-byte protocol and is shown in the following table:

Instruction Set

Instruction	Input Format			Operation
	Byte 1	Byte 2	Byte 3	
Programming Enable	1010 1100	0101 0011	xxxx xxxx	Enable serial programming interface after RST goes high.
Chip Erase	1010 1100	xxxx x100	xxxx xxxx	Chip erase both 8K & 2K memory arrays.
Read Code Memory	aaaa a001	low addr	xxxx xxxx	Read data from Code memory array at the selected address. The 5 MSBs of the first byte are the high order address bits. The low order address bits are in the second byte. Data are available at pin MISO during the third byte.
Write Code Memory	aaaa a010	low addr	data in	Write data to Code memory location at selected address. The address bits are the 5 MSBs of the first byte together with the second byte.
Read Data Memory	00aa a101	low addr	xxxx xxxx	Read data from Data memory array at selected address. Data are available at pin MISO during the third byte.
Write Data Memory	00aa a110	low addr	data in	Write data to Data memory location at selected address.
Write Lock Bits	1010 1100	LB1 LB2 LB3 x x111	xxxx xxxx	Write lock bits. Set LB1, LB2 or LB3 = "0" to program lock bits.

Notes: 1. DATA polling is used to indicate the end of a byte write cycle which typically takes less than 2.5 ms at 5V.
2. "aaaaa" = high order address.
3. "x" = don't care.

Flash and EEPROM Parallel Programming Modes

Mode	RST	PSEN	ALE/PROG	EA/V_{PP}	P2.6	P2.7	P3.6	P3.7	Data I/O P0.7:0	Address P2.5:0 P1.7:0
Serial Prog. Modes	H	h[1]	h[1]	x						
Chip Erase	H	L	⌐⌐ (2)	12V	H	L	L	L	X	X
Write (10K bytes) Memory	H	L	⌐⌐	12V	L	H	H	H	DIN	ADDR
Read (10K bytes) Memory	H	L	H	12V	L	L	H	H	DOUT	ADDR
Write Lock Bits:	H	L	⌐⌐	12V	H	L	H	L	DIN	X
Bit - 1									P0.7 = 0	X
Bit - 2									P0.6 = 0	X
Bit - 3									P0.5 = 0	X
Read Lock Bits:	H	L	H	12V	H	H	L	L	DOUT	X
Bit - 1									@P0.2	X
Bit - 2									@P0.1	X
Bit - 3									@P0.0	X
Read Atmel Code	H	L	H	12V	L	L	L	L	DOUT	30H
Read Device Code	H	L	H	12V	L	L	L	L	DOUT	31H
Serial Prog. Enable	H	L	⌐⌐ (2)	12V	L	H	L	H	P0.0 = 0	X
Serial Prog. Disable	H	L	⌐⌐ (2)	12V	L	H	L	H	P0.0 = 1	X
Read Serial Prog. Fuse	H	L	H	12V	H	H	L	H	@P0.0	X

Notes:
1. "h" = weakly pulled "High" internally.
2. Chip Erase and Serial Programming Fuse require a 10 ms PROG pulse. Chip Erase needs to be performed first before reprogramming any byte with a content other than FFH.
3. P3.4 is pulled Low during programming to indicate RDY/BSY.
4. "X" = don't care

Figure 13. Programming the Flash/EEPROM Memory

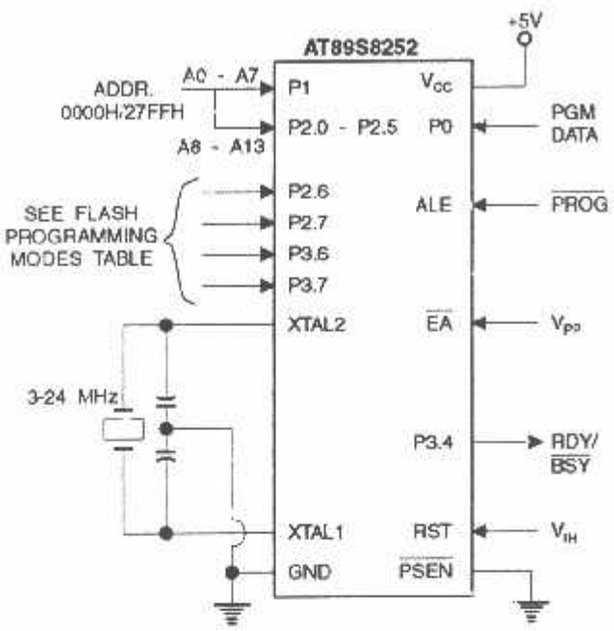


Figure 14. Verifying the Flash/EEPROM Memory

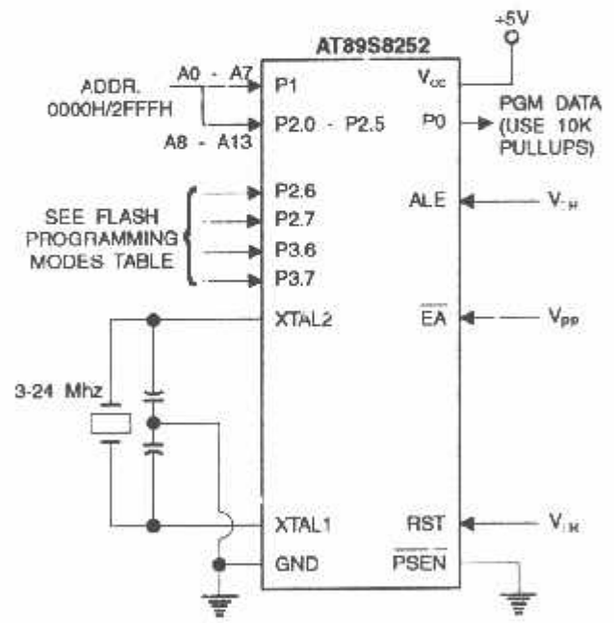
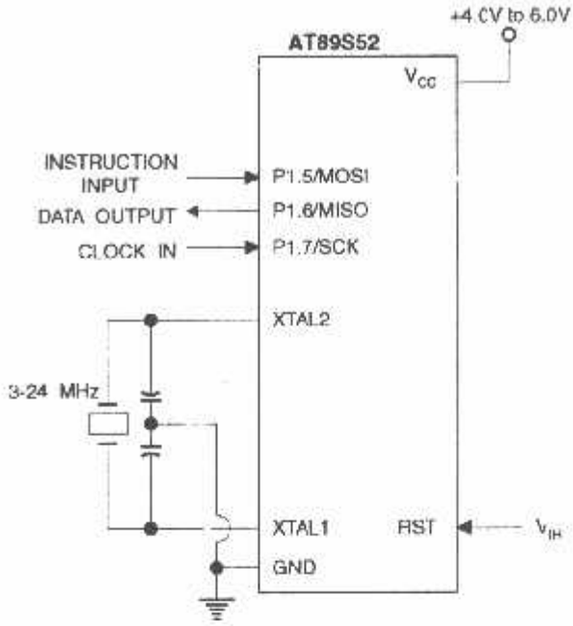


Figure 15. Flash/EEPROM Serial Downloading

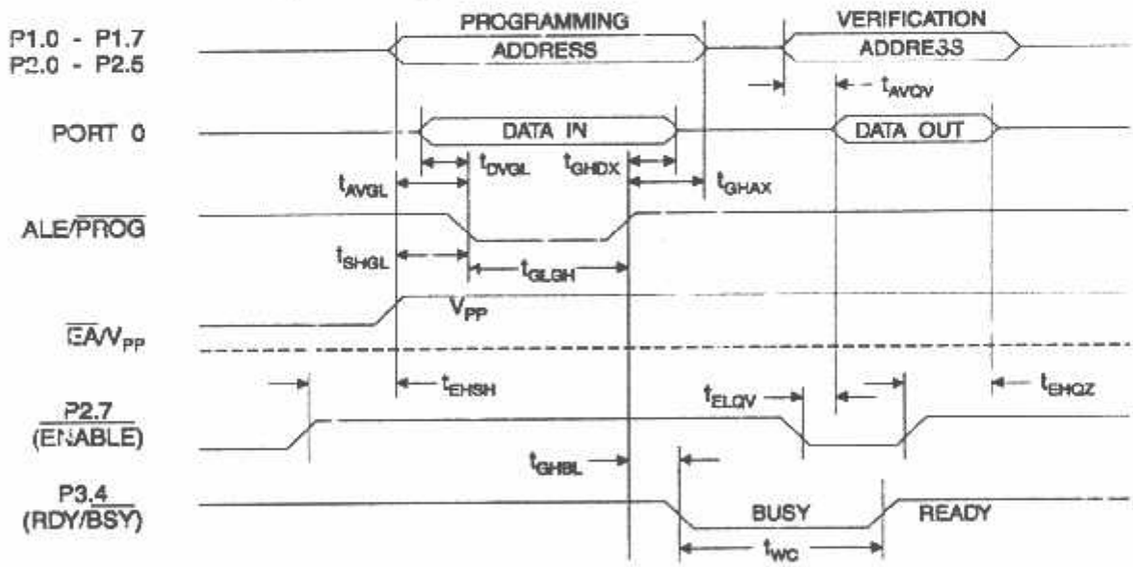


Flash Programming and Verification Characteristics – Parallel Mode

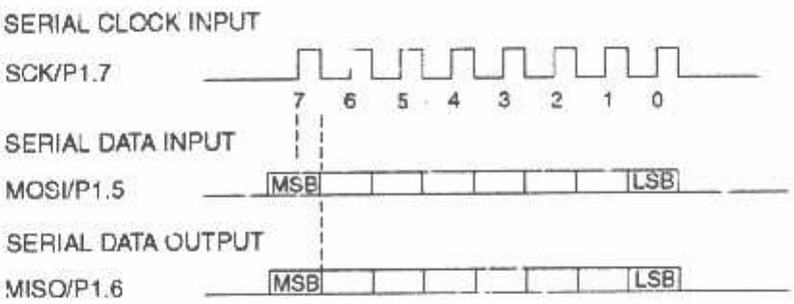
T_A = 0°C to 70°C, V_{CC} = 5.0V ± 10%

Symbol	Parameter	Min	Max	Units
V_{PP}	Programming Enable Voltage	11.5	12.5	V
I_{PP}	Programming Enable Current		1.0	mA
$1/t_{CLCL}$	Oscillator Frequency	3	24	MHz
t_{AVGL}	Address Setup to $\overline{PROG}$ Low	$48t_{CLCL}$		
t_{GHAX}	Address Hold after $\overline{PROG}$	$48t_{CLCL}$		
t_{DVGL}	Data Setup to $\overline{PROG}$ Low	$48t_{CLCL}$		
t_{GHDX}	Data Hold after $\overline{PROG}$	$48t_{CLCL}$		
t_{EHSH}	P2.7 ($\overline{ENABLE}$) High to V_{PP}	$48t_{CLCL}$		
t_{SHGL}	V_{PP} Setup to $\overline{PROG}$ Low	10		µs
t_{GLGH}	$\overline{PROG}$ Width	1	110	µs
t_{AVQV}	Address to Data Valid		$48t_{CLCL}$	
t_{ELQV}	$\overline{ENABLE}$ Low to Data Valid		$48t_{CLCL}$	
t_{EHQZ}	Data Float after $\overline{ENABLE}$	0	$48t_{CLCL}$	
t_{GHBL}	$\overline{PROG}$ High to $\overline{BUSY}$ Low		1.0	µs
t_{WC}	Byte Write Cycle Time		2.0	ms

Flash/EEPROM Programming and Verification Waveforms – Parallel Mode



Serial Downloading Waveforms



Serial Programming Characteristics

Figure 16. Serial Programming Timing

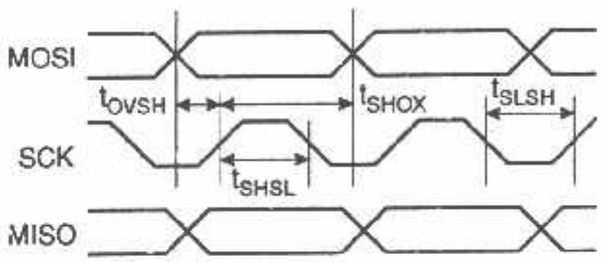


Table 11. Serial Programming Characteristics, T_A = -40°C to 85°C, V_{CC} = 4.0 - 6.0V (Unless Otherwise Noted)

Symbol	Parameter	Min	Typ	Max	Units
$1/t_{CLCL}$	Oscillator Frequency	0		24	MHz
t_{CLCL}	Oscillator Period	41.6			ns
t_{SHSL}	SCK Pulse Width High	24 t_{CLCL}			ns
t_{SLSH}	SCK Pulse Width Low	24 t_{CLCL}			ns
t_{OVSH}	MOSI Setup to SCK High	t_{CLCL}			ns
t_{SHOX}	MOSI Hold after SCK High	2 t_{CLCL}			ns

Absolute Maximum Ratings*

Operating Temperature	-55°C to +125°C
Storage Temperature	-65°C to +150°C
Voltage on Any Pin with Respect to Ground	-1.0V to +7.0V
Maximum Operating Voltage	6.6V
DC Output Current	15.0 mA

*NOTICE: Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC Characteristics

The values shown in this table are valid for T_A = -40°C to 85°C and V_{CC} = 5.0V ± 20%, unless otherwise noted.

Symbol	Parameter	Condition	Min	Max	Units
V_{IL}	Input Low-voltage	(Except $\overline{EA}$)	-0.5	0.2 V_{CC} - 0.1	V
V_{IL1}	Input Low-voltage ($\overline{EA}$)		-0.5	0.2 V_{CC} - 0.3	V
V_{IH}	Input High-voltage	(Except XTAL1, RST)	0.2 V_{CC} + 0.9	V_{CC} + 0.5	V
V_{IH1}	Input High-voltage	(XTAL1, RST)	0.7 V_{CC}	V_{CC} + 0.5	V
V_{OL}	Output Low-voltage [1] (Ports 1,2,3)	I_{OL} = 1.6 mA		0.5	V
V_{OL1}	Output Low-voltage [1] (Port 0, ALE, $\overline{PSEN}$)	I_{OL} = 3.2 mA		0.5	V
V_{OH}	Output High-voltage (Ports 1,2,3, ALE, $\overline{PSEN}$)	I_{OH} = -60 µA, V_{CC} = 5V ± 10%	2.4		V
		I_{OH} = -25 µA	0.75 V_{CC}		V
		I_{OH} = -10 µA	0.9 V_{CC}		V
V_{OH1}	Output High-voltage (Port 0 in External Bus Mode)	I_{OH} = -800 µA, V_{CC} = 5V ± 10%	2.4		V
		I_{OH} = -300 µA	0.75 V_{CC}		V
		I_{OH} = -80 µA	0.9 V_{CC}		V
I_{IL}	Logical 0 Input Current (Ports 1,2,3)	V_{IN} = 0.45V		-50	µA
I_{TL}	Logical 1 to 0 Transition Current (Ports 1,2,3)	V_{IN} = 2V, V_{CC} = 5V ± 10%		-650	µA
I_{LI}	Input Leakage Current (Port 0, $\overline{EA}$)	0.45 < V_{IN} < V_{CC}		±10	µA
RRST	Reset Pull-down Resistor		50	300	KΩ
C_{IO}	Pin Capacitance	Test Freq. = 1 MHz, T_A = 25°C		10	pF
I_{CC}	Power Supply Current	Active Mode, 12 MHz		25	mA
		Idle Mode, 12 MHz		6.5	mA
	Power-down Mode [2]	V_{CC} = 6V		100	µA
		V_{CC} = 3V		40	µA

Notes: 1. Under steady state (non-transient) conditions, I_{OL} must be externally limited as follows:
Maximum I_{OL} per port pin: 10 mA
Maximum I_{OL} per 8-bit port: Port 0: 26 mA; Ports 1, 2, 3: 15 mA
Maximum total I_{OL} for all output pins: 71 mA
If I_{OL} exceeds the test condition, V_{OL} may exceed the related specification. Pins are not guaranteed to sink current greater than the listed test conditions.
2. Minimum V_{CC} for Power-down is 2V

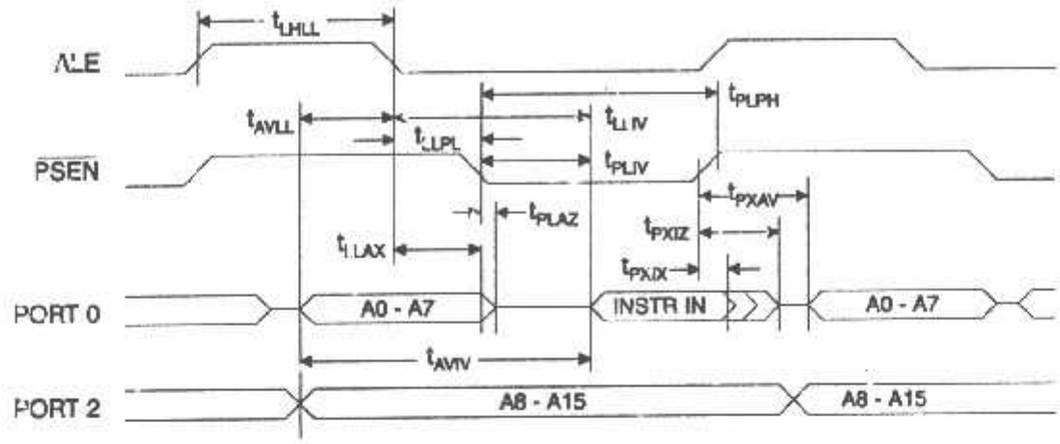
AC Characteristics

Under operating conditions, load capacitance for Port 0, ALE/$\overline{PROG}$, and $\overline{PSEN}$ = 100 pF; load capacitance for all other outputs = 80 pF.

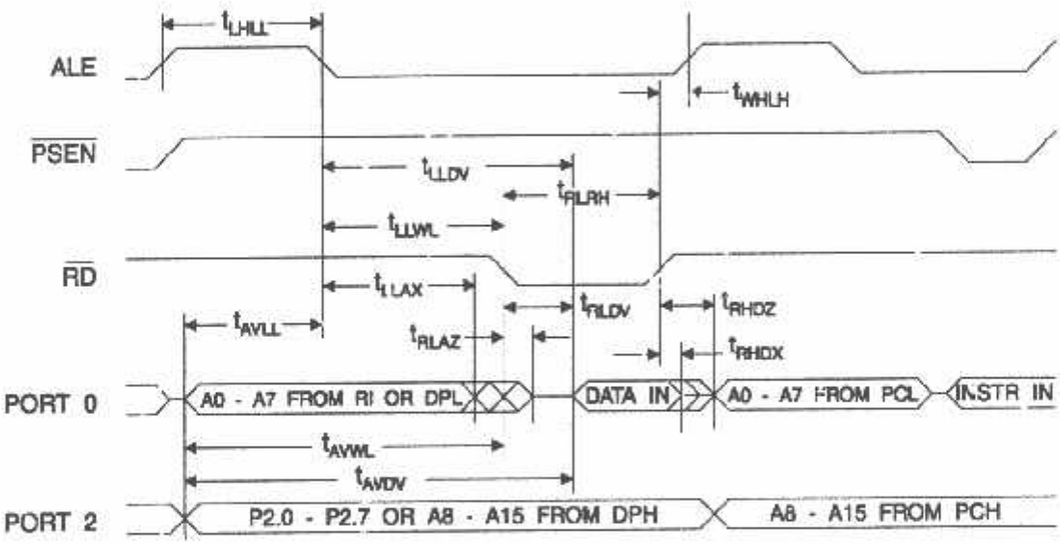
External Program and Data Memory Characteristics

Symbol	Parameter	Variable Oscillator		Units
		Min	Max	
$1/t_{CLCL}$	Oscillator Frequency	0	24	MHz
t_{LHLL}	ALE Pulse Width	$2t_{CLCL}$ - 40		ns
t_{AVLL}	Address Valid to ALE Low	t_{CLCL} - 13		ns
t_{LLAX}	Address Hold after ALE Low	t_{CLCL} - 20		ns
t_{LLIV}	ALE Low to Valid Instruction In		$4t_{CLCL}$ - 65	ns
t_{LLPL}	ALE Low to $\overline{PSEN}$ Low	t_{CLCL} - 13		ns
t_{PLPH}	$\overline{PSEN}$ Pulse Width	$3t_{CLCL}$ - 20		ns
t_{PLIV}	$\overline{PSEN}$ Low to Valid Instruction In		$3t_{CLCL}$ - 45	ns
t_{PXIX}	Input Instruction Hold after $\overline{PSEN}$	0		ns
t_{PXIZ}	Input Instruction Float after $\overline{PSEN}$		t_{CLCL} - 10	ns
t_{PXAV}	$\overline{PSEN}$ to Address Valid	t_{CLCL} - 8		ns
t_{AVIV}	Address to Valid Instruction In		$5t_{CLCL}$ - 55	ns
t_{PLAZ}	$\overline{PSEN}$ Low to Address Float		10	ns
t_{RLRH}	$\overline{RD}$ Pulse Width	$6t_{CLCL}$ - 100		ns
t_{WLWH}	$\overline{WR}$ Pulse Width	$6t_{CLCL}$ - 100		ns
t_{RLDV}	$\overline{RD}$ Low to Valid Data In		$5t_{CLCL}$ - 90	ns
t_{RHDX}	Data Hold after $\overline{RD}$	0		ns
t_{RHDZ}	Data Float after $\overline{RD}$		$2t_{CLCL}$ - 28	ns
t_{LLDV}	ALE Low to Valid Data In		$8t_{CLCL}$ - 150	ns
t_{AVDV}	Address to Valid Data In		$9t_{CLCL}$ - 165	ns
t_{LLWL}	ALE Low to $\overline{RD}$ or $\overline{WR}$ Low	$3t_{CLCL}$ - 50	$3t_{CLCL}$ + 50	ns
t_{AVWL}	Address to $\overline{RD}$ or $\overline{WR}$ Low	$4t_{CLCL}$ - 75		ns
t_{QVWX}	Data Valid to $\overline{WR}$ Transition	t_{CLCL} - 20		ns
t_{QVWH}	Data Valid to $\overline{WR}$ High	$7t_{CLCL}$ - 120		ns
t_{WHQX}	Data Hold after $\overline{WR}$	t_{CLCL} - 20		ns
t_{RLAZ}	$\overline{RD}$ Low to Address Float		0	ns
t_{WHLH}	$\overline{RD}$ or $\overline{WR}$ High to ALE High	t_{CLCL} - 20	t_{CLCL} + 25	ns

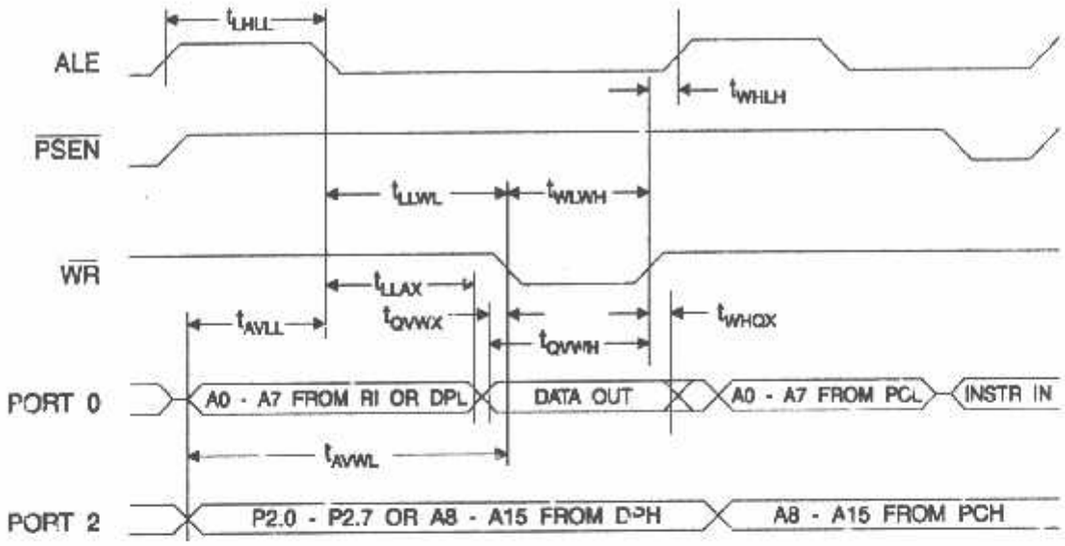
External Program Memory Read Cycle



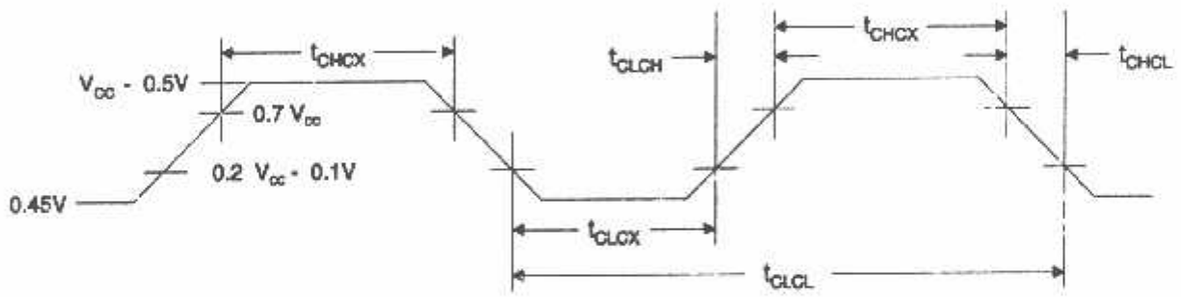
External Data Memory Read Cycle



External Data Memory Write Cycle



External Clock Drive Waveforms



External Clock Drive

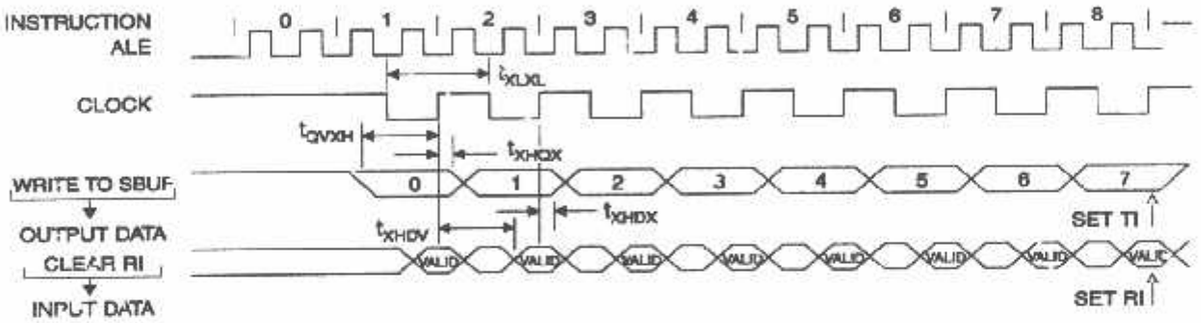
Symbol	Parameter	V_{CC} = 4.0V to 6.0V		Units
		Min	Max	
$1/t_{CLCL}$	Oscillator Frequency	0	24	MHz
t_{CLCL}	Clock Period	41.6		ns
t_{CHCX}	High Time	15		ns
t_{CLCX}	Low Time	15		ns
t_{CLCH}	Rise Time		20	ns
t_{CHCL}	Fall Time		20	ns

Serial Port Timing: Shift Register Mode Test Conditions

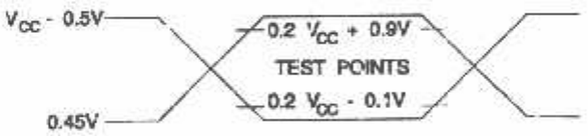
The values in this table are valid for V_{CC} = 4.0V to 6V and Load Capacitance = 80 pF.

Symbol	Parameter	Variable Oscillator		Units
		Min	Max	
t_{XLXL}	Serial Port Clock Cycle Time	$12t_{CLCL}$		µs
t_{QVXH}	Output Data Setup to Clock Rising Edge	$10t_{CLCL}$ - 133		ns
t_{XHQX}	Output Data Hold after Clock Rising Edge	$2t_{CLCL}$ - 117		ns
t_{XHDX}	Input Data Hold after Clock Rising Edge	0		ns
t_{XHDV}	Clock Rising Edge to Input Data Valid		$10t_{CLCL}$ - 133	ns

Shift Register Mode Timing Waveforms

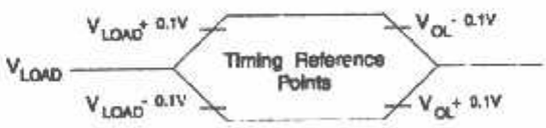


AC Testing Input/Output Waveforms[1]



Note: 1. AC Inputs during testing are driven at V_{CC} - 0.5V for a logic 1 and 0.45V for a logic 0. Timing measurements are made at V_{IH} min. for a logic 1 and V_{IL} max. for a logic 0.

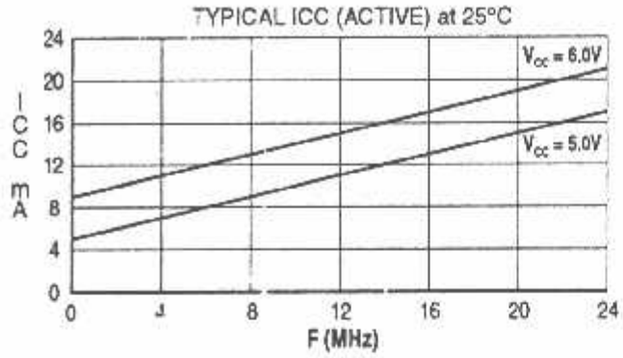
Float Waveforms[1]



Note: 1. For timing purposes, a port pin is no longer floating when a 100 mV change from load voltage occurs. A port pin begins to float when a 100 mV change from the loaded V_{OH}/V_{OL} level occurs.

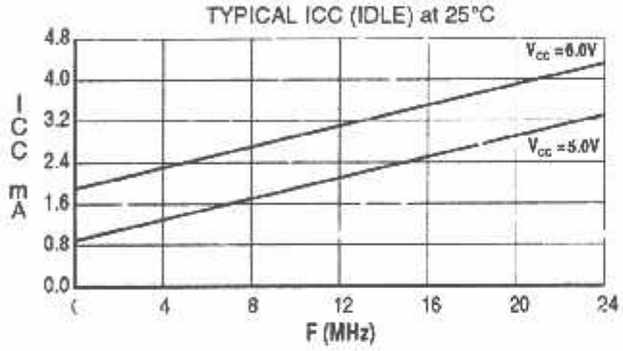
AT89S8252

TYPICAL ICC (ACTIVE) at 25°C



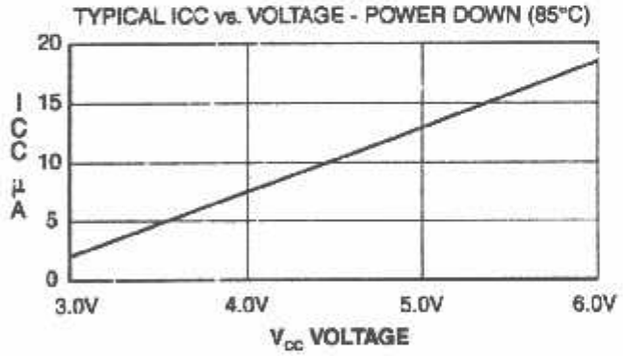
AT89S8252

TYPICAL ICC (IDLE) at 25°C



AT89S8252

TYPICAL ICC vs. VOLTAGE - POWER DOWN (85°C)



Notes: 1. XTAL1 tied to GND for Icc (power-down)
2. Lock bits programmed

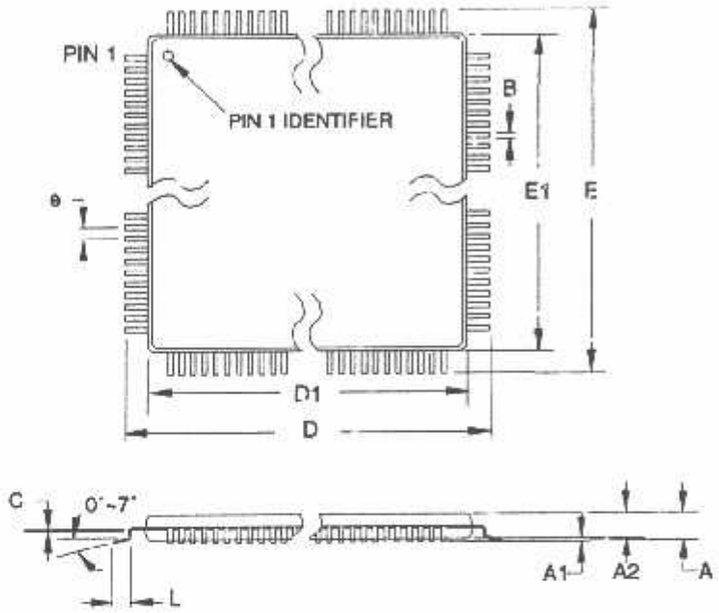
Ordering Information

Speed (MHz)	Power Supply	Ordering Code	Package	Operation Range
24	4.0V to 6.0V	AT89S8252-24AC AT89S8252-24JC AT89S8252-24PC	44A 44J 40P6	Commercial (0°C to 70°C)
	4.0V to 6.0V	AT89S8252-24AI AT89S8252-24JI AT89S8252-24PI	44A 44J 40P6	Industrial (-40°C to 85°C)

Package Type	
44A	44-lead, Thin Plastic Gull Wing Quad Flatpack (TQFP)
44J	44-lead, Plastic J-leaded Chip Carrier (PLCC)
40P6	40-lead, 0.600" Wide, Plastic Dual Inline Package (PDIP)

Packaging Information

44A – TQFP



COMMON DIMENSIONS
(Unit of Measure = mm)

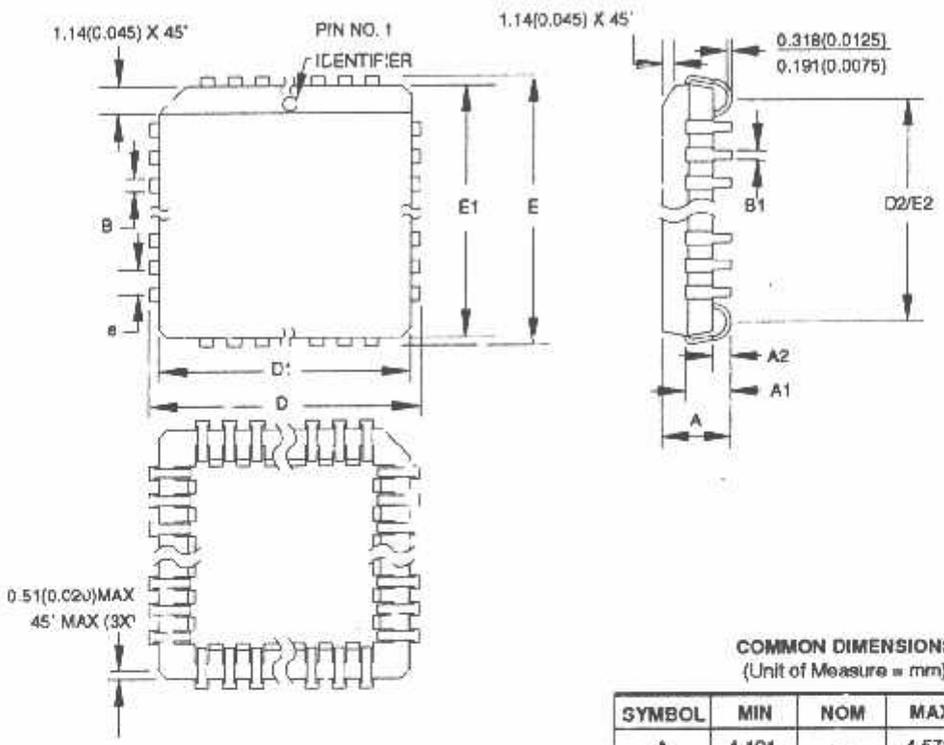
SYMBOL	MIN	NOM	MAX	NOTE
A	–	–	1.20	
A1	0.05	–	0.15	
A2	0.95	1.00	1.05	
D	11.75	12.00	12.25	
D1	9.90	10.00	10.10	Note 2
E	11.75	12.00	12.25	
E1	9.90	10.00	10.10	Note 2
B	0.30	–	0.45	
C	0.09	–	0.20	
L	0.45	–	0.75	
e	0.80 TYP			

Notes:
1. This package conforms to JEDEC reference MS-026, Variation ACB.
2. Dimensions D1 and E1 do not include mold protrusion. Allowable protrusion is 0.25 mm per side. Dimensions D1 and E1 are maximum plastic body size dimensions including mold mismatch.
3. Lead coplanarity is 0.10 mm maximum.

10/5/2001

	TITLE	DRAWING NO.	REV.
2325 Orchard Parkway San Jose, CA 95131	**44A,** 44-lead, 10 x 10 mm Body Size, 1.0 mm Body Thickness, 0.8 mm Lead Pitch, Thin Profile Plastic Quad Flat Package (TQFP)	44A	B

44J – PLCC



COMMON DIMENSIONS
(Unit of Measure = mm)

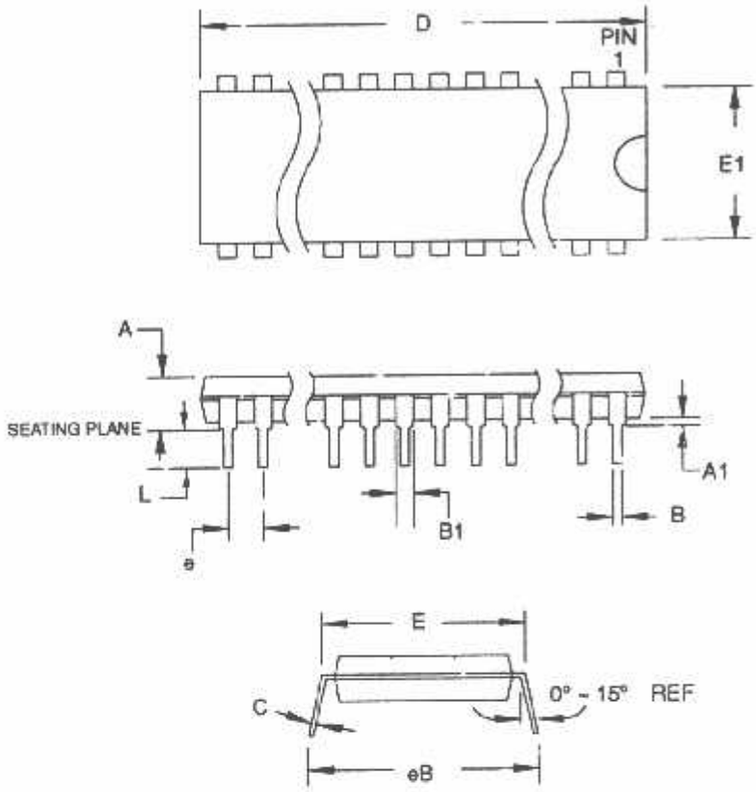
SYMBOL	MIN	NOM	MAX	NOTE
A	4.191	–	4.572	
A1	2.286	–	3.048	
A2	0.508	–	–	
D	17.399	–	17.653	
D1	16.510	–	16.662	Note 2
E	17.399	–	17.653	
E1	16.510	–	16.662	Note 2
D2/E2	14.986	–	16.002	
B	0.660	–	0.813	
B1	0.330	–	0.533	
e	1.270 TYP			

Notes:
1. This package conforms to JEDEC reference MS-016, Variation AC.
2. Dimensions D1 and E1 do not include mold protrusion. Allowable protrusion is .010" (0.254 mm) per side. Dimension D1 and E1 include mold mismatch and are measured at the extreme material condition at the upper or lower parting line.
3. Lead coplanarity is 0.004" (0.102 mm) maximum.

10/04/01

	TITLE	DRAWING NO.	REV.
2325 Orchard Parkway San Jose, CA 95131	**44J**, 44-lead, Plastic J-leaded Chip Carrier (PLCC)	44J	B

40P6 – PDIP



COMMON DIMENSIONS
(Unit of Measure = mm)

SYMBOL	MIN	NOM	MAX	NOTE
A	–	–	4.826	
A1	0.381	–	–	
D	52.070	–	52.578	Note 2
E	15.240	–	15.875	
E1	13.462	–	13.970	Note 2
B	0.356	–	0.559	
B1	1.041	–	1.651	
L	3.048	–	3.556	
C	0.203	–	0.381	
eB	15.494	–	17.526	
e	2.540 TYP			

Notes:
1. This package conforms to JEDEC reference MS-011, Variation AC.
2. Dimensions D and E1 do not include mold Flash or Protrusion. Mold Flash or Protrusion shall not exceed 0.25 mm (0.010").

09/28/01

	TITLE	DRAWING NO.	REV.
2325 Orchard Parkway San Jose, CA 95131	**40P6**, 40-lead (0.600"/15.24 mm Wide) Plastic Dual Inline Package (PDIP)	40P6	B

Features

- Compatible with MCS-51® Products
- 8K Bytes of In-System Programmable (ISP) Flash Memory
  - Endurance: 1000 Write/Erase Cycles
- 4.0V to 5.5V Operating Range
- Fully Static Operation: 0 Hz to 33 MHz
- Three-level Program Memory Lock
- 256 x 8-bit Internal RAM
- 32 Programmable I/O Lines
- Three 16-bit Timer/Counters
- Eight Interrupt Sources
- Full Duplex UART Serial Channel
- Low-power Idle and Power-down Modes
- Interrupt Recovery from Power-down Mode
- Watchdog Timer
- Dual Data Pointer
- Power-off Flag

Description

The AT89S52 is a low-power, high-performance CMOS 8-bit microcontroller with 8K bytes of in-system programmable Flash memory. The device is manufactured using Atmel's high-density nonvolatile memory technology and is compatible with the industry-standard 80C51 instruction set and pinout. The on-chip Flash allows the program memory to be reprogrammed in-system or by a conventional nonvolatile memory programmer. By combining a versatile 8-bit CPU with in-system programmable Flash on a monolithic chip, the Atmel AT89S52 is a powerful microcontroller which provides a highly-flexible and cost-effective solution to many embedded control applications.

The AT89S52 provides the following standard features: 8K bytes of Flash, 256 bytes of RAM, 32 I/O lines, Watchdog timer, two data pointers, three 16-bit timer/counters, a six-vector two-level interrupt architecture, a full duplex serial port, on-chip oscillator, and clock circuitry. In addition, the AT89S52 is designed with static logic for operation down to zero frequency and supports two software selectable power saving modes. The Idle Mode stops the CPU while allowing the RAM, timer/counters, serial port, and interrupt system to continue functioning. The Power-down mode saves the RAM contents but freezes the oscillator, disabling all other chip functions until the next interrupt or hardware reset.

8-bit Microcontroller with 8K Bytes In-System Programmable Flash

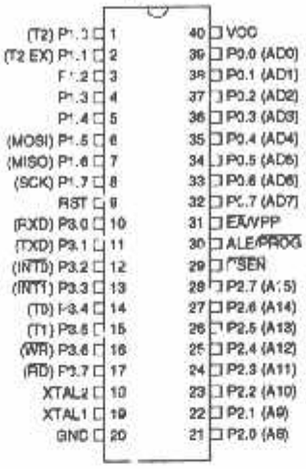
AT89S52

Preliminary

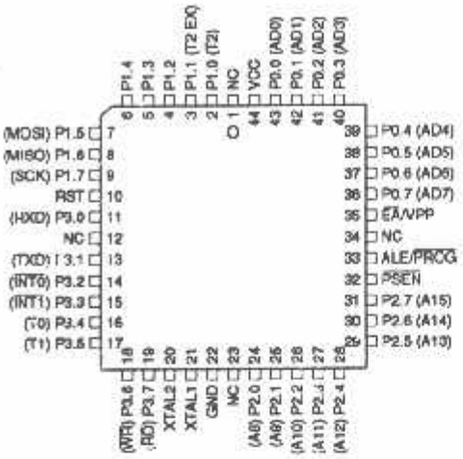
Rev. 1919A-C7/01

Pin Configurations

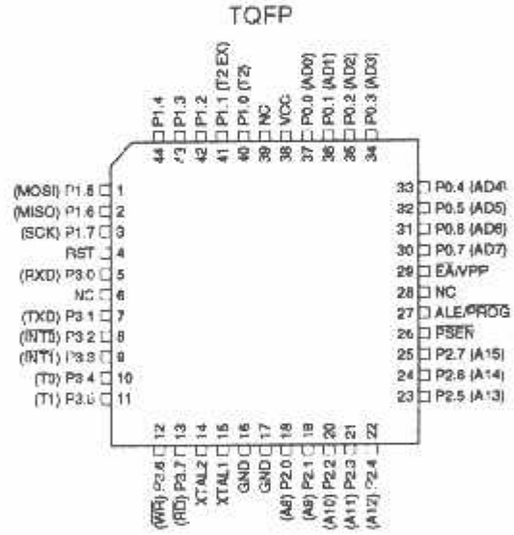
PDIP



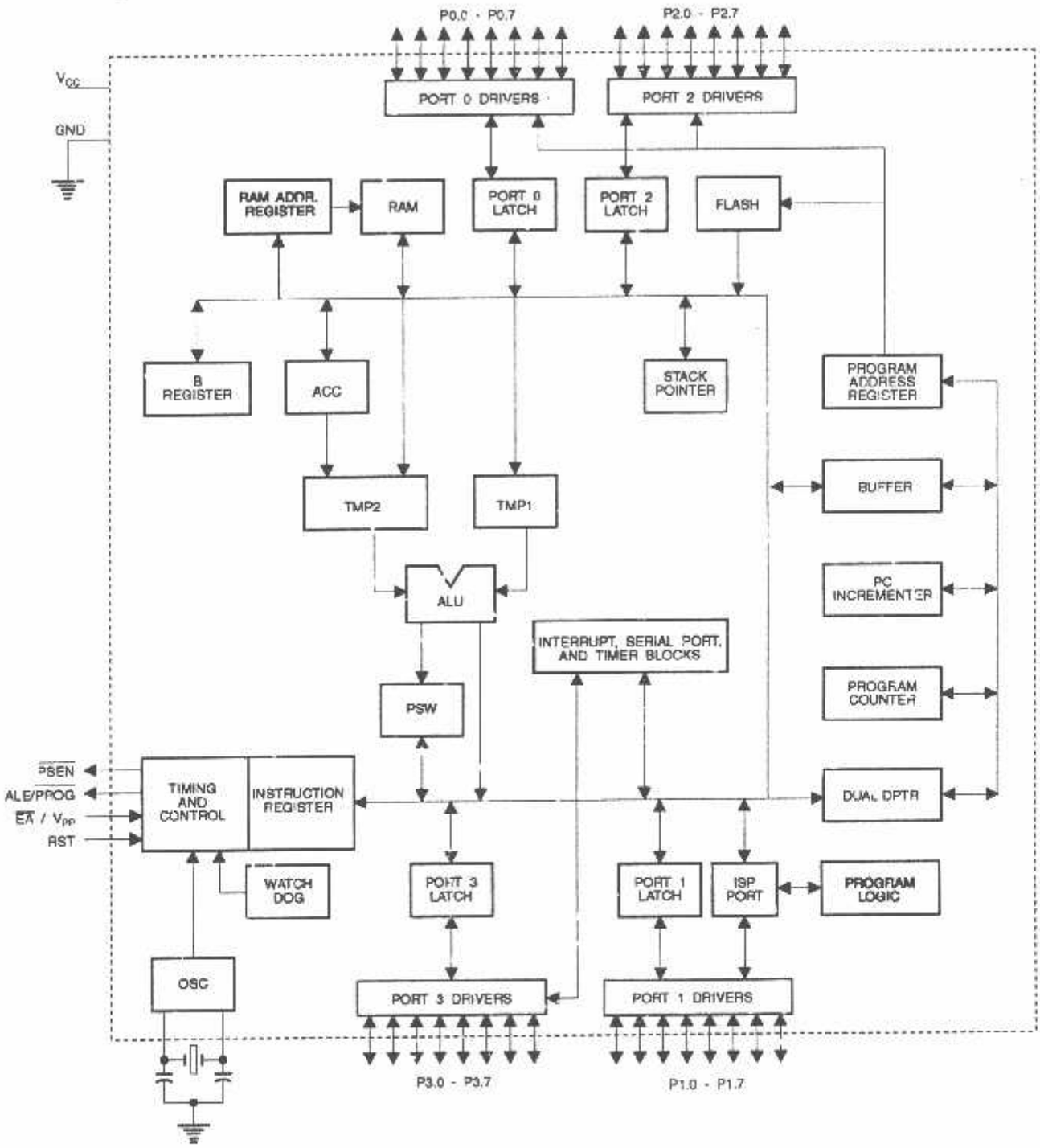
PLCC



TQFP



Block Diagram



Pin Description

VCC
Supply voltage.

GND
Ground.

Port 0
Port 0 is an 8-bit open drain bidirectional I/O port. As an output port, each pin can sink eight TTL inputs. When 1s are written to port 0 pins, the pins can be used as high-impedance inputs.

Port 0 can also be configured to be the multiplexed low-order address/data bus during accesses to external program and data memory. In this mode, P0 has internal pullups.

Port 0 also receives the code bytes during Flash programming and outputs the code bytes during program verification. External pullups are required during program verification.

Port 1
Port 1 is an 8-bit bidirectional I/O port with internal pullups. The Port 1 output buffers can sink/source four TTL inputs. When 1s are written to Port 1 pins, they are pulled high by the internal pullups and can be used as inputs. As inputs, Port 1 pins that are externally being pulled low will source current (I_{IL}) because of the internal pullups.

In addition, P1.0 and P1.1 can be configured to be the timer/counter 2 external count input (P1.0/T2) and the timer/counter 2 trigger input (P1.1/T2EX), respectively, as shown in the following table.

Port 1 also receives the low-order address bytes during Flash programming and verification.

Port Pin	Alternate Functions
P1.0	T2 (external count input to Timer/Counter 2), clock-out
P1.1	T2EX (Timer/Counter 2 capture/reload trigger and direction control)
P1.5	MOSI (used for In-System Programming)
P1.6	MISO (used for In-System Programming)
P1.7	SCK (used for In-System Programming)

Port 2
Port 2 is an 8-bit bidirectional I/O port with internal pullups. The Port 2 output buffers can sink/source four TTL inputs. When 1s are written to Port 2 pins, they are pulled high by the internal pullups and can be used as inputs. As inputs, Port 2 pins that are externally being pulled low will source current (I_{IL}) because of the internal pullups.

Port 2 emits the high-order address byte during fetches from external program memory and during accesses to external data memory that use 16-bit addresses (MOVX @ DPTR). In this application, Port 2 uses strong internal pullups when emitting 1s. During accesses to external data memory that use 8-bit addresses (MOVX @ RI), Port 2 emits the contents of the P2 Special Function Register.

Port 2 also receives the high-order address bits and some control signals during Flash programming and verification.

Port 3
Port 3 is an 8-bit bidirectional I/O port with internal pullups. The Port 3 output buffers can sink/source four TTL inputs. When 1s are written to Port 3 pins, they are pulled high by the internal pullups and can be used as inputs. As inputs, Port 3 pins that are externally being pulled low will source current (I_{IL}) because of the pullups.

Port 3 also serves the functions of various special features of the AT89S52, as shown in the following table.

Port 3 also receives some control signals for Flash programming and verification.

Port Pin	Alternate Functions
P3.0	RXD (serial input port)
P3.1	TXD (serial output port)
P3.2	$\overline{INT0}$ (external interrupt 0)
P3.3	$\overline{INT1}$ (external interrupt 1)
P3.4	T0 (timer 0 external input)
P3.5	T1 (timer 1 external input)
P3.6	$\overline{WR}$ (external data memory write strobe)
P3.7	$\overline{RD}$ (external data memory read strobe)

RST
Reset input. A high on this pin for two machine cycles while the oscillator is running resets the device. This pin drives High for 96 oscillator periods after the Watchdog times out. The DISRTO bit in SFR AUXR (address 8EH) can be used to disable this feature. In the default state of bit DISRTO, the RESET HIGH out feature is enabled.

ALE/$\overline{PROG}$
Address Latch Enable (ALE) is an output pulse for latching the low byte of the address during accesses to external memory. This pin is also the program pulse input ($\overline{PROG}$) during Flash programming.

In normal operation, ALE is emitted at a constant rate of 1/6 the oscillator frequency and may be used for external timing or clocking purposes. Note, however, that one ALE pulse is skipped during each access to external data memory.

If desired, ALE operation can be disabled by setting bit 0 of SFR location 8EH. With the bit set, ALE is active only during a MOVX or MOVC instruction. Otherwise, the pin is

weakly pulled high. Setting the ALE-disable bit has no effect if the microcontroller is in external execution mode.

PSEN

Program Store Enable ($\overline{PSEN}$) is the read strobe to external program memory.

When the AT89S52 is executing code from external program memory, $\overline{PSEN}$ is activated twice each machine cycle, except that two $\overline{PSEN}$ activations are skipped during each access to external data memory.

EA/VPP

External Access Enable. $\overline{EA}$ must be strapped to GND in order to enable the device to fetch code from external program memory locations starting at 0000H up to FFFFH. Note, however, that if lock bit 1 is programmed, $\overline{EA}$ will be internally latched on reset.

$\overline{EA}$ should be strapped to V_{CC} for internal program executions.

This pin also receives the 12-volt programming enable voltage (V_{PP}) during Flash programming.

XTAL1

Input to the inverting oscillator amplifier and input to the internal clock operating circuit.

XTAL2

Output from the inverting oscillator amplifier.

Table 1. AT89S52 SFR Map and Reset Values

0F8H									0FFH
0F0H	B 00000000								0F7H
0E8H									0EFH
0E0H	ACC 00000000								0E7H
0D8H									0DFH
0D0H	PSW 00000000								0D7H
0C8H	T2CON 00000000	T2MOD XXXXXX00	RCAP2L 00000000	RCAP2H 00000000	TL2 00000000	TH2 00000000			0CFH
0C0H									0C7H
0B8H	IP XX000000								0BFH
0B0H	P3 11111111								0B7H
0A8H	IE 0X000000								0AFH
0A0H	P2 11111111		AUXR1 XXXXXXX0				WDTRST XXXXXXXX		0A7H
98H	SCON 00000000	SBUF XXXXXXXX							9FH
90H	P1 11111111								97H
88H	TCON 00000000	TMOD 00000000	TL0 00000000	TL1 00000000	TH0 00000000	TH1 00000000	AUXR XXX00XX0		8FH
80H	P0 11111111	SP 00000111	DP0L 00000000	DP0H 00000000	DP1L 00000000	DP1H 00000000		PCON 0XXX0000	87H

Special Function Registers

A map of the on-chip memory area called the Special Function Register (SFR) space is shown in Table 1.

Note that not all of the addresses are occupied, and unoccupied addresses may not be implemented on the chip. Read accesses to these addresses will in general return random data, and write accesses will have an indeterminate effect.

User software should not write 1s to these unlisted locations, since they may be used in future products to invoke new features. In that case, the reset or inactive values of the new bits will always be 0.

Timer 2 Registers: Control and status bits are contained in registers T2CON (shown in Table 2) and T2MOD (shown in Table 3) for Timer 2. The register pair (RCAP2H, RCAP2L) are the Capture/Reload registers for Timer 2 in 16-bit capture mode or 16-bit auto-reload mode.

Interrupt Registers: The individual interrupt enable bits are in the IE register. Two priorities can be set for each of the six interrupt sources in the IP register.

Table 2. T2CON – Timer/Counter 2 Control Register

T2CON Address = 0C8H — Reset Value = 0000 0000B

Bit Addressable

Bit	TF2	EXF2	RCLK	TCLK	EXEN2	TR2	C/$\overline{T2}$	CP/$\overline{RL2}$
	7	6	5	4	3	2	1	0

Symbol	Function
TF2	Timer 2 overflow flag set by a Timer 2 overflow and must be cleared by software. TF2 will not be set when either RCLK = 1 or TCLK = 1.
EXF2	Timer 2 external flag set when either a capture or reload is caused by a negative transition on T2EX and EXEN2 = 1. When Timer 2 interrupt is enabled, EXF2 = 1 will cause the CPU to vector to the Timer 2 interrupt routine. EXF2 must be cleared by software. EXF2 does not cause an interrupt in up/down counter mode (DCEN = 1).
RCLK	Receive clock enable. When set, causes the serial port to use Timer 2 overflow pulses for its receive clock in serial port Modes 1 and 3. RCLK = 0 causes Timer 1 overflow to be used for the receive clock.
TCLK	Transmit clock enable. When set, causes the serial port to use Timer 2 overflow pulses for its transmit clock in serial port Modes 1 and 3. TCLK = 0 causes Timer 1 overflows to be used for the transmit clock.
EXEN2	Timer 2 external enable. When set, allows a capture or reload to occur as a result of a negative transition on T2EX if Timer 2 is not being used to clock the serial port. EXEN2 = 0 causes Timer 2 to ignore events at T2EX.
TR2	Start/Stop control for Timer 2. TR2 = 1 starts the timer.
C/$\overline{T2}$	Timer or counter select for Timer 2. C/$\overline{T2}$ = 0 for timer function. C/$\overline{T2}$ = 1 for external event counter (falling edge triggered).
CP/$\overline{RL2}$	Capture/Reload select. CP/$\overline{RL2}$ = 1 causes captures to occur on negative transitions at T2EX if EXEN2 = 1. CP/$\overline{RL2}$ = 0 causes automatic reloads to occur when Timer 2 overflows or negative transitions occur at T2EX when EXEN2 = 1. When either RCLK or TCLK = 1, this bit is ignored and the timer is forced to auto-reload on Timer 2 overflow.

Table 3a. AUXR: Auxiliary Register

AUXR — Address = 8EH — Reset Value = XXX00XX0B

Not Bit Addressable

Bit	7	6	5	4	3	2	1	0
	–	–	–	WDIDLE	DISRTO	–	–	DISALE

–: Reserved for future expansion

DISALE: Disable/Enable ALE

DISALE	Operating Mode
0	ALE is emitted at a constant rate of 1/6 the oscillator frequency
1	ALE is active only during a MOVX or MOVC instruction

DISRTO: Disable/Enable Reset out

DISRTO	
0	Reset pin is driven High after WDT times out
1	Reset pin is input only

WDIDLE: Disable/Enable WDT in IDLE mode

WDIDLE	
0	WDT continues to count in IDLE mode
1	WDT halts counting in IDLE mode

Dual Data Pointer Registers: To facilitate accessing both internal and external data memory, two banks of 16-bit Data Pointer Registers are provided: DP0 at SFR address locations 82H-83H and DP1 at 84H-85H. Bit DPS = 0 in SFR AUXR1 selects DP0 and DPS = 1 selects DP1. The user should always initialize the DPS bit to the appropriate value before accessing the respective Data Pointer Register.

Power Off Flag: The Power Off Flag (POF) is located at bit 4 (PCON.4) in the PCON SFR. POF is set to "1" during power up. It can be set and rest under software control and is not affected by reset.

Table 3b. AUXR1: Auxiliary Register 1

AUXR1 — Address = A2H — Reset Value = XXXXXXX0B

Not Bit Addressable

Bit	7	6	5	4	3	2	1	0
	–	–	–	–	–	–	–	DPS

–: Reserved for future expansion

DPS: Data Pointer Register Select

DPS	
0	Selects DPTR Registers DP0L, DP0H
1	Selects DPTR Registers DP1L, DP1H

Memory Organization

MCS-51 devices have a separate address space for Program and Data Memory. Up to 64K bytes each of external Program and Data Memory can be addressed.

Program Memory

If the $\overline{EA}$ pin is connected to GND, all program fetches are directed to external memory.

On the AT89S52, if $\overline{EA}$ is connected to V_{CC}, program fetches to addresses 0000H through 1FFFH are directed to internal memory and fetches to addresses 2000H through FFFFH are to external memory.

Data Memory

The AT89S52 implements 256 bytes of on-chip RAM. The upper 128 bytes occupy a parallel address space to the Special Function Registers. This means that the upper 128 bytes have the same addresses as the SFR space but are physically separate from SFR space.

When an instruction accesses an internal location above address 7FH, the address mode used in the instruction specifies whether the CPU accesses the upper 128 bytes of RAM or the SFR space. Instructions which use direct addressing access of the SFR space.

For example, the following direct addressing instruction accesses the SFR at location 0A0H (which is P2).

```
MOV 0A0H, #data
```

Instructions that use indirect addressing access the upper 128 bytes of RAM. For example, the following indirect addressing instruction, where R0 contains 0A0H, accesses the data byte at address 0A0H, rather than P2 (whose address is 0A0H).

```
MOV @R0, #data
```

Note that stack operations are examples of indirect addressing, so the upper 128 bytes of data RAM are available as stack space.

Watchdog Timer (One-time Enabled with Reset-out)

The WDT is intended as a recovery method in situations where the CPU may be subjected to software upsets. The WDT consists of a 13-bit counter and the Watchdog Timer Reset (WDTRST) SFR. The WDT is defaulted to disable from exiting reset. To enable the WDT, a user must write 01EH and 0E1H in sequence to the WDTRST register (SFR location 0A6H). When the WDT is enabled, it will increment every machine cycle while the oscillator is running. The WDT timeout period is dependent on the external clock frequency. There is no way to disable the WDT except through reset (either hardware reset or WDT overflow reset). When WDT overflows, it will drive an output RESET HIGH pulse at the RST pin.

Using the WDT

To enable the WDT, a user must write 01EH and 0E1H in sequence to the WDTRST register (SFR location 0A6H). When the WDT is enabled, the user needs to service it by writing 01EH and 0E1H to WDTRST to avoid a WDT overflow. The 13-bit counter overflows when it reaches 8191 (1FFFH), and this will reset the device. When the WDT is enabled, it will increment every machine cycle while the oscillator is running. This means the user must reset the WDT at least every 8191 machine cycles. To reset the WDT the user must write 01EH and 0E1H to WDTRST. WDTRST is a write-only register. The WDT counter cannot be read or written. When WDT overflows, it will generate an output RESET pulse at the RST pin. The RESET pulse duration is 96xTOSC, where TOSC=1/FOSC. To make the best use of the WDT, it should be serviced in those sections of code that will periodically be executed within the time required to prevent a WDT reset.

WDT During Power-down and Idle

In Power-down mode the oscillator stops, which means the WDT also stops. While in Power-down mode, the user does not need to service the WDT. There are two methods of exiting Power-down mode: by a hardware reset or via a level-activated external interrupt which is enabled prior to entering Power-down mode. When Power-down is exited with hardware reset, servicing the WDT should occur as it normally does whenever the AT89S52 is reset. Exiting Power-down with an interrupt is significantly different. The interrupt is held low long enough for the oscillator to stabilize. When the interrupt is brought high, the interrupt is serviced. To prevent the WDT from resetting the device while the interrupt pin is held low, the WDT is not started until the interrupt is pulled high. It is suggested that the WDT be reset during the interrupt service for the interrupt used to exit Power-down mode.

To ensure that the WDT does not overflow within a few states of exiting Power-down, it is best to reset the WDT just before entering Power-down mode.

Before going into the IDLE mode, the WDIDLE bit in SFR AUXR is used to determine whether the WDT continues to count if enabled. The WDT keeps counting during IDLE (WDIDLE bit = 0) as the default state. To prevent the WDT from resetting the AT89S52 while in IDLE mode, the user should always set up a timer that will periodically exit IDLE, service the WDT, and reenter IDLE mode.

With WDIDLE bit enabled, the WDT will stop to count in IDLE mode and resumes the count upon exit from IDLE.

UART

The UART in the AT89S52 operates the same way as the UART in the AT89C51 and AT89C52. For further information on the UART operation, refer to the ATMEL Web site (http://www.atmel.com). From the home page, select 'Products', then '8051-Architecture Flash Microcontroller', then 'Product Overview'.

Timer 0 and 1

Timer 0 and Timer 1 in the AT89S52 operate the same way as Timer 0 and Timer 1 in the AT89C51 and AT89C52. For further information on the timers' operation, refer to the ATMEL Web site (http://www.atmel.com). From the home page, select 'Products', then '8051-Architecture Flash Microcontroller', then 'Product Overview'.

Timer 2

Timer 2 is a 16-bit Timer/Counter that can operate as either a timer or an event counter. The type of operation is selected by bit C/$\overline{T2}$ in the SFR T2CON (shown in Table 2). Timer 2 has three operating modes: capture, auto-reload (up or down counting), and baud rate generator. The modes are selected by bits in T2CON, as shown in Table 3. Timer 2 consists of two 8-bit registers, TH2 and TL2. In the Timer function, the TL2 register is incremented every machine cycle. Since a machine cycle consists of 12 oscillator periods, the count rate is 1/12 of the oscillator frequency.

Table 3. Timer 2 Operating Modes

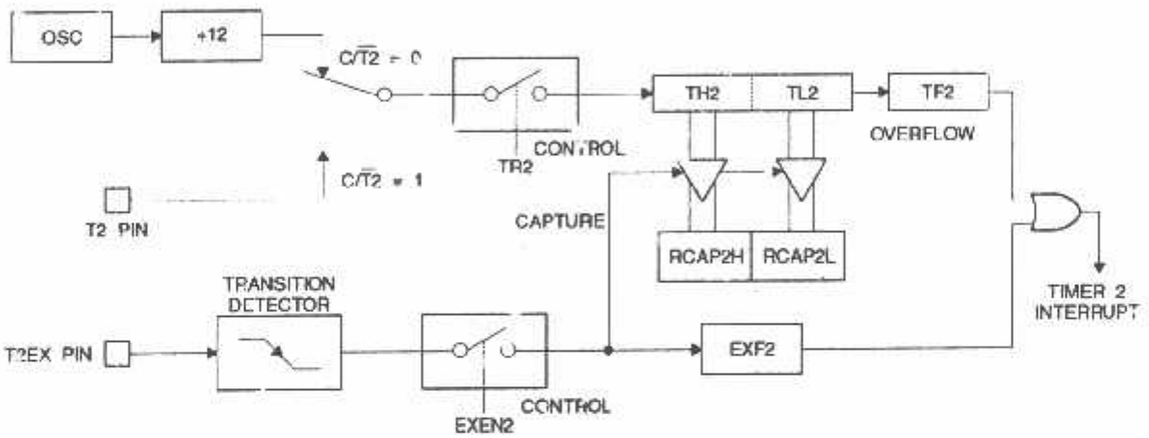
RCLK +TCLK	CP/$\overline{RL2}$	TR2	MODE
0	0	1	16-bit Auto-reload
0	1	1	16-bit Capture
1	X	1	Baud Rate Generator
X	X	0	(Off)

In the Counter function, the register is incremented in response to a 1-to-0 transition at its corresponding external input pin, T2. In this function, the external input is sampled during S5P2 of every machine cycle. When the samples show a high in one cycle and a low in the next cycle, the count is incremented. The new count value appears in the register during S3P1 of the cycle following the one in which the transition was detected. Since two machine cycles (24 oscillator periods) are required to recognize a 1-to-0 transition, the maximum count rate is 1/24 of the oscillator frequency. To ensure that a given level is sampled at least once before it changes, the level should be held for at least one full machine cycle.

Capture Mode

In the capture mode, two options are selected by bit EXEN2 in T2CON. If EXEN2 = 0, Timer 2 is a 16-bit timer or counter which upon overflow sets bit TF2 in T2CON. This bit can then be used to generate an interrupt. If EXEN2 = 1, Timer 2 performs the same operation, but a 1-to-0 transition at external input T2EX also causes the current value in TH2 and TL2 to be captured into RCAP2H and RCAP2L, respectively. In addition, the transition at T2EX causes bit EXF2 in T2CON to be set. The EXF2 bit, like TF2, can generate an interrupt. The capture mode is illustrated in Figure 5.

Figure 5. Timer in Capture Mode



Auto-reload (Up or Down Counter)

Timer 2 can be programmed to count up or down when configured in its 16-bit auto-reload mode. This feature is invoked by the DCEN (Down Counter Enable) bit located in the SFR T2MOD (see Table 4). Upon reset, the DCEN bit is set to 0 so that timer 2 will default to count up. When DCEN is set, Timer 2 can count up or down, depending on the value of the T2EX pin.

Figure 6 shows Timer 2 automatically counting up when DCEN=0. In this mode, two options are selected by bit EXEN2 in T2CON. If EXEN2 = 0, Timer 2 counts up to 0FFFFH and then sets the TF2 bit upon overflow. The overflow also causes the timer registers to be reloaded with the 16-bit value in RCAP2H and RCAP2L. The values in Timer in Capture ModeRCAP2H and RCAP2L are preset by software. If EXEN2 = 1, a 16-bit reload can be triggered either by an overflow or by a 1-to-0 transition at external input T2EX. This transition also sets the EXF2 bit. Both the TF2 and EXF2 bits can generate an interrupt if enabled.

Setting the DCEN bit enables Timer 2 to count up or down, as shown in Figure 6. In this mode, the T2EX pin controls the direction of the count. A logic 1 at T2EX makes Timer 2 count up. The timer will overflow at 0FFFFH and set the TF2 bit. This overflow also causes the 16-bit value in RCAP2H and RCAP2L to be reloaded into the timer registers, TH2 and TL2, respectively.

A logic 0 at T2EX makes Timer 2 count down. The timer underflows when TH2 and TL2 equal the values stored in RCAP2H and RCAP2L. The underflow sets the TF2 bit and causes 0FFFFH to be reloaded into the timer registers.

The EXF2 bit toggles whenever Timer 2 overflows or underflows and can be used as a 17th bit of resolution. In this operating mode, EXF2 does not flag an interrupt.

Figure 6. Timer 2 Auto Reload Mode (DCEN = 0)

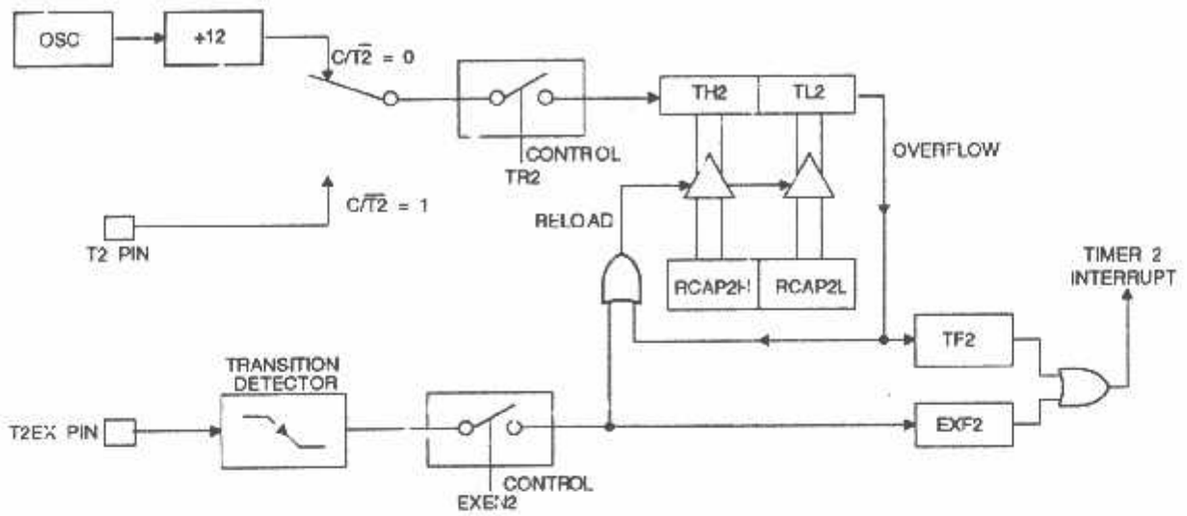


Table 4. T2MOD – Timer 2 Mode Control Register

T2MOD Address = 0C9H — Reset Value = XXXX XX00B

Not Bit Addressable

Bit	7	6	5	4	3	2	1	0
	–	–	–	–	–	–	T2OE	DCEN

Symbol	Function
–	Not implemented, reserved for future
T2OE	Timer 2 Output Enable bit
DCEN	When set, this bit allows Timer 2 to be configured as an up/down counter

Figure 7. Timer 2 Auto Reload Mode (DCEN = 1)

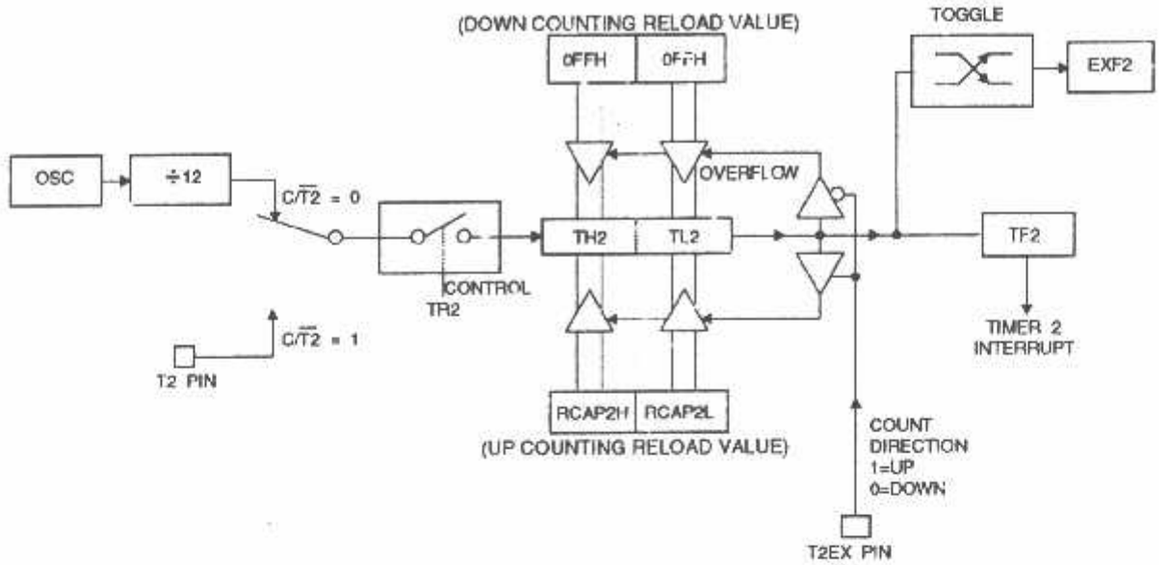
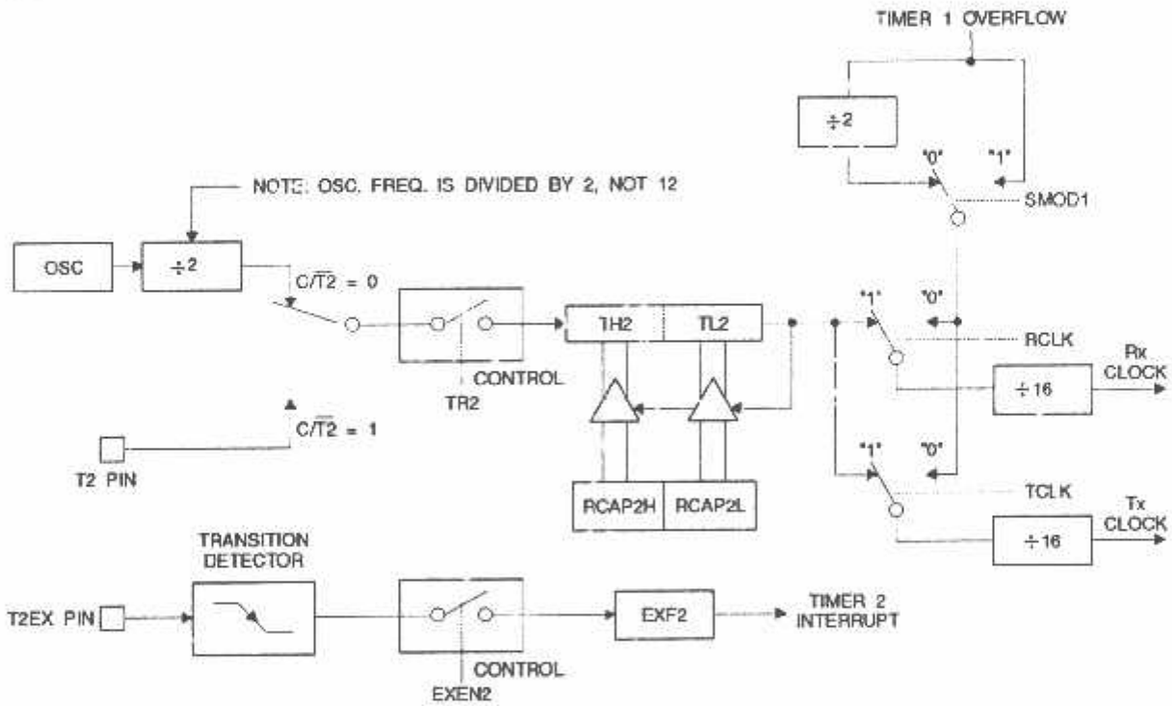


Figure 8. Timer 2 in Baud Rate Generator Mode



Baud Rate Generator

Timer 2 is selected as the baud rate generator by setting TCLK and/or RCLK in T2CON (Table 2). Note that the baud rates for transmit and receive can be different if Timer 2 is used for the receiver or transmitter and Timer 1 is used for the other function. Setting RCLK and/or TCLK puts Timer 2 into its baud rate generator mode, as shown in Figure 8.

The baud rate generator mode is similar to the auto-reload mode, in that a rollover in TH2 causes the Timer 2 registers to be reloaded with the 16-bit value in registers RCAP2H and RCAP2L, which are preset by software.

The baud rates in Modes 1 and 3 are determined by Timer 2's overflow rate according to the following equation.

$$\text{Modes 1 and 3 Baud Rates} = \frac{\text{Timer 2 Overflow Rate}}{16}$$

The Timer can be configured for either timer or counter operation. In most applications, it is configured for timer operation ($C/\overline{T2} = 0$). The timer operation is different for Timer 2 when it is used as a baud rate generator. Normally, as a timer, it increments every machine cycle (at 1/12 the oscillator frequency). As a baud rate generator, however, it increments every state time (at 1/2 the oscillator frequency). The baud rate formula is given below.

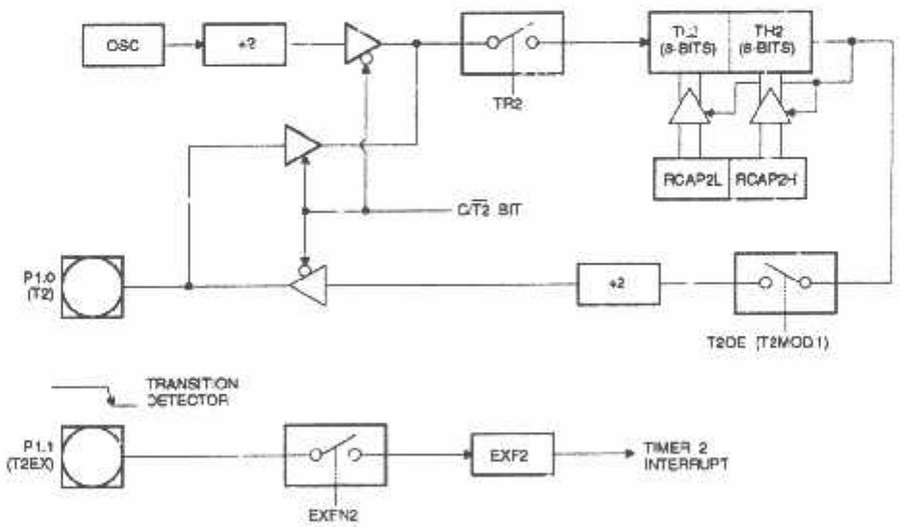
$$\frac{\text{Modes 1 and 3}}{\text{Baud Rate}} = \frac{\text{Oscillator Frequency}}{32 \times [65536\text{-RCAP2H,RCAP2L})]}$$

where (RCAP2H, RCAP2L) is the content of RCAP2H and RCAP2L taken as a 16-bit unsigned integer.

Timer 2 as a baud rate generator is shown in Figure 8. This figure is valid only if RCLK or TCLK = 1 in T2CON. Note that a rollover in TH2 does not set TF2 and will not generate an interrupt. Note too, that if EXEN2 is set, a 1-to-0 transition in T2EX will set EXF2 but will not cause a reload from (RCAP2H, RCAP2L) to (TH2, TL2). Thus, when Timer 2 is in use as a baud rate generator, T2EX can be used as an extra external interrupt.

Note that when Timer 2 is running (TR2 = 1) as a timer in the baud rate generator mode, TH2 or TL2 should not be read from or written to. Under these conditions, the Timer is incremented every state time, and the results of a read or write may not be accurate. The RCAP2 registers may be read but should not be written to, because a write might overlap a reload and cause write and/or reload errors. The timer should be turned off (clear TR2) before accessing the Timer 2 or RCAP2 registers.

Figure 9. Timer 2 in Clock-Out Mode



Programmable Clock Out

A 50% duty cycle clock can be programmed to come out on P1.0, as shown in Figure 9. This pin, besides being a regular I/O pin, has two alternate functions. It can be programmed to input the external clock for Timer/Counter 2 or to output a 50% duty cycle clock ranging from 61 Hz to 4 MHz at a 16 MHz operating frequency.

To configure the Timer/Counter 2 as a clock generator, bit C/$\overline{T2}$ (T2CON.1) must be cleared and bit T2OE (T2MOD.1) must be set. Bit TR2 (T2CON.2) starts and stops the timer.

The clock-out frequency depends on the oscillator frequency and the reload value of Timer 2 capture registers (RCAP2H, RCAP2L), as shown in the following equation.

$$\text{Clock-Out Frequency} = \frac{\text{Oscillator Frequency}}{4 \times [65536-(\text{RCAP2H,RCAP2L})]}$$

In the clock-out mode, Timer 2 roll-overs will not generate an interrupt. This behavior is similar to when Timer 2 is used as a baud-rate generator. It is possible to use Timer 2 as a baud-rate generator and a clock generator simultaneously. Note, however, that the baud-rate and clock-out frequencies cannot be determined independently from one another since they both use RCAP2H and RCAP2L.

Interrupts

The AT89S52 has a total of six interrupt vectors: two external interrupts ($\overline{INT0}$ and $\overline{INT1}$), three timer interrupts (Timers 0, 1, and 2), and the serial port interrupt. These interrupts are all shown in Figure 10.

Each of these interrupt sources can be individually enabled or disabled by setting or clearing a bit in Special Function Register IE. IE also contains a global disable bit, EA, which disables all interrupts at once.

Note that Table 5 shows that bit position IE.6 is unimplemented. In the AT89S52, bit position IE.5 is also unimplemented. User software should not write 1s to these bit positions, since they may be used in future AT89 products.

Timer 2 interrupt is generated by the logical OR of bits TF2 and EXF2 in register T2CON. Neither of these flags is cleared by hardware when the service routine is vectored to. In fact, the service routine may have to determine whether it was TF2 or EXF2 that generated the interrupt, and that bit will have to be cleared in software.

The Timer 0 and Timer 1 flags, TF0 and TF1, are set at S5P2 of the cycle in which the timers overflow. The values are then polled by the circuitry in the next cycle. However, the Timer 2 flag, TF2, is set at S2P2 and is polled in the same cycle in which the timer overflows.

Table 5. Interrupt Enable (IE) Register

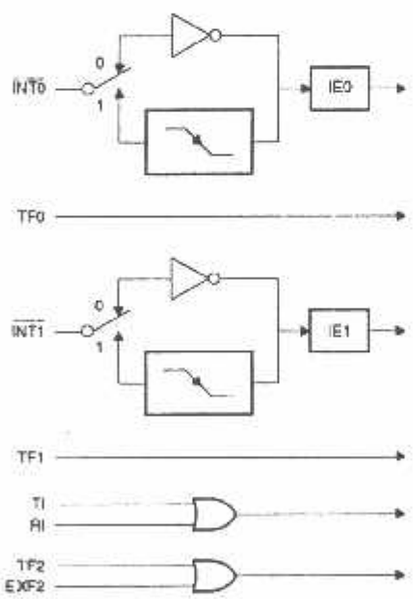
(MSB)							(LSB)
EA	--	ET2	ES	ET1	EX1	ET0	EX0

Enable Bit = 1 enables the interrupt.

Enable Bit = 0 disables the interrupt.

Symbol	Position	Function
EA	IE.7	Disables all interrupts. If EA = 0, no interrupt is acknowledged. If EA = 1, each interrupt source is individually enabled or disabled by setting or clearing its enable bit.
-	IE.6	Reserved.
ET2	IE.5	Timer 2 interrupt enable bit.
ES	IE.4	Serial Port interrupt enable bit.
ET1	IE.3	Timer 1 interrupt enable bit.
EX1	IE.2	External interrupt 1 enable bit.
ET0	IE.1	Timer 0 interrupt enable bit.
EX0	IE.0	External interrupt 0 enable bit.
User software should never write 1s to unimplemented bits, because they may be used in future AT89 products.		

Figure 10. Interrupt Sources



Oscillator Characteristics

XTAL1 and XTAL2 are the input and output, respectively, of an inverting amplifier that can be configured for use as an on-chip oscillator, as shown in Figure 11. Either a quartz crystal or ceramic resonator may be used. To drive the device from an external clock source, XTAL2 should be left unconnected while XTAL1 is driven, as shown in Figure 12. There are no requirements on the duty cycle of the external clock signal, since the input to the internal clocking circuitry is through a divide-by-two flip-flop, but minimum and maximum voltage high and low time specifications must be observed.

Idle Mode

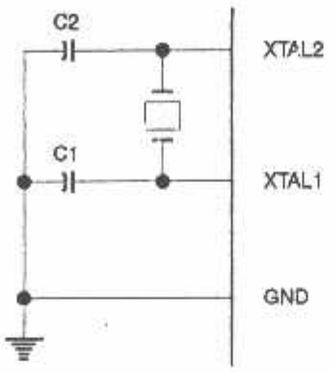
In idle mode, the CPU puts itself to sleep while all the on-chip peripherals remain active. The mode is invoked by software. The content of the on-chip RAM and all the special functions registers remain unchanged during this mode. The idle mode can be terminated by any enabled interrupt or by a hardware reset.

Note that when idle mode is terminated by a hardware reset, the device normally resumes program execution from where it left off, up to two machine cycles before the internal reset algorithm takes control. On-chip hardware inhibits access to internal RAM in this event, but access to the port pins is not inhibited. To eliminate the possibility of an unexpected write to a port pin when idle mode is terminated by a reset, the instruction following the one that invokes idle mode should not write to a port pin or to external memory.

Power-down Mode

In the Power-down mode, the oscillator is stopped, and the instruction that invokes Power-down is the last instruction executed. The on-chip RAM and Special Function Registers retain their values until the Power-down mode is terminated. Exit from Power-down mode can be initiated either by a hardware reset or by an enabled external interrupt. Reset redefines the SFRs but does not change the on-chip RAM. The reset should not be activated before V_{CC} is restored to its normal operating level and must be held active long enough to allow the oscillator to restart and stabilize.

Figure 11. Oscillator Connections



Note: C1, C2 = 30 pF ± 10 pF for Crystals
= 40 pF ± 10 pF for Ceramic Resonators

Figure 12. External Clock Drive Configuration

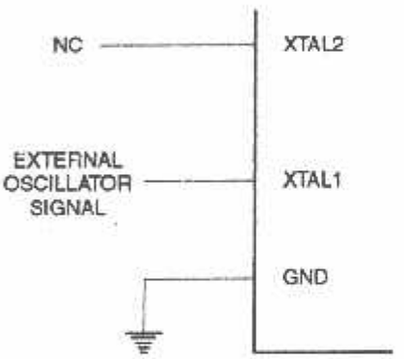


Table 6. Status of External Pins During Idle and Power-down Modes

Mode	Program Memory	ALE	$\overline{PSEN}$	PORT0	PORT1	PORT2	PORT3
Idle	Internal	1	1	Data	Data	Data	Data
Idle	External	1	1	Float	Data	Address	Data
Power-down	Internal	0	0	Data	Data	Data	Data
Power-down	External	0	0	Float	Data	Data	Data

Program Memory Lock Bits

The AT89S52 has three lock bits that can be left unprogrammed (U) or can be programmed (P) to obtain the additional features listed in the following table.

Table 7. Lock Bit Protection Modes

Program Lock Bits				
	LB1	LB2	LB3	Protection Type
1	U	U	U	No program lock features
2	P	U	U	MOVC instructions executed from external program memory are disabled from fetching code bytes from internal memory, $\overline{EA}$ is sampled and latched on reset, and further programming of the Flash memory is disabled
3	P	P	U	Same as mode 2, but verify is also disabled
4	P	P	P	Same as mode 3, but external execution is also disabled

When lock bit 1 is programmed, the logic level at the $\overline{EA}$ pin is sampled and latched during reset. If the device is powered up without a reset, the latch initializes to a random value and holds that value until reset is activated. The latched value of $\overline{EA}$ must agree with the current logic level at that pin in order for the device to function properly.

Programming the Flash – Parallel Mode

The AT89S52 is shipped with the on-chip Flash memory array ready to be programmed. The programming interface needs a high-voltage (12-volt) program enable signal and is compatible with conventional third-party Flash or EPROM programmers.

The AT89S52 code memory array is programmed byte-by-byte.

Programming Algorithm: Before programming the AT89S52, the address, data, and control signals should be set up according to the Flash programming mode table and figures 13 and 14. To program the AT89S52, take the following steps:

1. Input the desired memory location on the address lines.
2. Input the appropriate data byte on the data lines.
3. Activate the correct combination of control signals.
4. Raise $\overline{EA}/V_{PP}$ to 12V.
5. Pulse ALE/$\overline{PROG}$ once to program a byte in the Flash array or the lock bits. The byte-write cycle is self-timed and typically takes no more than 50 µs.
6. Repeat steps 1 through 5, changing the address and data for the entire array or until the end of the object file is reached.

Data Polling: The AT89S52 features $\overline{Data}$ Polling to indicate the end of a byte write cycle. During a write cycle, an attempted read of the last byte written will result in the complement of the written data on P0.7. Once the write cycle has been completed, true data is valid on all outputs, and the next cycle may begin. $\overline{Data}$ Polling may begin any time after a write cycle has been initiated.

Ready/$\overline{Busy}$: The progress of byte programming can also be monitored by the RDY/$\overline{BSY}$ output signal. P3.0 is pulled low after ALE goes high during programming to indicate $\overline{BUSY}$. P3.0 is pulled high again when programming is done to indicate READY.

Program Verify: If lock bits LB1 and LB2 have not been programmed, the programmed code data can be read back via the address and data lines for verification. The status of the individual lock bits can be verified directly by reading them back.

Reading the Signature Bytes: The signature bytes are read by the same procedure as a normal verification of locations 000H, 100H, and 200H, except that P3.6 and P3.7 must be pulled to a logic low. The values returned are as follows.

(000H) = 1EH indicates manufactured by Atmel
(100H) = 52H indicates 89S52
(200H) = 06H

Chip Erase: In the parallel programming mode, a chip erase operation is initiated by using the proper combination of control signals and by pulsing ALE/$\overline{PROG}$ low for a duration of 200 ns - 500 ns.

In the serial programming mode, a chip erase operation is initiated by issuing the Chip Erase instruction. In this mode, chip erase is self-timed and takes about 500 ms.

During chip erase, a serial read from any address location will return 00H at the data output.

Programming the Flash – Serial Mode

The Code memory array can be programmed using the serial ISP interface while RST is pulled to V_{CC}. The serial interface consists of pins SCK, MOSI (input) and MISO (output). After RST is set high, the Programming Enable instruction needs to be executed first before other operations can be executed. Before a reprogramming sequence can occur, a Chip Erase operation is required.

The Chip Erase operation turns the content of every memory location in the Code array into FFH.

Either an external system clock can be supplied at pin XTAL1 or a crystal needs to be connected across pins XTAL1 and XTAL2. The maximum serial clock (SCK)

frequency should be less than 1/16 of the crystal frequency. With a 33 MHz oscillator clock, the maximum SCK frequency is 2 MHz.

Serial Programming Algorithm

To program and verify the AT89S52 in the serial programming mode, the following sequence is recommended:

1. Power-up sequence:

   Apply power between VCC and GND pins.

   Set RST pin to "H".

   If a crystal is not connected across pins XTAL1 and XTAL2, apply a 3 MHz to 33 MHz clock to XTAL1 pin and wait for at least 10 milliseconds.
2. Enable serial programming by sending the Programming Enable serial instruction to pin MOSI/P1.5. The frequency of the shift clock supplied at pin SCK/P1.7 needs to be less than the CPU clock at XTAL1 divided by 16.
3. The Code array is programmed one byte at a time by supplying the address and data together with the appropriate Write instruction. The write cycle is self timed and typically takes less than 1 ms at 5V.
4. Any memory location can be verified by using the Read instruction which returns the content at the selected address at serial output MISO/P1.6.
5. At the end of a programming session, RST can be set low to commence normal device operation.

Power-off sequence (if needed)

Set XTAL1 to "L" (if a crystal is not used).

Set RST to "L".

Turn V_{CC} power off.

Data Polling: The Data Polling feature is also available in the serial mode. In this mode, during a write cycle an attempted read of the last byte written will result in the complement of the MSB of the serial output byte on MISO.

Serial Programming Instruction Set

The Instruction Set for Serial Programming follows a 4-byte protocol and is shown in Table 10.

Programming Interface – Parallel Mode

Every code byte in the Flash array can be programmed by using the appropriate combination of control signals. The write operation cycle is self-timed and once initiated, will automatically time itself to completion.

All major programming vendors offer worldwide support for the Atmel microcontroller series. Please contact your local programming vendor for the appropriate software revision.

Table 8. Flash Programming Modes

Mode	V_{CC}	RST	$\overline{PSEN}$	ALE/ $\overline{PROG}$	$\overline{EA}$/ V_{PP}	P2.6	P2.7	P3.3	P3.6	P3.7	P0.7-0 Data	P2.4-0 Address	P1.7-0 Address
Write Code Data	5V	H	L	(2)	12V	L	H	H	H	H	D_{IN}	A12-8	A7-0
Read Code Data	5V	H	L	H	H	L	L	L	H	H	D_{OUT}	A12-8	A7-0
Write Lock Bit 1	5V	H	L	(3)	12V	H	H	H	H	H	X	X	X
Write Lock Bit 2	5V	H	L	(3)	12V	H	H	H	L	L	X	X	X
Write Lock Bit 3	5V	H	L	(3)	12V	H	L	H	H	L	X	X	X
Read Lock Bits 1, 2, 3	5V	H	L	H	H	H	H	L	H	L	P0.2, P0.3, P0.4	X	X
Chip Erase	5V	H	L	(1)	12V	H	L	H	L	L	X	X	X
Read Atmel ID	5V	H	L	H	H	L	L	L	L	L	1EH	X 0000	00H
Read Device ID	5V	H	L	H	H	L	L	L	L	L	52H	X 0001	00H
Read Device ID	5V	H	L	H	H	L	L	L	L	L	06H	X 0010	00H

Notes:
1. Each $\overline{PROG}$ pulse is 200 ns - 500 ns for Chip Erase.
2. Each $\overline{PROG}$ pulse is 200 ns - 500 ns for Write Code Data.
3. Each $\overline{PROG}$ pulse is 200 ns - 500 ns for Write Lock Bits.
4. RDY/$\overline{BSY}$ signal is output on P3.0 during programming.
5. X = don't care.

Figure 13. Programming the Flash Memory (Parallel Mode)

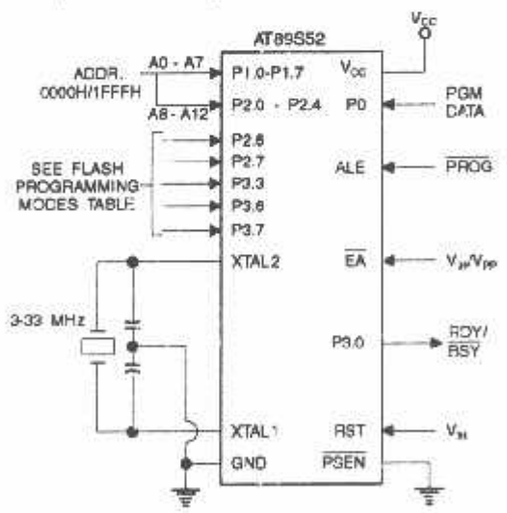
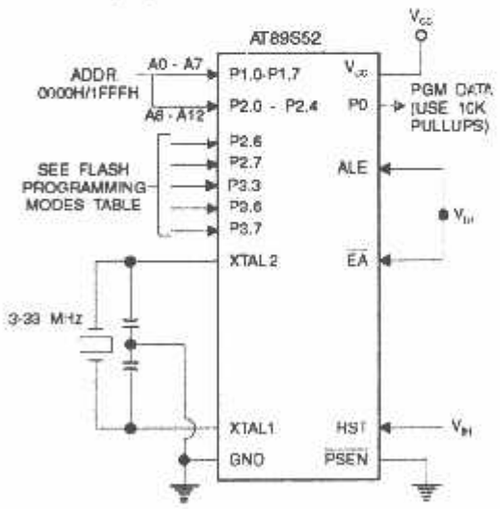


Figure 14. Verifying the Flash Memory (Parallel Mode)



Flash Programming and Verification Characteristics (Parallel Mode)

T_A = 20°C to 30°C, V_{CC} = 4.5 to 5.5V

Symbol	Parameter	Min	Max	Units
V_{PP}	Programming Supply Voltage	11.5	12.5	V
I_{PP}	Programming Supply Current		10	mA
I_{CC}	V_{CC} Supply Current		30	mA
$1/t_{CLCL}$	Oscillator Frequency	3	33	MHz
t_{AVGL}	Address Setup to $\overline{PROG}$ Low	$48t_{CLCL}$		
t_{GHAX}	Address Hold After $\overline{PROG}$	$48t_{CLCL}$		
t_{DVGL}	Data Setup to $\overline{PROG}$ Low	$48t_{CLCL}$		
t_{GHDX}	Data Hold After $\overline{PROG}$	$48t_{CLCL}$		
t_{EHSH}	P2.7 ($\overline{ENABLE}$) High to V_{PP}	$48t_{CLCL}$		
t_{SHGL}	V_{PP} Setup to $\overline{PROG}$ Low	10		µs
t_{GHSL}	V_{PP} Hold After $\overline{PROG}$	10		µs
t_{GLGH}	$\overline{PROG}$ Width	0.2	1	µs
t_{AVQV}	Address to Data Valid		$48t_{CLCL}$	
t_{ELQV}	$\overline{ENABLE}$ Low to Data Valid		$48t_{CLCL}$	
t_{EHQZ}	Data Float After $\overline{ENABLE}$	0	$48t_{CLCL}$	
t_{GHBL}	$\overline{PROG}$ High to $\overline{BUSY}$ Low		1.0	µs
t_{WC}	Byte Write Cycle Time		50	µs

Figure 15. Flash Programming and Verification Waveforms – Parallel Mode

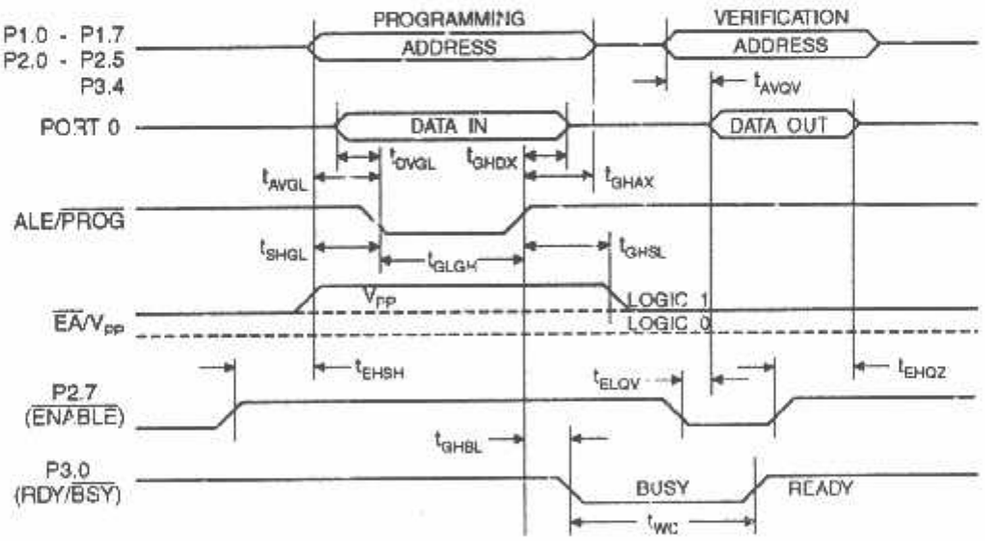
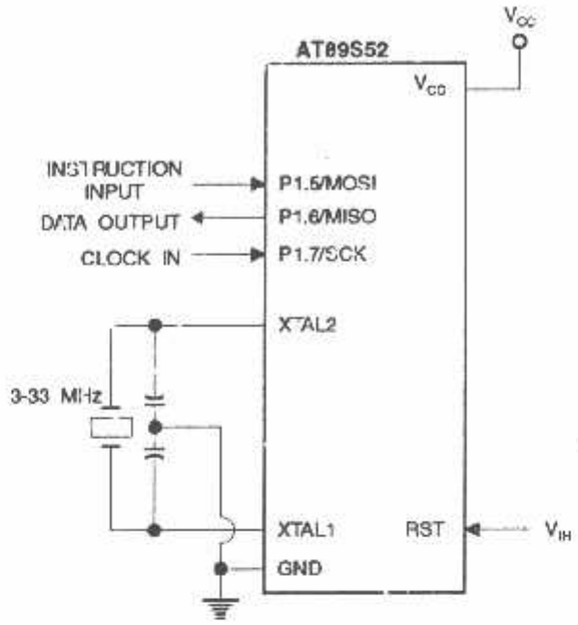


Figure 16. Flash Memory Serial Downloading



Flash Programming and Verification Waveforms – Serial Mode

Figure 17. Serial Programming Waveforms

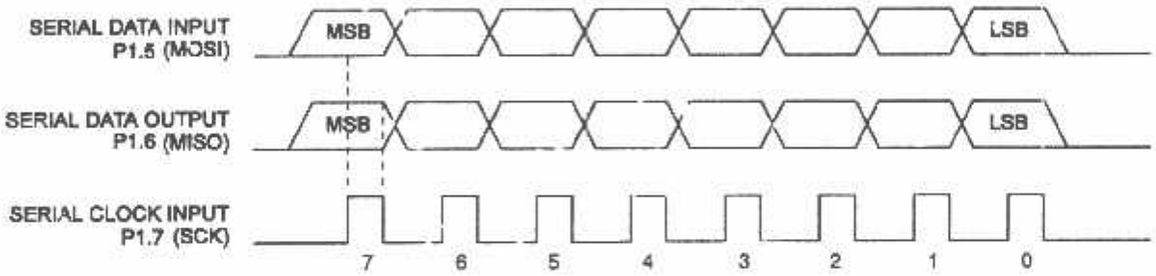


Table 9. Serial Programming Instruction Set

Instruction	Instruction Format Byte 1	Byte 2	Byte 3	Byte 4	Operation
Programming Enable	1010 1100	0101 0011	xxxx xxxx	xxxx xxxx 0110 1001 (Output)	Enable Serial Programming while RST is high
Chip Erase	1010 1100	100x xxxx	xxxx xxxx	xxxx xxxx	Chip Erase Flash memory array
Read Program Memory (Byte Mode)	0010 0000	xxx A12 A11 A10 A9 A8	A7 A6 A5 A4 A3 A2 A1 A0	D7 D6 D5 D4 D3 D2 D1 D0	Read data from Program memory in the byte mode
Write Program Memory (Byte Mode)	0100 0000	xxx A12 A11 A10 A9 A8	A7 A6 A5 A4 A3 A2 A1 A0	D7 D6 D5 D4 D3 D2 D1 D0	Write data to Program memory in the byte mode
Write Lock Bits[2]	1010 1100	1110 00 B1 B2	xxxx xxxx	xxxx xxxx	Write Lock bits. See Note (2).
Read Lock Bits	0010 0100	xxxx xxxx	xxxx xxxx	xx LB3 LB2 LB1 xx	Read back current status of the lock bits (a programmed lock bit reads back as a '1')
Read Signature Bytes[1]	0010 1000	xxx A5 A4 A3 A2 A1 A0	xxx xxxx	Signature Byte	Read Signature Byte
Read Program Memory (Page Mode)	0011 0000	xxx A12 A11 A10 A9 A8	Byte 0	Byte 1... Byte 255	Read data from Program memory in the Page Mode (256 bytes)
Write Program Memory (Page Mode)	0101 0000	xxx A12 A11 A10 A9 A8	Byte 0	Byte 1... Byte 255	Write data to Program memory in the Page Mode (256 bytes)

Notes: 1. The signature bytes are not readable in Lock Bit Modes 3 and 4.

2. B1 = 0, B2 = 0 --> Mode 1, no lock protection
   B1 = 0, B2 = 1 --> Mode 2, lock bit 1 activated
   B1 = 1, B2 = 0 --> Mode 3, lock bit 2 activated
   B1 = 1, B1 = 1 --> Mode 4, lock bit 3 activated

   Each of the lock bits needs to be activated sequentially before Mode 4 can be executed.

After Reset signal is high, SCK should be low for at least 64 system clocks before it goes high to clock in the enable data bytes. No pulsing of Reset signal is necessary. SCK should be no faster than 1/16 of the system clock at XTAL1.

For Page Read/Write, the data always starts from byte 0 to 255. After the command byte and upper address byte are latched, each byte thereafter is treated as data until all 256 bytes are shifted in/out. Then the next instruction will be ready to be decoded.

Serial Programming Characteristics

Figure 18. Serial Programming Timing

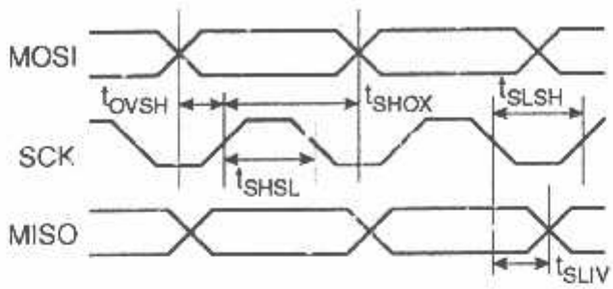


Table 10. Serial Programming Characteristics, T_A = -40°C to 85°C, V_{CC} = 4.0 - 5.5V (Unless otherwise noted)

Symbol	Parameter	Min	Typ	Max	Units
$1/t_{CLCL}$	Oscillator Frequency	0		33	MHz
t_{CLCL}	Oscillator Period	30			ns
t_{SHSL}	SCK Pulse Width High	$2\ t_{CLCL}$			ns
t_{SLSH}	SCK Pulse Width Low	$2\ t_{CLCL}$			ns
t_{OVSH}	MOSI Setup to SCK High	t_{CLCL}			ns
t_{SHOX}	MOSI Hold after SCK High	$2\ t_{CLCL}$			ns
t_{SLIV}	SCK Low to MISO Valid	10	16	32	ns
t_{ERASE}	Chip Erase Instruction Cycle Time			500	ms
t_{SWC}	Serial Byte Write Cycle Time			$64\ t_{CLCL} + 400$	us

Absolute Maximum Ratings*

Operating Temperature	-55°C to +125°C
Storage Temperature	-65°C to +150°C
Voltage on Any Pin with Respect to Ground	-1.0V to +7.0V
Maximum Operating Voltage	6.6V
DC Output Current	15.0 mA

*NOTICE: Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC Characteristics

The values shown in this table are valid for T_A = -40°C to 85°C and V_{CC} = 4.0V to 5.5V, unless otherwise noted.

Symbol	Parameter	Condition	Min	Max	Units
V_{IL}	Input Low Voltage	(Except $\overline{EA}$)	-0.5	0.2 V_{CC}-0.1	V
V_{IL1}	Input Low Voltage ($\overline{EA}$)		-0.5	0.2 V_{CC}-0.3	V
V_{IH}	Input High Voltage	(Except XTAL1, RST)	0.2 V_{CC}+0.9	V_{CC}+0.5	V
V_{IH1}	Input High Voltage	(XTAL1, RST)	0.7 V_{CC}	V_{CC}+0.5	V
V_{OL}	Output Low Voltage[1] (Ports 1,2,3)	I_{OL} = 1.6 mA		0.45	V
V_{OL1}	Output Low Voltage[1] (Port 0, ALE, $\overline{PSEN}$)	I_{OL} = 3.2 mA		0.45	V
V_{OH}	Output High Voltage (Ports 1,2,3, ALE, $\overline{PSEN}$)	I_{OH} = -60 µA, V_{CC} = 5V ± 10%	2.4		V
		I_{OH} = -25 µA	0.75 V_{CC}		V
		I_{OH} = -10 µA	0.9 V_{CC}		V
V_{OH1}	Output High Voltage (Port 0 in External Bus Mode)	I_{OH} = -800 µA, V_{CC} = 5V ± 10%	2.4		V
		I_{OH} = -300 µA	0.75 V_{CC}		V
		I_{OH} = -80 µA	0.9 V_{CC}		V
I_{IL}	Logical 0 Input Current (Ports 1,2,3)	V_{IN} = 0.45V		-50	µA
I_{TL}	Logical 1 to 0 Transition Current (Ports 1,2,3)	V_{IN} = 2V, V_{CC} = 5V ± 10%		-650	µA
I_{LI}	Input Leakage Current (Port 0, $\overline{EA}$)	0.45 < V_{IN} < V_{CC}		±10	µA
RRST	Reset Pulldown Resistor		10	30	KΩ
C_{IO}	Pin Capacitance	Test Freq. = 1 MHz, T_A = 25°C		10	pF
I_{CC}	Power Supply Current	Active Mode, 12 MHz		25	mA
		Idle Mode, 12 MHz		6.5	mA
	Power-down Mode[1]	V_{CC} = 5.5V		50	µA

Notes:
1. Under steady state (non-transient) conditions, I_{OL} must be externally limited as follows:
   Maximum I_{OL} per port pin: 10 mA
   Maximum I_{OL} per 8-bit port:
   Port 0: 26 mA Ports 1, 2, 3: 15 mA
   Maximum total I_{OL} for all output pins: 71 mA
   If I_{OL} exceeds the test condition, V_{OL} may exceed the related specification. Pins are not guaranteed to sink current greater than the listed test conditions.
2. Minimum V_{CC} for Power-down is 2V.

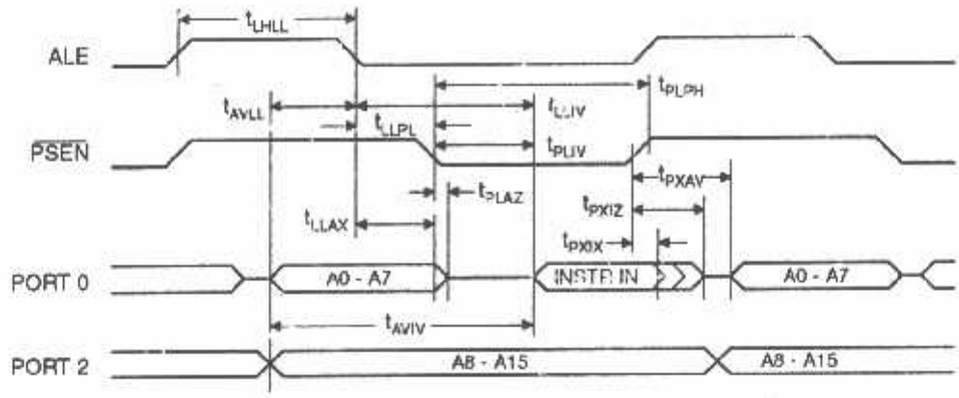
AC Characteristics

Under operating conditions, load capacitance for Port 0, ALE/$\overline{PROG}$, and $\overline{PSEN}$ = 100 pF; load capacitance for all other outputs = 80 pF.

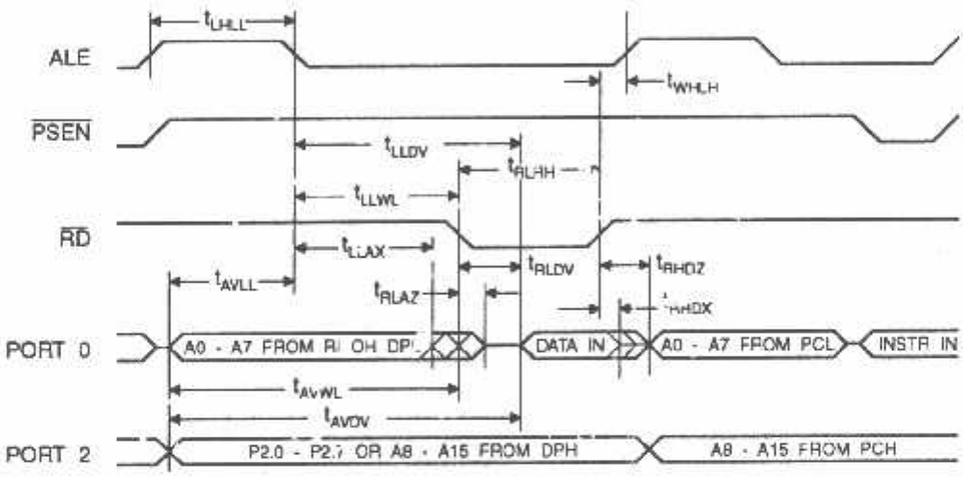
External Program and Data Memory Characteristics

Symbol	Parameter	12 MHz Oscillator		Variable Oscillator		Units
		Min	Max	Min	Max	
$1/t_{CLCL}$	Oscillator Frequency			0	33	MHz
t_{LHLL}	ALE Pulse Width	127		$2t_{CLCL}$-40		ns
t_{AVLL}	Address Valid to ALE Low	43		t_{CLCL}-25		ns
t_{LLAX}	Address Hold After ALE Low	48		t_{CLCL}-25		ns
t_{LLIV}	ALE Low to Valid Instruction In		233		$4t_{CLCL}$-65	ns
t_{LLPL}	ALE Low to $\overline{PSEN}$ Low	43		t_{CLCL}-25		ns
t_{PLPH}	$\overline{PSEN}$ Pulse Width	205		$3t_{CLCL}$-45		ns
t_{PLIV}	$\overline{PSEN}$ Low to Valid Instruction In		145		$3t_{CLCL}$-60	ns
t_{PXIX}	Input Instruction Hold After $\overline{PSEN}$	0		0		ns
t_{PXIZ}	Input Instruction Float After $\overline{PSEN}$		59		t_{CLCL}-25	ns
t_{PXAV}	$\overline{PSEN}$ to Address Valid	75		t_{CLCL}-8		ns
t_{AVIV}	Address to Valid Instruction In		312		$5t_{CLCL}$-80	ns
t_{PLAZ}	$\overline{PSEN}$ Low to Address Float		10		10	ns
t_{RLRH}	$\overline{RD}$ Pulse Width	400		$6t_{CLCL}$-100		ns
t_{WLWH}	$\overline{WR}$ Pulse Width	400		$6t_{CLCL}$-100		ns
t_{RLDV}	$\overline{RD}$ Low to Valid Data In		252		$5t_{CLCL}$-90	ns
t_{RHDX}	Data Hold After $\overline{RD}$	0		0		ns
t_{RHDZ}	Data Float After $\overline{RD}$		97		$2t_{CLCL}$-28	ns
t_{LLDV}	ALE Low to Valid Data In		517		$8t_{CLCL}$-150	ns
t_{AVDV}	Address to Valid Data In		585		$9t_{CLCL}$-165	ns
t_{LLWL}	ALE Low to $\overline{RD}$ or $\overline{WR}$ Low	200	300	$3t_{CLCL}$-50	$3t_{CLCL}$+50	ns
t_{AVWL}	Address to $\overline{RD}$ or $\overline{WR}$ Low	203		$4t_{CLCL}$-75		ns
t_{QVWX}	Data Valid to $\overline{WR}$ Transition	23		t_{CLCL}-30		ns
t_{QVWH}	Data Valid to $\overline{WR}$ High	433		$7t_{CLCL}$-130		ns
t_{WHQX}	Data Hold After $\overline{WR}$	33		t_{CLCL}-25		ns
t_{RLAZ}	$\overline{RD}$ Low to Address Float		0		0	ns
t_{WHLH}	$\overline{RD}$ or $\overline{WR}$ High to ALE High	43	123	t_{CLCL}-25	t_{CLCL}+25	ns

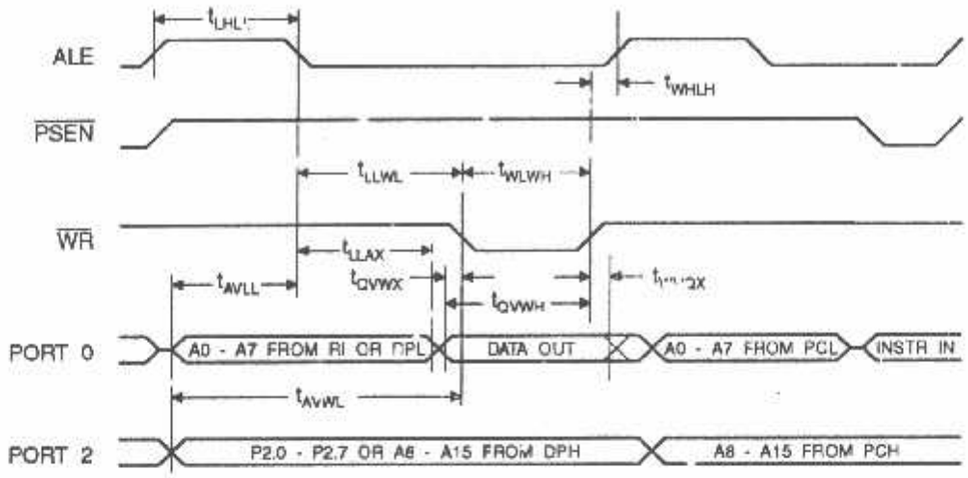
External Program Memory Read Cycle



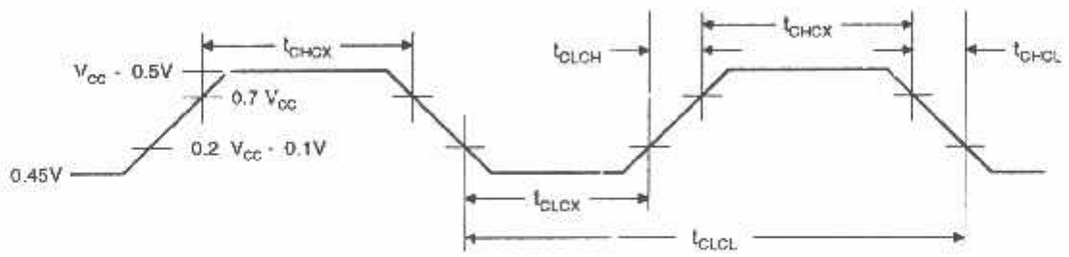
External Data Memory Read Cycle



External Data Memory Write Cycle



External Clock Drive Waveforms



External Clock Drive

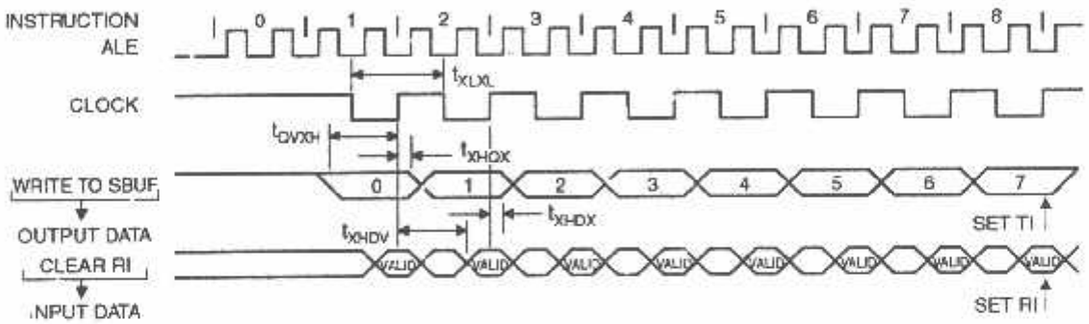
Symbol	Parameter	Min	Max	Units
$1/t_{CLCL}$	Oscillator Frequency	0	33	MHz
t_{CLCL}	Clock Period	30		ns
t_{CHCX}	High Time	12		ns
t_{CLCX}	Low Time	12		ns
t_{CLCH}	Rise Time		5	ns
t_{CHCL}	Fall Time		5	ns

Serial Port Timing: Shift Register Mode Test Conditions

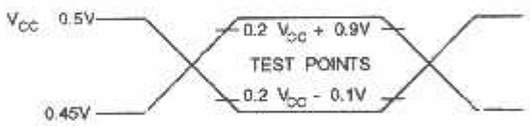
The values in this table are valid for V_{CC} = 4.0V to 5.5V and Load Capacitance = 80 pF.

Symbol	Parameter	12 MHz Osc		Variable Oscillator		Units
		Min	Max	Min	Max	
t_{XLXL}	Serial Port Clock Cycle Time	1.0		$12t_{CLCL}$		µs
t_{QVXH}	Output Data Setup to Clock Rising Edge	700		$10t_{CLCL}$-133		ns
t_{XHQX}	Output Data Hold After Clock Rising Edge	50		$2t_{CLCL}$-80		ns
t_{XHDX}	Input Data Hold After Clock Rising Edge	0		0		ns
t_{XHDV}	Clock Rising Edge to Input Data Valid		700		$10t_{CLCL}$-133	ns

Shift Register Mode Timing Waveforms

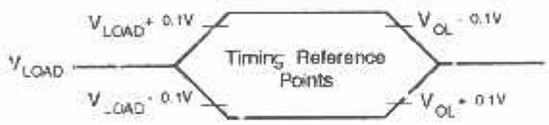


AC Testing Input/Output Waveforms[1]



Note: 1. AC Inputs during testing are driven at V_{CC} - 0.5V for a logic 1 and 0.45V for a logic 0. Timing measurements are made at V_{IH} min. for a logic 1 and V_{IL} max. for a logic 0.

Float Waveforms[1]



Note: 1. For timing purposes, a port pin is no longer floating when a 100 mV change from load voltage occurs. A port pin begins to float when a 100 mV change from the loaded V_{OH}/V_{OL} level occurs.

Ordering Information

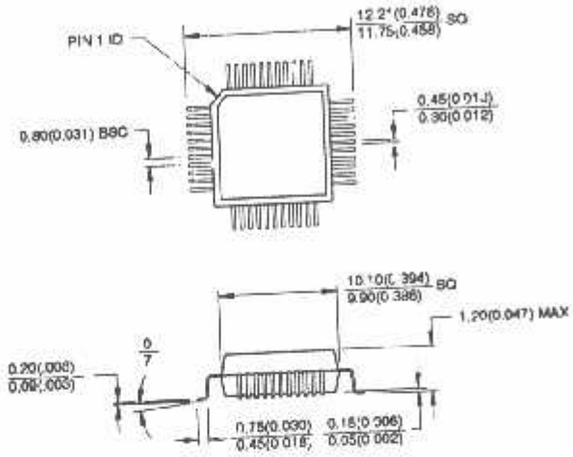
Speed (MHz)	Power Supply	Ordering Code	Package	Operation Range
24	4.0V to 5.5V	AT89S52-24AC AT89S52-24JC AT89S52-24PC	44A 44J 40P6	Commercial (0°C to 70°C)
		AT89S52-24AI AT89S52-24JI AT89S52-24PI	44A 44J 40P6	Industrial (-40°C to 85°C)
33	4.5V to 5.5V	AT89S52-33AC AT89S52-33JC AT89S52-33PC	44A 44J 40P6	Commercial (0°C to 70°C)

= Preliminary Availability

Package Type	
44A	44-lead, Thin Plastic Gull Wing Quad Flatpack (TQFP)
44J	44-lead, Plastic J-leaded Chip Carrier (PLCC)
40P6	40-pin, 0.600" Wide, Plastic Dual Inline Package (PDIP)

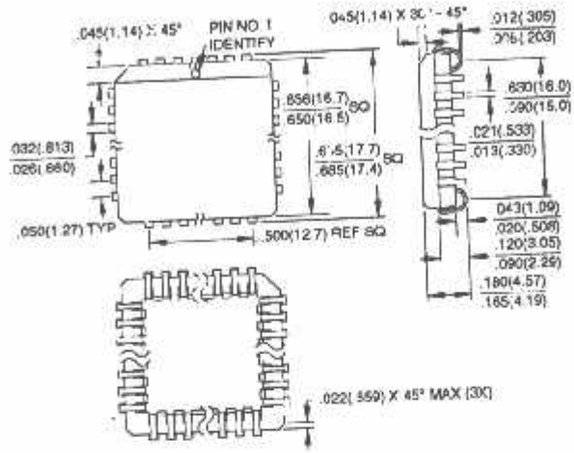
aging Information

A, 44-lead, Thin (1.0 mm) Plastic Gull Wing Quad
at Package (TQFP)
Dimensions in Millimeters and (Inches)*



*Controlling dimension: millimeters

44J, 44-lead, Plastic J-leaded Chip Carrier (PLCC)
Dimensions in Inches and (Millimeters)



40P6, 40-pin, 0.600" Wide, Plastic Dual Inline
Package (PDIP)
Dimensions in Inches and (Millimeters)
JEDEC STANDARD MS-011 AC