INSTITUT TEKNOLOGI NASIONAL MALANG
FAKULTAS TEKNOLOGI INDUSTRI
JURUSAN TEKNIK ELEKTRO S-1
KONSENTRASI TEKNIK ELEKTRONIKA

SKRIPSI

PERENCANAAN DAN PEMBUATAN ALAT PENGHEMAT LISTRIK DALAM PENGOPERASIAN MONITOR PERSONAL COMPUTER (PC) PADA WARTEL BERBASIS MIKROKONTROLER AT89S8252

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MARET 2007

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PERENCANAAN DAN PEMBUATAN ALAT PENGHEMAT LISTRIK DALAM PENGOPERASIAN MONITOR PERSONAL COMPUTER (PC) PADA WARTEL BERBASIS MIKROKONTROLER AT89S8252

SKRIPSI

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ABSTRAKSI

PERANCANGAN DAN PEMBUATAN ALAT PENGHEMAT LISTRIK DALAM PENGOPERASIAN MONITOR PERSONAL COMPUTER (PC) PADA WARTEL BERBASIS MIKROKONTROLLER AT89S8252

(Vico Romandika, 02.17.079, Teknik Elektro S-1/Elektronika)
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Kata Kunci : Penghematan Listrik, LCD, Mikrokontroller, Keypad

Pada skripsi ini dirancang sebuah sistem *Penghematan Listrik Pada Monitor PC Pada wartel,* dimana sistem ini bekerja apabila tidak ada penekanan atau gerakkan dari mouse dan ketboard maka monitor pada PC wartel akan standby. Ketika tidak ada gerakan mouse dan keyboard tersebut sesuai dengan inputan waktu standby yang telah ditentukan melalui keypad yang ditampilkan di LCD.

Pada saat monitor telah standby maka timer pada mikrokontroller akan aktif sesuai dengan lamanya waktu standby monitor, jika pada mouse atau keyboard ditekan atau digerakan maka waktu standby berhenti, kemudian disimpan di EEPROM dan screen pada monitor aktif kembali.

Penghematan listrik disini terjadi ketika monitor pada PC tersebut standby. Alat hanya dikususkan untuk wartel saja. Kelebihan alat ini juga dapat digunkan rental pengetikan untuk memonitoring penghematan listrik pada penggunaan monitor, tapi alat ini hanya dapat mengontrol dua buah monitor saja.

KATA PENGANTAR

Alhamdulillah, puji syukur kehadirat-Mu Ya Allah yang telah memberikan rahmat dan hidayah-Nya, sehingga dapat menyelesaikan skripsi yang berjudul "Perancangan Dan Pembuatan Alat Penghematan Listrik Dalam Pengoperasian Monitor Personal Computer (PC) Pada Wartel Berbasis Mikrokontroller At89S8252" ini dengan lancar. Skripsi ini merupakan persyaratan kelulusan Studi di Jurusan Teknik Elektro S-1 Konsentrasi Teknik Elektronika ITN Malang dan untuk mencapai gelar Sarjana Teknik.

Keberhasilan peyelesaian laporan skripsi ini tidak lepas dari dukungan dan bantuan berbagai pihak. Untuk itu penyusun menyampaikan terima kasih kepada :

1. Bapak Ir. F. Yudi Limpraptono, MT selaku Ketua Jurusan Teknik Elektro S-1.
2. Bapak Ir. Eko Nurcahyo selaku Dosen Pembimbing I, M.Ashar, ST. MT selaku Dosen Pembimbing II, dan Ka. Laboratorium Konversi Energi Listrik.
3. Ayah dan Ibu serta saudara-saudara kami yang telah memberikan do'a restu, dorongan, semangat, dan biaya.
4. Rekan-rekan Instruktur di Laboratorium Konversi Energi Listrik.
5. Semua yang telah membantu dalam penyelesaian penyusunan skripsi ini.

Penyusun telah berusaha semaksimal mungkin dan meyadari sepenuhnya akan keterbatasan pengetahuan dalam menyelasaikan laporan ini. Untuk itu penyusun mengharapkan saran dan kritik yang membangun dari pembaca demi kesempurnaan laporan ini.

Harapan penyusun semoga laporan skripsi ini memberikan manfaat bagi perkembangan ilmu pengetahuan dan pembaca.

Malang, Maret 2007

Penyusun

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KATA PENGANTAR

Alhamdulillah, puji syukur kehadirat-Mu Ya Allah yang telah memberikan rahmat dan hidayah-Nya, sehingga dapat menyelesaikan skripsi yang berjudul "Perancangan Dan Pembuatan Alat Penghematan Listrik Dalam Pengoperasian Monitor Personal Computer (PC) Pada Wartel Berbasis Mikrokontroller At89S8252" ini dengan lancar. Skripsi ini merupakan persyaratan kelulusan Studi di Jurusan Teknik Elektro S-1 Konsentrasi Teknik Elektronika ITN Malang dan untuk mencapai gelar Sarjana Teknik.

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Malang, Maret 2007

Penyusun

BAB I

PENDAHULUAN

1.1. Latar Belakang

Personal Computer (PC) sudah tidak asing lagi sekarang karena PC sudah begitu memegang peranan penting dalam menyelesaikan permasalahan yang dihadapi manusia. Hal ini disebabkan komputer memiliki kelebihan-kelebihan yang dapat membantu seperti daya ingat dan kecepatan dalam menyelesaikan suatu pekerjaan dalam jumlah besar. Dengan menggunakan komputer penyelesaian suatu persoalan berjalan dengan waktu yang relatif singkat serta data yang sewaktu-waktu diperlukan dapat diambil dalam media penyimpan seperti disket, harddisk, compact disk, atau media pernyimpan data lainnya.

Kadang kala kita sering meninggalkan *Personal Computer* tersebut begitu saja dalam keadaan "on" karena sesuatu hal yang penting dan mendesak dan besifat sementara. Hal ini menyebabkan pemborosan pemakaian daya listrik karena *Personal Computer* tetap on tanpa kita menggunakannya. Keborosan daya listrik pada monitor kususnya pada Personal Komputer pada wartel sehingga mengakibatkan biaya operasional komputer itu tinggi, sehingga perlu untuk mematikanmonitor *Personal Computer* apabila kita akan meninggalkan komputer tersebut walaupun dalam waktu yang relatif singkat. Sebenarnya fasilitas pengurang daya listrik pada monitor komputer telah ada pada sebuah system windows *Personal Computer* , jika komputer didiamkan beberapa menit maka layer monitor akan mati sendiri dan apabila keyboard ditekan atau mouse digeser maka monitor akan menyala kembali yaitu monitor dalam keadan standby. Untuk mematikan screen monitor pada *Personal Computer* wartel monitor tidak dapat dilakukan, karena system yang digunakan pada wartel dalam bentuk versi dos, jadi screen monitor tidak dapat dimatikan . Dimana sebuah alat dapat mematikan screen monitor pada *Personal Computer* wartel yang dapat diaktifkan kembali hanya dengan menyentuh mouse atau keyboard. Dengan penambahan rangkaian ini, maka screen monitor komputer mati (standby), jika komputer didiamkan beberapa menit sesuai dengan waktu yang telah diset pada alat, sehingga pemborosan daya listrik dapat dihindarkan dan pemakaian monitor PC dapat kita ketahui, sehinggakita akan menghemat rupiah untuk pembayaran rekening listriknya.

1.2. Rumusan Masalah

Untuk memecahkan permasalahan yang ada , maka rumusan masalah pada laporan TA ini dititik beratkan pada :

- Bagaimana mengontrol Monitor pada PC supaya standby
- Bagaimana mengetahui lamanya waktu stanby monitor
- Bagaimana membuat dan merencanakan perangkat lunak maupun perangkat keras yang dapat mengendalikan sistem.

1.3. Batasan Masalah

Dalam tugas akhir ini agar dicapai sasaran pembahasan yang tepat atau sesuai dengan judul tugas akhir ini serta mecegah meluasnya masalah yang dapat timbul maka diberikan batasan-batasan yang meliputi:

1. Pembahasan hanya pada bagian alat yaitu Pengkondisi Sinyal, Rangkaian pengontrol, dan mikrokontroller.
2. Alat hanya dikususkan pada PC WARTEL yang berbasis Dos
3. Pengontrolan hanaya pada 2 buah monitor

1.4. Tujuan

Tujuan utama penyusunan tugas akhir ini adalah untuk membuat suatu alat yang digunakan untuk mengontrol penghematan penggunaan listrik pada monitor Personal Computer kususnya untuk wartel.

1.5. Metodologi Perencanaan

Adapun langkah-langkah yang diambil untuk menyelesaikan perubahan teoritis pada pembuatan dan perancangan alat penghematan listrik dalam pengoperasian monitor PC pada wartel berbasis mikrokontroller AT89S8252 :

1. Studi literatur tentang teori yang berhubungan dengan judul diatas.
2. Setelah melakukan pengumpulan literatur, maka dilakukan perencanaan perangkat keras dan perangkat lunaknya.
3. Pengujian terhadap peralatan serta pengukuran data hasil pemantauan peralatan.
4. Penyusunan laporan Tugas Akhir.

1.6. Metodologi Pembahasan

Untuk dapat mencapai tujuan yang direncanakan dalam penyelesaian laporan tugas akhir ini, maka metode pembahasan yang diterapkan adalah dengan cara :

1. Mengadakan studi kepustakaan, meliputi buku – buku acuan tentang teori maupun praktek, modul serta data sheet komponen, dan lain-lain.
2. Merencanakan dan membuat alat.
3. Pengujian alat.

1.7.Sistematika Penulisan

Guna mempermudah pembuatan tugas akhir ini, pembahasan tugas akhir ini dibagi beberapa bab. Sedangkan uraian-uraian isi tulisan secara garis besar diantaranya:

Bab I Pendahuluan

Bab ini meliputi latar belakang, alasan pemilihan judul, tujuan penulisan, batasan masalah, metodologi pembahasan, sistematika penulisan.

Bab II Landasan Teori

Membahas teori dasar yang secara umum dibutuhkan untuk menunjang pembuatan alat.

Bab III Perancangan dan Pembuatan Alat

Disini penulis membahas dan menguraikan rangkaian serta perhitungan dari alat tersebut.

Bab IV Pengujian Alat dan Analisa

Membahas tentang proses kerja alat serta membandingkan data hasil pengujian dan pengukuran dengan data pada perencanaan

Bab V Penutup

Berisi tentang kesimpulan dan saran-saran serta daftar referensi dari tugas akhir.

BAB II

LANDASAN TEORI

2.1. Keyboard

Keyboard merupakan piranti masukan yang paling efektif dan digolongkan sebagi sarana pelengkap komputer seperti halnya disk drive, monitor, dan lainya.. Hubungan keyboard dengan komputer dilakukan melalui sarana input output (I/O port). Seperti halnya komputer, keyboard juga bisa bekerja berdasarkan interrupt yang terdiri dari interrupt BIOS dan interrupt DOS. Selain interrupt ada juga buffer yang disebut keyboard buffer, terletak pada daerah BIOS. Data area interrupt sepanjang 32 Byte, mulai alamat 40 : 001EH. Buffer berfungsi menampung semua karakter dari hasil penekanan keyboard sebelum diproses oleh komputer. Dimana keybord buffer dirancang sebagai *circular buffer*, artinya jika buffer telah terisi sampai batas akhir, selanjutnya pengisian akan memutar kembali (*Wrap*) kebatas awal. Setiap penekanan tombol yang tersimpan dibuffer membutuhkan tempat sebesar 2 Byte. Byte pertama untuk kode ASCII dan byte kedua untuk kode scan. Semua tombol diklasifikasikan sebagai salah satu dari dua tahapan yaitu *make* dan *break*. saat tombol ditekan mikroprosesor keyboard mendifinisikan sebagai break yang dikirimkan kekomputer.

Operasi-operasi dasar pada keyboard ditunjang oleh mikroprosesor tersendiri didalamnya (Intel 8048 untuk PC/XT, Intel 8042 untuk PC/AT, dan Intel 8049 untuk kedua type komputer IBM/ kompatibel).

Analisis kesalahan internal (dilakukan pada saat komputer dinyalakan),mendeteksi penekanan tombol dan pelepasan tombol, serta sebagai buffer dari keyboard dengan kemampuan 20 karakter yang pada kondisi normal buffer ini kosong. Buffer keyboard yang lain berada pada ROM BIOS sebesar 16 karakter.

Data dari keyboard terdiri dari 11 bit word yang dikirim secara asinkron melalui serial data port. Secara teknis komunikasi antar keyboard dengan komputer dilakukan melalui sepasang sinyal yaitu *clock line* dan *data line*. Ketika terdeteksi penekanan tombol keyboard, mikroprosesor akan memeriksa status clock line, jika setatusnya rendah (0) maka karakter tersebut akan disimpan dibuffer. Sebaliknya jika terdeteksi status clock line tinggi (1) maka keyboard akan memeriksa status data line. Bila status data tinggi maka berarti komputer siap menerima data dari keyboard dan keyboard akan mengirimkan data serial yang dimulai dari start bit (0) diikuti dengan 8 buah data bit, sebuah parity bit dan sebuah stop(1).

2.2. Mouse

Mouse dengan connector PS/2 yang dihubungkan ke komputer motherboard yang menggunakan jenis yang sama yaitu 6 pin connector [sebagai/ketika] PS/2 papan tombol. Data yang dikirim oleh mouse secara syncronous melalui port serial yang serupa dengan pengiriman data pada keyboard. Mouse dengan connector PS/2 sudah tersedia di setiap motherboard computer baik computer yang baru atau computer yang lama, karena mouse dengan connector sudah merupakan standart pada setiap motherboard.

Dimana mouse diatur dengan dua transmisi yaitu control Clock dan Data. Yang keduanya dikontrol dengan mouse tersebut dimana Clock berlogika low dan Data berlogika low atau high.

2.3 Mikrokontroller AT89S8252

Mikrokontroller AT89S8252 merupakan pengembangan dari mikrokontroller standard MCS-51. yang mana mikrokontroller AT89S8252 memiliki beberapa kelebihan dibandingkan dari mikrokontroller MCS-51.

Fitur dari mikrokontroller AT89S8252 sebagai berikut :

a. 8K *byte Downloadable flash memori*

b. 2K byte EEPROM

c. 3 level program *memori lock*

d. 256 *byte RAM internal*

e. 32 I/O yang dapat dipakai semua

f. 3 buah *timer/counter* 16 bit

g. Programmable UART (serial port)

h. SPI serial Interface

i. Programmable Watchdog Timer

j. Dual Data *Pointer*

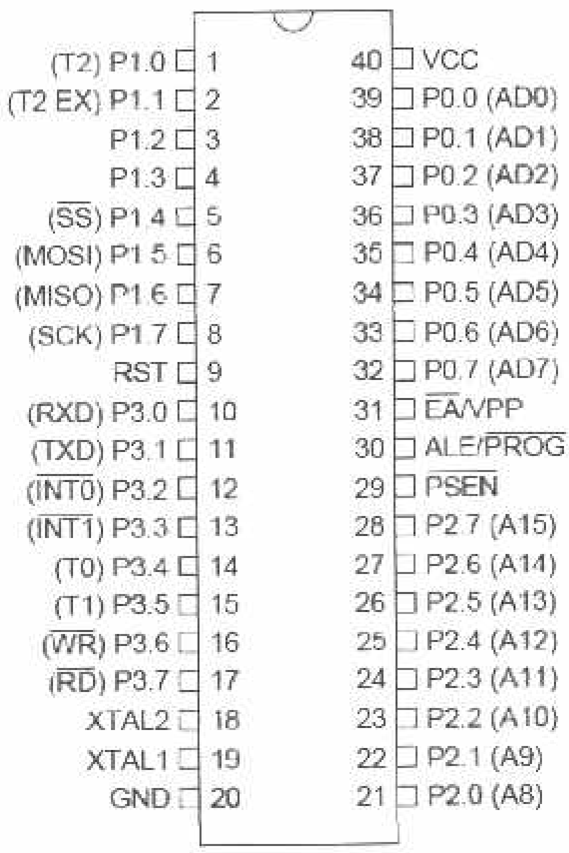
k. Frekuensi kerja 0 sampai 24 MHz

l. Tegangan operasi 2.7 Volt samapai 6 Volt

Terlihat bahwa mikrokontroller AT89S8252 memiliki banyak fitur yang menguntungkan. Dipakainya *downloadable flash* memori memungkinkan mikrokontroller ini bekerja sendiri tanpa diperlukan tambahan chip lainnya. Sementara flash memorinya mampu diprogram hingga seribu kali.

Hal lain yang menguntungkan adalah system peemrograman menjadi lebih sederhana dan tidak memerlukan rangkaian yang rumit seperti rangkaian MCS-51.

Timer/counter bertambah dari standar 2 buah pada MCS-51 menjadi 3 buah pada mikrokontroller ini. Selain itu frekuensi kerja yang lebar dan rancangan static sangat membantu untuk proses debugging. Dengan adanya beberapa fitur tambahan ini, maka akan mengakibatkan bertambahnya *SFR* (*Special Function Register*).



Gambar 2.1. Mikrokontroller AT89S8252
Sumber: At 89S8252 Data Sheet (http://www.atmel.com)

Mikrokontroller AT89S8252 memiliki 40 buah pin yang umumnya kemasan mikrokontroller ini adalah *DIP(Dual In Line Packaged)*, namun ada juga yang kemasannya PLCC dengan 44 buah pin.

Masing-masing dari mikrokontroller ini memiliki kegunaan sebagai berikut :

a. Port 1

Port 1 merupakan I/O dua arah *(bi-directional)* yang telah dilengkapi dengan pull-up internal. Port ini dapat menerima 4 masukan *TTL(Transistor-Transistor Logic)*. Pada port terdapat beberapa fungsi khusus yaitu :

Tabel 2.1. Pin 1

Port Pin	Fungsi Khusus
P1.0	T2 (masukkan luar untuk *timer/counter* 2)
P1.1	*T2EX(Timer/counter 2 capture/reload tringger* dan control arah.
P1.2	-
P1.3	-
P1.4	*SS (Slave port select input)*
P1.5	MOSI(*Master* data *output*, *Slave* data input kanal SPI
P1.6	MISO(*Master* data *input*, *Slave* data *output* kanal SPI
P1.7	SCK(*Master clock output*, *Slave clock input* kanal SPI

Sumber: At 89S8252 Data Sheet (http://www.atmel.com)

b. *RESET* (RST)

Masukkan untuk Reset. Suatu logika tinggi selama dua siklus pada pin *reset* akan menyebabkan terjadinya proses *reset*.

c. Port 3

Port 3 merupakan port 8 bit dua arah dengan *pull up internal*. Selain sebagai *port parallel* biasa, port 3 juga memiliki fungsi khusus sebagai berikut ini :

Tabel 2.2. Port 3

Port	Fungsi Khusus
3.0	RXD(masukan port serial UART)
P3.1	TXD(keluaran port serial UART)
P3.2	INT0(masukan interupsi luar 0)
P3.3	INT1(masukan interupsi luar 1)
P3.4	T0(masukan luar timer/counter 0)
P3.5	T1(masukan luar timer/counter 1)
P3.6	WR(pulsa penulisan data memori luar)
P3.7	RD(pulsa pembacaan data memori luar)

Sumber: At 89S8252 Data Sheet (http://www.atmel.com)

d. XTAL1

Masukan untuk penguat *inverting osilator* dan masukan rangkaian *clock internal*.

e. XTAL2

Keluaran dari penguat *inverting osilator*.

f. GND

Ground system

g. Port 2

Port 2 merupakan port parallel 8 bit yang bersifat dua arah dan memiliki *pull up internal.port* 2 mengirimkan byte tinggi dari alamat selama pengaksesan dari program memori luar dan selama penulisan ke data memori luar yang menggunakan alamat 16 bit.

h. PSEN

Program Store Enable adalah pulsa pengaktif untuk membaca program memori luar. Saat mikrokontroller melaksanakan instruksi dari program memori luar, PSEN akan diaktifkan dua kali tiap siklus mesin, kecuali pada saat mengakses data memori luar.

i. ALE

Address Latch Enable merupakan suatu pulsa keluaran untuk mengaitkan (*latch*) byte bawah dari alamat selama mengakses memori luar.

j. EA

External Access Enable. EA harus dihubungkan dengan *ground* jika ingin mengakses dari program memori luar dengan alamat 0000H sampai FFFFH. EA harus dihubungkan dengan VCC jika menggunakan progtam memori *internal*.

k. Port 0

Port 0 merupakan port 8 bit yang bersifat *open drain* dua arah. Sebagai keluaran, tiap pin dapat menerima 8 masukkan TTL. Saat logika 1 dituliskan pada port, pin port dapat digunakan sebagai masukkan dengan impedansi tinggi.

l. VCC

Dihubungkan dengan tegangan kerja +5 Volt.

2.3.1. SFR Pada AT89S8252

SFR(*Special Function Register*) pada AT89S8252 memiliki tambahan dari SFR MCS-51 yang gunanya untuk mengontrol alat tambahan pada mikrokontroller.

SFR tambahan ini meliputi : T2CON(Timer 2 *register* dengan alamat 0C8H), T2MOD(Timer 2 Mode dengan alamat 0C9H), WMCON(*Watchdog and Memory Control Register* dengan alamat 96H), SPCR(SPI Control Register dengan alamat D5H), SPSR(SPI Status *Register* dengan alamat AAH), SPDR(SPI Data *Register* dengan alamat 86H). Gambar berikut akan menjelaskan letak masing-masing SFR

0F8H									0FFH
0F0H	B 00000000								0F7H
0E8H									0EFH
0E0H	ACC 00000000								0E7H
0D8H									0DFH
0D0H	PSW 00000000					SPCR 000001XX			0D7H
0C8H	T2CON 00000000	T2MOD XXXXXX00	RCAP2L 00000000	RCAP2H 00000000	TL2 00000000	TH2 00000000			0CFH
0C0H									0C7H
0B8H	IP XX000000								0BFH
0B0H	P3 11111111								0B7H
0A8H	IE 0X000000		SPSR 00XXXXXX						0AFH
0A0H	P2 11111111								0A7H
98H	SCON 00000000	SBUF XXXXXXXX							9FH
90H	P1 11111111						WMCON 00000010		97H
88H	TCON 00000000	TMOD 00000000	TL0 00000000	TL1 00000000	TH0 00000000	TH1 00000000			8FH
80H	P0 11111111	SP 00000111	DP0L 00000000	DP0H 00000000	DP1L 00000000	DP1H 00000000	SPDR XXXXXXXX	PCON 0XXX0000	87H

Gambar 2.2. Letak SFR Pada Mikrokontroller AT89S8252

Sumber: AT 89S8252 Data Sheet (http://www.atmel.com)

2.3.2. SFR Untuk Timer 2

Pada *timer/counter* 2 ini dikendalikan oleh *special function register* yang bernama T2CON(Timer 2Control), T2MOD(Timer 2 Mode) dan sepasang *register* RCAP2H. RCAP2L merupakan *register capture/reload* untuk timer 2 dalam 16 bit *capture mode* atau *auto reload mode*.

Register R2CON yang beralamat di 0C8H memiliki bit-bit sebagai berikut:

Tabel 2.3. Register Pada Mikrokontroler

MSB							LSB
TF2	EXF2	RCLK	TCLK	EXEN2	TR2	C/T2	CP/RL2

Sumber: AT 89S8252 Data Sheet (http://www.atmel.com)

Tebel 2.4. Fungsi SFR Pada Mikrokontroler

Bit	Keterangan
TF2	Bendera overflow timer 2, diset oleh timer 2 dan harus diclear lewat software. TF2 tidak akan diset jika RCLK = 1 atau TCLK = 1.
EXF2	Bendera luar timer 2 diset saat suatu *capture* atau *reload* disebabkan oleh transisi negative pada T2EX dan EXEN2 = 1. jika sela timer 2 diaktifkan, EXF2 = 1 akan menyebabkan CPU mencabang ke rutin sela timer 2. EXF2 harus diclear dengan software. EXF2 tidak menyebabkan sela pada *mode up/down counter* (DCEN = 1).
RCLK	*Receive clock enable*. Jika diset menyebabkan serial port menggunakan pulsa overflow tmer 2 sebagai detak penerimaan pada serial port untuk mode 1 dan 3. Jika RCLK = 0 menyebabkan pulsa *overflow* timer 1 yang digunakan sebagai detak.
TCLK	*Transmit Clock enable*. Jika diset menyebabkan serial port menggunakan pulsa *overflow timer* 2 sebagai detak pengiriman. Jika TCLK = 0 menyebabkan pulsa *overflow timer* 1 yang digunakan sebagai detak pengiriman.
EXEN2	*Timer 2 eksternal enable*. Jika diset memungkinkan *capture atau reload* terjadi sebagai hasil dari transisi negative pada pin T2EX jika timer 2 sedang tidak digunakan sebagai *baud rate generator* untuk serial port. Jika EXEN2 = 0 menyebabkan timer 2 akan melakukan apa-apa kejadian pada pin T2EX.
TR2	Bit untuk mengatur *start/stop* untuk timer 2, jika TR2 = 1 *timer* akan aktif.
C/T2	Bit pemilih *timer* atau *counter* untuk timer 2. Jika C/T2 = 0 maka terpilih fungsi timer. C/T2 = 1 untuk fungsi *counter*.
CP/RL2	Pemilihan *Capture/Reload*. Jika diset maka proses *capture* akan terjadi pada transisi negative pada pin T2EX jika EXEN = 1. jika bit ini *diclear* maka proses *reload* otomatis akan terjadi saat timer 2 overflow atau transisi negative terjadi pada pin T2EX saat bit EXEN2 = 1. jika bit RCLK atau TCLK diset maka bit ini menjadi tidak diperhitungkan(ignore). Hal ini karena timer 2 dipakai sebagai *baut rate* generator pada serial port.

Sumber: At 89S8252 Data Sheet (http://www.atmel.com)

SFR ini memiliki nilai pada saat reset : 0000 0000B

Timer 2 juga memiliki SFR yang bernama T2MOD(*Timer 2 Mode Control Register*) yang beralamat di 0C9H dan memiliki nilai pada saat reset xxxx xx00B. bit-bit pada T2MOD adalah sebagai berikut :

Tabel 2.5. Komposisi Data

MSB							LSB
-	-	-	-	-	-	T2OE	DCEN

Bit	Keterangan
T2OE	*Timer 2 Output Enable bit*
DCEN	Jika diset memungkinkan *timer/counter* sebagai *up/down counter*

Sumber: At 89S8252 Data Sheet (http://www.atmel.com)

2.3.3. SFR untuk Watchdog dan Memori

Untuk menggunakan *watchdog timer* atau memori, maka dapat dilakukan dengan mengatur SFR yang bernama *WMCON* dengan alamat 96H. Bit-bit pada SFR ini dapat dijelaskan sebagai berikut :

Nilai SFR ini pada saat reset adalah 0000 0000B.

Tabel 2.6. Pemetaan Memori

MSB							LSB
PS2	PS1	PS0	EEMWE	EEMEN	DPS	WDTTRST	WDTEN

Bit	Keterangan
PS2 PS1 PS0	Ketiga bit ini merupakan bit *prescaler* untuk *watchdog timer*. Jika ketiga bit diclear maka periode watchdog timer adalah 16 ms. Jika ketiga bit diatas diset maka nominal periode waktu *watchdog timer* adalah 2048 *ms*.
EEMWE	Bit pengaktif penulisan EEPROM data memori. Bit ini harus diset sebelum penulisan ke EEPROM dengan instruksi *movx*. Setelah selesai penulisan maka bit ini harus diclear.
EEMEN	Bit pengaktif pengaksesan internal EEPROM. Saat EEMEN = 1 intruksi movx dengan DPTR akan mengakses internal EEPROM bukan pada data memori luar. Jika EEMEN = 0 instruksi movx dengan DPTR akan mengakses data memori luar.
DPS	*Data Pointer Register Select*. Jika bit ini diclear akan memilih bank pertama dari data *pointer register*(DP0). Jika bit ini diset akan terpilih *bank* kedua (DP1).
WDTRST	*Watchdog timer reset* dan bit bendera EEPROM *ready/busy*. Tiap saat bit ini diset

	ke 1 oleh *software* pengguna, suatu pulsa akan dihasilkan untuk *mereset watchdog timer*. Bit ini kemudian secara otomatis akan diclear. Bit ini bersifat hanya untuk ditulisi. Bit ini juga sebagi bit bendera *ready/busy* pada *mode read only* selama penulisan EEPROM. RDY/BSY = 1 berarti bahwa EEPROM siap untuk diprogram. Selama operasi pemrograman berlangsung, bit ini akan berlogika '0' dan secara otomatis akan direset ke '1' saat pemrograman selesai.
WDTEN	Bit pengaktif *watchdog timer*. Jika WDTEN = 1 akan mengaktifkan *watchdog timer*, jika WDTEN = 0 akan melumpuhkannya.

Sumber: At 89S8252 Data Sheet (http://www.atmel.com)

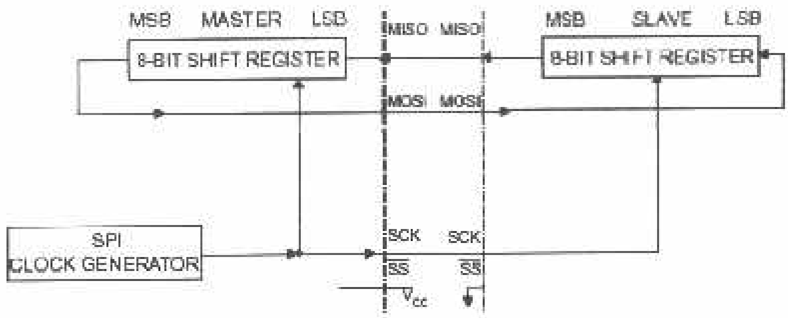
2.3.4. SFR Pengontrol SPI

Berbeda dengan MCS-51, mikrokontroller AT89S8252 memiliki fasilitas SPI(*Serial Peripheral Interface*). Fasilitas ini memungkinkan transferdata kecepatan tinggi secara sinkron antara mikrokontroller AT89S8252 dengan *peripheral* atau anta mikrokontroller AT89S8252.

Fitur SPI pada AT89S8252 meliputi :

a. *Full duplek*, 3 kawat dengan transfer data secara *sinkron*.
b. Operasi *Master atau Slave*.
c. *Frekuensi maksimum* 6 MHz.
d. Sistem data *transfer MSB* dahulu atau *LSB*.
e. 4 *bit rate* terprogram.
f. Bendera sela pada akhir transmisi.
g. *Write Collision Flag Protection*.
h. Bangun dari *mode idle* (hanya untuk *mode slave*).

Gambar berikut menunjukkan hubungan antara CPU *master dan slave.*



Gambar 2.3. Koneksi SPI Master dan Slave
Sumber: At 89S8252 Data Sheet (http://www.atmel.com)

Pin SCK adalah keluaran detak pada *mode master*, tetapi merupakan detak masukkan pada *mode slave*. Menulis ke SPI data register pada CPU master akan memulai SPI *clock generator*, dan data yang ditulis digeser keluar pada pin MOSI dan menuju pin *MOSI* pada *CPU slave*.

Setelah menggeser 1 *byte*, *SPI clock generator* akan berhenti, dan akan mengaktifkan bendera(*flag*) selesai pengiriman(*SPIF*). Jika kedua bit pengaktif sela SPI dan bit pengaktif *serial port* (ES) diset, suatu sela akan dibutuhkan.

Bit pemilih *slave select*(SS) pada port 1 pin 4(P1.4) dibuat rendah untuk memilih suatu alat *SPI individual* sebagai *slave*. Jika pin ini tinggi, maka port SPI tidak diaktifkan dan pin *MOSI*(P1.6) dapat digunakan sebagai masukkan.

Sedangkan *special function register* untuk mengontrol penggunaan SPI adalah *SPCR(SPI Control Register)* dengan alamat D5H dan SPSR(*SPI Status Register*) dengan alamat AAH.

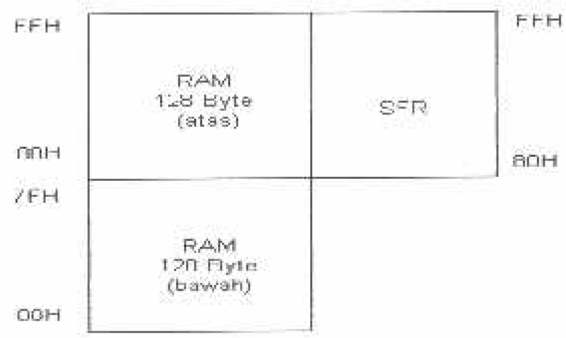
2.3.5. Data Memori (EEPROM) dan RAM

Mikrokontroller AT89S8252 dilengkapi dengan data memori yang berupa *EEPROM(Electrically Erasable Programmable Read Only Memory)*. *EEPROM* yang ditanamkan ini sebesar 2 K byte dan dapat dipakai untuk menyimpan data.

EEPROM on-chip ini diakses dengan mengeset bit *EEMEN* pada register *WMCON* pada alamat 96H. Alamat *EEPROM* ini adalah 000H sampai 7FFH. Instruksi movx digunakan untuk mengakses *EEPROM internal* ini. Namun jika ingin mengakses data memori luar dengan menggunakan *instruksi movx* ini maka bit *EEMEN* harus dibuat '0'.

Bit *EEMWE* pada register *WMCON* harus diset ke 1 sebelum sembarang lokasi pada *EEPROM* dapat ditulisi. Program pengguna harus mereset bit *EEMWE* ke '0' jika proses penulisan ke *EEPROM* tidak diperlukan lagi. Proses penulisan ke *EEPROM* dapat dilihat dengan membaca bit RDY/BSY pada *SFR WMCON*. Jika bit ini berlogika rendah maka berarti penulisan *EEPROM* sedang berlangsung, jika bit ini berlogika tinggi berarti penulisan sudah selesai dan penulisan lain dapat dimulai lagi.

Sedangkan RAM yang ada pada mikrokontroller AT89S8252 ini berkapasitas 256 byte. *RAM(Random Accses Memory)* merupakan memori yang bersifat sementara dan mudah terhapus isinya jika aliran listrik diputuskan. Karena itu RAM tidak digunakan sebagai penyimpan program tetapi untuk menyimpan data sementara. Peta dari RAM internal pada AT89S8252 adalah sebagai berikut :



Gambar 2.4. Alamat *internal RAM* dan *SFR*
Sumber: At 89S8252 Data Sheet (http://www.atmel.com)

2.3.6. Programmable Watchdog Timer (WDT)

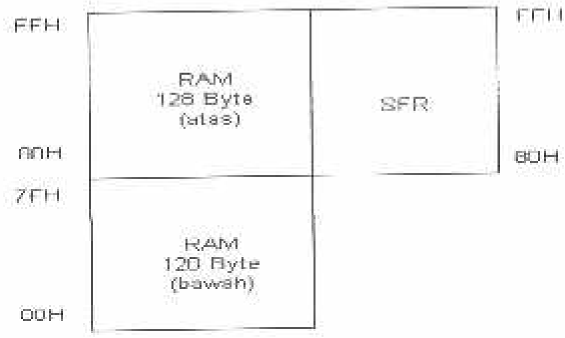
Pada mikrokontroller AT89S8252 dilengkapi dengan *Watchdog timer*. *Watchdog timer* ini menggunakan detak sendiri. Untuk mengatur rentang waktu (*periode*) pada *WDT* ini maka terdapat bit prescaler yang dapat mengatur rentang waktu yang dibutuhkan.

Bit prescaler ini adalah bit PS0, PS1 dan PS2 pada register *WMCON*. Perioda waktu pada WDT ini berkisar dari 16 *ms* sampai 2048 *ms*. Karena bit prescalernya ada tiga, maka akan ada 8 buah kemungkinan seperti yang tertera dibawah ini.

Tabel 2.7. Priode Waktu Pada WDT

PS2	PS1	PS0	Periode
0	0	0	16 mili detik
0	0	1	32 mili detik
0	1	0	64 mili detik
0	1	1	128 mili detik
1	0	0	256 mili detik
1	0	1	512 mili detik
1	1	0	1024 mili detik
1	1	1	2048 mili detik

Sumber- At 89S8252 Data Sheet (http://www.atmel.com)



Gambar 2.4. Alamat *internal RAM* dan *SFR*

Sumber: At 89S8252 Data Sheet (http://www.atmel.com)

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0	0	1	32 mili detik
0	1	0	64 mili detik
0	1	1	128 mili detik
1	0	0	256 mili detik
1	0	1	512 mili detik
1	1	0	1024 mili detik
1	1	1	2048 mili detik

Sumber: At 89S8252 Data Sheet (http://www.atmel.com)

Watchdog timer dilumpuhkan oleh *power on reset* (*POR*) dan selama *power down*. WDT diaktifkan dengan menseting bit *WDTEN* pada *SFR WMCON* (alamat 96H). jika perhitungan waktu WDT telah selesai(*time out*) tanpa ada reset atau dilumpuhkan, maka suatu pulsa *reset internal* akan dihasilkan untuk mereset CPU.

2.3.7. Timer

Pada mikrokontroller ini terdapat tambahan *timer* yaitu *timer* 2. timer yang lainya *timer* 1 dan *timer* 0 penggunaanya sama dengan pada MCS-51.

Hal yang perlu diperhatikan adalah bahwa *timer/counter* dapat digunakan sebagai generator *baud rate* untuk *serial port*. Selain menggunakan *timer* 1 untuk menghasilkan *baud rate* maka bisa digunakan pula timer 2 untuk menghasilkan *baut rate* untuk *serial port*.

Timer 2 ini merupakan *timer/counter* yang berukuran 16 bit yang dapat beroperasi sebagi *timer* atau penghitung kejadian dengan detak dari luar. Untuk mengatur fungsi ini dilakukan dengan mengatur bit C/T2 pada *SFR T2CON*. Terlihat bahwa jika bit tinggi maka akan terpilih fungsi *counter*, tetapi jika bit ini rendah maka akan terpilih fungsi timer 2.

Timer ini memiliki 3 mode operasi yaitu *capture, auto reload(up dan down counting)* dan *baud rate generator*. Untuk memilih mode ini dengan mengatur bit pada *SFR T2CON(Timer 2 Control Register)*.berikut ini *mode* operasi yang dapat dijalankan oleh *timer* 2.

Tabel 2.8. Pewaktuan I.C.AT89S8252

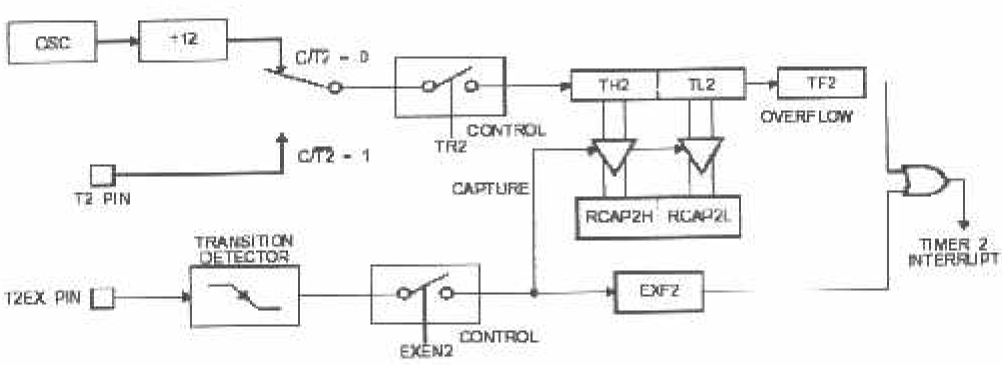
RCLK+TCLK	CP/RL2	TR2	MODE
0	0	1	*16 bit auto reload*
0	1	1	*16 bit capture*
1	X	1	*Baud rate generator*
X	X	0	*Off*

Sumber: At 89S8252 Data Sheet (http://www.atmel.com)

2.3.8. Mode Capture

Pada *mode* ini dua pilihan dipilih oleh bit EXEN2 pada *SFR T2CON*. Jika *EXEN2* = 0, *timer* 2 merupakan 16 bit *timer* atau *counter* yang jika telah *overflow* akan mengeset bit TF2 pada T2CON.

Bit ini kemudian dapat digunakan untuk menghasilkan sela. Jika EXEN2 = 1, timer 2 akan berlaku sama, tetapi suatu transisi tinggi ke rendah(1 to 0) pada pin T2EX(P1.1) akan menyebabkan nilai sekarang pada TH2 dan TL2 untuk ditangkap dan disimpan ke RCAP2H da RCAP2L. sebagai tambahan transisi tinggi ke rendah pada T2EX menyebabkan bit EXF2 pada T2CON diset. Bit EXF2 sama halnya dengan bit TF2 dapat menghasilkan sela.

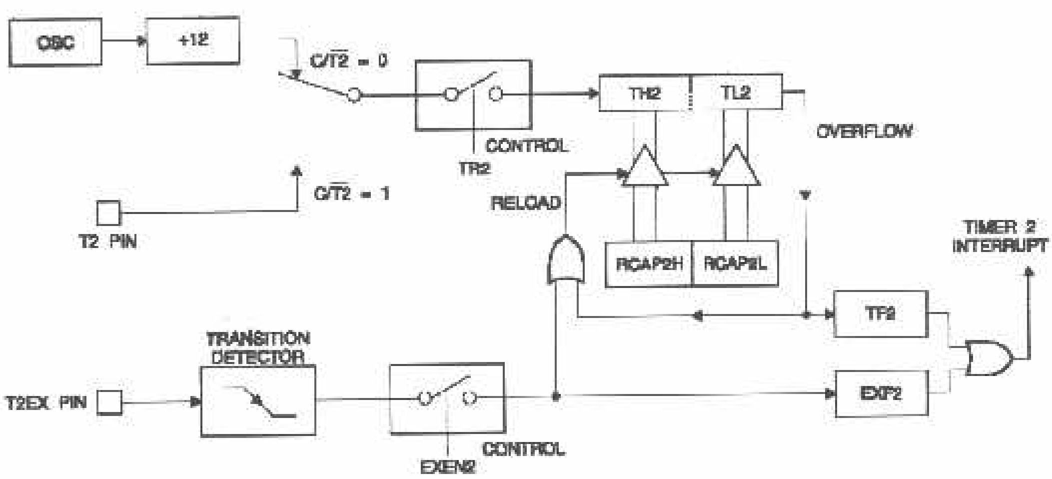


Gambar 2.5. Timer 2 Pada *Mode Capture*
Sumber: At 89S8252 Data Sheet (http://www.atmel.com)

2.3.9. Auto Reload (Up atau Down Counter)

Timer 2 dapat diprogram untuk menghitung naik atau menghitung mundur jika dikonfigurasikan sebagai mode 16 bit *auto reload*. Fitur ini dapat dimatikan dengan mengatur bit DCEN(*Down Counter Enable*) pada SFR T2MOD. Pada saat reset DCEN akan berlogika rendah maka timer 2 akan memiliki default untuk menghitung maju(*up counter*). Jika bit DCEN diset, timer 2 dapat menghitung maju atau mundur tergantung pada nilai logika pada pin T2EX.

Pada gambar berikut timer 2 secara otomatis menghitung naik saat DCEN = 0. pada mode ini, 2 pilihan dipilih oleh bit EXEN2 pada SFR T2CON. Jika EXEN2 = 0, *timer* 2 akan naik menjadi 0FFFFH dan kemudian akan mengeset bit TF2 jika telah *overflow*. *Overflow* juga menyebabkan terjadinya register timer diisi kembali dengan nilai 16 bit dari RCAP2H dan RCAP2L.



Gambar 2.6. Timer 2 Pada Mode Auto Reload DCEN = 0
Sumber: At 89S8252 Data Sheet (http://www.atmel.com)

2.3.10. Baud Rate Generator

Timer 2 dapat dipilih sebagai *baud rate generator* dengan menseting TCLK dan RCLK pada SFR T2CON. *Baud rate* untuk pengiriman dan penerimaan sementara *timer* 1 digunakan untuk tugas lain.

Baud rate generator secara teknis sama *mode auto reload*, dimana pelimpahan TH2 menyebabkan *register timer* 2 diisi kembali dengan 16 bit pada register RCAP2H dan RCAP2L yang telah diisi(*present*) oleh pemakai.

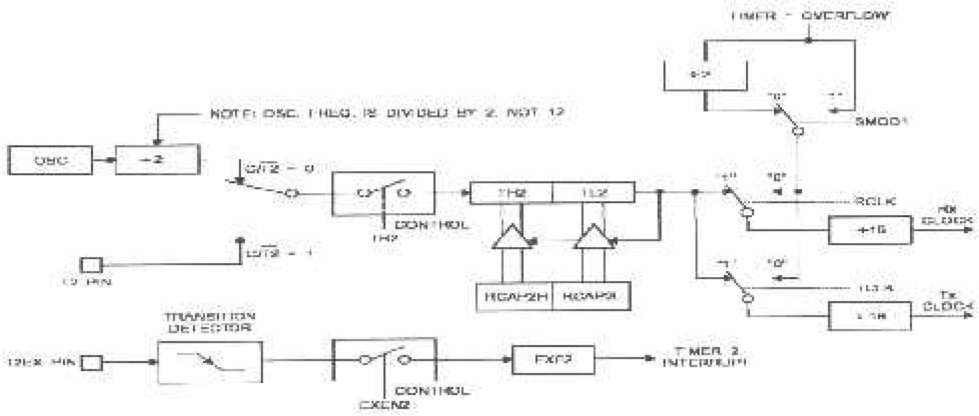
Baud rate pada *mode* 1 dan 3 ditentukan oleh *rate overflow timer* berdasarkan persamaan :

$$\text{Baud rate (mode 1,3)} = \frac{\text{Timer 2 Overflow Rate}}{16}$$

Timer dapat dikonfigurasikan sebagai *operasi* timer atau *counter*. Pada kebanyakan pemakai adalah difungsikan *timer* dimana bit CP/T2 dibuat '0'. Operasi *timer* adalah berbeda jika timer 2 difungsikan sebagai *baud rate generator*. Secara normal sebagai timer, akan naik setiap siklus mesin (pada 1/12 *frekwensi osilator*). Sebagai *baud rate generator* akan dinaikkan tiap state time (pada ½ *frekuensi osilator*). Rumus untuk baud rate adalah sebagai berikut :

$$\text{Baud rate (mode 1,3)} = \frac{\text{Frekuensi Osilator}}{32 \times [65536 - (RCAP2H, RCAP2L)]}$$

Dimana (RCAP2H, RCAP2L) adalah isi dari register RCAP2H dan RCAP2L yang diambil sebagai 16 bit integer tak bertanda.



Gambar 2.7. Timer 2 Sebagai Baud Rate Generator
Sumber: At 89S8252 Data Sheet (http://www.atmel.com)

2.3.11. Programmable Clock Out

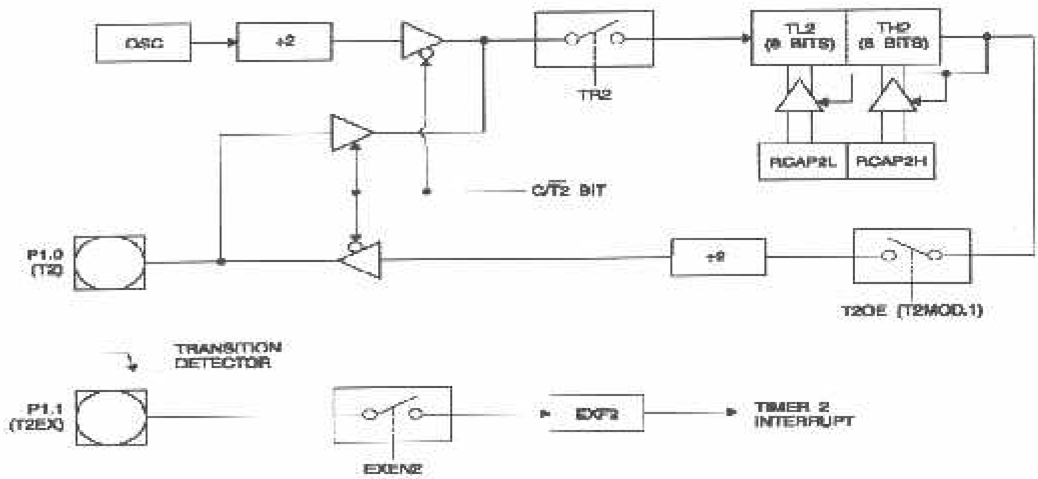
Fungsi terakhir dari timer 2 adalah untuk menghasilkan suatu detak(*clock*). Detak dengan siklus tugas 50% dapat diprogramkan sehingga keluaran dari P1.0. pin ini selain sebagai I/O biasa juga mempunyai dua fungsi alternatif. Dia dapat diprogram sebagai pin masukkan untuk *eksternal clock timer/counter* 2 atau sebagai penghasil *clock* dengan siklus 50% dengan rentang dari 61 Hz sampai 4 MHz jika dipakai 16 MHz kristal sebagai *frekwensi* mikrokontroller.

Untuk membuat *timer/counter* 2 sebagai generator detak, bit C/T2 (T2CON.1) harus dibuat rendah dan bit T2OE (T2MOD.1) harus diset. Bit TR2 (T2CON.2) sebagai *start timer*.

Frekuensi detak yang dihasilkan bergantung kepada frekuensi osilator yang dipakai dan nilai reload pada capture register timer 2 (RCAP2H, RCAP2L) seperti pada persamaan berikut :

$$\text{Frekuensi clock-out} = \frac{\text{Frekuensi Osilator}}{4 \times [65536 - (RCAP2H, RCAP2L)]}$$

Gambar berikut menunjukkan timer 2 sebagai clock out generator :



Gambar 2.8. Timer 2 Dalam Clock Out Mode
Sumber: At 89S8252 Data Sheet (http://www.atmel.com

2.4. LCD (*Liquid Cristal Display*)

Pada dasarnya indikator kristal cair terdiri dari satu jenis kristal cair yang transparan yang berada di antara 2 keping kaca.Bagian dalam keping kaca tersebut dilapisi bahan penghantar.Peghantar yang depan adalah tembus cahaya. Saat bahan penghantar diberi tegangan listrik maka terjadilah medan listrik yang menembus kristal. Kristal yang semula tampak bening dan tembus cahaya menjadi keruh.

Jarak antara kedua keping kaca adalah kira-kira 10μm, dan kuat medan yang diperlukan kira-kira 0,5V/μm. (Wasito S., 1994:189). Semakin kuat medannya maka akan semakin keruh kristal cair tersebut. Pada kuat medan kira-kira 3 sampai 5 V/μm terjadilah penjemuran (tidak dapat keruh lagi).

Karakteristik dari LCD dot matrik yang digunakan adalah sebagai berikut :

- 16 x 2 karakter dengan 5 x 7 dot matrik + kursor.
- ROM generator karakter dengan 192 tipe karakter.
- RAM generator karakter – karakter dengan 8 tipe karakter (untuk program write).
- 80 x 8 bit RAM data display.
- Dapat di interfacekan dengan kemungkinan MPU 4 bit atau 8 bit.
- RAM data atau RAM generator karakter yang dapat dibaca oleh MPU.
- + 5 Volt single power supplay.
- Power On Reset.
- Rangkaian temperature operasi 0°c sampai dengan 50°c.
- Beberapa fungsi instruksi yaitu display clear, cursor home, display ON/OFF, cursor ON/OFF, display blink, cursor shift, dan display shift.

Data pin pada display lcd lebih lengkapnya pada tabeldi bawah ini :

Tabel 2.9. Terminal Simbol LCD

NO	SYMBOL	LEVEL	FUNCTION	
1	Vss	-		0 V (GND)
2	Vcc	-		5 V $\pm$10%
3	Vee	-		For LCD Drive
4	RC	H/L	H : Data Input	L : Instruction Input
5	R/W	H/L	H : Read	L : Write
6	E	H	Enable signal	
7	DB0	H/L	Data bus	
8	DB1	H/L		
9	DB2	H/L		
10	DB3	H/L		
11	DB4	H/L		

Tampilan kristal cair menggunakan interaksi unik antara karakteristik elektrik dan optik dari suatu kelompok cairan agar tetap berada dalam bentuk kristal. Hal ini memberikan sifat optis yang sangat diperlukan sebagai piranti tampilan. Dengan pemakaian LCD, tidak ada cahaya yang dibangkitkan, sehingga mengurangi konsumsi arus dan dayanya. Sedangkan kemungkinan untuk mengaktifkan LCD diperlukan tegangan AC. Sehingga untuk penggerak (driver) LCD tidak dapat digunakan transistor-transistor bipolar.

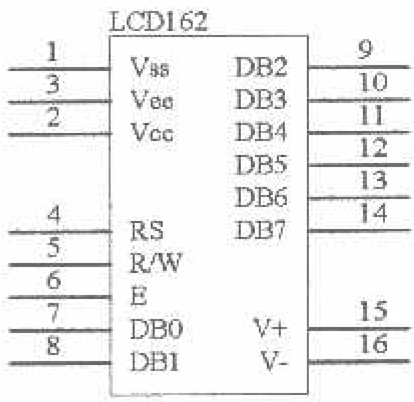
Alat ini menggunakan unit tampilan jenis LCD matrik jenis DMC 202. LCD ini memiliki 40 karakter (2 baris dengan 20 karakter tiap barisnya). Tiap karakter terdiri dari 5X7 titik ditambah dengan kursornya. Terdapat 192 karakter yang dapat ditulis dalam LCD ini [LCD USER MANUAL, 1987: 1). Rangkaian LCD dan hubungannya dengan mikrokontroler dapat dilihat pada bab berikutnya.

LCD jenis ini mempunyai 16 pin, pin 1 dihubungkan dengan Ground. Pin 2 adalah pin untuk mengatur kecerahan dari karakter yang ditulis, dihubungkan dengan +5volt melalui timer potensio 1Kohm. Sedangkan pin 3 adalah VDD yang dihubungkan dengan +5volt.

Pin 4 adalah RS (Register Selection) yang dipergunakan untuk memilih register. Jika diberi logika 1 maka register akan menjadi register data, jika diberi logika 0 maka akan menjadi register perintah. Pin 5 adalah R/W yaitu pin yang dipergunakan untuk memilih mode, yaitu mode baca atau tulis. Jika diberi logika 1 maka LCD akan membaca data dan jika diberi logika 0 maka LCD akan menulis data. Pin 6 adalah pin enable, untuk tiap pengiriman satu data ini harus diberi satu sinyal falling edge.

12	DB5	H/L		
13	DB6	H/L		
14	DB7	H/L		
15	V+BL	-	Back light supplay	4 – 4.2 V 50 – 200 mA
16	V-BL	-		0 V (GND)

Sumber : Roger L.Tokheim,1990



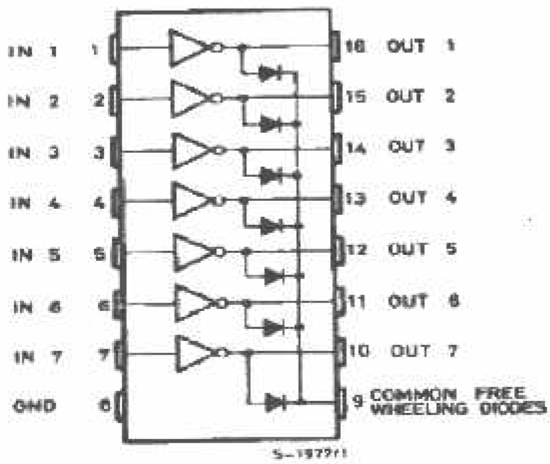
Gambar 2.9 Kontruksi Liquid Crystal Display

Sumber : Roger L.Tokheim,1990

2.5. IC ULN 2003A

Pada IC ULN 2003A didalamnya terdapat rangkaian penguat Darlington. Untuk satu IC ULN2003A terdapat 7 pasang rangkaian Darlington NPN yang tersusun dalam rangkaian *common catoda*. Rangkaian Darlington ini digunakan sebagai saklar. Pada masing-masing rangkaian Darlington arus kolektornya sebesar 500mA. Rangkaian Darlington yang ada di dalam IC ULN 2003A dapat diparalel guna untuk kebutuhan arus yang besar. Karenanya IC ini dapat diaplikasikan untuk *driver* relay, *driver* lampu, *driver display* dan *logic buffe* dan lain sebagainya.

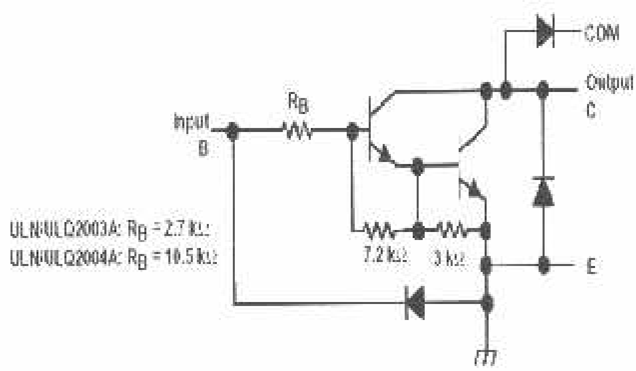
Adapun pin-pin koneksi yang ada dalam IC ULN 2003A dapat dilihai pada gambar 2.17 berikut ini:



Gambar 2.10. Pin-Pin Koneksi Dalam IC ULN 2003A

Data Sheet ULN2003A,Texas Instrumen Incorvorated ,hal 2

Sedangkan gambar untuk setiap rangkaian Darlington pada IC ULN 2003A dapat dilihat pada gambar 2.18.



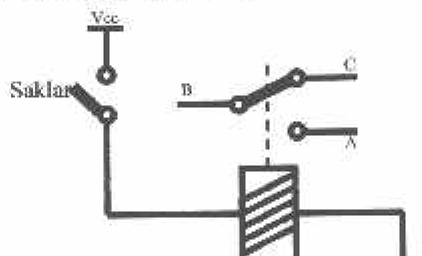
Gambar 2.11. Rangkaian Darlington didalam IC ULN 2003A

Data Sheet ULN2003A,Texas Instrumen Incorvorated ,hal 2

2.6. Relay

Relay adalah komponen elektronika yang umumnya digunakan untuk menghidupkan rangkaian kontrol dan peralatan lainnya yang mempunyai arus relatif kecil. Namun demikian relay dapat mengontrol tegangan dan arus yang lebih besar dengan menggunakan efek pengaturan. Efek pengaturan didapat dengan cara memanfaatkan tegangan kecil (5 - 34 volt) untuk mengaktifkan koil dan relay. Kemudian koil tersebut digunakan untuk mengubah-ubah posisi kontak. Kontak pada relay dapat digunakan untuk mensaklar (*switching*) tegangan yang lebih besar sampai 400Watt. Aliran arus yang digunakan untuk mengatur relay tersebut.

Pada dasarnya relay dapat dikatakan sebagai kontak beban elektrik yang mengontrol suatu rangkaian elektrik dengan cara membuka dan menutup kontak pada rangkaian lain. Apabila kontak relay adalah *normally open* (NO), maka akan terbuka bila relay tidak dialiri energi listrik. Sebaliknya pada titik kontak relay yang tergolong *normally close* (NC), akan tertutup bila relay tidak dialiri arus listrik. Pada kedua kondisi tersebut kontak - kontak pada relay akan berubah keadaannya apabila relay dialiri arus listrik.

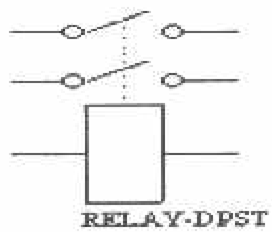


Gambar 2.12. Relay

(Sumber: Malvino, Prinsip-Prinsip Elektronika)

3. **DPST(*dual pin single terminal*)**

Simbol relay DPST

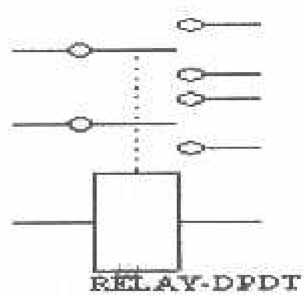


Gambar 2.15. Relay DPST

(Sumber: Malvino, Prinsip-Prinsip Elektronika)

4. **DPDT(*dual pin dual terminal*)**

Simbol relay DPDT



Gambar 2.16. Relay DPDT

(Sumber: Malvino, Prinsip-Prinsip Elektronika)

BAB III

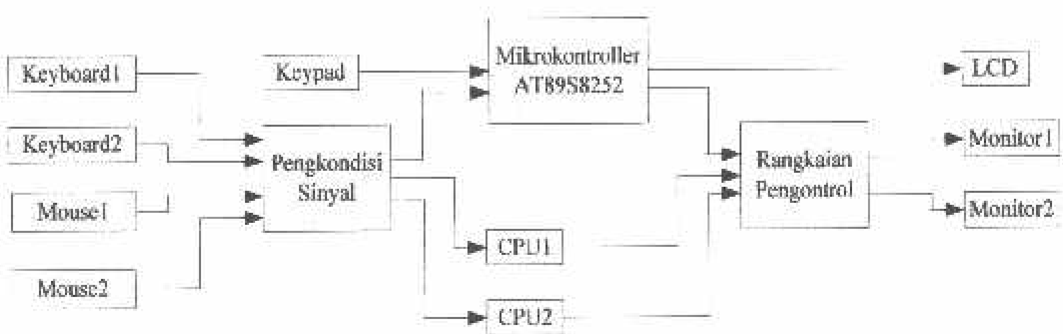
PERANCANGAN DAN PEMBUATAN ALAT

3.1 Gambaran Umum

Perancangan perangkat keras ini bertujuan untuk merencanakan sebuah rangkaian yang berfungsi mengontrol monitor pada Personal Computer wartel menjadi standby.

Adapun tahapan perancangan dan pembuatan alat yang berfungsi untuk membuat monitor pada Personal Computer wartel menjadi standby. adalah sebagai berikut : Rangkaian pembaca data, Rangkaian pengontrol, Keypad, Mikrokontroler AT89S8252, dan LCD TM 162 ABC.

3.2. Blok Diagram System



Gambar 3.1. Blok Diagram

Spesifikasi Alat :

1. **Mouse Dan Keyboard**

   Mouse dan *Keyboard* berfungsi sebagai inputan ke rangkaian pengkondisi sinyal.

2. **Keypad**

   Rangkaian keypad digunakan sebagai inputan *standby*.

3. **Rangkaian Pengkondisi Sinyal**

   Rangkaian ini digunakan sebagai pendeteksi inputan yang dihasil oleh *keyboard* atau *mouse* (apakah ada gerakan/sentuhan atau tidak).

4. **Rangkaian Pengontrol**

   Rangkaian yang digunakan sebagai pengontrol antara monitor dengan *PC* Sehinnga monitor dapat standby berdasarkan setingan waktu.

5. **LCD**

   Sebagai tampilan waktu yang disetting dari keypad.

6. **Mikrokontroller**

   Sebagai pusat pengendali keseluruhan sistem dengan menggunakan mikrokontroler AT89S8252.

3.3. Prinsip Kerja Alat

Dalam perencanaan dan pembuatan alat yang berfungsi untuk membuat monitor pada *Personal Computer* wartel menjadi standby, mikrokontroler AT89S8252 adalah sebagai pengendali utama. Mikrokontroler membutuhkan komponen system lain sebagai pendukung antara lain : Rangkaian pembaca data, Rangkaian pengontrol, LCD TM 162 ABC dan Keypad IC74922. Kerja system secara keseluruhan dapat dijelaskan sebagai berikut:

Rangkaian Pembaca Data adalah suatu Rangkaian berfungsi sebagai pembaca data-data masukan yang diambil dari mouse dan keyboard pada perangkat IBM PC. Rangkaian ini akan bekerja layaknya sebuah gerbang AND yang akan menghasilkan outputan logika 0 jika semua inputan logika 0 atau salah satu dari inputan berlogika 0. Sehingga jika mouse dan keyboard tidak aktif (tidak ditekan atau digeser), maka keluaran dari rangkaian ini akan berlogika 1. Data keluaran dari rangkaian ini akan diumpankan kemikrokontroler dan jika data yang diumpankan berlogika 1 maka oleh mikrokontroler data ini digunakan untuk mengaktifkan timer counter dan jika data pada timer counter ini sesuai dengan data waktu yang dimasukkan lewat keypad maka mikrokontroler akan mengeluarkan data untuk memutuskan hubungan antara CPU dengan monitor, dan apabila data yang masuk

3.4. Perencanaan Hardware

3.4.1. Perancangan Rangkaian Pengkondisi Sinyal

Rangkaian ini mendapatkan inputan dari Mouse dan Keyboard, dimana hubungan kaki konektor untuk keybord dan mouse dapat dilihat pada keterangan berikut:

A. Konektor Keybord

Kaki 1 = Pin Data,yang dihubungkan pada rangkaian AND (Keybord Data) dan PC

Kaki 2 = Reserved, langsung ke komputer

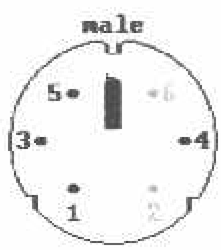
Kaki 3 = GND, dihubungkan ke ground Langsung ke komputer (Reserved)

Kaki 4 = +5V dihubungkan ke mikrokontroller dan langsung ke komputer

Kaki 5 = Pin Clock, Langsung dihubungkan ke computer

Kaki 6 = Reserved, langsung ke computer

Adapun gambar konektor keybord dapat dilihat dibawah ini.



Gambar 3.2. Konektor Keyboard

B. Konektor Mouse

Kaki 1 = Pin Data,yang dihubungkan pada rangkaian AND (Keybord Data) dan PC

Kaki 2 = Reserved, langsung ke komputer

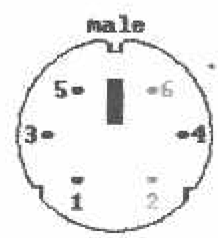
Kaki 3 = GND, dihubungkan ke ground Langsung ke komputer (Reserved)

Kaki 4 = +5V dihubungkan ke mikrokontroller dan langsung ke komputer

Kaki 5 = Pin Clock, Langsung dihubungkan ke computer

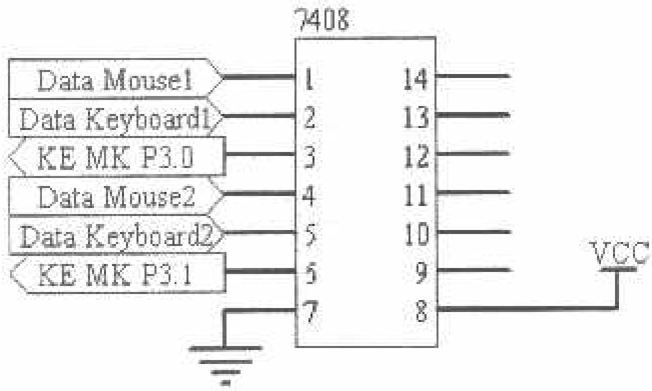
Kaki 6 = Reserved, langsung ke computer

Adapun gambar konektor keybord dapat dilihat dibawah ini.



Gambar 3.3. Konektor Keyboard

Rangkaian Pengkondisi Siyal ini berfungsi sebagai pembaca data-data masukan yang diambil dari mouse dan keyboard pada perangkat IBM PC. Rangkaian ini akan bekerja layaknya sebuah gerbang AND yang akan menghasilkan keluaran logika 1 jika semua masukan logika 0. Sehingga jika mouse dan keyboard tidak aktif (tidak ditekan atau digeser), maka keluaran dari rangkaian ini akan berlogika 1, gambar rangkaian pembaca data ditunjukkan pada Gambar 3.4 berikut:



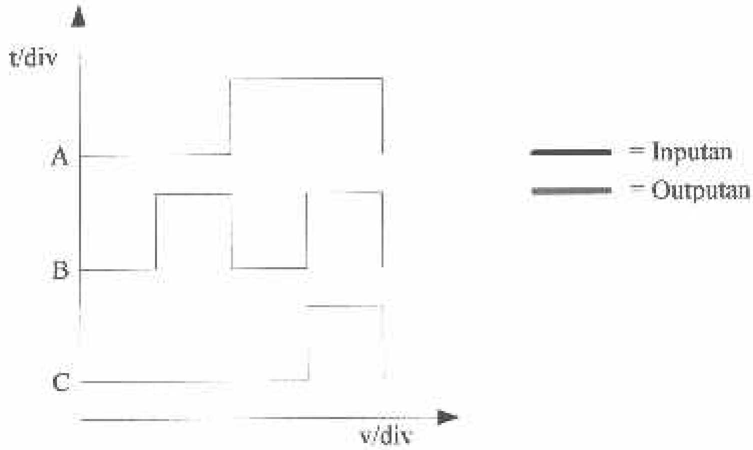
Gambar 3.4. Rangkaian Pembaca Data

Adapun hasil dari keluaran rangkaian pembaca data berdasarkan tabel kebenaran dari gerbang AND dengan tiga inputan yaitu A, B dan C dapat dilihat pada tabel 3.1 dibawah ini

Tabel 3.1.

Tabel Kebenaran Rangkaian Pembacaan Data Gerbang AND

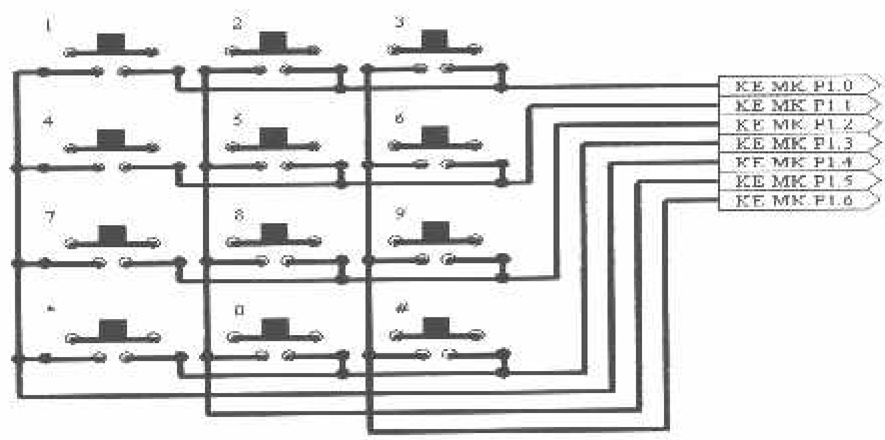
A	B	C
0	0	0
0	1	0
1	0	0
1	1	1



Grafik 3.1 Karakteristik Gerbang And

3.4.2. Perancangan Rangkaian Keypad

Rangkaian Keypad ini merupakan rangkaian yang berfungsi sebagai tombol untuk inputan waktu standby. Keypad ini tersusun atas tombol matrik 4x3 dan masing-masing tombol terhubung ke mikro.



Gambar 3.5. Keypad Matrik 3 x 4 dengan Mikrokontroller AT89S8252

Sumber : Perencanaan, Mata Kuliah ITN Malang

Dari rangkaian diatas, dalam proses scanning, jika kondisi awal pada mikrokontroller berlogika high (1), apabila ada penekanan tombol 1 maka P1.0 berlogika high "1" dan P1.4 berlogika low "0" dan seterus. Keterangan lebih lanjut dapat dilihat pada table sebagai berikut :

Tabel 3.2.

Pada Saat Keypad Kolom1 Di Clear

Tombol	Baris	Clr Kolom 1
1	P1.0=1	P1.4=0
4	P1.1=1	P1.4=0
7	P1.2=1	P1.4=0
*	P1.3=1	P1.4=0

Tabel 3.3.

Pada Saat Keypad Kolom2 Di Clear Dan Kolom1 Di Setbit

Tombol	Baris	Clr Kolom2/Setb Kolom1
2	P1.0=1	P1.5=0
5	P1.1=1	P1.5=0
8	P1.2=1	P1.5=0
0	P1.3=1	P1.5=0

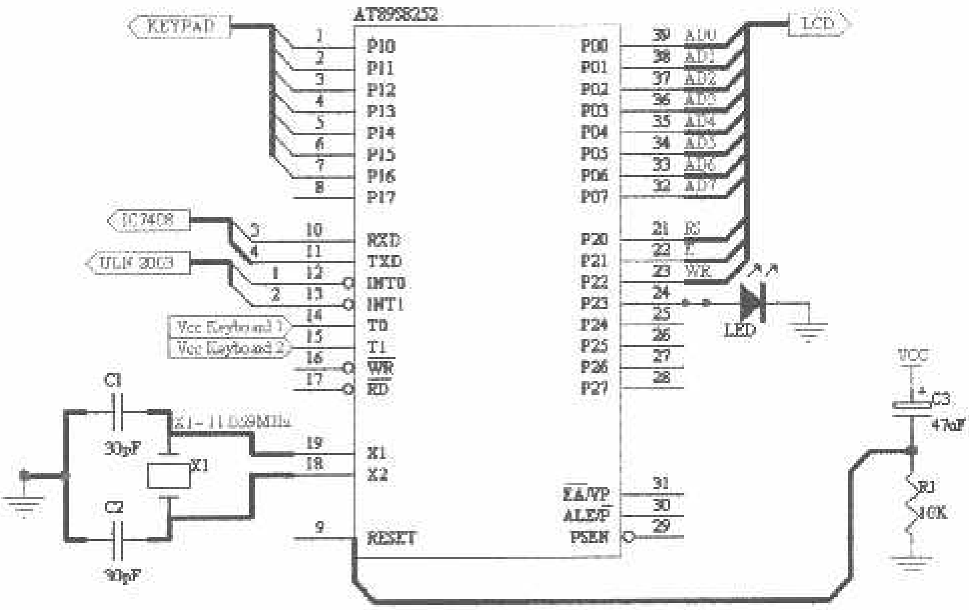
Tabel 3.4.

Pada Saa Keypad Kolom2 Di Clear Dan Kolom1 Di Setbit

Tombol	Baris	Clr Kolom3/Setb Kolom2
1	P1.0=1	P1.6=0
4	P1.1=1	P1.6=0
7	P1.2=1	P1.6=0
*	P1.3=1	P1.6=0

3.4.3. Perancangan Rangkaian Mikrokontroler AT89S8252

Mikrokontroler pada sistem berfungsi untuk mengolah data masukan dari keypad yang selanjutnya akan mengendalikan tampilan LCD. Mikrokontroler yang digunakan pada sistem ini adalah Mikrokontroler jenis AT89S8252 yang merupakan IC CMOS 8 bit internal RAM, 40 bit dan 3 port I/O. Diperlihatkan pada gambar 3.7. sebagai berikut :



Gambar 3.6. Rangkaian Mikrokontroler AT89S8252

Sumber : Perencanaan, Mata Kuliah ITN Malang

Adapun baagian-bagian fungsi pin yang digunakan :

1. Port 0.0 sampai Port 0.7 sebagai outputan ke LCD 162
2. Port 1.0 sampai Port 1.6 digunakan untuk inputan keypad 3x4
3. Port 3.0 dan Port 3.1 berfungsi sebagai inputan gerbang AND
4. Port 3.2 dan Port 3.3 berfungsi sebagai outputan ke ULN2003
5. Port 3.4 dan Port 3.5 berfungsi sebagai inputan dari Vcc keyboard

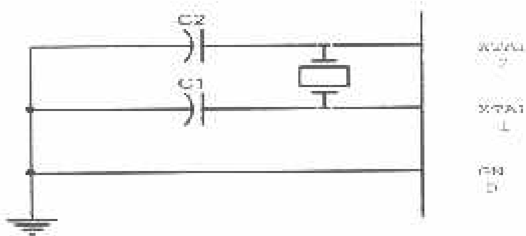
3.4.4. Perancangan Rangkaian Clock Internal

Mikrokontroler AT89S8252 ini memiliki *internal clock* generator yang berfungsi sebagai sumber *clock*, tetapi masih diperlukan rangkaian tambahan untuk membangkitkan *clock* tersebut. Rangkaian ini terdiri dari 2 buah kapasitor dan sebuah kristal dengan ketentuan:

C1 dan C2 = 20 pF – 40 pF untuk kristal

= 30 pF – 50 pF untuk keramik resonator

Dalam perencanaan rangkain mikrokontroller ini digunakan kapasitor sebesar 30 pF sampai dengan 10 pF.



Gambar 3.7. Rangkaian Clock

3.4.5. Perancangan Rangkaian LCD (*Liquid Cristal Display*) TM 162 ABC

Pada lembaran data sheet modul LCD M1632 *SEIKO INSTRUMENT INC.* disebutkan bahwa :

Power supply LCD meliputi :

Vss = 0 V (GND)

Vcc = 5 V ± 10% (2mA)

Vee = Vcc - 13,3 V sampai Vcc + 0,3 V (1mA pada Vee = 0,25 V)

Vee = Vcc - 13,3 V sampai Vcc + 0,3 V (1mA pada Vee = 0,25 V)

Power supply Back Light LCD :

V + BL = 4 V sampai 4,2 V (50 sampai 200 mA)

V - BL = 0 V (GND)

Untuk memenuhi ketentuan diatas, maka digunakan sebuah Variabel resistor dengan tujuan membuat tegangan variable untuk *input* Vee.

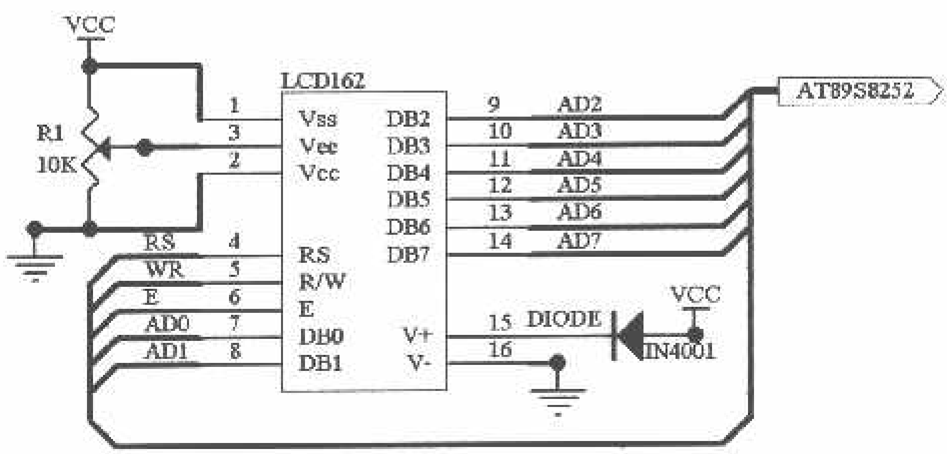
Pada input V + BL dipasang sebuah dioda IN4001 (bahan silicon dengan Vd = 0,65 V sampai 0,7 V). Tujuannya adalah didapatkan tegangan V + BL sebesar 4,3 V dengan perhitungan sebagai berukut :

$$Vcc = Vd + (V+BL)$$

$$5 = 0,7 + (V+BL)$$

$$(V+BL) = 5 - 0,7 = 4,3\ V$$

Dipilih dioda IN4001 karena arus maksimum yang bisa dilewatkan oleh dioda sebesar 1A. Berikut ini adalah rangkaian lengkap modul LCD yang digunakan dalam perancangan, yang ditunjukkan pada Gambar 3.5.



Gambar 3.8. Rangkaian LCD

Sumber : Perencanaan, Mata Kuliah ITN Malang

3.4.6. Perancangan Rangkaian Pengontrol

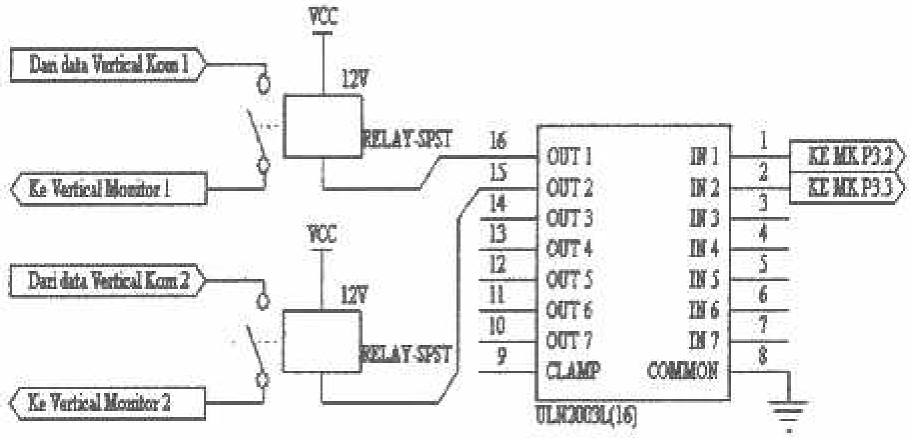
Untuk driver penggerak relay digunakan IC ULN2003A dan relay sebagai komponen utamanya, dengan tegangan 5 Volt dapat memicu IC ULN2003A dan arus maksimum yang diperbolehkan sebesar 500mA dengan suhu kerja dari -20°C sampai 80°C dengan data yang ada diatas maka IC ULN2003A mampu digunakan untuk menghidupkan dan mematikan relay yang memiliki tegangan maksimal sebesar 12 Volt dengan resistansi kumparan sebesar 400 Ω jadi dapat diketahui arus relay sebesar:

$$\text{Dimana: } I_{relay} = \frac{VCC}{R.relay}$$

$$= \frac{12}{400}$$

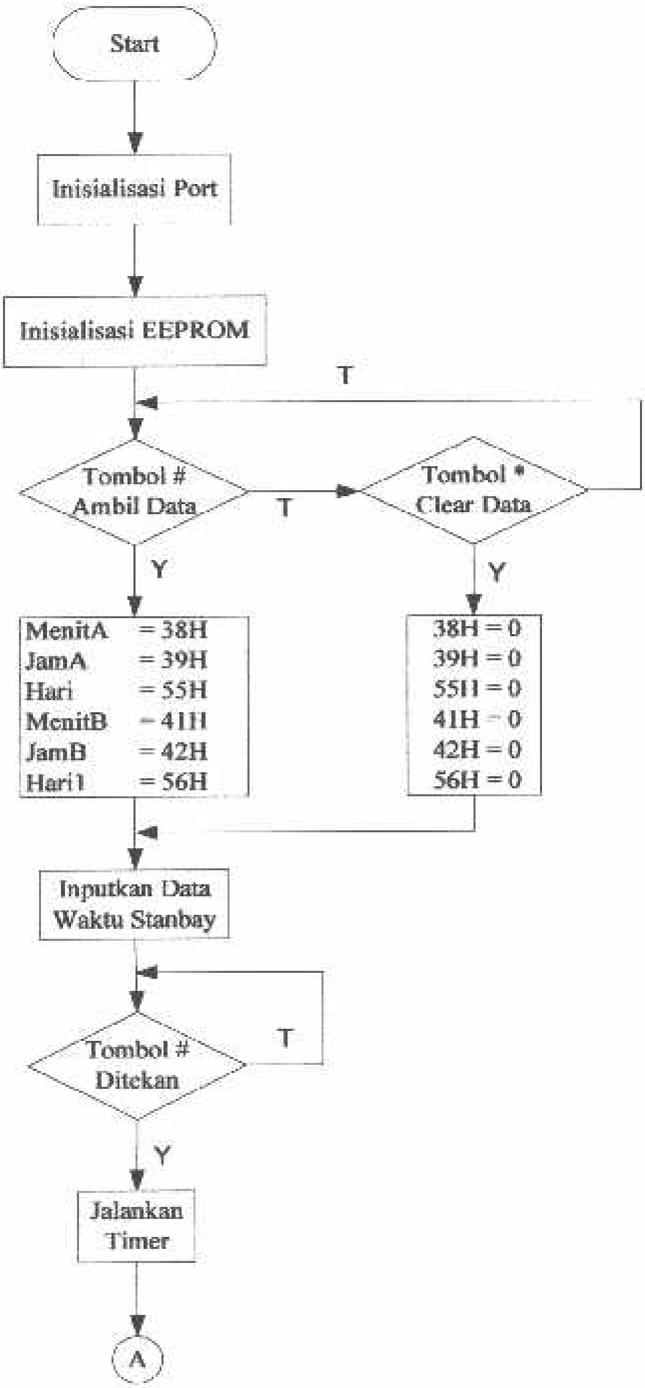
$$= 30 \text{ mA}$$

Jadi jika ULN 2003 tidak mendapatkan tegangan 5V dari Mikrokontroller AT89S8252 maka relay SPST 12V tidak aktif sehingga memutuskan data vertical CPU dengan vertical monitor dan monitor menjadi standbay. Jika ULN 2003 mendapatkan tegangan dari Mikrokontroller AT89S8252 maka relay SPST 12V akan aktif sehingga menghubungkan data vertical CPU dengan vertical monitor dan monitor menjadi akan aktif kembali.

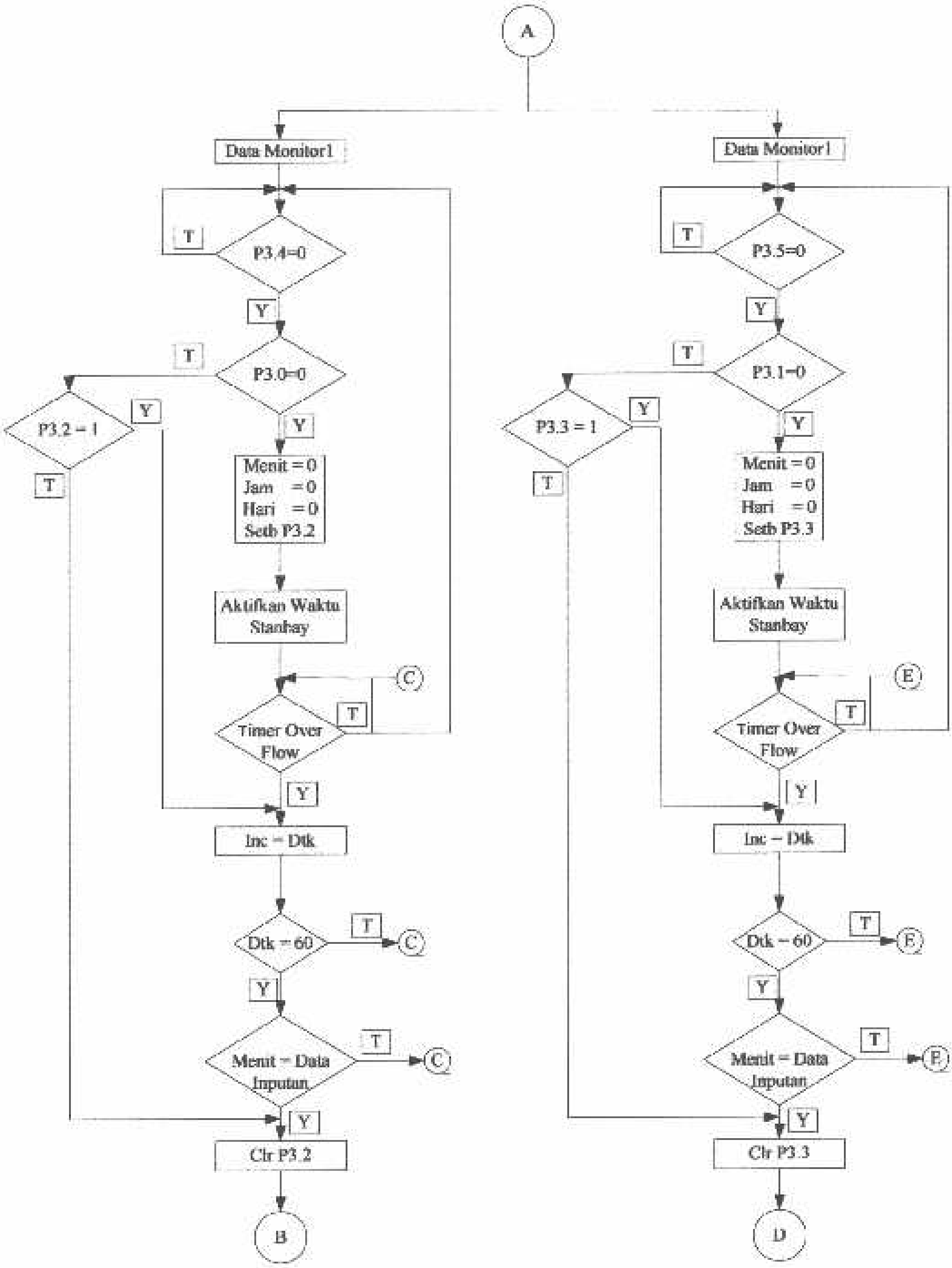


Gambar 3.9. Rangkaian Pengontrol

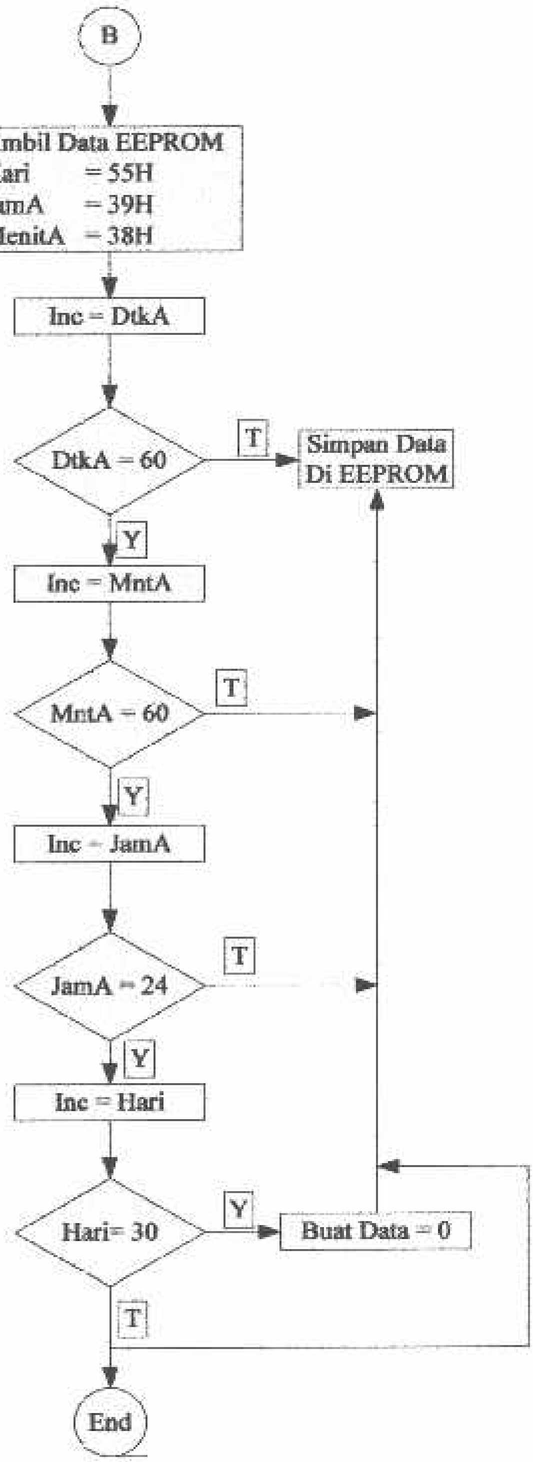
3.5. Perancangan Perangkat Lunak (Software)



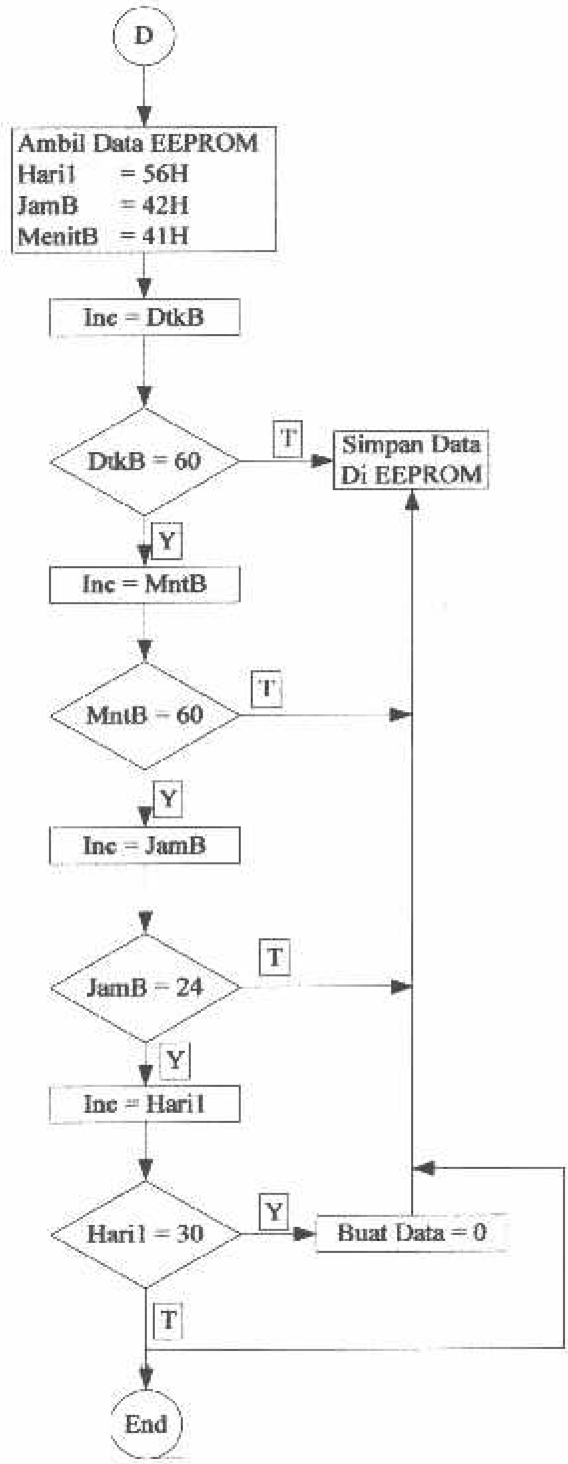
Gambar 3.10. Flowchart Diagram 1



Gamabar 3.11. Flowchart Diagram 2



Gamabar 3.12. Flowchart Diagram 3



Gamabar 3.13. Flowchart Diagram 4

BAB IV

PENGUJIAN ALAT DAN ANALISA DATA

4.1.PENGUJIAN ALAT

Untuk mendapatkan hasil yang maksimal setelah melaksanakan perancangan dan pembuatan alat, maka perlu dilakukan suatu pengujian terhadap alat yang telah dibuat. Pengujian ini bertujuan untuk mengetahui apakah alat yang telah dibuat dapat bekerja sesuai yang dengan perencanaan.

Bagian-bagian yang diuji dari peralatan ini adalah :

1. Outputan Mouse dan Keyboard
2. Rangkaian *keypad.*
3. Rangkaian Liquid Cristal Display (LCD) .
4. Rangkaian Pengontrol Driver Relay

4.1.1. Pengujian Outputan Mouse Dan Keyboard

a.Tujuan

Pengujian outputan data mouse dan keyboard di gerbang AND ditujukan untuk mengetahui apakah pada saat ada penekana atau pada saat tidak ada penekanan berlogika high atau low.

b.Peralatan yang digunakan

1. Ociloscope

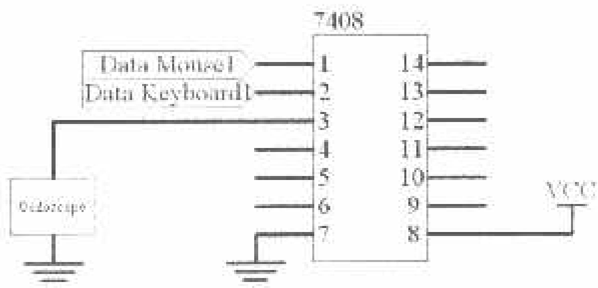
2.Mouse dan Keyboard

3.IC gerbang AND

c.Prosedur Pengujian

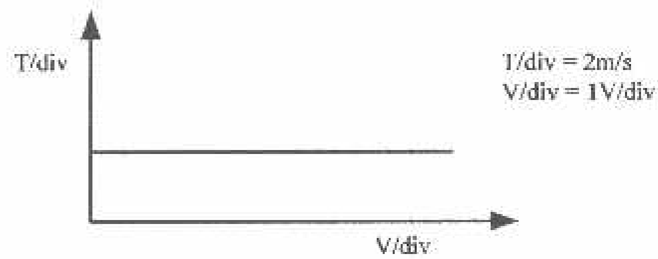
1.Mengatur posisi Ociloscope pada ouputan gerbang lalu dihubungkan ke ground

2.Mekukan penekanan pada mouse dan keyboard secara bergantian, cara pengukuran dapat dilihat seperti gambar berikut:

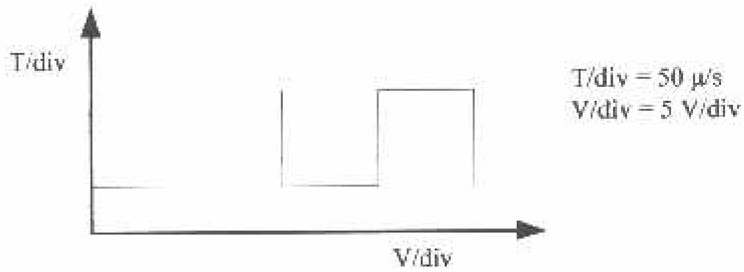


Gambar 4.1. Cara Pengukuran Outputan AND

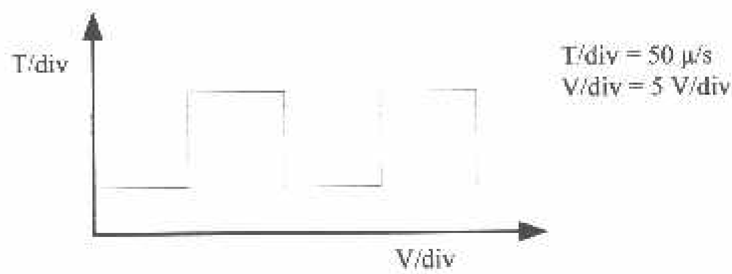
d.Hasil Pengujian



Grafik 4.1. Hasil Pengujian Pada Saat Tidak Ada Penekanan



Grafik 4.2. Hasil Penakanan Pada Mouse



Grafik 4.3. Hasil Penekanan Pada Keyboard

Tabel 4.1. Hasil Pengujian Mouse Dan Keyboard

Mouse	Keyboard	AND	Timer	Monitor
0	0	0	Off	On
0	1	0	Off	On
1	0	0	Off	On
1	1	1	On	Off

4.1.2. Pengujian Rangkaian Keypad

a.Tujuan

Pada rangkaian keypad, menggunakan matrik keypad 4x3 sehingga ada 12 fasilitas tombol yang tersedia. Tombol yang tersedia adalah 1, 2, 3 pada baris pertama, tombol 4, 5, 6 pada baris ke dua, tombol 7, 8, 9 pada baris ke tiga, serta tombol *, 0, # pada baris ke empat. Pada masing-masing tombol keypad ini prinsipnya hanya menghubungkan atau menggabungkan Port pada baris dengan Port pada kolom yang dimana kondisi awal pada mikro berlogika high.

b. Peralatan yang digunakan:

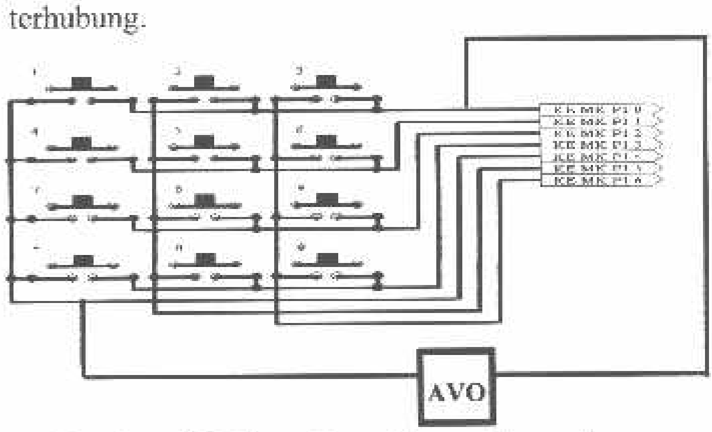
1) Avometer

2) Keypad

c. Prosedur pengujian:

1)Mengatur posisi Avometer pada posisi setiap baris dan kolom

2)Melakukan penekanan pada tombol keypad lalu mengukur dengan menggunakan avometer untuk mencari jalur mana yang terhubung.



Gambar 4.2. Cara Pengukuran Keypad

c.Hasil pengujian keypad ditunjukkan pada tabel dibawah ini.

Tabel 4.2. Hasil Pengujian Keypad

Pada Saat Kolom 1 Diclear

Tombol	Baris	Clr Kolom 1
1	Baris1=1	0
4	Baris2=1	0
7	Baris3=1	0
*	Baris4=1	0

Tabel 4.3. Hasil Pengujian Keypad

Pada Saat Kolom 2 Diclear Dan Kolom1 Di Setbit

Tombol	Baris	Clr Kolom2/Setb Kolom1
2	Baris1=1	0
5	Baris2=1	0
8	Baris3=1	0
0	Baris4=1	0

Tabel 4.4. Hasil Pengujian Keypad

Pada Saat Kolom 3 Diclear Dan Kolom2 Di Setbit

Tombol	Baris	Clr Kolom3/Setb Kolom2
1	Baris1=1	0
4	Baris2=1	0
7	Baris3=1	0
*	Baris4=1	0

d.Analisa Pengujian

karena kondisi awal pada mikrokontroller berlogiks high, maka jika menekan tombol

Berdasarkan hasil pengujian:

Pada saat Kolom 1 diclear

Tombol keypad 1 ditekan menghasilkan P1.0=1 dan P1.4=0

Tombol keypad 4 ditekan menghasilkan P1.1=1 dan P1.4=0

Tombol keypad 7 ditekan menghasilkan P1.2=1 dan P1.4=0

Tombol keypad * ditekan menghasilkan P1.3=1 dan P1.4=0

Pada saat Kolom 2 diclear dan Kolom1 Disetbit

Tombol keypad 2 ditekan menghasilkan P1.0=1 dan P1.5=0

Tombol keypad 5 ditekan menghasilkan P1.1=1 dan P1.5=0

Tombol keypad 8 ditekan menghasilkan P1.2=1 dan P1.5=0

Tombol keypad 0 ditekan menghasilkan P1.3=1 dan P1.5=0

Pada saat di Clr Kolom3 dan Set Kolom2

Tombol keypad 3 ditekan menghasilkan P1.0=1 dan P1.6=0

Tombol keypad 6 ditekan menghasilkan P1.0=1 dan P1.6=0

Tombol keypad 9 ditekan menghasilkan P1.0=1 dan P1.6=0

Tombol keypad # ditekan menghasilkan P1.0=1 dan P1.6=0

4.1.3. Pengujian Rangkaian LCD (Liquid Cristal Display)

a)Tujuan

Tujuan pengujian rangkaian LCD ini untuk dapat mengetahui kinerja dari pada LCD tersebut, dimana LCD yang diuji adalah LCD dengan tipe M 162 A yang terdiri dari 16 pin dengan fungsi masing-masing adapun alat yang digunakan adalah sebagai berikut:

b)Pengujian Rangkaian LCD.

Alat yang digunakan:

1).Avometer

2). LCD

c)Langkah pengujian

Sesuai dengan perencanaan alat dan dari hasil pengujian yang dilakukan, RS dari LCD dihubungkan Mikrokontroler master di Port 2.0 sementara itu Enable dihubungkan dengan Port 2.1. LCD apabila membaca instruksi maka Port 2.0 harus berlogika 0 (Low) secara program dengan perintah CLR P2.7. Pada saat membaca data dari MCU master maka P2.0 harus berlogika 1 (high) dengan perintah

SETB P2.0 Untuk pin Enable dihubungkan dengan Port 2.1 diberikan logika 1 pada saat penulisan atau pembacaan data. Untuk D0 sampai dengan D7 merupakan tempat masuknya data dan instruksi yang diberikan melalui port MCU master yaitu Port 0.0 sampai dengan P0.7.

d)Data Hasil Pengujian

Tabel 4.5. Hasil Pengujian LCD

Angka	D7	D6	D5	D4	D3	D2	D1	D0
1	0	0	0	1	0	0	1	1
2	0	0	1	0	0	0	1	1
3	0	0	1	1	0	0	1	1

4.1.4. Pengujian Rangkaian Pengontrol

a)Tujuan

Tujuan pengujian ini digunakan untuk mengetahui outputan tegangan dari Ic Driver ULN20003 yang dikontrol oleh mikrokontroller untuk mengaktifkan atau mengnonaktifkan Relay.

b) Alat yang Digunakan

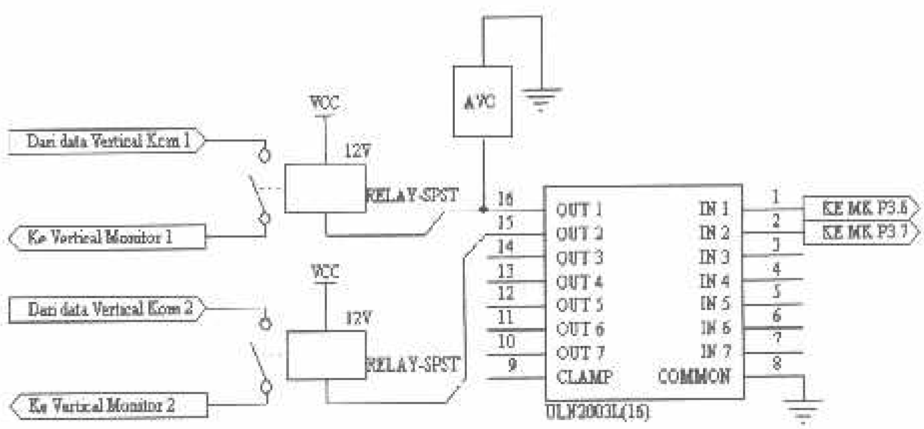
1.Rangkaian driver relay.

2.Power supply 12V dan 5V.

3.Multimeter.

c) **Prosedur Pengujian**

1. Merangkaian keseluruhan system pengujian seperti pada gambar 4.2.
2. Mengaktifkan power supply.
3. Memasangkan multimeter pada 5 titik pengukuran.
4. Mengukuran pada dua kondisi yaitu relay dalam kondisi aktif dan relay dalam kondisi tidak aktif.
5. Memasukkan hasil pengukuran pada tabel 4.2.



Gamabar 4.3. Pengukuran Outputan Relay

d)Hasil Pengukuran

Tabel 4.6. Hasil Pengukuran Relay

ULN	OUT(V)	RELAY
0	14	Relay Nonaktif
1	0	Relay Aktif

4.1.5. Pengujian Timer Pada Mikrokontroler

a)Tujuan

Pengujian disini untuk mengetahui berapa error waktu yang dibangkitkan pada mikrokontroler.

b)Procedur Pengujian

Membandingkan waktu pada jam yang sebenarnya dengan waktu yang dibangkitkan pada timer mikrokontroler yang di tam pilkan di display.

c)Analisa Pengujian

Dalam waktu satu jam pada mikrokontroler dibandingakan dengan dengan waktu yang sebenarnya. Dalam satu jam sama dengan 3600 detik. Dalam pengujian disini dilakukan pecobaan sebanyak 5 kali.

Tabel 4.7. Data Perbandinagan Timer Dengan Waktu Sebenarnaya

NO	JAM SEBENARNYA	TIMER MIKROKONTOLER	SELISIH
1	1 Jam	59 Menit 58 Detik	2 Detik
2	1 Jam	59 Menit 57 Detik	3 Detik
3	1 Jam	59 Menit 58 Detik	2 Detik
4	1 Jam	59 Menit 56 Detik	4 Detik
5	1 Jam	59 Menit 57 Detik	3 Detik
	Rata-Rata Selisih		

$$\text{Error} = \frac{\text{Selisih}}{\text{Waktu Sebenarnya}} \text{ X } 100\%$$

Presentase error timer mikrokontroler pada setiap percobaan :

Diketahui 1jam = 3600 detik

Percobaan 1 :

$$E_1 = \frac{2}{3600} X100\%$$
$$E_{1=0,055\%}$$

Percobaan 2 :

$$E_2 = \frac{3}{3600} X100\%$$
$$E_{2=0,083\%}$$

Percobaan 3 :

$$E_3 = \frac{2}{3600} X100\%$$
$$E_{3=0,055\%}$$

Percobaan 4 :

$$E4 = \frac{4}{3600} X100\%$$

$$E_4 = 0{,}11\%$$

Percbaan 5 :

$$E_5 = \frac{3}{3600} X100\%$$

$$E_5 = 0{,}083\%$$

Tabel 4.8. Persentase Error Timer Dengan Waktu Sebenarnaya

NO	JAM SEBENARNYA	TIMER MIKROKONTOLER	PERENTASE ERROR
1	1 Jam	59 Menit 58 Detik	0,055%
2	1 Jam	59 Menit 57 Detik	0,083%
3	1 Jam	59 Menit 58 Detik	0,055%
4	1 Jam	59 Menit 56 Detik	0,11%
5	1 Jam	59 Menit 57 Detik	0,083%

Sehingga rata-rata presentasi error yang didapat sebagaiberikut :

$$Rata-rata(Error) = \frac{E_1 + E_2 + E_3 + E_4 + E_5}{5}$$

$$Rata-rata(Error) = \frac{0{,}055 + 0{,}083 + 0{,}055 + 0{,}11 + 0{,}083}{5}$$

$$Rata-rata(Error) = 0.0772\%$$

4.2. ANALISA PERHITUNGAN STANDBY MONITOR

Analisa Perhitungan standby pada monitor disini untuk mengetahui berapa penghematan Energi listirik yang dipakai jika menggunakan alat ini. Dimana perhitungan disini menghitung daya listrik pada monitor 14 Inc dengan data sebagai berikut :

Arus = 1,5 Amper

Tegangan = 240 Volt

Berdasarkan Pengukuran spesifikasi monitor Pada Saat Aktif :

Tegangan = 230 Volt

Cos φ = 0,34

Arus = 1,5 Amper

Berdasarkan Pengukuran spesifikasi monitor Pada Saat Standby

Tegangan = 228 Volt

Cos φ = 0,25

Arus = 0,03 Amper

Perumusan Energi Listrik :

$E = V \times I \times \cos\varphi \times t$

Dimana :

V = Tegangan

I = Arus

Cos φ = Faktor daya

Besrdasarkan survey pada wartel, waktu yang tidak digunakan pada saat tidak penelepon rata rata 3 jam setiap harinya.

- Dimana pada saat penelepon tidak ada dan monitor sedang aktif :

  t – 3 jam

  $E_1 = 230x1,5x0,34x3 = 351,9 Watt.Jam$

- Dimana pada saat monitor dalam keadaan Standby :

  $E_2 = 228x0,03x0,25x3 = 5,13 Watt.Jam$

- Sehingga Energi listrik yang dihemat selama 3 jam:

  $E_3 = 351,9 - 5,13 = 346,77 Watt.Jam$

- Sehingga persentasi penghematan energi listrik pada saat monitor standby dengan monitor aktiv :

$$E_4 = \frac{E_3}{E1} x100\%$$
$$E_4 = \frac{346,77}{351,9} x100\%$$
$$E_4 = 98,5\%$$

BAB V

KESIMPULAN DAN SARAN

5.1. KESIMPULAN

Berdasarkan perencanaan dan pembuatan alat Penghematan Listrik Dalam Pengoperasian Monitor Personal Computer (CPU) Pada Wartel Berbasis Mikrokontroller AT89S8252 ini dapat ditarik Beberapa kesimpulan sebagai berikut :

1. Berdasarkan pengujian alat dihasilkan bahwa dengan mengontrol monitor *Personal Computer* pada wartel dapat diminimalisir daya listrik, sehingga diperoleh perbandingan persentase daya listrik antara monitor aktif dengan monitor standby sebesar 98,5%.
2. Berdasarkan pengujian timer pada mikrokontroler yang dibandingkan dengan wkatu sebenarnya, terjadi Error sebesar 0,772%.
3. Berdasarkan pengujian pada pemutusan data VGA pada monitor melalui keyboad dan mouse terjadi efek yang berupa garis-garis pada monitor, efek tersebut disebabkan karena adanya pengaruh tegangan pada driver relay.

5.2. SARAN

1. Alat ini hanya dapat mengontrol dua buah monitor saja, sehingga alat ini terbatas penggunaannya.
2. Tampilan dari alat ini hanya menampilkan lamanya waktu standby pada Monitor dan tampilan setingan inputan standby.

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Albert Paul Malvino, Ph.D. (1994). ***Prinsip-prinsip Elektronika jilid I danII.*** Alih Bahasa M. Barmawi, Ph.D. Jakarta : Penerbit Erlangga.

Elektuur, Steeman J.P.M. (1991). ***Data Sheet Book I.***Alih Bahasa Wasito Jakarta ; PT.Gramedia.

DAFTAR ACUAN

Atmel AT89S8252 Data Sheet

Motorola SN7408 Data Sheet

http://www.computer-engineering.org/

INSTITUT TEKNOLOGI NASIONAL MALANG
FAKULTAS TEKNOLOGI INDUSTRI
JURUSAN TEKNIK ELEKTRO

FORMULIR BIMBINGAN SKRIPSI

Nama : Vico Romandika
NIM : 02.17.079
Masa Bimbingan : 12 Januari 2007 s/d 12 Juli 2007
Judul Skripsi : Perencanaan Dan Pembuatan Alat Penghemat Listrik Dalam Pengoperasian Monitor Personal Computer (PC) Pada Wartel Berbasis Mikrokontroller AT89S8252

No	Tanggal	Uraian	Paraf Pembimbing
1	23-02-2007	Bab I, II, III	
2	24-02-2007	Bab I, II, III, IV	
3	25-02-2007	Revisi Blok Diagram	
4	27-02-2007	Revisi Pengujian	
5	28-02-2007	Revisi Perhitungan Analisa	
6	01-03-2007	Revisi Data	
7	02-03-2007	Revisi Teori Relay	
8	03-03-2007	Makalah Seminar	
9			
10			
11			

Malang, 11-Maret-2007
Dosen Pembimbing

(Ir. Eko Nurcahyo)
NIP : 1028700172

Form S-4a

INSTITUT TEKNOLOGI NASIONAL
Jl. Raya Karanglo Km 2
MALANG

FORM BIMBINGAN SKRIPSI

Nama	: Vico Romandika
NIM	: 02.17.079
Masa Bimbingan	: 12 Januari 2007 s/d 12 Juli 2007
Judul	: Perencanaan Dan Pembuatan Alat Penghemat Listrik Dalam Pengoperasian Monitor Personal Computer (PC) Pada Wartel Berbasis Mikrokontroler AT89S8252

NO	TANGGAL	URAIAN	PARAF
1	23/2 '07	Bab I, II, III	
2	25/2 '07	Bab I, II, III, IV	
3	26/2 07	Revisi Blok diagram	
4	27/2 07	Revisi Pengujian	
5	28/2 07	Revisi Analisa	
6	01/3 07	Revisi Data	
7	03/3 07	Revisi Teori Relay	
8	04/4 07	Makalah Seminar	
9	09/3 /07	Acc Compre	
10			

Malang, 23 - 02 - 2007
Dosen Pembimbing

(Ir.M. Ashar, MT) 090
NIP :

Form S-4a

INSTITUT TEKNOLOGI NASIONAL
FAKULTAS TEKNOLOGI INDUSTRI
JURUSAN TEKNIK ELEKTRO

Formulir Perbaikan Ujian Skripsi

Dalam pelaksanaan Ujian Skripsi Janjang Strata 1 Jurusan Teknik Elektro Konsentasi T. Energi Listrik / T. Elektronika, maka perlu adanya perbaikan skripsi untuk mahasiswa :

NAMA : Vido Rodiandika
N I M : 0217079
Perbaikan meliputi :

1. Bab II banyak yg tdk ada referensi pada gambar dan tabel nya.

2. Kesimpulan tolong direvisi. Pengujian timer dan efek penimbunan data VGA, mouse dan keyboard harus dicek ?

Malang,

(Ir. F. Yudi Limpraptono, MT)

INSTITUT TEKNOLOGI NASIONAL MALANG
FAKULTAS TEKNOLOGI INDUSTRI
JURUSAN TEKNIK ELEKTRO
Jl. Karanglo KM. 2 Malang

FORMOLIR PERBAIKAN SKRIPSI

Dalam pelaksanaan Ujian Skripsi Jenjang Strata Satu (S-1) Jurusan Teknik Elektro Konsentrasi Teknik Elektronika,makaperlu adanya perbaikan skripsi untuk mahasiswa :

Nama	: Vico Romandika
NIM	: 02.17.079
Jurusan	: Teknik Elektro S-1
Konsentrasi	: Teknik Elektronika
Masa Bimbingan	: 12 Januari 2007 s/d 12 Juli 2007
Judul Skripsi	: Perencanaan Dan Pembuatan Alat Penghemat Listrik Dalam Pengoperasian Monitor Personal Computer (PC) Pada Wartel Berbasis Mikrokontroller AT89S8252

Perbaikan Meliputi :

NO	URAIAN	PARAF
1	Perbaikan BAB II pada referensi gambar dan tabel	
2	Kesimpulan pada pengujian timer	
3	Kesimpulan pada efek yang ditimbulkan dalam pemutusan data VGA pada monitor	

Diperiksa Dan Disetujui

Pembimbing I	Pembimbing II
(Ir. Eko Nurcahyo.)	**(M. Ashar, ST. MT)**
NIP : 1018100036	**NIP :**

Anggota Penguji

Penguji Pertama	Penguji Kedua
(Ir.F.Yudi Limpraptono, MT)	**(Soeyohadi, ST. MT)**
NIP : 1039500274	**NIP**

```
Org     00h
; LCD CONSTANTA
DISPCLR     EQU 00000001B
BLINK       EQU 00001101B
ENTRMOD     EQU 00000110B
DISPON      EQU 00001100B
CURSOR      EQU 00011100B
FUNCSET     EQU 00111000B
;
;DEVICE ADDRESS [LCD]
RS          BIT P2.0    ;LCD
E           BIT P2.2    ;LCD

ON_OFF1      BIT P3.2
ON_OFF2      BIT P3.3

monitor1 BIT P3.0
monitor2 BIT P3.1

monitor1_MATI BIT P3.4
monitor2_MATI BIT P3.5

DTK         EQU 31H
MNT         EQU 32H
JAM         EQU 33H

;FLAGDTK      EQU PSW.5
STATDTK     EQU 0
DTK1        EQU 34H
MNT1         EQU 35H
JAM1        EQU 36H

DTKA        EQU 37H
MNTA         EQU 38H
JAMA        EQU 39H

DTKB        EQU 40H
MNTB         EQU 41H
JAMB        EQU 42H

DATAKEY3    EQU 44H
DATAKEY4    EQU 45H
DATAKEY5    EQU 46H
DATAKEY6    EQU 47H
DATAKEY7    EQU 48H
DATAKEY8    EQU 49H
DATAKEY9    EQU 57H
DATAKEY10   EQU 58H
DATAKEY11   EQU 52H
DATAKEY12   EQU 53H
LOKASI      EQU 54H
DATAQ       EQU 43H
HARI EQU 55H
HARI1   EQU 56H

;
WMCON     DATA     96H
EEMEN     EQU      00001000B
EEMWE     EQU      00010000B
WDTRST    EQU      00000010B

baris1          bit      P1.0     ; atas (1,2,3)
baris2          bit      P1.1
baris3          bit      P1.2
baris4          bit      P1.3
kolom1          bit      P1.4     ; kiri (1,4,7,redial)
kolom2          bit      P1.5
kolom3          bit      P1.6
;
keyport         equ      P1
keydata         equ      50h
```

```
keybounc        equ     51H
        JMP     MULAI


ISR_INTO:
        ORG     3H
        RETI
ISR_TIMER0:
        ORG     0BH
        CLR     TR0
        MOV     TL0,#0ECH
;RELOAD TIMER1
        MOV     TH0,#0F0H

        LCALL   HITUNG_WAKTU
        LCALL   DSPJAM
        RETI
ISR_TIMER1:
        ORG     1BH
        SETB    TR0
        CLR     TR0
        RETI

MULAI:
        CLR     ON_OFF1
        CLR     ON_OFF2
        ;MOV    WMCON,#96H
        LCALL   INIT_LCD
        LCALL   KEYPAD
        MOV     DATAKEY3,#0DFH
        MOV     DATAQ,#0

INISIALISASI:

;*************************
;*  INISIALISASI LCD     *
;*************************
DELAY_INIT_LCD:
        MOV R6,#20H

DLY_LCD_LP:

        MOV     R7,#0
        DJNZ    R7,$
        DJNZ    R6,DLY_LCD_LP
        RET

INIT_LCD:

        SETB RS
        CLR E
        MOV A,#DISPCLR
        LCALL CONTROLOUT
        LCALL DELAY_INIT_LCD
        MOV     A,#FUNCSET
        LCALL   CONTROLOUT
        MOV     A,#DISPON
        LCALL   CONTROLOUT
        MOV     A,#ENTRMOD
        LCALL   CONTROLOUT
        MOV     DPTR,#NAMA
        LCALL   PRINTSTRING1
        MOV     DPTR,#SEKOLAH
        LCALL   PRINTSTRING2
        MOV     R7,#100
LOOP2:  MOV     R6,#100
LOOP1:  MOV     R5,#100
        DJNZ    R5,$
        DJNZ    R6,LOOP1
        DJNZ    R7,LOOP2
```

```
        MOV     R7,#100
LOOP4:  MOV     R6,#100
LOOP3:  MOV     R5,#100
        DJNZ    R5,$
        DJNZ    R6,LOOP3
        DJNZ    R7,LOOP4

        MOV     DPTR,#PILIH6
        LCALL   PRINTSTRING1
        MOV     DPTR,#PILIH7
        LCALL   PRINTSTRING2

        MOV      keybounc,#50
KEY12A:
        SETB     kolom3
        clr      kolom1
key3A:  JB baris4,key4A
        DJNZ     keybounc,key3A
        JMP      ULANHG
looop:
        MOV     A,WMCON
        ANL     A,#WDTRST
        JZ      looop
        RET
key4A:
        SETB     kolom1
        CLR      kolom3
key11A:
        JB       baris4,key12A
        DJNZ     keybounc,key11A
        JMP      ULANHGG

eroor1:
        JMP     eroor

ULANHG:
        ORL    WMCON,#EEMEN
        ORL    WMCON,#EEMWE
        MOV    DPTR,#001H
        MOV    A,#00H
        MOVX   @DPTR,A
        CALL   LOOOP
        MOVX   A,@DPTR
        CJNE   A,#00H,eroor1
        MOV    HARI,A
        XRL    WMCON,#EEMWE
        XRL    WMCON,#EEMEN

        ORL    WMCON,#EEMEN
        ORL    WMCON,#EEMWE
        MOV    DPTR,#002H
        MOV    A,#00H
        MOVX   @DPTR,A
        CALL      LOOOP
        MOVX      A,@DPTR
        CJNE      A,#00H,eroor
        MOV       JAMA,A
        XRL       WMCON,#EEMWE
        XRL       WMCON,#EEMEN

        ORL    WMCON,#EEMEN
        ORL    WMCON,#EEMWE
        MOV    DPTR,#003H
        MOV    A,#00H
        MOVX   @DPTR,A
        CALL      LOOOP
        MOVX      A,@DPTR
        CJNE      A,#00H,eroor
        MOV       MNTA,A
        XRL       WMCON,#EEMWE
        XRL       WMCON,#EEMEN
```

```
          ORL     WMCON,#EEMEN
          ORL     WMCON,#EEMWE
          MOV     DPTR,#004H
          MOV     A,#00H
          MOVX    @DPTR,A
          CALL      LOOOP
          MOVX      A,@DPTR
          CJNE      A,#00H,eroor
          MOV       HARI1,A
          XRL       WMCON,#EEMWE
          XRL       WMCON,#EEMEN

          ORL     WMCON,#EEMEN
          ORL     WMCON,#EEMWE
          MOV     DPTR,#005H
          MOV     A,#00H
          MOVX    @DPTR,A
          CALL      LOOOP
          MOVX      A,@DPTR
          CJNE      A,#00H,eroor
          MOV       JAMB,A
          XRL       WMCON,#EEMWE
          XRL       WMCON,#EEMEN

          ORL     WMCON,#EEMEN
          ORL     WMCON,#EEMWE
          MOV     DPTR,#006H
          MOV     A,#00H
          MOVX    @DPTR,A
          CALL      LOOOP
          MOVX      A,@DPTR
          CJNE      A,#00H,eroor
          MOV       MNTB,A
          XRL       WMCON,#EEMWE
          XRL       WMCON,#EEMEN
          JMP       ULANH
eroor:
          MOV       HARI,#3FH
          MOV       DTKA,#3FH
          MOV       MNTA,#3FH
          MOV       JAMA,#3FH
          MOV       DTKB,#3FH
          MOV       MNTB,#3FH
          MOV       JAMB,#3FH
          JMP       ULANH

ULANHGG:
          ORL     WMCON,#EEMEN
          MOV     DPTR,#001H
          MOVX    A,@DPTR
          MOV     HARI,A
          XRL     WMCON,#EEMEN

          ORL     WMCON,#EEMEN
          MOV     DPTR,#002H
          MOVX    A,@DPTR
          MOV     JAMA,A
          XRL     WMCON,#EEMEN

          ORL     WMCON,#EEMEN
          MOV     DPTR,#003H
          MOVX    A,@DPTR
          MOV     MNTA,A
          XRL     WMCON,#EEMEN

          ORL     WMCON,#EEMEN
          MOV     DPTR,#004H
          MOVX    A,@DPTR
          MOV     HARI1,A
          XRL     WMCON,#EEMEN
```

```
        ORL     WMCON,#EEMEN
        MOV     DPTR,#005H
        MOVX    A,@DPTR
        MOV     JAMB,A
        XRL     WMCON,#EEMEN

        ORL     WMCON,#EEMEN
        MOV     DPTR,#006H
        MOVX    A,@DPTR
        MOV     MNTB,A
        XRL     WMCON,#EEMEN


ULANH:
        CALL ROLL
        MOV        DPTR,#PILIH4
        LCALL      PRINTSTRING1
        MOV        DPTR,#PILIH5
        LCALL      PRINTSTRING2



        MOV DATAKEY4,#0
        MOV DATAKEY5,#0
        MOV DATAKEY6,#0
        MOV DATAKEY7,#0
        MOV DATAKEY8,#0
        MOV DATAKEY9,#0
        MOV DATAKEY10,#0
        MOV DATAKEY11,#0
        MOV DATAKEY12,#0
        MOV LOKASI,#0

KEYPAD:

KEYLOOP:

ulang:  call    Keypad3x4
        mov     A,keydata
        cjne    A,#0FFH,tampil
        jmp     ulang

;====================================
; routine u/ baca keypad 3x4
; output pd keydata(0-9,E=redial,F=#)
;====================================
Keypad3x4:
        mov     keybounc,#50
        mov     keyport,#0FFh
        clr     kolom1
ul1:    jb      baris1,key1
        djnz    keybounc,ul1
        mov     keydata,#1
        ret
key1:   jb      baris2,key2
        djnz    keybounc,key1
        mov     keydata,#4
        ret
key2:   jb      baris3,key3
        djnz    keybounc,key2
        mov     keydata,#7
        ret
tampil:
        ljmp    tampil2

key3:   jb      baris4,key4
        djnz    keybounc,key3
        JMP     ULANH
        ret
key4:   setb    kolom1
```

```
         clr     kolom2
         jb      baris1,key5
         djnz    keybounc,key4
         mov     keydata,#2
         ret
key5:    jb      baris2,key6
         djnz    keybounc,key5
         mov     keydata,#5
         ret
key6:    jb      baris3,key7
         djnz    keybounc,key6
         mov     keydata,#8
         ret
key7:    jb      baris4,key8
         djnz    keybounc,key7
         mov     keydata,#0
         ret
key8:    setb    kolom2
         clr     kolom3
         jb      baris1,key9
         djnz    keybounc,key8
         mov     keydata,#3
         ret
key9:    jb      baris2,key10
         djnz    keybounc,key9
         mov     keydata,#6
         ret
key10:   jb      baris3,key11
         djnz    keybounc,key10
         mov     keydata,#9
         ret

tampil2:
         ljmp    tampil1

key11:   jb      baris4,key12
         djnz    keybounc,key11
         mov     keydata,#0Fh
         ret
key12:   mov     keydata,#0FFh
         ret

TAMPIL1:
         MOV     A,KEYDATA
         ANL     A,#0FH
         MOV     B,A
         CLR     C
         SUBB    A,#10
         JNC     LOOPKEY
         MOV     A,LOKASI
         INC     A
         MOV     LOKASI,A
PIL0:
         CJNE    A,#00000001B,PILL1
         MOV     DATAKEY12,B
         MOV A,#12
         LCALL POSISI1
         MOV A,DATAKEY12
         JMP     TAMPILL
PILL1:
         CJNE    A,#00000010B,PIL2
         MOV     DATAKEY11,B
         MOV A,#13
         LCALL POSISI1
         MOV A,DATAKEY11
         JMP     TAMPILL
PIL2:
         CJNE    A,#00000011B,PIL3
         MOV     DATAKEY10,B
         MOV A,#12
         LCALL POSISI2
```

```
        MOV A,DATAKEY10
        JMP     TAMPILL
PIL3:
        CJNE    A,#00000100B,PIL0
        MOV     DATAKEY9,B
        MOV A,#13
        LCALL POSISI2
        MOV A,DATAKEY9
        JMP     TAMPILL

;LOOPKEY:
;       LJMP    LOOPKEY1


PIL8:
        LJMP    PIL0
        RET
TAMPILL:
        ORL     A,#30H
        LCALL   DATAOUT
        CALL    roll
        JMP     KEYLOOP
        RET
roll:
        MOV     R7,#50
LOOPAC: MOV     R6,#50
LOOPAD: MOV     R5,#100
        DJNZ    R5,$
        DJNZ    R6,LOOPAD
        DJNZ    R7,LOOPAC
        RET
loopkey:

        MOV     DPTR,#PILIH4
        LCALL   PRINTSTRING1
        MOV     DPTR,#PILIH5
        LCALL   PRINTSTRING2

        MOV A,DATAKEY12
        SWAP A
        ORL A,DATAKEY11
        MOV DATAKEY11,A
        CLR A
        MOV A,DATAKEY10
        SWAP A
        ORL A,DATAKEY9
        MOV DATAKEY9,A

        MOV A,#12
        LCALL   POSISI1
        MOV     A,DATAKEY11
        SWAP    A
        ANL     A,#0FH
        ORL     A,#030H
        LCALL   DATAOUT
        MOV     A,DATAKEY11
        ANL     A,#0FH
        ORL     A,#030H
        LCALL   DATAOUT

        MOV A,#12
        LCALL   POSISI2
        MOV     A,DATAKEY9
        SWAP    A
        ANL     A,#0FH
        ORL     A,#030H
        LCALL   DATAOUT
        MOV     A,DATAKEY9
        ANL     A,#0FH
        ORL     A,#030H
        LCALL   DATAOUT
```

```
        MOV     DTKA,#0
        MOV     DTKB,#0
        MOV     DTK,#0
        MOV     MNT,#0
        MOV     JAM,#0
        MOV     DTK1,#0
        MOV     MNT1,#0
        MOV     JAM1,#0
        CLR     P2.4
        CLR     P2.5
        CLR     P2.6
        CLR     P2.7

        MOV     DATAKEY3,#0DFH
ENTER1:




;***************************
;*  INISIALISASI TIMER     *
;*  OUTO RELOAD UNTUK JAM  *
;***************************
WAKTU:  MOV     TMOD,#00100001B
        ;T1 MODE 2, TO MODE 3
        MOV     TH1,#25H
        MOV     TL1,TH1
        MOV     TL0,#0ECH
        MOV     TH0,#0F0H
        MOV     IE,#10001010B
        ;ENEBLE ALL INTRAF: TIMER0&1
        SETB    IP.1
        SETB    TR1     ;T1 RUN
        ; SEMUA BAFER WAKTU DIBUAT 0
        CLR     P2.5
        CLR     P2.4
TIMERON:
        CLR     P2.5
        MOV A,#1
        LCALL POSISI2
        MOV     A,#4DH
        LCALL   DATAOUT
layar3:
        JNB     P3.4,layar1
        SETB    P2.4
        JB      P3.0,layar2
        MOV     DTK,#0
        MOV     MNT,#0
        MOV     JAM,#0
        SETB    ON_OFF1
        JMP     layar2

layar1:
        CLR     P2.4
        MOV A,#1
        LCALL POSISI1
        MOV     A,#4DH
        LCALL   DATAOUT
layar2:
        JNB     P3.5,timeron
        SETB    P2.5
        JB      P3.1,layar3
        MOV     DTK1,#0
        MOV     MNT1,#0
        MOV     JAM1,#0
        SETB    ON_OFF2
        JMP     layar3
```

```
HITUNG_WAKTU:
        PUSH    ACC
        JNB   P2.4,RETURN_HW2
        JNB     ON_OFF1,RETURN_HW
        MOV A,#1
        LCALL POSISI1
        MOV     A,#4EH
        LCALL   DATAOUT
;*************************************************
;*************************************************
        CLR     C
        MOV     A,DTK    ;INC DTK
        INC     A
        DA      A
        MOV     DTK,A
        CJNE    A,#60H,RETURN_HW2
        MOV     DTK,#0

        MOV     A,MNT    ;INC MNT
        INC     A
        DA      A
        MOV     MNT,A
        CJNE    A,#99H,RETURN_HW2
        MOV     MNT,#0
        JMP     RETURN_HW2

RETURN_HW:

        CLR     C
        MOV     A,DTKA   ;INC DTK
        INC     A
        DA      A
        MOV     DTKA,A
        CJNE    A,#60H,RETURN_HW2
        MOV     DTKA,#0

        MOV     A,MNTA   ;INC MNT
        INC     A
        DA      A
        MOV     MNTA,A
        CJNE    A,#60H,RETURN_HW2
        MOV     MNTA,#0

        MOV     A,JAMA   ;INC JAM
        INC     A
        DA      A
        MOV     JAMA,A
        CJNE    A,#24H,RETURN_HW2
        MOV     JAMA,#0

        MOV     A,HARI   ;INC JAM
        INC     A
        DA      A
        MOV     HARI,A
        CJNE    A,#31H,RETURN_HW2
        MOV     HARI,#0


RETURN_HW2:
        JNB   P2.5,RETURN_HW1
        JNB     ON_OFF2,RETURN_HW3
        MOV A,#1
        LCALL POSISI2
        MOV     A,#4EH
        LCALL   DATAOUT
        CLR     C
        MOV     A,DTK1   ;INC DTK
        INC     A
        DA      A
        MOV     DTK1,A
```

```
DSPJAM:
        ;FORMAT DATA KE ASCII
        ;UNTUK MENAMPILKAN WAKTU
        ;=> SYARAT BITSTART = 1

        ORL     WMCON,#EEMEN
        ORL     WMCON,#EEMWE
        MOV     DPTR,#001H
        MOV     A,HARI
        MOVX    @DPTR,A
        ACALL    LOOOP
        MOVX    A,@DPTR
        ;CJNE    A,HARI,eroor2
        MOV     HARI,A
        XRL     WMCON,#EEMWE
        XRL     WMCON,#EEMEN

        ORL     WMCON,#EEMEN
        ORL     WMCON,#EEMWE
        MOV     DPTR,#002H
        MOV     A,JAMA
        MOVX    @DPTR,A
        ACALL      LOOOP
        MOVX       A,@DPTR
        ;CJNE      A,JAMA,eroor2
        MOV        JAMA,A
        XRL        WMCON,#EEMWE
        XRL        WMCON,#EEMEN

        ORL     WMCON,#EEMEN
        ORL     WMCON,#EEMWE
        MOV     DPTR,#003H
        MOV     A,MNTA
        MOVX    @DPTR,A
        ACALL      LOOOP
        MOVX       A,@DPTR
        ;CJNE      A,MNTA,eroor2
        MOV        MNTA,A
        XRL        WMCON,#EEMWE
        XRL        WMCON,#EEMEN

        ORL     WMCON,#EEMEN
        ORL     WMCON,#EEMWE
        MOV     DPTR,#004H
        MOV     A,HARI1
        MOVX    @DPTR,A
        ACALL      LOOOP
        MOVX       A,@DPTR
        ;CJNE      A,HARI1,eroor2
        MOV        HARI1,A
        XRL        WMCON,#EEMWE
        XRL        WMCON,#EEMEN

        ORL     WMCON,#EEMEN
        ORL     WMCON,#EEMWE
        MOV     DPTR,#005H
        MOV     A,JAMB
        MOVX    @DPTR,A
        ACALL      LOOOP
        MOVX       A,@DPTR
        ;CJNE      A,JAMB,eroor2
        MOV        JAMB,A
        XRL        WMCON,#EEMWE
        XRL        WMCON,#EEMEN

        ORL     WMCON,#EEMEN
        ORL     WMCON,#EEMWE
        MOV     DPTR,#006H
        MOV     A,MNTB
        MOVX    @DPTR,A
        ACALL      LOOOP
```

```
        CJNE    A,#60H,RETURN_HW1
        MOV     DTK1,#0

        MOV     A,MNT1;INC MNT
        INC     A
        DA      A
        MOV     MNT1,A
        CJNE    A,#99H,RETURN_HW1
        MOV     MNT1,#0
        JMP     RETURN_HW1

RETURN_HW3:
        CLR     C
        MOV     A,DTKB   ;INC DTK
        INC     A
        DA      A
        MOV     DTKB,A
        CJNE    A,#60H,RETURN_HW1
        MOV     DTKB,#0

        MOV     A,MNTB   ;INC MNT
        INC     A
        DA      A
        MOV     MNTB,A
        CJNE    A,#60H,RETURN_HW1
        MOV     MNTB,#0

        MOV     A,JAMB   ;INC JAM
        INC     A
        DA      A
        MOV     JAMB,A
        CJNE    A,#24H,RETURN_HW1
        MOV     JAMB,#0

        MOV     A,HARI1 ;INC JAM
        INC     A
        DA      A
        MOV     HARI1,A
        CJNE    A,#31H,RETURN_HW1
        MOV     HARI1,#0


RETURN_HW1:
        POP     ACC

        MOV A,MNT
        XRL A,DATAKEY11
        JZ EQUAL
HHH:
        MOV A,MNT1
        XRL A,DATAKEY9
        JZ EQUAL1
        RET

EQUAL:  clr ON_OFF1
        MOV A,#1
        LCALL POSISI1
        MOV     A,#53H
        LCALL   DATAOUT
        JMP HHH

EQUAL1: clr ON_OFF2
        MOV A,#1
        LCALL POSISI2
        MOV     A,#53H
        LCALL   DATAOUT
        RET


;TAMPILKAN WAKTU KELCD
```

```
        MOVX    A,@DPTR
        ;CJNE   A,MNTB,eroor2
        MOV     MNTB,A
        XRL     WMCON,#EEMWE
        XRL     WMCON,#EEMEN
        ;JMP    BENAAAR
;EROOR2:
        ;MOV    HARI,#3FH
        ;MOV    DTKA,#3FH
        ;;MOV   MNTA,#3FH
        ;MOV    JAMA,#3FH
        ;MOV    DTKB,#3FH
        ;MOV    MNTB,#3FH
        ;MOV    JAMB,#3FH
;BENAAAR:
        PUSH    ACC

        MOV A,#2
        LCALL   POSISI1
        MOV     A,#'|'
        LCALL   DATAOUT

        MOV     A,HARI
        SWAP    A
        ANL     A,#0FH
        ORL     A,#030H
        LCALL   DATAOUT

        MOV     A,HARI
        ANL     A,#0FH
        ORL     A,#030H
        LCALL   DATAOUT

        MOV     A,#'/'
        LCALL   DATAOUT

        MOV     A,JAMA
        SWAP    A
        ANL     A,#0FH
        ORL     A,#030H
        LCALL   DATAOUT

        MOV     A,JAMA
        ANL     A,#0FH
        ORL     A,#030H
        LCALL   DATAOUT


        MOV     A,DATAKEY3
        LCALL   DATAOUT

        MOV     A,MNTA
        SWAP    A
        ANL     A,#0FH
        ORL     A,#030H
        LCALL   DATAOUT

        MOV     A,MNTA
        ANL     A,#0FH
        ORL     A,#030H
        LCALL   DATAOUT

        MOV     A,#'|'
        LCALL   DATAOUT


        MOV A,#14
        LCALL   POSISI1

        MOV     A,DATAKEY3
```

```
LCALL    DATAOUT

MOV      A,MNT
SWAP     A
ANL      A,#0FH
ORL      A,#030H
LCALL    DATAOUT


MOV      A,MNT
ANL      A,#0FH
ORL      A,#030H
LCALL    DATAOUT


MOV A,#2
LCALL    POSISI2

MOV      A,#'|'
LCALL    DATAOUT

MOV      A,HARI1
SWAP     A
ANL      A,#0FH
ORL      A,#030H
LCALL    DATAOUT

MOV      A,HARI1
ANL      A,#0FH
ORL      A,#030H
LCALL    DATAOUT

MOV      A,#'/'
LCALL    DATAOUT

MOV      A,JAMB
SWAP     A
ANL      A,#0FH
ORL      A,#030H
LCALL    DATAOUT

MOV      A,JAMB
ANL      A,#0FH
ORL      A,#030H
LCALL    DATAOUT

MOV      A,DATAKEY3
LCALL    DATAOUT

MOV      A,MNTB
SWAP     A
ANL      A,#0FH
ORL      A,#030H
LCALL    DATAOUT

MOV      A,MNTB
ANL      A,#0FH
ORL      A,#030H
LCALL    DATAOUT

MOV      A,#'|'
LCALL    DATAOUT


MOV A,#14
LCALL    POSISI2
MOV      A,DATAKEY3
LCALL    DATAOUT
MOV      A,MNT1
SWAP     A
```

```
        ANL     A,#0FH
        ORL     A,#030H
        LCALL   DATAOUT

        MOV     A,MNT1
        ANL     A,#0FH
        ORL     A,#030H
        LCALL   DATAOUT

        MOV     A,DATAKEY3
        CPL     A
        MOV     DATAKEY3,A


        POP     ACC
        RET

;*********************************
;* KUMPULAN RUTIN PELAYANAN LCD *
;*********************************

POSISI2_1:
        MOV     A,#1
POSISI2:
        ADD     A,#11000000B
        SJMP    POSISI_SUB

POSISI1_1:
        MOV     A,#1
POSISI1:
        ADD     A,#10000000B
POSISI_SUB:
        DEC     A
        LCALL   CONTROLOUT
        RET

PRINTSTRING2:
        LCALL   POSISI2_1
        SJMP    PRINTSTRING

PRINTSTRING1:
        LCALL   POSISI1_1

PRINTSTRING:
        SJMP    OUTSTRING
PRINTSTRINGLOOP:
        LCALL   DATAOUT
        INC     DPTR

OUTSTRING:
        CLR     A
        MOVC    A,@A+DPTR
        JNZ     PRINTSTRINGLOOP
        RET

CONTROLOUT:
        CPL RS
        CPL E
        MOV P0,A
        CPL E
        CPL RS
        MOV P0,#0FFH
        SJMP LCD_OUT

DATAOUT:
        ;CPL RS
        CPL E
        MOV P0,A
        CPL E
        ;CPL RS
```

```
LCD_OUT:
        MOVX    @DPTR,A

DELAY_LCD:
        PUSH ACC
        MOV     A,#250
        DJNZ    ACC,$
        POP ACC
        RET


NAMA:         DB ' VICO ROMANDIKA ',0
SEKOLAH:      DB 'NIM : 02.17.079 ',0
SETWAKTU:     DB 'MASUKKAN WAKTU  ',0
PILIH4      : DB ' |00/00:00|  :  ',0
PILIH5  :     DB ' |00/00:00|  :  ',0
PILIH6      : DB 'Prs * Clr Memori',0
PILIH7  :     DB 'Prs # Aml Memori',0


        END
```

ures

- patible with MCS®51 Products
- ytes of In-System Reprogrammable Downloadable Flash Memory
- SPI Serial Interface for Program Downloading
- Endurance: 1,000 Write/Erase Cycles
- ytes EEPROM
- Endurance: 100,000 Write/Erase Cycles
- 6V Operating Range
- Static Operation: 0 Hz to 24 MHz
- -level Program Memory Lock
- 8-bit Internal RAM
- ogrammable I/O Lines
- 16-bit Timer/Counters
- Interrupt Sources
- ammable UART Serial Channel
- erial Interface
- power Idle and Power-down Modes
- upt Recovery from Power-down
- rammable Watchdog Timer
- Data Pointer
- r-off Flag

:ription

89S8252 is a low-power, high-performance CMOS 8-bit microcontroller with 8K f downloadable Flash programmable and erasable read-only memory and 2K f EEPROM. The device is manufactured using Atmel's high-density nonvolatile y technology and is compatible with the industry-standard 80C51 instruction l pinout. The on-chip downloadable Flash allows the program memory to be ammed In-System through an SPI serial interface or by a conventional nonvol-emory programmer. By combining a versatile 8-bit CPU with downloadable n a monolithic chip, the Atmel AT89S8252 is a powerful microcontroller, which s a highly-flexible and cost-effective solution to many embedded control tions.

89S8252 provides the following standard features: 8K bytes of downloadable 2K bytes of EEPROM, 256 bytes of RAM, 32 I/O lines, programmable watchdog wo data pointers, three 16-bit timer/counters, a six-vector two-level interrupt ture, a full duplex serial port, on-chip oscillator, and clock circuitry. In addition, 9S8252 is designed with static logic for operation down to zero frequency and s two software selectable power saving modes. The Idle Mode stops the CPU llowing the RAM, timer/counters, serial port, and interrupt system to continue ning. The Power-down mode saves the RAM contents but freezes the oscillator, g all other chip functions until the next external interrupt or hardware reset.

wnloadable Flash can be changed a single byte at a time and is accessible the SPI serial interface. Holding RESET active forces the SPI bus into a serial mming interface and allows the program memory to be written to or read from ock bits have been activated.

8-bit Microcontroller with 8K Bytes Flash

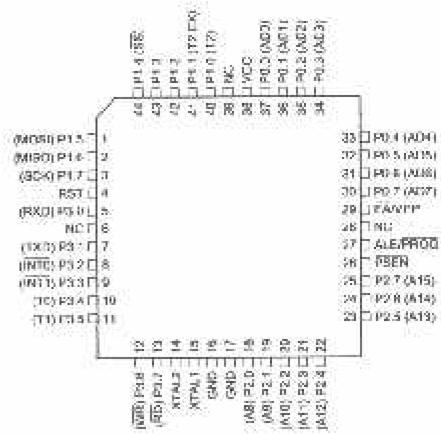
AT89S8252

0401F–MICRO–11/03

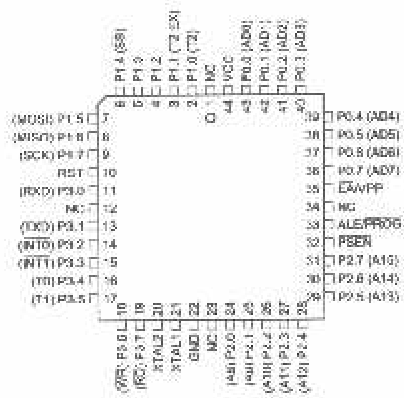
Configurations

PDIP

TQFP



PLCC



escription

Supply voltage.

Ground.

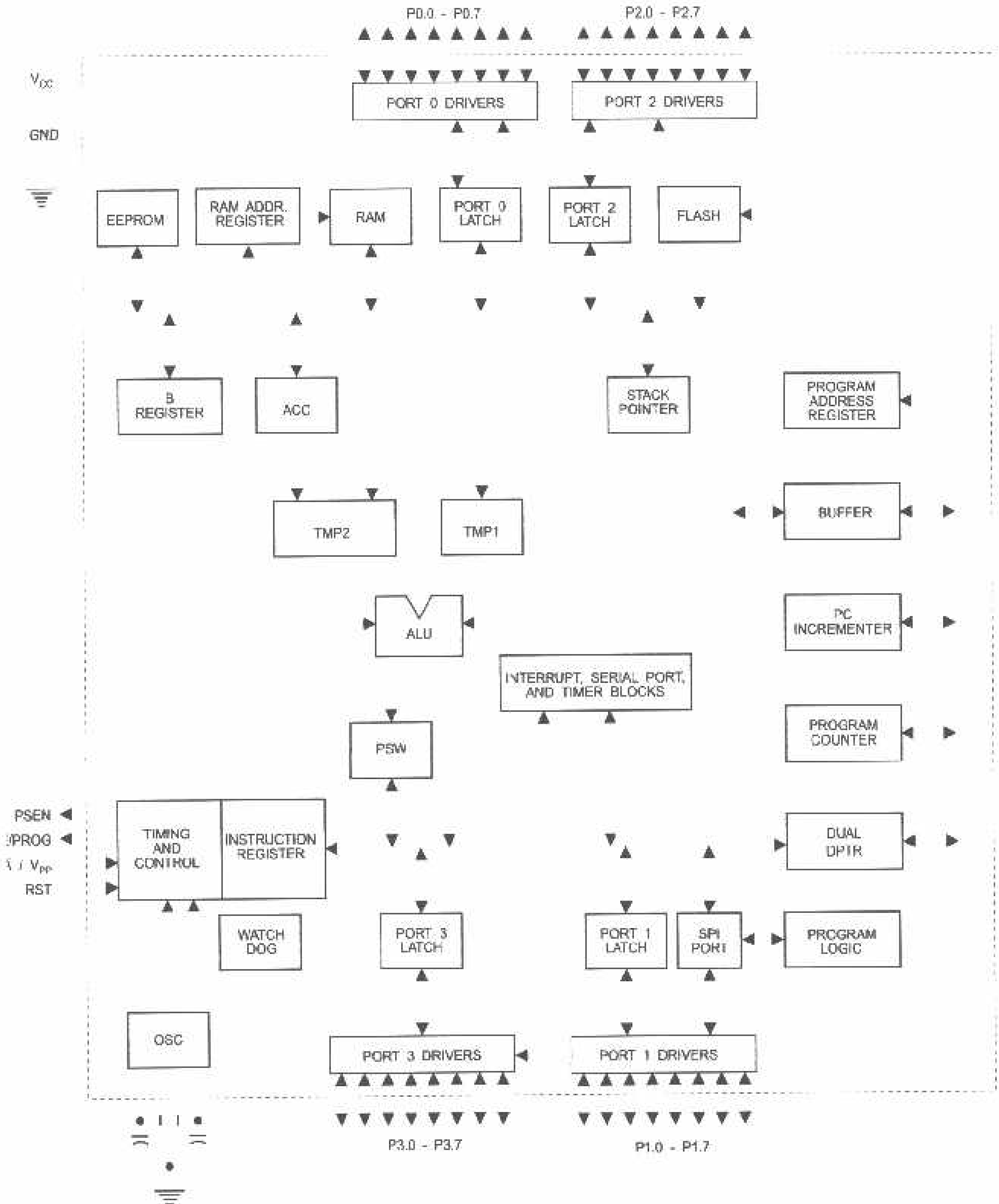
Port 0 is an 8-bit open drain bi-didirectional I/O port. As an output port, each pin can sink eight TTL inputs. When 1s are written to port 0 pins, the pins can be used as high-impedance inputs.

Port 0 can also be configured to be the multiplexed low-order address/data bus during accesses to external program and data memory. In this mode, P0 has internal pull-ups.

Port 0 also receives the code bytes during Flash programming and outputs the code bytes during program verification. External pull-ups are required during program verification.

Port 1 is an 8-bit bi-directional I/O port with internal pull-ups. The Port 1 output buffers can sink/source four TTL inputs. When 1s are written to Port 1 pins, they are pulled high by the internal pull-ups and can be used as inputs. As inputs, Port 1 pins that are externally being pulled low will source current (I_{IL}) because of the internal pull-ups.

k Diagram


P0.0 - P0.7
P2.0 - P2.7
VCC
GND
PORT 0 DRIVERS
PORT 2 DRIVERS
EEPROM
RAM ADDR. REGISTER
RAM
PORT 0 LATCH
PORT 2 LATCH
FLASH
B REGISTER
ACC
STACK POINTER
PROGRAM ADDRESS REGISTER
TMP2
TMP1
BUFFER
ALU
PC INCREMENTER
INTERRUPT, SERIAL PORT, AND TIMER BLOCKS
PROGRAM COUNTER
PSW
PSEN
TIMING AND CONTROL
INSTRUCTION REGISTER
DUAL DPTR
RST
WATCH DOG
PORT 3 LATCH
PORT 1 LATCH
SPI PORT
PROGRAM LOGIC
OSC
PORT 3 DRIVERS
PORT 1 DRIVERS
P3.0 - P3.7
P1.0 - P1.7

Some Port 1 pins provide additional functions. P1.0 and P1.1 can be configured to be the timer/counter 2 external count input (P1.0/T2) and the timer/counter 2 trigger input (P1.1/T2EX), respectively.

Furthermore, P1.4, P1.5, P1.6, and P1.7 can be configured as the SPI slave port select, data input/output and shift clock input/output pins as shown in the following table.

Port Pin	Alternate Functions
P1.0	T2 (external count input to Timer/Counter 2), clock-out
P1.1	T2EX (Timer/Counter 2 capture/reload trigger and direction control)
P1.4	$\overline{SS}$ (Slave port select input)
P1.5	MOSI (Master data output, slave data input pin for SPI channel)
P1.6	MISO (Master data input, slave data output pin for SPI channel)
P1.7	SCK (Master clock output, slave clock input pin for SPI channel)

Port 1 also receives the low-order address bytes during Flash programming and verification.

Port 2 is an 8-bit bi-directional I/O port with internal pull-ups. The Port 2 output buffers can sink/source four TTL inputs. When 1s are written to Port 2 pins, they are pulled high by the internal pull-ups and can be used as inputs. As inputs, Port 2 pins that are externally being pulled low will source current (I_{IL}) because of the internal pull-ups.

Port 2 emits the high-order address byte during fetches from external program memory and during accesses to external data memory that use 16-bit addresses (MOVX @ DPTR). In this application, Port 2 uses strong internal pull-ups when emitting 1s. During accesses to external data memory that use 8-bit addresses (MOVX @ RI), Port 2 emits the contents of the P2 Special Function Register.

Port 2 also receives the high-order address bits and some control signals during Flash programming and verification.

Port 3 is an 8-bit bi-directional I/O port with internal pull-ups. The Port 3 output buffers can sink/source four TTL inputs. When 1s are written to Port 3 pins, they are pulled high by the internal pull-ups and can be used as inputs. As inputs, Port 3 pins that are externally being pulled low will source current (I_{IL}) because of the pull-ups.

Port 3 receives some control signals for Flash programming and verification.

Port 3 also serves the functions of various special features of the AT89S8252, as shown in the following table.

Port Pin	Alternate Functions
P3.0	RXD (serial input port)
P3.1	TXD (serial output port)
P3.2	$\overline{\text{INT0}}$ (external interrupt 0)
P3.3	$\overline{\text{INT1}}$ (external interrupt 1)
P3.4	T0 (timer 0 external input)
P3.5	T1 (timer 1 external input)
P3.6	$\overline{\text{WR}}$ (external data memory write strobe)
P3.7	$\overline{\text{RD}}$ (external data memory read strobe)

Reset input. A high on this pin for two machine cycles while the oscillator is running resets the device.

$\overline{\text{PROG}}$

Address Latch Enable is an output pulse for latching the low byte of the address during accesses to external memory. This pin is also the program pulse input ($\overline{\text{PROG}}$) during Flash programming.

In normal operation, ALE is emitted at a constant rate of 1/6 the oscillator frequency and may be used for external timing or clocking purposes. Note, however, that one ALE pulse is skipped during each access to external data memory.

If desired, ALE operation can be disabled by setting bit 0 of SFR location 8EH. With the bit set, ALE is active only during a MOVX or MOVC instruction. Otherwise, the pin is weakly pulled high. Setting the ALE-disable bit has no effect if the microcontroller is in external execution mode.

Program Store Enable is the read strobe to external program memory.

When the AT89S8252 is executing code from external program memory, $\overline{\text{PSEN}}$ is activated twice each machine cycle, except that two $\overline{\text{PSEN}}$ activations are skipped during each access to external data memory.

P

External Access Enable. $\overline{\text{EA}}$ must be strapped to GND in order to enable the device to fetch code from external program memory locations starting at 0000H up to FFFFH. Note, however, that if lock bit 1 is programmed, $\overline{\text{EA}}$ will be internally latched on reset.

$\overline{\text{EA}}$ should be strapped to V_{CC} for internal program executions. This pin also receives the 12-volt programming enable voltage (V_{PP}) during Flash programming when 12-volt programming is selected.

Input to the inverting oscillator amplifier and input to the internal clock operating circuit.

Output from the inverting oscillator amplifier.

ial Function sters

A map of the on-chip memory area called the Special Function Register (SFR) space is shown in Table 1.

Note that not all of the addresses are occupied, and unoccupied addresses may not be implemented on the chip. Read accesses to these addresses will in general return random data, and write accesses will have an indeterminate effect.

User software should not write 1s to these unlisted locations, since they may be used in future products to invoke new features. In that case, the reset or inactive values of the new bits will always be 0.

Timer 2 Registers Control and status bits are contained in registers T2CON (shown in Table 2) and T2MOD (shown in Table 9) for Timer 2. The register pair (RCAP2H, RCAP2L) are the Capture/Reload registers for Timer 2 in 16-bit capture mode or 16-bit auto-reload mode.

. AT89S8252 SFR Map and Reset Values

								0FFH
B 00000000								0F7H
								0EFH
ACC 00000000								0E7H
								0DF H
PSW 00000000					SPCR 000001XX			0D7H
T2CON 00000000	T2MOD XXXXXX00	RCAP2L 00000000	RCAP2H 00000000	TL2 00000000	TH2 00000000			0CF H
								0C7H
IP XX000000								0BFH
P3 11111111								0B7H
IE 0X000000		SPSR 00XXXXXX						0AFH
P2 11111111								0A7H
SCON 00000000	SBUF XXXXXXXX							9FH
P1 11111111						WMCON 00000010		97H
TCON 00000000	TMOD 00000000	TL0 00000000	TL1 00000000	TH0 00000000	TH1 00000000			8FH
P0 11111111	SP 00000111	DP0L 00000000	DP0H 00000000	DP1L 00000000	DP1H 00000000	SPDR XXXXXXXX	PCON 0XXX0000	87H

. T2CON – Timer/Counter 2 Control Register

N Address = 0C8H							Reset Value = 0000 0000B
dressable							
TF2	EXF2	RCLK	TCLK	EXEN2	TR2	C/$\overline{T2}$	CP/$\overline{RL2}$
7	6	5	4	3	2	1	0

ol	Function
	Timer 2 overflow flag set by a Timer 2 overflow and must be cleared by software. TF2 will not be set when either RCLK = 1 or TCLK = 1.
	Timer 2 external flag set when either a capture or reload is caused by a negative transition on T2EX and EXEN2 = 1. When Timer 2 interrupt is enabled, EXF2 = 1 will cause the CPU to vector to the Timer 2 interrupt routine. EXF2 must be cleared by software. EXF2 does not cause an interrupt in up/down counter mode (DCEN = 1).
	Receive clock enable. When set, causes the serial port to use Timer 2 overflow pulses for its receive clock in serial port Modes 1 and 3. RCLK = 0 causes Timer 1 overflows to be used for the receive clock.
	Transmit clock enable. When set, causes the serial port to use Timer 2 overflow pulses for its transmit clock in serial port Modes 1 and 3. TCLK = 0 causes Timer 1 overflows to be used for the transmit clock.
2	Timer 2 external enable. When set, allows a capture or reload to occur as a result of a negative transition on T2EX if Timer 2 is not being used to clock the serial port. EXEN2 = 0 causes Timer 2 to ignore events at T2EX.
	Start/Stop control for Timer 2. TR2 = 1 starts the timer.
	Timer or counter select for Timer 2. C/$\overline{T2}$ = 0 for timer function. C/$\overline{T2}$ = 1 for external event counter (falling edge triggered).
2	Capture/Reload select. CP/$\overline{RL2}$ = 1 causes captures to occur on negative transitions at T2EX if EXEN2 = 1. CP/$\overline{RL2}$ = 0 causes automatic reloads to occur when Timer 2 overflows or negative transitions occur at T2EX when EXEN2 = 1. When either RCLK or TCLK = 1, this bit is ignored and the timer is forced to auto-reload on Timer 2 overflow.

dog and Memory Control Register The WMCON register contains control bits for the Watchdog Timer (shown in 3). The EEMEN and EEMWE bits are used to select the 2K bytes on-chip EEPROM, and to enable byte-write. The t selects one of two DPTR registers available.

;. WMCON—Watchdog and Memory Control Register

)N Address = 96H						Reset Value = 0000 0010B	
PS2	PS1	PS0	EEMWE	EEMEN	DPS	WDTRST	WDTEN
7	6	5	4	3	2	1	0

ol	Function
	Prescaler Bits for the Watchdog Timer. When all three bits are set to "0", the watchdog timer has a nominal period of 16 ms. When all three bits are set to "1", the nominal period is 2048 ms.
'E	EEPROM Data Memory Write Enable Bit. Set this bit to "1" before initiating byte write to on-chip EEPROM with the MOVX instruction. User software should set this bit to "0" after EEPROM write is completed.
N	Internal EEPROM Access Enable. When EEMEN = 1, the MOVX instruction with DPTR will access on-chip EEPROM instead of external data memory. When EEMEN = 0, MOVX with DPTR accesses external data memory.
	Data Pointer Register Select. DPS = 0 selects the first bank of Data Pointer Register, DP0, and DPS = 1 selects the second bank, DP1
ST $\overline{SY}$	Watchdog Timer Reset and EEPROM Ready/$\overline{Busy}$ Flag. Each time this bit is set to "1" by user software, a pulse is generated to reset the watchdog timer. The WDTRST bit is then automatically reset to "0" in the next instruction cycle. The WDTRST bit is Write-Only. This bit also serves as the RDY/$\overline{BSY}$ flag in a Read-Only mode during EEPROM write. RDY/$\overline{BSY}$ = 1 means that the EEPROM is ready to be programmed. While programming operations are being executed, the RDY/$\overline{BSY}$ bit equals "0" and is automatically reset to "1" when programming is completed.
N	Watchdog Timer Enable Bit. WDTEN = 1 enables the watchdog timer and WDTEN = 0 disables the watchdog timer.

SPI Registers Control and status bits for the Serial Peripheral Interface are contained in registers SPCR (shown in Table 4) and SPSR (shown in Table 5). The SPI data bits are contained in the SPDR register. Writing the SPI data register during serial data transfer sets the Write Collision bit, WCOL, in the SPSR register. The SPDR is double buffered for writing and the values in SPDR are not changed by Reset.

Interrupt Registers The global interrupt enable bit and the individual interrupt enable bits are in the IE register. In addition, the individual interrupt enable bit for the SPI is in the SPCR register. Two priorities can be set for each of the six interrupt sources in the IP register.

Dual Data Pointer Registers To facilitate accessing both internal EEPROM and external data memory, two banks of 16-bit Data Pointer Registers are provided: DP0 at SFR address locations 82H-83H and DP1 at 84H-85H. Bit DPS = 0 in SFR WMCON selects DP0 and DPS = 1 selects DP1. The user should **ALWAYS** initialize the DPS bit to the appropriate value before accessing the respective Data Pointer Register.

Power Off Flag The Power Off Flag (POF) is located at bit_4 (PCON.4) in the PCON SFR. POF is set to "1" during power up. It can be set and reset under software control and is not affected by RESET.

SPCR – SPI Control Register

Address = D5H — Reset Value = 0000 01XXB

SPIE	SPE	DORD	MSTR	CPOL	CPHA	SPR1	SPR0
7	6	5	4	3	2	1	0

l	Function
	SPI Interrupt Enable. This bit, in conjunction with the ES bit in the IE register, enables SPI interrupts: SPIE = 1 and ES = 1 enable SPI interrupts. SPIE = 0 disables SPI interrupts
	SPI Enable. SPI = 1 enables the SPI channel and connects $\overline{SS}$, MOSI, MISO and SCK to pins P1.4, P1.5, P1.6, and P1.7. SPI = 0 disables the SPI channel.
	Data Order. DORD = 1 selects LSB first data transmission. DORD = 0 selects MSB first data transmission.
	Master/Slave Select. MSTR = 1 selects Master SPI mode. MSTR = 0 selects Slave SPI mode.
	Clock Polarity. When CPOL = 1, SCK is high when idle. When CPOL = 0, SCK of the master device is low when not transmitting. Please refer to figure on SPI Clock Phase and Polarity Control.
	Clock Phase. The CPHA bit together with the CPOL bit controls the clock and data relationship between master and slave. Please refer to figure on SPI Clock Phase and Polarity Control.
	SPI Clock Rate Select. These two bits control the SCK rate of the device configured as master. SPR1 and SPR0 have no effect on the slave. The relationship between SCK and the oscillator frequency, $F_{OSC.}$, is as follows: SPR1 SPR0 SCK = F_{OSC} divided by 0 0 4 0 1 16 1 0 64 1 1 128

SPSR – SPI Status Register

ddress = AAH

Reset Value = 00XX XXXXB

SPIF	WCOL	–	–	–	–	–	–
7	6	5	4	3	2	1	0

l	Function
	SPI Interrupt Flag. When a serial transfer is complete, the SPIF bit is set and an interrupt is generated if SPIE = 1 and ES = 1. The SPIF bit is cleared by reading the SPI status register with SPIF and WCOL bits set, and then reading/writing the SPI data register.
	Write Collision Flag. The WCOL bit is set if the SPI data register is written during a data transfer. During data transfer, the result of reading the SPDR register may be incorrect, and writing to it has no effect. The WCOL bit (and the SPIF bit) are cleared by reading the SPI status register with SPIF and WCOL set, and then accessing the SPI data register.

. SPDR – SPI Data Register

Address = 86H

Reset Value = unchanged

SPD7	SPD6	SPD5	SPD4	SPD3	SPD2	SPD1	SPD0
7	6	5	4	3	2	1	0

Memory – ROM and RAM

The AT89S8252 implements 2K bytes of on-chip EEPROM for data storage and 256 bytes of RAM. The upper 128 bytes of RAM occupy a parallel space to the Special Function Registers. That means the upper 128 bytes have the same addresses as the SFR space but are physically separate from SFR space.

When an instruction accesses an internal location above address 7FH, the address mode used in the instruction specifies whether the CPU accesses the upper 128 bytes of RAM or the SFR space. Instructions that use direct addressing access SFR space.

For example, the following direct addressing instruction accesses the SFR at location 0A0H (which is P2).

```
MOV 0A0H, #data
```

Instructions that use indirect addressing access the upper 128 bytes of RAM. For example, the following indirect addressing instruction, where R0 contains 0A0H, accesses the data byte at address 0A0H, rather than P2 (whose address is 0A0H).

```
MOV @R0, #data
```

Note that stack operations are examples of indirect addressing, so the upper 128 bytes of data RAM are available as stack space.

The on-chip EEPROM data memory is selected by setting the EEMEN bit in the WMCON register at SFR address location 96H. The EEPROM address range is from 000H to 7FFH. The MOVX instructions are used to access the EEPROM. To access off-chip data memory with the MOVX instructions, the EEMEN bit needs to be set to "0".

The EEMWE bit in the WMCON register needs to be set to "1" before any byte location in the EEPROM can be written. User software should reset EEMWE bit to "0" if no further EEPROM write is required. EEPROM write cycles in the serial programming mode are self-timed and typically take 2.5 ms. The progress of EEPROM write can be monitored by reading the RDY/$\overline{\text{BSY}}$ bit (read-only) in SFR WMCON. RDY/$\overline{\text{BSY}}$ = 0 means programming is still in progress and RDY/$\overline{BSY}$ = 1 means EEPROM write cycle is completed and another write cycle can be initiated.

In addition, during EEPROM programming, an attempted read from the EEPROM will fetch the byte being written with the MSB complemented. Once the write cycle is completed, true data are valid at all bit locations.

rammable hdog Timer

The programmable Watchdog Timer (WDT) operates from an independent internal oscillator. The prescaler bits, PS0, PS1 and PS2 in SFR WMCON are used to set the period of the Watchdog Timer from 16 ms to 2048 ms. The available timer periods are shown in the following table and the actual timer periods (at V_{CC} = 5V) are within ±30% of the nominal.

The WDT is disabled by Power-on Reset and during Power-down. It is enabled by setting the WDTEN bit in SFR WMCON (address = 96H). The WDT is reset by setting the WDTRST bit in WMCON. When the WDT times out without being reset or disabled, an internal RST pulse is generated to reset the CPU.

Table 7. Watchdog Timer Period Selection

WDT Prescaler Bits			Period (nominal)
PS2	PS1	PS0	
0	0	0	16 ms
0	0	1	32 ms
0	1	0	64 ms
0	1	1	128 ms
1	0	0	256 ms
1	0	1	512 ms
1	1	0	1024 ms
1	1	1	2048 ms

0 and 1

Timer 0 and Timer 1 in the AT89S8252 operate the same way as Timer 0 and Timer 1 in the AT89C51 and AT89C52. For further information on the timers' operation, refer to the Atmel web site (http://www.atmel.com). From the home page, select "Products", then "Microcontrollers, then "8051-Architecture". Click on "Documentation", then on "Other Documents". Open the document "AT89 Series Hardware Description".

2

Timer 2 is a 16-bit Timer/Counter that can operate as either a timer or an event counter. The type of operation is selected by bit C/$\overline{T2}$ in the SFR T2CON (shown in Table 2). Timer 2 has three operating modes: capture, auto-reload (up or down counting), and baud rate generator. The modes are selected by bits in T2CON, as shown in Table 8.

Timer 2 consists of two 8-bit registers, TH2 and TL2. In the Timer function, the TL2 register is incremented every machine cycle. Since a machine cycle consists of 12 oscillator periods, the count rate is 1/12 of the oscillator frequency.

In the Counter function, the register is incremented in response to a 1-to-0 transition at its corresponding external input pin, T2. In this function, the external input is sampled during S5P2 of every machine cycle. When the samples show a high in one cycle and a low in the next cycle, the count is incremented. The new count value appears in the register during S3P1 of the cycle following the one in which the transition was detected.

Since two machine cycles (24 oscillator periods) are required to recognize a 1-to-0 transition, the maximum count rate is 1/24 of the oscillator frequency. To ensure that a given level is sampled at least once before it changes, the level should be held for at least one full machine cycle.

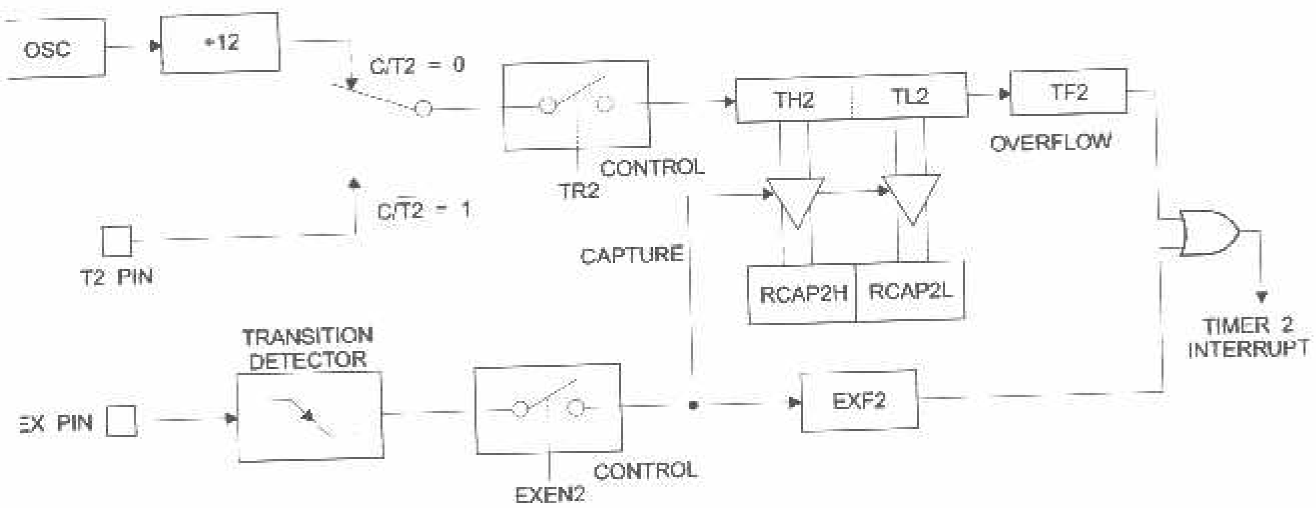
Table 8. Timer 2 Operating Modes

RCLK + TCLK	CP/$\overline{RL2}$	TR2	MODE
0	0	1	16-bit Auto-reload
0	1	1	16-bit Capture
1	X	1	Baud Rate Generator
X	X	0	(Off)

re Mode

In the capture mode, two options are selected by bit EXEN2 in T2CON. If EXEN2 = 0, Timer 2 is a 16-bit timer or counter which upon overflow sets bit TF2 in T2CON. This bit can then be used to generate an interrupt. If EXEN2 = 1, Timer 2 performs the same operation, but a l-to-0 transition at external input T2EX also causes the current value in TH2 and TL2 to be captured into RCAP2H and RCAP2L, respectively. In addition, the transition at T2EX causes bit EXF2 in T2CON to be set. The EXF2 bit, like TF2, can generate an interrupt. The capture mode is illustrated in Figure 1.

1. Timer 2 in Capture Mode



…eload (Up or Down …er)

Timer 2 can be programmed to count up or down when configured in its 16-bit auto-reload mode. This feature is invoked by the DCEN (Down Counter Enable) bit located in the SFR T2MOD (see Table 9). Upon reset, the DCEN bit is set to 0 so that timer 2 will default to count up. When DCEN is set, Timer 2 can count up or down, depending on the value of the T2EX pin.

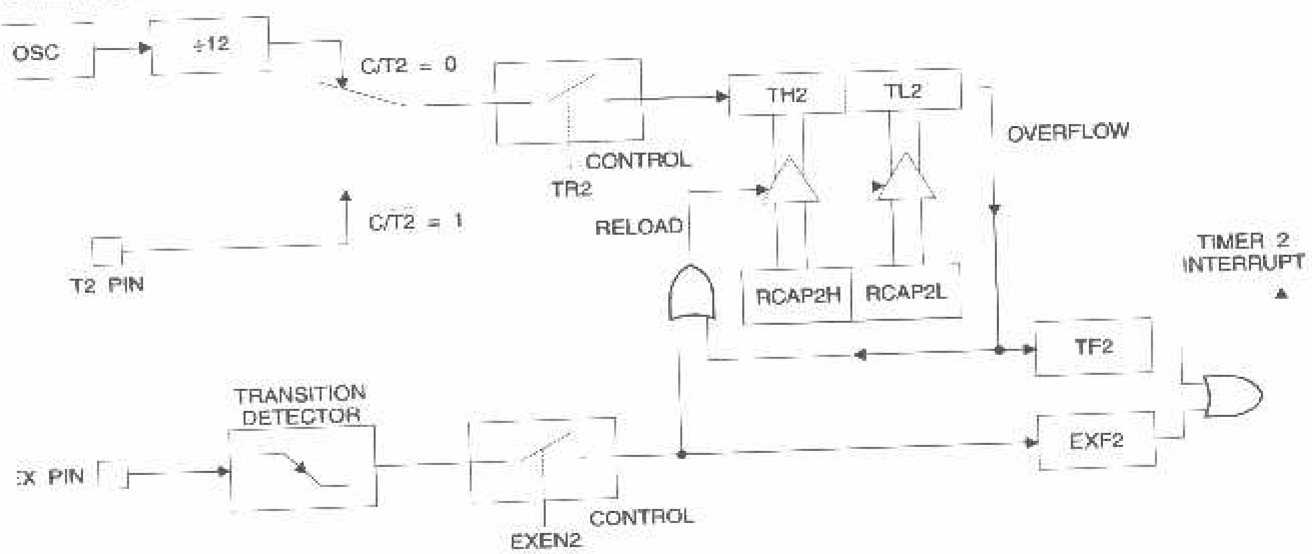
Figure 2 shows Timer 2 automatically counting up when DCEN = 0. In this mode, two options are selected by bit EXEN2 in T2CON. If EXEN2 = 0, Timer 2 counts up to 0FFFFH and then sets the TF2 bit upon overflow. The overflow also causes the timer registers to be reloaded with the 16-bit value in RCAP2H and RCAP2L. The values in RCAP2H and RCAP2L are preset by software. If EXEN2 = 1, a 16-bit reload can be triggered either by an overflow or by a 1-to-0 transition at external input T2EX. This transition also sets the EXF2 bit. Both the TF2 and EXF2 bits can generate an interrupt if enabled.

Setting the DCEN bit enables Timer 2 to count up or down, as shown in Figure 3. In this mode, the T2EX pin controls the direction of the count. A logic 1 at T2EX makes Timer 2 count up. The timer will overflow at 0FFFFH and set the TF2 bit. This overflow also causes the 16-bit value in RCAP2H and RCAP2L to be reloaded into the timer registers, TH2 and TL2, respectively.

A logic 0 at T2EX makes Timer 2 count down. The timer underflows when TH2 and TL2 equal the values stored in RCAP2H and RCAP2L. The underflow sets the TF2 bit and causes 0FFFFH to be reloaded into the timer registers.

The EXF2 bit toggles whenever Timer 2 overflows or underflows and can be used as a 17th bit of resolution. In this operating mode, EXF2 does not flag an interrupt.

…2. Timer 2 in Auto Reload Mode (DCEN = 0)



T2MOD – Timer 2 Mode Control Register

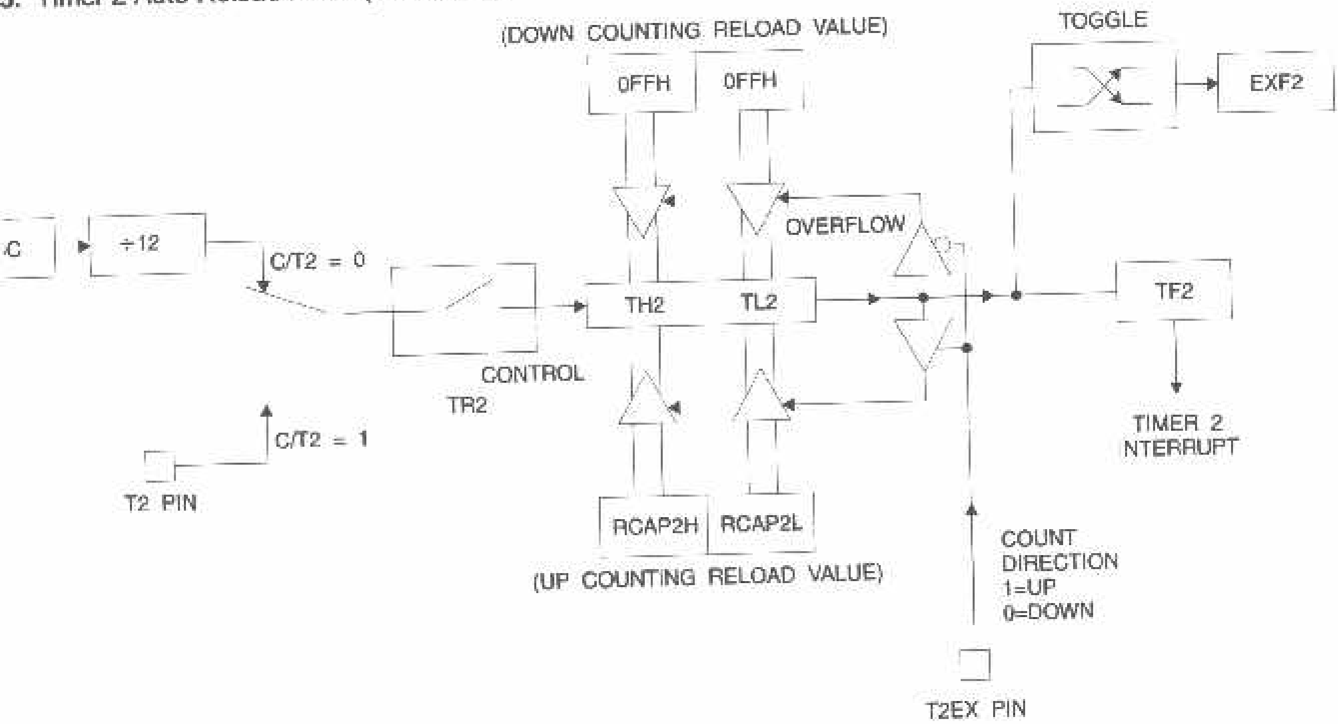
Address = 0C9H | Reset Value = XXXX XX00B

Addressable

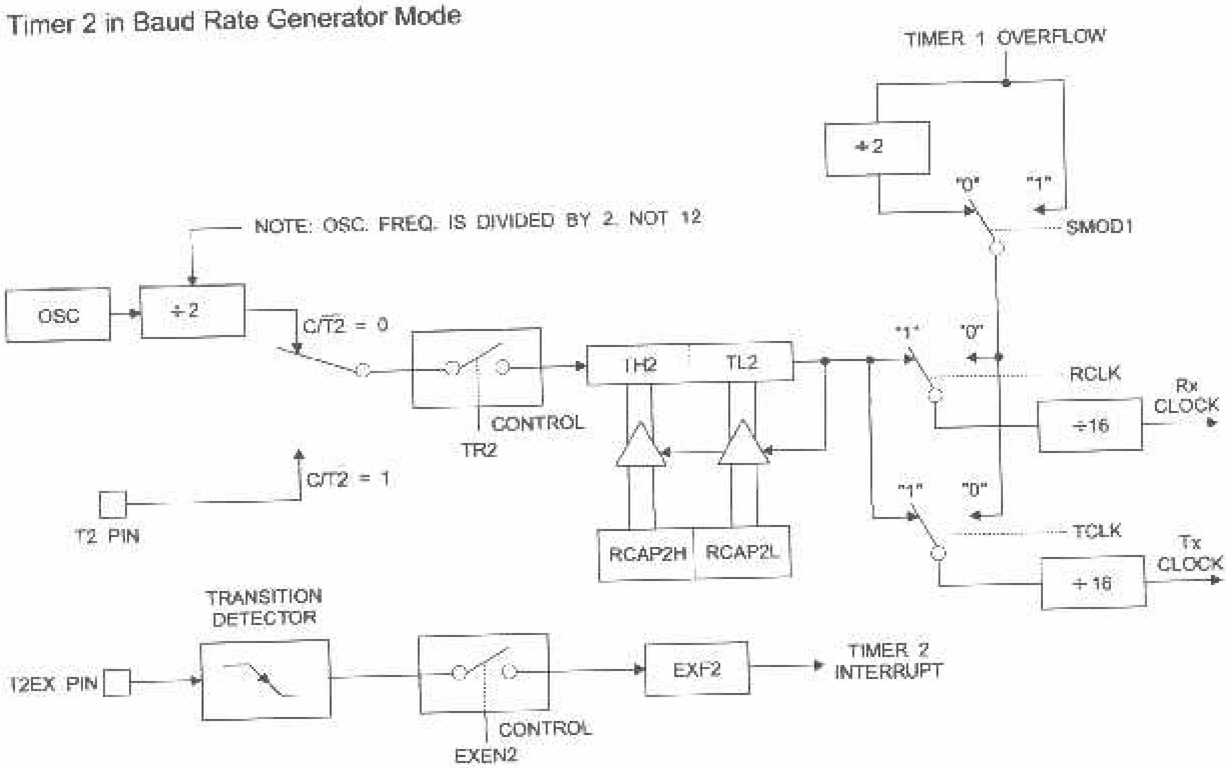
–	–	–	–	–	–	T2OE	DCEN
7	6	5	4	3	2	1	0

l	Function
	Not implemented, reserved for future use.
	Timer 2 Output Enable bit.
	When set, this bit allows Timer 2 to be configured as an up/down counter.

3. Timer 2 Auto Reload Mode (DCEN = 1)



. Timer 2 in Baud Rate Generator Mode



Rate Generator

Timer 2 is selected as the baud rate generator by setting TCLK and/or RCLK in T2CON (Table 2). Note that the baud rates for transmit and receive can be different if Timer 2 is used for the receiver or transmitter and Timer 1 is used for the other function. Setting RCLK and/or TCLK puts Timer 2 into its baud rate generator mode, as shown in Figure 4.

The baud rate generator mode is similar to the auto-reload mode, in that a rollover in TH2 causes the Timer 2 registers to be reloaded with the 16-bit value in registers RCAP2H and RCAP2L, which are preset by software.

The baud rates in Modes 1 and 3 are determined by Timer 2's overflow rate according to the following equation.

$$\text{Modes 1 and 3 Baud Rates} = \frac{\text{Timer 2 Overflow Rate}}{16}$$

The Timer can be configured for either timer or counter operation. In most applications, it is configured for timer operation ($CP/\overline{T2} = 0$). The timer operation is different for Timer 2 when it is used as a baud rate generator. Normally, as a timer, it increments every machine cycle (at 1/12 the oscillator frequency). As a baud rate generator, however, it increments every state time (at 1/2 the oscillator frequency). The baud rate formula is given below.

$$\frac{\text{Modes 1 and 3}}{\text{Baud Rate}} = \frac{\text{Oscillator Frequency}}{32 \times [65536 - (\text{RCAP2H,RCAP2L})]}$$

where (RCAP2H, RCAP2L) is the content of RCAP2H and RCAP2L taken as a 16-bit unsigned integer.

Timer 2 as a baud rate generator is shown in Figure 4. This figure is valid only if RCLK or TCLK = 1 in T2CON. Note that a rollover in TH2 does not set TF2 and will not generate an interrupt. Note too, that if EXEN2 is set, a 1-to-0 transition in T2EX will set EXF2 but will not cause a reload from (RCAP2H, RCAP2L) to (TH2, TL2). Thus when Timer 2 is in use as a baud rate generator, T2EX can be used as an extra external interrupt.

Note that when Timer 2 is running (TR2 = 1) as a timer in the baud rate generator mode, TH2 or TL2 should not be read from or written to. Under these conditions, the Timer is incremented every state time, and the results of a read or write may not be accurate. The RCAP2 registers may be read but should not be written to, because a write might overlap a reload and cause write and/or reload errors. The timer should be turned off (clear TR2) before accessing the Timer 2 or RCAP2 registers.

rammable
k Out

A 50% duty cycle clock can be programmed to come out on P1.0, as shown in Figure 5. This pin, besides being a regular I/O pin, has two alternate functions. It can be programmed to input the external clock for Timer/Counter 2 or to output a 50% duty cycle clock ranging from 61 Hz to 4 MHz (for a 16-MHz operating frequency).

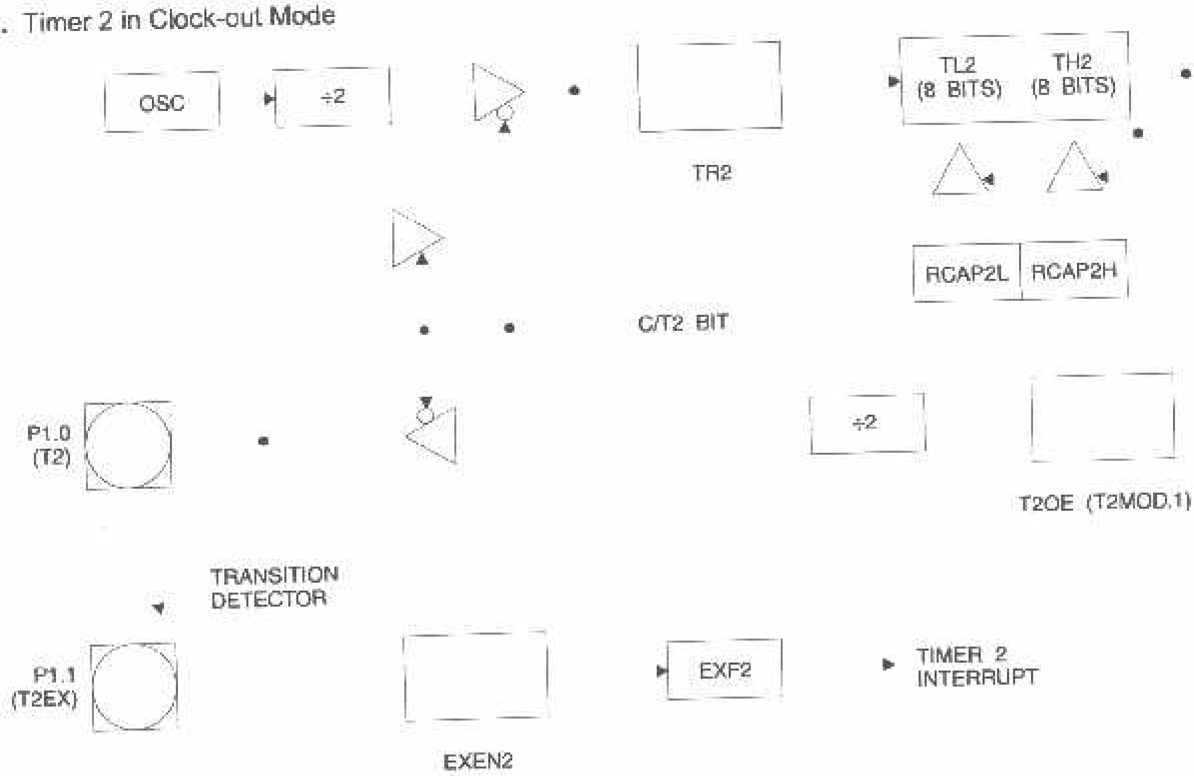
To configure the Timer/Counter 2 as a clock generator, bit C/$\overline{\text{T2}}$ (T2CON.1) must be cleared and bit T2OE (T2MOD.1) must be set. Bit TR2 (T2CON.2) starts and stops the timer.

The clock-out frequency depends on the oscillator frequency and the reload value of Timer 2 capture registers (RCAP2H, RCAP2L), as shown in the following equation.

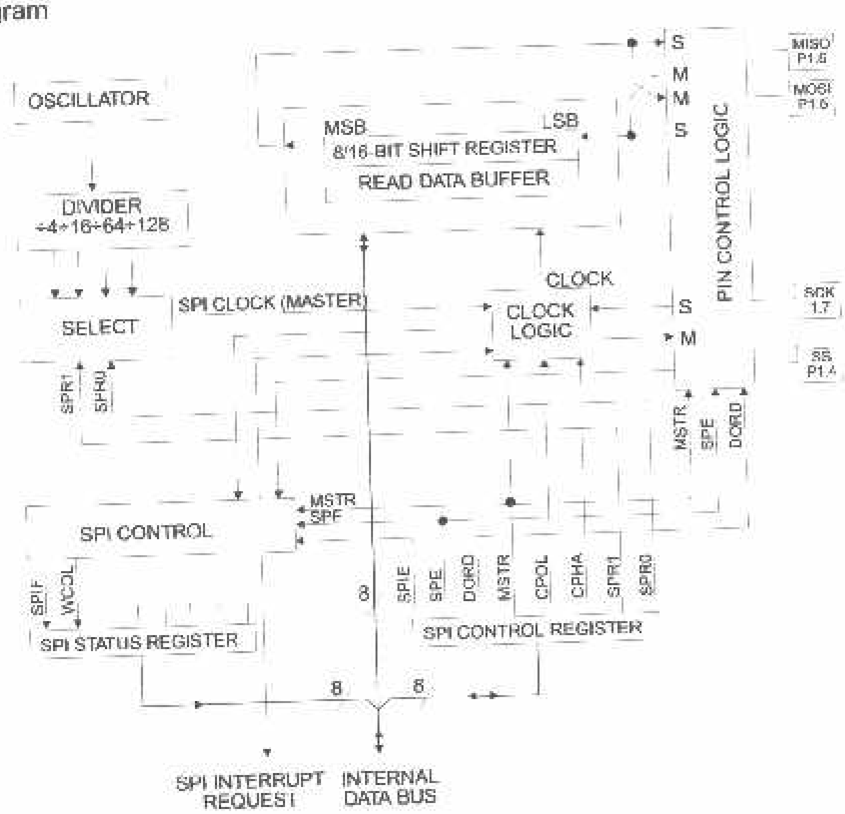
$$\text{Clock Out Frequency} = \frac{\text{Oscillator Frequency}}{4 \times [65536 - (\text{RCAP2H,RCAP2L})]}$$

In the clock-out mode, Timer 2 rollovers will not generate an interrupt. This behavior is similar to when Timer 2 is used as a baud-rate generator. It is possible to use Timer 2 as a baud-rate generator and a clock generator simultaneously. Note, however, that the baud-rate and clock-out frequencies cannot be determined independently from one another since they both use RCAP2H and RCAP2L.

. Timer 2 in Clock-out Mode



6. SPI Block Diagram



RO–11/03

The UART in the AT89S8252 operates the same way as the UART in the AT89C51 and AT89C52. For further information on the UART operation, refer to the Atmel web site (http://www.atmel.com). From the home page, select "Products", then "Microcontrollers, then "8051-Architecture". Click on "Documentation", then on "Other Documents". Open the document "AT89 Series Hardware Description".

l Peripheral ace

The serial peripheral interface (SPI) allows high-speed synchronous data transfer between the AT89S8252 and peripheral devices or between several AT89S8252 devices. The AT89S8252 SPI features include the following:

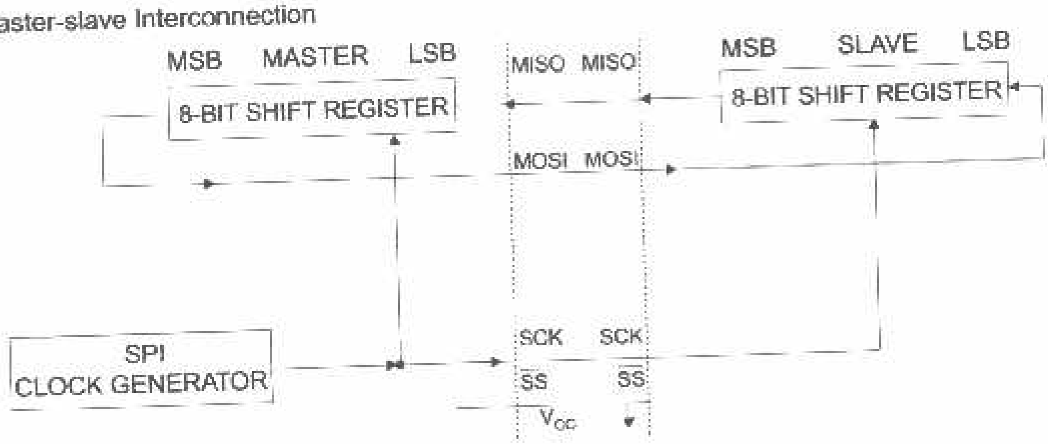
- Full-Duplex, 3-Wire Synchronous Data Transfer
- Master or Slave Operation
- 1.5 MHz Bit Frequency (max.)
- LSB First or MSB First Data Transfer
- Four Programmable Bit Rates
- End of Transmission Interrupt Flag
- Write Collision Flag Protection
- Wakeup from Idle Mode (Slave Mode Only)

The interconnection between master and slave CPUs with SPI is shown in the following figure. The SCK pin is the clock output in the master mode but is the clock input in the slave mode. Writing to the SPI data register of the master CPU starts the SPI clock generator, and the data written shifts out of the MOSI pin and into the MOSI pin of the slave CPU. After shifting one byte, the SPI clock generator stops, setting the end of transmission flag (SPIF). If both the SPI interrupt enable bit (SPIE) and the serial port interrupt enable bit (ES) are set, an interrupt is requested.

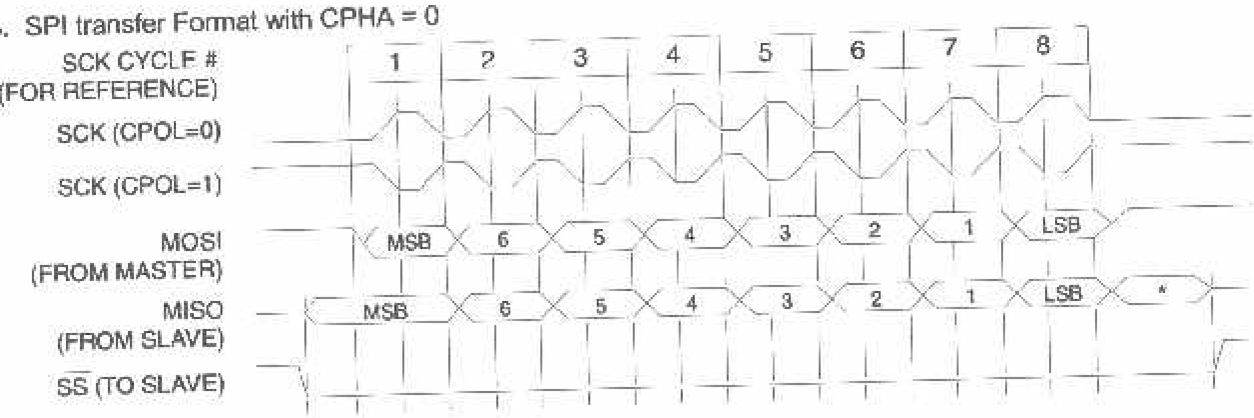
The Slave Select input, $\overline{SS}$/P1.4, is set low to select an individual SPI device as a slave. When $\overline{SS}$/P1.4 is set high, the SPI port is deactivated and the MOSI/P1.5 pin can be used as an input.

There are four combinations of SCK phase and polarity with respect to serial data, which are determined by control bits CPHA and CPOL. The SPI data transfer formats are shown in Figure 8 and Figure 9.

7. SPI Master-slave Interconnection

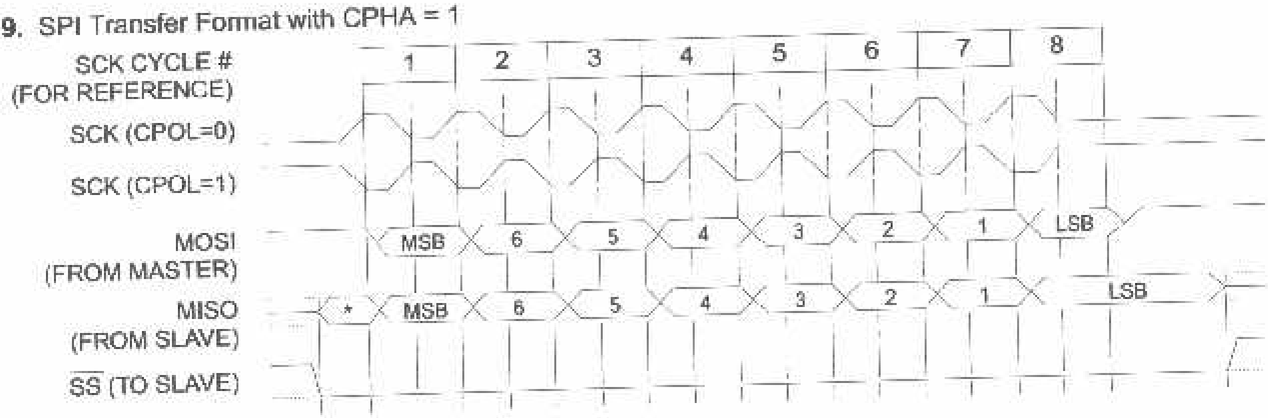


. SPI transfer Format with CPHA = 0



*Not defined but normally MSB of character just received

9. SPI Transfer Format with CPHA = 1



*Not defined but normally LSB of previously transmitted character.

upts

The AT89S8252 has a total of six interrupt vectors: two external interrupts ($\overline{INT0}$ and $\overline{INT1}$), three timer interrupts (Timers 0, 1, and 2), and the serial port interrupt. These interrupts are all shown in Figure 10.

Each of these interrupt sources can be individually enabled or disabled by setting or clearing a bit in Special Function Register IE. IE also contains a global disable bit, EA, which disables all interrupts at once.

Note that Table 10 shows that bit position IE.6 is unimplemented. In the AT89C51, bit position IE.5 is also unimplemented. User software should not write 1s to these bit positions, since they may be used in future AT89 products.

Timer 2 interrupt is generated by the logical OR of bits TF2 and EXF2 in register T2CON. Neither of these flags is cleared by hardware when the service routine is vectored to. In fact, the service routine may have to determine whether it was TF2 or EXF2 that generated the interrupt, and that bit will have to be cleared in software.

The Timer 0 and Timer 1 flags, TF0 and TF1, are set at S5P2 of the cycle in which the timers overflow. The values are then polled by the circuitry in the next cycle. However, the Timer 2 flag, TF2, is set at S2P2 and is polled in the same cycle in which the timer overflows.

. Interrupt Enable (IE) Register

SB)

EA	–	ET2	ES	ET1	EX1	ET0	EX0

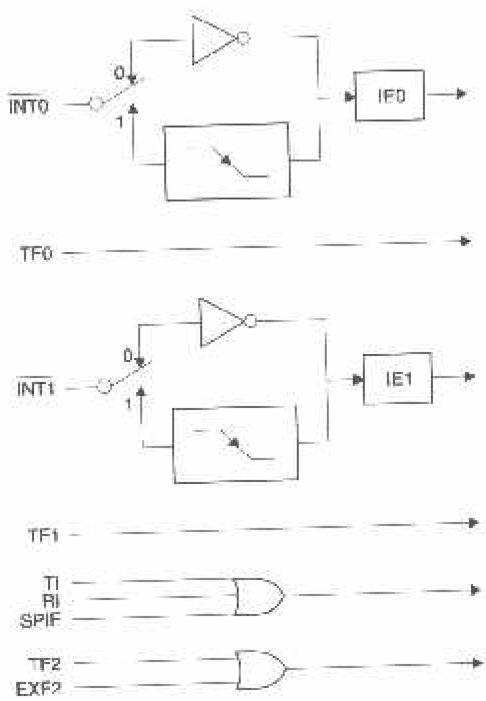
Enable Bit = 1 enables the interrupt.

Enable Bit = 0 disables the interrupt.

ymbol	Position	Function
EA	IE.7	Disables all interrupts. If EA = 0, no interrupt is acknowledged. If EA = 1, each interrupt source is individually enabled or disabled by setting or clearing its enable bit.
–	IE.6	Reserved.
ET2	IE.5	Timer 2 interrupt enable bit.
ES	IE.4	SPI and UART interrupt enable bit.
ET1	IE.3	Timer 1 interrupt enable bit.
EX1	IE.2	External interrupt 1 enable bit.
ET0	IE.1	Timer 0 interrupt enable bit.
EX0	IE.0	External interrupt 0 enable bit.

ftware should never write 1s to unimplemented bits, because they may be used in future AT89 products.

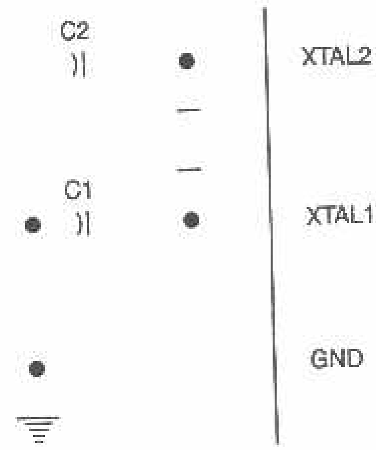
10. Interrupt Sources



ator
cteristics

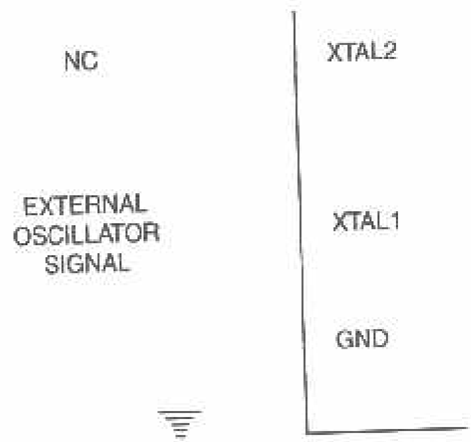
XTAL1 and XTAL2 are the input and output, respectively, of an inverting amplifier that can be configured for use as an on-chip oscillator, as shown in Figure 11. Either a quartz crystal or ceramic resonator may be used. To drive the device from an external clock source, XTAL2 should be left unconnected while XTAL1 is driven, as shown in Figure 12. There are no requirements on the duty cycle of the external clock signal, since the input to the internal clocking circuitry is through a divide-by-two flip-flop, but minimum and maximum voltage high and low time specifications must be observed.

Figure 11. Oscillator Connections



Note: C1, C2 = 30 pF ± 10 pF for Crystals
= 40 pF ± 10 pF for Ceramic Resonators

Figure 12. External Clock Drive Configuration



ode

In idle mode, the CPU puts itself to sleep while all the on-chip peripherals remain active. The mode is invoked by software. The content of the on-chip RAM and all the special functions registers remain unchanged during this mode. The idle mode can be terminated by any enabled interrupt or by a hardware reset.

Note that when idle mode is terminated by a hardware reset, the device normally resumes program execution from where it left off, up to two machine cycles before the internal reset algorithm takes control. On-chip hardware inhibits access to internal RAM in this event, but access to the port pins is not inhibited. To eliminate the possibility of an unexpected write to a port pin when idle mode is terminated by a reset, the instruction following the one that invokes idle mode should not write to a port pin or to external memory.

Status of External Pins During Idle and Power-down Modes

Mode	Program Memory	ALE	$\overline{PSEN}$	PORT0	PORT1	PORT2	PORT3
Idle	Internal	1	1	Data	Data	Data	Data
Idle	External	1	1	Float	Data	Address	Data
Power-down	Internal	0	0	Data	Data	Data	Data
Power-down	External	0	0	Float	Data	Data	Data

r-down Mode

In the power-down mode, the oscillator is stopped and the instruction that invokes power-down is the last instruction executed. The on-chip RAM and Special Function Registers retain their values until the power-down mode is terminated. Exit from power-down can be initiated either by a hardware reset or by an enabled external interrupt. Reset redefines the SFRs but does not change the on-chip RAM. The reset should not be activated before V_{CC} is restored to its normal operating level and must be held active long enough to allow the oscillator to restart and stabilize.

To exit power-down via an interrupt, the external interrupt must be enabled as level sensitive before entering power-down. The interrupt service routine starts at 16 ms (nominal) after the enabled interrupt pin is activated.

am Memory Bits

The AT89S8252 has three lock bits that can be left unprogrammed (U) or can be programmed (P) to obtain the additional features listed in the following table.

When lock bit 1 is programmed, the logic level at the $\overline{EA}$ pin is sampled and latched during reset. If the device is powered up without a reset, the latch initializes to a random value and holds that value until reset is activated. The latched value of $\overline{EA}$ must agree with the current logic level at that pin in order for the device to function properly.

Once programmed, the lock bits can only be unprogrammed with the Chip Erase operations in either the parallel or serial modes.

3it Protection Modes[(1)(2)]

Program Lock Bits			
LB1	LB2	LB3	Protection Type
U	U	U	No internal memory lock feature.
P	U	U	MOVC instructions executed from external program memory are disabled from fetching code bytes from internal memory. $\overline{EA}$ is sampled and latched on reset and further programming of the Flash memory (parallel or serial mode) is disabled.
P	P	U	Same as Mode 2, but parallel or serial verify are also disabled.
P	P	P	Same as Mode 3, but external execution is also disabled.

1. U = Unprogrammed
2. P = Programmed

...amming the ...and EEPROM

Atmel's AT89S8252 Flash Microcontroller offers 8K bytes of in-system reprogrammable Flash Code memory and 2K bytes of EEPROM Data memory.

The AT89S8252 is normally shipped with the on-chip Flash Code and EEPROM Data memory arrays in the erased state (i.e. contents = FFH) and ready to be programmed. This device supports a High-voltage (12-V V_{PP}) Parallel programming mode and a Low-voltage (5-V V_{CC}) Serial programming mode. The serial programming mode provides a convenient way to reprogram the AT89S8252 inside the user's system. The parallel programming mode is compatible with conventional third party Flash or EPROM programmers.

The Code and Data memory arrays are mapped via separate address spaces in the serial programming mode. In the parallel programming mode, the two arrays occupy one contiguous address space: 0000H to 1FFFH for the Code array and 2000H to 27FFH for the Data array.

The Code and Data memory arrays on the AT89S8252 are programmed byte-by-byte in either programming mode. An auto-erase cycle is provided with the self-timed programming operation in the serial programming mode. There is no need to perform the Chip Erase operation to reprogram any memory location in the serial programming mode unless any of the lock bits have been programmed.

In the parallel programming mode, there is no auto-erase cycle. To reprogram any non-blank byte, the user needs to use the Chip Erase operation first to erase both arrays.

Parallel Programming Algorithm: To program and verify the AT89S8252 in the parallel programming mode, the following sequence is recommended:

1. Power-up sequence:
   Apply power between V_{CC} and GND pins.
   Set RST pin to "H".
   Apply a 3 MHz to 24 MHz clock to XTAL1 pin and wait for at least 10 milliseconds.
2. Set $\overline{\text{PSEN}}$ pin to "L"
   ALE pin to "H"
   $\overline{\text{EA}}$ pin to "H" and all other pins to "H".
3. Apply the appropriate combination of "H" or "L" logic levels to pins P2.6, P2.7, P3.6, P3.7 to select one of the programming operations shown in the Flash Programming Modes table.
4. Apply the desired byte address to pins P1.0 to P1.7 and P2.0 to P2.5.
   Apply data to pins P0.0 to P0.7 for Write Code operation.
5. Raise $\overline{\text{EA}}/V_{PP}$ to 12V to enable Flash programming, erase or verification.
6. Pulse ALE/$\overline{\text{PROG}}$ once to program a byte in the Code memory array, the Data memory array or the lock bits. The byte-write cycle is self-timed and typically takes 1.5 ms.
7. To verify the byte just programmed, bring pin P2.7 to "L" and read the programmed data at pins P0.0 to P0.7.
8. Repeat steps 3 through 7 changing the address and data for the entire 2K or 8K bytes array or until the end of the object file is reached.
9. Power-off sequence:
   Set XTAL1 to "L".
   Set RST and $\overline{\text{EA}}$ pins to "L".
   Turn V_{CC} power off.

In the parallel programming mode, there is no auto-erase cycle and to reprogram any non-blank byte, the user needs to use the Chip Erase operation first to erase both arrays.

Data Polling: The AT89S8252 features $\overline{\text{DATA}}$ Polling to indicate the end of a byte write cycle. During a byte write cycle in the parallel or serial programming mode, an attempted read of the last byte written will result in the complement of the written datum on P0.7 (parallel mode), and on the MSB of the serial output byte on MISO (serial mode). Once the write cycle has been completed, true data are valid on all outputs, and the next cycle may begin. $\overline{\text{DATA}}$ Polling may begin any time after a write cycle has been initiated.

Ready/$\overline{\text{Busy}}$: The progress of byte programming in the parallel programming mode can also be monitored by the RDY/$\overline{\text{BSY}}$ output signal. Pin P3.4 is pulled Low after ALE goes High during programming to indicate $\overline{\text{BUSY}}$. P3.4 is pulled High again when programming is done to indicate READY.

Program Verify: If lock bits LB1 and LB2 have not been programmed, the programmed Code or Data byte can be read back via the address and data lines for verification. The state of the lock bits can also be verified directly in the parallel programming mode. In the serial programming mode, the state of the lock bits can only be verified indirectly by observing that the lock bit features are enabled.

Chip Erase: Both Flash and EEPROM arrays are erased electrically at the same time. In the parallel programming mode, chip erase is initiated by using the proper combination of control signals and by holding ALE/$\overline{\text{PROG}}$ low for 10 ms. The Code and Data arrays are written with all "1"s in the Chip Erase operation.

In the serial programming mode, a chip erase operation is initiated by issuing the Chip Erase instruction. In this mode, chip erase is self-timed and takes about 16 ms.

During chip erase, a serial read from any address location will return 00H at the data outputs.

Serial Programming Fuse: A programmable fuse is available to disable Serial Programming if the user needs maximum system security. The Serial Programming Fuse can only be programmed or erased in the Parallel Programming Mode.

The AT89S8252 is shipped with the Serial Programming Mode enabled.

Reading the Signature Bytes: The signature bytes are read by the same procedure as a normal verification of locations 030H and 031H, except that P3.6 and P3.7 must be pulled to a logic low. The values returned are as follows:

(030H) = 1EH indicates manufactured by Atmel
(031H) = 72H indicates 89S8252

amming ace

Every code byte in the Flash and EEPROM arrays can be written, and the entire array can be erased, by using the appropriate combination of control signals. The write operation cycle is self-timed and once initiated, will automatically time itself to completion.

Most worldwide major programming vendors offer support for the Atmel AT89 microcontroller series. Please contact your local programming vendor for the appropriate software revision.

Downloading

Both the Code and Data memory arrays can be programmed using the serial SPI bus while RST is pulled to V_{CC}. The serial interface consists of pins SCK, MOSI (input) and MISO (output). After RST is set high, the Programming Enable instruction needs to be executed first before program/erase operations can be executed.

An auto-erase cycle is built into the self-timed programming operation (in the serial mode ONLY) and there is no need to first execute the Chip Erase instruction unless any of the lock bits have been programmed. The Chip Erase operation turns the content of every memory location in both the Code and Data arrays into FFH.

The Code and Data memory arrays have separate address spaces:

0000H to 1FFFH for Code memory and 000H to 7FFH for Data memory.

Either an external system clock is supplied at pin XTAL1 or a crystal needs to be connected across pins XTAL1 and XTAL2. The maximum serial clock (SCK) frequency should be less than 1/40 of the crystal frequency. With a 24 MHz oscillator clock, the maximum SCK frequency is 600 kHz.

Programming thm

To program and verify the AT89S8252 in the serial programming mode, the following sequence is recommended:

1. Power-up sequence:

   Apply power between VCC and GND pins.

   Set RST pin to "H".

   If a crystal is not connected across pins XTAL1 and XTAL2, apply a 3 MHz to 24 MHz clock to XTAL1 pin and wait for at least 10 milliseconds.
2. Enable serial programming by sending the Programming Enable serial instruction to pin MOSI/P1.5. The frequency of the shift clock supplied at pin SCK/P1.7 needs to be less than the CPU clock at XTAL1 divided by 40.
3. The Code or Data array is programmed one byte at a time by supplying the address and data together with the appropriate Write instruction. The selected memory location is first automatically erased before new data is written. The write cycle is self-timed and typically takes less than 2.5 ms at 5V.
4. Any memory location can be verified by using the Read instruction which returns the content at the selected address at serial output MISO/P1.6.
5. At the end of a programming session, RST can be set low to commence normal operation.
6. Power-off sequence (if needed):

   Set XTAL1 to "L" (if a crystal is not used).

   Set RST to "L".

   Turn V_{CC} power off.

Programming tion

The Instruction Set for Serial Programming follows a 3-byte protocol and is shown in the following table:

on Set

tion	Input Format			Operation
	Byte 1	Byte 2	Byte 3	
nming Enable	1010 1100	0101 0011	xxxx xxxx	Enable serial programming interface after RST goes high.
ase	1010 1100	xxxx x100	xxxx xxxx	Chip erase both 8K & 2K memory arrays.
ode Memory	aaaa a001	low addr	xxxx xxxx	Read data from Code memory array at the selected address. The 5 MSBs of the first byte are the high order address bits. The low order address bits are in the second byte. Data are available at pin MISO during the third byte.
ode Memory	aaaa a010	low addr	data in	Write data to Code memory location at selected address. The address bits are the 5 MSBs of the first byte together with the second byte.
lata Memory	00aa a101	low addr	xxxx xxxx	Read data from Data memory array at selected address. Data are available at pin MISO during the third byte.
ata Memory	00aa a110	low addr	data in	Write data to Data memory location at selected address.
ock Bits	1010 1100	LB1 LB2 LB3 x x111	xxxx xxxx	Write lock bits. Set LB1, LB2 or LB3 = "0" to program lock bits.

1. DATA polling is used to indicate the end of a byte write cycle which typically takes less than 2.5 ms at 5V.
2. "aaaaa" = high order address.
3. "x" = don't care.

and EEPROM Parallel Programming Modes

	RST	$\overline{PSEN}$	ALE/$\overline{PROG}$	$\overline{EA}/V_{PP}$	P2.6	P2.7	P3.6	P3.7	Data I/O P0.7:0	Address P2.5:0 P1.7:0
og. Modes	H	h(1)	h(1)	x						
se	H	L	(2)	12V	H	L	L	L	X	X
0K bytes) Memory	H	L		12V	L	H	H	H	DIN	ADDR
0K bytes) Memory	H	L	H	12V	L	L	H	H	DOUT	ADDR
ock Bits:	H	L		12V	H	L	H	L	DIN	X
Bit - 1									P0.7 = 0	X
Bit - 2									P0.6 = 0	X
Bit - 3									P0.5 = 0	X
ock Bits:	H	L	H	12V	H	H	L	L	DOUT	X
Bit - 1									@P0.2	X
Bit - 2									@P0.1	X
Bit - 3									@P0.0	X
mel Code	H	L	H	12V	L	L	L	L	DOUT	30H
evice Code	H	L	H	12V	L	L	L	L	DOUT	31H
og. Enable	H	L	(2)	12V	L	H	L	H	P0.0 = 0	X
og. Disable	H	L	(2)	12V	L	H	L	H	P0.0 = 1	X
rial Prog. Fuse	H	L	H	12V	H	H	L	H	@P0.0	X

1. "h" = weakly pulled "High" internally.
2. Chip Erase and Serial Programming Fuse require a 10 ms $\overline{PROG}$ pulse. Chip Erase needs to be performed first before reprogramming any byte with a content other than FFH.
3. P3.4 is pulled Low during programming to indicate RDY/$\overline{BSY}$.
4. "X" = don't care

3. Programming the Flash/EEPROM Memory

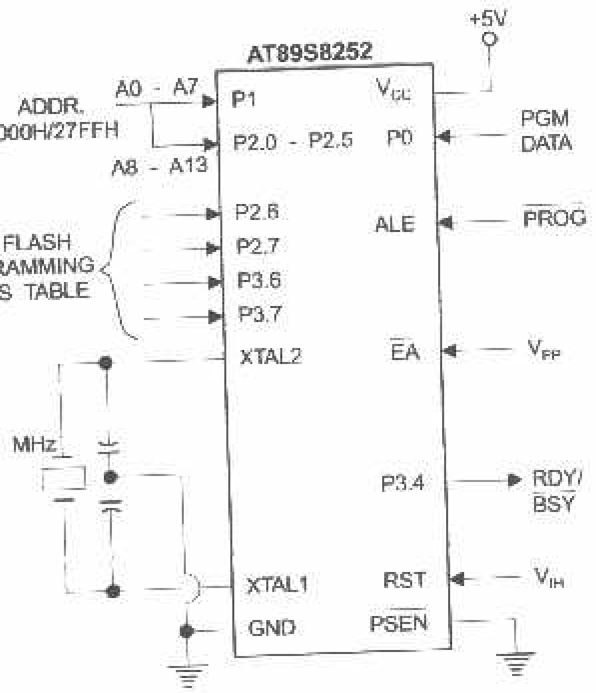
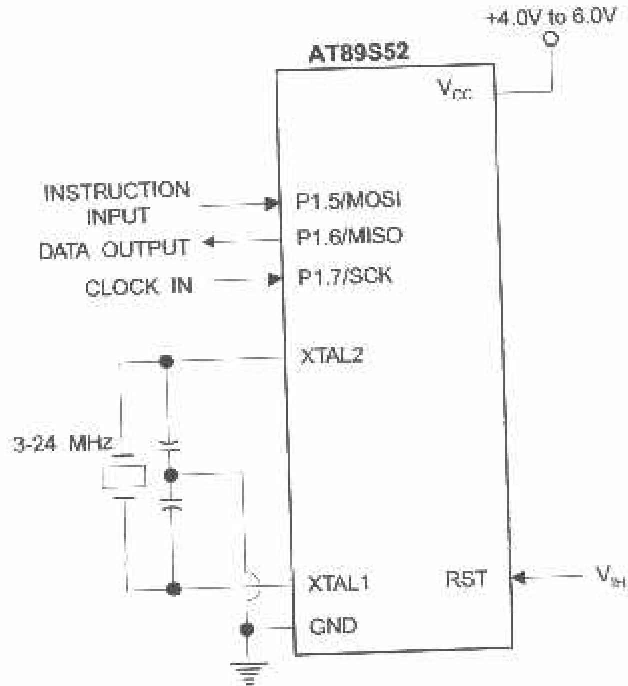
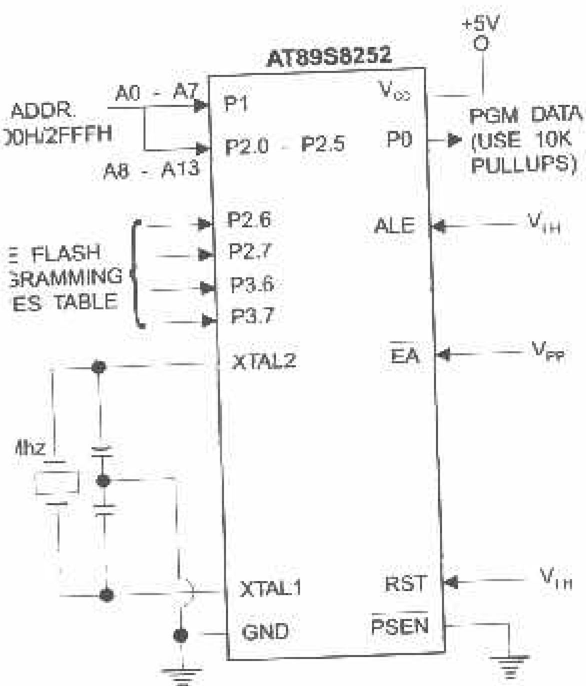


Figure 15. Flash/EEPROM Serial Downloading



14. Verifying the Flash/EEPROM Memory

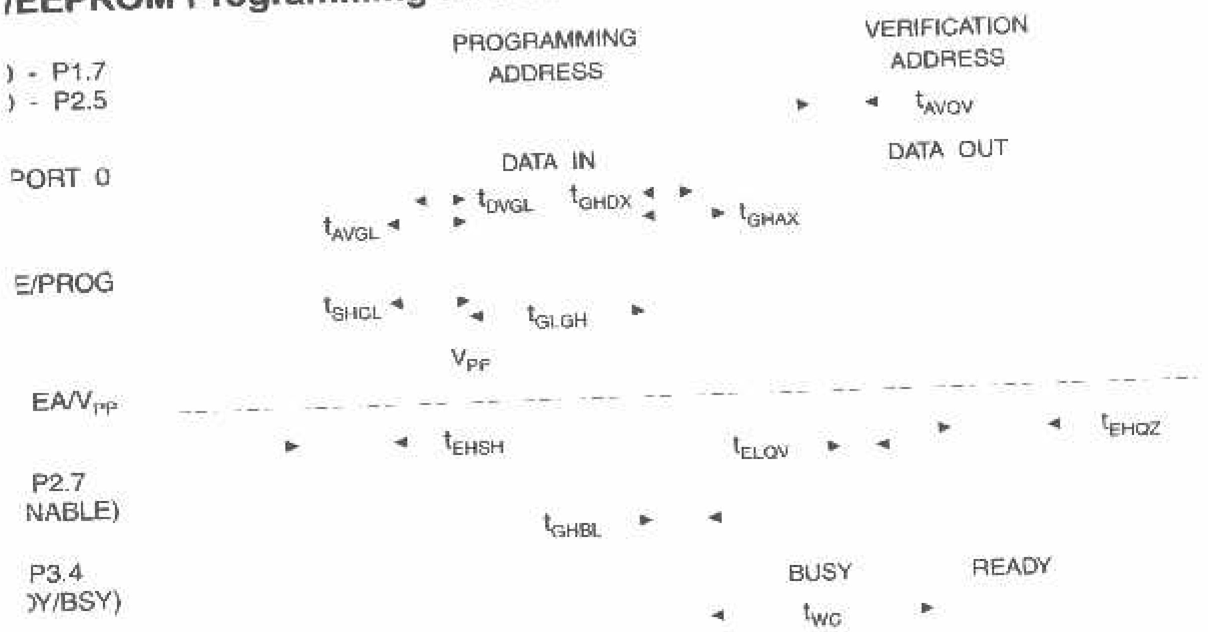


Programming and Verification Characteristics – Parallel Mode

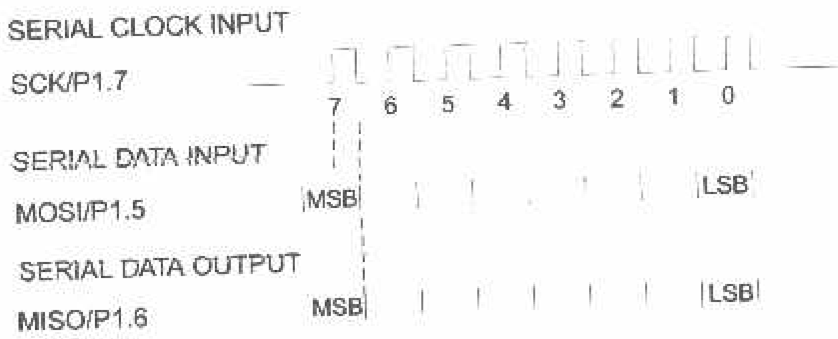
to 70°C, V_{CC} = 5.0V ±10%

Parameter	Min	Max	Units
Programming Enable Voltage	11.5	12.5	V
Programming Enable Current		1.0	mA
Oscillator Frequency	3	24	MHz
Address Setup to $\overline{PROG}$ Low	$48t_{CLCL}$		
Address Hold after $\overline{PROG}$	$48t_{CLCL}$		
Data Setup to $\overline{PROG}$ Low	$48t_{CLCL}$		
Data Hold after $\overline{PROG}$	$48t_{CLCL}$		
P2.7 ($\overline{ENABLE}$) High to V_{PP}	$48t_{CLCL}$		
V_{PP} Setup to $\overline{PROG}$ Low	10		µs
$\overline{PROG}$ Width	1	110	µs
Address to Data Valid		$48t_{CLCL}$	
$\overline{ENABLE}$ Low to Data Valid		$48t_{CLCL}$	
Data Float after $\overline{ENABLE}$	0	$48t_{CLCL}$	
$\overline{PROG}$ High to $\overline{BUSY}$ Low		1.0	µs
Byte Write Cycle Time		2.0	ms

/EEPROM Programming and Verification Waveforms – Parallel Mode

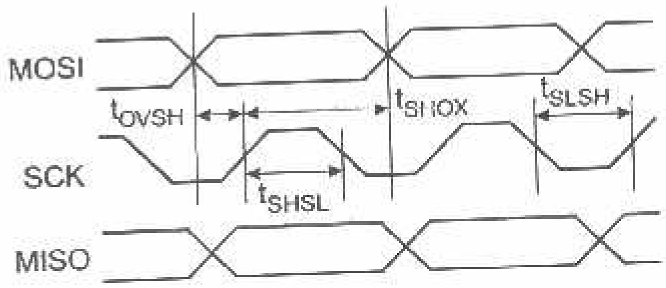


Downloading Waveforms



Programming Characteristics

16. Serial Programming Timing



. Serial Programming Characteristics, T_A = -40° C to 85° C, V_{CC} = 4.0 - 6.0V (Unless Otherwise Noted)

Parameter	Min	Typ	Max	Units
Oscillator Frequency	0		24	MHz
Oscillator Period	41.6			ns
SCK Pulse Width High	24 t_{CLCL}			ns
SCK Pulse Width Low	24 t_{CLCL}			ns
MOSI Setup to SCK High	t_{CLCL}			ns
MOSI Hold after SCK High	2 t_{CLCL}			ns

ute Maximum Ratings*

g Temperature	-55°C to +125°C
Temperature	-65°C to +150°C
on Any Pin spect to Ground	-1.0V to +7.0V
m Operating Voltage	6.6V
put Current	15.0 mA

*NOTICE: Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

haracteristics

ues shown in this table are valid for T_A = -40°C to 85°C and V_{CC} = 5.0V ± 20%, unless otherwise noted.

Parameter	Condition	Min	Max	Units
Input Low-voltage	(Except EA)	-0.5	0.2 V_{CC} - 0.1	V
Input Low-voltage (EA)		-0.5	0.2 V_{CC} - 0.3	V
Input High-voltage	(Except XTAL1, RST)	0.2 V_{CC} + 0.9	V_{CC} + 0.5	V
Input High-voltage	(XTAL1, RST)	0.7 V_{CC}	V_{CC} + 0.5	V
Output Low-voltage [1] (Ports 1,2,3)	I_{OL} = 1.6 mA		0.5	V
Output Low-voltage [1] (Port 0, ALE, PSEN)	I_{OL} = 3.2 mA		0.5	V
Output High-voltage (Ports 1,2,3, ALE, PSEN)	I_{OH} = -60 µA, V_{CC} = 5V ±10%	2.4		V
	I_{OH} = -25 µA	0.75 V_{CC}		V
	I_{OH} = -10 µA	0.9 V_{CC}		V
Output High-voltage (Port 0 in External Bus Mode)	I_{OH} = -800 µA, V_{CC} = 5V ±10%	2.4		V
	I_{OH} = -300 µA	0.75 V_{CC}		V
	I_{OH} = -80 µA	0.9 V_{CC}		V
Logical 0 Input Current (Ports 1,2,3)	V_{IN} = 0.45V		-50	µA
Logical 1 to 0 Transition Current (Ports 1,2,3)	V_{IN} = 2V, V_{CC} = 5V ± 10%		-650	µA
Input Leakage Current (Port 0, EA)	0.45 < V_{IN} < V_{CC}		±10	µA
Reset Pull-down Resistor		50	300	KΩ
Pin Capacitance	Test Freq. = 1 MHz, T_A = 25°C		10	pF
Power Supply Current	Active Mode, 12 MHz		25	mA
	Idle Mode, 12 MHz		6.5	mA
Power-down Mode [2]	V_{CC} = 6V		100	µA
	V_{CC} = 3V		40	µA

1. Under steady state (non-transient) conditions, I_{OL} must be externally limited as follows:
   Maximum I_{OL} per port pin: 10 mA
   Maximum I_{OL} per 8-bit port: Port 0: 26 mA; Ports 1, 2, 3: 15 mA
   Maximum total I_{OL} for all output pins: 71 mA
   If I_{OL} exceeds the test condition, V_{OL} may exceed the related specification. Pins are not guaranteed to sink current greater than the listed test conditions.
2. Minimum V_{CC} for Power-down is 2V

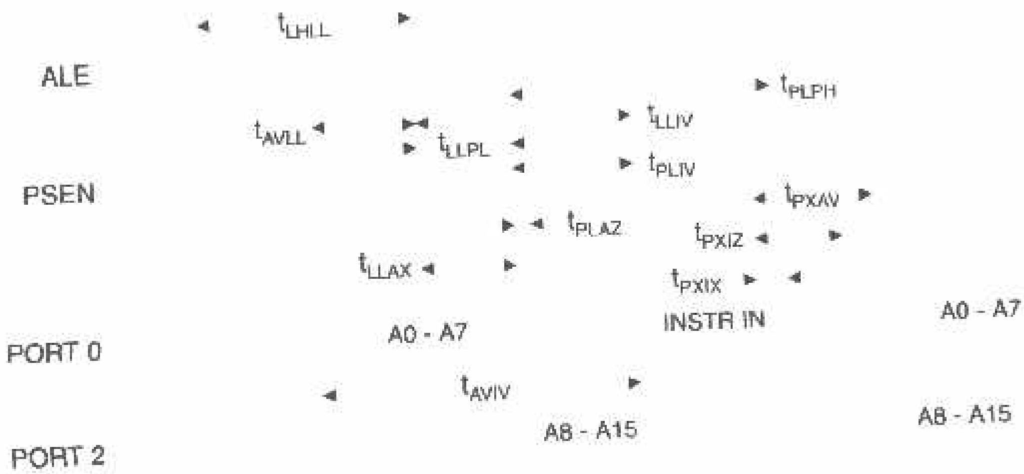
aracteristics

perating conditions, load capacitance for Port 0, ALE/$\overline{PROG}$, and $\overline{PSEN}$ = 100 pF; load capacitance for all other = 80 pF.

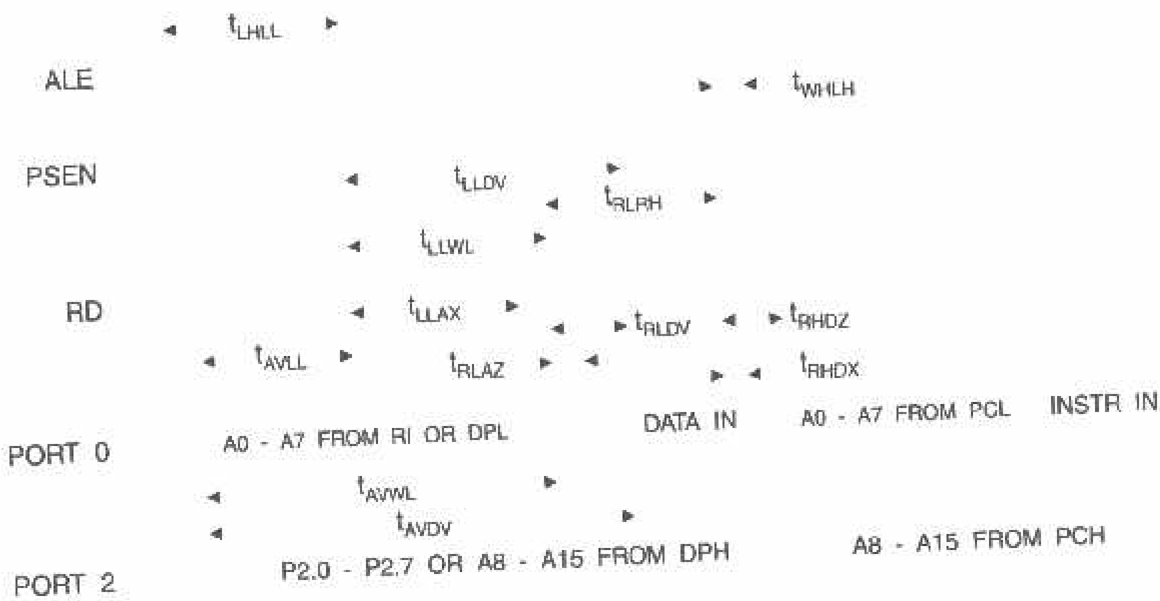
al Program and Data Memory Characteristics

Parameter	Variable Oscillator Min	Variable Oscillator Max	Units
Oscillator Frequency	0	24	MHz
ALE Pulse Width	$2t_{CLCL}$ - 40		ns
Address Valid to ALE Low	t_{CLCL} - 13		ns
Address Hold after ALE Low	t_{CLCL} - 20		ns
ALE Low to Valid Instruction In		$4t_{CLCL}$ - 65	ns
ALE Low to $\overline{PSEN}$ Low	t_{CLCL} - 13		ns
$\overline{PSEN}$ Pulse Width	$3t_{CLCL}$ - 20		ns
$\overline{PSEN}$ Low to Valid Instruction In		$3t_{CLCL}$ - 45	ns
Input Instruction Hold after $\overline{PSEN}$	0		ns
Input Instruction Float after $\overline{PSEN}$		t_{CLCL} - 10	ns
$\overline{PSEN}$ to Address Valid	t_{CLCL} - 8		ns
Address to Valid Instruction In		$5t_{CLCL}$ - 55	ns
$\overline{PSEN}$ Low to Address Float		10	ns
$\overline{RD}$ Pulse Width	$6t_{CLCL}$ - 100		ns
$\overline{WR}$ Pulse Width	$6t_{CLCL}$ - 100		ns
$\overline{RD}$ Low to Valid Data In		$5t_{CLCL}$ - 90	ns
Data Hold after $\overline{RD}$	0		ns
Data Float after $\overline{RD}$		$2t_{CLCL}$ - 28	ns
ALE Low to Valid Data In		$8t_{CLCL}$ - 150	ns
Address to Valid Data In		$9t_{CLCL}$ - 165	ns
ALE Low to $\overline{RD}$ or $\overline{WR}$ Low	$3t_{CLCL}$ - 50	$3t_{CLCL}$ + 50	ns
Address to $\overline{RD}$ or $\overline{WR}$ Low	$4t_{CLCL}$ - 75		ns
Data Valid to $\overline{WR}$ Transition	t_{CLCL} - 20		ns
Data Valid to $\overline{WR}$ High	$7t_{CLCL}$ - 120		ns
Data Hold after $\overline{WR}$	t_{CLCL} - 20		ns
$\overline{RD}$ Low to Address Float		0	ns
$\overline{RD}$ or $\overline{WR}$ High to ALE High	t_{CLCL} - 20	t_{CLCL} + 25	ns

nal Program Memory Read Cycle



nal Data Memory Read Cycle



nal Data Memory Write Cycle

t_{LHLL}

ALE

t_{WHLH}

PSEN

t_{LLWL} t_{WLWH}

WR

t_{LLAX}

t_{QVWX}

t_{WHQX}

t_{AVLL}

t_{QVWH}

PORT 0

A0 - A7 FROM RI OR DPL

DATA OUT

A0 - A7 FROM PCL

INSTR IN

t_{AVWL}

PORT 2

P2.0 - P2.7 OR A8 - A15 FROM DPH

A8 - A15 FROM PCH

nal Clock Drive Waveforms

t_{CHCX} t_{CHCL}

t_{CHCX} t_{CLCH}

V_{CC} - 0.5V

0.7 V_{CC}

0.2 V_{CC} - 0.1V

V

t_{CLCX}

t_{CLCL}

nal Clock Drive

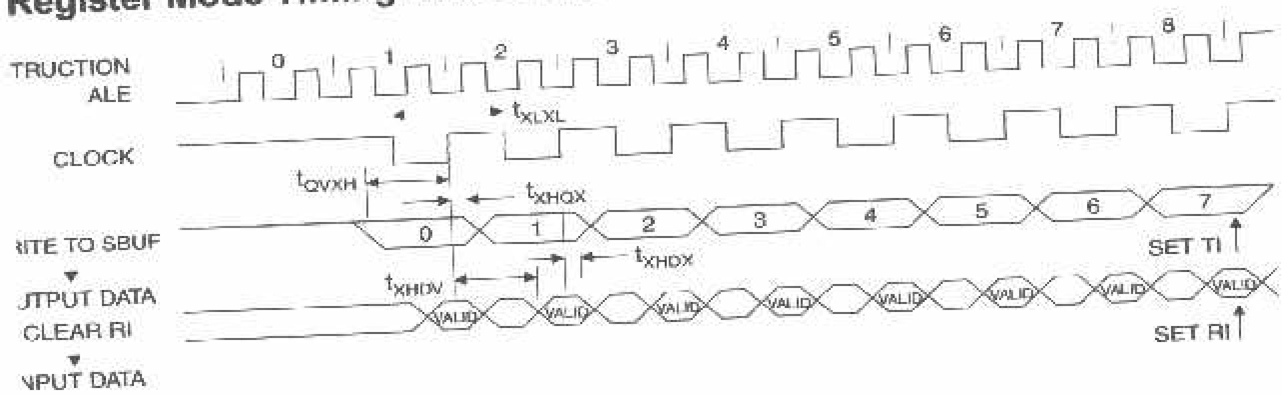
l	Parameter	V_{CC} = 4.0V to 6.0V Min	Max	Units
	Oscillator Frequency	0	24	MHz
	Clock Period	41.6		ns
	High Time	15		ns
	Low Time	15		ns
	Rise Time		20	ns
	Fall Time		20	ns

Port Timing: Shift Register Mode Test Conditions

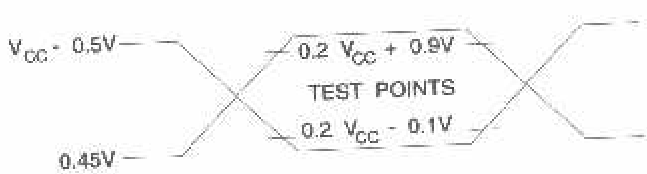
es in this table are valid for V_{CC} = 4.0V to 6V and Load Capacitance = 80 pF.

		Variable Oscillator		
	Parameter	Min	Max	Units
	Serial Port Clock Cycle Time	$12t_{CLCL}$		µs
	Output Data Setup to Clock Rising Edge	$10t_{CLCL}$ - 133		ns
	Output Data Hold after Clock Rising Edge	$2t_{CLCL}$ - 117		ns
	Input Data Hold after Clock Rising Edge	0		ns
	Clock Rising Edge to Input Data Valid		$10t_{CLCL}$ - 133	ns

Register Mode Timing Waveforms

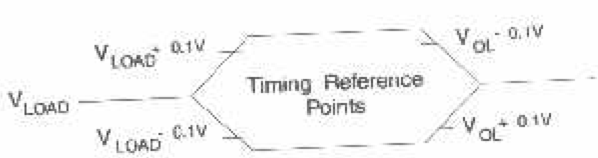


esting Input/Output Waveforms(1)



1. AC Inputs during testing are driven at V_{CC} - 0.5V for a logic 1 and 0.45V for a logic 0. Timing measurements are made at V_{IH} min. for a logic 1 and V_{IL} max. for a logic 0.

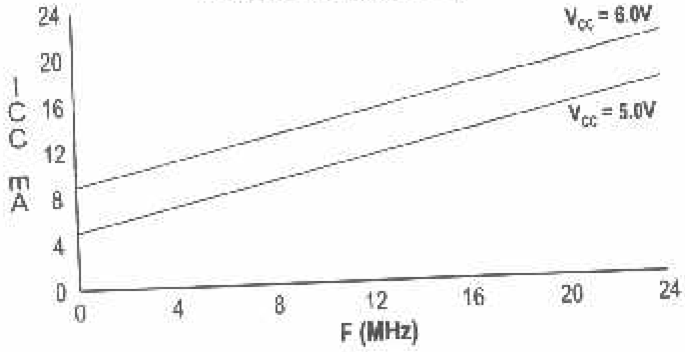
Waveforms(1)



1. For timing purposes, a port pin is no longer floating when a 100 mV change from load voltage occurs. A port pin begins to float when a 100 mV change from the loaded V_{OH}/V_{OL} level occurs.

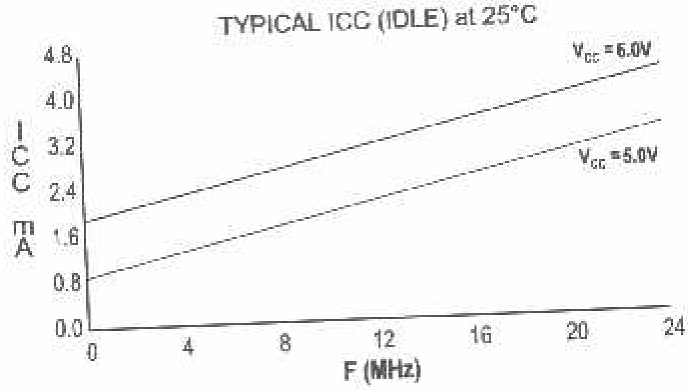
AT89S8252

TYPICAL ICC (ACTIVE) at 25°C



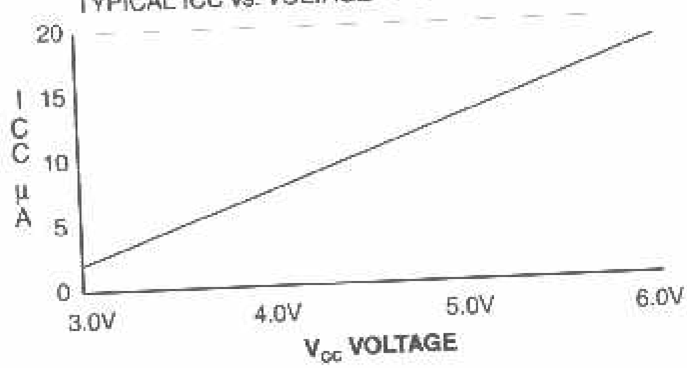
AT89S8252

TYPICAL ICC (IDLE) at 25°C



AT89S8252

TYPICAL ICC vs. VOLTAGE - POWER DOWN (85°C)



Notes: 1. XTAL1 tied to GND for Icc (power-down)
2. Lock bits programmed

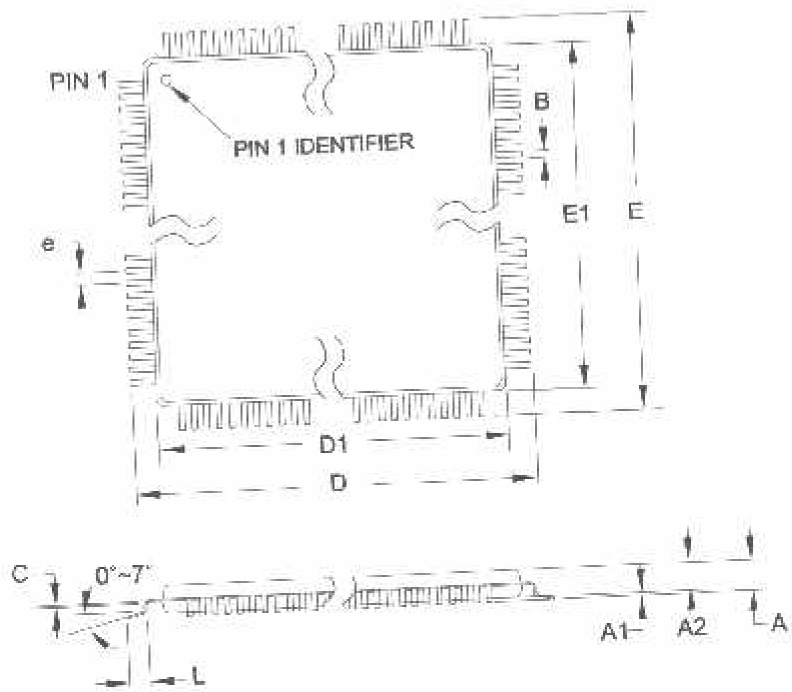
ing Information

d)	Power Supply	Ordering Code	Package	Operation Range
	4.0V to 6.0V	AT89S8252-24AC	44A	Commercial
		AT89S8252-24JC	44J	(0° C to 70° C)
		AT89S8252-24PC	40P6	
	4.0V to 6.0V	AT89S8252-24AI	44A	Industrial
		AT89S8252-24JI	44J	(-40° C to 85° C)
		AT89S8252-24PI	40P6	

	Package Type
	44-lead, Thin Plastic Gull Wing Quad Flatpack (TQFP)
	44-lead, Plastic J-leaded Chip Carrier (PLCC)
	40-lead, 0.600" Wide, Plastic Dual Inline Package (PDIP)

...ging Information

...TQFP



COMMON DIMENSIONS
(Unit of Measure = mm)

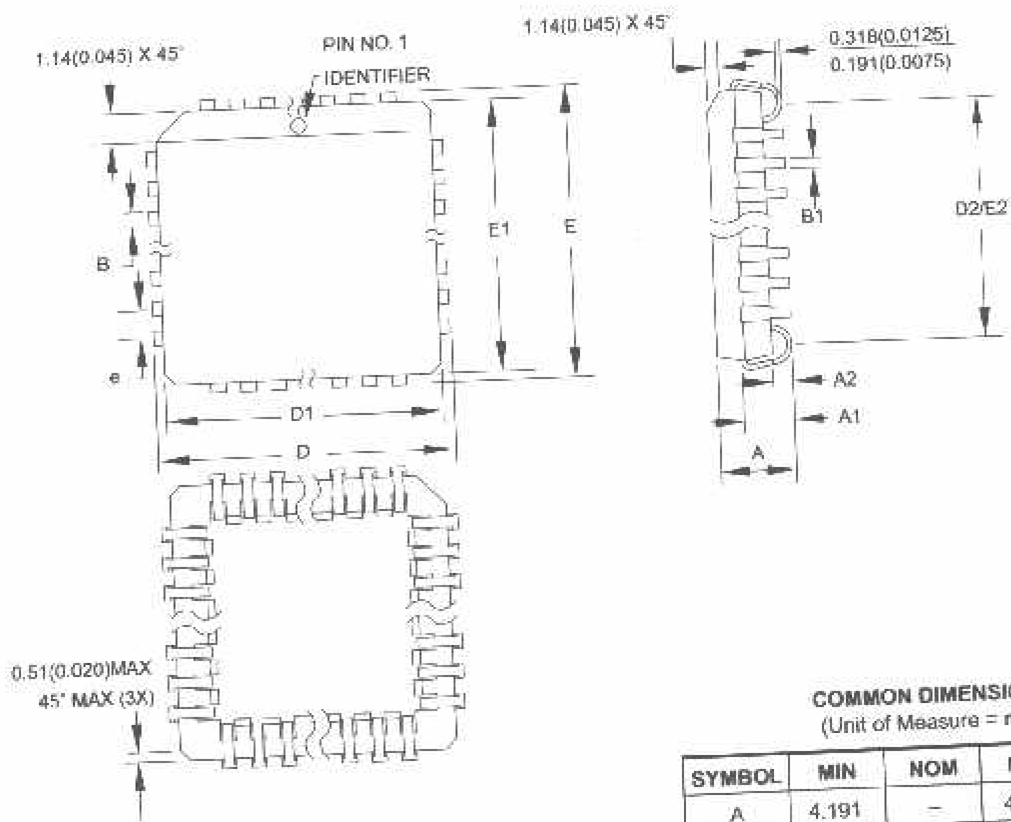
SYMBOL	MIN	NOM	MAX	NOTE
A	–	–	1.20	
A1	0.05	–	0.15	
A2	0.95	1.00	1.05	
D	11.75	12.00	12.25	
D1	9.90	10.00	10.10	Note 2
E	11.75	12.00	12.25	
E1	9.90	10.00	10.10	Note 2
B	0.30	–	0.45	
C	0.09	–	0.20	
L	0.45	–	0.75	
e	0.80 TYP			

...es:
1. This package conforms to JEDEC reference MS-026, Variation ACB.
2. Dimensions D1 and E1 do not include mold protrusion. Allowable protrusion is 0.25 mm per side. Dimensions D1 and E1 are maximum plastic body size dimensions including mold mismatch.
3. Lead coplanarity is 0.10 mm maximum.

10/5/2001

	TITLE	DRAWING NO.	REV.
2325 Orchard Parkway San Jose, CA 95131	**44A,** 44-lead, 10 x 10 mm Body Size, 1.0 mm Body Thickness, 0.8 mm Lead Pitch, Thin Profile Plastic Quad Flat Package (TQFP)	44A	B

PLCC



COMMON DIMENSIONS
(Unit of Measure = mm)

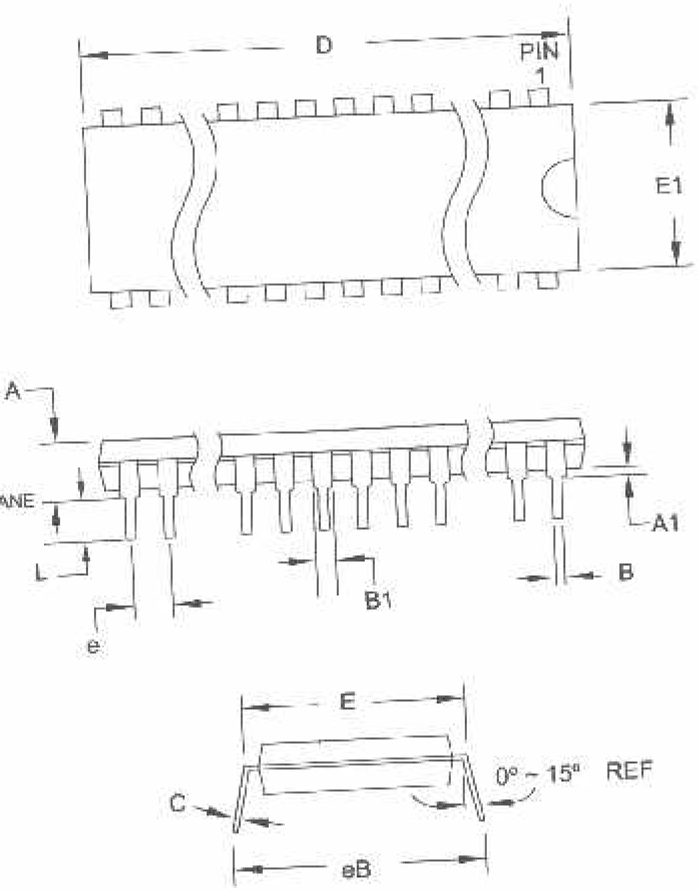
SYMBOL	MIN	NOM	MAX	NOTE
A	4.191	–	4.572	
A1	2.286	–	3.048	
A2	0.508	–	–	
D	17.399	–	17.653	
D1	16.510	–	16.662	Note 2
E	17.399	–	17.653	
E1	16.510	–	16.662	Note 2
D2/E2	14.986	–	16.002	
B	0.660	–	0.813	
B1	0.330	–	0.533	
e	1.270 TYP			

Notes:
1. This package conforms to JEDEC reference MS-018, Variation AC.
2. Dimensions D1 and E1 do not include mold protrusion. Allowable protrusion is .010"(0.254 mm) per side. Dimension D1 and E1 include mold mismatch and are measured at the extreme material condition at the upper or lower parting line.
3. Lead coplanarity is 0.004" (0.102 mm) maximum.

10/04/01

	TITLE	DRAWING NO.	REV.
2325 Orchard Parkway San Jose, CA 95131	**44J**, 44-lead, Plastic J-leaded Chip Carrier (PLCC)	44J	B

PDIP



tes: 1. This package conforms to JEDEC reference MS-011, Variation AC.
2. Dimensions D and E1 do not include mold Flash or Protrusion.
Mold Flash or Protrusion shall not exceed 0.25 mm (0.010").

COMMON DIMENSIONS
(Unit of Measure = mm)

SYMBOL	MIN	NOM	MAX	NOTE
A	–	–	4.826	
A1	0.381	–	–	
D	52.070	–	52.578	Note 2
E	15.240	–	15.875	
E1	13.462	–	13.970	Note 2
B	0.356	–	0.559	
B1	1.041	–	1.651	
L	3.048	–	3.556	
C	0.203	–	0.381	
eB	15.494	–	17.526	
e	2.540 TYP			

09/28/01

	TITLE	DRAWING NO.	REV.
2325 Orchard Parkway San Jose, CA 95131	**40P6**, 40-lead (0.600"/15.24 mm Wide) Plastic Dual Inline Package (PDIP)	40P6	B

GENERAL

1.1 General

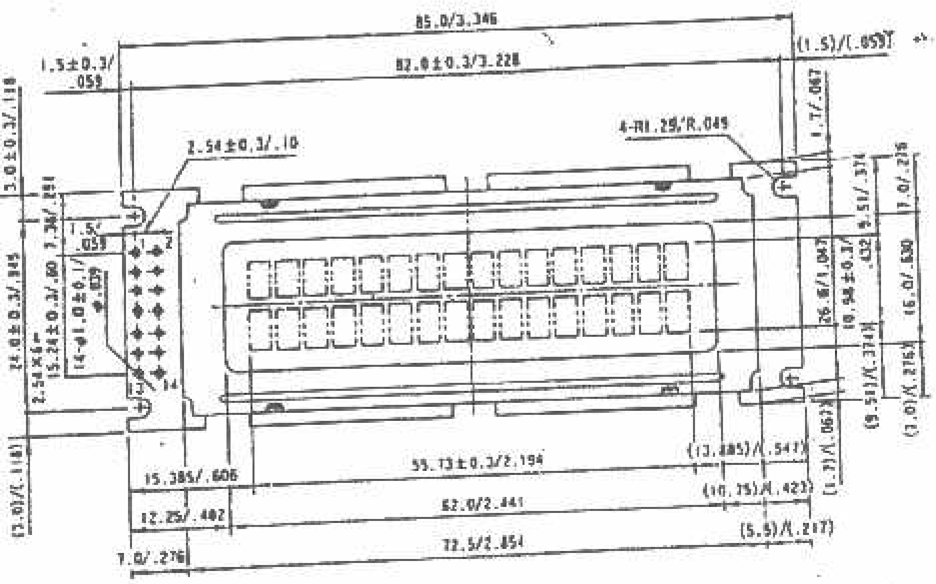
The M1632 is a low-power-consumption dot-matrix liquid crystal display (LCD) module with a high-contrast wide-view TN LCD panel and a CMOS LCD drive controller built in. The controller has a built-in character generator ROM/RAM, and display data RAM. All the display functions are controlled by instructions and the module can easily be interfaced with an MPU. This makes the module applicable to a wide range of purposes including terminal display units for microcomputers and display units for measuring gages.

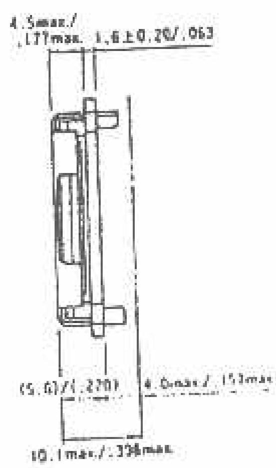
1.2 Features

- 16-character, two-line TN liquid crystal display of 5 x 7 dot matrix + cursor
- Duty ratio: 1/16
- Character generator ROM for 192 character types
  (character font: 5 x 7 dot matrix)
- Character generator RAM for eight character types (program write)
  (character font: 5 x 7 dot matrix)
- 80 x 8 bit display data RAM (80 characters maximum)
- Interface with four-bit and eight-bit MPUs possible
- Display data RAM and character generator RAM readable from MPU
- Many instruction functions

  Display Clear, Cursor Home, Display ON/OFF, Cursor ON/OFF, Display Character Blink, Cursor Shift, and Display Shift
- Built-in oscillator circuit
- +5 V single power supply
- Built-in automatic reset circuit at power-on
- CMOS process
- Operating temperature range: 0°C to 50°C

3 Dimensions Diagram





Unit : mm/inch
General tolerance : ±0.5 mm

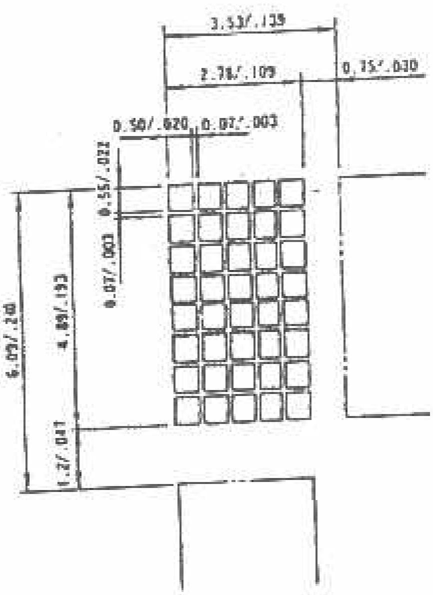
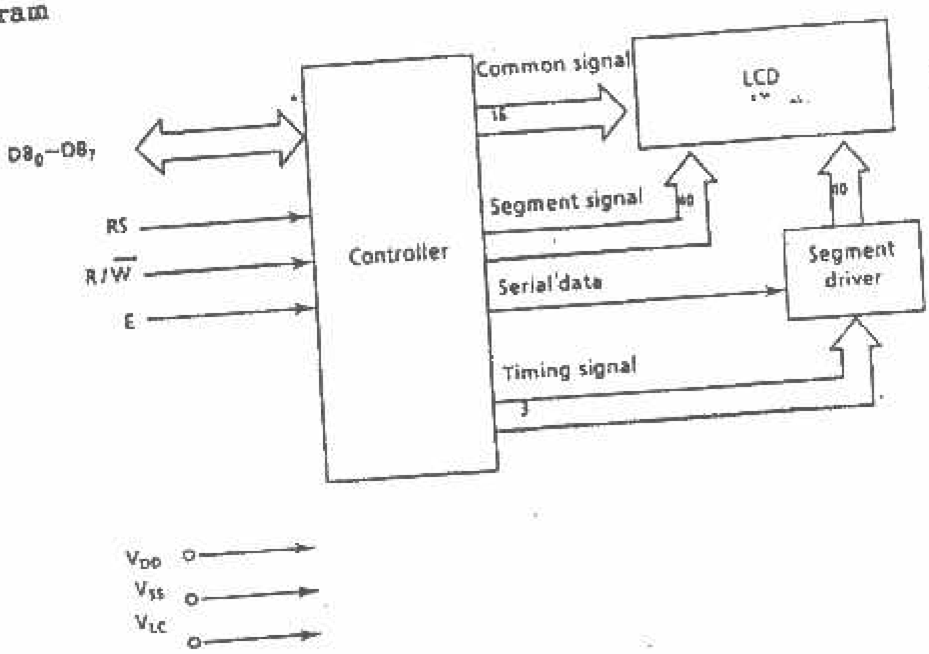


Figure 1 Dimensions diagram

No.	Symbol	Level	Function	
1	Vss	-	Power Supply	0V (GND)
2	Vcc	-		5V ±10%
3	Vee	-		for LCD Drive
4	RS	H/L	H: Data Input L: Instruction Input	
5	R/W	H/L	H:READ L:WRITE	
6	E	H, ⌐_	Enable Signal	
7	DB0	H/L	Data Bus	
8	DB1	H/L		
9	DB2	H/L		
10	DB3	H/L		
11	DB4	H/L		
12	DB5	H/L		
13	DB6	H/L		
14	DB7	H/L		
15	V+ BL	-	Back Light Supply	4 - 4.2V 50-200mA
16	V- BL	-		0V (GND)

Block Diagram



Absolute Maximum Ratings

$V_{SS} = 0\,V$

Item	Symbol	Standard	Unit	Remarks
Power supply voltage	V_{DD}	-0.3 to $+7.0$	V	
	V_{LC}	$V_{DD} - 13.5$ to $V_{DD} + 0.3$	V	
Input voltage	V_{in}	-0.3 to $V_{DD} + 0.3$	V	
Operating temperature	T_{opr}	0 to $+50$	°C	
Storage temperature	T_{stg}	-20 to $+60$	°C	At 50% RH

Electrical Characteristics

$V_{DD} = 5\,V \pm 5\%$, $V_{SS} = 0\,V$, $T_A = 0°C$ to $50°C$

Item		Symbol	Conditions	Standard			Unit
				Min.	Typ.	Max.	
Input voltage	High	V_{IH1}		2.2	–	V_{DD}	V
	Low	V_{IL1}		0	–	0.6	V
Output voltage (TTL)	High	V_{OH1}	$-I_{OH} = 0.205$ mA	2.4	–	–	V
	Low	V_{OL1}	$I_{OL} = 1.2$ mA	–	–	0.4	V
Output voltage (CMOS)	High	V_{OH2}	$-I_{OH} = 0.04$ mA	$0.9V_{DD}$	–	–	V
	Low	V_{OL2}	$I_{OL} = 0.04$ mA	–	–	$0.1V_{DD}$	V
Power supply voltage		V_{DD}		4.75	5.00	5.25	V
		V_{LC}	$V_{DD} = 5\,V$, $T_A = 25°C$	–	0.25	–	V
Current consumption		I_{DD}		–	2.0	3.0	mA
		I_{LC}	$V_{LC} = 0.25V$	–	–	1.0	mA
Clock oscillation freq.		f_{osc}	Resistance oscillation	190	270	350	kHz

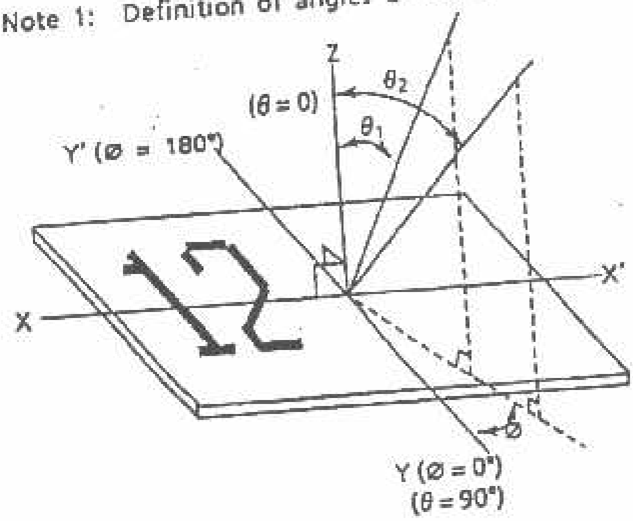
1.7 Optical Characteristics

1.7.1 Optical characteristics

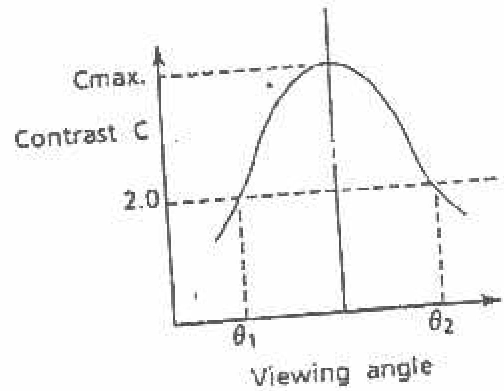
Maximum viewing angle: 6 o'clock ($\varnothing$ = 0°)
T_A = 25°C, V_{opr} = 4.75 V

Item	Symbol	Conditions	Min.	Typ.	Max.	Remarks
Viewing angle	$\theta_2 - \theta_1$	$C \geq 2.0$, $\varnothing = 0°$	35	–	–	See Notes 1 and 2.
Contrast	C	$\theta = 25°$, $\varnothing = 0°$	5	8	–	See Note 3.
Rise time	t_{on}	$\theta = 25°$, $\varnothing = 0°$	–	60 ms	70 ms	See Note 4.
Fall time	t_{off}	$\theta = 25°$, $\varnothing = 0°$	–	150 ms	170 ms	See Note 4.

Note 1: Definition of angles $\varnothing$ and θ

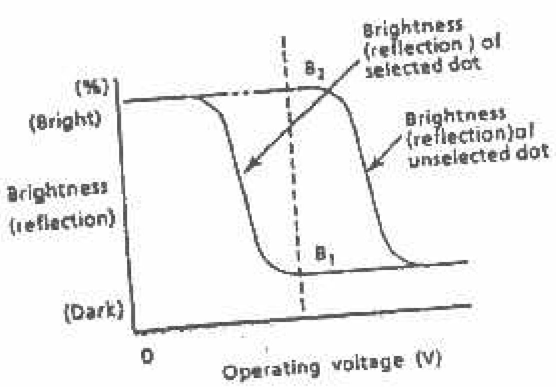


Note 2: Definition of viewing angles θ_1 and θ_2

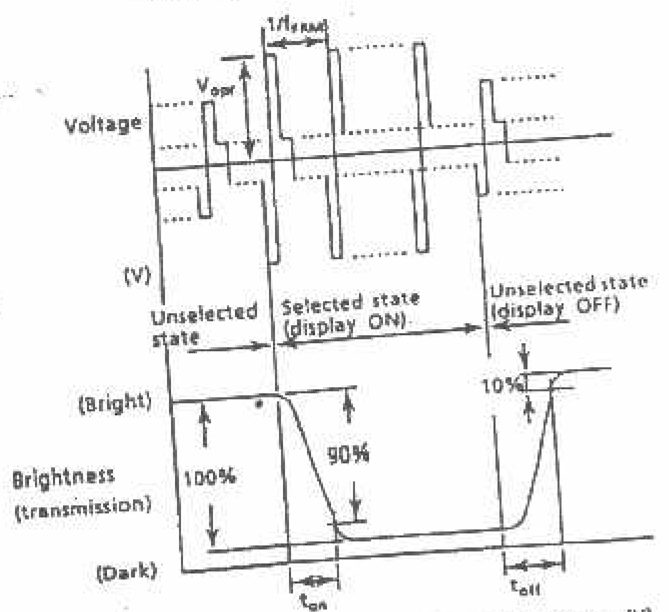


Note 3: Definition of contrast C

$$C = \frac{\text{Brightness (reflection) of unselected dot (B2)}}{\text{Brightness (reflection) of selected dot (B1)}}$$



Note 4: Definition of response time



V_{opr} : Operating voltage (V)
f_{FRM} : Frame frequency (Hz)
t_{on} : Response time (rise)(ms)
t_{off} : Response time (fall)(ms)

.7.2 Recommended operating voltage

The viewing angle and screen contrast of the LCD panel can be varied by changing the liquid crystal operating voltage (V_{opr}), that is V_{LC}.*

The optical characteristics is influenced by an ambient temperature. The recommended value of V_{opr} for an ambient temperatures are shown below.

Temperature (℃)	0	10	25	40	50
Voltage V_{opr} (V)	5.00	4.90	4.75	4.60	4.50

$V_{opr} = V_{DD} - V_{LC}$

PERATING INSTRUCTIONS

.1 Terminal Functions

Table 1 Terminal functions

gnal name	No. of terminals	I/O	Destination	Function
DB$_0$ to DB$_3$	4	I/O	MPU	Tristate bidirectional lower four data buses: Data is read from the module to the MPU or written to the module from the MPU through the buses. If the interface data is 4 bits, the signals are not used.
DB$_4$ to DB$_7$	4	I/O	MPU	Tristate bidirectional upper four data buses: Data is read from the module to the MPU or written to the module from the MPU through the buses. DB$_7$ is also used as a busy flag.
E	1	Input	MPU	Operation start signal: The signal activates data write or read.
R/$\overline{W}$	1	Input	MPU	Read (R) and Write ($\overline{W}$) selection signals 0 : Write 1 : Read
RS	1	Input	MPU	Register selection signals 0 : Instruction register (Write) Busy flag and address counter (Read) 1 : Data register (Write and Read)
V_{LC}	1	–	Power supply	Power supply terminal for driving liquid crystal display: The screen contrast can be varied by changing V_{LC}.
V_{DD}	1	–	Power supply	+5 V
V_{SS}	1	–	Power supply	Ground terminal: 0 V

Basic Operations

2.2.1 Registers

The controller has two kinds of eight-bit registers: the instruction register (IR) and the data register (DR). They are selected by the register select (RS) signal as shown in Table 2.

The IR stores instruction codes such as Display Clear and Cursor Shift, and the address ~~information~~ of display data RAM (DD RAM) and character generator RAM ~~(CG RAM)~~. They can be written from the MPU, but cannot be read to the MPU.

The DR temporarily stores data to be written into DD RAM or CG RAM, or read from DD RAM or CG RAM. When data is written into DD RAM or CG RAM from the MPU, the data in the DR is automatically written into DD RAM or CG RAM by internal operation. However, when data is read from DD RAM or CG RAM, the necessary data address is written into the IR. The specified data is read out to the DR and then the MPU reads it from the DR. After the read operation, the next address is set and DD RAM or CG RAM data at the address is read into the DR for the next read operation.

Table 2 Register selection

RS	$R/\overline{W}$	Operation
0	0	IR selection, IR write. Internal operation : Display clear
0	1	Busy flag (DB_7) and address counter (DB_0 to DB_6) read
1	0	DR selection, DR write. Internal operation : DR to DD RAM or CG RAM
1	1	DR selection, DR read. Internal operation : DD RAM or CG RAM to DR

2.2.2 Busy flag (BF)

The flag indicates whether the module is ready to accept the next instruction. As shown in Table 2, the signal is output to DB_7 if RS = 0 and $R/\overline{W}$ = 1. If the value is 1, the module is working internally and the instruction cannot be accepted. If the value is 0, the next instruction can be written. Therefore, the flag status needs to be checked before executing an instruction. If an instruction is executed without checking the flag status, wait for more than the execution time shown by 2.4 Instruction Outline.

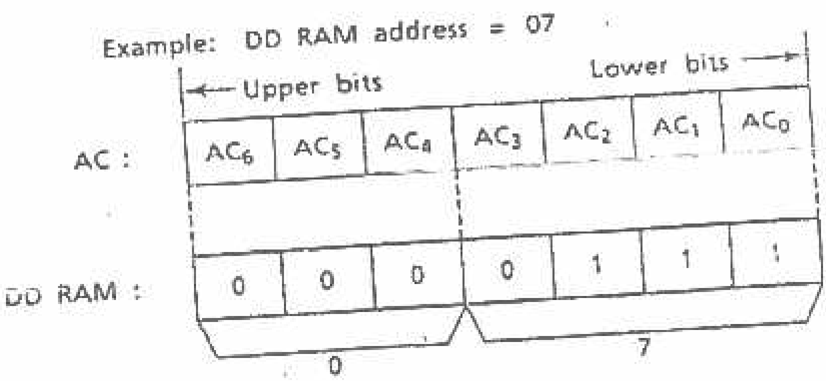
2.2.3 Address counter (AC)

The counter specifies an address when data is written into DD RAM or CG RAM and the data stored in DD RAM or CG RAM is read out. If an Address Set instruction (for DD RAM or CG RAM) is written in the IR, the address information is transferred from the IR to the AC. When display data is written into or read from DD RAM or CG RAM, the AC is automatically incremented or decremented by one according to the Entry Mode Set. The contents of the AC are output to DB_0 to DB_6 as shown in Table 2 if RS = 0 and $R/\overline{W}$ = 1.

2.2.4 Display data RAM (DD RAM)

DD RAM has a capacity of up to 80 × 8 bits and stores display data of 80 eight-bit character codes. Some storage areas of DD RAM which are not used for display can be used as general data RAM.

The DD RAM address to be set in the AC is expressed in hexadecimal form as follows.



00_H to $0F_H$ of the DD RAM address is set in the line 1, and 40_H to $4F_H$ in the line 2.

Note : The addresses in the digit 16 of line 1 and the digit 1 of line 2 are not consecutive.

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	Display digit
Line 1	00	01	02	03	04	05	06	07	08	09	0A	0B	0C	0D	0E	0F	DD RAM address
Line 2	40	41	42	43	44	45	46	47	48	49	4A	4B	4C	4D	4E	4F	

If the display is shifted, DD RAM address 00_H to 27_H are displayed in line 1 and 40_H to 67_H in line 2. The following figures are examples of display shifts.

*Left shift

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	Display digit
Line 1	01	02	03	04	05	06	07	08	09	0A	0B	0C	0D	0E	0F	10	DD RAM address
Line 2	41	42	43	44	45	46	47	48	49	4A	4B	4C	4D	4E	4F	50	

*Right shift

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	Display digit
Line 1	27	00	01	02	03	04	05	06	07	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	DD RAM address
Line 2	67	40	41	42	43	44	45	46	47	48	49	4A	4B	4C	4D	4E	

5 Character generator ROM (CG ROM)

Character generator ROM generates 192 types of 5 x 7 dot-matrix character patterns from eight-bit character codes.

Table 3 shows the correspondence between the CG ROM character codes and character patterns.

6 Character generator RAM (CG RAM)

CG RAM is used to create character patterns freely by programming. Eight types of character patterns can be written.

Table 4 shows the character patterns created from CG RAM addresses and data. To display a created character pattern, the character code in the left column of the table is written into DD RAM corresponding to the display position (digit). The areas not used for display are available as general data RAM.

Table 3 Correspondence between character codes and character patterns

per bit 4 bit / er bit	0 0000	2 0010	3 0011	4 0100	5 0101	6 0110	7 0111	1010	1011	1100	1101	1110	1111
× ×0000	CG RAM (1)		0	@	P	`	p		ー	タ	ミ	α	p
× ×0001	(2)	!	1	A	Q	a	q	。	ア	チ	ム	ä	q
× ×0010	(3)	"	2	B	R	b	r	「	イ	ツ	メ	β	θ
× ×0011	(4)	#	3	C	S	c	s	」	ウ	テ	モ	ε	∞
× ×0100	(5)	$	4	D	T	d	t	、	エ	ト	ヤ	μ	Ω
× ×0101	(6)	%	5	E	U	e	u	・	オ	ナ	ユ	σ	ü
× ×0110	(7)	&	6	F	V	f	v	ヲ	カ	ニ	ヨ	ρ	Σ
× ×0111	(8)	'	7	G	W	g	w	ァ	キ	ヌ	ラ	g	π
× ×1000	(1)	(	8	H	X	h	x	ィ	ク	ネ	リ	√	x̄
× ×1001	(2)	)	9	I	Y	i	y	ゥ	ケ	ノ	ル	$^{-1}$	y
× ×1010	(3)	*	:	J	Z	j	z	ェ	コ	ハ	レ	j	千
× ×1011	(4)	+	;	K	[	k	{	ォ	サ	ヒ	ロ	^{x}	万
× ×1100	(5)	,	<	L	¥	l			ャ	シ	フ	ワ	¢	円
× ×1101	(6)	-	=	M	]	m	}	ュ	ス	ヘ	ン	Ⱡ	÷
× ×1110	(7)	.	>	N	^	n	→	ョ	セ	ホ	゛	ñ	
× ×1111	(8)	/	?	O	_	o	←	ッ	ソ	マ	゜	ö	█

Table 4 Relationships between CG RAM addresses and character codes (DD RAM) and character patterns (CG RAM data)

Character code (DD RAM data) 7 6 5 4 3 2 1 0 (← Upper bit, Lower bit →)	CG RAM address 5 4 3 (← Upper bit)	CG RAM address 2 1 0 (Lower bit →)	Character pattern (CG RAM data) 7 6 5 4 3 2 1 0 (← Upper bit, Lower bit →)	
0 0 0 0 * 0 0 0	0 0 0	0 0 0	* * * 1 1 1 1 0	Example of character pattern (R)
		0 0 1	1 0 0 0 1	
		0 1 0	1 0 0 0 1	
		0 1 1	1 1 1 1 0	
		1 0 0	1 0 1 0 0	
		1 0 1	1 0 0 1 0	
		1 1 0	1 0 0 0 1	
		1 1 1	* * * 0 0 0 0 0	← Cursor position
0 0 0 0 * 0 0 1	0 0 1	0 0 0	* * * 1 0 0 0 1	Example of character pattern (Y)
		0 0 1	0 1 0 1 0	
		0 1 0	1 1 1 1 1	
		0 1 1	0 0 1 0 0	
		1 0 0	1 1 1 1 1	
		1 0 1	0 0 1 0 0	
		1 1 0	0 0 1 0 0	
		1 1 1	* * * 0 0 0 0 0	
		0 0 0	* * *	
		0 0 1		
0 0 0 0 * 1 1 1	1 1 1	1 0 0		
		1 0 1		
		1 1 0		
		1 1 1	* * *	

Notes: • In CG RAM data, 1 corresponds to Selection and 0 to Non-selection on the display.

- Character code bits 0 to 2 and CG RAM address bits 3 to 5 correspond with each other (three bits, eight types).

- CG RAM address bits 0 to 2 specify a line position for a character pattern. Line 8 of a character pattern is the cursor position where the logical sum of the cursor and CG RAM data is displayed. Set the data of line 8 to 0 to display the cursor. If the data is changed to 1, one bit lights, regardless of the cursor.

The character pattern column positions correspond to CG RAM data bits 0 to 4 and bit 4 comes to the left end. CG RAM data bits 5 to 7 are not displayed but can be used as general data RAM.

When reading a character pattern from CG RAM, set to 0 all of character code bits 4 to 7. Bits 0 to 2 determine which pattern will be read out. Since bit 3 is not valid, 00_H and 08_H select the same character.

Timing Characteristics

.3.1 Write timing characteristics

$V_{DD} = 5.0\,V \pm 5\%$, $V_{SS} = 0\,V$, T_A = 0°C to 50°C

Item		Symbol	Standard		Unit
			Min.	Max.	
Enable cycle time		t_{CYCE}	1000	–	ns
Enable pulse width	High level	PW_{EH}	450	–	ns
Enable rise and fall time		t_{Er}, t_{Ef}	–	25	ns
Setup time	RS, R/$\overline{W}$ — E	t_{AS}	140	–	ns
Address hold time		t_{AH}	10	–	ns
Data setup time		t_{DSW}	195	–	ns
Data hold time		t_H	10	–	ns

Write operation

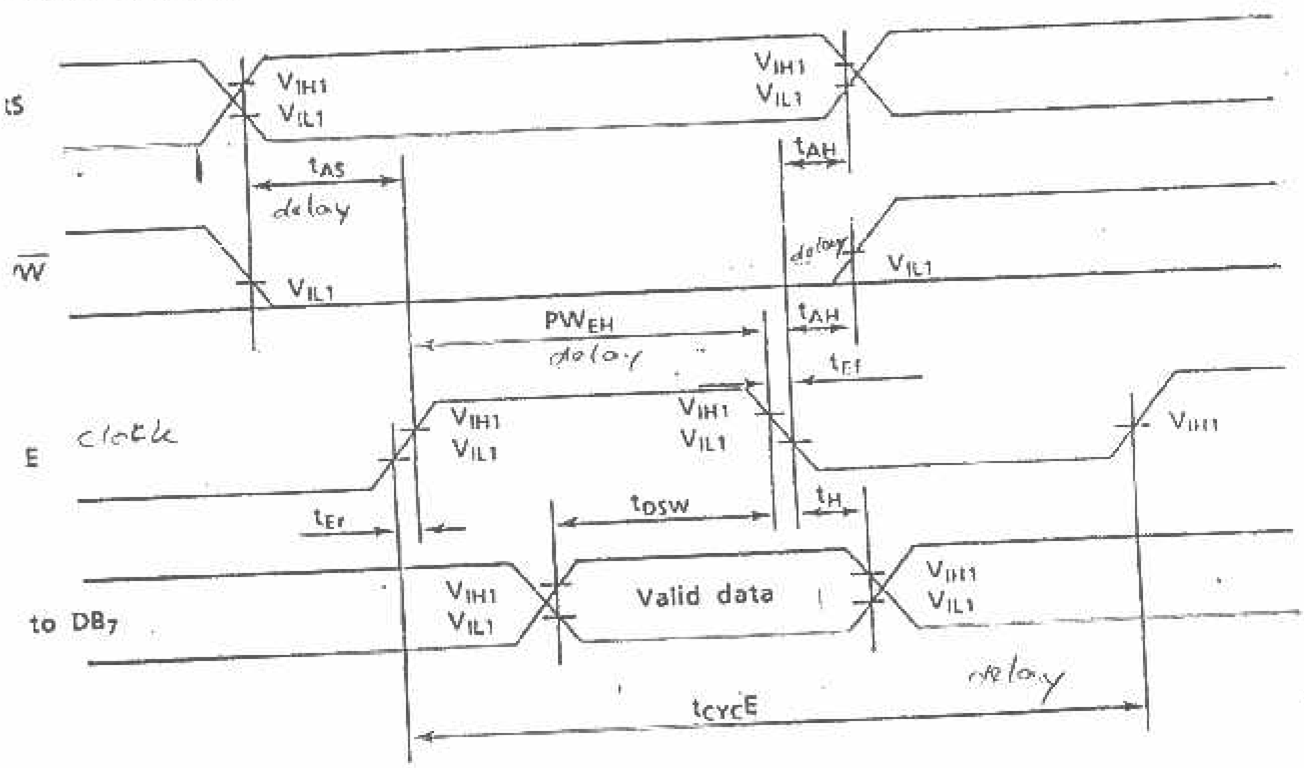


Figure 3 Data write from MPU to module

3.2 Read timing characteristics

$V_{DD} = 5.0\,V \pm 5\%$, $V_{SS} = 0\,V$; $T_A = 0°C$ to $50°C$

Item		Symbol	Standard Min.	Standard Max.	Unit
Enable cycle time		t_{cycE}	1000	–	ns
Enable pulse width	High level	PW_{EH}	450	–	ns
Enable rise and fall time		t_{Er}, t_{Ef}	–	25	ns
Setup time	RS, R/$\overline{W}$ — E	t_{AS}	140	–	ns
Address hold time		t_{AH}	10	–	ns
Data delay time		t_{DDR}	–	320	ns
Data hold time		t_H	20	–	ns

Read operation

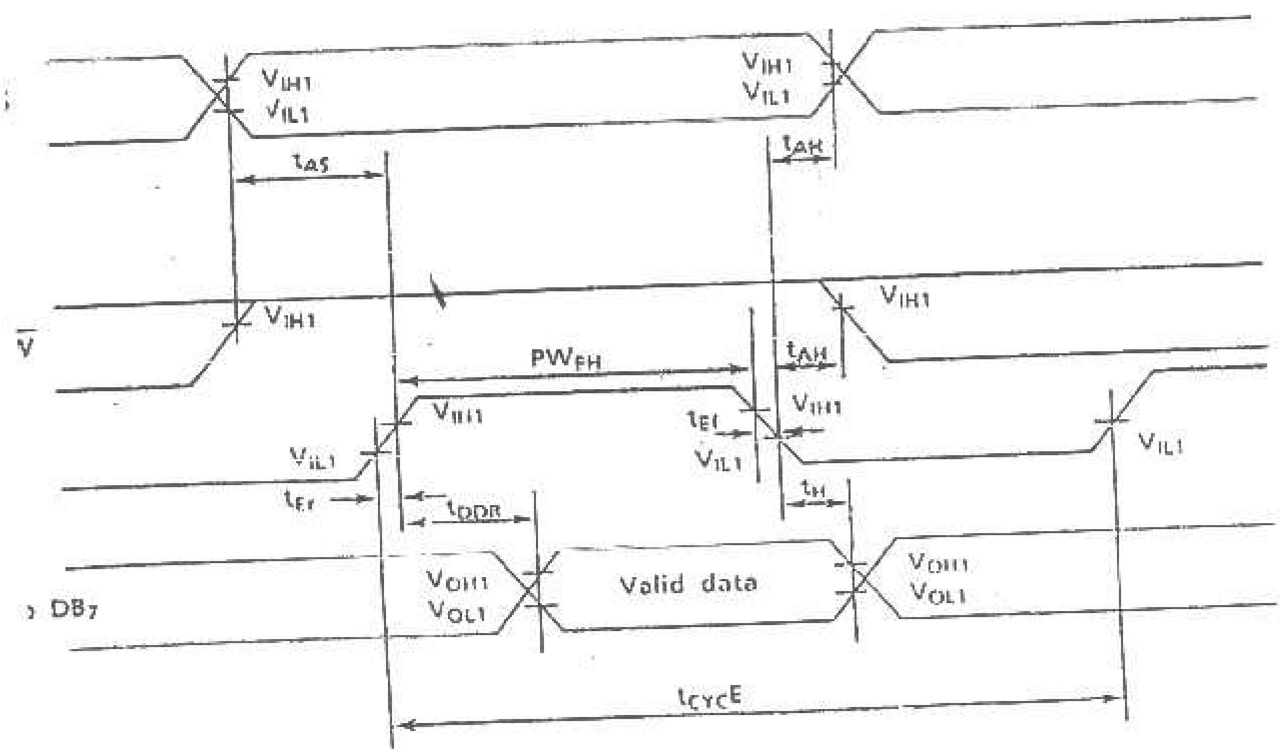


Figure 4 Data read from module to MPU

Instruction Outline

Table 5 List of instructions

nstruction	RS	R/W	DB_7	DB_6	DB_5	DB_4	DB_3	DB_2	DB_1	DB_0	Function	Execution time
play clear	0	0	0	0	0	0	0	0	0	1	Clears all display and returns cursor to home position (address 0)	1.64 ms
[illegible]	0	0	0	0	0	0	0	0	1	*	Returns cursor to home position. Shifted display returns to home position and DD RAM contents do not change.	1.64 ms
try Mode Set	0	0	0	0	0	0	0	1	I/D	S	Sets direction of cursor movement and whether display will be shifted when data is written or read	40 µs
play ON / OFF ntrol	0	0	0	0	0	0	1	D	C	B	Turns ON/OFF total display (D) and cursor (C), and makes cursor position column start blinking (B)	40 µs
rsor/Display Shift	0	0	0	0	0	1	S/C	R/L	*	*	Moves cursor and shifts display without changing DD RAM contents	40 µs
nction Set	0	0	0	0	1	DL	*	*	*	*	Sets interface data length (DL)	40 µs
RAM Address	0	0	0	1	A_{CG}						Sets CG RAM address to start transmitting or receiving CG RAM data	40 µs
RAM Address	0	0	1	A_{DD}							Sets DD RAM address to start transmitting or receiving DD RAM data	40 µs
/Address Read	0	1	BF	AC							Reads BF indicating module in internal operation and AC contents (used for both CG RAM and DD RAM)	0 µs
ata Write to CG AM or DD RAM	1	0	Write Data								Writes data into DD RAM or CG RAM	40 µs
[illegible] Read from G RAM or DD AM	1	1	Read Data								Reads data from DD RAM or CG RAM	40 µs

nvalid bit
CG RAM address
DD RAM address

I/D = 1 : Increment
I/D = 0 : Decrement

S = 1 : Display shift
S = 0 : No display shift

D = 1 : Display ON
D = 0 : Display OFF

C = 1 : Cursor ON
C = 0 : Cursor OFF

B = 1 : Blink ON
B = 0 : Blink OFF

S/C = 1 : Display shift
S/C = 0 : Cursor movement

R/L = 1 : Right shift
R/L = 0 : Left shift

DL = 1 : 8 bits
DL = 0 : 4 bits

BF = 1 : Internal operation in progress
BF = 0 : Instruction can be accepted

struction Details

Display Clear

	RS	R/$\overline{W}$	DB_7							DB_0
Code	0	0	0	0	0	0	0	0	0	1

Display Clear clears all display and returns cursor to home position (address 0). Space code 20 (hexadecimal) is written into all the addresses of DD RAM, and DD RAM address 0 is set to the AC. If shifted, the display returns to the original position. After execution of the Display Clear instruction, the entry mode is incremented.

Note : When executing the Display Clear instruction, follow the restrictions listed in Table 6.

Cursor Home

	RS	R/$\overline{W}$	DB_7							DB_0
Code	0	0	0	0	0	0	0	0	1	*

* : Invalid bit

Cursor Home returns cursor to home position (address 0). DD RAM address 0 is set to the AC. The cursor returns to the home position. If shifted, the display returns to the original position. The DD RAM contents do not change. If the cursor or blinking is ON, it returns to the left side.

Note : When executing the Cursor Home instruction, follow the restrictions listed in Table 6.

Table 6 Restrictions on execution of Display Clear and Cursor Home Instructions

Conditions of use	Restrictions
When executing the Display Clear or Cursor Home instruction when the display is shifted (after execution of Display Shift instruction)	The Cursor Home instruction should be executed again immediately after the Display Clear or Cursor Home instruction is executed. Do not [illegible] 400/f_{osc}* second after the first execution. Example: 1.5 ms, 3 ms, 4.5 ms for f_{osc} = 270 kHz *f_{osc}: Oscillation frequency
When 23_H, 27_H, 63_H, or 67_H is used as a DD RAM address to execute Cursor Home instruction	Before executing the Cursor Home instruction, the data of the four DD RAM addresses [illegible] and saved. After execution, write the data again in DD RAM. (This restriction is necessary to prevent the contents of the [illegible] from being destroyed after the Cursor Home instruction has been executed.)

Entry Mode Set

	RS	R/$\overline{W}$	DB_7							DB_0
Code	0	0	0	0	0	0	0	1	I/D	S

Entry Mode Set sets the direction of cursor movement and whether display will be shifted.

I/D : The DD RAM address is incremented or decremented by one when a character code is written into or read from DD RAM. This is also true for writing into or reading from CG RAM.

When I/D = 1, the address is incremented by one and the cursor or blink moves to the right.

When I/D = 0, the address is decremented by one and the cursor or blink moves to the left.

S : If S = 1, the entire display is shifted either to the right or left for writing into DD RAM. The cursor position does not change, only the display moves. There is no display shift for reading from DD RAM.

When S = 1 and I/D = 1, the display shifts to the left.
When S = 1 and I/D = 0, the display shifts to the right.

If S = 0, the display does not shift.

Display ON/OFF Control

	RS	R/$\overline{W}$	DB_7							DB_0
Code	0	0	0	0	0	0	1	D	C	B

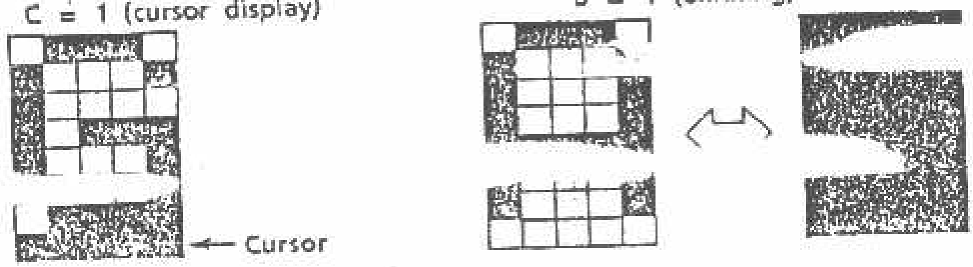
Display ON/OFF Control turns the total display and the cursor ON and OFF, and makes the cursor position start blinking. Cursor ON/OFF and blinking is done at the column indicated by the specified DD RAM address by the AC.

D : When D = 1, the display is turned ON.
When D = 0, the display is turned OFF.
If D = 0 is used, display data remains in DD RAM. Change 0 to 1 to display data.

C : When C = 1, the cursor is displayed.
When C = 0, the cursor is not displayed.
The cursor is displayed in the dot line below the 5 x 7 dot-matrix character fonts. If the cursor is OFF, display data is written into DD RAM in the order specified by I/D.

B : When B = 1, the character at the cursor position starts blinking.
When B = 0, it does not blink.
For blinking, all-black dots and the character are switched about every 0.4 seconds. The cursor and blinking can be set at the same time.

Example: C = 1 (cursor display) B = 1 (blinking)



Cursor/Display Shift

	RS	R/W	DB_7							DB_0	
Code	0	0	0	0	0	1	S/C	R/L	*	*	*: Invalid bit

Cursor/Display Shift moves the cursor and shifts the display without changing the DD RAM contents.
The cursor position and the AC contents match. This instruction is available for display correction and retrieval because the cursor position or display can be shifted without writing or reading display data. Since the DD RAM capacity is 40-character and two lines, the cursor is shifted from digit 40 of line 1 to digit 1 of line 2. Displays of lines 1 and 2 are shifted at the same time. Therefore, the display pattern of line 2 is not shifted to line 1.

S/C	R/L	Operation
0	0	The cursor position is shifted to the left (the AC decrements one).
0	1	The cursor position is shifted to the right (the AC increments one).
1	0	The entire display is shifted to the left with the cursor.
1	1	The entire display is shifted to the right with the cursor.

Note: If only display shift is done, the AC contents do not change.

Function Set

	RS	R/$\overline{W}$	DB_7							DB_0
Code	0	0	0	0	1	DL	1	*	*	*

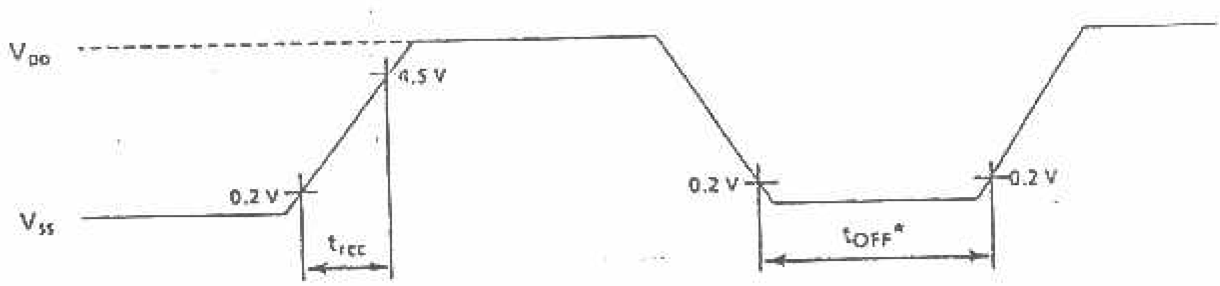
* : Invalid bit

Function Set sets the interface data length.

DL : Interface data length
When DL = 1, the data length is set at eight bits (DB_7 to DB_0).
When DL = 0, the data length is set at four bits (DB_7 to DB_4).
The upper four bits are transferred first, then the lower four bits follow.

The Function Set instruction must be executed prior to all other instructions except for Busy Flag/Address Read. If another instruction is executed first, no function instruction except changing the interface data length can be executed.

Remarks: Initialization
The system is automatically initialized at power-on if the following power supply conditions are satisfied.



$0.1\ ms \le t_{rcc} \le 10\ ms$ $\qquad$ $t_{OFF} \ge 1\ ms$

*t_{OFF}: Time when power supply is OFF if cut instantaneously or turned ON and OFF repeatedly

he following instructions are executed for initialization.

- 5 x 7 dot-matrix character font: 1/8 duty
- Display clear

· Function Set	DL = 1: Interface data length: 8 bits
· Display ON/OFF Control	D = 0: Display OFF C = 0: Cursor OFF B = 0: Blink OFF
· Entry mode	I/O = 1: Increment S = 0: No display shift

Since the condition is not suitable for the M1632, further function setting is ecessary.

If automatic initialization is not executed because the above power supply onditions are not satisfied, use the instruction from next page on.

Interface data length : Eight bits

Power-on

↓

Wait for 15 ms or more after V_{DD} reaches 4.5 V.

↓

S	R/W	DB_7	-	-	-	-	-	-	DB_0
0	0	0	0	1	1	*	*	*	*

(0x) is (33H)

The busy flag cannot be checked before the following instruction: Function Set (interface data length: 8 bits)

↓

Wait for 4.1 ms or more.

↓

S	R/W	DB_7	-	-	-	-	-	-	DB_0
0	0	0	0	1	1	*	*	*	*

The busy flag cannot be checked before the following instruction: Function Set (interface data length: 8 bits)

↓

Wait for 100 μs or more.

↓

S	R/W	DB_7	-	-	-	-	-	-	DB_0
0	0	0	0	1	1	*	*	*	*

The busy flag cannot be checked before the following instruction: Function Set (interface data length: 8 bits)

↓

S	R/W	DB_7	-	-	-	-	-	-	DB_0
0	0	0	0	1	1	1	*	*	*
0	0	0	0	0	0	1	0	0	0
0	0	0	0	0	0	0	0	0	1
0	0	0	0	0	0	0	1	I/D	S

The busy flag can be checked from the following instructions:

Function Set

Display OFF

Display Clear

Entry Mode Set

↓

End of initialization

he following instructions are executed for initialization.

- 5 x 7 dot-matrix character font: 1/8 duty
- Display clear
- Function Set — DL = 1: Interface data length: 8 bits
- Display ON/OFF Control — D = 0: Display OFF
  C = 0: Cursor OFF
  B = 0: Blink OFF
- Entry mode — I/O = 1: Increment
  S = 0: No display shift

Since the condition is not suitable for the M1632, further function setting is ecessary.

If automatic initialization is not executed because the above power supply onditions are not satisfied, use the instruction from next page on.

Interface data length : Eight bits

Power-on

↓

Wait for 15 ms or more after V_{DD} reaches 4.5 V.

↓

RS	R/$\overline{W}$	DB_7	–	–	–	–	–	–	DB_0
0	0	0	0	1	1	*	*	*	*

The busy flag cannot be checked before the following instruction: Function Set (interface data length: 8 bits)

fmk 6 (338)

↓

Wait for 4.1 ms or more.

↓

RS	R/$\overline{W}$	DB_7	–	–	–	–	–	–	DB_0
0	0	0	0	1	1	*	*	*	*

The busy flag cannot be checked before the following instruction: Function Set (interface data length: 8 bits)

↓

Wait for 100 μs or more.

↓

RS	R/$\overline{W}$	DB_7	–	–	–	–	–	–	DB_0
0	0	0	0	1	1	*	*	*	*

The busy flag cannot be checked before the following instruction: Function Set (interface data length: 8 bits)

↓

RS	R/$\overline{W}$	DB_7	–	–	–	–	–	–	DB_0
[illegible]	0	0	0	1	1	1	*	*	*
[illegible]	0	0	0	0	0	1	0	0	0
[illegible]	0	0	0	0	0	0	0	0	1
[illegible]	0	0	0	0	0	0	1	I/D	S

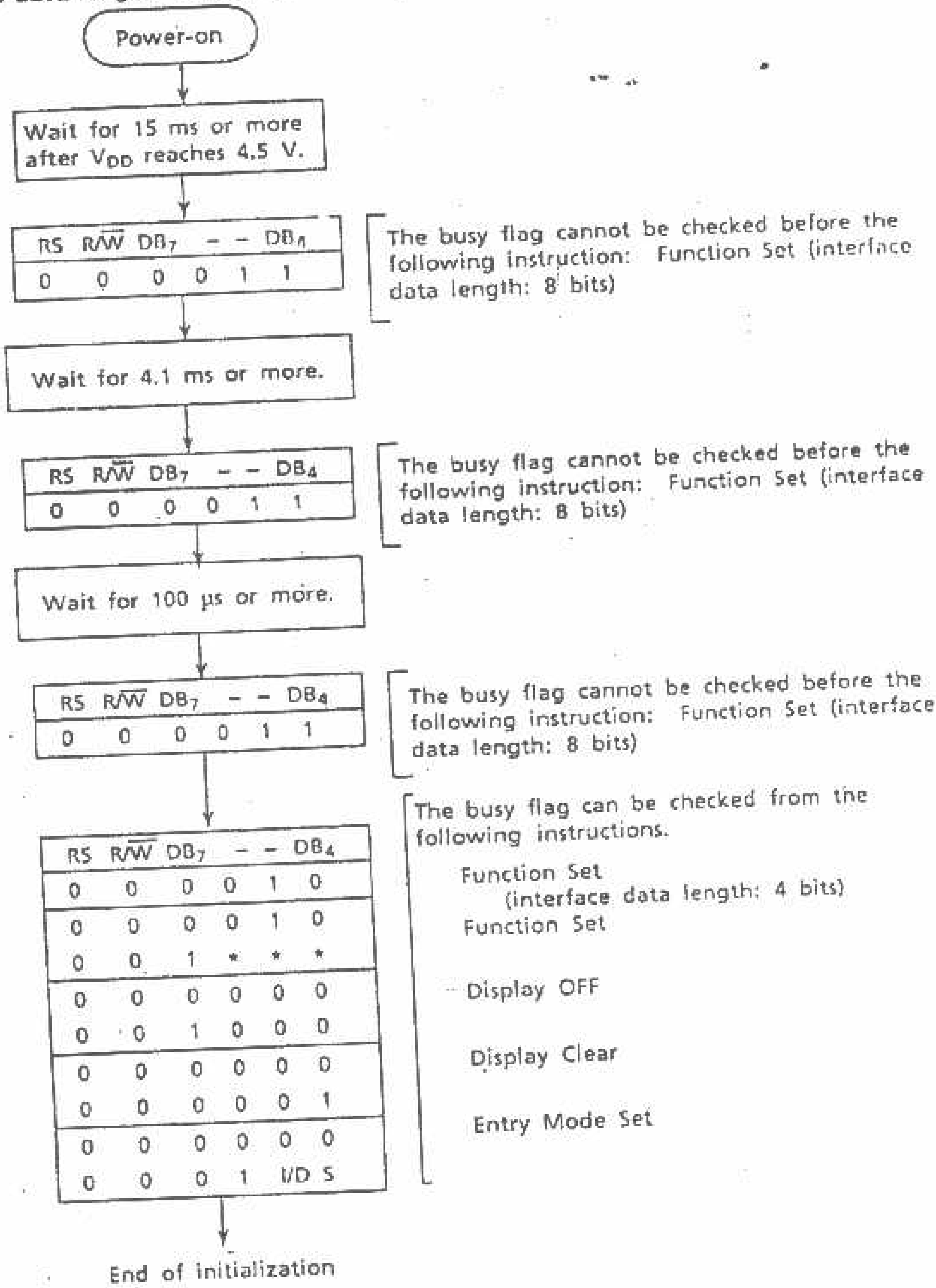
The busy flag can be checked from the following instructions

- Function Set
- Display OFF
- Display Clear
- Entry Mode Set

↓

End of initialization

Interface data length: Four bits



CG RAM Address Set

	RS	R/$\overline{W}$	DB_7							DB_0
Code	0	0	0	1	A	A	A	A	A	A

|← Upper bit Lower bit →|

CG RAM addresses expressed as binary AAAAAA are set to the AC. Then data in CG RAM is written from or read to the MPU.

DD RAM Address Set

	RS	R/$\overline{W}$	DB_7							DB_0
Code	0	0	1	A	A	A	A	A	A	A

|← Upper bit Lower bit →|

DD RAM addresses expressed as binary AAAAAAA are set to the AC. Then data in DD RAM is written from or read to the MPU. The addresses used for display in line 1 (AAAAAAA) are 00_H to 27_H and those for line 2 (AAAAAAA) are 40_H to 67_H.

Busy Flag/Address Read

	RS	R/$\overline{W}$	DB_7							DB_0
Code	0	1	BF	A	A	A	A	A	A	A

|← Upper bit Lower bit →|

The BF signal is read out, indicating that the module is working internally because f the previous instruction.

When BF = 1, the module is working internally and the next instruction cannot be accepted until the BF value becomes 0.

When BF = 0, the next instruction can be accepted.

Therefore, make sure that BF = 0 before writing the next instruction. The AC alues of binary AAAAAAA are read out at the same time as reading the busy flag. he AC addresses are used for both CG RAM and DD RAM but the address set efore execution of the instruction determines which address is to be used.

Data Write to CG RAM or DD RAM

	RS	R/$\overline{W}$	DB_7							DB_0
Code	1	0	D	D	D	D	D	D	D	D
			←Upper bit						Lower bit →	

Binary eight-bit data DDDDDDDD is written into CG RAM or DD RAM. The CG RAM Address Set instruction of (7) or the DD RAM Address Set instruction of (8) before this instruction selects either RAM. After the write operation, the address and display shift are determined by the entry mode setting.

Data Read from CG RAM or DD RAM

	RS	R/$\overline{W}$	DB_7							DB_0
Code	1	1	D	D	D	D	D	D	D	D
			←Upper bit						Lower bit →	

Binary eight-bit data DDDDDDDD is read from CG RAM or DD RAM. The CG RAM Address Set instruction of (7) or the DD RAM Address Set instruction of (8) before this instruction selects either RAM. In addition, either instruction (7) or (8) must be executed immediately before this instruction. If no address set instruction is executed before a read instruction, the first data read becomes invalid. If read instructions are executed consecutively, data is normally read from the second time. However, if the cursor is shifted by the Cursor Shift instruction when reading DD RAM, there is no need to execute an address set instruction because the Cursor Shift instruction does this.
After the read operation, the address is automatically incremented or decremented by one according to the entry mode, but the display is not shifted.

Note : The AC is automatically incremented or decremented by one according to the entry mode after a write instruction is executed to write data in CG RAM or DD RAM. However, the data of the RAM selected by the AC are not read out even if a read instruction is executed immediately afterwards.

Correct data is read out under the following conditions.

- An address set instruction is executed immediately before readout.
- For DD RAM, the Cursor Shift instruction is executed immediately before readout.
- The second, or later, instruction is executed in consecutive execution of read instructions.

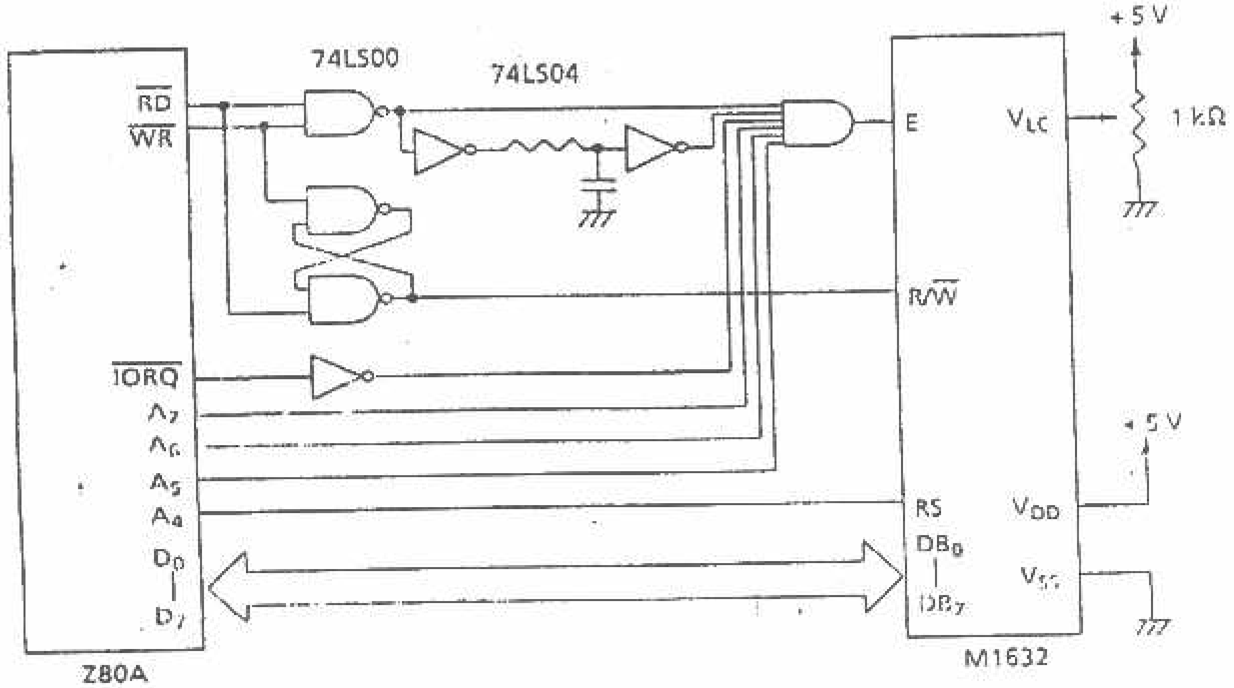
Examples of Instruction Use

Interface data length: Eight bits

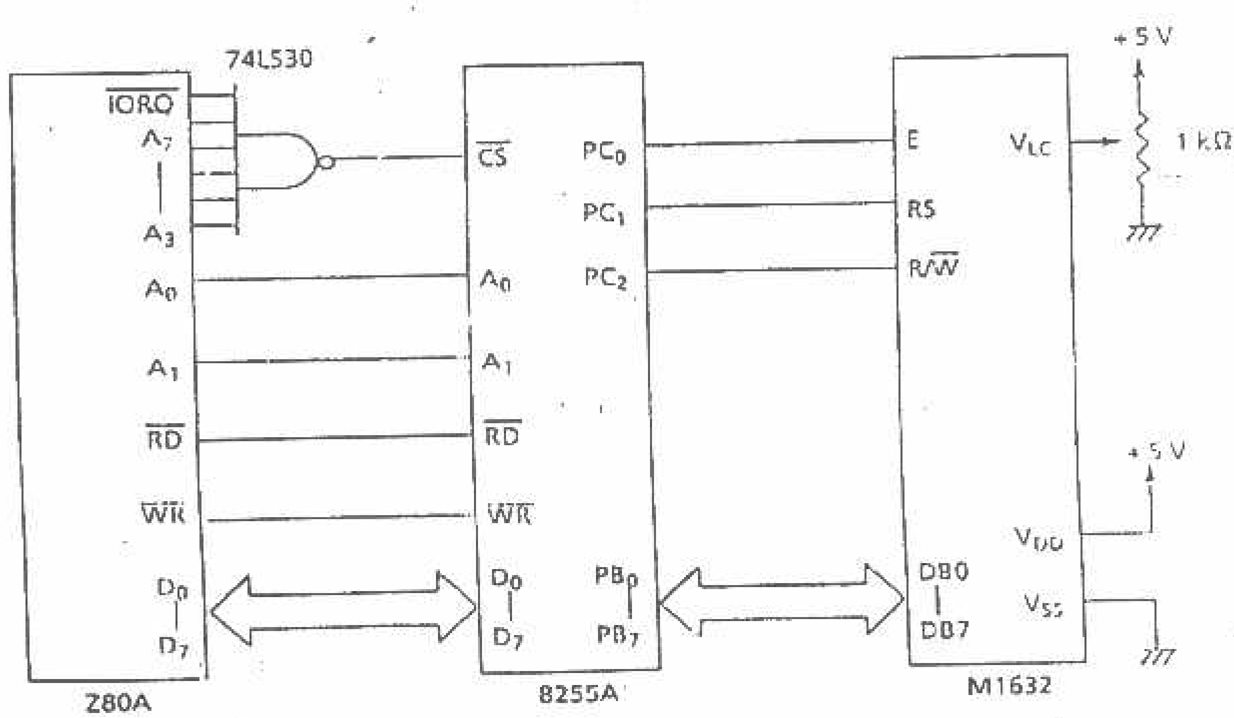
Instruction	Display	Operation
Power-on RS: / , R/W: / , DB7 — DB0: /	(blank) (blank)	The built-in reset circuit initializes the module.
Function Set ✓ RS: 0, R/W: 0, DB7 — DB0: 0 0 1 1 1 * * *	(blank) (blank)	The interface data length is set to 8 bits. The character format becomes 5 x 7 dot-matrix at 1/16 duty cycle.
Display ON/OFF Control RS: 0, R/W: 0, DB7 — DB0: 0 0 0 0 1 1 1 0	_ (blank)	The display and cursor are turned ON, but nothing is displayed.
Entry Mode Set RS: 0, R/W: 0, DB7 — DB0: 0 0 0 0 0 1 1 0	_ (blank)	The address is incremented by one and the cursor shifts to the right in a write operation to internal RAM. The display is not shifted.
Write to CG RAM or DD RAM RS: 1, R/W: 0, DB7 — DB0: 0 1 0 0 1 1 0 0	L_ (blank)	L is written. The AC is incremented by one and the cursor shifts to the right.
Write to CG RAM or DD RAM RS: 1, R/W: 0, DB7 — DB0: 0 1 0 0 0 0 1 1	LC_ (blank)	C is written.
⋮	⋮	
Write to CG RAM or DD RAM RS: 1, R/W: 0, DB7 — DB0: 0 0 1 1 0 0 1 0	LCD MODULE M1632 (blank)	2 is written in digit 16. Cursor disappears.

MPU Connection Diagrams

.1 Z80A



7.2 Z80A and 8255A

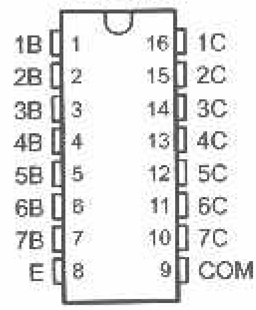


The ULN2001A is obsolete and is no longer supplied.

SLRS027F – DECEMBER 1976 – REVISED FEBRUARY 2003

- **500-mA-Rated Collector Current (Single Output)**
- **High-Voltage Outputs . . . 50 V**
- **Output Clamp Diodes**
- **Inputs Compatible With Various Types of Logic**
- **Relay-Driver Applications**
- **Designed to Be Interchangeable With Sprague ULN2001A Series**

ULN2001A . . . D OR N PACKAGE
ULN2002A . . . N PACKAGE
ULN2003A, ULN2004A . . . D, N, OR NS PACKAGE
ULQ2003A, ULQ2004A . . . D OR N PACKAGE
(TOP VIEW)



›scription/ordering information

The ULN2001A, ULN2002A, ULN2003A, ULN2004A, ULQ2003A, and ULQ2004A are high-voltage, high-current Darlington transistor arrays. Each consists of seven npn Darlington pairs that feature high-voltage outputs with common-cathode clamp diodes for switching inductive loads. The collector-current rating of a single Darlington pair is 500 mA. The Darlington pairs can be paralleled for higher current capability. Applications include relay drivers, hammer drivers, lamp drivers, display drivers (LED and gas discharge), line drivers, and logic buffers. For 100-V (otherwise interchangeable) versions of the ULN2003A and ULN2004A, see the SN75468 and SN75469, respectively.

ORDERING INFORMATION

T_A	PACKAGE†		ORDERABLE PART NUMBER	TOP-SIDE MARKING
–20°C to 70°C	PDIP (N)	Tube of 25	ULN2002AN	ULN2002AN
			ULN2003AN	ULN2003AN
			ULN2004AN	ULN2004AN
	SOIC (D)	Tube of 40	ULN2003AD	ULN2003A
		Reel of 2500	ULN2003ADR	
		Tube of 40	ULN2004AD	ULN2004A
		Reel of 2500	ULN2004ADR	
	SOP (NS)	Reel of 2000	ULN2003ANSR	ULN2003A
			ULN2004ANSR	ULN2004A
–40°C to 85°C	PDIP (N)	Tube of 25	ULQ2003AN	ULQ2003A
			ULQ2004AN	ULQ2004AN
	SOIC (D)	Tube of 40	ULQ2003AD	ULQ2003A
		Reel of 2500	ULQ2003ADR	ULQ2003A
		Tube of 40	ULQ2004AD	ULQ2004A
		Reel of 2500	ULQ2004ADR	ULQ2004A

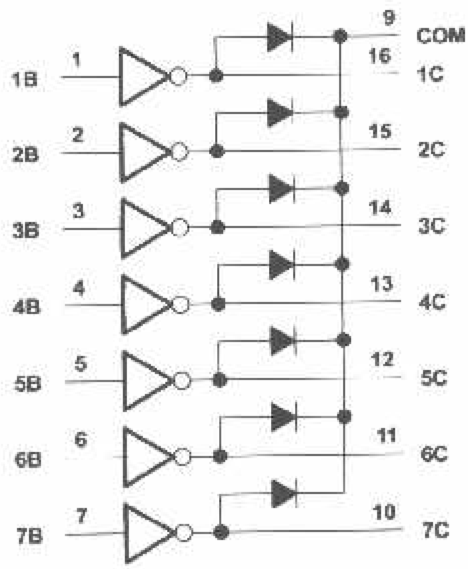
† Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.

The ULN2001A is obsolete and is no longer supplied.

iption/ordering information (continued)

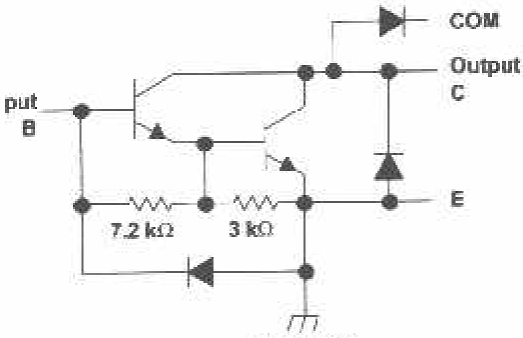
he ULN2001A is a general-purpose array and can be used with TTL and CMOS technologies. The ULN2002A designed specifically for use with 14-V to 25-V PMOS devices. Each input of this device has a Zener diode nd resistor in series to control the input current to a safe limit. The ULN2003A and ULQ2003A have a 2.7-kΩ eries base resistor for each Darlington pair for operation directly with TTL or 5-V CMOS devices. The LN2004A and ULQ2004A have a 10.5-kΩ series base resistor to allow operation directly from CMOS devices iat use supply voltages of 6 V to 15 V. The required input current of the ULN/ULQ2004A is below that of the LN/ULQ2003A, and the required voltage is less than that required by the ULN2002A.

diagram

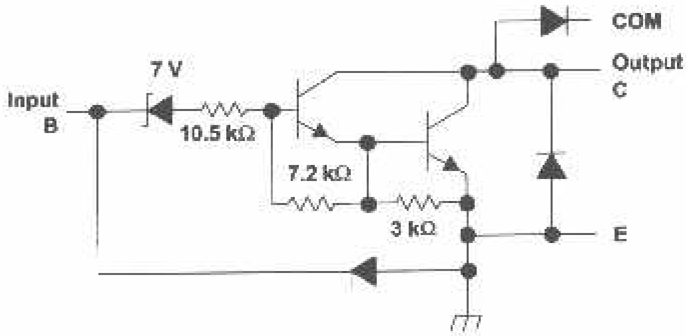


The ULN2001A is obsolete
and is no longer supplied.

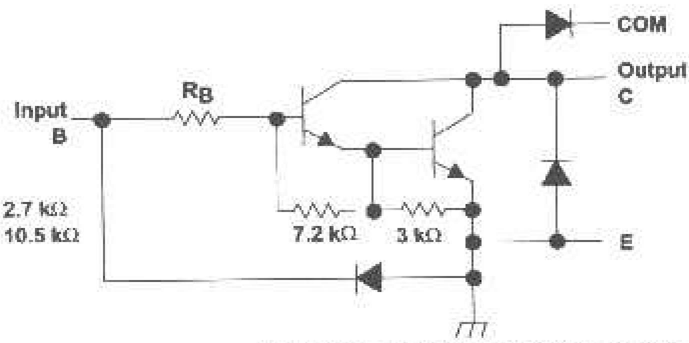
:hematics (each Darlington pair)



ULN2001A



ULN2002A



ULN/ULQ2003A: R_B = 2.7 kΩ
ULN/ULQ2004A: R_B = 10.5 kΩ

ULN2003A, ULN2004A, ULQ2003A, ULQ2004A

Jl resistor values shown are nominal.

The ULN2001A is obsolete and is no longer supplied.

ute maximum ratings at 25°C free-air temperature (unless otherwise noted)†

ollector-emitter voltage .... 50 V
lamp diode reverse voltage (see Note 1) .... 50 V
iput voltage, V_I (see Note 1) .... 30 V
eak collector current (see Figures 14 and 15) .... 500 mA
utput clamp current, I_{OK} .... 500 mA
otal emitter-terminal current .... –2.5 A
perating free-air temperature range, T_A: ULN200xA .... –20°C to 70°C
ULQ200xA .... –40°C to 85°C
ULQ200xAT .... –40°C to 105°C
ackage thermal impedance, θ_{JA} (see Notes 2 and 3): D package .... 73°C/W
N package .... 67°C/W
NS package .... 64°C/W
ackage thermal impedance, θ_{JC} (see Notes 4 and 5): D package .... 36°C/W
N package .... 54°C/W
perating virtual junction temperature, T_J .... 150°C
ead temperature 1,6 mm (1/16 inch) from case for 10 seconds .... 260°C
torage temperature range, T_{stg} .... –65°C to 150°C

s beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and ial operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not . Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

1. All voltage values are with respect to the emitter/substrate terminal E, unless otherwise noted.
2. Maximum power dissipation is a function of T_J(max), θ_{JA}, and T_A. The maximum allowable power dissipation at any allowable ambient temperature is $P_D = (T_J(max) - T_A)/\theta_{JA}$. Operating at the absolute maximum T_J of 150°C can affect reliability.
3. The package thermal impedance is calculated in accordance with JESD 51-7.
4. Maximum power dissipation is a function of T_J(max), θ_{JC}, and T_C. The maximum allowable power dissipation at any allowable case temperature is $P_D = (T_J(max) - T_C)/\theta_{JC}$. Operating at the absolute maximum T_J of 150°C can affect reliability.
5. The package thermal impedance is calculated in accordance with MIL-STD-883.

cal characteristics, T_A = 25°C (unless otherwise noted)

PARAMETER	TEST FIGURE	TEST CONDITIONS		ULN2001A			ULN2002A			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	
On-state input voltage	6	V_{CE} = 2 V,	I_C = 300 mA						13	V
Collector-emitter saturation voltage	5	I_I = 250 μA,	I_C = 100 mA		0.9	1.1		0.9	1.1	V
		I_I = 350 μA,	I_C = 200 mA		1	1.3		1	1.3	
		I_I = 500 μA,	I_C = 350 mA		1.2	1.6		1.2	1.6	
Clamp forward voltage	8	I_F = 350 mA			1.7	2		1.7	2	V
Collector cutoff current	1	V_{CE} = 50 V,	I_I = 0			50			50	μA
	2	V_{CE} = 50 V, T_A = 70°C	I_I = 0			100			100	
			V_I = 6 V						500	
Off-state input current	3	V_{CE} = 50 V, T_A = 70°C	I_C = 500 μA,	50	65		50	65		μA
Input current	4	V_I = 17 V						0.82	1.25	mA
Clamp reverse current	7	V_R = 50 V,	T_A = 70°C			100			100	μA
		V_R = 50 V				50			50	
Static forward-current transfer ratio	5	V_{CE} = 2 V,	I_C = 350 mA	1000						
Input capacitance		V_I = 0,	f = 1 MHz		15	25		15	25	pF

The ULN2001A is obsolete and is no longer supplied.

ectrical characteristics, T_A = 25°C (unless otherwise noted) (continued)

	PARAMETER	TEST FIGURE	TEST CONDITIONS		ULN2003A			ULN2004A			UNIT
					MIN	TYP	MAX	MIN	TYP	MAX	
(on)	On-state input voltage	6	V_{CE} = 2 V	I_C = 125 mA						5	V
				I_C = 200 mA			2.4			6	
				I_C = 250 mA			2.7				
				I_C = 275 mA						7	
				I_C = 300 mA			3				
				I_C = 350 mA						8	
CE(sat)	Collector-emitter saturation voltage	5	I_I = 250 µA,	I_C = 100 mA		0.9	1.1		0.9	1.1	V
			I_I = 350 µA,	I_C = 200 mA		1	1.3		1	1.3	
			I_I = 500 µA,	I_C = 350 mA		1.2	1.6		1.2	1.6	
EX	Collector cutoff current	1	V_{CE} = 50 V,	I_I = 0			50			50	µA
		2	V_{CE} = 50 V, T_A = 70°C	I_I = 0			100			100	
				V_I = 1 V						500	
F	Clamp forward voltage	8	I_F = 350 mA			1.7	2		1.7	2	V
off)	Off-state input current	3	V_{CE} = 50 V, T_A = 70°C	I_C = 500 µA,	50	65		50	65		µA
	Input current	4	V_I = 3.85 V			0.93	1.35				mA
			V_I = 5 V						0.35	0.5	
			V_I = 12 V						1	1.45	
	Clamp reverse current	7	V_R = 50 V				50			50	µA
			V_R = 50 V,	T_A = 70°C			100			100	
	Input capacitance		V_I = 0,	f = 1 MHz		15	25		15	25	pF

The ULN2001A is obsolete and is no longer supplied.

cal characteristics over recommended operating conditions (unless otherwise noted)

PARAMETER	TEST FIGURE	TEST CONDITIONS		ULQ2003A MIN	ULQ2003A TYP	ULQ2003A MAX	ULQ2004A MIN	ULQ2004A TYP	ULQ2004A MAX	UNIT
On-state input voltage	6	V_{CE} = 2 V	I_C = 125 mA						5	V
			I_C = 200 mA			2.7			6	
			I_C = 250 mA			2.9				
			I_C = 275 mA						7	
			I_C = 300 mA			3				
			I_C = 350 mA						8	
Collector-emitter saturation voltage	5	I_I = 250 μA,	I_C = 100 mA		0.9	1.2		0.9	1.1	V
		I_I = 350 μA,	I_C = 200 mA		1	1.4		1	1.3	
		I_I = 500 μA,	I_C = 350 mA		1.2	1.7		1.2	1.6	
Collector cutoff current	1	V_{CE} = 50 V,	I_I = 0			100			50	μA
	2	V_{CE} = 50 V	I_I = 0						100	
			V_I = 1 V						500	
Clamp forward voltage	8	I_F = 350 mA			1.7	2.3		1.7	2	V
Off-state input current	3	V_{CE} = 50 V,	I_C = 500 μA		65		50	65		μA
Input current	4	V_I = 3.85 V			0.93	1.35				mA
		V_I = 5 V						0.35	0.5	
		V_I = 12 V						1	1.45	
Clamp reverse current	7	V_R = 50 V,	T_A = 25°C			100			50	μA
		V_R = 50 V				100			100	
Input capacitance		V_I = 0,	f = 1 MHz		15	25		15	25	pF

ing characteristics, T_A = 25°C

PARAMETER	TEST CONDITIONS	ULN2001A, ULN2002A, ULN2003A, ULN2004A MIN	TYP	MAX	UNIT
Propagation delay time, low- to high-level output	See Figure 9		0.25	1	μs
Propagation delay time, high- to low-level output	See Figure 9		0.25	1	μs
High-level output voltage after switching	V_S = 50 V, I_O ≈ 300 mA, See Figure 10	V_S–20			mV

ing characteristics over recommended operating conditions (unless otherwise noted)

PARAMETER	TEST CONDITIONS	ULQ2003A, ULQ2004A MIN	TYP	MAX	UNIT
Propagation delay time, low- to high-level output	See Figure 9		1	10	μs
Propagation delay time, high- to low-level output	See Figure 9		1	10	μs
High-level output voltage after switching	V_S = 50 V, I_O ≈ 300 mA, See Figure 10	V_S–500			mV

The ULN2001A is obsolete and is no longer supplied.

PARAMETER MEASUREMENT INFORMATION

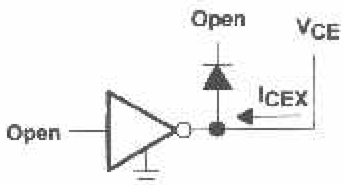


Figure 1. I_{CEX} Test Circuit

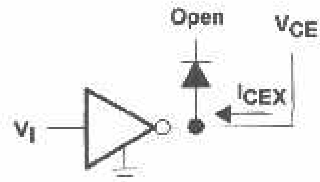


Figure 2. I_{CEX} Test Circuit

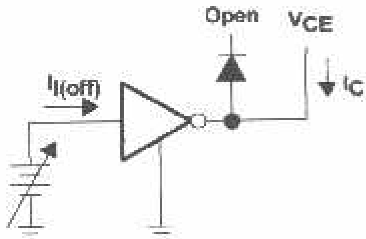


Figure 3. $I_{I(off)}$ Test Circuit

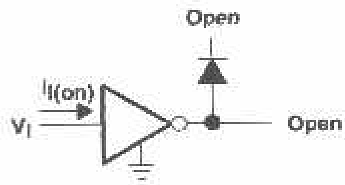
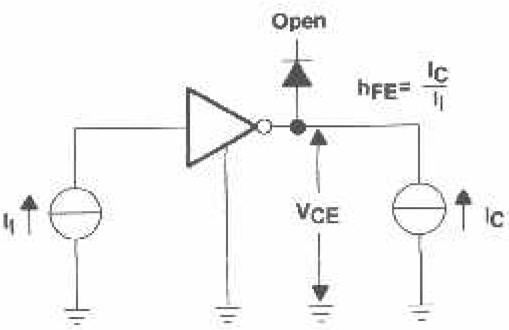


Figure 4. I_I Test Circuit



NOTE: I_I is fixed for measuring $V_{CE(sat)}$, variable for measuring h_{FE}.

Figure 5. h_{FE}, $V_{CE(sat)}$ Test Circuit

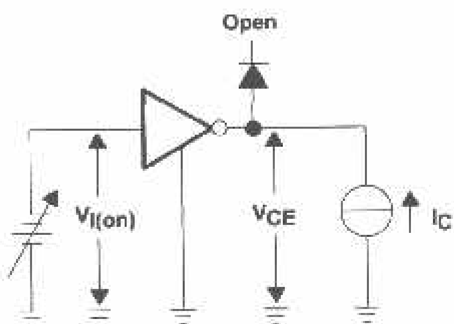


Figure 6. $V_{I(on)}$ Test Circuit

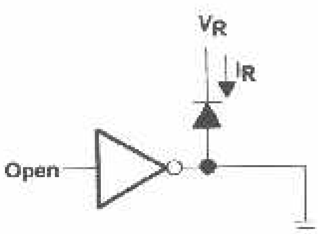


Figure 7. I_R Test Circuit

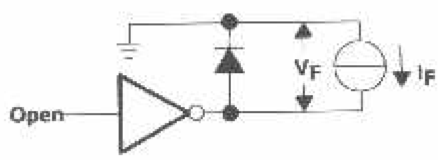


Figure 8. V_F Test Circuit

The ULN2001A is obsolete and is no longer supplied.

PARAMETER MEASUREMENT INFORMATION

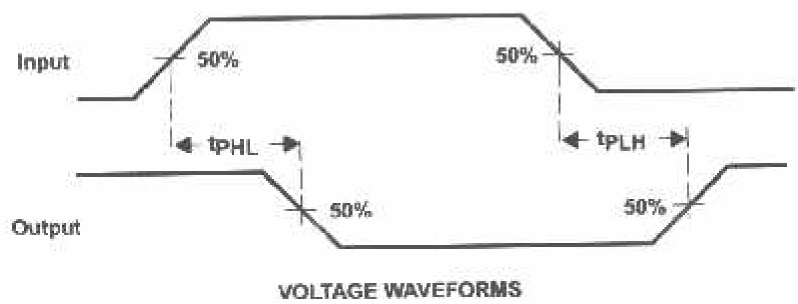
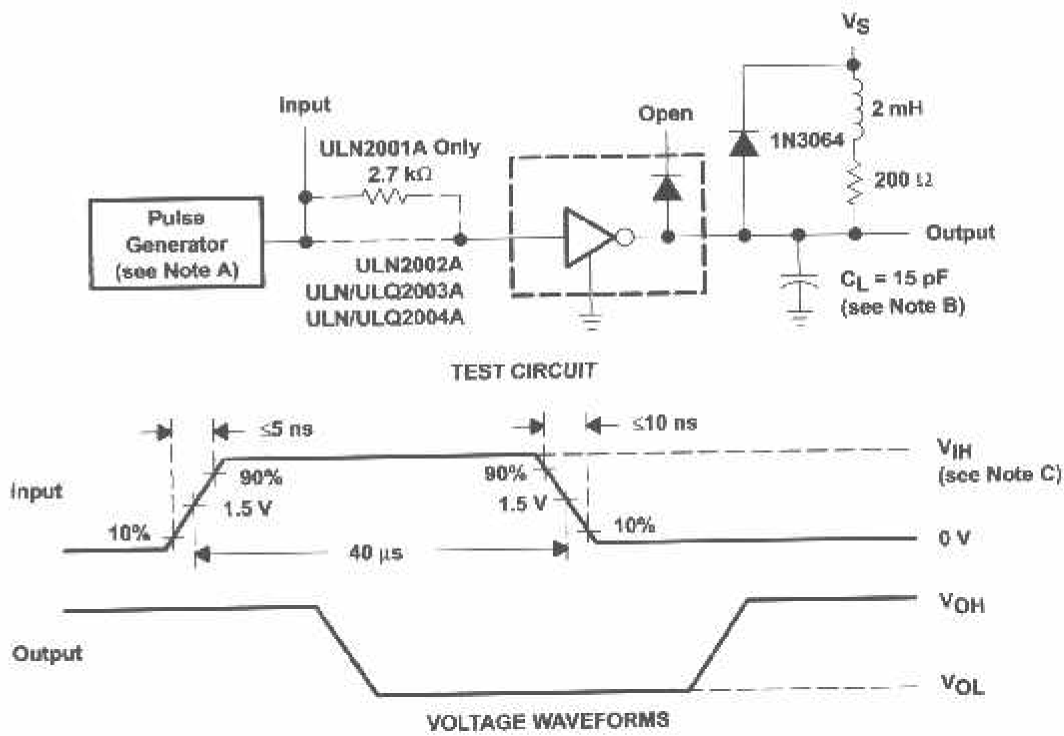


Figure 9. Propagation Delay-Time Waveforms



A. The pulse generator has the following characteristics: PRR = 12.5 kHz, Z_O = 50 Ω.
B. C_L includes probe and jig capacitance.
C. For testing the ULN2001A, the ULN2003A, and the ULQ2003A, V_{IH} = 3 V; for the ULN2002A, V_{IH} = 13 V; for the ULN2004A and the ULQ2004A, V_{IH} = 8 V.

Figure 10. Latch-Up Test Circuit and Voltage Waveforms

The ULN2001A is obsolete and is no longer supplied.

TYPICAL CHARACTERISTICS

COLLECTOR-EMITTER SATURATION VOLTAGE vs COLLECTOR CURRENT (ONE DARLINGTON)

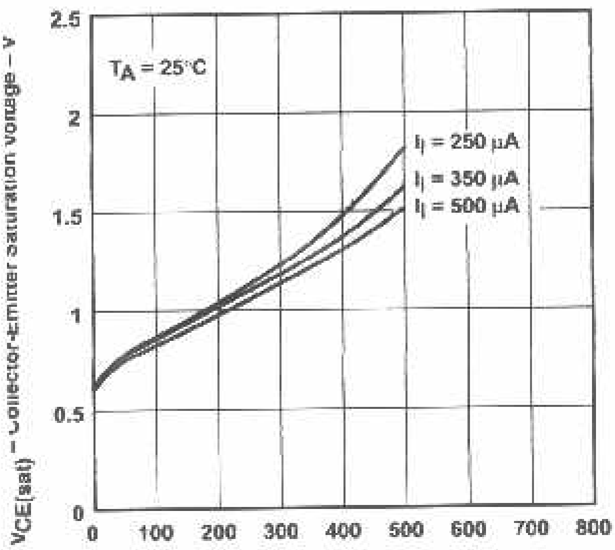


Figure 11

COLLECTOR-EMITTER SATURATION VOLTAGE vs TOTAL COLLECTOR CURRENT (TWO DARLINGTONS IN PARALLEL)

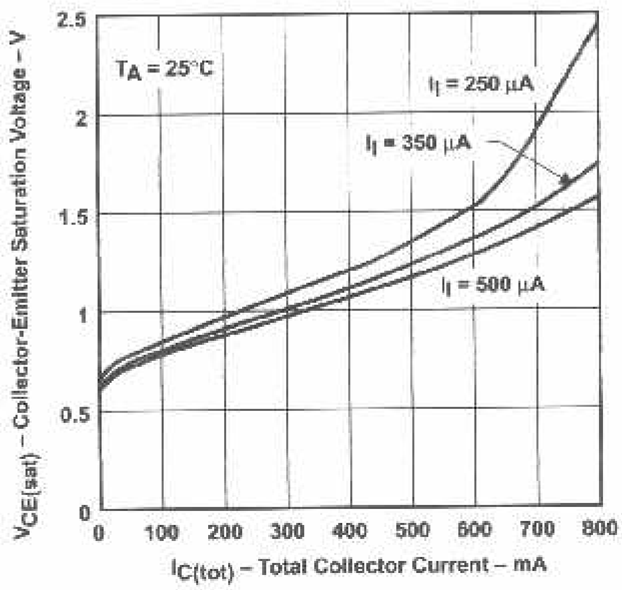


Figure 12

COLLECTOR CURRENT vs INPUT CURRENT

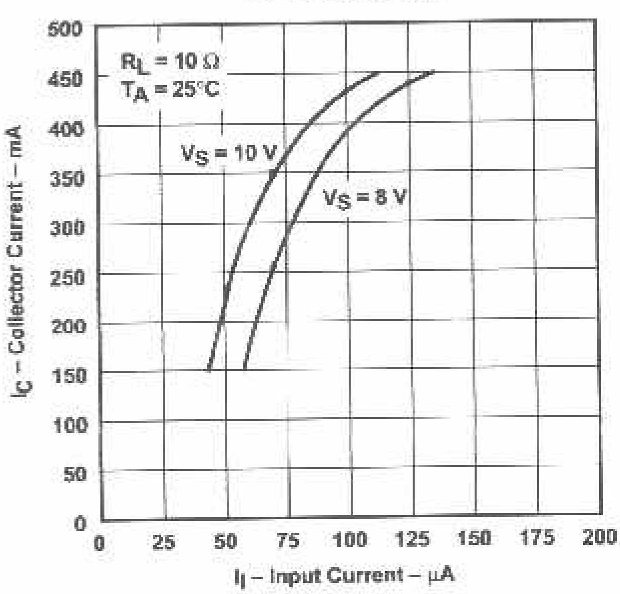


Figure 13

The ULN2001A is obsolete and is no longer supplied.

THERMAL INFORMATION

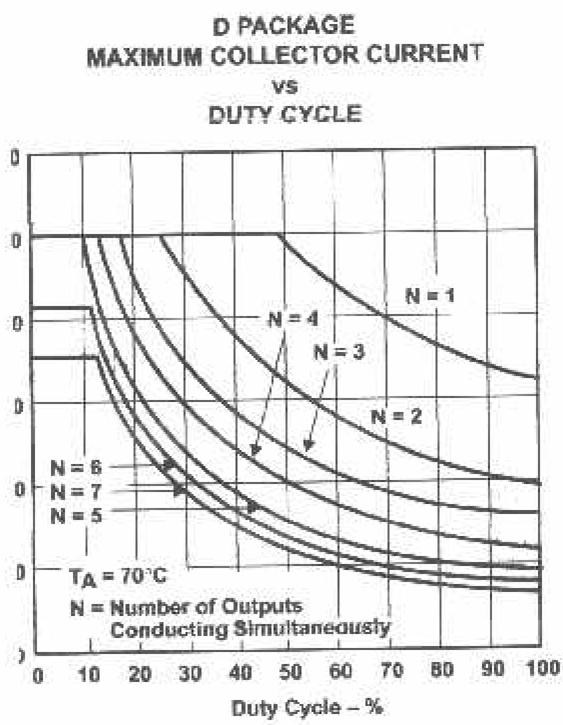


Figure 14

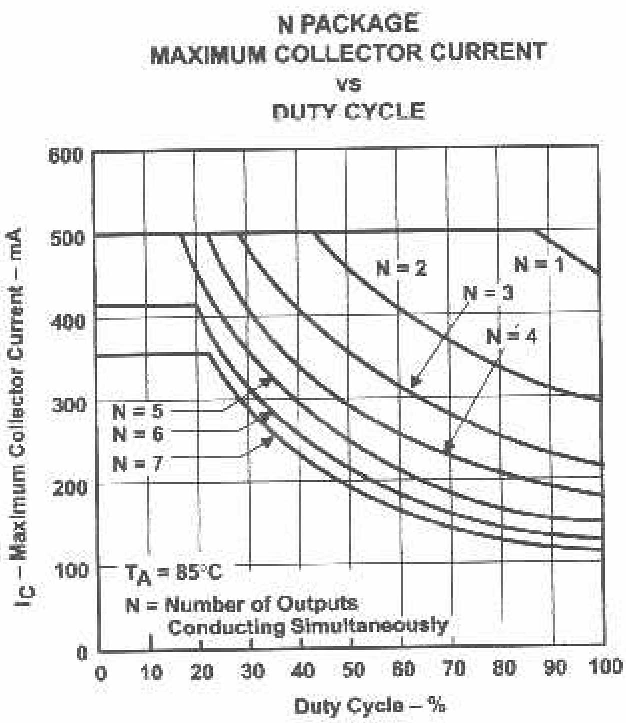


Figure 15

The ULN2001A is obsolete
and is no longer supplied.

APPLICATION INFORMATION

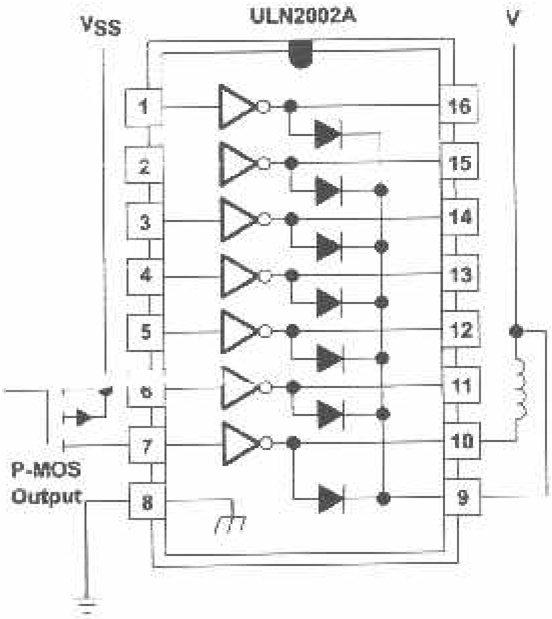


Figure 16. P-MOS to Load

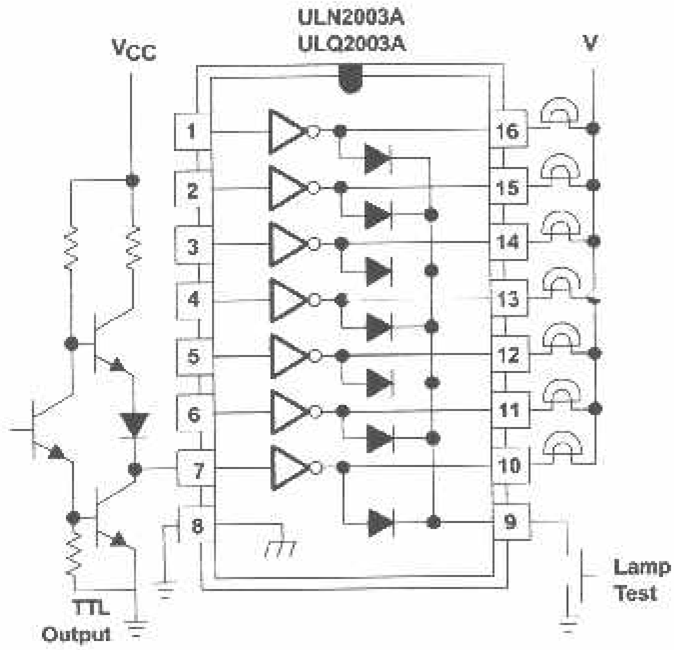


Figure 17. TTL to Load

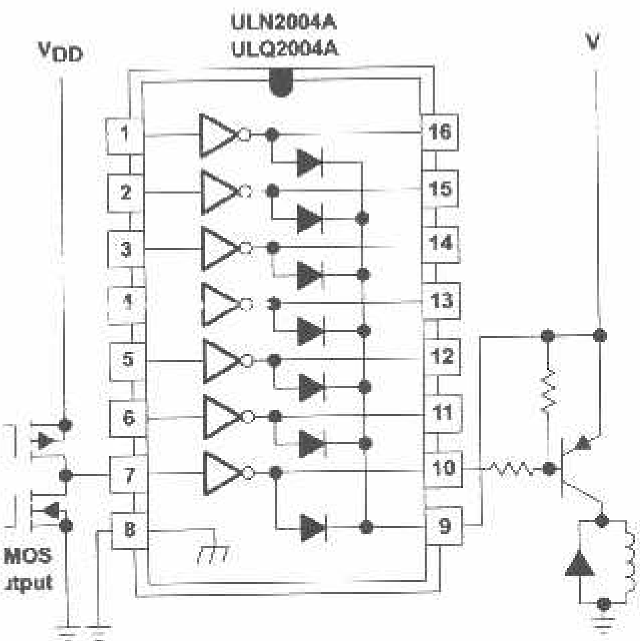


Figure 18. Buffer for Higher Current Loads

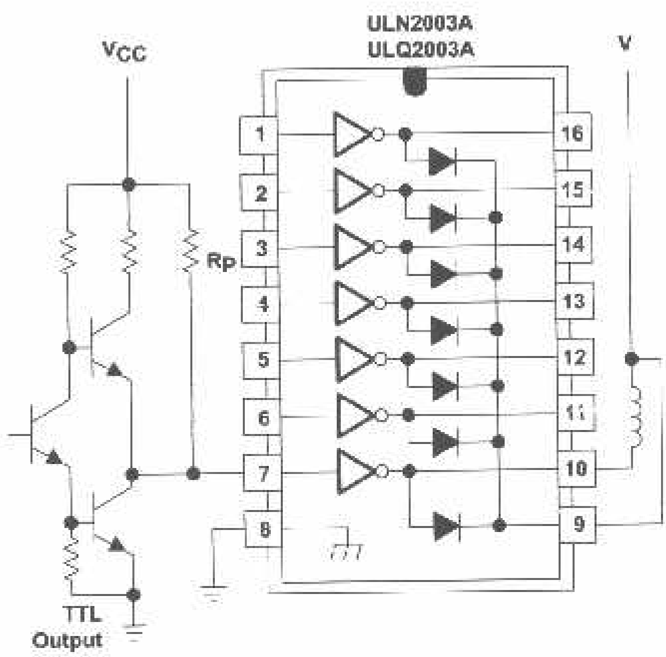
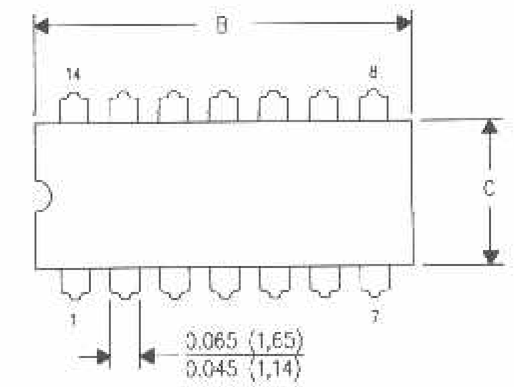
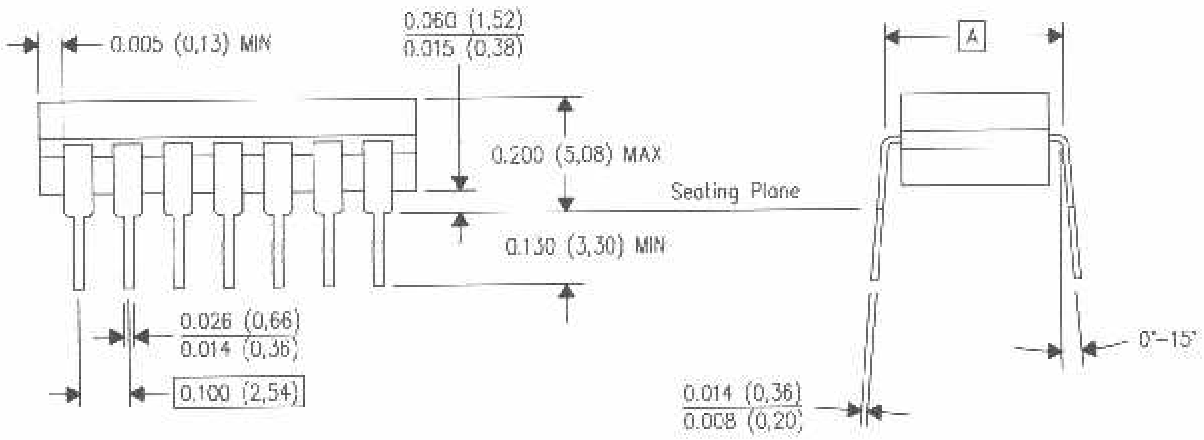


Figure 19. Use of Pullup Resistors to Increase Drive Current

CERAMIC DUAL IN–LINE PACKAGE



PINS ** / DIM	14	16	18	20
A	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC
B MAX	0.785 (19,94)	.840 (21,34)	0.960 (24,38)	1.060 (26,92)
B MIN	—	—	—	—
C MAX	0.300 (7,62)	0.300 (7,62)	0.310 (7,87)	0.300 (7,62)
C MIN	0.245 (6,22)	0.245 (6,22)	0.220 (5,59)	0.245 (6,22)

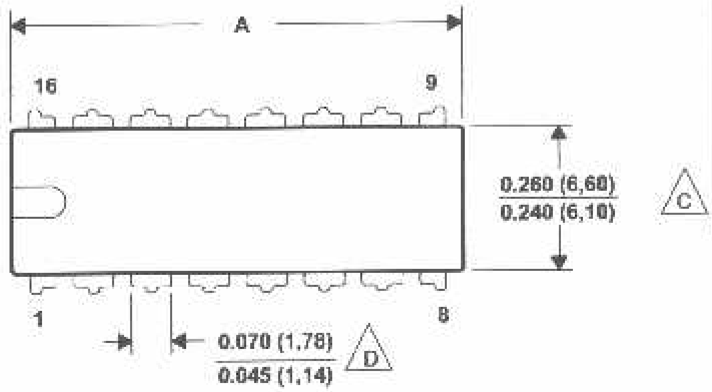


4040083/F 03/03

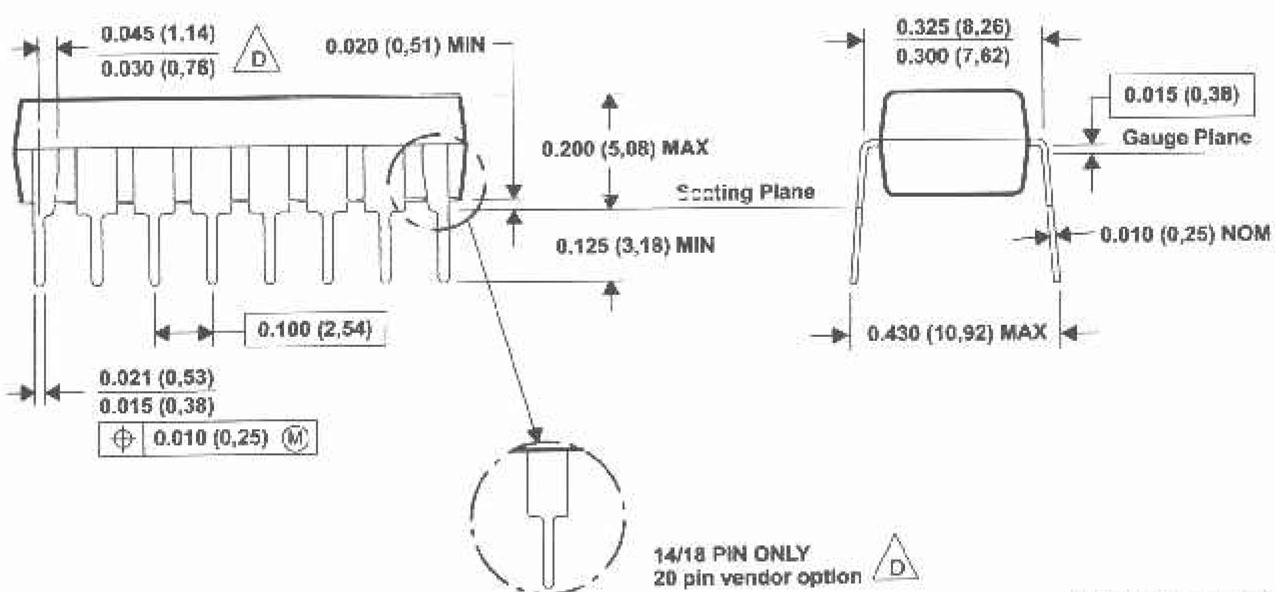
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. This package is hermetically sealed with a ceramic lid using glass frit.
D. Index point is provided on cap for terminal identification only on press ceramic glass frit seal only.
E. Falls within MIL STD 1835 GDIP1-T14, GDIP1-T16, GDIP1-T18 and GDIP1-T20.

(R-PDIP-T)** **PLASTIC DUAL IN-LINE PACKAGE**

PINS SHOWN



DIM \ PINS **	14	16	18	20
A MAX	0.775 (19,69)	0.775 (19,69)	0.920 (23,37)	1.060 (26,92)
A MIN	0.745 (18,92)	0.745 (18,92)	0.850 (21,59)	0.940 (23,88)
MS-100 VARIATION	AA	BB	AC	AD

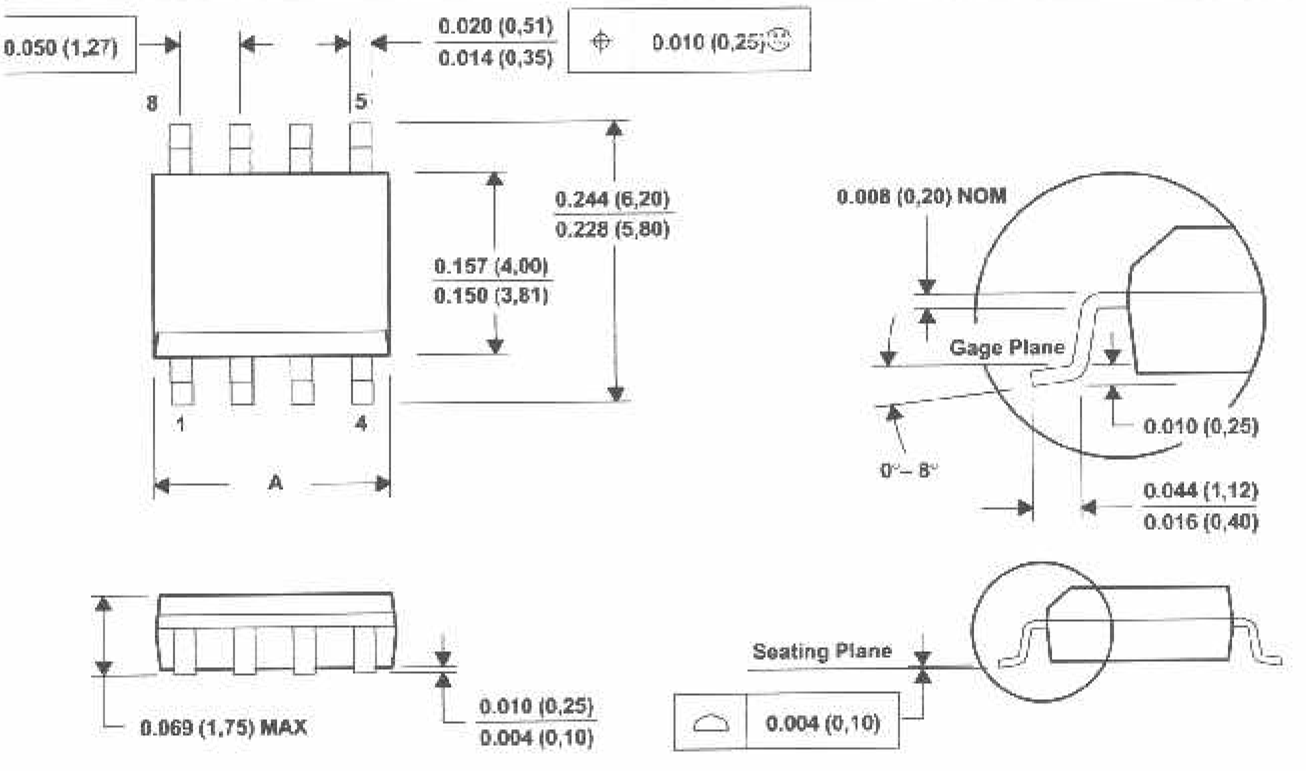


4040049/E 12/2002

TES: A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS-001, except 18 and 20 pin minimum body length (Dim A).
D. The 20 pin end lead shoulder width is a vendor option, either half or full width.

(R-PDSO-G)** **PLASTIC SMALL-OUTLINE PACKAGE**

PINS SHOWN



PINS ** / DIM	8	14	16
A MAX	0.197 (5,00)	0.344 (8,75)	0.394 (10,00)
A MIN	0.189 (4,80)	0.337 (8,55)	0.386 (9,80)

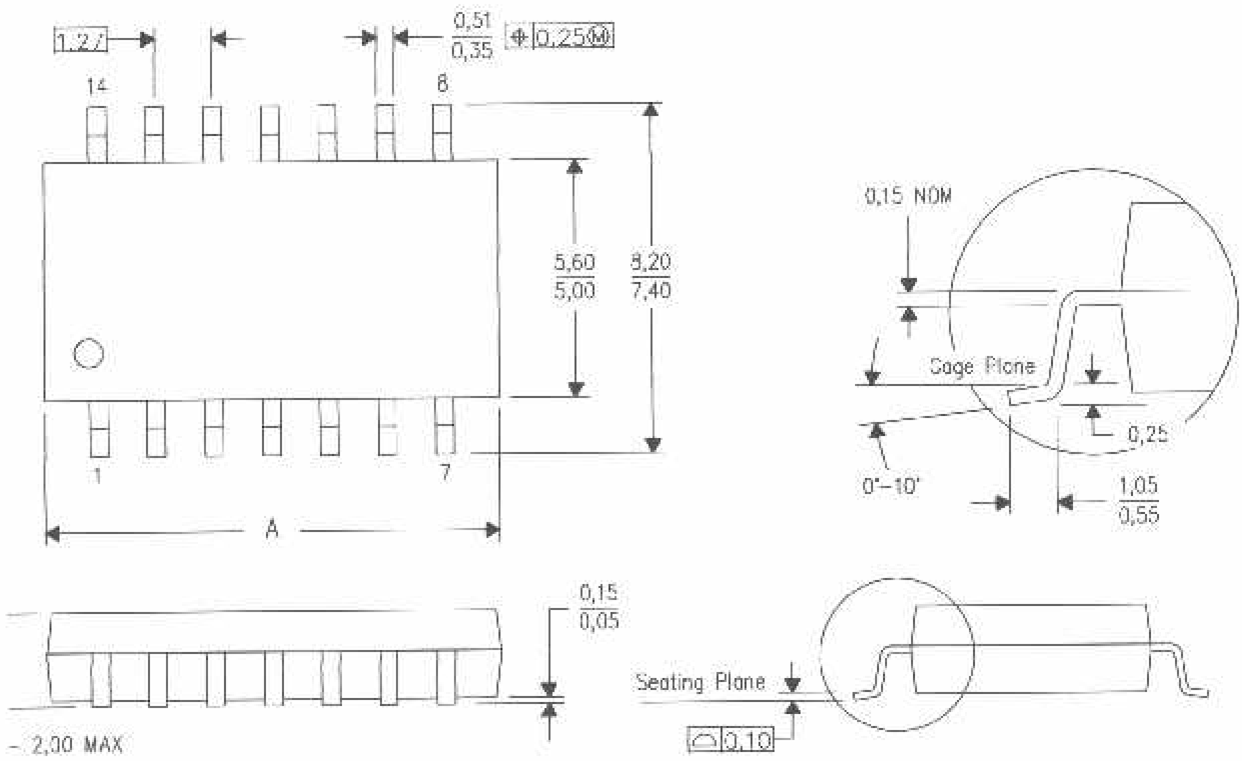
4040047/E 09/01

NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion, not to exceed 0.006 (0,15).
D. Falls within JEDEC MS-012

ꓤ-PDSO-G**)

PLASTIC SMALL-OUTLINE PACKAGE

ꓤS SHOWN



PINS ** / DIM	14	16	20	24
A MAX	10,50	10,50	12,90	15,30
A MIN	9,90	9,90	12,30	14,70

4040062/C 03/03

A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

```
yboard via a special "Y-splitter" cable adapter.

e "Y-splitter" cable adapter is connected as follows:

yboard (F)        Computer (M)        Mouse (F)
----------        ------------        ------------
n function        pin function        pin function

1=data ---------- 1=data        +--- 1=data
2 n.c.            2 -----------+     2 n.c.
3=gnd ----------- 3=gnd ----------- 3=gnd
4=+5v ----------- 4=+5v ----------- 4=+5v
5=clock --------- 5 clock   +------ 5=clock
6 n.c.            6 --------+       6 n.c.

is is the "4068"/"AK6K" ("stubby") "PS/2 Keyboard & Mouse Splitor
ni Din Din6M/F/F" from Blue Diamond.

u can also connect the keyboard or mouse alone to that connector,
thout the Y-splitter.  I don't know how the computer can tell which
vice is plugged into it, though.


ere is also another common Y-splitter available, which is connected
 follows:

yboard (F)        Computer (M)        Keyboard #2 (F)
----------        ------------        ---------------
n function        pin function        pin function

1=data ---------- 1=data ---------- 1=data
2 n.c. ---------- 2 --------------- 2 n.c.
3=gnd ----------- 3=gnd ----------- 3=gnd
4=+5v ----------- 4=+5v ----------- 4=+5v
5=clock --------- 5=clock --------- 5=clock
6 n.c. ---------- 6 --------------- 6 n.c.
```

is is the "5228"/"MFF6XI" ("long") "PS/2 Port Splitter" from Blue
amond. It cannot be used as a Keyboard/Mouse splitter, because it
esn't separate the data (& clock) lines of the two devices. I didn't
w what it was good for until I got an email from Ravn Gundersen,
o wrote: *"It's used if you want two keyboards to work as one on a
mputer. Possible uses are many, one example would be if you want a
rcode scanner connected to ps/2 together with a keyboard, or a barcode
anner and a magnetic card reader, etc."* Thanks, Ravn!

te: the connector is called a 6-pin mini-DIN, and the keyboard and
use connector pinout charts above show six pins, but some mice and
yboards are made with the (male) connector having only four pins
.e., with the unconnected pin 2 and pin 6 missing).

re's a web site with a lot more detailed technical information
 the PS/2 Mouse/Keyboard interface:
tp://www.computer-engineering.org/
http://panda.cs.ndsu.nodak.edu/~achapwes/PICmicro/PS2/ps2.htm (or here)

;2 keyboard and mouse mini-DIN-6 connector pinouts

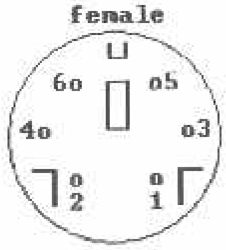
2_keyboard_and_mouse_mini-DIN-6_connector_pinouts.html

Dave Burton <mailto:dave@burtonsys.com.nospam?subject=PS2_keyboard and mouse_c
tp://www.burtonsys.com/

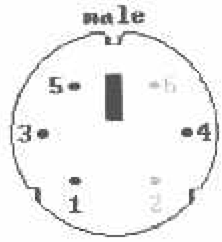
te: the original version of this document uses IBM PC Line-Drawing
aracters ("ANSI art"). You can download it from here:
2_keyboard_and_mouse_mini-DIN-6_connector_pinouts.txt
t it does not look right when viewed with a Windows character set.

M PS/2-type mouse and keyboard connectors are both "6-pin mini-DIN"
nnectors. The female connectors are on the computer, the male
nnectors are on the mouse and keyboard cables that plug into the
mputer.

ewing the female connector (on the computer), the pinout is:



ewing the male connector (on the keyboard or mouse cable), the pinout is:



both cases, the pins are normally used as follows:

```
pin  function

 1   data
 2   (reserved)
 3   gnd
 4   +5v
 5   clock
 6   (reserved)
```

wever, on the NEC Versa 24xx and Panasonic Toughbook CF-35 laptop
mputers, and some others, there is just one connector on the computer,
d it uses "reserved" pins to permit connecting both a mouse and a

ePanorama.net

The page cannot be displayed

ie page you are looking for is currently unavailable. The Web site
ight be experiencing technical difficulties, or you may need to adjust

'GA analogue display connector

arly all modern PC graphics cards use the same 15 pin conenctor that the original IBM VGA card :d. The connector is not very suitable for high resolution graphics because it does not have a well ined impedance characteristics like BNC connectors. 15 pin VGA connector is still commonly used :ause it is so popular that it is hard to sell product without it.

in numbering in female connector

VGA connector picture

inout

```
Red out *
Green out *
Blue out *
Monitor ID 2 in
Ground
Red return
Green return
Blue return
no pin
Sync return
Monitor ID 0 in
Monitor ID 1 in
Horizonal Sync out
Vertical Sync out
reserved (monitor ID 3)
```

ıals marked with * are analogue 0.7V p-p positive signals to 75 ohm load. All other signals are level signals.

e is an ASCII pinout diagram for those who prefer it:

```
                                                                    6
Red (Analog)     6 Red    Return     11 (ID0) GND (Color)      11. . . 1
Green (Analog)   7 Green Return      12 (ID1) NC (Color)          . . .
Blue (Analog)    8 Blue   Retuer     13 Horzontal Sync            . . .
Reserved         9 No Connect        14 Vertical  Sync            . . .
Ground          10 Ground            15 No Connect                . . .
                                                               15  10  5
```

onitor ID detection pin assignments

```
  11   12
! ID0  ID1

: n/c  n/c   no monitor
; n/c  GND   Mono monitor which does not support 1024x768
: GND  n/c   Color monitor which does not support 1024x768
; GND  n/c   Color monitor which supports 1024x768
```

D menas connected to ground
means that the pin has not bee connected anywhere

s monitor type detection is becoming more and more obsolete nowadays, because more and de intelligence is integrated to the monitor. New plug-and-play monitors communicate with the 1puter according to VESA DDC standard.

ESA DDC

;A Display Data Channel is a method for integrating digital interface to VGA conenctor to be able monitor and grapahics card to communicate. There are two different levels of DDC: DDC1 and C2.

)C1

C1 allows the monitor to tell it's parapeters to the computer. The following VGA card connector s had to be changed to allow DDC1 fuctions:

```
    new function
    Optional +5V output from graphics card
    Data from display
    Standard vertical sync signal which works also as data clock
    Monitor ID3
```

en grpahics card detects data on data-line it starts to read the data coming from the monitor cronous to vertical sync pulse. Vertical sync pulse frequency can be increased up to 25 KHz for time of the data transfer if a DDC1 compliant monitor is found (be sure not to send those high juencies to non DDC1 monitors!).

)C2

C2 allows bidirectional communication: monitor can tell it's parameters and computer can adjust itor settings. The bidirectional data bus is a syncronous data bus similar to Access Bus and is ed on I2C technology. Tho following pins had to be changed to to enable DDC2 to work:

```
    new function
    Optional +5V output from graphics card
    Bidirectional data line (SDA)
    Data clock (SLC)
```

signals in the data bus are standard I2C signals. The computer provides 15 kohm pullup for the \ and SLC lines. Monitor must provide 47 kohm pull-up on SCLK line.

TE: If the optional +5V power output pin is used, a special DDC/VGA connector must be used to rovide proper sequencing. The +5V output voltage must be withing +/-5% range and tha card st be able to supply at least 300 mA current (maximum 1A).

ESA DPMS power saving

;A has defined a standard method for computer to tell monitor when to go to power saving de. This power saving mode is controlled by changing the sync signals according the table ow:

	NORMAL	STANDBY	Suspended
ync	On	Off	On
ync	On	On	Off
er level	100%	0	0

i Engdahl
mi.Engdahl@iki.fi>

t modified: May 28, 2002
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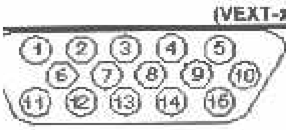
Keyboard, Monitor & Mouse Pinouts

for PC, SUN, MAC, USB, FireWire®, RS232, Digital Flat Panel and EVC configurations

VGA VIDEO with DDC (VEXT-xx, VEXT-xx-MM)



Mating face of 15-pin HD male

PIN#	SIGNAL	PIN#	SIGNAL
	RED	9	NC
	GREEN	10	SYNC RTN
	BLUE	11	ID0
	ID2	12	ID1 or DDC DATA
	GND	13	HSYNC
	RED SHIELD	14	VSYNC
	GREEN SHIELD	15	ID3 or DDC CLOCK
	BLUE SHIELD		

NTI's VGA cables extend a VGA monitor up to 100 feet at high resolutions up to 1920x1200.

See PS/2 CABLES for more details.

SUN AND SGI VIDEO

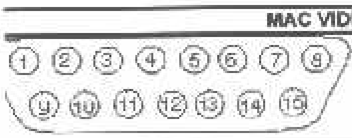
Mating face of 13W3 female

PIN#	SIGNAL	PIN#	SIGNAL
	GND	8	ID1
	VSYNC	9	ID0
	ID2	10	GND
	GND	A1	RED
	CSYNC	A2	GREEN
	HSYNC	A3	BLUE
	GND		

Sun computer cables and adapters include Sun to VGA adapters, Sun to BNC video adapters and SUN gender changers.

See SUN CABLES for more details.

MAC VIDEO

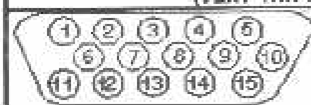


Mating face of 15D male

PIN#	SIGNAL	PIN#	SIGNAL
	GND	9	BLUE
	RED	10	ID3
	CSYNC	11	GND
	ID1	12	VS
	GREEN	13	GND
	GND	14	GND
	ID2	15	HS
	NC		

SGI Open LDI

VGA VIDEO with DDC (VEXT-FLT-xx, VEXT-FLT-xx-MM) (VEXT-THN-xx, VEXT-THN-xx-MM)



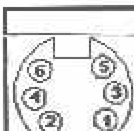
Mating face of 15-pin HD

PIN#	SIGNAL	PIN#	SIGNAL
1	RED	9	DDC+5
2	GREEN	10	SYNC RTN
3	BLUE	11	ID0
4	ID2	12	ID1 or DDC
5	GND	13	HSYNC
6	RED SHIELD	14	VSYNC
7	GREEN SHIELD	15	ID3 or DDC
8	BLUE SHIELD		

NTI's Flat and Super Thin VGA cables extend a VGA monito
These cables are ideal for applications where space is tight.

See PS/2 CABLES for more details.

PS/2 KEYBOARD OR MOUSE



Mating face of 6 pin miniDIN female

PIN#	SIGNAL	PIN#	SIGN.
1	DATA	4	+5
2	NC	5	CLOC
3	GND	6	NC

NTI's keyboard and mouse cables extend PC keyboards anc with no loss of signal.

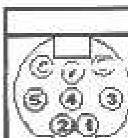
See PS/2 CABLES for more details.

PC/AT KEYBOARD

Mating face of 5 pin DIN female

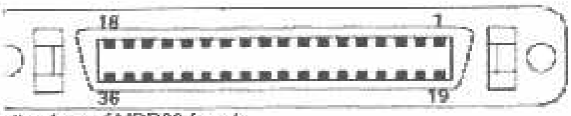
PIN#	SIGNAL	PIN#	SIGN.
1	CLOCK	4	GND
2	DATA	5	+5
3	NC		

SUN KEYBOARD AND MOUSE



Mating face of 8 pin miniDIN female

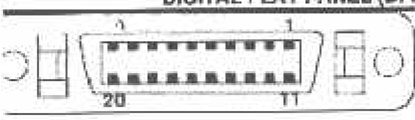
PIN#	SIGNAL	PIN#	SIGNAL
1	GND	5	KYBD RCV
2	GND	6	KYBD XMT
3	+5	7	PWRN
4	MOUSE	8	+5



ating face of MDR36 female

N#	SIGNAL	PIN#	SIGNAL
	Link2 **D0-**	19	Link2 **D3-**
	Link2 **DO+**	20	Link2 **D3+**
	Link2 **D1-**	21	Link2 **CLK-**
	Link2 **D1+**	22	Link2 **CLK+**
	Link2 **D2-**	23	DDD CLK SCL
	Link2 **D2+**	24	VCC
	NC	25	DDC DATA SDA
	NC	26	GND
	GND	27	NC
	GND	28	GND
	NC	29	NC
	NC	30	NC
	Link1 **D0-**	31	NC
	Link1 **D0+**	32	GND
	Link1 **D1-**	33	Link1 **CLK-**
	Link1 **D1+**	34	Link1 **CLK+**
	Link1 **D2-**	35	Link1 **D3-**
	Link1 **D2+**	36	Link1 **D3+**

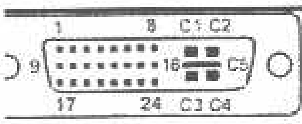
DIGITAL FLAT PANEL (DFP) PORT



Mating face of MDR20 female

N#	SIGNAL	PIN#	SIGNAL
	TX1+	11	TX2+
	TX1-	12	TX2-
	SHLD1	13	SHLD2
	SHLDC	14	SHLD0
	TXC+	15	TX0+
	TXC-	16	TX0-
	GND	17	NC
	+5V	18	HPD
	NC	19	DDC_DAT
	NC	20	DDC_CLK

DVI



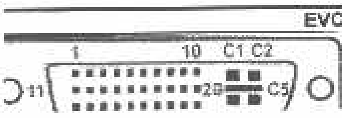
Mating face of DVI female

N#	SIGNAL	PIN#	SIGNAL
	T.M.D.S DATA 2-	16	HOT PLUG DETECT
	T.M.D.S DATA 2+	17	T.M.D.S DATA 0-
	T.M.D.S DATA 2/4 SHIELD	18	T.M.D.S DATA 0+
	T.M.D.S DATA 4-	19	T.M.D.S DATA 0/5 SHIELD
	T.M.D.S DATA 4+	20	T.M.D.S DATA 5-
	DDC CLOCK	21	T.M.D.S DATA 5+
	DDC DATA	22	T.M.D.S CLOCK SHIELD
	ANALOG VERT. SYNC	23	T.M.D.S CLOCK+
	T.M.D.S DATA 1-	24	T.M.D.S CLOCK-
	T.M.D.S DATA 1+		
	T.M.D.S DATA 1/3 SHIELD	C1	ANALOG RED
	T.M.D.S DATA 3-	C2	ANALOG GREEN
	T.M.D.S DATA 3+	C3	ANALOG BLUE
	+5V POWER	C4	ANALOG HORZ SYNC
	GND	C5	ANALOG GROUND

I's DVI cables extends signals up to 10 feet.

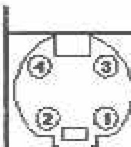
e **DVI CABLES** for more details.

EVC



Mating face of EVC female

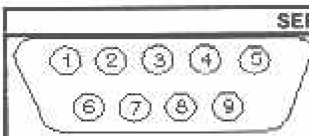
MAC KEYBOARD OR MOUSE



Mating face of 4 pin miniDIN female

PIN#	SIGNAL	PIN#	SIGN
1	DATA	3	+5
2	PWRN	4	GND

SERIAL MOUSE



Mating face of male 9D m

PIN#	SIGNAL	PIN#	SIGN
1	NC	6	NC
2	RX	7	RTS
3	TX	8	NC
4	DTR	9	NC
5	GND		

RS2

Mating face of male RS232 DB25

PIN#	SIGNAL	PIN#	SIGN
1	N/A	14	N/A
2	TXD	15	N/A
3	RXD	16	N/A
4	RTS	17	N/A
5	CTS	18	N/A
6	DSR	19	N/A
7	GND	20	DTR
8	DCD	21	N/A
9	N/A	22	RI
10	N/A	23	N/A
11	N/A	24	N/A
12	N/A	25	N/A
13	N/A		

USB TYPE A and B

Mating face of USB type A female

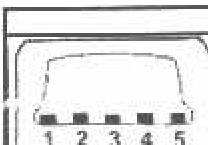
Mating face of USB type B female

PIN#	SIGNAL	PIN#	SIGN
1	+5	3	+Data
2	-Data	4	GND

NTI's USB KVM cables extend a VGA monitor and USB keyb to 15 feet.

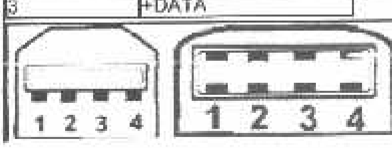
See **USB CABLES** for more details.

Mini USB TYPE B



Mating face of 5-pin Mini USB Type

PIN#	SIGNAL	PIN#	SIGN
1	+5	4	NC
2	-DATA	5	GND
3	+DATA		



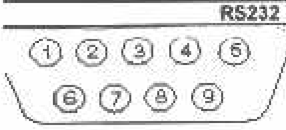
Mating face of 4 Type B female

IN#	SIGNAL	PIN#	SIGNAL
	T.M.D.S DATA 2+	19	1394 VG
	T.M.D.S DATA 2-	20	1394 VP
	T.M.D.S DATA 2 RTN	21	T.M.D.S DATA 0-
	SYNC RTN	22	T.M.D.S DATA 0+
	HORIZ. SYNC TTL	23	T.M.D.S DATA 0 RTN
	VERT. SYNC TTL	24	STEREO SYNC TTL
	T.M.D.S CLOCK RTN	25	DDC RTN
	CHARGING PWR INPUT+	26	DDC DATA SDA
	1394 PAIR A, DATA	27	DDC CLOCK SCL
)	1394 PAIR A, DATA+	28	+5 VDC
1	T.M.D.S DATA 1+	29	1394 PAIR B, CLOCK+
2	T.M.D.S DATA 1-	30	1394 PAIR B, CLOCK-
3	T.M.D.S. DATA 1 RTN	C1	RED VIDEO OUT
4	T.M.D.S CLOCK+	C2	GRN VIDEO OUT
5	T.M.D.S CLOCK-	C3	PX CLOCK OUT
6	USB DATA+	C4	BLU VIDEO OUT
7	USB DATA-	C5	COMMON GND RTN
8	**1394 SHIELD/CHARGING POWER INPUT-**		

TI's EVC adapters connect a VGA monitor to a EVC video port.

ee **EVC ADAPTERS** for more details.

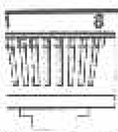
RS232 DB9 INTERFACE



Mating face of male RS232 DB9

N#	SIGNAL	PIN#	SIGNAL
	N/A	6	DSR
	RXD	7	RTS
	TXD	8	CTS
	DTR	9	N/A
	GND		

RS232 RJ45 INTERFACE



Mating face of female RS232 RJ45

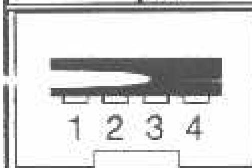
N#	SIGNAL	PIN#	SIGNAL
	RTS	5	GND
	DTS	6	RXD
	TXD	7	DSR
	GND	8	CTS

PIN#	SIGNAL	PIN#	SIGN
1	+5	3	+DAT
2	-DATA	4	GND

IEEE 1394

Mating face of 6-pin FireWire Socket

PIN#	SIGNAL	PIN#	SIGN
1	POWER	4	TPB+
2	GND	5	TPA-
3	TPB-	6	TPA+



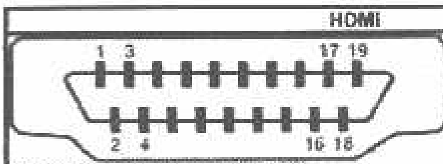
Mating face of 4-pin FireWire Socket

PIN#	SIGNAL	PIN#	SIGN
1	TPB-	3	TPA-
2	TPB+	4	TPA+

NTI's IEEE 1394 FireWire cables and adapters extend firewi meters.

See **FIREWIRE CABLES & ADAPTERS** for more details.

HDMI

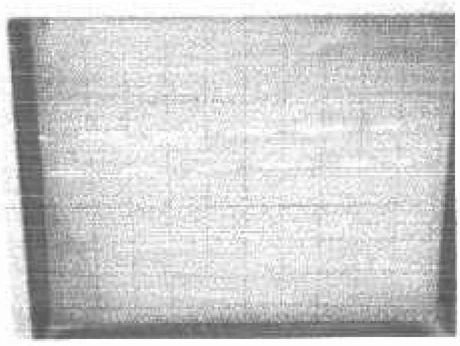


Mating face of HDMI Type-A male

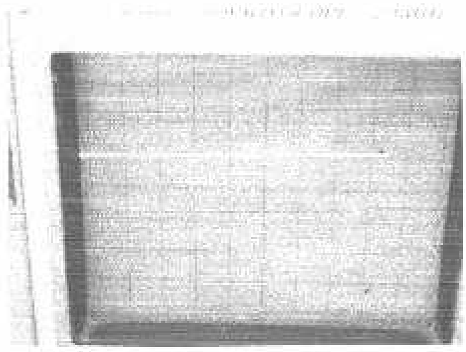
PIN#	SIGNAL	PIN#	SIGNAL
1	TMDS Data2+	11	TMDS Clock Shiel
2	TMDS Data2 Shield	12	TMDS Clock-
3	TMDS Data2-	13	CEC (not used)
4	TMDS Data1+	14	Reserved (N.C. or
5	TMDS Data1 Shield	15	SCL
6	TMDS Data1-	16	SDA
7	TMDS Data0+	17	DDC/CEC Ground
8	TMDS Data0 Shield	18	+5V Power
9	TMDS Data0-	19	Hot Plug Detect
10	TMDS Clock+		

NETWORK TECHNOLOGIES INCORPORATED

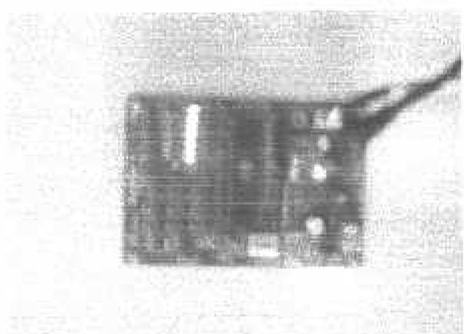
1275 Danner Drive
Aurora, OH 44202
Tel: 330-562-7070
Fax: 330-562-1999



Hasil Pengukuran Pada Saat Mouse Atau Keyboard Ditekan

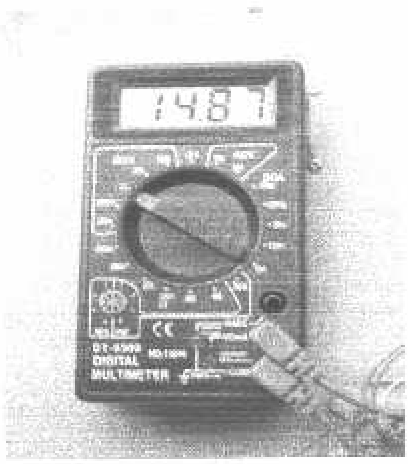


Hasil Pengukuran Pada Saat Mouse Dan Keyboard Tidak Ditekan



Hasil Pengujian Pada Mikrokontroler

Hasil Pengujian Pada LCD



Hasil Pengukuran Outputan Relay Pada Saat Tidak Aktif

Hasil Pengukuran Outputan Relay Pada Saat Tidak Aktif

Hasil Pengukuran Tegangan Monitor Pada Saat Aktif

Hasil Pengukuran Tegangan Monitor Pada Saat Standby

Hasil Pengukuran Arus Monitor Pada Saat Aktif

Hasil Pengukuran Arus Monitor Pada Saat Standby