ALAT PENGUBAH TEKS MENJADI SUARA SEBAGAI ALAT BANTU KOMUNIKASI PADA PENDERITA TUNA WICARA BERBASIS MIKROKONTROLER AT89S8252

SKRIPSI

Diajukan Untuk Memenuhi Salah Satu Syarat Memperoleh Gelar Sarjana Teknik
Pada Jurusan Teknik Elektro S-1 Konsentrasi Elektronika

Oleh :
MOHAMMAD ULINNUHA
02 17 119

KONSENTRASI ELEKTRONIKA
JURUSAN TEKNIK ELEKTRO S-1
FAKULTAS TEKNOLOGI INDUSTRI
INSTITUT TEKNOLOGI NASIONAL
MALANG
2007

LEMBAR PERSETUJUAN

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ABSTRAKSI

ALAT PENGUBAH TEKS MENJADI SUARA SEBAGAI ALAT BANTU KOMUNIKASI PADA PENDERITA TUNA WICARA BERBASIS MIKRIKONTROLER AT89S8252

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Kata Kunci : *Keypad, Mikrokontroler*, ISD, *Speaker, Teks ke Suara*

Media komunikasi berupa lisan sangat penting untuk berinteraksi dengan sesama. Tetapi diantara kita banyak yang mengalami gangguan pada lisannya sehingga sulit berkomunikasi dengan orang lain. Karena diantara kita sedikit yang mengerti bahasa isyarat maka komunikasi antara orang normal dan penderita tuna wicara akan terhambat.

Alat pengubah teks menjadi suara merupakan salah satu solusi agar orang normal dengan penderita tuna wicara dapat berkomunikasi dengan baik dan tidak terjadi kesalahpahaman. Dari segi penggunaan alat ini sangat mudah digunakan karena si pengguna hanya mengetikkan kata yang ingin di ucapkan dan alat tersebut akan mengucapkan sesuai dengan kata yang di masukkan.

Kata yang didapat dimasukkan merupakan kata yang digunakan dalam bahasa sehari-hari. Suara yang dihasilkan merupakan susunan suku kata dari kata yang dimasukkan. Untuk suku kata dengan susunan V, VK, KV, KKV dan KVK alat ini mampu mengubah teks menjadi suara dengan baik, tetapi untuk suku kata yang menggunakan "ng" alat ini tidak dapat mengubah suara dengan baik.

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Alhamdulillah, puji syukur kehadirat-Mu Ya Allah yang telah memberikan rahmat dan hidayah-Nya, sehingga penyusun dapat menyelesaikan skripsi ini dengan judul "Alat Pengubah Teks Menjadi Suara Sebagai Alat Bantu Komunikasi Pada Penderita Tuna Wicara Berbasis Mikrokontroler AT89S8252". Skripsi ini merupakan persyaratan kelulusan Studi di Jurusan Teknik Elektro S-1 Konsentrasi Teknik Elektronika ITN Malang dan untuk mencapai gelar Sarjana Teknik.

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Penyusun telah berusaha semaksimal mungkin dan menyadari sepenuhnya akan keterbatasan pengetahuan dalam menyelasaikan laporan ini. Untuk itu

penyusun mengharapkan saran dan kritik yang membangun dari pembaca demi kesempurnaan laporan ini.

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Malang, Maret 2007

Penyusun

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BAB I

PENDAHULUAN

1.1 Latar Belakang

Manusia merupakan makhluk sosial dimana setiap orang selalu membutuhkan bantuan orang lain. Komunikasi antar sesama manusia sangatlah penting guna terjalinnya interaksi dengan sesama. Media yang digunakan untuk berkomunikasi dengan sesama manusia dapat berupa lisan maupun tulisan. Media itulah yang biasanya digunakan dalam masyarakat pada umumnya karena media tersebut mudah untuk dimengerti oleh manusia.

Disisi lain banyak diantara kita yang mengalami gangguan pada lisannya schingga mereka sulit berkomunikasi secara lisan dengan orang lain. Orang-orang tersebut yang biasa kita kenal atau kita sebut dengan penderita tuna wicara. Umumnya penderita tuna wicara berkomunikasi dengan orang lain menggunakan bahasa isyarat, tetapi tidak semua atau bahkan sedikit dari kita yang mengerti dengan bahasa isyarat tersebut. Dengan sedikitnya orang yang mengerti bahasa isyarat tersebut mengakibatkan penderita tuna wicara tidak dapat berkomunikasi dengan baik kepada orang lain schingga pergaulan mereka menjadi sangat terbatas. Bahkan diantara mereka biasanya akan minder atau malu bila bertemu dengan orang lain.

Salah satu solusi yang dapat dilakukan supaya antara orang normal dengan penderita tuna wicara dapat berkomunikasi dengan baik dan tidak terjadi salah pengertian antara orang-orang tersebut, maka kita dapat menggunakan suatu alat

yang dapat mengubah teks menjadi suara. Dari segi manfaat alat ini sangat membantu sekali bagi para penderita tuna wicara. Dari segi penggunaan alat ini tergolong alat yang mudah digunakan karena pengguna hanya tinggal menuliskan kata yang akan dia ucapkan dan alat tersebut akan mengucapkan seperti yang ditulis oleh penggunanya.

Mikrokontroler merupakan salah satu komponen elektronika yang dapat digunakan untuk merancang dan membuat alat tersebut karena mikrokontroler dapat menjalankan suatu proses yang mana sudah dirancang sedemikian rupa sehingga dapat berjalan sesuai dengan program yang dimasukkan. Dengan demikian kita dapat merealisasikan suatu alat yang akan kita rancang menggunakan mikrokontroler.

1.2 Rumusan Masalah

Dalam perancangan dan pembuatan alat ini terdapat beberapa rumusan masalah sebagai berikut :

1. Bagaimana merancang suatu piranti yang dapat mengubah teks dari keypad, menampilkan ke LCD dan menyimpan ke dalam memori.
2. Bagaimana merancang dan menguji sistem mikrokontroler AT89S8252 yang berhubungan dengan ISD.
3. Bagaimana cara menggunakan mikrokontroler AT89S8252 sebagai pengontrol utama dari sistem tersebut.

1.3 Batasan Masalah

Agar permasalahan yang ada dapat dijelaskan secara tepat dan terhindar dari permasalahan yang tidak sesuai dengan topik yang akan dibahas maka dianggap perlu adanya batasan masalah. Adapun batasan masalah pada tugas akhir ini antara lain :

1. Menggunakan mikrokontroler AT89S8252 sebagai pengontrol utama.
2. Teks yang dimasukkan adalah teks yang berupa kata yang ditulis dalam bahasa Indonesia yang hanya berupa huruf tanpa menggunakan angka.
3. Kata yang akan dimasukkan merupakan kata yang digunakan dalam bahasa sehari-hari.
4. Tidak membedakan intonasi suara untuk masukan, baik berupa kalimat pertanyaan maupun kalimat perintah.
5. Suara yang dihasilkan berupa susunan suku kata dari kata yang dimasukkan.
6. Tidak membahas catu daya yang digunakan.

1.4 Tujuan

Adapun tujuan dari tugas akhir ini adalah merancang dan membuat alat pengubah teks menjadi suara sebagai alat bantu komunikasi pada penderita tuna wicara.

1.5 Metodologi

Penyusunan tugas akhir ini didasarkan pada masalah yang bersifat aplikatif, yaitu perencanaan dan perealisasian alat agar dapat menampilkan unjuk kerjanya sesuai dengan yang direncanakan dengan mengacu pada rumusan masalah. Untuk mencapai tujuan yang direncanakan, maka pada tugas akhir ini menggunakan metodologi sebagai berikut :

- **Study Literatur**

  Yaitu dengan melakukan studi ke perpustakaan untuk memperoleh teori serta gambaran tentang masalah yang akan dibahas serta mempelajari teori aplikasi dari mikrokontroler AT89S8252.

- **Perencanaan dan Pembuatan Alat**

  Dalam pembuatan alat ini menggunakan konsep sebagai berikut :

  - Perencanaan sistem secara keseluruhan (pembuatan blok diagram sistem).
  - Mendiskripsikan fungsi dari masing-masing blok diagram.
  - Membuat perangkat keras (*hardware*) dan perangkat lunak (*software*) dari alat tersebut.

- **Pengujian Alat**

  Pada pengujian alat kita dapat mengetahui unjuk kerja dari alat tersebut, apakah sesuai dengan dengan perencanaan yang telah kita rencanakan. Adapun pengujian alat yang akan dilakukan berupa pengujian per- blok dan pengujian dari keseluruhan alat tersebut.

- **Pengambilan Kesimpulan**

  Pengambilan kesimpulan berdasarkan atas pengujian dan pengukuran dari alat yang telah dibuat.

1.6 Sistematika Penulisan

Adapun sistematika dari penyusunan laporan tugas akhir ini adalah sebagai berikut :

BAB I :

Berisi latar belakang, rumusan masalah, batasan masalah, tujuan, metodologi dan sistematika penyusunan laporan tugas akhir.

BAB II :

Membahas tentang teori dasar, cara kerja rangkaian serta hubungan dengan perangkat yang digunakan.

BAB III :

Membahas perencanaan dari setiap rangkaian elektronika dan perangkat lunak yang digunakan.

BAB IV :

Membahas hasil pengujian terhadap alat yang telah dibuat, baik setiap blok rangkaian maupun secara keseluruhan.

BAB V :

Penutup berisi kesimpulan, saran dan daftar pustaka.

BAB II

DASAR TEORI

2.1 Mikrokontroler AT89S8252

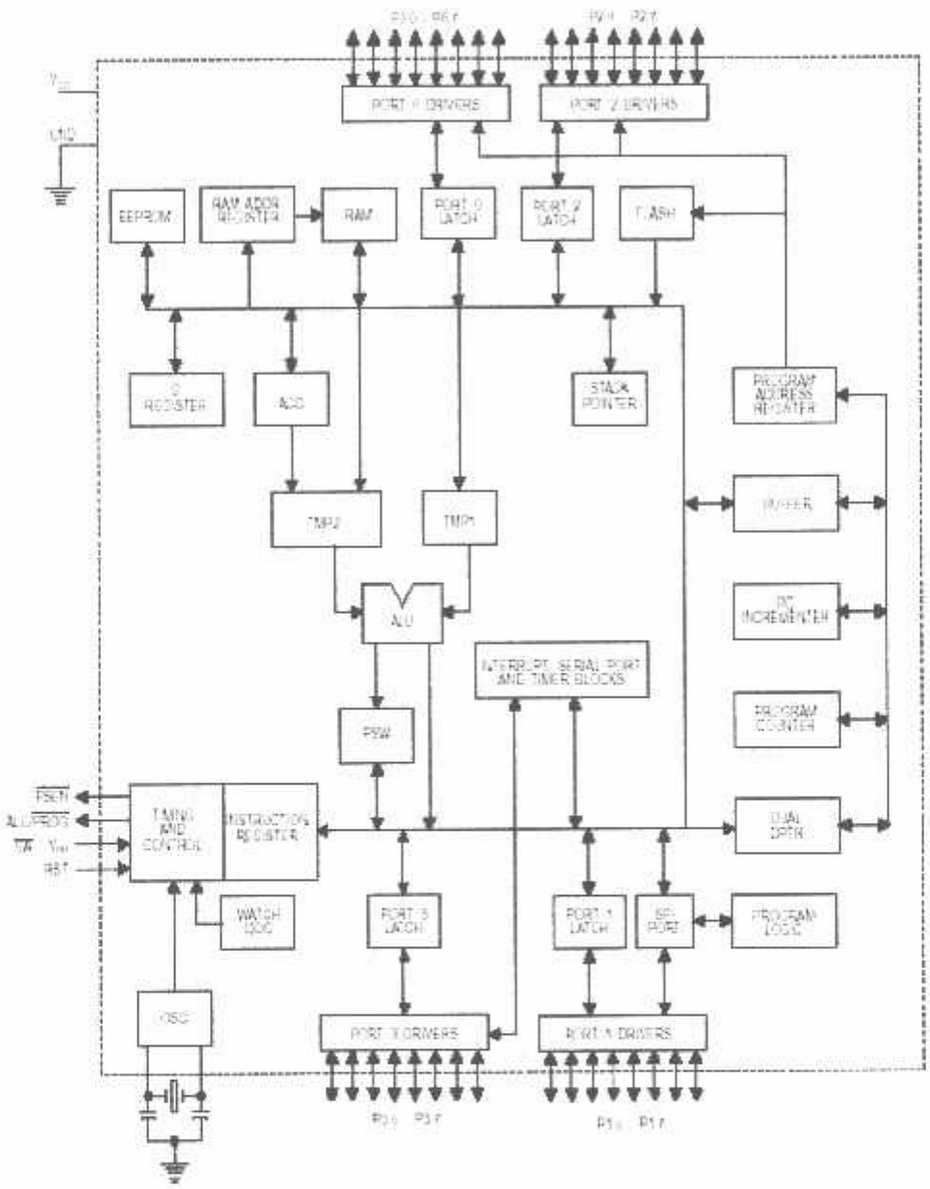
Mikrokontroler AT89S8252 adalah sebuah mikrokontroler CMOS 8-bit performa tinggi yang hemat daya dengan 8Kbytes *Downloadable Flash Programmable and Erasable Read-Only Memory* (Flash PEROM) dan 2Kbytes EEPROM. Mikrokontroler ini dibuat menggunakan teknologi *high-density nonvolatile memory* milik Atmel dan kompatibel dengan set instuksi dan pin standart industri MCS-51. *On-chip downloadable Flash* memungkinkan memori program untuk diprogram ulang di dalam sistem melalui sebuah antarmuka serial SPI atau dengan sebuah pemprogram memori nonvolatile yang konvensional. Dengan mengkombinasikan sebuah CPU 8 bit dengan downloadable Flash pada sebuah chip monolitik. Atmel AT89S8252 adalah sebuah mikrokontroler yang menyediakan sebuah solusi dengan fleksibilitas yang tinggi dan biaya yang efektif untuk berbagai aplikasi control.

Downloadable Flash dapat mengubah sebuah byte tunggal dalam satu waktu dan dapat diakses melalui antarmuka serial SPI serial port interface. Dengan menahan RESET akan mengaktifkan bus SPI ke dalam sebuah antarmuka pemprograman serial dan memungkinkan memori program untuk ditulis kepadanya ataupun dibaca darinya ketika tidak ada bit lock yang diaktifkan.

Mikrokontroler AT89S8252 memiliki kelengkapan sebagai berikut :

- Kompatibel dengan mikrokontroler MCS-51
- 8Kbyte Downloadable Flash memori
- 2Kbyte EEPROM
- Tegangan operasi antara 4 volt sampai 6 volt
- Frekuensi kerja 0 sampai 24 MHz
- 3 level program memori lock
- 256 byte RAM internal
- 32 I/O yang dapat dipakai semua
- 3 buah timer/counter 16 bit
- Programmable UART (serial port)
- SPI serial interface
- Programmable watchdog timer
- Dual data pointer

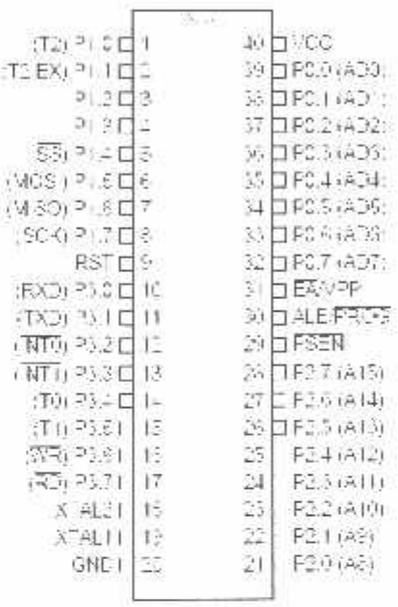
Adapun blok diagram mikrokontroler AT89S8252 dapat dilihat di dalam gambar 2.1 berikut :



Gambar 2.1 Blok Diagram AT89S8252 [1]

2.1.1 Susunan Pena Mikrokontroler MCS-51

Mikrokontroler MCS-51 memiliki pena berjumlah 40 buah. Umumnya kemasan mikrokontroler ini adalah DIP (Dual in Line Packaged).Adapun konfigurasi pin dari mikrokontroler AT89S8252 dapat dilihat dalam gambar 2.2 berikut :



Gambar 2.2 Konfigurasi pin Mikrokontroler AT89S8252 [2]

Masing-masing pena pada mikrokontroler ini memiliki kegunaan sebagai berikut:

a. Pena VCC

   Dihubungkan dengan tegangan kerja +5 volt

b. GND

   Ground sistem

c. Port 0

   Port 0 merupakan port 8 bit yang bersifat open drain dua arah. Sebagai port keluaran, tiap pena dapat menerima masukan TTL (*transistor-*

transistor logic). Saat logika 1 dituliskan pada port, pena port dapat digunakan sebagai masukan dengan impedansi tinggi.

d. Port 1

Port 1 merupakan port I/O dua arah yang telah dilengkapi pull up internal. Port ini dapat memberi daya atau menerima 4 masukan TLL (*transistor-transistor logic)*. Jika suatu logika 1 ditulis pada port ini maka port akan dibuat tinggi oleh pull up internal dan dapat digunakan sebagai masukan. Pada saat sebagai port masukan, port ini akan rendah (externally pulled low) dan port ini akan memberi daya karena adanya pull up internal.

e. Port 2

Port 2 merupakan port parallel 8 bit yang bersifat dua arah dan memiliki pull up internal. Penyangga pada port 3 ini dapat menangani 4 masukan TLL (*transistor-transistor logic)*. Jika suatu logika 1 dituliskan pada port ini, maka port ini akan dibuat tinggi oleh pull up internalnya. Port 2 mengirimkan byte tinggi dari alamat selama pengaksesan dari program memori luar dan selama penulisan data memori luar yang menggunakan alamat 16 bit.

f. Port 3

Port 3 merupakan 8 bit dua arah dengan pull up internal. Keluaran dari port 3 ini dapat memberi daya atau menerima sebanyak 4 masukan TTL (*transistor-transistor logic)*. Jika suatu logika 1 dituliskan pada port ini, maka port ini akan dibuat tinggi oleh pull up internal dan dapat digunakan sebagai masukan. Selain sebagai port paralel biasa, port 3 ini juga

memiliki fungsi khusus, Adapun fungsi-fungsi khusus port 3 ini diperlihatkan pada table 2.1 berikut.

Tabel 2.1 Fungsi Khusus Port 3 [3]

Port	**Fungsi Khusus**
P3.0	RXD (masukan port serial)
P3.1	TXD (keluaran Port serial)
P3.2	INT0 (masukan interupsi luar 0)
P3.3	INT1 (masukan interupsi luar 1)
P3.4	T0 (masukan luar Timer/Counter 0)
P3.5	T1 (masukan luar Timer/Counter 1)
P3.6	WR (pulsa penulisan data memori luar)
P3.7	RD (pulsa pembacaan data memori luar)

g. Reset (RST)

Masukan untuk Reset. Suatu logika tinggi selama dua siklus pada pena RST akan menyebabkan terjadinya proses reset.

h. ALE

Address Latch Enable merupakan suatu pulsa keluaran untuk mengaitkan (latch) byte bawah dari alamat selama mengakses memori luar.

i. PSEN

Program Store Enable adalah pulsa pengaktif untuk membaca program memori luar. Saat mikrokontroler melaksanakan instruksi dari program

memori luar, PSEN akan diaktifkan dua kali tiap siklus mesin, kecuali pada saat pengaksesan data memori luar.

j. EA

External Access Enable, EA harus dihubungkan dengan ground jika ingin mengakses dari program memori luar dengan alamat 0000H sampai FFFFH. EA harus dihubungkan dengan VCC jika menggunaka program memori internal.

k. XTAL1

Masukan untuk penguat inverting osilator dan masukan rangkaian clock internal.

l. XTAL2

Keluaran dari penguat inverting osilator.

2.1.2 Peta Memori Mikrokontroler MCS-51

Mikrokontroler MCS-51 memiliki 2 jenis memori yaitu :

a. Memori internal (on-chip memori)

Memori internal yang terpasang pada mikrokontroler MCS-51 terbagi menjadi ROM/EPROM dan RAM. ROM/EPROM berukuran 4K- 8Kbyte digunakan untuk menyimpan program. Sementara RAM berkapasitas 128 byte- 256byte digunakan untuk menyimpan data sementara.

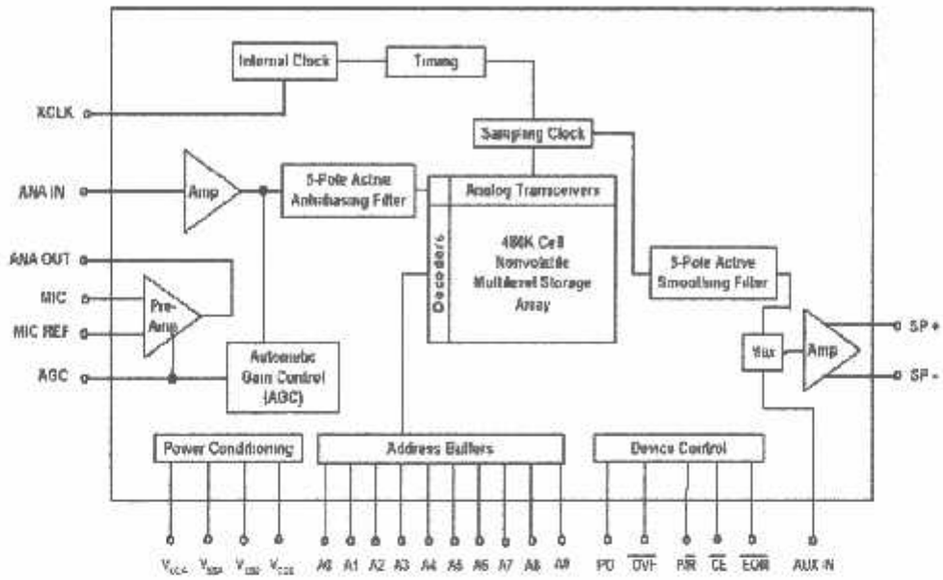
b. Memori eksternal

Memori eksternal dapat ditambahkan pada mikrokontroler MCS-51 apabila diperlukan kapasitas memori yang lebih besar. Memori eksternal

tersebut dapat berupa EPROM sampai kapasitas 64Kbyte untuk menyimpan program dan RAM sampai kapasitas 64Kbyte untuk menyimpan data juga dapat di tambahkan. Namun jika menggunakan memori luar maka port 0 dan port 2 terpaksa digunakan untuk menghubungkan memori tersebut schingga tidak dapat dipakai sebagai port parallel biasa.

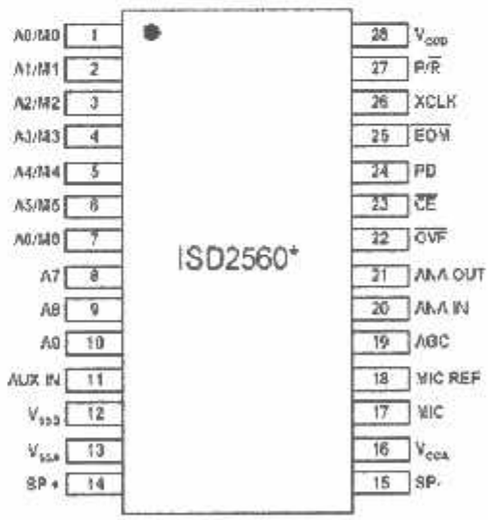
2.2 Information Storage Device (ISD) 2500

Peralatan penyimpan informasi suara atau ISD seri 2500 mempunyai kualitas yang sangat bagus dengan durasi penyimpanan 60 sampai 120 detik. Peralatan CMOS yang ada didalamnya adalah *Chip Oscilator, Microphone Preamplifier, Automatic Gain Control, Antiliasing Filter, Smouthing Filter Speaker Amplifier.* Secara keseluruhan seri ISD 2500 dapat melakukan sebuah perekaman atau pemutaran ulang pesan dengan komponen sederhana seperti mikropon, speaker, beberapa komponen penunjang, dua buah saklar dan sumber tegangan. Rekaman akan disimpan dalam sel memori yang tidak mudah hilang *(nonvolatile).* Teknik penyimpanan analog langsung, dengan jalan sinyal suara (voice) dan bunyi disimpan secara langsung dalam bentuk analog kedalam memori EPROM. Penyimpanan analog langsung memungkinkan reproduksi suara secara alami dalam satu chip tunggal. Adapun blok diagram seri ISD2500 dapat dilihat dalam gambar 2.3 berikut :



Gambar 2.3 Blok Diagram Seri ISD 2500 [4]

ISD2500 kompatibel dengan mikrokontroler AT89C52 sehingga pengalamatan dan jalur kendali dapat dihubungkan dengan mikrokontroler. Adapun susunan kaki-kaki dari ISD 2500 dapat dilihat dalam gambar 2.4 berikut :



Gambar 2.4 Susunan Kaki-kaki ISD 2500 [5]

Penjelasan dari fungsi spesifik masing-masing kaki dari ISD2500 adalah sebagai berikut :

- *Voltage Input* (Vcca, Vccd)

  Analog dan digital sirkuit yang terdapat didalam chip ISD menggunakan bus power yang terpisah untuk meminimalisasi noise. Pin power harus dihubungkan sedekat mungkin dengan sumber tegangan.

- *Ground Input* (Vssa, Vssd)

  Sama seperti Vccd dan Vcca, analog input dan digital sirkuit di dalam ISD 2500 menggunakan bus ground yang terpisah untuk meminimalisasi noise. Pin harus dihubungkan sedekat mungkin dengan ground.

- *Power Down Input* (PD)

  Ketika sedang tidak digunakan untuk merekam atau menyalakan, pin PD harus diberi logika tinggi. Ketika pulsa *overflow* (OVF) rendah maka PD harus dibawa ke logika tinggi untuk mereset addres pointer kembali ke awal perekam atau playback.

- *Chip Enable Input* (CE)

  Pin CE diberi logika rendah untuk membolehkan operasi perekaman atau playback. Alamat input dan *playback/record input* (P/R) ditahan dengan adanya transisi turun dari CE.

- *Playback/Record Input* (P/R)

  Input ditahan dengan adanya transisi turun dari pin CE. Logika tinggi akan memilih *playback cycle* dan logika rendah untuk memilih *record cycle*. Untuk *record cycle* alamat input menetapkan mulainya alamat dan

merekam secara kontinu sampai PD atau CE ke transisi tinggi atau dengan adanya *overflow*. Ketika *record cycle* berhenti dengan adanya transisi tinggi dari PD atau CE sinyal *End Of Massage* (EOM) di simpan di alamat terakhir di memori. Untuk *Playback cycle* alamat input menetapkan mulainya dan akan memutar suara perekam sampai alamat EOM ditemukan.

- *End Of Massage/Run Output* (EOM)

  Sebuah alamat akan dimasukkan secara otomatis diakhir masing-masing perekam. Pulsa Output EOM akan rendah untuk setiap akhir periode dari masing-masing perekam.

- *Microphone Input* (MIC)

  Digunakan untuk mentransfer sinyal suara ke *on-chip preamplifier*. Rangkaian *On-Chip Automatic Gain Control* (AGC) untuk mengontrol penguatan dari penguat mulai dari -15 sampai 24 dB.

- *Microphone Reference Input* (MIC REF)

  Adalah input pembalik ke *microphone preamplifier* untuk memberikan *noise canceling* atau *common mode rejection input* ke IC ini ketika dihubungkan ke sebuah *mikrofon diferensial*.

- *Over Flow Output* (OVF)

  Sinyal pulsa rendah pada akhir tempat memori mengindikasikan bahwa IC ini telah terpenuhi dan pesan telah melebihi kapasitas. Keluaran OVF kemudian diikuti masukan CE sampai pulsa PD telah mereset. Pin ini juga

dapat digunakan untuk menambah beberapa IC ISD2500 schingga durasi dari *record/playback* menjadi lebih lama.

- *Automatic Gain Control* (AGC)

  AGC secara dinamik mengubah penguatan dari penguat mula untuk mengimbangi lebar jarak dari mikrofon input. AGC memberikan jarak secara penuh dari suara rendah ke tinggi untuk direkam dengan distorsi minimal.

- *Analog Output* (ANA OUT)

  Pin ini memberikan keluaran penguat mula ke pengguna. Tegangan penguatan dari penguat mula ditentukan oleh level tegangan dari pin AGC.

- *Analog Input* (ANA IN)

  Pin masukan analog akan mentransfer sinyal kedalam *chip* untuk perekaman. Untuk masukan mikrofon pin ANA OUT harus dihubungkan ke kapasitor eksternal ke pin ANA IN. Jika permintaan input diperoleh dari sumber lain dari mikrofon maka sinyal ini dapat langsung dikopel oleh kapasitor ke pin ANA IN.

- *Eksternal Clock Input* (XCKL)

  Untuk ISD2500 mempunyai sebuah *pull-down internal*. Frekuensi *clock sampling* internal ± 1% dari spesifikasi. Frekuensi ini berfariasi dari ± 2,25% berada pada suhu kamar dan dalam range tegangan operasi. *Internal clock* mempunyai toleransi ± 5% pada temperature dan tegangan kerja. Jika power suplay yang digunakan mempunyai tekanan tinggi maka maka alat ini dapat di *clock* langsung pada pin XCLK. *Duty Cycle* pada

masukan *clock* tidak perlu dipermasalahkan karena *clock* dengan segera dibagi dua. Jika pin XCLK tidak digunakan harus dihubungkan ke ground.

- *Speaker Output* (SP+/SP-)

  ISD2500 telah mempunyai *driver onchip diferensial speaker* yang sanggup menampung beban 50 mW dalam 16 Ω dari AUX IN. Speaker output berada pada level Vssa selama proses *record* dan *power down.*

- *Auxiliry Input* (AUX IN)

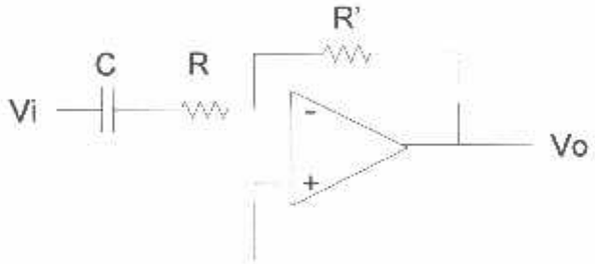
  AUX IN dihubungkan langsung ke kaki keluaran amplifier dan keluaran speaker ketika CE, PR berada pada logika tinggi dan *playback* tidak aktif.

- *Addres/Mode Input* (AX/MX)

  Mempunyai dua fungsi tergantung pada level dari dua *most significant bit (MSB)* dari alamat tersebut (A8 dan A9). Jika salah satu atau kedua dari MSB berlogika rendah maka semua input dianggap sebagai bit alamat dan digunakan sebagai awal alamat untuk proses *record* atau *playback cycle* terbaru. Alamat input ditahan oleh transisi turun dari CE. Jika kedua MSB berlogika tinggi maka masukan *addres/mode* dianggap bit mode ISD2500.

2.3 Penguat Sinyal AC

Di dalam beberapa aplikasi dibutuhkan suatu alat yang digunakan untuk memberikan penguatan pada sinyal AC sedangkan sinyal DC yang muncul harus diblok. Sebuah sinyal AC yang sangat sederhana dan stabil ditunjukkan dalam gambar 2.5, dimana kapasitor C memblok komponen DC dari sinyal input dan bersama dengan R menentukan frekuensi *cut off* bawah dari penguatan secara keseluruhan. Adapun gambar penguat sinyal AC dapat ditunjukkan pada gambar 2.5 berikut :



Gambar 2.5 Penguat Sinyal AC [6]

Tegangan keluaran Vo yang dihasilkan dari persamaan rangkaian gambar diatas :

$$Vo = -\frac{R'}{R}Vi$$

Atau

$$Av = \frac{Vo}{Vi} = -\frac{R'}{R}$$

Dari persamaan di atas dapat kita ketahui bahwa frekuensi cut off adalah :

$$F_c = -\frac{1}{2\pi RC}$$

2.4 Liquid Crystal Display (LCD)

LCD model M1641 produksi SEIKO *Instrument Inc. Corporation* memiliki spesifikasi sebagai berikut :

a. Menampilkan 16 karakter dengan 5 x 7 *dot matrik.*

b. Pembangkit karakter ROM untuk 192 jenis karakter.

c. Pembangkit karakter RAM untuk 8 jenis karakter.

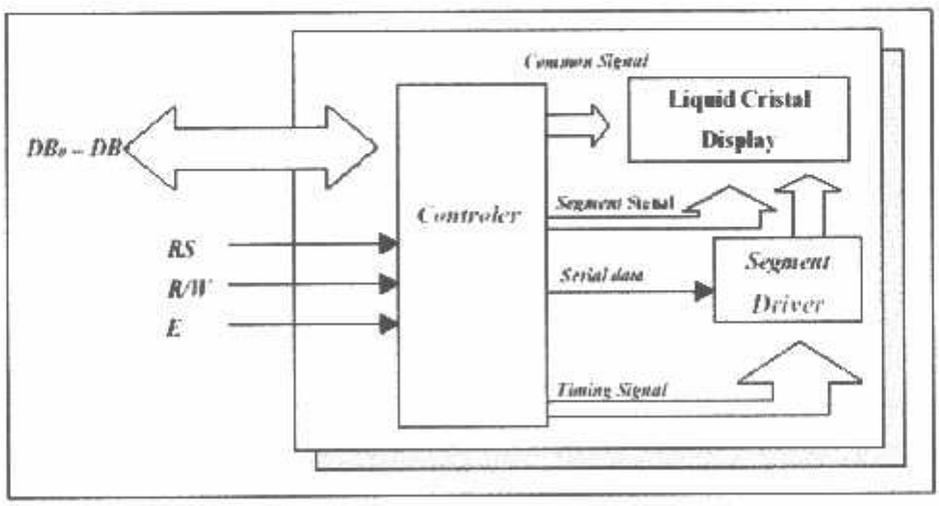
d. 80 x8 bit data RAM.

e. Antarmuka dengan 4 bit atau 8 bit MPU.

f. Tegangan catu 5 volt dan temperature operasi 0 – 500 °C

g. Otomatis reset saat di hidupkan.

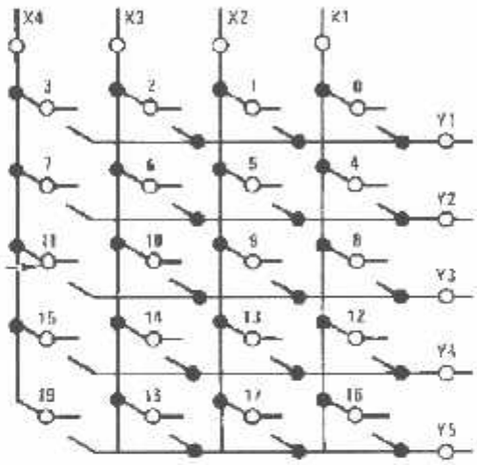
Masukan yang diperlukan untuk mengendalikan modul LCD ini berupa bus data yang masih termultipleks dengan bus alamat serta 3 bit sinyal kontrol yaitu RS, R/W dan E. Sementara pengendali dot matriks LCD dilakukan secara internal oleh kontroler yang sudah terpasang pada modul LCD. Blok diagram dapat dilihat dalam gambar 2.6 berikut :



Gambar 2.6 Blok Diagram LCD M1641 [7]

2.5 *Keypad* dan *Enkoder Keypad*

Keypad merupakan komponen yang digunakan sebagai sarana untuk memasukkan data ke komputer atau minimum sistem. Untuk rangkaian *keypad* 4x4 yaitu dengan menggunakan 16 buah saklar tekan (*push button*) yang dirangkai dalam bentuk matrik. Gambar rangkaian ditunjukkan pada gambar 2.7 berikut :



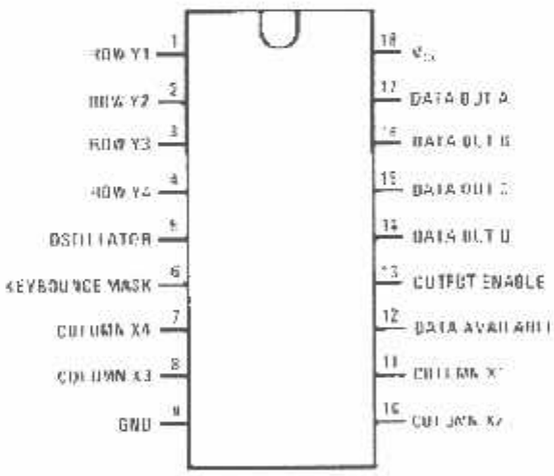
Gambar 2.7 Rangkaian Keypad dalam bentuk matrik [8]

Untuk menggunakan *keypad* diperlukan sebuah *driver*, *driver* yang biasa digunakan untuk menghubungkan *keypad* ke suatu minimum sistem adalah IC 74C922. *Keypad* juga dapat dihubungkan langsung dengan mikrokontroler . Jika kita menggunakan IC *Enkoder* (74C922) kita dapat dengan mudah mengirimkan data dari keypad ke minimum sistem karena di dalam IC *Enkoder* tersebut sudah memiliki beberapa kelengkapan seperti misalnya rangkaian *debouncing* yang hanya memerlukan kapasitor eksternal. Rangkaian internal register akan mengingat tombol terakhir yang ditekan meskipun tombol sudah dilepas. Selain itu dengan menggunakan IC *Enkoder keypad* juga dapat digunakan langsung

dengan cara menghubungkan langsung keypad dengan mikrokontroler, namun apabila menggunakan cara ini maka kita harus menyediakan port lebih banyak karena di setiap kolom dan basis dari keypad langsung dihubungkan dengan port mikrokontroler sehingga memerlukan lebih banyak port lagi.

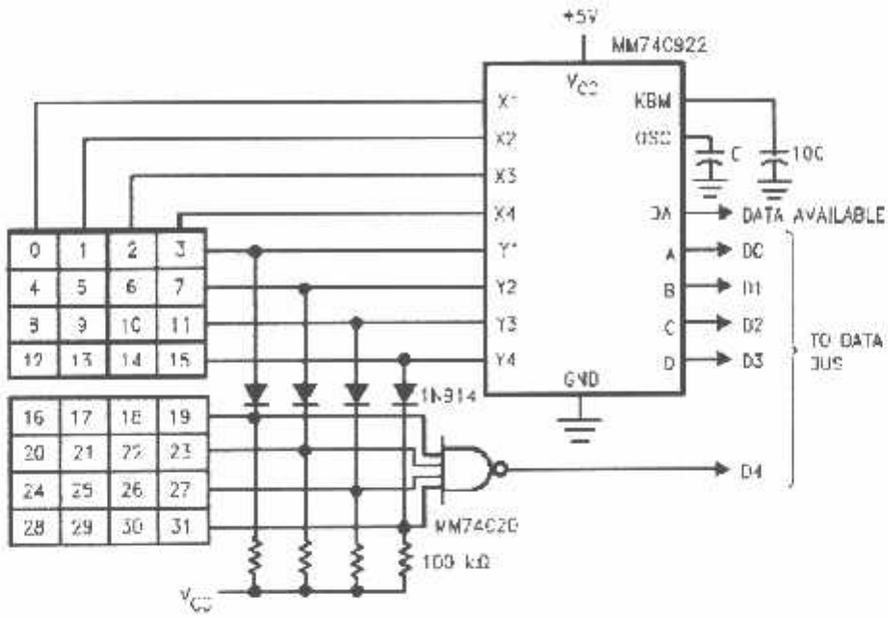
Enkoder adalah rangkaian logika kombinasional untuk mengubah bilangan desimal ke dalam kode biner. Sedangkan dekoder digunakan untuk menerjemahkan kode biner ke dalam kode khusus, seperti bilangan desimal yang ditampilkan dalam seven segment display.

Enkoder yang biasa diguanakan untuk mengubah nomor tombol dari sebuah *keypad* ke dalam kode biner adalah IC 74C922. IC ini dkenal sebagai 16 key encoder. Gambar IC 74C922 ditunjukkan dalam Gambar 2.8 berikut :



Gambar 2.8 Enkoder Keypad 74C922 [9]

Apabila kita menggunakan dua buah keypad maka kita memerlukan tam bahan komponen IC 74C20 untuk mengaktifkan atau sebagai jembatan dari keypad kedua. Adapun susunan dari dua buah keypad yang digabung dapat ditunjukkan dalam gambar 2. 9 berikut :



Gambar 2.9 Susunan dua buah keypad [10]

Jika salah satu tombol *keypad* ditekan, kolom dan baris pada lokasi tombol tersebut berada akan berlogika rendah. Misalkan ditekan nomor 3 (keypad pertama), maka kolom X4 dan baris Y1 akan berlogika rendah sehingga X4X3X2X1 akan sama dengan 0111 dan Y4Y3Y2Y1 sama dengan 1110. Penekanan tombol 3 ini dideteksi oleh *enkoder keypad* 74C922 dan diterjemahkan menjadi kode biner. Untuk penekanan tombol 3, keluaran EDCBA dari *enkoder* akan sama dengan 00011. Misalkan ditekan nomor 19 (keypad kedua), maka kolom X4 dan baris Y1 akan berlogika rendah sehingga X4X3X2X1 akan sama dengan 0111 dan Y4Y3Y2Y1 sama dengan 1110. Penekanan tombol 19 ini di deteksi oleh *enkoder keypad* 74C922 dan juga IC 74C20 karena merupakan keypad kedua dan data yang diterima diterjemahkan menjadi kode biner. Untuk penekanan tombol 19, keluaran EDCBA dari *encoder* akan sama dengan 10011.

Untuk lebih jelasnya kita dapat melihat Tabel Kebenaran dari Key Enkoder pada tabel 2.2 berikut :

Tabel 2.2 Tabel Kebenaran Key Encoder [11]

Switch Position		0 Y1.X1	1 Y1.X2	2 Y1.X3	3 Y1.X4	4 Y2.X1	5 Y2.X2	6 Y2.X3	7 Y2.X4	8 Y3.X1	9 Y3.X2	10 Y3.X3	11 Y3.X4	12 Y4.X1	13 Y4.X2	14 Y4.X3	15 Y4.X4	16 Y5'.X1	17 Y5'.X2	18 Y5'.X3	19 Y5'.X4
D																					
A	A	1	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1
T	B	0	0	1	1	0	0	1	1	0	0	1	1	0	0	1	1	0	0	1	1
A	C	0	0	0	0	1	1	1	1	0	0	0	0	1	1	1	1	0	0	0	0
O	D	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	0	0	0	0
U	D'	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1
T																					

Kondensator yang dihubungkan ke pin 5 diperlukan untuk melengkapi rangkaian osilator internal IC ini. Osilator ini diperlukan untuk melakukan penelusuran masukan-masukan X1...X4 dan Y1...Y4 guna mendeteksi tombol *keypad* yang ditekan. Kondensator pada pin 6 diperlukan untuk meredam getaran mekanik (*key bounce*) yang dapat timbul pada saat sebuah tombol ditekan. Sebuah registerinternal di dalam IC ini mengingat nomor terakhir yang ditekan, juga setelah tombol ini dilepaskan. Setelah *enkoder* mendeteksi nomor yang ditekan keluaran DA (*data available*) dari IC akan menjadi tinggi. Keluaran tinggi dari DA ini menyatakan bahwa data masukan telah diterima oleh *enkoder*. Setelah tombol dilepaskan, keluaran DA akan menjadi rendah.

2.6 Speaker

Speaker merupakan suatu transduser yang dapat mengubah dari energi listrik menjadi energi mekanik. Speaker biasanya di gunakan sebagai outputan dari suatu perangkat elektronika untuk menghasilkan sinyal suara.

BAB III

PERANCANGAN DAN PEMBUATAN ALAT

Dalam perencanaan alat ini dilakukan bertahap blok demi blok untuk memudahkan analisis sistem setiap bagian maupun sistem secara keseluruhan. Perencanaan dan pembuatan sistem ini terdiri atas dua bagian yaitu perencanaan perangkat keras dan perencanaan perangkat lunak. Beberapa aspek lain yang perlu dijelaskan dalam pembahasan bab ini adalah penentuan spesifikasi dari sistem yang dirancang, blok diagram dan prinsip kerja sistem.

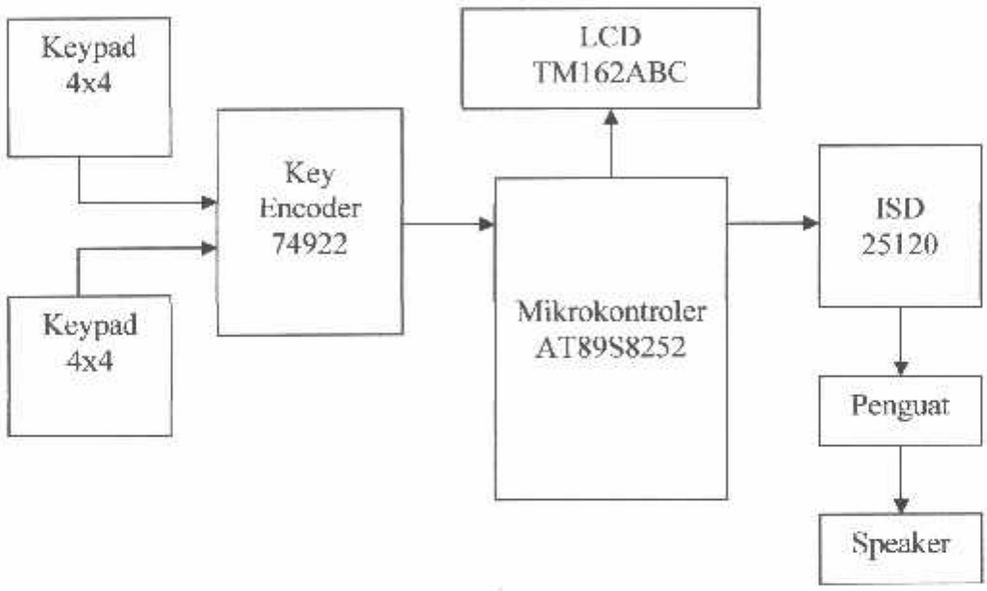
3.1 Spesifikasi Alat

Adapun spesifikasi alat yang direncanakan adalah sebagai berikut :

a. Alat yang dirancang menggunakan Mikrokontroller AT89S8252 sebagai pengontrol utama.
b. Masukan untuk mengetikkan kata berupa 32 tombol yang tersusun dari 2 buah *keypad* 4 x 4.
c. Hasil ketikan ditampilkan melalui LCD 2 x 16 karakter.
d. Database suara menggunakan pemutar/perekam suara ISD25120 dengan kapasitas 120 detik.
e. Alat dapat menampilkan suara sesuai dengan hasil ketikan yang disimpan di dalam RAM.

3.2 Perencanaan Blok Rangkaian

Pembuatan blok diagram rangkaian pengubah teks menjadi suara ini merupakan dasar dari perancangan sistem. Diagram blok ini nantinya yang akan digunakan untuk pengecekan masing-masing blok dari rangkaian seperti yang terlihat dalam Gambar 3.1.



Gambar 3.1 Blok Diagram Sistem

3.3 Prinsip Kerja Sistem

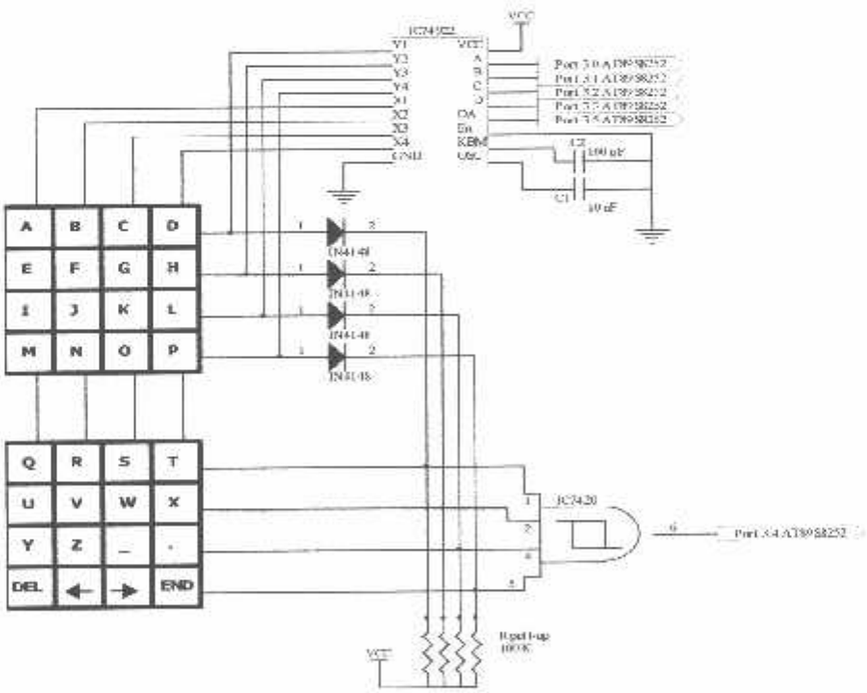
Prinsip kerja dari blok diagram sistem diatas adalah data dalam hal ini berupa kata-kata yang akan diolah mikrokontroler di masukkan melalui keypad. Data yang di keluarkan keypad dikodekan oleh key Enkoder agar data yang akan diolah dapat dibaca oleh mikrokontroler. Data yang diterima mikrokontroler disimpan ke dalam RAM mikrokontroler dan ditampilkan ke dalam LCD. Setelah mikrokontroler menerima perintah untuk mengeluarkan data yang telah disimpan

untuk diteruskan ke ISD, maka data tersebut di keluarkan oleh ISD sesuai dengan urutan alamat yang telah di olah oleh mikrokontroler. Karena suara yang dihasilkan oleh ISD kurang begitu keras maka kita membutuhkan suatu penguat audio sehingga kita dapat menentukan seberapa besar suara yang akan di keluarkan olah speaker.

3.4 Perancangan Perangkat Keras

3.4.1 *Keypad* dan *Enkoder Keypad*

Alat pengubah teks menjadi suara ini menggunakan 2 buah *keypad* 4 x4. Adapun *enkoder keypad* yang digunakan dalam alat ini adalah IC 74922. Rangkaian *keypad* dan *enkoder keypad* dapat dilihat pada Gambar 3.2



Gambar 3.2 Rangkaian *Keypad* dan *Enkoder Keypad*

IC 74922 adalah sebuah *enkoder keypad* yang digunakan untuk menangani *keypad* 4 x 4. Karena dalam pembuatan alat ini membutuhkan 32 tombol maka perlu dibuat rangkaian tambahan sehingga IC 74922 mampu menangani 32 tombol (2 buah *keypad* 4 x 4).

Dengan menggunakan rangkaian ini ketika tombol ke-2 *keypad* pertama (huruf B) ditekan maka kondisi logika pada X2 adalah '0' dan maka kondisi logika pada Y1 adalah '0', sedang kondisi logika pada pin baris dan kolom yang lain tetap '1'. Karena yang ditekan adalah *keypad* pertama maka dioda 1N4148 tidak ada yang aktif sehingga keluaran dari 7420 adalah '0'.

Akan tetapi ketika tombol ke-2 *keypad* kedua (huruf R) ditekan maka kondisi logika pada X2 adalah '0'. Karena yang ditekan adalah *keypad* kedua maka dioda 1N4148 menjadi aktif sehingga kondisi logika pada Y1 adalah '0' dan keluaran dari 7420 adalah '1', sedang kondisi logika pada pin baris dan kolom yang lain tetap '1'.

Ketika *keypad* kedua tidak ditekan maka masukan IC 7420 berada pada kondisi ambang. Resistor *pull up* digunakan untuk menjaga agar tidak terjadi kondisi ambang, melainkan logika '1'. Resistor *pull up* ini juga digunakan untuk mensuplai arus ketika tidak ada *keypad* yang ditekan. Ketika masukan 7420 dalam kondisi logika '1' maka tegangan masukannya (V_{IH}) adalah 3,15 V (dari data sheet). Karena arus yang dibutuhkan ketika logika '1' (I_{IH}) adalah 20 μA (dari data sheet) dan catu daya yang digunakan (Vcc) adalah 5V, maka nilai R *pull up* yang dibutuhkan adalah:

$$R_{pull\_up} = \frac{Vcc - V_{IH}}{I_{IH}} \qquad (3.1)$$

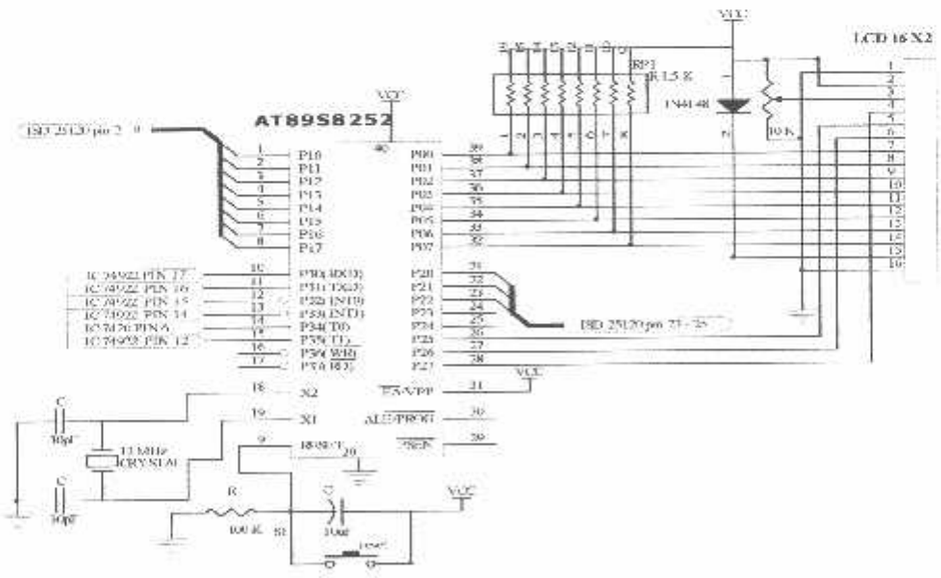
$$R_{pull\_up} = \frac{5V - 3{,}15V}{20\mu A}$$

$$R_{pull\_up} = 92{,}5k\Omega \approx 100k\Omega$$

3.4.2 Rangkaian Mikrokontroler AT89S8252

3.4.2.1 Minimum Sistem Mikrokontroler AT89S8252

Pada rangkaian ini komponen utamanya adalah unit mikrokontroler tipe AT89S8252 yang kompatibel dengan keluarga MCS-51. Alasan penggunaan mikrkontroler AT89S8252 karena mikrokontroler ini memiliki kapasitas RAM (*Random Access Memory*) yang lebih besar bila dibandingkan dengan keluarga MCS-51 yang lain sehingga jumlah kata yang dapat diolah menjadi lebih banyak. Sebagai otak dari pengolahan data dan pengontrolan alat, pin-pin AT89S8252 dihubungkan pada rangkaian pendukung membentuk suatu sistem minimum seperti dalam Gambar 3.3.



Gambar 3.3 Minimum sistem AT89S8252

Mikrokontroler AT89S8252 mempunyai 4 port, 32 jalur yang dapat diprogram menjadi masukan atau keluaran, pada perancangan ini pin-pin yang digunakan adalah:

Port 0 : digunakan untuk jalur data LCD.

Port 1 : digunakan untuk alamat ISD25120 (P1.0-P1.7 terhubung ke A_1 A_8 dari ISD25120).

P2.5 – P2.7 : digunakan untuk mengendalikan LCD, yaitu enable dan operasi baca tulis LCD.

P2.0 – P2.2 : digunakan mengendalikan ISD25120, yaitu *power down*, chip enable dan operasi *play/record*.

P3.0 – P3.4 : dihubungkan dengan keluaran dari *enkoder keypad*.

P3.5 : digunakan untuk mendeteksi sinyal DA (Data Available) dari *enkoder keypad*.

Pin18, Pin19 : digunakan sebagai masukan dari rangkaian osilator kristal. Rangkaian osilator kristal terdiri atas kristal osilator 12 MHz, kapasitor C_1 dan C_2 masing-masing 30pF (berdasarkan *data sheet*) akan membangkitkan pulsa *clock* yang akan menjadi penggerak bagi seluruh operasi internal MCU.

Pada rangkaian di atas, karena port 0 bersifat *open drain*, maka ketika mengeluarkan logika '0' maka akan terbaca sebagai logika ambang. Untuk itu dibutuhkan resistor *pull up* agar bisa memberikan logika '0'. Ketika memberikan logika '0' maka tegangan keluaran (V_{OL}) seharusnya adalah 0,5 V (dari data sheet). Karena arus yang dibutuhkan ketika logika '0' (I_{OL}) adalah 3,2 mA (dari

data sheet) dan catu daya yang digunakan (Vcc) adalah 5V, maka nilai R *pull up* yang dibutuhkan adalah:

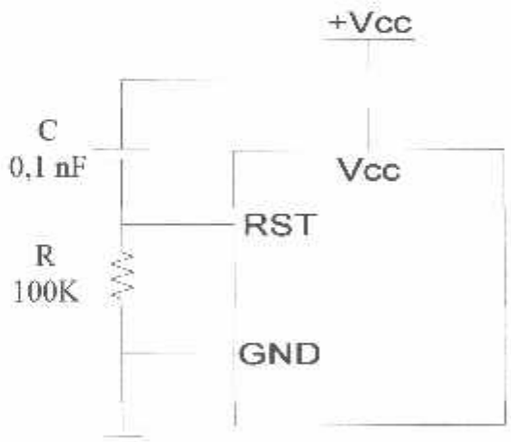
$$R_{pull\_up} = \frac{Vcc - V_{OL}}{I_{OL}} \qquad (3.2)$$

$$R_{pull\_up} = \frac{5V - 0{,}5V}{3{,}2mA}$$

$$R_{pull\_up} = 1406.25\,\Omega \approx 1{,}5k\Omega$$

3.4.2.2 Rangkaian *Reset*

Untuk m*ereset* mikrokontroler AT89S8252, maka pin RST diberi logika tinggi selama sekurangnya dua siklus mesin (2 x 12 periode osilator). Untuk membangkitkan sinyal *reset* kapasitor dihubungkan dengan Vcc dan sebuah *resistor* yang dihubungkan ke *ground*. Rangkaian *reset* ditunjukkan dalam gambar 3.4 sebagai berikut :



Gambar 3.4 Rangkaian *Reset* dan sctaranya.

Kristal yang digunakan mempunyai frekuensi sebesar 12 MHz, maka satu periode membutuhkan waktu sebesar :

$$T = \frac{1}{f_{XTAL}} \tag{3.3}$$

$$T = \frac{1}{12MHz}$$

$$T = 8{,}33x10^{-8}\text{s}$$

Sehingga waktu minimal logika tinggi yang dibutuhkan untuk *mereset* mikrokontroler adalah :

Reset (min) = T × periode yang dibutuhkan

$= 8{,}33 \times 10^{-8} \times 24 = 1{,}9992\ \mu s$

Jadi mikrokontroler membutuhkan waktu minimal 1,9992 μs untuk *mereset*. Waktu minimal inilah yang dijadikan pedoman untuk menentukan nilai R dan C. Dengan menggunakan pemisalan R = 100K dan t minimum adalah 2 μs maka untuk amannya dimisalkan = 4 μs maka :

$$t = 0{,}357 .R\ C \tag{3.4}$$

$4.10^{-6} = 0{,}357 \times 100\ K \times C$

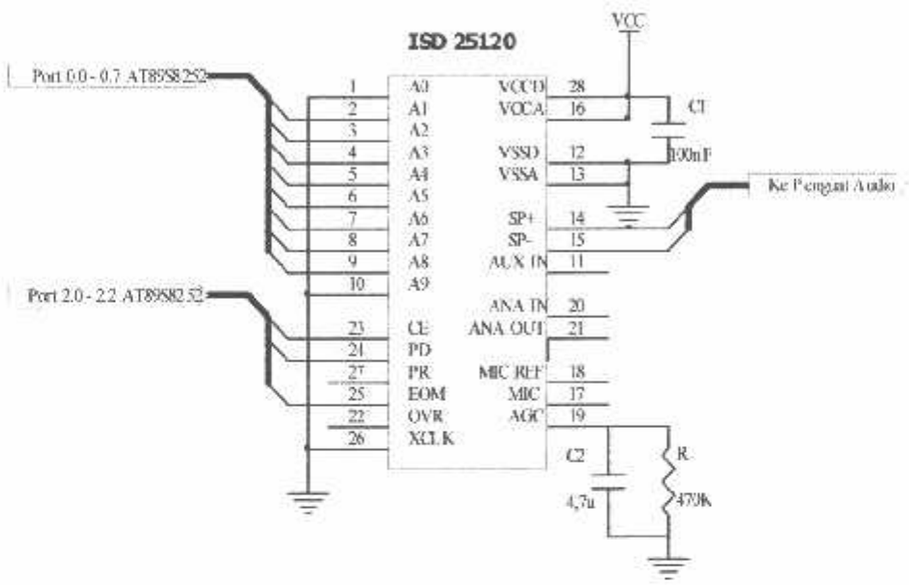
$C = 0.1\ nF$

telah memenuhi syarat minimal untuk dapat me-*reset* mikrokontroler AT89S8252

3.4.3 Pemutar/Perekam Suara ISD25120

Pada alat pengubah teks menjadi suara ini pemutar/perekam suara ISD25120 digunakan untuk menyimpan rekaman suara yang berupa suku kata-suku kata. Pemutar/perekam suara ISD25120 ini kompatibel dengan keluarga MCS-51, sehingga mudah untuk dihubungkan dengan mikrokontroler yang digunakan yaitu AT89S8252. Alasan penggunaan pemutar/perekam suara

ISD25120 adalah karena pemutar/perekam suara ini memiliki kapasitas yang cukup besar yaitu 120 detik yang terbagi menjadi 600 ruang alamat. Sebagai penyimpan rekaman suara, pin-pin ISD25120 dihubungkan pada rangkaian mikrokontroler membentuk suatu sistem minimum seperti dalam Gambar 3.5.



Gambar 3.5 Rangkaian ISD25120

Pemutar/perekam suara mempunyai 10 jalur alamat dan 3 buah pin kontrol. Pada perancangan ini pin-pin yang digunakan adalah:

A1-A8 : Alamat ISD yang dihubungkan ke mikrokontroler AT89S8252 port 1.

CE : digunakan untuk mengaktifkan ISD25120 dan dihubungkan ke port2.0.

PD : digunakan untuk merekam ke ISD25120 dan dihubungkan ke port2.1.

EOM : digunakan sebagai penanda akhir dari sebuah rekaman pada ISD25120 dan dihubungkan ke port2.2.

Pada pembuatan alat pengubah teks menjadi suara, karena pemutar/perekam suara ISD25120 memiliki durasi waktu 120 detik yang terbagi menjadi 600 ruang alamat (alamat 000h sampai dengan alamat 257h) sehingga

tiap ruang alamat memiliki durasi 0,2 detik. Karena durasi waktu yang dibutuhkan untuk mengucapkan 1 suku kata adalah 0,3 detik maka dibutuhkan 2 ruang alamat pada ISD25120 untuk menyimpan rekaman satu suku kata. Dengan demikian ISD25120 dapat menampung 300 suku kata. Adapun daftar suku kata yang telah di rekam ke dalam ISD25120 terdapat pada tabel 3.1 berikut :

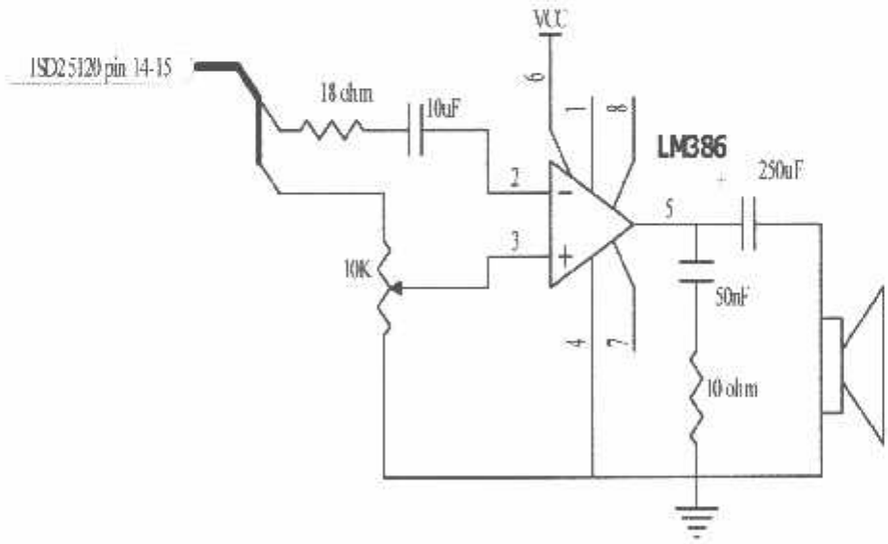
Tabel 3.1 Daftar Suku Kata yang di Rekam di ISD 25120

Alamat	**+0**	**+2**	**+4**	**+6**	**+8**
0	ba	be	bi	bo	bu
10	ca	ce	ci	co	cu
20	da	de	di	do	du
30	fa	fe	fi	fo	fu
40	ga	ge	gi	go	gu
50	ha	he	hi	ho	hu
60	ja	je	ji	jo	ju
70	ka	ke	ki	ko	ku
80	la	le	li	lo	lu
90	ma	me	mi	mo	mu
100	na	ne	ni	no	nu
110	pa	pe	pi	po	pu
120	qa	qe	qi	qo	qu
130	ra	re	ri	ro	ru
140	sa	se	si	so	su
150	ta	te	ti	to	tu
160	va	ve	vi	vo	vu
170	wa	we	wi	wo	wu
180	xa	xe	xi	xo	xu
190	ya	ye	yi	yo	yu
200	za	ze	zi	zo	zu
230	nga	nge	ngi	ngo	ngu
240	nya	nye	nyi	nyo	nyu
250	sya	sye	syi	syo	syu
260	fra	fre	fri	fro	fru
270	gra	gre	gri	gro	gru
280	kra	kre	kri	kro	kru
290	pra	pre	pri	pro	pru
300	tra	tre	tri	tro	tru
310	ab	eb	ib	ob	ub
330	ad	ed	id	od	ud
340	af	ef	if	of	uf

350	ag	eg	ig	og	ug
360	ah	eh	ih	oh	uh
380	ak	ek	ik	ok	uk
390	al	el	il	ol	ul
400	am	em	im	om	um
410	an	en	in	on	un
420	ap	ep	ip	op	up
440	ar	er	ir	or	ur
450	as	es	is	os	us
460	at	et	it	ot	ut
490	ang	eng	ing	ong	ung
500	a	e	i	o	u

3.4.4 Penguat Audio

Penguat Audio digunakan untuk menguatkan tegangan keluaran dari ISD25120 sehingga suara yang dihasilkan menjadi lebih keras. Komponen utama dari rangkaian penguat audio ini adalah IC Op-amp LM386. Adapun rangkaian dari penguat audio ini dapat ditunjukkan pada gambar 3.6 berikut:



Gambar 3.6 Rangkaian Penguat Audio

Rangkaian diatas merupakan rangkaian aplikasi dari penguat audio dengan menggunakan LM386. Di dalam data sheet LM386 terdapat beberapa aplikasi yang dapat secara langsung kita gunakan sebagai acuan untuk membuat penguat, aplikasi tersebut antara lain penguat dengan penguatan 20 kali, penguat dengan penguatan 50 kali dan lainnya. Pada rangkaian penguat audio yang dirancang kita menggunakan aplikasi dari penguat dengan penguatan 20 kali. Karena beda tegangan keluaran pin SP+ dan SP- pada ISD25120 adalah 2,5 Vpp maka kita dapat menentukan tegangan keluaran yang di hasilkan sebagai berikut :

$$Av = \frac{Vo}{Vi} \tag{3.5}$$

$Vo = 2{,}5 \times 20$

$= 50\ volt$

Dari rangkaian diatas kita juga dapat menentukan frekuensi cut off yang akan dihasilkan oleh penguat audio tersebut sebagai berikut :

$$Fc = \frac{1}{2\pi RC} \tag{3.6}$$

$$Fc = \frac{1}{2x3{,}14x18ohmx10uF}$$

$Fc - 884.6\ Hz$

Karena frekuensi yang dapat di dengar oleh manusia sekitar 20-20 KHz maka penguat audio yang kita rancang dapat digunakan karena frekuensi cut offnya telah memenuhi persyaratan dari suara yang dapat di dengar oleh manusia.

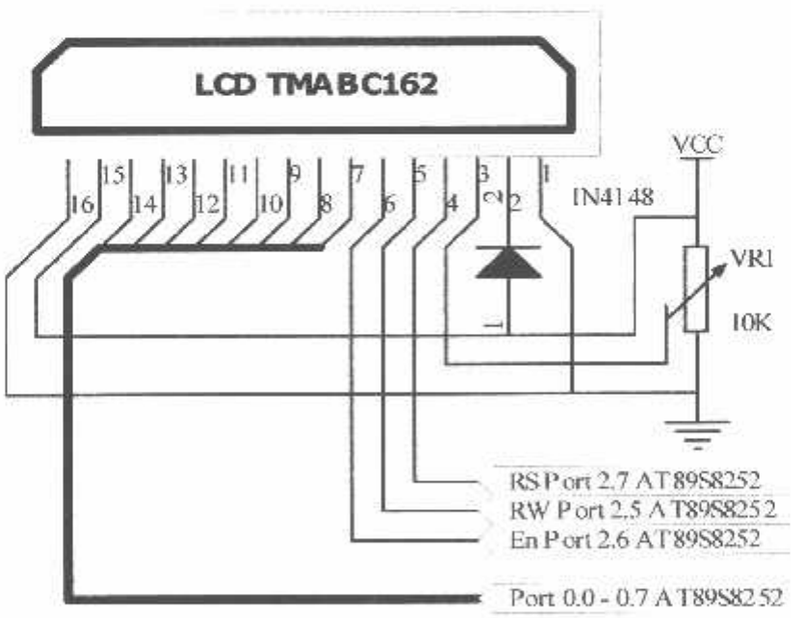
3.4.5 Rangkaian Display LCD

Di dalam antarmuka dengan LCD ada dua proses, yaitu proses penulisan data maupun instruksi. Aturan yang berlaku dalam operasi penulisan LCD dapat dilihat dalam Tabel 3.2

Tabel 3.2 Operasi Penulisan LCD

RS	R/W	Operasi
0	0	Operasi menuliskan instruksi
1	0	Operasi menuliskan data

LCD yang digunakan adalah LCD TMABC162. LCD ini dikontrol oleh mikrokontroler AT89S8252. Adapun gambar rangkaian LCD TMABC162 dapat dilihat pada gambar 3.7 berikut:



Gambar 3.7 Rangkaian LCD

Gambar 3.7 menunjukan anatarmuka LCD dengan mikrokontroller. Pin RS dari LCD terhubung ke port 2.7 pada mikrokontroler, Pin RW dari LCD terhubung ke port 2.5 dan Pin *Enable* dari LCD terhubung ke port 2.6 dari mikrokontroler. Seperti dilihat dalam Tabel 3.2 saat RS = 0 berfungsi untuk menulis instruksi ke LCD dan saat RS = 1 berfungsi untuk menulis data/karakter ke LCD. Alamat untuk menuliskan data/karakter pada LCD 16 karakter X 2 baris dapat dilihat dalam Tabel 3.3

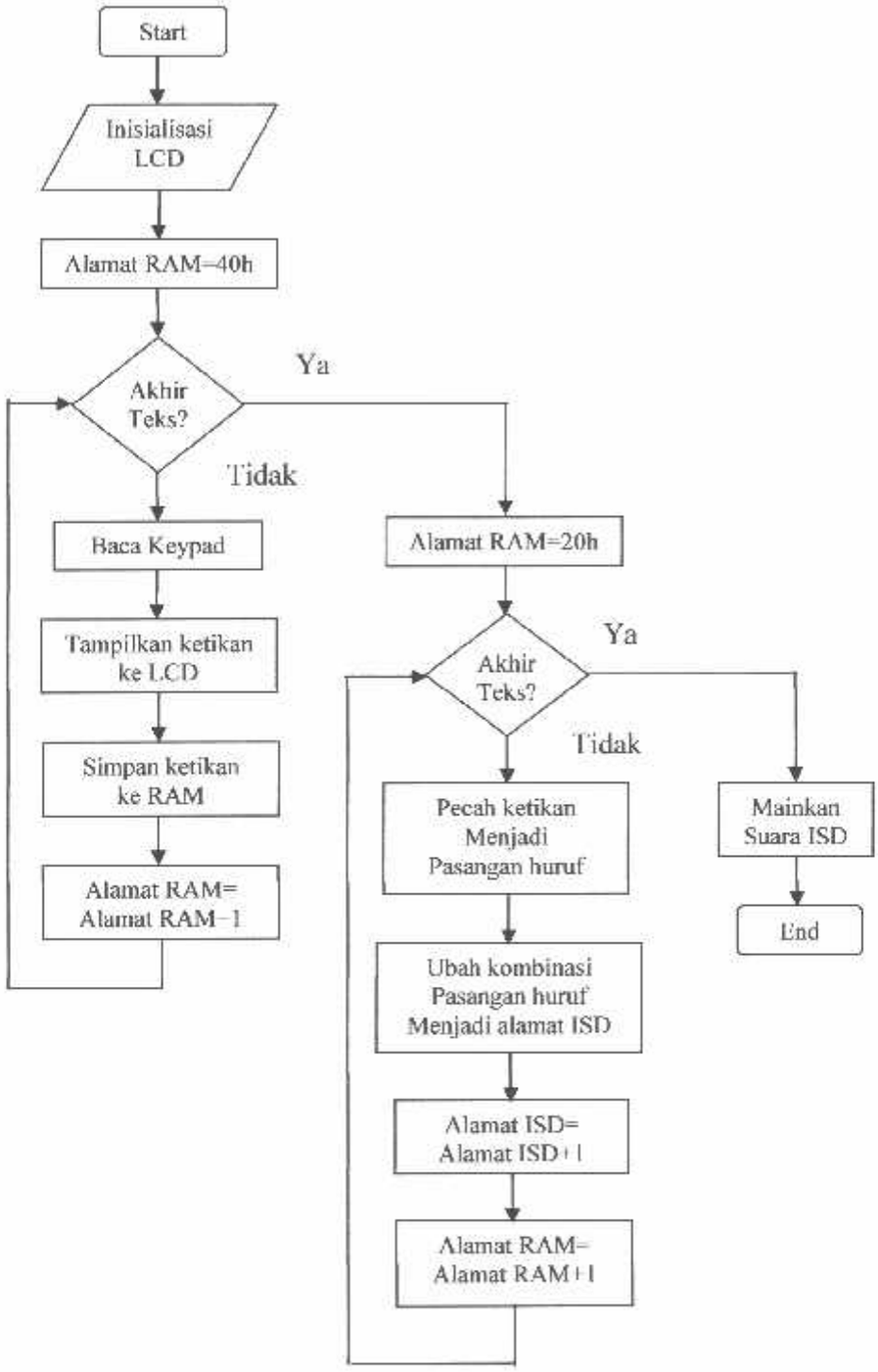
Tabel 3.3 Alamat LCD 16 Karakter X 2 Baris

80h	81h	82h	83h	84h	85h	86h	87h	88h	89h	8Ah	8Bh	8Ch	8Dh	8Eh	8Fh
C0h	C1h	C2h	C3h	C4h	C5h	C6h	C7h	C8h	C9h	CAh	CBh	CCh	CDh	CEh	CFh

3.5 Perencanaan Perangkat Lunak

Perencanaan dari perangkat lunak sistem ini dapat di lihat dari flow chart program pada gambar 3.8 berikut :

Flow Chart Program



Gambar 3.8 Flowchart Program

BAB IV

PENGUJIAN ALAT

Untuk mendapatkan hasil yang maksimal setelah melaksanakan perancangan dan pembuatan alat, maka perlu dilakukan suatu pengujian terhadap alat yang telah kita buat. Pengujian ini bertujuan untuk mengetahui apakah alat yang telah dibuat dapat bekerja sesuai yang dengan perencanaan.

Bagian yang akan di uji dari peralatan ini adalah :

1. Rangkaian LCD
2. Rangkaian *keypad* dan *key encoder*
3. Rangkaian ISD25120
4. Rangkaian keseluruhan sistem

4.1 Pengujian LCD (*Liquid Crystal Display*)

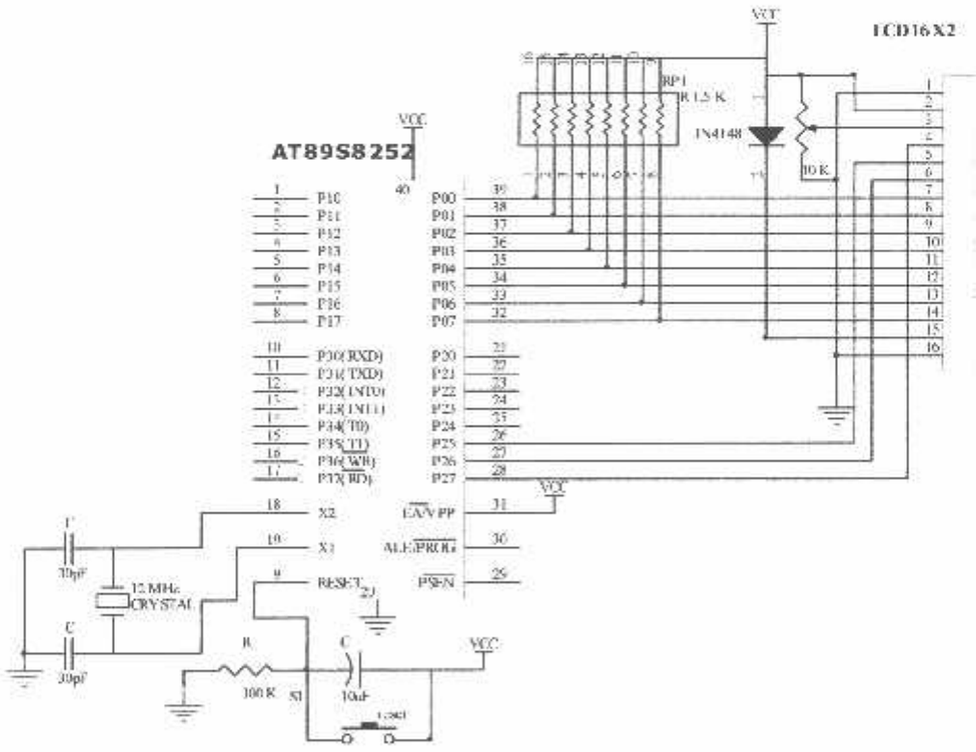
Pengujian terhadap LCD (*Liquid Crystal Display*) dilakukan untuk memeriksa apakah terdapat kesalahan dalam perangkat lunak yang sudah disusun untuk menangani penampil teks dan untuk mengetahui apakah kondisi penampil teks berupa LCD (*Liquid Crystal Display*) sudah bekerja sesuai dengan perancangan. Pengujian dilakukan dengan cara membuat program untuk menampilkan teks ke LCD (*Liquid Crystal Display*).

4.1.1 Peralatan yang digunakan

1. LCD (*Liquid Crystal Display*)
2. Mikrokontroler AT89S8252
3. Perangkat lunak pengujian LCD
4. Downloader mikrokontroler
5. Catu daya

4.1.2 Proses pengujian

1. Membuat perangkat lunak untuk program pengujian LCD, melakukan *compiling* dan menngisikan program ke mikrokontroler AT89S8252.
2. menyusun rangkaia seperti gambar 4.1 berikut :



Gambar 4.1 Rangkaian pengujian LCD

3. Menghidupkan catu daya
4. Mengamati hasil.

4.1.3 Hasil pengujian

Dari hasil pengujian dapat diketahui bahwa rangkaian LCD (*Liquid Crystal Display*) yang dirancang dapat menampilkan teks sesuai dengan yang diinginkan dan dapat bekerja dengan baik.

4.2 Pengujian rangkaian *Keypad* dan *key Encoder*

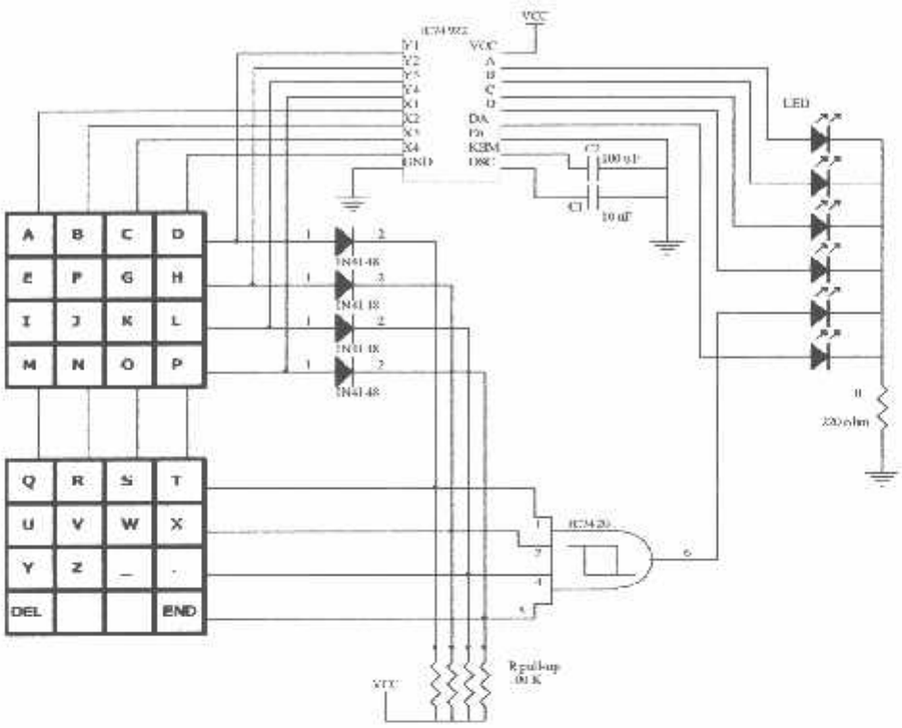
Pengujian terhadap rangkaian *keypad* dan *key encoder* dilakukan untuk mengetahui apakah *keypad dan key encoder* yang dirancang sudah bisa mengeluarkan kondisi logika yang sesuai untuk penekanan masing-masing tombol.

4.2.1 Peralatan yang digunakan

1. Dua buah *keypad* 4x4
2. *Key Encoder* (IC 74922 dan IC7420)
3. 6 buah LED
4. Catu daya

4.2.2Proses pengujian

1. Mengatur rangkaian seperti gambar 4.2 berikut :



Gambar 4.2 Rangkaian Pengujian *keypad* dan *key encoder*

2. Mengaktifkan catu daya
3. Menekan salah satu tombol *keypad*
4. Menguji dan mencatat kondisi logika yang ditampilkan melalui LED (A,B,C,D,E dan DA) pada saat tombol ditekan

4.2.3 Hasil pengujian

Hasil pengujian keypad dan key encoder dapat dilihat pada tabel 4.1 berikut :

Tabel 4.1 Hasil Pengujian *Keypad*

Tombol yang ditekan			**Keluaran**					
Keypad	**Baris**	**Kolom**	**E**	**D**	**C**	**B**	**A**	**DA**
1	1	1	0	0	0	0	0	1
	1	2	0	0	0	0	1	1
	1	3	0	0	0	1	0	1
	1	4	0	0	0	1	1	1
	2	1	0	0	1	0	0	1
	2	2	0	0	1	0	1	1
	2	3	0	0	1	1	0	1
	2	4	0	0	1	1	1	1
	3	1	0	1	0	0	0	1
	3	2	0	1	0	0	1	1
	3	3	0	1	0	1	0	1
	3	4	0	1	0	1	1	1
	4	1	0	1	1	0	0	1
	4	2	0	1	1	0	1	1
	4	3	0	1	1	1	0	1
	4	4	0	1	1	1	1	1
2	1	1	1	0	0	0	0	1
	1	2	1	0	0	0	1	1
	1	3	1	0	0	1	0	1
	1	4	1	0	0	1	1	1
	2	1	1	0	1	0	0	1
	2	2	1	0	1	0	1	1
	2	3	1	0	1	1	0	1
	2	4	1	0	1	1	1	1
	3	1	1	1	0	0	0	1
	3	2	1	1	0	0	1	1
	3	3	1	1	0	1	0	1
	3	4	1	1	0	1	1	1
	4	1	1	1	1	0	0	1
	4	2	1	1	1	0	1	1
	4	3	1	1	1	1	0	1
	4	4	1	1	1	1	1	1

Setiap kali terjadi penekanan tombol maka DA memberikan logika '1'. Jika penekanan tombol dihentikan atau tombol dilepaskan maka DA memberikan logika '0'. Dengan demikian pin DA dapat digunakan sebagai indikator ada tidaknya penekanan tombol *keypad*. Saat salah satu tombol pada *keypad* pertama ditekan maka logika keluaran dari gerbang NAND adalah '0'. Sedangkan penekanan salah satu tombol pada *keypad* kedua mengakibatkan logika keluaran dari gerbang NAND adalah '1'. Tiap-tiap penekanan tombol yang berbeda dihasilkan kondisi keluaran yang berbeda. Contohnya: untuk penekanan tombol pada baris ke-2 kolom ke-3 pada *keypad* ke-1 akan menghasilkan kondisi keluaran 00110. Dengan demikian maka rangkaian *keypad* telah bekerja sesuai dengan perancangan.

4.3 Pengujian ISD25120

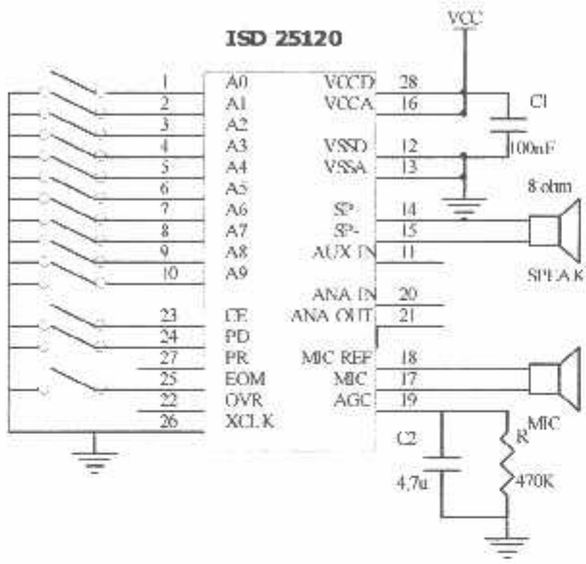
Pengujian terhadap ISD25120 dilakukan untuk memeriksa apakah ISD25120 dapat melakukan perekaman dan memainkan ulang hasil rekaman sesuai dengan perancangan. Pengujian dilakukan dengan cara melakukan perekaman suara dan memainkan ulang hasil rekaman tersebut.

4.3.1 Peralatan yang digunakan

1. ISD25120
2. Modul ISD
3. Catu daya

4.3.2 Proses pengujian

1. Mengatur rangkaian seperti pada gambar berikut :



Gambar 4.3 Rangkaian Pengujian ISD

2. Menghidupkan catu daya
3. Memberi logika 0 pada pin PD, CE dan PR
4. Merekam suara melalui mikrophone
5. Mengamati dan mencatat kondisi EOM pada modul ISD
6. Memberi logika 0 pada pin PD dan CE
7. Mendengarkan hasil rekaman melalui speaker
8. Mengamati dan mencatat kondisi EOM pada modul ISD

4.3.3 Hasil pengujian

Dari pengujian yang dilakukan diperoleh hasil pengujian seperti pada tabel 4.2 berikut :

Tabel 4.2 Hasil Pengujian ISD25120

Alamat	Suara yang di rekam	Hasil rekaman	EOM
00000000	pengujian	pengujian	1
00001010	alat	alat	1
00001110	pengubah	pengubah	1
00010110	teks	teks	1
00011000	suara	suara	1

Dari tabel hasil pengujian dapat dilihat bahwa rangkaian ISD25120 telah dapat bekerja sesuai dengan yang diharapkan pada perancangan. Rangkaian ini dapat melakukan proses perekaman dan pemutaran ulang suara. Tiap-tiap akhir dari proses pemutaran ulang suara maka ditandai dengan adanya sinyal EOM yang memberikan pulsa tinggi.

4.4 Pengujian Keseluruhan Sistem

Untuk mengetahui kinerja sistem secara keseluruhan berdasarkan perancangan yang telah dibuat, maka dilakukan pengujian sistem secara keseluruhan.

4.4.1 Peralatan yang digunakan

1. Rangkaian keseluruhan Mikrokontroler AT89S8252
2. LCD (*Liquid Crystal Display*)
3. Rangkaian *keypad* dan *key encoder*
4. Rangkaian ISD25120
5. Catu daya

4.4.2 Proses pengujian

1. Menggabungkan seluruh rangkaian
2. Menghidupkan catu daya
3. Mengamati dan mencatat hasil keluaran dari speaker

4.4.3 Hasil pengujian

Dari pengujian keseluruhan sistem yang dilakukan dapat diperoleh hasil pengujian seperti pada tabel 4.3 berikut :

Tabel 4.3 Hasil Pengujian Keseluruhan Sistem

NO	Masukan kata	Keluaran yang diharapkan	Keluaran alat	Benar/Salah
1	saya	sa/ya	sa/ya	benar
2	masuk	ma/su/uk	ma/su/uk	benar
3	pramuka	pra/mu/ka	pra/mu/ka	benar
4	april	a/pri/il	a/pri/il	benar
5	belajar	be/la/ja/ar	be/la/ja/ar	benar
6	anggap	ang/ga/ap	a/ang/gi/up	salah
7	krabat	kra/ba/at	kra/ba/at	benar
8	sanyo	sa/nyo	sa/nyo	benar
9	siang	si/ang	si/a/ang	salah
10	sangat	sa/nga/at	sa/nga/at	benar

Dari pengujian keseluruhan system yang dilakukan dapat diketahui bahwa alat yang dibuat dapat mengubah teks menjadi suara. Alat yang dibuat dapat mengubah suku kata yang tersusun atas V,VK,KV,KKV dan KVK menjadi suara dengan . Untuk suku kata yang menggunakan "ng" alat ini tidak dapat mengubah suku kata tersebut menjadi lebih baik karena dalam bahasa indonesia "ng" dianggap sebagai sebuah huruf, tetapi pada alat ini "ng" dianggap sebagai dua huruf yang berdiri sendiri. Dengan demikian maka alat yang dibuat ini dapat mengubah teks menjadi suara sesuai dengan perancangan.

BAB V

PENUTUP

5.1 Kesimpulan

Dari perancangan, pembuatan dan pengujian alat dapat di rumuskan kesimpulan sebagai berikut :

1. Data yang di tampilkan oleh LCD merupakan data yang telah diolah oleh mikrokontroler berdasarkan dari program yang telah di buat.
2. Pada pengujian *keypad* dan *encoder keypad* data dari masing-masing tombol keypad telah sesuai dengan data pada data sheet *key encoder* sehingga mikrokontroler dapat menterjemahkan data dari masing-masing tombol *keypad*.
3. Kejelasan suara yang dihasilkan oleh ISD tergantung bagaimana cara kita merekam ISD tersebut.
4. Alat ini dapat mengubah teks menjadi suara dengan baik apabila suku katanya tersusun atas V, VK, KV, KKV dan KVK tetapi untuk suku kata yang menggunakan "ng" alat ini tidak dapat mengubah suku kata dengan baik.

5.2 Saran-saran

1. Perlu digunakan ISD dengan kapasitas yang lebih besar agar jumlah suara yang dapat ditampung menjadi lebih banyak sehingga suara yang dihasilkan bisa lebih bagus.
2. Pengisian ISD sebaiknya dilakukan ditempat yang tenang karena suara dari luar dapat mempengaruhi hasil dari rekaman ISD tersebut.
3. Perlu digunakan Mikrokontroler dengan kapasitas RAM yang lebih besar agar jumlah kata yang dapat diubah menjadi suara dalam satu kali proses pengubahan menjadi lebih banyak.

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Data sheet ISD 25120. http://www.winbond-usa.com

Data sheet LM 368. http://www.national.com

Data sheet Dioda 1N4148. http://www.datasheetcatalog.com

DAFTAR INDEKS

[1] *Data sheet* Mikrokontroler AT89S8252

[2] *Data sheet* Mikrokontroler AT89S8252

[3] Moh Ibnu Malik,ST "Belajar Mikrokontroler AT89S8252"

[4] *Data sheet* ISD 2500

[5] *Data sheet* ISD 2500

[6] Robert F Coughlin "Penguat Operasional dan Rangkaian Terpadu Linier"

[7] *Manual Book* LCD TM162ABC

[8] *Data sheet Key Encoder* 74C922

[9] *Data sheet Key Encoder* 74C922

[10] *Data sheet Key Encoder* 74C922

[11] *Data sheet Key Encoder* 74C922

INSTITUT TEKNOLOGI NASIONAL
Jl. Raya Karanglo Km 2
MALANG

FORM BIMBINGAN SKRIPSI

Nama : MOHAMMAD ULINNUHA
NIM : 02 17 119
Masa Bimbingan : 30 Juni 2006 s/d 30 Desember 2006
Judul : Alat Pengubah Teks Menjadi Suara Sebagai Alat Bantu Komunikasi Pada Penderita Tuna Wicara Berbasis Mikrokontroler AT89S8252

NO	Tanggal	Uraian	Paraf
1	27/1 2007	Bab 1 - 4	
2	3/3 2007	Demo	
3	5/3 2007	Seminar hasil + Bab IV	
4	15/3 2007	Bab V	
5			
6			
7			
8			
9			
10			

Malang, 200
Dosen Pembimbing

Ir. F. Yudi Limbraptono, MT
NIP : P.1039500274

Form S-4a

INSTITUT TEKNOLOGI NASIONAL
Jl. Raya Karanglo Km 2
MALANG

FORM BIMBINGAN SKRIPSI

Nama : MOHAMMAD ULINNUHA
NIM : 02 17 119
Masa Bimbingan : 30 Juni 2006 s/d 30 Desember 2006
Judul : Alat Pengubah Teks Menjadi Suara Sebagai Alat Bantu Komunikasi Pada Penderita Tuna Wicara Berbasis Mikrokontroler AT89S8252

NO	Tanggal	Uraian	Paraf
1	26-02-07	BAB I : Metodologi penel. - pre. penguat audio	
2		- Gbr. diagram blok - flow chart program	
3		II.	
4	02-03-07	BAB I Acc. - pre penguat Audio.	
5		Acc. materials sumber (cari penguat audio diperbaiki)	
6	14-03-07	Acc. BAB III, IV, V	
7			
8			
9			
10			

Malang, 14-03-2007
Dosen Pembimbing

Irmalia Suryani Faradisa, ST
NIP. Y.1030000365

Form S-4a

INSTITUT TEKNOLOGI NASIONAL
FAKULTAS TEKNOLOGI INDUSTRI
JURUSAN TEKNIK ELEKTRO

Formulir Perbaikan Ujian Skripsi

Dalam pelaksanaan Ujian Skripsi Janjang Strata 1 Jurusan Teknik Elektro Konsentasi T. Energi Listrik / T. Elektronika, maka perlu adanya perbaikan skripsi untuk mahasiswa :

NAMA : Mohammad Ulinuha
NIM : 0217113
Perbaikan meliputi :

1) Print flow chart utk proses searching. Kata. yg cocok → utk keseluruhan address ke LCD.

2)

Malang,

(Koing S. 27,44)

INSTITUT TEKNOLOGI NASIONAL
FAKULTAS TEKNOLOGI INDUSTRI
JURUSAN TEKNIK ELEKTRO

Formulir Perbaikan Ujian Skripsi

Dalam pelaksanaan Ujian Skripsi Janjang Strata 1 Jurusan Teknik Elektro Konsentasi T. Energi Listrik / T. Elektronika, maka perlu adanya perbaikan skripsi untuk mahasiswa :

NAMA : Mohammad Wisnuha
NIM : 0217119
Perbaikan meliputi :

1) Gambar pengaruh arah dan rapatan lempeng dgn hasil nya!
2) Yang menganalisa sebaiknya Inggris?
3) Gambar cara menghitung text / Chapter menjadi word (Gambar rata dekat).

Malang,

(Dr. Sidyo [illegible])

INSTITUT TEKNOLOGI NASIONAL
FAKULTAS TEKNOLOGI INDUSTRI
JURUSAN TEKNIK ELEKTRO S-1
Jl. Karanglo KM. 2 Malang

FORMULIR PERBAIKAN SKRIPSI

Dalam pelaksanaan Ujian Skripsi Jenjang Strata Satu (S-1) Jurusan Teknik Elektro Konsentrasi Teknik Elektronika, maka perlu adanya perbaikan skripsi untuk mahasiswa :

Nama	: Mohammad Ulinnuha
NIM	: 02 17 119
Jurusan	: Teknik Elektro S-1
Konsentrasi	: Teknik Elektronika
Masa Bimbingan	: 30 Juni 2006 s/d 30 Desember 2006
Judul Skripsi	: Alat Pengubah Teks Menjadi Suara Sebagai Alat Bantu Komunikasi Pada Penderita Tuna Wicara Berbasis Mikrokontroler AT89S8252

Tanggal	Uraian	Paraf
23 Maret 2007	Buat Flow Chart untuk proses searching kata yang sesuai untuk alamat ISD	

Diperiksa / Disetujui :

PENGUJI

(I Komang Somawirata, ST. MT)
NIP.P.1030100361

Mengetahui :

Dosen Pembimbing I

(Ir. F. Yudi Limpraptono, MT)
NIP.Y.1039500274

Dosen Pembimbing II

(Irmalia Suryani F. ST)
NIP.P.1030100365

INSTITUT TEKNOLOGI NASIONAL
FAKULTAS TEKNOLOGI INDUSTRI
JURUSAN TEKNIK ELEKTRO S-1
Jl. Karanglo KM. 2 Malang

FORMULIR PERBAIKAN SKRIPSI

Dalam pelaksanaan Ujian Skripsi Jenjang Strata Satu (S-1) Jurusan Teknik Elektro Konsentrasi Teknik Elektronika, maka perlu adanya perbaikan skripsi untuk mahasiswa :

Nama	: Mohammad Ulinnuha
NIM	: 02 17 119
Jurusan	: Teknik Elektro S-1
Konsentrasi	: Teknik Elektronika
Masa Bimbingan	: 30 Juni 2006 s/d 30 Desember 2006
Judul Skripsi	: Alat Pengubah Teks Menjadi Suara Sebagai Alat Bantu Komunikasi Pada Penderita Tuna Wicara Berbasis Mikrokontroler AT89S8252

Tanggal	Uraian	Paraf
23 Maret 2007	Jelaskan pengaruh dioda dalam rangkaian keypad terhadap inputan Y ?	
	Kenapa mengunakan Schimith Trigger ?	
	Jelaskan cara mengikat teks/karakter menjadi suara ?	

Diperiksa / Disetujui :

PENGUJI

(Dr. Cahyo Crysdian,MSc)
NIP

Mengetahui :

Dosen Pembimbing I

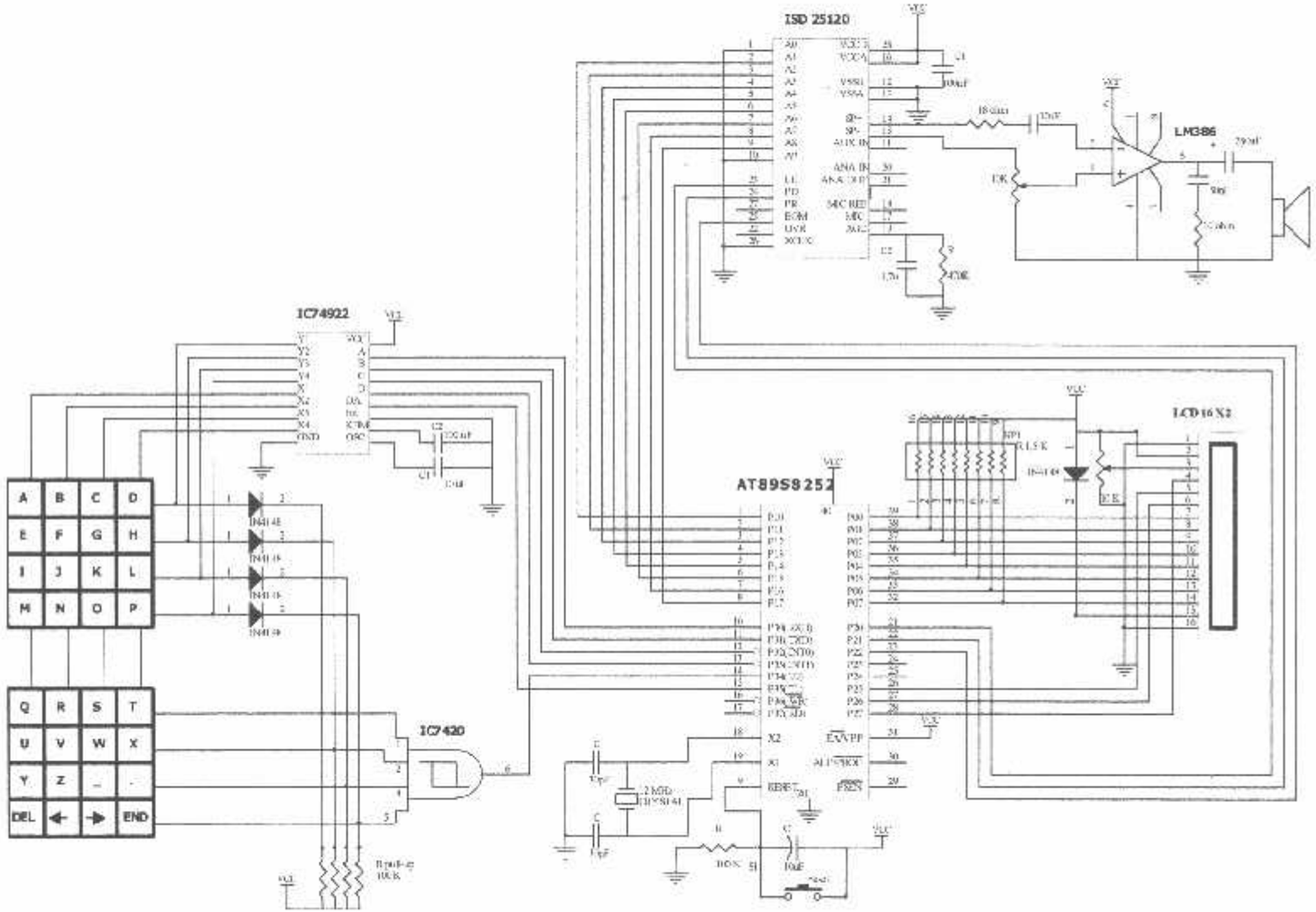
(Ir. F. Yudi Limproptono, MT)
NIP.Y.1039500274

Dosen Pembimbing II

(Irmalia Suryani F. ST)
NIP.P.1030100365

Flow Chart untuk Searching kata ke ISD

1. Pengaruh dioda dalam rangkaian keypad terhadap inputan Y pada IC74922 adalah :
    a. Apabila pada rangkaian tidak terdapat dioda maka untuk scan baris pada inputan Y tidak akan terpengaruh oleh tombol dari keypad kedua (Y pada kondisi 1)
    b. Dipasangnya dioda pada rangkaian keypad sebagai pengkondisi dari dua buah keypad untuk outputan dari IC7420, sehingga apabila tombol pada keypad 1 ditekan maka outputan dari IC7420 tetap berlogika 0. Apabila rangkaian tanpa dioda dan hanya di hubungkan dengan kabel maka apabila tombol pada keypad pertama ada yang ditekan maka outputan dari IC7420 akan berlogika 1.
2. Penggunaan Schimith Trigger disini untuk menentukan outputan dari IC 7420 agar diperoleh sinyal kotak.
3. Cara mengikat teks/karakter menjadi suara adalah :
    a. Mengolah data di RAM untuk menampilkan ke LCD
    Data yang diterima dari keypad berupa data heksa, untuk menampilkan data tersebut ke LCD maka data tersebut diubah ke bentuk huruf.
    b. Mengolah data untuk menetukan vocal atau konsonan
    Data berupa heksa yang diterima diolah dengan menetukan data tersebut termasuk vocal atau konsonan.
    c. Memisahkan data sesuai dengan pasangan vocal atau konsonan
    Setelah data tersebut diketahui karakter vocal dan konsonannya, maka data tersebut akan di pasang-pasangkan sesuai dengan pemisahan data dan juga urutan data yang masuk.
    d. Menentukan suku kata dan alamat ISD
    Setelah susunan suku kata di ketahiu maka data tersebut akan di cocokkan sesuai dengan alamat dari suku kata yang ada di ISD.


ISD 25120
LM386
IC74922
IC7420
AT89S8252
LCD 16 X2
A B C D
E F G H
I J K L
M N O P
Q R S T
U V W X
Y Z _ .
DEL END

```
;$MOD51
        org     00h
;=============================================
;****** MC INITIALISATION ******
;=============================================
enable  bit P2.6
rs      bit P2.7
rw      bit P2.5
EOM     bit p2.2
CE      bit P2.0 ;pulsa
PD      bit P2.1 ;low
Dta     equ 08h
All     equ 09h
Bars    equ 0Ah
Free    equ 0Bh
Mov     sp,#0Ch
;=============================================
;       ! LCD INITIALISATION !
;=============================================
        call    tunda_lcd
        mov     dta,#30h
        call    send_order
        call    tunda_lcd
        mov     dta,#30h
        call    send_order
        call    tunda_lcd
        mov     dta,#30h
        call    send_order
        call    tunda_lcd
        mov     dta,#30h
        call    send_order
        call    tunda_lcd
        mov     dta,#38h
        call    send_order
        call    tunda_lcd
        mov     dta,#08h
        call    send_order
        call    tunda_lcd
        mov     dta,#01h
        call    send_order
        call    tunda_lcd
        mov     dta,#0ch
        call    send_order
        call    tunda_lcd
        mov     dta,#06h
        call    send_order
;=============================================
;***** MAIN PROGRAM *****
;=============================================
start:  mov     bars,#10h
        call    set_baris
        mov     dptr,#txt_string
        call    string
```

```
        mov     bars,#20h
        call    set_baris
        mov     dptr,#txt_string1
        call    string
        mov     free,#0ah
        call    delay_var
        mov     r0,#20h
clear:
        mov     @r0,#15h
        inc     r0
        cjne    r0,#7Fh,clear
        call    tunda_lcd
        mov     dta,#08h
        call    send_order
        call    tunda_lcd
        mov     dta,#01h        ;curcor home
        call    send_order
        call    tunda_lcd
        mov     dta,#0eh
        call    send_order
        mov     r0,#40h
        call    baca_key
        call    tunda_lcd
        mov     dta,#08h
        call    send_order
        call    tunda_lcd
        mov     dta,#01h        ;curcor home
        call    send_order
        call    tunda_lcd
        mov     dta,#0eh
        call    send_order
        call    convert
        call    suara
        jmp     start

txt_string:  db "Teks ke Ucapan '",0
txt_string1: db "Ulinnuha '",0
;=============================
; BACA KEYPAD SIMPAN DI RAM
;=============================
baca_key:
        mov     r1,#40h
        mov     r2,#10h
        mov     bars,#20h
        call    set_baris
baca:
        mov     a,p3
        anl     a,#20h
        cjne    a,#20h,baca
        mov     a,p3
        anl     a,#1fh
        mov     dptr,#angka
        movc    a,@a+dptr
```

```
        cjne    a,#1dh,right
        dec     r0
        dec     r2
        mov     dta,#10h
        call    send_order
        jmp     baca1
right:  cjne    a,#1eh,abjad
        inc     r0
        inc     r2
        mov     dta,#14h
        call    send_order
        jmp     baca1
abjad:
        mov     @r0,a
        mov     r5,a
        mov     dptr,#huruf
        movc    a,@a+dptr
        mov     dta,a
        call    send_ascii
        call    chek_status
        inc     r0
        inc     r2
baca1:
        mov     a,p3
        anl     a,#20h
        cjne    a,#00h,baca1
        cjne    r2,#20h,baca2
        call    move_up
        jmp     baca3
baca2:
        cjne    r2,#0fh,baca3
        call    move_down
baca3:
        mov     a,r5
        cjne    a,#1fh,baca
        nop
        ret

angka:  db
16h,00h,01h,02h,17h,03h,04h,05h,18h,06h,07h,08h,09h,0ah,19h,0bh,0ch,0dh,0eh,0fh,1a
h,10h,11h,12h,13h,14h,15h,1bh,1ch,1dh,1eh,1fh,00h
huruf:  db "bcdfghjklmnpqrstvwxyz aeiou.    '",0
;-------------------------------------------
; Geser Tampilan ke atas atau bawah
;-------------------------------------------
move_down:
        mov     r2,#00h
        mov     bars,#10h
        call    set_baris
        mov     a,r1
        mov     b,#20h
        subb    a,b
        mov     r1,a
```

```
        mov     r3,#2fh
        mov     r4,#1fh
        jmp     move1

move_up:
        mov     r2,#00h
        mov     bars,#10h
        call    set_baris
        mov     r3,#20h
        mov     r4,#10h
move1:
        mov     a,@r1
        mov     dptr,#huruf
        movc    a,@a+dptr
        mov     dta,a
        call    send_ascii
        call    chek_status
        inc     r1
        inc     r2
        cjne    r2,#10h,move1
        mov     bars,#20h
        call    set_baris
move2:
        mov     a,@r1
        mov     dptr,#huruf
        movc    a,@a+dptr
        mov     dta,a
        call    send_ascii
        call    chek_status
        inc     r1
        inc     r2
        cjne    r2,#20h,move2
        mov     a,r3
        mov     bars,a
        call    set_baris
        mov     a,r4
        mov     r2,a
        mov     a,r1
        mov     b,#10h
        subb    a,b
        mov     r1,a
        nop
        nop
        ret
;=============================
; KIRIM SUARA LEWAT ISD
;=============================
suara:  mov     r1,#20h
suara2: mov     a,@r1
        cjne    a,#0f0h,suara3
        mov     free,#07h
        call    delay_var
        jmp     suara4
```

```
suara3: mov     p1,a
        clr     pd
        setb    CE
        clr     CE
        call    tunda_lcd
        setb    CE
        jnb     EOM,$
        setb    pd
        call    tunda_lcd
suara4: inc     r1
        djnz    r7,suara2
        nop
        ret
;=============================
;***** KONVERSI KE SUARA*****
;-----------------------------
convert:
        mov     dptr,#teks
        call    string
        mov     r1,#20h
        mov     r3,#3f11
        mov     r4,#00h
        mov     r5,#00h
        mov     r6,#00h
        mov     r7,#00h
cari:   mov     a,r3
        mov     r0,a
        mov     r2,#00h
cari1:  inc     r0
        inc     r2
        mov     a,r0
        mov     r3,a
        mov     a,@r0
        cjnc    a,#11h,caria
        call    spasi
        mov     @r1,#0F0h
        jmp     end_convert
caria:  cjne    a,#1bh,cari2
        call    spasi
        mov     @r1,#0F0h
        inc     r1
        inc     r7
        jmp     cari
cari2:  cjne    a,#15h,cari3
        call    spasi
        mov     @r1,#0F0h
        inc     r1
        inc     r7
        jmp     cari
cari3:  jc      cari1
        cjne    r2,#01h,dua
        call    vok
        jmp     cari
```

```
dua:    cjne    r2,#02h,tiga
        dec     r0
        call    KV
        jmp     cari
tiga:   cjne    r2,#03h,empat
        dec     r0
        dec     r0
        jmp     kecual
biasa:  dec     r0
        dec     r0
        dec     r0
        mov     a,@r0
        cjne    a,#15h,langsung
        dec     r1
        dec     r7
langsung:
        inc     r0
        call    vk
        call    kV
        jmp     cari

empat:  dec     r0
        dec     r0
        dec     r0
        dec     r0
        call    vk
        jmp     ang
kecual: mov     a,@r0
        cjne    a,#0ah,rsisip
        inc     r0
        mov     a,@r0
        dec     r0
        cjne    a,#04h,ny
        mov     r5,#5dh
        jmp     kon3
ny:     mov     r5,#62h
        jmp     kon3
ang:    mov     a,@r0
        cjne    a,#04,rsisip
        mov     r5,#0dfh
        dec     r0
        dec     r0
        mov     a,@r0
        mov     b,r5
        add     a,b
        dec     r1
        dec     r7
        mov     @r1,a
        inc     r1
        inc     r7
        inc     r0
        call    kv
        jmp     cari
```

```
rsisip:  inc   r0
         mov   a,@r0
         cjne  a,#0dh,biasa
         dec   r0
         mov   a,@r0
         cjne  a,#03h,gr
         mov   r5,#6ch
         jmp   kon3
gr:      cjne  a,#04h,kr
         mov   r5,#71h
         jmp   kon3
kr:      cjne  a,#07h,pr
         mov   r5,#76h
         jmp   kon3
pr:      cjne  a,#0bh,tr
         mov   r5,#7bh
         jmp   kon3
tr:      mov   r5,#80h
kon3:    inc   r0
         inc   r0
         mov   a,@r0
         mov   b,r5
         add   a,b
         mov   @r1,a
         inc   r1
         inc   r7
         jmp   cari

spasi:   cjne  r2,#01h,sdua
         nop
         ret
sdua:    cjne  r2,#02,stiga
         dec   r0
         dec   r0
         jmp   vk
stiga:   dec   r0
         dec   r0
         dec   r0
         mov   a,@r0
         mov   r4,a
         mov   a,#00h
         mov   r5,#0DFh
         inc   r0
         inc   r0
         inc   r0
         jmp   gab
Vok:     mov   a,@r0
         mov   r4,a
         mov   a,#00h
         mov   r5,#0E4h
         jmp   gab
KV:      mov   a,@r0
         mov   r6,a
```

```
        inc     r0
        mov     a,@r0
        mov     r4,a
        mov     a,r6
        mov     r5,#0EAh
        jmp     gab
VK:     mov     a,@r0
        mov     r4,a
        inc     r0
        mov     a,@r0
        mov     r5,#85h
        inc     r0
gab:    mov     b,#05h
        mul     ab
        mov     b,r4
        add     a,b
        mov     b,r5
        add     a,b
        mov     @r1,a
        inc     r1
        inc     r7
        ret
end_convert:
        nop
        ret
teks:   db "ubah ke suara  ",0
;=============================
;****** LCD ROUTINE ******
;=============================
send_order:
        clr     rs
        jmp     dataout

send_ascii:
        setb    rs
dataout:
        clr     rw
        mov     p0,dta
        setb    enable
        nop
        nop
        nop
        clr     enable
        ret
chek_status:
        acall   status
        anl     a,#80h
        cjne    a,#00h,chek_status
        ret
status:
        clr     rs
        jmp     datain
```

```
chek_ascii:
        setb    rs
datain:
        setb    rw
        setb    enable
        mov     a,p0
        nop
        nop
        nop
        clr     enable
        ret
;-----------------------------------------------
;>>>>>>>>> STRING <<<<<<<<<
;-----------------------------------------------
string:
        mov     a,#00h
        movc    a,@a+dptr
        cjne    a,#"",tulis
        ret
tulis:
        inc     dptr
        mov     dta,a
        call    send_ascii
        call    chek_status
        jmp     string
;-----------------------------------------------
;               ! SEND ORDER !
;-----------------------------------------------
order:
        mov     dta,all
        call    send_order
        call    chek_status
        ret
;-----------------------------------------------
;               ! ROW SET !
;-----------------------------------------------
set_baris:
        mov     a,bars
        anl     a,#30h
        cjne    a,#20h,baris1
        mov     a,bars
        anl     a,#0fh
        mov     all,#0c0h
        orl     all,a
        call    order
        ret
baris1: mov     a,bars
        anl     a,#0fh
        mov     all,#80h
        orl     all,a
        call    order
        ret
```

```
;=============================
;              ! DELAY ROUTINE !
;=============================
        mov     free,#05d
        setb    tr1
lgi:    mov     th1,#3ch
        mov     tl1,#0afh
ulng:   jbc     tf1,hitng
        sjmp    ulng
hitng:  djnz    free,lgi
        clr     tr1
        ret
tunda_lcd:
        mov     tmod,#10h
;---------------------------------------------
;              ! VARIABEL DELAY !
;---------------------------------------------
;register variable using free
;tmod = (ffffh-3cafh) * 10e-6 =0.05 s
;setiap 1 hitungan = 50 ms
delay_var:
        mov     tmod,#10h
        setb    tr1
lagi2:  mov     th1,#3ch
        mov     tl1,#0afh
ulang2:
        jbc     tf1,hitung2
        sjmp    ulang2
hitung2:
        djnz    free,lagi2
        clr     tr1
        ret

akhir:  sjmp    $
        nop
        end
```

atures

ompatible with MCS®51 Products
(Bytes of In-System Reprogrammable Downloadable Flash Memory
– SPI Serial Interface for Program Downloading
– Endurance: 1,000 Write/Erase Cycles
(Bytes EEPROM
– Endurance: 100,000 Write/Erase Cycles
/ to 6V Operating Range
ılly Static Operation: 0 Hz to 24 MHz
ıree-level Program Memory Lock
i6 x 8-bit Internal RAM
! Programmable I/O Lines
ıree 16-bit Timer/Counters
ine Interrupt Sources
ɔgrammable UART Serial Channel
PI Serial Interface
ɔw-power Idle and Power-down Modes
terrupt Recovery from Power-down
ɔgrammable Watchdog Timer
ual Data Pointer
ɔwer-off Flag

scription

AT89S8252 is a low-power, high-performance CMOS 8-bit microcontroller with 8K ıs of downloadable Flash programmable and erasable read-only memory and 2K s of EEPROM. The device is manufactured using Atmel's high-density nonvolatile nory technology and is compatible with the industry-standard 80C51 instruction and pinout. The on-chip downloadable Flash allows the program memory to be ɔgrammed In-System through an SPI serial interface or by a conventional nonvol- memory programmer. By combining a versatile 8-bit CPU with downloadable ;h on a monolithic chip, the Atmel AT89S8252 is a powerful microcontroller, which ɔvides a highly-flexible and cost-effective solution to many embedded control lications.

AT89S8252 provides the following standard features: 8K bytes of downloadable ;h, 2K bytes of EEPROM, 256 bytes of RAM, 32 I/O lines, programmable watchdog ɔr, two data pointers, three 16-bit timer/counters, a six-vector two-level interrupt ıitecture, a full duplex serial port, on-chip oscillator, and clock circuitry. In addition, AT89S8252 is designed with static logic for operation down to zero frequency and ports two software selectable power saving modes. The Idle Mode stops the CPU le allowing the RAM, timer/counters, serial port, and interrupt system to continue ctioning. The Power-down mode saves the RAM contents but freezes the oscillator, ıbling all other chip functions until the next external interrupt or hardware reset.

downloadable Flash can be changed a single byte at a time and is accessible ugh the SPI serial interface. Holding RESET active forces the SPI bus into a serial ɡramming interface and allows the program memory to be written to or read from ɜss lock bits have been activated.

ATMEL®

8-bit Microcontroller with 8K Bytes Flash

AT89S8252

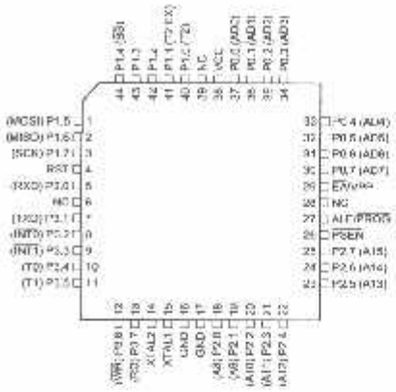
0401F–MICRO–11/03

ATMEL

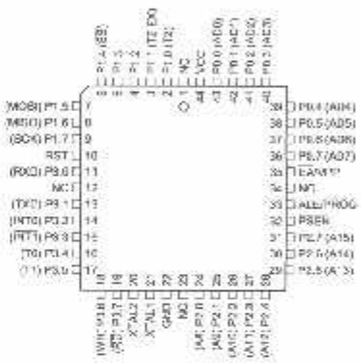
ı Configurations

PDIP

TQFP



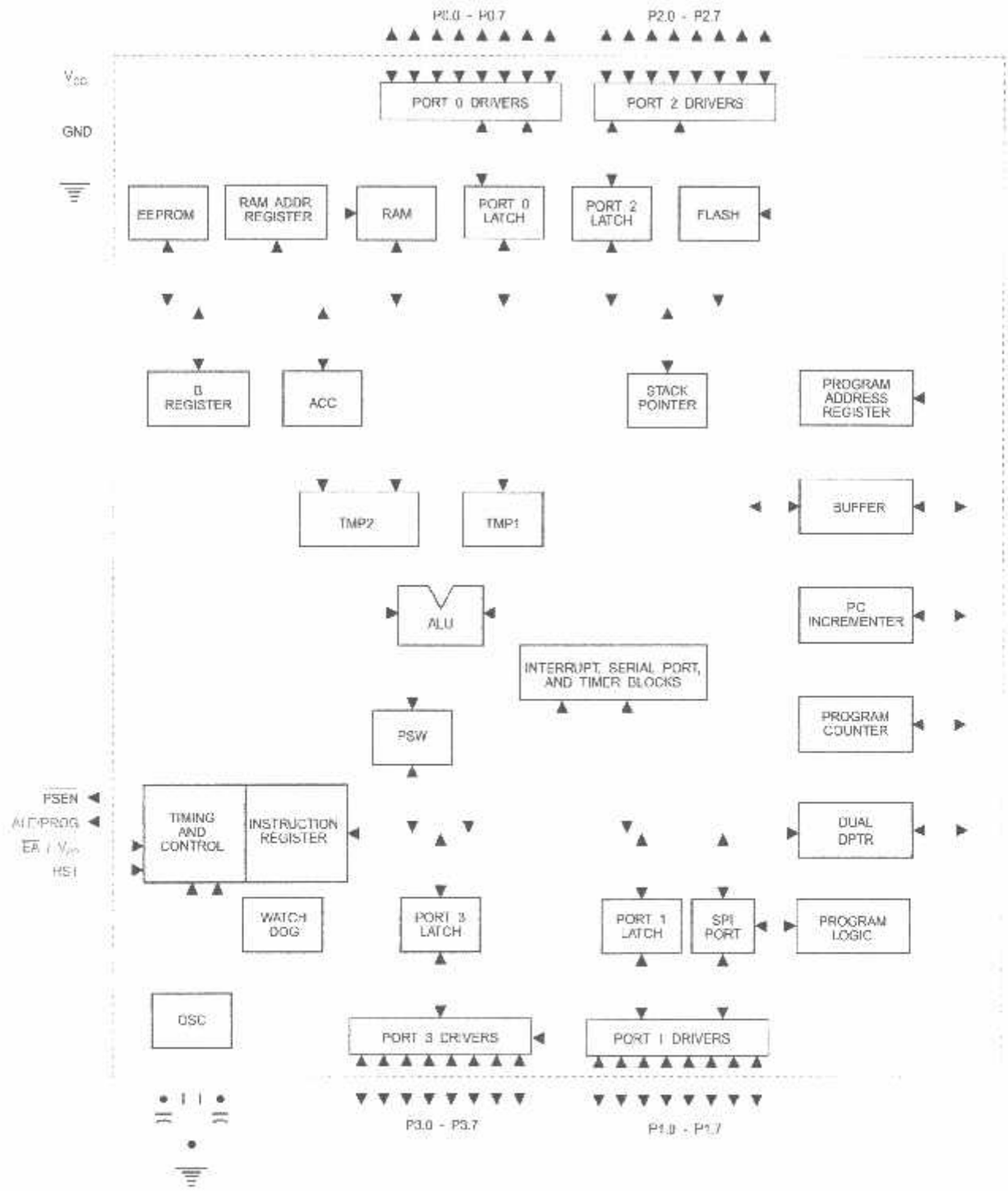
PLCC



ı Description

ɔ	Supply voltage.
ɒ	Ground.
t 0	Port 0 is an 8-bit open drain bi-didirectional I/O port. As an output port, each pin can sink eight TTL inputs. When 1s are written to port 0 pins, the pins can be used as high-impedance inputs. Port 0 can also be configured to be the multiplexed low-order address/data bus during accesses to external program and data memory. In this mode, P0 has internal pull-ups. Port 0 also receives the code bytes during Flash programming and outputs the code bytes during program verification. External pull-ups are required during program verification.
rt 1	Port 1 is an 8-bit bi-directional I/O port with internal pull-ups. The Port 1 output buffers can sink/source four TTL inputs. When 1s are written to Port 1 pins, they are pulled high by the internal pull-ups and can be used as inputs. As inputs, Port 1 pins that are externally being pulled low will source current (I_{IL}) because of the internal pull-ups.

ock Diagram


P0.0 - P0.7
P2.0 - P2.7
VCC
GND
PORT 0 DRIVERS
PORT 2 DRIVERS
EEPROM
RAM ADDR. REGISTER
RAM
PORT 0 LATCH
PORT 2 LATCH
FLASH
B REGISTER
ACC
STACK POINTER
PROGRAM ADDRESS REGISTER
TMP2
TMP1
BUFFER
ALU
PC INCREMENTER
INTERRUPT, SERIAL PORT, AND TIMER BLOCKS
PSW
PROGRAM COUNTER
PSEN
ALE/PROG
EA / VPP
RST
TIMING AND CONTROL
INSTRUCTION REGISTER
DUAL DPTR
WATCH DOG
PORT 3 LATCH
PORT 1 LATCH
SPI PORT
PROGRAM LOGIC
OSC
PORT 3 DRIVERS
PORT 1 DRIVERS
P3.0 - P3.7
P1.0 - P1.7

Some Port 1 pins provide additional functions. P1.0 and P1.1 can be configured to be the timer/counter 2 external count input (P1.0/T2) and the timer/counter 2 trigger input (P1.1/T2EX), respectively.

Furthermore, P1.4, P1.5, P1.6, and P1.7 can be configured as the SPI slave port select, data input/output and shift clock input/output pins as shown in the following table.

Port Pin	Alternate Functions
P1.0	T2 (external count input to Timer/Counter 2), clock-out
P1.1	T2EX (Timer/Counter 2 capture/reload trigger and direction control)
P1.4	$\overline{SS}$ (Slave port select input)
P1.5	MOSI (Master data output, slave data input pin for SPI channel)
P1.6	MISO (Master data input, slave data output pin for SPI channel)
P1.7	SCK (Master clock output, slave clock input pin for SPI channel)

Port 1 also receives the low-order address bytes during Flash programming and verification.

rt 2

Port 2 is an 8-bit bi-directional I/O port with internal pull-ups. The Port 2 output buffers can sink/source four TTL inputs. When 1s are written to Port 2 pins, they are pulled high by the internal pull-ups and can be used as inputs. As inputs, Port 2 pins that are externally being pulled low will source current (I_{IL}) because of the internal pull-ups.

Port 2 emits the high-order address byte during fetches from external program memory and during accesses to external data memory that use 16-bit addresses (MOVX @ DPTR). In this application, Port 2 uses strong internal pull-ups when emitting 1s. During accesses to external data memory that use 8-bit addresses (MOVX @ RI), Port 2 emits the contents of the P2 Special Function Register.

Port 2 also receives the high-order address bits and some control signals during Flash programming and verification.

rt 3

Port 3 is an 8-bit bi-directional I/O port with internal pull-ups. The Port 3 output buffers can sink/source four TTL inputs. When 1s are written to Port 3 pins, they are pulled high by the internal pull-ups and can be used as inputs. As inputs, Port 3 pins that are externally being pulled low will source current (I_{IL}) because of the pull-ups.

Port 3 receives some control signals for Flash programming and verification.

Port 3 also serves the functions of various special features of the AT89S8252, as shown in the following table.

Port Pin	Alternate Functions
P3.0	RXD (serial input port)
P3.1	TXD (serial output port)
P3.2	$\overline{INT0}$ (external interrupt 0)
P3.3	$\overline{INT1}$ (external interrupt 1)
P3.4	T0 (timer 0 external input)
P3.5	T1 (timer 1 external input)
P3.6	$\overline{WR}$ (external data memory write strobe)
P3.7	$\overline{RD}$ (external data memory read strobe)

T

Reset input. A high on this pin for two machine cycles while the oscillator is running resets the device.

E/$\overline{PROG}$

Address Latch Enable is an output pulse for latching the low byte of the address during accesses to external memory. This pin is also the program pulse input ($\overline{PROG}$) during Flash programming.

In normal operation, ALE is emitted at a constant rate of 1/6 the oscillator frequency and may be used for external timing or clocking purposes. Note, however, that one ALE pulse is skipped during each access to external data memory.

If desired, ALE operation can be disabled by setting bit 0 of SFR location 8EH. With the bit set, ALE is active only during a MOVX or MOVC instruction. Otherwise, the pin is weakly pulled high. Setting the ALE-disable bit has no effect if the microcontroller is in external execution mode.

$\overline{EN}$

Program Store Enable is the read strobe to external program memory.

When the AT89S8252 is executing code from external program memory, $\overline{PSEN}$ is activated twice each machine cycle, except that two $\overline{PSEN}$ activations are skipped during each access to external data memory.

/VPP

External Access Enable. $\overline{EA}$ must be strapped to GND in order to enable the device to fetch code from external program memory locations starting at 0000H up to FFFFH. Note, however, that if lock bit 1 is programmed, EA will be internally latched on reset.

$\overline{EA}$ should be strapped to V_{CC} for internal program executions. This pin also receives the 12-volt programming enable voltage (V_{PP}) during Flash programming when 12-volt programming is selected.

AL1

Input to the inverting oscillator amplifier and input to the internal clock operating circuit.

AL2

Output from the inverting oscillator amplifier.

ecial Function gisters

A map of the on-chip memory area called the Special Function Register (SFR) space is shown in Table 1.

Note that not all of the addresses are occupied, and unoccupied addresses may not be implemented on the chip. Read accesses to these addresses will in general return random data, and write accesses will have an indeterminate effect.

User software should not write 1s to these unlisted locations, since they may be used in future products to invoke new features. In that case, the reset or inactive values of the new bits will always be 0.

Timer 2 Registers Control and status bits are contained in registers T2CON (shown in Table 2) and T2MOD (shown in Table 9) for Timer 2. The register pair (RCAP2H, RCAP2L) are the Capture/Reload registers for Timer 2 in 16-bit capture mode or 16-bit auto-reload mode.

le 1. AT89S8252 SFR Map and Reset Values

F8H								0FFH
F0H	B 00000000							0F7H
E8H								0EFH
E0H	ACC 00000000							0E7H
D8H								0DF H
D0H	PSW 00000000					SPCR 000001XX		0D7H
C8H	T2CON 00000000	T2MOD XXXXXX00	RCAP2L 00000000	RCAP2H 00000000	TL2 00000000	TH2 00000000		0CF H
C0H								0C7H
B8H	IP XX000000							0BFH
B0H	P3 11111111							0B7H
A8H	IE 0X000000		SPSR 00XXXXXX					0AFH
A0H	P2 11111111							0A7H
98H	SCON 00000000	SBUF XXXXXXXX						9FH
90H	P1 11111111						WMCON 00000010	97H
88H	TCON 00000000	TMOD 00000000	TL0 00000000	TL1 00000000	TH0 00000000	TH1 00000000		8FH
80H	P0 11111111	SP 00000111	DP0L 00000000	DP0H 00000000	DP1L 00000000	DP1H 00000000	SPDR XXXXXXXX	PCON 0XXX0000 87H

le 2. T2CON – Timer/Counter 2 Control Register

CON Address = 0C8H — Reset Value = 0000 0000B

Addressable

TF2	EXF2	RCLK	TCLK	EXEN2	TR2	C/$\overline{T2}$	CP/$\overline{RL2}$
7	6	5	4	3	2	1	0

mbol	Function
2	Timer 2 overflow flag set by a Timer 2 overflow and must be cleared by software. TF2 will not be set when either RCLK = 1 or TCLK = 1.
F2	Timer 2 external flag set when either a capture or reload is caused by a negative transition on T2EX and EXEN2 = 1. When Timer 2 interrupt is enabled, EXF2 = 1 will cause the CPU to vector to the Timer 2 interrupt routine. EXF2 must be cleared by software. EXF2 does not cause an interrupt in up/down counter mode (DCEN = 1).
CLK	Receive clock enable. When set, causes the serial port to use Timer 2 overflow pulses for its receive clock in serial port Modes 1 and 3. RCLK = 0 causes Timer 1 overflows to be used for the receive clock.
CLK	Transmit clock enable. When set, causes the serial port to use Timer 2 overflow pulses for its transmit clock in serial port Modes 1 and 3. TCLK = 0 causes Timer 1 overflows to be used for the transmit clock.
EN2	Timer 2 external enable. When set, allows a capture or reload to occur as a result of a negative transition on T2EX if Timer 2 is not being used to clock the serial port. EXEN2 = 0 causes Timer 2 to ignore events at T2EX.
2	Start/Stop control for Timer 2. TR2 = 1 starts the timer.
$\overline{T2}$	Timer or counter select for Timer 2. C/$\overline{T2}$ = 0 for timer function. C/$\overline{T2}$ = 1 for external event counter (falling edge triggered).
/$\overline{RL2}$	Capture/Reload select. CP/$\overline{RL2}$ = 1 causes captures to occur on negative transitions at T2EX if EXEN2 = 1. CP/$\overline{RL2}$ = 0 causes automatic reloads to occur when Timer 2 overflows or negative transitions occur at T2EX when EXEN2 = 1. When either RCLK or TCLK = 1, this bit is ignored and the timer is forced to auto-reload on Timer 2 overflow.

chdog and Memory Control Register The WMCON register contains control bits for the Watchdog Timer (shown in le 3). The EEMEN and EEMWE bits are used to select the 2K bytes on-chip EEPROM, and to enable byte-write. The 3 bit selects one of two DPTR registers available.

le 3. WMCON—Watchdog and Memory Control Register

MCON Address = 96H — Reset Value = 0000 0010B

PS2	PS1	PS0	EEMWE	EEMEN	DPS	WDTRST	WDTEN
7	6	5	4	3	2	1	0

mbol	Function
2 1 0	Prescaler Bits for the Watchdog Timer. When all three bits are set to "0", the watchdog timer has a nominal period of 16 ms. When all three bits are set to "1", the nominal period is 2048 ms.
MWE	EEPROM Data Memory Write Enable Bit. Set this bit to "1" before initiating byte write to on-chip EEPROM with the MOVX instruction. User software should set this bit to "0" after EEPROM write is completed.
MEN	Internal EEPROM Access Enable. When EEMEN = 1, the MOVX instruction with DPTR will access on-chip EEPROM instead of external data memory. When EEMEN = 0, MOVX with DPTR accesses external data memory.
S	Data Pointer Register Select. DPS = 0 selects the first bank of Data Pointer Register, DP0, and DPS = 1 selects the second bank, DP1
TRST Y/$\overline{\text{BSY}}$	Watchdog Timer Reset and EEPROM Ready/$\overline{\text{Busy}}$ Flag. Each time this bit is set to "1" by user software, a pulse is generated to reset the watchdog timer. The WDTRST bit is then automatically reset to "0" in the next instruction cycle. The WDTRST bit is Write-Only. This bit also serves as the RDY/$\overline{\text{BSY}}$ flag in a Read-Only mode during EEPROM write. RDY/$\overline{\text{BSY}}$ = 1 means that the EEPROM is ready to be programmed. While programming operations are being executed, the RDY/$\overline{\text{BSY}}$ bit equals "0" and is automatically reset to "1" when programming is completed.
TEN	Watchdog Timer Enable Bit. WDTEN = 1 enables the watchdog timer and WDTEN = 0 disables the watchdog timer.

SPI Registers Control and status bits for the Serial Peripheral Interface are contained in registers SPCR (shown in Table 4) and SPSR (shown in Table 5). The SPI data bits are contained in the SPDR register. Writing the SPI data register during serial data transfer sets the Write Collision bit, WCOL, in the SPSR register. The SPDR is double buffered for writing and the values in SPDR are not changed by Reset.

Interrupt Registers The global interrupt enable bit and the individual interrupt enable bits are in the IE register. In addition, the individual interrupt enable bit for the SPI is in the SPCR register. Two priorities can be set for each of the six interrupt sources in the IP register.

Dual Data Pointer Registers To facilitate accessing both internal EEPROM and external data memory, two banks of 16-bit Data Pointer Registers are provided: DP0 at SFR address locations 82H-83H and DP1 at 84H-85H. Bit DPS = 0 in SFR WMCON selects DP0 and DPS = 1 selects DP1. The user should **ALWAYS** initialize the DPS bit to the appropriate value before accessing the respective Data Pointer Register.

Power Off Flag The Power Off Flag (POF) is located at bit_4 (PCON.4) in the PCON SFR. POF is set to "1" during power up. It can be set and reset under software control and is not affected by RESET.

le 4. SPCR – SPI Control Register

CR Address = D5H — Reset Value = 0000 01XXB

	SPIE	SPE	DORD	MSTR	CPOL	CPHA	SPR1	SPR0
it	7	6	5	4	3	2	1	0

mbol	Function
IE	SPI Interrupt Enable. This bit, in conjunction with the ES bit in the IE register, enables SPI interrupts: SPIE = 1 and ES = 1 enable SPI interrupts. SPIE = 0 disables SPI interrupts.
E	SPI Enable. SPI = 1 enables the SPI channel and connects $\overline{SS}$, MOSI, MISO and SCK to pins P1.4, P1.5, P1.6, and P1.7. SPI = 0 disables the SPI channel.
ORD	Data Order. DORD = 1 selects LSB first data transmission. DORD = 0 selects MSB first data transmission.
STR	Master/Slave Select. MSTR = 1 selects Master SPI mode. MSTR = 0 selects Slave SPI mode.
OL	Clock Polarity. When CPOL = 1, SCK is high when idle. When CPOL = 0, SCK of the master device is low when not transmitting. Please refer to figure on SPI Clock Phase and Polarity Control.
PHA	Clock Phase. The CPHA bit together with the CPOL bit controls the clock and data relationship between master and slave. Please refer to figure on SPI Clock Phase and Polarity Control.
PR0 PR1	SPI Clock Rate Select. These two bits control the SCK rate of the device configured as master. SPR1 and SPR0 have no effect on the slave. The relationship between SCK and the oscillator frequency, F_{osc}, is as follows: SPR1 SPR0 SCK = F_{osc} divided by 0 0 4 0 1 16 1 0 64 1 1 128

le 5. SPSR – SPI Status Register

'SR Address = AAH — Reset Value = 00XX XXXXB

	SPIF	WCOL	–	–	–	–	–	–
;it	7	6	5	4	3	2	1	0

'mbol	Function
'IF	SPI Interrupt Flag. When a serial transfer is complete, the SPIF bit is set and an interrupt is generated if SPIE = 1 and ES = 1. The SPIF bit is cleared by reading the SPI status register with SPIF and WCOL bits set, and then reading/writing the SPI data register.
COL	Write Collision Flag. The WCOL bit is set if the SPI data register is written during a data transfer. During data transfer, the result of reading the SPDR register may be incorrect, and writing to it has no effect. The WCOL bit (and the SPIF bit) are cleared by reading the SPI status register with SPIF and WCOL set, and then accessing the SPI data register.

le 6. SPDR – SPI Data Register

'DR Address = 86H — Reset Value = unchanged

	SPD7	SPD6	SPD5	SPD4	SPD3	SPD2	SPD1	SPD0
;it	7	6	5	4	3	2	1	0

ta Memory – EPROM and RAM

The AT89S8252 implements 2K bytes of on-chip EEPROM for data storage and 256 bytes of RAM. The upper 128 bytes of RAM occupy a parallel space to the Special Function Registers. That means the upper 128 bytes have the same addresses as the SFR space but are physically separate from SFR space.

When an instruction accesses an internal location above address 7FH, the address mode used in the instruction specifies whether the CPU accesses the upper 128 bytes of RAM or the SFR space. Instructions that use direct addressing access SFR space.

For example, the following direct addressing instruction accesses the SFR at location 0A0H (which is P2).

```
MOV 0A0H, #data
```

Instructions that use indirect addressing access the upper 128 bytes of RAM. For example, the following indirect addressing instruction, where R0 contains 0A0H, accesses the data byte at address 0A0H, rather than P2 (whose address is 0A0H).

```
MOV @R0, #data
```

Note that stack operations are examples of indirect addressing, so the upper 128 bytes of data RAM are available as stack space.

The on-chip EEPROM data memory is selected by setting the EEMEN bit in the WMCON register at SFR address location 96H. The EEPROM address range is from 000H to 7FFH. The MOVX instructions are used to access the EEPROM. To access off-chip data memory with the MOVX instructions, the EEMEN bit needs to be set to "0".

The EEMWE bit in the WMCON register needs to be set to "1" before any byte location in the EEPROM can be written. User software should reset EEMWE bit to "0" if no further EEPROM write is required. EEPROM write cycles in the serial programming mode are self-timed and typically take 2.5 ms. The progress of EEPROM write can be monitored by reading the RDY/$\overline{BSY}$ bit (read-only) in SFR WMCON. RDY/$\overline{BSY}$ = 0 means

programming is still in progress and RDY/$\overline{BSY}$ = 1 means EEPROM write cycle is completed and another write cycle can be initiated.

In addition, during EEPROM programming, an attempted read from the EEPROM will fetch the byte being written with the MSB complemented. Once the write cycle is completed, true data are valid at all bit locations.

ogrammable atchdog Timer

The programmable Watchdog Timer (WDT) operates from an independent internal oscillator. The prescaler bits, PS0, PS1 and PS2 in SFR WMCON are used to set the period of the Watchdog Timer from 16 ms to 2048 ms. The available timer periods are shown in the following table and the actual timer periods (at V_{CC} = 5V) are within ±30% of the nominal.

The WDT is disabled by Power-on Reset and during Power-down. It is enabled by setting the WDTEN bit in SFR WMCON (address = 96H). The WDT is reset by setting the WDTRST bit in WMCON. When the WDT times out without being reset or disabled, an internal RST pulse is generated to reset the CPU.

Table 7. Watchdog Timer Period Selection

WDT Prescaler Bits			
PS2	PS1	PS0	Period (nominal)
0	0	0	16 ms
0	0	1	32 ms
0	1	0	64 ms
0	1	1	128 ms
1	0	0	256 ms
1	0	1	512 ms
1	1	0	1024 ms
1	1	1	2048 ms

ner 0 and 1

Timer 0 and Timer 1 in the AT89S8252 operate the same way as Timer 0 and Timer 1 in the AT89C51 and AT89C52. For further information on the timers' operation, refer to the Atmel web site (http://www.atmel.com). From the home page, select "Products", then "Microcontrollers, then "8051-Architecture". Click on "Documentation", then on "Other Documents". Open the document "AT89 Series Hardware Description".

ner 2

Timer 2 is a 16-bit Timer/Counter that can operate as either a timer or an event counter. The type of operation is selected by bit C/$\overline{T2}$ in the SFR T2CON (shown in Table 2). Timer 2 has three operating modes: capture, auto-reload (up or down counting), and baud rate generator. The modes are selected by bits in T2CON, as shown in Table 8.

Timer 2 consists of two 8-bit registers, TH2 and TL2. In the Timer function, the TL2 register is incremented every machine cycle. Since a machine cycle consists of 12 oscillator periods, the count rate is 1/12 of the oscillator frequency.

In the Counter function, the register is incremented in response to a 1-to-0 transition at its corresponding external input pin, T2. In this function, the external input is sampled during S5P2 of every machine cycle. When the samples show a high in one cycle and a low in the next cycle, the count is incremented. The new count value appears in the register during S3P1 of the cycle following the one in which the transition was detected.

Since two machine cycles (24 oscillator periods) are required to recognize a 1-to-0 transition, the maximum count rate is 1/24 of the oscillator frequency. To ensure that a given level is sampled at least once before it changes, the level should be held for at least one full machine cycle.

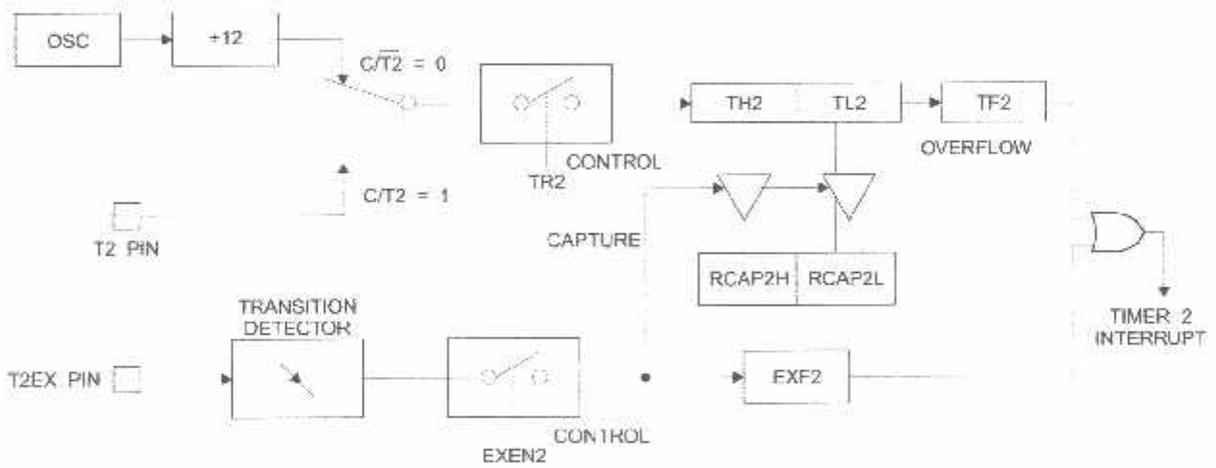
Table 8. Timer 2 Operating Modes

RCLK + TCLK	CP/$\overline{RL2}$	TR2	MODE
0	0	1	16-bit Auto-reload
0	1	1	16-bit Capture
1	X	1	Baud Rate Generator
X	X	0	(Off)

pture Mode

In the capture mode, two options are selected by bit EXEN2 in T2CON. If EXEN2 = 0, Timer 2 is a 16-bit timer or counter which upon overflow sets bit TF2 in T2CON. This bit can then be used to generate an interrupt. If EXEN2 = 1, Timer 2 performs the same operation, but a I-to-0 transition at external input T2EX also causes the current value in TH2 and TL2 to be captured into RCAP2H and RCAP2L, respectively. In addition, the transition at T2EX causes bit EXF2 in T2CON to be set. The EXF2 bit, like TF2, can generate an interrupt. The capture mode is illustrated in Figure 1.

ıre 1. Timer 2 in Capture Mode



to-reload (Up or Down unter)

Timer 2 can be programmed to count up or down when configured in its 16-bit auto-reload mode. This feature is invoked by the DCEN (Down Counter Enable) bit located in the SFR T2MOD (see Table 9). Upon reset, the DCEN bit is set to 0 so that timer 2 will default to count up. When DCEN is set, Timer 2 can count up or down, depending on the value of the T2EX pin.

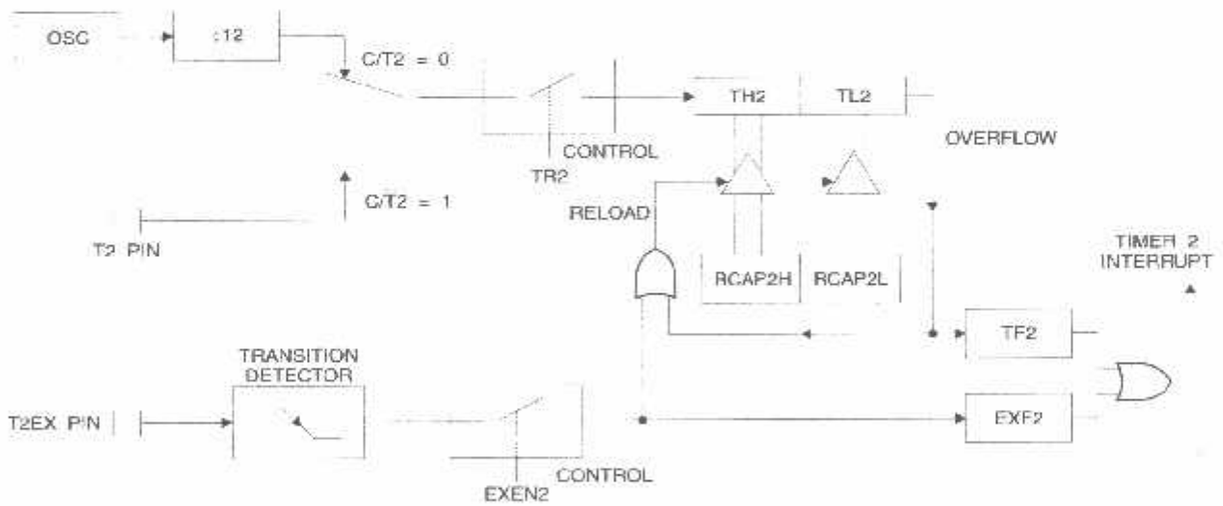
Figure 2 shows Timer 2 automatically counting up when DCEN = 0. In this mode, two options are selected by bit EXEN2 in T2CON. If EXEN2 = 0, Timer 2 counts up to 0FFFFH and then sets the TF2 bit upon overflow. The overflow also causes the timer registers to be reloaded with the 16-bit value in RCAP2H and RCAP2L. The values in RCAP2H and RCAP2L are preset by software. If EXEN2 = 1, a 16-bit reload can be triggered either by an overflow or by a 1-to-0 transition at external input T2EX. This transition also sets the EXF2 bit. Both the TF2 and EXF2 bits can generate an interrupt if enabled.

Setting the DCEN bit enables Timer 2 to count up or down, as shown in Figure 3. In this mode, the T2EX pin controls the direction of the count. A logic 1 at T2EX makes Timer 2 count up. The timer will overflow at 0FFFFH and set the TF2 bit. This overflow also causes the 16-bit value in RCAP2H and RCAP2L to be reloaded into the timer registers, TH2 and TL2, respectively.

A logic 0 at T2EX makes Timer 2 count down. The timer underflows when TH2 and TL2 equal the values stored in RCAP2H and RCAP2L. The underflow sets the TF2 bit and causes 0FFFFH to be reloaded into the timer registers.

The EXF2 bit toggles whenever Timer 2 overflows or underflows and can be used as a 17th bit of resolution. In this operating mode, EXF2 does not flag an interrupt.

ure 2. Timer 2 in Auto Reload Mode (DCEN = 0)



le 9. T2MOD – Timer 2 Mode Control Register

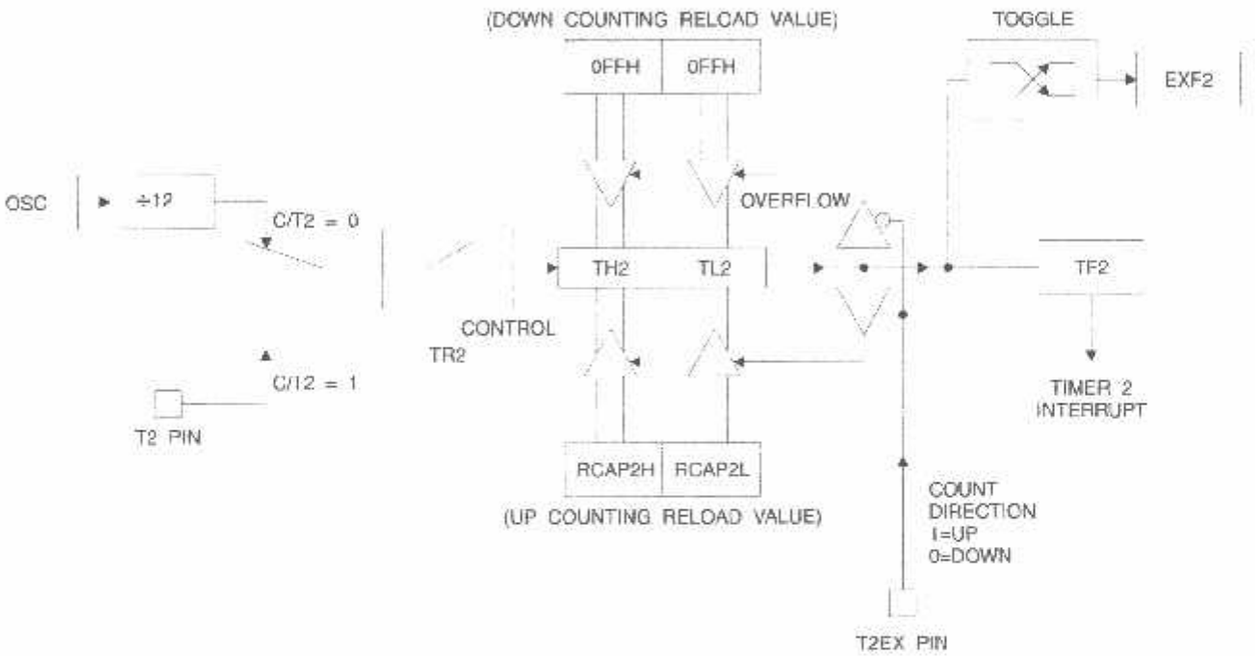
:MOD Address = 0C9H — Reset Value = XXXX XX00B

t Bit Addressable

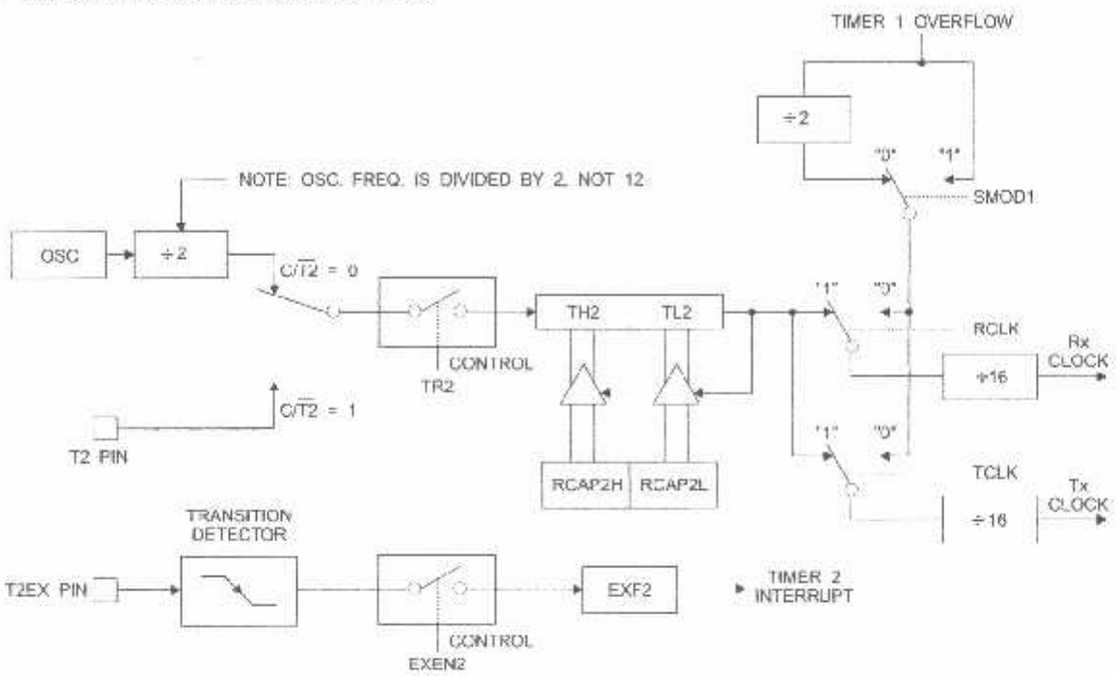
	–	–	–	–	–	–	T2OE	DCEN
Bit	7	6	5	4	3	2	1	0

mbol	Function
	Not implemented, reserved for future use.
OE	Timer 2 Output Enable bit.
EN	When set, this bit allows Timer 2 to be configured as an up/down counter.

ure 3. Timer 2 Auto Reload Mode (DCEN = 1)



ure 4. Timer 2 in Baud Rate Generator Mode



ıud Rate Generator

Timer 2 is selected as the baud rate generator by setting TCLK and/or RCLK in T2CON (Table 2). Note that the baud rates for transmit and receive can be different if Timer 2 is used for the receiver or transmitter and Timer 1 is used for the other function. Setting RCLK and/or TCLK puts Timer 2 into its baud rate generator mode, as shown in Figure 4.

The baud rate generator mode is similar to the auto-reload mode, in that a rollover in TH2 causes the Timer 2 registers to be reloaded with the 16-bit value in registers RCAP2H and RCAP2L, which are preset by software.

The baud rates in Modes 1 and 3 are determined by Timer 2's overflow rate according to the following equation.

$$\text{Modes 1 and 3 Baud Rates} = \frac{\text{Timer 2 Overflow Rate}}{16}$$

The Timer can be configured for either timer or counter operation. In most applications, it is configured for timer operation ($CP/\overline{T2} = 0$). The timer operation is different for Timer 2 when it is used as a baud rate generator. Normally, as a timer, it increments every machine cycle (at 1/12 the oscillator frequency). As a baud rate generator, however, it increments every state time (at 1/2 the oscillator frequency). The baud rate formula is given below.

$$\frac{\text{Modes 1 and 3}}{\text{Baud Rate}} = \frac{\text{Oscillator Frequency}}{32 \times [65536 - (\text{RCAP2H,RCAP2L})]}$$

where (RCAP2H, RCAP2L) is the content of RCAP2H and RCAP2L taken as a 16-bit unsigned integer.

Timer 2 as a baud rate generator is shown in Figure 4. This figure is valid only if RCLK or TCLK = 1 in T2CON. Note that a rollover in TH2 does not set TF2 and will not generate an interrupt. Note too, that if EXEN2 is set, a 1-to-0 transition in T2EX will set EXF2 but will not cause a reload from (RCAP2H, RCAP2L) to (TH2, TL2). Thus when Timer 2 is in use as a baud rate generator, T2EX can be used as an extra external interrupt.

Note that when Timer 2 is running (TR2 = 1) as a timer in the baud rate generator mode, TH2 or TL2 should not be read from or written to. Under these conditions, the Timer is incremented every state time, and the results of a read or write may not be accurate. The RCAP2 registers may be read but should not be written to, because a write might overlap a reload and cause write and/or reload errors. The timer should be turned off (clear TR2) before accessing the Timer 2 or RCAP2 registers.

ogrammable ock Out

A 50% duty cycle clock can be programmed to come out on P1.0, as shown in Figure 5. This pin, besides being a regular I/0 pin, has two alternate functions. It can be programmed to input the external clock for Timer/Counter 2 or to output a 50% duty cycle clock ranging from 61 Hz to 4 MHz (for a 16-MHz operating frequency).

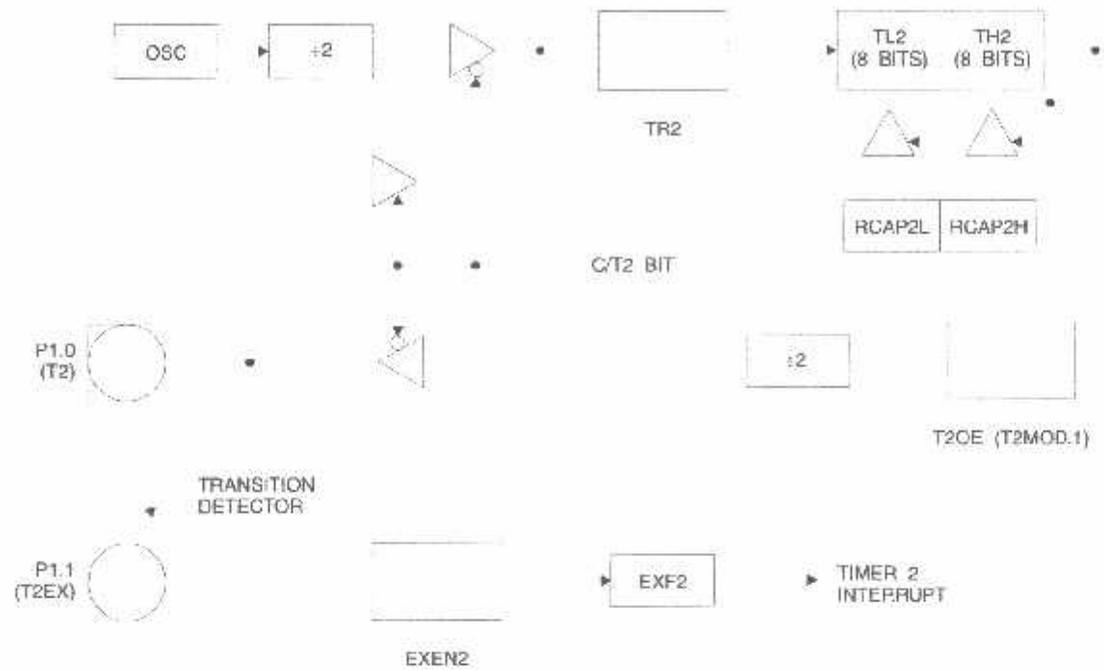
To configure the Timer/Counter 2 as a clock generator, bit C/$\overline{T2}$ (T2CON.1) must be cleared and bit T2OE (T2MOD.1) must be set. Bit TR2 (T2CON.2) starts and stops the timer.

The clock-out frequency depends on the oscillator frequency and the reload value of Timer 2 capture registers (RCAP2H, RCAP2L), as shown in the following equation.

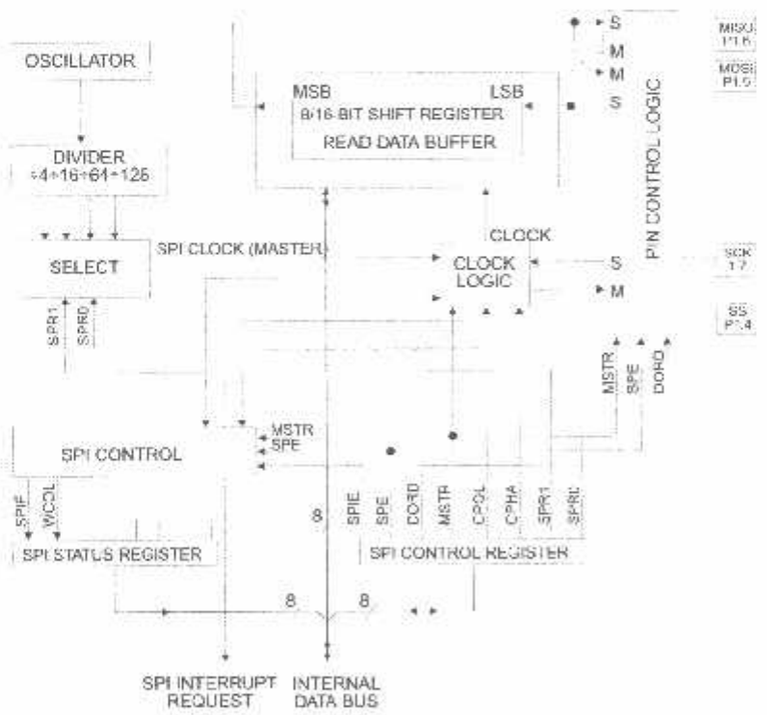
$$\text{Clock Out Frequency} = \frac{\text{Oscillator Frequency}}{4 \times [65536 - (\text{RCAP2H,RCAP2L})]}$$

In the clock-out mode, Timer 2 rollovers will not generate an interrupt. This behavior is similar to when Timer 2 is used as a baud-rate generator. It is possible to use Timer 2 as a baud-rate generator and a clock generator simultaneously. Note, however, that the baud-rate and clock-out frequencies cannot be determined independently from one another since they both use RCAP2H and RCAP2L.

ure 5. Timer 2 in Clock-out Mode



ure 6. SPI Block Diagram



ıRT

The UART in the AT89S8252 operates the same way as the UART in the AT89C51 and AT89C52. For further information on the UART operation, refer to the Atmel web site (http://www.atmel.com). From the home page, select "Products", then "Microcontrollers, then "8051-Architecture". Click on "Documentation", then on "Other Documents". Open the document "AT89 Series Hardware Description".

ırial Peripheral ɛrface

The serial peripheral interface (SPI) allows high-speed synchronous data transfer between the AT89S8252 and peripheral devices or between several AT89S8252 devices. The AT89S8252 SPI features include the following:

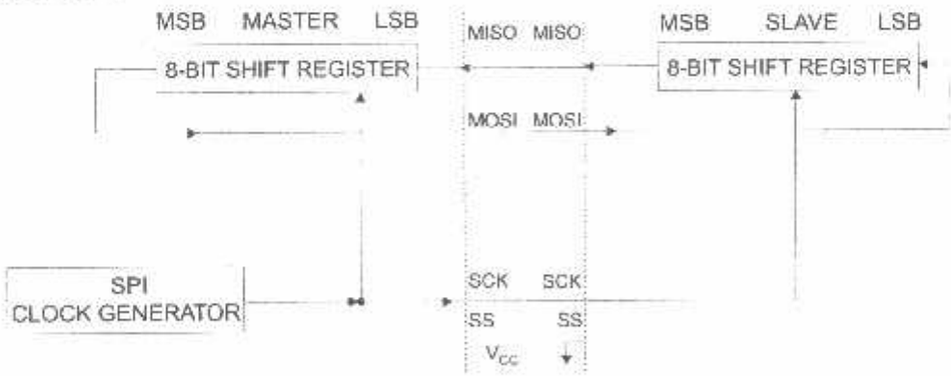
- Full-Duplex, 3-Wire Synchronous Data Transfer
- Master or Slave Operation
- 1.5 MHz Bit Frequency (max.)
- LSB First or MSB First Data Transfer
- Four Programmable Bit Rates
- End of Transmission Interrupt Flag
- Write Collision Flag Protection
- Wakeup from Idle Mode (Slave Mode Only)

The interconnection between master and slave CPUs with SPI is shown in the following figure. The SCK pin is the clock output in the master mode but is the clock input in the slave mode. Writing to the SPI data register of the master CPU starts the SPI clock generator, and the data written shifts out of the MOSI pin and into the MOSI pin of the slave CPU. After shifting one byte, the SPI clock generator stops, setting the end of transmission flag (SPIF). If both the SPI interrupt enable bit (SPIE) and the serial port interrupt enable bit (ES) are set, an interrupt is requested.

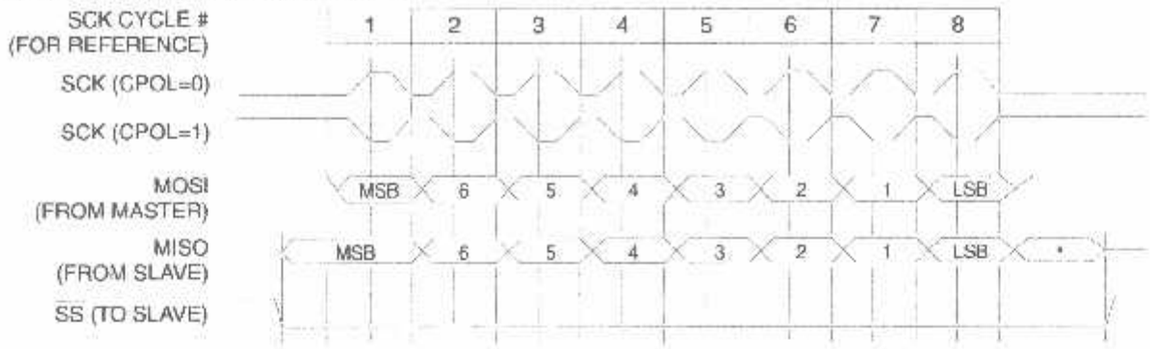
The Slave Select input, $\overline{SS}$/P1.4, is set low to select an individual SPI device as a slave. When $\overline{SS}$/P1.4 is set high, the SPI port is deactivated and the MOSI/P1.5 pin can be used as an input.

There are four combinations of SCK phase and polarity with respect to serial data, which are determined by control bits CPHA and CPOL. The SPI data transfer formats are shown in Figure 8 and Figure 9.

ure 7. SPI Master-slave Interconnection

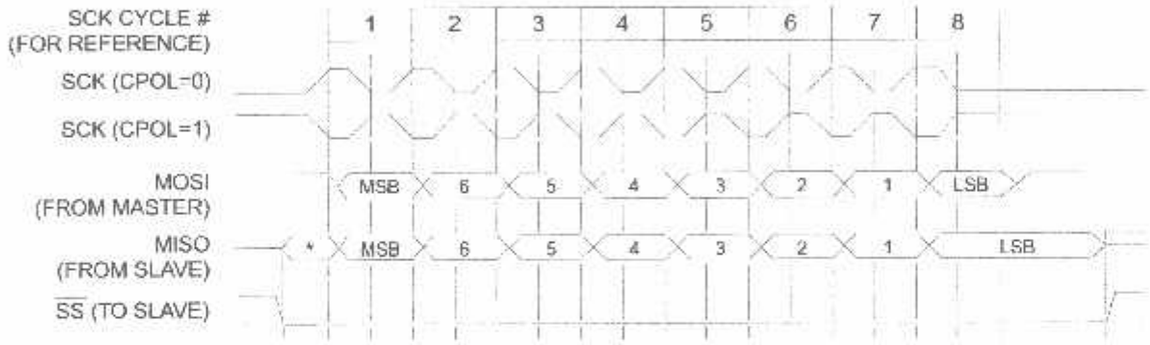


ure 8. SPI transfer Format with CPHA = 0



e: *Not defined but normally MSB of character just received

ure 9. SPI Transfer Format with CPHA = 1



e: *Not defined but normally LSB of previously transmitted character.

errupts

The AT89S8252 has a total of six interrupt vectors: two external interrupts ($\overline{INT0}$ and $\overline{INT1}$), three timer interrupts (Timers 0, 1, and 2), and the serial port interrupt. These interrupts are all shown in Figure 10.

Each of these interrupt sources can be individually enabled or disabled by setting or clearing a bit in Special Function Register IE. IE also contains a global disable bit, EA, which disables all interrupts at once.

Note that Table 10 shows that bit position IE.6 is unimplemented. In the AT89C51, bit position IE.5 is also unimplemented. User software should not write 1s to these bit positions, since they may be used in future AT89 products.

Timer 2 interrupt is generated by the logical OR of bits TF2 and EXF2 in register T2CON. Neither of these flags is cleared by hardware when the service routine is vectored to. In fact, the service routine may have to determine whether it was TF2 or EXF2 that generated the interrupt, and that bit will have to be cleared in software.

The Timer 0 and Timer 1 flags, TF0 and TF1, are set at S5P2 of the cycle in which the timers overflow. The values are then polled by the circuitry in the next cycle. However, the Timer 2 flag, TF2, is set at S2P2 and is polled in the same cycle in which the timer overflows.

le 10. Interrupt Enable (IE) Register

ISB)(LSB)

EA	–	ET2	ES	ET1	EX1	ET0	EX0

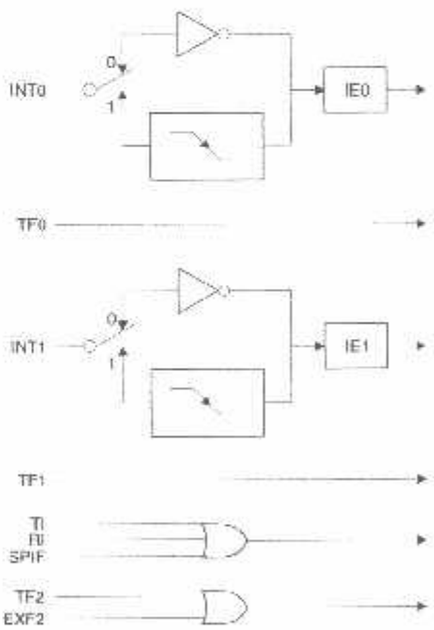
Enable Bit = 1 enables the interrupt.

Enable Bit = 0 disables the interrupt.

Symbol	Position	Function
EA	IE.7	Disables all interrupts. If EA = 0, no interrupt is acknowledged. If EA = 1, each interrupt source is individually enabled or disabled by setting or clearing its enable bit.
–	IE.6	Reserved.
ET2	IE.5	Timer 2 interrupt enable bit.
ES	IE.4	SPI and UART interrupt enable bit.
ET1	IE.3	Timer 1 interrupt enable bit.
EX1	IE.2	External interrupt 1 enable bit.
ET0	IE.1	Timer 0 interrupt enable bit.
EX0	IE.0	External interrupt 0 enable bit.

er software should never write 1s to unimplemented bits, because they may be used in future AT89 products.

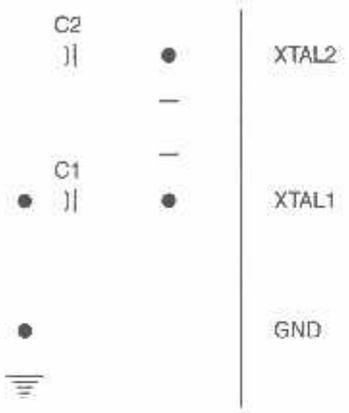
ure 10. Interrupt Sources



scillator
haracteristics

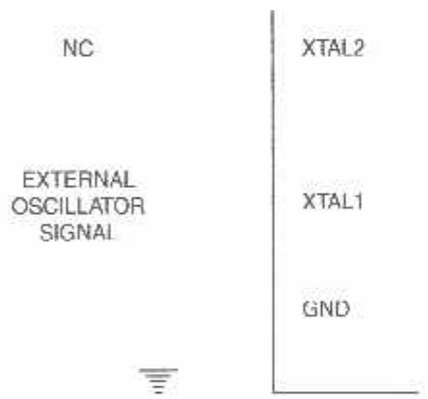
XTAL1 and XTAL2 are the input and output, respectively, of an inverting amplifier that can be configured for use as an on-chip oscillator, as shown in Figure 11. Either a quartz crystal or ceramic resonator may be used. To drive the device from an external clock source, XTAL2 should be left unconnected while XTAL1 is driven, as shown in Figure 12. There are no requirements on the duty cycle of the external clock signal, since the input to the internal clocking circuitry is through a divide-by-two flip-flop, but minimum and maximum voltage high and low time specifications must be observed.

Figure 11. Oscillator Connections



Note: C1, C2 = 30 pF ± 10 pF for Crystals
= 40 pF ± 10 pF for Ceramic Resonators

Figure 12. External Clock Drive Configuration



le Mode

In idle mode, the CPU puts itself to sleep while all the on-chip peripherals remain active. The mode is invoked by software. The content of the on-chip RAM and all the special functions registers remain unchanged during this mode. The idle mode can be terminated by any enabled interrupt or by a hardware reset.

Note that when idle mode is terminated by a hardware reset, the device normally resumes program execution from where it left off, up to two machine cycles before the internal reset algorithm takes control. On-chip hardware inhibits access to internal RAM in this event, but access to the port pins is not inhibited. To eliminate the possibility of an unexpected write to a port pin when idle mode is terminated by a reset, the instruction following the one that invokes idle mode should not write to a port pin or to external memory.

Status of External Pins During Idle and Power-down Modes

Mode	Program Memory	ALE	$\overline{PSEN}$	PORT0	PORT1	PORT2	PORT3
Idle	Internal	1	1	Data	Data	Data	Data
Idle	External	1	1	Float	Data	Address	Data
Power-down	Internal	0	0	Data	Data	Data	Data
Power-down	External	0	0	Float	Data	Data	Data

›wer-down Mode

In the power-down mode, the oscillator is stopped and the instruction that invokes power-down is the last instruction executed. The on-chip RAM and Special Function Registers retain their values until the power-down mode is terminated. Exit from power-down can be initiated either by a hardware reset or by an enabled external interrupt. Reset redefines the SFRs but does not change the on-chip RAM. The reset should not be activated before V_{CC} is restored to its normal operating level and must be held active long enough to allow the oscillator to restart and stabilize.

To exit power-down via an interrupt, the external interrupt must be enabled as level sensitive before entering power-down. The interrupt service routine starts at 16 ms (nominal) after the enabled interrupt pin is activated.

›ogram Memory ›ck Bits

The AT89S8252 has three lock bits that can be left unprogrammed (U) or can be programmed (P) to obtain the additional features listed in the following table.

When lock bit 1 is programmed, the logic level at the $\overline{EA}$ pin is sampled and latched during reset. If the device is powered up without a reset, the latch initializes to a random value and holds that value until reset is activated. The latched value of $\overline{EA}$ must agree with the current logic level at that pin in order for the device to function properly.

Once programmed, the lock bits can only be unprogrammed with the Chip Erase operations in either the parallel or serial modes.

›ck Bit Protection Modes[1][2]

	Program Lock Bits			
	LB1	LB2	LB3	Protection Type
1	U	U	U	No internal memory lock feature.
2	P	U	U	MOVC instructions executed from external program memory are disabled from fetching code bytes from internal memory. EA is sampled and latched on reset and further programming of the Flash memory (parallel or serial mode) is disabled.
3	P	P	U	Same as Mode 2, but parallel or serial verify are also disabled.
4	P	P	P	Same as Mode 3, but external execution is also disabled.

es: 1. U = Unprogrammed
2. P = Programmed

ogramming the ash and EEPROM

Atmel's AT89S8252 Flash Microcontroller offers 8K bytes of in-system reprogrammable Flash Code memory and 2K bytes of EEPROM Data memory.

The AT89S8252 is normally shipped with the on-chip Flash Code and EEPROM Data memory arrays in the erased state (i.e. contents = FFH) and ready to be programmed. This device supports a High-voltage (12-V V_{PP}) Parallel programming mode and a Low-voltage (5-V V_{CC}) Serial programming mode. The serial programming mode provides a convenient way to reprogram the AT89S8252 inside the user's system. The parallel programming mode is compatible with conventional third party Flash or EPROM programmers.

The Code and Data memory arrays are mapped via separate address spaces in the serial programming mode. In the parallel programming mode, the two arrays occupy one contiguous address space: 0000H to 1FFFH for the Code array and 2000H to 27FFH for the Data array.

The Code and Data memory arrays on the AT89S8252 are programmed byte-by-byte in either programming mode. An auto-erase cycle is provided with the self-timed programming operation in the serial programming mode. There is no need to perform the Chip Erase operation to reprogram any memory location in the serial programming mode unless any of the lock bits have been programmed.

In the parallel programming mode, there is no auto-erase cycle. To reprogram any non-blank byte, the user needs to use the Chip Erase operation first to erase both arrays.

Parallel Programming Algorithm: To program and verify the AT89S8252 in the parallel programming mode, the following sequence is recommended:

1. Power-up sequence:
   Apply power between V_{CC} and GND pins.
   Set RST pin to "H".
   Apply a 3 MHz to 24 MHz clock to XTAL1 pin and wait for at least 10 milliseconds.
2. Set $\overline{PSEN}$ pin to "L"
   ALE pin to "H"
   $\overline{EA}$ pin to "H" and all other pins to "H".
3. Apply the appropriate combination of "H" or "L" logic levels to pins P2.6, P2.7, P3.6, P3.7 to select one of the programming operations shown in the Flash Programming Modes table.
4. Apply the desired byte address to pins P1.0 to P1.7 and P2.0 to P2.5.
   Apply data to pins P0.0 to P0.7 for Write Code operation.
5. Raise $\overline{EA}/V_{PP}$ to 12V to enable Flash programming, erase or verification.
6. Pulse ALE/$\overline{PROG}$ once to program a byte in the Code memory array, the Data memory array or the lock bits. The byte-write cycle is self-timed and typically takes 1.5 ms.
7. To verify the byte just programmed, bring pin P2.7 to "L" and read the programmed data at pins P0.0 to P0.7.
8. Repeat steps 3 through 7 changing the address and data for the entire 2K or 8K bytes array or until the end of the object file is reached.
9. Power-off sequence:
   Set XTAL1 to "L".
   Set RST and $\overline{EA}$ pins to "L".
   Turn V_{CC} power off.

In the parallel programming mode, there is no auto-erase cycle and to reprogram any non-blank byte, the user needs to use the Chip Erase operation first to erase both arrays.

Data Polling: The AT89S8252 features DATA Polling to indicate the end of a byte write cycle. During a byte write cycle in the parallel or serial programming mode, an attempted read of the last byte written will result in the complement of the written datum on P0.7 (parallel mode), and on the MSB of the serial output byte on MISO (serial mode). Once the write cycle has been completed, true data are valid on all outputs, and the next cycle may begin. DATA Polling may begin any time after a write cycle has been initiated.

Ready/Busy: The progress of byte programming in the parallel programming mode can also be monitored by the RDY/BSY output signal. Pin P3.4 is pulled Low after ALE goes High during programming to indicate BUSY. P3.4 is pulled High again when programming is done to indicate READY.

Program Verify: If lock bits LB1 and LB2 have not been programmed, the programmed Code or Data byte can be read back via the address and data lines for verification. The state of the lock bits can also be verified directly in the parallel programming mode. In the serial programming mode, the state of the lock bits can only be verified indirectly by observing that the lock bit features are enabled.

Chip Erase: Both Flash and EEPROM arrays are erased electrically at the same time. In the parallel programming mode, chip erase is initiated by using the proper combination of control signals and by holding ALE/PROG low for 10 ms. The Code and Data arrays are written with all "1"s in the Chip Erase operation.

In the serial programming mode, a chip erase operation is initiated by issuing the Chip Erase instruction. In this mode, chip erase is self-timed and takes about 16 ms.

During chip erase, a serial read from any address location will return 00H at the data outputs.

Serial Programming Fuse: A programmable fuse is available to disable Serial Programming if the user needs maximum system security. The Serial Programming Fuse can only be programmed or erased in the Parallel Programming Mode.

The AT89S8252 is shipped with the Serial Programming Mode enabled.

Reading the Signature Bytes: The signature bytes are read by the same procedure as a normal verification of locations 030H and 031H, except that P3.6 and P3.7 must be pulled to a logic low. The values returned are as follows:

(030H) = 1EH indicates manufactured by Atmel
(031H) = 72H indicates 89S8252

ogramming lerface

Every code byte in the Flash and EEPROM arrays can be written, and the entire array can be erased, by using the appropriate combination of control signals. The write operation cycle is self-timed and once initiated, will automatically time itself to completion.

Most worldwide major programming vendors offer support for the Atmel AT89 microcontroller series. Please contact your local programming vendor for the appropriate software revision.

ɪrial Downloading

Both the Code and Data memory arrays can be programmed using the serial SPI bus while RST is pulled to V_{CC}. The serial interface consists of pins SCK, MOSI (input) and MISO (output). After RST is set high, the Programming Enable instruction needs to be executed first before program/erase operations can be executed.

An auto-erase cycle is built into the self-timed programming operation (in the serial mode ONLY) and there is no need to first execute the Chip Erase instruction unless any of the lock bits have been programmed. The Chip Erase operation turns the content of every memory location in both the Code and Data arrays into FFH.

The Code and Data memory arrays have separate address spaces:

0000H to 1FFFH for Code memory and 000H to 7FFH for Data memory.

Either an external system clock is supplied at pin XTAL1 or a crystal needs to be connected across pins XTAL1 and XTAL2. The maximum serial clock (SCK) frequency should be less than 1/40 of the crystal frequency. With a 24 MHz oscillator clock, the maximum SCK frequency is 600 kHz.

rial Programming gorithm

To program and verify the AT89S8252 in the serial programming mode, the following sequence is recommended:

1. Power-up sequence:

   Apply power between VCC and GND pins.

   Set RST pin to "H".

   If a crystal is not connected across pins XTAL1 and XTAL2, apply a 3 MHz to 24 MHz clock to XTAL1 pin and wait for at least 10 milliseconds.
2. Enable serial programming by sending the Programming Enable serial instruction to pin MOSI/P1.5. The frequency of the shift clock supplied at pin SCK/P1.7 needs to be less than the CPU clock at XTAL1 divided by 40.
3. The Code or Data array is programmed one byte at a time by supplying the address and data together with the appropriate Write instruction. The selected memory location is first automatically erased before new data is written. The write cycle is self-timed and typically takes less than 2.5 ms at 5V.
4. Any memory location can be verified by using the Read instruction which returns the content at the selected address at serial output MISO/P1.6.
5. At the end of a programming session, RST can be set low to commence normal operation.
6. Power-off sequence (if needed):

   Set XTAL1 to "L" (if a crystal is not used).

   Set RST to "L".

   Turn V_{CC} power off.

rial Programming
struction

The Instruction Set for Serial Programming follows a 3-byte protocol and is shown in the following table:

truction Set

struction	Input Format			Operation
	Byte 1	Byte 2	Byte 3	
ogramming Enable	1010 1100	0101 0011	xxxx xxxx	Enable serial programming interface after RST goes high.
ip Erase	1010 1100	xxxx x100	xxxx xxxx	Chip erase both 8K & 2K memory arrays.
ead Code Memory	aaaa a001	low addr	xxxx xxxx	Read data from Code memory array at the selected address. The 5 MSBs of the first byte are the high order address bits. The low order address bits are in the second byte. Data are available at pin MISO during the third byte.
rite Code Memory	aaaa a010	low addr	data in	Write data to Code memory location at selected address. The address bits are the 5 MSBs of the first byte together with the second byte.
ead Data Memory	00aa a101	low addr	xxxx xxxx	Read data from Data memory array at selected address. Data are available at pin MISO during the third byte.
rite Data Memory	00aa a110	low addr	data in	Write data to Data memory location at selected address.
rite Lock Bits	1010 1100	LB1 LB2 LB3 x x111	xxxx xxxx	Write lock bits. Set LB1, LB2 or LB3 = "0" to program lock bits.

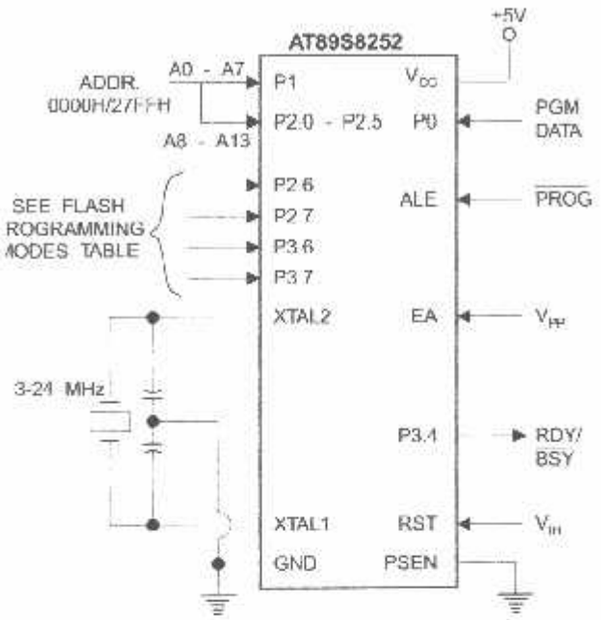
es: 1. DATA polling is used to indicate the end of a byte write cycle which typically takes less than 2.5 ms at 5V.
2. "aaaaa" = high order address.
3. "x" = don't care.

ash and EEPROM Parallel Programming Modes

›de	RST	PSEN	ALE/$\overline{PROG}$	$\overline{EA}/V_{PP}$	P2.6	P2.7	P3.6	P3.7	Data I/O P0.7:0	Address P2.5:0 P1.7:0
›rial Prog. Modes	H	h[1]	h[1]	x						
›ip Erase	H	L	(2)	12V	H	L	L	L	X	X
›ite (10K bytes) Memory	H	L		12V	L	H	H	H	DIN	ADDR
›ad (10K bytes) Memory	H	L	H	12V	L	L	H	H	DOUT	ADDR
›rite Lock Bits:	H	L		12V	H	L	H	L	DIN	X
Bit - 1									P0.7 = 0	X
Bit - 2									P0.6 = 0	X
Bit - 3									P0.5 = 0	X
›ad Lock Bits:	H	L	H	12V	H	H	L	L	DOUT	X
Bit - 1									@P0.2	X
Bit - 2									@P0.1	X
Bit - 3									@P0.0	X
›ad Atmel Code	H	L	H	12V	L	L	L	L	DOUT	30H
›ad Device Code	H	L	H	12V	L	L	L	L	DOUT	31H
›rial Prog. Enable	H	L	(2)	12V	L	H	L	H	P0.0 = 0	X
›rial Prog. Disable	H	L	(2)	12V	L	H	L	H	P0.0 = 1	X
›ad Serial Prog. Fuse	H	L	H	12V	H	H	L	H	@P0.0	X

es:
1. "h" = weakly pulled "High" internally.
2. Chip Erase and Serial Programming Fuse require a 10 ms $\overline{PROG}$ pulse. Chip Erase needs to be performed first before reprogramming any byte with a content other than FFH.
3. P3.4 is pulled Low during programming to indicate RDY/$\overline{BSY}$.
4. "X" = don't care

ıure 13. Programming the Flash/EEPROM Memory



ıure 14. Verifying the Flash/EEPROM Memory

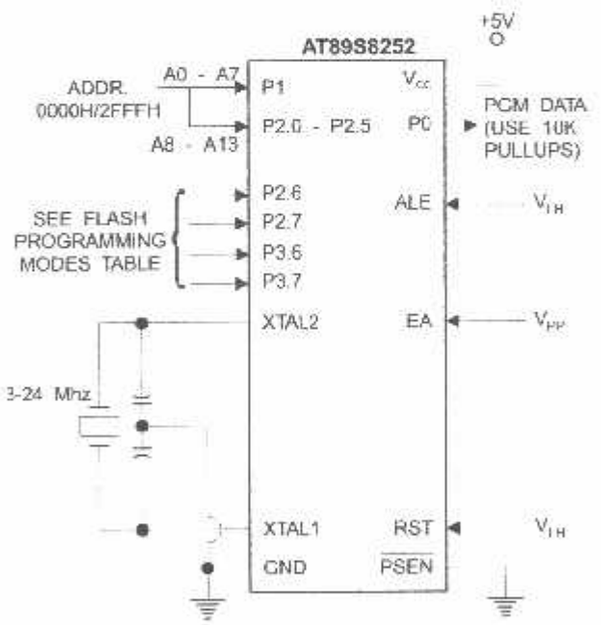
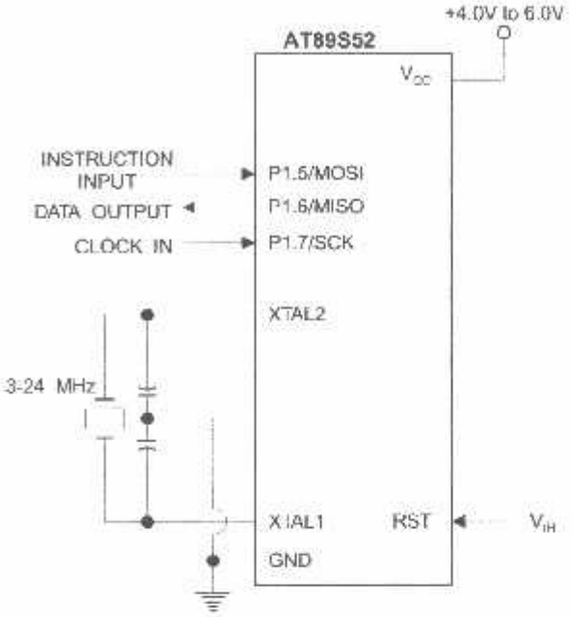


Figure 15. Flash/EEPROM Serial Downloading

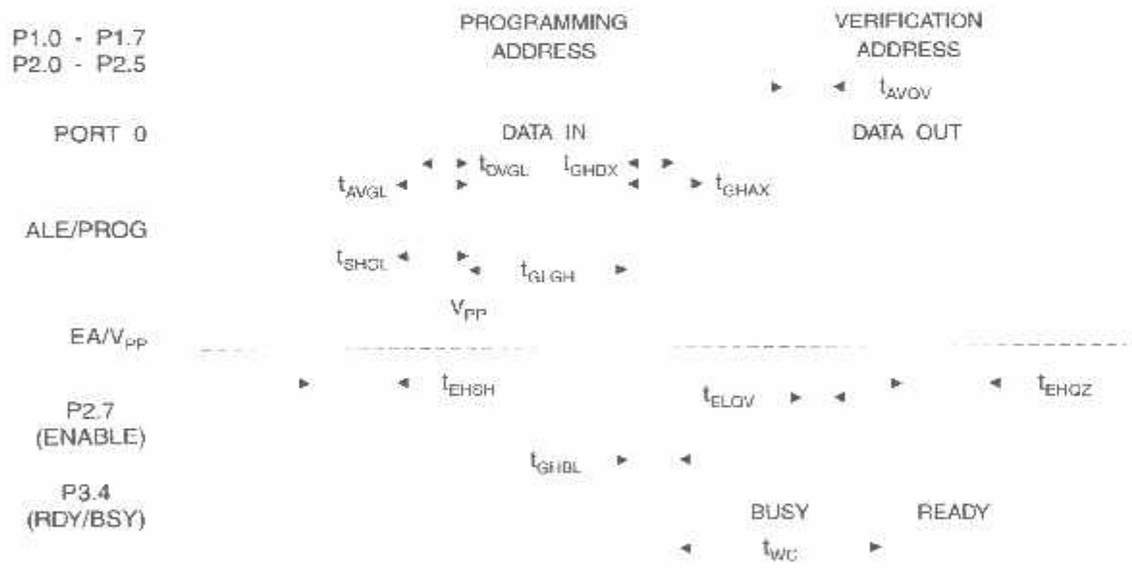


ash Programming and Verification Characteristics – Parallel Mode

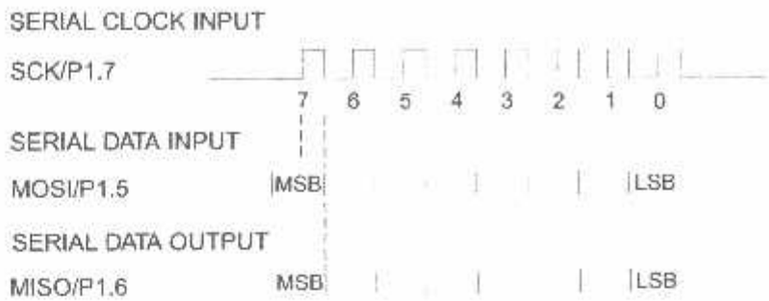
= 0°C to 70°C, V_{CC} = 5.0V ± 10%

ymbol	Parameter	Min	Max	Units
PP	Programming Enable Voltage	11.5	12.5	V
P	Programming Enable Current		1.0	mA
t_{CLCL}	Oscillator Frequency	3	24	MHz
AVGL	Address Setup to $\overline{PROG}$ Low	$48t_{CLCL}$		
GHAX	Address Hold after $\overline{PROG}$	$48t_{CLCL}$		
DVGL	Data Setup to $\overline{PROG}$ Low	$48t_{CLCL}$		
GHDX	Data Hold after $\overline{PROG}$	$48t_{CLCL}$		
EHSH	P2.7 ($\overline{ENABLE}$) High to V_{PP}	$48t_{CLCL}$		
SHGL	V_{PP} Setup to $\overline{PROG}$ Low	10		µs
GLGH	$\overline{PROG}$ Width	1	110	µs
AVQV	Address to Data Valid		$48t_{CLCL}$	
ELQV	$\overline{ENABLE}$ Low to Data Valid		$48t_{CLCL}$	
EHQZ	Data Float after $\overline{ENABLE}$	0	$48t_{CLCL}$	
GHBL	$\overline{PROG}$ High to $\overline{BUSY}$ Low		1.0	µs
WC	Byte Write Cycle Time		2.0	ms

ash/EEPROM Programming and Verification Waveforms – Parallel Mode

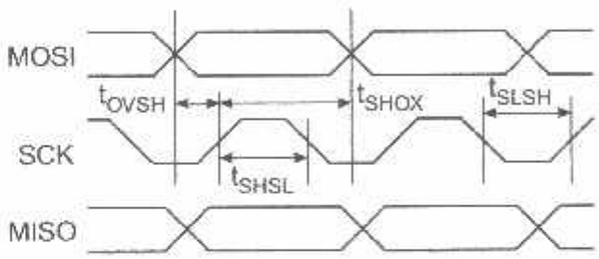


rial Downloading Waveforms



rial Programming Characteristics

ure 16. Serial Programming Timing



le 11. Serial Programming Characteristics, T_A = -40° C to 85° C, V_{CC} = 4.0 - 6.0V (Unless Otherwise Noted)

mbol	Parameter	Min	Typ	Max	Units
CLCL	Oscillator Frequency	0		24	MHz
CL	Oscillator Period	41.6			ns
SL	SCK Pulse Width High	24 t_{CLCL}			ns
SH	SCK Pulse Width Low	24 t_{CLCL}			ns
SH	MOSI Setup to SCK High	t_{CLCL}			ns
ICX	MOSI Hold after SCK High	2 t_{CLCL}			ns

›solute Maximum Ratings*

›erating Temperature	-55°C to +125°C
orage Temperature	-65°C to +150°C
iltage on Any Pin th Respect to Ground	-1.0V to +7.0V
aximum Operating Voltage	6.6V
: Output Current	15.0 mA

*NOTICE: Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

: Characteristics

: values shown in this table are valid for T_A = -40°C to 85°C and V_{CC} = 5.0V ± 20%, unless otherwise noted.

mbol	Parameter	Condition	Min	Max	Units
	Input Low-voltage	(Except $\overline{EA}$)	-0.5	0.2 V_{CC} - 0.1	V
1	Input Low-voltage ($\overline{EA}$)		-0.5	0.2 V_{CC} - 0.3	V
ı	Input High-voltage	(Except XTAL1, RST)	0.2 V_{CC} + 0.9	V_{CC} + 0.5	V
H	Input High-voltage	(XTAL1, RST)	0.7 V_{CC}	V_{CC} + 0.5	V
L	Output Low-voltage (1) (Ports 1,2,3)	I_{OL} = 1.6 mA		0.5	V
L1	Output Low-voltage (1) (Port 0, ALE, $\overline{PSEN}$)	I_{OL} = 3.2 mA		0.5	V
H	Output High-voltage (Ports 1,2,3, ALE, $\overline{PSEN}$)	I_{OH} = -60 µA, V_{CC} = 5V ± 10%	2.4		V
		I_{OH} = -25 µA	0.75 V_{CC}		V
		I_{OH} = -10 µA	0.9 V_{CC}		V
H1	Output High-voltage (Port 0 in External Bus Mode)	I_{OH} = -800 µA, V_{CC} = 5V ± 10%	2.4		V
		I_{OH} = -300 µA	0.75 V_{CC}		V
		I_{OH} = -80 µA	0.9 V_{CC}		V
	Logical 0 Input Current (Ports 1,2,3)	V_{IN} = 0.45V		-50	µA
	Logical 1 to 0 Transition Current (Ports 1,2,3)	V_{IN} = 2V, V_{CC} = 5V ± 10%		-650	µA
	Input Leakage Current (Port 0, $\overline{EA}$)	0.45 < V_{IN} < V_{CC}		±10	µA
ıST	Reset Pull-down Resistor		50	300	KΩ
)	Pin Capacitance	Test Freq. = 1 MHz, T_A = 25°C		10	pF
	Power Supply Current	Active Mode, 12 MHz		25	mA
		Idle Mode, 12 MHz		6.5	mA
	Power-down Mode (2)	V_{CC} = 6V		100	µA
		V_{CC} = 3V		40	µA

es: 1. Under steady state (non-transient) conditions, I_{OL} must be externally limited as follows:
Maximum I_{OL} per port pin: 10 mA
Maximum I_{OL} per 8-bit port: Port 0: 26 mA; Ports 1, 2, 3: 15 mA
Maximum total I_{OL} for all output pins: 71 mA
If I_{OL} exceeds the test condition, V_{OL} may exceed the related specification. Pins are not guaranteed to sink current greater than the listed test conditions.
2. Minimum V_{CC} for Power-down is 2V

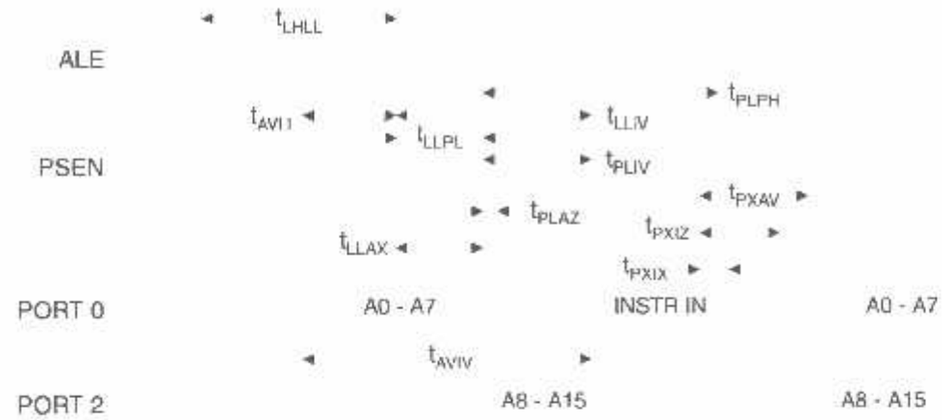
: Characteristics

der operating conditions, load capacitance for Port 0, ALE/$\overline{PROG}$, and $\overline{PSEN}$ = 100 pF; load capacitance for all other puts = 80 pF.

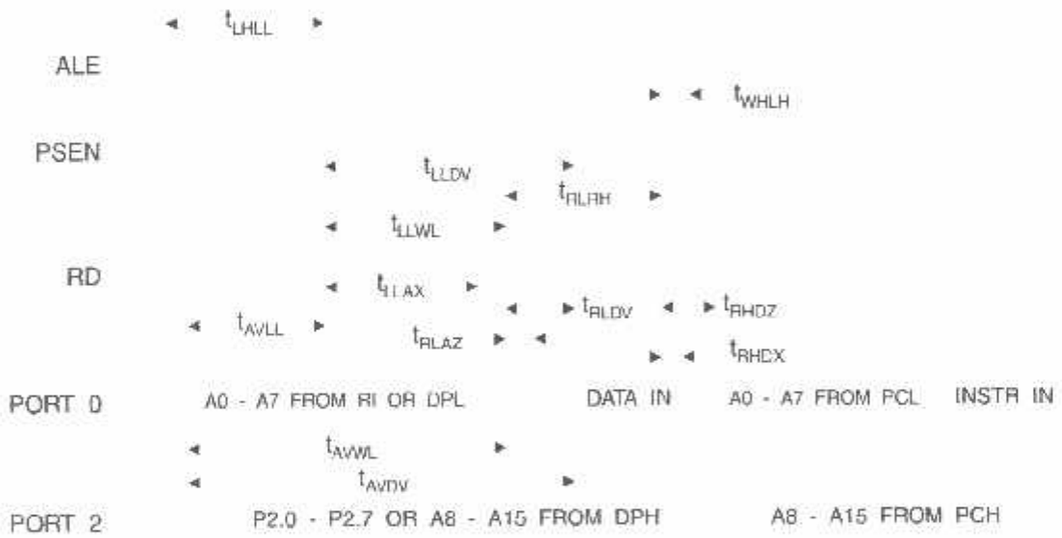
ternal Program and Data Memory Characteristics

mbol	Parameter	Variable Oscillator Min	Variable Oscillator Max	Units
CLCL	Oscillator Frequency	0	24	MHz
LL	ALE Pulse Width	$2t_{CLCL}$ - 40		ns
LL	Address Valid to ALE Low	t_{CLCL} - 13		ns
AX	Address Hold after ALE Low	t_{CLCL} - 20		ns
IV	ALE Low to Valid Instruction In		$4t_{CLCL}$ - 65	ns
PL	ALE Low to $\overline{PSEN}$ Low	t_{CLCL} - 13		ns
PH	$\overline{PSEN}$ Pulse Width	$3t_{CLCL}$ - 20		ns
IV	$\overline{PSEN}$ Low to Valid Instruction In		$3t_{CLCL}$ - 45	ns
IX	Input Instruction Hold after $\overline{PSEN}$	0		ns
IZ	Input Instruction Float after $\overline{PSEN}$		t_{CLCL} - 10	ns
AV	$\overline{PSEN}$ to Address Valid	t_{CLCL} - 8		ns
IV	Address to Valid Instruction In		$5t_{CLCL}$ - 55	ns
AZ	$\overline{PSEN}$ Low to Address Float		10	ns
RH	$\overline{RD}$ Pulse Width	$6t_{CLCL}$ - 100		ns
WH	$\overline{WR}$ Pulse Width	$6t_{CLCL}$ - 100		ns
DV	$\overline{RD}$ Low to Valid Data In		$5t_{CLCL}$ - 90	ns
HDX	Data Hold after RD	0		ns
HDZ	Data Float after $\overline{RD}$		$2t_{CLCL}$ - 28	ns
DV	ALE Low to Valid Data In		$8t_{CLCL}$ - 150	ns
AV	Address to Valid Data In		$9t_{CLCL}$ - 165	ns
VL	ALE Low to $\overline{RD}$ or $\overline{WR}$ Low	$3t_{CLCL}$ - 50	$3t_{CLCL}$ + 50	ns
WL	Address to $\overline{RD}$ or $\overline{WR}$ Low	$4t_{CLCL}$ - 75		ns
WX	Data Valid to $\overline{WR}$ Transition	t_{CLCL} - 20		ns
WH	Data Valid to $\overline{WR}$ High	$7t_{CLCL}$ - 120		ns
QX	Data Hold after $\overline{WR}$	t_{CLCL} - 20		ns
AZ	$\overline{RD}$ Low to Address Float		0	ns
LH	$\overline{RD}$ or $\overline{WR}$ High to ALE High	t_{CLCL} - 20	t_{CLCL} + 25	ns

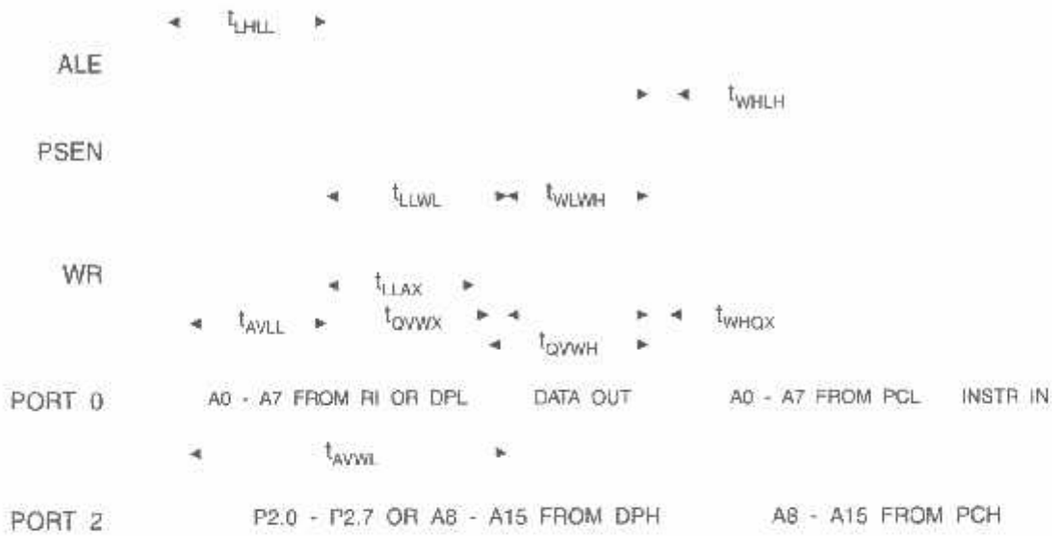
:ternal Program Memory Read Cycle



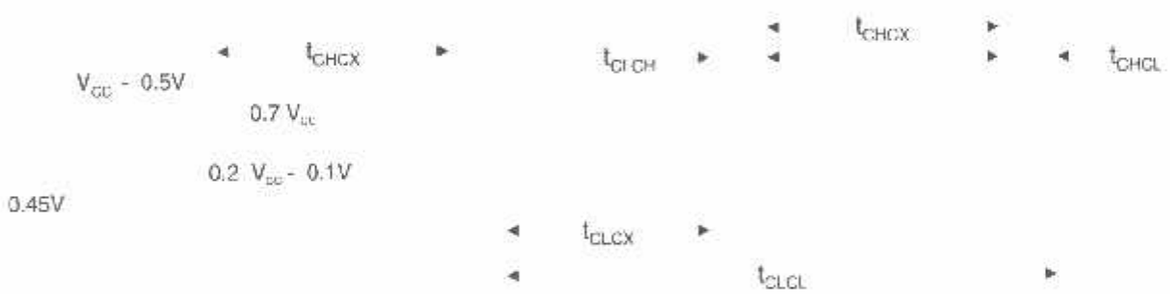
:ternal Data Memory Read Cycle



:ternal Data Memory Write Cycle



:ternal Clock Drive Waveforms



tternal Clock Drive

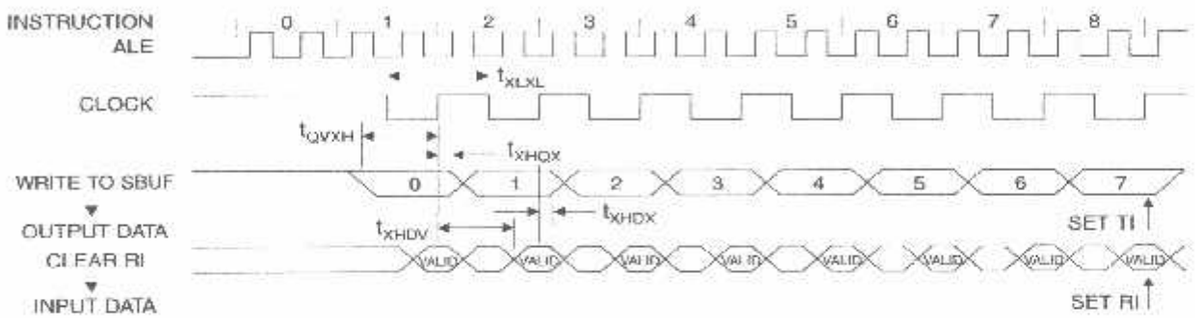
·mbol	Parameter	V_{CC} = 4.0V to 6.0V Min	Max	Units
·CLCL	Oscillator Frequency	0	24	MHz
·CL	Clock Period	41.6		ns
ICX	High Time	15		ns
·CX	Low Time	15		ns
·CH	Rise Time		20	ns
·CL	Fall Time		20	ns

rial Port Timing: Shift Register Mode Test Conditions

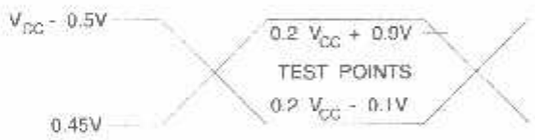
values in this table are valid for V_{CC} = 4.0V to 6V and Load Capacitance = 80 pF.

mbol	Parameter	Variable Oscillator Min	Variable Oscillator Max	Units
XL	Serial Port Clock Cycle Time	$12t_{CLCL}$		µs
QVH	Output Data Setup to Clock Rising Edge	$10t_{CLCL}$ - 133		ns
QX	Output Data Hold after Clock Rising Edge	$2t_{CLCL}$ - 117		ns
DX	Input Data Hold after Clock Rising Edge	0		ns
DV	Clock Rising Edge to Input Data Valid		$10t_{CLCL}$ - 133	ns

ift Register Mode Timing Waveforms



Testing Input/Output Waveforms[1]



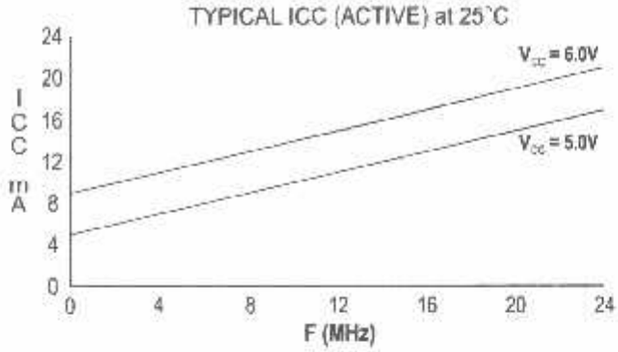
1. AC Inputs during testing are driven at V_{CC} - 0.5V for a logic 1 and 0.45V for a logic 0. Timing measurements are made at V_{IH} min. for a logic 1 and V_{IL} max. for a logic 0.

oat Waveforms[1]

1. For timing purposes, a port pin is no longer floating when a 100 mV change from load voltage occurs. A port pin begins to float when a 100 mV change from the loaded V_{OH}/V_{OL} level occurs.

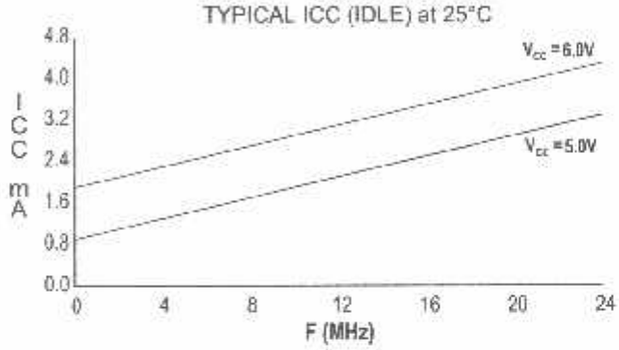
AT89S8252

TYPICAL ICC (ACTIVE) at 25°C



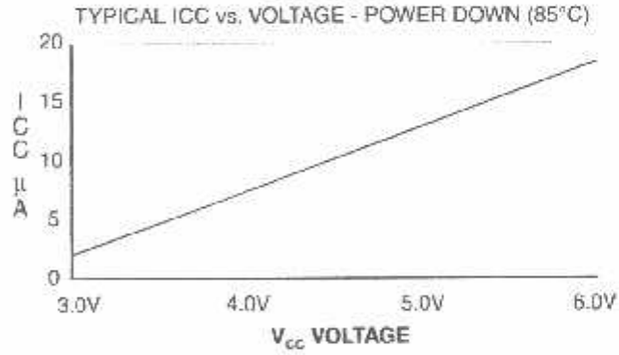
AT89S8252

TYPICAL ICC (IDLE) at 25°C



AT89S8252

TYPICAL ICC vs. VOLTAGE - POWER DOWN (85°C)



Notes: 1. XTAL1 tied to GND for Icc (power-down)
2. Lock bits programmed

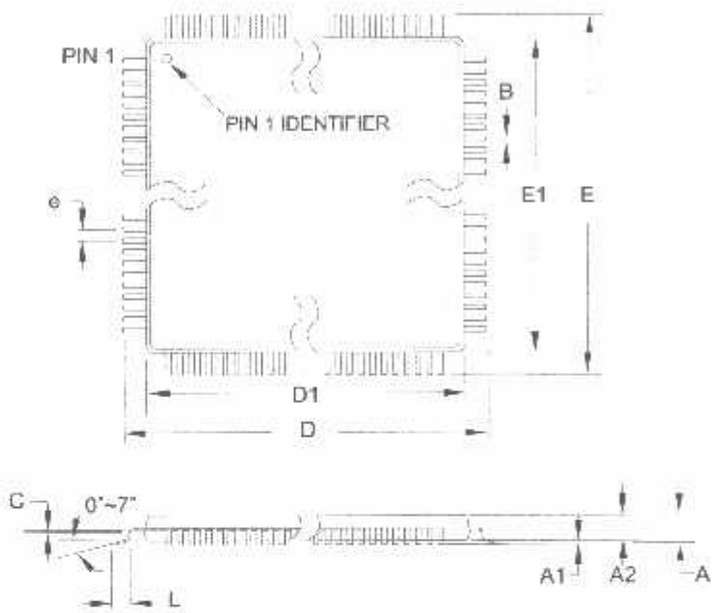
·dering Information

Speed (MHz)	Power Supply	Ordering Code	Package	Operation Range
24	4.0V to 6.0V	AT89S8252-24AC	44A	Commercial (0° C to 70° C)
		AT89S8252-24JC	44J	
		AT89S8252-24PC	40P6	
	4.0V to 6.0V	AT89S8252-24AI	44A	Industrial (-40° C to 85° C)
		AT89S8252-24JI	44J	
		AT89S8252-24PI	40P6	

	Package Type
A	44-lead, Thin Plastic Gull Wing Quad Flatpack (TQFP)
J	44-lead, Plastic J-leaded Chip Carrier (PLCC)
P6	40-lead, 0.600" Wide, Plastic Dual Inline Package (PDIP)

ıckaging Information

A – TQFP



COMMON DIMENSIONS
(Unit of Measure = mm)

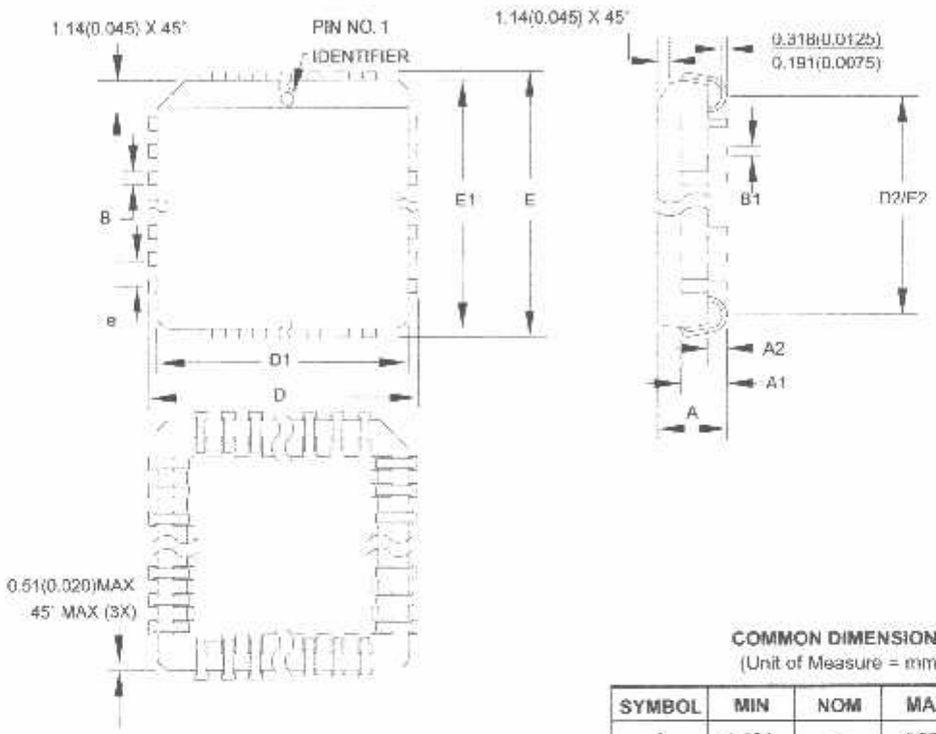
SYMBOL	MIN	NOM	MAX	NOTE
A	–	–	1.20	
A1	0.05		0.15	
A2	0.95	1.00	1.05	
D	11.75	12.00	12.25	
D1	9.90	10.00	10.10	Note 2
E	11.75	12.00	12.25	
E1	9.90	10.00	10.10	Note 2
B	0.30	–	0.45	
C	0.09	–	0.20	
L	0.45	–	0.75	
e	0.80 TYP			

Notes:
1. This package conforms to JEDEC reference MS-026, Variation ACB.
2. Dimensions D1 and E1 do not include mold protrusion. Allowable protrusion is 0.25 mm per side. Dimensions D1 and E1 are maximum plastic body size dimensions including mold mismatch.
3. Lead coplanarity is 0.10 mm maximum.

10/5/2001

	TITLE	DRAWING NO.	REV.
2325 Orchard Parkway San Jose, CA 95131	**44A**, 44-lead, 10 x 10 mm Body Size, 1.0 mm Body Thickness, 0.8 mm Lead Pitch, Thin Profile Plastic Quad Flat Package (TQFP)	44A	B

J – PLCC



COMMON DIMENSIONS
(Unit of Measure = mm)

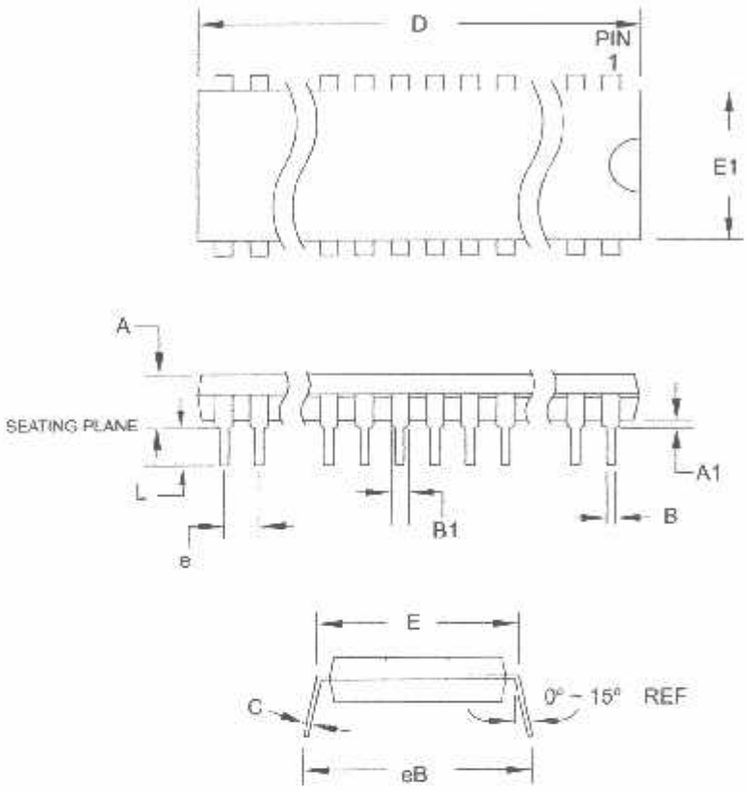
SYMBOL	MIN	NOM	MAX	NOTE
A	4.191	–	4.572	
A1	2.286	–	3.048	
A2	0.508	–	–	
D	17.399	–	17.653	
D1	16.510	–	16.662	Note 2
E	17.399	–	17.653	
E1	16.510	–	16.662	Note 2
D2/E2	14.986	–	16.002	
B	0.660	–	0.813	
B1	0.330	–	0.533	
e	1.270 TYP			

Notes:
1. This package conforms to JEDEC reference MS-018, Variation AC.
2. Dimensions D1 and E1 do not include mold protrusion. Allowable protrusion is .010"(0.254 mm) per side. Dimension D1 and E1 include mold mismatch and are measured at the extreme material condition at the upper or lower parting line.
3. Lead coplanarity is 0.004" (0.102 mm) maximum.

10/04/01

	TITLE	DRAWING NO.	REV.
2325 Orchard Parkway San Jose, CA 95131	**44J**, 44-lead, Plastic J-leaded Chip Carrier (PLCC)	44J	B

P6 – PDIP



COMMON DIMENSIONS
(Unit of Measure = mm)

SYMBOL	MIN	NOM	MAX	NOTE
A		–	4.826	
A1	0.381	–	–	
D	52.070	–	52.578	Note 2
E	15.240	–	15.875	
E1	13.462	–	13.970	Note 2
B	0.356	–	0.558	
B1	1.041	–	1.651	
L	3.048	–	3.556	
C	0.203	–	0.381	
eB	15.494	–	17.526	
e	2.540 TYP			

Notes:
1. This package conforms to JEDEC reference MS-011, Variation AC.
2. Dimensions D and E1 do not include mold Flash or Protrusion. Mold Flash or Protrusion shall not exceed 0.25 mm (0.010").

09/28/01

	TITLE	DRAWING NO.	REV.
2325 Orchard Parkway San Jose, CA 95131	**40P6**, 40-lead (0.600"/15.24 mm Wide) Plastic Dual Inline Package (PDIP)	40P6	B

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Fax: (33) 4-76-58-34-80

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www.atmel.com/literature

0401F–MICRO–11/03 xM

Winbond Electronics Corp.

ISD2560/75/90/120

SINGLE-CHIP, MULTIPLE-MESSAGES,

VOICE RECORD/PLAYBACK DEVICE

60-, 75-, 90-, AND 120-SECOND DURATION

Publication Release Date: May 2003
Revision 1.0

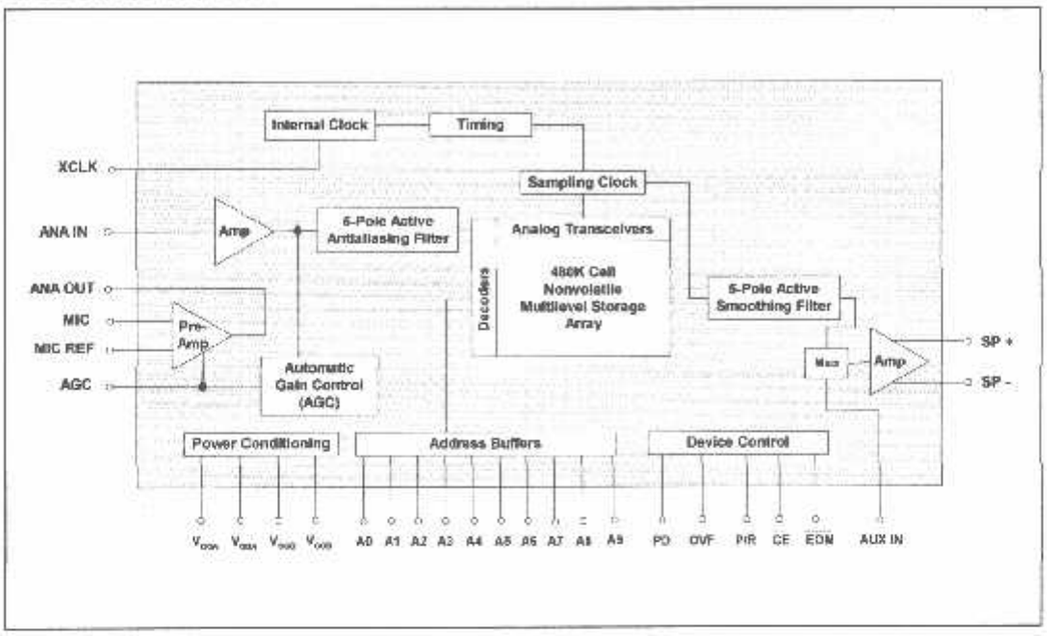
1. GENERAL DESCRIPTION

Winbond's ISD2500 ChipCorder® Series provide high-quality, single-chip, Record/Playback solutions for 60- to 120-second messaging applications. The CMOS devices include an on-chip oscillator, microphone preamplifier, automatic gain control, antialiasing filter, smoothing filter, speaker amplifier, and high density multi-level storage array. In addition, the ISD2500 is microcontroller compatible, allowing complex messaging and addressing to be achieved. Recordings are stored into on-chip nonvolatile memory cells, providing zero-power message storage. This unique, single-chip solution is made possible through Winbond's patented multilevel storage technology. Voice and audio signals are stored directly into memory in their natural form, providing high-quality, solid-state voice reproduction.

2. FEATURES

- Easy-to-use single-chip, voice record/playback solution
- High-quality, natural voice/audio reproduction
- Single-chip with duration of 60, 75, 90, or 120 seconds.
- Manual switch or microcontroller compatible
- Playback can be edge- or level-activated
- Directly cascadable for longer durations
- Automatic power-down (push-button mode)
  - Standby current 1 µA (typical)
- Zero-power message storage
  - Eliminates battery backup circuits
- Fully addressable to handle multiple messages
- 100-year message retention (typical)
- 100,000 record cycles (typical)
- On-chip clock source
- Programmer support for play-only applications
- Single +5 volt power supply
- Available in die form, PDIP, SOIC and TSOP packaging
- Temperature = die (0° C to +50°C) and package (0°C to +70°C)

3. BLOCK DIAGRAM



Winbond Electronics Corp.

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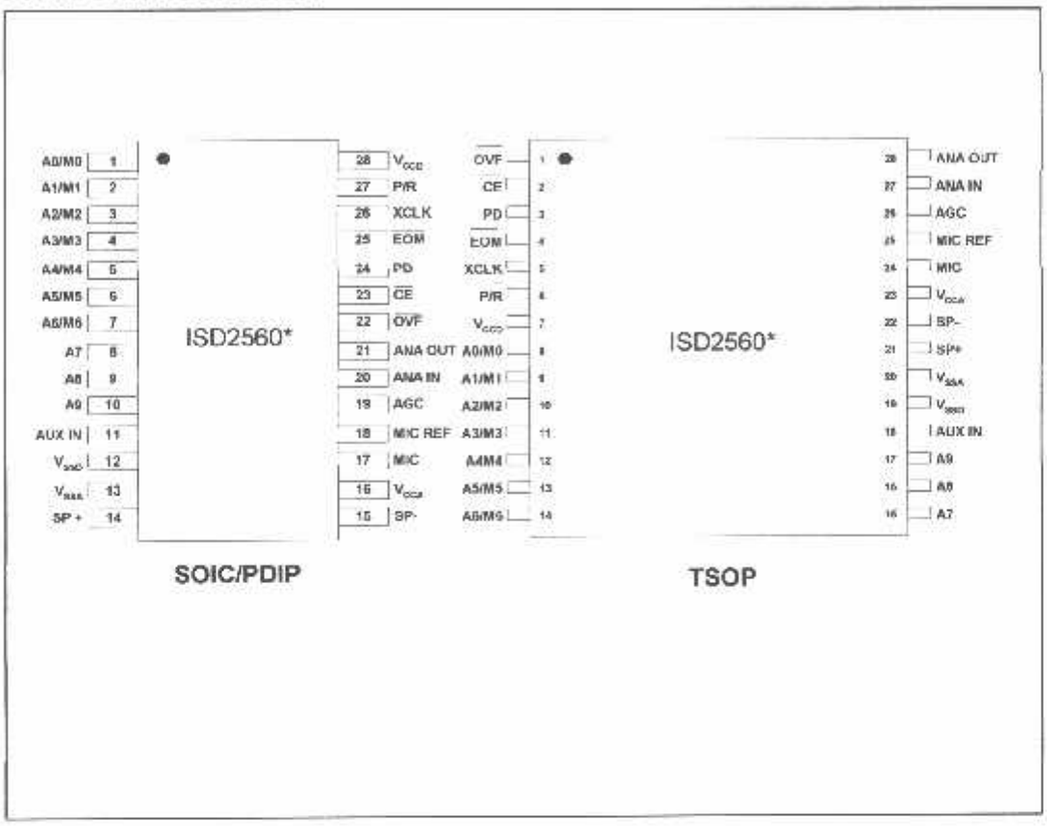
5. PIN CONFIGURATION



* Same pinouts for ISD2575 / 2590 / 25120 products

6. PIN DESCRIPTION

Ax/Mx	1-10/ 1-7	8-17/ 8-14	**Address/Mode Inputs**: The Address/Mode inputs have two functions depending on the level of the two Most Significant Bits (MSB) of the address pins (A8 and A9). If either or both of the two MSBs are LOW, the inputs are all interpreted as address bits and are used as the start address for the current record or playback cycle. The address pins are inputs only and do not output any internal address information during the operation. Address inputs are latched by the falling edge of $\overline{CE}$. If both MSBs are HIGH, the Address/Mode inputs are interpreted as Mode bits according to the Operational Mode table on page 12. There are six operational modes (M0...M6) available as indicated in the table. It is possible to use multiple operational modes simultaneously. Operational Modes are sampled on each falling edge of $\overline{CE}$, and thus Operational Modes and direct addressing are mutually exclusive.
AUX IN	11	18	**Auxiliary Input**: The Auxiliary Input is multiplexed through to the output amplifier and speaker output pins when $\overline{CE}$ is HIGH, $P/\overline{R}$ is HIGH, and playback is currently not active or if the device is in playback overflow. When cascading multiple ISD2500 devices, the AUX IN pin is used to connect a playback signal from a following device to the previous output speaker drivers. For noise considerations, it is suggested that the auxiliary input not be driven when the storage array is active.
V_{SSA}, V_{SSD}	13, 12	20, 19	**Ground**: The ISD2500 series of devices utilizes separate analog and digital ground busses. These pins should be connected separately through a low-impedance path to power supply ground.
SP+/SP-	14/15	21/22	**Speaker Outputs**: All devices in the ISD2500 series include an on-chip differential speaker driver, capable of driving 50 mW into 16 Ω from AUX IN (12.2mW from memory). [1] The speaker outputs are held at V_{SSA} levels during record and power down. It is therefore not possible to parallel speaker outputs of multiple ISD2500 devices or the outputs of other speaker drivers. [2] A single-end output may be used (including a coupling capacitor between the SP pin and the speaker). These outputs may be used individually with the output signal taken from either pin. However, the use of single-end output results in a 1 to 4 reduction in its output power.

[1] Connection of speaker outputs in parallel may cause damage to the device.
[2] Never ground or drive an unused speaker output.

V_{CCA}, V_{CCD}	16, 28	23, 7	**Supply Voltage**: To minimize noise, the analog and digital circuits in the ISD2500 series devices use separate power busses. These voltage busses are brought out to separate pins and should be tied together as close to the supply as possible. In addition, these supplies should be decoupled as close to the package as possible.
MIC	17	24	**Microphone**: The microphone pin transfers input signal to the on-chip preamplifier. A built-in Automatic Gain Control (AGC) circuit controls the gain of this preamplifier from –15 to 24dB. An external microphone should be AC coupled to this pin via a series capacitor. The capacitor value, together with the internal 10 KΩ resistance on this pin, determines the low-frequency cutoff for the ISD2500 series passband. See Winbond's Application Information for additional information on low-frequency cutoff calculation.
MIC REF	18	25	**Microphone Reference**: The MIC REF input is the inverting input to the microphone preamplifier. This provides a noise-canceling or common-mode rejection input to the device when connected to a differential microphone.
AGC	19	26	**Automatic Gain Control**: The AGC dynamically adjusts the gain of the preamplifier to compensate for the wide range of microphone input levels. The AGC allows the full range of whispers to loud sounds to be recorded with minimal distortion. The "attack" time is determined by the time constant of a 5 KΩ internal resistance and an external capacitor (C2 on the schematic of Figure 5 in section 11) connected from the AGC pin to V_{SSA} analog ground. The "release" time is determined by the time constant of an external resistor (R2) and an external capacitor (C2) connected in parallel between the AGC pin and V_{SSA} analog ground. Nominal values of 470 KΩ and 4.7 µF give satisfactory results in most cases.
ANA IN	20	27	**Analog Input**: The analog input transfers analog signal to the chip for recording. For microphone inputs, the ANA OUT pin should be connected via an external capacitor to the ANA IN pin. This capacitor value, together with the 3.0 KΩ input impedance of ANA IN, is selected to give additional cutoff at the low-frequency end of the voice passband. If the desired input is derived from a source other than a microphone, the signal can be fed, capacitively coupled, into the ANA IN pin directly.
ANA OUT	21	28	**Analog Output**: This pin provides the preamplifier output to the user. The voltage gain of the preamplifier is determined by the voltage level at the AGC pin.

$\overline{OVF}$	22	1	**Overflow**: This signal pulses LOW at the end of memory array, indicating the device has been filled and the message has overflowed. The $\overline{OVF}$ output then follows the $\overline{CE}$ input until a PD pulse has reset the device. This pin can be used to cascade several ISD2500 devices together to increase record/playback durations.
$\overline{CE}$	23	2	**Chip Enable**: The $\overline{CE}$ input pin is taken LOW to enable all playback and record operations. The address pins and playback/record pin (P/$\overline{R}$) are latched by the falling edge of $\overline{CE}$. $\overline{CE}$ has additional functionality in the M6 (Push-Button) Operational Mode as described in the Operational Mode section.
PD	24	3	**Power Down**: When neither record nor playback operation, the PD pin should be pulled HIGH to place the part in standby mode (see I_{SB} specification). When overflow ($\overline{OVF}$) pulses LOW for an overflow condition, PD should be brought HIGH to reset the address pointer back to the beginning of the memory array. The PD pin has additional functionality in the M6 (Push-Button) Operation Mode as described in the Operational Mode section.
$\overline{EOM}$	25	4	**End-Of-Message**: A nonvolatile marker is automatically inserted at the end of each recorded message. It remains there until the message is recorded over. The $\overline{EOM}$ output pulses LOW for a period of T_{EOM} at the end of each message. In addition, the ISD2500 series has an internal V_{CC} detect circuit to maintain message integrity should V_{CC} fall below 3.5V. In this case, $\overline{EOM}$ goes LOW and the device is fixed in Playback-only mode. When the device is configured in Operational Mode M6 (Push-Button Mode), this pin provides an active-HIGH signal, indicating the device is currently recording or playing. This signal can conveniently drive an LED for visual indicator of a record or playback operation in process.

<table>
<tr><td>XCLK</td><td>26</td><td>5</td><td>External Clock: The external clock input has an internal pull-down device. The device is configured at the factory with an internal sampling clock frequency centered to ±1 percent of specification. The frequency is then maintained to a variation of ±2.25 percent over the entire commercial temperature and operating voltage ranges. If greater precision is required, the device can be clocked through the XCLK pin as follows:
<table>
<tr><th>Part Number</th><th>Sample Rate</th><th>Required Clock</th></tr>
<tr><td>ISD2560</td><td>8.0 kHz</td><td>1024 kHz</td></tr>
<tr><td>ISD2575</td><td>6.4 kHz</td><td>819.2 kHz</td></tr>
<tr><td>ISD2590</td><td>5.3 kHz</td><td>682.7 kHz</td></tr>
<tr><td>ISD25120</td><td>4.0 kHz</td><td>512 kHz</td></tr>
</table>
These recommended clock rates should not be varied because the antialiasing and smoothing filters are fixed, and aliasing problems can occur if the sample rate differs from the one recommended. The duty cycle on the input clock is not critical, as the clock is immediately divided by two. If the XCLK is not used, this input must be connected to ground.</td></tr>
<tr><td>P/$\overline{R}$</td><td>27</td><td>6</td><td>Playback/Record: The P/$\overline{R}$ input pin is latched by the falling edge of the $\overline{CE}$ pin. A HIGH level selects a playback cycle while a LOW level selects a record cycle. For a record cycle, the address pins provide the starting address and recording continues until PD or $\overline{CE}$ is pulled HIGH or an overflow is detected (i.e. the chip is full). When a record cycle is terminated by pulling PD or $\overline{CE}$ HIGH, then End-Of-Message ($\overline{EOM}$) marker is stored at the current address in memory. For a playback cycle, the address inputs provide the starting address and the device will play until an $\overline{EOM}$ marker is encountered. The device can continue to pass an $\overline{EOM}$ marker if $\overline{CE}$ is held LOW in address mode, or in an Operational Mode. (See Operational Modes section)</td></tr>
</table>

7. FUNCTIONAL DESCRIPTION

7.1. Detailed Description

Speech/Sound Quality

The Winbond's ISD2500 series includes devices offered at 4.0, 5.3, 6.4, and 8.0 kHz sampling frequencies, allowing the user a choice of speech quality options. Increasing the duration within a product series decreases the sampling frequency and bandwidth, which affects the sound quality. Please refer to the ISD2560/75/90/120 Product Summary table below to compare the duration, sampling frequency and filter pass band.

The speech samples are stored directly into the on-chip nonvolatile memory without any digitization and compression associated like other solutions. Direct analog storage provides a very true, natural sounding reproduction of voice, music, tones, and sound effects not available with most solid state digital solutions.

Duration

To meet various system requirements, the ISD2560/75/90/120 products offer single-chip solutions at 60, 75, 90, and 120 seconds. Parts may also be cascaded together for longer durations.

TABLE 1: ISD2560/75/90/120 PRODUCT SUMMARY

ISD2560	60	8.0	3.4
ISD2575	75	6.4	2.7
ISD2590	90	5.3	2.3
ISD25120	120	4.0	1.7

* 3db roll-off point

EEPROM Storage

One of the benefits of Winbond's ChipCorder® technology is the use of on-chip nonvolatile memory, providing zero-power message storage. The message is retained for up to 100 years typically without power. In addition, the device can be re-recorded typically over 100,000 times.

Microcontroller Interface

In addition to its simplicity and ease of use, the ISD2500 series includes all the interfaces necessary for microcontroller-driven applications. The address and control lines can be interfaced to a microcontroller and manipulated to perform a variety of tasks, including message assembly, message concatenation, predefined fixed message segmentation, and message management.

Programming

The ISD2500 series is also ideal for playback-only applications, where single or multiple messages are referenced through buttons, switches, or a microcontroller. Once the desired message configuration is created, duplicates can easily be generated via a gang programmer.

7.2. OPERATIONAL MODES

The ISD2500 series is designed with several built-in Operational Modes that provide maximum functionality with minimum external components. These modes are described in details as below. The Operational Modes are accessed via the address pins and mapped beyond the normal message address range. When the two Most Significant Bits (MSB), A8 and A9, are HIGH, the remaining address signals are interpreted as mode bits and not as address bits. Therefore, Operational Modes and direct addressing are not compatible and cannot be used simultaneously.

There are two important considerations for using Operational Modes. First, all operations begin initially at address 0 of its memory. Later operations can begin at other address locations, depending on the Operational Mode(s) chosen. In addition, the address pointer is reset to 0 when the device is changed from record to playback, playback to record (except M6 mode), or when a Power-Down cycle is executed.

Second, Operational Modes are executed when $\overline{CE}$ goes LOW. This Operational Mode remains in effect until the next LOW-going CE signal, at which point the current mode(s) are sampled and executed.

TABLE 2: OPERATIONAL MODES

M0	Message cueing	Fast-forward through messages	M4, M5, M6
M1	Delete $\overline{EOM}$ markers	Position $\overline{EOM}$ marker at the end of the last message	M3, M4, M5, M6
M2	Not applicable	Reserved	N/A
M3	Looping	Continuous playback from Address 0	M1, M5, M6
M4	Consecutive addressing	Record/playback multiple consecutive messages	M0, M1, M5
M5	$\overline{CE}$ level-activated	Allows message pausing	M0, M1, M3, M4
M6	Push-button control	Simplified device interface	M0, M1, M3

(1) Besides mode pin needed to be "1", A8 and A9 pin are also required to be "1" in order to enter into the related operational mode.

(2) Indicates additional Operational Modes which can be used simultaneously with the given mode.

7.2.1. Operational Modes Description

The Operational Modes can be used in conjunction with a microcontroller, or they can be hardwired to provide the desired system operation.

M0 – Message Cueing

Message Cueing allows the user to skip through messages, without knowing the actual physical addresses of each message. Each $\overline{CE}$ LOW pulse causes the internal address pointer to skip to the next message. This mode is used for playback only, and is typically used with the M4 Operational Mode.

M1 – Delete $\overline{EOM}$ Markers

The M1 Operational Mode allows sequentially recorded messages to be combined into a single message with only one $\overline{EOM}$ marker set at the end of the final message. When this Operational Mode is configured, messages recorded sequentially are played back as one continuous message.

M2 – Unused

When Operational Modes are selected, the M2 pin should be LOW.

M3 – Message Looping

The M3 Operational Mode allows for the automatic, continuously repeated playback of the message located at the beginning of the address space. A message can completely fill the ISD2500 device and will loop from beginning to end without $\overline{OVF}$ going LOW.

M4 – Consecutive Addressing

During normal operation, the address pointer will reset when a message is played through an $\overline{EOM}$ marker. The M4 Operational Mode inhibits the address pointer reset on $\overline{EOM}$, allowing messages to be played back consecutively.

M5 - $\overline{CE}$-Level Activated

The default mode for ISD2500 devices is for $\overline{CE}$ to be edge-activated on playback and level-activated on record. The M5 Operational Mode causes the $\overline{CE}$ pin to be interpreted as level-activated as opposed to edge-activated during playback. This is especially useful for terminating playback operations using the $\overline{CE}$ signal. In this mode, $\overline{CE}$ LOW begins a playback cycle, at the beginning of the device memory. The playback cycle continues as long as $\overline{CE}$ is held LOW. When $\overline{CE}$ goes HIGH, playback will immediately end. A new $\overline{CE}$ LOW will restart the message from the beginning unless M4 is also HIGH.

M6 – Push-Button Mode

The ISD2500 series contain a Push-Button Operational Mode. The Push-Button Mode is used primarily in very low-cost applications and is designed to minimize external circuitry and components, thereby reducing system cost. In order to configure the device in Push-Button Operational Mode, the two most significant address bits must be HIGH, and the M6 mode pin must also be HIGH. A device in this mode always powers down at the end of each playback or record cycle after $\overline{CE}$ goes HIGH.

When this operational mode is implemented, three of the pins on the device have alternate functionality as described in the table below.

TABLE 3: ALTERNATE FUNCTIONALITY IN PINS

$\overline{CE}$	Start/Pause Push-Button (LOW pulse-activated)
PD	Stop/Reset Push-Button (HIGH pulse-activated)
$\overline{EOM}$	Active-HIGH Run Indicator

$\overline{CE}$ (START/PAUSE)

In Push-Button Operational Mode, $\overline{CE}$ acts as a LOW-going pulse-activated START/PAUSE signal. If no operation is currently in progress, a LOW-going pulse on this signal will initiate a playback or record cycle according to the level on the P/$\overline{R}$ pin. A subsequent pulse on the $\overline{CE}$ pin, before an $\overline{EOM}$ is reached in playback or an overflow condition occurs, will pause the current operation, and the address counter is not reset. Another $\overline{CE}$ pulse will cause the device to continue the operation from the place where it is paused.

PD (STOP/RESET)

In Push-Button Operational Mode, PD acts as a HIGH-going pulse-activated STOP/RESET signal. When a playback or record cycle is in progress and a HIGH-going pulse is observed on PD, the current cycle is terminated and the address pointer is reset to address 0, the beginning of the message space.

$\overline{EOM}$ (RUN)

In Push-Button Operational Mode, $\overline{EOM}$ becomes an active-HIGH RUN signal which can be used to drive an LED or other external device. It is HIGH whenever a record or playback operation is in progress.

Recording in Push-Button Mode

1. The PD pin should be LOW, usually using a pull-down resistor.

2. The P/R pin is taken LOW.
3. The $\overline{CE}$ pin is pulsed LOW. Recording starts, $\overline{EOM}$ goes HIGH to indicate an operation in progress.
4. When the $\overline{CE}$ pin is pulsed LOW. Recording pauses, $\overline{EOM}$ goes back LOW. The internal address pointers are not cleared, but the $\overline{EOM}$ marker is stored in memory to indicate as the message end. The P/R pin may be taken HIGH at this time. Any subsequent $\overline{CE}$ would start a playback at address 0.
5. The $\overline{CE}$ pin is pulsed LOW. Recording starts at the next address after the previous set $\overline{EOM}$ marker. $\overline{EOM}$ goes back HIGH.[3]
6. When the recording sequences are finished, the final $\overline{CE}$ pulse LOW will end the last record cycle, leaving a set $\overline{EOM}$ marker at the message end. Recording may also be terminated by a HIGH level on PD, which will leave a set $\overline{EOM}$ marker.

Playback in Push-Button Mode

1. The PD pin should be LOW.
2. The $\overline{P/R}$ pin is taken HIGH.
3. The $\overline{CE}$ pin is pulsed LOW. Playback starts, $\overline{EOM}$ goes HIGH to indicate an operation in progress.
4. If the $\overline{CE}$ pin is pulsed LOW or an $\overline{EOM}$ marker is encountered during an operation, the part will pause. The internal address pointers are not cleared, and $\overline{EOM}$ goes back LOW. The $\overline{P/R}$ pin may be changed at this time. A subsequent record operation would not reset the address pointers and the recording would begin where playback ended.
5. $\overline{CE}$ is again pulsed LOW. Playback starts where it left off, with $\overline{EOM}$ going HIGH to indicate an operation in progress.
6. Playback continues as in steps 4 and 5 until PD is pulsed HIGH or overflow occurs.
7. If in overflow, pulling $\overline{CE}$ LOW will reset the address pointer and start playback from the beginning. After a PD pulse, the part is reset to address 0.

Note: Push-Button Mode can be used in conjunction with modes M0, M1, and M3.

[3] If the M1 Operational Mode pin is also HIGH, the just previously written $\overline{EOM}$ bit is erased, and recording starts at that address.

Good Audio Design Practices

Winbond products are very high-quality single-chip voice recording and playback systems. To ensure the highest quality voice reproduction, it is important that good audio design practices on layout and power supply decoupling be followed. See Application Information or below links for details.

Good Audio Design Practices

http://www.winbond-usa.com/products/isd_products/chipcorder/applicationinfo/apin11.pdf

Single-Chip Board Laycut Diagrams

http://www.winbond-usa.com/products/isd_products/chipcorder/applicationinfo/apin12.pdf

8. TIMING DIAGRAMS

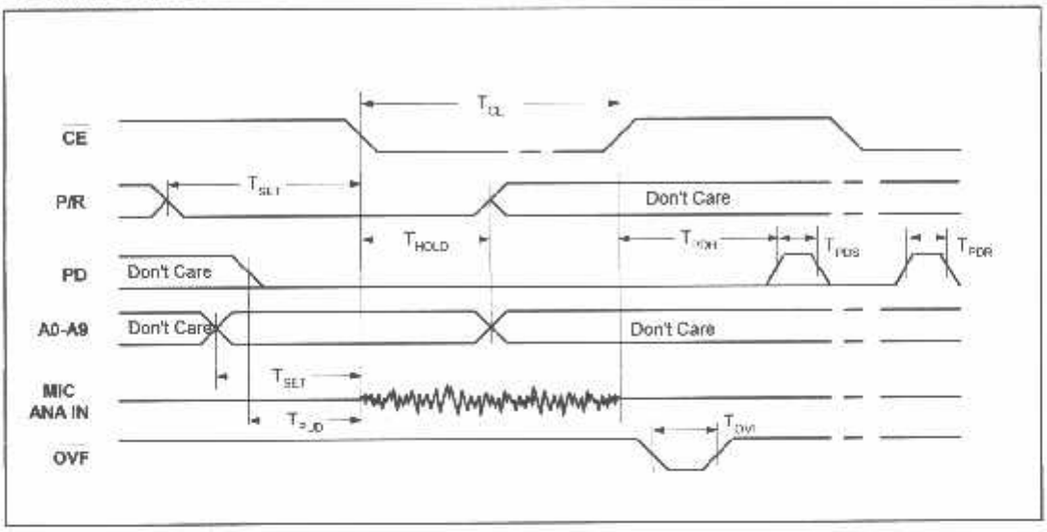


FIGURE 1: RECORD

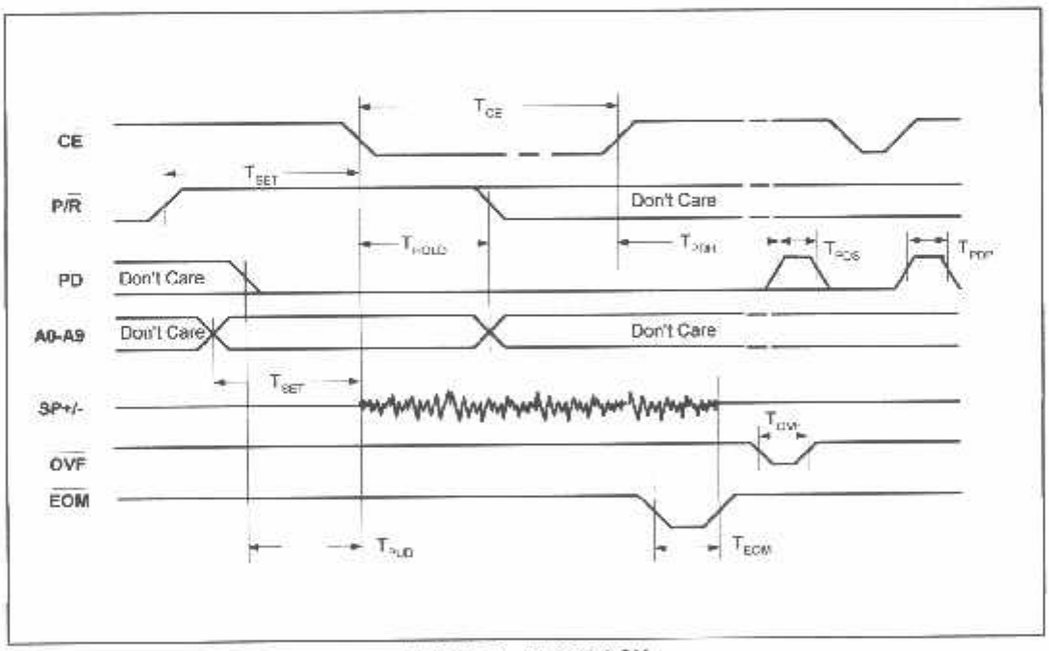


FIGURE 2: PLAYBACK

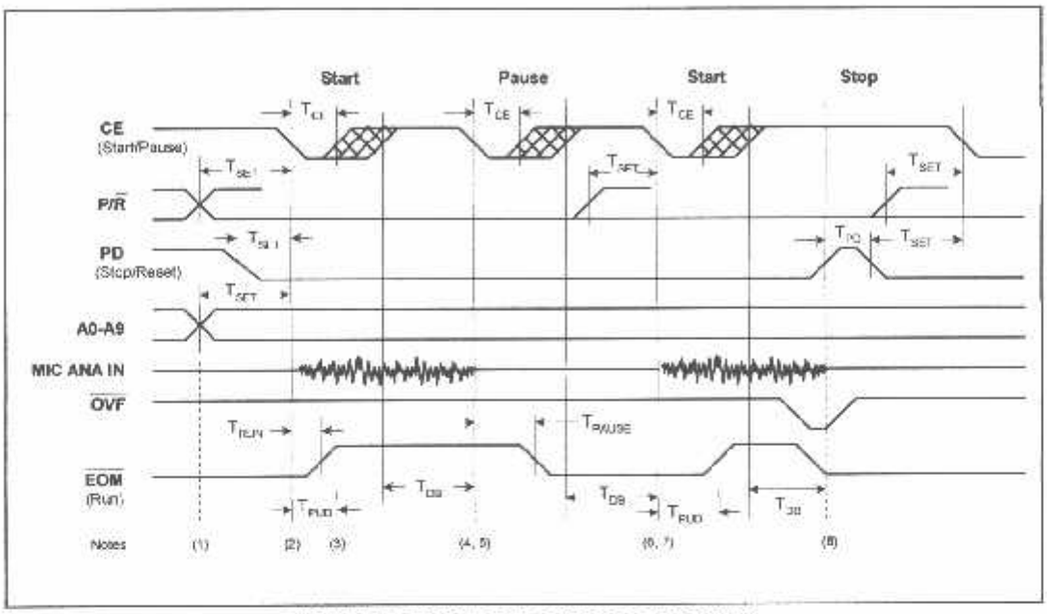


FIGURE 3: PUSH-BUTTON MODE RECORD

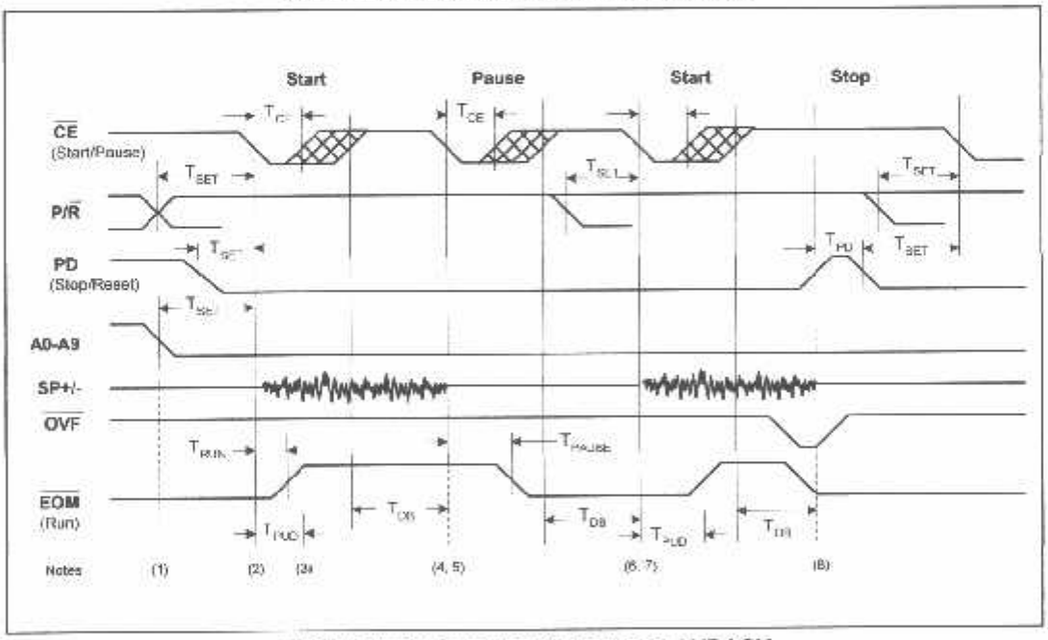


FIGURE 4: PUSH-BUTTON MODE PLAYBACK

Notes for Push-Button modes:

1. A9, A8, and A6 = 1 for push-button operation.
2. The first $\overline{CE}$ LOW pulse performs a start function.
3. The part will begin to play or record after a power-up delay T_{PUD}.
4. The part must have $\overline{CE}$ HIGH for a debounce period T_{DB} before it will recognize another falling edge of $\overline{CE}$ and pause.
5. The second $\overline{CE}$ LOW pulse, and every even pulse thereafter, performs a Pause function.
6. Again, the part must have $\overline{CE}$ HIGH for a debounce period T_{DB} before it will recognize another falling edge of $\overline{CE}$, which would restart an operation. In addition, the part will not do an internal power down until $\overline{CE}$ is HIGH for the T_{CE} time.
7. The third $\overline{CE}$ LOW pulse, and every odd pulse thereafter, performs a Resume function.
8. At any time, a HIGH level on PD will stop the current function, reset the address counter, and power down the device.

9. ABSOLUTE MAXIMUM RATINGS

TABLE 4: ABSOLUTE MAXIMUM RATINGS (DIE)

Junction temperature	150°C
Storage temperature range	-65°C to +150°C
Voltage applied to any pad	(V_{SS} –0.3V) to (V_{CC} +0.3V)
Voltage applied to any pad (Input current limited to +20mA)	(V_{SS} –1.0V) to (V_{CC} +1.0V)
V_{CC} – V_{SS}	-0.3V to +7.0V

TABLE 5: ABSOLUTE MAXIMUM RATINGS (PACKAGED PARTS)

Junction temperature	150°C
Storage temperature range	-65°C to +150°C
Voltage applied to any pin	(V_{SS} –0.3V) to (V_{CC} +0.3V)
Voltage applied to any pin (Input current limited to ±20 mA)	(V_{SS} –1.0V) to (V_{CC} +1.0V)
Lead temperature (Soldering – 10sec)	300°C
V_{CC} – V_{SS}	-0.3V to +7.0V

Note: Stresses above those listed may cause permanent damage to the device. Exposure to the absolute maximum ratings may affect device reliability and performance. Functional operation is not implied at these conditions.

9.1 OPERATING CONDITIONS

TABLE 6: OPERATING CONDITIONS (DIE)

Commercial operating temperature range	0°C to +50°C
Supply voltage (V_{CC}) [1]	+4.5V to +6.5V
Ground voltage (V_{SS}) [2]	0V

TABLE 7: OPERATING CONDITIONS (PACKAGED PARTS)

Commercial operating temperature range [3]	0°C to +70°C
Supply voltage (V_{CC}) [1]	+4.5V to +5.5V
Ground voltage (V_{SS}) [2]	0V

[1] $V_{CC} = V_{CCA} = V_{CCD}$

[2] $V_{SS} = V_{SSA} = V_{SSD}$

[3] Case Temperature

10. ELECTRICAL CHARACTERISTICS

10.1. PARAMETERS FOR PACKAGED PARTS

TABLE 8: DC PARAMETERS – Packaged Parts

Input Low Voltage	V_{IL}			0.8	V	
Input High Voltage	V_{IH}	2.0			V	
Output Low Voltage	V_{OL}			0.4	V	I_{OL} = 4.0 mA
Output High Voltage	V_{OH}	V_{CC} - 0.4			V	I_{OH} = -10 µA
$\overline{OVF}$ Output High Voltage	V_{OH1}	2.4			V	I_{OH1} = -1.6 mA
$\overline{EOM}$ Output High Voltage	V_{OH2}	V_{CC} – 1.0	V_{CC} - 0.8		V	I_{OH} = -3.2 mA
V_{CC} Current (Operating)	I_{CC}		25	30	mA	R_{EXT} = ∞ [3]
V_{CC} Current (Standby)	I_{SB}		1	10	µA	[3]
Input Leakage Current	I_{IL}			±1	µA	
Input Current HIGH w/Pull Down	I_{ILPD}			130	µA	Force V_{CC} [4]
Output Load Impedance	R_{EXT}	16			Ω	Speaker Load
Preamp Input Resistance	R_{MIC}	4	9	15	KΩ	MIC and MIC REF Pins
AUX IN Input Resistance	R_{AUX}	5	11	20	KΩ	
ANA IN Input Resistance	$R_{ANA\ IN}$	2.3	3	5	KΩ	
Preamp Gain 1	A_{PRE1}	21	24	26	dB	AGC = 0.0V
Preamp Gain 2	A_{PRE2}		-15	5	dB	AGC = 2.5V
AUX IN/SP+ Gain	A_{AUX}		0.98	1.0	V/V	
ANA IN to SP+/- Gain	A_{ARP}	21	23	26	dB	
AGC Output Resistance	R_{AGC}	2.5	5	9.5	KΩ	

Notes:

[1] Typical values @ T_A = 25° and V_{CC} = 5.0V.

[2] All Min/Max limits are guaranteed by Winbond via electrical testing or characterization. Not all specifications are 100 percent tested.

[3] V_{CCA} and V_{CCD} connected together.

[4] XCLK pin only.

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TABLE 9: AC PARAMETERS – Packaged Parts

Sampling Frequency	F_S					
ISD2560			8.0		kHz	[7]
ISD2575			6.4		kHz	[7]
ISD2590			5.3		kHz	[7]
ISD25120			4.0		kHz	[7]
Filter Pass Band	F_{CF}					
ISD2560			3.4		kHz	3 dB Roll-Off Point[3][8]
ISD2575			2.7		kHz	3 dB Roll-Off Point[3][8]
ISD2590			2.3		kHz	3 dB Roll-Off Point[3][8]
ISD25120			1.7		kHz	3 dB Roll-Off Point[3][8]
Record Duration	T_{REC}					
ISD2560		58.1	60.0	62.0	sec	Commercial Operation[7]
ISD2575		72.6	75.0	77.5	sec	Commercial Operation[7]
ISD2590		87.1	90.0	93.0	sec	Commercial Operation[7]
ISD25120		116.1	120.0	123.9	sec	Commercial Operation[7]
Playback Duration	T_{PLAY}					
ISD2560		58.1	60.0	62.0	sec	Commercial Operation
ISD2575		72.6	75.0	77.5	sec	Commercial Operation
ISD2590		87.1	90.0	93.0	sec	Commercial Operation
ISD25120		116.1	120.0	123.9	sec	Commercial Operation
$\overline{CE}$ Pulse Width	T_{CC}		100		nsec	
Control/Address Setup Time	T_{SET}		300		nsec	
Control/Address Hold Time	T_{HCLD}		0		nsec	
Power-Up Delay	T_{PUD}					
ISD2560		24.1	25.0	27.8	msec	Commercial Operation
ISD2575		30.2	31.3	34.3	msec	Commercial Operation
ISD2590		36.2	37.5	40.8	msec	Commercial Operation
ISD25120		48.2	50.0	53.6	msec	Commercial Operation
PD Pulse Width (record)	T_{PCR}					
ISD2560			25.0		msec	
ISD2575			31.25		msec	
ISD2590			37.5		msec	
ISD25120			50.0		msec	

TABLE 9: AC PARAMETERS – Packaged Parts (Cont'd)

PD Pulse Width (Play)	T_{PDP}					
ISD2560			12.5		msec	
ISD2575			15.625		msec	
ISD2590			18.75		msec	
ISD25120			25.0		msec	
PD Pulse Width (Static)	T_{PDS}		100		nsec	[6]
Power Down Hold	T_{PDH}		0		nsec	
$\overline{EOM}$ Pulse Width	T_{EOM}					
ISD2560			12.5		msec	
ISD2575			15.625		msec	
ISD2590			18.75		msec	
ISD25120			25.0		msec	
Overflow Pulse Width	T_{OVF}		6.5		µsec	
Total Harmonic Distortion	THD		1	2	%	@ 1 kHz
Speaker Output Power	P_{OUT}		12.2	50	mW	R_{EXT} = 16 Ω[4]
Voltage Across Speaker Pins	V_{OUT}			2.5	V p-p	R_{EXT} = 600 Ω
MIC Input Voltage	V_{IN1}			20	mV	Peak-to-Peak[5]
ANA IN Input Voltage	V_{IN2}			50	mV	Peak-to-Peak
AUX Input Voltage	V_{IN3}			1.25	V	Peak-to-Peak; R_{EXT} = 16 Ω

Notes:

[1] Typical values @ T_A = 25°C and V_{CC} = 5.0V.

[2] All Min/Max limits are guaranteed by Winbond via electrical testing or characterization. Not all specifications are 100 percent tested.

[3] Low-frequency cutoff depends upon the value of external capacitors (see Pin Descriptions).

[4] From AUX IN; if ANA IN is driven at 50 mV p-p, the P_{OUT} = 12.2 mW, typical.

[5] With 5.1 K Ω series resistor at ANA IN.

[6] T_{PDS} is required during a static condition, typically overflow.

[7] Sampling Frequency and playback Duration can vary as much as ±2.25 percent over the commercial temperature range. For greater stability, an external clock can be utilized (see Pin Descriptions).

[8] Filter specification applies to the antialiasing filter and the smoothing filter. Therefore, from input to output, expect a 6 dB drop by nature of passing through both filters.

10.1.1. Typical Parameter Variation with Voltage and Temperature (Packaged Parts)

Chart 1: Record Mode Operating Current (I_{CC})

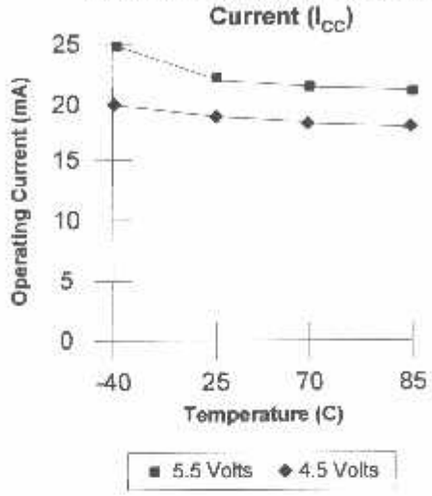


Chart 3: Standby Current (I_{SB})

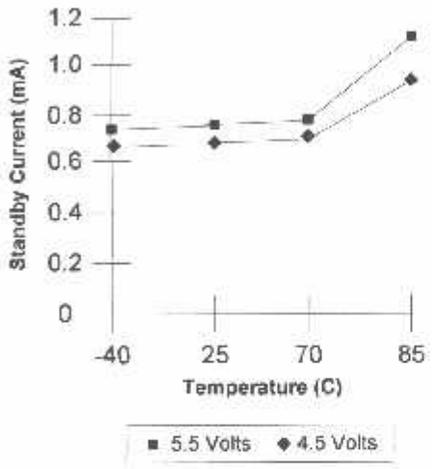


Chart 2: Total Harmonic Distortion

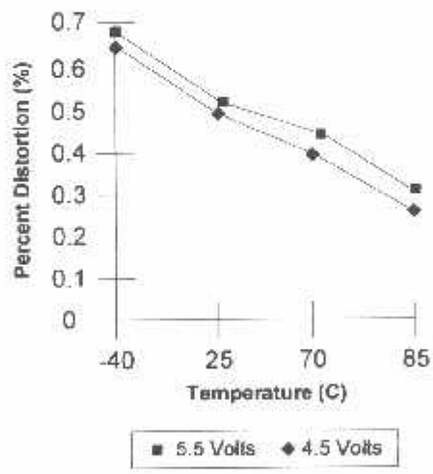
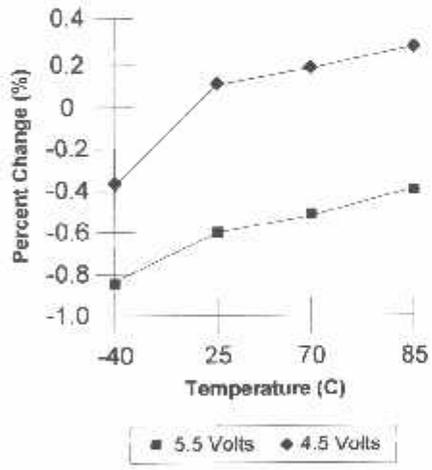


Chart 4: Oscillator Stability



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10.2. PARAMETERS FOR DIE

TABLE 10: DC PARAMETERS – Die

Input Low Voltage	V_{IL}			0.8	V	
Input High Voltage	V_{IH}	2.0			V	
Output Low Voltage	V_{OL}			0.4	V	I_{OL} = 4.0 mA
Output High Voltage	V_{OH}	V_{CC} - 0.4			V	I_{OH} = -10 µA
$\overline{OVF}$ Output High Voltage	V_{OH1}	2.4			V	I_{OH} = -1.6 mA
$\overline{EOM}$ Output High Voltage	V_{OH2}	V_{CC} – 1.0	V_{CC} - 0.8		V	I_{OH} = -3.2 mA
V_{CC} Current (Operating)	I_{CC}		25	30	mA	R_{EX}- = ∞ [3]
V_{CC} Current (Standby)	I_{SB}		1	10	µA	[2]
Input Leakage Current	I_{IL}			±1	µA	
Input Current HIGH w/Pull Down	I_{ILPD}			130	µA	Force V_{CC} [4]
Output Load Impedance	R_{EXT}	16			Ω	Speaker Load
Preamp IN Input Resistance	R_{MIC}	4	9	15	KΩ	MIC and MIC REF Pads
AUX IN Input Resistance	R_{AUX}	5	11	20	KΩ	
ANA IN Input Resistance	$R_{ANA\ IN}$	2.3	3	5	KΩ	
Preamp Gain 1	A_{PRE1}	21	24	26	dB	AGC = 0.0V
Preamp Gain 2	A_{PRE2}		-15	5	dB	AGC = 2.5V
AUX IN/SP+ Gain	A_{AUX}		0.98	1.0	V/V	
ANA IN to SP+/- Gain	A_{ARP}	21	23	26	dB	
AGC Output Resistance	R_{AGC}	2.5	5	9.5	KΩ	

Notes

[1] Typical values @ T_a = 25°C and V_{CC} = 5.0V.

[2] All Min/Max limits are guaranteed by Winbond via electrical testing or characterization. Not all specifications are 100 percent tested.

[3] V_{CCA} and V_{CCD} connected together

[4] XCLK pad only.

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TABLE 11: AC PARAMETERS – Die

Sampling Frequency	F_S					
ISD2560			8.0		kHz	[7]
ISD2575			6.4		kHz	[7]
ISD2590			5.3		kHz	[7]
ISD25120			4.0		kHz	[7]
Filter Pass Band	F_{CF}					
ISD2560			3.4		kHz	3 dB Roll-Off Point[3][8]
ISD2575			2.7		kHz	3 dB Roll-Off Point[3][8]
ISD2590			2.3		kHz	3 dB Roll-Off Point[3][8]
ISD25120			1.7		kHz	3 dB Roll-Off Point[3][8]
Record Duration	T_{REC}					
ISD2560		58.1	60.0	62.0	sec	Commercial Operation[7]
ISD2575		72.6	75.0	77.5	sec	Commercial Operation[7]
ISD2590		87.1	90.0	93.0	sec	Commercial Operation[7]
ISD25120		116.1	120.0	123.9	sec	Commercial Operation[7]
Playback Duration	T_{PLAY}					
ISD2560		58.1	60.0	62.0	sec	Commercial Operation[7]
ISD2575		72.6	75.0	77.5	sec	Commercial Operation[7]
ISD2590		87.1	90.0	93.0	sec	Commercial Operation[7]
ISD25120		116.1	120.0	123.9	sec	Commercial Operation[7]
$\overline{CE}$ Pulse Width	T_{CE}		100		nsec	
Control/Address Setup Time	T_{SET}		300		nsec	
Control/Address Hold Time	T_{HOLD}		0		nsec	
Power-Up Delay	T_{PUD}					
ISD2560		24.1	25.0	27.8	msec	Commercial Operation
ISD2575		30.2	31.3	34.3	msec	Commercial Operation
ISD2590		36.2	37.5	40.8	msec	Commercial Operation
ISD25120		48.2	50.0	53.6	msec	Commercial Operation
PD Pulse Width (Record)	T_{PDR}					
ISD2560			25.0		msec	
ISD2575			31.25		msec	
ISD2590			37.5		msec	
ISD25120			50.0		msec	

TABLE 11: AC PARAMETERS – Die (Cont'd)

PD Pulse Width (Play) ISD2560 ISD2575 ISD2590 ISD25120	T_{PDP}		 12.5 15.625 18.75 25.0		 msec msec msec msec	
PD Pulse Width (Static)	T_{PDS}		100		nsec	[6]
Power Down Hold	T_{PDH}		0		nsec	
$\overline{EOM}$ Pulse Width ISD2560 ISD2575 ISD2590 ISD25120	T_{EOM}		 12.5 15.625 18.75 25.0		 msec msec msec msec	
Overflow Pulse Width	T_{OVF}		6.5		µsec	
Total Harmonic Distortion	THD		1	3	%	@ 1 kHz
Speaker Output Power	P_{OUT}		12.2	50	mW	R_{EXT} = 16 Ω[4]
Voltage Across Speaker Pins	V_{OUT}			2.5	V p-p	R_{EXT} = 600 Ω
MIC Input Voltage	V_{IN1}			20	mV	Peak-to-Peak[5]
ANA IN Input Voltage	V_{IN2}			50	mV	Peak-to-Peak
AUX Input Voltage	V_{IN3}			1.25	V	Peak-to-Peak; R_{EXT} = 16 Ω

Notes:

[1] Typical values @ T_A = 25°C and V_{CC} = 5.0V.

[2] All Min/Max limits are guaranteed by Winbond via electrical testing or characterization. Not all specifications are 100 percent tested.

[3] Low-frequency cutoff depends upon the value of external capacitors (see Pin Descriptions).

[4] From AUX IN; if ANA IN is driven at 50 mV p-p, the P_{OUT} = 12.2 mW, typical.

[5] With 5.1 K Ω series resistor at ANA IN.

[6] T_{PDS} is required during a static condition, typically overflow.

[7] Sampling Frequency and playback Duration can vary as much as ±2.25 percent over the commercial temperature range. For greater stability, an external clock can be utilized (see Pin Descriptions).

[8] Filter specification applies to the antialiasing filter and the smoothing filter. Therefore, from input to output, expect a 6 dB drop by nature of passing through both filters.

10.2.1. Typical Parameter Variation with Voltage and Temperature (Die)

Chart 5: Record Mode Operating Current (I_{CC})

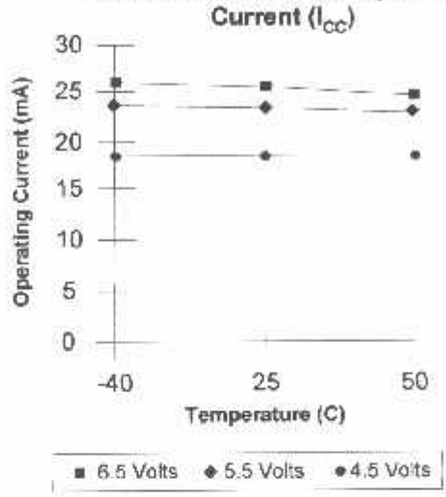


Chart 7: Standby Current (I_{SB})

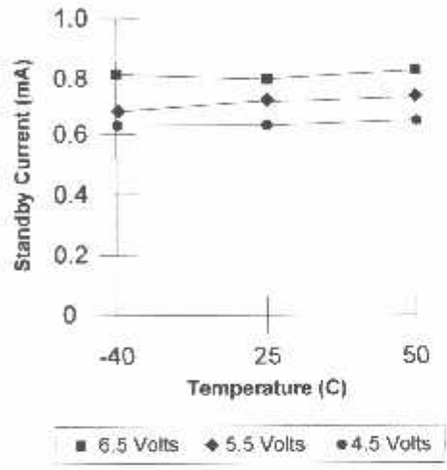


Chart 6: Total Harmonic Distortion

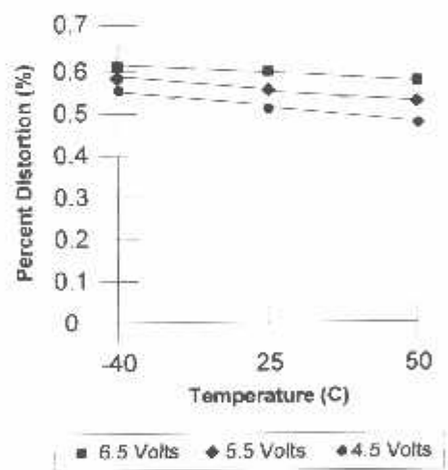
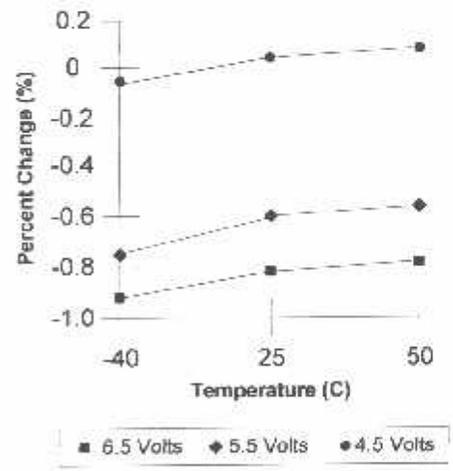


Chart 8: Oscillator Stability



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10.3. PARAMETERS FOR PUSH-BUTTON MODE

TABLE 12: PARAMETERS FOR PUSH-BUTTON MODE

$\overline{CE}$ Pulse Width (Start/Pause)	T_{CE}		300		nsec	
Control/Address Setup Time	T_{SET}		300		nsec	
Power-Up Delay	T_{PUD}					
ISD2560			25.0		msec	
ISD2575			31.25		msec	
ISD2590			37.25		msec	
ISD25120			50.0		msec	
PD Pulse Width (Stop/Restart)	T_{PD}		300		nsec	
$\overline{CE}$ to $\overline{EOM}$ HIGH	T_{RUN}	25		400	nsec	
$\overline{CE}$ to $\overline{EOM}$ LOW	T_{PAUSE}	50		400	nsec	
$\overline{CE}$ HIGH Debounce	T_{DB}					
ISD2560		70		105	msec	
ISD2575		85		135	msec	
ISD2590		105		160	msec	
ISD25120		135		215	msec	

Notes:

(1) Typical values @ T_A = 25°C and V_{CC} = 5.0V.

(2) All Min/Max limits are guaranteed by Winbond via electrical testing or characterization. Not all specifications are 100 percent tested.

11. TYPICAL APPLICATION CIRCUIT

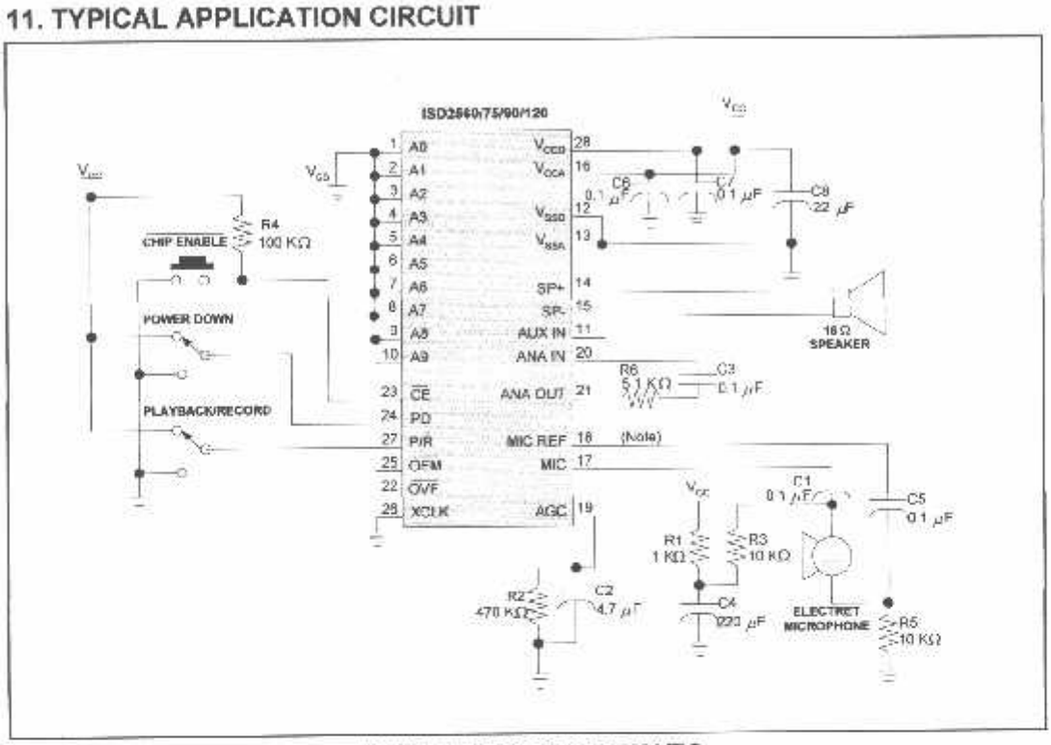


FIGURE 5: DESIGN SCHEMATIC

Note: If desired, pin 18 (PDIP package) may be left unconnected (microphone preamplifier noise will be higher). In this case, pin 18 must not be tied to any other signal or voltage. Additional design example schematics are provided below.

TABLE 13: APPLICATION EXAMPLE – BASIC DEVICE CONTROL

1	Power up chip and select Record/Playback Mode	1. PD = LOW, 2. P/$\overline{R}$ = As desired
2	Set message address for record/playback	Set addresses A0-A9
3A	Begin playback	P/$\overline{R}$ = HIGH, $\overline{CE}$ = Pulse LOW
3B	Begin record	P/$\overline{R}$ = LOW, $\overline{CE}$ = LOW
4A	End playback	Automatic
4B	End record	PD or $\overline{CE}$ = HIGH

TABLE 14: APPLICATION EXAMPLE – PASSIVE COMPONENT FUNCTIONS

R1	Microphone power supply decoupling	Reduces power supply noise
R2	Release time constant	Sets release time for AGC
R3, R5	Microphone biasing resistors	Provides biasing for microphone operation
R4	Series limiting resistor	Reduces level to prevent distortion at higher supply voltages
R6	Series limiting resistor	Reduces level to high supply voltages
C1, C5	Microphone DC-blocking capacitor Low-frequency cutoff	Decouples microphone bias from chip. Provides single-pole low-frequency cutoff and command mode noise rejection.
C2	Attack/Release time constant	Sets attack/release time for AGC
C3	Low-frequency cutoff capacitor	Provides additional pole for low-frequency cutoff
C4	Microphone power supply decoupling	Reduces power supply noise
C6, C7, C8	Power supply capacitors	Filter and bypass of power supply

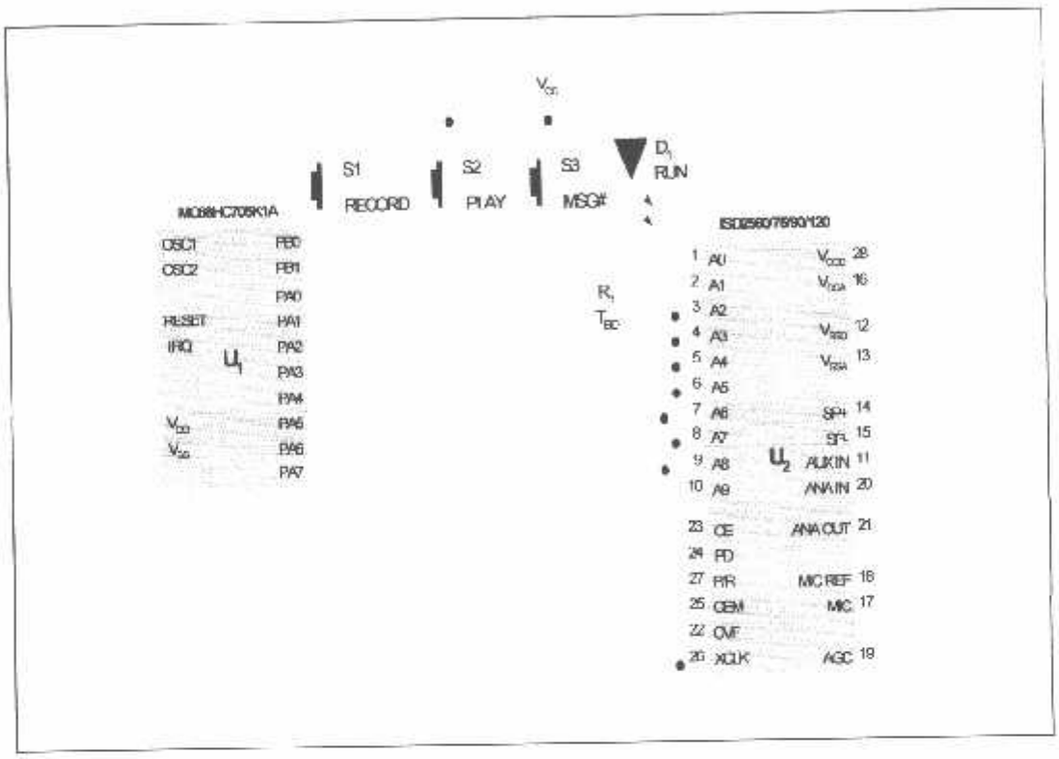


FIGURE 6: ISD2560/75/90/120 APPLICATION EXAMPLE – MICROCONTROLLER/ISD2500 INTERFACE

In this simplified block diagram of a microcontroller application, the Push-Button Mode and message cueing are used. The microcontroller is a 16-pin version with enough port pins for buttons, an LED, and the ISD2500 series device. The software can be written to use three buttons: one each for play and record, and one for message selection. Because the microcontroller is interpreting the buttons and commanding the ISD2500 device, software can be written for any function desired in a particular application.

Note: Winbond does not recommend connecting address lines directly to a microprocessor bus. Address lines should be externally latched.

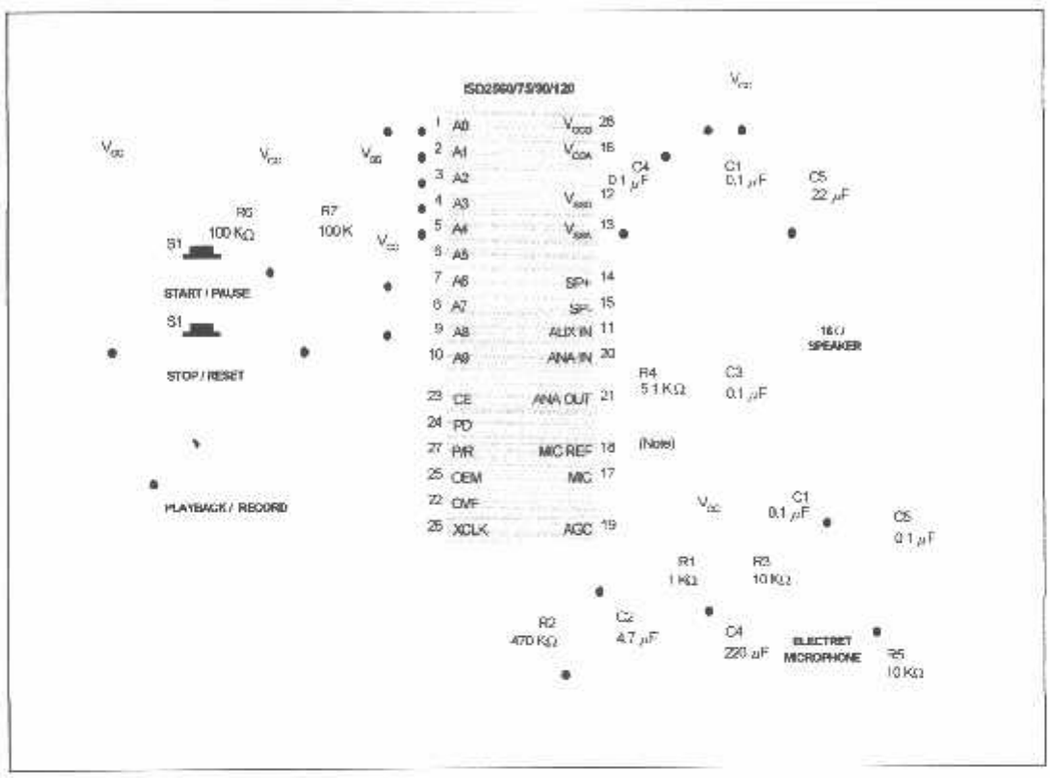


FIGURE 7: ISD2560/75/90/120 APPLICATION EXAMPLE – PUSH-BUTTON

Note: Please refer to page 13 for more details.

TABLE 15: APPLICATION EXAMPLE – PUSH-BUTTON CONTROL

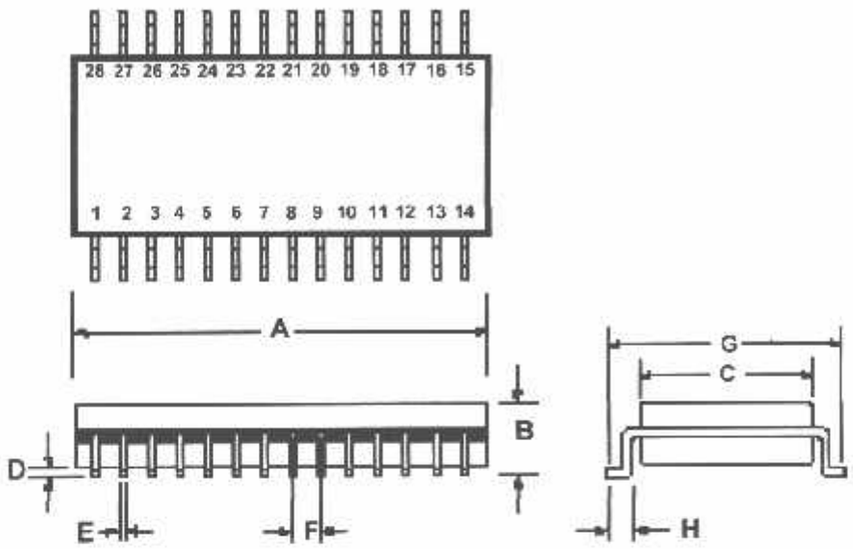
1	Select Record/Playback Mode	P/$\overline{R}$ = As desired
2A	Begin playback	P/$\overline{R}$ = HIGH, $\overline{CE}$ = Pulse LOW
2B	Begin record	P/$\overline{R}$ = LOW, $\overline{CE}$ = Pulse LOW
3	Pause record or playback	$\overline{CE}$ = Pulsed LOW
4A	End playback	Automatic at $\overline{EOM}$ marker or PD = Pulsed HIGH
4B	End record	PD = Pulsed HIGH

TABLE 16: APPLICATION EXAMPLE – PASSIVE COMPONENT FUNCTIONS

R2	Release time constant	Sets release time for AGC
R4	Series limiting resistor	Reduces level to prevent distortion at higher supply voltages
R6, R7	Pull-up and pull-down resistors	Defines static state of inputs
C1, C4, C5	Power supply capacitors	Filters and bypass of power supply
C2	Attack/Release time constant	Sets attack/release time for AGC
C3	Low-frequency cutoff capacitor	Provides additional pole for low-frequency cutoff

12. PACKAGE DRAWING AND DIMENSIONS

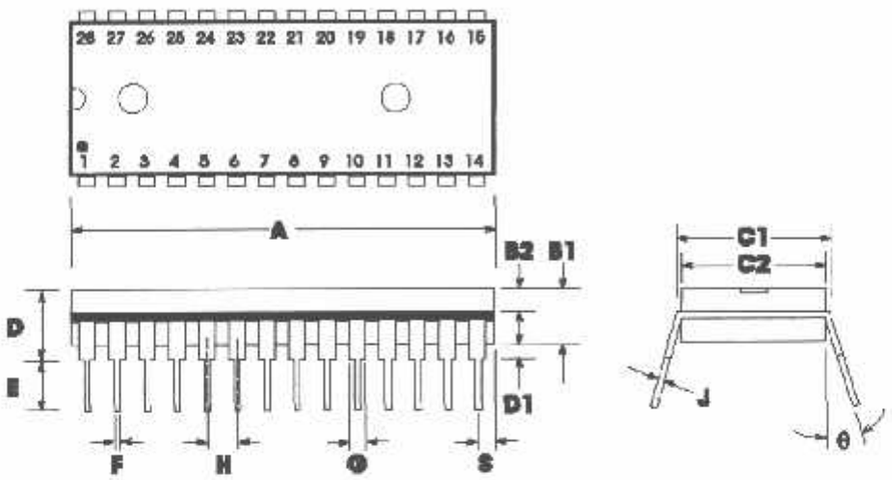
12.1. 28-LEAD 300-MIL PLASTIC SMALL OUTLINE IC (SOIC)



A	0.701	0.706	0.711	17.81	17.93	18.06
B	0.097	0.101	0.104	2.46	2.56	2.64
C	0.292	0.296	0.299	7.42	7.52	7.59
D	0.005	0.009	0.0115	0.127	0.22	0.29
E	0.014	0.016	0.019	0.35	0.41	0.48
F		0.050			1.27	
G	0.400	0.406	0.410	10.16	10.31	10.41
H	0.024	0.032	0.040	0.61	0.81	1.02

Note: Lead coplanarity to be within 0.004 inches.

12.2. 28-LEAD 600-MIL PLASTIC DUAL INLINE PACKAGE (PDIP)



A	1.445	1.450	1.455	36.70	36.83	36.96
B1		0.150			3.81	
B2	0.065	0.070	0.075	1.65	1.78	1.91
C1	0.600		0.625	15.24		15.88
C2	0.530	0.540	0.550	13.46	13.72	13.97
D			0.19			4.83
D1	0.015			0.38		
E	0.125		0.135	3.18		3.43
F	0.015	0.018	0.022	0.38	0.46	0.56
G	0.055	0.060	0.065	1.40	1.52	1.62
H		0.100			2.54	
J	0.008	0.010	0.012	0.20	0.25	0.30
S	0.070	0.075	0.080	1.78	1.91	2.03
q	0°		15°	0°		15°

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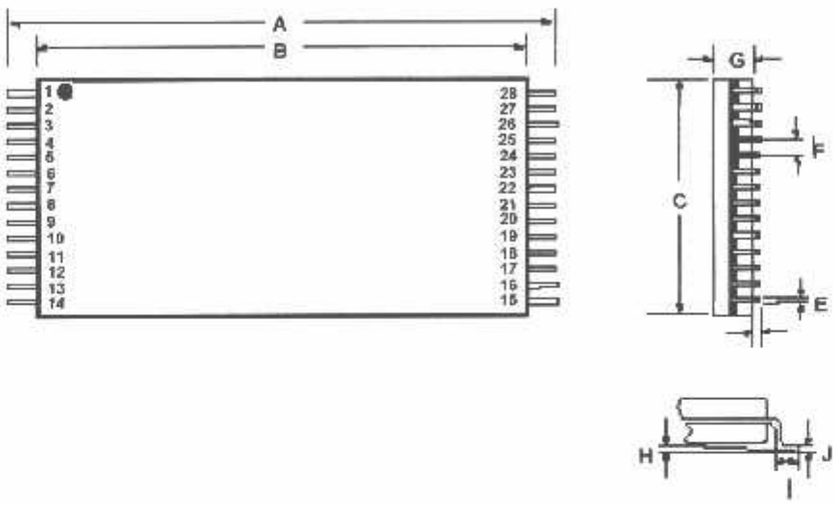
12.3. 28-LEAD 8X13.4MM PLASTIC THIN SMALL OUTLINE PACKAGE (TSOP) TYPE 1



Plastic Thin Small Outline Package (TSOP) Type 1 Dimensions

A	0.520	0.528	0.535	13.20	13.40	13.60
B	0.461	0.465	0.469	11.70	11.80	11.90
C	0.311	0.315	0.319	7.90	8.00	8.10
D	0.002		0.006	0.05		0.15
E	0.007	0.009	0.011	0.17	0.22	0.27
F		0.0217			0.55	
G	0.037	0.039	0.041	0.95	1.00	1.05
H	0^0	3^0	6^0	0^0	3^0	6^0
I	0.020	0.022	0.028	0.50	0.55	0.70
J	0.004		0.008	0.10		0.21

Note: *Lead coplanarity to be within 0.004 inches.*

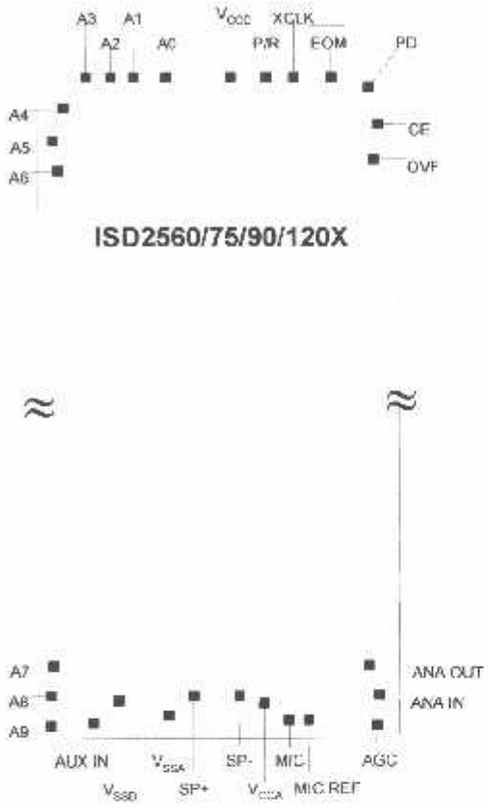
12.4. ISD2560/75/95/120 Product Bonding Physical Layout (Die) [1]

ISD2560/75/95/120

- Die Dimensions
  X: 149.5 ± 1 mils
  Y: 262.0 ± 1 mils

- Die Thickness [2]
  11.8 ± .4 mils

- Pad Opening
  111 x 111 microns
  4.4 x 4.4 mils



ISD2560/75/90/120X

Notes:

[1] The backside of die is internally connected to V_{SS}. It **MUST NOT** be connected to any other potential or damage may occur.

[2] Die thickness is subject to change, please contact Winbond factory for status and availability.

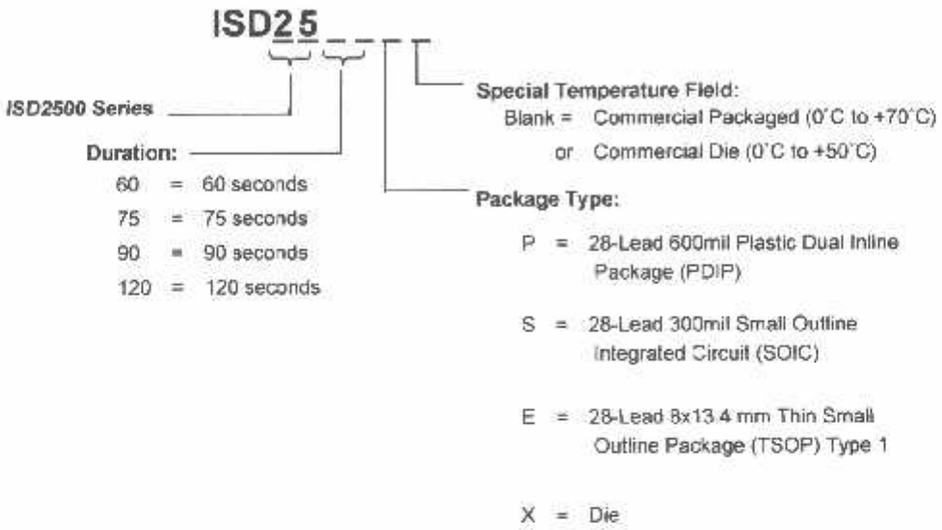
ISD2560/75/90/120 PRODUCT PAD DESIGNATIONS

(with respect to die center)

A0	Address 0	-897.9	3135.2
A1	Address 1	-1115.4	3135.2
A2	Address 2	-1331.0	3135.2
A3	Address 3	-1544.0	3135.2
A4	Address 4	-1640.4	2888.9
A5	Address 5	-1698.2	2671.0
A6	Address 6	-1698.2	2441.5
A7	Address 7	-1731.2	-2583.2
A8	Address 8	-1731.2	-2768.4
A9	Address 9	-1731.2	-3050.8
AUX IN	Auxiliary Input	-1410.2	-3115.7
V_{SSD}	V_{SS} Digital Power Supply	-1112.4	-3096.5
V_{SSA}	V_{SS} Analog Power Supply	-408.2	-3138.9
SP+	Speaker Output +	-46.65	-3068.4
SP-	Speaker Output -	386.1	-3068.4
V_{CCA}	V_{CC} Analog Power Supply	746.9	-3110.8
MIC	Microphone Input	1101.2	-3146.0
MIC REF	Microphone Reference	1294.7	-3146.0
AGC	Automatic Gain Control	1666.4	-3130.3
ANA IN	Analog Input	1728.6	-2654.0
ANA OUT	Analog Output	1700.9	-2411.0
$\overline{OVF}$	Overflow Output	1674.6	2489.5
$\overline{CE}$	Chip Enable Input	1726.7	2824.4
PD	Power Down Input	1730.5	3094.0
$\overline{EOM}$	End of Message	1341.2	3122.1
XCLK	No Connect (optional)	986.5	3160.7
$P/\overline{R}$	Playback/Record	807.2	3163.4
V_{CCD}	V_{CC} Digital Power Supply	544.4	3159.6

13. ORDERING INFORMATION

Product Number Descriptor Key



When ordering ISD2560/75/90/120 products refer to the following part numbers which are supported in volume for this product series. Consult the local Winbond Sales Representative or Distributor for availability information.

ISD2560P	ISD2575P	ISD2590P	ISD25120P
ISD2560S	ISD2575S	ISD2590S	ISD25120S
ISD2560E	ISD2575E	ISD2590E	
ISD2560X	ISD2575X	ISD2590X	ISD25120X

For the latest product information, access Winbond's worldwide website at http://www.winbond-usa.com

14. VERSION HISTORY

VERSION	DATE	PAGE	DESCRIPTION
0	Apr. 1998	All	Preliminary Specifications
1.0	May 2003	All	Re-format the document. Update TSOP pin configuration. Revise Overflow pad designation.

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National Semiconductor

July 1993

MM54C922/MM74C922 16-Key Encoder
MM54C923/MM74C923 20-Key Encoder

General Description

These CMOS key encoders provide all the necessary logic to fully encode an array of SPST switches. The keyboard scan can be implemented by either an external clock or external capacitor. These encoders also have on-chip pull-up devices which permit switches with up to 50 kΩ on resistance to be used. No diodes in the switch array are needed to eliminate ghost switches. The internal debounce circuit needs only a single external capacitor and can be defeated by omitting the capacitor. A Data Available output goes to a high level when a valid keyboard entry has been made. The Data Available output returns to a low level when the entered key is released, even if another key is depressed. The Data Available will return high to indicate acceptance of the new key after a normal debounce period; this two-key rollover is provided between any two switches.

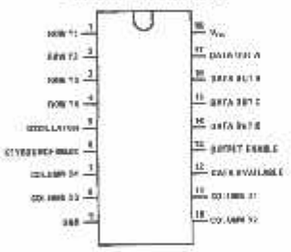
An internal register remembers the last key pressed even after the key is released. The TRI-STATE® outputs provide for easy expansion and bus operation and are LPTTL compatible.

Features

- 50 kΩ maximum switch on resistance
- On or off chip clock
- On-chip row pull-up devices
- 2 key roll-over
- Keybounce elimination with single capacitor
- Last key register at outputs
- TRI-STATE output LPTTL compatible
- Wide supply range 3V to 15V
- Low power consumption

Connection Diagrams

Pin Assignment for Dual-In-Line Package

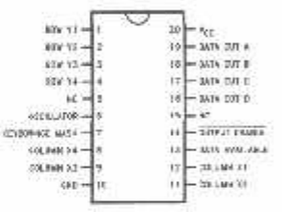


TL/F/6037–1

Top View

Order Number MM54C922 or MM74C922

Pin Assignment for SOIC

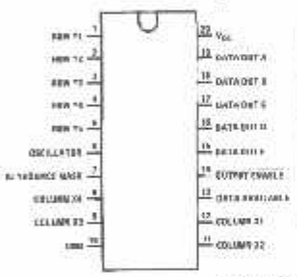


TL/F/6037–14

Top View

Order Number MM74C922

Pin Assignment for DIP and SOIC Package



TL/F/6037–7

Top View

Order Number MM54C923 or MM74C923

TRI-STATE® is a registered trademark of National Semiconductor Corporation

RRD-B30M105/Printed in U.S.A.

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Voltage at Any Pin V_{CC} − 0.3V to V_{CC} + 0.3V

Operating Temperature Range

MM54C922, MM54C923	−55°C to +125°C
MM74C922, MM74C923	−40°C to +85°C

Storage Temperature Range	−65°C to +150°C
Power Dissipation (P_D)	
Dual-In-Line	700 mW
Small Outline	500 mW
Operating V_{CC} Range	3V to 15V
V_{CC}	18V
Lead Temperature (Soldering, 10 seconds)	260°C

DC Electrical Characteristics Min/Max limits apply across temperature range unless otherwise specified

Symbol	Parameter	Conditions	Min	Typ	Max	Units
CMOS TO CMOS						
V_{T+}	Positive-Going Threshold Voltage at Osc and KBM Inputs	V_{CC} = 5V, I_{IN} ≥ 0.7 mA V_{CC} = 10V, I_{IN} ≥ 1.4 mA V_{CC} = 15V, I_{IN} ≥ 2.1 mA	3.0 6.0 9.0	3.6 6.8 10	4.3 8.6 12.9	V V V
V_{T-}	Negative-Going Threshold Voltage at Osc and KBM Inputs	V_{CC} = 5V, I_{IN} ≥ 0.7 mA V_{CC} = 10V, I_{IN} ≥ 1.4 mA V_{CC} = 15V, I_{IN} ≥ 2.1 mA	0.7 1.4 2.1	1.4 3.2 5	2.0 4.0 6.0	V V V
$V_{IN(1)}$	Logical "1" Input Voltage, Except Osc and KBM Inputs	V_{CC} = 5V V_{CC} = 10V V_{CC} = 15V	3.5 8.0 12.5	4.5 9 13.5		V V V
$V_{IN(0)}$	Logical "0" Input Voltage, Except Osc and KBM Inputs	V_{CC} = 5V V_{CC} = 10V V_{CC} = 15V		0.5 1 1.5	1.5 2 2.5	V V V
I_{up}	Row Pull-Up Current at Y1, Y2, Y3, Y4 and Y5 Inputs	V_{CC} = 5V, V_{IN} = 0.1 V_{CC} V_{CC} = 10V V_{CC} = 15V		−2 −10 −22	−5 20 −45	μA μA μA
$V_{OUT(1)}$	Logical "1" Output Voltage	V_{CC} = 5V, I_O = −10 μA V_{CC} = 10V, I_O = −10 μA V_{CC} = 15V, I_O = −10 μA	4.5 9 13.5			V V V
$V_{OUT(0)}$	Logical "0" Output Voltage	V_{CC} = 5V, I_O = 10 μA V_{CC} = 10V, I_O = 10 μA V_{CC} = 15V, I_O = 10 μA			0.5 1 1.5	V V V
R_{ON}	Column "ON" Resistance at X1, X2, X3 and X4 Outputs	V_{CC} = 5V, V_O = 0.5V V_{CC} = 10V, V_O = 1V V_{CC} = 15V, V_O = 1.5V		500 300 200	1400 700 500	Ω Ω Ω
I_{CC}	Supply Current Osc at 0V, (one Y low)	V_{CC} = 5V V_{CC} = 10V V_{CC} = 15V		0.55 1.1 1.7	1.1 1.9 2.6	mA mA mA
$I_{IN(1)}$	Logical "1" Input Current at Output Enable	V_{CC} = 15V, V_{IN} = 15V		0.005	1.0	μA
$I_{IN(0)}$	Logical "0" Input Current at Output Enable	V_{CC} = 15V, V_{IN} = 0V	−1.0	−0.005		μA
CMOS/LPTTL INTERFACE						
$V_{IN(1)}$	Logical "1" Input Voltage, Except Osc and KBM Inputs	54C, V_{CC} = 4.5V 74C, V_{CC} = 4.75V	V_{CC} − 1.5 V_{CC} − 1.5			V V
$V_{IN(0)}$	Logical "0" Input Voltage, Except Osc and KBM Inputs	54C, V_{CC} = 4.5V 74C, V_{CC} = 4.75V			0.8 0.8	V V
$V_{OUT(1)}$	Logical "1" Output Voltage	54C, V_{CC} = 4.5V I_O = −360 μA 74C, V_{CC} = 4.75V I_O = −360 μA	2.4 2.4			V V
$V_{OUT(0)}$	Logical "0" Output Voltage	54C, V_{CC} = 4.5V I_O = −360 μA 74C, V_{CC} = 4.75V I_O = 360 μA			0.4 0.4	V V

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Temperature Range" they are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

DC Electrical Characteristics

Min/Max limits apply across temperature range unless otherwise specified (Continued)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
OUTPUT DRIVE (See 54C/74C Family Characteristics Data Sheet) (Short Circuit Current)						
I_{SOURCE}	Output Source Current (P-Channel)	V_{CC} = 5V, V_{OUT} = 0V, T_A = 25°C	−1.75	−3.3		mA
I_{SOURCE}	Output Source Current (P-Channel)	V_{CC} = 10V, V_{OUT} = 0V, T_A = 25°C	−8	−15		mA
I_{SINK}	Output Sink Current (N-Channel)	V_{CC} = 5V, V_{OUT} = V_{CC}, T_A = 25°C	1.75	3.6		mA
I_{SINK}	Output Sink Current (N-Channel)	V_{CC} = 10V, V_{OUT} = V_{CC}, T_A = 25°C	8	16		mA

AC Electrical Characteristics*

T_A = 25°C, C_L = 50 pF, unless otherwise noted

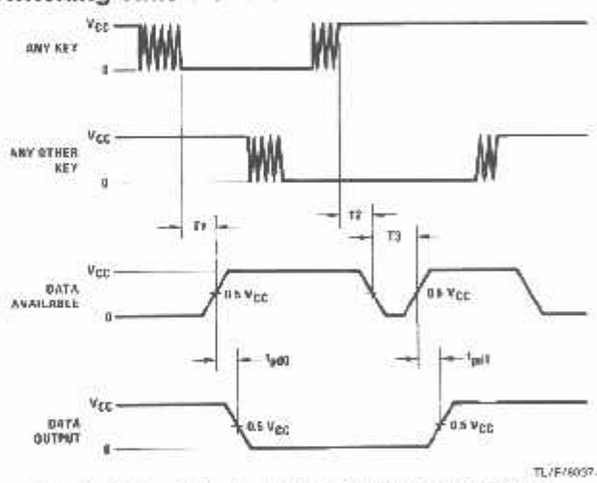
Symbol	Parameter	Conditions	Min	Typ	Max	Units
t_{pd0}, t_{pd1}	Propagation Delay Time to Logical "0" or Logical "1" from D.A.	C_L = 50 pF *(Figure 1)* V_{CC} = 5V V_{CC} = 10V V_{CC} = 15V		 60 35 25	 150 80 60	 ns ns ns
t_{0H}, t_{1H}	Propagation Delay Time from Logical "0" or Logical "1" into High Impedance State	R_L = 10k, C_L = 10 pF *(Figure 2)* V_{CC} = 5V, R_L = 10k V_{CC} = 10V, C_L = 10 pF V_{CC} = 15V		 80 85 50	 200 150 110	 ns ns ns
t_{H0}, t_{H1}	Propagation Delay Time from High Impedance State to a Logical "0" or Logical "1"	R_L = 10k, C_L = 50 pF *(Figure 2)* V_{CC} = 5V, R_L = 10k V_{CC} = 10V, C_L = 50 pF V_{CC} = 15V		 100 55 40	 250 125 90	 ns ns ns
C_{IN}	Input Capacitance	Any Input (Note 2)		5	7.5	pF
C_{OUT}	TRI-STATE Output Capacitance	Any Output (Note 2)		10		pF

*AC Parameters are guaranteed by DC correlated testing.

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Temperature Range" they are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

Note 2: Capacitance is guaranteed by periodic testing.

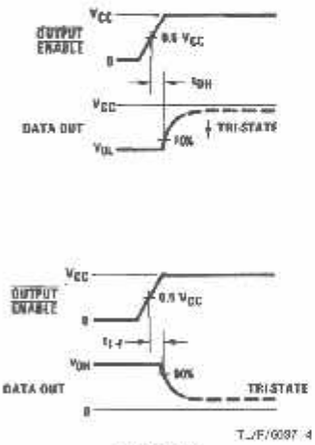
Switching Time Waveforms



TL/F/6037–3

T1 = T2 = RC, T3 = 0.7 RC, where R = 10k and C is external capacitor at KBM input.

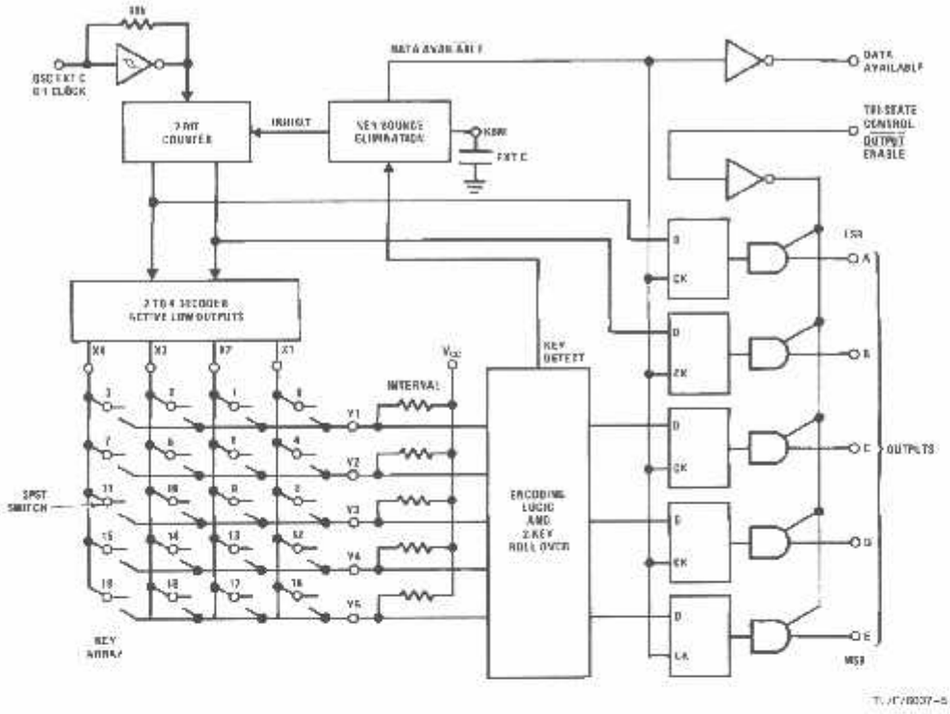
FIGURE 1



TL/F/6037–4

FIGURE 2

Block Diagram



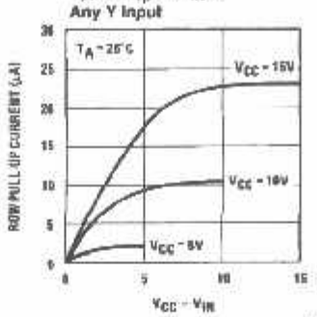
Truth Table

Switch Position	0 Y1,X1	1 Y1,X2	2 Y1,X3	3 Y1,X4	4 Y2,X1	5 Y2,X2	6 Y2,X3	7 Y2,X4	8 Y3,X1	9 Y3,X2	10 Y3,X3	11 Y3,X4	12 Y4,X1	13 Y4,X2	14 Y4,X3	15 Y4,X4	16 Y5',X1	17 Y5',X2	18 Y5',X3	19 Y5',X4
DATA OUT A	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1
DATA OUT B	0	0	1	1	0	0	1	1	0	0	1	1	0	0	1	1	0	0	1	1
DATA OUT C	0	0	0	0	1	1	1	1	0	0	0	0	1	1	1	1	0	0	0	0
DATA OUT D	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	0	0	0	0
DATA OUT E*	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1

*Only for MM54C922/MM74C922

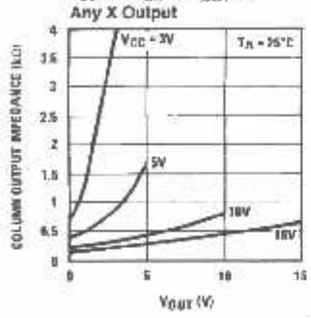
Typical Performance Characteristics

Typical I_{rp} vs V_{IN} at Any Y Input



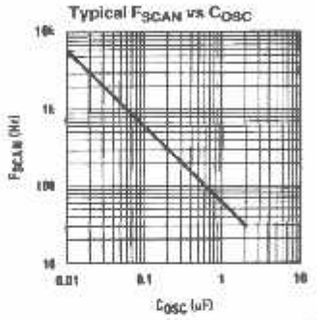
TL/F/6037–6

Typical R_{on} vs V_{OUT} at Any X Output



TL/F/6037–7

Typical F_{SCAN} vs C_{OSC}



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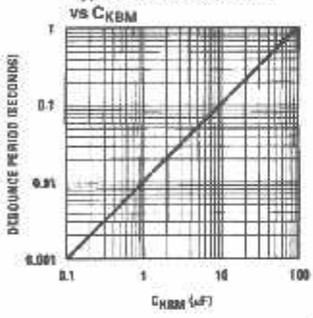
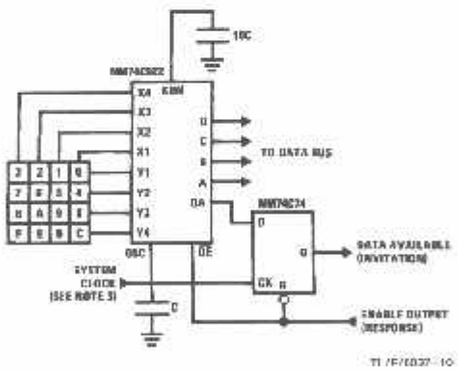
Typical Debounce Period vs C_{KBM}



TL/F/6037–9

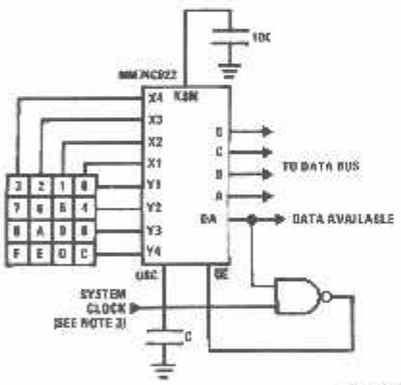
Typical Applications

Synchronous Handshake (MM74C922)



TL/F/6037–10

Synchronous Data Entry Onto Bus (MM74C922)



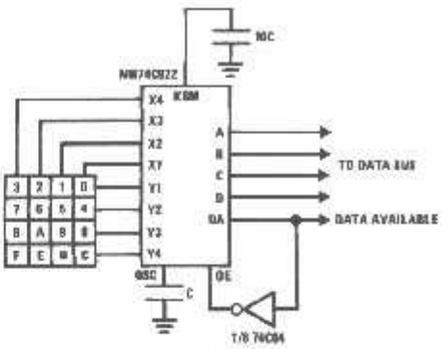
TL/F/6037–11

Outputs are enabled when valid entry is made and go into THI-STATE when key is released.

Note 3: The keyboard may be synchronously scanned by omitting the capacitor at osc. and driving osc. directly if the system clock rate is lower than 10 kHz.

Typical Applications (Continued)

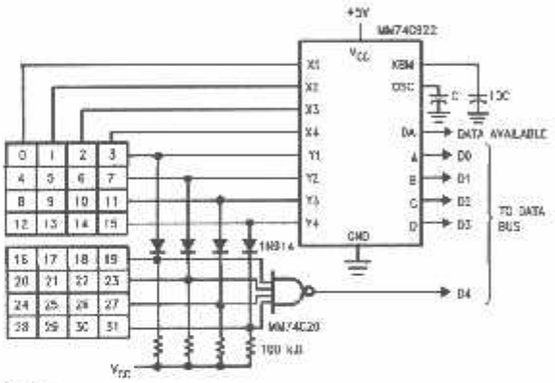
Asynchronous Data Entry Onto Bus (MM74C922)



TL/F/5637-12

Outputs are in TRI-STATE until key is pressed, then data is placed on bus. When key is released, outputs return to TRI-STATE.

Expansion to 32 Key Encoder (MM74C922)



TL/F/5637-13

Theory of Operation

The MM74C922/MM74C923 Keyboard Encoders implement all the logic necessary to interface a 16 or 20 SPST key switch matrix to a digital system. The encoder will convert a key switch closer to a 4(MM74C922) or 5(MM74C923) bit nibble. The designer can control both the keyboard scan rate and the key debounce period by altering the oscillator capacitor, C_{OSC}, and the key bounce mask capacitor, C_{MSK}. Thus, the MM74C922/MM74C923's performance can be optimized for many keyboards.

The keyboard encoders connect to a switch matrix that is 4 rows by 4 columns (MM74C922) or 5 rows by 4 columns (MM74C923). When no keys are depressed, the row inputs are pulled high by internal pull-ups and the column outputs sequentially output a logic "0". These outputs are open drain and are therefore low for 25% of the time and otherwise off. The column scan rate is controlled by the oscillator input, which consists of a Schmitt trigger oscillator, a 2-bit counter, and a 2–4-bit decoder.

When a key is depressed, key 0, for example, nothing will happen when the X1 input is off, since Y1 will remain high. When the X1 column is scanned, X1 goes low and Y1 will go low. This disables the counter and keeps X1 low. Y1 going low also initiates the key bounce circuit timing and locks out the other Y inputs. The key code to be output is a combination of the frozen counter value and the decoded Y inputs. Once the key bounce circuit times out, the data is latched, and the Data Available (DAV) output goes high.

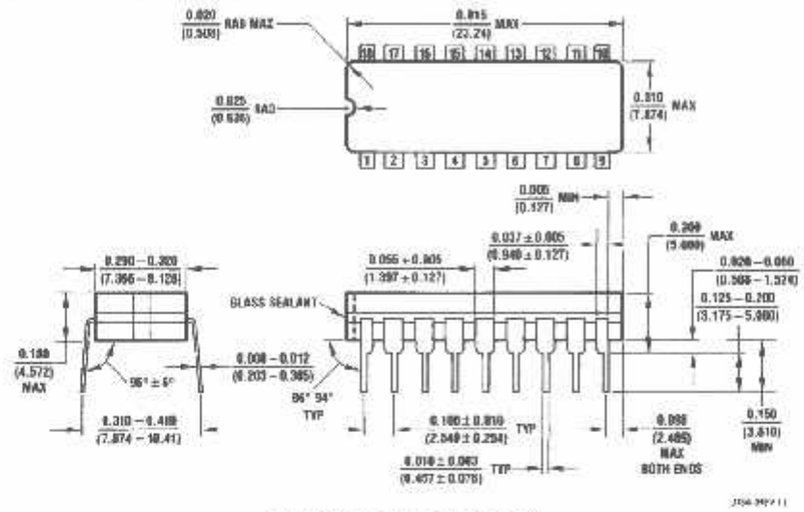
If, during the key closure the switch bounces, Y1 input will go high again, restarting the scan and resetting the key bounce circuitry. The key may bounce several times, but as soon as the switch stays low for a debounce period, the closure is assumed valid and the data is latched.

A key may also bounce when it is released. To ensure that the encoder does not recognize this bounce as another key closure, the debounce circuit must time out before another closure is recognized.

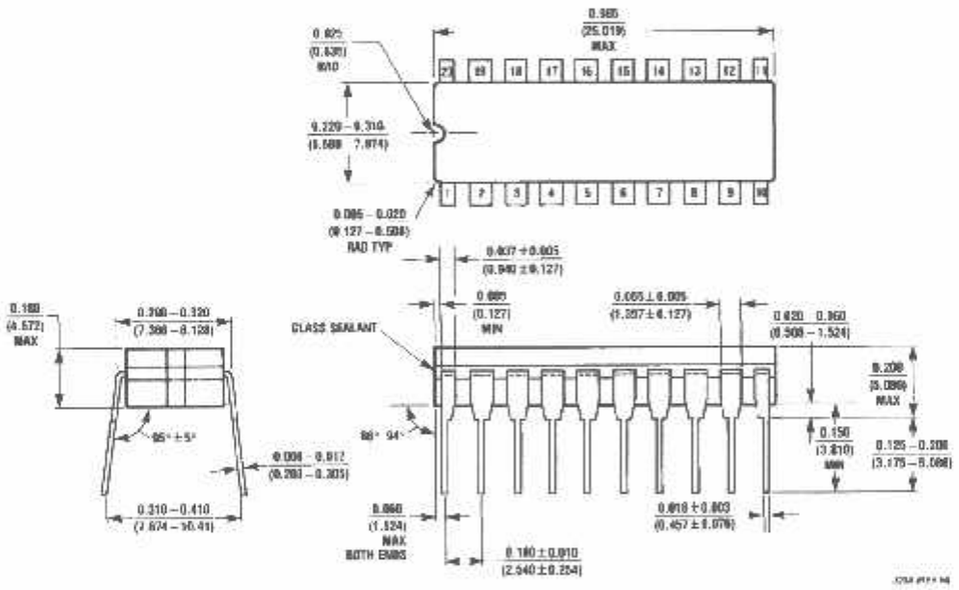
The two-key roll-over feature can be illustrated by assuming a key is depressed, and then a second key is depressed. Since all scanning has stopped, and all other Y inputs are disabled, the second key is not recognized until the first key is lifted and the key bounce circuitry has reset.

The output latches feed TRI-STATE, which is enabled when the Output Enable ($\overline{OE}$) input is taken low.

Physical Dimensions inches (millimeters)

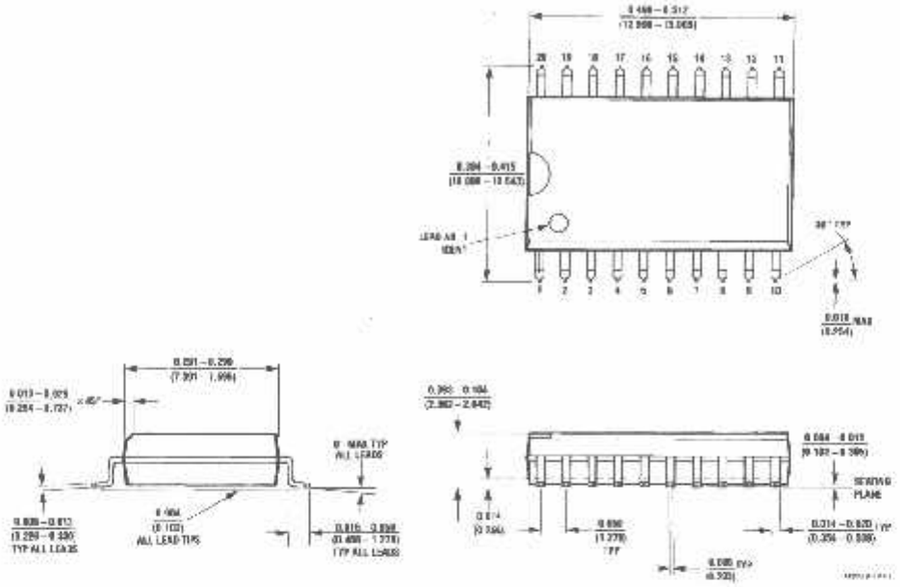


Ceramic Dual-In-Line Package (J)
Order Number MM54C922J or MM74C922J
NS Package Number J18A



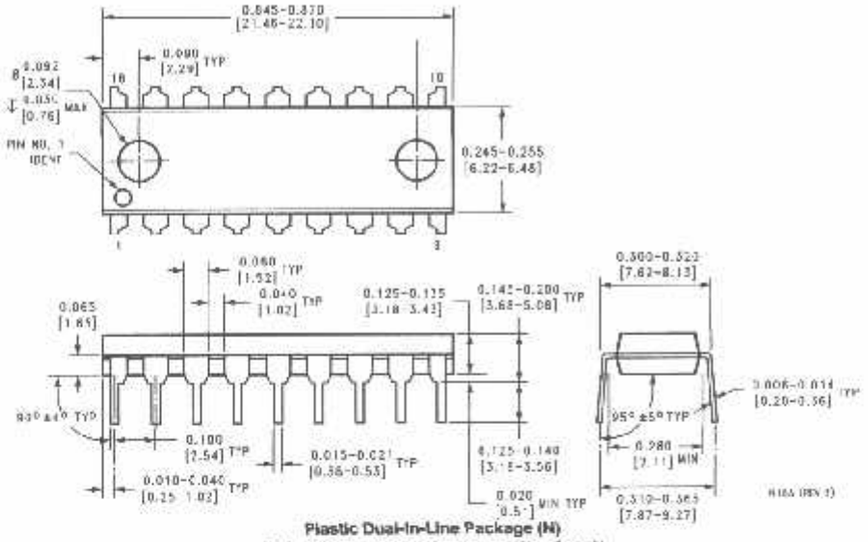
Ceramic Dual-In-Line Package (J)
Order Number MM54C923J or MM74C923J
NS Package Number J20A

Physical Dimensions inches (millimeters) (Continued)



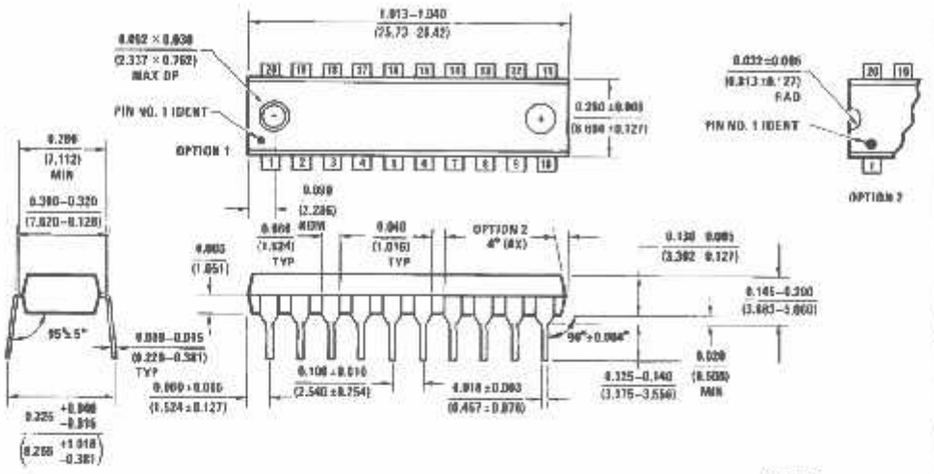
Plastic Small Outline I.C. Package (M)
Order Number MM74C922M or MM74C923M
NS Package Number M20B

Physical Dimensions inches (millimeters) (Continued)



Plastic Dual-In-Line Package (N)
Order Number MM54C922N or MM74C922N
NS Package Number N18A

Physical Dimensions inches (millimeters) (Continued)



Plastic Dual-In-Line Package (N)
Order Number MM54C923N or MM74C923N
NS Package Number N20A

LIFE SUPPORT POLICY

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1. Life support devices or systems are devices or systems which, (a) are intended for surgical implant into the body, or (b) support or sustain life, and whose failure to perform, when properly used in accordance with instructions for use provided in the labeling, can be reasonably expected to result in a significant injury to the user.
2. A critical component is any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

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National Semiconductor

August 2000

LM386
Low Voltage Audio Power Amplifier

General Description

The LM386 is a power amplifier designed for use in low voltage consumer applications. The gain is internally set to 20 to keep external part count low, but the addition of an external resistor and capacitor between pins 1 and 8 will increase the gain to any value from 20 to 200.

The inputs are ground referenced while the output automatically biases to one-half the supply voltage. The quiescent power drain is only 24 milliwatts when operating from a 6 volt supply, making the LM386 ideal for battery operation.

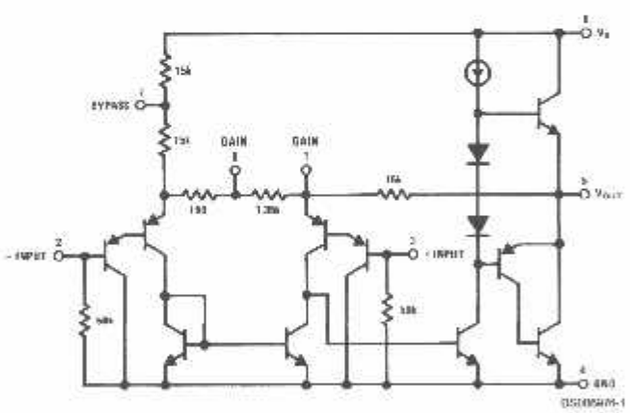
Features

- Battery operation
- Minimum external parts
- Wide supply voltage range: 4V 12V or 5V 18V
- Low quiescent current drain: 4mA
- Voltage gains from 20 to 200
- Ground referenced input
- Self-centering output quiescent voltage
- Low distortion: 0.2% (A_V = 20, V_S = 6V, R_L = 8Ω, P_O = 125mW, f = 1kHz)
- Available in 8 pin MSOP package

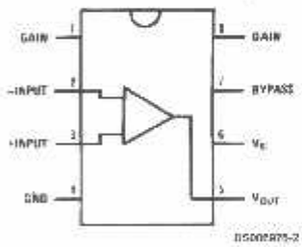
Applications

- AM-FM radio amplifiers
- Portable tape player amplifiers
- Intercoms
- TV sound systems
- Line drivers
- Ultrasonic drivers
- Small servo drivers
- Power converters

Equivalent Schematic and Connection Diagrams



Small Outline, Molded Mini Small Outline, and Dual-In-Line Packages



Top View
Order Number LM386M-1, LM386MM-1, LM386N-1, LM386N-3 or LM386N-4
See NS Package Number M08A, MUA08A or N08E

Absolute Maximum Ratings (Note 2)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Supply Voltage	
(LM386N-1, -3, LM386M-1)	15V
Supply Voltage (LM386N-4)	22V
Package Dissipation (Note 3)	
(LM386N)	1.25W
(LM386M)	0.73W
(LM386MM-1)	0.595W
Input Voltage	±0.4V
Storage Temperature	−65˚C to +150˚C
Operating Temperature	0˚C to +70˚C
Junction Temperature	+150˚C
Soldering Information	
Dual-In-Line Package	
Soldering (10 sec)	+260˚C
Small Outline Package	
(SOIC and MSOP)	
Vapor Phase (60 sec)	+215˚C
Infrared (15 sec)	+220˚C

See AN-450 "Surface Mounting Methods and Their Effect on Product Reliability" for other methods of soldering surface mount devices.

Thermal Resistance	
θ_{JC} (DIP)	37˚C/W
θ_{JA} (DIP)	107˚C/W
θ_{JC} (SO Package)	35˚C/W
θ_{JA} (SO Package)	172˚C/W
θ_{JA} (MSOP)	210˚C/W
θ_{JC} (MSOP)	56˚C/W

Electrical Characteristics (Notes 1, 2)

T_A = 25˚C

Parameter	Conditions	Min	Typ	Max	Units
Operating Supply Voltage (V_S)					
LM386N-1, -3, LM386M-1, LM386MM-1		4		12	V
LM386N-4		5		18	V
Quiescent Current (I_Q)	V_S = 6V, V_{IN} = 0		4	8	mA
Output Power (P_{OUT})					
LM386N-1, LM386M-1, LM386MM-1	V_S = 6V, R_L = 8Ω, THD = 10%	250	325		mW
LM386N-3	V_S = 9V, R_L = 8Ω, THD = 10%	500	700		mW
LM386N-4	V_S = 16V, R_L = 32Ω, THD = 10%	700	1000		mW
Voltage Gain (A_V)	V_S = 6V, f = 1 kHz		26		dB
	10 µF from Pin 1 to 8		46		dB
Bandwidth (BW)	V_S = 6V, Pins 1 and 8 Open		300		kHz
Total Harmonic Distortion (THD)	V_S = 6V, R_L = 8Ω, P_{OUT} = 125 mW		0.2		%
	f = 1 kHz, Pins 1 and 8 Open				
Power Supply Rejection Ratio (PSRR)	V_S = 6V, f = 1 kHz, C_{BYPASS} = 10 µF		50		dB
	Pins 1 and 8 Open, Referred to Output				
Input Resistance (R_{IN})			50		kΩ
Input Bias Current (I_{BIAS})	V_S = 6V, Pins 2 and 3 Open		250		nA

Note 1: All voltages are measured with respect to the ground pin, unless otherwise specified.

Note 2: Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is functional, but do not guarantee specific performance limits. Electrical Characteristics state DC and AC electrical specifications under particular test conditions which guarantee specific performance limits. This assumes that the device is within the Operating Ratings. Specifications are not guaranteed for parameters where no limit is given, however, the typical value is a good indication of device performance.

Note 3: For operation in ambient temperatures above 25˚C, the device must be derated based on a 150˚C maximum junction temperature and 1) a thermal resistance of 107˚C/W junction to ambient for the dual-in-line package and 2) a thermal resistance of 170˚C/W for the small outline package.

Application Hints

GAIN CONTROL

To make the LM386 a more versatile amplifier, two pins (1 and 8) are provided for gain control. With pins 1 and 8 open the 1.35 kΩ resistor sets the gain at 20 (26 dB). If a capacitor is put from pin 1 to 8, bypassing the 1.35 kΩ resistor, the gain will go up to 200 (46 dB). If a resistor is placed in series with the capacitor, the gain can be set to any value from 20 to 200. Gain control can also be done by capacitively coupling a resistor (or FET) from pin 1 to ground.

Additional external components can be placed in parallel with the internal feedback resistors to tailor the gain and frequency response for individual applications. For example, we can compensate poor speaker bass response by frequency shaping the feedback path. This is done with a series RC from pin 1 to 5 (paralleling the internal 15 kΩ resistor). For 6 dB effective bass boost: R = 15 kΩ, the lowest value for good stable operation is R = 10 kΩ if pin 8 is open. If pins 1 and 8 are bypassed then R as low as 2 kΩ can be used. This restriction is because the amplifier is only compensated for closed-loop gains greater than 9.

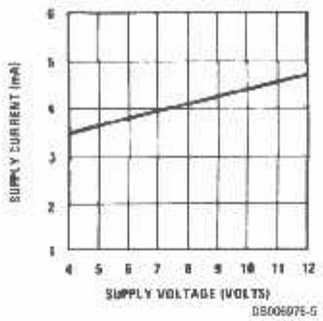
INPUT BIASING

The schematic shows that both inputs are biased to ground with a 50 kΩ resistor. The base current of the input transistors is about 250 nA, so the inputs are at about 12.5 mV when left open. If the dc source resistance driving the LM386 is higher than 250 kΩ it will contribute very little additional offset (about 2.5 mV at the input, 50 mV at the output). If the dc source resistance is less than 10 kΩ, then shorting the unused input to ground will keep the offset low (about 2.5 mV at the input, 50 mV at the output). For dc source resistances between these values we can eliminate excess offset by putting a resistor from the unused input to ground, equal in value to the dc source resistance. Of course all offset problems are eliminated if the input is capacitively coupled.

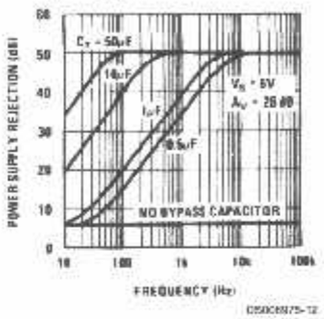
When using the LM386 with higher gains (bypassing the 1.35 kΩ resistor between pins 1 and 8) it is necessary to bypass the unused input, preventing degradation of gain and possible instabilities. This is done with a 0.1 µF capacitor or a short to ground depending on the dc source resistance on the driven input.

Typical Performance Characteristics

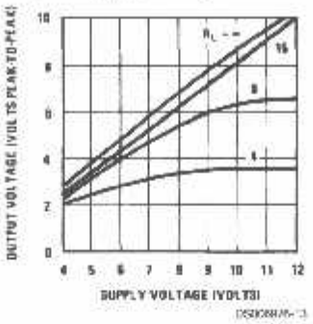
Quiescent Supply Current vs Supply Voltage



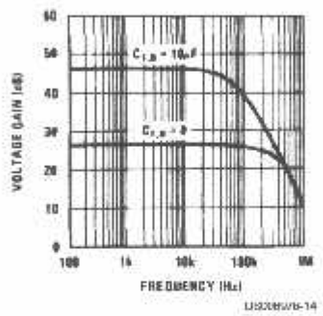
Power Supply Rejection Ratio (Referred to the Output) vs Frequency



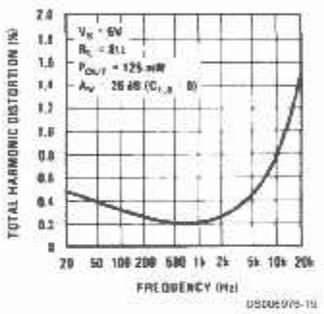
Peak-to-Peak Output Voltage Swing vs Supply Voltage



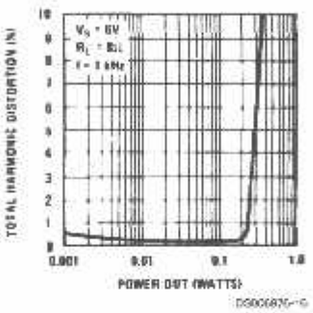
Voltage Gain vs Frequency



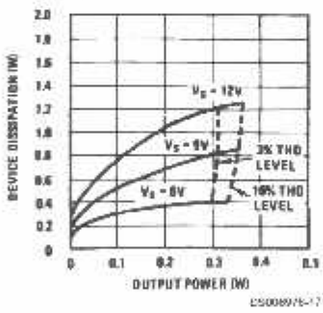
Distortion vs Frequency



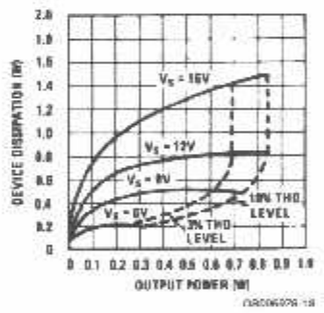
Distortion vs Output Power



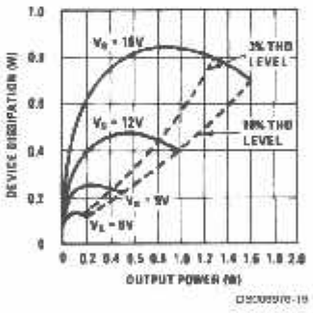
Device Dissipation vs Output Power—4Ω Load



Device Dissipation vs Output Power—8Ω Load

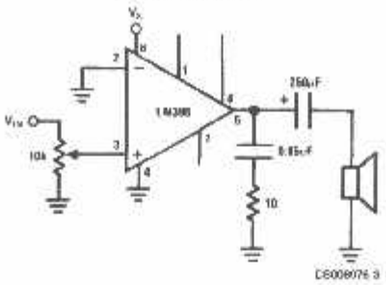


Device Dissipation vs Output Power—16Ω Load

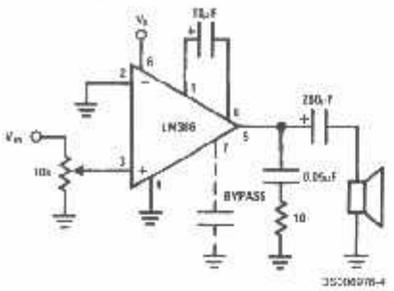


Typical Applications

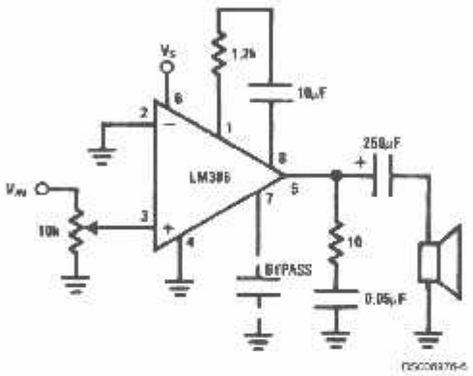
Amplifier with Gain = 20
Minimum Parts



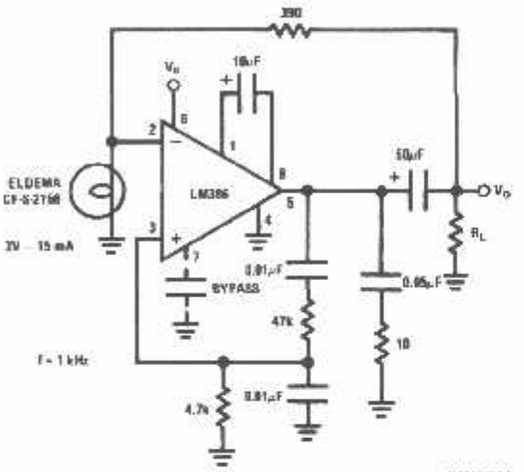
Amplifier with Gain = 200



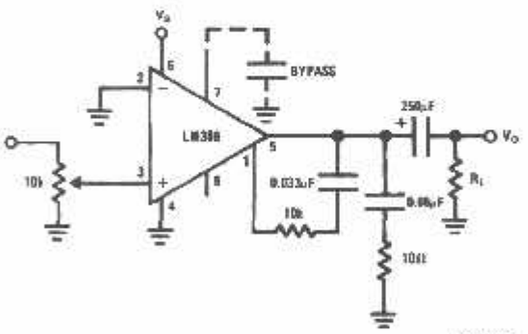
Amplifier with Gain = 50



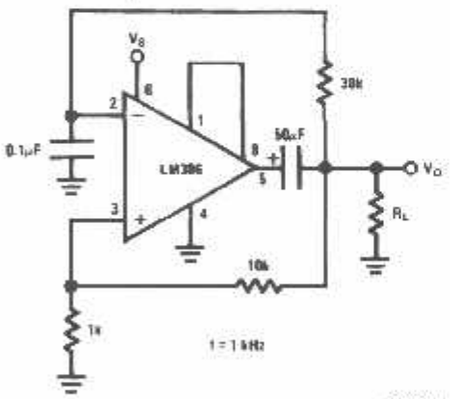
Low Distortion Power Wienbridge Oscillator



Amplifier with Bass Boost

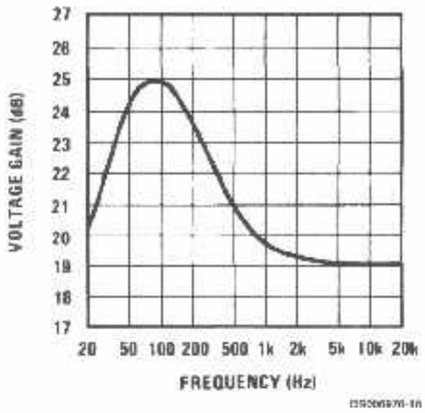


Square Wave Oscillator

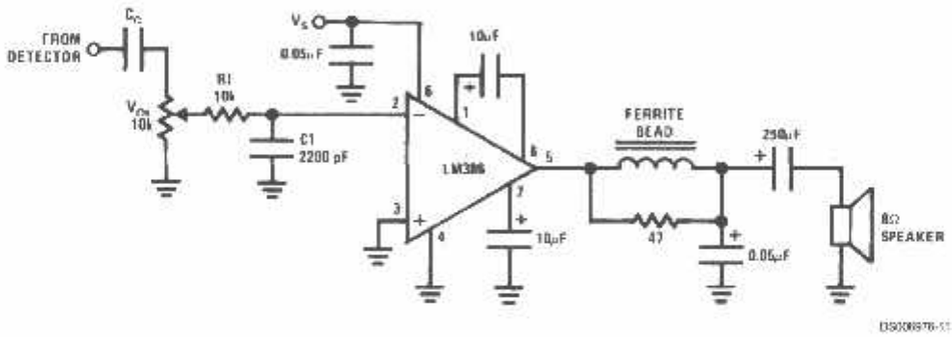


Typical Applications (Continued)

Frequency Response with Bass Boost



AM Radio Power Amplifier



Note 4: Twist Supply lead and supply ground very tightly.

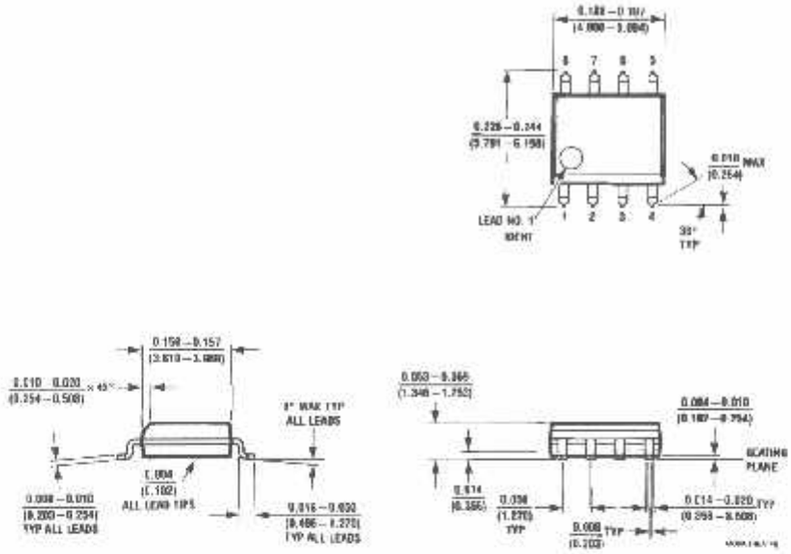
Note 5: Twist speaker lead and ground very tightly.

Note 6: Ferrite bead in Ferroxcube K5-001-001/3B with 3 turns of wire.

Note 7: R1C1 band limits input signals.

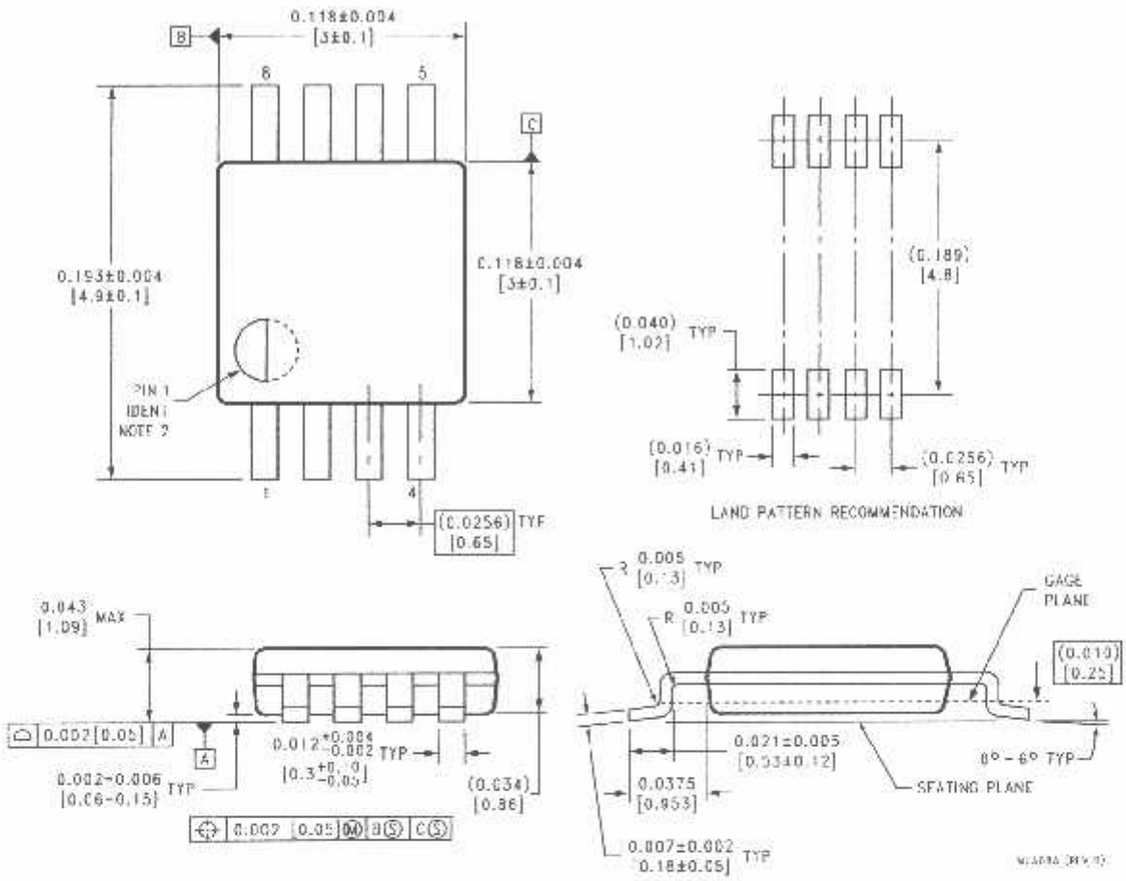
Note 8: All components must be spaced very closely to IC.

Physical Dimensions inches (millimeters) unless otherwise noted



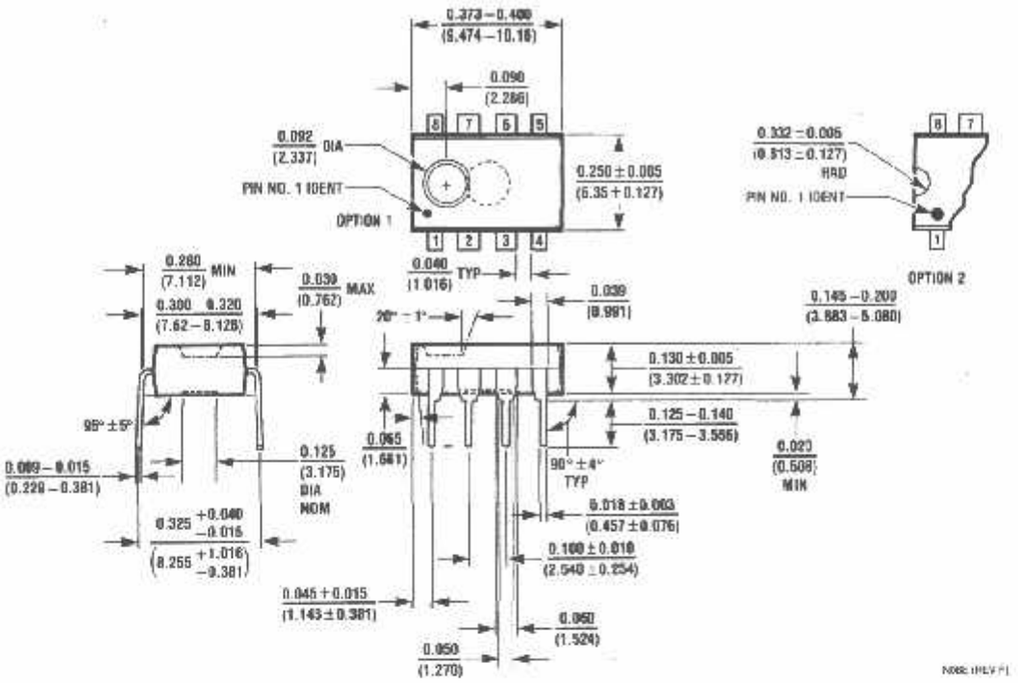
SO Package (M)
Order Number LM386M-1
NS Package Number M08A

Physical Dimensions inches (millimeters) unless otherwise noted (Continued)



8-Lead (0.118" Wide) Molded Mini Small Outline Package
Order Number LM386MM-1
NS Package Number MUA08A

Physical Dimensions inches (millimeters) unless otherwise noted (Continued)



Dual-In-Line Package (N)
Order Number LM386N-1, LM386N-3 or LM386N-4
NS Package Number N08E

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