SKRIPSI

PERENCANAAN DAN PEMBUATAN WEB SERVER BERBASISKAN MIKROKONTROLER AT89S8252 DENGAN MODUL ETHERNET EG-SR-7150MJ UNTUK MENGENDALIKAN LAMPU SECARA REMOTE

Disusun Oleh :

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JURUSAN TEKNIK ELEKTRO S-1

KONSENTRASI TEKNIK ELEKTRONIKA

FAKULTAS TEKNOLOGI INDUSTRI

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SEPTEMBER 2007

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LEMBAR PERSETUJUAN

PERENCANAAN DAN PEMBUATAN WEB SERVER BERBASISKAN MIKROKONTROLER AT89S8252 DENGAN MODUL ETHERNET EG-SR-7150MJ UNTUK MENGENDALIKAN LAMPU SECARA REMOTE

SKRIPSI

Disusun dan Diajukan Sebagai Salah Satu Syarat Untuk Memperoleh Gelar Sarjana Teknik Elektro Strata Satu (S-1)

Disusun Oleh :

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JURUSAN TEKNIK ELEKTRO S-1
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2007

INSTITUT TEKNOLOGI NASIONAL MALANG
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JURUSAN TEKNIK ELEKTRO S-1
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ABSTRAK

PERENCANAAN DAN PEMBUATAN WEB SERVER BERBASISKAN MIKROKONTROLER AT89S8252 DENGAN MODUL ETHERNET EG-SR-7150MJ UNTUK MENGENDALIKAN LAMPU SECARA REMOTE

(Moh Zulkarnain, 0017082, Jurusan Teknik Elektro S-1/Elektronika)
(Dosen Pembimbing I: Ir. Yudi Limpraptono, MT.)
(Dosen Pembimbing II: Joseph Dedy Irawan, ST. MT.)

Kata Kunci: *web server*, mikrokontroler, protokol komunikasi, TCP/IP.

Pada Skripsi ini telah direalisasikan sebuah *web server* yang menyimpan halaman-halaman *web* pada sebuah mikrokontroler. Untuk merealisasikan sebuah *web server* yang terhubung ke jaringan internet, maka protokol TCP/IP harus diimplementasikan sebagai perangkat lunak terlebih dahulu pada sistem mikrokontroler yang digunakan sebagai *web server*. Protokol-protokol penyusun TCP/IP yang diimplementasikan yaitu internet protokol(IP), *Transmission Control Protocol* (TCP), *Hypertext Transfer Protocol* (HTTP). Sistem mikrokontroler yang dihubungkan ke jaringan internet menggunakan *serial to Ethernet gateway* EG-SR-7150MJ. Kelebihan sistem *web server* pada skripsi ini dibandingkan yang sudah ada di pasaran adalah protokol TCP/IP terletak di mikrokontroler sebagai perangkat lunak, sehingga realisasi sistem menjadi jauh lebih efisien, karena tidak memerlukan IC TCP/IP menjadikan sistem lebih ringkas dan murah. Dari hasil pengujian dapat disimpulkan bahwa sistem dapat bekerja dengan baik. Itu semua dapat ditunjukkan dengan adanya halaman *web* dari *web server* yang tampil pada *web browser PC-Client*, sesuai dengan tujuan dari skripsi ini yakni untuk memantau dan mengendalikan lampu secara remote maka pada tampilan utama dari halaman webnya adalah terdiri dari status dari masing-masing lampu serta *link* untuk menyalakan dan mematikan lampu.

KATA PENGANTAR

Atas Berkat Rahmat Allah Yang Maha Kuasa, sehingga penulis dapat menyelesaikan laporan Skripsi dengan judul:

"Perencanaan dan Pembuatan Web Server Berbasiskan Mikrokontroler AT89S8252 Dengan Modul Ethernet EG-SR-7150MJ Untuk Mengendalikan Lampu Secara Remote"

Pembuatan Skripsi ini disusun guna memenuhi syarat akhir kelulusan pendidikan jenjang Strata-1 di Institut Teknologi Nasional Malang. Laporan Skripsi ini merupakan tanggung jawab tertulis atas ilmu pengetahuan yang didapat selama penyusun mengikuti kuliah.

Atas terselesaikannya Skripsi ini, penulis mengucapkan terima kasih kepada :

- Bapak Dr. Ir. Abraham Lomi, MSEE selaku Rektor Institut Teknologi Nasional Malang.
- Bapak Ir. Mochtar Asroni, MSME selaku Dekan Fakultas Teknologi Industri Institut Teknologi Nasional Malang
- Bapak Ir. Yudi Limpraptono, MT selaku Ketua Jurusan Teknik Elektro S1 / Elektronika.
- Bapak Ir. Yudi Limpraptono, MT selaku Dosen Pembimbing pertama yang telah memberikan bimbingan, pengarahan, serta ilmu-ilmu yang sangat berharga sehingga Skripsi ini dapat terselesaikan.

- Bapak Joseph Dedy Irawan ST, MT selaku Dosen Pembimbing kedua yang telah memberikan bimbingan, pengarahan, serta ilmu-ilmu yang sangat berharga sehingga Skripsi ini dapat terselesaikan.

Penulis menyadari bahwa laporan ini masih banyak yang perlu disempurnakan. Oleh sebab itu kritik dan saran yang membangun sangat diharapkan.

Akhir kata, penulis mohan maaf kepada semua pihak bilamana selama penyusunan Skripsi ini penyusun membuat kesalahan secara tidak sengaja dan semoga Skripsi ini dapat bermanfaat bagi kita semua.

Malang, Agustus 2007

Penulis

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BAB I

PENDAHULUAN

1.1. Latar Belakang

Dengan berkembangnya teknologi internet yang merupakan suatu sistem komunikasi yang *reliable*, maka internet sering digunakan sebagai media pada pemantauan dan pengendalian jarak jauh. Internet diharapkan dapat menjadi sebuah media pemantau dan pengendali jarak jauh yang cukup baik karena banyaknya protokol-protokol yang digunakan serta kemampuan protokol-protokol komunikasi tersebut untuk mengurangi kesalahan informasi yang dikirimkan seminimal mungkin.

Akan tetapi kendala yang dihadapi adalah masalah ketidakpraktisan (tidak portable) dan boros daya karena mimimal harus menggunakan sebuah *Personal Computer* (PC) sebagai *Web Server* untuk menghubungkan alat yang dikendalikan dengan jaringan internet.

Oleh karena itu untuk tujuan portabilitas dan efisiensi daya, pada skripsi ini diciptakan suatu perangkat kecil pengganti PC sebagai *Web Server* untuk dapat menghubungkan alat yang dikendalikan dengan jaringan internet, yang dalam hal ini pemantauan dan pengaturan lampu secara remote sesuai dengan judul skripsi ini yaitu **"Perencanaan Dan Pembuatan Web Server Berbasiskan Mikrokontroler AT89S8252 Dengan Modul Ethernet EG-SR-7150MJ Untuk Mengendalikan Lampu Secara Remote"** dan sesuai dengan namanya, *Web*

Server ini bekerja dengan bantuan Modul Ethernet EG-SR-7150MJ Sebagai penghubung ke jaringan internet. Adapun kelebihan dari sistem ini dibandingkan *Web Server* yang ada di pasaran adalah protokol TCP/IP terletak di dalam mikrokontroler sebagai perangkat lunak, sehingga realisasi sistem menjadi jauh lebih efisien, karena tidak memerlukan PC sebagai *Web Server* dan tentunya lebih ringkas serta relatif terjangkau.

1.2. Rumusan Masalah

Mengacu pada permasalahan yang ada, maka dalam perencanaan dan pembuatan alat ini diutamakan pada hal-hal sebagai berikut :

1. Mempelajari dan meneliti Modul Ethernet EG-SR-7150MJ
2. Membuat dan merencanakan rangkaian antarmuka RS-232
3. Membuat dan merencanakan rangkaian unit *Web Server* berbasis mikrokontroler AT89S8252
4. Membuat dan merencanakan rangkaian driver relay

1.3. Batasan Masalah

Dalam laporan akhir "Perencanaan Dan Pembuatan *Web Server* Berbasiskan Mikrokontroler AT89S8252 Dengan Modul Ethernet EG-SR-7150MJ Untuk Mengendalikan Lampu Secara *Remote*", maka perlu kiranya memberikan batasan-batasan masalah agar tidak terjadi penyimpangan maksud dan tujuan utama penyusunan skripsi ini.

1. Menggunakan Modul Ethernet EG-SR-7150MJ sebagai antarmuka antara Web Server Dengan jaringan Internet
2. Menggunakan web browser (Internet Explorer) pada PC-Client
3. Menggunakan rangkaian RS-232 sebagai antarmuka antara Modul Ethernet dengan Web Server

1.4. Tujuan

Tujuan dari penulisan skripsi ini adalah untuk membuat suatu sistem yang terdiri atas ethernet dan mikrokontroler sehingga dapat mengetahui dan mengatur kondisi lampu secara remote.

1.5. Metodelogi Pembahasan

Metodelogi penelitian yang dipakai dalam pembuatan Skripsi ini:

1. Studi Literatur.
2. Perancangan dan pembuatan alat.
3. Pelaksanaan uji coba alat.
4. Penyusunan Laporan Skripsi.

1.6. Sistematika Penulisan

Penulisan Skripsi ini terbagi dalam lima Bab dengan sistematika sebagai berikut:

BAB I. PENDAHULUAN

Berisi latar belakang, tujuan, permasalahan, batasan masalah, metodelogi, dan sistematika penulisan.

BAB II. LANDASAN TEORI

Membahas teori – teori dasar penunjang, perancangan dan pembuatan alat.

BAB III. PERANCANGAN DAN PEMBUATAN ALAT

Membahas tentang perancangan alat baik perangkat keras maupun perangkat lunak, serta cara kerja blok diagram.

BAB IV. PENGUJIAN ALAT

Mencakup pembahasan tentang proses pengujian alat yang terdiri dari peralatan yang digunakan, langkah kerja dan analisa hasil pengujian.

BAB V. PENUTUP

Berisi kesimpulan dan saran.


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BAB II

LANDASAN TEORI

Landasan teori sangat membantu untuk dapat memahami suatu sistem. Landasan teori juga dapat digunakan sebagai acuan di dalam merencanakan suatu sistem. Dengan pertimbangan hal-hal tersebut, maka landasan teori merupakan bagian yang harus dipahami untuk pembahasan lebih lanjut. Dalam landasan teori ini akan dibahas teori dasar yang berhubungan dengan ,*Ethernet EG-SR-7150MJ, Protokol TCP/IP, HTML, RS-232, Mikrokontroler AT-89S8252, Optocoupler, relay.*

2.1. Modul Ethernet EG-SR-7150MJ

Modul Ethernet EG-SR-7150MJ adalah Modul antarmuka serial ke ethernet *gateway* atau dengan kata lain sebuah Modul yang dapat mengkonversikan data serial ke ethernet dengan protokol *TCP/IP,UDP,ARP,ICMP,MAC(IGMP,PPPoE)* atau sebaliknya dari TCP/IP ke dalam bentuk data serial. Keunggulan digunakannya Modul ini adalah kemampuannya untuk berdiri sendiri tanpa adanya PC(*Personal Computer)* Modul ini bisa bertindak sebagai *Client* dapat juga bertindak sebagai *Server* tergantung bagaimana mengkonfigurasikannya, koneksi yang dipakai adalah soket RJ-45 yang terhubung ke jaringan atau *network.* Modul Ethernet ini sangat

kompatibel ke banyak perangkat dan aplikasi yang ingin digunakan dan salah satunya di aplikasikan pada pengendalian lampu secara *remote.*

Modul Ethernet EG-SR-7150MJ mempunyai spesifikasi sebagai berikut:

1. Antarmuka LAN menggunakan 10/100 Mbps auto sensing, RJ-45 konektor
2. Protokol yang digunakan TCP/IP, UDP, ARP, ICMP, MAC, (IGMP, PPPoE)
3. Modul Ethernet ini berbasis mikrokontroler AT89C51RC2(8bit MCU dan 32K Flash)
4. Antarmuka dengan perangkat luarnya adalah RS-232 (LVTTL)
5. Sinyal serial : TXD, RXD, RTS, CTS, GND
6. Memiliki Serial Parameters :

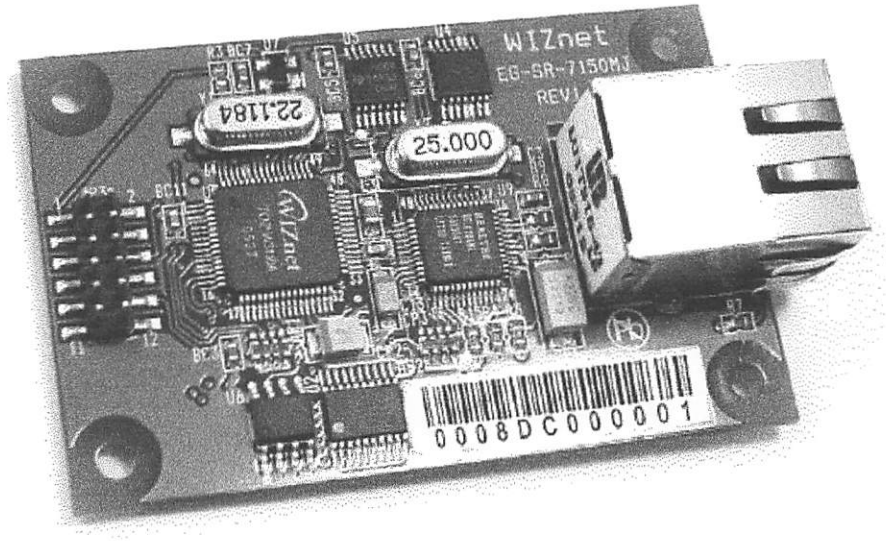
   Parity : None, Even, Odd

   Data : 7, 8

   Flow Control : RTS/CTS, XON/XOFF

   Speed : up to 230Kbps
7. Pengaturan konfigurasi pada sistem operasi Microsoft Windows
8. Temperature 0° C ~ 70° C (Operating), - 40° C ~ 85° C (Storage)
9. Kelembaban 10 ~ 90%
10. Power 3,3 V (150mA)

Adapun gambar fisik dari Modul Ethernet EG-SR-7150MJ dapat digambarkan sebagai berikut:



Gambar 2.1.

Modul Ethernet EG-SR-7150MJ

Sumber : www.wiznet.co.kr

Gambar diatas merupakan Modul dari Ethernet EG-SR-7150MJ secara fisik yang terdiri dari konektor LAN RJ-45, Chip *interface* LAN PHY RTL 8201CP, MCU AT89C51RC2, dan chip wiznet W3150A sebagai komponen utama dari Modul Ethernet tersebut serta komponen-komponen pendukung lainnya.

Selain spesifikasi diatas Modul Ethernet ini juga memiliki *feature* yang tidak disebutkan dalam spesifikasi tersebut diantaranya :

- Modul Ethernet EG-SR-7150MJ sebagai serial ke ethernet gateway terpasang di Modulnya konektor RJ-45
- Mendukung perintah serial

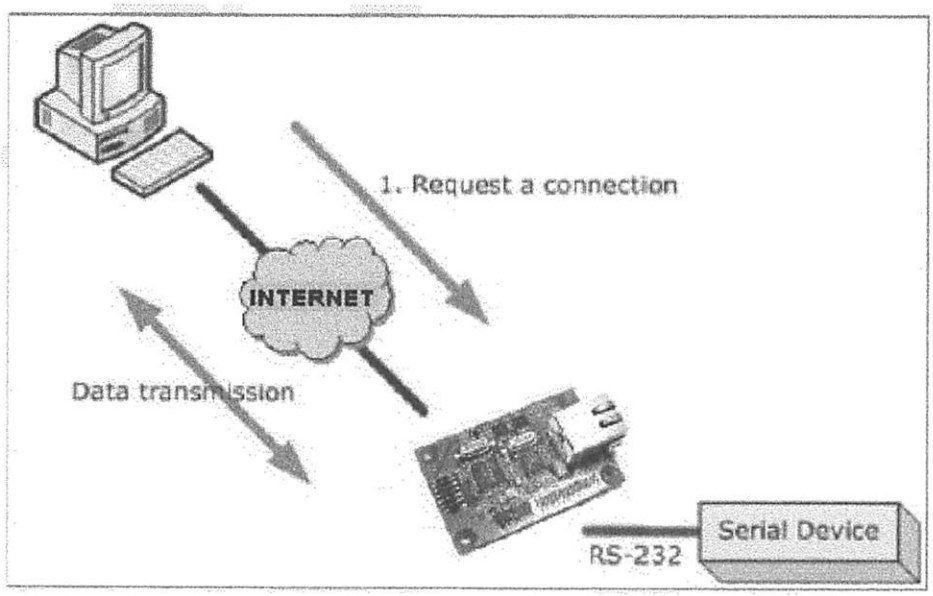
- Perintah frame formatnya sederhana
- Cakupannya luas dan serta mudah diseting pada jaringan dan serial
- Konfigurasi sistem tanpa PC
- Stabilitas sistem tinggi dan pemakaiannya dipercayakan pada Chip W3150A Wiznet, yang medukung secara penuh perangkat keras TCP/IP
- Mudah dan konfigurasinya sederhana
- Antarmuka Ethernet 10/100 Mbps, Antarmuka serial maksimal 230kbps

2.1.1. Mode Operasi Ethernet EG-SR-7150MJ

Ada beberapa perbedaan dalam mode operasi yang didukung pada ethernet ini yakni TCP *Server*, TCP *Client*, dan UDP letak perbedaan dari ketiga mode tersebut hanya pada proses pengiriman data, pada TCP pengiriman data dapat terjamin kualitasnya sampai ke penerima ini semua dapat terwujud karena pada TCP data yang di transmisikan melalui proses verifikasi terlebih dahulu, berbeda halnya dengan UDP setiap data yang dikirim tanpa melalui proses verifikasi dan tidak ada jaminan apakah data yang dikirim benar atau tidak. Pada TCP *Server* dan TCP *Client* hubungannya sangat erat karena pada kedua mode ini sama-sama menggunakan hubungan dua arah antara *Server* ke *Client* atau sebaliknya *Client* ke *Server*.

Berikut gambaran singkat tentang ketiga mode operasi tersebut di atas:

A. TCP Mode server

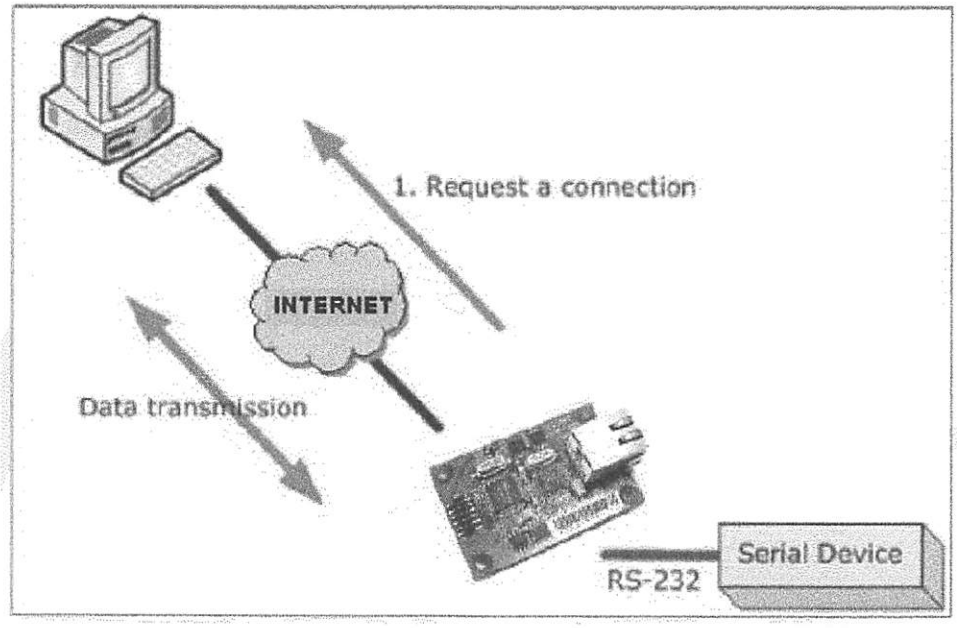


Gambar 2.2. TCP Server Mode
Sumber : www.wiznet.co.kr

Pada mode operasi ini local IP, subnet, *gateway address* dan *local port number* harus dikonfigurasi terlebih dahulu. Modul EG-SR-7150MJ akan menunggu koneksi dengan komputer *host* atau PC-*Client,* selanjutnya PC-*Client* akan meminta data dari serial *device* dalam hal ini mikrokontroler yang terhubung ke perangkat lain ,berikut ilustrasi singkat mengenai transmisi data diatas :

1. PC *Client* terkoneksi dengan ethernet EG-SR-715MJ yang dikonfigurasi pada TCP *Server mode.*
2. Pada saat koneksi terjadi, data ditransmisikan dalam dua arah, dari PC-*Client* Ethernet EG-SR-7150MJ atau sebaliknya dari ethernet EG-SR7150MJ ke PC-*Client.*

B. TCP Client Mode



Gambar 2.3. TCP Client Mode
Sumber : www.wiznet.co.kr

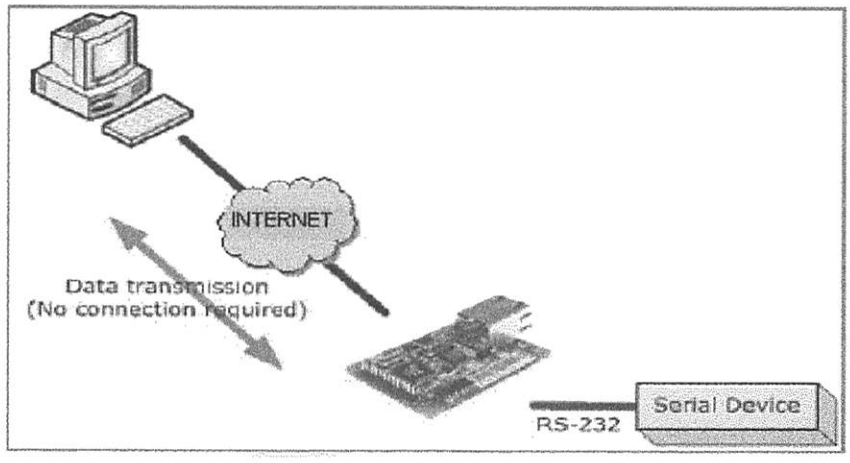
Pada mode operasi ini tidak jauh berbeda dengan sistem operasi TCP *Server Mode*, lokal IP, subnet, *gateway address*, *Server* IP, *Server port number* harus diseting terlebih dahulu. Dalam TCP *Client mode*, Ethernet EG-SR-7150MJ berada pada kondisi open pada saat terkoneksi dengan PC-*Client.*

Gambaran mengenai komunikasi data diatas adalah sebagai berikut :

1. Ethernet EG-SR-7150MJ yang beroperasi pada mode TCP *Client* akan berada pada kondisi dimana sistem yang digunakan sama seperti yang pertama hanya saja perlu adanya setingan pada TCP *Client connection method (Startup, Any Character)* dengan kata lain pada waktu modul EG-SR-7150MJ *start-up* dan terkoneksi ke jaringan kemudian data dari *serial device* dikirim *(any character).*

2. Sesuai dengan keterangan diatas Modul EG-SR-7150MJ yang sudah terkoneksi kejaringan akan mengirim data ke PC-*Client* atau sebaliknya PC-*Client* ke Modul Ethernet EG-SR-7150MJ.

C. UDP Mode



Gambar 2.4. UDP Mode
Sumber : www.wiznet.co.kr

Pada mode operasi ini semua ketentuan diatas tidak berlaku pada mode ini. Dengan kata lain mode ini tidak direkomendasikan.

2.1.2. Spesifikasi Komunikasi Serial Modul EG-SR-7150MJ

Pada subbab ini membicarakan tentang spesifikasi dan struktur data *frame* yang dipakai, serta *command-command* yang ada pada saat menerima respon dari *serial device*.

2.1.2.1. Frame Format

Tabel 2.1 Command Frame Format

Descriptor	STX	Command code	Parameter	ETX
Length(bytes)	1	2	Variable	1

Sumber : www.wiznet.co.kr

Tabel 2.2 Reply Frame Format

Descriptor	STX	Reply code	Parameter	ETX
Length(bytes)	1	1	Variable	1

Sumber : www.wiznet.co.kr

2.1.2.2. STX Dan ETX

Tabel 2.3 STX dan ETX

Setting	Comments
STX	'<' : Hex = 3Ch
ETX	'>' : Hex = 3Eh

Sumber : www.wiznet.co.kr

2.1.2.3. Reply Code

Tabel 2.4 Reply Code

Reply	Comments
S	Command was successful
F	Command failed
1	Invalid command
2	Invalid parameter
E	Enter serial command mode

Sumber : www.wiznet.co.kr

2.1.2.4. Command Code

Tabel 2.5 Command Code

Command	Parameter	Comments
WI	xxx.xxx.xxx.xxx (eg. 192.168.11.133)	Set Local IP
WS	xxx.xxx.xxx.xxx (eg. 255.255.255.0)	Set Subnet mask
WG	xxx.xxx.xxx.xxx (eg. 192.168.11.1)	Set Gateway
WP	0~65535	Set Local IP's port number
WD	0 : Static 1 : DHCP	Set the IP configuration method
WM	0 : TCP server 1 : TCP client 2 : UDP	Set the operation mode
WC	0 : startup 1 : any character	TCP client method
WB	XXXX eg. [Baudrate]1: 115200, 2: 57600, 3: 38400, 4: 19200, 5: 9600, 6: 4800, 7: 2400,8: 1200 [data byte] 7 : 7bit, 8bit [parity] 0 : no parity, 1 : Odd, 2 :Even [Flow] 0 : no, 1 : Xon/Xoff, 2 :RTS/CTS	Set the serial baud rate, data, parity and flow control. 4bytes:[Baud][data byte][parity][flow]
WT	0 : Disable 1 : H/W trigger 2 : S/W trigger	Set the serial command method
WE	xxxxxx (eg. In hex format : 2B 2B 2B)	Set the command mode character

Sumber : www.wiznet.co.kr

WX	xxx.xxx.xxx.xxx (eg. 192.168.11.144)	Set server IP address
WN	0~65535	Set server port number
WR		Restart
OC	XX	Set delimiter character in hex
OS	0~255	Set delimiter size
OT	0~65535	Set delimiter time
OI	0~65535	Set Inactivity timer value
Command	Parameter	Comments
RI		Get Local IP
RS		Get Subnet mask
RG		Get Gateway
RP		Get Local IP's port number
RD		Get the IP configuration method
RM		Get the operation mode
RC		Get the TCP client method
RB		Get the serial baud rate
RT		Get the serial command method
RE		Get the command mode character
RF		Get the firmware version
RX		Get the server IP address
RN		Get the server port number
QC		Get delimiter character in hex
QS		Get delimiter size
QT		Get delimiter time
QI		Get Inactivity timer value

Sumber : www.wiznet.co.kr

2.2. Protokol TCP/IP

Diawali dengan riset yang dilakukan oleh *Advance Research Project Agency* (ARPA) pada tahun 1969 untuk membuat suatu *packet-switching network.* Setelah selesai melakukan eksperimen dan berhasil, semua referensinya di atur di dalam standar *RFC (request for comment),* kemudian TCP/IP yang pertama kali

dikembangkan ini akan digunakan dalam militer sebagai Military Standard (MIL STD) pada tahun 1983. Dan semenjak tahun 1983 internet mulai berkembang secara cepat dan digunakan secara luas.

2.2.1. Arsitektur TCP/IP

Mengacu pada standard OSI (*Open Systems Interconnect Reference Model*), TCP/IP biasanya dideskripsikan atas 3 – 5 level pada *protokol architecture.* Pada gambar dibawah ini didasarkan atas 3 *layer,* yaitu *application, host to host,* dan *network access.*

4 Application Layer
consist of application and processes that use the network.

---

3 Host-to-Host Transport layer
provides end - to - end data delivery service.

---

2 Internet Layer
Defines the datagram and handles The routing of data.

---

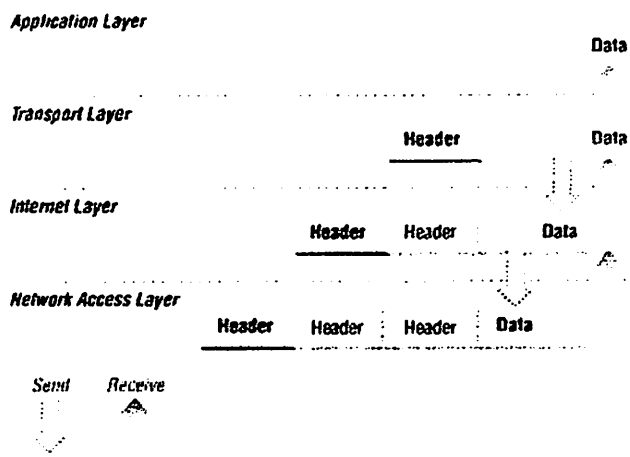
1 Network Acces Layer
consist of routines for accessing physical networks.

Gambar 2.5

Layer Pada TCP/IP Protokol Architecture
Sumber : TCP/IP Network Administrator, 1997

Seperti pada model OSI, data dilewatkan dari hierarki atas ke bawah bila data dikirimkan ke *network,* dan sebaliknya bila data diterima oleh *network* maka

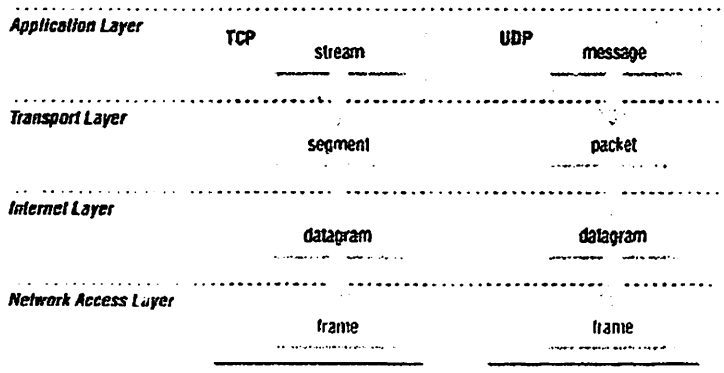
data dilewatkan dari hierarki bawah ke atas. Untuk pengiriman data antar *layer* disebut data *encapsulation.* Pada setiap *layer, header* data yang akan diproses dan di-*passing*-kan ke *layer* berikutnya akan dibuang terlebih dahulu, demikian pula sebaliknya.



Gambar 2.6. Data Encapsulation layer TCP/IP
Sumber : Matthew G Naugle, 1998:693

Setiap *layer* memiliki struktur data yang tersendiri dan bersifat independent. Struktur data tersebut haruslah *compatible* dengan *layer* diatas maupun dibawahnya agar data yang dikirimkan efisien. Bila data yang ditransmisikan menggunakan TCP, data akan dikirim berupa stream. Bila ditransmisikan menggunakan UDP (*User Datagram Protokol*) disebut data berupa *message.* Untuk struktur data pada TCP disebut segment, pada UDP disebut packet. Pada *internet layer* semua data ditampilkan dalam format

datagram. Sedangkan pada network layer sebagian besar data ditransmisikan berupa *packet* atau *frame.*



Gambar 2.7. Struktur Data
Sumber : Matthew G Naugle, 1998:694

2.2.2 Network Acces Layer

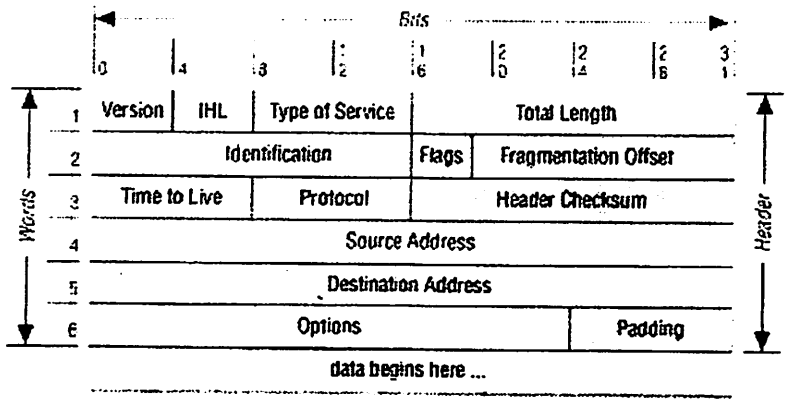
Network Acces Layer ini merupakan *layer* terendah pada TCP/IP. Pada *layer* ini data dikirimkan ke peralatan lain , atau langsung ke *network* yang dituju. Selain itu pada layer ini harus diketahui secara detail address ataupun struktur paket data yang dikirim secara detail. Hal ini mengacu pada *network, data link,* dan *physical layer* pada OSI model yang sering kali tidak mendapat perhatian oleh pengguna internet. Jadi pada *layer* ini berhubungan dengan pengiriman data IP *datagram* oleh network dan *mapping* dari IP *address* ke *physical address* yang digunakan oleh *network.*

2.2.3 Internet Layer

Layer ini merupakan bagian yang paling penting pada TCP/IP. IP mengirimkan *packet data* dimana TCP/IP tersebut ada. Semua data akan dikirimkan melalui IP baik *incoming* maupun *outgoing data.* Pada *layer* ini dilakukan beberapa aktifitas antara lain :

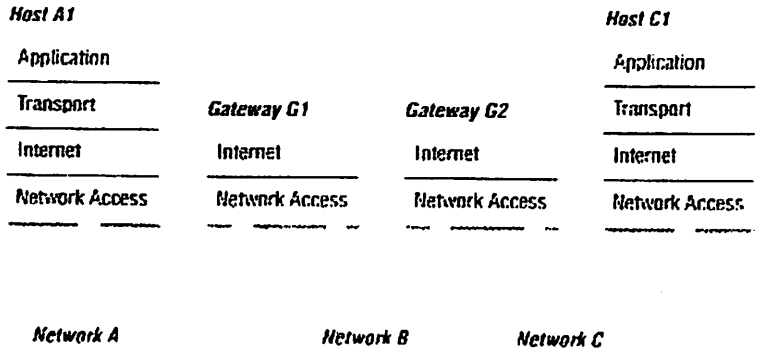
- Pendefinisian *datagram* yang merupakan *basic unit* pada transmisi di internet.
- Pendefinisian skema *internet address.*
- Memindahkan data antara *Network Access layer* dan *Host to Host Transport Layer.*
- *Routing datagram* hingga *remote host.*
- Melakukan proses *fragmentasi* dan *re-assembly datagram.*

TCP/IP protokol ini dibuat untuk mentransmisikan data secara *packet switching network.* Pada *system packet* ini digunakan *addressing* yang terdapat dalam *packet* tersebut untuk membawa *packet data* dari *physical network* yang satu ke *network* yang lain hingga sampai ke tujuan akhir dari *packet data* tersebut. Setiap *packet data* dikrim secara *independent* dan tidak terpengaruh dengan *packet data* yang lain.



Gambar 2.8. Format IP Datagram
Sumber : Matthew G. Naugle, 1998:694

Destination address pada *words* ke 5 pada *header*, berupa standard 32 *bit* IP *address.* Bila *address* tujuan pada *local network* maka akan langsung dikirimkan, tetapi apabila tidak ditemukan pada *local network,* maka paket ini akan dikirimkan ke *gateway* untuk dikirimkan ke *physical network* yang berbeda. Internet *gateway* biasanya disebut IP *router* karena digunakan untuk *routing* paket antar *network.*

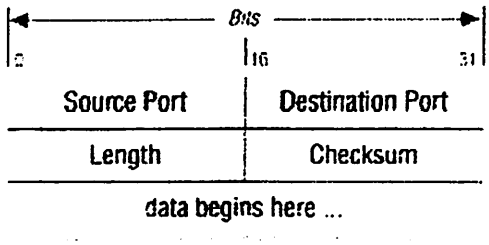


Gambar 2.9. Routing Melalui Gateway
Sumber : Matthew G. Naugle, 1998:695

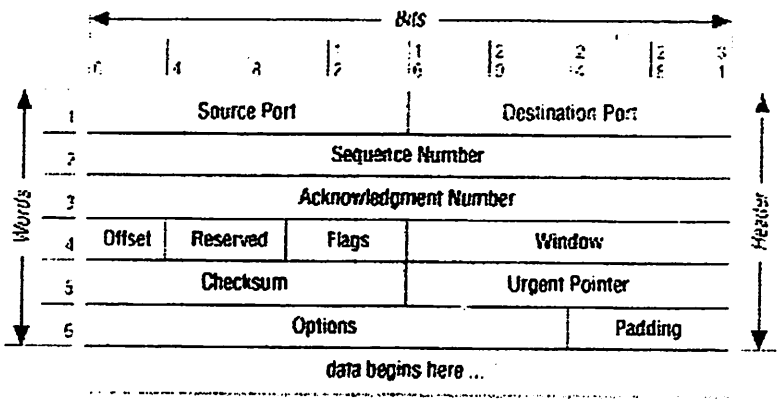
Apabila *datagram* akan dikirim ke *network* yang berbeda, maka diperlukan untuk memecah *datagram* tersebut menjadi bagian yang lebih kecil agar tidak terlalu untuk dikirimkan sebagai sebuah paket data. Setiap *network* memliki batas ukuran paket untuk transfer data, yang disebut sebagai *maximum transmission unit* (mtu). Oleh karena itu perlu dilakukan pemecahan paket data menjadi ukuran yang lebih kecil, yang dinamakan *fragmentation.* Pada *word* ke-2 pada *header* IP terdapat informasi tentang fragmentasi datagram ini dan bagaimana untuk menyatukan kembali *datagram* yang sudah ini menjadi satu paket informasi data utuh.

2.2.4. Transport Layer

Pada *layer* ini terdapat dua *protocol* yang dapat digunakan yaitu *Transmission Control Protokol* (TCP) dan *User Datagram Protocol.* Pada TCP data dikirimkan disertai dengan deteksi error dan koreksi error baik pada pengirim maupun penerima. Sedangkan pada UDP *protocol* yang digunakan lebih sederhana dan tidak seberat pada TCP. UDP sering digunakan apabila data yang ditransmisikan berukuran kecil sehingga proses *hand shake* (untuk memastikan pengiriman data) dirasa lebih besar daripada ukuran data yang dikirimkan.



Gambar 2.10. Format UDP
Sumber : Matthew G. Naugle, 1998:733



Gambar 2.11. TCP Format
Sumber : Matthew G. Naugle, 1998:694

2.2.5. Application Layer

Pada bagian paling atas dari TCP/IP *protocol architecture* ini memuat semua proses yang melibatkan *Transport Layer Protocol* untuk mengirimkan data. Terdapat berbagai *protocol* pada *layer* ini yang kebanyakan menyediakan layanan untuk pengguna, seperti :

- Telnet : yang menyediakan *remote login*

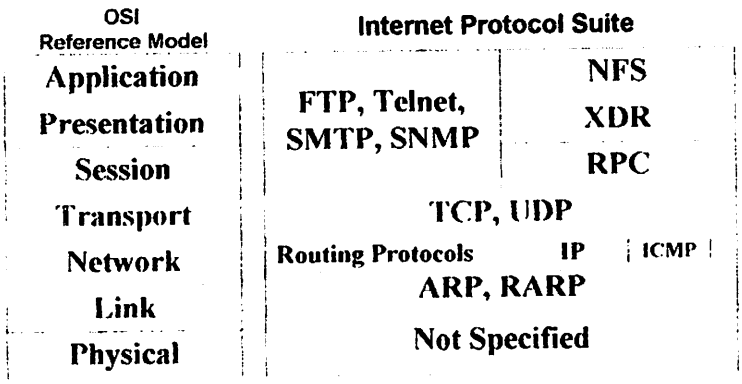
- ftp (*file transfer protokol*) : untuk penerimaan *file* secara *remote*
- smtp (*simple mail transfer protocol*) : digunakan untuk pengiriman *email*
- http (*hypertext transfer protocol*) : untuk pengiriman *web page*

Bila kita bekerja sebagai user dan sekaligus sebagai *system administrator*, selain itu masih terdapat beberapa *protocol* lain yang digunakan pada layer ini antara lain :

- DNS *(Domain Name System)* : untuk IP *address* ke bentuk huruf
- OSPF (*Open Shortest Part First*) : digunakan untuk pertukaran informasi *routing network.*
- NFS *(Network File System)* : digunakan untuk *file Sharing* untuk berbagai macam *Host* dalam *network*

2.2.6. Internet Protokol

Internet Protokol (IP) adalah protokol lapisan jaringan (lapisan 3) yang berisi informasi pengalamatan dan sejumlah informasi kontrol yang membuat paket-paket data dikirimkan. Bersama dengan *Transmission Control Protocol* (TCP), IP mewakili jantung dari protokol–protokol internet. IP memiliki dua tanggung jawab utama : menyediakan usaha pengantaran datagram melalui sebuah internet *network* dan melaksanakan pembongkaran dan perakitan ulang datagram untuk mendukung *link-link* data ukuran unit transmisi maksimum yang berbeda-beda.



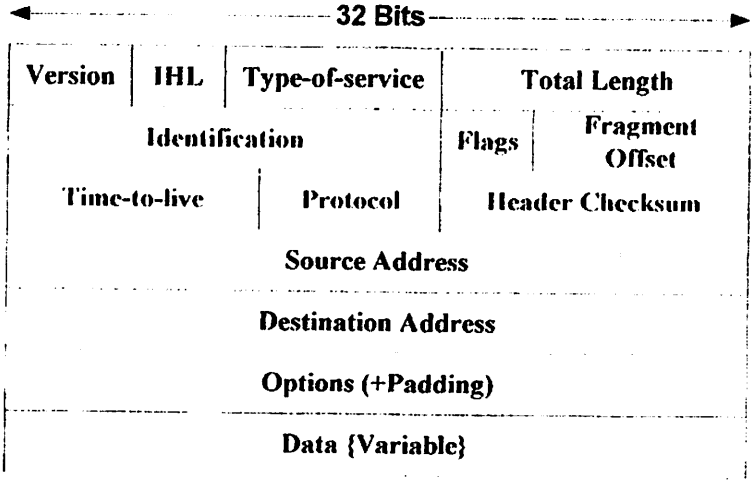
Gambar 2.12

Protokol-Protokol Internet Dan Kesetaraannya Dengan Model OSI

Sumber : Matthew G. Naugle, 1998:692

2.2.6.1 Format Paket IP

Sebuah paket IP berisi bebrapa jenis informasi, seperti digambarkan berikut ini :



Gambar 2-13 Format Paket IP

Sumber : Matthew G. Naugle, 1998:696

Berikut ini penjelesan dari masing-masing *field* paket IP yang diilustrasikan pada gambar 2.13. :

- **Version** – menunjukkan versi IP yang dipakai
- **IP Header Length (IHL)** – menunjukkan panjang *header* datagram *word* 32-bit.
- **Type-Of-Service** – Menentukan bagaimana protokol dilapisan atas menangani datagram.
- **Total length** – menentukan panjang, dalam *byte*, dari seluruh paket IP, termasuk data dan *header.*
- **Identification** – Berisi bilangan bulat yang mengidentifikasi datagram. *Field* ini digunakan untuk membantu penyatuan kembali fragmen-fragmen datagram.
- **Flags** – Terdiri dari tiga bit, dua bit *low-order* mengontrol fragmentasi. Bit ke 0 menentukan apakah paket dapat difragmentasi atau tidak. Bit ke 1 menentukan apakah paket adalah fragmen terakhir dalam satu seri paket yang difragmentasi. Bit ke 2 tidak digunakan.
- **Fragment Offset** – Menunjukkan posisi fragmen data relatif terhadap awal datagram aslinya, yang memungkinkan IP tujuan memproses rekonstruksi data kembali ke datagram aslinya.
- **Time-to-Live** – Menetapkan sebuah penghitung yang secara berkala mengurangi nilainya menuju nol, dimana datagram tidak dikirimkan lagi. Ini menghindari pengiriman sebuah datagram yang tak berakhir.

- **Protokol** – Menunjukkan protokol apa yang dipakai untuk menerima paket data yang datang setelah diproses oleh IP.
- **Header Checksum** – Membantu untuk memastikan integritas *header* IP.
- **Source Address** – Menentukan alamat pengirim.
- **Destination Address** – Menentukan alamat penerima.
- **Option (+ Padding)** – Memungkinkan IP untuk mendukung berbagai opsi, seperti keamanan.
- **Data** – Berisi informasi *layer* diatasnya.

2.2.6.2. Pengalamatan IP

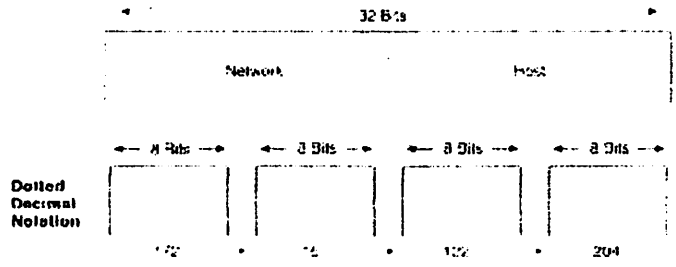
Seperti protokol lapis-jaringan lainnya, pengalamatan IP telah menyatu pada proses pngiriman datagram IP melalui sebuah internet *network.* Setiap alamat IP memiliki komponen-komponen tertentu dan mengikuti sebuah format dasar. Alamat IP ini dapat dibagi dan digunakan untuk menciptakan alamat-alamat untuk sub jaringan, seperti dibicarakan lebih detail pada bagian 2.2.6.3 Format Alamat IP.

Setiap *host* pada jaringan TCP/IP diberi sebuah alamat logik 32-bit yang unik, yang dibagi dalam dua bagian utama: nomor jaringan dan nomor *host.* Nomor jaringan mengidentefikasi sebuah jaringan dan harus didaftarkan Internet *Network Information Center (InterNIC)* jika jaringan tersebut menjadi bagian dari internet. Sebuah penyedia layanan internet (ISP) dapat memperoleh blok-blok alamat jaringan dari *InterNIC* dan dapat mengatur ruang-ruang alamat menurut

keperluannya sendiri. Nomor *host* mengidentifikasi sebuah *host* dalam sebuah jaringan dan didaftarkan oleh administrator jaringan lokal.

2.2.6.3. Format Alamat IP

32-bit alamat IP dikelompokkan masing-masing 8-bit, dipisahkan tanda titik, dan mewakili format desimal (dikenal dengan *dotted decimal notation*). Masing-masing kelompok dapat bernilai minimum dan maksimum 255. Gambar 2.14. mengilustrasikan format dasar sebuah alamat IP.



Gambar 2.14. Format Alamat IP
Sumber : Matthew G. Naugle, 1998:701

2.2.6.4. Kelas-kelas Alamat IP

Pengalamatan IP mendukung lima kelas alamat yang berbeda: A, B, C, D dan E. Hanya kelas A, B dan C yang disediakan untuk keperluan komersial. Bit-bit paling kiri (*high order*) menunjukkan kelas *network*. Tabel 2.2 memberikan informasi ke lima kelas alamat IP.

IP Addr Class	Format	Purpose	High-Order Bit(s)	Address Range	No. Bits Network/Host	Max. Hosts
A	N.H.H.H[1]	Few large organizations	0	1.0.0.0 to 126.0.0.0	7/24	16,777, 214[2] (2^{24} - 2)
B	N.N.H.H	Medium-size organizations	1, 0	128.1.0.0 to 191.254.0.0	14/16	65, 543 (2^{16} - 2)
C	N.N.N.H	Relatively small organizations	1, 1, 0	192.0.1.0 to 223.255.254.0	22/8	245 (2^{8} - 2)
D	N/A	Multicast groups (RFC 1112)	1, 1, 1, 0	224.0.0.0 to 239.255.255.255	N/A (not for commercial use)	N/A
E	N/A	Experimental	1, 1, 1, 1	240.0.0.0 to 254.255.255.255	N/A	N/A

Sumber: www.cisco.com

Tabel 2.1 Informasi Kelas-Kelas Alamat IP
Sumber: www.cisco.com

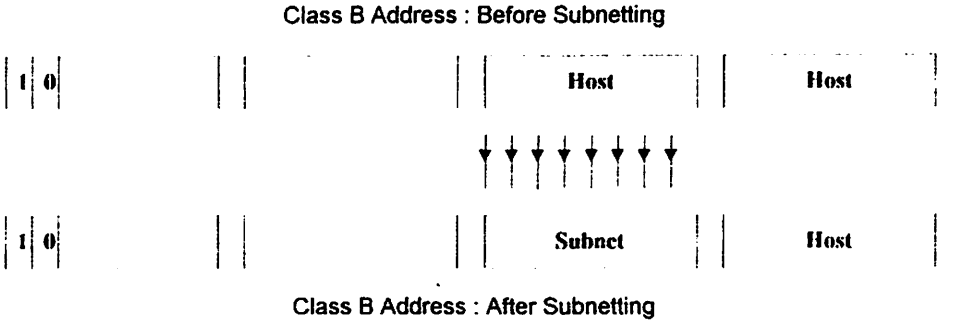
2.2.6.5. Pengalamatan Subnet IP

Jaringan IP dapat dibagi-bagi kedalam jaringan-jaringan yang lebih kecil disebut *subnetwork* (atau *subnet*). Dengan disubkan, jaringan memberikan beberapa keuntungan pada administrator jaringan, termasuk fleksibilitas ekstra, penggunaan *address* jaringan yang lebih efisien, dan kemampuan untuk membatasi lalulintas *broadcast* (*broadcast* tidak akan melintasi sebuah *router*).

Subnet berada dibawah administrasi lokal. Sedemikian sehingga, "dunia luar " melihat sebuah organisasi sebagai sebuah jaringan tunggal dan tidak mengetahui detil struktur internal organisasi.

Sebuah *address* jaringan dapat dipecah-pecah menjadi banyak *subnetwork*. Sebagai contoh, 172.16.1.0, 172.16.2.0, 172.16.3.0 dan 172.16.4.0.

Sebuah *address* subnet diciptakan dengan "meminjam" bit-bit dari *field* host dan menempatkannya sebagai *field* subnet. Jumlah bit yang dipinjam bervariasi dan ditentukan dengan subnet *mask*. Gambar 2-15 menunjukkan bagaimana bit-bit dipinjam dari *field address host* untuk menciptakan *field address* subnet.



Gambar 2-15 Pengalamatan Subnet IP
Sumber : Matthew G. Naugle, 1998:707

Subnet mask menggunakan format dan teknik represetasi yang sama denagn penalamatan IP. Subnet mask, karenanya, memiliki nilai binary 1 pada semua bitnya, untuk menunjukkan *field network* dan *subnetwork*, dan nilai *binary* 0 pada semua bitnya untuk menunjukkan *field host*. Gambar 2.16 menggambarkan sebuah contoh subnet *mask*.

	Network	Network	Subnet	Host
Binary Representation	11111111	11111111	11111111	00000000
Dotted Decimal Representation	255 .	255 .	255 .	0

Gambar 2-16 Contoh Subnet Mask
Sumber : Matthew G. Naugle, 1998:707

Bit-bit subnet mask harus dimulai dari *high-order* bit dari *field host*, seperti yang digambarkan dalam Gambar 2.17. berikut detil tipe-tipe subnet *mask* untuk Class B dan C

128	64	32	16	8	4	2	1	
1	0	0	0	0	0	0	0	= 128
1	1	0	0	0	0	0	0	= 192
1	1	1	0	0	0	0	0	= 224
1	1	1	1	0	0	0	0	= 240
1	1	1	1	1	0	0	0	= 248
1	1	1	1	1	1	0	0	= 252
1	1	1	1	1	1	1	0	= 254
1	1	1	1	1	1	1	1	= 255

Gambar 2.17.

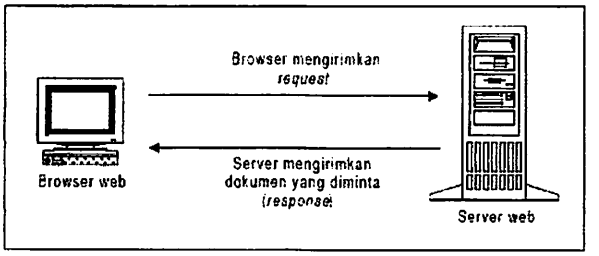
Beberapa Tipe Subnet Mask untuk Class B dan C
Sumber : Matthew G. Naugle, 1998:708

2.2.7 WORLD WIDE WEB

Pada awalnya *internet* adalah sebuah proyek yang dimaksudkan untuk menghubungkan para ilmuwan dan peneliti di Amerika, namun ini telah tumbuh menjadi media komunikasi global yang dipakai semua orang di muka bumi. Pertumbuhan ini membawa beberapa masalah penting mendasar, diantaranya kenyataan bahwa *Internet* tidak diciptakan pada jaman *Graphical User Interface* (GUI) seperti saat ini, *Internet* dimulai pada masa dimana orang masih menggunakan alat – alat akses yang tidak *user – friendly* yaitu terminal berbasis teks serta perintah – perintah *command line* yang panjang – panjang serta sukar diingat, sangat berbeda dengan komputer dewasa ini yang menggunakan klik tombol mouse pada layar grafik berwarna.

Kemudian orang berpikir untuk membuat sesuatu yang lebih baik. Popularitas *Internet* mulai berkembang pesat seperti jamur di musim penghujan setelah standar baru yaitu HTTP dan HTML diperkenalkan kepada masyarakat. HTTP (*Hypertext Transfer Protocol*) membuat pengaksesan informasi melalui protokol TCP/IP menjadi lebih mudah dari sebelumnya. HTML (*Hypertext Markup Language*) memungkinkan orang menyajikan informasi yang secara visual lebih menarik. Pemunculan HTTP dan HTML kemudian membuat orang mengenal istilah baru dalam *internet* yang sekarang menjadi sangat populer, bahkan sedemikian populernya sehingga sering dianggap identik dengan *internet* itu sendiri, yaitu *World Wide Web* (WWW).

Pada prinsipnya *World Wide Web* (singkatan cukup disebut "*web*" saja) bekerja dengan cara menampilkan *file–file* HTML yang berasal dari *server web* pada program *client* khusus, yaitu *browser web*. Program *browser* pada *client* mengirimkan permintaan (*request*) kepada *server web*, yang kemudian akan dikirimkan oleh *server* dalam bentuk HTML. *File* HTML berisi instruksi – instruksi yang diperlukan untuk membentuk tampilan. Perintah–perintah HTML ini kemudian diterjemahkan oleh *browser web* sehingga isi informasinya dapat ditampilkan secara visual kepada pengguna di layar komputer.



Gambar 2.18

Konsep Dasar Browser Dan Server Web

Sumber : Onno W Purbo, 2001:5

2.2.7.1. HTML (HYPERTEXT MARKUP LANGUAGE)

HTML (*HyperText Markup Language*) merupakan suatu metode untuk mengimplementasikan konsep hypertext dalam suatu naskah atau dokumen. HTML sendiri bukan tergolong pada suatu bahasa pemrograman karena sifatnya yang hanya memberikan tanda (*marking up*) pada suatu naskah teks dan bukan sebagai program. Berdasarkan kata-kata penyusunnya HTML dapat diartikan lebih dalam lagi menjadi :

A. Hypertext

Link *hypertext* adalah kata atau frase yang dapat menunjukkan hubungan suatu naskah dokumen dengan naskah-naskah lainnya. Jika kita klik pada kata atau frase untuk mengikuti *link* ini maka *web browser* akan memindahkan tampilan pada bagian lain dari naskah atau dokumen yang kita tuju.

B. Markup

Pada pengertiannya di sini markup menunjukkan bahwa pada file HTML berisi suatu intruksi tertentu yang dapat memberikan suatu format pada dokumen yang akan ditampilkan pada *World Wide Web*.

C. Language

Meski HTML sendiri bukan merupakan bahasa pemrograman, HTML merupakan kumpulan dari beberapa instruksi yang dapat digunakan untuk mengubah-ubah format suatu naskah atau dokumen. Pada awalnya HTML dikembangkan sebagai subset SGML (*Standard Generalized Mark-up Language)*. Karena HTML didedikasikan untuk ditransmisikan melalui media Internet, maka HTML relatif lebih sederhana daripada SGML yang lebih ditekankan pada format dokumen yang berorientasi pada aplikasi.

2.2.7.2 HYPERTEXT TRANSFER PROTOCOL (HTTP)

Web merupakan terobosan baru sebagai teknologi sistem informasi yang menghubungkan data dari banyak sumber dan layanan yang beragam macamnya

di *internet*. Pengguna tinggal mengklikkan tombol mousenya pada link – link *hypertext* yang ada untuk melompat ke dokumen – dokumen di berbagai lokasi si *internet*. Link – linknya sendiri bisa mengacu kepada dokumen *web*., *server* FTP (*File Trasfer Protokol*), e-mail ataupun layanan – layanan lain.

Server dan *browser web* berkomunikasi satu sama lain dengan protokol yang memang dibuat khusus untuk ini, yaitu HTTP. HTTP bertugas menangani permintaan – permintaan (*request*) dari *browser* untuk mengambil dokumen – dokumen *web*.

HTTP bisa dianggap sebagai sistem yang bermodel *client-server. Browser web*, sebagai *client*nya, mengirimkan permintaan kepada *server web* untuk menentukan apakah dokumen yang diminta bisa dikirimkan kepada *browser* atau tidak.

HTTP bekerja di atas *Transmission Control Protocol* (TCP) yang menjamin sampainya data di tujuan dalam urutan yang benar. Bila suatu kesalahan terjadi selama proses pengiriman, pihak pengirim akan mendapat pemberitahuan bahwa telah terjadi ketidakberesan. Karenanya *server* dan *client* tidak harus menyediakan mekanisme untuk memeriksa kesalahan transmisi data, yang berarti mempermudah pekerjaan pemrograman. Namun demikian, HTTP tidak memiliki apa yang disebut *session*, seperti halnya FTP, yang menjaga hubungan antara *server* dan *client* secara konsisten. Setiap halaman *web* yang dikirim akan melibatkan satu proses penyambungan antara *client* dan *server*, baru kemudian datanya ditransfer. Setelah data selesai ditransfer, koneksi antara *server* dan *client*

akan diputus. Sifatnya ini membuat HTTP sering disebut dengan istilah protokol *hit-and-run.*

Suatu halaman *web* seringkali berisi bebrapa *file* gambar, atau beberapa *file–file* lain. HTTP memaksa *server* untuk menjalin hubungan baru setiap kali hendak mengirim satu buah *file.* Ini tidak menguntungkan dan tidak efisien, mengingat proses hubung-putus-hubung semacam ini menyebabkan beban bagi jaringan.

Standar baru protokol HTTP, yaitu HTTP/1.1 yang baru-baru ini diperkenalkan, dirancang untuk mengatasi masalah di atas. *Web* diarahkan agar mengarah ke pengguna *persistent connection* (sambungan yang terjaga berkesinambungan) secara lebih efisien. Dalam HTTP/1.1, *server* tidak akan memutuskan hubungan dengan *client* pada akhir pentransferan dokumen. Hubungan tetap terbuka untuk melayani bila saja ada *request* lagi dalam waktu yang singkat. Hubungan baru akan diputuskan bila setelah melewati suatu batas waktu tertentu (yang bisa ditentukan oleh administrator *server*) *client* tidak mengirimkan *request* lagi.

Keuntungan lain dari *persisten connection* adalah penggunaan *pipelining. Pipelining* adalah proses pengiriman *request* berikutnya segera setelah *request* sebelumnya dikirimkan tanpa menunggu balasan dari *server* terlebih dahulu. *server*nya tetap harus melayani setiap *request* secara berurutan, namun ini mengurangi waktu tunda antara setiap *request.* Hasilnya, data akan lebih cepat sampai di tujuan.

Standar HTTP/1.1 ini sekarang sudah mulai dimasyarakatkan dan banyak paket perangkat lunak *server web* komersial dan non-komersial yang sudah mendukung standar baru ini. *Browser-browser web* keluaran terbaru umumnya juga sudah mendukung HTTP/1.1.

HTTP/1.1 sendiri memiliki beberapa metode dalam pengoperasiannya berikut beberapa metode yang dipakai dalam HTTP/1.1 :

1. **Request HTTP**

   Untuk meminta sebuah halaman atau data tertentu disisi *server*, *browser* harus mengirimkan sebuah request (permintaan) melalui protokol HTTP. Format dari *request* HTTP sebagai berikut;

   [request-line]

   [headers]

   [blank line]

   [request-body]

   Di request HTTP, baris pertama mengindikasikan tipe dari *request*, resource yang akan diakses, dan versi HTTP yang digunakan. Kemudian bagian *headers*, mengindikasikan informasi tambahan yang mungkin digunakan di *server*. Setelah *headers* yaitu baris kosong, yang kemudian dapat ditambahkan data tambahan (disebut *body*).

2. **Request GET**

   Ketika mengetikkan URL di *browser web*, *browser* mengirimkan *request* GET ke *server* berdasarkan URL tersebut, yang kemudian

memberitahukan *server* untuk mendapatkan *resource* dan mengirimkan balik. Berikut adalah contoh dari request GET untuk http://www.itn .ac.id

GET /images/ HTTP/1.1

Host: www.itn.ac.id

User-Agent: Mozilla/5.0 (Windows; U; Windows NT5.1; en-US; rv: 1.7.6)

Gecko/20050225 Firefox/1.0.1

Connection: Keep-Alive

3. Request POST

Pada request POST ditambahkan data tambahan yang dikirmkan ke *server* yang terletak di bagian *body request*. Misalnya, ketika kita mengisi suatu *form* isian, maka data dikirimkan melalui request POST.

Contohnya:

POST / HTTP/1.1

Host: www.itn.ac.id

User-Agent: Mozilla/5.0 (Windows; U; Windows NT 5.1; en-US; rv:1.7.6)

Gecko/20050225 Firefox/1.0.1

Content-Length: 40

Connection: Keep-Alive

Name=seminarITN&tahun=2007

4. Response HTTP

Setelah proses *request* dilakukan, *server* akan memberikan balasan atau response melalui protokol http juga. Format *response* HTTP mirip dengan request, yaitu:

[status-line]

[headers]

[blank line]

[response-body]

Status umum yang digunakan antara lain:

- 200 (OK) : *Request* yang kita minta dibalas dengan baik oleh *server*
- 304 (NOT MODIFIED) : Tidak ada perubahan *request* yang diberikan sejak request terakhir, hal ini disebabkan karena mekanisme *caching* oleh *browser*
- 401 (UNAUTHORIZED) : *Client* tidak berhak mengakses halaman ini, hal ini disebabkan karena *request* membutuhkan *username* dan *password* dan *user* tidak memberikannya
- 403 (FORBIDDEN) : *Client* tidak berhak untuk mengakses halaman ini, hal ini disebabkan karena *request* membutuhkan *username* dan *password* dan *user* memiliki *username* atau *password* yang tidak *valid*

2.2.6.8 BROWSER DAN SERVER WEB

Dalam dunia *web*, perangkat lunak *client*, yaitu *browser web* mempunyai tugas yang sama yaitu menterjemahkan informasi yang diterima dari *server web* dan menampilkannya pada layar komputer pengguna. Oleh karena HTTP memungkinkan *server web* mengirimkan beragam data, seperti teks atau gambar, *browser* harus bisa mengenali berbagai macam data yang akan diterimanya, dan selanjutnya harus tahu cara untuk menampilkannya dengan benar. Teks harus ditampilkan sebagai teks dan gambar harus ditampilkan sebagai gambar.

Umumnya *browser web* menerima data dalam bentuk HTML. *File* HTML sebenarnya adalah *file* teks biasa yang selain berisi informasi yang hendak ditampilkan kepada pengguna, juga mempunyai perintah – perintah untuk mengatur tampilan data tersebut, *Browser* lah yang memiliki kuasa penuh dalam menerjemahkan perintah – perintah tadi. Meskipun sudah dibuat konsensus untuk menstandarkan format dan elemen-elemen HTML, setiap jenis *browser* bisa menterjemahkan *file* HTML yang sama secara berbeda.

Pada awal pertama kalinya protokol-protokol dasar *web* dikembangkan yaitu sekitar awal 1990-an, *browser web* pertama yang diperkenalkan adalah Mosaic yang dibuat oleh *National Center for Supercomputing Applications* (NCSA) di Amerika Serikat. Mosaic dimaksudkan agar menjadi sebuah *interface* grafis yang mudah dipergunakan, yang dengan demikian diharapkan dapat mempercepat perkembangan dan dukungan umum akan *web*. Mosaic langsung dibuat untuk tiga macam *platform* berbeda, yaitu X Window (untuk lingkungan

UNIX dan keluarganya), Microsoft Windows dan Macintosh. Mosaic inilah yang lalu dianggap sebagai legenda yang memacu revolusi *web* menjadi sedemikian populernya seperti sekarang ini.

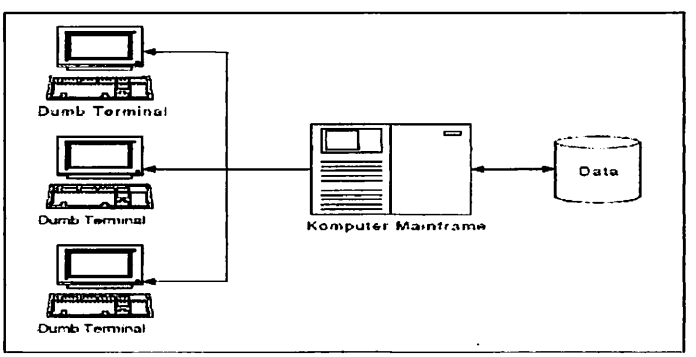
Perkembangan jaman serta semakin populernya lingkungan GUI (*Graphical User Interface*) membuat banyak orang sekarang berlomba-lomba membuat program *browser* yang menarik serta mudah dipakai. *Browser-browser web* modern dilengkapi dengan fasilitas-fasilitas yang mendukung tampilan multimedia berupa *audio* (suara), animasi 3 dimensi, bahkan video. Program *browser web* yang paling terkenal saat ini adalah Opera dan Microsoft *Internet* Explorer.

Sementara itu *server web* pada dasarnya adalah perangkat lunak khusus yang bertugas melayani permintaan-permintaan dari *browser web* akan dokumen-dokumen yang tersimpan di dalamnya. Perangkat lunak *server web* sekarang tersedia untuk berbagai macam *platform* dan lingkungan sistem operasi untuk lingkungan UNIX, yang paling populer adalah Apache, Netscape FastTrack, O'Reilly *Website* dan banyak lagi. Sistem operasi jaringan Novell Netware pun memiliki suatu modul *add-on* yang berfungsi sebagai *server web*, yang bisa dijalankan pada saat *startup* jaringan.

Beberapa perangkat lunak *server web* mempunyai *feature* seperti *server side programming, security control* dan lain sebagainya. Meskipun beragam macamnya, secara fungsional semua jenis *server web* adalah sama saja, yaitu berfungsi melayani permintaan-permintaan dari *browser web*.

2.2.6.9. INTERNET SEBAGAI SISTEM CLIENT/SERVER

Istilah *client/server* dewasa ini telah demikian populer. Keuntungan utama dari sistem berbasis *client/server* adalah bahwa perangkat keras dan perangkat lunak bisa ditempatkan di mana saja mereka bisa bekerja secara lebih optimal. Dulu, di jaman komputer *mainframe*, komputer *mainframe*-lah yang menjadi pusat kendali dan mengerjakan semua proses komputasi. Pengguna berinteraksi dengan sistem *mainframe* melalui terminal – terminal yang dibutuhkan secara langsung ke komputer *mainframe.* Terminal-terminal ini tidak punya kemampuan pemrosesan sama sekali, dan oleh karena itu disebut "terminal dungu" (*dumb terminal*). Termianl dungu tidak lebih dari sekedar perpanjangan kabel untuk keyboard dan layar monitor, dan hanya berfungsi sebagai alat untuk memasukkan dan melihat data saja.



Gambar 2.19

Konsep Sistem Mainframe

Sumber : Onno W Purbo, 2001:7

Definisi yang banyak dipergunakan untuk menjelaskan sistem berbasis *client/server* adalah "sistem yang memisahkan antara tugas-tugas komputasi antara proses-proses *client* dan *serve* ". Dengan sistem *client/server*, kekuatan pemrosesan bisa disebarkan (didistribusikan) ke banyak mesin *client* dan mesin *server* yang terpisah secara fisik (itu sebabnya disebut *distributed system*).

Misalnya sebuah *server web* yang mengambil informasi dari *database* menampilkan hasilnya pada *client* dengan menggunakan *broser web*. *server web* dan *database* bisa saja ditempatkan pada sutu mesin saja, namun apabila jumlah *client* yang melakukan akses ke *server* semakin banyak dan melebihi kapasitas mesin *server*, perangkat lunak *database* dan *server web* bisa saja dipisahkan dan ditempatkan di mesin kedua, ketiga atau bahkan lebih. Dengan begitu pemrosesan pada sisi *server* dapat disebarkan ke beberapa mesin, yang memungkinkan efisiensi komputasi. Begitu pula, dengan cara ini, kapasitas *server* bisa dikembangkan dan ditingkatkan sesuai dengan kebutuhan.

Dari susut pandang lain, sistem berbasis *client/server* juga bisa memanfaatkan *browser web* untuk meringankan kerja *server*. Tugas menampilkan informasi dan menyediakan tampilan pengguna (user interface) tidak perlu dilakukan secara langsung oleh *server*, namun diserahkan sepenuhnya kepada *browser web*. Dengan hadirnya teknologi pemrograman *client-side* (yang dijalankan di sisi *client*) seperti Java dan bahasa *client-scripting* seperti Javascript, fungsi – fungsi lain seperti pemeriksaan /validasi input bisa dilakukan oleh *browser* sebelum data dikirimkan kepada *server*, menjamin data yang

dikirimkan ke *server* tidak keliru. Hal ini mempercepat kerja *server*, karena hanya mengerjakan tugas-tugas yang berguna.

Konsep dasar sistem berbasis *clint-server* adalah *balancing* (penyebaran), yaitu proses yang mencegah suatu prosesor mengalami overload (terbeban lagi) sementara mesin lainnya justru menganggur .

Jadi, setidaknya dalam teori, sistem berbasis *client/server* memberikan keuntungan yang banyak seperti penggunaan resource secara lebih efisien, penyimpanan data terpusat, serta lalu lintas di dalam jaringan menjadi lebih rendah (dibandingkan dengan sistem yang seluruhnya terpusat). Satu-satunya kelemahan utama dari sistem berbasis *client/server* adalah manajemen dan perawatan mesin-mesin *client* yang membutuhkan *upgrading* serta proses konfigurasi yang memakan waktu dan tenaga. Semua program *client*, misalnya front-end untuk suatu *database*, harus dipasang satu persatu di setiap komputer *client*, dan apabila pada suatu saat program *client* tersebut harus diubah atau dikembangkan, prosesnya harus diulang di setiap komputer *client*.

Bagaimana dengan *Internet*, dalam hal ini *web*? Sebenarnya, secara mudah kita bisa mengatakan bahwa konsep *web* pada awalnya bisa dipandang mirip dengan konsep jaringan dengan *dump terminal*; pengguna *browser web* mengirimkan permintaan ke *server web*, lalu menerima informasi dari *server* berupa dokumen statis yang oleh *browser* hanya perlu ditampilkan saja ke layar. Meskipun kommputer *client* memiliki prosesor sendiri, memori sendiri serta media penyimpanan sendiri, sifat-sifat alami *browser web* sebenarnya memenuhi

syarat-syarat sebagai *dumb terminal*. Oleh karana *browser web* mempunyai kemampuan untuk membentuk *user interface* (tampilan pengguna) yang sifatnya grafis, sebagian orang menyebutnya sebagai *"smart dumb terminal"* (terminal dungu yang cerdas, atau tidak terlalu dungu).

Struktur fisik dari *Internet* sendiri juga tidak berbeda jauh dari sistem *mainframe*. *Bandwidth* (lebar jalur) besarnya terbatas. Tidak seperti teknologi lokal (LAN) seperti Ethernet atau Token Ring yang bisa membawa informasi sampai 10 bahkan 100 Mbps, kebanyakan pengguna *Internet* masih terbatas pada sambungan berorde kilobit per detik. Perusahaan-perusahaan besar mungkin sanggup menyewa sambungan kapasitas besar seperti T1 (1,55 Mbps) ke *internet*, namun kebanyakan pengguna yang lebih kecil aatau rumah tangga hanya mempunyai sambungan berkecepatan rendah, sekitar 33 – 56 Kbps. Bahkan teknologi ISDN pun (yang masih saat ini masih tergolong mahal) jarang melampaui 128 Kbps.

Melihat kenyatan bahwa pada mesin-mesin yang menjalankan *browser* pada umumnya adalah komputer-komputer modern yang memiliki potensi pemrosesan dan penyimpanan data yang cukup besar, mesin-mesin *client* seharusnya bisa mengerjakan lebih banyak pekerjaan lagi. Juga, tidak seperti sistem berbasis *client/server* "tradisional", kenyatan bahwa penggunaan *browser web* nyaris tidak membutuhkan perawatan yang mahal, *upgrade* berkala dan konfigurasi yang rumit, membuat *web* (dan *Internet* pada umumnya) menjadi tempat yang menarik untuk mengembangkan sistem berbasis *client/server*.

Dari sisi pengelola jaringan, sistem berbasis *web* mengundang banyak perhatian karena sistem semacam ini bisa mengatasi banyak kekurangan dari sistem-sistem konvensional. Pada intinya, mengembangkan sistem *client/server* di *web* membawa keuntungan-keuntungan langsung seperti :

1. **Tidak ada masalah distribusi program**

   Pendistribusian berlangsung secara sendirinya, karan setiap salinan dokumen (sebagai satu komponen aplikasi) di-*download* ke mesin *client* setiap saat mesin *client* membutuhkan dan meminta *update* atau salinan yang lebih baru. Tidak perlu lagi seorang administrator jaringan meng-*install* perangkat lunak *client* untuk setiap komputer yang ada di organisasinya, suatu pekerjaan yang melelahkan dan memboroskan waktu.

2. **Efisien**

   Distribusi otomatis dan tidak perlunya instalasi untuk setiap *client* jelas mempermudah perawatan dan *updating* aplikasi. Perubahan-perubahan pada aplikasi bisa dikerjakan secara terpusat dan bisa langsung diterapkan tanpa perlu menyesuaikan semua *client.* Bahkan tampilan pada pengguna bisa diubah – ubah secara berkala sisesuaikan dengan waktu dan situasi.

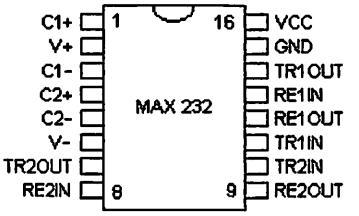
3. **Fleksibel**

   Browser web tersedia untuk hampir semua macam *platform* mesin dan sistem operasi, baik itu mesin Windows berbasis prosesor Intel, mesin UNIX berbasis prosesor RISC, ataupun komputer Macintosh. Fleksibilitas aplikasi

web lebih terjamin, karena tidak perlu lagi mengembangkan program-program *client* yang berbeda untuk tiap macam *platform.*

2.3. RANGKAIAN PENGUBAH LEVEL TEGANGAN

Kita menggunakan RS232 untuk komunikasi dengan *ethernet* dan *mikrokontroler* secara serial maka dibutuhkan piranti tambahan berupa IC LVTTL MAX3232CPE untuk menyesuaikan level tegangan *ethernet* yakni +3,3V, sedangkan untuk *mikrokontroler* pada sisi Driver Relay memerlukan sebuah piranti yang berfungsi sebagai pengubah level tegangan maka digunakan IC MAX232CPE untuk Level tegangan yang lebih tinggi yaitu +5V. RS232 menggunakan level/karakteristik elektrik yang berbeda dengan level TTL. RS232 bekerja pada level tegangan +3 s/d +25 Volt untuk *space (logic 0)* dan -3 s/d -25 Volt untuk *mark (logic 1).* Sedangkan TTL bekerja pada level tegangan -5 s/d +5 Volt. Piranti tambahan yang kita butuhkan adalah IC MAX232. Pada dasarnya IC ini hanya digunakan sebagai pengubah level tegangan ke level *Transistor Transistor Logic* (TTL), tidak berfungsi sebagai pengkodean sinyal yang melewati RS232, dan juga tidak mengkonversikan data serial ke paralel.



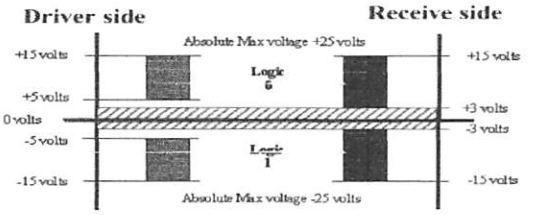
Gambar 2.20

IC MAX232/MAX3232 Sebagai Pengubah Level Tegangan

Sumber : Datasheet Maxim MAX232/MAX3232

RS232 sebagai komunikasi serial mempunyai 9 pin yang memiliki fungsi masing-masing. Pin yang biasa digunakan adalah pin 2 sebagai *received data*, pin 3 sebagai *transmited data*, dan pin 5 sebagai *ground signal*. Karakteristik elektrik dari RS232 adalah sebagi berikut :

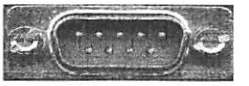
- *Space (logic 0)* mempunyai level tegangan sebesar +3 s/d +25 Volt.
- *Mark (logic 1)* mempunyai level tegangan sebesar -3 s/d -25 Volt.
- Level tegangan antara +3 s/d -3 Volt tidak terdefinisikan.
- Arus yang melalui rangkaian tidak boleh melebihi dari 500 mA., ini dibutuhlan agar sistem yang dibangun bekerja dengan akurat.



Gambar 2.21

Karakteristik Elektrik RS232

Sumber : Fundamental Of RS-232 Serial communications, 1998



Gambar 2.22

RS232 (Sebagai Komunikasi Serial)

Sumber : Fundamental Of RS-232 Serial communications, 1998

Tabel 2.2

Fungsi masing-masing pin RS232

RS232 Pin Assignments (DB9 PC signal set)	
Pin 1	*Received* Line Signal Detector (Data Carrier Detect)
Pin 2	*Received* Data
Pin 3	Transmit Data
Pin 4	Data Terminal Ready
Pin 5	Signal Ground
Pin 6	Data Set Ready
Pin 7	Request To Send
Pin 8	Clear To Send
Pin 9	Ring Indicator

Sumber : Fundamental Of RS-232 Serial communications, 1998

Keterangan Pin :

a. Pin 1 DCD (Data Carrier Detect)

   Akan bernilai high selama DCE menerima sinyal yang sesuai dengan kriteria sinyal yang sesuai

b. Pin 2 RXD (Receive Data)

Data yang ditransfer nilai *logic* 1 akan dikirimkan sebagai *low level* dan *logic* 0 dikirimkan sebagai *high level*

c. Pin 3 TXD (Transmit Data)

Data yang ditransfer nilai *logic* 1 akan dikirimkan sebagai *low level* dan *logic* 0 dikirimkan sebagai *high level*

d. Pin 4 DTR (Data terminal Ready)

Digunakan pada saat awal komunikasi antara DTE dan DCE telah terhubung untuk memastikan bahwa keduanya berada dalam keadaan telah siap untuk menerima dan mengirimkan data. Pertama kali DTR harus *high* dan kemudian akan dibalas dengan DSR yang bernilai *high*

e. Pin 5 GND (Signal Ground)

Sebagai referensi level tegangan untuk semua sinyal

f. Pin 6 DSR (Data Set Ready)

Digunakan pada saat awal komunikasi antara DTE dan DCE telah terhubung untuk memastikan bahwa keduanya berada dalam keadaan telah siap untuk menerima dan mengirimkan data. Pertama kali DTR harus *high* dan kemudian akan dibalas dengan DSR yang bernilai *high*

g. Pin 7 RTS (Request To Send)

Digunakan sebagai tanda utuk mengawali atau menghentikan komu

nikasi antara *host system* (DTE) dan pheriperal system (DCE), setelah DTE siap akan mengirimkan data maka RTS akan dibuat *high* yang kemudian DCE akan dibuat *high* agar pengiriman dapat segera dimulai

h. Pin 8 CTS (Clear To Send)

Digunakan sebagai tanda utuk mengawali atau menghentikan komu nikasi antara *host system* (DTE) dan *pheriperal system* (DCE), setelah DTE siap akan mengirimkan data maka RTS akan dibuat *high* yang kemudian DCE akan dibuat *high* agar pengiriman dapat segera dimulai

i. Pin 9 RI (Ring Indicator)

Digunakan untuk menandakan bahwa sinyal ring telah diterima

2.4. Mikrokontroler AT89S8252

Mikrokontroler *Atmel* AT89S8252 merupakan pengembangan dari mikrokontroler standart MCS-51. Hal-hal yang terdapat pada penjelasan mikrokontroler MCS-51 juga berlaku untuk mikrokontroler *Atmel AT89S8252.*

2.4.1. Fitur Mikrokontroler Atmel AT89S8252

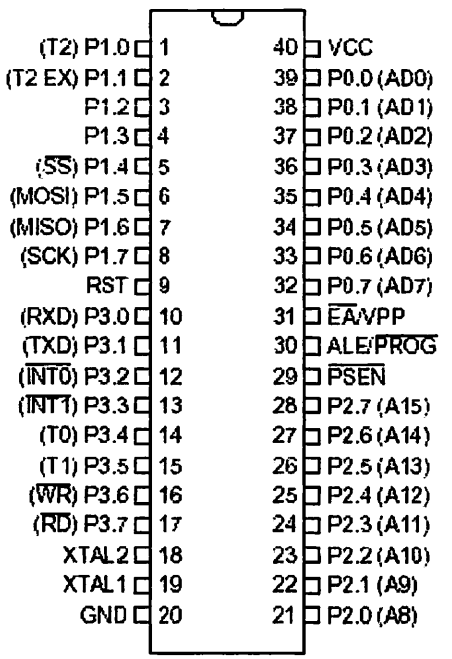
Mikrokontroler AT89S8252 merupakan pengembangan dari mikrokontroler standard MCS – 51, dengan banyak kelebihan yang ditawarkan antara lain :

- Kompatibel dengan Mikrokontroler MCS – 51
- 8K byte Downloadable Flash memori
- 2K byte EEPROM
- 3 level program memori lock
- 256 byte RAM internal
- 32 I/O yang dapat dipakai semua
- 3 buah timer / counter 16 bit
- Programmable watchdog timer
- Dual data pointer
- Frekuensi kerja 0 sampai 24 MHZ
- Tegangan operasi 2,7 – 6 volt

Dipakainya *downloadable flash* memori memungkinkan mikrokontroler ini bekerja sendiri tanpa diperlukan tambahan chip lainnya. Dan flash memori dapat diprogram hingga seribu kali. Hal lain yang menguntungkan adalah sistem pemrograman jauh lebih sederhana dan tidak memerlukan rangkaian yang rumit seperti rangkaian untuk memprogram AT89C51.

Timer / counter juga bertambah satu dari standar 2 buah pada MCS – 51. Selain itu frekuensi kerja yang lebar dan rancangan statik sangat membantu untuk proses *debugging*. Dengan adanya beberapa fitur tambahan itu, maka akan mengakibatka bertambahnya SFR (*Special Function Register*). Gambar berikut adalah gambar mikrokontroler AT 89S8252. Tata letak pin – pin ini masih

mengacu pada mikrokontroler MCS – 51 sehingga AT 89S8252 dapat menggantikan mikrokontoler MCS – 51.



Gambar 2.23 Mikrokontroler AT89S8252
Sumber: Data Sheet ATMEL AT89S8252

Keterangan pin :

a. Pin 40 (VCC)

   Merupakan pin catu daya dengan tegangan sebesar +5 V (DC)

b. Pin 20 (GND)

   Merupakan pin GROUND yang nanti terhubung dengan grounding rangkaian.

c. Pin 32 – 39 (Port 0)

   PORT 0 mempunyai fungsi sebagai port alamat dan data , maka jika mikrokontroler sedang mengakses alamat, P0 akan aktif

sebagai pembawa alamat 8 bit yang bawah (A0 – A8). Ketika mengakses data (bisa input atau output) port ini sebagai jalur data (D7 – D0).

d. Pin 21 – 28 (Port 2)

Port 2 berfungsi sebagai pembawa alamat 8 bit atas (A8 – A15). Berbeda dengan port 0, port ini tidak bersifat sebagai jalur data hanya sebagai pembawa alamat. Dengan demikian jelas bahwa untuk alamat AT89S8252 menyediakan 16 bit sedangkan untuk jalur data hanya 8 bit.

e. Pin 10 – 17 (port 3)

Port 3 ini mempunyai fungsi yang berlainan dari setiap pin-pinnya, seperti yang di tunjukkan di bawah ini:

- P 3.7: Kaki *read* yang aktif manakala sedang melakukan eksekusi yang sifatnya membaca data.
- P 3.6 : Kaki *write* yang aktif saat melakukan eksekusi yang sifatnya menulis data ke suatu alamat.
- P 3.5 : Merupakan pin yang berhubungan dengan timer register timer 1 (T1).
- P 3.4 : Merupakan pin yang berhubungan dengan timer register 0 (T0).
- P 3.3 : Berhubungan dengan control interupt (INT1).
- P 3.2 : Berhubungan dengan control interupt (INT0).

- P 3.1 : Berhubungan dengan port serial (TXD).
- P 3.0 : Berhubungan dengan port serial (RXD).

Untuk lebih jelasnya lihat daftar tabel dibawah ini :

Tabel 2.3 Konfigurasi Port 3 Atmel AT89S8252

Port Pin	Alternate Functions
P3.0	RXD (serial input port)
P3.1	TXD (serial output port)
P3.2	$\overline{\text{INT0}}$ (external interrupt 0)
P3.3	$\overline{\text{INT1}}$ (external interrupt 1)
P3.4	T0 (timer 0 external input)
P3.5	T1 (timer 1 external input)
P3.6	$\overline{\text{WR}}$ (external data memory write strobe)
P3.7	$\overline{\text{RD}}$ (external data memory read strobe)

Sumber: Data Sheet ATMEL AT89S8252

f. Pin 9 (RST (*Reset*))

Pin reset ini aktif tinggi (1), jika pin ini aktif tinggi minimal dua kali siklus mesin bekerja maka akan mereset peralatan.

g. Pin 30 (ALE/PROG (*Address Latch Enable/Program*))

Pin ALE ini aktif tinggi dengan mengeluarkan pulsa output untuk melatch (mengunci/menahan) 1 byte alamat rendah selama mengakses ke alamat memori eksternal. ALE dapat mengendalikan 8 beban TTL dan juga merupakan input program yang aktif rendah selama pemrograman *Flash Eprom.* Pada operasi normal, ALE

dikeluarkan pada suatu kecepatan yang konstan yaitu 1/6 dari frekuensi osilator, dan juga dapat dipergunakan untuk pewaktu atau timing eksternal atau untuk pemberian clock.

h. Pin 29 (PSEN (*Program Strobe Enable*))

   Pin ini aktif rendah, yang merupakan pulsa pengaktif untuk pembacaan ke program memori eksternal.

i. Pin 19 (XTAL - !)

   Sebagai pin input ke penguat osilator pembalik dan input rangkaian clock internal untuk operasi system.

j. Pin 18 ((XTAL – 2)

   Pin output dari penguat osilator.

k. Pin 31 (EA/VPP (*Externall Access/Program Supplay Voltage*))

   Pin ini harus di tahan dalam kondisi rendah secara eksternal atau dihubungkan ke-*ground* agar AT 89S8252 dapat mengakses kode mesin dari memori eksternal. Jika menggunakan internal program memori maka pin ini harus diberi logika tinggi (1).

Semua pin pada mikrokontroler AT89S8252 adalah sama dengan mikrokontroler MCS – 51. Namun pada port 1 mikrokontroler AT89S8252 terdapat beberapa fungsi khusus yang tidak terdapat pada mikrokontoler MCS – 51. Fungsi khusus tersebut dijelaskan pada tabel berikut :

Tabel 2.4. Fungsi khusus pada Port 1 Atmel 89S8252

Port PIN	**Fungsi Khusus**
P 1.0	T2 (masukan luar untuk timer / counter 2)
P 1.1	T2 EX (timer / counter capture / reload trigger dan control arah)
P 1.2	-
P 1.3	-
P 1.4	SS (*slave port select input*)
P 1.5	MOSI (master data ouput, slave dan input untuk kanal SPI)
P 1.6	MISO (master data input, slave data output untuk kanal SPI)
P 1.7	SCK (master clock output, slave clock input untuk kanal SPI)

Sumber: Data Sheet ATMEL AT89S8252

2.4.2. SFR tambahan pada Atmel AT89S8252

Selain memiliki SFR(*Special Function Register*) seperti halnya pada MCS-51, mikrokontroler Atmel AT89S8252 memiliki tambahan SFR. Hal ini tak lain adalah karena adanya fitur tambahan pada mikrokontroler Atmel AT89S8252.

SFR tambahan ini meliputi: T2CON(Timer 2 Register dangan alamat

0C8H), T2MOD(*Timer 2 Mode* dengan alamaat 0C9H), WMCON(*Watchdog and Memory Control Register* dengan alamat 96H), SPCR(*SPI Control Register* dengan alamat D5H), SPSR(*SPI Status Refister* dengan alamat AAH), SPDR(SPI Data Register dengan alamat 86H).

2.4.3. Data Memory (EEPROM) dan RAM

Berbeda dengan mokrokontroler standart MCS-51, mikrokontroler Atmel AT89S8252 juga dilengkapi dengan data memori yang berupa EEPROM (*Electrically Erasable Programmable Read Only Memory*). EEPROM yang ditanamkan ini besarnya 2 kilo byte (2K) dan dipakai untuk penyimpanan data.

EEPROM ini diakses dengan mengeset bit EEMEN pada registerWMCON pada alamat 96H. Alamat EEPROM ini adalah 000H sampai 7FFH. Instruksi movx digunakan untuk mengakses EEPROM internal ini. Namun jika ingin mengakses data memori luar (diluar mikrokontroler Atmel AT89S8252) dengan menggunakan instruksi movx ini maka bit EEMEN harus dibuat"0".

Bit EEMWE pada register WMCON harus diset ke 1 sebelum sembarang lokasi padaEEPROM dapat ditulisi. Program pengguna harus mereset bit EEMWE ke "0" jika proses penulisan ke EEPROM tidak diperlukan lagi. Proses penulisan pada EEPROM dapat dilihat dengan membaca bt RDY/BSY pada SFR WMCON. Jika bit ini berlogika rendah maka penulisan EEPROM sedang berlangsung, jika bit ini berlogika tinggi maka penulisan sudah selesai dan penulisan lain dapat dimulai lagi. Sedangkan RAM yang ada pada mikrokontroler

Atmel AT89S8252 adalah berkapasitas 256 byte. Penjelasan mengenai RAM ini adalah sama dengan RAM yang ada pada mikrokontroler standart MCS-51.

2.4.4. Programable Watchdog Timer (WDT)

Pada mikrokontroler Atmel AT89S8252 juga dilengkapi oleh *watchdog Timer* ini menggunakan detak tersendiri. Untuk mengatur rentang waktu(perioda) pada WDT ini maka terdapat bit prescaler yang dapat mengatur rentang waktru yang dibutuhkan.

Bit prascaler ini adalah bit PS0, PS1dan PS2 pada register WMCON. Perioda waktu pada WDT ini berkisar dari 16 mili detik sampai 2048 mili detik. Karena bit prescalernya ada 3, maka akan ada 8 buah kemungkinan yaitu:

Tabel 2.5. Pemilihan Perioda Waktu WDT

PS2	PS1	PS0	Perioda
0	0	0	16 ms
0	0	1	32 ms
0	1	0	64 ms
0	1	1	128 ms
1	0	0	256 ms
1	0	1	512 ms
1	1	0	1024 ms
1	1	1	2048 ms

Sumber: Data Sheet ATMEL AT89S8252

WDT dilumpuhkan oleh Power on Reset (POR) dan selama Power Down. WDT diaktifkan dengan menseting bit WDTEN pada SFR WMCON (alamat 96H). Jika perhitungan waktu WDT telah selesai tanpa ada reset atau dilumpuhkan, maka suatu pulsa reset internal akan dihasilkan untuk mereset CPU.

2.4.5. Timer 2

Pada mikrokontroler Atmel AT89S8252 terdapat tambahan *Timer* 2. *Timer* yang lain adalah *timer* 0 dan *timer* 1. Hal yang perlu diperhatikan adalah *Timer/Counter* dapat digunakan sebagai generator *baudrate* untuk serial *port.* Pada standart MS-51 biasanya yang digunakan adalah *timer* 1 sebagai penghasil *baudrate.* Pada mikrokontroler Atmel AT89S8252 selain menggunakan *timer* 1 sebagai *baudrate* (untuk menjaga kompabilitas dengan MCS-51) juga dapat menggunakan *Timer* 2 sebagai penghasil *baudrate* untuk serial *port. Timer* 2 ini merupakan Timer/Counter yang berukuran 16 bit yang dapat beroperasi sebagai timer atau dapat beroperasi sebagai penghitung kejadian dengan detak dari luar. Untuk mengatur fungsi ini dilakukan dengan mengatur bit C/T2 pada SFR T2CON. Terlihat bahwa jika bit ini tinggi maka akan terpilih fungsi *counter*, tapi jika bit ini rendah maka akan terpilih fungsi *Timer* 2. *Timer* 2 ini memiliki 3 mode operasi yaitu: *capture, auto reload (up dan down counting)* dan *baud rate* generator. Untuk memilih mode ini dilakukan dengan mengatur bit pada SFR T2CON.

Timer 2 ini terdiri dari 2 buah *timer* 8 bit *register* yaitu TH2 dan TL2 dinaikkan tiap siklus mesin. Karena siklus mesin terdiri dari 1 *periode* osilasi, maka *count rate* menjadi 1/12 dari frekuensi osilator.

Pada fungsi *counter, register* dinaikkan berdasarkan tanggapan adanya transisi tinggi ke rendah pada pena yang bersesuaian (dalam hal ini pin T2 atau Pi.0). pada fungsi ini, masukan luar akan disampling selama S5P2 dari tiap siklus mesin. Jika hasil sampling menunjukkan logika tinggi pada selama satu siklus dan logika rendah pada siklus selanjutnya maka akan terdeteksi transisi tinggi ke rendah dan akibatnya perhitungan akan dinaikkan. Nilai perhitungan yang baru akan muncul pada register selama S3P1 dari siklus setelah transisi tinggi ke rendah terdeteksi.

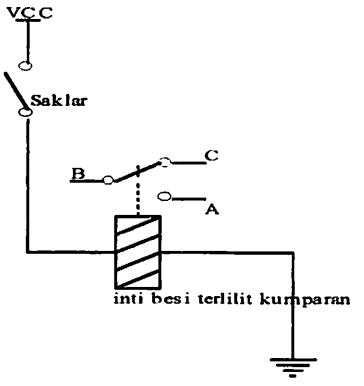
Tabel 2.6. Mode Operasi Timer 2

RCLK+TCLK	CP/RL2	TR2	MODE
0	0	1	16 bit auto reload
0	1	1	16 bit capture
1	X	1	Baud rate generator
X	X	0	Off

Sumber: Data Sheet ATMEL AT89S8252

2.3. Relay

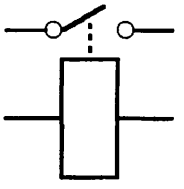
Relay adalah komponen elektronika yang terdiri dari sebuah lilitan kawat (kumparan/koil) yang terlilit pada sebuah besi lunak. Jika kumparan dialiri arus listrik maka inti besi akan menjadi magnet dan menarik pegas sehingga kotak AB terhubung dan BC terputus.



Gambar 2.24 Cara Kerja Relay
Sumber: IEI Surabaya, 1992:5

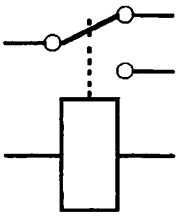
Relay merupakan suatu alat untuk menghubungkan atau memutuskan kontak antara komponen yang satu dengan yang lain. Dalam memutus atau menghubungkan kontak digerakkan oleh *fluksi* yang ditimbulkan dari adanya medan magnet listrik yang dihasilkan oleh kumparan yang melilit pada besi lunak. Ada beberapa macam relay, antara lain:

- SPST *(Single Pin Single Terminal)*



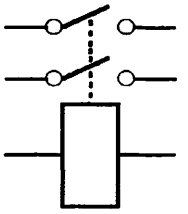
Gambar 2.25 Relay SPST
Sumber: IEI Surabaya, 1992:6

- SPDT *(Single Pin Dual Terminal)*



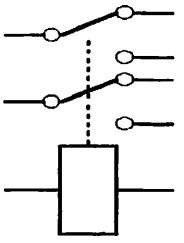
Gambar 2.26 Relay SPDT
Sumber: IEI Surabaya, 1992:6

- DPST *(Dual Pin Single Terminal)*



Gambar 2.27 Relay DPST
Sumber: IEI Surabaya, 1992:7

- DPDT *(Dual Pin Dual Terminal)*



Gambar 2.28 Relay DPDT
Sumber: IEI Surabaya, 1992:7

Relay yang umum digunakan saat ini adalah relay jenis elektro mekanis yang terdiri atas kumparan yang jika mendapat bias arus akan dapat

mengendalikan kontak penghubung. Kontak yang ada pada relay ada dua macam yaitu:

1. Kontak Terbuka (*Normally Open*)

   Adalah relay yang tidak bekerja apabila kontaknya terbuka.

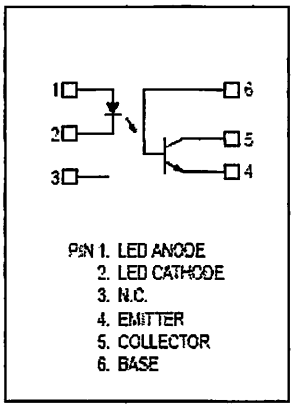
2. Kontak Tertutup (*Normally Close*)

   Adalah relay yang akan bekerja apabila kontaknya terhubung.

2.5. Optocoupler (4N35)

Optocoupler disebut juga optoisolator merupakan gabungan dari LED (pada sisi input) dan Photodioda (pada sisi output) dalam satu kemasan. Fungsi dari optocupler adalah mengisolasi antara satu bagian rangkaian dengan bagian rangkaian yang lain. Tujuan dari pengisolasian ini adalah untuk mencegah agar tidak terjadi kerusakan komponen pada suatu bagian sebagai akibat dari munculnya tegangan tinggi yang tidak diinginkan pada bagian lainnya.

Keuntungan pokok dari optocoupler adalah terjadinya isolasi elektrik antara satu rangkaian input dan output. Dengan optocoupler, hanya terdapat kontak input dan output dalam bentuk pancaran sinar. Oleh karena itu, dimungkinkan untuk mengisolasi resistansi antara dua rangkaian dalam orde ribuan megaohm. Isolasi yang seperti itu berguna dalam aplikasi tegangan tinggi dimana beda potensial dua rangkaian sampai dengan ribuan volt. [Malvino, 2003:171]. Dalam tugas akhir ini digunakan optocoupler 4N35 yang dapat mengisolasi tegangan sampai dengan 5300 volt pada sisi photodioda.



Gambar 2.29 Konfigurasi Pin 4N35
Sumber : Motorolla DataSheet, 1999

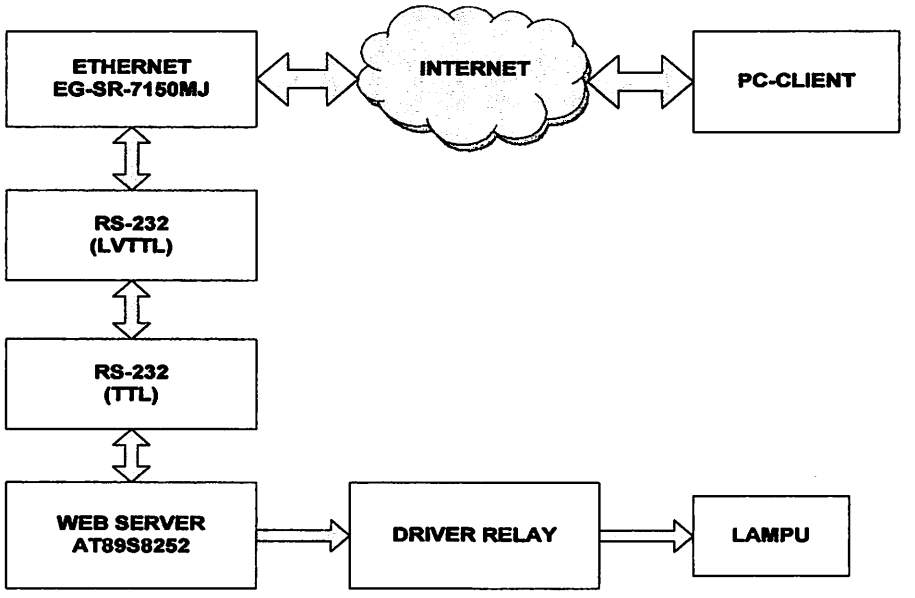
BAB III

PERENCANAAN DAN PEMBUATAN ALAT

Pada Bab ini akan dibahas mengenai peralatan yang direncanakan dan akan direalisasikan sebagaimana fungsinya. Adapun perencanaan dan pembuatan alat meliputi perencanaan dan pembuatan perangkat keras serta perencanaan dan pembuatan perangkat lunak secara garis besarnya.

3.1. Perencanaan Dan Pembuatan Perangkat Keras

3.1.1. Diagram Blok



Gambar 3.1. Blok Diagram Keseluruhan Sistem

Fungsi dari tiap blok adalah sebagai berikut :

1. **PC-CLIENT** merupakan bagian yang bertugas untuk memanggil alamat IP dari ethernet dalam hal ini local IP dari ethernet EG-SR7150MJ
2. **INTERNET** merupakan bagian daripada jaringan yang menghubungkan antara PC-Client dengan ethernet EG-SR-7150MJ dan Web server
3. **ETHERNET EG–SR–7150MJ** merupakan bagian yang bertugas sebagai Ethernet gateway ke serial
4. **RS-232(LVTTL)** merupakan bagian yang berfungsi sebagai antarmuka serial yang bekerja pada level tegangan +3.3Vpada sisi Ethernet
5. **RS-232(TTL)** merupakan bagian yang berfungsi sebagai antarmuka serial yang bekerja pada level tegangan +5V pada sisi Web server
6. **WEB SERVER (AT89S8252)** merupakan bagian yang berfungsi sebagai database untuk melayani setiap permintaan dari PC-CLIENT
7. **DRIVER RELAY** bagian ini berfungsi sebagai pengendali untuk mematikan dan menghidupkan lampu
8. **LAMPU** bagian yang berfungsi sebagai penerang yang ditempatkan di rumah atau perkantoran

3.1.2. Prinsip Kerja Alat

Pada prinsipnya kerja alat ini adalah tergantung dari permintaan PC-Client pada saat PC-Client *On-Line* dan terhubung ke jaringan, dalam perancangan ini jaringan yang digunakan hanya terbatas pada jaringan lokal saja atau LAN(lokal area *network*) namun realisasinya bisa dipakai dalam jaringan internet yang sebenarnya, ketika PC-Client *On-Line* dan sistem pada bagian unit *web server* ON

maka selanjutnya *PC-Client* akan melakukan pemanggilan alamat dalam hal ini lokal IP address dari ethernet gateway EG-SR-7150MJ, tentu dibutuhkan sebuah web browser dan yang digunakan adalah *Internet Explorer* untuk memasukkan alamat tersebut, alamat IP *Address*-nya sendiri adalah *http;// 192.168.11.2/B10,* ketika alamat IP tersebut sudah betul maka web browser melalui protokol HTTP akan mengirimkan request GET pada *Web Server* berdasarkan alamat IP, yang kemudian memberitahukan *Web Server* untuk mendapatkan *resource* dan mengirimkan balik ke *web browser.*

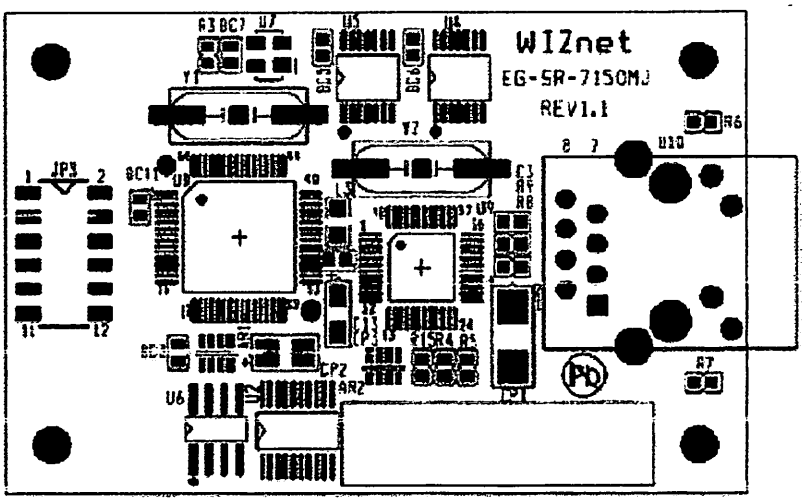
Kemudian pada halaman web yang ada kita akan dihadapkan oleh link-link yang dialamatkan pada web server, seperti contoh link *nyalakan lampu 1* dengan alamat IP *http;// 192.168.11.2/B11* bilamana link ini di klik maka browser akan mengirimkan request GET sesuai link yang diminta dan web server dalam hal ini mikrokontroler akan mengkondisikannya pada logic "1"(aktif *high*) untuk mengaktifkan driver *relay* disamping itu web server juga mengirim balik informasi berupa status dari masing-masing lampu.

3.1.3. Perancanaan dan Pembuatan Modul Ethernet EG-SR-7150MJ

3.1.3.1. Perancangan Penggunaan Port-Port Pada Modul Ethernet EG-SR-7150MJ

Pada skripsi ini Modul Ethernet EG-SR-7150MJ berfungsi sebagai ethernet gateway serial ke TCP/IP atau TCP/IP ke serial yang menjembatani antara web server(AT89S252) dengan jaringan LAN. Pada modul ethernet ini ada beberapa port yang mesti di pakai dengan seksama sesuai dengan kegunaannya yang terdiri dari port LAN RJ-45 dan port serial sebagai I/O.

Gambar 3.2 menunjukkan rancangan *port-port* I/O serta sinyal-sinyal pada Modul Ethernet EG-SR-7150MJ dan terintegrasi di dalamnya IC mikrokontroler AT89C51RC2 yang dimanfaatkan pada skripsi ini.



Gambar 3.2. Pemakaian PIN pada port Serial dari Modul EG-SR-7150MJ

JP3

/RESET - 1	2 - 3.3V
RXD - 3	4 - 3.3V
CTS - 5	6 - /FACTORY_RESET
TXD - 7	8 - /HW_TRIGGER
RTS - 9	10 - /PSEN
GND - 11	12 - GND

Gambar 3.3. Keterangan dari JP3

- Pin 1, /RESET

  Input reset pada pin 10 adalah reset master untuk AT89C51RC2

- Pin 2/4, VCC (+3.3V)

Modul ethernet ini di operasikan dengan tegangan supply +3.3V dan pin VCC berada pada pin 2,22,39,38,58 untuk Chip Wiznet W3150+ dan untuk AT89C51RC2 sendiri pin Vcc berada pada pin 38

- Pin 3, RXD *(Port 3.0 dari IC AT89C51RC2)*

  Pin 3/Port 3.0 merupakan port yang berada pada pin 11 dari IC AT89C51RC2. Dalam perancangan, P3.0 digunakan sebagai port input serial.

- Pin 5, CTS *(Clear To Send)*

  Pin 5 merupakan port yang digunakan dalam mengendalikan arah data yang masuk

- Pin 6, /FACTORY_ RESET

  Pin 6 merupakan port yang digunkan sebagai sebagai reset untuk mengembalikan setingan *default* dari ethernet EG-SR-7150MJ.

- Pin 7, TXD *(Port 3.1 dari IC AT89C51RC2)*

  Pin 7/Port 3.0 dalam perancangan ini P3.0 berada pada pin 13 dari IC AT89C51RC2 dan dalam perencanaannya, P3.0 digunakan sebagai output serial

- Pin 8, /HARDWARE TRIGGER

  Pin 8 merupakan port yang digunakan sebagai command mode serial.

- Pin 9.RTS *(Request To Send)*

  Pin 9 merupakn port yang digunakan dalam mengendalikan arah data yang keluar

- Pin 10,/PSEN *(Program Strore Enable)*

/PSEN adalah suatu sinyal keluaran yang terdapat pada pin 32. Fungsinya adalah sebagai sinyal kontrol untuk memungkinkan mikrokontroler membaca program (code) dari memori eksternal. Jika eksekusi program dari ROM internal (8051/8052) atau dari *flash* memori AT89C51RC2 , maka */PSEN* berada pada kondisi tidak aktif *(high).*

- Pin 11/12, GND (Ground)

  Pin 11 dan pin 12 adalh pin yang digunakan sebagai ground, dalam modul ini untuk Chip Wiznet W3150+ berada pada pin 3,13,23,36,45,54 sedangkan untuk AT89C51RC2 Gnd berada pada pin 16.

3.1.4. Antarmuka Serial RS-232(LVTTL) dan RS-232(TTL)

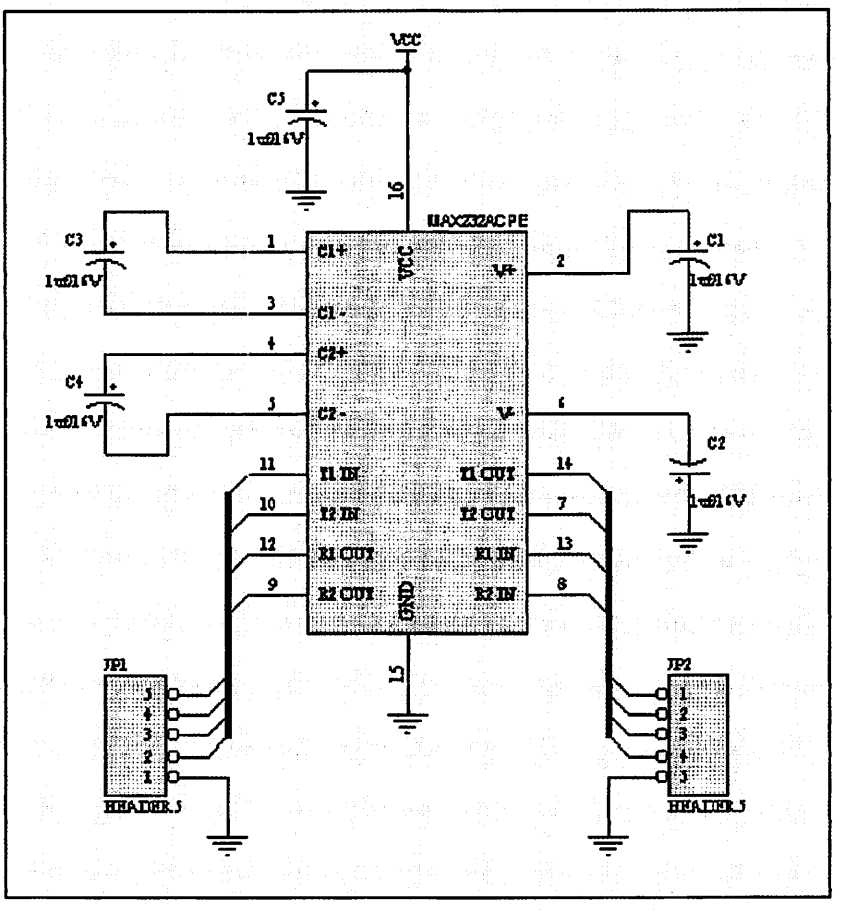
Sebagai penghubung antara ethernet EG-SR-7150MJ dengan mikrokontroler AT89S8252 adalah RS-232 yang konfigurasinya terdiri dari IC MAX 3232 untuk LVTTL dan MAX 232 untuk TTL keduanya sangat berperan dalam penyesuaian level tegangan yang diminta untuk ethernet sendiri pada bagian serialnya membutuhkan level signal tegangan +3.3V maka dipakai IC dari MAXIM yaitu MAX 3232, sedangkan untuk level tegangan yang lebih besar dipakai IC MAX 232 yang beroperasi pada level tegangan +5V untuk bisa berkomunikasi dengan Mikrokontroler AT89S8252, IC MAX232CPE sebagai pengubah level tegangan ini mempunyai 2 *receivers* yang berfungsi sebagai pengubah level tegangan dari level RS232 ke level *Voltage Transistor Transistor Logic* (TTL) dan mempunyai 2 *drivers* yang berfungsi mengubah level tegangan dari level *TTL* ke level RS232. Pasangan *driver*/receiver ini digunakan untuk *TX* dan *RX* , sedangkan pasangan yang lainnya digunakan untuk *CTS* dan *RTS.*

Tabel 3.1

Konfigurasi Pin IC MAX232CPE

Nbr	Name	Purpose	Signal Voltage
1	C1+	+ connector for capacitor C1	capacitor should stand at least 16V
2	V+	output of voltage pump	+10V
3	C1-	+ connector for capacitor C1	capacitor should stand at least 16V
4	C2+	+ connector for capacitor C2	capacitor should stand at least 16V
5	C2-	- connector for capacitor C2	capacitor should stand at least 16V
6	V-	output of voltage pump / inverter	-10V
7	$T2_{out}$	Driver 2 output	RS-232
8	$R2_{in}$	Receiver 2 input	RS-232
9	$R2_{out}$	Receiver 2 output	TTL
10	$T2_{in}$	Driver 2 input	TTL
11	$T1_{in}$	Driver 1 input	TTL
12	$R1_{out}$	Receiver 1 output	TTL
13	$R1_{in}$	Receiver 1 input	RS-232
14	$T1_{out}$	Driver 1 output	RS-232
15	GND	Ground	0V
16	Vcc	Power supply	+5V

Dalam pembuatan rangkaian, IC MAX232 memerlukan beberapa kapasitor. Kami menggunakan kapasitor sebesar 0.1 μF dengan tegangan 16 Volt pada beberapa kaki pin. IC ini memerlukan input +5 Volt.



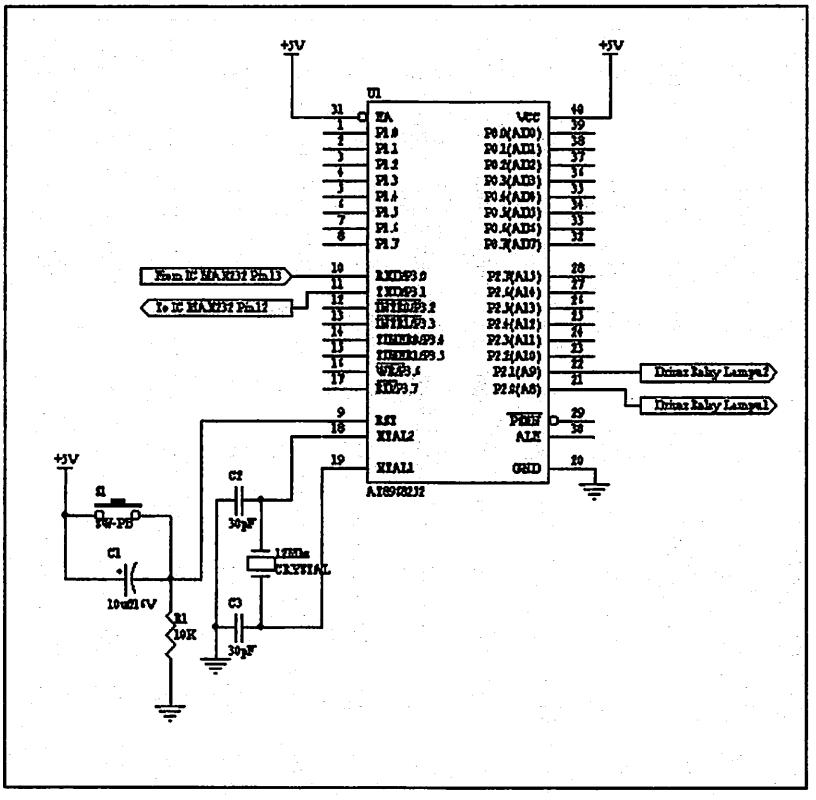
Gambar 3.3. Rangkaian Pengubah Level Tegangan RS-232

Ada 4 kapasitor yang digunakan dalam rangkaian ini yaitu pada pin 1 (+) dengan pin 3 (-), pin 4 (+) dengan pin 5 (-), pin 2 (+) dengan pin 16 (-). Untuk pin 6, karena bertegangan -10 Volt maka terhubung dengan kaki kapasitor (-) sedangkan *Ground* (+). Koneksi antara IC MAX232 dengan RS232 terhubung melalui pin 14 *(driver 1 output)* yaitu sebagai *Tx (transmitter)* dengan DB9 pin2 *(received data)* dan pin 13 *(receiver 1 input)* sebagai *Rx (receiver)* dengan DB9 pin 3 *(transmitted data)*. Sedangkan pin 12 dan pin 13 menuju ke *mikrokontroller.* ketentuan dan data teknis diatas juga berlaku untuk IC MAX3232 yang ditempatkan disisi Ethernet EG-SR7150MJ hanya saja pada IC MAX3232 level tegangannya berada pada +3,3V atau LVTTL.

3.1.3.1. Perancangan Penggunaan Port-Port Pada Mikrokontroler AT89S8252

Pada skripsi ini IC mikrokontroler AT89S8252 digunakan sebagai pusat pengendali kerja dari alat yang dibuat karena pada IC inilah akan disimpan program-program *(software)* perintah serta alamat yang akan dituju program. Untuk melaksanakan fungsi tersebut diatas maka perlu dirancang *port-port* I/O serta sinyal-sinyal yang akan digunakan dengan seksama.

Gambar 3.2 menunjukkan rancangan port-port I/O serta sinyal-sinyal pada IC mikrokontroler AT89S8252 yang dimanfaatkan pada skripsi ini.



Gambar 3.2. Pemakaian *Port-Port* Mikrokontroler AT89S8252.

- Port 2

  Port 2 merupakan *port* dua fungsi yang berada pada pin 21-22 dari IC AT89S8252. Dalam perancangan, P2.0-P2.1 digunakan sebagai *port* keluaran ke *Driver relay* 1-2.

- Port 3

  Port 3 dalam perancangan ini P3.0(RXD), P3.1(TXD), dengan pin 10, dan pin 11, digunakan sebagai I/O untuk antarmuka serial MAX 232.

- $\overline{PSEN}$ *(Program Strore Enable)*

  $\overline{PSEN}$ adalah suatu sinyal keluaran yang terdapat pada pin 29. Fungsinya adalah sebagai sinyal kontrol untuk memungkinkan mikrokontroller membaca program (code) dari memori eksternal. Jika eksekusi program dari ROM internal (8051/8052) atau dari flash memori AT89S8252 , maka $\overline{PSEN}$ berada pada kondisi tidak aktif (high).

- ALE *(Address Latch Enable)*

  Sinyal output ALE yang berada pada pin 30 fungsinya untuk demultipleks bus alamat dan bus data. Sinyal ALE membangkitkan pulsa sebesar 1/6 frekwensi oscilator dan dapat dipakai sebagai clock yang dipergunakan secara umum.

- $\overline{EA}$ *(External Access)*

  Masukan sinyal $\overline{EA}$ terdapat pada pin 31 yang dapat diberikan logika rendah (pin terhubung ground) atau logika tinggi (pin terhubung Vcc). Jika $\overline{EA}$ diberikan logika tinggi, maka mikrokontroller akan mengakses program dari ROM internal (EPROM/flash memory). Jika $\overline{EA}$ diberikan

logika rendah, maka mikrokontroller akan mengakses program dari memori eksternal. Pada skripsi ini $\overline{EA}$ dihubungkan ke Vcc

- RST *(Reset)*

  Input reset pada pin 9 adalah reset master untuk AT89S8252.

- Oscilator

  Oscilator yang disediakan pada chip dikemudikan dengan XTAL yang dihubungkan pada pin 18 dan pin 19. Besar nilai XTAL yang digunakan sebesar 11,0592 MHz untuk keluarga MCS-51, dan diperlukan dua buah kapasitor penstabil sebesar 30pF.

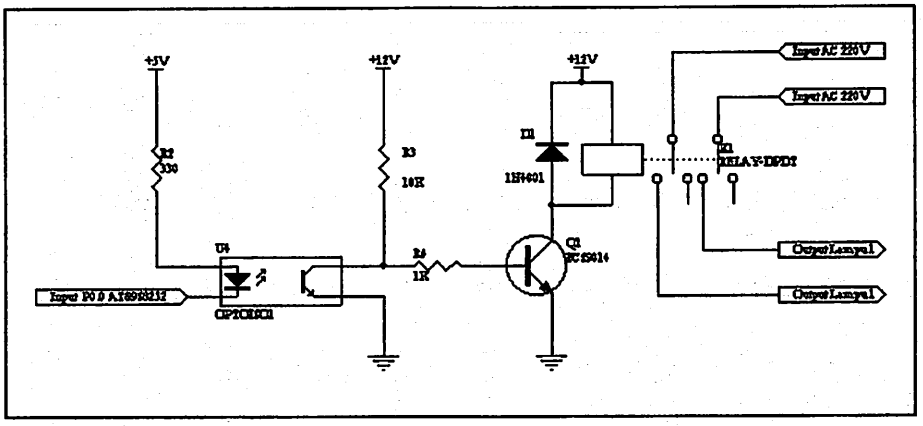
- Vcc

  AT89S8252 dioperasikan dengan tegangan supply +5V. Pin Vcc berada pada pin nomor 40 yang dipararel dengan EA/VPP pada pin 31, sedangkan Vss (ground) pada AT89S8252 berada pada pin 20.

3.1.5. Driver Relay

Rangkaian driver berfungsi untuk mengaktifkan lampu yang nantinya akan menerangi suatu ruangan. Pada perancangan ini terdiri dari sebuah *optocoupler* 4N35. Pemasangan *optocoupler* berfungsi sebagai penahan *bouncing* yang muncul akibat kelebihan arus yang ditimbulkan oleh beban, sehingga dapat menyebabkan mikrokontroler menjadi rusak baik secara fisik maupun non fisik (program di dalam mikrokontroler itu sendiri). Walaupun sebenarnya *bouncing* itu sendiri telah diantisipasi dengan memasang sebuah diode yang terpasang paralel dengan *relay*-nya sebelum masuk ke beban. Namun masih muncul juga *bouncing* yang dapat merusak mikrokontroler, sehingga dengan memasang sebuah

optocoupler dapat mencegah terjadinya *bouncing*. Untuk lebih jelasnya rangkaian driver ini dapat dilihat pada gambar 3.5.



Gambar 3.5. Rangkaian *Driver Relay.*

Langkah perancangan dan pemilihan komponen yang dipakai adalah:

- Menentukan arus nominal relay yang digunakan, dan didapatkan nilai arus nominal sebesar 76.4 mA pada tegangan 12 Volt (sesuai nilai pengukuran yang didapat).
- Nilai arus relay sebesar 76.4 mA adalah sebagai arus *collector* (Ic) pada transistor.
- Transistor pada rangkaian driver ini berfungsi sebagai saklar. Transistor yang dipakai adalah C9014 jenis NPN bekerja pada keadaan aktif *high*, jika logika "1" maka transistor akan tertutup sehingga arus mengalir dari Vcc sebagai arus *collector*(Ic) ke relay dan sebaliknya. Transitor ini mempunyai konstanta tipikal (β) = 150
- Logika "1" keluaran mikrokontroler AT89S8252 sebesar 5 Volt.

- Resistansi dalam *relay* (Rd) adalah sebesar 157 Ω (berdasarkan hasil pengukuran).
- Besarnya tegangan LED pada *optocoupler* adalah 1.15 Volt, berdasarkan pada data sheet.

Dalam perancangan driver relay ini arus yang diperlukan untuk menggerakkan relay sama dengan arus yang mengalir pada *collector*, sehingga besarnya arus pada *collector* adalah:

$$Ic = \frac{Vcc}{Rd}$$

$$Ic = \frac{12}{157}$$

$$= 76.4 \text{ mA.}$$

Maka besarnya *Ib* adalah sebagai berikut:

$$Ib = \frac{Ic}{\beta}$$

$$Ib = \frac{76.4}{150}$$

$$= 5{,}09 \text{ mA.}$$

Sehingga arus yang mengalir pada *relay* (*Ic=Irelay)* = 76.4 mA.

Berdasarkan analisa rangkaian didapatkan besarnya *Rb* adalah:

$$Ib = \frac{Vbb - Vbe}{Rb}$$

maka,

$$Rb = \frac{Vbb - Vbe}{Ib}$$

$$Rb = \frac{5 - 0.7}{5.09}$$

$$= 844.7 \ \Omega.$$

Karena di pasaran tidak ada nilai 844.7 Ω maka pada perencanaan ini dipilih *Rb* sebesar = 1 kΩ.

Untuk LED pada *optocoupler* digunakan resistor yang besarnya adalah:

$$R1 = \frac{Vcc - V_{LED}}{I_{LED}}$$

$$= \frac{5Volt - 3Volt}{60mA}$$

R1 = 333 Ω ≈333 Ω

Karena di pasaran tidak ada nilai 333 Ω, sehingga dipilih R1 sebesar 330 Ω.

3.2. Perancangan Perangkat Lunak (Software)

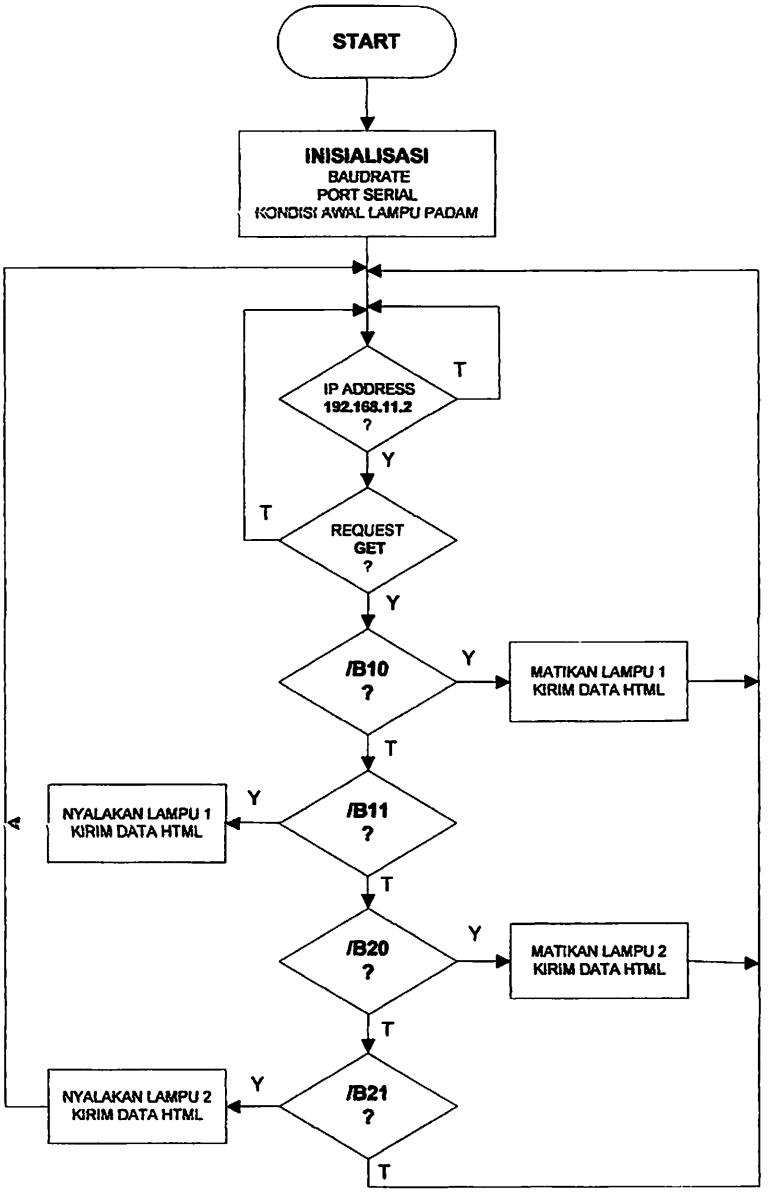
Untuk pemakaian mikrokontroler didalam suatu sistem, perlu direncanakan perangkat lunak mikrokontroller yang dapat mengatur system tersebut. Perangkat lunak disini adalah perintah-perintah (program) didalam memori yang harus dilaksanakan oleh mikrokontroler.

Didalam suatu mikrokontroller memori merupakan fasilitas utama karena disinilah disimpan perintah-perintah yang harus dikerjakan. Memori disini dapat dibedakan menurut fungsinya menjadi memori program dan memori data.

Perencanaan perangkat lunak *(software*) didasarkan perencanaan perangkat keras yang telah dibuat sebelumnya.

3.2.1. Flow Chart

Cara kerja dari perangkat lunak (*software*) secara umum sebagai berikut:



Gambar 3.7. Flowchart Keseluruhan Sistem.

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BAB IV

PENGUJIAN ALAT

4.1. Umum

Pengujian alat ini dilakukan untuk mengetahui kinerja dari keseluruhan sistem rangkaian. Jadi pada tahap ini akan diketahui nilai-nilai serta parameter-parameter dari setiap bagian yang menyusun sistem secara keseluruhan. Secara umum, pengujian ini bertujuan untuk mengetahui apakah piranti yang telah direalisasikan dapat bekerja sesuai dengan spesifikasi perencanaan yang telah ditetapkan. Pengujian yang dilakukan antara lain rangkaian Sistem Ethernet EG-SR-7150MJ, antarmuka RS-232, *Web Server* (AT89S8252), dan rangkaian *Driver Relay.*

4.2. Pengujian Perangkat Keras

4.2.1. Pengujian Modul Ethernet EG-SR-7150MJ

1. Tujuan.

Untuk mengetahui kondisi awal dari Ethernet EG-SR-7150MJ apakah sudah sesuai dengan yang direncanakan.

2. Peralatan Yang Dibutuhkan.

- Komputer (*PC-Client*).
- Antarmuka RS-232 (LVTTL).
- Modul Ethernet EG-SR-7150MJ.

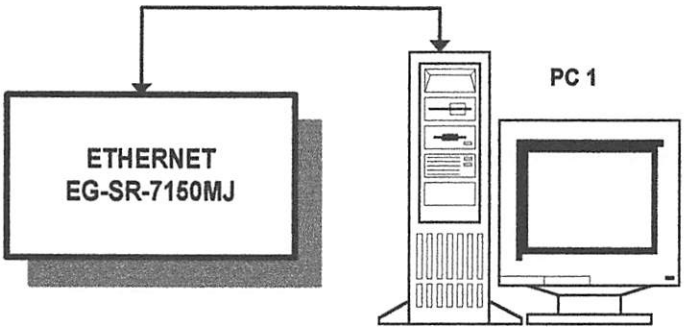
3. Prosedur Pengujian.

Pada pengujian ini ada 2 cara yang digunakan:

- Melakukan Ping pada Lokal IP dari Modul Ethernet EG-SR-7150MJ.
- Melakukan pengiriman HTTP/1.1 dengan request GET pada PC 1 kedalam bentuk data serial pada PC 2.

A. Langkah pengujian melakukan Ping pada lokal IP dari Modul Ethernet EG-SR-7150MJ.

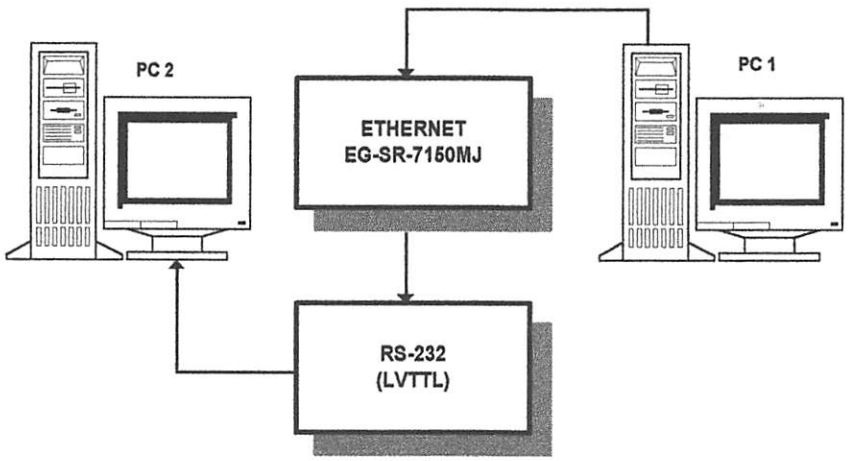
- Merangkai peralatan sesuai dengan gambar 4.1.
- Memasang catu daya modul Ethernet sebesar +3.3V.
- Menyiapkan program MS-DOS dan melakukan ping pada alamat Lokal IP Ethernet yakni 192.168.11.2.
- Mengamati hasil pengujian.



Gambar 4.1. Rangkaian Pengujian Modul Ethernet

B. Langkah pengujian dengan melakukan pengiriman HTTP/1.1 dengan *request* GET dari PC 1 kedalam bentuk data serial pada PC 2

- Merangkai peralatan yang digunakan sesuai dengan gambar 4.2
- Memasang catudaya Modul Ethernet dan rangkaian RS232(LVTTL) sebesar +3.3V.
- Menyiapkan dua buah PC.
- Memasang konektor DB-9 pada PC 2.
- Memasang konektor RJ-45 pada PC 1.
- Mnyiapkan Web Browser Internet Explorer pada PC 1.
- Menyiapkan program hyperterminal pada PC 2.



Gambar 4.2. Diagram Blok Pengujian Modul Ethernet

4. Hasil Pengujian

- Hasil pengujian dengan melakukan ping pada alamat lokal IP dari Ethernet

ome Port 1 pins provide additional functions. P1.0 and 1.1 can be configured to be the timer/counter 2 external ount input (P1.0/T2) and the timer/counter 2 trigger input 1.1/T2EX), respectively.

in Description

urthermore, P1.4, P1.5, P1.6, and P1.7 can be configured s the SPI slave port select, data input/output and shift ck input/output pins as shown in the following table.

rt Pin	Alternate Functions
.0	T2 (external count input to Timer/Counter 2), clock-out
1.1	T2EX (Timer/Counter 2 capture/reload trigger and direction control)
P1.4	SS (Slave port select input)
P1.5	MOSI (Master data output, slave data input pin for SPI channel)
P1.6	MISO (Master data input, slave data output pin for SPI channel)
P1.7	SCK (Master clock output, slave clock input pin for SPI channel)

ort 1 also receives the low-order address bytes during lash programming and verification.

ort 2

ort 2 is an 8-bit bi-directional I/O port with internal pullups. he Port 2 output buffers can sink/source four TTL inputs. /hen 1s are written to Port 2 pins, they are pulled high by ie internal pullups and can be used as inputs. As inputs, ort 2 pins that are externally being pulled low will source urrent (I_{IL}) because of the internal pullups.

ort 2 emits the high-order address byte during fetches om external program memory and during accesses to xternal data memory that use 16-bit addresses (MOVX @ PTR). In this application, Port 2 uses strong internal pul- ips when emitting 1s. During accesses to external data emory that use 8-bit addresses (MOVX @ RI), Port 2 nits the contents of the P2 Special Function Register.

ort 2 also receives the high-order address bits and some ontrol signals during Flash programming and verification.

ort 3

ort 3 is an 8 bit bi-directional I/O port with internal pullups. he Port 3 output buffers can sink/source four TTL inputs. /hen 1s are written to Port 3 pins, they are pulled high by e internal pullups and can be used as inputs. As inputs, Port 3 pins that are externally being pulled low will source current (I_{IL}) because of the pullups.

Port 3 also serves the functions of various special features of the AT89S8252, as shown in the following table.

Port 3 also receives some control signals for Flash programming and verification.

Port Pin	Alternate Functions
P3.0	RXD (serial input port)
P3.1	TXD (serial output port)
P3.2	$\overline{INT0}$ (external interrupt 0)
P3.3	$\overline{INT1}$ (external interrupt 1)
P3.4	T0 (timer 0 external input)
P3.5	T1 (timer 1 external input)
P3.6	$\overline{WR}$ (external data memory write strobe)
P3.7	$\overline{RD}$ (external data memory read strobe)

RST

Reset input. A high on this pin for two machine cycles while the oscillator is running resets the device.

ALE/$\overline{PROG}$

Address Latch Enable is an output pulse for latching the low byte of the address during accesses to external memory. This pin is also the program pulse input ($\overline{PROG}$) during Flash programming.

In normal operation, ALE is emitted at a constant rate of 1/6 the oscillator frequency and may be used for external timing or clocking purposes. Note, however, that one ALE pulse is skipped during each access to external data memory.

If desired, ALE operation can be disabled by setting bit 0 of SFR location 8EH. With the bit set, ALE is active only during a MOVX or MOVC instruction. Otherwise, the pin is weakly pulled high. Setting the ALE-disable bit has no effect if the microcontroller is in external execution mode.

$\overline{PSEN}$

Program Store Enable is the read strobe to external program memory.

When the AT89S8252 is executing code from external program memory, $\overline{PSEN}$ is activated twice each machine cycle, except that two $\overline{PSEN}$ activations are skipped during each access to external data memory.

$\overline{EA}$/VPP

External Access Enable. $\overline{EA}$ must be strapped to GND in order to enable the device to fetch code from external pro-

am memory locations starting at 0000H up to FFFFH. ote, however, that if lock bit 1 is programmed, $\overline{EA}$ will be ernally latched on reset.

$\overline{A}$ should be strapped to V_{CC} for internal program execu- ns. This pin also receives the 12-volt programming iable voltage (V_{PP}) during Flash programming when 12- lt programming is selected.

XTAL1

Input to the inverting oscillator amplifier and input to the internal clock operating circuit.

XTAL2

Output from the inverting oscillator amplifier.

ble 1. AT89S8252 SFR Map and Reset Values

F8H								0FFH
0H	B 00000000							0F7H
JE8H								0EFH
0E0H	ACC 00000000							0E7H
0D8H								0DFH
0D0H	PSW 00000000					SPCR 000001XX		0D7H
0C8H	T2CON 00000000	T2MOD XXXXXX00	RCAP2L 00000000	RCAP2H 00000000	TL2 00000000	TH2 00000000		0CFH
0C0H								0C7H
0B8H	IP XX000000							0BFH
0B0H	P3 11111111							0B7H
0A8H	IE 0X000000		SPSR 00XXXXXX					0AFH
0A0H	P2 11111111							0A7H
98H	SCON 00000000	SBUF XXXXXXXX						9FH
90H	P1 11111111						WMCON 00000010	97H
88H	TCON 00000000	TMOD 00000000	TL0 00000000	TL1 00000000	TH0 00000000	TH1 00000000		8FH
80H	P0 11111111	SP 00000111	DP0L 00000000	DP0H 00000000	DP1L 00000000	DP1H 00000000	SPDR XXXXXXXX	PCON 0XXX0000	87H

Special Function Registers

A map of the on-chip memory area called the Special Function Register (SFR) space is shown in Table 1.

Note that not all of the addresses are occupied, and unoccupied addresses may not be implemented on the chip. Read accesses to these addresses will in general return random data, and write accesses will have an indeterminate effect.

User software should not write 1s to these unlisted locations, since they may be used in future products to invoke new features. In that case, the reset or inactive values of the new bits will always be 0.

Timer 2 Registers Control and status bits are contained in registers T2CON (shown in Table 2) and T2MOD (shown in Table 9) for Timer 2. The register pair (RCAP2H, RCAP2L) are the Capture/Reload registers for Timer 2 in 16 bit capture mode or 16-bit auto-reload mode.

Table 2. T2CON—Timer/Counter 2 Control Register

T2CON Address = 0C8H — Reset Value = 0000 0000B

Bit Addressable

Bit	7	6	5	4	3	2	1	0
	TF2	EXF2	RCLK	TCLK	EXEN2	TR2	C/$\overline{T2}$	CP/$\overline{RL2}$

Symbol	Function
TF2	Timer 2 overflow flag set by a Timer 2 overflow and must be cleared by software. TF2 will not be set when either RCLK = 1 or TCLK = 1.
EXF2	Timer 2 external flag set when either a capture or reload is caused by a negative transition on T2EX and EXEN2 = 1. When Timer 2 interrupt is enabled, EXF2 = 1 will cause the CPU to vector to the Timer 2 interrupt routine. EXF2 must be cleared by software. EXF2 does not cause an interrupt in up/down counter mode (DCEN = 1).
RCLK	Receive clock enable. When set, causes the serial port to use Timer 2 overflow pulses for its receive clock in serial port Modes 1 and 3. RCLK = 0 causes Timer 1 overflows to be used for the receive clock.
TCLK	Transmit clock enable. When set, causes the serial port to use Timer 2 overflow pulses for its transmit clock in serial port Modes 1 and 3. TCLK = 0 causes Timer 1 overflows to be used for the transmit clock.
EXEN2	Timer 2 external enable. When set, allows a capture or reload to occur as a result of a negative transition on T2EX if Timer 2 is not being used to clock the serial port. EXEN2 = 0 causes Timer 2 to ignore events at T2EX.
TR2	Start/Stop control for Timer 2. TR2 = 1 starts the timer.
C/$\overline{T2}$	Timer or counter select for Timer 2. C/$\overline{T2}$ = 0 for timer function. C/$\overline{T2}$ = 1 for external event counter (falling edge triggered).
CP/$\overline{RL2}$	Capture/Reload select. CP/$\overline{RL2}$ = 1 causes captures to occur on negative transitions at T2EX if EXEN2 = 1. CP/$\overline{RL2}$ = 0 causes automatic reloads to occur when Timer 2 overflows or negative transitions occur at T2EX when EXEN2 = 1. When either RCLK or TCLK = 1, this bit is ignored and the timer is forced to auto-reload on Timer 2 overflow.

Watchdog and Memory Control Register The WMCON register contains control bits for the Watchdog Timer (shown in Table 3). The EEMEN and EEMWE bits are used to select the 2K bytes on-chip EEPROM, and to enable byte-write. The DPS bit selects one of two DPTR registers available.

Table 3. WMCON—Watchdog and Memory Control Register

WMCON Address = 96H — Reset Value = 0000 0010B

Bit	PS2	PS1	PS0	EEMWE	EEMEN	DPS	WDTRST	WDTEN
	7	6	5	4	3	2	1	0

Symbol	Function
PS2 PS1 PS0	Prescaler Bits for the Watchdog Timer. When all three bits are set to "0", the watchdog timer has a nominal period of 16 ms. When all three bits are set to "1", the nominal period is 2048 ms.
EEMWE	EEPROM Data Memory Write Enable Bit. Set this bit to "1" before initiating byte write to on-chip EEPROM with the MOVX instruction. User software should set this bit to "0" after EEPROM write is completed.
EEMEN	Internal EEPROM Access Enable. When EEMEN = 1, the MOVX instruction with DPTR will access on-chip EEPROM instead of external data memory. When EEMEN = 0, MOVX with DPTR accesses external data memory.
DPS	Data Pointer Register Select. DPS = 0 selects the first bank of Data Pointer Register, DP0, and DPS = 1 selects the second bank, DP1
WDTRST RDY/$\overline{BSY}$	Watchdog Timer Reset and EEPROM Ready/$\overline{Busy}$ Flag. Each time this bit is set to "1" by user software, a pulse is generated to reset the watchdog timer. The WDTRST bit is then automatically reset to "0" in the next instruction cycle. The WDTRST bit is Write-Only. This bit also serves as the RDY/$\overline{BSY}$ flag in a Read-Only mode during EEPROM write. RDY/$\overline{BSY}$ = 1 means that the EEPROM is ready to be programmed. While programming operations are being executed, the RDY/$\overline{BSY}$ bit equals "0" and is automatically reset to "1" when programming is completed.
WDTEN	Watchdog Timer Enable Bit. WDTEN = 1 enables the watchdog timer and WDTEN = 0 disables the watchdog timer.

SPI Registers Control and status bits for the Serial Peripheral Interface are contained in registers SPCR (shown in Table 4) and SPSR (shown in Table 5). The SPI data bits are contained in the SPDR register. Writing the SPI data register during serial data transfer sets the Write Collision bit, WCOL, in the SPSR register. The SPDR is double buffered for writing and the values in SPDR are not changed by Reset.

Interrupt Registers The global interrupt enable bit and the individual interrupt enable bits are in the IE register. In addition, the individual interrupt enable bit for the SPI is in the SPCR register. Two priorities can be set for each of the six interrupt sources in the IP register.

Dual Data Pointer Registers To facilitate accessing both internal EEPROM and external data memory, two banks of 16 bit Data Pointer Registers are provided: DP0 at SFR address locations 82H-83H and DP1 at 84H-85H. Bit DPS = 0 in SFR WMCON selects DP0 and DPS = 1 selects DP1. The user should always initialize the DPS bit to the appropriate value before accessing the respective Data Pointer Register.

Power Off Flag The Power Off Flag (POF) is located at bit_4 (PCON.4) in the PCON SFR. POF is set to "1" during power up. It can be set and reset under software control and is not affected by RESET.

Table 4. SPCR—SPI Control Register

SPCR Address = D5H

Reset Value = 0000 01XXB

Bit	SPIE	SPE	DORD	MSTR	CPOL	CPHA	SPR1	SPR0
	7	6	5	4	3	2	1	0

Symbol	Function
SPIE	SPI Interrupt Enable. This bit, in conjunction with the ES bit in the IE register, enables SPI interrupts: SPIE = 1 and ES = 1 enable SPI interrupts. SPIE = 0 disables SPI interrupts.
SPE	SPI Enable. SPI = 1 enables the SPI channel and connects $\overline{SS}$, MOSI, MISO and SCK to pins P1.4, P1.5, P1.6, and P1.7. SPI = 0 disables the SPI channel.
DORD	Data Order. DORD = 1 selects LSB first data transmission. DORD = 0 selects MSB first data transmission.
MSTR	Master/Slave Select. MSTR = 1 selects Master SPI mode. MSTR = 0 selects Slave SPI mode.
CPOL	Clock Polarity. When CPOL = 1, SCK is high when idle. When CPOL = 0, SCK of the master device is low when not transmitting. Please refer to figure on SPI Clock Phase and Polarity Control.
CPHA	Clock Phase. The CPHA bit together with the CPOL bit controls the clock and data relationship between master and slave. Please refer to figure on SPI Clock Phase and Polarity Control.
SPR0 SPR1	SPI Clock Rate Select. These two bits control the SCK rate of the device configured as master. SPR1 and SPR0 have no effect on the slave. The relationship between SCK and the oscillator frequency, $F_{osc.}$, is as follows: SPR1 SPR0 SCK = $F_{osc.}$ divided by 0 0 4 0 1 16 1 0 64 1 1 128

Table 5. SPSR – SPI Status Register

SPSR Address = AAH

Reset Value = 00XX XXXXB

Bit	SPIF	WCOL	–	–	–	–	–	–
	7	6	5	4	3	2	1	0

Symbol	Function
SPIF	SPI Interrupt Flag. When a serial transfer is complete, the SPIF bit is set and an interrupt is generated if SPIE = 1 and ES = 1. The SPIF bit is cleared by reading the SPI status register with SPIF and WCOL bits set, and then accessing the SPI data register.
WCOL	Write Collision Flag. The WCOL bit is set if the SPI data register is written during a data transfer. During data transfer, the result of reading the SPDR register may be incorrect, and writing to it has no effect. The WCOL bit (and the SPIF bit) are cleared by reading the SPI status register with SPIF and WCOL set, and then accessing the SPI data register.

Table 6. SPDR – SPI Data Register

SPDR Address = 86H

Reset Value = unchanged

Bit	SPD7	SPD6	SPD5	SPD4	SPD3	SPD2	SPD1	SPD0
	7	6	5	4	3	2	1	0

Data Memory – EEPROM and RAM

The AT89S8252 implements 2K bytes of on-chip EEPROM for data storage and 256 bytes of RAM. The upper 128 bytes of RAM occupy a parallel space to the Special Function Registers. That means the upper 128 bytes have the same addresses as the SFR space but are physically separate from SFR space.

When an instruction accesses an internal location above address 7FH, the address mode used in the instruction specifies whether the CPU accesses the upper 128 bytes of RAM or the SFR space. Instructions that use direct addressing access SFR space.

For example, the following direct addressing instruction accesses the SFR at location 0A0H (which is P2).

```
MOV 0A0H, #data
```

Instructions that use indirect addressing access the upper 128 bytes of RAM. For example, the following indirect addressing instruction, where R0 contains 0A0H, accesses the data byte at address 0A0H, rather than P2 (whose address is 0A0H).

```
MOV @R0, #data
```

Note that stack operations are examples of indirect addressing, so the upper 128 bytes of data RAM are available as stack space.

The on-chip EEPROM data memory is selected by setting the EEMEN bit in the WMCON register at SFR address location 96H. The EEPROM address range is from 000H to 7FFH. The MOVX instructions are used to access the EEPROM. To access off-chip data memory with the MOVX instructions, the EEMEN bit needs to be set to "0".

The EEMWE bit in the WMCON register needs to be set to "1" before any byte location in the EEPROM can be written. User software should reset EEMWE bit to "0" if no further EEPROM write is required. EEPROM write cycles in the serial programming mode are self-timed and typically take 2.5 ms. The progress of EEPROM write can be monitored by reading the RDY/$\overline{BSY}$ bit (read-only) in SFR WMCON. RDY/$\overline{BSY}$ = 0 means programming is still in progress and RDY/$\overline{BSY}$ = 1 means EEPROM write cycle is completed and another write cycle can be initiated.

In addition, during EEPROM programming, an attempted read from the EEPROM will fetch the byte being written with the MSB complemented. Once the write cycle is completed, true data are valid at all bit locations.

Programmable Watchdog Timer

The programmable Watchdog Timer (WDT) operates from an independent oscillator. The prescaler bits, PS0, PS1 and PS2 in SFR WMCON are used to set the period of the Watchdog Timer from 16 ms to 2048 ms. The available timer periods are shown in the following table and the actual timer periods (at V_{CC} = 5V) are within ±30% of the nominal.

The WDT is disabled by Power-on Reset and during Power-down. It is enabled by setting the WDTEN bit in SFR WMCON (address = 96H). The WDT is reset by setting the WDTRST bit in WMCON. When the WDT times out without being reset or disabled, an internal RST pulse is generated to reset the CPU.

Table 7. Watchdog Timer Period Selection

WDT Prescaler Bits			
PS2	PS1	PS0	Period (nominal)
0	0	0	16 ms
0	0	1	32 ms
0	1	0	64 ms
0	1	1	128 ms
1	0	0	256 ms
1	0	1	512 ms
1	1	0	1024 ms
1	1	1	2048 ms

Timer 0 and 1

Timer 0 and Timer 1 in the AT89S8252 operate the same way as Timer 0 and Timer 1 in the AT89C51, AT89C52 and AT89C55. For further information, see the October 1995 Microcontroller Data Book, page 2-45, section titled, "Timer/Counters."

Timer 2

Timer 2 is a 16 bit Timer/Counter that can operate as either a timer or an event counter. The type of operation is selected by bit C/$\overline{T2}$ in the SFR T2CON (shown in Table 2). Timer 2 has three operating modes: capture, auto-reload (up or down counting), and baud rate generator. The modes are selected by bits in T2CON, as shown in Table 8.

Timer 2 consists of two 8-bit registers, TH2 and TL2. In the Timer function, the TL2 register is incremented every machine cycle. Since a machine cycle consists of 12 oscillator periods, the count rate is 1/12 of the oscillator frequency.

In the Counter function, the register is incremented in response to a 1-to-0 transition at its corresponding external input pin, T2. In this function, the external input is sampled during S5P2 of every machine cycle. When the samples show a high in one cycle and a low in the next cycle, the count is incremented. The new count value appears in the register during S3P1 of the cycle following the one in which

the transition was detected. Since two machine cycles (24 oscillator periods) are required to recognize a 1-to-0 transition, the maximum count rate is 1/24 of the oscillator frequency. To ensure that a given level is sampled at least once before it changes, the level should be held for at least one full machine cycle.

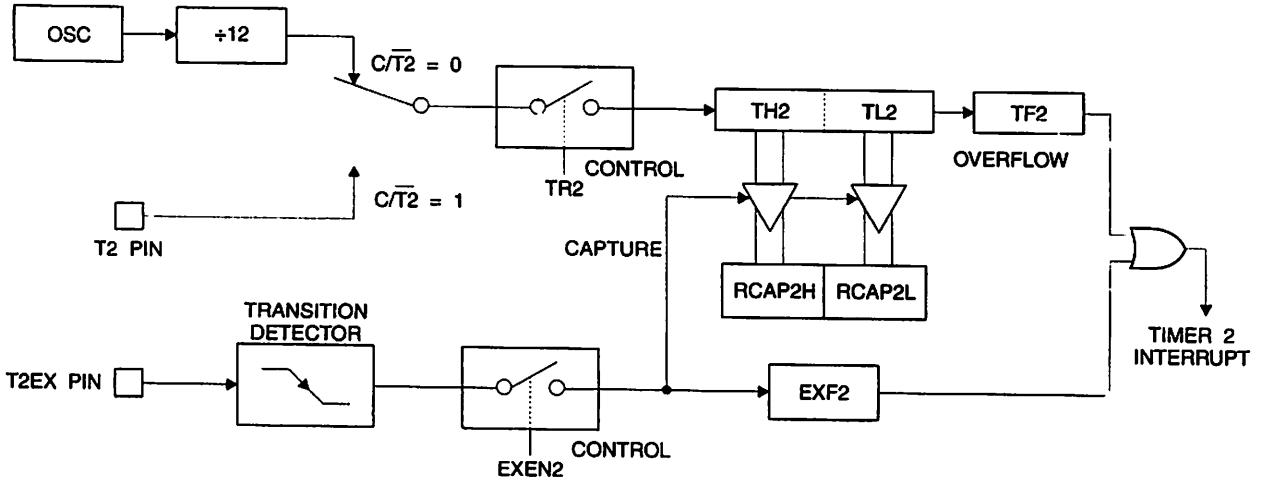
Table 8. Timer 2 Operating Modes

RCLK + TCLK	CP/$\overline{RL2}$	TR2	MODE
0	0	1	16-bit Auto-reload
0	1	1	16-bit Capture
1	X	1	Baud Rate Generator
X	X	0	(Off)

Capture Mode

In the capture mode, two options are selected by bit EXEN2 in T2CON. If EXEN2 = 0, Timer 2 is a 16 bit timer or counter which upon overflow sets bit TF2 in T2CON. This bit can then be used to generate an interrupt. If EXEN2 = 1, Timer 2 performs the same operation, but a 1-to-0 transition at external input T2EX also causes the current value in TH2 and TL2 to be captured into RCAP2H and RCAP2L, respectively. In addition, the transition at T2EX causes bit EXF2 in T2CON to be set. The EXF2 bit, like TF2, can generate an interrupt. The capture mode is illustrated in Figure 1.

Figure 1. Timer 2 in Capture Mode



Auto-reload (Up or Down Counter)

Timer 2 can be programmed to count up or down when configured in its 16 bit auto-reload mode. This feature is invoked by the DCEN (Down Counter Enable) bit located in the SFR T2MOD (see Table 9). Upon reset, the DCEN bit is set to 0 so that timer 2 will default to count up. When DCEN is set, Timer 2 can count up or down, depending on the value of the T2EX pin.

Figure 2 shows Timer 2 automatically counting up when DCEN = 0. In this mode, two options are selected by bit EXEN2 in T2CON. If EXEN2 = 0, Timer 2 counts up to 0FFFFH and then sets the TF2 bit upon overflow. The overflow also causes the timer registers to be reloaded with the 16 bit value in RCAP2H and RCAP2L. The values in RCAP2H and RCAP2L are preset by software. If EXEN2 = 1, a 16 bit reload can be triggered either by an overflow or by a 1-to-0 transition at external input T2EX. This transition also sets the EXF2 bit. Both the TF2 and EXF2 bits can generate an interrupt if enabled.

Setting the DCEN bit enables Timer 2 to count up or down, as shown in Figure 3. In this mode, the T2EX pin controls the direction of the count. A logic 1 at T2EX makes Timer 2 count up. The timer will overflow at 0FFFFH and set the TF2 bit. This overflow also causes the 16 bit value in RCAP2H and RCAP2L to be reloaded into the timer registers, TH2 and TL2, respectively.

A logic 0 at T2EX makes Timer 2 count down. The timer underflows when TH2 and TL2 equal the values stored in RCAP2H and RCAP2L. The underflow sets the TF2 bit and causes 0FFFFH to be reloaded into the timer registers.

The EXF2 bit toggles whenever Timer 2 overflows or underflows and can be used as a 17th bit of resolution. In this operating mode, EXF2 does not flag an interrupt.

Figure 2. Timer 2 in Auto Reload Mode (DCEN = 0)

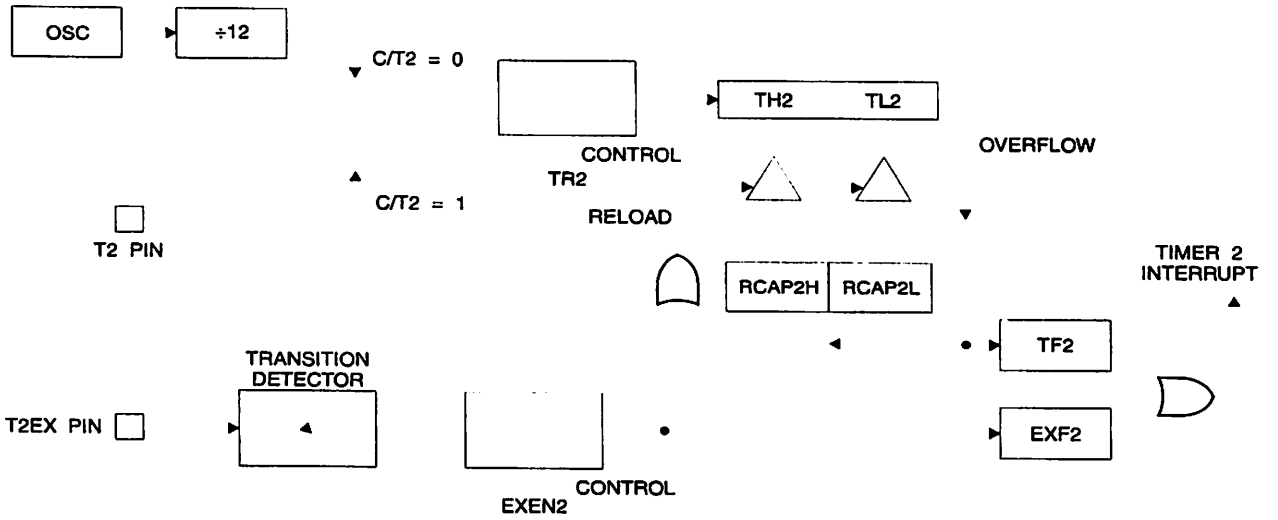


Table 9. T2MOD – Timer 2 Mode Control Register

T2MOD Address = 0C9H — Reset Value = XXXX XX00B

Not Bit Addressable

Bit	7	6	5	4	3	2	1	0
	–	–	–	–	–	–	T2OE	DCEN

Symbol	Function
–	Not implemented, reserved for future use.
T2OE	Timer 2 Output Enable bit.
DCEN	When set, this bit allows Timer 2 to be configured as an up/down counter.

Figure 3. Timer 2 Auto Reload Mode (DCEN = 1)

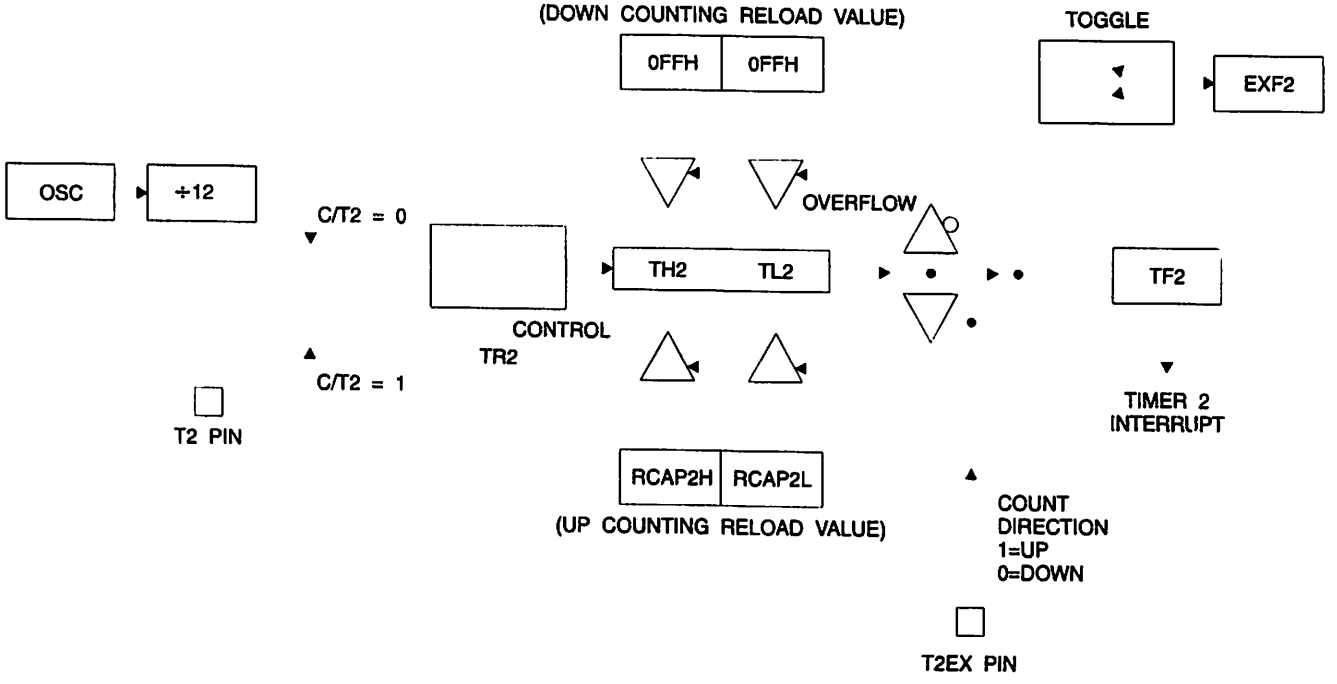
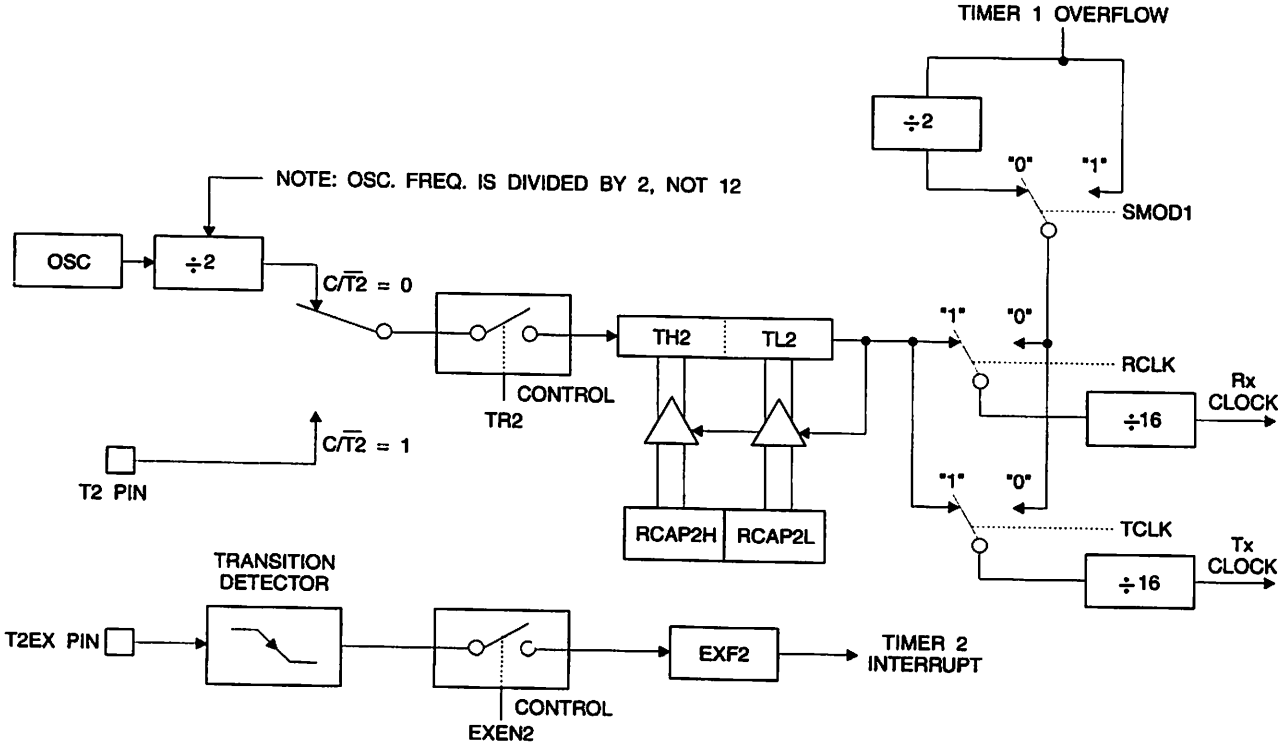


Figure 4. Timer 2 in Baud Rate Generator Mode



Baud Rate Generator

Timer 2 is selected as the baud rate generator by setting TCLK and/or RCLK in T2CON (Table 2). Note that the baud rates for transmit and receive can be different if Timer 2 is used for the receiver or transmitter and Timer 1 is used for the other function. Setting RCLK and/or TCLK puts Timer 2 into its baud rate generator mode, as shown in Figure 4.

The baud rate generator mode is similar to the auto-reload mode, in that a rollover in TH2 causes the Timer 2 registers to be reloaded with the 16 bit value in registers RCAP2H and RCAP2L, which are preset by software.

The baud rates in Modes 1 and 3 are determined by Timer 2's overflow rate according to the following equation.

$$\text{Modes 1 and 3 Baud Rates} = \frac{\text{Timer 2 Overflow Rate}}{16}$$

The Timer can be configured for either timer or counter operation. In most applications, it is configured for timer operation ($C/\overline{T2} = 0$). The timer operation is different for Timer 2 when it is used as a baud rate generator. Normally, as a timer, it increments every machine cycle (at 1/12 the oscillator frequency). As a baud rate generator, however, it increments every state time (at 1/2 the oscillator frequency). The baud rate formula is given below.

$$\frac{\text{Modes 1 and 3}}{\text{Baud Rate}} = \frac{\text{Oscillator Frequency}}{32 \times [65536 - (\text{RCAP2H,RCAP2L})]}$$

Where (RCAP2H, RCAP2L) is the content of RCAP2H and RCAP2L taken as a 16 bit unsigned integer.

Timer 2 as a baud rate generator is shown in Figure 4. This figure is valid only if RCLK or TCLK = 1 in T2CON. Note that a rollover in TH2 does not set TF2 and will not generate an interrupt. Note too, that if EXEN2 is set, a 1-to-0 transition in T2EX will set EXF2 but will not cause a reload from (RCAP2H, RCAP2L) to (TH2, TL2). Thus when Timer 2 is in use as a baud rate generator, T2EX can be used as an extra external interrupt.

Note that when Timer 2 is running (TR2 = 1) as a timer in the baud rate generator mode, TH2 or TL2 should not be read from or written to. Under these conditions, the Timer is incremented every state time, and the results of a read or write may not be accurate. The RCAP2 registers may be read but should not be written to, because a write might overlap a reload and cause write and/or reload errors. The timer should be turned off (clear TR2) before accessing the Timer 2 or RCAP2 registers.

Programmable Clock Out

A 50% duty cycle clock can be programmed to come out on P1.0, as shown in Figure 5. This pin, besides being a regular I/O pin, has two alternate functions. It can be programmed to input the external clock for Timer/Counter 2 or to output a 50% duty cycle clock ranging from 61 Hz to 4 MHz at a 16 MHz operating frequency.

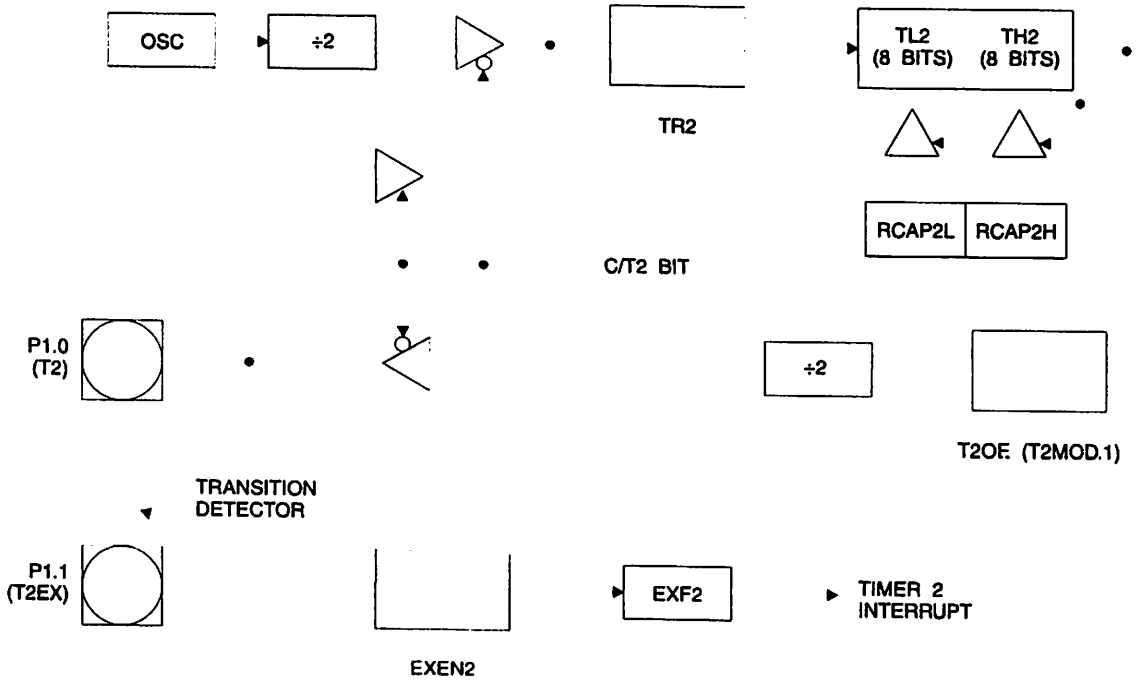
To configure the Timer/Counter 2 as a clock generator, bit $C/\overline{T2}$ (T2CON.1) must be cleared and bit T2OE (T2MOD.1) must be set. Bit TR2 (T2CON.2) starts and stops the timer.

The clock-out frequency depends on the oscillator frequency and the reload value of Timer 2 capture registers (RCAP2H, RCAP2L), as shown in the following equation.

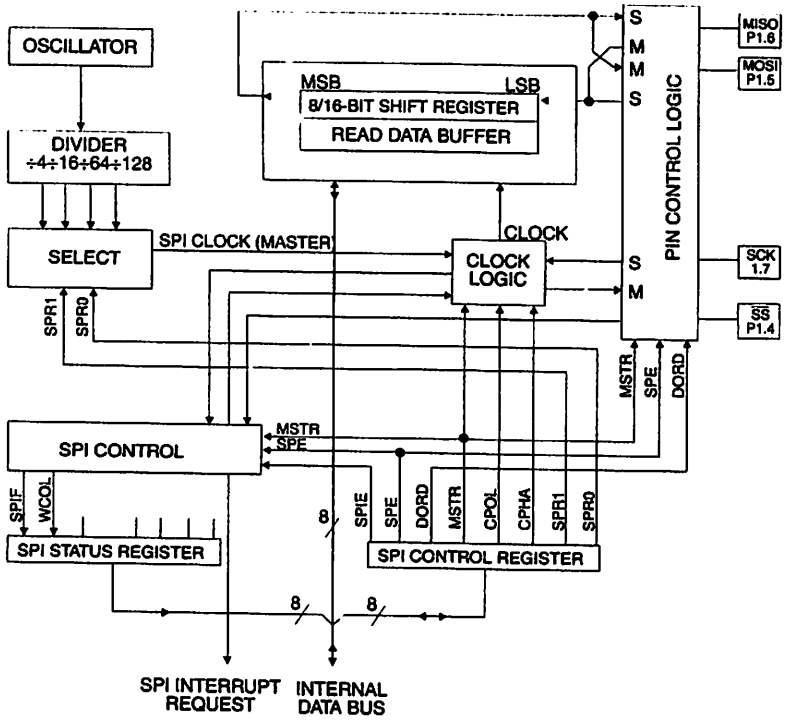
$$\text{Clock Out Frequency} = \frac{\text{Oscillator Frequency}}{4 \times [65536 - (\text{RCAP2H,RCAP2L})]}$$

In the clock-out mode, Timer 2 rollovers will not generate an interrupt. This behavior is similar to when Timer 2 is used as a baud-rate generator. It is possible to use Timer 2 as a baud-rate generator and a clock generator simultaneously. Note, however, that the baud-rate and clock-out frequencies cannot be determined independently from one another since they both use RCAP2H and RCAP2L.

igure 5. Timer 2 in Clock-out Mode



igure 6. SPI Block Diagram



UART

The UART in the AT89S8252 operates the same way as the UART in the AT89C51, AT89C52 and AT89C55. For further information, see the October 1995 Microcontroller Data Book, page 2-49, section titled, "Serial Interface."

Serial Peripheral Interface

The serial peripheral interface (SPI) allows high-speed synchronous data transfer between the AT89S8252 and peripheral devices or between several AT89S8252 devices. The AT89S8252 SPI features include the following:

- Full-Duplex, 3-Wire Synchronous Data Transfer
- Master or Slave Operation
- 1.5 MHz Bit Frequency (max.)
- LSB First or MSB First Data Transfer
- Four Programmable Bit Rates
- End of Transmission Interrupt Flag
- Write Collision Flag Protection
- Wakeup from Idle Mode (Slave Mode Only)

The interconnection between master and slave CPUs with SPI is shown in the following figure. The SCK pin is the clock output in the master mode but is the clock input in the slave mode. Writing to the SPI data register of the master CPU starts the SPI clock generator, and the data written shifts out of the MOSI pin and into the MOSI pin of the slave CPU. After shifting one byte, the SPI clock generator stops, setting the end of transmission flag (SPIF). If both the SPI interrupt enable bit (SPIE) and the serial port interrupt enable bit (ES) are set, an interrupt is requested.

The Slave Select input, $\overline{SS}$/P1.4, is set low to select an individual SPI device as a slave. When $\overline{SS}$/P1.4 is set high, the SPI port is deactivated and the MOSI/P1.5 pin can be used as an input.

There are four combinations of SCK phase and polarity with respect to serial data, which are determined by control bits CPHA and CPOL. The SPI data transfer formats are shown in Figure 8 and Figure 9.

Figure 7. SPI Master-slave Interconnection

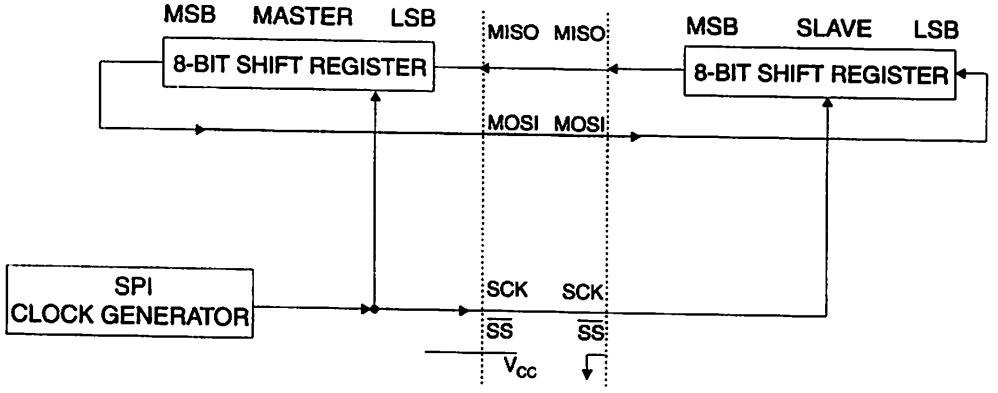
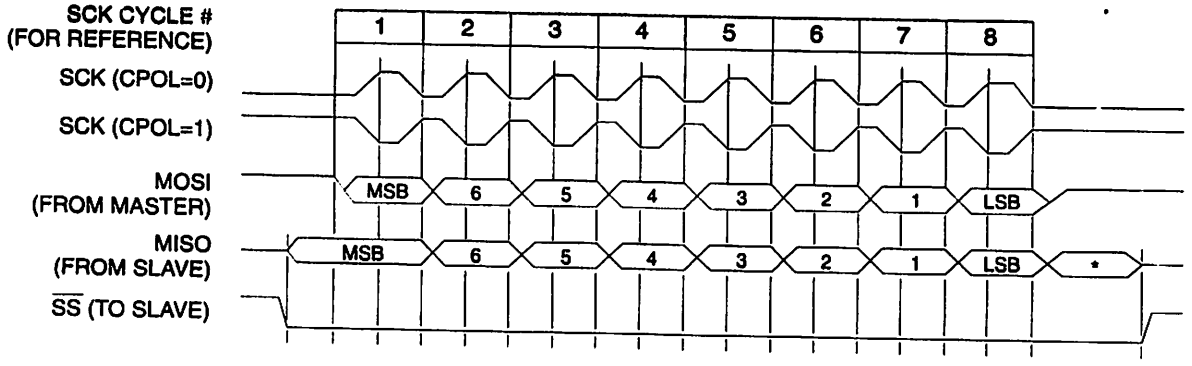
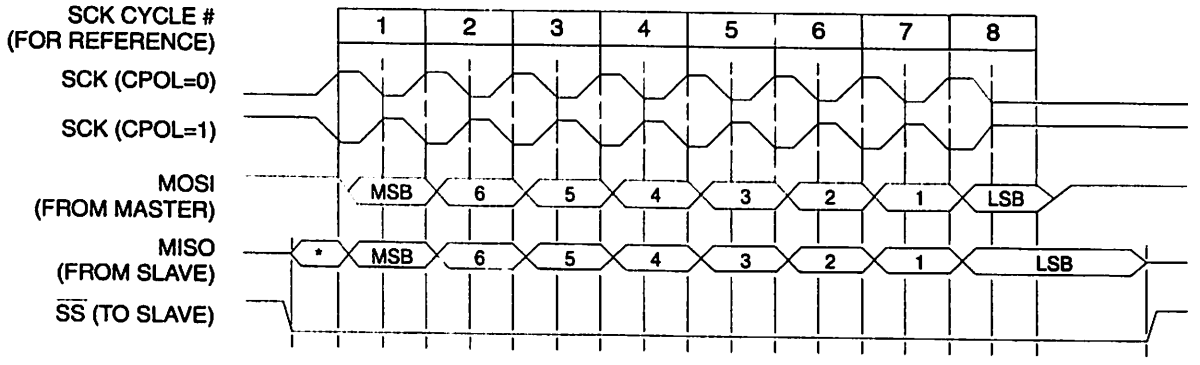


Figure 8. SPI transfer Format with CPHA = 0



*Not defined but normally MSB of character just received

Figure 9. SPI Transfer Format with CPHA = 1



*Not defined but normally LSB of previously transmitted character

Interrupts

The AT89S8252 has a total of six interrupt vectors: two external interrupts ($\overline{INT0}$ and $\overline{INT1}$), three timer interrupts (Timers 0, 1, and 2), and the serial port interrupt. These interrupts are all shown in Figure 10.

Each of these interrupt sources can be individually enabled or disabled by setting or clearing a bit in Special Function Register IE. IE also contains a global disable bit, EA, which disables all interrupts at once.

Note that Table 10 shows that bit position IE.6 is unimplemented. In the AT89C51, bit position IE.5 is also unimplemented. User software should not write 1s to these bit positions, since they may be used in future AT89 products.

Timer 2 interrupt is generated by the logical OR of bits TF2 and EXF2 in register T2CON. Neither of these flags is cleared by hardware when the service routine is vectored to. In fact, the service routine may have to determine whether it was TF2 or EXF2 that generated the interrupt, and that bit will have to be cleared in software.

The Timer 0 and Timer 1 flags, TF0 and TF1, are set at S5P2 of the cycle in which the timers overflow. The values are then polled by the circuitry in the next cycle. However, the Timer 2 flag, TF2, is set at S2P2 and is polled in the same cycle in which the timer overflows.

Table 10. Interrupt Enable (IE) Register

(MSB)(LSB)

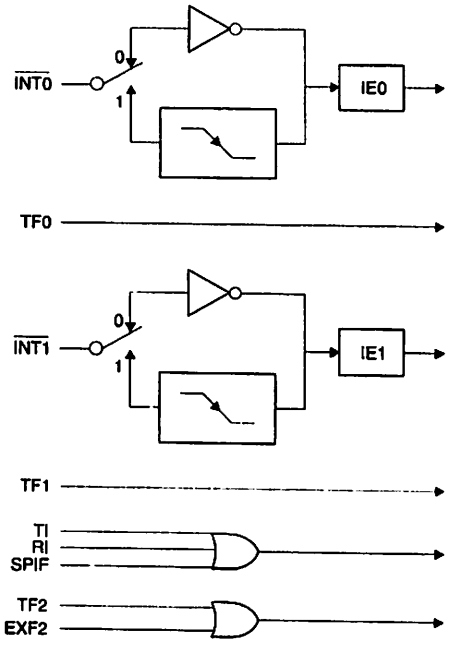
EA	–	ET2	ES	ET1	EX1	ET0	EX0

Enable Bit = 1 enables the interrupt.

Enable Bit = 0 disables the interrupt.

Symbol	Position	Function
EA	IE.7	Disables all interrupts. If EA = 0, no interrupt is acknowledged. If EA = 1, each interrupt source is individually enabled or disabled by setting or clearing its enable bit.
–	IE.6	Reserved.
ET2	IE.5	Timer 2 interrupt enable bit.
ES	IE.4	SPI and UART interrupt enable bit.
ET1	IE.3	Timer 1 interrupt enable bit.
EX1	IE.2	External interrupt 1 enable bit.
ET0	IE.1	Timer 0 interrupt enable bit.
EX0	IE.0	External interrupt 0 enable bit.
User software should never write 1s to unimplemented bits, because they may be used in future AT89 products.		

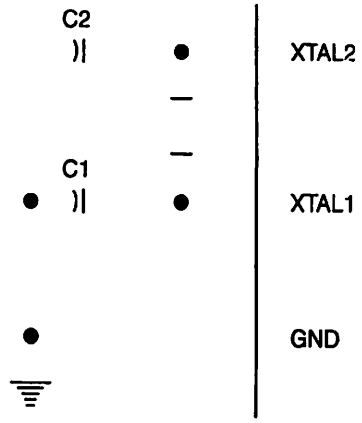
Figure 10. Interrupt Sources



Oscillator Characteristics

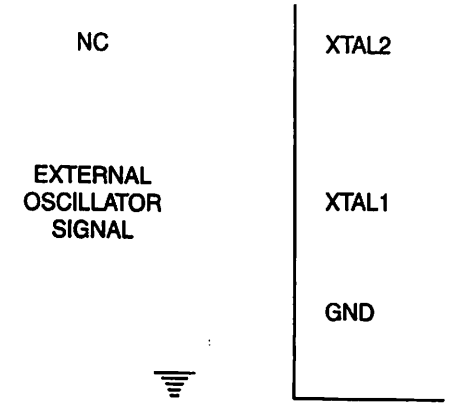
XTAL1 and XTAL2 are the input and output, respectively, of an inverting amplifier that can be configured for use as an on-chip oscillator, as shown in Figure 11. Either a quartz crystal or ceramic resonator may be used. To drive the device from an external clock source, XTAL2 should be left unconnected while XTAL1 is driven, as shown in Figure 12. There are no requirements on the duty cycle of the external clock signal, since the input to the internal clocking circuitry is through a divide-by-two flip-flop, but minimum and maximum voltage high and low time specifications must be observed.

Figure 11. Oscillator Connections



Note: Note: C1, C2 = 30 pF ± 10 pF for Crystals
= 40 pF ± 10 pF for Ceramic Resonators

Figure 12. External Clock Drive Configuration



Idle Mode

In idle mode, the CPU puts itself to sleep while all the on-chip peripherals remain active. The mode is invoked by software. The content of the on-chip RAM and all the special functions registers remain unchanged during this mode. The idle mode can be terminated by any enabled interrupt or by a hardware reset.

Note that when idle mode is terminated by a hardware reset, the device normally resumes program execution from where it left off, up to two machine cycles before the internal reset algorithm takes control. On-chip hardware inhibits access to internal RAM in this event, but access to the port pins is not inhibited. To eliminate the possibility of an unexpected write to a port pin when idle mode is terminated by a reset, the instruction following the one that invokes idle mode should not write to a port pin or to external memory.

Status of External Pins During Idle and Power-down Modes

Mode	Program Memory	ALE	$\overline{PSEN}$	PORT0	PORT1	PORT2	PORT3
Idle	Internal	1	1	Data	Data	Data	Data
Idle	External	1	1	Float	Data	Address	Data
Power-down	Internal	0	0	Data	Data	Data	Data
Power-down	External	0	0	Float	Data	Data	Data

Power-down Mode

In the power-down mode, the oscillator is stopped and the instruction that invokes power-down is the last instruction executed. The on-chip RAM and Special Function Registers retain their values until the power-down mode is terminated. Exit from power-down can be initiated either by a hardware reset or by an enabled external interrupt. Reset redefines the SFRs but does not change the on-chip RAM. The reset should not be activated before V_{CC} is restored to its normal operating level and must be held active long enough to allow the oscillator to restart and stabilize.

To exit power-down via an interrupt, the external interrupt must be enabled as level sensitive before entering power-down. The interrupt service routine starts at 16 ms (nominal) after the enabled interrupt pin is activated.

Program Memory Lock Bits

The AT89S8252 has three lock bits that can be left unprogrammed (U) or can be programmed (P) to obtain the additional features listed in the following table.

When lock bit 1 is programmed, the logic level at the $\overline{EA}$ pin is sampled and latched during reset. If the device is powered up without a reset, the latch initializes to a random value and holds that value until reset is activated. The latched value of $\overline{EA}$ must agree with the current logic level at that pin in order for the device to function properly.

Once programmed, the lock bits can only be unprogrammed with the Chip Erase operations in either the parallel or serial modes.

Lock Bit Protection Modes[1][2]

Program Lock Bits				
	LB1	LB2	LB3	Protection Type
1	U	U	U	No internal memory lock feature.
2	P	U	U	MOVC instructions executed from external program memory are disabled from fetching code bytes from internal memory. $\overline{EA}$ is sampled and latched on reset and further programming of the Flash memory (parallel or serial mode) is disabled.
3	P	P	U	Same as Mode 2, but parallel or serial verify are also disabled.
4	P	P	P	Same as Mode 3, but external execution is also disabled.

Notes: 1. U = Unprogrammed
2. P = Programmed

'rogramming the Flash and EEPROM

tmel's AT89S8252 Flash Microcontroller offers 8K bytes in-system reprogrammable Flash Code memory and 2K ytes of EEPROM Data memory.

he AT89S8252 is normally shipped with the on-chip Flash ode and EEPROM Data memory arrays in the erased ate (i.e. contents = FFH) and ready to be programmed. his device supports a High-voltage (12V) Parallel proramming mode and a Low-voltage (5V) Serial 'ogramming mode. The serial programming mode prodes a convenient way to download the AT89S8252 inside e user's system. The parallel programming mode is comatible with conventional third party Flash or EPROM 'ogrammers.

ne Code and Data memory arrays are mapped via sepate address spaces in the serial programming mode. In e parallel programming mode, the two arrays occupy one ntiguous address space: 0000H to 1FFFH for the Code ray and 2000H to 27FFH for the Data array.

ne Code and Data memory arrays on the AT89S8252 are ogrammed byte-by-byte in either programming mode. An to-erase cycle is provided with the self-timed programing operation in the serial programming mode. There is need to perform the Chip Erase operation to reprogram ny memory location in the serial programming mode less any of the lock bits have been programmed.

the parallel programming mode, there is no auto-erase cle. To reprogram any non-blank byte, the user needs to e the Chip Erase operation first to erase both arrays.

arallel Programming Algorithm: To program and verify e AT89S8252 in the parallel programming mode, the folwing sequence is recommended:

Power-up sequence:

Apply power between V_{CC} and GND pins.

Set RST pin to "H".

Apply a 3 MHz to 24 MHz clock to XTAL1 pin and wait for at least 10 milliseconds.

Set $\overline{PSEN}$ pin to "L"

ALE pin to "H"

$\overline{EA}$ pin to "H" and all other pins to "H".

Apply the appropriate combination of "H" or "L" logic levels to pins P2.6, P2.7, P3.6, P3.7 to select one of the programming operations shown in the Flash Programming Modes table.

Apply the desired byte address to pins P1.0 to P1.7 and P2.0 to P2.5.

Apply data to pins P0.0 to P0.7 for Write Code operation.

5. Raise $\overline{EA}/V_{PP}$ to 12V to enable Flash programming, erase or verification.
6. Pulse ALE/$\overline{PROG}$ once to program a byte in the Code memory array, the Data memory array or the lock bits. The byte-write cycle is self-timed and typically takes 1.5 ms.
7. To verify the byte just programmed, bring pin P2.7 to "L" and read the programmed data at pins P0.0 to P0.7.
8. Repeat steps 3 through 7 changing the address and data for the entire 2K or 8K bytes array or until the end of the object file is reached.
9. Power-off sequence:

   Set XTAL1 to "L".

   Set RST and $\overline{EA}$ pins to "L".

   Turn V_{CC} power off.

In the parallel programming mode, there is no auto-erase cycle and to reprogram any non-blank byte, the user needs to use the Chip Erase operation first to erase both arrays.

Data Polling: The AT89S8252 features $\overline{DATA}$ Polling to indicate the end of a write cycle. During a write cycle in the parallel or serial programming mode, an attempted read of the last byte written will result in the complement of the written datum on P0.7 (parallel mode), and on the MSB of the serial output byte on MISO (serial mode). Once the write cycle has been completed, true data are valid on all outputs, and the next cycle may begin. $\overline{DATA}$ Polling may begin any time after a write cycle has been initiated.

Ready/$\overline{Busy}$: The progress of byte programming in the parallel programming mode can also be monitored by the RDY/$\overline{BSY}$ output signal. Pin P3.4 is pulled Low after ALE goes High during programming to indicate $\overline{BUSY}$. P3.4 is pulled High again when programming is done to indicate READY.

Program Verify: If lock bits LB1 and LB2 have not been programmed, the programmed Code or Data byte can be read back via the address and data lines for verification. The state of the lock bits can also be verified directly in the parallel programming mode. In the serial programming mode, the state of the lock bits can only be verified indirectly by observing that the lock bit features are enabled.

Chip Erase: Both Flash and EEPROM arrays are erased electrically at the same time. In the parallel programming mode, chip erase is initiated by using the proper combination of control signals and by holding ALE/$\overline{PROG}$ low for 10 ms. The Code and Data arrays are written with all "1"s in the Chip Erase operation.

n the serial programming mode, a chip erase operation is iitiated by issuing the Chip Erase instruction. In this mode, hip erase is self-timed and takes about 16 ms.

)uring chip erase, a serial read from any address location vill return 00H at the data outputs.

ierial Programming Fuse: A programmable fuse is avail-ible to disable Serial Programming if the user needs naximum system security. The Serial Programming Fuse an only be programmed or erased in the Parallel Program-ning Mode.

The AT89S8252 is shipped with the Serial Programming Mode enabled.

leading the Signature Bytes: The signature bytes are ead by the same procedure as a normal verification of ocations 030H and 031H, except that P3.6 and P3.7 must e pulled to a logic low. The values returned are as follows:

(030H) = 1EH indicates manufactured by Atmel
(031H) = 72H indicates 89S8252

Programming Interface

Every code byte in the Flash and EEPROM arrays can be vritten, and the entire array can be erased, by using the ippropriate combination of control signals. The write oper-ition cycle is self-timed and once initiated, will iutomatically time itself to completion.

All major programming vendors offer worldwide support for he Atmel microcontroller series. Please contact your local rogramming vendor for the appropriate software revision.

Serial Downloading

Both the Code and Data memory arrays can be pro-grammed using the serial SPI bus while RST is pulled to V_{CC}. The serial interface consists of pins SCK, MOSI (input) ind MISO (output). After RST is set high, the Programming Enable instruction needs to be executed first before pro-gram/erase operations can be executed.

An auto-erase cycle is built into the self-timed programming operation (in the serial mode ONLY) and there is no need o first execute the Chip Erase instruction unless any of the ock bits have been programmed. The Chip Erase opera-ion turns the content of every memory location in both the Code and Data arrays into FFH.

The Code and Data memory arrays have separate address spaces:

0000H to 1FFFH for Code memory and 000H to 7FFH for Data memory.

Either an external system clock is supplied at pin XTAL1 or a crystal needs to be connected across pins XTAL1 and XTAL2. The maximum serial clock (SCK) frequency should be less than 1/40 of the crystal frequency. With a 24 MHz oscillator clock, the maximum SCK frequency is 600 kHz.

Serial Programming Algorithm

To program and verify the AT89S8252 in the serial programming mode, the following sequence is recommended:

1. Power-up sequence:

   Apply power between VCC and GND pins.

   Set RST pin to "H".

   If a crystal is not connected across pins XTAL1 and XTAL2, apply a 3 MHz to 24 MHz clock to XTAL1 pin and wait for at least 10 milliseconds.
2. Enable serial programming by sending the Programming Enable serial instruction to pin MOSI/P1.5. The frequency of the shift clock supplied at pin SCK/P1.7 needs to be less than the CPU clock at XTAL1 divided by 40.
3. The Code or Data array is programmed one byte at a time by supplying the address and data together with the appropriate Write instruction. The selected memory location is first automatically erased before new data is written. The write cycle is self-timed and typically takes less than 2.5 ms at 5V.
4. Any memory location can be verified by using the Read instruction which returns the content at the selected address at serial output MISO/P1.6.
5. At the end of a programming session, RST can be set low to commence normal operation.

Power-off sequence (if needed):

Set XTAL1 to "L" (if a crystal is not used).

Set RST to "L".

Turn V_{CC} power off.

Serial Programming Instruction

The Instruction Set for Serial Programming follows a 3-byte protocol and is shown in the following table:

nstruction Set

Instruction	Input Format			Operation
	Byte 1	Byte 2	Byte 3	
Programming Enable	1010 1100	0101 0011	xxxx xxxx	Enable serial programming interface after RST goes high.
Chip Erase	1010 1100	xxxx x100	xxxx xxxx	Chip erase both 8K & 2K memory arrays.
Read Code Memory	aaaa a001	low addr	xxxx xxxx	Read data from Code memory array at the selected address. The 5 MSBs of the first byte are the high order address bits. The low order address bits are in the second byte. Data are available at pin MISO during the third byte.
Write Code Memory	aaaa a010	low addr	data in	Write data to Code memory location at selected address. The address bits are the 5 MSBs of the first byte together with the second byte.
Read Data Memory	00aa a101	low addr	xxxx xxxx	Read data from Data memory array at selected address. Data are available at pin MISO during the third byte.
Write Data Memory	00aa a110	low addr	data in	Write data to Data memory location at selected address.
Write Lock Bits	1010 1100	x x111	xxxx xxxx	Write lock bits. Set LB1, LB2 or LB3 = "0" to program lock bits.

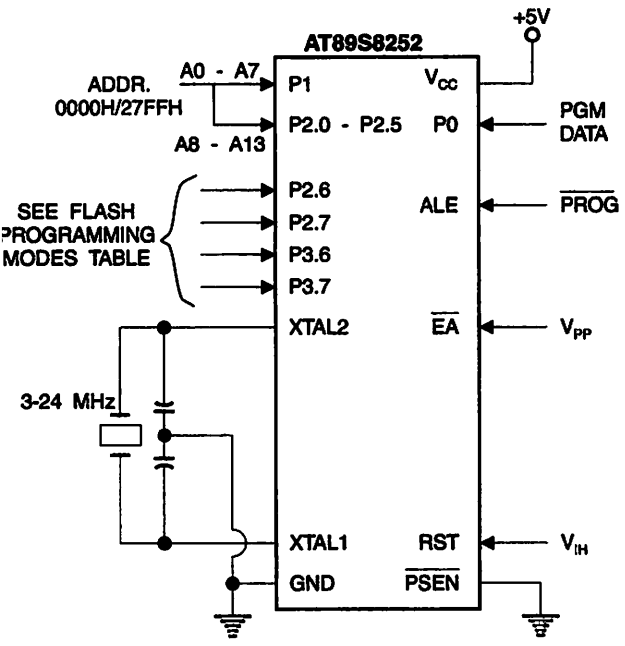
lote:
1. DATA polling is used to indicate the end of a write cycle which typically takes less than 2.5 ms at 5V.
2. "aaaaa" = high order address.
3. "x" = don't care.

ash and EEPROM Parallel Programming Modes

ode	RST	$\overline{PSEN}$	ALE/$\overline{PROG}$	$\overline{EA}/V_{PP}$	P2.6	P2.7	P3.6	P3.7	Data I/O P0.7:0	Address P2.5:0 P1.7:0
erial Prog. Modes	H	h(1)	h(1)	x						
hip Erase	H	L	(2)	12V	H	L	L	L	X	X
rite (10K bytes) Memory	H	L		12V	L	H	H	H	DIN	ADDR
ead (10K bytes) Memory	H	L	H	12V	L	L	H	H	DOUT	ADDR
rite Lock Bits:	H	L		12V	H	L	H	L	DIN	X
Bit - 1									P0.7 = 0	X
Bit - 2									P0.6 = 0	X
Bit - 3									P0.5 = 0	X
ead Lock Bits:	H	L	H	12V	H	H	L	L	DOUT	X
Bit - 1									@P0.2	X
Bit - 2									@P0.1	X
Bit - 3									@P0.0	X
ead Atmel Code	H	L	H	12V	L	L	L	L	DOUT	30H
ead Device Code	H	L	H	12V	L	L	L	L	DOUT	31H
erial Prog. Enable	H	L	(2)	12V	L	H	L	H	P0.0 = 0	X
erial Prog. Disable	H	L	(2)	12V	L	H	L	H	P0.0 = 1	X
ead Serial Prog. Fuse	H	L	H	12V	H	H	L	H	@P0.0	X

tes:
1. "h" = weakly pulled "High" internally.
2. Chip Erase and Serial Programming Fuse require a 10 ms $\overline{PROG}$ pulse. Chip Erase needs to be performed first before reprogramming any byte with a content other than FFH.
3. P3.4 is pulled Low during programming to indicate RDY/$\overline{BSY}$.
4. "X" = don't care

gure 13. Programming the Flash/EEPROM Memory



gure 14. Verifying the Flash/EEPROM Memory

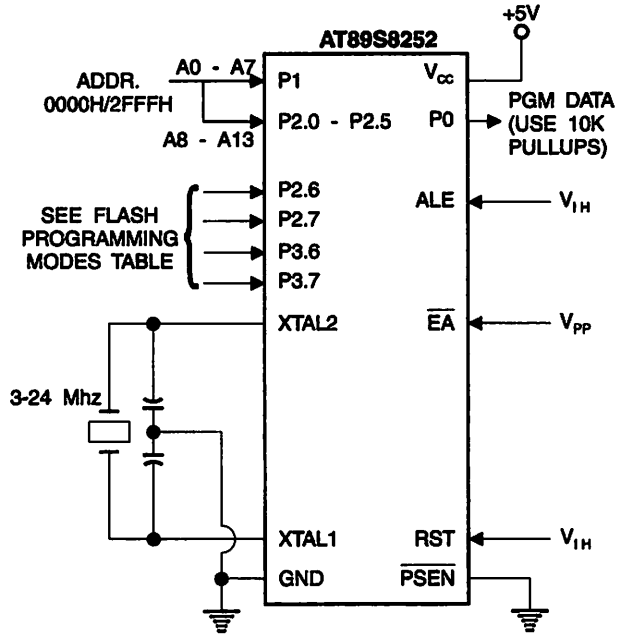
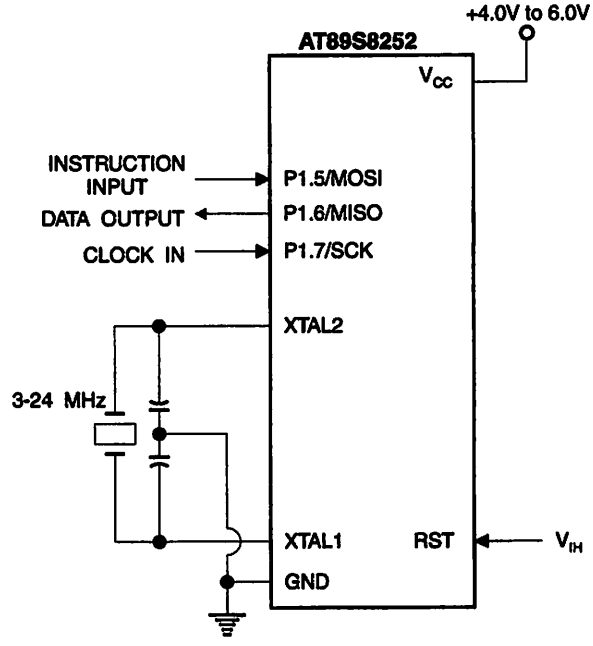


Figure 15. Flash/EEPROM Serial Downloading

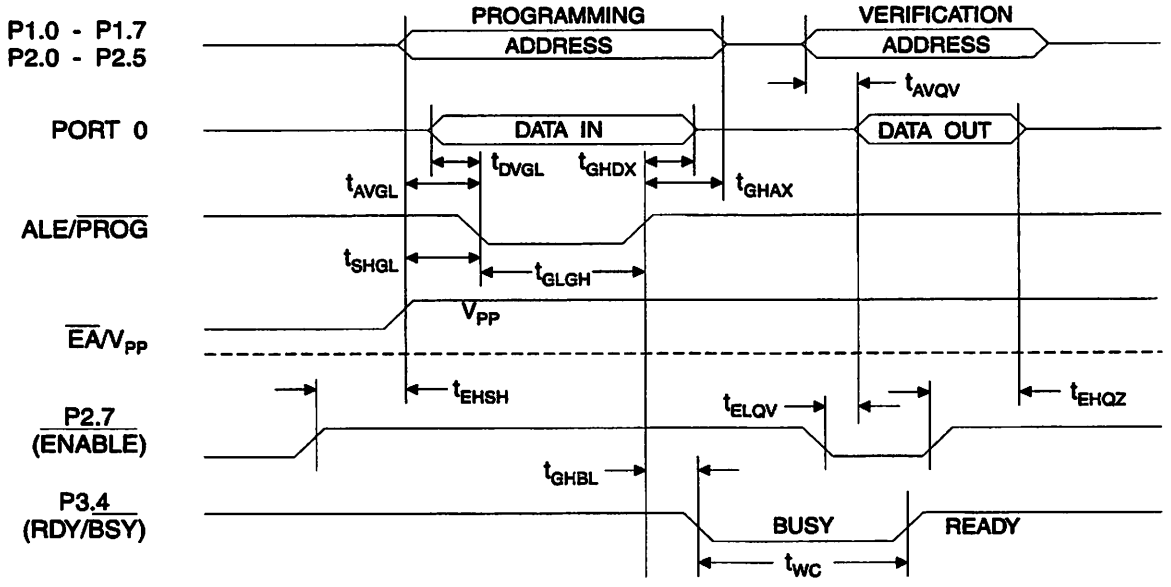


lash Programming and Verification Characteristics – Parallel Mode

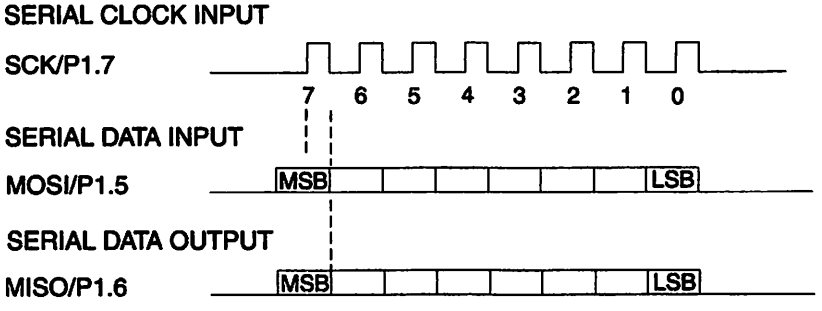
$_A$ = 0°C to 70°C, V_{CC} = 5.0V ± 10%

Symbol	Parameter	Min	Max	Units
$/_{PP}$	Programming Enable Voltage	11.5	12.5	V
PP	Programming Enable Current		1.0	mA
$1/t_{CLCL}$	Oscillator Frequency	3	24	MHz
AVGL	Address Setup to $\overline{PROG}$ Low	$48t_{CLCL}$		
GHAX	Address Hold after $\overline{PROG}$	$48t_{CLCL}$		
DVGL	Data Setup to $\overline{PROG}$ Low	$48t_{CLCL}$		
GHDX	Data Hold after $\overline{PROG}$	$48t_{CLCL}$		
EHSH	P2.7 ($\overline{ENABLE}$) High to V_{PP}	$48t_{CLCL}$		
SHGL	V_{PP} Setup to $\overline{PROG}$ Low	10		µs
GLGH	$\overline{PROG}$ Width	1	110	µs
AVQV	Address to Data Valid		$48t_{CLCL}$	
ELQV	$\overline{ENABLE}$ Low to Data Valid		$48t_{CLCL}$	
EHQZ	Data Float after $\overline{ENABLE}$	0	$48t_{CLCL}$	
GHBL	$\overline{PROG}$ High to $\overline{BUSY}$ Low		1.0	µs
WC	Byte Write Cycle Time		2.0	ms

lash/EEPROM Programming and Verification Waveforms – Parallel Mode



erial Downloading Waveforms



bsolute Maximum Ratings*

Operating Temperature	-55°C to +125°C
Storage Temperature	-65°C to +150°C
Voltage on Any Pin with Respect to Ground	-1.0V to +7.0V
Maximum Operating Voltage	6.6V
DC Output Current	15.0 mA

*NOTICE: Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

C Characteristics

ne values shown in this table are valid for T_A = -40°C to 85°C and V_{CC} = 5.0V ± 20%, unless otherwise noted.

Symbol	Parameter	Condition	Min	Max	Units
V_{IL}	Input Low-voltage	(Except $\overline{EA}$)	-0.5	0.2 V_{CC} - 0.1	V
V_{IL1}	Input Low-voltage ($\overline{EA}$)		-0.5	0.2 V_{CC} - 0.3	V
V_{IH}	Input Hifh-voltage	(Except XTAL1, RST)	0.2 V_{CC} + 0.9	V_{CC} + 0.5	V
V_{IH1}	Input Hifh-voltage	(XTAL1, RST)	0.7 V_{CC}	V_{CC} + 0.5	V
V_{OL}	Output Low-voltage [1] (Ports 1,2,3)	I_{OL} = 1.6 mA		0.5	V
V_{OL1}	Output Low-voltage [1] (Port 0, ALE, $\overline{PSEN}$)	I_{OL} = 3.2 mA		0.5	V
V_{OH}	Output Hifh-voltage (Ports 1,2,3, ALE, $\overline{PSEN}$)	I_{OH} = -60 µA, V_{CC} = 5V ± 10%	2.4		V
		I_{OH} = -25 µA	0.75 V_{CC}		V
		I_{OH} = -10 µA	0.9 V_{CC}		V
V_{OH1}	Output Hifh-voltage (Port 0 in External Bus Mode)	I_{OH} = -800 µA, V_{CC} = 5V ± 10%	2.4		V
		I_{OH} = -300 µA	0.75 V_{CC}		V
		I_{OH} = -80 µA	0.9 V_{CC}		V
I_{IL}	Logical 0 Input Current (Ports 1,2,3)	V_{IN} = 0.45V		-50	µA
I_{TL}	Logical 1 to 0 Transition Current (Ports 1,2,3)	V_{IN} = 2V, V_{CC} = 5V ± 10%		-650	µA
I_{LI}	Input Leakage Current (Port 0, $\overline{EA}$)	0.45 < V_{IN} < V_{CC}		±10	µA
R_{RST}	Reset Pull-down Resistor		50	300	KΩ
C_{IO}	Pin Capacitance	Test Freq. = 1 MHz, T_A = 25°C		10	pF
I_{CC}	Power Supply Current	Active Mode, 12 MHz		25	mA
		Idle Mode, 12 MHz		6.5	mA
	Power-down Mode [2]	V_{CC} = 6V		100	µA
		V_{CC} = 3V		40	µA

otes:
1. Under steady state (non-transient) conditions, I_{OL} must be externally limited as follows:
   Maximum I_{OL} per port pin: 10 mA
   Maximum I_{OL} per 8-bit port:
   Port 0: 26 mA
   Ports 1, 2, 3: 15 mA
   Maximum total I_{OL} for all output pins: 71 mA
   If I_{OL} exceeds the test condition, V_{OL} may exceed the related specification. Pins are not guaranteed to sink current greater than the listed test conditions.
2. Minimum V_{CC} for Power-down is 2V

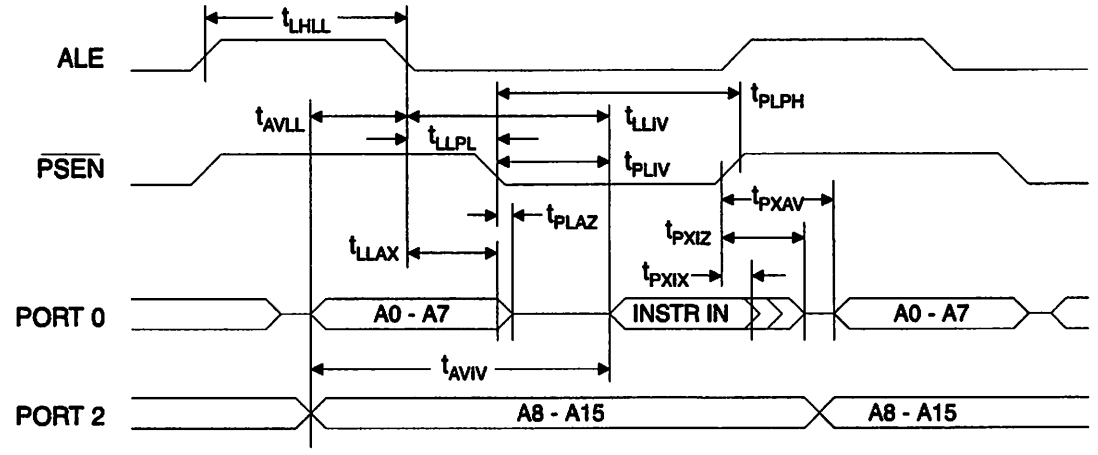
C Characteristics

ıder operating conditions, load capacitance for Port 0, ALE/$\overline{PROG}$, and $\overline{PSEN}$ = 100 pF; load capacitance for all other tputs = 80 pF.

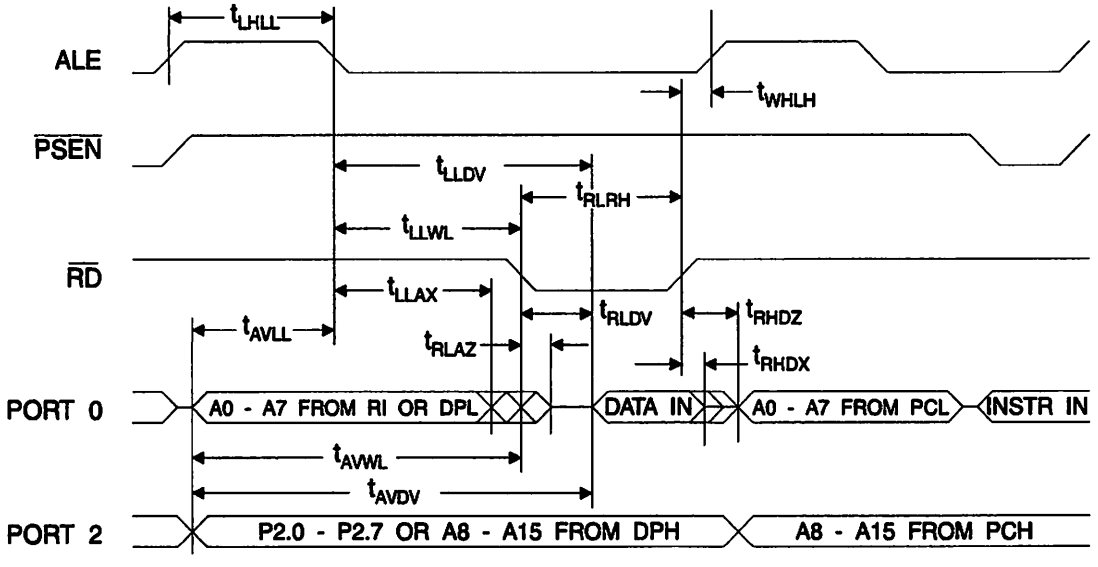
xternal Program and Data Memory Characteristics

ymbol	Parameter	Variable Oscillator		Units
		Min	Max	
$/t_{CLCL}$	Oscillator Frequency	0	24	MHz
.HLL	ALE Pulse Width	$2t_{CLCL}$ - 40		ns
\VLL	Address Valid to ALE Low	t_{CLCL} - 13		ns
.LAX	Address Hold after ALE Low	t_{CLCL} - 20		ns
.LIV	ALE Low to Valid Instruction In		$4t_{CLCL}$ - 65	ns
.LPL	ALE Low to $\overline{PSEN}$ Low	t_{CLCL} - 13		ns
PLPH	$\overline{PSEN}$ Pulse Width	$3t_{CLCL}$ - 20		ns
PLIV	$\overline{PSEN}$ Low to Valid Instruction In		$3t_{CLCL}$ - 45	ns
PXIX	Input Instruction Hold after $\overline{PSEN}$	0		ns
PXIZ	Input Instruction Float after $\overline{PSEN}$		t_{CLCL} - 10	ns
PXAV	$\overline{PSEN}$ to Address Valid	t_{CLCL} - 8		ns
\VIV	Address to Valid Instruction In		$5t_{CLCL}$ - 55	ns
PLAZ	$\overline{PSEN}$ Low to Address Float		10	ns
RLRH	$\overline{RD}$ Pulse Width	$6t_{CLCL}$ - 100		ns
WLWH	$\overline{WR}$ Pulse Width	$6t_{CLCL}$ - 100		ns
RLDV	$\overline{RD}$ Low to Valid Data In		$5t_{CLCL}$ - 90	ns
RHDX	Data Hold after $\overline{RD}$	0		ns
RHDZ	Data Float after $\overline{RD}$		$2t_{CLCL}$ - 28	ns
.LDV	ALE Low to Valid Data In		$8t_{CLCL}$ - 150	ns
\VDV	Address to Valid Data In		$9t_{CLCL}$ - 165	ns
.LWL	ALE Low to $\overline{RD}$ or $\overline{WR}$ Low	$3t_{CLCL}$ - 50	$3t_{CLCL}$ + 50	ns
\VWL	Address to $\overline{RD}$ or $\overline{WR}$ Low	$4t_{CLCL}$ - 75		ns
QVWX	Data Valid to $\overline{WR}$ Transition	t_{CLCL} - 20		ns
QVWH	Data Valid to $\overline{WR}$ High	$7t_{CLCL}$ - 120		ns
WHQX	Data Hold after $\overline{WR}$	t_{CLCL} - 20		ns
RLAZ	$\overline{RD}$ Low to Address Float		0	ns
WHLH	$\overline{RD}$ or $\overline{WR}$ High to ALE High	t_{CLCL} - 20	t_{CLCL} + 25	ns

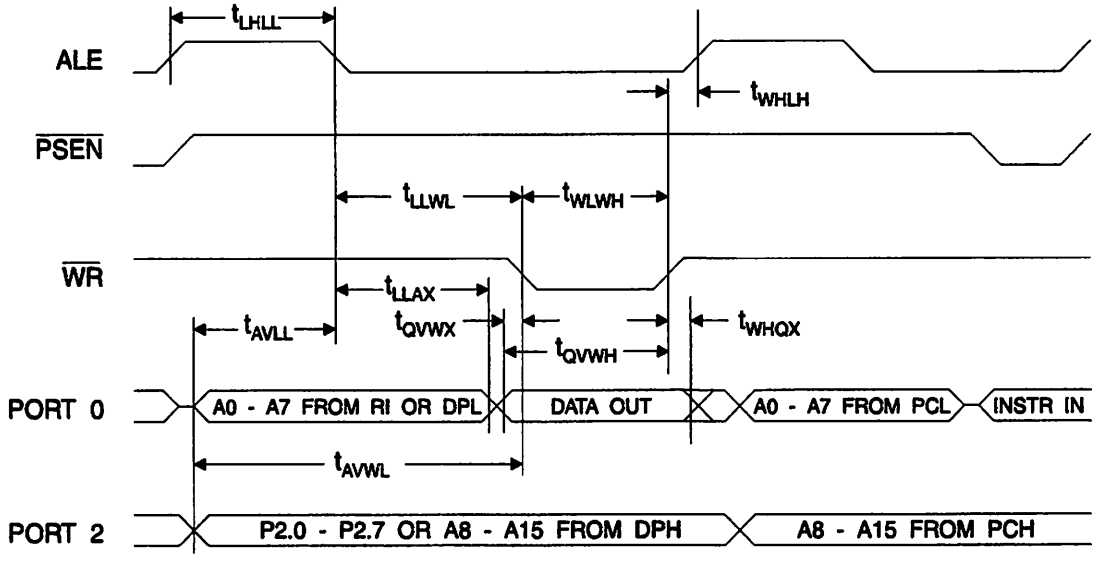
xternal Program Memory Read Cycle



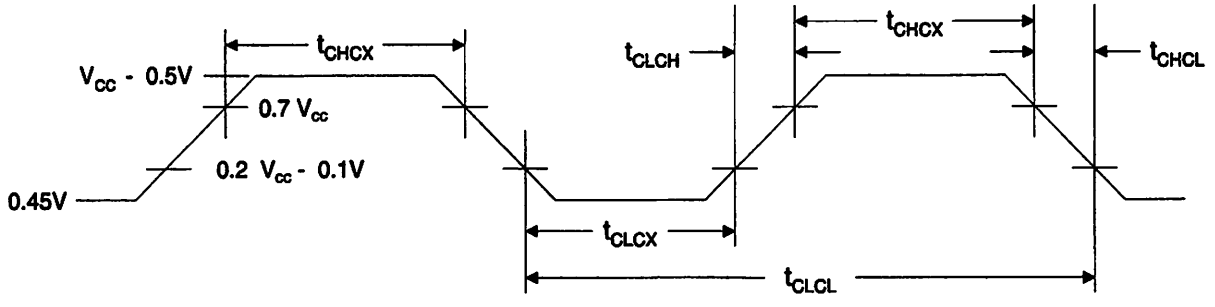
xternal Data Memory Read Cycle



xternal Data Memory Write Cycle



xternal Clock Drive Waveforms



xternal Clock Drive

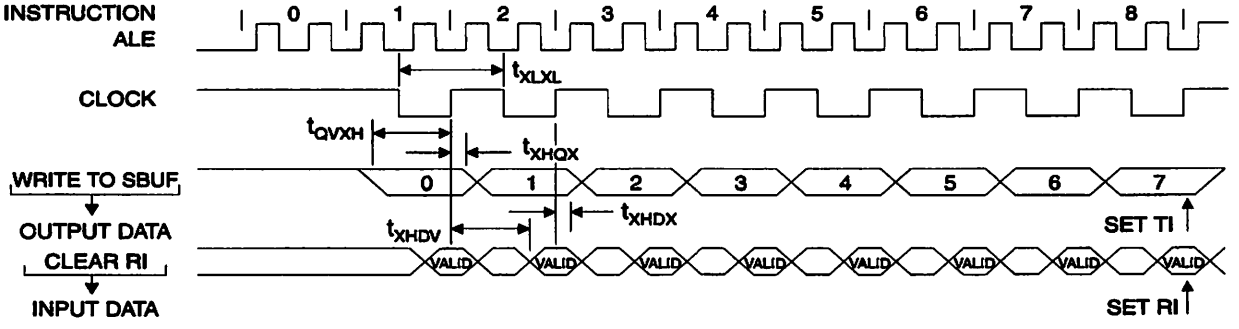
ymbol	Parameter	V_{CC} = 4.0V to 6.0V		Units
		Min	Max	
$/t_{CLCL}$	Oscillator Frequency	0	24	MHz
$_{CLCL}$	Clock Period	41.6		ns
$_{CHCX}$	High Time	15		ns
$_{CLCX}$	Low Time	15		ns
$_{CLCH}$	Rise Time		20	ns
$_{CHCL}$	Fall Time		20	ns

erial Port Timing: Shift Register Mode Test Conditions

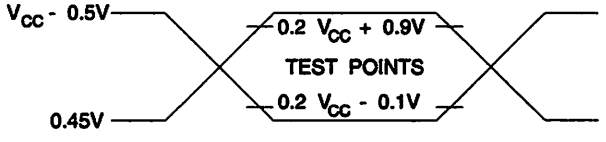
ıe values in this table are valid for V_{CC} = 4.0V to 6V and Load Capacitance = 80 pF.

Symbol	Parameter	Variable Oscillator		Units
		Min	Max	
XLXL	Serial Port Clock Cycle Time	$12t_{CLCL}$		µs
QVXH	Output Data Setup to Clock Rising Edge	$10t_{CLCL}$ - 133		ns
XHQX	Output Data Hold after Clock Rising Edge	$2t_{CLCL}$ - 117		ns
XHDX	Input Data Hold after Clock Rising Edge	0		ns
XHDV	Clock Rising Edge to Input Data Valid		$10t_{CLCL}$ - 133	ns

hift Register Mode Timing Waveforms

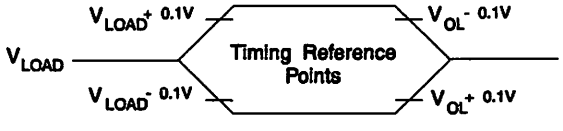


.C Testing Input/Output Waveforms[1]



ɔtes: 1. AC Inputs during testing are driven at V_{CC} - 0.5V for a logic 1 and 0.45V for a logic 0. Timing measurements are made at V_{IH} min. for a logic 1 and V_{IL} max. for a logic 0.

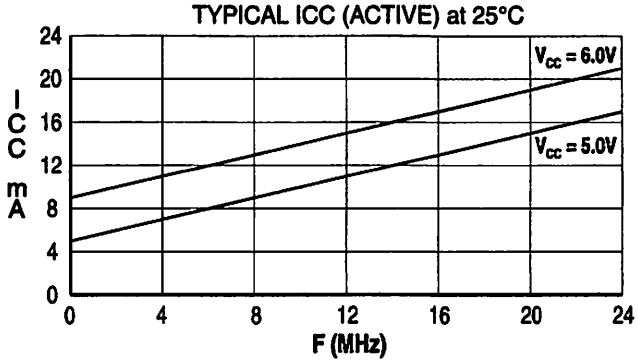
Float Waveforms[1]



Notes: 1. For timing purposes, a port pin is no longer floating when a 100 mV change from load voltage occurs. A port pin begins to float when a 100 mV change from the loaded V_{OH}/V_{OL} level occurs.

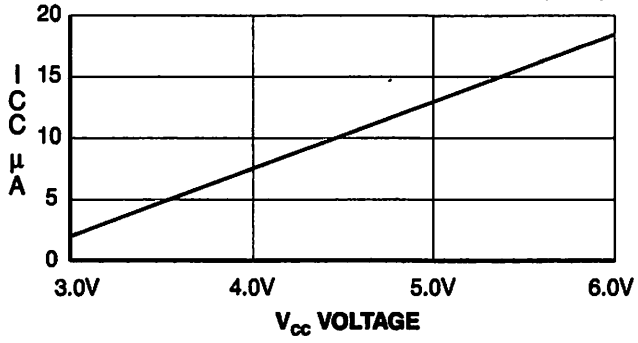
AT89S8252

TYPICAL ICC (ACTIVE) at 25°C



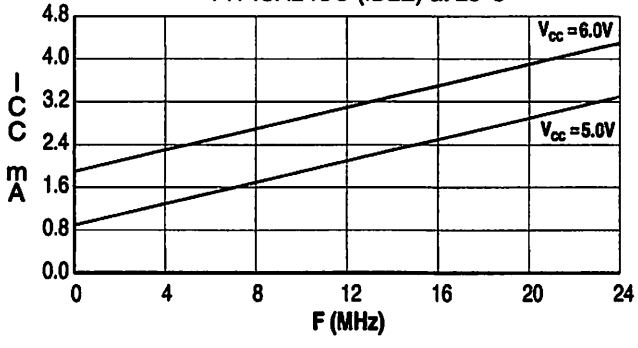
AT89S8252

TYPICAL ICC vs. VOLTAGE - POWER DOWN (85°C)



AT89S8252

TYPICAL ICC (IDLE) at 25°C



Notes: 1. XTAL1 tied to GND for Icc (power-down)
2. Lock bits programmed

rdering Information

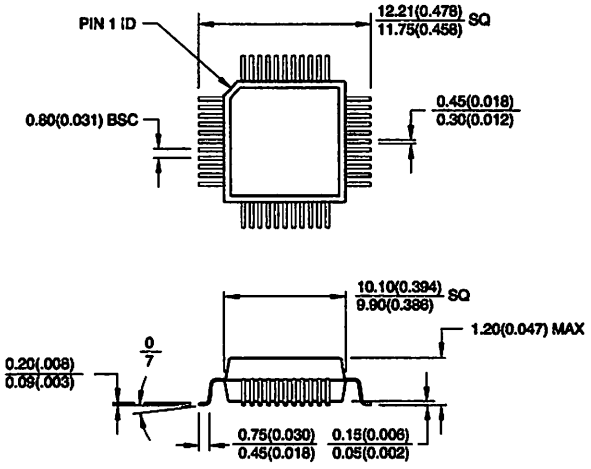
Speed (MHz)	Power Supply	Ordering Code	Package	Operation Range
24	4.0V to 6.0V	AT89S8252-24AC AT89S8252-24JC AT89S8252-24PC AT89S8252-24QC	44A 44J 40P6 44Q	Commercial (0°C to 70°C)
	4.0V to 6.0V	AT89S8252-24AI AT89S8252-24JI AT89S8252-24PI AT89S8252-24QI	44A 44J 40P6 44Q	Industrial (-40°C to 85°C)
33	4.5V to 5.5V	AT89S8252-33AC AT89S8252-33JC AT89S8252-33PC AT89S8252-33QC	44A 44J 40P6 44Q	Commercial (0°C to 70°C)

= Preliminary Information

	Package Type
4A	44-lead, Thin Plastic Gull Wing Quad Flatpack (TQFP)
4J	44-lead, Plastic J-leaded Chip Carrier (PLCC)
0P6	40-lead, 0.600" Wide, Plastic Dual Inline Package (PDIP)
4Q	44-lead, Plastic Gull Wing Quad Flatpack (PQFP)

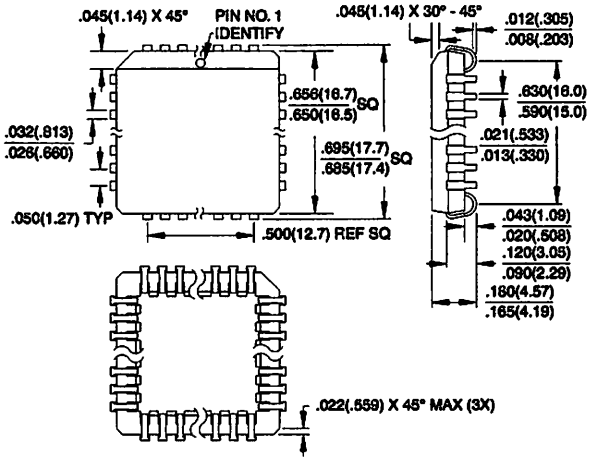
ackaging Information

44A, 44-lead, Thin (1.0 mm) Plastic Gull Wing Quad Flatpack (TQFP)
Dimensions in Millimeters and (Inches)*
JEDEC STANDARD MS-026 ACB

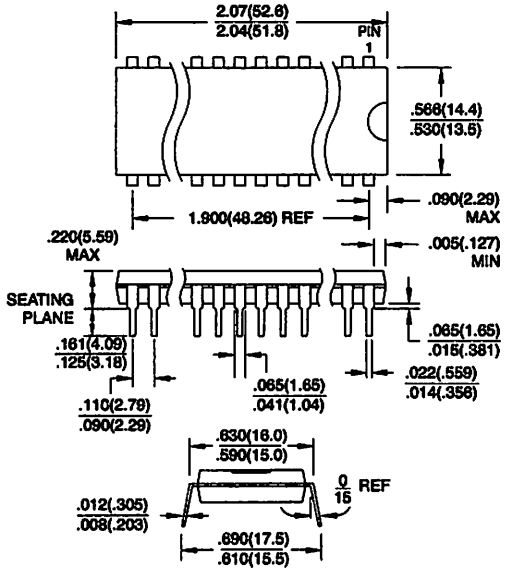


Controlling dimension: millimeters

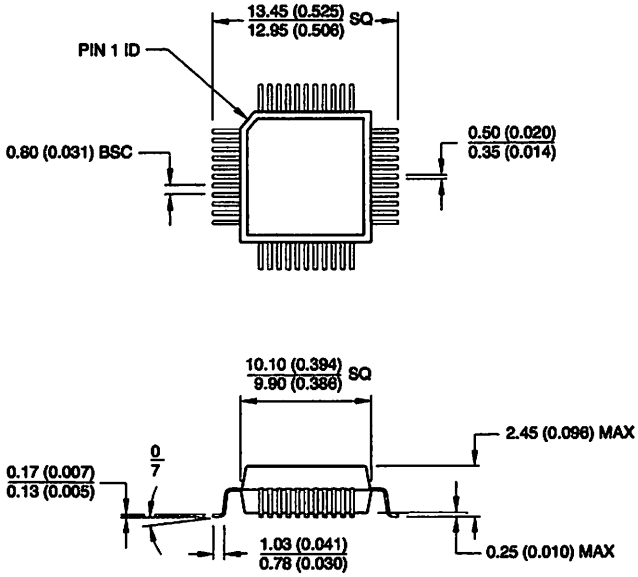
44J, 44-lead, Plastic J-leaded Chip Carrier (PLCC)
Dimensions in Inches and (Millimeters)
JEDEC STANDARD MS-018 AC



40P6, 40-lead, 0.600" Wide, Plastic Dual Inline Package (PDIP)
Dimensions in Inches and (Millimeters)



44Q, 44-lead, Plastic Quad Flat Package (PQFP)
Dimensions in Millimeters and (Inches)*
JEDEC STANDARD MS-022 AB



Controlling dimension: millimeters

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19-0175; Rev 3; 5/96

MAXIM

±15kV ESD-Protected, +5V RS-232 Transceivers

General Description

The MAX202E–MAX213E, MAX232E/MAX241E line drivers/receivers are designed for RS-232 and V.28 communications in harsh environments. Each transmitter output and receiver input is protected against ±15kV electrostatic discharge (ESD) shocks, without latchup. The various combinations of features are outlined in the *Selection Guide*. The drivers and receivers for all ten devices meet all EIA/TIA-232E and CCITT V.28 specifications at data rates up to 120kbps, when loaded in accordance with the EIA/TIA-232E specification.

The MAX211E/MAX213E/MAX241E are available in 28-pin SO packages, as well as a 28-pin SSOP that uses 60% less board space. The MAX202E/MAX232E come in 16-pin narrow SO, wide SO, and DIP packages. The MAX203E comes in a 20-pin DIP/SO package, and needs no external charge-pump capacitors. The MAX205E comes in a 24-pin wide DIP package, and also eliminates external charge-pump capacitors. The MAX206E/MAX207E/MAX208E come in 24-pin SO, SSOP, and narrow DIP packages. The MAX232E/MAX241E operate with four 1µF capacitors, while the MAX202E/MAX206E/MAX207E/MAX208E/MAX211E/MAX213E operate with four 0.1µF capacitors, further reducing cost and board space.

Applications

Notebook, Subnotebook, and Palmtop Computers
Battery-Powered Equipment
Hand-Held Equipment

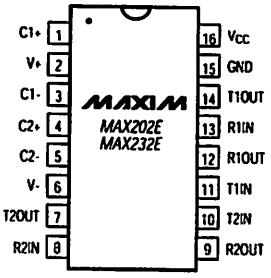
Ordering Information appears at end of data sheet.

Features

- **ESD Protection for RS-232 I/O Pins:**
  ±15kV—Human Body Model
  ±8kV—IEC1000-4-2, Contact Discharge
  ±15kV—IEC1000-4-2, Air-Gap Discharge
- **Latchup Free (unlike bipolar equivalents)**
- **Guaranteed 120kbps Data Rate—LapLink™ Compatible**
- **Guaranteed 3V/µs Min Slew Rate**
- **Operate from a Single +5V Power Supply**

Pin Configurations

TOP VIEW



DIP/SO

Pin Configurations and Typical Operating Circuits continued at end of data sheet.

Selection Guide

PART	No. of RS-232 DRIVERS	No. of RS-232 RECEIVERS	RECEIVERS ACTIVE IN SHUTDOWN	No. of EXTERNAL CAPACITORS	LOW-POWER SHUTDOWN	TTL THREE-STATE
MAX202E	2	2	0	4 (0.1µF)	No	No
MAX203E	2	2	0	None	No	No
MAX205E	5	5	0	None	Yes	Yes
MAX206E	4	3	0	4 (0.1µF)	Yes	Yes
MAX207E	5	3	0	4 (0.1µF)	No	No
MAX208E	4	4	0	4 (0.1µF)	No	No
MAX211E	4	5	0	4 (0.1µF)	Yes	Yes
MAX213E	4	5	2	4 (0.1µF)	Yes	Yes
MAX232E	2	2	0	4 (1µF)	No	No
MAX241E	4	5	0	4 (1µF)	Yes	Yes

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ABSOLUTE MAXIMUM RATINGS

VCC .....-0.3V to +6V
V+ .....(VCC - 0.3V) to +14V
V- .....-14V to +0.3V
Input Voltages
T_IN .....-0.3V to (V+ + 0.3V)
R_IN .....±30V
Output Voltages
T_OUT .....(V- - 0.3V) to (V+ + 0.3V)
R_OUT .....-0.3V to (VCC + 0.3V)
Short-Circuit Duration, T_OUT .....Continuous
Continuous Power Dissipation (TA = +70°C)
16-Pin Plastic DIP (derate 10.53mW/°C above +70°C) 842mW
16-Pin Narrow SO (derate 8.70mW/°C above +70°C) 696mW
16-Pin Wide SO (derate 9.52mW/°C above +70°C) 762mW
20-Pin Plastic DIP (derate 11.11mW/°C above +70°C)...889mW
20-Pin SO (derate 10.00mW/°C above +70°C).....800mW
24-Pin Narrow Plastic DIP
(derate 13.33mW/°C above +70°C) 1.07W
24-Pin Wide Plastic DIP
(derate 14.29mW/°C above +70°C).....1.14W
24-Pin SO (derate 11.76mW/°C above +70°C).....941mW
24-Pin SSOP (derate 8.00mW/°C above +70°C) 640mW
28-Pin SO (derate 12.50mW/°C above +70°C).....1W
28-Pin SSOP (derate 9.52mW/°C above +70°C) 762mW
Operating Temperature Ranges
MAX2_ _FC_ _ .....0°C to +70°C
MAX2_ _EE_ _ .....-40°C to +85°C
Storage Temperature Range .....-65°C to +165°C
Lead Temperature (soldering, 10sec) .....+300°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability

ELECTRICAL CHARACTERISTICS

(VCC = +5V ±10% for MAX202E/206E/208E/211E/213E/232E/241E; VCC = +5V ±5% for MAX203E/205E/207E; C1–C4 = 0.1µF for MAX202E/206E/207E/208E/211E/213E; C1–C4 = 1µF for MAX232E/241E; TA = TMIN to TMAX; unless otherwise noted. Typical values are at TA = +25°C.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
DC CHARACTERISTICS							
VCC Supply Current	ICC	No load, TA = +25°C	MAX202E/203E		8	15	mA
			MAX205E–208E		11	20	
			MAX211E/213E		14	20	
			MAX232E		5	10	
			MAX241E		7	15	
Shutdown Supply Current		TA = +25°C, Figure 1	MAX205E/206E		1	10	µA
			MAX211E/241E		1	10	
			MAX213E		15	50	
LOGIC							
Input Pull-Up Current		T_IN = 0V (MAX205E–208E/211E/213E/241E)			15	200	µA
Input Leakage Current		T_IN = 0V to VCC (MAX202E/203E/232E)				±10	µA
Input Threshold Low	VIL	T_IN; EN, $\overline{SHDN}$ (MAX213E) or $\overline{EN}$, SHDN (MAX205E–208E/211E/241E)				0.8	V
Input Threshold High	VIH	T_IN		2.0			V
		EN, $\overline{SHDN}$ (MAX213E) or $\overline{EN}$, SHDN (MAX205E–208E/211E/241E)		2.4			
Output Voltage Low	VOL	R_OUT; IOUT = 3.2mA (MAX202E/203E/232E) or IOUT = 1.6mA (MAX205E/208E/211E/213E/241E)				0.4	V
Output Voltage High	VOH	R_OUT; IOUT = -1.0mA		3.5	VCC - 0.4		V
Output Leakage Current		$\overline{EN}$ = VCC, EN = 0V, 0V ≤ ROUT ≤ VCC. MAX205E–208E/211E/213E/241E outputs disabled			±0.05	±10	µA

ELECTRICAL CHARACTERISTICS (continued)

(V_{CC} = +5V ±10% for MAX202E/206E/208E/211E/213E/232E/241E; V_{CC} = +5V ±5% for MAX203E/205E/207E; C1–C4 = 0.1µF for MAX202E/206E/207E/208E/211E/213E; C1–C4 = 1µF for MAX232E/241E; T_A = T_{MIN} to T_{MAX}; unless otherwise noted. Typical values are at T_A = +25°C.)

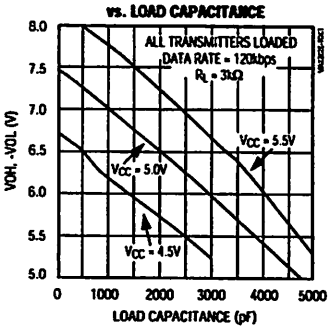
PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
EIA/TIA-232E RECEIVER INPUTS							
Input Voltage Range				-30		30	V
Input Threshold Low		T_A = +25°C, V_{CC} = 5V	All parts, normal operation	0.8	1.2		V
			MAX213E, $\overline{SHDN}$ = 0V, EN = V_{CC}	0.6	1.5		
Input Threshold High		T_A = +25°C, V_{CC} = 5V	All parts, normal operation		1.7	2.4	V
			MAX213E (R4, R5), $\overline{SHDN}$ = 0V, EN = V_{CC}		1.5	2.4	
Input Hysteresis		V_{CC} = 5V, no hysteresis in shutdown		0.2	0.5	1.0	V
Input Resistance		T_A = +25°C, V_{CC} = 5V		3	5	7	kΩ
EIA/TIA-232E TRANSMITTER OUTPUTS							
Output Voltage Swing		All drivers loaded with 3kΩ to ground (Note 1)		±5	±9		V
Output Resistance		V_{CC} = V+ = V- = 0V, V_{OUT} = ±2V		300			Ω
Output Short-Circuit Current					±10	±60	mA
TIMING CHARACTERISTICS							
Maximum Data Rate		R_L = 3kΩ to 7kΩ, C_L = 50pF to 1000pF, one transmitter switching		120			kbps
Receiver Propagation Delay	t_{PHLR}, t_{PHLR}	C_L = 150pF	All parts, normal operation		0.5	10	µs
			MAX213E (R4, R5), $\overline{SHDN}$ = 0V, EN = V_{CC}		4	40	
Receiver Output Enable Time		MAX205E/206E/211E/213E/241E normal operation, Figure 2			600		ns
Receiver Output Disable Time		MAX205E/206E/211E/213E/241E normal operation, Figure 2			200		ns
Transmitter Propagation Delay	t_{PLHT}, t_{PHLT}	R_L = 3kΩ, C_L = 2500pF, all transmitters loaded			2		µs
Transition-Region Slew Rate		T_A = +25°C, V_{CC} = 5V, R_L = 3kΩ to 7kΩ, C_L = 50pF to 1000pF, measured from -3V to +3V or +3V to -3V, Figure 3		3	6	30	V/µs
ESD PERFORMANCE: TRANSMITTER OUTPUTS, RECEIVER INPUTS							
ESD-Protection Voltage		Human Body Model			±15		kV
		IEC1000-4-2, Contact Discharge			±8		
		IEC1000-4-2, Air-Gap Discharge			±15		

Note 1: MAX211EE_ _ tested with V_{CC} = +5V ±5%.

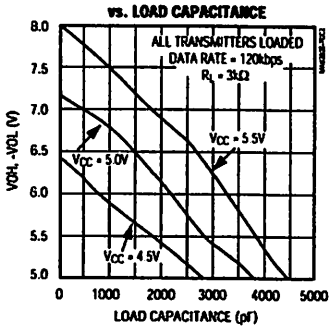
Typical Operating Characteristics

(Typical Operating Circuits, V_{CC} = +5V, T_A = +25°C, unless otherwise noted.)

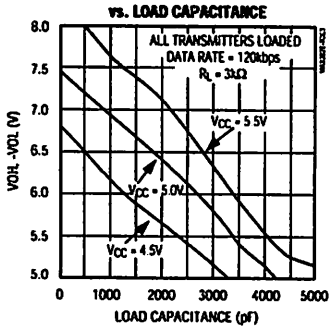
MAX232E
TRANSMITTER OUTPUT VOLTAGE
vs. LOAD CAPACITANCE



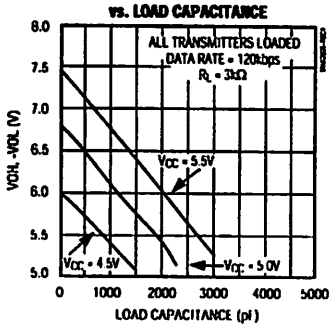
MAX202E/MAX203E
TRANSMITTER OUTPUT VOLTAGE
vs. LOAD CAPACITANCE



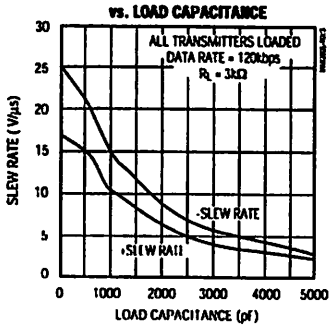
MAX241E
TRANSMITTER OUTPUT VOLTAGE
vs. LOAD CAPACITANCE



MAX211E/MAX213E
TRANSMITTER OUTPUT VOLTAGE
vs. LOAD CAPACITANCE



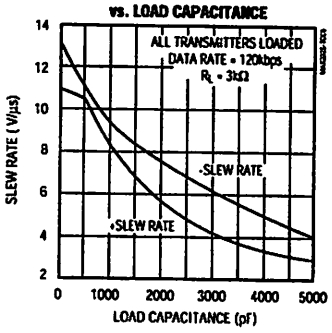
MAX211E/MAX213E/MAX241E
TRANSMITTER SLEW RATE
vs. LOAD CAPACITANCE



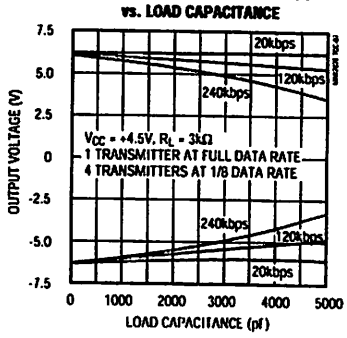
Typical Operating Characteristics (continued)

(Typical Operating Circuits, V_{CC} = +5V, T_A = +25°C, unless otherwise noted.)

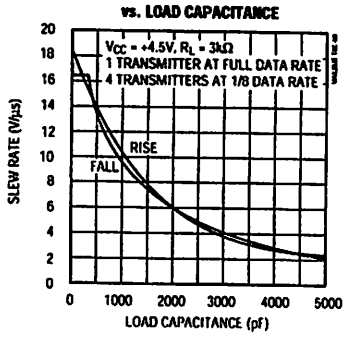
MAX202E/MAX203E/MAX232E TRANSMITTER SLEW RATE vs. LOAD CAPACITANCE



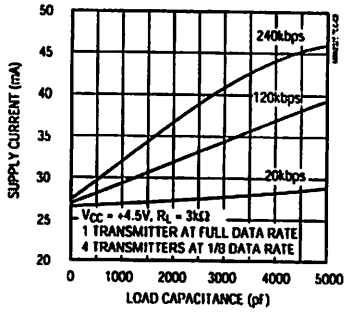
MAX205E–MAX208E TRANSMITTER OUTPUT VOLTAGE vs. LOAD CAPACITANCE



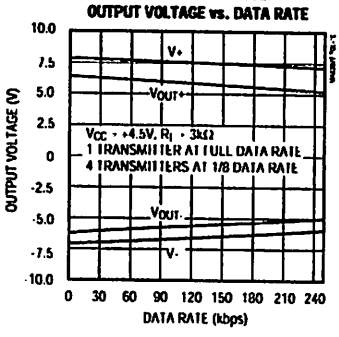
MAX205E–MAX208E TRANSMITTER SLEW RATE vs. LOAD CAPACITANCE



MAX205E–MAX208E SUPPLY CURRENT vs. LOAD CAPACITANCE



MAX205E–MAX208E OUTPUT VOLTAGE vs. DATA RATE



Pin Descriptions

MAX202E/MAX232E

PIN		NAME	FUNCTION
DIP/SO	LCC		
1, 3	2, 4	C1+, C1-	Terminals for positive charge-pump capacitor
2	3	V+	+2VCC voltage generated by the charge pump
4, 5	5, 7	C2+, C2-	Terminals for negative charge-pump capacitor
6	8	V-	-2VCC voltage generated by the charge pump
7, 14	9, 18	T_OUT	RS-232 Driver Outputs
8, 13	10, 17	R_IN	RS-232 Receiver Outputs
9, 12	12, 15	R_OUT	RS-232 Receiver Outputs
10, 11	13, 14	T_IN	RS-232 Driver Inputs
15	19	GND	Ground
16	20	VCC	+4.5V to +5.5V Supply-Voltage Input
—	1, 6, 11, 16	N.C.	No Connect—not internally connected.

MAX203E

PIN		NAME	FUNCTION
DIP	SO		
1, 2	1, 2	T_IN	RS-232 Driver Inputs
3, 20	3, 20	R_OUT	RS-232 Receiver Outputs
4,19	4, 19	R_IN	RS-232 Receiver Inputs
5,18	5, 18	T_OUT	RS-232 Transmitter Outputs
6, 9	6, 9	GND	Ground
7	7	VCC	+4.5V to +5.5V Supply-Voltage Input
8	13	C1+	Make no connection to this pin.
10, 16	11, 16	C2-	Connect pins together.
12, 17	10, 17	V-	-2VCC voltage generated by the charge pump. Connect pins together.
13	14	C1-	Make no connection to this pin.
14	8	V+	+2VCC voltage generated by the charge pump
11, 15	12, 15	C2+	Connect pins together.

MAX205E

PIN	NAME	FUNCTION
1–4, 19	T_OUT	RS-232 Driver Outputs
5, 10, 13, 18, 24	R_IN	RS-232 Receiver Inputs
6, 9, 14, 17, 23	R_OUT	TTL/CMOS Receiver Outputs. All receivers are inactive in shutdown.
7, 8, 15, 16, 22	T_IN	TTL/CMOS Driver Inputs. Internal pull-ups to VCC.
11	GND	Ground
12	VCC	+4.75V to +5.25V Supply Voltage
20	$\overline{EN}$	Receiver Enable—active low
21	SHDN	Shutdown Control—active high

Pin Descriptions (continued)

MAX206E

PIN	NAME	FUNCTION
1, 2, 3, 24	T_OUT	RS-232 Driver Outputs
4, 16, 23	R_IN	RS-232 Receiver Inputs
5, 17, 22	R_OUT	TTL/CMOS Receiver Outputs. All receivers are inactive in shutdown.
6, 7, 18, 19	T_IN	TTL/CMOS Driver Inputs. Internal pull-ups to V_{CC}.
8	GND	Ground
9	V_{CC}	+4.5V to +5.5V Supply Voltage
10, 12	C1+, C1-	Terminals for positive charge-pump capacitor
11	V+	+2V_{CC} generated by the charge pump
13, 14	C2+, C2-	Terminals for negative charge-pump capacitor
15	V-	-2V_{CC} generated by the charge pump
20	$\overline{EN}$	Receiver Enable—active low
21	SHDN	Shutdown Control—active high

MAX207E

PIN	NAME	FUNCTION
1, 2, 3, 20, 24	T_OUT	RS-232 Driver Outputs
4, 16, 23	R_IN	RS-232 Receiver Inputs
5, 17, 22	R_OUT	TTL/CMOS Receiver Outputs. All receivers are inactive in shutdown.
6, 7, 18, 19, 21	T_IN	TTL/CMOS Driver Inputs. Internal pull-ups to V_{CC}.
8	GND	Ground
9	V_{CC}	+4.75V to +5.25V Supply Voltage
10, 12	C1+, C1-	Terminals for positive charge-pump capacitor
11	V+	+2V_{CC} generated by the charge pump
13, 14	C2+, C2-	Terminals for negative charge-pump capacitor
15	V-	-2V_{CC} generated by the charge pump

MAX208E

PIN	NAME	FUNCTION
1, 2, 20, 24	T_OUT	RS-232 Driver Outputs
3, 7, 16, 23	R_IN	RS-232 Receiver Inputs
4, 6, 17, 22	R_OUT	TTL/CMOS Receiver Outputs. All receivers are inactive in shutdown.
5, 18, 19, 21	T_IN	TTL/CMOS Driver Inputs. Internal pull-ups to V_{CC}.
8	GND	Ground
9	V_{CC}	+4.5V to +5.5V Supply Voltage
10, 12	C1+, C1-	Terminals for positive charge-pump capacitor
11	V+	+2V_{CC} generated by the charge pump
13, 14	C2+, C2-	Terminals for negative charge-pump capacitor
15	V-	-2V_{CC} generated by the charge pump

Pin Descriptions (continued)

MAX211E/MAX213E/MAX241E

PIN	NAME	FUNCTION
1, 2, 3, 28	T_OUT	RS-232 Driver Outputs
4, 9, 18, 23, 27	R_IN	RS-232 Receiver Inputs
5, 8, 19, 22, 26	R_OUT	TTL/CMOS Receiver Outputs. For the MAX213E, receivers R4 and R5 are active in shutdown mode when EN = 1. For the MAX211E and MAX241E, all receivers are inactive in shutdown.
6, 7, 20, 21	T_IN	TTL/CMOS Driver Inputs. Only the MAX211E, MAX213E, and MAX241E have internal pull-ups to V_{CC}.
10	GND	Ground
11	V_{CC}	+4.5V to +5.5V Supply Voltage
12, 14	C1+, C1-	Terminals for positive charge-pump capacitor
13	V+	+2V_{CC} voltage generated by the charge pump
15, 16	C2+, C2-	Terminals for negative charge-pump capacitor
17	V-	-2V_{CC} voltage generated by the charge pump
24	$\overline{EN}$	Receiver Enable—active low (MAX211E, MAX241E)
	EN	Receiver Enable—active high (MAX213E)
25	SHDN	Shutdown Control—active high (MAX211E, MAX241E)
	$\overline{SHDN}$	Shutdown Control—active low (MAX213E)

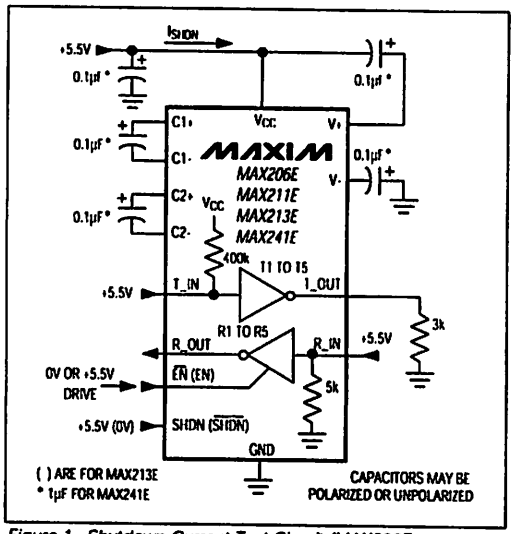


Figure 1. Shutdown-Current Test Circuit (MAX206E, MAX211E/MAX213E/MAX241E)

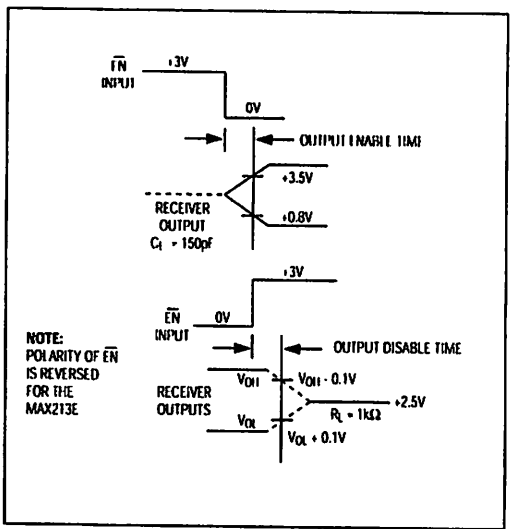


Figure 2. Receiver Output Enable and Disable Timing (MAX205E/MAX206E/MAX211E/MAX213E/MAX241E)

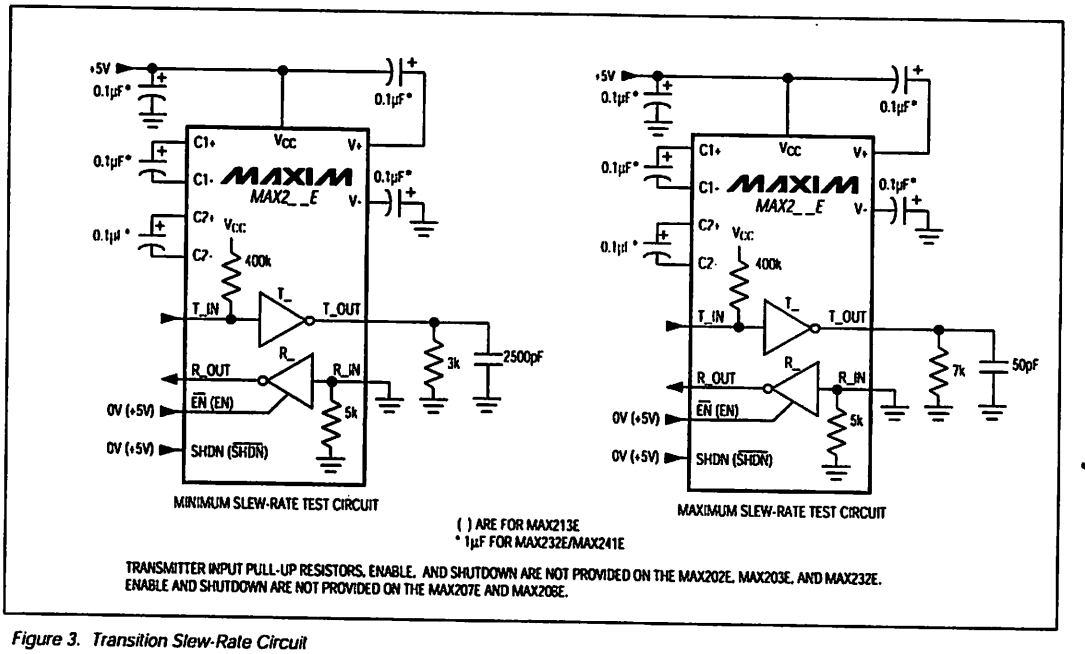


Figure 3. Transition Slew-Rate Circuit

Detailed Description

The MAX202E–MAX213E, MAX232E/MAX241E consist of three sections: charge-pump voltage converters, drivers (transmitters), and receivers. These E versions provide extra protection against ESD. They survive ±15kV discharges to the RS-232 inputs and outputs, tested using the Human Body Model. When tested according to IEC1000-4-2, they survive ±8kV contact-discharges and ±15kV air-gap discharges. The rugged E versions are intended for use in harsh environments or applications where the RS-232 connection is frequently changed (such as notebook computers). The standard (non-"E") MAX202, MAX203, MAX205–MAX208, MAX211, MAX213, MAX232, and MAX241 are recommended for applications where cost is critical.

+5V to ±10V Dual Charge-Pump Voltage Converter

The +5V to ±10V conversion is performed by dual charge-pump voltage converters (Figure 4). The first charge-pump converter uses capacitor C1 to double the +5V into +10V, storing the +10V on the output filter capacitor, C3. The second uses C2 to invert the +10V into -10V, storing the -10V on the V- output filter capacitor, C4.

In shutdown mode, V+ is internally connected to Vcc by a 1kΩ pull-down resistor, and V- is internally connected to ground by a 1kΩ pull-up resistor.

RS-232 Drivers

With Vcc = 5V, the typical driver output voltage swing is ±8V when loaded with a nominal 5kΩ RS-232 receiver. The output swing is guaranteed to meet EIA/TIA-232E and V.28 specifications that call for ±5V minimum output levels under worst-case conditions. These include a 3kΩ load, minimum Vcc, and maximum operating temperature. The open-circuit output voltage swings from (V+ - 0.6V) to V-.

Input thresholds are CMOS/TTL compatible. The unused drivers' inputs on the MAX205E–MAX208E, MAX211E, MAX213E, and MAX241E can be left unconnected because 400kΩ pull-up resistors to Vcc are included on-chip. Since all drivers invert, the pull-up resistors force the unused drivers' outputs low. The MAX202E, MAX203E, and MAX232E do not have pull-up resistors on the transmitter inputs.

When in low-power shutdown mode, the MAX205E/MAX206E/MAX211E/MAX213E/MAX241E driver outputs are turned off and draw only leakage currents—even if they are back-driven with voltages between 0V and 12V. Below -0.5V in shutdown, the transmitter output is diode-clamped to ground with a 1kΩ series impedance.

RS-232 Receivers

The receivers convert the RS-232 signals to CMOS-logic output levels. The guaranteed 0.8V and 2.4V receiver input thresholds are significantly tighter than the ±3V thresholds required by the EIA/TIA-232E specification. This allows the receiver inputs to respond to TTL/CMOS-logic levels, as well as RS-232 levels.

The guaranteed 0.8V input low threshold ensures that receivers shorted to ground have a logic 1 output. The 5kΩ input resistance to ground ensures that a receiver with its input left open will also have a logic 1 output.

Receiver inputs have approximately 0.5V hysteresis. This provides clean output transitions, even with slow rise/fall-time signals with moderate amounts of noise and ringing.

In shutdown, the MAX213E's R4 and R5 receivers have no hysteresis.

Shutdown and Enable Control (MAX205E/MAX206E/MAX211E/MAX213E/MAX241E)

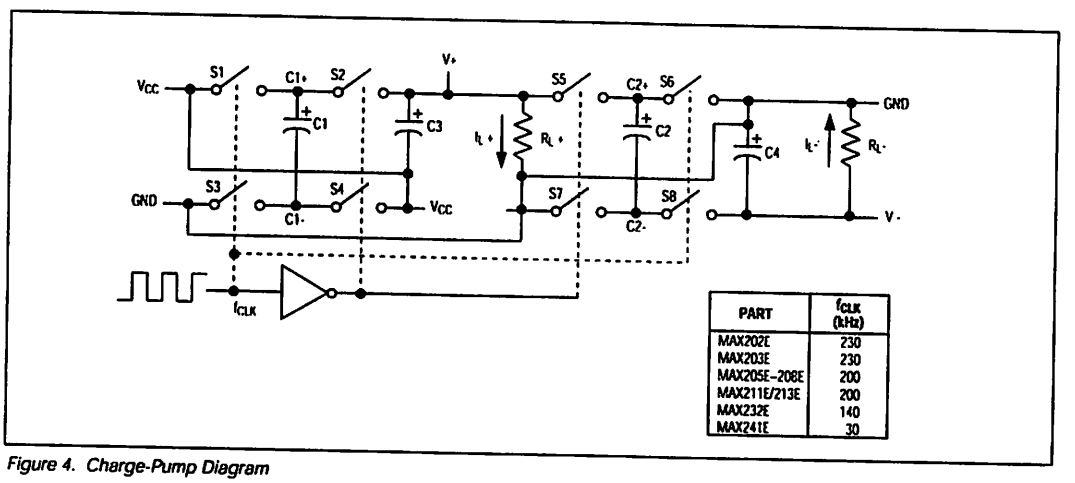
In shutdown mode, the charge pumps are turned off, V+ is pulled down to Vcc, V- is pulled to ground, and the transmitter outputs are disabled. This reduces supply current typically to 1µA (15µA for the MAX213E). The time required to exit shutdown is under 1ms, as shown in Figure 5.

Receivers

All MAX213E receivers, except R4 and R5, are put into a high-impedance state in shutdown mode (see Tables 1a and 1b). The MAX213E's R4 and R5 receivers still function in shutdown mode. These two awake-in-shutdown receivers can monitor external activity while maintaining minimal power consumption.

The enable control is used to put the receiver outputs into a high-impedance state, to allow wire-OR connection of two EIA/TIA-232E ports (or ports of different types) at the UART. It has no effect on the RS-232 drivers or the charge pumps.

Note: The enable control pin is active low for the MAX211E/MAX241E (EN), but is active high for the MAX213E (EN). The shutdown control pin is active high for the MAX205E/MAX206E/MAX211E/MAX241E (SHDN), but is active low for the MAX213E (SHDN).



PART	f_{CLK} (kHz)
MAX202E	230
MAX203E	230
MAX205E–208E	200
MAX211E/213E	200
MAX232E	140
MAX241E	30

Figure 4. Charge-Pump Diagram

The MAX213E's receiver propagation delay is typically 0.5µs in normal operation. In shutdown mode, propagation delay increases to 4µs for both rising and falling transitions. The MAX213E's receiver inputs have approximately 0.5V hysteresis, except in shutdown, when receivers R4 and R5 have no hysteresis.

When entering shutdown with receivers active, R4 and R5 are not valid until 80µs after $\overline{SHDN}$ is driven low. When coming out of shutdown, all receiver outputs are invalid until the charge pumps reach nominal voltage levels (less than 2ms when using 0.1µF capacitors).

±15kV ESD Protection

As with all Maxim devices, ESD-protection structures are incorporated on all pins to protect against electrostatic discharges encountered during handling and assembly. The driver outputs and receiver inputs have extra protection against static electricity. Maxim's engineers developed state-of-the-art structures to protect these pins against ESD of ±15kV without damage. The ESD structures withstand high ESD in all states: normal operation, shutdown, and powered down. After an ESD event, Maxim's E versions keep working without latchup, whereas competing RS-232 products can latch and must be powered down to remove latchup.

ESD protection can be tested in various ways; the transmitter outputs and receiver inputs of this product family are characterized for protection to the following limits:

1) ±15kV using the Human Body Model
2) ±8kV using the contact-discharge method specified in IEC1000-4-2
3) ±15kV using IEC1000-4-2's air-gap method.

ESD Test Conditions

ESD performance depends on a variety of conditions. Contact Maxim for a reliability report that documents test set-up, test methodology, and test results.

Human Body Model

Figure 6a shows the Human Body Model, and Figure 6b shows the current waveform it generates when discharged into a low impedance. This model consists of a 100pF capacitor charged to the ESD voltage of interest, which is then discharged into the test device through a 1.5kΩ resistor.

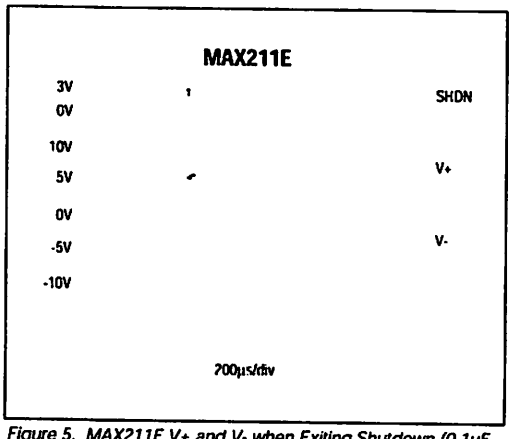


Figure 5. MAX211E V+ and V- when Exiting Shutdown (0.1µF capacitors)

Table 1a. MAX205E/MAX206E/MAX211E/ MAX241E Control Pin Configurations

SHDN	EN	OPERATION STATUS	Tx	Rx
0	0	Normal Operation	All Active	All Active
0	1	Normal Operation	All Active	All High-Z
1	X	Shutdown	All High-Z	All High-Z

X = Don't Care

Table 1b. MAX213E Control Pin Configurations

$\overline{SHDN}$	EN	OPERATION STATUS	Tx 1–4	Rx	
				1–3	4, 5
0	0	Shutdown	All High-Z	High-Z	High-Z
0	1	Shutdown	All High-Z	High-Z	Active*
1	0	Normal Operation	All Active	High-Z	High-Z
1	1	Normal Operation	All Active	Active	Active

**Active = active with reduced performance*

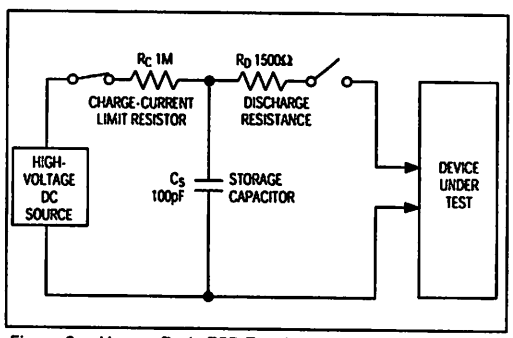


Figure 6a. Human Body ESD Test Model

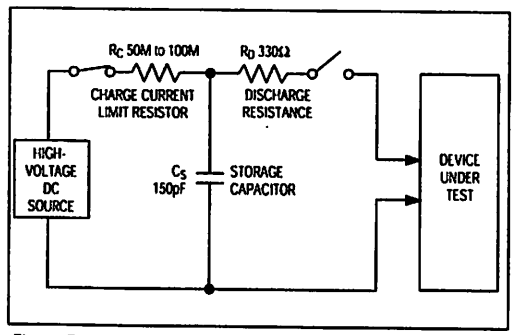


Figure 7a. IEC1000-4-2 ESD Test Model

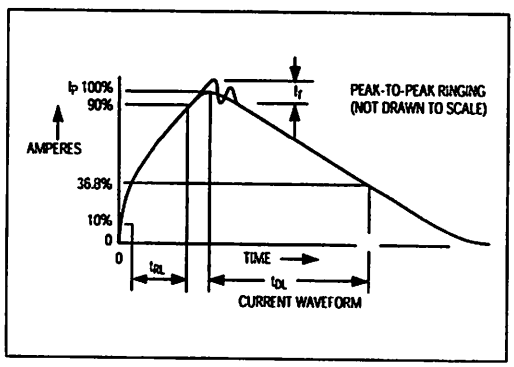


Figure 6b. Human Body Model Current Waveform

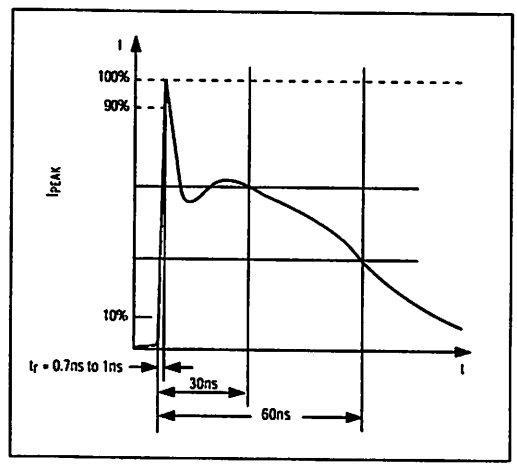


Figure 7b. IEC1000-4-2 ESD Generator Current Waveform

IEC1000-4-2

The IEC1000-4-2 standard covers ESD testing and performance of finished equipment; it does not specifically refer to integrated circuits. The MAX202E/MAX203E–MAX213E, MAX232E/MAX241E help you design equipment that meets level 4 (the highest level) of IEC1000-4-2, without the need for additional ESD-protection components.

The major difference between tests done using the Human Body Model and IEC1000-4-2 is higher peak current in IEC1000-4-2, because series resistance is lower in the IEC1000-4-2 model. Hence, the ESD withstand voltage measured to IEC1000-4-2 is generally lower than that measured using the Human Body Model. Figure 7b shows the current waveform for the 8kV IEC1000-4-2 level-four ESD contact-discharge test.

The air-gap test involves approaching the device with a charged probe. The contact-discharge method connects the probe to the device before the probe is energized.

Machine Model

The Machine Model for ESD tests all pins using a 200pF storage capacitor and zero discharge resistance. Its objective is to emulate the stress caused by contact that occurs with handling and assembly during manufacturing. Of course, all pins require this protection during manufacturing, not just RS-232 inputs and outputs. Therefore, after PC board assembly, the Machine Model is less relevant to I/O ports.

Applications Information

Capacitor Selection

The capacitor type used for C1–C4 is not critical for proper operation. The MAX202E, MAX206–MAX208E, MAX211E, and MAX213E require 0.1µF capacitors, and the MAX232E and MAX241E require 1µF capacitors, although in all cases capacitors up to 10µF can be used without harm. Ceramic, aluminum-electrolytic, or tantalum capacitors are suggested for the 1µF capacitors, and ceramic dielectrics are suggested for the 0.1µF capacitors. When using the minimum recommended capacitor values, make sure the capacitance value does not degrade excessively as the operating temperature varies. If in doubt, use capacitors with a larger (e.g., 2x) nominal value. The capacitors' effective series resistance (ESR), which usually rises at low temperatures, influences the amount of ripple on V+ and V-.

Use larger capacitors (up to 10µF) to reduce the output impedance at V+ and V-. This can be useful when "stealing" power from V+ or from V-. The MAX203E and MAX205E have internal charge-pump capacitors.

Bypass V_{CC} to ground with at least 0.1µF. In applications sensitive to power-supply noise generated by the charge pumps, decouple V_{CC} to ground with a capacitor the same size as (or larger than) the charge-pump capacitors (C1–C4).

V+ and V- as Power Supplies

A small amount of power can be drawn from V+ and V-, although this will reduce both driver output swing and noise margins. Increasing the value of the charge-pump capacitors (up to 10µF) helps maintain performance when power is drawn from V+ or V-.

Driving Multiple Receivers

Each transmitter is designed to drive a single receiver. Transmitters can be paralleled to drive multiple receivers.

Driver Outputs when Exiting Shutdown

The driver outputs display no ringing or undesirable transients as they come out of shutdown.

High Data Rates

These transceivers maintain the RS-232 ±5.0V minimum driver output voltages at data rates of over 120kbps. For data rates above 120kbps, refer to the Transmitter Output Voltage vs. Load Capacitance graphs in the *Typical Operating Characteristics*. Communication at these high rates is easier if the capacitive loads on the transmitters are small; i.e., short cables are best.

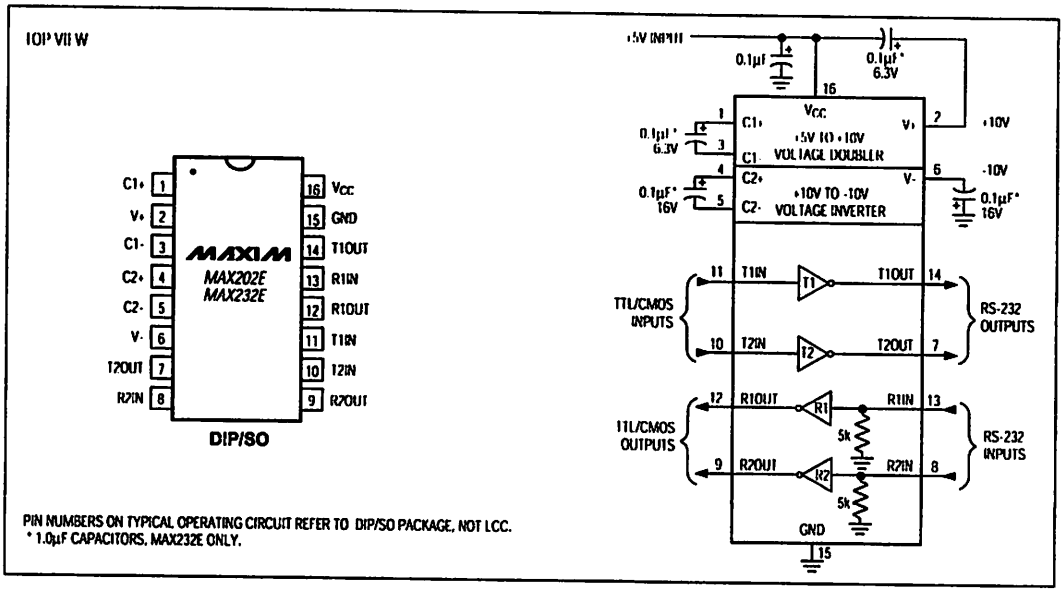
Table 2. Summary of EIA/TIA-232E, V.28 Specifications

PARAMETER		CONDITIONS	EIA/TIA-232E, V.28 SPECIFICATIONS
Driver Output Voltage	0 Level	3kΩ to 7kΩ load	+5V to +15V
	1 Level	3kΩ to 7kΩ load	-5V to -15V
Driver Output Level, Max		No load	±25V
Data Rate		3kΩ ≤ R_L ≤ 7kΩ, C_L ≤ 2500pF	Up to 20kbps
Receiver Input Voltage	0 Level		+3V to +15V
	1 Level		-3V to -15V
Receiver Input Level			±25V
Instantaneous Slew Rate, Max		3kΩ ≤ R_L ≤ 7kΩ, C_L ≤ 2500pF	30V/µs
Driver Output Short-Circuit Current, Max			100mA
Transition Rate on Driver Output		V.28	1ms or 3% of the period
		EIA/TIA-232E	4% of the period
Driver Output Resistance		-2V < V_{OUT} < +2V	300Ω

Table 3. DB9 Cable Connections Commonly Used for EIA/TIAE-232E and V.24 Asynchronous Interfaces

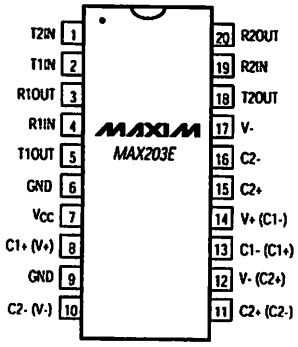
PIN	CONNECTION	
1	Received Line Signal Detector (sometimes called Carrier Detect. DCD)	Handshake from DCE
2	Receive Data (RD)	Data from DCE
3	Transmit Data (TD)	Data from DTE
4	Data Terminal Ready	Handshake from DTE
5	Signal Ground	Reference point for signals
6	Data Set Ready (DSR)	Handshake from DCE
7	Request to Send (RTS)	Handshake from DTE
8	Clear to Send (CTS)	Handshake from DCE
9	Ring Indicator	Handshake from DCE

Pin Configurations and Typical Operating Circuits (continued)



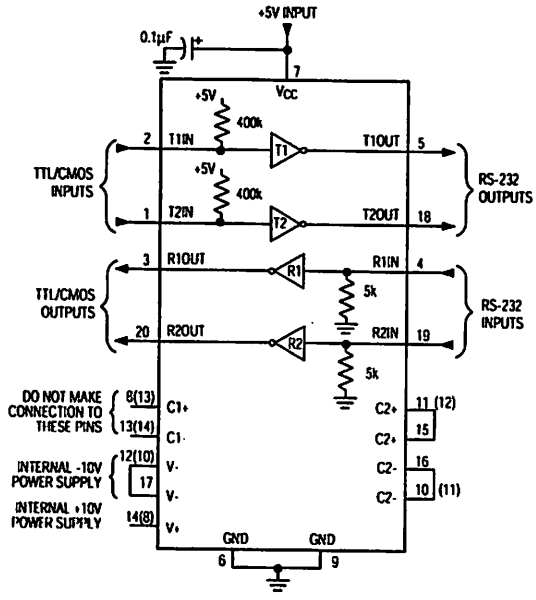
Pin Configurations and Typical Operating Circuits (continued)

TOP VIEW



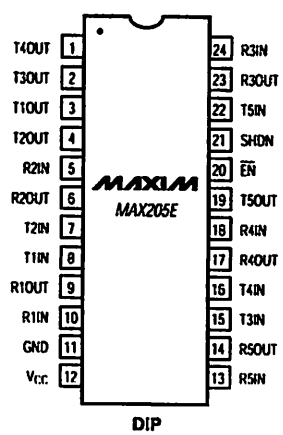
DIP/SO

PIN NUMBERS IN ( ) ARE FOR SO PACKAGE.



Pin Configurations and Typical Operating Circuits (continued)

TOP VIEW



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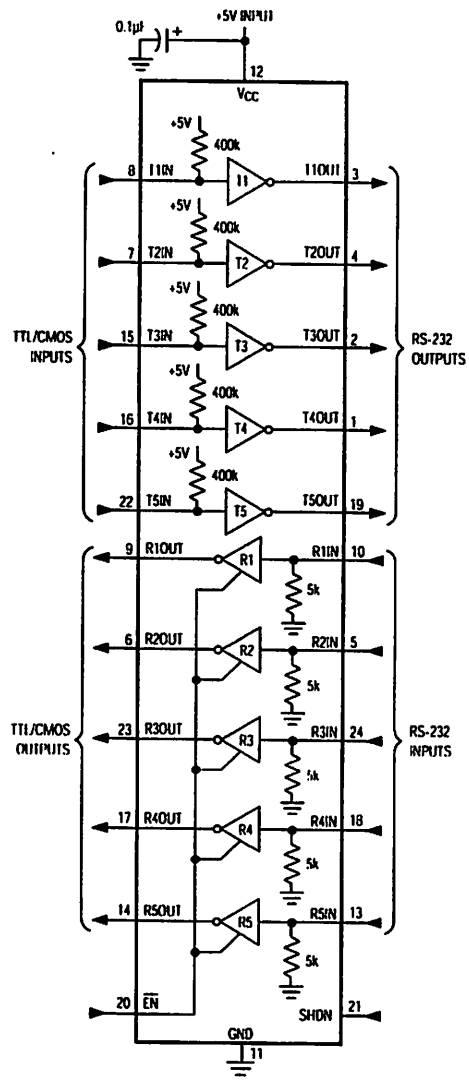
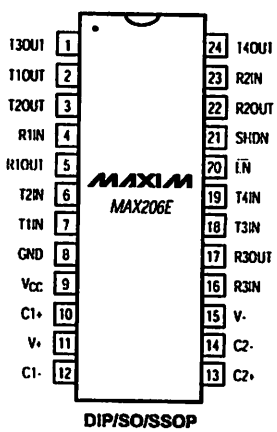
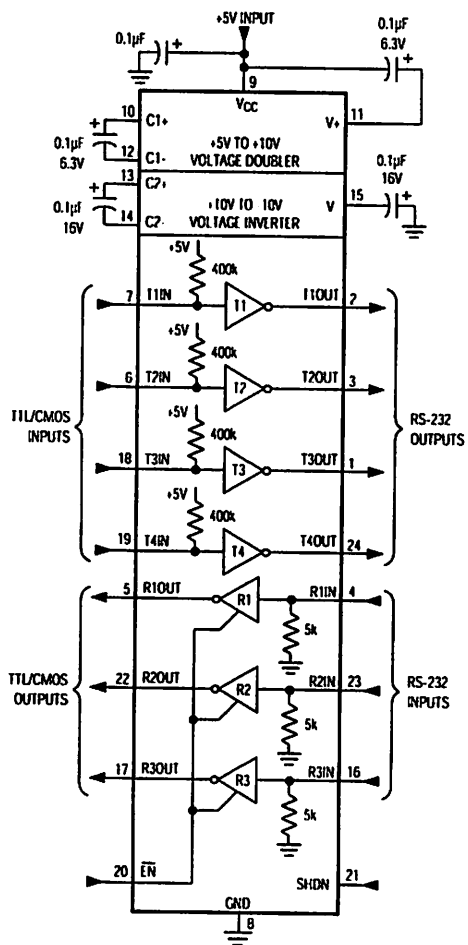


Pin Configurations and Typical Operating Circuits (continued)

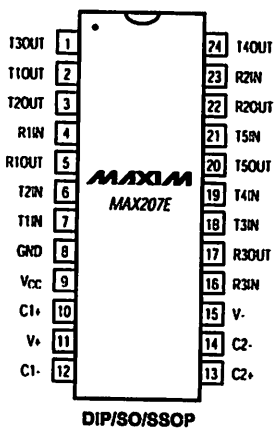
TOP VIEW





Pin Configurations and Typical Operating Circuits (continued)

TOP VIEW



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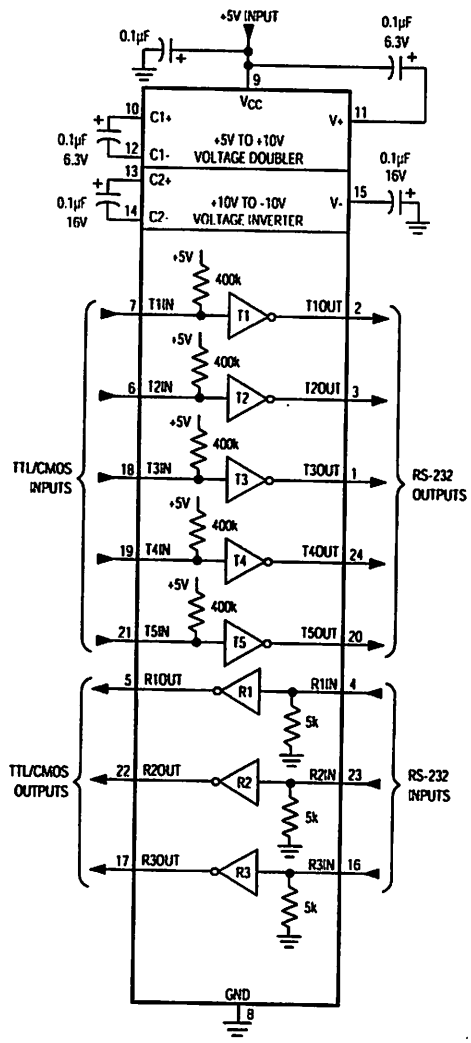
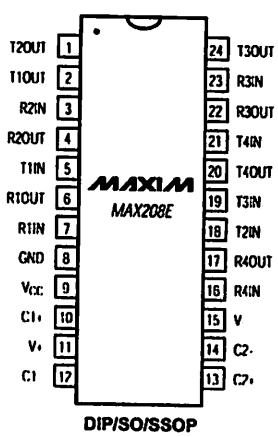
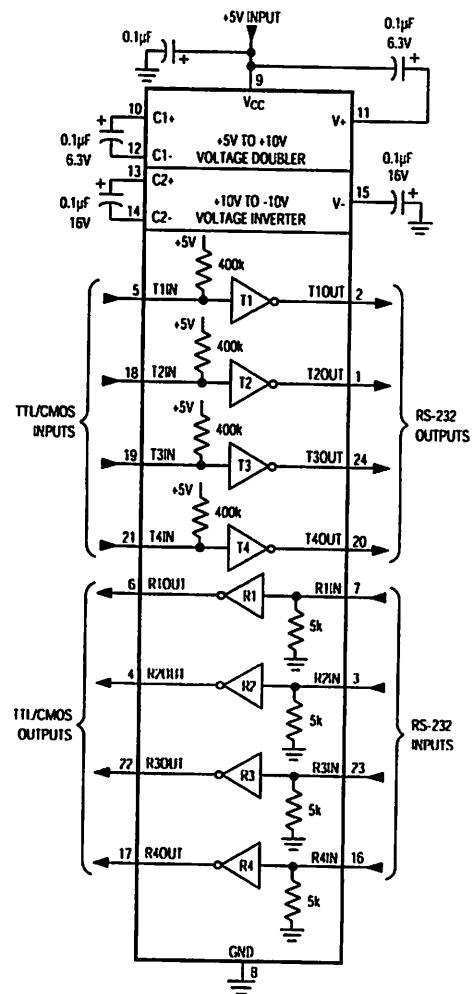


Pin Configurations and Typical Operating Circuits (continued)

TOP VIEW



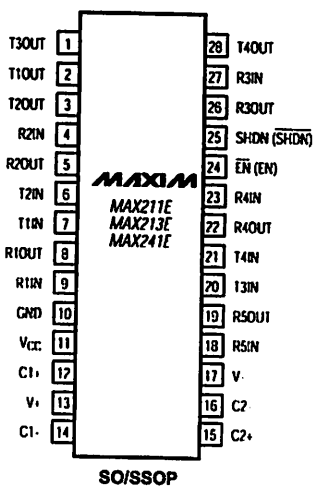
DIP/SO/SSOP



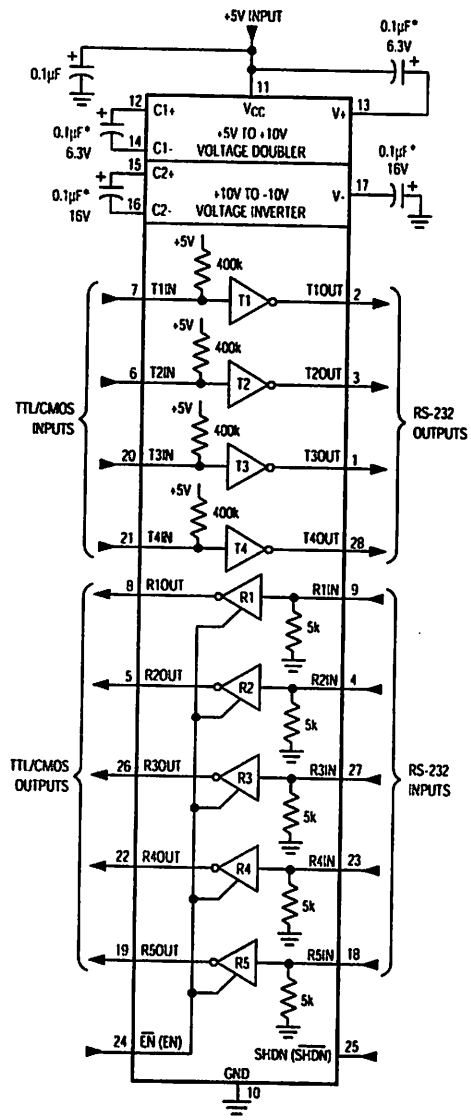
±15kV ESD-Protected, +5V RS-232 Transceivers

Pin Configurations and Typical Operating Circuits (continued)

TOP VIEW

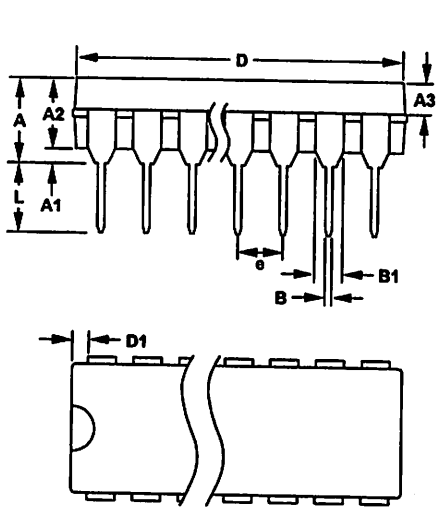


SO/SSOP



( ) ARE FOR MAX213E ONLY
* 1.0µF CAPACITORS, MAX241E ONLY

Package Information

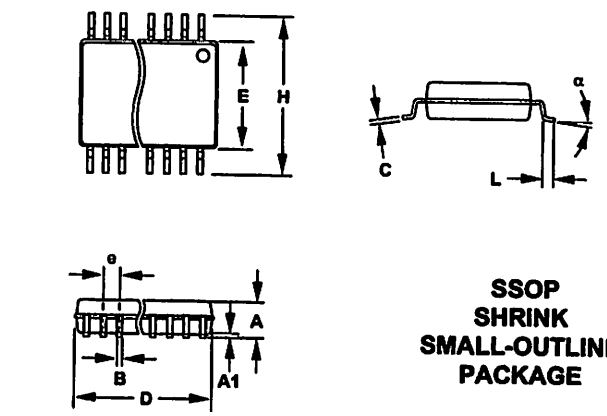


Plastic DIP
PLASTIC
DUAL-IN-LINE
PACKAGE
(0.300 in.)

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	–	0.200	–	5.08
A1	0.015	–	0.38	–
A2	0.125	0.175	3.18	4.45
A3	0.055	0.080	1.40	2.03
B	0.016	0.022	0.41	0.56
B1	0.045	0.065	1.14	1.65
C	0.008	0.012	0.20	0.30
D1	0.005	0.080	0.13	2.03
E	0.300	0.325	7.62	8.26
E1	0.240	0.310	6.10	7.87
e	0.100	–	2.54	–
eA	0.300	–	7.62	–
eB	–	0.400	–	10.16
L	0.115	0.150	2.92	3.81

PKG.	DIM	PINS	INCHES		MILLIMETERS	
			MIN	MAX	MIN	MAX
P	D	8	0.348	0.390	8.84	9.91
P	D	14	0.735	0.765	18.67	19.43
P	D	16	0.745	0.765	18.92	19.43
P	D	18	0.885	0.915	22.48	23.24
P	D	20	1.015	1.045	25.78	26.54
N	D	24	1.14	1.265	28.96	32.13

21-0043A



SSOP
SHRINK
SMALL-OUTLINE
PACKAGE

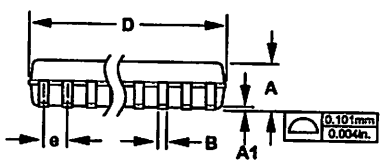
DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.068	0.078	1.73	1.99
A1	0.002	0.008	0.05	0.21
B	0.010	0.015	0.25	0.38
C	0.004	0.008	0.09	0.20
D	SEE VARIATIONS			
E	0.205	0.209	5.20	5.38
e	0.0256 BSC		0.65 BSC	
H	0.301	0.311	7.65	7.90
L	0.025	0.037	0.63	0.95
α	0°	8°	0°	8°

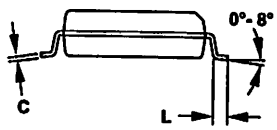
DIM	PINS	INCHES		MILLIMETERS	
		MIN	MAX	MIN	MAX
D	14	0.239	0.249	6.07	6.33
D	16	0.239	0.249	6.07	6.33
D	20	0.278	0.289	7.07	7.33
D	24	0.317	0.328	8.07	8.33
D	28	0.397	0.407	10.07	10.33

21-0056A

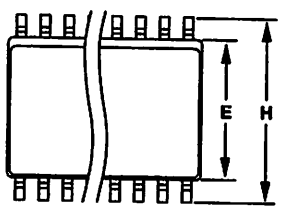
±15kV ESD-Protected, +5V RS-232 Transceivers

Package Information (continued)





DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.093	0.104	2.35	2.65
A1	0.004	0.012	0.10	0.30
B	0.014	0.019	0.35	0.49
C	0.009	0.013	0.23	0.32
E	0.291	0.299	7.40	7.60
e	0.050		1.27	
H	0.394	0.419	10.00	10.65
L	0.016	0.050	0.40	1.27



Wide SO
SMALL-OUTLINE
PACKAGE
(0.300 in.)

DIM	PINS	INCHES		MILLIMETERS	
		MIN	MAX	MIN	MAX
D	16	0.398	0.413	10.10	10.50
D	18	0.447	0.463	11.35	11.75
D	20	0.496	0.512	12.60	13.00
D	24	0.598	0.614	15.20	15.60
D	28	0.697	0.713	17.70	18.10

21-0042A

19-0273; Rev 7; 1/07

MAXIM

3.0V to 5.5V, Low-Power, up to 1Mbps, True RS-232 Transceivers Using Four 0.1µF External Capacitors

General Description

The MAX3222/MAX3232/MAX3237/MAX3241 transceivers have a proprietary low-dropout transmitter output stage enabling true RS-232 performance from a 3.0V to 5.5V supply with a dual charge pump. The devices require only four small 0.1µF external charge-pump capacitors. The MAX3222, MAX3232, and MAX3241 are guaranteed to run at data rates of 120kbps while maintaining RS-232 output levels. The MAX3237 is guaranteed to run at data rates of 250kbps in the normal operating mode and 1Mbps in the MegaBaud™ operating mode, while maintaining RS-232 output levels.

The MAX3222/MAX3232 have 2 receivers and 2 drivers. The MAX3222 features a 1µA shutdown mode that reduces power consumption and extends battery life in portable systems. Its receivers remain active in shutdown mode, allowing external devices such as modems to be monitored using only 1µA supply current. The MAX3222 and MAX3232 are pin, package, and functionally compatible with the industry-standard MAX242 and MAX232, respectively.

The MAX3241 is a complete serial port (3 drivers/5 receivers) designed for notebook and subnotebook computers. The MAX3237 (5 drivers/3 receivers) is ideal for fast modem applications. Both these devices feature a shutdown mode in which all receivers can remain active while using only 1µA supply current. Receivers R1 (MAX3237/MAX3241) and R2 (MAX3241) have extra outputs in addition to their standard outputs. These extra outputs are always active, allowing external devices such as a modem to be monitored without forward biasing the protection diodes in circuitry that may have VCC completely removed.

The MAX3222, MAX3237, and MAX3241 are available in space-saving TSSOP and SSOP packages.

Applications

Notebook, Subnotebook, and Palmtop Computers

High-Speed Modems

Battery-Powered Equipment

Hand-Held Equipment

Peripherals

Printers

Typical Operating Circuits appear at end of data sheet.

Next Generation Device Features

- **For Smaller Packaging: MAX3228E/MAX3229E: +2.5V to +5.5V RS-232 Transceivers in UCSP™**
- **For Integrated ESD Protection: MAX3222E/MAX3232E/MAX3237E/MAX3241E*/ MAX3246E: ±15kV ESD-Protected, Down to 10nA, 3.0V to 5.5V, Up to 1Mbps, True RS-232 Transceivers**
- **For Low-Voltage or Data Cable Applications: MAX3380E/MAX3381E: +2.35V to +5.5V, 1µA, 2 Tx/2 Rx RS-232 Transceivers with ±15kV ESD-Protected I/O and Logic Pins**

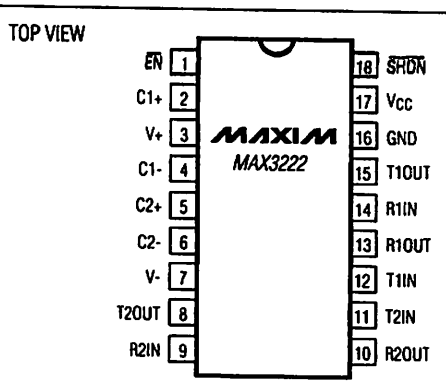
Ordering Information

PART	TEMP RANGE	PIN-PACKAGE	PKG CODE
MAX3222CUP+	0°C to +70°C	20 TSSOP	U20+2
MAX3222CAP+	0°C to +70°C	20 SSOP	A20+1
MAX3222CWN+	0°C to +70°C	18 SO	W18+1
MAX3222CPN+	0°C to +70°C	18 Plastic Dip	P18+5

+Denotes lead-free package.

Ordering Information continued at end of data sheet.

Pin Configurations



Pin Configurations continued at end of data sheet.

MegaBaud and UCSP are trademarks of Maxim Integrated Products, Inc.

**Covered by U.S. Patent numbers 4,636,930; 4,679,134; 4,777,577; 4,797,899; 4,809,152; 4,897,774; 4,999,761; and other patents pending.*

ABSOLUTE MAXIMUM RATINGS

V_{CC} ..... -0.3V to +6V
V+ (Note 1) ..... -0.3V to +7V
V- (Note 1) ..... +0.3V to -7V
V+ + V- (Note 1) ..... +13V
Input Voltages
T_IN, $\overline{SHDN}$, $\overline{EN}$ ..... -0.3V to +6V
MBAUD ..... -0.3V to (V_{CC} + 0.3V)
R_IN ..... ±25V
Output Voltages
T_OUT ..... ±13.2V
R_OUT ..... -0.3V to (V_{CC} + 0.3V)
Short-Circuit Duration
T_OUT ..... Continuous

Continuous Power Dissipation (T_A = +70°C)
16-Pin TSSOP (derate 6.7mW/°C above +70°C) 533mW
16-Pin Narrow SO (derate 8.70mW/°C above +70°C) 696mW
16-Pin Wide SO (derate 9.52mW/°C above +70°C) 762mW
16-Pin Plastic DIP (derate 10.53mW/°C above +70°C) 842mW
18-Pin SO (derate 9.52mW/°C above +70°C) 762mW
18-Pin Plastic DIP (derate 11.11mW/°C above +70°C) 889mW
20-Pin SSOP (derate 7.00mW/°C above +70°C) 559mW
20-Pin TSSOP (derate 8.0mW/°C above +70°C) 640mW
28-Pin TSSOP (derate 8.7mW/°C above +70°C) 696mW
28-Pin SSOP (derate 9.52mW/°C above +70°C) 762mW
28-Pin SO (derate 12.50mW/°C above +70°C) 1W
Operating Temperature Ranges
MAX32_ _C_ _ ..... 0°C to +70°C
MAX32_ _E_ _ ..... -40°C to +85°C
Storage Temperature Range ..... -65°C to +150°C
Lead Temperature (soldering, 10s) ..... +300°C

Note 1: V+ and V- can have a maximum magnitude of 7V, but their absolute difference cannot exceed 13V.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(V_{CC} = +3.0V to +5.5V, C1–C4 = 0.1µF (Note 2), T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at T_A = +25°C.)

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
DC CHARACTERISTICS						
V_{CC} Power-Supply Current	No load, V_{CC} = 3.3V or 5.0V, T_A = +25°C	MAX3222/MAX3232/ MAX3241		0.3	1.0	mA
		MAX3237		0.5	2.0	
Shutdown Supply Current	SHDN = GND, T_A = +25°C			1.0	10	µA
LOGIC INPUTS AND RECEIVER OUTPUTS						
Input Logic Threshold Low (Note 3)	T_IN, $\overline{EN}$, $\overline{SHDN}$, MBAUD				0.8	V
Input Logic Threshold High (Note 3)	V_{CC} = 3.3V		2.0			V
	V_{CC} = 5.0V		2.4			
Input Leakage Current	T_IN, $\overline{EN}$, $\overline{SHDN}$, MBAUD			±0.01	±1.0	µA
Output Leakage Current	Receivers disabled			±0.05	±10	µA
Output Voltage Low	I_{OUT} = 1.6mA				0.4	V
Output Voltage High	I_{OUT} = -1.0mA		V_{CC} - 0.6	V_{CC} - 0.1		V
RECEIVER INPUTS						
Input Voltage Range			-25		25	V
Input Threshold Low	T_A = +25°C	V_{CC} = 3.3V	0.6	1.2		V
		V_{CC} = 5.0V	0.8	1.5		
Input Threshold High	T_A = +25°C	V_{CC} = 3.3V		1.5	2.4	V
		V_{CC} = 5.0V		1.8	2.4	

ELECTRICAL CHARACTERISTICS (continued)

(V_{CC} = +3.0V to +5.5V, C1–C4 = 0.1µF (Note 2), T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at T_A = +25°C.)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Input Hysteresis			0.3		V
Input Resistance	T_A = +25°C	3	5	7	kΩ
TRANSMITTER OUTPUTS					
Output Voltage Swing	All transmitter outputs loaded with 3kΩ to ground	±5.0	±5.4		V
Output Resistance	V_{CC} = V+ = V- = 0V, T_{OUT} = ±2V	300	10M		Ω
Output Short-Circuit Current			±35	±60	mA
Output Leakage Current	V_{OUT} = ±12V, V_{CC} = 0V or 3V to 5.5V, transmitters disabled			±25	µA
MOUSE DRIVEABILITY (MAX3241)					
Transmitter Output Voltage	T1IN = T2IN = GND, T3IN = V_{CC}, T3OUT loaded with 3kΩ to GND, T1OUT and T2OUT loaded with 2.5mA each	±5.0			V

TIMING CHARACTERISTICS—MAX3222/MAX3232/MAX3241

(V_{CC} = +3.0V to +5.5V, C1–C4 = 0.1µF (Note 2), T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at T_A = +25°C.)

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Maximum Data Rate	R_L = 3kΩ, C_L = 1000pF, one transmitter switching		120	235		kbps
Receiver Propagation Delay	R_IN to R_OUT, C_L = 150pF	t_{PHL}		0.3		µs
		t_{PLH}		0.3		
Receiver Output Enable Time	Normal operation			200		ns
Receiver Output Disable Time	Normal operation			200		ns
Transmitter Skew	| t_{PHL} - t_{PLH} |			300		ns
Receiver Skew	| t_{PHL} - t_{PLH} |			300		ns
Transition-Region Slew Rate	V_{CC} = 3.3V, R_L = 3kΩ to 7kΩ, +3V to -3V or -3V to +3V, T_A = +25°C, one transmitter switching	C_L = 150pF to 1000pF	6		30	V/µs
		C_L = 150pF to 2500pF	4		30	

TIMING CHARACTERISTICS—MAX3237

(V_{CC} = +3.0V to +5.5V, C1–C4 = 0.1µF (Note 2), T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at T_A = +25°C.)

PARAMETER	CONDITIONS			MIN	TYP	MAX	UNITS
Maximum Data Rate	R_L = 3kΩ, C_L = 1000pF, one transmitter switching, MBAUD = GND			250			kbps
	V_{CC} = 3.0V to 4.5V, R_L = 3kΩ, C_L = 250pF, one transmitter switching, MBAUD = V_{CC}			1000			
	V_{CC} = 4.5V to 5.5V, R_L = 3kΩ, C_L = 1000pF, one transmitter switching, MBAUD = V_{CC}			1000			
Receiver Propagation Delay	R_IN to R_OUT, C_L = 150pF	t_{PHL}			0.15		µs
		t_{PLH}			0.15		
Receiver Output Enable Time	Normal operation				200		ns
Receiver Output Disable Time	Normal operation				200		ns
Transmitter Skew	| t_{PHL} - t_{PLH} |, MBAUD = GND				100		ns
	| t_{PHL} - t_{PLH} |, MBAUD = V_{CC}				25		ns
Receiver Skew	| t_{PHL} - t_{PLH} |				50		ns
Transition-Region Slew Rate	V_{CC} = 3.3V, R_L = 3Ω to 7kΩ, +3V to -3V or -3V to +3V, T_A = +25°C	C_L = 150pF to 1000pF	MBAUD = GND	6		30	V/µs
			MBAUD = V_{CC}	24		150	
		C_L = 150pF to 2500pF, MBAUD = GND		4		30	

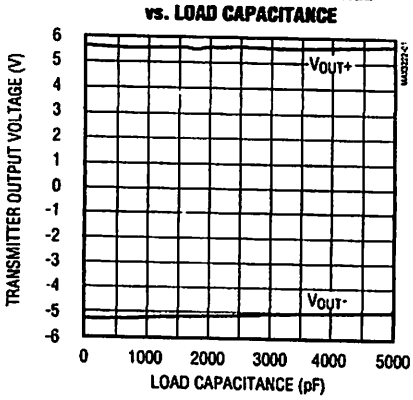
Note 2: MAX3222/MAX3232/MAX3241: C1–C4 = 0.1µF tested at 3.3V ±10%; C1 = 0.047µF, C2–C4 = 0.33µF tested at 5.0V ±10%. MAX3237: C1–C4 = 0.1µF tested at 3.3V ±5%; C1–C4 = 0.22µF tested at 3.3V ±10%; C1 = 0.047µF, C2–C4 = 0.33µF tested at 5.0V ±10%.

Note 3: Transmitter input hysteresis is typically 250mV.

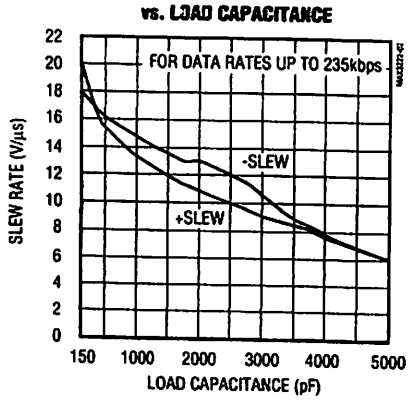
Typical Operating Characteristics

(V_{CC} = +3.3V, 235kbps data rate, 0.1µF capacitors, all transmitters loaded with 3kΩ, T_A = +25°C, unless otherwise noted.)

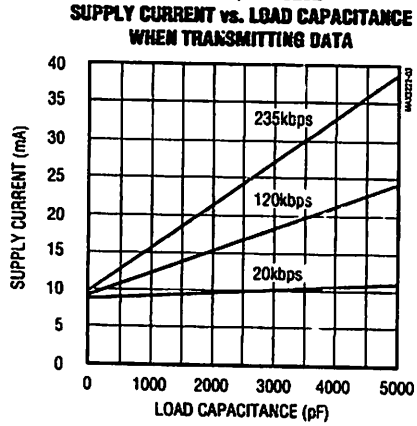
MAX3222/MAX3232 TRANSMITTER OUTPUT VOLTAGE vs. LOAD CAPACITANCE



MAX3222/MAX3232 SLEW RATE vs. LOAD CAPACITANCE



MAX3222/MAX3232 SUPPLY CURRENT vs. LOAD CAPACITANCE WHEN TRANSMITTING DATA

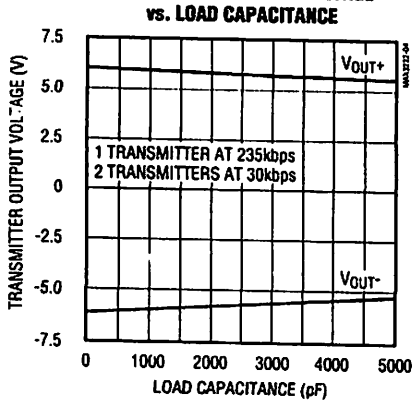


3.0V to 5.5V, Low-Power, up to 1Mbps, True RS-232 Transceivers Using Four 0.1µF External Capacitors

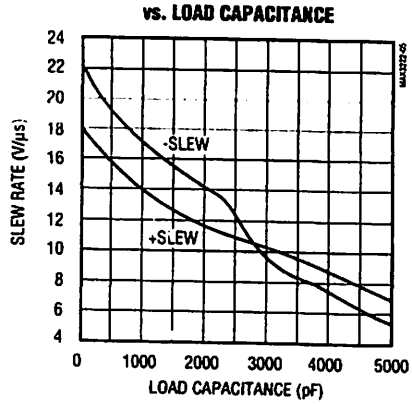
Typical Operating Characteristics (continued)

(VCC = +3.3V, 235kbps data rate, 0.1µF capacitors, all transmitters loaded with 3kΩ, TA = +25°C, unless otherwise noted.)

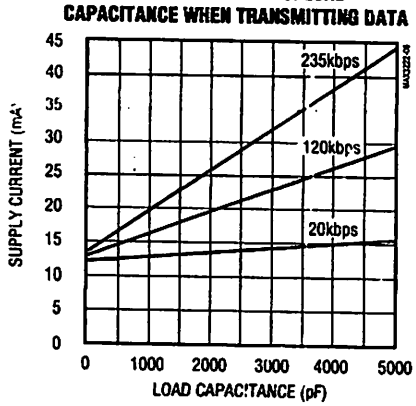
MAX3241
TRANSMITTER OUTPUT VOLTAGE vs. LOAD CAPACITANCE



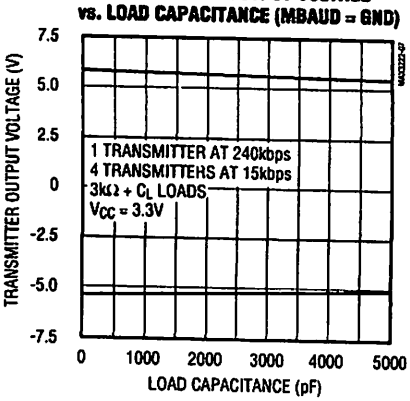
MAX3241
SLEW RATE vs. LOAD CAPACITANCE



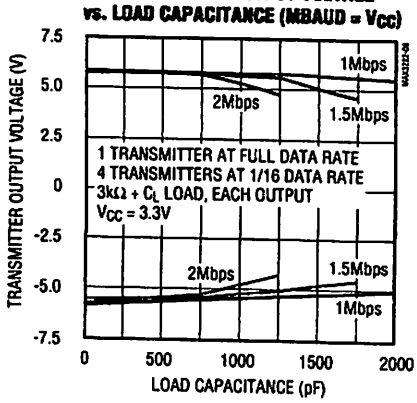
MAX3241
SUPPLY CURRENT vs. LOAD CAPACITANCE WHEN TRANSMITTING DATA



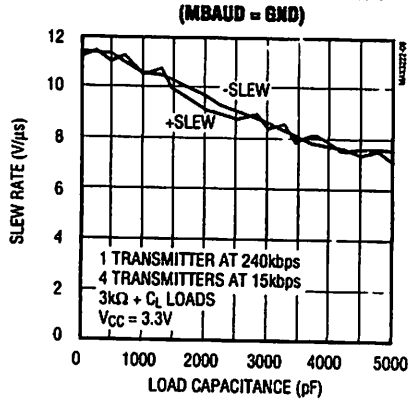
MAX3237
TRANSMITTER OUTPUT VOLTAGE vs. LOAD CAPACITANCE (MBAUD = GND)



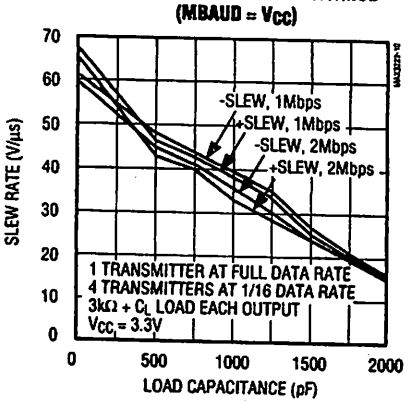
MAX3237
TRANSMITTER OUTPUT VOLTAGE vs. LOAD CAPACITANCE (MBAUD = VCC)



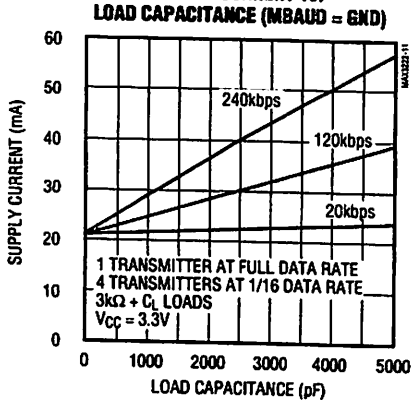
MAX3237
SLEW RATE vs. LOAD CAPACITANCE (MBAUD = GND)



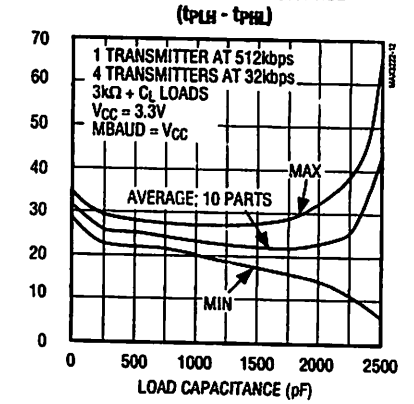
MAX3237
SLEW RATE vs. LOAD CAPACITANCE (MBAUD = VCC)



MAX3237
SUPPLY CURRENT vs. LOAD CAPACITANCE (MBAUD = GND)



MAX3237
SKEW vs. LOAD CAPACITANCE (t_{PLH} - t_{PHL})



Pin Description

PIN					NAME	FUNCTION
MAX3222		MAX3232	MAX3237	MAX3241		
DIP/SO	SSOP					
1	1	—	13	23	$\overline{EN}$	Receiver Enable. Active low.
2	2	1	28	28	C1+	Positive Terminal of Voltage-Doubler Charge-Pump Capacitor
3	3	2	27	27	V+	+5.5V Generated by the Charge Pump
4	4	3	25	24	C1-	Negative Terminal of Voltage-Doubler Charge-Pump Capacitor
5	5	4	1	1	C2+	Positive Terminal of Inverting Charge-Pump Capacitor
6	6	5	3	2	C2-	Negative Terminal of Inverting Charge-Pump Capacitor
7	7	6	4	3	V-	-5.5V Generated by the Charge Pump
8, 15	8, 17	7, 14	5, 6, 7, 10, 12	9, 10, 11	T_OUT	RS-232 Transmitter Outputs
9, 14	9, 16	8, 13	8, 9, 11	4–8	R_IN	RS-232 Receiver Inputs
10, 13	10, 15	9, 12	18, 20, 21	15–19	R_OUT	TTL/CMOS Receiver Outputs
11, 12	12, 13	10, 11	17, 19, 22, 23, 24	12, 13, 14	T_IN	TTL/CMOS Transmitter Inputs
16	18	15	2	25	GND	Ground
17	19	16	26	26	V_{CC}	+3.0V to +5.5V Supply Voltage
18	20	—	14	22	$\overline{SHDN}$	Shutdown Control. Active low.
—	11, 14	—	—	—	N.C.	No Connection
—	—	—	15	—	MBAUD	MegaBaud Control Input. Connect to GND for normal operation; connect to V_{CC} for 1Mbps transmission rates.
—	—	—	16	20, 21	R_OUTB	Noninverting Complementary Receiver Outputs. Always active.

3.0V to 5.5V, Low-Power, up to 1Mbps, True RS-232 Transceivers Using Four 0.1µF External Capacitors

Detailed Description

Dual Charge-Pump Voltage Converter

The MAX3222/MAX3232/MAX3237/MAX3241's internal power supply consists of a regulated dual charge pump that provides output voltages of +5.5V (doubling charge pump) and -5.5V (inverting charge pump), regardless of the input voltage (VCC) over the 3.0V to 5.5V range. The charge pumps operate in a discontinuous mode; if the output voltages are less than 5.5V, the charge pumps are enabled, and if the output voltages exceed 5.5V, the charge pumps are disabled. Each charge pump requires a flying capacitor (C1, C2) and a reservoir capacitor (C3, C4) to generate the V+ and V- supplies.

RS-232 Transmitters

The transmitters are inverting level translators that convert CMOS-logic levels to 5.0V EIA/TIA-232 levels.

The MAX3222/MAX3232/MAX3241 transmitters guarantee a 120kbps data rate with worst-case loads of 3kΩ in parallel with 1000pF, providing compatibility with PC-to-PC communication software (such as LapLink™). Typically, these three devices can operate at data rates of 235kbps. Transmitters can be paralleled to drive multiple receivers or mice.

The MAX3222/MAX3237/MAX3241's output stage is turned off (high impedance) when the device is in shutdown mode. When the power is off, the MAX3222/MAX3232/MAX3237/MAX3241 permit the outputs to be driven up to ±12V.

The transmitter inputs do not have pullup resistors. Connect unused inputs to GND or VCC.

MAX3237 MegaBaud Operation

In normal operating mode (MBAUD = GND), the MAX3237 transmitters guarantee a 250kbps data rate with worst-case loads of 3kΩ in parallel with 1000pF. This provides compatibility with PC-to-PC communication software, such as Laplink.

For higher speed serial communications, the MAX3237 features MegaBaud operation. In MegaBaud operating mode (MBAUD = VCC), the MAX3237 transmitters guarantee a 1Mbps data rate with worst-case loads of 3kΩ in parallel with 250pF for 3.0V < VCC < 4.5V. For 5V ±10% operation, the MAX3237 transmitters guarantee a 1Mbps data rate into worst-case loads of 3kΩ in parallel with 1000pF.

LapLink is a trademark of Traveling Software, Inc.

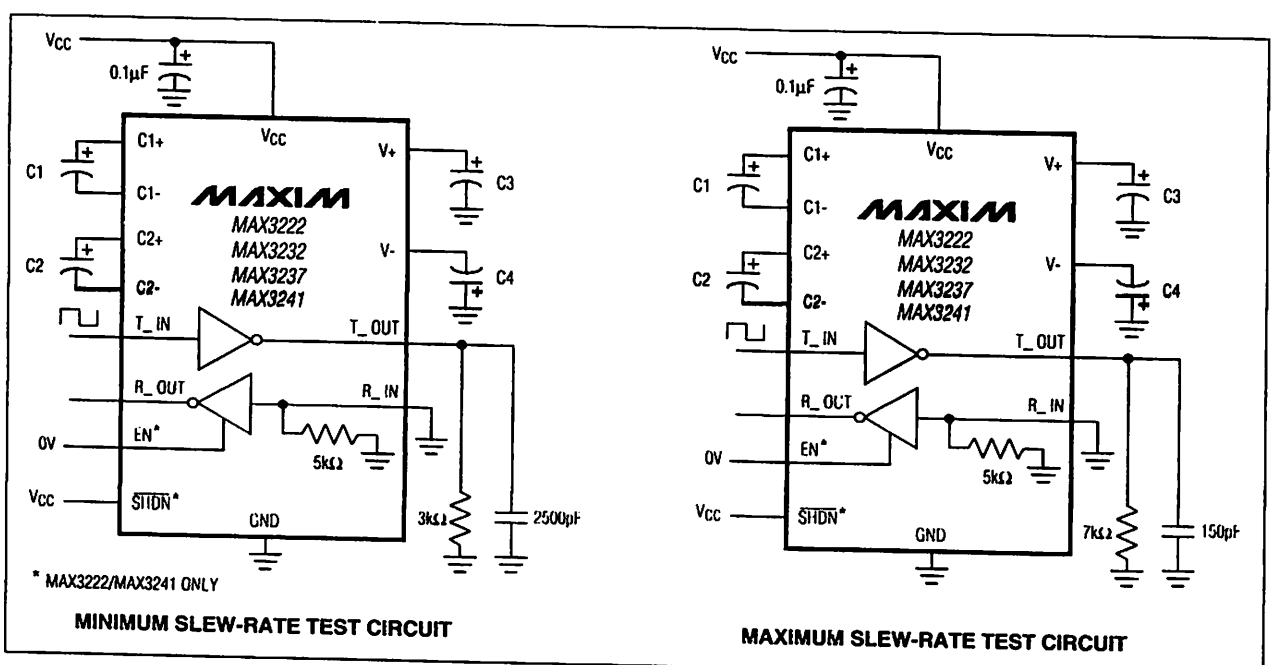
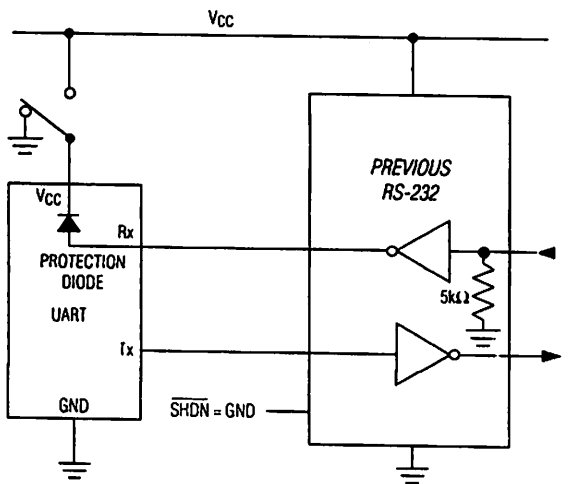
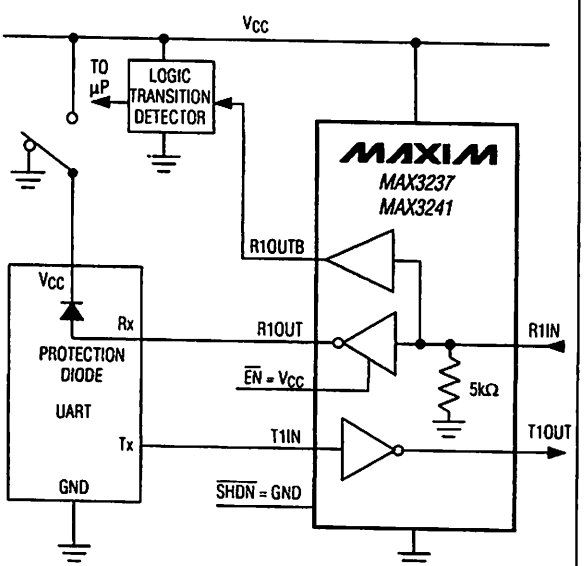


Figure 1. Slew-Rate Test Circuits



a) OLDER RS-232: POWERED-DOWN UART DRAWS CURRENT FROM ACTIVE RECEIVER OUTPUT IN SHUTDOWN.



b) NEW MAX3237/MAX3241: $\overline{EN}$ SHUTS DOWN RECEIVER OUTPUTS (EXCEPT FOR B OUTPUTS), SO NO CURRENT FLOWS TO UART IN SHUTDOWN. B OUTPUTS INDICATE RECEIVER ACTIVITY DURING SHUTDOWN WITH $\overline{EN}$ HIGH.

Figure 2. Detection of RS-232 Activity when the UART and Interface are Shut Down; Comparison of MAX3237/MAX3241 (b) with Previous Transceivers (a).

RS-232 Receivers

The receivers convert RS-232 signals to CMOS-logic output levels. The MAX3222/MAX3237/MAX3241 receivers have inverting three-state outputs. In shutdown, the receivers can be active or inactive (Table 1).

The complementary outputs on the MAX3237 (R1OUTB) and the MAX3241 (R1OUTB, R2OUTB) are always active, regardless of the state of $\overline{EN}$ or $\overline{SHDN}$. This allows for Ring Indicator applications without forward biasing other devices connected to the receiver outputs. This is ideal for systems where VCC is set to 0V in shutdown to accommodate peripherals, such as UARTs (Figure 2).

MAX3222/MAX3237/MAX3241 Shutdown Mode

Supply current falls to less than 1µA in shutdown mode ($\overline{SHDN}$ = low). When shut down, the device's charge pumps are turned off, V+ is pulled down to VCC, V- is pulled to ground, and the transmitter outputs are disabled (high impedance). The time required to exit shutdown is typically 100µs, as shown in Figure 3. Connect $\overline{SHDN}$ to VCC if the shutdown mode is not used. $\overline{SHDN}$ has no effect on R_OUT or R_OUTB.

MAX3222/MAX3237/MAX3241 Enable Control

The inverting receiver outputs (R_OUT) are put into a high-impedance state when $\overline{EN}$ is high. The complementary outputs R1OUTB and R2OUTB are always active, regardless of the state of $\overline{EN}$ and $\overline{SHDN}$ (Table 1). $\overline{EN}$ has no effect on T_OUT.

Applications Information

Capacitor Selection

The capacitor type used for C1–C4 is not critical for proper operation; polarized or nonpolarized capacitors can be used. The charge pump requires 0.1µF capacitors for 3.3V operation. For other supply voltages, refer to Table 2 for required capacitor values. Do not use values lower than those listed in Table 2. Increasing the capacitor values (e.g., by a factor of 2) reduces ripple on the transmitter outputs and slightly reduces power consumption. C2, C3, and C4 can be increased without changing C1's value. However, do not increase C1 without also increasing the values of C2, C3, and C4, to maintain the proper ratios (C1 to the other capacitors).

When using the minimum required capacitor values, make sure the capacitor value does not degrade excessively with temperature. If in doubt, use capacitors with a higher nominal value. The capacitor's equivalent series resistance (ESR), which usually rises at low temperatures, influences the amount of ripple on V+ and V-.

Table 1. MAX3222/MAX3237/MAX3241 Shutdown and Enable Control Truth Table

SHDN	EN	T_OUT	R_OUT	R_OUTB (MAX3237/ MAX3241)
0	0	High-Z	Active	Active
0	1	High-Z	High-Z	Active
1	0	Active	Active	Active
1	1	Active	High-Z	Active

Table 2. Required Minimum Capacitor Values

Vcc (V)	C1 (µF)	C2, C3, C4 (µF)
MAX3222/MAX3232/MAX3241		
3.0 to 3.6	0.1	0.1
4.5 to 5.5	0.047	0.33
3.0 to 5.5	0.1	0.47
MAX3237		
3.0 to 3.6	0.22	0.22
3.15 to 3.6	0.1	0.1
4.5 to 5.5	0.047	0.33
3.0 to 5.5	0.22	1.0

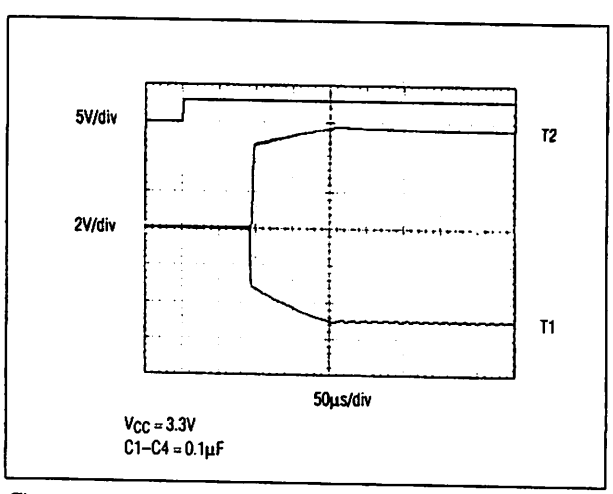


Figure 3. Transmitter Outputs when Exiting Shutdown or Powering Up

Power-Supply Decoupling

In most circumstances, a 0.1µF bypass capacitor is adequate. In applications that are sensitive to power-supply noise, decouple VCC to ground with a capacitor of the same value as charge-pump capacitor C1. Connect bypass capacitors as close to the IC as possible.

Operation Down to 2.7V

Transmitter outputs will meet EIA/TIA-562 levels of ±3.7V with supply voltages as low as 2.7V

Transmitter Outputs when Exiting Shutdown

Figure 3 shows two transmitter outputs when exiting shutdown mode. As they become active, the two transmitter outputs are shown going to opposite RS-232 levels (one transmitter input is high, the other is low). Each transmitter is loaded with 3kΩ in parallel with 2500pF. The transmitter outputs display no ringing or undesirable transients as they come out of shutdown. Note that the transmitters are enabled only when the magnitude of V- exceeds approximately 3V.

Mouse Driveability

The MAX3241 has been specifically designed to power serial mice while operating from low-voltage power supplies. It has been tested with leading mouse brands from manufacturers such as Microsoft and Logitech. The MAX3241 successfully drove all serial mice tested and met their respective current and voltage requirements. Figure 4a shows the transmitter output voltages under increasing load current at 3.0V. Figure 4b shows a typical mouse connection using the MAX3241.

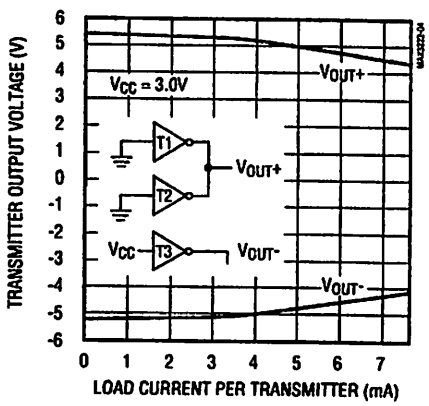


Figure 4a. MAX3241 Transmitter Output Voltage vs. Load Current per Transmitter

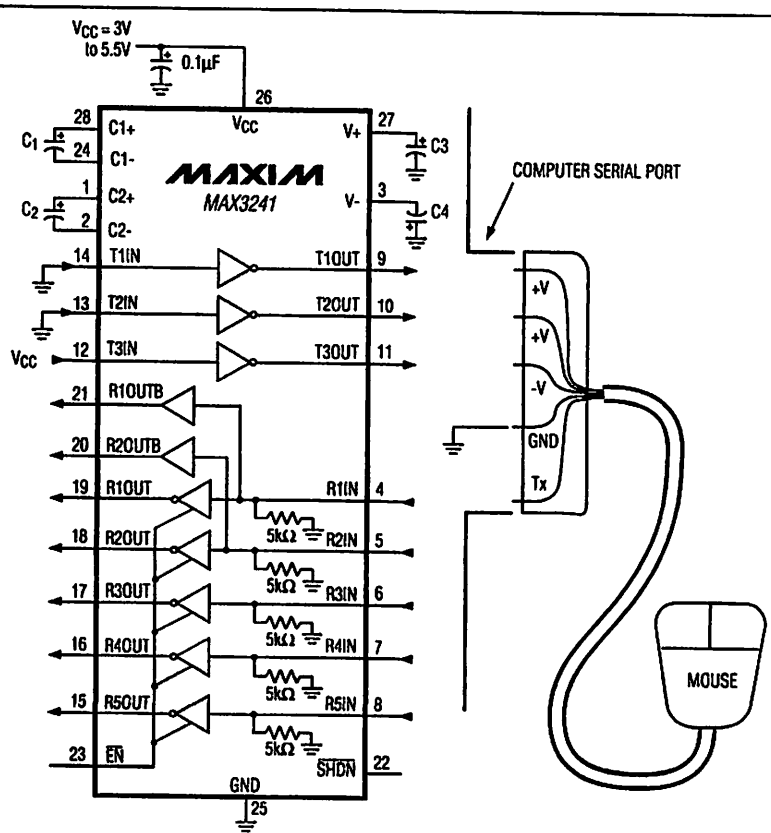


Figure 4b. Mouse Driver Test Circuit

3.0V to 5.5V, Low-Power, up to 1Mbps, True RS-232 Transceivers Using Four 0.1µF External Capacitors

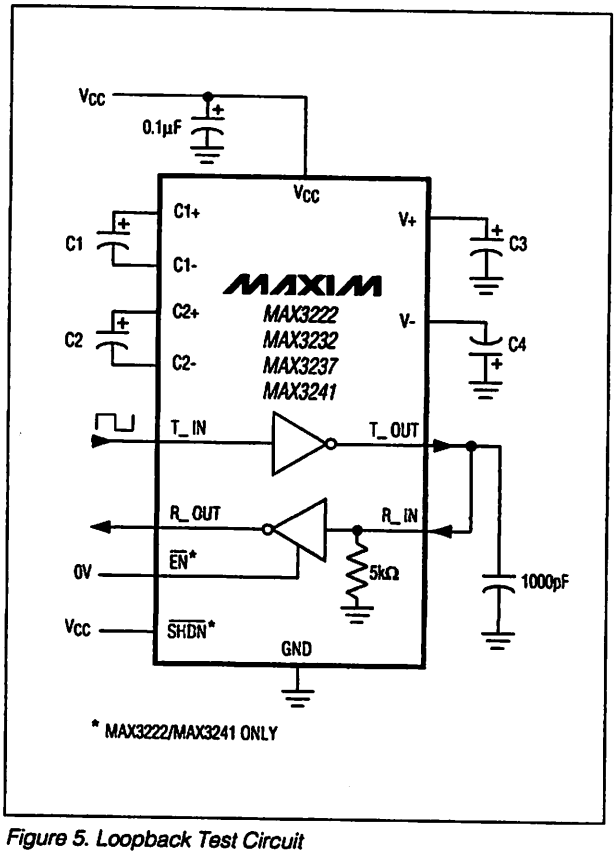


Figure 5. Loopback Test Circuit

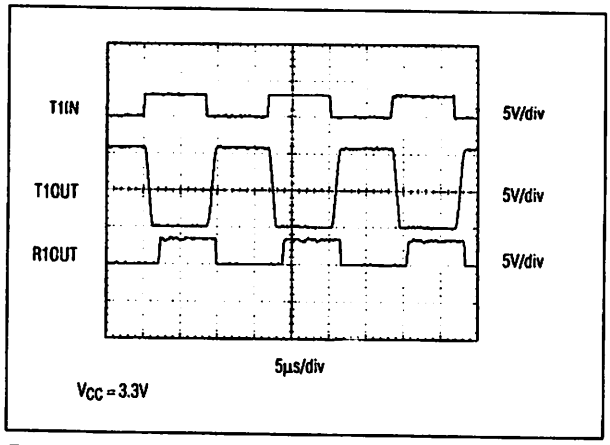


Figure 6. MAX3241 Loopback Test Result at 120kbps

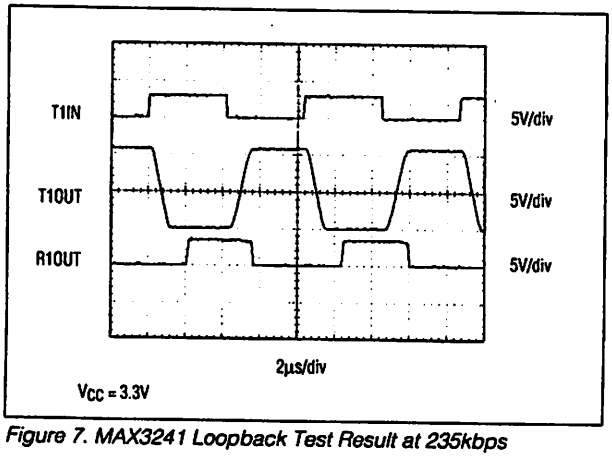


Figure 7. MAX3241 Loopback Test Result at 235kbps

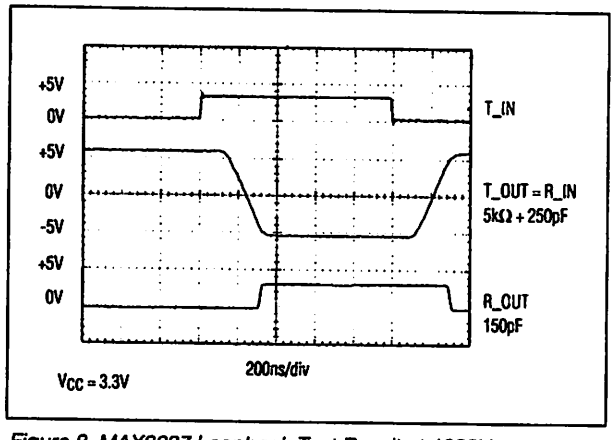


Figure 8. MAX3237 Loopback Test Result at 1000kbps (MBAUD = VCC)

High Data Rates

The MAX3222/MAX3232/MAX3241 maintain the RS-232 ±5.0V minimum transmitter output voltage even at high data rates. Figure 5 shows a transmitter loopback test circuit. Figure 6 shows a loopback test result at 120kbps, and Figure 7 shows the same test at 235kbps. For Figure 6, all transmitters were driven simultaneously at 120kbps into RS-232 loads in parallel with 1000pF. For Figure 7, a single transmitter was driven at 235kbps, and all transmitters were loaded with an RS-232 receiver in parallel with 1000pF.

The MAX3237 maintains the RS-232 ±5.0V minimum transmitter output voltage at data rates up to 1Mbps. Figure 8 shows a loopback test result at 1Mbps with MBAUD = VCC. For Figure 8, all transmitters were loaded with an RS-232 receiver in parallel with 250pF.

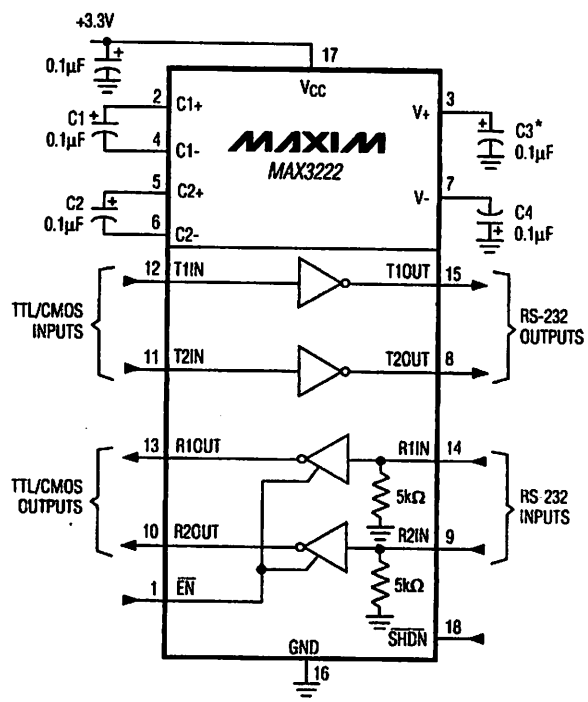
Interconnection with 3V and 5V Logic

The MAX3222/MAX3232/MAX3237/MAX3241 can directly interface with various 5V logic families, including ACT and HCT CMOS. See Table 3 for more information on possible combinations of interconnections.

Table 3. Logic-Family Compatibility with Various Supply Voltages

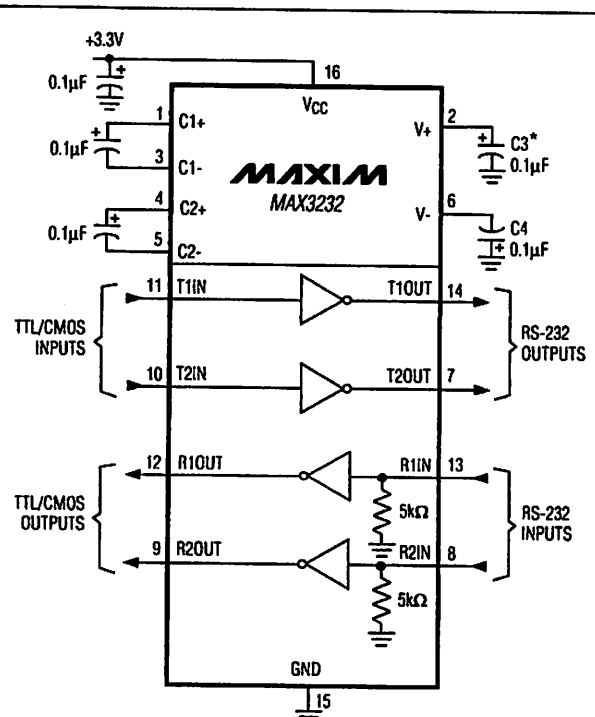
SYSTEM POWER-SUPPLY VOLTAGE (V)	MAX32__ VCC SUPPLY VOLTAGE (V)	COMPATIBILITY
3.3	3.3	Compatible with all CMOS families.
5	5	Compatible with all TTL and CMOS-logic families.
5	3.3	Compatible with ACT and HCT CMOS, and with TTL. Incompatible with AC, HC, and CD4000 CMOS.

Typical Operating Circuits



PIN NUMBERS REFER TO DIP/SO PACKAGES.

* C3 CAN BE RETURNED TO EITHER VCC OR GROUND.

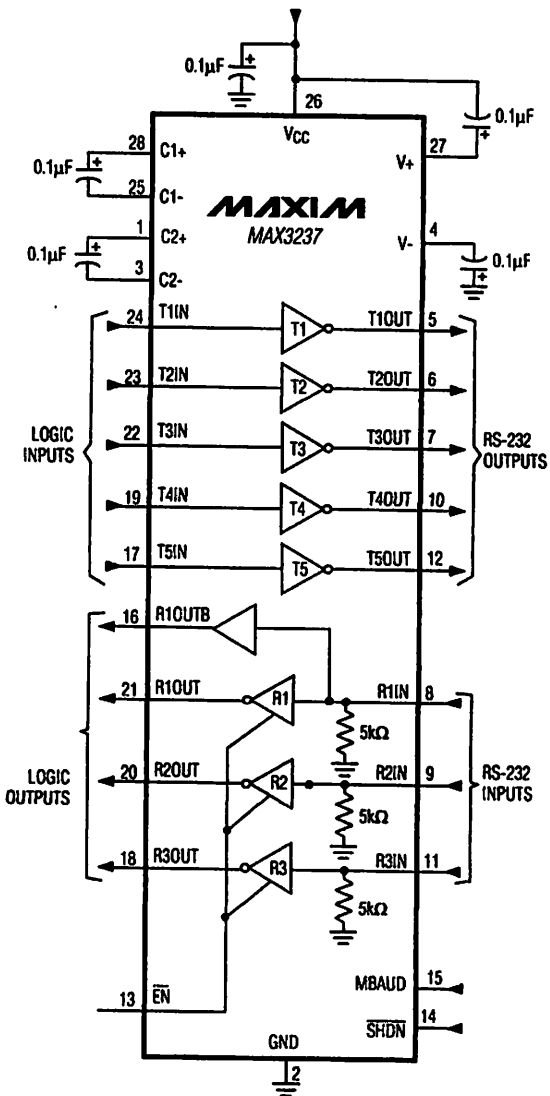


* C3 CAN BE RETURNED TO EITHER VCC OR GROUND.

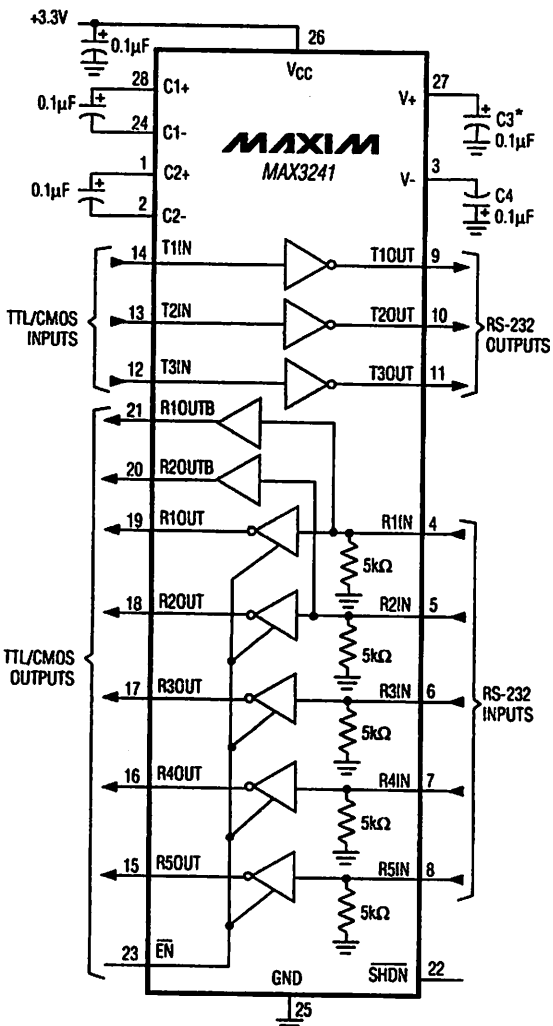
SEE TABLE 2 FOR CAPACITOR SELECTION

3.0V to 5.5V, Low-Power, up to 1Mbps, True RS-232 Transceivers Using Four 0.1µF External Capacitors

Typical Operating Circuits (continued)



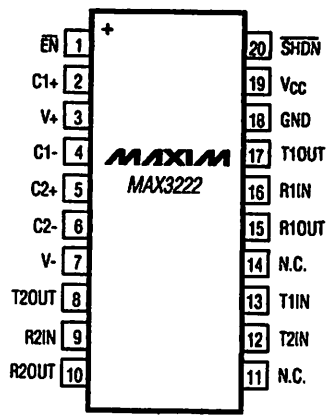
* C3 CAN BE RETURNED TO EITHER V_{CC} OR GROUND.



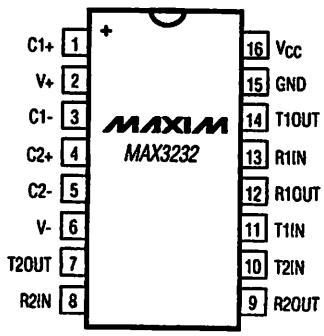
* C3 CAN BE RETURNED TO EITHER V_{CC} OR GROUND.

Pin Configurations (continued)

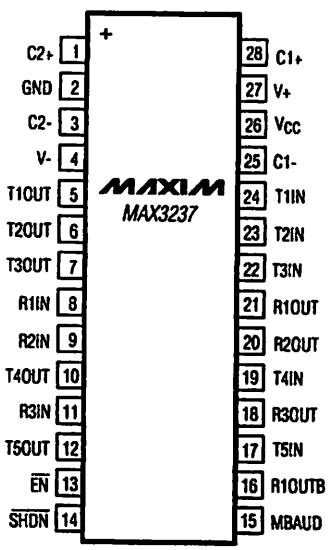
TOP VIEW



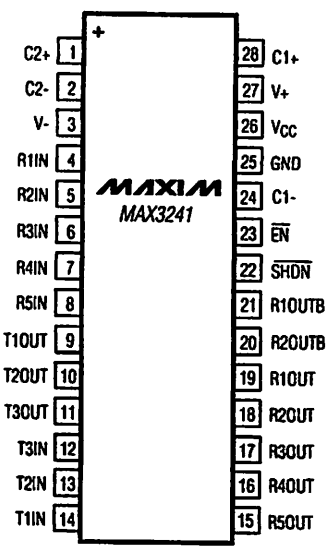
SSOP/TSSOP



DIP/SO/TSSOP



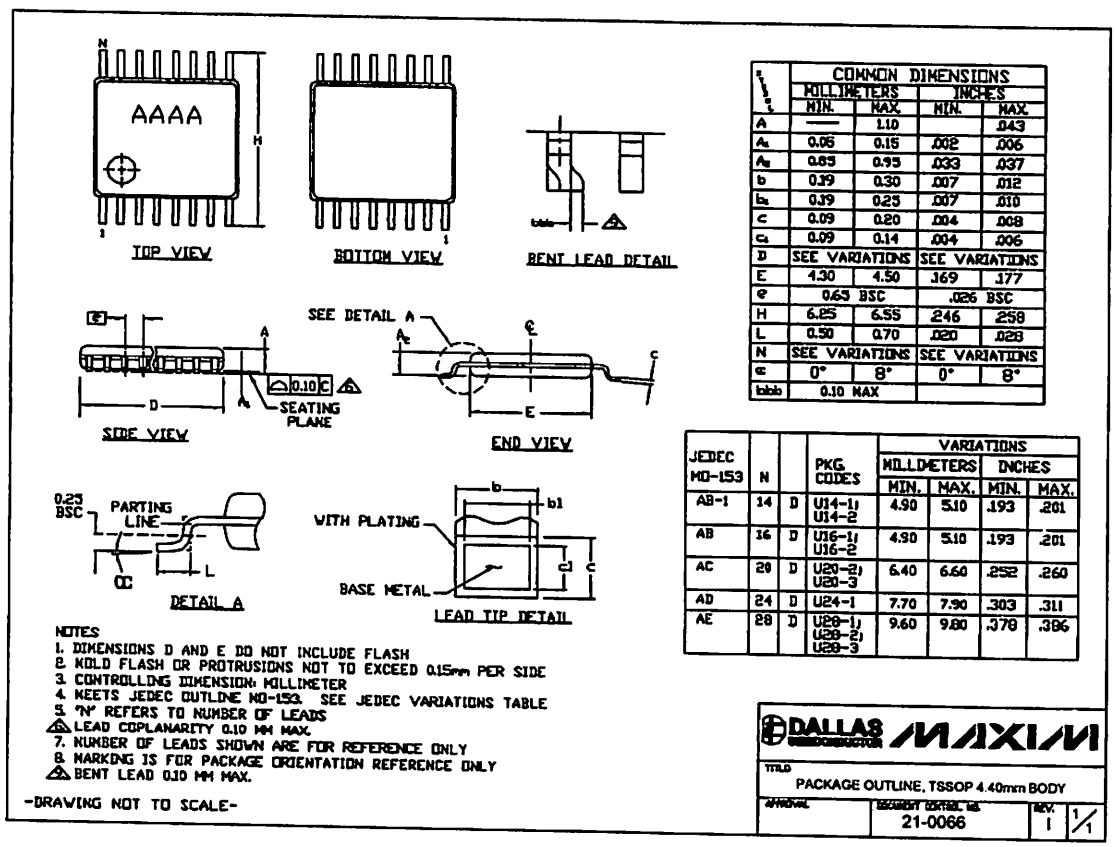
SSOP



SO/SSOP/TSSOP

Package Information

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information, go to www.maxim-ic.com/packages.)

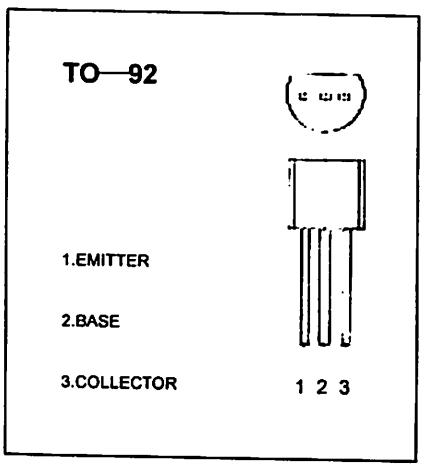


SYMBOL	COMMON DIMENSIONS			
	MILLIMETERS		INCHES	
	MIN.	MAX.	MIN.	MAX.
A	——	1.10		.043
A_1	0.05	0.15	.002	.006
A_2	0.85	0.95	.033	.037
b	0.19	0.30	.007	.012
b_1	0.19	0.25	.007	.010
c	0.09	0.20	.004	.008
c_1	0.09	0.14	.004	.006
D	SEE VARIATIONS		SEE VARIATIONS	
E	4.30	4.50	.169	.177
e	0.65 BSC		.026 BSC	
H	6.25	6.55	.246	.258
L	0.50	0.70	.020	.028
N	SEE VARIATIONS		SEE VARIATIONS	
α	0°	8°	0°	8°
bbb	0.10 MAX			

JEDEC MO-153	N		PKG. CODES	VARIATIONS			
				MILLIMETERS		INCHES	
				MIN.	MAX.	MIN.	MAX.
AB-1	14	D	U14-1, U14-2	4.90	5.10	.193	.201
AB	16	D	U16-1, U16-2	4.90	5.10	.193	.201
AC	20	D	U20-2, U20-3	6.40	6.60	.252	.260
AD	24	D	U24-1	7.70	7.90	.303	.311
AE	28	D	U28-1, U28-2, U28-3	9.60	9.80	.378	.386

Revision History

Pages changed at Rev 7: 1, 15, 16, 17



FEATURES

Power dissipation

P_{CM} : 0.4 W (Tamb=25℃)

Collector current

I_{CM} : 0.1 A

Collector-base voltage

$V_{(BR)CBO}$: 50 V

ELECTRICAL CHARACTERISTICS (Tamb=25℃ unless otherwise specified)

Parameter	Symbol	Test conditions	MIN	TYP	MAX	UNIT
Collector-base breakdown voltage	$V(BR)_{CBO}$	Ic= 100 μA, I_E=0	50			V
Collector-emitter breakdown voltage	$V(BR)_{CEO}$	Ic= 0. 1 mA, I_B=0	45			V
Emitter-base breakdown voltage	$V(BR)_{EBO}$	I_E= 100 μA, I_C=0	5			V
Collector cut-off current	I_{CBO}	V_{CB}=50 V, I_E=0			0.1	μA
Collector cut-off current	I_{CEO}	V_{CE}=35 V, I_B=0			0.1	μA
Emitter cut-off current	I_{EBO}	V_{EB}= 3 V, I_C=0			0.1	μA
DC current gain(note)	$H_{FE\ (1)}$	V_{CE}= 5 V, I_C= 1mA	60		1000	
Collector-emitter saturation voltage	V_{CE}(sat)	I_C= 100mA, I_B= 5 mA			0.3	V
Base-emitter saturation voltage	V_{BE}(sat)	I_C= 100 mA, I_B= 5mA			1	V
Transition frequency	f_T	V_{CE}= 5 V, I_C= 10mA f =30MHz	150			MHz

CLASSIFICATION OF $H_{FE(1)}$

Rank	A	B	C	D
Range	60-150	100-300	200-600	400-1000

Wing Shing Computer Components Co., (H.K.)Ltd.
Homepage: http://www.wingshing.com
Tel:(852)2341 9276 Fax:(852)2797 8153
E-mail: wsccltd@hkstar.com

MOTOROLA
SEMICONDUCTOR TECHNICAL DATA

Order this document
by 4N35/D

GlobalOptoisolator™

VDE | UL | CSA | SETI | SEMKO | DEMKO | NEMKO | BABT

6-Pin DIP Optoisolators Transistor Output

4N35*
4N36
4N37
[CTR = 100% Min]

*Motorola Preferred Device

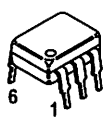
The 4N35, 4N36 and 4N37 devices consist of a gallium arsenide infrared emitting diode optically coupled to a monolithic silicon phototransistor detector.

- Current Transfer Ratio — 100% Minimum @ Specified Conditions
- Guaranteed Switching Speeds
- Meets or Exceeds all JEDEC Registered Specifications
- ***To order devices that are tested and marked per VDE 0884 requirements, the suffix "V" must be included at end of part number. VDE 0884 is a test option.***

Applications

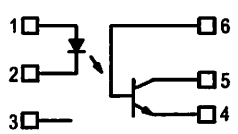
- General Purpose Switching Circuits
- Interfacing and coupling systems of different potentials and impedances
- Regulation Feedback Circuits
- Monitor & Detection Circuits
- Solid State Relays

STYLE 1 PLASTIC



STANDARD THRU HOLE
CASE 730A–04

SCHEMATIC



PIN 1. LED ANODE
2. LED CATHODE
3. N.C.
4. EMITTER
5. COLLECTOR
6. BASE

MAXIMUM RATINGS (T_A = 25°C unless otherwise noted)

Rating	Symbol	Value	Unit
INPUT LED			
Reverse Voltage	V_R	6	Volts
Forward Current — Continuous	I_F	60	mA
LED Power Dissipation @ T_A = 25°C with Negligible Power in Output Detector	P_D	120	mW
Derate above 25°C		1.41	mW/°C
OUTPUT TRANSISTOR			
Collector–Emitter Voltage	V_{CEO}	30	Volts
Emitter–Base Voltage	V_{EBO}	7	Volts
Collector–Base Voltage	V_{CBO}	70	Volts
Collector Current — Continuous	I_C	150	mA
Detector Power Dissipation @ T_A = 25°C with Negligible Power in Input LED	P_D	150	mW
Derate above 25°C		1.76	mW/°C
TOTAL DEVICE			
Isolation Source Voltage(1) (Peak ac Voltage, 60 Hz, 1 sec Duration)	V_{ISO}	7500	Vac(pk)
Total Device Power Dissipation @ T_A = 25°C	P_D	250	mW
Derate above 25°C		2.94	mW/°C
Ambient Operating Temperature Range(2)	T_A	−55 to +100	°C
Storage Temperature Range(2)	T_{stg}	−55 to +150	°C
Soldering Temperature (10 sec, 1/16" from case)	T_L	260	°C

1. Isolation surge voltage is an internal device dielectric breakdown rating. For this test, Pins 1 and 2 are common, and Pins 4, 5 and 6 are common.
2. Refer to Quality and Reliability Section in Opto Data Book for information on test conditions.

Preferred devices are Motorola recommended choices for future use and best overall value.

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MOTOROLA

ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise noted)(1)

Characteristic		Symbol	Min	Typ(1)	Max	Unit
INPUT LED						
Forward Voltage (I_F = 10 mA)	T_A = 25°C T_A = –55°C T_A = 100°C	V_F	0.8 0.9 0.7	1.15 1.3 1.05	1.5 1.7 1.4	V
Reverse Leakage Current (V_R = 6 V)		I_R	—	—	10	µA
Capacitance (V = 0 V, f = 1 MHz)		C_J	—	18	—	pF
OUTPUT TRANSISTOR						
Collector–Emitter Dark Current (V_{CE} = 10 V, T_A = 25°C) (V_{CE} = 30 V, T_A = 100°C)		I_{CEO}	— —	1 —	50 500	nA µA
Collector–Base Dark Current (V_{CB} = 10 V)	T_A = 25°C T_A = 100°C	I_{CBO}	—	0.2 100	20 —	nA
Collector–Emitter Breakdown Voltage (I_C = 1 mA)		$V_{(BR)CEO}$	30	45	—	V
Collector–Base Breakdown Voltage (I_C = 100 µA)		$V_{(BR)CBO}$	70	100	—	V
Emitter–Base Breakdown Voltage (I_E = 100 µA)		$V_{(BR)EBO}$	7	7.8	—	V
DC Current Gain (I_C = 2 mA, V_{CE} = 5 V)		h_{FE}	—	400	—	—
Collector–Emitter Capacitance (f = 1 MHz, V_{CE} = 0)		C_{CE}	—	7	—	pF
Collector–Base Capacitance (f = 1 MHz, V_{CB} = 0)		C_{CB}	—	19	—	pF
Emitter–Base Capacitance (f = 1 MHz, V_{EB} = 0)		C_{EB}	—	9	—	pF
COUPLED						
Output Collector Current (I_F = 10 mA, V_{CE} = 10 V)	T_A = 25°C T_A = –55°C T_A = 100°C	I_C (CTR)(2)	10 (100) 4 (40) 4 (40)	30 (300) — —	— — —	mA (%)
Collector–Emitter Saturation Voltage (I_C = 0.5 mA, I_F = 10 mA)		$V_{CE(sat)}$	—	0.14	0.3	V
Turn–On Time	(I_C = 2 mA, V_{CC} = 10 V, R_L = 100 Ω)(3)	t_{on}	—	7.5	10	µs
Turn–Off Time		t_{off}	—	5.7	10	
Rise Time		t_r	—	3.2	—	
Fall Time		t_f	—	4.7	—	
Isolation Voltage (f = 60 Hz, t = 1 sec)		V_{ISO}	7500	—	—	Vac(pk)
Isolation Current(4) ($V_{I–O}$ = 3550 Vpk) ($V_{I–O}$ = 2500 Vpk) ($V_{I–O}$ = 1500 Vpk)	4N35 4N36 4N37	I_{ISO}	— — —	— — 8	100 100 100	µA
Isolation Resistance (V = 500 V)(4)		R_{ISO}	10^{11}	—	—	Ω
Isolation Capacitance (V = 0 V, f = 1 MHz)(4)		C_{ISO}	—	0.2	2	pF

1. Always design to the specified minimum/maximum electrical limits (where applicable).
2. Current Transfer Ratio (CTR) = I_C/I_F x 100%.
3. For test circuit setup and waveforms, refer to Figure 11.
4. For this test, Pins 1 and 2 are common, and Pins 4, 5 and 6 are common.

TYPICAL CHARACTERISTICS

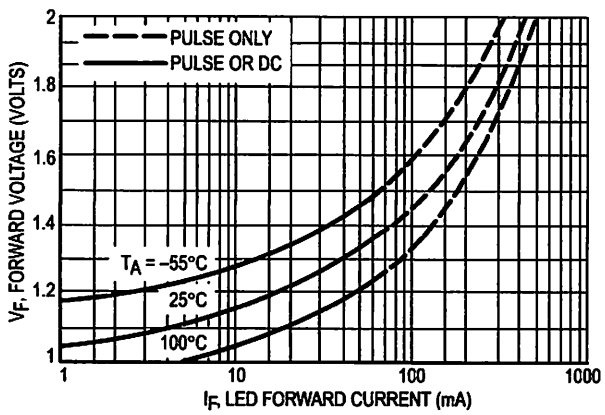


Figure 1. LED Forward Voltage versus Forward Current

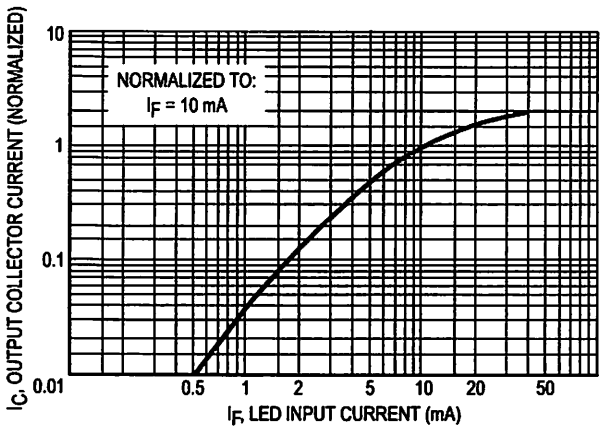


Figure 2. Output Current versus Input Current

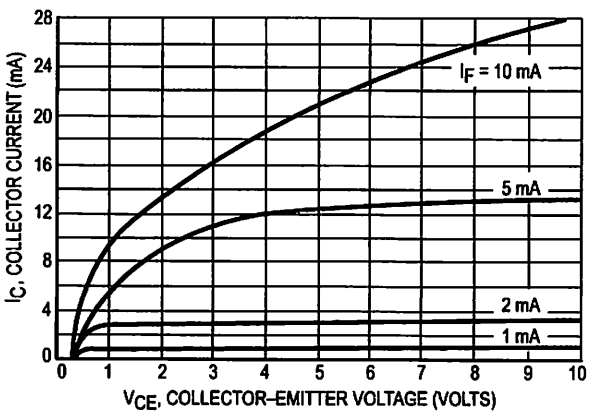


Figure 3. Collector Current versus Collector–Emitter Voltage

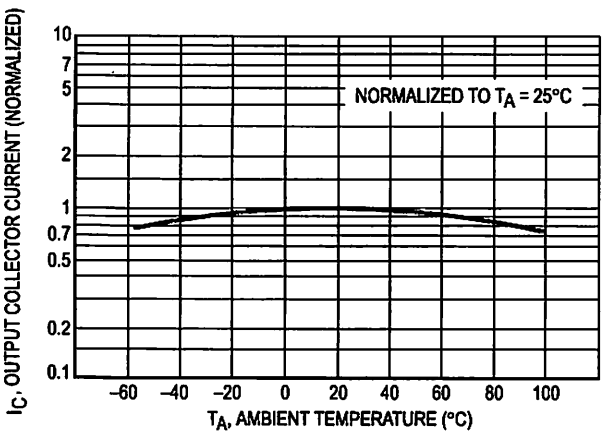


Figure 4. Output Current versus Ambient Temperature

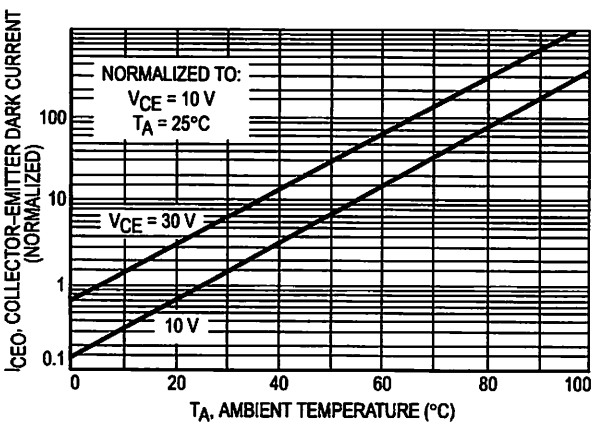


Figure 5. Dark Current versus Ambient Temperature

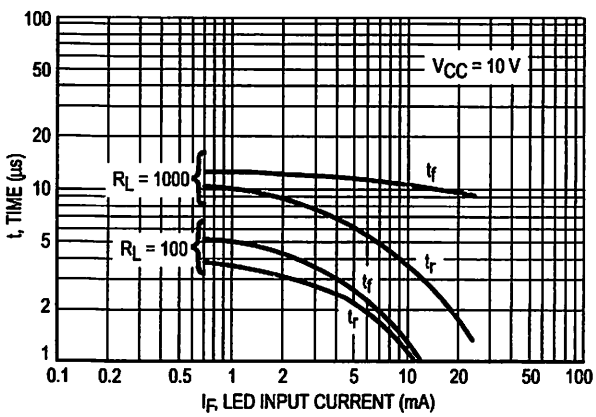


Figure 6. Rise and Fall Times (Typical Values)

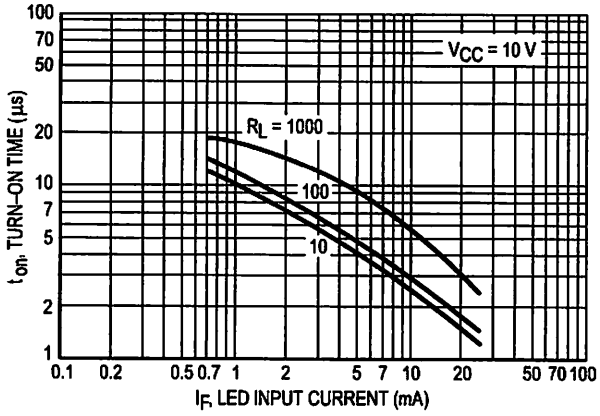


Figure 7. Turn–On Switching Times

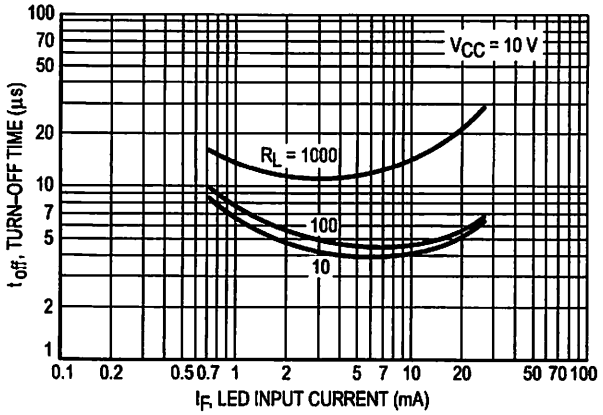


Figure 8. Turn–Off Switching Times

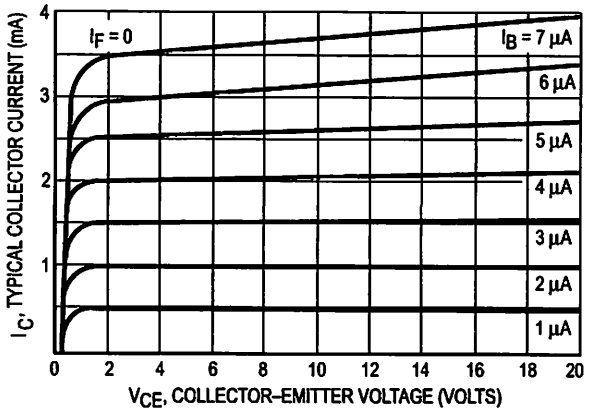


Figure 9. DC Current Gain (Detector Only)

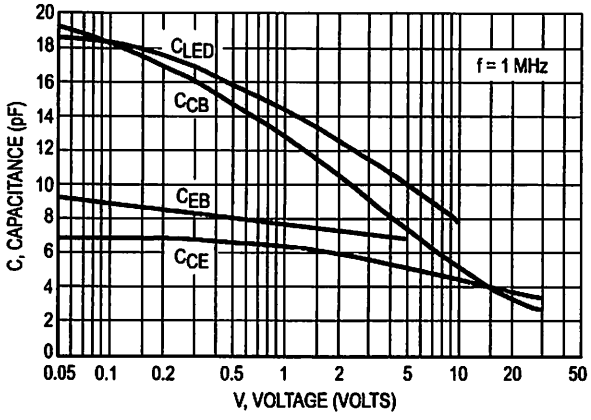


Figure 10. Capacitances versus Voltage

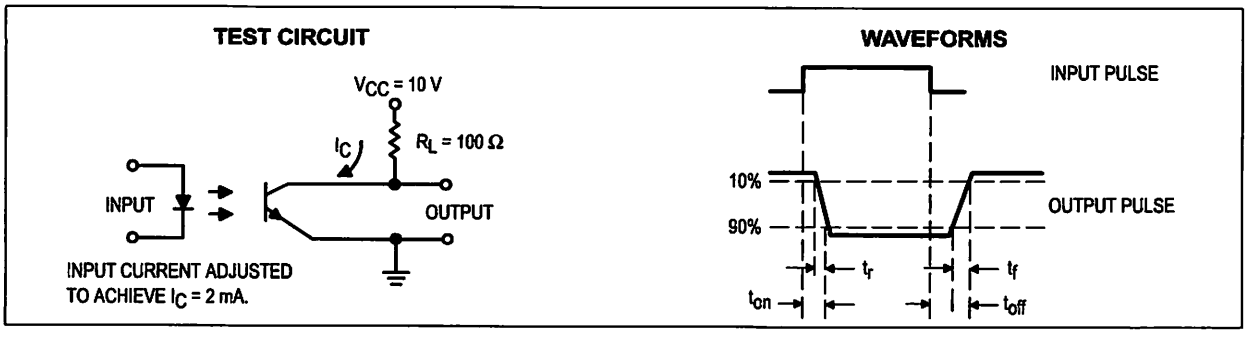
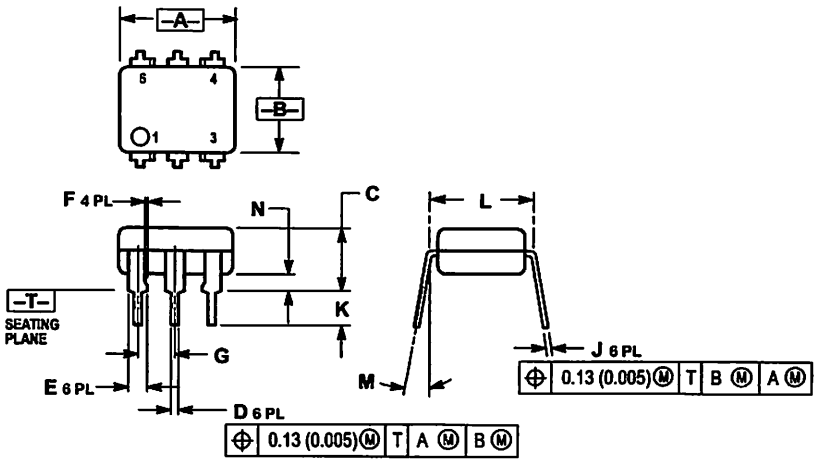


Figure 11. Switching Time Test Circuit and Waveforms

PACKAGE DIMENSIONS

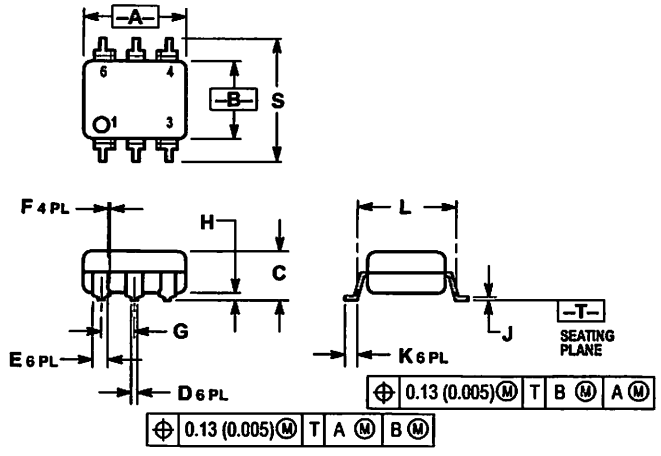


NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. DIMENSION L TO CENTER OF LEAD WHEN FORMED PARALLEL.

	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	0.320	0.350	8.13	8.89
B	0.240	0.260	6.10	6.60
C	0.115	0.200	2.93	5.08
D	0.016	0.020	0.41	0.50
E	0.040	0.070	1.02	1.77
F	0.010	0.014	0.25	0.36
G	0.100 BSC		2.54 BSC	
J	0.008	0.012	0.21	0.30
K	0.100	0.150	2.54	3.81
L	0.300 BSC		7.62 BSC	
M	0°	15°	0°	15°
N	0.015	0.100	0.38	2.54

STYLE 1:
PIN 1. ANODE
2. CATHODE
3. NC
4. EMITTER
5. COLLECTOR
6. BASE

CASE 730A–04
ISSUE G

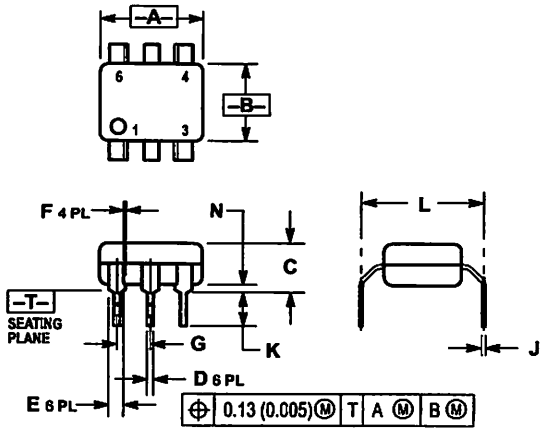


NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.

	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	0.320	0.350	8.13	8.89
B	0.240	0.260	6.10	6.60
C	0.115	0.200	2.93	5.08
D	0.016	0.020	0.41	0.50
E	0.040	0.070	1.02	1.77
F	0.010	0.014	0.25	0.36
G	0.100 BSC		2.54 BSC	
H	0.020	0.025	0.51	0.63
J	0.008	0.012	0.20	0.30
K	0.006	0.035	0.16	0.88
L	0.320 BSC		8.13 BSC	
S	0.332	0.390	8.43	9.90

***Consult factory for leadform option availability**

CASE 730C–04
ISSUE D



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. DIMENSION L TO CENTER OF LEAD WHEN FORMED PARALLEL.

	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	0.320	0.350	8.13	8.89
B	0.240	0.260	6.10	6.60
C	0.115	0.200	2.93	5.08
D	0.016	0.020	0.41	0.50
E	0.040	0.070	1.02	1.77
F	0.010	0.014	0.25	0.36
G	0.100 BSC		2.54 BSC	
J	0.008	0.012	0.21	0.30
K	0.100	0.150	2.54	3.81
L	0.400	0.425	10.16	10.80
N	0.015	0.040	0.38	1.02

***Consult factory for leadform option availability**

CASE 730D–05
ISSUE D

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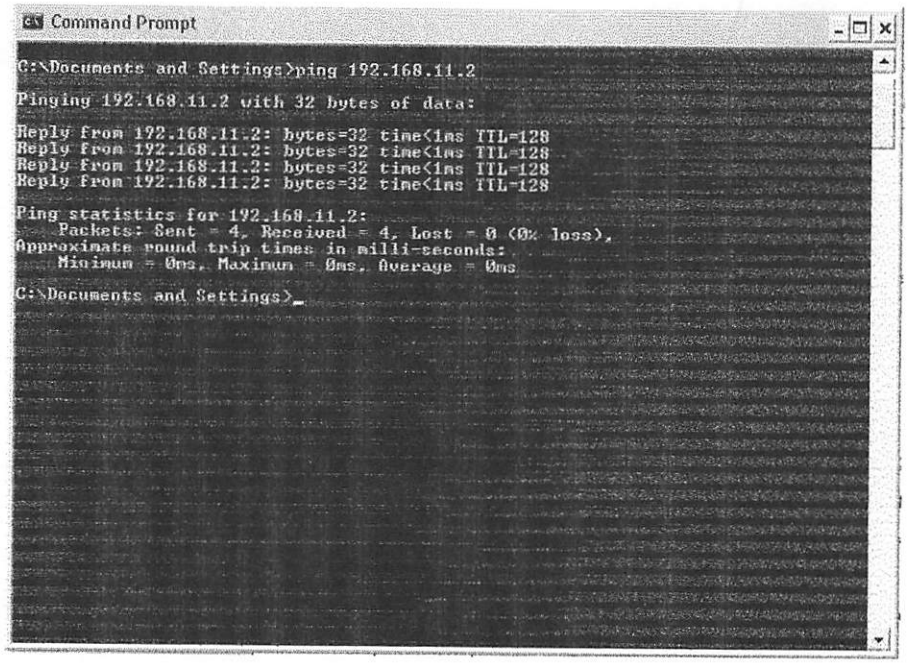
JAPAN: Nippon Motorola Ltd.; Tatsumi–SPD–JLDC, Toshikatsu Otsuki,
6F Seibu–Butsuryu–Center, 3–14–2 Tatsumi Koto–Ku, Tokyo 135, Japan. 03–3521–8315

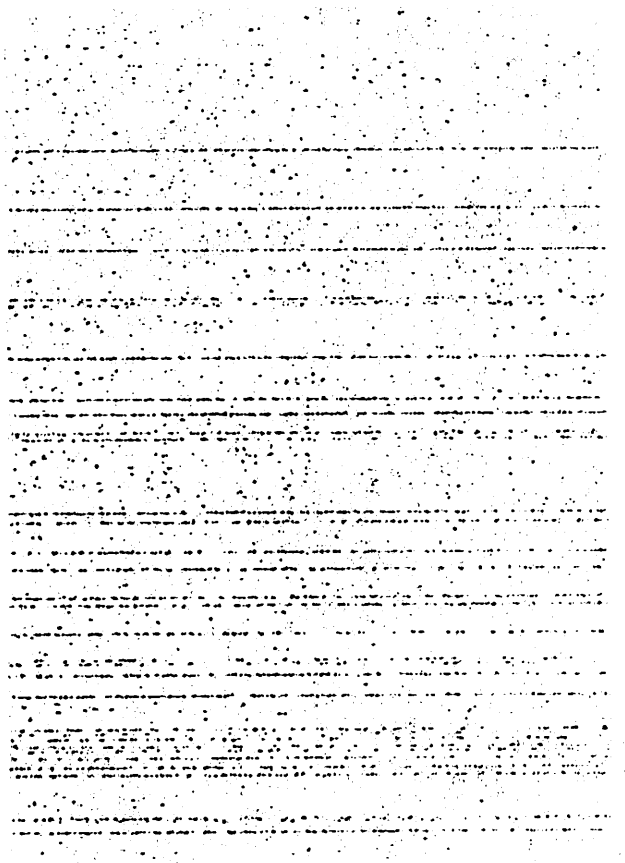
HONG KONG: Motorola Semiconductors H.K. Ltd.; 8B Tai Ping Industrial Park,
51 Ting Kok Road, Tai Po, N.T., Hong Kong. 852–26629298

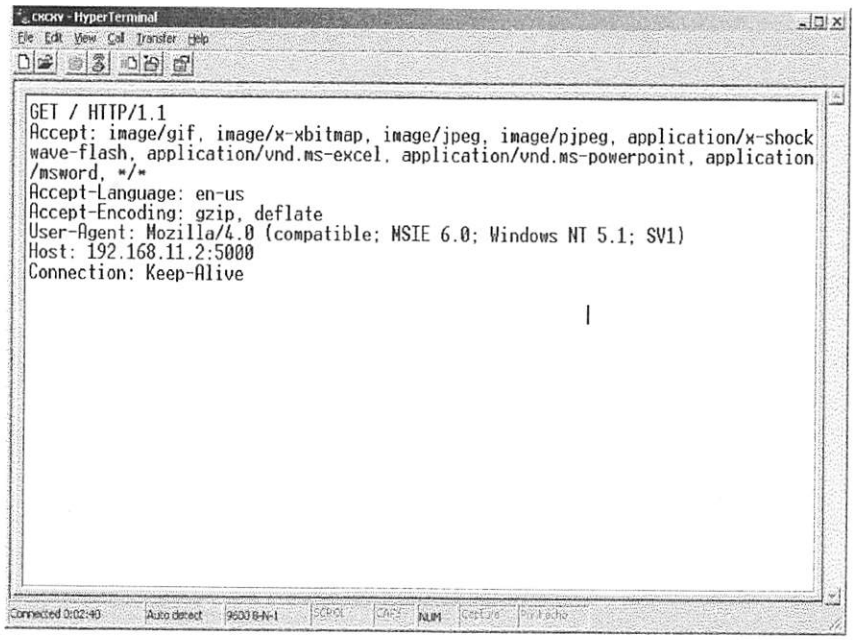


Gambar 4.3. Pengujian Dengan Melakukan Ping

Pengujian dilakukan dengan cara melakukan ping 192.168.11.2 yang merupakan alamat lokal IP dari Modul Ethernet EG-SR-7150MJ. Pengujian dilakukan untuk mengetahui apakah Modul Ethernet yang terpasang telah berkerja dengan baik atau tidak. Terlihat bahwa Modul Ethernet yang terpasang melakukan respon ketika dilakukan dilakukan ping. Dengan menunjukkan *Reply form* 191.168.11.2 seperti dalam gambar 4.3

- Hasil pengujian dengan melakukan pengiriman HTTP 1.1 dengan request GET pada PC 1 kedalam bentuk data serial pada PC 2





Gambar 4.4. Pengujian dengan HTTP/1.1

Pengujian dilakukan dengan cara mengirimkan *request* GET HTTP/1.1 dari *web browser* pada PC 1 ke PC 2. Pengujian dilakukan untuk mengetahui apakah modul ethernet yang terpasang bekerja dengan baik atau tidak, terlihat bahwa modul Ethernet yang terpasang dapat mengkonversi data TCP/IP ke dalam bentuk data serial pada PC 2 seperti ditunjukkan pada gambar 4.4

4.2.2. Pengujian Rangkaian Antarmuka RS-232(LVTTL) dan RS-232(TTL)

1. Tujuan.

Tujuan dari pengujian rangkaian antarmuka RS-232 adalah untuk mengecek apakah sesuai dengan apa yag disebutkan di dalam *datasheet* bahwa

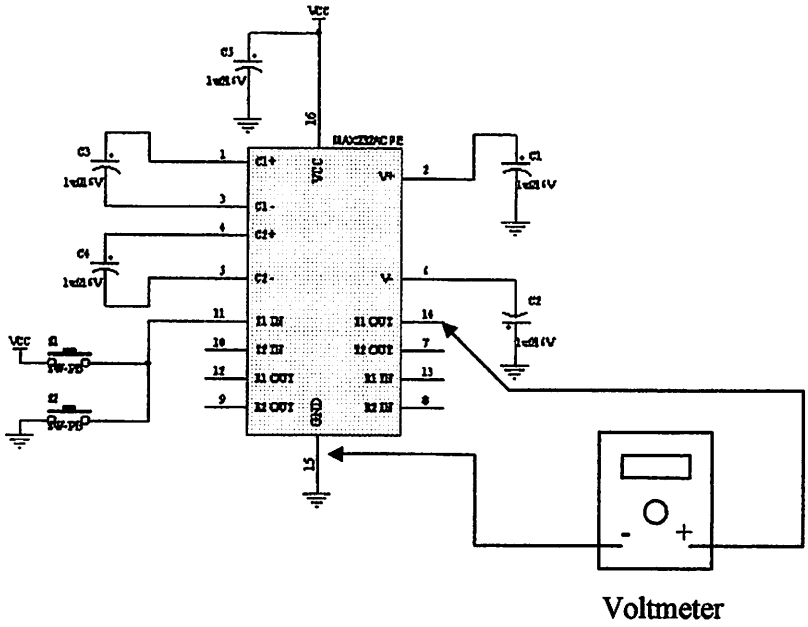
apabila RS-232 menerima 0V akan mengeluarkan +15V dan apabila menerima +5V akan mengeluarkan -15V.

2. Peralatan yang dibutuhkan

- Catu daya untuk RS-232(LVTTL) sebesar +3.3V dan +5V untuk RS-232(TTL)
- Switch.
- Multitester.

3. Prosedur pengujian

- Merangkai rangkaian seperti pada gambar 4.5.
- Memasang catudaya untuk masing-masing pengujian.
- Mengukur tegangan input dan output RS-232.



Gambar 4.5. Rangkaian Pengujian RS-232(LVTTL) dan RS-232(TTL)

4. Hasil pengujian :

Dari hasil pengujian dapat diketahui bahwa rangkaian RS-232 dapat berfungsi dengan baikhal ini dapat diketahui dengan melihat hasil pengukuran keluaran dari pin 14 pada RS-232, berikut ini adalah hasil pengukuran dari output pin 7 RS-232

Tabel 4.1 Hasil pengukuran output RS-232

RS 232(TTL)			Output
INPUT	LOW	0.24 Volt	9.01 Volt
	HIGH	4.69 Volt	-9.01 Volt

Tabel 4.1 Hasil pengukuran output RS-232 (LVTTL)

RS 232 (LVTTL)			Output
INPUT	LOW	0.20 Volt	7.76 Volt
	HIGH	3.01 Volt	-7.76 Volt

4.2.3. Pengujian Sistem Mikrokontroler

1. Tujuan.

Untuk mengetahui kondisi awal dari mikrokontroler apakah sudah sesuai dengan yang direncanakan.

2. Peralatan Yang Dibutuhkan.

- *Personal Computer* (PC)
- Sistem mikrokontroler.

3. Prosedur Pengujian.

- Membuat program yang digunakan dalam pengujian mikrokontroler.
- Program yang digunakan dalam pengujian mikrokontroler ini merupakan program sederhana dengan memasukkan bilangan 0FH dan F0H ke *port* 2.
- *Port* 2 AT89S8252. Program yang dibuat adalah sebagai berikut :

```
        ORG     0H
MULAI:  MOV     P2,#0FH         ;kondisi satu
        CALL    DELAY
        MOV     P2,# F0H        :kondisi dua
        CALL    DELAY
        JMP     MULAI
DELAY:  MOV     R0,#0
DELAY1: MOV     R5,#50H
        DJNZ    R5,$
        DJNZ    R0,DELAY1
        END
```

C. Membuat rangkaian seperti Gambar 4.1:

Gambar 4.6. Diagram Blok Pengujian Mikrokontroler

- Memasang catu rangkaian sebesar 5V.

- Men*download* program diatas.
- Mengamati keluaran pada LED d*isplay*.
- Hasil pengujian.

Hasil pengujian mikrokontroller adalah sebagai berikut :

Tabel 4.1.

Hasil Pengujian Sistem Mikrokontroler

KONDISI	KELUARAN PADA LED DISPLAY							
	Bit 0	**Bit 1**	**Bit 2**	**Bit 3**	**Bit 4**	**Bit 5**	**Bit 6**	**Bit 7**
Satu	0	0	0	0	1	1	1	1
Dua	1	1	1	1	0	0	0	0

Apabila sistem mikrokontroler dapat bekerja dengan baik maka hasil keluaran tampilan LED akan sesuai dengan data masukan yang diberikan lewat program. Dalam tabel tersebut, nilai 1 menunjukkan bahwa LED dalam keadaan menyala, sedangkan nilai 0 menunjukkan LED dalam keadaan mati.

Pada saat *port* 2 diberi bilangan 0FH, LED pada P2.0 sampai dengan P2.3 padam, dan LED pada P2.4 sampai P2.7 nyala. Ketika *port* 1 diberi bilangan F0H, P2.0 sampai P2.3 nyala dan P2.4 sampai P2.7 padam. Kemudian program terus mengulang sehingga LED akan menyala dan padam secara bergantian.

4.2.4. Pengujian Rangkaian Driver Relay

1. Tujuan

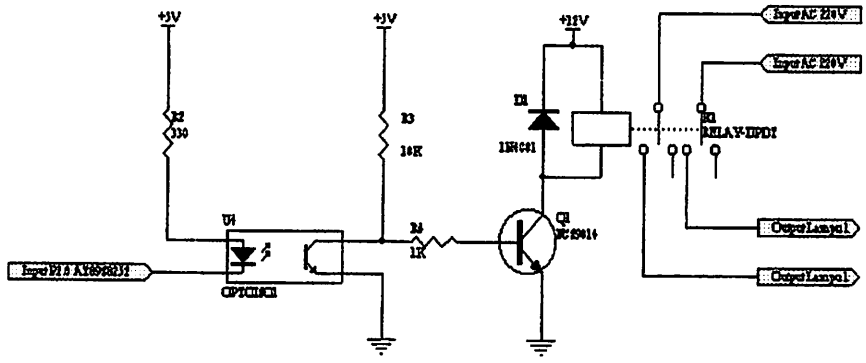
- Mengetahui unjuk kerja *relay* pada saat dioperasikan yang difungsikan untuk menyalakan dan mematikan lampu. *Relay* yang digunakan adalah *relay* DPDT (*dual pole dual totem*).

2. Peralatan yang digunakan :

- Multimeter
- Catu daya 12V DC
- Catu daya 5V DC

3. Prosedur pengujian

- Menghubungkan catu daya 12 V pada rangkaian *relay*.
- Menghubungkan *common relay* dengan kutub positif catu daya.
- Mengamati perubahan kuat arus Ic dan Ib, dan mencatat hasilnya pada Tabel 4.2.



Gambar 4.7. Gambar Rangkaian Pengujian Driver Relay

4. Hasil pengujian dan analisis

Hasil pengujian rangkaian relay ditunjukkan dalam Tabel 4.2

Tabel 4.2 Hasil Pengujian Rangkaian Driver Relay

Arus Yang Diukur	Hasil Pengukuran (mA)	Hasil Perhitungan (mA)
Ic	70.3	76.4
Ib	4,95	5.09

$$\text{Error} = \frac{|perhitungan - pengukuran|}{perhitungan} \times 100\%$$

$$\text{Error Ic} = \frac{|76.4 - 70.3|}{76.4} \times 100\%$$

$$\text{Error Ic} = 7.98\%$$

$$\text{Error Ib} = \frac{|5.09 - 4.95|}{5.09} \times 100\%$$

$$\text{Error Ib} = 2.75\%$$

4.3. Pengujian Perangkat Keras dan perangkat lunak Secara Keseluruhan

4.3.1 Pengujian Perangkat Keras Secara Keseluruhan

1. Tujuan.

Tujuan dari pengujian perangkat keras secara keseluruhan ini adalah untuk mengetahui kinerja perangkat keras secara keseluruhan apabila dijalankan sesuai perintah yang kita jalankan.

2. Peralatan Yang Dibutuhkan.

- *Personal Computer* (PC)
- Kabel LAN dan konektor RJ-45
- Catu daya 5V
- Catu daya 3.3V

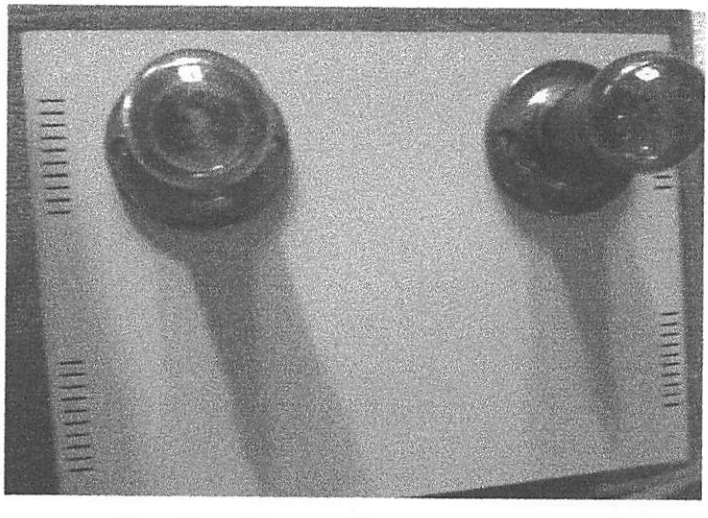
3. Prosedur Pengujian.

- Merangkai semua perangkat keras menjadi satu sesuai dengan blok diagram.
- Mengaktifkan catu daya.
- Memasukkan alamat IP lokal dari web server http://192.168.11.2
- Mengamati kondisi lampu

4. Hasil pengujian :

Hasil Pengujian kondisi awal lampu 1dan lampu 2

- Kondisi awal lampu dalam keadaan padam semua

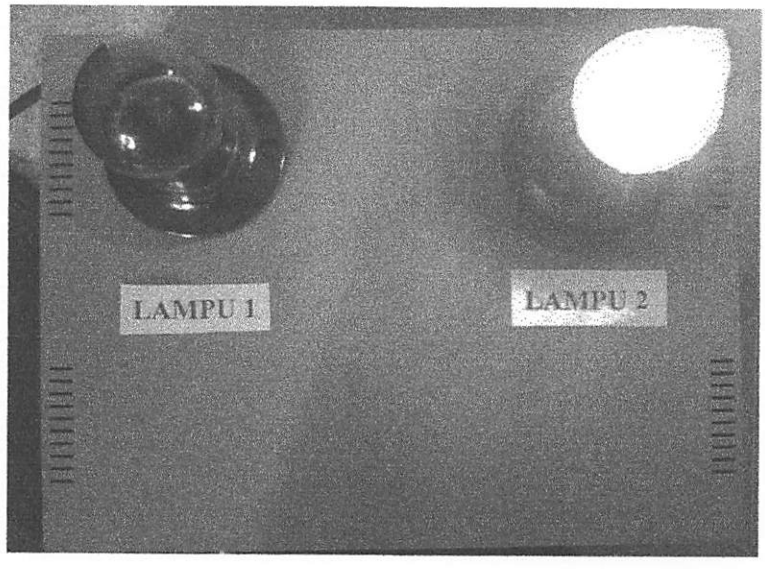


Gambar 4.8. Kondisi Lampu Padam

- Kondisi Lampu 1 menyala dengan mengklik link http://192.168.11.2/B11

Gambar 4.9. Lampu 1 Menyala

- Kondisi lampu 2 menyala dengan mengklik link http://192.168.11.2/B21



Gambar 4.10. Lampu 2 Menyala

- Kodisi Lampu 1 dan Lampu 2 menyala dengan mengklik link http://192.168.11.2/B11 dan link http://192.168.11.2/B21

Gambar 4.11. Kedua Lampu Menyala

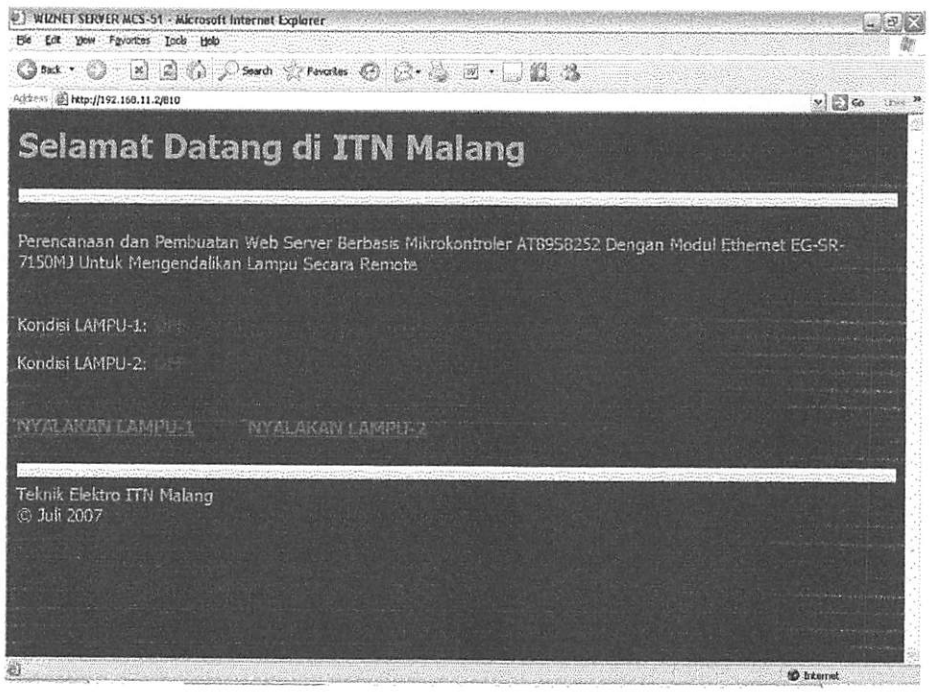
Kondisi-kondisi lampu diatas adalah link untuk menyalakan lampu 1 dan lampu 2 sedangkan untuk mematikan lampu maka link-nya adalah sebagai berikut:

- http://192.168.11.2/B10 (matikan lampu 1)
- http://192.168.11.2/B20 (matikan lampu 2)

4.3.2. Pengujian perangkat Lunak Pada PC-Client

Program yang digunakan adalah Internet Explorer V6.0 yang berjalan di Microsoft Windows XP profesional SP1, *web browser* akan mengirimkan request

GET ke *Web Server* dengan alamat IP lokal http://192.168.11.2 dan Web Server akan mengirim respon dari request tersebut, berikut tampilan utama atau tampilan awal dari sistem pengendalian lampu secara remote:



Gambar 4.12.

Halaman Web Utama Dari Pemantauan Dan Pengendalian Lampu Secara Remote

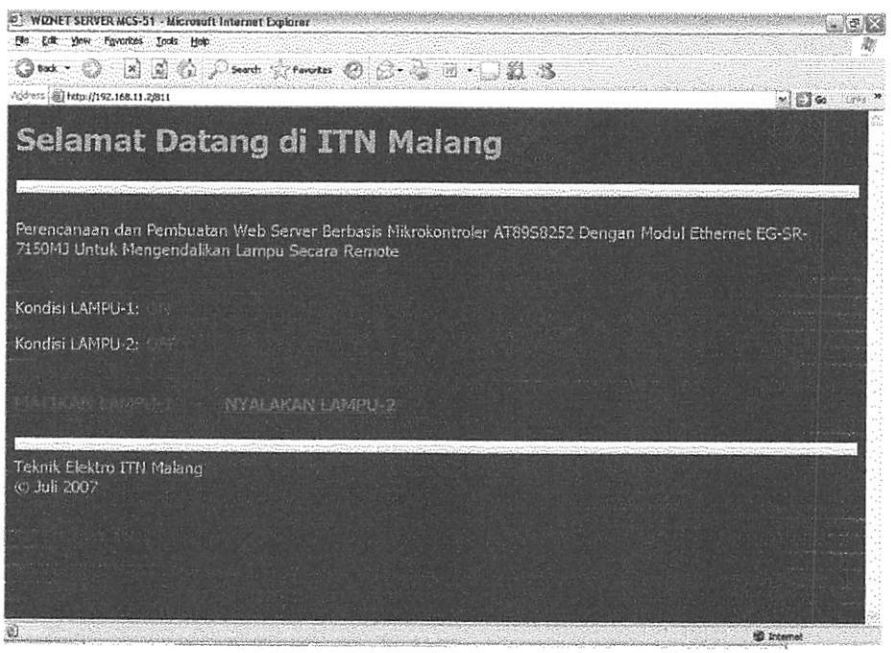
Dari tampilan halaman utama tersebut dapat kita lihat bahwa halaman tersebut cukup sederhana mengingat keterbatasan dari Web Server itu sendiri, informasi dari halaman tersebut terdiri dari :

- Header selamat datang di ITN Malang
- Judul Skripsi
- Kondisi atau status lampu

- Link untuk menyalakan dan mematikan lampu
- Jurusan Teknik Elektro Malang
- Copyright juli 2007

Ada beberapa link yang dapat diakses dalam halaman tersebut diantaranya adalah :

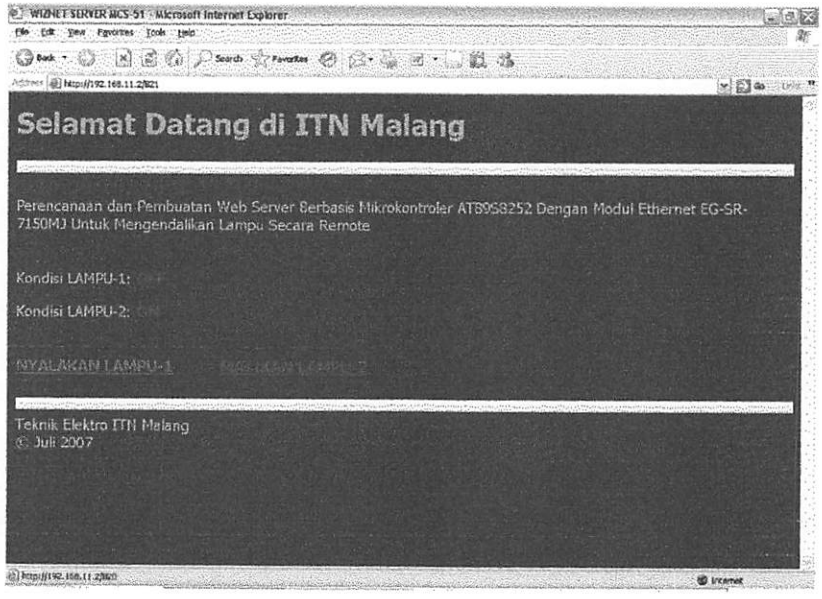
- Link untuk menyalakan lampu 1 alamat link-nya http://192.168.11.2/B11 berikut tampilan halaman webnya :



Gambar 4.13.

Halaman Web Untuk Menyalakan Lampu 1

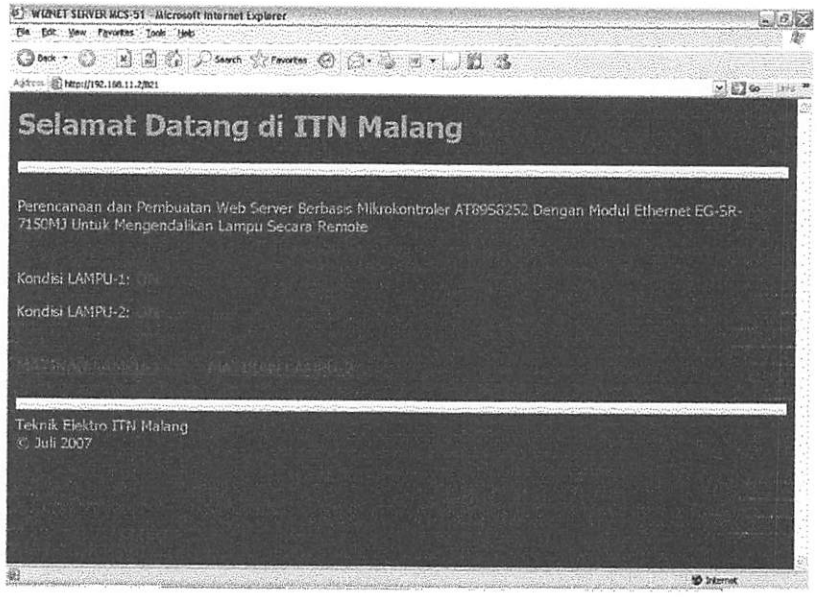
- Link untuk menyalakan lampu 2 alamat link-nya http://192.168.11.2/B21



Gambar 4.14.

Halaman Web Untuk Menyalakan Lampu 2

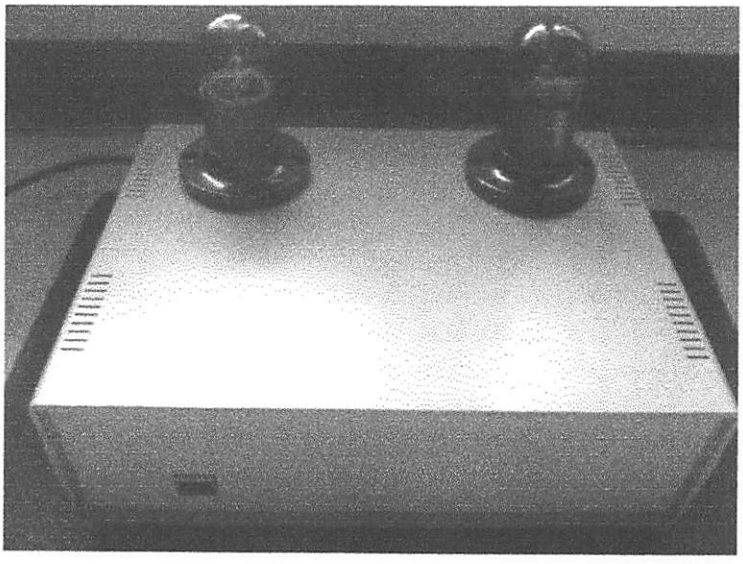
- Tampilan halaman web lampu 1 dan lampu 2 nyala



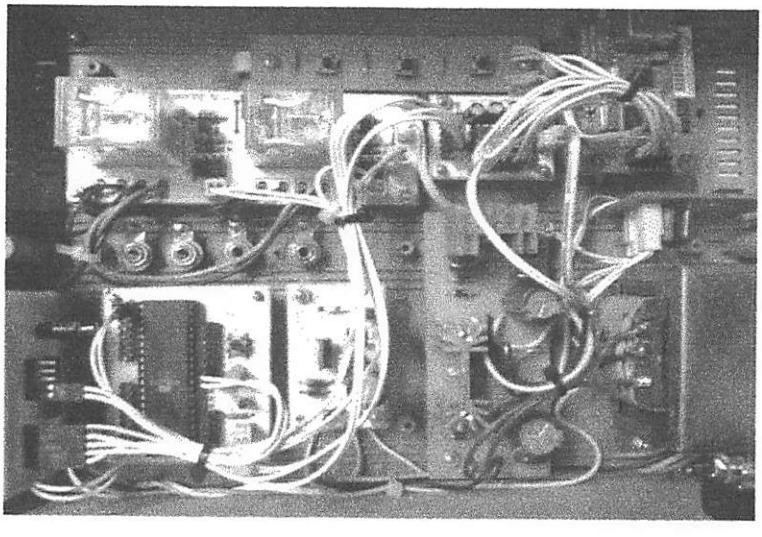
Gambar 4.15.

Halaman Web Pada Kondisi Lampu 1 Dan Lampu2 Menyala

- **Foto keseluruhan alat**



(a)



(b)

BAB V

PENUTUP

5.1. Kesimpulan

Dari perencanaan, pembuatan, dan pengujian yang telah dilakukan dapat ditarik kesimpulan sebagai berikut:

1. Dengan melakukan Ping pada alamat lokal IP 192.168.11.2 didapatkan bahwa Modul Ethernet EG-SR-7150MJ merespon dengan baik dan menampilkan *reply from* dari IP tersebut.
2. Pengujian HTTP/1.1 dengan request GET pada alamat IP http://192.168.11.2 menghasilkan respon yang sangat baik dengan ditampilkannya respon tersebut melalui program *Hyperterminal.*
3. Pada pengujian Driver Relay dengan menerima masukan logika *high (ON)* dan logika *low (OFF)* secara bergantian tidak ditemukan adanya *Error,* dengan kata lain bilamana masukan logika *high (ON)* lampu menyala dan logika *low (OFF)* lampu padam.
4. Pada pengujian sistem secara keseluruhan didapat hasil yang stabil dengan mencoba menyalakan dan mematikan lampu secara berulang-ulang melalui link yang terdapat pada halaman web.

5.2. Saran

1. Karena keterbatasan dari mikrokontroler sebagai *Web Server* yang hanya bisa menampilkan informasi berupa teks saja maka di upayakan untuk masa yang akan datang ada penyempurnaan halaman web yaang memasukkan unsur gambar dan animasi.
2. Penggunaan rangkaian RS-232 bisa dihilangkan dengan mengganti mikrokontroler dari keluarga AVR type (L) yang bekerja pada level tegangan 3.3V

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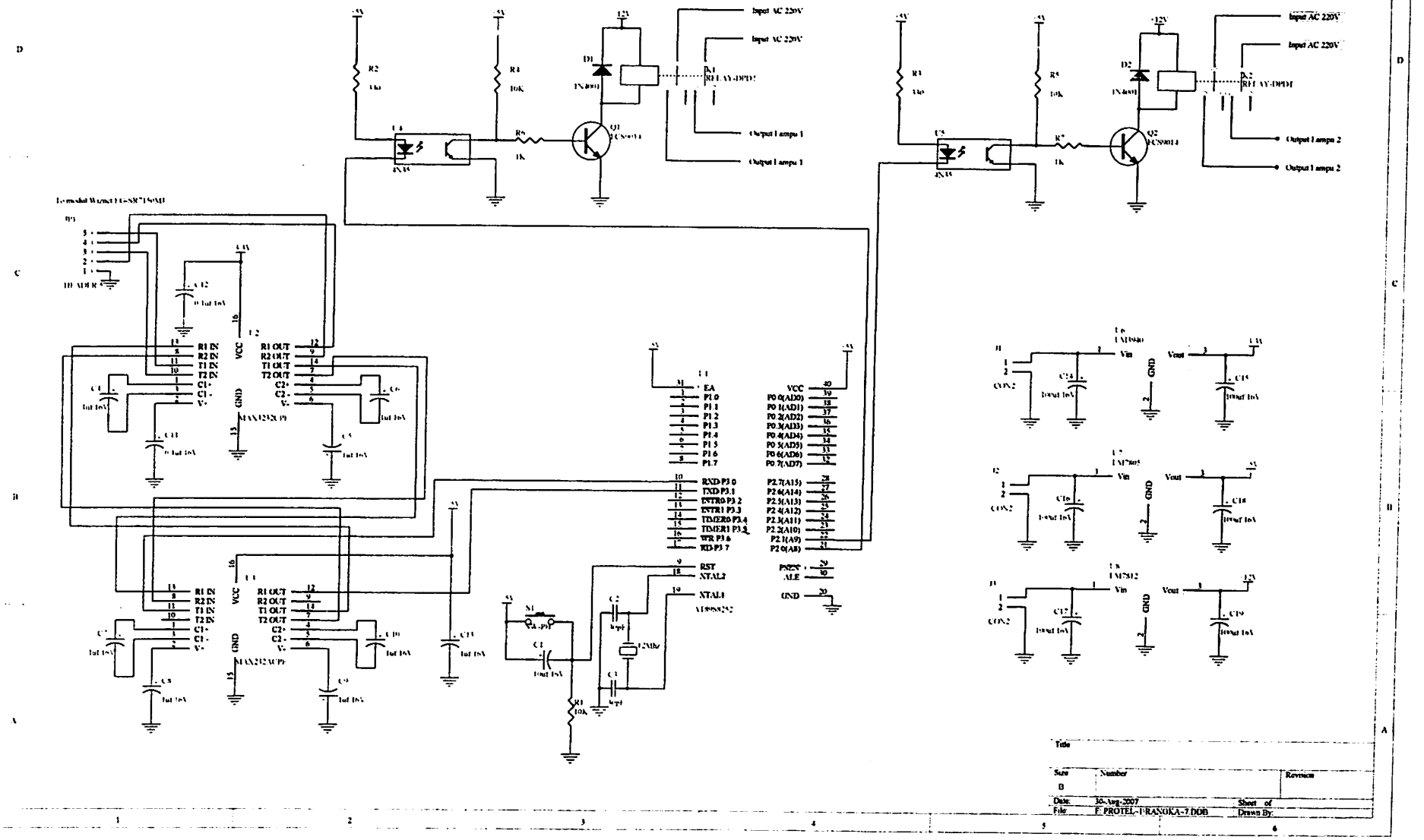
[9]. Lee, Berners, *RFC 1945:"hypertext Transfer Protocol (HTTP)*", request For Comment Standard, 1996.


Input AC 220V
Input AC 220V
Output Lampu 1
Output Lampu 1
Input AC 220V
Input AC 220V
Output Lampu 2
Output Lampu 2
RELAY-DPDT
RELAY-DPDT
MAX232(N)
MAX232(N)
12MHz
Title
Size
B
Number
Revision
Date: 30-Aug-2007
File: F:\PROTEL-1\RANGKA-7.DDB
Sheet of
Drawn By:

INSTITUT TEKNOLOGI NASIONAL
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MALANG

FORMULIR BIMBINGAN SKRIPSI

Nama : Moh.Zulkarnain
Nim : 00.17.082
Masa Bimbingan : 11-April-2007 s/d 11-Oktober-2007
Judul Skripsi : Perencanaan Dan Pembuatan Web Server Berbasiskan Mikrokontroler AT89S8252 Dengan Modul Ethernet EG-SR-7150MJ Untuk Mengendalikan Lampu Secara Remote

No	Tanggal	Uraian	Paraf Pembimbing
1		Bab I	
2		Bab II	
3		Bab III	
4		Bab IV	
5		Bab V diperbaiki.	
6		Oke	
7			
8			
9			
10			

Malang,

Dosen pembimbing I

Ir. F. Yudi Limpraptono, MT
NIP Y. 1039500274

Form S-4a

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Jl. Bendungan Sigura – gura No.2
MALANG

FORMULIR BIMBINGAN SKRIPSI

Nama : Moh.Zulkarnain
Nim : 00.17.082
Masa Bimbingan : 11-April-2007 s/d 11-Oktober-2007
Judul Skripsi : Perencanaan Dan Pembuatan Web Server Berbasiskan Mikrokontroler AT89S8252 Dengan Modul Ethernet EG-SR-7150MJ Untuk Mengendalikan Lampu Secara Remote

No	Tanggal	Uraian	Paraf Pembimbing
1	4/8 '2007	Bab I Susunan kata pengantar	
2	6/8 '2007	Bab II Sumber.	
3	7/8 '2007	Bab III Driver Relay	
4	9/8 '2007	Bab IV hasil pengujian. Kesesuaian	
5	10/8 '2007	Bab V Kesimpulan. & perbaiki	
6			
7			
8	1/9 '2007	ACC ICOMPRE	
9			
10			

Malang,

Dosen pembimbing II

Joseph Dedy Irawan ST, MT
NIP. 132315178

Form S-4a

LAMPIRAN

SOFTWARE

```
/*
  WEBSERV.C

  Program webserver berbasis mikrokontroler MCS-51

*/

#include <reg51.h>
#include <stdio.h>
#include <string.h>

#define ON 1
#define OFF 0

sbit BEBAN1 = P2 ^ 0;
sbit BEBAN2 = P2 ^ 1;

bit STATUS_BEBAN1 = OFF;
bit STATUS_BEBAN2 = OFF;

code char *PAGE1 = {
"HTTP/1.1 200 OK\r\n"
"Server: MCS51 n WIZNET\r\n" \
"Content-Length: 818\r\n" \
"Connection: Keep-Alive\r\n" \
"Content-Type: text/html\r\n" \
"\r\n" \
"<HTML>" \
"  <HEAD>" \
"    <TITLE>WIZNET SERVER MCS-51</TITLE>" \
"  </HEAD>" \
"  <BODY BGCOLOR=maroon TEXT=orange>" \
"    <FONT FACE=Tahoma>" \
"    <H1>Selamat Datang di ITN Malang</H1>" \
"    <HR SIZE=15 COLOR=yellow><BR>"
};

code char *PAGE2 = {
"    <BR><BR><HR SIZE=15 COLOR=yellow>" \
"    Teknik Elektro ITN Malang<BR>" \
```

```
"     &copy; Juli 2007" \
"     </FONT>" \
"   </BODY>" \
"</HTML>" \
"\r\n"
};

unsigned T0_Counter = 0;
unsigned char cbuf[64];

/*******************************/
/*   RUTIN INTERUPSI TIMER 0   */
/*******************************/
void Timer0_ISR (void) interrupt 1
{
  EA = 0;
  T0_Counter++;
  EA = 1;
}


void delay(unsigned int n)
{
  unsigned int i, j;

  for (i=1;i<=n;i++) for (j=1;j<=10;j++);
}

void clear_cbuf()
{
  char i;

  for (i=0;i<=63;i++)
  {
    cbuf[i] = 0;
  }
}
```

```
/* PROGRAM UTAMA */

void main()
{
  char ch, i;

  BEBAN1 = 0; BEBAN2 = 0;     //semua off

  SCON = 0x52;
  TMOD = 0x22;
  TH1 = 0xFD;   //baudrate 1200
  TR1 = 1;

  TH0 = 0xff - 100;
  TL0 = TH0;
  ET0 = 1;
  TR0 = 1;

  EA = 1;

  while(1)
  {
    if (RI)
    {
      ch = SBUF; RI = 0;
      if (ch=='G' || ch=='g')
      {
        T0_Counter = 0;
        while (!RI && T0_Counter<=1000);
        if (T0_Counter>=1000) goto IGNORE;
        ch = SBUF; RI = 0;
        if (ch=='E' || ch=='e')
        {
          T0_Counter = 0;
          while(!RI && T0_Counter<=1000);
          if (T0_Counter>=1000) goto IGNORE;
          ch = SBUF; RI = 0;
          if (ch=='T' || ch=='t')
          {
            clear_cbuf();
```

```
            for (i=0;i<=10;i++)
            {
              T0_Counter = 0;
              while(!RI && T0_Counter<=1000);
              if (T0_Counter>=1000)
              {
                printf(PAGE1);
                printf("<P><I>Bad Request: Browser Anda mengirimkan
perintah<BR>");
                printf("yang tidak saya mengerti.</I></P>");
                printf("<BR><BR>");
                printf(PAGE2);
                goto IGNORE;
              }
              cbuf[i] = SBUF; RI = 0;
            }

            printf(PAGE1);
            printf("<P>Perencanaan dan Pembuatan Web Server\r\n");
            printf("Berbasis Mikrokontroler AT89S8252 Dengan Modul\r\n");
            printf("Ethernet EG-SR-7150MJ Untuk Mengendalikan Lampu Secara
Remote");
            printf("<BR><BR><BR>");

            if (cbuf[2]=='B' && cbuf[3]=='1' && cbuf[4]=='0')
            {
              BEBAN1 = 0;
              STATUS_BEBAN1 = OFF;
            }
            else if (cbuf[2]=='B' && cbuf[3]=='1' && cbuf[4]=='1')
            {
              BEBAN1 = 1;
              STATUS_BEBAN1 = ON;
            }
            else if (cbuf[2]=='B' && cbuf[3]=='2' && cbuf[4]=='0')
            {
              BEBAN2 = 0;
              STATUS_BEBAN2 = OFF;
            }
            else if (cbuf[2]=='B' && cbuf[3]=='2' && cbuf[4]=='1')
```

```
            {
              BEBAN2 = 1;
              STATUS_BEBAN2 = ON;
            }

            if (STATUS_BEBAN1==ON)
              printf("<P>Kondisi LAMPU-1: <FONT COLOR=RED><B>ON
</B></FONT>");
            else
              printf("<P>Kondisi LAMPU-1: <FONT
COLOR=RED><B>OFF</B></FONT>");

            if (STATUS_BEBAN2==ON)
              printf("<P>Kondisi LAMPU-2: <FONT COLOR=RED><B>ON
</B></FONT>");
            else
              printf("<P>Kondisi LAMPU-2: <FONT
COLOR=RED><B>OFF</B></FONT>");

            printf("<BR><BR><BR>");

            if (STATUS_BEBAN1==ON)
            {
              printf("<A HREF=B10>");
              printf("<B><FONT COLOR=RED  SIZE=3>MATIKAN  LAMPU-
1</FONT></B></A>");
            }
            else
            {
              printf("<A HREF=B11>");
              printf("<B><FONT COLOR=GREEN SIZE=3>NYALAKAN
LAMPU-1</FONT></B></A>");
            }


printf("          ");
            if (STATUS_BEBAN2==ON)
            {
              printf("<A HREF=B20>");
```

```
            printf("<B><FONT COLOR=RED  SIZE=3>MATIKAN LAMPU-2
</FONT></B></A>");
            }
            else
            {
              printf("<A HREF=B21>");
              printf("<B><FONT COLOR=GREEN SIZE=3>NYALAKAN
LAMPU-2</FONT></B></A>");
            }
            printf(PAGE2);
          }
        }
      }
IGNORE:
      delay(1);
    }
  }
}
```

HARDWARE

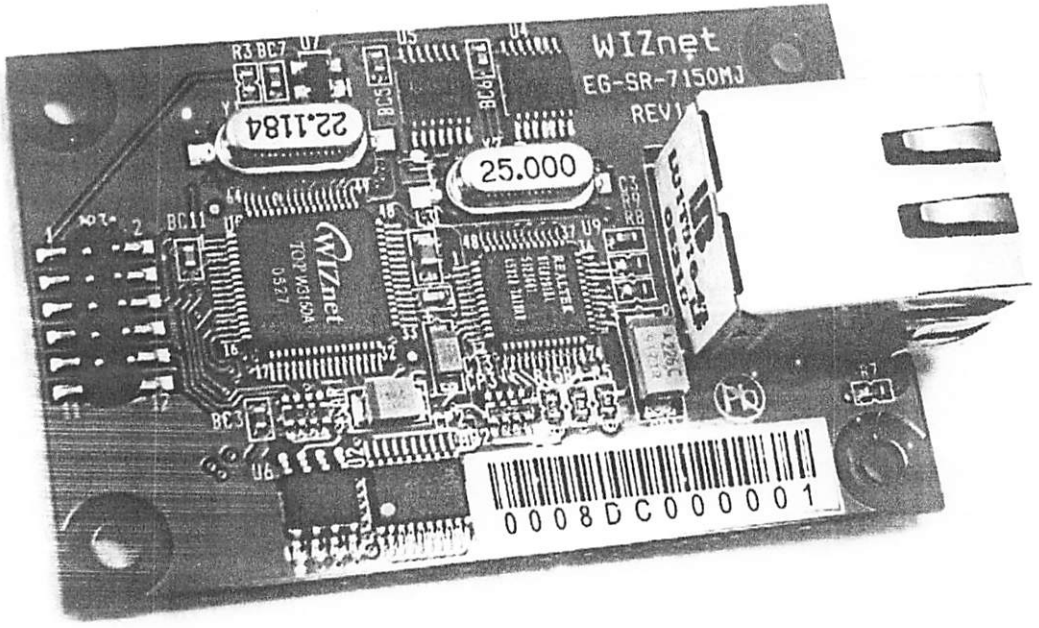
	CD (Containing Manual, H/W & S/W Materials)

☞ Please immediately notify your sales representative if any of the items above is missing or damaged.

EG-SR-7150MJ

User's Manual

(V 1.1)



WIZnet

For more information, visit our website at http://www.wiznet.co.kr

If you have any question about WIZnet Products, write them down onto our Q&A Board on our website at www.wiznet.co.kr. A WIZnet engineer will promptly provide you with an answer.

EG-SR-7150MJ User's Manual

1. Introduction

The EG-SR-7150MJ is a gateway module that converts serial data into TCP/IP data type. It transmits the data sent by a serial equipment to the Internet and TCP/IP data to the equipment.

With the EG-SR-7150MJ mounted with an RJ-45 connector, users can have an easier and quicker interface with the Ethernet.

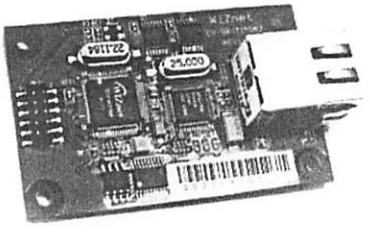
The EG-SR-7150MJ provides serial commands, with which the developers of any serial device can add local configuration capability to their products. For example, a card reader developer can program the keypad on a card reader to configure serial or network on-site without the use of a laptop or PC.

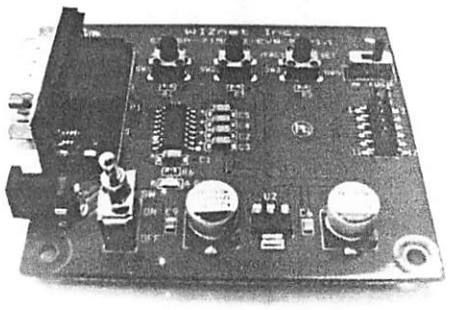
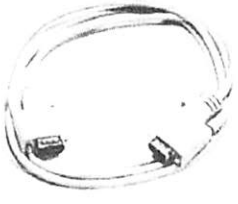
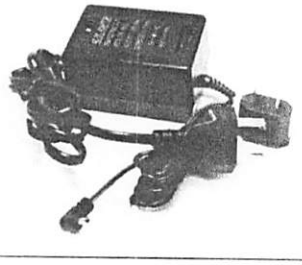
1.1. Key Features

- Ready-to-go serial to Ethernet gateway module mounted with an RJ-45 connector
- Serial Command Support
  - Simple command frame format
  - Comprehensive & readable command set for network and serial settings
  - On-site configuration without PC
- High stability & reliability by using a W3150A WIZnet Chip, a fully-hardwired TCP/IP stack
- Easy and powerful configuration program
- 10/100Mbps Ethernet interface, Max. 230Kbps Serial interface
- RoHS compliant

1.2. Products Contents (EG-SR-7150MJ-EVB)

The EG-SR-7150MJ-EVB, the evaluation kit for the EG-SR-7150MJ contains the following items;

	EG-SR-7150MJ Module

	Test Board for EG-SR-7150MJ
	12pin Cable (Connecting EG-SR-7150MJ to Test Board)
	Serial Cable (Connecting Serial Device to Test Board)
	LAN Cable (Connecting EG-SR-7150MJ to Host)
	Power (DC 5V Adaptor)

1.3. Specifications of the EG-SR-7150MJ

Category	Specifications
Form Factor	2mm Pitch 2x6 pins, 62x40 mm
LAN Interface	10/100 Mbps auto-sensing, RJ-45 connector
Protocol	TCP, UDP, IP, ARP, ICMP, MAC, (IGMP, PPPoE)
CPU	AT89C51RC2 (8bit MCU and 32K Flash)
Serial Interface	RS 232 (LVTTL)
Serial Signals	TXD, RXD, RTS, CTS, GND
Serial Parameters	Parity : None, Even, Odd Data bits : 7, 8 Flow control : RTS/CTS, XON/XOFF Speed : up to 230Kbps
Management	Configuration utility based on Windows
Temperature	0℃~70℃ (Operating), -40℃~85℃ (Storage)
Humidity	10~90%
Power	150mA @ 3.3V (max)
Size	40mm x 62mm x 17mm

2. Getting Started

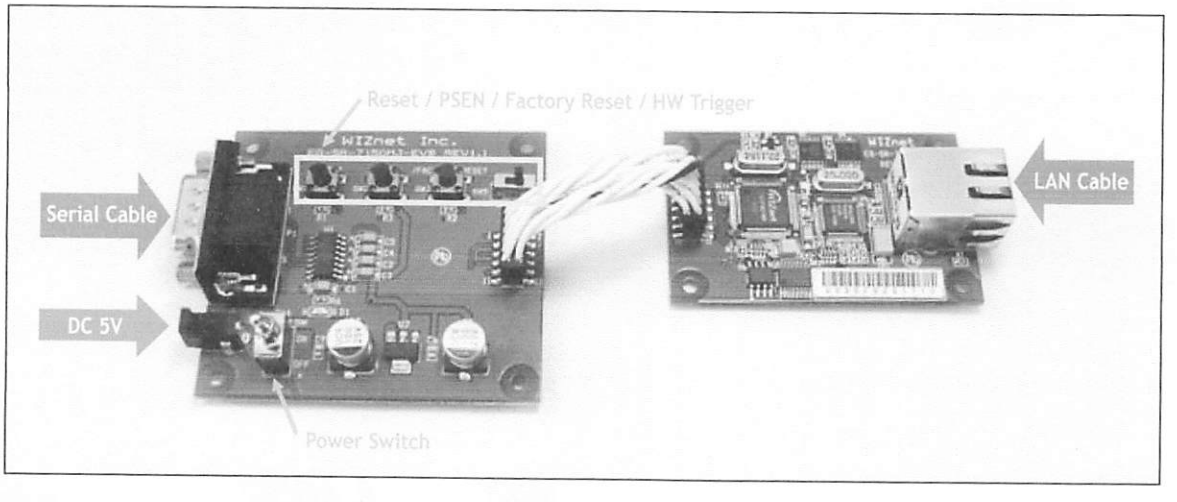
This Chapter describes how to set up and configure the EG-SR-7150MJ.

The following items are required to get started.

- Power Cable (included in the EG-SR-7150MJ-EVB package)
- Serial and Ethernet Cables (included in the of EG-SR-7150MJ-EVB package)
- PC or Laptop with Network Interface Card (hereafter, NIC) and/or one RS232 serial port

2.1. Hardware Installation procedure

Follow steps below to prepare the module and evaluation board for testing.



STEP 1: Connect the EG-SR-7150MJ module to the test board by using the 12pin cable.

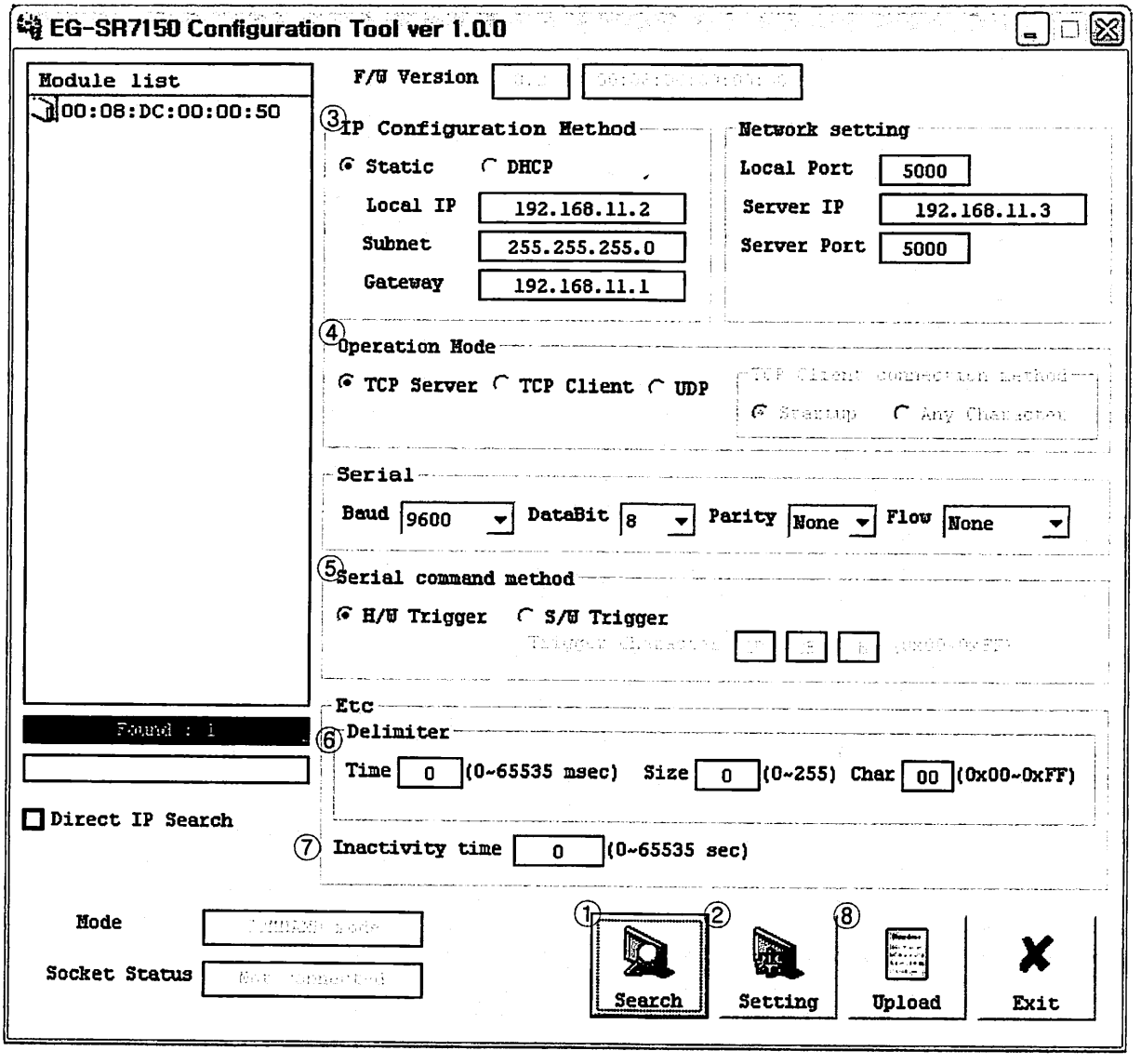
STEP 2: Connect the 5V DC power line to the power jack of the test board.

STEP 3: Use the RJ45 Ethernet cable in order to connect the module to an Ethernet network.

STEP 4: Use the serial data cable to connect the test board to a serial device.

2.2. Configuration Tool

2.2.1. Configuration tool features



① Search

The Search function is used to search all modules existing on the same Subnet. The UDP broadcast is used for searching modules on a LAN.

The MAC address for a searched module will be listed in the "**Module list**".

If **Direct IP Search** is checked, TCP will be used for searching instead of UDP. This mode is used more for searching the EG-SR-7150MJ modules on remote networks than local networks with the same subnet. An IP address assigned to the module will be required.

② Setting

If you select one of the MAC addresses listed in the "**Module list**", the configuration value of the selected module will be displayed. After changing each value in the configuration program, click the "**Setting**" button to complete the configuration.

The module will be initialized with the new configurations.

③ IP Configuration method: Static, DHCP

Static: The IP address can be manually assigned by users.

DHCP: The module assigns IP, subnet and gateway addresses by acquiring them from the DHCP server

☞ Other configurations should be set manually except for the IP configuration of DHCP.

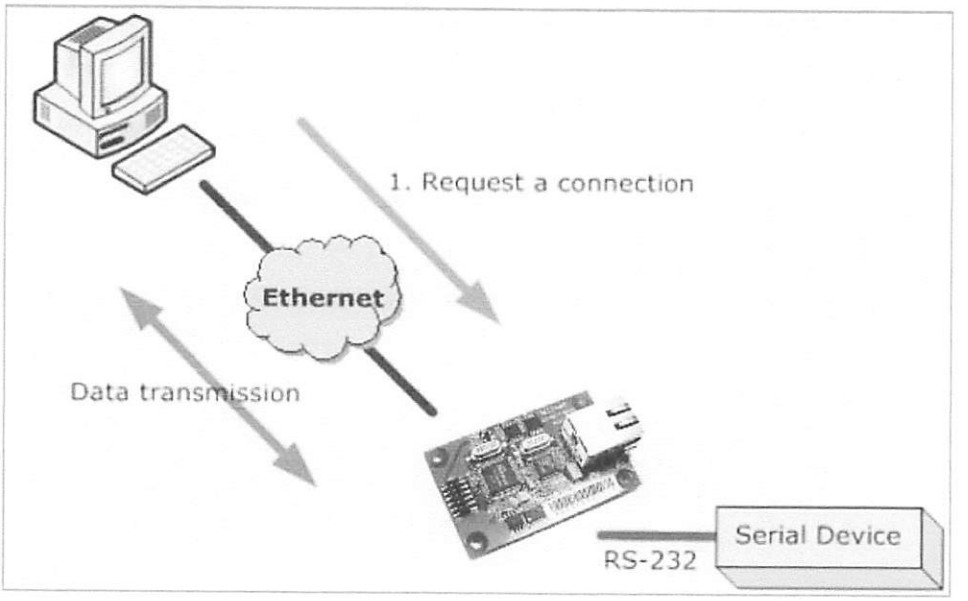
④ Operation mode: TCP server, TCP client, UDP

Three different operation modes are supported — TCP Server, TCP Client, and UDP.

The main difference between the TCP and UDP protocols is that TCP guarantees the delivery of data by requesting the recipient to send an acknowledgement to the sender. On the other hand, UDP does not require this type of verification, so data can be delivered quicker, but its delivery can not be guaranteed.

The TCP Server and TCP Client mode are related to the first step of connection establishment. Once the connection is established, data will be transparently transmitted in both directions (from Server to Client or from Client to Server).

TCP server mode

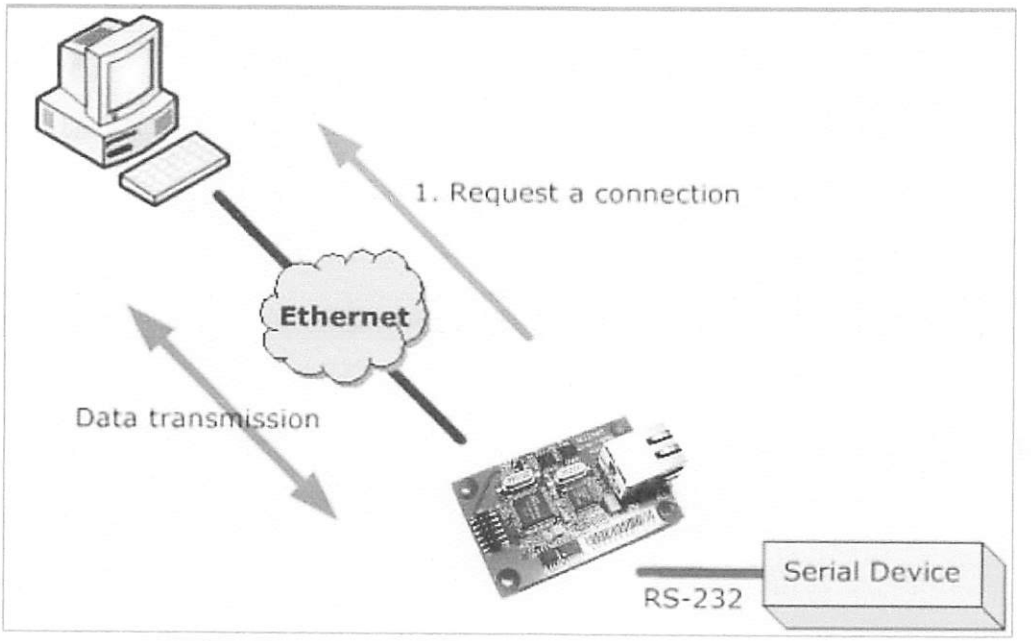


To operate this mode, the **Local IP, Subnet, gateway address and local port number** should be configured. The EG-SR-7150MJ waits to be connected by the host computer, allowing the host computer to establish a connection and get data from the serial device.

As illustrated in the figure above, the data transmission is as follows:

1. The host connects to the EG-SR-7150MJ which is configured as TCP Server Mode.
2. Once the connection is established, data can be transmitted in both directions - from the host to the EG-SR-7150MJ, and from the EG-SR-7150MJ to the host.

TCP client mode

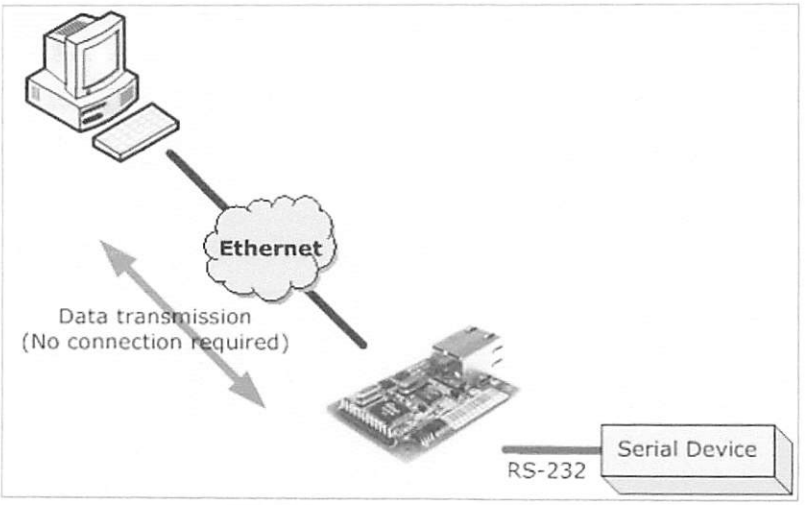


To operate this mode, the **Local IP, Subnet, gateway address, server IP, server port number** should be set. In the **TCP Client mode**, the EG-SR-7150MJ proceeds active open for establishing a TCP connection to a host computer.

As illustrated in the figure above, data transmission is as follows:

1. The EG-SR-7150MJ operating as TCP Client Mode establishes a connection based on the condition set in the **TCP client connection method** (**Startup, Any character**). i.e. the EG-SR-7150MJ can try to connect as soon as one starts up(**Startup**), or later when data from serial device arrives. (**Any character**).
2. After the connection is established, data can be transmitted in both directions - from the host to the EG-SR-7150-MJ, and from the EG-SR-7150-MJ to the host.

UDP mode



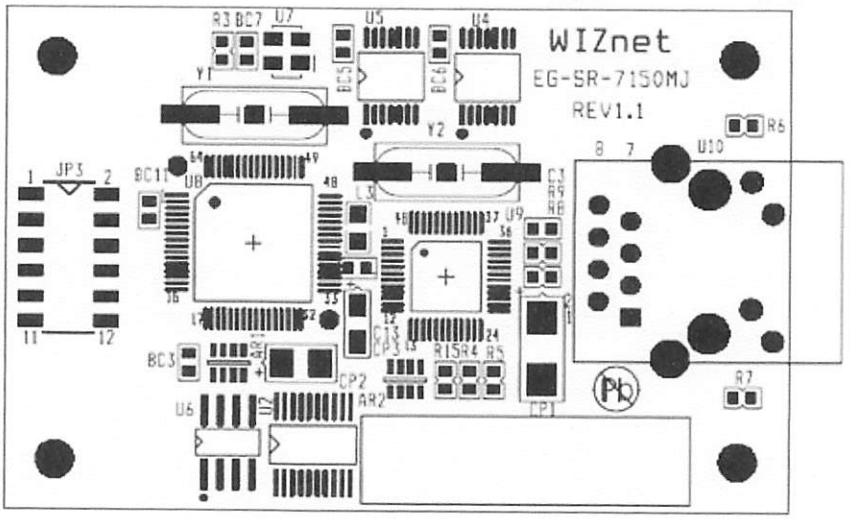
In UDP mode, any TCP/IP connection procedure is not required.

⑤ Serial command method: H/W trigger, S/W trigger

With this menu, you can designate how the Serial command mode can be entered. Two types are supported - H/W Trigger and S/W Trigger.

H/W trigger: Serial command mode can be triggered by pulling H/W trigger pin to low. It can be exited by pulling it to high.

```
-----------------------------------
            JP3
-----------------------------------
/RESET - 1   2 -  3.3V
   RXD - 3   4 - 3.3V
   CTS - 5   6 - /FACTORY_RESET
   TXD - 7   8 - /HW_TRIGGER
   RTS - 9   10 - /PSEN
   GND - 11  12 - GND
```



S/W trigger: Serial command mode can be triggered when 3 user-defined characters are detected. It can be exited by using the WR command.

⑥ Delimiter: Time, Size, Character

You can designate how the serial data can be packed and sent to the Ethernet. There are 3 delimiters - Time, Size and Character. If all of them are set as '0', whenever the serial data arrives, they will be sent to the Ethernet without any condition. When any of the three delimiters is satisfied, data can be sent to the Ethernet.

Ex) Delimiter: Size=10, Char=0x0D

Serial data: 0123456789abc

Ethernet data: 0123456789

☞ "abc" data remains in the serial buffer of module

⑦ Inactivity time

After the connection is established, if there is not any data transmission within the time defined in **"Inactivity time"**, the connection will be automatically closed.

⑧ Upload

Upload the firmware through the network.

☞ After uploading the firmware, 10~20 seconds are required for initialization.

2.3. Serial Communication Specification

In this chapter, we describe the structure of the data frames used in issuing commands and receiving responses to and from the device.

2.3.1. Frame Format

Command Frame format

Descriptor	STX	Command code	Parameter	ETX
Length(bytes)	1	2	Variable	1

Reply Frame format

Descriptor	STX	Reply code	Parameter	ETX
Length(bytes)	1	1	Variable	1

2.3.2. STX & ETX

Setting	Comments
STX	'<' : Hex = 3Ch
ETX	'>' : Hex = 3Eh

2.3.3. Reply Code

Reply	Comments
S	Command was successful
F	Command failed
1	Invalid command
2	Invalid parameter
E	Enter serial command mode

2.3.4. Command Code

Command	Parameter	Comments
WI	xxx.xxx.xxx.xxx (eg. 192.168.11.133)	Set Local IP
WS	xxx.xxx.xxx.xxx (eg. 255.255.255.0)	Set Subnet mask
WG	xxx.xxx.xxx.xxx (eg. 192.168.11.1)	Set Gateway
WP	0~65535	Set Local IP's port number
WD	0 : Static 1 : DHCP	Set the IP configuration method
WM	0 : TCP server 1 : TCP client 2 : UDP	Set the operation mode
WC	0 : startup 1 : any character	TCP client method
WB	XXXX eg. [Baudrate]1: 115200, 2: 57600, 3: 38400, 4: 19200, 5: 9600, 6: 4800, 7: 2400,8: 1200 [data byte] 7 : 7bit, 8bit [parity] 0 : no parity, 1 : Odd, 2 :Even [Flow] 0 : no, 1 : Xon/Xoff, 2 :RTS/CTS	Set the serial baud rate, data, parity and flow control. 4bytes:[Baud][data byte][parity][flow]
WT	0 : Disable 1 : H/W trigger 2 : S/W trigger	Set the serial command method
WE	xxxxxx (eg. In hex format : 2B 2B 2B)	Set the command mode character

2.3.3. Reply Code

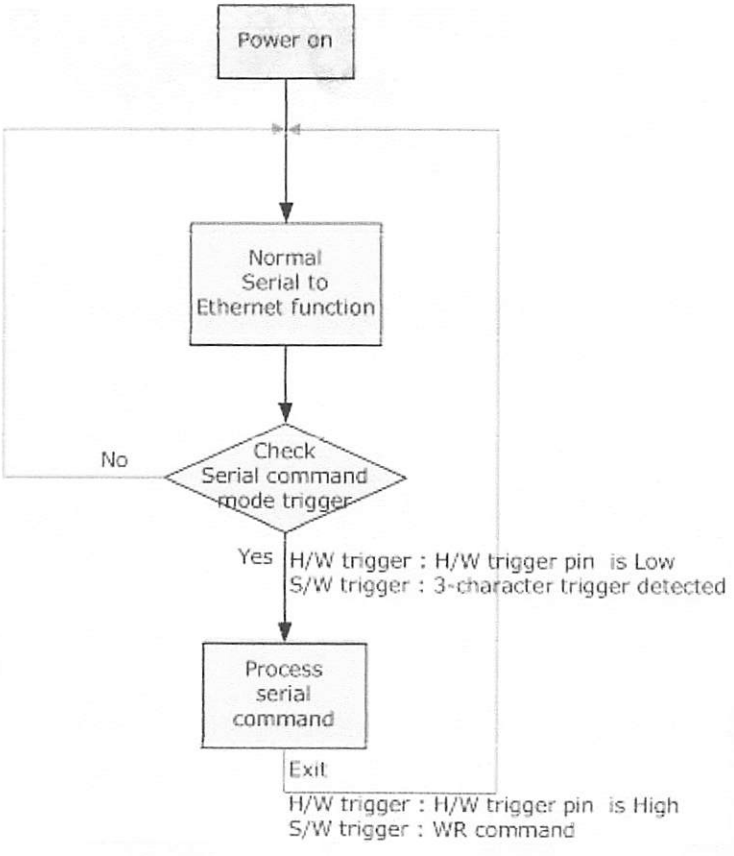
Reply	Comments
S	Command was successful
F	Command failed
1	Invalid command
2	Invalid parameter
E	Enter serial command mode

2.3.4. Command Code

Command	Parameter	Comments
WI	xxx.xxx.xxx.xxx (eg. 192.168.11.133)	Set Local IP
WS	xxx.xxx.xxx.xxx (eg. 255.255.255.0)	Set Subnet mask
WG	xxx.xxx.xxx.xxx (eg. 192.168.11.1)	Set Gateway
WP	0~65535	Set Local IP's port number
WD	0 : Static 1 : DHCP	Set the IP configuration method
WM	0 : TCP server 1 : TCP client 2 : UDP	Set the operation mode
WC	0 : startup 1 : any character	TCP client method
WB	XXXX eg. [Baudrate]1: 115200, 2: 57600, 3: 38400, 4: 19200, 5: 9600, 6: 4800, 7: 2400,8: 1200 [data byte] 7 : 7bit, 8bit [parity] 0 : no parity, 1 : Odd, 2 :Even [Flow] 0 : no, 1 : Xon/Xoff, 2 :RTS/CTS	Set the serial baud rate, data, parity and flow control. 4bytes:[Baud][data byte][parity][flow]
WT	0 : Disable 1 : H/W trigger 2 : S/W trigger	Set the serial command method
WE	xxxxxx (eg. In hex format : 2B 2B 2B)	Set the command mode character

WX	xxx.xxx.xxx.xxx (eg. 192.168.11.144)	Set server IP address
WN	0~65535	Set server port number
WR		Restart
OC	XX	Set delimiter character in hex
OS	0~255	Set delimiter size
OT	0~65535	Set delimiter time
OI	0~65535	Set Inactivity timer value
Command	Parameter	Comments
RI		Get Local IP
RS		Get Subnet mask
RG		Get Gateway
RP		Get Local IP's port number
RD		Get the IP configuration method
RM		Get the operation mode
RC		Get the TCP client method
RB		Get the serial baud rate
RT		Get the serial command method
RE		Get the command mode character
RF		Get the firmware version
RX		Get the server IP address
RN		Get the server port number
QC		Get delimiter character in hex
QS		Get delimiter size
QT		Get delimiter time
QI		Get Inactivity timer value

2.4. Operation Flow



2.5. Factory Default

While the Factory Reset is low and the /Reset is applied, the module is initialized with the factory default value.

IP configuration	Static
Local IP address	192.168.11.2
Subnet mask	255.255.255.0
Gateway address	192.168.11.1
Local port number	5000
Server IP address	192.168.11.3
Server port number	5000
Operation mode	TCP server mode
Serial port	9600 bps 8-N-1
Serial command method	H/W trigger

3. Demonstration and Test

In this chapter, three examples are given to show how functions of the EG-SR-7150MJ can be tested. The testing environment is as follows:

Hardware

- PC having RS-232 serial port.
- EG-SR-7150MJ & Test board

Software

- Windows operating system installed on testing PC.
- EG-SR-7150MJ Configuration tool
- Hyper Terminal Program

Testing Structure

- Ethernet cross cable to connect the LAN ports of PC and EG-SR-7150MJ.
- RS-232 cable to connect the COM port of PC (usually COM1 or COM2) and serial port of EG-SR-7150MJ-EVB.

3.1. Case 1: Getting IP address using H/W trigger

STEP1: Configure the trigger mode as "H/W trigger" in the Configuration Tool.

STEP2: Check the serial port setting such as baud rate of the module.

STEP3: Start HyperTerminal program and set the serial port of PC to the setting of module checked in STEP2.

STEP4: Pull H/W trigger pin to low to enter the serial command mode.

STEP5: Use HyperTerminal program to send "**<RI>**" (command to request IP address)

STEP6: HyperTerminal program displays "**<S192.168.11.2>**"

(It indicates that the command was successfully executed and IP address is 192.168.11.2)

STEP7: Pull H/W trigger pin to high to exit the serial command mode

3.2. Case 2: Changing IP address using H/W trigger

STEP1: Configure the trigger mode as "H/W trigger" in the Configuration Tool.

STEP2: Check the serial port setting such as baud rate of the module.

STEP3: Start HyperTerminal program and set the serial port of PC to the setting of module checked in STEP2.

STEP4: Pull H/W trigger pin to low to enter serial command mode.

STEP5: Use HyperTerminal program to send "**<WI192.168.11.10>**"

(command to change the IP address as 192.168.11.10)

STEP6: HyperTerminal program displays "**<S>**"
(Indicates the command was successfully executed)

STEP7: Use HyperTerminal program to send "**<RI>**" (command to request IP address)

STEP8: HyperTerminal program displays "**<S192.168.11.10>**"
(Indicates the command was executed successfully and IP address is 192.168.11.10)

STEP9: Pull H/W trigger pin to high to exit serial command mode

☞ All changes are applied after exit the serial command mode

3.3. Case 3: Changing IP address using S/W trigger

STEP1: Configure the trigger mode as S/W trigger at the Configuration program, and check the three trigger characters. For example, assume the trigger is "25 25 25"

STEP2: Check the serial port setting such as baud rate of the module.

STEP3: Start HyperTerminal program and set the serial port of the PC to the serial setting of the module checked in STEP2.

STEP4: Use HyperTerminal program to send three trigger characters to enter the serial command mode; **%%%** (in hex :0x25 0x25 0x25) in this case.

STEP5: Use HyperTerminal program to send "**<WI192.168.11.10>**"
(command to change the IP address as 192.168.11.10)

STEP6: HyperTerminal program displays "**<S>**"
(Indicate the command was executed successfully)

STEP7: Use HyperTerminal program to send "**<RI>**" (command to request IP address)

STEP8: HyperTerminal program displays "**<S192.168.11.10>**"
(Indicate the command was executed successfully and IP address is 192.168.11.10)

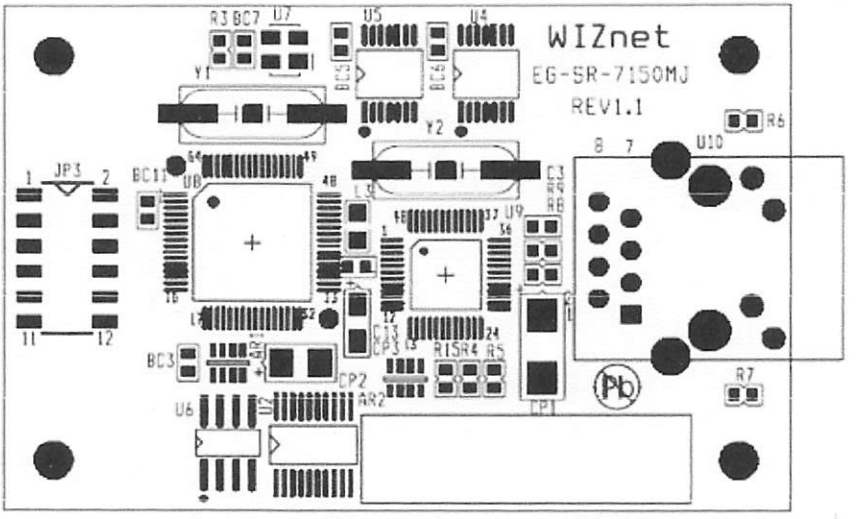
STEP9: Use HyperTerminal program to send "**<WR>**"
(command to exit serial command mode)

☞ All changes are applied after exiting the serial command mode.

4. PIN Assignment and Dimensions

JP3

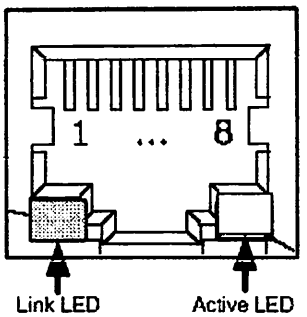
/RESET - 1 2 - 3.3V
RXD - 3 4 - 3.3V
CTS - 5 6 - /FACTORY_RESET
TXD - 7 8 - /HW_TRIGGER
RTS - 9 10 - /PSEN
GND - 11 12 - GND



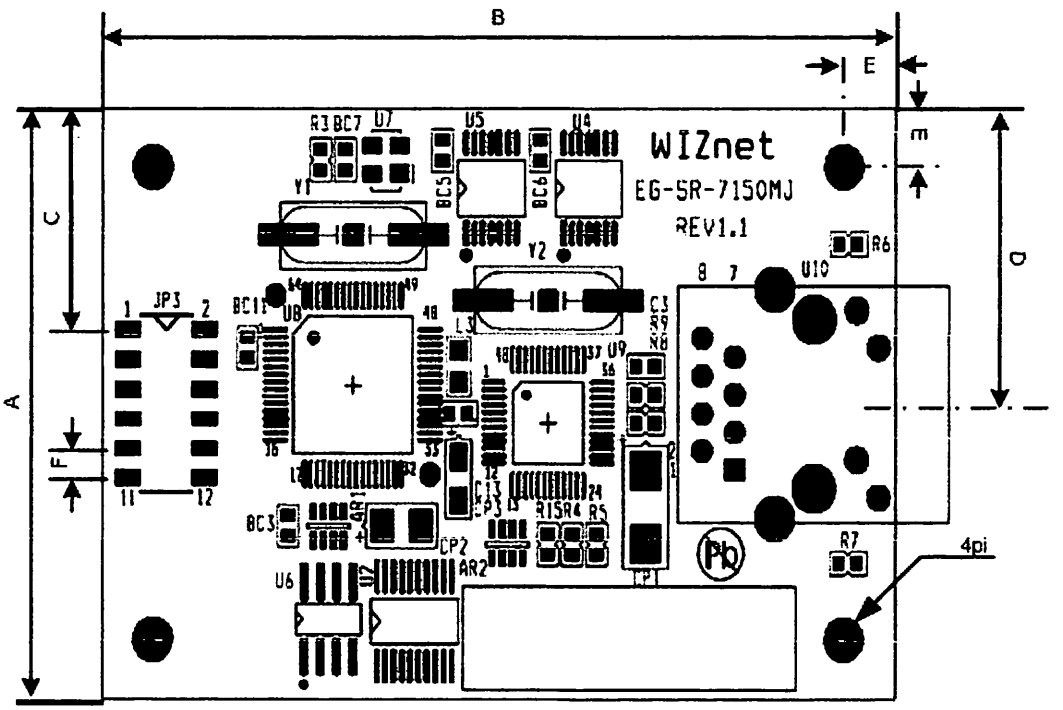
Name	Functions	I/O	
3.3V	Power		
/RESET	Low active reset Minimum 1.2 usec is required.	Input	
RXD	RS-232 Data Input	Input	
CTS	RS-232 Clear To Send	Input	Optional
TXD	RS-232 Data Output	Output	
RTS	RS-232 Request To Send	Output	Optional
Factory Reset	Pull Factory Reset to low and if /RESET is activated, the configuration is changed to factory default.	Input	
H/W Trigger	Pull H/W Trigger to low, enter the serial command mode	Input	
/PSEN	Pull /PSEN to low and if /RESET is activated, the module enter the bootloader for FLIP connection	Input	

☞ All signal levels are 3.3V LVTTL.

Ethernet port Pinouts

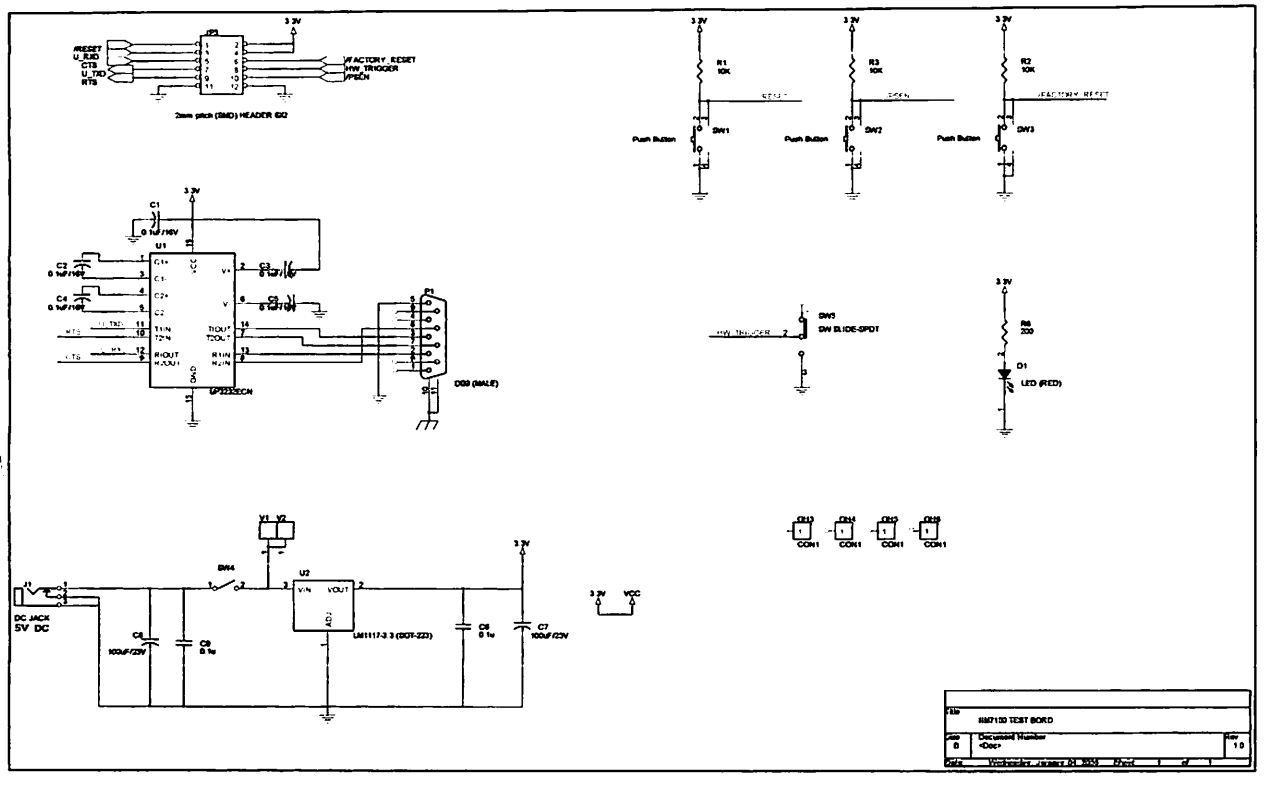


Pin	Signal
1	TX+
2	TX-
3	RX+
6	RX-



Symbol	Dimension(mm)
A	40
B	62
C	15
D	20
E	4
F	2

5. Reference Schematic



6. ETC

6.1. Firmware Uploading through the FLIP software

The following items are required to get started. :

- EG-SR-7150-MJ test board
- UART cross cable
- Program file in HEX file format
- FLIP utility installed on your PC

On a PC, one must have a file in HEX format to program the EG-SR-7150MJ. For example this file could be named "app.hex".

Step 1

Connect the EG-SR-7150MJ test board to a PC with the UART cable supplied.

Important : If you have any program running on your PC with which COM port is used such as "Hyperterminal", be sure to connect the cable to the COM port not used.

Step 2

Power on the test board.

While pressing the /PSEN button, click the /RESET button. Then release the /PSEN button

Step 3

Run the ISP software named FLIP by ATMEL.

Step 4

Select the device by pushing the F2 button. Here you must choose AT89C51RC2.

Step 5

Set up the communication port by pushing the F3 button. Make sure to select the same port as the one you have plug in the UART cable of the EG-SR-7150MJ test board.

Step 6

Now, you should be connected to the board and able to program.

Now you will have to browse your PC to load your file in hex format.

Step 7

After programming, check if the BSB, SBV and SSB are set as FF, 00 and FF respectively.

6.2. Warranty

WIZnet Co., Ltd offers the following limited warranties applicable only to the original purchaser. This offer is non-transferable.

WIZnet warrants our products and its parts against defects in materials and workmanship under normal use for period of standard ONE(1)YEAR for the EG-SR-7150MJ Module, Evaluation Board and labor warranty after the date of original retail purchase. During this period, WIZnet will repair or replace a defective products or part free of charge.

Warranty Conditions:

1. The warranty applies only to products distributed by WIZnet or our official distributors.
2. The warranty applies only to defects in material or workmanship as mentioned above in 6.2 Warranty. The warranty applies only to defects which occur during normal use

and does not extend to damage to products or parts which results from alternation, repair, modification, faulty installation or service by anyone other than someone authorized by WIZnet Inc. ; damage to products or parts caused by accident, abuse, or misuse, poor maintenance, mishandling, misapplication, or used in violation of instructions furnished by us ; damage occuring in shipment or any damage caused by an act of God, such as lightening or line surge.

Procedure for Obtaining Warranty Service

1. Contact an authorized distributors or dealer of WIZnet Inc. for obtaining an RMA (Return Merchandise Authorization) request form within the applicable warranty period.
2. Send the products to the distributors or dealers together with the completed RMA request form. All products returned for warranty must be carefully repackaged in the original packing materials.
3. Any service issue, please contact to sales@wiznet.co.kr

Features

- Compatible with MCS-51™ Products
- 8K Bytes of In-System Reprogrammable Downloadable Flash Memory
  - SPI Serial Interface for Program Downloading
  - Endurance: 1,000 Write/Erase Cycles
- 2K Bytes EEPROM
  - Endurance: 100,000 Write/Erase Cycles
- 4V to 6V Operating Range
- Fully Static Operation: 0 Hz to 24 MHz
- Three-level Program Memory Lock
- 256 x 8-bit Internal RAM
- 32 Programmable I/O Lines
- Three 16-bit Timer/Counters
- Nine Interrupt Sources
- Programmable UART Serial Channel
- SPI Serial Interface
- Low-power Idle and Power-down Modes
- Interrupt Recovery From Power-down
- Programmable Watchdog Timer
- Data Pointer
- Power-off Flag

Description

The AT89S8252 is a low-power, high-performance CMOS 8-bit microcomputer with 8K bytes of downloadable Flash programmable and erasable read only memory and 2K bytes of EEPROM. The device is manufactured using Atmel's high-density nonvolatile memory technology and is compatible with the industry-standard 80C51 instruction set and pinout. The on-chip downloadable Flash allows the program memory to be reprogrammed in-system through an SPI serial interface or by a conventional nonvolatile memory programmer. By combining a versatile 8-bit CPU with downloadable Flash on a monolithic chip, the Atmel AT89S8252 is a powerful microcomputer which provides a highly-flexible and cost-effective solution to many embedded control applications.

The AT89S8252 provides the following standard features: 8K bytes of downloadable Flash, 2K bytes of EEPROM, 256 bytes of RAM, 32 I/O lines, programmable watchdog timer, two data pointers, three 16-bit timer/counters, a six-vector two-level interrupt architecture, a full duplex serial port, on-chip oscillator, and clock circuitry. In addition, the AT89S8252 is designed with static logic for operation down to zero frequency and supports two software selectable power saving modes. The Idle Mode stops the CPU while allowing the RAM, timer/counters, serial port, and interrupt system to continue functioning. The Power-down mode saves the RAM contents but freezes the oscillator, disabling all other chip functions until the next interrupt or hardware reset.

The downloadable Flash can be changed a single byte at a time and is accessible through the SPI serial interface. Holding RESET active forces the SPI bus into a serial programming interface and allows the program memory to be written to or read from unless Lock Bit 2 has been activated.

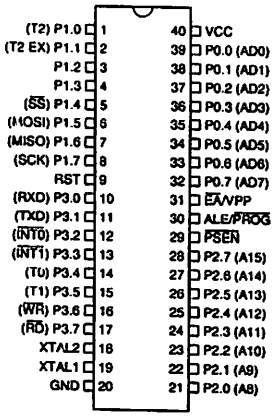
8-bit Microcontroller with 8K Bytes Flash

AT89S8252

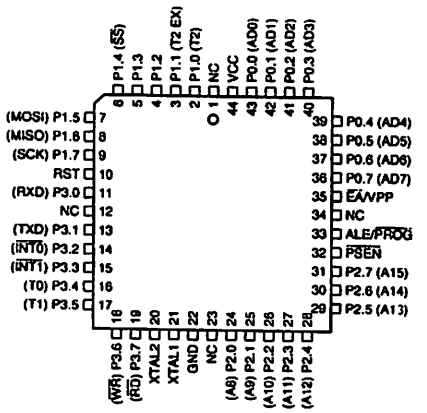
Rev. 0401E–02/00

Pin Configurations

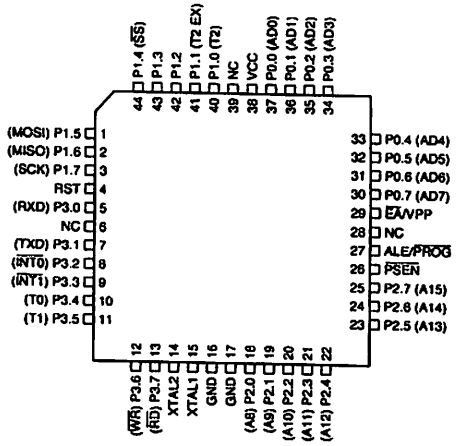
PDIP



PLCC



PQFP/TQFP



Pin Description

VCC

Supply voltage.

GND

Ground.

Port 0

Port 0 is an 8-bit open drain bbi-didirectional I/O port. As an output port, each pin can sink eight TTL inputs. When 1s are written to port 0 pins, the pins can be used as high-impedance inputs.

Port 0 can also be configured to be the multiplexed low-order address/data bus during accesses to external program and data memory. In this mode, P0 has internal pullups.

Port 0 also receives the code bytes during Flash programming and outputs the code bytes during program verification. External pullups are required during program verification.

Port 1

Port 1 is an 8-bit bi-directional I/O port with internal pullups. The Port 1 output buffers can sink/source four TTL inputs. When 1s are written to Port 1 pins, they are pulled high by the internal pullups and can be used as inputs. As inputs, Port 1 pins that are externally being pulled low will source current (I_{IL}) because of the internal pullups.

Block Diagram