INSTITUT TEKNOLOGI NASIONAL MALANG
FAKULTAS TEKNIK INDUSTRI
JURUSAN TEKNIK ELEKTRO S-1
Jl.Raya Karanglo Km. 2
Malang

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Tanggal : 23 maret 2009
Dengan Nilai : 75,6 (B+)

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PERANCANGAN DAN PEMBUATAN SISTEM AKUISISI DATA YANG DILENGKAPI DTMF (*Dual Tone Multiple Frequency*) DENGAN MEMAKAI DDS (*Direct Digital Synthesis*)

Disusun Oleh :

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JURUSAN TEKNIK ELEKTRO S-1
KONSENTRASI TEKNIK ELEKTRONIKA
FAKULTAS TEKNOLOGI INDUSTRI
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Dengan Memakai DI8S (Dzvv (Digital Switches)

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LEMBAR PERSETUJUAN

PERENCANAAN DAN PEMBUATAN SISTEM AKUISISI DATA YANG DILENGKAPI DTMF (*DUAL TONE MULTIPLE FREQUENCY*) DENGAN MEMAKAI DDS (*DIRECT DIGITAL SYNTHESIS*)

SKRIPSI

Disusun dan diajukan sebagai salah satu syarat untuk memperoleh gelar Sarjana Teknik Elektronika Strata Satu (S-1)

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JURUSAN TEKNIK ELEKTRO S-1
KONSENTRASI TEKNIK ELEKTRONIKA
FAKULTAS TEKNOLOGI INDUSTRI
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2009

ABSTRAK

Santo Rukmono Hadi, 2009. **Perencanaan dan pembuatan system akuisisi data menggunakan DTMF (*Dual Tone Multiple Frequency*) dengan memakai DDS (*Direct Digital Synthesis*).** Skripsi Jurusan Teknik Elektronika, Fakultas Teknik Industri, Institut Teknologi Industri. Dosen pembimbing: Ir.F.Yudi Limpraptono, MT dan Sotyohadi, ST

Perkembangan teknologi informasi dan elektronika saat ini berkembang pesat. Perkembangan ini dapat dilihat dengan banyaknya alat-alat komunikasi. Alat-alat komunikasi tersebut dalam menyampaikan data terkadang penyampaiannya tidak selalu dapat disampaikan ke tujuan dengan benar. Banyaknya gangguan seperti noise dalam penyampaian inilah yang terkadang menghambat penyampaian data.

Alat kontrol jarak jauh dinilai tepat membantu kita dalam menjalankan pekerjaan dengan lebih efisien, praktis dan nyaman. Dalam kehidupan sehari-hari sudah banyak dijumpai alat akuisisi data yang menggunakan bermacam-macam media komunikasi pada aplikasinya saluran telepon, seperti alat yang dibuat diatas yaitu perencanaan dan pembuatan alat sistem akuisisi data yang dilengkapi DTMF dengan memakai DDS.

KATA PENGANTAR

Alhamdulillah, dengan memanjatkan puji syukur kehadirat Allah SWT, yang telah memberikan rahmat, hidayah serta karunia-Nya, tak lupa sholawat dan salam kepada nabi Muhammad SAW. dan keluarganya, akhirnya penyusun dapat dapat menyelesaikan skripsi ini yang berjudul "Perencanaan dan pembuatan system akuisisi data menggunakan DTMF (*Dual Tone Multiple Frequency*) dengan memakai DDS (*Direct Digital Synthesis*), laporan skripsi ini merupakan salah satu persyaratan kelulusan Program Strata 1 Teknik Elektro Konsentrasi Elektronika Institut Teknologi Nasional Malang.

Keberhasilan penyusunan laporan skripsi ini tidak lepas dari dukungan dan bantuan berbagai pihak. Untuk itu penyusun menyampaikan terimakasih kepada:

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4. Bapak Ir. F. Yudi Limpraptono, MT. selaku Ketua Jurusan Teknik Elektro S-1 Institut Teknologi Nasional Malang serta sekaligus menjadi Dosen Pembimbing I
5. Bapak Sotyohadi, ST. selaku Dosen Pembimbing II

6. Teman-teman yang telah memberikan motifasi serta bantuan baik berupa tenaga maupun fikiran dalam proses penyelesaian skripsi ini.

Penyusun telah berusaha semaksimal mungkin dan menyadari sepenuhnya akan keterbatasan pengetahuan dalam penyelesaian laporan ini. Untuk itu penyusun mengharapkan saran dan kritik yang bersifat membangun demi kesempurnaan laporan ini.

Malang, Maret 2009

Penyusun

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DAFTAR GAMBAR

DAFTAR TABEL

BAB I

PENDAHULUAN

1.1. Latar Belakang

Perkembangan teknologi informasi dan elektronika saat ini berkembang pesat. Perkembangan ini dapat dilihat dengan banyaknya alat-alat komunikasi. Alat-alat komunikasi tersebut dalam menyampaikan data terkadang penyampaiannya tidak selalu dapat disampaikan ke tujuan dengan benar. Banyaknya gangguan seperti noise dalam penyampaian inilah yang terkadang menghambat penyampaian data.

Alat control jarak jauh dinilai tepat membantu kita dalam menjalankan pekerjaan dengan lebih efisien, praktis dan nyaman. Dalam kehidupan sehari-hari sudah banyak dijumpai alat akuisisi data yang menggunakan bermacam-macam media komunikasi pada aplikasinya saluran telepon, seperti alat yang dibuat diatas yaitu perencanaan dan pembuatan alat sistem akuisisi data yang dilengkapi DTMF dengan memakai DDS.

Dengan adanya alat yang dibuat maka akan terjaga kerahasiaan datanya dari kebocoran pada saat mengirim data memakai DTMF yang dilengkapi dengan sistem DDS.

1.2. Perumusan Masalah

Berdasarkan uraian pada latar belakang diatas, maka dalam skripsi ini dapat dirumuskan permasalahan sebagai berikut:

1. Mengetahui lebih dalam tentang DDS (*Direct digital synthesis*).

2. Mengetahui prinsip kerja DTMF (*Dual Tone Multyple Frequency*).
3. Bagaimana cara membuat alat sistem akuisisi data yang dilengkapi DTMF dengan memakai DDS.

1.3. Tujuan

Adapun tujuan yang ingin dicapai dalam skripsi ini adalah merancang dan membuat alat sistem akuisisi data yang dilengkapi DTMF dengan memakai DDS dan menampilkan hasil data ke dalam LCD.

1.4. Batasan Masalah

Agar pembahasan dari perencanaan dan pembuatan sistem akuisisi data yang dilengkapi DTMF (*Dual Tone Multi Frequency*) dengan memakai DDS (*direct digital synthesis*) tidak meluas maka perlu adanya pembatasan permasalahan yang meliputi :

1. Perangkat keras yang digunakan IC mikrokontroler AT89S51 dan IC MT8870.
2. Menggunakan DDS (*Direct digital synthesis*).
3. Memakai DAC menggunakan R2R.
4. Memakai ADC mengubah frekuensi analog ke digital.
5. Menggunakan DTMF (*Dual Tone Multi Frequency*) sebagai demodulator
6. Menggunakan LCD sebagai penampil data.

Batasan masalah yang akan dibahas pada skripsi ini menitikberatkan pada penggunaan DTMF dan DDS.

1.5. Metodologi Penelitian

Dalam penulisan skripsi ini penulis menggunakan metode-metode sebagai berikut:

1. Studi literatur yang berhubungan dengan perancangan dan pembuatan alat.
2. Perencanaan dan pembuatan alat sistem akuisisi data yang dilengkapi DTMF dengan memakai DDS.
3. Pelaksanaan uji coba alat sistem akuisisi data yang dilengkapi DTMF dengan memakai DDS.
4. Hasil dari data alat diperlihatkan lewat LCD.
5. Kesimpulan dari perencanaan dan pembuatan alat.

1.6. Sistematika Penulisan

Tugas akhir ini disusun berdasarkan sistematika penulisan sebagai berikut:

BAB I: Pendahuluan

Pada bab ini dibahas latar belakang masalah, perumusan masalah, batasan masalah, tujuan, metodologi pembahasan dan sistematika penulisan.

BAB II : Landasan Teori

Pada bab ini dibahas tentang teori-teori yang mendukung dalam perancangan dan pembuatan alat sistem akuisisi data yang dilengkapi DTMF (*Dual Tone Multi Frequency*) dengan memakai DDS (*direct digital synthesis*).

BAB III: Perancangan Dan Pembuatan Alat

Pada bab ini dibahas tentang perancangan dan pembuatan keseluruhan sistem akuisisi data dilengkapi DTMF memakai DDS.

BAB IV : Pengujian Alat

Pada bab ini akan dilakukan pengujian alat dari sistem akuisisi data dilengkapi DTMF memakai DDS dan memuat hasil dari pengujian alat ini.

BAB V : Penutup

Pada bab ini akan disampaikan kesimpulan dari perancangan dan pembuatan sistem ini.

BAB II

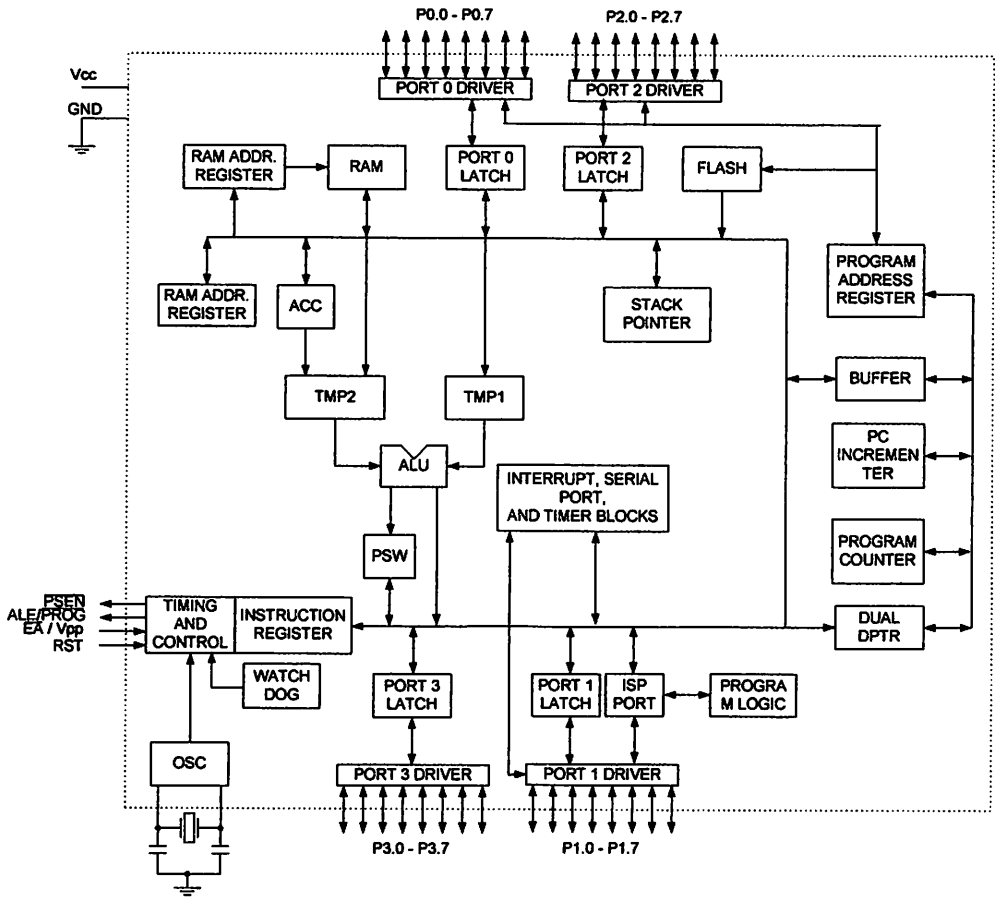
LANDASAN TEORI

2.1. Mikrokontroler AT89S52

Mikrokontroler AT89S52 merupakan IC mikrokontroler dengan konsumsi daya rendah dengan performansi tinggi dan *compatible* dengan produk MCS-52, memiliki struktur sebagai berikut :

1. 8 bit CPU (*central processing unit*) / merupakan mikrokontroler 8 bit.
2. 8 *Kbyte Flash Programmable And Erasable Read Only Memory* (PEROM).
3. 256 x 8 bit Internal RAM.
4. 32 pin I/O yang tersusun dalam 4 port (P0, P1, P2, P3) dengan setiap port terdiri dari 8 bit.
5. Memiliki 6 sumber interupsi.
6. 3 *Timer* / Counter 16 bit
7. *Full Duplex* serial port yang dapat diprogram.
8. *On Chip Oscilator.*
9. *Watchdog Timer*
10. Dual data pointer.
11. Flexible ISP Programming.

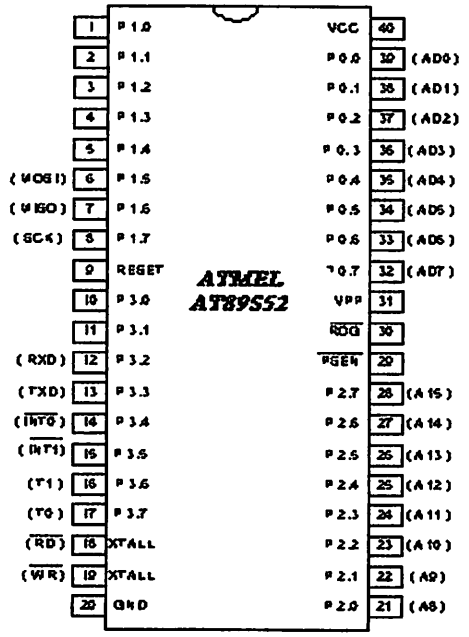
Secara lengkap struktur dari mikrokontroler AT89S52 dapat ditunjukan pada gambar 2.1:



Gambar 2.1 Blok Diagram Mikrokontroler AT89S52[1]

2.1.1. Definisi Pin Mikrokontroler AT89S52

Mikrokontroler AT89S52 memiliki 40 Pin yang didefinisikan seperti pada gambar 2.2:



Gambar 2.2 Konfigurasi pin AT89S52[1]

1. Vcc : Catu daya (supply tegangan).
2. Gnd : Ground.
3. Port 0 : Port 0 merupakan port 8 bit yang bersifat open drain dua arah. Sebagai port keluaran, tiap pin dapat menerima 8 masukan TTL. Saat logika 1 dituliskan pada port, pin port dapat digunakan sebagai masukan dengan impedansi tinggi.
4. Port 1: Port ini merupakan port I/O biderectional dengan internal pull-up. Out put Port ini dapat mendayai atau menerima 4 masukan TTL. Jika suatu logika 1 dituliskan pada port ini, maka port akan dibuat tinggi oleh *pull-up* internal dan dapat digunakan sebagai masukan. Pada saat sebagai port masukan, port ini akan dibuat rendah dan port ini akan mendayai karena adanya *pull-up* internal.

5. Port 2: Port ini merupakan port I/O biderectional dengan internal *pull-up*. Penyangga pada port ini mampu menangani 4 masukan TTL. Jika logika 1 dituliskan pada port ini, maka port akan dibuat tinggi oleh *pull-up* internalnya.
6. Port 3: Port ini merupakan port I/O bidirectional dengan internal *pull-up*. Out put Port ini dapat mendayai atau menerima 4 masukan TTL. Jika suatu logika 1 dituliskan pada port ini, maka port akan dibuat tinggi oleh *pull-up*. Selain sebagai port parallel port ini juga mempunyai fungsi khusus yaitu :

Tabel 2.1 Fungsi khusus Port 3[1]

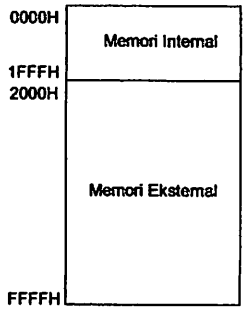
Port Pin	Fungsi Khusus
P3.0	RXD (masukan port serial (UART))
P3.1	TXD (keluaranan port serial (UART))
P3.2	INT0 (masukan interupsi luar 0)
P3.3	INT1 (masukan interupsi luar1)
P3.4	T0 (masukan luar Timer / Counter 0)
P3.5	T1 (masukan luar Tmer)
P3.6	WR (pulsa penulisan data memori luar)
P3.7	RD (pulsa pembacaan memori luar)

7. Reset: Masukan untuk reset. Suatu logika *high* selama dua siklus pada pin reset akan menyebabkan terjadinya proses reset.
8. ALE: *Addres latch enable* merupakan suatu pulsa keluaran untuk mengaitkan (*latch*) byte bawah dari alamat selama mengakses memori luar.
9. PSEN: Program *store enable* adalah pulsa pengaktif untuk membaca program memori luar. Saat Mikrokontroler melaksanakan instruksi dari program memori luar, PSEN akan diaktifkan dua kali siklus mesin, kecuali pada saat mengakses data memori luar.

10. EA/VPP: *External access enable*. EA harus dihubungkan dengan ground jika ingin mengakses dari program memori luar dengan alamat 0000H sampai FFFFH. EA harus dihubungkan ke V_{CC} jika menggunakan program memori internal.
11. XTAL1: Masukan untuk penguat inverting osilator dan masukan rangkaian *clock* internal.
12. XTAL2: Keluaran dari penguat inverting osilator.

2.1.2. Organisasi Memori

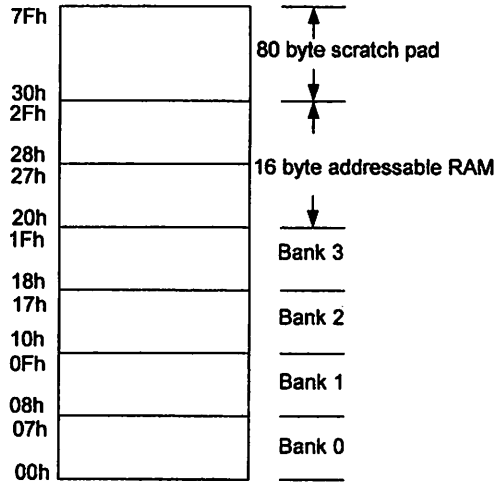
Didalam Mikrokontroler AT89S52 telah dibedakan antara program memori dan data memori. Untuk program memori AT89S52 mempunyai Flash memori internal (PEROM) dengan kapasitas 8 Kbyte, kapasitas ini bisa dinaikan menjadi maximal 64 Kbyte dengan menambah memori eksternal. Secara otomatis Mikrokontroler akan mengakses memori eksternal jika alamat progam (*address*) melebihi alamat 0FFFh. Organisasi memori AT89S52 dapat dilihat pada gambar 2.3:



Gambar 2.3 Organisasi Program Memori[1]

Sedangkan untuk data memori AT89S52 memiliki RAM internal yang berkapasitas 256 byte, kapasitas ini dapat dinaikan menjadi maximal 64 Kbyte

dengan menambah memori eksternal. Data memori dibagi menjadi dua bagian yaitu register khusus yang digunakan oleh mikrokontroler (SFR) dan register yang dapat dipakai oleh pengguna. RAM (*Random Access Memori*) merupakan memori yang bersifat mudah terhapus isinya jika aliran listrik diputus, karena itu RAM tidak digunakan untuk menyimpan program tetapi untuk menyimpan data sementara. Peta dari RAM internal pada MCS-52 dapat ditunjukan pada gambar 2.4:



Gambar 2.4 Peta memori RAM internal[1]

Pada gambar diatas terlihat bahwa RAM internal 256 byte terbagi menjadi beberapa bagian. Untuk alamat bawah yang pertama yaitu 00h sampai 7Fh sebanyak 128 byte yang terbagi dalam tiga besar berdasarkan kegunaanya yaitu :

a. Register Bank 0 – 3

- Lokasi register bank dimulai dari 00h – 1Fh terdiri dari 32 byte.

- Register bank ini terdiri dari empat buah register 8 bit yang dapat dipilih melalui pengaturan RS0 dan RS1 yang merupakan bit ke 3 dari program status *word register.*

b. Bit Addressable

- Lokasi register ini dimulai dari 20h – 2Fh
- Register ini bersifat *Addressable*, artinya bahwa perubahan dapat dilakukan per bit, tidak perlu per byte (8 bit). Fitur ini sangat berguna untuk meng-*on-off* kan suatu bit. Lokasi ini juga dapat dialamati secara langsung untuk 128 byte yang tersedia.

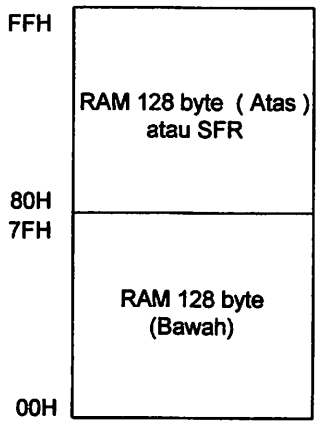
c. Scratch Pad

Lokasi register ini dimulai dari 30h – 7Fh yang digunakan untuk keperluan apa saja termasuk untuk alokasi stack pointer.

Tabel 2.2 Register Bank[1]

RS0	RS1	Register Bank	Address
0	0	0	00H - 07H
0	1	1	08H - 09H
1	0	2	10H - 17H
1	1	3	18H - 1FH

Setelah RAM 128 byte yang pertama, diatasnya diletakkan alamat untuk SFR (*Special Function Register*), perlu diingat bahwa RAM 256 byte atas sama dengan alamat SFR yaitu 80H – FFH, seperti ditunjukan pada gambar 2.5:



Gambar 2.5 Memori internal (RAM) dan SFR[1]

2.1.2.1.*Special Function register* (SFR)

SFR merupakan register dengan fungsi khusus. SFR pada mikrokontroler MCS-52 memiliki alamat 80H - FFH sehingga terdapat 256 lokasi untuk alamat SFR. Dari alamat-alamat ini hanya beberapa saja yang digunakan oleh SFR.

Tabel 2.3 Byte Special Function Register [1]

Simbol	Nama	Address
ACC	Accumulator	0E0H
B	B Register	0F0H
PSW	Program status Word	0D0H
SP	Stack Pointer	81H
DPTR	Data Pointer	
DPL	Low Byte	82H
DPH	High Byte	83H
P0	Port 0	80H
P1	Port 1	90H
P2	Port 2	0A0H
P3	Port 3	0B0H
IP	Interrupt Priority Control	0B8H
IE	Interrupt Enable Control	0A8H
TMOD	Timer/Counter Mode Control	89H
TCON	Timer/Counter Control	88H
TH0	Timer/Counter 0 High Control	8CH
TL0	Timer/Counter 0 Low Control	8AH

2.1.2.2.*Program status Word* (PSW)

Program status word berguna untuk memilih bank memori yang aktif, selain itu PSW juga memiliki kegunaan yang lain. Kegunaan lain itu dapat dilihat dari masing-masing bit penyusun PSW. PSW ini bersifat *bit-addressable* artinya bit-bitnya masing-masing dapat dirubah tanpa harus merubah satu kesatuan byte. Berikut adalah bit-bit penyusun PSW :

Posisi	PSW.7	PSW.6	PSW.5	PSW.4	PSW.3	PSW.2	PSW.1	PSW.0
Bit	CY	AC	F0	RS1	RS0	OV	-	P

Keterangan :

Bit CY : Bit *Carry Flag*

Bit AC : Bit *Auxiliary Carry Flag*

Bit F0 : Flag 0 untuk kegunaan umum

Bit RS1 : Bit pemilih bank memori

Bit RS0 : Bit pemilih bank memori

Bit OV : Bit *Overflow Flag*

Bit PAW.1 : Bit didefinisikan pemakai

Bit P : Bit Parity. Menunjukan jumlah bit 1 pada accumulator

2.1.2.3.*Power Control Register* (PCON)

Register Power Control beralamat di 87H berguna untuk mengatur kebutuhan daya mikrokontroler. Dengan adanya register pengatur daya ini memungkinkan mikrokontroler ke mode "*idle*" atau "*sleep*" yang mana akan

menghemat pemakaian daya. Selain itu ada bit-bit pada register PCON ini untuk mengatur *Baud Rate* pada serial port. Bit-bit pada PCON adalah sebagai berikut:

MSB							LSB
SMOD	-	-	-	GF1	GF0	PD	IDL

Keterangan :

Bit SMOD : Digunakan untuk membuat dobel (2 kali) baud rate pada timer 1

Bit - : Tidak digunakan, untuk pengembangan selanjutnya

Bit GF1 : Bit Flag serbaguna

Bit GF0 : Bit Flag serbaguna

Bit PD : Bit power down. Bila berlogika 1 mode power down aktif

Bit IDL : Bit idle mode. Aktif jika berlogika 1

2.1.2.4.Accumulator

Dari namanya dapat diketahui bahwa fungsi dari accumulator adalah pengumpul. SFR. Register ini merupakan register yang banyak dipakai. Untuk semua operasi aritmatika biasanya menggunakan/melibatkan accumulator. Alamat dari accumulator adalah E0H.

2.1.2.5.B Register

B Register beralamat di F0H. Register ini digunakan untuk operasi perkalian dan pembagian. Contoh instruksi yang menggunakan register ini adalah:
Mul AB ; kalikan isi pada accumulator dan pada B register

Div AB; membagi isi accumulator dengan isi B register, accumulator akan berisi hasil bagi dan B register akan berisi sisa pembagian.

2.1.2.6.*Stack Pointer* (SP)

Stack pointer adalah penunjuk *stack* yang memiliki alamat di 81H. Isi register ini mengindikasikan dimana nilai selanjutnya yang harus diambil oleh *stack* pada RAM internal. Jika anda memasukan (*PUSH*) suatu nilai ke *stack*, maka nilai tersebut akan dituliskan pada alamat SP+1 (alamat SP ditambah satu). Jika SP berisi 07H kemudian suatu instruksi *PUSH* dijalankan, maka nilai yang dimasukan akan dituliskan pada alamat 08H. Nilai *default* untuk *stack pointer* adalah berada pada alamat 07H.

2.1.2.7.Data *Pointer* (DPTR)

Data *Pointer* (DPTR) yang berukuran 16 bit terdiri dari dua register yaitu DPL (Data *Pointer Low* byte) yang beralamat di 82H dan DPH (Data *Pointer High* byte) yang beralamat di 83H. Data *Pointer* digunakan untuk membentuk alamat berukuran 16 bit untuk mengakses memori luar.

2.1.3. *Timer/Counter*

Pada mikrokontroler keluarga MCS-52 terdapat dua buah *Timer/Counter*. Dengan adanya *timer/counter* menambah fungsionalitas dari mikrokontroler ini. Sebagaimana peralatan lain pada mikrokontroler ini, *timer/counter* juga diatur oleh SFR (*Special Function Register*) yaitu *Timer/Counter Control* (TCON alamat 88H), dan *Timer/Counter Mode Control* (TMOD alamat 89H). Selain itu

nilai byte bawah dan byte atas dari *Timer/Counter* disimpan dalam register TL dan TH. Jika difungsikan sebagai timer maka akan menggunakan sistem *clock* sebagai sumber masukan pulsanya, kemudian jika difungsikan sebagai *counter* (penghitung) maka akan menggunakan pulsa dari eksternal sebagai masukan pulsanya. Sebagaimana diketahui port 3 pada fungsi khususnya terdapat T0 (masukan luar untuk *Timer/Counte* 0) dan T1 (masukan luar untuk *Timer/Counter*1).

2.1.3.1.Register TMOD

Register TMOD dibagi menjadi 2 bagian secara simetris, yaitu bit 0 – 3 register TMOD (TMOD bit 0..TMOD bit 3) dipakai untuk mengatur timer 0, dan bit 4 sampai 7 register TMOD (TMOD bit 4..TMOD bit 7) dipakai untuk mengatur timer 1, susunan bit dapat dilihat dibawah ini :

MSB LSB

Timer/Counter 1				Timer/Counter 0			
GATE	C/T	M1	M0	GATE	C/T	M1	M0

Keterangan :

Bit GATE = Jika bit ini diset timer akan berjalan hanya jika INT1 (P3.3) sedang tinggi. Jika bit ini diclear timer akan berjalan tanpa mempertimbangkan kondisi INT1.

Bit C/T = Saat bit ini diset *timer* akan menghitung kejadian pada T1 (P3.5) sebagai fungsi *counter*. Jika bit ini di*clear* maka *timer* akan menghitung tiap siklus mesin (sebagai fungsi *timer*).

Bit M0 dan M1 bit *mode Timer/Counter*

Tabel 2.4 Bit pemilih mode *timer*

M1	M0	Timer Mode	Keterangan
0	0	0	13 bit timer
0	1	1	16 bit timer
1	0	2	8 bit auto reload
1	1	3	split mode

2.1.3.2.Register TCON

Register TMOD dibagi menjadi 2 bagian secara simetris, bit 0 sampai 3 register TMOD (TMOD bit 0 .. TMOD bit 3) dipakai untuk mengatur Timer 0, bit 4 sampai bit 7 register TMOD (TMOD bit 4 .. TMOD bit 7) dipakai untuk mengatur timer 1, susunan bit dapat dilihat dibawah ini :

MSB							LSB
bit 7	bit 6	bit 5	bit 4	bit 3	bit2	bit 1	bit 0
TF1	TR1	TF0	TR0	IE1	IT1	IE0	IT0

Keterangan :

Bit (7) TF1 = *Timer* 1 *overflow*, diset oleh Mikrokontroler jika hitungan timer 1 melimpah (*overflow*).

Bit (6) TR1 = *Timer* 1 *Run*, jika bit ini diset maka timer 1 on, jika bit ini di*clear* maka *timer* 1 *off*.

Bit (5) TF0 = *Timer* 0 *overflow*, bit ini diset oleh Mikrokontroler saat *timer* 0 melimpah.

Bit (4) TR0 = *Timer* 0 *Run*, jika bit ini diset maka *timer* 0 on, jika di*clear* maka *timer* 0 *off*.

Bit (3) IE1 = *Interupt* 1 *edge flag*. Diset oleh *hardware* jika sisi suatu sela luar terdeteksi. Di*clear* jika instruksi RET1 dijalankan.

Bit (2) IT1 = *Interupt* 1 type. Berhubungan dengan sela luar 1. Fungsinya sama dengan IT0.

Bit (1) IE0 = *Interupt* 0 *edge flag*. Diset oleh *hardware* jika sisi suatu sela luar terdeteksi. Di*clear* jika instruksi RET1 dijalankan.

Bit (0) IT0 = *Interupt* 0 type. Sela luar 0 diterima melalui bit 2 pada port 3. Jika bit ini diset, maka INT0 dikenali pada sisi turun sinyal. Jika bit ini di*clear* maka suatu sela akan dikenali pada saat suatu sinyal *low*.

2.1.4. Metode Pengalamatan

Metode pengalamatan dengan menggunakan bahasa pemrograman *assembler* pada Mikrokontroler keluarga MCS-52 adalah sebagai berikut:

a. Pengalamatan Tak Langsung

Operand pengalamatan tak langsung menunjuk kearah sebuah register yang berisi lokasi alamat memori yang akan digunakan didalam operasi. Lokasi yang nyata tergantung pada isi register saat instruksi dijalankan. Untuk melaksanakan pengalamatan tak langsung digunakan simbol @.

ADD A,@R0 ; Tambahkan isi RAM yang lokasinya; ditunjukan oleh register R0 ke Accumulator

DEC @R1; Kurangi satu isi Ram yang alamatnya; oleh register R1

MOVX @DPTR,A; Pindahkan isi dari accumulator ke memori luar; yang lokasinya ditunjukkan oleh data pointer

b. Pengalamatan Langsung

Pengalamatan langsung dilakukan dengan memberikan nilai ke suatu register secara langsung. Untuk melaksanakannya digunakan tanda #.

MOV A,#01H ; Isi accumulator dengan bilangan 01H.

MOV DPTR,#20CDH ; Isi register DPTR dengan bilangan 20CDH.

Pengalamatan data langsung dari 0 sampai dengan 127 akan mengakses RAM internal, sedangkan pengalamatan dari 128 sampai 255 akan mengakses register perangkat keras.

MOV P3,A ; Pindahkan isi accumualtor ke alamat data.

B0H ; (B0H adalah alamat port 3).

INC 60 ; Naikkan lokasi 60 (desimal) menjadi bernilai *high*.

c. Pengalamatan Bit.

Pengalamatan bit adalah penunjukan alamat lokasi bit baik dalam lokasi RAM internal (byte 32 sampai 37) maupun bit perangkat keras. Untuk melakukan pengalamatan bit digunakan simbol titik (.),

SET P1.3 ; Ubah bit ke 3 pada port 1 menjadi bernilai *high*

d. Pengalamatan Kode

Terdapat tiga macam yang dibutuhkan dalam pengalamatan kode, yaitu relative jump, in-block jump atau call dan long jump.

2.2. ADC (*Analog Digital Converter*) 0804

Agar dapat mengukur atau mengolah suatu variabel fisik yang umumnya dalam besaran analog dengan piranti digital, variabel tersebut harus diubah dahulu menjadi variabel digital yang nilainya proporsional dengan nilai variabel yang akan diukur atau diolah. Konversi ini dilakukan oleh konverter analog ke digital, ADC (*Analog to Digital Converter*).

Resolusi ADC didefinisikan sebagai *voltage input* yang diperlukan untuk 1 bit *output* dan dapat dinyatakan dengan persamaan berikut :

$$\text{Res} = \frac{\mathbf{E}}{\mathbf{2^N - 1}}$$

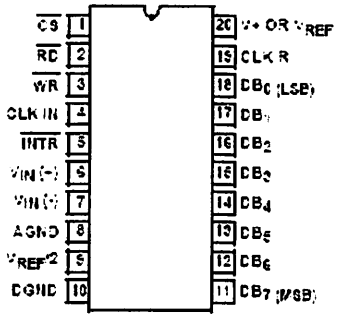
Atau jika dinyatakan dalam % Resolusi :

$$\%\ \text{Res} = \frac{\mathbf{E}}{\mathbf{2^N - 1}} \text{ x } 100\ \%$$

Resolusi ADC mengacu pada jumlah bit dalam keluaran biner ADC. Resolusi ADC 8-bit sama dengan $\left(\frac{\text{I}}{255}\right)$ x 100 %.

Spesifikasi penting selain ketelitian (akurasi) dan linearitas adalah waktu konversi (*converse time*). Waktu konversi ADC adalah waktu yang diperlukan ADC untuk menghasilkan kode biner yang valid untuk tegangan masukan yang diberikan. Semakin pendek waktu konversi, maka kecepatan konverter itu semakin tinggi. ADC yang banyak digunakan adalah :

1. *Counting* atau *Counter* ADC
2. *Successive Approximation* ADC (SAC)
3. *Paralel-Comparatoe* atau flash ADC
4. *Dual slope* atau ratiometrik ADC



Gambar 2.6 Konfigurasi PIN ADC 0804[2]

Fitur ADC 0804 :

- Kompatibel dengan mikroprosesor atau mikrokontroller tanpa memerlukan rangkaian *interfacing.*
- Dapat beroperasi dalam mode *stand alone* atau diinterfacekan ke mikroprosesor atau mikrokontroller
- Input tegangan analog yang differensial
- Generator clock on chip
- Tegangan input analog 0-5 V

Spesifikasi :

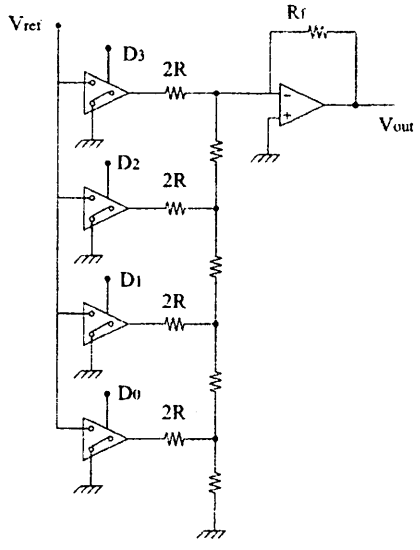
- Resolusi 8 bit
- Error total ± 1 LSB
- Waktu konversi 100 µs
- Supply tegangan 5 V
- Bekerja pada temperatur 0° C sampai 70° C

2.3. DAC R2R.

DAC digunakan untuk mengkonversi data digital menjadi sinyal analog. Pada umumnya semua bentuk konverter digital ke analog akan menghasilkan

suatu keluaran yang berupa arus dan tegangan yang merupakan bentuk hasil perkalian antara tegangan analog referensi dengan data digital tertentu (*Multiplying D/A Converter*).

Karena konverter digital ke analog ini banyak macamnya, maka pada umumnya dipakai cara konversi dengan rangkaian resistor berbobot (*binary weighted resistor*) dimana posisi dari bit digital yang akan diberikan akan menghasilkan besar arus tegangan yang sesuai bobot biner pada data digital. Didalam penerapannya, cara pemakaian harga tahanan yang bervariasi akan menimbulkan kesulitan dalam memilih harga tahanan yang sesuai, sehingga dipakai rangkaian tangga tahanan R2R yang lebih sederhana.



Gambar 2.7 Rangkaian DAC dengan R-2R Ladder[3]

Tahanan keluaran Vout dapat dihitung dengan rumus berikut :

$$\text{Vout} = -\frac{Rf}{R} Vref\left(\frac{D_0}{2^n} + \frac{D_1}{2^{n-1}} + \frac{D_2}{2^{n-2}}\right) - \left(\frac{D_{(n-2)}}{2^2} + \frac{D_{(n-1)}}{2^1}\right)$$

Dimana : $D_0 ... D_1$ = bernilai 1 atau 0

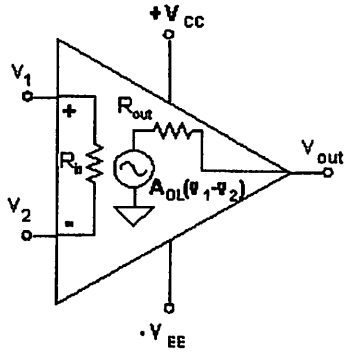
n = banyaknya bit masukan

Vref = tegangan referensi

2.4. Penguat (Op-Amp)

Amplifier atau lazim disebut penguat dalam suatu rangkaian dapat difungsikan dalam suatu rangkaian penguat sinyal input, rangkaian penjumlahan tegangan input, rangkaian pembanding antara 2 sinyal input, rangkaian filter dan masih banyak lagi.

Rangkaian penguat ini sangat sederhana dalam pemakaianya baik secara merangkaianya maupun dalam penggunaanya. Rangkaian ini terdiri dari kombinasi antara pengutan operasional yang dirangkai bersama kompenen pasif tahanan atau kondensator. Dengan kombinasi ini dapat dikembangkan lagi menjadi rangkaian yang mempunyai spesifikasi khusus seperti rangkaian instrumentasi, rangkaian isolator, dan lain sebagaianya. Gambar 2.8 menunjukan simbol dari op-amp dengan lima terminal dasar terdiri dari 2 terminal catu daya, 2 terminal input atau masukan yaitu (+) dan (-) dan terminal *output* atau keluaran dari op-amp



Gambar 2.8. Simbol Op-Amplifier[4]

2.5. DTMF (*Dual Tone Multiple Frequency*)

DTMF (*Dual Tone Multiple Frequency*) merupakan metode yang paling banyak digunakan dalam bidang telekomunikasi.sebagaian besar industri telekomunikasi manggunakan sistem DTMF sebagai *tone* dialer karena lebih efisiensi dan memberikan kecepatan dalam melakukan *dialing*. Dalam perkembangannya, pensinyalannya DTMF tidak saja digunakan untuk sistem *dialing* saja namun akan digunakan untuk sistem komunikasi data, pengendali jarak jauh melalui telepon, mesin penjawab telepon dan lain-lain.

DTMF menggunakan 16 buah audio frekuensi yang merupakan sistem sinyal frekuensi ganda. Dalam sistem ini, sebuah frekuensi tersusun atas sebuah kombinasi dari 2 buah audio frekuensi, yaitu *low* group dan hig group,yang dipilih satu demi satu pada tiap frekuensi (lebih tinggi atau lebih rendah) yang membentuk sebuah pasangan nada. penekanan masing-masing *keypad* akan dialokasikan dan dihubungkan dengan sebuah angka atau kode. Alokasi frekuensi DTMF seperti ditujukkan pada tabel berikut ini :

Tabel 2.5 Alokasi frekuensi DTMF[5]

Low frequency (Hz)	High frequency (Hz)			
	1209	1336	1477	1633
697	1	2	3	A
770	4	5	6	B
852	7	8	9	C
941	#	0	*	D

Dari tabel 2.5 dapat di baca bahwa setiap penekanan tombol di pesawat telepon, telpon akan membangkitkan dua nada (*tone*) yaitu nada berfrekwensi tinggi dan satu nada berfrekwensi rendah. Kedua sinyal tersebut dikirimkan ke penerima.

2.5.1 Rangkaian DTMF Decoder

Untuk menangkap tombol apa yang ditekan oleh penelepon maka peranti pertama yang harus disediakan adalah peranti yang bertugas mendeteksi sinyal apa yang dikirimkan. Jika sinyal yang dikirimkan bukan sinyal bicara melainkan sinyal yang dikarenakan penekanan tombol telepon maka dapat digunakan tabel 2.5 untuk melakukan pendekode-an. Untuk itu diperlukan sebuah rangkaian elektronik yang mendapat masukan dari kabel telepon dan keluaran bilangan hasil pendekodean sinyal tersebut.

Jika dilihat tombol tombol yang di kodekan ada 16 buah, digunakan 2 buah nada dengan variasi nilai masing masing nada 4 nilai. Keluaran dari rangkaian ini yang diharapkan adalah bilangan biner 4 digit. Dari tabel 2.5 dapat

di buat tabel 2.6 dibawah ini yang menunjukan konversi masukan menjadi keluaran. Karena ada 16 buah keluaran sebetulnya keluran ini jika dilambangkan dengan bilangan biner dapat diwakili dengan 4 bit bilangan biner dari 0000 sampai dengan 1111.

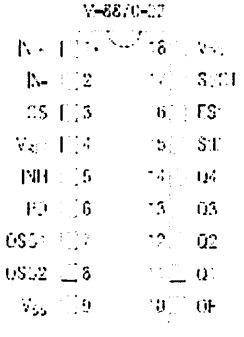
Tabel 2.6 Fungsi Transfer dari input menjadi *output*[5]

Frekwensi rendah	Frekwensi Tinggi	Tombol yang ditekan
679 Hz	1209 Hz	1
679 Hz	1366 Hz	2
679 Hz	1477 Hz	3
679 Hz	1633 Hz	A
770 Hz	1209 Hz	4
770 Hz	1366 Hz	5
770 Hz	1477 Hz	6
770 Hz	1633 Hz	B
852 Hz	1209 Hz	7
852 Hz	1366 Hz	8
852 Hz	1477 Hz	9
852 Hz	1633 Hz	C
941 Hz	1209 Hz	*
941 Hz	1366 Hz	0
941 Hz	1477 Hz	#
941 Hz	1633 Hz	D

Untuk keperluan mendekode masukan tersebut diperlukan sebuah peranti elektronika dengan masukan sinyal telepon dan keluaran logika 4 bit. Untuk keperluan ini dapat digunakan salah satu produk IC *Dual Tone Multiple Frquencies Dekoder* yaitu MT8770 produk MITEL.

2.6 Microkontroller MT8870

Dekoder DTMF MT8870, Decoder DTMF merupakan rangkaian yang dapat menghasilkan kode biner dari sinyal DTMF. Untuk kebutuhan tersebut, untuk saat ini dipasaran telah tersedia rangkaian DTMF dalam bentuk IC (*integrated circuit*). Salah satunya adalah produksi MITEL, yaitu MT8870. DTMF MT8870 mempunyai bentuk yang kecil, berdaya rendah, dapat diandalkan, dan dapat dioperasikan pada suhu -40 C sampai 80 C.



Gambar 2.9 Konfigurasi pin IC MT 8870[5]

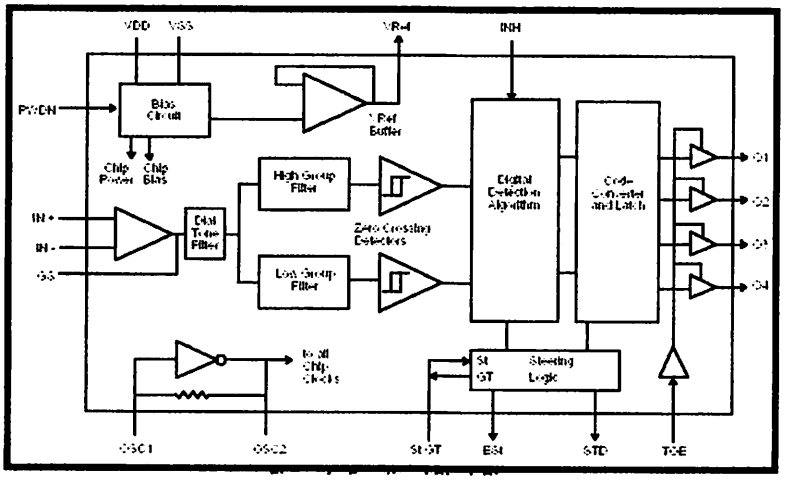
Decoder ini mengkodekan sinyal– sinyal DTMF menjadi kode biner (*binary code*) 4 bit. Decoder ini telah dilengkapi dengan filter untuk frekuensi tinggi (*high frequency*) dan frekuensi rendah (*low frequency*) serta sebuah digital decoder. Filter menggunakan *switched capacitor* untuk membedakan frekuensi yang masuk, sedang decoder menggunakan teknik pencacahan (*counting techniques*)

secara digital untuk mendeteksi dan mengkodekan 16 buah pasangan frekuensi DTMF menjdai kode biner 4 bit. Selain itu, MT8870 juga dilengkapi dengn rangkaian internal penguat differential, *oscillator clock*,dan sebuah rangkaian latch 3 state pada bagian *output*.dengan demikian rangkaian external tambahan untuk membentuk sebuah decoder DTMF yang lengkap dapat dikurangi.

Tabel 2.7 Konfigurasi tone dialing dan angka[5]

Dial code	*Input frequency (Hz)*	*DTMF decoder output*			
		Q4	Q3	Q2	Q1
1	1209 – 697	0	0	0	1
2	1336 – 697	0	0	1	0
3	1477 – 697	0	0	1	1
4	1209 – 770	0	1	0	0
5	1336 – 770	0	1	0	1
6	1477 – 770	0	1	1	0
7	1209 – 852	0	1	1	1
8	1336 – 852	1	0	0	0
9	1477 – 852	1	0	0	1
0	1633 – 941	1	0	1	0
*	1209 – 941	1	0	1	1
#	1477 – 941	1	1	0	0
A	1633 – 697	1	1	0	1
B	1633 – 770	1	1	1	0
C	1633 – 852	1	1	1	1
D	1633 – 941	0	0	0	0

Block diagram dari decoder MT8870 adalah sebagai berikut :



Gambar 2.10 Diagram blok IC MT8770[5]

Fungsi masing-masing kaki *decoder* MT 8870 adlah sebagai berikut :

1. Non Inverting OP – AMP (IN +)

   Sinyal dimasukan ke kaki ini apabila tidak diperlukan pembalikan fase.

2. Inverting OP – AMP (IN -)

   Sinyal dimasukan ke kaki ini apabila diperlukan pembalikan fase.

3. Gain select (GS)

   Kaki ini diperlukan untuk pemilihan penguatan sinyal. Apabila diperlukan penguatan, maka diperlukan sebuah resistor yang dihubungkan ke kaki ini.

4. Vref

   Tegangan referensai nominal $^1/_2$ VDD digunakansebagai input bias.

5. Inhid (INH)

   Digunakan dalam mendeteksi nada yang diwakili karakter A, B, C dan D.

6. Power Down (PD)

   Logika high diberikan pada saat menerima sinyal (standbay mode)

7. OSC1

   Kaki ini sebagai masukan dari crystal oscillator. Nilai crytal yang digunakan sebesar 3,579545 Mhz.

8. OSC2

   Kaki ini sebagai keluaran dari crytal oscillator.

9. Ground (Vss)

10. Three State *Output* Enable (TOE)

    Kaki ini berfungsi untuk mengendalikan data keluaran Q1, Q2, Q3, dan Q4. Bila kaki ini diberikan logika high, maka akan mengeluarkan data.

11. Q1 – Q4

    Output data 4 bit.

12. Delayed Steering (StD)

    Bila masukan mendeteksi nada – nada DTMF, maka kaki ini akan memberikan logika high dan sebaliknya.

13. Early Steering (Est)

    Kaki ini akan mengeluarkan logika high apabila bagian digital algoritma pasangan nada – nada DTMF (sinyal kondisi). Bila sinyal kondisi tersebut hilang seketika, maka akan menyebabkan Est berlogika low.

14. Steering Input / Guard Biderectional (St/GT)

    Jika tegangan yang terdeteksi oleh St lebih besar daripada tegangan VTSt, maka menyebabkan pasangan nada yang terdeteksi untuk dicatat dan dilakukan penguncian keluaran yang terbaru. Jika tegangn yang dideteksi lebih kecil maka akan bebas menerima pasangan nada yang baru.

15. Power Supply (VDD)

    Kaki ini dihubungkan ke sumber tegangan 5 Volt.

IC MT 8870 memerlukan komponen luar untuk menerima nada – nada DTMF. Komponen tersebut untuk penguat masukan, oscillator clock, dan rangkaian kendali.

Nilai R3 yang digunakan dalam penguat ditentukan dengan persamaan :

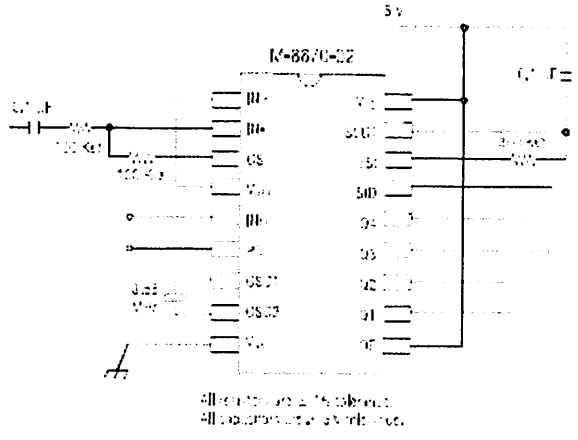
$$R3 = \frac{R2 \cdot R5}{R2 + R5} \quad \text{..... (i)}$$

Sedangkan penguatan tegangan dihitung dengan persamaan :

$$\text{Av diff} = \frac{R5}{R1} \quad \text{..... (ii)}$$

Dimana : Avdiff = penguatan tegangan (kali).

Rangkaian oscillator sudah ada dalam IC ini secara internal, sehingga hanya memerlukan 1 komponen external, yaitu berupa crystal oscillator yang dipasang anatara kaki 7 dan kaki 8. Crytal yang digunakan bernilai 3,579545 Mhz.Rangkaian kendali berfungsi untuk mengendalikan *output* stD.



Gambar 2.12 Rangkaian dasar kendali[5]

Logika high pada Est menyebabkan tegangan VC2 naik dan apabila logika pada ESt kembali rendah kembali rendah, maka akan membuat tegangan VC2 turun.

2.7. Sistem DDS (*Direct digital synthesis*)

Sistem DDS (*Direct digital synthesis*) merupakan salah satu cara untuk menghasilkan sinyal sinusoida secara langsung. Inti dari sistem ini adalah arsitektur akumulator dengan resolusi mencapai mili Hertz dan frekuensi sinyal yang dihasilkan dapat diatur tergantung dari sinyal frekuesi referensi dan metode perancangan. Keluaran sistem DDS yang diproses oleh mikrokontroler berupa

arsitektur akumulator dengan resolusi mencapai mili Hertz dan frekuensi sinyal yang dihasilkan dapat diatur tergantung dari sinyal frekuesi referensi dan metode perancangan. Keluaran sistem DDS yang diproses oleh mikrokontroler berupa sinyal digital kemudian menjadi masukan untuk DAC (D/A converter) dan LPF (Low Pass Filter) untuk menghasilkan sinyal sinusoida yang sempurna.

Semua parameter kontrol sistem DDS berada dalam bentuk digital. Sistem DDS pada dasarnya terdiri atas akumulator phasa, LUT (Look Up Table), dan osilator sebagai pembangkit frekuensi referensi (clock). Sedangkan DAC (Digital To Analog Converter) dan LPF (Low Pass Filter) merupakan komponen–komponen penunjang sistem DDS

2.7.1 Kelebihan Dan Flesibilitas DDS

Kelebihan penggunaan Sistem DDS adalah karakteristik sistem DDS itu sendiri, dimana keutamaan dari sistem ini adalah memiliki setting time/kecepatan yang cepat dan memiliki resulusi frekuensi yang halus terhadap frekuensi keluaran, operasi atas suatu sepektrum frekuensi yang lebar dan dengan kemajuan dalam desain teknologi proses. Serta sangat ringkas dan sedikit membutuhkan daya. Sehingga sangat memungkinkan sistem DDS bisa lebih dikembangkan untuk desain alat yang berkaitan dengan aplikasi-aplikasi frekuensi hopping serta sistem-sistem yang berkaitan dengan peralatan pemancar radio,TV,peralatan test, dll.

Figure 1-4. Signal flow through the DDS architecture

Gambar 2.13 Signal Sinusoida *Direct digital synthesis* (DDS)[6]

2.8 LCD (Liquid Crystal Display)

Merupakan komponen optoelektronik yaitu komponen yang bekerja atau dipengaruhi oleh sinar (optolistirk), komponen pembangkit cahaya (*Light Emiting*) dan komponen – komponen yang akan mengubah sinar. LCD terbuat dari bahan Kristal cair yang merupakan suatu komponen oraganik dan mempunyai sifat optik seperti benda padat meskipun bahan tetap cair.

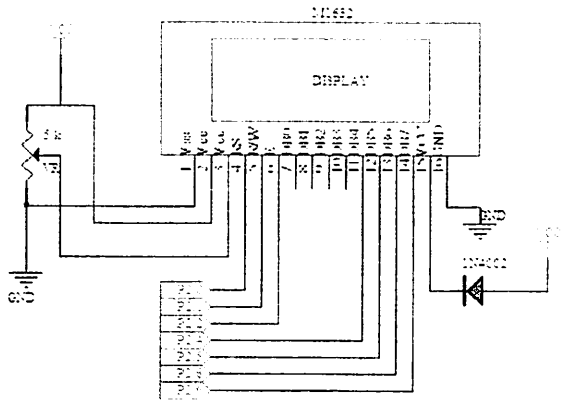
Sel Kristal cair terdiri dari selapis bahan Kristal cair yang diapit antara dua kaca tipis yang transparan. Antara dua lembar kaca tersebut diberi bahan Kristal cair (*liquid crystal*) yang tembus cahaya. Permukaan luar dari masing – masing keeping kaca mempunyai lapisan penghantar tembus cahaya seperti oxide timah (*tin oxide*) atau oxide indium (*indium oxide*). Sel mempunyai ketebalan sekitar 1 x 10^{-5} meter dan diisi dengan crstal cair.

Karena sel – sel kristal cair merefleksikan cahaya dan bulan membangkitkan cahaya maka konsumsi daya yang dibutuhkan relatif rendah. Energi yang dipergunakan hanya untuk mengaktifkan kristal cair. Pada dasarnya LCD bekerja pada tegangan rendah (13 – 15 Vrms), frekuensi rendah (25 – 60 Hz) sinyal AC dan memakai arus listrik yang sangat kecil (25 – 300 μA). LCD sering kali ditata sebagai tampilan *seven segment* untuk menampilkan angka tetapi

juga memiliki keistimewaan lain yaitu, kemampuan untuk menampilkan karakter dan berbagai macam simbol.

Salah satu jenis LCD diantaranya adalah LCD M1632. Suatu jenis piranti dengan konsumsi daya yang rendah, disusun dari dot matrik dan dikontrol oleh ROM atau RAM generator karakter dan RAM data display. Pengontrolan utamanya adalah pada ROM generator dan display data RAM yang menghasilkan kode ASCH jika padanya diberikan input ASCH. Untuk dapat difungsikan dengan baik maka perlu diperhatikan proses analisasi yang telah ditentukan oleh pabrik pembuatannya. Timing penganalisasian sangat dipertimbangkan, karena jika melesat sampai ordo*/milisecon* maka dapat dipastikan LCD tidak dapat berfungsi.

LCD Display Module M1632 buatan Seiko Instrument Inc. ini terdiri dari dua bagian, yang pertama merupakan panel LCD sebagai media penampil informasi dalam bentuk huruf/angka dua baris, masing – masing baris bisa menampung 16 huruf/angka. Bagian kedua merupakan sebuah sistem yang dibentuk dengan mikrokontroler yang ditempelkan dibalik pada panel LCD, berfungsi mengatur tampilan informasi serta berfungsi mengatur komunikasi M1632 dengan mikrokontroler yang memakai tampilan LCD itu. Dengan demikian pemakaian M1632 menjadi sederhana, sistem lain yang M1632 cukup mengirimkan kode – kode ASCH dari informasi yang ditampilkan seperti layaknya memakai sebuah printer.



Gambar 2.14. Rangkaian LCD M1632[7]

Adapun karekteristik dari LCD M1632 antara lain :

- Dengan 16 karakter – 2 baris dalam bentuk dotmatrik 5x7 dan cursor
- *Duty ratio* 1/16
- Memiliki ROM pembangkit karakter untuk 192 jenis karakter
- RAM untuk data display sebanyak 80x8 bit
- Dapat dirangkai dengan MPU 8 bit / 4 bit
- RAM data display dan RAM pembangkit karakter dapat dibaca oleh MPU
- Memiliki fungsi intruksi anatara lain *display on/off, cursor on/off, display* karakter *blink, cursor shift* dan *display shift.*
- Memiliki rangkaian oscillator sendiri
- Catu tegangan tunggal yaitu ± 5V
- Memiliki rangkaian *reset* otomatis pada catu daya yang dihidupkan.

LCD memiliki 16 pin, masing – masing memiliki fungsi sebagai berikut :

Tabel 2.8 Fungsi tiap pin LCD

No pin	Simbol	Level	fungsi	
1	Vss	-	Power supply	0 V (GND)
2	Vcc	-		5 V ± 10%
3	VEE	-		For LCD drive
4	RS	H/L	Sinyal seleksi regester H ; data input [register data (*write/read*)] L ; *instruction input* [register instruksi *(write), busy flag* dan *address counter (read)*]	
5	R/W	H/L	H ; *read* L ; *write*	
6	E	H	*Enable* signal [sinyal penanda mulai operasi, aktif saat operasi *write* atau *read*]	
7	DB0	H/L	4 *bit* bus data *lower* 2 arah, dapat dibaca atau ditulis terhadap mikrokontroler	
8	DB1	H/L		
9	DB2	H/L		
10	DB3	H/L		
11	DB4	H/L	4 *bit* bus data *upper* 2 arah, dapat dibaca atau ditulis terhadap mikrokontroler, DB7 juga sebagai *busy flag*	
12	DB5	H/L		
13	DB6	H/L		
14	DB7	H/L		
15	V+BL	-	Back Light Supply	4 – 4,2 V 50 – 200 mA
16	V-BL	-		0 V (GND)

Instruksi Operasi

Tabel 2.9 Instruksi pada LCD

Instruksi	RS	RW	D7	D6	D5	D4	D3	D2	D1	D0
Display Clear	0	0	0	0	0	0	0	0	0	1
Cursor Home	0	0	0	0	0	0	0	0	1	*
Entry Mode Set	0	0	0	0	0	0	0	1	I/D	S
Display On/Off	0	0	0	0	0	0	1	D	C	B
Cursor Display Shift	0	0	0	0	0	1	S/C	R/L	*	*
Function Set	0	0	0	0	1	DL	1	*	*	*
CG RAM Address Set	0	0	0	1	ACG					
DD RAM Address Set	0	0	1	ADD						
BF/Address Read	0	1	BF	AC						
Data Write to CG RAM	1	0	Write data							
Data Read from CG RAM	1	1	Read data							

*invalid bit

ACG : CG RAM *Address* dan ADD

DD RAM *Address*

Pada LCD juda terdapat instruksi – instruksi sebagai berikut :

1. Display *Clear*

   Memberikan tampilan yang ada pada LCD serta menyimpan, sedangkan kursor kembali ke posisi semula.

2. *Cursor Home*

   Hanya memberikan tampilan dan kursor kembali ke semula

3. Empty Mode Set : layar beraksi sebagai tampilan tulis

   S : 1/10 = menggeser layar

   1/0 : 1 = kursor bergerak ke kanan dan layar bergerak ke kiri

   1/0 : 0 = kursor bergerak ke kiri dan layar bergerak ke kanan

4. Display On/Off Control

   D : 1 = layar on

   D : 0 = layar off

C : 1 = kursor on

C : 0 = kursor off

B : 1 = kursor berkedip – kedip

B : 0 = kursor tidak berkedip – kedip

5. Cursor Display Shift

   S/C : 1 = LCD diidentifikasikan sebagai layar

   S/C : 0 = LCD diidentifikasikan sebagai kursor

   R/L : 1 = menggeser satu spasi ke kanan

   R/L : 0 = menggeser satu spasi ke kiri

6. Fuction Set

   DL : 1 = panjang data LCD pada 8 bit

   DL : 0 = panjang data LCD pada 4 bit

   Bit upper di transfer terlebih dahulu kemudian diikuti dengan 4 bit lower

   N : 1/0 = LCD menggunakan 2 atau 1 baris karakter

   P : 1/0 = LCD menggunakan 5 x 10 dot matrik

7. CG RAM address set : menulis alamat RAM ke karakter
8. DD RAM address set : menulis alamat RAM ke tampilan
9. BF/address set : BF = 1/0, LCD dalam keadaan sibuk atau tidak sibuk
10. Data write to CG RAM or DD RAM : membaca byte dari alamat terakhir RAM yang dipilih.

Operasi Dasar

- Register

  Control dari LCD memiliki 2 buah register 8 bit yaitu register intruksi (IR) dan register data (DR). IR memiliki instruksi seperti display, *clear*, *cursor shift* dan display data (DD RAM) serta karakter (CG RAM). DR menyimpan data untuk ditulis ke DD RAM ataupun membaca data dari DD RAM maka DR secara otomatis menulis data ke DD RAM atau CG RAM. Ketika data pada CG RAM atau DD RAM akan dibaca maka alamat data ditulis pada IR. Sedangkan data akan dimasukkan melalui DR sehingga dapat dibaca oleh mikrokontroler.

Table 2.10 Pemilihan register pada LCD

RS	RW	Operasi
0	0	Seleksi IR, IR Write Display Clear
0	1	Busy Flag (DB7), @ Counter (DB0 – DB7) Read
1	0	Seleksi DR, DR Write
1	1	Seleksi DR, DR Read

- Busy Flag

  Busy Flag menunjukkan bahwa modul siap untuk menerima instruksi selanjutnya sebagaimana terlihat pada tabel diatas. Register seleksi sinyal akan melalui DB7 jika RS=0 dan R/W=1. Jika bernilai 1 maka sedang melakukan kerja internal dan instruksi tidak akan dapat diterima, oleh karena itu status dari flag harus diperiksa sebelum melaksanakan instruksi selanjutnya.

- Address Counter (AC)

  AC menunjukkan lokasi memori dalam modul LCD. Pemilihan lokasi alamat lewat AC diberikan lewat register instruksi (IR) ketika data pada A, maka AC secara otomatis menaikkan atau menurunkan alamat tergantung dari *Entry Mode Set.*

- Display Data RAM

  Pada LCD, masing – masing line memiliki *range* tersendiri.alamat itu diekspresikan dengan bilangan hexadecimal. Untuk line 1 *range* alamat berkisar antara 40H-4FH.

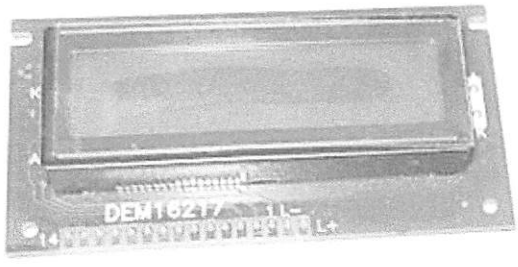
- Character Generator ROM (CG ROM)

  CG ROM memiliki tipe dot matrik 5x7, dimana pada LCD telah tersedia ROM sebagai pembangkit karakter dalam kode ASCH.

- Character Generator RAM (CG RAM)

  CG RAM dipakai untuk pembuatan karakter tersendiri melalui program.

  Adapun bentuk fisik dari LCD M1632 adalah pada gambar berikut :



Gambar 2.15 *Liquid Crytal Display* LCD[7]

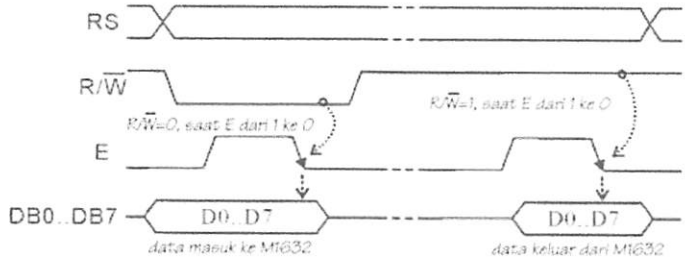
Sinyal interface M1632

Untuk berhubungan dengan mikrokontroler pemakai, M1632 dilengkapi dengan 8 jalur data (DB0 – DB7) yang dipakai untuk menyalurkan kode ASCH ataupun perintah pengatur kerjanya M1632. Selain itu dilengkapi pula dengan E, R/W, dan RS seperti layaknya komponen yang kompatibel dengan mikroprosesor.

Kombinasi lainnya E dan R/W merupakan sinyal standar pada komponen buatan Motorola. Sebaliknya sinyal –sinyal dari MCS51 merupakan sinyal khas intel dengan kombinasi sinyal WR dan RD.

RS, singkatan dari *Register select*, dipakai untuk membedakan jenis data yang dikirim ke M1632, kalau RS=0 data yang dikirim adalah perintah untuk mengatur kerja M1632, sebaliknya kalau RS=1 data yang akan dikirim adalah kode ASCH yang ditampilkan.

Demikian pula saat pengambilan data, saat RS=0 data yang diambil dari M1632 merupakan data status yang mewakili aktivitas M1632 dan saat RS=1 maka data yang diambil merupakan kode ASCH dari data yang ditampilkan.
Proses mengirim/mengambil data ke/dari M1632 bisa dijabarkan sebagai berikut :



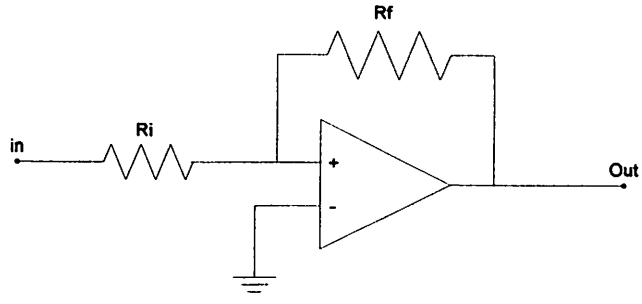
Gambar 2.16 Mengirim/Mengambil Data Ke/Dari M1632[7]

1. RS harus dipersiapkan dulu, untuk menentukan jenis data seperti yang telah dibicarakan di atas
2. R/W di nol kan untuk menandakan akan diadakan pengiriman data ke M1632. Data yang akan dikirim disiapkan di DB0..DB7, sesaat kemudian sinyal E di satu kan dan di nol kan kembali. Sinyal E merupakan sinyal sinkronisasi, saat E berubah dari 1 menjadi 0 data di DB0..DB7 diterima M1632.
3. Untuk mengambil data dari M1632 sinyal R/W di satu kan, menyusul sinyal E di satu kan. Pada suatu E menjadi 1, M1632 akan meletakkan datanya di DB0..DB7, data ini harus diambil sebelum sinyal E di nol kan kembali.

2.9 Buffer

Pada penguat inverting tegangan input diberikan pada tegangan terminal input negative sedangkan terminal positifnya dihubungkan dengan ground. Pada perancangan ini penguat inverting difungsikan sebagai *buffer*, dan menggunakan IC op amp LM741.

Rangkaian dasar penguat inverting adalah seperti yang ditunjukkan pada gambar 2-11 :



Gambar 2.17. Rangkaian Buffer[8]

Penguatannya dapat dilihat dari persamaan dibawah ini :

$$A = \frac{Vout}{Vin}$$

$$A = \left[\frac{RF}{Ri} \right]$$

$$A = \left[\frac{RF}{Ri} \right] \text{x Vin}$$

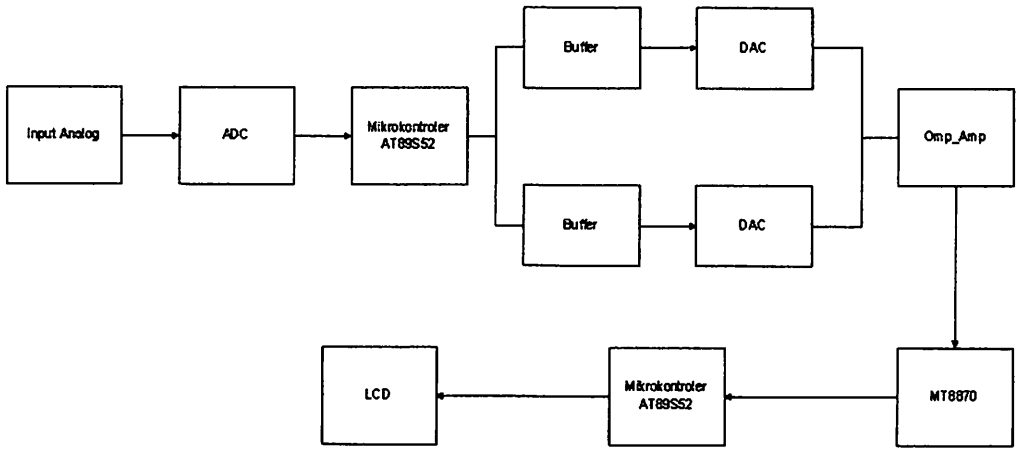
BAB III

PERENCANAAN DAN PEMBUATAN ALAT

Bab ini akan membahas tentang perencanaan dan pembuatan sistem akuisisi data dilengkapi DTMF memakai DDS yang meliputi perancangan perangkat keras (*hardware*) dan perangkat lunak (*software*), untuk lebih detailnya akan dijelaskan pada sub bab berikut ini :

3.1.Diagram Blok Rangkaian

Secara garis besar, prinsip kerja alat ini dapat digambarkan melalui blok diagram dibawah ini:



Gambar 3-1 Blok Diagram Rangkaian

Prinsip kerja dari blok diagram diatas adalah :

1. ***Input Analog*** sebagai contoh masukan data
2. **ADC (*Analog to Digital Conventer*)** untuk mengubah data *analog* menjadi data *digital.*
3. **Mikrokontroler AT89S52** sebagai membuat penggabungan 2 frekuensi *high* dan frekuensi *low* dengan bantuan sistem DDS.

4. ***Buffer*** sebagai penguat digital
5. **DAC (R2R)** untuk mengubah data *digital* menjadi data *analog.*
6. **Op amp** sebagai penguat analog
7. **Mikrokontroler MT8870** sebagai menterjemah sinyal DTMF yang dikirim oleh DAC.
8. **Mikrokontroler AT89S52** sebagai penterjemah data yg berasal dari MT8870
9. **LCD** untuk menampilkan angka atau tulisan (data).

3.2. Perencanaaan Hardware

Dalam perencanaan ini rancangan *hardware* yang dibuat bertujuan guna mendukung dan memberikan kemudahan pada proses kerja perancangan *software* agar nantinya sesuai dengan kondisi yang diinginkan, Untuk perancangan *hardware* sendiri dibagi menjadi 8 bagian yaitu :

1. Minimum Sistem AT89S52
2. *Analog Digital Converter* (ADC) 0804
3. *Buffer*
4. DAC (R2R) *Resistor to Resistor*
5. Op amp
6. Minimum Sistem MT8870
7. LCD

3.2.1 Perancangan Minimum Sistem Mikrokontroller AT89S52

Penggunaan mikrokontroller AT89S52 harus didukung oleh beberapa rangkaian penunjang agar dapat melakukan fungsinya, antara lain rangkaian *clock* dan rangkaian *reset*. Selain itu juga harus ditentukan penggunaan port-portnya untuk rangkaian pendukung yang lain.

3.2.1.1 Rangkaian *clock*

Kecepatan proses pengolahan data pada mikrokontroller ditentukan oleh *clock* (pewaktu) yang dikendalikan oleh mikrokontroller tersebut. Pada mikrokontroller AT89S52 terdapat *internal clock generator* yang berfungsi sebagai sumber *clock*, tapi masih memerlukan rangkaian tambahan untuk membangkitkan *clock* yang diinginkan.

Rangkaian tambahan ini terdiri atas 2 buah kapasitor dan sebuah kristal yang terangkai sedemikian rupa dan kemudian dihubungkan dengan port yang khusus tersedia pada mikrokontroller.

Dalam perancangan rangkaian ini menggunakan :

- 2 Kapasitor 33 pF. Penentuan besarnya kapasitansi disesuaikan dengan spesifikasi pada data sheet.
- Kristal 24 MHz.

Dengan demikian perhitungannya dapat dilihat sebagai berikut :

f = 24 MHz

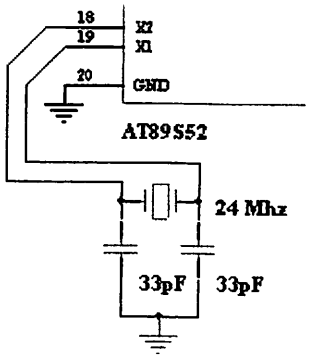
$$T = \frac{1}{f}$$

$$T = \frac{1}{24x10^6}$$

karena 1 siklus mesin = 12T maka

$$1 \text{ siklus mesin} = 12 \text{ x } \frac{1}{24x10^6} = 0{,}499 \ \mu s$$

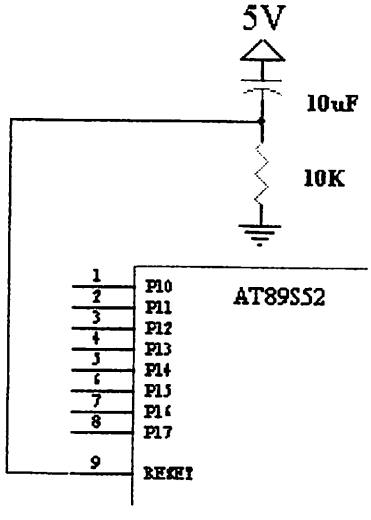
Adapun gambar rangkaian *clock* sebagai berikut :



Gambar 3-2 Rangkaian *Clock*

3.2.1.2 Rangkaian *reset*

Reset pada mikrokontroller merupakan masukan aktif *high* '1' pulsa transisi dari rendah '0' ketinggi akan me-*reset* mikrokontroller menuju alamat 0000H. Pin *reset* dihubungkan dengan rangkaian *power-on reset* seperti pada gambar 3-3:



Gambar 3-3 Rangkaian *Reset*

Rangkaian *reset* bertujuan agar mikrokontroller dapat menjalankan proses dari awal. Rangkaian *reset* untuk mikrokontroller dirancang agar mempunyai kemampuan *power on reset*, yaitu *reset* yang terjadi pada saat sistem dinyalakan untuk pertama kalinya. *Reset* juga bias dilakukan secara manual dengan menekan tombol *reset* yang berupa *switch push button.*

Rangkaian *reset* terbentuk oleh komponen resistor dan kapasitor yang sudah baku (ditetapkan oleh perusahaan pembuat IC AT89S52). Nilai resistor yang dipakai adalah 10KΩ dan kapasitor 10μF. Karena kristal yang digunakan mempunyai frekuensi sebesar 12 MHz, maka satu periode membutuhkan waktu sebesar :

$$T = \frac{1}{f_{XTAL}} = \frac{1}{12MHz} S = 8{,}333 \times 10^{-8}$$

Sehingga waktu minimal logika yang dibutuhkan untuk me-*reset* mikrokontroller adalah :

Reset (minimal) = T x periode yang dibutuhkan

$= 8{,}333 \times 10^{-8} \times 24 = 1{,}999\ \mu s$

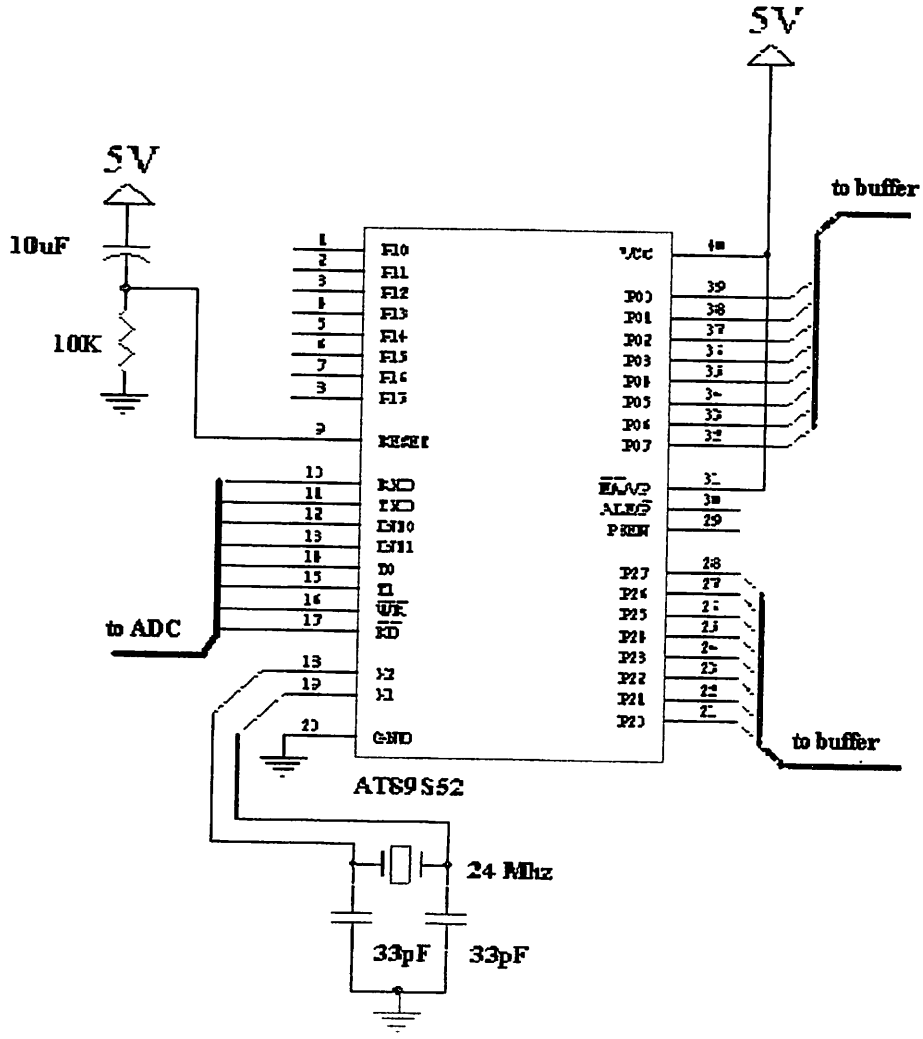
Jadi mikrokontroller membutuhkan waktu minimal 1,999 μs untuk me-*reset*. Waktu inilah yang dijadikan pedoman untuk menetukan nilai R dan C. Dengan menetukan nilai R = 10 kΩ dan C = 10 μF, maka :

$T = 0.357\ R.C = 0{,}357 \times 10000\ \Omega \times 10.10^{-6} = 35{,}7$ ms

Jadi dengan nilai komponen R = 10 kΩ dan C = 10 μF dapat memenuhi syarat minimal untuk waktu yang dibutukan mikrokontroller

3.2.1.3 Perancangan Penggunaan Port-Port Pada Mikrokontroller AT89S52

Pada skripsi ini mikrokontroller AT89S52 digunakan sebagai pusat pengendali kerja dari alat yang dibuat Gambar 3-4 menunjukkan rancangan port-port I/O pada mikrokontroller AT89S52 yang dimanfaatkan pada skripsi



Gambar 3-4 Perancangan mikrokontroller box 1

1. Port 0

Port 0.0 – Port 0.7 (pin 32 – 39) digunakan sebagai port keluaran untuk *buffer*

2. Port 1

Port 1.0 – Port 1.7 (pin 1 – 8) tidak digunakan pada alat ini

3. Port 2

   Port 2.0 – Port 2.7 (pin 21 – 28) dihubungkan ke *buffer*

4. Pin 10 – pin 17 (P3.0 – P3.7) merupakan port dari mikrokontroler yang digunakan sebagai port masukan dari ADC

5. Pin 9 (*reset)* dihibungkan dengan rangkaian *reset*

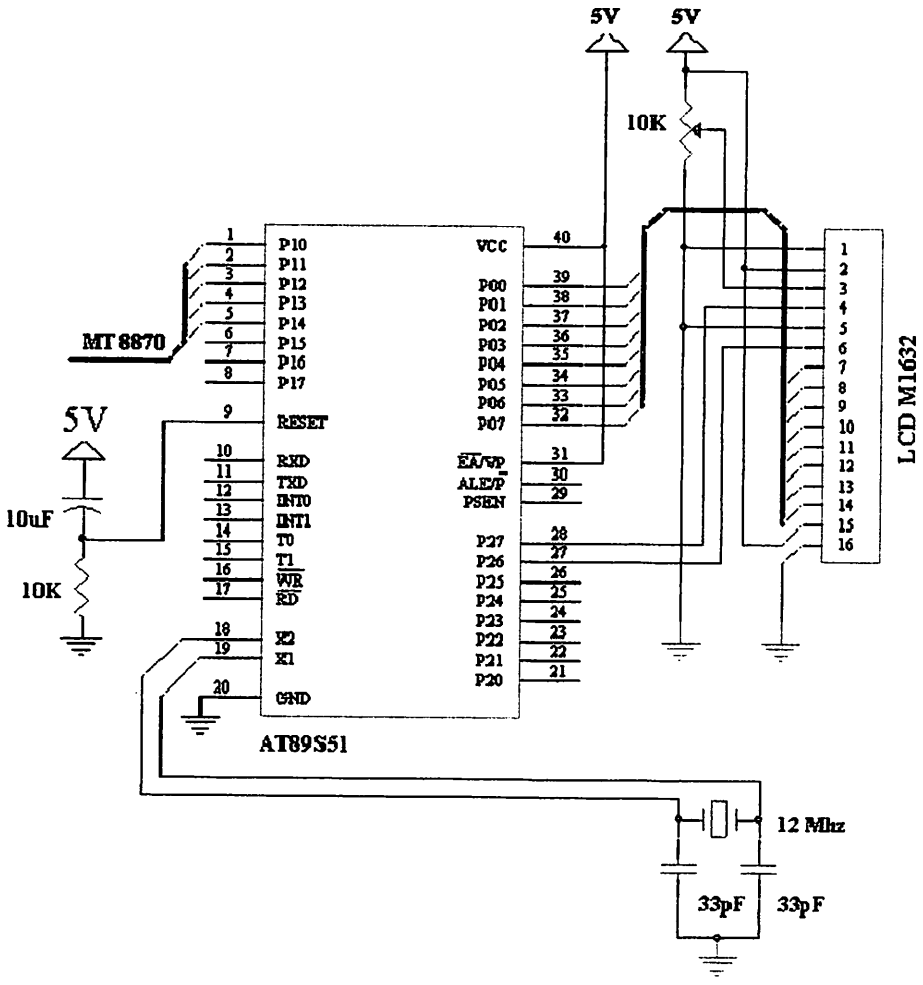
6. Pin 18 dan pin 19 dihubungkan dengan rangkaian rangkaian *clock* atau *Oscillator external*

7. Pin 31 (EA) diberi logika tinggi (*high)* atau dihubungkan dengan Vcc maka mikrokontroller akan mengakses program dari ROM internal (EPROM atau *flash memory*)

8. Pin 29 dan pin 30 (ALE/PROG dan PSEN) tidak digunakan karena pada pembuatan alat ini tidak menggunakan atau mengakses *memory eksternal*

9. Pin 40 (Vcc) dihubungkan dengan tegangan *supply* +5V

10. Pin 20 (GND) dihubungkan dengan tegangan *supply ground*



Gambar 3-5 Perancangan mikrokontroller box 2

1. Port 0

   Port 0.0 – Port 0.7 (pin 39 – 32) digunakan sebagai *outputan* data yang dikirim untuk LCD M1632

2. Port 1

   Port 1.0 – Port 1.4 (pin 1 – 5) digunakan sebagai masukan dari IC MT 8870

3. Port 2

   Port 2.6 – Port 2.7 (pin 27 – 28) dihubungkan ke LCD M1632

4. Pin 10 – pin 17, pin 25 – pin 20 dan pin 6 – pin 8 tidak digunakan pada alat ini

5. Pin 9 (*reset)* dihibungkan dengan rangkaian *reset*
6. Pin 18 dan pin 19 dihubungkan dengan rangkaian rangkaian *clock* atau *Oscillator external*
7. Pin 31 (EA) diberi logika tinggi (*high)* atau dihubungkan dengan Vcc maka mikrokontroller akan mengakses program dari ROM internal (EPROM atau *flash memory*)
8. Pin 29 dan pin 30 (ALE/PROG dan PSEN) tidak digunakan karena pada pembuatan alat ini tidak menggunakan atau mengakses *memory eksternal*
9. Pin 40 (Vcc) dihubungkan dengan tegangan *supply* +5V
10. Pin 20 (GND) dihubungkan dengan tegangan *supply ground*

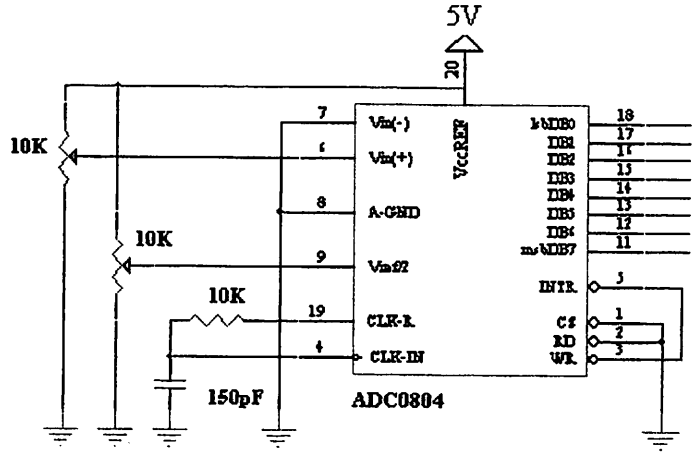
3.2.1.4 Rangkaian *Analog Digital Converter* (ADC) 0804

Transformator tegangan berguna untuk menurunkan tegangan dari jala-jala menjadi tegangan yang dibutuhkan oleh ADC dan mikrokontroller untuk bisa bekerja, yaitu sebesar 0 – 5 Volt. Karena tegangan yang diukur adalah tegangan ±220volt, maka diperlukan adanya transformator penurun tegangan (transformator *stepdown*). Tegangan ini kemudian disearahkan atau diubah menjadi tegangan DC agar dapat diterjemahkan menjadi tegangan digital oleh rangkaian ADC 0808. Dengan mengetahui N_1 dan N_2, membaca tegangan V_2, serta menganggap transformator ideal maka tegangan V_1 adalah:

$$V_1 = \frac{N_1}{N_2} \text{ x } V_2$$

Pentanahan rangkaian sekunder diperlukan untuk mencegah adanya beda potensial yang besar antara kumparan primer dan kumparan sekunder.

ADC yang digunakan adalah ADC 0804 yang merupakan ADC satu kanal *input* dengan output pararel 8 bit. Agar ADC dapat bekerja secara optimal maka diberi catu daya 5 volt. ADC 0804 telah dilengkapi *clock internal* yang dapat diaktifkan dengan menghubungkan dengan tahanan dan kapasitor *eksternal.*



Gambar 3-6 Rangkaian *Analog Digital Converter* (ADC) 0804

Nilai tahanan R2 ditentukan sebesar 10 KΩ dan nilai kapasitor C2 sebesar 150 pF, sehingga memberikan frekuensi *clock* sebesar :

$$F = \frac{1}{1{,}1RC} = \frac{1}{1{,}1x10K\Omega x150pF} = 606{,}06\ KHz$$

Berdasarkan frekuensi *clock* diatas, maka waktu konversi maksimum yang dibutuhkan ADC adalah :

$$T = \frac{2^n}{f} = \frac{2^8}{606{,}06x10^3} = 0{,}42\ ms$$

ADC ini dirancang agar dapat menerima tegangan *input* antara 0 – 4,5 Volt. Pada perencanaan ini diberikan tegangan reverensi (Vref/2) pada pin 9 sebesar 2,25 volt. Untuk mendapatkan Vref/2 digunakan rangkaian resistor pembagi tegangan yang terdiri dari 2 buah resistor yang terhubung secara seri,

perancangan, salah satu resistor digunakan *variable* resistor sebesar 10KΩ ingga tegangan keluarannya dapat diatur sesuai dengan kebutuhan.

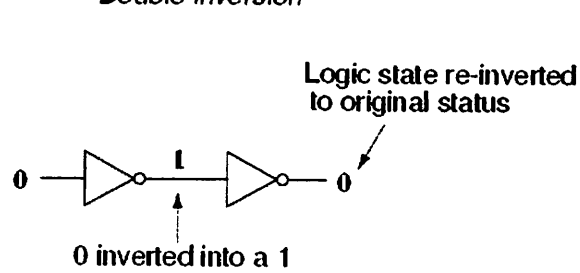
Dengan Vref/2 sebesar 2,25 Volt maka ADC akan memiliki resolusi sebesar

$$\text{Resolusi} = 2 \text{ x } \frac{Vref/2}{2^n - 1} \text{ Volt / step}$$

$$= 2 \text{ x } \frac{2{,}25}{2^8 - 1} \text{ Volt / step } = 17{,}65 \text{ mV / step}$$

3.3. Buffer

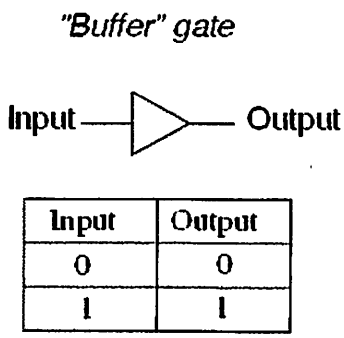
Untuk menghubungkan dua pintu inverter bersama sehingga output dari satu menjadi masukan dari yang lain, dua fungsi pembalikan akan "membatalkan" satu sama lain agar tak akan ada pembalikan masukan dari final output:



Gambar 3-7 Dua pintu inverter

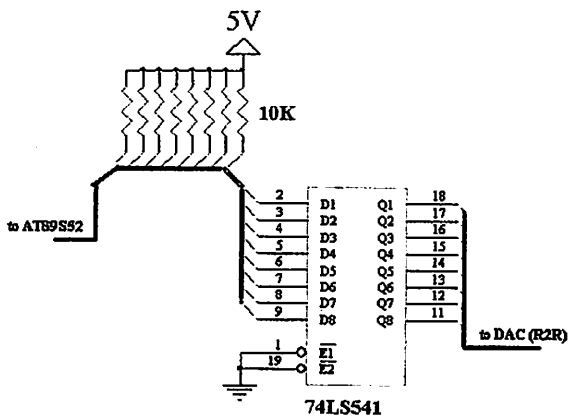
Ingat bahwa pintu gerbang sirkuit adalah sinyal *Amplifier*, tanpa memperhitungkan logika apa yang mungkin dilakukan oleh fungsi. Sebuah sumber sinyal lemah (yang tidak mampu atau dengan men-source sangat banyak saat ini tenggelam ke beban) mungkin di dukung oleh sarana inverters seperti dua pasangan yang ditampilkan dalam ilustrasi sebelumnya. Logiknya adalah tingkat

tidak berubah, tetapi saat ini penuh dengan men-source kemampuan akhir inverter tersedia untuk drive beban tahan jika diperlukan. Untuk tujuan ini, khusus pintu gerbang logika disebut *penyangga* yang diproduksi untuk melakukan fungsi yang sama dengan dua inverters. Simbol yang hanya sebuah segitiga, dengan tidak inverting "gelembung" pada output terminal:



Input	Output
0	0
1	1

Gambar 3.8 Buffer gate atau jembatan buffer



Gambar 3.9 rangkaian buffer

3.4 *Rangkaian Digital Analog Converter* (DAC) R-2R

Digital To Analog Converter R 2 R digunakan untuk mengkonversi data *digital* menjadi sinyal *analog*. Pada umumnya semua bentuk konverter *digital* ke *analog* akan menghasilkan suatu keluaran yang berupa arus dan tegangan yang merupakan bentuk hasil perkalian antara tegangan analog referensi dengan data digital tertentu (*Multiplying D/A Converter*).

Karena konverter *digital* ke *analog* ini banyak macamnya, maka pada umumnya dipakai cara konversi dengan rangkaian resistor berbobot (*binary weighted resistor*) dimana posisi dari bit digital yang akan diberikan akan menghasilkan besar arus tegangan yang sesuai bobot biner pada data *digital*. Didalam penerapannya, cara pemakaian harga tahanan yang bervariasi akan menimbulkan kesulitan dalam memilih harga tahanan yang sesuai, sehingga dipakai rangkaian tangga tahanan R-2R yang lebih sederhana.

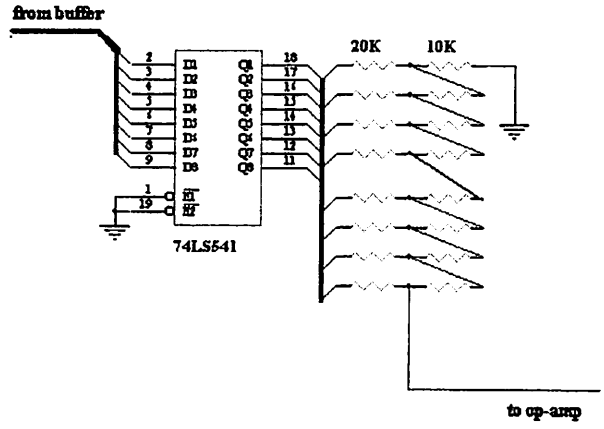
Tahanan keluaran V*out* dapat dihitung dengan rumus berikut;

$$\text{Vout} = - \frac{Rf}{R} Vref \left(\frac{D_0}{2^n} + \frac{D_1}{2^{n-1}} + \frac{D_2}{2^{n-2}} \right) - \left(\frac{D_{(n-2)}}{2^2} + \frac{D_{(n-1)}}{2^1} \right)$$

Dimana: $D_0 ... D_1$ = bernilai 1 atau 0

n = banyaknya bit masukan

Vre = tegangan referensi

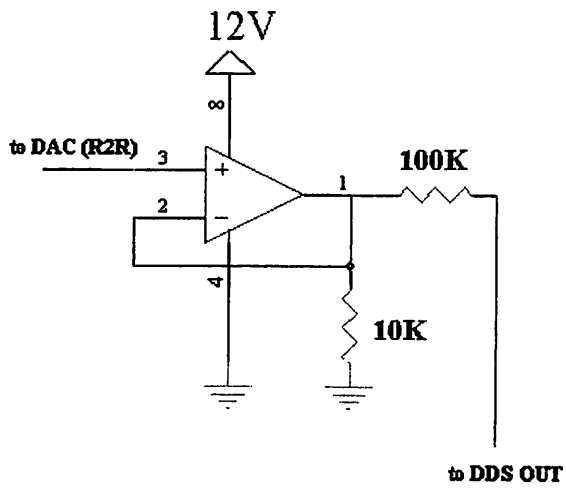


Gambar 3-7 Rangkaian DAC R 2 R (Digital Analog Converter)

3.5 Omp_Amp

Amplifier atau lazim disebut penguat dalam suatu rangkaian dapat difungsikan dalam suatu rangkaian penguat sinyal input, rangkaian penjumlahan tegangan input, rangkaian pembanding antara 2 sinyal input, rangkaian filter dan masih banyak lagi.

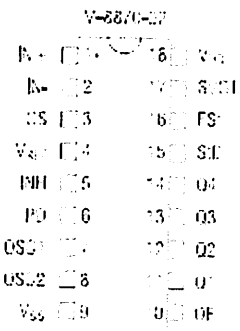
Rangkaian penguat ini sangat sederhana dalam pemakaianya baik secara merangkaianya maupun dalam penggunaanya. Rangkaian ini terdiri dari kombinasi antara pengutan operasional yang dirangkai bersama kompenen pasif tahanan atau kondensator. Dengan kombinasi ini dapat dikembangkan lagi menjadi rangkaian yang mempunyai spesifikasi khusus seperti rangkaian instrumentasi, rangkaian isolator, dan lain sebagaianya. Gambar 3-8 menunjukan simbol dari op-amp dengan lima terminal dasar terdiri dari 2 terminal catu daya, 2 terminal input atau masukan yaitu (+) dan (-) dan terminal *output* atau keluaran dari op-amp.



Gambar 3.8 Rangkaian Op Amp.

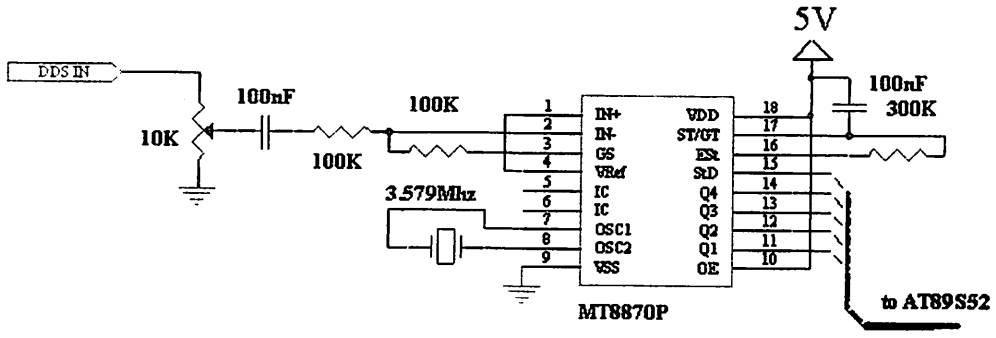
3.6 Minimum Sistem MT8870

Dekoder DTMF MT8870, Decoder DTMF merupakan rangkaian yang dapat menghasilkan kode biner dari sinyal DTMF. DTMF MT8870 mempunyai bentuk yang kecil, berdaya rendah, dapat diandalkan, dan dapat dioperasikan pada suhu -40 C sampai 80 C.



Gambar 3-9 Konfigurasi pin IC MT 8870

Decoder ini mengkodekan sinyal– sinyal DTMF menjadi kode biner (*binary code*) 4 bit. Decoder ini telah dilengkapi dengan filter untuk frekuensi tinggi (*high frequency*) dan frekuensi rendah (*low frequency*) serta sebuah digital decoder. Filter menggunakan *switched capacitor* untuk membedakan frekuensi yang masuk, sedang decoder menggunakan teknik pencacahan (*counting techniques*) secara digital untuk mendeteksi dan mengkodekan 16 buah pasangan frekuensi DTMF menjadi kode biner 4 bit. Selain itu, MT8870 juga dilengkapi dengan rangkaian internal penguat differential, *oscillator clock*,dan sebuah rangkaian latch 3 state pada bagian *output*. Dengan demikian rangkaian external tambahan untuk membentuk sebuah decoder DTMF yang lengkap dapat dikurangi.

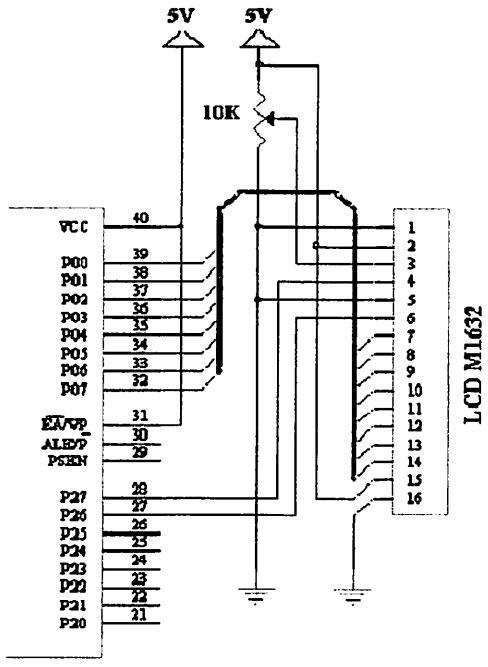


Gambar 3-19 rangkaian DTMF MT8870

3.7 LCD (*Liquid Crystal Display*)

Untuk tampilan masukan besaran yang diinginkan serta menampilkan apakah besaran sudah tercapai..

Dengan bantuan perangkat lunak yang dibuat, dapat ditampilkan karakter (besaran) yang bisa dilihat pada LCD.



Gambar 3.8 Rangkaian LCD

3.8 Sistem DDS (*Direct digital Synthesis*)

Sistem DDS (*Direct digital Synthesis*) merupakan salah satu cara untuk menghasilkan sinyal sinusoida secara langsung. Inti dari sistem ini adalah arsitektur akumulator dengan resolusi mencapai mili Hertz dan frekuensi sinyal yang dihasilkan dapat diatur tergantung dari sinyal frekuesi referensi dan metode perancangan. Keluaran sistem DDS yang diproses oleh mikrokontroler berupa sinyal digital kemudian menjadi masukan untuk DAC (D/A converter) dan LPF (Low Pass Filter) untuk menghasilkan sinyal sinusoida yang sempurna.

Semua parameter kontrol sistem DDS berada dalam bentuk digital. Sistem DDS pada dasarnya terdiri atas akumulator phasa, LUT (Look Up Table), dan osilator sebagai pembangkit frekuensi referensi (clock). Sedangkan DAC (Digital

To Analog Converter) dan LPF (Low Pass Filter) merupakan komponen–komponen penunjang sistem DDS

3.8.1 Kelebihan Dan Flesibilitas DDS

Kelebihan penggunaan Sistem DDS adalah karateristik sistem DDS itu sendiri, dimana keutamaan dari sistem ini adalah memiliki setting time/kecepatan yang cepat dan memiliki resolusi frekuensi yang halus terhadap frekuensi keluaran, operasi atas suatu spektrum frekuensi yang lebar dan dengan kemajuan dalam desain teknologi proses. Serta sangat ringkas dan sedikit membutuhkan daya. Sehingga sangat memungkinkan sistem DDS bisa lebih dikembangkan untuk desain alat yang berkaitan dengan aplikasi-aplikasi frekuensi hopping serta sistem-sistem yang berkaitan dengan peralatan pemancar radio,TV,peralatan test, dll.

Figure 1-4. Signal flow through the DDS architecture

Gambar 3-9 Signal Sinusoida Direct Digital Synthesis (DDS)

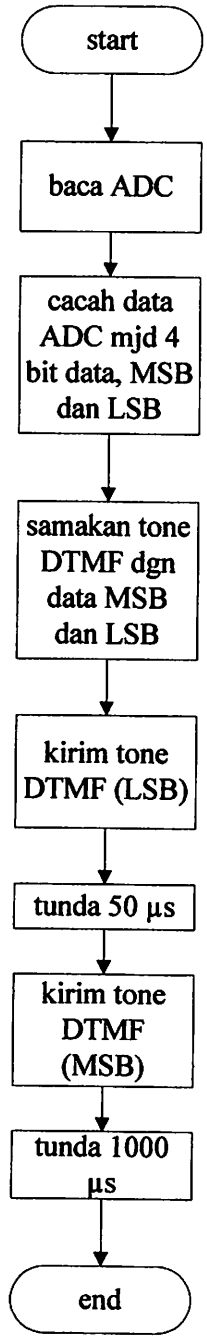
3.9. Perancangan Perangkat Lunak

Dalam menunjang kerja sistem secara keseluruhan diperlukan suatu perangkat lunak (*software*). *Software* yang digunakan untuk AT89S52 disini menggunakan bahasa *assembler* keluarga MCS52. Program yang ditulis dengan bahasa assembly terdiri dari *label; kode mnemonic* dan lain sebagainya yang pada

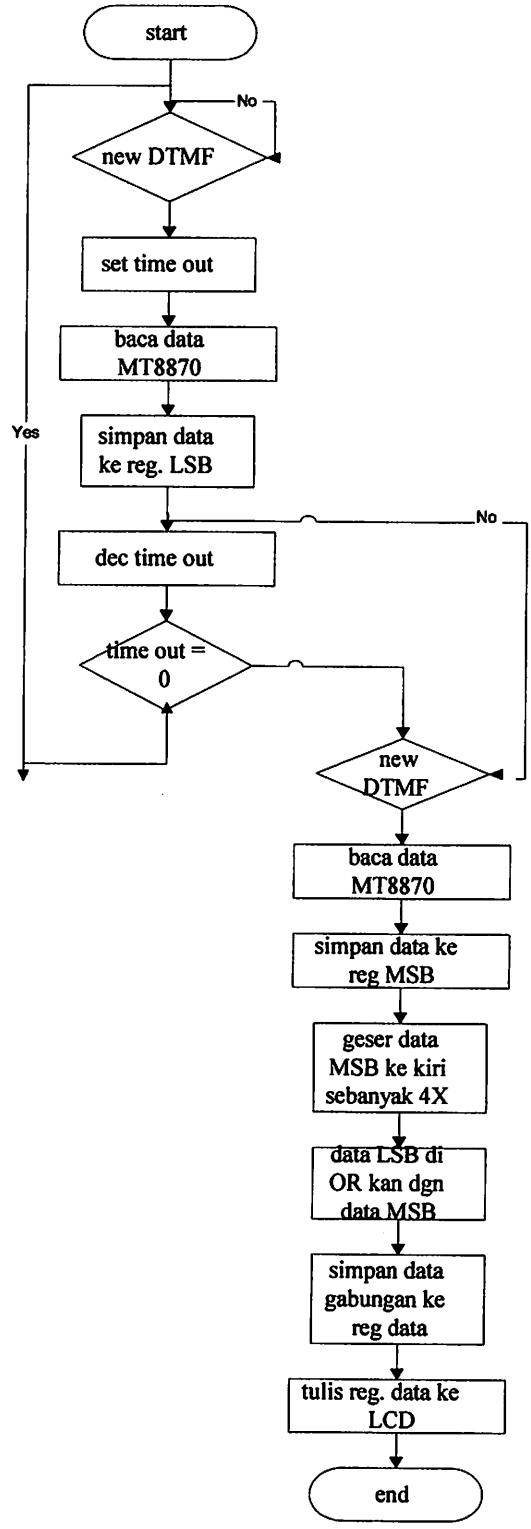
umumnya dinamakan sebagai program sumber (*source code*) yang belum bisa diterima oleh prosesor untuk dijalankan sebagai program, tetapi harus dijalankan dulu menjadi bahasa mesin dalam bentuk *kode biner.*

- Penulisan program dengan menggunakan teks editor dan disimpan dengan ekstensi *Asm.*
- Meng-compile program yang telah ditulis dengan menggunakan Compiler MCS52 sehingga didapatkan file dengan ekstensi *Hex.*
- Mengubah file berekstensi *Hex* menjafi file berekstensi *Bin.*
- Men-download file berekstensi Bin ke dalam EPROM Mikrokontroler AT89S52.

3.9.1 Flow Chart Kerja Rangkaian



Gambar 3-16 *flowchart* program utama



Gambar 3-12 ***Flowchart*** **program pendukung**

BAB IV

PENGUJIAN ALAT

Bab ini akan membahas pengujian alat yang telah dirancang, dirakit serta direalisasikan. Tujuan pengujian alat ini adalah mengetahui kerja dari masing-masing sistem yang dibuat secara per-blok. Dengan demikian dapat diketahui kepresisian kerja dari alat yang direncanakan dan dibuat. Secara umum tujuan dari pengujian alat tersebut adalah sebagai berikut :

1. Mengetahui proses kerja dari masing-masing rangkaian (blok).
2. Memudahkan pendataan spesifikasi alat.
3. Mengetahui hasil dari suatu perencanaan yang telah dibuat.
4. Memudahkan perawatan dan perbaikan apabila sewaktu-waktu terjadi kerusakan.

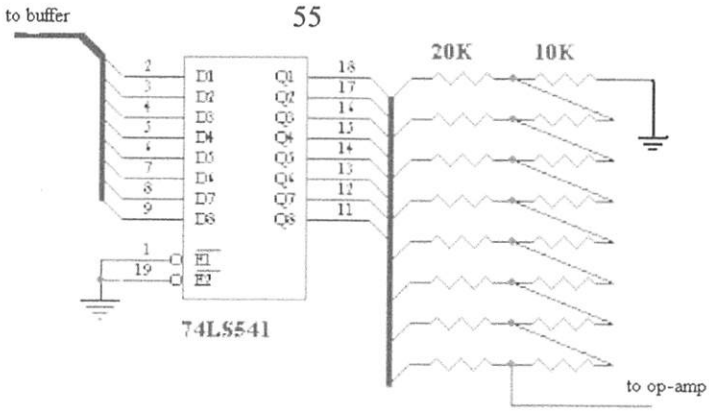
4.1 Pengujian Rangkaian DAC R2R

4.1.1. Tujuan

Pengujian rangkaian DAC R2R ini bertujuan untuk mengetahui bagaimana kondisi sinyal sinusoida pada saat dijalankan.

4.1.2. Langkah- Langkah Pengujian

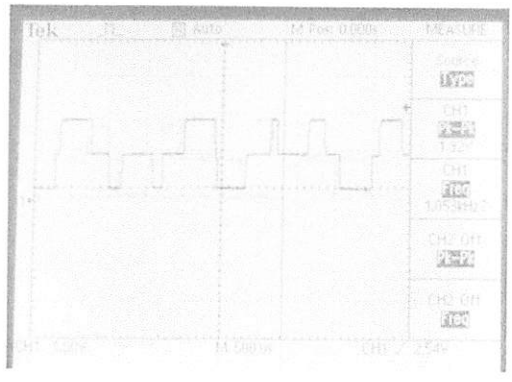
1. Menyusun rangkaian DAC R2R seperti pada gambar 4-1.
2. Rangkaian minimum sistem AT89S52
3. Menggunakan multitester digital
4. Menghubungkan rangkaian DAC R2R dengan tegangan Vcc (5V).
5. Mengamati hasil pengujian.



Gambar 4-1 Rangkaian DAC R2R

4.1.3. Hasil dan Analisa

Setelah melakukan pengujian DAC R2R maka hasil yang diperoleh adalah sebagai berikut :



Gambar 4-2 hasil pengujian sinusoida pada rangkain DAC R2R

Tabel 4 – 1 Hasil perhitungan dan Pengukuran Konversi Digital to Analog

No	Data Digital		Tegangan (V)
	Desimal	Biner	Pengukuran

0	0	00000000	0
1	25	00011001	0.5
2	51	00110011	1
3	77	01001101	1.5
4	103	01100111	2
5	129	10000001	2.5
6	155	10011011	3
7	182	10110110	3.5
8	208	11010001	4
9	233	11101001	4.5
10	255	11111111	5

Tabel 4 – 2 Hasil perhitungan dan Pengukuran Konversi Digital to Analog

No	Data Digital		Tegangan (V)		Eror (%)
	Desimal	Biner	Pengukuran	Perhitungan	
0	0	00000000	0	0	0
1	25	00011001	0.5	0.53	0.05
2	51	00110011	1	1.1	0.09
3	77	01001101	1.5	1.6	0.06
4	103	01100111	2	2.2	0.09
5	129	10000001	2.5	2.7	0.07
6	155	10011011	3	3.3	0.09
7	182	10110110	3.5	3.9	0.1

8	208	11010001	4	4.4	0.09
9	233	11101001	4.5	5	0.1
10	255	11111111	5	5.5	0.09

Sedangkan hasil perhitungan tegangan analog yang keluar dari rangkaian DAC R2R menggunakan rumus sebagai berikut :

$$\text{Vout} = Vref\left(\frac{D_0}{128}+\frac{D_1}{64}+\frac{D_2}{32}+\frac{D_3}{16}+\frac{D_4}{8}+\frac{D_5}{4}+\frac{D_6}{2}+\frac{D_7}{1}\right)$$

Ket :

V_{ref} = 5.5 V

Dn = Logika bit ke – ^{n}

$$\text{Vout} = 5{,}5x\left(\frac{0}{128}+\frac{0}{64}+\frac{0}{32}+\frac{1}{16}+\frac{1}{8}+\frac{0}{4}+\frac{0}{2}+\frac{1}{1}\right)$$

V_{out} = 0.5V

Dari contoh perhitungan, maka nilai tegangan analog hasil keluaran dari DAC R2R bisa diketahui. Dengan diketahuinya nilai tegangan analog keluaran DAC R2R hasil pengujian dan perhitungan, maka % kesalahan dapat diketahui dengan rumusan sebagai berikut :

$$\%\ \text{kesalahan} = \left(\frac{\text{perhitungan} - \text{pengukuran}}{\text{perhitungan}}\right) x\ 100\%$$

Adapun perbandingan antara tegangan keluaran DAC R2R hasil perhitungan, hasil pengujian dan % kesalahan yang terjadi ditampilkan pada table 4.3. Data tersebut menunjukkan bahwa rangkaian DAC R2R bisa beroperasi sesuai dengan data digital mikrokontroler AT89S52.

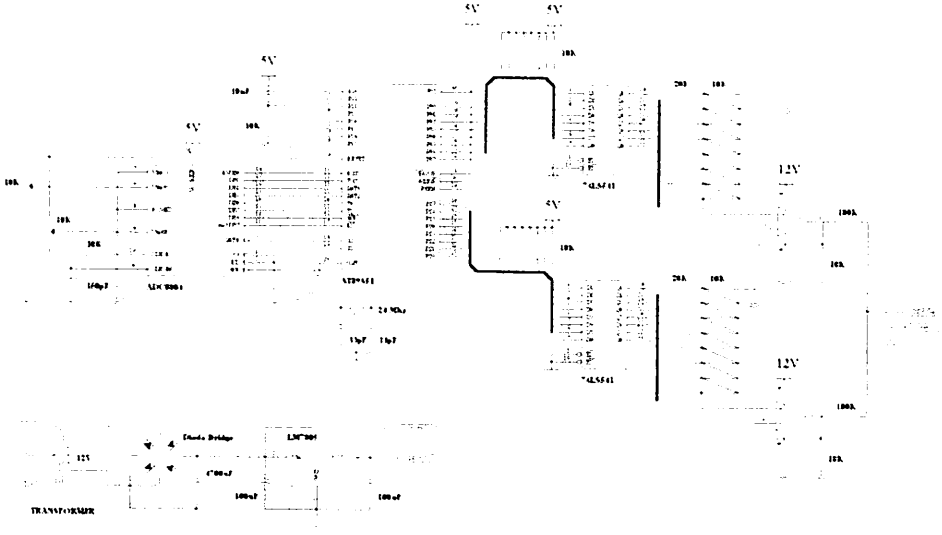
4.2. Pengujian Rangkaian keseluruhan

4.2.1. Tujuan

Pengujian ini bertujuan untuk mengetahui kinerja perangkat keras secara keseluruhan apabila dijalankan.

4.2.2. Langkah-Langkah Pengujian

1. Menyusun rangkaian keseluruan seperti pada gambar 4-3
2. Menghubungkan rangkaian keseluruan dengan jala-jala listrik.
3. Memutar potensiometer.
4. Mengamati hasil yang ditunjukan pada LCD.



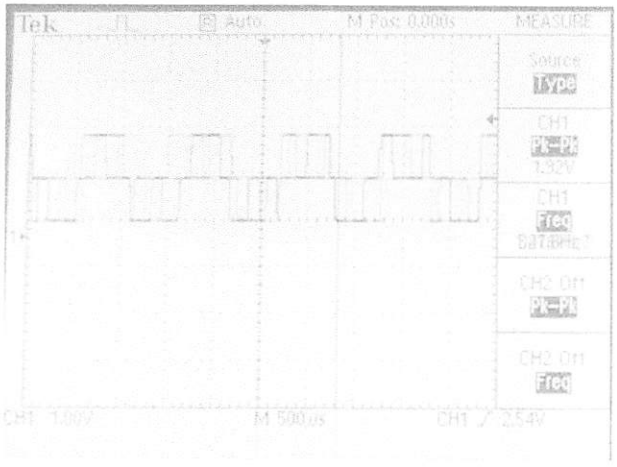
Gambar 4-3 Rangkaian Keseluruhan

4.2.3. Hasil dan Analisa

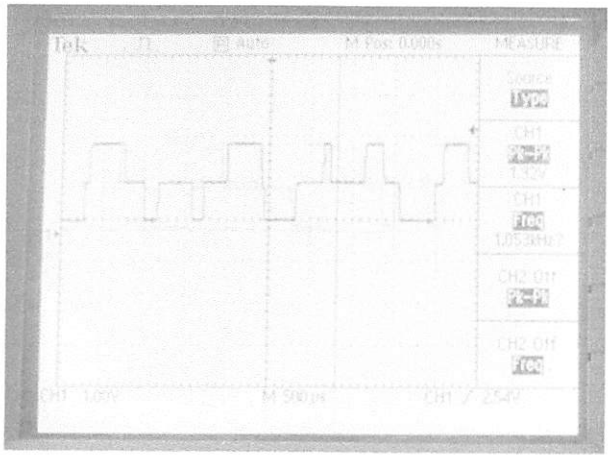
Pengujian sistem secara keseluruhan dilakukan dengan menggabungkan semua blok rangkaian dan menjalankan perangkat lunak

yang telah dibuat untuk menjalankan peralatan. Pengujian ini dimaksudkan untuk mengetahui kerja sistem keseluruhan.

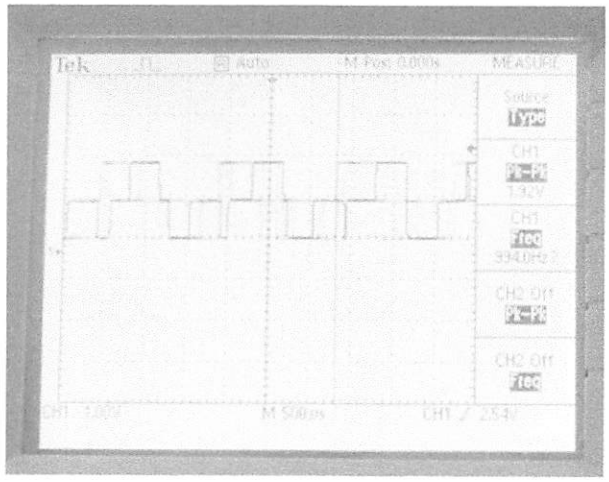
Hasil dari pengujian alat untuk rangkaian keseluruan adalah sebagai berikut :



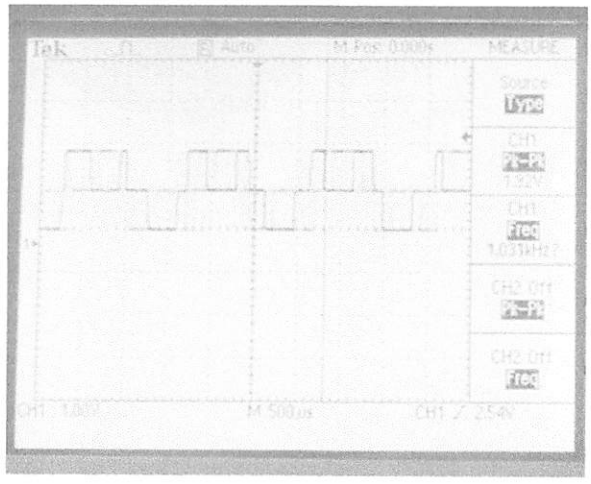
Gambar 4-4 hasil DTMF tone 0



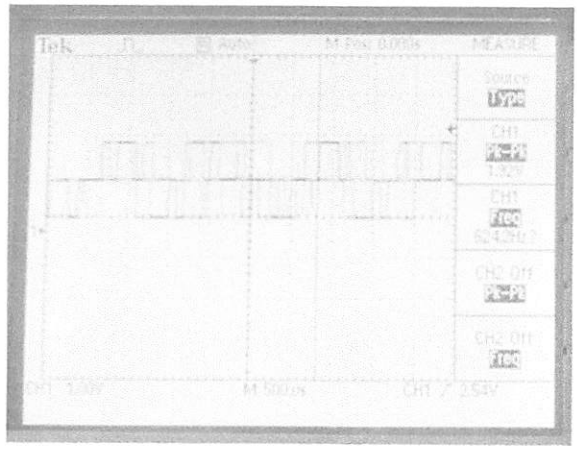
Gambar 4-5 Hasil DTMF tone 1



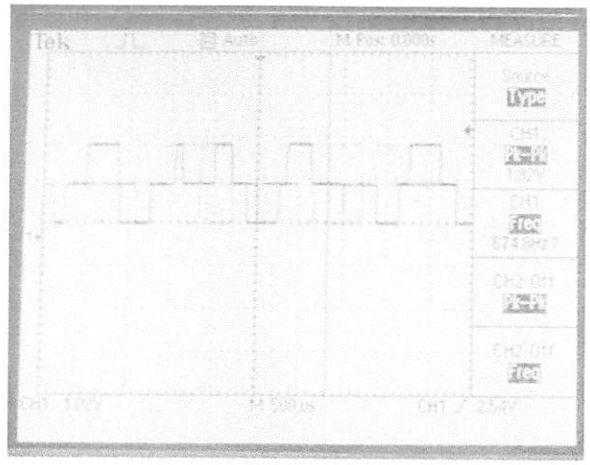
Gambar 4-6 Hasil DTMF tone 2



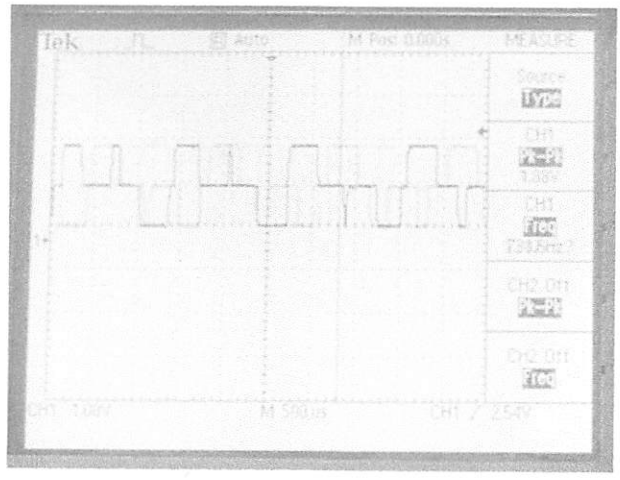
Gambar 4-7 Hasil DTMF tone 3



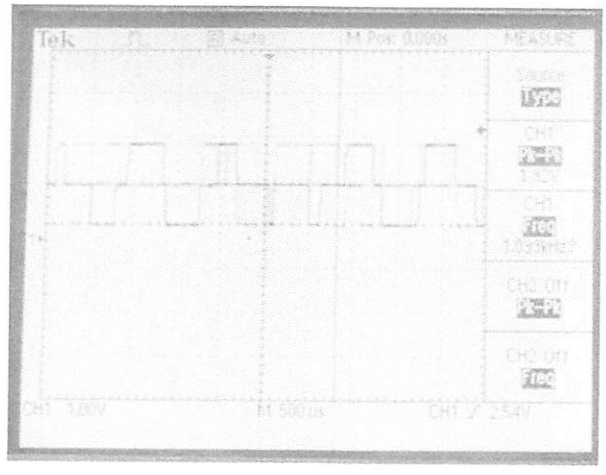
Gambar 4-8 Hasil DTMF tone 4



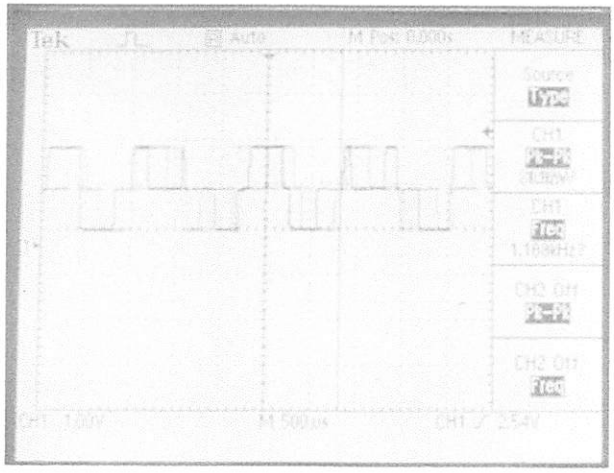
Gambar 4-9 Hasil DTMF tone 5



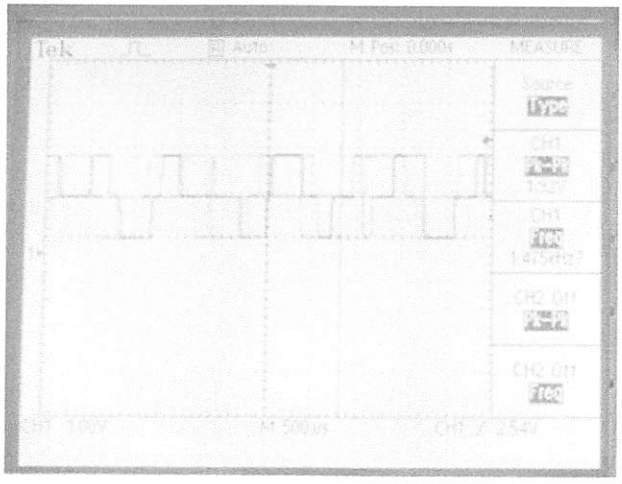
Gambar 4-10 Hasil DTMF tone 6



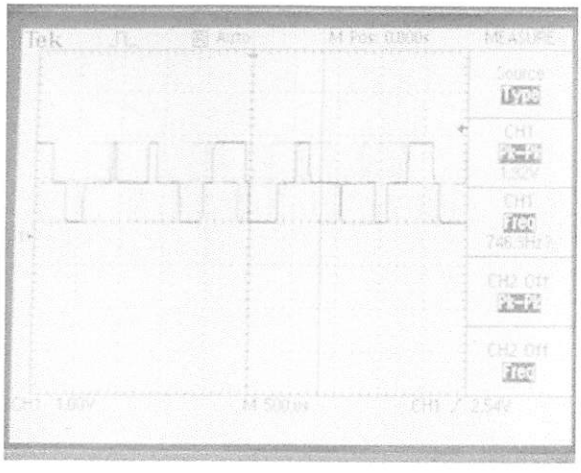
Gambar 4-11 Hasil DTMF tone 7



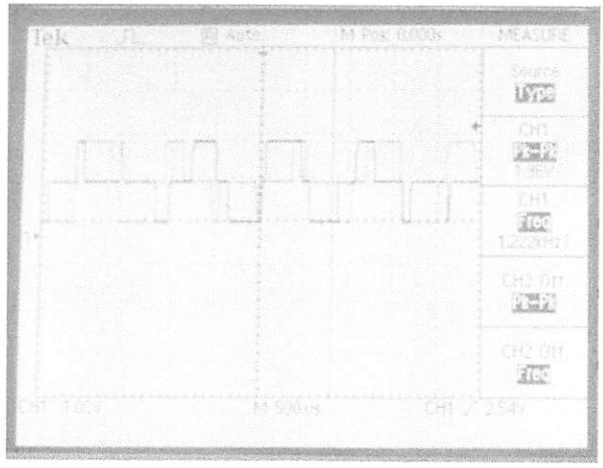
Gambar 4-12 Hasil DTMF tone 8



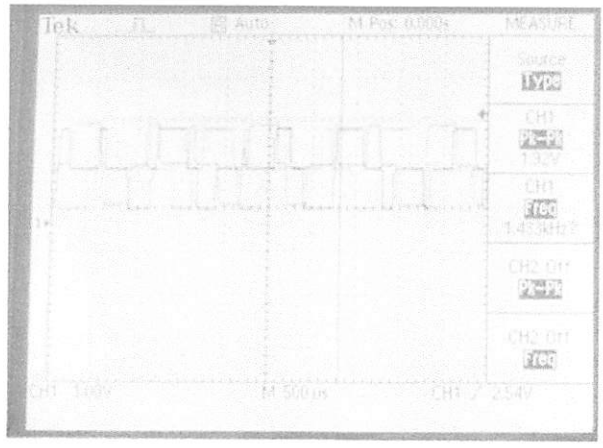
Gambar 4-13 Hasil DTMF tone 9



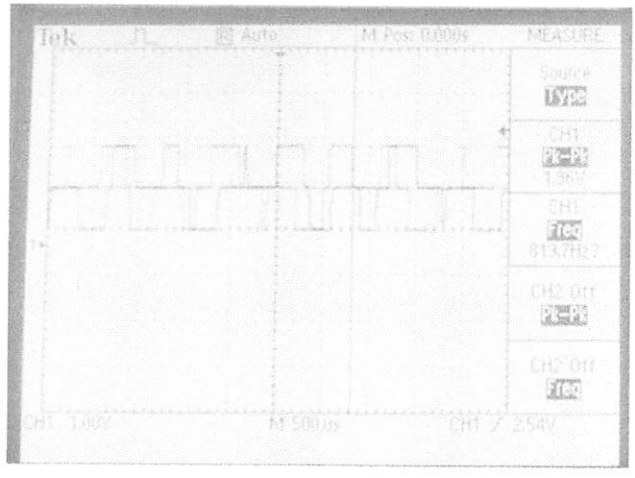
Gambar 4-14 Hasil DTMF tone 10



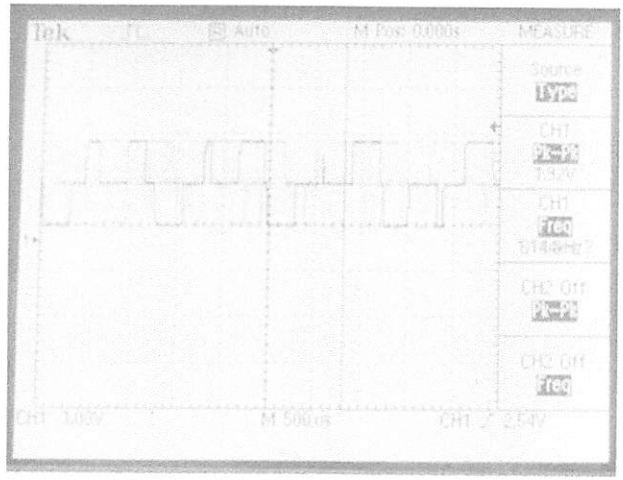
Gambar 4-15 Hasil DTMF tone11



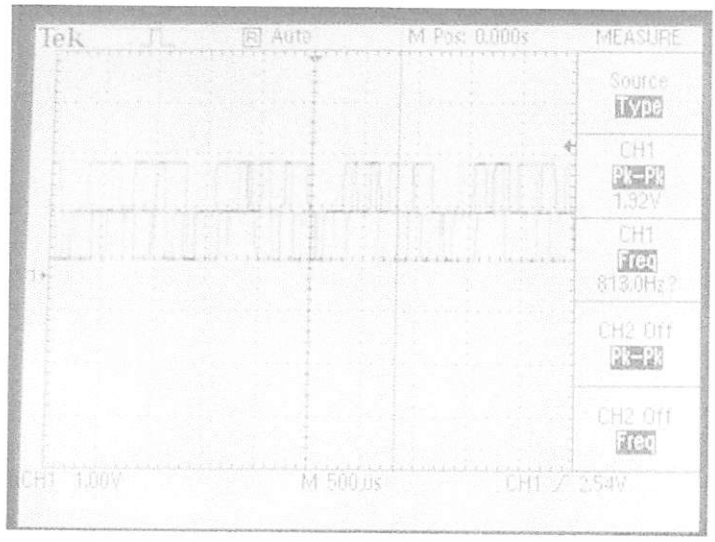
Gambar 4-16 Hasil DTMF tone12



Gambar 4-17 Hasil DTMF tone 13



Gambar 4-18 Hasil DTMF tone 14



Gambar 4-19 Hasil DTMF tone 15

Tabel 4-2 Hasil Pengukuran DTMF

Tombol	LOW	HIGH	DTMF
01	697,3 Hz	1211 KHz	1053 KHz
02	697,3 Hz	1337 KHz	994,0 KHz
03	697,3 Hz	1475 KHz	1031 KHz

04	770,4 Hz	1211 KHz	624,2 KHz
05	770,4 Hz	1337 KHz	674,8 KHz
06	770,4 Hz	1475 KHz	738,6 KHz
07	853,3 Hz	1211 KHz	1099 KHz
08	853,3 Hz	1337 KHz	1188 KHz
09	853,3 Hz	1475 KHz	1475 KHz
11	941,7 Hz	1211 KHz	1222 KHz
10	941,7 Hz	1337 KHz	746,3 Khz
12	941,7 Hz	1475 KHz	1433 KHz
13	697,3 Hz	1634 KHz	819,7 KHz
14	770,4 Hz	1634 KHz	1144 KHz
15	853,3 Hz	1634 KHz	813,0 KHz
16/00	941,7 Hz	1634 KHz	827,8 KHz

Tabel 4-8 Hasil Pengujian Frekuensi LOW Secara Keseluruhan

Tombol	Data Frek. LOW	Hasil Pengukuran frek. LOW	Selisih	Error (%)
01	697 Hz	697,3 Hz	0,3	0,00043
02	697 Hz	697,3 Hz	0,3	0,00043
03	697 Hz	697,3 Hz	0,3	0,00043
04	770 Hz	770,4 Hz	0,4	0,00051
05	770 Hz	770,4 Hz	0,4	0,00051

06	770 Hz	770,4 Hz	0,4	0,00051
07	852 Hz	853,3 Hz	1,3	0,00152
08	852 Hz	853,3 Hz	1,3	0,00152
09	852 Hz	853,3 Hz	1,3	0,00152
11	941 Hz	941,7 Hz	0,7	0,00074
10	941 Hz	941,7 Hz	0,7	0,00074
12	941 Hz	941,7 Hz	0,7	0,00074
13	697 Hz	697,3 Hz	0,3	0,00043
14	770 Hz	770,4 Hz	0,4	0,00051
15	852 Hz	853,3 Hz	1,3	0,00152
16/00	941 Hz	941,7 Hz	0,7	0,00074

Dari tabel diatas didapatkan error rata-rata sebagai berikut :

$$\text{Error rata-rata} = \frac{jumlaherror}{banyaknyapercobaan}$$

$$= \frac{0{,}0128}{16} = 0{,}0008\%$$

Dari perhitungan frekuensi low diatas dapat disimpulkan bahwa alat mempunyai kesalahan atau error dalam setiap pengujian sebesar 0,0008%.

Tabel 4-5 Hasil Pengujian Frekuensi HIGH Secara Keseluruhan

Tombol	Data Frek. HIGH	Hasil Pengukuran frek. HIGH	Selisih	Error (%)

01	1209 KHz	1211 KHz	2	0,0016
02	1336 KHz	1337 KHz	1	0,0007
03	1477 KHz	1475 KHz	2	0,0013
04	1209 KHz	1211 KHz	2	0,0016
05	1336 KHz	1337 KHz	1	0,0007
06	1477 KHz	1475 KHz	2	0,0013
07	1209 KHz	1211 KHz	2	0,0016
08	1336 KHz	1337 KHz	1	0,0007
09	1477 KHz	1475 KHz	2	0,0013
11	1209 KHz	1211 KHz	2	0,0016
10	1336 KHz	1337 KHz	1	0,0007
12	1477 KHz	1475 KHz	2	0,0013
13	1633 KHz	1634 KHz	1	0,0006
14	1633 KHz	1634 KHz	1	0,0006
15	1633 KHz	1634 KHz	1	0,0006
16/00	1633 KHz	1634 KHz	1	0,0006

Dari tabel diatas didapatkan error rata-rata sebagai berikut :

$$\text{Error rata-rata} = \frac{jumlaherror}{banyaknyapercobaan}$$

$$= \frac{0,0168}{16} = 0,00105\%$$

Dari perhitungan frekuensi high diatas dapat disimpulkan bahwa alat mempunyai kesalahan atau error dalam setiap pengujian sebesar 0,00105%.

Maka hasil dari keseluruhan pengujian frekuensi low dan frekuensi high yaitu DTMF mempunyai kesalahan atau error sebesar :

$$= \frac{0.0008 - 0.00105}{2} = 0,000925\%$$

BAB V

PENUTUP

5.1 Kesimpulan

Dari pengamatan dan analisa selama proses perancangan dan pembuatan alat dapat diambil beberapa kesimpulan sebagai berikut :

1. Pada alat ini tidak mampu membuat sinyal sinus karena mikrokontrolernya yang digunakan cuma 1 (satu) sehingga sinyal yang dihasilkan dari alat ini adalah sinyal kotak yang bisa diterima dengan baik oleh DTMF MT 8870 sebagai demodulator.
2. Mikrokontroler dapat membentuk frekuensi high dan low dengan sistem DDS yang dapat diterjemahkan MT 8870.
3. Maka hasil dari keseluruhan pengujian pada alat ini mempunyai kesalahan atau eror sebesar 0,000925%

5.2 Saran- saran

Ada beberapa hal yang perlu diperhatikan dalam pengembangan alat ini, antara lain :

1. Agar alat ini dapat bekerja dengan baik, diharapkan untuk mengikuti petunjuk pengoperasian alat dengan benar
2. Dalam mengembangkan alat ini lebih lanjut bisa ditambahkan sistem wireless untuk komunikasi jarak jauh.

3. Agar hasil bentuk gelombang DTMF baik diharapkan menggunakan 2 (dua) mikrokontroler yang berfungsi untuk membuat frekuensi low dan frekuensi high.

DAFTAR PUSTAKA

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lampiran

INSTITUT TEKNOLOGI NASIONAL
FAKULTAS TEKNOLOGI INDUSTRI
JURUSAN TEKNIK ELEKTRO S-1
Jl. Karanglo KM. 2 Malang

FORMULIR BIMBINGAN SKRIPSI

: SANTO RUKMONO HADI
: 0017063
imbingan : 24 Oktober 2008 – 24 April 2009
Skripsi : PERENCANAAN DAN PEMBUATAN SISTEM AKUISISI DATA YANG DILENGKAPI DTMF (Dual Tone Multiple Frequency) DENGAN MEMAKAI DDS (Direct Digital Synthesis).

Tanggal	URAIAN	Paraf Pembimbing
13/03 09	Revisi Bab 1 & Bab 2	
17/03 09	Maju alat (Demo)	

Malang,
Dosen Pembimbing I

Ir. F. Yudi Limpraptono, MT.
NIP. 1039500274

INSTITUT TEKNOLOGI NASIONAL
FAKULTAS TEKNOLOGI INDUSTRI
JURUSAN TEKNIK ELEKTRO S-1
Jl. Karanglo KM. 2 Malang

FORMULIR BIMBINGAN SKRIPSI

	: SANTO RUKMONO HADI
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Tanggal	URAIAN	Paraf Pembimbing
6/12 2008	maju alat skripsi	
8/01 09	Revisi Bab 3 & Bab 4	

Malang,
Dosen Pembimbing II

Sotyohadi, ST.
NIP. 1039700309

INSTITUT TEKNOLOGI NASIONAL MALANG
FAKULTAS TEKNOLOGI INDUSTRI
JURUSAN TEKNIK ELEKTRO

Formulir Perbaikan Ujian Skripsi

Dalam pelaksanaan Ujian Skripsi Janjang Strata 1 Jurusan Teknik Elektro Konsentrasi T. Energi Listrik / T. Elektronika / T.Infokom, maka perlu adanya perbaikan skripsi untuk mahasiswa :

NAMA : Bunto Rahmono H
NIM : 0017063
Perbaikan meliputi :

Gbr 2.11 Rangkaian Pengujian Modulasi

Malang, 23 maret 2009

(M. Ibrahim A, ST)

INSTITUT TEKNOLOGI NASIONAL MALANG
FAKULTAS TEKNIK INDUSTRI
JURUSAN TEKNIK ELEKTRO
Jl.Raya Karanglo Km. 2
Malang

FORMULIR PERBAIKAN UJIAN SKRIPSI

Dalam melaksanakan Ujian Skripsi Jenjang Strata 1 Jurusan Teknik Elektro Konsentrasi Teknik Elektronika, perlu adanya perbaikan skripsi untuk mahasiswa :

Nama	: Santo Rukmono Hadi
NIM	: 00.17.063
Jurusan	: Teknik Elektro S-1
Konsentrasi	: Teknik Elektronika
Masa Bimbingan	: 24 Oktober 2008 – 24 April 2009
Judul skripsi	: Perancangan dan Pembuatan Sistem Akuisisi Data yang Dilengkapi DTMF (Dual Tone Multiple Frequency) Dengan Memakai DDS (*Direct Digital Synthesis*)

No.	Tanggal	Uraian	Paraf
1.	20-10-2008	• Gambar 2-11 Rangkaian Penguat masukan	

Mengetahui,

Dosen Penguji I

Ir. Eko Nurcahyo
NIP. Y. 1028700172

Dosen Penguji II

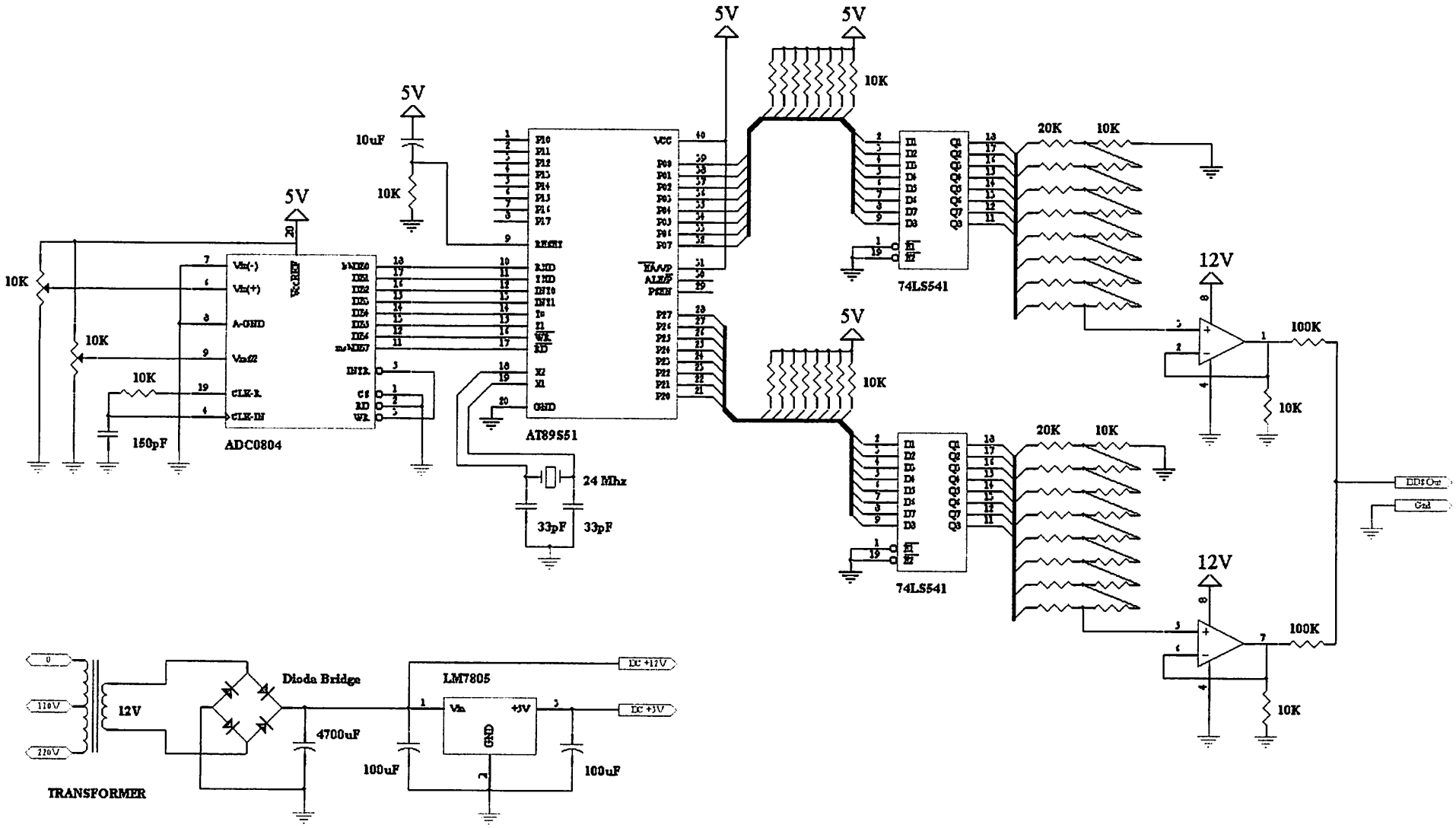
M. Ibrahim Ashari, ST. MT
NIP. Y. 1030100358

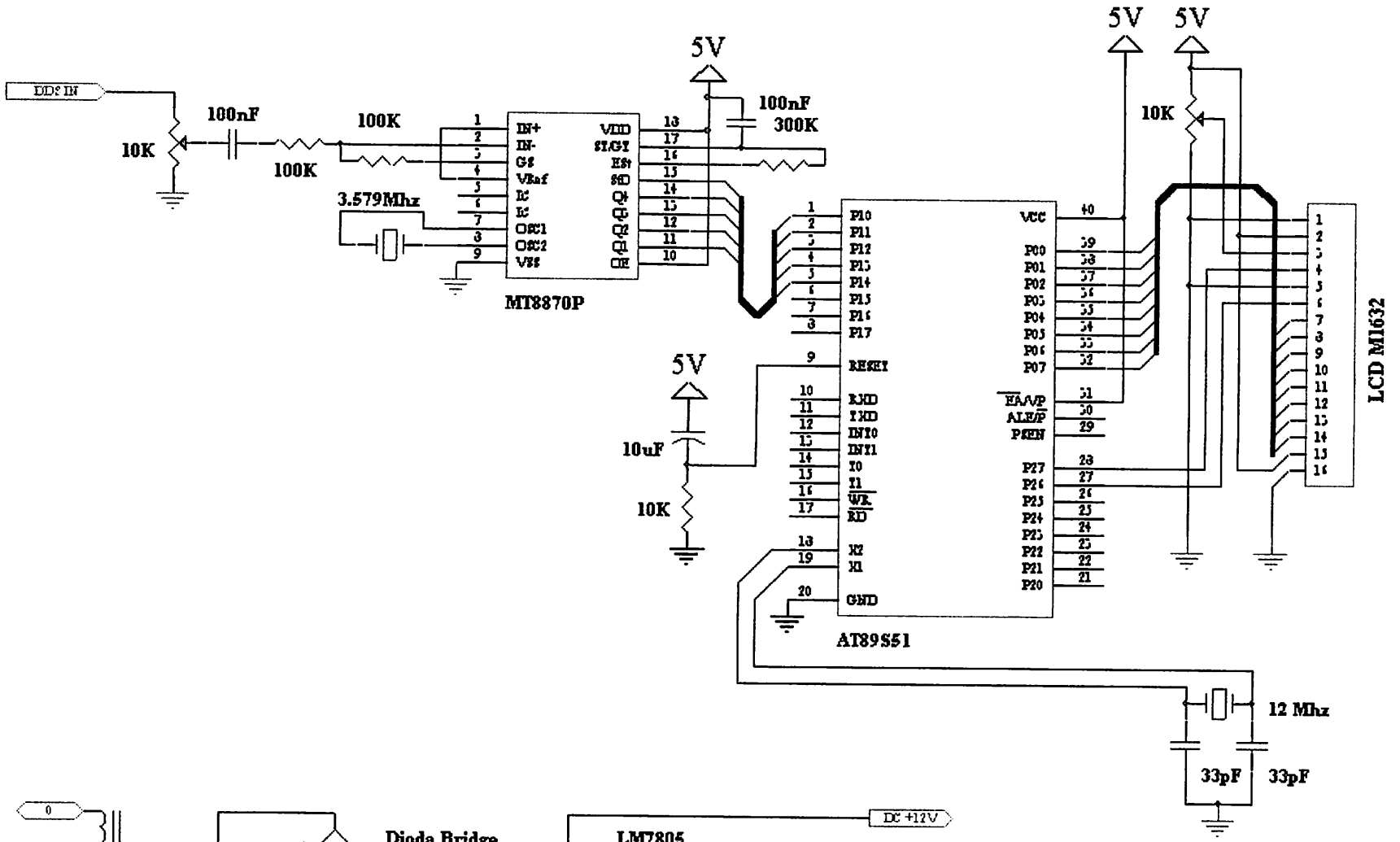
Dosen Pembimbing I

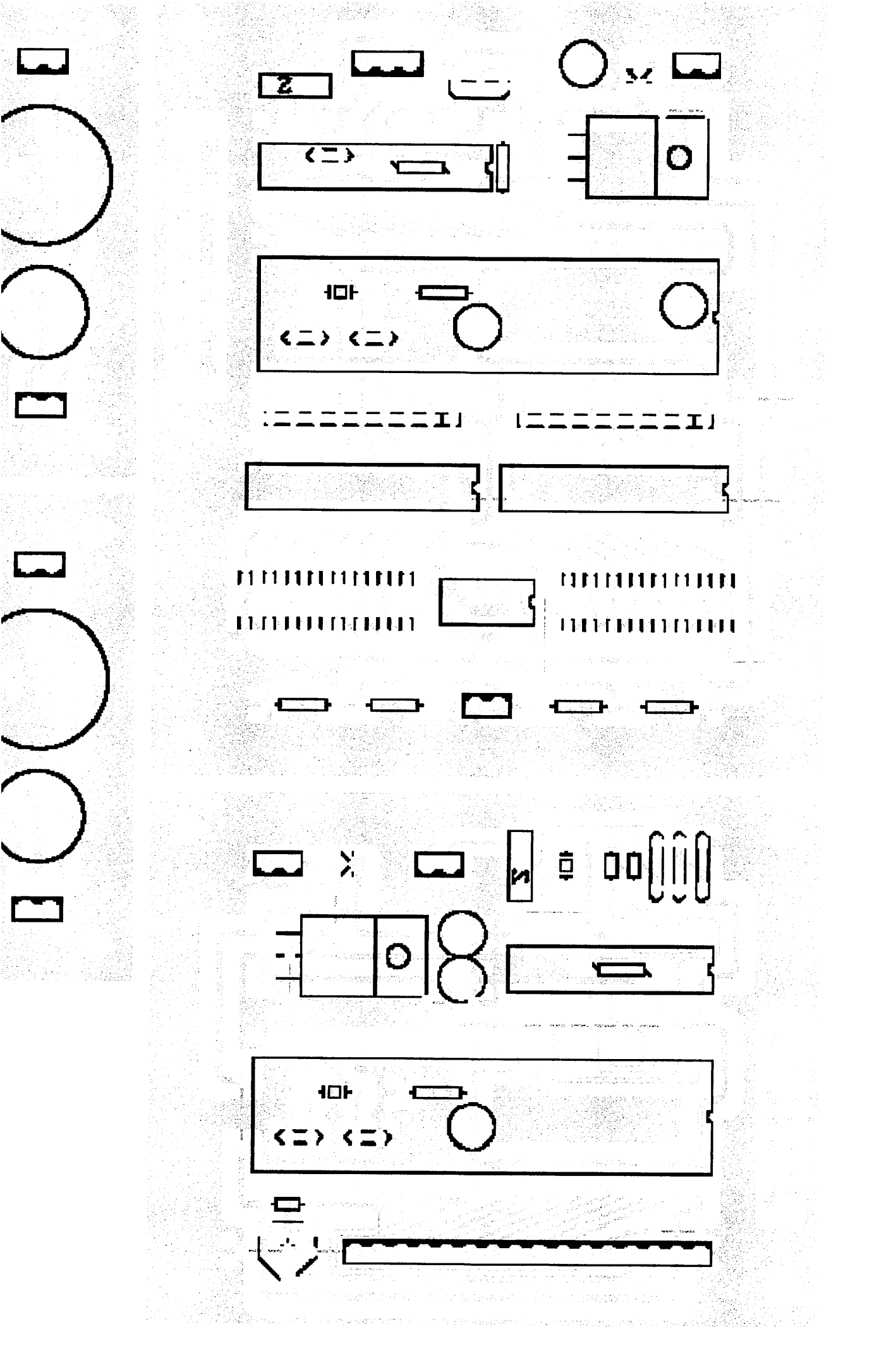
Ir. F. Yudi Limpraptono, MT
NIP. Y. 1039500274

Dosen Pembimbing II

Sotyohadi, ST
NIP.Y. 1039700309


5V
10uF
10K
ADC0804
150pF
AT89S51
24 Mhz
33pF
74LS541
20K
100K
12V
DDS Out
Gnd
TRANSFORMER
0
110V
220V
12V
Dioda Bridge
4700uF
LM7805
Vin
+5V
GND
100uF
DC +12V
DC +5V


DDS IN
10K
100nF
100K
100K
3.579Mhz
MT8870P
5V
100nF
300K
10K
5V
5V
10uF
10K
AT89S51
LCD M1632
12 Mhz
33pF
33pF
0
110V
220V
12V
TRANSFORMER
Dioda Bridge
4700uF
LM7805
Vin
+5V
GND
100uF
100uF
DC +12V
DC +5V



```
        org     00h
        ljmp    init

        org     0Bh
        mov     TL0,Dt0L
        mov     TH0,Dt0H
        clr     TF0
        mov     A,P0
        cpl     A
        mov     P0,A
        reti

        org     1Bh
        mov     TL1,Dt1L
        mov     TH1,Dt1H
        clr     TF1
        mov     A,P2
        cpl     A
        mov     P2,A
        reti

        Dt0L    Equ 30h
        Dt0H    Equ 31h
        Dt1L    Equ 32h
        Dt1H    Equ 33h
        Dlsb    Equ 34h
        Dmsb    Equ 35h
        Dly0    Equ 40h
        Dly1    Equ 41h
        Dly2    Equ 42h

t:      acall   delay1
        acall   tmr_in
        mov     P0,#0
        mov     P2,#0

ai:     mov     A,P3                    ;\
        anl     A,#00001111b            ; |
        mov     Dlsb,A                  ; |
        mov     A,P3                    ; |
        anl     A,#11110000b            ; | cacah data adc
        RR      A                       ; | mjd MSB & LSB
        RR      A                       ; |
        RR      A                       ; |
        RR      A                       ; |
        mov     Dmsb,A                  ;/

        mov     A,Dlsb
        acall   sctone
        mov     A,Dmsb
        acall   sctone

        acall   delay2
        sjmp    mulai

one:    cjne    A,#01,sctn00            ; scan tone
        mov     Dt0L,#06Ch              ; 65536-(1jt/697)       0
        mov     Dt0H,#0FAh              ; 65536-1434=64102
        mov     Dt1L,#0CBh              ; 65536-(1jt/1209)      0
        mov     Dt1H,#0FCh              ; 65536-827=64709
n00:    cjne    A,#02,sctn01
        mov     Dt0L,#06Ch              ; 65536-(1jt/697)       0
        mov     Dt0H,#0FAh              ; 65536-1434=64102
        mov     Dt1L,#019h              ; 65536-(1jt/1336)      1
        mov     Dt1H,#0FDh              ; 65536-749=64787
n01:    cjne    A,#03,sctn02
        mov     Dt0L,#06Ch              ; 65536-(1jt/697)       0
        mov     Dt0H,#0FAh              ; 65536-1434=64102
        mov     Dt1L,#060h              ; 65536-(1jt/1477)      2
        mov     Dt1H,#0FDh              ; 65536-677=64859
n02:    cjne    A,#04,sctn03
        mov     Dt0L,#0F4h              ; 65536-(1jt/770)       1
        mov     Dt0H,#0FAh              ; 65536-1299=FAED
        mov     Dt1L,#0CBh              ; 65536-(1jt/1209)      0
        mov     Dt1H,#0FCh              ; 65536-827=64709
n03:    cjne    A,#05,sctn04
        mov     Dt0L,#0F4h              ; 65536-(1jt/770)       1
        mov     Dt0H,#0FAh              ; 65536-1299=FAED
        mov     Dt1L,#019h              ; 65536-(1jt/1336)      1
```

```
      mov     Dt1H,#0FDh              ; 65536-749=64787
n04:  cjne    A,#06,sctn05
      mov     Dt0L,#0F4h              ; 65536-(1jt/770)       1
      mov     Dt0H,#0FAh              ; 65536-1299=FAED
      mov     Dt1L,#060h              ; 65536-(1jt/1477)      2
      mov     Dt1H,#0FDh              ; 65536-677=64859
n05:  cjne    A,#07,sctn06
      mov     Dt0L,#071h              ; 65536-(1jt/852)       2
      mov     Dt0H,#0FBh              ; 65536-1174=FB6A
      mov     Dt1L,#0CBh              ; 65536-(1jt/1209)      0
      mov     Dt1H,#0FCh              ; 65536-827=64709
n06:  cjne    A,#08,sctn07
      mov     Dt0L,#071h              ; 65536-(1jt/852)       2
      mov     Dt0H,#0FBh              ; 65536-1174=FB6A
      mov     Dt1L,#019h              ; 65536-(1jt/1336)      1
      mov     Dt1H,#0FDh              ; 65536-749=64787
n07:  cjne    A,#09,sctn08
      mov     Dt0L,#071h              ; 65536-(1jt/852)       2
      mov     Dt0H,#0FBh              ; 65536-1174=FB6A
      mov     Dt1L,#060h              ; 65536-(1jt/1477)      2
      mov     Dt1H,#0FDh              ; 65536-677=64859
n08:  cjne    A,#11,sctn09
      mov     Dt0L,#0DFh              ; 65536-(1jt/941)       3
      mov     Dt0H,#0FBh              ; 65536-1063=FBD9
      mov     Dt1L,#0CBh              ; 65536-(1jt/1209)      0
      mov     Dt1H,#0FCh              ; 65536-827=64709
n09:  cjne    A,#10,sctn10
      mov     Dt0L,#0DFh              ; 65536-(1jt/941)       3
      mov     Dt0H,#0FBh              ; 65536-1063=FBD9
      mov     Dt1L,#019h              ; 65536-(1jt/1336)      1
      mov     Dt1H,#0FDh              ; 65536-749=64787
n10:  cjne    A,#12,sctn11
      mov     Dt0L,#0DFh              ; 65536-(1jt/941)       3
      mov     Dt0H,#0FBh              ; 65536-1063=FBD9
      mov     Dt1L,#060h              ; 65536-(1jt/1477)      2
      mov     Dt1H,#0FDh              ; 65536-677=64859
n11:  cjne    A,#13,sctn12
      mov     Dt0L,#06Ch              ; 65536-(1jt/697)       0
      mov     Dt0H,#0FAh              ; 65536-1434=64102
      mov     Dt1L,#0A2h              ; 65536-(1jt/1633)      3
      mov     Dt1H,#0FDh              ; 65536-612=64924
n12:  cjne    A,#14,sctn13
      mov     Dt0L,#0F4h              ; 65536-(1jt/770)       1
      mov     Dt0H,#0FAh              ; 65536-1299=FAED
      mov     Dt1L,#0A2h              ; 65536-(1jt/1633)      3
      mov     Dt1H,#0FDh              ; 65536-612=64924
n13:  cjne    A,#15,sctn14
      mov     Dt0L,#071h              ; 65536-(1jt/852)       2
      mov     Dt0H,#0FBh              ; 65536-1174=FB6A
      mov     Dt1L,#0A2h              ; 65536-(1jt/1633)      3
      mov     Dt1H,#0FDh              ; 65536-612=64924
n14:  cjne    A,#00,sctn15
      mov     Dt0L,#0DFh              ; 65536-(1jt/941)       3
      mov     Dt0H,#0FBh              ; 65536-1063=FBD9
      mov     Dt1L,#0A2h              ; 65536-(1jt/1633)      3
      mov     Dt1H,#0FDh              ; 65536-612=64924
n15:  setb    TR0
      setb    TR1
      acall   delay1
      clr     TR0
      clr     TR1
      acall   delay1
      ret

in:   mov     TMOD,#11h
      mov     TL0,#000h
      mov     TH0,#000h
      mov     TL1,#000h
      mov     TH1,#000h
      setb    EA
      setb    ET0
      clr     TF0
      setb    TR0
      setb    ET1
      clr     TF1
      setb    TR1
      ret

y0:   djnz    Dly0,delay0
```

```
      ret

lay1: acall   delay0
      djnz    Dly1,delay1
      ret

lay2: mov     Dly2,#5
y2:   acall   delay1
      djnz    Dly2,dely2
      ret

      end
```

```
        org     00h

        DTRq    Bit P1.4
        Rest    Bit P2.6
        Enbl    Bit P2.7
        Char    Equ 30h
        Dlsb    Equ 31h
        Dmsb    Equ 32h
        Dly0    Equ 33h
        Dly1    Equ 34h
        Dly2    Equ 35h

t:      acall   lcd_in

ai:     mov     DPTR,#nama
        acall   line1
        mov     Char,#16
        acall   tulis
        mov     DPTR,#nim
        acall   line2
        mov     Char,#16
        acall   tulis
        acall   delay2
        mov     DPTR,#jur
        acall   line1
        mov     Char,#16
        acall   tulis
        mov     DPTR,#univ
        acall   line2
        mov     Char,#16
        acall   tulis
        acall   delay2
        mov     DPTR,#judul
        acall   line1
        mov     Char,#16
        acall   tulis
        mov     DPTR,#dtaadc
        acall   line2
        mov     Char,#16
        acall   tulis

)0:     jnb     DTRq,loop0
        mov     A,P1
        anl     A,#15
        mov     Dlsb,A
)1:     jb      DTRq,loop1

)2:     jnb     DTRq,loop2
        mov     A,P1
        anl     A,#15
        mov     Dmsb,A
)3:     jb      DTRq,loop3

        mov     A,Dmsb
        RR      A
        RR      A
        RR      A
        RR      A
        orl     A,Dlsb

        mov     DPTR,#angka
        mov     P0,#0CCh
        acall   w_ins
        mov     B,#100
        div     AB
        acall   wr_chr
        mov     A,B
        mov     B,#10
        div     AB
        acall   wr_chr
        mov     A,B
        acall   wr_chr
        mov     P0,#0D0h
        acall   w_ins
        acall   delay1
        acall   delay1
        acall   delay1
        acall   delay1
```

```
      sjmp    loop0

ie1:  mov     P0,#080h
      acall   w_ins
      ret

ie2:  mov     P0,#0C0h
      acall   w_ins
      ret

is:   clr     A
      acall   wr_chr
      inc     DPTR
      djnz    Char,tulis
      ret

chr:  movc    A,@A+DPTR
      mov     P0,A
      acall   w_chr
      ret

ns:   clr     Enbl
      clr     Rest
      setb    Enbl
      clr     Enbl
      acall   delay0
      acall   delay0
      ret

hr:   clr     Enbl
      setb    Rest
      setb    Enbl
      clr     Enbl
      acall   delay0
      acall   delay0
      ret

_in:  acall   delay1
      mov     P0,#01h                 ; Display Clear
      acall   w_ins
      mov     P0,#38h                 ; Function Set
      acall   w_ins
      mov     P0,#0Dh                 ; Display On, Cursor, Blink
      acall   w_ins
      mov     P0,#06h                 ; Entry Mode
      acall   w_ins
      mov     P0,#02h                 ; Cursor Home
      acall   w_ins
      ret

:lr:  mov     P0,#01h                 ; Display Clear
      acall   w_ins
      acall   delay0
      acall   delay0
      acall   delay0
      acall   delay0
      acall   delay0
      ret

ıy0:  djnz    Dly0,delay0
      ret

.y1:  acall   delay0
      djnz    Dly1,delay1
      ret

.y2:  mov     Dly2,#40
2:    acall   delay1
      djnz    Dly2,dely2
      ret

.y3:  mov     Dly2,#5
3:    acall   delay0
      djnz    Dly2,dely3
      ret

.:    DB      '  Santo R Hadi  '
      DB      '   000.17.063   '
      DB      ' Teknik Elektro '
```

```
v:   DB      '   ITN Malang   '
lul: DB      ' Akuisisi  Data '
adc: DB      ' Data ADC : 000 '
ka:  DB      '0123456789      '
ong: DB      '                '

     end
```

eatures

- Compatible with MCS-51® Products
- K Bytes of In-System Programmable (ISP) Flash Memory
  - Endurance: 1000 Write/Erase Cycles
- .0V to 5.5V Operating Range
- ully Static Operation: 0 Hz to 33 MHz
- hree-level Program Memory Lock
- 56 x 8-bit Internal RAM
- 2 Programmable I/O Lines
- hree 16-bit Timer/Counters
- ight Interrupt Sources
- ull Duplex UART Serial Channel
- ow-power Idle and Power-down Modes
- nterrupt Recovery from Power-down Mode
- Vatchdog Timer
- ual Data Pointer
- ower-off Flag

escription

e AT89S52 is a low-power, high-performance CMOS 8-bit microcontroller with 8K es of in-system programmable Flash memory. The device is manufactured using nel's high-density nonvolatile memory technology and is compatible with the indus- standard 80C51 instruction set and pinout. The on-chip Flash allows the program mory to be reprogrammed in-system or by a conventional nonvolatile memory pro- mmer. By combining a versatile 8-bit CPU with in-system programmable Flash on nonolithic chip, the Atmel AT89S52 is a powerful microcontroller which provides a hly-flexible and cost-effective solution to many embedded control applications.

e AT89S52 provides the following standard features: 8K bytes of Flash, 256 bytes RAM, 32 I/O lines, Watchdog timer, two data pointers, three 16-bit timer/counters, a -vector two-level interrupt architecture, a full duplex serial port, on-chip oscillator, d clock circuitry. In addition, the AT89S52 is designed with static logic for operation wn to zero frequency and supports two software selectable power saving modes. e Idle Mode stops the CPU while allowing the RAM, timer/counters, serial port, and errupt system to continue functioning. The Power-down mode saves the RAM con- ts but freezes the oscillator, disabling all other chip functions until the next interrupt ardware reset.

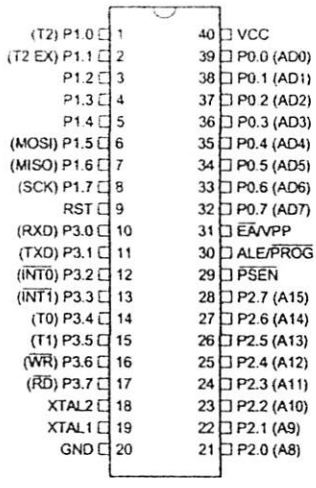
8-bit Microcontroller with 8K Bytes In-System Programmable Flash

AT89S52

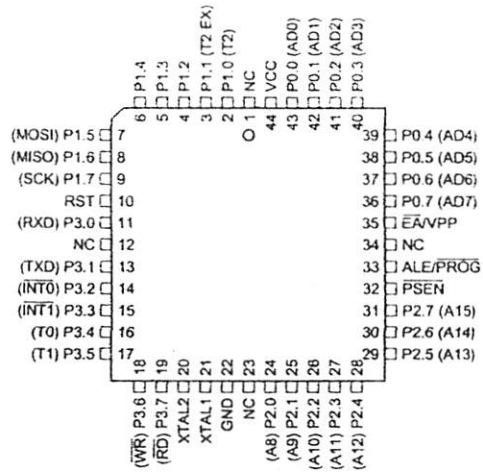
Rev. 1919A-07/01

n Configurations

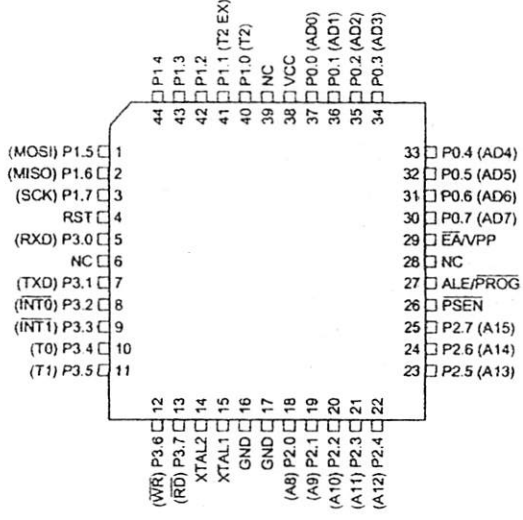
PDIP



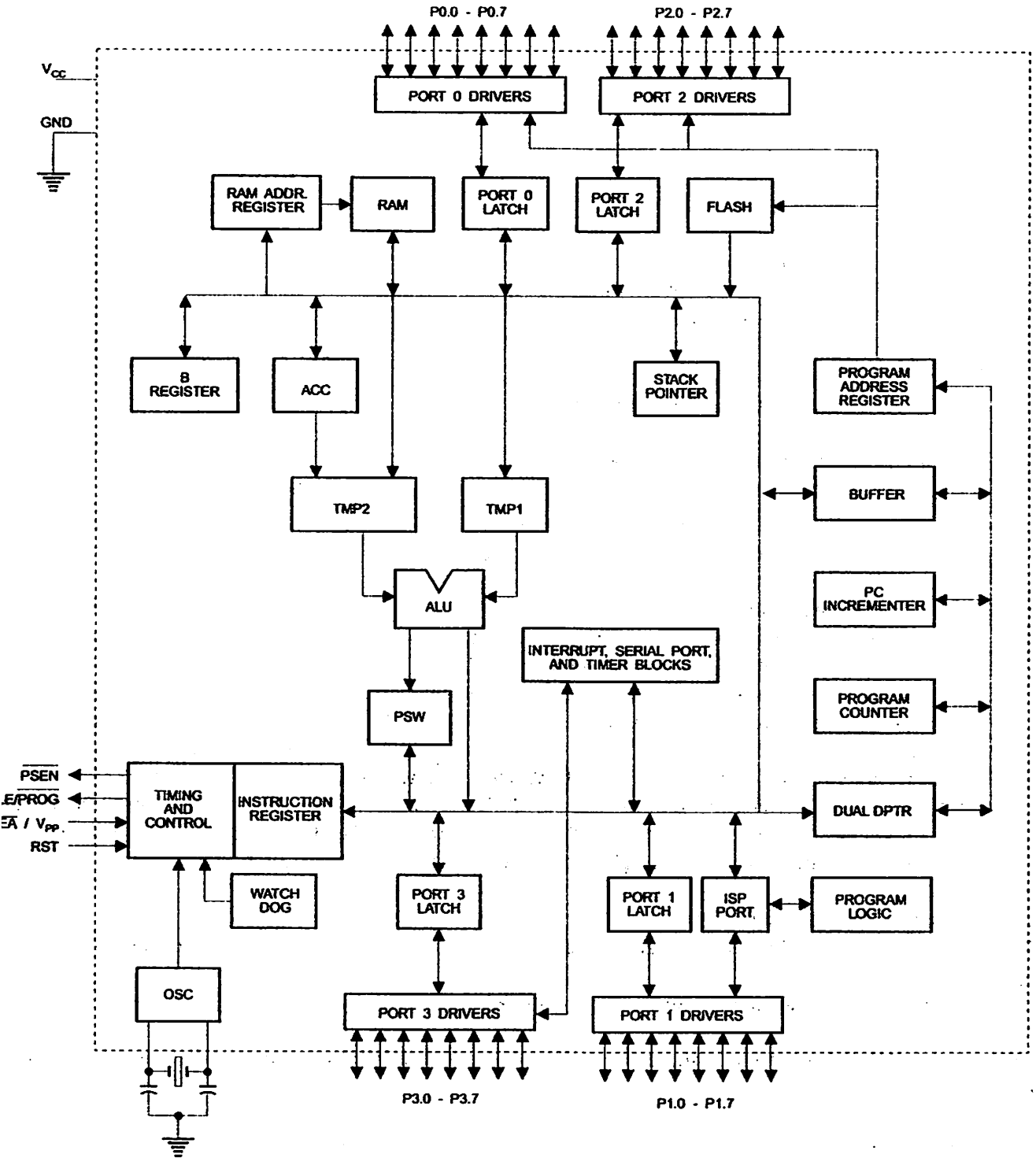
PLCC



TQFP



ock Diagram


P0.0 - P0.7
P2.0 - P2.7
V_{CC}
GND
PORT 0 DRIVERS
PORT 2 DRIVERS
RAM ADDR. REGISTER
RAM
PORT 0 LATCH
PORT 2 LATCH
FLASH
B REGISTER
ACC
STACK POINTER
PROGRAM ADDRESS REGISTER
BUFFER
TMP2
TMP1
ALU
PC INCREMENTER
INTERRUPT, SERIAL PORT, AND TIMER BLOCKS
PSW
PROGRAM COUNTER
PSEN
ALE/PROG
EA / V_{PP}
RST
TIMING AND CONTROL
INSTRUCTION REGISTER
DUAL DPTR
WATCH DOG
PORT 3 LATCH
PORT 1 LATCH
ISP PORT
PROGRAM LOGIC
OSC
PORT 3 DRIVERS
PORT 1 DRIVERS
P3.0 - P3.7
P1.0 - P1.7

in Description

:C

ipply voltage.

ND

ound.

rt 0

rt 0 is an 8-bit open drain bidirectional I/O port. As an tput port, each pin can sink eight TTL inputs. When 1s e written to port 0 pins, the pins can be used as high-pedance inputs.

rt 0 can also be configured to be the multiplexed low-der address/data bus during accesses to external ogram and data memory. In this mode, P0 has internal llups.

rt 0 also receives the code bytes during Flash program-ng and outputs the code bytes during program verifica-n. External pullups are required during program rification.

rt 1

rt 1 is an 8-bit bidirectional I/O port with internal pullups. e Port 1 output buffers can sink/source four TTL inputs. nen 1s are written to Port 1 pins, they are pulled high by e internal pullups and can be used as inputs. As inputs, rt 1 pins that are externally being pulled low will source rrent (I_{IL}) because of the internal pullups.

addition, P1.0 and P1.1 can be configured to be the ier/counter 2 external count input (P1.0/T2) and the ier/counter 2 trigger input (P1.1/T2EX), respectively, as own in the following table.

rt 1 also receives the low-order address bytes during ish programming and verification.

ort Pin	Alternate Functions
1.0	T2 (external count input to Timer/Counter 2), clock-out
1.1	T2EX (Timer/Counter 2 capture/reload trigger and direction control)
1.5	MOSI (used for In-System Programming)
1.6	MISO (used for In-System Programming)
1.7	SCK (used for In-System Programming)

rt 2

rt 2 is an 8-bit bidirectional I/O port with internal pullups. e Port 2 output buffers can sink/source four TTL inputs. nen 1s are written to Port 2 pins, they are pulled high by e internal pullups and can be used as inputs. As inputs, rt 2 pins that are externally being pulled low will source rrent (I_{IL}) because of the internal pullups.

rt 2 emits the high-order address byte during fetches m external program memory and during accesses to external data memory that use 16-bit addresses (MOVX @ DPTR). In this application, Port 2 uses strong internal pullups when emitting 1s. During accesses to external data memory that use 8-bit addresses (MOVX @ RI), Port 2 emits the contents of the P2 Special Function Register.

Port 2 also receives the high-order address bits and some control signals during Flash programming and verification.

Port 3

Port 3 is an 8-bit bidirectional I/O port with internal pullups. The Port 3 output buffers can sink/source four TTL inputs. When 1s are written to Port 3 pins, they are pulled high by the internal pullups and can be used as inputs. As inputs, Port 3 pins that are externally being pulled low will source current (I_{IL}) because of the pullups.

Port 3 also serves the functions of various special features of the AT89S52, as shown in the following table.

Port 3 also receives some control signals for Flash programming and verification.

Port Pin	Alternate Functions
P3.0	RXD (serial input port)
P3.1	TXD (serial output port)
P3.2	$\overline{INT0}$ (external interrupt 0)
P3.3	$\overline{INT1}$ (external interrupt 1)
P3.4	T0 (timer 0 external input)
P3.5	T1 (timer 1 external input)
P3.6	$\overline{WR}$ (external data memory write strobe)
P3.7	$\overline{RD}$ (external data memory read strobe)

RST

Reset input. A high on this pin for two machine cycles while the oscillator is running resets the device. This pin drives High for 96 oscillator periods after the Watchdog times out. The DISRTO bit in SFR AUXR (address 8EH) can be used to disable this feature. In the default state of bit DISRTO, the RESET HIGH out feature is enabled.

ALE/$\overline{PROG}$

Address Latch Enable (ALE) is an output pulse for latching the low byte of the address during accesses to external memory. This pin is also the program pulse input ($\overline{PROG}$) during Flash programming.

In normal operation, ALE is emitted at a constant rate of 1/6 the oscillator frequency and may be used for external timing or clocking purposes. Note, however, that one ALE pulse is skipped during each access to external data memory.

If desired, ALE operation can be disabled by setting bit 0 of SFR location 8EH. With the bit set, ALE is active only during a MOVX or MOVC instruction. Otherwise, the pin is

akly pulled high. Setting the ALE-disable bit has no ect if the microcontroller is in external execution mode.

EN

gram Store Enable ($\overline{PSEN}$) is the read strobe to exter- program memory.

en the AT89S52 is executing code from external pro- m memory, $\overline{PSEN}$ is activated twice each machine le, except that two $\overline{PSEN}$ activations are skipped during h access to external data memory.

/VPP

ernal Access Enable. $\overline{EA}$ must be strapped to GND in er to enable the device to fetch code from external pro- m memory locations starting at 0000H up to FFFFH. Note, however, that if lock bit 1 is programmed, $\overline{EA}$ will be internally latched on reset.

$\overline{EA}$ should be strapped to V_{CC} for internal program executions.

This pin also receives the 12-volt programming enable voltage (V_{PP}) during Flash programming.

XTAL1

Input to the inverting oscillator amplifier and input to the internal clock operating circuit.

XTAL2

Output from the inverting oscillator amplifier.

le 1. AT89S52 SFR Map and Reset Values

0F8H								0FFH
0F0H	B 00000000							0F7H
0E8H								0EFH
0E0H	ACC 00000000							0E7H
0D8H								0DFH
0D0H	PSW 00000000							0D7H
0C8H	T2CON 00000000	T2MOD XXXXXX00	RCAP2L 00000000	RCAP2H 00000000	TL2 00000000	TH2 00000000		0CFH
0C0H								0C7H
0B8H	IP XX000000							0BFH
0B0H	P3 11111111							0B7H
0A8H	IE 0X000000							0AFH
0A0H	P2 11111111		AUXR1 XXXXXXX0				WDTRST XXXXXXXX	0A7H
98H	SCON 00000000	SBUF XXXXXXXX						9FH
90H	P1 11111111							97H
88H	TCON 00000000	TMOD 00000000	TL0 00000000	TL1 00000000	TH0 00000000	TH1 00000000	AUXR XXX00XX0	8FH
80H	P0 11111111	SP 00000111	DP0L 00000000	DP0H 00000000	DP1L 00000000	DP1H 00000000	PCON 0XXX0000	87H

ıecial Function Registers

ıap of the on-chip memory area called the Special Func- Register (SFR) space is shown in Table 1.

:e that not all of the addresses are occupied, and unoc- ıied addresses may not be implemented on the chip. ad accesses to these addresses will in general return dom data, and write accesses will have an indetermi- e effect.

ər software should not write 1s to these unlisted loca- ıs, since they may be used in future products to invoke new features. In that case, the reset or inactive values of the new bits will always be 0.

Timer 2 Registers: Control and status bits are contained in registers T2CON (shown in Table 2) and T2MOD (shown in Table 3) for Timer 2. The register pair (RCAP2H, RCAP2L) are the Capture/Reload registers for Timer 2 in 16-bit capture mode or 16-bit auto-reload mode.

Interrupt Registers: The individual interrupt enable bits are in the IE register. Two priorities can be set for each of the six interrupt sources in the IP register.

ıle 2. T2CON – Timer/Counter 2 Control Register

T2CON Address = 0C8H — Reset Value = 0000 0000B

Bit Addressable

Bit	TF2	EXF2	RCLK	TCLK	EXEN2	TR2	C/$\overline{T2}$	CP/$\overline{RL2}$
	7	6	5	4	3	2	1	0

ymbol	Function
F2	Timer 2 overflow flag set by a Timer 2 overflow and must be cleared by software. TF2 will not be set when either RCLK = 1 or TCLK = 1.
XF2	Timer 2 external flag set when either a capture or reload is caused by a negative transition on T2EX and EXEN2 = 1. When Timer 2 interrupt is enabled, EXF2 = 1 will cause the CPU to vector to the Timer 2 interrupt routine. EXF2 must be cleared by software. EXF2 does not cause an interrupt in up/down counter mode (DCEN = 1).
CLK	Receive clock enable. When set, causes the serial port to use Timer 2 overflow pulses for its receive clock in serial port Modes 1 and 3. RCLK = 0 causes Timer 1 overflow to be used for the receive clock.
CLK	Transmit clock enable. When set, causes the serial port to use Timer 2 overflow pulses for its transmit clock in serial port Modes 1 and 3. TCLK = 0 causes Timer 1 overflows to be used for the transmit clock.
XEN2	Timer 2 external enable. When set, allows a capture or reload to occur as a result of a negative transition on T2EX if Timer 2 is not being used to clock the serial port. EXEN2 = 0 causes Timer 2 to ignore events at T2EX.
R2	Start/Stop control for Timer 2. TR2 = 1 starts the timer.
$\overline{T2}$	Timer or counter select for Timer 2. C/$\overline{T2}$ = 0 for timer function. C/$\overline{T2}$ = 1 for external event counter (falling edge triggered).
P/$\overline{RL2}$	Capture/Reload select. CP/$\overline{RL2}$ = 1 causes captures to occur on negative transitions at T2EX if EXEN2 = 1. CP/$\overline{RL2}$ = 0 causes automatic reloads to occur when Timer 2 overflows or negative transitions occur at T2EX when EXEN2 = 1. When either RCLK or TCLK = 1, this bit is ignored and the timer is forced to auto-reload on Timer 2 overflow.

ıle 3a. AUXR: Auxiliary Register

JXR	Address = 8EH						Reset Value = XXX00XX0B	
	Not Bit Addressable							
	–	–	–	WDIDLE	DISRTO	–	–	DISALE
Bit	7	6	5	4	3	2	1	0

Reserved for future expansion

SALE Disable/Enable ALE

DISALE	Operating Mode
0	ALE is emitted at a constant rate of 1/6 the oscillator frequency
1	ALE is active only during a MOVX or MOVC instruction

SRTO Disable/Enable Reset out

DISRTO	
0	Reset pin is driven High after WDT times out
1	Reset pin is input only

DIDLE Disable/Enable WDT in IDLE mode

WDIDLE	
0	WDT continues to count in IDLE mode
1	WDT halts counting in IDLE mode

al Data Pointer Registers: To facilitate accessing both ernal and external data memory, two banks of 16-bit ta Pointer Registers are provided: DP0 at SFR address ations 82H-83H and DP1 at 84H-85H. Bit DPS = 0 SFR AUXR1 selects DP0 and DPS = 1 selects DP1. e user should always initialize the DPS bit to the appropriate value before accessing the respective Data Pointer Register.

Power Off Flag: The Power Off Flag (POF) is located at bit 4 (PCON.4) in the PCON SFR. POF is set to "1" during power up. It can be set and reset under software control and is not affected by reset.

ıle 3b. AUXR1: Auxiliary Register 1

JXR1	Address = A2H						Reset Value = XXXXXXX0B	
	Not Bit Addressable							
	–	–	–	–	–	–	–	DPS
Bit	7	6	5	4	3	2	1	0

Reserved for future expansion

PS Data Pointer Register Select

DPS	
0	Selects DPTR Registers DP0L, DP0H
1	Selects DPTR Registers DP1L, DP1H

emory Organization

:S-51 devices have a separate address space for Pro-
m and Data Memory. Up to 64K bytes each of external
gram and Data Memory can be addressed.

ogram Memory

ıe $\overline{EA}$ pin is connected to GND, all program fetches are
cted to external memory.

the AT89S52, if $\overline{EA}$ is connected to V_{CC}, program
hes to addresses 0000H through 1FFFH are directed to
rnal memory and fetches to addresses 2000H through
FFH are to external memory.

ıta Memory

AT89S52 implements 256 bytes of on-chip RAM. The
er 128 bytes occupy a parallel address space to the
cial Function Registers. This means that the upper 128
es have the same addresses as the SFR space but are
sically separate from SFR space.

When an instruction accesses an internal location above address 7FH, the address mode used in the instruction specifies whether the CPU accesses the upper 128 bytes of RAM or the SFR space. Instructions which use direct addressing access of the SFR space.

For example, the following direct addressing instruction accesses the SFR at location 0A0H (which is P2).

```
MOV 0A0H, #data
```

Instructions that use indirect addressing access the upper 128 bytes of RAM. For example, the following indirect addressing instruction, where R0 contains 0A0H, accesses the data byte at address 0A0H, rather than P2 (whose address is 0A0H).

```
MOV @R0, #data
```

Note that stack operations are examples of indirect addressing, so the upper 128 bytes of data RAM are available as stack space.

atchdog Timer
ne-time Enabled with Reset-out)

WDT is intended as a recovery method in situations ere the CPU may be subjected to software upsets. The T consists of a 13-bit counter and the Watchdog Timer set (WDTRST) SFR. The WDT is defaulted to disable n exiting reset. To enable the WDT, a user must write EH and 0E1H in sequence to the WDTRST register R location 0A6H). When the WDT is enabled, it will rement every machine cycle while the oscillator is run-g. The WDT timeout period is dependent on the external ck frequency. There is no way to disable the WDT ept through reset (either hardware reset or WDT over-v reset). When WDT overflows, it will drive an output SET HIGH pulse at the RST pin.

sing the WDT

enable the WDT, a user must write 01EH and 0E1H in quence to the WDTRST register (SFR location 0A6H). en the WDT is enabled, the user needs to service it by ing 01EH and 0E1H to WDTRST to avoid a WDT over-v. The 13-bit counter overflows when it reaches 8191 FFH), and this will reset the device. When the WDT is abled, it will increment every machine cycle while the illator is running. This means the user must reset the T at least every 8191 machine cycles. To reset the T the user must write 01EH and 0E1H to WDTRST. TRST is a write-only register. The WDT counter cannot read or written. When WDT overflows, it will generate an put RESET pulse at the RST pin. The RESET pulse ation is 96xTOSC, where TOSC=1/FOSC. To make the st use of the WDT, it should be serviced in those sec-ns of code that will periodically be executed within the e required to prevent a WDT reset.

DT During Power-down and Idle

Power-down mode the oscillator stops, which means the T also stops. While in Power-down mode, the user es not need to service the WDT. There are two methods exiting Power-down mode: by a hardware reset or via a el-activated external interrupt which is enabled prior to ering Power-down mode. When Power-down is exited h hardware reset, servicing the WDT should occur as it rmally does whenever the AT89S52 is reset. Exiting wer-down with an interrupt is significantly different. The *errupt is held low long enough for the oscillator to stabi-*. When the interrupt is brought high, the interrupt is viced. To prevent the WDT from resetting the device ile the interrupt pin is held low, the WDT is not started il the interrupt is pulled high. It is suggested that the T be reset during the interrupt service for the interrupt ed to exit Power-down mode.

To ensure that the WDT does not overflow within a few states of exiting Power-down, it is best to reset the WDT just before entering Power-down mode.

Before going into the IDLE mode, the WDIDLE bit in SFR AUXR is used to determine whether the WDT continues to count if enabled. The WDT keeps counting during IDLE (WDIDLE bit = 0) as the default state. To prevent the WDT from resetting the AT89S52 while in IDLE mode, the user should always set up a timer that will periodically exit IDLE, service the WDT, and reenter IDLE mode.

With WDIDLE bit enabled, the WDT will stop to count in IDLE mode and resumes the count upon exit from IDLE.

UART

The UART in the AT89S52 operates the same way as the UART in the AT89C51 and AT89C52. For further information on the UART operation, refer to the ATMEL Web site (http://www.atmel.com). From the home page, select 'Products', then '8051-Architecture Flash Microcontroller', then 'Product Overview'.

Timer 0 and 1

Timer 0 and Timer 1 in the AT89S52 operate the same way as Timer 0 and Timer 1 in the AT89C51 and AT89C52. For further information on the timers' operation, refer to the ATMEL Web site (http://www.atmel.com). From the home page, select 'Products', then '8051-Architecture Flash Microcontroller', then 'Product Overview'.

Timer 2

Timer 2 is a 16-bit Timer/Counter that can operate as either a timer or an event counter. The type of operation is selected by bit C/$\overline{T2}$ in the SFR T2CON (shown in Table 2). Timer 2 has three operating modes: capture, auto-reload (up or down counting), and baud rate generator. The modes are selected by bits in T2CON, as shown in Table 3. Timer 2 consists of two 8-bit registers, TH2 and TL2. In the Timer function, the TL2 register is incremented every machine cycle. Since a machine cycle consists of 12 oscillator periods, the count rate is 1/12 of the oscillator frequency.

Table 3. Timer 2 Operating Modes

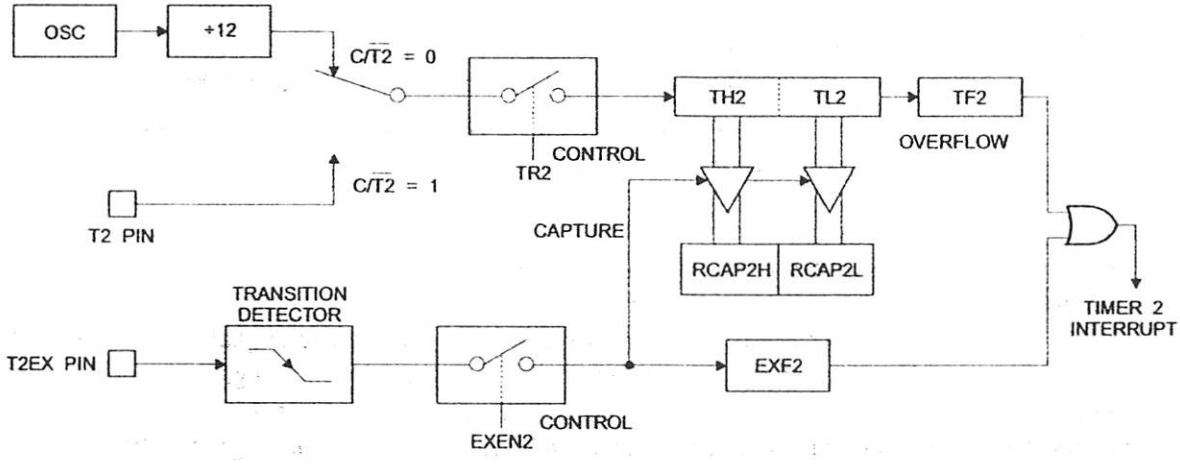
RCLK +TCLK	CP/$\overline{RL2}$	TR2	MODE
0	0	1	16-bit Auto-reload
0	1	1	16-bit Capture
1	X	1	Baud Rate Generator
X	X	0	(Off)

the Counter function, the register is incremented in sponse to a 1-to-0 transition at its corresponding external ut pin, T2. In this function, the external input is sampled ring S5P2 of every machine cycle. When the samples ow a high in one cycle and a low in the next cycle, the unt is incremented. The new count value appears in the ister during S3P1 of the cycle following the one in which transition was detected. Since two machine cycles (24 cillator periods) are required to recognize a 1-to-0 transi-n, the maximum count rate is 1/24 of the oscillator fre-ency. To ensure that a given level is sampled at least ce before it changes, the level should be held for at least e full machine cycle.

apture Mode

the capture mode, two options are selected by bit EN2 in T2CON. If EXEN2 = 0, Timer 2 is a 16-bit timer counter which upon overflow sets bit TF2 in T2CON.

ure 5. Timer in Capture Mode



ure 6 shows Timer 2 automatically counting up when EN=0. In this mode, two options are selected by bit EN2 in T2CON. If EXEN2 = 0, Timer 2 counts up to FFFH and then sets the TF2 bit upon overflow. The erflow also causes the timer registers to be reloaded with 16-bit value in RCAP2H and RCAP2L. The values in ner in Capture ModeRCAP2H and RCAP2L are preset software. If EXEN2 = 1, a 16-bit reload can be triggered her by an overflow or by a 1-to-0 transition at external ut T2EX. This transition also sets the EXF2 bit. Both the 2 and EXF2 bits can generate an interrupt if enabled.

tting the DCEN bit enables Timer 2 to count up or down, shown in Figure 6. In this mode, the T2EX pin controls the direction of the count. A logic 1 at T2EX makes Timer 2 count up. The timer will overflow at 0FFFFH and set the TF2 bit. This overflow also causes the 16-bit value in RCAP2H and RCAP2L to be reloaded into the timer registers, TH2 and TL2, respectively.

A logic 0 at T2EX makes Timer 2 count down. The timer underflows when TH2 and TL2 equal the values stored in RCAP2H and RCAP2L. The underflow sets the TF2 bit and causes 0FFFFH to be reloaded into the timer registers.

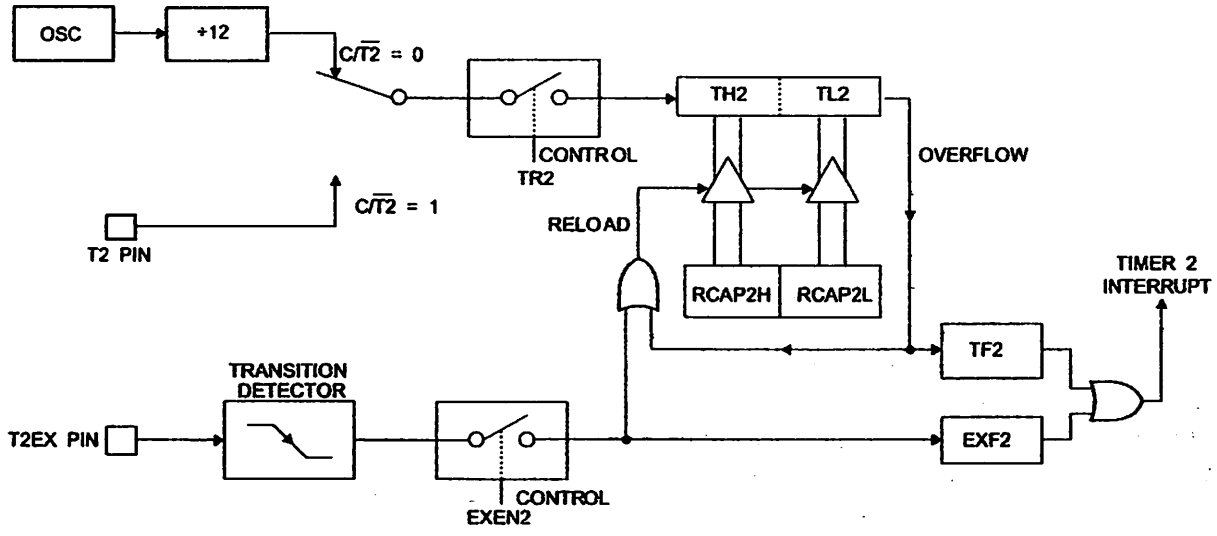
The EXF2 bit toggles whenever Timer 2 overflows or underflows and can be used as a 17th bit of resolution. In this operating mode, EXF2 does not flag an interrupt.

This bit can then be used to generate an interrupt. If EXEN2 = 1, Timer 2 performs the same operation, but a 1-to-0 transition at external input T2EX also causes the current value in TH2 and TL2 to be captured into RCAP2H and RCAP2L, respectively. In addition, the transition at T2EX causes bit EXF2 in T2CON to be set. The EXF2 bit, like TF2, can generate an interrupt. The capture mode is illustrated in Figure 5.

Auto-reload (Up or Down Counter)

Timer 2 can be programmed to count up or down when configured in its 16-bit auto-reload mode. This feature is invoked by the DCEN (Down Counter Enable) bit located in the SFR T2MOD (see Table 4). Upon reset, the DCEN bit is set to 0 so that timer 2 will default to count up. When DCEN is set, Timer 2 can count up or down, depending on the value of the T2EX pin.

ure 6. Timer 2 Auto Reload Mode (DCEN = 0)



ble 4. T2MOD – Timer 2 Mode Control Register

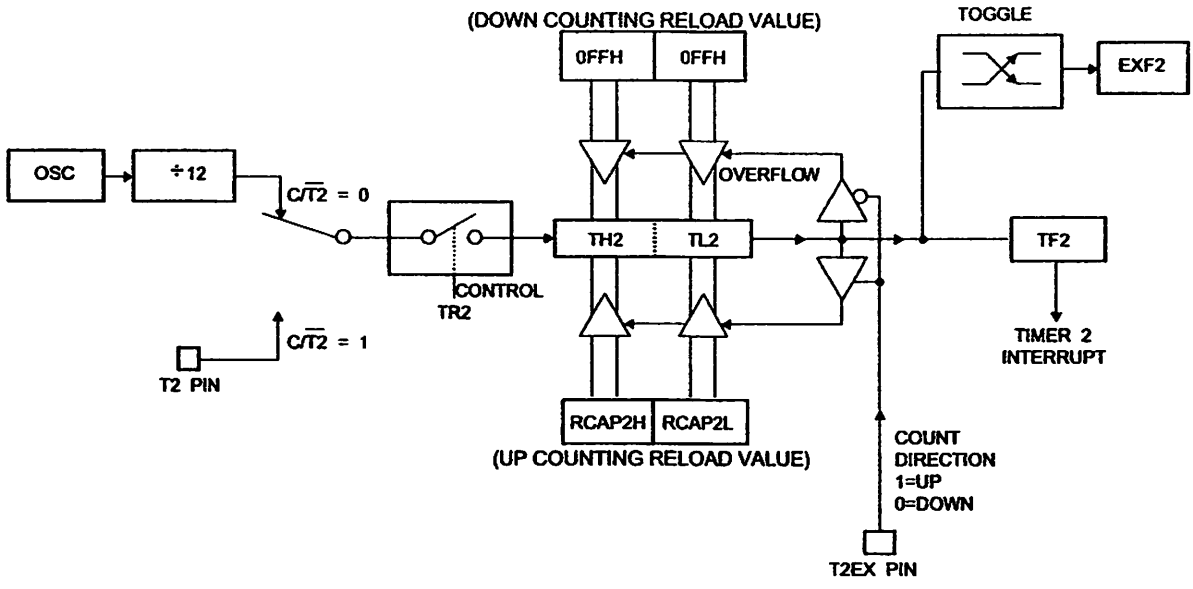
T2MOD Address = 0C9H — Reset Value = XXXX XX00B

Not Bit Addressable

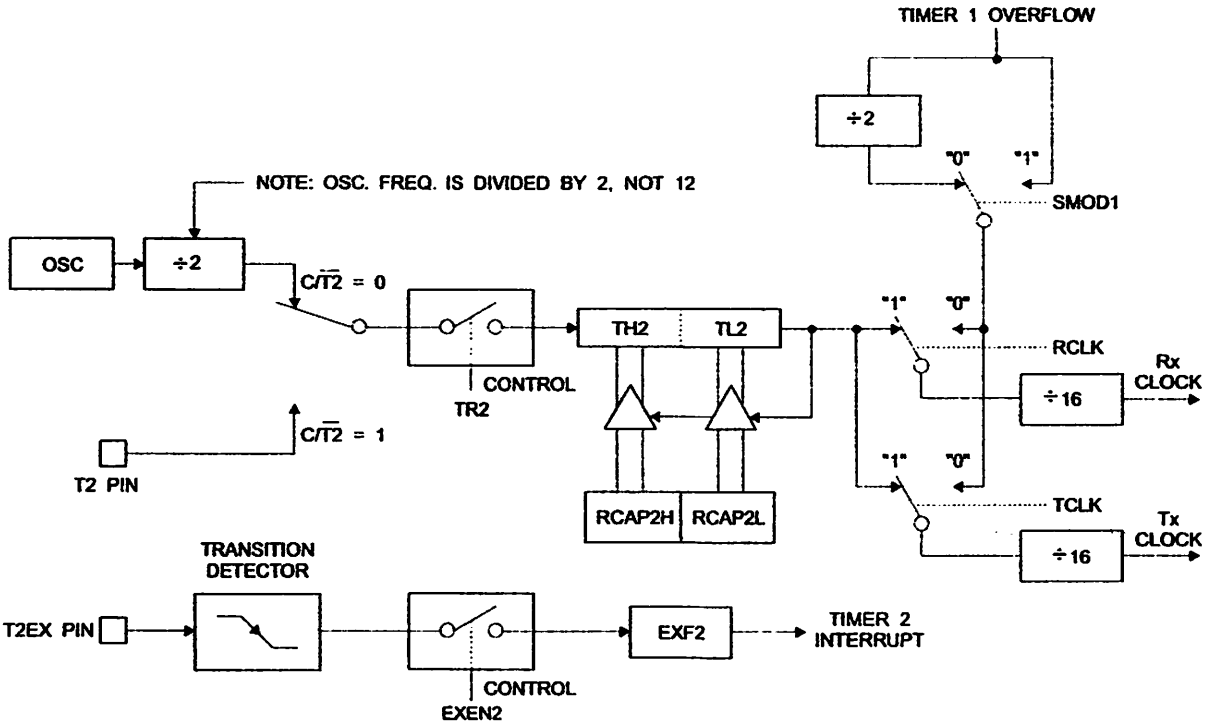
	–	–	–	–	–	–	T2OE	DCEN
Bit	7	6	5	4	3	2	1	0

ymbol	Function
	Not implemented, reserved for future
2OE	Timer 2 Output Enable bit
CEN	When set, this bit allows Timer 2 to be configured as an up/down counter

ure 7. Timer 2 Auto Reload Mode (DCEN = 1)



ure 8. Timer 2 in Baud Rate Generator Mode



ıud Rate Generator

ıer 2 is selected as the baud rate generator by setting LK and/or RCLK in T2CON (Table 2). Note that the ıd rates for transmit and receive can be different if Timer ; used for the receiver or transmitter and Timer 1 is used the other function. Setting RCLK and/or TCLK puts ıer 2 into its baud rate generator mode, as shown in Fig- 8.

ə baud rate generator mode is similar to the auto-reload de, in that a rollover in TH2 causes the Timer 2 registers ɔe reloaded with the 16-bit value in registers RCAP2H ı RCAP2L, which are preset by software.

ə baud rates in Modes 1 and 3 are determined by Timer overflow rate according to the following equation.

$$\text{Modes 1 and 3 Baud Rates} = \frac{\text{Timer 2 Overflow Rate}}{16}$$

ə Timer can be configured for either timer or counter əration. In most applications, it is configured for timer əration ($C/\overline{T2} = 0$). The timer operation is different for ıer 2 when it is used as a baud rate generator. Normally, a timer, it increments every machine cycle (at 1/12 the ;illator frequency). As a baud rate generator, however, it increments every state time (at 1/2 the oscillator frequency). The baud rate formula is given below.

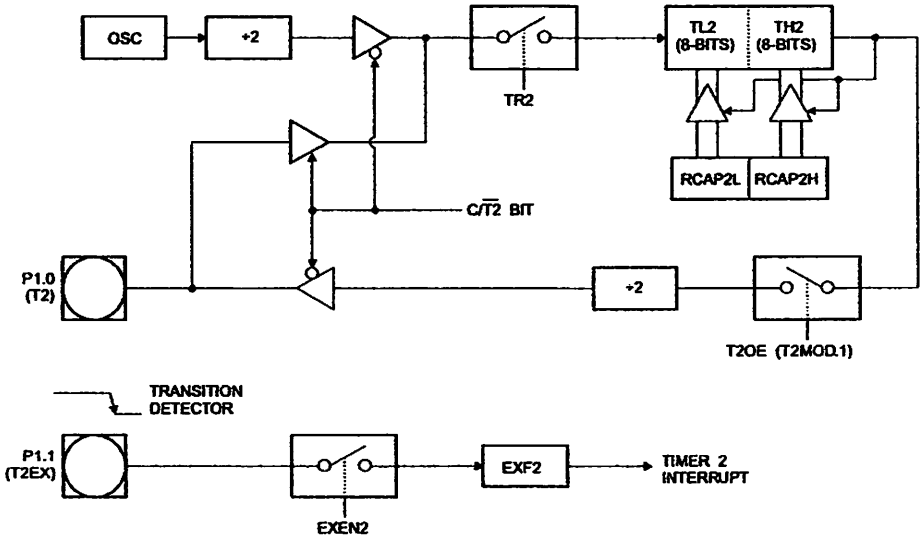
$$\frac{\text{Modes 1 and 3}}{\text{Baud Rate}} = \frac{\text{Oscillator Frequency}}{32 \times [65536\text{-RCAP2H,RCAP2L})]}$$

where (RCAP2H, RCAP2L) is the content of RCAP2H and RCAP2L taken as a 16-bit unsigned integer.

Timer 2 as a baud rate generator is shown in Figure 8. This figure is valid only if RCLK or TCLK = 1 in T2CON. Note that a rollover in TH2 does not set TF2 and will not generate an interrupt. Note too, that if EXEN2 is set, a 1-to-0 transition in T2EX will set EXF2 but will not cause a reload from (RCAP2H, RCAP2L) to (TH2, TL2). Thus, when Timer 2 is in use as a baud rate generator, T2EX can be used as an extra external interrupt.

Note that when Timer 2 is running (TR2 = 1) as a timer in the baud rate generator mode, TH2 or TL2 should not be read from or written to. Under these conditions, the Timer is incremented every state time, and the results of a read or write may not be accurate. The RCAP2 registers may be read but should not be written to, because a write might overlap a reload and cause write and/or reload errors. The timer should be turned off (clear TR2) before accessing the Timer 2 or RCAP2 registers.

ıure 9. Timer 2 in Clock-Out Mode



ɔgrammable Clock Out

)% duty cycle clock can be programmed to come out on), as shown in Figure 9. This pin, besides being a regu- I/O pin, has two alternate functions. It can be pro- nmed to input the external clock for Timer/Counter 2 or utput a 50% duty cycle clock ranging from 61 Hz to 4 z *at a 16 MHz operating frequency.*

ɔnfigure the Timer/Counter 2 as a clock generator, bit 2 (T2CON.1) must be cleared and bit T2OE (T2MOD.1) t be set. Bit TR2 (T2CON.2) starts and stops the timer. clock-out frequency depends on the oscillator fre- ncy and the reload value of Timer 2 capture registers AP2H, RCAP2L), as shown in the following equation.

$$\text{ɔck-Out Frequency} = \frac{\text{Oscillator Frequency}}{4 \times [65536-(\text{RCAP2H,RCAP2L})]}$$

he clock-out mode, Timer 2 roll-overs will not generate interrupt. This behavior is similar to when Timer 2 is d as a baud-rate generator. It is possible to use Timer 2 a baud-rate generator and a clock generator simulta- usly. Note, however, that the baud-rate and clock-out quencies cannot be determined independently from one ther since they both use RCAP2H and RCAP2L.

errupts

AT89S52 has a total of six interrupt vectors: two exter- interrupts ($\overline{INT0}$ and $\overline{INT1}$), three timer interrupts (Tim- 0, 1, and 2), and the serial port interrupt. These rupts are all shown in Figure 10.

h of these interrupt sources can be individually enabled lisabled by setting or clearing a bit in Special Function ister IE. IE also contains a global disable bit, EA, which bles all interrupts at once.

e that Table 5 shows that bit position IE.6 is unimple- nted. In the AT89S52, bit position IE.5 is also unimple- nted. User software should not write 1s to these bit itions, since they may be used in future AT89 products.

er 2 interrupt is generated by the logical OR of bits TF2 I EXF2 in register T2CON. Neither of these flags is ared by hardware when the service routine is vectored In fact, the service routine may have to determine ther it was TF2 or EXF2 that generated the interrupt, I that bit will have to be cleared in software.

Timer 0 and Timer 1 flags, TF0 and TF1, are set at P2 of the cycle in which the timers overflow. The values then polled by the circuitry in the next cycle. However, Timer 2 flag, TF2, is set at S2P2 and is polled in the ne cycle in which the timer overflows.

Table 5. Interrupt Enable (IE) Register

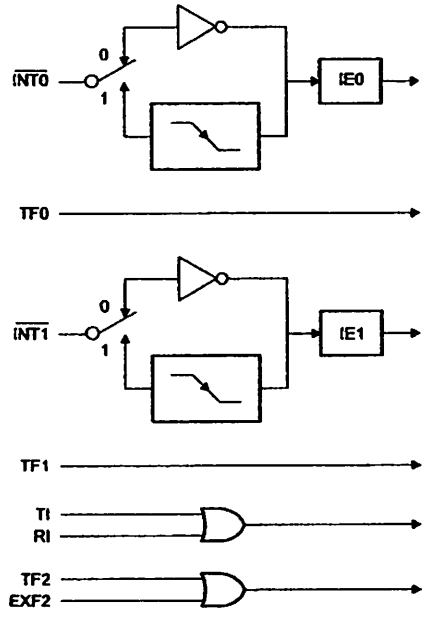
(MSB)							(LSB)
EA	–	ET2	ES	ET1	EX1	ET0	EX0

Enable Bit = 1 enables the interrupt.

Enable Bit = 0 disables the interrupt.

Symbol	Position	Function
EA	IE.7	Disables all interrupts. If EA = 0, no interrupt is acknowledged. If EA = 1, each interrupt source is individually enabled or disabled by setting or clearing its enable bit.
–	IE.6	Reserved.
ET2	IE.5	Timer 2 interrupt enable bit.
ES	IE.4	Serial Port interrupt enable bit.
ET1	IE.3	Timer 1 interrupt enable bit.
EX1	IE.2	External interrupt 1 enable bit.
ET0	IE.1	Timer 0 interrupt enable bit.
EX0	IE.0	External interrupt 0 enable bit.
User software should never write 1s to unimplemented bits, because they may be used in future AT89 products.		

Figure 10. Interrupt Sources



cillator Characteristics

.L1 and XTAL2 are the input and output, respectively, n inverting amplifier that can be configured for use as n-chip oscillator, as shown in Figure 11. Either a quartz tal or ceramic resonator may be used. To drive the ce from an external clock source, XTAL2 should be left nnected while XTAL1 is driven, as shown in Figure 12. re are no requirements on the duty cycle of the external k signal, since the input to the internal clocking circuitry rough a divide-by-two flip-flop, but minimum and maxi- n voltage high and low time specifications must be erved.

e Mode

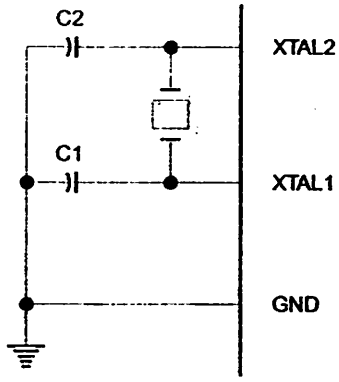
lle mode, the CPU puts itself to sleep while all the on- peripherals remain active. The mode is invoked by ware. The content of the on-chip RAM and all the spe- functions registers remain unchanged during this le. The idle mode can be terminated by any enabled rupt or by a hardware reset.

e that when idle mode is terminated by a hardware t, the device normally resumes program execution where it left off, up to two machine cycles before the nal reset algorithm takes control. On-chip hardware its access to internal RAM in this event, but access to port pins is not inhibited. To eliminate the possibility of inexpected write to a port pin when idle mode is termi- d by a reset, the instruction following the one that kes idle mode should not write to a port pin or to exter- nemory.

wer-down Mode

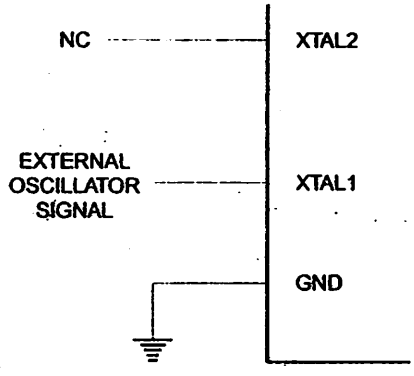
e Power-down mode, the oscillator is stopped, and the uction that invokes Power-down is the last instruction cuted. The on-chip RAM and Special Function Regis- retain their values until the Power-down mode is termi- d. Exit from Power-down mode can be initiated either hardware reset or by an enabled external interrupt. et redefines the SFRs but does not change the on-chip M. The reset should not be activated before V_{CC} is ored to its normal operating level and must be held active long enough to allow the oscillator to restart and stabilize.

Figure 11. Oscillator Connections



Note: C1, C2 = 30 pF ± 10 pF for Crystals
= 40 pF ± 10 pF for Ceramic Resonators

Figure 12. External Clock Drive Configuration



e 6. *Status of External Pins During Idle and Power-down Modes*

de	Program Memory	ALE	$\overline{PSEN}$	PORT0	PORT1	PORT2	PORT3
	Internal	1	1	Data	Data	Data	Data
	External	1	1	Float	Data	Address	Data
ver-down	Internal	0	0	Data	Data	Data	Data
ver-down	External	0	0	Float	Data	Data	Data

ogram Memory Lock Bits

AT89S52 has three lock bits that can be left unpro-mmed (U) or can be programmed (P) to obtain the addi-al features listed in the following table.

le 7. Lock Bit Protection Modes

Program Lock Bits				
	LB1	LB2	LB3	Protection Type
	U	U	U	No program lock features
2	P	U	U	MOVC instructions executed from external program memory are disabled from fetching code bytes from internal memory, $\overline{EA}$ is sampled and latched on reset, and further programming of the Flash memory is disabled
3	P	P	U	Same as mode 2, but verify is also disabled
	P	P	P	Same as mode 3, but external execution is also disabled

en lock bit 1 is programmed, the logic level at the $\overline{EA}$ pin ampled and latched during reset. If the device is pow-d up without a reset, the latch initializes to a random ue and holds that value until reset is activated. The hed value of $\overline{EA}$ must agree with the current logic level iat pin in order for the device to function properly.

ogramming the Flash – Parallel Mode

AT89S52 is shipped with the on-chip Flash memory ly ready to be programmed. The programming interface ds a high-voltage (12-volt) program enable signal and compatible with conventional third-party Flash or ROM programmers.

AT89S52 code memory array is programmed byte-by-e.

gramming Algorithm: Before programming the 89S52, the address, data, and control signals should be up according to the Flash programming mode table and ures 13 and 14. To program the AT89S52, take the fol-ing steps:

Input the desired memory location on the address lines.

Input the appropriate data byte on the data lines.

Activate the correct combination of control signals.

Raise $\overline{EA}/V_{PP}$ to 12V.

Pulse ALE/$\overline{PROG}$ once to program a byte in the Flash array or the lock bits. The byte-write cycle is self-timed and typically takes no more than 50 µs.

Repeat steps 1 through 5, changing the address and data for the entire array or until the end of the object file is reached.

$\overline{Data}$ Polling: The AT89S52 features $\overline{Data}$ Polling to indicate the end of a byte write cycle. During a write cycle, an attempted read of the last byte written will result in the complement of the written data on P0.7. Once the write cycle has been completed, true data is valid on all outputs, and the next cycle may begin. $\overline{Data}$ Polling may begin any time after a write cycle has been initiated.

Ready/$\overline{Busy}$: The progress of byte programming can also be monitored by the RDY/$\overline{BSY}$ output signal. P3.0 is pulled low after ALE goes high during programming to indicate $\overline{BUSY}$. P3.0 is pulled high again when programming is done to indicate READY.

Program Verify: If lock bits LB1 and LB2 have not been programmed, the programmed code data can be read back via the address and data lines for verification. The status of the individual lock bits can be verified directly by reading them back.

Reading the Signature Bytes: The signature bytes are read by the same procedure as a normal verification of locations 000H, 100H, and 200H, except that P3.6 and P3.7 must be pulled to a logic low. The values returned are as follows.

(000H) = 1EH indicates manufactured by Atmel
(100H) = 52H indicates 89S52
(200H) = 06H

Chip Erase: In the parallel programming mode, a chip erase operation is initiated by using the proper combination of control signals and by pulsing ALE/$\overline{PROG}$ low for a duration of 200 ns - 500 ns.

In the serial programming mode, a chip erase operation is initiated by issuing the Chip Erase instruction. In this mode, chip erase is self-timed and takes about 500 ms.

During chip erase, a serial read from any address location will return 00H at the data output.

Programming the Flash – Serial Mode

The Code memory array can be programmed using the serial ISP interface while RST is pulled to V_{CC}. The serial interface consists of pins SCK, MOSI (input) and MISO (output). After RST is set high, the Programming Enable instruction needs to be executed first before other operations can be executed. Before a reprogramming sequence can occur, a Chip Erase operation is required.

The Chip Erase operation turns the content of every memory location in the Code array into FFH.

Either an external system clock can be supplied at pin XTAL1 or a crystal needs to be connected across pins XTAL1 and XTAL2. The maximum serial clock (SCK)

uency should be less than 1/16 of the crystal fre-
ıcy. With a 33 MHz oscillator clock, the maximum SCK
uency is 2 MHz.

ial Programming Algorithm

ırogram and verify the AT89S52 in the serial program-
ı mode, the following sequence is recommended:

Power-up sequence:

Apply power between VCC and GND pins.

Set RST pin to "H".

If a crystal is not connected across pins XTAL1 and XTAL2, apply a 3 MHz to 33 MHz clock to XTAL1 pin and wait for at least 10 milliseconds.

Enable serial programming by sending the Programming Enable serial instruction to pin MOSI/P1.5. The frequency of the shift clock supplied at pin SCK/P1.7 needs to be less than the CPU clock at XTAL1 divided by 16.

The Code array is programmed one byte at a time by supplying the address and data together with the appropriate Write instruction. The write cycle is self-timed and typically takes less than 1 ms at 5V.

4. Any memory location can be verified by using the Read instruction which returns the content at the selected address at serial output MISO/P1.6.
5. At the end of a programming session, RST can be set low to commence normal device operation.

Power-off sequence (if needed):

Set XTAL1 to "L" (if a crystal is not used).

Set RST to "L".

Turn V_{CC} power off.

$\overline{\text{Data}}$ Polling: The $\overline{\text{Data}}$ Polling feature is also available in the serial mode. In this mode, during a write cycle an attempted read of the last byte written will result in the complement of the MSB of the serial output byte on MISO.

Serial Programming Instruction Set

The Instruction Set for Serial Programming follows a 4-byte protocol and is shown in Table 10.

ogramming Interface – Parallel Mode

ry code byte in the Flash array can be programmed by ig the appropriate combination of control signals. The e operation cycle is self-timed and once initiated, will matically time itself to completion.

All major programming vendors offer worldwide support for the Atmel microcontroller series. Please contact your local programming vendor for the appropriate software revision.

le 8. Flash Programming Modes

de	V_{CC}	RST	$\overline{PSEN}$	ALE/ $\overline{PROG}$	$\overline{EA}$/ V_{PP}	P2.6	P2.7	P3.3	P3.6	P3.7	P0.7-0 Data	P2.4-0 Address	P1.7-0 Address
te Code Data	5V	H	L	(2)	12V	L	H	H	H	H	D_{IN}	A12-8	A7-0
ad Code Data	5V	H	L	H	H	L	L	L	H	H	D_{OUT}	A12-8	A7-0
te Lock Bit 1	5V	H	L	(3)	12V	H	H	H	H	H	X	X	X
te Lock Bit 2	5V	H	L	(3)	12V	H	H	H	L	L	X	X	X
te Lock Bit 3	5V	H	L	(3)	12V	H	L	H	H	L	X	X	X
ad Lock Bits , 3	5V	H	L	H	H	H	H	L	H	L	P0.2, P0.3, P0.4	X	X
p Erase	5V	H	L	(1)	12V	H	L	H	L	L	X	X	X
ad Atmel ID	5V	H	L	H	H	L	L	L	L	L	1EH	X 0000	00H
ad Device ID	5V	H	L	H	H	L	L	L	L	L	52H	X 0001	00H
ad Device ID	5V	H	L	H	H	L	L	L	L	L	06H	X 0010	00H

s:
1. Each $\overline{PROG}$ pulse is 200 ns - 500 ns for Chip Erase.
2. Each $\overline{PROG}$ pulse is 200 ns - 500 ns for Write Code Data.
3. Each $\overline{PROG}$ pulse is 200 ns - 500 ns for Write Lock Bits.
4. RDY/$\overline{BSY}$ signal is output on P3.0 during programming.
5. X = don't care.

re 13. Programming the Flash Memory (Parallel Mode)

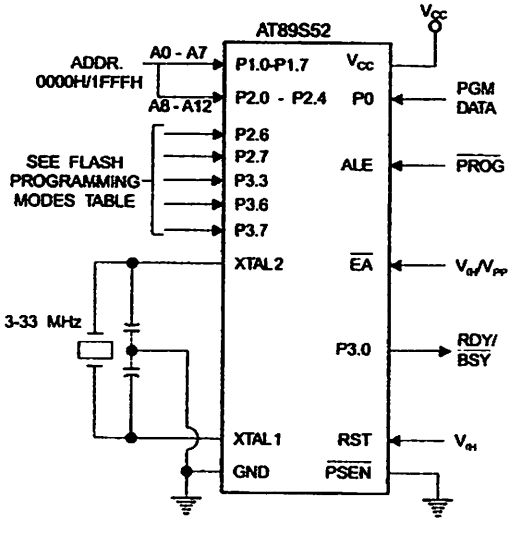
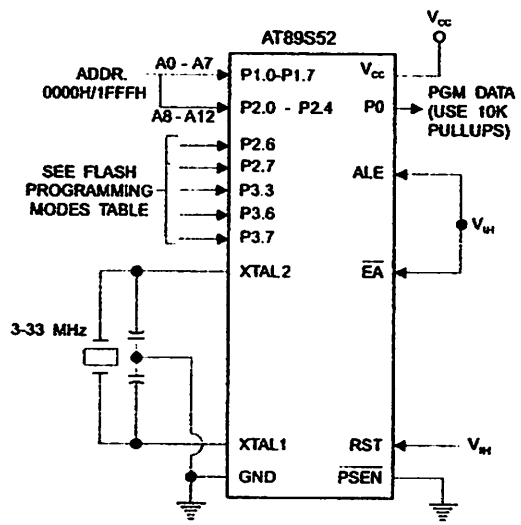


Figure 14. Verifying the Flash Memory (Parallel Mode)

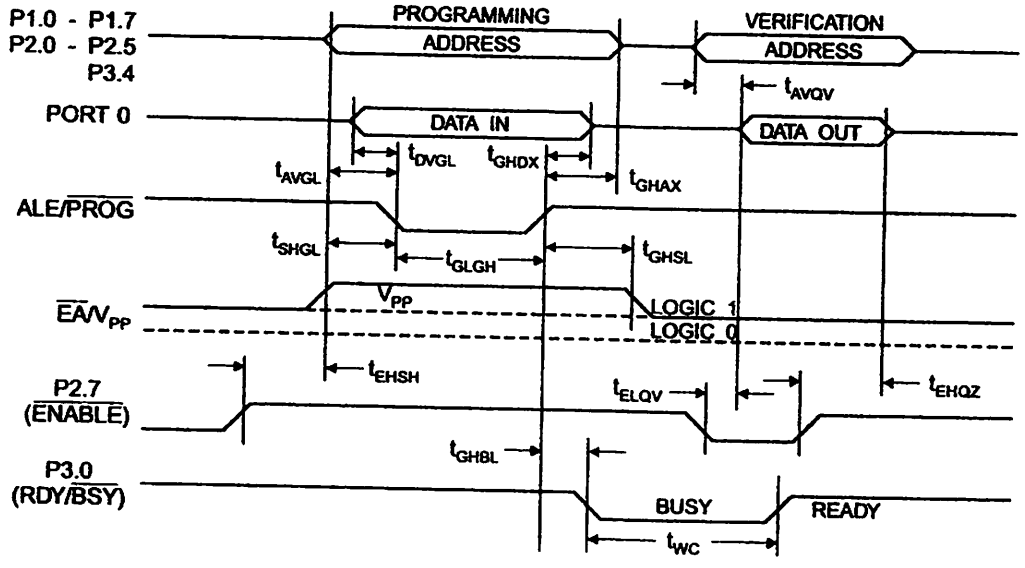


ash Programming and Verification Characteristics (Parallel Mode)

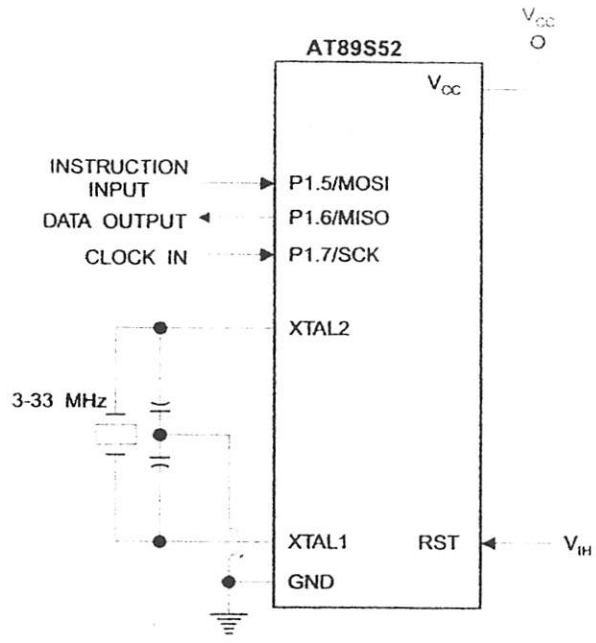
= 20°C to 30°C, V_{CC} = 4.5 to 5.5V

mbol	Parameter	Min	Max	Units
P	Programming Supply Voltage	11.5	12.5	V
	Programming Supply Current		10	mA
	V_{CC} Supply Current		30	mA
CLCL	Oscillator Frequency	3	33	MHz
GL	Address Setup to $\overline{PROG}$ Low	$48t_{CLCL}$		
AX	Address Hold After $\overline{PROG}$	$48t_{CLCL}$		
GL	Data Setup to $\overline{PROG}$ Low	$48t_{CLCL}$		
DX	Data Hold After $\overline{PROG}$	$48t_{CLCL}$		
SH	P2.7 ($\overline{ENABLE}$) High to V_{PP}	$48t_{CLCL}$		
GL	V_{PP} Setup to $\overline{PROG}$ Low	10		µs
SL	V_{PP} Hold After $\overline{PROG}$	10		µs
GH	$\overline{PROG}$ Width	0.2	1	µs
AV	Address to Data Valid		$48t_{CLCL}$	
AV	$\overline{ENABLE}$ Low to Data Valid		$48t_{CLCL}$	
AZ	Data Float After $\overline{ENABLE}$	0	$48t_{CLCL}$	
BL	$\overline{PROG}$ High to $\overline{BUSY}$ Low		1.0	µs
	Byte Write Cycle Time		50	µs

re 15. Flash Programming and Verification Waveforms – Parallel Mode

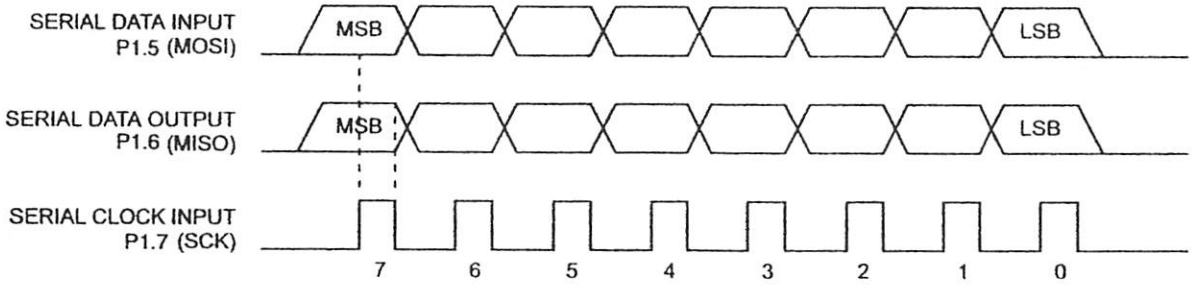


ure 16. Flash Memory Serial Downloading



ash Programming and Verification Waveforms – Serial Mode

ure 17. Serial Programming Waveforms



le 9. Serial Programming Instruction Set

	Instruction Format				
ɜtruction	Byte 1	Byte 2	Byte 3	Byte 4	Operation
ɔgramming Enable	1010 1100	0101 0011	xxxx xxxx	xxxx xxxx 0110 1001 (Output)	Enable Serial Programming while RST is high
ıip Erase	1010 1100	100x xxxx	xxxx xxxx	xxxx xxxx	Chip Erase Flash memory array
ıad Program Memory yte Mode)	0010 0000	xxx A12 A11 A10 A9 A8	A7 A6 A5 A4 A3 A2 A1 A0	D7 D6 D5 D4 D3 D2 D1 D0	Read data from Program memory in the byte mode
rite Program Memory yte Mode)	0100 0000	xxx A12 A11 A10 A9 A8	A7 A6 A5 A4 A3 A2 A1 A0	D7 D6 D5 D4 D3 D2 D1 D0	Write data to Program memory in the byte mode
rite Lock Bits[2]	1010 1100	1110 00 B1 B2	xxxx xxxx	xxxx xxxx	Write Lock bits. See Note (2).
ıad Lock Bits	0010 0100	xxxx xxxx	xxxx xxxx	xx LB3 LB2 LB1 xx	Read back current status of the lock bits (a programmed lock bit reads back as a '1')
ıad Signature Bytes[1]	0010 1000	xxx A5 A4 A3 A2 A1 A0	xxx xxxx	Signature Byte	Read Signature Byte
ɜad Program Memory age Mode)	0011 0000	xxx A12 A11 A10 A9 A8	Byte 0	Byte 1... Byte 255	Read data from Program memory in the Page Mode (256 bytes)
rite Program Memory age Mode)	0101 0000	xxx A12 A11 A10 A9 A8	Byte 0	Byte 1... Byte 255	Write data to Program memory in the Page Mode (256 bytes)

es: 1. The signature bytes are not readable in Lock Bit Modes 3 and 4.

2. B1 = 0, B2 = 0 ---> Mode 1, no lock protection
   B1 = 0, B2 = 1 ---> Mode 2, lock bit 1 activated
   B1 = 1, B2 = 0 ---> Mode 3, lock bit 2 activated
   B1 = 1, B1 = 1 ---> Mode 4, lock bit 3 activated

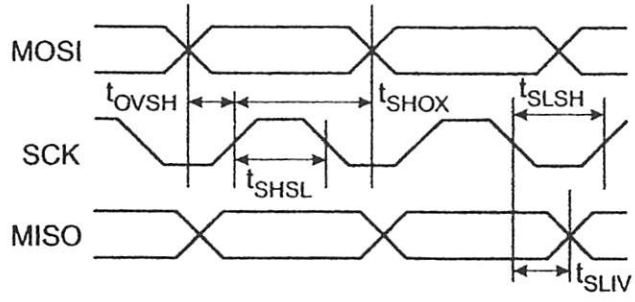
   } Each of the lock bits needs to be activated sequentially before Mode 4 can be executed.

ɜr Reset signal is high, SCK should be low for at least 64 tem clocks before it goes high to clock in the enable a bytes. No pulsing of Reset signal is necessary. SCK ɔuld be no faster than 1/16 of the system clock at AL1.

For Page Read/Write, the data always starts from byte 0 to 255. After the command byte and upper address byte are latched, each byte thereafter is treated as data until all 256 bytes are shifted in/out. Then the next instruction will be ready to be decoded.

rial Programming Characteristics

ure 18. Serial Programming Timing



ble 10. Serial Programming Characteristics, T_A = -40° C to 85° C, V_{CC} = 4.0 - 5.5V (Unless otherwise noted)

ymbol	Parameter	Min	Typ	Max	Units
t_{CLCL}	Oscillator Frequency	0		33	MHz
LCL	Oscillator Period	30			ns
HSL	SCK Pulse Width High	2 t_{CLCL}			ns
LSH	SCK Pulse Width Low	2 t_{CLCL}			ns
VSH	MOSI Setup to SCK High	t_{CLCL}			ns
HOX	MOSI Hold after SCK High	2 t_{CLCL}			ns
LIV	SCK Low to MISO Valid	10	16	32	ns
RASE	Chip Erase Instruction Cycle Time			500	ms
WC	Serial Byte Write Cycle Time			64 t_{CLCL} + 400	µs

ɔsolute Maximum Ratings*

perating Temperature	-55°C to +125°C
orage Temperature	-65°C to +150°C
ltage on Any Pin th Respect to Ground	-1.0V to +7.0V
aximum Operating Voltage	6.6V
C Output Current	15.0 mA

*NOTICE: Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

C Characteristics

values shown in this table are valid for T_A = -40°C to 85°C and V_{CC} = 4.0V to 5.5V, unless otherwise noted.

mbol	Parameter	Condition	Min	Max	Units
	Input Low Voltage	(Except $\overline{EA}$)	-0.5	0.2 V_{CC}-0.1	V
.1	Input Low Voltage ($\overline{EA}$)		-0.5	0.2 V_{CC}-0.3	V
H	Input High Voltage	(Except XTAL1, RST)	0.2 V_{CC}+0.9	V_{CC}+0.5	V
H1	Input High Voltage	(XTAL1, RST)	0.7 V_{CC}	V_{CC}+0.5	V
L	Output Low Voltage[1] (Ports 1,2,3)	I_{OL} = 1.6 mA		0.45	V
L1	Output Low Voltage[1] (Port 0, ALE, $\overline{PSEN}$)	I_{OL} = 3.2 mA		0.45	V
OH	Output High Voltage (Ports 1,2,3, ALE, $\overline{PSEN}$)	I_{OH} = -60 µA, V_{CC} = 5V ± 10%	2.4		V
		I_{OH} = -25 µA	0.75 V_{CC}		V
		I_{OH} = -10 µA	0.9 V_{CC}		V
OH1	Output High Voltage (Port 0 in External Bus Mode)	I_{OH} = -800 µA, V_{CC} = 5V ± 10%	2.4		V
		I_{OH} = -300 µA	0.75 V_{CC}		V
		I_{OH} = -80 µA	0.9 V_{CC}		V
	Logical 0 Input Current (Ports 1,2,3)	V_{IN} = 0.45V		-50	µA
	Logical 1 to 0 Transition Current (Ports 1,2,3)	V_{IN} = 2V, V_{CC} = 5V ± 10%		-650	µA
	Input Leakage Current (Port 0, $\overline{EA}$)	0.45 < V_{IN} < V_{CC}		±10	µA
RST	Reset Pulldown Resistor		10	30	KΩ
D	Pin Capacitance	Test Freq. = 1 MHz, T_A = 25°C		10	pF
	Power Supply Current	Active Mode, 12 MHz		25	mA
		Idle Mode, 12 MHz		6.5	mA
	Power-down Mode[1]	V_{CC} = 5.5V		50	µA

es:
1. Under steady state (non-transient) conditions, I_{OL} must be externally limited as follows:
   Maximum I_{OL} per port pin: 10 mA
   Maximum I_{OL} per 8-bit port:
   Port 0: 26 mA *Ports 1, 2, 3: 15 mA*
   Maximum total I_{OL} for all output pins: 71 mA
   If I_{OL} exceeds the test condition, V_{OL} may exceed the related specification. Pins are not guaranteed to sink current greater than the listed test conditions.
2. Minimum V_{CC} for Power-down is 2V.

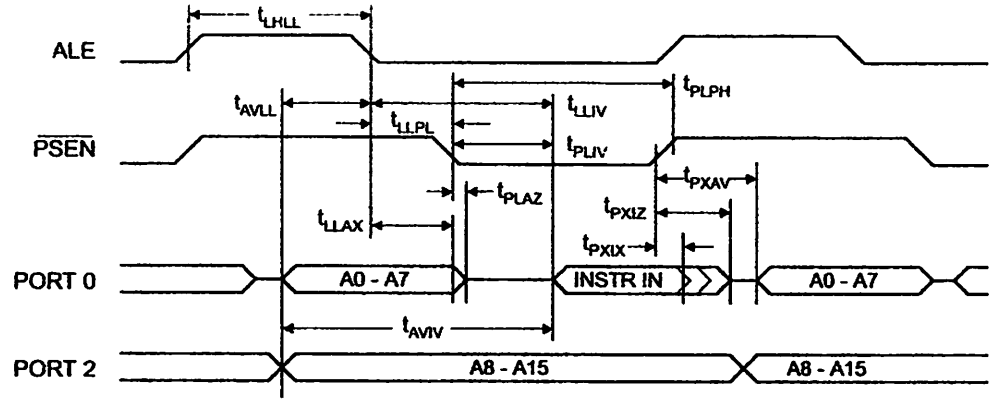
; Characteristics

ler operating conditions, load capacitance for Port 0, ALE/$\overline{PROG}$, and $\overline{PSEN}$ = 100 pF; load capacitance for all other)uts = 80 pF.

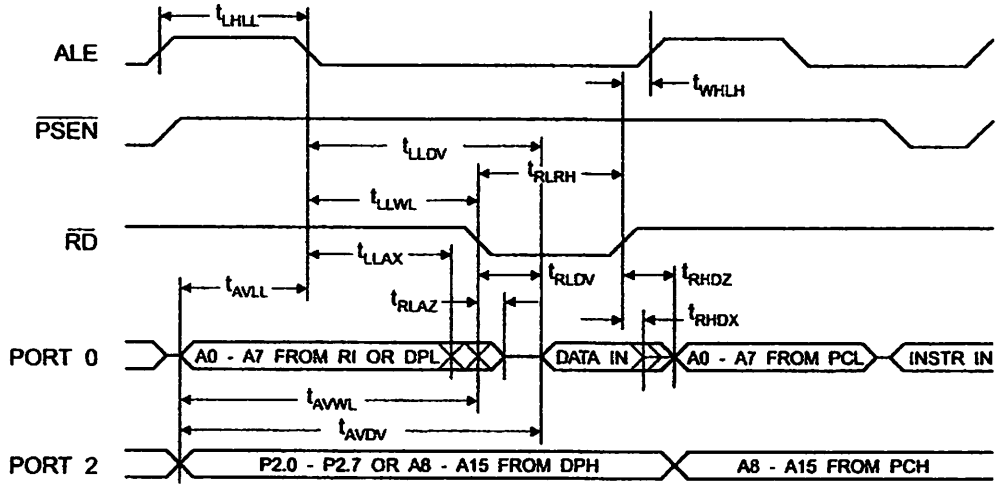
ternal Program and Data Memory Characteristics

mbol	Parameter	12 MHz Oscillator		Variable Oscillator		Units
		Min	Max	Min	Max	
CLCL	Oscillator Frequency			0	33	MHz
LL	ALE Pulse Width	127		$2t_{CLCL}$-40		ns
LL	Address Valid to ALE Low	43		t_{CLCL}-25		ns
AX	Address Hold After ALE Low	48		t_{CLCL}-25		ns
LV	ALE Low to Valid Instruction In		233		$4t_{CLCL}$-65	ns
PL	ALE Low to $\overline{PSEN}$ Low	43		t_{CLCL}-25		ns
PH	$\overline{PSEN}$ Pulse Width	205		$3t_{CLCL}$-45		ns
PV	$\overline{PSEN}$ Low to Valid Instruction In		145		$3t_{CLCL}$-60	ns
PX	Input Instruction Hold After $\overline{PSEN}$	0		0		ns
PZ	Input Instruction Float After $\overline{PSEN}$		59		t_{CLCL}-25	ns
AV	$\overline{PSEN}$ to Address Valid	75		t_{CLCL}-8		ns
AV	Address to Valid Instruction In		312		$5t_{CLCL}$-80	ns
AZ	$\overline{PSEN}$ Low to Address Float		10		10	ns
RH	$\overline{RD}$ Pulse Width	400		$6t_{CLCL}$-100		ns
WH	$\overline{WR}$ Pulse Width	400		$6t_{CLCL}$-100		ns
DV	$\overline{RD}$ Low to Valid Data In		252		$5t_{CLCL}$-90	ns
DX	Data Hold After $\overline{RD}$	0		0		ns
DZ	Data Float After $\overline{RD}$		97		$2t_{CLCL}$-28	ns
QV	ALE Low to Valid Data In		517		$8t_{CLCL}$-150	ns
AV	Address to Valid Data In		585		$9t_{CLCL}$-165	ns
WL	ALE Low to $\overline{RD}$ or $\overline{WR}$ Low	200	300	$3t_{CLCL}$-50	$3t_{CLCL}$+50	ns
WL	Address to $\overline{RD}$ or $\overline{WR}$ Low	203		$4t_{CLCL}$-75		ns
WX	Data Valid to $\overline{WR}$ Transition	23		t_{CLCL}-30		ns
WH	Data Valid to $\overline{WR}$ High	433		$7t_{CLCL}$-130		ns
QX	Data Hold After $\overline{WR}$	33		t_{CLCL}-25		ns
AZ	$\overline{RD}$ Low to Address Float		0		0	ns
LH	$\overline{RD}$ or $\overline{WR}$ High to ALE High	43	123	t_{CLCL}-25	t_{CLCL}+25	ns

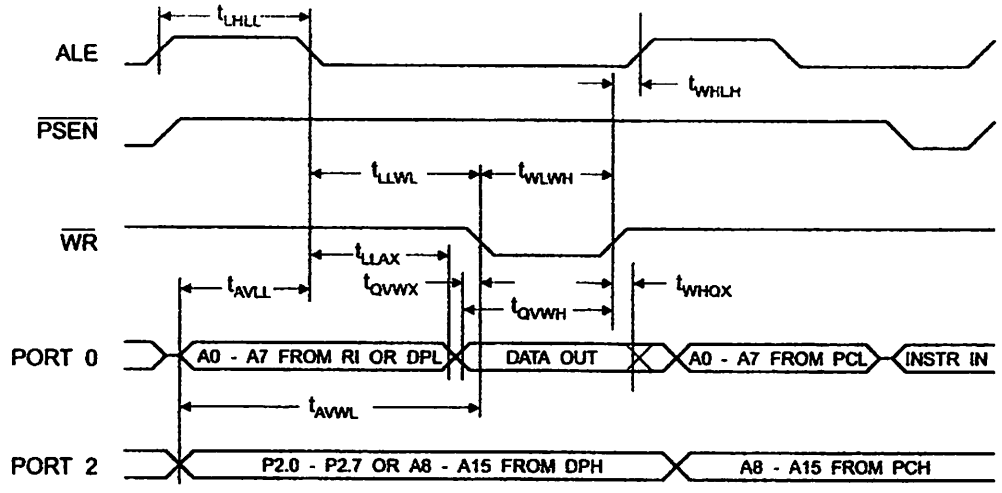
ternal Program Memory Read Cycle



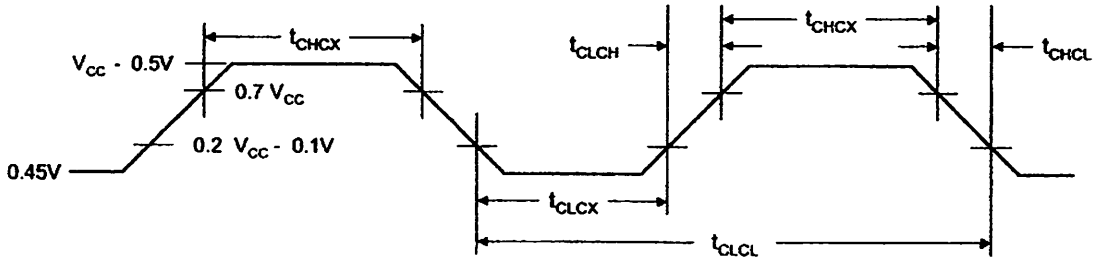
ternal Data Memory Read Cycle



ternal Data Memory Write Cycle



ternal Clock Drive Waveforms



ternal Clock Drive

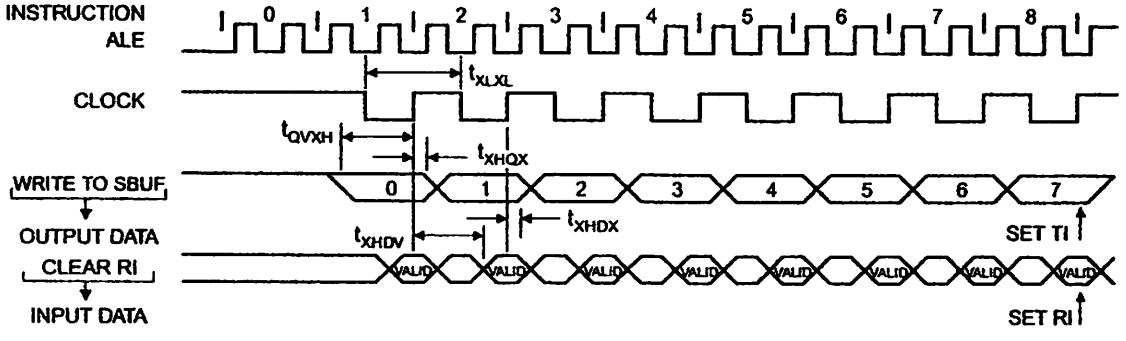
mbol	Parameter	Min	Max	Units
CLCL	Oscillator Frequency	0	33	MHz
CL	Clock Period	30		ns
ICX	High Time	12		ns
CX	Low Time	12		ns
CH	Rise Time		5	ns
ICL	Fall Time		5	ns

ɛrial Port Timing: Shift Register Mode Test Conditions

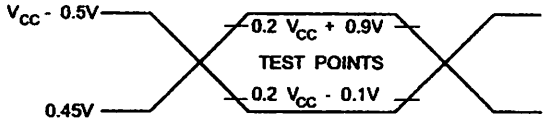
ɛ values in this table are valid for V_{CC} = 4.0V to 5.5V and Load Capacitance = 80 pF.

ymbol	Parameter	12 MHz Osc		Variable Oscillator		Units
		Min	Max	Min	Max	
LXL	Serial Port Clock Cycle Time	1.0		$12t_{CLCL}$		µs
VXH	Output Data Setup to Clock Rising Edge	700		$10t_{CLCL}$-133		ns
HQX	Output Data Hold After Clock Rising Edge	50		$2t_{CLCL}$-80		ns
HDX	Input Data Hold After Clock Rising Edge	0		0		ns
HDV	Clock Rising Edge to Input Data Valid		700		$10t_{CLCL}$-133	ns

ıift Register Mode Timing Waveforms

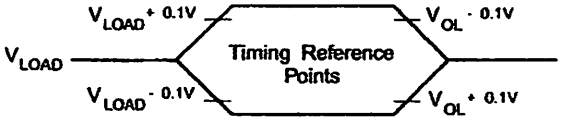


ɔ Testing Input/Output Waveforms[1]



e: 1. AC Inputs during testing are driven at V_{CC} - 0.5V for a logic 1 and 0.45V for a logic 0. Timing measurements are made at V_{IH} min. for a logic 1 and V_{IL} max. for a logic 0.

Float Waveforms[1]



Note: 1. For timing purposes, a port pin is no longer floating when a 100 mV change from load voltage occurs. A port pin begins to float when a 100 mV change from the loaded V_{OH}/V_{OL} level occurs.

dering Information

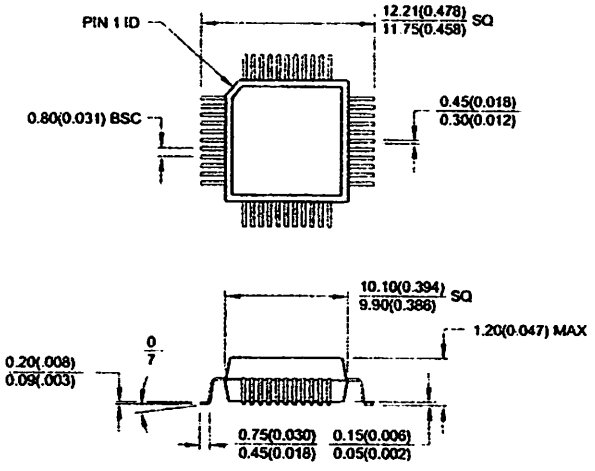
Speed (MHz)	Power Supply	Ordering Code	Package	Operation Range
24	4.0V to 5.5V	AT89S52-24AC	44A	Commercial (0°C to 70°C)
		AT89S52-24JC	44J	
		AT89S52-24PC	40P6	
		AT89S52-24AI	44A	Industrial (-40°C to 85°C)
		AT89S52-24JI	44J	
		AT89S52-24PI	40P6	
33	4.5V to 5.5V	AT89S52-33AC	44A	Commercial (0°C to 70°C)
		AT89S52-33JC	44J	
		AT89S52-33PC	40P6	

= Preliminary Availability

	Package Type
A	44-lead, Thin Plastic Gull Wing Quad Flatpack (TQFP)
J	44-lead, Plastic J-leaded Chip Carrier (PLCC)
P6	40-pin, 0.600" Wide, Plastic Dual Inline Package (PDIP)

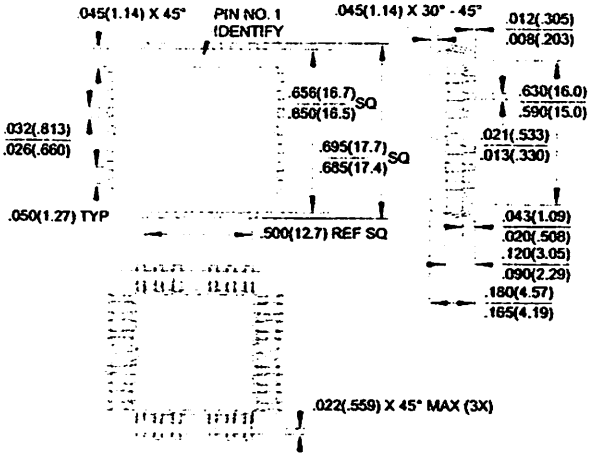
ackaging Information

44A, 44-lead, Thin (1.0 mm) Plastic Gull Wing Quad Flat Package (TQFP)
Dimensions in Millimeters and (Inches)*

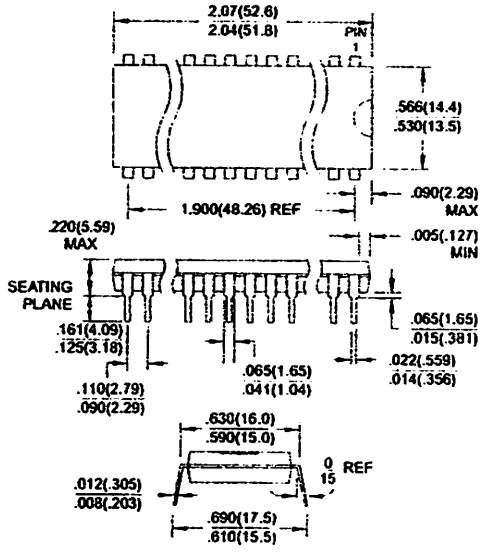


*Controlling dimension: millimeters

44J, 44-lead, Plastic J-leaded Chip Carrier (PLCC)
Dimensions in Inches and (Millimeters)



40P6, 40-pin, 0.600" Wide, Plastic Dual Inline Package (PDIP)
Dimensions in Inches and (Millimeters)
JEDEC STANDARD MS-011 AC



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Rev. 1919A-07/01/xM

DATA SHEET

ADC0803/0804
CMOS 8-bit A/D converters

roduct data
upersedes data of 2001 Aug 03

2002 Oct 17

ips
niconductors

PHILIPS

SCRIPTION

ADC0803 family is a series of three CMOS 8-bit successive roximation A/D converters using a resistive ladder and acitive array together with an auto-zero comparator. These verters are designed to operate with microprocessor-controlled es using a minimum of external circuitry. The 3-State output data s can be connected directly to the data bus.

differential analog voltage input allows for increased mon-mode rejection and provides a means to adjust the -scale offset. Additionally, the voltage reference input provides a ns of encoding small analog voltages to the full 8 bits of lution.

ATURES

mpatible with most microprocessors

fferential inputs

State outputs

gic levels TTL and MOS compatible

n be used with internal or external clock

alog input range 0 V to V_{CC}

ngle 5 V supply

aranteed specification with 1 MHz clock

PIN CONFIGURATION

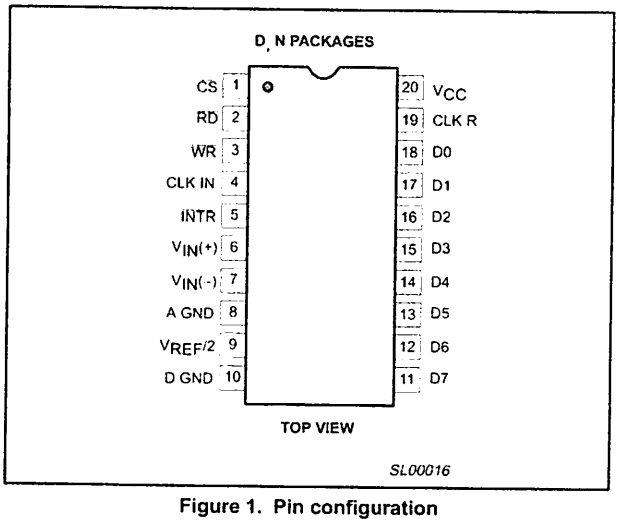


Figure 1. Pin configuration

APPLICATIONS

- Transducer-to-microprocessor interface
- Digital thermometer
- Digitally-controlled thermostat
- Microprocessor-based monitoring and control systems

DERING INFORMATION

DESCRIPTION	TEMPERATURE RANGE	ORDER CODE	TOPSIDE MARKING	DWG #
in plastic small outline (SO) package	0 to 70 °C	ADC0803CD, ADC0804CD	ADC0803-1CD, ADC0804-1CD	SOT163-1
in plastic small outline (SO) package	–40 to 85 °C	ADC0803LCD, ADC0804LCD	ADC0803-1LCD, ADC0804-1LCD	SOT163-1
in plastic dual in-line package (DIP)	0 to 70 °C	ADC0803CN, ADC0804CN	ADC0803-1CN, ADC0804-1CN	SOT146-1
in plastic dual in-line package (DIP)	–40 to +85 °C	ADC0803LCN, ADC0804LCN	ADC0803-1LCN, ADC0804-1LCN	SOT146-1

SOLUTE MAXIMUM RATINGS

MBOL	PARAMETER	CONDITIONS	RATING	UNIT
	Supply voltage		6.5	V
	Logic control input voltages		–0.3 to +16	V
	All other input voltages		–0.3 to (V_{CC} +0.3)	V
	Operating temperature range			
	ADC0803LCD/ADC0804LCD		–40 to +85	°C
	ADC0803LCN/ADC0804LCN		–40 to +85	°C
	ADC0803CD/ADC0804CD		0 to +70	°C
	ADC0803CN/ADC0804CN		0 to +70	°C
	Storage temperature		–65 to +150	°C
	Lead soldering temperature (10 seconds)		230	°C
	Maximum power dissipation[1]	T_{amb} = 25 °C (still air)		
	N package		1690	mW
	D package		1390	mW

E:

erate above 25 °C, at the following rates: N package at 13.5 mW/°C; D package at 11.1 mW/°C.

OCK DIAGRAM

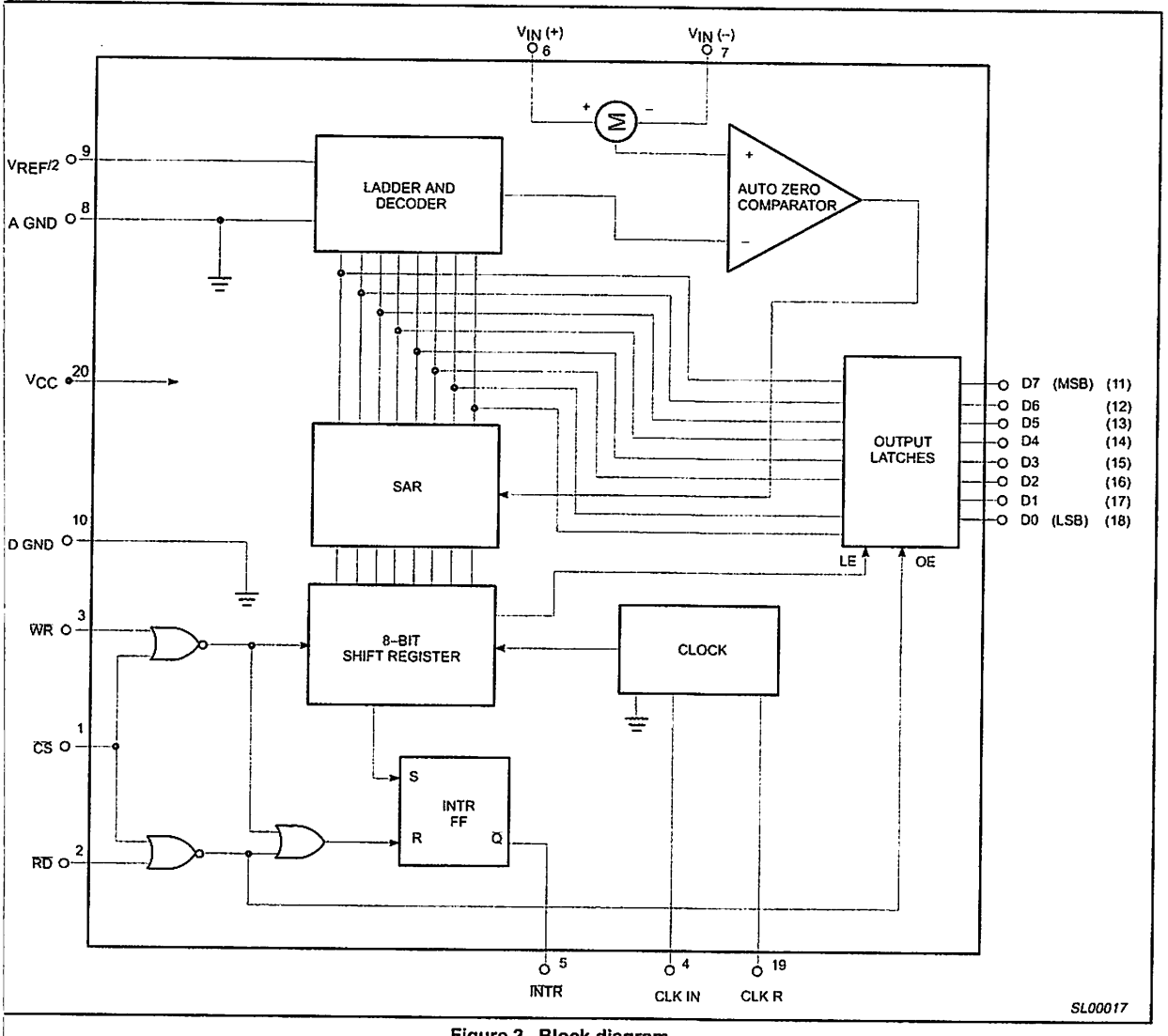


Figure 2. Block diagram

ELECTRICAL CHARACTERISTICS

= 5.0 V, f_{CLK} = 1 MHz, $T_{min} \leq T_{amb} \leq T_{max}$, unless otherwise specified.

MBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNIT
			Min	Typ	Max	
	ADC0803 relative accuracy error (adjusted)	Full-Scale adjusted			0.50	LSB
	ADC0804 relative accuracy error (unadjusted)	$V_{REF}/2$ = 2.500 V_{DC}			1	LSB
	$V_{REF}/2$ input resistance[3]	V_{CC} = 0 V[2]	400	680		Ω
	Analog input voltage range[3]		−0.05		V_{CC}+0.05	V
	DC common-mode error	Over analog input voltage range		1/16	1/8	LSB
	Power supply sensitivity	V_{CC} = 5V ±10%[1]		1/16		LSB
ntrol inputs						
	Logical "1" input voltage	V_{CC} = 5.25 V_{DC}	2.0		15	V_{DC}
	Logical "0" input voltage	V_{CC} = 4.75 V_{DC}			0.8	V_{DC}
	Logical "1" input current	V_{IN} = 5 V_{DC}		0.005	1	μA_{DC}
	Logical "0" input current	V_{IN} = 0 V_{DC}	−1	−0.005		μA_{DC}
ck in and clock R						
	Clock in positive-going threshold voltage		2.7	3.1	3.5	V_{DC}
	Clock in negative-going threshold voltage		1.5	1.8	2.1	V_{DC}
	Clock in hysteresis $(V_T+)-(V_T-)$		0.6	1.3	2.0	V_{DC}
	Logical "0" clock R output voltage	I_{OL} = 360 µA, V_{CC} = 4.75 V_{DC}			0.4	V_{DC}
	Logical "1" clock R output voltage	I_{OH} = −360 µA, V_{CC} = 4.75 V_{DC}	2.4			V_{DC}
a output and INTR						
	Logical "0" output voltage					
	Data outputs	I_{OL} = 1.6 mA, V_{CC} = 4.75 V_{DC}			0.4	V_{DC}
	$\overline{INTR}$ outputs	I_{OL} = 1.0 mA, V_{CC} = 4.75 V_{DC}			0.4	V_{DC}
	Logical "1" output voltage	I_{OH} = −360 µA, V_{CC} = 4.75 V_{DC}	2.4			V_{DC}
		I_{OH} = −10 µA, V_{CC} = 4.75 V_{DC}	4.5			
	3-State output leakage	V_{OUT} = 0 V_{DC}, $\overline{CS}$ = logical "1"	−3			μA_{DC}
	3-State output leakage	V_{OUT} = 5 V_{DC}, $\overline{CS}$ = logical "1"			3	μA_{DC}
	+Output short-circuit current	V_{OUT} = 0 V, T_{amb} = 25 °C	4.5	12		mA_{DC}
	−Output short-circuit current	V_{OUT} = V_{CC}, T_{amb} = 25 °C	9.0	30		mA_{DC}
	Power supply current	f_{CLK} = 1 MHz, $V_{REF}/2$ = OPEN, $\overline{CS}$ = Logical "1", T_{amb} = 25 °C		3.0	3.5	mA

ES:

nalog inputs must remain within the range: $-0.05 \leq V_{IN} \leq V_{CC} + 0.05$ V.

ee typical performance characteristics for input resistance at V_{CC} = 5 V.

REF/2 and V_{IN} must be applied after the V_{CC} has been turned on to prevent the possibility of latching.

ELECTRICAL CHARACTERISTICS

YMBOL	PARAMETER	TO	FROM	TEST CONDITIONS	LIMITS			UNIT
					Min	Typ	Max	
	Conversion time			f_{CLK} = 1 MHz[1]	66		73	µs
K	Clock frequency[1]				0.1	1.0	3.0	MHz
	Clock duty cycle[1]				40		60	%
	Free-running conversion rate			$\overline{CS}$ = 0, f_{CLK} = 1 MHz $\overline{INTR}$ tied to $\overline{WR}$			13690	conv/s
WR)L	Start pulse width			$\overline{CS}$ = 0	30			ns
C	Access time	Output	$\overline{RD}$	$\overline{CS}$ = 0, C_L = 100 pF		75	100	ns
, t_{0H}	3-State control	Output	$\overline{RD}$	C_L = 10 pF, R_L = 10 kΩ See 3-State test circuit		70	100	ns
, t_{R1}	$\overline{INTR}$ delay	$\overline{INTR}$	$\overline{WD}$ or $\overline{RD}$			100	150	ns
	Logic input=capacitance					5	7.5	pF
UT	3-State output capacitance					5	7.5	pF

E:

ccuracy is guaranteed at f_{CLK} = 1 MHz. Accuracy may degrade at higher clock frequencies.

NCTIONAL DESCRIPTION

e devices operate on the Successive Approximation principle. pg switches are closed sequentially by successive pximation logic until the input to the auto-zero comparator (+)–V_{IN}(–)] matches the voltage from the decoder. After all bits sted and determined, the 8-bit binary code corresponding to put voltage is transferred to an output latch. Conversion begins he arrival of a pulse at the $\overline{WR}$ input if the CS input is low. On ligh-to-Low transition of the signal at the WR or the CS input, AR is initialized, the shift register is reset, and the $\overline{INTR}$ output high. The A/D will remain in the reset state as long as the $\overline{CS}$ $\overline{WR}$ inputs remain low. Conversion will start from one to eight periods after one or both of these inputs makes a Low-to-High tion. After the conversion is complete, the $\overline{INTR}$ pin will make a to-Low transition. This can be used to interrupt a processor, or wise signal the availability of a new conversion result. A read operation (with $\overline{CS}$ low) will clear the $\overline{INTR}$ line and enable the t latches. The device may be run in the free-running mode as ibed later. A conversion in progress can be interrupted by g another start command.

tal Control Inputs

igital control inputs (CS, WR, $\overline{RD}$) are compatible with ard TTL logic voltage levels. The required signals at these s correspond to Chip Select, START Conversion, and Output e control signals, respectively. They are active-Low for easy ace to microprocessor and microcontroller control buses. For cations not using microprocessors, the $\overline{CS}$ input (Pin 1) can be ded and the A/D START function is achieved by a ive-going pulse to the $\overline{WR}$ input (Pin 3). The Output Enable on is achieved by a logic low signal at the $\overline{RD}$ input (Pin 2), may be grounded to constantly have the latest conversion nt at the output.

ANALOG OPERATION

Analog Input Current

The analog comparisons are performed by a capacitive charge summing circuit. The input capacitor is switched between $V_{IN(+)}$4 and $V_{IN(-)}$, while reference capacitors are switched between taps on the reference voltage divider string. The net charge corresponds to the weighted difference between the input and the most recent total value set by the successive approximation register.

The internal switching action causes displacement currents to flow at the analog inputs. The voltage on the on-chip capacitance is switched through the analog differential input voltage, resulting in proportional currents entering the $V_{IN(+)}$ input and leaving the $V_{IN(-)}$ input. These transient currents occur at the leading edge of the internal clock pulses. They decay rapidly so do not inherently cause errors as the on-chip comparator is strobed at the end of the clock period.

Input Bypass Capacitors and Source Resistance

Bypass capacitors at the input will average the charges mentioned above, causing a DC and an AC current to flow through the output resistance of the analog signal sources. This charge pumping action is worse for continuous conversions with the $V_{IN(+)}$ input at full scale. This current can be a few microamps, so bypass capacitors should NOT be used at the analog inputs of the $V_{REF}/2$ input for high resistance sources (> 1 kΩ). If input bypass capacitors are desired for noise filtering and a high source resistance is desired to minimize capacitor size, detrimental effects of the voltage drop across the input resistance can be eliminated by adjusting the full scale with both the input resistance and the input bypass capacitor in place. This is possible because the magnitude of the input current is a precise linear function of the differential voltage.

ge values of source resistance where an input bypass capacitor ot used will not cause errors as the input currents settle out prior ie comparison time. If a low pass filter is required in the system, a low valued series resistor (< 1 kΩ) for a passive RC section or an op amp active filter (low pass). For applications with source stances at or below 1 kΩ, a 0.1 µF bypass capacitor at the inputs prevent pickup due to series lead inductance or a long wire. A Ω series resistor can be used to isolate this capacitor (both the stor and capacitor should be placed out of the feedback loop) the output of the op amp, if used.

alog Differential Voltage Inputs and mmon-Mode Rejection

se A/D converters have additional flexibility due to the analog rential voltage input. The $V_{IN(-)}$ input (Pin 7) can be used to ract a fixed voltage from the input reading (tare correction). This so useful in a 4/20 mA current loop conversion. Common-mode e can also be reduced by the use of the differential input.

time interval between sampling $V_{IN(+)}$ and $V_{IN(-)}$ is 4.5 clock ds. The maximum error due to this time difference is given by:

max) = (V_P) $(2f_{CM})$ $(4.5/f_{CLK})$.

e:

= error voltage due to sampling delay

= peak value of common-mode voltage

M = common mode frequency

xample, with a 60 Hz common-mode frequency, f_{cm}, and a lz A/D clock, f_{CLK}, keeping this error to 1/4 LSB (about 5 mV) allow a common-mode voltage, V_P, which is given by:

$$= \frac{[V(max)\ (f_{CLK})}{(2f_{CM})(4.5)}$$

$$= \frac{(5 \times 10^{-3})\ (10^4)}{(6.28)\ (60)\ (4.5)} = 2.95V$$

llowed range of analog input voltages usually places more e restrictions on input common-mode voltage levels than this, ver.

nalog input span less than the full 5 V capability of the device, her with a relatively large zero offset, can be easily handled by f the differential input. (See Reference Voltage Span Adjust).

se and Stray Pickup

eads of the analog inputs (Pins 6 and 7) should be kept as as possible to minimize input noise coupling and stray signal up. Both EMI and undesired digital signal coupling to these s can cause system errors. The source resistance for these s should generally be below 5 kΩ to help avoid undesired noise p. Input bypass capacitors at the analog inputs can create s as described previously. Full scale adjustment with any input ss capacitors in place will eliminate these errors.

erence Voltage

pplication flexibility, these A/D converters have been designed commodate fixed reference voltages of 5V to Pin 20 or 2.5 V to or an adjusted reference voltage at Pin 9. The reference can t by forcing it at $V_{REF}/2$ input, or can be determined by the y voltage (Pin 20). Figure 6 indicates how this is accomplished.

Reference Voltage Span Adjust

Note that the Pin 9 ($V_{REF}/2$) voltage is either 1/2 the voltage applied to the V_{CC} supply pin, or is equal to the voltage which is externally forced at the $V_{REF}/2$ pin. In addition to allowing for flexible references and full span voltages, this also allows for a ratiometric voltage reference. The internal gain of the $V_{REF}/2$ input is 2, making the full-scale differential input voltage twice the voltage at Pin 9.

For example, a dynamic voltage range of the analog input voltage that extends from 0 to 4 V gives a span of 4 V (4–0), so the $V_{REF}/2$ voltage can be made equal to 2 V (half of the 4 V span) and full scale output would correspond to 4 V at the input.

On the other hand, if the dynamic input voltage had a range of 0.5 to 3.5 V, the span or dynamic input range is 3 V (3.5–0.5). To encode this 3 V span with 0.5 V yielding a code of zero, the minimum expected input (0.5 V, in this case) is applied to the $V_{IN}(-)$ pin to account for the offset, and the $V_{REF}/2$ pin is set to 1/2 the 3 V span, or 1.5 V. The A/D converter will now encode the $V_{IN}(+)$ signal between 0.5 and 3.5 V with 0.5 V at the input corresponding to a code of zero and 3.5 V at the input producing a full scale output code. The full 8 bits of resolution are thus applied over this reduced input voltage range. The required connections are shown in Figure 7.

Operating Mode

These converters can be operated in two modes:

1) absolute mode
2) ratiometric mode

In absolute mode applications, both the initial accuracy and the temperature stability of the reference voltage are important factors in the accuracy of the conversion. For $V_{REF}/2$ voltages of 2.5 V, initial errors of ±10 mV will cause conversion errors of ±1 LSB due to the gain of 2 at the $V_{REF}/2$ input. In reduced span applications, the initial value and stability of the $V_{REF}/2$ input voltage become even more important as the same error is a larger percentage of the $V_{REF}/2$ nominal value. See Figure 8.

In ratiometric converter applications, the magnitude of the reference voltage is a factor in both the output of the source transducer and the output of the A/D converter, and, therefore, cancels out in the final digital code. See Figure 9.

Generally, the reference voltage will require an initial adjustment. Errors due to an improper reference voltage value appear as full-scale errors in the A/D transfer function.

ERRORS AND INPUT SPAN ADJUSTMENTS

There are many sources of error in any data converter, some of which can be adjusted out. Inherent errors, such as relative accuracy, cannot be eliminated, but such errors as full-scale and zero scale offset errors can be eliminated quite easily. See Figure 7.

Zero Scale Error

Zero scale error of an A/D is the difference of potential between the ideal 1/2 LSB value (9.8 mV for $V_{REF}/2$=2.500 V) and that input voltage which just causes an output transition from code 0000 0000 to a code of 0000 0001.

If the minimum input value is not ground potential, a zero offset can be made. The converter can be made to output a digital code of 0000 0000 for the minimum expected input voltage by biasing the $V_{IN}(-)$ input to that minimum value expected at the $V_{IN}(-)$ input to that minimum value expected at the $V_{IN}(+)$ input. This uses the differential mode of the converter. Any offset adjustment should be done prior to full scale adjustment.

l Scale Adjustment

scale gain is adjusted by applying any desired offset voltage to –), then applying the $V_{IN}(+)$ a voltage that is 1-$^1/_2$ LSB less than desired analog full-scale voltage range and then adjusting the nitude of $V_{REF}/2$ input voltage (or the V_{CC} supply if there is no F/2 input connection) for a digital output code which just ges from 1111 1110 to 1111 1111. The ideal $V_{IN}(+)$ voltage for full-scale adjustment is given by:

$$_N(+) = V_{IN}(-) - 1.5 \times \frac{V_{MAX} - V_{MIN}}{255}$$

re:

$_{MAX}$ = high end of analog input range (ground referenced)

$_{MIN}$ = low end (zero offset) of analog input (ground referenced)

OCKING OPTION

clock signal for these A/Ds can be derived from external ces, such as a system clock, or self-clocking can be mplished by adding an external resistor and capacitor, as n in Figure 11.

y capacitive or DC loading of the CLK R pin should be avoided is will disturb normal converter operation. Loads less than 50pF llowed. This permits driving up to seven A/D converter CLK IN of this family from a single CLK R pin of one converter. For r loading of the clock line, a CMOS or low power TTL buffer or input logic should be used to minimize the loading on the CLK .

tart During a Conversion

nversion in process can be halted and a new conversion began inging the $\overline{CS}$ and $\overline{WR}$ inputs low and allowing at least one of to go high again. The output data latch is not updated if the ersion in progress is not completed; the data from the ously completed conversion will remain in the output data es until a subsequent conversion is completed.

tinuous Conversion

ovide continuous conversion of input data, the $\overline{CS}$ and $\overline{RD}$ s are grounded and $\overline{INTR}$ output is tied to the $\overline{WR}$ input. This /$\overline{WR}$ connection should be momentarily forced to a logic low power-up to insure circuit operation. See Figure 10 for one o accomplish this.

DRIVING THE DATA BUS

This CMOS A/D converter, like MOS microprocessors and memories, will require a bus driver when the total capacitance of the data bus gets large. Other circuitry tied to the data bus will add to the total capacitive loading, even in the high impedance mode.

There are alternatives in handling this problem. The capacitive loading of the data bus slows down the response time, although DC specifications are still met. For systems with a relatively low CPU clock frequency, more time is available in which to establish proper logic levels on the bus, allowing higher capacitive loads to be driven (see Typical Performance Characteristics).

At higher CPU clock frequencies, time can be extended for I/O reads (and/or writes) by inserting wait states (8880) or using clock-extending circuits (6800, 8035).

Finally, if time is critical and capacitive loading is high, external bus drivers must be used. These can be 3-State buffers (low power Schottky is recommended, such as the N74LS240 series) or special higher current drive products designed as bus drivers. High current bipolar bus drivers with PNP inputs are recommended as the PNP input offers low loading of the A/D output, allowing better response time.

POWER SUPPLIES

Noise spikes on the V_{CC} line can cause conversion errors as the internal comparator will respond to them. A low inductance filter capacitor should be used close to the converter V_{CC} pin and values of 1 µF or greater are recommended. A separate 5 V regulator for the converter (and other 5 V linear circuitry) will greatly reduce digital noise on the V_{CC} supply and the attendant problems.

WIRING AND LAYOUT PRECAUTIONS

Digital wire-wrap sockets and connections are not satisfactory for breadboarding this (or any) A/D converter. Sockets on PC boards can be used. All logic signal wires and leads should be grouped or kept as far as possible from the analog signal leads. Single wire analog input leads may pick up undesired hum and noise, requiring the use of shielded leads to the analog inputs in many applications.

A single-point analog ground separate from the logic or digital ground points should be used. The power supply bypass capacitor and the self-clocking capacitor, if used, should be returned to digital ground. Any $V_{REF}/2$ bypass capacitor, analog input filter capacitors, and any input shielding should be returned to the analog ground point. Proper grounding will minimize zero-scale errors which are present in every code. Zero-scale errors can usually be traced to improper board layout and wiring.

ʾLICATIONS

roprocessor Interfacing

family of A/D converters was designed for easy microprocessor acing. These converters can be memory mapped with ɔpriate memory address decoding for $\overline{CS}$ (read) input. The ɘ-Low write pulse from the processor is then connected to the nput of the A/D converter, while the processor active-Low read : is fed to the converter $\overline{RD}$ input to read the converted data. If lock signal is derived from the microprocessor system clock, esigner/programmer should be sure that there is no attempt to the converter until 74 converter clock pulses after the start : goes high. Alternatively, the $\overline{INTR}$ pin may be used to interrupt rocessor to cause reading of the converted data. Of course, the ɘrter can be connected and addressed as a peripheral (in I/O ɘ), as shown in Figure 12. A bus driver should be used as a r to the A/D output in large microprocessor systems where the leaves the PC board and/or must drive capacitive loads in ;s of 100 pF. See Figure 14.

acing the SCN8048 microcomputer family is pretty simple, as n in Figure 13. Since the SCN8048 family has 24 I/O lines, one ɨse (shown here as bit 0 or port 1) can be used as the chip t signal to the converter, eliminating the need for an address ɨer. The $\overline{RD}$ and $\overline{WR}$ signals are generated by reading from /riting to a dummy address.

tizing a Transducer Interface Output

ɨit Description

ɘ 15 shows an example of digitizing transducer interface output ɟe. In this case, the transducer interface is the NE5521, an (Linear Variable Differential Transformer) Signal Conditioner. iode at the A/D input is used to insure that the input to the A/D not go excessively beyond the supply voltage of the A/D. See the NE5521 data sheet for a complete description of the operation of that part.

Circuit Adjustment

To adjust the full scale and zero scale of the A/D, determine the range of voltages that the transducer interface output will take on. Set the LVDT core for null and set the Zero Scale Scale Adjust Potentiometer for a digital output from the A/D of 1000 000. Set the LVDT core for maximum voltage from the interface and set the Full Scale Adjust potentiometer so the A/D output is just barely 1111 1111.

A Digital Thermostat

Circuit Description

The schematic of a Digital Thermostat is shown in Figure 16. The A/D digitizes the output of the LM35, a temperature transducer IC with an output of 10 mV per °C. With $V_{REF}/2$ set for 2.56 V, this 10 mV corresponds to 1/2 LSB and the circuit resolution is 2 °C. Reducing $V_{REF}/2$ to 1.28 yields a resolution of 1 °C. Of course, the lower $V_{REF}/2$ is, the more sensitive the A/D will be to noise.

The desired temperature is set by holding either of the set buttons closed. The SCC80C451 programming could cause the desired (set) temperature to be displayed while either button is depressed and for a short time after it is released. At other times the ambient temperature could be displayed.

The set temperature is stored in an SCN8051 internal register. The A/D conversion is started by writing anything at all to the A/D with port pin P10 set high. The desired temperature is compared with the digitized actual temperature, and the heater is turned on or off by clearing setting port pin P12. If desired, another port pin could be used to turn on or off an air conditioner.

The display drivers are NE587s if common anode LED displays are used. Of course, it is possible to interface to LCD displays as well.

ʼICAL PERFORMANCE CHARACTERISTICS

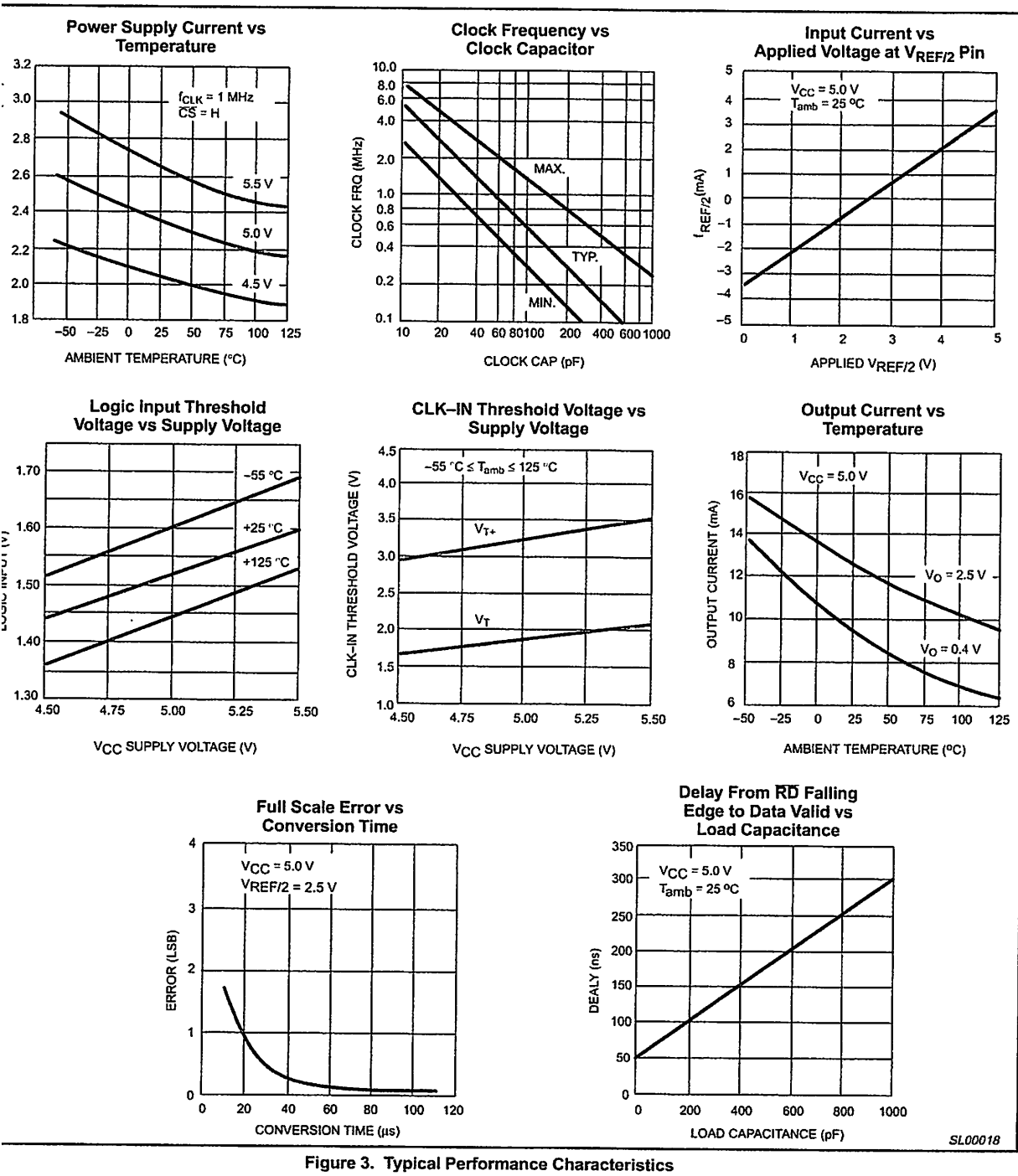


Figure 3. Typical Performance Characteristics

ſATE TEST CIRCUITS AND WAVEFORMS (ADC0801-1)

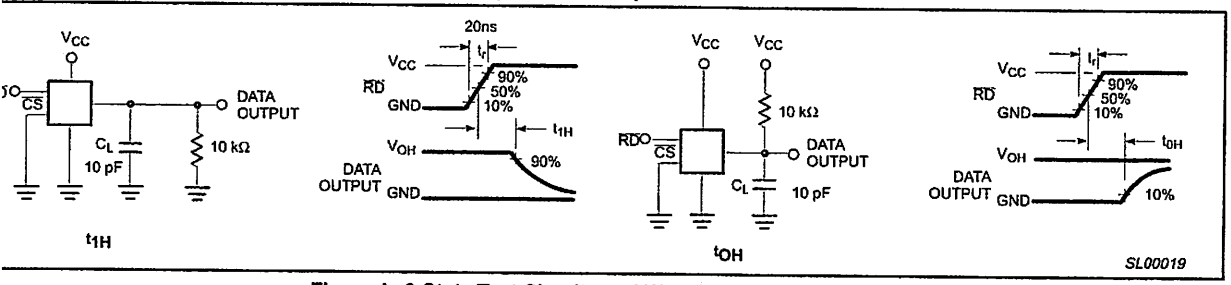
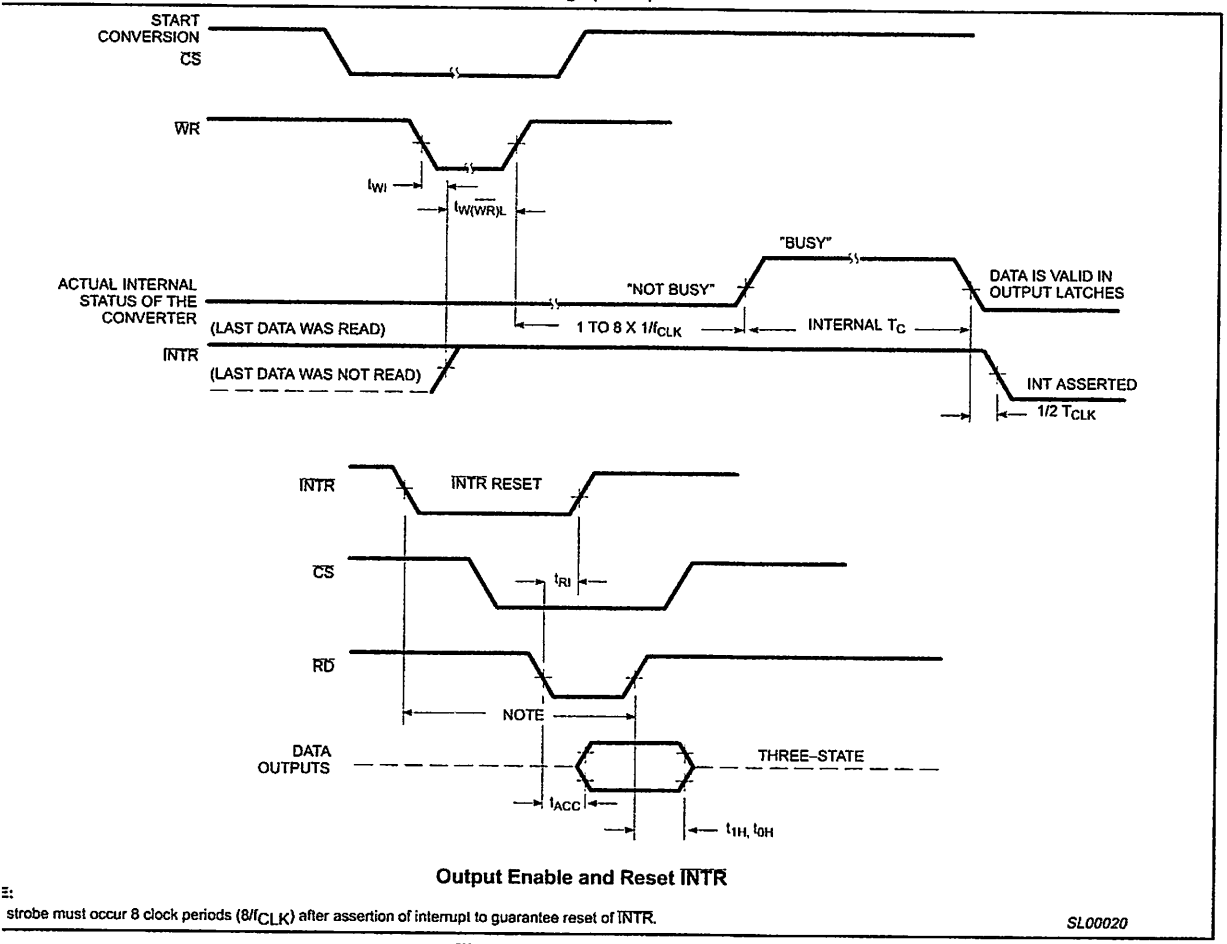


Figure 4. 3-State Test Circuits and Waveforms (ADC0801-1)

NG DIAGRAMS (All timing is measured from the 50% voltage points)



Output Enable and Reset INTR

E:
strobe must occur 8 clock periods ($8/f_{CLK}$) after assertion of interrupt to guarantee reset of INTR.

Figure 5. Timing Diagrams

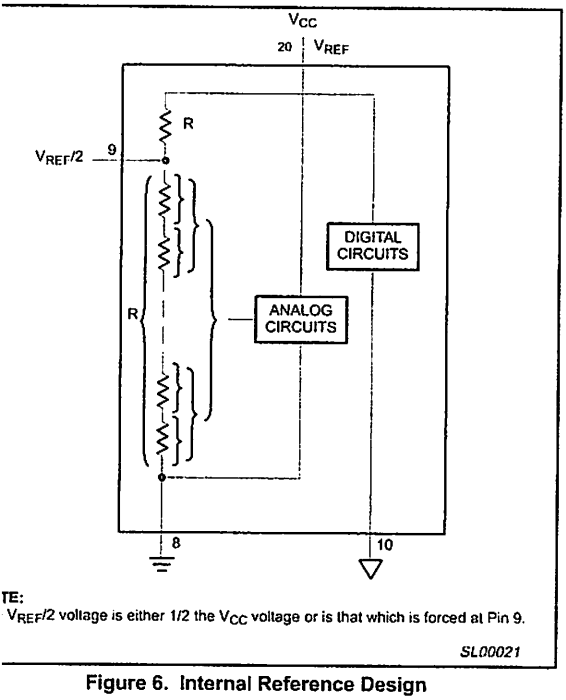


Figure 6. Internal Reference Design

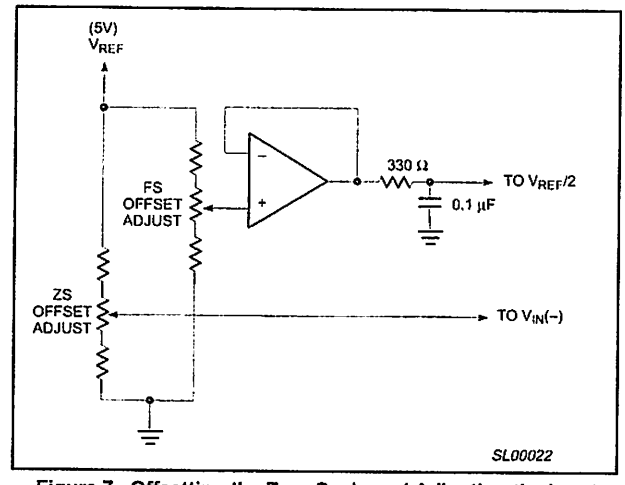


Figure 7. Offsetting the Zero Scale and Adjusting the Input Range (Span)

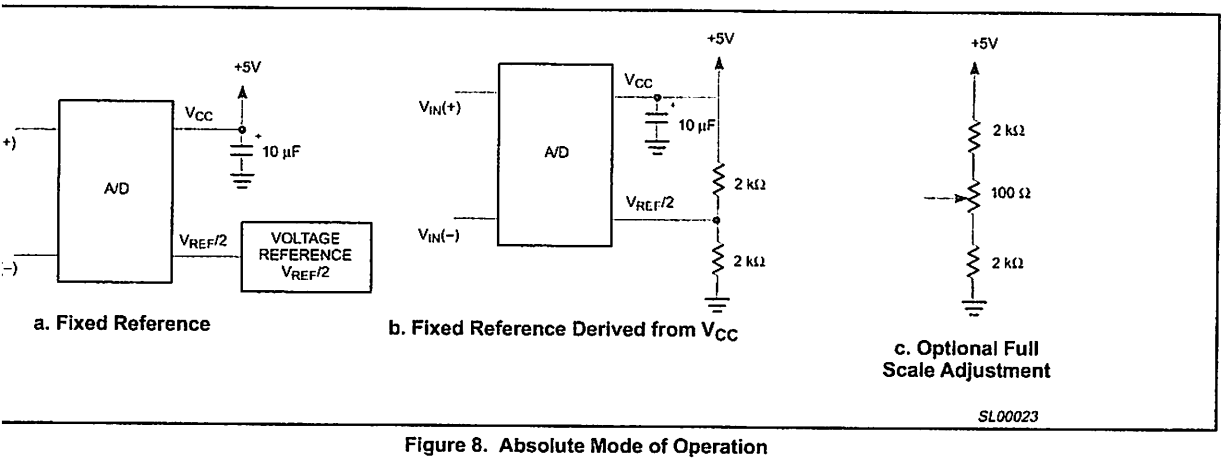
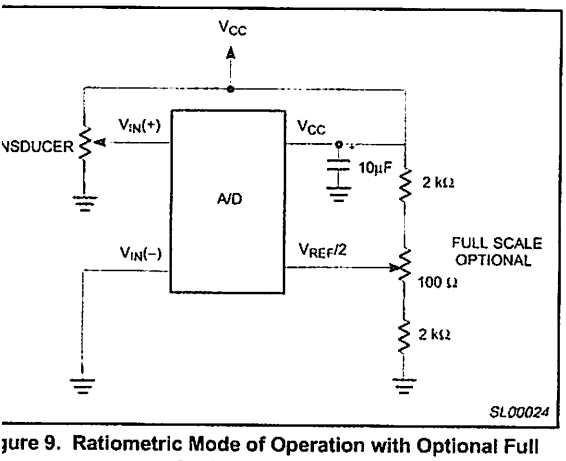


Figure 8. Absolute Mode of Operation



ɟure 9. Ratiometric Mode of Operation with Optional Full Scale Adjustment

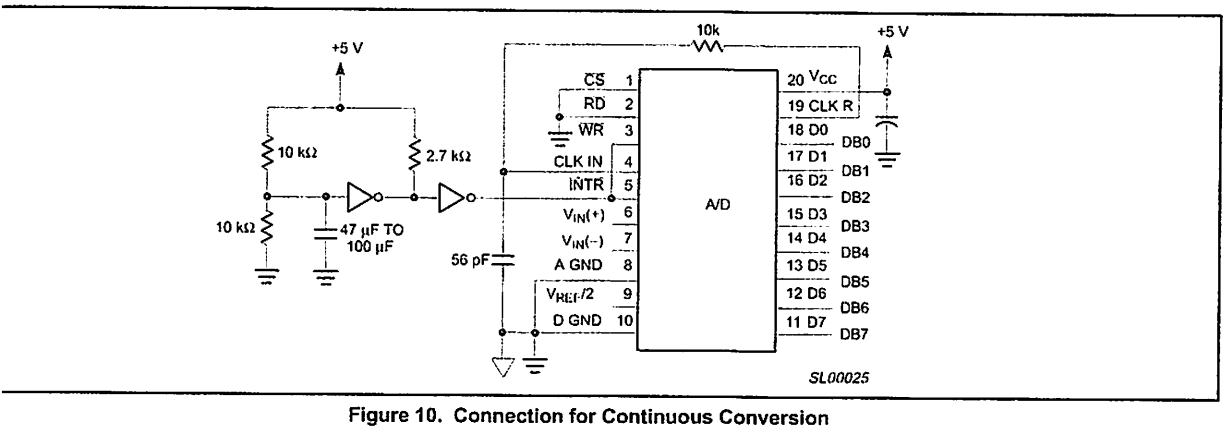


Figure 10. Connection for Continuous Conversion

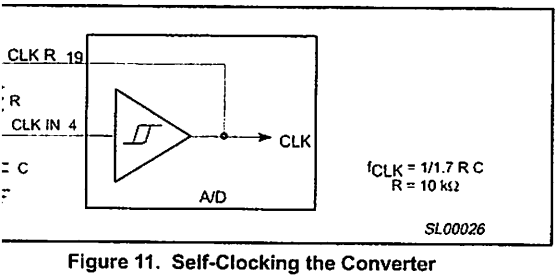


Figure 11. Self-Clocking the Converter

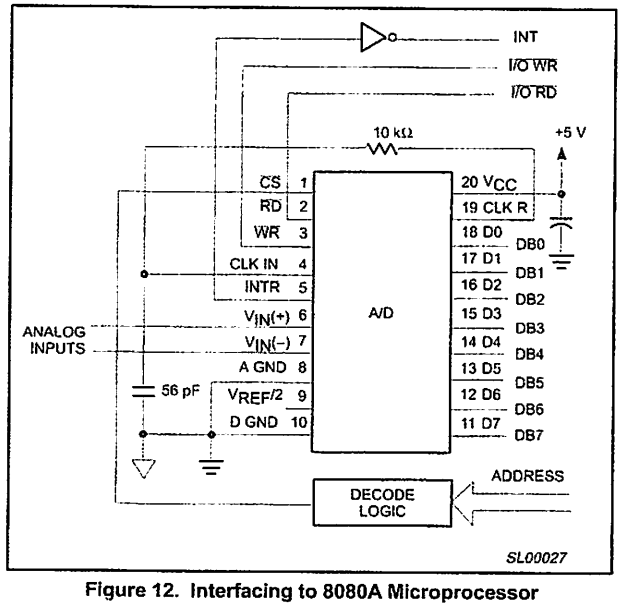


Figure 12. Interfacing to 8080A Microprocessor

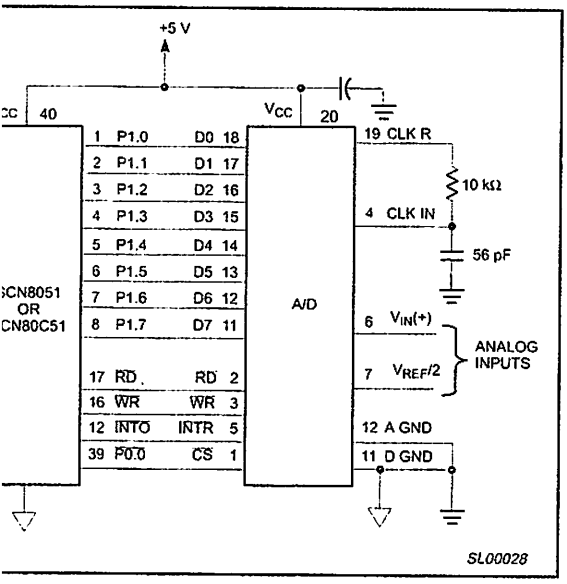


Figure 13. SCN8051 Interfacing

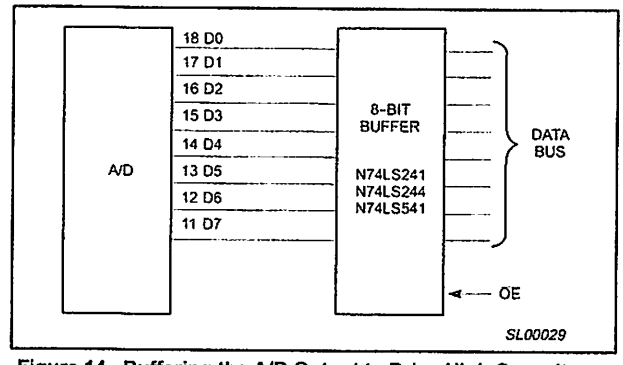


Figure 14. Buffering the A/D Output to Drive High Capacitance Loads and for Driving Off-Board Loads

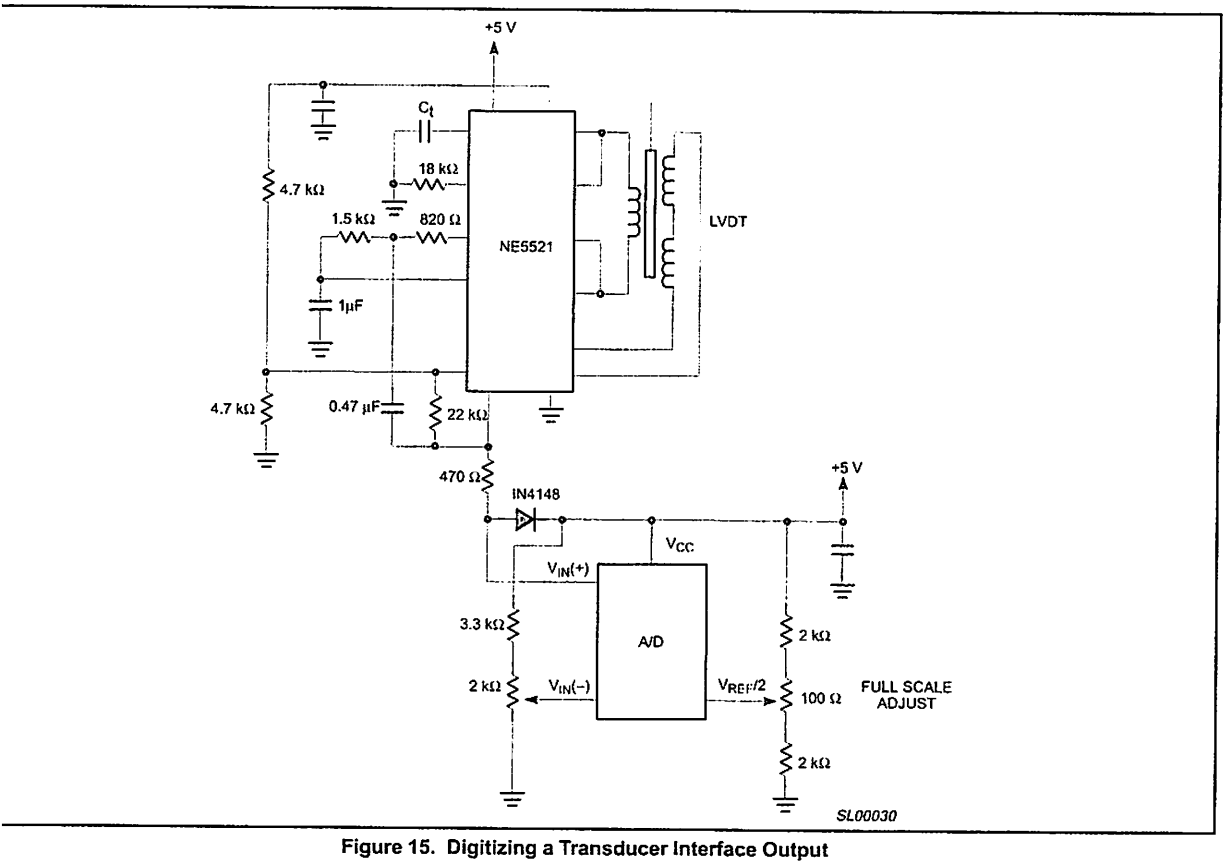


Figure 15. Digitizing a Transducer Interface Output

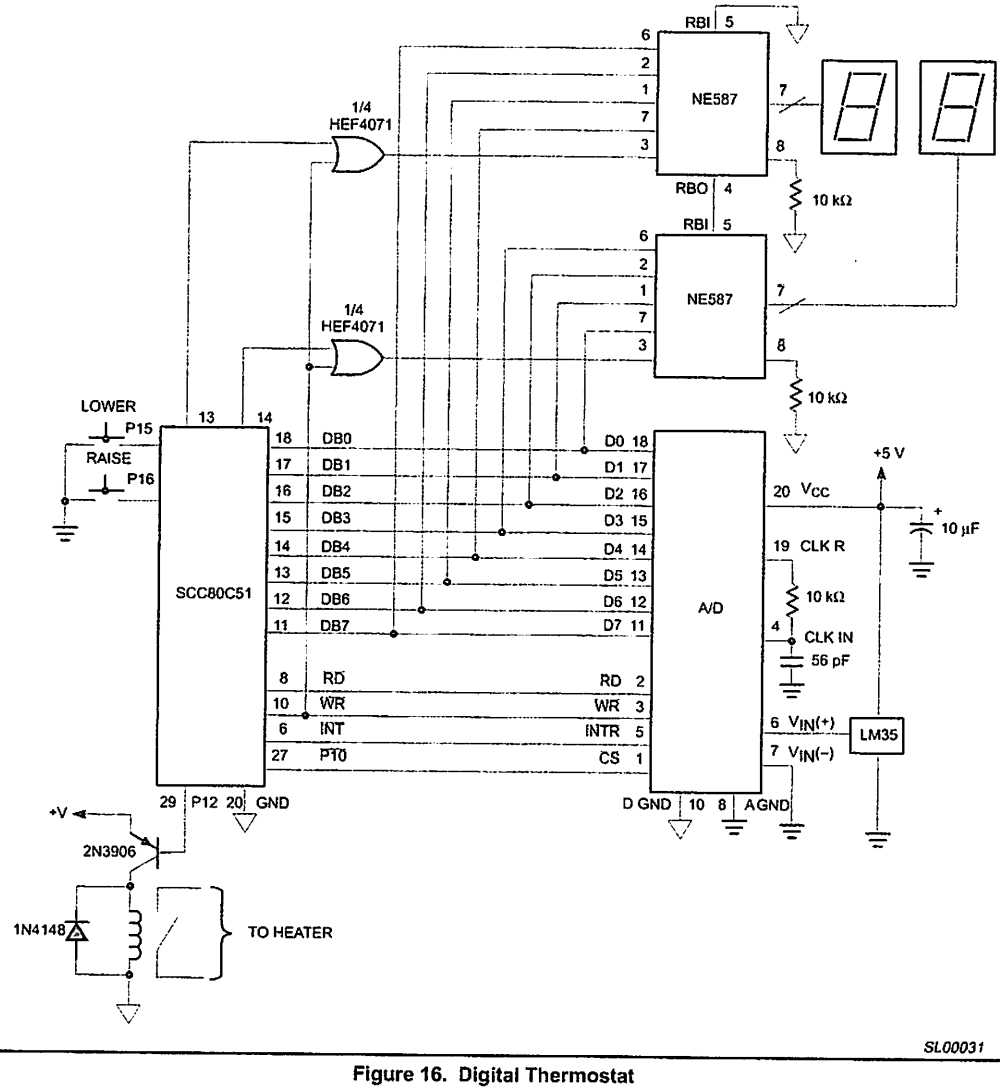
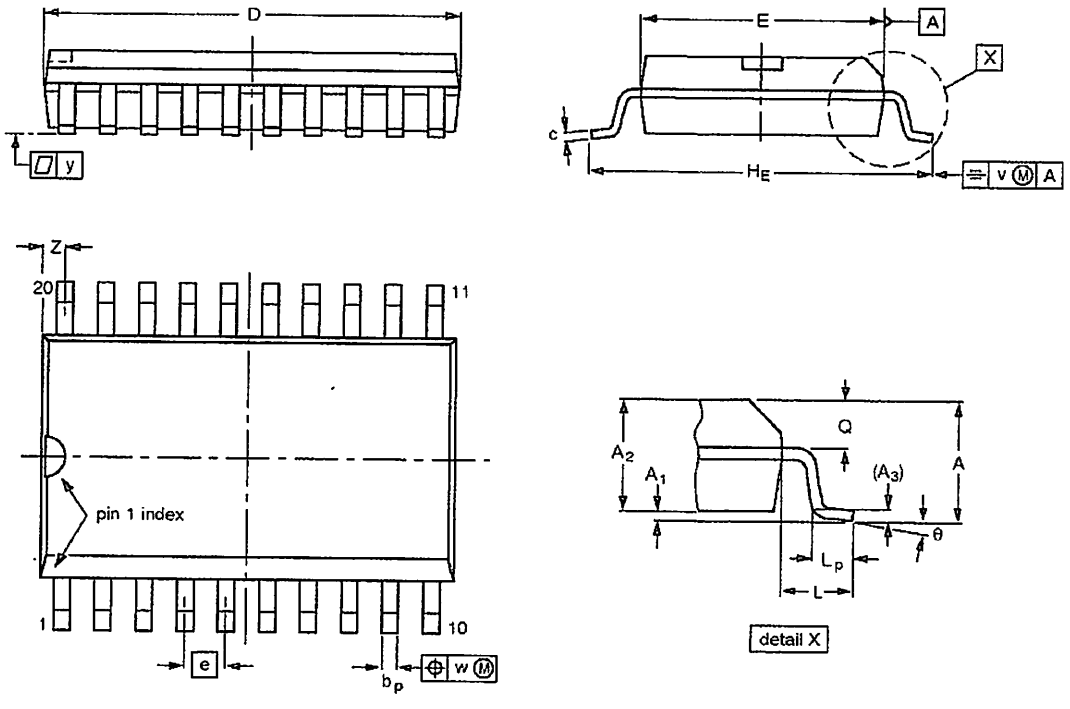
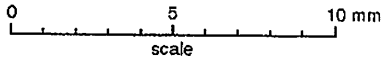


Figure 16. Digital Thermostat

020: plastic small outline package; 20 leads; body width 7.5 mm

SOT163-1





MENSIONS (inch dimensions are derived from the original mm dimensions)

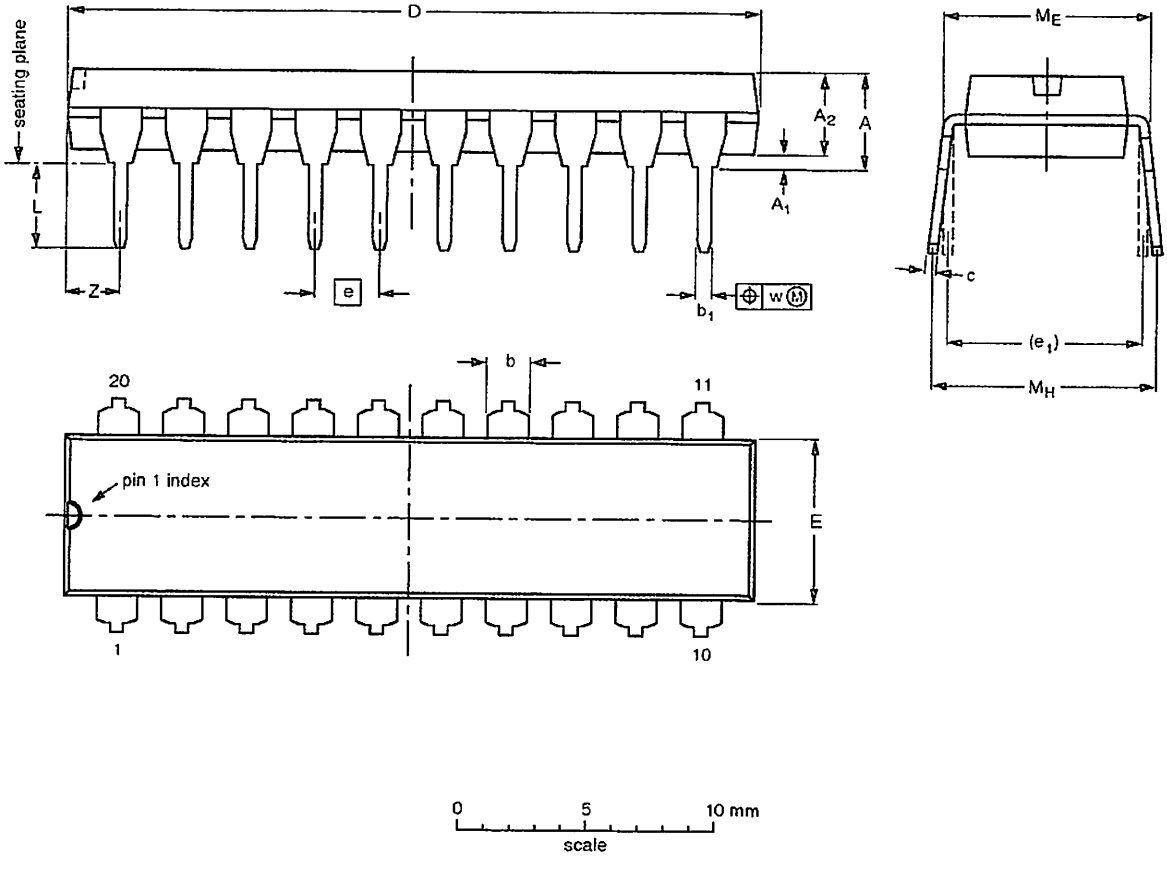
UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(1)}$	e	H_E	L	L_p	Q	v	w	y	$Z^{(1)}$	θ
mm	2.65	0.30 0.10	2.45 2.25	0.25	0.49 0.36	0.32 0.23	13.0 12.6	7.6 7.4	1.27	10.65 10.00	1.4	1.1 0.4	1.1 1.0	0.25	0.25	0.1	0.9 0.4	8° 0°
ches	0.10	0.012 0.004	0.096 0.089	0.01	0.019 0.014	0.013 0.009	0.51 0.49	0.30 0.29	0.050	0.419 0.394	0.055	0.043 0.016	0.043 0.039	0.01	0.01	0.004	0.035 0.016	

te

Plastic or metal protrusions of 0.15 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT163-1	075E04	MS-013				~~97-05-22~~ 99-12-27

P20: plastic dual in-line package; 20 leads (300 mil) **SOT146-1**



MENSIONS (inch dimensions are derived from the original mm dimensions)

UNIT	A max.	A_1 min.	A_2 max.	b	b_1	c	$D^{(1)}$	$E^{(1)}$	e	e_1	L	M_E	M_H	w	$Z^{(1)}$ max.
mm	4.2	0.51	3.2	1.73 1.30	0.53 0.38	0.36 0.23	26.92 26.54	6.40 6.22	2.54	7.62	3.60 3.05	8.25 7.80	10.0 8.3	0.254	2.0
nches	0.17	0.020	0.13	0.068 0.051	0.021 0.015	0.014 0.009	1.060 1.045	0.25 0.24	0.10	0.30	0.14 0.12	0.32 0.31	0.39 0.33	0.01	0.078

te

Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT146-1		MS-001	SC-603			~~95-05-24~~ 99-12-27

VISION HISTORY

	Date	Description
	20021017	**Product data; third version; supersedes data of 2001 Aug 03.** Engineering Change Notice 853–0034 28949 (date: 20020916). **Modifications:** • Add "Topside Marking" column to Ordering Information table.
	20010803	**Product data; second version (9397 750 08926).** Engineering Change Notice 853–0034 26832 (date: 20010803).
	19940831	**Product data; initial version.** Engineering Change Notice 853–0034 13721 (date: 19940831).

ta sheet status

vel	Data sheet status [1]	Product status [2] [3]	Definitions
	Objective data	Development	This data sheet contains data from the objective specification for product development. Philips Semiconductors reserves the right to change the specification in any manner without notice.
	Preliminary data	Qualification	This data sheet contains data from the preliminary specification. Supplementary data will be published at a later date. Philips Semiconductors reserves the right to change the specification without notice, in order to improve the design and supply the best possible product.
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iting values definition — Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 60134). Stress above one or more of the limiting es may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given e Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.

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Date of release: 10-02

Document order number: 9397 750 10538

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XILINX® LogiCORE

DDS v5.0

April 28, 2005

Product Specification

ıres

p-in module for Virtex™, Virtex-E, Virtex-II, Virtex-II , Virtex-4, Spartan™-II, Spartan-IIE, Spartan-3, and ırtan-3E FPGAs

e, Cosine, or quadrature outputs

k-up table can be allocated to distributed or block nory

ıse dithering and Taylor series correction option vide high dynamic range signals using minimal ɔunt of FPGA resources. SFDR range is 18 dB to dB

ıse dithering removes the spectral line structure ɔciated with conventional phase truncation eform synthesis architectures

port for 1 to 16 independent channels

ı-precision synthesizer with fine frequency ɔlution (Δf = 0.02 Hz @ fclk = 100 MHz, 32-bit se accumulator)

32-bit two's complement output sample precision

ional phase offset capability providing support for iple synthesizers with precisely controlled phase rences

ple fixed-output frequency option

s relationally placed macro (RPM) mapping and ement technology for maximum and predictable ɔrmance

rporates Xilinx Smart-IP™ technology for utmost parameterization and optimum implementation

- For use with v7.1i and later of the Xilinx CORE Generator™ system

Applications

- Digital radios and modems
- Software-defined radios (SDR)
- Digital down/up converters for cellular and PCS base stations
- Waveform synthesis in digital phase locked loops
- Generating injection frequencies for analog mixers

General Description

Direct digital synthesizers (DDS), or numerically controlled oscillators (NCO), are important components in many digital communication systems. Quadrature synthesizers are used for constructing digital down and up converters, demodulators, and implementing various types of modulation schemes, including PSK (phase shift keying), FSK (frequency shift keying), and MSK (minimum shift keying). A common method for digitally generating a complex or real valued sinusoid employs a look-up table scheme. The look-up table stores samples of a sinusoid. A digital integrator is used to generate a suitable phase argument that is mapped by the look-up table to the desired output waveform. A simple user interface accepts system-level parameters such as the desired output frequency and spur suppression of the generated waveforms.

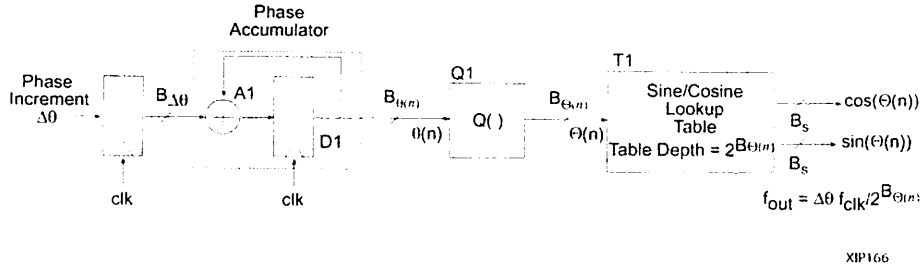


Figure 1: **Phase Truncation DDS (A simplified view of the DDS core)**

ıry of Operation

level view of the DDS Core is presented in .
egrator (components D1 and A1) computes a phase
ıat is mapped to a sinusoid (possibly complex) by the
ı table T1. The quantizer Q1, which is simply a slicer,
ş the high-precision phase angle $\Theta(n)$ and gener-
lower precision representation of the angle denoted
ı in the figure. This value is presented to the address
a look-up table that performs the mapping from
space to time.

elity of a signal formed by recalling samples of a
d from a look-up table is affected by both the phase
ıplitude quantization of the process. The length and
ıf the look-up table affect the signal's phase angle
on and the signal's amplitude resolution respec-
hese resolution limits are equivalent to time base jit-
to amplitude quantization of the signal, and add
l modulation lines and a white broad-band noise
the signal's spectrum.

ligital synthesizers use an addressing scheme with
opriate look-up table to form samples of an arbitrary
:cy sinusoid. If an analog output is required, the DDS
s these samples to a digital-to-analog converter
ınd a low-pass filter to obtain an analog waveform
ş specific frequency structure. Of course, the sam-
ş also commonly used directly in the digital domain.
k-up table traditionally stores uniformly spaced sam-
ə cosine and a sine wave. These samples represent
cycle of a length $N = 2^{B_{\Theta(n)}}$ prototype complex sinu-
d correspond to specific values of the sinusoid's
nt $\Theta(n)$ as shown in Eq.(1).

$$\Theta(n) = n\frac{2\pi}{N} \tag{1}$$

ı is the time series sample index.

wave symmetry in the basis waveform can be
d to construct a DDS that uses shortened tables. In
ıe, the two most significant bits of the quantized
ıngle $\Theta(n)$ are used to perform quadrant mapping.
ɔlementation results in a more area efficient imple-
ɔn because the memory requirements are mini-
either fewer FPGA block RAMs or reduced
ed memory. Based on the Core customization
ters, the DDS core will automatically employ quar-
ə symmetry when appropriate[1].

t Frequency

put frequency, f_{out}, of the DDS waveform is a func-
ıe system clock frequency f_{clk}, the number of bits
n the phase accumulator and the phase increment
θ. That is, $f_{out} = f\left(f_{clk}, B_{\Theta(n)}, \Delta\theta\right)$.

Output frequency in Hertz is defined as

$$f_{out} = \frac{f_{clk}\Delta\theta}{2^{B_{\Theta(n)}}}\ \text{Hz} \tag{2}$$

For example, if the DDS parameters are

$$\begin{aligned} f_{clk} &= 120\ \text{MHz} \\ B_{\Theta(n)} &= 10 \\ \Delta\theta &= 12_{10} \end{aligned} \tag{3}$$

the output frequency will be

$$\begin{aligned} f_{out} &= \frac{f_{clk}\Delta\theta}{2^{B_{\Theta(n)}}}\ \text{Hz} \\ &= \frac{120\times10^6\times12}{2^{10}} \\ &= 1.406250\ \text{MHz} \end{aligned} \tag{4}$$

The phase increment value required to generate an output frequency f_{out} Hz is

$$\Delta\theta = \frac{f_{out}2^{B_{\Theta(n)}}}{f_{clk}} \tag{5}$$

Frequency Resolution

The frequency resolution Δf of the synthesizer is a function of the clock frequency and the number of bits $B_{\Theta(n)}$ employed in the phase accumulator. The frequency resolution can be determined using the following equation

$$\Delta f = \frac{f_{clk}}{2^{B_{\Theta(n)}}} \tag{6}$$

For example, for the DDS parameters

$$\begin{aligned} f_{clk} &= 120\ \text{MHz} \\ B_{\Theta(n)} &= 32 \end{aligned} \tag{7}$$

the frequency resolution is

$$\begin{aligned} \Delta f &= \frac{f_{clk}}{2^{B_{\Theta(n)}}} \\ &= \frac{120\times10^6}{2^{32}} \\ &= 0.0279396\ \text{Hz} \end{aligned} \tag{8}$$

Phase Increment

The phase increment is an unsigned value. The phase increment term $\Delta\theta$ defines the synthesizer output frequency. Consider a DDS with the following parameterization

ry short tables, FPGA logic resources are actually minimized by storing a complete cycle. The user is not required to make any
ı decisions in this context; the CORE Generator will always produce the smallest core possible.

$$f_{clk} = 100\ \text{MHz}$$
$$B_{\theta(n)} = 28 \qquad (9)$$
$$B_{\Theta(n)} = 12$$

erate a sinusoid with frequency $f_{out} = 19$ MHz, the d phase increment would be

$$\Delta\theta = \frac{f_{out} 2^{B\Theta(n)}}{f_{clk}} = \frac{19\times10^6 \times 2^{12}}{100\times10^6} = 778.24 \qquad (10)$$

ral Purity Considerations

elity of a signal formed by recalling samples of a d from a look-up table is affected by both the phase ıplitude quantization of the process. The length and f the look-up table affect the signal's phase angle on and the signal's amplitude resolution respec- hese resolution limits are equivalent to time base jit- l to amplitude quantization of the signal and add l modulation lines and a white broad-band noise the signal's spectrum.

ınction with the system clock frequency, the phase ılator width determines the frequency resolution of S. The accumulator must have a sufficient field width the desired frequency resolution. For most practical ions, a large number of bits are allocated to the ıccumulator in order to satisfy the system frequency ɔn requirements. By way of example, if the required ɔn is 1 Hz, and the clock frequency is 100 MHz, the d field width of the accumulator is

$$B_{\theta(n)} = \log_2\left\lceil \frac{f_{clk}}{\Delta f} \right\rceil = \left\lceil \log_2 \frac{100\times10^6}{1} \right\rceil = \lceil 26.5754 \rceil = 27\ \text{bits} \qquad (11)$$

⌈ ⌉ denotes the ceiling operator. Due to excessive r requirements, the full precision of the phase accu- cannot be used to index the sine/cosine look-up quantized (or truncated) version of the phase angle for this purpose. The block labeled Q1 in the phase ɔn DDS, , performs the phase angle quanti- The lookup table can be located in block or distrib- ɜmory.

ing the phase accumulator introduces time base jit- e output waveform. As shown in Eq. (12), this jitter n undesired phase modulation that is proportional to ntization error.

$$\Theta(n) = \theta(n) + \delta\theta(n)$$
$$e^{j\Theta(n)} = e^{j[\theta(n)+\delta\theta(n)]} = e^{j\theta(n)} e^{j\delta\theta(n)}$$
$$e^{j\Theta(n)} \approx e^{j\theta(n)}[1 + j\delta\theta(n)] \approx e^{j\theta(n)} + j\delta\theta(n) e^{j\theta(n)} \qquad (12)$$

shows the look-up table addressing error, complex output time-series and the spectral domain representation of the output waveform produced by the DDS structure shown in . The normalized frequency for this signal is 0.022 Hz, which corresponds to phase accumulation steps of 7.92 degrees per output sample. The angular resolution of the 256-point look-up table is 360 / 256 or 1.40625 degrees per address, which is equivalent to 7.92 / 1.40625 or 5.632 addresses per output sample. Since the address must be an integer, the fractional part is discarded and the resultant phase jitter is the cause of the spectral artifacts. provides an exploded view of the spectral plot in (c).

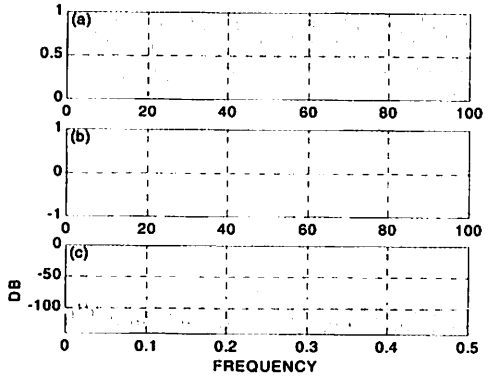


Figure 2: **Phase truncation DDS. $f_{out} = 0.022$ Hz, table depth = 256 12-bit precision samples. (a) Phase angle addressing error; (b) Complex output time series; (c) Output spectrum.**

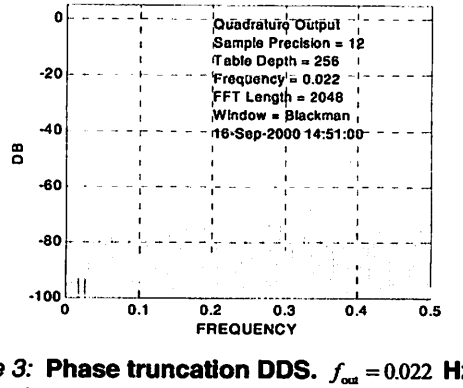
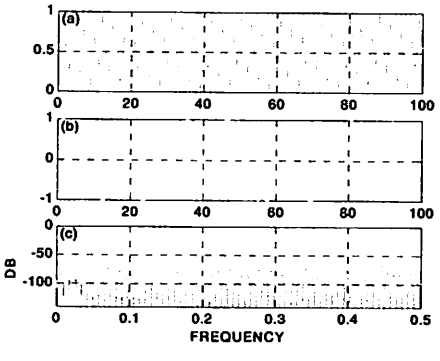


Figure 3: **Phase truncation DDS. $f_{out} = 0.022$ Hz, table depth = 256 12-bit precision samples. Exploded view of (c).**

ke two observations related to the phase jitter struc-
/el. Observe that the fractional part of the address
is a periodic (sawtooth) error sequence which is
sible for the harmonic rich (and aliased) low-level
modulation evident in Figure 3. We also note that the
istortion level due to incidental phase modulation is
imately 48 dB below the desired signal level, which is
ent with 6 dB/bit of address space. Put another way,
of spur suppression is required in the output wave-
is referenced to the 0 dB primary tone, the DDS
table must support at least $\lceil S/6 \rceil$ address bits. For
e, if S = 70 dB, which means that the highest spur
70 dB below the main signal, then the minimum num-
address bits for the lookup table is $\lceil 70/6 \rceil$ 12 bits;
a 4096-deep table.

and Figure 3 demonstrate the performance of a
DDS to the one presented in Figure 2 but in this
e 16-bit precision output samples have been used.
e that the highest spur is still at the –48 dB level, and
ng 4 additional bits to the output samples has not
ited to any further spur reduction. For a phase trun-
DDS, the only option to further reduce the spur levels
rease the depth of the look-up table.



4: **Phase truncation DDS. $f_{out} = 0.022$ Hz, table = 256 16-bit precision samples. (a) Phase angle ssing error. (b) Complex output time series. (c) Output spectrum.**

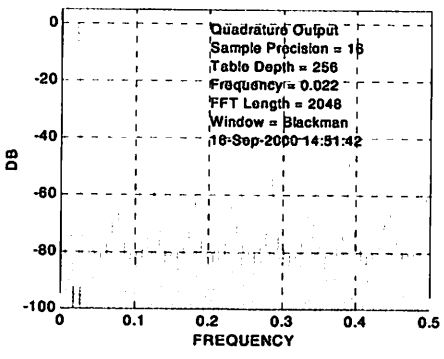


Figure 5: **Phase truncation DDS. $f_{out} = 0.022$ Hz, table depth = 256 16-bit precision samples. Exploded view of Figure 4 (c).**

Further examples illustrating the performance of various DDS configurations are shown in Figure 6 through Figure 15. The configuration details are annotated on the plot. For some of these examples, the synthesized frequency has been swept across a small range of the available output bandwidth. For these cases, the sweep start frequency, stop frequency, frequency increment δf and the number of tones in the sweep interval (*Num Tones*) is indicated. The analysis transform length and window function applied to the output time series is also indicated on the plots.

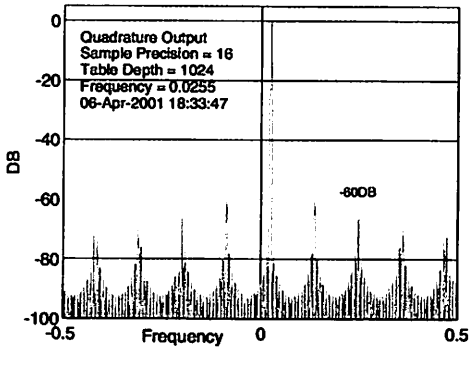


Figure 6:

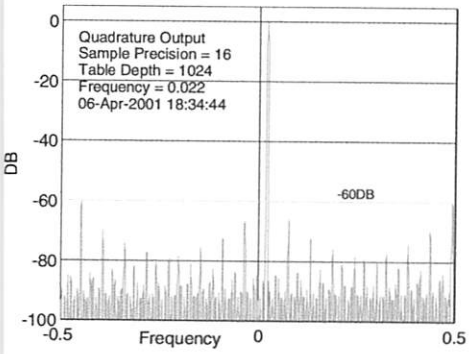


Figure 7:

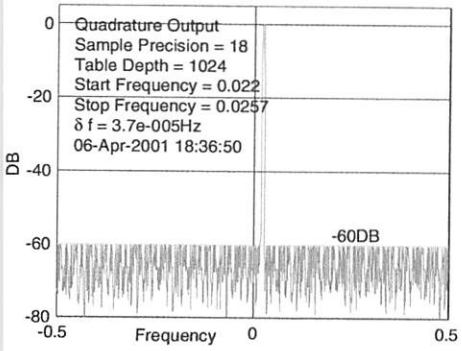


Figure 8:

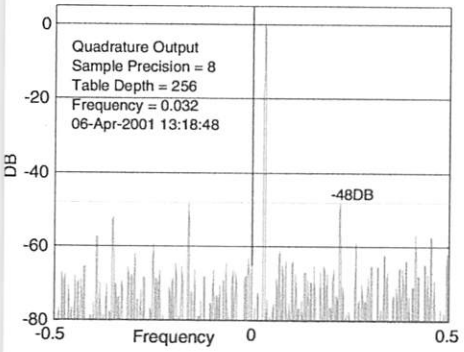


Figure 9:

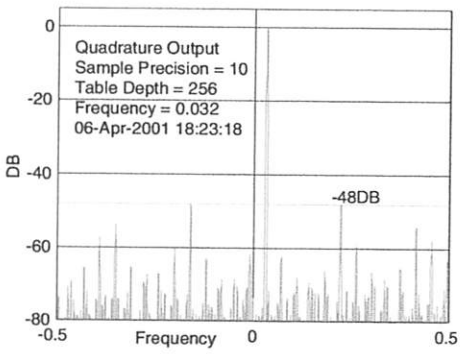


Figure 10:

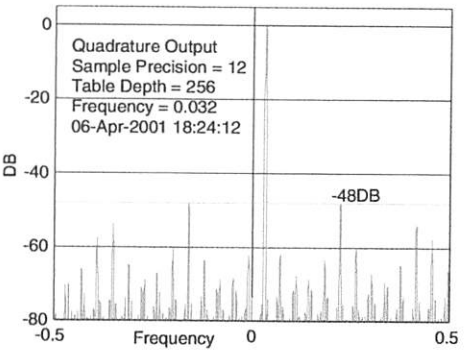


Figure 11:

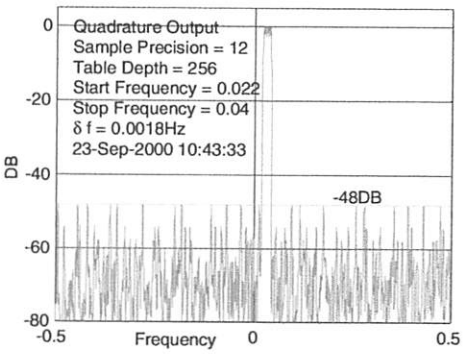


Figure 12:

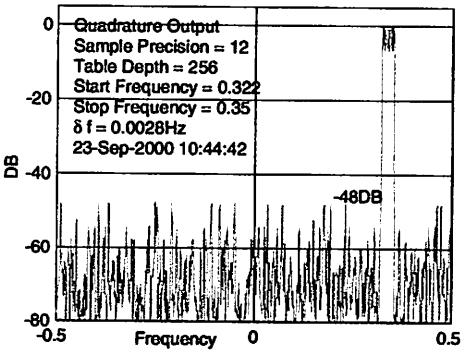


Figure 13:

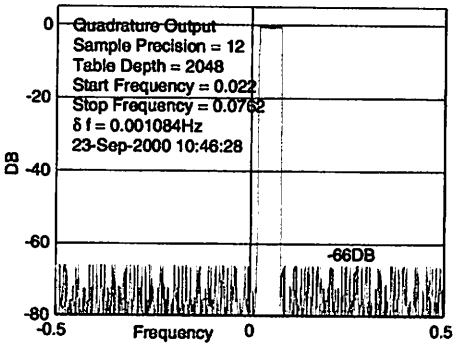


Figure 15:

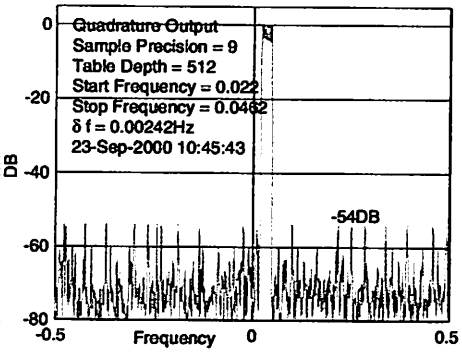


Figure 14:

Figure 1 provides a simplified view of the DDS core. A detailed view is shown in Figure 16. This detailed figure is similar to the simplified view, but also indicates the DDS control and interface *signals CE, A, WE, DATA, RFD* and *RDY*. Also note the inclusion of the *PHASE OFFSET* register designated *POFF*. This register is used for applying a constant phase offset to the phase slope computed in the phase accumulator *PACC*. When the Core is customized, the phase offset source can be defined as either a register, a constant, or it can be omitted entirely. When the *register* option is selected, the phase offset value is supplied via the *DATA* port. The phase offset value is treated as an unsigned quantity. If necessary, the phase offset is zero-extended before it is added to the phase accumulator.

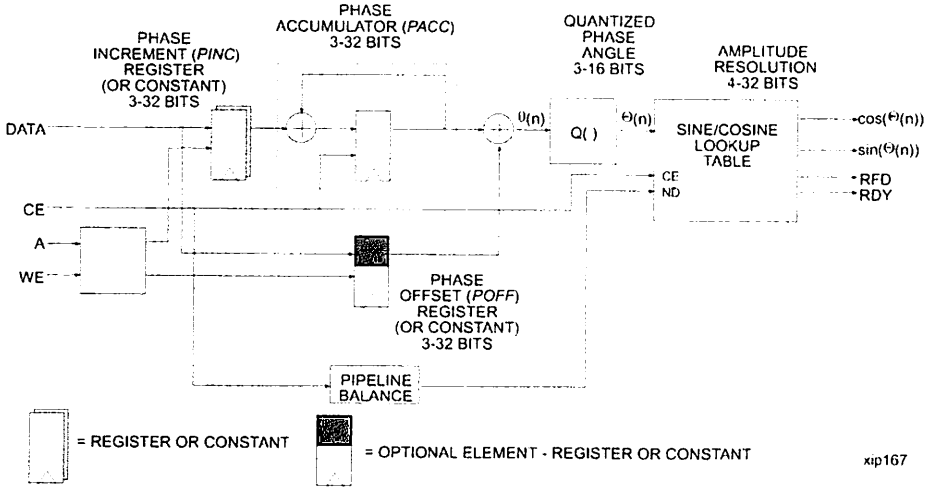
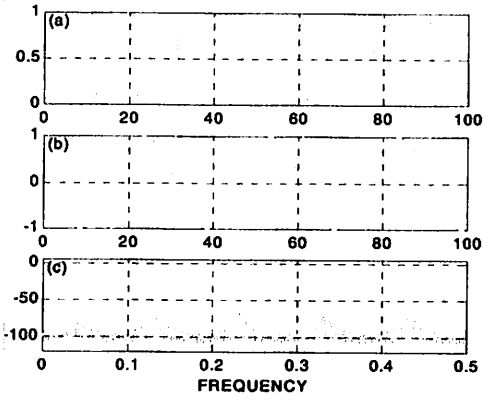


Figure 16: **DDS Core (Detailed View)**

ase increment value can be sourced from either a register or a constant. When the registered option is selected, the ort supplies the phase increment value to the phase increment register. When the *constant* option is selected, the tput frequency is fixed and cannot be adjusted once the core is embedded in a design.

;e Dithered DDS

)hase truncation DDS architecture shown in
antizer Q1 introduces a phase error in the phase
y discarding the least significant part, actually frac-
omponent, of the high-precision phase accumulator.
ase error due to the discarded fractional part of the
s count is a periodic series which results in an
ed spectral line structure. provides an
e of this process for a DDS with a table depth
and table sample precision of 16 bits. (a)
phase error generated by taking the difference
n the quantizer input and output signals,
ie output time series and (c) is the signal
spectrum. Observe in (a) the periodic saw-
ructure of the phase error signal. The line spectrum
ite with this correlated error sequence is impressed
inal output waveform and results in spectral lines in
thesizer output spectrum. These spurious compo-
an be clearly seen in (c).



e 17: **DDS plots showing (a) phase error time
es, (b) complex output time series, (c) output
trum. 1024 deep lookup table, 16-bit samples,
output frequency is 0.333 Hz.**

This structure can be suppressed by breaking up the regularity of the address error with an additive randomizing signal. This randomizing sequence, called *dither*, is a noise sequence, with variance approximately equal to the least significant integer bit of the phase accumulator. The dither sequence is added to the high-precision accumulator output prior to quantization by Q1. The resulting *dithered DDS* architecture is shown in .

The dithered DDS supplies, approximately, an additional 12 dB of spurious free dynamic range (SFDR) in comparison to a phase truncation design. The additional logic resources required to implement the dither sequence generator are not significant.

To provide S dB of spur suppression using a phase truncation DDS, as referenced to the 0 dB primary tone, the internal lookup table must support at least $\lceil S/6 \rceil$ address bits. To achieve this same performance using the dithered architecture requires two fewer address bits, minimizing the number of block RAMs (or logic slices for a distributed memory implementation) used in the FPGA implementation. In summary, for a dithered DDS implementation, the number of address bits needed to support S dB spur suppression is equal to $\lceil S/6 \rceil$ 2.

, , and provide the results for several dithered DDS simulations. shows eight simulations for a complex dithered DDS employing a table depth $N = 4096$ and 16-bit precision samples. For each plot the output frequency is different and is annotated on the plot. A phase truncation design would typically generate output spurs 72 dB below the output frequency, independent of the actual value of the output frequency. Indicated on each of the plots by the parameter *A* is the peak spur level achieved for the simulation. The eight spurs are -88.12, -88.22, -86.09, -88.80, -87.21, -87.55, -87.83, -87.12 dB below the output frequency. The worst case value of -86.09 is 14.09 dB better than a similarly configured phase truncation DDS.

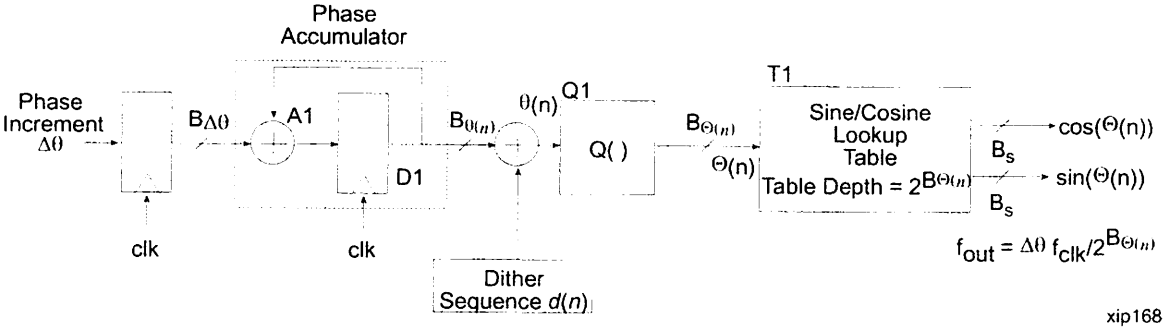
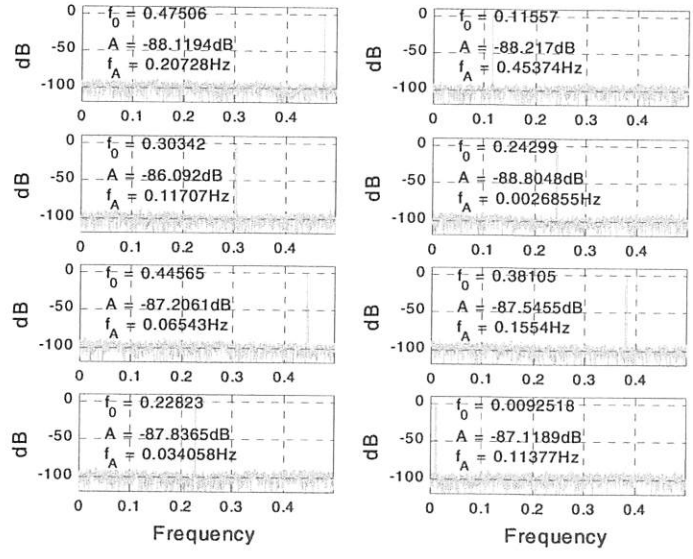


Figure 18: **Phase Dithered DDS Architecture**

eve this same SFDR by extending the table length of e truncation design would require extending the table e than a factor of four.

20 and Figure 21 provide two more dithered DDS ions where the output frequency is swept over a band of frequencies. The spectrum for each discrete tone in the sweep band is overlaid to construct the final plot. The sweep start frequency, end frequency, number of tones in the sweep, and DDS configuration are annotated on the plot.



re 19: **Dithered DDS Simulations. The DDS configuration is $N = 4096$, $B_s = 16$. The eight plots are spectral in representations for eight different output frequencies. Each plot is annotated with the peak spur level.**

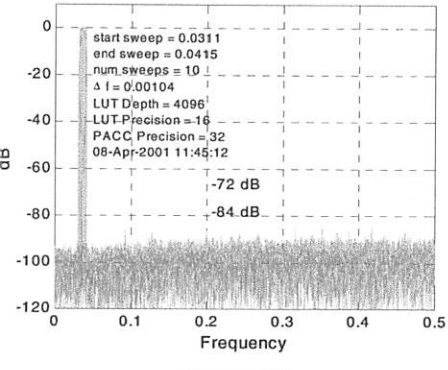


Figure 20:

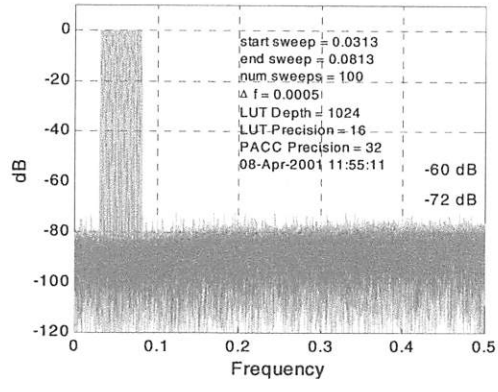


Figure 21:

e 20 the synthesized signal is swept over a range of cies starting from 0.0311 to 0.0415 Hz. There are s in the sweep separated in frequency by 0.00104 his example the phase truncation DDS would pro- ak spurs at –72 dB with respect to the 0 dB primary The dithered DDS provides approximately 12 dB better performance with the peak spur –84 dB below the output signal.

Figure 21 shows the results of a second swept frequency dithered DDS simulation. In this case the start frequency is 0.0313 Hz, the sweep termination frequency is 0.0813 Hz and there are 100 tones in the sweep. The frequency differential between successive simulations is 0.0005 Hz. A sim-

nfigured phase truncation DDS, with a table depth of 5-bit samples, would produce spurs approximately elow the output signal. Observe from the plot that ered DDS generates spurs that are 72 dB below the tput signal.

r advantage of the dithered DDS is that the spectral ucture present in a phase truncation design is d and the out-of-band signal is significantly whit- his white broadband noise floor is more desirable line structured spectrum. In digital communication s that use a DDS for generating mixing signals for ng channelization functions, the spurs in a phase n DDS can act as low-level mixing tones and cause ble spectral contamination of the desired channel. ally all applications the preferred implementation is ered DDS.

r Series Corrected DDS

se dithered DDS, as well as the phase truncation ve a quantizer Q1 which produces a lower precision discarding the fractional component of the high pre- n). The reason for this quantization step is to keep of the lookup memory to a reasonable size. The is spectral purity. With the availability of embedded rs in the Virtex-II, Virtex-II Pro, Spartan-IIE, and -3 FPGAs, it is now practical, from a silicon-area nt, to use the previously discarded fractional bits to corrections that can be added to the lookup table nd produce outputs with very high spurious free range (SFDR). These embedded multipliers are e multipliers and do not consume any of the logic he Taylor series correction DDS fixes a number of meters as described in the section oise Shaping. The additional resources required phase truncation DDS are two embedded multipli- constant coefficient multiplier, and four adders.

, , , and show the f four different Taylor series corrected DDS simula- e Taylor series corrected architecture uses a table = 4096 and 18-bit precision samples. However, the at the output of the feed-forward error processor is For each plot the output frequency is different and d directly on the plot. A similarly configured phase n DDS would produce spurs at –72 dB and a phase DDS at –84 dB. The peak spurs for the four plots .25, –118.13, –118.10, and –118.17 dB below the equency.

shows a swept frequency Taylor series corrected e starting frequency for this example is 0.0313 Hz, frequency is 0.0813 and there are 100 tones in the Using this configuration, a phase truncation DDS oduce peak spurs at approximately 72 dB below it signal and a phase dithered DDS would produce rs at approximately 84 dB below the output signal. n in the plot the Taylor series corrected DDS pro- duced spurs that were all the way down to 118 dB below the output signal. This result is 34 dB better than the phase dithering DDS, 46 dB better than the phase truncation DDS, and still only consumes a single 18Kb block RAM for the lookup storage. shows another frequency sweep simulation with 35 tones over a broader frequency range.

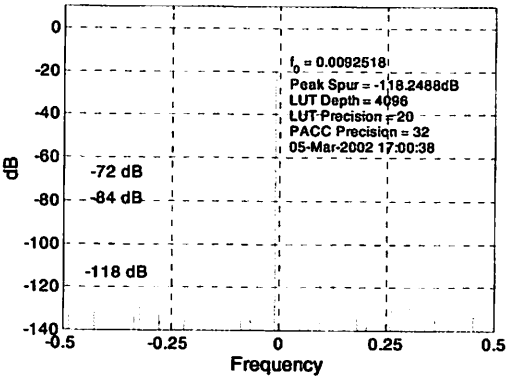


Figure 22: **Taylor series corrected DDS – single tone test. f_0 = 0.0092518.**

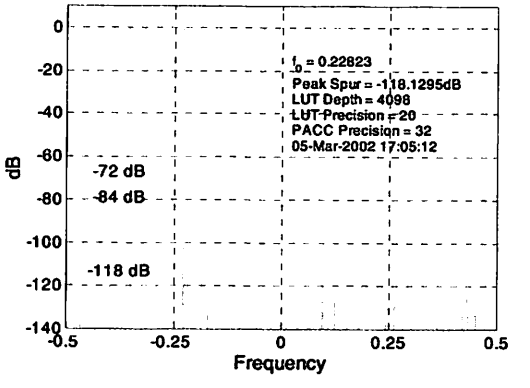
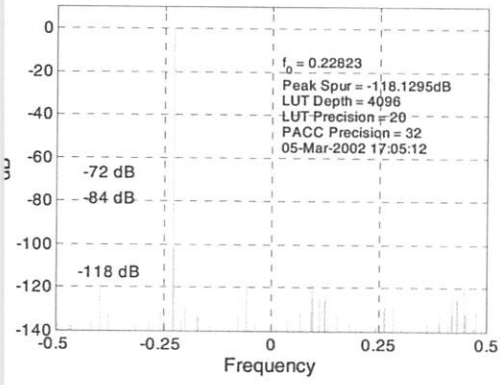
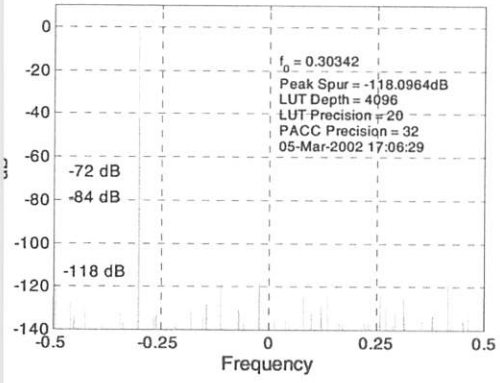


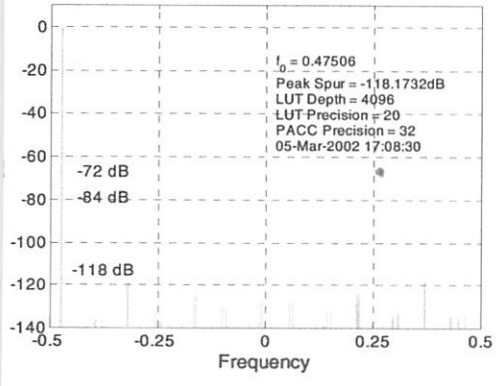
Figure 23: **Taylor series corrected DDS - single tone test. f_0 = 0.22823.**



e 24: **Taylor series corrected DDS - single tone test. f_0 = 0.22823.**



e 25: **Taylor series corrected DDS - single-tone test. f_0 = 0.30342.**



e 26: **Taylor series corrected DDS - single tone test. f_0 = 47506.**

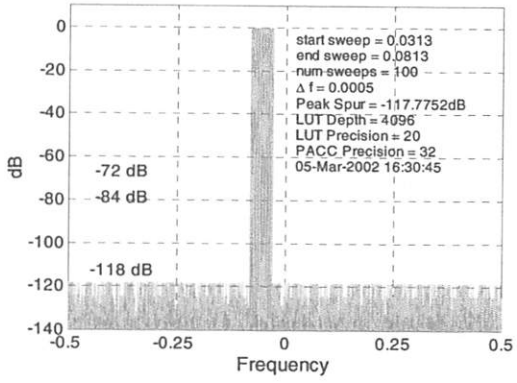


Figure 27: **Taylor series corrected DDS - frequency sweep simulation. 100 tones.**

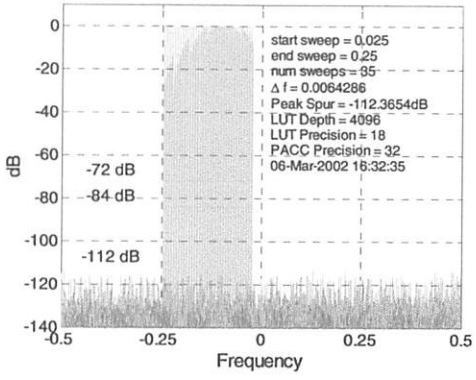


Figure 28: **Taylor series corrected DDS - frequency sweep simulation. 35 tones.**

Interface, Control, and Timing

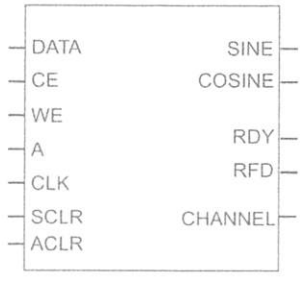


Figure 29: **DDS Symbol**

1: **Core Signal Pinout**

nal ne	Direction	Description
	Input	Master Clock - active rising edge.
	Input	Address select for writing to the phase increment (*PINC*) memory and the phase offset (*POFF*) memory. When A_{MSB}=0, the *PINC* memory is selected. When A_{MSB}=1, the *POFF* memory is selected. The four lower order bits of A are used to address up to 16 channels for the currently selected memory. The memory map is shown in Table 2.
	Input	Write enable - active high. Enables a write operation to the *PINC* or *POFF* memories.
	Input	Clock enable - active high. *CE* must be high during normal Core operation, but it is not required to be active during a write access to the *PINC* or *POFF* memories.
	Input	Time shared data bus. The *DATA* port is used for supplying values to the *PINC* or *POFF* memories.
	Input	Asynchronous clear - active high. When *ACLR* is asserted, the all registers in the Core are cleared. *RDY* is also deasserted.
	Input	Synchronous clear - active high. When *SCLR* is asserted, all registers in the Core are cleared. *RDY* is also deasserted.
	Output	Output data ready - active high. Indicates when the output samples are available.

Table 1: **Core Signal Pinout *(Continued)***

Signal Name	Direction	Description
RFD†	Output	Ready for data - active high. *RFD* is a dataflow control signal present on many Xilinx LogiCOREs. In the context of the DDS, it is supplied only for consistency with other LogiCOREs. This optional port is always tied to VCC.
CHANNEL†	Output	Channel index. Indicates which channel is currently available at the output when the DDS is configured for multi-channel operation. This is an unsigned two's complement signal. It's width is determined by the number of channels.
SINE	Output	Sine time-series.
COSINE	Output	Cosine time-series.

† denotes optional pin

Figure 10 shows the timing sequence for a single-channel DDS core. In this example, the DDS has both a phase increment *(PINC)* and a phase offset *(POFF)* memory. The *PINC* memory is first written with the *PINC* value 0x0010. This is realized by supplying the value on the *DATA* port and addressing the *PINC* memory by defining the MSB of the *A* port as A_{MSB}=0, as shown by the memory map in Table 2. Since this example is a single-channel case, the remaining four bits of the *A* port should be set to zeros. The write is performed on the positive clock edge. *WE* must be active; *i.e., WE*=1, to perform this operation. Immediately after the *PINC* memory is loaded, the value 0x1000 is written to the *POFF* memory. This requires A_{MSB}=1 and *WE*=1.

Table 2: **Phase Increment and Phase Offset memory map**

Address	Location Description
0 - 0	Phase Increment (PINC) values for channel 0 through 15
1 - 1	Phase Offset (POFF) values for channel 0 through 15

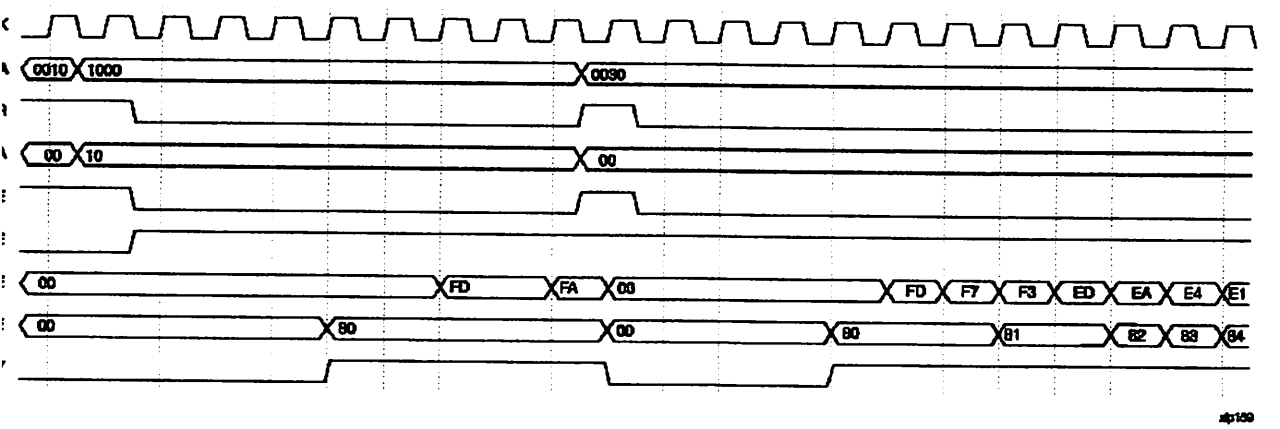


Figure 30: **DDS Timing: single-channel**

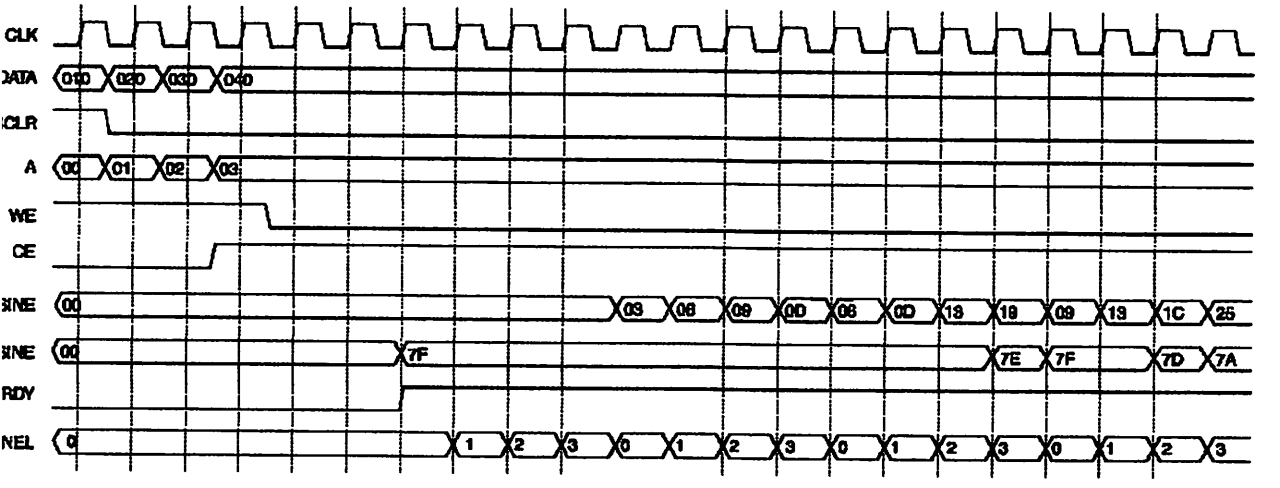


Figure 31: **DDS Timing: multichannel**

mory is loaded on the rising edge of the clock. *CE* ıt have to be active to write to either the *PINC* or nemories. The DDS will start operating once the ıable is applied (*CE*=1). Since *CE* is an optional pin, ınfigurations that do not include this pin will begin ıg once the FPGA is configured and the system active. After a start-up latency (measured from the n of *CE*[2]) that depends on the pipelining configura- sen for the core samples will be presented on the ort(s). This is indicated by *RDY*=1. For most config- , the assertion by the Core of *RDY* indicates the first tput sample. However, there is an exception. If a customized such that the *0-cycle* latency phase lator option is selected, and the sine-cosine look-up in distributed memory, and the table is purely combinatorial, any writes to the *PINC* register will be immediately reflected at the output port(s). This is irrespective of whether *CE* is asserted or not. In this situation, there are no registers between the *PINC* register and the output nodes, there is only a combinatorial arrangement of logic. Therefore, the *CE* pin cannot have any influence on this path through the system. The *CE* pin will, of course, still control the operation of the register (now in the upper arm of the phase accumulator shown in Figure 36 (b)) in the *PACC*. As illustrated in Figure 30, valid samples begin appearing at the output ports when *RDY* goes high.

The DDS can have an optional asynchronous clear or synchronous clear port. When either type of clear is applied, the *SINE* and *COSINE* output ports will assume a value of

ıing this part is present.

re 30 shows the *SCLR* being asserted and a new alue being written on the same clock. This results in oing low until the pipeline fills, and then back high valid samples are available again. The new *PINC* s 0x0030, which represents an output frequency that times that of the previous *PINC* value. The new out- mples can be seen to be changing at a faster rate, as ed.

31 shows the timing for a four-channel DDS imple- on. The *PINC* value for each channel is written on four clock cycles. Valid samples are available on the when the *RDY* signal goes high. The additional *NEL* port indicates which channel is currently avail- the output.

meters

)S parameterization screens are shown in Figure 32, 33, Figure 34, Figure 36, and Figure 37.

stomization parameter definitions are:

mponent Name: The user-defined DDS component ne.

nction: The DDS may have a quadrature output e and cosine), or a single output port — either sine osine. In addition, the sign of the output signal(s) be defined using the *Negative Sine* and *Negative sine* checkboxes. For example, if the quadrature out option is selected (*Sine and Cosine* GUI option), both the *Negative Sine* and *Negative Cosine* boxes unchecked, then the output signal *s(n)* is

$$s(n) = e^{j\Theta(n)} = \cos\Theta(n) + j\sin\Theta(n) \quad (13)$$

e Negative Sine box has been checked, the output nal is defined by

$$s(n) = e^{-j\Theta(n)} = \cos\Theta(n) - j\sin\Theta(n) \quad (14)$$

Channels: The DDS core can generate a single-channel implementation as well as a multichannel implementation with support for up to 16 independent channels. If a multichannel implementation is generated, all channels will time-share the DDS outputs.

- DDS Performance Options: Both system-level and circuit-level performance requirements are specified and the DDS core generates an implementation to meet these requirements
  - **DDS Clock Rate:** The frequency at which the DDS core will be clocked
  - **Spurious Free Dynamic Range (SFDR):** This parameter defines the frequency domain requirements of the out-of-band noise generated by the DDS outputs. The range is from 16 to 115 dB of spur suppression. Note that an SFDR value of 102 dB or greater will force an implementation employing a Taylor Series Correction which requires the use of embedded multipliers.
  - **Frequency Resolution:** This parameter determines the granularity of the tuning frequency. If the value entered is 10, the tuning frequency can be adjusted to a precision of 10 Hz. As an example, you could tune the DDS to a frequency of 5.00003 MHz.

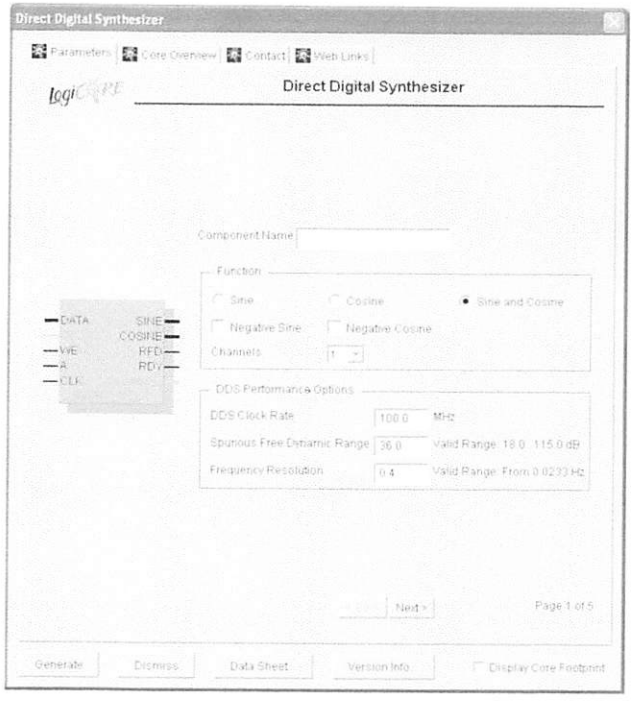


Figure 32: **DDS Parameterization Screen - Field 1**

tput Frequencies: For each channel, an lependent frequency can be entered into the table for e Sine and Cosine outputs. The allowable upper nge is displayed above the table and is calculated by king one half of the DDS clock rate and then dividing the total number of channels. This upper limit is quired so that the DDS clock rate does not drop low the Nyquist frequency.

Phase Increment: The user has the choice of making the output frequency a constant value or in-circuit changeable. Selecting *Fixed* will make the frequencies constant and selecting *Programmable* will allow the phase increment values to be changed in-circuit. If *Programmable* is selected, the values entered in the table will be the initial frequencies that take effect once the FPGA has been configured. If an ACLR or SCLR signal is asserted, the output frequencies settings will not be altered. Note that the *Fixed* or *Programmable* option is applied for all DDS channels.

ase Offset Angles: An independent offset can be ded to the phase angle of each channel by entering value into the table. The entered values will be ltiplied by 2π radians. The valid range is -1.0 to 1.0.

Phase Offset: The user has the choice of making the phase offset angles a constant value, in-circuit changeable, or not used. Selecting *Fixed* will make the offsets constant; selecting *Programmable* will allow them to be changed in-circuit; selecting *None* will prevent any offset from being added. If *Programmable* is selected, the values entered in the table will be the initial offsets that will take effect once the FPGA has been configured. If an ACLR or SCLR signal is asserted, the phase offset angles settings will not be altered. Note that the *Fixed*, *Programmable*, or *None* option is applied for all DDS channels.

- **Clear Options:** If the *ACLR Pin* is selected, the core will be generated with a asynchronous reset. If the *SCLR Pin* is selected, the core will be generated with a reset that is synchronized to the clock. When asserted, the internal logic returns to its initialized state. Note that all programmable values are retained. The Sine and Cosine output ports will be driven to zeros until enough clock cycles have passed to fill the core's internal pipeline, which can be determined by the Latency value.
- **Clock Enable:** The Core can have an optional clock enable port.

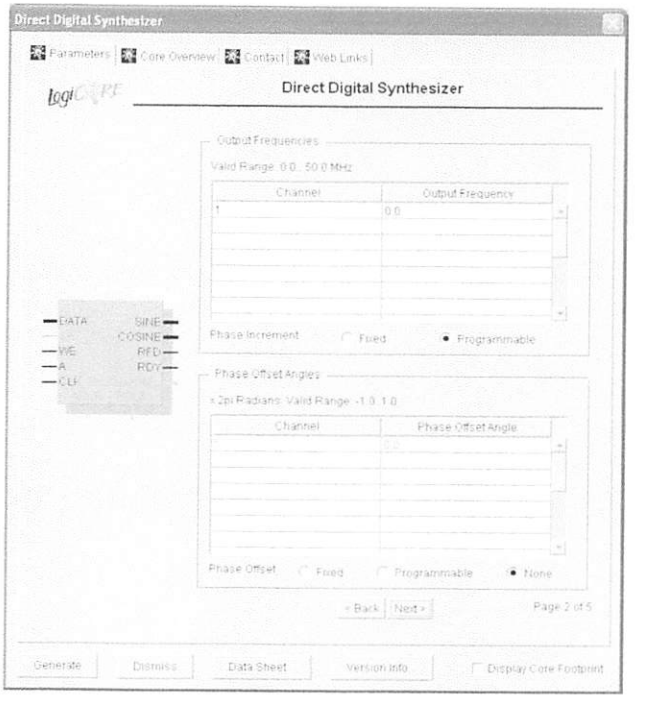
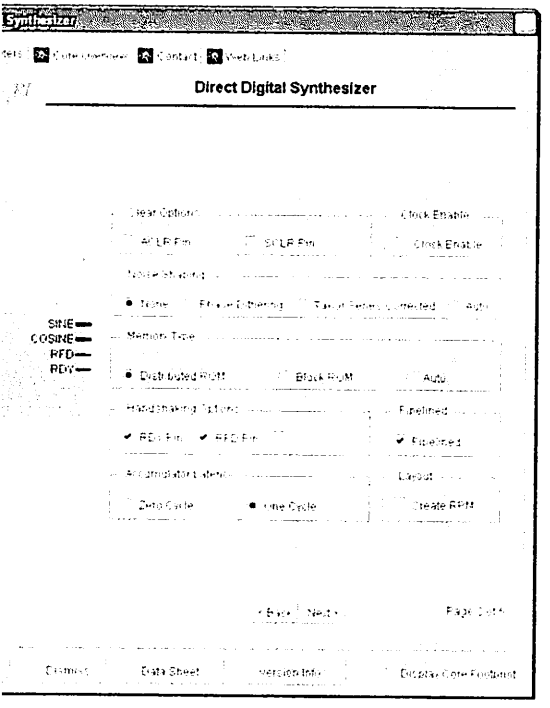


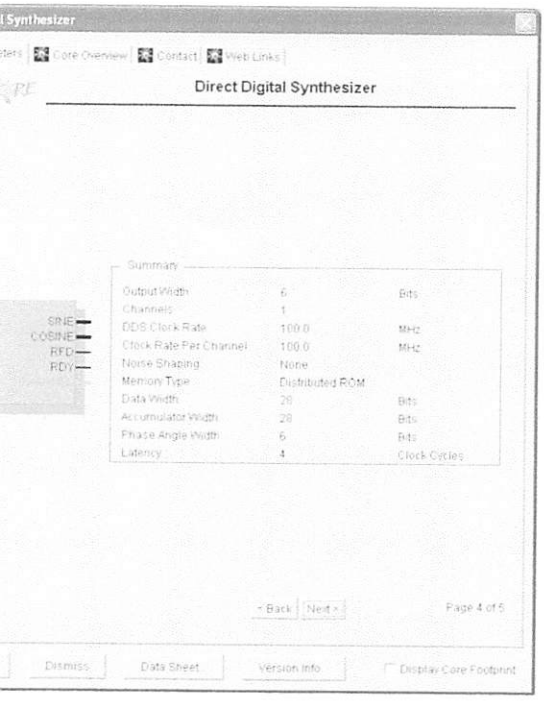
Figure 33: **DDS Parameterization Screen - Field 2**



34: **DDS Parameterization Screen - Field 3**

se Shaping: The radio buttons in this frame control ther a phase truncation, dithered DDS, or Taylor es corrected DDS implementation are generated. en *Auto* is selected, the noise-shaping type will be matically determined, based on other core meters including *SFDR*. When *None* is selected, a se truncation DDS is produced. When *Phase ering* is selected, a dithered DDS implementation is erated. When *Taylor Series Corrected* is selected, a or series corrected DDS implementation is erated. Taylor series corrected implementations are orted for only Virtex-II, Virtex-II Pro, Spartan-IIE, Spartan-3 FPGAs. The *Taylor Series Corrected* button will be disabled when other architectures selected. When *Taylor Series Corrected* is cted, the accumulator width will be fixed to 32 bits; the phase angle width will be fixed to 12 bits; the memory type will be fixed to block ROM; outputs required will be fixed to sine and cosine; negative sine will be fixed to true; negative cosine will be fixed to false; pipelining will be fixed to true, and the output width will be fixed to 20 bits.

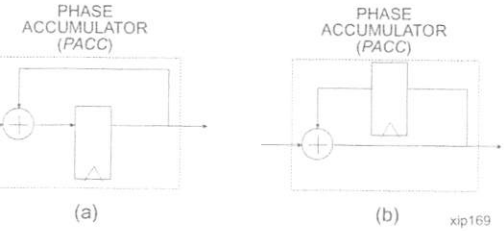
- **Memory Type:** This field controls the location of the DDS trigonometric lookup table. When *Distributed ROM* is selected, the table is placed in distributed memory. If *Block ROM* is selected, the table will be implemented using block memory. If *Auto* is selected, the actual memory type will be automatically determined, based on other core parameters, including *SFDR*.
- **Handshaking Options:** Optional handshaking ports—*RDY* and *RFD*—can be included on the Core. The *RFD* output signal is simply tied to VCC and is an optional port that can be included for compatibility with other Xilinx LogiCORE products that employ this style of dataflow interface. As shown in , the *RDY* output signal identifies when valid sine/cosine samples appear on these ports after the Core is started from rest — either after system power-on or a reset (synchronous or asynchronous). Any type of core reset will cause RDY to be removed (*RDY*=0). When the *Channels* parameter is set to a value of two or more and the *Channel Pin* parameter is selected, an additional output will be generated to indicate which channel the current output samples belong to.
- **Pipelined:** When *Pipelined* is selected, the core will be generated with pipelining registers inserted throughout the datapath. The insertion of pipeline registers enables the core to run at higher clock rates by shortening the delays between register stages. Pipelining increases the latency of the core, which is reported by the *Latency* value on the summary page of the GUI ( ). If *Pipelined* is not selected, the latency of the core will be zero when a distributed memory implementation has been selected and the latency will be one when a block memory implementation has been selected.



e 35: **DDS Parameterization Screen - Field 4**

ıse Accumulator: Phase accumulator precision. s field defines the precision of the *PACC* register ure 16). The location of the register in the phase umulator is controlled by the latency selection ons. When the *one-cycle* latency option is selected, phase accumulator will be as shown in re 36(a). When the *zero-cycle* option is selected, arrangement in Figure 36(b) is employed.

out: This checkbox controls whether a relationally ed MACRO (RPM) or a module with no placement rmation is generated. When checked, an RPM is luced.



igure 36: **Register Options for the Phase Accumulator--PACC**

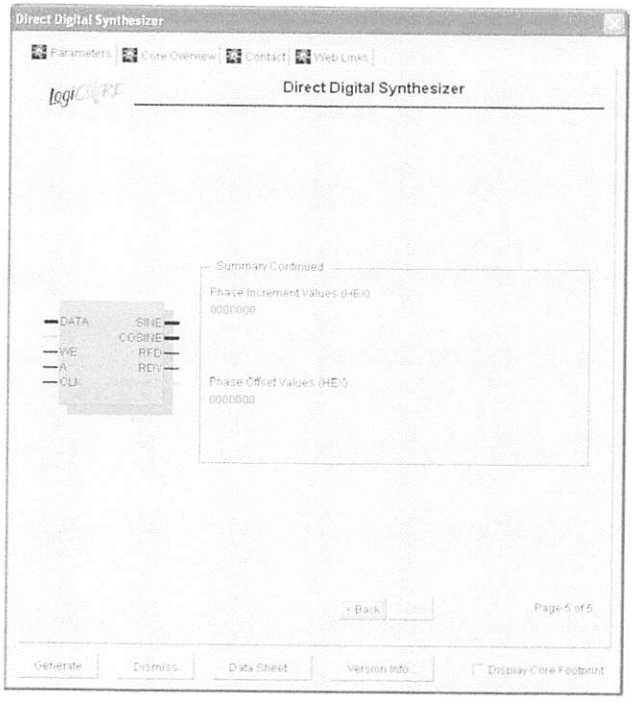


Figure 37: **DDS Parameterization Screen - Field 5**

Table 3: **Virtex Core Resource Utilization for Various Table Sizes (*Distributed ROM Implementation: 32-bit Data Width; 32-bit Phase Accumulator Width*)**

Phase Angle Width	Output Width	Single Output	Sine and Cosine
6*	8	32	49
	12	40	65
	16	48	81
	32	80	145
8	8	43	71
	12	53	91
	16	63	111
	32	103	191
10	8	95	175
	12	133	251
	16	171	327
	32	323	631

* Fullwave gets stored.

Note: Slice count is an approximation.

4: Virtex-II Core Resource Utilization for Various Table Sizes (*Distributed ROM nentation: 32-bit Data Width; 32-bit Phase Accumulator Width)*

ıase Angle Width	Output Width	Single Output	Sine and Cosine
6*	8	32	49
	12	40	65
	16	48	81
	32	80	145
8*	8	80	145
	12	112	209
	16	144	273
	32	272	529
10	8	89	162
	12	123	230
	16	157	296
	32	292	568

ve gets stored.
ce count is an approximation.

5: Virtex Core Resource Utilization for Various Table Sizes (*Block ROM Implementation: 32-bit Data Width; Phase Accumulator Width*)

eta dth	Output Width	Single Output		Sine and Cosine	
		No. of Slices	No. of Block ROMs	No. of Slices	No. of Block ROMs
5	8	16	1*	17	1*
	12	16	1*	17	1*
	16	16	1*	17	1*
	32	16	1*	62	2
3	8	16	1*	17	1*
	12	16	1*	17	1*
	16	16	1*	17	1*
	32	42	1	68	2
0	8	33	1	50	1
	12	35	1	54	1
	16	37	1	58	1
	32	45	2	74	2
3	8	37	4	59	4
	12	39	6	63	6
	16	41	8	67	8
	32	48	16	81	16

5: Virtex Core Resource Utilization for Various Table Sizes (*Block ROM Implementation: 32-bit Data Width; Phase Accumulator Width*) *(Continued)*

eta dth	Output Width	Single Output		Sine and Cosine	
		No. of Slices	No. of Block ROMs	No. of Slices	No. of Block ROMs
6	8	69	28	120	28
	12	87	44	156	44
	16	105	60	192	60
	32	239	124	461	124

: Virtex-II Core Resource Utilization for Various Table Sizes (*Block ROM Implementation: 32-bit Data Width; Phase Accumulator Width*)

e Angle Width	Output Width	Single Output		Sine and Cosine	
		No. of Slices	No. of Block ROMs	No. of Slices	No. of Block ROMs
6	8	16	1*	17	1*
	12	16	1*	17	1*
	16	16	1*	17	1*
	32	16	1*	17	1*
8	8	16	1*	17	1*
	12	16	1*	17	1*
	16	16	1*	17	1*
	32	16	1*	17	1*
10	8	16	1*	17	1*
	12	16	1*	17	1*
	16	16	1*	17	1*
	32	45	1	74	1
13	8	36	1	57	1
	12	38	2	61	2
	16	40	2	65	2
	32	49	4	83	4
16	8	39	7	62	7
	12	63	10	110	10
	16	65	14	114	14
	32	122	28	226	28

gets stored. *Note: Slice count is an approximation.*

litional logic required for the phase dithered DDS is 55 slices. The total slice count can be calculated by adding 55 f the slice count data shown in Table 3, Table 4, Table 5, and Table 6.

zation for the Taylor series corrected DDS is as follows: 315 slices; one 18Kb block RAM, and two 18x18s embed-tipliers.

File Parameters

'ameters supplied via the filter GUI are captured and logged to the.*xco* file. The full name of this file is simply the nent Name with an .xco file extension. Table 7 defines the .xco file parameter names and range specifications. 8 is an example .xco file.

': XCO File Parameter Names, Definitions, and Range Specifications

Parameter Name	Definition	Range
rmat	Controls the notation employed for identifying buses in the output edif netlist file	{BusFormatAngleBracket | BusFormatParen}
itionOutputProducts	Core HDL simulation selection — either VHDL or Verilog	{VHDL | VERILOG}
gicLibraryAlias	Pathname to Viewlogic directory	Valid path name for the user's operating system
amily	The FPGA target device family	{Virtex | Virtexe | Virtex2 | Virtex2p | Spartan2 | Spartan2e | Spartan3}
Flow	HDL flow specifier	{VHDL | VERILOG}
ndor	Design flow vendor information	{Other | Synplicity | Exemplar | Synopsis | Foundation}
ls	The number of independent channels the generated core will support	[1,...,16]
_rpm	When *create_rpm=true* a Core with embedded physical placement information is generated. If *create_rpm=false* the Core is generated without placement data.	{true | false}
d	This parameter controls the degree of pipelining employed in the sine/cosine lookup table. When set to *true* the table is fully pipelined. When set to *false* the minimum (zero for the case of a distributed ROM) number of pipeline registers are used.	{true | false}
haping	When *noise_shaping=Taylor_Series_Corrected,* a Taylor series corrected DDS is generated. When *noise_shaping=Phase_Dithering,* a dithered DDS is generated. When *noise_shaping=None,* a phase truncation DDS is generated. When *noise_shaping=Auto,* the noise shaping type will be determined by the core.	{Taylor_Series_Corrected | {Phase_Dithering | None | Auto}
nable	Clock enable. When *ce_enable=true* a clock enable port is included on the component. When *clock_enable=false* the clock enable port suppressed.	{true | false}
s_free_dynamic_range	A quantity that describes the spectral purity of the output waveforms	[18,...,115]

7: XCO File Parameter Names, Definitions, and Range Specifications *(Continued)*

Parameter Name	Definition	Range
ulator_latency	The user may control the position of the register in the phase accumulator. When *accumulator_register=ONE_CYCLE* the register location shown in [illegible](a) is employed. When *accumulator_register=ZERO_CYCLE*, the register location shown in [illegible](b) is employed.	{ONE_CYCLE I ZERO_CYCLE}
n	Synchronous clear. When *sclr_pin=true*, a synchronous reset port is included on the component. When *sclr_pin=false*, the synchronous re reset port suppressed.	{true I false}
ı	When *rdy_pin=true*, the DDS Core includes a *RDY* output signal. If *rdy_pin=false*, the *RDY* port is suppressed.	{true I false}
y_type	The sine/cosine samples can be stored in distributed or block memory. When *memory_type=Block_ROM*, the samples are stored in Block memory. When *memory_type=Distributed_ROM*, distributed memory is used. When *memory_type=Auto*, the memory type will be determined by the core.	{Block_ROM I Distributed_ROM I Auto}
increment	The phase increment value, that is the delta phase increment supplied to the phase accumulator, may be sourced (by the *PACC*) from either a memory (*phase_increment=Programmable*) or a constant (*phase_increment=Fixed*).	{Programmable I Fixed}
l_pin	If *channels* is greater than one, a *CHANNEL* port can optionally be added	{true I false}
ock_rate	Frequency of the DDS clock signal	[0,...,300]
ı	Asynchronous clear. When *aclr_pin=true*, an asynchronous reset port is included on the component. When *aclr_pin=false*, the asynchronous reset port suppressed.	{true I false}
ıent_name	Textbox that defines the DDS component name	Any valid file name for the user's operating system consisting of the letters a...z, 0...9 and '_'. The component name may be a maximum of 32 characters.
e_sine	Applicable only if a sine port has been specified for the particular core instance. When *negative_sine=false*, the signal presented at the *sine* port is sin $\theta(n)$. When negative_sine=true, the signal presented at the sine port is - sin $\theta(n)$.	{true I false}

7: XCO File Parameter Names, Definitions, and Range Specifications *(Continued)*

Parameter Name	Definition	Range
s_required	The DDS may be customized to provide a sine-only output (*function=Sine*), cosine-only output (*function=Cosine*) or both sine and cosine (quadrature) outputs (*function=Sine_and_Cosine*).	{Sine I Cosine I Sine_and_Cosine}
_frequencies	A comma-delimited set of frequency values. The number of values is determined by the *channels* value. Frequency values are decimals.	
ve_cosine	Applicable only if a cosine port has been specified for the particular core instance. When *negative_cosine=false*, the signal presented at the *cosine* port is cos $\theta(n)$. When *negative_cosine=true*, the signal presented at the cosine port is - cos $\theta(n)$.	{true I false}
	When *rfd_pin=true*, the DDS core includes a *RFD* output signal. If *rfd_pin=false*, the *RFD* port is suppressed.	{true I false}
_offset_angles	A comma-delimited set of phase offset angle factors. The number of values is determined by the *channels* value. Phase offset values are decimals from -1.0 to 1.0.	
ncy_resolution	A decimal value which determines the granularity of the *output_frequencies*	
_offset	As shown in Figure 16, an optional phase offset can be introduced at the output of the phase accumulator. When *phase_offset=Programmable*, this value is supplied by a memory. When *phase_offset=Fixed*, the phase offset is a constant that is supplied by the *phase_offset_angles* field when the core is elaborated. If *phase_offset=None*, no phase offset is included in the datapath.	{Programmable I Fixed I None}

```
# Xilinx CORE Generator 5.1.02i; Cores Update # 1
# Username = nyquist
# COREGenPath = c:\xilinx\coregen
# ProjectPath=C:\xilinx_projects\DSPGroup\ip_portfolio\dds\core
# ExpandedProjectPath = C:\xilinx_projects\DSPGroup\ip_portfolio\dds\core
# Core name: xco_example
SET BusFormat = BusFormatParen
SET SimulationOutputProducts = VHDL
SET ViewlogicLibraryAlias = ""
SET XilinxFamily = Virtex2
SET DesignFlow = VHDL
SET FlowVendor = Synplicity
SELECT Direct_Digital_Synthesizer Virtex2 Xilinx,_Inc. 4.2
CSET channels = 1
CSET create_rpm = true
CSET pipelined = true
CSET noise_shaping = Taylor_Series_Corrected
CSET clock_enable = true
CSET spurious_free_dynamic_range = 104
CSET accumulator_latency = One_Cycle
CSET sclr_pin = false
CSET rdy_pin = true
CSET memory_type = Block_ROM
CSET phase_increment = Programmable
CSET channel_pin = false
CSET dds_clock_rate = 100.0
CSET aclr_pin = false
CSET component_name = xco_example
CSET negative_sine = true
CSET outputs_required = Sine_and_Cosine
CSET output_frequencies = 33.333
CSET negative_cosine = false
CSET rfd_pin = false
CSET phase_offset_angles = 0.0
CSET frequency_resolution = 0.4
CSET phase_offset = None
GENERATE
```

Figure 38: **Example DDS XCO File**

Design Example 1

ɜr a DDS that is to satisfy the following requirements

frequency resolution $\Delta f = 0.25$ Hz
minimum spur suppression $S = 96$ dB
$f_{clk} = 120$ MHz
Quarature output: $s(n)=e^{-j(\Theta(n)+\phi)}\cos(\Theta(n)+\phi)\text{-}\sin(\Theta(n)+\phi))$
where the phase offset $\phi=+\pi/4$ radians

S GUI accepts system-level parameters instead of ıl parameters such as the width of the phase accu- width of the phase angle, etc. Because of this all of iirements above can be entered into the GUI directly having to calculate low-level core details. To illus- s example 1 will show some calculations that the ɜs automatically.

ld width of the phase accumulator (PACC in) defines the DDS frequency resolution according

$$\Delta f = \frac{f_{clk}}{2^{B_{\theta(n)}}} \qquad (15)$$

Therefore, the bit-precision for the PACC register is

$$\begin{aligned} B_{\theta(n)} &= \log_2\left\lceil \frac{f_{clk}}{\Delta f} \right\rceil \\ &= \left\lceil \log_2 \frac{120\times10^6}{0.25} \right\rceil \\ &= \lceil 28.838459 \rceil \\ &= 29 \text{ bits} \end{aligned} \qquad (16)$$

The spur suppression requirement is the dominant consideration when selecting the depth of the sine/cosine lookup table. Of course, the table samples must be specified with an appropriate precision to support this value. As noted in an earlier section of this document, each sine/cosine table address bit contributes approximately 6 dB of spur suppression. To meet the -96 dB spur level, the number of address bits required is

$$\begin{aligned} B_{\Theta(n)} &= \left\lceil \frac{96}{6} \right\rceil \\ &= \lceil 16 \rceil \\ &= 16 \text{ bits} \end{aligned} \qquad (17)$$

ɔle depth *N* is

$$N = 2^{B_{\theta(n)}} = 2^{16} = 65536 \text{ samples} \quad (18)$$

ase offset value *POFF* is determined as

$$\begin{aligned} \text{POFF} &= 2^{B_\theta} \cdot \frac{\phi}{2\pi} \\ &= \left\lceil 2^{29} \cdot \frac{\pi/4}{2\pi} \right\rceil \\ &= 67108864_{10} \end{aligned} \quad (19)$$

ərate a 10.2 MHz output signal the phase increment ɔe

$$\begin{aligned} \Delta\theta &= \frac{f_{out} 2^{B_{\theta(n)}}}{f_{clk}} \\ &= \frac{10.2\times10^6 \times 2^{29}}{120\times10^6} \\ &= \lceil 45634027.52 \rceil \\ &= 45634028 \end{aligned} \quad (20)$$

'INC is configured to be programmable then the out- ɪuency can be adjusted while the DDS is running. In ır the DDS to be tuned to 8.2 MHz the new *PINC* can ulated to be

$$\begin{aligned} \Delta\theta &= \frac{f_{out} 2^{B_{\theta(n)}}}{f_{clk}} \\ &= \frac{8.2\times10^6 \times 2^{29}}{120\times10^6} \\ &= \lceil 36686178.98 \rceil \\ &= 36686178 \end{aligned} \quad (21)$$

this new value to the *PINC* memory it must be pre- on the *DATA* port along with an active *WE* and iate address on the *A* port. The *DATA* port will the same width as the *PACC* which was calculated bits. The width of the DATA port is also reported on ( ) of the GUI. The PINC value represented -bit binary value is

'00100010111111001001011000'

is a spectral plot of the 10.2 MHz output signal. ɜ that the highest spur meets the 96 dB spur sup- ɪ requirement.

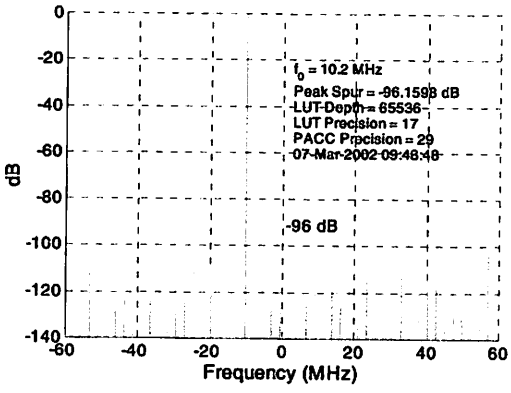


Figure 39: **Phase truncation DDS example 1. 10.2 MHz output tone. The highest spur is below the required 96 dB suppression value. The table depth is 65536 samples.**

In this example, the phase truncation DDS requires 16 of the 18Kb block RAMs for the lookup table storage. If a phase dithered DDS is used the table depth can be reduced to 16384 samples which reduces the memory requirement to 4 block RAMs. The output power spectrum for the preferred dithered DDS design is shown in Figure 40. Note that the minimum spur suppression has been achieved and the line structure of the spectrum shown in Figure 39 is no longer present.

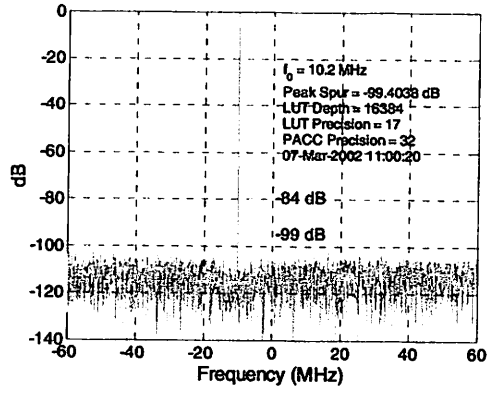
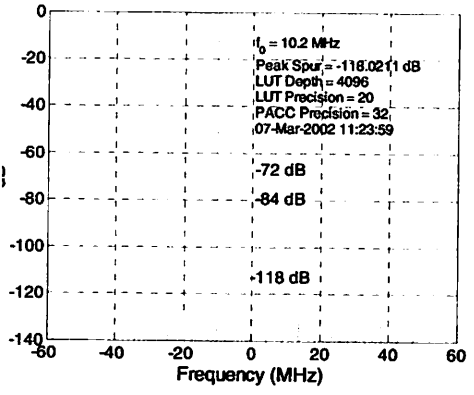


Figure 40: **Dithered DDS design for example 1. 10.2 MHz output tone.**

Using the dithered DDS, the highest spur, at -99.4038 dB, is well below the required 96 dB suppression value. If Virtex-II, Virtex-II Pro, Spartan-IIE, or Spartan-3 FPGAs are being used and two embedded multipliers are available the Taylor series corrected DDS can be used. While this architecture produces spurs at about -115 dB, which is much cleaner than the required -96 dB, the table depth is reduced to 4096 samples which fits in a single 18Kb block RAM. The output

spectrum for the Taylor series corrected DDS is in .



e 41: **Taylor series corrected DDS design for example 1, 1. 10.2Mhz output tone.**

ıe same requirements as before this example can ıded to use a multi-channel DDS. In doing so some ılculations change slightly. Assuming a four channel ; frequency resolution is defined by

$$\Delta f = \frac{\frac{f_{clk}}{channels}}{2^{B_{\theta(n)}}} \quad (22)$$

e, the bit-precision for the PACC register is

$$B_{\theta(n)} = \log_2\left[\frac{\frac{f_{clk}}{channels}}{\Delta f}\right] \quad (23)$$

$$= \left\lceil \log_2 \frac{\frac{120\times10^6}{4}}{0.25} \right\rceil$$

$$= \lceil 26.83845 \rceil$$

$$= 27 \text{ bits}$$

g that the four tones to be generated are 8.2 MHz, z, 12.2 MHz, and 14.2 MHz, the phase increment

$$\Delta\theta = \frac{f_{out}\,2^{B_{\theta(n)}}}{\frac{f_{clk}}{4}} \quad (24)$$

$$= \frac{f_{out}\times 2^{12}}{\frac{120\times10^6}{4}}$$

$$\Delta\theta_0 = 1120$$

$$\Delta\theta_1 = 1393$$

$$\Delta\theta_2 = 1666$$

$$\Delta\theta_3 = 1939$$

These four PINC values represented as 27-bit binary values are

$$\Delta\theta_0 = 000000000000000010001100000_2$$
$$\Delta\theta_1 = 000000000000000010101110001_2 \quad (25)$$
$$\Delta\theta_2 = 000000000000000011010000010_2$$
$$\Delta\theta_3 = 000000000000000011110010011_2$$

shows the power spectrum for the four-channel DDS implemented as a Taylor series corrected DDS.

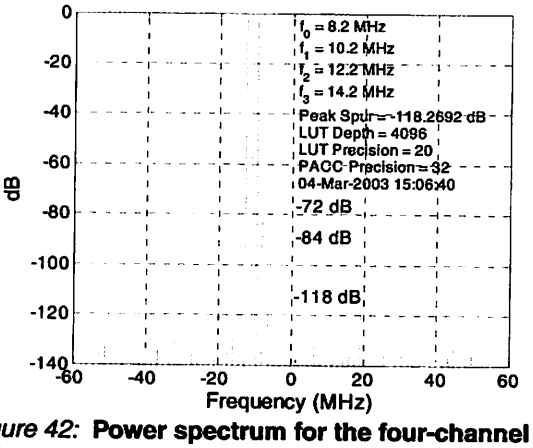


Figure 42: **Power spectrum for the four-channel DDS implemented as a Taylor series corrected DDS.**

Design Example 2

ler a DDS that is to satisfy the following requirements

frequency resolution $\Delta f = 0.3$ Hz
minimum spur suppression $S = 82$ dB
$f_{clk} = 80$ MHz
Quadrature output: $s(n)=e^{-j(\Theta(n)+\phi)}\cos(\Theta(n)+\phi)$-$\sin(\Theta(n)+\phi))$
where the phase offset ϕ=-50 degrees

DS GUI has been redesigned allowing the user to ystem-level parameters instead of low-level parame- ch as the width of the phase accumulator. Because all of the requirements above can be entered into the rectly without having to calculate low-level core As an exercise this example will show some calcula- at the core does automatically.

eld width of the phase accumulator (PACC in), defines the DDS frequency resolution according

$$\Delta f = \frac{f_{clk}}{2^{B_{\Theta(n)}}} \qquad (26)$$

ore, the bit-precision for the PACC register is

$$B_{(n)} \quad \log_2\left\lceil\frac{f_{clk}}{f}\right\rceil \quad \left\lceil\log_2\frac{80\ \ 10^6}{0.3}\right\rceil \quad \lceil 27.99046\rceil = 28 \text{ bits} \qquad (27)$$

ur suppression requirement is the dominant consid- when selecting the depth of the sine/cosine look-up f course, the table samples must be specified with opriate precision to support this value. As noted in er section of this document, each sine/cosine table bit contributes approximately 6 dB of spur suppres- meet the -82 dB spur level, the number of address uired is

$$B_{\Theta(n)} = \left\lceil\frac{82}{6}\right\rceil = \lceil 13.666\rceil = 14 \text{ bits} \qquad (28)$$

le depth N is

$$N = 2^{B_{\Theta(n)}} = 2^{14} = 16384 \text{ samples} \qquad (29)$$

example, the required phase offset has been speci- a negative value. The phase offset value -50 is the same as +310 degrees.

The phase offset value *POFF* is determined as

$$\text{POFF} = N \cdot \frac{\phi}{360} = \left\lceil 16384 \cdot \frac{310}{360}\right\rceil = 14336_{10} \qquad (30)$$

To generate an 8.4 MHz output signal, the phase increment would be

$$\Delta\theta = \frac{f_{out}\,2^{B_{\Theta(n)}}}{f_{clk}} = \frac{8.4\times10^6\times2^{14}}{80\times10^6} = \lceil 1720.32\rceil = 1720 \qquad (31)$$

If the DDS is configured such that the output frequency is programmable then the value of 1720 must be presented on the *DATA* port for writing to the *PINC* memory. The *DATA* port will assume the same width as the *PACC* which was calculated to be 28 bits. The *PINC* value represented as a 28-bit binary value is $\Delta\theta = 0001101011100001010001111011_2$.

Figure 43 is a spectral plot of the 8.4 MHz output signal. Observe that the highest spur meets the 82 dB spur suppression requirement.

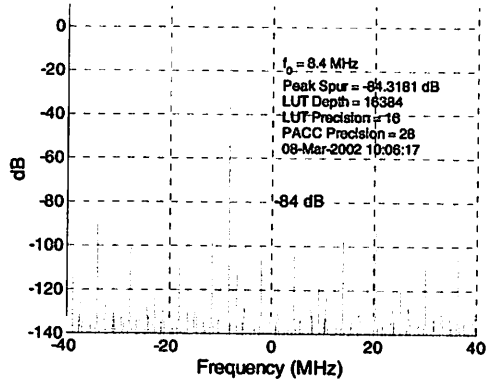
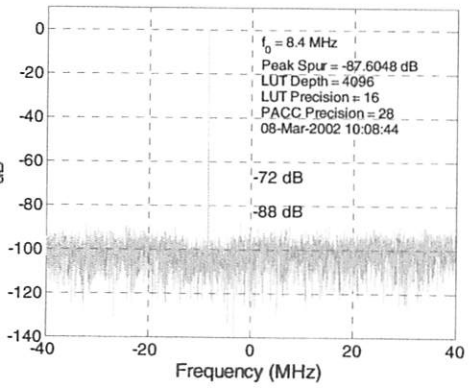


Figure 43: **Phase truncation DDS example 2. 8.4 MHz output tone. The highest spur is below the required 82 dB suppression value.**

The output power spectrum for the preferred dithered DDS design is shown Figure 44. In this case a 4096-deep table has been employed. Note that the minimum spur suppression has been achieved and the line structure of the spectrum shown in Figure 43 is no longer present. Since the desired spur suppression has been achieved while only consuming a single 18Kb block RAM the phase dithered DDS is the best area efficient solution, since moving to the Taylor series corrected architecture would require more resources.



44: **Dithered DDS Design for Example 2. 8.4 utput tone. Using the dithered DDS the highest pur, at 88 dB, is below the required 82 dB ssion value. The design uses a table that is one quarter the depth of the phase truncation implementation.**

sion History

owing table shows the revision history for this document.

te	Version	Revision
5/03	1.0	Initial revision history.
1/04	2.0	Updated document to support Xilinx software v6.2i and Virtex-4 FPGA.
3/05	2.1	Updated support for Spartan-3E and Xilinx ISE software v7.1i.

Ordering Information

This core may be downloaded from the Xilinx IP Center for use with the Xilinx CORE Generator system v7.1i and later. The CORE Generator system is bundled with the ISE Foundation software at no additional charge.

To order Xilinx software, please visit the Xilinx Silicon Xpresso Cafe or contact your local Xilinx sales representative.

Information on additional Xilinx LogiCORE modules is available on the Xilinx IP Center.

National Semiconductor

May 1999

DAC0808
8-Bit D/A Converter

General Description

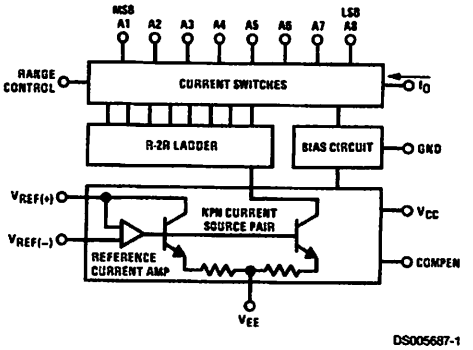
The DAC0808 is an 8-bit monolithic digital-to-analog converter (DAC) featuring a full scale output current settling time of 150 ns while dissipating only 33 mW with ±5V supplies. No reference current (I_{REF}) trimming is required for most applications since the full scale output current is typically ±1 LSB of 255 $I_{REF}/256$. Relative accuracies of better than ±0.19% assure 8-bit monotonicity and linearity while zero level output current of less than 4 µA provides 8-bit zero accuracy for $I_{REF} \geq 2$ mA. The power supply currents of the DAC0808 is independent of bit codes, and exhibits essentially constant device characteristics over the entire supply voltage range.

The DAC0808 will interface directly with popular TTL, DTL or CMOS logic levels, and is a direct replacement for the MC1508/MC1408. For higher speed applications, see DAC0800 data sheet.

Features

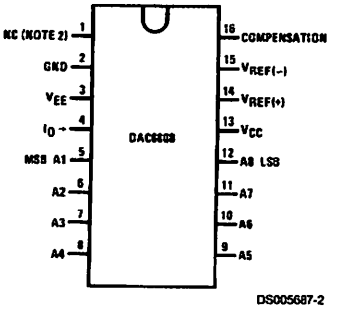
- Relative accuracy: ±0.19% error maximum
- Full scale current match: ±1 LSB typ
- Fast settling time: 150 ns typ
- Noninverting digital inputs are TTL and CMOS compatible
- High speed multiplying input slew rate: 8 mA/µs
- Power supply voltage range: ±4.5V to ±18V
- Low power consumption: 33 mW @ ±5V

Block and Connection Diagrams



DS005687-1

Dual-In-Line Package

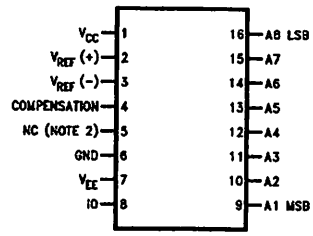


DS005687-2

Top View
Order Number DAC0808
See NS Package M16A or N16A

Block and Connection Diagrams (Continued)

Small-Outline Package



DS005687-13

Ordering Information

ACCURACY	OPERATING TEMPERATURE RANGE	N PACKAGE (N16A) (Note 1)		SO PACKAGE (M16A)
8-bit	0°C≤T_A≤+75°C	DAC0808LCN	MC1408P8	DAC0808LCM

Note 1: Devices may be ordered by using either order number.

solute Maximum Ratings (Note 2)

litary/Aerospace specified devices are required, e contact the National Semiconductor Sales Office/ ibutors for availability and specifications.

r Supply Voltage

:	+18 V_{DC}
:	−18 V_{DC}
l Input Voltage, V5–V12	−10 V_{DC} to +18 V_{DC}
ed Output Voltage, V_O	−11 V_{DC} to +18 V_{DC}
ence Current, I_{14}	5 mA
ence Amplifier Inputs, V14, V15	V_{CC}, V_{EE}
r Dissipation (Note 4)	1000 mW
Susceptibility (Note 5)	TBD
Storage Temperature Range	−65˚C to +150˚C
Lead Temp. (Soldering, 10 seconds)	
Dual-In-Line Package (Plastic)	260˚C
Dual-In-Line Package (Ceramic)	300˚C
Surface Mount Package	
Vapor Phase (60 seconds)	215˚C
Infrared (15 seconds)	220˚C

Operating Ratings

Temperature Range	$T_{MIN} \le T_A \le T_{MAX}$
DAC0808	$0 \le T_A \le +75$˚C

ctrical Characteristics

: 5V, V_{EE} = −15 V_{DC}, V_{REF}/R14 = 2 mA, and all digital inputs at high logic level unless otherwise noted.)

ol	Parameter	Conditions	Min	Typ	Max	Units
	Relative Accuracy (Error Relative to Full Scale I_O)	(*Figure 4*)				%
	DAC0808LC (LM1408-8)				±0.19	%
	Settling Time to Within ½ LSB (Includes t_{PLH})	T_A=25˚C (Note 7), (*Figure 5*)		150		ns
L	Propagation Delay Time	T_A = 25˚C, (*Figure 5*)		30	100	ns
	Output Full Scale Current Drift			±20		ppm/˚C
	Digital Input Logic Levels	(*Figure 3*)				
	High Level, Logic "1"		2			V_{DC}
	Low Level, Logic "0"				0.8	V_{DC}
	Digital Input Current	(*Figure 3*)				
	High Level	V_{IH} = 5V		0	0.040	mA
	Low Level	V_{IL} = 0.8V		−0.003	−0.8	mA
	Reference Input Bias Current	(*Figure 3*)		−1	−3	μA
	Output Current Range	(*Figure 3*)				
		V_{EE} = −5V	0	2.0	2.1	mA
		V_{EE} = −15V, T_A = 25˚C	0	2.0	4.2	mA
	Output Current	V_{REF} = 2.000V, R14 = 1000Ω, (*Figure 3*)	1.9	1.99	2.1	mA
	Output Current, All Bits Low	(*Figure 3*)		0	4	μA
	Output Voltage Compliance (Note 3)	$E_r \le 0.19\%$, T_A = 25˚C				
	V_{EE}=−5V, I_{REF}=1 mA				−0.55, +0.4	V_{DC}
	V_{EE} Below −10V				−5.0, +0.4	V_{DC}
	Reference Current Slew Rate	(*Figure 6*)	4	8		mA/μs
	Output Current Power Supply Sensitivity	−5V ≤ V_{EE} ≤ −16.5V		0.05	2.7	μA/V
	Power Supply Current (All Bits Low)	(*Figure 3*)				
				2.3	22	mA
				−4.3	−13	mA
	Power Supply Voltage Range	T_A = 25˚C, (*Figure 3*)				
			4.5	5.0	5.5	V_{DC}
			−4.5	−15	−16.5	V_{DC}
	Power Dissipation					

Electrical Characteristics (Continued)

(V_{CC} = 5V, V_{EE} = −15 V_{DC}, V_{REF}/R14 = 2 mA, and all digital inputs at high logic level unless otherwise noted.)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
	All Bits Low	V_{CC} = 5V, V_{EE} = −5V		33	170	mW
		V_{CC} = 5V, V_{EE} = −15V		106	305	mW
	All Bits High	V_{CC} = 15V, V_{EE} = −5V		90		mW
		V_{CC} = 15V, V_{EE} = −15V		160		mW

Note 2: Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. DC and AC electrical specifications do not apply when operating the device beyond its specified operating conditions.

Note 3: Range control is not required.

Note 4: The maximum power dissipation must be derated at elevated temperatures and is dictated by T_{JMAX}, θ_{JA}, and the ambient temperature, T_A. The maximum allowable power dissipation at any temperature is $P_D = (T_{JMAX} - T_A)/\theta_{JA}$ or the number given in the Absolute Maixmum Ratings, whichever is lower. For this device, T_{JMAX} = 125°C, and the typical junction-to-ambient thermal resistance of the dual-in-line J package when the board mounted is 100°C/W. For the dual-in-line N package, this number increases to 175°C/W and for the small outline M package this number is 100°C/W.

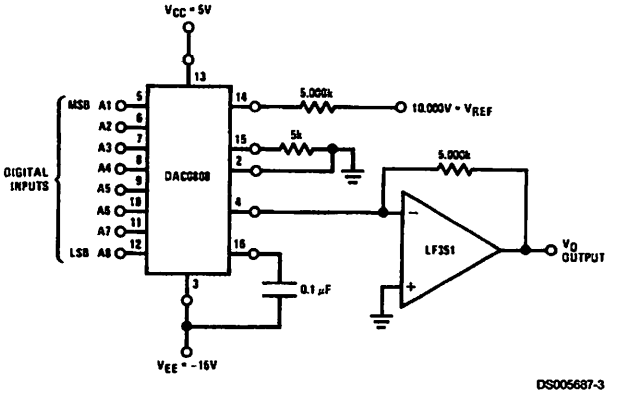
Note 5: Human body model, 100 pF discharged through a 1.5 kΩ resistor.

Note 6: All current switches are tested to guarantee at least 50% of rated current.

Note 7: All bits switched.

Note 8: Pin-out numbers for the DAL080X represent the dual-in-line package. The small outline package pinout differs from the dual-in-line package.

Typical Application



DS005687-3

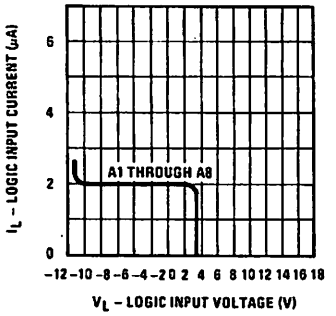
$$V_O = 10V\left(\frac{A1}{2}+\frac{A2}{4}+\ldots\frac{A8}{256}\right)$$

DS005687-23

FIGURE 1. +10V Output Digital to Analog Converter (Note 8)

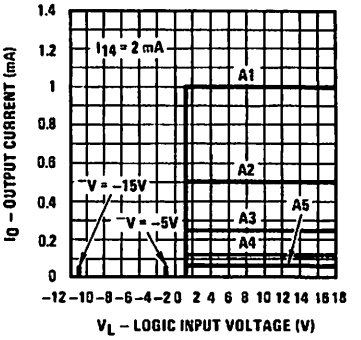
Typical Performance Characteristics V_{CC} = 5V, V_{EE} = −15V, T_A = 25°C, unless otherwise noted

Logic Input Current vs Input Voltage



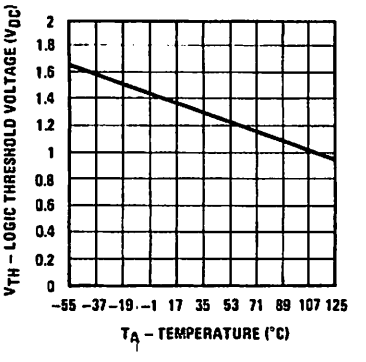
DS005687-14

Bit Transfer Characteristics



DS005687-15

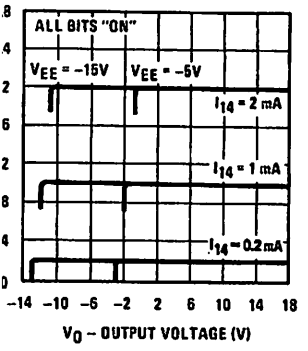
Logic Threshold Voltage vs Temperature



DS005687-16

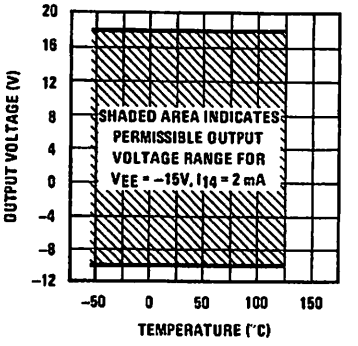
ıical Performance Characteristics V_{CC} = 5V, V_{EE} = −15V, T_A = 25°C, unless otherwise
(Continued)

ıt Current vs Output
ge (Output Voltage
ıliance)



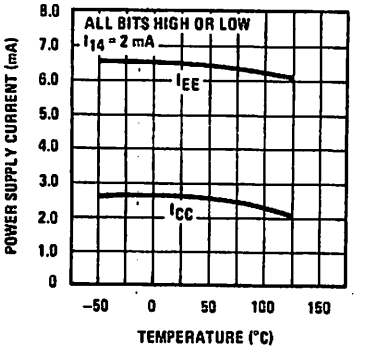
DS005687-17

Output Voltage Compliance vs Temperature



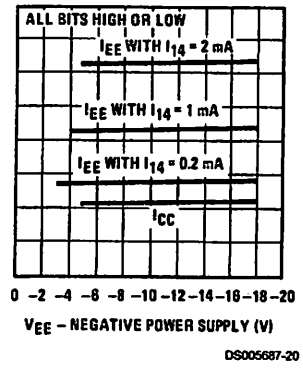
DS005687-18

Typical Power Supply Current vs Temperature



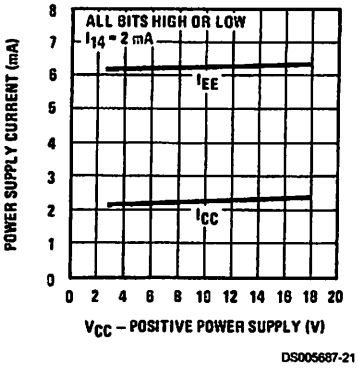
DS005687-19

ıl Power Supply
ıt vs V_{EE}



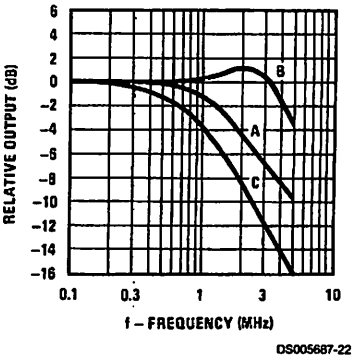
DS005687-20

Typical Power Supply Current vs V_{CC}



DS005687-21

Reference Input Frequency Response



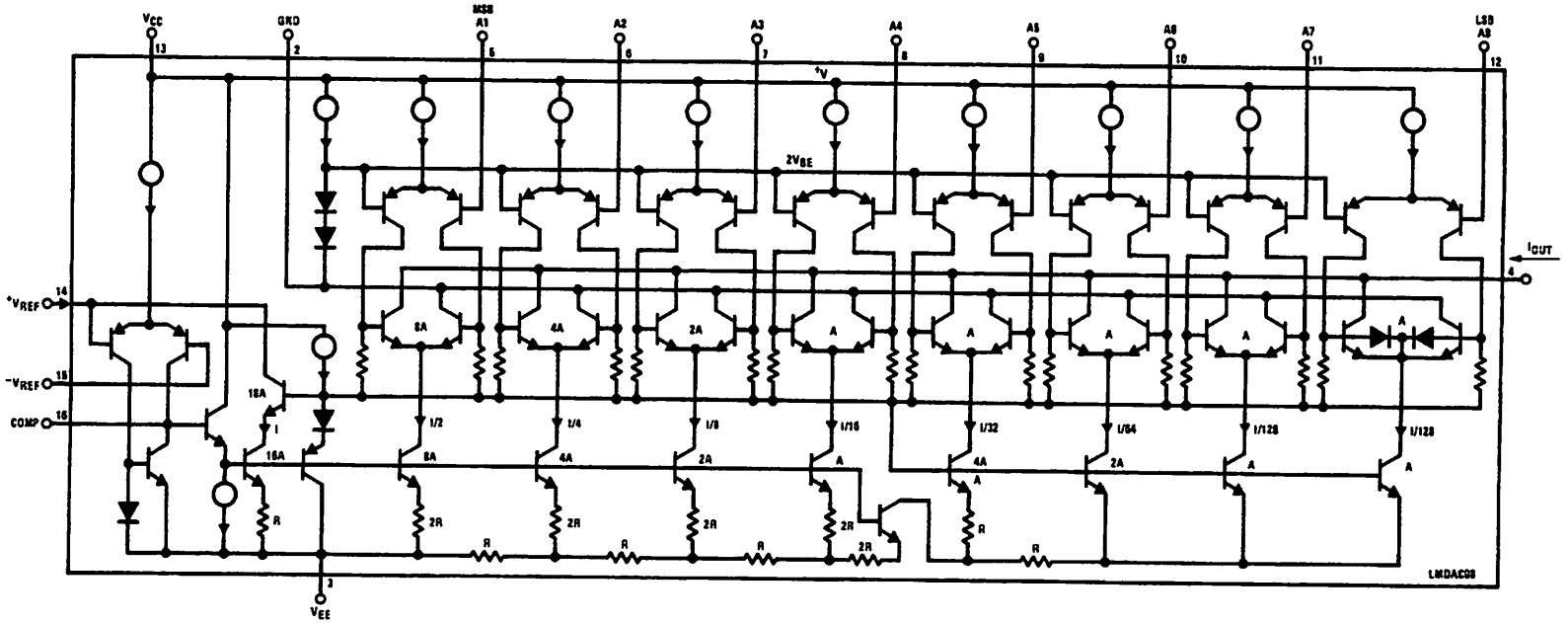
DS005687-22

, otherwise specified: R14 = R15 = 1 kΩ, C = 15 pF, pin 16 to V_{EE}, R_L = 50Ω, pin 4 to ground.

A: Large Signal Bandwidth Method of *Figure 7*, V_{REF} = 2 Vp-p offset 1V above ground.

B: Small Signal Bandwidth Method of *Figure 7*, R_L = 250Ω, V_{REF} = 50 mVp-p offset 200 mV above ground.

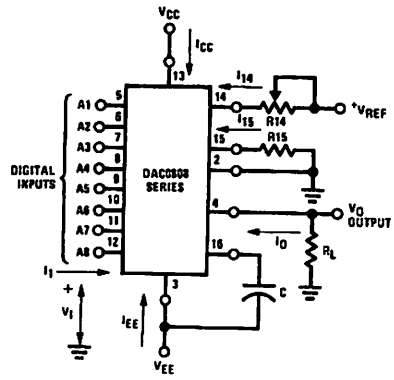
C: Large and Small Signal Bandwidth Method of *Figure 9* (no op amp, R_L = 50Ω), R_S = 50Ω, V_{REF} = 2V, V_S = 100 mVp-p
ed at 0V.



DS005687-4

FIGURE 2. Equivalent Circuit of the DAC0808 Series (Note 8)

st Circuits



DS005687-6

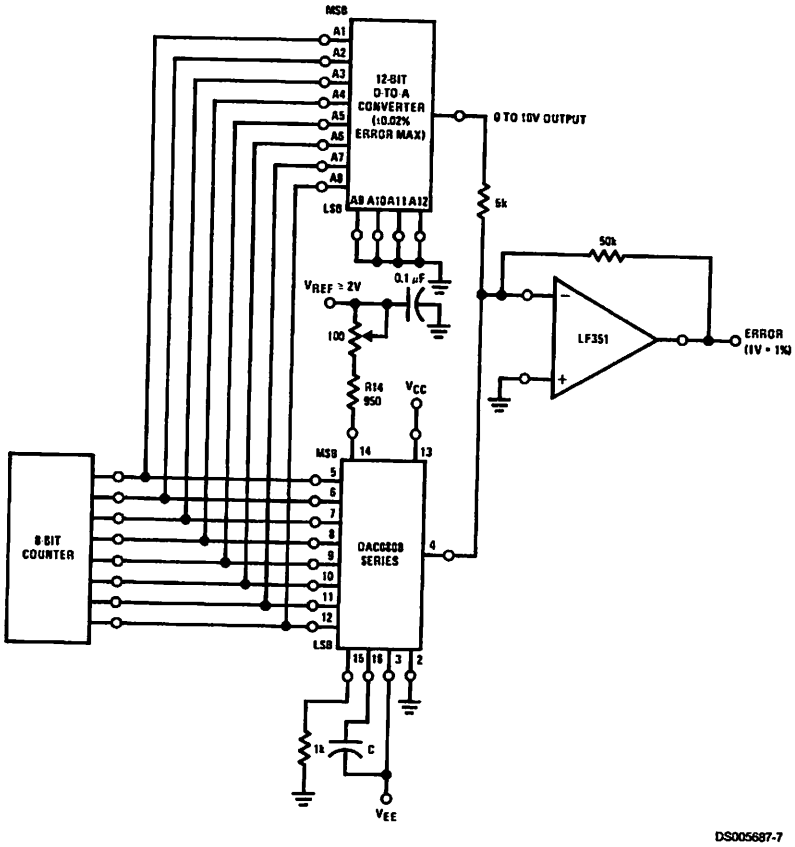
I_1 apply to inputs A1–A8.
sistor tied to pin 15 is to temperature compensate the bias current and may not be necessary for all applications.

$$= K\left(\frac{A1}{2}+\frac{A2}{4}+\frac{A3}{8}+\frac{A4}{16}+\frac{A5}{32}+\frac{A6}{64}+\frac{A7}{128}+\frac{A8}{256}\right)$$

$$\text{re } K \cong \frac{V_{REF}}{R14}$$

= "1" if A_N is at high level
)" if A_N is at low level

FIGURE 3. Notation Definitions Test Circuit (Note 8)



DS005687-7

FIGURE 4. Relative Accuracy Test Circuit (Note 8)

Test Circuits (Continued)

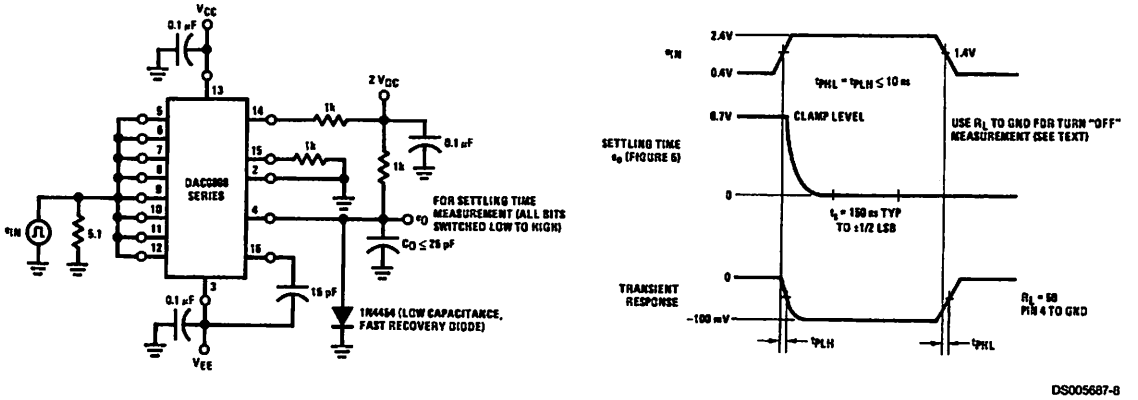


FIGURE 5. Transient Response and Settling Time (Note 8)

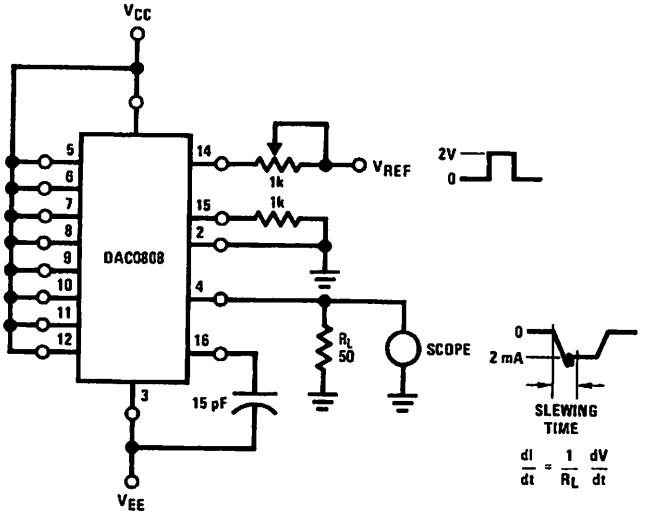


FIGURE 6. Reference Current Slew Rate Measurement (Note 8)

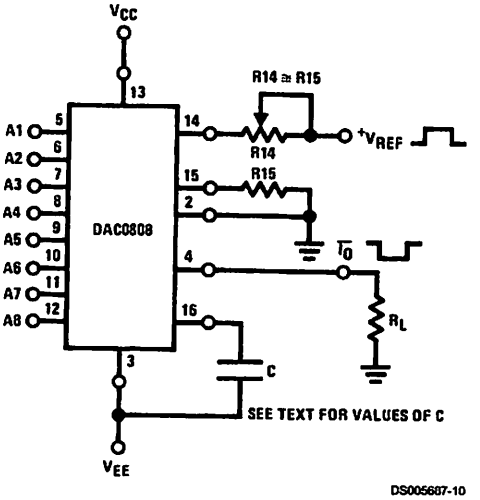


FIGURE 7. Positive V_{REF} (Note 8)

ɜt Circuits (Continued)

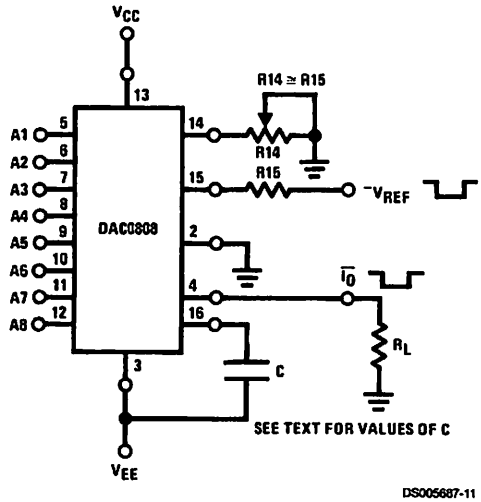


FIGURE 8. Negative V_{REF} (Note 8)

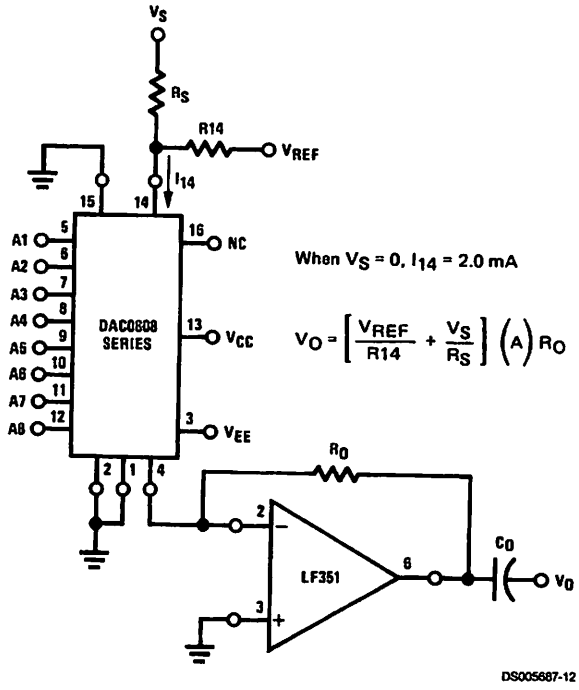


FIGURE 9. Programmable Gain Amplifier or Digital Attenuator Circuit (Note 8)

ɔlication Hints

RENCE AMPLIFIER DRIVE AND COMPENSATION

eference amplifier provides a voltage at pin 14 for rting the reference voltage to a current, and a round circuit or current mirror for feeding the ladder. ɔference amplifier input currrent, I_{14}, must always flow in 14, regardless of the set-up method or reference e polarity.

ɔctions for a positive voltage are shown in *Figure 7.* eference voltage source supplies the full current I_{14}.

For bipolar reference signals, as in the multiplying mode, R15 can be tied to a negative voltage corresponding to the minimum input level. It is possible to eliminate R15 with only a small sacrifice in accuracy and temperature drift.

The compensation capacitor value must be increased with increases in R14 to maintain proper phase margin; for R14 values of 1, 2.5 and 5 kΩ, minimum capacitor values are 15, 37 and 75 pF. The capacitor may be tied to either V_{EE} or ground, but using V_{EE} increases negative supply rejection.

A negative reference voltage may be used if R14 is grounded and the reference voltage is applied to R15 as shown in *Figure 8.* A high input impedance is the main

Application Hints (Continued)

advantage of this method. Compensation involves a capacitor to V_{EE} on pin 16, using the values of the previous paragraph. The negative reference voltage must be at least 4V above the V_{EE} supply. Bipolar input signals may be handled by connecting R14 to a positive reference voltage equal to the peak positive input level at pin 15.

When a DC reference voltage is used, capacitive bypass to ground is recommended. The 5V logic supply is not recommended as a reference voltage. If a well regulated 5V supply which drives logic is to be used as the reference, R14 should be decoupled by connecting it to 5V through another resistor and bypassing the junction of the 2 resistors with 0.1 µF to ground. For reference voltages greater than 5V, a clamp diode is recommended between pin 14 and ground.

If pin 14 is driven by a high impedance such as a transistor current source, none of the above compensation methods apply and the amplifier must be heavily compensated, decreasing the overall bandwidth.

OUTPUT VOLTAGE RANGE

The voltage on pin 4 is restricted to a range of −0.55 to 0.4V when V_{EE} = −5V due to the current switching methods employed in the DAC0808.

The negative output voltage compliance of the DAC0808 is extended to −5V where the negative supply voltage is more negative than −10V. Using a full-scale current of 1.992 mA and load resistor of 2.5 kΩ between pin 4 and ground will yield a voltage output of 256 levels between 0 and −4.980V. Floating pin 1 does not affect the converter speed or power dissipation. However, the value of the load resistor determines the switching time due to increased voltage swing. Values of R_L up to 500Ω do not significantly affect performance, but a 2.5 kΩ load increases worst-case settling time to 1.2 µs (when all bits are switched ON). Refer to the subsequent text section on Settling Time for more details on output loading.

OUTPUT CURRENT RANGE

The output current maximum rating of 4.2 mA may be used only for negative supply voltages more negative than −8V, due to the increased voltage drop across the resistors in the reference current amplifier.

ACCURACY

Absolute accuracy is the measure of each output current level with respect to its intended value, and is dependent upon relative accuracy and full-scale current drift. Relative accuracy is the measure of each output current level as a fraction of the full-scale current. The relative accuracy of the DAC0808 is essentially constant with temperature due to the excellent temperature tracking of the monolithic resistor ladder. The reference current may drift with temperature, causing a change in the absolute accuracy of output current. However, the DAC0808 has a very low full-scale current drift with temperature.

The DAC0808 series is guaranteed accurate to within ±½ LSB at a full-scale output current of 1.992 mA. This corresponds to a reference amplifier output current drive to the ladder network of 2 mA, with the loss of 1 LSB (8 µA) which is the ladder remainder shunted to ground. The input current to pin 14 has a guaranteed value of between 1.9 and 2.1 mA, allowing some mismatch in the NPN current source pair. The accuracy test circuit is shown in *Figure 4*. The 12-bit converter is calibrated for a full-scale output current of 1.992 mA. This is an optional step since the DAC0808 accuracy is essentially the same between 1.5 and 2.5 mA. Then the DAC0808 circuits' full-scale current is trimmed to the same value with R14 so that a zero value appears at the error amplifier output. The counter is activated and the error band may be displayed on an oscilloscope, detected by comparators, or stored in a peak detector.

Two 8-bit D-to-A converters may not be used to construct a 16-bit accuracy D-to-A converter. 16-bit accuracy implies a total error of ±½ of one part in 65,536 or ±0.00076%, which is much more accurate than the ±0.019% specification provided by the DAC0808.

MULTIPLYING ACCURACY

The DAC0808 may be used in the multiplying mode with 8-bit accuracy when the reference current is varied over a range of 256:1. If the reference current in the multiplying mode ranges from 16 µA to 4 mA, the additional error contributions are less than 1.6 µA. This is well within 8-bit accuracy when referred to full-scale.

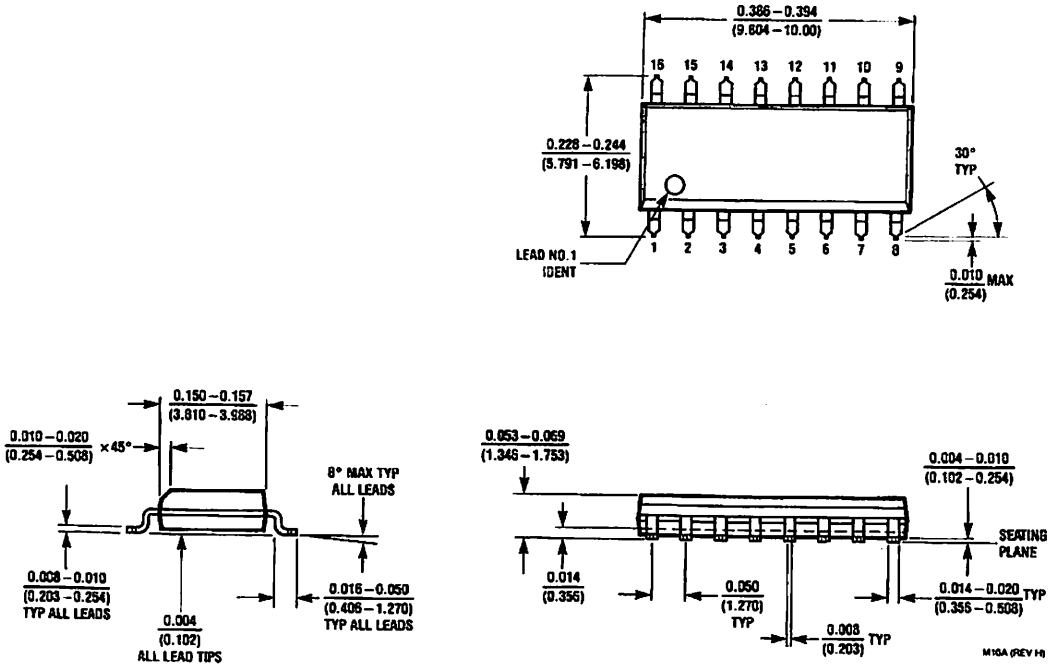
A monotonic converter is one which supplies an increase in current for each increment in the binary word. Typically, the DAC0808 is monotonic for all values of reference current above 0.5 mA. The recommended range for operation with a DC reference current is 0.5 to 4 mA.

SETTLING TIME

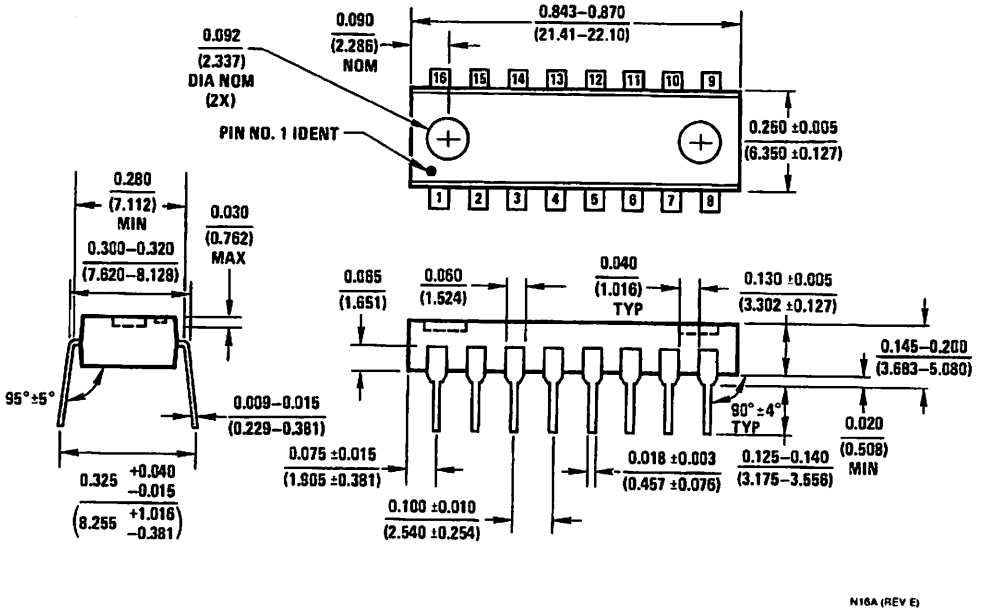
The worst-case switching condition occurs when all bits are switched ON, which corresponds to a low-to-high transition for all bits. This time is typically 150 ns for settling to within ±½ LSB, for 8-bit accuracy, and 100 ns to ½ LSB for 7 and 6-bit accuracy. The turn OFF is typically under 100 ns. These times apply when $R_L \leq 500\Omega$ and $C_O \leq 25$ pF.

Extra care must be taken in board layout since this is usually the dominant factor in satisfactory test results when measuring settling time. Short leads, 100 µF supply bypassing for low frequencies, and minimum scope lead length are all mandatory.

sical Dimensions inches (millimeters) unless otherwise noted



Small Outline Package
Order Number DAC0808LCM
NS Package Number M16A



Dual-In-Line Package
Order Number DAC0808
NS Package Number N16A

Notes

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M-8870
DTMF Receiver

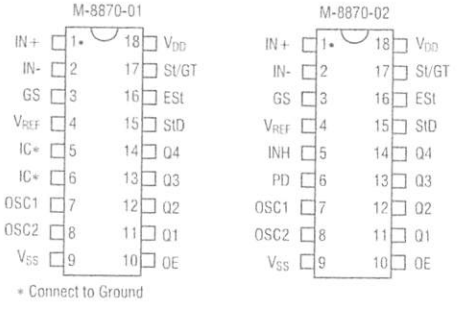
tures

ow Power Consumption
djustable Acquisition and Release Times
entral Office Quality and Performance
ower-down and Inhibit Modes (-02 only)
expensive 3.58 MHz Time Base
ngle 5 Volt Power Supply
al Tone Suppression

lications

lephone switch equipment
emote data entry
aging systems
ersonal computers
redit card systems

Configuration



Description

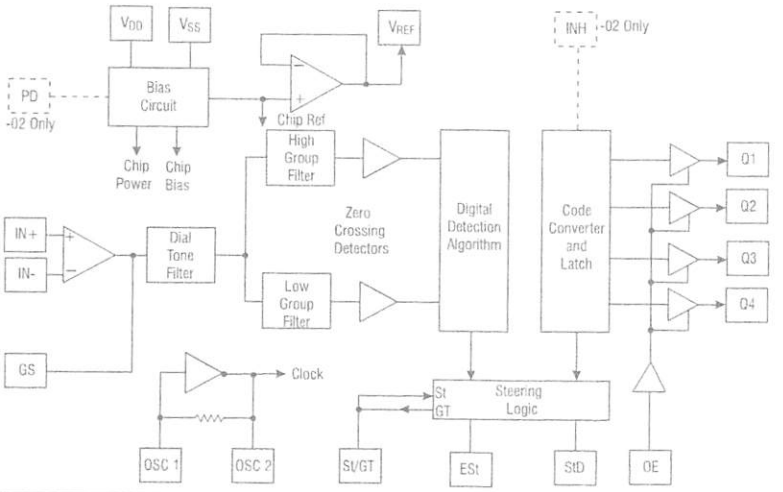
The M-8870 is a full DTMF Receiver that integrates both bandsplit filter and decoder functions into a single 18-pin DIP or SOIC package. Manufactured using CMOS process technology, the M-8870 offers low power consumption (35 mW max) and precise data handling. Its filter section uses switched capacitor technology for both the high and low group filters and for dial tone rejection. Its decoder uses digital counting techniques to detect and decode all 16 DTMF tone pairs into a 4-bit code. External component count is minimized by provision of an on-chip differential input amplifier, clock generator, and latched tri-state interface bus. Minimal external components required include a low-cost 3.579545 MHz color burst crystal, a timing resistor, and a timing capacitor.

The M-8870-02 provides a "power-down" option which, when enabled, drops consumption to less than 0.5 mW. The M-8870-02 can also inhibit the decoding of fourth column digits (see Tone Decoding table on page 5).

Ordering Information

Part #	Description
M-8870-01	18-pin plastic DIP
M-8870-01SM	18-pin plastic SOIC
M-8870-01SMTR	18-pin plastic SOIC, tape and reel
M-8870-02	18-pin plastic DIP, power-down, option
M-8870-02SM	18-pin plastic SOIC, power-down, option
M-8870-02T	18-pin plastic SOIC, power-down option, tape and reel

k Diagram



olute Maximum Ratings

ameter	Symbol	Value
er supply voltage (V_{DD} - V_{SS})	V_{DD}	6.0 V max
ge on any pin	V_{DC}	V_{SS} -0.3, VDD +0.3
ent on any pin	I_{DD}	10 mA max
ating temperature	T_A	-40°C to + 85°C
ge temperature	T_S	-65°C to + 150°C

fing these ratings may cause permanent damage. Functional operation under onditions is not implied.

Absolute Maximum Ratings are stress ratings. Stresses in excess of these ratings can cause permanent damage to the device. Functional operation of the device at these or any other conditions beyond those indicated in the operational sections of this data sheet is not implied. Exposure of the device to the absolute maximum ratings for an extended period may degrade the device and effect its reliability.

Characteristics

ameter	Symbol	Min	Typ	Max	Units	Test Conditions
ating supply voltage	V_{DD}	4.75	-	5.25	V	-
ating supply current	I_{DD}	-	3.0	7.0	mA	-
dby supply current (see Note 3)	$I_{DD}Q$	-	-	100	µA	PD=V_{DD}
er consumption	P_D	-	15	35	mW	f = 3.579 MHz, V_{DD} = 5.0 V
level input voltage	V_{IL}	-	-	1.5	V	-
level input voltage	V_{IH}	3.5	-	-	V	-
leakage current	I_{IH}/I_{IL}	-	0.1	-	µA	V_{IN} = V_{SS} or V_{DD} (see Note 2)
p (source) current on OE	I_{SO}	-	6.5	15.0	µA	OE = 0 V
impedance, signal inputs 1, 2	R_{IN}	8	10	-	mΩ	@ 1 kHz
ing threshold voltage	V_{TSt}	2.2	-	2.5	V	-
level output voltage	V_{OL}	-	-	0.03	V	No load
level output voltage	V_{OH}	V_{DD} - 0.03	-	-	V	No load
ut low (sink) current	I_{OL}	1.0	2.5	-	mA	V_{OUT} = 0.4 V
ut high (source) current	I_{OH}	0.4	0.8	-	mA	V_{OUT} = V_{DD} - 0.4 V
ut voltage V_{REF}	V_{REF}	2.4	-	2.7	V	No load
ut resistance V_{REF}	R_{OR}	-	10	-	kΩ	-

cal figures are at 25°C and are for design aid only; not guaranteed and not subject to production testing.

rating Characteristics - Gain Setting Amplifier

ameter	Symbol	Min	Typ	Max	Units	Test Conditions
leakage current	I_N	-	± 100	-	nA	V_{SS} < V_{IN} < V_{DD}
resistance	R_{IN}	4	-	-	MΩ	-
offset voltage	V_{OS}	-	± 25	-	mV	-
r supply rejection	PSRR	50	-	-	dB	1 KHz
non mode rejection	CMRR	55	-	-	dB	-3.0V < V_{IN} < 3.0V
en loop voltage gain	A_{VOL}	60	-	-	dB	-
loop unity gain bandwidth	f_C	1.2	1.5	-	MHz	-
ut voltage swing	V_O	3.5	-	-	V_{P-P}	RL ≈ 100 KΩ to V_{SS}
ible capacitive load (GS)	C_L	-	-	100	pF	-
ible resistive load (GS)	R_L	-	-	50	kΩ	-
non mode range	V_{CM}	2.5	-	-	V_{P-P}	No load

al figures are at 25°C and are for design aid only; not guaranteed and not subject to production testing.
:
voltages referenced to V_{SS} unless otherwise noted. For typical values, V_{DD} = 5.0V, V_{SS} = 0V, TA = 25°C.

ıctional Description

870 operating functions (see block diagram on e 1) include a bandsplit filter that separates the ı and low tones of the received pair, and a digital oder that verifies both the frequency and duration ıe received tones before passing the resulting 4-bit e to the output bus.

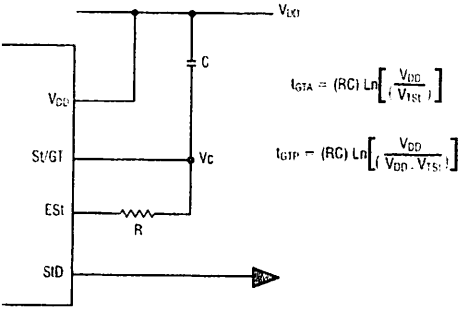
ɛr

low and high group tones are separated by apply- the dual-tone signal to the inputs of two 6th order ched capacitor bandpass filters with bandwidths correspond to the bands enclosing the low and group tones. The filter also incorporates notches 50 and 440 Hz, providing excellent dial tone rejec- Each filter output is followed by a single-order ched capacitor section that smooths the signals to limiting. Signal limiting is performed by high- comparators provided with hysteresis to prevent ction of unwanted low-level signals and noise. comparator outputs provide full-rail logic swings e frequencies of the incoming tones.

oder

M-8870 decoder uses a digital counting tech- e to determine the frequencies of the limited tones to verify that they correspond to standard DTMF ıencies. A complex averaging algorithm is used to ɛct against tone simulation by extraneous signals ɲ as voice) while tolerating small frequency varia- . The algorithm ensures an optimum combination ımunity to talkoff and tolerance to interfering sig- (third tones) and noise. When the detector rec- ɛes the simultaneous presence of two valid tones wn as signal condition), it raises the Early ring flag (ESt). Any subsequent loss of signal ition will cause ESt to fall.

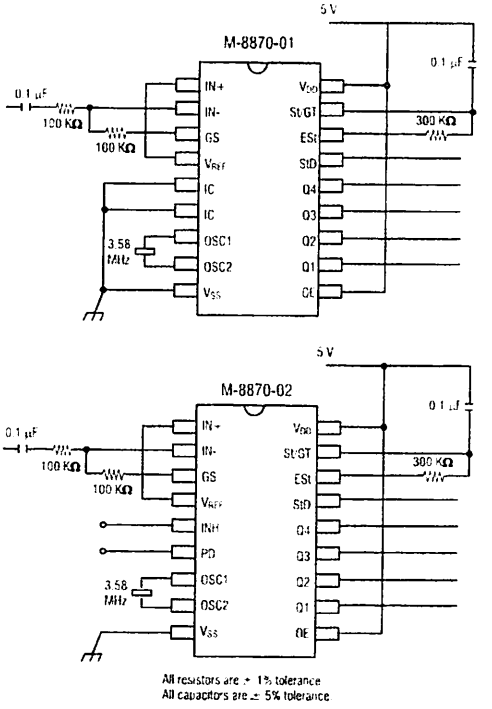
c Steering Circuit



Steering Circuit

Before a decoded tone pair is registered, the receiver checks for a valid signal duration (referred to as character-recognition-condition). This check is performed by an external RC time constant driven by ESt. A logic high on ESt causes VC (see block diagram on page 1) to rise as the capacitor discharges. Provided that signal condition is maintained (ESt remains high) for the validation period (t_{GTF}), V_C reaches the threshold (V_{TSt}) of the steering logic to register the tone pair, thus latching its corresponding 4-bit code (see DC Characteristics on page 2) into the output latch. At this point, the GT output is activated and drives V_C to V_{DD}. GT continues to drive high as long as ESt remains high. Finally, after a short delay to allow the output latch to settle, the delayed steering output flag (StD) goes high, signaling that a received tone pair has been registered. The contents of the output latch are made available on the 4-bit output bus by raising the three-state control input (OE) to a logic high. The steering circuit works in reverse to validate the interdigit pause between signals. Thus, as well as rejecting signals too short to be considered valid, the receiver will tolerate signal interruptions (dropouts) too short to be considered a valid pause. This capability, together with the ability to select the steering time constants externally, allows the designer to tailor performance to meet a wide variety of system requirements.

Single-Ended Input Configuration



Functions

	Name	Description	
	IN+	Non-inverting input	Connections to the front-end differential amplifier.
	IN-	Inverting input	
	GS	Gain select. Gives access to output of front-end amplifier for connection of feedback resistor.	
	V_{REF}	Reference voltage output (nominally VDD/2). May be used to bias the inputs at mid-rail.	
	INH*	Inhibits detection of tones representing keys A, B, C, and D.	
	PD*	Power down. Logic high powers down the device and inhibits the oscillator. Internal pulldown.	
	OSC1	Clock input	3.579545 MHz crystal connected between these pins completes the internal oscillator.
	OSC2	Clock output	
	VSS	Negative power supply (normally connected to 0 V).	
	OE	Tri-statable output enable (input). Logic high enables the outputs Q1 - Q4. Internal pullup.	
14	Q1, Q2, Q3, Q4	Tri-statable data outputs. When enabled by OE, provides the code corresponding to the last valid tone pair received (see Tone Decoding table on page 5).	
	StD	Delayed steering output. Presents a logic high when a received tone pair has been registered and the output latch is updated. Returns to logic low when the voltage on St/GT falls below VTSt.	
	ESt	Early steering output. Presents a logic high immediately when the digital algorithm detects a recognizable tone pair (signal condition). Any momentary loss of signal condition will cause ESt to return to a logic low.	
	St/GT	Steering input/guard time output (bidirectional). A voltage greater than VTSt detected at St causes the device to register the detected tone pair and update the output latch. A voltage less than VTSt frees the device to accept a new tone pair. The GT output acts to reset the external steering time constant, and its state is a function of ESt and the voltage on St. (See Common Crystal Connection on page 5).	
	V_{DD}	Positive power supply. (Normally connected to +5V.)	

nly. Connect to V_{SS} for -01 version

ard Time Adjustment

ere independent selection of signal duration and rdigit pause are not required, the simple steering uit of Basic Steering Circuit is applicable. nponent values are chosen according to the formu-

$$t_{REC} = t_{DP} + t_{GTP}$$
$$t_{GTP} @ 0.67\ RC$$

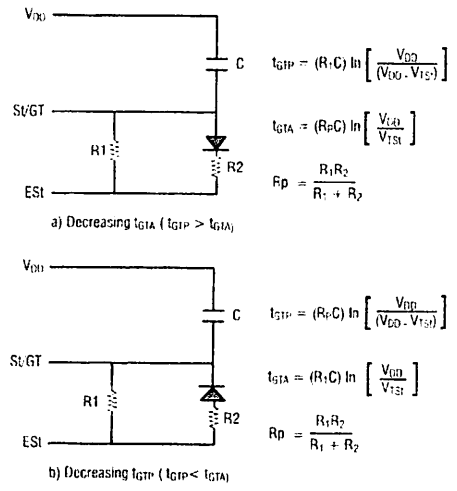
value of tDP is a parameter of the device and C is the minimum signal duration to be recognized he receiver. A value for C of 0.1 µF is recommend- or most applications, leaving R to be selected by designer. For example, a suitable value of R for a of 40 ms would be 300 kΩ. A typical circuit using steering configuration is shown in the Single - ed Input Configuration on page 4. The timing lirements for most telecommunication applications satisfied with this circuit. Different steering arrange- its may be used to select independently the guard s for tone-present (t_{GTP}) and tone-absent (t_{GTA}). may be necessary to meet system specifications place both accept and reject limits on both tone ation and interdigit pause.

ard time adjustment also allows the designer to tai- ystem parameters such as talkoff and noise immu- Increasing t_{REC} improves talkoff performance, e it reduces the probability that tones simulated by ech will maintain signal condition long enough to be registered. On the other hand, a relatively short t_{REC} with a long t_{DO} would be appropriate for extremely noisy environments where fast acquisition time and immunity to dropouts would be required. Design information for guard time adjustment is shown in the Guard Time Adjustment below.

Power-down and Inhibit Mode (-02 only)

A logic high applied to pin 6 (PD) will place the device into standby mode to minimize power consumption. It

Figure 5 Guard Time Adjustment



ɔs the oscillator and the functioning of the filters. the M-8870-01 models, this pin is tied to ground ic low).

ɔit mode is enabled by a logic high input to pin 5 ł). It inhibits the detection of 1633 Hz. The output ə will remain the same as the previous detected ə (see Pin functions table on page 4). On the M-)-01 models, this pin is tied to ground (logic low).

ıt Configuration

input arrangement of the M-8870 provides a dif-ntial input operational amplifier as well as a bias ce (V_{REF}) to bias the inputs at mid-rail. Provision ade for connection of a feedback resistor to the ımp output (GS) for gain adjustment.

In a single-ended configuration, the input pins are connected as shown in the Single - Ended Input Configuration on page 3 with the op-amp connected for unity gain and V_{REF} biasing the input at $1/2V_{DD}$. The Differential Input Configuration bellow permits gain adjustment with the feedback resistor R_5.

DTMF Clock Circuit

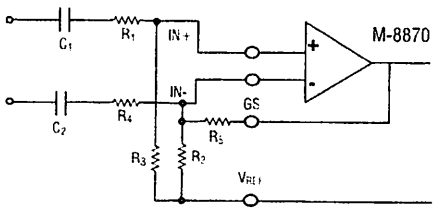
The internal clock circuit is completed with the addition of a standard 3.579545 MHz television color burst crystal. The crystal can be connected to a single M-8870 as shown in the Single - Ended Input Configuration on page 3, or to a series of M-8870s. As illustrated in the Common Crystal Connection below, a single crystal can be used to connect a series of M-8870s by coupling the oscillator output of each M-8870 through a 30 pF capacitor to the oscillator input of the next M-8870.

ə Decoding

W	FHIGH	Key (ref.)	OE	Q4	Q3	Q2	Q1
	1209	1	H	0	0	0	1
	1336	2	H	0	0	1	0
	1477	3	H	0	0	1	1
	1209	4	H	0	1	0	0
	1336	5	H	0	1	0	1
	1477	6	H	0	1	1	0
	1209	7	H	0	1	1	1
	1336	8	H	1	0	0	0
	1477	9	H	1	0	0	1
	1336	0	H	1	0	1	0
	1209	S	H	1	0	1	1
	1477	#	H	1	1	0	0
	1633	A	H	1	1	0	1
	1633	B	H	1	1	1	0
	1633	C	H	1	1	1	1
	1633	D	H	0	0	0	0
	ANY	ANY	L	Z	Z	Z	Z

ic low, H = logic high, Z = high impedance

rential Input Configuration



Differential Input Amplifier
$C_1 = C_2 = 10$ nF
$R_1 = R_4 = R_5 = 100$ KΩ
$R_2 = 60$ KΩ, $R_3 = 37.5$ KΩ

$R_3 = \frac{R_2 R_5}{R_2 + R_5}$

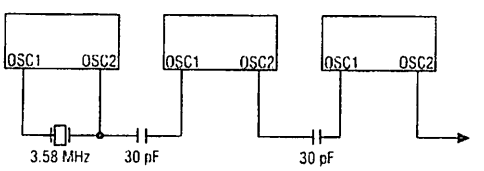
Voltage Gain (Av diff) = $\frac{R_5}{R_1}$

All resistors are ± 1% tolerance.
All capacitors are ± 5% tolerance.

Input Impedance

$(Z_{INDIFF}) = 2\sqrt{R_1^2 + \left(\frac{1}{\omega C}\right)^2}$

Common Crystal Connection



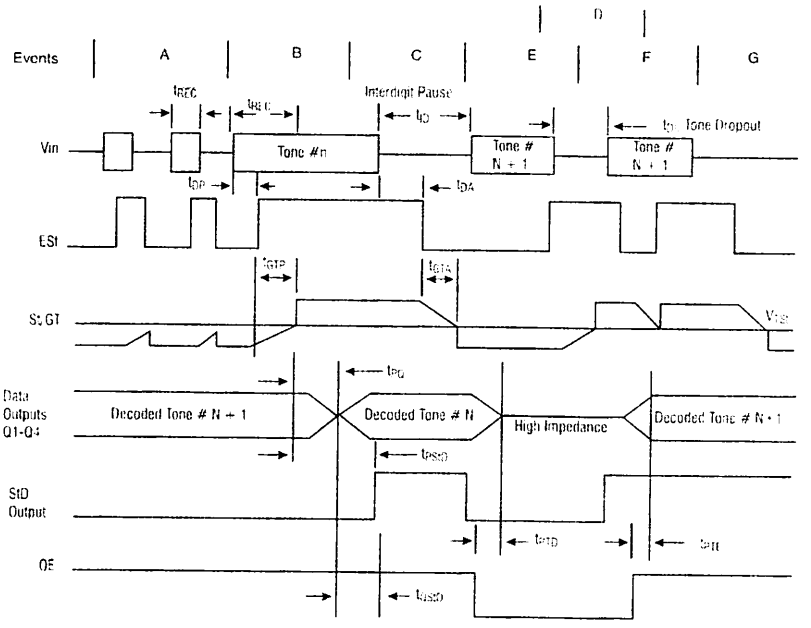
Characteristics

ameter	Symbol	Min	Typ*	Max	Units	Notes
l input signal levels (each tone	-	-29	-	+1	dBm	1,2,3,4,5,8
)mposite signal)	-	27.5	-	869	mVRMS	
tive twist accept	-	-	-	10	dB	2,3,4,8
ative twist accept	-	-	-	10	dB	
uency deviation accept limit	-	-	-	± 1.5% + 2 Hz	Nom.	2,3,5,8,10
uency deviation reject limit	-	±3.5%	-	-	Nom.	2,3,5
l tone tolerance	-	-25	-16	-	dB	2,3,4,5,8,9,13,14
e tolerance	-	-	-12	-	dB	2,3,4,5,6,8,9
tone tolerance	-	+18	+22	-	dB	2,3,4,5,7,8,9
present detection time	t_{DP}	5	8	14	ms	See Timing Diagram on page 7
absent detection time	t_{DA}	0.5	3	8.5	ms	
mum tone duration accept	t_{REC}	-	-	40	ms	User adjustable (see Basic Steering Circuit and Guard Time Adjustment on pages 3 and 4.)
mum tone duration reject	$t_{\overline{REC}}$	20	-	-	ms	
mum interdigit pause accept	t_{ID}	-	-	40	ms	
mum interdigit pause reject	t_{DO}	20	-	-	ms	
agation delay (St to Q)	t_{PQ}	-	6	11	µs	OE = VDD
agation delay (St to StD)	t_{PStD}	-	9	16	µs	
ut data setup (Q to StD)	t_{QStD}	-	4.0	-	µs	
agation delay (OE to Q), enable	t_{PTE}	-	50	60	ns	R_L = 10 kΩ, C_L = 50 pF
agation delay (OE to Q), disable	t_{PTD}	-	300	-	ns	
al clock frequency	f_{CLK}	3.5759	3.5795	3.5831	MHz	-
output (OSC2), capacitive load	C_{LO}	-	-	30	pF	-

ges referenced to V_{SS} unless otherwise noted. For typical values V_{DD} = 5.0 V, V_{SS} = 0 V, TA = 25°C, f_{CLK} = 3.579545 MHz.
l figures are at 25°C and are for design aid only; not guaranteed and not subject to production testing.

= decibels above or below a reference power of 1 mW into a 600Ω load.
sequence consists of all 16 DTMF tones.
duration = 40 ms. Tone pause = 40 ms.
nal DTMF frequencies are used, measured at GS.
tones in the composite signal have an equal amplitude.
width limited (0 to 3 kHz) Gaussian noise.
precise dial tone frequencies are (350 and 440 Hz) ± 2%.
n error rate of better than 1 in 10,000.
enced to lowest level frequency component in DTMF signal.
mum signal acceptance level is measured with specified maximum frequency deviation.
t pins defined as IN+, IN-, and OE.
rnal voltage source used to bias V_{REF}.
parameter also applies to a third tone injected onto the power supply.
renced to Single - Ended Input Configuration on page 3. Input DTMF tone level at -28 dBm.

ing Diagram



lanation of Events

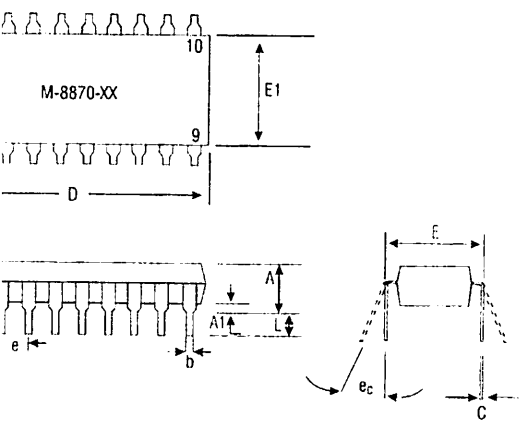
one bursts detected, tone duration invalid, outputs not updated.
one #n detected, tone duration valid, tone decoded and latched in outputs.
nd of tone #n detected, tone absent duration valid, outputs remain latched until next valid tone.
utputs switched to high impedance state.
one #n + 1 detected, tone duration valid, tone decoded and latched in outputs (currently high impedance).
cceptable dropout of tone #n + 1, tone absent duration invalid, outputs remain latched.
nd of tone #n + 1 detected, tone absent duration valid, outputs remain latched until next valid tone.

anation of Symbols

IN	DTMF composite input signal.
St	Early steering output. Indicates detection of valid tone frequencies.
t/GT	Steering input/guard time output. Drives external RC timing circuit.
1 - Q4	4-bit decoded tone output.
tD	Delayed steering output. Indicates that valid frequencies have been present/ absent for the required guardtime, thus constituting a valid signal.
E	Output enable (input). A low level shifts Q1 - Q4 to its high impedance state.
$\overline{EC}$	Maximum DTMF signal duration not detected as valid.
EC	Minimum DTMF signal duration required for valid recognition.
)	Minimum time between valid DTMF signals.
ɔ	Maximum allowable dropout during valid DTMF signal.
ɔ	Time to detect the presence of valid DTMF signals.
٨	Time to detect the absence of valid DTMF signals.
iTP	Guard time, tone present.
iTA	Guard time, tone absent.

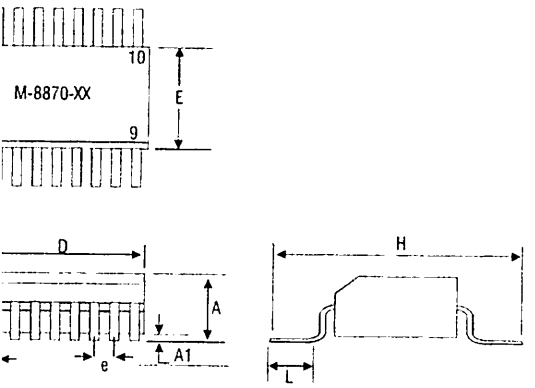
ıre 9 Mechanical Dimensions

n DIP



Tolerances for 18 - pin Dip				
	Inches		Metric (mm)	
	Min	Max	Min	Max
A	-	.210	-	5.33
A1	.015	-	.38	-
b	.014	.022	.36	.56
b2	.045	.070	1.1	1.7
C	.008	.014	.20	.36
D	.880	.920	23.35	23.37
E	.300	.325	7.62	8.26
E1	.240	.280	6.10	7.11
e	.100 BSC		2.54 BSC	
ec	0°	15°	0°	15°
L	.115	.150	2.92	3.81

'in SOIC



Tolerances for 18 - pin Dip				
	Inches		Metric (mm)	
	Min	Max	Min	Max
A	.0926	.1043	2.35	2.65
A1	.0040	.0118	.10	.30
b	.013	.020	.33	.51
D	.4469	.4625	11.35	11.75
E	.2914	.2992	7.4	7.6
e	.050 BSC		1.27 BSC	
H	.394	.419	10.00	10.65
L	.016	.050	.40	1.27

ing not to scale.
not reflect actual part marking.

Dimensions
mm
(inches)

LARE

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Fax: 886-2-2523-6369

http://www.clare.com

Specification: DS-M-8870-R3

7/25/01

LCM

Liquid Crystal Display Modules

Seiko Instruments GmbH

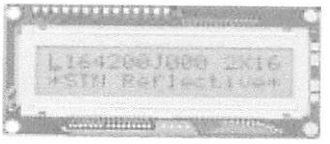
ot Matrix Liquid Crystal Display Modules

ARACTER TYPE

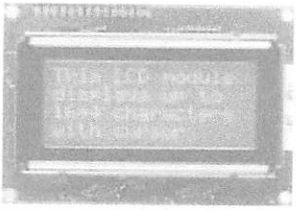
• FEATURES :

- Slim, light weight and low power consumption
- High contrast and wide viewing angle
- Built-in controller for easy interfacing
- LCD modules with built-in EL or LED backlight

M1641



L1642



L1614

M1632

L1652

L2012

• SPECIFICATIONS :

: Standard products : Products of optional specification

Format (character x line)		16 x 1	16 x 2	16 x 2	16 x 2	16 x 4	20 x 2
		M1641	M1632	L1642	L1652	L1614	L2012
		M16410AS	M16320AS	L164200J000S	L165200J200S	L161400J000S	L201200J000S
ht		M16419DWS	M16329DWS	L164221J000S	L165221J200S	L161421J000S	L201221J000S
ight		M16417DYS	M16327DYS	L1642B1J000S	L1652B1J200S	L1614B1J000S	L2012B1J000S
(wide temp)		M16410CS	M16320CS	L164200L000S	L165200L200S	L161400L000S	L201200L000S
ight (wide temp)		M16417JYS	M16327JYS	L1642B1L000S	L1652B1L200S	L1614B1L000S	L2012B1L000S
font		5x7 dots + cursor	5x7 dots + cursor	5x7 dots + cursor	5x7 dots + cursor	5x7 dots + cursor	5x7 dots + cursor
	Reflective	80,0 x 36,0 x 11,3	85,0 x 30,0 x 10,1	80,0 x 36,0 x 11,3	122,0 x 44,0 x 11,3	87,0 x 60,0 x 11,6	116,0 x 37,0 x 11,3
	EL backlight	80,0 x 36,0 x 11,3	85,0 x 30,0 x 10,1	80,0 x 36,0 x 11,3	122,0 x 44,0 x 11,3	87,0 x 60,0 x 11,6	116,0 x 37,0 x 11,3
m	LED backlight	80,0 x 36,0 x 15,8	80,0 x 30,0 x 15,8	80,0 x 36,0 x 15,8	122,0 x 44,0 x 15,8	87,0 x 60,0 x 15,8	116,0 x 37,0 x 15,8
rea (HxV) mm		64,5 x 13,8	62,0 x 16,0	64,5 x 13,8	99,0 x 24,0	61,8 x 25,2	83,0 x 18,6
size (HxV) mm *1		3,07 x 5,73	2,78 x 4,27	2,95 x 3,80	4,84 x 8,06	2,95 x 4,15	3,20 x 4,85
lxV) mm		0,55 x 0,75	0,50 x 0,55	0,50 x 0,55	0,92 x 1,10	0,55 x 0,55	0,60 x 0,65
pply voltage (VDD-VSS) V		+ 5 V	+ 5 V	+ 5 V	+ 5 V	+ 5 V	+ 5 V
nsumption	IDD	1,5	2,0	1,6	2,0	2,7	2,0
	ILC *4	0,2	0,2	0,3	0,4	1,1	0,4
ethod (duty)		1/16	1/16	1/16	1/16	1/16	1/16
l		KS0066 or equivalent	KS0066 MSM5839 or equivalent	KS0066 MSM5839 or equivalent	KS0066 MSM5839 or equivalent	KS0066 KS0063 or equivalent	KS0066 KS0063 or equivalent
emperature (°C)	normal temp.	0 to + 50	0 to + 50	0 to + 50	0 to + 50	0 to + 50	0 to + 50
	wide temp. *2	- 20 to + 70	- 20 to + 70	- 20 to + 70	- 20 to + 70	- 20 to + 70	- 20 to + 70
mperature (°C)	normal temp.	- 20 to + 60	- 20 to + 60	- 20 to + 60	- 20 to + 60	- 20 to + 60	- 20 to + 60
	wide temp.	- 30 to + 80	- 30 to + 80	- 30 to + 80	- 30 to + 80	- 30 to + 80	- 30 to + 80
Reflective		25	25	25	50	50	40
EL backlight		30	30	30	55	55	45
LED backlight		35	40	35	65	65	60
Model		5S	5S	5S	5C	5A	5A
Power supply (V)		+ 5.0	+ 5.0	+ 5.0	+ 5.0	+ 5.0	+ 5.0
current consumption (mA) *3		10	10	10	35	45	45
Forward current consumption (mA)		100	112	100	240	200	154
Forward input voltage (V,typ.)		+ 4,1	+ 4,1	+ 4,1	+ 4,1	+ 4,1	+ 4,1

H : Horizontal V : Vertical T : Thickness (max)

g cursor

ernal temperature compensation

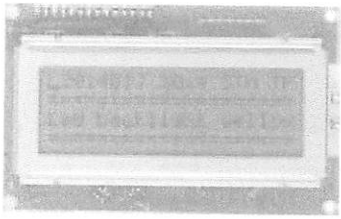
g EL backlight

n normal temperature range

licy is one of continues improvements we reserve the right to change the specifications for the products in the catalogue without notice.

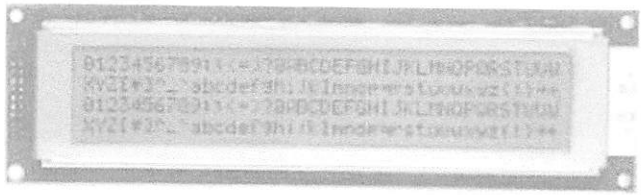
L2022

L2432



L2014

L4042



M4024

• SPECIFICATIONS :

: Standard products : Products of optional specification

haracter Format (character x line)		20 x 2	20 x 4	24 x 2	40 x 2	40 x 4
odel		L2022	L2014	L2432	L4042	M4024
eflective		-	L201400J000S	L243200J000S	L404200J000S	M40240AS
backlight		-	L201421J000S	L243221J000S	L404221J000S	M40249DWS
ED backlight		-	L2014B1J000S	L2432B1J000S	L4042B1J000S	M40247DYS
eflective (wide temp)		L202200P000S	L201400L000S	L243200L000S	L404200L000S	M40240CS
D backlight (wide temp)		L2022B1P000S	L2014B1L000S	L2432B1L000S	L4042B1L000S	M40247JYS
haracter font		5x7 dots + cursor	5x7 dots + cursor	5x7 dots + cursor	5x7 dots + cursor	5x7 dots + cursor
odule	Reflective	180.0 x 40.0 x 10.5	98.0 x 60.0 x 11.6	118.0 x 36.0 x 11.3	182.0 x 33.5 x 11.3	190.0 x 54.0 x 10.1
e	EL backlight	180.0 x 40.0 x 10.5	98.0 x 60.0 x 11.6	118.0 x 36.0 x 11.3	182.0 x 33.5 x 11.3	190.0 x 54.0 x 10.1
xVxT) mm	LED backlight	180.0 x 40.0 x 14.8	98.0 x 60.0 x 15.8	118.0 x 36.0 x 15.8	182.0 x 33.5 x 16.3	190.0 x 54.0 x 16.3
ewing area (HxV) mm		149.0 x 23.0	76.0 x 25.2	94.5 x 17.8	154.4 x 15.8	147.0 x 29.5
haracter size (HxV) mm *1		6.00 x 9.66	2.95 x 4.15	3.20 x 4.85	3.20 x 4.85	2.78 x 4.27
t size (HxV) mm		1.12 x 1.12	0.55 x 0.55	0.60 x 0.65	0.60 x 0.65	0.50 x 0.55
wer supply voltage (VDD-VSS) V		+ 5 V	+ 5 V	+ 5 V	+ 5 V	+ 5 V
rrent consumption	IDD	4.2	2.9	2.5	3.0	8.0
A,typ)	ILC *4	2.6	1.2	0.5	1.0	3.0
iving method (duty)		1/16	1/16	1/16	1/16	1/16
ilt-in LSI		KS0066 KS0063 or equivalent	KS0066 MSM5839 or equivalent	KS0066 KS0063 or equivalent	KS0066 KS0063 or equivalent	KS0066 MSM5839 or equivalent
erating temperature (°C)	normal temp.	-	0 to + 50	0 to + 50	0 to + 50	0 to + 50
	wide temp. *2	- 20 to + 70	- 20 to + 70	- 20 to + 70	- 20 to + 70	- 20 to + 70
orage temperature (°C)	normal temp.	-	- 20 to + 60	- 20 to + 60	- 20 to + 60	- 20 to + 60
	wide temp.	- 30 to + 70	- 30 to + 80	- 30 to + 80	- 30 to + 80	- 30 to + 80
ight	Reflective	80	55	40	70	90
typ.)	EL backlight	-	60	45	75	105
	LED backlight	110	70	60	95	140
erters	Model	-	5A	5A	5C	5D
EL	Power supply (V)	+ 5.0	+ 5.0	+ 5.0	+ 5.0	+ 5.0
	current consumption (mA) *3	-	45	45	25	80
D	Forward current consumption (mA)	320	240	150	260	480
cklight	Forward input voltage (V,typ.)	+ 4.1	+ 4.1	+ 4.1	+ 4.1	+ 4.1

: Excluding cursor
: With external temperature compensation
: Including EL backlight
: Based on normal temperature range

H : Horizontal V : Vertical T : Thickness (max)

ot Matrix Liquid Crystal Display Modules

RAPHIC TYPE

FEATURES :

- •Wide viewing angle and high contrast
- •Full dot configuration fits any application
- •Slim, light weight and low power consumption
- •Available in STN and FSTN

• SPECIFICATIONS :

(HxV,dot)			97 x 32	128 x 32	128 x 64	128 x 64
			Y97031	G1213	G1216	G1226
le)	Reflective	built-in RAM	-	-	-	-
	Reflective wide temp.	built-in RAM	-	G121300N000S	G121600N000S	-
	LED backlight	built-in RAM	-	-	-	G1226B1J000S
	LED backlight wide temp	built-in RAM	-	G1213B1N000S	G1216B1N000S	-
le)	Transmissive with CFL backlight	-	-	-	-	-
		built-in controller	-	-	-	-
	Transflective	built-in RAM	Y97031LF60W	-	-	-
e	Reflective (no backlight)		47,5 x 65,4 x 2,1	75,0 x 41,5 x 6,8	75,0 x 52,7 x 6,8	-
)	LED backlight		-	75,0 x 41,5 x 8,9	75,0 x 52,7 x 8,9	93,0 x 70,0 x 11,4
	CFL backlight		-	-	-	-
ea (HxV) mm			43,5 x 23,9	60,0 x 21,3	60,0 x 32,5	70,7 x 38,8
x V) mm			0,35 x 0,48	0,40 x 0,48	0,40 x 0,40	0,44 x 0,44
x V) mm			0,39 x 0,52	0,43 x 0,51	0,43 x 0,43	0,48 x 0,48
ply voltage (V)		(VDD - VSS)	+ 5,0	+ 5,0	+ 5,0	+ 5,0
		(VLC - VSS)	-	- 8,0	- 8,1	-8,2
sumption		IDD	0,10	2,0	2,0	3,0
		IDD (built-in controller)	-	-	-	-
		ILC	-	1,8	1,8	2,0
	Driving method (duty)		1/33	1/64	1/64	1/64
		Driver	SED1530 or equivalent	HD61202 HD61203 or equivalent	HD61202 HD61203 or equivalent	KS0107 KS0108 or equivalent
		Controller	-	-	-	-
emperature range (°C)			- 20 to + 70	- 20 to + 70	- 20 to + 70	0 to + 50
perature range (°C)			- 30 to + 80	- 30 to + 80	- 30 to + 80	- 20 to + 60
	Reflective (Transflective no backlight)		10	23	35	-
	LED backlight		-	35	45	72
	CFL backlight		-	-	-	-
ht	Forward current consumption (mA)		-	40	90	125
	Forward input voltage (V, typ.)		-	3,8	4,1	4,1
	Mode		-	-	-	-
CFL	Power supply voltage (V)		-	-	-	-
	Current consumption (mA, typ.)		-	-	-	-

DC/DC converter (single power source)

h external temperature compensation circuit

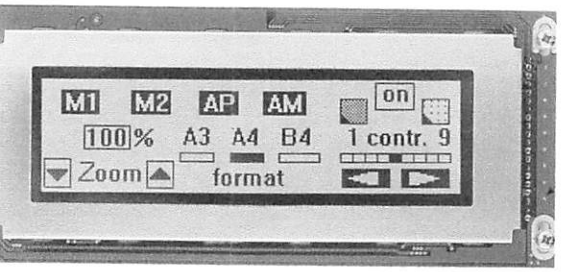
olicy is one of continues improvements we reserve the right to change the specifications of the products in the catalogue without notice.

rmat (HxV,dot)			240 x 64	240 x 128	320 x 200	320 x 240	640 x 200
l			G2446	G242C	G321D	G324E	G649D
lype	Reflective	built-in RAM	-	-	-	-	-
mode)	Reflective wide temp.	built-in RAM	-	-	-	-	-
	LED backlight	built-in RAM	-	-	-	-	-
	LED backlight wide temp	built-in RAM	-	-	-	-	-
l type	Transmissive	-	G2446X5R1A0S	G242CX5R1ACS	G321DX5R1A0S	G324EX5R1A0S	G649DX5R010S
mode)	with CFL backlight	built-in controller	G2446X5R1ACS	G242CX5R1A0S	G321DX5R1ACS	G324EX5R1ACS	-
	Transflective	built-in RAM	-	-	-	-	-
le size	Reflective (no backlight)			-	-	-	-
V x T)	LED backlight			-	-	-	-
	CFL backlight		191,0 x 79,0 x 15,1	180,0 x 110,0 x 15,1	166,0 x 134,0 x 15,1	166,0 x 134,0 x 15,1	260,0 x 122,0 x 15,7
ng area (HxV) mm			134,0 x 41,0	134,0 x 76,0	128,0 x 110,0	128,0 x 110,0	216,0 x 83,0
ze (H x V) mm			0,49 x 0,49	0,47 x 0,47	0,34 x 0,48	0,32 x 0,39	0,30 x 0,36
tch (H x V) mm			0,53 x 0,53	0,51 x 0,51	0,38 x 0,52	0,36 x 0,43	0,33 x 0,39
r supply voltage (V)		(VDD - VSS)	+5,0	+5,0	+5,0	+5,0	+5,0
		(VLC - VSS)	*1	*1	-24,0	-24,0	-24,0
nt consumption		IDD	12	30	8	7,5	11
		IDD (built-in controller)	15	40	23	23	-
yp.)		ILC	-	-	6	6,5	9
Driving method (duty)			1/64	1/128	1/200	1/240	1/200
n LSI		Driver	MSM5298 MSM5299 or equivalent	KS0103 KS0104 or equivalent	MSM5298 MSM5299 or equivalent	HD66204 HD66205 or equivalent	MSM5298 MSM5299 or equivalent
		Controller	SED1330FB	SED1330FB	SED1330FB	SED1330FB	-
ting temperature range (°C)			0 to +50	0 to +50	0 to +50	0 to +50	0 to +50
ge temperature range (°C)			- 20 to +60	- 20 to +60	- 20 to +60	- 20 to +60	- 20 to +60
t	Reflective (Transflective no backlight)		-	-	-	-	-
.)	LED backlight		-	-	-	-	-
	CFL backlight		200	280	350	350	420
acklight	Forward current consumption (mA)		-	-	-	-	-
	Forward input voltage (V, typ.)		-	-	-	-	-
	Mode		4800210	4800210	4800210	4800210	4800120
er for CFL	Power supply voltage (V)		+5,0	+5,0	+5,0	+5,0	+12,0
	Current consumption (mA, typ.)		250	350	365	365	390

uit-in DC/DC converter (single power source)

se with external temperature compensation

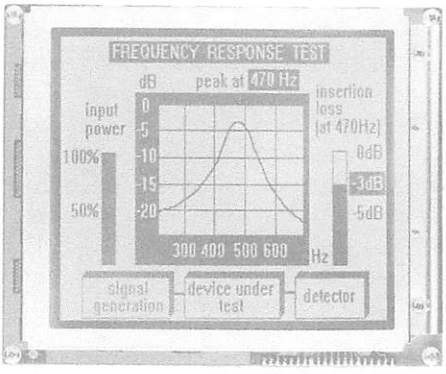
our policy is one of continous improvemets, we reserve the right to change the specifications of the products in the catalogue without notice.



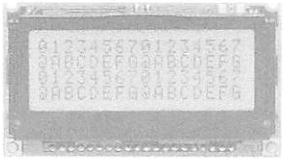
G2446

G1226

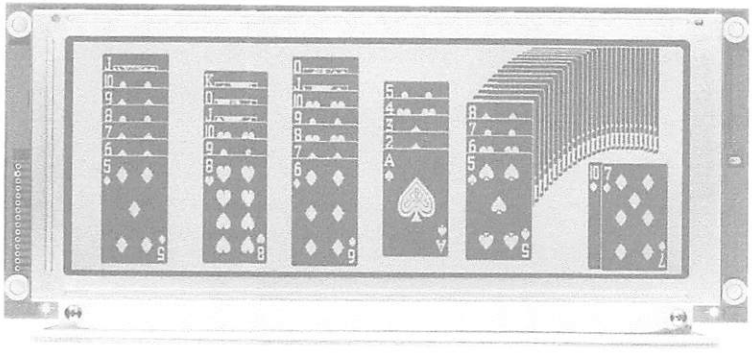
G1216



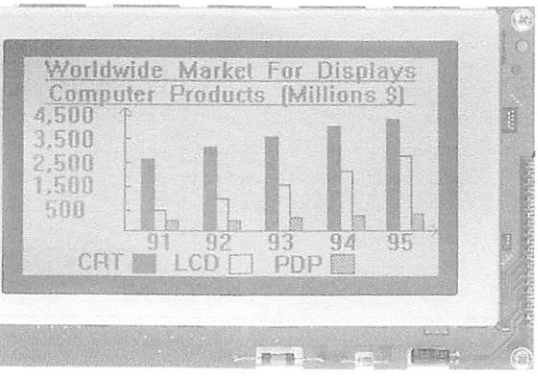
G321D



G1213



G649D



G242C

G324E

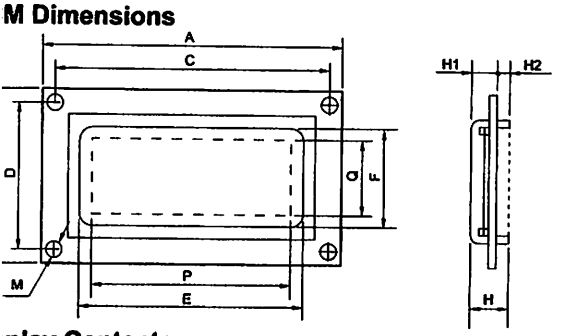
ECK LIST FOR CUSTOM DESIGNED LCD MODULE

mpany_____ **2. Application**_____ **3. Customer Specified Part No.**_____

sign

lew ☐Modified : Manufacturer_____, Part No._____, Remarks _____
:quivalent: Manufacturer_____, Part No._____, Remarks _____

M Dimensions



A x B : Module size _____ x _____ mm
E x F : Viewing area _____ x _____ mm
P x Q : Active display area _____ x _____ mm
C : Length between mounting holes _____ mm
D : Length between mounting holes _____ mm
M : Diameter of mounting hole _____ mm
H : Total thickness _____ mm
H1 : Upper thickness _____ mm
H2 : Lower thickness _____ mm

play Contents

haracter type:_____characters_____lines
haracter font_____x_____dots + cursor
haracter pitch_____x_____mm
ot pitch_____x_____mm
ot size_____x_____mm
raphics (Full dot) type:_____x_____dots
ot pitch_____x_____mm
ot size_____x_____mm
egment type:_____digits_____lines
thers_____

D Panel

ing angle: ☐6 o'clock ☐12 o'clock☐____o'clock
: ☐TN ☐FSTN (Black and white)
STN (☐Yellow green ☐Gray ☐Blue)
Chromaticity coordinates
(_____ ≦ x ≦ _____ , _____ ≦ y ≦ _____)
Positive type ☐Negative type
Reflective ☐Transflective ☐Transmissive
Others_____
scale: ☐Yes_____ gray scale ☐No
erential specifications:
Response time t_{on} ____ ms (____°C) t_{off} ____ ms (____°C)
Viewing angle____deg. (____°C) ☐Contrast____(____°C)
Others_____
surface finishing:
Normal ☐Anti-glare☐_____
rizer color: ☐Normal (neutral gray) ☐Red
Green ☐Blue ☐_____

ving Method

lexing:1/_____duty, 1/_____bias
e frequency: _____Hz

driver: ☐Specified ☐Unspecified
egment driver _____(Manufacturer _____)
ommon driver _____(Manufacturer _____)
roller: ☐Internal ☐External
pe No._____(Manufacturer _____)
: ☐Internal ☐External
pe No._____(Manufacturer _____)
: ☐Internal ☐External
e No. /Memory size_____(Kbit) (Manufacturer _____)

wer Supply

gle power supply: ☐5V ☐_____V
ower supplies
r logic: (V_{DD}-Vss) : ☐5V ☐_____V
r LC drive: (V_{LC}-Vss) : ☐_____V

11. Temperature Compensation Circuit

☐Internal ☐External ☐Unnecessary
Compensation range: ☐ 0°C to 50°C ☐ ___°C to ___°C

12. Current Consumption

For logic: typ._____mA, max._____mA
For LC drive: typ._____mA, max._____mA
Others ( ) : typ._____mA, max._____mA

13. Contrast Adjustment

☐Internal ☐External ☐Unnecessary
Method: ☐ Temp. compensation circuit ☐Volume ☐____

14. Temperature Range

Operating temperature range: ☐ 0°C to 50°C ☐____°C to____°C
Storage temperature range: ☐- 20°C to 60°C ☐____°C to____°C

15. Input/Output Terminals

Specifying allocation: ☐Yes ☐No
Specifying position: ☐Yes ☐No

16. Weight

typ._____g, max._____g

17. Connector

☐ Internal ☐ External ☐ Unnecessary
Type No._____(Manufacturer _____)

18. Backlight

☐Internal ☐External ☐Unnecessary
☐EL: ☐Green ☐White ☐_____
☐LED: ☐Yellow green ☐Amber ☐_____
☐CFL: ☐White ☐_____
☐Incandescent lamp ☐Others_____
☐Backlight type ☐Edge backlight type
Brightness:_____cd/m^2
Inverter: ☐Internal ☐External ☐Unnecessary
Power supply voltage_____V
Current consumption (backlight included)_____ mA
Brightness control: ☐Yes ☐No

19. Others

_____
_____
_____

20. Schedule

Estimate:_____
Sample: Delivery_____, Quantity:_____pcs
Mass production: Target price:_____
Delivery _____, Total quantity:_____pcs
Quantity per month_____pcs

uid Crystal Displays

CK LIST FOR CUSTOM DESIGNED LCD

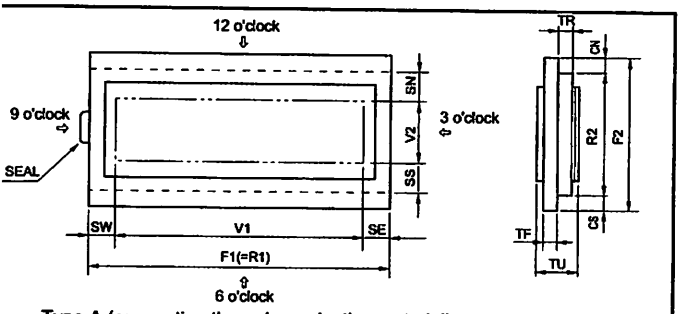
ıpany_____ **2. Application**_____ **3. Customer Specified Part No.**_____

ign

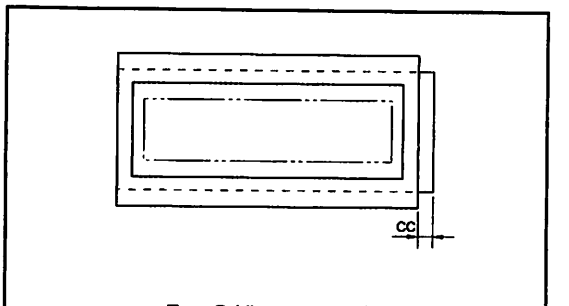
ew ☐Modified: Manufacturer _____ , Part No._____ , Remarks_____

uivalent: Manufacturer_____ , Part No._____ , Remarks_____

el Dimensions



- Type A (connection through conductive material) -



- Type B (direct common) -

izontal length of upper glass _____ mm

ical length of upper glass_____ mm

izontal length of lower glass_____ the same as F1

rtical length of lower glass_____ mm

generally longer than F2 when terminals are with pin.

**: Thickness of glass_____ mm

ıdard type: 1.1 mm or 0.7 mm

ckness of LCD_____ mm

il: ☐Right ☐Left ☐Right or Left

V1 :Horizontal length of viewing area _____ mm

V2 :Vertical length of viewing area _____ mm

CN**: Terminal length_____ mm

CS**:Terminal length_____ mm

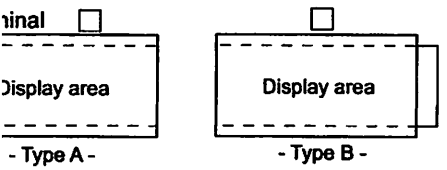
**CN or CS=0 in case of one side terminal type.

CC: Terminal length_____ mm

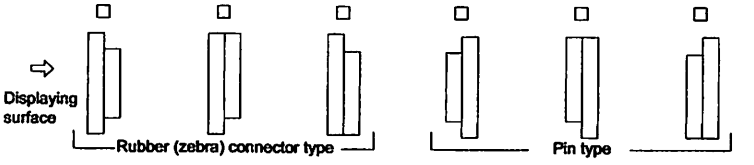
SE,SW,SN,SS : Seal width

(According to design or manufacturing condition:
about 2.0 mm to 4.0 mm)

el Form



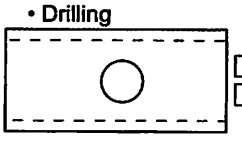
- Type A - - Type B -



nfering

☐ Yes
☐ No

• Drilling



☐ Yes
☐ No

lay Mode

ıg angle : ☐6 o'clock ☐ 12 o'clock ☐_____o'clock

☐TN ☐FSTN (Black and white)

;TN: (☐ Yellow green ☐ Gray ☐ Blue)

ıromaticity coordinates (____≦x≦ ____, ____≦y≦ ____)

'ositive type ☐Negative type

!eflective ☐Transflective ☐Transmissive

ential specifications:

!esponse time t_{on} ____ ms (____ °C) t_{off} ____ ms (____ °C)

iewing angle ____deg. (____ °C) ☐Contrast____ (____ °C)

)thers _____

rizer

:e finishing: ☐ Normal ☐ Anti-glare ☐_____

☐Normal (neutral gray) ☐Red ☐Green

☐Blue ☐_____

ɔolarizer : ☐ Attached type ☐ Separate type

ɔolarizer : ☐ Attached type ☐ Separate type

ng Method

c ☐ Multiplexing: (1/_____ duty, 1/_____ bias)

ting voltage (V_{opr}) :_____ V

frequency:_____ Hz

g IC:_____ (Manufacturer _____)

nt consumption:_____ μA

10. Temperature Range

Operating temperature range

☐With temperature compensation circuit (or volume)

(☐ 0°C to 50°C ☐_____°C to_____°C)

☐Without temperature compensation circuit

(☐ 0°C to 50°C ☐_____°C to_____°C)

Storage temperature range

(☐ - 20°C to 60°C ☐_____°C to_____°C)

11. Terminal Connecting Method

☐Rubber connector (Zebra rubber)

☐Pin: ☐DIL ☐SIL ☐_____

Pitch (☐2.54 ☐_____mm) Length (_____mm)

☐Heat seal: ☐Equipped ☐Unnecessary

12. Others

Print (Characters, lines, masks etc.) : ☐Yes ☐ No

Protective film:

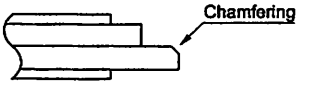
☐Yes (Color: ☐ Red ☐Translucent ☐Transparent) ☐No

Chamfering (for heat-seal connector) :

☐Yes (Position:_____)

(Quantity:_____)

☐No



13. Schedule

Estimate :_____

Sample : Delivery_____ , Quantity :_____ pcs

Mass production : Target price : _____

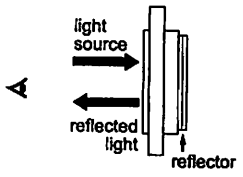
Delivery _____ , Total quantity:_____ pcs

Quantity per month:_____ pcs

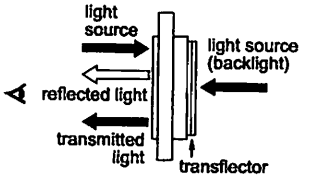
uid Crystal Display Modules

FLECTIVE/TRANSFLECTIVE/TRANSMISSIVE LCD

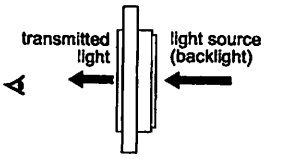
flective LCD
ctor bonded to the rear polarizer
ts the incoming ambient light. Low power
imption because no backlight is required.



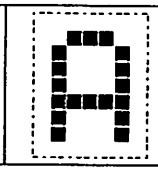
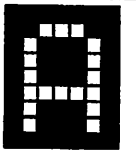
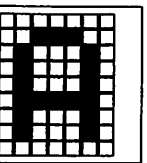
❷ Transflective LCD
Transflector bonded to the rear polarizer reflects light from the front as well as enabling lights to pass through the back. Used with backlight off in bright light and with it on in low light to reduce power consumption.



❸ Transmissive LCD
Without reflector or transflector bonded to the rear polarizer. Backlight required. Most common is transmissive negative image.



SITIVE/NEGATIVE MODE

'ositive type	
Negative type	
Negative type (inverse image) (when data is inverted)	

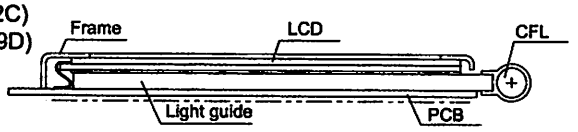
TYPE/STN TYPE/FSTN TYPE

(Background/dot color) Gray/Black	TN(Twisted Nematic) type is most conventional and economical. It is used for static drive LCD and low-duty drive LCD (watch,calculator, etc.)
Yellowgreen/Dark blue Gray/Dark blue White/Blue	STN (Super Twisted Nematic) type has a higher twist angle, and thus provides clear visibility and wider viewing angle. This is suitable especially for high-duty drive LCD.
White/Black	FSTN (Film Super Twisted Nematic) type utilizes RCF (Retardation Control Film) to remove the coloring of STN LCD. Thus FSTN type provides easy-to-read black-and-white display.

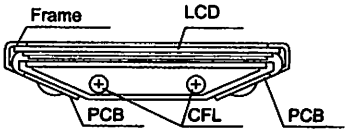
UCTURE AND FEATURE OF LCD MODULE WITH BACKLIGHT

(Cold Cathode Fluorescent Lamp) backlight
itures: high brightness, long service life, inverter required

ige backlight type
G2446,G242C)
G321D,G649D)

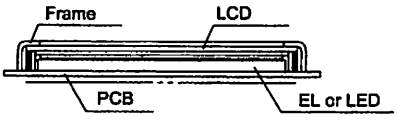


cklight type



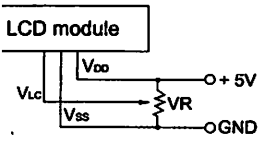
EL (Electroluminescent Lamp) backlight
LED (Light Emitting Diode) backlight

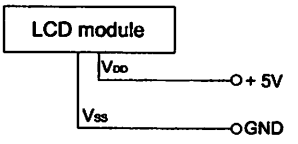
Features: EL: thin, inverter required
LED: long service life, low voltage driving, no inverter required

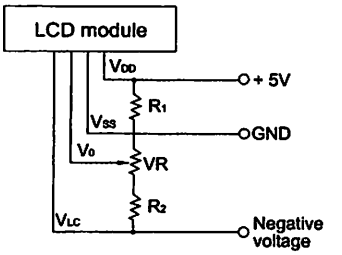


VER SUPPLY

acter modules (single power supply) • G2446,G242C (Built-in DC-DC conv.) • G321D, G324E and G649D

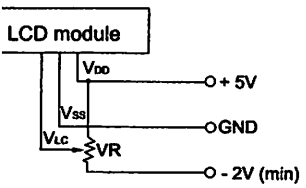


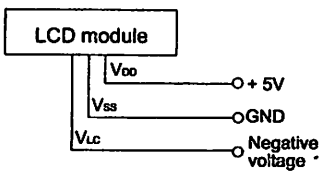




Note 1:Contrast can be adjusted by VR.
Note 2:For module with backlight, power supply for backlight is necessary.

iracter Modules(Dual power supply) • Y1206 and G1226





*Negative voltage should be variable for contrast adjustment.

ɔcautions

ty Instructions

ıe LCD panel is damaged, be careful not to get the ıid crystal in your mouth and not to be injured by shed glasses.

ɔu should swallow the liquid crystal, first, wash your uth thoroughly with water, then, drink a lot of water ł induce vomiting, and then, consult a physician.

ıe liquid crystal should get in your eye, flush your ɜ with running water for at least fifteen minutes.

ıe liquid crystal touches your skin or clothes, re- ve it and wash the affected part of your skin or thes with soap and running water.

or CFL backlight is driven by a high voltage with an ərter. Do not touch the connection part or the wir- pattern of the inverter.

not use inverters without a load or in the short-cir- : mode.

ɜ the LCD module within the rated voltage to pre- ıt overheating and/or damage. Also, take steps to ɜure that the connector does not come off.

lling Precautions

ce the LCD panel has glass substrate, avoid apply- mechanical shock or pressure on the module. Do drop, bend, twist or press the module.

not soil or damage LCD panel terminals.

ce the polarizer is made of easily-scratched mate- , be careful not to touch or place objects on the dis- y surface.

ɜp the display surface clean. Do not touch it with ır skin.

:OS LSI is used in the LCD module. Be careful of tic electricity.

not disassemble the module or remove the liquid stal panel or the panel frame.

not damage the film surface of the EL lamp; other- e the lamp will be damaged by humidity.

set an EL lamp in an LCD module, push the EL ıp with its emitting side up, without pushing the rub- connectors too hard. If you damage them, the LCD dule may not work properly.

ıting and Designing

protect the polarizer and the LCD panel, cover the ɔlay surface with a transparent plate (e.g., acrylic ılass) with a small gap between the transparent plate l the display surface.

ɜp the module dry. Avoid condensation to prevent transparent electrodes from being damaged.

ve LCD panel with AC waveform in which DC ele- nt is not included to prevent deterioration in the LCD ıel.

ıtrast of LCD varies depending on the ambient tem- ature. To offer the optimum contrast, LC drive volt- ɜ should be adjusted. LCD driven in a high duty o must be provided with drive voltage adjustment thod.

unt a LCD module with the specified mounting part/ ɜs.

- Design the equipment so that input signal is not applied to the LCD module while power supply voltage is not applied to it.
- Do not locate the CFL tube and the lamp lead wire close to a metal plate or a plated part inside the equipment. Otherwise stray capacity causes a drop in voltage, decreasing the brightness and the ability to start-up.

Cleaning

- Do not wipe the polarizer with a dry cloth, as it may scratch the surface.
- Wipe the LCD panel gently with a soft cloth soaked with a petroleum benzine.
- Do not use ketonic solvents (ketone and acetone)or aromatic solvents (toluene and xylene), as they may damage the polarizer.

Storing

- Store the LCD panel in a dark place, where the temperature is 25°C±10°C and the relative humidity below 65%. If possible, store the LCD panel in the packaging situation when it was delivered.
- Do not store the module near organic solvents or corrosive gases.
- Keep the module (including accessories) safe from vibration, shock and pressure.
- Use an LCD module with built-in EL backlight within six months of delivery.
- EL backlight is easily affected by environmental conditions such as temperature and humidity; the quality may deteriorate if stored for an extended period of time. Contact Seiko Instruments GmbH for details.
- Some parts of the backlight and the inverter generate heat. Take care so that the heat does not affect the liquid crystal or any other parts.
- Dust particles attached to the surface of the LCD or the surface of the backlight degrade the display quality. Be careful to keep dust out in designing the structure as well as in handling the module.
- Black or white air-bubbles may be produced if the LCD panel is stored for long time in the lower temperature or mechanical shocks are applied onto the LCD panel.

On This Brochure

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