SKRIPSI

PERANCANGAN DAN PEMBUATAN ALAT PENJAWAB SOAL *TEST TOEFL MULTI CLIENT* BERBASIS *PERSONAL KOMPUTER*

Disusun Oleh :

ABDUL GAFUR

NIM: 02.17.170

KONSENTRASI TEKNIK ELEKTRONIKA

JURUSAN TEKNIK ELEKTRO S-1

FAKULTAS TEKNOLOGI INDUSTRI

INSTITUT TEKNOLOGI NASIONAL MALANG

2009

LEMBAR PERSETUJUAN

PERANCANGAN DAN PEMBUATAN ALAT PENJAWAB SOAL *TEST TOEFL MULTI CLIENT* BERBASIS *PERSONAL KOMPUTER*

SKRIPSI

Disusun dan Diajukan Sebagai Salah Satu Syarat Untuk Memperoleh Gelar Sarjana Teknik Elektronika Strata Satu (S-1)

Disusun Oleh :

ABDUL GAFUR

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ABSTRAKSI

PERANCANGAN DAN PEMBUATAN ALAT PENJAWAB SOAL *TEST TOEFL MULTI CLIENT* BERBASIS *PERSONAL KOMPUTER*

Abdul Gafur : 0217170, Jurusan Teknik Elektronika S-1
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ABSTRAKSI

Dalam skripsi ini merancang alat yang diperuntukan untuk ujian *test toefl* dengan tujuan menggantikan fungsi kertas, pengerjaan alat didasarkan pada ujian toefl yang umumnya ujian *toefl* masih menggunakan alat tulis dalam menyelesaikan soal *toefl.*

Sistem kerja alat sebagai berikut; -Identitas peserta test yang dimasukan menggunakan *keypad matriks* yang ditampilkan ke LCD, selanjutnya data ID diproses menggunakan sistem *terprogram* mikrokontroller AT89S52 sebagai pengontrol utama sistem alat. Dengan serial data ke komputer sebagai *database* pada bagian instruktur ujian. Sedangkan sistem soal yang digunakan yakni pilihan ganda (A.B.C.D), peserta cukup menggunakan tombol penjawab untuk menjawab soal.

Hasil akhir adalah suatu solusi untuk mengatasi keterbatasan komputer dengan terminal RS-232 yang hanya mampu membentuk jaringan *one to one* , menjadi mampu untuk dikembangkan ke sistem jaringan *one to many* dengan menggunakan kabel RS-485 dengan tetap menggunakan terminal RS-232 tanpa harus mengganti terminal RS-232 menjadi terminal RS-*485.*

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Dipertahankan Dihadapan Team Penguji Skripsi Jenjang Strata Satu (S-1), pada:

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Puji syukur penulis panjatkan atas Berkat Rahmat Allah Yang Maha Kuasa, berupa nikmat kesehatan dan kesempatan. Shalawat beserta Salam kepada Nabi Besar Muhammad SAW sebagai pembawa kebenaran dan penerang di muka bumi ini, sehingga penulis dapat menyelesaikan laporan Skripsi dengan judul:

"Perancangan Dan Pembuatan Alat Penjawab Soal Test Toefl Multi Client Berbasis Personal Computer"

Pembuatan Skripsi ini disusun guna memenuhi syarat akhir kelulusan pendidikan jenjang Strata-1 di Institut Teknologi Nasional Malang. Laporan Skripsi ini merupakan tanggung jawab tertulis atas ilmu pengetahuan yang didapat selama penyusun mengikuti kuliah.

Atas terselesaikannya Skripsi ini, penulis mengucapkan terima kasih kepada :

1. Kedua Orang tua tercinta terima kasih atas Do'a, semua cinta, kasih sayang, yang telah banyak membantu dan selalu memberikan dorongan, semangat dan pengorbanan besar yang tulus sehingga penulis bisa mempersembahkan setitik keberhasilan ini. Semoga saya selalu menjadi anak yang shaleh dan berbakti
2. Bapak Dr.Ir.Abraham Lomi, MSEE selaku Rektor Institut Teknologi Nasional Malang.
3. Bapak Ir.H.Sidik Noertjahjono,MT selaku Dekan Fakultas Teknologi Industri Institut Teknologi Nasional Malang
4. Bapak Ir. Yudi Limpraptono, MT selaku Ketua Jurusan Teknik Elektro S1.
5. Bapak I.Komang Somawirata, ST, MT selaku Dosen Pembimbing I yang telah memberikan masukan, bimbingan, pengarahan, serta ilmu-ilmu yang sangat bermanfaat sehingga Skripsi ini dapat terselesaikan.
6. Bapak Ir.Yusuf Ismail Nakhoda, MT selaku Dosen Pembimbing II yang telah memberikan masukan selama bimbingan Skripsi, baik pengarahan, serta ilmu-ilmu yang sangat bermanfaat sehingga Skripsi ini dapat terselesaikan.
7. Bapak dan Ibu dosen Institut Teknologi Nasional Malang. atas ilmu yang telah diberika selama perkuliahan.

8. Buat Finaku tersayang, yang tanpa henti-hentinya selalu memberikan bantuan, semangat serta dukungan dan do'a sehingga penulis tetap optimis untuk tegak melangkah dalam menggapai cita-cita. *No body perfect, but you're the most perfect girl that i ever had. I love you.*
9. Teman-teman seperjuangan T.Elektronika 2002 yang telah membantu dalam penyelesaian Skripsi ini. Semangat Bro
10. Terima kasih untuk semua pihak yang telah mendukungku yang tak dapat kusebutkan satu persatu.

Penulis menyadari bahwa laporan ini masih banyak yang perlu disempurnakan. Oleh sebab itu kritik dan saran yang membangun sangat diharapkan.

Akhir kata, penulis mohan maaf kepada semua pihak bilamana selama penyusunan Skripsi ini penyusun membuat kesalahan secara tidak sengaja, dan semoga Skripsi ini dapat bermanfaat bagi kita semua. Terutama untuk jurusan Teknik Elektronika S-1

Malang, Maret 2009

Penulis

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BAB I

PENDAHULUAN

1.1 Latar Belakang

Teknologi informasi sebagai salah-satu hasil pengembangan dari teknologi elektronika komunikasi yang digunakan oleh kebanyakan masyarakat, salah-satu pengembangan kearah pendidikan yakni pengembangan sistem ujian *toefl* komputer, akan tetapi pengembangan dilakukan dengan penambahan perangkat elektronika yang akan mempermudah dalam mengerjakan *test toefl*. Yakni menggunakan perangkat elektronika tambahan yang bertujuan menggantikan fungsi alat tulis pada ujian *test toefl* komputer.

Bentuk pengerjaan soal dengan alat yang digunakan yakni sistem soal berbentuk pilihan ganda ABCD, alat tesebut mampu mempersingkat waktu, dan akan menjadi salah satu solusi yang lebih mengoptimalkan peran kerja dari instruktur sebagai pelaksana ujian *test toefl*.

Dalam pengerjaanya alat yang digunakan sebagai alat *test toefl* pilihan ganda ABCD, diimplementasi menggunakan 2 *client/peserta* test dengan satu buah PC pada bagian instruktur sebagai tampilan *database client. Personal Komputer (PC)* yang digunakan sebagaimana sebagai tampilan *database* peserta test yang meliputi:

a. Tampilan identitas peserta test
b. Tampilan soal dalam bentuk pilihan ganda ABCD dan
c. Tampilan nilai hasil test.

Untuk komunikasi data *client* pada saat test menggunakan komunikasi serial RS-485 dan RS-232. Peserta hanya cukup menggunakan tombol penjawab soal untuk pilihan jawaban soal (ABCD).

1.2. Rumusan Masalah

Mengacu pada permasalahan yang ada maka rumusan masalah sebagai berikut:

- Bagaimana membuat sistem kerja alat yang membantu peserta (*client*) dalam menjawab beberapa soal dalam bentuk *test toefl* yang diberikan oleh instruktur *toefl.*
- Bagaimana peserta (*client*) memperoleh kemudahan dalam menjawab soal pilihan ganda dengan memanfaatkan kerja mekanik alat dalam menjawab soal test *toefl* berupa pilihan ganda (A.B.C.D), yang menggantikan fungsi alat tulis lembar ujian soal pilihan ganda yang ditampilkan lewat LCD.

1.3. Tujuan

Tujuan tugas akhir ini adalah sebagai berikut:

- Untuk mengetahui sejauh mana kinerja sistem yang dibuat dalam peningkatan kedisiplinan dan mempermudah peserta (*client*) dalam menghadapi soal test
- Memberdayakan mutu pendidikan dan sumber daya manusia (SDM), dalam pengembangan ilmu pengetahuan
- Alatpun mampu menggantikan fungsi alat tulis untuk ujian test *toefl.*

1.4. Batasan Masalah

Guna tercapai apa yang menjadi tujuan pembahasan skripsi ini, maka perlu adanya batasan-batasan masalah dalam lingkup pembahasannya, meliputi :

1. Tidak membahas proses percakapan antara instruktur dengan peserta test.
2. Mikrokontroller yang digunakan adalah AT89S52.
3. Komunikasi serial/*converter* data antara mikro dengan komputer menggunakan RS232 dan RS485.
4. *Database* menggunakan Bahasa *Pemrograman Borland Delphi.*
5. Tidak membahas tentang catu daya.

1.5. Metodologi

Metodologi yang digunakan dalam skripsi ini adalah :

1. Studi Literatur

   Pengumpulan data-data mengenai karakteristik komponen yang dipakai. Data tersebut merupakan data sekunder yang dapat dijadikan sebagai acuan dalam perancangan alat.

2. Perancangan dan Pembuatan Alat

   Penyusunan skripsi ini dilakukan dengan perecanaan dan pembuatan perangkat keras (*hardware*) dan perangkat lunak (*software*) sesuai dengan kebutuhan alat.

3. Pengujian Alat

   Dilakukan untuk mengetahui apakah alat telah bekerja sesuai dengan perencanaan.

1.6. Sistematika Penulisan

Bab I Pendahuluan

Pada bab ini di bahas tentang latar belakang permasalahan, rumusan masalah, batasan masalah, tujuan, metodologi, dan sistematika penulisan.

Bab II Landasan Teori

Pada bab ini di bahas tentang teori-teori yang menunjang dalam perencanaan dan pembuatan alat.

Bab III Perencanaan dan Pembuatan Alat Pada bab ini dibahas tentang perencanaan dan pembuatan perangkat keras (hardware) dan perangkat lunak (software).

Bab IV Pengujian Alat dan Analisa

Pada bab ini dibahas tentang proses serta hasil dari pengujian alat.

Bab V Penutup

Pada bab ini akan disampaikan kesimpulan dari perencanaan dan pembuatan serta pengujian alat.

BAB II

LANDASAN TEORI

2.2. Pendahuluan

Pada bagian bab ini akan membahas teori dasar yang melandasi permasalahan dan penyelesaiannya yang diangkat dalam tugas akhir ini. Bab ini akan membahas teori yang menunjang perancangan dan pembuatan alat.

Diawali dengan pembahasan tentang landasan teori mikrokontroler AT89S52 yang diterapkan untuk unit kontrol dan pada bagian lain juga dibahas tentang komunikasi data serial 485, Keypad,LCD, *Personal komputer* meliputi: pembuatan database yang selanjutnya akan dijelaskan lebih rinci dalam pembahasan berikut.

Pokok pembahasan pada bab ini meliputi :

- Teori mikrokontroller AT 89S52
- Teori *LCD*
- Teori dari *Keypad matriks*
- Teori tentang tombol penjawab soal
- Interface RS 232 dan RS 485
- Pembahasan *Personal computer*
- Teori *Borland Delphi*

- Alamat memori program eksternal 64 *Kilobyte.*
- Alamat memori data eksternal 64 *Kilobyte.*
- Memori program internal sebesar 8 *Kilobyte.*
- 32 jalur I/O yang dapat dipakai semua
- 3 buah *Timer/Counter* 16 bit
- 8 sumber interupt
- *Full Duplex* UART (*serial port*)
- SPI *Serial Interface*
- *Dual Data Pointer*
- Frekuensi kerja 0 sampai 33 MHz
- Tegangan operasi 4,0 Volt sampai 5,5 Volt
- Waktu pemrograman yang cepat

2.2.1. Mikrokontroller AT 89S52

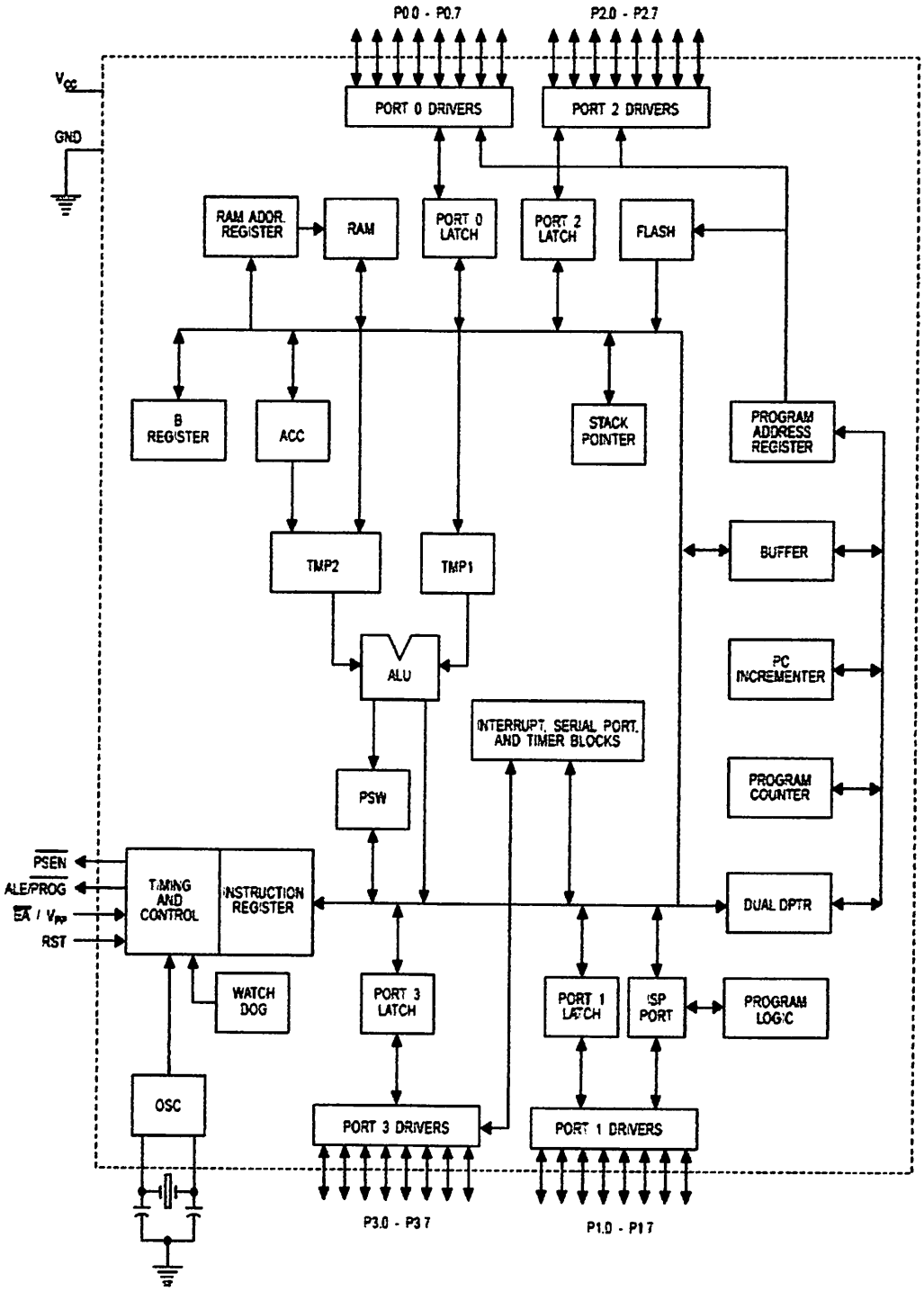
Mikrokontroller AT89S52 merupakan salah satu anggota keluarga dari MCS®51 yaitu suatu komponen produksi ATMEL yang berorientasi kontrol *(microcontroller).* Intel mengklarifikasikan dalam kelompok *embedded microcontroller* yang artinya mikrokontroller yang dapat diprogram ulang *(reprogrammable).* Didalam *chip* mikrokontroller AT89S52 sudah tersedia berbagai macam-macam peralatan pendukung *mikroprosessor* seperti RAM.

Serial Port, Bus data dan lainnya yang membuat pemakai *chip* ini dapat menekan penambahan komponen pendukung. Memori ini biasa digunakan untuk menyimpan instruksi (perintah) berstandar MCS-51 code sehingga memungkinkan *mikrokontroller* ini untuk bekerja dalam mode *single chip operation* (mode operasi keping tunggal) yang tidak memerlukan *external memory* (memori luar) unruk menyimpan *source code* tersebut.

Mikrokontroller AT89S52 merupakan mikrokontroller CMOS 8-*bit* dengan performa tinggi, *low power*, 8K*bytes Flash memory* didalamnya. dan kompatibel dengan MCS-51 mikrokomputer yang merupakan produksi dari ATMEL. Secara rinci arsitektur dari AT89S52 adalah sebagai berikut :

- Kompatibel dengan mikrokontroler MCS-51
- CPU *(Central Processing Unit)* dengan lebar data 8 *bit*
- 8 K byte *Downloadable Flash Memory*
- Pemrograman ISP yang fleksibel (*Mode Byte* dan *Page*)
- 3 *level program memory lock internal*
- Memori data internal 256 x 8 bit RAM *internal*

Adapun blok diagram dari Mikrokontroller adalah sebagai berikut:

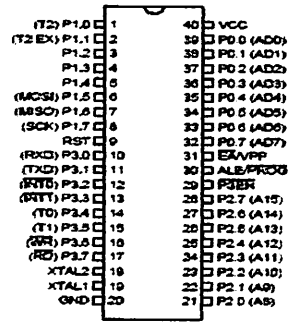


Gambar 2-1 Diagram Blok Mikrokontroller AT 89S52[1]

Sumber: Atmel AT 89S52 *Data Sheet*

2.2.3. Konfigurasi kaki-kaki MC AT89S52

Berikut ini adalah fisik dan konfigurasi dari kaki – kaki pada MC AT89S52. diperlihatkan pada gambar berikut:



Gambar 2-2 Konfigurasi PIN Mikrokontroller AT 89S52[2]

Sumber: *Atmel AT 89S52 Corporation.1998: 2*

Fungsi dari tiap-tiap pin Mikrokontroller AT89S52 adalah sebagai berikut:

GND :

Dihubungkan dengan *ground* rangkaian.

VCC :

Digunakan sebagai masukan catu daya +5 volt, dengan toleransi kurang lebih 10%. Keluarga MCS®51 yang diproduksi Intel dengan konfigurasi yang berbeda-beda sesuai dengan jenisnya.

Port 1 (P1.0-P1.7) :

Merupakan port paralel 8-bit dua arah dan memiliki alamat 90H yang bersifat *bidirectional* sehingga berfungsi sebagai *input* maupun *output* dapat bekerja baik untuk operasi *bit* maupun *byte.* Penyangga keluaran port 1 mampu menyerap arus empat masukan TTL (sekitar 1,6 mA), tergantung dari pengaturan *software.*

Tabel 2.1

Fungsi khusus pada port 1 AT89S8252[1]

PORT PIN	FUNGSI KHUSUS
P1.0	T2 (Masukan luar untuk *Timer/Counter* 2)
P1.1	T2 EX (*Timer/Counter* 2 *capture/reload trigger* dan control arah)
P1.5	MOSI (*Master data output, Slave data input* untuk kanal SPI)
P1.6	MISO (*Master data input, Slave data Output* untuk kanal SPI)
P1.7	SCK (*Master clock output, Slave clock input* untuk kanal SPI)

Pin 20 sampai 27 (P2.0-P2.7):

Merupakan port paralel 8-bit saluran I/O dua arah setiap salurannya mampu melayani 4 masukan dan memiliki alamat A0H. Port 2 juga dapat digunakan sebagai alamat *bus* baik *byte* tinggi, mengeluarkan alamat bagian tinggi (A8-A15) selama adanya akses kememori program luar. pengambilan data memori eksternal yang menggunakan mode pengalamatan 16-*bit*.

Pin 10 sampai 17:

Yakni *Port* 3 (P3.0-P3.7) mempunyai fungsi sebagai I/O 8 bit dua arah dengan fungsi pengganti. Bila fungsi pengganti tidak dipakai, maka dapat digunakan sebagai port paralel 8 bit serbaguna. Selain itu sebagian dari port 3 dapat berfungsi sebagai sinyal kontrol pada saat proses pemograman dan verifikasi. Keluaran port menyerap arus empat masukan TTL (sekitar 1,6 mA). Selain itu port 3 juga mempunyai fungsi khusus ditunjukan pada tabel berikut antara lain:

Tabel 2-2.

Fungsi khusus port 3 pada AT89S52[1]

Pin-pin pada port 3	**Fungsi pengganti**
P3.0	RXD (port input serial)
P3.1	TXD (port output serial)
P3.2	INT0 (interrupt eksternal 0)
P3.3	INT1 (interrupt eksternal 1)
P3.4	T0 (input eksternal timer 0)
P3.5	T1 (input eksternal timer 1)
P3.6	WR (perintah write pada memori eksternal)
P3.7	RD (perintah read pada memori eksternal)

Sumber: Bereksperimen dengan Mikrokontroller 8031

Fungsi khusus port 3 berdasarkan keterangan fungsi tabel diatas sebagai berikut:

RD (P3.7) : Sinyal pembacaan memori data luar

WR (P3.6) : Sinyal penulisan memori data luar

T1 (P3.5) : Masukan dari pewaktu/ pencacah 1

T0 (P3.4) : Masukan dari pewaktu/ pencacah 0

INT1 (P3.3) : Masukan interupsi 1

INT0 (P3.2) : Masukan interupsi 2

TXD (P3.1) : Keluaran pengiriman data untuk *serial port* (*asynchronus*) atau keluaran clock (*synchronous*).

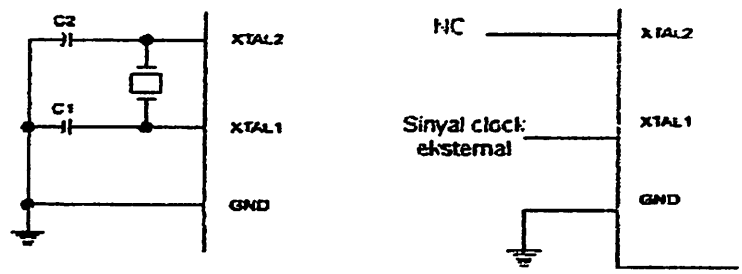
RXD (P3.0) : Masukan penerima *data serial* (*asynchrounus*), atau sebagai masukan / keluaran *data* (*synchronous*).

Pin 9 RST / VPD:

Merupakan masukan reset (aktif tinggi), pulsa transisi dari rendah ke tinggi selama dua siklus mesin maka ketika osilator bekerja akan m*ereset* peralatan.

Pin 18 dan 19:

Merupakan masukan ke penguat osilator berpenguat tinggi. Karenanya pin 18 dan 19 sangat diperlukan untuk dihubungkan dengan kristal. Selain itu XTAL 1 dapat juga sebagai input untuk *inverting oscilator amplifier* dan input ke rangkaian *internal clock* sedangkan XTAL 2 merupakan *output* dari *inverting oscilator amplifier.*



(a) (b)

Gambar 2-3

(a) *Oscilator External* pemasangan rangkaian *Internal Clock*

(b) *Eksternal Clock* Mikrokontroller AT 89S52[2]

Sumber: *Atmel AT 89S52 Data Sheet*

Pin 29:

Pin 29 digunakan untuk *Program Store Enable* (PSEN) yang memiliki fungsi kerja sebagai sinyal pengontrol untuk mengakses program memori eksternal masuk kedalam bus alamat selama proses pemberian/pengambilan instruksi (*fetching*).

Pin 30 ALE (*Address Latch Enable*) **Prog** (*Pulse Program*):

Pin ALE jika pada kondisi aktif *high* akan mengeluarkan pulsa *output* untuk mengunci satu *byte* alamat rendah selama mengakses ke memori *eksternal*. ALE dapat mengendalikan 8 beban TTL. Pin ini juga merupakan input pulsa *program* yang aktif rendah selama pemrograman EPPROM.

Pin 31 EA/VPP (*External Acces/ Programming Supply Voltage*):

Pin bagian ini dihubungkan dengan V_{SS} untuk memungkinkan pengambilan instruksi pada memori *program eksternal* yang berlokasi pada alamat (0000_H sampai $FFFF_H$). Apabila diset rendah (L) maka mikrokontroller akan melaksanakan seluruh instruksi dari memori *program eksternal*, sedangkan apabila diset tinggi (H) maka mikrokontroller akan melaksanakan instruksi dari memori *program internal*.

Pin 32 sampai 39 (*Port* 0):

Port 0 terdiri dari 8 saluran data masukan atau keluaran dua arah dan memiliki alamat 80H. Setiap saluran mampu melayani 8 masukan. *Port* 0 merupakan saluran alamat bagian rendah (A0-A7), yang digunakan pada saat mengakses memori data eksternal dan memori program eksternal.

Pin 40 (V_{CC}):

Power Supply merupakan masukan catu daya +5 volt, dengan toleransi kurang lebih 10%. Keluarga MCS®51 yang diproduksi Intel mempunyai konfigurasi yang berbeda-beda sesuai dengan jenisnya. Masing-masing jenis saling kompatibel serta mempunyai kelebihan tersendiri. Tabel 2-1 memperlihatkan spesifikasi dari MCS®51.

Tabel 2-3

Spesifikasi Keluarga MCS®51[2]

Tipe	Tipe tanpa EPROM	Tipe ber-EPROM	Kapasitas ROM	Kapasitas RAM	Port I/O	Pewaktu
8051	8031	-	4K	128	4	2
8051AH	8031AH	8751H	4K	128	4	2
8052AH	8032AH	8752BH	8K	256	4	3
80C51BH	80C31BH	87C51	4K	128	4	2
80C52	80C32	-	8K	256	4	3
83C51FA	80C51BH	8751FA	8K	256	4	3
83C51FB	80C51FB	87C51FB	16K	256	4	3
83C152	80C152	-	8K	256	5	3
89S52	-	89S52	8K	256	4	3

Sumber : *Bereksperimen* dengan *Mikrokontroller 8031.*

2.2.4. Organisasi Memori

Organisasi memori mikrokontroller AT89S52 dapat dibagi menjadi dua bagian besar yaitu: memori program dan memori data. Pembagian tersebut didasarkan atas fungsi dari penyimpanan data maupun program.

- Memori program digunakan untuk menyimpan instruksi-instruksi yang akan dijalankan oleh mikrokontroller.
- memori data digunakan sebagai tempat penyimpanan data yang sedang diolah oleh mikrokontroller.

2.2.5. Memori Program

Memori program pada AT89S52 berupa ROM menggunakan alamat 16 bit, untuk dapat menggunakan memori *program eksternal* ini penyemat / $\overline{EA}$ dihubungkan dengan penyemat Vss (logika 0). Pengambilan program dimulai alamat 0000_H-$FFFF_H$, dengan kapasitas penyimpanan program maksimal adalah 2^{16} (256*byte*) mampu mengakses memori data eksternal 64 K*byte* yang dilengkapi dengan ROM internal, namun untuk program yang besar digunakan dengan ROM eksternal yang terpisah dari mikrokontroller. Sinyal yang digunakan untuk membaca memori program eksternal adalah sinyal *PSEN (Program Store Enable).* sebesar 64 K*byte.*

2.2.6. Memori Data

Memori data pada AT89S52 terdiri 256 *bytes* dari RAM *internal.* Ruang alamat parallel diatas 128 bytes menduduki fungsi register *special* (SFR). Ini berarti bahwa yang berada diatas 128 *bytes* mempunyai alamat yang sama seperti ruang SFR tetapi secara fisik terpisah dari ruang SFR. Semua memori data internal dapat dialamati dengan pengalamatan langsung atau tidak langsung.

Ciri dari pengalamatan langsung adalah *operand* berisi alamat data yang diolah. Sedangkan ciri dari pengalamatan tidak langsung adalah *operand* alamat *register* yang berisi alamat data yang akan diolah. Untuk membaca data digunakan sinyal / RD, sedangkan untuk menulis data digunakan sinyal / WR. Ketika sebuah instruksi mengakses lokasi *internal* diatas alamat 7FH, mode pengalamatan menggunakan spesifikasi instruksi apakah CPU mengakses RAM

yang berada diatas 128 *bytes* atau ruang SFR. Instruksi yang menggunakan pengalamatan langsung mengakses ruang SFR.

2.2.7. *Register* Fungsi Khusus

Register fungsi khusus *(Special Function Register)* terletak pada 128 *byte* bagian atas memori data internal dan berisi register-register untuk pelayanan *latch port, timer, program* status *words, control peripheral* dan sebagainya.

Register-register ini hanya dapat diakses dengan pengalamatan langsung. Enam belas alamat pada *register* fungsi khusus dapat dialamati per*bit* maupun per-*byte* dan terletak pada alamat 80_H-FF_H. Secara perangkat keras, *register* fungsi khusus ini dibedakan dengan memori data internal. Alamat *register* fungsi khusus ditunjukkan pada tabel dibawah sebagai berikut:

Tabel 2-4

Alamat *Register* pada *Register* Fungsi Khusus mikrokontroller AT 89S52[1]

Simbol	Nama *Register*	Nilai pada saat *reset*	Alamat
Acc	*Accumulator*	00_H	$0E0_H$
B	*Register* B	00_H	$0F0_H$
PSW	*Program Status Word*	00_H	$0D0_H$
SP	*Stack Pointer*	07_H	81_H
DPTR	Data *Pointer* 2 *bytes*	0000_H	82_H
DPL	*Low bytes*	0000_H	83_H
DPH	*High bytes*	FF_H	80_H
P0	*Port* 0	FF_H	90_H
P1	*Port* 1	FF_H	$0A0_H$
P2	*Port* 2	FF_H	$0B0_H$
P3	*Port* 3	$XXX00000_B$	$0B8_H$

IP	*Interrupt Priority control*	$0XX00000_B$	$0A8_H$
IE	*Interrupt Enable Control*	00_H	89_H
TMOD	*Timer/Counter Mode Control*	00_H	88_H
TCON	*Timer/Counter Control*	00_H	$8C_H$
TH0	*Timer/Counter 0 high byte*	00_H	$8A_H$
TL0	*Timer/Counter 0 low byte*	00_H	$8D_H$
TH1	*Timer/Counter 1 high byte*	00_H	$8B_H$
TL1	*Timer/Counter 1 low byte*	00_H	98_H
SCON	*Serial Control*	Independen	99_H
SBUF	*Serial Data Buffer*	HMOS	87_H
PCON	*Power Control*	$0XXXXXXX_B$	
		CHMOS	

Sumber: *Elex Media Komputindo. Bereksperimen dengan Mikrokontroler 8031*

Beberapa macam *register* fungsi khusus mikrokontroller AT 89S52 sebagai berikut :

- *Accumulator* (register A) merupakan *register* untuk penambahan dan pengurangan. perintah *Mnemonic* untuk mengakses akumulator disederhanakan sebagai A.
- *Register* B merupakan *register* khusus yang berfungsi melayani operasi perkalian dan pembagian.
- *Program Status Word* (PSW) terdiri dari beberapa *bit* status yang menggambarkan kejadian di akumulator sebelumnya. Yaitu *carry bit, auxiliary carry,* dua *bit* pemilih bank, bendera *overflow, parity bit,* dan dua bendera yang dapat didefenisikan sendiri oleh pemakai.

- *Stack Pointer* (SP) merupakan *register* 8 *bit* yang dapat diletakkan di alamat manapun pada RAM internal. Isi *register* ini ditambah sebelum data disimpan, selama instruksi *PUSH* dan *CALL*. Pada saat *reset*, *register* SP di inisialisasi pada alamat 07_H, sehingga *stack* akan dimulai pada lokasi 08_H.
- *Data Pointer* (DPTR) terdiri dari dua *register*, yaitu *byte* tinggi (Data *Pointer High*, DPH) dan *byte* rendah (*Data Pointer Low*, DPL) yang berfungsi untuk pengalamatan alamat 16 *bit*.
- *Port* 0 sampai *port* 3 merupakan *register* yang berfungsi untuk membaca dan mengeluarkan data *port* 0, 1, 2, 3. Masing-masing *register* ini dapat dialamati per-*byte* maupun per-*bit*.
- *Serial Control Register* (SCON) Register yang berfungsi untuk mengontrol kerja port serial pada Mikrokontroller AT89S52 bersifat full duplex, yang berarti dapat mengirim dan menerima data secara bersamaan.
- Register penerima dan pengirim pada port serial diakses pada SBUF (*serial buffer*). Merupakan data dua *register* yang terpisah, *register buffer* pengirim dan sebuah *register buffer* penerima, mengirimkan data melalui transmisi *serial*. membaca data SBUF berarti menerima data dari *buffer* penerima.
- *Power Control Register* (PCON), *Control Register* untuk mengontrol sistem interupsi terdapat dua *register* khusus yaitu *register* IP *(Interrupt Priority)* dan *register* IE *(Interrupt Enable)*. *register* TCON Untuk mengontrol pelayanan *timer/counter* serta untuk pelayanan *port serial*.

2.2.8. Sistem Interupsi

Mikrokontroller AT89S52 mempunyai dua sumber interupsi eksternal dan interupsi internal yang dapat diprogram agar sensitif terhadap perubahan level atau transisi. Interupsi *timer* aktif saat *register timer* yang bersangkutan mengalami *rollover,* interupsi *serial* akan aktif pada saat mikrokontroller mengirim atau menerima data.

Setiap sumber interupsi dapat diaktifkan atau dimatikan melalui perangkat lunak. Interupsi yang mempunyai tingkatan prioritas lebih tinggi tidak dapat diinterupsi oleh yang lebih rendah. Meskipun demikian melalui perangkat lunak dapat diubah, yaitu dalam *register interrupt priority* (IP).

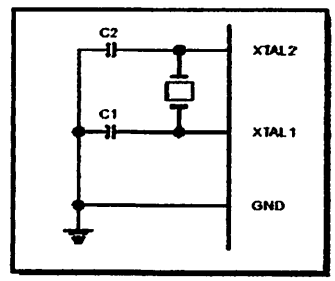
2.2.9. *Timer* atau *counter*

Apabila *timer* atau *counter* diaktifkan pada frekuensi kerja 11.059200 MHz, *timer* tersebut akan melakukan perhitungan waktu setiap 1 mikrodetik secara *independent*, tidak tergantung pada pelaksanaan instruksi. Satu siklus pencacahan waktu berpadanan dengan satu siklus intruksi, sedangkan satu siklus dilakukan dalam satu *mikrodetik* dan pada saat itu pula *timer* atau *counter* menunjukkan periode waktu 5 mikrodetik.

2.2.10. Osilator

Mikrokontroler AT89S52 memiliki osilator internal (*On chip oscillator*) yang dapat digunakan sebagai sumber pewaktuan (*clock*) bagi CPU. Untuk menggunakan osilator internal diperlukan sebuah kristal atau resonator keramik antara pin $XTAL_1$ dan pin $XTAL_2$ dan sebuah kapasitor ke *ground.* Untuk

kristalnya dapat digunakan kristal dengan frekuensi 11.05920 sampai dengan 24 MHz. berikut rangkaian osilator yang digunakan.



Gambar 2-4 *Oscilator External* Mikrokontroller AT89S52[1]

Sumber: Atmel AT89S52 *Data Sheet*

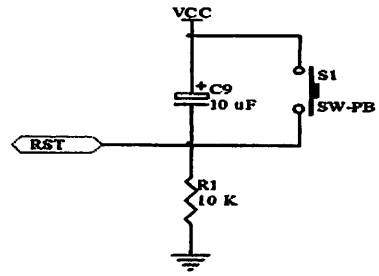
Didalam komunikasi serial antara mikrokontroler dengan komputer terlebih dahulu ditentukan *baud rate* yang digunakan. Pada sistem ini digunakan *baud rate* sebesar 9600 bps dengan menggunakan f_{osc} = 11,0592 MHz. Sesuai *data sheet* besar nilai kapasitor yang digunakan meliputi:

C1 = C2 = 30 pF ± 10 pF menggunakan kristal dan C1 = C2 40 pF ± 10 pF jika menggunakan Ceramic Resonator. Pewaktuan yang dihasilkan oleh osilator internal menentukan rentetan kondisi yang membentuk sebuah siklus mesin mikrokontroller. Siklus mesin terdiri dari 6 *state* mulai S1 sampai S6, masing-masing *state* dengan panjangnya 2 periode osilator dengan 1 siklus mesin paling lama dikerjakan dalam 12 perioda osilator.

2.2.11. Reset

Untuk mereset rangkaian mikrokontroller, dipilih rangkaian power – on reset. Rangkaian ini akan mereset mikrokontroller secara otomatis setiap kali catu daya diaktifkan, karena rangkaian reset akan menahan logika tinggi pada penyemat sehingga terjadi reset untuk jangka waktu tertentu. Jangka waktu

tersebut ditentukan oleh pengosongan muatan pada kondensator. Untuk memastikan keabsahan reset, logika yang lebih lama dari dua siklus mesin ditambah waktu mulai hidup (start – on) osilator. Input reset pada pin 9 adalah reset master untuk AT89S52.



Gambar 2.5. Rangkaian Reset AT89S52. [1]

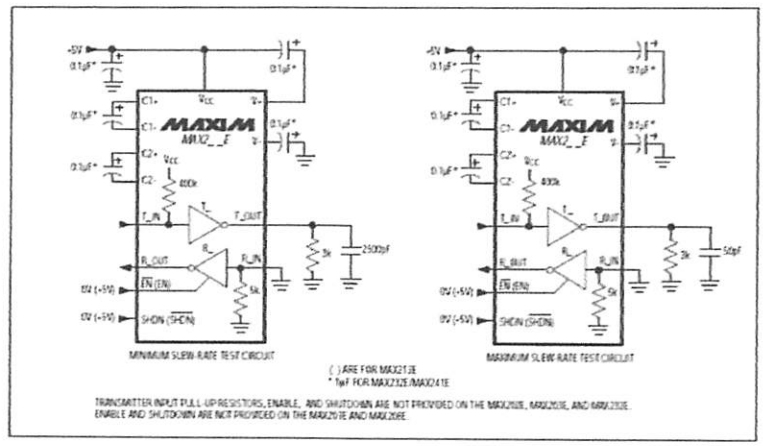
2.3. Komunikasi Serial

Yang dimaksudkan dengan komunikasi serial ialah pengiriman data secara serial yakni data dikirim satu per-satu secara berurutan, sehingga komunikasi serial jauh lebih lambat dari pada komunikasi paralel. Serial *port* lebih sulit ditangani karena peralatan yang dihubungkan ke serial *port* harus berkomunikasi menggunakan transmisi serial sedangkan data di komputer diolah secara paralel. Oleh karena itu data ke serial port harus dikonversikan kebentuk paralel untuk bisa digunakan.

Kelebihan komunikasi serial ialah jangkauan panjang kabel yang lebih jauh dibandingkan paralel karena serial *port* mengirimkan logika 1 dengan kisaran tegangan (-3 hingga -25 *volt*) dan logika 0 sebagai (+3 hingga +25 *volt*) sehingga kehilangan daya karena panjangnya kabel bukan masalah utama.

Sedangkan TTL bekerja pada level tegangan -5 s/d +5 Volt. Piranti tambahan yang kita butuhkan adalah IC MAX232. Pada dasarnya IC ini hanya

digunakan sebagai pengubah level tegangan ke level *Transistor Transistor Logic* (TTL), tidak berfungsi sebagai pengkodean sinyal yang melewati RS232 dan juga tidak mengkonversikan data serial ke paralel.



Gambar 2.6 *IC MAX232 sebagai pengubah level tegangan*[5]

Sumber: Data Sheet max-232

Tabel 2-5.

Spesifikasi Pin MAX-232 serta kegunaannya[5]

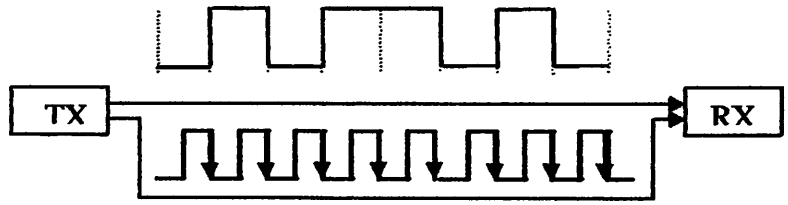
PIN	NAMA PIN	FUNGSI
1	C1+	Kapasitor *eksternal* '+' untuk *internal voltage doubler*
2	V+	Secara *internal* menghasilkan tegangan +10 volt
3	C1-	Kapasitor *eksternal* '-' untuk *internal voltage doubler*
4	C2+	Kapasitor *eksternal* '+' membalikkan tegangan *internal*
5	C2-	Kapasitor *eksternal* '-' membalikkan tegangan *internal*
6	V-	Secara *internal* menghasilkan tegangan -10 volt
7	$T2_{OUT}$	RS-232 *Transmitter* 2 dengan keluaran ±10 volt

8	$R2_{IN}$	Masukan RS232 *receiver* 2 dengan *resistor pulldown* 5K *internal* ke GND
9	$R2_{OUT}$	Keluaran *receiver* 2 TTL/CMOS
10	$T2_{IN}$	Masukan *transmitter* 2 TTL/ACMOS, dengan *resistor pullup* 400K *internal* ke Vcc
11	$T1_{IN}$	Masukan *Transmitter* 1 TTL/CMOS, dengan *resistor pullup* 400K *internal* ke Vcc
12	$R1_{OUT}$	Keluaran *receiver* 1 TTL/CMOS
13	$R1_{IN}$	Masukan RS232, dengan *resistor pulldown* 5K *internal* ke GND
14	$T1_{OUT}$	RS232 *transmitter* 1 dengan keluaran ±10V
15	GND	Ground
16	VCC	*Power Supply* positif +5V

2.3.1. Metode Transmisi Data Serial

Dalam komunikasi secara serial terdapat dua macam mode transmisi data serial dalam mentransmisikan bit-bit data harus ada sinkronisasi atau penyesuaian data antara pengirim dan penerima agar data yang dikirimkan dapat diterima dengan baik, antara lain yaitu sebagai berikut:

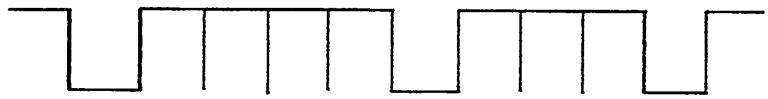
- *Komunikasi Serial Synchronous* adalah komunikasi dimana hanya ada satu pihak (pengirim atau penerima) yang menghasilkan *clock* dan mengirimkan *clock* tersebut bersama-sama dengan data. Berikut model komunikasi *Serial Synchronous.*



Gambar 2-7. Komunikasi serial dengan sinyal *Sinkronisasi*[5]

Setiap TX mengirimkan Dx atau bit ke x dari satu *byte* data akan diikuti dengan sinyal sinkronisasi yang berupa sinyal transisi dari rendah ke tinggi atau tinggi ke rendah. RX akan mengetahui bahwa dijalur data ada data milik Dx, sesuai dengan banyaknya sinyal sinkronisasi yang diterima, saat sinyal sinkronisasi pertama data milik D0, kedua milik D1dan seterusnya.

• *Komunikasi Serial Asynchronous* serial adalah komunikasi dimana kedua pihak (pengirim dan penerima) masing-masing menghasilkan *clock* namun hanya data yang ditransmisikan tanpa *clock* agar data yang dikirim sama dengan data yang diterima, maka kedua frekuensi *clock* harus sama terdapat sinkronisasi. Berikut bentuk komunikasi *Serial Asynchronous.*



Gambar 2-8. Format Sinyal Serial Asinkron[5]

Cara kedua dengan komunikasi *asinkron*, yaitu dengan menetapkan kecepatan bit dengan menyisipkan beberapa bit protokol, yaitu bit *START*, *PARITY* bit dan *STOP* seperti diperlihatkan pada gambar diatas.

2.3.2. Arah Pengiriman Data

Dikenal tiga macam arah pengiriman data, yaitu *Simplex, Half Duplex,* dan *Full Duplex.*

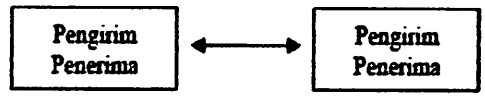
2.3.3. Mode Komunikasi *Simplex*

Merupakan sistem pemindahan data yang hanya dengan satu arah saja, misalnya dari A sebagai pengirim dan B sebagai penerima, dan tidak dapat mengirimkan data dari B ke A. Dalam komunikasi pengirim dan penerima adalah permanen.

Gambar 2.9. Hubungan Simplex

2.3.4. Mode Komunikasi Half Duplex

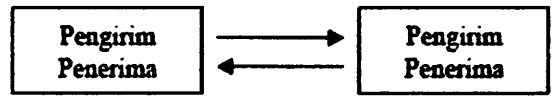
Merupakan sistem pemindahan data dua arah, tetapi tidak dapat dilakukan secara bersamaan, harus bergantian sebagai penerima atau sebagai pengirim data seperti yang ditunjukkan pada gambar berikut:



Gambar 2.10. Hubungan *Half-duplex*

2.3.5. Mode komunikasi Full-Duplex

Merupakan sistem pemindahan data dua arah dan dapat berlangsung secara bersamaan dalam satu waktu. Mode komunikasi *full duplex* dilakukan dalam dua arah yang terjadi secara bersamaan seperti ditunjukkan pada gambar dibawah ini.



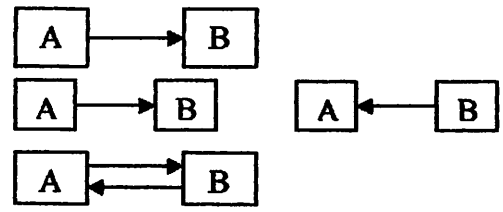
Gambar 2.11. Hubungan *Full-Duplex*

Untuk lebih jelasnya, dapat dilihat pada gambar berikut :

a. Komunikasi data *Simplex*

b. Komunkasi data *Half Duplex*

c. Komunikasi data *Full Duplex*



2.3.6. Kecepatan mobilitas data per-bit

Laju baud rate dalam kanal komunikasi merupakan laju tercepat dari pemindahan bit, laju pemindahan bit kanal jaringan biasanya lebih rendah dari laju baud rate. Keterlambatan tersebut karena bit ekstra ditambahkan untuk keperluan pewaktuan.

Dalam sistem kecepatan tinggi pemindahan data juga diperlambat oleh penundaan aktif proses pengolahan data serial dapat dimobilisasikan pada berbagai baud rate. Baud rate yang digunakan dalam teknik komunikasi sinyal *sinkronisasi* data serial 9600 bps. Terdiri dari 7 bit dan 8 bit (panjang data karakter saja).

2.3.7. Peralatan Komunikasi Serial

Perangkat keras pada komunikasi serial *port* dibagi menjadi dua kelompok, yaitu *Data Communication Equipment (DCE)* dan *Data Terminal Equipment (DTE)*. DTE ialah terminal di komputer. RS232 sebagai komunikasi serial mempunyai 9 pin yang memiliki fungsi masing-masing. Pin yang biasa digunakan

adalah pin 2 sebagai *received data*, pin 3 sebagai *transmited data*, dan pin 5 sebagai *ground signal*. Karakteristik elektrik dari RS232 adalah sebagi berikut :

- *Space (logic 0)* mempunyai level tegangan sebesar +3 s/d +25 Volt.
- *Mark (logic 1)* mempunyai level tegangan sebesar -3 s/d -25 Volt.
- Level tegangan antara +3 s/d -3 Volt tidak terdefinisikan.
- Arus yang melalui rangkaian tidak boleh melebihi dari 500 mA., ini dibutuhlan agar sistem yang dibangun bekerja dengan akurat.

Tabel 2.6.

Tabel Mode Serial dan *Baudrate*[5]

MODE	BAUDRATE	
0	1/12 f_{osc}	
1	SMOD = 0	SMOD = 1
	$Baudrate = \frac{fosc}{12 \times (256 - TH1) \times 32}$	$Baudrate = \frac{fosc}{12 \times (256 - TH1) \times 16}$
2	1/32 f_{osc}	1/32 f_{osc}
3	$Baudrate = \frac{fosc}{12 \times (256 - TH1) \times 32}$	$Baudrate = \frac{fosc}{12 \times (256 - TH1) \times 16}$

Sumber : www.delta-electronics.com

2.3.8. Baud Rate Serial

Baud rate dari Port Serial AT89S52 dapat diatur pada Mode 1 dan Mode 3, namun pada Mode 0 dan Mode 2, baud rate tersebut mempunyai kecepatan yang permanen yaitu untuk Mode 0 adalah 1/12 frekwensi osilator sedangkan Mode 2 adalah 1/64 frekwensi osilator. Dengan mengubah bit SMOD yang terletak pada

Register PCON menjadi set (kondisi awal pada saat sistem reset adalah clear) maka *baud rate* pada Mode 1, 2 dan 3 akan berubah menjadi dua kali lipat.

Pada Mode 1 dan 3 baud rate dapat diatur dengan menggunakan Timer1. Cara yang biasa digunakan adalah Timer Mode 2 (8 bit auto reload) yang hanya menggunakan register TH1 saja. Pengiriman setiap bit data terjadi setiap Timer 1 *overflow* sebanyak 32 kali sehingga dapat disimpulkan bahwa:

- Lama pengiriman setiap bit data = Timer 1 Overflow X 32
- Baud rate (jumlah bit data yang terkirim tiap detik)

Apabila diinginkan *baud rate* 9600 bps maka timer 1 harus diatur agar *overflow* setiap Timer 1 overflow setiap kali TH1 mencapai nilai limpahan *(overflow)* dengan frekwensi sebesar f /12 atau periode 12/f. Bit SMOD pada Register PCON, apabila bit ini set maka faktor pengali 32 akan berubah menjadi 16. Oleh karena itu dapat disimpulkan formula untuk *baud rate* serial untuk Mode 1 dan Mode 3 dalam sistem transmisi data menggunakan *Baud rate* 9600 bps maka perhitungan pada transmisi data sebagai berikut:

$$\text{Baudrate} = \frac{2^{SMOD}}{32} \times \frac{\text{Frequensi Osilator}}{12\,[256-(TH1)]}$$

$$9600\ \text{bps} = \frac{2^1}{32} \times \frac{11{,}0592.10^6}{12\,[256-(TH1)]}$$

$$[256-(TH1)] = \frac{2^1}{32} \times \frac{11{,}0592.10^6}{12 \times 9600}$$

$$[256-(TH1)] = \frac{2^1}{32} \times \frac{11{,}0592.10^6}{12 \times 9600}$$

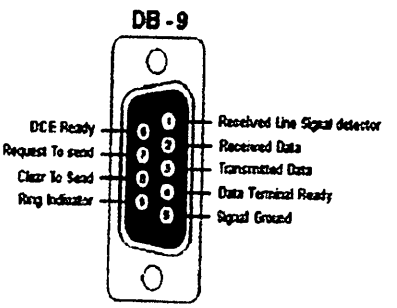
$$[256-(TH1)] = 3$$

$$TH1 = 256-3$$

$$TH1 = 253 \text{ atau } 0FDH$$

2.3.9. Antarmuka Serial RS - 485 Pada Personal Komputer (*PC*)

Pada *Personal Komputer* terdapat antarmuka serial yang mengikuti standar antarmuka RS-232 menggunakan rangkaian terintegrasi UART (*Universal Asyncronous Reciever/ Transmitter*). Personal Komputer dapat mempunyai beberapa antarmuka serial, dua diantaranya yang paling penting adalah *primary asynchronous communication adaptor* yang disebut COM 1 dan *secondary asynchronous adaptor* yang disebut COM 2. Standar ini menggunakan beberapa piranti dalam implementasinya adalah plug DB9 untuk RS232 biasanya dipakai untuk serial port pada komputer port mouse dan modem.



Gambar 2.12. Konektor serial DB-9 pada bagian belakang CPU

Keterangan fungsi saluran RS-232 pada konektor DB-9 adalah sebagai berikut:

- *DCE ready,* merupakan sinyal aktif yang menunjukan bahwa DCE sudah siap
- *Clear to Send,* dengan saluran ini DCE diminta untuk mengirim data oleh DTE
- *Ring Indikator,* pada saluran ini DCE memberitahukan ke DTE bahwa sebuah stasiun menghendaki hubungan denganya.
- *Receiver Line Signal Detect,* dengan saluran tersebut DCE memberitahukan ke DTE bahwa pada terminal masukan ada data masuk

- *Receiver Data*, digunakan pada saat menerima data dari DCE
- *Data Terminal Ready*, pada saluran ini DTE memberitahukan kesiapan terminalnya
- *Transmit Data*, digunakan DTE pada saat mengirimkan data ke DCE
- *Signal Ground*, merupakan saluran ground.

Tabel 2.7.

Fungsi masing-masing pin DB9[5]

RS232 Pin Assignments (DB9 PC signal set)	
Pin 1	*Received* Line Signal Detector (Data Carrier Detect)
Pin 2	*Received* Data
Pin 3	Transmit Data
Pin 4	Data Terminal Ready
Pin 5	Signal Ground
Pin 6	Data Set Ready
Pin 7	Request To Send
Pin 8	Clear To Send
Pin 9	Ring Indicator

Sumber: *Data Sheet max-232*

2.3.10. Sinyal Interface EIA 232 Terhadap DB9

Sinyal yang dikeluarkan oleh komputer secara DCE maupun DTE adalah:

- RLSD (Received Line Signal Detect1): Dengan saluran DCE memberitahukan ke DTE bahwa pada terminal masukan terdapat data yang masuk.

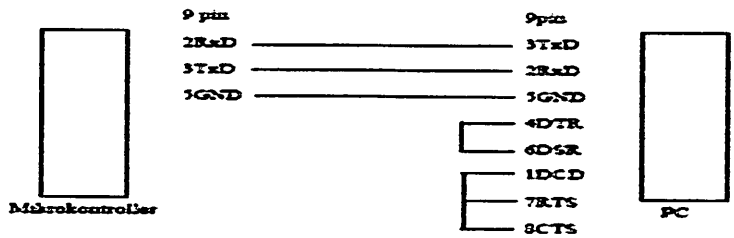
- RXD (Received Data): Sinyal yang digunakan DTE untuk menerima data dari DCE.
- TXD (Transmitted Data): Sinyal yang digunakan DTE untuk mengirim data ke DCE.
- DTR (DataTerminal *Ready*): Sinyal yang digunakan oleh PC untuk memberitahukan kepada DE bahwa PC siap menerima data dari DCE.
- Signal Ground (GND): Saluran ke bagian tanah / ground.
- DSR (Data Set Ready): Sinyal aktif pada saluran menunjukan bahwa DTE sudah siap.
- RTS (Request To Sead): Sinyal ini digunakan oleh PC untuk memberitahukan kepada DCE bahwa PC akan mengirim data dan apabila DE dalam kondisi siap maka modem akan memberikan sinyal CTS
- CTS (Clear To Sead): Sinyal yang dikirim oleh DCE untuk memberitahukan pada PC bahwa data boleh untuk dikirim
- RI (Ring Indikator): Pada saluran ini DCE memberitahukan kepada DCE bahwa station menghendaki hubungan denganya.

Komunikasi antara PC dengan mikrokontroler adalah komunikasi serial dimana menggunakan serial RS-232 sebagai konnektor interface. Pada mikrokontroler terdapat parameter setup windows yang harus diset sesuai dengan parameter MS Comm. Parameter-parameter tersebut antara lain:

- Transmission Speed : Pilih 9600

- Data Length : Pilih 8 bit sebagai bit data
- Stop bit : Pilih 1
- Parity Check : Pilih NONE
- Flow control : Pilih NONE

Untuk melakukan pengiriman data ke mikrokontroler maka untuk RS-232 sebagai konnektor interfacenya hanya menggunakan 3 pin saja



Gambar 2.13. Koneksi RS-232 pada mikrokontroller dan PC

Tabel 2.8.

Konfigurasi pin dan nama sinyal konektor serial

Nomor Pin	Nama Sinyal	Direction	Keterangan
1	DCD	In	Data Carrier Detect/Receiver Line Sinyal Detect
2	RXD	In	Receiver Data
3	TXD	Out	Transmit Data
4	DTR	Out	Data Terminal Ready
5	GND	-	Ground
6	DSR	In	Data Set Ready
7	RST	Out	Request to Send
8	CTS	In	Clear to Send
9	RI	In	Ring Indicator

2.3.11. Konverter Serial RS 232 to RS 485

Standar RS-485 yang diterapkan oleh Electronik Industry Association (EIA) dan Telecomunication Association (TIA) pada tahun 1983 sehingga standar RS 485 hanya membicarakan karakteristik sinyal dalam transmisi data secara *balanced digital multipoint sistem.* Sistem komunikasi dengan menggunakan RS 485 digunakan untuk komunikasi data antara 32 unit peralatan elektronik hanya dalam dua kabel saja. Selain itu, jarak komunikasi dapat mencapai 1,6 km dengan digunakannya kabel AWG-24 twisted pair.

RS232 yang hanya mampu membentuk jaringan *one to one* , menjadi mampu untuk dikembangkan ke sistem jaringan *one to many* dengan menggunakan kabel RS485 dengan tetap menggunakan terminal RS232 tanpa harus mengganti terminal RS232 menjadi terminal RS485

Dengan saluran sejauh 4000 *feet* dan kecepatan ≤1 megabit/detik. RS485 menggunakan saluran ganda (*Differensial atau Urbalancced transmition)* transmisi saluran ganda memakai satu pasang kabel untuk mengirim sinyal informasi logika yang ditransmisikan dari beda tegangan dengan 2 saluran yang bersifat berlawanan, satu kabel bertegangan tinggi.

Maka kabel yang lain bertegangan rendah, sedangkan rangkaian penerima sinyal membandingkan tegangan kedua kabel saluran dengan level logika pada bagian output ditentukan oleh kabel posistif. Jadi jauh lebih sederhana penggunaanya dibandingkan dengan standar RS232 yang mencakupi ketentuan tentang karakteristik sinyal, serta konfigurasi sinyal pada kaki konektor dan juga tata cara pertukaran informasi antara komputer dengan alat pelengkap lainya.

Meskipun demikian saluran ganda tidak dipakai untuk mentransmisikan banyak saluran, mengingat RS485 dapat menggunakan saluran *half duplex* yaitu saluran dua arah secara bergantian untuk menghubungkan line *receivers* menjadi satu sistem sebagai komunikasi *Multidroop (Multi Comunicattion)* biasa digunakan untuk menyediakan *signal* serial yang kuat pada *boudraet* yang tinggi dalam lingkungan listrik yang berpotensi menimbulkan *noise* atau interferensi elektromagnetik yang tinggi.

2.3.12. Spesifikasi dari RS-485

Tabel 2-9.

Address Register RS-485[5]

Nama Register	**COM1**	**COM2**
TX Buffer (Transmit Buffer)	03F8H	02F8H
RX Buffer (Receive Buffer)	03F8H	02F8H
Baud rate devisor latch LSB	03F8H	02F8H
Baud rate devisor latch MSB	03F9H	02F9H
Interrupt Enable Register	03F9H	02F9H
Interrupt identification Register	03FAH	02FAH
Line Control Register	03FBH	02FBH
Modem Control Register	03FCH	02FCH
Line Status Rgister	03FDH	02FDH
Modem Status Register	03FEH	02FEH

Sumber: Data Sheet max- RS-485

Fungsi dari beberapa Address Register diantaranya adalah sebagai berikut:

a) TX *buffer* : menampung dan menyimpan data yang akan dikirim keluar. Data ini dikirim oleh CPU ke TX *buffer* setelah mengecek kepastian tentang diperbolehkannya melakukan pengiriman.

b) RX *buffer* : menampung dan menyimpan data yang diterima dari luar. data itu harus dibaca oleh CPU setelah mengecek kepastian tentang masukannya data.

c) *Baud rate devisor last significant bit*: menampung angka byte bobot rendah untuk pembagi clock yang akan dimasukkan agar didapat baudrate yang diplih. Angka pembagi dapat dipilih antara 01H hingga FFH.

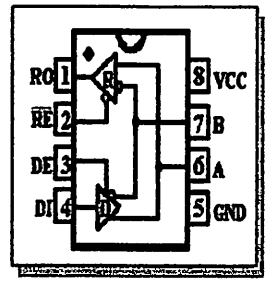
d) *Baud rate devisor most significant bit*, menampung angka *byte* bobot tinggi untuk pembagi *clock* yang akan dimasukkan agar didapat *baud rate* yang dipilih. Angka pembagi dapat dipilih antara 00H hingga FFH.

Tabel 2.10

Spesifikasi RS-485

Keistimewaan	Karakteristik
Jenis operasi	*Differential* (seimbang)
Jenis penggerak dan Penerima per jalur	1 *driver* 32 *receiver*
Data rate maksimum	10 Mbps
Panjang saluran maksimum	4000 ft (1200 m)
Tegangan keluaran penggerak	± 1,5 volt
Sensitivitas penerima	± 200 mV

Sumber : *Anonymous* , 2000

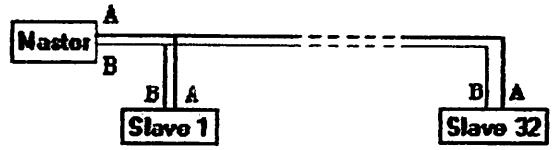


Gambar 2.14 Bentuk Mekanis Komponen IC RS-485[5]

Sumber: *Anonymous* , 1996:7

2.3.13. SN75176

SN75176 adalah IC yang menjadi komponen utama Modul SR-485 yang didisain untuk komunikasi data secara *bidirectional* atau *multipoint* dengan Standard ANSI EIA/TIA-422-B dan ITU V11. Data yang ditransmisikan oleh IC ini dikirim dalam bentuk perbedaan tegangan yang ada pada kaki A dan B dari dari kondisi kaki-kaki kontrolnya yaitu DE dan RE. Apabila kaki DE berlogika 0 dan RE berlogika 0, maka SN75176 berfungsi sebagai penerima data sedangkan bila kaki DE berlogika 1 dan RE berlogika 1 maka SN75176 berfungsi sebagai pengirim.



Gambar 2-15. Diagram Komunikasi Data Master dan 32 Slave

Register adalah memori sementara yang digunakan untuk pengolahan data, register geser (shift register) merupakan memori sementara yang dapat dipindahkan dengan jalan menggeser dari tingkat bit rendah ke yang lebih tinggi atau sebaliknya. Dalam perancangan ini menggunakan register geser dengan masukan seri dan keluaran parallel 8 bit dengan tipe IC 74LS164.

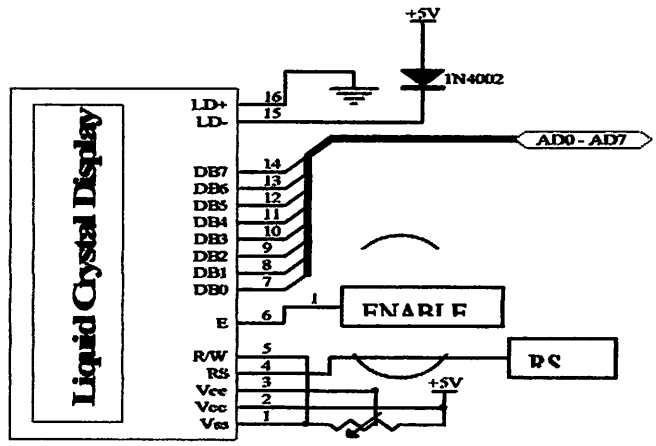
2.4. LCD (Liquid Crystal Display) M1632

M1632 merupakan modul LCD *matrix* dengan konfigurasi 16 karakter dan 2 baris dengan tiap karakter dibentuk oleh 8 baris pixel dan 5 kolom pixel (*1 baris pixel terakhir adalah kursur*). Yang terbentuk oleh hubungan antara layar LCD dengan HD44780 yang merupakan mikrokontroler kendali LCD. HD44780 ini sudah tersedia dalam mudul M1632.

HD44780 sebetulnya merupakan mikrokontroler yang dirancang khusus untuk mengendalikan LCD dan mempunyai kemampuan untuk mengatur proses *scanning* pada layar LCD yang terbentuk oleh 16 COM dan 40 SEG sehingga mikrokontroler/perangkat yang mengakses modul LCD ini tidak perlu lagi mengatur proses *secenning* pada layar LCD. Mikrokontroler hanya mengirimkan data-data yang merupakan karakter yang akan ditampilkan pada LCD.

Spesifikasi modul LCD M1632 adalah :

- Dua baris tampilan LCD yang terdiri dari 5X7 dot matrix ditambah kursor, masing-masing baris 16 karakter.
- ROM membangkitkan 192 tipe karakter.
- RAM untuk data penampil sebanyak 80X8 bit (maksimum 80 karakter).
- Osilator internal. Secara otomatis akan reset saat catu daya dinyalakan.



Gambar 2.16. Blok Diagram LCD M1632[3]

Sumber : Seiko : 1987 : 3

Konfigurasi Pin LCD M1632:

1. Vcc : +5V
2. GND : 0V
3. VEE : Tegangan Kontras LCD
4. RS : *Register Select*
5. R/W : 1= *read*, 0 = *write*
6. E : *Enable Clock LCD*
7. D0 - D7 : Data Bus 0 - Data Bus 7
8. Anode : Tegangan positif *backlight*
9. Katode : Tegangan negatif *backlight*

Untuk dapat berhubungan dengan mikrokontroler pemakai, LCD M1632 dilengkapi dengan 8 jalur data (DB0..DB7) yang digunakan untuk menyalurkan kode ASCII maupun perintah pengatur kerjanya M1632. Selain itu dilengkapi pula dengan E, R/W dan RS. Kombinasi lainya E dan R/W merupakan sinyal

standar buatan Motorola. Proses mengirim/mengambil data dari M1632 dijabarkan sebagai berikut:

1. RS harus dipersiapkan dulu, untuk menentukan jenis data yang dikirim ke M1632.
2. R/W di-nol-kan untuk menandakan akan diadakan pengiriman data ke M1632. Data yang akan dikirim disiapkan di DB0..DB7, sesaat kemudian sinyal E disatukan dan dinol kan kembali. Sinyal E merupakan sinyal sinkronisasi, saat E berubah dari 1 menjadi 0 data di DB0 .. DB7 diterima oleh M1632.
3. Untuk mengambil data dari M1632 sinyal R/W di-satu-kan, menyusul sinyal E disatukan. Pada saat E menjadi 1, M1632 akan meletakkan datanya di DB0 .. DB7, data ini harus diambil sebelum sinyal E di-nol-kan kembali.

Setelah diberi sumber daya, ada beberapa langkah persiapan yang harus dikerjakan dulu agar M1632 bisa digunakan.

Langkah-langkah tersebut antara lain adalah :

1. Tunggu dulu selama 15 mili-detik atau lebih.
2. Mengirim perintah 30h, artinya transfer data antara M1632 dan mikrokontroler dilakukan dengan mode 8 bit.
3. Tunggu selama 4.1 mili-detik.
4. Kirimkan sekali lagi perintah 30h.
5. Tunggu lagi selama 100 mikro-detik.

Tabel 2.13

Fungsi Kaki-Kaki M1632[3]

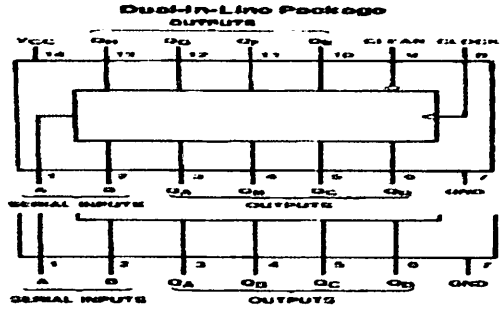
No Pin	Nama Penyemat	Fungsi
1	Vss	0 V (GND)
2	Vcc	5V ±10%
3	Vee	Drive LCD
4	RS	Pemilih Register 0 = Instruksi register (tulis) Bussy flag dan address counter (baca) 1 = Register data (baca dan tulis)
5	R/W	Sinyal pemilih baca dan tulis 0 = tulis 1 = baca
6	Enable	Sinyal untuk mengawali operasi
7-14	Data Bus	Saluran data
15	V + BL	Pengendali kecerahan latar belakang LCD, 4-4,42 V dan 50-200 mA
16	V – BL	Pengendali kecerahan latar belakang LCD, 0 V

Sumber : Seiko : 1987 :2

2.4.1. IC 74LS164

DM 74LS164 merupakan sebuah IC yang berfungsi sebagai *shift register* 8-bit. IC ini memiliki 2 *serial input, input clock, input reset* dan *output paralel.* Dan merupakan IC *Shift register 8-bit* dengan input data serial dan output data parallel yang digunakan sebagai interface data antara LCD dengan mikrokontroler AT89S52.

Pada saaat logika *LOW*, kedua *input* menghalangi masukan data baru dan me*reset* flip-flop pertama menjadi *LOW* pada saat pulsa *clock* pulsa berikutnya, hal ini untuk mengendalikan data yang masuk. Sedangkan pada saat logika *HIGH*, kedua *input* memungkinkan adanya inputan yang lain, yang mana kemudian akan menentukan status flip-flop yang pertama, data pada *serial input* kemungkinan akan berubah pada saat *clock high* atau *low* akan tetapi informasinya saja yang akan masuk



Gambar 2.17 Konfigurasi PIN IC DM 74LS164[4]

(Sumber: Thomson, 1994:1)

Prinsip dasar kerja dari register geser ini adalah bila 1 bit data dimasukkan ke inputan bersama dengan naiknya pulsa clock maka satu bit akan disimpan dan dikeluarkan oleh RS flip-flop yang pertama (Q_A) sedangkan keadaan keluaran yang lain (Q_B sampai Q_H) seperti keadaan semula dan apabila di-inputkan lagi bit ke dua bersama dengan clock, maka bit yang ada di Q_A akan digeser ke Q_B, sedangkan isi Q_A adalah bit yang baru di-inputkan tersebut, dan itu akan berlaku terus selama masukan diberi data bersamaan dengan pulsa clock. Untuk menghapus isi dari setiap register yaitu dengan memberikan sinyal low pada clear. Pada tabel 2-5 menunjukkan hubungan input dan output dari 74LS164.

Tabel 2.14.

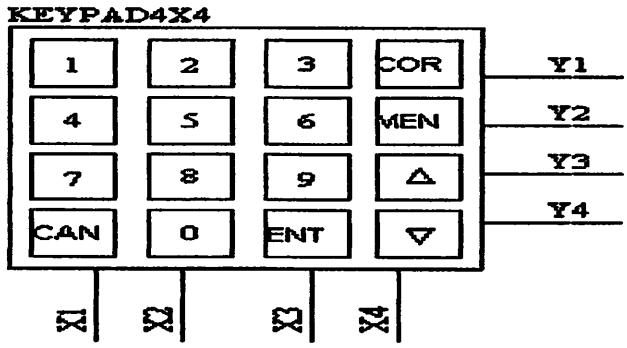
Tabel Kebenaran IC74LS164[4]

Output Control	Latch Enable	Data (Dn)	Output (Qn)
L	H	H	H
L	H	L	L
L	L	X	Qo
H	X	X	Z

Sumber: Thomson, 1994:1)

2.5. Keypad 4x4

Keypad merupakan salah satu sarana untuk memasukkan suatu data ke komputer atau minimum sistem. Untuk rangkaian keypad dalam skripsi ini digunakan keypad matrik 4 x 4. Keypad matrik 4 x 4 merupakan susunan 16 tombol membentuk keypad sebagai sarana masukan ke Mikrokontroller, meskipun jumlah tombol ada 16 tapi hanya memerlukan 8 jalur port pararel, seperti pada gambar dibawah ini :



Gambar 2-18 Keypad 4 x 4[6]

Dalam gambar tersebut masing-masing tombol menghubungkan sebuah jalur *output* (K1; K2; K3 atau K4) ke sebuah jalur *input* (B1; B2; B3 atau B4),

seperti yang digambarkan secara rinci dalam bulatan bagian kanan gambar, tombol "A" menghubungkan jalur K1 ke jalur B4.

Semua tombol mekanis yang biasa dipakai untuk *keypad*, saat ditekan tombol dilepas akan bergetar selama lebih kurang 30 sampai 50 mili-detik, sifat ini akan mengakibatkan sub-rutin pembacaan *keypad* merasakan adanya penekanan tombol secara berulang-ulang, meskipun sesungguhnya tombol hanya ditekan sekali saja. Gejala ini biasanya disebut sebagai *bounce*. Untuk mengatasi masalah ini, setelah berhasil membaca nilai tombol yang ditekan, kontroller dipaksa "istirahat" berapa saat sampai tombol tidak bergetar, sebelum membaca tombol berikutnya.

2.6. *Personal Komputer*

IBM PC mempunyai organisasi dan struktur yang sama dengan PC yang lainya. diantaranya prosesor, memori utama , memori sekunder *input / output*.

2.6.1. Prosesor

Central Processing Unit (CPU) adalah "otak" dari sebuah komputer. Fungsi CPU adalah menjalankan program yang disimpan dalam memori utama dengan cara mengambil dan menguji instruksi tersebut dan kemudian menjalankanya satu demi satu. Komponen-komponen itu dihubungkan oleh sebuah bus, yaitu sekumpulan kabel paralel untuk mentransmisikan alamat (*address*) data dan sinyal-sinyal kontrol. *Bus* dapat berada diluar CPU, yang menghubungkan CPU dengan memori dan peralatan I/O (input/output).

CPU juga berisi sebuah memori kecil berkecapatan tinggi yang digunakan untuk menyimpan hasil-hasil sementara dan informasi kontrol tertentu. Memori ini terdiri dari sejumlah register, yang masing-masing memiliki ukuran dan fungsi tersendiri. Setiap register dapat menyimpan satu bilangan, hingga mencapai jumlah maksimum tertentu tergantung pada ukuran register tersebut. Register-register dapat dibaca dan ditulis dengan kecepatan tinggi karena berada dalam CPU. Register yang paling penting adalah *Program Counter* (PC) yang menunjuk ke instruksi berikutnya yang harus diambil untuk dijalankan.

2.6.2. Memori Utama

Memori adalah bagian dari komputer tempat program-program dan data-data disimpan. Tanpa sebuah memori sebagai tempat untuk mendapatkan informasi guna dibaca dan ditulis oleh mikroprosesor.

2.6.3. Memori Sekunder

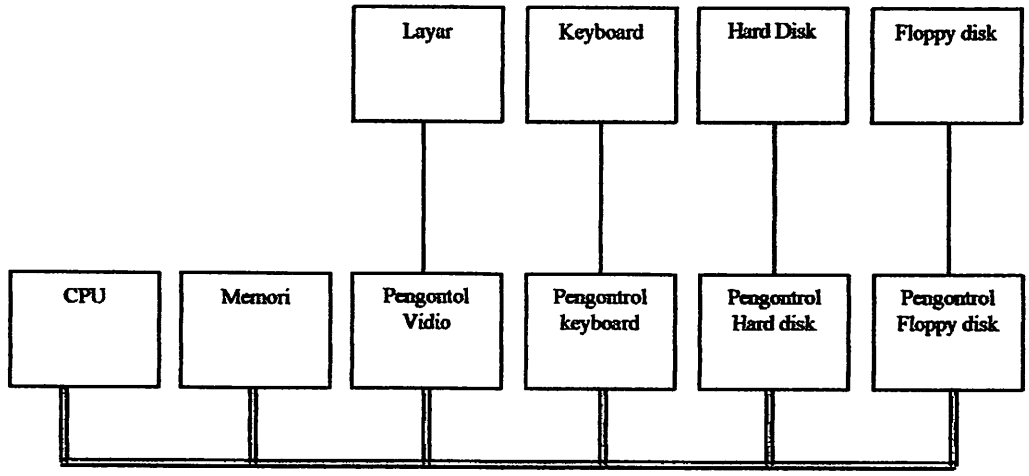
Memori sekunder terdiri dari disk magnetik, *floppy disk*, disk-disk IDE, disk-disk SCSI, RAID, CD-ROM, CD-RW, DVD dan banyak lagi yang lainnya.

2.6.4. Bus Data

Struktur komputer memiliki sebuah *bus* tunggal yang digunakan untuk menghubungkan CPU, memori dan piranti-piranti I/O sebagian besar sistem memilki dua *bus* atau lebih. Masing-masing piranti I/O terdiri dari dua bagian, bagian pertama memuat sebagian besar elektronik yang disebut pengontrol, dan bagian satunya lagi memuat piranti I/O itu sendiri, seperti misalnya *disk drive*.

Tugas pengontrol adalah untuk mengontrol piranti I/O dan menangani akses *bus* untuk piranti I/O tersebut. Sebagai contoh, ketika sebuah program

menghendaki data dari *disk*, program memberikan perintah kepada pengontrol *disk* yang selanjutnya menerbitkan pencarian dan perintah-perintah lainnya kepada *drive*. Pada umumnya piranti-piranti I/O diberi prioritas diatas CPU, sebab disk dan piranti-piranti bergerak lainnya tidak dapat dihentikan dan memaksa piranti-piranti tersebut untuk menunggu akan kehilangan data. Ketika tidak ada I/O yang tidak bekerja, CPU dapat memiliki semua siklus *bus*. Tetapi ketika piranti I/O tetentu juga sedang bekerja, maka piranti itu akan meminta siklus tersebut. Proses ini disebut siklus pengambil alihan dan akan memperlambat komputer.



Gambar 2-19 Stuktur *Logic* Untuk Komputer Sederhana

Sumber: Atmel AT 89S52 Data Sheet

2.7. Bahasa Pemrograman Borland Delphi

Delphi adalah perangkat lunak untuk menyusun program aplikasi yang berdasarkan pada bahasa pemrograman bahasa *pascal* dan bekerja dalam lingkungan sistem operasi *Windows.* Karena *Delphi* menggunakan komponen-komponen yang akan menghemat penulisan program dengan fasilitas *VCL (Visual Component Library).*

Dalam pembuatan sebuah program, *Delphi* menggunakan sistem yang disebut *RAD (Rapid Aplication Development).* Sistem ini memanfaatkan bahasa pemrograman visual yang membuat seorang programmer lebih mudah mendesain tampilan program (*User Interface.* Cara ini bermanfaat untuk membuat program yang bekerja pada sistem *Windows* yang memang tampilan layarnya lebih rumit (sekaligus dapat dilihat dengan indah) dibanding dengan sistem DOS.

Aplikasi dalam tatanan *GUI (Graphical User Interface)* yaitu karakter program aplikasi yang menggunakan sarana perantara grafis dapat dibentuk dengan *Delphi.* Seperti kotak dialog (*dialog box*), tombol (*button, menu*) dan lain sebagainya. Dengan *Delphi* sebuah *Windows* yang mengandung tombol-tombol, kotak cek, tombol pilihan panel dan komponen lainnya dapat dengan mudah diciptakan.

2.7.1. IDE (*Integrated Development Environment*) Delphi

IDE adalah suatu lingkungan dimana sebuah tools yang diperlukan untuk desain, menjalankan dan mengetes sebuah aplikasi disajikan dan terhubung dengan baik sehingga memudahkan pengembangan program. Pada *Delphi* terdiri

dari *main Windows, Component Palette, Toolbar, Form designer, Code Editor, Code Explorer.*

2.7.2. *Main Windows* (jendela utama)

Main Widows adalah bagian utama dari IDE. *Main Windows* mempunyai semua fungsi utama dari program-program *Windows* lainnya. *Main Windows* dibagi tiga bagian yaitu *menu utama, toolbar*, dan *component palette.*

❖ **Menu utama.** Seperti program *Windows* lainnya, menu utama dipakai untuk membuat dan menyimpan file memanggil *wziard*, menampilkan jendela lain, mengubah option dan lain sebagainya setiap pilihan pada menu juga dapat dipanggil dengan sebuah tombol pada *toolbar.*

❖ ***Toolbar.*** Beberapa operasi pada menu utama dapat dilakukan melalui *toolbar.* Setiap tombol pada toolbar mempunyai sebuah *tooltip* yang berisi informasi mengenai fungsi dari tombol tersebut. Selain *component palette*, ada 5 *toolbar* terpisah yaitu *debug, desktop, standart, view, dan custom.*

❖ ***Component Palette*** adalah toolbar dengan ketinggian ganda, yaitu berisi page kontrol dengan semua komponennya dari menu utama.

❖ ***Form designer.*** Diawali dengan jendela kosong yang memungkinkan untuk merancang aplikasi *Windows*.Berinteraksi dengan *form designer* dengan cara memilih komponen *palette* dan meletakkannya ke dalam *form.*

❖ **Object Editor.** Object Editor terdiri dari dua tab yaitu *tab properties* dan *tab events. Tab properties* memberi fasilitas untuk melihat dan mengubah

property dari setiap item. Klik pada sebuah form kosong, dan perhatikan atribut-atribut yang ada. Jika terdapat tanda + disamping property maka *property* tersebut berarti mempunyai *sub property*

❖ **Struktur Menu Delphi.** Struktur menu Delphi memberikan tools untuk mengakses lingkungan Delphi.

a. **Menu file** adalah menu paling penting dan akan dijabarkan pada bagian berikut:

b. ***New Application :*** Digunakan untuk membuat *project* baru.

c. ***New Form*** **:** Menu ini dipakai untuk membuat form baru.

d. ***New frame*** **:** Untuk membuat frame kosong dan menambahkannya ke dalam *project.*

e. ***Open*** **:** Menyatakan pada *Delphi* bahwa akan dibuka sebuah object dapat berupa sebuah program atau seluruh *project.*

f. ***Open Project*** **:** Untuk membuka sebuah project.

g. ***Reopen*** **:** Menu ini dipakai untuk membuka object favorit yang sudah pernah dibuka.

h. ***Save*** **:** Menu ini dipakai untuk menyimpan *module* yang sedang aktif.

i. ***Save as*** **:** Dipakai untuk menyimpan *module* dengan nama lain.

j. ***Save project as.:*** Menu ini dipakai untuk menyimpan project dengan nama baru.

k. ***Save al*** **:** Menyimpan sebuah object yang dibuka.

l. ***Close*** **:** Untuk menutup module program dengan formnya.

m. ***Close al*** : Menutup project.

n. ***Use Unit*** **:** Delphi akan menambahkan *klauda uses* pada program yang dibuat. Artinya sebuah unit akan dipakai dalam project.

o. ***Print*** **:** Mencetak item Delphi yang telah dipilih.

p. ***Exit*** **:** Keluar dari aplikasi Delphi.

q. ***Edit*** **:** Dipakai untuk menyuting program.

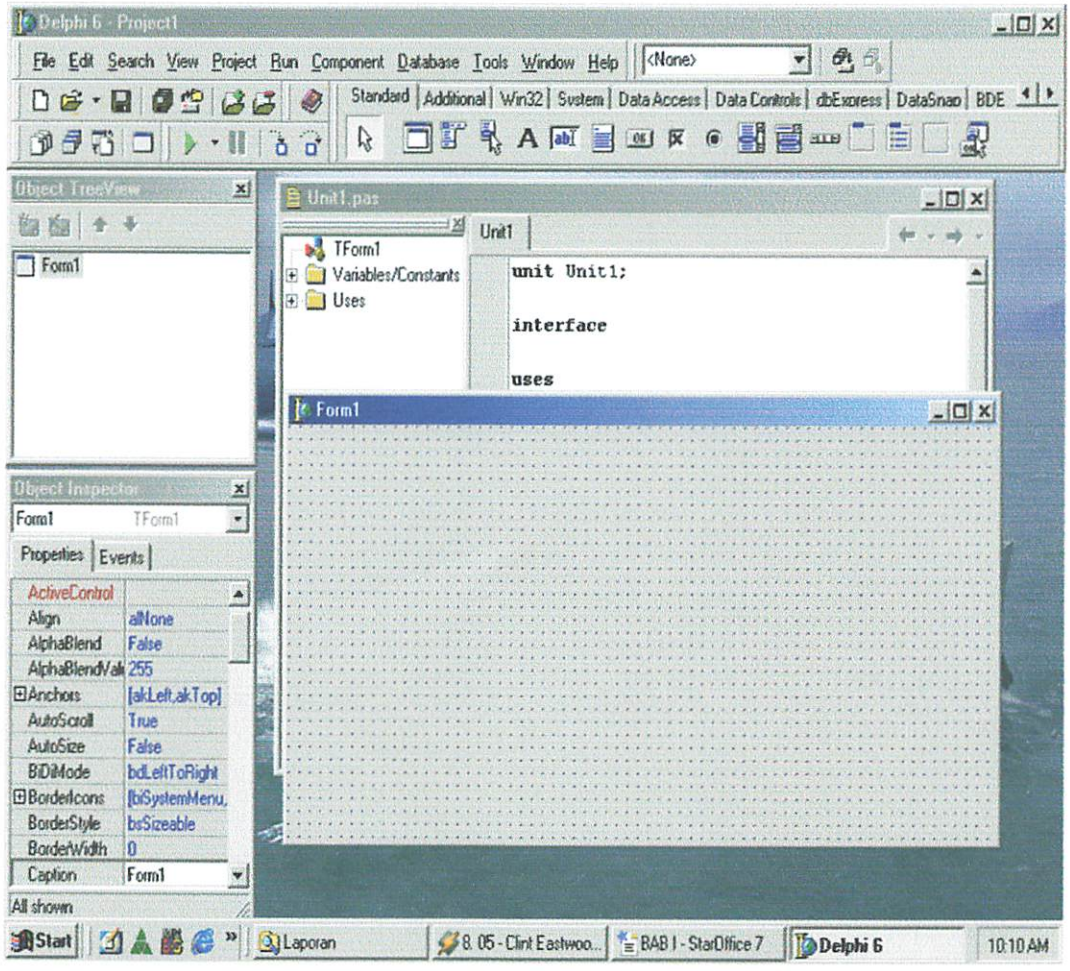
r. ***Search*** **:** Dipakai untuk mencari dan mengganti kata-kata pada saat menyuting program.

s. ***View*** **:** Dipakai untuk menampilkan atau menyembunyikan jendela-jendela tertentu, misalnya *object inspector, code explorer, debug* dan lain-lain.

t. ***Project*** **:** Dipakai untuk mengelola *project. Form daplay* ditambah dan dibuang dari object dengan mengkompilasi project dan lain-lain.

u. ***Run*** **:** Menu ini dipakai untuk menjalankan program dan memantau jalannya program. pada saat di run dan apabila terjadi salah tulis akan dapat diketahui.

v. ***Component :*** Dengan menu ini komponen baru dapat ditambah atau diinstal.



Gambar 2-19. Lembar Kerja Delphi

Sumber : www.ilmukomputer.com

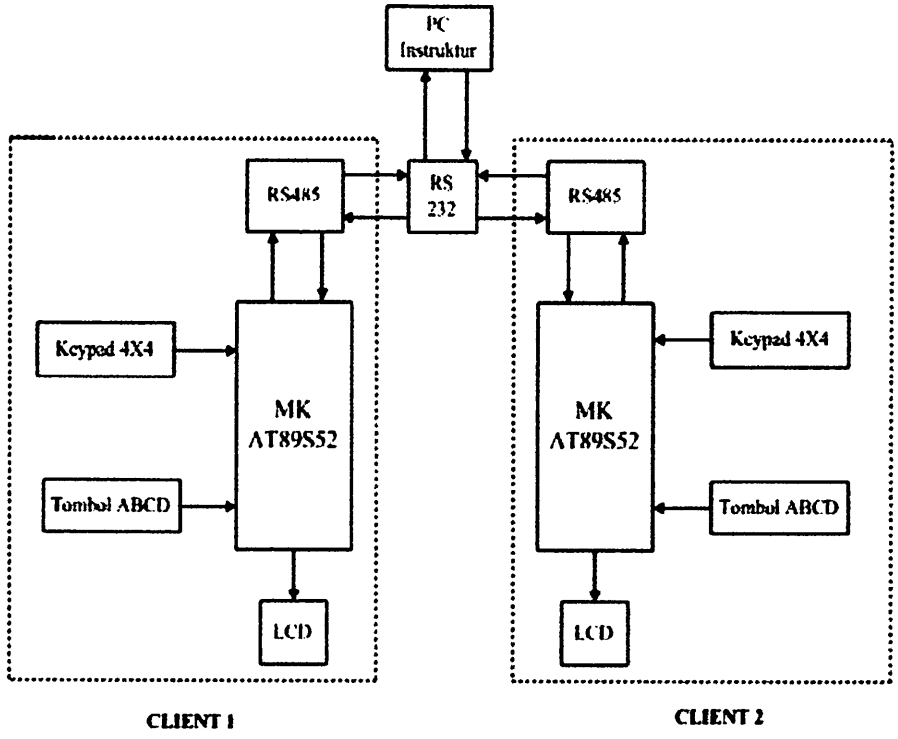
BAB III

PERANCANGAN DAN PEMBUATAN ALAT

Bab ini membahas perancangan alat untuk *Test Toefl*. Pembuatan alat disini dibagi dalam beberapa blok perangkat yang mempunyai fungsi sendiri-sendiri. Pembuatan sistem meliputi perancangan perangkat keras dan perangkat lunak.

3.1 Perencanaan Perangkat Keras

Diagram blok sistem pengerjaan alat pada test *toefl* menggunakan *Personal Computer* pada bagian instruktur pelaksana ujian, dapat dilihat dalam Gambar 3.1 di bawah ini:



Gambar 3.1 Diagram Blok Keseluruhan Sistem Alat

❖ Fungsi diagram blok sistem alat adalah :

1. Unit system Mikrolontroller AT89S52 merupakan unit pengolah data.
2. Unit *Keypad* 4x4 sebagai memasukan data identitas *client/* peserta test.
3. Unit LCD sebagai penampil data ID *Client,* beserta menampilkan soal pilihan ganda.
4. Unit Tombol Penjawab Soal sebagai inputan untuk menjawab soal pilihan ganda (A,B,C,D)
5. Unit *Personal Komputer* sebagai tampilan *data base* soal dan ID peserta.
6. Unit Komunikasi serial Menggunakan (RS 485 ke RS-232) sebagai jalur transfer data serial antara mikrokontroler dengan komputer instruktur.

3.1.2. Prinsip kerja alat sebagai berikut:

Alat bekerja berdasarkan kinerja *Software* yang menjalankan instruksi ke sistem kerja alat secara keseluruhan. Penggunaan mikrokontroller AT89S52 sebagai pengontrol utama pada alat bekerja berdasarkan adanya masukan data dari *keypad* berupa ID Client yang ditampilkan ke LCD. Selanjutnya data dikirim ke PC sebagai *database client*. Dengan menggunakan fungsi kerja RS232 dan RS485 dalam mentransfer data kebagian PC instruktur, sehingga data serial ke PC yang telah memuat data Id maupun data hasil jawaban soal *toefl,* akan tersimpan sebagai database.

3.2. Perancangan Perangkat Keras

3.2.1. Mikrokontroller AT89S52

Perancangan alat menggunakan mikrokontroller AT89S52 sebagai kontrol utama pada alat. Rangkaian ini digunakan untuk pengontrolan kerja alat *test toefl*, yang terdiri dari sebuah *chip* tunggal sebagai pengolah data yang terdiri atas 40 pin sebagai fungsi dalam menghubungkan dengan rangkaian lainya sehingga membentuk suatu minimum sistem.

Komunikasi data serial antara Mikrokontroller dengan PC Instruktur, melalui jalur data serial RS 485 dan RS232 yang terhubung dengan *port* (DB9) yang terdapat pada PC, dalam proses *interface* data dengan memanfaatkan fungsi pin *Tx*, *Rx* yang ada pada AT89S52 digunakan sebagai komunikasi *serial*..

3.2.1. Perancangan Rangkaian *Clock*

Kecepatan proses yang dilakukan oleh mikrokontroler AT89S52 ditentukan oleh sumber *clock* (pewaktuan). Sistem yang dirancang menggunakan *oscilator* internal yang tersusun dari 2 buah *capasitor* dan sebuah kristal atau *resonator* keramik, digunakan sebagai rangkaian pembangkit *internal clock generator.* Rangkaian ini terdiri dari dua buah kapasitor dan sebuah kristal, dengan ketentuan sebagai berikut:

C1 dan C2 = 20pF – 40pF untuk kristal

C1 dan C2 = 30pF – 50pF untuk resonator keramik

Untuk menentukan frekuensi osilatornya cukup dengan cara menghubungkan kristal pada pin XTAL1 dan XTAL2 serta dua buah kapasitor ke

ground. Besar kapasitansinya disesuaikan dengan spesifikasi pada lebar data AT89S52 yaitu 30 pF.

Pemilihan besar frekuensi kristal disesuaikan dengan pemilihan kecepatan yang diharapkan untuk transfer data melalui pin *serial interface* AT89S52 tersebut. Sistem ini dirancang untuk memiliki kemampuan *baud rate* sebesar 9600 bps, sehingga dipilih kristal dengan nilai 11,0592 *MHz* sesuai dengan spesifikasi pada lembar data 89S52. Siklus tersebut berdasarkan ketentuan mikrokontroller AT89S52 yaitu 12 *clock* = 1 siklus mesin. Sedangkan perhitungannya dapat dilihat dari bentuk rumus sebagai berikut:

$$T = \frac{1}{f}$$

$$f = 11{,}0592 \quad \text{MHz}$$

$$T = \frac{1}{11{,}0592.10^{6}} \text{ s}$$

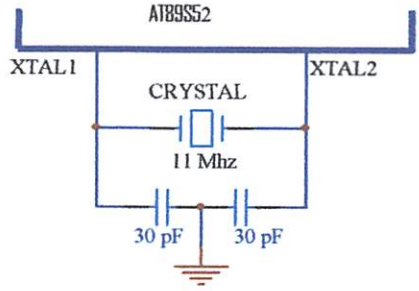
$$T = 9{,}042 \times 10^{-8} \ \mu\text{s}$$

frekwensi yang digunakan 12 MHz, maka waktu yang dipakai dalam setiap 1 siklus mesin adalah 1μs. Karena 1 siklus mesin = 12 T.

$$\text{Maka,1 siklus mesin} = 12 \times \frac{1}{11.0592 \times 10^{6}}$$

$$= 1{,}085 \ \mu\text{s}.$$

Program akan dijalankan selama 1,085 μs. Karena nilai kristal yang digunakan sebesar 11,0592 MHz.

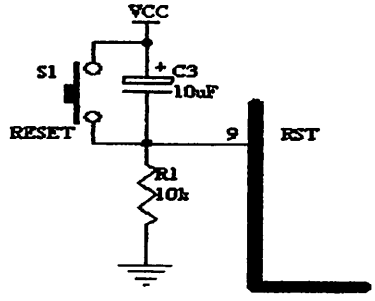


Gambar 3.2 Perancangan Rangkaian Clock

3.2.3. Rangkaian Reset

Penggunaan rangkaian *reset* sebagai rangkaian yang mendukung kerja dari mikrokontroller AT89S52 bertujuan agar mikrokontroller dapat menjalankan proses dari awal. Terbentuk oleh komponen Resistor dan kapasitor, mempunyai kemampuan *power on reset*, *reset* terjadi pada saat sistem dinyalakan untuk pertama kalinya. *Reset* terhadap mikrokontroller merupakan masukan aktif *high* '1'. Pulsa transisi dari rendah '0' ke tinggi, akan me-*reset* mikrokontroller menuju alamat 0000H.

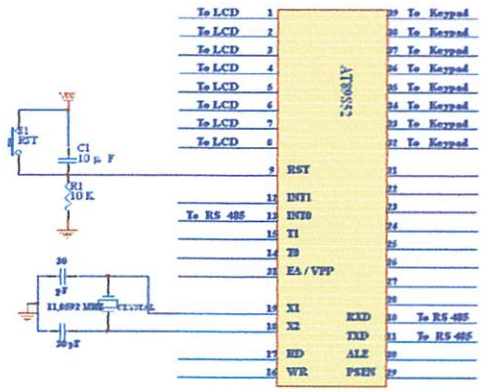
Pin *reset* dihubungkan dengan rangkaian *power-on reset pin* 9 MCS52. Pin RST harus diberi logika tinggi selama sekurangnya-sekurangnya (minimal) dua siklus mesin (24 periode oscilator), untuk membangkitkan sinyal reset. Sebuah kapasitor dihubungkan dengan V_{CC} dan resistor dihubungkan dengan *Ground*, diantara kapasitor dipasang sebuah saklar *push on* untuk membangkitkan sinyal reset secara manual. Rangkaian reset ditunjukkan dalam gambar berikut.



Gambar 3.3 Rangkaian Reset

Pemberian catu daya pada mikrokontroller tanpa suatu sinyal *reset* dapat menyebabkan mikrokontroller memulai eksekusi instruksinya dari lokasi yang tak menentu. Ini di sebabkan karena *Program Counter* tidak terinisialisasi.

3.2.4. Konfigurasi Kaki Mikrokontroller AT89S52



Gambar 3.4 Minimum Sistem AT89S52

Untuk mengakses memori *eksternal* digunakan sinyal kontrol RD, WR, ALE, PSEN dan EA. Sinyal-sinyal tersebut untuk mengontrol proses pemindahan data mikrokontroler. Penggunaan fungsi port-port mikrokontroleri adalah sebagai berikut:

1. Port 0
   - ✓ Port 0.0 s/d Port 0.7 digunakan sebagai masukan data *keypad matriks.*
2. Port 1
   - ✓ Port 1.0 s/d Port 1.7 dihubungkan dengan data kolom 74LS164 Ic *Shift register* yang terhubung dengan data baris LCD dalam proses *scanning.*
3. Port 3.0
   - ✓ Port 3.0 (RXD) kaki pin 10 digunakan sebagai *modem* untuk data sudah diterima dari RS 485.
   - ✓ Port 3.1 (TXD) kaki pin 11 digunakan sebagai *modem* data dikirim dari mikrokontroler ke MAX 232 komputer.
   - ✓ Port 3.4 s/d 3.7. digunakan sebagai kontrol sinyal, tombol penjawab (A,B,C,D).

4. Pin 20

   ✓ Pin 20 (GND) dihubungkan dengan ground.

5. Pin 40 VCC

   ✓ Digunakan sebagai sumber tegangan sebesar +5V.

6. Pin 30

   ✓ Sinyal ALE berfungsi untuk memisahkan *bit-bit* data dan *bit-bit* alamat rendah yang *dimultipleks* pada *port* 0.

7. Pin 31

   ✓ Sinyal EA, untuk memori eksternal diakses mulai alamat 0000H sampai FFFFH.

8. Kaki pin 18

   ✓ (XTAL 2) dan kaki pin (XTAL 1) untuk memberikan *clock inputan* yang dibutuhkan oleh mikrokontroler AT89S52.

9. Kaki pin 9

   ✓ Sebagai inputan rangkaian *Reset* untuk mereset *hardware.*

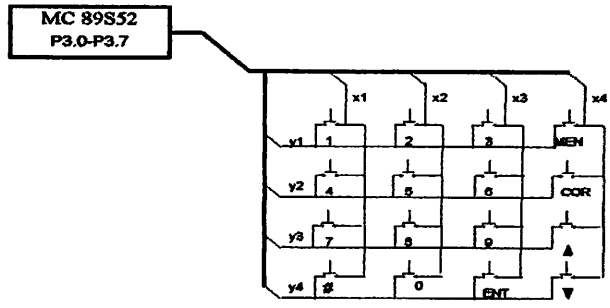
3.3. Perancangan Rangkaian *Keypad*

Keypad matriks 4x4 yang digunakan untuk memasukan identitas peserta *toefl.* Terdiri dari angka 0 sampai 9. ditambah dengan CAN, ENTER, SEND, UP, dan DOWN.

Adapun cara kerja *keypad* yang direncanakan dapat dijelaskan sebagai berikut:

- Setiap kali penekanan tombol akan terjadi suatu persilangan antara baris (X) dengan kolom (Y). Kondisi *logic* dihubungkan pada *port* input (P3.0 – P3.7) mikrokontroler AT89S52.

- Hasil *scanning* data *keypad* sementara disimpan *dimemory internal* mikrokontroller.



Gambar 3.5 Rangkaian *Encoder Keypad.*

Untuk *Scanning* data *keypad* terdapat penyesuaian data *valid* terhadap LCD, penekanan tombol akan terjadi suatu pengambilan data. Secara mekanis kaki keypad dihubungkan pada *port* input (P0.1–P0.7) mikrokontroller.

3.4. Perancangan Rangkaian Tombol Penjawab Soal.

Dalam perancangan rangkaian ini menggunakan rangkaian *push button.* Proses penekanan tombol penjawab dilakukan dengan proses *polling* terhadap empat buah tombol penjawab. Setiap kali penekanan tombol terjadi pengambilan data hasil penekanan tombol yang terhubung ke *port input* (P3.4–P3.7).

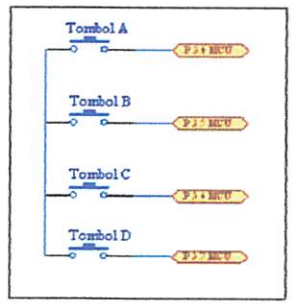
Pada proses *scanning* data tombol penjawab yang dihubungkan ke port 3 mikrokontroller memberikan input *logic* "1" jika terdapat penekanan sebaliknya jika tidak ditekan pada kondisi logic "0". Hasil *scanning,* data diinterfacekan melalui RS485 dan RS232 ke PC.

Secara umum dalam perancangan alat tombol tersebut yang dihubungkan pada port mikrokontroller sebagai:

1. Port 3.4 mikrokontroller dihubungkan dengan Tombol penjawab D

2. Port 3.5 mikrokontroller dihubungkan dengan Tombol penjawab C
3. Port 3.6 mikrokontroller yang dihubungkan dengan Tombol penjawab B
4. Port 3.7 mikrokontroller dihubungkan dengan Tombol penjawab A.

Tombol penjawab sebagai media penjawab soal, sistem kerjanya hampir menyamai keypad matriks, namun penggunaan tombol penjawab ini menerapkan sistem yang cukup murah dan efektif karena dirancang dan diatur sendiri sehingga penggunaan dapat dimaksimalkan tanpa banyak tombol. penjelasan rangkaian tombol penjawab pada gambar dibawah:



Gambar 3-6 Rangkaian Tombol Penjawab Soal

3.5. Perancangan Rangkaian LCD

LCD (*Liquid Crystal Display* jenis TM162ABC yang merupakan LCD dua baris dengan tiap barisnya terdiri dari 16 karakter untuk huruf maupun angka. Yang terhubung dengan salah satu IC 74164 sebagai IC yang berfungsi mengatur aliran data mikro yang masuk ke LCD.

LCD ini membutuhkan sinyal kontrol yang terdiri atas:

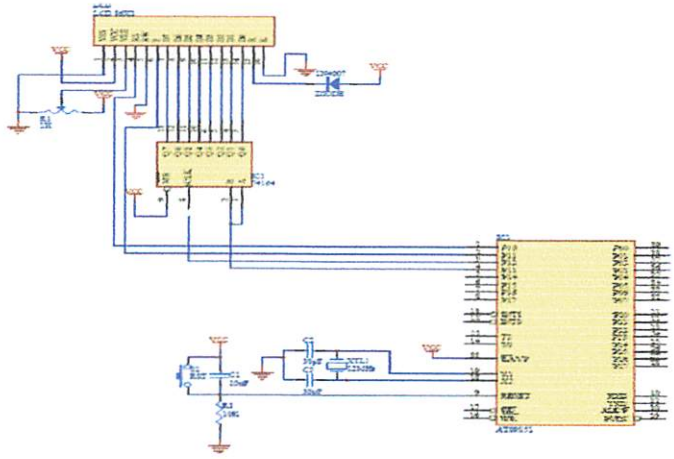
- R/W (*read/write*) untuk menentukan apakah data akan dibaca atau ditulis.
- Penyemat *Enable* merupakan kontrol saluran data (data *bus*) dihubungkan ke port 0 mikrokontroler sehingga mengaktifkan data tulis atau baca.
- RS (*Register Select*) untuk memilih register yang diakses.

- Penyemat DB0-DB7 dihubungkan ke pin data IC 75LS176 *(Sheef Register)* digunakan menampilkan karakter yang dikehendaki oleh mikrokontroler.

Adapun fungsi dari pin-pin LCD dalam menerima data dari mikrokontroler sebagai berikut:

- Untuk pin Vcc pada LCD dihubungkan ke supply +Vcc dan Vss dihubungkan ke *ground.*
- pin Vcc dihubungkan dengan tegangan +5volt.
- Pin V_{EE} dan Vss dihubungkan ke *trimer potensio* atau *trimpot* digunakan untuk mengatur kontras dari tampilan LCD dengan cara mengubah tegangan pada pin V_{EE}
- Pin R/W dihubungkan ke *ground* selalu berlogika 0, karena dalam operasi tulis dan pin RS dihubungkan ke pin A0 sistem mikrokontroler.
- Kaki 1 (GND) : Kaki tersebut dihubungkan dengan tegangan +5 volt yang merupakan sumber daya dari M1632 yang dihubungkan dengan VCC.
- Kaki 2 (VCC) : Kaki yang dihubungkan dengan tegangan 0 volt
- Kaki 3 (VEE/VLCD) : Tegangan pengatur kontras LCD yang mencapai nilai maksimum pada saat kondisi level tegangan 0 volt.
- Kaki 4 (RS) : Untuk Register Select, yang akan di akses ke register data.
- Kaki 5 (R/W): Logika ini menunjukan bahwa LCD sedang pada mode pembacaan dan logika 0 pada proses mode penulisan.
- Kaki 6 (E) : *Enable Clock LCD,* kaki ini mengaktifkan clock LCD dengan logika 1 pada kaki ini diberikan pada saat penulisan

- Kaki 7-14 (D0-D7) : Data Bus adalah aliran data sebanyak 4 bit ataupun 8 bit mengalir pada saat proses penulisan maupun pembacaan data.
- Kaki 15 (Anoda) : Berfungsi untuk tegangan positif dari *backlight* modul LCD sekitar 4,5 volt
- Kaki 16 (Katoda) : Tegangan negatif *backlight* modul LCD sebesar 0 volt
- pin E. Dimana pin E ini dari *address* dekoder dan perintah *write* mikrokontroler ketika terdapat data jalur data ditahan dengan memberikan *clock* pin E pada LCD.

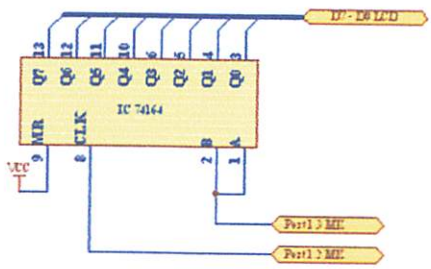


Gambar 3.7 *Liquid Crystal Display* (LCD)

3.5.1. Rangkaian Register Geser pada LCD

Register (*shift register*) merupakan memori sementara yang dapat dipindahkan dengan jalan menggeser data dari tingkat bit rendah ke yang lebih tinggi. Register geser dengan masukan seri dan keluaran parallel 8 bit dengan tipe IC 74LS164, berfungsi untuk mengubah data serial dari mikrokontroller menjadi data pararel yang akan bergeser pada tiap bit-nya seiring dengan diberikannya pulsa clock. Bit-bit akan terus bergeser kekanan dan data tersebut akan low "0"

semua ketika pulsa *clear* diberikan. Register geser yang tedapat pada LCD akan menggeser setiap data yang masuk ke LCD, register geser akan menggeser data pada tiap bitnya untuk selanjutnya data akan tampilkan ke layar LCD.



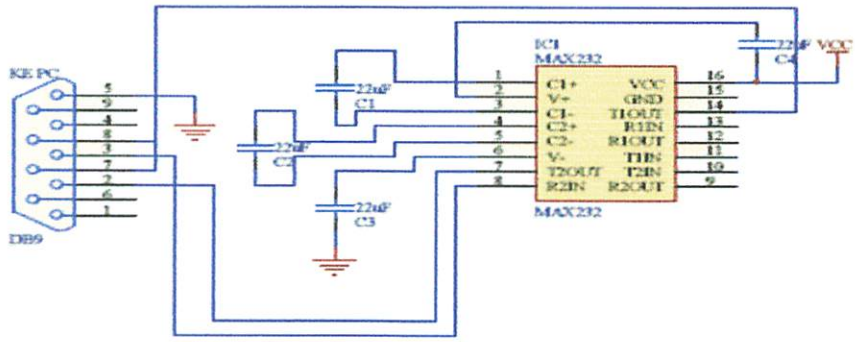
Gambar 3.8 Rangkaian Penggeser Data

Sumber : *Data sheet*

3.6. PERANCANGAN RANGKAIAN SERIAL RS 232

IC MAX232 mempunyai 2 *receivers* yang berfungsi sebagai pengubah level tegangan dari level RS232 ke level *Transistor Logic* (TTL) dan mempunyai 2 *drivers* yang berfungsi mengubah level tegangan dari level TTL ke level RS232. Pasangan *driver*/receiver ini digunakan untuk *TX* dan *RX* , sedangkan pasangan yang lainnya digunakan untuk *CTS* dan *RTS*.

Dalam pembuatan rangkaian, IC MAX232 memerlukan beberapa kapasitor. Besar nilai kapaistor yang digunakan sebesar 22 µF dengan tegangan 16 Volt pada beberapa kaki pin. IC ini memerlukan input +5 Volt.



Gambar 3.9. Rangkaian Serial RS232[5]

Fungsi pin RS232 sebagai berikut:

a. Pin 7 (T2OUT) – 8 (R2IN) dihubungkan dengan pin 2 – 3 DB 9 digunakan sebagai transfer data serial.

b. Pin 14 (T1OUT) dihubungkan dengan pin 7 DB9 difungsikan sebagai jalur permintaan data di aktifkan pada PC.

c. Pin 2 – 16 dihubungkan dengan tegangan VCC.

d. Pin 1 (+) dengan pin 3 (-), pin 4 (+) dengan pin 5 (-) dihubungkan dengan kapasitor 22 µF.

e. Untuk pin 6, karena bertegangan -10 Volt maka terhubung dengan kaki kapasitor (-) sedangkan *Ground* (+).

f. Pin 10 (T2IN) dihubungkan dengan pin 4 (DI) RS485 sebagai jalur data serial.

g. Pin 11 T1IN) dihubungkan dengan pin 2-3 (DE) RS485 sebagai jalur data serial.

Dalam sistem transmisi data menggunakan baud rate 9600 bps (9,6 KHz) bps dengan menggunakan f_{osc} = 11,0592 MHz , TH1 pada timer 1 yang dimasukkan adalah 253 d atau 0xFDH maka:

$$\text{Baudrate} = \frac{2^{SMOD}}{32} \times \frac{\text{Frequensi Osilator}}{12\,[256-(TH1)]}$$

$$9600 \text{ bps} = \frac{2^1}{32} \times \frac{11{,}0592.10^6}{12\,[256-(TH1)]}$$

$$[256-(TH1)] = \frac{2^1}{32} \times \frac{11{,}0592.10^6}{12 \times 9600}$$

$$[256-(TH1)] = \frac{2^1}{32} \times \frac{11{,}0592.10^6}{12 \times 9600}$$

$$[256-(TH1)] = 3$$

$$TH1 = 256-3$$

$$TH1 = 253 \text{ atau } 0FDH$$

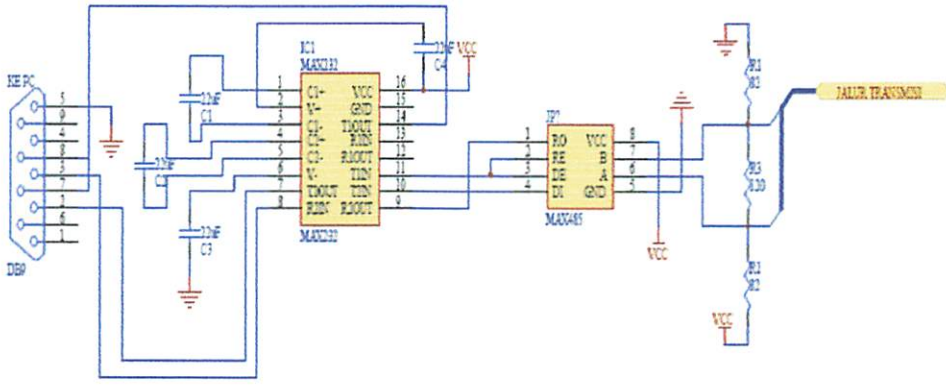
Penggunaan fungsi Pin pada DB9 yaitu :

- Pin 5 dihubungkan dengan ground.
- Pin 2 (*ReceiverData)* dihubungkan dengan Pin 7 (T2 Out) dari RS232.
- Pin 3 (*TransmitterData*) dihubungkan dengan pin 8 (R2in) dengan RS232 ini dilakukan supaya pengiriman data dari mikrokontroler dapat diterima komputer.
- Pin 7 (*Request To Send*) yang dihubungkan dengan pin 13 (T1in) untuk pengaturan permintaan pengiriman atau tidak.
- Pin 8 (*Clear To Send*) dihubungkan dengan RTS berfungsi sebagai sinyal yang dikirimkan DCE untuk memberitahukan kepada PC bahwa data boleh dikirim.

3.6.1. Konverter RS-232 ke RS-485

Pada komputer hanya tersedia port komunikasi serial RS-232 sehingga untuk mengubah tegangan RS-232 menjadi RS-485 diperlukan sebuah rangkaian yang mengubah level tegangan, rangkaian tesebut dirancang atas dua buah IC

yaitu Max-232 dan IC Max 485. IC Max 232 berfungsi mengubah level tegangan RS-232 menjadi level tegangan TTL. Rangkaian terlihat pada gambar dibawah:



Gambar 3.10. Perancangan Rangkaian konverter RS-232 ke RS-485.

Konverter RS-232 ke RS 485 dan apabila terdapat beda tegangan masukan (VaB) dan ±200 mV (Va lebih positif dari Vb), maka dalam port penerima (Receiver) RS 485 akan berlogika "1". Sebaliknya jika beda tegangan VAB ≤ 200 mV maka (Va lebih negatif dari Vb), sehingga port penerima (*Receiver*) akan berlogika "0".

untuk pin DE/RE yang dihubungkan singkat berfungsi sebagai pin pengendali kapan IC Max-485 mengirim (Receiver) dan menerima data (Driver). Jika pin DE/RE diberikan logika "1", maka akan berfungsi sebagai pengirim data sebaliknya jika pin DE/RE diberikan logika rendah maka akan berfungsi sebagai penerima data (Receiver) pemberian berlogika dikeluarkan melalui perangkat lunak. Jika pin GE diberi logika 1 maka akan berfungsi sebagai penerima data (*Transmitter*).

3.7. Perancangan dan pembuatan Perangkat lunak

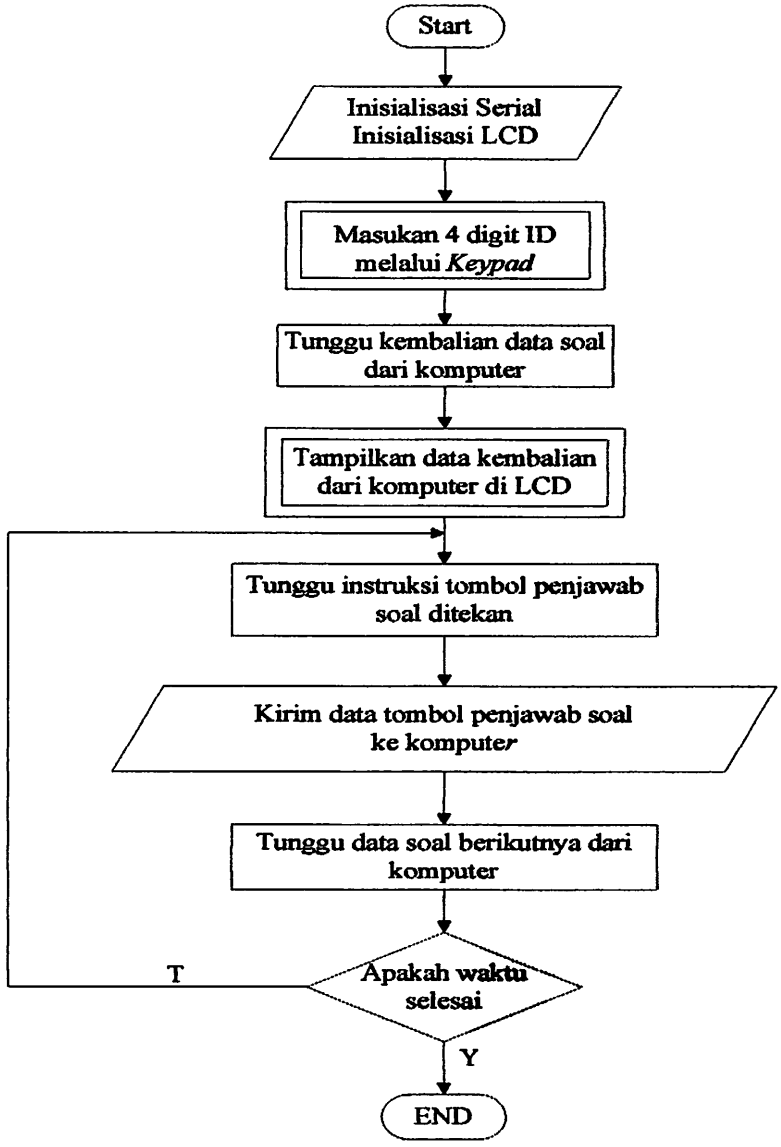
Pembuatan perangkat lunak alat test *toefl* berbasis PC berdasarkan pada pengendali mikrokontroler AT89S52. Untuk mendukung agar perangkat keras berfungsi sesuai dengan perancangan, maka diperlukan perangkat lunak sebagai penunjang. Perancangan *Software* disini mengunakan bahasa *pemrograman.*

- Bahasa C yang merupakan serangkaian perintah/simbol yang didefinisikan program, Variabel/Konstanta, atau operator yang diakhiri dengan tanda (;). Program dengan bahasa C digunakan menjalankan beberapa perintah dari mikrokontroler.
- Program untuk *Database* yakni menggunakan sub-*pemrograman Delphi* yang digunakan untuk menyusun aplikasi berdasarkan pada *pemrograman* bahasa *pascal* dan bekerja dalam lingkungan sistem operasi *Windows* Seperti kotak dialog (*dialog box*), tombol (*button, menu*) dan lain sebagainya.

Komunikasi antara komputer (PC) dengan hardware diperlukan suatu software pendukung, digunakan bahasa *pemrograman Borland Delphi* 7. Software yang dibuat ini bisa berkomunikasi dengan perangkat dari luar, software ini digunakan untuk memberi instruksi pada hardware dan untuk menyimpan data dalam *database,* dari data hasil yang telah diinputkan ke dalam PC.

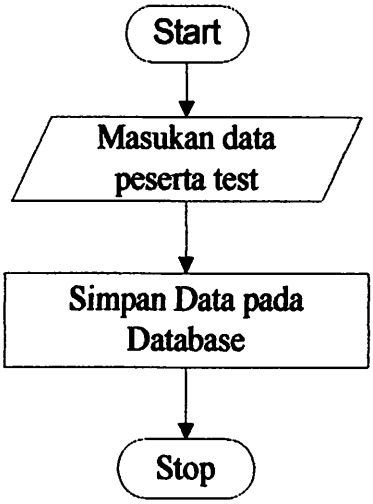
3.7.1. *Flowchart* Program Utama

Perancangan *Flowchart* disini menggunakan penjelasan system kerja secara umum termasuk mikrokontroler AT89S52. *Software* ini disini akan memegang peranan penting mengatur aliran data mikrokontroller sebagai pengendali utama sistem. Berikut penjelasan mengenai *flowchart* mikrokontroller. *Flowchart program* utama pada Mikrokontroller.

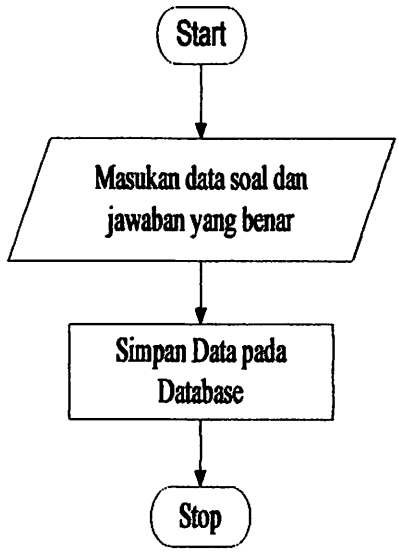


Gambar 3.11 *Flowchart* Program Utama

Flowchart dibawah ini menjelaskan penjabaran dari *program* utama pada mikrokontroller sesuai dengan urutan yang dilakukan:



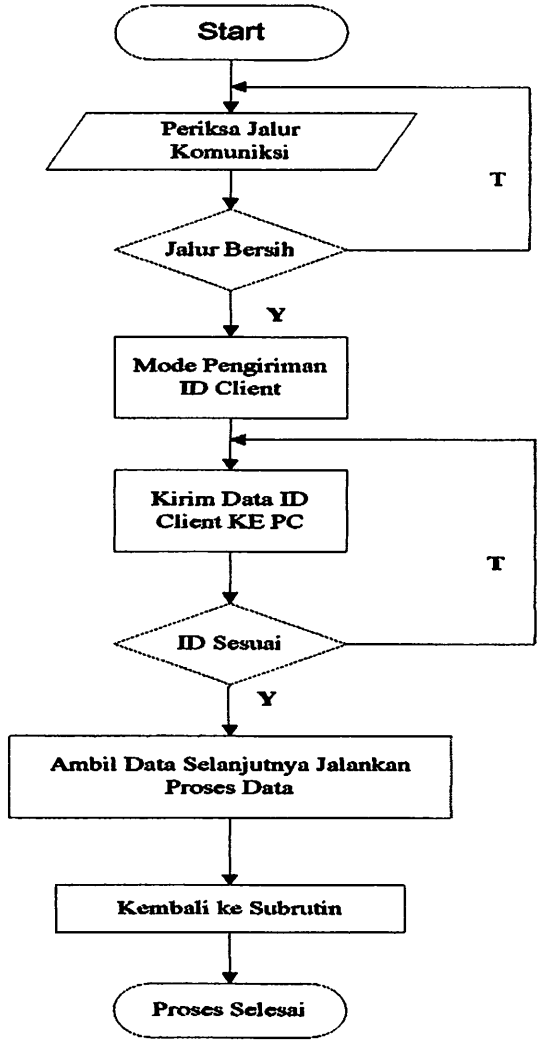
Gambar 3.12. *Flowchart Software Delphi* ID Client



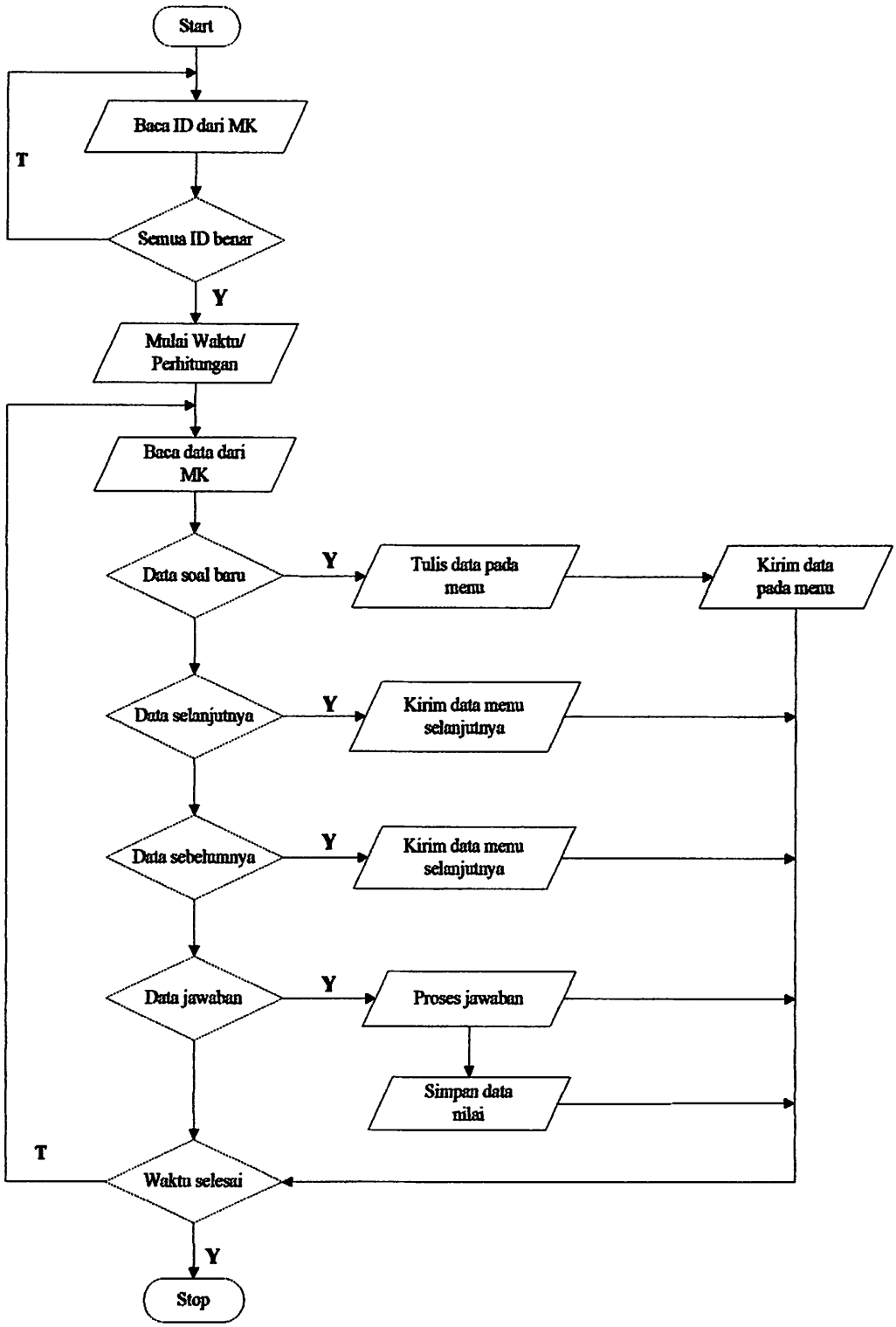
Gambar 3.13. *Flowchart Software Delphi* pada sistem soal 1.

3.7.2. *Flowchar Software* Komunikasi secara serial konverter

Agar komunikasi data pada sistem multipoint yang digunakan pada komunikasi RS-485 dan RS232 berada pada posisi mengirimkan jalur data jika kondisi jalur komuniksi data tersebut tidak sibuk/data tidak dalam keadaan tidak jalan. Komunikasi ini menggunakan jalur data untuk jarak komunikasi terhadap PC mengirim ID slave dan data soal *toefl*. Apabila jalur masih sibuk, maka pengiriman data harus menunggu hingga jalur sepi.



Gambar 3.14 Flowchart Pengiriman Data



Gambar 3.16. *Flowchart Data Base* pada sistem soal 2.

BAB IV

PENGUJIAN DAN ANALISA

4.1 Tujuan

Dalam skripsi ini dilakukan dua macam pengujian, yaitu pengujian *database* dan perangkat keras. Tujuan umum dari pengujian ini adalah untuk mengetahui kinerja yang berupa kehandalan dan ketepatan eksekusi antara program dengan modul yang telah dibuat. Sehingga akan diperoleh kesimpulan apakah program yang dibuat dapat mengontrol sistem yang ada.

4.1.1 Pengujian Perangkat Keras

4.1.2 Tujuan pengujian

Tujuan pengujian hardware adalah untuk mengetahui keadaan masukan atau keluaran dari tiap blok rangkaian yang direncanakan, sehingga dengan pengujian ini dapat diketahui apakah alat yang direncanakan dapat berfungsi dengan baik dan sesuai dengan yang diharapkan atau tidak. Tahap pengujian dilakukan dengan urutan rangkaian sebagai berikut:

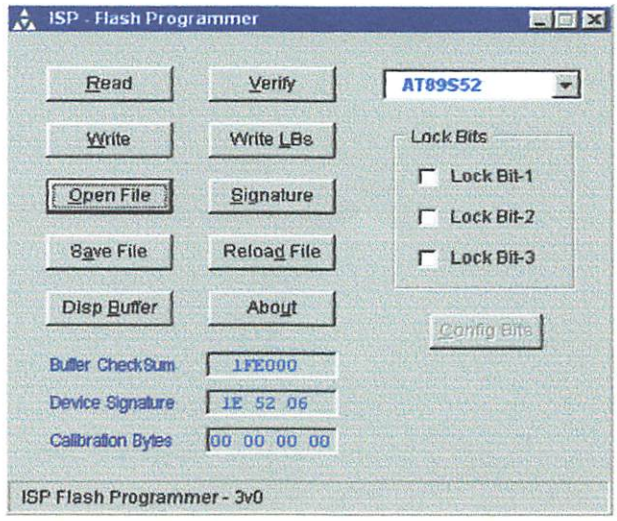
1. Pengujian Rangkaian Rangkaian *Mikrokontroler AT89S52*
2. Pengujian Rangkaian *LCD*
3. Pengujian Rangkaian *Keypad 4x4*
4. Pengujian Rangkaian Tombol Penjawab Soal
5. Pengujian Rangkaian *Serial* RS-232 dan *Transceiver* RS485 (SN75176).
6. Pengujian Keseluruhan Sistem

Peralatan Yang Digunakan meliputi:

1. Rangkaian Sistem alat
2. Catu daya +5V.
3. Multimeter.
4. Komputer.
5. Osciloskop.

4.1.3. Prosedur Pengujian Download Flash Program MK AT89S52

Prosedur pengujian Mikro AT89S52 yakni pengujian sistem pengiriman data secara serial berekstensi *dot hex*. Jenis *Software* yang dipakai ialah menggunakan ***ISP-Flash Programmer Version* 3.0a** yang merupakan keluaran dari *ATMEL* Berikut merupakan tampilan software downloader ***ISP – Flash Programmer Version* 3.0a.**



Gambar 4.1 Tampilan Menu Utama ISP Flash Programmer.

Keterangan :

- *Read* (baca) dan *Write* (tulis) file Hexa ke *mikrokontroller*.

- *Read Signature,* untuk mengunci bit.
- *Clear* dan *Fill,* untuk mengoso*ng*kan dan mengisi kembali memori pada *buffer.*
- *Verify,* untuk mem-verifikasi memori pada *buffer*
- *Reload,* untuk mengisi kembali *mikrokontroller* dengan program yang terakhir kali di-*download*-kan.
- *Display Buffer,* digunakan untuk pengecekan dan tampilan isi pada *buffer*
- *Auto Detection of Hardware,* untuk mendeteksi perangkat keras sistem minimum AT89S52.

4.1.4. Pengujian Rangkaian *Reset* Mikrokontroller

Pengujian rangkaian *reset* bertujuan untuk mengukur tegangan *reset* pada saat *reset* berkondisi *High* dan pada saat *reset* berkondisi *Low*. *Multitester*. Pengetesan ini dilakukan dengan cara tester (-) dari *Multitester* dihubungkan ke ground dan tester (+) dihubungkan pada Pin 9 dari AT89S52. ternyata hasil dari pengukurannya sebagai berikut.

Tabel 4.1 Hasil Pengukuran Rangkaian *Reset*

Reset	**Tegangan**
High	4,89 *Volt*
Low	0,2 *Volt*

Analisa hasil pengujian:

Dari pengujian ini diperoleh hasil yang sesuai dengan *data sheet*, bahwa AT89S52 pada saat di*reset* akan berkondisi Aktif *High.*

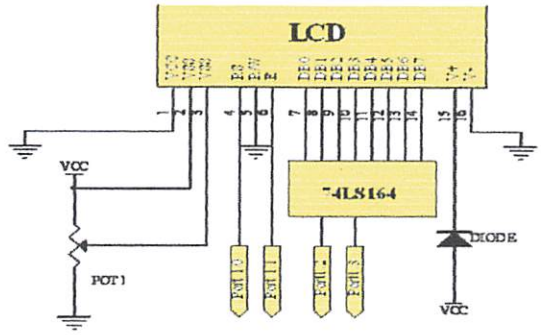
4.2 Pengujian Rangkaian LCD(*Liquid Crystal Display*)

A. Tujuan pengujian antara lain untuk mengetahui kemampuan rangkaian tampilan yang sudah yang direncanakan untuk menampilkan data inputan keypad.

B. Peralatan Yang Digunakan

1. LCD (*Liquid Crystal Display*).
2. Mikrokontroler AT89S52.
3. Perangkat lunak pengujian LCD.
4. *Downloader* mikrokontroler AT89S52
5. Catu daya.

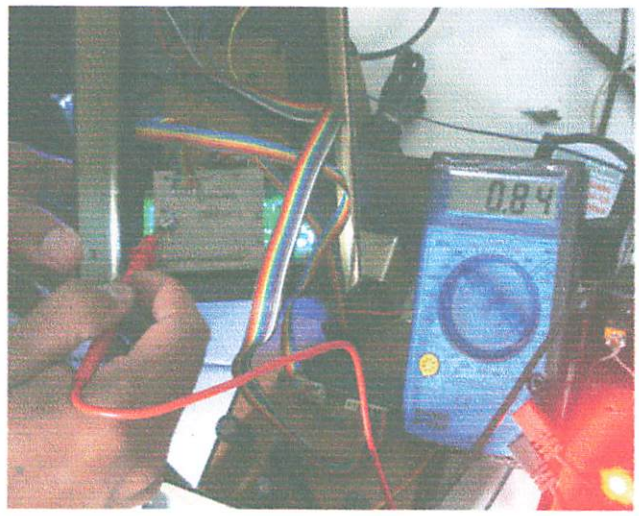
C. Rangkaian Pengujian



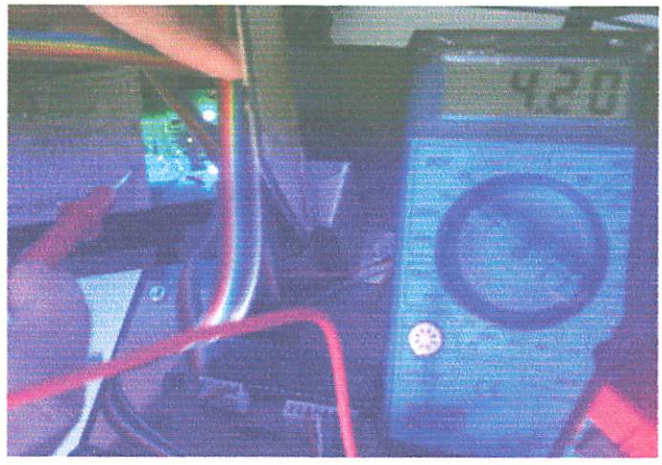
Gambar 4.2 Rangkaian pengujian LCD.

D. Prosedur pengujian

1. Membuat perangkat lunak untuk pengujian LCD, melakukan *compiling* dan mengisikan *program* ke mikrokontroler AT89S52.
2. Menghidupkan catu daya.
3. Mengamati hasil pengujian LCD.



Gambar 4.3 Pengujian Tegangan VR yang masuk ke LCD.



Gambar 4.4 Pengukuran besar tegangan setelah Dioda

E. Analisa hasil pengujian LCD

Dari hasil pengujian tegangan pada LCD didapatkan nilai VR yang masuk ke LCD adalah 0,84 volt. Sedangkan pengukuran tegangan setelah dioda diperoleh sebesar 4,20 Volt. Dengan mengurangi nilai VCC dengan nilai VDD, maka didapatkan nilai V+BL sebesar 4,2 volt, sudah dapat menyalakan LCD.

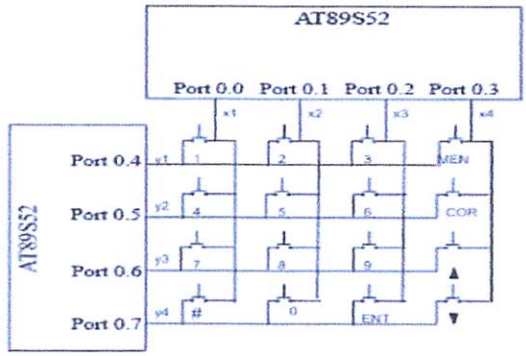
4.3 Pengujian Rangkaian Keypad 4X4

Pengujian ini bertujuan untuk mengetahui konfigurasi logika keluaran dari unit papan tombol saat tombol ditekan. Dalam proses *scanning* yang terjadi pada lajur baris dan kolom. Lajur baris merupakan bagian output sedangkan lajur kolom merupakan bagian input.

A. Peralatan yang digunakan antara lain:

1. Rangkaian *keypad* 4x4.
2. Sistem mikrokontroler dan LCD.
3. Perangkat lunak pengujian *keypad*
4. *Downloader* mikrokontroller.
5. Catu daya.

B. Rangkaian pengujian



Gambar 4.5. Diagram Pengujian Pengkode *Keypad.*

C. Prosedur pengujian

1. Menghubungkan rangkaian *keypad* ke mikrokontroler AT89S52.
2. Menjalankan program untuk pengujian *keypad.*
3. Memasukan 4 digit ID peserta test
4. Mengamati hasil pengujian

Gambar 4.6 Foto hasil pengujian rangkaian *keypad matriks.*

D. Analisa pengujian *keypad* meliputi:

Penekanan tombol angka 0 sampai 9 satu-per satu berfungsi menampilkan karakter data ditampilkan hasil secara langsung terlihat pada LCD berupa masukan *ID Client toef.* Dari tegangan yang diukur dari LCD disimpulkan LCD dapat bekerja pada *range* tegangan antara

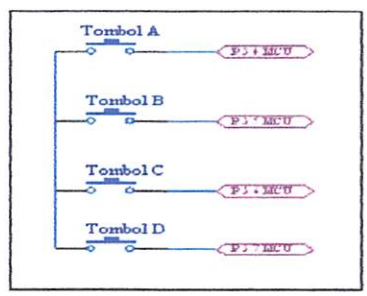
4.4. Pengujian Tombol penjawab Soal

Tujuan rancangan rangkaian yang digunakan dapat bekerja sebagaimana fungsinya data jawaban soal yang ditampilkan ke LCD dan selanjutnya ditampilka pada databse PC.

A. Peralatan Yang Digunakan meliputi:

1. Rangkaian Mikrokontroler
2. Rangkaian tombol penjawab
3. Catu daya +5V.
4. Multimeter.

B. Rangkaian Pengujian



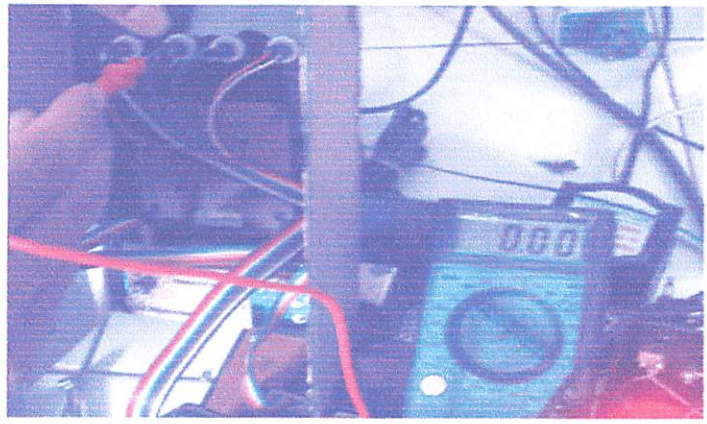
Gambar 4.7 Rangkaian pengujian tombol penjawab soal.

C. Prosedur pengujian

1. Menghubungkan rangkaian dengan rangkaian mikrokontroller AT 89S52
2. menghidupkan catu daya
3. mengukur keluaran tombol
4. mengamati hasil pengukuran

D. Pengukuran tegangan pada tombol penjawab soal *toefl*

Terlihat hasil pengukuran dari rangkaian tombol penjawab soal sebagai berikut:



Gambar 4.8 Foto pengukuran tegangan pada tombol penjawab soal ditekan.

Gambar 4.9 Foto pengukuran pada tombol penjawab soal dalam kondisi tombol tidak ditekan.

Analisa Hasil Pengujian

Dari hasil pengujian terdapat perbedaan kondisi tegangan pada saat tombol ditekan tegangan yang dihasilkan sebesar 0.00 Volt, sebaliknya jika tombol tidak ditekan menghasilkan tegangan keluaran sebesar 4.84 Volt, yang berarti sistem komunikasi data ke mikro secara langsung berjalan dengan baik.

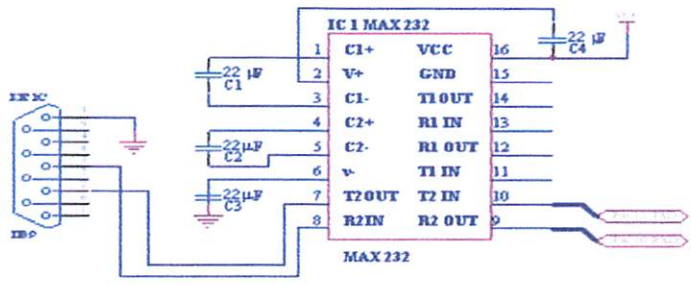
4.5. Pengujian Antarmuka Komunikasi Serial

Tujuan antara lain untuk mengetahui apakah antarmuka serial yang dibangun, telah bekerja dalam level tegangan TTL. RS232 dapat bekerja dengan baik sehingga pengiriman data dapat berjalan dengan baik diterima oleh PC sesuai dengan data yang dikirim oleh mikrokontroler.

A. Peralatan yang digunakan meliputi:

- Komputer
- Rangkaian Mikrokontroler AT 89S52
- Kabel serial DB9
- Multi meter digital
- Power supply

C. Rangkaian pengujian

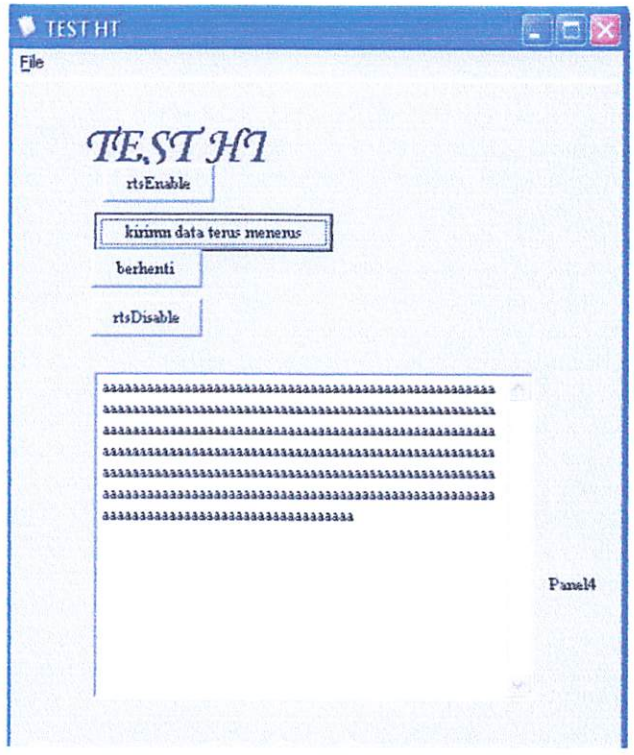


Gambar 4.10. Rangkaian pengujian komunikasi serial.

D. Langkah-langkah pengujian:

- Menghubungkan rangkaian RS232 dengan PC melalui *port serial* DB9.
- Memberikan catu daya pada rangkaian.
- Menghubungkan probe+multimeter dengan out+pada rangkaian
- Menghubungkan rangkaian pada catu daya sebagai sumber tegangan dan mengaktifkannya.
- Membuka aplikasi *Hyper Terminal* dan membuat koneksi baru melalui COM 1.
- Mengamati hasil keluaran dari RS232 di PC.
- Mengamati hasil pengukuran dari multimeter.

E. Pengujian pengiriman data serial



Gambar 4.11. Hasil data Percobaan serial yang diterima oleh PC

Pada transmisi data serial menentukan kecepatan *baudrate* sebesar 9600 Bps dengan frekuensi osilator kristal 11,0592Mhz. TH1 pada timer 1 yang dimasukkan adalah 253 d atau 0xFDH maka:

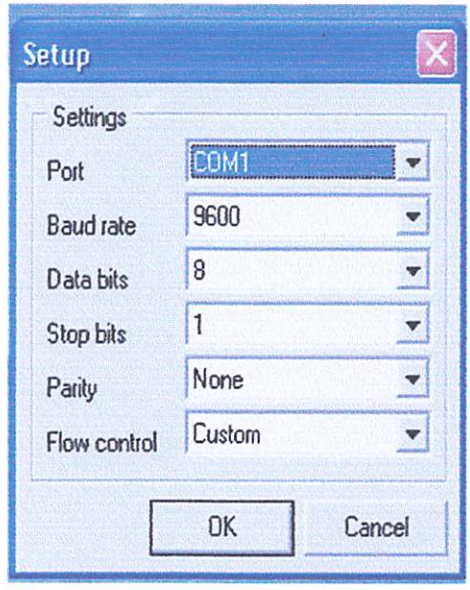
$$\text{Baudrate} = \frac{2^{SMOD}}{32} \times \frac{\text{Frequensi Osilator}}{12\,(256 - TH1)}$$

$$9600\ \text{bps} = \frac{2^{0}}{32} \times \frac{11{,}0592.10^{6}}{12\,(256 - TH1)}$$

$$[256-(TH1)] = \frac{1}{32} \times \frac{11{,}0592.10^{6}}{12 \times 96}$$

$$[256-(TH1)] = 3$$

$$TH1 = 256-3 = 253 \text{ atau } 0xFDH.$$

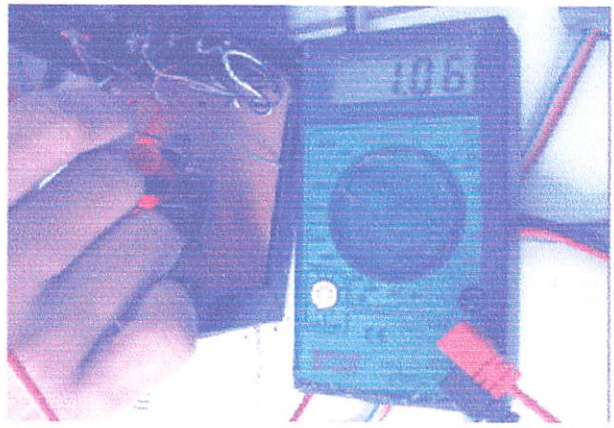


Gambar 4.12. Tampilan pengaturan *Baud Rate* transmisi data serial.

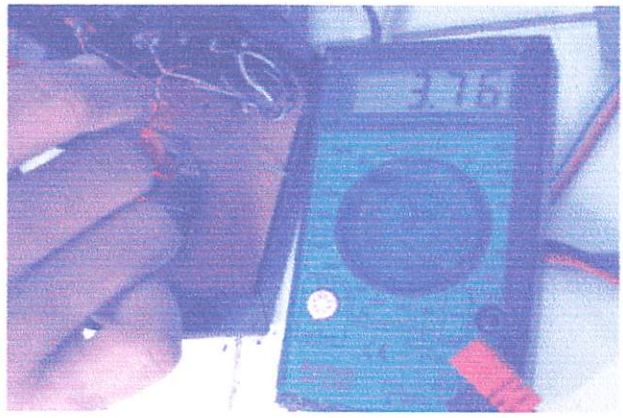
F. Tahap pengujian dan pengukuran

Pengujian tegangan keluaran *Test point* 1 menggunakan pengukuran dengan Avometer dilakukan untuk membandingkan besar tegangan jika pada saat terjadinya komunikasi data secara serial.

G. Pengukuran dengan multimeter digital



Gambar 4.13. Foto pengukuran untuk *Test Point 1A* sebelum komunikasi data serial.



Gambar 4.14. Foto hasil pengukuran untuk *Test Point 1B* sebelum komunikasi data serial.

H. Tabel hasil pengukuran untuk *test point* komunikasi data serial

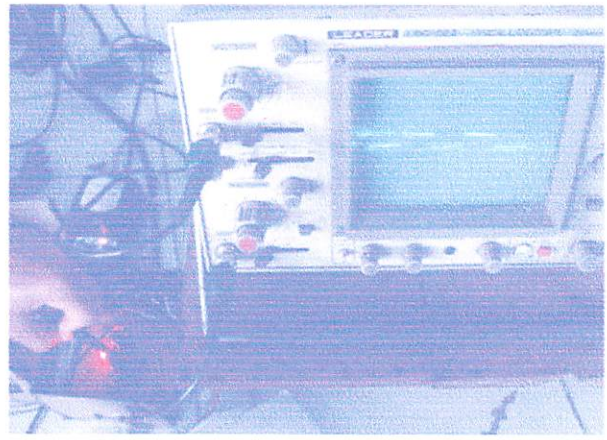
Tabel 4.2 Hasil Pengukuran *Output* RS232

Tx (Volt)	**Rx (Volt)**
Kondisi *high*	
5	3,76
Kondisi *low*	
0	1,06

I. Pengujian komunikasi data serial dengan Osiloskop

Untuk pengujian melalui *osiloskop* ini hanya diambil beberapa sample saja. Hasil dari pengujian ini yakni mengamati prosedur komunikasi data yang diterima/dikirim. Berikut keluaran sinyal keluaran tidak menunjukan adanya komunikasi data serial, dari hasil pengukuran menggunakan *osciloscope* adalah berikut:

Gambar 4.15. Foto Keluaran Gelombang TP1 A tidak ada data yang dikirim



Gambar 4.16. Foto keluaran gelombang TP 1 B tidak ada data yang dikirim

Keluaran pada TP1-A dan TP1- B pada saat terdapat pengiriman data berikut:

V/Div = 2 Volt

T/Div = 1 ms

Analisa hasil pengujian

Pada jalur Tx dan Rx diberikan resistor *pull-up* sehingga jalur data bersifat *open drain*, maka dalam kondisi tidak ada data, jalur tersebut dalam keadaan high.

Dari hasil pengujian didapatkan logika high pada Rx dan Tx adalah 3,76 Volt dan logika low adalah 0 Volt. Mampu mentransfer data pada jalur komunikasi data serial antara mikro dengan PC berjalan dengan baik.

J. Pengujian Rangkaian RS 485

Gambar 4.17. Percobaan pengukuran tegangan pada RS485

L. Analisis hasil pengujian tegangan pada RS485

Menunjukan komunikasi data antara mikrokontroler dan komputer melalui jaringan standar RS-485 dan RS232 dapat berjalan dengan baik. Terlihat hasil pengukuran tegangan keluaran VCC.

4.6 Pengujian Secara Keseluruhan Sistem

Pengujian keseluruhan sistem dilakukan secara bertahap dan apabila tahap pertama belum berhasil maka pengujian berikutnya akan tertunda sampai pengujian tahap pertama selesai dilakukan, maka baik dari segi *hardware* maupun *software* harus siap dan dilakukan bertahap sehingga semua berjalan dengan baik serta dapat dianalisa kekurangan yang ada.

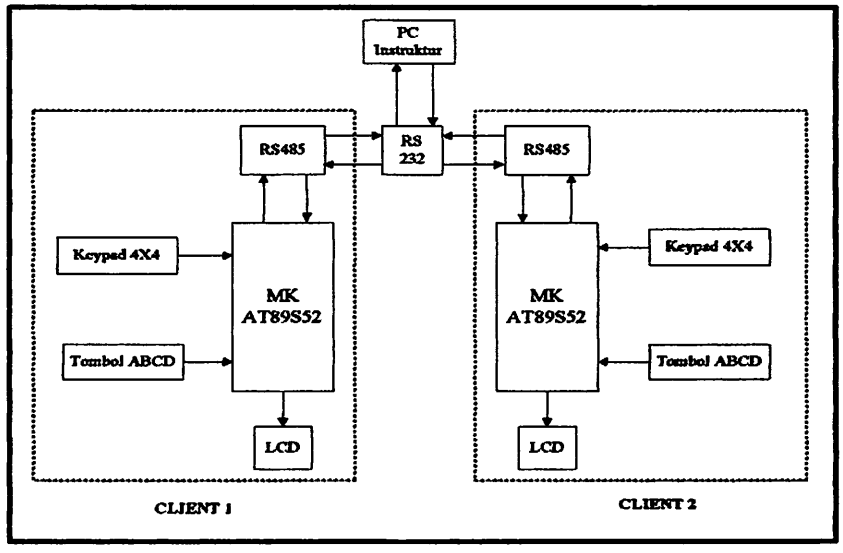
A. Tujuan Pengujian

Untuk membuktikan bahwa sistem yang dijalankan dapat bekerja dengan baik sesuai perancangan sistem alat.

B. Peralatan Yang Digunakan

- Personal Komputer (PC)
- Kabel Serial
- Rangkaian Sistem Alat Keseluruhan

C. Blok Diagram Prosedur Pengujian alat secara keseluruhan :



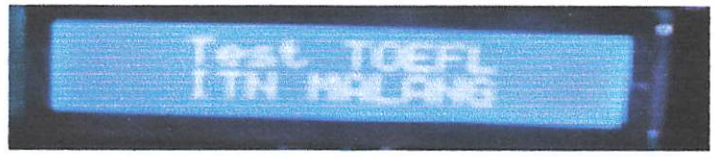
Gambar 4.18 Blok diagram prosedur pengujian sistem keseluruhan alat.

D. Prosedur Pengujian

- Hubungkan rangkaian sistem alat dengan komputer melalui kabel serial
- Menghidupkan catu daya.
- Aktifkan komputer dan rangkaian sistem *Test Toefl*
- *Database* dengan *software delphi* pada komputer
- Periksa tampilan pada LCD dan PC
- Uji coba sistem alat dengan menggunakan sistem berbasiskan komputer.

E. Hasil Pengujian

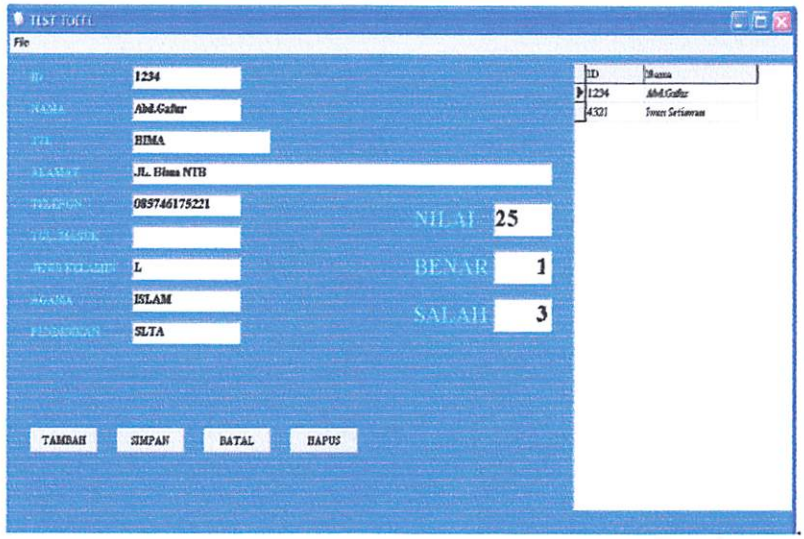
Dari pengujian keseluruhan sistem yang dilakukan dapat diperoleh hasil pengujian seperti tampilan *Test Toefl* pada LCD, saat alat dihidupkan pertama kali untuk memulai test dengan masukkan ID *Client* jika memulai *test toefl*



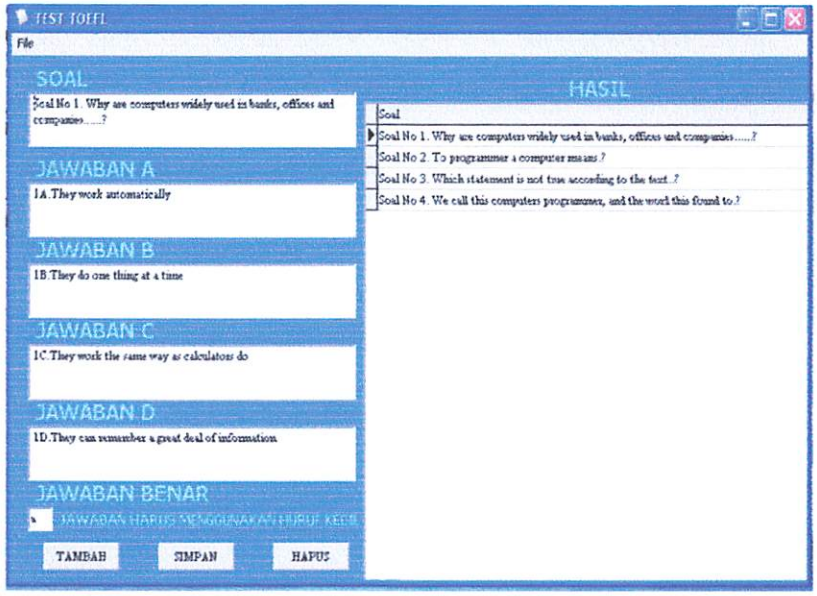
Gambar 4.19. Foto tampilan LCD awal masuk *test toefl*

Gambar 4.20. Foto tampilan ID *Client* di LCD

Gambar 4.21. Foto tampilan soal pada LCD



Gambar 4.22. Tampilan data *base client* pada saat memasukan (ID) *identitas Client*



Gambar 4.23. Tampilan hasil *database PC* pada pengujian keseluruhan sistem alat *test toefl.*

Analisa hasil pengujian keseluruhan sistem

Menunjukan hubungan jalur komunikasi data dari mikrokontroler ke *Personal Komputer* melalui jalur transfer data menggunakan serial (RS-485 dan RS-232), menunjukan hasil seperti yang terlihat pada hasil *database* diatas, bahwa komunikasi data serial mampu bekerja dengan baik pengiriman data serial.

BAB V

PENUTUP

5.1. Kesimpulan

Setelah melalui beberapa tahap pengujian memberikan gambaran mengenai unjuk kerja alat yang telah dibuat. Maka pengujian dan *analisis* diperoleh kesimpulan sebagai berikut :

- Pengujian dari rangkaian reset mikrokontroler yakni dengan frekuensi yang dihasilkan serta periode *clock* yang telah diketahui, maka akan memberikan siklus ke mikrokontroler untuk bekerja terus bekerja pada aktif *high* pada saat proses pengiriman data dengan sistem *pemrograman.*
- Hasil pengujian Rangkaian LCD, menunjukan hasil *scanning* LCD dapat beroperasi dengan baik pada saat sistem dijalankan, sebaliknya keypad yakni *scanning* data *ID* maupun soal *keypad* ditekan akan menghasilkan inputan pada LCD dengan sangat baik.
- Hubungan komunikasi serial antara data mikrokontroler dengan pengaturan *Baudrate* sebesar 9600bps, frekuensi osilator 11.0592 maka jumlah *error* pada pengiriman *data base* terhadap *Personal Komputer* dapat diperkecil, sehingga menunjukan tampilan *database* berjalan dengan baik.

5.2. SARAN

Dalam perencanaan dan pembuatan alat *toefl* ini masih dipelukan analisa sistem dengan pengembangan yang lebih lanjut guna kesempurnaan alat ini. Hal-hal tersebut ini antara lain :

1. Untuk mendapatkan peningkatan kinerja alat, yakni di implementasikan ke sistem Praktek Lab. Bahasa dengan sistem interaksi komunikasi antara peserta test dengan instruktur lebih ke sistem *listening*
2. Alat ini dapat di kembangkan lebih lanjut ke sistem ujian penerimaan mahasiswa baru di Institut Perguruan Tinggi.

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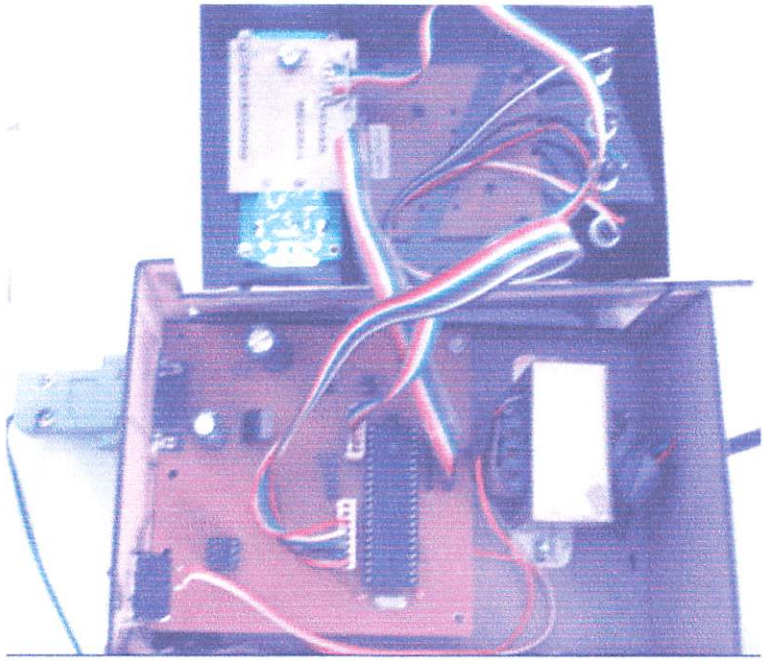
LAMPIRAN

FOTO ALAT *TEST TOEFL*

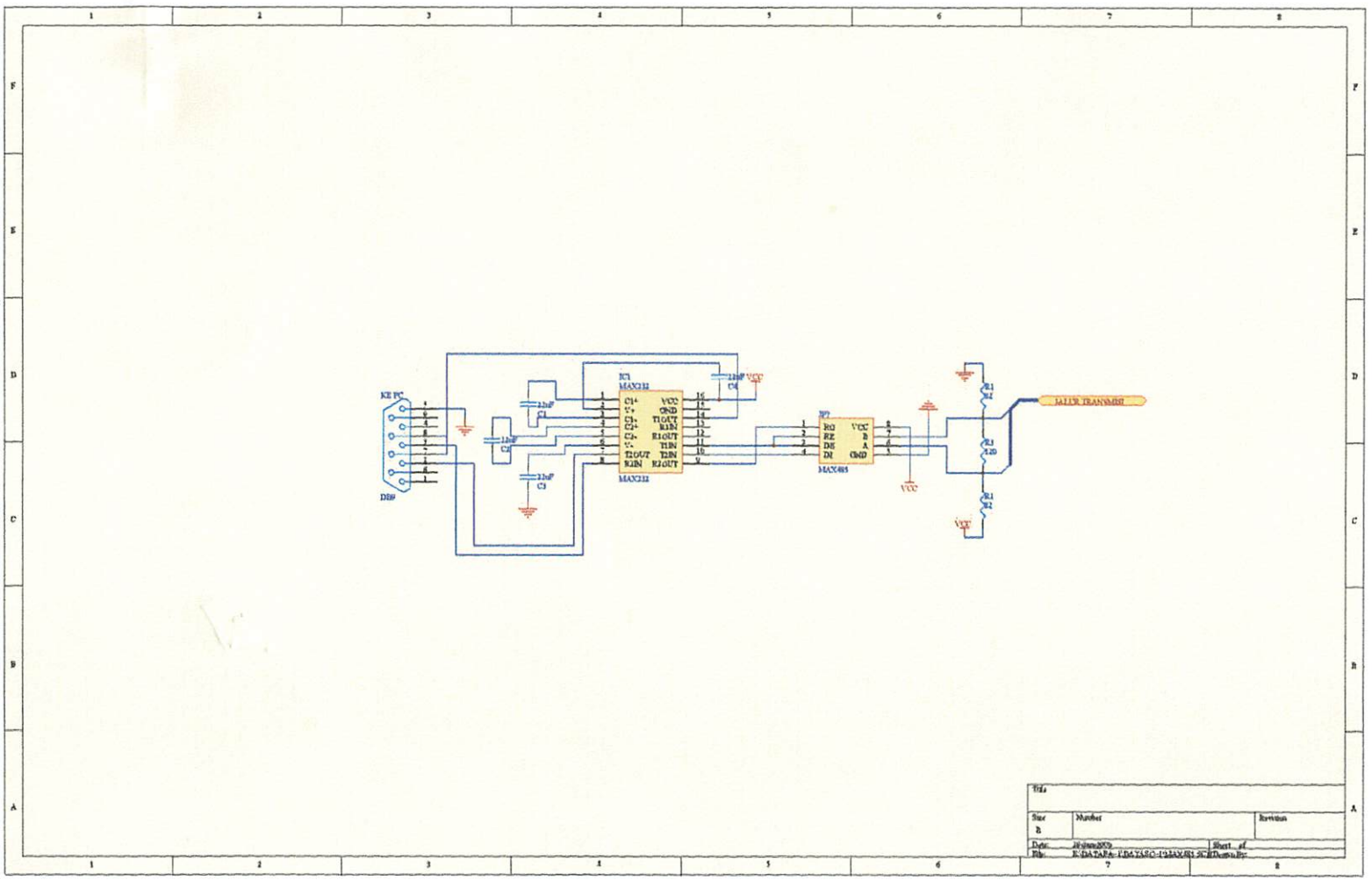
Gambar

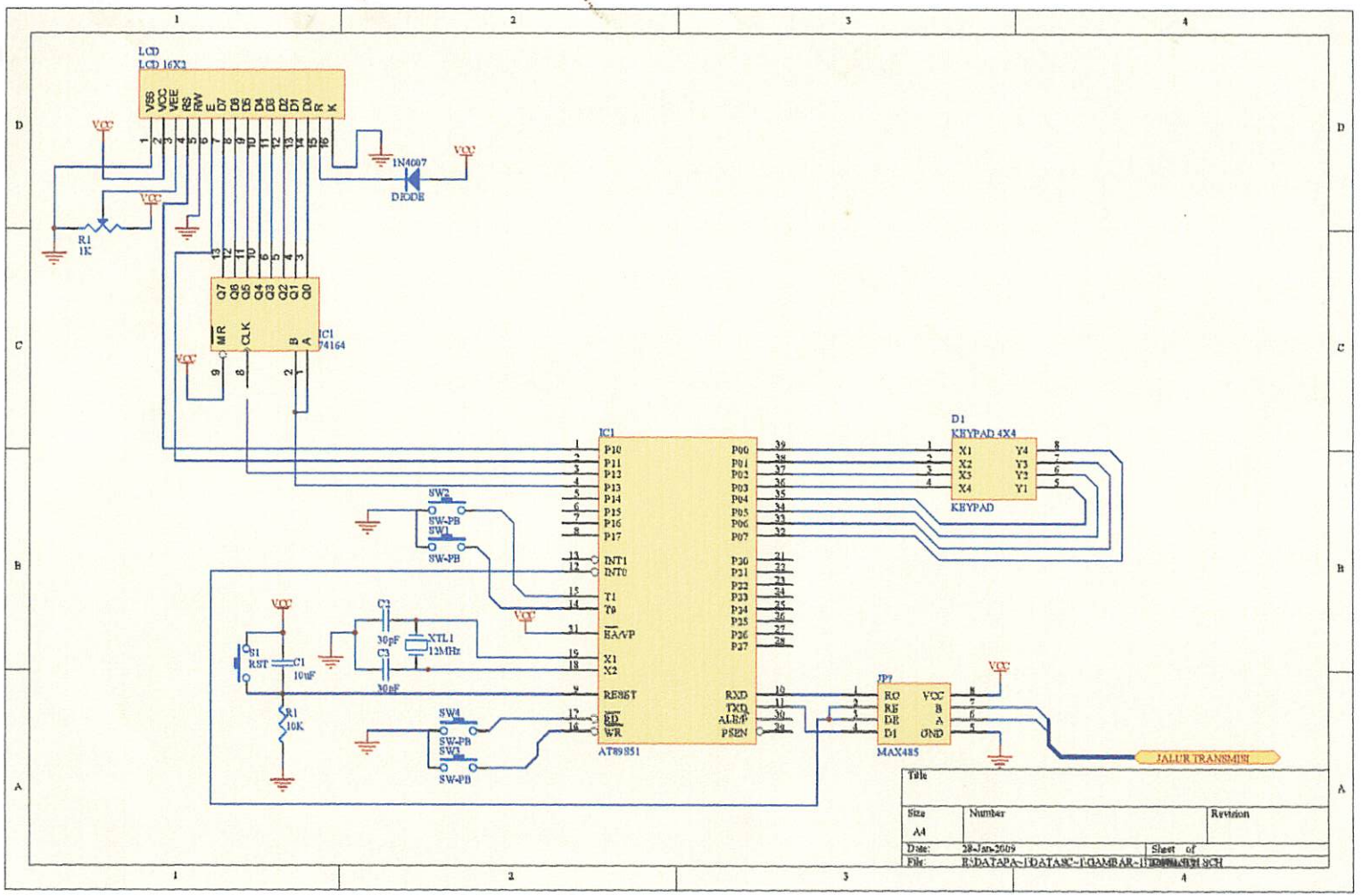
Foto Alat Tampak dari luar



Gambar

Foto Alat Tampak dari dalam


KE PC
DB9
C1
C2
C3
C4
IC1
MAX232
VCC
GND
T1OUT
R1IN
R1OUT
T1IN
T2OUT
T2IN
R2IN
R2OUT
MAX232
IC2
RO
RE
DE
DI
VCC
B
A
GND
MAX485
R1
R2
R3
VCC
VEE
TALUK TRANSMIT
Title
Size
B
Number
Revision
Date:
Sheet of
File:


LCD
LCD 16X2
VSS VCC VEE RS RW E D7 D6 D5 D4 D3 D2 D1 D0 R K
1N4007
DIODE
R1
1K
IC1
74164
Q7 Q6 Q5 Q4 Q3 Q2 Q1 Q0
MR CLK B A
IC1
AT89S51
P10 P11 P12 P13 P14 P15 P16 P17
P00 P01 P02 P03 P04 P05 P06 P07
P30 P31 P32 P33 P34 P35 P36 P37
INT1 INT0 T1 T0 EA/VP X1 X2 RESET RD WR
RXD TXD ALE/P PSEN
D1
KEYPAD 4X4
X1 X2 X3 X4 Y4 Y3 Y2 Y1
KEYPAD
SW2
SW1
SW4
SW3
SW-PB
C2
30pF
XTL1
12MHz
C3
30pF
S1
RST
C1
10uF
R1
10K
JP7
RO RE DE DI VCC B A GND
MAX485
JALUR TRANSMISI
Title
Size
A4
Number
Revision
Date:
28-Jan-2009
Sheet of
File:
R:\DATAPA~1\DATASC~1\GAMBAR~1\

INSTITUT TEKNOLOGI NASIONAL MALANG
FAKULTAS TEKNOLOGI INDUSTRI
JURUSAN TEKNIK ELEKTRO S-1
KONSENTRASI TEKNIK ELEKTRONIKA

FORMULIR PERBAIKAN SKRIPSI

Nama : ABDUL GAFUR

NIM : 02 17170

Masa Bimbingan : **19 Desember 2008 s/d 19 Juni 2009**

Judul : **"PERANCANGAN DAN PEMBUATAN ALAT PENJAWAB SOAL *TEST TOEFL MULTI CLIENT* BERBASIS *PERSONAL KOMPUTER"***

No.	Tanggal	MATERI PERBAIKAN	PARAF
1.	18 Maret 2009	BAB III Diperbaiki Susunanya	

Disetujui:

Penguji I

(M.Ibrahim Ashari,ST,MT)
NIP.P.1030100358

Penguji II

(Irmalia Suryani Faradisa,ST,MT)
NIP.P.1030100365

Mengetahui:

Dosen Pembimbing I

(Ir.Yusuf Ismail Nakhoda,MT)
NIP.Y.1018800189

Dosen Pembimbing II

(I.Komang Somawirata,ST,MT)
NIP.P.1030100361

INSTITUT TEKNOLOGI NASIONAL MALANG
FAKULTAS TEKNOLOGI INDUSTRI
JURUSAN TEKNIK ELEKTRO

Formulir Perbaikan Ujian Skripsi

Dalam pelaksanaan Ujian Skripsi Janjang Strata 1 Jurusan Teknik Elektro Konsentrasi T. Energi Listrik / T. Elektronika / T.Infokom, maka perlu adanya perbaikan skripsi untuk mahasiswa :

NAMA : ABDUL GOFUR
NIM : 0217170
Perbaikan meliputi :

Bab III diperbaiki sesuai usul

Malang, 18 - 03 2009

(Ir. Nalia ST.)

INSTITUT TEKNOLOGI NASIONAL
Jl. Raya Karanglo Km 2
MALANG

FORMULIR BIMBINGAN SKRIPSI

Nama : ABDUL GAFUR
NIM : 02.17.170
Masa Bimbingan : 19 Desember 2008 s/d 19 Juni 2009
Judul : **Perancangan dan Pembuatan Alat Penjawab Soal *Test Toefl Multi Client* Berbasis *Personal Komputer***

No	Tanggal	Uraian	Paraf
1	14-02-2009	Konsultasi laporan Bab II, teori dasar Mikrokontroller AT89S52	
2	17-02-2009	Revisi format penulisan laporan Bab II teori dasar	
3	24-02-2009	ACC Laporan Bab II	
4	27-02-2009	Konsultasi *Flowchart diagram* alir komunikasi data *serial interface RS232 dan RS485*	
5	04-03-2009	Konsultasi Bab III Perancangan alat	
6	09-03-2009	Perbaikan blok diagram alat, alur penjelasan diperjelas.	
7	11-03-2009	ACC perancangan format penulisan Bab III, rancangan rangkaian LCD	
8	14-03-2009	Konsultasi keseluruhan Bab II, Bab III, Bab IV	
9	15-03-2009	Analisa pengujian alat, foto alat, perjelas perhitungan keluaran serial *interface.*	
10	21-03-2009	ACC Semua Bab, Bab II, Bab III, Bab IV, Bab V	

Malang, Februari, 2009

Dosen Pembimbing I

Ir. Yusuf Ismail Nakhoda,MT
NIP. Y.1018800189

Form S-4a

INSTITUT TEKNOLOGI NASIONAL
Jl. Raya Karanglo Km 2
MALANG

FORMULIR BIMBINGAN SKRIPSI

Nama : ABDUL GAFUR
NIM : 02.17.170
Masa Bimbingan : 19 Desember 2008 s/d 19 Juni 2009
Judul : **Perancangan dan Pembuatan Alat Penjawab Soal *Test Toefl Multi Client* Berbasis *Personal Komputer***

No	Tanggal	Uraian	Paraf
1	10-02-2009	Konsultasi laporan bimbingan Bab II, Teori Dasar Mikrokontroller AT89S52	
2	14-02-2009	Perbaikan sistem komunikasi serial RS232-RS485 untuk komunikasi *data Base*	
3	16-02-2009	ACC Bab II, Teori dasar mikrokontroller hub komunikasi serial *database*	
4	19-02-2009	Konsultasi Bab III Perancangan Alat	
5	21-02-2009	Revisi Bimbingan laporan, pada perancangan Blok Digram sistem alat	
6	23-02-2009	ACC Perancangan alat dan *Flowchart* sistem keja mikrokontroler.	
7	25-02-2009	Revisi laporan Bab IV analisa sistem kerja *keypad*	
8	29-02-2009	ACC Bab III dan Bab IV perhitungan serial RS232	
9	10-03-2009	Revisi sistem kerja sesuaikan perancangan sistem alat terhadap LCD	
10	13-03-2009	ACC semua Bab II, Bab III, Bab IV, Bab V	

Malang, Februari, 2009
Dosen Pembimbing II

(I.Komang Somawirata,ST,MT)
NIP. 1030100361

Form S-4a

LAMPIRAN PROGRAM

LIsting program keseluruhan tofel delphi

```
unit Unit1;

interface

uses
  Windows, Messages, SysUtils, Variants, Classes, Graphics, Controls, Forms,
  Dialogs, DB, Menus, CPort, DBTables, Mask, DBCtrls, StdCtrls, Buttons,
  ComCtrls, Grids, DBGrids, ExtCtrls;

type
  TForm1 = class(TForm)
    ComPort1: TComPort;
    Button2: TButton;
    BKIRIM: TButton;
    Timer1: TTimer;
    Edit4: TEdit;
    TbID: TTable;
    etting1: TMenuItem;
    Utama1: TMenuItem;
    Button4: TButton;
    Edit3: TEdit;
    LID: TLabel;
    Memo1: TMemo;
    Memo2: TMemo;
    Notebook1: TNotebook;
    Label1: TLabel;
    Label2: TLabel;
    Label3: TLabel;
    Label4: TLabel;
    Label5: TLabel;
    Label6: TLabel;
    Label7: TLabel;
    MasukkanIdentitas1: TMenuItem;
    Button6: TButton;
    DBGrid1: TDBGrid;
    Label8: TLabel;
    DBGrid2: TDBGrid;
    DBGrid3: TDBGrid;
    Utama2: TMenuItem;
    RevisiSoal1: TMenuItem;
    Timer2: TTimer;
    Button10: TButton;
    Button12: TButton;
    WaktuUjian1: TMenuItem;
    procedure ComPort1RxChar(Sender: TObject; Count: Integer);
    procedure kirimData(data : String);
    procedure Button12Click(Sender: TObject);
    procedure WaktuUjian1Click(Sender: TObject);

    private
    { Private declarations }
  public
    { Public declarations }
  end;

var
  Form1: TForm1;
  id1,id2:string;
  SOAL1,SOAL2,baris1,baris2,NOMOR1,NOMOR2:integer;

implementation



{$R *.dfm}

procedure TForm1.kirimData(data : String);
var i:integer;
```

```
begin
//ShowMessage(data);
  ComPort1.FlowControl.ControlRTS:=rtsDisable;
  sleep(5);
  i:=0;
//  repeat
//  inc(i);
//  ComPort1.WriteStr(copy(data,i,1));
  ComPort1.WriteStr(DATA);
end;

procedure TForm1.ComPort1RxChar(Sender: TObject; Count: Integer);
var     data,no,buf: String;
    i,benar,salah,nilai:integer;
begin
Timer1.Enabled:=false;
ComPort1.ReadStr(data,count);
edit3.Text := data;
no:=copy(data,1,1);
IF POS('z',data)<>0 then
  begin
//  ShowMessage(COPY(data,3,pos('z',data)-3));
  if TbID.FindKey([COPY(data,3,pos('z',data)-3)])then
    begin
    kirimData('$'+no+'b');
    if no='1' then
      BEGIN
      TBSOAL.First;
      BSOAL.Next;
      until TBSOAL.Eof;

      SOAL1:=1;
      id1:=COPY(data,3,pos('z',data)-3);
      NOMOR1:=1;
      Memo1.Clear;
      TBSOAL.First;
      buf:=TBSOAL.fieldbyname('soal').AsString;
        REPEAT
        UNTIL length(buf)<=0;
      ines.ValueFromIndex[baris1]);
      END
    else
      BEGIN
      TBSOAL.First;
      repeat
      TBSOAL.Edit;
      until TBSOAL.Eof;

      SOAL2:=1;
      id2:=COPY(data,3,pos('z',data)-3);
      NOMOR1:=2;
      Memo2.Clear;
      TBSOAL.First;
      buf:=TBSOAL.fieldbyname('soal').AsString;
        REPEAT
              END;
//  ShowMessage('masuk');

    end
  else kirimData('$'+no+'s');
  end
else if pos('D',data)<>0 then
  begin
    kirimData('$'+no+'5');
//  ShowMessage('D');
    if no='1' then
      BEGIN
//  ShowMessage('1');
```

```
        inc(baris1);
        Sleep(100);
        kirimData(Memo1.Lines.ValueFromIndex[baris1]);
        inc(baris1);
//        Sleep(100);
        kirimData(Memo1.Lines.ValueFromIndex[baris1]);
        END
      ELSE
        BEGIN
//    ShowMessage('2');
        inc(baris2);
        Sleep(100);
        kirimData(Memo2.Lines.ValueFromIndex[baris2]);
        inc(baris2);
        Sleep(100);
        kirimData(Memo2.Lines.ValueFromIndex[baris2]);
        END;
    end
  else if pos('U',data)<>0 then
    begin
      kirimData('$'+no+'5');
      if no='1' then
        BSOAL.Next;
        inc(i);
        end;
    end;
    end
  else if pos('M',data)<>0 then
    begin
      kirimData('$'+no+'5');
      if no='1' then
        begin
        dec(SOAL1);
        if SOAL1<1 then SOAL1:=TBSOAL.RecordCount;
        Memo1.Clear;
        TBSOAL.First;
        i:=1;

        while i<SOAL1 do
        begin
        TBSOAL.Next;
        inc(i);
        end;

\\       begin
        i:=1;
        TBSOAL.First;
        while i<SOAL2 do
        begin
              inc(SOAL2);
        if SOAL2>TBSOAL.RecordCount then SOAL2:=1;
        Memo2.Clear;
        TBSOAL.First;
        i:=1;

        while i<SOAL2 do
        begin
        TBSOAL.Next;
        inc(i);
        end;

       procedure TForm1.Timer2Timer(Sender: TObject);
  var benar1,benar2,salah1,salah2,nilai1,nilai2:integer;
  begin
  Lwaktu.Caption:=IntToStr(StrToInt(Lwaktu.Caption)+1);
  if StrToInt(Lwaktu.Caption)>=tbwaktu.FieldByName('waktu').AsInteger then
      begin
      timer2.Enabled:=false;
```

```
      TBSOAL.First;
    ilai2:=round(benar2*100/TBSOAL.RecordCount);
     if TbID.FindKey([id1]) then
       end;
end;

procedure TForm1.Button2Click(Sender: TObject);
begin
timer1.Enabled:=true;
end;

procedure TForm1.Button10Click(Sender: TObject);
begin
timer1.Enabled:=false;
end;

Button11.Visible:=false;
end;

procedure TForm1.FormShow(Sender: TObject);
begin
Notebook1.ActivePage:='utama';
end;

procedure TForm1.Button12Click(Sender: TObject);
begin
tbwaktu.Edit;
tbwaktu.Post;
end;

procedure TForm1.WaktuUjian1Click(Sender: TObject);
begin
Notebook1.ActivePage:='waktu';
end;

end.
```

```
#include <at89x52.h>
#include "Pending.c"
#include "lcdku.c"
#include "myser1.c"


#define control          P3_2
#define cs               P3_3
#define toma             P3_7
#define tomb             P3_6
#define tomc             P3_5
#define tomd             P3_4


unsigned char j[16],i,k[21],a,b1,a2,b3,b4,a5,a6,a7,a8,tandap,kondisi,id,b,p;
//unsigned char d[10];
unsigned int tout;
unsigned long Ndata;
bit t;

#define MatrikX1         P0_4
#define MatrikX2         P0_5
#define MatrikX3         P0_6
#define MatrikX4         P0_7

char Tombolnya()
{
        MatrikX1         = 0;
        MatrikX2         = 1;
        MatrikX4         = 1;
        switch ( P0 & 0x0F )
        {
        case 0x0E:
                while(MatrikY1==0){;}
                return '1';
                break;
        case 0x0D:
                while(MatrikY2==0){;}
                return '4';
                break;
        }
        MatrikX1         = 1;
        MatrikX2         = 0;
        MatrikX4         = 1;
        switch ( P0 & 0x0F )
        {
        case 0x0E:
                while(MatrikY1==0){;}
                return '2';
                break;
        case 0x0D:
                while(MatrikY2==0){;}
                return '5';
                break;
          return 'D';
  //return '.';
                break;
        default:
                return 'Z';
        //      break;
        }
yes=Tombolnya();
while (yes=='w') yes=Tombolnya();
}
void cetakid()
  {
  a=0;i=0;
   while(a!='N')
```

```
      {
      key();
      a=yes;
      k[i]=yes;i++;
      //yes='*';
      dataout();
      }
    }
    void cetakpass()
    {
    a=0;i=10;
     while(a!='N')
      {
      key();
      a=yes;
      yes='*';
      dataout();
      }
    }
unsigned char rx2325()
{
  control=0;
   while(!RI){;}
         RI              = 0     ;
  return (SBUF);
}

void tx485(char kirim)
{
  control=1;
   ES      = 0 ;
        SBUF    = kirim;
        while(!TI){;}
        TI              = 0;//Lo;
        ES      = 1 ;
        control=0;
}

void cekrx(unsigned char r,unsigned char s,unsigned char t)
 {
        b=0;p=0;
        //EA=0;
        while(b!=1)
           {
   p=rx445();
   if(p==r)
    {
    p=rx445();
    if(p==s)
      {
       p=rx485();
       if(p==t) b=1;
       else b=0;
      }
    else b=0;
          }
         else b=0;
         }

           //EA=1;
 }
//unsigned char cekon(unsigned char r,unsigned char s)
unsigned char cekon()
 {
  //unsigned char r,s;
        b=0;p=0;
        //EA=0;
        while(b!=1)
```

```
            {
    p=rx232();
    if(p=='$')
     {
     p=rx445();
     if(p==id)
       {
        p=rx232();
        b=1;
        //busek();pos(1,1);yes=p;dataout();delay(2000);
       }
     else b=0;
           }
         else b=0;
         }
          // EA=1;
           return(p);
 }

 void kirimkom()
{
 i=0;yes=0;
  while(yes!='E')
  {
   yes=k[i];
   //tx232('a');
   i++;
  }

  //delay(10);
  //tx232('z');

}

void tampil()
  {
  a=0;yes=0;
 while(yes!='%')
   k[a]=yes;d++;
  }
  a=0;yes=0;
  while(yes!='%')
  {yes=k[a];
   if(yes=='%');
   else dataout();
   a++;
   }
  }
void lanjut()
  {
  //busek();
  cekrx('$',id,'5');
   while(1)
    {
  a=rkey();
  cekrx('$',id,'5');delay(100);tx232(id);tx232(',');
  tx485(a);cekrx('$',id,'5');
  tampilsemua();
    }

    //delay(4000);
  }
//---------------
// Program Utama
// ----------------------------------------------------
void main ()
  initser(0xfd);//19200
  initlcd();
```

```
    i=0;toma=1;tomb=1;tomc=1;tomd=1;
    control=0;id='2';
     tx485('T');
          while(1)//* Pengulangan Loop tanpa henti
          cs=1;
          delay(1000);
          cs=0;
          delay(1000);
      */
    cs=0;
    cetak(1,1,"   Test TOEFL   ");
    cetak(2,1,"   ITN MALANG   ");
    delay(2000);

    busek();cetak(1,1,"ID: ");
     cs=1;
     cekrx('$',id,'5');
          delay(100);
    tx485(id);tx485(',');
    kirimkom();
     if(kondisi=='b') lanjut();
    else cetak(1,1," Salah Myeskan  ");
     delay(2000);
     busek();
          }//* End of While
}//* End of Main
```

Features

- Compatible with MCS-51® Products
- 8K Bytes of In-System Programmable (ISP) Flash Memory
  - Endurance: 1000 Write/Erase Cycles
- 4.0V to 5.5V Operating Range
- Fully Static Operation: 0 Hz to 33 MHz
- Three-level Program Memory Lock
- 256 x 8-bit Internal RAM
- 32 Programmable I/O Lines
- Three 16-bit Timer/Counters
- Eight Interrupt Sources
- Full Duplex UART Serial Channel
- Low-power Idle and Power-down Modes
- Interrupt Recovery from Power-down Mode
- Watchdog Timer
- Dual Data Pointer
- Power-off Flag

Description

The AT89S52 is a low-power, high-performance CMOS 8-bit microcontroller with 8K bytes of in-system programmable Flash memory. The device is manufactured using Atmel's high-density nonvolatile memory technology and is compatible with the industry-standard 80C51 instruction set and pinout. The on-chip Flash allows the program memory to be reprogrammed in-system or by a conventional nonvolatile memory programmer. By combining a versatile 8-bit CPU with in-system programmable Flash on a monolithic chip, the Atmel AT89S52 is a powerful microcontroller which provides a highly-flexible and cost-effective solution to many embedded control applications.

The AT89S52 provides the following standard features: 8K bytes of Flash, 256 bytes of RAM, 32 I/O lines, Watchdog timer, two data pointers, three 16-bit timer/counters, a six-vector two-level interrupt architecture, a full duplex serial port, on-chip oscillator, and clock circuitry. In addition, the AT89S52 is designed with static logic for operation down to zero frequency and supports two software selectable power saving modes. The Idle Mode stops the CPU while allowing the RAM, timer/counters, serial port, and interrupt system to continue functioning. The Power-down mode saves the RAM contents but freezes the oscillator, disabling all other chip functions until the next interrupt or hardware reset.

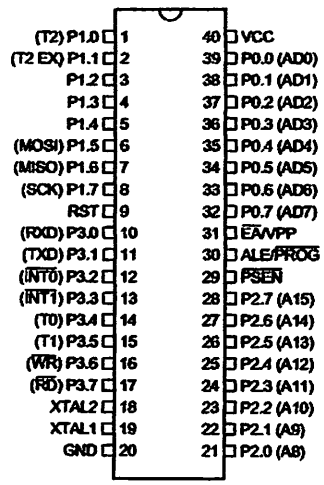
8-bit Microcontroller with 8K Bytes In-System Programmable Flash

AT89S52

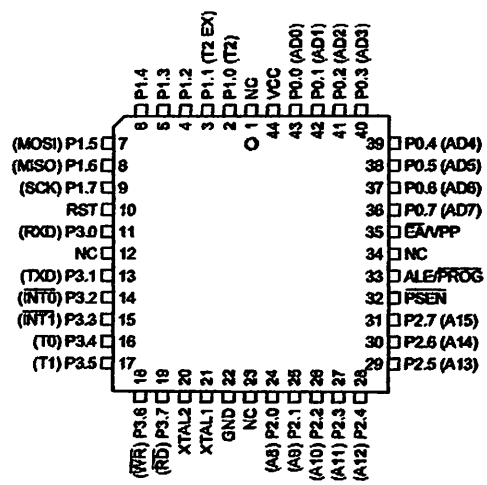
Rev. 1919A-07/01

Pin Configurations

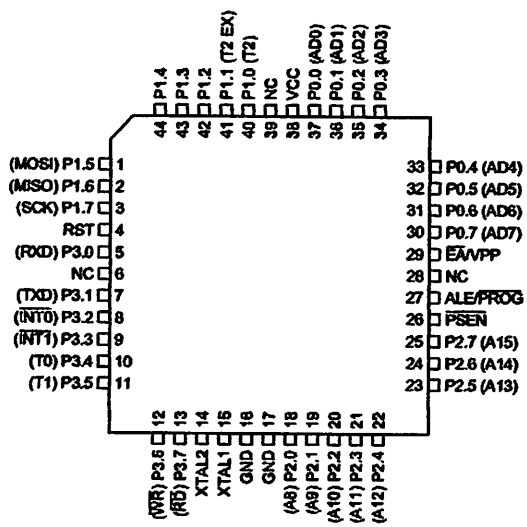
PDIP



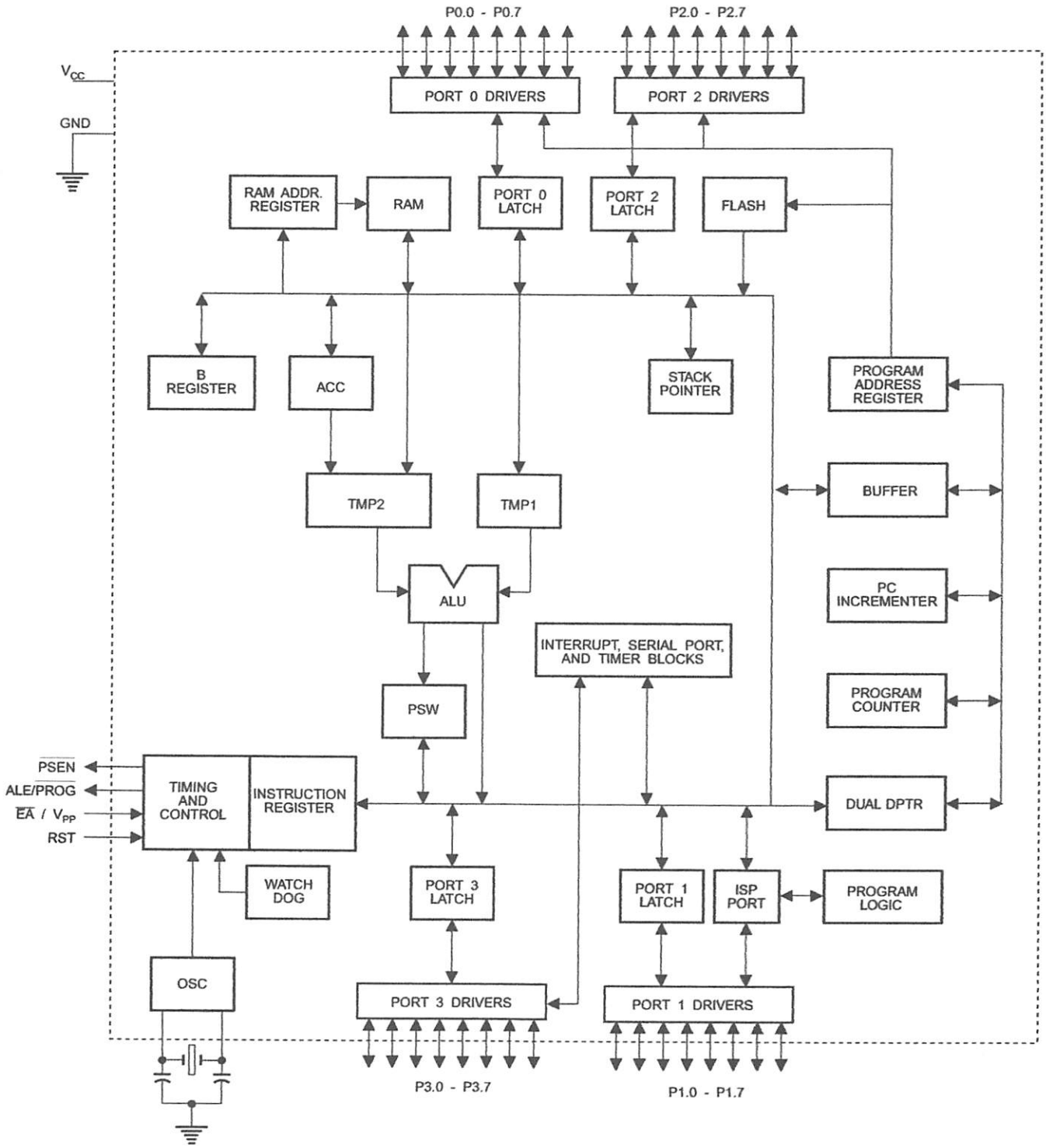
PLCC



TQFP



Block Diagram



Pin Description

VCC

Supply voltage.

GND

Ground.

Port 0

Port 0 is an 8-bit open drain bidirectional I/O port. As an output port, each pin can sink eight TTL inputs. When 1s are written to port 0 pins, the pins can be used as high-impedance inputs.

Port 0 can also be configured to be the multiplexed low-order address/data bus during accesses to external program and data memory. In this mode, P0 has internal pullups.

Port 0 also receives the code bytes during Flash programming and outputs the code bytes during program verification. External pullups are required during program verification.

Port 1

Port 1 is an 8-bit bidirectional I/O port with internal pullups. The Port 1 output buffers can sink/source four TTL inputs. When 1s are written to Port 1 pins, they are pulled high by the internal pullups and can be used as inputs. As inputs, Port 1 pins that are externally being pulled low will source current (I_{IL}) because of the internal pullups.

In addition, P1.0 and P1.1 can be configured to be the timer/counter 2 external count input (P1.0/T2) and the timer/counter 2 trigger input (P1.1/T2EX), respectively, as shown in the following table.

Port 1 also receives the low-order address bytes during Flash programming and verification.

Port Pin	Alternate Functions
P1.0	T2 (external count input to Timer/Counter 2), clock-out
P1.1	T2EX (Timer/Counter 2 capture/reload trigger and direction control)
P1.5	MOSI (used for In-System Programming)
P1.6	MISO (used for In-System Programming)
P1.7	SCK (used for In-System Programming)

Port 2

Port 2 is an 8-bit bidirectional I/O port with internal pullups. The Port 2 output buffers can sink/source four TTL inputs. When 1s are written to Port 2 pins, they are pulled high by the internal pullups and can be used as inputs. As inputs, Port 2 pins that are externally being pulled low will source current (I_{IL}) because of the internal pullups.

Port 2 emits the high-order address byte during fetches from external program memory and during accesses to external data memory that use 16-bit addresses (MOVX @ DPTR). In this application, Port 2 uses strong internal pullups when emitting 1s. During accesses to external data memory that use 8-bit addresses (MOVX @ RI), Port 2 emits the contents of the P2 Special Function Register.

Port 2 also receives the high-order address bits and some control signals during Flash programming and verification.

Port 3

Port 3 is an 8-bit bidirectional I/O port with internal pullups. The Port 3 output buffers can sink/source four TTL inputs. When 1s are written to Port 3 pins, they are pulled high by the internal pullups and can be used as inputs. As inputs, Port 3 pins that are externally being pulled low will source current (I_{IL}) because of the pullups.

Port 3 also serves the functions of various special features of the AT89S52, as shown in the following table.

Port 3 also receives some control signals for Flash programming and verification.

Port Pin	Alternate Functions
P3.0	RXD (serial input port)
P3.1	TXD (serial output port)
P3.2	$\overline{INT0}$ (external interrupt 0)
P3.3	$\overline{INT1}$ (external interrupt 1)
P3.4	T0 (timer 0 external input)
P3.5	T1 (timer 1 external input)
P3.6	$\overline{WR}$ (external data memory write strobe)
P3.7	$\overline{RD}$ (external data memory read strobe)

RST

Reset input. A high on this pin for two machine cycles while the oscillator is running resets the device. This pin drives High for 96 oscillator periods after the Watchdog times out. The DISRTO bit in SFR AUXR (address 8EH) can be used to disable this feature. In the default state of bit DISRTO, the RESET HIGH out feature is enabled.

ALE/$\overline{PROG}$

Address Latch Enable (ALE) is an output pulse for latching the low byte of the address during accesses to external memory. This pin is also the program pulse input ($\overline{PROG}$) during Flash programming.

In normal operation, ALE is emitted at a constant rate of 1/6 the oscillator frequency and may be used for external timing or clocking purposes. Note, however, that one ALE pulse is skipped during each access to external data memory.

If desired, ALE operation can be disabled by setting bit 0 of SFR location 8EH. With the bit set, ALE is active only during a MOVX or MOVC instruction. Otherwise, the pin is

weakly pulled high. Setting the ALE-disable bit has no effect if the microcontroller is in external execution mode.

PSEN

Program Store Enable ($\overline{PSEN}$) is the read strobe to external program memory.

When the AT89S52 is executing code from external program memory, $\overline{PSEN}$ is activated twice each machine cycle, except that two $\overline{PSEN}$ activations are skipped during each access to external data memory.

EA/VPP

External Access Enable. $\overline{EA}$ must be strapped to GND in order to enable the device to fetch code from external program memory locations starting at 0000H up to FFFFH. Note, however, that if lock bit 1 is programmed, $\overline{EA}$ will be internally latched on reset.

$\overline{EA}$ should be strapped to V_{CC} for internal program executions.

This pin also receives the 12-volt programming enable voltage (V_{PP}) during Flash programming.

XTAL1

Input to the inverting oscillator amplifier and input to the internal clock operating circuit.

XTAL2

Output from the inverting oscillator amplifier.

Table 1. AT89S52 SFR Map and Reset Values

0F8H									0FFH
0F0H	B 00000000								0F7H
0E8H									0EFH
0E0H	ACC 00000000								0E7H
0D8H									0DFH
0D0H	PSW 00000000								0D7H
0C8H	T2CON 00000000	T2MOD XXXXXX00	RCAP2L 00000000	RCAP2H 00000000	TL2 00000000	TH2 00000000			0CFH
0C0H									0C7H
0B8H	IP XX000000								0BFH
0B0H	P3 11111111								0B7H
0A8H	IE 0X000000								0AFH
0A0H	P2 11111111		AUXR1 XXXXXXX0				WDTRST XXXXXXXX		0A7H
98H	SCON 00000000	SBUF XXXXXXXX							9FH
90H	P1 11111111								97H
88H	TCON 00000000	TMOD 00000000	TL0 00000000	TL1 00000000	TH0 00000000	TH1 00000000	AUXR XXX00XX0		8FH
80H	P0 11111111	SP 00000111	DP0L 00000000	DP0H 00000000	DP1L 00000000	DP1H 00000000		PCON 0XXX0000	87H

Special Function Registers

A map of the on-chip memory area called the Special Function Register (SFR) space is shown in Table 1.

Note that not all of the addresses are occupied, and unoccupied addresses may not be implemented on the chip. Read accesses to these addresses will in general return random data, and write accesses will have an indeterminate effect.

User software should not write 1s to these unlisted locations, since they may be used in future products to invoke new features. In that case, the reset or inactive values of the new bits will always be 0.

Timer 2 Registers: Control and status bits are contained in registers T2CON (shown in Table 2) and T2MOD (shown in Table 3) for Timer 2. The register pair (RCAP2H, RCAP2L) are the Capture/Reload registers for Timer 2 in 16-bit capture mode or 16-bit auto-reload mode.

Interrupt Registers: The individual interrupt enable bits are in the IE register. Two priorities can be set for each of the six interrupt sources in the IP register.

Table 2. T2CON – Timer/Counter 2 Control Register

T2CON Address = 0C8H — Reset Value = 0000 0000B

Bit Addressable

Bit	TF2	EXF2	RCLK	TCLK	EXEN2	TR2	C/$\overline{T2}$	CP/$\overline{RL2}$
	7	6	5	4	3	2	1	0

Symbol	Function
TF2	Timer 2 overflow flag set by a Timer 2 overflow and must be cleared by software. TF2 will not be set when either RCLK = 1 or TCLK = 1.
EXF2	Timer 2 external flag set when either a capture or reload is caused by a negative transition on T2EX and EXEN2 = 1. When Timer 2 interrupt is enabled, EXF2 = 1 will cause the CPU to vector to the Timer 2 interrupt routine. EXF2 must be cleared by software. EXF2 does not cause an interrupt in up/down counter mode (DCEN = 1).
RCLK	Receive clock enable. When set, causes the serial port to use Timer 2 overflow pulses for its receive clock in serial port Modes 1 and 3. RCLK = 0 causes Timer 1 overflow to be used for the receive clock.
TCLK	Transmit clock enable. When set, causes the serial port to use Timer 2 overflow pulses for its transmit clock in serial port Modes 1 and 3. TCLK = 0 causes Timer 1 overflows to be used for the transmit clock.
EXEN2	Timer 2 external enable. When set, allows a capture or reload to occur as a result of a negative transition on T2EX if Timer 2 is not being used to clock the serial port. EXEN2 = 0 causes Timer 2 to ignore events at T2EX.
TR2	Start/Stop control for Timer 2. TR2 = 1 starts the timer.
C/$\overline{T2}$	Timer or counter select for Timer 2. C/$\overline{T2}$ = 0 for timer function. C/$\overline{T2}$ = 1 for external event counter (falling edge triggered).
CP/$\overline{RL2}$	Capture/Reload select. CP/$\overline{RL2}$ = 1 causes captures to occur on negative transitions at T2EX if EXEN2 = 1. CP/$\overline{RL2}$ = 0 causes automatic reloads to occur when Timer 2 overflows or negative transitions occur at T2EX when EXEN2 = 1. When either RCLK or TCLK = 1, this bit is ignored and the timer is forced to auto-reload on Timer 2 overflow.

Table 3a. AUXR: Auxiliary Register

AUXR — Address = 8EH — Reset Value = XXX00XX0B

Not Bit Addressable

Bit	7	6	5	4	3	2	1	0
	–	–	–	WDIDLE	DISRTO	–	–	DISALE

– Reserved for future expansion

DISALE Disable/Enable ALE

DISALE	Operating Mode
0	ALE is emitted at a constant rate of 1/6 the oscillator frequency
1	ALE is active only during a MOVX or MOVC instruction

DISRTO Disable/Enable Reset out

DISRTO	
0	Reset pin is driven High after WDT times out
1	Reset pin is input only

WDIDLE Disable/Enable WDT in IDLE mode

WDIDLE	
0	WDT continues to count in IDLE mode
1	WDT halts counting in IDLE mode

Dual Data Pointer Registers: To facilitate accessing both internal and external data memory, two banks of 16-bit Data Pointer Registers are provided: DP0 at SFR address locations 82H-83H and DP1 at 84H-85H. Bit DPS = 0 in SFR AUXR1 selects DP0 and DPS = 1 selects DP1. The user should always initialize the DPS bit to the appropriate value before accessing the respective Data Pointer Register.

Power Off Flag: The Power Off Flag (POF) is located at bit 4 (PCON.4) in the PCON SFR. POF is set to "1" during power up. It can be set and rest under software control and is not affected by reset.

Table 3b. AUXR1: Auxiliary Register 1

AUXR1 — Address = A2H — Reset Value = XXXXXXX0B

Not Bit Addressable

Bit	7	6	5	4	3	2	1	0
	–	–	–	–	–	–	–	DPS

– Reserved for future expansion

DPS Data Pointer Register Select

DPS	
0	Selects DPTR Registers DP0L, DP0H
1	Selects DPTR Registers DP1L, DP1H

Memory Organization

MCS-51 devices have a separate address space for Program and Data Memory. Up to 64K bytes each of external Program and Data Memory can be addressed.

Program Memory

If the $\overline{EA}$ pin is connected to GND, all program fetches are directed to external memory.

On the AT89S52, if $\overline{EA}$ is connected to V_{CC}, program fetches to addresses 0000H through 1FFFH are directed to internal memory and fetches to addresses 2000H through FFFFH are to external memory.

Data Memory

The AT89S52 implements 256 bytes of on-chip RAM. The upper 128 bytes occupy a parallel address space to the Special Function Registers. This means that the upper 128 bytes have the same addresses as the SFR space but are physically separate from SFR space.

When an instruction accesses an internal location above address 7FH, the address mode used in the instruction specifies whether the CPU accesses the upper 128 bytes of RAM or the SFR space. Instructions which use direct addressing access of the SFR space.

For example, the following direct addressing instruction accesses the SFR at location 0A0H (which is P2).

```
MOV 0A0H, #data
```

Instructions that use indirect addressing access the upper 128 bytes of RAM. For example, the following indirect addressing instruction, where R0 contains 0A0H, accesses the data byte at address 0A0H, rather than P2 (whose address is 0A0H).

```
MOV @R0, #data
```

Note that stack operations are examples of indirect addressing, so the upper 128 bytes of data RAM are available as stack space.

Watchdog Timer (One-time Enabled with Reset-out)

The WDT is intended as a recovery method in situations where the CPU may be subjected to software upsets. The WDT consists of a 13-bit counter and the Watchdog Timer Reset (WDTRST) SFR. The WDT is defaulted to disable from exiting reset. To enable the WDT, a user must write 01EH and 0E1H in sequence to the WDTRST register (SFR location 0A6H). When the WDT is enabled, it will increment every machine cycle while the oscillator is running. The WDT timeout period is dependent on the external clock frequency. There is no way to disable the WDT except through reset (either hardware reset or WDT overflow reset). When WDT overflows, it will drive an output RESET HIGH pulse at the RST pin.

Using the WDT

To enable the WDT, a user must write 01EH and 0E1H in sequence to the WDTRST register (SFR location 0A6H). When the WDT is enabled, the user needs to service it by writing 01EH and 0E1H to WDTRST to avoid a WDT overflow. The 13-bit counter overflows when it reaches 8191 (1FFFH), and this will reset the device. When the WDT is enabled, it will increment every machine cycle while the oscillator is running. This means the user must reset the WDT at least every 8191 machine cycles. To reset the WDT the user must write 01EH and 0E1H to WDTRST. WDTRST is a write-only register. The WDT counter cannot be read or written. When WDT overflows, it will generate an output RESET pulse at the RST pin. The RESET pulse duration is 96xTOSC, where TOSC=1/FOSC. To make the best use of the WDT, it should be serviced in those sections of code that will periodically be executed within the time required to prevent a WDT reset.

WDT During Power-down and Idle

In Power-down mode the oscillator stops, which means the WDT also stops. While in Power-down mode, the user does not need to service the WDT. There are two methods of exiting Power-down mode: by a hardware reset or via a level-activated external interrupt which is enabled prior to entering Power-down mode. When Power-down is exited with hardware reset, servicing the WDT should occur as it normally does whenever the AT89S52 is reset. Exiting Power-down with an interrupt is significantly different. The interrupt is held low long enough for the oscillator to stabilize. When the interrupt is brought high, the interrupt is serviced. To prevent the WDT from resetting the device while the interrupt pin is held low, the WDT is not started until the interrupt is pulled high. It is suggested that the WDT be reset during the interrupt service for the interrupt used to exit Power-down mode.

To ensure that the WDT does not overflow within a few states of exiting Power-down, it is best to reset the WDT just before entering Power-down mode.

Before going into the IDLE mode, the WDIDLE bit in SFR AUXR is used to determine whether the WDT continues to count if enabled. The WDT keeps counting during IDLE (WDIDLE bit = 0) as the default state. To prevent the WDT from resetting the AT89S52 while in IDLE mode, the user should always set up a timer that will periodically exit IDLE, service the WDT, and reenter IDLE mode.

With WDIDLE bit enabled, the WDT will stop to count in IDLE mode and resumes the count upon exit from IDLE.

UART

The UART in the AT89S52 operates the same way as the UART in the AT89C51 and AT89C52. For further information on the UART operation, refer to the ATMEL Web site (http://www.atmel.com). From the home page, select 'Products', then '8051-Architecture Flash Microcontroller', then 'Product Overview'.

Timer 0 and 1

Timer 0 and Timer 1 in the AT89S52 operate the same way as Timer 0 and Timer 1 in the AT89C51 and AT89C52. For further information on the timers' operation, refer to the ATMEL Web site (http://www.atmel.com). From the home page, select 'Products', then '8051-Architecture Flash Microcontroller', then 'Product Overview'.

Timer 2

Timer 2 is a 16-bit Timer/Counter that can operate as either a timer or an event counter. The type of operation is selected by bit C/$\overline{T2}$ in the SFR T2CON (shown in Table 2). Timer 2 has three operating modes: capture, auto-reload (up or down counting), and baud rate generator. The modes are selected by bits in T2CON, as shown in Table 3. Timer 2 consists of two 8-bit registers, TH2 and TL2. In the Timer function, the TL2 register is incremented every machine cycle. Since a machine cycle consists of 12 oscillator periods, the count rate is 1/12 of the oscillator frequency.

Table 3. Timer 2 Operating Modes

RCLK +TCLK	CP/$\overline{RL2}$	TR2	MODE
0	0	1	16-bit Auto-reload
0	1	1	16-bit Capture
1	X	1	Baud Rate Generator
X	X	0	(Off)

In the Counter function, the register is incremented in response to a 1-to-0 transition at its corresponding external input pin, T2. In this function, the external input is sampled during S5P2 of every machine cycle. When the samples show a high in one cycle and a low in the next cycle, the count is incremented. The new count value appears in the register during S3P1 of the cycle following the one in which the transition was detected. Since two machine cycles (24 oscillator periods) are required to recognize a 1-to-0 transition, the maximum count rate is 1/24 of the oscillator frequency. To ensure that a given level is sampled at least once before it changes, the level should be held for at least one full machine cycle.

Capture Mode

In the capture mode, two options are selected by bit EXEN2 in T2CON. If EXEN2 = 0, Timer 2 is a 16-bit timer or counter which upon overflow sets bit TF2 in T2CON. This bit can then be used to generate an interrupt. If EXEN2 = 1, Timer 2 performs the same operation, but a 1-to-0 transition at external input T2EX also causes the current value in TH2 and TL2 to be captured into RCAP2H and RCAP2L, respectively. In addition, the transition at T2EX causes bit EXF2 in T2CON to be set. The EXF2 bit, like TF2, can generate an interrupt. The capture mode is illustrated in Figure 5.

Auto-reload (Up or Down Counter)

Timer 2 can be programmed to count up or down when configured in its 16-bit auto-reload mode. This feature is invoked by the DCEN (Down Counter Enable) bit located in the SFR T2MOD (see Table 4). Upon reset, the DCEN bit is set to 0 so that timer 2 will default to count up. When DCEN is set, Timer 2 can count up or down, depending on the value of the T2EX pin.

Figure 5. Timer in Capture Mode

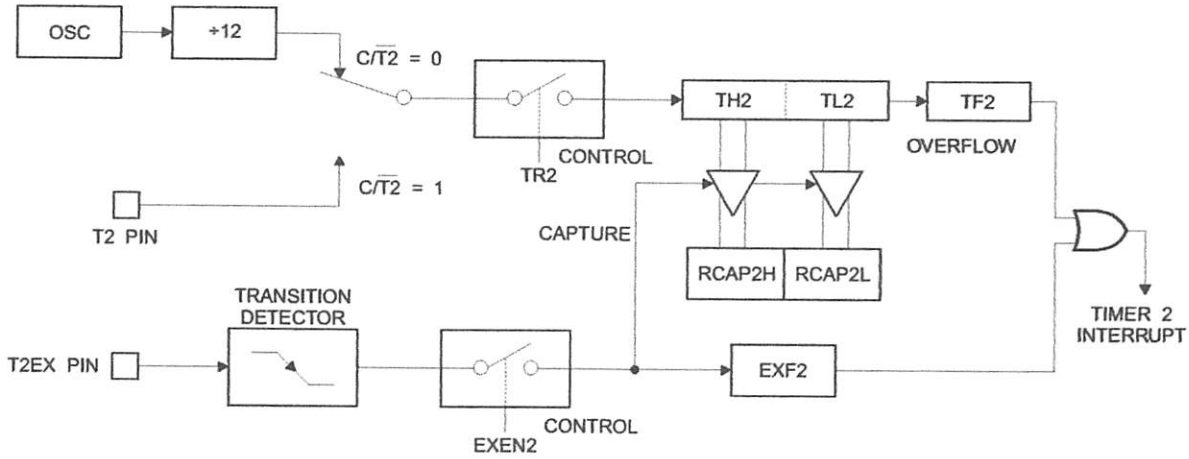


Figure 6 shows Timer 2 automatically counting up when DCEN=0. In this mode, two options are selected by bit EXEN2 in T2CON. If EXEN2 = 0, Timer 2 counts up to 0FFFFH and then sets the TF2 bit upon overflow. The overflow also causes the timer registers to be reloaded with the 16-bit value in RCAP2H and RCAP2L. The values in Timer in Capture ModeRCAP2H and RCAP2L are preset by software. If EXEN2 = 1, a 16-bit reload can be triggered either by an overflow or by a 1-to-0 transition at external input T2EX. This transition also sets the EXF2 bit. Both the TF2 and EXF2 bits can generate an interrupt if enabled.

Setting the DCEN bit enables Timer 2 to count up or down, as shown in Figure 6. In this mode, the T2EX pin controls the direction of the count. A logic 1 at T2EX makes Timer 2 count up. The timer will overflow at 0FFFFH and set the TF2 bit. This overflow also causes the 16-bit value in RCAP2H and RCAP2L to be reloaded into the timer registers, TH2 and TL2, respectively.

A logic 0 at T2EX makes Timer 2 count down. The timer underflows when TH2 and TL2 equal the values stored in RCAP2H and RCAP2L. The underflow sets the TF2 bit and causes 0FFFFH to be reloaded into the timer registers.

The EXF2 bit toggles whenever Timer 2 overflows or underflows and can be used as a 17th bit of resolution. In this operating mode, EXF2 does not flag an interrupt.

Figure 6. Timer 2 Auto Reload Mode (DCEN = 0)

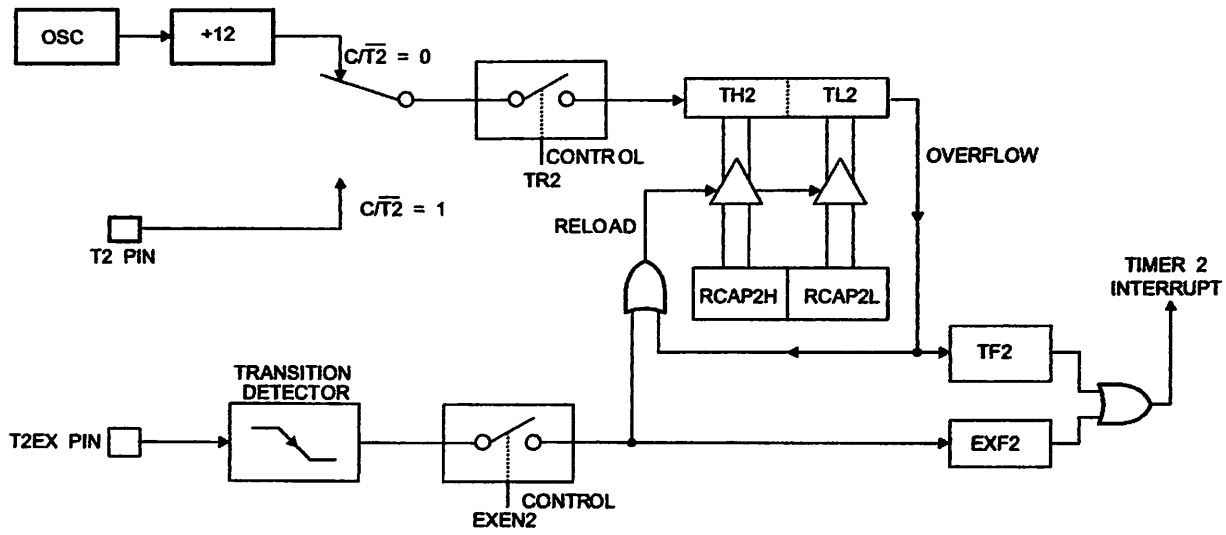


Table 4. T2MOD – Timer 2 Mode Control Register

T2MOD Address = 0C9H — Reset Value = XXXX XX00B

Not Bit Addressable

Bit	7	6	5	4	3	2	1	0
	–	–	–	–	–	–	T2OE	DCEN

Symbol	Function
–	Not implemented, reserved for future
T2OE	Timer 2 Output Enable bit
DCEN	When set, this bit allows Timer 2 to be configured as an up/down counter

Figure 7. Timer 2 Auto Reload Mode (DCEN = 1)

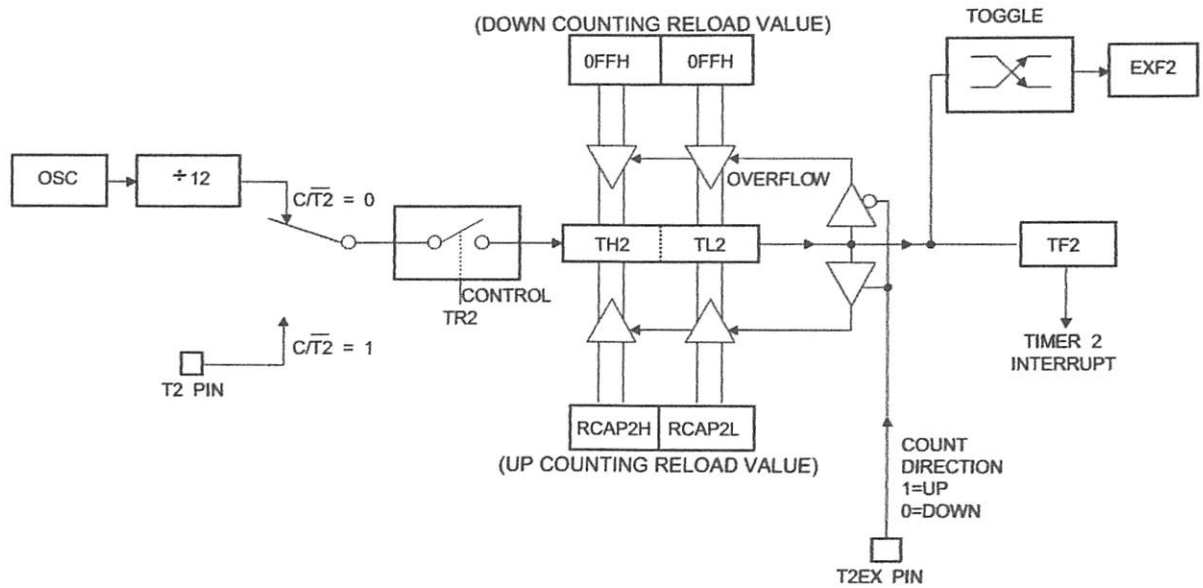
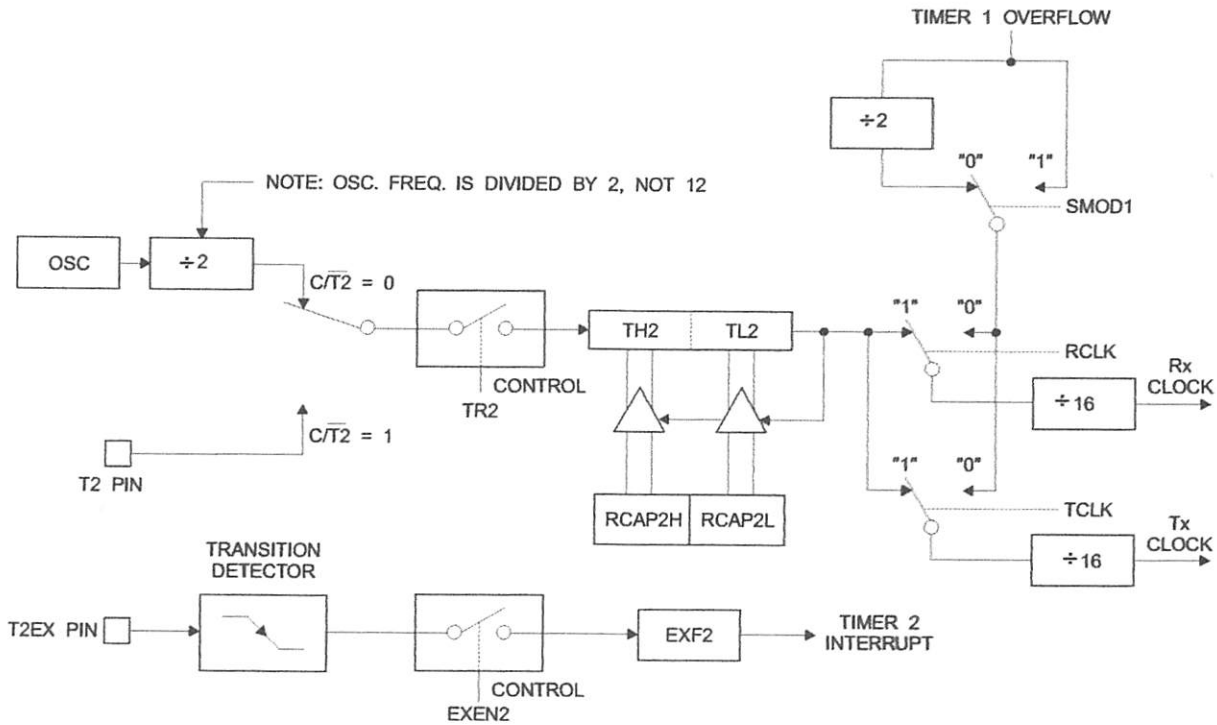


Figure 8. Timer 2 in Baud Rate Generator Mode



Baud Rate Generator

Timer 2 is selected as the baud rate generator by setting TCLK and/or RCLK in T2CON (Table 2). Note that the baud rates for transmit and receive can be different if Timer 2 is used for the receiver or transmitter and Timer 1 is used for the other function. Setting RCLK and/or TCLK puts Timer 2 into its baud rate generator mode, as shown in Figure 8.

The baud rate generator mode is similar to the auto-reload mode, in that a rollover in TH2 causes the Timer 2 registers to be reloaded with the 16-bit value in registers RCAP2H and RCAP2L, which are preset by software.

The baud rates in Modes 1 and 3 are determined by Timer 2's overflow rate according to the following equation.

$$\text{Modes 1 and 3 Baud Rates} = \frac{\text{Timer 2 Overflow Rate}}{16}$$

The Timer can be configured for either timer or counter operation. In most applications, it is configured for timer operation ($C/\overline{T2} = 0$). The timer operation is different for Timer 2 when it is used as a baud rate generator. Normally, as a timer, it increments every machine cycle (at 1/12 the oscillator frequency). As a baud rate generator, however, it increments every state time (at 1/2 the oscillator frequency). The baud rate formula is given below.

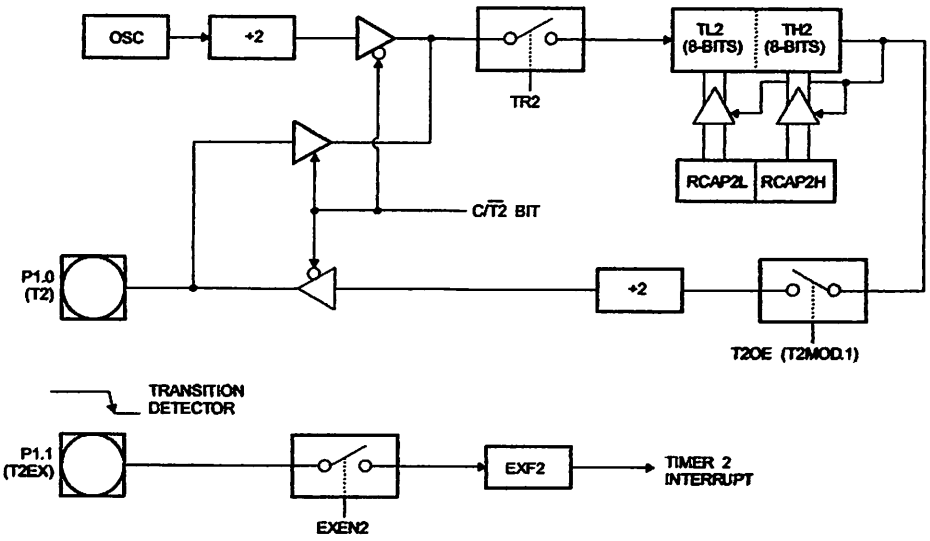
$$\frac{\text{Modes 1 and 3}}{\text{Baud Rate}} = \frac{\text{Oscillator Frequency}}{32 \times [65536 - \text{RCAP2H,RCAP2L})]}$$

where (RCAP2H, RCAP2L) is the content of RCAP2H and RCAP2L taken as a 16-bit unsigned integer.

Timer 2 as a baud rate generator is shown in Figure 8. This figure is valid only if RCLK or TCLK = 1 in T2CON. Note that a rollover in TH2 does not set TF2 and will not generate an interrupt. Note too, that if EXEN2 is set, a 1-to-0 transition in T2EX will set EXF2 but will not cause a reload from (RCAP2H, RCAP2L) to (TH2, TL2). Thus, when Timer 2 is in use as a baud rate generator, T2EX can be used as an extra external interrupt.

Note that when Timer 2 is running (TR2 = 1) as a timer in the baud rate generator mode, TH2 or TL2 should not be read from or written to. Under these conditions, the Timer is incremented every state time, and the results of a read or write may not be accurate. The RCAP2 registers may be read but should not be written to, because a write might overlap a reload and cause write and/or reload errors. The timer should be turned off (clear TR2) before accessing the Timer 2 or RCAP2 registers.

Figure 9. Timer 2 in Clock-Out Mode



Programmable Clock Out

A 50% duty cycle clock can be programmed to come out on P1.0, as shown in Figure 9. This pin, besides being a regular I/O pin, has two alternate functions. It can be programmed to input the external clock for Timer/Counter 2 or to output a 50% duty cycle clock ranging from 61 Hz to 4 MHz at a 16 MHz operating frequency.

To configure the Timer/Counter 2 as a clock generator, bit C/$\overline{T2}$ (T2CON.1) must be cleared and bit T2OE (T2MOD.1) must be set. Bit TR2 (T2CON.2) starts and stops the timer.

The clock-out frequency depends on the oscillator frequency and the reload value of Timer 2 capture registers (RCAP2H, RCAP2L), as shown in the following equation.

$$\text{Clock-Out Frequency} = \frac{\text{Oscillator Frequency}}{4 \times [65536-(\text{RCAP2H,RCAP2L})]}$$

In the clock-out mode, Timer 2 roll-overs will not generate an interrupt. This behavior is similar to when Timer 2 is used as a baud-rate generator. It is possible to use Timer 2 as a baud-rate generator and a clock generator simultaneously. Note, however, that the baud-rate and clock-out frequencies cannot be determined independently from one another since they both use RCAP2H and RCAP2L.

Interrupts

The AT89S52 has a total of six interrupt vectors: two external interrupts ($\overline{INT0}$ and $\overline{INT1}$), three timer interrupts (Timers 0, 1, and 2), and the serial port interrupt. These interrupts are all shown in Figure 10.

Each of these interrupt sources can be individually enabled or disabled by setting or clearing a bit in Special Function Register IE. IE also contains a global disable bit, EA, which disables all interrupts at once.

Note that Table 5 shows that bit position IE.6 is unimplemented. In the AT89S52, bit position IE.5 is also unimplemented. User software should not write 1s to these bit positions, since they may be used in future AT89 products.

Timer 2 interrupt is generated by the logical OR of bits TF2 and EXF2 in register T2CON. Neither of these flags is cleared by hardware when the service routine is vectored to. In fact, the service routine may have to determine whether it was TF2 or EXF2 that generated the interrupt, and that bit will have to be cleared in software.

The Timer 0 and Timer 1 flags, TF0 and TF1, are set at S5P2 of the cycle in which the timers overflow. The values are then polled by the circuitry in the next cycle. However, the Timer 2 flag, TF2, is set at S2P2 and is polled in the same cycle in which the timer overflows.

Table 5. Interrupt Enable (IE) Register

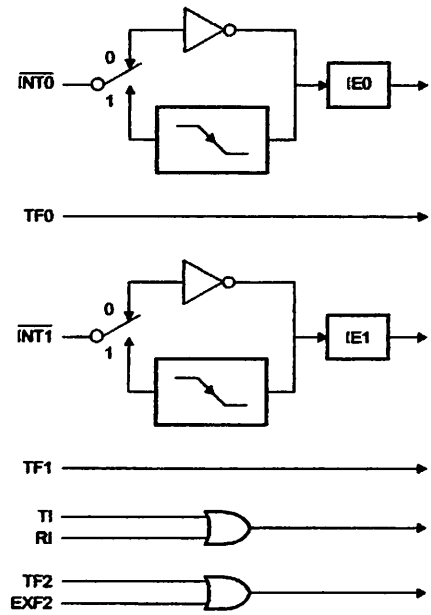
(MSB)							(LSB)
EA	–	ET2	ES	ET1	EX1	ET0	EX0

Enable Bit = 1 enables the interrupt.

Enable Bit = 0 disables the interrupt.

Symbol	Position	Function
EA	IE.7	Disables all interrupts. If EA = 0, no interrupt is acknowledged. If EA = 1, each interrupt source is individually enabled or disabled by setting or clearing its enable bit.
–	IE.6	Reserved.
ET2	IE.5	Timer 2 interrupt enable bit.
ES	IE.4	Serial Port interrupt enable bit.
ET1	IE.3	Timer 1 interrupt enable bit.
EX1	IE.2	External interrupt 1 enable bit.
ET0	IE.1	Timer 0 interrupt enable bit.
EX0	IE.0	External interrupt 0 enable bit.
User software should never write 1s to unimplemented bits, because they may be used in future AT89 products.		

Figure 10. Interrupt Sources



Oscillator Characteristics

XTAL1 and XTAL2 are the input and output, respectively, of an inverting amplifier that can be configured for use as an on-chip oscillator, as shown in Figure 11. Either a quartz crystal or ceramic resonator may be used. To drive the device from an external clock source, XTAL2 should be left unconnected while XTAL1 is driven, as shown in Figure 12. There are no requirements on the duty cycle of the external clock signal, since the input to the internal clocking circuitry is through a divide-by-two flip-flop, but minimum and maximum voltage high and low time specifications must be observed.

Idle Mode

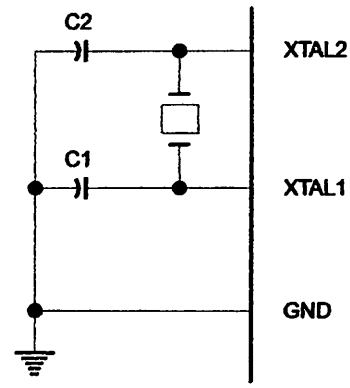
In idle mode, the CPU puts itself to sleep while all the on-chip peripherals remain active. The mode is invoked by software. The content of the on-chip RAM and all the special functions registers remain unchanged during this mode. The idle mode can be terminated by any enabled interrupt or by a hardware reset.

Note that when idle mode is terminated by a hardware reset, the device normally resumes program execution from where it left off, up to two machine cycles before the internal reset algorithm takes control. On-chip hardware inhibits access to internal RAM in this event, but access to the port pins is not inhibited. To eliminate the possibility of an unexpected write to a port pin when idle mode is terminated by a reset, the instruction following the one that invokes idle mode should not write to a port pin or to external memory.

Power-down Mode

In the Power-down mode, the oscillator is stopped, and the instruction that invokes Power-down is the last instruction executed. The on-chip RAM and Special Function Registers retain their values until the Power-down mode is terminated. Exit from Power-down mode can be initiated either by a hardware reset or by an enabled external interrupt. Reset redefines the SFRs but does not change the on-chip RAM. The reset should not be activated before V_{CC} is restored to its normal operating level and must be held active long enough to allow the oscillator to restart and stabilize.

Figure 11. Oscillator Connections



Note: C1, C2 = 30 pF ± 10 pF for Crystals
= 40 pF ± 10 pF for Ceramic Resonators

Figure 12. External Clock Drive Configuration

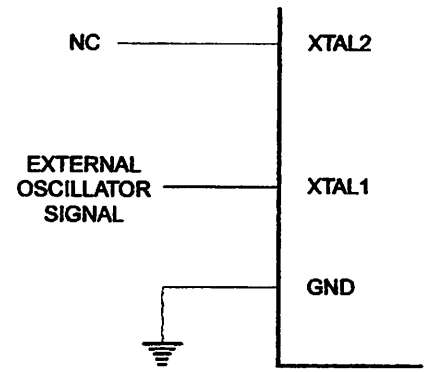


Table 6. Status of External Pins During Idle and Power-down Modes

Mode	Program Memory	ALE	$\overline{PSEN}$	PORT0	PORT1	PORT2	PORT3
Idle	Internal	1	1	Data	Data	Data	Data
Idle	External	1	1	Float	Data	Address	Data
Power-down	Internal	0	0	Data	Data	Data	Data
Power-down	External	0	0	Float	Data	Data	Data

Program Memory Lock Bits

The AT89S52 has three lock bits that can be left unprogrammed (U) or can be programmed (P) to obtain the additional features listed in the following table.

Table 7. Lock Bit Protection Modes

Program Lock Bits				
	LB1	LB2	LB3	Protection Type
1	U	U	U	No program lock features
2	P	U	U	MOVC instructions executed from external program memory are disabled from fetching code bytes from internal memory, $\overline{EA}$ is sampled and latched on reset, and further programming of the Flash memory is disabled
3	P	P	U	Same as mode 2, but verify is also disabled
4	P	P	P	Same as mode 3, but external execution is also disabled

When lock bit 1 is programmed, the logic level at the $\overline{EA}$ pin is sampled and latched during reset. If the device is powered up without a reset, the latch initializes to a random value and holds that value until reset is activated. The latched value of $\overline{EA}$ must agree with the current logic level at that pin in order for the device to function properly.

Programming the Flash – Parallel Mode

The AT89S52 is shipped with the on-chip Flash memory array ready to be programmed. The programming interface needs a high-voltage (12-volt) program enable signal and is compatible with conventional third-party Flash or EPROM programmers.

The AT89S52 code memory array is programmed byte-by-byte.

Programming Algorithm: Before programming the AT89S52, the address, data, and control signals should be set up according to the Flash programming mode table and Figures 13 and 14. To program the AT89S52, take the following steps:

1. Input the desired memory location on the address lines.
2. Input the appropriate data byte on the data lines.
3. Activate the correct combination of control signals.
4. Raise $\overline{EA}/V_{PP}$ to 12V.
5. Pulse ALE/$\overline{PROG}$ once to program a byte in the Flash array or the lock bits. The byte-write cycle is self-timed and typically takes no more than 50 µs.

Repeat steps 1 through 5, changing the address and data for the entire array or until the end of the object file is reached.

$\overline{Data}$ Polling: The AT89S52 features $\overline{Data}$ Polling to indicate the end of a byte write cycle. During a write cycle, an attempted read of the last byte written will result in the complement of the written data on P0.7. Once the write cycle has been completed, true data is valid on all outputs, and the next cycle may begin. $\overline{Data}$ Polling may begin any time after a write cycle has been initiated.

Ready/$\overline{Busy}$: The progress of byte programming can also be monitored by the RDY/$\overline{BSY}$ output signal. P3.0 is pulled low after ALE goes high during programming to indicate $\overline{BUSY}$. P3.0 is pulled high again when programming is done to indicate READY.

Program Verify: If lock bits LB1 and LB2 have not been programmed, the programmed code data can be read back via the address and data lines for verification. The status of the individual lock bits can be verified directly by reading them back.

Reading the Signature Bytes: The signature bytes are read by the same procedure as a normal verification of locations 000H, 100H, and 200H, except that P3.6 and P3.7 must be pulled to a logic low. The values returned are as follows.

(000H) = 1EH indicates manufactured by Atmel
(100H) = 52H indicates 89S52
(200H) = 06H

Chip Erase: In the parallel programming mode, a chip erase operation is initiated by using the proper combination of control signals and by pulsing ALE/$\overline{PROG}$ low for a duration of 200 ns - 500 ns.

In the serial programming mode, a chip erase operation is initiated by issuing the Chip Erase instruction. In this mode, chip erase is self-timed and takes about 500 ms.

During chip erase, a serial read from any address location will return 00H at the data output.

Programming the Flash – Serial Mode

The Code memory array can be programmed using the serial ISP interface while RST is pulled to V_{CC}. The serial interface consists of pins SCK, MOSI (input) and MISO (output). After RST is set high, the Programming Enable instruction needs to be executed first before other operations can be executed. Before a reprogramming sequence can occur, a Chip Erase operation is required.

The Chip Erase operation turns the content of every memory location in the Code array into FFH.

Either an external system clock can be supplied at pin XTAL1 or a crystal needs to be connected across pins XTAL1 and XTAL2. The maximum serial clock (SCK)

frequency should be less than 1/16 of the crystal frequency. With a 33 MHz oscillator clock, the maximum SCK frequency is 2 MHz.

Serial Programming Algorithm

To program and verify the AT89S52 in the serial programming mode, the following sequence is recommended:

1. Power-up sequence:

   Apply power between VCC and GND pins.

   Set RST pin to "H".

   If a crystal is not connected across pins XTAL1 and XTAL2, apply a 3 MHz to 33 MHz clock to XTAL1 pin and wait for at least 10 milliseconds.
2. Enable serial programming by sending the Programming Enable serial instruction to pin MOSI/P1.5. The frequency of the shift clock supplied at pin SCK/P1.7 needs to be less than the CPU clock at XTAL1 divided by 16.
3. The Code array is programmed one byte at a time by supplying the address and data together with the appropriate Write instruction. The write cycle is self-timed and typically takes less than 1 ms at 5V.
4. Any memory location can be verified by using the Read instruction which returns the content at the selected address at serial output MISO/P1.6.
5. At the end of a programming session, RST can be set low to commence normal device operation.

Power-off sequence (if needed):

Set XTAL1 to "L" (if a crystal is not used).

Set RST to "L".

Turn V_{CC} power off.

$\overline{\text{Data}}$ Polling: The $\overline{\text{Data}}$ Polling feature is also available in the serial mode. In this mode, during a write cycle an attempted read of the last byte written will result in the complement of the MSB of the serial output byte on MISO.

Serial Programming Instruction Set

The Instruction Set for Serial Programming follows a 4-byte protocol and is shown in Table 10.

Programming Interface – Parallel Mode

Every code byte in the Flash array can be programmed by using the appropriate combination of control signals. The write operation cycle is self-timed and once initiated, will automatically time itself to completion.

All major programming vendors offer worldwide support for the Atmel microcontroller series. Please contact your local programming vendor for the appropriate software revision.

Table 8. Flash Programming Modes

Mode	V_{CC}	RST	$\overline{PSEN}$	ALE/ $\overline{PROG}$	$\overline{EA}$/ V_{PP}	P2.6	P2.7	P3.3	P3.6	P3.7	P0.7-0 Data	P2.4-0 Address	P1.7-0 Address
Write Code Data	5V	H	L	(2)	12V	L	H	H	H	H	D_{IN}	A12-8	A7-0
Read Code Data	5V	H	L	H	H	L	L	L	H	H	D_{OUT}	A12-8	A7-0
Write Lock Bit 1	5V	H	L	(3)	12V	H	H	H	H	H	X	X	X
Write Lock Bit 2	5V	H	L	(3)	12V	H	H	H	L	L	X	X	X
Write Lock Bit 3	5V	H	L	(3)	12V	H	L	H	H	L	X	X	X
Read Lock Bits 1, 2, 3	5V	H	L	H	H	H	H	L	H	L	P0.2, P0.3, P0.4	X	X
Chip Erase	5V	H	L	(1)	12V	H	L	H	L	L	X	X	X
Read Atmel ID	5V	H	L	H	H	L	L	L	L	L	1EH	X 0000	00H
Read Device ID	5V	H	L	H	H	L	L	L	L	L	52H	X 0001	00H
Read Device ID	5V	H	L	H	H	L	L	L	L	L	06H	X 0010	00H

Notes:
1. Each $\overline{PROG}$ pulse is 200 ns - 500 ns for Chip Erase.
2. Each $\overline{PROG}$ pulse is 200 ns - 500 ns for Write Code Data.
3. Each $\overline{PROG}$ pulse is 200 ns - 500 ns for Write Lock Bits.
4. RDY/$\overline{BSY}$ signal is output on P3.0 during programming.
5. X = don't care.

Figure 13. Programming the Flash Memory (Parallel Mode)

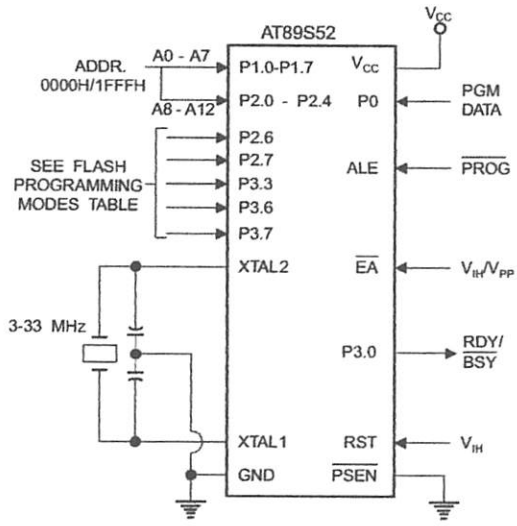
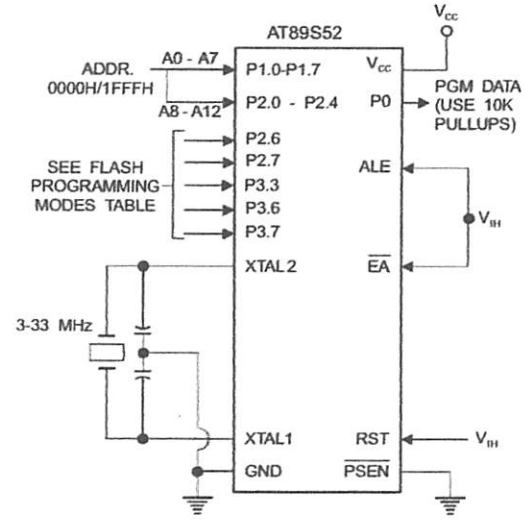


Figure 14. Verifying the Flash Memory (Parallel Mode)



Flash Programming and Verification Characteristics (Parallel Mode)

T_A = 20°C to 30°C, V_{CC} = 4.5 to 5.5V

Symbol	Parameter	Min	Max	Units
V_{PP}	Programming Supply Voltage	11.5	12.5	V
I_{PP}	Programming Supply Current		10	mA
I_{CC}	V_{CC} Supply Current		30	mA
$1/t_{CLCL}$	Oscillator Frequency	3	33	MHz
t_{AVGL}	Address Setup to $\overline{PROG}$ Low	$48t_{CLCL}$		
t_{GHAX}	Address Hold After $\overline{PROG}$	$48t_{CLCL}$		
t_{DVGL}	Data Setup to $\overline{PROG}$ Low	$48t_{CLCL}$		
t_{GHDX}	Data Hold After $\overline{PROG}$	$48t_{CLCL}$		
t_{EHSH}	P2.7 ($\overline{ENABLE}$) High to V_{PP}	$48t_{CLCL}$		
t_{SHGL}	V_{PP} Setup to $\overline{PROG}$ Low	10		µs
t_{GHSL}	V_{PP} Hold After $\overline{PROG}$	10		µs
t_{GLGH}	$\overline{PROG}$ Width	0.2	1	µs
t_{AVQV}	Address to Data Valid		$48t_{CLCL}$	
t_{ELQV}	$\overline{ENABLE}$ Low to Data Valid		$48t_{CLCL}$	
t_{EHQZ}	Data Float After $\overline{ENABLE}$	0	$48t_{CLCL}$	
t_{GHBL}	$\overline{PROG}$ High to $\overline{BUSY}$ Low		1.0	µs
t_{WC}	Byte Write Cycle Time		50	µs

Figure 15. Flash Programming and Verification Waveforms – Parallel Mode

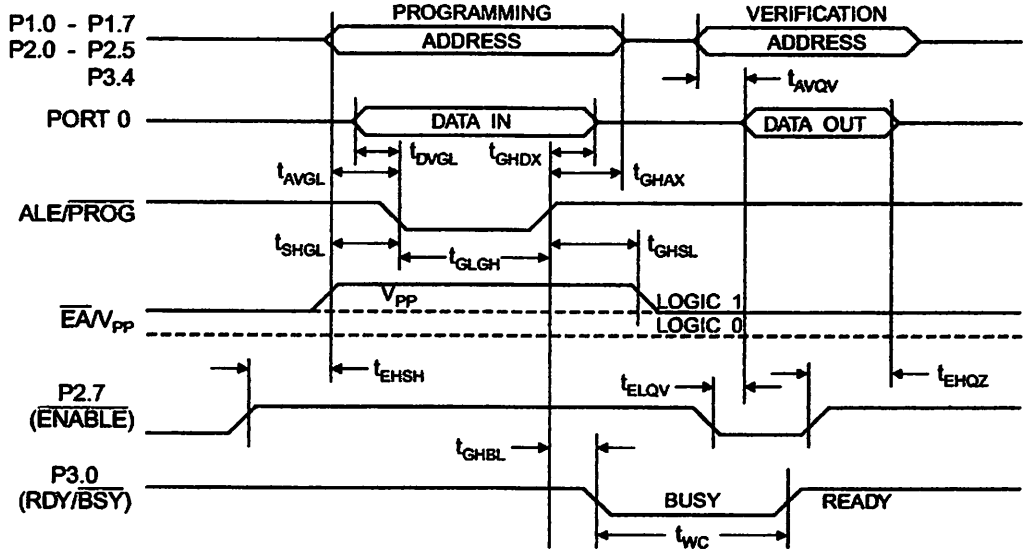
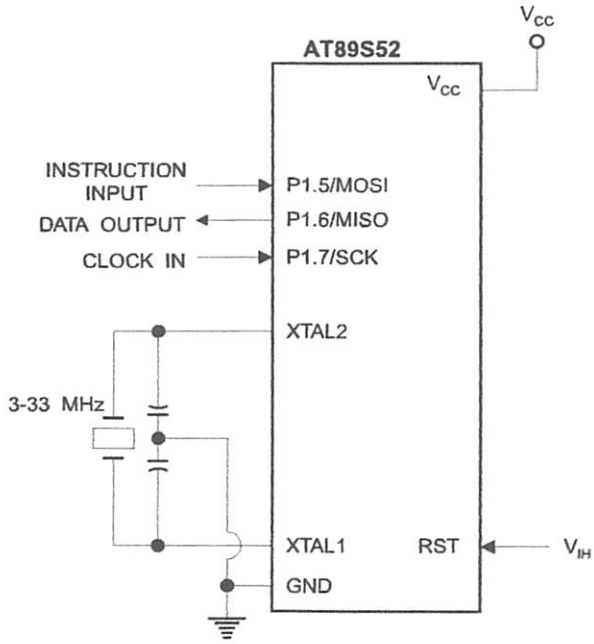


Figure 16. Flash Memory Serial Downloading



Flash Programming and Verification Waveforms – Serial Mode

Figure 17. Serial Programming Waveforms

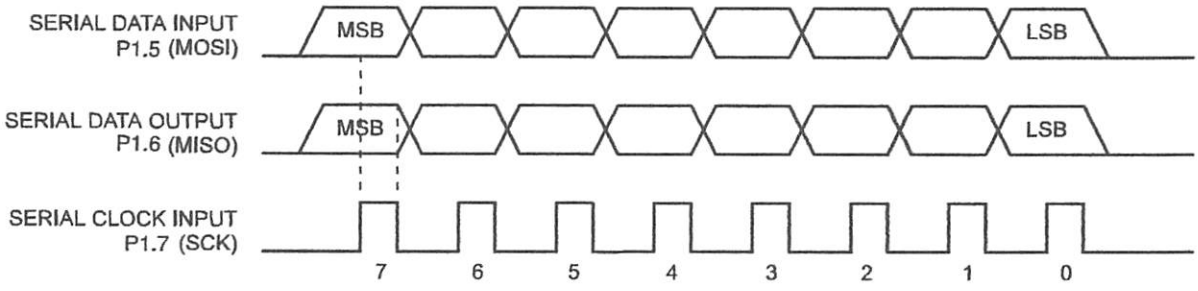


Table 9. Serial Programming Instruction Set

Instruction	Instruction Format Byte 1	Byte 2	Byte 3	Byte 4	Operation
Programming Enable	1010 1100	0101 0011	xxxx xxxx	xxxx xxxx 0110 1001 (Output)	Enable Serial Programming while RST is high
Chip Erase	1010 1100	100x xxxx	xxxx xxxx	xxxx xxxx	Chip Erase Flash memory array
Read Program Memory (Byte Mode)	0010 0000	xxx A12 A11 A10 A9 A8	A7 A6 A5 A4 A3 A2 A1 A0	D7 D6 D5 D4 D3 D2 D1 D0	Read data from Program memory in the byte mode
Write Program Memory (Byte Mode)	0100 0000	xxx A12 A11 A10 A9 A8	A7 A6 A5 A4 A3 A2 A1 A0	D7 D6 D5 D4 D3 D2 D1 D0	Write data to Program memory in the byte mode
Write Lock Bits[2]	1010 1100	1110 00 B1 B2	xxxx xxxx	xxxx xxxx	Write Lock bits. See Note (2).
Read Lock Bits	0010 0100	xxxx xxxx	xxxx xxxx	xx LB3 LB2 LB1 xx	Read back current status of the lock bits (a programmed lock bit reads back as a '1')
Read Signature Bytes[1]	0010 1000	xxx A5 A4 A3 A2 A1 A0	xxx xxxx	Signature Byte	Read Signature Byte
Read Program Memory (Page Mode)	0011 0000	xxx A12 A11 A10 A9 A8	Byte 0	Byte 1... Byte 255	Read data from Program memory in the Page Mode (256 bytes)
Write Program Memory (Page Mode)	0101 0000	xxx A12 A11 A10 A9 A8	Byte 0	Byte 1... Byte 255	Write data to Program memory in the Page Mode (256 bytes)

Notes: 1. The signature bytes are not readable in Lock Bit Modes 3 and 4.

2. B1 = 0, B2 = 0 —> Mode 1, no lock protection
   B1 = 0, B2 = 1 —> Mode 2, lock bit 1 activated
   B1 = 1, B2 = 0 —> Mode 3, lock bit 2 activated
   B1 = 1, B1 = 1 —> Mode 4, lock bit 3 activated

   Each of the lock bits needs to be activated sequentially before Mode 4 can be executed.

After Reset signal is high, SCK should be low for at least 64 system clocks before it goes high to clock in the enable data bytes. No pulsing of Reset signal is necessary. SCK should be no faster than 1/16 of the system clock at XTAL1.

For Page Read/Write, the data always starts from byte 0 to 255. After the command byte and upper address byte are latched, each byte thereafter is treated as data until all 256 bytes are shifted in/out. Then the next instruction will be ready to be decoded.

Serial Programming Characteristics

Figure 18. Serial Programming Timing

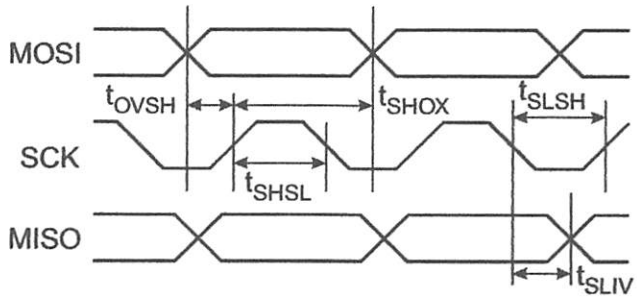


Table 10. Serial Programming Characteristics, T_A = -40° C to 85° C, V_{CC} = 4.0 - 5.5V (Unless otherwise noted)

Symbol	Parameter	Min	Typ	Max	Units
$1/t_{CLCL}$	Oscillator Frequency	0		33	MHz
t_{CLCL}	Oscillator Period	30			ns
t_{SHSL}	SCK Pulse Width High	2 t_{CLCL}			ns
t_{SLSH}	SCK Pulse Width Low	2 t_{CLCL}			ns
t_{OVSH}	MOSI Setup to SCK High	t_{CLCL}			ns
t_{SHOX}	MOSI Hold after SCK High	2 t_{CLCL}			ns
t_{SLIV}	SCK Low to MISO Valid	10	16	32	ns
t_{ERASE}	Chip Erase Instruction Cycle Time			500	ms
t_{SWC}	Serial Byte Write Cycle Time			64 t_{CLCL} + 400	µs

Absolute Maximum Ratings*

Operating Temperature	-55°C to +125°C
Storage Temperature	-65°C to +150°C
Voltage on Any Pin with Respect to Ground	-1.0V to +7.0V
Maximum Operating Voltage	6.6V
DC Output Current	15.0 mA

*NOTICE: Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC Characteristics

The values shown in this table are valid for T_A = -40°C to 85°C and V_{CC} = 4.0V to 5.5V, unless otherwise noted.

Symbol	Parameter	Condition	Min	Max	Units
V_{IL}	Input Low Voltage	(Except $\overline{EA}$)	-0.5	0.2 V_{CC}-0.1	V
V_{IL1}	Input Low Voltage ($\overline{EA}$)		-0.5	0.2 V_{CC}-0.3	V
V_{IH}	Input High Voltage	(Except XTAL1, RST)	0.2 V_{CC}+0.9	V_{CC}+0.5	V
V_{IH1}	Input High Voltage	(XTAL1, RST)	0.7 V_{CC}	V_{CC}+0.5	V
V_{OL}	Output Low Voltage[1] (Ports 1,2,3)	I_{OL} = 1.6 mA		0.45	V
V_{OL1}	Output Low Voltage[1] (Port 0, ALE, $\overline{PSEN}$)	I_{OL} = 3.2 mA		0.45	V
V_{OH}	Output High Voltage (Ports 1,2,3, ALE, $\overline{PSEN}$)	I_{OH} = -60 µA, V_{CC} = 5V ± 10%	2.4		V
		I_{OH} = -25 µA	0.75 V_{CC}		V
		I_{OH} = -10 µA	0.9 V_{CC}		V
V_{OH1}	Output High Voltage (Port 0 in External Bus Mode)	I_{OH} = -800 µA, V_{CC} = 5V ± 10%	2.4		V
		I_{OH} = -300 µA	0.75 V_{CC}		V
		I_{OH} = -80 µA	0.9 V_{CC}		V
I_{IL}	Logical 0 Input Current (Ports 1,2,3)	V_{IN} = 0.45V		-50	µA
I_{TL}	Logical 1 to 0 Transition Current (Ports 1,2,3)	V_{IN} = 2V, V_{CC} = 5V ±10%		-650	µA
I_{LI}	Input Leakage Current (Port 0, $\overline{EA}$)	0.45 < V_{IN} < V_{CC}		±10	µA
RRST	Reset Pulldown Resistor		10	30	KΩ
C_{IO}	Pin Capacitance	Test Freq. = 1 MHz, T_A = 25°C		10	pF
I_{CC}	Power Supply Current	Active Mode, 12 MHz		25	mA
		Idle Mode, 12 MHz		6.5	mA
	Power-down Mode[1]	V_{CC} = 5.5V		50	µA

Notes:
1. Under steady state (non-transient) conditions, I_{OL} must be externally limited as follows:
   Maximum I_{OL} per port pin: 10 mA
   Maximum I_{OL} per 8-bit port:
   Port 0: 26 mA Ports 1, 2, 3: 15 mA
   Maximum total I_{OL} for all output pins: 71 mA
   If I_{OL} exceeds the test condition, V_{OL} may exceed the related specification. Pins are not guaranteed to sink current greater than the listed test conditions.
2. Minimum V_{CC} for Power-down is 2V.

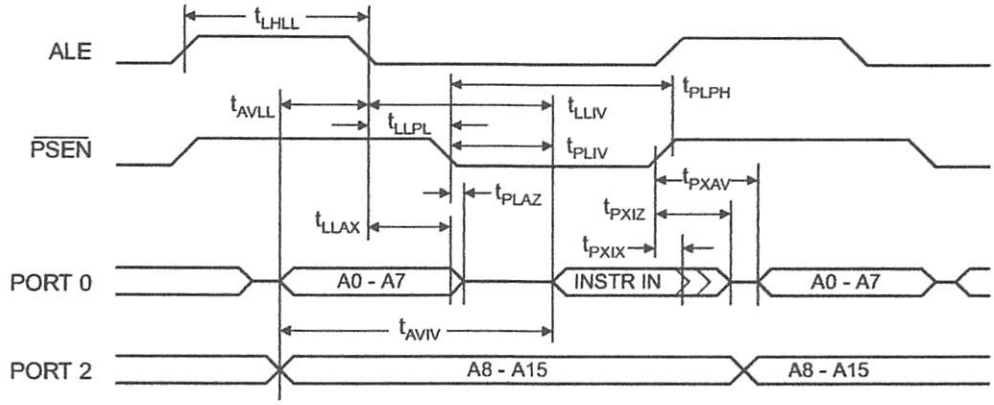
AC Characteristics

Under operating conditions, load capacitance for Port 0, ALE/$\overline{PROG}$, and $\overline{PSEN}$ = 100 pF; load capacitance for all other outputs = 80 pF.

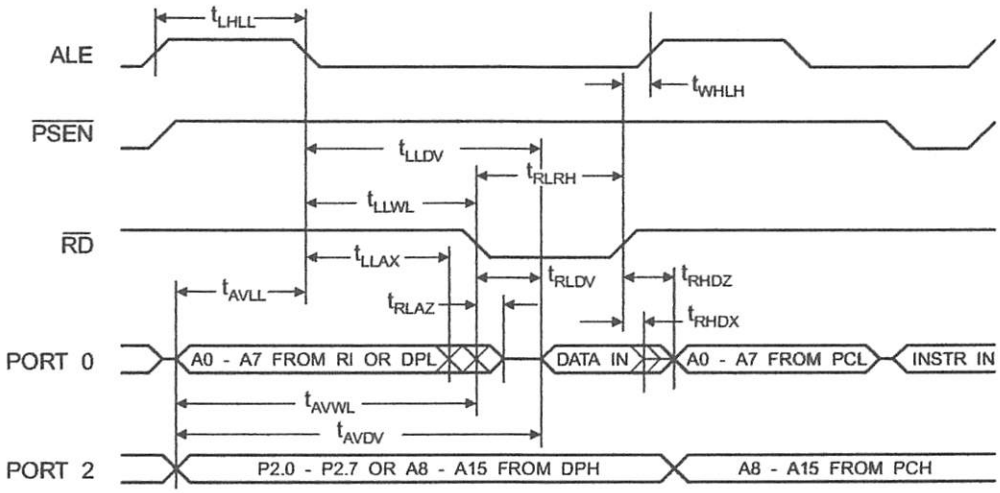
External Program and Data Memory Characteristics

Symbol	Parameter	12 MHz Oscillator		Variable Oscillator		Units
		Min	Max	Min	Max	
$1/t_{CLCL}$	Oscillator Frequency			0	33	MHz
t_{LHLL}	ALE Pulse Width	127		$2t_{CLCL}$-40		ns
t_{AVLL}	Address Valid to ALE Low	43		t_{CLCL}-25		ns
t_{LLAX}	Address Hold After ALE Low	48		t_{CLCL}-25		ns
t_{LLIV}	ALE Low to Valid Instruction In		233		$4t_{CLCL}$-65	ns
t_{LLPL}	ALE Low to $\overline{PSEN}$ Low	43		t_{CLCL}-25		ns
t_{PLPH}	$\overline{PSEN}$ Pulse Width	205		$3t_{CLCL}$-45		ns
t_{PLIV}	$\overline{PSEN}$ Low to Valid Instruction In		145		$3t_{CLCL}$-60	ns
t_{PXIX}	Input Instruction Hold After $\overline{PSEN}$	0		0		ns
t_{PXIZ}	Input Instruction Float After $\overline{PSEN}$		59		t_{CLCL}-25	ns
t_{PXAV}	$\overline{PSEN}$ to Address Valid	75		t_{CLCL}-8		ns
t_{AVIV}	Address to Valid Instruction In		312		$5t_{CLCL}$-80	ns
t_{PLAZ}	$\overline{PSEN}$ Low to Address Float		10		10	ns
t_{RLRH}	$\overline{RD}$ Pulse Width	400		$6t_{CLCL}$-100		ns
t_{WLWH}	$\overline{WR}$ Pulse Width	400		$6t_{CLCL}$-100		ns
t_{RLDV}	$\overline{RD}$ Low to Valid Data In		252		$5t_{CLCL}$-90	ns
t_{RHDX}	Data Hold After $\overline{RD}$	0		0		ns
t_{RHDZ}	Data Float After $\overline{RD}$		97		$2t_{CLCL}$-28	ns
t_{LLDV}	ALE Low to Valid Data In		517		$8t_{CLCL}$-150	ns
t_{AVDV}	Address to Valid Data In		585		$9t_{CLCL}$-165	ns
t_{LLWL}	ALE Low to $\overline{RD}$ or $\overline{WR}$ Low	200	300	$3t_{CLCL}$-50	$3t_{CLCL}$+50	ns
t_{AVWL}	Address to $\overline{RD}$ or $\overline{WR}$ Low	203		$4t_{CLCL}$-75		ns
t_{QVWX}	Data Valid to $\overline{WR}$ Transition	23		t_{CLCL}-30		ns
t_{QVWH}	Data Valid to $\overline{WR}$ High	433		$7t_{CLCL}$-130		ns
t_{WHQX}	Data Hold After $\overline{WR}$	33		t_{CLCL}-25		ns
t_{RLAZ}	$\overline{RD}$ Low to Address Float		0		0	ns
t_{WHLH}	$\overline{RD}$ or $\overline{WR}$ High to ALE High	43	123	t_{CLCL}-25	t_{CLCL}+25	ns

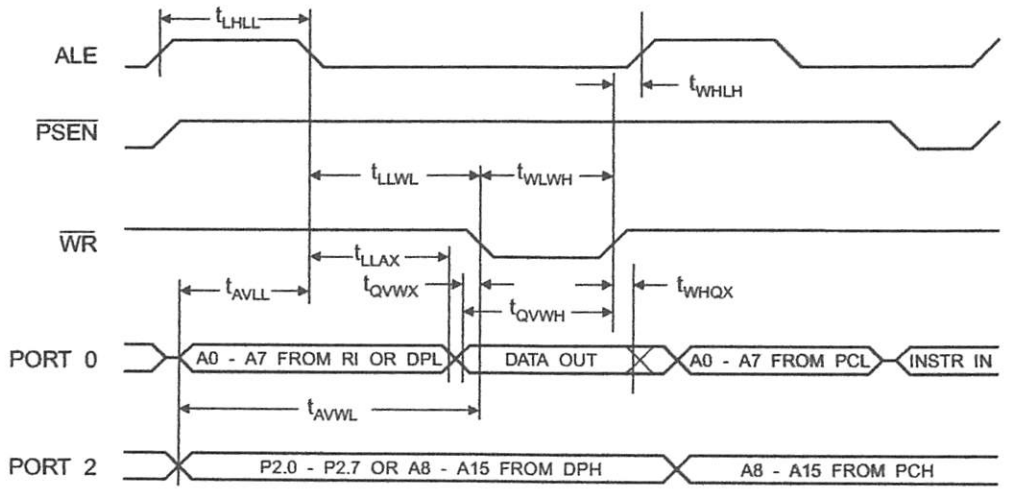
External Program Memory Read Cycle



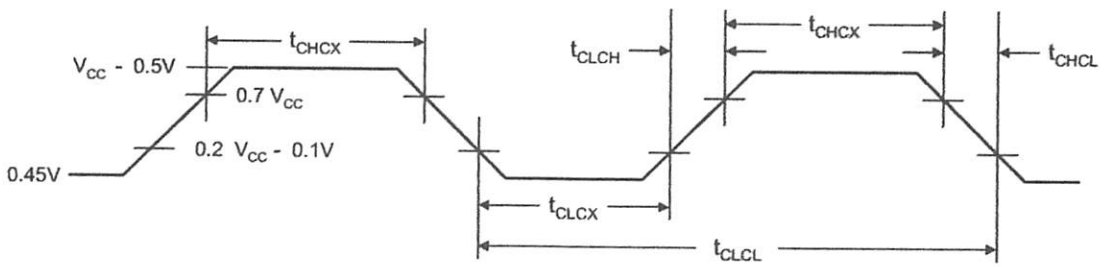
External Data Memory Read Cycle



External Data Memory Write Cycle



External Clock Drive Waveforms



External Clock Drive

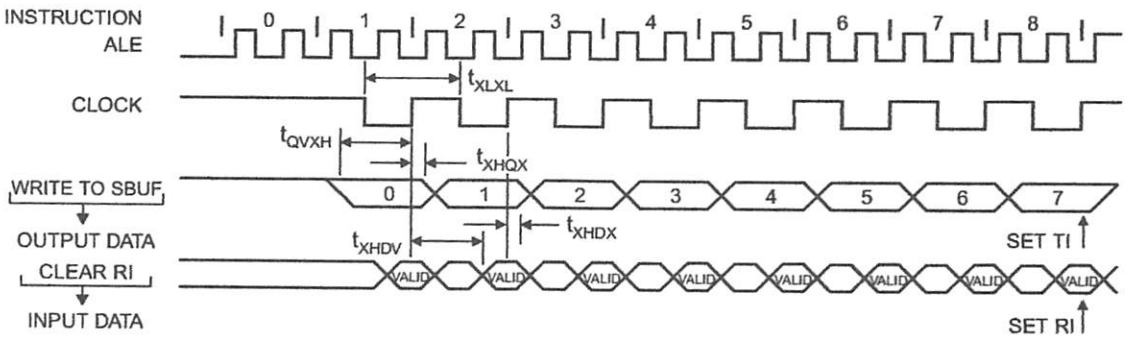
Symbol	Parameter	Min	Max	Units
$1/t_{CLCL}$	Oscillator Frequency	0	33	MHz
t_{CLCL}	Clock Period	30		ns
t_{CHCX}	High Time	12		ns
t_{CLCX}	Low Time	12		ns
t_{CLCH}	Rise Time		5	ns
t_{CHCL}	Fall Time		5	ns

Serial Port Timing: Shift Register Mode Test Conditions

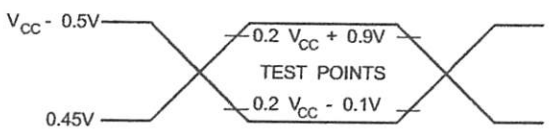
The values in this table are valid for V_{CC} = 4.0V to 5.5V and Load Capacitance = 80 pF.

Symbol	Parameter	12 MHz Osc		Variable Oscillator		Units
		Min	Max	Min	Max	
t_{XLXL}	Serial Port Clock Cycle Time	1.0		$12t_{CLCL}$		µs
t_{QVXH}	Output Data Setup to Clock Rising Edge	700		$10t_{CLCL}$-133		ns
t_{XHQX}	Output Data Hold After Clock Rising Edge	50		$2t_{CLCL}$-80		ns
t_{XHDX}	Input Data Hold After Clock Rising Edge	0		0		ns
t_{XHDV}	Clock Rising Edge to Input Data Valid		700		$10t_{CLCL}$-133	ns

Shift Register Mode Timing Waveforms

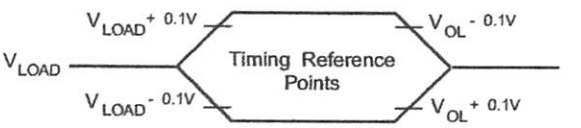


AC Testing Input/Output Waveforms[1]



Note: 1. AC Inputs during testing are driven at V_{CC} - 0.5V for a logic 1 and 0.45V for a logic 0. Timing measurements are made at V_{IH} min. for a logic 1 and V_{IL} max. for a logic 0.

Float Waveforms[1]



Note: 1. For timing purposes, a port pin is no longer floating when a 100 mV change from load voltage occurs. A port pin begins to float when a 100 mV change from the loaded V_{OH}/V_{OL} level occurs.

Ordering Information

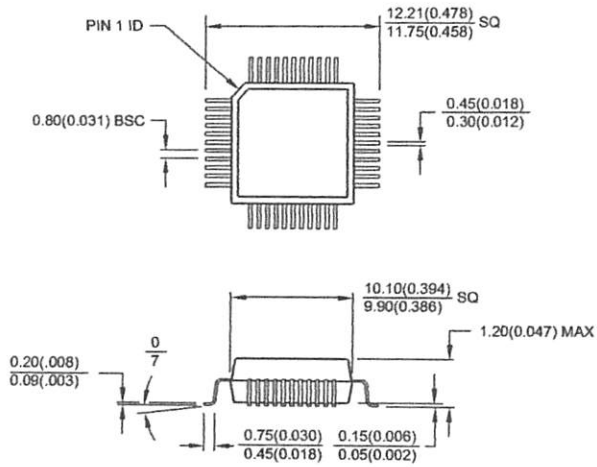
Speed (MHz)	Power Supply	Ordering Code	Package	Operation Range
24	4.0V to 5.5V	AT89S52-24AC AT89S52-24JC AT89S52-24PC	44A 44J 40P6	Commercial (0° C to 70° C)
		AT89S52-24AI AT89S52-24JI AT89S52-24PI	44A 44J 40P6	Industrial (-40° C to 85° C)
33	4.5V to 5.5V	AT89S52-33AC AT89S52-33JC AT89S52-33PC	44A 44J 40P6	Commercial (0° C to 70° C)

= Preliminary Availability

Package Type	
44A	44-lead, Thin Plastic Gull Wing Quad Flatpack (TQFP)
44J	44-lead, Plastic J-leaded Chip Carrier (PLCC)
40P6	40-pin, 0.600" Wide, Plastic Dual Inline Package (PDIP)

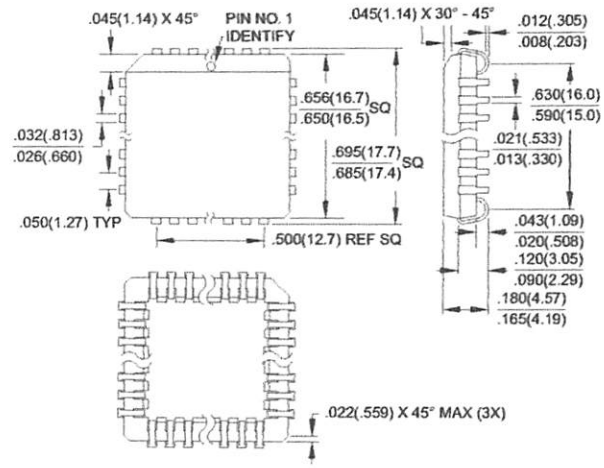
Packaging Information

44A, 44-lead, Thin (1.0 mm) Plastic Gull Wing Quad Flat Package (TQFP)
Dimensions in Millimeters and (Inches)*

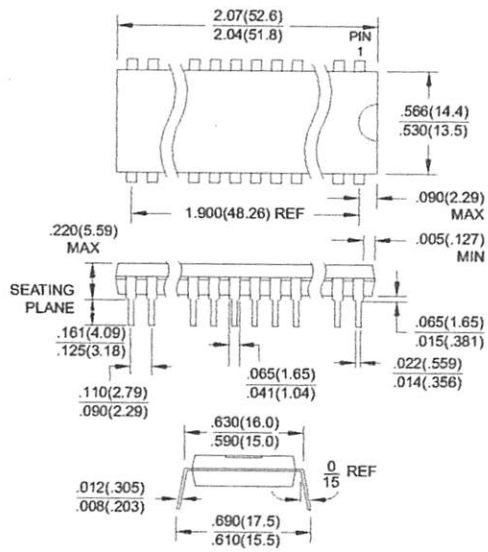


*Controlling dimension: millimeters

44J, 44-lead, Plastic J-leaded Chip Carrier (PLCC)
Dimensions in Inches and (Millimeters)



40P6, 40-pin, 0.600" Wide, Plastic Dual Inline Package (PDIP)
Dimensions in Inches and (Millimeters)
JEDEC STANDARD MS-011 AC



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Rev.1919A-07/01/xM

19-0175; Rev 3; 5/96

MAXIM

±15kV ESD-Protected, +5V RS-232 Transceivers

General Description

The MAX202E–MAX213E, MAX232E/MAX241E line drivers/receivers are designed for RS-232 and V.28 communications in harsh environments. Each transmitter output and receiver input is protected against ±15kV electrostatic discharge (ESD) shocks, without latchup. The various combinations of features are outlined in the *Selection Guide*. The drivers and receivers for all ten devices meet all EIA/TIA-232E and CCITT V.28 specifications at data rates up to 120kbps, when loaded in accordance with the EIA/TIA-232E specification.

The MAX211E/MAX213E/MAX241E are available in 28-pin SO packages, as well as a 28-pin SSOP that uses 60% less board space. The MAX202E/MAX232E come in 16-pin narrow SO, wide SO, and DIP packages. The MAX203E comes in a 20-pin DIP/SO package, and needs no external charge-pump capacitors. The MAX205E comes in a 24-pin wide DIP package, and also eliminates external charge-pump capacitors. The MAX206E/MAX207E/MAX208E come in 24-pin SO, SSOP, and narrow DIP packages. The MAX232E/MAX241E operate with four 1µF capacitors, while the MAX202E/MAX206E/MAX207E/MAX208E/MAX211E/MAX213E operate with four 0.1µF capacitors, further reducing cost and board space.

Applications

Notebook, Subnotebook, and Palmtop Computers
Battery-Powered Equipment
Hand-Held Equipment

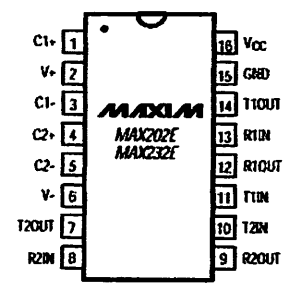
Ordering Information appears at end of data sheet.

Features

- **ESD Protection for RS-232 I/O Pins:**
  ±15kV—Human Body Model
  ±8kV—IEC1000-4-2, Contact Discharge
  ±15kV—IEC1000-4-2, Air-Gap Discharge
- **Latchup Free (unlike bipolar equivalents)**
- **Guaranteed 120kbps Data Rate—LapLink™ Compatible**
- **Guaranteed 3V/µs Min Slew Rate**
- **Operate from a Single +5V Power Supply**

Pin Configurations

TOP VIEW



DIP/SO

Pin Configurations and Typical Operating Circuits continued at end of data sheet.

Selection Guide

PART	No. of RS-232 DRIVERS	No. of RS-232 RECEIVERS	RECEIVERS ACTIVE IN SHUTDOWN	No. of EXTERNAL CAPACITORS	LOW-POWER SHUTDOWN	TTL THREE-STATE
MAX202E	2	2	0	4 (0.1µF)	No	No
MAX203E	2	2	0	None	No	No
MAX205E	5	5	0	None	Yes	Yes
MAX206E	4	3	0	4 (0.1µF)	Yes	Yes
MAX207E	5	3	0	4 (0.1µF)	No	No
MAX208E	4	4	0	4 (0.1µF)	No	No
MAX211E	4	5	0	4 (0.1µF)	Yes	Yes
MAX213E	4	5	2	4 (0.1µF)	Yes	Yes
MAX232E	2	2	0	4 (1µF)	No	No
MAX241E	4	5	0	4 (1µF)	Yes	Yes

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ABSOLUTE MAXIMUM RATINGS

VCC .....-0.3V to +6V
V+ .....(VCC - 0.3V) to +14V
V- .....-14V to +0.3V
Input Voltages
T_IN .....-0.3V to (V+ + 0.3V)
R_IN .....±30V
Output Voltages
T_OUT .....(V- - 0.3V) to (V+ + 0.3V)
R_OUT .....-0.3V to (VCC + 0.3V)
Short-Circuit Duration, T_OUT .....Continuous
Continuous Power Dissipation (TA = +70°C)
16-Pin Plastic DIP (derate 10.53mW/°C above +70°C) 842mW
16-Pin Narrow SO (derate 8.70mW/°C above +70°C) 696mW
16-Pin Wide SO (derate 9.52mW/°C above +70°C) 762mW
20-Pin Plastic DIP (derate 11.11mW/°C above +70°C)...889mW
20-Pin SO (derate 10.00mW/°C above +70°C).....800mW
24-Pin Narrow Plastic DIP
(derate 13.33mW/°C above +70°C) 1.07W
24-Pin Wide Plastic DIP
(derate 14.29mW/°C above +70°C).....1.14W
24-Pin SO (derate 11.76mW/°C above +70°C).....941mW
24-Pin SSOP (derate 8.00mW/°C above +70°C) 640mW
28-Pin SO (derate 12.50mW/°C above +70°C).....1W
28-Pin SSOP (derate 9.52mW/°C above +70°C) 762mW
Operating Temperature Ranges
MAX2__EC__ .....0°C to +70°C
MAX2__EE__ .....-40°C to +85°C
Storage Temperature Range .....-65°C to +165°C
Lead Temperature (soldering, 10sec) .....+300°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(VCC = +5V ±10% for MAX202E/206E/208E/211E/213E/232E/241E; VCC = +5V ±5% for MAX203E/205E/207E; C1–C4 = 0.1µF for MAX202E/206E/207E/208E/211E/213E; C1–C4 = 1µF for MAX232E/241E; TA = TMIN to TMAX; unless otherwise noted. Typical values are at TA = +25°C.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
DC CHARACTERISTICS							
VCC Supply Current	ICC	No load, TA = +25°C	MAX202E/203E		8	15	mA
			MAX205E–208E		11	20	
			MAX211E/213E		14	20	
			MAX232E		5	10	
			MAX241E		7	15	
Shutdown Supply Current		TA = +25°C, Figure 1	MAX205E/206E		1	10	µA
			MAX211E/241E		1	10	
			MAX213E		15	50	
LOGIC							
Input Pull-Up Current		T_IN = 0V (MAX205E–208E/211E/213E/241E)			15	200	µA
Input Leakage Current		T_IN = 0V to VCC (MAX202E/203E/232E)				±10	µA
Input Threshold Low	VIL	T_IN; EN, $\overline{SHDN}$ (MAX213E) or $\overline{EN}$, SHDN (MAX205E–208E/211E/241E)				0.8	V
Input Threshold High	VIH	T_IN		2.0			V
		EN, $\overline{SHDN}$ (MAX213E) or $\overline{EN}$, SHDN (MAX205E–208E/211E/241E)		2.4			
Output Voltage Low	VOL	R_OUT; IOUT = 3.2mA (MAX202E/203E/232E) or IOUT = 1.6mA (MAX205E/208E/211E/213E/241E)				0.4	V
Output Voltage High	VOH	R_OUT; IOUT = -1.0mA		3.5	VCC - 0.4		V
Output Leakage Current		$\overline{EN}$ = VCC, EN = 0V, 0V ≤ ROUT ≤ VCC, MAX205E–208E/211E/213E/241E outputs disabled			±0.05	±10	µA

ELECTRICAL CHARACTERISTICS (continued)

(V_{CC} = +5V ±10% for MAX202E/206E/208E/211E/213E/232E/241E; V_{CC} = +5V ±5% for MAX203E/205E/207E; C1–C4 = 0.1µF for MAX202E/206E/207E/208E/211E/213E; C1–C4 = 1µF for MAX232E/241E; T_A = T_{MIN} to T_{MAX}; unless otherwise noted. Typical values are at T_A = +25°C.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
EIA/TIA-232E RECEIVER INPUTS							
Input Voltage Range				-30		30	V
Input Threshold Low		T_A = +25°C, V_{CC} = 5V	All parts, normal operation	0.8	1.2		V
			MAX213E, $\overline{SHDN}$ = 0V, EN = V_{CC}	0.6	1.5		
Input Threshold High		T_A = +25°C, V_{CC} = 5V	All parts, normal operation		1.7	2.4	V
			MAX213E (R4, R5), $\overline{SHDN}$ = 0V, EN = V_{CC}		1.5	2.4	
Input Hysteresis		V_{CC} = 5V, no hysteresis in shutdown		0.2	0.5	1.0	V
Input Resistance		T_A = +25°C, V_{CC} = 5V		3	5	7	kΩ
EIA/TIA-232E TRANSMITTER OUTPUTS							
Output Voltage Swing		All drivers loaded with 3kΩ to ground (Note 1)		±5	±9		V
Output Resistance		V_{CC} = V+ = V- = 0V, V_{OUT} = ±2V		300			Ω
Output Short-Circuit Current					±10	±60	mA
TIMING CHARACTERISTICS							
Maximum Data Rate		R_L = 3kΩ to 7kΩ, C_L = 50pF to 1000pF, one transmitter switching		120			kbps
Receiver Propagation Delay	t_{PLHR}, t_{PHLR}	C_L = 150pF	All parts, normal operation		0.5	10	µs
			MAX213E (R4, R5), $\overline{SHDN}$ = 0V, EN = V_{CC}		4	40	
Receiver Output Enable Time		MAX205E/206E/211E/213E/241E normal operation, Figure 2			600		ns
Receiver Output Disable Time		MAX205E/206E/211E/213E/241E normal operation, Figure 2			200		ns
Transmitter Propagation Delay	t_{PLHT}, t_{PHLT}	R_L = 3kΩ, C_L = 2500pF, all transmitters loaded			2		µs
Transition-Region Slew Rate		T_A = +25°C, V_{CC} = 5V, R_L = 3kΩ to 7kΩ, C_L = 50pF to 1000pF, measured from -3V to +3V or +3V to -3V, Figure 3		3	6	30	V/µs
ESD PERFORMANCE: TRANSMITTER OUTPUTS, RECEIVER INPUTS							
ESD-Protection Voltage		Human Body Model			±15		kV
		IEC1000-4-2, Contact Discharge			±8		
		IEC1000-4-2, Air-Gap Discharge			±15		

Note 1: MAX211EE_ _ tested with V_{CC} = +5V ±5%.

ELECTRICAL CHARACTERISTICS (continued)

(V_{CC} = +5V ±10% for MAX202E/206E/208E/211E/213E/232E/241E; V_{CC} = +5V ±5% for MAX203E/205E/207E; C1–C4 = 0.1µF for MAX202E/206E/207E/208E/211E/213E; C1–C4 = 1µF for MAX232E/241E; T_A = T_{MIN} to T_{MAX}; unless otherwise noted. Typical values are at T_A = +25°C.)

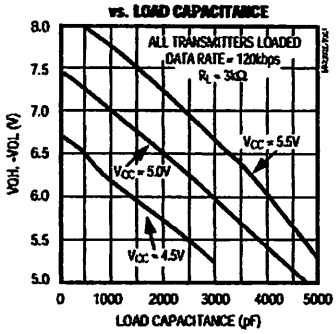
PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
EIA/TIA-232E RECEIVER INPUTS							
Input Voltage Range				-30		30	V
Input Threshold Low		T_A = +25°C, V_{CC} = 5V	All parts, normal operation	0.8	1.2		V
			MAX213E, $\overline{SHDN}$ = 0V, EN = V_{CC}	0.6	1.5		
Input Threshold High		T_A = +25°C, V_{CC} = 5V	All parts, normal operation		1.7	2.4	V
			MAX213E (R4, R5), $\overline{SHDN}$ = 0V, EN = V_{CC}		1.5	2.4	
Input Hysteresis		V_{CC} = 5V, no hysteresis in shutdown		0.2	0.5	1.0	V
Input Resistance		T_A = +25°C, V_{CC} = 5V		3	5	7	kΩ
EIA/TIA-232E TRANSMITTER OUTPUTS							
Output Voltage Swing		All drivers loaded with 3kΩ to ground (Note 1)		±5	±9		V
Output Resistance		V_{CC} = V+ = V- = 0V, V_{OUT} = ±2V		300			Ω
Output Short-Circuit Current					±10	±60	mA
TIMING CHARACTERISTICS							
Maximum Data Rate		R_L = 3kΩ to 7kΩ, C_L = 50pF to 1000pF, one transmitter switching		120			kbps
Receiver Propagation Delay	t_{PLHR}, t_{PHLR}	C_L = 150pF	All parts, normal operation		0.5	10	µs
			MAX213E (R4, R5), $\overline{SHDN}$ = 0V, EN = V_{CC}		4	40	
Receiver Output Enable Time		MAX205E/206E/211E/213E/241E normal operation, Figure 2			600		ns
Receiver Output Disable Time		MAX205E/206E/211E/213E/241E normal operation, Figure 2			200		ns
Transmitter Propagation Delay	t_{PLHT}, t_{PHLT}	R_L = 3kΩ, C_L = 2500pF, all transmitters loaded			2		µs
Transition-Region Slew Rate		T_A = +25°C, V_{CC} = 5V, R_L = 3kΩ to 7kΩ, C_L = 50pF to 1000pF, measured from -3V to +3V or +3V to -3V, Figure 3		3	6	30	V/µs
ESD PERFORMANCE: TRANSMITTER OUTPUTS, RECEIVER INPUTS							
ESD-Protection Voltage		Human Body Model			±15		kV
		IEC1000-4-2, Contact Discharge			±8		
		IEC1000-4-2, Air-Gap Discharge			±15		

Note 1: MAX211EE_ _ tested with V_{CC} = +5V ±5%.

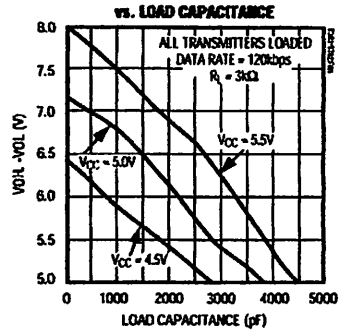
Typical Operating Characteristics

(Typical Operating Circuits, V_{CC} = +5V, T_A = +25°C, unless otherwise noted.)

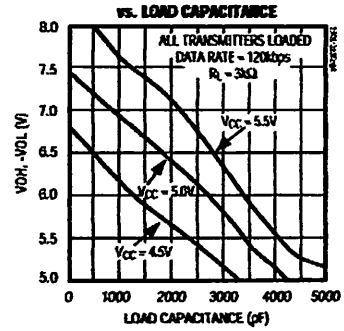
MAX232E
TRANSMITTER OUTPUT VOLTAGE
vs. LOAD CAPACITANCE



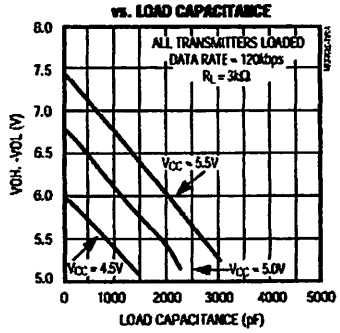
MAX202E/MAX203E
TRANSMITTER OUTPUT VOLTAGE
vs. LOAD CAPACITANCE



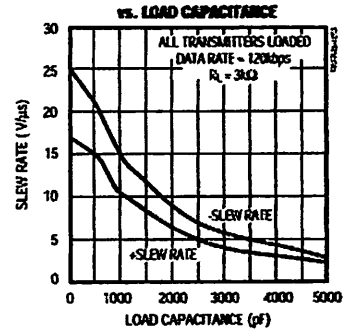
MAX241E
TRANSMITTER OUTPUT VOLTAGE
vs. LOAD CAPACITANCE



MAX211E/MAX213E
TRANSMITTER OUTPUT VOLTAGE
vs. LOAD CAPACITANCE



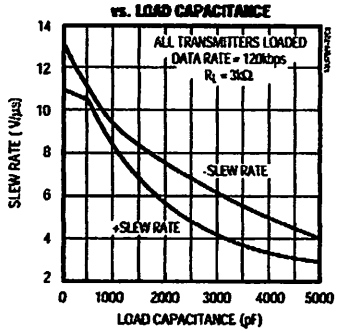
MAX211E/MAX213E/MAX241E
TRANSMITTER SLEW RATE
vs. LOAD CAPACITANCE



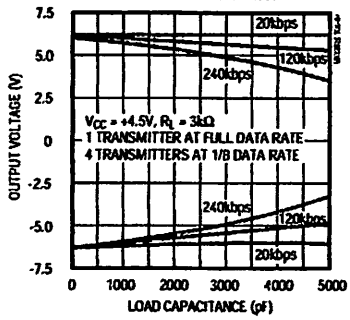
Typical Operating Characteristics (continued)

(Typical Operating Circuits, V_{CC} = +5V, T_A = +25°C, unless otherwise noted.)

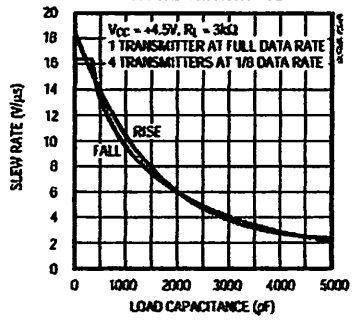
MAX202E/MAX203E/MAX232E
TRANSMITTER SLEW RATE
vs. LOAD CAPACITANCE



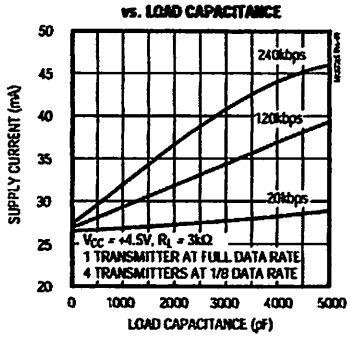
MAX205E–MAX208E
TRANSMITTER OUTPUT VOLTAGE
vs. LOAD CAPACITANCE



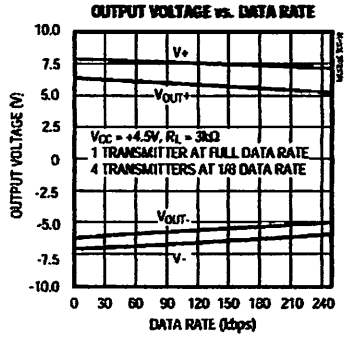
MAX205E–MAX208E
TRANSMITTER SLEW RATE
vs. LOAD CAPACITANCE



MAX205E–MAX208E
SUPPLY CURRENT
vs. LOAD CAPACITANCE



MAX205E–MAX208E
OUTPUT VOLTAGE vs. DATA RATE



Pin Descriptions

MAX202E/MAX232E

PIN		NAME	FUNCTION
DIP/SO	LCC		
1, 3	2, 4	C1+, C1-	Terminals for positive charge-pump capacitor
2	3	V+	+2VCC voltage generated by the charge pump
4, 5	5, 7	C2+, C2-	Terminals for negative charge-pump capacitor
6	8	V-	-2VCC voltage generated by the charge pump
7, 14	9, 18	T_OUT	RS-232 Driver Outputs
8, 13	10, 17	R_IN	RS-232 Receiver Outputs
9, 12	12, 15	R_OUT	RS-232 Receiver Outputs
10, 11	13, 14	T_IN	RS-232 Driver Inputs
15	19	GND	Ground
16	20	VCC	+4.5V to +5.5V Supply-Voltage Input
—	1, 6, 11, 16	N.C.	No Connect—not internally connected.

MAX203E

PIN		NAME	FUNCTION
DIP	SO		
1, 2	1, 2	T_IN	RS-232 Driver Inputs
3, 20	3, 20	R_OUT	RS-232 Receiver Outputs
4,19	4, 19	R_IN	RS-232 Receiver Inputs
5,18	5, 18	T_OUT	RS-232 Transmitter Outputs
6, 9	6, 9	GND	Ground
7	7	VCC	+4.5V to +5.5V Supply-Voltage Input
8	13	C1+	Make no connection to this pin.
10, 16	11, 16	C2-	Connect pins together.
12, 17	10, 17	V-	-2VCC voltage generated by the charge pump. Connect pins together.
13	14	C1-	Make no connection to this pin.
14	8	V+	+2VCC voltage generated by the charge pump
11, 15	12, 15	C2+	Connect pins together.

MAX205E

PIN	NAME	FUNCTION
1–4, 19	T_OUT	RS-232 Driver Outputs
5, 10, 13, 18, 24	R_IN	RS-232 Receiver Inputs
6, 9, 14, 17, 23	R_OUT	TTL/CMOS Receiver Outputs. All receivers are inactive in shutdown.
7, 8, 15, 16, 22	T_IN	TTL/CMOS Driver Inputs. Internal pull-ups to VCC.
11	GND	Ground
12	VCC	+4.75V to +5.25V Supply Voltage
20	$\overline{EN}$	Receiver Enable—active low
21	SHDN	Shutdown Control—active high

Pin Descriptions (continued)

MAX208E

PIN	NAME	FUNCTION
1, 2, 3, 24	T_OUT	RS-232 Driver Outputs
4, 16, 23	R_IN	RS-232 Receiver Inputs
5, 17, 22	R_OUT	TTL/CMOS Receiver Outputs. All receivers are inactive in shutdown.
6, 7, 18, 19	T_IN	TTL/CMOS Driver Inputs. Internal pull-ups to V_{CC}.
8	GND	Ground
9	V_{CC}	+4.5V to +5.5V Supply Voltage
10, 12	C1+, C1-	Terminals for positive charge-pump capacitor
11	V+	+2V_{CC} generated by the charge pump
13, 14	C2+, C2-	Terminals for negative charge-pump capacitor
15	V-	-2V_{CC} generated by the charge pump
20	$\overline{EN}$	Receiver Enable—active low
21	SHDN	Shutdown Control—active high

MAX207E

PIN	NAME	FUNCTION
1, 2, 3, 20, 24	T_OUT	RS-232 Driver Outputs
4, 16, 23	R_IN	RS-232 Receiver Inputs
5, 17, 22	R_OUT	TTL/CMOS Receiver Outputs. All receivers are inactive in shutdown.
6, 7, 18, 19, 21	T_IN	TTL/CMOS Driver Inputs. Internal pull-ups to V_{CC}.
8	GND	Ground
9	V_{CC}	+4.75V to +5.25V Supply Voltage
10, 12	C1+, C1-	Terminals for positive charge-pump capacitor
11	V+	+2V_{CC} generated by the charge pump
13, 14	C2+, C2-	Terminals for negative charge-pump capacitor
15	V-	-2V_{CC} generated by the charge pump

MAX208E

PIN	NAME	FUNCTION
1, 2, 20, 24	T_OUT	RS-232 Driver Outputs
3, 7, 16, 23	R_IN	RS-232 Receiver Inputs
4, 6, 17, 22	R_OUT	TTL/CMOS Receiver Outputs. All receivers are inactive in shutdown.
5, 18, 19, 21	T_IN	TTL/CMOS Driver Inputs. Internal pull-ups to V_{CC}.
8	GND	Ground
9	V_{CC}	+4.5V to +5.5V Supply Voltage
10, 12	C1+, C1-	Terminals for positive charge-pump capacitor
11	V+	+2V_{CC} generated by the charge pump
13, 14	C2+, C2-	Terminals for negative charge-pump capacitor
15	V-	-2V_{CC} generated by the charge pump

Pin Descriptions (continued)

MAX211E/MAX213E/MAX241E

PIN	NAME	FUNCTION
1, 2, 3, 28	T_OUT	RS-232 Driver Outputs
4, 9, 18, 23, 27	R_IN	RS-232 Receiver Inputs
5, 8, 19, 22, 26	R_OUT	TTL/CMOS Receiver Outputs. For the MAX213E, receivers R4 and R5 are active in shutdown mode when EN = 1. For the MAX211E and MAX241E, all receivers are inactive in shutdown.
6, 7, 20, 21	T_IN	TTL/CMOS Driver Inputs. Only the MAX211E, MAX213E, and MAX241E have internal pull-ups to V_{CC}.
10	GND	Ground
11	V_{CC}	+4.5V to +5.5V Supply Voltage
12, 14	C1+, C1-	Terminals for positive charge-pump capacitor
13	V+	$+2V_{CC}$ voltage generated by the charge pump
15, 16	C2+, C2-	Terminals for negative charge-pump capacitor
17	V-	$-2V_{CC}$ voltage generated by the charge pump
24	$\overline{EN}$	Receiver Enable—active low (MAX211E, MAX241E)
	EN	Receiver Enable—active high (MAX213E)
25	SHDN	Shutdown Control—active high (MAX211E, MAX241E)
	$\overline{SHDN}$	Shutdown Control—active low (MAX213E)

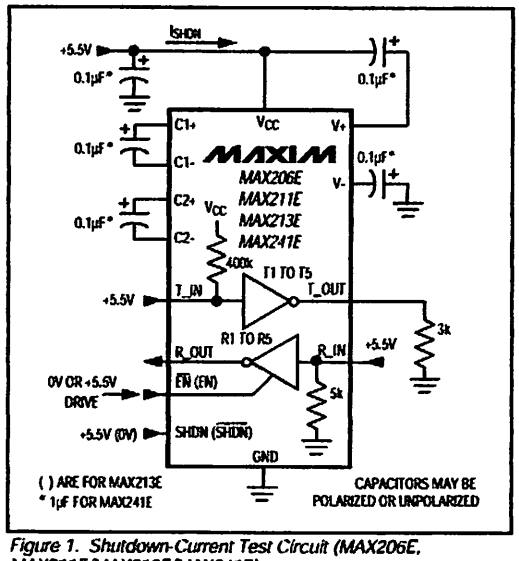


Figure 1. Shutdown-Current Test Circuit (MAX206E, MAX211E/MAX213E/MAX241E)

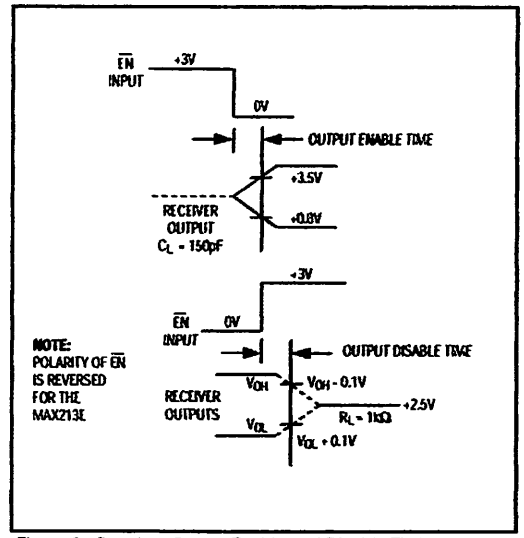


Figure 2. Receiver Output Enable and Disable Timing (MAX205E/MAX206E/MAX211E/MAX213E/MAX241E)

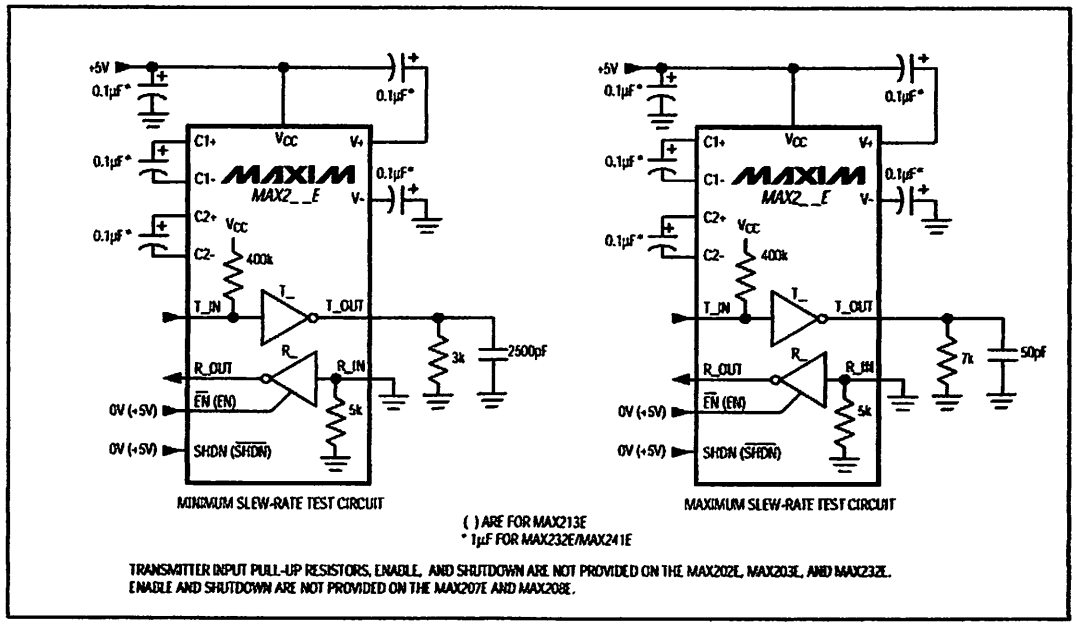


Figure 3. Transition Slew-Rate Circuit

Detailed Description

The MAX202E–MAX213E, MAX232E/MAX241E consist of three sections: charge-pump voltage converters, drivers (transmitters), and receivers. These E versions provide extra protection against ESD. They survive ±15kV discharges to the RS-232 inputs and outputs, tested using the Human Body Model. When tested according to IEC1000-4-2, they survive ±8kV contact-discharges and ±15kV air-gap discharges. The rugged E versions are intended for use in harsh environments or applications where the RS-232 connection is frequently changed (such as notebook computers). The standard (non-"E") MAX202, MAX203, MAX205–MAX208, MAX211, MAX213, MAX232, and MAX241 are recommended for applications where cost is critical.

+5V to ±10V Dual Charge-Pump Voltage Converter

The +5V to ±10V conversion is performed by dual charge-pump voltage converters (Figure 4). The first charge-pump converter uses capacitor C1 to double the +5V into +10V, storing the +10V on the output filter capacitor, C3. The second uses C2 to invert the +10V into -10V, storing the -10V on the V- output filter capacitor, C4.

In shutdown mode, V+ is internally connected to VCC by a 1kΩ pull-down resistor, and V- is internally connected to ground by a 1kΩ pull-up resistor.

RS-232 Drivers

With VCC = 5V, the typical driver output voltage swing is ±8V when loaded with a nominal 5kΩ RS-232 receiver. The output swing is guaranteed to meet EIA/TIA-232E and V.28 specifications that call for ±5V minimum output levels under worst-case conditions. These include a 3kΩ load, minimum VCC, and maximum operating temperature. The open-circuit output voltage swings from (V+ - 0.6V) to V-.

Input thresholds are CMOS/TTL compatible. The unused drivers' inputs on the MAX205E–MAX208E, MAX211E, MAX213E, and MAX241E can be left unconnected because 400kΩ pull-up resistors to VCC are included on-chip. Since all drivers invert, the pull-up resistors force the unused drivers' outputs low. The MAX202E, MAX203E, and MAX232E do not have pull-up resistors on the transmitter inputs.

When in low-power shutdown mode, the MAX205E/MAX206E/MAX211E/MAX213E/MAX241E driver outputs are turned off and draw only leakage currents—even if they are back-driven with voltages between 0V and 12V. Below -0.5V in shutdown, the transmitter output is diode-clamped to ground with a 1kΩ series impedance.

RS-232 Receivers

The receivers convert the RS-232 signals to CMOS-logic output levels. The guaranteed 0.8V and 2.4V receiver input thresholds are significantly tighter than the ±3V thresholds required by the EIA/TIA-232E specification. This allows the receiver inputs to respond to TTL/CMOS-logic levels, as well as RS-232 levels.

The guaranteed 0.8V input low threshold ensures that receivers shorted to ground have a logic 1 output. The 5kΩ input resistance to ground ensures that a receiver with its input left open will also have a logic 1 output.

Receiver inputs have approximately 0.5V hysteresis. This provides clean output transitions, even with slow rise/fall-time signals with moderate amounts of noise and ringing.

In shutdown, the MAX213E's R4 and R5 receivers have no hysteresis.

Shutdown and Enable Control (MAX205E/MAX206E/MAX211E/MAX213E/MAX241E)

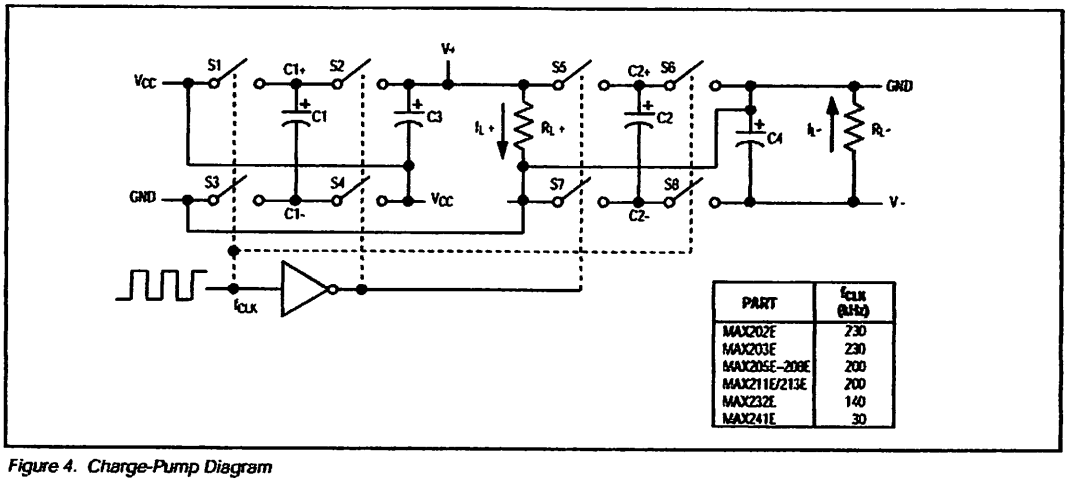
In shutdown mode, the charge pumps are turned off, V+ is pulled down to V_{CC}, V- is pulled to ground, and the transmitter outputs are disabled. This reduces supply current typically to 1µA (15µA for the MAX213E). The time required to exit shutdown is under 1ms, as shown in Figure 5.

Receivers

All MAX213E receivers, except R4 and R5, are put into a high-impedance state in shutdown mode (see Tables 1a and 1b). The MAX213E's R4 and R5 receivers still function in shutdown mode. These two awake-in-shutdown receivers can monitor external activity while maintaining minimal power consumption.

The enable control is used to put the receiver outputs into a high-impedance state, to allow wire-OR connection of two EIA/TIA-232E ports (or ports of different types) at the UART. It has no effect on the RS-232 drivers or the charge pumps.

Note: The enable control pin is active low for the MAX211E/MAX241E ($\overline{EN}$), but is active high for the MAX213E (EN). The shutdown control pin is active high for the MAX205E/MAX206E/MAX211E/MAX241E (SHDN), but is active low for the MAX213E ($\overline{SHDN}$).



PART	f_{CLK} (kHz)
MAX202E	230
MAX203E	230
MAX205E–208E	200
MAX211E/213E	200
MAX232E	140
MAX241E	30

Figure 4. Charge-Pump Diagram

The MAX213E's receiver propagation delay is typically 0.5µs in normal operation. In shutdown mode, propagation delay increases to 4µs for both rising and falling transitions. The MAX213E's receiver inputs have approximately 0.5V hysteresis, except in shutdown, when receivers R4 and R5 have no hysteresis.

When entering shutdown with receivers active, R4 and R5 are not valid until 80µs after $\overline{SHDN}$ is driven low. When coming out of shutdown, all receiver outputs are invalid until the charge pumps reach nominal voltage levels (less than 2ms when using 0.1µF capacitors).

±15kV ESD Protection

As with all Maxim devices, ESD-protection structures are incorporated on all pins to protect against electrostatic discharges encountered during handling and assembly. The driver outputs and receiver inputs have extra protection against static electricity. Maxim's engineers developed state-of-the-art structures to protect these pins against ESD of ±15kV without damage. The ESD structures withstand high ESD in all states: normal operation, shutdown, and powered down. After an ESD event, Maxim's E versions keep working without latchup, whereas competing RS-232 products can latch and must be powered down to remove latchup.

ESD protection can be tested in various ways; the transmitter outputs and receiver inputs of this product family are characterized for protection to the following limits:

1) ±15kV using the Human Body Model
2) ±8kV using the contact-discharge method specified in IEC1000-4-2
3) ±15kV using IEC1000-4-2's air-gap method.

ESD Test Conditions

ESD performance depends on a variety of conditions. Contact Maxim for a reliability report that documents test set-up, test methodology, and test results.

Human Body Model

Figure 6a shows the Human Body Model, and Figure 6b shows the current waveform it generates when discharged into a low impedance. This model consists of a 100pF capacitor charged to the ESD voltage of interest, which is then discharged into the test device through a 1.5kΩ resistor.

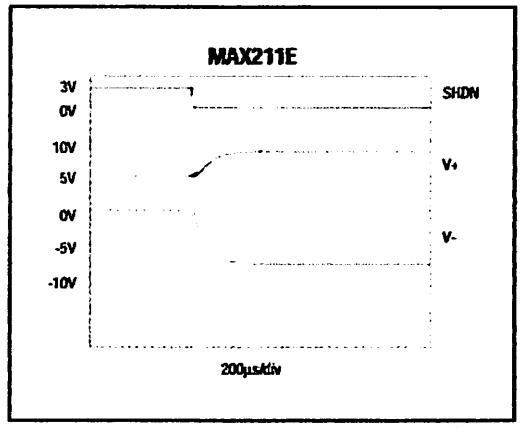


Figure 5. MAX211E V+ and V- when Exiting Shutdown (0.1µF capacitors)

Table 1a. MAX205E/MAX206E/MAX211E/ MAX241E Control Pin Configurations

SHDN	EN	OPERATION STATUS	Tx	Rx
0	0	Normal Operation	All Active	All Active
0	1	Normal Operation	All Active	All High-Z
1	X	Shutdown	All High-Z	All High-Z

X = Don't Care

Table 1b. MAX213E Control Pin Configurations

SHDN	EN	OPERATION STATUS	Tx 1–4	Rx	
				1–3	4, 5
0	0	Shutdown	All High-Z	High-Z	High-Z
0	1	Shutdown	All High-Z	High-Z	Active*
1	0	Normal Operation	All Active	High-Z	High-Z
1	1	Normal Operation	All Active	Active	Active

**Active = active with reduced performance*

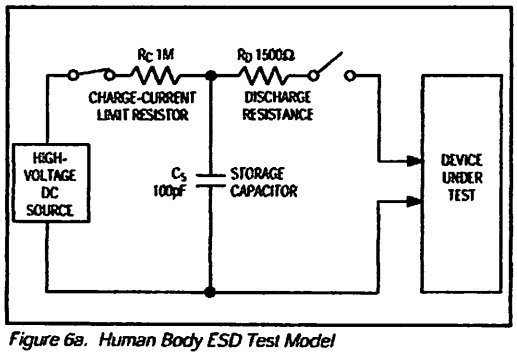


Figure 6a. Human Body ESD Test Model

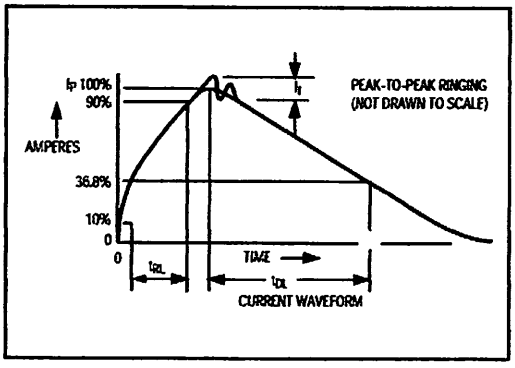


Figure 6b. Human Body Model Current Waveform

IEC1000-4-2

The IEC1000-4-2 standard covers ESD testing and performance of finished equipment; it does not specifically refer to integrated circuits. The MAX202E/MAX203E–MAX213E, MAX232E/MAX241E help you design equipment that meets level 4 (the highest level) of IEC1000-4-2, without the need for additional ESD-protection components.

The major difference between tests done using the Human Body Model and IEC1000-4-2 is higher peak current in IEC1000-4-2, because series resistance is lower in the IEC1000-4-2 model. Hence, the ESD withstand voltage measured to IEC1000-4-2 is generally lower than that measured using the Human Body Model. Figure 7b shows the current waveform for the 8kV IEC1000-4-2 level-four ESD contact-discharge test.

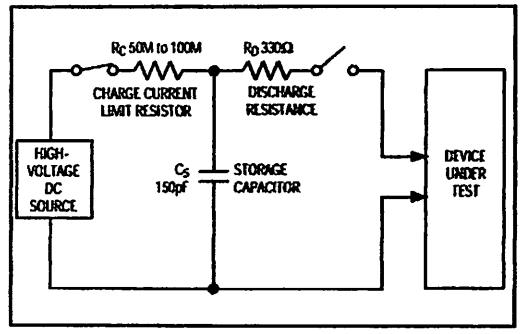


Figure 7a. IEC1000-4-2 ESD Test Model

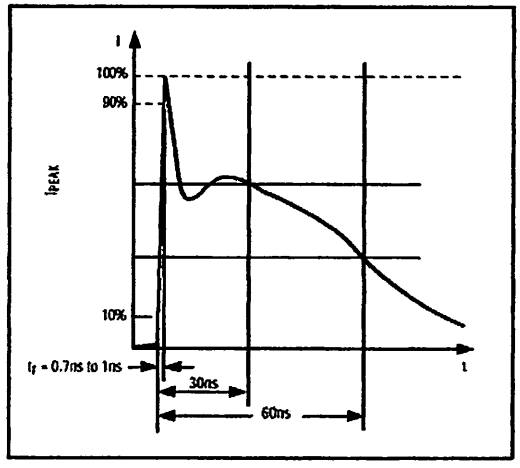


Figure 7b. IEC1000-4-2 ESD Generator Current Waveform

The air-gap test involves approaching the device with a charged probe. The contact-discharge method connects the probe to the device before the probe is energized.

Machine Model

The Machine Model for ESD tests all pins using a 200pF storage capacitor and zero discharge resistance. Its objective is to emulate the stress caused by contact that occurs with handling and assembly during manufacturing. Of course, all pins require this protection during manufacturing, not just RS-232 inputs and outputs. Therefore, after PC board assembly, the Machine Model is less relevant to I/O ports.

Applications Information

Capacitor Selection

The capacitor type used for C1–C4 is not critical for proper operation. The MAX202E, MAX206–MAX208E, MAX211E, and MAX213E require 0.1µF capacitors, and the MAX232E and MAX241E require 1µF capacitors, although in all cases capacitors up to 10µF can be used without harm. Ceramic, aluminum-electrolytic, or tantalum capacitors are suggested for the 1µF capacitors, and ceramic dielectrics are suggested for the 0.1µF capacitors. When using the minimum recommended capacitor values, make sure the capacitance value does not degrade excessively as the operating temperature varies. If in doubt, use capacitors with a larger (e.g., 2x) nominal value. The capacitors' effective series resistance (ESR), which usually rises at low temperatures, influences the amount of ripple on V+ and V-.

Use larger capacitors (up to 10µF) to reduce the output impedance at V+ and V-. This can be useful when "stealing" power from V+ or from V-. The MAX203E and MAX205E have internal charge-pump capacitors.

Bypass V_{CC} to ground with at least 0.1µF. In applications sensitive to power-supply noise generated by the charge pumps, decouple V_{CC} to ground with a capacitor the same size as (or larger than) the charge-pump capacitors (C1–C4).

V+ and V- as Power Supplies

A small amount of power can be drawn from V+ and V-, although this will reduce both driver output swing and noise margins. Increasing the value of the charge-pump capacitors (up to 10µF) helps maintain performance when power is drawn from V+ or V-.

Driving Multiple Receivers

Each transmitter is designed to drive a single receiver. Transmitters can be paralleled to drive multiple receivers.

Driver Outputs when Exiting Shutdown

The driver outputs display no ringing or undesirable transients as they come out of shutdown.

High Data Rates

These transceivers maintain the RS-232 ±5.0V minimum driver output voltages at data rates of over 120kbps. For data rates above 120kbps, refer to the Transmitter Output Voltage vs. Load Capacitance graphs in the *Typical Operating Characteristics*. Communication at these high rates is easier if the capacitive loads on the transmitters are small; i.e., short cables are best.

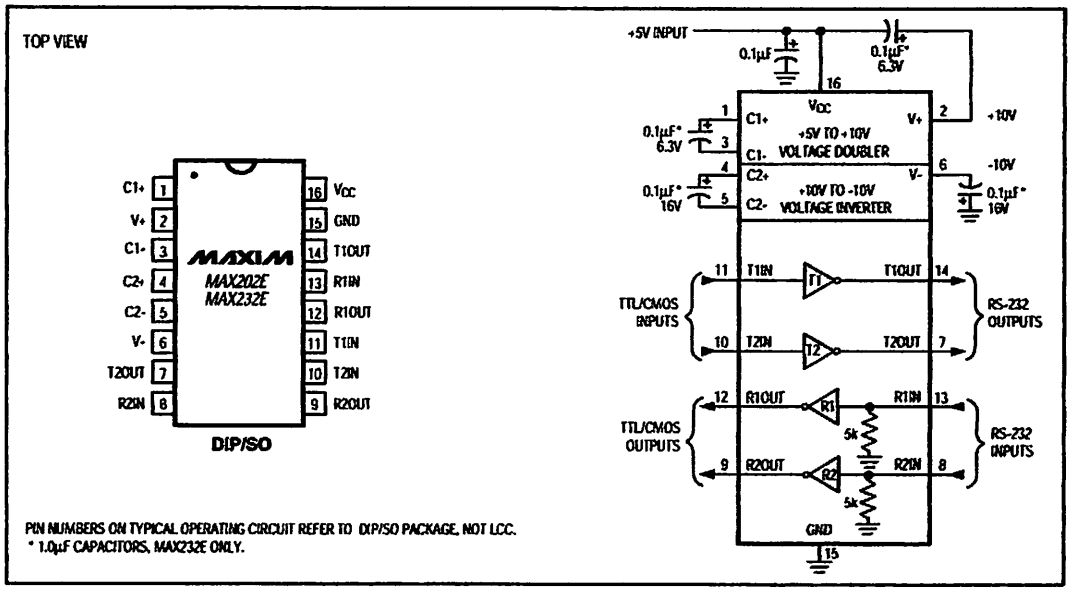
Table 2. Summary of EIA/TIA-232E, V.28 Specifications

PARAMETER		CONDITIONS	EIA/TIA-232E, V.28 SPECIFICATIONS
Driver Output Voltage	0 Level	3kΩ to 7kΩ load	+5V to +15V
	1 Level	3kΩ to 7kΩ load	-5V to -15V
Driver Output Level, Max		No load	±25V
Data Rate		3kΩ ≤ R_L ≤ 7kΩ, C_L ≤ 2500pF	Up to 20kbps
Receiver Input Voltage	0 Level		+3V to +15V
	1 Level		-3V to -15V
Receiver Input Level			±25V
Instantaneous Slew Rate, Max		3kΩ ≤ R_L ≤ 7kΩ, C_L ≤ 2500pF	30V/µs
Driver Output Short-Circuit Current, Max			100mA
Transition Rate on Driver Output		V.28	1ms or 3% of the period
		EIA/TIA-232E	4% of the period
Driver Output Resistance		-2V < V_{OUT} < +2V	300Ω

Table 3. DB9 Cable Connections Commonly Used for EIA/TIAE-232E and V.24 Asynchronous Interfaces

PIN	CONNECTION	
1	Received Line Signal Detector (sometimes called Carrier Detect, DCD)	Handshake from DCE
2	Receive Data (RD)	Data from DCE
3	Transmit Data (TD)	Data from DTE
4	Data Terminal Ready	Handshake from DTE
5	Signal Ground	Reference point for signals
6	Data Set Ready (DSR)	Handshake from DCE
7	Request to Send (RTS)	Handshake from DTE
8	Clear to Send (CTS)	Handshake from DCE
9	Ring Indicator	Handshake from DCE

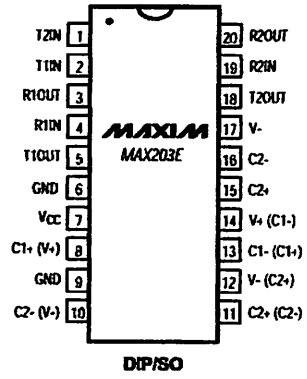
Pin Configurations and Typical Operating Circuits (continued)



PIN NUMBERS ON TYPICAL OPERATING CIRCUIT REFER TO DIP/SO PACKAGE, NOT LCC.
* 1.0µF CAPACITORS, MAX232E ONLY.

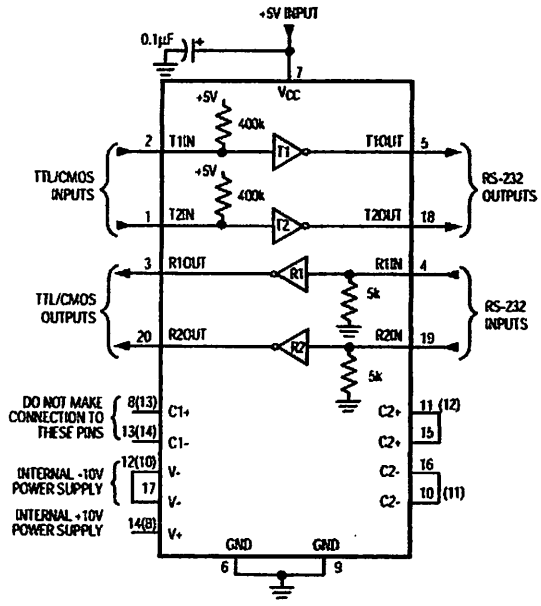
Pin Configurations and Typical Operating Circuits (continued)

TOP VIEW



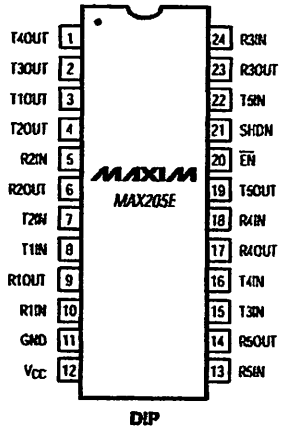
DIP/SO

PIN NUMBERS IN ( ) ARE FOR SO PACKAGE.

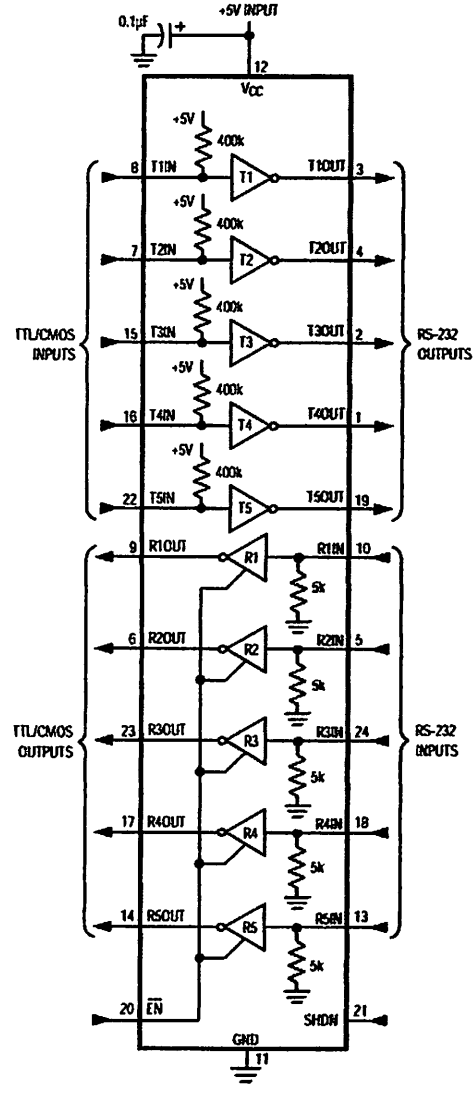


Pin Configurations and Typical Operating Circuits (continued)

TOP VIEW

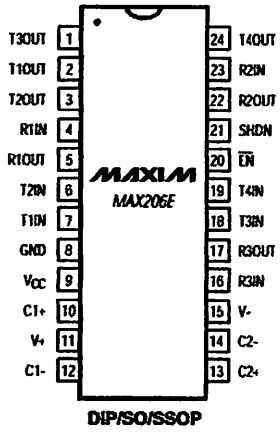


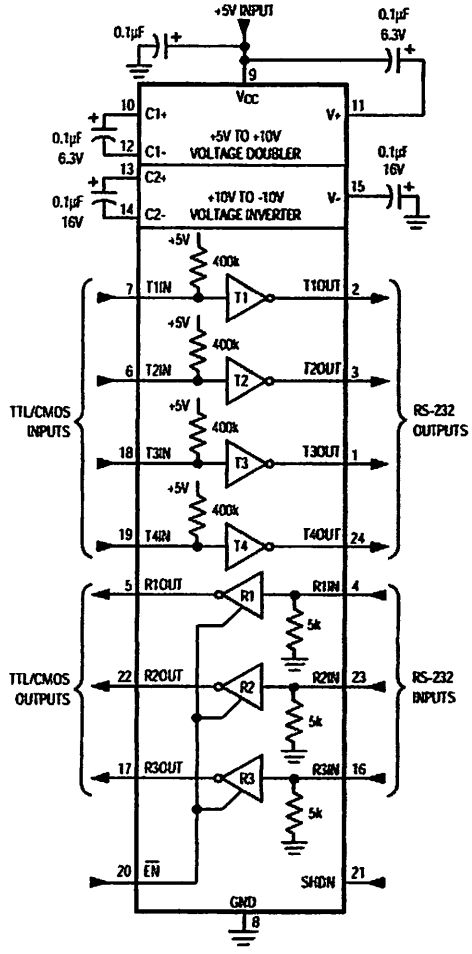
DIP



Pin Configurations and Typical Operating Circuits (continued)

TOP VIEW

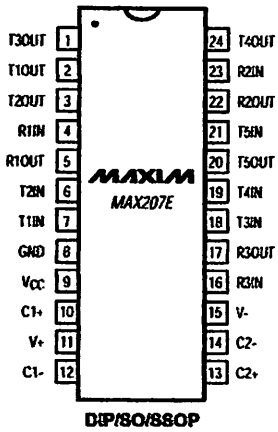




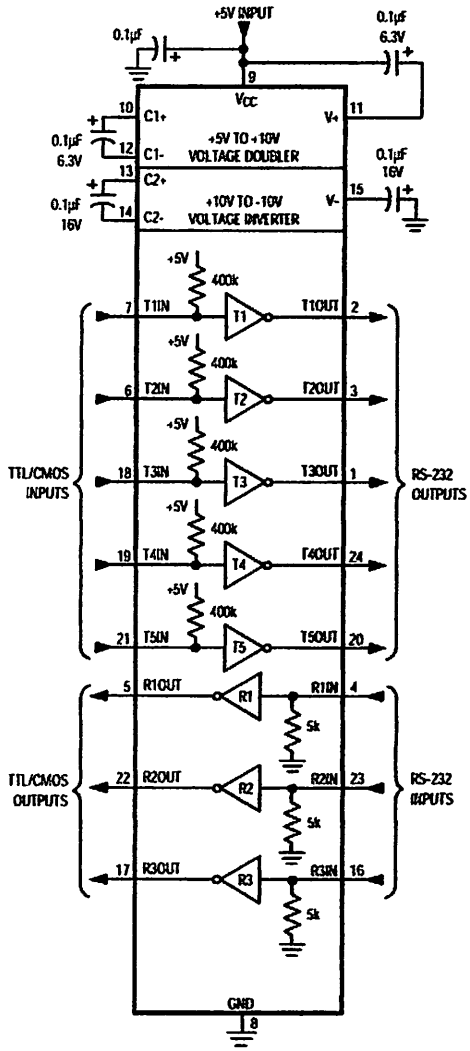
±15kV ESD-Protected, +5V RS-232 Transceivers

Pin Configurations and Typical Operating Circuits (continued)

TOP VIEW

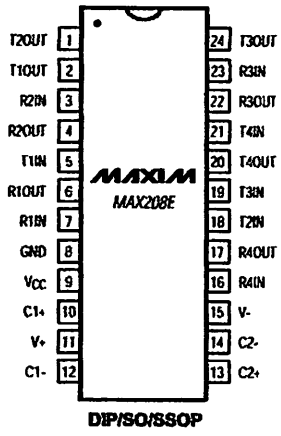


DIP/SO/SSOP

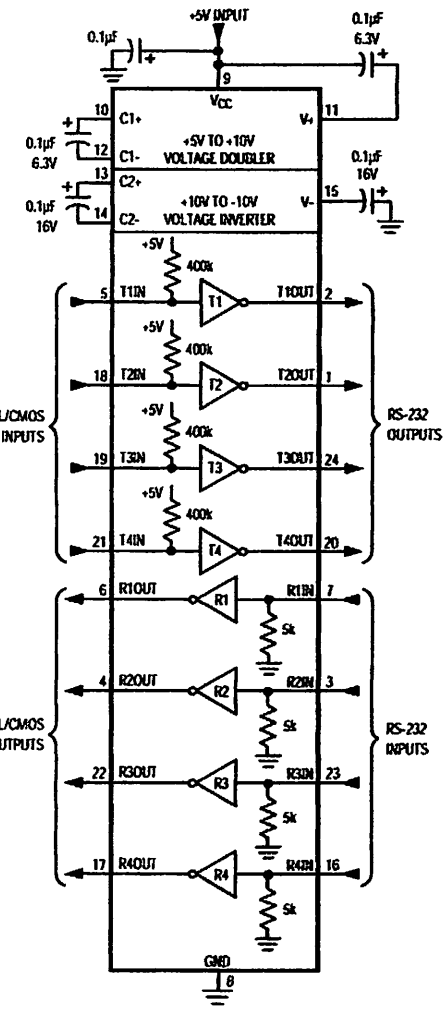


Pin Configurations and Typical Operating Circuits (continued)

TOP VIEW

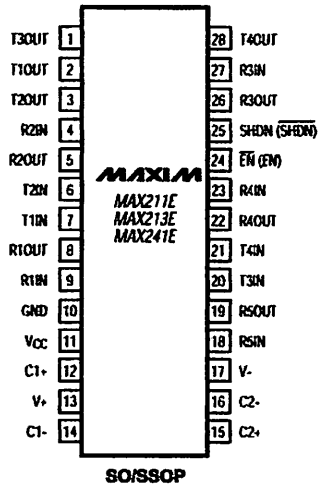


DIP/SO/SSOP

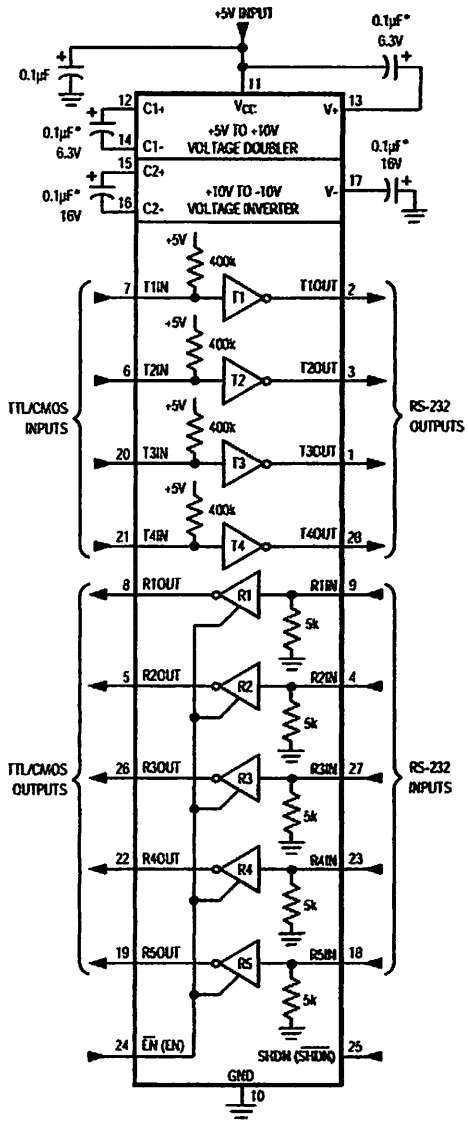


Pin Configurations and Typical Operating Circuits (continued)

TOP VIEW



SO/SSOP



() ARE FOR MAX213E ONLY
* 1.0µF CAPACITORS, MAX241E ONLY

Ordering Information

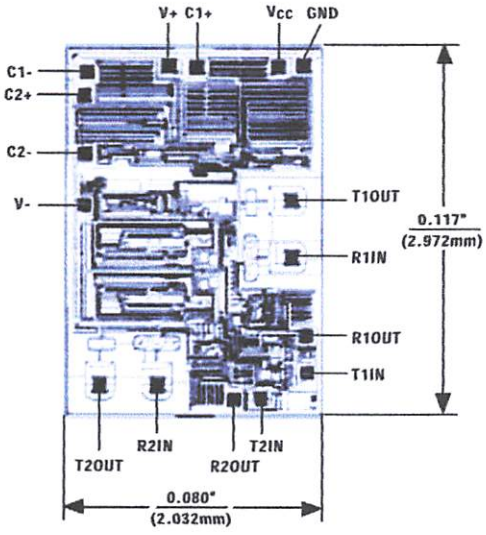
PART	TEMP. RANGE	PIN-PACKAGE
MAX202ECPE	0°C to +70°C	16 Plastic DIP
MAX202ECSE	0°C to +70°C	16 Narrow SO
MAX202ECWE	0°C to +70°C	16 Wide SO
MAX202EC/D	0°C to +70°C	Dice*
MAX202EEPE	-40°C to +85°C	16 Plastic DIP
MAX202EESE	-40°C to +85°C	16 Narrow SO
MAX202EEWE	-40°C to +85°C	16 Wide SO
MAX203ECPP	0°C to +70°C	20 Plastic DIP
MAX203ECWP	0°C to +70°C	20 SO
MAX203EEPP	-40°C to +85°C	20 Plastic DIP
MAX203EEWP	-40°C to +85°C	20 SO
MAX205ECPG	0°C to +70°C	24 Wide Plastic DIP
MAX205EEPG	-40°C to +85°C	24 Wide Plastic DIP
MAX206ECNG	0°C to +70°C	24 Narrow Plastic DIP
MAX206ECWG	0°C to +70°C	24 SO
MAX206ECAG	0°C to +70°C	24 SSOP
MAX206EENG	-40°C to +85°C	24 Narrow Plastic DIP
MAX206EEWG	-40°C to +85°C	24 SO
MAX206EEAG	-40°C to +85°C	24 SSOP
MAX207ECNG	0°C to +70°C	24 Narrow Plastic DIP
MAX207ECWG	0°C to +70°C	24 SO
MAX207ECAG	0°C to +70°C	24 SSOP
MAX207EENG	-40°C to +85°C	24 Narrow Plastic DIP
MAX207EEWG	-40°C to +85°C	24 SO
MAX207EEAG	-40°C to +85°C	24 SSOP

PART	TEMP. RANGE	PIN-PACKAGE
MAX208ECNG	0°C to +70°C	24 Narrow Plastic DIP
MAX208ECWG	0°C to +70°C	24 SO
MAX208ECAG	0°C to +70°C	24 SSOP
MAX208EENG	-40°C to +85°C	24 Narrow Plastic DIP
MAX208EEWG	-40°C to +85°C	24 SO
MAX208EEAG	-40°C to +85°C	24 SSOP
MAX211ECWI	0°C to +70°C	28 SO
MAX211ECAI	0°C to +70°C	28 SSOP
MAX211EEWI	-40°C to +85°C	28 SO
MAX211EEAI	-40°C to +85°C	28 SSOP
MAX213ECWI	0°C to +70°C	28 SO
MAX213ECAI	0°C to +70°C	28 SSOP
MAX213EEWI	-40°C to +85°C	28 SO
MAX213EEAI	-40°C to +85°C	28 SSOP
MAX232ECPE	0°C to +70°C	16 Plastic DIP
MAX232ECSE	0°C to +70°C	16 Narrow SO
MAX232ECWE	0°C to +70°C	16 Wide SO
MAX232EC/D	0°C to +70°C	Dice*
MAX232EEPE	-40°C to +85°C	16 Plastic DIP
MAX232EESE	-40°C to +85°C	16 Narrow SO
MAX232EEWE	-40°C to +85°C	16 Wide SO
MAX241ECWI	0°C to +70°C	28 SO
MAX241ECAI	0°C to +70°C	28 SSOP
MAX241EEWI	-40°C to +85°C	28 SO
MAX241EEAI	-40°C to +85°C	28 SSOP

*Dice are specified at T_A = +25°C.

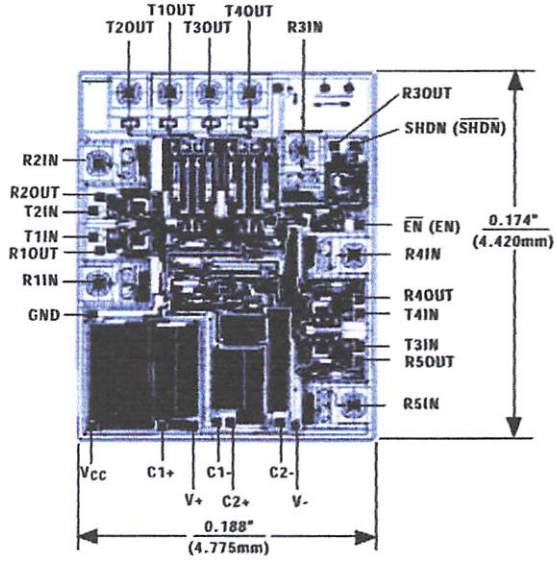
Chip Topographies

MAX202E/MAX232E



TRANSISTOR COUNT: 123
SUBSTRATE CONNECTED TO GND

MAX211E/MAX213E/MAX241E



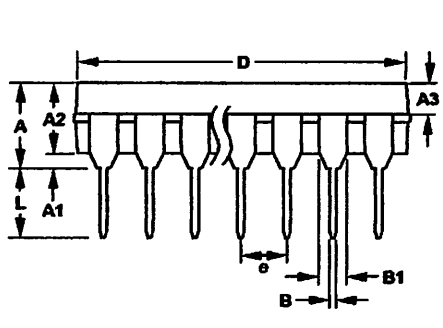
( ) ARE FOR MAX213E ONLY

TRANSISTOR COUNT: 542
SUBSTRATE CONNECTED TO GND

Chip Information

MAX205E/MAX206E/MAX207E/MAX208E
TRANSISTOR COUNT: 328
SUBSTRATE CONNECTED TO GND

Package Information

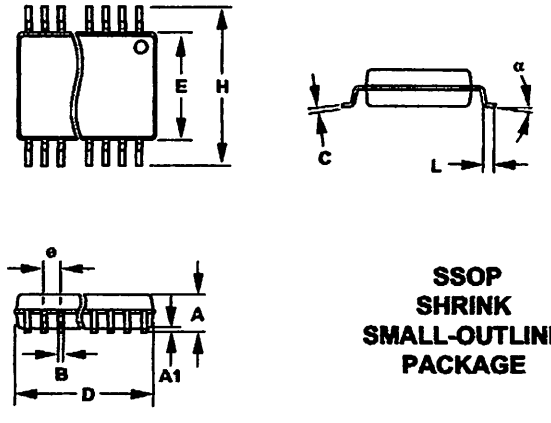


Plastic DIP
PLASTIC
DUAL-IN-LINE
PACKAGE
(0.300 in.)

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	–	0.200	–	5.08
A1	0.015	–	0.38	–
A2	0.125	0.175	3.18	4.45
A3	0.055	0.080	1.40	2.03
B	0.016	0.022	0.41	0.56
B1	0.045	0.065	1.14	1.65
C	0.008	0.012	0.20	0.30
D1	0.005	0.080	0.13	2.03
E	0.300	0.325	7.62	8.26
E1	0.240	0.310	6.10	7.87
e	0.100	–	2.54	–
eA	0.300	–	7.62	–
eB	–	0.400	–	10.16
L	0.115	0.150	2.92	3.81

PKG.	DIM	PINS	INCHES		MILLIMETERS	
			MIN	MAX	MIN	MAX
P	D	8	0.348	0.390	8.84	9.91
P	D	14	0.735	0.765	18.67	19.43
P	D	16	0.745	0.765	18.92	19.43
P	D	18	0.885	0.915	22.48	23.24
P	D	20	1.015	1.045	25.78	26.54
N	D	24	1.14	1.265	28.96	32.13

21-0043A



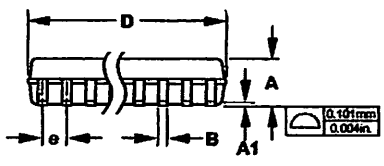
SSOP
SHRINK
SMALL-OUTLINE
PACKAGE

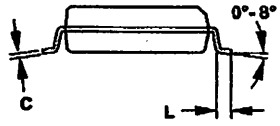
DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.068	0.078	1.73	1.99
A1	0.002	0.008	0.05	0.21
B	0.010	0.015	0.25	0.38
C	0.004	0.008	0.09	0.20
D	SEE VARIATIONS			
E	0.205	0.209	5.20	5.38
e	0.0256 BSC		0.65 BSC	
H	0.301	0.311	7.65	7.90
L	0.025	0.037	0.63	0.95
α	0°	8°	0°	8°

DIM	PINS	INCHES		MILLIMETERS	
		MIN	MAX	MIN	MAX
D	14	0.239	0.249	6.07	6.33
D	16	0.239	0.249	6.07	6.33
D	20	0.278	0.289	7.07	7.33
D	24	0.317	0.328	8.07	8.33
D	28	0.397	0.407	10.07	10.33

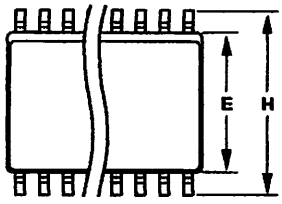
21-0056A

Package Information (continued)





DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.093	0.104	2.35	2.65
A1	0.004	0.012	0.10	0.30
B	0.014	0.019	0.35	0.49
C	0.009	0.013	0.23	0.32
E	0.291	0.299	7.40	7.60
e	0.050		1.27	
H	0.394	0.419	10.00	10.65
L	0.016	0.050	0.40	1.27



Wide SO
SMALL-OUTLINE
PACKAGE
(0.300 in.)

DIM	PINS	INCHES		MILLIMETERS	
		MIN	MAX	MIN	MAX
D	16	0.398	0.413	10.10	10.50
D	18	0.447	0.463	11.35	11.75
D	20	0.496	0.512	12.60	13.00
D	24	0.598	0.614	15.20	15.60
D	28	0.697	0.713	17.70	18.10

21-0042A

19-0122; Rev 5; 2/96

MAXIM

Low-Power, Slew-Rate-Limited RS-485/RS-422 Transceivers

General Description

The MAX481, MAX483, MAX485, MAX487–MAX491, and MAX1487 are low-power transceivers for RS-485 and RS-422 communication. Each part contains one driver and one receiver. The MAX483, MAX487, MAX488, and MAX489 feature reduced slew-rate drivers that minimize EMI and reduce reflections caused by improperly terminated cables, thus allowing error-free data transmission up to 250kbps. The driver slew rates of the MAX481, MAX485, MAX490, MAX491, and MAX1487 are not limited, allowing them to transmit up to 2.5Mbps.

These transceivers draw between 120µA and 500µA of supply current when unloaded or fully loaded with disabled drivers. Additionally, the MAX481, MAX483, and MAX487 have a low-current shutdown mode in which they consume only 0.1µA. All parts operate from a single 5V supply.

Drivers are short-circuit current limited and are protected against excessive power dissipation by thermal shutdown circuitry that places the driver outputs into a high-impedance state. The receiver input has a fail-safe feature that guarantees a logic-high output if the input is open circuit.

The MAX487 and MAX1487 feature quarter-unit-load receiver input impedance, allowing up to 128 MAX487/MAX1487 transceivers on the bus. Full-duplex communications are obtained using the MAX488–MAX491, while the MAX481, MAX483, MAX485, MAX487, and MAX1487 are designed for half-duplex applications.

Applications

Low-Power RS-485 Transceivers

Low-Power RS-422 Transceivers

Level Translators

Transceivers for EMI-Sensitive Applications

Industrial-Control Local Area Networks

Features

- **In µMAX Package: Smallest 8-Pin SO**
- **Slew-Rate Limited for Error-Free Data Transmission (MAX483/487/488/489)**
- **0.1µA Low-Current Shutdown Mode (MAX481/483/487)**
- **Low Quiescent Current:**
  120µA (MAX483/487/488/489)
  230µA (MAX1487)
  300µA (MAX481/485/490/491)
- **-7V to +12V Common-Mode Input Voltage Range**
- **Three-State Outputs**
- **30ns Propagation Delays, 5ns Skew (MAX481/485/490/491/1487)**
- **Full-Duplex and Half-Duplex Versions Available**
- **Operate from a Single 5V Supply**
- **Allows up to 128 Transceivers on the Bus (MAX487/MAX1487)**
- **Current-Limiting and Thermal Shutdown for Driver Overload Protection**

Ordering Information

PART	TEMP. RANGE	PIN-PACKAGE
MAX481CPA	0°C to +70°C	8 Plastic DIP
MAX481CSA	0°C to +70°C	8 SO
MAX481CUA	0°C to +70°C	8 µMAX
MAX481C/D	0°C to +70°C	Dice*

Ordering Information continued at end of data sheet.

* *Contact factory for dice specifications.*

Selection Table

PART NUMBER	HALF/FULL DUPLEX	DATA RATE (Mbps)	SLEW-RATE LIMITED	LOW-POWER SHUTDOWN	RECEIVER/ DRIVER ENABLE	QUIESCENT CURRENT (µA)	NUMBER OF TRANSMITTERS ON BUS	PIN COUNT
MAX481	Half	2.5	No	Yes	Yes	300	32	8
MAX483	Half	0.25	Yes	Yes	Yes	120	32	8
MAX485	Half	2.5	No	No	Yes	300	32	8
MAX487	Half	0.25	Yes	Yes	Yes	120	128	8
MAX488	Full	0.25	Yes	No	No	120	32	8
MAX489	Full	0.25	Yes	No	Yes	120	32	14
MAX490	Full	2.5	No	No	No	300	32	8
MAX491	Full	2.5	No	No	Yes	300	32	14
MAX1487	Half	2.5	No	No	Yes	230	128	8

Low-Power, Slew-Rate-Limited RS-485/RS-422 Transceivers

ABSOLUTE MAXIMUM RATINGS

Supply Voltage (V_{CC}) 12V
Control Input Voltage ($\overline{RE}$, DE) ..... -0.5V to (V_{CC} + 0.5V)
Driver Input Voltage (DI) ..... -0.5V to (V_{CC} + 0.5V)
Driver Output Voltage (A, B) ..... -8V to +12.5V
Receiver Input Voltage (A, B) ..... -8V to +12.5V
Receiver Output Voltage (RO) ..... -0.5V to (V_{CC} +0.5V)
Continuous Power Dissipation (T_A = +70°C)
8-Pin Plastic DIP (derate 9.09mW/°C above +70°C) 727mW
14-Pin Plastic DIP (derate 10.00mW/°C above +70°C) ..800mW
8-Pin SO (derate 5.88mW/°C above +70°C) 471mW
14-Pin SO (derate 8.33mW/°C above +70°C) 667mW
8-Pin µMAX (derate 4.1mW/°C above +70°C) 830mW
8-Pin CERDIP (derate 8.00mW/°C above +70°C) 640mW
14-Pin CERDIP (derate 9.09mW/°C above +70°C) 727mW
Operating Temperature Ranges
MAX4_ _C_ _/MAX1487C_ A ..... 0°C to +70°C
MAX4_ _E_ _/MAX1487E_ A ..... -40°C to +85°C
MAX4_ _MJ_/MAX1487MJA ..... -55°C to +125°C
Storage Temperature Range ..... -65°C to +160°C
Lead Temperature (soldering, 10sec) ..... +300°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC ELECTRICAL CHARACTERISTICS

(V_{CC} = 5V ±5%, T_A = T_{MIN} to T_{MAX}, unless otherwise noted.) (Notes 1, 2)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Differential Driver Output (no load)	V_{OD1}					5	V
Differential Driver Output (with load)	V_{OD2}	R = 50Ω (RS-422)		2			V
		R = 27Ω (RS-485), Figure 4		1.5		5	
Change in Magnitude of Driver Differential Output Voltage for Complementary Output States	ΔV_{OD}	R = 27Ω or 50Ω, Figure 4				0.2	V
Driver Common-Mode Output Voltage	V_{OC}	R = 27Ω or 50Ω, Figure 4				3	V
Change in Magnitude of Driver Common-Mode Output Voltage for Complementary Output States	ΔV_{OD}	R = 27Ω or 50Ω, Figure 4				0.2	V
Input High Voltage	V_{IH}	DE, DI, $\overline{RE}$		2.0			V
Input Low Voltage	V_{IL}	DE, DI, $\overline{RE}$				0.8	V
Input Current	I_{IN1}	DE, DI, $\overline{RE}$				±2	µA
Input Current (A, B)	I_{IN2}	DE = 0V; V_{CC} = 0V or 5.25V, all devices except MAX487/MAX1487	V_{IN} = 12V			1.0	mA
			V_{IN} = -7V			-0.8	
		MAX487/MAX1487, DE = 0V, V_{CC} = 0V or 5.25V	V_{IN} = 12V			0.25	mA
			V_{IN} = -7V			-0.2	
Receiver Differential Threshold Voltage	V_{TH}	-7V ≤ V_{CM} ≤ 12V		-0.2		0.2	V
Receiver Input Hysteresis	ΔV_{TH}	V_{CM} = 0V			70		mV
Receiver Output High Voltage	V_{OH}	I_O = -4mA, V_{ID} = 200mV		3.5			V
Receiver Output Low Voltage	V_{OL}	I_O = 4mA, V_{ID} = -200mV				0.4	V
Three-State (high impedance) Output Current at Receiver	I_{OZR}	0.4V ≤ V_O ≤ 2.4V				±1	µA
Receiver Input Resistance	R_{IN}	-7V ≤ V_{CM} ≤ 12V, all devices except MAX487/MAX1487		12			kΩ
		-7V ≤ V_{CM} ≤ 12V, MAX487/MAX1487		48			kΩ

DC ELECTRICAL CHARACTERISTICS (continued)

(V_{CC} = 5V ±5%, T_A = T_{MIN} to T_{MAX}, unless otherwise noted.) (Notes 1, 2)

PARAMETER	SYMBOL	CONDITIONS			MIN	TYP	MAX	UNITS
No-Load Supply Current (Note 3)	I_{CC}	MAX488/MAX489, DE, DI, $\overline{RE}$ = 0V or V_{CC}				120	250	µA
		MAX490/MAX491, DE, DI, $\overline{RE}$ = 0V or V_{CC}				300	500	
		MAX481/MAX485, $\overline{RE}$ = 0V or V_{CC}	DE = V_{CC}			500	900	
			DE = 0V			300	500	
		MAX1487, $\overline{RE}$ = 0V or V_{CC}	DE = V_{CC}			300	500	
			DE = 0V			230	400	
		MAX483/MAX487, $\overline{RE}$ = 0V or V_{CC}	DE = 5V	MAX483		350	650	
				MAX487		250	400	
			DE = 0V			120	250	
Supply Current in Shutdown	I_{SHDN}	MAX481/483/487, DE = 0V, $\overline{RE}$ = V_{CC}				0.1	10	µA
Driver Short-Circuit Current, V_O = High	I_{OSD1}	-7V ≤ V_O ≤12V (Note 4)			35		250	mA
Driver Short-Circuit Current, V_O = Low	I_{OSD2}	-7V ≤ V_O ≤12V (Note 4)			35		250	mA
Receiver Short-Circuit Current	I_{OSR}	0V ≤ V_O ≤ V_{CC}			7		95	mA

SWITCHING CHARACTERISTICS—MAX481/MAX485, MAX490/MAX491, MAX1487

(V_{CC} = 5V ±5%, T_A = T_{MIN} to T_{MAX}, unless otherwise noted.) (Notes 1, 2)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Driver Input to Output	t_{PLH}	Figures 6 and 8, R_{DIFF} = 54Ω, C_{L1} = C_{L2} = 100pF		10	30	60	ns
	t_{PHL}			10	30	60	
Driver Output Skew to Output	t_{SKEW}	Figures 6 and 8, R_{DIFF} = 54Ω, C_{L1} = C_{L2} = 100pF			5	10	ns
Driver Rise or Fall Time	t_R, t_F	Figures 6 and 8, R_{DIFF} = 54Ω, C_{L1} = C_{L2} = 100pF	MAX481, MAX485, MAX1487	3	15	40	ns
			MAX490C/E, MAX491C/E	5	15	25	
			MAX490M, MAX491M	3	15	40	
Driver Enable to Output High	t_{ZH}	Figures 7 and 9, C_L = 100pF, S2 closed			40	70	ns
Driver Enable to Output Low	t_{ZL}	Figures 7 and 9, C_L = 100pF, S1 closed			40	70	ns
Driver Disable Time from Low	t_{LZ}	Figures 7 and 9, C_L = 15pF, S1 closed			40	70	ns
Driver Disable Time from High	t_{HZ}	Figures 7 and 9, C_L = 15pF, S2 closed			40	70	ns
Receiver Input to Output	t_{PLH}, t_{PHL}	Figures 6 and 10, R_{DIFF} = 54Ω, C_{L1} = C_{L2} = 100pF	MAX481, MAX485, MAX1487	20	90	200	ns
			MAX490C/E, MAX491C/E	20	90	150	
			MAX490M, MAX491M	20	90	200	
$\lvert t_{PLH} - t_{PHL} \rvert$ Differential Receiver Skew	t_{SKD}	Figures 6 and 10, R_{DIFF} = 54Ω, C_{L1} = C_{L2} = 100pF			13		ns
Receiver Enable to Output Low	t_{ZL}	Figures 5 and 11, C_{RL} = 15pF, S1 closed			20	50	ns
Receiver Enable to Output High	t_{ZH}	Figures 5 and 11, C_{RL} = 15pF, S2 closed			20	50	ns
Receiver Disable Time from Low	t_{LZ}	Figures 5 and 11, C_{RL} = 15pF, S1 closed			20	50	ns
Receiver Disable Time from High	t_{HZ}	Figures 5 and 11, C_{RL} = 15pF, S2 closed			20	50	ns
Maximum Data Rate	f_{MAX}			2.5			Mbps
Time to Shutdown	t_{SHDN}	MAX481 (Note 5)		50	200	600	ns

Low-Power, Slew-Rate-Limited RS-485/RS-422 Transceivers

SWITCHING CHARACTERISTICS—MAX481/MAX485, MAX490/MAX491, MAX1487 (continued)

(V_{CC} = 5V ±5%, T_A = T_{MIN} to T_{MAX}, unless otherwise noted.) (Notes 1, 2)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Driver Enable from Shutdown to Output High (MAX481)	$t_{ZH(SHDN)}$	Figures 7 and 9, C_L = 100pF, S2 closed		40	100	ns
Driver Enable from Shutdown to Output Low (MAX481)	$t_{ZL(SHDN)}$	Figures 7 and 9, C_L = 100pF, S1 closed		40	100	ns
Receiver Enable from Shutdown to Output High (MAX481)	$t_{ZH(SHDN)}$	Figures 5 and 11, C_L = 15pF, S2 closed, A - B = 2V		300	1000	ns
Receiver Enable from Shutdown to Output Low (MAX481)	$t_{ZL(SHDN)}$	Figures 5 and 11, C_L = 15pF, S1 closed, B - A = 2V		300	1000	ns

SWITCHING CHARACTERISTICS—MAX483, MAX487/MAX488/MAX489

(V_{CC} = 5V ±5%, T_A = T_{MIN} to T_{MAX}, unless otherwise noted.) (Notes 1, 2)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Driver Input to Output	t_{PLH}	Figures 6 and 8, R_{DIFF} = 54Ω, C_{L1} = C_{L2} = 100pF	250	800	2000	ns
	t_{PHL}		250	800	2000	
Driver Output Skew to Output	t_{SKEW}	Figures 6 and 8, R_{DIFF} = 54Ω, C_{L1} = C_{L2} = 100pF		100	800	ns
Driver Rise or Fall Time	t_R, t_F	Figures 6 and 8, R_{DIFF} = 54Ω, C_{L1} = C_{L2} = 100pF	250		2000	ns
Driver Enable to Output High	t_{ZH}	Figures 7 and 9, C_L = 100pF, S2 closed	250		2000	ns
Driver Enable to Output Low	t_{ZL}	Figures 7 and 9, C_L = 100pF, S1 closed	250		2000	ns
Driver Disable Time from Low	t_{LZ}	Figures 7 and 9, C_L = 15pF, S1 closed	300		3000	ns
Driver Disable Time from High	t_{HZ}	Figures 7 and 9, C_L = 15pF, S2 closed	300		3000	ns
Receiver Input to Output	t_{PLH}	Figures 6 and 10, R_{DIFF} = 54Ω, C_{L1} = C_{L2} = 100pF	250		2000	ns
	t_{PHL}		250		2000	
| t_{PLH} - t_{PHL} | Differential Receiver Skew	t_{SKD}	Figures 6 and 10, R_{DIFF} = 54Ω, C_{L1} = C_{L2} = 100pF		100		ns
Receiver Enable to Output Low	t_{ZL}	Figures 5 and 11, C_{RL} = 15pF, S1 closed		20	50	ns
Receiver Enable to Output High	t_{ZH}	Figures 5 and 11, C_{RL} = 15pF, S2 closed		20	50	ns
Receiver Disable Time from Low	t_{LZ}	Figures 5 and 11, C_{RL} = 15pF, S1 closed		20	50	ns
Receiver Disable Time from High	t_{HZ}	Figures 5 and 11, C_{RL} = 15pF, S2 closed		20	50	ns
Maximum Data Rate	f_{MAX}	t_{PLH}, t_{PHL} < 50% of data period	250			kbps
Time to Shutdown	t_{SHDN}	MAX483/MAX487 (Note 5)	50	200	600	ns
Driver Enable from Shutdown to Output High	$t_{ZH(SHDN)}$	MAX483/MAX487, Figures 7 and 9, C_L = 100pF, S2 closed			2000	ns
Driver Enable from Shutdown to Output Low	$t_{ZL(SHDN)}$	MAX483/MAX487, Figures 7 and 9, C_L = 100pF, S1 closed			2000	ns
Receiver Enable from Shutdown to Output High	$t_{ZH(SHDN)}$	MAX483/MAX487, Figures 5 and 11, C_L = 15pF, S2 closed			2500	ns
Receiver Enable from Shutdown to Output Low	$t_{ZL(SHDN)}$	MAX483/MAX487, Figures 5 and 11, C_L = 15pF, S1 closed			2500	ns

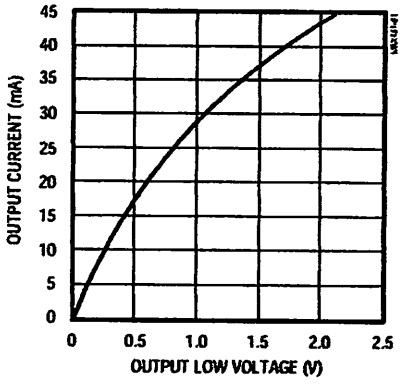
NOTES FOR ELECTRICAL/SWITCHING CHARACTERISTICS

Note 1: All currents into device pins are positive; all currents out of device pins are negative. All voltages are referenced to device ground unless otherwise specified.
Note 2: All typical specifications are given for V_{CC} = 5V and T_A = +25°C.
Note 3: Supply current specification is valid for loaded transmitters when DE = 0V.
Note 4: Applies to peak current. See *Typical Operating Characteristics*.
Note 5: The MAX481/MAX483/MAX487 are put into shutdown by bringing $\overline{RE}$ high and DE low. If the inputs are in this state for less than 50ns, the parts are guaranteed not to enter shutdown. If the inputs are in this state for at least 600ns, the parts are guaranteed to have entered shutdown. See *Low-Power Shutdown Mode* section.

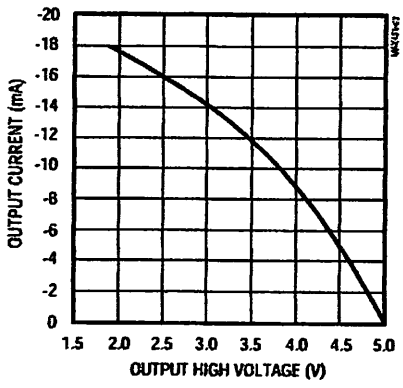
Typical Operating Characteristics

(V_{CC} = 5V, T_A = +25°C, unless otherwise noted.)

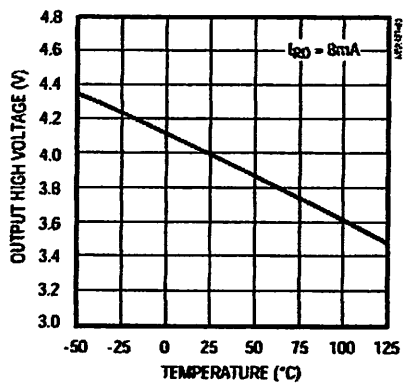
OUTPUT CURRENT vs. RECEIVER OUTPUT LOW VOLTAGE



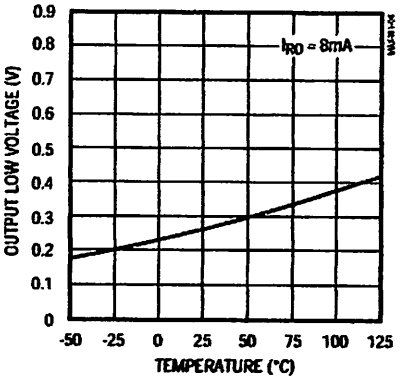
OUTPUT CURRENT vs. RECEIVER OUTPUT HIGH VOLTAGE



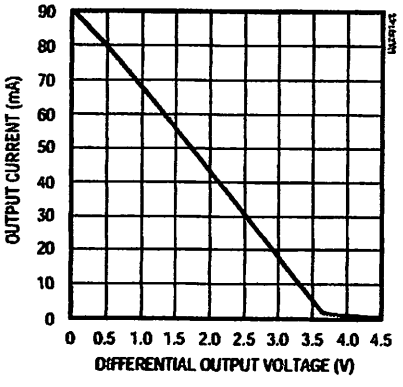
RECEIVER OUTPUT HIGH VOLTAGE vs. TEMPERATURE



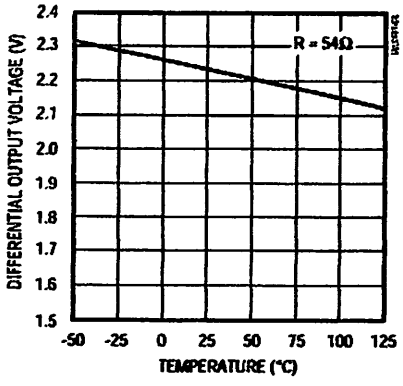
RECEIVER OUTPUT LOW VOLTAGE vs. TEMPERATURE



DRIVER OUTPUT CURRENT vs. DIFFERENTIAL OUTPUT VOLTAGE



DRIVER DIFFERENTIAL OUTPUT VOLTAGE vs. TEMPERATURE

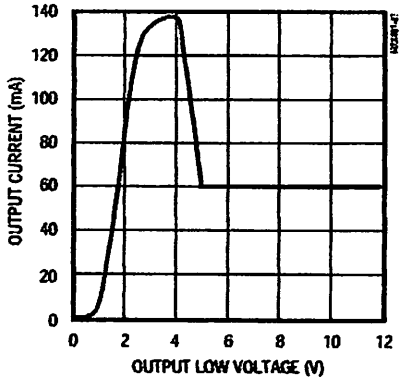


Low-Power, Slew-Rate-Limited RS-485/RS-422 Transceivers

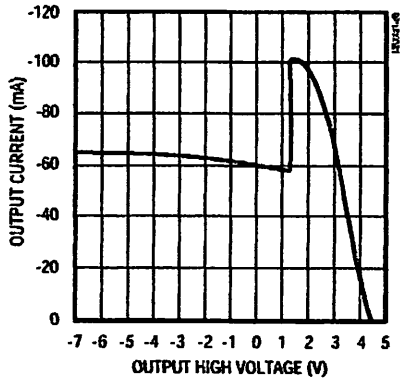
Typical Operating Characteristics (continued)

(V_{CC} = 5V, T_A = +25°C, unless otherwise noted.)

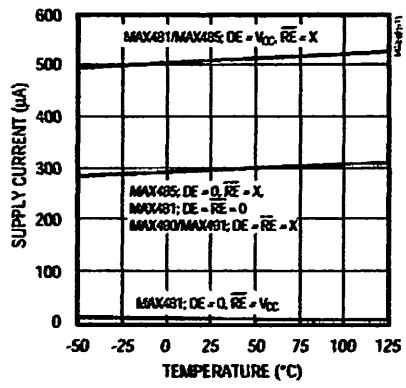
OUTPUT CURRENT vs. DRIVER OUTPUT LOW VOLTAGE



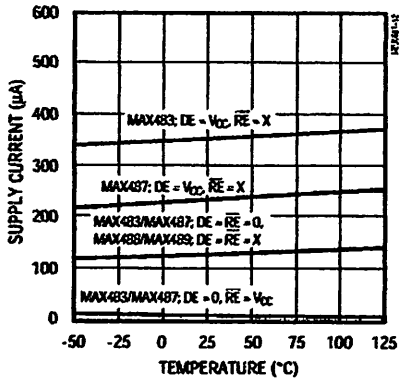
OUTPUT CURRENT vs. DRIVER OUTPUT HIGH VOLTAGE



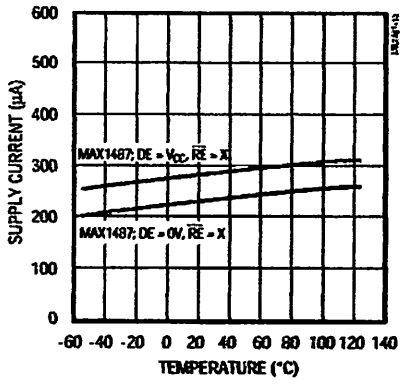
MAX481/MAX485/MAX490/MAX491 SUPPLY CURRENT vs. TEMPERATURE



MAX483/MAX487–MAX489 SUPPLY CURRENT vs. TEMPERATURE



MAX1487 SUPPLY CURRENT vs. TEMPERATURE



Pin Description

PIN					NAME	FUNCTION
MAX481/MAX483/ MAX485/MAX487/ MAX1487		MAX488/ MAX490		MAX489/ MAX491		
DIP/SO	µMAX	DIP/SO	µMAX	DIP/SO		
1	3	2	4	2	RO	Receiver Output: If A > B by 200mV, RO will be high; If A < B by 200mV, RO will be low.
2	4	—	—	3	$\overline{RE}$	Receiver Output Enable. RO is enabled when $\overline{RE}$ is low; RO is high impedance when $\overline{RE}$ is high.
3	5	—	—	4	DE	Driver Output Enable. The driver outputs, Y and Z, are enabled by bringing DE high. They are high impedance when DE is low. If the driver outputs are enabled, the parts function as line drivers. While they are high impedance, they function as line receivers if $\overline{RE}$ is low.
4	6	3	5	5	DI	Driver Input. A low on DI forces output Y low and output Z high. Similarly, a high on DI forces output Y high and output Z low.
5	7	4	6	6, 7	GND	Ground
—	—	5	7	9	Y	Noninverting Driver Output
—	—	6	8	10	Z	Inverting Driver Output
6	8	—	—	—	A	Noninverting Receiver Input and Noninverting Driver Output
—	—	8	2	12	A	Noninverting Receiver Input
7	1	—	—	—	B	Inverting Receiver Input and Inverting Driver Output
—	—	7	1	11	B	Inverting Receiver Input
8	2	1	3	14	VCC	Positive Supply: 4.75V ≤ VCC ≤ 5.25V
—	—	—	—	1, 8, 13	N.C.	No Connect—not internally connected

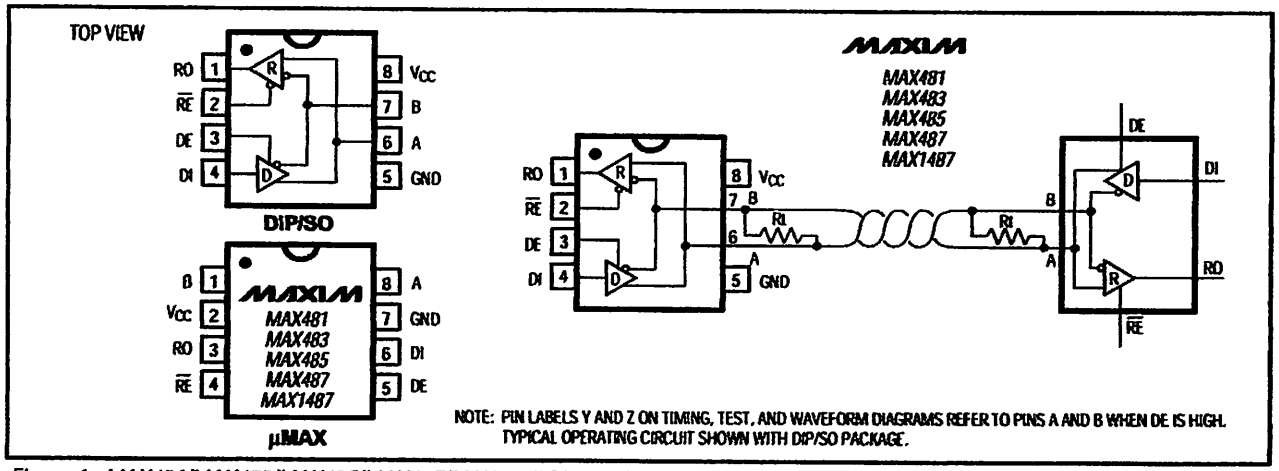


Figure 1. MAX481/MAX483/MAX485/MAX487/MAX1487 Pin Configuration and Typical Operating Circuit

Low-Power, Slew-Rate-Limited RS-485/RS-422 Transceivers

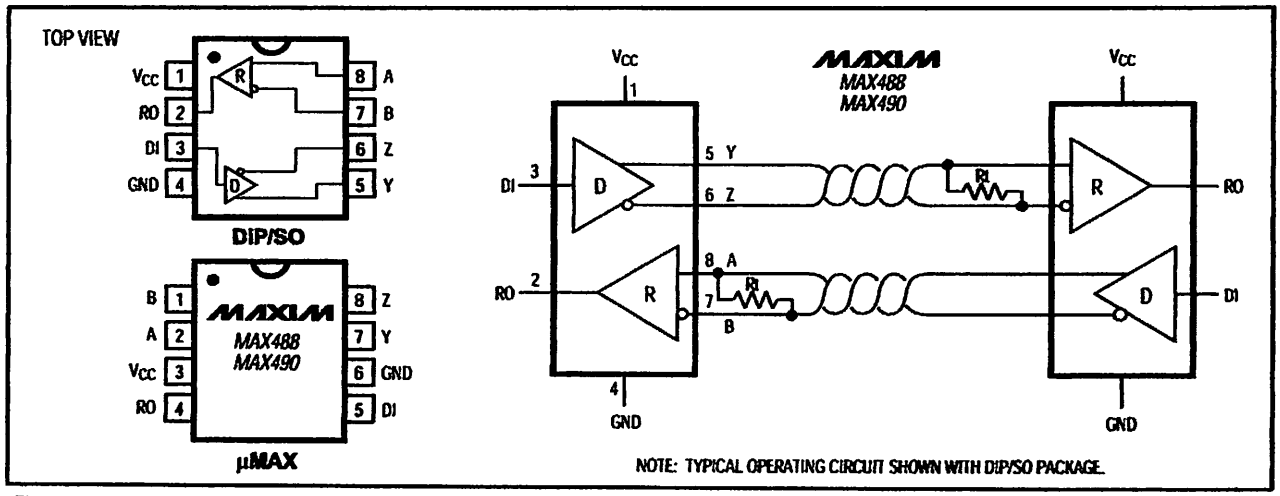


Figure 2. MAX488/MAX490 Pin Configuration and Typical Operating Circuit

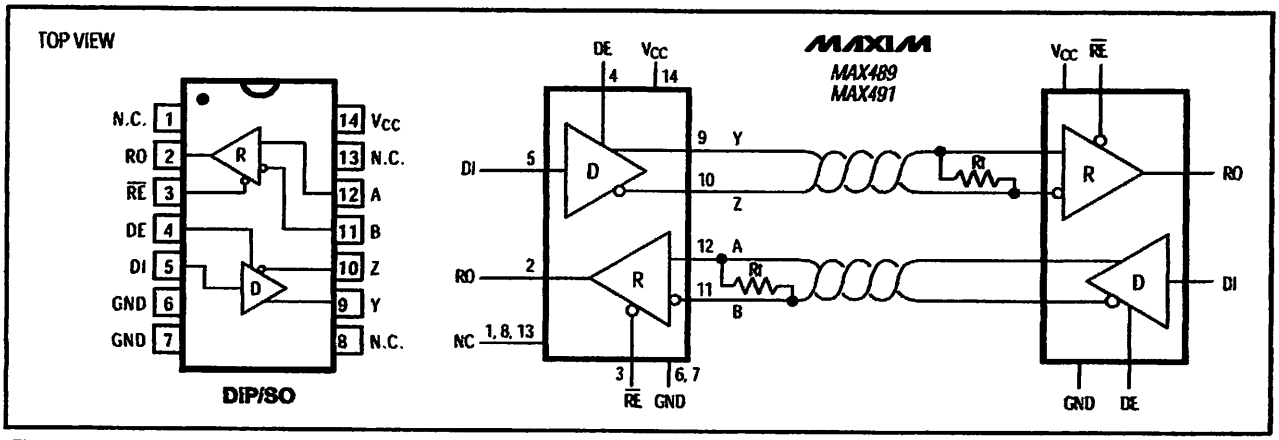


Figure 3. MAX489/MAX491 Pin Configuration and Typical Operating Circuit

Applications Information

The MAX481/MAX483/MAX485/MAX487–MAX491 and MAX1487 are low-power transceivers for RS-485 and RS-422 communications. The MAX481, MAX485, MAX490, MAX491, and MAX1487 can transmit and receive at data rates up to 2.5Mbps, while the MAX483, MAX487, MAX488, and MAX489 are specified for data rates up to 250kbps. The MAX488–MAX491 are full-duplex transceivers while the MAX481, MAX483, MAX485, MAX487, and MAX1487 are half-duplex. In addition, Driver Enable (DE) and Receiver Enable ($\overline{RE}$) pins are included on the MAX481, MAX483, MAX485, MAX487, MAX489, MAX491, and MAX1487. When disabled, the driver and receiver outputs are high impedance.

MAX487/MAX1487: 128 Transceivers on the Bus

The 48kΩ, 1/4-unit-load receiver input impedance of the MAX487 and MAX1487 allows up to 128 transceivers on a bus, compared to the 1-unit load (12kΩ input impedance) of standard RS-485 drivers (32 transceivers maximum). Any combination of MAX487/MAX1487 and other RS-485 transceivers with a total of 32 unit loads or less can be put on the bus. The MAX481/MAX483/MAX485 and MAX488–MAX491 have standard 12kΩ Receiver Input impedance.

Test Circuits

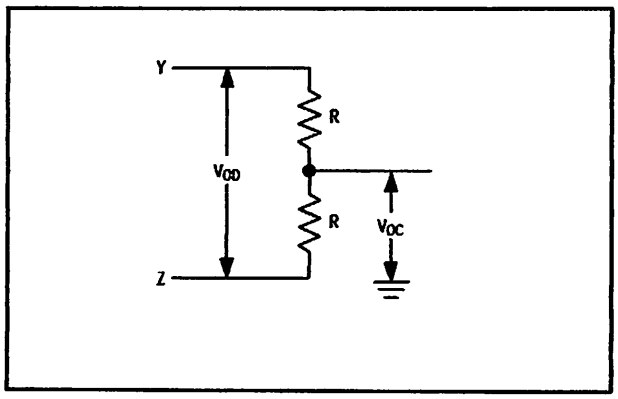


Figure 4. Driver DC Test Load

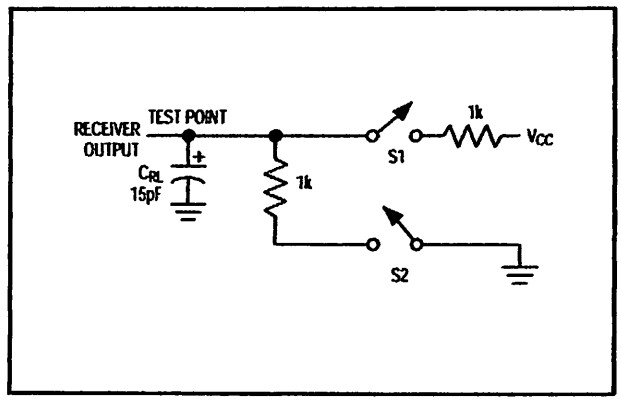


Figure 5. Receiver Timing Test Load

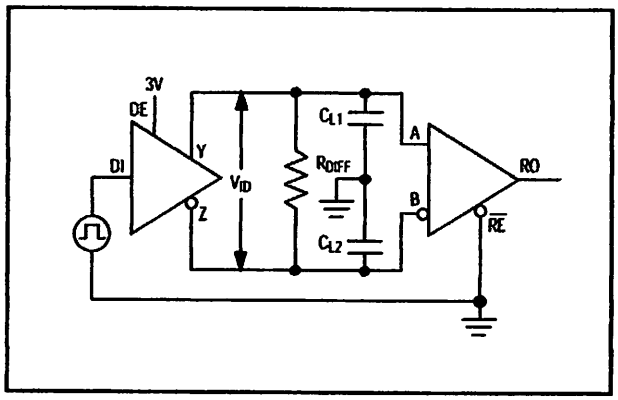


Figure 6. Driver/Receiver Timing Test Circuit

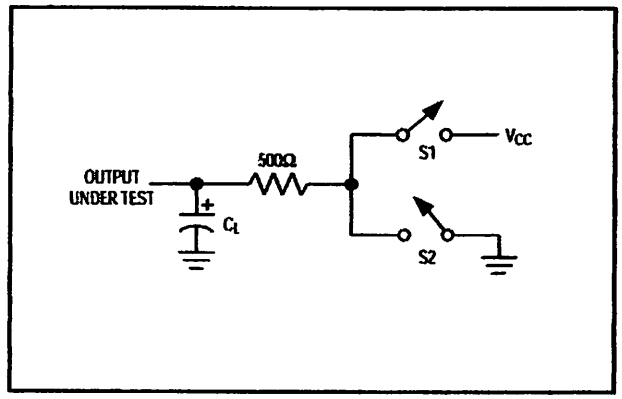


Figure 7. Driver Timing Test Load

MAX483/MAX487/MAX488/MAX489: Reduced EMI and Reflections

The MAX483 and MAX487–MAX489 are slew-rate limited, minimizing EMI and reducing reflections caused by improperly terminated cables. Figure 12 shows the driver output waveform and its Fourier analysis of a 150kHz signal transmitted by a MAX481, MAX485, MAX490, MAX491, or MAX1487. High-frequency harmonics with large amplitudes are evident. Figure 13 shows the same information displayed for a MAX483, MAX487, MAX488, or MAX489 transmitting under the same conditions. Figure 13's high-frequency harmonics have much lower amplitudes, and the potential for EMI is significantly reduced.

Low-Power, Slew-Rate-Limited RS-485/RS-422 Transceivers

Switching Waveforms

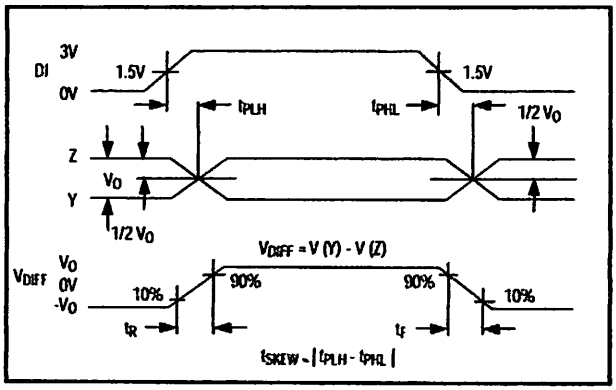


Figure 8. Driver Propagation Delays

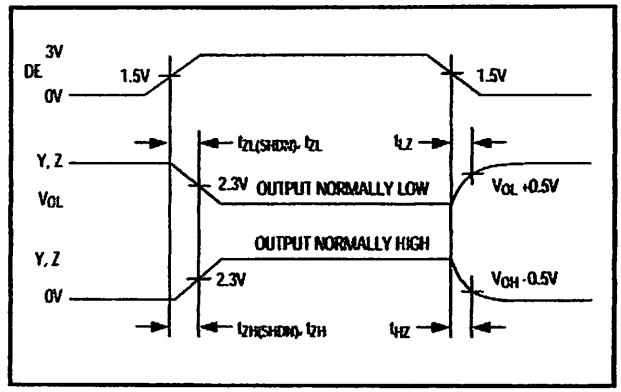


Figure 9. Driver Enable and Disable Times (except MAX488 and MAX490)

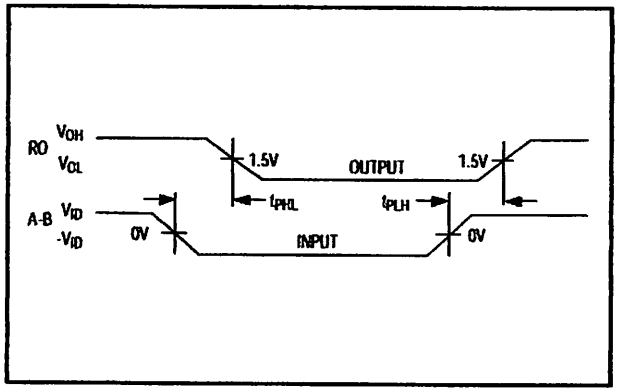


Figure 10. Receiver Propagation Delays

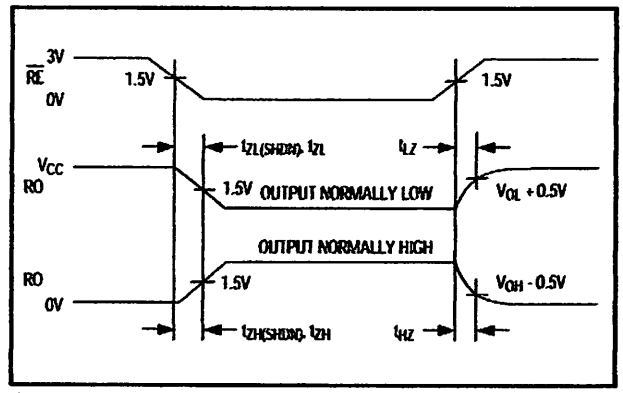


Figure 11. Receiver Enable and Disable Times (except MAX488 and MAX490)

Function Tables (MAX481/MAX483/MAX485/MAX487/MAX1487)

Table 1. Transmitting

INPUTS			OUTPUTS	
$\overline{RE}$	DE	DI	Z	Y
X	1	1	0	1
X	1	0	1	0
0	0	X	High-Z	High-Z
1	0	X	High-Z*	High-Z*

X = Don't care
High-Z = High impedance
* Shutdown mode for MAX481/MAX483/MAX487

Table 2. Receiving

INPUTS			OUTPUT
$\overline{RE}$	DE	A-B	RO
0	0	≥ +0.2V	1
0	0	≤ -0.2V	0
0	0	Inputs open	1
1	0	X	High-Z*

X = Don't care
High-Z = High impedance
* Shutdown mode for MAX481/MAX483/MAX487

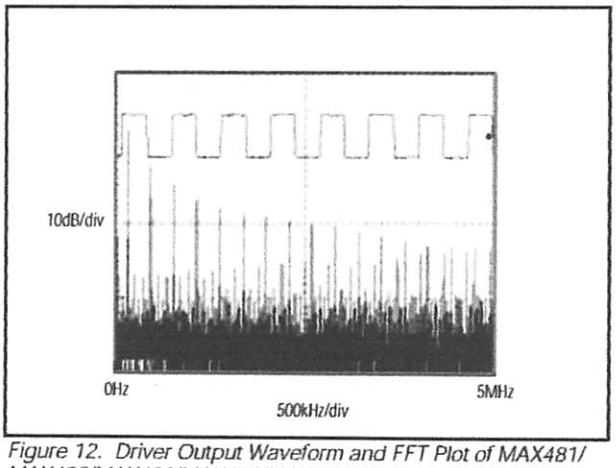


Figure 12. Driver Output Waveform and FFT Plot of MAX481/MAX485/MAX490/MAX491/MAX1487 Transmitting a 150kHz Signal

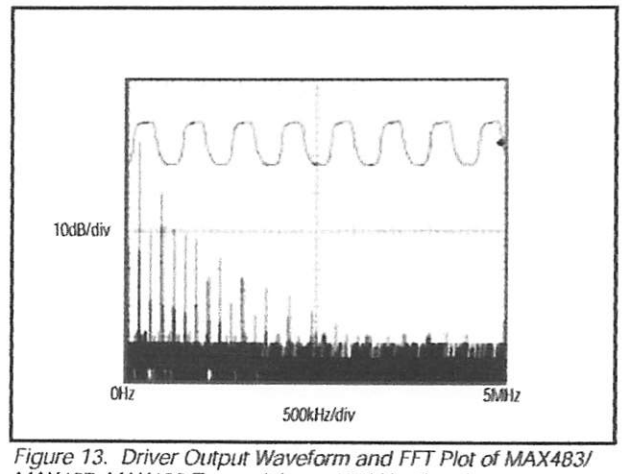


Figure 13. Driver Output Waveform and FFT Plot of MAX483/MAX487–MAX489 Transmitting a 150kHz Signal

Low-Power Shutdown Mode (MAX481/MAX483/MAX487)

A low-power shutdown mode is initiated by bringing both $\overline{RE}$ high and DE low. The devices will not shut down unless both the driver and receiver are disabled. In shutdown, the devices typically draw only 0.1µA of supply current.

$\overline{RE}$ and DE may be driven simultaneously; the parts are guaranteed not to enter shutdown if $\overline{RE}$ is high and DE is low for less than 50ns. If the inputs are in this state for at least 600ns, the parts are guaranteed to enter shutdown.

For the MAX481, MAX483, and MAX487, the t_{ZH} and t_{ZL} enable times assume the part was not in the low-power shutdown state (the MAX485/MAX488–MAX491 and MAX1487 can not be shut down). The $t_{ZH(SHDN)}$ and $t_{ZL(SHDN)}$ enable times assume the parts were shut down (see *Electrical Characteristics*).

It takes the drivers and receivers longer to become enabled from the low-power shutdown state ($t_{ZH(SHDN)}$, $t_{ZL(SHDN)}$) than from the operating mode (t_{ZH}, t_{ZL}). (The parts are in operating mode if the $\overline{RE}$, DE inputs equal a logical 0,1 or 1,1 or 0, 0.)

Driver Output Protection

Excessive output current and power dissipation caused by faults or by bus contention are prevented by two mechanisms. A foldback current limit on the output stage provides immediate protection against short circuits over the whole common-mode voltage range (see *Typical Operating Characteristics*). In addition, a thermal shutdown circuit forces the driver outputs into a high-impedance state if the die temperature rises excessively.

Propagation Delay

Many digital encoding schemes depend on the difference between the driver and receiver propagation delay times. Typical propagation delays are shown in Figures 15–18 using Figure 14's test circuit.

The difference in receiver delay times, $|t_{PLH} - t_{PHL}|$, is typically under 13ns for the MAX481, MAX485, MAX490, MAX491, and MAX1487 and is typically less than 100ns for the MAX483 and MAX487–MAX489.

The driver skew times are typically 5ns (10ns max) for the MAX481, MAX485, MAX490, MAX491, and MAX1487, and are typically 100ns (800ns max) for the MAX483 and MAX487–MAX489.

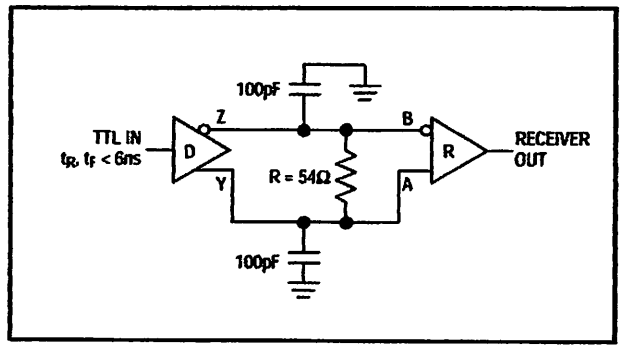


Figure 14. Receiver Propagation Delay Test Circuit

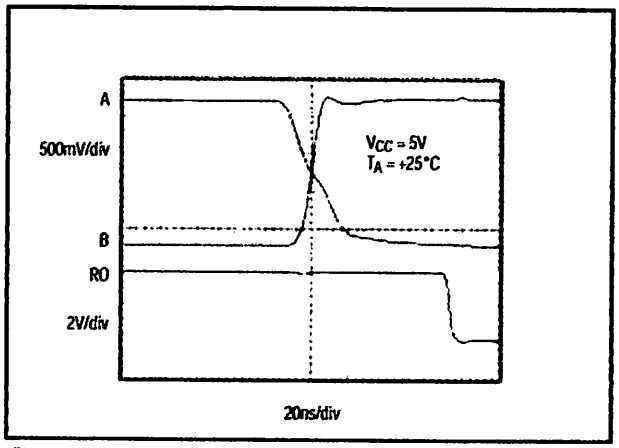


Figure 15. MAX481/MAX485/MAX490/MAX491/MAX1487 Receiver t_{PHL}

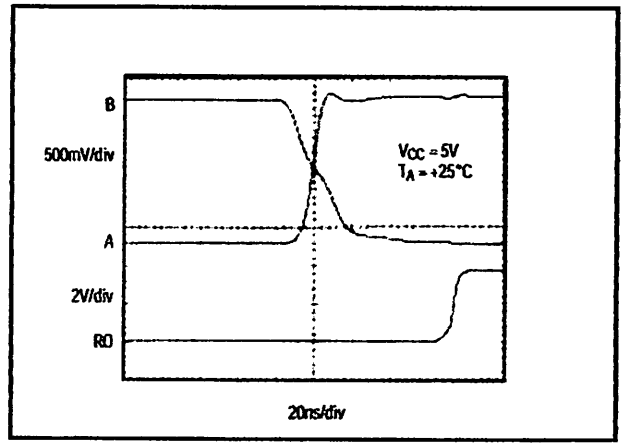


Figure 16. MAX481/MAX485/MAX490/MAX491/MAX1487 Receiver t_{PLH}

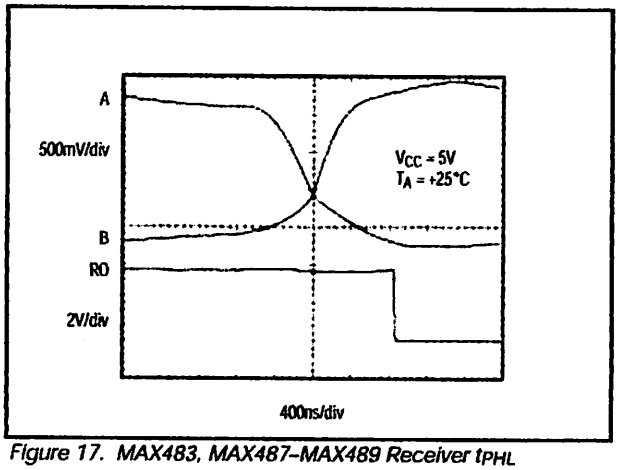


Figure 17. MAX483, MAX487–MAX489 Receiver t_{PHL}

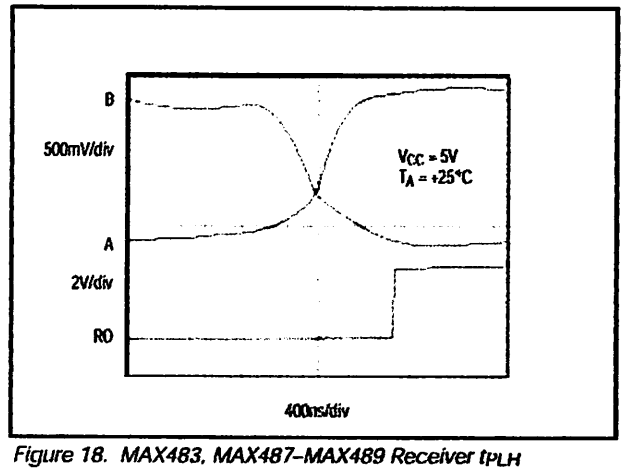


Figure 18. MAX483, MAX487–MAX489 Receiver t_{PLH}

Line Length vs. Data Rate

The RS-485/RS-422 standard covers line lengths up to 4000 feet. For line lengths greater than 4000 feet, see Figure 23.

Figures 19 and 20 show the system differential voltage for the parts driving 4000 feet of 26AWG twisted-pair wire at 110kHz into 120Ω loads.

Typical Applications

The MAX481, MAX483, MAX485, MAX487–MAX491, and MAX1487 transceivers are designed for bidirectional data communications on multipoint bus transmission lines.

Figures 21 and 22 show typical network applications circuits. These parts can also be used as line repeaters, with cable lengths longer than 4000 feet, as shown in Figure 23.

To minimize reflections, the line should be terminated at both ends in its characteristic impedance, and stub lengths off the main line should be kept as short as possible. The slew-rate-limited MAX483 and MAX487–MAX489 are more tolerant of imperfect termination.

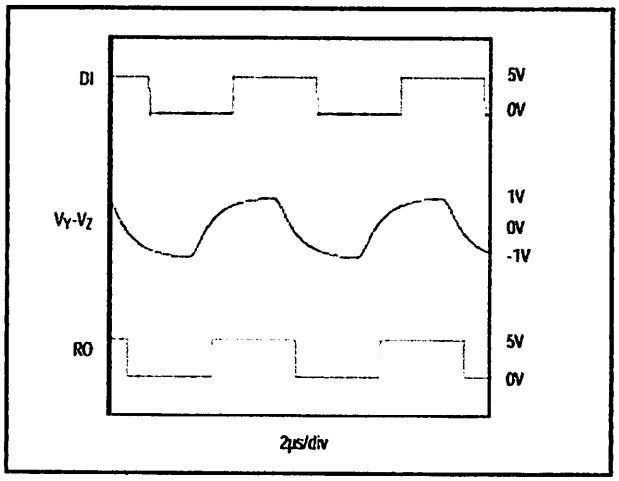


Figure 19. MAX481/MAX485/MAX490/MAX491/MAX1487 System Differential Voltage at 110kHz Driving 4000ft of Cable

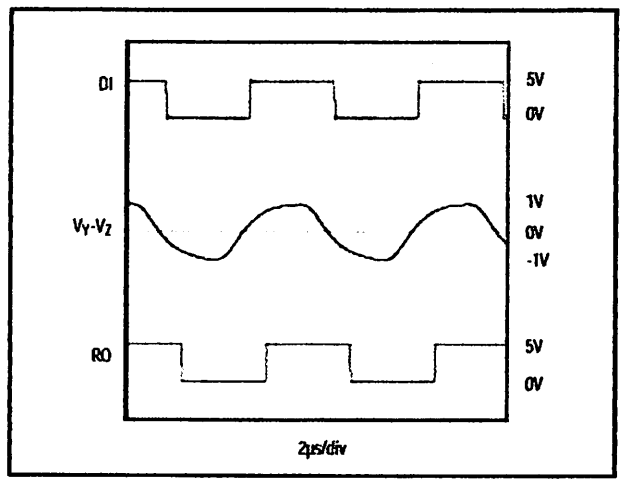


Figure 20. MAX483, MAX487–MAX489 System Differential Voltage at 110kHz Driving 4000ft of Cable

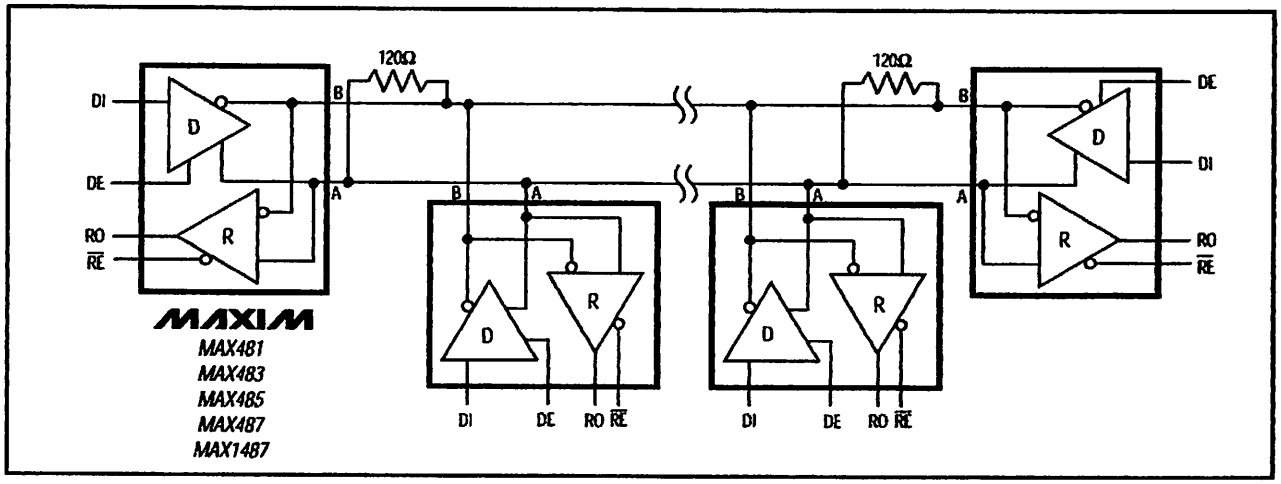


Figure 21. MAX481/MAX483/MAX485/MAX487/MAX1487 Typical Half-Duplex RS-485 Network

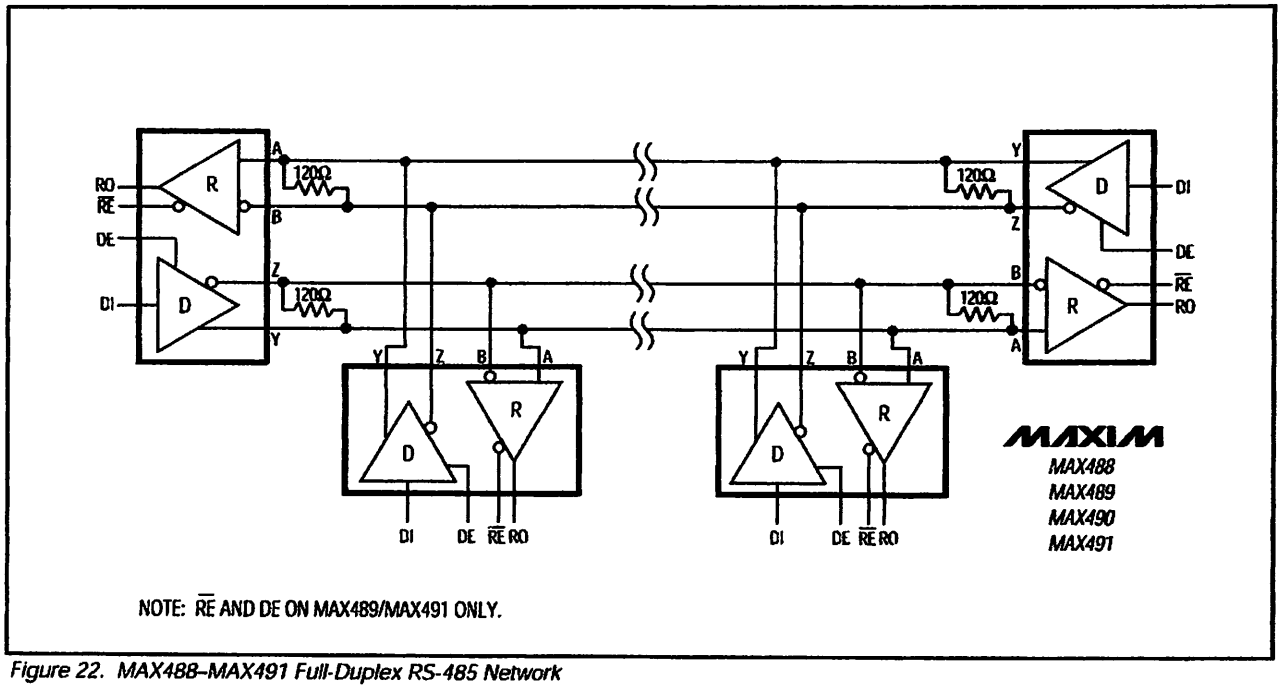


Figure 22. MAX488–MAX491 Full-Duplex RS-485 Network

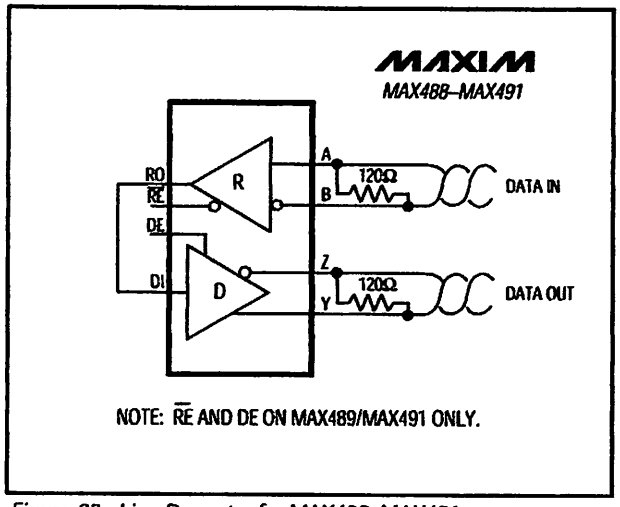


Figure 23. Line Repeater for MAX488–MAX491

Isolated RS-485

For isolated RS-485 applications, see the MAX253 and MAX1480 data sheets.

Ordering Information (continued)

PART	TEMP. RANGE	PIN-PACKAGE
MAX481EPA	-40°C to +85°C	8 Plastic DIP
MAX481ESA	-40°C to +85°C	8 SO
MAX481MJA	-55°C to +125°C	8 CERDIP
MAX483CPA	0°C to +70°C	8 Plastic DIP
MAX483CSA	0°C to +70°C	8 SO
MAX483CUA	0°C to +70°C	8 µMAX
MAX483C/D	0°C to +70°C	Dice*
MAX483EPA	-40°C to +85°C	8 Plastic DIP
MAX483ESA	-40°C to +85°C	8 SO
MAX483MJA	-55°C to +125°C	8 CERDIP
MAX485CPA	0°C to +70°C	8 Plastic DIP
MAX485CSA	0°C to +70°C	8 SO
MAX485CUA	0°C to +70°C	8 µMAX
MAX485C/D	0°C to +70°C	Dice*
MAX485EPA	-40°C to +85°C	8 Plastic DIP
MAX485ESA	-40°C to +85°C	8 SO
MAX485MJA	-55°C to +125°C	8 CERDIP
MAX487CPA	0°C to +70°C	8 Plastic DIP
MAX487CSA	0°C to +70°C	8 SO
MAX487CUA	0°C to +70°C	8 µMAX
MAX487C/D	0°C to +70°C	Dice*
MAX487EPA	-40°C to +85°C	8 Plastic DIP
MAX487ESA	-40°C to +85°C	8 SO
MAX487MJA	-55°C to +125°C	8 CERDIP
MAX488CPA	0°C to +70°C	8 Plastic DIP
MAX488CSA	0°C to +70°C	8 SO
MAX488CUA	0°C to +70°C	8 µMAX
MAX488C/D	0°C to +70°C	Dice*
MAX488EPA	-40°C to +85°C	8 Plastic DIP
MAX488ESA	-40°C to +85°C	8 SO
MAX488MJA	-55°C to +125°C	8 CERDIP
MAX489CPD	0°C to +70°C	14 Plastic DIP
MAX489CSD	0°C to +70°C	14 SO
MAX489C/D	0°C to +70°C	Dice*
MAX489EPD	-40°C to +85°C	14 Plastic DIP
MAX489ESD	-40°C to +85°C	14 SO
MAX489MJD	-55°C to +125°C	14 CERDIP

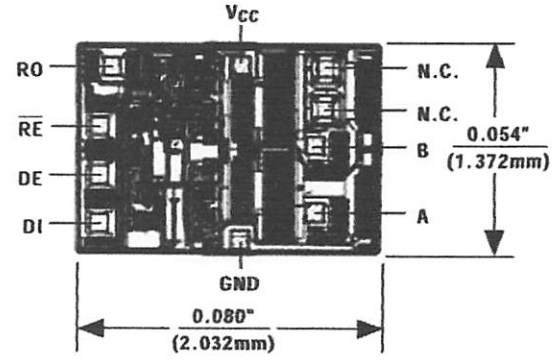
Ordering Information (continued)

PART	TEMP. RANGE	PIN-PACKAGE
MAX490CPA	0°C to +70°C	8 Plastic DIP
MAX490CSA	0°C to +70°C	8 SO
MAX490CUA	0°C to +70°C	8 µMAX
MAX490C/D	0°C to +70°C	Dice*
MAX490EPA	-40°C to +85°C	8 Plastic DIP
MAX490ESA	-40°C to +85°C	8 SO
MAX490MJA	-55°C to +125°C	8 CERDIP
MAX491CPD	0°C to +70°C	14 Plastic DIP
MAX491CSD	0°C to +70°C	14 SO
MAX491C/D	0°C to +70°C	Dice*
MAX491EPD	-40°C to +85°C	14 Plastic DIP
MAX491ESD	-40°C to +85°C	14 SO
MAX491MJD	-55°C to +125°C	14 CERDIP
MAX1487CPA	0°C to +70°C	8 Plastic DIP
MAX1487CSA	0°C to +70°C	8 SO
MAX1487CUA	0°C to +70°C	8 µMAX
MAX1487C/D	0°C to +70°C	Dice*
MAX1487EPA	-40°C to +85°C	8 Plastic DIP
MAX1487ESA	-40°C to +85°C	8 SO
MAX1487MJA	-55°C to +125°C	8 CERDIP

* *Contact factory for dice specifications.*

Chip Topographies

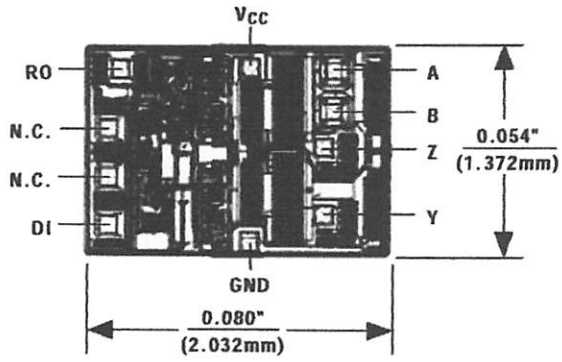
MAX481/MAX483/MAX485/MAX487/MAX1487



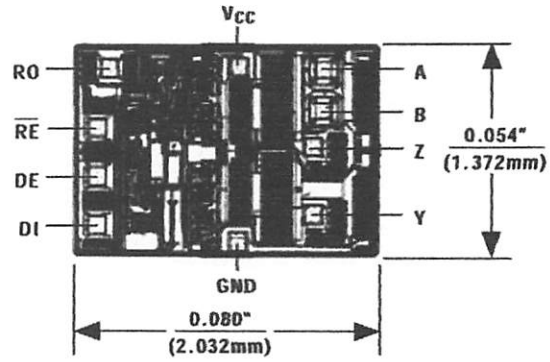
Low-Power, Slew-Rate-Limited RS-485/RS-422 Transceivers

Chip Topographies (continued)

MAX488/MAX490



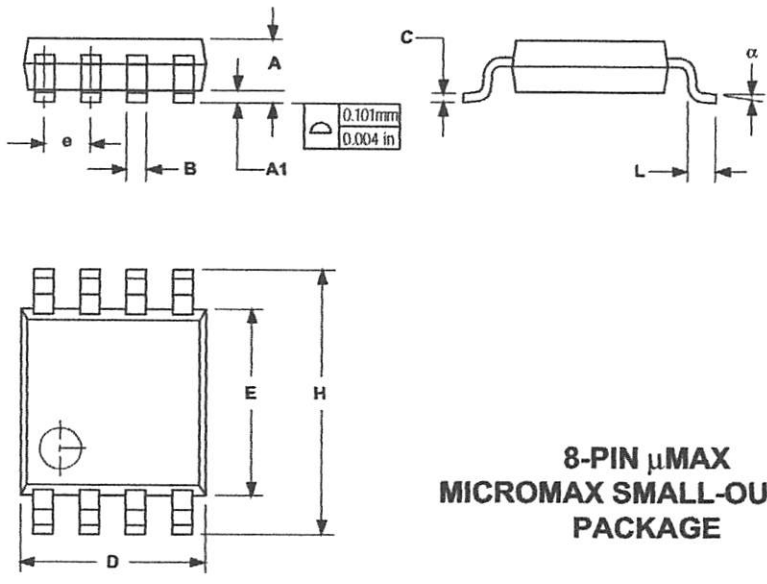
MAX489/MAX491



TRANSISTOR COUNT: 248

SUBSTRATE CONNECTED TO GND

Package Information



DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.036	0.044	0.91	1.11
A1	0.004	0.008	0.10	0.20
B	0.010	0.014	0.25	0.36
C	0.005	0.007	0.13	0.18
D	0.116	0.120	2.95	3.05
E	0.116	0.120	2.95	3.05
e	0.0256		0.65	
H	0.188	0.198	4.78	5.03
L	0.016	0.026	0.41	0.66
α	0°	6°	0°	6°

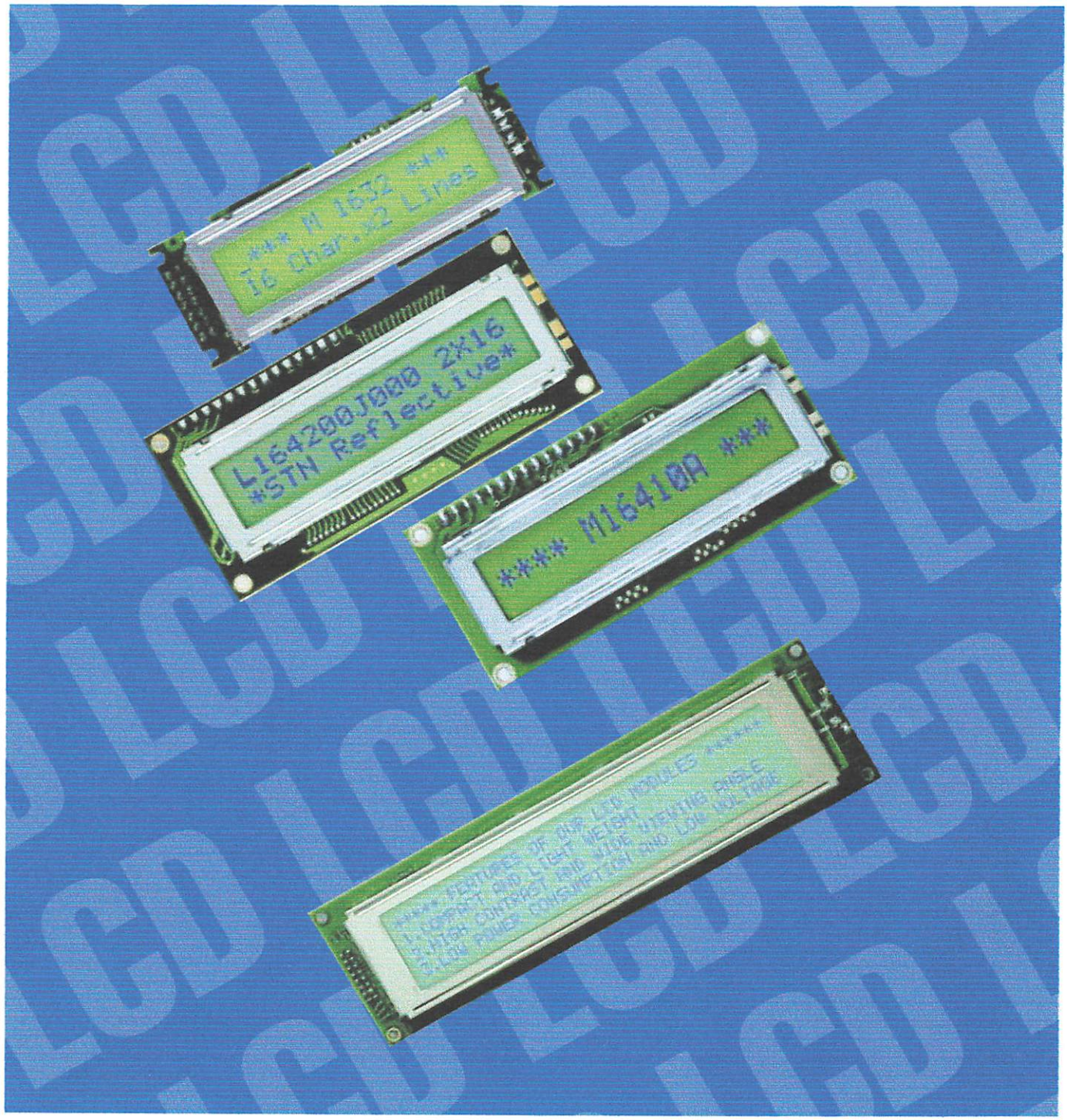
21-0036D

8-PIN μMAX
MICROMAX SMALL-OUTLINE
PACKAGE

LCM

Liquid Crystal Display Modules

Seiko Instruments GmbH

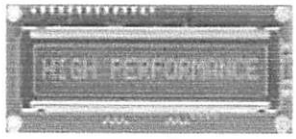


Dot Matrix Liquid Crystal Display Modules

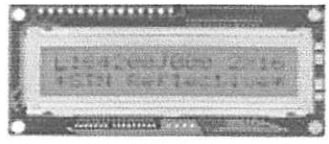
CHARACTER TYPE

• FEATURES :

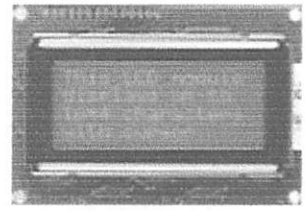
- Slim, light weight and low power consumption
- High contrast and wide viewing angle
- Built-in controller for easy interfacing
- LCD modules with built-in EL or LED backlight



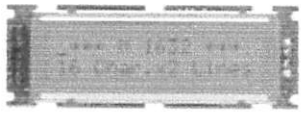
M1641



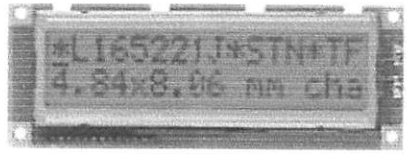
L1642



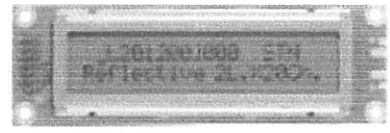
L1614



M1632



L1652



L2012

• SPECIFICATIONS :

: Standard products : Products of optional specification

Character Format (character x line)			16 x 1	16 x 2	16 x 2	16 x 2	16 x 4	20 x 2
Model			M1641	M1632	L1642	L1652	L1614	L2012
Reflective			M16410AS	M16320AS	L164200J000S	L165200J200S	L161400J000S	L201200J000S
EL backlight			M16419DWS	M16329DWS	L164221J000S	L165221J200S	L161421J000S	L201221J000S
LED backlight			M16417DYS	M16327DYS	L1642B1J000S	L1652B1J200S	L1614B1J000S	L2012B1J000S
Reflective (wide temp)			M16410CS	M16320CS	L164200L000S	L165200L200S	L161400L000S	L201200L000S
LED backlight (wide temp)			M16417JYS	M16327JYS	L1642B1L000S	L1652B1L200S	L1614B1L000S	L2012B1L000S
Character font			5x7 dots + cursor	5x7 dots + cursor	5x7 dots + cursor	5x7 dots + cursor	5x7 dots + cursor	5x7 dots + cursor
Module size (HxVxT) mm	Reflective		80,0 x 36,0 x 11,3	85,0 x 30,0 x 10,1	80,0 x 36,0 x 11,3	122,0 x 44,0 x 11,3	87,0 x 60,0 x 11,6	116,0 x 37,0 x 11,3
	EL backlight		80,0 x 36,0 x 11,3	85,0 x 30,0 x 10,1	80,0 x 36,0 x 11,3	122,0 x 44,0 x 11,3	87,0 x 60,0 x 11,6	116,0 x 37,0 x 11,3
	LED backlight		80,0 x 36,0 x 15,8	80,0 x 30,0 x 15,8	80,0 x 36,0 x 15,8	122,0 x 44,0 x 15,8	87,0 x 60,0 x 15,8	116,0 x 37,0 x 15,8
Viewing area (HxV) mm			64,5 x 13,8	62,0 x 16,0	64,5 x 13,8	99,0 x 24,0	61,8 x 25,2	83,0 x 18,6
Character size (HxV) mm *1			3,07 x 5,73	2,78 x 4,27	2,95 x 3,80	4,84 x 8,06	2,95 x 4,15	3,20 x 4,85
Dot size (HxV) mm			0,55 x 0,75	0,50 x 0,55	0,50 x 0,55	0,92 x 1,10	0,55 x 0,55	0,60 x 0,65
Power supply voltage (VDD-VSS) V			+ 5 V	+ 5 V	+ 5 V	+ 5 V	+ 5 V	+ 5 V
Current consumption (mA,typ)		IDD	1,5	2,0	1,6	2,0	2,7	2,0
		ILC *4	0,2	0,2	0,3	0,4	1,1	0,4
Driving method (duty)			1/16	1/16	1/16	1/16	1/16	1/16
Built-in LSI			KS0066 or equivalent	KS0066 MSM5839 or equivalent	KS0066 MSM5839 or equivalent	KS0066 MSM5839 or equivalent	KS0066 KS0063 or equivalent	KS0066 KS0063 or equivalent
Operating temperature (°C)		normal temp.	0 to + 50	0 to + 50	0 to + 50	0 to + 50	0 to + 50	0 to + 50
		wide temp. *2	- 20 to + 70	- 20 to + 70	- 20 to + 70	- 20 to + 70	- 20 to + 70	- 20 to + 70
Storage temperature (°C)		normal temp.	- 20 to + 60	- 20 to + 60	- 20 to + 60	- 20 to + 60	- 20 to + 60	- 20 to + 60
		wide temp.	- 30 to + 80	- 30 to + 80	- 30 to + 80	- 30 to + 80	- 30 to + 80	- 30 to + 80
Weight (g, typ.)	Reflective		25	25	25	50	50	40
	EL backlight		30	30	30	55	55	45
	LED backlight		35	40	35	65	65	60
Inverters for EL	Model		5S	5S	5S	5C	5A	5A
	Power supply (V)		+ 5.0	+ 5.0	+ 5.0	+ 5.0	+ 5.0	+ 5.0
	current consumption (mA) *3		10	10	10	35	45	45
LED backlight	Forward current consumption (mA)		100	112	100	240	200	154
	Forward input voltage (V,typ.)		+ 4,1	+ 4,1	+ 4,1	+ 4,1	+ 4,1	+ 4,1

*1 : Excluding cursor

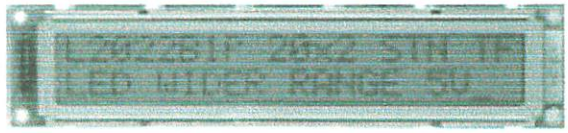
H : Horizontal V : Vertical T : Thickness (max)

*2 : With external temperature compensation

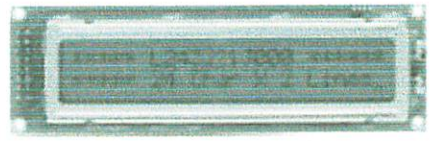
*3 : Including EL backlight

*4 : Based on normal temperature range

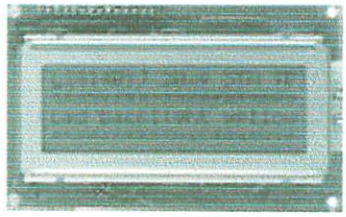
Since our policy is one of continues improvements we reserve the right to change the specifications for the products in the catalogue without notice.



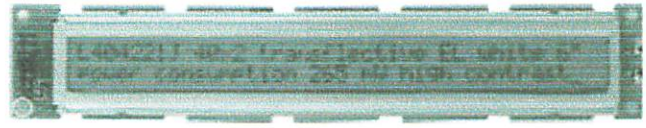
L2022



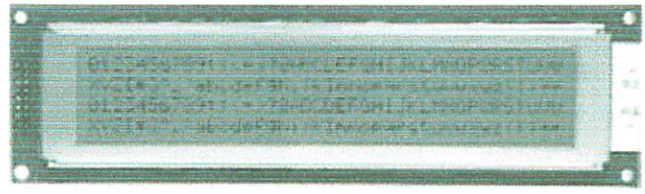
L2432



L2014



L4042



M4024

• SPECIFICATIONS :

: Standard products : Products of optional specification

Character Format (character x line)			20 x 2	20 x 4	24 x 2	40 x 2	40 x 4
Model			L2022	L2014	L2432	L4042	M4024
Reflective			-	L201400J000S	L243200J000S	L404200J000S	M40240AS
EL backlight			-	L201421J000S	L243221J000S	L404221J000S	M40249DWS
LED backlight			-	L2014B1J000S	L2432B1J000S	L4042B1J000S	M40247DYS
Reflective (wide temp)			L202200P000S	L201400L000S	L243200L000S	L404200L000S	M40240CS
LED backlight (wide temp)			L2022B1P000S	L2014B1L000S	L2432B1L000S	L4042B1L000S	M40247JYS
Character font			5x7 dots + cursor	5x7 dots + cursor	5x7 dots + cursor	5x7 dots + cursor	5x7 dots + cursor
Module size (HxVxT) mm		Reflective	180,0 x 40,0 x 10,5	98,0 x 60,0 x 11,6	118,0 x 36,0 x 11,3	182,0 x 33,5 x 11,3	190,0 x 54,0 x 10,1
		EL backlight	180,0 x 40,0 x 10,5	98,0 x 60,0 x 11,6	118,0 x 36,0 x 11,3	182,0 x 33,5 x 11,3	190,0 x 54,0 x 10,1
		LED backlight	180,0 x 40,0 x 14,8	98,0 x 60,0 x 15,8	118,0 x 36,0 x 15,8	182,0 x 33,5 x 16,3	190,0 x 54,0 x 16,3
Viewing area (HxV) mm			149,0 x 23,0	76,0 x 25,2	94,5 x 17,8	154,4 x 15,8	147,0 x 29,5
Character size (HxV) mm *1			6,00 x 9,66	2,95 x 4,15	3,20 x 4,85	3,20 x 4,85	2,78 x 4,27
Dot size (HxV) mm			1,12 x 1,12	0,55 x 0,55	0,60 x 0,65	0,60 x 0,65	0,50 x 0,55
Power supply voltage (VDD-VSS) V			+ 5 V	+ 5 V	+ 5 V	+ 5 V	+ 5 V
Current consumption (mA,typ)		IDD	4,2	2,9	2,5	3,0	8,0
		ILC *4	2,6	1,2	0,5	1,0	3,0
Driving method (duty)			1/16	1/16	1/16	1/16	1/16
Built-in LSI			KS0066 KS0063 or equivalent	KS0066 MSM5839 or equivalent	KS0066 KS0063 or equivalent	KS0066 KS0063 or equivalent	KS0066 MSM5839 or equivalent
Operating temperature (°C)		normal temp.	-	0 to + 50	0 to + 50	0 to + 50	0 to + 50
		wide temp. *2	- 20 to + 70	- 20 to + 70	- 20 to + 70	- 20 to + 70	- 20 to + 70
Storage temperature (°C)		normal temp.	-	- 20 to + 60	- 20 to + 60	- 20 to + 60	- 20 to + 60
		wide temp.	- 30 to + 80	- 30 to + 80	- 30 to + 80	- 30 to + 80	- 30 to + 80
Weight (g, typ.)		Reflective	80	55	40	70	90
		EL backlight	-	60	45	75	105
		LED backlight	110	70	60	95	140
Inverters for EL		Model	-	5A	5A	5C	5D
		Power supply (V)	+ 5.0	+ 5.0	+ 5.0	+ 5.0	+ 5.0
		current consumption (mA) *3	-	45	45	25	80
LED backlight		Forward current consumption (mA)	320	240	150	260	480
		Forward input voltage (V,typ.)	+ 4,1	+ 4,1	+ 4,1	+ 4,1	+ 4,1

*1 : Excluding cursor H : Horizontal V : Vertical T : Thickness (max)

*2 : With external temperature compensation

*3 : Including EL backlight

*4 : Based on normal temperature range

Dot Matrix Liquid Crystal Display Modules

GRAPHIC TYPE

- **FEATURES :**
  - •Wide viewing angle and high contrast
  - •Full dot configuration fits any application
  - •Slim, light weight and low power consumption
  - •Available in STN and FSTN

- **SPECIFICATIONS :**

Dot format (HxV,dot)			97 x 32	128 x 32	128 x 64	128 x 64
Model			Y97031	G1213	G1216	G1226
STN type (Gray mode)	Reflective	built-in RAM	-	-	-	-
	Reflective wide temp.	built-in RAM	-	G121300N000S	G121600N000S	-
	LED backlight	built-in RAM	-	-	-	G1226B1J000S
	LED backlight wide temp	built-in RAM	-	G1213B1N000S	G1216B1N000S	-
FSTN type (B&W mode)	Transmissive	-	-	-	-	-
	with CFL backlight	built-in controller	-	-	-	-
	Transflective	built-in RAM	Y97031LF60W	-	-	-
Module size (H x V x T) mm	Reflective (no backlight)		47,5 x 65,4 x 2,1	75,0 x 41,5 x 6,8	75,0 x 52,7 x 6,8	-
	LED backlight		-	75,0 x 41,5 x 8,9	75,0 x 52,7 x 8,9	93,0 x 70,0 x 11,4
	CFL backlight		-	-	-	-
Viewing area (HxV) mm			43,5 x 23,9	60,0 x 21,3	60,0 x 32,5	70,7 x 38,8
Dot size (H x V) mm			0,35 x 0,48	0,40 x 0,48	0,40 x 0,40	0,44 x 0,44
Dot pitch (H x V) mm			0,39 x 0,52	0,43 x 0,51	0,43 x 0,43	0,48 x 0,48
Power supply voltage (V)		(VDD - VSS)	+5,0	+5,0	+5,0	+5,0
		(VLC - VSS)	-	- 8,0	- 8,1	-8,2
Current consumption (mA, typ.)		IDD	0,10	2,0	2,0	3,0
		IDD (built-in controller)	-	-	-	-
		ILC	-	1,8	1,8	2,0
Driving method (duty)			1/33	1/64	1/64	1/64
Built-in LSI		Driver	SED1530 or equivalent	HD61202 HD61203 or equivalent	HD61202 HD61203 or equivalent	KS0107 KS0108 or equivalent
		Controller	-	-	-	-
Operating temperature range (°C)			- 20 to + 70	- 20 to + 70	- 20 to + 70	0 to + 50
Storage temperature range (°C)			- 30 to + 80	- 30 to + 80	- 30 to + 80	- 20 to + 60
Weight (g, typ.)	Reflective (Transflective no backlight)		10	23	35	-
	LED backlight		-	35	45	72
	CFL backlight		-	-	-	-
LED backlight	Forward current consumption (mA)		-	40	90	125
	Forward input voltage (V, typ.)		-	3,8	4,1	4,1
Inverter for CFL	Mode		-	-	-	-
	Power supply voltage (V)		-	-	-	-
	Current consumption (mA, typ.)		-	-	-	-

*1 : built-in DC/DC converter (single power source)

*2 : Use with external temperature compensation circuit

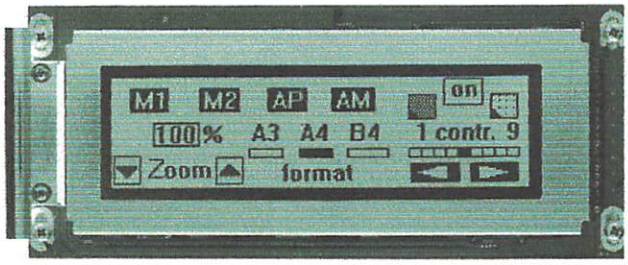
Since our policy is one of continues improvements we reserve the right to change the specifications of the products in the catalogue without notice.

Dot format (HxV,dot)			240 x 64	240 x 128	320 x 200	320 x 240	640 x 200
Model			G2446	G242C	G321D	G324E	G649D
STN type (Gray mode)	Reflective	built-in RAM	-	-	-	-	-
	Reflective wide temp.	built-in RAM	-	-	-	-	-
	LED backlight	built-in RAM	-	-	-	-	-
	LED backlight wide temp	built-in RAM	-	-	-	-	-
FSTN type (B&W mode)	Transmissive	-	G2446X5R1A0S	G242CX5R1ACS	G321DX5R1A0S	G324EX5R1A0S	G649DX5R010S
	with CFL backlight	built-in controller	G2446X5R1ACS	G242CX5R1A0S	G321DX5R1ACS	G324EX5R1ACS	-
	Transflective	built-in RAM	-	-	-	-	-
Module size (H x V x T) mm	Reflective (no backlight)			-	-	-	-
	LED backlight			-	-	-	-
	CFL backlight		191,0 x 79,0 x 15,1	180,0 x 110,0 x 15,1	166,0 x 134,0 x 15,1	166,0 x 134,0 x 15,1	260,0 x 122,0 x 15,7
Viewing area (HxV) mm			134,0 x 41,0	134,0 x 76,0	128,0 x 110,0	128,0 x 110,0	216,0 x 83,0
Dot size (H x V) mm			0,49 x 0,49	0,47 x 0,47	0,34 x 0,48	0,32 x 0,39	0,30 x 0,36
Dot pitch (H x V) mm			0,53 x 0,53	0,51 x 0,51	0,38 x 0,52	0,36 x 0,43	0,33 x 0,39
Power supply voltage (V)		(VDD - VSS)	+5,0	+5,0	+5,0	+5,0	+5,0
		(VLC - VSS)	*1	*1	-24,0	-24,0	-24,0
Current consumption (mA, typ.)		IDD	12	30	8	7,5	11
		IDD (built-in controller)	15	40	23	23	-
		ILC	-	-	6	6,5	9
Driving method (duty)			1/64	1/128	1/200	1/240	1/200
Built-in LSI		Driver	MSM5298 MSM5299 or equivalent	KS0103 KS0104 or equivalent	MSM5298 MSM5299 or equivalent	HD66204 HD66205 or equivalent	MSM5298 MSM5299 or equivalent
		Controller	SED1330FB	SED1330FB	SED1330FB	SED1330FB	-
Operating temperature range (°C)			0 to +50	0 to +50	0 to +50	0 to +50	0 to +50
Storage temperature range (°C)			- 20 to +60	- 20 to +60	- 20 to +60	- 20 to +60	- 20 to +60
Weight (g, typ.)	Reflective (Transflective no backlight)		-	-	-	-	-
	LED backlight		-	-	-	-	-
	CFL backlight		200	280	350	350	420
LED backlight	Forward current consumption (mA)		-	-	-	-	-
	Forward input voltage (V, typ.)		-	-	-	-	-
Inverter for CFL	Mode		4800210	4800210	4800210	4800210	4800120
	Power supply voltage (V)		+5,0	+5,0	+5,0	+5,0	+12,0
	Current consumption (mA, typ.)		250	350	365	365	390

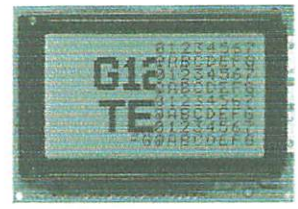
*1 : built-in DC/DC converter (single power source)

*2 : Use with external temperature compensation

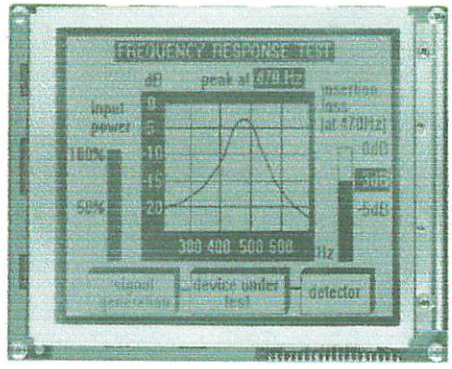
Since our policy is one of continous improvements, we reserve the right to change the specifications of the products in the catalogue without notice.



G2446

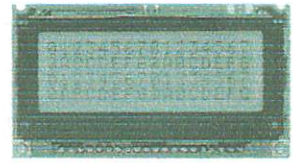


G1226

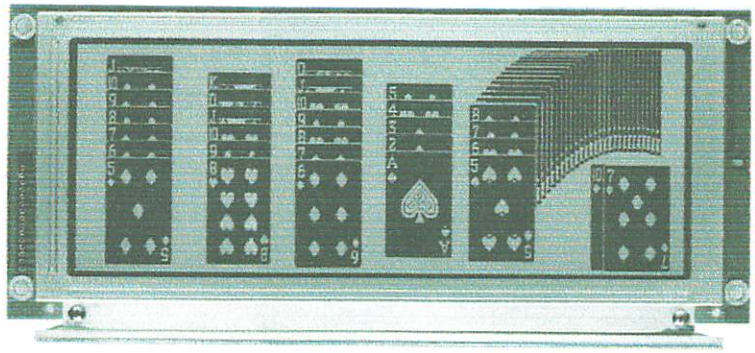


G321D

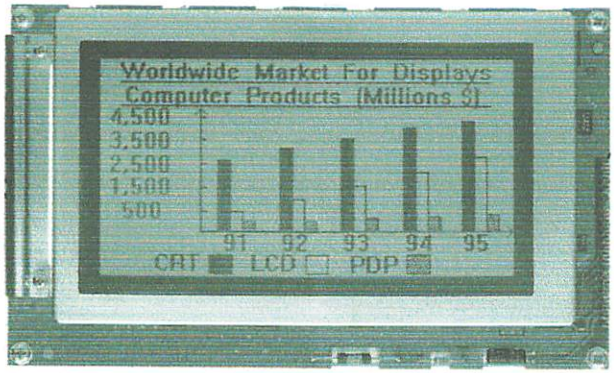
G1216



G1213



G649D



G242C

G324E

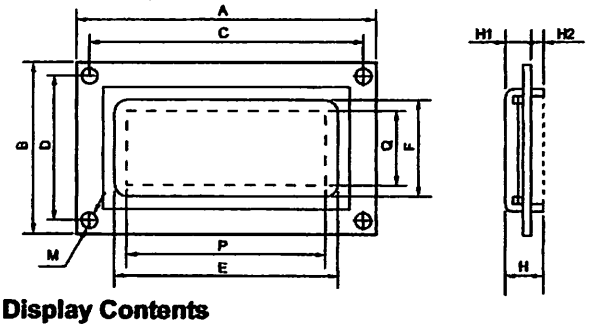
CHECK LIST FOR CUSTOM DESIGNED LCD MODULE

1. Company_____ **2. Application**_____ **3. Customer Specified Part No.**_____

4. Design

☐ New ☐ Modified : Manufacturer_____, Part No._____, Remarks _____
☐ Equivalent: Manufacturer_____, Part No._____, Remarks _____

5. LCM Dimensions



A x B : Module size_____ x _____ mm
E x F : Viewing area_____ x _____ mm
P x Q : Active display area_____ x _____ mm
C : Length between mounting holes_____ mm
D : Length between mounting holes_____ mm
M : Diameter of mounting hole_____ mm
H : Total thickness_____ mm
H1 : Upper thickness_____ mm
H2 : Lower thickness_____ mm

6. Display Contents

☐ Character type:_____characters_____lines
Character font_____x_____dots + cursor
Character pitch_____x_____mm
Dot pitch_____x_____mm
Dot size_____x_____mm
☐ Graphics (Full dot) type:_____x_____dots
Dot pitch_____x_____mm
Dot size_____x_____mm
☐ Segment type:_____digits_____lines
☐ Others_____

7. LCD Panel

Viewing angle: ☐ 6 o'clock ☐ 12 o'clock ☐____ o'clock
Type: ☐ TN ☐ FSTN (Black and white)
☐ STN (☐ Yellow green ☐ Gray ☐ Blue)
Chromaticity coordinates
(_____ ≦ x ≦ _____ , _____ ≦ y ≦ _____)
☐ Positive type ☐ Negative type
☐ Reflective ☐ Transflective ☐ Transmissive
☐ Others_____
Gray scale: ☐ Yes_____ gray scale ☐ No
Preferential specifications:
☐ Response time t_{on} ____ ms (____ °C) t_{off} ____ ms (____ °C)
☐ Viewing angle____ deg. (____ °C) ☐ Contrast____ (____ °C)
☐ Others_____
LCD surface finishing:
☐ Normal ☐ Anti-glare ☐_____
Polarizer color: ☐ Normal (neutral gray) ☐ Red
☐ Green ☐ Blue ☐_____

8. Driving Method

Multiplexing:1/_____duty, 1/_____bias
Frame frequency: _____Hz

9. IC

LCD driver: ☐ Specified ☐ Unspecified
Segment driver _____(Manufacturer _____)
Common driver _____(Manufacturer _____)
Controller: ☐ Internal ☐ External
Type No._____(Manufacturer _____)
MPU: ☐ Internal ☐ External
Type No._____(Manufacturer _____)
RAM: ☐ Internal ☐ External
Type No. /Memory size____(Kbit) (Manufacturer _____)

10. Power Supply

☐ Single power supply: ☐ 5V ☐_____V
☐ 2 power supplies
For logic: (V_{DD}-V_{SS}) : ☐ 5V ☐_____V
For LC drive: (V_{LC}-V_{SS}) : ☐_____V

11. Temperature Compensation Circuit

☐ Internal ☐ External ☐ Unnecessary
Compensation range: ☐ 0°C to 50°C ☐ ___°C to ___°C

12. Current Consumption

For logic: typ._____mA, max._____mA
For LC drive: typ._____mA, max._____mA
Others ( ) : typ._____mA, max._____mA

13. Contrast Adjustment

☐ Internal ☐ External ☐ Unnecessary
Method: ☐ Temp. compensation circuit ☐ Volume ☐____

14. Temperature Range

Operating temperature range: ☐ 0°C to 50°C ☐____°C to____°C
Storage temperature range: ☐ -20°C to 60°C ☐____°C to____°C

15. Input/Output Terminals

Specifying allocation: ☐ Yes ☐ No
Specifying position: ☐ Yes ☐ No

16. Weight

typ._____g, max._____g

17. Connector

☐ Internal ☐ External ☐ Unnecessary
Type No._____(Manufacturer _____)

18. Backlight

☐ Internal ☐ External ☐ Unnecessary
☐ EL: ☐ Green ☐ White ☐_____
☐ LED: ☐ Yellow green ☐ Amber ☐_____
☐ CFL: ☐ White ☐_____
☐ Incandescent lamp ☐ Others_____
☐ Backlight type ☐ Edge backlight type
Brightness:_____cd/m²
Inverter: ☐ Internal ☐ External ☐ Unnecessary
Power supply voltage_____V
Current consumption (backlight included)_____mA
Brightness control: ☐ Yes ☐ No

19. Others

_____
_____
_____

20. Schedule

Estimate:_____
Sample: Delivery_____, Quantity:_____pcs
Mass production: Target price:_____
Delivery _____, Total quantity:_____pcs
Quantity per month_____pcs

CHECK LIST FOR CUSTOM DESIGNED LCD

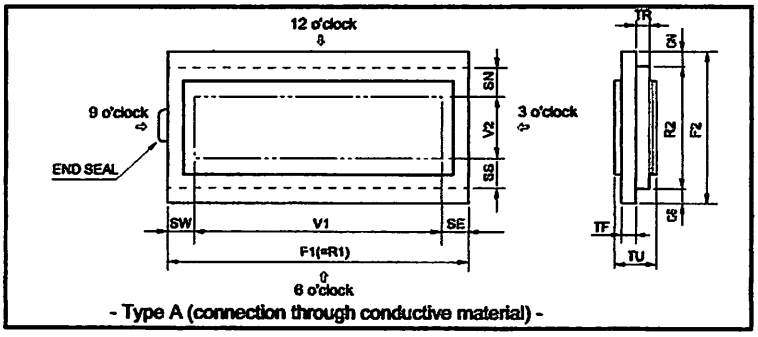
1. Company_____ **2. Application**_____ **3. Customer Specified Part No.**_____

4. Design

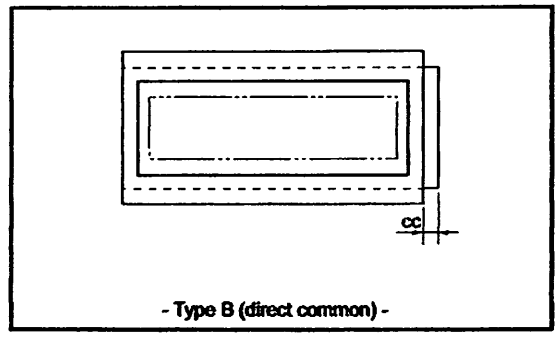
☐New ☐Modified: Manufacturer _____ , Part No._____ , Remarks_____

☐Equivalent: Manufacturer_____ , Part No._____ , Remarks_____

5. Panel Dimensions



- Type A (connection through conductive material) -



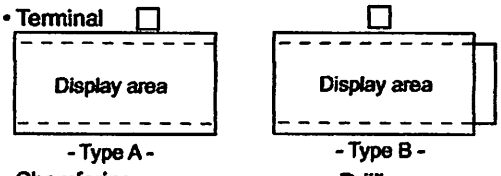
- Type B (direct common) -

F1: Horizontal length of upper glass _____ mm
F2: Vertical length of upper glass_____ mm
R1: Horizontal length of lower glass_____ the same as F1
R2*: Vertical length of lower glass_____ mm
*R2 is generally longer than F2 when terminals are with pin.
TF, TR***: Thickness of glass_____ mm
***Standard type: 1.1 mm or 0.7 mm
TU: Thickness of LCD_____ mm
End seal: ☐Right ☐Left ☐Right or Left

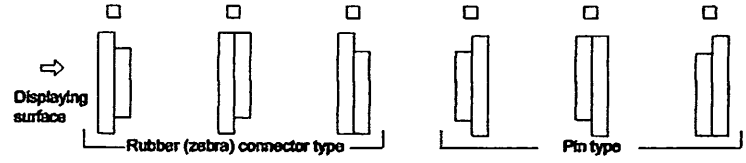
V1 :Horizontal length of viewing area _____ mm
V2 :Vertical length of viewing area _____ mm
CN**: Terminal length_____ mm
CS**:Terminal length_____ mm
**CN or CS=0 in case of one side terminal type.
CC: Terminal length_____ mm
SE,SW,SN,SS : Seal width
(According to design or manufacturing condition:
about 2.0 mm to 4.0 mm)

6. Panel Form

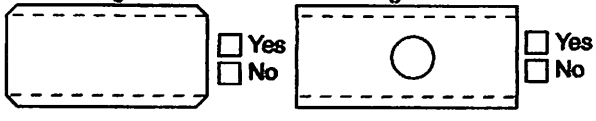
• Terminal ☐



- Type A - - Type B -



• Chamfering • Drilling



☐Yes ☐No ☐Yes ☐No

7. Display Mode

Viewing angle : ☐6 o'clock ☐12 o'clock ☐_____o'clock
Type: ☐TN ☐FSTN (Black and white)
☐STN: (☐Yellow green ☐Gray ☐Blue)
Chromaticity coordinates (____≦x≦____, ____≦y≦____)
☐Positive type ☐Negative type
☐Reflective ☐Transflective ☐Transmissive
Preferential specifications:
☐Response time t_{on} ____ ms (____ °C) t_{off} ____ ms (____ °C)
☐Viewing angle ____ deg. (____ °C) ☐Contrast ____ (____ °C)
☐Others_____

8. Polarizer

Surface finishing: ☐Normal ☐Anti-glare ☐_____
Color: ☐Normal (neutral gray) ☐Red ☐Green
☐Blue ☐_____
Front polarizer : ☐Attached type ☐Separate type
Rear polarizer : ☐Attached type ☐Separate type

9. Driving Method

☐Static ☐Multiplexing: (1/_____duty, 1/_____bias)
Operating voltage (V_{opr}) :_____V
Frame frequency:_____Hz
Driving IC: _____(Manufacturer _____)
Current consumption:_____μA

10. Temperature Range

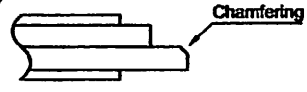
Operating temperature range
☐With temperature compensation circuit (or volume)
(☐0°C to 50°C ☐_____°C to_____°C)
☐Without temperature compensation circuit
(☐0°C to 50°C ☐_____°C to_____°C)
Storage temperature range
(☐-20°C to 60°C ☐_____°C to_____°C)

11. Terminal Connecting Method

☐Rubber connector (Zebra rubber)
☐Pin: ☐DIL ☐SIL ☐_____
Pitch (☐2.54 ☐_____mm) Length (_____mm)
☐Heat seal: ☐Equipped ☐Unnecessary

12. Others

Print (Characters, lines, masks etc.) : ☐Yes ☐No
Protective film:
☐Yes (Color: ☐Red ☐Translucent ☐Transparent) ☐No
Chamfering (for heat-seal connector) :
☐Yes (Position:_____)
(Quantity:_____)
☐No



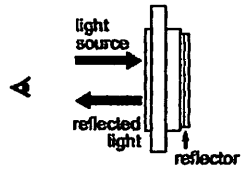
13. Schedule

Estimate :_____
Sample : Delivery_____ , Quantity :_____pcs
Mass production : Target price : _____
Delivery _____ , Total quantity:_____pcs
Quantity per month:_____pcs

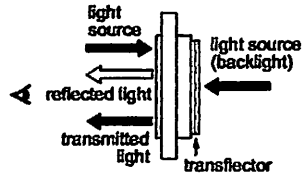
Liquid Crystal Display Modules

■ REFLECTIVE/TRANSFLECTIVE/TRANSMISSIVE LCD

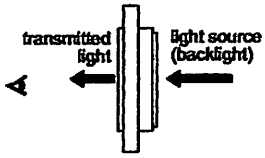
❶ Reflective LCD
Reflector bonded to the rear polarizer reflects the incoming ambient light. Low power consumption because no backlight is required.



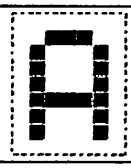
❷ Transflective LCD
Transflector bonded to the rear polarizer reflects light from the front as well as enabling lights to pass through the back. Used with backlight off in bright light and with it on in low light to reduce power consumption.

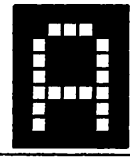
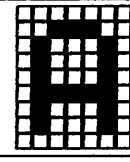


❸ Transmissive LCD
Without reflector or transflector bonded to the rear polarizer. Backlight required. Most common is transmissive negative image.



■ POSITIVE/NEGATIVE MODE

Positive type	

Negative type		Negative type (inverse image) (when data is inverted)	

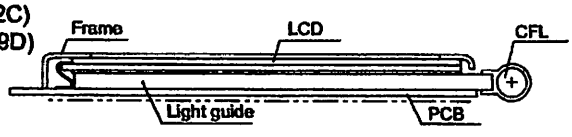
■ TN TYPE/STN TYPE/FSTN TYPE

TN	(Background/dot color) Gray/Black	TN(Twisted Nematic) type is most conventional and economical. It is used for static drive LCD and low-duty drive LCD (watch,calculator, etc.)
STN	Yellowgreen/Dark blue Gray/Dark blue White/Blue	STN (Super Twisted Nematic) type has a higher twist angle, and thus provides clear visibility and wider viewing angle. This is suitable especially for high-duty drive LCD.
FSTN	White/Black	FSTN (Film Super Twisted Nematic) type utilizes RCF (Retardation Control Film) to remove the coloring of STN LCD. Thus FSTN type provides easy-to-read black-and-white display.

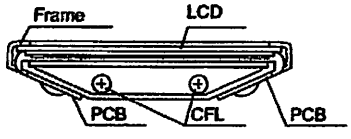
■ STRUCTURE AND FEATURE OF LCD MODULE WITH BACKLIGHT

CFL (Cold Cathode Fluorescent Lamp) backlight
Features: high brightness, long service life, inverter required

- Edge backlight type
  (G2446,G242C)
  (G321D,G649D)

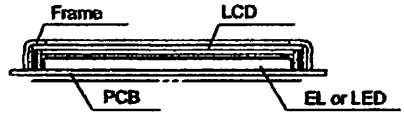


- Backlight type



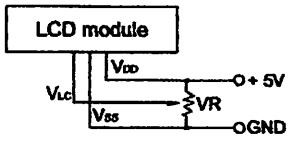
EL (Electroluminescent Lamp) backlight
LED (Light Emitting Diode) backlight

Features: EL: thin, inverter required
LED: long service life, low voltage driving, no inverter required

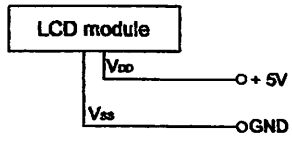


■ POWER SUPPLY

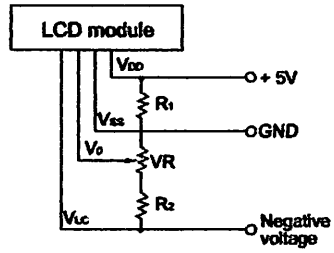
- Character modules (single power supply)



- G2446,G242C (Built-in DC-DC conv.)

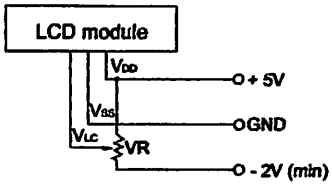


- G321D, G324E and G649D

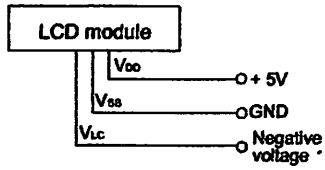


Note 1:Contrast can be adjusted by VR.
Note 2:For module with backlight, power supply for backlight is necessary.

- Character Modules(Dual power supply)



- Y1206 and G1226



·Negative voltage should be variable for contrast adjustment.

Precautions

Safety Instructions

- If the LCD panel is damaged, be careful not to get the liquid crystal in your mouth and not to be injured by crushed glasses.
- If you should swallow the liquid crystal, first, wash your mouth thoroughly with water, then, drink a lot of water and induce vomiting, and then, consult a physician.
- If the liquid crystal should get in your eye, flush your eye with running water for at least fifteen minutes.
- If the liquid crystal touches your skin or clothes, remove it and wash the affected part of your skin or clothes with soap and running water.
- EL or CFL backlight is driven by a high voltage with an inverter. Do not touch the connection part or the wiring pattern of the inverter.
- Do not use inverters without a load or in the short-circuit mode.
- Use the LCD module within the rated voltage to prevent overheating and/or damage. Also, take steps to ensure that the connector does not come off.

Handling Precautions

- Since the LCD panel has glass substrate, avoid applying mechanical shock or pressure on the module. Do not drop, bend, twist or press the module.
- Do not soil or damage LCD panel terminals.
- Since the polarizer is made of easily-scratched material, be careful not to touch or place objects on the display surface.
- Keep the display surface clean. Do not touch it with your skin.
- CMOS LSI is used in the LCD module. Be careful of static electricity.
- Do not disassemble the module or remove the liquid crystal panel or the panel frame.
- Do not damage the film surface of the EL lamp; otherwise the lamp will be damaged by humidity.
- To set an EL lamp in an LCD module, push the EL lamp with its emitting side up, without pushing the rubber connectors too hard. If you damage them, the LCD module may not work properly.

Mounting and Designing

- To protect the polarizer and the LCD panel, cover the display surface with a transparent plate (e.g., acrylic or glass) with a small gap between the transparent plate and the display surface.
- Keep the module dry. Avoid condensation to prevent the transparent electrodes from being damaged.
- Drive LCD panel with AC waveform in which DC element is not included to prevent deterioration in the LCD panel.
- Contrast of LCD varies depending on the ambient temperature. To offer the optimum contrast, LC drive voltage should be adjusted. LCD driven in a high duty ratio must be provided with drive voltage adjustment method.
- Mount a LCD module with the specified mounting part/ holes.
- Design the equipment so that input signal is not applied to the LCD module while power supply voltage is not applied to it.
- Do not locate the CFL tube and the lamp lead wire close to a metal plate or a plated part inside the equipment. Otherwise stray capacity causes a drop in voltage, decreasing the brightness and the ability to start-up.

Cleaning

- Do not wipe the polarizer with a dry cloth, as it may scratch the surface.
- Wipe the LCD panel gently with a soft cloth soaked with a petroleum benzine.
- Do not use ketonic solvents (ketone and acetone)or aromatic solvents (toluene and xylene), as they may damage the polarizer.

Storing

- Store the LCD panel in a dark place, where the temperature is 25°C±10°C and the relative humidity below 65%. If possible, store the LCD panel in the packaging situation when it was delivered.
- Do not store the module near organic solvents or corrosive gases.
- Keep the module (including accessories) safe from vibration, shock and pressure.
- Use an LCD module with built-in EL backlight within six months of delivery.
- EL backlight is easily affected by environmental conditions such as temperature and humidity; the quality may deteriorate if stored for an extended period of time. Contact Seiko Instruments GmbH for details.
- Some parts of the backlight and the inverter generate heat. Take care so that the heat does not affect the liquid crystal or any other parts.
- Dust particles attached to the surface of the LCD or the surface of the backlight degrade the display quality. Be careful to keep dust out in designing the structure as well as in handling the module.
- Black or white air-bubbles may be produced if the LCD panel is stored for long time in the lower temperature or mechanical shocks are applied onto the LCD panel.

On This Brochure

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Notes :

FAIRCHILD SEMICONDUCTOR™

August 1986
Revised April 2000

DM74LS164
8-Bit Serial In/Parallel Out Shift Register

General Description

These 8-bit shift registers feature gated serial inputs and an asynchronous clear. A low logic level at either input inhibits entry of the new data, and resets the first flip-flop to the low level at the next clock pulse, thus providing complete control over incoming data. A high logic level on either input enables the other input, which will then determine the state of the first flip-flop. Data at the serial inputs may be changed while the clock is HIGH or LOW, but only information meeting the setup and hold time requirements will be entered. Clocking occurs on the LOW-to-HIGH level transition of the clock input. All inputs are diode-clamped to minimize transmission-line effects.

Features

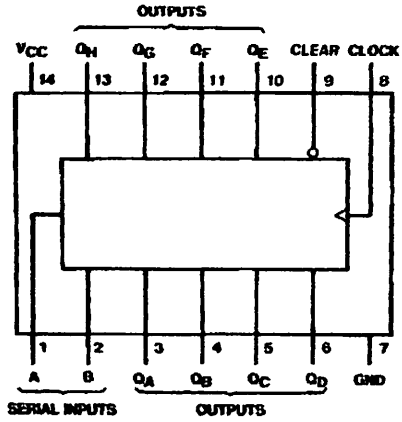
- Gated (enable/disable) serial inputs
- Fully buffered clock and serial inputs
- Asynchronous clear
- Typical clock frequency 36 MHz
- Typical power dissipation 80 mW

Ordering Code:

Order Number	Package Number	Package Description
DM74LS164M	M14A	14-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-120, 0.150 Narrow
DM74LS164N	N14A	14-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300 Wide

Devices also available in Tape and Reel. Specify by appending the suffix letter "X" to the ordering code.

Connection Diagram

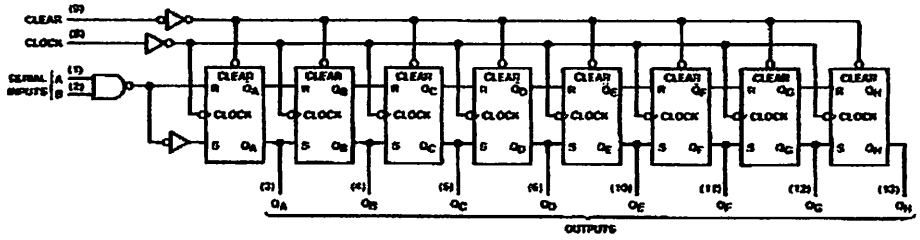


Function Table

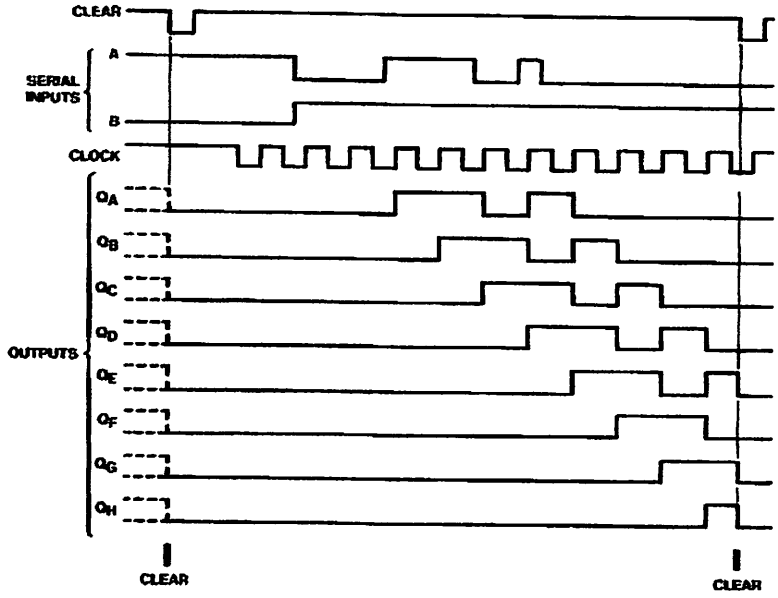
Inputs				Outputs			
Clear	Clock	A	B	Q_A	Q_B	...	Q_H
L	X	X	X	L	L	...	L
H	L	X	X	Q_{A0}	Q_{B0}	...	Q_{H0}
H	↑	H	H	H	Q_{An}	...	Q_{Gn}
H	↑	L	X	L	Q_{An}	...	Q_{Gn}
H	↑	X	L	L	Q_{An}	...	Q_{Gn}

H = HIGH Level (steady state)
L = LOW Level (steady state)
X = Don't Care (any input, including transitions)
↑ = Transition from LOW-to-HIGH level
Q_{A0}, Q_{B0}, Q_{H0} = The level of Q_A, Q_B, or Q_H, respectively, before the indicated steady-state input conditions were established.
Q_{An}, Q_{Gn} = The level of Q_A or Q_G before the most recent ↑ transition of the clock; indicates a one-bit shift.

Logic Diagram



Timing Diagram



Absolute Maximum Ratings (Note 1)

Supply Voltage	7V
Input Voltage	7V
Operating Free Air Temperature Range	0°C to +70°C
Storage Temperature Range	−65°C to +150°C

Note 1: The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the Electrical Characteristics tables are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" tables will define the conditions for actual device operation.

Recommended Operating Conditions

Symbol	Parameter		Min	Nom	Max	Units
V_{CC}	Supply Voltage		4.75	5	5.25	V
V_{IH}	HIGH Level Input Voltage		2			V
V_{IL}	LOW Level Input Voltage				0.8	V
I_{OH}	HIGH Level Output Current				−0.4	mA
I_{OL}	LOW Level Output Current				8	mA
f_{CLK}	Clock Frequency (Note 2)		0		25	MHz
t_W	Pulse Width	Clock	20			ns
	(Note 2)	Clear	20			
t_{SU}	Data Setup Time (Note 2)		17			ns
t_H	Data Hold Time (Note 2)		5			ns
t_{REL}	Clear Release Time (Note 2)		30			ns
T_A	Free Air Operating Temperature		0		70	°C

Note 2: $T_A = 25°C$ and $V_{CC} = 5V$.

Electrical Characteristics

over recommended operating free air temperature range (unless otherwise noted)

Symbol	Parameter	Conditions	Min	Typ (Note 3)	Max	Units
V_I	Input Clamp Voltage	V_{CC} = Min, I_I = −18 mA			−1.5	V
V_{OH}	HIGH Level Output Voltage	V_{CC} = Min, I_{OH} = Max, V_{IL} = Max, V_{IH} = Min	2.7	3.4		V
V_{OL}	LOW Level Output Voltage	V_{CC} = Min, I_{OL} = Max, V_{IL} = Max, V_{IH} = Min		0.35	0.5	V
		I_{OL} = 4 mA, V_{CC} = Min		0.25	0.4	
I_I	Input Current @ Max Input Voltage	V_{CC} = Max, V_I = 7V			0.1	mA
I_{IH}	HIGH Level Input Current	V_{CC} = Max, V_I = 2.7V			20	µA
I_{IL}	LOW Level Input Current	V_{CC} = Max, V_I = 0.4V			−0.4	mA
I_{OS}	Short Circuit Output Current	V_{CC} = Max (Note 4)	−20		−100	mA
I_{CC}	Supply Current	V_{CC} = Max (Note 5)		16	27	mA

Note 3: All typicals are at $V_{CC} = 5V$, $T_A = 25°C$.

Note 4: Not more than one output should be shorted at a time, and the duration should not exceed one second.

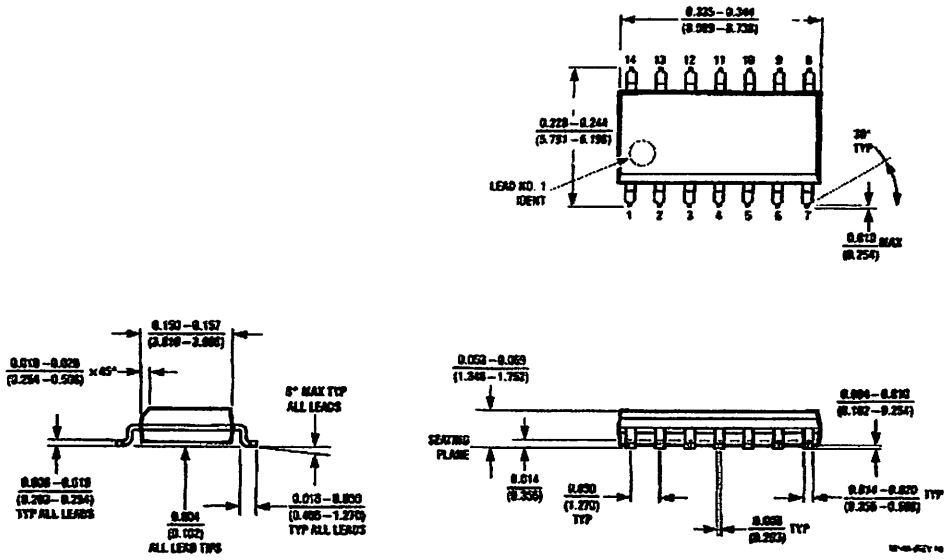
Note 5: I_{CC} is measured with all outputs OPEN, the SERIAL input grounded, the CLOCK input at 2.4V, and a momentary ground, then 4.5V, applied to the CLEAR input.

Switching Characteristics

at $V_{CC} = 5V$ and $T_A = 25°C$

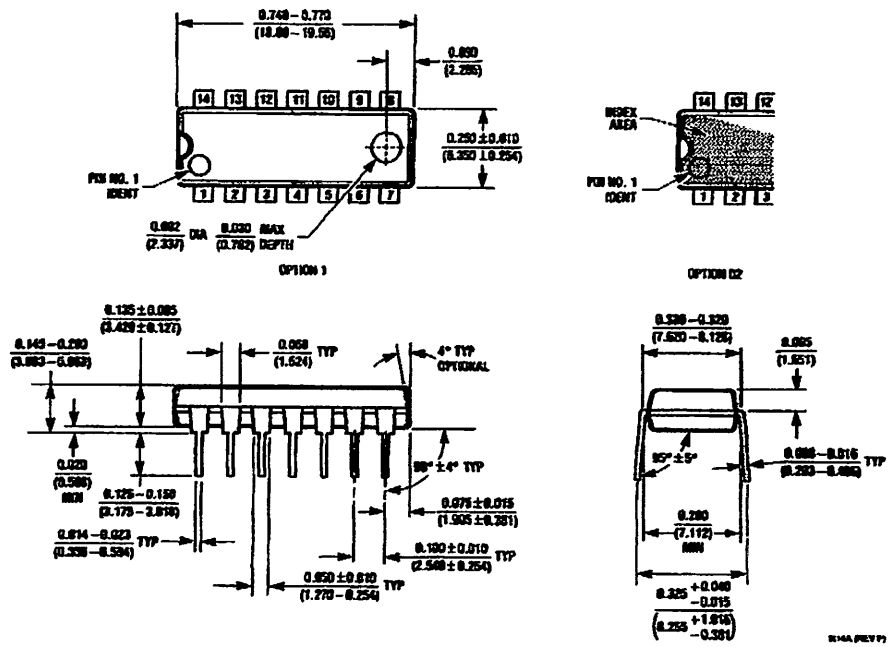
Symbol	Parameter	From (Input) To (Output)	$R_L = 2\ k\Omega$				Units
			$C_L = 15$ pF		$C_L = 50$ pF		
			Min	Max	Min	Max	
f_{MAX}	Maximum Clock Frequency		25				MHz
t_{PLH}	Propagation Delay Time LOW-to-HIGH Level Output	Clock to Output		27		30	ns
t_{PHL}	Propagation Delay Time HIGH-to-LOW Level Output	Clock to Output		32		40	ns
t_{PHL}	Propagation Delay Time HIGH-to-LOW Level Output	Clear to Output		36		45	ns

Physical Dimensions inches (millimeters) unless otherwise noted



14-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-120, 0.150 Narrow
Package Number M14A

Physical Dimensions inches (millimeters) unless otherwise noted (Continued)



14-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300 Wide
Package Number N14A