INSTITUT TEKNOLOGI NASIONAL MALANG
FAKULTAS TEKNOLOGI INDUSTRI
JURUSAN TEKNIK ELEKTRO S-1
KONSENTRASI TEKNIK ELEKTRONIKA

SKRIPSI

PERENCANAAN DAN PEMBUATAN ALAT PENGUKUR KADAR NATRIUM (Na) DALAM DARAH BERBASIS MIKROKONTROLLER AT89S8252

Disusun Oleh:
HESTI PUSPITA
NIM : 02.17.061

MARET 2007

LEMBAR PERSETUJUAN

PERENCANAAN DAN PEMBUATAN ALAT PENGUKUR
KADAR NATRIUM (Na) DALAM DARAH
BERBASIS MIKROKONTROLLER AT89S8252

SKRIPSI

Diajukan Guna Memenuhi Salah Satu Syarat Untuk Memperoleh Gelar Sarjana
Teknik Pada Jurusan Teknik Elektro S-1 Konsentrasi Elektronika

Disusun Oleh :

HESTI PUSPITA

NIM : 02.17.061

Mengetahui	Diperiksa dan Disetujui
Ketua Jurusan Teknik Elektro S-1	Dosen Pembimbing
(Ir. F. Yudi Limpraptono, MT)	**(I Komang Somawirata, ST,MT)**
NIP.Y. 1039500274	**NIP. 1030100361**

KONSENTRASI ELEKTRONIKA
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BERITA ACARA UJIAN SKRIPSI
FAKULTAS TEKNOLOGI INDUSTRI

Nama Mahasiswa	:	Hesti Puspita
NIM	:	02.17.061
Jurusan	:	Teknik Elektro S-1
Konsentrasi	:	Teknik Elektronika
Judul Skripsi	:	Perencanaan Dan Pembuatan Alat Pengukur Kadar Natrium (Na) Dalam Darah Berbasis Mikrokontroller AT89S8252

Dipertahankan dihadapan Team Penguji Skripsi Jenjang Strata Satu (S-1) Pada :

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Tanggal	:	17 Maret 2007
Dengan Nilai	:	84 (A)

Panitia Ujian Skripsi

Ketua	Sekretaris
(Ir.Mochtar Asroni, MSME)	**(Ir.F.Yudi Limpraptono, MT)**
NIP.Y. 1018100036	**NIP.Y. 1039500274**

Anggota Penguji

Penguji Pertama	Penguji Kedua
(Ir. Usman Djuanda , MM)	**(Ir. Teguh Herbasuki, MT)**
NIP. 1018700143	**NIP.Y. 1038900209**

ABSTRAKSI

PERENCANAAN DAN PEMBUATAN ALAT PENGUKUR KADAR NATRIUM (Na) DALAM DARAH BERBASIS MIKROKONTROLLER AT89S8252

(Hesti Puspita, 0217061, Teknik Elektro/Elektronika S-1)

(Dosen Pembimbing : I Komang Somawirata, ST, MT)

Kata Kunci : Natrium, Darah, Mikrokontroller AT89S8252

Pada skripsi ini dibuat sebuah alat yang dapat mengukur kadar natrium (Na) dalam darah pada manusia dengan menggunakan lampu tungsten halogen sebagai sumber cahaya yang mampu menghasilkan cahaya tampak dalam daerah panjang gelombang 350-2500 nm, dan untuk mendapatkan cahaya monokrom kuning dengan panjang gelombang 580-595 nm maka dipasang filter cahaya transparan kuning. Dan LDR (*Light Dependent Resistors*) NORP12 RS *stock number* 651-507 sebagai sensor.

Kerja dari alat pengukur kadar natrium (Na) darah ini adalah cahaya polikrom dari lampu difilter oleh transparan kuning sehingga menghasilkan cahaya monokrom kuning. Cahaya yang dilewatkan lalu difokuskan dan dilewatkan oleh sampel serum dan diterima oleh sensor LDR.

Dari hasil pengujian, untuk serum dengan kadar Na 135 mmol/L terdapat error 4 %, serum dengan kadar Na 141 mmol/L terdapat error 2,167 %, dan utnuk serum dengan kadar Na 151 mmol/L terdapat error 3,33 %. Waktu yang dibutuhkan lampu sampai mendapatkan cahaya yang diinginkan (cahaya putih) ± 20 detik. Jarak antara lampu sebagai sumber cahaya ke sensor baik dengan obyek penghalang atau tanpa obyek penghalang adalah ± 39 cm.

KATA PENGANTAR

Assalamu'alaikum Wr. Wb

Dengan memanjatkan puji syukur kepada Allah SWT atas segala rahmat dan hidayah serta atas bimbingan-Nya sehingga penyusun dapat menyelesaikan Laporan Skripsi yang berjudul "Perencanaan Dan Pembuatan Alat Pengukur Kadar Natrium (Na) Dalam Darah Berbasis Mikrokontroller AT89S8252" ini dengan lancar. Skripsi ini merupakan persyaratan kelulusan Studi di Jurusan Teknik Elektro S-1 Konsentrasi Teknik Elektronika Institut Teknologi Nasional Malang dan untuk mencapai gelar Sarjana Teknik.

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Malang, Maret 2007

Penulis

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BAB I

PENDAHULUAN

1.1. Latar Belakang

Dunia elektronika adalah dunia teknologi yang sangat luas, yang selalu berkembang dari waktu ke waktu. Seiring dengan perkembangannya banyak hal di dunia ini yang dapat dilakukan oleh dunia elektronika. Dari hal-hal yang bersifat rumit hingga yang sederhana seperti yang ada pada kehidupan sehari-hari.

Elektronika mencakup segala aspek kehidupan, diantaranya aspek kesehatan dalam hal ini bidang medica. Sebagian besar peralatan medis berbasis elektronika, hal ini berdampak sangat baik bagi kehidupan manusia. Efisiensi waktu sangat berperan penting dalam penerapannya.

Salah satu bentuk penerapan tersebut adalah pada pengukuran kadar natrium dalam darah manusia. Darah adalah suatu jaringan tubuh yan terdapat dalam pembuluh darah yang warnanya merah, warna merah tersebut tergantung pada banyakanya O_2 dan CO_2 di dalamnya. Darah beredar dalam tubuh karena adanya kerja jantung dan selama darah berada dalam pembuluh maka akan tetap encer, tetapi jika keluar dari pembuluhnya maka ia akan menjadi beku. Pembekuan ini dapat dicegah dengan mencampurkan dalam darah dengan sedikit sitrat natrikus.

Bagian-bagian darah adalah air, protein (albumin, globulin, protombin, fibrinogen), mineral (natrium, magnesium, kalsium, zat besi), dan bahan organik.

Pertukaran cairan tersebut harus seimbang, karena hal tersebut dapat menyebabkan terjadinya edema yaitu tertimbunnya cairan dalam jaringan karena gangguan keseimbangan cairan. Misalnya pengaruh natrium terhadap tubuh yang mana natrium merupakan cairan yang sangat peting dalam mempertahankan tekanan osmotik cairan tubuh. Kelebihan natrium (hipernatremia) dapat menyebabkan terjadinya tekanan darah tinggi, dan kekurangan natrium (hiponatremia) dapat menyebabkan terjadinya pembengkakan pada sel termasuk sel otak. Sehingga perlu dilakukan pengukuran terhadap kadar natrium dalam darah agar dapat dilakukan pencegahan lebih awal.

Pengukuran natrium biasa dilakukan oleh laboran, yang mana proses tersebut membutuhkan waktu yang lama dan faktor manusia (*human error*) di sini sangat besar pengaruhnya terhadap hasil yang di dapat. Proses pengukuran natrium dalam darah biasanya dilakukan dengan titrasi antara sitrat natrikus dan darah dengan perbandingan tertentu, selanjutnya dilakukan pemisahan natrium dari larutan lainnya menggunakan reaksi *reagen*. Seorang laboran harus teliti dan menjaga sterilisasi saat pencampuran larutan, karena hal tersebut dapat menyebabkan terjadinya kesalahan analisa atau perhitungan yang dapat berakibat fatal.

1.2. Rumusan Masalah

Dalam perencanaan dan pembuatan alat pengukur kadar natrium (Na) darah berbasis mikrokontroller AT89S8252, masalah yang muncul dapat dirumuskan sebagai berikut :

1. Bagaimana membuat alat atau perangkat keras untuk mengukur kadar natrium (Na) dalam darah yang berbasis mikrokontroller AT89S8252
2. Bagaimana membuat perangkat lunak yang berbasis mikrokontroller AT89S8252 untuk pengukuran kadar natrium (Na) dalam darah.

1.3. Tujuan

Tujuan dari penulisan skripsi ini adalah untuk merancang dan membuat alat yang dapat mengukur kadar natrium (Na) dalam darah manusia secara digital berbasis mikrokontroller AT89S8252.

1.4. Batasan Masalah

Mengacu pada permasalahan yang ada, maka diperlukan adanya batasan-batasan dalam pembahasannya, yaitu :

1. Menggunakan mikrokontroller AT89S8252 sebagai pemroses data utama
2. Perencanaan dan pembuatan alat ini khusus untuk pengukuran kadar natrium darah pada manusia
3. Tidak membahas tentang bagian-bagian darah yang lain
4. Tidak membahas proses pemisahan larutan secara kimiawi
5. Tidak membahas tentang rangkaian catu daya

1.5. Metodologi

Metodologi pembahasan yang digunakan dalam skripsi ini adalah sebagai berikut :

- Studi literatur :

  Mempelajari teori-teori yang menunjang kelancaran didalam proses pembuatan alat.

- Perencanaan dan pembuatan alat :

  Sebagai bentuk aplikasi, dibuat sebuah alat serta pembahasannya yang dimulai dari masing-masing blok diagram.

- Pengujian alat :

  Melakukan pengujian dari beberapa rangkaian yang dibuat, serta menganalisa hasil pengujian untuk kemudian diambil suatu kesimpulan.

1.6. Sistematika Penulisan

Penulisan skripsi ini terbagi dalam lima (5) bab dengan sistematika penulisan sebagai berikut :

BAB I PENDAHULUAN

Berisi latar belakang, rumusan masalah, tujuan, batasan masalah, metodologi, dan sistematika penulisan.

BAB II LANDASAN TEORI

Membahas teori-teori dasar yang mendukung perancangan dan pembuatan alat.

BAB III PERANCANGAN DAN PEMBUATAN ALAT

Membahas tentang perancangan dan pembuatan alat yang dilakukan perblok dari sistem secara keseluruhan.

BAB IV PENGUJIAN ALAT

Berisi cara pengujian alat dan analisa hasil pengujian yang dilakukan dari blok diagram hasil perancangan.

BAB V PENUTUP

Berisi kesimpulan dan saran yang memungkinkan sebagai pengembangan alat lebih lanjut

DAFTAR PUSTAKA

LAMPIRAN

BAB II

LANDASAN TEORI

2.1. Pendahuluan

Dalam bab ini akan dibahas tentang teori-teori dasar yang mendukung sistem alat pengukur kadar natrium (Na) dalam darah berbasis mikrokontroller AT89S8252. Teori-teori dasar ini langsung didapat dari data sheet maupun dari studi lapangan dan beberapa buku literatur. Pokok pembahasan pada bab ini adalah :

- Teori tentang Darah dan Natrium (Na) Darah
- Sumber Cahaya dan Spektrum Cahaya
- Transistor Bipolar
- Relay
- Sensor
- (*Analog to Digital Converter)* ADC 0808
- Mikrokontroller AT89S8252
- LCD (*Liquid Crystal Display*) M1632

2.2. Teori tentang Darah dan Natrium (Na) Darah

2.2.1. Darah

Darah adalah suatu jaringan tubuh yang terdapat di dalam pembuluh darah yang warnanya merah. Warna merah itu keadaannya tidak tetap tergantung pada banyaknya O_2 dan CO_2 didalamnya. Darah yang banyak mengandung CO_2 warnanya merah tua. Adanya O_2 dalam darah diambil dengan jalan bernapas, dan zat ini sangat berguna pada peristiwa pembakaran/metabolisme di dalam tubuh.

Darah selamanya beredar di dalam tubuh karena adanya kerja atau pompa jantung dan selama darah berada dalam pembuluh maka akan tetap encer, tetapi kalau darah keluar dari pembuluhnya maka darah akan jadi beku. Pembekuan ini dapat dicegah dengan mencampurkan ke dalam darah sedikit obat anti pembekuan/sitrat natrikus. Ini sangat berguna apabila darah tersebut diperlukan untuk transfusi darah.

Darah berperan penting dalam proses metabolisme tubuh, selain sebagai alat pengangkut (mengambil O_2 dari paru-paru dan mengangkat CO_2 dari jaringan), fungsi darah yang lain adalah sebagai pertahanan tubuh terhadap serangan bibit penyakit dan racun. Darah juga berfungsi untuk meyebarkan panas ke seluruh tubuh.

Bagian-bagian darah adalah air, protein (albumin, globulin, protombin, fibrinogen), mineral (natrium, magnesium, kalsium, zat besi), dan bahan organik. Dalam darah terdapat benda-benda kecil bundar yang disebut sel-sel darah yaitu eritrosit (sel darah merah), leukosit (sel darah putih), dan trombosit (sel pembeku darah). Sedangkan cairannya berwarna kekuning-kuningan disebut plasma darah.

Sekali darah membeku atau berkoagulasi, fase cairan sisanya disebut serum. Dan mineral darah terdapat dalam serum. Serum kekurangan faktor-faktor pembekuan (termasuk fibrinogen) yang normal berada dalam plasma tetapi telah terpakai selama proses koagulasi.

2.2.2. Natrium (Na) Darah

Natrium adalah kation utama cairan ekstrasel. Natrium sangat penting dalam mempertahankan tekanan osmotik cairan tubuh, sehingga natrium melindungi tubuh terhadap kehilangan cairan yang berlebihan. Natrium banyak ditemukan dalam bahan makanan yaitu garam dapur (NaCL), dan pada umumnya daging lebih banyak mengandung natrium daripada bahan makanan nabati.

Natrium dalam darah berperan penting pada saat pertukaran antar cairan karena proses tersebut tergantung pada tekanan osmotik. Pertukaran cairan tersebut harus seimbang, karena hal tersebut dapat menyebabkan terjadinya edema yaitu tertimbunnya cairan dalam jaringan karena gangguan keseimbangan cairan. Kadar Na dalam darah >145 mEq/l atau >340 mg/dl adalah kelebihan natrium (hipernatremia) yang dapat menyebabkan terjadinya tekanan darah tinggi/hipertensi, dan kadar Na darah <135 mEq/l atau <310 mg/dl adalah kekurangan natrium (hiponatremia) yang dapat menyebabkan terjadinya pembengkakan pada sel termasuk sel otak.

2.2.3. Pengukuran Natrium (Na) Darah

Pengukuran kadar natrium darah yang dilakukan dalam kedokteran klinis diawali dengan pengambilan darah yang melalui pembuluh vena. Darah yang diambil dimasukkan ke dalam tabung gelas percobaan kecil. Dan proses ini menentukan waktu pembekuan (*clotting time*). Harus dijaga agar tidak ada faktor jaringan dari tempat penusukan vena (*venipuncture*) yang masuk ke dalam tabung gelas percobaan. Selanjutnya, darah secara perlahan digoyang dengan teratur untuk menentukan waktu yang diperlukan untuk koagulasi. Jika darah yang diambil tersebut akan disimpan dan digunakan untuk proses transfusi darah, maka perlu ditambahkan antikoagulan atau larutan sitrat natrikus untuk mencegah pembekuan darah.

Setelah terjadi pembekuan, maka terdapat pemisahan antara bagian yang menggumpal dan bagian yang cair. Bagian yang menggumpal adalah sel-sel darah sedangkan bagian yang cair berupa cairan kekuningan adalah serum darah. Selanjutnya serum darah tersebut dipindahkan ke tabung percobaan kecil yang lain. Dalam serum terdapat berbagai mineral darah, jika ingin menganalisa salah satu mineral maka harus ditambahkan larutan reagen yang dapat memperkuat unsur dari mineral tersebut.

Terdapat berbagai metode yang digunakan dalam pengukuran mineral dalam darah. Salah satu metode yang digunakan adalah metode spektrometri absorbsi. Spektrometri absorbsi adalah sebuah metode untuk mengukur absorbsi/penyerapan cahaya dengan energi (panjang gelombang) tertentu oleh suatu atom/molekul. Absorbsi hanya terjadi jika selisish kedua tingkat energi

tersebut ($\Delta E = E_2 - E_1$) sesuai dengan energi cahaya (foton) yang datang, yaitu :

$$\Delta E = E_{foton}$$

Besar penyerapan cahaya (absorbansi) dari suatu kumpulan atom/molekul dinyatakan oleh Hukum Beer-Lambert, yang dapat dituliskan sebagai berikut :

$$A = \log (I_0 / I) = \varepsilon c l$$

dimana I_0 adalah intensitas berkas cahaya datang, I adalah intensitas berkas cahaya keluar, ε adalah molar absorbsivitas untuk panjang gelombang tertentu (dalam l mol^{-1} cm^{-1}), c adalah konsentrasi molar (mol l^{-1}), dan l adalah panjang/ketebalan dari bahan/medium yang dilintasi oleh cahaya (cm)

2.3. Sumber Cahaya dan Spektrum Cahaya

2.3.1. Lampu Tungsten Halogen

Lampu tungsten halogen termasuk dalam jenis lampu pijar. Lampu halogen diciptakan dengan memperbaiki proses lampu pijar biasa, yaitu dengan mengurangi masalah menguapnya tungsten. Kaca lampu dibuat dari kaca kuarsa yang tipis dan tahan panas, kemudian gas yang diisikan ditambahkan sedikit gas halogen.

Lampu tungsten halogen biasa dipakai sebagai sumber cahaya tampak. Lampu ini menghasilkan cahaya tampak dalam daerah panjang gelombang 350-2500 nm. Untuk keperluan spektroskopi cahaya tampak, hanya daerah 350-800 nm saja yang dimanfaatkan. Lampu tungsten halogen terbuat dari tabung kuarsa yang berisi filamen tungsten dan sejumlah kecil iodine. Filamen tungsten itu tidak lain adalah sebuah resistor (serupa dengan bola lampu untuk pemakaian

di rumah/kantor). Ketika filamen dialiri arus maka energi listrik tersebut diubah menjadi energi panas. Suhu dari filamen bisa mencapai lebih dari 2000^{0}C. Pada suhu yang demikian tinggi tersebut, energi panas (radiasi) dan cahaya terpancar dari filamen tadi.

Umumnya umur lampu pijar biasa hanya sekitar 750 hingga 1500 jam, sementara umur lampu halogen bisa mencapai 2000 hingga 4000 jam.

2.3.2. Spektrum Cahaya

Variasi warna suatu sistem berubah dengan berubahnya konsentrasi suatu komponen. Warna itu biasanya disebabkan oleh pembentukan suatu senyawa berwarna dengan ditambahkannya reagensia yang tepat, atau warna itu dapat melekat dalam penyusun yang diinginkan itu sendiri. Cahaya terdiri dari radiasi terhadap mana mata manusia peka. Gelombang dengan panjang berlainan akan menimbulkan cahaya dengan warna berlainan, sedangkan campuran cahaya dengan panjang-panjang gelombang ini akan menyusun cahaya putih. Cahaya putih meliputi seluruh spektrum nampak 400-760 nm. Hubungan antara panjang gelombang dengan warna pada cahaya dan warna komplementernya terlihat pada tabel 2.1. Warna komplementer diperlukan pada saat pemilihan filter, yang mana sebagai aturan umum filter terbaik untuk digunakan dalam penetapan tertentu adalah yang memberikan absorpsi maksimum atau transmisi minimum untuk konsentrasi tertentu. Metode pemilihan filter yang kurang baik diantaranya adalah penggunaan sebuah filter yang warnanya mendekati warna komplementer dari larutan tersebut.

Tabel 2-1
Warna dan Warna Komplementer

Panjang gelombang (nm)	Warna	Warna Komplementer
400 – 435	Ungu	Hijau Kekuningan
435 – 480	Biru	Kuning
480 – 490	Biru Kehijauan	Jingga
490 – 500	Hijau Kebiruan	Merah
500 – 560	Hijau	Ungu Kemerahan
560 – 580	Hijau kekuningan	Ungu
580 – 595	Kuning	Biru
595 – 610	Jingga	Biru Kehijauan
610 – 750	Merah	Hijau Kebiruan

Sumber : Buku Ajar VOGEL

2.4. Transistor Bipolar

Prinsip kerja transistor adalah arus bias base-emiter yang kecil mengatur besar arus kolektor-emiter. Bagian penting berikutnya adalah bagaimana caranya memberi arus bias yang tepat sehingga transistor dapat bekerja optimal.

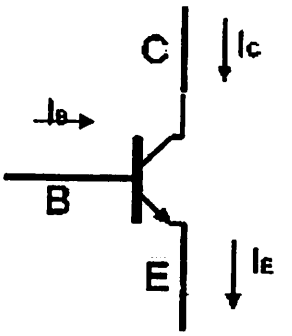
2.4.1. Arus bias

Ada tiga cara yang umum untuk memberi arus bias pada transistor, yaitu rangkaian *CE (Common Emitter), CC (Common Collector)* dan *CB (Common Base).* Namun dalam hal ini akan lebih detail dijelaskan bias transistor rangkaian CE. Dengan menganalisa rangkaian CE akan dapat diketahui beberapa parameter penting dan berguna terutama untuk memilih transistor yang tepat untuk berbagai aplikasi.

2.4.2. Arus *Emiter*

Dari hukum Kirchhoff diketahui bahwa jumlah arus yang masuk ke satu titik akan sama jumlahnya dengan arus yang keluar. Jika teorema tersebut diaplikasikan pada transistor, maka hukum itu menjelaskan hubungan :

$$I_E = I_C + I_B \quad \text{.....(2-1)}$$



Gambar 2-1. Arus Emitor
Sumber : *www.electroniclab.com*

Persamaan (2-1) tersebut mengatakan arus *emiter* I_E adalah jumlah dari arus kolektor I_C dengan arus base I_B. Karena arus I_D sangat kecil sekali atau disebutkan $I_B << I_C$, maka dapat dinyatakan :

$$I_E = I_C \quad \text{.....(2-2)}$$

2.4.3. *Alpha* (α)

Pada tabel data transistor (*databook*) sering dijumpai spesifikasi α_{dc} *(alpha dc)* yang tidak lain adalah :

$$\alpha_{dc} = I_C/I_E \quad \text{.....(2-3)}$$

Definisinya adalah perbandingan arus kolektor terhadap arus emitor. Karena besar arus kolektor umumnya hampir sama dengan besar arus emitor maka idealnya besar α_{dc} adalah = 1 (satu). Namun umumnya transistor yang ada memiliki α_{dc} kurang lebih antara 0,95 sampai 0,99.

2.4.4. *Beta* (β)

Beta didefenisikan sebagai besar perbandingan antara arus kolektor dengan arus *base*.

$$\beta = I_C/I_B \quad \text{.....(2-4)}$$

Dengan kata lain, β adalah parameter yang menunjukkan kemampuan penguatan arus *(current gain)* dari suatu transistor. Parameter ini ada tertera di *data book* transistor dan sangat membantu para perancang rangkaian elektronika dalam merencanakan rangkaiannya.

Misalnya jika suatu transistor diketahui besar β =250 dan diinginkan arus kolektor sebesar 10 mA, maka arus bias base yang diperlukan adalah :

$$I_B = I_C / \beta = 10mA/250 = 40\ uA$$

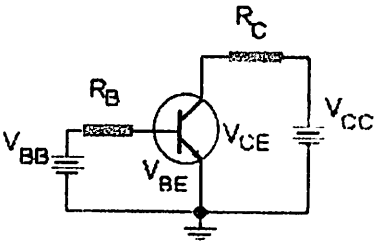
Arus yang terjadi pada kolektor transistor yang memiliki β = 200 jika diberi arus bias base sebesar 0,1 mA adalah :

$$I_C = \beta\ I_B = 200 \times 0.1mA = 20\ mA$$

Dari rumusan ini lebih terlihat definisi penguatan arus transistor, yaitu arus *base* yang kecil menjadi arus kolektor yang lebih besar.

2.4.5. *Common Emitter* (CE)

Rangkaian CE adalah rangkaian yang paling sering digunakan untuk berbagai aplikasi yang mengunakan transistor. Dinamakan rangkaian CE, sebab titik *ground* atau titik tegangan 0 volt dihubungkan pada titik *emiter*.



Gambar 2-2. Rangkaian CE
Sumber : www.electroniclab.com

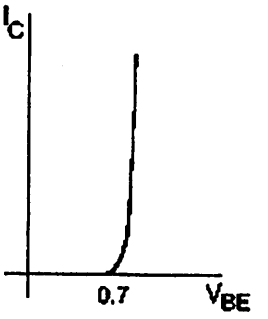
Sekilas tentang notasi, ada beberapa notasi yang sering digunakan untuk menunjukkan besar tegangan pada suatu titik maupun antar titik. Notasi dengan 1 *subscript* adalah untuk menunjukkan besar tegangan pada satu titik, misalnya V_C = tegangan kolektor, V_B = tegangan base dan V_E = tegangan emiter.

Ada juga notasi dengan 2 *subscript* yang dipakai untuk menunjukkan besar tegangan antar 2 titik, yang disebut juga dengan tegangan jepit. Diantaranya adalah :

- V_{CE} = tegangan jepit kolektor-emitor.
- V_{BE} = tegangan jepit base-emitor.
- V_{CB} = tegangan jepit kolektor-base.

Notasi seperti V_{BB}, V_{CC}, V_{EE} berturut-turut adalah besar sumber tegangan yang masuk ke titik base, kolektor dan emitor.

2.4.6 Kurva *Base*



Grafik 2-1. Kurva I_B -V_{BE}

Sumber : www.electroniclab.com

Hubungan antara I_B dan V_{BE} tentu saja akan berupa kurva dioda. Karena memang telah diketahui bahwa junction *base-emitor* tidak lain adalah sebuah dioda. Jika hukum Ohm diterapkan pada loop base maka diketahui :

$$I_B = (V_{BB} - V_{BE}) / R_B \quad \text{.....(2-5)}$$

V_{BE} adalah tegangan jepit dioda *junction base-emitor*. Arus hanya akan mengalir jika tegangan antara base-emitor lebih besar dari V_{BE}. Sehingga arus I_B mulai aktif mengalir pada saat nilai V_{BE} tertentu. Besar V_{BE} umumnya tercantum di dalam *databook*. Tetapi untuk penyerdehanaan umumnya diketahui V_{BE} = 0.7 volt untuk transistor silikon dan V_{BE} = 0.3 volt untuk transistor germanium.

Sampai disini akan sangat mudah mengetahui arus I_B dan arus I_C dari rangkaian berikut ini, jika diketahui besar $\beta = 200$. Katakanlah yang digunakan adalah transistor yang dibuat dari bahan silikon.

$$I_B = (V_{BB} - V_{BE}) / R_B$$

$$= (2V - 0.7V) / 100\ K$$

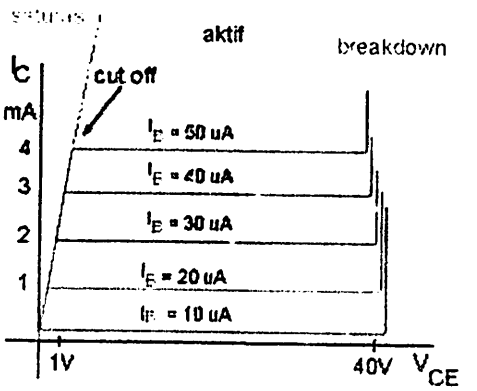
$$= 13\ uA$$

Dengan $\beta = 200$, maka arus kolektor adalah :

$$I_C = \beta I_B = 200 \times 13uA = 2.6\ mA$$

2.4.7. Kurva Kolektor

Sekarang sudah diketahui konsep arus base dan arus kolektor. Satu hal lain yang menarik adalah bagaimana hubungan antara arus base I_B, arus kolektor I_C dan tegangan kolektor-emiter V_{CE}. Pada grafik berikut telah diplot beberapa kurva kolektor arus I_C terhadap V_{CE} dimana arus I_B dibuat konstan.



Grafik 2-2. Kurva Kolektor

Sumber *: www.electroniclab.com*

Dari kurva ini terlihat ada beberapa *region* yang menunjukkan daerah kerja transistor. Pertama adalah daerah *saturasi*, lalu daerah *cut-off*, kemudian daerah aktif dan seterusnya daerah *breakdown.*

2.4.8. Daerah Aktif

Daerah kerja transistor yang normal adalah pada daerah aktif, dimana arus I_C konstan terhadap berapapun nilai V_{CE}. Dari kurva ini diperlihatkan bahwa arus I_C hanya tergantung dari besar arus I_B. Daerah kerja ini biasa juga disebut daerah linier (*linear region*).

Jika hukum Kirckhoff mengenai tegangan dan arus diterapkan pada loop kolektor (rangkaian CE), maka dapat diperoleh hubungan :

$$V_{CE} = V_{CC} - I_C R_C \quad \text{.....(2-6)}$$

Dapat dihitung disipasi daya transistor adalah :

$$P_D = V_{CE} I_C \quad \text{.....(2-7)}$$

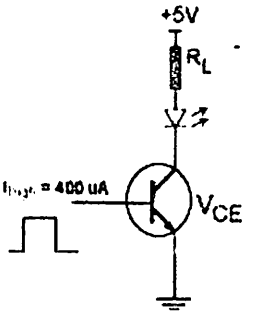
Rumus ini mengatakan jumlah disipasi daya transistor adalah tegangan kolektor-emitor dikali jumlah arus yang melewatinya. Disipasi daya ini berupa panas yang menyebabkan naiknya temperatur transistor. Umumnya untuk transistor power sangat perlu untuk mengetahui spesifikasi $P_D$max. Spesifikasi ini menunjukkan temperatur kerja maksimum yang diperbolehkan agar transistor masih bekerja normal. Sebab jika transistor bekerja melebihi kapasitas daya $P_D$max, maka transistor dapat rusak atau terbakar.

2.4.9 Daerah Saturasi

Daerah saturasi adalah mulai dari V_{CE} = 0 volt sampai kira-kira 0.7 volt (transistor silikon), yaitu akibat dari efek dioda kolektor-base yang mana tegangan V_{CE} belum mencukupi untuk dapat menyebabkan aliran elektron.

2.4.10 Daerah *Cut-Off*

Jika kemudian tegangan V_{CC} dinaikkan perlahan-lahan, sampai tegangan V_{CE} tertentu tiba-tiba arus I_C mulai konstan. Pada saat perubahan ini, daerah kerja transistor berada pada daerah *cut-off* yaitu dari keadaan saturasi (OFF) lalu menjadi aktif (ON). Perubahan ini dipakai pada system digital yang hanya mengenal angka biner 1 dan 0 yang tidak lain dapat direpresentasikan oleh status transistor ON dan OFF.



Gambar 2-3. Rangkaian Driver LED
Sumber : *www.electroniclab.com*

Misalkan pada rangkaian driver LED di atas, transistor yang digunakan adalah transistor dengan $\beta = 50$. Penyalaan LED diatur oleh sebuah gerbang logika (*logic gate)* dengan arus *output high* = 400 uA dan diketahui tegangan forward LED $V_{LED} = 2.4$ volt. Lalu pertanyaannya adalah, berapakah seharusnya resistansi R_L yang dipakai.

$$I_C = \beta I_B = 50 \times 400 \text{ uA} = 20 \text{ mA}$$

Arus sebesar ini cukup untuk menyalakan LED pada saat transistor *cut-off.* Tegangan V_{CE} pada saat *cut-off* idealnya = 0, dan aproksimasi ini sudah cukup untuk rangkaian ini.

$$R_L = (V_{CC} - V_{LED} - V_{CE}) / I_C$$

$$= (5 - 2.4 - 0)V / 20 \text{ mA}$$

$$= 2.6V / 20 \text{ mA}$$

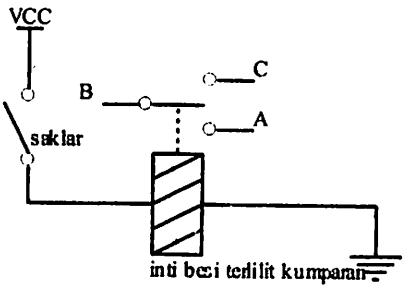
$$= 130 \text{ Ohm}$$

2.4.11. Daerah *Breakdown*

Dari kurva kolektor, terlihat jika tegangan V_{CE} lebih dari 40V, arus I_C menanjak naik dengan cepat. Transistor pada daerah ini disebut berada pada daerah breakdown. Seharusnya transistor tidak boleh bekerja pada daerah ini, karena akan dapat merusak transistor tersebut. Untuk berbagai jenis transistor nilai tegangan V_{CE}max yang diperbolehkan sebelum breakdown bervariasi. V_{CE}max pada databook transistor selalu dicantumkan juga.

2.5. Relay

Relay adalah komponen elektronika yang terdiri dari sebuah lilitan kawat (kumparan/koil) yang terlilit pada sebuah besi lunak. Jika kumparan dialiri arus listrik maka inti besi akan menjadi magnet dan menarik pegas sehingga kontak AB terhubung dan BC terputus.



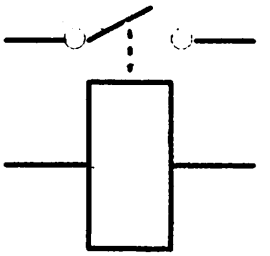
Gambar 2-4. Cara kerja relay
Sumber: Relay,www.national.com. 2001

Relay merupakan suatu alat untuk menghubungkan kontak antar komponen, dan dalam memutus atau menghubungkan kontak digerakkan oleh

fluksi yang ditimbulkan dari adanya medan magnet yang dihasilkan oleh kumparan yang melilit pada besi lunak yang terdapat di relay.

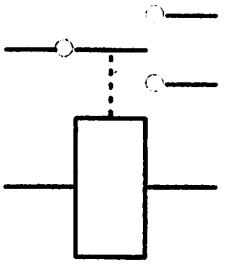
Ada beberapa macam relay, antara lain :

- SPST (*Single Pin Single Terminal*)



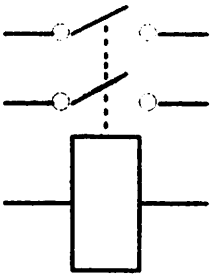
Gambar 2-5. Relay SPST
Sumber: Relay,www.national.com. 2001

- SPDT (*Single Pin Dual Terminal*)



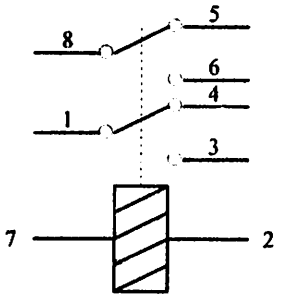
Gambar 2-6. Relay SPDT
Sumber: Relay,www.national.com. 2001

- DPST (*Dual Pin Single Terminal*)



Gambar 2-7. Relay DPST
Sumber: Relay,www.national.com. 2001

- DPDT (*Dual Pin Dual Terminal*)



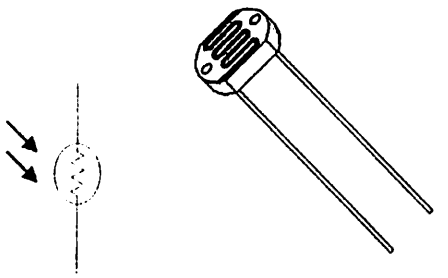
Gambar 2-8. Relay DPDT
Sumber: Relay,www.national.com. 2001

2.6. *Light Dependent Resistor* (LDR)

LDR adalah suatu komponen elektronika yang bersifat resistif, dimana nilai resistansi dipengaruhi oleh intensitas cahaya yang diterimanya. Bila LDR dibawa dari ruangan dengan intensitas cahaya tertentu ke ruangan dengan intensitas cahaya yang lemah, maka nilai resistansinya akan berubah secara perlahan-lahan dalam selang waktu tertentu.

Laju perubahan merupakan ukuran yang tepat untuk menunjukkan perubahan resistansi dalam selang waktu tertentu. Besar laju perubahan yang

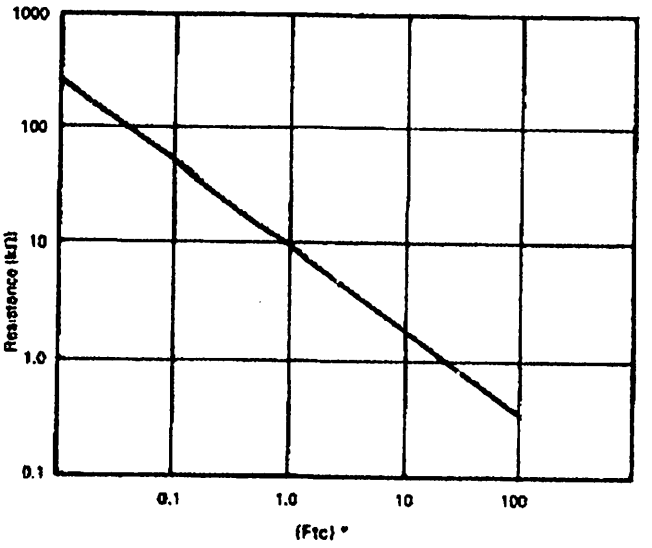
diberikan dinyatakan dalam satuan KΩ/detik. Untuk LDR tipe arus nilainya lebih dari 200 KΩ/detik, diukur selama 20 menit pertama mulai dari level cahaya 1000 lux.



Gambar 2-9. Simbol dan Kontruksi LDR
Sumber: RS Component, March 1997

Kecepatan dan perubahan resistansi ini akan lebih besar nilainya pada arah sebaliknya yaitu dari tempat yang gelap ke tempat yang terang dengan intensitas cahaya sekitar 300 lux akan memerlukan waktu 10 milidetik untuk mencapai nilai resistansi yang setara dengan level kuat cahaya 400 lux.

Sensitivitas LDR tidak sama untuk setiap panjang gelombang cahaya yang jatuh padanya. Kurva pada pada gambar 2-4 menunjukkan hubungan antara sensitivitas LDR dengan panjang gelombang cahaya yang disebut karakteristik respon spektrum LDR.



Gambar 2-10. Kurva Karakteristik LDR
Sumber: : RS Component

Dalam aplikasi rangkaian elektronika, LDR banyak dipakai sebagai alat pengindera cahaya. Penggunaannya antara lain sebagai saklar cahaya, mengukur intensitas cahaya, dan lain-lain.

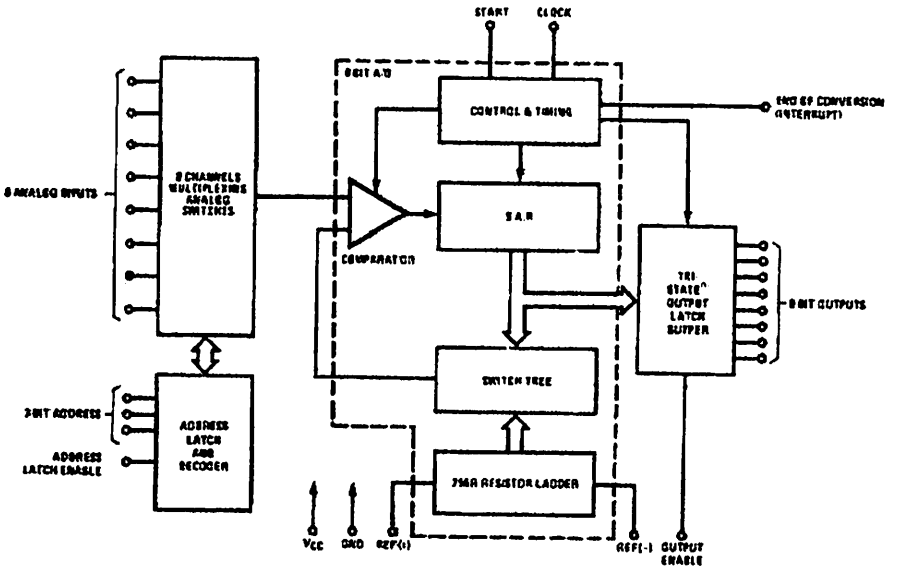
2.7. ADC 0808

Agar dapat mengukur atau mengolah suatu varibel fisik yang umumnya dalam bentuk besaran analog dengan piranti digital, varibel tersebut harus terlebih dahulu diubah menjadi varibel digital yang nilainya proporsional dengan nilai variabel yang akan diukur atau diolah tersebut. Proses konversi ini dilakukan oleh konverter analog ke digital (anolog to digital converter).

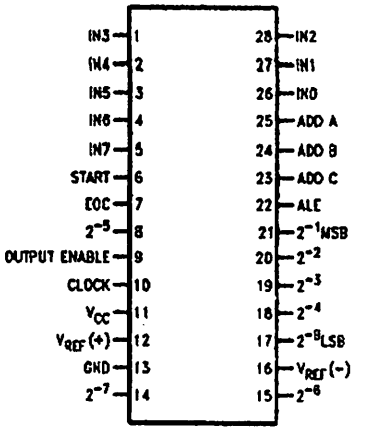
Spesifikasi penting lain selain ketelitian (akurasi) dan linieritas adalah waktu konversi (convertion time). Waktu konversi ADC adalah waktu yang diperlukan ADC untuk menghasilkan kode biner yang valid untuk tegangan

masukan yang diberikan. Semakin pendek waktu konversi berarti kecepatan konversi semakin tinggi.

Dalam pembuatan alat ini digunakan ADC jenis 0808 yang mempunyai 8 bit channel multiplekser dan menggunakan metode pendekatan Successive Approximation Register (SAR). Waktu konversi ADC ini adalah 100μs dengan rentangan input sebesar 0 - 5 volt dan supply tegangan sebesar 5 volt.



Gambar 2-11. Blok Diagram ADC 0808
Sumber: *www.national.com*



Gambar 2-12. Konfigurasi Pin ADC 0808
Sumber : www.national.com

2.8. Mikrokontroller AT89S8252

2.8.1. Pendahuluan

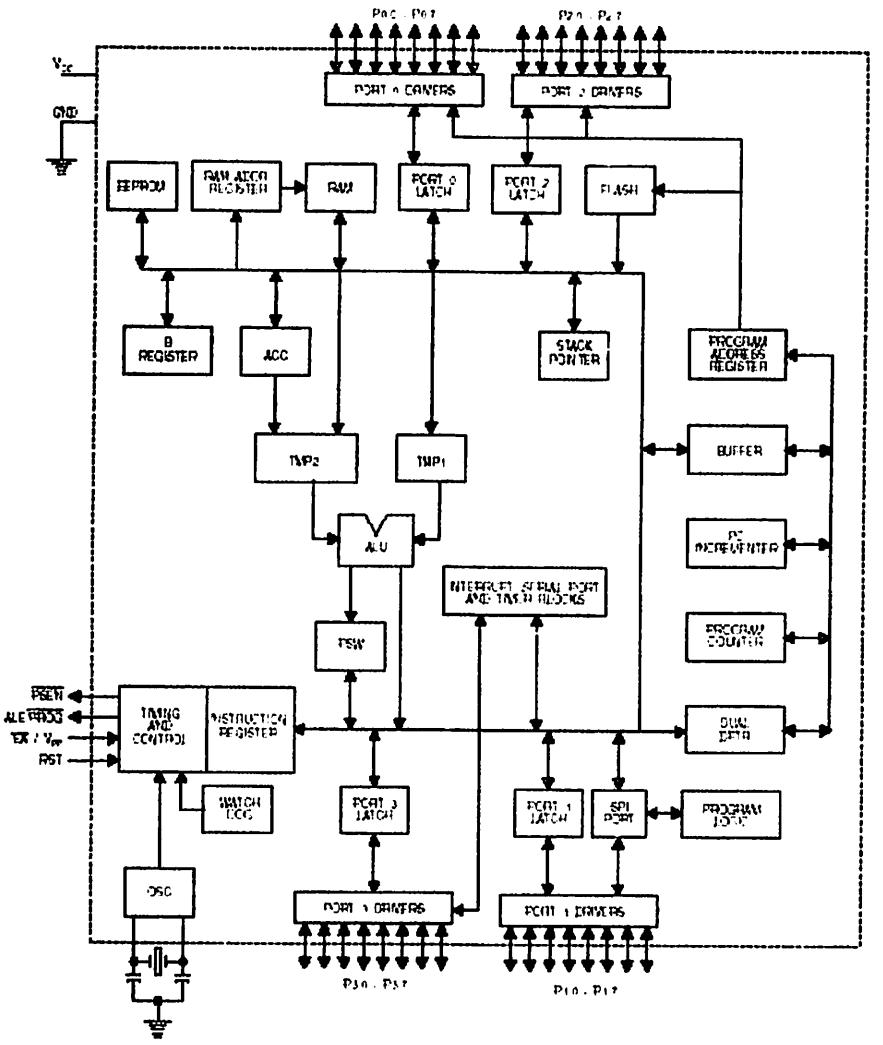
Perbedaan mendasar antara mikrokontroller dan mikroprosesor adalah jika mikrokontroiler selain memiliki CPU *(Central Processing Unit)* juga dilengkapi dengan memori dan I/O *(Input/Output).* Maka mikrokontroller dapat dikatakan sebagai *microcomputer* dalam keping tunggal *(single chip microcomputer) yang* dapat berdiri sendiri.

Mikrokontroller AT89S8252 adalah mikrokontroller keluarga MCS-51 yang membutuhkan daya rendah, memiliki kemampuan yang tinggi, dan merupakan mikrokomputer 8 bit yang dilengkapi 8 K*byte Flash* PEROM *(Programmable and Erasable Read Only Memory)* yaitu ROM yang dapat ditulis ulang atau dihapus menggunakan sebuah perangkat *programmer.* Serta terdapat EEPROM *internal* sebesar 2 K*byte.*

Flash PEROM dalam AT89S8252 menggunakan *Atmel's High-Density*

Non Volatile Technology yang mempunyai kemampuan untuk ditulis ulang hingga 1000 kali dan berisikan perintah *standard* MCS-51. Selain itu juga dilengkapi RAM *internal* sebesar 256 b*yte*. Dalam sistem Mikrokontroller terdapat dua hal yang mendasar, yaitu perangkat keras dan perangkat lunak yang keduanya saling terkait dan mendukung.

2.8.2. Perangkat Keras Mikrokontroller AT89S8252



Gambar 2-13. Blok Diagram Mikrokontroller AT89S8252
***Sumber** : Belajar Mikrokontroller ATMEL AT89S8252*

Mikrokontroller AT89S8252 secara umum memiliki:

- CPU 8 bit
- 8 Kbyte FLASH PEROM
- 2 Kbyte EEPROM
- *Memory* 256 x 8 bit *Internal* RAM
- 32 Port I/O *Lines*
- 3 *Timer* dan *Counter* 16 bit
- 9 Sumber Interupsi
- SPI serial interface
- Oscillator dan clock maksimal 24 MHz
- *Programmable Watchdog Timer*
- *Programmable UART Serial Chanel*
- *Dual Data Pointer*
- *Power-Off Flag*

2.8.3. Arsitektur AT89S8252

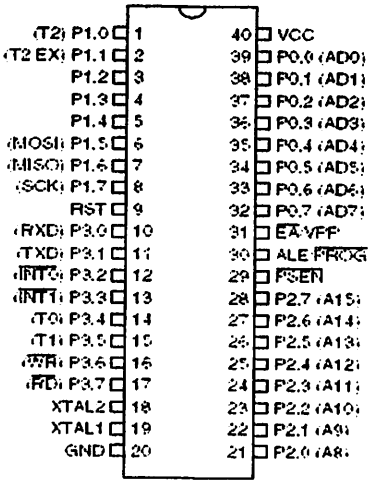
Arsitektur Mikrokontroller AT89S8252 adalah sebagai berikut :

1. CPU *(Central Processing Unit)* 8 bit dengan *register A (Accumulator)* & B.
2. 16-bit *Program Counter* (PC) dan *(Data Pointer)* DTPR.
3. 8-bit *Program Status Word (PSW).*
4. 8-bit *Stack Pointer (SP).*
5. 8 *Kbyte* Flash PEROM *internal.*

6. 256 *byte internal* RAM.
   - 4 bank *register,* masing-masing berisi *8 register.*
   - 16 *byte* yang dapat dialamati pada *bit-level.*
   - 208 byte *general purpose memory data.*
7. 32 pin *input-output* tersusun atas P0-P3, masing-masing 8-bit.
8. 3 buah *timer (T0 & T1)* dengan masing-masing 16-bit *timer/counter.*
9. *Receiver/transmiter data* secara *serial full duplex: Serial buffer* (SBUF).
10. *Control register :* TCON, TMOD, SCON, PCON, IP & IE.
11. 9 buah *sumber* interupsi (4 buah sumber interupsi *external* dan *5* buah sumber interupsi *internal*).
12. *Oscillator* dan *clock internal.*

2.8.4. Konfigurasi Pin Mikrokontroller AT89S8252

Konfigurasi kaki-kaki mikrokontroller terdiri dari 40 pin, seperti terlihat pada gambar 2.2 berikut ini :



Gambar 2-14. Konfigurasi Pin-Pin AT89S8252
***Sumber** : Belajar Mikrokontroller ATMEL AT89S8252*

Fungsi dari tiap-tiap pin adalah sebagai berikut :

- **Pin 40 : Vcc** (sumber tegangan).
- **Pin 20 : GND** *(Ground).*
- **Pin 32-39: Port 0:**

  Merupakan port *input-output* dua arah multipleks dan dua *bus* alamat rendah (A0-A7) serta data selama pengaksesan program dan data memori *external.*
- **Pin 1-8: Port 1:**

  Merupakan port *input-output* dua arah dengan *internal pull-up.*
- **Pin 21-28: Port 2:**

  Merupakan port *input-output* dengan *internal pull-up.* Mengeluarkan *address* tinggi selama pengambilan *(fetching) program memory external.* Selama pengaksesan ke *external data memory,* port 2 mengeluarkan isi P2 SFR *(Special Function Register).* Menerima *address* dan beberapa sinyal kontrol selama pemprograman dan verifikasi.
- **Pin 10-17: Port 3:**

  Merupakan port *input-output* dengan *internal pull-up.* Port 3 juga memiliki fungsi khusus, yaitu :

  - RXD (P3.0) : Port *serial input.*
  - TXD (P3.1) : Port *serial output.*
  - INT0 (P3.2) : *external interrupt 0.*
  - INT1 (P3.3) : *external interrupt 1.*
  - T0 (P3.4) : *Input external timer 0.*
  - T1 (P3.5) : *Input external timer 1.*

- WR (P3.6) : *Strobe* tulis data memori *external.*
- RD (P3.7) : *Strobe* baca data memori *external.*

➢ **Pin 9: RST *(Reset)*:**

Input reset berfungsi *me-reset* CPU saat sumber tegangan dihidupkan.

➢ **Pin 30: ALE/PROG *(Address Latch Enable)/Programming*:**

Pulsa *output* ALE digunakan untuk proses *'latching' byte address* rendah (A0-A7) selama pengaksesan ke memori *external.* Pin ini juga digunakan untuk memasukkan pulsa program selama pemprograman.

➢ **Pin 29: PSEN *(Program Store Enable)*:**

Merupakan *strobe* baca ke program memori *external.*

➢ **Pin 31: *EA/VPP (External Address)*:**

EA *low* jika mengakses memori *external.* Untuk mengakses memori *internal* maka EA dihubungkan ke-Vcc (+5V).

➢ **Pin 18-19: *XTAL1* dan *XTAL2:***

Kaki ini dihubungkan dengan kristal bila menggunakan *Oscillator internal.* XTAL1 merupakan *input inverting Oscillator amplifier* sedangkan XTAL2 merupakan *output inverting oscillator amplifier.*

2.8.5. Organisasi Memori

Dalam mikrokontroller AT89S8252 ruang alamat telah dibedakan untuk program memori dan data memori.

2.8.5.1. *Internal Program Memory*

Mikrokontroller AT89S8252 memiliki program memori *internal* sebesar

8 Kbyte dengan ruang alamat 0000H-0FA0H. Jika alamat-alamat program lebih tinggi dari pada 0FA0H dimana melebihi kapasitas ROM *internal*, menyebabkan AT89S8252 secara otomatis mengambil kode byte dari program memori *external*. Kode *byte* juga dapat diambil hanya dari memori *external* dengan alamat 0000H-FFFFH dengan cara menghubungkan pin EA ke *ground*.

2.8.5.2. *Random Access Memory* (RAM)

Ruangan alamat memory data *internal* (RAM) dengan kapasitas 256 *byte* yaitu : 00H-FFH yang terbagi atas 3 daerah, yaitu :

1. Empat *bank register*

   Setiap *bank* terdiri dari *8 register* (R0-R7) sehingga jumlah *register* untuk ke-empat *bank register* menjadi 32 buah *register* yang menempati ruang alamat 00H-1FH. Mengaktifkan salah satu *bank register* dapat dilakukan dengan mengatur RS0-RS1 pada *Program Status Word (PSW)*.

2. Bit Addressable

   Terdiri dari *16 byte* yang berada pada alamat 20H-2FH. Masing-masing bit dalam 208 bit yang lokasinya dapat dialamati secara langsung.

3. RAM Keperluan Umum

   Terdiri atas 208 *byte* yang menempati alamat 30H-FFH, dan dapat dialamati secara langsung maupun tak langsung dalam penggunaan untuk keperluan umum *(general purpose)*.

Table 2-2
Pengaturan RS0-RS1 *Bank Register*

RS1	RS0	Register Bank Select Bits
0	0	Bank 0
0	1	Bank 1
1	0	Bank 2
1	1	Bank 3

Sumber : Belajar Mikrokontroller ATMEL AT89S8252

2.8.5.3. SFR *(Special Function Register)*

Untuk operasi AT89S8252 yang menggunakan alamat internal RAM (00H-FFH). Beberapa dari *register-register* ini juga mampu dengan pengalamatan bit sehingga dapat dioperasikan seperti *yang* ada pada RAM.

2.8.5.3.1. PSW *(Program Status Word)*

Cara mendefenisikannya *register* ini ditunjukkan dalam tabel 2.2 :

Tabel 2-3
Pengaturan RS0-RS1 *Bank Register*

Data	Simbol	Posisi	Fungsi /Art-1
D0	P	PSW.0	*Parity flag*
D1	-	PSW.1	*Flag* didefinisikan oleh pemakai.
D2	OV	PSW.2	*Overflow Flag*
D3	RS0	PSW.3	Bit pemilih *bank register.*
D4	RS1	PSW.4	Bit pemilih *bank register.*
D5	F0	PSW.5	*Flag 0*
D6	AC	PSW.6	*Auxiliary CarryFlag*
D7	CY	PSW.7	*Carry Flag*

Sumber : Belajar Mikrokontroller ATMEL AT89S8252

2.8.5.3.2. PCON *(Power Control)*

Untuk *register* cara mendefenisikannya ditunjukkan dalam tabel 2.3 :

Tabel 2-4
Skema Mendefinisikan PCON

Data	Simbol	Fungsi /Arti
D0	IDL	*Idle* mode bit
D1	PD	*Power Down* bit
D2	GF0	*Bit flag* serbaguna.
D3	GF1	Bit *flag* serbaguna.
D4	-	Tidak dipakai.
D5	-	Tidak dipakai.
D6	-	Tidak dipakai.
D7	SMOD	Digunakan untuk menghasilkan *baudrate* dan SMOD_1, maka *baudrate* akan *double* baik mode 0,1,2 atau 3.

Sumber : Belajar Mikrokontroller ATMEL AT89S8252

2.8.5.3.3. Sistem Interupsi

Mikrokontroller AT89S8252 mempunyai 9 buah sumber interupsi yang dapat mengakibatkan permintaan interupsi, yaitu INT0, INT1, T0, T1 port serial dan beberapa port lainnya. Saat terjadi interupsi mikrokontroller secara otomatis akan menuju ke *subrutin* pada alamat tersebut. Setelah interupsi *service* selesai dikerjakan, Mikrokontroller akan mengerjakan program semula. Sumber interupsi *external* adalah INT0, INT1, dimana kedua interupsi *external* ini akan aktif pada transisi rendah selain itu juga ada *Timer/Counter 0, Timer/Counter 0* dan interupsi dari port serial *(receiver)*. Interupsi serial dibangkitkan dengan melakukan operasi OR pada R1 dan T1. Tiap-tiap sumber interupsi dapat *di-enable* atau *di-disable* secara *software*. Tingkat prioritas semua sumber interupsi dapat diprogram sendiri-sendiri dengan *set* atau *clear* bit pada SFRS IP *(Interrupt Priority)*.

Tabel 2-5
Alamat Sumber Interupsi

Sumber Interupsi	Alamat Awal
Power On Reset	0000h
Interrupt luar 0 (INT 0)	0003h
Pewaktu/ pencacah 0 (T0)	000Bh
Interrupt luar 1 (INT 1)	0013h
Pewaktu/ pencacah 1 (T1)	001Bh
Port 110 *Serial*	0023h

***Sumber** : Belajar Mikrokontroller ATMEL AT89S8252*

Register yang berperan dalam mengatur aktif tidaknya interupsi adalah *interrupt enable register,* susunan dari bit-bit beserta kegunaannya adalah :

Tabel 2-6
Kegunaan *Interrupt Enable Register*

Data	Simbol	Posisi	Fungsi /Arti
D0	EX0	IE.0	Diatur secara *software* untuk interupsi dari INT1.
D1	ET0	IE.1	Diatur secara *software* untuk interupsi dari *timer/counter* 1.
D2	EX 1	IE.2	Diatur secara *software* untuk interupsi dari INT 1.
D3	ET1	IE.3	Diatur secara *software* untuk interupsi dari *timer/counter*1.
D4	ES	IE.4	Untuk mengatur *enable* atau *disables* atau interupsi R1/T1.
D5	-	IE.5	Kosong
D6	-	IE.6	Kosong
D7	EA	IE.7	Jika diatur 0 maka semua interupsi *di-disable,* jika diatur 1 maka interupsi diatur *di-disable* atau *di-enable* menurut masing-masing bit.

***Sumber** : Belajar Mikrokontroller ATMEL AT89S8252*

2.8.5.3.4. *Timer/Counter*

Pengendalian kerja dari *timer/counter* dilakukan dengan pengaturan register yang berhubungan dengan kerja dari *timer/counter* yaitu melalui sebuah *timer/counter mode control.* Untuk mengaktifkan *timer/counter* yang meliputi penentuan fungsi sebagai *timer* atau sebagai *counter* serta pemilihan *mode* operasi dapat diatur melalui TMOD. Konfigurasi dari *register* TMOD seperti yang ditunjukkan dalam tabel 2.6 berikut ini :

Tabel 2-7
Register TMOD

Data	Simbol	Posisi	Fungsi /Arti
D0	IT0	TCON.0	*Interrupt 0 type control bit.*
DI	IE0	TCON.1	*External interrupt 0 edge flag.*
D2	IT1	TCON.2	*Interrupt type 1 control bit.* Diatur oleh *software* untuk menentukan aktif *low* atau *high trigger* dari *external.*
D3	IE1	TCON.3	*External interrupt 1 edge flag.* Diatur oleh *hardware* ketika *external interrupt* terdeteksi dan nol-kan melalui *software* ketika *interrupt* diproses.
D4	TR0	TCON.4	*Timer 0 control bit.* Diatur oleh *software* ketika *timer counter 0.*
D5	TF0	TCON.5	*Timer 0 overflow flag control bit.* Diatur oleh *software* ketika *timer/counter 0 overlow.*
D6	TR1	TCON.6	*Timer 1 control bit.* Diatur oleh *software* ketika *timer counter 0.*
D7	TF1	TCON.7	*Timer 1 overflow flag control bit.* Diatur oleh *software* ketika *timer/counter 0 overflow.*

***Sumber** : Belajar Mikrokontroller ATMEL AT89S8252*

Tabel 2-8
Timer/Counter Mode Control Register

Data	Simbol	Fungsi/Arti
D0	*Timer* 0; M0 (0)	Untuk memilih mode *timer.*
D1	*Timer* 0; M1 (0)	Untuk memilih mode *timer.*
D2	*Timer* 0; C/T (0)	1 = *Counter* & *0* = *Timer*
D3	*Timer* 0; GATE (0)	*Timer* akan berjalan jika bit di *set* dan INT0 (untuk *Timer 0)* atau INT1 (untuk *Timer 1).*
D4	*Timer* 1; M0 (1)	Untuk memilih mode *timer.*
D5	*Timer* 1; MI (1)	Untuk memilih mode *timer.*
D6	*Timer* 1; C/T (0)	1 = *Counter* & *0* = *Timer*
D7	*Timer* 1; GATE (1)	*Timer* akan berjalan jika bit di set dan INT0 (untuk *Timer 0)* atau INT1 (untuk *Timer 1).*

Sumber : Belajar Mikrokontroller ATMEL AT89S8252

Tabel 2-9
Mode Operasi *Timer/Counter*

M1	M0	Operating Mode
0	0	*Timer* 13 bit
0	1	*Timer/Counter* 16 bit
1	0	8 bit *Auto reload Timer/Counter*
1	1	TL0 dari *Timer* adalah 8 Bit *Timer/Counter* dikendalikan oleh kontrol bit *Timer* 0. TH0 adalah 8 bit yang dikendalikan oleh *Timer* 1 *control* bit.

Sumber : Belajar Mikrokontroller ATMEL AT89S8252

2.8.5.3.5. Metode Pengalamatan

1. Pengalamatan bit *(Direct Bit Addressing)* :

   Pengalamatan langsung tiap bit ini hanya dilakukan pada lokasi RAM *internal* yaitu 20H-2FH, dan sebagian SFR yaitu port 0, port 1, port 2, port 3, TCON *register,* SCON *register, IE register, PSW register, ACC* dan *B register.*

2. Pengalamatan tak langsung *(Indirect Bit Addressing)* :

   Pada *pengalamatan* tak langsung, instruksi menunjukkan suatu *register* yang isinya adalah alamat dari *operand, eksternal* dan *internal* RAM dapat dialamati secara tidak langsung. *Register* alamat untuk data dengan lebar 8 bit dapat berupa R0 dan R1 yang digunakan untuk memilih angka *register* atau *stack pointer. Register* alamat untuk data, dengan lebar 16 bit digunakan *Data Pointer* (DPTR).

3. Pengalamatan ber-indeks :

   Yang dapat diakses dengan pengalamatan berindeks hanya *memory program.* Mode ini dimaksudkan untuk membaca *look-up table program.*

4. Konstanta *immediet* :

   Pengalamatan langsung dilakukan dengan memberikan nilai ke *register* secara langsung, dilakukan dengan menggunakan tanda #, (Contoh : Mov A, #100).

2.9. LCD *(Liquid Crystal Display)* M1632

LCD *(Liquid Crystal Display)* adalah suatu jenis piranti *output* yang menggunakan daya rendah dengan pengontrol kontras dan kecerahan. Pengontrol utamanya dan karakter ada pada ROM *(Read Only Memory) generator* dan *display* data RAM *(Random Access Memory)* yang akan menghasilkan *extended key codes* (kode tombol/*keyboard* standart *international* dalam Hexsa) jika padanya diberikan inputan. Untuk dapat memfungsikan dengan baik maka perlu diperhatikan proses inisialisasi yang telah ditentukan oleh pabrik pembuatnya. *Timing* penginisialisasian sangat perlu dipertimbangkan, karena jika meleset

sampai orde *mili secon*, maka dapat dipastikan LCD itu tidak dapat berfungsi.

Ada dua jenis *register* yang terdapat dalam LCD M1632 ini, yaitu *data register* dan *instruction register*. Dengan menggunakan pin RS *(Register Select)* pada LCD, pemakaian kedua *register* dapat dipilih. Pemilihan *register* pada LCD ditunjukkan dalam tabel 2.9 berikut ini :

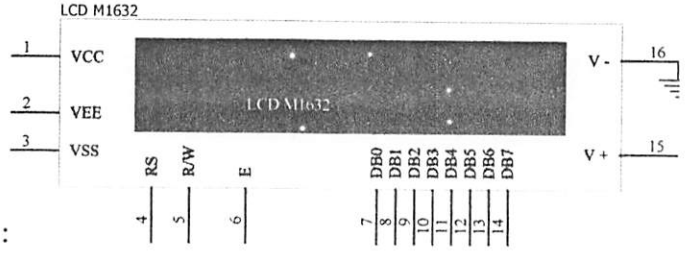
Tabel 2-10
Pemilihan *Register* Pada LCD M1632

Nama Sinyal	No. Terminal	I/O	Tujuan	Keterangan Sinyal
RS	4	Input	MPU	0 : Instruction Register 1 : Data Register

***Sumber** : Seiko Instrument Inc, 1987*

Jika bagian yang dipilih adalah *instruction register* maka output yang dihasilkan adalah meliputi operasional dari LCD, misalnya fungsi *display clear, cursor home, entry mode set, display on/off, cursor shift* dan sejenisnva. Sebaliknya, jika bagian yang dipilih adalah *data register, output* yang dihasilkan adalah meliputi karakter yang tabelnya terdapat pada lampiran.

Berikut adalah gambar dari LCD dengan pin-pin yang akan terhubumg dengan mikrokontroller AT89S8252 :



Gambar 2-15. Pin-pin LCD M1632

***Sumber** : Seiko Instrument Inc, 1987*

LCD M1632 mempunyai spesifikasi sebagai berikut :

- 16 karakter 2 bans dalam bentuk *dot matrik 5 x 7* dan kursor.
- *Duty ratio* 1/16.
- Memiliki ROM pembangkit karakter untuk 192 jenis karakter.
- RAM untuk data *display* sebanyak 80 x 8 bit (80 karakter maksimum).
- Dapat dirangkai dengan MPU *(Microprocesor Unit) 8* bit atau 4 bit.
- RAM data *display* dan RAM pembangkit karakter dibaca oleh *MPU.*
- Memiliki fungsi instruksi : *display ON/OFF, cursor ON/OFF, display character blink, cursor shift* dan *display shift.*
- Memiliki rangkaian *oscillator* sendiri.
- Sumber tegangan tunggal *+5* Volt.
- Memiliki rangkaian *reset* otomatis pada saat catu daya dihidupkan.
- Temperatur operasi 0° – *50°*.

LCD M1632 mempunyai 16 pin dengan fungsi masing-masing pin sebagai berikut:

Tabel 2-11
Fungsi pin-pin LCD M1632

No. PIN	Nama PIN	Fungsi
1	Vss	Terminal Ground
2	Vcc	Tegangan Catu + 5 volt
3	Vee	Mengendalikan kecerahan LCD
4	RS	Sinyal pemilihan register 0 = Tulis 1 = Baca
5	R/W	Sinyal seleksi tulis atau baca 0 = Tulis 1 = Baca
6	E	Sinyal operasi awal yang mengaktifkan data tulis atau baca
7 - 14	DB0 – DB7	Merupakan saluran data berisi perintah data yang akan ditampilkan
15	V + BL	Back Light Supply 5 Volt (Volt)
16	V - BL	Back Ligth Supply 0 (Ground)

Sumber : Seiko Instrument Inc, 1987

Pada LCD juga terdapat instruksi – instruksi sebagai berikut :

1. Display clear : membersihkan tampilan yang ada pada LCD serta menyimpan, sedangkan kursor kembali ke posisi semula.

2. Cursor home : hanya membersihkan tampilan dan kursor kembali ke semula.
3. Empty mode Set : layar beraksi sebagai tampilan tulis.

   S : 1/0 = menggeser layar.

   1/0 : 1 = kursor bergerak ke kanan dan layar bergerak ke kiri.

   1/0 : 0 = kursor bergerak ke kiri dan layar bergerak ke kanan
4. Display On/Off kontrol.

   D : 1 = layar on

   D : 0 = layar off

   C : 1 = kursor on

   C : 0 = kursor off

   B : 1 = kursor berkedip-kedip

   B : 0 kursor tidak berkedip – kedip
5. Cursor Display Shift

   S/C : 1 = LCD diidentifikasikan sebagai layar

   S/C : 0 = LCD diidentifikasikan sebagai kursor

   R/L : 1 = menggeser satu spasi ke kanan

   R/L : 0 = menggeser satu spasi ke kiri
6. Fuction Set

   DL : 1 = panjang data LCD pada 8 bit

   DL : 0 = panjang data LCD pada 4 bit

   Bit upper ditransfer terlebih dahulu kemudian diikuti dengan 4 bit lower.

N : 1/0 = LCD menggunakan 2 atau 1 baris karakter

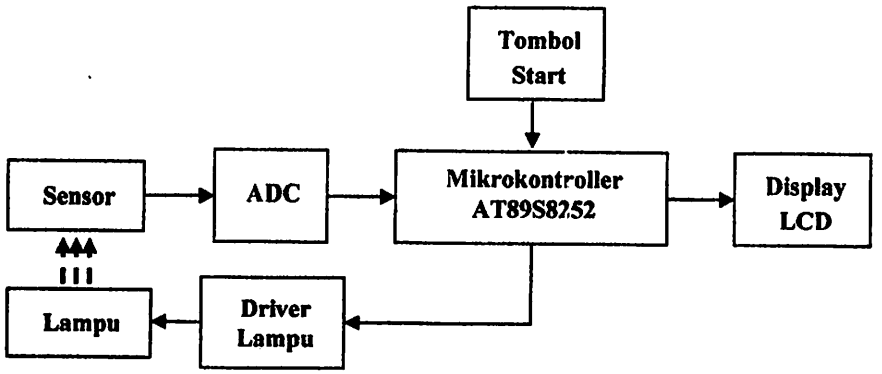
P : 1/0 = LCD menggunakan 5 x 10 dot matrik

7. CG RAM address set : menulis alamat RAM ke karakter
8. DD RAM address set : menulis alamat RAM ke tampilan
9. BF/address set : BF = 1/0, LCD dalam keadaan sibuk atau tidak sibuk.
10. Data write to CG RAM or DD RAM : membaca byte dari alamat terakhir RAM yang dipilih.

BAB III

PERENCANAAN DAN PEMBUATAN ALAT

Dalam bab ini akan dibahas mengenai perancangan dan pembuatan alat yang meliputi perangkat keras (hardware) dan perangkat lunak (software). Pembahasan dalam bab ini akan dilakukan perblok dari diagram keseluruhan seperti ditunjukkan pada gambar 3-1 di bawah ini :



Gambar 3-1. Diagram Blok Keseluruhan Sistem

Fungsi dari masing-masing blok :

1. Sensor

   Sensor yang digunakan pada sistem ini adalah sensor LDR (*Light Dependent Resistors)* yang berfungsi untuk mendeteksi perubahan intensitas cahaya yang diterima.

2. ADC

   Berfungsi untuk merubah sinyal analog dari sensor menjadi sinyal digital. ADC yang digunakan adalah 0808.

3. Mikrokontroler AT89S8252

   Untuk memproses sinyal atau data yang masuk dan mengeksekusi instruksi yang akan dijalankan oleh sistem.

4. Tombol Start

   Untuk memulai proses pengukuran.

6. Display

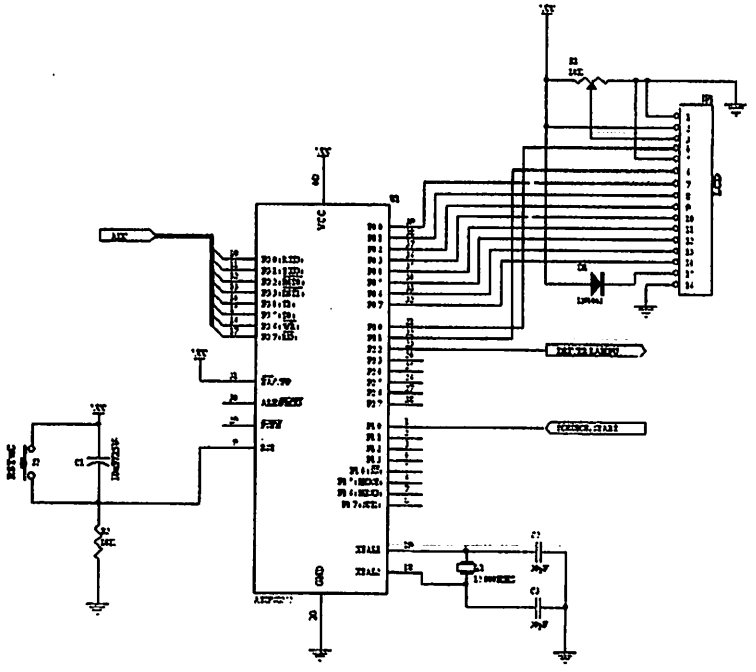
   Untuk display yang digunakan adalah LCD sebagai keluaran dalam bentuk tulisan.

3.1. Perancangan Perangkat Keras (Hardware)

3.1.1. Rangkaian Mikrokontroller AT89S8252

Rangkaian mikrokontroller AT89S8252 berfungsi sebagai pengolah data yang dihasilkan oleh ADC 0808 yang berfungsi sebagai inputan dan menampilkan data tersebut ke dalam LCD yang berfungsi sebagai outputan. Mikrokontroller juga akan menampilkan data identitas penulis ke dalam LCD pada awal penyalaan sistem.

Pengaturan jalur *input* dan *output* pada rangkaian mikrokontroller untuk sebuah rancangan terprogram, sangat berkaitan erat dengan program yang kita buat. Agar tidak terjadi kesalahan saat pembacaan data, mikrokontroller menyediakan jalur-jalur 32 *input-output* yang dapat digunakan secara berkelompok atau bersamaan untuk tiap kelompok terisi 8 bit. Untuk lebih jelasnya, hubungan mikrokontroller dengan perangkat pendukungnya dapat dilihat dalam gambar 3-2 di bawah ini.

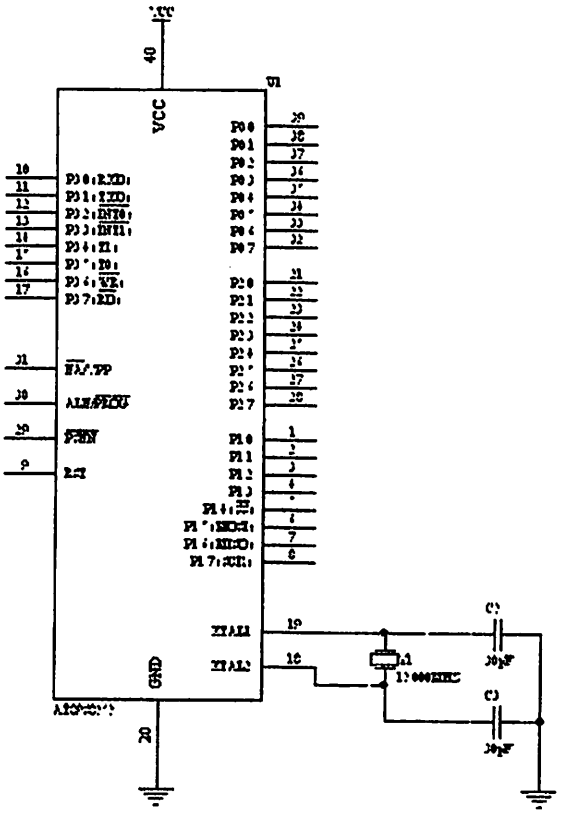


Gambar 3-2. Perancangan Mikrokontroller AT89S8252

3.1.1.1. Rangkaian Clock

Kecepatan proses yang dilakukan oleh mikrokontroller ditentukan oleh sumber *clock* (pewaktuan) yang mengendalikan mikrokontroller tersebut. Sistem yang akan dirancang ini akan menggunakan asilator internal yang sudah tersedia dalam chip mikrokontroller AT89S8252. Untuk menentukan frekuensi osilatornya cukup dengan cara menghubungkan kristal pada pin 19 (XTAL 1) dan pin 18 (XTAL 2) serta dua buah kapasitor ke pentanahan (ground).

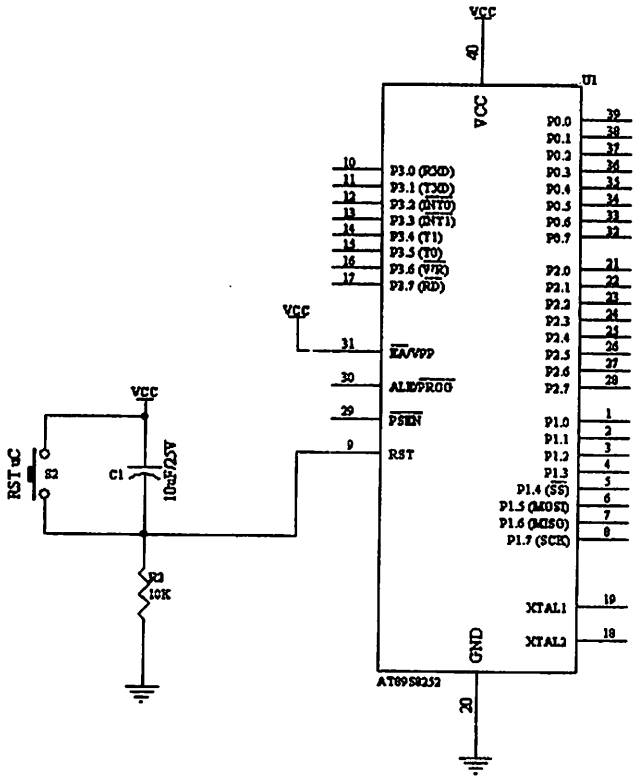
Besar kapasitansi, disesuaikan dengan spesifikasi pada lembar data AT89S8252 yaitu 30 pF. Kristal yang digunakan adalah 12 MHz. gambar 3-3 memperlihatkan rangkaian *clock* yang digunakan.



Gambar 3-3. Perancangan Rangkaian Clock

3.1.1.2. Rangkaian Reset

Untuk m*ereset* mikrokontroler AT89S8252, maka pin RST diberi logika tinggi selama sekurangnya dua siklus mesin (24 periode osilator). Untuk membangkitkan sinyal *reset* kapasitor dihubungkan dengan Vcc dan sebuah resistor yang dihubungkan ke *ground*. Rangkaian *reset* ditunjukkan dalam gambar 3-4 sebagai berikut :



Gambar 3-4. Perancangan Rangkaian Reset

Karena kristal yang digunakan mempunyai frekuensi sebesar 12 MHz, maka satu periode membutuhkan waktu sebesar :

$$T = \frac{1}{f_{XTAL}} = \frac{1}{12\,MHz}\,S = 8{,}333\times10^{-8}\,s$$

Sehingga waktu minimal logika tinggi yang dibutuhkan untuk *mereset* mikrokontroler adalah :

Reset (min) = T × periode yang dibutuhkan

$= 8{,}333 \times 10^{-8} \times 24 = 1{,}999\ \mu s$

Jadi mikrokontroller membutuhkan waktu minimal 1,999 μs untuk *mereset*. Waktu minimal inilah yang dijadikan pedoman untuk menentukan nilai R dan C. Dari

persamaan konstanta waktu T = R × C (Malvino, 1984 : 152) dan jika nilai R ditentukan sebesar 10 kΩ (Manual Data Sheet Book AT89S8252 : 9) maka nilai C adalah

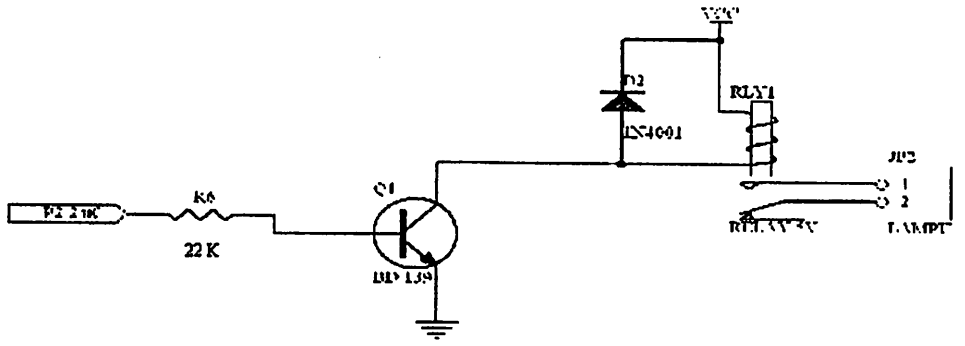
$$C = \frac{T}{R}$$

$$= \frac{1{,}999 \times 10^{-6}}{10 \times 10^{3}}$$

$$= 199{,}9 \times 10^{-12}\,\text{F}$$

Kapasitor minimal yang dibutuhkan adalah 199,9 pF. Dengan menggunakan kapasitor sebesar 10 μF, maka akan menjamin waktu reset di atas nilai minimal waktu yang dibutuhkan untuk mereset mikrokontroller.

3.1.2. Rangkaian Driver Lampu



Gambar 3-5. Perancangan Rangkaian Driver Lampu

Relay di sini digunakan sebagai saklar untuk ON/OFF saja.

Diketahui data transistor :

hfe = 160

V_{BE} = 0,7 V

R_{Relay} = 440 Ω

V_{CC} = 12 V

Maka dapat dihitung :

$$I_C = \frac{V_{CC}}{R_{Relay}} = \frac{12}{440} = 27\ mA$$

$$I_B = \frac{I_C}{hfe} = \frac{0,027}{160} = 0,16875\ mA$$

$$R_B = \frac{5 - V_{BE}}{I_B} = \frac{5 - 0,7}{0,00016875} = 25,48\ K\Omega$$

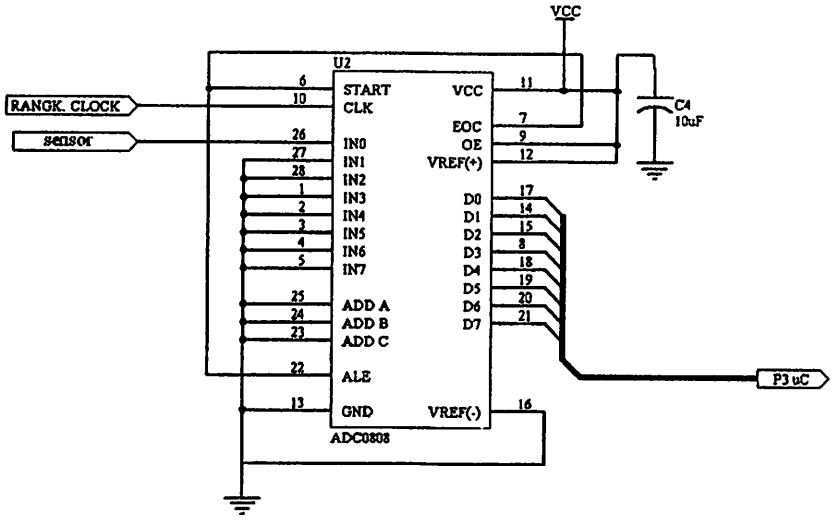
$$= 25\ K\Omega$$

Karena nilai resistansi di atas tidak ada di pasaran maka diambil nilai hambatan yang mendekati yaitu 22 KΩ. Pemasangan dioda disusun secara paralel dengan relay bertujuan membuang arus balik pada saat relay dalam keadaan ON. Jika arus ini tidak dibuang maka akan menyebabkan induksi magnetic pada kumparan relay sehingga menyebabkan rusaknya transistor.

3.1.3. Rangkaian ADC 0808

Dalam pembuatan alat ini juga dibutuhkan pengubah sinyal analog menjadi sinyal digital atau disebut juga Analog to Digital Converter (ADC), hal ini disebabkan karena sinyal-sinyal yang didapat dari sensor adalah berupa sinyal analog sedangkan

rangkaian mikrokontroller menggunakan system digital sehingga membutuhkan masukan berupa sinyal digital. ADC yang digunakan adalah ADC 0808. ADC ini dapat menerima hingga 8 inputan, tetapi yang digunakan pada alat ini hanya 1 inputan dan sisa inputan yang lain digroundkan. Karena hanya menggunakan 1 input maka ADD A, ADD B, ADD C diberi nilai low dengan cara dihubungkan ke ground. Rangkaian ADC 0808 ditunjukan dalam gambar 3-6 sebagai berikut :

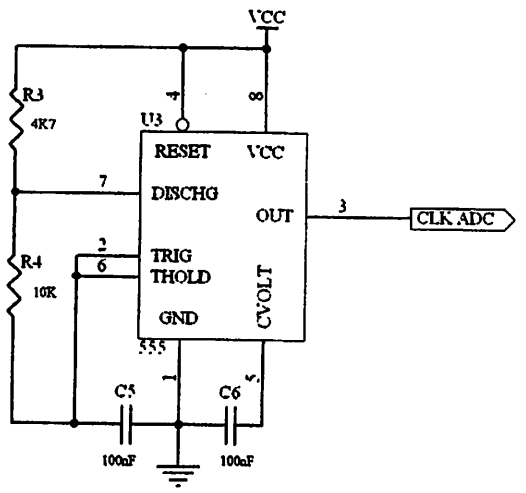


Gambar 3-6. Perancangan Rangkaian ADC 0808

Penjelasannya adalah sebagai berikut :

- Input 0 (pin 26) merupakan masukan yang berupa sinyal analog dari sensor LDR. Input 1 sampai input 7 digroundkan karena tidak digunakan.
- D0 sampai D7 yang merupakan output ADC 0808 dipergunakan untuk mengirim data digital ke mikrokontoller AT89S8252.

ADC 0808 tidak mempunyai clock internal sehingga memerlukan eksternal clock. Rangkaian eksternal clock untuk ADC 0808 ditunjukan oleh gambar 3-7 sebagai berikut :



Gambar 3-7. Perancangan Rangkaian Clock

Dari gambar rangkaian di atas dapat dihitung besarnya frekuensi yang dihasilkan adalah sebagai berikut:

$$f = \frac{1{,}44}{(R_A + 2R_B)C}$$

$$f = \frac{1{,}44}{(4{,}7.10^3 + 2.10.10^3)100.10^{-9}}$$

$f = 0{,}583$ KHz

Berdasarkan perhitungan di atas dapat diketahui besarnya frekuensi yang dihasilkan oleh rangkaian *clock eksternal* adalah 0,583 KHz.

3.1.4. Rangkaian LCD M1632

LCD Display Module M1632 buatan Seiko Instrument Inc. adalah komponen *display* yang paling umum digunakan saat ini. LCD M1632 merupakan panel LCD sebagai media penampil informasi dalam bentuk huruf/angka dua baris, masing-masing baris bisa menampung 16 huruf/angka.

Untuk berhubungan dengan mikrokontroller, pemakai LCD M1632 dilengkapi dengan 8 jalur data (**DB0..DB7**) yang dipakai untuk menyalurkan kode ASCII maupun perintah pengatur kerjanya M1632. Selain itu dilengkapi pula dengan **E, R/W*** dan **RS** seperti layaknya komponen yang kompatibel dengan mikroprosessor.

RS (Register Select) dipakai untuk membedakan jenis data yang dikirim ke M1632, kalau **RS=0** data yang dikirim adalah perintah untuk mengatur kerja M1632, sebaliknya kalau **RS=1** data yang dikirim adalah kode ASCII yang ditampilkan.

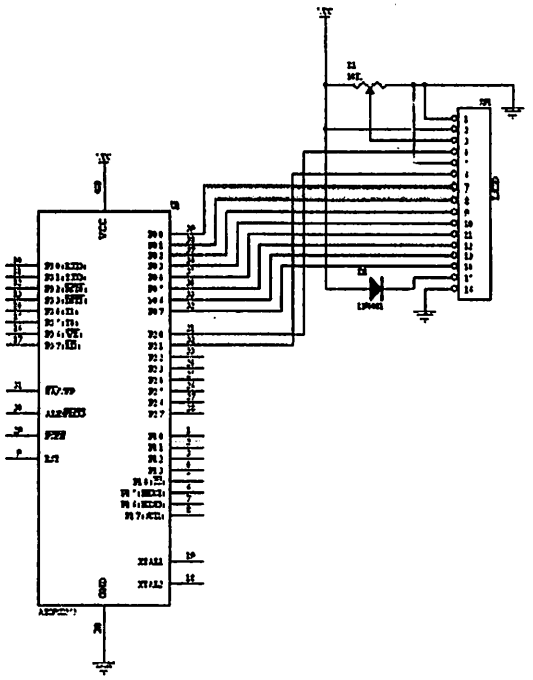
Proses mengirim/mengambil data ke/dari M1632 bisa dijabarkan sebagai berikut :

- **RS** harus dipersiapkan dulu, untuk menentukan jenis data seperti yang telah dibicarakan di atas.
- **R/W*** di-nol-kan untuk menandakan akan diadakan pengiriman data ke M1632. Data yang akan dikirim disiapkan di **DB0..DB7**, sesaat kemudian sinyal **E** di-satu-kan dan di-nol-kan kembali. Sinyal **E** merupakan sinyal sinkronisasi, saat **E** berubah dari 1 menjadi 0 data di **DB0 .. DB7** diterima oleh M1632.

- Untuk mengambil data dari M1632 sinyal **R/W*** di-satu-kan, menyusul sinyal **E** di-satu-kan. Pada saat **E** menjadi 1, M1632 akan meletakkan datanya di **DB0 .. DB7**, data ini harus diambil sebelum sinyal **E** di-nol-kan kembali.

M1632 mempunyai seperangkat perintah untuk mengatur tata kerjanya, perangkat perintah tersebut meliputi perintah untuk menghapus tampilan, meletakkan kembali cursor pada baris huruf pertama baris pertama, menghidup/matikan tampilan dan lain sebagainya, semua itu dibahas secara terperinci dalam Lembar Data M1632.

Untuk tampilan dipergunakan LCD Dot Matrik 2 x 16 karakter. Sinyal-sinyal yang diperlukan oleh LCD adalah RS dan Enable, sinyal RS dan Enable dipergunakan sebagai input yang outputnya dipakai untuk mengaktifkan LCD. LCD akan aktif apabila mikrokontroller memberikan instruksi tulis pada LCD. Saat kondisi RS don't care dan Enable 0 maka LCD tetap pada kondisi semula, pengiriman data ke LCD dilakukan saat RS berlogika 0 dan enable berlogika 1. Instruksi dikirim pada LCD bila keadaan RS 1 dan Enable 1. Pin LCD ini untuk data terkoneksi pada *Port 0* mikrokontoller. Kemudian untuk RS dihubungkan pada *Port 2.0*, tulis/baca *(Read/Write)* diberikan logika *low* karena disini LCD bersifat menulis data, dan yang terakhir *Enable* (E) dikendalikan dengan *Port 2.1*. Gambar rangkaian LCD ditunjukkan pada gambar 3-8 sebagai berikut :

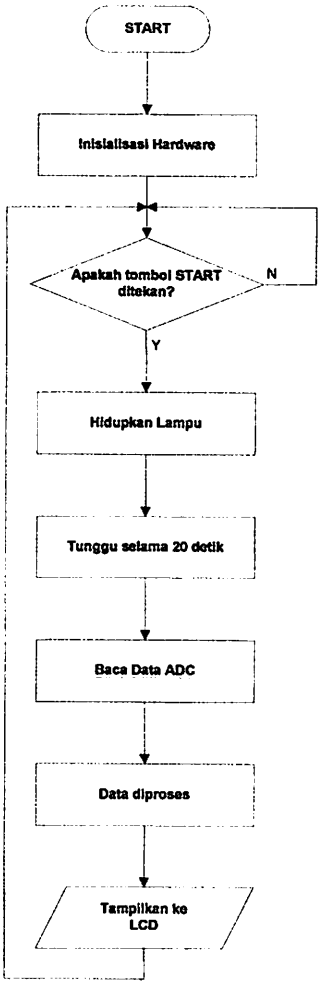


Gambar 3-8. Perancangan Liquid Crystal Display (LCD)

3.2. Perancangan Perangkat Lunak (Software)

Perancangan perangkat lunak (*software*) sangat diperlukan oleh *programmer* dalam mempermudah menentukan langkah-langkah atau alur dari program. Selain mempermudah langkah-langkah pemrograman, diagram alir juga difungsikan supaya program sesuai dan sinkron dengan kerja perangkat keras (*hardware*), sehingga sesuai dengan apa yang direncanakan. Mikrokontroller AT89S8252 menggunakan bahasa *C*. Untuk *compiler* menggunakan SDCC *(Small Device C Compiler)* dan untuk *software downloading programmer*-nya menggunakan *ISP-Flash Programmer-3.0a*

Mendesain *flowchart* sebelum membuat suatu program sangatlah penting, sehingga program yang akan dirancang sedemikian rupa. Selain itu juga memudahkan dalam penganalisaan bila terjadi kesalahan saat membuat program, dengan demikian akan menghasilkan suatu program yang waktu mengeksekusi bahasa atau menjalankan program sangat cepat. Agar perancangan perangkat lunak ini dalam pemahamannya lebih mudah, maka digunakan diagram alir seperti yang ditunjukkan dalam gambar 3-9 di bawah ini



Gambar 3-9. Flowchart Perangkat Lunak (Software)

BAB IV

PENGUJIAN ALAT

Setelah perangkat keras dan perangkat lunak yang direncanakan selesai dibuat, selanjutnya dilakukan pengujian terahadap alat yang dibuat. Tahap pengujian alat ini perlu untuk dilakukan untuk mendapatkan hasil pengukuran serta kerja alat sesuai dengan yang diharapkan.

4.1. Pengujian LDR

4.1.1. Tujuan

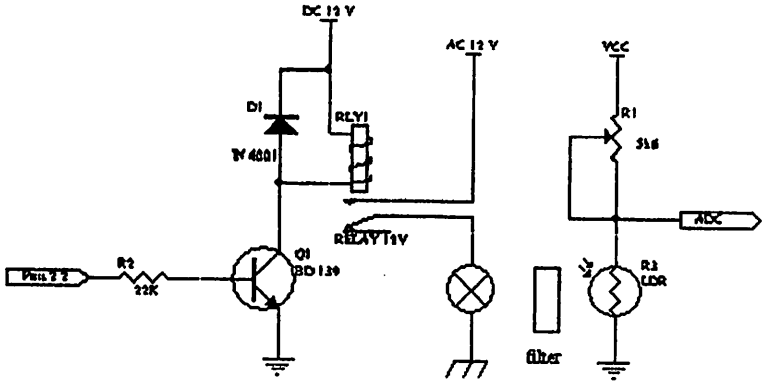
Pengujian LDR bertujuan untuk menguji kepekaan LDR terhadap intensitas cahaya yang dilewatkan.

4.1.2. Peralatan yang digunakan

- Power Supply
- Rangkain Pengujian LDR (sebagai sensor)
- Multimeter Digital

4.1.3. Langkah pengujian

- Merangkai rangkaian seperti pada gambar 4-1
- Menghubungkan rangkaian pengujian LDR dengan sumber tegangan.
- Menghubungkan kutub positif dan negatif multimeter digital (multimeter diset pada skala 20 Volt DC) dan mencatatnya pada tabel 4-1.



Gambar 4-1. Rangkaian Pengujian LDR

4.1.4. Hasil Pengujian

Tabel 4-1. Hasil Pengujian Kepekaan LDR

Percobaan	Tegangan Keluaran (Vo)		
	Lampu→LDR	Lampu→Filter →LDR	Lampu→Filter →Fokus →LDR
1	0,39Volt	0,43 Volt	0,26 Volt
2	0,38 Volt	0,44 Volt	0,26 Volt
3	0,38 Volt	0,43 Volt	0,25 Volt
4	0,39 Volt	0,43 Volt	0,26 Volt
5	0,39 Volt	0,44 Volt	0,25 Volt

Dari hasil pengujian dapat dihitung rata-rata tegangan keluaran (Vo) LDR sebagai berikut :

- Vo rata-rata Lampu → LDR

$$Vo = \frac{0,39+0,38+0,38+0,39+0,39}{5}$$

$$= 0,386 \text{ Volt}$$

- Vo rata-rata Lampu → Filter → LDR

$$Vo = \frac{0,43 + 0,44 + 0,43 + 0,43 + 0,44}{5}$$

$$= 0,434 \text{ Volt}$$

- Vo rata-rata Lampu → Filter → Fokus → LDR

$$Vo = \frac{0,26 + 0,26 + 0,25 + 0,26 + 0,25}{5}$$

$$= 0,256 \text{ Volt}$$

4.1.5. Kesimpulan

Dari data di atas dapat diperoleh kesimpulan bahwa semakin banyak penghalang antara cahaya lampu ke LDR maka intensitas cahaya yang masuk ke LDR akan kecil dengan demikian besarnya resistansi LDR akan semakin besar sehingga tegangan yang keluar dari rangkaian sensor akan kecil, demikian pula sebaliknya.

4.2. Pengujian Driver Lampu

4.2.1. Tujuan

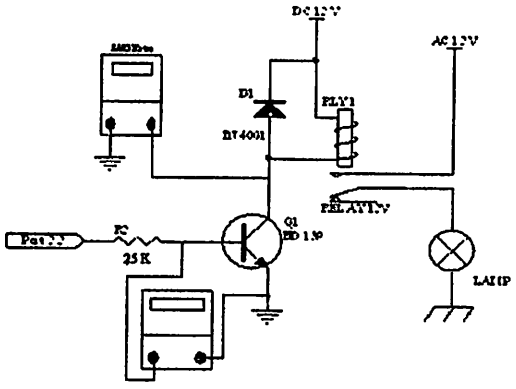
Pengujian driver lampu bertujuan untuk menguji fungsi kerja relay sebagai saklar.

4.2.2. Peralatan yang digunakan

- Power Supply
- Rangkain Pengujian Driver Lampu
- Multimeter Digital

4.2.3. Langkah Pengujian

- Merangkai rangkaian seperti pada gambar 4-2
- Menghubungkan rangkaian pengujian driver lampu dengan sumber tegangan.
- Menghubungkan kutub positif dan negatif multimeter digital dan diset pada skala 20 Volt DC lalu mencatatnya pada tabel 4-2.
- Menghubungkan kutub positif dan negatif multimeter digital dan diset pada skala 200 mA lalu mencatatnya pada tabel 4-2.



Gambar 4-2. Rangkaian Pengujian Driver Lampu

4.2.4. Hasil Pengujian

Tabel 4-2. Hasil Pengujian Diver Lampu

Percobaan	Tegangan (Volt)	Arus (mA)
1	0,72	26,7
2	0,73	27,1
3	0,73	27
4	0,72	26,8
5	0,71	25

4.2.5. Kesimpulan

Dari hasil pengujian driver lampu di atas dapat disimpulkan relay berfungsi dengan baik sebagai saklar, dan tegangan keluaran semakin besar bersamaan dengan semakin stabilnya cahaya lampu.

4.3. Pengujian ADC 0808

4.3.1 Tujuan

Untuk mengetahui kombinasi logika keluaran dari ADC terhadap inputan tegangan yang diberikan.

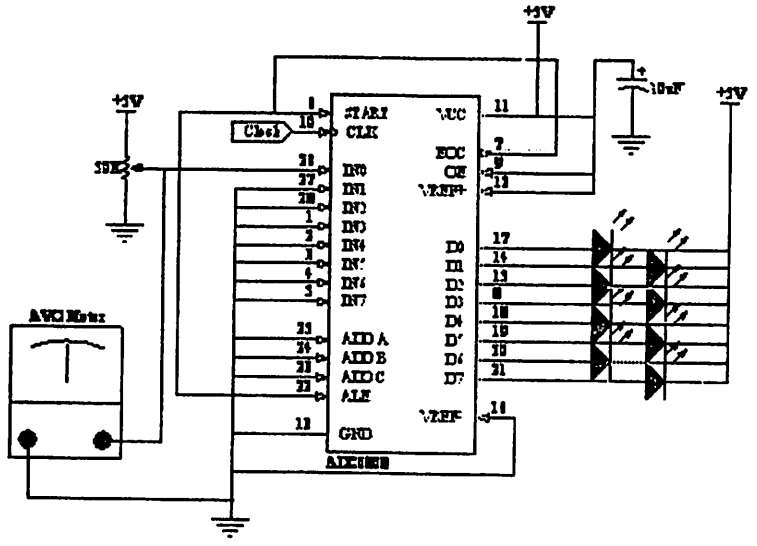
4.3.2. Peralatan yang digunakan

- Power Supply
- Rangkaian Pengujian ADC 0808
- Multimeter Digital

4.3.3. Langkah Pengujian

- Merangkai rangkaian seperti pada gambar 4-3
- Menghubungkan pin – pin keluaran dari ADC 0808 dengan rangkaian LED.
- Menghubungkan V_R ke pin 26 pada ADC 0808 (Vin-0).
- Menghubungkan rangkaian pengujian ADC 0808 dengan sumber tegangan 5 Volt.
- Menghubungkan kutub positif dan negatif multimeter digital (multimeter diset pada skala 20 Volt DC) pada V_R sebagai Vin-0, kemudian memutar V_R (tentukan nilai Vin-0 yang diinginkan) dan mencatatnya pada tabel 4-3.

➢ Mengamati LED yang menyala dan mati sebagai indikator keluaran 8 bit dari ADC 0808. Mencatat hasilnya pada tabel 4-3



Gambar 4-3. Rangkaian Pengujian ADC 0808

4.3.4. Hasil Pengujian

Tabel 4-3. Hasil Pengujian ADC 0808

Vin (Volt)	Keluaran ADC 0808				Selisih (Hexa)
	Pengukuran		Perhitungan		
	D7 – D0	Hexa	D7 – D0	Hexa	
0	00000000	00h	00000000	00h	00h
0,86	00101011	2Bh	00101100	2Ch	01h
1,01	00110100	34h	00110100	34h	00h
1,26	01000000	40h	01000000	40h	00h
1,88	01011101	5Dh	01100000	60h	03h
2,06	01101000	68h	01101001	69h	01h
2,5	10000000	80h	10000000	80h	00h
3,5	10110100	B4h	10110011	B3h	01h

3,76	10111110	BEh	11000000	C0h	02h
3,86	11000100	C4h	10110101	C5h	01h
4,12	11010001	D1h	11010010	D2h	01h
4,46	11100010	E2h	11100100	E4h	02h

Untuk perhitungan Beda tegangan/bit dari output ADC 0808 dapat dicari dengan menggunakan rumus berikut:

$$\text{Beda tegangan / bit} = \frac{Vref^{(+)} - Vref^{(-)}}{2^8 - 1}$$

Dimana: $Vref^{(+)} = 5$ Volt

$Vref^{(-)} = 0$ Volt

Sehingga:

$$\text{Beda tegangan / bit} = \frac{Vref^{(+)} - Vref^{(-)}}{2^8 - 1}$$

$$= \frac{5-0}{256-1} = \frac{5}{255} = 0{,}0196 \text{ Volt}$$

Dan untuk keluaran ADC 0808 dapat dicari dengan menggunakan rumus berikut:

$$Out_{ADC(desimal)} = \frac{Vin}{BedaTegangan/Bit}$$

Dimana:

Vin = tegangan input ADC 0808

Beda Tegangan/Bit = 0,0196 Volt

Contoh: Jika diketahui Vin 1,01 Volt. Maka berapakah keluaran ADC 0808 ?

Penyelesaian:

$$Out_{ADC(desimal)} = \frac{Vin}{BedaTegangan/Bit}$$

$$Out_{ADC(desimal)} = \frac{1,01}{0,0196}$$

$$= 51,53 \approx 52_{(10)}$$

$Out_{ADC(biner)} = 00110100_{(2)}$

$Out_{ADC(hexa)} = 34_{(16)}$

Dari tabel diatas dapat dicari persentase kesalahan (%error) dari rangkaian. Untuk persentase kesalahan dapat dicari dengan menggunakan persamaan sebagai berikut:

$$\text{Error rata-rata} = \frac{JumlahError}{JumlahPerhitungan} x100\%$$

Jika dari tabel diketahui:

$\sum$ Perhitungan (desimal) = 1495

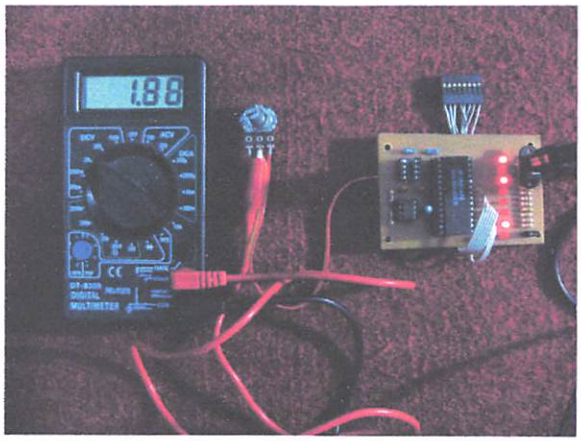
$\sum$ Error $= 12_{(16)} = 18_{(10)}$

Sehingga kesalahan rata-ratanya:

$$\text{Error rata-rata} = \frac{JumlahError}{JumlahPerhitungan} x100\%$$

$$= \frac{18}{1495} x100\%$$

$$= 0,012\ \%$$



Gambar 4-4. Hasil Pengujian ADC 0808

4.3.5. Kesimpulan

Pada saat tegangan sebesar 0 volt semua LED nyala dan pada saat tegangan 5 volt semua LED mati dan perubahan setiap bitnya sebesar 19,6 mV.

4.4. Pengujian LCD M1632

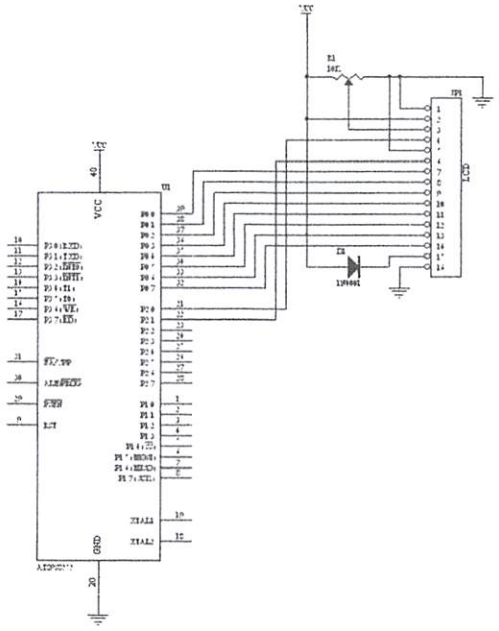
4.4.1. Tujuan

Untuk mengetahui LCD yang digunakan dalam keadaan baik.

4.4.2. Peralatan yang digunakan

- Minimum Sistem AT89S8252
- LCD M1632
- Power Supply

Berikut adalah gambar dari LCD M1632 yang akan diuji :



Gambar 4-5. Rangkaian Pengujian LCD M1632

4.4.3. Hasil Pengujian

Gambar 4-6. Pengujian Rangkaian LCD M1632

Di bawah ini adalah tabel dari pengujian instruksi dari LCD M1632.

Tabel 4-4. Hasil Pengujian Instruksi

Instruksi	Kode										Fungsi
	RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	
Display Clear	0	0	0	0	0	0	0	0	0	1	Menghapus semua tampilan layar dan mengembalikan *cursor* ke posisi semula
Cursor Home	0	0	0	0	0	0	0	0	1	*	*Cursor* kembali ke posisi semula dan geser layar ke posisi semula
Empty Mode Set	0	0	0	0	0	0	0	1	I/D	S	Mengatur arah gerakan *cursor* dan menggeser layar ketika data sudah ditulis/dibaca
Display ON/OFF Control	0	0	0	0	0	0	1	D	C	B	Menyalakan/mematikan semua layar (D) dan *cursor* (C), dan membuat kolom *cursor* pada posisi awal kosong
Cursor/Display Shift	0	0	0	0	0	1	S/C	R/L	*	*	Memindahkan *cursor* dan menggeser layar
Function Set	0	0	0	0	1	DL	1	*	*	*	Mengatur penambahan banyaknya data
CG RAM Address Set	0	0	0	1	A_{CG}						Menulis alamat RAM ke karakter
DD RAM Address Set	0	0	1	A_{DD}							Menulis alamat RAM ke tampilan
BF/address read	0	1	BF	AC							LCD dalam keadaan sibuk atau tidak sibuk
Data Write to CG RAM or DD RAM	1	0	Write data								Menulis data ke DD RAM atau CG RAM
Data Write from CG RAM or DD RAM	1	1	Read data								Membaca data dari DD RAM atau CG RAM

Keterangan :

1. Empty mode Set : layar beraksi sebagai tampilan tulis.

   S : 1/0 = menggeser layar.

   I/D : 1 = kursor bergerak ke kanan dan layar bergerak ke kiri.

I/D : 0 = kursor bergerak ke kiri dan layar bergerak ke kanan

2. Display On/Off kontrol.

   D : 1 = layar on

   D : 0 = layar off

   C : 1 = kursor on

   C : 0 = kursor off

   B : 1 = kursor berkedip-kedip

   B : 0 = kursor tidak berkedip – kedip

3. Cursor Display Shift

   S/C : 1 = LCD diidentifikasikan sebagai layar

   S/C : 0 = LCD diidentifikasikan sebagai kursor

   R/L : 1 = menggeser satu spasi ke kanan

   R/L : 0 = menggeser satu spasi ke kiri

4. Fuction Set

   DL : 1 = panjang data LCD pada 8 bit

   DL : 0 = panjang data LCD pada 4 bit

   Bit upper ditransfer terlebih dahulu kemudian diikuti dengan 4 bit lower.

5. CG RAM Address Set :

   A_{CG} = alamat CG RAM

6. DD RAM address set :

   A_{DD} = alamat DD RAM

7. BF/address read :

BF : 1 = pengoperasian instruksi sedang dijalankan

BF : 0 = instruksi dapat diterima

4.4.4. Kesimpulan

Setelah dilakukan pengujian seperti tabel di atas, kemudian dibandingkan dengan *data sheet* LCD M1632 ternyata hasilnya sesuai. Berarti dapat disimpulkan bahwa LCD dalam keadaan baik.

4.5. Pengujian Alat Keseluruhan

4.5.1. Tujuan

Untuk mengetahui alat yang dibuat sesuai dengan yang telah dirancangkan.

4.5.2. Peralatan yang digunakan

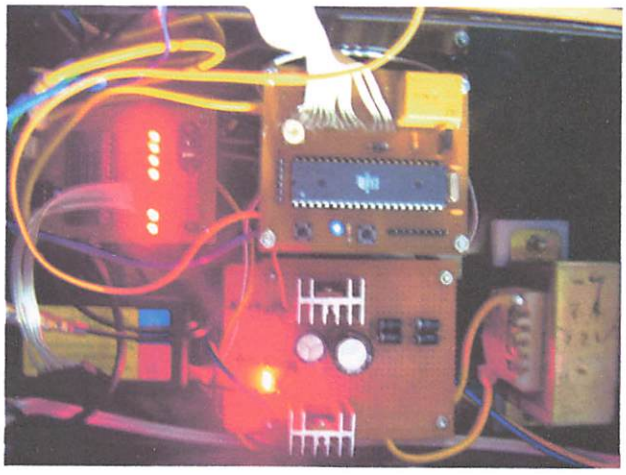
- Alat Ukur Kadar Na Darah
- Sampel serum darah
- Wadah sampel (kuvet)
- Suntik

4.5.3. Langkah Pengujian

- Siapkan serum darah dalam kuvet dan letakkna kuvet pada tempat yang disediakan pada alat
- Hidupkan saklar catu daya
- Tekan tombol start dan tunggu sampai muncul tampilan hasil
- Untuk melakukan pengukuran ulang, tekan tombol start

Di bawah ini adalah gambar alat yang akan diuji :

Gambar 4-7. Alat Pengukur Kadar Na Darah



Gambar 4-8. Pengujian Keseluruhan Rangkaian

4.5.4. Hasil Pengujian

Tabel 4-5. Hasil Pengujian Alat

Sampel	Kadar Na Darah (mmol/L)		Selisih Hasil Pengukuran
	Electrolite Analyzer	Alat Ukur Na Darah	
1	135	127	8
		134	1
		131	4
		129	6
		134	1
		131	4
2	141	140	1
		145	4
		145	4
		143	2
		140	1
		140	1
3	151	150	1
		159	8
		152	1
		156	5
		150	1
		147	4

Dari tabel diatas dapat dicari persentase kesalahan (%error) alat. Untuk persentase kesalahan dapat dicari dengan menggunakan persamaan sebagai berikut:

$$\text{Error rata-rata} = \frac{JumlahSelisih}{BanyakPercobaan} x100\%$$

Jika dari tabel diketahui untuk kadar Na darah = 135 mmol/L :

$\sum$ Selisih hasil pengukuran = 24

$\sum$ Banyak percobaan = 6

Sehingga kesalahan rata-ratanya:

$$\text{Error rata-rata} = \frac{JumlahSelisih}{BanyakPercobaan} x100\%$$

$$= \frac{24}{6} x100\%$$

$$= 4\,\%$$

Jika dari tabel diketahui untuk kadar Na darah = 141 mmol/L :

$\sum$ Selisih hasil pengukuran = 13

$\sum$ Banyak percobaan = 6

Sehingga kesalahan rata-ratanya:

$$\text{Error rata-rata} = \frac{JumlahSelisih}{BanyakPercobaan} x100\%$$

$$= \frac{13}{6} x100\%$$

$$= 2{,}167\,\%$$

Jika dari tabel diketahui untuk kadar Na darah = 151 mmol/L :

$\sum$ Selisih hasil pengukuran = 20

$\sum$ Banyak percobaan = 6

Sehingga kesalahan rata-ratanya:

$$\text{Error rata-rata} = \frac{JumlahSelisih}{BanyakPercobaan} x100\%$$

$$= \frac{20}{6} x100\%$$

$$= 3{,}33\ \%$$

Gambar 4-9. Tampilan LCD Hasil Pengujian Alat

4.5.5. Kesimpulan

Dari hasil pengujian alat secara keseluruhan didapatkan selisih atau error yang berbeda untuk tiap sampel. Posisi wadah sampel atau kuvet harus tegak lurus dan sejajar dengan titik fokus cahaya yang diteruskan oleh lensa fokus dan sensor.

BAB V

PENUTUP

5.1. Kesimpulan

Dari perancangan dan pembuatan alat pengukur kadar natrium (Na) darah berbasis mikrokontroller AT89S8252 ini, maka dapat diambil kesimpulan sebagai berikut :

1. Dari hasil pengujian, untuk serum dengan kadar Na 135 mmol/L terdapat error 4 %, serum dengan kadar Na 141 mmol/L terdapat error 2,167 %, dan utnuk serum dengan kadar Na 151 mmol/L terdapat error 3,33 %.
2. Lampu yang digunakan adalah lampu tungsten halogen yang mampu menghasilkan cahaya tampak dalam daerah panjang gelombang 350-2500 nm, dan untuk mendapatkan cahaya monokrom kuning dengan panjang gelombang 580-595 nm maka dipasang filter cahaya transparan kuning.
3. Sensor cahaya yang digunakan adalah sensor LDR (*Light Dependent Resistors*) NORP12 RS *stock number* 651-507.
4. Waktu yang dibutuhkan lampu sampai mendapatkan cahaya yang diinginkan (cahaya putih) ± 20 detik.
5. Posisi wadah sampel atau kuvet harus tegak lurus dan sejajar dengan titik fokus cahaya yang diteruskan oleh lensa fokus dan sensor.
6. Jarak antara lampu sebagai sumber cahaya ke sensor baik dengan obyek penghalang atau tanpa obyek penghalang adalah ± 39 cm.

5.2. Saran

1. Agar alat ini dapat bekerja dengan lebih baik, sebaiknya menggunakan komponen-komponen yang lebih baik dan lebih sensitive misalnya sensor yang digunakan dapat menggunakan sensor photodioda silicon type VTB1012 atau VTB1013
2. Untuk pengembangan lebih lanjut, sebaiknya alat ini dihubungkan langsung ke komputer sehingga dapat dijadikan data base dan hasil pengukuran juga dapat langsung dicetak.

DAFTAR PUSTAKA

Basset J, dkk, **Buku Ajar VOGEL Kimia Analisis Kuantitatif Anorganik**, EGC, Jakarta, 2002

Ibnu Malik, Mohammad, **Belajar Mikrokontroller ATMEL AT89S8252**, Gava Media, Yogyakarta, 2002

Khopkar, SM, **Konsep Dasar Kimia Analitik**, Universitas Indonesia, Jakarta, 2003

Malvino, Albert P, **Prinsip-Prinsip Elektronika**, PT. Salemba Teknika, Jakarta, 2003

Peter A, Mayes, dkk, **Biokimia Harper Edisi 20**, EGC, Jakarta, 1992

Wasito S, **Vademekum Elektronika Edisi Kedua**, PT. Gramedia Pustaka Utama, Jakarta, 1990

www.wikipedia.com

www.alldatasheet.com

www.national.com

LAMPIRAN

INSTITUT TEKNOLOGI NASIONAL
JL. RAYA KARANGLO KM2
MALANG

FORMULIR BIMBINGAN SKRIPSI

Nama : Hesti Puspita
Nim : 02 17 061
Masa Bimbingan : 5 Oktober 2006 – 5 April 2006
Judul Skripsi : **Perencanaan Dan Pembuatan Alat Pengukur Kadar Natrium (Na) Dalam Darah Berbasis Mikrokontroller AT89S8252.**

NO	Tanggal	Uraian	Paraf Pembimbing
1	2/03/07	Konsultasi Bab 1, Bab 2, Bab 3	
2	5/04/07	Konsultasi Bab 4 & Bab 5	
3	8/03/07	Mahalah seminar proposal	
4	14/03/07	Laporan skripsi Revisi. Kesimpulan & penyajian	
5	15/03/07	Acc skripsi	
6			
7			
8			
9			
10			

Malang,
Dosen Pembimbing

I Komang Somawirata, ST, MT
Nip. **1030100361**

INSTITUT TEKNOLOGI NASIONAL MALANG
FAKULTAS TEKNOLOGI INDUSTRI
JURUSAN TEKNIK ELEKTRO S-1
KONSENTRASI TEKNIK ELEKTRONIKA

FORMULIR PERBAIKAN SKRIPSI

Dari hasil ujian komprehensip jenjang Strata Satu (S-1) Jurusan Teknik Elektro, Konsentrasi Elektronika yang diselenggarakan pada:

Hari : Sabtu
Tanggal : 17 Maret 2007

Telah dilakukan perbaikan skripsi oleh :

Nama : Hesti Puspita
N.I.M : 02.17.061
Masa Bimbingan : 05 Oktober s/d 05 April
Judul : Perencanaan Dan Pembuatan Alat Pengukur Kadar Natrium (Na) Dalam Darah Berbasis Mikrokontroller AT89S8252

Perbaikan Meliputi :

No.	Materi Perbaikan	Paraf Dosen Penguji
1.	Kata-kata Tugas Akhir harap dirubah Skripsi (hal. 4)	

Disetujui Oleh:
Penguji Kedua

(Ir. Teguh Herbasuki, MT)
NIP.Y. 1038900209

Mengetahui
Dosen Pembimbing

I Komang Somawirata,ST,MT
NIP. 1030100361

INSTITUT TEKNOLOGI NASIONAL MALANG
FAKULTAS TEKNOLOGI INDUSTRI
JURUSAN TEKNIK ELEKTRO S-1
KONSENTRASI TEKNIK ELEKTRONIKA

FORMULIR PERBAIKAN UKNTSPI

Dalam hasil ujian komprehensif terdapat satu atau lebih (2-1) mahasiswa tersebut

Elektro Konsentrasi Elektronika yang dipertanggungkan bahwa:

Hari : Selasa
Tanggal : 11 Maret 2003

Telah dilakukan perbaikan skripsi oleh :

Nama : Ifan Tusbita
NIM : 03.17.091
Masa Bimbingan : 02 Oktober s/d 02 April
Judul : Perancangan dan Pembuatan Alat Pendukung Kedap
Mikrokontroller AT89S8252

Perbaikan Meliputi :

No.	Materi Perbaikan	Paraf Dosen Penguji
1.	Kata-kata dalam Abstrak perlu diperbaiki (hal. 4)	

Disetujui Oleh:

Penguji Kedua

(Ir. Taufik Hidayat, ME)
NIP.Y. 1028900350

Mengetahui
Dosen Pembimbing

(Ir. Ichsan Setiawan S.T.M.T.)
NIP. 1030100391

INSTITUT TEKNOLOGI NASIONAL
FAKULTAS TEKNOLOGI INDUSTRI
JURUSAN TEKNIK ELEKTRO

Formulir Perbaikan Ujian Skripsi

ım pelaksanaan Ujian Skripsi Janjang Strata 1 Jurusan Teknik Elektro Konsentasi ~~T. Energi~~
ik / T. Elektronika, maka perlu adanya perbaikan skripsi untuk mahasiswa :

IA : Hesti Puspita
I : 0217061.
aikan meliputi :

tn² Tugas Akhir harap dirubah "Skripsi". hal 4.

Malang,

(_____)

DATA HASIL PENGUKURAN

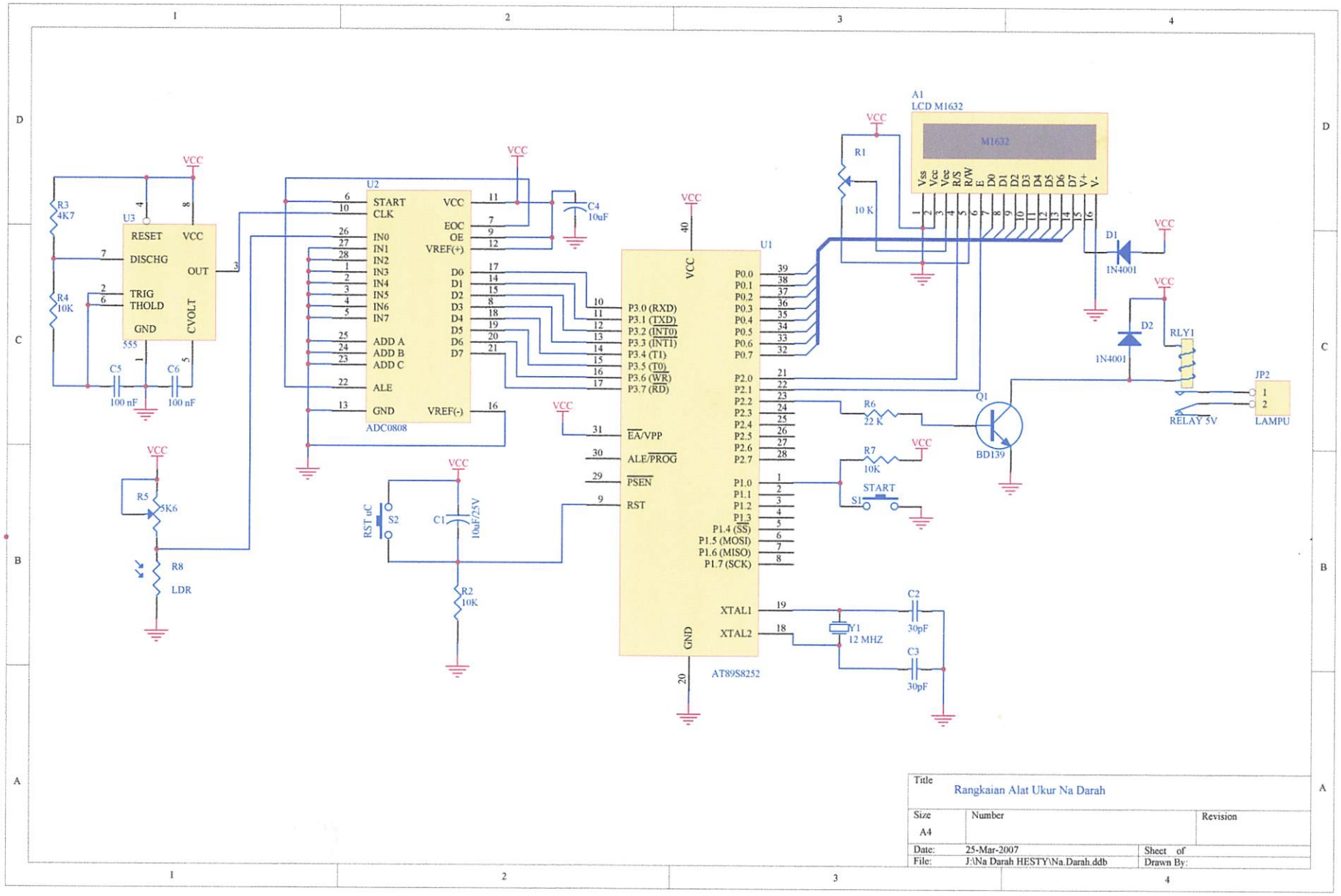
Sampel	Kadar Na Darah (mmol/L)		Selisih Hasil Pengukuran
	Electrolite Analyzer	Alat Ukur Na Darah	
1	135	127	8
		134	1
		131	4
		129	6
		134	1
		131	4
2	141	140	1
		145	4
		145	4
		143	2
		140	1
		140	1
3	151	150	1
		159	8
		152	1
		156	5
		150	1
		147	4

Mengetahui
Ka. Instalasi Laboratorium Sentral
RSU Dr. Saiful Anwar Malang

a/n

RSU. dr. "SAIFUL ANWAR MALANG"
INSTALASI LABORATORIUM SENTRAL

Dr. Ati Rastini Retno Indrati, SpPK (K)
NIP : 130809127



Title	Rangkaian Alat Ukur Na Darah		
Size A4	Number		Revision
Date:	25-Mar-2007	Sheet of	
File:	J:\Na Darah HESTY\Na.Darah.ddb	Drawn By:	

```
                                        Natrium
************************************************************
            Hesti Puspita

       Institut Teknologi Nasional Malang

************************************************************/

clude       <AT89S8252.h>   //AT89S8252.h
clude       <stdio.h>
clude       "lcd.h"         //Data P0, RS P2.0, E P2.1

fine relay  P2_2            //Aktif High
fine start  P1_0            //Aktif Low
fine adc    P3

at datadc;

i inittimer0()

    TMOD = 0x10;
    TH1 = 60;
    TL1 = 176;
    TR1 = 1;


i delay1s()

    unsigned int j = 0;
    TR1 = 1;
    while( j < 20 )
    {
            while(!TF1);
            TF1 = 0;
            j++;
    }
    TR1 = 0;


i delay4s()

    unsigned char hit = 0;
    while( hit < 4 )
    {
            delay1s();
            hit++;
    }


l tunggu()

    clear();
    TulisLCD(0x80,"Please Wait");
    delay4s();
    TulisLCD(0x8B,".");
    delay4s();
    TulisLCD(0x8C,".");
    delay4s();
    TulisLCD(0x8D,".");
    delay4s();
    TulisLCD(0x8E,".");
    delay4s();


l tampil_angka(int lokasi,int nilai)

    unsigned int angka;
    LCDdata(0,0x04);                //auto decrement
    LCDdata(0,lokasi);
```

```
    while(nilai > 9)
    {
            angka = nilai % 10;
            LCDdata(1,angka + 0x30);
            nilai = nilai / 10;
    }
    LCDdata(1,nilai + 0x30);
    LCDdata(1,0x20);
    LCDdata(0,0x06);                    //auto increment


i main()

    relay = 0;
    inittimer0();
    initLCD();
    clear();

    TulisLCD(0x80," Hesti Puspita ");
    TulisLCD(0xC0,"   02.17.061   ");

    while(1)
    {
            if (start == 0)
            {
                    relay = 1;
                    tunggu();
                    clear();
                    TulisLCD(0x80," Kadar Na Darah ");
                    datadc = adc;
                    datadc = (datadc/256)*582;
                    if ( datadc >= 120 && datadc <=200 )
                    {
                            TulisLCD(0xC7,"mmol/L");
                            tampil_angka(0xC5,datadc);
                    }
                    else
                    {
                            TulisLCD(0xC0,"   Data Error   ");
                    }
                    relay = 0;
            }
    }
```

Data Sheet

Light dependent resistors

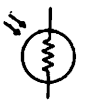
NORP12 RS stock number 651-507
NSL19-M51 RS stock number 596-141

Two cadmium sulphide (CdS) photoconductive cells with spectral responses similar to that of the human eye. The cell resistance falls with increasing light intensity. Applications include smoke detection, automatic lighting control, batch counting and burglar alarm systems.

Guide to source illuminations

Light source	Illumination (Lux)
Moonlight	0.1
60W bulb at 1m	50
1W MES bulb at 0.1m	100
Fluorescent lighting	500
Bright sunlight	30,000

Circuit symbol



Light memory characteristics

Light dependent resistors have a particular property in that they remember the lighting conditions in which they have been stored. This memory effect can be minimised by storing the LDRs in light prior to use. Light storage reduces equilibrium time to reach steady resistance values.

NORP12 (RS stock no. 651-507)

Absolute maximum ratings

Voltage, ac or dc peak	320V
Current	75mA
Power dissipation at 30°C	250mW
Operating temperature range	-60°C to +75°C

Electrical characteristics

T_A = 25°C. 2854°K tungsten light source

Parameter	Conditions	Min.	Typ.	Max.	Units
Cell resistance	1000 lux	-	400	-	Ω
	10 lux	-	9	-	kΩ
Dark resistance	-	1.0	-	-	MΩ
Dark capacitance	-	-	3.5	-	pF
Rise time 1	1000 lux	-	2.8	-	ms
	10 lux	-	18	-	ms
Fall time 2	1000 lux	-	48	-	ms
	10 lux	-	120	-	ms

1. Dark to 110% R_L
2. To 10 × R_L

R_L = photocell resistance under given illumination.

Features

- Wide spectral response
- Low cost
- Wide ambient temperature range.

Dimensions

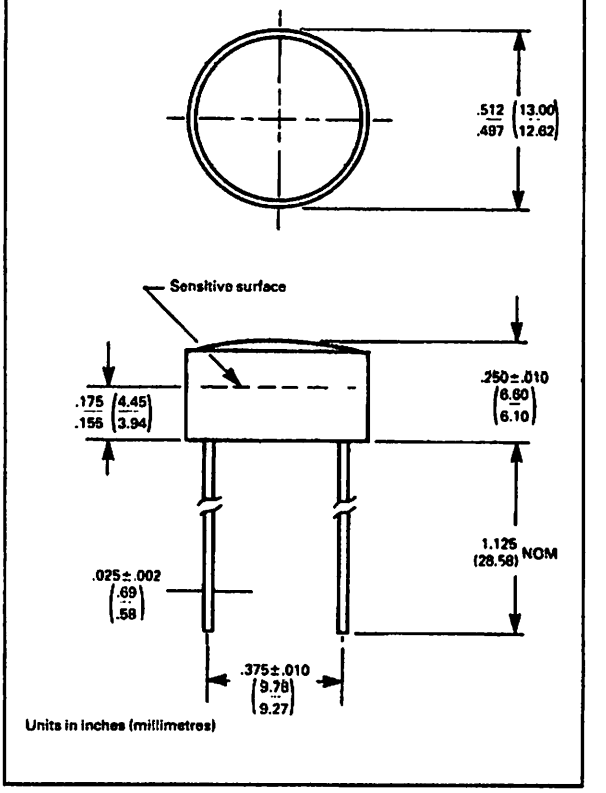


Figure 1 Power dissipation derating

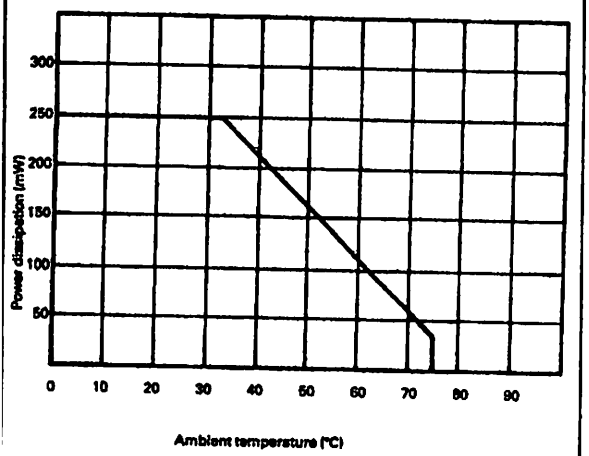
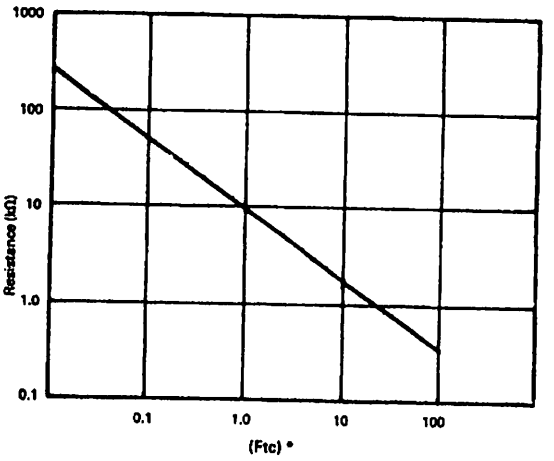
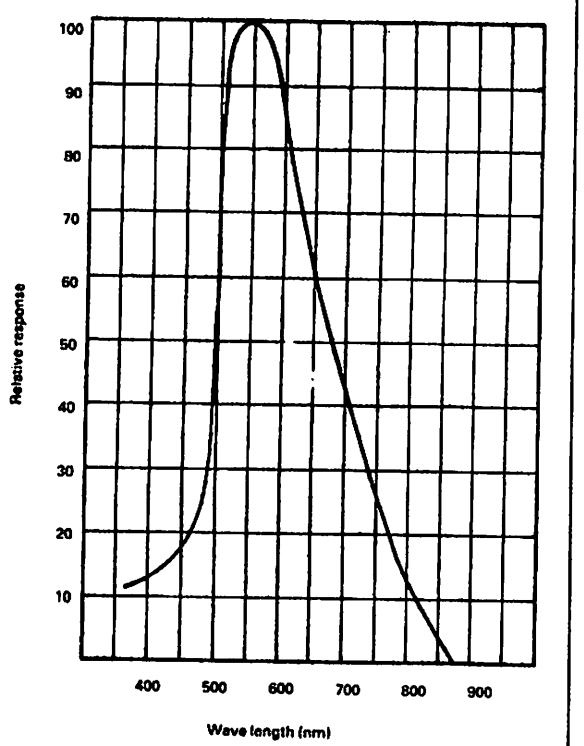


Figure 3 Resistance as a function of illumination



*1Ftc=10.764 lumens

Figure 2 Spectral response



Absolute maximum ratings

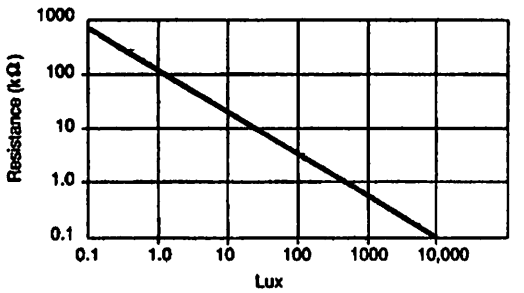
Voltage, ac or dc peak _____ 100V
Current _____ 5mA
Power dissipation at 25°C _____ 50mW*
Operating temperature range _____ -25°C +75°C

*Derate linearly from 50mW at 25°C to 0W at 75°C.

Electrical characteristics

Parameter	Conditions	Min.	Typ.	Max.	Units
Cell resistance	10 lux	20	-	100	kΩ
	100 lux	-	5	-	kΩ
Dark resistance	10 lux after 10 sec	20	-	-	MΩ
Spectral response	-	-	550	-	nm
Rise time	10ftc	-	45	-	ms
Fall time	10ftc	-	55	-	ms

Figure 4 Resistance as a function illumination



Dimensions

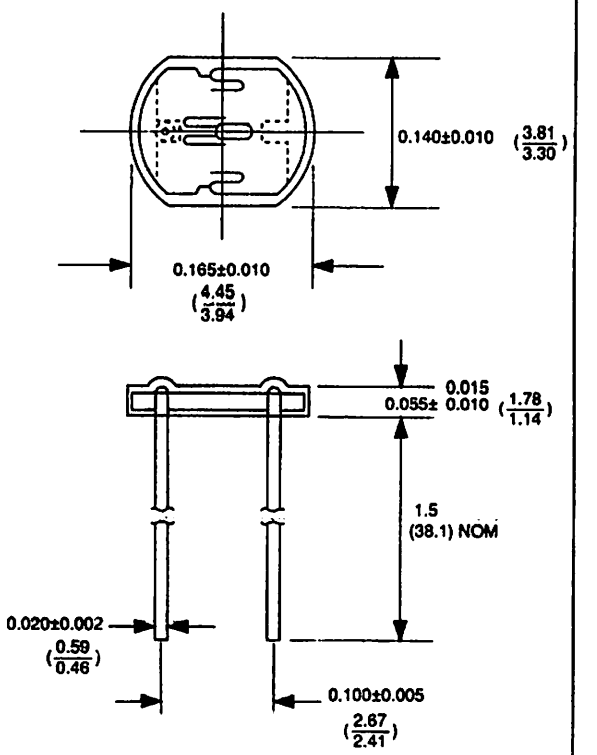
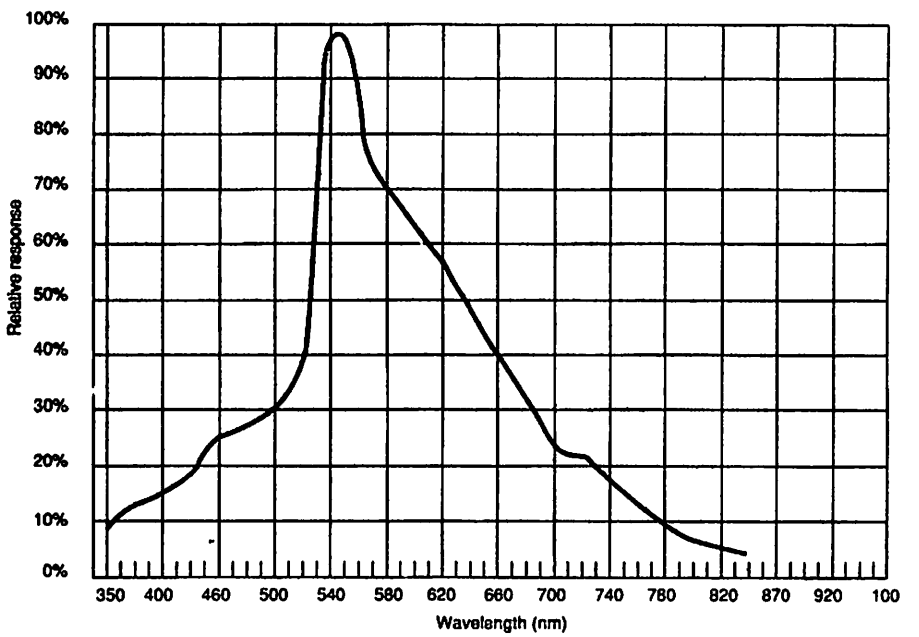
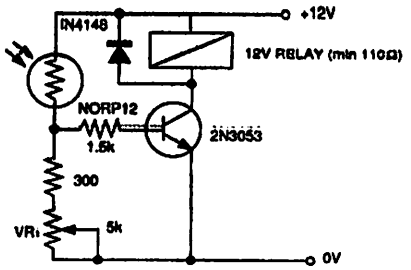


Figure 5 Spectral response



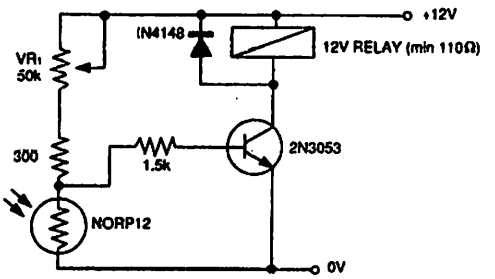
Typical application circuits

Figure 6 Sensitive light operated relay



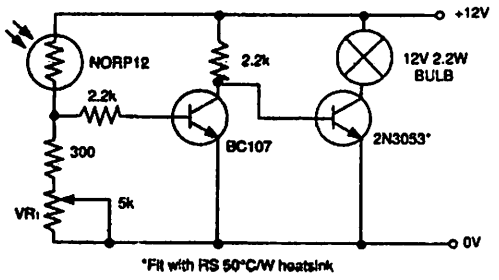
Relay energised when light level increases above the level set by VR_1

Figure 7 Light interruption detector



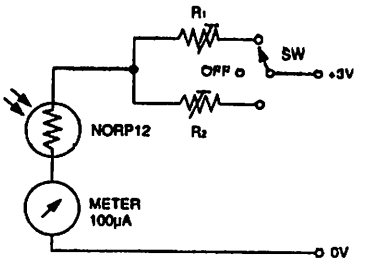
As Figure 6 relay energised when light level drops below the level set by VR_1

Figure 8 Automatic light circuit



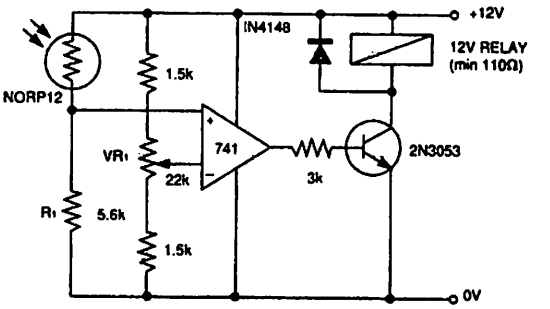
Adjust turn-on point with VR_1

Figure 9 Logarithmic law photographic light meter



Typical value $R^1 = 100k\Omega$
$R^2 = 200k\Omega$ preset to give two overlapping ranges.
(Calibration should be made against an accurate meter.)

Figure 10 Extremely sensitive light operated relay



(Relay energised when light exceeds preset level.)
Incorporates a balancing bridge and op-amp. R_1 and NORP12 may be interchanged for the reverse function.

BD135
BD139

NPN SILICON TRANSISTORS

- STMicroelectronics PREFERRED SALESTYPES

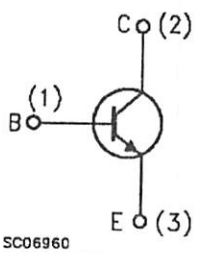
SOT-32

DESCRIPTION

The BD135 and BD139 are silicon epitaxial planar NPN transistors in Jedec SOT-32 plastic package, designed for audio amplifiers and drivers utilizing complementary or quasi compementary circuits.

The complementary PNP types are BD136 and BD140 respectively.

INTERNAL SCHEMATIC DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value		Unit
		BD135	BD139	
V_{CBO}	Collector-Base Voltage (I_E = 0)	45	80	V
V_{CEO}	Collector-Emitter Voltage (I_B = 0)	45	80	V
V_{EBO}	Emitter-Base Voltage (I_C = 0)	5		V
I_C	Collector Current	1.5		A
I_{CM}	Collector Peak Current	3		A
I_B	Base Current	0.5		A
P_{tot}	Total Dissipation at $T_c \leq 25$ °C	12.5		W
P_{tot}	Total Dissipation at $T_{amb} \leq 25$ °C	1.25		W
T_{stg}	Storage Temperature	-65 to 150		°C
T_j	Max. Operating Junction Temperature	150		°C

THERMAL DATA

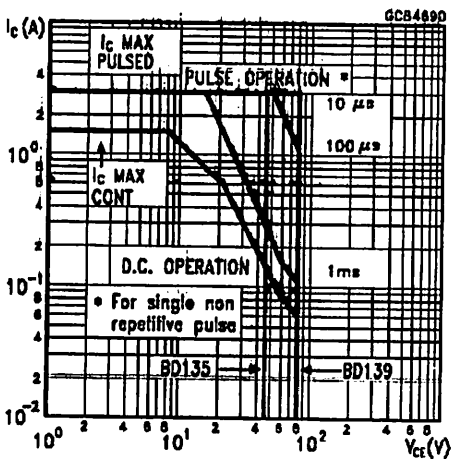
$R_{thj\text{-}case}$	Thermal Resistance Junction-case	Max	10	°C/W

ELECTRICAL CHARACTERISTICS (T_{case} = 25 °C unless otherwise specified)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
I_{CBO}	Collector Cut-off Current (I_E = 0)	V_{CB} = 30 V V_{CB} = 30 V T_C = 125 °C			0.1 10	µA µA
I_{EBO}	Emitter Cut-off Current (I_C = 0)	V_{EB} = 5 V			10	µA
$V_{CEO(sus)}$*	Collector-Emitter Sustaining Voltage	I_C = 30 mA for **BD135** for **BD139**	 45 80			 V V
$V_{CE(sat)}$*	Collector-Emitter Saturation Voltage	I_C = 0.5 A I_B = 0.05 A			0.5	V
V_{BE}*	Base-Emitter Voltage	I_C = 0.5 A V_{CE} = 2 V			1	V
h_{FE}*	DC Current Gain	I_C = 5 mA V_{CE} = 2 V I_C = 0.5 A V_{CE} = 2 V I_C = 150 mA V_{CE} = 2 V	25 25 40		 250	
h_{FE}	h_{FE} Groups	I_C = 150 mA V_{CE} = 2 V for BD139 group 10	 63		 160	

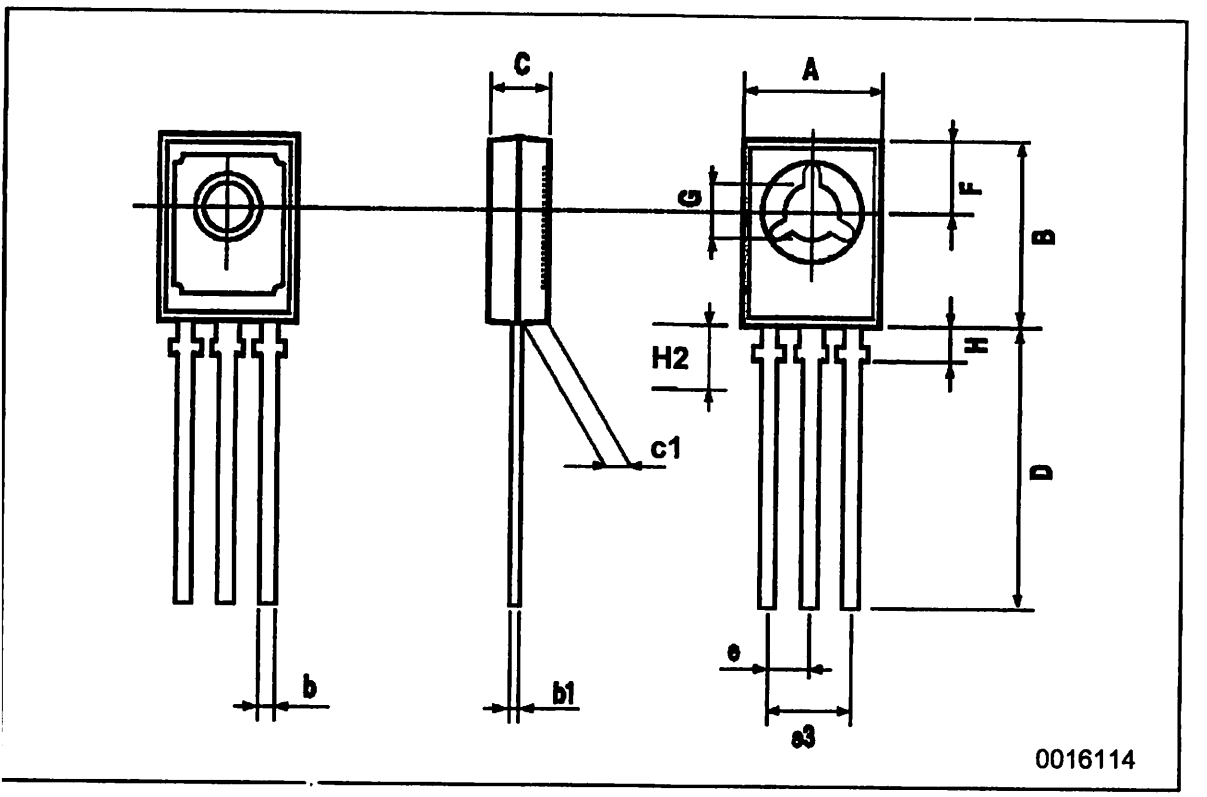
* Pulsed: Pulse duration = 300 µs, duty cycle 1.5 %

Safe Operating Area



SOT-32 (TO-126) MECHANICAL DATA

DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A	7.4		7.8	0.291		0.307
B	10.5		10.8	0.413		0.445
b	0.7		0.9	0.028		0.035
b1	0.49		0.75	0.019		0.030
C	2.4		2.7	0.040		0.106
c1	1.0		1.3	0.039		0.050
D	15.4		16.0	0.606		0.629
e		2.2			0.087	
e3	4.15		4.65	0.163		0.183
F		3.8			0.150	
G	3		3.2	0.118		0.126
H			2.54			0.100



National Semiconductor

October 2002

ADC0808/ADC0809

8-Bit µP Compatible A/D Converters with 8-Channel Multiplexer

General Description

The ADC0808, ADC0809 data acquisition component is a monolithic CMOS device with an 8-bit analog-to-digital converter, 8-channel multiplexer and microprocessor compatible control logic. The 8-bit A/D converter uses successive approximation as the conversion technique. The converter features a high impedance chopper stabilized comparator, a 256R voltage divider with analog switch tree and a successive approximation register. The 8-channel multiplexer can directly access any of 8-single-ended analog signals.

The device eliminates the need for external zero and full-scale adjustments. Easy interfacing to microprocessors is provided by the latched and decoded multiplexer address inputs and latched TTL TRI-STATE outputs.

The design of the ADC0808, ADC0809 has been optimized by incorporating the most desirable aspects of several A/D conversion techniques. The ADC0808, ADC0809 offers high speed, high accuracy, minimal temperature dependence, excellent long-term accuracy and repeatability, and consumes minimal power. These features make this device ideally suited to applications from process and machine control to consumer and automotive applications. For 16-channel multiplexer with common output (sample/hold port) see ADC0816 data sheet. (See AN-247 for more information.)

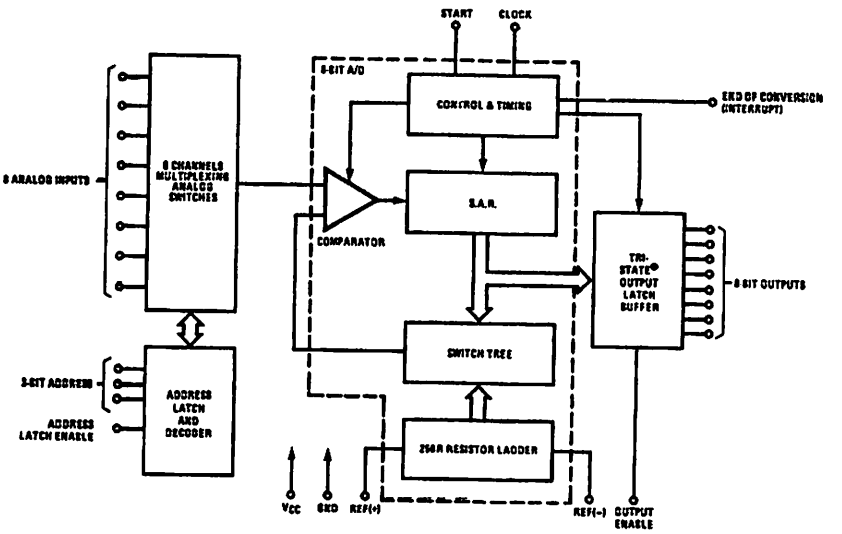
Features

- Easy interface to all microprocessors
- Operates ratiometrically or with 5 V_{DC} or analog span adjusted voltage reference
- No zero or full-scale adjust required
- 8-channel multiplexer with address logic
- 0V to 5V input range with single 5V power supply
- Outputs meet TTL voltage level specifications
- ADC0808 equivalent to MM74C949
- ADC0809 equivalent to MM74C949-1

Key Specifications

■ Resolution	8 Bits
■ Total Unadjusted Error	±½ LSB and ±1 LSB
■ Single Supply	5 V_{DC}
■ Low Power	15 mW
■ Conversion Time	100 µs

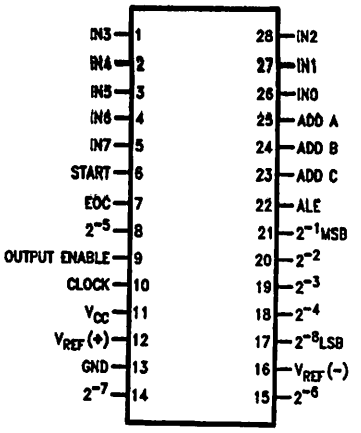
Block Diagram



See Ordering Information

Connection Diagrams

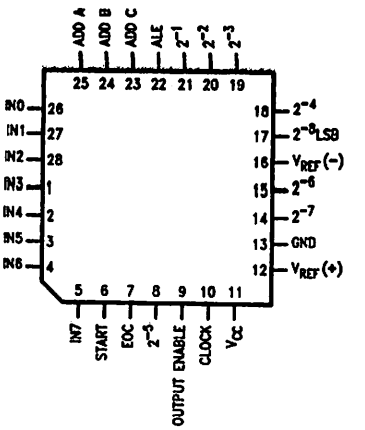
Dual-In-Line Package



00567211

Order Number ADC0808CCN or ADC0809CCN
See NS Package J28A or N28A

Molded Chip Carrier Package



00567212

Order Number ADC0808CCV or ADC0809CCV
See NS Package V28A

Ordering Information

TEMPERATURE RANGE		–40°C to +85°C	
Error	±½ LSB Unadjusted	ADC0808CCN	ADC0808CCV
	±1 LSB Unadjusted	ADC0809CCN	ADC0809CCV
Package Outline		N28A Molded DIP	V28A Molded Chip Carrier

ɔsolute Maximum Ratings (Notes 2,

Military/Aerospace specified devices are required, ase contact the National Semiconductor Sales Office/ tributors for availability and specifications.

pply Voltage (V_{CC}) (Note 3)	6.5V
ltage at Any Pin	−0.3V to (V_{CC}+0.3V)
Except Control Inputs	
ltage at Control Inputs	−0.3V to +15V
START, OE, CLOCK, ALE, ADD A, ADD B, ADD C)	
rage Temperature Range	−65°C to +150°C
ckage Dissipation at T_A=25°C	875 mW
ıd Temp. (Soldering, 10 seconds)	
Dual-In-Line Package (plastic)	260°C
Molded Chip Carrier Package	
Vapor Phase (60 seconds)	215°C
Infrared (15 seconds)	220°C
ESD Susceptibility (Note 8)	400V

Operating Conditions (Notes 1, 2)

Temperature Range (Note 1)	$T_{MIN} \le T_A \le T_{MAX}$
ADC0808CCN,ADC0809CCN	−40°C≤T_A≤+85°C
ADC0808CCV, ADC0809CCV	−40°C≤T_A≤+85°C
Range of V_{CC} (Note 1)	4.5 V_{DC} to 6.0 V_{DC}

ɛctrical Characteristics

ıverter Specifications: V_{CC}=5 V_{DC}=V_{REF+}, $V_{REF(-)}$=GND, $T_{MIN} \le T_A \le T_{MAX}$ and f_{CLK}=640 kHz unless otherwise stated.

Symbol	Parameter	Conditions	Min	Typ	Max	Units
	ADC0808					
	Total Unadjusted Error	25°C			±½	LSB
	(Note 5)	T_{MIN} to T_{MAX}			±¾	LSB
	ADC0809					
	Total Unadjusted Error	0°C to 70°C			±1	LSB
	(Note 5)	T_{MIN} to T_{MAX}			±1¼	LSB
	Input Resistance	From Ref(+) to Ref(−)	1.0	2.5		kΩ
	Analog Input Voltage Range	(Note 4) V(+) or V(−)	GND−0.10		V_{CC}+0.10	V_{DC}
)	Voltage, Top of Ladder	Measured at Ref(+)		V_{CC}	V_{CC}+0.1	V
$\frac{V_{REF(+)}+V_{REF(-)}}{2}$	Voltage, Center of Ladder		V_{CC}/2-0.1	V_{CC}/2	V_{CC}/2+0.1	V
)	Voltage, Bottom of Ladder	Measured at Ref(-)	−0.1	0		V
	Comparator Input Current	f_c=640 kHz, (Note 6)	−2	±0.5	2	µA

ɛctrical Characteristics

al Levels and DC Specifications: ADC0808CCN, ADC0808CCV, ADC0809CCN and ADC0809CCV, 4.75≤V_{CC}≤5.25V, C≤T_A≤+85°C unless otherwise noted

nbol	Parameter	Conditions	Min	Typ	Max	Units
G MULTIPLEXER						
	OFF Channel Leakage Current	V_{CC}=5V, V_{IN}=5V,				
		T_A=25°C		10	200	nA
		T_{MIN} to T_{MAX}			1.0	µA
	OFF Channel Leakage Current	V_{CC}=5V, V_{IN}=0,				
		T_A=25°C	−200	−10		nA
		T_{MIN} to T_{MAX}	−1.0			µA
OL INPUTS						
	Logical "1" Input Voltage		V_{CC}−1.5			V
	Logical "0" Input Voltage				1.5	V
	Logical "1" Input Current (The Control Inputs)	V_{IN}=15V			1.0	µA
	Logical "0" Input Current (The Control Inputs)	V_{IN}=0	−1.0			µA
	Supply Current	f_{CLK}=640 kHz		0.3	3.0	mA

Electrical Characteristics (Continued)

Digital Levels and DC Specifications: ADC0808CCN, ADC0808CCV, ADC0809CCN and ADC0809CCV, $4.75 \le V_{CC} \le 5.25V$, $-40°C \le T_A \le +85°C$ unless otherwise noted

Symbol	Parameter	Conditions	Min	Typ	Max	Units
DATA OUTPUTS AND EOC (INTERRUPT)						
$V_{OUT(1)}$	Logical "1" Output Voltage	V_{CC} = 4.75V I_{OUT} = −360µA I_{OUT} = −10µA		 2.4 4.5		 V(min) V(min)
$V_{OUT(0)}$	Logical "0" Output Voltage	I_O=1.6 mA			0.45	V
$V_{OUT(0)}$	Logical "0" Output Voltage EOC	I_O=1.2 mA			0.45	V
I_{OUT}	TRI-STATE Output Current	V_O=5V V_O=0	 −3		3	µA µA

Electrical Characteristics

Timing Specifications $V_{CC}=V_{REF(+)}=5V$, $V_{REF(-)}=GND$, $t_r=t_f=20$ ns and $T_A=25°C$ unless otherwise noted.

Symbol	Parameter	Conditions	Min	Typ	Max	Units
t_{WS}	Minimum Start Pulse Width	(*Figure 5*)		100	200	ns
t_{WALE}	Minimum ALE Pulse Width	(*Figure 5*)		100	200	ns
t_S	Minimum Address Set-Up Time	(*Figure 5*)		25	50	ns
t_H	Minimum Address Hold Time	(*Figure 5*)		25	50	ns
t_D	Analog MUX Delay Time From ALE	R_S=0Ω (*Figure 5*)		1	2.5	µs
t_{H1}, t_{H0}	OE Control to Q Logic State	C_L=50 pF, R_L=10k (*Figure 8*)		125	250	ns
t_{1H}, t_{0H}	OE Control to Hi-Z	C_L=10 pF, R_L=10k (*Figure 8*)		125	250	ns
t_c	Conversion Time	f_c=640 kHz, (*Figure 5*) (Note 7)	90	100	116	µs
f_c	Clock Frequency		10	640	1280	kHz
t_{EOC}	EOC Delay Time	(*Figure 5*)	0		8+2 µS	Clock Periods
C_{IN}	Input Capacitance	At Control Inputs		10	15	pF
C_{OUT}	TRI-STATE Output Capacitance	At TRI-STATE Outputs		10	15	pF

Note 1: Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. DC and AC electrical specifications do not apply when operating the device beyond its specified operating conditions.

Note 2: All voltages are measured with respect to GND, unless otherwise specified.

Note 3: A zener diode exists, internally, from V_{CC} to GND and has a typical breakdown voltage of 7 V_{DC}.

Note 4: Two on-chip diodes are tied to each analog input which will forward conduct for analog input voltages one diode drop below ground or one diode drop greater than the V_{CC}n supply. The spec allows 100 mV forward bias of either diode. This means that as long as the analog V_{IN} does not exceed the supply voltage by more than 100 mV, the output code will be correct. To achieve an absolute $0V_{DC}$ to $5V_{DC}$ input voltage range will therefore require a minimum supply voltage of 4.900 V_{DC} over temperature variations, initial tolerance and loading.

Note 5: Total unadjusted error includes offset, full-scale, linearity, and multiplexer errors. See *Figure 3*. None of these A/Ds requires a zero or full-scale adjust. However, if an all zero code is desired for an analog input other than 0.0V, or if a narrow full-scale span exists (for example: 0.5V to 4.5V full-scale) the reference voltages can be adjusted to achieve this. See *Figure 13*.

Note 6: Comparator input current is a bias current into or out of the chopper stabilized comparator. The bias current varies directly with clock frequency and has little temperature dependence (*Figure 6*). See paragraph 4.0.

Note 7: The outputs of the data register are updated one clock cycle before the rising edge of EOC.

Note 8: Human body model, 100 pF discharged through a 1.5 kΩ resistor.

nctional Description

ıplexer. The device contains an 8-channel single-ended ɔg signal multiplexer. A particular input channel is se-ıd by using the address decoder. *Table 1* shows the input ıs for the address lines to select any channel. The ess is latched into the decoder on the low-to-high tran-ı of the address latch enable signal.

TABLE 1.

SELECTED	ADDRESS LINE		
ANALOG CHANNEL	C	B	A
IN0	L	L	L
IN1	L	L	H
IN2	L	H	L
IN3	L	H	H
IN4	H	L	L
IN5	H	L	H
IN6	H	H	L
IN7	H	H	H

IVERTER CHARACTERISTICS

Converter

heart of this single chip data acquisition system is its analog-to-digital converter. The converter is designed to fast, accurate, and repeatable conversions over a wide e of temperatures. The converter is partitioned into 3 r sections: the 256R ladder network, the successive ɔximation register, and the comparator. The converter's ıl outputs are positive true.

256R ladder network approach (*Figure 1*) was chosen the conventional R/2R ladder because of its inherent ɔtonicity, which guarantees no missing digital codes. ɔtonicity is particularly important in closed loop feedback ol systems. A non-monotonic relationship can cause ations that will be catastrophic for the system. Addition-he 256R network does not cause load variations on the ence voltage.

The bottom resistor and the top resistor of the ladder network in *Figure 1* are not the same value as the remainder of the network. The difference in these resistors causes the output characteristic to be symmetrical with the zero and full-scale points of the transfer curve. The first output transition occurs when the analog signal has reached +½ LSB and succeeding output transitions occur every 1 LSB later up to full-scale.

The successive approximation register (SAR) performs 8 iterations to approximate the input voltage. For any SAR type converter, n-iterations are required for an n-bit converter. *Figure 2* shows a typical example of a 3-bit converter. In the ADC0808, ADC0809, the approximation technique is extended to 8 bits using the 256R network.

The A/D converter's successive approximation register (SAR) is reset on the positive edge of the start conversion start pulse. The conversion is begun on the falling edge of the start conversion pulse. A conversion in process will be interrupted by receipt of a new start conversion pulse. Continuous conversion may be accomplished by tying the end-of-conversion (EOC) output to the SC input. If used in this mode, an external start conversion pulse should be applied after power up. End-of-conversion will go low between 0 and 8 clock pulses after the rising edge of start conversion.

The most important section of the A/D converter is the comparator. It is this section which is responsible for the ultimate accuracy of the entire converter. It is also the comparator drift which has the greatest influence on the repeatability of the device. A chopper-stabilized comparator provides the most effective method of satisfying all the converter requirements.

The chopper-stabilized comparator converts the DC input signal into an AC signal. This signal is then fed through a high gain AC amplifier and has the DC level restored. This technique limits the drift component of the amplifier since the drift is a DC component which is not passed by the AC amplifier. This makes the entire A/D converter extremely insensitive to temperature, long term drift and input offset errors.

Figure 4 shows a typical error curve for the ADC0808 as measured using the procedures outlined in AN-179.

Functional Description (Continued)

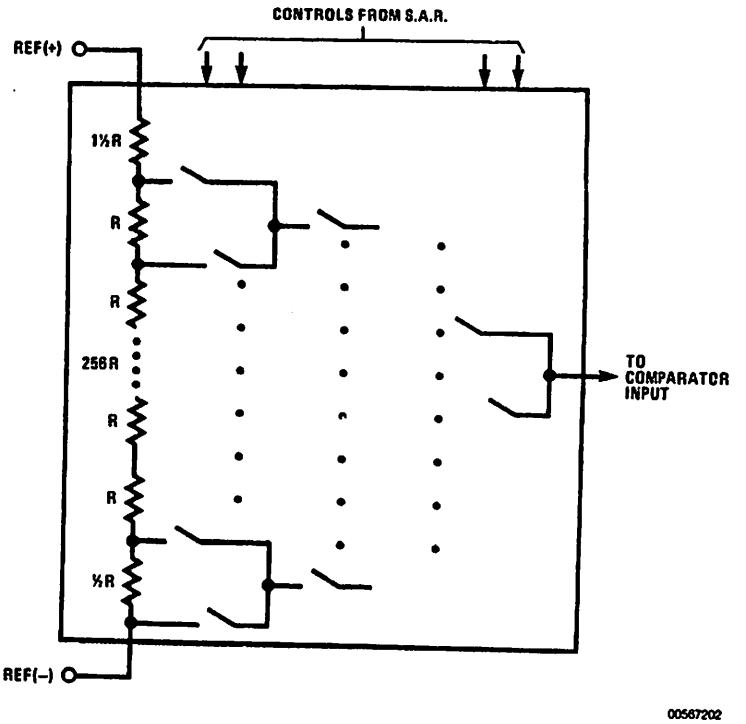


FIGURE 1. Resistor Ladder and Switch Tree

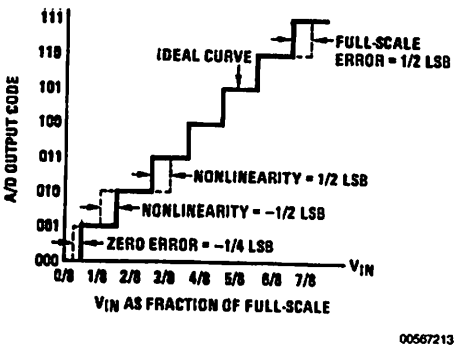


FIGURE 2. 3-Bit A/D Transfer Curve

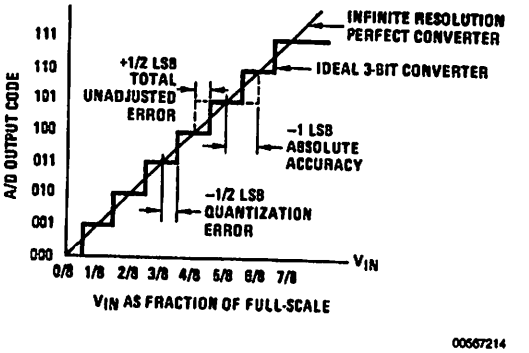


FIGURE 3. 3-Bit A/D Absolute Accuracy Curve

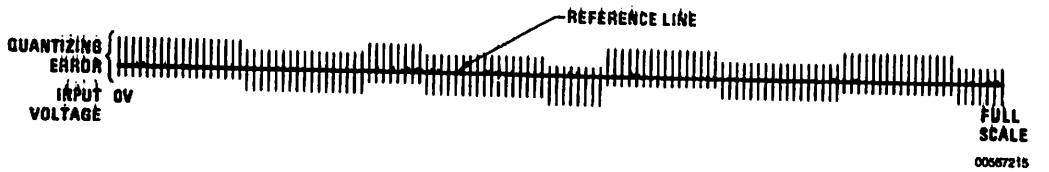


FIGURE 4. Typical Error Curve

iming Diagram

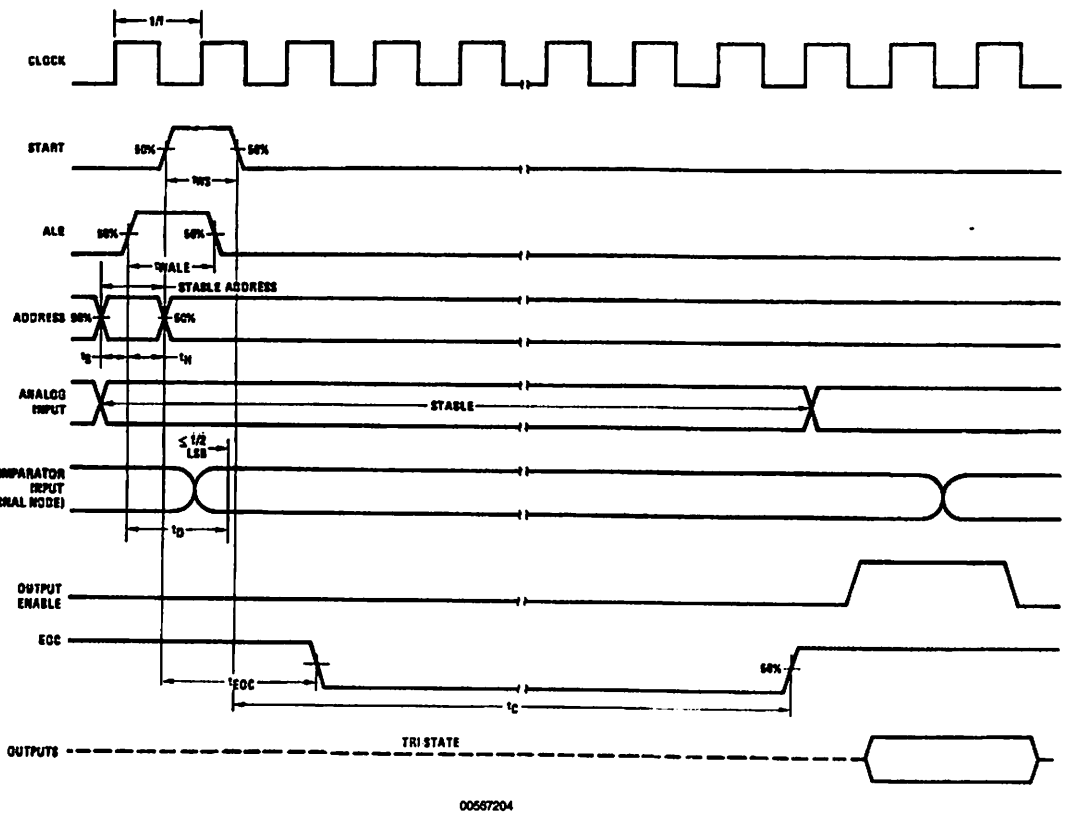


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FIGURE 5.

Typical Performance Characteristics

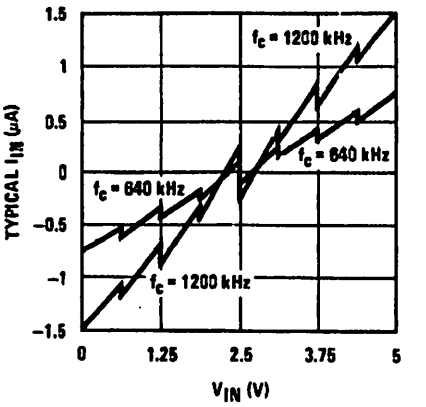


FIGURE 6. Comparator I_{IN} vs V_{IN} (V_{CC}=V_{REF}=5V)

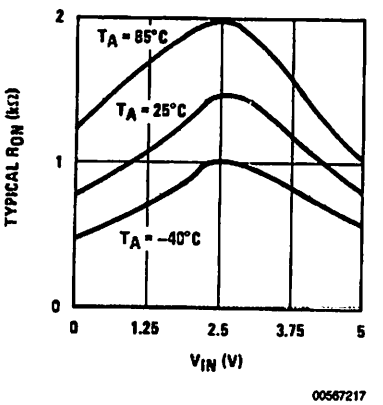


FIGURE 7. Multiplexer R_{ON} vs V_{IN} (V_{CC}=V_{REF}=5V)

I-STATE Test Circuits and ıing Diagrams

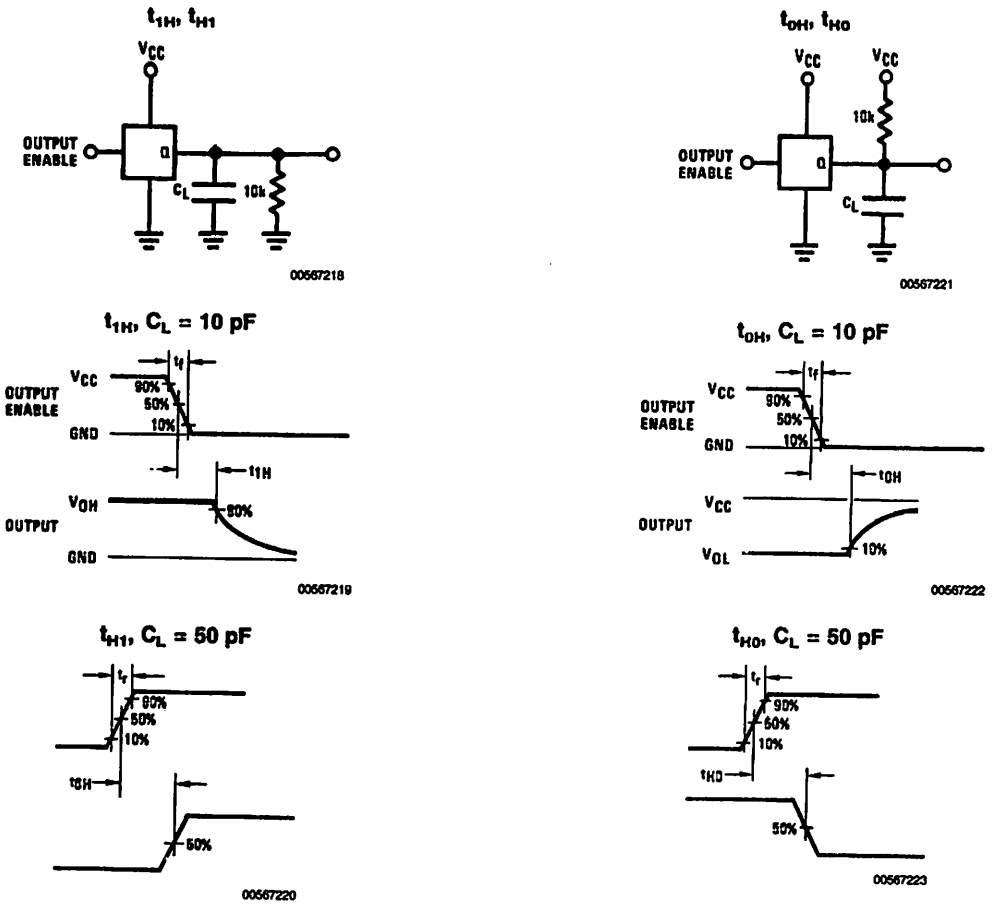


FIGURE 8.

lications Information

ATION

ITIOMETRIC CONVERSION

)C0808, ADC0809 is designed as a complete Data ition System (DAS) for ratiometric conversion sys- In ratiometric systems, the physical variable being red is expressed as a percentage of full-scale which is :essarily related to an absolute standard. The voltage) the ADC0808 is expressed by the equation

$$\frac{V_{IN}}{V_{fs}-V_Z} = \frac{D_X}{D_{MAX}-D_{MIN}} \quad (1)$$

Input voltage into the ADC0808
Full-scale voltage
Zero voltage
Data point being measured
=Maximum data limit
D_{MIN}=Minimum data limit

A good example of a ratiometric transducer is a potentiometer used as a position sensor. The position of the wiper is directly proportional to the output voltage which is a ratio of the full-scale voltage across it. Since the data is represented as a proportion of full-scale, reference requirements are greatly reduced, eliminating a large source of error and cost for many applications. A major advantage of the ADC0808, ADC0809 is that the input voltage range is equal to the supply range so the transducers can be connected directly across the supply and their outputs connected directly into the multiplexer inputs, (*Figure 9*).

Ratiometric transducers such as potentiometers, strain gauges, thermistor bridges, pressure transducers, etc., are suitable for measuring proportional relationships; however, many types of measurements must be referred to an absolute standard such as voltage or current. This means a system reference must be used which relates the full-scale voltage to the standard volt. For example, if $V_{CC}=V_{REF}=5.12V$, then the full-scale range is divided into 256 standard steps. The smallest standard step is 1 LSB which is then 20 mV.

Applications Information (Continued)

2.0 RESISTOR LADDER LIMITATIONS

The voltages from the resistor ladder are compared to the selected into 8 times in a conversion. These voltages are coupled to the comparator via an analog switch tree which is referenced to the supply. The voltages at the top, center and bottom of the ladder must be controlled to maintain proper operation.

The top of the ladder, Ref(+), should not be more positive than the supply, and the bottom of the ladder, Ref(−), should not be more negative than ground. The center of the ladder voltage must also be near the center of the supply because the analog switch tree changes from N-channel switches to P-channel switches. These limitations are automatically satisfied in ratiometric systems and can be easily met in ground referenced systems.

Figure 10 shows a ground referenced system with a separate supply and reference. In this system, the supply must be trimmed to match the reference voltage. For instance, if a 5.12V is used, the supply should be adjusted to the same voltage within 0.1V.

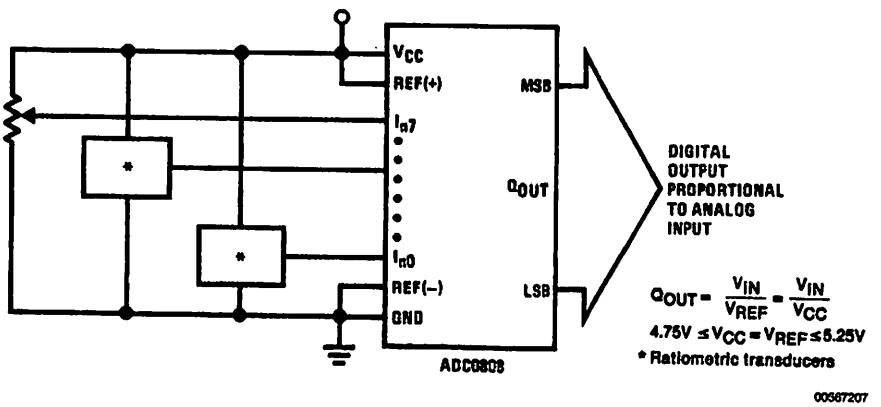
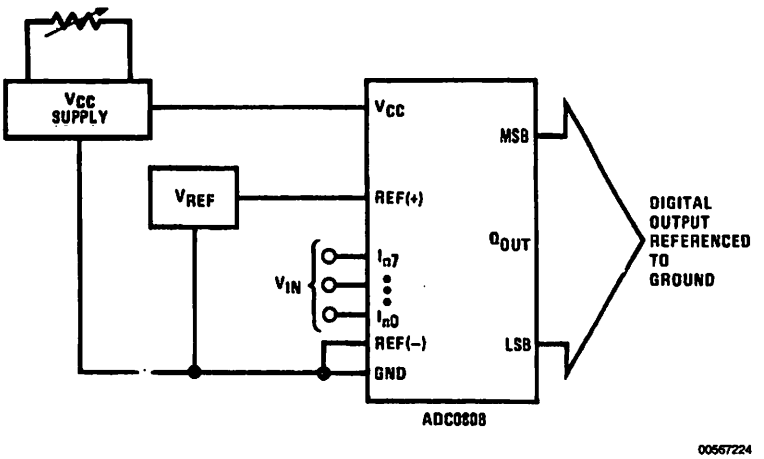


FIGURE 9. Ratiometric Conversion System

The ADC0808 needs less than a milliamp of supply current so developing the supply from the reference is readily accomplished. In *Figure 11* a ground referenced system is shown which generates the supply from the reference. The buffer shown can be an op amp of sufficient drive to supply the milliamp of supply current and the desired bus drive, or if a capacitive bus is driven by the outputs a large capacitor will supply the transient supply current as seen in *Figure 12*. The LM301 is overcompensated to insure stability when loaded by the 10 µF output capacitor.

The top and bottom ladder voltages cannot exceed V_{CC} and ground, respectively, but they can be symmetrically less than V_{CC} and greater than ground. The center of the ladder voltage should always be near the center of the supply. The sensitivity of the converter can be increased, (i.e., size of the LSB steps decreased) by using a symmetrical reference system. In *Figure 13*, a 2.5V reference is symmetrically centered about $V_{CC}/2$ since the same current flows in identical resistors. This system with a 2.5V reference allows the LSB bit to be half the size of a 5V reference system.

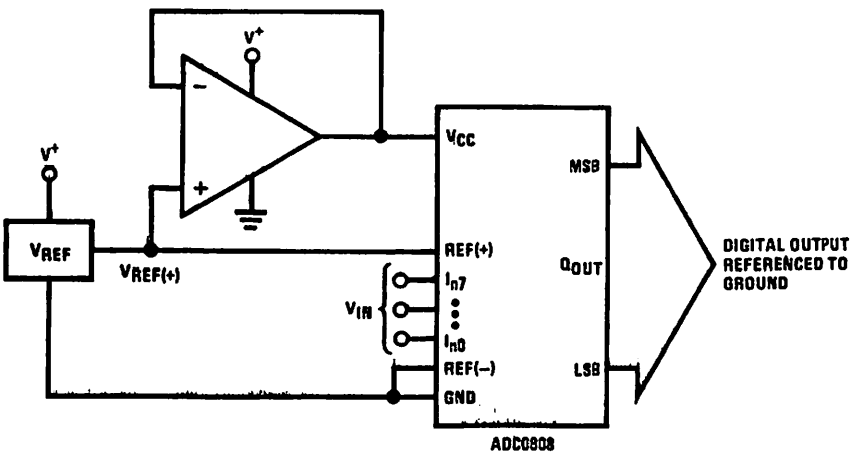
plications Information (Continued)



$$Q_{OUT} = \frac{V_{IN}}{V_{REF}}$$

$4.75V \leq V_{CC} = V_{REF} \leq 5.25V$

FIGURE 10. Ground Referenced Conversion System Using Trimmed Supply



$$Q_{OUT} = \frac{V_{IN}}{V_{REF}}$$

$4.75V \leq V_{CC} = V_{REF} \leq 5.25V$

FIGURE 11. Ground Referenced Conversion System with Reference Generating V_{CC} Supply

Applications Information (Continued)

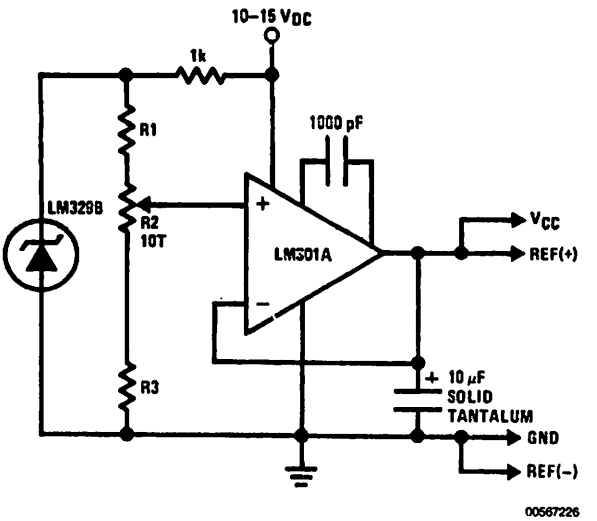
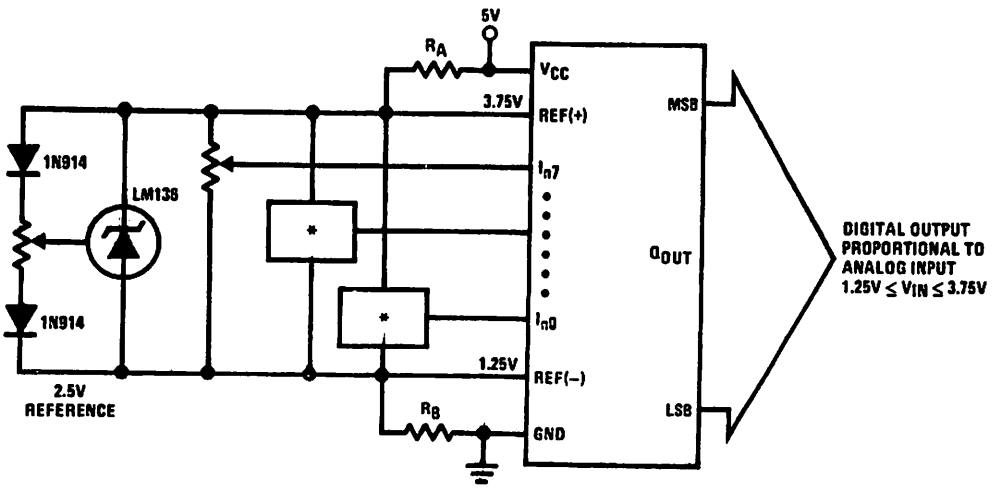


FIGURE 12. Typical Reference and Supply Circuit



$R_A = R_B$

*Ratiometric transducers

FIGURE 13. Symmetrically Centered Reference

3.0 CONVERTER EQUATIONS

The transition between adjacent codes N and N+1 is given by:

$$V_{IN} = \left\{(V_{REF(+)} - V_{REF(-)})\left[\frac{N}{256} + \frac{1}{512}\right] \pm V_{TUE}\right\} + V_{REF(-)} \quad (2)$$

The center of an output code N is given by:

$$V_{IN}\left\{(V_{REF(+)} - V_{REF(-)})\left[\frac{N}{256}\right] \pm V_{TUE}\right\} + V_{REF(-)} \quad (3)$$

The output code N for an arbitrary input are the integers within the range:

$$N = \frac{V_{IN} - V_{REF(-)}}{V_{REF(+)} - V_{REF(-)}} \times 256 \pm \text{Absolute Accuracy} \quad (4)$$

Where: V_{IN}=Voltage at comparator input

$V_{REF(+)}$=Voltage at Ref(+)

$V_{REF(-)}$=Voltage at Ref(–)

V_{TUE}=Total unadjusted error voltage (typically $V_{REF(+)} \div 512$)

pplications Information (Continued)

ANALOG COMPARATOR INPUTS

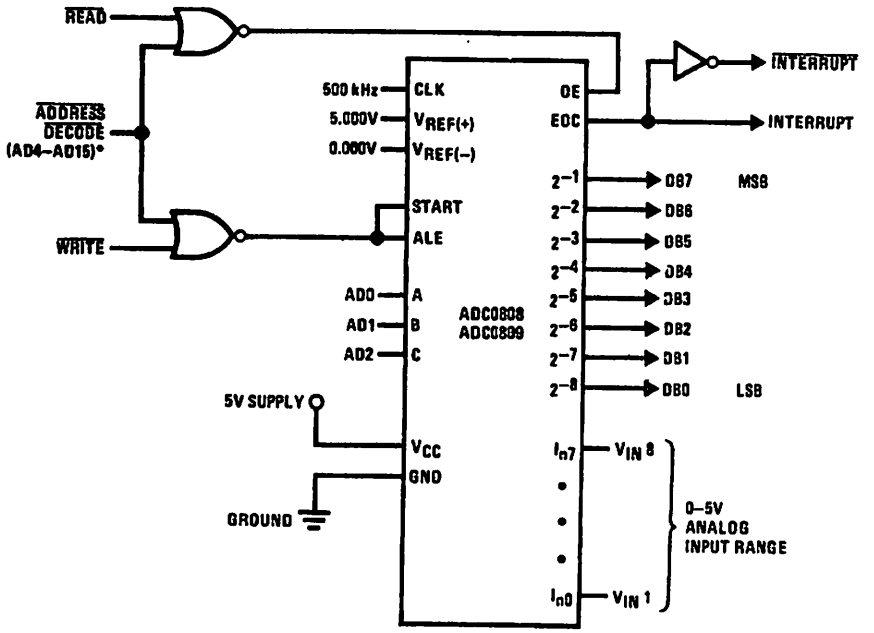
dynamic comparator input current is caused by the lodic switching of on-chip stray capacitances. These are inected alternately to the output of the resistor ladder/ tch tree network and to the comparator input as part of operation of the chopper stabilized comparator.

average value of the comparator input current varies ictly with clock frequency and with V_{IN} as shown in *ure 6.*

If no filter capacitors are used at the analog inputs and the signal source impedances are low, the comparator input current should not introduce converter errors, as the transient created by the capacitance discharge will die out before the comparator output is strobed.

If input filter capacitors are desired for noise reduction and signal conditioning they will tend to average out the dynamic comparator input current. It will then take on the characteristics of a DC bias current whose effect can be predicted conventionally.

ypical Application



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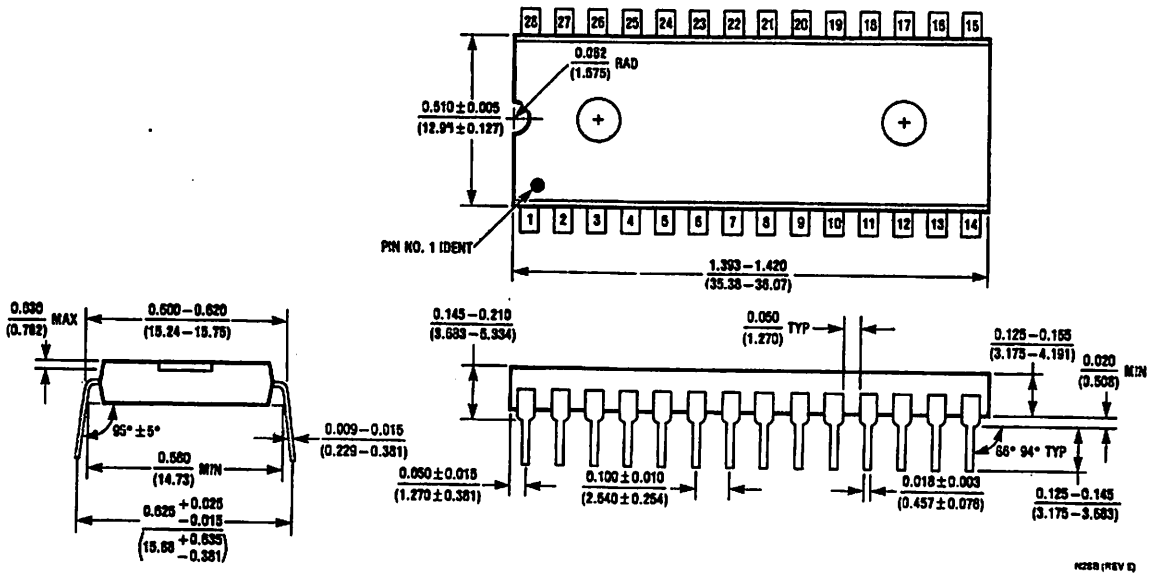
ress latches needed for 8085 and SC/MP interfacing the ADC0808 to a microprocessor

TABLE 2. Microprocessor Interface Table

PROCESSOR	$\overline{\text{READ}}$	$\overline{\text{WRITE}}$	INTERRUPT (COMMENT)
8080	$\overline{\text{MEMR}}$	$\overline{\text{MEMW}}$	INTR (Thru RST Circuit)
8085	$\overline{\text{RD}}$	$\overline{\text{WR}}$	INTR (Thru RST Circuit)
Z-80	$\overline{\text{RD}}$	$\overline{\text{WR}}$	$\overline{\text{INT}}$ (Thru RST Circuit, Mode 0)
SC/MP	NRDS	NWDS	SA (Thru Sense A)
6800	VMA•φ2•R/W	VMA•φ•$\overline{\text{R/W}}$	$\overline{\text{IRQA}}$ or $\overline{\text{IRQB}}$ (Thru PIA)

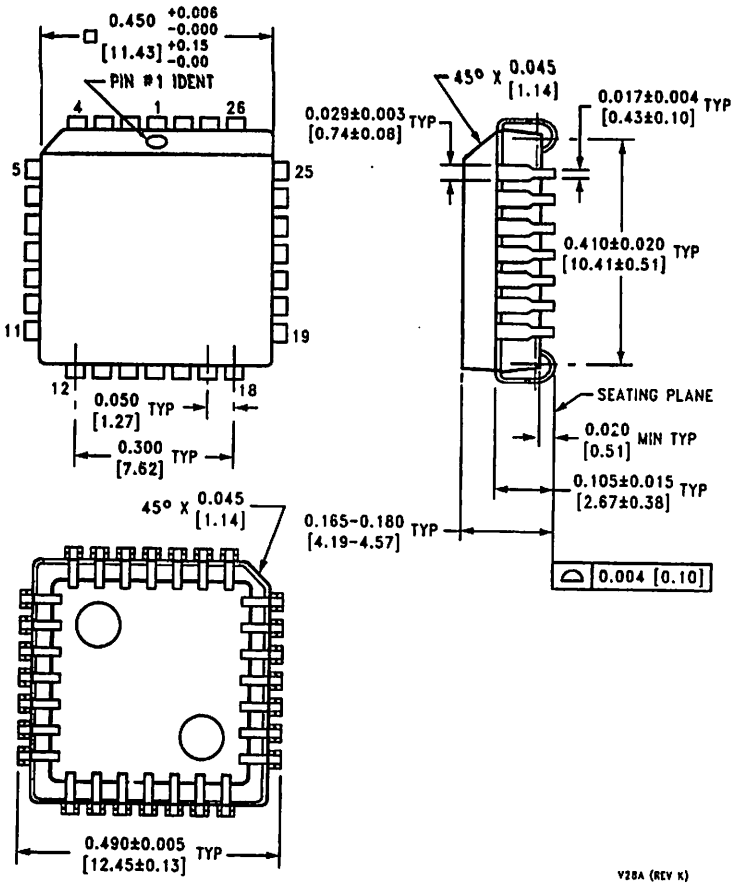
Physical Dimensions inches (millimeters)

unless otherwise noted



Molded Dual-In-Line Package (N)
Order Number ADC0808CCN or ADC0809CCN
NS Package Number N28B

ysical Dimensions Inches (millimeters) unless otherwise noted (Continued)



Molded Chip Carrier (V)
Order Number ADC0808CCV or ADC0809CCV
NS Package Number V28A

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support devices or systems are devices or tems which, (a) are intended for surgical implant the body, or (b) support or sustain life, and se failure to perform when properly used in ordance with instructions for use provided in the ling, can be reasonably expected to result in a ificant injury to the user.

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National Semiconductor
Europe
Fax: +49 (0) 180-530 85 86
Email: europe.support@nsc.com
Deutsch Tel: +49 (0) 69 9508 6208
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National Semiconductor

February 2000

LM555
Timer

General Description

The LM555 is a highly stable device for generating accurate time delays or oscillation. Additional terminals are provided for triggering or resetting if desired. In the time delay mode of operation, the time is precisely controlled by one external resistor and capacitor. For astable operation as an oscillator, the free running frequency and duty cycle are accurately controlled with two external resistors and one capacitor. The circuit may be triggered and reset on falling waveforms, and the output circuit can source or sink up to 200mA or drive TTL circuits.

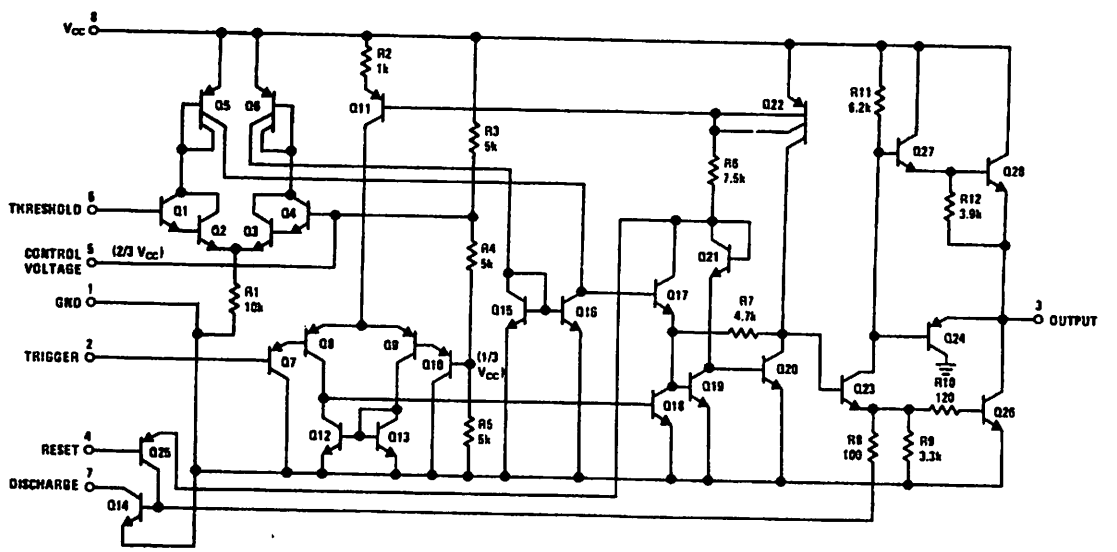
Features

- Direct replacement for SE555/NE555
- Timing from microseconds through hours
- Operates in both astable and monostable modes
- Adjustable duty cycle
- Output can source or sink 200 mA
- Output and supply TTL compatible
- Temperature stability better than 0.005% per °C
- Normally on and normally off output
- Available in 8-pin MSOP package

Applications

- Precision timing
- Pulse generation
- Sequential timing
- Time delay generation
- Pulse width modulation
- Pulse position modulation
- Linear ramp generator

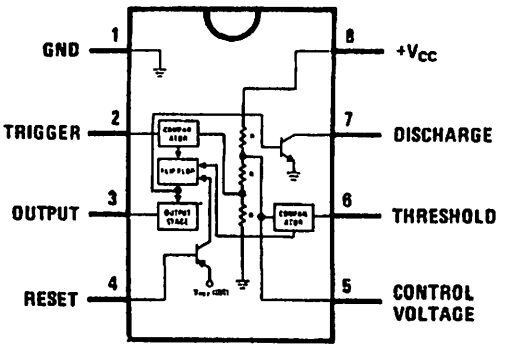
Schematic Diagram



DS007851-1

Connection Diagram

Dual-In-Line, Small Outline and Molded Mini Small Outline Packages



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Top View

Ordering Information

Package	Part Number	Package Marking	Media Transport	NSC Drawing
8-Pin SOIC	LM555CM	LM555CM	Rails	M08A
	LM555CMX	LM555CM	2.5k Units Tape and Reel	
8-Pin MSOP	LM555CMM	Z55	1k Units Tape and Reel	MUA08A
	LM555CMMX	Z55	3.5k Units Tape and Reel	
8-Pin MDIP	LM555CN	LM555CN	Rails	N08E

ɔsolute Maximum Ratings (Note 2)

Military/Aerospace specified devices are required, ıse contact the National Semiconductor Sales Office/ tributors for availability and specifications.

ɔply Voltage	+18V
ver Dissipation (Note 3)	
M555CM, LM555CN	1180 mW
M555CMM	613 mW
ırating Temperature Ranges	
M555C	0°C to +70°C
age Temperature Range	−65°C to +150°C

Soldering Information

Dual-In-Line Package	
Soldering (10 Seconds)	260°C
Small Outline Packages	
(SOIC and MSOP)	
Vapor Phase (60 Seconds)	215°C
Infrared (15 Seconds)	220°C

See AN-450 "Surface Mounting Methods and Their Effect on Product Reliability" for other methods of soldering surface mount devices.

ɔctrical Characteristics (Notes 1, 2)

T_A = 25°C, V_{CC} = +5V to +15V, unless othewise specified)

Parameter	Conditions	Limits			Units
		LM555C			
		Min	Typ	Max	
ɔply Voltage		4.5		16	V
Supply Current	V_{CC} = 5V, R_L = ∞		3	6	mA
	V_{CC} = 15V, R_L = ∞ (Low State) (Note 4)		10	15	mA
ing Error, Monostable					
itial Accuracy			1		%
rift with Temperature	R_A = 1k to 100kΩ, C = 0.1µF, (Note 5)		50		ppm/°C
ccuracy over Temperature			1.5		%
rift with Supply			0.1		%/V
ng Error, Astable					
itial Accuracy			2.25		%
rift with Temperature	R_A, R_B = 1k to 100kΩ, C = 0.1µF, (Note 5)		150		ppm/°C
ccuracy over Temperature			3.0		%
ift with Supply			0.30		%/V
shold Voltage			0.667		x V_{CC}
ger Voltage	V_{CC} = 15V		5		V
	V_{CC} = 5V		1.67		V
ger Current			0.5	0.9	µA
t Voltage		0.4	0.5	1	V
t Current			0.1	0.4	mA
shold Current	(Note 6)		0.1	0.25	µA
Control Voltage Level	V_{CC} = 15V	9	10	11	V
	V_{CC} = 5V	2.6	3.33	4	V
' Leakage Output High			1	100	nA
' Sat (Note 7)					
tput Low	V_{CC} = 15V, I_7 = 15mA		180		mV
tput Low	V_{CC} = 4.5V, I_7 = 4.5mA		80	200	mV

Electrical Characteristics (Notes 1, 2) (Continued)

(T_A = 25°C, V_{CC} = +5V to +15V, unless otherwise specified)

Parameter	Conditions	Limits			Units
		LM555C			
		Min	Typ	Max	
Output Voltage Drop (Low)	V_{CC} = 15V				
	I_{SINK} = 10mA		0.1	0.25	V
	I_{SINK} = 50mA		0.4	0.75	V
	I_{SINK} = 100mA		2	2.5	V
	I_{SINK} = 200mA		2.5		V
	V_{CC} = 5V				
	I_{SINK} = 8mA				V
	I_{SINK} = 5mA		0.25	0.35	V
Output Voltage Drop (High)	I_{SOURCE} = 200mA, V_{CC} = 15V		12.5		V
	I_{SOURCE} = 100mA, V_{CC} = 15V	12.75	13.3		V
	V_{CC} = 5V	2.75	3.3		V
Rise Time of Output			100		ns
Fall Time of Output			100		ns

Note 1: All voltages are measured with respect to the ground pin, unless otherwise specified.

Note 2: Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is functional, but do not guarantee specific performance limits. Electrical Characteristics state DC and AC electrical specifications under particular test conditions which guarantee specific performance limits. This assumes that the device is within the Operating Ratings. Specifications are not guaranteed for parameters where no limit is given, however, the typical value is a good indication of device performance.

Note 3: For operating at elevated temperatures the device must be derated above 25°C based on a +150°C maximum junction temperature and a thermal resistance of 106°C/W (DIP), 170°C/W (S0-8), and 204°C/W (MSOP) junction to ambient.

Note 4: Supply current when output high typically 1 mA less at V_{CC} = 5V.

Note 5: Tested at V_{CC} = 5V and V_{CC} = 15V.

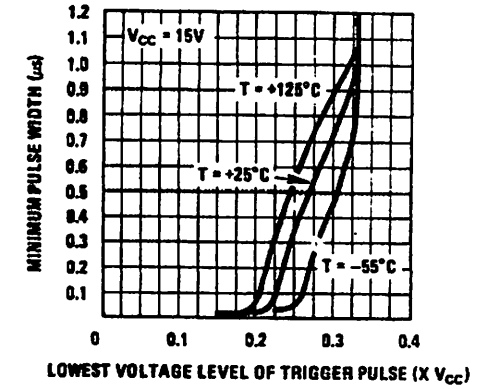
Note 6: This will determine the maximum value of $R_A + R_B$ for 15V operation. The maximum total ($R_A + R_B$) is 20MΩ.

Note 7: No protection against excessive pin 7 current is necessary providing the package dissipation rating will not be exceeded.

Note 8: Refer to RETS555X drawing of military LM555H and LM555J versions for specifications.

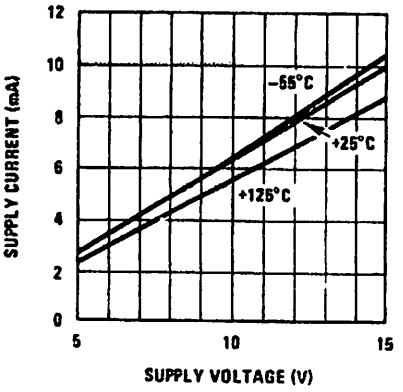
ypical Performance Characteristics

**imuim Pulse Width
quired for Triggering**



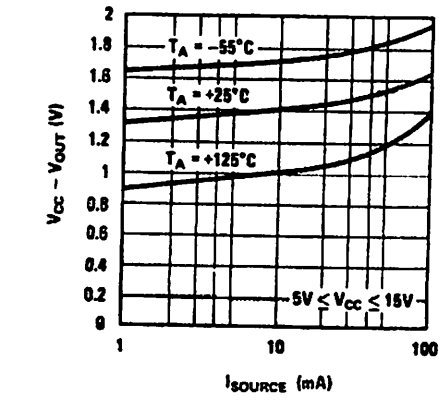
DS007851-4

**Supply Current vs.
Supply Voltage**



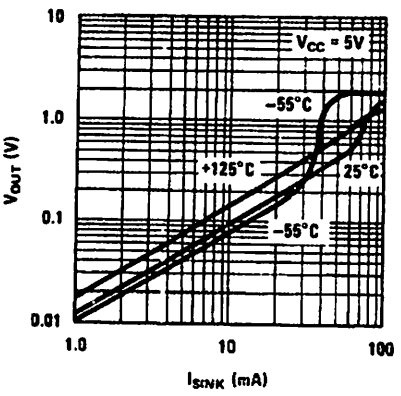
DS007851-19

**h Output Voltage vs.
put Source Current**



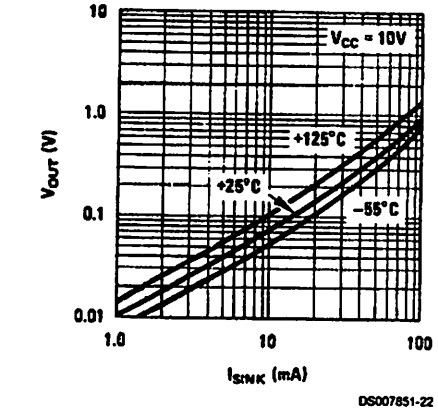
DS007851-20

**Low Output Voltage vs.
Output Sink Current**



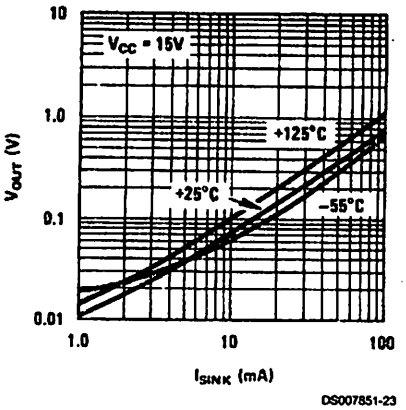
DS007851-21

**Output Voltage vs.
ut Sink Current**



DS007851-22

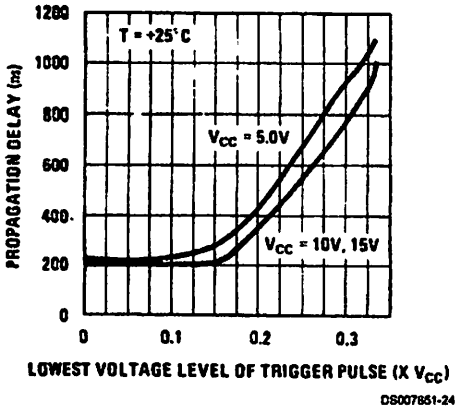
**Low Output Voltage vs.
Output Sink Current**



DS007851-23

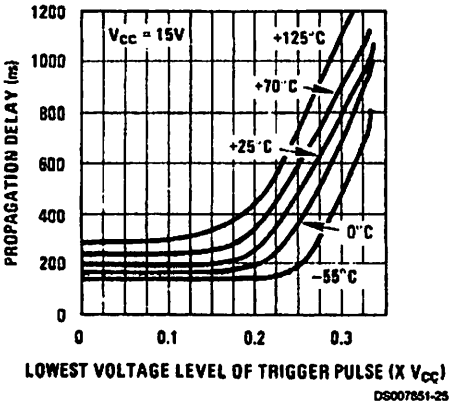
Typical Performance Characteristics (Continued)

Output Propagation Delay vs. Voltage Level of Trigger Pulse



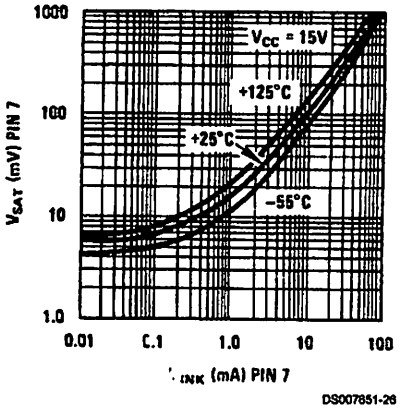
DS007851-24

Output Propagation Delay vs. Voltage Level of Trigger Pulse



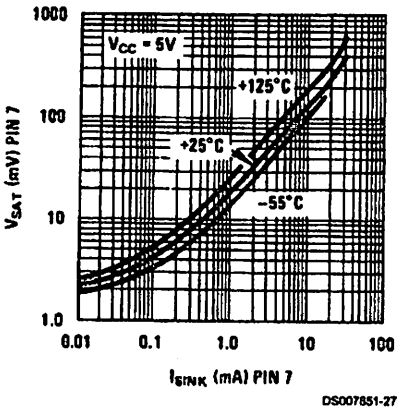
DS007851-25

Discharge Transistor (Pin 7) Voltage vs. Sink Current



DS007851-26

Discharge Transistor (Pin 7) Voltage vs. Sink Current



DS007851-27

ɔlications Information

ɔSTABLE OPERATION

ı mode of operation, the timer functions as a one-shot
'e 1). The external capacitor is initially held discharged
ransistor inside the timer. Upon application of a nega-
igger pulse of less than 1/3 V_{CC} to pin 2, the flip-flop is
ıich both releases the short circuit across the capacitor
rives the output high.

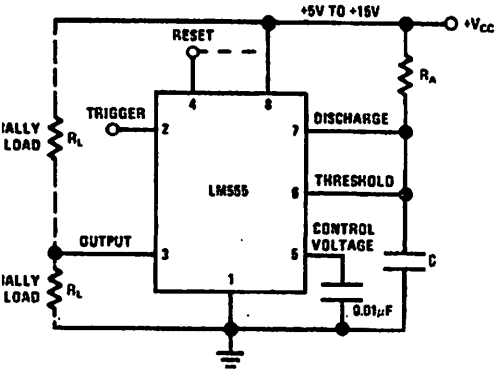
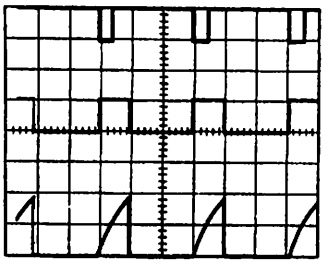


FIGURE 1. Monostable

oltage across the capacitor then increases exponen-
ɔr a period of t = 1.1 R_A C, at the end of which time the
e equals 2/3 V_{CC}. The comparator then resets the
p which in turn discharges the capacitor and drives the
: to its low state. *Figure 2* shows the waveforms gener-
n this mode of operation. Since the charge and the
old level of the comparator are both directly propor-
to supply voltage, the timing internal is independent of
'.



ıV
0.1 ms/DIV.
lkΩ
lµF

Top Trace: Input 5V/Div.
Middle Trace: Output 5V/Div.
Bottom Trace: Capacitor Voltage 2V/Div.

FIGURE 2. Monostable Waveforms

the timing cycle when the output is high, the further
ıtion of a trigger pulse will not effect the circuit so long
trigger input is returned high at least 10µs before the
the timing interval. However the circuit can be reset
this time by the application of a negative pulse to the
ərminal (pin 4). The output will then remain in the low
ntil a trigger pulse is again applied.

ihe reset function is not in use, it is recommended that
ɔnnected to V_{CC} to avoid any possibility of false trig-

3 is a nomograph for easy determination of R, C val-
various time delays.

NOTE: In monostable operation, the trigger should be driven high before the end of timing cycle.

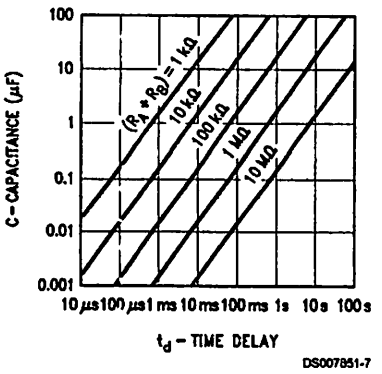


FIGURE 3. Time Delay

ASTABLE OPERATION

If the circuit is connected as shown in *Figure 4* (pins 2 and 6 connected) it will trigger itself and free run as a multivibrator. The external capacitor charges through R_A + R_B and discharges through R_B. Thus the duty cycle may be precisely set by the ratio of these two resistors.

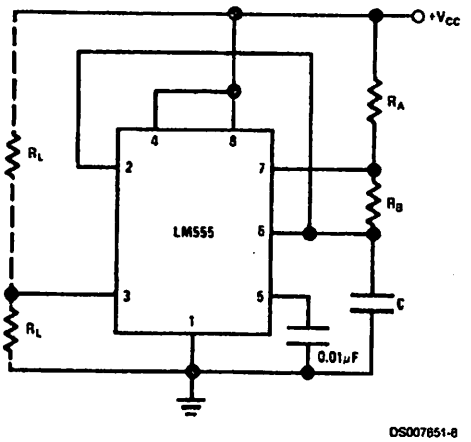
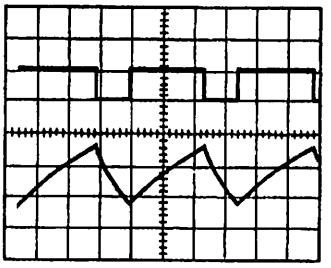


FIGURE 4. Astable

In this mode of operation, the capacitor charges and discharges between 1/3 V_{CC} and 2/3 V_{CC}. As in the triggered mode, the charge and discharge times, and therefore the frequency are independent of the supply voltage.

Applications Information (Continued)

Figure 5 shows the waveforms generated in this mode of operation.



DS007851-9

V_{CC} = 5V Top Trace: Output 5V/Div.
TIME = 20µs/DIV. Bottom Trace: Capacitor Voltage 1V/Div.
R_A = 3.9kΩ
R_B = 3kΩ
C = 0.01µF

FIGURE 5. Astable Waveforms

The charge time (output high) is given by:

$$t_1 = 0.693\ (R_A + R_B)\ C$$

And the discharge time (output low) by:

$$t_2 = 0.693\ (R_B)\ C$$

Thus the total period is:

$$T = t_1 + t_2 = 0.693\ (R_A + 2R_B)\ C$$

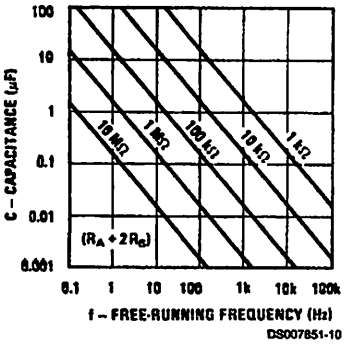
The frequency of oscillation is:

$$f = \frac{1}{T} = \frac{1.44}{(R_A + 2R_B)\ C}$$

Figure 6 may be used for quick determination of these RC values.

The duty cycle is:

$$D = \frac{R_B}{R_A + 2R_B}$$

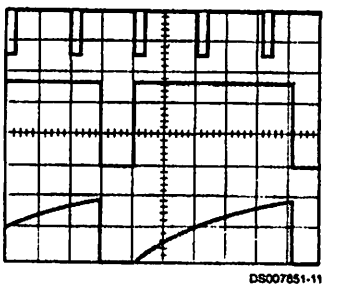


DS007851-10

FIGURE 6. Free Running Frequency

FREQUENCY DIVIDER

The monostable circuit of *Figure 1* can be used as a frequency divider by adjusting the length of the timing cycle. *Figure 7* shows the waveforms generated in a divide by three circuit.



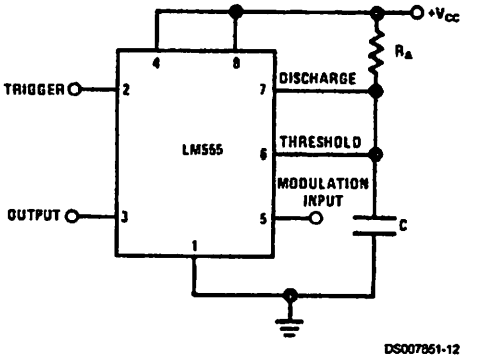
DS007851-11

V_{CC} = 5V Top Trace: Input 4V/Div.
TIME = 20µs/DIV. Middle Trace: Output 2V/Div.
R_A = 9.1kΩ Bottom Trace: Capacitor 2V/Div.
C = 0.01µF

FIGURE 7. Frequency Divider

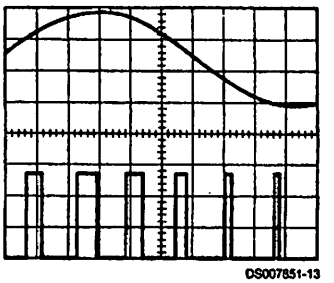
PULSE WIDTH MODULATOR

When the timer is connected in the monostable mode and triggered with a continuous pulse train, the output pulse width can be modulated by a signal applied to pin 5. *Figure 8* shows the circuit, and in *Figure 9* are some waveform examples.



DS007851-12

FIGURE 8. Pulse Width Modulator



DS007851-13

V_{CC} = 5V Top Trace: Modulation 1V/Div.
TIME = 0.2 ms/DIV. Bottom Trace: Output Voltage 2V/Div.
R_A = 9.1kΩ
C = 0.01µF

FIGURE 9. Pulse Width Modulator

›plications Information (Continued)

.SE POSITION MODULATOR

; application uses the timer connected for astable opera-, as in *Figure 10*, with a modulating signal again applied ıe control voltage terminal. The pulse position varies with nodulating signal, since the threshold voltage and hence time delay is varied. *Figure 11* shows the waveforms ərated for a triangle wave modulation signal.

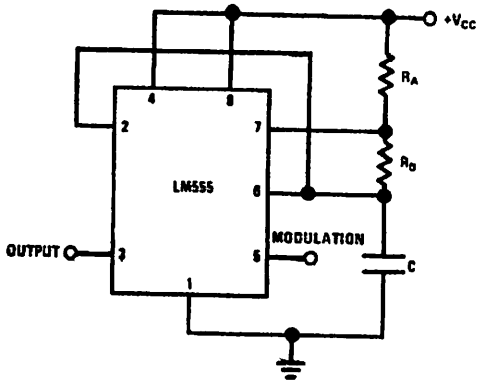
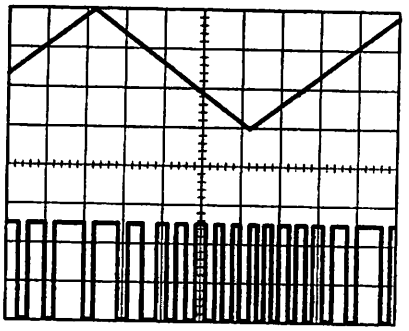


FIGURE 10. Pulse Position Modulator



5V Top Trace: Modulation Input 1V/Div.
0.1 ms/DIV. Bottom Trace: Output 2V/Div.
.9kΩ
kΩ
)1μF

FIGURE 11. Pulse Position Modulator

ıR RAMP

the pullup resistor, R_A, in the monostable circuit is re- l by a constant current source, a linear ramp is gener- *Figure 12* shows a circuit configuration that will perform nction.

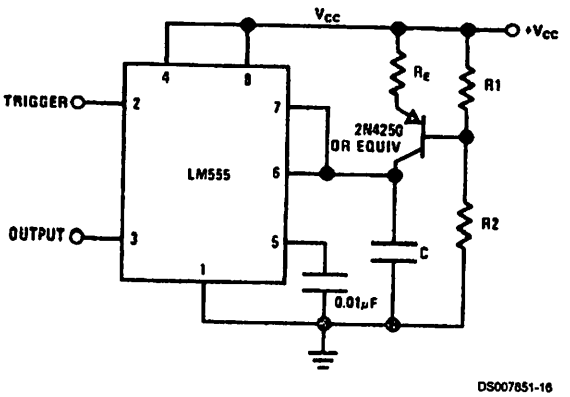


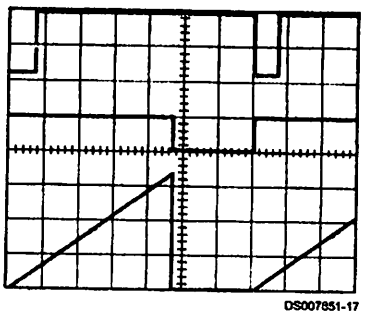
FIGURE 12.

Figure 13 shows waveforms generated by the linear ramp. The time interval is given by:

$$T = \frac{2/3\, V_{CC}\, R_E\, (R_1 + R_2)\, C}{R_1\, V_{CC} - V_{BE}\, (R_1 + R_2)}$$

$$V_{BE} \cong 0.6V$$

$$V_{BE} \simeq 0.6V$$



V_{CC} = 5V Top Trace: Input 3V/Div.
TIME = 20μs/DIV. Middle Trace: Output 5V/Div.
R_1 = 47kΩ Bottom Trace: Capacitor Voltage 1V/Div.
R_2 = 100kΩ
R_E = 2.7 kΩ
C = 0.01 μF

FIGURE 13. Linear Ramp

Applications Information (Continued)

50% DUTY CYCLE OSCILLATOR

For a 50% duty cycle, the resistors R_A and R_B may be connected as in *Figure 14*. The time period for the output high is the same as previous, $t_1 = 0.693\ R_A\ C$. For the output low it is t_2 =

$$\left[(R_A R_B)/(R_A + R_B)\right] C\ ln\left[\frac{R_B - 2R_A}{2R_B - R_A}\right]$$

Thus the frequency of oscillation is

$$f = \frac{1}{t_1 + t_2}$$

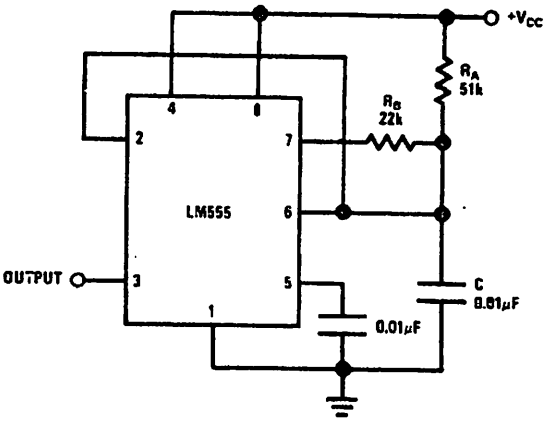


FIGURE 14. 50% Duty Cycle Oscillator

Note that this circuit will not oscillate if R_B is greater than 1/2 R_A because the junction of R_A and R_B cannot bring pin 2 down to 1/3 V_{CC} and trigger the lower comparator.

ADDITIONAL INFORMATION

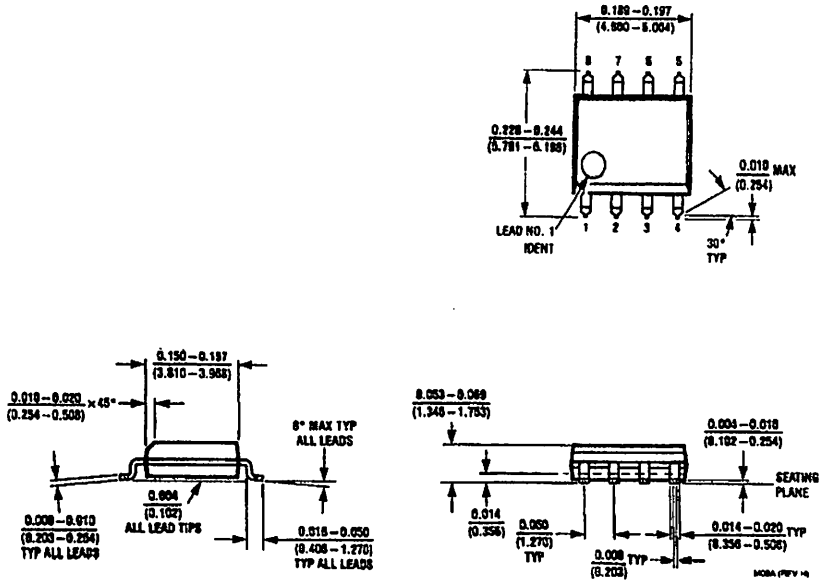
Adequate power supply bypassing is necessary to protect associated circuitry. Minimum recommended is 0.1µF in parallel with 1µF electrolytic.

Lower comparator storage time can be as long as 10µs when pin 2 is driven fully to ground for triggering. This limits the monostable pulse width to 10µs minimum.

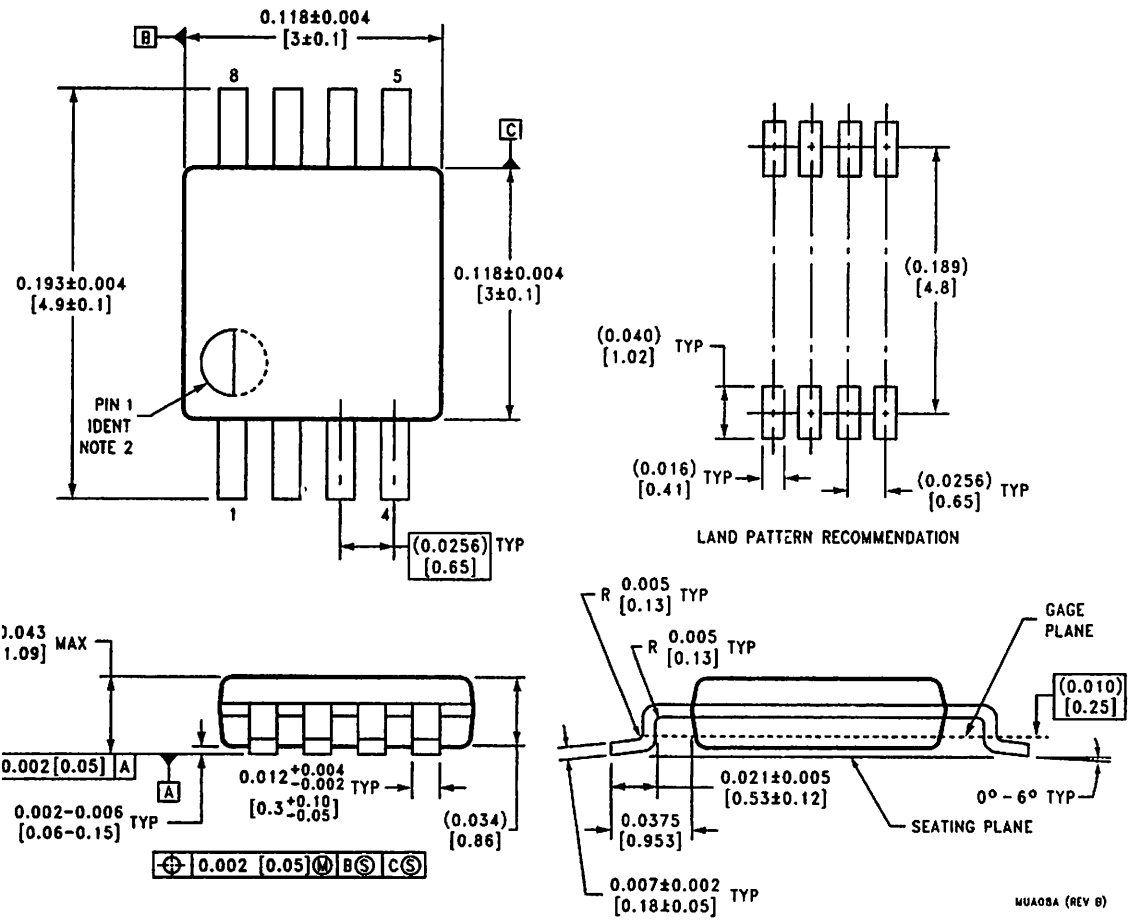
Delay time reset to output is 0.47µs typical. Minimum reset pulse width must be 0.3µs, typical.

Pin 7 current switches within 30ns of the output (pin 3) voltage.

ysical Dimensions inches (millimeters) unless otherwise noted

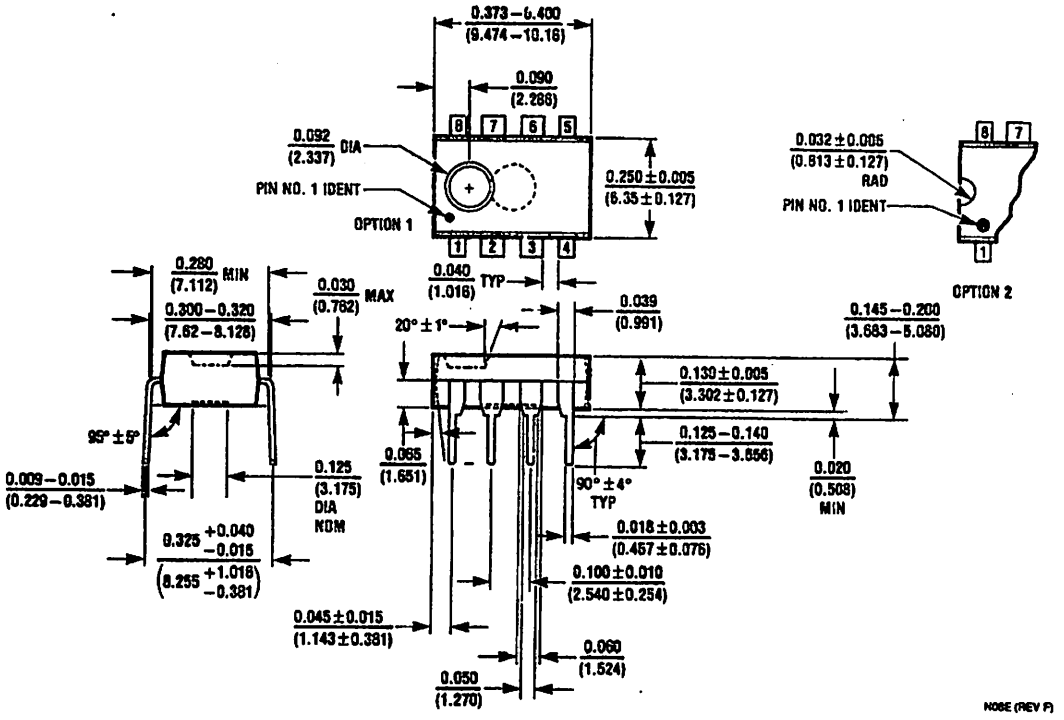


Small Outline Package (M)
NS Package Number M08A



8-Lead (0.118" Wide) Molded Mini Small Outline Package
NS Package Number MUA08A

Physical Dimensions inches (millimeters) unless otherwise noted (Continued)



Molded Dual-In-Line Package (N)
NS Package Number N08E

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2. A critical component is any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

National Semiconductor Corporation
Americas
Tel: 1-800-272-9959
Fax: 1-800-737-7018
Email: support@nsc.com
www.national.com

National Semiconductor Europe
Fax: +49 (0) 180-530 85 86
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Deutsch Tel: +49 (0) 69 9508 6208
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- Static Operation: 0 Hz to 24 MHz
- e-level Program Memory Lock
- 8-bit Internal RAM
- ogrammable I/O Lines
- 16-bit Timer/Counters
- Interrupt Sources
- rammable UART Serial Channel
- erial Interface
- power Idle and Power-down Modes
- upt Recovery From Power-down
- rammable Watchdog Timer
- Data Pointer
- r-off Flag

ription

T89S8252 is a low-power, high-performance CMOS 8-bit microcomputer with
s of downloadable Flash programmable and erasable read only memory and
s of EEPROM. The device is manufactured using Atmel's high-density nonvol-
emory technology and is compatible with the industry-standard 80C51
ion set and pinout. The on-chip downloadable Flash allows the program mem-
be reprogrammed in-system through an SPI serial interface or by a
tional nonvolatile memory programmer. By combining a versatile 8-bit CPU
wnloadable Flash on a monolithic chip, the Atmel AT89S8252 is a powerful
mputer which provides a highly-flexible and cost-effective solution to many
led control applications.

89S8252 provides the following standard features: 8K bytes of downloadable
2K bytes of EEPROM, 256 bytes of RAM, 32 I/O lines, programmable watch-
er, two data pointers, three 16-bit timer/counters, a six-vector two-level
t architecture, a full duplex serial port, on-chip oscillator, and clock circuitry. In
, the AT89S8252 is designed with static logic for operation down to zero fre-
and supports two software selectable power saving modes. The Idle Mode
e CPU while allowing the RAM, timer/counters, serial port, and interrupt sys-
continue functioning. The Power-down mode saves the RAM contents but
the oscillator, disabling all other chip functions until the next interrupt or hard-
set.

wnloadable Flash can be changed a single byte at a time and is accessible
the SPI serial interface. Holding RESET active forces the SPI bus into a serial
mming interface and allows the program memory to be written to or read from
Lock Bit 2 has been activated.

ATMEL®

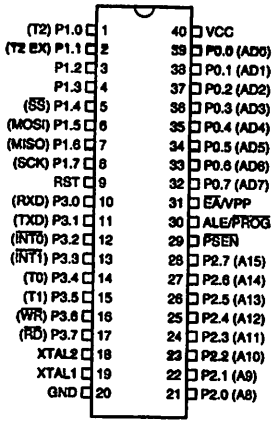
8-bit Microcontroller with 8K Bytes Flash

AT89S8252

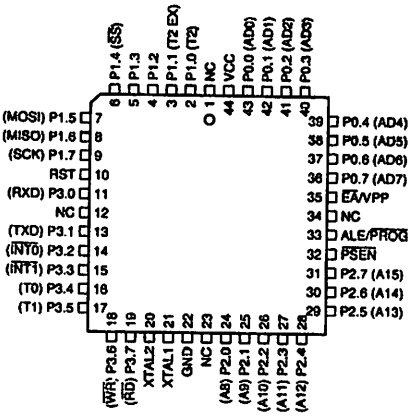
Rev. 0401E–02/00

Configurations

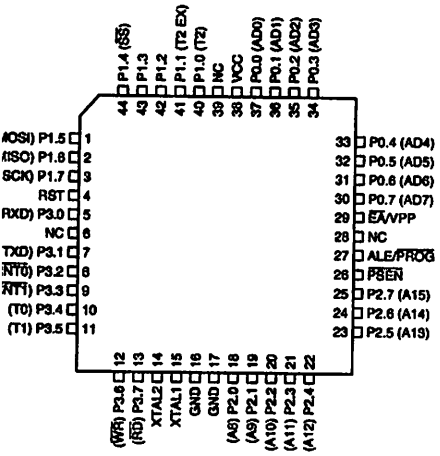
PDIP



PLCC



PQFP/TQFP



escription

oltage.

an 8-bit open drain bbi-didirectional I/O port. As an ort, each pin can sink eight TTL inputs. When 1s en to port 0 pins, the pins can be used as high- ce inputs.

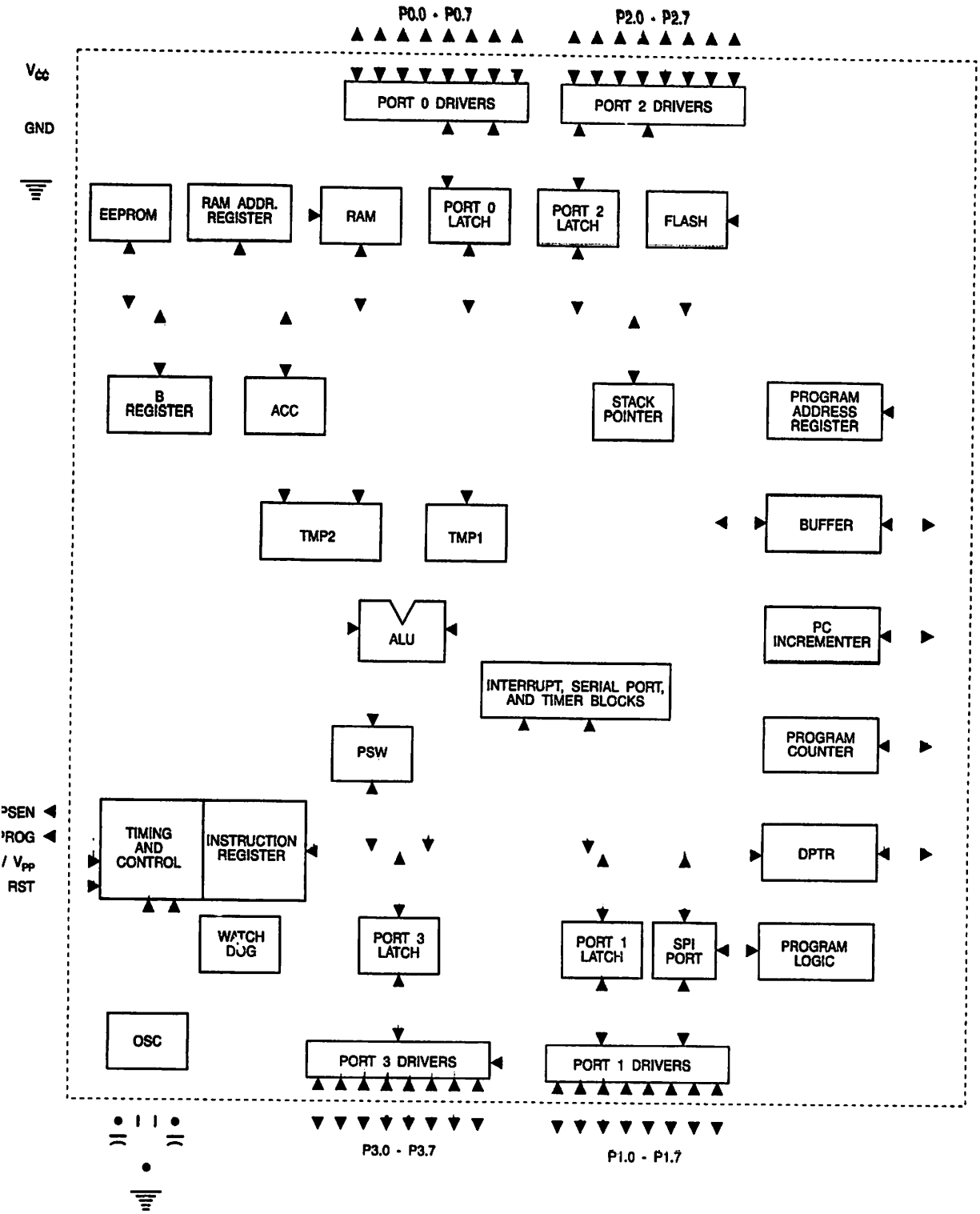
in also be configured to be the multiplexed low- ldress/data bus during accesses to external program and data memory. In this mode, P0 has internal pullups.

Port 0 also receives the code bytes during Flash programming and outputs the code bytes during program verification. External pullups are required during program verification.

Port 1

Port 1 is an 8-bit bi-directional I/O port with internal pullups. The Port 1 output buffers can sink/source four TTL inputs. When 1s are written to Port 1 pins, they are pulled high by the internal pullups and can be used as inputs. As inputs, Port 1 pins that are externally being pulled low will source current (I_{IL}) because of the internal pullups.

Diagram


P0.0 - P0.7
P2.0 - P2.7
VCC
GND
PORT 0 DRIVERS
PORT 2 DRIVERS
EEPROM
RAM ADDR. REGISTER
RAM
PORT 0 LATCH
PORT 2 LATCH
FLASH
B REGISTER
ACC
STACK POINTER
PROGRAM ADDRESS REGISTER
TMP2
TMP1
BUFFER
ALU
PC INCREMENTER
INTERRUPT, SERIAL PORT, AND TIMER BLOCKS
PSW
PROGRAM COUNTER
PSEN
PROG
/ VPP
RST
TIMING AND CONTROL
INSTRUCTION REGISTER
DPTR
WATCH DOG
PORT 3 LATCH
PORT 1 LATCH
SPI PORT
PROGRAM LOGIC
OSC
PORT 3 DRIVERS
PORT 1 DRIVERS
P3.0 - P3.7
P1.0 - P1.7

Port 1 pins provide additional functions. P1.0 and in be configured to be the timer/counter 2 external iput (P1.0/T2) and the timer/counter 2 trigger input 2EX), respectively.

escription

nore, P1.4, P1.5, P1.6, and P1.7 can be configured SPI slave port select, data input/output and shift put/output pins as shown in the following table.

n	Alternate Functions
	T2 (external count input to Timer/Counter 2), clock-out
	T2EX (Timer/Counter 2 capture/reload trigger and direction control)
	$\overline{SS}$ (Slave port select input)
	MOSI (Master data output, slave data input pin for SPI channel)
	MISO (Master data input, slave data output pin for SPI channel)
	SCK (Master clock output, slave clock input pin for SPI channel)

lso receives the low-order address bytes during ogramming and verification.

an 8-bit bi-directional I/O port with internal pullups. 2 output buffers can sink/source four TTL inputs. are written to Port 2 pins, they are pulled high by nal pullups and can be used as inputs. As inputs, ns that are externally being pulled low will source I_{IL}) because of the internal pullups.

mits the high-order address byte during fetches ernal program memory and during accesses to data memory that use 16-bit addresses (MOVX @ In this application, Port 2 uses strong internal pul- on emitting 1s. During accesses to external data that use 8-bit addresses (MOVX @ RI), Port 2 contents of the P2 Special Function Register.

so receives the high-order address bits and some ignals during Flash programming and verification.

an 8 bit bi-directional I/O port with internal pullups. 3 output buffers can sink/source four TTL inputs. are written to Port 3 pins, they are pulled high by ial pullups and can be used as inputs. As inputs, Port 3 pins that are externally being pulled low will source current (I_{IL}) because of the pullups.

Port 3 also serves the functions of various special features of the AT89S8252, as shown in the following table.

Port 3 also receives some control signals for Flash programming and verification.

Port Pin	Alternate Functions
P3.0	RXD (serial input port)
P3.1	TXD (serial output port)
P3.2	$\overline{INT0}$ (external interrupt 0)
P3.3	$\overline{INT1}$ (external interrupt 1)
P3.4	T0 (timer 0 external input)
P3.5	T1 (timer 1 external input)
P3.6	$\overline{WR}$ (external data memory write strobe)
P3.7	$\overline{RD}$ (external data memory read strobe)

RST

Reset input. A high on this pin for two machine cycles while the oscillator is running resets the device.

ALE/$\overline{PROG}$

Address Latch Enable is an output pulse for latching the low byte of the address during accesses to external memory. This pin is also the program pulse input ($\overline{PROG}$) during Flash programming.

In normal operation, ALE is emitted at a constant rate of 1/6 the oscillator frequency and may be used for external timing or clocking purposes. Note, however, that one ALE pulse is skipped during each access to external data memory.

If desired, ALE operation can be disabled by setting bit 0 of SFR location 8EH. With the bit set, ALE is active only during a MOVX or MOVC instruction. Otherwise, the pin is weakly pulled high. Setting the ALE-disable bit has no effect if the microcontroller is in external execution mode.

$\overline{PSEN}$

Program Store Enable is the read strobe to external program memory.

When the AT89S8252 is executing code from external program memory, $\overline{PSEN}$ is activated twice each machine cycle, except that two $\overline{PSEN}$ activations are skipped during each access to external data memory.

$\overline{EA}$/VPP

External Access Enable. $\overline{EA}$ must be strapped to GND in order to enable the device to fetch code from external pro-

nemory locations starting at 0000H up to FFFFH. owever, that if lock bit 1 is programmed, $\overline{EA}$ will be lly latched on reset.

uld be strapped to V_{CC} for internal program execu- This pin also receives the 12-volt programming voltage (V_{PP}) during Flash programming when 12- gramming is selected.

XTAL1

Input to the inverting oscillator amplifier and input to the internal clock operating circuit.

XTAL2

Output from the inverting oscillator amplifier.

- AT89S8252 SFR Map and Reset Values

								0FFH
B 00000000								0F7H
								0EFH
ACC 00000000								0E7H
								0DFH
PSW 00000000					SPCR 000001XX			0D7H
T2CON 00000000	T2MOD XXXXXX00	RCAP2L 00000000	RCAP2H 00000000	TL2 00000000	TH2 00000000			0CFH
								0C7H
IP XX000000								0BFH
P3 11111111								0B7H
IE 0X000000		SPSR 00XXXXXX						0AFH
P2 11111111								0A7H
SCON 00000000	SBUF XXXXXXXX							9FH
P1 11111111						WMCON 00000010		97H
TCON 00000000	TMOD 00000000	TL0 00000000	TL1 00000000	TH0 00000000	TH1 00000000			8FH
P0 11111111	SP 00000111	DP0L 00000000	DP0H 00000000	DP1L 00000000	DP1H 00000000	SPDR XXXXXXXX	PCON 0XXX0000	87H

al Function Registers

the on-chip memory area called the Special Function Register (SFR) space is shown in Table 1.

: not all of the addresses are occupied, and unoc- ddresses may not be implemented on the chip. cesses to these addresses will in general return lata, and write accesses will have an indeterminate

ftware should not write 1s to these unlisted locations, since they may be used in future products to invoke new features. In that case, the reset or inactive values of the new bits will always be 0.

Timer 2 Registers Control and status bits are contained in registers T2CON (shown in Table 2) and T2MOD (shown in Table 9) for Timer 2. The register pair (RCAP2H, RCAP2L) are the Capture/Reload registers for Timer 2 in 16 bit capture mode or 16-bit auto-reload mode.

T2CON—Timer/Counter 2 Control Register

Address = 0C8H Reset Value = 0000 0000B

ssable

$\overline{TF2}$	EXF2	RCLK	TCLK	EXEN2	$\overline{TR2}$	$C/\overline{T2}$	$CP/\overline{RL2}$
7	6	5	4	3	2	1	0

	Function
	Timer 2 overflow flag set by a Timer 2 overflow and must be cleared by software. TF2 will not be set when either RCLK = 1 or TCLK = 1.
	Timer 2 external flag set when either a capture or reload is caused by a negative transition on T2EX and EXEN2 = 1. When Timer 2 interrupt is enabled, EXF2 = 1 will cause the CPU to vector to the Timer 2 interrupt routine. EXF2 must be cleared by software. EXF2 does not cause an interrupt in up/down counter mode (DCEN = 1).
	Receive clock enable. When set, causes the serial port to use Timer 2 overflow pulses for its receive clock in serial port Modes 1 and 3. RCLK = 0 causes Timer 1 overflows to be used for the receive clock.
	Transmit clock enable. When set, causes the serial port to use Timer 2 overflow pulses for its transmit clock in serial port Modes 1 and 3. TCLK = 0 causes Timer 1 overflows to be used for the transmit clock.
	Timer 2 external enable. When set, allows a capture or reload to occur as a result of a negative transition on T2EX if Timer 2 is not being used to clock the serial port. EXEN2 = 0 causes Timer 2 to ignore events at T2EX.
	Start/Stop control for Timer 2. TR2 = 1 starts the timer.
	Timer or counter select for Timer 2. $C/\overline{T2}$ = 0 for timer function. $C/\overline{T2}$ = 1 for external event counter (falling edge triggered).
	Capture/Reload select. $CP/\overline{RL2}$ = 1 causes captures to occur on negative transitions at T2EX if EXEN2 = 1. $CP/\overline{RL2}$ = 0 causes automatic reloads to occur when Timer 2 overflows or negative transitions occur at T2EX when EXEN2 = 1. When either RCLK or TCLK = 1, this bit is ignored and the timer is forced to auto-reload on Timer 2 overflow.

log and Memory Control Register The WMCON r contains control bits for the Watchdog Timer in Table 3). The EEMEN and EEMWE bits are used to select the 2K bytes on-chip EEPROM, and to enable byte-write. The DPS bit selects one of two DPTR registers available.

. WMCON—Watchdog and Memory Control Register

N Address = 96H

Reset Value = 0000 0010B

PS2	PS1	PS0	EEMWE	EEMEN	DPS	WDTRST	WDTEN
7	6	5	4	3	2	1	0

	Function
	Prescaler Bits for the Watchdog Timer. When all three bits are set to "0", the watchdog timer has a nominal period of 16 ms. When all three bits are set to "1", the nominal period is 2048 ms.
E	EEPROM Data Memory Write Enable Bit. Set this bit to "1" before initiating byte write to on-chip EEPROM with the MOVX instruction. User software should set this bit to "0" after EEPROM write is completed.
I	Internal EEPROM Access Enable. When EEMEN = 1, the MOVX instruction with DPTR will access on-chip EEPROM instead of external data memory. When EEMEN = 0, MOVX with DPTR accesses external data memory.
	Data Pointer Register Select. DPS = 0 selects the first bank of Data Pointer Register, DP0, and DPS = 1 selects the second bank, DP1
ST SY	Watchdog Timer Reset and EEPROM Ready/$\overline{\text{Busy}}$ Flag. Each time this bit is set to "1" by user software, a pulse is generated to reset the watchdog timer. The WDTRST bit is then automatically reset to "0" in the next instruction cycle. The WDTRST bit is Write-Only. This bit also serves as the RDY/$\overline{\text{BSY}}$ flag in a Read-Only mode during EEPROM write. RDY/$\overline{\text{BSY}}$ = 1 means that the EEPROM is ready to be programmed. While programming operations are being executed, the RDY/$\overline{\text{BSY}}$ bit equals "0" and is automatically reset to "1" when programming is completed.
I	Watchdog Timer Enable Bit. WDTEN = 1 enables the watchdog timer and WDTEN = 0 disables the watchdog timer.

Isters Control and status bits for the Serial Periph- rface are contained in registers SPCR (shown in and SPSR (shown in Table 5). The SPI data bits ained in the SPDR register. Writing the SPI data during serial data transfer sets the Write Collision)L, in the SPSR register. The SPDR is double buff- writing and the values in SPDR are not changed by

t Registers The global interrupt enable bit and the al interrupt enable bits are in the IE register. In the individual interrupt enable bit for the SPI is in R register. Two priorities can be set for each of the upt sources in the IP register.

Dual Data Pointer Registers To facilitate accessing both internal EEPROM and external data memory, two banks of 16 bit Data Pointer Registers are provided: DP0 at SFR address locations 82H-83H and DP1 at 84H-85H. Bit DPS = 0 in SFR WMCON selects DP0 and DPS = 1 selects DP1. The user should always initialize the DPS bit to the appropriate value before accessing the respective Data Pointer Register.

Power Off Flag The Power Off Flag (POF) is located at bit_4 (PCON.4) in the PCON SFR. POF is set to "1" during power up. It can be set and reset under software control and is not affected by RESET.

SPCR—SPI Control Register

ddress = D5H

Reset Value = 0000 01XXB

SPIE	SPE	DORD	MSTR	CPOL	CPHA	SPR1	SPR0
7	6	5	4	3	2	1	0

	Function
	SPI Interrupt Enable. This bit, in conjunction with the ES bit in the IE register, enables SPI interrupts: SPIE = 1 and ES = 1 enable SPI interrupts. SPIE = 0 disables SPI interrupts.
	SPI Enable. SPI = 1 enables the SPI channel and connects $\overline{SS}$, MOSI, MISO and SCK to pins P1.4, P1.5, P1.6, and P1.7. SPI = 0 disables the SPI channel.
	Data Order. DORD = 1 selects LSB first data transmission. DORD = 0 selects MSB first data transmission.
	Master/Slave Select. MSTR = 1 selects Master SPI mode. MSTR = 0 selects Slave SPI mode.
	Clock Polarity. When CPOL = 1, SCK is high when idle. When CPOL = 0, SCK of the master device is low when not transmitting. Please refer to figure on SPI Clock Phase and Polarity Control.
	Clock Phase. The CPHA bit together with the CPOL bit controls the clock and data relationship between master and slave. Please refer to figure on SPI Clock Phase and Polarity Control.
	SPI Clock Rate Select. These two bits control the SCK rate of the device configured as master. SPR1 and SPR0 have no effect on the slave. The relationship between SCK and the oscillator frequency, $F_{osc.}$, is as follows: SPR1SPR0 SCK = $F_{osc.}$ divided by 0 0 4 0 1 16 1 0 64 1 1 128

SPSR – SPI Status Register

ldress = AAH

Reset Value = 00XX XXXXB

SPIF	WCOL	–	–	–	–	–	–
7	6	5	4	3	2	1	0

	Function
	SPI Interrupt Flag. When a serial transfer is complete, the SPIF bit is set and an interrupt is generated if SPIE = 1 and ES = 1. The SPIF bit is cleared by reading the SPI status register with SPIF and WCOL bits set, and then accessing the SPI data register.
	Write Collision Flag. The WCOL bit is set if the SPI data register is written during a data transfer. During data transfer, the result of reading the SPDR register may be incorrect, and writing to it has no effect. The WCOL bit (and the SPIF bit) are cleared by reading the SPI status register with SPIF and WCOL set, and then accessing the SPI data register.

SPDR – SPI Data Register

ldress = 86H

Reset Value = unchanged

SPD7	SPD6	SPD5	SPD4	SPD3	SPD2	SPD1	SPD0
7	6	5	4	3	2	1	0

Memory – EEPROM and RAM

39S8252 implements 2K bytes of on-chip EEPROM storage and 256 bytes of RAM. The upper 128 RAM occupy a parallel space to the Special Function Registers. That means the upper 128 bytes have the addresses as the SFR space but are physically separate SFR space.

n instruction accesses an internal location above 7FH, the address mode used in the instruction s whether the CPU accesses the upper 128 bytes or the SFR space. Instructions that use direct ng access SFR space.

mple, the following direct addressing instruction s the SFR at location 0A0H (which is P2).

```
0A0H, #data
```

ons that use indirect addressing access the upper 8s of RAM. For example, the following indirect ng instruction, where R0 contains 0A0H, accesses byte at address 0A0H, rather than P2 (whose is 0A0H).

```
@R0, #data
```

at stack operations are examples of indirect ng, so the upper 128 bytes of data RAM are avail- stack space.

chip EEPROM data memory is selected by setting IEN bit in the WMCON register at SFR address 96H. The EEPROM address range is from 000H to he MOVX instructions are used to access the M. To access off-chip data memory with the MOVX ns, the EEMEN bit needs to be set to "0".

IWE bit in the WMCON register needs to be set to any byte location in the EEPROM can be written. tware should reset EEMWE bit to "0" if no further M write is required. EEPROM write cycles in the gramming mode are self-timed and typically take The progress of EEPROM write can be monitored ng the RDY/$\overline{BSY}$ bit (read-only) in SFR WMCON. $\overline{Y}$ = 0 means programming is still in progress and $\overline{Y}$ = 1 means EEPROM write cycle is completed her write cycle can be initiated.

n, during EEPROM programming, an attempted n the EEPROM will fetch the byte being written MSB complemented. Once the write cycle is com- ue data are valid at all bit locations.

ammable Watchdog Timer

rammable Watchdog Timer (WDT) operates from endent oscillator. The prescaler bits, PS0, PS1 in SFR WMCON are used to set the period of the g Timer from 16 ms to 2048 ms. The available riods are shown in the following table and the actual timer periods (at V_{CC} = 5V) are within ±30% of the nominal.

The WDT is disabled by Power-on Reset and during Power-down. It is enabled by setting the WDTEN bit in SFR WMCON (address = 96H). The WDT is reset by setting the WDTRST bit in WMCON. When the WDT times out without being reset or disabled, an internal RST pulse is generated to reset the CPU.

Table 7. Watchdog Timer Period Selection

WDT Prescaler Bits			
PS2	PS1	PS0	Period (nominal)
0	0	0	16 ms
0	0	1	32 ms
0	1	0	64 ms
0	1	1	128 ms
1	0	0	256 ms
1	0	1	512 ms
1	1	0	1024 ms
1	1	1	2048 ms

Timer 0 and 1

Timer 0 and Timer 1 in the AT89S8252 operate the same way as Timer 0 and Timer 1 in the AT89C51, AT89C52 and AT89C55. For further information, see the October 1995 Microcontroller Data Book, page 2-45, section titled, "Timer/Counters."

Timer 2

Timer 2 is a 16 bit Timer/Counter that can operate as either a timer or an event counter. The type of operation is selected by bit C/$\overline{T2}$ in the SFR T2CON (shown in Table 2). Timer 2 has three operating modes: capture, auto-reload (up or down counting), and baud rate generator. The modes are selected by bits in T2CON, as shown in Table 8.

Timer 2 consists of two 8-bit registers, TH2 and TL2. In the Timer function, the TL2 register is incremented every machine cycle. Since a machine cycle consists of 12 oscillator periods, the count rate is 1/12 of the oscillator frequency.

In the Counter function, the register is incremented in response to a 1-to-0 transition at its corresponding external input pin, T2. In this function, the external input is sampled during S5P2 of every machine cycle. When the samples show a high in one cycle and a low in the next cycle, the count is incremented. The new count value appears in the register during S3P1 of the cycle following the one in which

sition was detected. Since two machine cycles (24 r periods) are required to recognize a 1-to-0 transi- e maximum count rate is 1/24 of the oscillator cy. To ensure that a given level is sampled at least fore it changes, the level should be held for at least machine cycle.

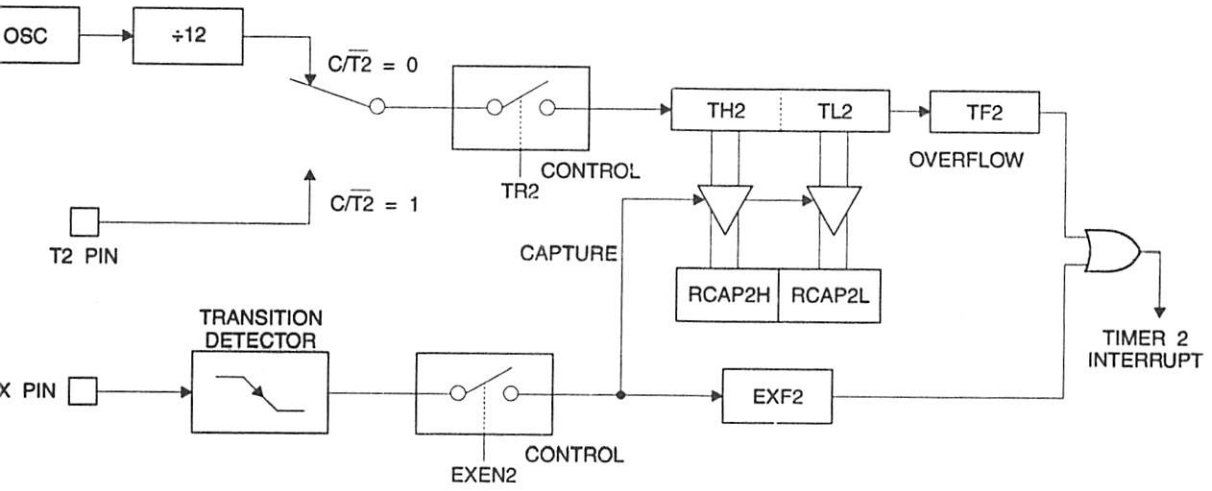
Timer 2 Operating Modes

+ TCLK	CP/$\overline{RL2}$	TR2	MODE
0	0	1	16-bit Auto-reload
0	1	1	16-bit Capture
1	X	1	Baud Rate Generator
X	X	0	(Off)

Capture Mode

In the capture mode, two options are selected by bit EXEN2 in T2CON. If EXEN2 = 0, Timer 2 is a 16 bit timer or counter which upon overflow sets bit TF2 in T2CON. This bit can then be used to generate an interrupt. If EXEN2 = 1, Timer 2 performs the same operation, but a l-to-0 transition at external input T2EX also causes the current value in TH2 and TL2 to be captured into RCAP2H and RCAP2L, respectively. In addition, the transition at T2EX causes bit EXF2 in T2CON to be set. The EXF2 bit, like TF2, can generate an interrupt. The capture mode is illustrated in Figure 1.

. Timer 2 in Capture Mode



reload (Up or Down Counter)

2 can be programmed to count up or down when red in its 16 bit auto-reload mode. This feature is l by the DCEN (Down Counter Enable) bit located in 1 T2MOD (see Table 9). Upon reset, the DCEN bit) 0 so that timer 2 will default to count up. When s set, Timer 2 can count up or down, depending on e of the T2EX pin.

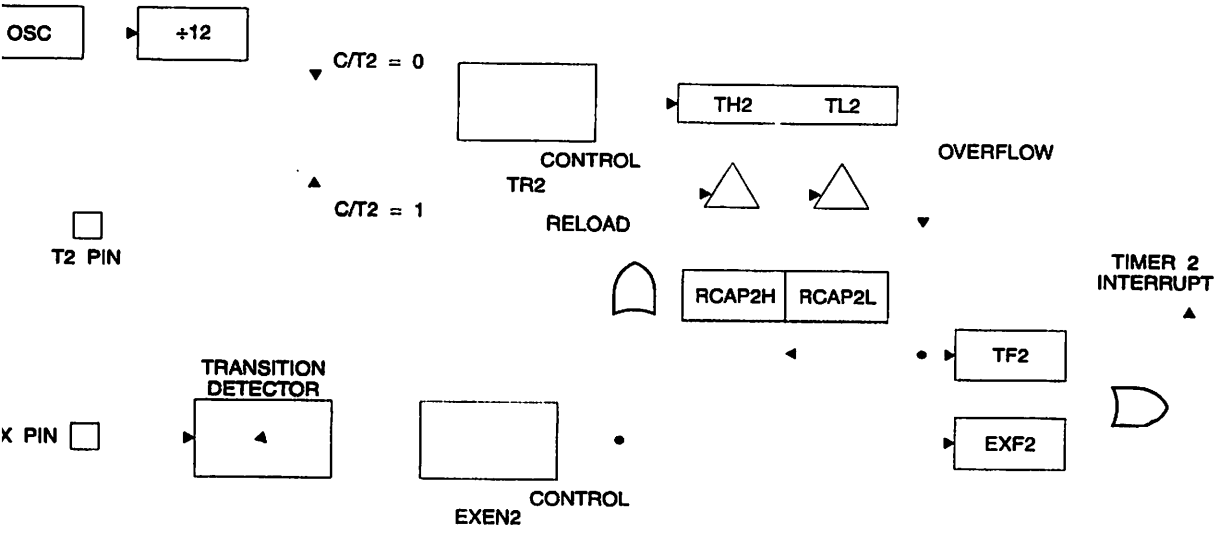
2 shows Timer 2 automatically counting up when = 0. In this mode, two options are selected by bit in T2CON. If EXEN2 = 0, Timer 2 counts up to H and then sets the TF2 bit upon overflow. The / also causes the timer registers to be reloaded with)it value in RCAP2H and RCAP2L. The values in H and RCAP2L are preset by software. If EXEN2 =)it reload can be triggered either by an overflow or by a 1-to-0 transition at external input T2EX. This transition also sets the EXF2 bit. Both the TF2 and EXF2 bits can generate an interrupt if enabled.

Setting the DCEN bit enables Timer 2 to count up or down, as shown in Figure 3. In this mode, the T2EX pin controls the direction of the count. A logic 1 at T2EX makes Timer 2 count up. The timer will overflow at 0FFFFH and set the TF2 bit. This overflow also causes the 16 bit value in RCAP2H and RCAP2L to be reloaded into the timer registers, TH2 and TL2, respectively.

A logic 0 at T2EX makes Timer 2 count down. The timer underflows when TH2 and TL2 equal the values stored in RCAP2H and RCAP2L. The underflow sets the TF2 bit and causes 0FFFFH to be reloaded into the timer registers.

The EXF2 bit toggles whenever Timer 2 overflows or underflows and can be used as a 17th bit of resolution. In this operating mode, EXF2 does not flag an interrupt.

2. Timer 2 in Auto Reload Mode (DCEN = 0)



T2MOD – Timer 2 Mode Control Register

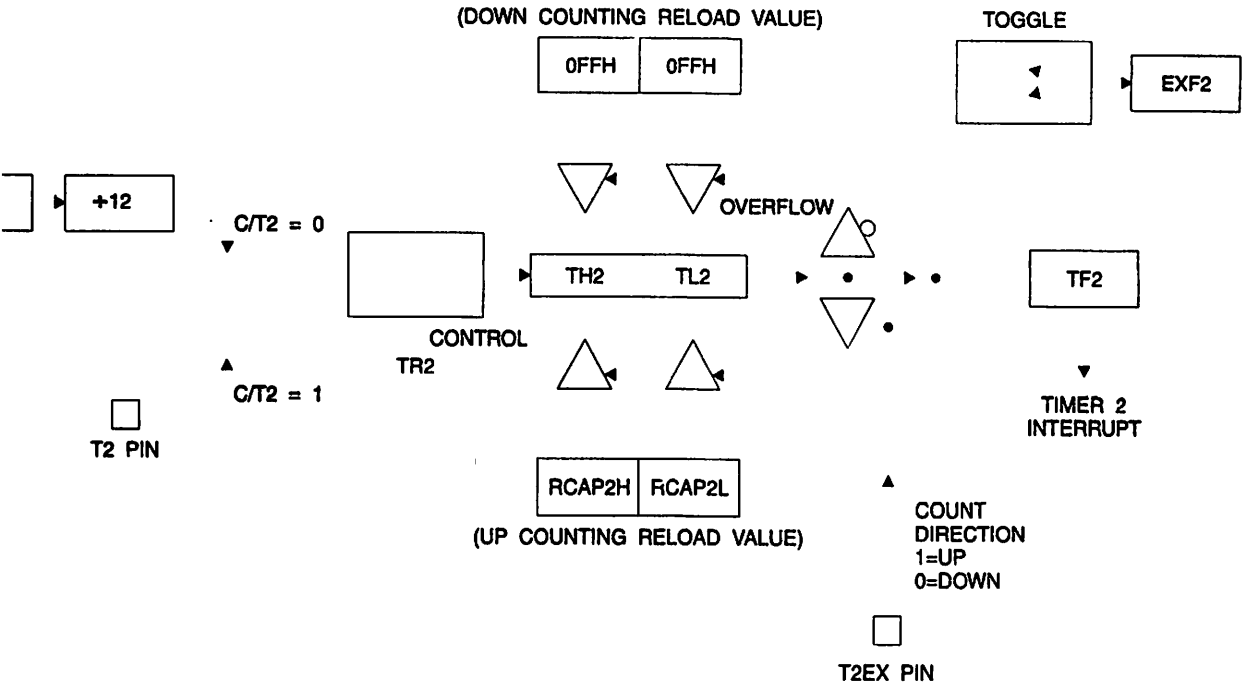
Address = 0C9H — Reset Value = XXXX XX00B

Addressable

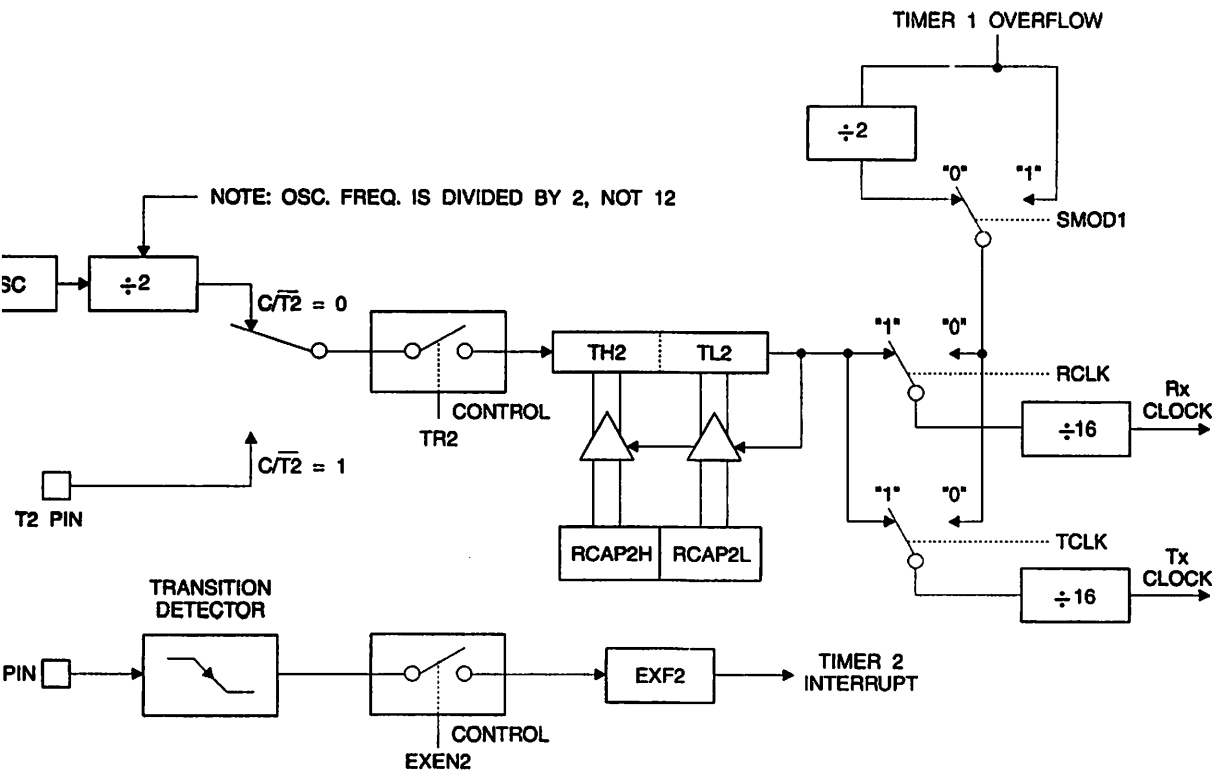
–	–	–	–	–	–	T2OE	DCEN
7	6	5	4	3	2	1	0

	Function
	Not implemented, reserved for future use.
	Timer 2 Output Enable bit.
	When set, this bit allows Timer 2 to be configured as an up/down counter.

. Timer 2 Auto Reload Mode (DCEN = 1)



. Timer 2 in Baud Rate Generator Mode



Rate Generator

is selected as the baud rate generator by setting nd/or RCLK in T2CON (Table 2). Note that the es for transmit and receive can be different if Timer 1 for the receiver or transmitter and Timer 1 is used other function. Setting RCLK and/or TCLK puts into its baud rate generator mode, as shown in Fig-

d rate generator mode is similar to the auto-reload that a rollover in TH2 causes the Timer 2 registers oaded with the 16 bit value in registers RCAP2H AP2L, which are preset by software.

d rates in Modes 1 and 3 are determined by Timer low rate according to the following equation.

$$\text{s 1 and 3 Baud Rates} = \frac{\text{Timer 2 Overflow Rate}}{16}$$

er can be configured for either timer or counter n. In most applications, it is configured for timer 1 ($CP/\overline{T2} = 0$). The timer operation is different for when it is used as a baud rate generator. Normally, er, it increments every machine cycle (at 1/12 the frequency). As a baud rate generator, however, it nts every state time (at 1/2 the oscillator fre- The baud rate formula is given below.

$$\frac{\text{1 and 3}}{\text{Rate}} = \frac{\text{Oscillator Frequency}}{32 \times [65536 - (\text{RCAP2H,RCAP2L})]}$$

CAP2H, RCAP2L) is the content of RCAP2H and taken as a 16 bit unsigned integer.

s a baud rate generator is shown in Figure 4. This valid only if RCLK or TCLK = 1 in T2CON. Note lover in TH2 does not set TF2 and will not gener- terrupt. Note too, that if EXEN2 is set, a 1-to-0 in T2EX will set EXF2 but will not cause a reload AP2H, RCAP2L) to (TH2, TL2). Thus when Timer 2 is in use as a baud rate generator, T2EX can be used as an extra external interrupt.

Note that when Timer 2 is running (TR2 = 1) as a timer in the baud rate generator mode, TH2 or TL2 should not be read from or written to. Under these conditions, the Timer is incremented every state time, and the results of a read or write may not be accurate. The RCAP2 registers may be read but should not be written to, because a write might overlap a reload and cause write and/or reload errors. The timer should be turned off (clear TR2) before accessing the Timer 2 or RCAP2 registers.

Programmable Clock Out

A 50% duty cycle clock can be programmed to come out on P1.0, as shown in Figure 5. This pin, besides being a regular I/O pin, has two alternate functions. It can be programmed to input the external clock for Timer/Counter 2 or to output a 50% duty cycle clock ranging from 61 Hz to 4 MHz at a 16 MHz operating frequency.

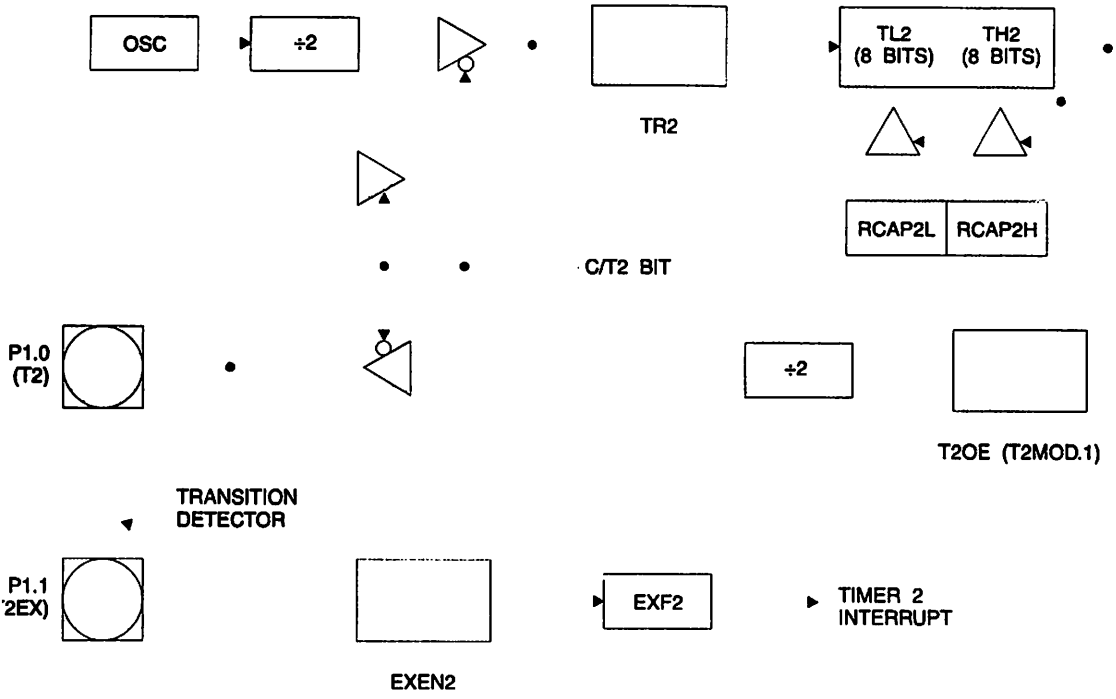
To configure the Timer/Counter 2 as a clock generator, bit $C/\overline{T2}$ (T2CON.1) must be cleared and bit T2OE (T2MOD.1) must be set. Bit TR2 (T2CON.2) starts and stops the timer.

The clock-out frequency depends on the oscillator frequency and the reload value of Timer 2 capture registers (RCAP2H, RCAP2L), as shown in the following equation.

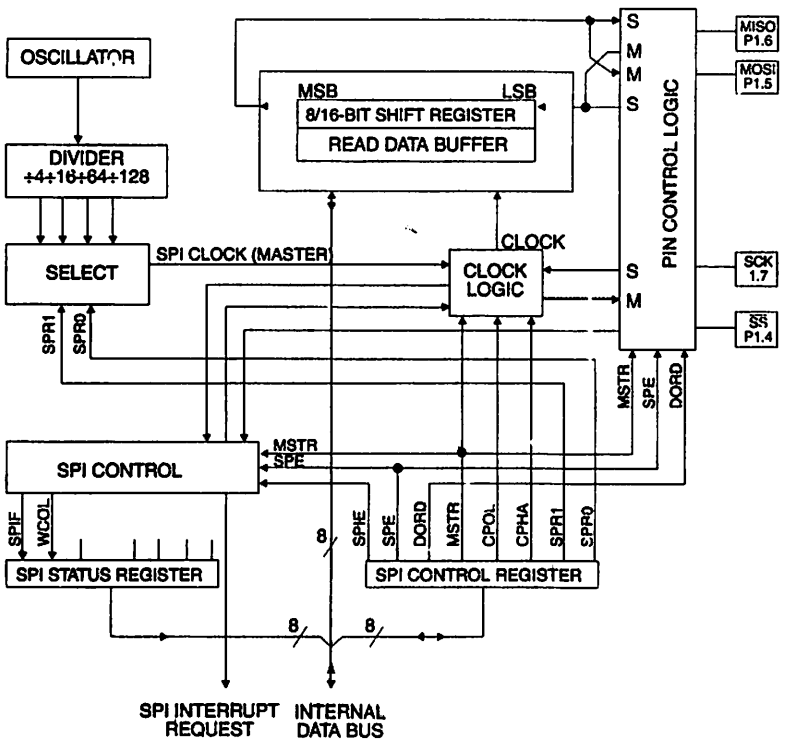
$$\text{Clock Out Frequency} = \frac{\text{Oscillator Frequency}}{4 \times [65536 - (\text{RCAP2H,RCAP2L})]}$$

In the clock-out mode, Timer 2 rollovers will not generate an interrupt. This behavior is similar to when Timer 2 is used as a baud-rate generator. It is possible to use Timer 2 as a baud-rate generator and a clock generator simultaneously. Note, however, that the baud-rate and clock-out frequencies cannot be determined independently from one another since they both use RCAP2H and RCAP2L.

Timer 2 in Clock-out Mode



SPI Block Diagram



RT in the AT89S8252 operates the same way as RT in the AT89C51, AT89C52 and AT89C55. For information, see the October 1995 Microcontroller ok, page 2-49, section titled, "Serial Interface."

l Peripheral Interface

al peripheral interface (SPI) allows high-speed syn- us data transfer between the AT89S8252 and ral devices or between several AT89S8252 s. The AT89S8252 SPI features include the :

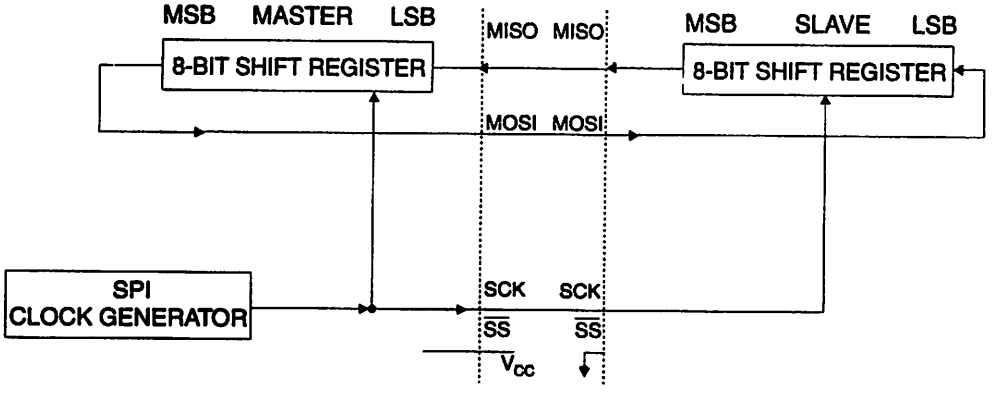
- uplex, 3-Wire Synchronous Data Transfer
- r or Slave Operation
- Hz Bit Frequency (max.)
- irst or MSB First Data Transfer
- Programmable Bit Rates
- f Transmission Interrupt Flag
- Write Collision Flag Protection
- Wakeup from Idle Mode (Slave Mode Only)

The interconnection between master and slave CPUs with SPI is shown in the following figure. The SCK pin is the clock output in the master mode but is the clock input in the slave mode. Writing to the SPI data register of the master CPU starts the SPI clock generator, and the data written shifts out of the MOSI pin and into the MOSI pin of the slave CPU. After shifting one byte, the SPI clock generator stops, setting the end of transmission flag (SPIF). If both the SPI interrupt enable bit (SPIE) and the serial port interrupt enable bit (ES) are set, an interrupt is requested.

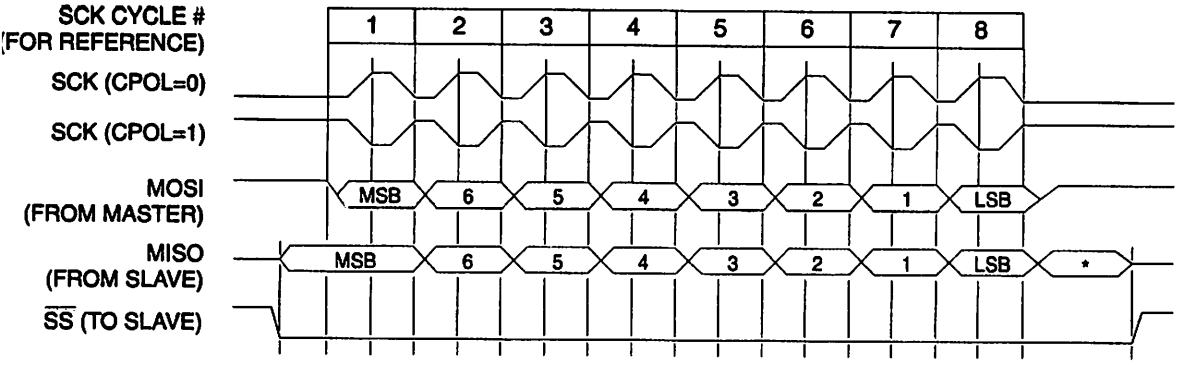
The Slave Select input, $\overline{SS}$/P1.4, is set low to select an individual SPI device as a slave. When $\overline{SS}$/P1.4 is set high, the SPI port is deactivated and the MOSI/P1.5 pin can be used as an input.

There are four combinations of SCK phase and polarity with respect to serial data, which are determined by control bits CPHA and CPOL. The SPI data transfer formats are shown in Figure 8 and Figure 9.

. SPI Master-slave Interconnection

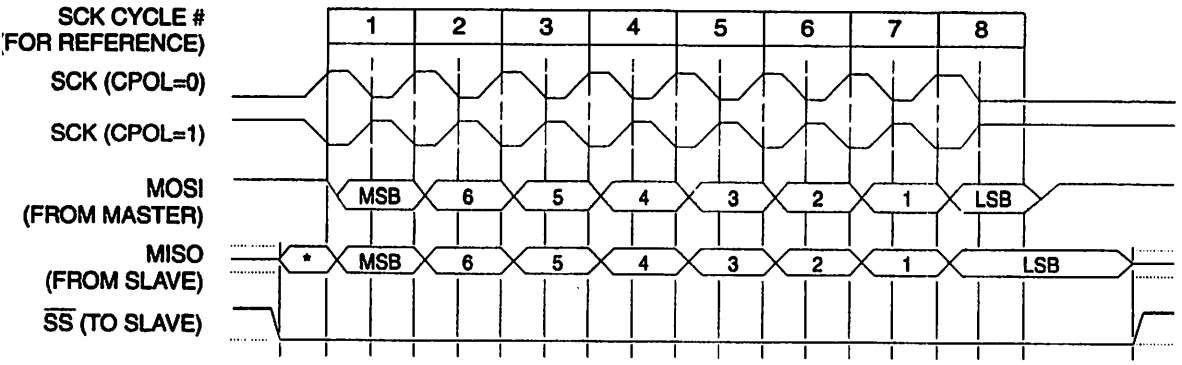


. SPI transfer Format with CPHA = 0



ned but normally MSB of character just received

. SPI Transfer Format with CPHA = 1



ned but normally LSB of previously transmitted character

ıpts

9S8252 has a total of six interrupt vectors: two interrupts ($\overline{INT0}$ and $\overline{INT1}$), three timer interrupts 0, 1, and 2), and the serial port interrupt. These s are all shown in Figure 10.

hese interrupt sources can be individually enabled ed by setting or clearing a bit in Special Function IE. IE also contains a global disable bit, EA, which all interrupts at once.

t Table 10 shows that bit position IE.6 is unimple-. In the AT89C51, bit position IE.5 is also nented. User software should not write 1s to these ions, since they may be used in future AT89

nterrupt is generated by the logical OR of bits TF2 F2 in register T2CON. Neither of these flags is by hardware when the service routine is vectored ct, the service routine may have to determine it was TF2 or EXF2 that generated the interrupt, bit will have to be cleared in software.

er 0 and Timer 1 flags, TF0 and TF1, are set at the cycle in which the timers overflow. The values polled by the circuitry in the next cycle. However, r 2 flag, TF2, is set at S2P2 and is polled in the cle in which the timer overflows.

Table 10. Interrupt Enable (IE) Register

(MSB)(LSB)

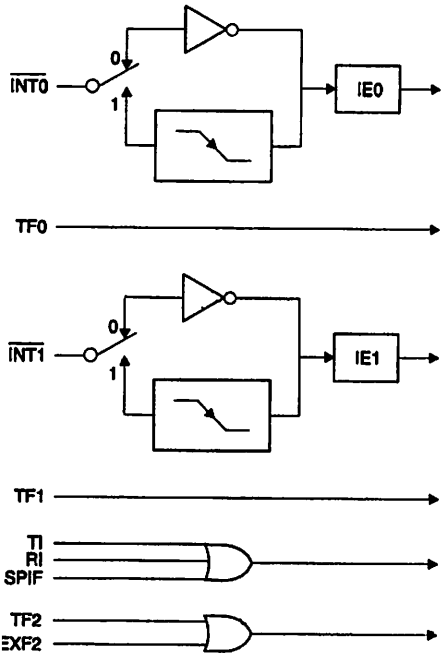
EA	–	ET2	ES	ET1	EX1	ET0	EX0

Enable Bit = 1 enables the interrupt.

Enable Bit = 0 disables the interrupt.

Symbol	Position	Function
EA	IE.7	Disables all interrupts. If EA = 0, no interrupt is acknowledged. If EA = 1, each interrupt source is individually enabled or disabled by setting or clearing its enable bit.
–	IE.6	Reserved.
ET2	IE.5	Timer 2 interrupt enable bit.
ES	IE.4	SPI and UART interrupt enable bit.
ET1	IE.3	Timer 1 interrupt enable bit.
EX1	IE.2	External interrupt 1 enable bit.
ET0	IE.1	Timer 0 interrupt enable bit.
EX0	IE.0	External interrupt 0 enable bit.
User software should never write 1s to unimplemented bits, because they may be used in future AT89 products.		

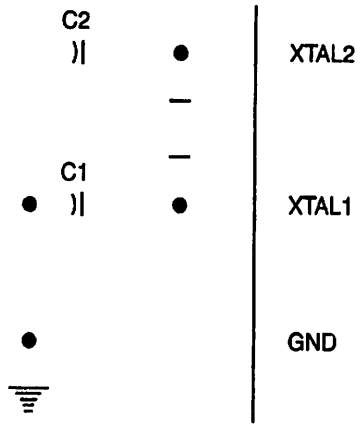
10. Interrupt Sources



ator Characteristics

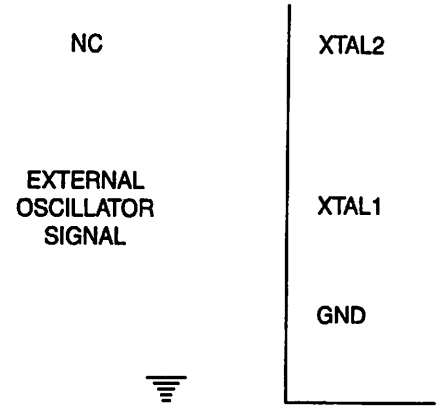
ınd XTAL2 are the input and output, respectively, 'erting amplifier that can be configured for use as ip oscillator, as shown in Figure 11. Either a quartz ır ceramic resonator may be used. To drive the ɔm an external clock source, XTAL2 should be left cted while XTAL1 is driven, as shown in Figure 12. e no requirements on the duty cycle of the external nal, since the input to the internal clocking circuitry h a divide-by-two flip-flop, but minimum and maxi- ltage high and low time specifications must be l.

Figure 11. Oscillator Connections



Note: Note: C1, C2 = 30 pF ± 10 pF for Crystals
= 40 pF ± 10 pF for Ceramic Resonators

Figure 12. External Clock Drive Configuration



ode

ode, the CPU puts itself to sleep while all the on-
ipherals remain active. The mode is invoked by
. The content of the on-chip RAM and all the spe-
:tions registers remain unchanged during this
he idle mode can be terminated by any enabled
or by a hardware reset.

it when idle mode is terminated by a hardware
e device normally resumes program execution from where it left off, up to two machine cycles before the internal reset algorithm takes control. On-chip hardware inhibits access to internal RAM in this event, but access to the port pins is not inhibited. To eliminate the possibility of an unexpected write to a port pin when idle mode is terminated by a reset, the instruction following the one that invokes idle mode should not write to a port pin or to external memory.

s of External Pins During Idle and Power-down Modes

	Program Memory	ALE	$\overline{PSEN}$	PORT0	PORT1	PORT2	PORT3
	Internal	1	1	Data	Data	Data	Data
	External	1	1	Float	Data	Address	Data
own	Internal	0	0	Data	Data	Data	Data
own	External	0	0	Float	Data	Data	Data

-down Mode

wer-down mode, the oscillator is stopped and the
n that invokes power-down is the last instruction
. The on-chip RAM and Special Function Regis-
in their values until the power-down mode is
d. Exit from power-down can be initiated either by
re reset or by an enabled external interrupt. Reset
the SFRs but does not change the on-chip RAM.
should not be activated before V_{CC} is restored to
al operating level and must be held active long
allow the oscillator to restart and stabilize.

ower-down via an interrupt, the external interrupt
enabled as level sensitive before entering power-
e interrupt service routine starts at 16 ms (nomi-
the enabled interrupt pin is activated.

Program Memory Lock Bits

The AT89S8252 has three lock bits that can be left unprogrammed (U) or can be programmed (P) to obtain the additional features listed in the following table.

When lock bit 1 is programmed, the logic level at the $\overline{EA}$ pin is sampled and latched during reset. If the device is powered up without a reset, the latch initializes to a random value and holds that value until reset is activated. The latched value of $\overline{EA}$ must agree with the current logic level at that pin in order for the device to function properly.

Once programmed, the lock bits can only be unprogrammed with the Chip Erase operations in either the parallel or serial modes.

Bit Protection Modes[1][2]

ram Lock Bits			
B1	LB2	LB3	Protection Type
U	U	U	No internal memory lock feature.
P	U	U	MOVC instructions executed from external program memory are disabled from fetching code bytes from internal memory. $\overline{EA}$ is sampled and latched on reset and further programming of the Flash memory (parallel or serial mode) is disabled.
P	P	U	Same as Mode 2, but parallel or serial verify are also disabled.
P	P	P	Same as Mode 3, but external execution is also disabled.

. U = Unprogrammed
. P = Programmed

ramming the Flash and EEPROM

AT89S8252 Flash Microcontroller offers 8K bytes stem reprogrammable Flash Code memory and 2K EEPROM Data memory.

89S8252 is normally shipped with the on-chip Flash nd EEPROM Data memory arrays in the erased e. contents = FFH) and ready to be programmed. vice supports a High-voltage (12V) Parallel pro- ing mode and a Low-voltage (5V) Serial nming mode. The serial programming mode pro- convenient way to download the AT89S8252 inside 's system. The parallel programming mode is com- with conventional third party Flash or EPROM mers.

de and Data memory arrays are mapped via sepa- dress spaces in the serial programming mode. In llel programming mode, the two arrays occupy one us address space: 0000H to 1FFFH for the Code d 2000H to 27FFH for the Data array.

de and Data memory arrays on the AT89S8252 are med byte-by-byte in either programming mode. An se cycle is provided with the self-timed program- eration in the serial programming mode. There is to perform the Chip Erase operation to reprogram mory location in the serial programming mode ny of the lock bits have been programmed.

arallel programming mode, there is no auto-erase o reprogram any non-blank byte, the user needs to Chip Erase operation first to erase both arrays.

Programming Algorithm: To program and verify 9S8252 in the parallel programming mode, the fol- equence is recommended:

er-up sequence:

y power between V_{CC} and GND pins.

RST pin to "H".

y a 3 MHz to 24 MHz clock to XTAL1 pin and wait t least 10 milliseconds.

$\overline{PSEN}$ pin to "L"

pin to "H"

in to "H" and all other pins to "H".

y the appropriate combination of "H" or "L" logic s to pins P2.6, P2.7, P3.6, P3.7 to select one of rogramming operations shown in the Flash ramming Modes table.

y the desired byte address to pins P1.0 to P1.7 P2.0 to P2.5.

ly data to pins P0.0 to P0.7 for Write Code ation.

5. Raise $\overline{EA}/V_{PP}$ to 12V to enable Flash programming, erase or verification.
6. Pulse ALE/$\overline{PROG}$ once to program a byte in the Code memory array, the Data memory array or the lock bits. The byte-write cycle is self-timed and typically takes 1.5 ms.
7. To verify the byte just programmed, bring pin P2.7 to "L" and read the programmed data at pins P0.0 to P0.7.
8. Repeat steps 3 through 7 changing the address and data for the entire 2K or 8K bytes array or until the end of the object file is reached.
9. Power-off sequence:

   Set XTAL1 to "L".

   Set RST and $\overline{EA}$ pins to "L".

   Turn V_{CC} power off.

In the parallel programming mode, there is no auto-erase cycle and to reprogram any non-blank byte, the user needs to use the Chip Erase operation first to erase both arrays.

$\overline{Data}$ Polling: The AT89S8252 features $\overline{DATA}$ Polling to indicate the end of a write cycle. During a write cycle in the parallel or serial programming mode, an attempted read of the last byte written will result in the complement of the written datum on P0.7 (parallel mode), and on the MSB of the serial output byte on MISO (serial mode). Once the write cycle has been completed, true data are valid on all outputs, and the next cycle may begin. $\overline{DATA}$ Polling may begin any time after a write cycle has been initiated.

Ready/$\overline{Busy}$: The progress of byte programming in the parallel programming mode can also be monitored by the RDY/$\overline{BSY}$ output signal. Pin P3.4 is pulled Low after ALE goes High during programming to indicate $\overline{BUSY}$. P3.4 is pulled High again when programming is done to indicate READY.

Program Verify: If lock bits LB1 and LB2 have not been programmed, the programmed Code or Data byte can be read back via the address and data lines for verification. The state of the lock bits can also be verified directly in the parallel programming mode. In the serial programming mode, the state of the lock bits can only be verified indirectly by observing that the lock bit features are enabled.

Chip Erase: Both Flash and EEPROM arrays are erased electrically at the same time. In the parallel programming mode, chip erase is initiated by using the proper combination of control signals and by holding ALE/$\overline{PROG}$ low for 10 ms. The Code and Data arrays are written with all "1"s in the Chip Erase operation.

rial programming mode, a chip erase operation is by issuing the Chip Erase instruction. In this mode, se is self-timed and takes about 16 ms.

hip erase, a serial read from any address location n 00H at the data outputs.

rogramming Fuse: A programmable fuse is avail- disable Serial Programming if the user needs n system security. The Serial Programming Fuse be programmed or erased in the Parallel Program- de.

9S8252 is shipped with the Serial Programming abled.

the Signature Bytes: The signature bytes are the same procedure as a normal verification of 030H and 031H, except that P3.6 and P3.7 must to a logic low. The values returned are as follows:

H) = 1EH indicates manufactured by Atmel
H) = 72H indicates 89S8252

amming Interface

de byte in the Flash and EEPROM arrays can be and the entire array can be erased, by using the ate combination of control signals. The write oper- ycle is self-timed and once initiated, will cally time itself to completion.

programming vendors offer worldwide support for l microcontroller series. Please contact your local ning vendor for the appropriate software revision.

Downloading

Code and Data memory arrays can be pro- d using the serial SPI bus while RST is pulled to serial interface consists of pins SCK, MOSI (input) O (output). After RST is set high, the Programming nstruction needs to be executed first before pro- se operations can be executed.

erase cycle is built into the self-timed programming (in the serial mode ONLY) and there is no need ecute the Chip Erase instruction unless any of the have been programmed. The Chip Erase opera- the content of every memory location in both the d Data arrays into FFH.

and Data memory arrays have separate address 0000H to 1FFFH for Code memory and 000H to 7FFH for Data memory.

Either an external system clock is supplied at pin XTAL1 or a crystal needs to be connected across pins XTAL1 and XTAL2. The maximum serial clock (SCK) frequency should be less than 1/40 of the crystal frequency. With a 24 MHz oscillator clock, the maximum SCK frequency is 600 kHz.

Serial Programming Algorithm

To program and verify the AT89S8252 in the serial programming mode, the following sequence is recommended:

1. Power-up sequence:

   Apply power between VCC and GND pins.

   Set RST pin to "H".

   If a crystal is not connected across pins XTAL1 and XTAL2, apply a 3 MHz to 24 MHz clock to XTAL1 pin and wait for at least 10 milliseconds.
2. Enable serial programming by sending the Programming Enable serial instruction to pin MOSI/P1.5. The frequency of the shift clock supplied at pin SCK/P1.7 needs to be less than the CPU clock at XTAL1 divided by 40.
3. The Code or Data array is programmed one byte at a time by supplying the address and data together with the appropriate Write instruction. The selected memory location is first automatically erased before new data is written. The write cycle is self-timed and typically takes less than 2.5 ms at 5V.
4. Any memory location can be verified by using the Read instruction which returns the content at the selected address at serial output MISO/P1.6.
5. At the end of a programming session, RST can be set low to commence normal operation.

Power-off sequence (if needed):

Set XTAL1 to "L" (if a crystal is not used).

Set RST to "L".

Turn V_{CC} power off.

Serial Programming Instruction

The Instruction Set for Serial Programming follows a 3-byte protocol and is shown in the following table:

ıction Set

tion	Input Format			Operation
	Byte 1	Byte 2	Byte 3	
nming Enable	1010 1100	0101 0011	xxxx xxxx	Enable serial programming interface after RST goes high.
ase	1010 1100	xxxx x100	xxxx xxxx	Chip erase both 8K & 2K memory arrays.
ode Memory	aaaa a001	low addr	xxxx xxxx	Read data from Code memory array at the selected address. The 5 MSBs of the first byte are the high order address bits. The low order address bits are in the second byte. Data are available at pin MISO during the third byte.
ode Memory	aaaa a010	low addr	data in	Write data to Code memory location at selected address. The address bits are the 5 MSBs of the first byte together with the second byte.
ata Memory	00aa a101	low addr	xxxx xxxx	Read data from Data memory array at selected address. Data are available at pin MISO during the third byte.
ata Memory	00aa a110	low addr	data in	Write data to Data memory location at selected address.
ck Bits	1010 1100	x x111	xxxx xxxx	Write lock bits. Set LB1, LB2 or LB3 = "0" to program lock bits.

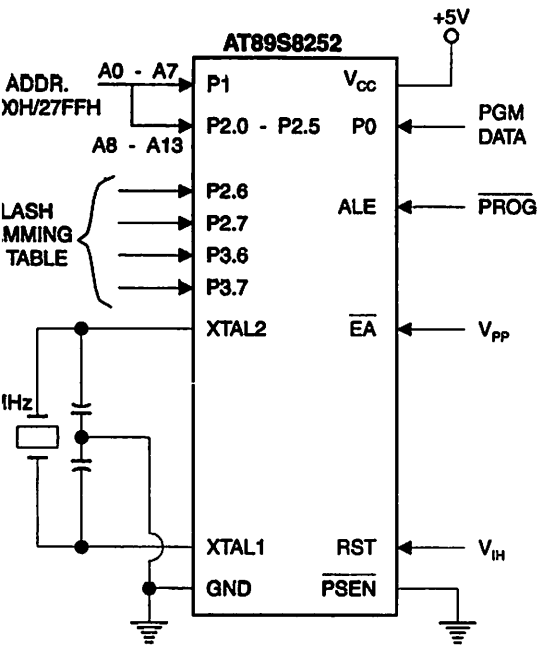
1. DATA polling is used to indicate the end of a write cycle which typically takes less than 2.5 ms at 5V.
2. "aaaaa" = high order address.
3. "x" = don't care.

and EEPROM Parallel Programming Modes

	RST	PSEN	ALE/PROG	EA/V_{PP}	P2.6	P2.7	P3.6	P3.7	Data I/O P0.7:0	Address P2.5:0 P1.7:0
rog. Modes	H	h[1]	h[1]	x						
ase	H	L	(2)	12V	H	L	L	L	X	X
0K bytes) Memory	H	L		12V	L	H	H	H	DIN	ADDR
0K bytes) Memory	H	L	H	12V	L	L	H	H	DOUT	ADDR
ck Bits:	H	L		12V	H	L	H	L	DIN	X
Bit - 1									P0.7 = 0	X
Bit - 2									P0.6 = 0	X
Bit - 3									P0.5 = 0	X
ck Bits:	H	L	H	12V	H	H	L	L	DOUT	X
Bit - 1									@P0.2	X
Bit - 2									@P0.1	X
Bit - 3									@P0.0	X
nel Code	H	L	H	12V	L	L	L	L	DOUT	30H
vice Code	H	L	H	12V	L	L	L	L	DOUT	31H
og. Enable	H	L	(2)	12V	L	H	L	H	P0.0 = 0	X
og. Disable	H	L	(2)	12V	L	H	L	H	P0.0 = 1	X
rial Prog. Fuse	H	L	H	12V	H	H	L	H	@P0.0	X

1. "h" = weakly pulled "High" internally.
2. Chip Erase and Serial Programming Fuse require a 10 ms PROG pulse. Chip Erase needs to be performed first before reprogramming any byte with a content other than FFH.
3. P3.4 is pulled Low during programming to indicate RDY/BSY.
4. "X" = don't care

I. Programming the Flash/EEPROM Memory



I. Verifying the Flash/EEPROM Memory

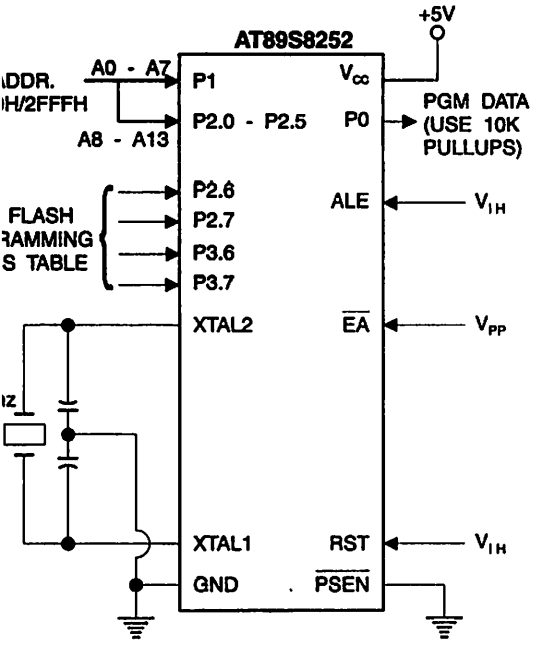
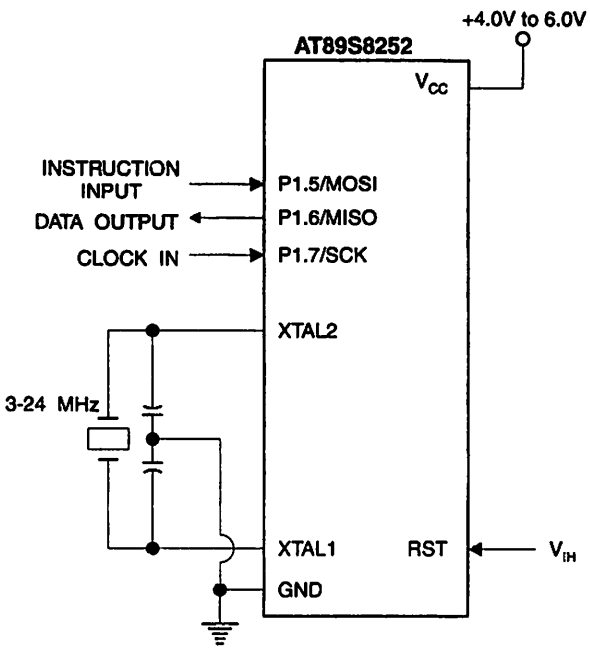


Figure 15. Flash/EEPROM Serial Downloading

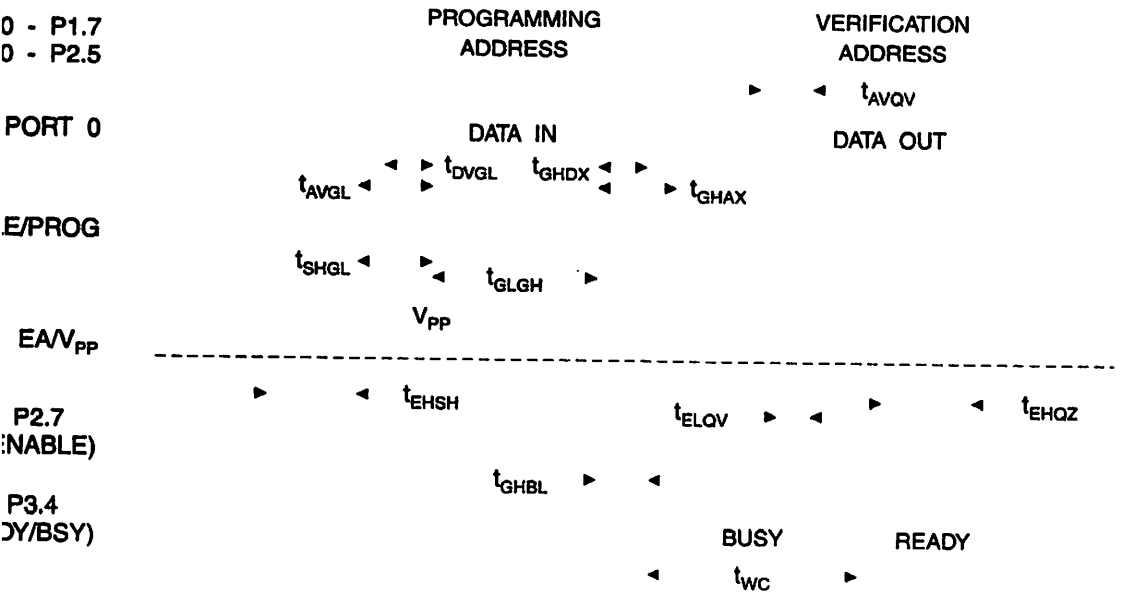


Programming and Verification Characteristics – Parallel Mode

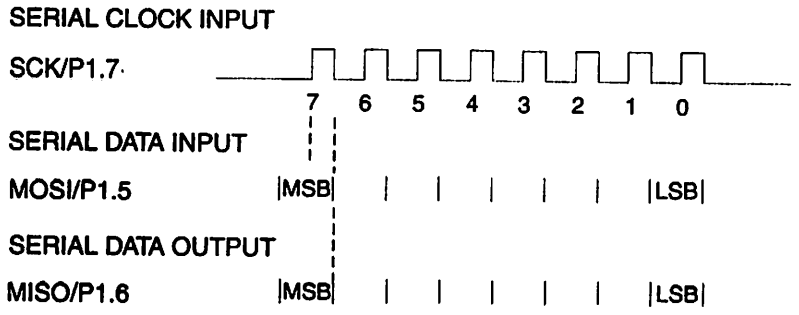
to 70°C, V_{CC} = 5.0V ± 10%

	Parameter	Min	Max	Units
	Programming Enable Voltage	11.5	12.5	V
	Programming Enable Current		1.0	mA
	Oscillator Frequency	3	24	MHz
	Address Setup to $\overline{PROG}$ Low	$48t_{CLCL}$		
	Address Hold after $\overline{PROG}$	$48t_{CLCL}$		
	Data Setup to $\overline{PROG}$ Low	$48t_{CLCL}$		
	Data Hold after $\overline{PROG}$	$48t_{CLCL}$		
	P2.7 ($\overline{ENABLE}$) High to V_{PP}	$48t_{CLCL}$		
	V_{PP} Setup to $\overline{PROG}$ Low	10		µs
	$\overline{PROG}$ Width	1	110	µs
	Address to Data Valid		$48t_{CLCL}$	
	$\overline{ENABLE}$ Low to Data Valid		$48t_{CLCL}$	
	Data Float after $\overline{ENABLE}$	0	$48t_{CLCL}$	
	$\overline{PROG}$ High to $\overline{BUSY}$ Low		1.0	µs
	Byte Write Cycle Time		2.0	ms

/EEPROM Programming and Verification Waveforms – Parallel Mode



Downloading Waveforms



ute Maximum Ratings*

g Temperature	-55°C to +125°C
Temperature	-65°C to +150°C
›n Any Pin pect to Ground	-1.0V to +7.0V
n Operating Voltage	6.6V
ut Current	15.0 mA

*NOTICE: Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

aracteristics

›s shown in this table are valid for T_A = -40°C to 85°C and V_{CC} = 5.0V ± 20%, unless otherwise noted.

Parameter	Condition	Min	Max	Units
Input Low-voltage	(Except $\overline{EA}$)	-0.5	0.2 V_{CC} - 0.1	V
Input Low-voltage ($\overline{EA}$)		-0.5	0.2 V_{CC} - 0.3	V
Input Hifh-voltage	(Except XTAL1, RST)	0.2 V_{CC} + 0.9	V_{CC} + 0.5	V
Input Hifh-voltage	(XTAL1, RST)	0.7 V_{CC}	V_{CC} + 0.5	V
Output Low-voltage (1) (Ports 1,2,3)	I_{OL} = 1.6 mA		0.5	V
Output Low-voltage (1) (Port 0, ALE, $\overline{PSEN}$)	I_{OL} = 3.2 mA		0.5	V
Output Hifh-voltage (Ports 1,2,3, ALE, $\overline{PSEN}$)	I_{OH} = -60 µA, V_{CC} = 5V ± 10%	2.4		V
	I_{OH} = -25 µA	0.75 V_{CC}		V
	I_{OH} = -10 µA	0.9 V_{CC}		V
Output Hifh-voltage (Port 0 in External Bus Mode)	I_{OH} = -800 µA, V_{CC} = 5V ± 10%	2.4		V
	I_{OH} = -300 µA	0.75 V_{CC}		V
	I_{OH} = -80 µA	0.9 V_{CC}		V
Logical 0 Input Current (Ports 1,2,3)	V_{IN} = 0.45V		-50	µA
Logical 1 to 0 Transition Current (Ports 1,2,3)	V_{IN} = 2V, V_{CC} = 5V ± 10%		-650	µA
Input Leakage Current (Port 0, $\overline{EA}$)	0.45 < V_{IN} < V_{CC}		±10	µA
Reset Pull-down Resistor		50	300	KΩ
Pin Capacitance	Test Freq. = 1 MHz, T_A = 25°C		10	pF
Power Supply Current	Active Mode, 12 MHz		25	mA
	Idle Mode, 12 MHz		6.5	mA
Power-down Mode (2)	V_{CC} = 6V		100	µA
	V_{CC} = 3V		40	µA

Under steady state (non-transient) conditions, I_{OL} must be externally limited as follows:
Maximum I_{OL} per port pin: 10 mA
Maximum I_{OL} per 8-bit port:
Port 0: 26 mA
Ports 1, 2, 3: 15 mA
Maximum total I_{OL} for all output pins: 71 mA
If I_{OL} exceeds the test condition, V_{OL} may exceed the related specification. Pins are not guaranteed to sink current greater than the listed test conditions.

2. Minimum V_{CC} for Power-down is 2V

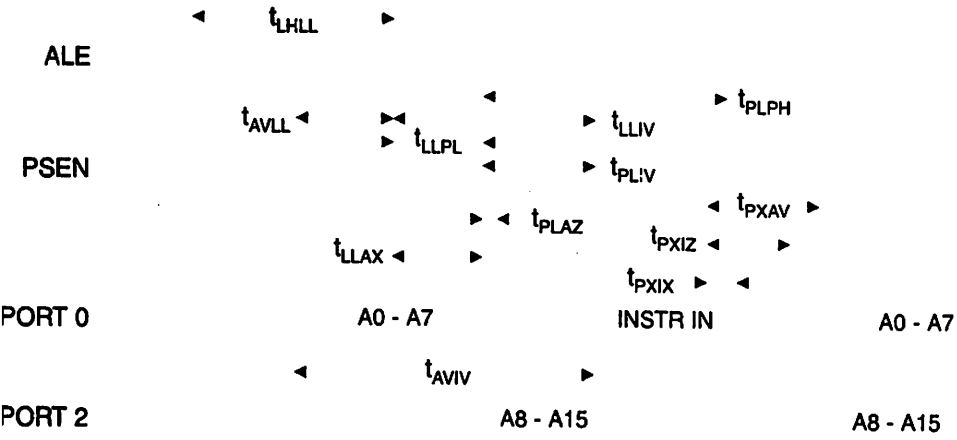
aracteristics

erating conditions, load capacitance for Port 0, ALE/$\overline{PROG}$, and $\overline{PSEN}$ = 100 pF; load capacitance for all other 80 pF.

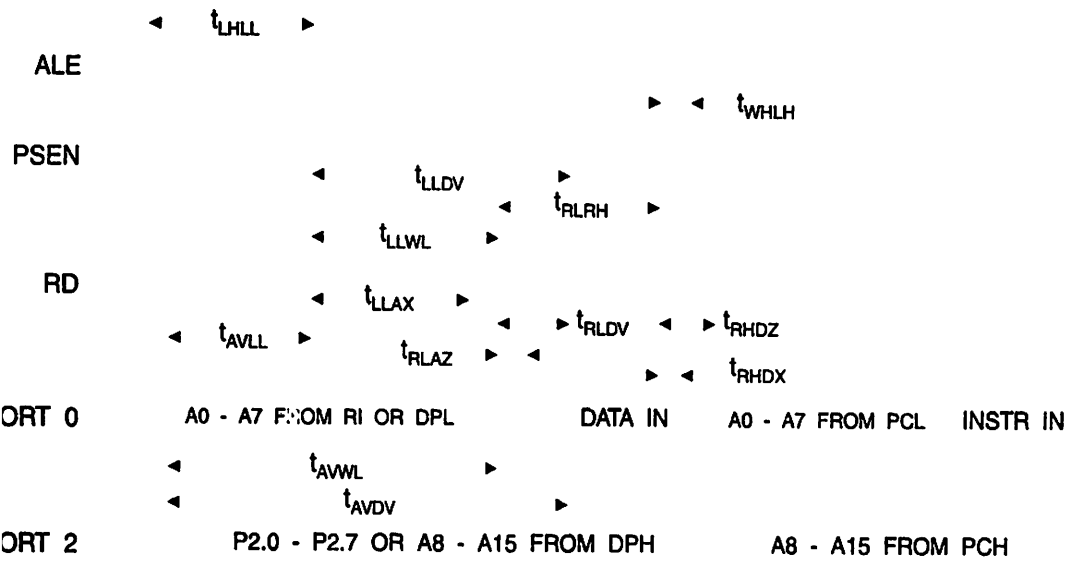
al Program and Data Memory Characteristics

Parameter	Variable Oscillator		Units
	Min	Max	
Oscillator Frequency	0	24	MHz
ALE Pulse Width	$2t_{CLCL}$ - 40		ns
Address Valid to ALE Low	t_{CLCL} - 13		ns
Address Hold after ALE Low	t_{CLCL} - 20		ns
ALE Low to Valid Instruction In		$4t_{CLCL}$ - 65	ns
ALE Low to $\overline{PSEN}$ Low	t_{CLCL} - 13		ns
$\overline{PSEN}$ Pulse Width	$3t_{CLCL}$ - 20		ns
$\overline{PSEN}$ Low to Valid Instruction In		$3t_{CLCL}$ - 45	ns
Input Instruction Hold after $\overline{PSEN}$	0		ns
Input Instruction Float after $\overline{PSEN}$		t_{CLCL} - 10	ns
$\overline{PSEN}$ to Address Valid	t_{CLCL} - 8		ns
Address to Valid Instruction In		$5t_{CLCL}$ - 55	ns
$\overline{PSEN}$ Low to Address Float		10	ns
$\overline{RD}$ Pulse Width	$6t_{CLCL}$ - 100		ns
$\overline{WR}$ Pulse Width	$6t_{CLCL}$ - 100		ns
$\overline{RD}$ Low to Valid Data In		$5t_{CLCL}$ - 90	ns
Data Hold after $\overline{RD}$	0		ns
Data Float after $\overline{RD}$		$2t_{CLCL}$ - 28	ns
ALE Low to Valid Data In		$8t_{CLCL}$ - 150	ns
Address to Valid Data In		$9t_{CLCL}$ - 165	ns
ALE Low to $\overline{RD}$ or $\overline{WR}$ Low	$3t_{CLCL}$ - 50	$3t_{CLCL}$ + 50	ns
Address to $\overline{RD}$ or $\overline{WR}$ Low	$4t_{CLCL}$ - 75		ns
Data Valid to $\overline{WR}$ Transition	t_{CLCL} - 20		ns
Data Valid to $\overline{WR}$ High	$7t_{CLCL}$ - 120		ns
Data Hold after $\overline{WR}$	t_{CLCL} - 20		ns
$\overline{RD}$ Low to Address Float		0	ns
$\overline{RD}$ or $\overline{WR}$ High to ALE High	t_{CLCL} - 20	t_{CLCL} + 25	ns

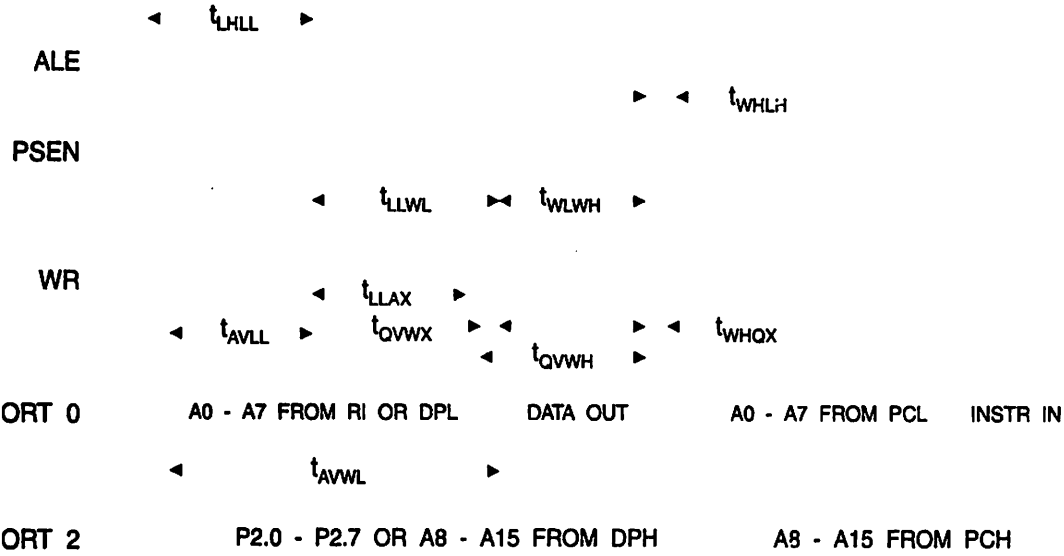
ıal Program Memory Read Cycle



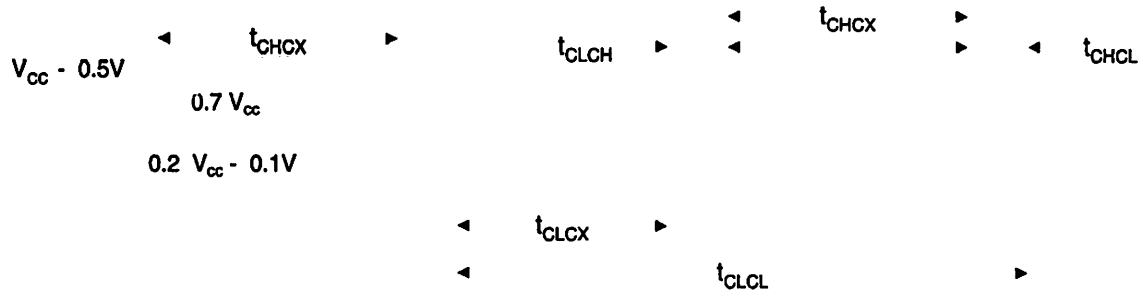
ıal Data Memory Read Cycle



ıal Data Memory Write Cycle



ıal Clock Drive Waveforms



ıal Clock Drive

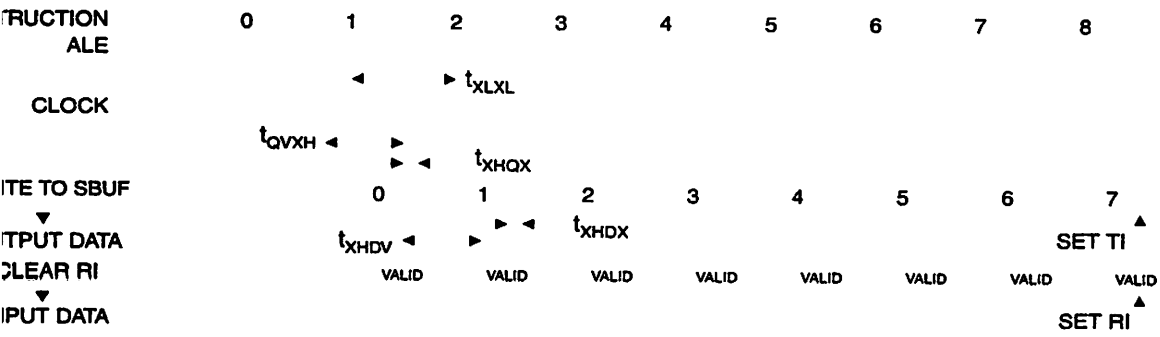
Parameter	V_{CC} = 4.0V to 6.0V		Units
	Min	Max	
Oscillator Frequency	0	24	MHz
Clock Period	41.6		ns
High Time	15		ns
Low Time	15		ns
Rise Time		20	ns
Fall Time		20	ns

l Port Timing: Shift Register Mode Test Conditions

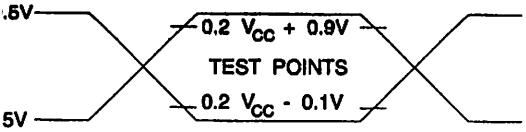
ıes in this table are valid for V_{CC} = 4.0V to 6V and Load Capacitance = 80 pF.

l	Parameter	Variable Oscillator		Units
		Min	Max	
	Serial Port Clock Cycle Time	$12t_{CLCL}$		µs
	Output Data Setup to Clock Rising Edge	$10t_{CLCL}$ - 133		ns
	Output Data Hold after Clock Rising Edge	$2t_{CLCL}$ - 117		ns
	Input Data Hold after Clock Rising Edge	0		ns
	Clock Rising Edge to Input Data Valid		$10t_{CLCL}$ - 133	ns

Register Mode Timing Waveforms

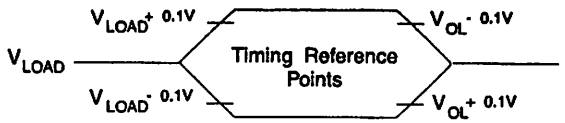


sting Input/Output Waveforms[1]



1. AC Inputs during testing are driven at V_{CC} - 0.5V for a logic 1 and 0.45V for a logic 0. Timing measurements are made at V_{IH} min. for a logic 1 and V_{IL} max. for a logic 0.

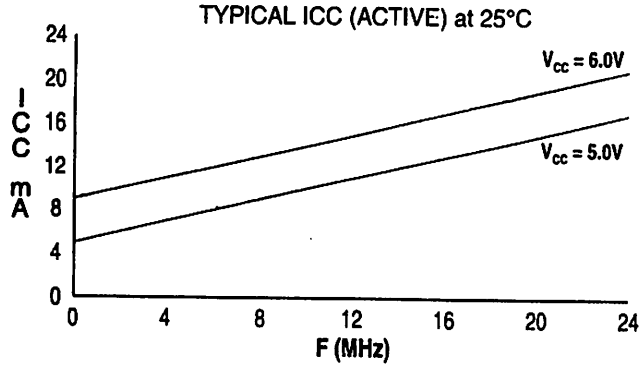
Float Waveforms[1]



Notes: 1. For timing purposes, a port pin is no longer floating when a 100 mV change from load voltage occurs. A port pin begins to float when a 100 mV change from the loaded V_{OH}/V_{OL} level occurs.

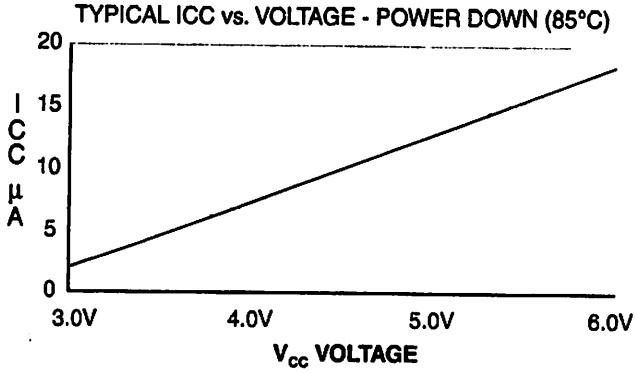
AT89S8252

TYPICAL ICC (ACTIVE) at 25°C



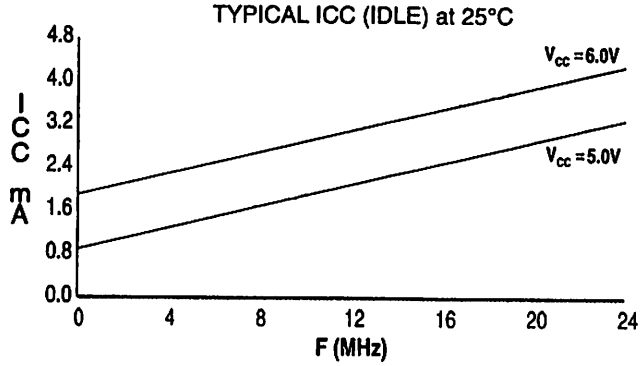
AT89S8252

TYPICAL ICC vs. VOLTAGE - POWER DOWN (85°C)



AT89S8252

TYPICAL ICC (IDLE) at 25°C



Notes: 1. XTAL1 tied to GND for Icc (power-down)
2. Lock bits programmed

ring Information

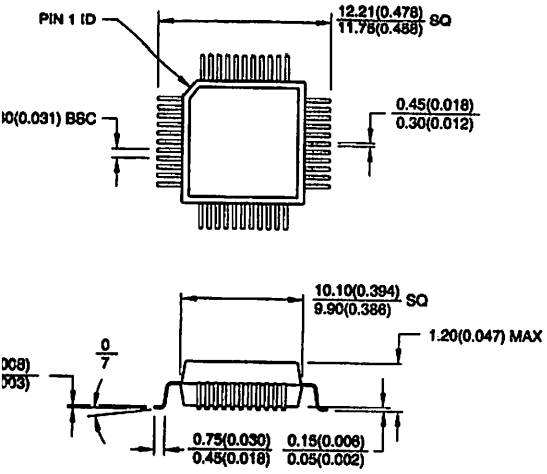
d t)	Power Supply	Ordering Code	Package	Operation Range
	4.0V to 6.0V	AT89S8252-24AC AT89S8252-24JC AT89S8252-24PC AT89S8252-24QC	44A 44J 40P6 44Q	Commercial (0°C to 70°C)
	4.0V to 6.0V	AT89S8252-24AI AT89S8252-24JI AT89S8252-24PI AT89S8252-24QI	44A 44J 40P6 44Q	Industrial (-40°C to 85°C)
	4.5V to 5.5V	AT89S8252-33AC AT89S8252-33JC AT89S8252-33PC AT89S8252-33QC	44A 44J 40P6 44Q	Commercial (0°C to 70°C)

[ ] = Preliminary Information

	Package Type
	44-lead, Thin Plastic Gull Wing Quad Flatpack (TQFP)
	44-lead, Plastic J-leaded Chip Carrier (PLCC)
	40-lead, 0.600" Wide, Plastic Dual Inline Package (PDIP)
	44-lead, Plastic Gull Wing Quad Flatpack (PQFP)

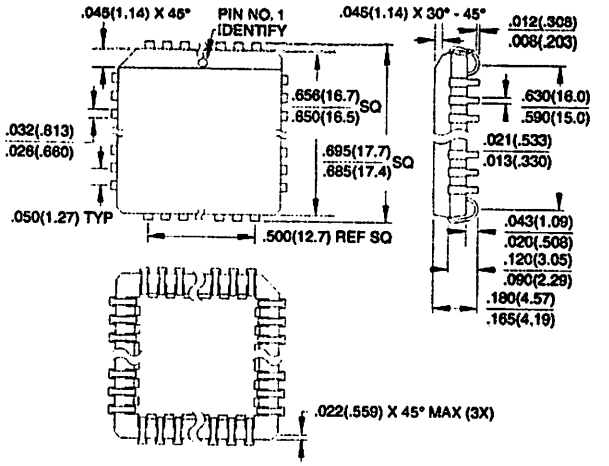
aging Information

\, 44-lead, Thin (1.0 mm) Plastic Gull Wing Quad
pack (TQFP)
ıensions in Millimeters and (Inches)*
EC STANDARD MS-026 ACB

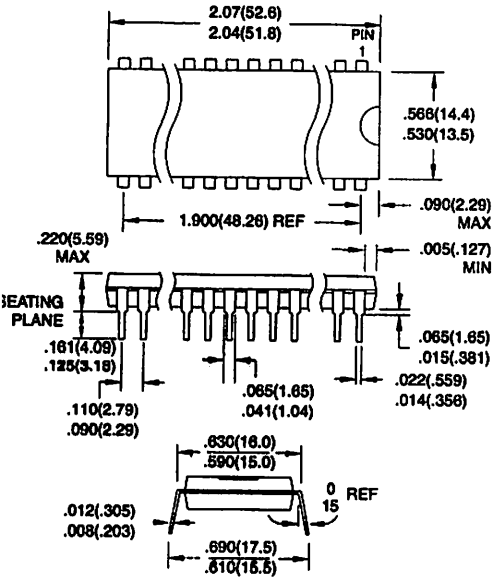


trolling dimension: millimeters

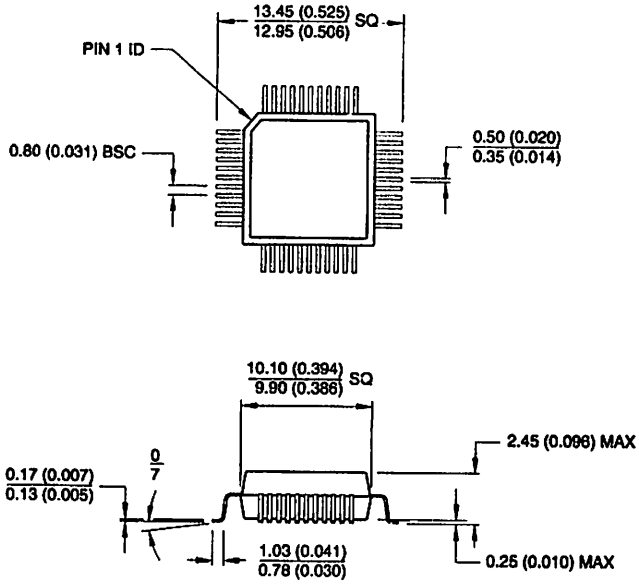
44J, 44-lead, Plastic J-leaded Chip Carrier (PLCC)
Dimensions in Inches and (Millimeters)
JEDEC STANDARD MS-018 AC



3, 40-lead, 0.600" Wide, Plastic Dual Inline
tage (PDIP)
ensions in Inches and (Millimeters)



44Q, 44-lead, Plastic Quad Flat Package (PQFP)
Dimensions in Millimeters and (Inches)*
JEDEC STANDARD MS-022 AB



Controlling dimension: millimeters

l Headquarters

rate Headquarters
Orchard Parkway
Jose, CA 95131
(408) 441-0311
(408) 487-2600

l U.K., Ltd.
eum Business Centre
'side Way
oerley, Surrey GU15 3YL
and
(44) 1276-686-677
(44) 1276-686-697

l Asia, Ltd.
1 1219
achem Golden Plaza
ody Road Tsimhatsui
Kowloon
Kong
852) 2721-9778
852) 2722-1369

l Japan K.K.
onetsu Shinkawa Bldg.
8 Shinkawa
-ku, Tokyo 104-0033
l
81) 3-3523-3551
81) 3-3523-7581

Atmel Operations

Atmel Colorado Springs
1150 E. Cheyenne Mtn. Blvd.
Colorado Springs, CO 80906
TEL (719) 576-3300
FAX (719) 540-1759

Atmel Rousset
Zone Industrielle
13106 Rousset Cedex
France
TEL (33) 4-4253-6000
FAX (33) 4-4253-6001

Fax-on-Demand
North America:
1-(800) 292-8635
International:
1-(408) 441-0732

e-mail
literature@atmel.com

Web Site
http://www.atmel.com

BBS
1-(408) 436-4309

0401E–02/00/xM

LIQUID CRYSTAL DISPLAY MODULE

M 1 6 3 2

USER MANUAL

Seiko Instruments Inc.

PREFACE

This manual describes technical informations on functions and instructions of M1632 from Seiko Instruments Inc. Please read this instruction manual carefully to understand all the module functions and make the best use of them. Description details may be changed without notice.

Revision Record

Edition	Revision	Date
1	Original	April 1985
2	Completely revised	Jan. 1987

Printed in Japan

ENERAL

1 General

The M1632 is a low-power-consumption dot-matrix liquid crystal display (LCD) module with a high-contrast wide-view TN LCD panel and a CMOS LCD drive controller built in. The controller has a built-in character generator ROM/RAM, and display data RAM. All the display functions are controlled by instructions and the module can easily be interfaced with an MPU. This makes the module applicable to a wide range of purposes including terminal display units for microcomputers and display units for measuring gages.

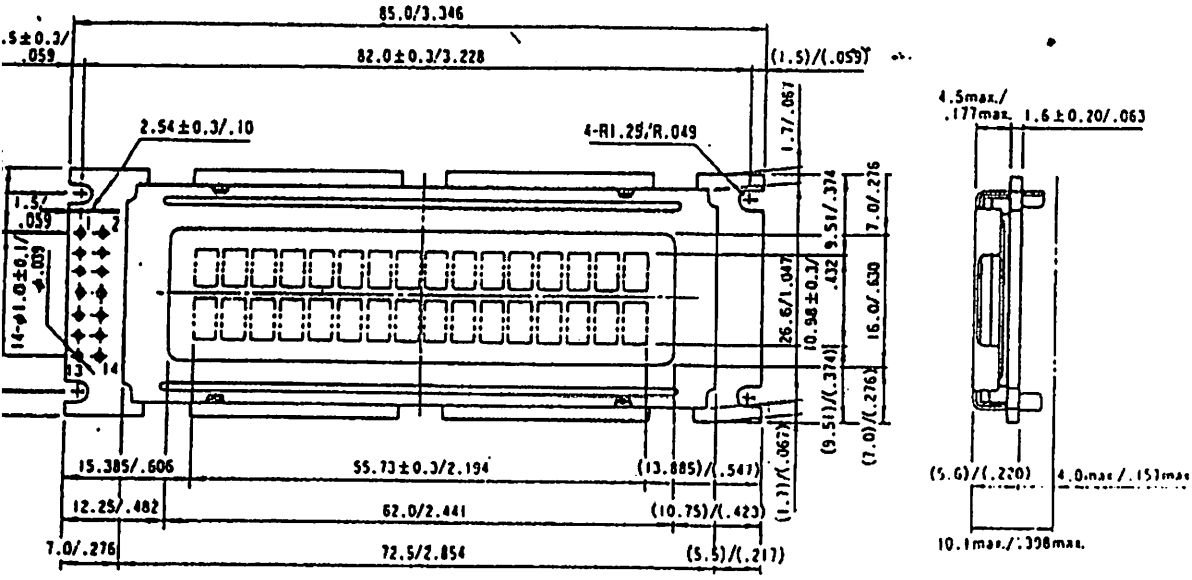
Features

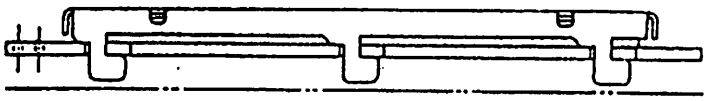
- 16-character, two-line TN liquid crystal display of 5 x 7 dot matrix + cursor
- Duty ratio: 1/16
- Character generator ROM for 192 character types.
  (character font: 5 x 7 dot matrix)
- Character generator RAM for eight character types (program write)
  (character font: 5 x 7 dot matrix)
- 80 x 8 bit display data RAM (80 characters maximum)
- Interface with four-bit and eight-bit MPUs possible
- Display data RAM and character generator RAM readable from MPU
- Many instruction functions

  Display Clear, Cursor Home, Display ON/OFF, Cursor ON/OFF, Display Character Blink, Cursor Shift, and Display Shift

- Built-in oscillator circuit
- +5 V single power supply
- Built-in automatic reset circuit at power-on
- CMOS process
- Operating temperature range: 0°C to 50°C

Dimensions Diagram





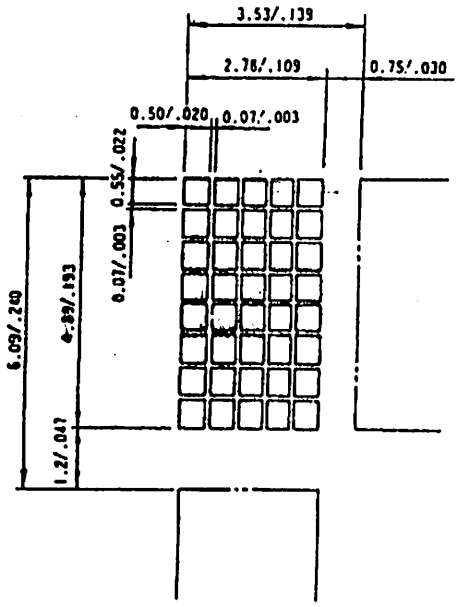
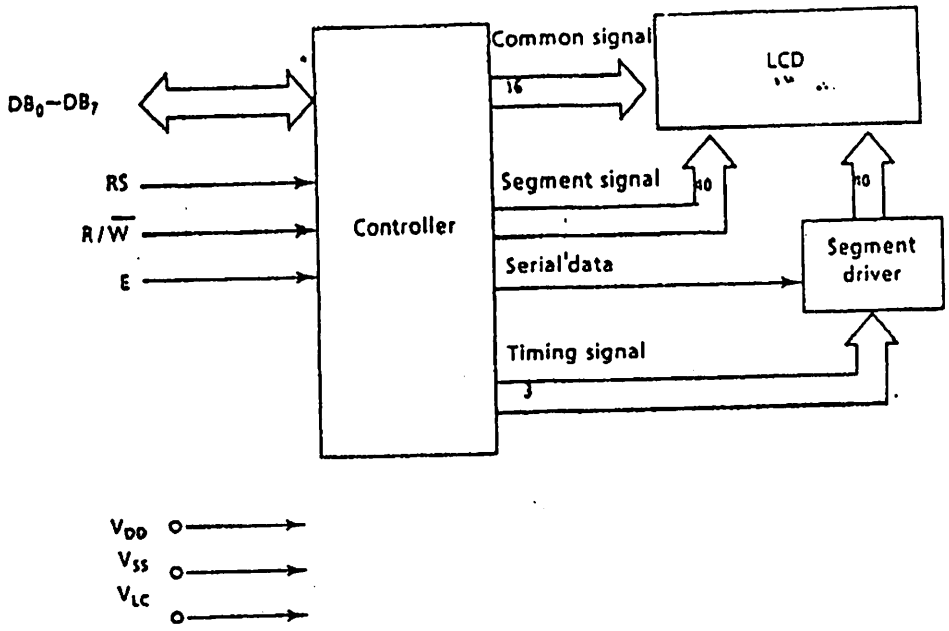


Figure 1 Dimensions diagram

Unit : mm/inch
General tolerance : ± 0.5 mm

No.	Symbol	Level	Function	
1	Vss	-	Power Supply	0V (GND)
2	Vcc	-		5V ±10%
3	Vee	-		for LCD Drive
4	RS	H/L	H: Data Input L: Instruction Input	
5	R/W	H/L	H:READ L:WRITE	
6	E	H, ↓	Enable Signal	
7	DB0	H/L	Data Bus	
8	DB1	H/L		
9	DB2	H/L		
10	DB3	H/L		
11	DB4	H/L		
12	DB5	H/L		
13	DB6	H/L		
14	DB7	H/L		
15	V+ BL	-	Back Light Supply	4 - 4.2V 50-200mA
16	V- BL	-		0V (GND)

ıck Diagram


Common signal
LCD
16
DB0–DB7
RS
R/W
E
Controller
Segment signal
40
40
Serial data
Segment driver
Timing signal
3
VDD
VSS
VLC

solute Maximum Ratings

V_{SS} = 0 V

Item	Symbol	Standard	Unit	Remarks
Power supply voltage	V_{DD}	− 0.3 to + 7.0	V	
	V_{LC}	V_{DD} − 13.5 to V_{DD} + 0.3	V	
Input voltage	V_{in}	− 0.3 to V_{DD} + 0.3,	V	
Operating temperature	T_{opr}	0 to + 50	°C	
Storage temperature	T_{stg}	− 20 to + 60	°C	At 50% RH

ctrical Characteristics

V_{DD} = 5 V ± 5%, V_{SS} = 0 V, T_A = 0°C to 50°C

Item		Symbol	Conditions	Standard			Unit
				Min.	Typ.	Max.	
Input voltage	High	V_{IH1}		2.2	−	V_{DD}	V
	Low	V_{IL1}		0	−	0.6	V
Output voltage (TTL)	High	V_{OH1}	$-I_{OH}$ = 0.205 mA	2.4	−	−	V
	Low	V_{OL1}	I_{OL} = 1.2 mA	−	−	0.4	V
Output voltage (CMOS)	High	V_{OH2}	$-I_{OH}$ = 0.04 mA	0.9V_{DD}	−	−	V
	Low	V_{OL2}	I_{OL} = 0.04 mA	−	−	0.1V_{DD}	V
Power supply voltage		V_{DD}		4.75	5.00	5.25	V
		$-V_{LC}$	V_{DD} = 5 V, T_A = 25°C	−	0.25	−	V
Current consumption		I_{DD}		−	2.0	3.0	mA
		I_{LC}	V_{LC} = 0.25V	−	−	1.0	mA
Clock oscillation freq.		f_{osc}	Resistance oscillation	190	270	350	kHz

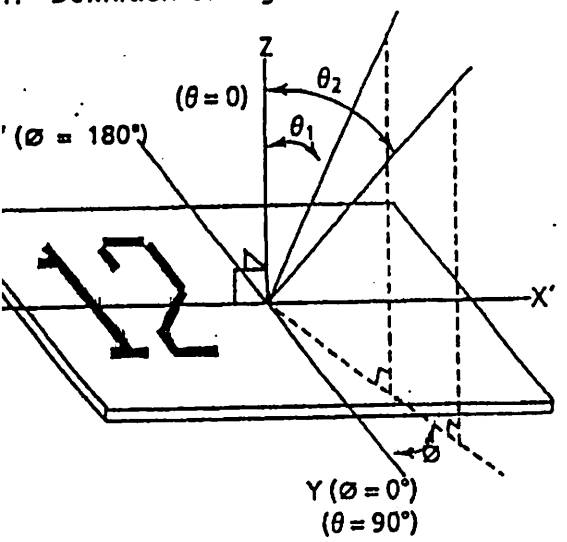
ptical Characteristics

1 Optical characteristics

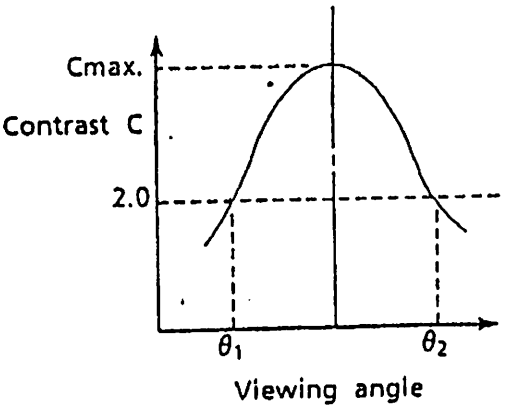
Maximum viewing angle: 6 o'clock ($\varnothing$ = 0°)
T_A = 25°C, V_{opr} = 4.75 V

Item	Symbol	Conditions	Min.	Typ.	Max.	Remarks
Viewing angle	$\theta_2 - \theta_1$	$C \geq 2.0$, $\varnothing = 0°$	35	–	–	See Notes 1 and 2.
Contrast	C	$\theta = 25°$, $\varnothing = 0°$	5	8	–	See Note 3.
Rise time	t_{on}	$\theta = 25°$, $\varnothing = 0°$	–	60 ms	70 ms	See Note 4.
Fall time	t_{off}	$\theta = 25°$, $\varnothing = 0°$	–	150 ms	170 ms	See Note 4.

1: Definition of angles $\varnothing$ and θ

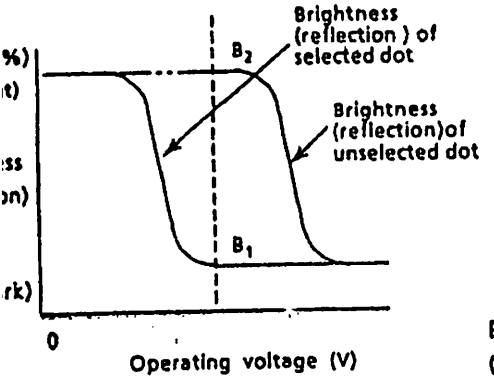


Note 2: Definition of viewing angles θ_1 and θ_2

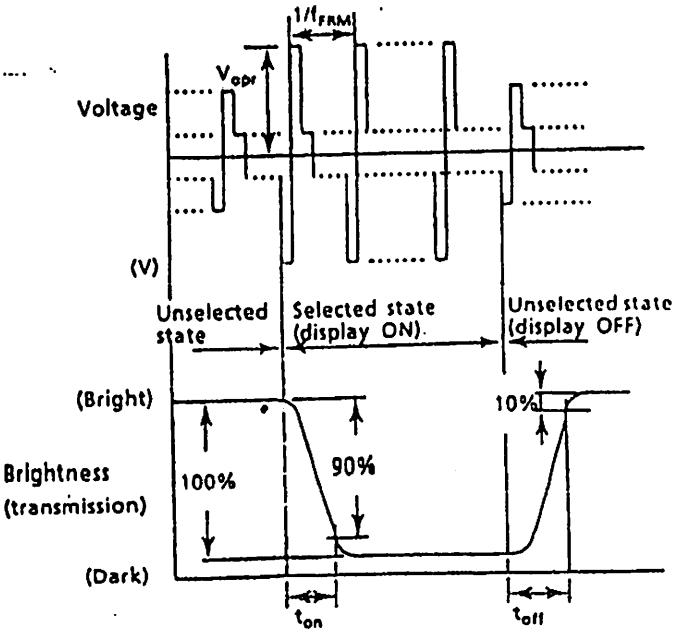


te 3: Definition of contrast C

Brightness (reflection) of unselected dot (B2)
Brightness (reflection) of selected dot (B1)



Note 4: Definition of response time



V_{opr} : Operating voltage (V)
f_{FRM} : Frame frequency (Hz)
t_{on} : Response time (rise)(ms)
t_{off} : Response time (fall)(ms)

Recommended operating voltage

The viewing angle and screen contrast of the LCD panel can be varied by changing the liquid crystal operating voltage (V_{opr}), that is V_{LC}.

The optical characteristics is influenced by an ambient temperature. The recommended value of V_{opr} for an ambient temperatures are shown below.

Temperature (℃)	0	10	25	40	50
Voltage V_{opr} (V)	5.00	4.90	4.75	4.60	4.50

$V_{opr} = V_{DD} - V_{LC}$

ATING INSTRUCTIONS

erminal Functions

Table 1 Terminal functions

ame	No. of terminals	I/O	Destination	Function
DB_3	4	I/O	MPU	Tristate bidirectional lower four data buses: Data is read from the module to the MPU or written to the module from the MPU through the buses. If the interface data is 4 bits, the signals are not used.
DB_7	4	I/O	MPU	Tristate bidirectional upper four data buses: Data is read from the module to the MPU or written to the module from the MPU through the buses. DB_7 is also used as a busy flag.
	1	Input	MPU	Operation start signal: The signal activates data write or read.
$\overline{V}$	1	Input	MPU	Read (R) and Write ($\overline{W}$) selection signals 0 : Write 1 : Read
	1	Input	MPU	Register selection signals 0 : Instruction register (Write) Busy flag and address counter (Read) 1 : Data register (Write and Read)
C	1	–	Power supply	Power supply terminal for driving liquid crystal display: The screen contrast can be varied by changing V_{LC}.
D	1	–	Power supply	+5 V
S	1	–	Power supply	Ground terminal: 0 V

asic Operations

l Registers

The controller has two kinds of eight-bit registers: the instruction register (IR) and the data register (DR). They are selected by the register select (RS) signal as shown in Table 2.

The IR stores instruction codes such as Display Clear and Cursor Shift, and the address information of display data RAM (DD RAM) and character generator RAM (CG RAM). They can be written from the MPU, but cannot be read to the MPU.

The DR temporarily stores data to be written into DD RAM or CG RAM, or read from DD RAM or CG RAM. When data is written into DD RAM or CG RAM from the MPU, the data in the DR is automatically written into DD RAM or CG RAM by internal operation. However, when data is read from DD RAM or CG RAM, the necessary data address is written into the IR. The specified data is read out to the DR and then the MPU reads it from the DR. After the read operation, the next address is set and DD RAM or CG RAM data at the address is read into the DR for the next read operation.

Table 2 Register selection

	R/$\overline{W}$	Operation
	0	IR selection, IR write. Internal operation : Display clear
	1	Busy flag (DB_7) and address counter (DB_0 to DB_6) read
	0	DR selection, DR write. Internal operation : DR to DD RAM or CG RAM
	1	DR selection, DR read. Internal operation : DD RAM or CG RAM to DR

.2 Busy flag (BF)

The flag indicates whether the module is ready to accept the next instruction. As shown in Table 2, the signal is output to DB_7 if RS = 0 and R/$\overline{W}$ = 1. If the value is 1, the module is working internally and the instruction cannot be accepted. If the value is 0, the next instruction can be written. Therefore, the flag status needs to be checked before executing an instruction. If an instruction is executed without checking the flag status, wait for more than the execution time shown by 2.4 Instruction Outline.

Address counter (AC)

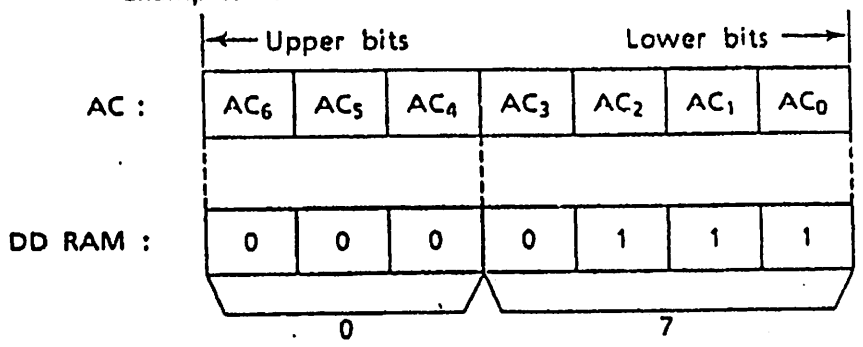
The counter specifies an address when data is written into DD RAM or CG RAM and the data stored in DD RAM or CG RAM is read out. If an Address Set instruction (for DD RAM or CG RAM) is written in the IR, the address information is transferred from the IR to the AC. When display data is written into or read from DD RAM or CG RAM, the AC is automatically incremented or decremented by one according to the Entry Mode Set. The contents of the AC are output to DB_0 to DB_6 as shown in Table 2 if RS = 0 and $R/\overline{W}$ = 1.

Display data RAM (DD RAM)

DD RAM has a capacity of up to 80 × 8 bits and stores display data of 80 eight-bit character codes. Some storage areas of DD RAM which are not used for display can be used as general data RAM.

A DD RAM address to be set in the AC is expressed in hexadecimal form as follows.

Example: DD RAM address = 07



00_H to $0F_H$ of the DD RAM address is set in the line 1, and 40_H to $4F_H$ in the line 2.

Note : The addresses in the digit 16 of line 1 and the digit 1 of line 2 are not consecutive.

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	Display digit
1	00	01	02	03	04	05	06	07	08	09	0A	0B	0C	0D	0E	0F	DD RAM address
2	40	41	42	43	44	45	46	47	48	49	4A	4B	4C	4D	4E	4F	

If the display is shifted, DD RAM address 00H to 27H are displayed in line 1 and 40H to 67H in line 2. The following figures are examples of display shifts.

*Left shift

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	Display digit
1	01	02	03	04	05	06	07	08	09	0A	0B	0C	0D	0E	0F	10	DD RAM address
2	41	42	43	44	45	46	47	48	49	4A	4B	4C	4D	4E	4F	50	

*Right shift

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	Display digit
1	27	00	01	02	03	04	05	06	07	08	09	0A	0B	0C	0D	0E	DD RAM address
2	67	40	41	42	43	44	45	46	47	48	49	4A	4B	4C	4D	4E	

Character generator ROM (CG ROM)

Character generator ROM generates 192 types of 5 x 7 dot-matrix character patterns from eight-bit character codes.

Table 3 shows the correspondence between the CG ROM character codes and character patterns.

Character generator RAM (CG RAM)

CG RAM is used to create character patterns freely by programming. Eight types character patterns can be written.

Table 4 shows the character patterns created from CG RAM addresses and data. To display a created character pattern, the character code in the left column of the table is written into DD RAM corresponding to the display position (digit). The areas not used for display are available as general data RAM.

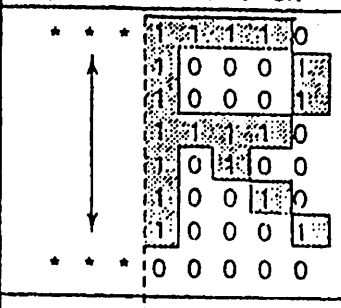
Table 3 Correspondence between character codes and character patterns

it / lit	0 0000	2 0010	3 0011	4 0100	5 0101	6 0110	7 0111	1010	1011	1100	1101	1110	1111
0	CG RAM (1)												
1	(2)												
0	(3)												
1	(4)												
00	(5)												
01	(6)												
10	(7)												
11	(8)												
00	(1)												
01	(2)												
10	(3)												
11	(4)												
00	(5)												
01	(6)												
10	(7)												
11	(8)												

Table 4 Relationships between CG RAM addresses and character codes (DD RAM) and character patterns (CG RAM data)

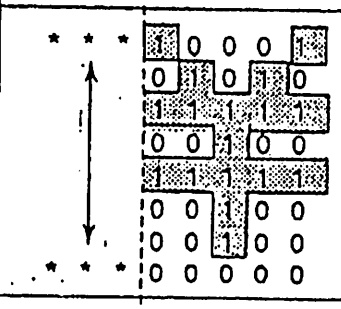
aracter code D RAM data)	CG RAM address	Character pattern (CG RAM data)
5 4 3 2 1 0 bit Lower bit →	5 4 3 ←Upper bit	2 1 0 Lower bit →
0 0 * 0 0 0	0 0 0	0 0 0 0 0 1 0 1 0 0 1 1 1 0 0 1 0 1 1 1 0 1 1 1
0 0 * 0 0 1	0 0 1	0 0 0 0 0 1 0 1 0 0 1 1 1 0 0 1 0 1 1 1 0 1 1 1
		0 0 0 0 0 1
0 0 * 1 1 1	1 1 1	1 0 0 1 0 1 1 1 0 1 1 1

7 6 5 4 3 2 1 0 ←Upper bit Lower bit →



Example of character pattern (R)

← Cursor position



Example of character pattern (¥)

otes:
- In CG RAM data, 1 corresponds to Selection and 0 to Non-selection on the display.
- Character code bits 0 to 2 and CG RAM address bits 3 to 5 correspond with each other (three bits, eight types).
- CG RAM address bits 0 to 2 specify a line position for a character pattern. Line 8 of a character pattern is the cursor position where the logical sum of the cursor and CG RAM data is displayed. Set the data of line 8 to 0 to display the cursor. If the data is changed to 1, one bit lights, regardless of the cursor.

The character pattern column positions correspond to CG RAM data bits 0 to 4 and bit 4 comes to the left end. CG RAM data bits 5 to 7 are not displayed but can be used as general data RAM.

When reading a character pattern from CG RAM, set to 0 all of character code bits 4 to 7. Bits 0 to 2 determine which pattern will be read out. Since bit 3 is not valid, 00_H and 08_H select the same character.

ing Characteristics

Write timing characteristics

V_{DD} = 5.0 V ± 5%, V_{SS} = 0 V, T_A = 0°C to 50°C

Item		Symbol	Standard		Unit
			Min.	Max.	
nable cycle time		$t_{CYC}E$	1000	–	ns
nable pulse width	High level	PW_{EH}	450	–	ns
nable rise and fall time		t_{Er},t_{Ef}	–	25	ns
etup time	RS, R/$\overline{W}$ — E	t_{AS}	140	–	ns
ddress hold time		t_{AH}	10	–	ns
ata setup time		t_{DSW}	195	–	ns
ata hold time		t_H	10	–	ns

e operation

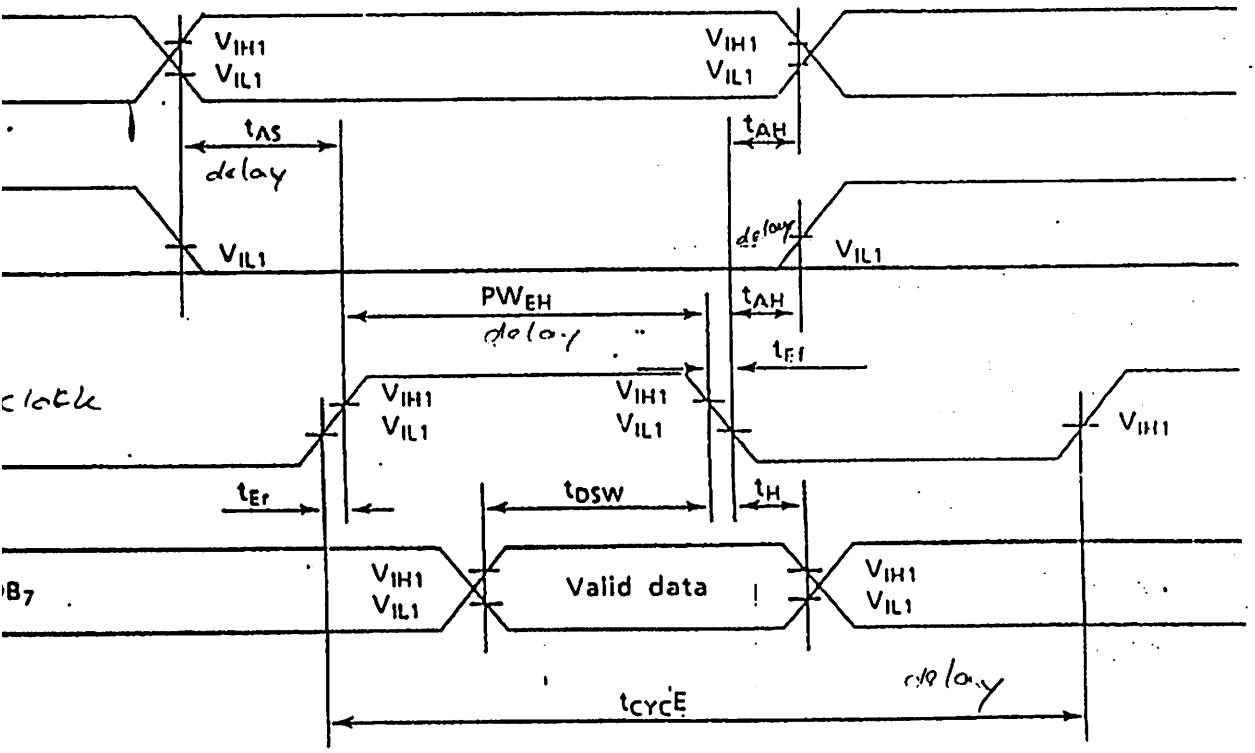


Figure 3 Data write from MPU to module

2 Read timing characteristics

V_{DD} = 5.0 V ± 5%, V_{SS} = 0 V, T_A = 0°C to 50°C

Item		Symbol	Standard		Unit
			Min.	Max.	
Enable cycle time		t_{CYCE}	1000	–	ns
Enable pulse width	High level	PW_{EH}	450	–	ns
Enable rise and fall time		t_{Er},t_{Ef}	–	25	ns
Setup time	RS, R/$\overline{W}$—E	t_{AS}	140	–	ns
Address hold time		t_{AH}	10	–	ns
Data delay time		t_{DDR}	–	320	ns
Data hold time		t_{H}	20	–	ns

d operation

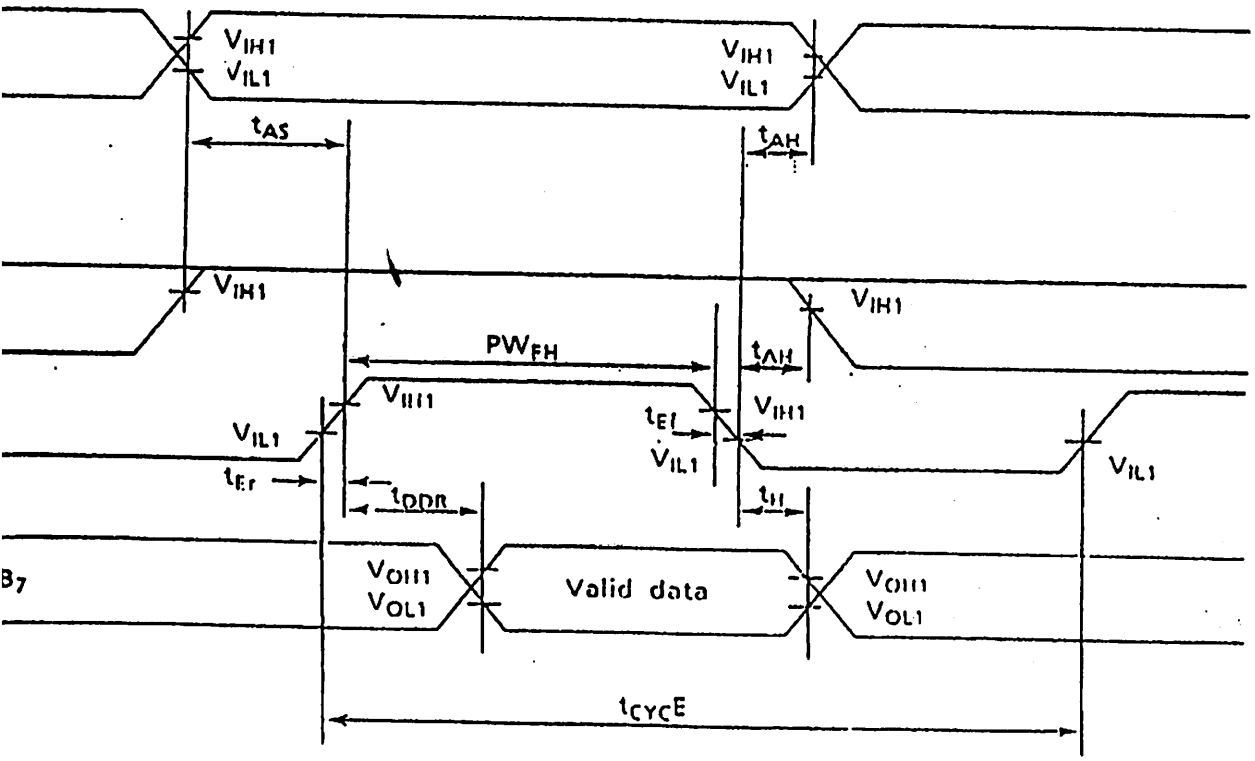


Figure 4 Data read from module to MPU

ruction Outline

Table 5 List of instructions

tion	Code										Function	Execution time
	RS	R/W	DB_7	DB_6	DB_5	DB_4	DB_3	DB_2	DB_1	DB_0		
ear	0	0	0	0	0	0	0	0	0	1	Clears all display and returns cursor to home position (address 0)	1.64 ms
me	0	0	0	0	0	0	0	0	1	•	Returns cursor to home position. Shifted display retutns to home position and DD RAM contents do not change.	1.64 ms
le Set	0	0	0	0	0	0	0	1	I/D	S	Sets direction of cursor movement and whether display will be shifted when data is written or read	40 µs
N / OFF	0	0	0	0	0	0	1	D	C	B	Turns ON/OFF total display (D) and cursor (C), and makes cursor position column start blinking (B)	40 µs
play Shift	0	0	0	0	0	1	S/C	R/L	•	•	Moves cursor and shifts display without changing DD RAM contents	40 µs
Set	0	0	0	0	1	DL	1	•	•	•	Sets interface data length (DL)	40 µs
Address	0	0	0	1	A_{CG}						Sets CG RAM address to start transmitting or receiving CG RAM data	40 µs
Address	0	0	1	A_{DD}							Sets DD RAM address to start transmitting or receiving DD RAM data	40 µs
Read	0	1	BF	AC							Reads BF indicating module in internal operation and AC contents (used for both CG RAM and DD RAM)	0 µs
ite to CG DD RAM	1	0	Write Data								Writes data into DD RAM or CG RAM	40 µs
ad from or DD	1	1	Read Data								Reads data from DD RAM or CG RAM	40 µs

t
M address
M address

I/D = 1 : Increment
I/D = 0 : Decrement

S = 1 : Display shift
S = 0 : No display shift

D = 1 : Display ON
D = 0 : Display OFF

C = 1 : Cursor ON
C = 0 : Cursor OFF

B = 1 : Blink ON
B = 0 : Blink OFF

S/C = 1 : Display shift
S/C = 0 : Cursor movement

R/L = 1 : Right shift
R/L = 0 : Left shift

DL = 1 : 8 bits
DL = 0 : 4 bits

BF = 1 : Internal operation in progress
BF = 0 : Instruction can be accepted

uction Details

splay Clear

	RS	R/$\overline{W}$	DB_7							DB_0
Code	0	0	0	0	0	0	0	0	0	1

Display Clear clears all display and returns cursor to home position (address 0). Space code 20 (hexadecimal) is written into all the addresses of DD RAM, and DD AM address 0 is set to the AC. If shifted, the display returns to the original osition. After execution of the Display Clear instruction, the entry mode is cremented.

Note : When executing the Display Clear instruction, follow the restrictions listed in Table 6.

ursor Home

	RS	R/$\overline{W}$	DB_7							DB_0
Code	0	0	0	0	0	0	0	0	1.	*

* : Invalid bit

Cursor Home returns cursor to home position (address 0).

DD RAM address 0 is set to the AC. The cursor returns to the home position. If hifted, the display returns to the original position. The DD RAM contents do not hange. If the cursor or blinking is ON, it returns to the left side.

Note : When executing the Cursor Home instruction, follow the restrictions listed in Table 6.

ble 6 Restrictions on execution of Display Clear and Cursor Home instructions

Conditions of use	Restrictions
en executing the Display Clear or Cursor ne instruction when the display is ted (after execution of Display Shift ruction)	The Cursor Home instruction should be executed again immediately after the Display Clear or Cursor Home instruction is executed. Do not leave an interval of a multiple of $400/f_{osc}$* second after the first execution. Example: 1.5 ms, 3 ms, 4.5 ms for f_{osc} = 270 kHz *f_{osc}: Oscillation frequency
en 23_H, 27_H, 63_H, or 67_H is used as a DD M address to execute Cursor Home truction	Before executing the Cursor Home instruction, the data of the four DD RAM addresses given at the left should be read and saved. After execution, write the data again in DD RAM. (This restriction is necessary to prevent the contents of the DD RAM addresses from being destroyed after the Cursor Home instruction has been executed.)

Entry Mode Set

	RS	R/W	DB_7							DB_0
Code	0	0	0	0	0	0	0	1	I/D	S

Entry Mode Set sets the direction of cursor movement and whether display will be shifted.

I/D : The DD RAM address is incremented or decremented by one when a character code is written into or read from DD RAM. This is also true for writing into or reading from CG RAM.

When I/D = 1, the address is incremented by one and the cursor or blink moves to the right.

When I/D = 0, the address is decremented by one and the cursor or blink moves to the left.

S : If S = 1, the entire display is shifted either to the right or left for writing into DD RAM. The cursor position does not change, only the display moves. There is no display shift for reading from DD RAM.

When S = 1 and I/D = 1, the display shifts to the left.
When S = 1 and I/D = 0, the display shifts to the right.

If S = 0, the display does not shift.

Display ON/OFF Control

	RS	R/W	DB_7							DB_0
Code	0	0	0	0	0	0	1	D	C	B

Display ON/OFF Control turns the total display and the cursor ON and OFF, and makes the cursor position start blinking. Cursor ON/OFF and blinking is done at the column indicated by the specified DD RAM address by the AC.

D : When D = 1, the display is turned ON.
When D = 0, the display is turned OFF.
If D = 0 is used, display data remains in DD RAM. Change 0 to 1 to display data.

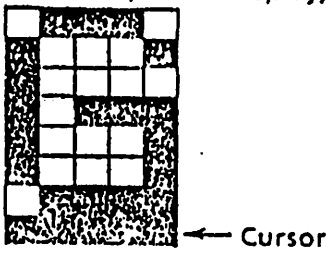
C : When C = 1, the cursor is displayed.
When C = 0, the cursor is not displayed.

The cursor is displayed in the dot line below the 5 x 7 dot-matrix character fonts. If the cursor is OFF, display data is written into DD RAM in the order specified by I/D.

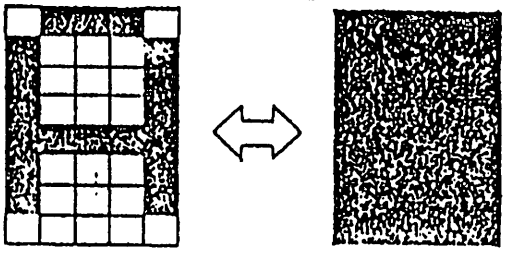
B : When B = 1, the character at the cursor position starts blinking.
When B = 0, it does not blink.

For blinking, all-black dots and the character are switched about every 0.4 seconds. The cursor and blinking can be set at the same time.

Example: C = 1 (cursor display)



B = 1 (blinking)



ırsor/Display Shift

	RS	R/$\overline{W}$	DB_7							DB_0
Code	0	0	0	0	0	1	S/C	R/L	*	*

* :Invalid bit

Cursor/Display Shift moves the cursor and shifts the display without changing the) RAM contents.

The cursor position and the AC contents match. This instruction is available for ;play correction and retrieval because the cursor position or display can be shifted thout writing or reading display data. Since the DD RAM capacity is 40-character d two lines, the cursor is shifted from digit 40 of line 1 to digit 1 of line 2. splays of lines 1 and 2 are shifted at the same time. Therefore, the display ttern of line 2 is not shifted to line 1.

S/C	R/L	Operation
0	0	The cursor position is shifted to the left (the AC decrements one).
0	1	The cursor position is shifted to the right (the AC increments one).
1	0	The entire display is shifted to the left with the cursor.
1	1	The entire display is shifted to the right with the cursor.

Note: If only display shift is done, the AC contents do not change.

ıction Set

	RS	R/W	DB7						DB0
Code	0	0	0	0	1	DL	1	*	*	*

* : Invalid bit

ıction Set sets the interface data length.

)L : Interface data length

When DL = 1, the data length is set at eight bits (DB_7 to DB_0).

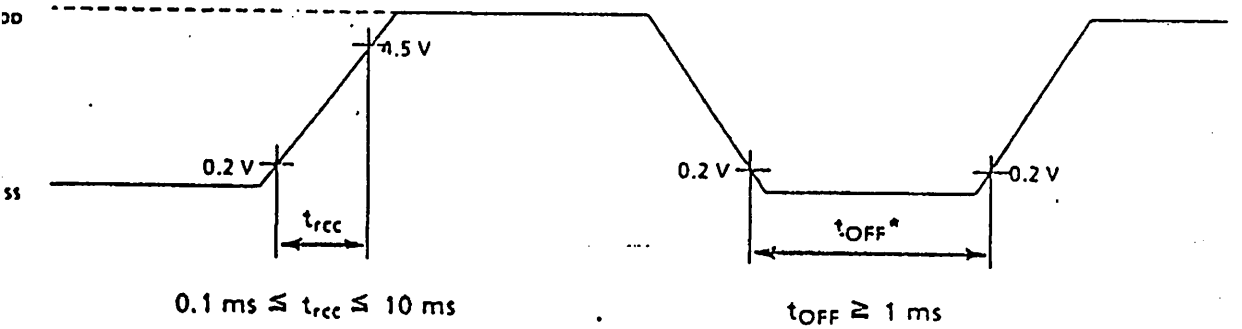
When DL = 0, the data length is set at four bits (DB_7 to DB_4).

The upper four bits are transferred first, then the lower four bits follow.

'he Function Set instruction must be executed prior to all other instructions ept for Busy Flag/Address Read. If another instruction is executed first, no ction instruction except changing the interface data length can be executed.

narks: Initialization

he system is automatically initialized at power-on if the following power supply ditions are satisfied.



0.1 ms ≤ t_{rcc} ≤ 10 ms

t_{OFF} ≥ 1 ms

*t_{OFF}: Time when power supply is OFF if cut instantaneously or turned ON and OFF repeatedly

llowing instructions are executed for initialization.

x 7 dot-matrix character font: 1/8 duty

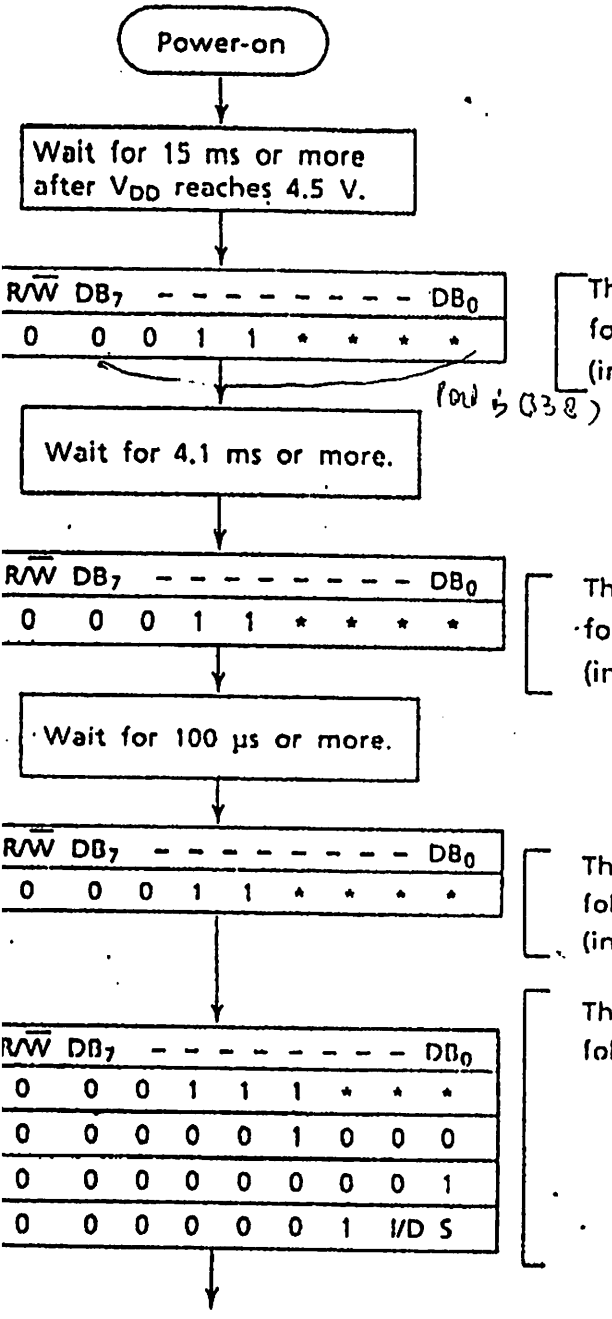
isplay clear

unction Set	DL = 1: Interface data length: 8 bits
)ispiny ON/OFF Control	D = 0: Display OFF C = 0: Cursor OFF B = 0: Blink OFF
;ntry mode	I/O = 1: Increment S = 0: No display shift

ce the condition is not suitable for the M1632, further function setting is sary.

ıutomatic initialization is not executed because the above power supply tions are not satisfied, use the instruction from next page on.

Interface data length : Eight bits



The busy flag cannot be checked before the following instruction: Function Set (interface data length: 8 bits)

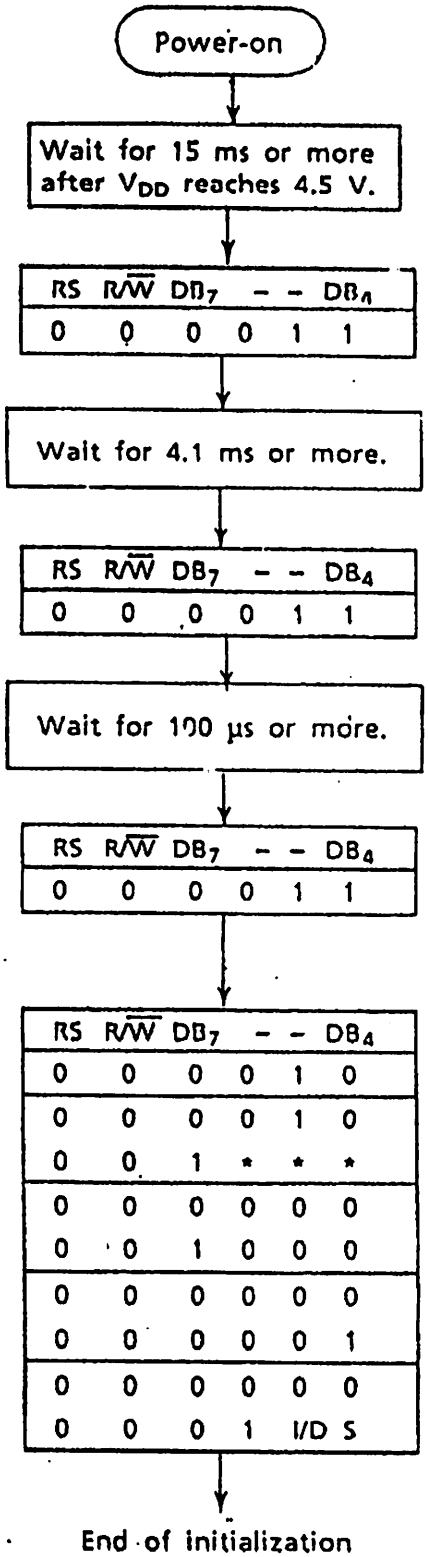
The busy flag cannot be checked before the following instruction: Function Set (interface data length: 8 bits)

The busy flag cannot be checked before the following instruction: Function Set (interface data length: 8 bits)

The busy flag can be checked from the following instructions.

- Function Set
- Display OFF
- Display Clear
- Entry Mode Set

terface data length: Four bits



The busy flag cannot be checked before the following instruction: Function Set (interface data length: 8 bits)

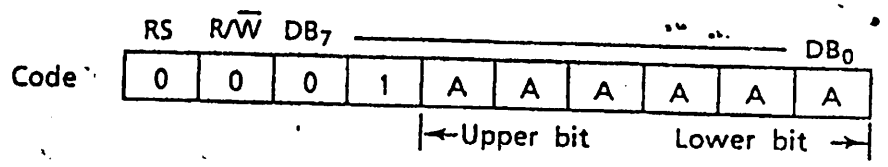
The busy flag cannot be checked before the following instruction: Function Set (interface data length: 8 bits)

The busy flag cannot be checked before the following instruction: Function Set (interface data length: 8 bits)

The busy flag can be checked from the following instructions.

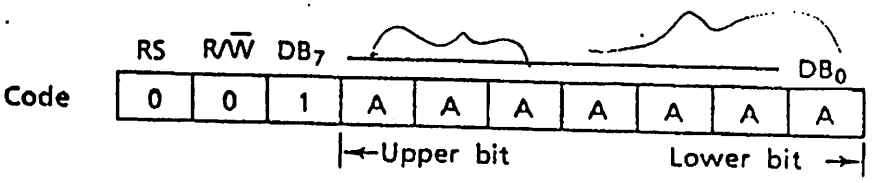
- Function Set (interface data length: 4 bits)
- Function Set
- Display OFF
- Display Clear
- Entry Mode Set

RAM Address Set



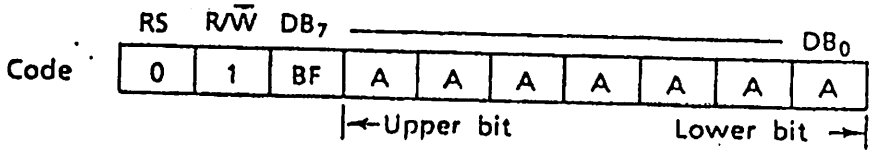
RAM addresses expressed as binary AAAAAA are set to the AC. Then data in RAM is written from or read to the MPU.

RAM Address Set



RAM addresses expressed as binary AAAAAAA are set to the AC. Then data RAM is written from or read to the MPU. The addresses used for display in (AAAAAAA) are 00_H to 27_H and those for line 2 (AAAAAAA) are 40_H to 67_H.

Flag/Address Read



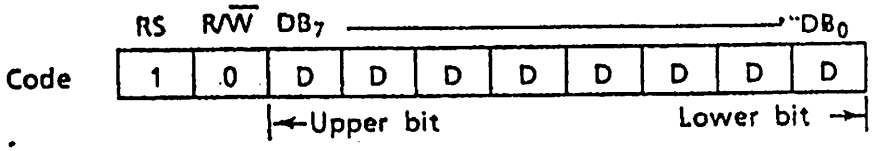
BF signal is read out, indicating that the module is working internally because previous instruction.

n BF = 1, the module is working internally and the next instruction cannot be accepted until the BF value becomes 0.

n BF = 0, the next instruction can be accepted.

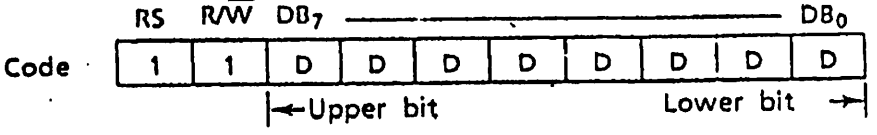
refore, make sure that BF = 0 before writing the next instruction. The AC of binary AAAAAAA are read out at the same time as reading the busy flag. C addresses are used for both CG RAM and DD RAM but the address set execution of the instruction determines which address is to be used.

a Write to CG RAM or DD RAM



inary eight-bit data DDDDDDDD is written into CG RAM or DD RAM. The CG M. Address Set instruction of (7) or the DD RAM Address Set instruction of (8) ore this instruction selects either RAM. After the write operation, the address l display shift are determined by the entry mode setting.

ta Read from CG RAM or DD RAM



Binary eight-bit data DDDDDDDD is read from CG RAM or DD RAM. The CG AM Address Set instruction of (7) or the DD RAM Address Set instruction of (8) fore this instruction selects either RAM. In addition, either instruction (7) or (8) ist be executed immediately before this instruction. If no address set instruction executed before a read instruction, the first data read becomes invalid. If read structions are executed consecutively, data is normally read from the second time. owever, if the cursor is shifted by the Cursor Shift instruction when reading DD AM, there is no need to execute an address set instruction because the Cursor Shift struction does this.

ter the read operation, the address is automatically incremented or decremented one according to the entry mode, but the display is not shifted.

Note : The AC is automatically incremented or decremented by one according to the entry mode after a write instruction is executed to write data in CG RAM or DD RAM. However, the data of the RAM selected by the AC are not read out even if a read instruction is executed immediately afterwards.

Correct data is read out under the following conditions.

- An address set instruction is executed immediately before readout.
- For DD RAM, the Cursor Shift instruction is executed immediately before readout.
- The second, or later, instruction is executed in consecutive execution of read instructions.

nples of Instruction Use

:erface data length: Eight bits

Instruction	Display	Operation
ower-on tS R/W DB_7 —— DB_0		The built-in reset circuit initializes the module.
nction Set ✓ :S R/W DB_7 —— DB_0) 0 0 0 1 1 1 * * *		The interface data length is set to 8 bits. The character format becomes 5 x 7 dot-matrix at 1/16 duty cycle.
;play ON/OFF Control :S R/W DB_7 —— DB_0) 0 0 0 0 0 1 1 1 0	_	The display and cursor are turned ON, but nothing is displayed.
try Mode Set S R/W DB_7 —— DB_0) 0 0 0 0 0 0 1 1 0	_	The address is incremented by one and the cursor shifts to the right in a write operation to internal RAM. The display is not shifted.
ite to CG RAM or DD RAM S R/W DB_7 —— DB_0 0 1 0 0 1 1 0 0	L_	L is written. The AC is incremented by one and the cursor shifts to the right.
ite to CG RAM or DD RAM ; R/W DB_7 —— DB_0 0 1 0 0 0 0 1 1	LC_	C is written.
⋮	⋮	
ite to CG RAM or DD RAM S R/W DB_7 —— DB_0 0 0 1 1 0 0 1 0	LCD MODULE M1632	2 is written in digit 16. Cursor disappears.

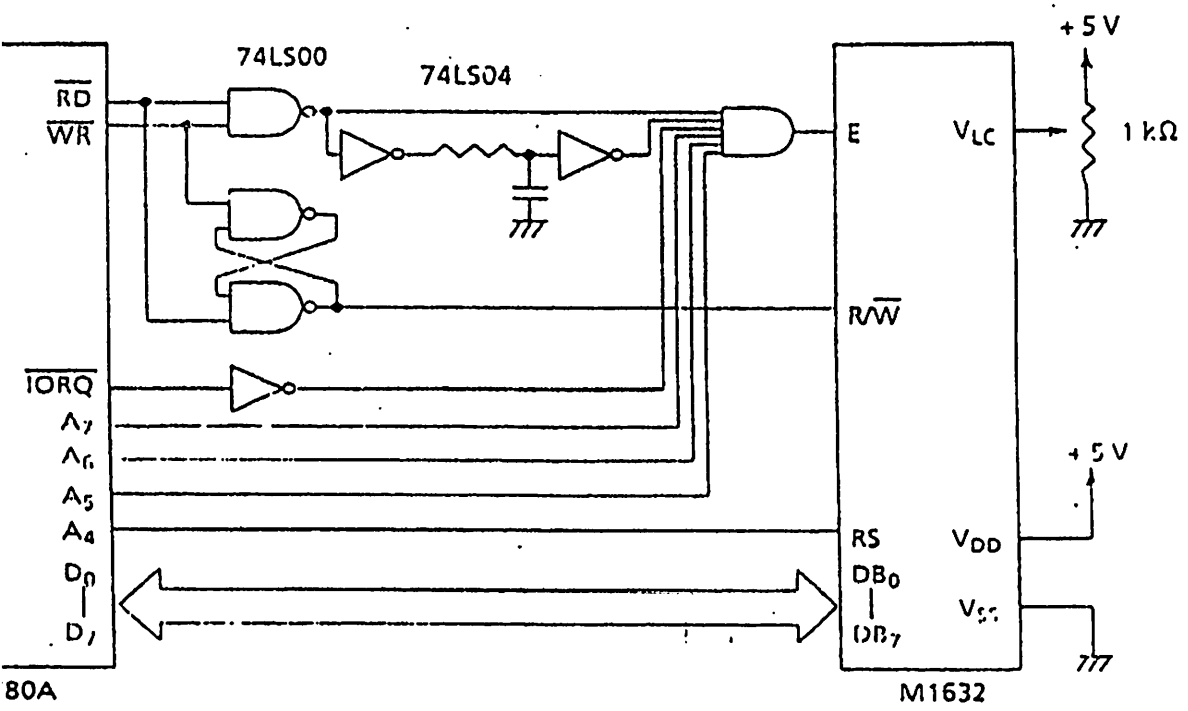
Instruction	Display	Operation
) RAM address set RS: 0 R/W: 0 DB7 —— DB0: 1 1 0 0 0 0 0 0	LCD MODULE M1632 _	The DD RAM address is set so that the cursor appears at digit 1 of line 2.
rite to CG RAM or DD RAM RS: 1 R/W: 0 DB7 —— DB0: 0 0 1 1 0 0 0 1	LCD MODULE M1632 1_	1 is written.
ite to CG RAM or DD RAM RS: 1 R/W: 0 DB7 —— DB0: 0 0 1 1 0 1 1 0	LCD MODULE M1632 16_	6 is written.
⋮	⋮	
ite to CG RAM or DD RAM RS: 1 R/W: 0 DB7 —— DB0: 0 1 0 1 0 0 1 1	LCD MODULE M1632 16DIGITS,2LINES	S is written.
) RAM address set RS: 0 R/W: 0 DB7 —— DB0: 1 0 0 0 0 0 0 0	LCD MODULE M1632 16DIGITS,2LINES	The cursor returns to the home position.
splay clear RS: 0 R/W: 0 DB7 —— DB0: 0 0 0 0 0 0 0 1	_	All the display disappears and the cursor remains at the home position.
⋮	⋮	

Interface data length: Four bits

Instruction	Display	Operation
Power-on RS | R/W | DB_7 — DB_4		The built-in reset circuit initializes the module.
Function Set RS | R/W | DB_7 — DB_4 0 | 0 | 0 0 1 0		Four-bit operation mode is set. *Eight-bit operation mode is set by initialization, and the instruction is executed only once.
Function Set RS | R/W | DB_7 — DB_4 0 | 0 | 0 0 1 0 0 | 0 | 1 * * *		The 4-bit operation mode, 1/16 duty cycle, and 5 x 7 dot-matrix character format are selected. Then 4-bit operation mode starts.
Display ON/OFF Control RS | R/W | DB_7 — DB_4 0 | 0 | 0 0 0 0 0 | 0 | 1 1 1 0	_	The display and cursor are turned ON, but nothing is displayed.
Entry Mode Set RS | R/W | DB_7 — DB_4 0 | 0 | 0 0 0 0 0 | 0 | 0 1 1 0	_	The address is incremented by one and the cursor shifts to the right in a write operation to internal RAM. The display is not shifted.
Write to CG RAM or DD RAM. RS | R/W | DB_7 — DB_4 1 | 0 | 0 1 0 0 1 | 0 | 1 1 0 0	L_	L is written. the AC is incremented by one and the cursor shifts to the right.

nnection Diagrams

80A



80A and 8255A