INSTITUT TEKNOLOGI NASIONAL MALANG
FAKULTAS TEKNOLOGI INDUSTRI
JURUSAN TEKNIK ELEKTRO S-1
KONSENTRASI TEKNIK ELEKTRONIKA

SKRIPSI

PERENCANAAN DAN PEMBUATAN TELETHERMAL DENGAN MENGGUNAKAN INFRA RED

Disusun Oleh :
YUDI PURNOMO
00.17.246

MARET 2006

LEMBAR PERSETUJUAN

PERENCANAAN DAN PEMBUATAN TELETHERMAL DENGAN MENGGUNAKAN INFRA RED

SKRIPSI

Disusun dan diajukan sebagai salah satu syarat untuk memperoleh gelar Sarjana Teknik Elektronika Strata Satu (S-1)

Disusun Oleh :

YUDI PURNOMO
00.17.246

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Judul Skripsi	:	

"PERENCANAAN DAN PEMBUATAN TELETHERMAL DENGAN MENGUNAKAN INFRA RED "

Dipertahankan Dihadapan Team Penguji Skripsi Jenjang Strata Satu (S-1), pada :

Hari	:	Selasa
Tanggal	:	21 Maret 2006
Dengan nilai	:	81,75 (A)

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(M. Ibrahim Ashari, ST)
Penguji II

Tak ada syukur yang saya panjatkan selain kepada kehadiran Allah SWT atas semua limpahan rahmat dan barokahNYA sehingga saya bisa menyelesaikan skripsi ini dan semoga Allah SWT selalu membuka jalan untuk memberi kemudahan dalam menempuh hidup ini

Semua ini kupersembahkan hanya kepada

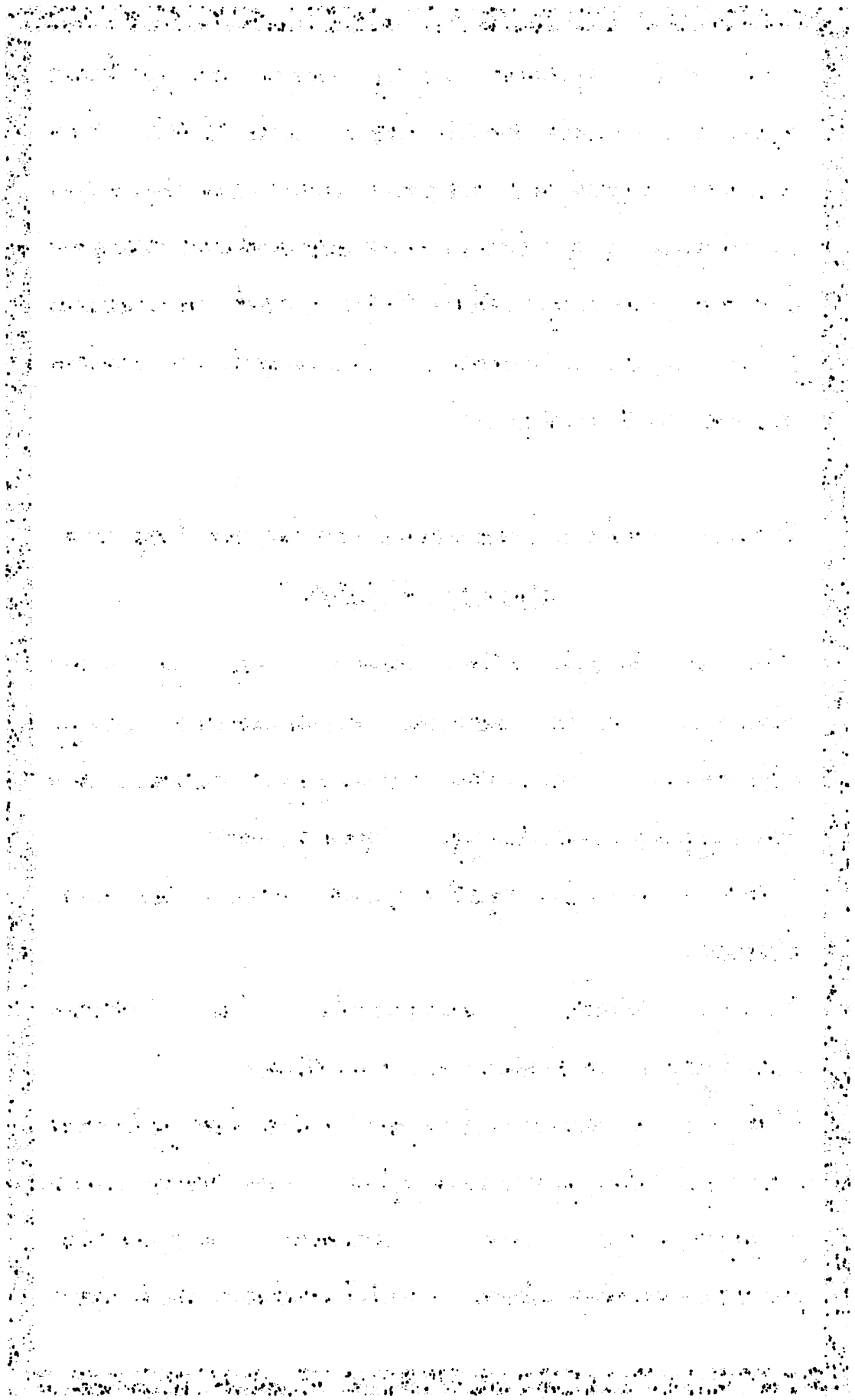
ABAH & UMMI

Terima kasih atas kasih sayang dan doanya serta semua kesabaran yang diberikan kepadaku sehingga semua ini bisa dijalan ini dengan lapang hati

Matur suwun banget kepada semua temen-temen

Yang telah membantu ku dalam mengerjakan skripsi ini untuk :

Pak jacky suwun banget atas ide gilanya /he..he... aku ga nyangka /,mas tony atas programnya dan semua komentar pedesmu,mas dony sambil makan sekalian



ngomongin skripsi (pusing pusingdech!!) dan cak gambier suwun yo ngeterno aku nang suroboyo (aduh gak enak aku ngrepoti),koko Gentong suwun flash diske yo! Mas kemo boxnya berapa???,pajank kost matur suwunnnnn, mbak rury aku wes nyusul

Untuk temen seperjuanganku Kebo,Awie,Kokok,kriwul,havid,boy,stev,Teguh,d an semua angkatan 2000 yang tersisa SENENGE rek!

Dan semuanya yang telah membantu makasih.....

Pay imoets
Maret 2006

ABSTRAKSI

PERENCANAAN DAN PEMBUATAN TELETHERMAL DENGAN MENGGUNAKAN INFRA RED

(Yudi Purnomo, 0017246, Jurusan Teknik Elektro S-1, Konsentrasi Teknik Elektronika, 63 halaman)

(Dosen Pembimbing : Ir. Usman Djuanda,MM dan Ir. Mimien Mustikawati)

Kata kunci Infra red,Photodiode,Op Amp,Mikrokontroller,ADC,LCD

Kondisi teknologi dewasa ini telah mencapai tingkat perkembangan yang sedemikian pesatnya. Apalagi sudah memasuki era millenium, banyak orang berharap melakukan pekerjaan dapat dilakukan dengan sesingkat mungkin. Hal ini dimaksudkan agar pekerjaan manusia bisa berjalan dengan cepat dan efisien. Banyaknya penggunaan infra red dalam piranti teknologi masa kini, salah satunya adalah pendeteksian suhu pada suatu benda dengan menggunakan sinar infra red tanpa harus menyentuh ke obyek benda Misalkan saja untuk mengetahui kondisi suhu tubuh manusia, terutama bayi yang masih kecil. Maka akan sangat repot untuk mengetahui suhu tubuh seorang bayi apabila alat yang digunakan ditempelkan pada bayi. Oleh karena itu dibutuhkan suatu alat yang dapat mengetahui suhu suatu benda dengan jarak tertentu.

Pada tugas akhir ini, dibuat sebuah system untuk menangkap perubahan suhu suatu benda pada jarak tertentu. Sistem kontrol yang digunakan adalah dengan menggunakan Sinar Infra merah sebagai tolak ukur frekuensi pantulan, sehingga didapatkan nilai tegangan kemudian di transmisikan pada rangkaian Infra red receiver. Setelah itu inputtan tegangan akan dikuatkan lagi sehingga bisa diolah oleh ADC dan mikro yang kemudian ditampilkan ke LCD

KATA PENGANTAR

Alhamdulillah, dengan memanjatkan puji syukur kehadirat Allah SWT, yang telah memberikan rahmat, hidayah serta karunia-Nya, tak lupa sholawat dan salam kepada nabi Muhammad SAW. dan keluarganya, akhirnya penyusun dapat dapat menyelesaikan skripsi ini yang berjudul "*Perencanaan Dan Pembuatan Telethermal Dengan Menggunakan Infra Red*", laporan skripsi ini merupakan salah satu persyaratan kelulusan Program Strata 1 Teknik Elektro/Konsentrasi Elektronika Institut Teknologi Nasional Malang.

Keberhasilan penyusunan laporan skripsi ini tidak lepas dari dukungan dan bantuan berbagai pihak. Untuk itu penyusun menyampaikan terimakasih kepada:

1. Abah dan ummi tercinta yang selalu memberikan kasih sayang, do'a restu, dukungan dan bantuan secara moril maupun materiil kepada penyusun, dengan segala dukungan orang tua dapat membesarkan hati penyusun meyelesaikan skripsi ini.
2. Bapak Dr. Ir. Abraham Lomi, MSEE. selaku Rektor Institut Teknologi Nasional Malang.
3. Bapak Ir. Mochtar Asroni, MSME. selaku Dekan Fakultas Teknologi Industri Institut Teknologi Nasional Malang
4. Bapak Ir. F. Yudi Limpraptono, MT. selaku Ketua Jurusan Teknik Elektro S-1 Institut Teknologi Nasional Malang
5. Bapak Ir. Usman Djuanda, MT selaku Dosen Pembimbing I
6. Ibu Ir. Mimien Mustikawati selaku Dosen Pembimbing II

7. Teman-teman yang telah memberikan motifasi serta bantuan baik berupa tenaga maupun fikiran dalam proses penyelesaian skripsi ini

Penyusun telah berusaha semaksimal mungkin dan menyadari sepenuhnya akan keterbatasan pengetahuan dalam penyelesaian laporan ini. Untuk itu penyusun mengharapkan saran dan kritik yang bersifat membangun demi kesempurnaan laporan ini.

Malang, Maret 2006

Penyusun

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BAB I

PENDAHULUAN

1.1 Latar belakang

Kondisi teknologi dewasa ini telah mencapai tingkat perkembangan yang sedemikian pesatnya. Apalagi sudah memasuki era millenium, banyak orang berharap melakukan pekerjaan dapat dilakukan dengan sesingkat mungkin. Hal ini dimaksudkan agar pekerjaan manusia bisa berjalan dengan cepat dan efisien. Misalkan saja untuk mengetahui kondisi suhu tubuh manusia, terutama bayi yang masih kecil. Maka akan sangat repot untuk mengetahui suhu tubuh seorang bayi apabila alat yang digunakan ditempelkan pada bayi. Oleh karena itu dibutuhkan suatu alat yang dapat mengetahui suhu tubuh manusia tanpa tersentuh oleh tubuh dengan jarak tertentu.

Pada tugas akhir ini, saya mencoba merencanakan dan membuat alat yang dapat mengukur dan mendeteksi radiasi suhu panas pada jarak tertentu dengan menggunakan LED infra merah sebagai salah satu LED yang dapat menghasilkan sinar infra merah. Jumlah radiasi infra merah yang dipancarkan pada suatu objek, maka frekuensi pantulan dari infra merah ini akan berubah. Besar perubahan frekuensi infra merah ini tergantung suhu dari benda / objek itu sendiri. Ini merupakan dasar yang penting karena mengimplikasikan bahwa sinar infra merah dapat dijadikan sebagai pendeteksi suhu. Sebagai detektor digunakan sensor photodiode yang dapat menangkap perubahan frekuensi dan kemudian frekuensi

ini akan diubah dalam bentuk tegangan. Kemudian tegangan outputan ini akan dproses lagi sehingga bisa diubah kedalam bentuk digital yang bisa ditampilkan ke LCD (liquid crystal display).sistem akan diharapakan bekerja dengan baik sehingga alat bisa membaca dan memberikan outputan yang dibutuhkan.

1.2 Tujuan

dari permasalahan yang ada maka tujuan dari perencanaan dan pembuatan alat ini adalah sebagai berikut :

1. merancang dan membuat alat untuk mendeteksi dan mengukur suhu dengan menggunakan sensor infra merah.
2. diharapkan dengan menggunakan sensor infra red alat ini dapat membaca radiasi panas pada jarak tertentu.

1.3 Rumusan Masalah

dari latar belakang yang telah dikemukakan, maka rumusan masalah yang dihadapi adalah :

1. Bagaimana merancang dan membuat telethermal dengan menggunakan sensor infra merah.
2. Bagaima mengimplikasikan sensor infra merah sehingga dapat digunakan sebagai pendeteksi suhu.
3. Bagaimana supaya system alat dapat bekerja sehingga menghasilkan outputtan yang diinginkan .

1.4. Batasan Masalah

dari permasalah yang telah dijelaskan untuk lebih terarahnya pembahasan skripsi ini maka ruang lingkup pembahasan masalah penyusun batasi pada hal-hal berikut :

1. pada saat pengukuran tempat pengukuran dianggap memiliki suhu dan pencahayaan yang sama
2. batas pengukuran suhu minimum dan maksimum adalah antaara 27^0 - 80^0
3. tidak membahas secara keseluruhan teori tentang infra merah
4. tidak membahas software
5. tidak membahas catu daya

1.5. Sistematika Penulisan

penulisan skripsi ini terbagi dalam lima bab dengan sistematika sebagai berikut :

BAB 1 PENDAHULUAN

Berisi latar belakang,tujuan, permasalahan, batasan masalah, metodologiDan sistematika penulisan

BAB II TEORI PENUNJANG

Membahas teori teori dasar penunjang perancangan dan pembuatan alat ini

BAB III PERANCANGAN DAN PEMBUATAN ALAT INI

Membahas tentang perancangan alat, baik perangkat keras dan cara kerja blok diagram.

BAB IV PENGUJIAN ALAT

Mencakup pembahasan tentang proses pengujian alat yang terdiri dari peralatan yang digunakan, langkah kerja dan analisa hasil pengujian

BAB V PENUTUP

Berisi kesimpulan dan saran

BAB II

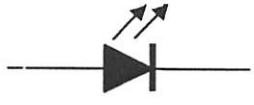
LANDASAN TEORI

2.1. LED (Light Emmiting Diode)

Light Emiting Diode (LED) adalah jenis semikonduktor p-n junction yang bekerja pada kondisi forward bias, yang dapat memancarkan radiasi dalam daerah ultra violet, visible (sinar tampak), dan infra merah pada spektrum elektromagnetik. Radiasi cahaya yang dihasilkan LED Infra Red ini sebanding dengan arus forward bias yang diberikan pada LED tersebut.

LED Infra Red merupakan LED biasa, hanya saja cahaya yang dipancarkan adanya akibat arus forward bias tidak dapat dilihat oleh mata, karena cahaya yang dipancarkan berada didaerah Infra Red.

Karakteristik dari LED Infra Red sama dengan LED pada umumnya. Saat tegangan forward bias yang diberikan masih dibawah tegangan ambang dari LED tersebut, maka arus belum dapat mengalir, tetapi setelah tegangan forward yang dikenakan pada LED mencapai tegangan ambang, maka pertambahan arus akan meningkat dengan cepat dan tegangan mendekati keadaan konstan.



Gambar 2-1

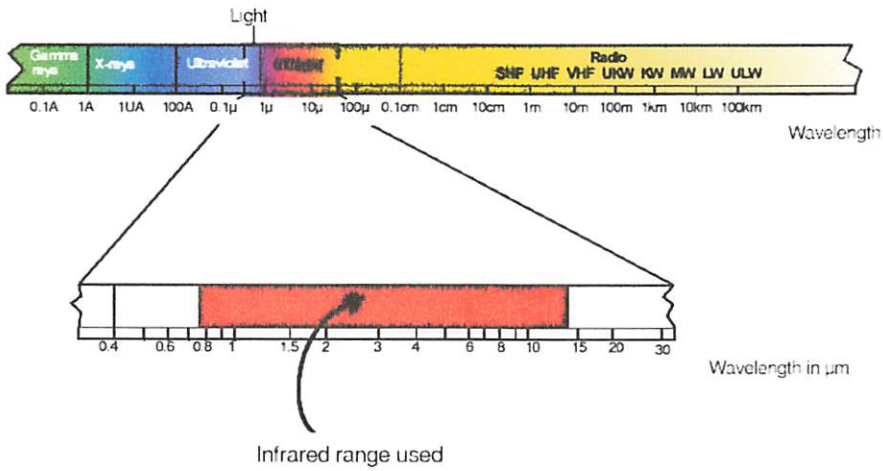
Simbol LED (Light Emmiting Diode)

Cahaya infra merah merupakan cahaya yang tidak tampak. Jika dilihat dengan dengan spektroskop cahaya maka radiasi cahaya infra merah akan nampak pada spektrum elektromagnet dengan panjang gelombang di atas panjang gelombang cahaya merah. Dengan panjang gelombang ini maka cahaya infra merah ini akan tidak tampak oleh mata namun radiasi panas yang ditimbulkannya masih terasa atau terdeteksi.

Cahaya infra merah, walaupun mempunyai panjang gelombang yang sangat panjang tetap tidak dapat menembus bahan-bahan yang tidak dapat melewatkan cahaya yang nampak sehingga cahaya infra merah tetap mempunyai karakteristik seperti halnya cahaya yang nampak oleh mata. *rattle snake* dan *beetle.*

2.2.. Infra Red

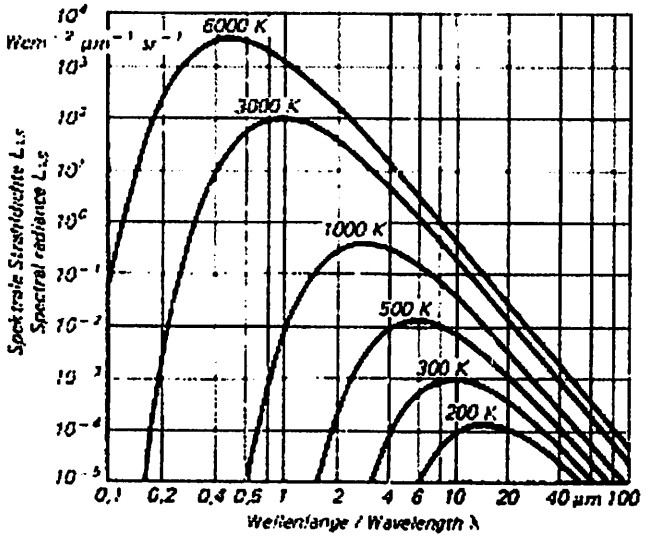
Setiap benda yang memanncarkan radiasi infra merah dapat dijadikan acuan bahwa setiap benda mempunyai temperatur. Hal ini dinamakan karakteristik dari Radiasi. Sepektrum dari radiasi mempunyai panjang gelombang dengan range berkisar antara 0.7 sampai 1000 mikro m. Radiasi ini tidak bisa normal, bahkan selalu berubah – ubah



Gambar 2-2
Spectrum Sinar Infra Red

Kalau kita lihat pada spektrum gelombang cahaya, infra merah (panjang gelombang sekira 0,7 mikro m – 14 mikro m) terletak di antara cahaya tampak dan microwave. Mata manusia yang terbatas pada daerah frekuensi cahaya tampak (warna pelangi) tidak mampu melihat sinar infra merah ini. Hanya ada 2 spesies di muka bumi yang diidentifikasikan mampu melihatnya yaitu *rattle snake* dan *beetle*.

Tipikal radiasi setiap benda mempunyai perberbedaan besar kecilnya temperatur. Sebagai indikasi temperatur yang memancarkan sedikit ukuran dari radiasi tetap.intensitas radiasi menunjukkan bahwa pada panjang gelombang 0.2 mikro m lebih banyak dari pada temperatur mempunyai panjang gelombang 10 mikro m.

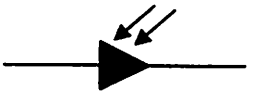


Gambar 2-3
Karakteristik Radiasi Suatu Benda Hitam Dalam Hubungan Dengan Temperaturnya.

2.3 Photodioda

Photodioda dapat digunakan untuk mendeteksi adanya sinar infra merah. Selama dalam pendeteksian pada photodioda akan terdapat arus bocor sebesar 0.5 uA dan ini juga tergantung pada kekuatan sinar infra merah yang datang dan sudut datangnya.

Kekuatan sinar dan sudut datang merupakan faktor penting dalam keberhasilan transmisi data melalui infra merah selain filter dan penguatan pada bagian receivernya.

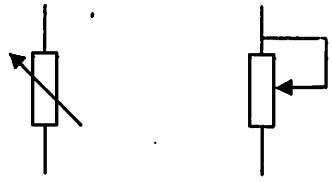


Gambar 2-4

Simbol Photo Dioda

2.4. Potensiometer

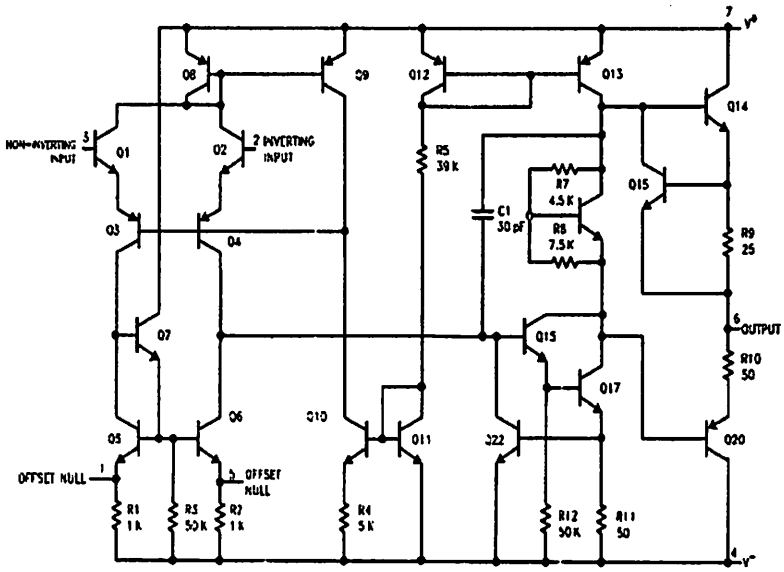
potensiometer adalah sebuah tahanan dengan nilai hambatan yang bisa diubah ubah. Konstruksi dari potensiometer erlihat pada gambar dibawah ini. Pada kepingan keramik atau pertinax dipasang lapisan karbon sepanjang mana melunsur sebuah penjalanya. Hambatan antara A dan B, B dan C tergantung dari kedudukan penjalanya. Dalam tugas akhir ini, potensiometer akan dimanfaatkan sebagai kalibrasi untuk pengukuran.



Gambar 2-5
Simbol Potensiomter

2.3. Operational Amplifier

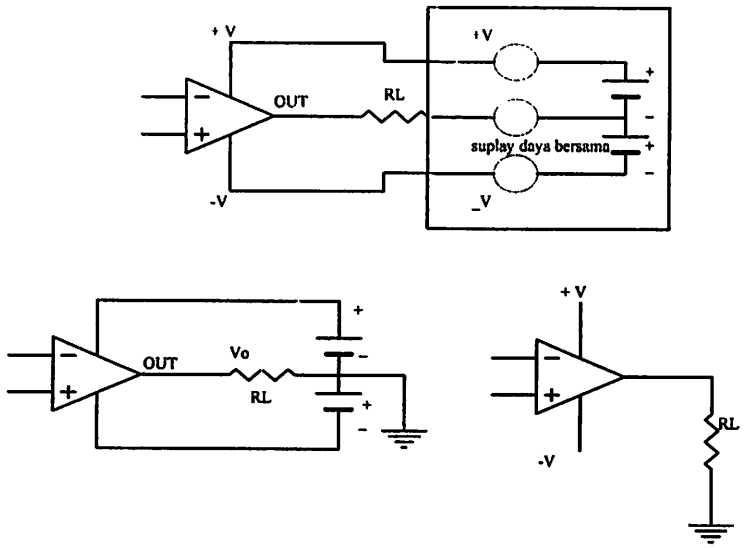
Op amp adalah nama penguat operasional yang bekerja pada tegangan yang lebih rendah (Op Amp rangkaian terpadu linier).Op Amp mempunyai lima terminal dasar : dua untuk mensuplai daya, dua untuk isyarat masukan, dan satu untuk keluaran. Bagian dalam Op Amp dapat diperlihatkan seperti skematik dibawah ini :



Gambar 2-6
Skema Op Amp

2.3.1 Terminal Op Amp

Skema rangkaian untuk op amp merupakan ujung panah , seperti terlihat dalam gambar 2- ujung panah tersebut melabangkan penguatan dan titik dari masukan ke keluaran.



Gambar 2-7
Menghubungkan Daya Dan Beban Ke Sebuah Op Amp

Gambar atas : Hubungan penghantar sebenarnya dari suplai daya ke op amp.

Gambar bawah : Penggambaran skema pensuplaian daya ke sebuah op amp.

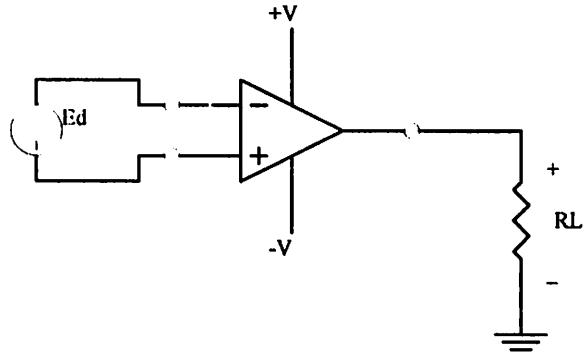
Terminal suplai daya bersama boleh atau tidak dihubungkan ke ground tanah melalaui kawat ketiga dari kabelnya. Suplai daya pada gambar 2-6 disebut bipolar atau suplai terpisah dan dan mempunyai harga khas sebesar ± 15 V, ± 12 V, dan ± 6 V. Op amp kegunaan khusus mungkin memerlukan suplai tak simetris seperti 12 V dan 6 V, atau bahkan suplai polaritas tunggal 30V dan ground. Arus yang kembali dari op amp kesuplainya harus kembali melalui elemen-elemen rangakain luar seperti misalnya tahanan beban RL. Tegangan suplai maksimum yang dapat diterapkan antara +V dan –V biasanya 36V atau ±18V.

2.3.2 Terminal Keluaran

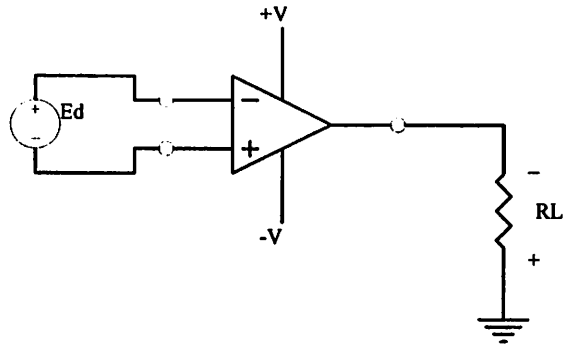
Dalam gambar 2- terminal keluaran op ampnya dihubungkan kesalah satu ujung tahanan RL. Ujung RL yang lain dikawatkan ke ground. Tegnagn keluaran Vo diukur terhadap ground, karena dalam sebuah op amp hanya ada satu terminal keluaran, keluaran ini disebut *keluaran berujung tunggal.* Batas arus yang dialirkan dari terminal keluaran op amp, biasanya ad pada orde sebesar 5 sampai 10 mA. Ada juga batas pada taraf-taraf tegangan terminal keluaran, yaitu batas ini ditentukan oleh tegangan suplai dan oleh transistor-transistor keluaran Q16 dab 11 dalam gambar 2-9. Berapa op amp , seperti misalnya 741 mempunyai rangakain bagian dalam yang secara automatik membatasi arus yang dialirkan dari terminal keluarannya. Bahkan dengan suatu hubung singkat untuk RL, arus keluaranya terbatas sampai kira-kira 25 mA, seperti tercatat dalam apendik 1. Keistimewaannya adalah mencegah kerusakan op amp bila terjadi hubung singkat.

2.3.3. Terminal masukan

Dalam gambar 2-11 ada dua terminal masukan, bertanda – dan +. Keduanya disebut terminal masukan karena tegangan keluaran Vo tergantung pada perbedaan tegangan antara kedua terminal itu, Ed, dan gain dari penguatnya AOL. Seperti terlihat dalam gambar 2-11 (a), terminal kelurannya positip +V terhadap masuakan (-). Bila Ed dibalik dalam gambar 2-11(b) untuk membuat masukan (+) menjadi negatif terhadap masukan (-) maka Vo menjadi negatif terhadap ground.



(a) Vo menjadi positif bila masukan (+) nya positif terhadap masukan (-) nya.

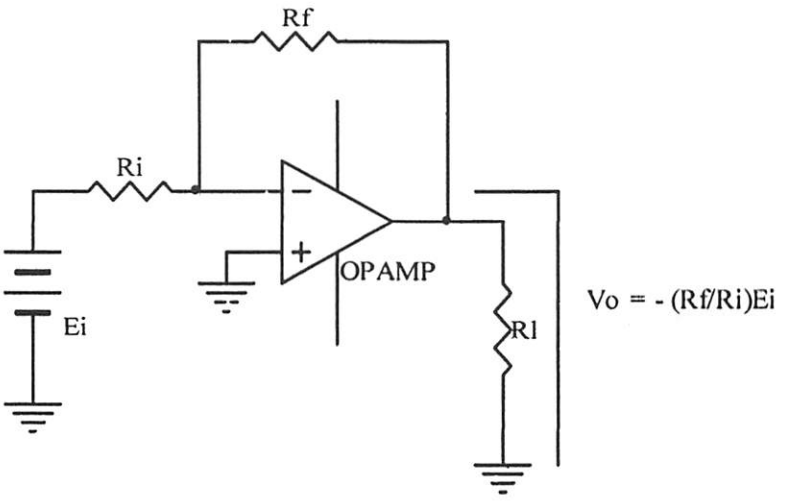


(b) Vo menjadi negatif bila masukan (+) nya negatif terhadap masukan (-) nya.

Gambar 2-8
Polaritas Vo tergantung pada polaritas tegangan masukan diferensial Ed.

2.3.4 Penguat Inverting

1. Penguat operasional dengan tegangan positif dihubungkan pada input pembalik.



Gambar 2-9.
Rangkaian Op Amp Inverting dengan Ei Positif dihubungkan pada input Pembalik
Sumber : Penguat Operasional dan Rangkaian Terpadu Linier

Tegangan Ei positif dihubungkan melalui tahanan masukan Ri kemasukan (-) dari Op-Amp. Umpan balik Negatif disusun oleh tahanan Rf. Tegangan antara input (+) dengan input (-) pada dasarnya nol (virtual ground atau ground semu). Karena ujung Ri yang satu berada pada Ground semu tersebut maka penurunan tegangan melalui Ri adalah Ei.

- Arus yang mengalir melalui Ri adalah:

$$I = \frac{Ei}{Ri} *$$

- Untuk tegangan output Vo dapat dicari dengan rumus :

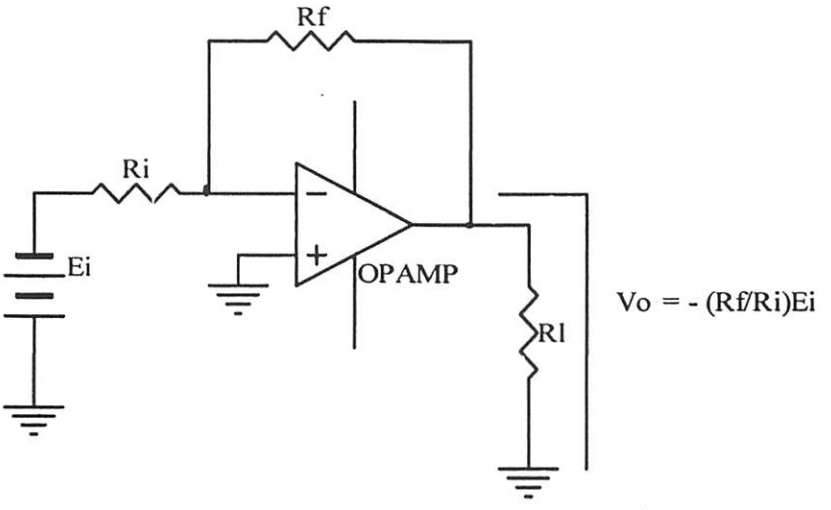
$$Vo = - Ei \frac{Rf}{Ri} *$$

- Untuk penguatan tegangan output Vo adalah :

$$A_V = \frac{Vo}{Ei} = - \frac{Rf}{Ri} *$$

* BAB 3 " *Penguct Operasional dan Rangkaian Terpadu, Edisi kedua" Robert F. Coughlin, Frederick F. Driscoll, Ir. Herman Widodo Soemitro, Penerbit Erlangga.*

2. Penguat operasional dengan tegangan negatif dihubungkan pada input pembalik.

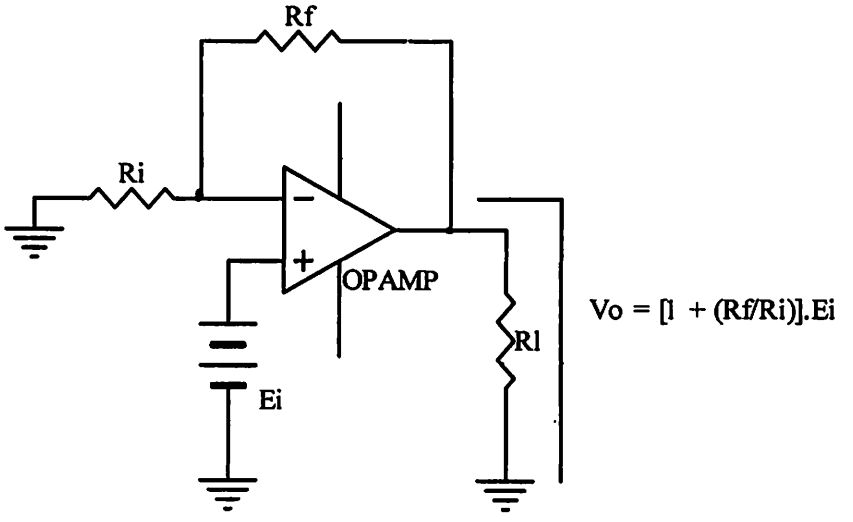


Gambar 2-10
Rangkaian Op Amp Inverting dengan Ei Negatif dihubungkan pada input Pembalik
Sumber : Penguat Operasional dan Rangkaian Terpadu Linier

Rangkaian pada gambar 2-9 di atas pada prinsipnya mempunyai rumus yang sama dengan rangkaian pada gambar 2-8. Perbedaannya hanya pada arah arusnya. Dengan membalik polaritas tegangan inputnya maka akan membalik semua arah dari arusnya. Sehingga keluaran dari penguat tersebut menjadi positif.

2.3.5 Penguat Non Inverting

1. Penguat Operasional dengan tegangan positif dihubungkan pada input tak membalik.



Gambar 2-11
Rangkaian Op Amp Non Inverting dengan Ei Positif dihubungkan pada input Pembalik
Sumber : Penguat Operasioanl dan Rangkaian Terpadu Linier

Tegangan Vo memiliki Polaritas yang sama seperti masukan Ri. Tahanan masukan dari penguat pembalik adalah Ri. Untuk tahanan masukan dari penguat tak membalik nilainya sangat besar, biasanya melebihi 100MΩ. Karena tegangan antara inputan (+) dan inputan (-) itu secara praktis 0, maka kedua inputan tersebut berada pada potensial Ei yang sama.

- Arus yang mengalir melalui Ri adalah:

$$I = \frac{Ei}{Ri} *$$

- Untuk tegangan output Vo dapat dicari dengan rumus :

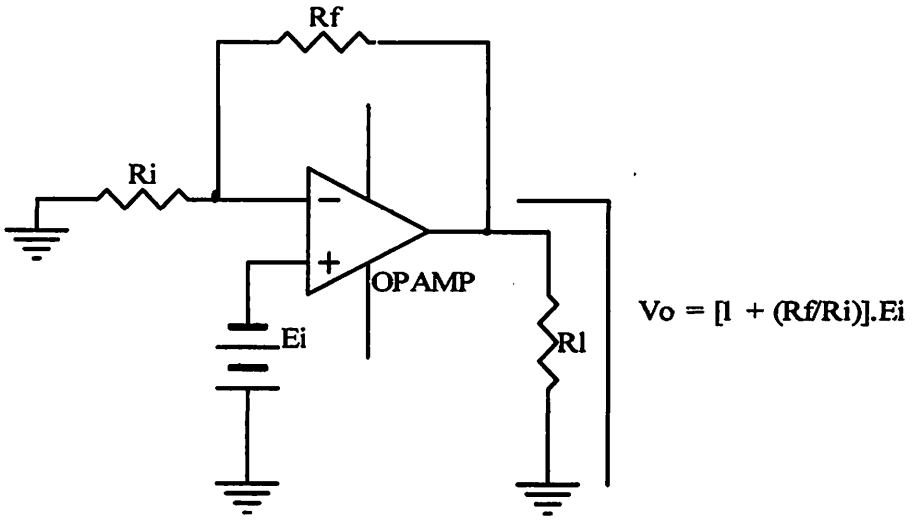
$$Vo = (1 + \frac{Rf}{Ri})\ Ei\ *$$

- Untuk penguatan Tegangan output Vo adalah:

$$Av = \frac{Vo}{Ei} = 1 + \frac{Rf}{Ri}\ *$$

* BAB 3 *" Penguat Operasional dan Rangkaian Terpadu, Edisi kedua" Robert F. Coughlin, Frederick F. Driscoll, Ir. Herman Widodo Soemitro, Penerbit Erlangga.*

2. Penguat Operasional dengan tegangan negatif dihubungkan pada input tak membalik.

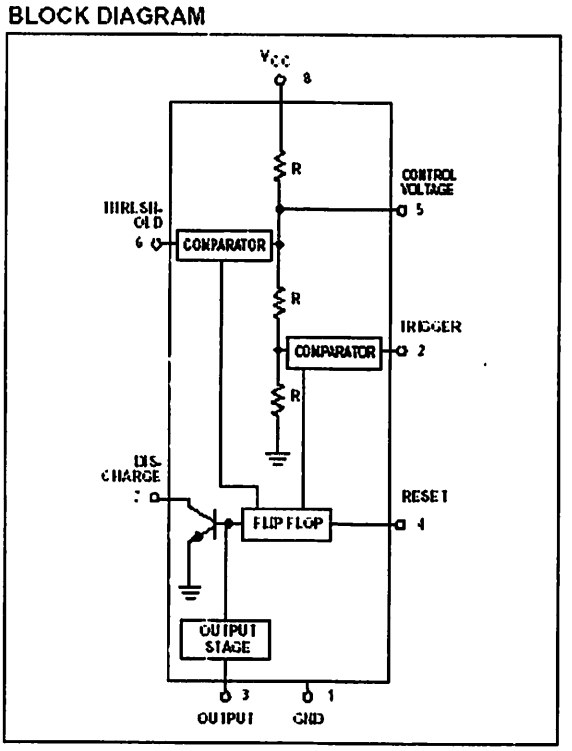


Gambar 2-12.
Rangkaian Op Amp Non Inverting dengan Ei Negatif dihubungkan pada input Pembalik
Sumber : Penguat Operasioanl dan Rangkaian Terpadu Linier

Adapun rumus yang digunakan sama dengan rangkaian pada gambar Perbedaannya terletak pada arah arusnya.

2.5. IC 555

Ic 555 mempunyai dua cara kerja,sebagai multivibrator astabil multivibrator monostabil.cara kerja astabil (bergerak bebas) dari Ic 555 adalah sebagai berikut,tegangan keluaran beralih dari high ke low dan kembali lagi. Waktu high atau low ditentukan oieh sebuah jaringan kapasitor dan resistor yang dihubungkan pada kaki kaki luar Ic. Cara kerja monostabil(satu tembakan) tegangan keluarannya low sampai sebuah pulsa pemicu negatif yang diberikan pada pewaktu tersebut,kemudian keluarannya kembali high. Waktu high atau high atau low ditentukan oleh sebuah jaringan kapsitor dan resistor yang dihubungkan pada kaki luar Ic. Adapun konfigurasi blok diagram Ic 555 seperti gambar dibawah ini :



Gambar 2-13
Konfigurasi IC 555

Ferkuensi dari Ic 555 ini dapat dihitung dengan menggunakan rumus sebagai berikut :

T high = 0,695 (RA + RB) * C

T low = 0,695*RB*C

Jadi periode osilasi total adalah :

T = T high + T low

= 0,695 (RA+2RB)C

Frekuensi osilasi bergerak bebas f adalah :

$$f = \frac{1}{T}$$

$$= \frac{144}{(RA + 2RB)C}$$

2.5. Dioda

Semua dioda prinsip kerjanya adalah sebagai penyearah. Tetapi karena proses pembuatan , bahan dan penerapannya yang berbeda- beda , maka namanya juga berbeda serta memiliki karakteristik yang berbeda pula.

Macam – macan dioda diantaranya :

1) Dioda Penyerah
2) Dioda Zener
3) Dioda Varaktor
4) Dioda Photo

2.4.1 Dioda Penyearah

Dioda penyearah sering kita jumpai pada rangkaian regulator yang dipakai untuk penyerah dari gelombang bolak balik. Kebanyakan dibuat dari silikon, mengingat kemampuan dan keandalannya yang cukup tinggi. Mampu dilewati arus yang besar dan dapat bekerja pada suhu yang tinggi.

Gambar 2-14
Simbol Dioda

2.6. Kapasitor

Kapasitor adalah komponen elektronika yang terdiri dari plat konduktor yang satu disekat terhadap yang lainnya dengan osilator dan berfungsi sebagai pelawan untuk arus bolak-balik, filter , tuning, kopel antar rangakain, pembangkit gelombang dan konduktor khusus.

Sebuah kapasitor dikatakan memepunyai kapasitas satu farad apabila muatan sebesar satu *columb* membuat tegangan naik sebesar satu volt, karena satuan farad terlampau besar maka dipakai satuan lebih rendah yaitu *mikro farad* ,*nano farad* dan *piko farad.*

Dalam kapasitor terdapat reaktansi, jika kapasitor tersebut diterapkan pada arus bolak-balik sinus, tegangan akan tertinggal sejauh 90°.

Untuk menentukan besarnya nilai reaktansi adalah :

$$Xc = \frac{1}{3.14.FC} \qquad (2\text{-}1)$$

Dimana

Xc = Reaktansi kapasitor

F = Frekuensi dalam Ω

C = Kapasitor dalam farad

Untuk menetukan banyaknya muatan iistrik yang dapat disimpan oleh kapasitor dapat dirumuskan sebagai berikut :

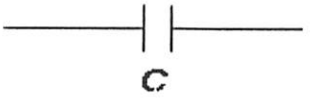
$$Q = C \times V \qquad (2\text{-}2)$$

Dimana :

C = kapasitor dalam farad

V = Tegangan yang ada keping-keping dalam volt

Q = Banyak muatan dalam columb



Gambar 2-15
Simbol Kapasitor

Cara kerja kapasitor adalah terjadinya perubahan pada kapasitor menyebabkan perubahan tersebut berbanding lurus dengan perubahan tegangan, energi akan timbul kembali pada saat tegangan berkurang menjadi nol.

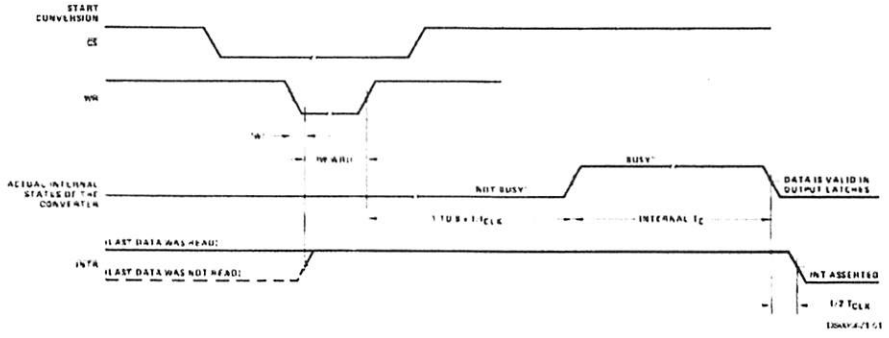
2.7. Analog To Digital Converter (ADC) 0804

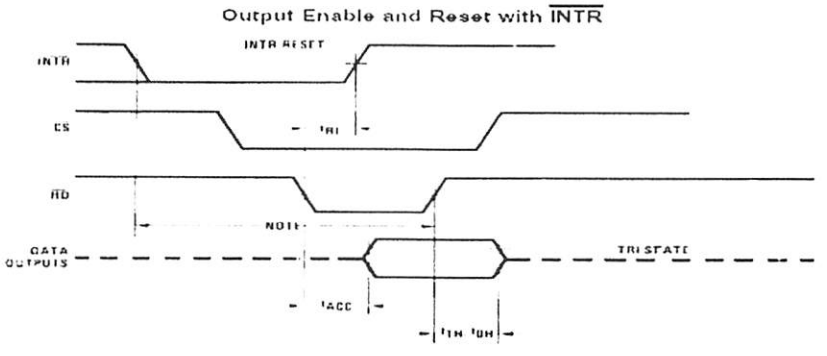
Untuk mengubah data analog dari keluaran sensor induksi menjadi data digital agar dapat di olah oleh program mikrokontroller maka diperlukan perangakat ADC. ADC yang dipergunakan adalah ADC0804 yang mempunyai resolusi 8 bit dan mempunyai 8 jalur output satu jalur input serta mempunyai clock internal dengan cara menghubungkan tahanan luar dan sebuah capasitor pada clock out dan clock in dan ground.

Spesifikasi lain untuk adc adalah waktu konversi suatu adc adalah waktu yang diperlukan ADC untuk menghasilkan kode biner yang *valid* (*tepat*) untuk tegangan masukan yang diberikan. Sebuah koverter disebut berkecepatan tinggi jika memiliki waktu konversi yang pendek. Beberapa karakteristik dan fungsi yang perlu diketahui adalah :

1. Dua input analog : Vin(+) dan Vin(-) yang merupakan input differensial. Apabila digunakan untuk pengukuran tunggal, maka digunakan untuk pengukuran tunggal, maka digunakan input Vin(+) dan V(-) harus dihubungkan ke analog ground. Selama beropersi normal, konverter ini menggunakan Vcc = +5 Volt sebagai tegangan referensinya. Dan input analognya mempunyai variasi range antara 0 sampai 5 Volt.
2. Dapat mengkonversi tegangan input analog menjadi 8 bit output digital. Output digital memiliki *buffer tristate,* sehingga dapat dengan mudah dihubungkan dengan port dari sebuah mikrokontroller. Dengan 8 bit, maka resolusinya adalah 5 Volt/19,6mVolt.

3. mempunyai fasilitas *internal clock* dengan frekuensi f=1(1,1 RC) dengan R dan C merupakan komponen luar yang harus ditambahkan. Frekuensi *clock typicalnya* adalah 640 Khz yang merupakan menggunakan komponen tambahan R = 10 K dan C = 150 pF. Dan apabila menggunakan ***eksternal clock***, maka pin CLK IN harus digunakan.





Gambar 2-16
Diagram Waktu ADC
Sumber : Data Sheet ADC National Semikonduktor

Perangkaian IC ini memudahkan berhubungan dengan port Mikrokontroller. Dan fungsi-fungsi dari system I/O ini adalah :

1. $\overline{CS}$ *(Chip Select)*

   Input ini mempunyai sifat aktif *Low* pada saat input RD atau WR digunakan.

2. $\overline{RD}$ *(Output)*

   Input ini digunakan untuk meng-*enable buffer* output ADC. Dengan CS, RD *Low*, pin output ADC akan memiliki level logika akhir konversi dari A/D.

3. $\overline{WR}$ *(Start Conversi)*

   Digunakan untuk memulai konversi, yaitu dengan memberikan pulsa rendah sesaat.

4. $\overline{INTR}$

   Sinyal Output sesaat akan menuju tinggi pada saat start konversi dimulai dan akan kembali rendah setelah selesei konversi.

5. CLK-R

   Sebuah resistor harus dihubungkan pada *clock*

6. CLK-IN

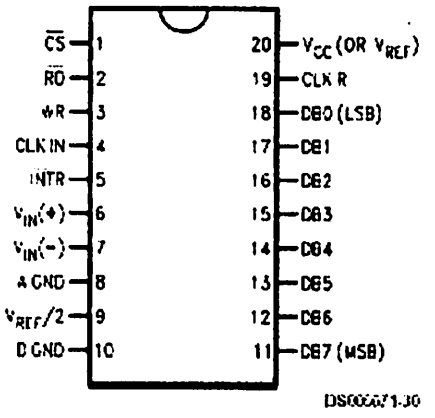
   Digunakan untuk *eksternal clock* input dengan menghubungkan kapasitor untuk penggunaan *internal clock.*

7. Vref/2

   Ini adalah input yang akan digunakan untuk menghasilkan tegangan referensi dan dapat mengubah *range* input analognya. Pada saat

input belum disambungkan, input ini masih 2,5 Volt (Vcc/2) atau selama Vcc digunakan sebagai tegangan referensinya. Dengan menghubungkan tegangan luar pada pin, maka internal referensi akan berubah yang membagi tegangan tersebut, demikian halnya *range input* analognya

ADC080X
Dual-In-Line and Small Outline (SO) Packages



Gambar 2-17
Analog To Digital Converter
Sumber : Data Sheet ADC National Semiconduktor

2.8 Mikrokontroller AT89S51

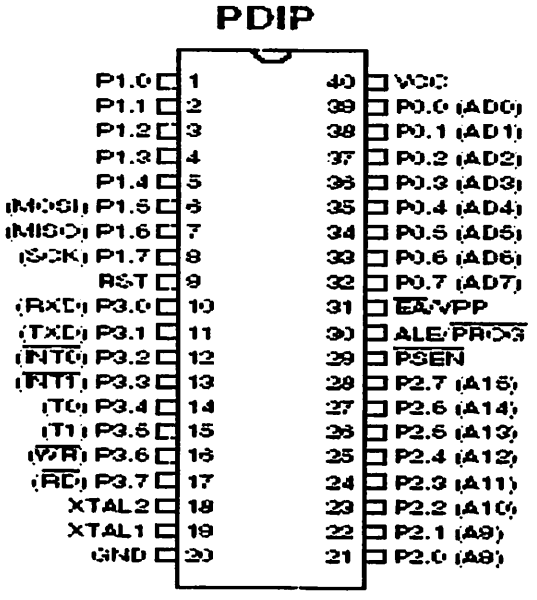
2.8.1 Arsitektur Perangkat Keras

Mikrokontroller AT89S51 adalah mikrokontroller ATMEL yang kompatibel penuh dengan mikrokontroler keluarga MCS – 51, membutuhkan daya rendah, memiliki performance yang tinggi dan merupakan mikrokomputer 8 bit yang dilengkapi 4Kbyte EEPROM *(Electrical Erasable and Programmable Read Only Memory)* dan 128 Byte RAM internal. Program memori yang dapat diprogram ulang dalam sistem atau menggunakan programmer *Nonvolatile* Memory konvensional. Dalam sistem mikrokontroller terdapat dua hal yang

mendasar, yaitu: perangkat lunak dan perangkat keras yang keduanya saling terkait dan mendukung.

Secara umum Mikrokontroller AT89S51 memiliki :

- CPU 8 bit termasuk keluarga MCS-51
- 4 Kb Flash memory
- 128 byte Internal RAM
  - 4 bank regester, masing – masing berisi 8 register.
  - 16 byte yang dapat dialamati pada bit level.
  - 80 byte *general purpose memory data.*
- 32 buah Port I/O, tersusun atas P0 – P3,masing – masing 8 bit.
- 2 Timer/ counter 16 bit
- 2 Serial Port Full Duplex
- Kecepatan pelaksanaan intruksi per siklus 1 us pada frekuensi clock 12 Mhz
- 2 DPTR (*Data Pointer*)
- Watchdog Timer
- Fleksibel ISP Programming



Gambar 2-18
Konfigurasi Pin Mikrokontroler AT89S51
Sumber : Data sheet AT89S51

Berikut ini adalah penjelasan dari masing-masing pin mikrokontroler AT89S51:

- Pin 1 sampai 8

  Port 1 : Merupakan 8-*bit* saluran masukan atau keluaran dua arah, setiap saluran mampu melayani 4 masukan.

- Pin 9

  RST : Merupakan masukan reset. Logika high yang akan membuat mikrokontroler AT89S51 menjalankan rutin reset.

- Pin 10 sampai 17

  Port 3 : Port 3 terdiri dari 8 saluran masukan atau keluaran dua arah. Setiap salurannya mampu melayani 4 masukan. Selain sebagai port masukan atau keluaran, port 3 juga mempunyai fungsi-fungsi khusus yang dimiliki oleh keluarga MCS-51.

- Pin 18 dan 19

  X1 (*XTAL*1) dan X2 (*XTAL*2) : Jika dikonfigurasikan bersama sebuah kristal akan membentuk rangkaian osilator on-chip pada mikrokontroler.

- Pin 20 sampai 27

  Port 2 : Port 2 terdiri dari 8 saluran masukan dan keluaran dua arah. Setiap salurannya mampu melayani 4 masukan. Port 2 mengeluarkan alamat bagian high (A8-A15), selama pengambilan instruksi dari memori program eksternal dan pengambilan data dari memori data eksternal yang menggunakan mode pengalamatan 16-bit.

- Pin 29

  $\overline{PSEN}$: *Program Store Enable* merupakan sinyal baca yang mengeksekusi memori program eksternal.

- Pin 30

  ALE/ $\overline{PROG}$: Address *Latch Enable* merupakan pulsa yang berfungsi menahan alamat rendah (A0-A7) pada port 0, selama dilakukan proses baca dan tulis memori eksternal. Pin ini juga berfungsi sebagai masukan pulsa program ($\overline{PROG}$), selama dilakukan pemrograman pada *EEPROM eksternal.*

- Pin 31

  $\overline{EA}$ /VP : *Eksternal Acces.* $\overline{EA}$ dihubungkan dengan VSS untuk memungkinkan pengambilan instruksi pada memori program eksternal yang berlokasi 0000_H sampai $FFFF_H$. Jika diinginkan menggunakan program internal, maka $\overline{EA}$ dihubungkan VCC.

- Pin 32 sampai 39

  Port 0 : Port 0 terdiri dari 8 saluran masukan dan keluaran dua arah. Setiap saluran mampu melayani 8 masukan. Port 0 merupakan saluran alamat bagian low (A0-A7), yang dimultipleks dengan saluran bus data (D0-D7), yang digunakan pada saat mengakses memori data eksternal dan memori program eksternal.

- Pin 40

  VCC : Merupakan masukan catu daya 5 volt, dengan toleransi kurang lebih 10μs.

Tabel 2-1 . Keluarga MCS 51

Tipe	Tipe tanpa EPROM	Tipe ber EPROM	Kapasitas ROM	Kapasitas RAM	Port I/O	Pewaktu
8031	8031	-	4K	128	4	2
8051AH	8031AH	8751H	4K	128	4	2
8052AH	8032AH	8752BH	8K	256	4	3
80C52BH	80C31BH	87C51	4K	128	4	2
80C52	80C32	-	8K	256	4	3
83C51FA	80C51BH	87C51FA	8K	256	4	3
83C51FB	80C51FB	87C51FB	16K	256	4	3
83C152	80C152	-	8K	256	5	3
89S52	-	89S52	8K	256	4	3

Sumber: Elex Media Komputindo. Bereksperimen dengan Mikrokontroler 8031

Keluarga MCS-51 yang diproduksi Intel mempunyai konfigurasi yang berbeda-beda sesuai dengan jenisnya. Masing-masing jenis saling kompatibel serta mempunyai kelebihan tersendiri. Misalnya mikrokontroler AT89S51 merupakan padanan dari mikrokontroler 8051. Tabel tersebut memperlihatkan sebagian dari keluarga MCS-51.

2.8.2 Organisasi Memori

Organisasi memori pada mikrokontroler AT89S51 dapat dibagi menjadi dua bagian besar yaitu memori program dan memori data. Pembagian tersebut didasarkan atas fungsi dari penyimpanan data maupun program. Memori program digunakan untuk menyimpan instruksi-instruksi yang akan dijalankan oleh mikrokontroler, sedangkan memori data digunakan sebagai tempat penyimpanan data yang sedang diolah mikrokontroler

Program mikrokontroler disimpan dalam memori program berupa ROM. Mikrokontroler AT89S51 dilengkapi dengan ROM internal namun untuk program yang besar digunakan ROM eksternal yang terpisah dari mikrokontroler. Untuk dapat menggunakan memori program eksternal ini penyemat /$\overline{EA}$ dihubungkan dengan penyemat Vss (logika 0).

Memori program mikrokontroler menggunakan alamat 16 bit mulai 0000_H-$FFFF_H$, sehingga kapasitas penyimpanan program maksimal adalah 2^{16} *byte* atau 64 Kb. Sinyal yang digunakan untuk membaca memori program eksternal adalah sinyal /PSEN (*Program Store Enable*).

Selain memori program mikrokontroler AT89S51 juga memiliki memori data internal berkapasitas 128 *byte* dan mampu mengakses memori data eksternal

sebesar 64 Kb. Semua memori data internal dapat dialamati dengan pengalamatan langsung atau tidak langsung. Ciri dari pengalamatan langsung adalah *operand* berisi alamat data yang diolah. Sedangkan ciri dari pengalamatan tidak langsung adalah *operand* alamat *register* yang berisi alamat data yang akan diolah. Sebagian memori tersebut dapat dialamati dengan pengalamatan register, dan sebagian lagi dapat dialamati dengan memori satu *bit.* Untuk membaca data digunakan sinyal $\overline{/RD}$, sedangkan untuk menulis data digunakan sinyal $\overline{/WR}$.

2.8.3 Register Fungsi Khusus

Register fungsi khusus (*Special Function Register*) terletak pada 64 *byte* bagian atas memori data internal dan berisi *register-register* untuk pelayanan *latch port, timer, program status words, control peripheral* dan sebagainya. Alamat register fungsi khusus ditunjukkan pada tabel 2-.

Register-register ini hanya dapat diakses dengan pengalamatan langsung. Enam belas alamat pada register fungsi khusus dapat dialamati per-*bit* maupun per-*byte* dan terletak pada alamat 80_H-FF_H. Secara perangkat keras, register fungsi khusus ini dibedakan dengan memori data internal.

Tabel 2-2. Nama dan Alamat Register pada Register Fungsi Khusus

Simbol	Nama Register	Nilai pada saat reset	Alamat
ACC	Accumulator	0000_H	$0E0_H$
B	Register B	00_H	$0F0_H$
PSW	Program Status Word	00_H	$0D0_H$
SP	Stack Pointer	07_H	81_H
DPTR	Data Pointer 2 byte	-	-
DPL	Low bytes	0000_H	82_H
DPH	High bytes	0000_H	83_H
P0	Port 0	FF_H	80_H
P1	Port 1	FF_H	90_H
P2	Port 2	FF_H	$0A0_H$
P3	Port 3	FF_H	$0B0_H$
IP	Interupt priority control	$XXX00000_B$	$0B8_H$
IE	Interupt enable control	$0XX00000_B$	$0A8_H$
TMOD	Timer/counter mode control	00_H	89_H
TCON	Timer/ counter control	00_H	88_H
TH0	Timer/counter 0 high byte	00_H	$8C_H$
TL0	Timer counter 0 low byte	00_H	$8A_H$
TH1	Timer / counter 1 high byte	00_H	$8D_H$
TL1	Timer/ counter 1 low byte	00_H	$8B_H$
SCON	Serial control	00_H	$9B_H$
SBUF	Serial data buffer	Independen	99_H
PCON	Power control	HMOS $0XXXXXXX_B$ CHMOS $0XXX0000_B$	87_H

(Sumber: Elex Media Komputindo. Bereksperimen dengan Mikrokontroler 8031)

Beberapa macam register fungsi khusus yang sering digunakan, dijelaskan sebagai berikut :

- *Accumulator* (ACC) merupakan *register* untuk penambahan dan pengurangan. Perintah *Mnemonic* untuk mengakses akumulator disederhanakan sebagai A.

- *Register* B merupakan *register* khusus yang berfungsi melayani operasi perkalian dan pembagian.
- *Program Status Word* (PSW) terdiri dari beberapa *bit* status yang menggambarkan kejadian di akumulator sebelumnya. Yaitu *carry bit, auxiliary carry*, dua *bit* pemilih bank, bendera *overflow, parity bit*, dan dua bendera yang dapat didefinisikan sendiri oleh pemakai.
- *Stack Pointer* (SP) merupakan *register* 8 bit yang dapat diletakkan di alamat manapun pada RAM internal. Isi *register* ini ditambah sebelum data disimpan, selama instruksi *PUSH* dan *CALL*. Pada saat *reset, register* SP diinisialisasikan pada alamat 07_H , sehingga stack akan dimulai pada lokasi 08_H.
- *Data pointer* (DPTR) terdiri dari dua *register*, yaitu untuk *byte* tinggi (*Data pointer high*, DPH) dan *byte* rendah (*Data pointer Low*, DPL) yang berfungsi untuk mengunci alamat 16 *bit*.
- *Port 0* sampai *port 3* merupakan *register* yang berfungsi untuk membaca dan mengeluarkan data pada *port* 0, 1, 2, 3. masing-masing register ini dapat dialamati per-*byte* maupun per-*bit*.
- *Serial data buffer* (SBUF) merupakan dua *register* yang terpisah, *register buffer* pengirim dan sebuah register *buffer* penerima. Meletakkan data pada SBUF berarti meletakkan pada *buffer* pengirim yang akan mengirimkan data melalui transmisi serial. Membaca data SBUF berarti menerima data dari *buffer* penerima.

- *Control register* terdiri dari *register* yang mempunyai fungsi kontrol. Untuk mengontrol sistem interupsi, terdapat dua register khusus, yaitu register IP (*interrupt priority*) dan register IE (*interrupt enable*). Untuk mengontrol pelayanan timer counter terdapat register khusus, yaitu register TCON (*timer counter control*) serta untuk pelayanan port serial menggunakan register SCON (*serial port control*).

2.8.4. Port Masukan dan Keluaran

Mikrokontroler AT89S51 mempunyai 4 port dan masing-masing port terdiri dari 8 saluran *bit*. Ke empat port ini bersifat bidirectional yaitu dapat digunakan sebagai masukan atau keluaran.

Port 0 digunakan sebagai saluran data yang di multipleks dengan saluran alamat rendah untuk mengakses memori eksternal, baik memori program maupun memori data. Port 2 mengeluarkan bagian alamat high untuk mode pengalamatan memori 16 bit. Port 1 dan 3 berfungsi sebagai saluran masukan dan keluaran multi fungsi. Jika dibutuhkan port 3 mempunyai fungsi khusus seperti ditunjukkan pada tabel berikut.

Tabel 2-3 .Fungsi Khusus Port 3

Nama Penyemat	Fungsi Khusus
Port 3.0	RxD (port asukan serial)
Port 3.1	TxD (port keluaran serial)
Port 3.2	/INT0 (masukan interupsi eksternal 0)
Port 3.3	/INT1 (masukan interupsi)
Port 3.4	T0 (masukan pewaktu eksternal 0)
Port 3.5	T1 (masukan pewaktu eksternal 1)
Port 3.6	/WR (sinyal tulis memori data eksternal)
Port 3.7	/RD (sinyal baca memori data eksternal)

2.8.5. Sistem Interupsi

Mikrokontroler AT89S51 mempunyai dua sumber interupsi eksternal dan sumber interupsi internal yang dapat diprogram agar sensitive terhadap perubahan level atau transisi. Interupsi timer aktif saat register timer yang bersangkutan mengalami *rollover*. Interupsi serial akan aktif pada saat mikrokontroler mengirim/menerima data. Setiap sumber interupsi dapat diaktifkan/dimatikan melalui perangkat lunak.

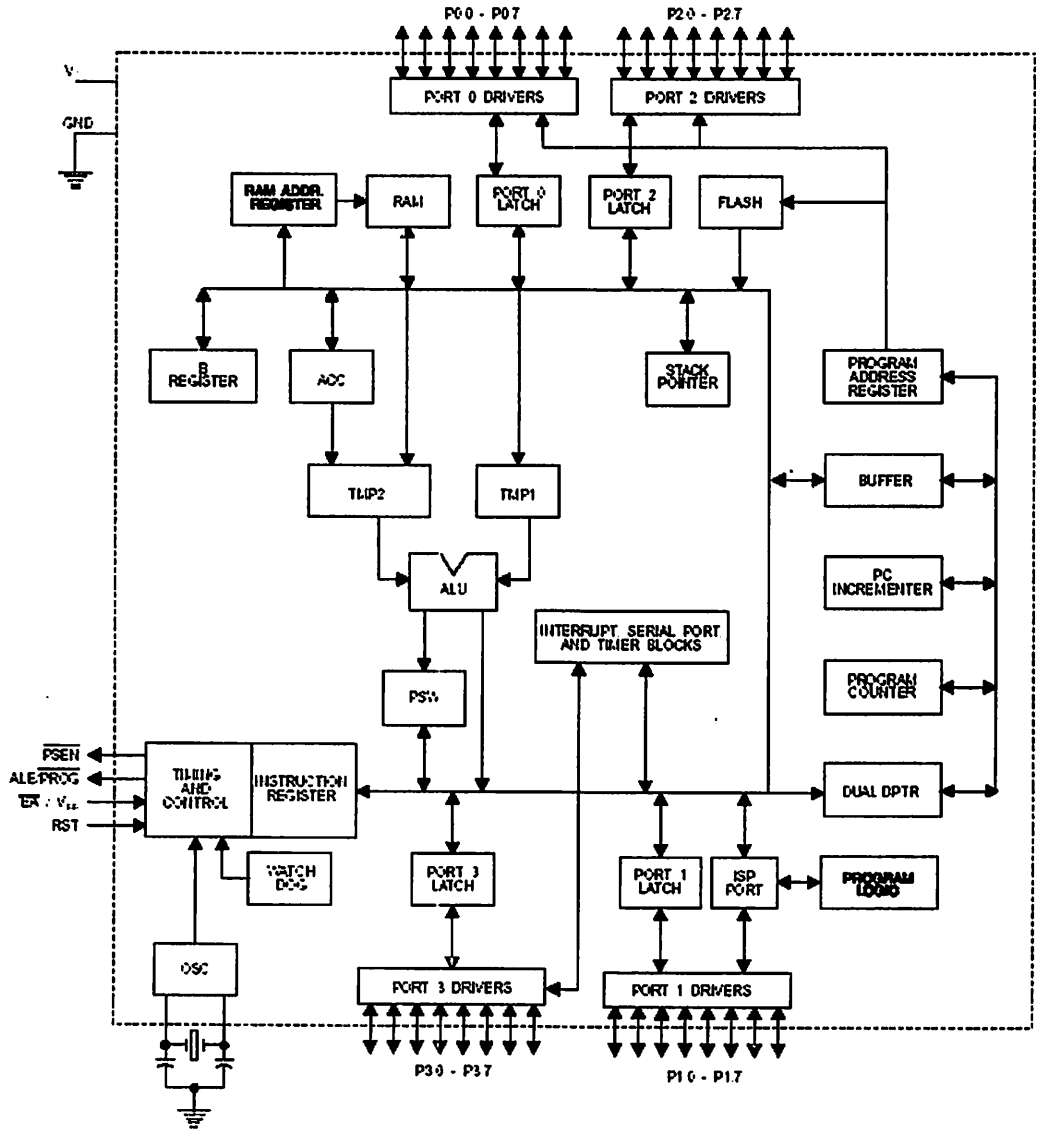
Tabel 2- 4 Tingkatan Prioritas Interupsi

Prioritas Interupsi	Sumber Interupsi	Alamat Vektor
1	IE0 (Interupsi eksternal 0)	0003_H
2	TF0 (timer overflow flag 0)	$000B_H$
3	IE1 (interupsi eksternal 1)	0013_H
4	TF1 (timer overflow flag 1)	$001B_H$
5	R1 dan T1	0023_H
6	TF2 dan EXF2	$002B_H$

(Sumber: Intel. 1994: 3-25)

Hirarki tingkatan prioritas interupsi dapat dilihat dalam tabel diatas. Interupsi yang mempunyai tingkatan prioritas lebih tinggi tidak dapat diinterupsi oleh yang lebih rendah. Meskipun demikian melalui perangkat lunak hirarki tersebut dapat diubah, yaitu dalam register *interrupt priority* (IP).

Block Diagram



Gambar 2-19
Blok Diagram Mokrokontroler AT89S51
(Sumber : ATMELDatasheet Book)

2.9. LCD (Liquid Crystal Display)

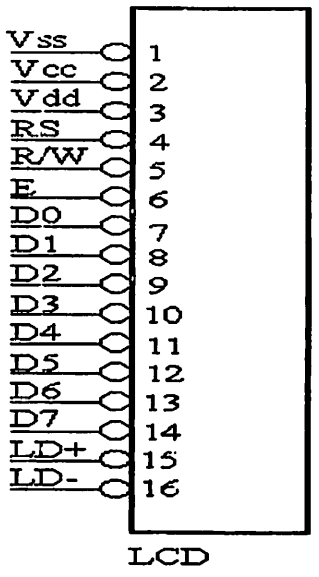
LCD atau *Liquid Crystal Display* merupakan sarana tampilan yang terdiri dari tumpukan tipis antar sel dari dua lembar kaca yang pinggirnya tertutup rapat. Diantara kedua lapisan tersebut diberi kristal cair yang tembus cahaya. Permukaan luar masing – masing keping kaca memiliki lapisan penghantar tembus cahaya. Sel memiliki ketebalan kira – kira $1x10^5$ m yang diisi dengan kristal cair. Pada modul LCD TM162 keluaran Seiko Instrument, LCD memiliki 2 baris tampilan dengan 16 karakter setiap barisnya.

Tabel 2-5 Nama dan Fungsi Penyemat Pensinyalan pada Modul LCD

Nama	Fungsi
D0 – D7	Saluran data yang berisi perintah dan data LCD
Enable	Sinyal pengaktif komponen '1' untuk mengaktifkan '0' untuk tidak memilihnya
R/W	Selektor baca tulis '1' untuk membaca '0' untuk menulis
RS	Pemilih register '0' untuk register inisialisasi (hanya tulis / write only) '1' untuk register data (baca dan tulis)
VLC	Pengendali terang redupnya cahaya LCD
VCC	Catu daya positif (5 V)
VSS	Catu negatif (ground)

(Sumber : Datasheet Seiko Instrument LCD, 1987)

Konfigurasi kaki pada modul LCD dapat dijelaskan pada Gambar 2-4 di bawah ini :



Gambar 2-20 Konfigurasi kaki LCD
(Sumber : Datasheet Seiko Instrument LCD, 1987)

Adapun karateristik dari LCD TM162 adalah sebagai berikut:

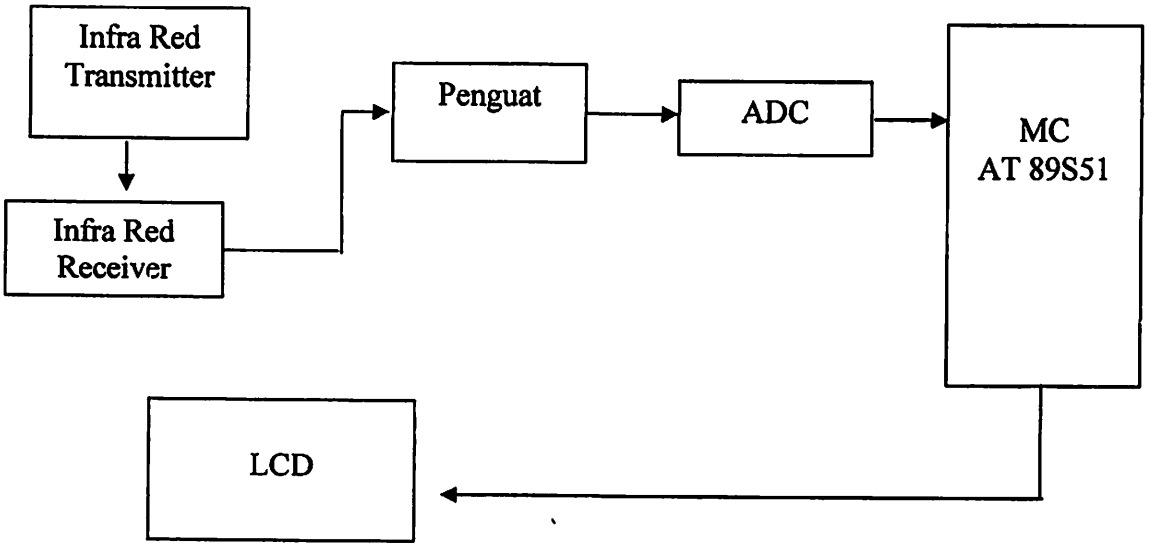
- 16x2 karakter dengan 5x7 dot matriks.
- ROM generator karakter dengan 192 tipe karakter
- RAM generator karakter dengan 8 tipe karakter (untuk program write).
- 80 x 8 bit RAM data display dengan 80 karakter maksimal
- Dapat diantarmukakan dengan MPU 4 atau 8 bit
- RAM data dan RAM generator karakter dapat dibaca dari MPU
- Rangkain osilator terpadu
- Catu daya tunggal 5V
- Reset otomatis terpadu
- Temperatur antara 0^{0}C sampai 50^{0}C

BAB III

PERENCANAAN DAN PEMBUATAN ALAT

3.1. Pendahuluan

Dalam bab ini akan dibahas mengenai perencanaan dan pembuatan alat pendeteksi suhu yang menggunakan infra red, dimana LED infra red yang merupakan led yang bisa menghasilkan sinar infra merah yang dimungkinkan untuk mendeteksi radiasi panas pada benda. Perencanaan alat ini dibuat tahap demi tahap sesuai dengan diagram blok dibawah ini :



Gambar 3-1 Diagram Blok

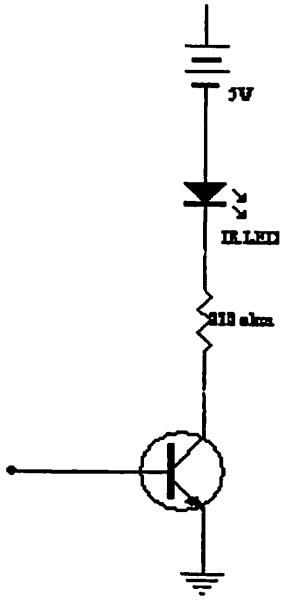
3.2 Perancangan Hardware

3.2.1 Perancangan Infra Red Transmitter

rangkaian pemancar infra red difungsikan untuk menembakkan sinar infra merah pada obyek pengukuran, dimana sinar infra merah tersebut akan membawa sinyal clock sehingga perubahan radiasi panas pada obyek pengukuran dapat terbaca oleh detector infra merah. Dimana rangkaian infra red transmitter ini merupakan suatu modul pengirim data melalui gelombang infra red.

3.2.1.1. Perancangan Rangkaian Infra Red

Infra red difungsikan sebagai media pembawa data (transmisit data) dimana sinar infra red akan ditembakkkan ke obyek sehingga radiasi panas bisa dibaca oleh detector, adapun rangkaian infra red seperti dibawah ini:



Gambar 3-2
Rangkaian Infra Red

Adapun perhitungan untuk mencari nilai Resistor yang dibutuhkan adalah sebagai berikut :

$$R = \frac{Vcc - Vled}{ILed}$$

$$= \frac{5v - 1.7v}{15mA}$$

$$= 0.22\ k\Omega = 220\ \Omega$$

Untuk perhitungan arus Colector adalah :

$$Ic = \frac{Vcc}{Rc}$$

$$= \frac{5v}{220}$$

$$= 1100\ mA$$

3.2.1.2. Rangkaian Clock

Rangkaian clock diperlukan untuk mengaktifkan sistem yang dirangkai. Pembangkitan clock digunakan multivirator astabil menggunaan IC NE 555. adapun perhitungan perencanaan perancangan adalah sebagai berikut :

T High = 0,695 (1k + 3,3k)(10μF) = 29.8 μs

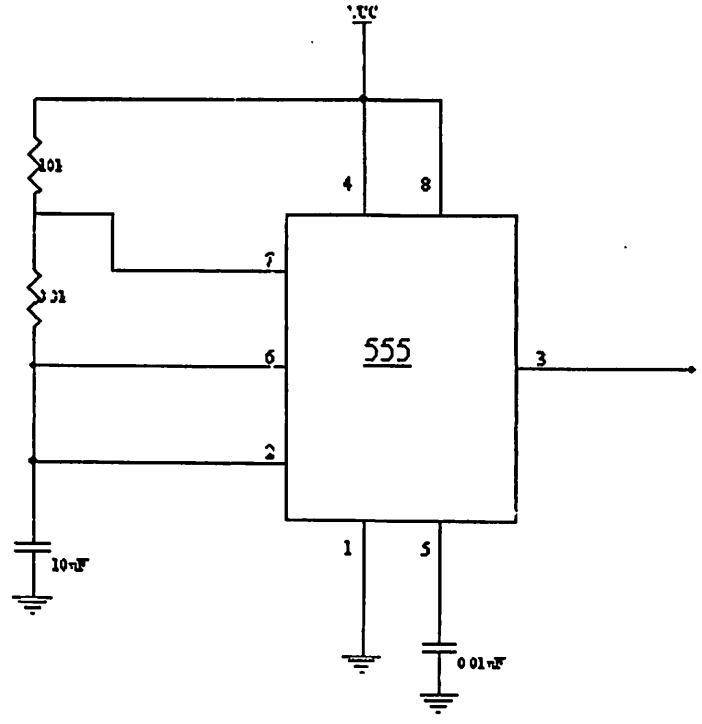
T Low = 0.695 (3.3k*10 μF) = 2.39 μs

Jadi frekuensi osilasi f adalah :

$$F = \frac{1.44}{1k + 2 * 3.3k * 10\upsilon F}$$

$$= 189.4\ Hz$$

Dari perhitungan datas bisa didapatkan kecepatan frekuensi yang dibutuhkan untuk melakukan transmit data yang berupa radiasi panas,dengan nilai frekuensi 189.4 Hz



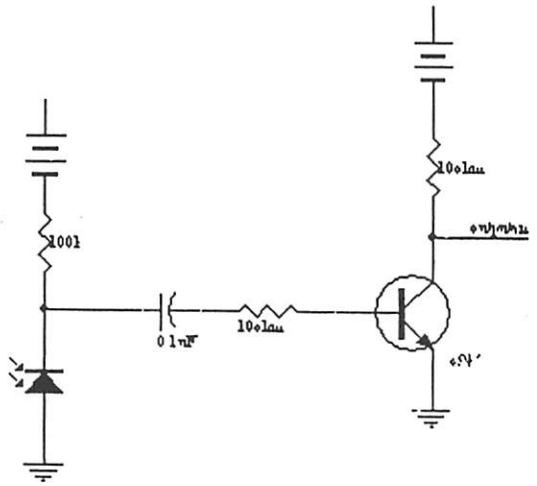
Gambar 3-3 Rangkaian clock

3.2.2. Perancangan Infra Red Receiver

pada saat rangkaian infra red receiver menerima inputtan berupa frekuensi radiasi infra red maka tegangan output yang dihasilkan akan dikuatkan lagi dikarenakan tegangan yang diterima masih kecil

3.2.2.1 Rangkaian Sensor Infra Red

Untuk menangkap perubahan data sinyal clock yang dikirim melalui LED infra red digunkaan photodiode sebagai detector. Adapun skema rangkaian sensornya adalah seperti gambar dibawah ini :



Gambar 3-4
Rangkaian Sensor Infra Red

Besarnya arus pada photodiode bergantung dari energi yang diterimanya tidak bergantung pada Ei besarnya arus ini diubah menjadi tegangan oleh R1, adapun perhitungannya adalah sebagai berikut :

$$Vo = R1.\, IL$$

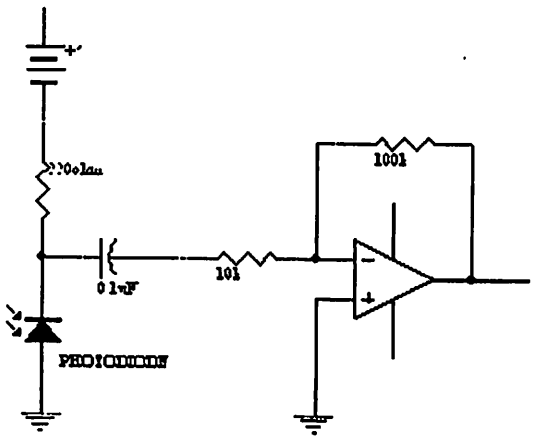
Suatu misal arus yang yang diterima oleh photodiode adalah 0,5 mA dan R1 = 10 kΩ maka :

$$Vo = 10\ k\Omega \times 0.05\ mA$$

$$= 0.5\ mV = 0.0005\ V$$

3.2.2.2. Rangkaian Penguat Inverting

Dikarenakan tegangan yang diterima oleh photodiode kecil sekali mak diperlukan penguatan sehingga outputtan yang dibutuhkan bisa diinputkan ke ADC, gambar rangkaian penguat inverting adalah sebagai berikut :



Gambar 3- 5
Rangkaian Penguat Inverting

infra red yang diterima oleh detector yaitu photodiode berupa frekuensi radiasi panas. Dikarenakan tegangan yang diterima oleh photodiode lemah maka diperlukan beberapa kali penguatan, adapun perhitungan penguatan adalah sebagai berikut :

$$Av = -\frac{Rf}{Ri} = \frac{Vo}{Ei}$$

$$Vo = -Ei\ \frac{Rf}{Ri}$$

Jika tegangan masukan dari sensor sebesar 0.05 mV maka tegangan outputannya

$$Vo = -0.05\ mV\ \frac{100k\Omega}{10k\Omega}$$

$$= 0.5\ mV$$

Dengan Av (faktor penguatannya)

$$Av = \frac{100k\Omega}{10k\Omega}$$

$$= 10 \text{ kali}$$

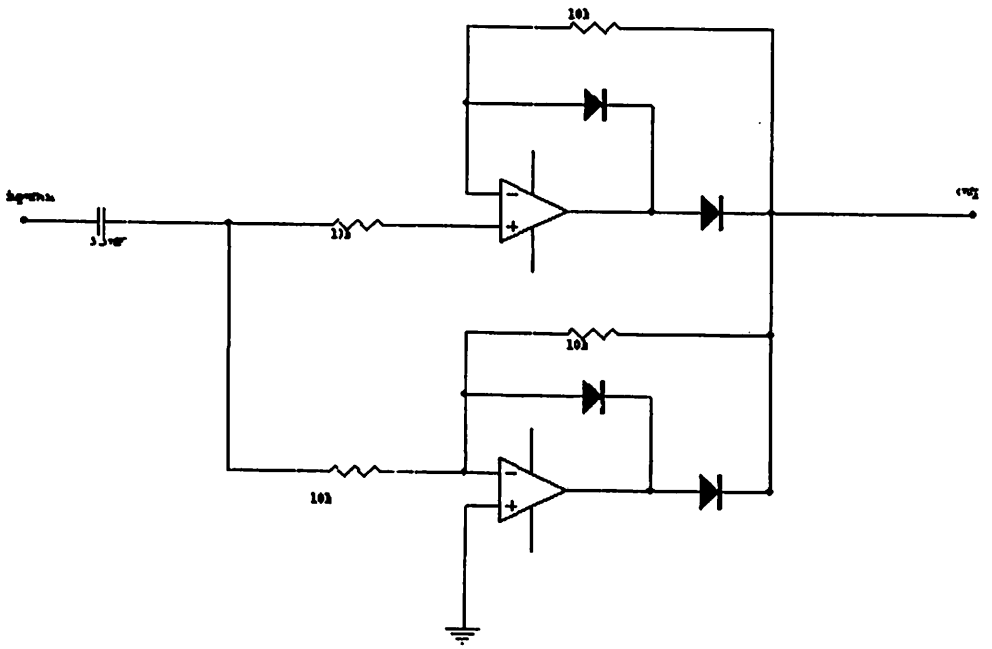
Dimana :

Av = faktor penguatan yang dibutuhkan

Vout = tegangan keluaran dari penguat Op Amp

3.2.3. Perancangan Penyearah Gelombang Penuh

untuk penguatan akhir sinyal yang diterima dari infra red receiver maka dibutuhkan rangkaian penyarah gelombang penuh, penyarah gelombang penuh berfungsi untuk pengubah tegangan AC ke DC karena sinyal outputtan masih ada yang berupa tegangan AC sebab ADC tidak bisa membaca sinyal AC untuk itulah dibutuhkan pengkondisi sinyal ini.



Gambar 3- 6
Skema Rangkaian Penyearah Gelombang Penuh

rangkaian penyarah gelombang penuh mengeluarka suatu keluaran yang sebanding dengan masukan tetapi tidak sebanding dengan polaritas masukannya. Misalnya keluarannya bisa menjadi positif pada 5V ,baik untuk masukan + 5V maupun – 5 V .

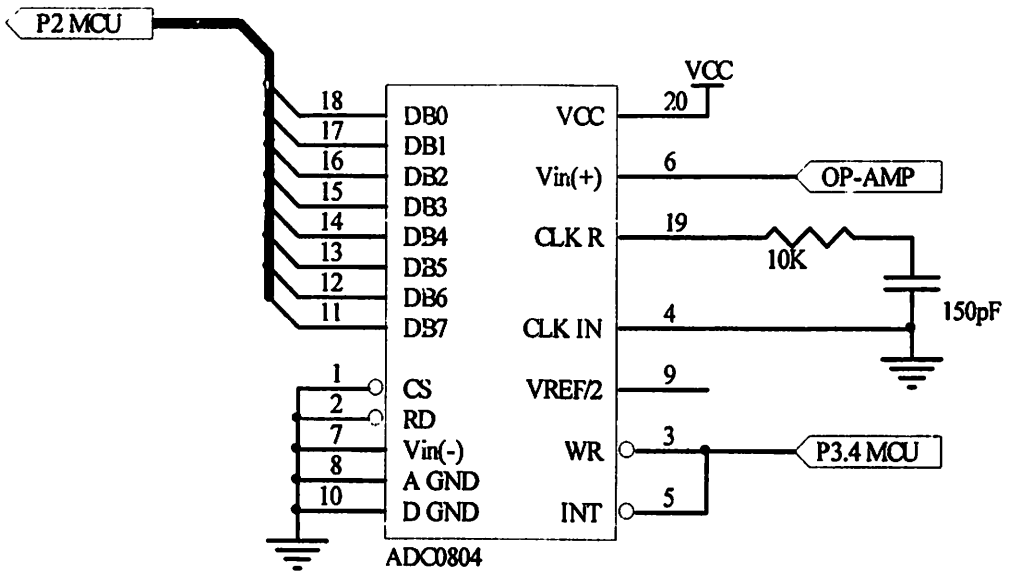
3.3. Perancangan ADC (Analog To Digital Converter)

Untuk mengkonversikan data analog dari tegangan outyput sensor pH dipergunakan IC 0804. IC ini memiliki sebuah input dan memiliki 8 output pararel. ADC memiliki *clock* generator internal.

Penjelasan rangkaian ADC :

- Untuk tegangan *referensi* ADC diperiksa tegangan sebesar 5 Volt.
- Input tegangan merupakan hasil dari tegngan output op Amp.
- Delapan output pararel akan dihubungkan ke port 2 MCU.
- Pin 3 ($\overline{WR}$) pada ADC dihubungkan ke port 6 pin 3.4 pada MCU.
- Pin 5 ($\overline{INTR}$) pada ADC dihubungkan ke PO. 7 pin 3.4 pada MCU.

Sehingga dapat digambarkan :



Gambar 3-7

Rangkaian ADC 0804

Kerja ADC 0804 0ptimum pada frekuensi *clock* sebesar 640 KHz

Dengan nilai R=10 kΩ

Maka, F*clock*=1(1.1RC)

C=142pF~150pF

F=1/(1.1RC)

$=1/(1.1x10^{4}x150x10^{-12})$

=606KHz

T*clock*=1,65us

Sehingga waktu konversi yang diperlukan adalah :

=8x T*clock*

=13,2us

Pada adc diberikan teganagan referensi sebesar 3 Volt sehingga memiliki step size :

$$\text{Step size}=V_{reff}/(2^8-1)$$

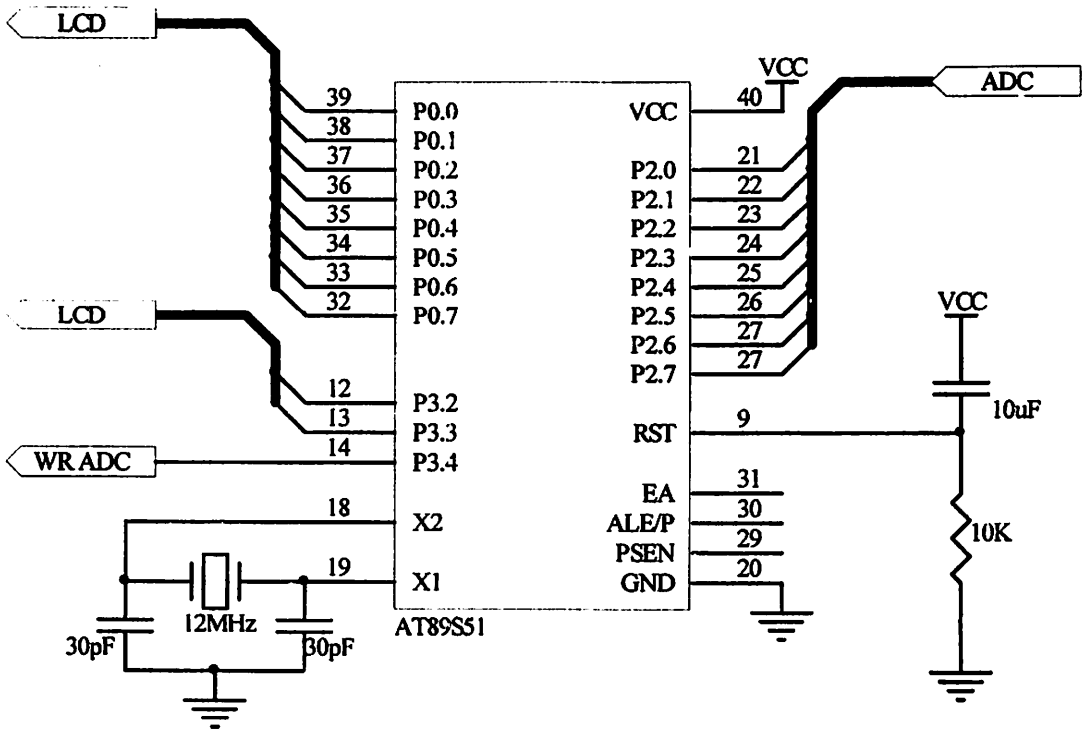
$$=5/255$$

$$=19{,}6mV\sim20mV$$

3.4. Perencanaan MCU AT89S51

AT89S51 merupakan sebuah chip tunggal sebagai pengaturan keluar masuknya data. Karena dalam sistem ini menggunakan komunikasi data serial, sehingga harus ada suatu komponen yang dapat mengubah data serial menjadi data pararel untuk diproses oleh mikrokontroller yang bekerja dalam data pararel. Ada IC khusus yang dapat menangani hal tersebut yaitu IC UART (*Universal Asyncronous Receiver Transmitter*). Dalam berbagai macam mikrokontroller ada yang dilengkapi UART diantaranya yaitu AT89S51. Alasan menggunakan produksi Atmel dengan tipe AT89S51 adalah karena mudah diperoleh dipasaran dengan harga yang relatif murah, mudah dan praktis dalam pemrograman karena mempunyai program memori tipe EEPROM. AT89S51 merupakan memori dengan teknologi nonvolatile memori, artinya isi memori tersebut dapat diisi ulang ataupun dihapus berulang kali. MCU ini merupakan rangkaian slave yang berfungsi sebagai penerima perintah- perintah dari PC.

Rangkaian sistem mikrokontroller AT89S51 sebagaimana diperlihatkan dalam gambar dibawah ini.

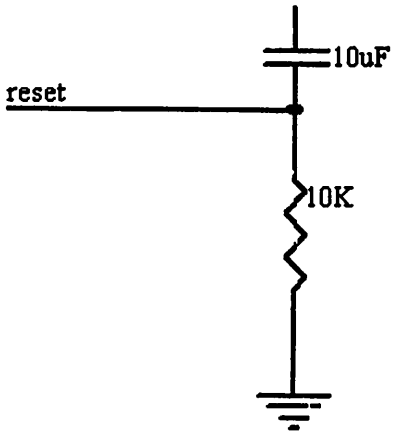


Gambar 3-8
Skema Rangkaian Koneksi AT 89S51

Port-port yang digunakan dalam system adalah :

- Port 2.0 – 2.7 (port2) difungsikan sebagai input dari ADC (Analog To Digital Converter) ADC 0804
- Port 0.0-0.7 merupakan output ke LCD sehingga data bisa ditampilkan
- Port 3.4 digunakan untuk memberikan inputan balik ke ADC apakah data sudah dibaca oleh micro
- Port 3.2 -3.3 juga merupakan outputan ke LCD
- Port 4.0 merupakan inputtan Vcc

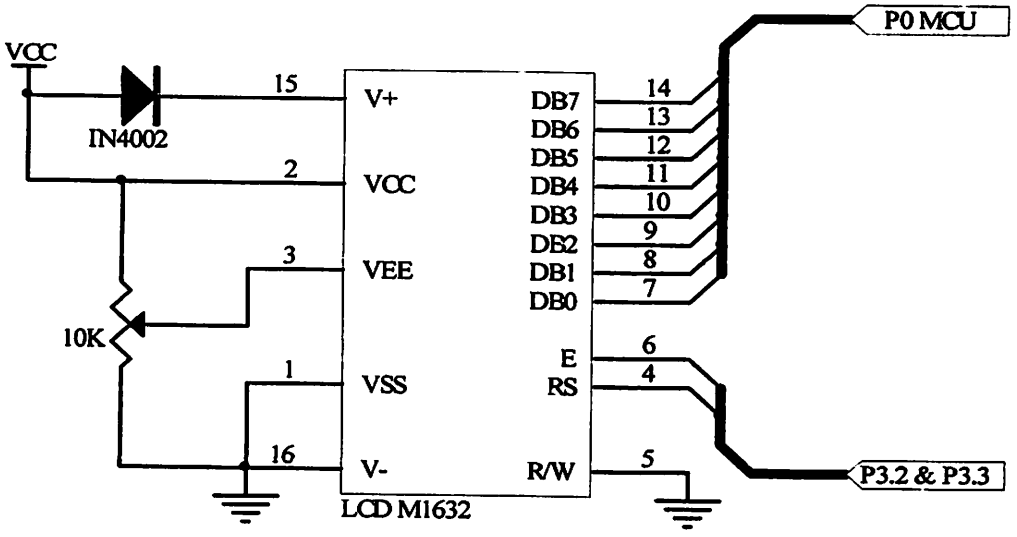
Sedangkan pada pin reset pada mikrokontroller ini dugunakan susunana RC seperti berikut :



Gambar 3 - 9
Rangkaian Reset Pada Mikrokontroller

3.5 Perancangan LCD (Liquid Crystal Display)

Pada perancangan ini digunakan LCD (Liquid Crystal Display) sebagai tampilan. LCD yang digunakan adalah jenis M1632 yang merupakan LCD dua baris dengan tiap barisnya terdiri dari 16 karakter.



Gambar 3-10
Rangkaian LCD (Liquid Crystal Display)

Port port yang digunakan lcd yang meupakam tampilan data :

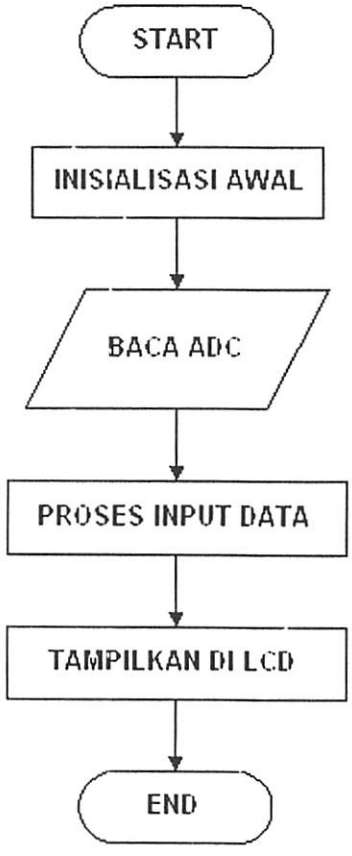
- Port DB0-DB7 merupkan output data dari microcontroller yang membawa data tampilan suhu dari pengolah ADC
- Port 3.2 dan port 3.3 yang terhubung ke port E dan RS yang merupakan sinyal pengaktif komponen '1' untuk mengaktifkan dan '0' umtuk tidak memilihnya dan juga port RS berfungsi sebagai pemilih register '0' untuk registrasi inisialisasi (hanya tulis / write only) dan '1' untuk register data (baca dan tulis)

3.6 Perancangan Perangkat Lunak

Sebelum perangkat lunak diimplementasikan kedalam bahasa pemograman,maka terlebih dahulu harus dibuat suatau flow chart alogaritma yang akan mempresentasikan kerja suatu program. Flow chart ini nantinya digunakan sebagai acuan dalam pembuatan program, namun demikian flow chart ini hanya berisikan garis besar skema perlatan yang akan dibuat seperti terlihat pada gambar dibawah ini

Software yang digunakan untuk AT89S51 disini menggunakan bahasa assembler keluarga MCS-51:

Flow Chart Program Utama Untuk Proses Tampilan Ke LCD :



Gambar 3-11
Diagram Alir Perancangan Perangkat Lunak

BAB IV

PENGUJIAN ALAT

Pada bab ini dilakukan pengujian dan pengukuran dari system yang telah dibuat. Dari pengujian dan pengukuran ini dapat diketahui apakah sistem yang dibuat dapat bekerja dengan baik atau masih ada kekurangannya. Pengujian dan pengukuran dilakukan tiap blok dari setiap fungsi kerja alat.

4.1. Pengujian Infra Red Transmitter

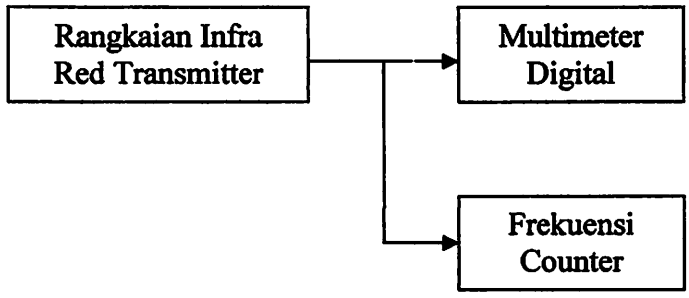
- Tujuan Pengujian

pengujian rangkaian infra red transmitter dilakukan bertujuan untuk mengetahui apakah data tegangan outputtan yang dibutuhkan pada saat pengiriman data data berupa frekuensi radiasi panas bisa dilakukan

peralatan pengujian

  - catu daya 5 Volt
  - multimeter digital
  - frekuensi counter
  - logic probe

- Prosedur Pengujian
  - menyusun pengujian rangkaian transmitter seperti yang ditunjukkan dalam gambar 4-1
  - menghubungkan catu daya ke rangkaian pengujian
  - mengukur tegangan keluaran pada outputtan



Gambar 4-1
Blok Diagram Pengujian Rangkaian Transmitter Infra Red

- Hasil Pengujian Pada Rangkaian Transmitter Infra Red

Tabel 4.1 Hasil Pengujian Rangkaian Transmitter Infra Red

Tegangan masukan (Vcc)	Tegangan Keluaran (mVolt)	Frekuensi Perhitungan (Hz)	Frekuensi Pengukuran (Hz)
5	50	189,4	122

- Analisa Hasil Pengujian

Dari tabel diatas bisa dilihat tegangan keluaran sangat kecil sekitar kisaran 0.05 mVolt. Adapun presentasi kesalahan hasil pengujian bisa dihitung dengan presentase penyimpangan :

$$\text{Presentase penyimpangan} = \frac{Fperhitungan - Fpengukuran}{Fpengukuran} \times 100\%$$

$$= \frac{189{,}4 - 122}{122} \times 100\%$$

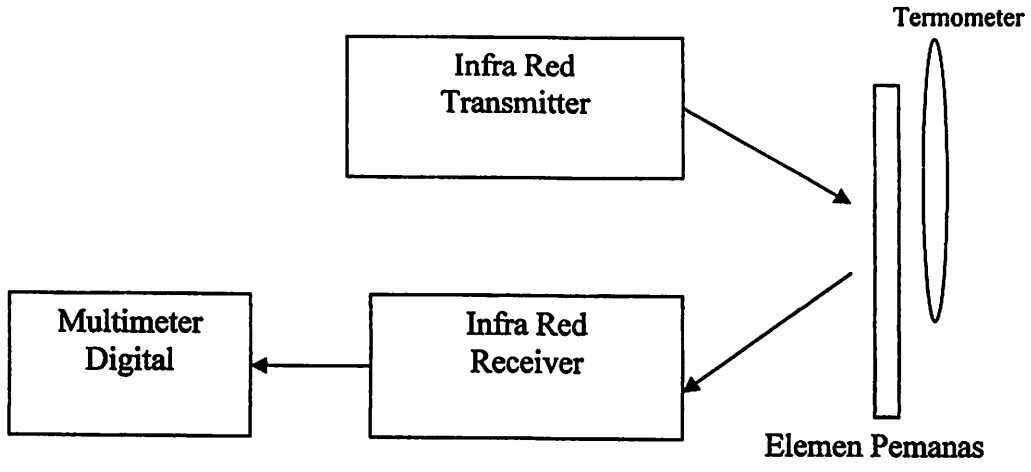
$$= 0.55\,\%$$

4.2 Pengujian Infra Red Receiver

- Tujuan Pengujian

pengujian infra red receiver bertujuan untuk mengetahui apakah photodiode dapat mendeteksi perubahan suhu pada obyek pengukuran dengan mengukur tegangan keluaran yang dihasilkan oleh photodiode. Dimana tegangan keluaran nanti akan liniear sehingga bisa diproses lebih lanjut.

- Peralatan Pengujian
    - Elemen pemanas
    - Thermometer
    - Multimeter Digital
    - Catu daya 5 Volt
- Prosedur Pengujian
    - Menyusun rangkaian pengujian infra red receiver sesuai dengan gambar 4-2
    - Menghubungkan catu daya ke rangkaian pengujian .
    - Mengaktifkan infra red transmitter guna memberikan data inputtan dengan cara menembakkan pada elemen pemanas
    - Menaikkan suhu dengan cara menyalakan elemen pemanas
    - Mengukur tegangan keluaran dengan multimeter digital
    - Jarak pengukuran pada elemen pemanas ±25 mm



Gambar 4-2
Pengujian Pada Infra Red Receiver

- Hasil Pengujian

Hasil pengujian rangkaian Infra Red Receiver ditunjukkan pada tabel 4-2

Tabel 4-2

Hasil Pengukuran Tegangan Outputtan Sensor Infra Red Receiver Terhadap Panas

Suhu Pada Elemen Pemanas	Tegangan Output (mVolt)
27	0.09
30	0.13
35	0.15
40	0.22
45	0.29
50	0.33

- Analisis Hasil Pengujian

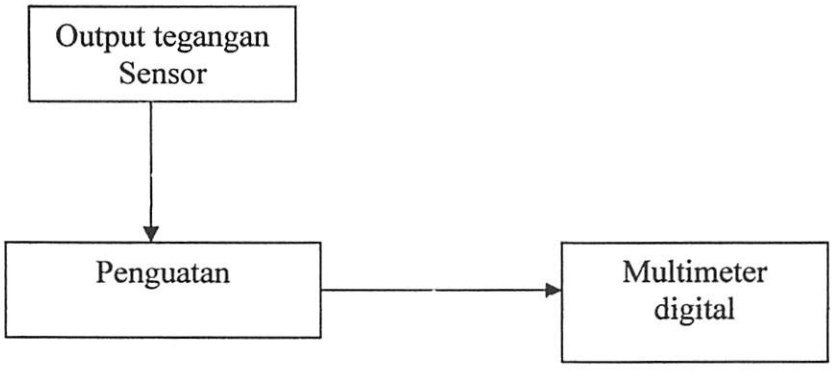
Dari tabel 4.2 bisa dilihat bahwa tegangan outputan pada sensor infra red receiver juga ikut meningkat dengan kenaikan suhu benda dengan kenaikan panas radiasi yang simultan.

4.3 Pengujian Penguatan

- Tujuan Pengujian

Tujuan pengujian rangkaian penguat adalah untuk membandingkan teganagn keluaran hasil pengamatan dengan hasil perhitungan berdasarkan tegangan pada masukkan pada tegangan outputtan pada infra receiver dengan perencanaan penguatan 10 kali.

- Peralatan Pengujian
    - Catu daya 5 volt
    - Multimeter Digital
- Prosedur Pengujian
    - Menyiapkan rangkaian penguat tegangan seperti ditunjukkan dalam Gambar 4-3
    - Memberikan tegangan variabel sebagai tegangan refrensi pada masukkan pembalik
    - Mengukur tegangan keluaran penguat dan memasukkan kedalam tabel 4-3



Gambar 4-3
Diagram Blok Pengujian Penguat

- Hasil Pengujian

Tabel 4-3 Hasil pengujian pada penguatan

Tegangan Masukan (mVolt)	Penguatan (kali)	Perhitungan (mVolt)	Pengukuran (mVolt)
0.09	10	90	110
0.13	10	130	155
0.15	10	150	180
0.22	10	220	225
0.29	10	290	310
0.33	10	330	355

- Analisis Hasil Pengujian

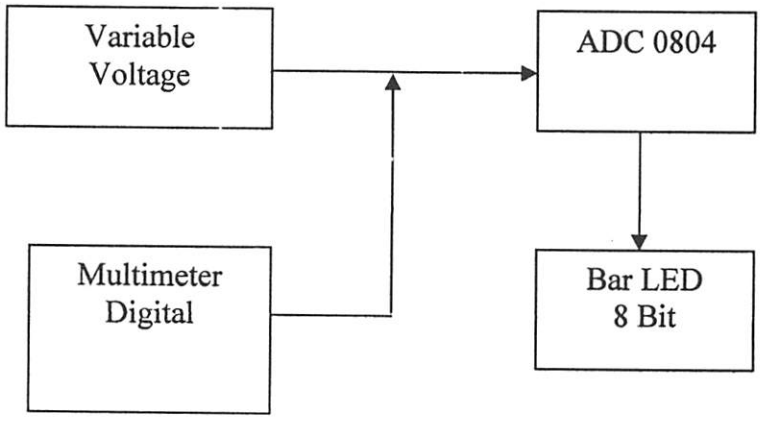
Penguat yang akan diuji adalah penguat pembalik (inverting) yang mempunyai penguatan 10 kali. Dimana proses penguatannya terjadi 3 kali proses penguatan. Dari tabel hasil pengujian bisa dilihat bahwa rangkaian tersebut mampu menguatkan tegangan masukan menjadi tegangan keluaran yang direncanakan

4.4 Pengujian ADC 0804

- Tujuan Pengujian

  Tujuan pengujian rangkaian ADC (Analog To Digital Converter) ini adalah untuk mengetahui level tegangan keluaran ADC dan Menguji serta kelineran ADC dalam mengkonversi tegangan analog kedalam nilai digital 8 Bit yang ekivalen

- Peralatan Yang Digunakan
  - Multimeter digital
  - Catu daya 5 volt
  - LED display
- Prosedur Pengujian
  - Menghubungkan masukan rangkaian ADC secara bergantian dari tegangan 0 – 5 Volt
  - Menghubungkan keluaran ADC 8 Bit dengan LED peraga untuk mengetahui keluaran nilai biner dalam mengkonversikan masukan analog ke bentuk digital
  - Mengamati dan mencatat hasil pengujian dengan memperhatikan nyala masing masing LED peraga untuk tiap-tiap masukan analog yang berbeda



Gambar 4-4
Diagram Blok Pengujian ADC 0804

- Hasil Pengujian

Hasil pengujian ADC ditunjukkan pada tabel 4.4

Tabel 4-4 Hasil Pengujian Output ADC 0804 Terhadap Variable Input

Vin ADC (mVolt)	Resolusi (Volt)	Output (Desimal)	Output (Biner)
110	0.0196	5.61	00000101
155	0.0196	7.91	00000111
180	0.0196	9.18	00001001
225	0.0196	13.0	00001101
310	0.0196	15.81	00001111
355	0.0196	18.11	00010010

- Analisis Hasil Pengujian

Dari tabel hasil pengujian dapat diketahui bahwa ADC 0804 mampu mengkonversi masukan analog 0 volt sampai 5 volt menjadi keluaran biner. Hasil konversi tersebut mendekati ADC hasil perhitungan.

Nilai kesalahan menunjukkan nilai penyimpangan data digital keluaran ADC dengan nilai sebenarnnya. Nilai kesalahan maksimum berdasarkan data yang diberikan ke ADC adalah sebesar 1 LSB .

Bobot biner 1 LSB adalah untuk sistem ini adalah :

$$\text{Resolusi} = \frac{Vref}{2^8 - 1}$$

$$= \frac{5}{256 - 1}$$

$$= 0.0196$$

Besarnya kesalahan perubahan tiap bit dapat diperoleh dengan perhitungan sebagai berikut :

$$\textit{Presentase penyimpangan perubahan bit} = \frac{0.01963 - 0.0196}{0.0196} \times 100\%$$

$$= 0.153\ \%$$

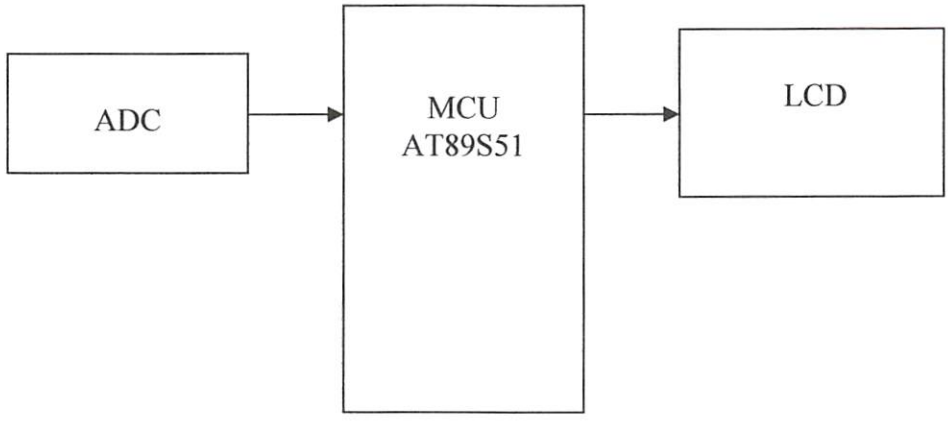
Adanya kesalahan hasil konversi ADC dapat disebabkan oleh tingkat akurasi komponen ADC 0804 sebesar 1 LSB dan kesalahan dalam pengukuran.

4.5 Pengujian LCD Sebagai Tampilan Pada Mikrokontroller

- Tujuan Pengujian

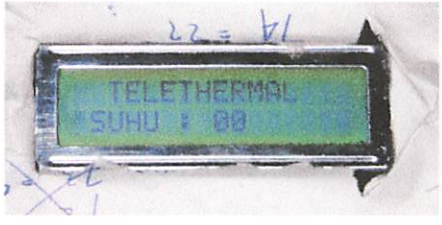
  Dalam pengujian LCD (liquid crystal Display) sebagai tampilan pada mikrokontroller untuk mengetahui LCD dapat bekerja dengan baik sehingga proses data yang diterima ADC (Analog To Digital Converter) yang kemudian diproses oleh mikrokontroller dapat ditampilkan oleh LCD.

- Prosedur Pengujian
    - Menyusun skema rangkaian pengujian sesuai dengan gambar 4-5
    - Mengaktifkan alat penguji
    - Mengamati apakah LCD bisa berfungsi



Gambar 4-5
Skema pengujian LCD sebagai tampilan pada mikrokontroller

- Hasil Pengujian



Gambar 4-6 Tampilan LCD

- Analisis Hasil Pengujian

  Dari pengujian skema diatas ternyata LCD dapat menampilkan data yang dibutuhkan

BAB V

PENUTUP

5.1 Kesimpulan

Dari perencanaan dan pembuatan alat ini dapat ditarik beberapa kesimpulan antara lain :

1. pada saat menembakkan sinar infra red pada infra red transmitter terjadi perbedaan ferkuensi pada perhitungan dan pengukuran dengan selisih presentase penyimpangan 0.55%
2. Tegangan keluaran yang dihasilkan oleh sensor Infra Red pada saat menerima inputtan tegangannya lemah untuk itulah diperlukkan penguat dengan faktor penguattan 10 kali
3. Tegangan keluaran sensor Infra Red terhadap perubahan suhu sebanding dimana terjadi peningkattan tegangan disertai dengan peningkatan suhu
4. Untuk mendapatkan hasil konversi yang bagus pada rangkaian ADC 0804 hendaknya memperhatikan Vreferensinya karena Vreferensi berpengaruh pada resolusi konversinya
5. Proses kalibrasi dilakkukan dengan pengamatan secara langsung , berapa tegangan yang keluar pada saat pengamatan suhu berlangsung

5.2 saran-saran

1. mengingat inputtan data sangat kecil maka perlu perhitungan rangkaian pengkondisi sinyal yang mantap
2. agar didapat hasil pengukuran yang sesuai harapan,maka dalam penggunaan komponen harus tepat terutama sensor infra red
3. jika melakukan pengembangan dalam alat ini,sebaiknya pada rangkaian infra red receiver digunakan sensor yang benar-benar bisa tepat membaca perubahan radiasi pada spektrum infra red

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MALANG

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Nama : Yudi Purnomo
Nim : 00.17.246
Masa Bimbingan : 18 Juli 2005 S/D 18 Januari 2006
Judul : Perencanaan Dan Pembuatan Telethermal Dengan Menggunakan Infra Red

NO	Tanggal	Uraian	Paraf Pembimbing
1	28-02-2006	BAB I & BAB II PENDAHULUAN & LANDASAN TEORI	
2	02-03-06	BAB III PERANCANGAN ALAT.	
3	08-03-06	BAB III Revisi Perencanaan Transmie. IR	
4	10-03-06	BAB III Revisi perhitungan Op Amp	
5	14-03-06	BAB IV Pengujian alat	
6	17-03-06	BAB IV Konsultasi Kesimpulan.	
7	17-03-06	Acc Seminar. Maju Comprey	
8			
9			
10			

Malang, 2005
Dosen Pembimbing

(Ir. Usman Djuanda, MM)

From. S-4a

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FORMULIR BIMBINGAN SKRIPSI

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1	30/02 2006	BAB I	
2	02/03 2006	II	
3	07/03 2006	III	
4	07/03 2006	IV	
5	07/03 2006	V	
6	10/03 2006	Seminar hasil	
7	18/03 2006	kumpul	
8			
9			
10			

Malang, 2005
Dosen Pembimbing

(Ir. Mimien Mustikawati)

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FAKULTAS TEKNOLOGI INDUSTRI
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KONSENTRASI TEKNIK ELEKTRONIKA

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2. NIM : 00 17246
3. Jurusan : Teknik Elektro S-1
4. Konsentrasi : Teknik Elektronika
5. Judul Skripsi :

PERENCANAAN DAN PEMBUATAN TELETHERMAL DENGAN MENGGUNAKAN INFRA RED

6. Tanggal Pengajuan Skripsi : 18 Juli 2005
7. Selesai menulis skripsi : 15 Maret 2006
8. Dosen Pembimbing : Ir. Usman Djuanda, MM
   Ir. Mimien Mustikawati
9. Telah Dievaluasi Dengan Nilai : 90

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JURUSAN TEKNIK ELEKTRO S-1
KONSENTRASI TEKNIK ELEKTRONIKA

FORMULIR PERBAIKAN SKRIPSI

Nama : YUDI PURNOMO

NIM : 00 17246

Masa Bimbingan : 18 Juli 2005 s/d 18 Januari 2006

Judul :

"PERENCANAAN DAN PEMBUATAN TELETHERMAL DENGAN MENGGUNAKAN INFRA RED "

Tanggal	Uraian	Paraf
21 Maret 2006	-	

Disetujui:

Penguji I

(Ir.Widodo Pudji Mulyanto, MT)

Penguji II

(M. Ibrahim Ashari, ST)

Mengetahui,

Dosen Pembimbing I

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Dosen Pembimbing II

(Ir. Mimien Mustikawati)

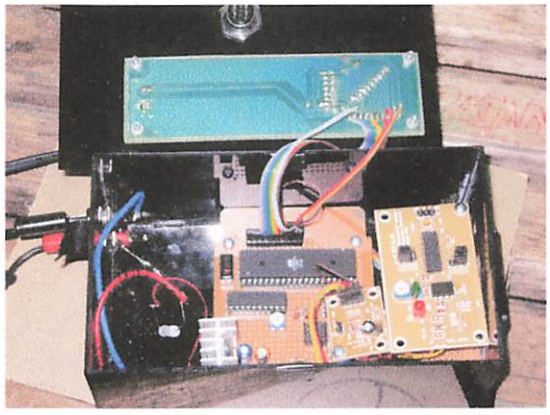

INSTITUT TEKNOLOGI NASIONAL MALANG
PERPUSTAKAAN

GAMBAR ALAT

Tampak Atas

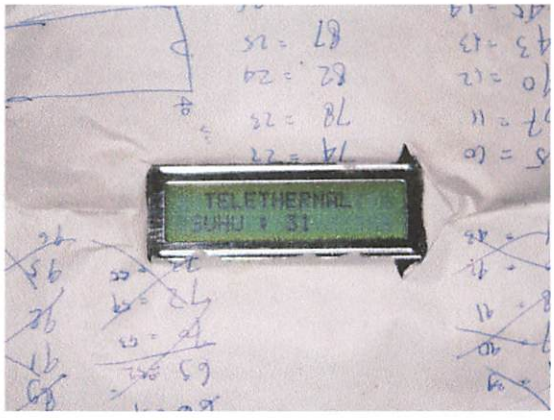
Tampak Belakang

Tampak Depan

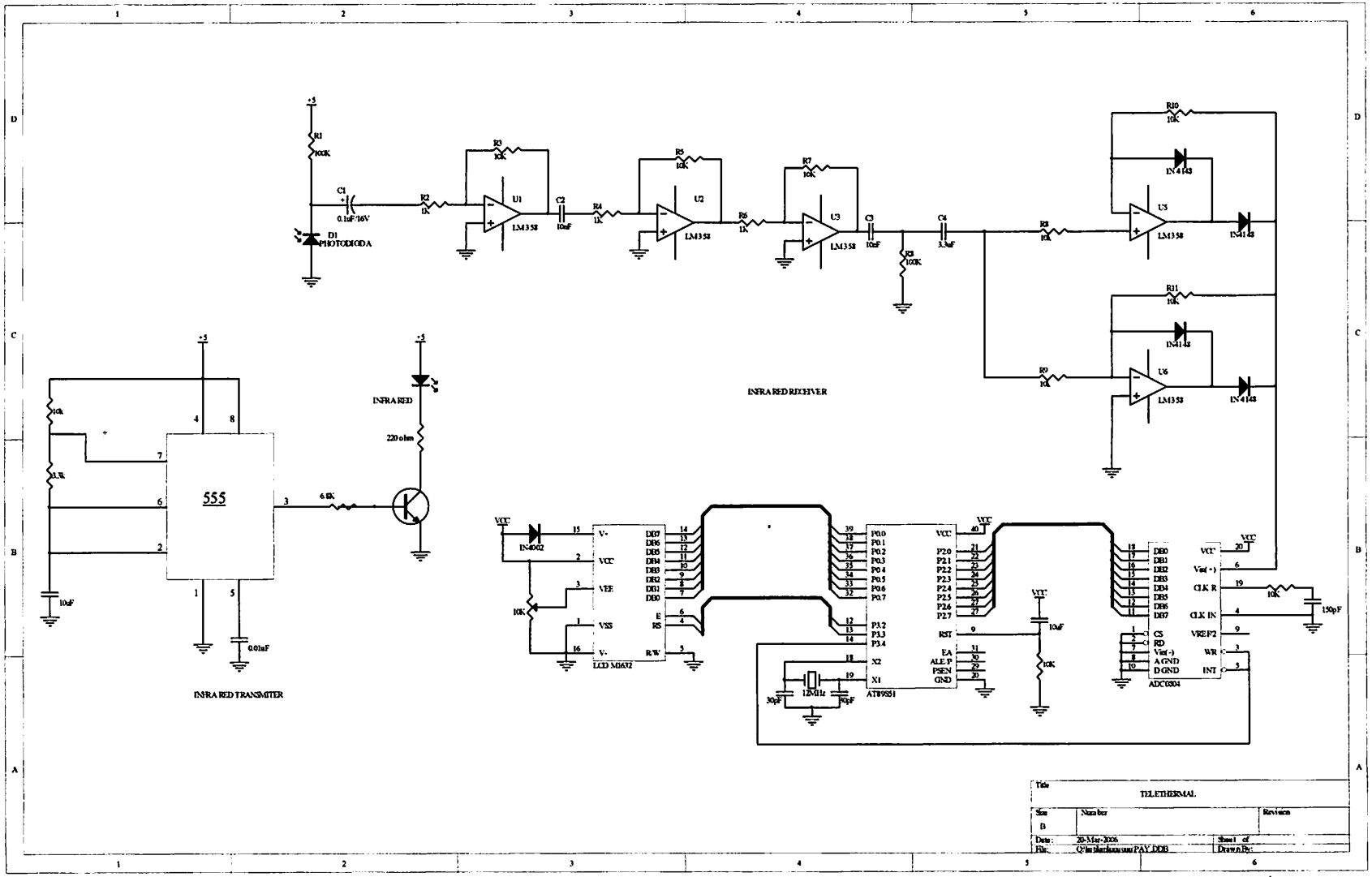


Rangkaian

Display Saat 0° C



Display Saat 30° C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R1
100K
C1
0.1uF/16V
D1
PHOTODIODA
R2
1K
U1
LM358
R3
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C2
10uF
R4
1K
U2
LM358
R5
10K
R6
1K
U3
LM358
R7
10K
C3
10uF
C4
3.3uF
R8
10K
R9
10K
R10
10K
R11
10K
IN4148
U5
U6
LM358
INFRA RED RECEIVER
555
INFRA RED
220 ohm
6.8K
3.3K
10uF
0.01uF
INFRA RED TRANSMITTER
VCC
IN4002
10K
LCD M0632
AT89S51
12MHz
30pF
ADC0804
150pF
Title
TELETHERMAL
Size
B
Number
Revision
Date:
20-Mar-2006
Sheet of
File:
Drawn By:

```
        ORG   00H
        JMP   MULAI
MULAI:      MOV   A,#03FH
        LCALL  WRITE_INST
        LCALL  WRITE_INST
        MOV   A,#0DH
        LCALL  WRITE_INST
        MOV   A,#06H
        LCALL  WRITE_INST
        MOV   A,#01H
        LCALL  WRITE_INST
        MOV   A,#0CH
        LCALL  WRITE_INST

TULIS:      MOV   DPTR,#PAYMO
        LCALL  BARISA
        CLR   P3.0
        LCALL  DELAY
        SETB  P3.0
AWALAN:     MOV   R7,P1
        CJNE  R7,#00H,TULIS1
        MOV   DPTR,#PAYMO2
        LCALL  BARISB
        LCALL  LDELAY
TULIS1:     CJNE  R7,#19H,TULIS2
        MOV   DPTR,#PAYMO3
        LCALL  BARISB
        LCALL  LDELAY
        LJMP  AWALAN
TULIS2:     CJNE  R7,#1AH,TULIS3
        MOV   DPTR,#PAYMO4
        LCALL  BARISB
        LCALL  LDELAY
        LJMP  AWALAN
TULIS3:     CJNE  R7,#1BH,TULIS4
        MOV   DPTR,#PAYMO5
        LCALL  BARISB
        LCALL  LDELAY
        LJMP  AWALAN
TULIS4:     CJNE  R7,#1CH,TULIS5
        MOV   DPTR,#PAYMO6
        LCALL  BARISB
        LCALL  LDELAY
        LJMP  AWALAN
```

```
TULIS5:    CJNE  R7,#1DH,TULIS6
           MOV   DPTR,#PAYMO7
           LCALL BARISB
           LCALL LDELAY
           LJMP  AWALAN
TULIS6:    CJNE  R7,#1EH,TULIS7
           MOV   DPTR,#PAYMO8
           LCALL BARISB
           LCALL LDELAY
           LJMP  AWALAN
TULIS7:    CJNE  R7,#1FH,TULIS8
           MOV   DPTR,#PAYMO9
           LCALL BARISB
           LCALL LDELAY
           LJMP  AWALAN
TULIS8:    CJNE  R7,#20H,TULIS9
           MOV   DPTR,#PAYMO10
           LCALL BARISB
           LCALL LDELAY
           LJMP  AWALAN
TULIS9:    CJNE  R7,#21H,TULIS10
           MOV   DPTR,#PAYMO11
           LCALL BARISB
           LCALL LDELAY
           LJMP  AWALAN
TULIS10:   CJNE  R7,#22H,TULIS11
           MOV   DPTR,#PAYMO12
           LCALL BARISB
           LCALL LDELAY
           LJMP  AWALAN
TULIS11:   CJNE  R7,#23H,TULIS12
           MOV   DPTR,#PAYMO13
           LCALL BARISB
           LCALL LDELAY
           LJMP  AWALAN
TULIS12:   CJNE  R7,#24H,TULIS13
           MOV   DPTR,#PAYMO14
           LCALL BARISB
           LCALL LDELAY
           LJMP  AWALAN
TULIS13:   CJNE  R7,#25H,TULIS14
           MOV   DPTR,#PAYMO15
           LCALL BARISB
           LCALL LDELAY
```

```
        LJMP   AWALAN
TULIS14:    CJNE   R7,#26H,TULIS15
        MOV    DPTR,#PAYMO16
        LCALL  BARISB
        LCALL  LDELAY
        LJMP   AWALAN
TULIS15:    CJNE   R7,#27H,TULIS16
        MOV    DPTR,#PAYMO17
        LCALL  BARISB
        LCALL  LDELAY
        LJMP   AWALAN
TULIS16:    CJNE   R7,#28H,TULIS17
        MOV    DPTR,#PAYMO18
        LCALL  BARISB
        LCALL  LDELAY
        LJMP   AWALAN
TULIS17:    CJNE   R7,#29H,TULIS18
        MOV    DPTR,#PAYMO19
        LCALL  BARISB
        LCALL  LDELAY
        LJMP   AWALAN
TULIS18:    CJNE   R7,#2AH,TULIS19
        MOV    DPTR,#PAYMO20
        LCALL  BARISB
        LCALL  LDELAY
        LJMP   AWALAN
TULIS19:    CJNE   R7,#2BH,TULIS20
        MOV    DPTR,#PAYMO21
        LCALL  BARISB
        LCALL  LDELAY
        LJMP   AWALAN
TULIS20:    CJNE   R7,#2CH,TULIS21
        MOV    DPTR,#PAYMO22
        LCALL  BARISB
        LCALL  LDELAY
        LJMP   AWALAN
TULIS21:    CJNE   R7,#2DH,TULIS22
        MOV    DPTR,#PAYMO23
        LCALL  BARISB
        LCALL  LDELAY
        LJMP   AWALAN
TULIS22:    CJNE   R7,#2EH,TULIS23
        MOV    DPTR,#PAYMO24
        LCALL  BARISB
```

```
        LCALL LDELAY
        LJMP  AWALAN
TULIS23:  CJNE  R7,#2FH,TULIS24
        MOV   DPTR,#PAYMO25
        LCALL BARISB
        LCALL LDELAY
        LJMP  AWALAN
TULIS24:  CJNE  R7,#30H,TULIS25
        MOV   DPTR,#PAYMO26
        LCALL BARISB
        LCALL LDELAY
        LJMP  AWALAN
TULIS25:  CJNE  R7,#31H,TULIS26
        MOV   DPTR,#PAYMO27
        LCALL BARISB
        LCALL LDELAY
        LJMP  AWALAN
TULIS26:  CJNE  R7,#32H,TULIS27
        MOV   DPTR,#PAYMO28
        LCALL BARISB
        LCALL LDELAY
        LJMP  AWALAN
TULIS27:  CJNE  R7,#33H,TULIS28
        MOV   DPTR,#PAYMO29
        LCALL BARISB
        LCALL LDELAY
        LJMP  AWALAN
TULIS28:  CJNE  R7,#34H,TULIS29
        MOV   DPTR,#PAYMO30
        LCALL BARISB
        LCALL LDELAY
        LJMP  AWALAN
TULIS29:  CJNE  R7,#35H,TULIS30
        MOV   DPTR,#PAYMO31
        LCALL BARISB
        LCALL LDELAY
        LJMP  AWALAN
TULIS30:  CJNE  R7,#36H,TULIS31
        MOV   DPTR,#PAYMO32
        LCALL BARISB
        LCALL LDELAY
        LJMP  AWALAN
TULIS31:  CJNE  R7,#37H,TULIS32
        MOV   DPTR,#PAYMO33
```

```
        LCALL  BARISB
        LCALL  LDELAY
        LJMP   AWALAN
TULIS32:    CJNE   R7,#38H,TULIS33
        MOV    DPTR,#PAYMO34
        LCALL  BARISB
        LCALL  LDELAY
        LJMP   AWALAN
TULIS33:    CJNE   R7,#39H,TULIS34
        MOV    DPTR,#PAYMO35
        LCALL  BARISB
        LCALL  LDELAY
        LJMP   AWALAN
TULIS34:    CJNE   R7,#3AH,TULIS35
        MOV    DPTR,#PAYMO36
        LCALL  BARISB
        LCALL  LDELAY
        LJMP   AWALAN
TULIS35:    CJNE   R7,#3BH,TULIS36
        MOV    DPTR,#PAYMO37
        LCALL  BARISB
        LCALL  LDELAY
        LJMP   AWALAN
TULIS36:    CJNE   R7,#3CH,TULIS37
        MOV    DPTR,#PAYMO38
        LCALL  BARISB
        LCALL  LDELAY
        LJMP   AWALAN
TULIS37:    CJNE   R7,#3DH,TULIS38
        MOV    DPTR,#PAYMO39
        LCALL  BARISB
        LCALL  LDELAY
        LJMP   AWALAN
TULIS38:    CJNE   R7,#3EH,TULIS39
        MOV    DPTR,#PAYMO40
        LCALL  BARISB
        LCALL  LDELAY
        LJMP   AWALAN
TULIS39:    CJNE   R7,#3FH,TULIS40
        MOV    DPTR,#PAYMO41
        LCALL  BARISB
        LCALL  LDELAY
        LJMP   AWALAN
TULIS40:    CJNE   R7,#40H,TULIS41
```

```
        MOV   DPTR,#PAYMO42
        LCALL  BARISB
        LCALL  LDELAY
        LJMP   AWALAN
TULIS41:    CJNE   R7,#41H,TULIS42
        MOV   DPTR,#PAYMO43
        LCALL  BARISB
        LCALL  LDELAY
        LJMP   AWALAN
TULIS42:    CJNE   R7,#42H,TULIS43
        MOV   DPTR,#PAYMO44
        LCALL  BARISB
        LCALL  LDELAY
        LJMP   AWALAN
TULIS43:    CJNE   R7,#43H,TULIS44
        MOV   DPTR,#PAYMO45
        LCALL  BARISB
        LCALL  LDELAY
        LJMP   AWALAN
TULIS44:    CJNE   R7,#44H,TULIS45
        MOV   DPTR,#PAYMO46
        LCALL  BARISB
        LCALL  LDELAY
        LJMP   AWALAN
TULIS45:    CJNE   R7,#45H,TULIS46
        MOV   DPTR,#PAYMO47
        LCALL  BARISB
        LCALL  LDELAY
        LJMP   AWALAN
TULIS46:    CJNE   R7,#46H,BINGUNG
        MOV   DPTR,#PAYMO48
        LCALL  BARISB
        LCALL  LDELAY
BINGUNG:    LJMP   AWALAN

WRITE_INST:  CLR   P2.7
WRITE:      MOV   P0,A
        CLR   P2.6
        SETB  P2.6
        LCALL  DELAY
        RET

WRITE_DATA:  SETB  P2.7
        LJMP   WRITE
```

```
BARISA:     MOV   R3,#16
            MOV   A,#80H
BB:         LCALL WRITE_INST
TULISAN:    CLR   A
            MOVC  A,@A+DPTR
            INC   DPTR
            LCALL WRITE_DATA
            DJNZ  R3,TULISAN
            RET

BARISB:     MOV   R3,#16
            MOV   A,#0C0H
            LJMP  BB

DELAY:      MOV   R0,#0
DELAY1:     MOV   R5,#50H
            DJNZ  R5,$
            DJNZ  R0,DELAY1
            RET

LDELAY:     MOV   R2,#04FH
LD1:        LCALL DELAY
            DJNZ  R2,LD1
            RET

PAYMO:      DB    ' TELETHERMAL '
PAYMO2:     DB    'SUHU : 00    '
PAYMO3:     DB    'SUHU : 25    '
PAYMO4:     DB    'SUHU : 26    '
PAYMO5:     DB    'SUHU : 27    '
PAYMO6:     DB    'SUHU : 28    '
PAYMO7:     DB    'SUHU : 29    '
PAYMO8:     DB    'SUHU : 30    '
PAYMO9:     DB    'SUHU : 31    '
PAYMO10:    DB    'SUHU : 32    '
PAYMO11:    DB    'SUHU : 33    '
PAYMO12:    DB    'SUHU : 34    '
PAYMO13:    DB    'SUHU : 35    '
PAYMO14:    DB    'SUHU : 36    '
PAYMO15:    DB    'SUHU : 37    '
PAYMO16:    DB    'SUHU : 38    '
PAYMO17:    DB    'SUHU : 39    '
PAYMO18:    DB    'SUHU : 40    '
```

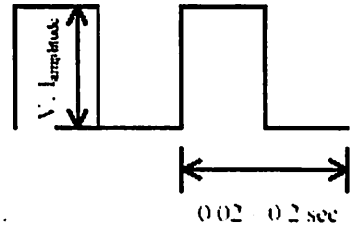
```
PAYMO19:    DB    ' SUHU : 41    '
PAYMO20:    DB    ' SUHU : 42    '
PAYMO21:    DB    ' SUHU : 43    '
PAYMO22:    DB    ' SUHU : 44    '
PAYMO23:    DB    ' SUHU : 45    '
PAYMO24:    DB    ' SUHU : 46    '
PAYMO25:    DB    ' SUHU : 47    '
PAYMO26:    DB    ' SUHU : 48    '
PAYMO27:    DB    ' SUHU : 49    '
PAYMO28:    DB    ' SUHU : 50    '
PAYMO29:    DB    ' SUHU : 51    '
PAYMO30:    DB    ' SUHU : 52    '
PAYMO31:    DB    ' SUHU : 53    '
PAYMO32:    DB    ' SUHU : 54    '
PAYMO33:    DB    ' SUHU : 55    '
PAYMO34:    DB    ' SUHU : 56    '
PAYMO35:    DB    ' SUHU : 57    '
PAYMO36:    DB    ' SUHU : 58    '
PAYMO37:    DB    ' SUHU : 59    '
PAYMO38:    DB    ' SUHU : 60    '
PAYMO39:    DB    ' SUHU : 61    '
PAYMO40:    DB    ' SUHU : 62    '
PAYMO41:    DB    ' SUHU : 63    '
PAYMO42:    DB    ' SUHU : 64    '
PAYMO43:    DB    ' SUHU : 65    '
PAYMO44:    DB    ' SUHU : 66    '
PAYMO45:    DB    ' SUHU : 67    '
PAYMO46:    DB    ' SUHU : 68    '
PAYMO47:    DB    ' SUHU : 69    '
PAYMO48:    DB    ' SUHU : 70    '

END
```

INFRARED EMITTER
OPERATING SPECIFICATIONS

TO-5 housing. Chip mounted with PVB.
Normal temperature and pressure.
Duty ratio = 1/2. F=5 Hz.
Nominal parameters(750 °C)
For other frequencies, parameters may vary.

INPUT SIGNAL WAVEFORM
Bi-polar drive voltage may be used.



Nominal parameters (750 °C)	Batch	23-18
	Window	NA
	Reflector	NA
	Atmosphere	air
	R [Ohm] in hot state	48
	Input power [mW]	1000
	$V_{amplitude}$ [V]	7.0
	$I_{amplitude}$ [mA]	140
	Decay time (50% of peak) [ms]	5.4

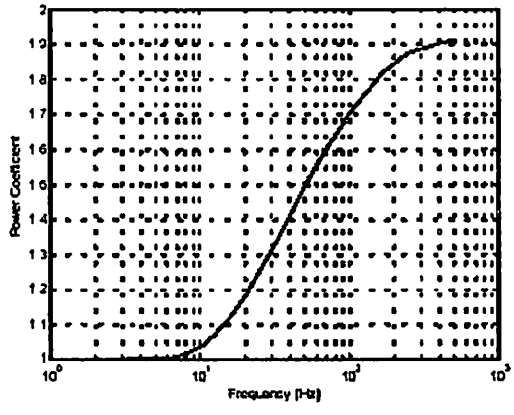
OPERATIONAL GUIDELINES

The source of the infrared radiation is a thin thermoresistive film of conducting amorphous carbon. The infrared radiation is the result of heating by passing an electric current through the film. The current can have any polarity. The maximum temperature of the film should not exceed 750°C in continuous operation. A red luminescence of the film is observed during operation at temperatures near 750°C. Short term heating (in air) up to 850 °C is possible but will reduce device lifetime.

In the specifications the pulse parameters are indicated for an emitter operating without a radiator and at ambient temperature and pressure. A rectangular voltage pulse at a frequency of 5 Hz and with a duty ratio of 50% is used for heating.

The pulsed power indicated in the specifications cannot be exceeded for longer pulses. In direct current (dc) mode, it is recommended to keep the power on the emitter below 0.9x of the pulsed power indicated in the specification.

By reducing the length of the heating pulse, the membrane will not have time to reach 750°C. The pulsed power can therefore be increased to obtain a maximum of 750°C for the membrane. The increase in power is dependent on the duty ratio and frequency. For a duty ratio of 50% the power can be increased by a factor (power coefficient) given in the figure to the right.



At very high frequencies, the temperature variation of the membrane varies insignificantly during a pulse cycle and depends on the mean power during the cycle, approaching dc conditions. The mean power should then be reduced to <0.9x of the pulsed power of the standard operating condition.

7080 N. Cathedral Rock Pl , Tucson, AZ 85718 - 520.299.9533 - fx 520.844.8255

Timer — NE/SA/SE555/SE555C

DESCRIPTION

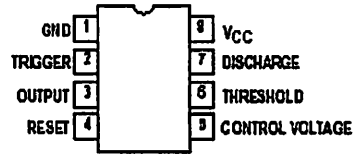
The 555 monolithic timing circuit is a highly stable controller capable of producing accurate time delays, or oscillation. In the time delay mode of operation, the time is precisely controlled by one external resistor and capacitor. For a stable operation as an oscillator, the free running frequency and the duty cycle are both accurately controlled with two external resistors and one capacitor. The circuit may be triggered and reset on falling waveforms, and the output structure can source or sink up to 200mA.

FEATURES

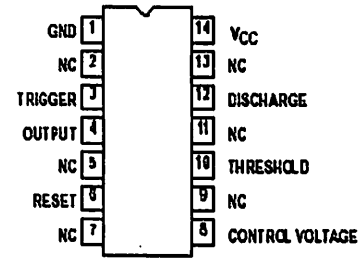
- Turn-off time less than 2µs
- Max. operating frequency greater than 500kHz
- Timing from microseconds to hours
- Operates in both astable and monostable modes
- High output current
- Adjustable duty cycle
- TTL compatible
- Temperature stability of 0.005% per °C

PIN CONFIGURATIONS

D, N, FE Packages



F Package



TOP VIEW

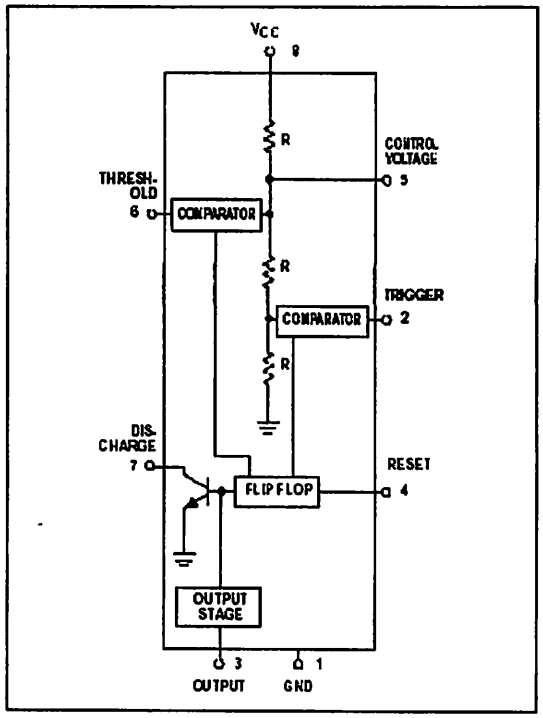
APPLICATIONS

- Precision timing
- Pulse generation
- Sequential timing
- Time delay generation
- Pulse width modulation

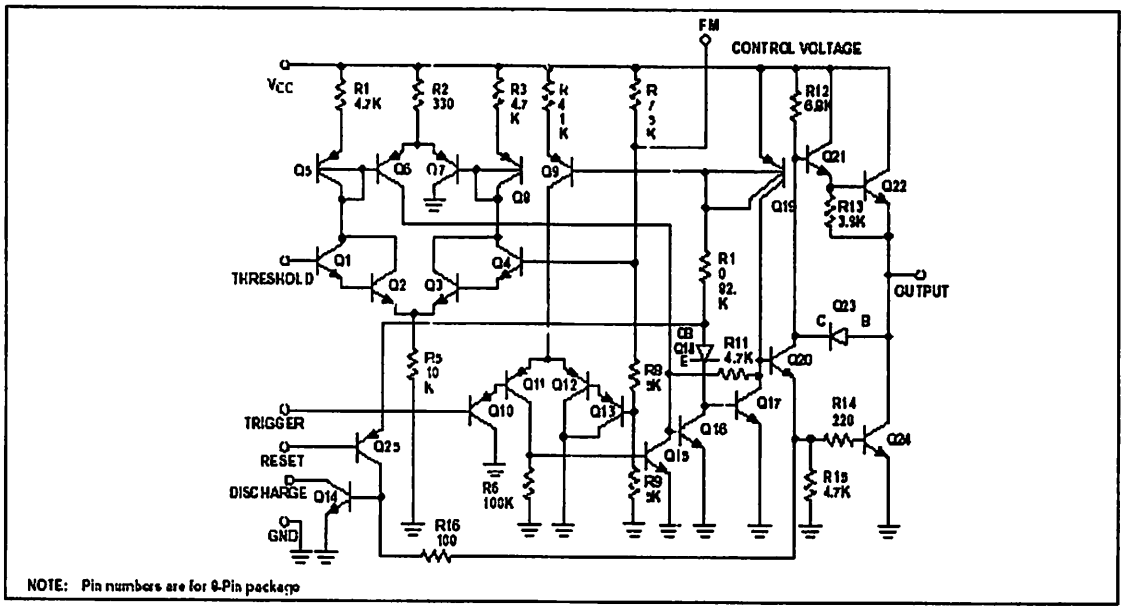
ORDERING INFORMATION

DESCRIPTION	TEMPERATURE RANGE	ORDER CODE	DWG #
8-Pin Plastic Small Outline (SO) Package	0 to +70°C	NE555D	0174C
8-Pin Plastic Dual In-Line Package (DIP)	0 to +70°C	NE555N	0404B
8-Pin Plastic Dual In-Line Package (DIP)	-40°C to +85°C	SA555N	0404B
8-Pin Plastic Small Outline (SO) Package	-40°C to +85°C	SA555D	0174C
8-Pin Hermetic Ceramic Dual In-Line Package (CERDIP)	-55°C to +125°C	SE555CFE	
8-Pin Plastic Dual In-Line Package (DIP)	-55°C to +125°C	SE555CN	0404B
14-Pin Plastic Dual In-Line Package (DIP)	-55°C to +125°C	SE555N	0405B
8-Pin Hermetic Cerdip	-55°C to +125°C	SE555FE	
14-Pin Ceramic Dual In-Line Package (CERDIP)	0 to +70°C	NE555F	0581B
14-Pin Ceramic Dual In-Line Package (CERDIP)	-55°C to +125°C	SE555F	0581B
14-Pin Ceramic Dual In-Line Package (CERDIP)	-55°C to +125°C	SE555CF	0581B

BLOCK DIAGRAM



EQUIVALENT SCHEMATIC



NOTE: Pin numbers are for 8-Pin package

ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Supply voltage		
	SE555	+18	V
	NE555, SE555C, SA555	+16	V
P_D	Maximum allowable power dissipation[1]	600	mW
T_A	Operating ambient temperature range		
	NE555	0 to +70	°C
	SA555	-40 to +85	°C
	SE555, SE555C	-55 to +125	°C
T_{STG}	Storage temperature range	-65 to +150	°C
T_{SOLD}	Lead soldering temperature (10sec max)	+300	°C

NOTES:

1. The junction temperature must be kept below 125°C for the D package and below 150°C for the FE, N and F packages. At ambient temperatures above 25°C, where this limit would be derated by the following factors:
   D package 160°C/W
   FE package 150°C/W
   N package 100°C/W
   F package 105°C/W

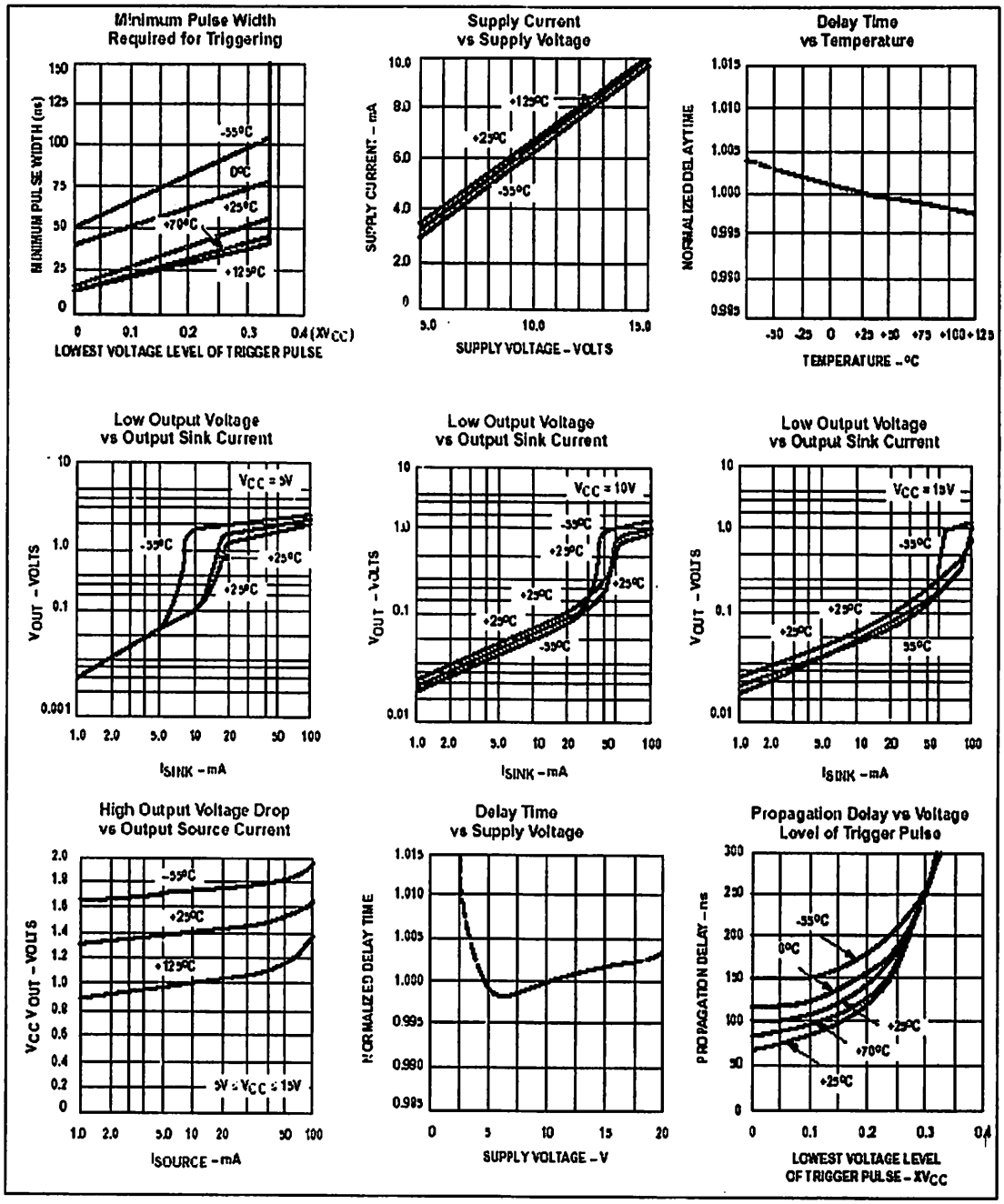
DC AND AC ELECTRICAL CHARACTERISTICS

T_A = 25°C, V_{CC} = +5V to +15 unless otherwise specified.

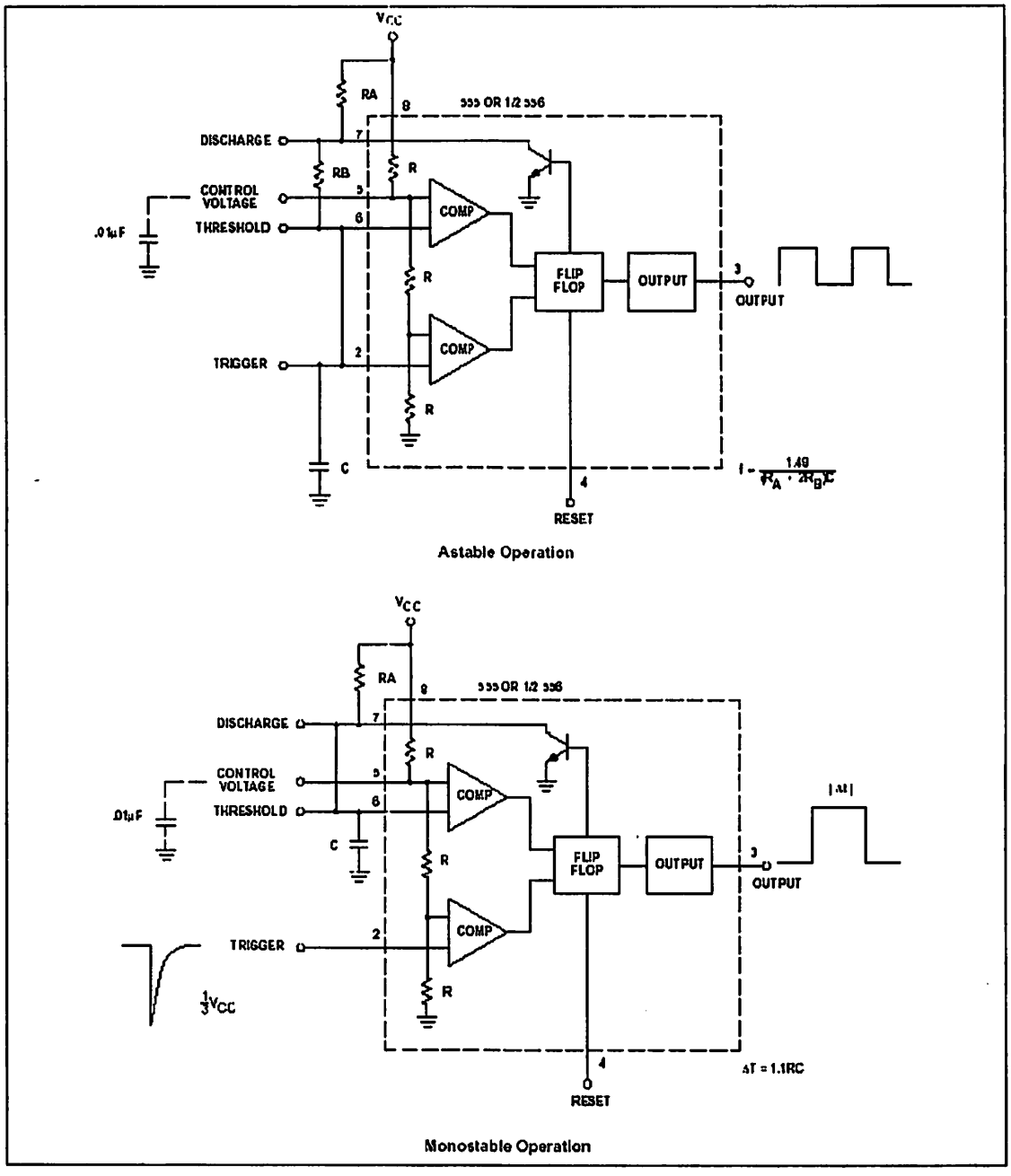
SYMBOL	PARAMETER	TEST CONDITIONS	SE555			NE555/SE555C			UNIT
			Min	Typ	Max	Min	Typ	Max	
V_{CC}	Supply voltage		4.5		18	4.5		16	V
I_{CC}	Supply current (low state)[1]	V_{CC}=5V, R_L=∞		3	5		3	6	mA
		V_{CC}=15V, R_L=∞		10	12		10	15	mA
	Timing error (monostable)	R_A=2kΩ to 100kΩ							
t_M	Initial accuracy[2]	C=0.1μF		0.5	2.0		1.0	3.0	%
$\Delta t_M/\Delta T$	Drift with temperature			30	100		50	150	ppm/°C
$\Delta t_M/\Delta V_S$	Drift with supply voltage			0.05	0.2		0.1	0.5	%/V
	Timing error (astable)	R_A, R_B=1kΩ to 100kΩ							
t_A	Initial accuracy[2]	C=0.1μF		4	6		5	13	%
$\Delta t_A/\Delta T$	Drift with temperature	V_{CC}=15V			500			500	ppm/°C
$\Delta t_A/\Delta V_S$	Drift with supply voltage			0.15	0.6		0.3	1	%/V
V_C	Control voltage level	V_{CC}=15V	9.6	10.0	10.4	9.0	10.0	11.0	V
		V_{CC}=5V	2.9	3.33	3.8	2.6	3.33	4.0	V
V_{TH}	Threshold voltage	V_{CC}=15V	9.4	10.0	10.6	8.8	10.0	11.2	V
		V_{CC}=5V	2.7	3.33	4.0	2.4	3.33	4.2	V
I_{TH}	Threshold current[3]			0.1	0.25		0.1	0.25	μA
V_{TRIG}	Trigger voltage	V_{CC}=15V	4.8	5.0	5.2	4.5	5.0	5.6	V
		V_{CC}=5V	1.45	1.67	1.9	1.1	1.67	2.2	V
I_{TRIG}	Trigger current	V_{TRIG}=0V		0.5	0.9		0.5	2.0	μA
V_{RESET}	Reset voltage[4]	V_{CC}=15V, V_{TH}=10.5V	0.3		1.0	0.3		1.0	V
I_{RESET}	Reset current	V_{RESET}=0.4V		0.1	0.4		0.1	0.4	mA
	Reset current	V_{RESET}=0V		0.4	1.0		0.4	1.5	mA
V_{OL}	Output voltage (low)	V_{CC}=15V							
		I_{SINK}=10mA		0.1	0.15		0.1	0.25	V
		I_{SINK}=50mA		0.4	0.5		0.4	0.75	V
		I_{SINK}=100mA		2.0	2.2		2.0	2.5	V
		I_{SINK}=200mA		2.5			2.5		V
		V_{CC}=5V							
		I_{SINK}=8mA		0.1	0.25		0.3	0.4	V
		I_{SINK}=5mA		0.05	0.2		0.25	0.35	V
V_{OH}	Output voltage (high)	V_{CC}=15V							
		I_{SOURCE}=200mA		12.5			12.5		V
		I_{SOURCE}=100mA	13.0	13.3		12.75	13.3		V
		V_{CC}=5V							
		I_{SOURCE}=100mA	3.0	3.3		2.75	3.3		V
t_{OFF}	Turn-off time[5]	V_{RESET}=V_{CC}		0.5	2.0		0.5	2.0	μs
t_R	Rise time of output			100	200		100	300	ns
t_F	Fall time of output			100	200		100	300	ns
	Discharge leakage current			20	100		20	100	nA

NOTES:
1. Supply current when output high typically 1mA less.
2. Tested at V_{CC}=5V and V_{CC}=15V.
3. This will determine the max value of R_A+R_B, for 15V operation, the max total R=10MΩ, and for 5V operation, the max. total R=3.4MΩ.
4. Specified with trigger input high.
5. Time measured from a positive going input pulse from 0 to 0.8×V_{CC} into the threshold to the drop from high to low of the output. Trigger is tied to threshold.

TYPICAL PERFORMANCE CHARACTERISTICS



TYPICAL APPLICATIONS



TYPICAL APPLICATIONS

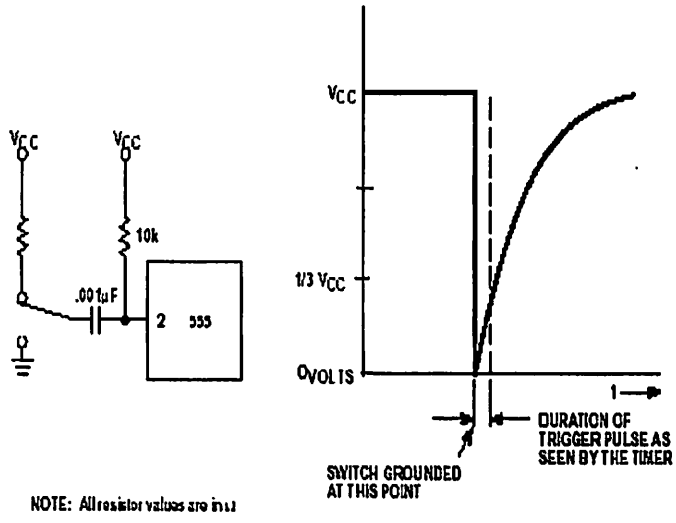


Figure 1. AC Coupling of the Trigger Pulse

Trigger Pulse Width Requirements and Time Delays

Due to the nature of the trigger circuitry, the timer will trigger on the negative going edge of the input pulse. For the device to time out properly, it is necessary that the trigger voltage level be returned to some voltage greater than one third of the supply before the time out period. This can be achieved by making either the trigger pulse sufficiently short or by AC coupling into the trigger. By AC coupling the trigger, see Figure 1, a short negative going pulse is achieved when the trigger signal goes to ground. AC coupling is most frequently used in conjunction with a switch or a signal that goes to ground which initiates the timing cycle. Should the trigger be held low, without AC coupling, for a longer duration than the timing cycle the output will remain in a high state for the duration of the low trigger signal, without regard to the threshold comparator state. This is due to the predominance of Q_{15} on the base of Q_{16}, controlling the state of the bi-stable flip-flop. When the trigger signal then returns to a high level, the output will fall immediately. Thus, the output signal will follow the trigger signal in this case.

Another consideration is the "turn-off time". This is the measurement of the amount of time required after the threshold reaches 2/3 V_{CC} to turn the output low. To explain further, Q_1 at the threshold input turns on after reaching 2/3 V_{CC}, which then turns on Q_5, which turns on Q_8. Current from Q_8 turns on Q_{18} which turns Q_{17} off. This allows current from Q_{19} to turn on Q_{20} and Q_{24} to given an output low. These steps cause the 2µs max. delay as stated in the data sheet.

Also, a delay comparable to the turn-off time is the trigger release time. When the trigger is low, Q_{10} is on and turns on Q_{11} which turns on Q_{15}. Q_{15} turns off Q_{16} and allows Q_{17} to turn on. This turns off current to Q_{20} and Q_{24}, which results in output high. When the trigger is released, Q_{10} and Q_{11} shut off, Q_{15} turns off, Q_{16} turns on and the circuit then follows the same path and time delay explained as "turn off time". This trigger release time is very important in designing the trigger pulse width so as not to interfere with the output signal as explained previously.

Photodiode Linearity and Optical Filter Transmission

Introduction

The purpose of this experiment is to demonstrate the operating characteristics of a photodiode detector and the properties of commonly-used optical filters. A very useful property of a detector is linearity, i.e. an output signal that is proportional to the intensity of light falling on the detector. Photodiodes are found to be linear over a wide range of intensities (about 10^7). Your first task in this experiment will be to verify the linearity of the photodiode, although over a smaller range of intensities. The second part of the experiment is a measurement the transmission properties of a set of optical filters, i.e. the fraction of light that each filter lets through as a function of wavelength. You will be using standard U, B, V, R, and I filters which are widely used in optical photometry.

Experimental Setup and Procedure

Photodiode Linearity

The detector is a PIN silicon photodiode (United Detector Technology Model 020A) mounted in a small rectangular box which is in turn mounted on a metal plate for mechanical stability. The diode mount resides inside a large, rectangular wooden box ($5' \times 1' \times 1'$). The box is painted black on the inside and has a lid so that it can isolate the apparatus from stray light in the room. When the photodiode is illuminated it produces a current which is measured with a Keithley electrometer (a fancy ammeter). The diode is connected to the electrometer through a pair of bulkhead connectors at the end of the box. At the other end another set of bulkhead connectors allow the quartz lamp to draw power from a transformer that sits outside the box. The arrangement is shown schematically in Figure 1.

After making checking that everything is connected properly, turn on the quartz lamp with the switch located on the transformer outside the box. Set the electrometer to read current in the μA (10^{-6} A) range. Adjust the multiplier knob so that when the quartz lamp is up close to the photodiode, the electrometer reads close to the maximum value that it can read. In the course of making measurements do not change the Ampére range switch to nA or anything else. This will change the input impedance of the electrometer and shift it to a different part of the current *vs* voltage curve. **All measurements of current should be made with the lid firmly closed. The current may take a few seconds to reach its final value after the lid is closed; wait for it to settle down before reading it off the meter.**

To adjust the intensity of light illuminating the photodiode move the lamp back and forth and measure its distance with the ruler. In addition to moving the lamp back and forth you can also insert neutral density filters in front of the lamp to reduce the intensity even further. There are three different filters available which produce an attenuation of 10^{-1}, 10^{-2}, and 10^{-1}. You should verify the attenuation produced by each filter experimentally, to be on the safe side. By combining these two techniques you can illuminate the photodiode with light spanning a fairly wide range of intensities.

When making measurements you should take proper account of any background current. Background current is current produced by the photodiode which does not result from direct illumination by the lamp. It could result from thermal noise in the material of the photodiode or from scattered light within the box. Any shiny, metal objects inside the box will scatter light and increase the background, so you should not keep any optical components in the box other than what you are using. To measure the background current you can put something between the lamp and the photodiode to stop direct light from reaching the photodiode. Then close the lid and read off any residual current produced by the photodiode. This background measurement must be made every time to change the configuration by moving the lamp or adding a neutral density filter.

Make 10 to 15 measurements of the current produced in the photodiode trying to sample as wide a range of light intensities as possible. Make sure to measure the background current *each time* and subtract it from the final current. Also, estimate the uncertainty in the intensity and in the current for each measurement. Of course, you cannot know the *absolute* intensity of the light falling on the photodiode but you should be able to determine the *relative* intensity. In your report you should explain how you determined the relative intensity (i.e., what is it relative to?). Make a plot of the current *vs* the relative intensity with error bars and check if you can fit a straight line through it by eye and measure its slope.

You should also try a quantitative assessment of the linearity of the photodiode using the χ^2 test. To simplify this exercise, ignore the errors in the intensity and use only the errors in the current. If the relationship between the current, I, and the illuminating flux, F, is of the form $I = aF + b$, then the coefficients can be determined by a least squared method through the formulae:

$$a = \frac{1}{\Delta}\left\{\left(\sum_{i=1}^{n}\frac{1}{\sigma_i^2}\right)\left(\sum_{i=1}^{n}\frac{F_i I_i}{\sigma_i^2}\right) - \left(\sum_{i=1}^{n}\frac{F_i}{\sigma_i^2}\right)\left(\sum_{i=1}^{n}\frac{I_i}{\sigma_i^2}\right)\right\}$$

and

$$b = \frac{1}{\Delta}\left\{\left(\sum_{i=1}^{n}\frac{F_i^2}{\sigma_i^2}\right)\left(\sum_{i=1}^{n}\frac{I_i}{\sigma_i^2}\right) - \left(\sum_{i=1}^{n}\frac{F_i}{\sigma_i^2}\right)\left(\sum_{i=1}^{n}\frac{F_i I_i}{\sigma_i^2}\right)\right\},$$

where

$$\Delta = \left(\sum_{i=1}^{n}\frac{1}{\sigma_i^2}\right)\left(\sum_{i=1}^{n}\frac{F_i^2}{\sigma_i^2}\right) - \left(\sum_{i=1}^{n}\frac{F_i}{\sigma_i^2}\right)^2.$$

In the above formulae, n is the number data points and F_i, I_i and σ_i denote the illuminating flux, current, and error bar on the current in the i^{th} measurement. Once the coefficients a and b have been determined, you can apply the χ^2 test to see if the best-fitting straight line is indeed consistent with the data. The definition of the reduced χ^2 for this particular straight-line fit is

$$\chi_r^2 = \frac{1}{D}\sum_{i=1}^{n}\frac{(I_i - aF_i - b)^2}{\sigma_i^2},$$

where D is the number of degrees of freedom (number of data points minus the number of free parameters). How many free parameters are there in this case? What values of χ^2 or χ^2_ν would indicate to you that a straight line is consistent with the data?

The above sums may be somewhat tedious to perform with a calculator, so you may have to resort to a computer. If you need to use a computer in the department talk to your instructor or T.A.

Optical Filter Transmission

Now that you have verified that the photodiode responds linearly to the intensity of illuminating light you can use it as a tool to measure the transmission through a set of filters as a function of wavelength. The basic principle behind this measurement is that when a filter is inserted into the beam it attenuates the light that reaches the photodiode. By measuring the intensity of the light with and without the filter in the beam the transmission properties of the filter can be determined. The transmission as a function of wavelength can be studied with the help of a monochromator, a device which uses a curved grating to select only light of a specific wavelength, which is allowed to exit the device. There is a crank on the side of the monochromator box that is used to select the wavelength. The selected wavelength is displayed on the top of the box in nanometers (1 nm = 10 Å).

The same wooden box used in the previous part of the experiment is used in this part too. However the arrangement of the apparatus inside the box is different. The new arrangement is shown in Figure 2. Light from the quartz lamp is focused by a lens onto the slit at the entrance of the monochromator. The next lens takes the light from the exit slit of the monochromator and focuses it onto the photodiode. An aluminum filter holder, which also acts as a colimator, is mounted in front of the quartz lamp housing. The purpose of the assembly of lenses is to direct all the light from the lamp to the monochromator entrance aperture and from the monochromator exit aperture to the photodiode.

You should take extra care when setting up the apparatus. Make sure that the light beam is well-aligned and well-focussed at the entrance aperture of the monochromator and at the face of the photodiode. You can use a piece of paper as a screen to trace the light path and verify the alignment. Whenever you make any change to the setup (e.g., when you change filters) there is a chance that the alignment is disturbed, so check it again before making any measurements. Since the whole point of this experiment is to measure the attenuation of light by the filters, any loss of light for other reasons, such as misalignment or poor focus, will introduce an error in the results.

Another potential source of error is the background current in the photodiode. The discussion of background current given in the photodiode linearity experiment applies here as well. Make sure to measure the background every time you change the filter (there is no need to re-measure the background if you are only adjusting the wavelength setting of the monochromator).

The first set of measurements you need to make are of the intensity of the unfiltered light from the lamp as a function of wavelength. Make measurements every 30 nm, starting at 300 nm and going up to 1020 nm. Follow all of the precautions mentioned above and in the previous section (as well as any other precautions that may seem reasonable) and try to estimate the typical uncertainty in your measurements.

When you finish the first set of measurements insert a filter into the filter holder, check the beam alignment, measure the background and repeat the whole series of measurements all over again *at the exact same wavelengths*. Measure as many filters as time permits, in the order I, R, V, B, U. If you get as far as the B and U filters you should exercise extra care with them because their transmission efficiency is low and so is the apparent intensity of the unfiltered light at those wavelengths. As a result, good measurements of the background are very important.

Construct transmission curves for the filters that you measured by dividing the filtered intensity by the unfiltered intensity, wavelength by wavelength. Plot the transmission curves *and their error bars*. From the plots determine the full width at half maximum of the filter passband. Use the measured transmission efficiencies to determine a transmission-weighted mean wavelength for each filter. The transmission-weighted mean wavelength is the first moment of the transmission curve (recall the definition of the first moment of a *properly normalized* distribution). Finally, contemplate the following questions and write your thoughts in the report

(a) Do the transmission curves that you determined depend in any way on the spectrum of the quartz lamp or the detection efficiency of the photodiode? Explain.

(b) Does the measured intensity of the unfiltered light as a function of wavelength represent the spectrum of the quartz lamp? Explain.

Lab Report

Your lab report should contain a *brief* summary of the experimental setup and procedure and a clear presentation of the results. You should answer all the little questions that are scattered around in the text and carry out all the exercises associated with the analysis of the data. The accuracy of the measurements is a major issue in this experiment so you should include a discussion of the potential sources of error, what you did to minimize their impact, and an assessment of the uncertainty in your results.

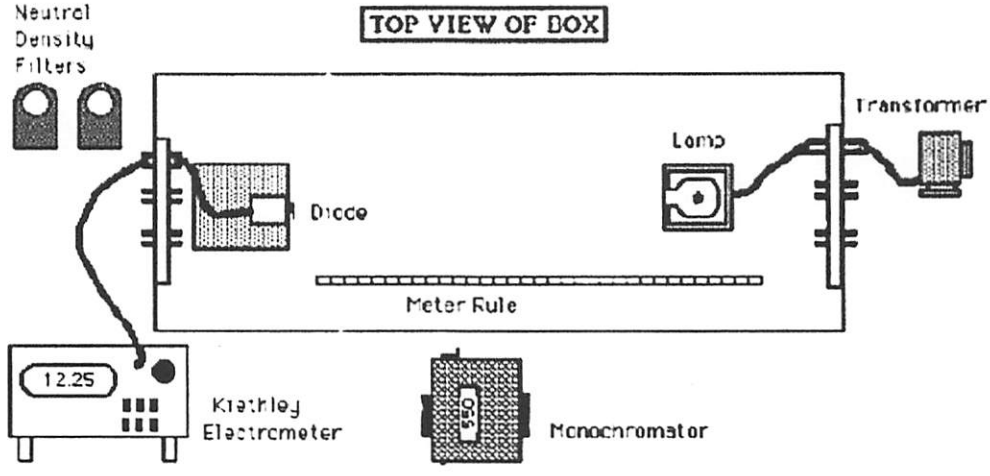


Figure 1: Schematic arrangement of the apparatus for the photodiode linearity experiment. The quartz lamp and photodiode assembly reside inside the box. The neutral density filters are used for some of the measurements.

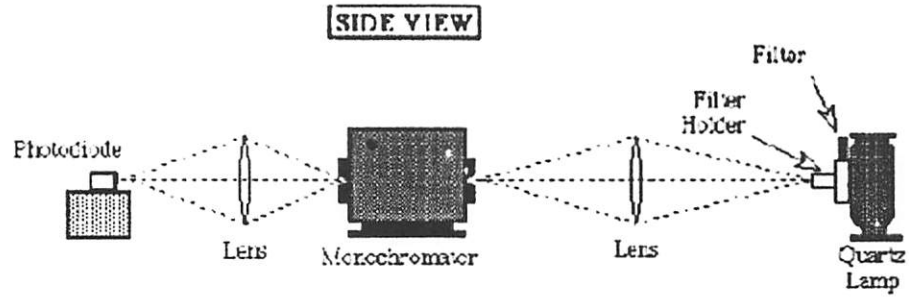


Figure 2: Schematic arrangement of the apparatus for the filter transmission measurement. This entire setup resides inside the wooden box with connections to exterior devices as shown in Figure 1. Notice the filter holder mounted in front of the lamp housing.

Photodiode-Based Detector Operates at 60 GHz

Careful design of device structure and drive circuitry yield high speed photodetector for optical detection

By: Andrew Davidson, Focused Research Inc. and Kathy Li Dessau, New Focus Inc.

With the recent advancement of gigabit fiber communication and the photonic distribution of microwave signals, there is a growing need to characterize the high-speed optical signals found in such systems. This task is typically accomplished with a high-speed photodetector followed by an instrument such as a sampling oscilloscope, a radio frequency (RF) spectrum analyzer, or a vector network analyzer. For the measurement to be a true representation of the actual signal, the speed or bandwidth of the combined measurement system should exceed that of the signal under test. The high-speed photodetector is thus an essential part of the system.

Designing a high-speed detector

Two types of photodetectors commonly used for high-speed applications are *p-i-n* and Schottky photodiodes (see Figure 1). In both devices, photon absorption in the depletion region of a reverse-biased junction creates electron-hole pairs. These carriers are swept out of the high-field region to create a current in an external circuit.

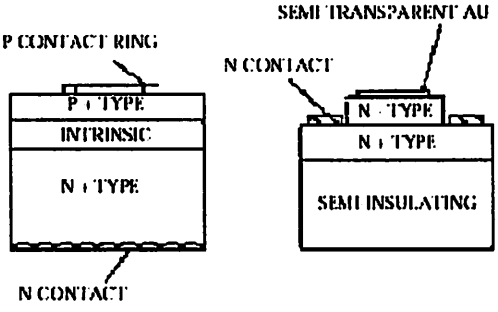


FIGURE 1: The high-field region is the intrinsic layer in the p-i-n photodiode (left) and the n-region in the Schottky photodiode (right).

The speed of these photodiodes is limited by depletion region transit time and capacitance. Transit time refers to the time required for the electrons and holes to drift across the high-field depletion region. It is determined by carrier velocity, which is constant ($\sim 3 \times 10^6$ cm/s) and the depletion region thickness t, which can vary. Depletion region thickness is thus the design parameter controlling transit time, and should be made inversely proportional to the desired bandwidth.

Capacitance slows the device via an RC time constant where the resistance is that of the device load impedance. The capacitance is proportional to the active area and inversely proportional to depletion region thickness. For high-speed operation, then, both the active area and depletion region thickness should be minimized. A small active area, however, places demanding requirements on the focusing optics for the detector. A thin depletion region means only a fraction of the incident photons will be absorbed. To optimize speed while maintaining performance, designers generally make the active area and depletion region thickness just small enough to satisfy the speed requirements; transit time is typically made comparable to the RC time constant. Using this simple approach, engineers at New Focus have designed high-speed Schottky detectors that can achieve bandwidths as high as 60 GHz.

The design team chose a Schottky configuration because it is the faster of the two designs — in the case of a *p-i-n* diode, if the top *p* -layer is absorbing, the carriers generated in this undepleted, low-field region must diffuse out at slow speeds. Schottky photodiodes also offer lower parasitic resistance. The *n* -type Schottky diode, for example, has only an *n*-layer and no *p*-layer. In a top-illuminated *n* -type diode, the carriers are created near the top metal contact; the holes, which are the slower carriers,

travel just a short distance to the metal.

The detectors have been designed for both back-side and front-side illumination. For back-side illumination, light is incident through the transparent indium phosphide (InP) substrate and absorbed in the indium gallium arsenide (InGaAs) active region, permitting detection of wavelengths from 950 nm to 1650 nm. The top Schottky contact serves as a mirror, allowing a double-pass through the absorbing layer to enhance quantum efficiency.

The front-illuminated devices are fabricated with both InGaAs and gallium arsenide (GaAs) absorbing layers and have a thin, semi-transparent gold (Au) Schottky metal. The sheet resistance of the gold is detrimental to the high-speed performance, so a current-collecting ring of thick gold is added to the periphery of the active area to minimize this resistance (see Figure 2). The devices are sensitive for wavelengths ranging from 400 nm to 1650 nm.

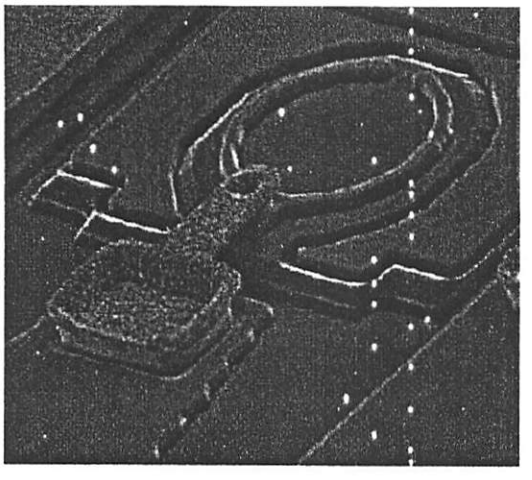


FIGURE 2: SEM of a front-illuminated InGaAs Schottky photodiode. Photo Courtesy of New Focus

Flat frequency response and ring-free impulse response detectors

An intrinsic photodiode designed for high-speed operation is necessary, but not sufficient, for high-speed optical detection. The bias circuitry and the high-speed connection to the 50-ohm output transmission line must also be carefully designed to produce the desired response. This response is dictated by the application and is generally either a flat frequency response, with the responsivity varying only slightly across the operating bandwidth, or a fast, ring-free impulse response. Fourier transform techniques show

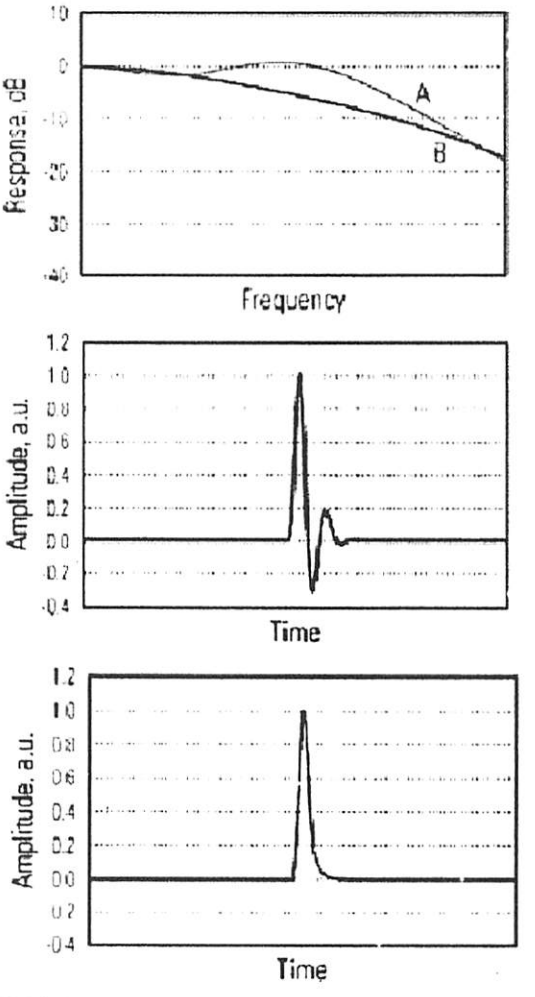


FIGURE 3: Detector designed for enhanced responsivity at high frequencies provides a nearly flat frequency response (top, curve A), but suffers from ringing in the temporal domain (middle). Detector with a clean, ring-free impulse response in the temporal domain (bottom) experiences roll off in the frequency domain, reducing the 3-dB frequency.

that the flat frequency response suffers from controlled ringing in the temporal domain (impulse response, see Figure 3). The ring-free impulse response, on the other hand, corresponds to a characteristic roll-off in the frequency domain and a corresponding reduction in the 3-dB frequency.

Recently developed time-domain optimized detectors with a fast, minimal-ringing impulse response are especially useful for digital com-

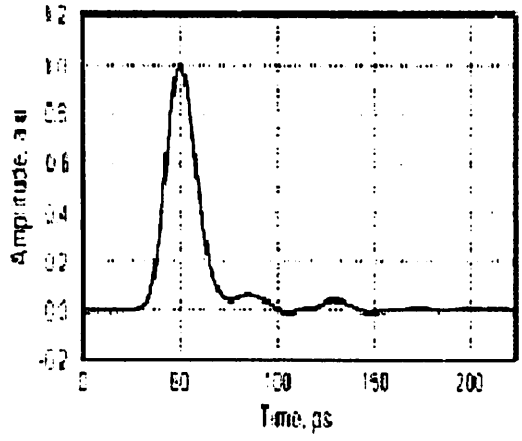


FIGURE 4: Impulse response of the Model 1414 measured with a 50-GHz scope and a 150-fs full-width-at-half-maximum input pulse at 1.06 μm shows only slight amounts on ringing.

munications applications in which spurious ringing can degrade an eye diagram and bit error rate (BER). These detectors have been designed with a resistive matching network that presents the diodes with a constant 50-ohm impedance to eliminate unwanted reflections, and also terminates the detector so that its impedance is 50 ohms. The internal 50-ohm termination makes the detectors directly compatible with BER testing using switched digital hierarchy and SONET filters. The detectors are also fabricated with on-chip bias circuitry, such as integrated bypass capacitors which provide near-ideal performance to well beyond 60 GHz.

The impulse response of a detector with an 18-ps full-width-at-half-maximum shows only a slight amount of ringing (see Figure 4). The measurement has been made with a 50-GHz sampling oscilloscope and short (less than 200 fs) pulses from a diode-pumped neodymium-doped glass (Nd:glass) laser operating at 1.06 μm. Connecting the detector module directly to the input of the oscilloscope eliminates RF cables, and the detector's fiber-optic input then receives signals from the system under test.

Detectors with a flat frequency response can be implemented with some slight inductive peaking to enhance the responsivity at higher frequencies. Such detectors are useful for applications involving the optical transmission of microwave and millimeter wave RF signals, such as wireless cellular networks or antenna remoting in military or commercial communication satellite systems.

High-speed detectors are an important component in characterizing high-bandwidth optical communications. By optimizing the photodiode for high-speed operation, and by designing the microwave circuitry to produce either a ring-free impulse response or a flat frequency response, a wide range of measurement needs can be addressed.

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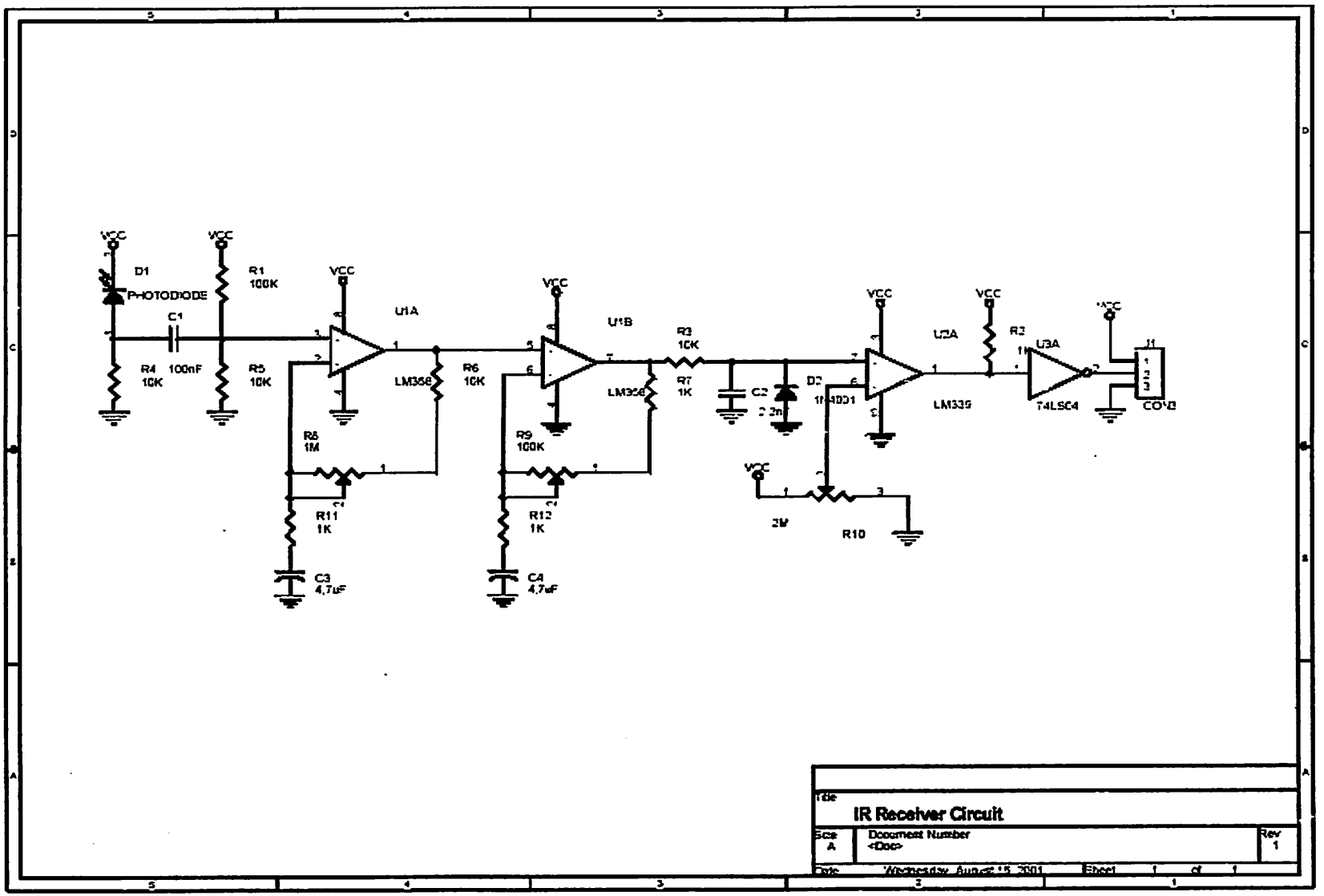
Edited by Kristin Lewotsky


VCC
D1
PHOTODIODE
C1
R1
100K
R4
10K
100nF
R5
10K
U1A
LM358
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U1B
LM358
R3
10K
R7
1K
C2
2.2n
D2
1N4001
U2A
LM339
R2
1K
U3A
74LS04
J1
CONN
R8
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R11
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Title
IR Receiver Circuit
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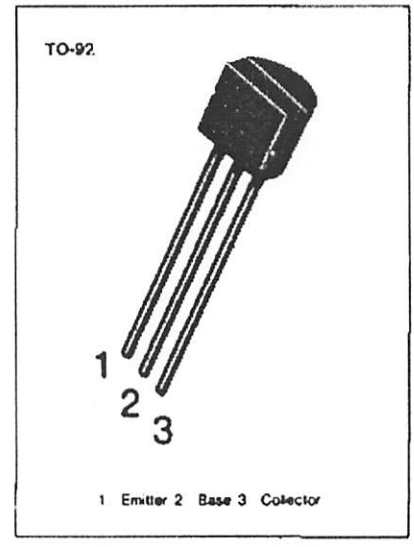
Sheet 1 of 1

Transistors
2SC9014

USHA (INDIA) LTD

PRE-AMPLIFIER, LOW LEVEL & LOW NOISE

- High total power dissipation. (PT=450mW)
- High h_{FE} and good linearity
- Complementary to SS9015



ABSOLUTE MAXIMUM RATINGS (T_a=25°C)

Characteristic	Symbol	Rating	Unit
Collector-Base Voltage	V_{CBO}	50	V
Collector-Emitter Voltage	V_{CEO}	45	V
Emitter-Base Voltage	V_{EBO}	5	V
Collector Current	I_C	100	mA
Collector Dissipation	P_C	450	mW
Junction Temperature	Tj	150	°C
Storage Temperature	Tstg	−55~150	°C

ELECTRICAL CHARACTERISTICS (T_a=25°C)

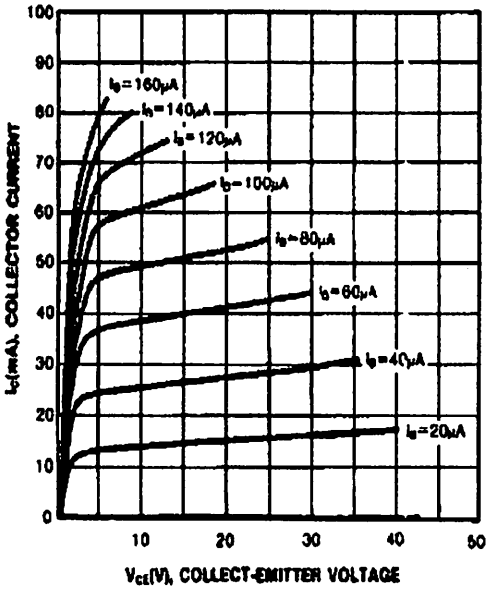
Characteristic	Symbol	Test Conditions	Min	Typ	Max	Unit
Collector-Base Breakdown Voltage	BV_{CBO}	I_C=100μA, I_E=0	50			V
Collector-Emitter Breakdown Voltage	BV_{CEO}	I_C=1mA, I_B=0	45			V
Emitter-Base Breakdown Voltage	BV_{EBO}	I_E=100μA, I_C=0	5			V
Collector Cutoff Current	I_{CBO}	V_{CB}=50V, I_E=0			50	nA
Emitter Cutoff Current	I_{EBO}	V_{EB}=5V, I_C=0			50	nA
DC Current Gain	h_{FE}	V_{CE}=5V, I_C=1mA	60	280	1000	
Collector-Base Saturation Voltage	V_{CE}(sat)	I_C=100mA, I_B=5mA		0.14	0.3	V
Base-Emitter Saturation Voltage	V_{BE}(sat)	I_C=100mA, I_B=5mA		0.84	1.0	V
Base-Emitter On Voltage	V_{BE}(on)	V_{CE}=5V, I_C=2mA	0.58	0.63	0.7	V
Output Capacitance	C_{ob}	V_{CB}=10V, I_E=0 f=1MHz		2.2	3.5	pF
Current Gain-Bandwidth Product	f_T	V_{CE}=5V, I_C=10mA	150	270		MHz
Noise Figure	NF	V_{CE}=5V, I_C=0.2mA f=1KHz, R_S=2KΩ		0.9	10	dB

h_{FE} CLASSIFICATION

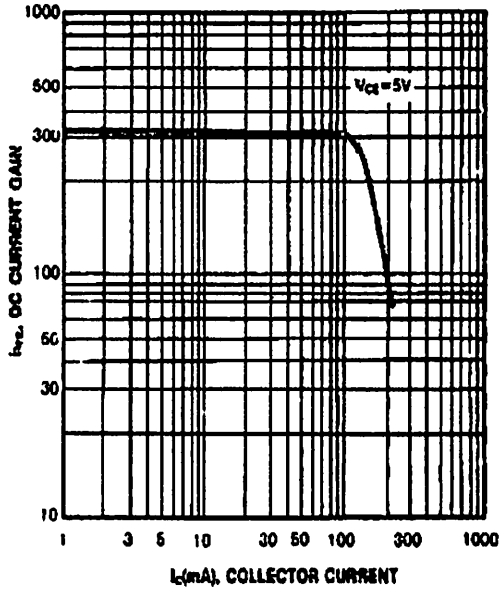
Classification	A	B	C	D
h_{FE}	60-150	100-300	200-600	400-1000

ISO 14001 CERTIFIED

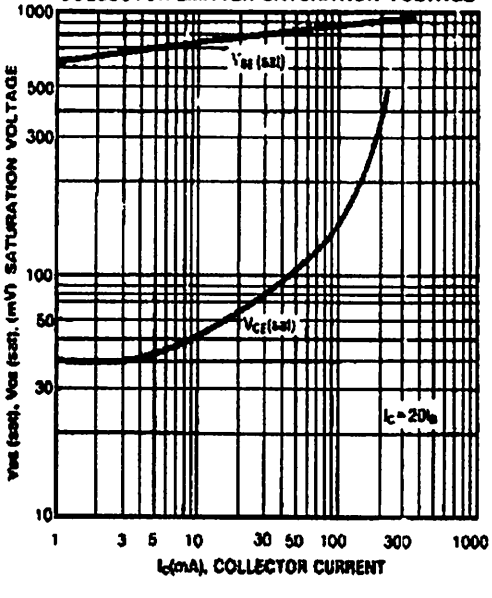
STATIC CHARACTERISTIC



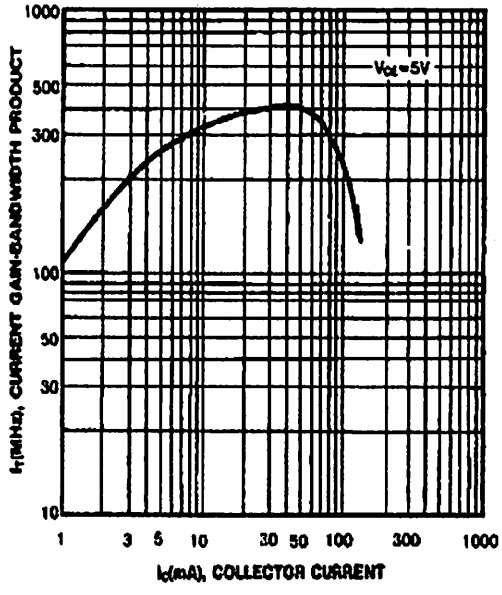
DC CURRENT GAIN



BASE-EMITTER SATURATION VOLTAGE
COLLECTOR-EMITTER SATURATION VOLTAGE



CURRENT GAIN-BANDWIDTH PRODUCT



61060	PHOTODIODE "PIGTAIL"	**Mii** OPTOELECTRONIC PRODUCTS DIVISION

Features:	**Applications:**
• Hermetically sealed • High sensitivity • Small package • Suitable for high-density pc board mounting • Spectrally matched to the 62017 series LED.	• Incremental encoding • Reflective sensors • Position sensors • Level sensors

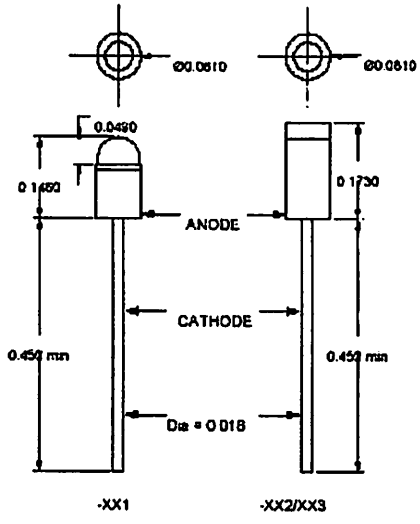
DESCRIPTION

The ***61060*** is a Silicon Photodiode in a package designed to be mounted in a single-clad printed circuit board. It is available with a wide angle flat lens or narrow angle domed lens for minimum response to stray light. High sensitivity, low dark current leakage, and low saturation voltage make this device ideal for interfacing with TTL circuits. Also available with lead attached to the case so that it may be connected without the use of a printed circuit board. Available in custom binned to customer specifications or screened to MIL-PRF-19500.

ABSOLUTE MAXIMUM RATINGS

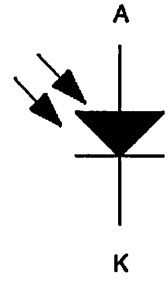
Storage Temperature	-65°C to +150°C
Operating Temperature (See part selection guide for actual operating temperature)	-55°C to +125°C
Reverse Voltage	50V
Power Dissipation (Derate at the rate of 1.67 mW/°C above 25°C)	75mW
Lead Soldering Temperature (3 minutes)	240°C

Package Dimensions



DIMENSIONS ARE IN INCHES
UNLESS OTHERWISE NOTED ALL DIMENSIONS NOMINAL

Schematic Diagram



ELECTRICAL CHARACTERISTICS

T_A = 25°C unless otherwise specified

PARAMETER		SYMBOL	MIN	TYP	MAX	UNITS	TEST CONDITIONS	NOTE
Light Current	61060-XXX	I_L	5.0	15		µA	V_R = 5.0V, H = 20mW/cm^2	1
Dark Current	61060-XXX	I_D			25	nA	V_R = 10V, H = 0	1
Reverse Breakdown Voltage	61060-XXX	V_{BR}	50			V	I_R = 5µA, H = 0	
Rise Time	61060-XXX	t_r		300		nS	V_R = 5V,	
Angular Response	61060-X01 61060-X02	θ		30 12		degrees		2

NOTES:

1. Irradiance in mW/cm^2 from a tungsten source at a color temperature of 2870K.
2. The angle between incidence for peak response and incidence for 50% of peak response.

RECOMMENDED OPERATING CONDITIONS:

PARAMETER	SYMBOL	MIN	MAX	UNITS
Reverse Voltage	V_R	5	10	V
Irradiance (H)	H	15	25	mW/cm^2

SELECTION GUIDE

PART NUMBER	PART DESCRIPTION	I_L Range
61060-001	Photodiode in coax package, domed lens, commercial version	+5µA
61060-101	Photodiode in coax package, domed lens with 100% screening	+5µA
61060-002	Photodiode in coax package, flat lens, commercial version	+5µA
61060-102	Photodiode in coax package, flat lens with 100% screening	+5µA

National Semiconductor

March 1998

LM158/LM258/LM358/LM2904
Low Power Dual Operational Amplifiers

General Description

The LM158 series consists of two independent, high gain, internally frequency compensated operational amplifiers which were designed specifically to operate from a single power supply over a wide range of voltages. Operation from split power supplies is also possible and the low power supply current drain is independent of the magnitude of the power supply voltage.

Application areas include transducer amplifiers, dc gain blocks and all the conventional op amp circuits which now can be more easily implemented in single power supply systems. For example, the LM158 series can be directly operated off of the standard +5V power supply voltage which is used in digital systems and will easily provide the required interface electronics without requiring the additional ±15V power supplies.

Unique Characteristics

- In the linear mode the input common-mode voltage range includes ground and the output voltage can also swing to ground, even though operated from only a single power supply voltage.
- The unity gain cross frequency is temperature compensated.
- The input bias current is also temperature compensated.

Advantages

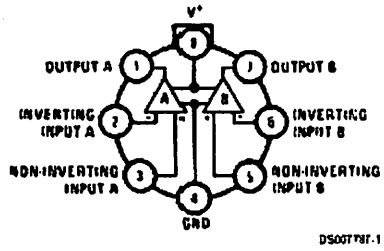
- Two internally compensated op amps in a single package
- Eliminates need for dual supplies
- Allows directly sensing near GND and V_{OUT} also goes to GND
- Compatible with all forms of logic
- Power drain suitable for battery operation
- Pin-out same as LM1558/LM1458 dual operational amplifier

Features

- Internally frequency compensated for unity gain
- Large dc voltage gain: 100 dB
- Wide bandwidth (unity gain): 1 MHz (temperature compensated)
- Wide power supply range:
  — Single supply: 3V to 32V
  — or dual supplies: ±1.5V to ±16V
- Very low supply current drain (500 µA) — essentially independent of supply voltage
- Low input offset voltage: 2 mV
- Input common-mode voltage range includes ground
- Differential input voltage range equal to the power supply voltage
- Large output voltage swing: 0V to V+ − 1.5V

Connection Diagrams (Top Views)

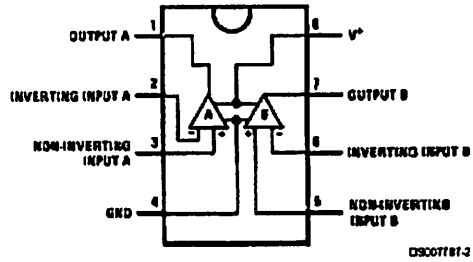
Metal Can Package



DS007787-1

Order Number LM158AH, LM158AH/883 (Note 1), LM158H, LM158H/883 (Note 1), LM258H or LM358H
See NS Package Number H08C

DIP/SO Package



DS007787-2

Order Number LM158J, LM158J/883 (Note 1), LM158AJ or LM158AJ/883 (Note 1)
See NS Package Number J08A
Order Number LM358M, LM358AM or LM2904M
See NS Package Number M08A
Order Number LM358AN, LM358N or LM2904N
See NS Package Number N08E

Note 1: LM158 is available per SMD #5962-8771001
LM158A is available per SMD #5962-8771002

Absolute Maximum Ratings (Note 10)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

	LM158/LM258/LM358 LM158A/LM258A/LM358A	LM2904
Supply Voltage, V^+	32V	26V
Differential Input Voltage	32V	26V
Input Voltage	−0.3V to +32V	−0.3V to +26V
Power Dissipation (Note 2)		
Molded DIP	830 mW	830 mW
Metal Can	550 mW	
Small Outline Package (M)	530 mW	530 mW
Output Short-Circuit to GND		
(One Amplifier) (Note 3)		
$V^+ \leq 15V$ and $T_A = 25°C$	Continuous	Continuous
Input Current ($V_{IN} < -0.3V$) (Note 4)	50 mA	50 mA
Operating Temperature Range		
LM358	0°C to +70°C	−40°C to +85°C
LM258	−25°C to +85°C	
LM158	−55°C to +125°C	
Storage Temperature Range	−65°C to +150°C	−65°C to +150°C
Lead Temperature, DIP		
(Soldering, 10 seconds)	260°C	260°C
Lead Temperature, Metal Can		
(Soldering, 10 seconds)	300°C	300°C
Soldering Information		
Dual-In-Line Package		
Soldering (10 seconds)	260°C	260°C
Small Outline Package		
Vapor Phase (60 seconds)	215°C	215°C
Infrared (15 seconds)	220°C	220°C
See AN-450 "Surface Mounting Methods and Their Effect on Product Reliability" for other methods of soldering surface mount devices.		
ESD Tolerance (Note 11)	250V	250V

Electrical Characteristics

$V^+ = +5.0V$, unless otherwise stated

Parameter	Conditions	LM158A			LM358A			LM158/LM258			Units
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
Input Offset Voltage	(Note 6), $T_A = 25°C$		1	2		2	3		2	5	mV
Input Bias Current	$I_{IN(+)}$ or $I_{IN(-)}$, $T_A = 25°C$, $V_{CM} = 0V$, (Note 7)		20	50		45	100		45	150	nA
Input Offset Current	$I_{IN(+)} - I_{IN(-)}$, $V_{CM} = 0V$, $T_A = 25°C$		2	10		5	30		3	30	nA
Input Common-Mode Voltage Range	$V^+ = 30V$, (Note 8) (LM2904, $V^+ = 26V$), $T_A = 25°C$	0		$V^+-1.5$	0		$V^+-1.5$	0		$V^+-1.5$	V
Supply Current	Over Full Temperature Range $R_L = \infty$ on All Op Amps										
	$V^+ = 30V$ (LM2904 $V^+ = 26V$)		1	2		1	2		1	2	mA
	$V^+ = 5V$		0.5	1.2		0.5	1.2		0.5	1.2	mA

Electrical Characteristics

V^+ = +5.0V, unless otherwise stated

Parameter	Conditions	LM358			LM2904			Units
		Min	Typ	Max	Min	Typ	Max	
Input Offset Voltage	(Note 6), T_A = 25°C		2	7		2	7	mV
Input Bias Current	$I_{IN(+)}$ or $I_{IN(-)}$, T_A = 25°C, V_{CM} = 0V, (Note 7)		45	250		45	250	nA
Input Offset Current	$I_{IN(+)} - I_{IN(-)}$, V_{CM} = 0V, T_A = 25°C		5	50		5	50	nA
Input Common-Mode Voltage Range	V^+ = 30V, (Note 8) (LM2904, V^+ = 26V), T_A = 25°C	0		$V^+-1.5$	0		$V^+-1.5$	V
Supply Current	Over Full Temperature Range R_L = ∞ on All Op Amps V^+ = 30V (LM2904 V^+ = 26V) V^+ = 5V		1 0.5	2 1.2		1 0.5	2 1.2	mA mA

Electrical Characteristics

V^+ = +5.0V, (Note 5), unless otherwise stated

Parameter		Conditions	LM158A			LM358A			LM158/LM258			Units
			Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
Large Signal Voltage Gain		V^+ = 15V, T_A = 25°C, R_L ≥ 2 kΩ, (For V_O = 1V to 11V)	50	100		25	100		50	100		V/mV
Common-Mode Rejection Ratio		T_A = 25°C, V_{CM} = 0V to $V^+-1.5V$	70	85		65	85		70	85		dB
Power Supply Rejection Ratio		V^+ = 5V to 30V (LM2904, V^+ = 5V to 26V), T_A = 25°C	65	100		65	100		65	100		dB
Amplifier-to-Amplifier Coupling		f = 1 kHz to 20 kHz, T_A = 25°C (Input Referred), (Note 9)		-120			-120			-120		dB
Output Current	Source	V_{IN}^+ = 1V, V_{IN}^- = 0V, V^+ = 15V, V_O = 2V, T_A = 25°C	20	40		20	40		20	40		mA
	Sink	V_{IN}^- = 1V, V_{IN}^+ = 0V, V^+ = 15V, T_A = 25°C, V_O = 2V	10	20		10	20		10	20		mA
		V_{IN}^- = 1V, V_{IN}^+ = 0V, T_A = 25°C, V_O = 200 mV, V^+ = 15V	12	50		12	50		12	50		µA
Short Circuit to Ground		T_A = 25°C, (Note 3), V^+ = 15V		40	60		40	60		40	60	mA
Input Offset Voltage		(Note 6)			4			5			7	mV
Input Offset Voltage Drift		R_S = 0Ω		7	15		7	20		7		µV/°C
Input Offset Current		$I_{IN(+)} - I_{IN(-)}$			30			75			100	nA
Input Offset Current Drift		R_S = 0Ω		10	200		10	300		10		pA/°C
Input Bias Current		$I_{IN(+)}$ or $I_{IN(-)}$		40	100		40	200		40	300	nA
Input Common-Mode Voltage Range		V^+ = 30 V, (Note 8) (LM2904, V^+ = 26V)	0		V^+-2	0		V^+-2	0		V^+-2	V

Electrical Characteristics (Continued)

V^+ = +5.0V, (Note 5), unless otherwise stated

Parameter		Conditions		LM158A			LM358A			LM158/LM258			Units
				Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
Large Signal Voltage Gain		V^+ = +15V (V_O = 1V to 11V) $R_L \geq 2$ kΩ		25			15			25			V/mV
Output Voltage	V_{OH}	V^+ = +30V	R_L = 2 kΩ	26			26			26			V
		(LM2904, V^+ = 26V)	R_L = 10 kΩ	27	28		27	28		27	28		V
Swing	V_{OL}	V^+ = 5V, R_L = 10 kΩ			5	20		5	20		5	20	mV
Output Current	Source	V_{IN}^+ = +1V, V_{IN}^- = 0V, V^+ = 15V, V_O = 2V		10	20		10	20		10	20		mA
	Sink	V_{IN}^- = +1V, V_{IN}^+ = 0V, V^+ = 15V, V_O = 2V		10	15		5	8		5	8		mA

Electrical Characteristics

V^+ = +5.0V, (Note 5), unless otherwise stated

Parameter		Conditions	LM358			LM2904			Units
			Min	Typ	Max	Min	Typ	Max	
Large Signal Voltage Gain		V^+ = 15V, T_A = 25°C, $R_L \geq 2$ kΩ, (For V_O = 1V to 11V)	25	100		25	100		V/mV
Common-Mode Rejection Ratio		T_A = 25°C, V_{CM} = 0V to V^+ − 1.5V	65	85		50	70		dB
Power Supply Rejection Ratio		V^+ = 5V to 30V (LM2904, V^+ = 5V to 26V), T_A = 25°C	65	100		50	100		dB
Amplifier-to-Amplifier Coupling		f = 1 kHz to 20 kHz, T_A = 25°C (Input Referred), (Note 9)		−120			−120		dB
Output Current	Source	V_{IN}^+ = 1V, V_{IN}^- = 0V, V^+ = 15V, V_O = 2V, T_A = 25°C	20	40		20	40		mA
	Sink	V_{IN}^- = 1V, V_{IN}^+ = 0V, V^+ = 15V, T_A = 25°C, V_O = 2V	10	20		10	20		mA
		V_{IN}^- = 1V, V_{IN}^+ = 0V, T_A = 25°C, V_O = 200 mV, V^+ = 15V	12	50		12	50		µA
Short Circuit to Ground		T_A = 25°C, (Note 3), V^+ = 15V		40	60		40	60	mA
Input Offset Voltage		(Note 6)			9			10	mV
Input Offset Voltage Drift		R_S = 0Ω		7			7		µV/°C
Input Offset Current		$I_{IN(+)} - I_{IN(-)}$			150		45	200	nA
Input Offset Current Drift		R_S = 0Ω		10			10		pA/°C
Input Bias Current		$I_{IN(+)}$ or $I_{IN(-)}$		40	500		40	500	nA
Input Common-Mode Voltage Range		V^+ = 30 V, (Note 8) (LM2904, V^+ = 26V)	0		V^+ −2	0		V^+ −2	V

Electrical Characteristics (Continued)

V^+ = +5.0V, (Note 5), unless otherwise stated

Parameter		Conditions		LM358			LM2904			Units
				Min	Typ	Max	Min	Typ	Max	
Large Signal Voltage Gain		V^+ = +15V (V_O = 1V to 11V) $R_L \geq 2\ k\Omega$		15			15			V/mV
Output Voltage	V_{OH}	V^+ = +30V	R_L = 2 kΩ	26			22			V
		(LM2904, V^+ = 26V)	R_L = 10 kΩ	27	28		23	24		V
Swing	V_{OL}	V^+ = 5V, R_L = 10 kΩ			5	20		5	100	mV
Output Current	Source	V_{IN}^+ = +1V, V_{IN}^- = 0V, V^+ = 15V, V_O = 2V		10	20		10	20		mA
	Sink	V_{IN}^- = +1V, V_{IN}^+ = 0V, V^+ = 15V, V_O = 2V		5	8		5	8		mA

Note 2: For operating at high temperatures, the LM358/LM358A, LM2904 must be derated based on a +125 C maximum junction temperature and a thermal resistance of 120 C/W which applies for the device soldered in a printed circuit board, operating in a still air ambient. The LM258/LM258A and LM158/LM158A can be derated based on a +150 C maximum junction temperature. The dissipation is the total of both amplifiers — use external resistors, where possible, to allow the amplifier to saturate or to reduce the power which is dissipated in the integrated circuit.

Note 3: Short circuits from the output to V^+ can cause excessive heating and eventual destruction. When considering short circuits to ground, the maximum output current is approximately 40 mA independent of the magnitude of V^+. At values of supply voltage in excess of +15V, continuous short-circuits can exceed the power dissipation ratings and cause eventual destruction. Destructive dissipation can result from simultaneous shorts on all amplifiers.

Note 4: This input current will only exist when the voltage at any of the input leads is driven negative. It is due to the collector-base junction of the input PNP transistors becoming forward biased and thereby acting as input diode clamps. In addition to this diode action, there is also lateral NPN parasitic transistor action on the IC chip. This transistor action can cause the output voltages of the op amps to go to the V^+ voltage level (or to ground for a large overdrive) for the time duration that an input is driven negative. This is not destructive and normal output states will re-establish when the input voltage, which was negative, again returns to a value greater than −0.3V (at 25 C).

Note 5: These specifications are limited to −55 C ≤ T_A ≤ +125 C for the LM158/LM158A. With the LM258/LM258A, all temperature specifications are limited to −25 C ≤ T_A ≤ +85 C. The LM358/LM358A temperature specifications are limited to 0 C ≤ T_A ≤ +70 C, and the LM2904 specifications are limited to −40 C ≤ T_A ≤ +85 C.

Note 6: V_O = 1.4V, R_S = 0Ω with V^+ from 5V to 30V; and over the full input common-mode range (0V to V^+ −1.5V) at 25 C. For LM2904, V^+ from 5V to 26V.

Note 7: The direction of the input current is out of the IC due to the PNP input stage. This current is essentially constant, independent of the state of the output so no loading change exists on the input lines.

Note 8: The input common-mode voltage of either input signal voltage should not be allowed to go negative by more than 0.3V (at 25 C). The upper end of the common-mode voltage range is V^+ −1.5V (at 25 C), but either or both inputs can go to +32V without damage (+26V for LM2904), independent of the magnitude of V^+.

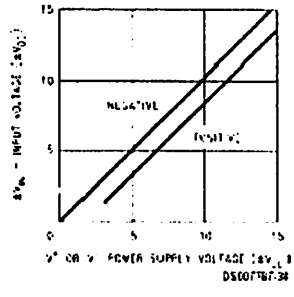
Note 9: Due to proximity of external components, insure that coupling is not originating via stray capacitance between these external parts. This typically can be detected as this type of capacitance increases at higher frequencies.

Note 10: Refer to RETS158AX for LM158A military specifications and to RETS158X for LM158 military specifications.

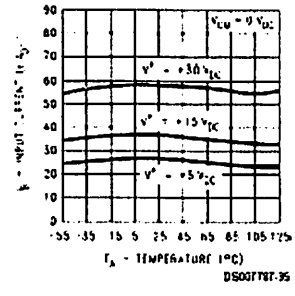
Note 11: Human body model, 1.5 kΩ in series with 100 pF.

Typical Performance Characteristics

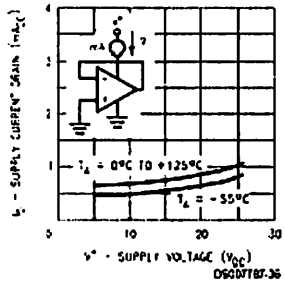
Input Voltage Range



Input Current

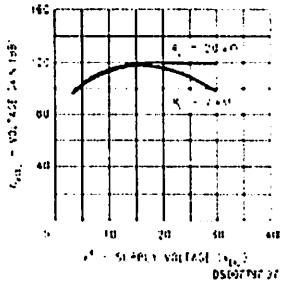


Supply Current

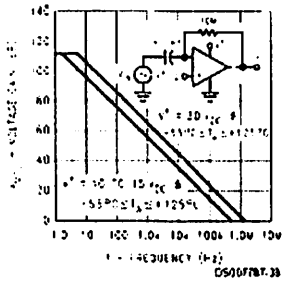


Typical Performance Characteristics (Continued)

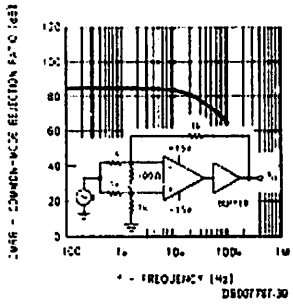
Voltage Gain



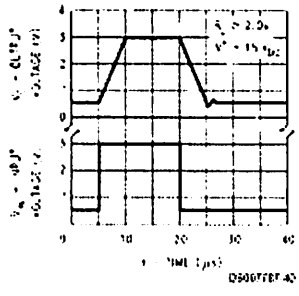
Open Loop Frequency Response



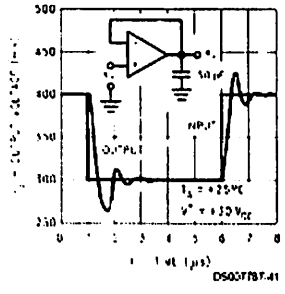
Common-Mode Rejection Ratio



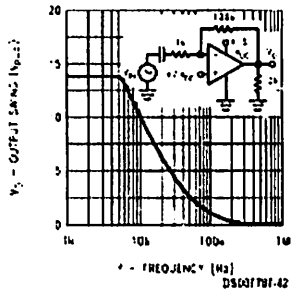
Voltage Follower Pulse Response



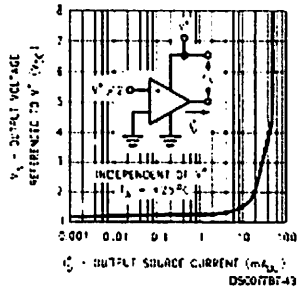
Voltage Follower Pulse Response (Small Signal)



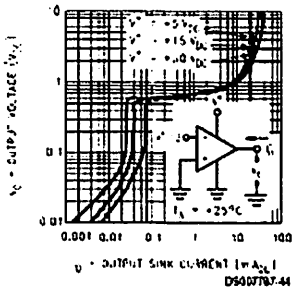
Large Signal Frequency Response



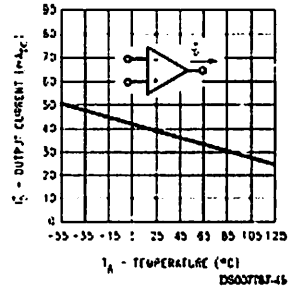
Output Characteristics Current Sourcing



Output Characteristics Current Sinking

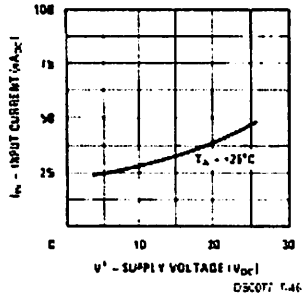


Current Limiting

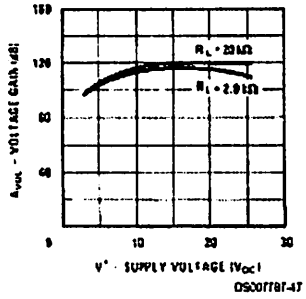


Typical Performance Characteristics (Continued)

Input Current (LM2902 only)



Voltage Gain (LM2902 only)



Application Hints

The LM158 series are op amps which operate with only a single power supply voltage, have true-differential inputs, and remain in the linear mode with an input common-mode voltage of 0 V_{DC}. These amplifiers operate over a wide range of power supply voltage with little change in performance characteristics. At 25°C amplifier operation is possible down to a minimum supply voltage of 2.3 V_{DC}.

Precautions should be taken to insure that the power supply for the integrated circuit never becomes reversed in polarity or that the unit is not inadvertently installed backwards in a test socket as an unlimited current surge through the resulting forward diode within the IC could cause fusing of the internal conductors and result in a destroyed unit.

Large differential input voltages can be easily accomodated and, as input differential voltage protection diodes are not needed, no large input currents result from large differential input voltages. The differential input voltage may be larger than V⁺ without damaging the device. Protection should be provided to prevent the input voltages from going negative more than -0.3 V_{DC} (at 25°C). An input clamp diode with a resistor to the IC input terminal can be used.

To reduce the power supply current drain, the amplifiers have a class A output stage for small signal levels which converts to class B in a large signal mode. This allows the amplifiers to both source and sink large output currents. Therefore both NPN and PNP external current boost transistors can be used to extend the power capability of the basic amplifiers. The output voltage needs to raise approximately 1 diode drop above ground to bias the on-chip vertical PNP transistor for output current sinking applications.

For ac applications, where the load is capacitively coupled to the output of the amplifier, a resistor should be used, from the output of the amplifier to ground to increase the class A bias current and prevent crossover distortion. Where the load is directly coupled, as in dc applications, there is no crossover distortion.

Capacitive loads which are applied directly to the output of the amplifier reduce the loop stability margin. Values of 50 pF can be accomodated using the worst-case non-inverting unity gain connection. Large closed loop gains or resistive isolation should be used if larger load capacitance must be driven by the amplifier.

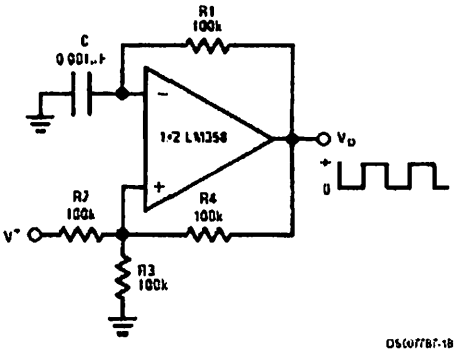
The bias network of the LM158 establishes a drain current which is independent of the magnitude of the power supply voltage over the range of 3 V_{DC} to 30 V_{DC}.

Output short circuits either to ground or to the positive power supply should be of short time duration. Units can be destroyed, not as a result of the short circuit current causing metal fusing, but rather due to the large increase in IC chip dissipation which will cause eventual failure due to excessive function temperatures. Putting direct short-circuits on more than one amplifier at a time will increase the total IC power dissipation to destructive levels, if not properly protected with external dissipation limiting resistors in series with the output leads of the amplifiers. The larger value of output source current which is available at 25°C provides a larger output current capability at elevated temperatures (see typical performance characteristics) than a standard IC op amp.

The circuits presented in the section on typical applications emphasize operation on only a single power supply voltage. If complementary power supplies are available, all of the standard op amp circuits can be used. In general, introducing a pseudo-ground (a bias voltage reference of V⁺/2) will allow operation above and below this value in single power supply systems. Many application circuits are shown which take advantage of the wide input common-mode voltage range which includes ground. In most cases, input biasing is not required and input voltages which range to ground can easily be accommodated.

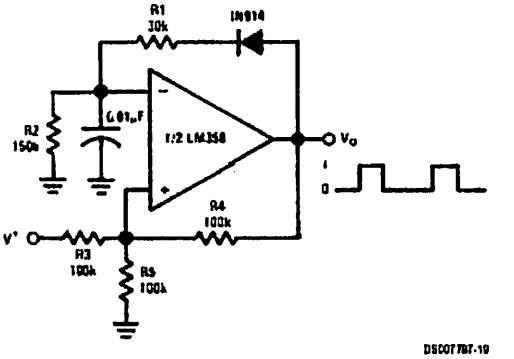
Typical Single-Supply Applications ($V^+ = 5.0\ V_{DC}$) (Continued)

Squarewave Oscillator



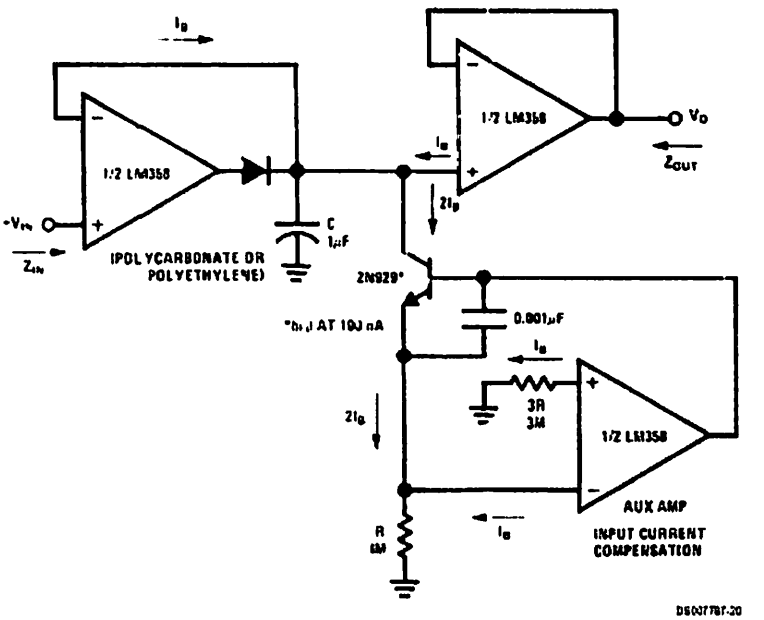
DS007787-18

Pulse Generator



DS007787-19

Low Drift Peak Detector

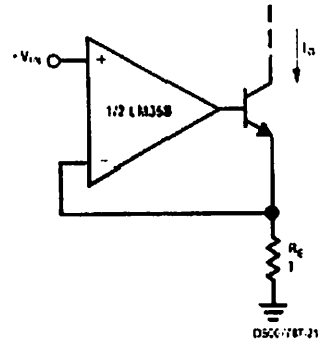


DS007787-20

HIGH Z_{IN}
LOW Z_{OUT}

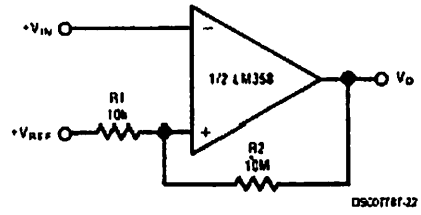
Typical Single-Supply Applications ($V^+ = 5.0\ V_{DC}$) (Continued)

High Compliance Current Sink

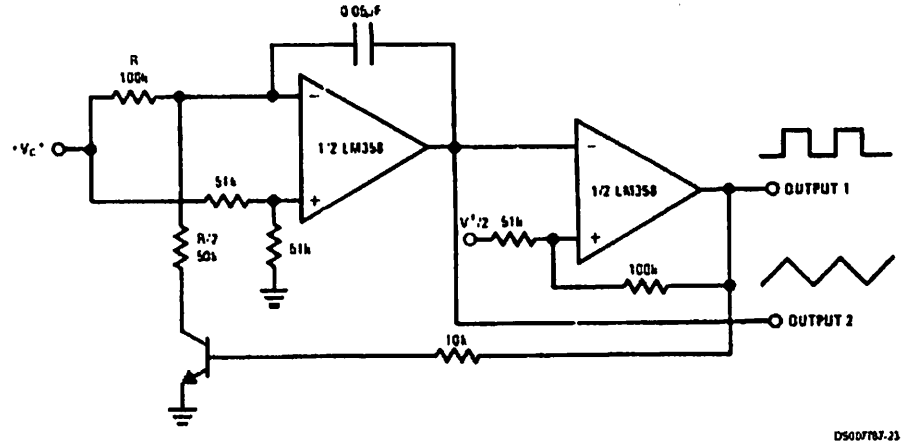


I_O = 1 amp/volt V_{IN}
(Increase R_E for I_O small)

Comparator with Hysteresis



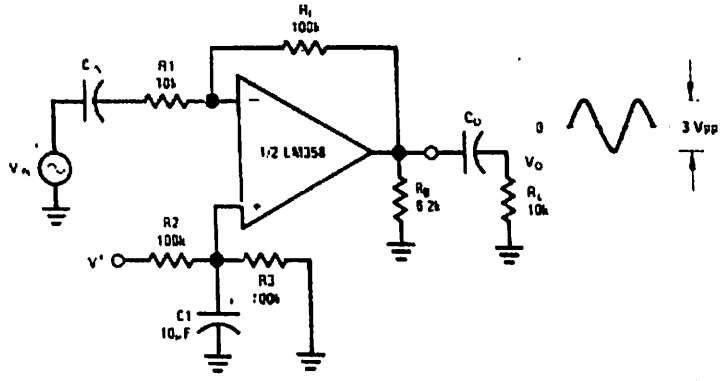
Voltage Controlled Oscillator (VCO)



*WIDE CONTROL VOLTAGE RANGE: $0\ V_{DC} \leq V_C \leq 2\ (V^+ - 1.5V_{DC})$

Typical Single-Supply Applications (V^+ = 5.0 V_{DC}) (Continued)

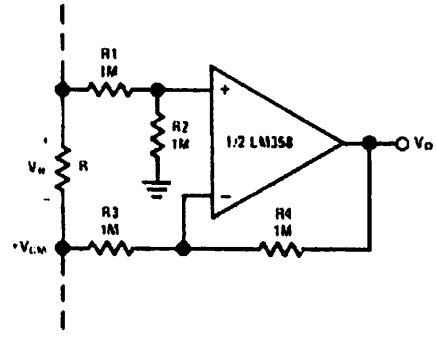
AC Coupled Inverting Amplifier



DS007787-24

$$A_V = -\frac{R_f}{R1} \quad \text{(As shown } A_V = -10\text{)}$$

Ground Referencing a Differential Input Signal



DS007787-25

National Semiconductor

December 1994

ADC0801/ADC0802/ADC0803/ADC0804/ADC0805 8-Bit μP Compatible A/D Converters

General Description

The ADC0801, ADC0802, ADC0803, ADC0804 and ADC0805 are CMOS 8-bit successive approximation A/D converters that use a differential potentiometric ladder—similar to the 256R products. These converters are designed to allow operation with the NSC800 and INS8080A derivative control bus with TRI-STATE® output latches directly driving the data bus. These A/Ds appear like memory locations or I/O ports to the microprocessor and no interfacing logic is needed.

Differential analog voltage inputs allow increasing the common-mode rejection and offsetting the analog zero input voltage value. In addition, the voltage reference input can be adjusted to allow encoding any smaller analog voltage span to the full 8 bits of resolution.

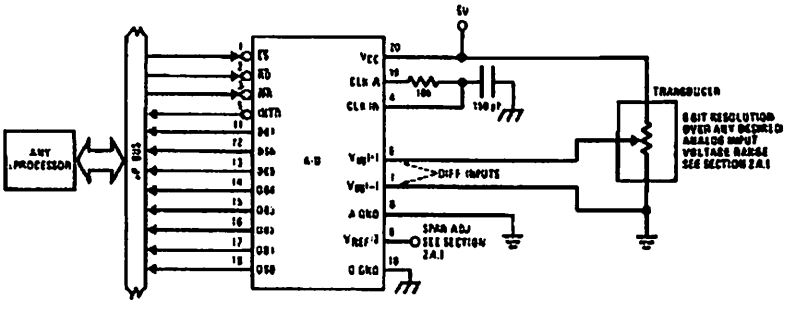
Features

- Compatible with 8080 μP derivatives—no interfacing logic needed - access time - 135 ns
- Easy interface to all microprocessors, or operates "stand alone"
- Differential analog voltage inputs
- Logic inputs and outputs meet both MOS and TTL voltage level specifications
- Works with 2.5V (LM336) voltage reference
- On-chip clock generator
- 0V to 5V analog input voltage range with single 5V supply
- No zero adjust required
- 0.3" standard width 20-pin DIP package
- 20-pin molded chip carrier or small outline package
- Operates ratiometrically or with 5 V_{DC}, 2.5 V_{DC}, or analog span adjusted voltage reference

Key Specifications

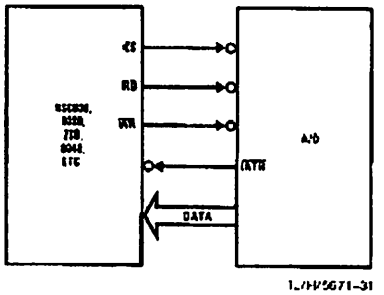
- Resolution — 8 bits
- Total error — ±¼ LSB, ±½ LSB and ±1 LSB
- Conversion time — 100 μs

Typical Applications



TL/H/5671–1

8080 Interface



TL/H/5671–31

Error Specification (Includes Full-Scale, Zero Error, and Non-Linearity)			
Part Number	Full-Scale Adjusted	$V_{REF}/2 = 2.500\ V_{DC}$ (No Adjustments)	$V_{REF}/2$ = No Connection (No Adjustments)
ADC0801	±¼ LSB		
ADC0802		±½ LSB	
ADC0803	±½ LSB		
ADC0804		±1 LSB	
ADC0805			±1 LSB

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Z-80® is a registered trademark of Zilog Corp.

Absolute Maximum Ratings (Notes 1 & 2)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage (V_{CC}) (Note 3)	6.5V
Voltage	
Logic Control Inputs	0.3V to +18V
At Other Input and Outputs	0.3V to (V_{CC} + 0.3V)
Lead Temp. (Soldering, 10 seconds)	
Dual-In-Line Package (plastic)	260°C
Dual-In-Line Package (ceramic)	300°C
Surface Mount Package	
Vapor Phase (60 seconds)	215°C
Infrared (15 seconds)	220°C
Storage Temperature Range	−65°C to +150°C
Package Dissipation at T_A = 25°C	875 mW
ESD Susceptibility (Note 10)	800V

Operating Ratings (Notes 1 & 2)

Temperature Range	$T_{MIN} \le T_A \le T_{MAX}$
ADC0801/02LJ, ADC0802LJ/883	−55°C ≤ T_A ≤ +125°C
ADC0801/02/03/04LCJ	−40°C ≤ T_A ≤ +85°C
ADC0801/02/03/05LCN	−40°C ≤ T_A ≤ +85°C
ADC0804LCN	0°C ≤ T_A ≤ +70°C
ADC0802/03/04LCV	0°C ≤ T_A ≤ +70°C
ADC0802/03/04LCWM	0°C ≤ T_A ≤ +70°C
Range of V_{CC}	4.5 V_{DC} to 6.3 V_{DC}

Electrical Characteristics

The following specifications apply for V_{CC} = 5 V_{DC}, $T_{MIN} \le T_A \le T_{MAX}$ and f_{CLK} = 640 kHz unless otherwise specified.

Parameter	Conditions	Min	Typ	Max	Units
ADC0801: Total Adjusted Error (Note 8)	With Full-Scale Adj. (See Section 2.5.2)			±¼	LSB
ADC0802: Total Unadjusted Error (Note 8)	$V_{REF}/2$ = 2.500 V_{DC}			±½	LSB
ADC0803: Total Adjusted Error (Note 8)	With Full-Scale Adj. (See Section 2.5.2)			±½	LSB
ADC0804: Total Unadjusted Error (Note 8)	$V_{REF}/2$ = 2.500 V_{DC}			±1	LSB
ADC0805: Total Unadjusted Error (Note 8)	$V_{REF}/2$-No Connection			±1	LSB
$V_{REF}/2$ Input Resistance (Pin 9)	ADC0801/02/03/05 ADC0804 (Note 9)	2.5 0.75	8.0 1.1		kΩ kΩ
Analog Input Voltage Range	(Note 4) V(+) or V(−)	Gnd−0.05		V_{CC} + 0.05	V_{DC}
DC Common-Mode Error	Over Analog Input Voltage Range		±1/16	±⅛	LSB
Power Supply Sensitivity	V_{CC} = 5 V_{DC} ± 10% Over Allowed V_{IN}(+) and V_{IN}(−) Voltage Range (Note 4)		±1/16	±⅛	LSB

AC Electrical Characteristics

The following specifications apply for V_{CC} = 5 V_{DC} and T_A = 25°C unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Units
T_C	Conversion Time	f_{CLK} = 640 kHz (Note 6)	103		114	μs
T_C	Conversion Time	(Note 5, 6)	66		73	$1/f_{CLK}$
f_{CLK}	Clock Frequency Clock Duty Cycle	V_{CC} = 5V, (Note 5) (Note 5)	100 40	640	1460 60	kHz %
CR	Conversion Rate in Free-Running Mode	$\overline{INTR}$ tied to $\overline{WR}$ with $\overline{CS}$ = 0 V_{DC}, f_{CLK} = 640 kHz	8770		9708	conv/s
$t_{W(\overline{WR})L}$	Width of $\overline{WR}$ Input (Start Pulse Width)	$\overline{CS}$ = 0 V_{DC} (Note 7)	100			ns
t_{ACC}	Access Time (Delay from Falling Edge of $\overline{RD}$ to Output Data Valid)	C_L = 100 pF		135	200	ns
t_{1H}, t_{0H}	TRI-STATE Control (Delay from Rising Edge of $\overline{RD}$ to Hi-Z State)	C_L = 10 pF, R_L = 10k (See TRI-STATE Test Circuits)		125	200	ns
t_{WI}, t_{RI}	Delay from Falling Edge of $\overline{WR}$ or $\overline{RD}$ to Reset of $\overline{INTR}$			300	450	ns
C_{IN}	Input Capacitance of Logic Control Inputs			5	7.5	pF
C_{OUT}	TRI-STATE Output Capacitance (Data Buffers)			5	7.5	pF
CONTROL INPUTS [Note: CLK IN (Pin 4) is the input of a Schmitt trigger circuit and is therefore specified separately]						
V_{IN}(1)	Logical "1" Input Voltage (Except Pin 4 CLK IN)	V_{CC} = 5.25 V_{DC}	2.0		15	V_{DC}

AC Electrical Characteristics (Continued)

The following specifications apply for $V_{CC} = 5V_{DC}$ and $T_{MIN} \leq T_A \leq T_{MAX}$, unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Units
CONTROL INPUTS [Note: CLK IN (Pin 4) is the input of a Schmitt trigger circuit and is therefore specified separately]						
$V_{IN}(0)$	Logical "0" Input Voltage (Except Pin 4 CLK IN)	$V_{CC} = 4.75\ V_{DC}$			0.8	V_{DC}
$I_{IN}(1)$	Logical "1" Input Current (All Inputs)	$V_{IN} = 5\ V_{DC}$		0.005	1	μA_{DC}
$I_{IN}(0)$	Logical "0" Input Current (All Inputs)	$V_{IN} = 0\ V_{DC}$	-1	-0.005		μA_{DC}
CLOCK IN AND CLOCK R						
V_T+	CLK IN (Pin 4) Positive Going Threshold Voltage		2.7	3.1	3.5	V_{DC}
V_T-	CLK IN (Pin 4) Negative Going Threshold Voltage		1.5	1.8	2.1	V_{DC}
V_H	CLK IN (Pin 4) Hysteresis $(V_T+) - (V_T-)$		0.6	1.3	2.0	V_{DC}
$V_{OUT}(0)$	Logical "0" CLK R Output Voltage	$I_O = 360\ \mu A$ $V_{CC} = 4.75\ V_{DC}$			0.4	V_{DC}
$V_{OUT}(1)$	Logical "1" CLK R Output Voltage	$I_O = -360\ \mu A$ $V_{CC} = 4.75\ V_{DC}$	2.4			V_{DC}
DATA OUTPUTS AND $\overline{INTR}$						
$V_{OUT}(0)$	Logical "0" Output Voltage Data Outputs $\overline{INTR}$ Output	 $I_{OUT} = 1.6\ mA$, $V_{CC} = 4.75\ V_{DC}$ $I_{OUT} = 1.0\ mA$, $V_{CC} = 4.75\ V_{DC}$			 0.4 0.4	 V_{DC} V_{DC}
$V_{OUT}(1)$	Logical "1" Output Voltage	$I_O = -360\ \mu A$, $V_{CC} = 4.75\ V_{DC}$	2.4			V_{DC}
$V_{OUT}(1)$	Logical "1" Output Voltage	$I_O = -10\ \mu A$, $V_{CC} = 4.75\ V_{DC}$	4.5			V_{DC}
I_{OUT}	TRI-STATE Disabled Output Leakage (All Data Buffers)	$V_{OUT} = 0\ V_{DC}$ $V_{OUT} = 5\ V_{DC}$	-3		 3	μA_{DC} μA_{DC}
I_{SOURCE}		V_{OUT} Short to Gnd, $T_A = 25°C$	4.5	6		mA_{DC}
I_{SINK}		V_{OUT} Short to V_{CC}, $T_A = 25°C$	9.0	16		mA_{DC}
POWER SUPPLY						
I_{CC}	Supply Current (Includes Ladder Current) ADC0801/02/03/04LCJ/05 ADC0804LCN/LCV/LCWM	$f_{CLK} = 640\ kHz$, $V_{REF}/2 = NC$, $T_A = 25°C$ and $\overline{CS} = 5V$		 1.1 1.9	 1.8 2.5	 mA mA

Note 1: Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. DC and AC electrical specifications do not apply when operating the device beyond its specified operating conditions.

Note 2: All voltages are measured with respect to Gnd, unless otherwise specified. The separate A Gnd point should always be wired to the D Gnd.

Note 3: A zener diode exists, internally, from V_{CC} to Gnd and has a typical breakdown voltage of 7 V_{DC}.

Note 4: For $V_{IN}(-) \geq V_{IN}(+)$ the digital output code will be 0000 0000. Two on-chip diodes are tied to each analog input (see block diagram) which will forward conduct for analog input voltages one diode drop below ground or one diode drop greater than the V_{CC} supply. Be careful, during testing at low V_{CC} levels (4.5V), as high level analog inputs (5V) can cause the input diode to conduct—especially at elevated temperatures, and cause errors for analog inputs near full-scale. The spec allows 50 mV forward bias of either diode. This means that as long as the analog V_{IN} does not exceed the supply voltage by more than 50 mV, the output code will be correct. To achieve an absolute 0 V_{DC} to 5 V_{DC} input voltage range will therefore require a minimum supply voltage of 4.950 V_{DC} over temperature variations, initial tolerance and loading.

Note 5: Accuracy is guaranteed at $f_{CLK} = 640\ kHz$. At higher clock frequencies accuracy can degrade. For lower clock frequencies, the duty cycle limits can be extended so long as the minimum clock high time interval or minimum clock low time interval is no less than 275 ns.

Note 6: With an asynchronous start pulse, up to 8 clock periods may be required before the internal clock phases are proper to start the conversion process. The start request is internally latched, see *Figure 2* and section 2.0.

Note 7: The $\overline{CS}$ input is assumed to bracket the $\overline{WR}$ strobe input and therefore timing is dependent on the $\overline{WR}$ pulse width. An arbitrarily wide pulse width will hold the converter in a reset mode and the start of conversion is initiated by the low to high transition of the $\overline{WR}$ pulse (see timing diagrams).

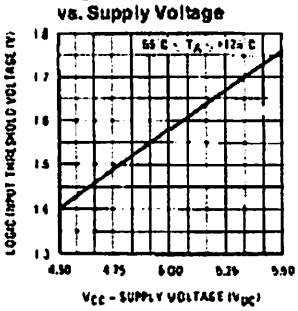
Note 8: None of these A/Ds requires a zero adjust (see section 2.5.1). To obtain zero code at other analog input voltages see section 2.5 and *Figure 5*.

Note 9: The $V_{REF}/2$ pin is the center point of a two resistor divider connected from V_{CC} to ground. In all versions of the ADC0801, ADC0802, ADC0803, and ADC0805, and in the ADC0804LCJ, each resistor is typically 16 kΩ. In all versions of the ADC0804 except the ADC0804LCJ, each resistor is typically 2.2 kΩ.

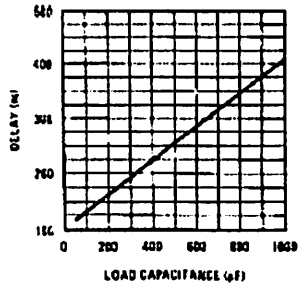
Note 10: Human body model, 100 pF discharged through a 1.5 kΩ resistor.

Typical Performance Characteristics

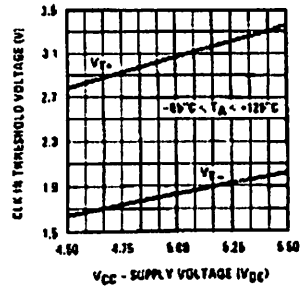
Logic Input Threshold Voltage vs. Supply Voltage



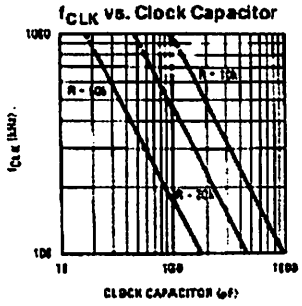
Delay From Falling Edge of $\overline{RD}$ to Output Data Valid vs. Load Capacitance



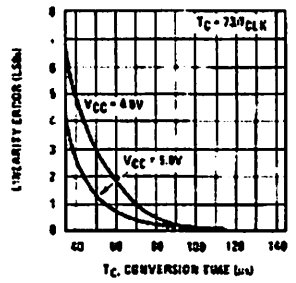
CLK IN Schmitt Trip Levels vs. Supply Voltage



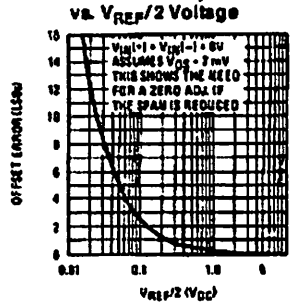
f_{CLK} vs. Clock Capacitor



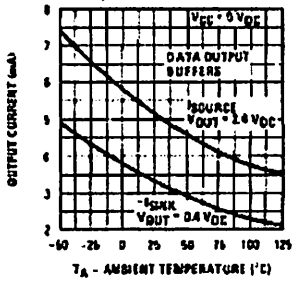
Full-Scale Error vs Conversion Time



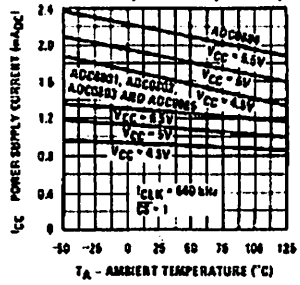
Effect of Unadjusted Offset Error vs. $V_{REF}/2$ Voltage



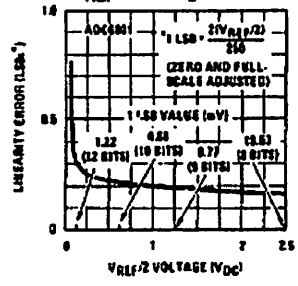
Output Current vs Temperature



Power Supply Current vs Temperature (Note 9)



Linearity Error at Low $V_{REF}/2$ Voltages



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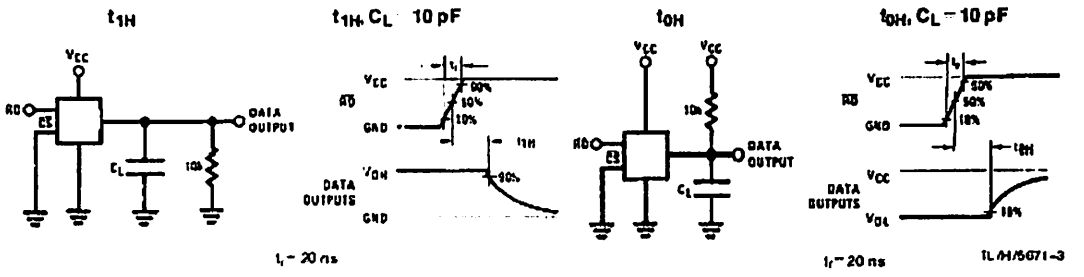
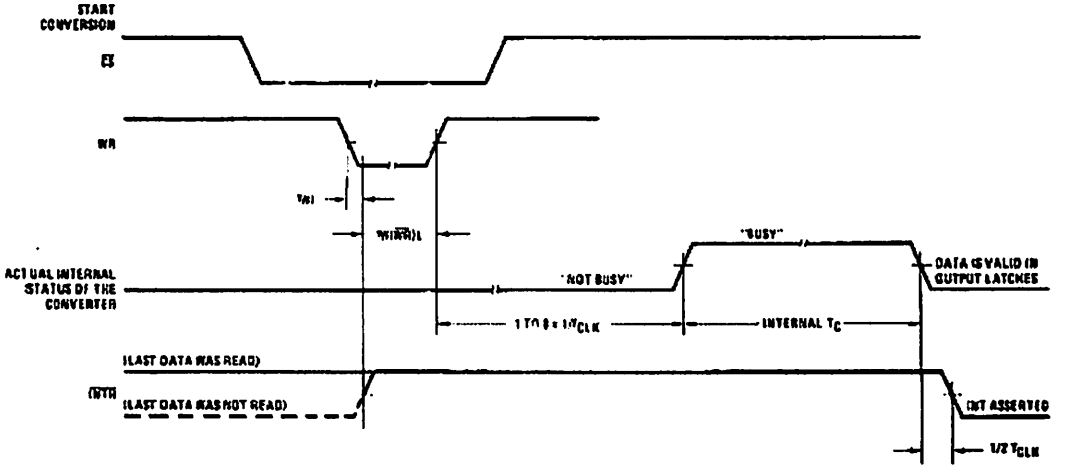
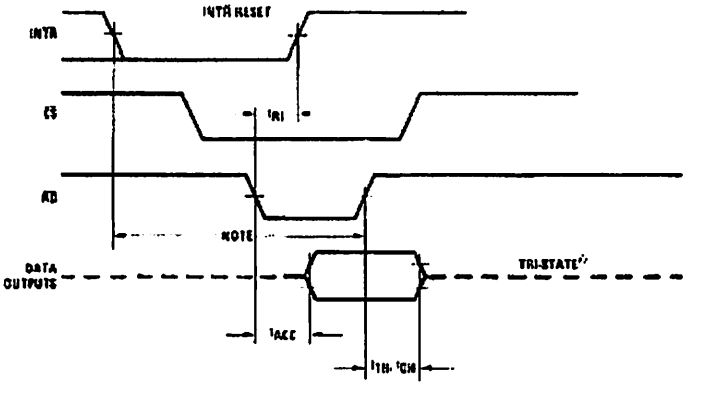
TRI-STATE Test Circuits and Waveforms



Timing Diagrams (All timing is measured from the 50% voltage points)



Output Enable and Reset $\overline{INTR}$



Note: Read strobe must occur 8 clock periods ($8/f_{C\_K}$) after assertion of interrupt to guarantee reset of $\overline{INTR}$.

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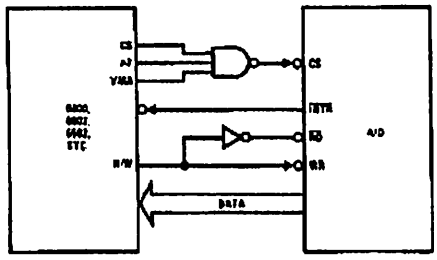
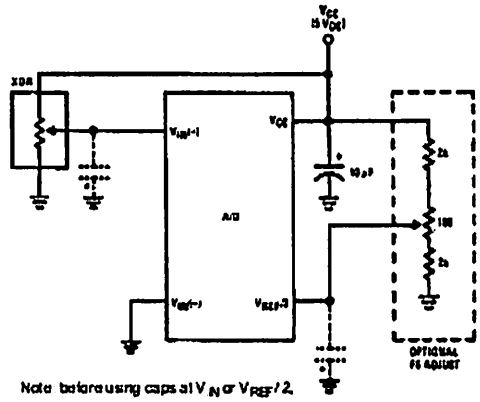
Typical Applications (Continued)

6800 Interface

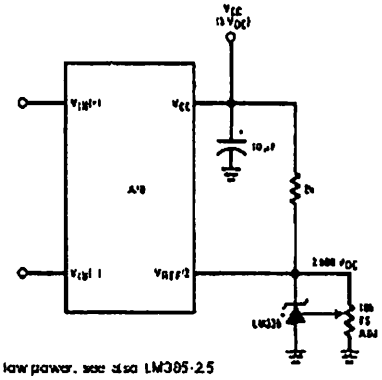


Ratiometric with Full-Scale Adjust



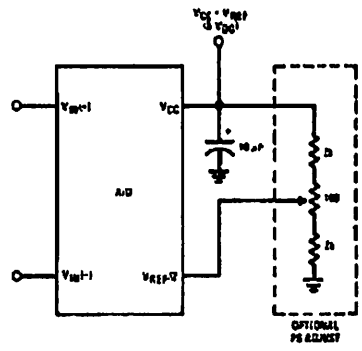
Note: before using caps at V_{IN} or $V_{REF}/2$, see section 2.0 2 Input Bypass Capacitors.

Absolute with a 2.500V Reference

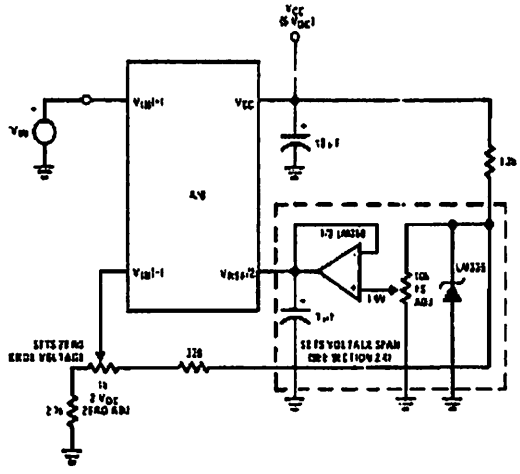


*For low power, see also LM385-2.5

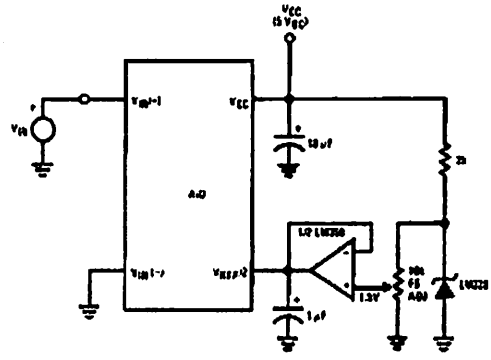
Absolute with a 5V Reference



Zero-Shift and Span Adjust: 2V ≤ V_{IN} ≤ 5V



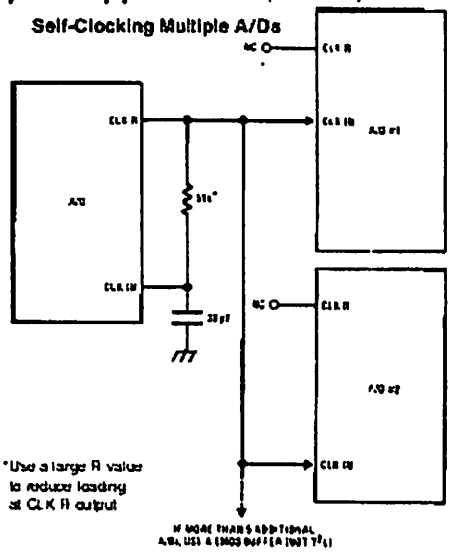
Span Adjust: 0V ≤ V_{IN} ≤ 3V



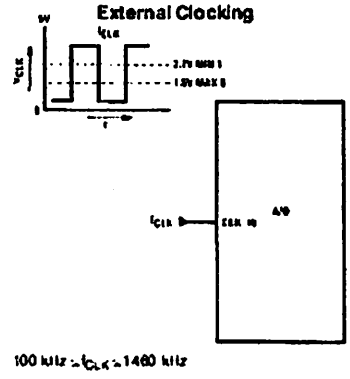
TL/H/5071-5

Typical Applications (Continued)

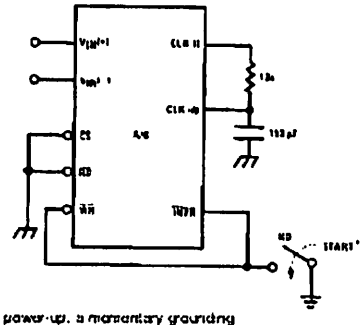
Self-Clocking Multiple A/Ds



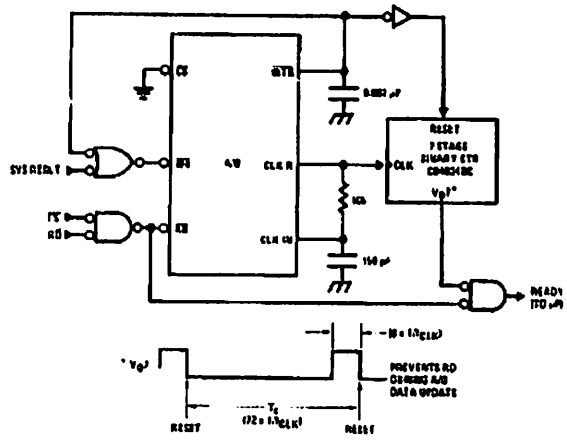
External Clocking



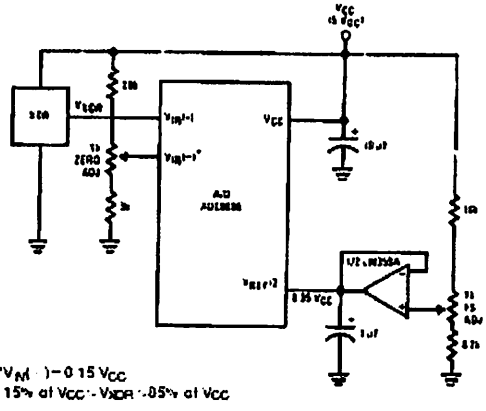
Self-Clocking in Free-Running Mode



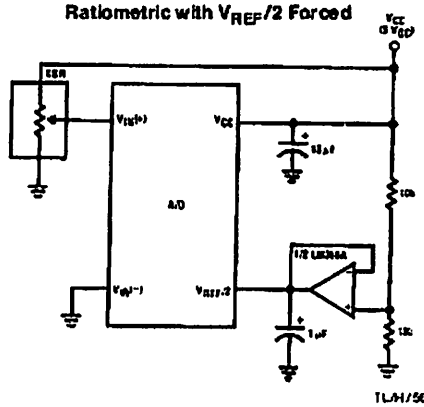
µP Interface for Free-Running A/D



Operating with "Automotive" Ratiometric Transducers



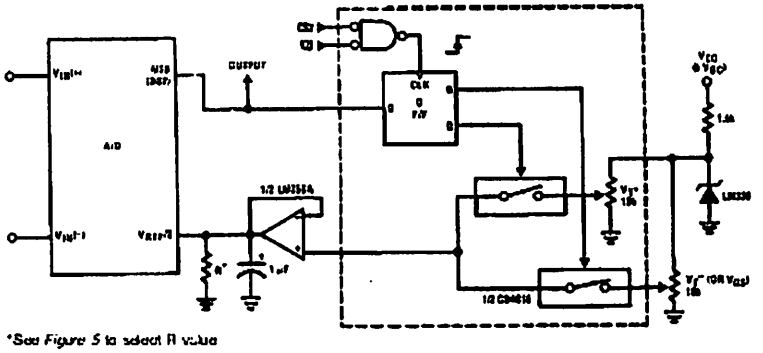
Ratiometric with $V_{REF}/2$ Forced



TL/H/5671-7

Typical Applications (Continued)

µP Compatible Differential-Input Comparator with Pre-Set V_{OS} (with or without Hysteresis)

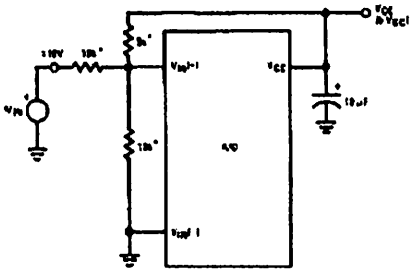


*See *Figure 5* to select R value

DB7 = "1" for $V_{IN}(+) > V_{IN}(-) + (V_{REF}/2)$

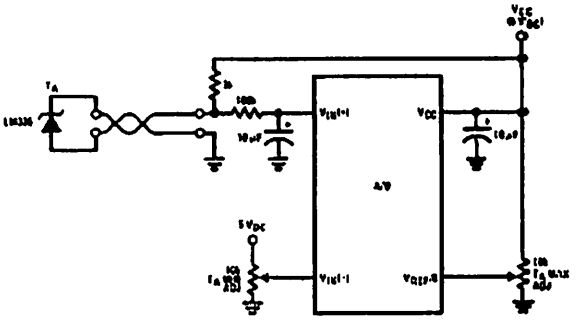
Omit circuitry within the dotted area if hysteresis is not needed

Handling ± 10V Analog Inputs

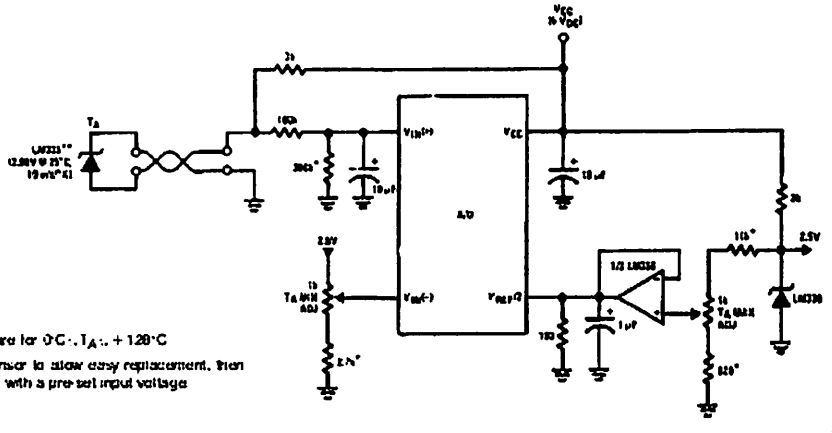


*Beckman Instruments #694-3-R10K resistor array

Low-Cost, µP Interfaced, Temperature-to-Digital Converter



µP Interfaced Temperature-to-Digital Converter



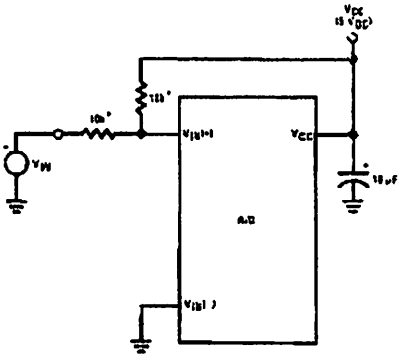
*Circuit values shown are for 0°C ≤ T_A ≤ +128°C

**Can calibrate each sensor to allow easy replacement, then A/D can be calibrated with a pre-set input voltage

TL/H/5671–8

Typical Applications (Continued)

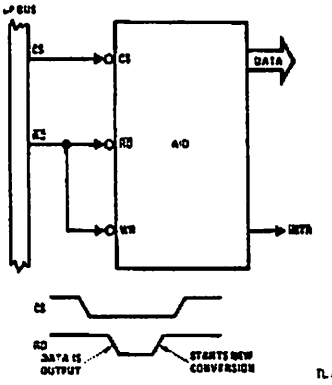
Handling ± 5V Analog Inputs



TL/H/5671–33

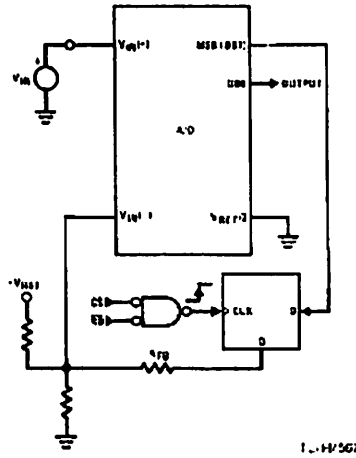
*Beckman Instruments # 694-3-R10K resistor array

Read-Only Interface



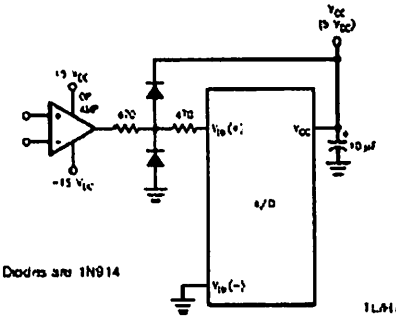
TL/H/5671–34

µP Interfaced Comparator with Hysteresis



TL/H/5671–35

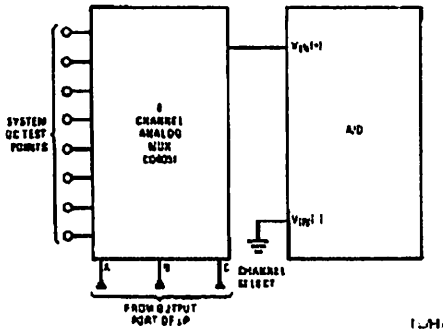
Protecting the Input



Diodes are 1N914

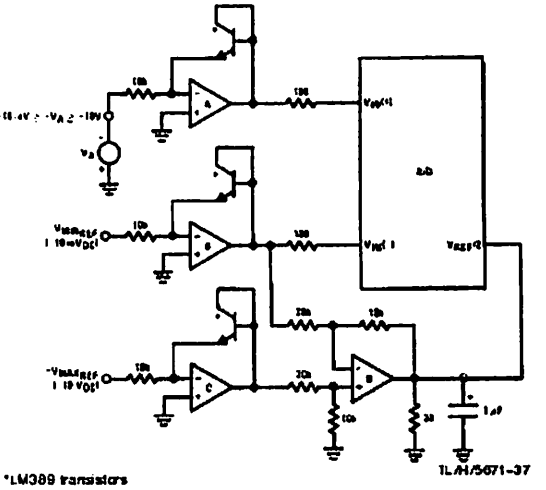
TL/H/5671–9

Analog Self-Test for a System



TL/H/5671–36

A Low-Cost, 3-Decade Logarithmic Converter



*LM389 transistors

A, B, C, D = LM324A quad op amp

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Functional Description (Continued)

After the "1" is clocked through the 8-bit shift register (which completes the SAR search) it appears as the input to the D-type latch, LATCH 1. As soon as this "1" is output from the shift register, the AND gate, G2, causes the new digital word to transfer to the TRI-STATE output latches. When LATCH 1 is subsequently enabled, the Q output makes a high-to-low transition which causes the INTR F/F to set. An inverting buffer then supplies the $\overline{INTR}$ input signal.

Note that this $\overline{SET}$ control of the INTR F/F remains low for 8 of the external clock periods (as the internal clocks run at 1/8 of the frequency of the external clock). If the data output is continuously enabled ($\overline{CS}$ and $\overline{RD}$ both held low), the $\overline{INTR}$ output will still signal the end of conversion (by a high-to-low transition), because the $\overline{SET}$ input can control the Q output of the INTR F/F even though the RESET input is constantly at a "1" level in this operating mode. This $\overline{INTR}$ output will therefore stay low for the duration of the $\overline{SET}$ signal, which is 8 periods of the external clock frequency (assuming the A/D is not started during this interval).

When operating in the free-running or continuous conversion mode ($\overline{INTR}$ pin tied to $\overline{WR}$ and $\overline{CS}$ wired low—see also section 2.8), the START F/F is SET by the high-to-low transition of the $\overline{INTR}$ signal. This resets the SHIFT REGISTER which causes the input to the D-type latch, LATCH 1, to go low. As the latch enable input is still present, the $\overline{Q}$ output will go high, which then allows the INTR F/F to be RESET. This reduces the width of the resulting $\overline{INTR}$ output pulse to only a few propagation delays (approximately 300 ns).

When data is to be read, the combination of both $\overline{CS}$ and $\overline{RD}$ being low will cause the INTR F/F to be reset and the TRI-STATE output latches will be enabled to provide the 8-bit digital outputs.

2.1 Digital Control Inputs

The digital control inputs ($\overline{CS}$, $\overline{RD}$, and $\overline{WR}$) meet standard T²L logic voltage levels. These signals have been renamed when compared to the standard A/D Start and Output Enable labels. In addition, these inputs are active low to allow an easy interface to microprocessor control busses. For non-microprocessor based applications, the $\overline{CS}$ input (pin 1) can be grounded and the standard A/D Start function is obtained by an active low pulse applied at the $\overline{WR}$ input (pin 3) and the Output Enable function is caused by an active low pulse at the $\overline{RD}$ input (pin 2).

2.2 Analog Differential Voltage Inputs and Common-Mode Rejection

This A/D has additional applications flexibility due to the analog differential voltage input. The $V_{IN}(-)$ input (pin 7) can be used to automatically subtract a fixed voltage value from the input reading (tare correction). This is also useful in 4 mA–20 mA current loop conversion. In addition, common-mode noise can be reduced by use of the differential input.

The time interval between sampling $V_{IN}(+)$ and $V_{IN}(-)$ is 4-½ clock periods. The maximum error voltage due to this slight time difference between the input voltage samples is given by:

$$\Delta V_e(MAX) = (V_P)(2\pi f_{cm})\left(\frac{4.5}{f_{CLK}}\right),$$

where:

ΔV_e is the error voltage due to sampling delay

V_P is the peak value of the common-mode voltage

f_{cm} is the common-mode frequency

As an example, to keep this error to ¼ LSB (~5 mV) when operating with a 60 Hz common-mode frequency, f_{cm}, and using a 640 kHz A/D clock, f_{CLK}, would allow a peak value of the common-mode voltage, V_P, which is given by:

$$V_P = \frac{[\Delta V_{e(MAX)}(f_{CLK})]}{(2\pi f_{cm})(4.5)}$$

or

$$V_P = \frac{(5 \times 10^{-3})(640 \times 10^3)}{(6.28)(60)(4.5)}$$

which gives

$V_P \simeq 1.9V$.

The allowed range of analog input voltages usually places more severe restrictions on input common-mode noise levels.

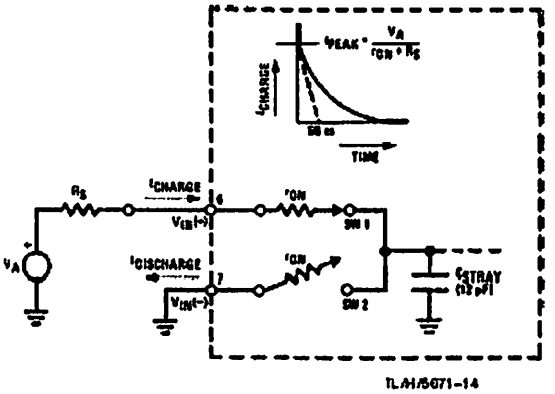
An analog input voltage with a reduced span and a relatively large zero offset can be handled easily by making use of the differential input (see section 2.4 Reference Voltage).

2.3 Analog Inputs

2.3.1 Input Current

Normal Mode

Due to the internal switching action, displacement currents will flow at the analog inputs. This is due to on-chip stray capacitance to ground as shown in *Figure 3*.



r_{ON} of SW 1 and SW 2 = 5 kΩ

$\tau = r_{ON} C_{STRAY} = 5\ k\Omega \times 12\ pF = 60\ ns$

FIGURE 3. Analog Input Impedance

Functional Description (Continued)

The voltage on this capacitance is switched and will result in currents entering the $V_{IN}(+)$ input pin and leaving the $V_{IN}(-)$ input which will depend on the analog differential input voltage levels. These current transients occur at the leading edge of the internal clocks. They rapidly decay and *do not cause errors* as the on-chip comparator is strobed at the end of the clock period.

Fault Mode

If the voltage source applied to the $V_{IN}(+)$ or $V_{IN}(-)$ pin exceeds the allowed operating range of $V_{CC}+50$ mV, large input currents can flow through a parasitic diode to the V_{CC} pin. If these currents can exceed the 1 mA max allowed spec, an external diode (1N914) should be added to bypass this current to the V_{CC} pin (with the current bypassed with this diode, the voltage at the $V_{IN}(+)$ pin can exceed the V_{CC} voltage by the forward voltage of this diode).

2.3.2 Input Bypass Capacitors

Bypass capacitors at the inputs will average these charges and cause a DC current to flow through the output resistances of the analog signal sources. This charge pumping action is worse for continuous conversions with the $V_{IN}(+)$ input voltage at full-scale. For continuous conversions with a 640 kHz clock frequency with the $V_{IN}(+)$ input at 5V, this DC current is at a maximum of approximately 5 μA. Therefore, *bypass capacitors should not be used at the analog inputs or the $V_{REF}/2$ pin* for high resistance sources (> 1 kΩ). If input bypass capacitors are necessary for noise filtering and high source resistance is desirable to minimize capacitor size, the detrimental effects of the voltage drop across this input resistance, which is due to the average value of the input current, can be eliminated with a full-scale adjustment while the given source resistor and input bypass capacitor are both in place. This is possible because the average value of the input current is a precise linear function of the differential input voltage.

2.3.3 Input Source Resistance

Large values of source resistance where an input bypass capacitor is not used, *will not cause errors* as the input currents settle out prior to the comparison time. If a low pass filter is required in the system, use a low valued series resistor (≤ 1 kΩ) for a passive RC section or add an op amp RC active low pass filter. For low source resistance applications, (≤ 1 kΩ), a 0.1 μF bypass capacitor at the inputs will prevent noise pickup due to series lead inductance of a long wire. A 100Ω series resistor can be used to isolate this capacitor—both the R and C are placed outside the feedback loop—from the output of an op amp, if used.

2.3.4 Noise

The leads to the analog inputs (pin 6 and 7) should be kept as short as possible to minimize input noise coupling. Both noise and undesired digital clock coupling to these inputs can cause system errors. The source resistance for these inputs should, in general, be kept below 5 kΩ. Larger values of source resistance can cause undesired system noise pickup. Input bypass capacitors, placed from the analog inputs to ground, will eliminate system noise pickup but can create analog scale errors as these capacitors will average the transient input switching currents of the A/D (see section 2.3.1.). This scale error depends on both a large source resistance and the use of an input bypass capacitor. This error can be eliminated by doing a full-scale adjustment of the A/D (adjust $V_{REF}/2$ for a proper full-scale reading—see section 2.5.2 on Full-Scale Adjustment) with the source resistance and input bypass capacitor in place.

2.4 Reference Voltage

2.4.1 Span Adjust

For maximum applications flexibility, these A/Ds have been designed to accommodate a 5 V_{DC}, 2.5 V_{DC} or an adjusted voltage reference. This has been achieved in the design of the IC as shown in *Figure 4*.

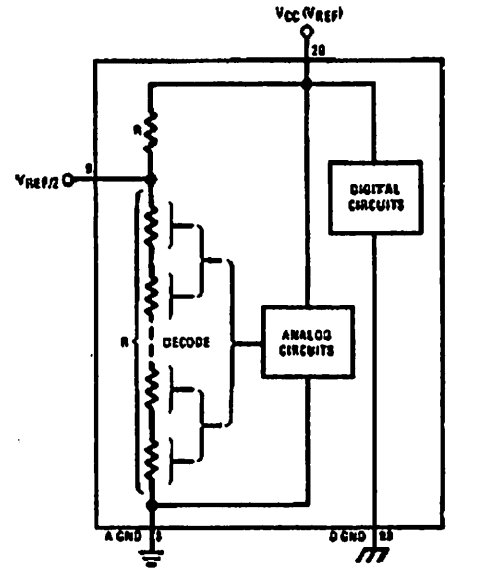


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FIGURE 4. The $V_{REFERENCE}$ Design on the IC

Notice that the reference voltage for the IC is either ½ of the voltage applied to the V_{CC} supply pin, or is equal to the voltage that is externally forced at the $V_{REF}/2$ pin. This allows for a ratiometric voltage reference using the V_{CC} supply, a 5 V_{DC} reference voltage can be used for the V_{CC} supply or a voltage less than 2.5 V_{DC} can be applied to the $V_{REF}/2$ input for increased application flexibility. The internal gain to the $V_{REF}/2$ input is 2, making the full-scale differential input voltage twice the voltage at pin 9.

An example of the use of an adjusted reference voltage is to accommodate a reduced span—or dynamic voltage range of the analog input voltage. If the analog input voltage were to range from 0.5 V_{DC} to 3.5 V_{DC}, instead of 0V to 5 V_{DC}, the span would be 3V as shown in *Figure 5*. With 0.5 V_{DC} applied to the $V_{IN}(-)$ pin to absorb the offset, the reference voltage can be made equal to ½ of the 3V span or 1.5 V_{DC}. The A/D now will encode the $V_{IN}(+)$ signal from 0.5V to 3.5 V with the 0.5V input corresponding to zero and the 3.5 V_{DC} input corresponding to full-scale. The full 8 bits of resolution are therefore applied over this reduced analog input voltage range.

Functional Description (Continued)

2.5.3 Adjusting for an Arbitrary Analog Input Voltage Range

If the analog zero voltage of the A/D is shifted away from ground (for example, to accommodate an analog input signal that does not go to ground) this new zero reference should be properly adjusted first. A $V_{IN}(+)$ voltage that equals this desired zero reference plus ½ LSB (where the LSB is calculated for the desired analog span, 1 LSB = analog span/256) is applied to pin 6 and the zero reference voltage at pin 7 should then be adjusted to just obtain the 00_{HEX} to 01_{HEX} code transition.

The full-scale adjustment should then be made (with the proper $V_{IN}(-)$ voltage applied) by forcing a voltage to the $V_{IN}(+)$ input which is given by:

$$V_{IN}(+)\text{fs adj} = V_{MAX} - 1.5\left[\frac{(V_{MAX} - V_{MIN})}{256}\right]$$

where:

V_{MAX} = The high end of the analog input range

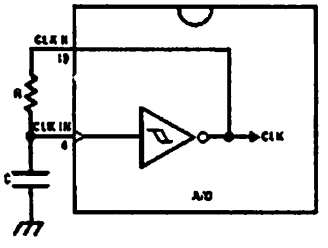
and

V_{MIN} = the low end (the offset zero) of the analog range. (Both are ground referenced.)

The $V_{REF}/2$ (or V_{CC}) voltage is then adjusted to provide a code change from FE_{HEX} to FF_{HEX}. This completes the adjustment procedure.

2.6 Clocking Option

The clock for the A/D can be derived from the CPU clock or an external RC can be added to provide self-clocking. The CLK IN (pin 4) makes use of a Schmitt trigger as shown in *Figure 6*.



$$f_{CLK} \simeq \frac{1}{1.1\,RC}$$

$$R \simeq 10\ k\Omega$$

1-01/5071-17

FIGURE 6. Self-Clocking the A/D

Heavy capacitive or DC loading of the clock R pin should be avoided as this will disturb normal converter operation. Loads less than 50 pF, such as driving up to 7 A/D converter clock inputs from a single clock R pin of 1 converter, are allowed. For larger clock line loading, a CMOS or low power TTL buffer or PNP input logic should be used to minimize the loading on the clock R pin (do not use a standard TTL buffer).

2.7 Restart During a Conversion

If the A/D is restarted ($\overline{CS}$ and $\overline{WR}$ go low and return high) during a conversion, the converter is reset and a new conversion is started. The output data latch is not updated if the conversion in process is not allowed to be completed, therefore the data of the previous conversion remains in this latch. The $\overline{INTR}$ output simply remains at the "1" level.

2.8 Continuous Conversions

For operation in the free-running mode an initializing pulse should be used, following power-up, to ensure circuit operation. In this application, the $\overline{CS}$ input is grounded and the $\overline{WR}$ input is tied to the $\overline{INTR}$ output. This $\overline{WR}$ and $\overline{INTR}$ node should be momentarily forced to logic low following a power-up cycle to guarantee operation.

2.9 Driving the Data Bus

This MOS A/D, like MOS microprocessors and memories, will require a bus driver when the total capacitance of the data bus gets large. Other circuitry, which is tied to the data bus, will add to the total capacitive loading, even in TRI-STATE (high impedance mode). Backplane bussing also greatly adds to the stray capacitance of the data bus.

There are some alternatives available to the designer to handle this problem. Basically, the capacitive loading of the data bus slows down the response time, even though DC specifications are still met. For systems operating with a relatively slow CPU clock frequency, more time is available in which to establish proper logic levels on the bus and therefore higher capacitive loads can be driven (see typical characteristics curves).

At higher CPU clock frequencies time can be extended for I/O reads (and/or writes) by inserting wait states (8080) or using clock extending circuits (6800).

Finally, if time is short and capacitive loading is high, external bus drivers must be used. These can be TRI-STATE buffers (low power Schottky such as the DM74LS240 series is recommended) or special higher drive current products which are designed as bus drivers. High current bipolar bus drivers with PNP inputs are recommended.

2.10 Power Supplies

Noise spikes on the V_{CC} supply line can cause conversion errors as the comparator will respond to this noise. A low inductance tantalum filter capacitor should be used close to the converter V_{CC} pin and values of 1 μF or greater are recommended. If an unregulated voltage is available in the system, a separate LM340LAZ-5.0, TO-92, 5V voltage regulator for the converter (and other analog circuitry) will greatly reduce digital noise on the V_{CC} supply.

2.11 Wiring and Hook-Up Precautions

Standard digital wire wrap sockets are not satisfactory for breadboarding this A/D converter. Sockets on PC boards can be used and all logic signal wires and leads should be grouped and kept as far away as possible from the analog signal leads. Exposed leads to the analog inputs can cause undesired digital noise and hum pickup, therefore shielded leads may be necessary in many applications.

Functional Description (Continued)

A single point analog ground that is separate from the logic ground points should be used. The power supply bypass capacitor and the self-clocking capacitor (if used) should both be returned to digital ground. Any $V_{REF}/2$ bypass capacitors, analog input filter capacitors, or input signal shielding should be returned to the analog ground point. A test for proper grounding is to measure the zero error of the A/D converter. Zero errors in excess of ¼ LSB can usually be traced to improper board layout and wiring (see section 2.5.1 for measuring the zero error).

3.0 TESTING THE A/D CONVERTER

There are many degrees of complexity associated with testing an A/D converter. One of the simplest tests is to apply a known analog input voltage to the converter and use LEDs to display the resulting digital output code as shown in *Figure 7*.

For ease of testing, the $V_{REF}/2$ (pin 9) should be supplied with 2.560 V_{DC} and a V_{CC} supply voltage of 5.12 V_{DC} should be used. This provides an LSB value of 20 mV.

If a full-scale adjustment is to be made, an analog input voltage of 5.090 V_{DC} (5.120−1½ LSB) should be applied to the $V_{IN}(+)$ pin with the $V_{IN}(-)$ pin grounded. The value of the $V_{REF}/2$ input voltage should then be adjusted until the digital output code is just changing from 1111 1110 to 1111 1111. This value of $V_{REF}/2$ should then be used for all the tests.

The digital output LED display can be decoded by dividing the 8 bits into 2 hex characters, the 4 most significant (MS) and the 4 least significant (LS). Table I shows the fractional binary equivalent of these two 4-bit groups. By adding the voltages obtained from the "VMS" and "VLS" columns in Table I, the nominal value of the digital display (when $V_{REF}/2$ − 2.560V) can be determined. For example, for an output LED display of 1011 0110 or B6 (in hex), the voltage values from the table are 3.520 + 0.120 or 3.640 V_{DC}. These voltage values represent the center-values of a perfect A/D converter. The effects of quantization error have to be accounted for in the interpretation of the test results.

For a higher speed test system, or to obtain plotted data, a digital-to-analog converter is needed for the test set-up. An accurate 10-bit DAC can serve as the precision voltage source for the A/D. Errors of the A/D under test can be expressed as either analog voltages or differences in 2 digital words.

A basic A/D tester that uses a DAC and provides the error as an analog output voltage is shown in *Figure 8*. The 2 op amps can be eliminated if a lab DVM with a numerical subtraction feature is available to read the difference voltage, "A−C", directly. The analog input voltage can be supplied by a low frequency ramp generator and an X-Y plotter can be used to provide analog error (Y axis) versus analog input (X axis).

For operation with a microprocessor or a computer-based test system, it is more convenient to present the errors digitally. This can be done with the circuit of *Figure 9*, where the output code transitions can be detected as the 10-bit DAC is incremented. This provides ¼ LSB steps for the 8-bit A/D under test. If the results of this test are automatically plotted with the analog input on the X axis and the error (in LSB's) as the Y axis, a useful transfer function of the A/D under test results. For acceptance testing, the plot is not necessary and the testing speed can be increased by establishing internal limits on the allowed error for each code.

4.0 MICROPROCESSOR INTERFACING

To dicuss the interface with 8080A and 6800 microprocessors, a common sample subroutine structure is used. The microprocessor starts the A/D, reads and stores the results of 16 successive conversions, then returns to the user's program. The 16 data bytes are stored in 16 successive memory locations. All Data and Addresses will be given in hexadecimal form. Software and hardware details are provided separately for each type of microprocessor.

4.1 Interfacing 8080 Microprocessor Derivatives (8048, 8085)

This converter has been designed to directly interface with derivatives of the 8080 microprocessor. The A/D can be mapped into memory space (using standard memory address decoding for $\overline{CS}$ and the $\overline{MEMR}$ and $\overline{MEMW}$ strobes) or it can be controlled as an I/O device by using the $\overline{I/O\ R}$ and $\overline{I/O\ W}$ strobes and decoding the address bits A0 → A7 (or address bits A8 → A15 as they will contain the same 8-bit address information) to obtain the $\overline{CS}$ input. Using the I/O space provides 256 additional addresses and may allow a simpler 8-bit address decoder but the data can only be input to the accumulator. To make use of the additional memory reference instructions, the A/D should be mapped into memory space. An example of an A/D in I/O space is shown in *Figure 10*.

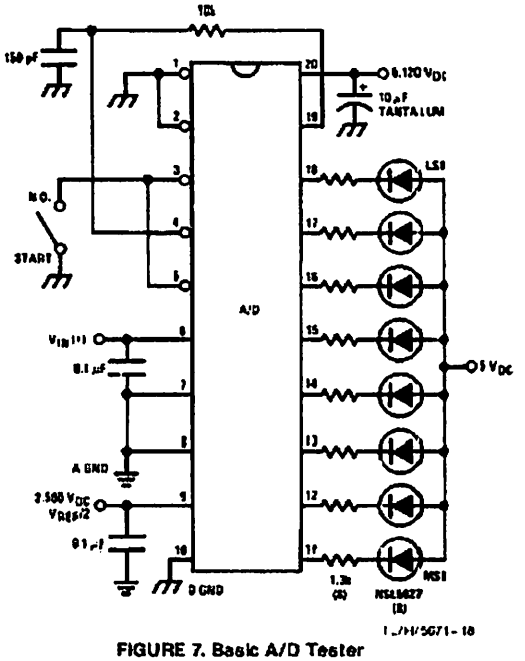


FIGURE 7. Basic A/D Tester

Functional Description (Continued)

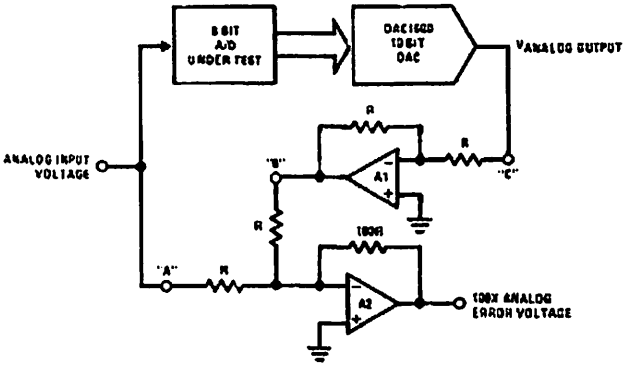


FIGURE 8. A/D Tester with Analog Error Output

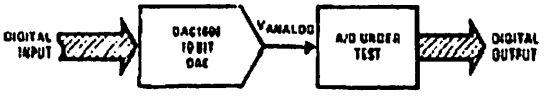


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FIGURE 9. Basic "Digital" A/D Tester

TABLE I. DECODING THE DIGITAL OUTPUT LEDs

HEX	BINARY	FRACTIONAL BINARY VALUE FOR		OUTPUT VOLTAGE CENTER VALUES WITH $V_{REF}/2 = 2.560\ V_{DC}$	
		MS GROUP	LS GROUP	VMS GROUP*	VLS GROUP*
F	1 1 1 1	15/16	15/256	4.800	0.300
E	1 1 1 0	7/8	7/128	4.480	0.280
D	1 1 0 1	13/16	13/256	4.160	0.260
C	1 1 0 0	3/4	3/64	3.840	0.240
B	1 0 1 1	11/16	11/256	3.520	0.220
A	1 0 1 0	5/8	5/128	3.200	0.200
9	1 0 0 1	9/16	9/256	2/880	0.180
8	1 0 0 0	1/2	1/32	2/560	0.160
7	0 1 1 1	7/16	7/256	2.240	0.140
6	0 1 1 0	3/8	3/128	1.920	0.120
5	0 1 0 1	5/16	2/256	1.600	0.100
4	0 1 0 0	1/4	1/64	1/280	0.080
3	0 0 1 1	3/16	3/256	0.960	0.060
2	0 0 1 0	1/8	1/128	0.640	0.040
1	0 0 0 1	1/16	1/256	0.320	0.020
0	0 0 0 0			0	0

*Display Output = VMS Group + VLS Group

Features

- Compatible with MCS-51™ Products
- 4K Bytes of In-System Programmable (ISP) Flash Memory
  - Endurance: 1000 Write/Erase Cycles
- 4.0V to 5.5V Operating Range
- Fully Static Operation: 0 Hz to 33 MHz
- Three-level Program Memory Lock
- 128 x 8-bit Internal RAM
- 32 Programmable I/O Lines
- Two 16-bit Timer/Counters
- Six Interrupt Sources
- Full Duplex UART Serial Channel
- Low-power Idle and Power-down Modes
- Interrupt Recovery from Power-down Mode
- Watchdog Timer
- Dual Data Pointer
- Power-off Flag
- Fast Programming Time
- Flexible ISP Programming (Byte and Page Mode)

Description

The AT89S51 is a low-power, high-performance CMOS 8-bit microcontroller with 4K bytes of in-system programmable Flash memory. The device is manufactured using Atmel's high-density nonvolatile memory technology and is compatible with the industry-standard 80C51 instruction set and pinout. The on-chip Flash allows the program memory to be reprogrammed in-system or by a conventional nonvolatile memory programmer. By combining a versatile 8-bit CPU with in-system programmable Flash on a monolithic chip, the Atmel AT89S51 is a powerful microcontroller which provides a highly-flexible and cost-effective solution to many embedded control applications.

The AT89S51 provides the following standard features: 4K bytes of Flash, 128 bytes of RAM, 32 I/O lines, Watchdog timer, two data pointers, two 16-bit timer/counters, a five-vector two-level interrupt architecture, a full duplex serial port, on-chip oscillator, and clock circuitry. In addition, the AT89S51 is designed with static logic for operation down to zero frequency and supports two software selectable power saving modes. The Idle Mode stops the CPU while allowing the RAM, timer/counters, serial port, and interrupt system to continue functioning. The Power-down mode saves the RAM contents but freezes the oscillator, disabling all other chip functions until the next external interrupt or hardware reset.

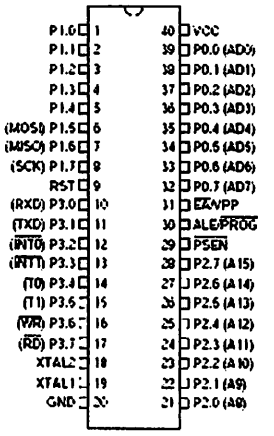
8-bit Microcontroller with 4K Bytes In-System Programmable Flash

AT89S51

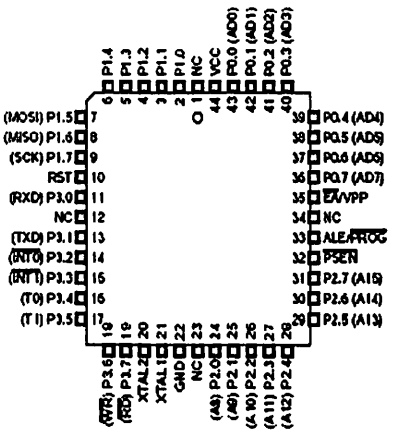
Rev. 2487A–10/01

Pin Configurations

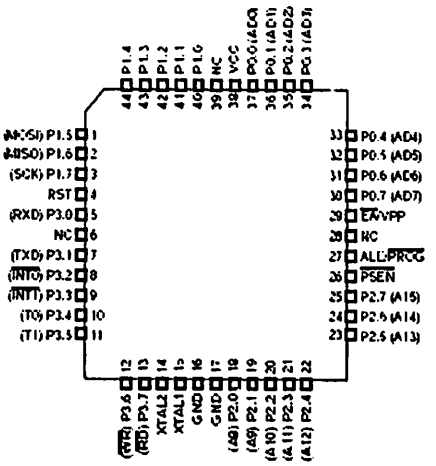
PDIP



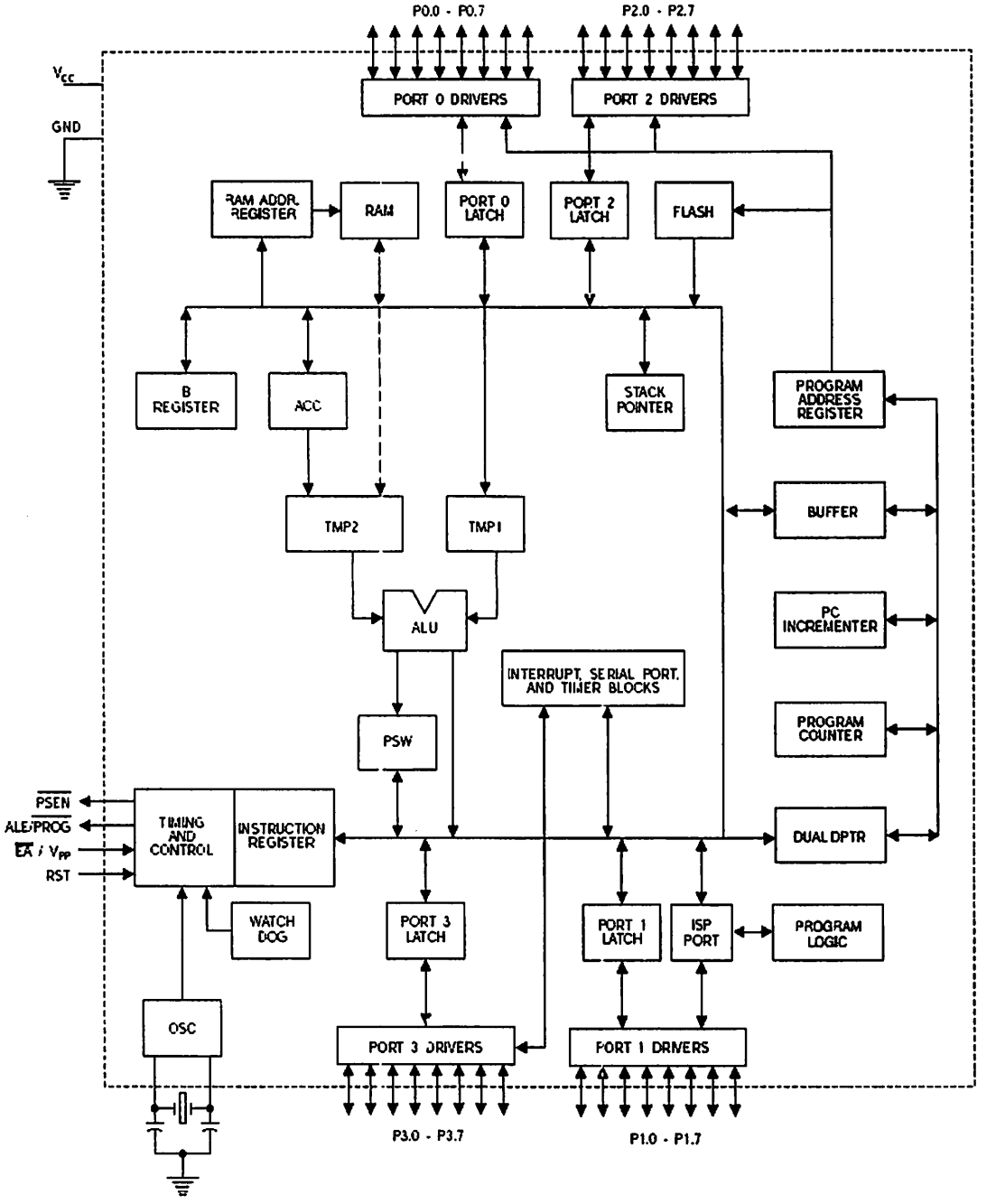
PLCC



TQFP



Block Diagram



Pin Description

VCC

Supply voltage.

GND

Ground.

Port 0

Port 0 is an 8-bit open drain bidirectional I/O port. As an output port, each pin can sink eight TTL inputs. When 1s are written to port 0 pins, the pins can be used as high-impedance inputs.

Port 0 can also be configured to be the multiplexed low-order address/data bus during accesses to external program and data memory. In this mode, P0 has internal pull-ups.

Port 0 also receives the code bytes during Flash programming and outputs the code bytes during program verification. **External pull-ups are required during program verification.**

Port 1

Port 1 is an 8-bit bidirectional I/O port with internal pull-ups. The Port 1 output buffers can sink/source four TTL inputs. When 1s are written to Port 1 pins, they are pulled high by the internal pull-ups and can be used as inputs. As inputs, Port 1 pins that are externally being pulled low will source current (I_{IL}) because of the internal pull-ups.

Port 1 also receives the low-order address bytes during Flash programming and verification.

Port Pin	Alternate Functions
P1.5	MOSI (used for In-System Programming)
P1.6	MISO (used for In-System Programming)
P1.7	SCK (used for In-System Programming)

Port 2

Port 2 is an 8-bit bidirectional I/O port with internal pull-ups. The Port 2 output buffers can sink/source four TTL inputs. When 1s are written to Port 2 pins, they are pulled high by the internal pull-ups and can be used as inputs. As inputs, Port 2 pins that are externally being pulled low will source current (I_{IL}) because of the internal pull-ups.

Port 2 emits the high-order address byte during fetches from external program memory and during accesses to external data memory that use 16-bit addresses (MOVX @ DPTR). In this application, Port 2 uses strong internal pull-ups when emitting 1s. During accesses to external data memory that use 8-bit addresses (MOVX @ RI), Port 2 emits the contents of the P2 Special Function Register.

Port 2 also receives the high-order address bits and some control signals during Flash programming and verification.

Port 3

Port 3 is an 8-bit bidirectional I/O port with internal pull-ups. The Port 3 output buffers can sink/source four TTL inputs. When 1s are written to Port 3 pins, they are pulled high by the internal pull-ups and can be used as inputs. As inputs, Port 3 pins that are externally being pulled low will source current (I_{IL}) because of the pull-ups.

Port 3 receives some control signals for Flash programming and verification.

Port 3 also serves the functions of various special features of the AT89S51, as shown in the following table.

Port Pin	Alternate Functions
P3.0	RXD (serial input port)
P3.1	TXD (serial output port)
P3.2	$\overline{INT0}$ (external interrupt 0)
P3.3	$\overline{INT1}$ (external interrupt 1)
P3.4	T0 (timer 0 external input)
P3.5	T1 (timer 1 external input)
P3.6	$\overline{WR}$ (external data memory write strobe)
P3.7	$\overline{RD}$ (external data memory read strobe)

RST

Reset input. A high on this pin for two machine cycles while the oscillator is running resets the device. This pin drives High for 98 oscillator periods after the Watchdog times out. The DISRTO bit in SFR AUXR (address 8EH) can be used to disable this feature. In the default state of bit DISRTO, the RESET HIGH out feature is enabled.

ALE/$\overline{PROG}$

Address Latch Enable (ALE) is an output pulse for latching the low byte of the address during accesses to external memory. This pin is also the program pulse input ($\overline{PROG}$) during Flash programming.

In normal operation, ALE is emitted at a constant rate of 1/6 the oscillator frequency and may be used for external timing or clocking purposes. Note, however, that one ALE pulse is skipped during each access to external data memory.

If desired, ALE operation can be disabled by setting bit 0 of SFR location 8EH. With the bit set, ALE is active only during a MOVX or MOVC instruction. Otherwise, the pin is weakly pulled high. Setting the ALE-disable bit has no effect if the microcontroller is in external execution mode.

$\overline{PSEN}$

Program Store Enable ($\overline{PSEN}$) is the read strobe to external program memory.

When the AT89S51 is executing code from external program memory, $\overline{PSEN}$ is activated twice each machine cycle, except that two $\overline{PSEN}$ activations are skipped during each access to external data memory.

$\overline{EA}$/VPP

External Access Enable. $\overline{EA}$ must be strapped to GND in order to enable the device to fetch code from external program memory locations starting at 0000H up to FFFFH. Note, however, that if lock bit 1 is programmed, $\overline{EA}$ will be internally latched on reset.

$\overline{EA}$ should be strapped to V_{CC} for internal program executions.

This pin also receives the 12-volt programming enable voltage (V_{PP}) during Flash programming.

XTAL1

Input to the inverting oscillator amplifier and input to the internal clock operating circuit.

XTAL2

Output from the inverting oscillator amplifier

Special Function Registers

A map of the on-chip memory area called the Special Function Register (SFR) space is shown in Table 1.

Note that not all of the addresses are occupied, and unoccupied addresses may not be implemented on the chip. Read accesses to these addresses will in general return random data, and write accesses will have an indeterminate effect.

Table 1. AT89S51 SFR Map and Reset Values

0F8H									0FFH
0F0H	B 00000000								0F7H
0E8H									0EFH
0E0H	ACC 00000000								0E7H
0D8H									0DFH
0D0H	PSW 00000000								0D7H
0C8H									0CFH
0C0H									0C7H
0B8H	IP XX000000								0BFH
0B0H	P3 11111111								0B7H
0A8H	IE 0X000000								0AFH
0A0H	P2 11111111		AUXR1 XXXXXXX0				WDTRST XXXXXXXX		0A7H
98H	SCON 00000000	SBUF XXXXXXXX							9FH
90H	P1 11111111								97H
88H	TCON 00000000	TMOD 00000000	TL0 00000000	TL1 00000000	TH0 00000000	TH1 00000000	AUXR XXX00XX0		8FH
80H	P0 11111111	SP 00000111	DP0L 00000000	DP0H 00000000	DP1L 00000000	DP1H 00000000		PCON 0XXX0000	87H

User software should not write 1s to these unlisted locations, since they may be used in future products to invoke new features. In that case, the reset or inactive values of the new bits will always be 0.

Interrupt Registers: The individual interrupt enable bits are in the IE register. Two priorities can be set for each of the five interrupt sources in the IP register.

Table 2. AUXR: Auxiliary Register

AUXR — Address = 8EH — Reset Value = XXX00XX0B

Not Bit Addressable

	-	-	-	WDIDLE	DISRTO	-	-	DISALE
Bit	7	6	5	4	3	2	1	0

Reserved for future expansion

DISALE Disable/Enable ALE

DISALE Operating Mode

0 ALE is emitted at a constant rate of 1/6 the oscillator frequency

1 ALE is active only during a MOVX or MOVC instruction

DISRTO Disable/Enable Reset out

DISRTO

0 Reset pin is driven High after WDT times out

1 Reset pin is input only

WDIDLE Disable/Enable WDT in IDLE mode

WDIDLE

0 WDT continues to count in IDLE mode

1 WDT halts counting in IDLE mode

Dual Data Pointer Registers: To facilitate accessing both internal and external data memory, two banks of 16-bit Data Pointer Registers are provided: DP0 at SFR address locations 82H-83H and DP1 at 84H-85H. Bit DPS = 0 in SFR AUXR1 selects DP0 and DPS = 1 selects DP1. The user should always initialize the DPS bit to the appropriate value before accessing the respective Data Pointer Register.

Power Off Flag: The Power Off Flag (POF) is located at bit 4 (PCON.4) in the PCON SFR. POF is set to "1" during power up. It can be set and rest under software control and is not affected by reset.

Table 3. AUXR1: Auxiliary Register 1

AUXR1

Address = A2H

Reset Value = XXXXXXX0B

Not Bit Addressable

Bit	7	6	5	4	3	2	1	0
	-	-	-	-	-	-	-	DPS

Reserved for future expansion

DPS Data Pointer Register Select

DPS	
0	Selects DPTR Registers DP0L, DP0H
1	Selects DPTR Registers DP1L, DP1H

Memory Organization

MCS-51 devices have a separate address space for Program and Data Memory. Up to 64K bytes each of external Program and Data Memory can be addressed

Program Memory

If the $\overline{EA}$ pin is connected to GND, all program fetches are directed to external memory.

On the AT89S51, if $\overline{EA}$ is connected to V_{CC}, program fetches to addresses 0000H through FFFH are directed to internal memory and fetches to addresses 1000H through FFFFH are directed to external memory.

Data Memory

The AT89S51 implements 128 bytes of on-chip RAM. The 128 bytes are accessible via direct and indirect addressing modes. Stack operations are examples of indirect addressing, so the 128 bytes of data RAM are available as stack space.

Watchdog Timer (One-time Enabled with Reset-out)

The WDT is intended as a recovery method in situations where the CPU may be subjected to software upsets. The WDT consists of a 14-bit counter and the Watchdog Timer Reset (WDTRST) SFR. The WDT is defaulted to disable from exiting reset. To enable the WDT, a user must write 01EH and 0E1H in sequence to the WDTRST register (SFR location 0A6H). When the WDT is enabled, it will increment every machine cycle while the oscillator is running. The WDT timeout period is dependent on the external clock frequency. There is no way to disable the WDT except through reset (either hardware reset or WDT overflow reset). When WDT overflows, it will drive an output RESET HIGH pulse at the RST pin.

Using the WDT

To enable the WDT, a user must write 01EH and 0E1H in sequence to the WDTRST register (SFR location 0A6H). When the WDT is enabled, the user needs to service it by writing 01EH and 0E1H to WDTRST to avoid a WDT overflow. The 14-bit counter overflows when it reaches 16383 (3FFFH), and this will reset the device. When the WDT is enabled, it will increment every machine cycle while the oscillator is running. This means the user must reset the WDT at least every 16383 machine cycles. To reset the WDT the user must write 01EH and 0E1H to WDTRST. WDTRST is a write-only register. The WDT counter cannot be read or written. When WDT overflows, it will generate an output RESET pulse at the RST pin. The RESET pulse duration is 98xTOSC, where TOSC=1/FOSC. To make the best use of the WDT, it

should be serviced in those sections of code that will periodically be executed within the time required to prevent a WDT reset.

WDT During Power-down and Idle

In Power-down mode the oscillator stops, which means the WDT also stops. While in Power-down mode, the user does not need to service the WDT. There are two methods of exiting Power-down mode: by a hardware reset or via a level-activated external interrupt, which is enabled prior to entering Power-down mode. When Power-down is exited with hardware reset, servicing the WDT should occur as it normally does whenever the AT89S51 is reset. Exiting Power-down with an interrupt is significantly different. The interrupt is held low long enough for the oscillator to stabilize. When the interrupt is brought high, the interrupt is serviced. To prevent the WDT from resetting the device while the interrupt pin is held low, the WDT is not started until the interrupt is pulled high. It is suggested that the WDT be reset during the interrupt service for the interrupt used to exit Power-down mode.

To ensure that the WDT does not overflow within a few states of exiting Power-down, it is best to reset the WDT just before entering Power-down mode.

Before going into the IDLE mode, the WDIDLE bit in SFR AUXR is used to determine whether the WDT continues to count if enabled. The WDT keeps counting during IDLE (WDIDLE bit = 0) as the default state. To prevent the WDT from resetting the AT89S51 while in IDLE mode, the user should always set up a timer that will periodically exit IDLE, service the WDT, and reenter IDLE mode.

With WDIDLE bit enabled, the WDT will stop to count in IDLE mode and resumes the count upon exit from IDLE.

UART

The UART in the AT89S51 operates the same way as the UART in the AT89C51. For further information on the UART operation, refer to the ATMEL Web site (http://www.atmel.com). From the home page, select 'Products', then '8051-Architecture Flash Microcontroller', then 'Product Overview'.

Timer 0 and 1

Timer 0 and Timer 1 in the AT89S51 operate the same way as Timer 0 and Timer 1 in the AT89C51. For further information on the timers' operation, refer to the ATMEL Web site (http://www.atmel.com). From the home page, select 'Products', then '8051-Architecture Flash Microcontroller', then 'Product Overview'.

Interrupts

The AT89S51 has a total of five interrupt vectors: two external interrupts ($\overline{INT0}$ and $\overline{INT1}$), two timer interrupts (Timers 0 and 1), and the serial port interrupt. These interrupts are all shown in Figure 1.

Each of these interrupt sources can be individually enabled or disabled by setting or clearing a bit in Special Function Register IE. IE also contains a global disable bit, EA, which disables all interrupts at once.

Note that Table 4 shows that bit position IE.6 is unimplemented. In the AT89S51, bit position IE.5 is also unimplemented. User software should not write 1s to these bit positions, since they may be used in future AT89 products.

The Timer 0 and Timer 1 flags, TF0 and TF1, are set at S5P2 of the cycle in which the timers overflow. The values are then polled by the circuitry in the next cycle

Table 4. Interrupt Enable (IE) Register

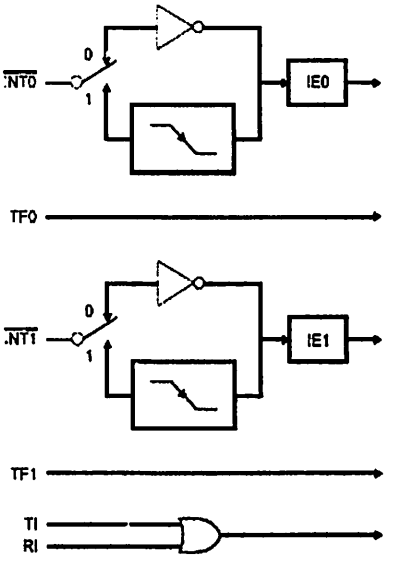
(MSB)							(LSB)
EA	–	–	ES	ET1	EX1	ET0	EX0

Enable Bit = 1 enables the interrupt.

Enable Bit = 0 disables the interrupt.

Symbol	Position	Function
EA	IE.7	Disables all interrupts. If EA = 0, no interrupt is acknowledged. If EA = 1, each interrupt source is individually enabled or disabled by setting or clearing its enable bit.
–	IE.6	Reserved
–	IE.5	Reserved
ES	IE.4	Serial Port interrupt enable bit
ET1	IE.3	Timer 1 interrupt enable bit
EX1	IE.2	External interrupt 1 enable bit
ET0	IE.1	Timer 0 interrupt enable bit
EX0	IE.0	External interrupt 0 enable bit
User software should never write 1s to reserved bits, because they may be used in future AT89 products.		

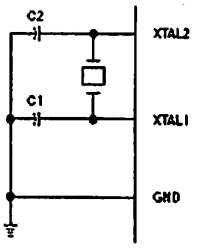
Figure 1. Interrupt Sources



Oscillator Characteristics

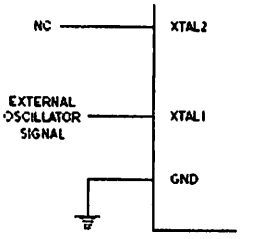
XTAL1 and XTAL2 are the input and output, respectively, of an inverting amplifier that can be configured for use as an on-chip oscillator, as shown in Figure 2. Either a quartz crystal or ceramic resonator may be used. To drive the device from an external clock source, XTAL2 should be left unconnected while XTAL1 is driven, as shown in Figure 3. There are no requirements on the duty cycle of the external clock signal, since the input to the internal clocking circuitry is through a divide-by-two flip-flop, but minimum and maximum voltage high and low time specifications must be observed.

Figure 2. Oscillator Connections



Note: C1, C2 = 30 pF ± 10 pF for Crystals = 40 pF ± 10 pF for Ceramic Resonators

Figure 3. External Clock Drive Configuration



Idle Mode

In idle mode, the CPU puts itself to sleep while all the on-chip peripherals remain active. The mode is invoked by software. The content of the on-chip RAM and all the special function registers remain unchanged during this mode. The idle mode can be terminated by any enabled interrupt or by a hardware reset.

Note that when idle mode is terminated by a hardware reset, the device normally resumes program execution from where it left off, up to two machine cycles before the internal reset algorithm takes control. On-chip hardware inhibits access to internal RAM in this event, but access to the port pins is not inhibited. To eliminate the possibility of an unexpected write to a port pin when idle mode is terminated by a reset, the instruction following the one that invokes idle mode should not write to a port pin or to external memory.

Power-down Mode

In the Power-down mode, the oscillator is stopped, and the instruction that invokes Power-down is the last instruction executed. The on-chip RAM and Special Function Registers retain their values until the Power-down mode is terminated. Exit from Power-down mode can be initiated either by a hardware reset or by activation of an enabled external interrupt into $\overline{INT0}$ or $\overline{INT1}$. Reset redefines the SFRs but does not change the on-chip RAM. The reset should not be activated before V_{CC} is restored to its normal operating level and must be held active long enough to allow the oscillator to restart and stabilize.

Table 5. Status of External Pins During Idle and Power-down Modes

Mode	Program Memory	ALE	$\overline{PSEN}$	PORT0	PORT1	PORT2	PORT3
Idle	Internal	1	1	Data	Data	Data	Data
Idle	External	1	1	Float	Data	Address	Data
Power-down	Internal	0	0	Data	Data	Data	Data
Power-down	External	0	0	Float	Data	Data	Data

Program Memory Lock Bits

The AT89S51 has three lock bits that can be left unprogrammed (U) or can be programmed (P) to obtain the additional features listed in the following table.

Table 6. Lock Bit Protection Modes

Program Lock Bits				
	LB1	LB2	LB3	Protection Type
1	U	U	U	No program lock features
2	P	U	U	MOVC instructions executed from external program memory are disabled from fetching code bytes from internal memory, $\overline{EA}$ is sampled and latched on reset, and further programming of the Flash memory is disabled
3	P	P	U	Same as mode 2, but verify is also disabled
4	P	P	P	Same as mode 3, but external execution is also disabled

When lock bit 1 is programmed, the logic level at the $\overline{EA}$ pin is sampled and latched during reset. If the device is powered up without a reset, the latch initializes to a random value and holds that value until reset is activated. The latched value of $\overline{EA}$ must agree with the current logic level at that pin in order for the device to function properly.

Programming the Flash – Parallel Mode

The AT89S51 is shipped with the on-chip Flash memory array ready to be programmed. The programming interface needs a high-voltage (12-volt) program enable signal and is compatible with conventional third-party Flash or EPROM programmers.

The AT89S51 code memory array is programmed byte-by-byte.

Programming Algorithm: Before programming the AT89S51, the address, data, and control signals should be set up according to the Flash programming mode table and Figures 13 and 14. To program the AT89S51, take the following steps:

1. Input the desired memory location on the address lines.
2. Input the appropriate data byte on the data lines.
3. Activate the correct combination of control signals.
4. Raise $\overline{EA}/V_{PP}$ to 12V.
5. Pulse ALE/$\overline{PROG}$ once to program a byte in the Flash array or the lock bits. The byte-write cycle is self-timed and typically takes no more than 50 µs. Repeat steps 1 through 5, changing the address and data for the entire array or until the end of the object file is reached.

$\overline{Data}$ Polling: The AT89S51 features $\overline{Data}$ Polling to indicate the end of a byte write cycle. During a write cycle, an attempted read of the last byte written will result in the complement of the written data on P0.7. Once the write cycle has been completed, true data is valid on all outputs, and the next cycle may begin. $\overline{Data}$ Polling may begin any time after a write cycle has been initiated.

Ready/$\overline{\text{Busy}}$: The progress of byte programming can also be monitored by the RDY/$\overline{\text{BSY}}$ output signal. P3.0 is pulled low after ALE goes high during programming to indicate $\overline{\text{BUSY}}$. P3.0 is pulled high again when programming is done to indicate READY.

Program Verify: If lock bits LB1 and LB2 have not been programmed, the programmed code data can be read back via the address and data lines for verification. The status of the individual lock bits can be verified directly by reading them back.

Reading the Signature Bytes: The signature bytes are read by the same procedure as a normal verification of locations 000H, 100H, and 200H, except that P3.6 and P3.7 must be pulled to a logic low. The values returned are as follows.

(000H) = 1EH indicates manufactured by Atmel
(100H) = 51H indicates 89S51
(200H) = 06H

Chip Erase: In the parallel programming mode, a chip erase operation is initiated by using the proper combination of control signals and by pulsing ALE/$\overline{\text{PROG}}$ low for a duration of 200 ns - 500 ns.

In the serial programming mode, a chip erase operation is initiated by issuing the Chip Erase instruction. In this mode, chip erase is self-timed and takes about 500 ms.

During chip erase, a serial read from any address location will return 00H at the data output.

Programming the Flash – Serial Mode

The Code memory array can be programmed using the serial ISP interface while RST is pulled to V_{CC}. The serial interface consists of pins SCK, MOSI (input) and MISO (output). After RST is set high, the Programming Enable instruction needs to be executed first before other operations can be executed. Before a reprogramming sequence can occur, a Chip Erase operation is required.

The Chip Erase operation turns the content of every memory location in the Code array into FFH.

Either an external system clock can be supplied at pin XTAL1 or a crystal needs to be connected across pins XTAL1 and XTAL2. The maximum serial clock (SCK) frequency should be less than 1/16 of the crystal frequency. With a 33 MHz oscillator clock, the maximum SCK frequency is 2 MHz.

Serial Programming Algorithm

To program and verify the AT89S51 in the serial programming mode, the following sequence is recommended:

1. Power-up sequence:

   Apply power between VCC and GND pins.

   Set RST pin to "H".

   If a crystal is not connected across pins XTAL1 and XTAL2, apply a 3 MHz to 33 MHz clock to XTAL1 pin and wait for at least 10 milliseconds.
2. Enable serial programming by sending the Programming Enable serial instruction to pin MOSI/P1.5 The frequency of the shift clock supplied at pin SCK/P1.7 needs to be less than the CPU clock at XTAL1 divided by 16.
3. The Code array is programmed one byte at a time in either the Byte or Page mode. The write cycle is self-timed and typically takes less than 0.5 ms at 5V.
4. Any memory location can be verified by using the Read instruction that returns the content at the selected address at serial output MISO/P1.6.
5. At the end of a programming session, RST can be set low to commence normal device operation.

Power-off sequence (if needed):

Set XTAL1 to "L" (if a crystal is not used).

Set RST to "L".

Turn V_{CC} power off.

Data Polling: The Data Polling feature is also available in the serial mode. In this mode, during a write cycle an attempted read of the last byte written will result in the complement of the MSB of the serial output byte on MISO.

Serial Programming Instruction Set

The Instruction Set for Serial Programming follows a 4-byte protocol and is shown in Table 8 on page 18.

Programming Interface – Parallel Mode

Every code byte in the Flash array can be programmed by using the appropriate combination of control signals. The write operation cycle is self-timed and once initiated, will automatically time itself to completion.

All major programming vendors offer worldwide support for the Atmel microcontroller series. Please contact your local programming vendor for the appropriate software revision.

Table 7. Flash Programming Modes

Mode	V_{CC}	RST	PSEN	ALE/PROG	EA/V_{PP}	P2.6	P2.7	P3.3	P3.6	P3.7	P0.7-0 Data	P2.3-0 Address	P1.7-0 Address
Write Code Data	5V	H	L	(2)	12V	L	H	H	H	H	D_{IN}	A11-8	A7-0
Read Code Data	5V	H	L	H	H	L	L	L	H	H	D_{OUT}	A11-8	A7-0
Write Lock Bit 1	5V	H	L	(3)	12V	H	H	H	H	H	X	X	X
Write Lock Bit 2	5V	H	L	(3)	12V	H	H	H	L	L	X	X	X
Write Lock Bit 3	5V	H	L	(3)	12V	H	L	H	H	L	X	X	X
Read Lock Bits 1, 2, 3	5V	H	L	H	H	H	H	L	H	L	P0.2, P0.3, P0.4	X	X
Chip Erase	5V	H	L	(1)	12V	H	L	H	L	L	X	X	X
Read Atmel ID	5V	H	L	H	H	L	L	L	L	L	1EH	0000	00H
Read Device ID	5V	H	L	H	H	L	L	L	L	L	51H	0001	00H
Read Device ID	5V	H	L	H	H	L	L	L	L	L	06H	0010	00H

Notes:
1. Each PROG pulse is 200 ns - 500 ns for Chip Erase.
2. Each PROG pulse is 200 ns - 500 ns for Write Code Data.
3. Each PROG pulse is 200 ns - 500 ns for Write Lock Bits.
4. RDY/BSY signal is output on P3.0 during programming.
5. X = don't care.

Figure 4. Programming the Flash Memory (Parallel Mode)

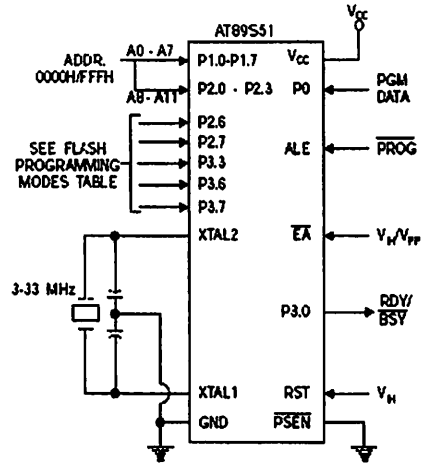
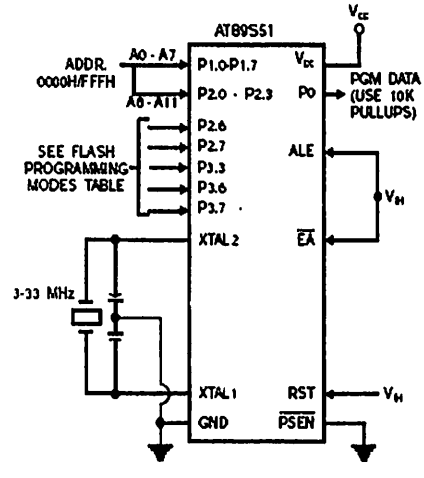
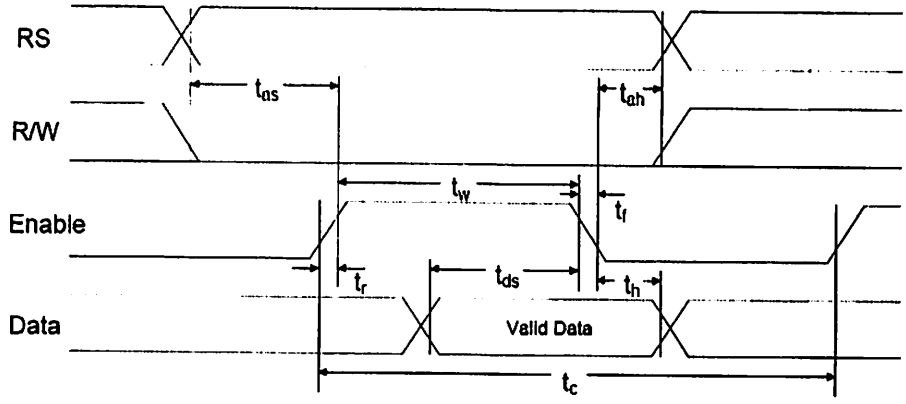


Figure 5. Verifying the Flash Memory (Parallel Mode)



Instruction	RS	RW	D7	D6	D5	D4	D3	D2	D1	D0	Description	Clocks
NOP	0	0	0	0	0	0	0	0	0	0	No Operation	0
Clear Display	0	0	0	0	0	0	0	0	0	1	Clears display & sets address counter to zero.	165
Cursor Home	0	0	0	0	0	0	0	0	1	0	Sets address counter to zero, returns shifted display to original position. DDRAM contents remains unchanged.	3
Entry Mode Set	0	0	0	0	0	0	0	1	I/D	S	Sets cursor move direction, and specifies automatic shift.	3
Display Control	0	0	0	0	0	0	1	D	C	B	Turns display (D), cursor on/off (C) or cursor blinking(B).	3
Cursor/display shift	0	0	0	0	0	1	S/C	R/L	0	0	Moves cursor and shift display. DDRAM contents remains unchanged.	3
Function Set	0	0	0	0	1	DL	N	M	G	0	Sets interface data width(DL), number of display lines (N.M) and voltage generator control (G).	3
Set CGRAM Addr	0	0	0	1	Character Generator RAM						Sets CGRAM Address	3
Set DDRAM Addr	0	0	1	Display Data RAM Address							Sets DDRAM Address	3
Busy Flag & Addr	0	1	BF	Address Counter							Reads Busy Flag & Address Counter	0
Read Data	1	0	Read Data								Reads data from CGRAM or DDRAM	3
Write Data	1	1	Write Data								Writes data from CGRAM or DDRAM	3

Write Cycle

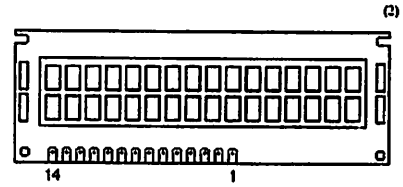


Parameter	Symbol	Min [1]	Typ [1]	Max [1]	Unit
Enable Cycle Time	t_c	500	-	-	ns
Enable Pulse Width (High)	t_w	230	-	-	ns
Enable Rise/Fall Time	t_r,t_f	-	-	20	ns
Address Setup Time	t_{as}	40	-	-	ns
Address Hold Time	t_{ah}	10	-	-	ns
Data Setup Time	t_{ds}	80	-		ns
Data Hold Time	t_h	10	-	-	ns

Note [1] The above specifications are a indication only. Timing will vary from manufacturer to manufacturer.

Note [2] A 2 line by 16 Character LCD Module is Pictured. Data will work on most 1 line x 16 character, 1 line x 20 character, 2 line x 16 character, 2 line x 20 character, 4 lines x 20 character, 2 lines x 40 character etc. modules compatible with the HD44780 LCD Module.

[2]



Pin No	Name	I/O	Description
1	Vss	Power	GND
2	Vdd	Power	+5v
3	Vo	Analog	Contrast Control
4	RS	Input	Register Select
5	R/W	Input	Read/Write
6	E	Input	Enable *(Strobe)*
7	D0	I/O	Data *LSB*
8	D1	I/O	Data
9	D2	I/O	Data
10	D3	I/O	Data
11	D4	I/O	Data
12	D5	I/O	Data
13	D6	I/O	Data
14	D7	I/O	Data *MSB*