INSTITUT TEKNOLOGI NASIONAL MALANG
FAKULTAS TEKNOLOGI INDUSTRI
JURUSAN TEKNIK ELEKTRO S -1
KONSENTRASI TEKNIK ELEKTRONIKA

PERENCANAAN DAN PEMBUATAN ALAT PENGUKUR ARUS LISTRIK DENGAN SISTEM INDUKSI (TANG AMPERE) MENGGUNAKAN TEKNOLOGI VHDL

SKRIPSI

Disusun Oleh :

ALI MUNTAHA
00.17.271

SEPTEMBER 2005

LEMBAR PERSETUJUAN

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SKRIPSI

Disusun dan diajukan sebagai salah satu syarat untuk memperoleh gelar Sarjana Teknik Elektronika Strata Satu (S-1)

Disusun Oleh :

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2005

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ABSTRAKSI

PERENCANAAN DAN PEMBUATAN ALAT PENGUKUR ARUS LISTRIK DENGAN SISTEM INDUKSI (TANG AMPERE) MENGGUNAKAN TEKNOLOGI VHDL

(Ali Muntaha, NIM : 0017271, Teknik Elektro/Elektronika S-1, 60 halaman)

(Dosen Pembimbing : Ir. Teguh Herbasuki, MT)

Kata Kunci : *Pengukur arus listrik, Teknologi VHDL*

Dalam skripsi ini dibahas suatu perencanaan dan pembuatan alat pengukur arus listrik dengan sistem induksi (Tang Ampere) menggunakan teknologi VHDL. Hal ini diharapkan dapat membuat suatu alat ukur yang tidak perlu mengupas kabel terlebih dahulu.

Perencanaan blok diagram alat yang direncanakan ini meliputi sensor induksi arus listrik, pengkondisi sinyal, pembanding 74ls85, GAL 22v10 dan GAL 16V8, sevent segment. Sensor induksi untuk mengetahui adanya induksi arus listrik pada suatu pengahantar, Pengkondisi sinyal digunakan untuk mengkondisikan sinyal keluaran dari sensor agar dapat dibaca oleh ADC, ADC digunakan untuk mengolag tegangan analog menjadi data biner agar dapat di olah oleh IC GAL., pembanding digunakn untuk mmbandingkan data dari ADC dengan data keluaran dari GAL 22v10, multiplekser analog digunakan untuk memilih range pengukuran, clock digunakan untuk mebangkitkan sinyal detak pada IC gal. Gal 16v8 dan seven segment digunakan sebagai unit display untuk menampilkan hasil pengukuran.

KATA PENGANTAR

Dengan mengucapkan puji syukur kehadirat Tuhan Yang Maha Esa Penulis dapat menyelesaikan skripsi ini karena berkat rahmat-Nyalah Penulis dapat menyusun skripsi ini yang menjadi salah satu syarat akademik dalam menyelesaikan studi untuk menempuh gelar Sarjana S-1 di Fakultas Teknologi Industri Jurusan Teknik Elektro di Institut Teknologi Nasional Malang.

Skripsi ini disusun berdasarkan hasil-hasil percobaan beserta teori dasar dan beberapa jawaban pertanyaan dari permasalahan yang ada sehinga Penulis sekaligus Penyusun dapat menambah wawasan dan tidak hanya menguasai teori saja namun juga memahami pengetahuan tersebut secara teknis.

Tersusunnya skripsi ini karena adanya dorongan, masukan, juga fasilitas dari pihak-pihak yang berhubungan dengan pelaksanaan dan penyusunan skripsi ini. Oleh karena itu penulis mengucapkan terima kasih yang sebesar-besarnya kepada :

1. Dr. Ir. Abraham Lomi, MSEE selaku Rektor Institut Teknologi Nasional Malang
2. Ir. Yudi Limpraptono, MT selaku Ketua Jurusan Teknik Elektro Institut Teknologi Nasional Malang
3. Ir. Teguh Herbasuki, MT selaku Dosen Pembimbing
4. Rekan-rekan yang telah banyak membantu dalam pelaksanaan dan penyusunan skripsi ini.

Namun Penulis sadar bahwa isi dari skripsi ini masih jauh dari sempurna. Oleh sebab itu kritik dan saran yang membangun sangat penulis harapkan guna dalam perbaikan pada periode mendatang.

Penyusun berharap semoga skripsi ini dapat bermanfaat bagi Penyusun sendiri juga pembaca sekalian.

Malang, September 2005

Penulis

LEMBAR PERSEMBAHAN

Ketika aku sadar bahwa tulisan ini hanyalah serik dari hidup yang sesungguhnya, maka semua kata mengap lenyap. Sebutir debu ditengah sahara yang berbisik halus nyaris tak terdengar. Namun setidaknya, ia mencoba berkata-kata. Dan semoga ini ada gunanya.

Saya datang kedunia ini tidak sendiri melainkan bersama kedua orang tuaku tercinta, Bapak Sudirman dan Ibu tercinta Suminі. Terimakasih dan sembah bakti ku untuk mu, aku merasakan kebahagian hidup bersama bimbingan dan didikan mu, yang akhirnya dapat membetuk pribadi yang tangguh.

Terima kasih buat saudara-saudara kandungku, kakaku mas Muryanto n istri, kerja yang rajin biar cepet jadi orang sukses n Melinda cepetan gede ya... Mbak Sri ahyanik, juga harus ranjin-2 kerja, tapi jangan lupa me-manage uang, gak usah pusing-2 mbeliin baju buat adiknya klo mo lebaran. Buat adik ku Choirul wakhidah, harus rajin kuliah n klo ngajar murid-2nya jangan galak-2.

Terima kasih buat Kep.sek SMK YP 17-1 Madiun, Bp. Suryanto Budi .W, saya sudah diberi kesempatan nimba ilmu n kerja di situ. Bp. Sujadi, kajur T.Listrik, moga kita tetep bisa sharing saling tukar ilmu pengetahuan.

Dan semua rekan kerja di SMK YP 17-1 Madiun.

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BAB I

PENDAHULUAN

1.1. Latar Belakang

Pada perkembangan teknologi pada masa sekarang ini, banyak digunakan instrumentasi elektronika yang dapat memudahkan manusia dalam menjalankan tugas kesehariannya. Elektronika otomatisasi dinilai dapat menggantikan tugas para pekerja dengan efisien, praktis dan nyaman. Khususnya dibidang instrumentasi juga diperlukan suatu penemuan alat maupun otomatisasi kontrol yang dapat membantu mereka untuk mempermudah pekerjaan guna mempersingkat waktu dengan hasil yang memuaskan.

Dengan memperhatikan kesulitan dari para teknisi yang ternyata dalam mengetahui berapa besar arus yang mengalir pada beban masih banyak mengalami kendala yaitu harus merangkai secara seri alat ukur arus (ampere meter) dengan beban yang akan di ukur arusnya. Untuk melakukan pemasangan seri antara alat ukur dengan beban, maka beban mau tidak mau harus dimatikan dulu baru dapat dilakukan pemasangan ampere meter. Pemutusan arus listrik pada beban terlebih dulu tidak akan begitu terasa akibatnya, kalau beban yang akan diukur tidak begitu penting, lain halnya kalau pada suatu proses produksi yang menuntut beban (mesin listrik) yang akan dimatikan harus secara kontinyu bekerja. Maka pemutusan arus listrik pada beban tersebut akan fatal dampaknya, bisa jadi mesin-mesin berikutnya tidak bekerja, dan berapa besar kerugian yang akan ditanggung akibat dari pemutusan tersebut. Maka agar mudah untuk mengetahui berapa besar arus listrik yang mengalir pada beban tanpa harus

memutus arus listrik yang mengalir pada beban, saya merencanakan suatu alat Pengukur Arus Listrik Menggunakan Sistem Induksi (Ampere Meter) Menggunakan Teknologi VHDL untuk menghindari terjadinya pemutusan sementara pada beban yang akan diketahui berapa besar arus yang mengalir, apakah masih sesuai dengan spesifikasi mesin listrik tersebut atau sudah over load. Dengan sebuah alat pengukur arus secara induksi ini diharapkan baik para teknisi maupun masyarakat bisa dengan mudah melakukan pengukuran arus listrik.

1.2. Rumusan Masalah

Pada laporan skripsi ini di rumuskan beberapa permasalahan yang nantinya akan di bahas dan dipecahkan pada perencanaan alat antara lain:

1. Bagaimana cara mengambil induksi arus listrik pada penghantar yang dilalui aoleh arus listrik.
2. Bagaimana cara kerja sensor untuk merubah induksi arus listrik menjadi tegangan agar dapat di baca oleh Analog To Digital Converter
3. Bagaimana cara menentukan range selector
4. Bagaimana menampilkan perubahan tegangan yang terjadi menjadi angka pada Seven–segment.

1.3. Tujuan

Adapun tujuan dari penulisan skripsi adalah merancang dan membuat alat Pengukur Arus Listrik Menggunakan Sistem Induksi (Ampere Meter)

Menggunakan Teknologi VHDL, sehingga dapat mempermudah para teknisi untuk melakukan pengukuran arus tanpa mematikan beban terlebih dulu.

1.4. Batasan masalah

Dalam penyusunan skripsi ini diperlukan batasan masalah agar tidak menyimpang dari ruang lingkup yang akan dibahas. Adapun batasan masalah adalah sebagai berikut:

- Alat ini menggunakan IC PLD GAL16V8 dan GAL 22v10 yang difungsikan sebagai unit kontrol utama.
- Hanya membahas perangkat kerasnya, sedangkan perancangan perangkat lunaknya dibahas secara garis besar
- Tidak membahas besarnya flux yang timbul akibat perubahan arus listrik.
- Tidak membahas catu daya

1.5. Metodologi

Metodologi yang digunakan untuk perencanaan dan pembuatan laporan skripsi ini adalah:

1. Pengumpulan literatur

   Mempelajari teori tentang VHDL yaitu cara pemrograman dan simulasinya serta teori penunjang yang lain.

2. Perencanaan dan pembuatan

   Setelah melakukan pengumpulan literatur maka dilakukan perencanaan dan pembuatan perangkat keras dan perangkat lunak untuk membentuk suatu sistem.

3. Pengujian alat

   Setelah rangkaian selesai di rakit maka di lakukan pengujian perangkat keras dan lunak. Pengujian dilakukan pada setiap bagian setelah semuanya siap.

1.6 . Sistematika

Ada pun sistematika dari penyusunan laporan tugas akhir ini adalah :

BAB I PENDAHULUAN

Berisi tentang latar belakang, rumusan masalah, tujuan, batasan masalah, metodologi penulisan, dan sistematika penyusunan dan pembuatan alat.

BAB II DASAR TEORI

Berisi tentang teori dasar yang memiliki hubungan sebagai dasar dari perencanaan dan pembuatan alat.

BAB III PERENCANAAN DAN PEMBUATAN

Berisi tentang perencanaan hardware dan software.

BAB IV PENGUJIAN ALAT

Berisi tentang data hasil pengujian alat yang telah dibuat secara kescluruhan .

BAB V PENUTUP

Berisi Kesimpulan dari hasil pengujian alat dan saran.

BAB II
DASAR TEORI

2.1. Verry High Speed Integrated Circuit Hardware Discription Language (VHDL)

2.1.1. Sejarah VHDL

DI Pertengahan tahun 1980, departemen pertahanan Amerika Serikat (Departemet of Defense (DoD) dan IEEE menseponsori pengembangan bahasa pemrograman tingkat tinggi Hardware Description Language yang kemudian di sebut dengan VHDL. Sejak di perkenalkan VHDL memiliki beberapa kelebihan antara lain:

- Dapat dilakukan dengan desain terpisah secara hirarki.
- Setiap komponen yang di desain dapat saling di hubungkan secara tepat menurut spesifikasi prilaku komponen yang di desain.
- Spesifikasi prilaku dari desain dapat di bentuk melalui algoritma atau struktur hardware sesungguhnya.
- Persetujuan,pewaktuan dan clocking dapat dimodel dan VHDL dapat pula menangani struktur scquential asinkronous dan sinkronous.
- Operasi logika dan pewaktuan pada desain dapat di simulasikan.

Dengan kelebihan yang di milikinya VHDL di luncurkan berupa dokumentasi dan bahasa modeling dengan memperhitungkan desain digital untuk ketepatan/ keakuratannya serta dapat mensimulasikannya.

Sebagai bahasa modeling dan simulasi VHDL merupakan Inovasi yang sangat penting. Alat-alat VHDL dan popularitasnya, membuat sebuah *Quantum leap*

dengan perkembangan perdagangan pada alat-alat p[1]erpaduan VHDL. Program ini dapat membuat sirkuit logika langsung dari deskripsi behavioral dan dapat mendesain, mensimulasi dan memadukan segala sesuatu dari sebuah sirkuit kombinasi yang sederhana untuk melengkapi sebuah sistem mikroprosesor pada sebuah chip (IC)

Sebagai suatu bahasa pemrograman tingkat tinggi VHDL di gunakan untuk memprogram suatu IC digital PLD (Programmable Logic Device). Dimana IC PLD terdiri atas sejumlah gerbang-gerbang yang dapat diprogram dengan cara memutuskan fuse yang terdapat pada IC tersebut. Seperti bahasa pemrograman yang lain, VHDL memiliki aturan-aturan tersendiri seperti sistematika pemrograman sampai dengan syntax yang digunakan. Teknologi VHDL ini terbagi berdasarkan jumlah gate yang ada, yaitu :

< 500 gerbang SPLD *(Simple Programmable Logic Device)*

500 sampai 5000 gerbang CPLD *(Complex Programmable Logic Device)*

5000 sampai 10.000 gerbang FPGA *(Fast Programmable Gate Array)*

10.000 sampai > 20.000 gerbang ASIC *(Aplication Specific Intregrated Circuit)*

2.1.2. Pemrograman VHDL

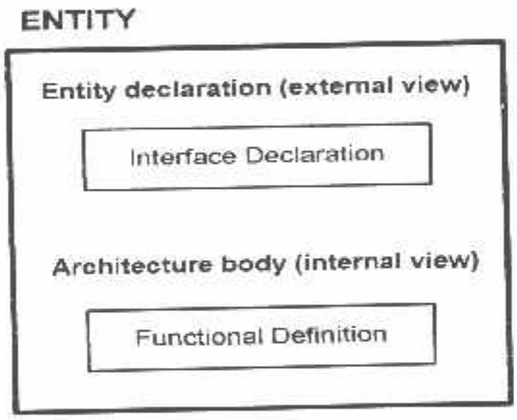
Pemrograman dengan menggunakan bahasa VHDL harus memenuhi kaidah pemrograman yang telah ditetapkan oleh perusahaan yang mengeluarkan Software yang bersangkutan, tetapi pada umumnya mengacu pada standart internasional IEEE.

Dalam pembuatan desain VHDL, bergantung pada alat bantu (tools) yang digunakan, anatar perusahaan satu dengan yang lain berbeda-beda, ada alat bantu yang dapat menghasilkan kode VHDL dari skema rangkaian ada juga yang tidak. Tetapi pada dasarnya, kode VHDL merupakan kode berbasis teks, yang bisa dibuat dengan menggunakan berbagai macam program kata (word processor) seperti notepad, edit, ws, dan ms word.

Azas bangunan dari desain entity VHDL terdiri dari 2 unsur, yaitu :

1. *Entity declaration*
2. *Architecture body*

Desain entity merupakan abstraksi dari suatu desain yang menggambarkan suatu sistem secara lengkap.



Gambar 2-1.

Hubungan Antar Desain Entity dan Architecture Body

Sumber : John f. Wakerly, Digital Design Principles & Practice third edition update, Prentice Hall, New Jersey 07458, hal 269

2.1.3. Entity Declaration

Entity declaration menggambarkan I/O dari desain *entity*. *Entity declaration* analog dengan skematik simbol yang menjelaskan hubungan komponen dalam

suatu desain. Signal I/O di Entity declaration didefinisikan sebagai port yang analog dengan pin dari skematik simbol.

Struktur penulisan *entity declaration* harus mengandung unsur *name* dan *port declaration*, sedangkan *port declaration* menjelaskan nama-nama pin I/O rangkaian digital dari suatu desain. Direction (mode) menjelaskan kondisi I/O dan data type menjelaskan tipe data yang digunakan (sesuai dengan standar IEEE 1076/1164).

Ada 4 macam direction (mode), yaitu ;

IN merupakan *Unidirection* data input (Aliran data berasal dari luar *entity* masuk kedalam *entity*).

OUT merupakan *Unidirection* data output (Aliran data berasal dari dalam *entity* keluar *entity*).

BUFFER merupakan data outptu dengan *internal feedback*. (Digunakan sebagai *port* dan *driver* dengan *architecture*, serupa dengan mode OUT tetapi juga berfungsi sebagai *internal feedback* bukan *Bidirection port*).

INOUT merupakan *Bidirection signal*. (Signal *driver* dapat berasal dari dalam atau luar *entity*, menggunakan mode INOUT ini untuk signal yang benar-benar *Bidirectional*, kalau tidak akan mengurangi kemampuan membaca kode sehingga sulit menentukan sumber signal).

Ada 2 macam Data type yang digunakan berdasarkan standar IEEE, yaitu :

Berdasarkan standar IEEE 1076/93, yaitu : *Boolean, Bit, Bit_vector* dan *Integer.*

Berdasarkan standar IEEE 1164, yaitu *Std Ulogic, std Logic* dan *std_Logic Vector.*

Structure penulisan *Entity Declaration*

```
Entity entity_name is
    Port (
        [signal]{identifier{,identifier}:[mode] signal_type
        [signal]{identifier{,identifier}:[mode] signal_type});
End [Entity][Entity_name];
```

Contoh :

```
Entity adder is port (
        a,b     : in std_logic_vector(3 downto 0);
        cin     : in std_logic;
        sum     : out std_logic_vector(3 downto 0);
        cout    : out std_logic);
end adder;
```

2.1.4. Architecture Body

Architecture Body dalam sebuah *entity* berfungsi untuk mendeskripsikan apa yang akan dilakukan atau proses apa yang akan dikerjakan oleh perangkat keras yang didesain.

Architecture Body berhubungan erat dengan *Entity declaration* didalam desain *entity* VHDL. *Architecture body* menggambarkan fungsi dari *entity* yang sekaligus menjelaskan fungsi dari *entity* . Jika *entity declaration* ditampilkan sebagai kotak hitam yang mana input dan output itu diketahui sedangkan apa yang

ada didalam kotak itu tidak diketahui, maka *architecture body* itu adalah isi dari kotak hitam tersebut.

Sedangkan didalam *architecture body* ada beberapa jenis, anata lain :

1. *Structural description*
2. *Data flow description*
3. *Behavioral description*

Penjelasan dari masing-masing architecture body, yaitu :

Structural description

Perencanaan didasarkan pada pemakaian komponen (*logical gate*) pada library dan hubungan antar componen-componen tersebut (*a set of interconected component*).

Data flow description

Perencanaan berdasarkan pada proses data *transfer* (dari signal atau dari input ke output tanpa statement sequential) yang merupakan sekumpulan dari *concurent assignment statement*. Perbedaan utama antara *data flow* dengan *behavioral* adalah yang satu menggunakan proses yang lain tidak. Penulisan persamaan pada data flow lebih ringkas dan mudah yaitu menggunakan *conditional signal assignment (when-else) statement*. Data flow menggunakan concurent assignment lebih disukai dari pada proses dan sequential statement.

Behavioral description

Perencanaan didasarkan pada proses pengerjaan *statement* antar input dan output secara *sequential*/berurutan/*step by step* dengan menggunakan *statement sequential (a set of sequential statement)*. Keuntungan dari

behavioral description yang merupakan *high level description* adalah kita tidak perlu memfokuskan pada *gate level* pada desain implementasi tetapi kita fokuskan pada usaha mengakuratkan model fungsi. Proses statement dimulai dengan sebuah label yang diikuti dengan tanda ':' kemudian kata 'proses' dan *sensitivity list* dan dibawahnya diikuti dengan *sequential statement*, setelah bagian sequential statement selesai diakhiri dengan *'end process'* dan *label process*.

Yang termasuk *sequential statement*, antara lain :

a. *Process statement*
b. *If-then-else statement*
c. *Case-when statement*
d. *For-loop statement*
e. *While-loop statement*

Struktur penulisan *Architecture Body*

Architecture *architecture name* of *entity name* is

Type_declaration

|signal_declaration

|constan_declaration

|alias_declaration

|subprogram_declaration

begin

{process_statement

|concurent_signal_asignment_statement

|component_instantion_statement

[generate_statement]

End [architecture][*architecture_name*];

2.1.5. Declaration Component

Library adalah suatu tempat *directory* yang dipanggil pada saat kita mengkompile, biasanya menggunakan 2 *library* dalam mendesain yaitu :

- *IEEE library*
- *Work library*

IEEE Library tempat menyimpan desain unit IEEE standar seperti *package std 1164* dan *numeric std*. Dalam perintahnya menggunakan *library clause : library IEEE; Work library* tempat menyimpan desain unit yang kita rancang, setelah kita merancang desain unit dan desain tersebut ingin di gunakan kembali maka kita dapat menempatkannya dalam *library work*, untuk keperluan desain yang lebih besar lagi.

Packages adalah desain unit yang dapat digunakan untuk membuat *type, component, function* dan declarasi lain untuk desaim unit lain. Sebuah *package* terdiri dari sebuah *package declaration* dan *option package body*. Penulisannya adalah : **Use library_name. Package_name.item;**

Package declaration digunakan untuk mendeklarasikan item-item seperti ***Signal, type dan component.***

Signal menyatakan *wire-wire* yang menghubungkan antar komponen, *type* mendefinisikan *state* pada *state machine* dan *component* digunakan untuk memanggil *library component. Entity declaration, Architecture body* dan *package declaration* semuanya merupakan desain unit yang digabung dalam satu *file*.

Karena *Entity declaration* dan *package declaration* merupakan desain unit utama maka dipisah dalam *library* dan *use*.

2.1.6. Concurrent Statement

Concurrent statement merupakan pernyataan yang selalu digunakan dalam architecture dataflow, yang tidak mementingkan urutan pengerjaan. Semua penugasan dalam architecture ini dieksekusi secara bersamaan. Dibawah ini merupakan beberapa perintah jenis concurrent.

1. Boolean Equation

Deskripsi :

relation { **and** relation }

| relation { **or** relation }

| relation { **xor** relation }

| relation { **nand** relation }

| relation { **nor** relation }

Contoh :

```
Architecture boole is
begin
        v <= (a and b and c) or d;
        w <= a or b or c;
        x <= a xor b xor c;
        y <= a nand b nand c;
    z <= a nor b;
end boole;
```

2. **When-else conditional signal statement**

Deskripsi :

{ expression **when** condition **else** } expression;

Contoh :

```
Architecture whenelse is
Begin
x <= '1' when b = c else '0';
y <= j when state = idle else
     k when state = first_state else
     l when state = second state else
     m when others;
end whenelse;
```

2.1.7. Sequential Statement

Berbeda dengan perintah jenis concurrent, perintah jenis ini dikerjakan secara berurutan. Perintah ini selalu digunakan dalam architecture behavioral yang mempunyai pengerjaan yang sama dengan pengerjaan bahasa pemrograman tingkat tinggi. Suatu ciri khas yang dimiliki deskripsi behavioral adalah ***process statement,*** yang diikuti oleh ***sensitivity list.*** Sensitivity list mendefinisikan signal mana yang akan menyebabkan proses dieksekusi. Dibawah ini merupakan beberapa perintah sequential. Kemiripan deskripsi behavioral dengan bahasa pemrograman tingkat tinggi menyebabkan deskripsi behavioral relatif jauh lebih mudah untuk dipahami.

1. **Process Statement**

Deskripsi:

```
[process_label:]
process (sensitivity_list)
        {type_declaration
         constant_declaration
        | variable_declaration
        | alias_declaration}
begin
        {wait_statement
        | signal_assignment_statement
        | variable_assignment_statement
        | if statement
        | case_statement
        | loop_statement
end process [process_label];
```

Contoh:

```
New_process:
process (rst,clk)
        constant  latch:std_logic_vector (7 downto 0) :="00000000";
begin
        wait until clk='1';
```

```
    if (rst='1') then
      q <= latch;
    elsif (en='1') then
      q <= data;
    else
      q <= q;
    end if;
  end new_process;
```

2. if-then-else Statement

Deskripsi:

If condition **then** sequence_of_statements
{**elsif** condition **then** sequence_of_stetement}
[**else** sequence_of_statement]
end if;

Contoh:

```
If (count:="00") then
   a <= b;
elsif (count:="10") then
   a <= c;
else
   a <= d;
end if;
```

3. **case-when Statement**

Deskripsi :

case expression **is**

(**when** identifier | expression | discrete_range | **others=>**

sequence_of_statement}

end case;

Contoh :

Case count **is**

when "00" =>

a <= b;

when "10" =>

a <= c;

when others =>

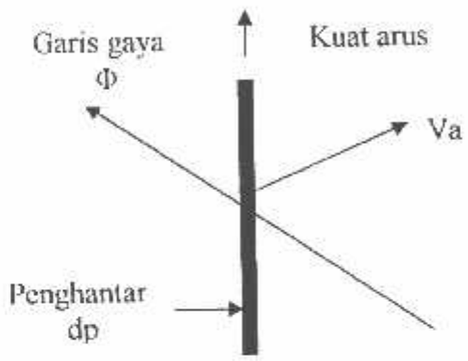
a <= d;

end case;

2.2.Induksi arus listrik dalam sepotong kawat

Apabila sepotong kawat yang ditempatkan (dp) bertemu dengan garis gaya (Φ) dari sebuah kutub utara - selatan. Berdasarkan penjelasan dengan melihat (gambar 2-2) bahwa kuat arus I mengalir dari bawah ke atas dimana bagian kecil dp (departiel 1 panjang) akan terdorong ke arah yang terbalik dari pada arah Va (lihat gambar 2-1).

Aksi gerakan kawat tersebut,akan menimbulkan reaksi yang menentang gerakan aksi itu.



Gambar 2-2

Induksi arus listrik

Sumber : Alciatore, G david. and Histand, B Michael. *Introduction To mechatronics and measurement System*, Mc Graw Hill, New York, 2004.

Reaksi atau gerakan kawat menurut anak panah Va ini akan berupa aliran listrik (tegangan listrik) yang mengalir dari bawah kc atas. Sebab aliran tersebut akan menyebabkan dp bergerak menurut arah yang bertentangan dengan arah panah Va dari gambar di atas.

Tegangan dan aliran yang dibangkitkan dengan gerakan Va,dinamakan dengan tegangan dan arus induksi.

Untuk mengingat hubungan antrara arah Va (gerakan aksi) arah gaya (Φ) dan arah aliran I dapat diingat dengan *kaidah penetapan tangan*.

Kalau jari penunjuk jari tengan tengah dan ibu jari dari tangan kanan ditempatkan siku (90°) satu terhadap yang lainnya, jari penunjuk diarahkan menurut arh fluks (Φ) ibu jari menurut arah gerakan kawat, maka jari tengah akan menunjukan arah tegangan dan arus induksi.

2.3 . Operasional Amplifier (OP-Amp)

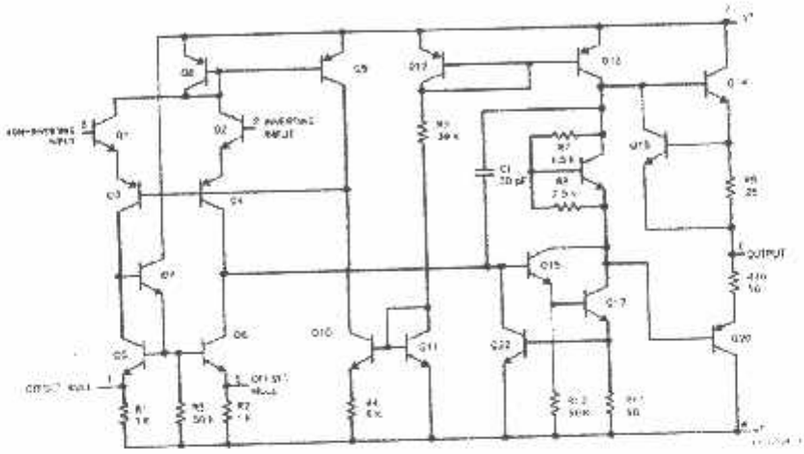
2.3.1. Sekilas Tentang Op-Amp

Operasional amplifier adalah penguat gain tinggi yang dirancang untuk melaksanakan tugas-tugas matematis seperti penjumlahan, pengurangan, perkalian, dan pembagian. Pada saat ini Op-Amp rangkaian terpadu linier dapat bekerja dengan tegangan yang rendah dan dengan hasil yang tidak kalah baiknya dengan pendahulunya. Dengan harga yang relatif murah dan mudah diganti-ganti serta sifatnya yang dapat di andalkan, maka tidak heran kalau setiap tahunya berjuta-juta Op-Amp di gunakan. Dari kelebihan yang dimiliki Op-Amp telah memperluas penggunaan Op-amp sampai jauh melampui kegunaannya saat pertama dirancang.

Pada Op-amp mempunyai lima terminal dasar yang terbagi dalam: dua untuk mensuplay daya, dua untuk isarat masukan, dan satu untuk keluarannya. Bagian dalam dari Op-amp itu sendiri rumit, gambar sekematik dari Op-amp dapat di lihat dalam gambar 2-1. untuk dapat menggunakan Op-amp tidak perlu mengetahui hal apapun tentang cara kerja bagian dalam dari Op-amp, karena Op-

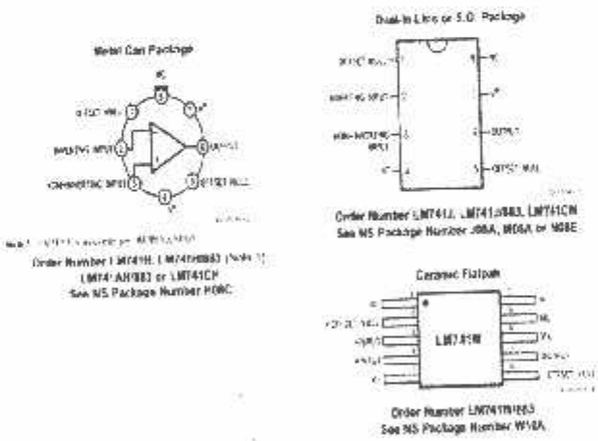
amp telah dirancang sedemikian rupa sehingga komponen luarlah yang akan menentukan keguanaan dari dari Op-amp.

Paket-paket Op-amp dalam bentuk single chip yang umum dan banyak terdapat dipasaran dapat dilihat pada gambar 2-4.



Gambar 2-3

Skematik Op-Amp



Gambar 2-4

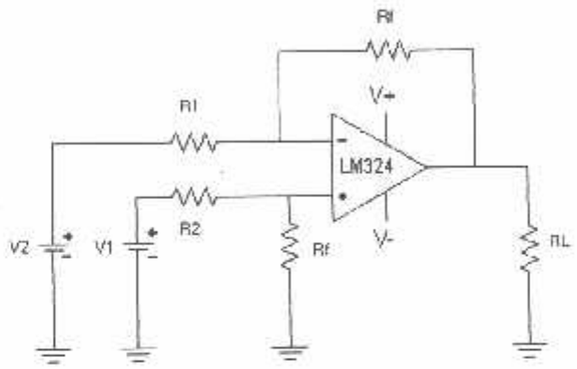
Diagram paket Op-Amp

Sumber : National Semiconductor, LM 741 Operational Amplifier.

National Semiconductor Corporation, 2000

2.3.2. Op-amp sebagai penguat differensial dasar

Dalam hal ini transduser merupakan alat yang merubah perubahan arus listrik menjadi tegangan. Sifat penguat ini memungkinkan suatu sinyal kecil di ambil dari sinyal yang lebih besar dengan rangkaian yang di tunjukan pada gambar 2.3. sinyal yang kecil merupakan masukan diferensial dan keluaranya berupa tegangan masukan diferensial yang di perkuat



Gambar 2-5

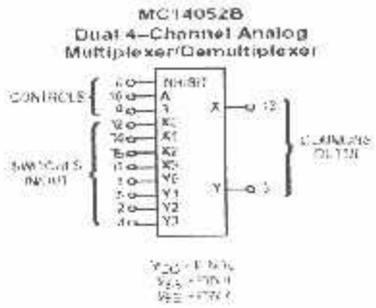
Rangkaian Penguat Differensial Dasar

Sumber: Robert F. Coughlin, Frederick F. Driscll, Herman Widodo Sumito, Penguat Operasional dan Rangkaian Terpadu Linear edisi 2, Erlangga, hal 173-175

2.4. Multiplekser

2.4.1. Multiplekser Analog

Multiplekser merupakan suatu saklar yang dapat digunakan untuk memilih data masukan yang mana yang akan dikeluarkan. Pemilihan tersebut dapat dilakukan dengan memberikan data biner pada pin control. Pada multiplekser type MC 14052B terdapat dua macam input dan dua macam output yaitu X dan Y. Input X terdiri dari X0-X3 dan output nya X. Input Y terdiri dari Y0-Y3 dan output Y.



Gambar 2-6

Analog multiplekser MC 14052B

Sumber : Motorola datasheet

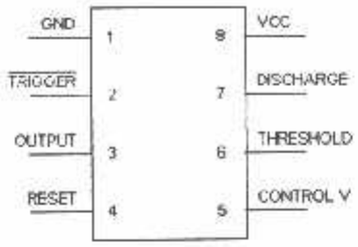
Multiplekser dalam perencanaan dan pembuatan alat ini digunakan multi plekser analog buatan Motorola semiconductor MC14052B. Multi plekser ini membutuhkan tegangan supply antara 3 volt sampai dengan 18 volt. Tegangan analog yang diberikan pada masukan maksimal adalah +0.5 volt dari tegangan supply yang diukur dari VEE.

2.5. Pewaktu IC 555

2.5.1. Pewaktu IC 555 sebagai multivibrator Astabil

Pewaktu ic 555 mempunyai dua cara kerja, sebagai multivibrator astabil dan multivibrator monostabil. Cara kerja astabil (bergerak bebas) dari ic 555 adalah sebagai berikut, tegangan keluaran beralih dari high ke low dan kembali lagi. Waktu high atau low ditentukan oleh sebuah jaringan kapasitor dan resistor yang dihubungkan pada kaki-kaki luar ic. Cara kerja monostabil (satu tembakan) tegangan keluarannya low sampai sebuah pulsa pemicu yang negatif diberikan pada pewaktu tersebut, kemudian keluarannya kembali high. Waktu high atau low

ditentukan oleh sebuah jaringan kapasitor dan resistor yang dihubungkan pada kaki-kaki luar ic.



Gambar 2.7

Pewaktu Ic 555

Sumber : Couglin, F Robert and Driscoll, F Frederick, *Penguat Operasional dan Rangkaian Terpadu linier,* Erlangga, Jakarta, 1992

Frekuensi osilasi dari ic 555 ini dapat dihitung dengan mnggunakan rumus sebagai berikut :

$$T\ high=0.695\ (RA+RB)*C$$

$$T\ low=0.695*\ RB*C$$

Jadi perioda osilasi total T adalah :

$$T = t\ high + t\ low$$

$$= 0.695(RA + 2RB)C$$

Frekuensi osilasi bergerak bebas *f* adalah:

$$f = 1/T$$

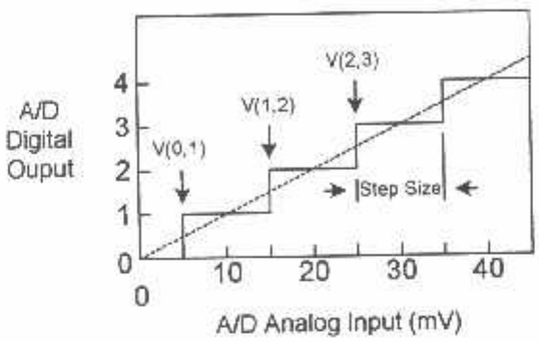
$$= 1.44 / (RA + 2RB)C$$

2.6. Analog to Digital converter

2.6.1 Prinsip dasar ADC

Analog-to-digital (A/D) converter merubah tegangan analog menjadi kode biner (digital Output). Biasanya hubungan antara input analog dengan output digital adalah linear. A/d Converter membag.i tegangan input menjadi $2^N - 1$, dimana N adalah banyaknya bit pada keluaran A/D converter. Beberapa A/D

converter memerlukan tegangan inputan yang tetap sebelum melakukan proses konversi, yang mana dilakukan dalam beberapa mikrodetik. Gambar berikut menunjukan kurva respon A/D converter terhadap inputan analog untuk V_{ref}=0 v



Gambar 2-8

Respon Ideal A/D *Converter* terhadap

Variasi Tegangan Input Analog

untuk A/D converter yang ideal, digtal output n adalah fungsi linear dari analog inputnya V diantara dua voltage referensi V^-_{ref} dan V^+_{ref}. Ring analog input dari V^-_{ref} dan V^+_{ref} dibagi menjadi 2^N-1 menyamai lebar ΔV yang mana

$$\Delta V = \frac{V^+_{ref} - V^-_{ref}}{2^N - 1}$$

Kurva respon yang ideal adalah yang menyentuh bagian tengah dari setiap step Karena keluaran yang sama di hasilkan dari ring analog input, kurva respon yang paling baik,teratur dari perubahan tegangan, yang mana keluarannya berubah per bit. Bagian tengah dari setiap step dapat diperhitungkan sebagi titik tengah antara yang mendekati perubahan voltage. Pada kenaikan yang baik, perubahan tegangan yang pertama V(0,1) terjadi pada 0,5 LSB,dan yang kedua V(1,2) terjadi pada 1,5 LSB. Perubahan tegangan yang ke n adalah:

$V(n-1,n)=V_{ref}+(n-0,5)*\Delta V$. Sementara nilai n di samakan untuk ring Tegangan yang memiliki lebar ΔV,perubahan tegangan antara n-1 dan n disamakan sebagai nilai V. Linieritas ditentukan oleh bagaimana perubahan tegangan pada suatu garis lurus, deferensial linieritas ditentukan persamaan ukuran dari setiap kenaikan.

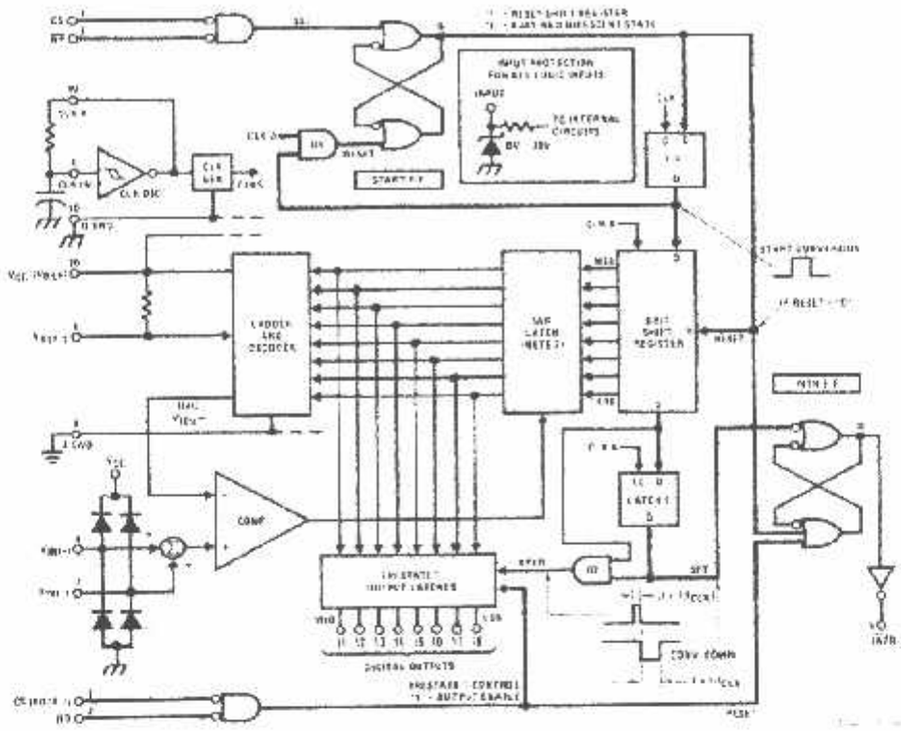
2.6.2 ADC 0804

ADC 0804 merupakan A/D Converter buatan National Semiconductor, A/D converter ini memiliki inputan defferensial dan output 8 bit. A/D ini sering sekali di gunakan pada instrumentasi yang membutuhkan data digital dari suatu inputan analog. A/D converter ini memiliki beberapa kelebihan diantaranya adalah[9]:

- Mudah untuk menginterfacekan dengan mikroprosesor atau bekerja sendiri.
- Bekerja dengan 2.5V tegangan reverensi.
- Tegangan input analog 0 sampai 5 V dengan single tegangan
- Dikemas dalam bentuk single chip DIP 20 pin sehingga bentuknya kecil.

Pada dasarnya Prinsip kerja dari A/D ini sama dengan A/D converter tipe yang lain yaitu mencacah inputan analog yang masuk menjadi outputan digital. ADC 0804 memilki 8 bit, berarti A/D ini memiliki 2^N kombinasi atau $2^8 = 256$ kombinasi untuk mencari tegangan yang diwakili tiap bitnya adalah:

$V_{bit}=\frac{V_{hr\,max}-V_{hr\,min}}{2^N}-\frac{5-0}{2^8}=\frac{5}{256}=0.01953125\cong 0.02V$ atau 20 mV. Gambar diagram blok dari ADC 0804 ini dapat dilihat pada gambar 2-9. Untuk dapat menggunakan ADC 0804 tidak perlu mempelajari secara detail tentang fungsi dari masing-masing blok.



Gambar 2-9

Diagram Blok ADC 0804

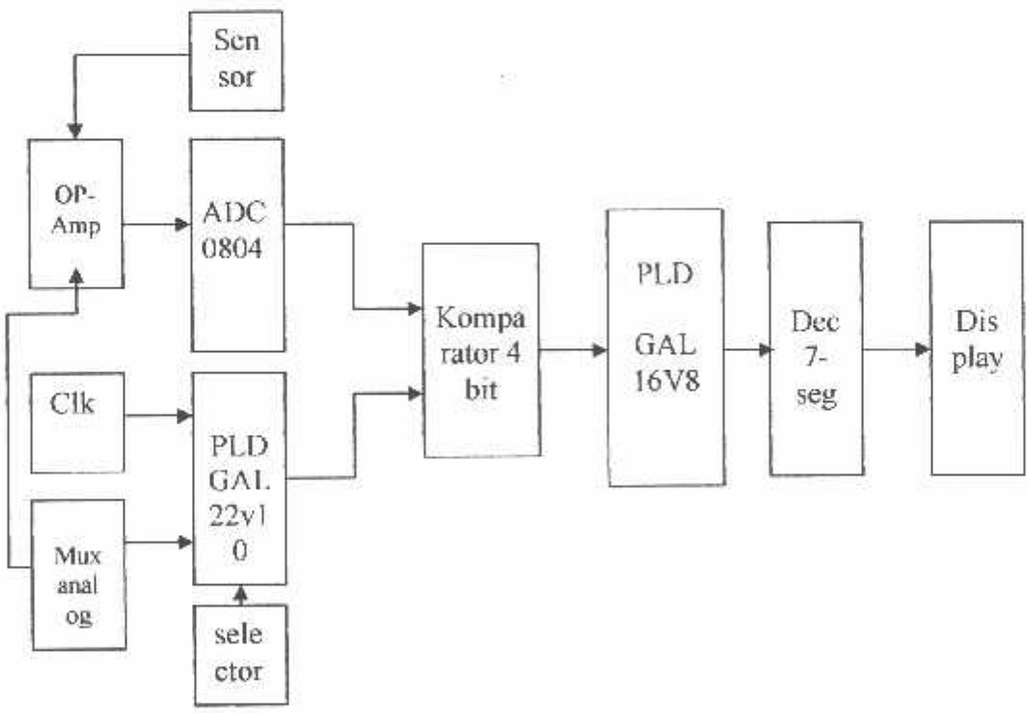
Sumber : National semiconductor. ADC 0801/ADC0802/ADC0803/

ADC0804/ADC0805 8-bit μP Compatible A/D Converters

BAB III
PERENCANAAN DAN PEMBUATAN ALAT

3.1. Pendahuluan

pada bab ini akan dibahas mengenai perancangan dan pembuatan alat pengukur arus listrik menggunakan sitem induksi (tang ampere meter). Pada perancangan dan pembuatan alat dibagi menjadi dua tahap yaitu perancangan perangkat keras (hardware) dan perancangan perangkat lunak (software). Perancangan perangkat keras meliputi pembuatan sensor dan koneksi pada pin-pin IC PLD, untuk perancangan software adalah pembuatan tampilan angka dari perubahan arus listrik ke seven-segment display.



Gambar 3-1

Diagram Blok Perencanaan Alat

Sumber : Perancangan

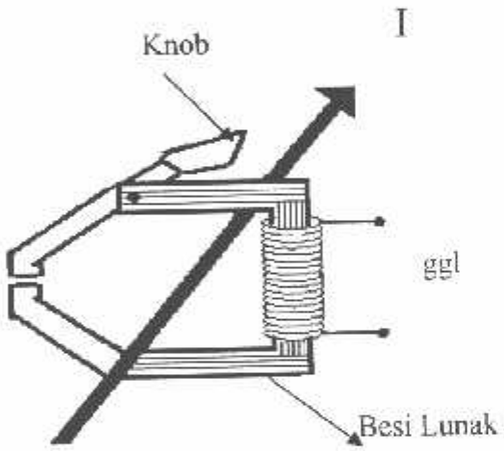
3.2.Perancangan Alat

Perancangan alat dibagi menjadi dua tahap perancangan yaitu: Perancangan perangkat keras dan Perancangan perangkat lunak.

3.2.1. Perancangan Perangkat Keras

3.2.1.1. Transducer Induksi Arus

Untuk mengetahui adanya arus yang lewat pada suatu penghantar maka di gunakan transducer induktif yang berupa lilitan kawat pada sebuah inti besi. Jika pada suatu gulungan kawat di lalui oleh arus listrik maka dalam kawat tersebut akan timbul ggl sesuai dengan jumlah lilitannya.

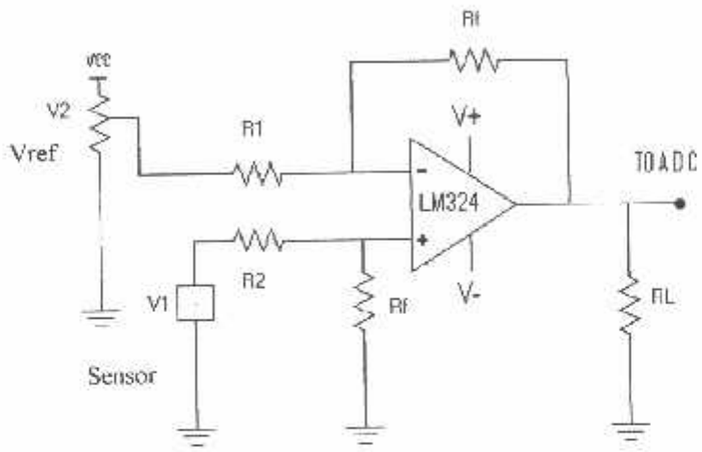


Gambar 3-2.
Lilitan yang dilalui arus listrik
Sumber : Perancangan

Tegangan yang timbul dari kawat inilah yang nantinya akan dibaca pada ADC dan di konversikan ke bilangan biner. Tegangan yang keluar dari lilitan tidak boleh melebihi 5 volt, karena tegangan ini yang nantinya menjadi batas maksimal tegangan input untuki ADC.

3.2.1.2. Rangkaian Penguat Differensial

Keluaran dari penguat buffer nilai tegangan minimumnya 0V dan nilai tegangan maksimumnya 5 V maka diperlukan penguatan berbeda-beda tiap rangenya agar nilai V_{out} = 5. Keluaran penguat tersebut kemudian dijadikan sebagai inputan untuk ADC. Gambar rangkaian penguat non inverting adalah sebagai berikut :



Gambar 3–3

Rangkaian Penguat Differensial Dasar

Sumber : Perancangan

Keluaran penguat differensial dasar tersebut kemudian dijadikan sebagai inputan untuk ADC. Tegangan keluaran Vo tergantung pada perbedaan tegangan antara kedua terminal inverting dan non inverting.

Tegangan keluarn dari sensor masih sangat lemah yaitu berkisar 10 mvolt pada arus listrik 0,13 amper. Maka tegangan keluaran ini harus di kuatkan. Penguatan nya dapat dicari dengan rumus sebagai berikut :

$$Vout = Vd \,.\, Av$$

$$Vd = V1\text{-}V2$$

$$AV = RF/R1$$

Dimana :

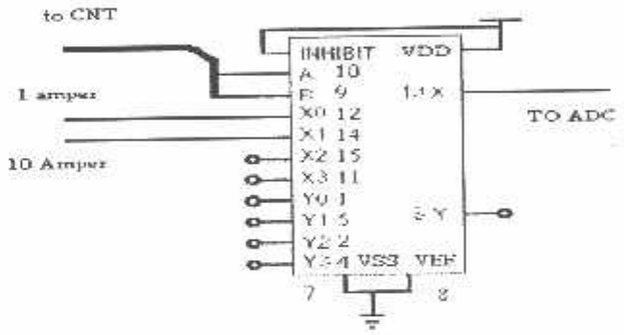
Vout – Tegangan keluaran dari penguat differensial

Vd = Perbedaan tegangan antara v2 dengan V1

AV =Faktor penguatan yang dibutuhkan

3.2.1.3. Rangkaian Multiplekser Analog

Ketelitian pengukuran dapat dilakukan dengan cara mengubah range selector. Range selector terdiri dari keypad yang di inputkan ke IC PLD, kemudian data inputan akan diolah dan dikeluarkan ke multiplekser analog untuk memilih range pengukuran yang di inginkan.



Gambar 3-4

Multiplekser Analog

Sumber :Perancangan

3.2.1.4. Rangkaian Clock

Rangkaian clock diperlukan untuk mengaktifkan sistem yang dirangkai. Pembangkitan clock digunakan mulvibrator astabil menggunakn IC NE 555. Kecepatan clock yang digunakan dalam perancangan alat ini kecepatan frekuensi yang digunakan adalah 1.075Khz.

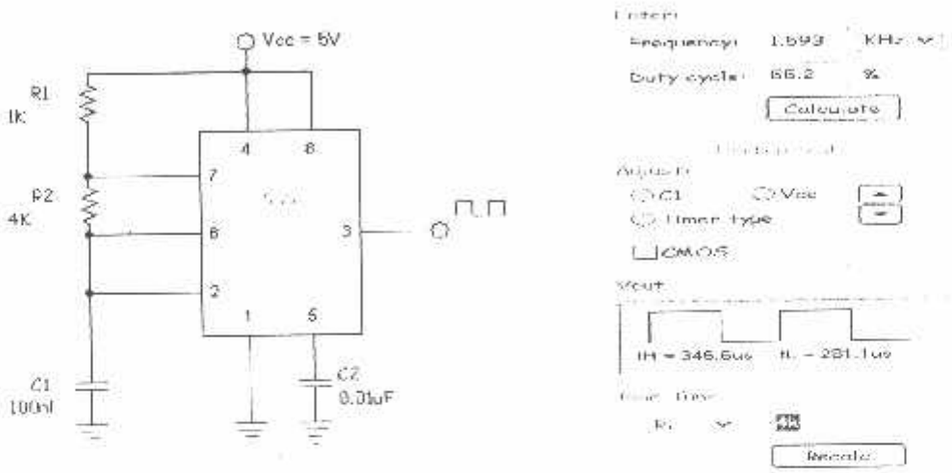
T high = 0.695(1k+4k)(0.1uF) =346.6us

T high = 0.695(4k*0.1uF) =281.1us

Jadi frekuensi osilasi *f* adalah :

f = 1.44/ 1k +2*40k*0.1uF =1.593Khz

Hitungan diatas dapat dicek dengan menggunakan software 555 Timer Pro, seperti terlihat pada gambar diwah ini.



Gambar 3.5

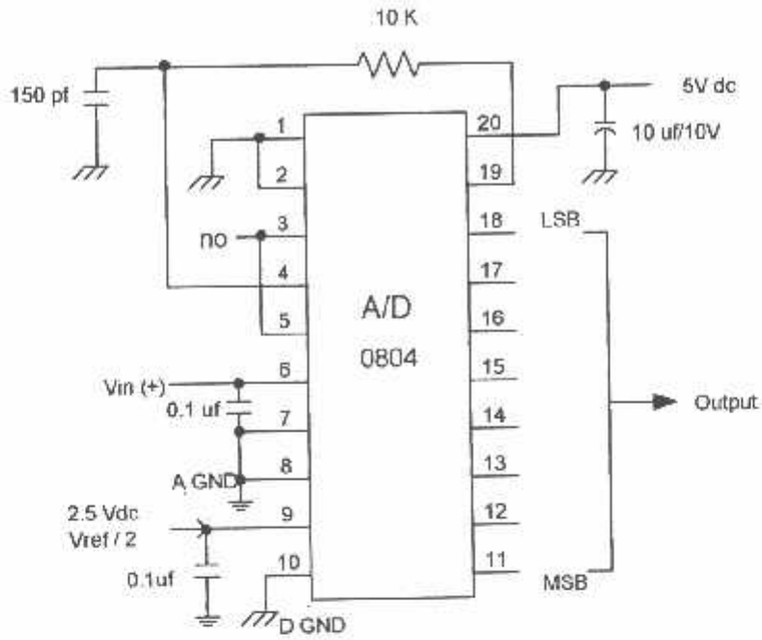
Rangkaian Pewaktu 555

Sumber : Perancangan

Dari gambar diatas terlihat bahwa penghitungan menggunakan persamaan hasilnya mendekati sama dengan hasil pengecekan dengan software 555 timer pro.

3.2.1.5. Rangkaian A/D Converter

Agar perubahan dari tegangan analog menjadi suatu angka biner maka diperlukan suatu rangkaian pengubah yaitu rangkaian A/D Converter. A/D Converter di sini akan mengubah tegangan analog menjadi angka biner delapan bit.



Gambar 3-6

Rangkaian A/D Converter 0804

Sumber : Perancangan

A/D Conventer yang digunakan adalah ADC 0804 buatan national semiconductor yang mana ADC inputan analog yang masuk di ubah menjadi outputan biner 8 bit. Rangkaian dari A/D converter seperti gambar 3-6 di atas. Sebagai Vcc adalah tegangan 5V stabil yang dihubungkan dengan pin 20 pada chip. Pemasangan kapasitor pada pin 20 terhadap ground berfungsi sebagai filter yang besarnya sekitar 1 μf. Tegangan inputan untuk pin 9 pada chip besarnya 2.50V atau V_{ref} / 2. Untuk mendapatkan clock maka pin 19 dan pin 4 dihubungkan dengan resistor dan capasitor terhadap ground yang mana frekuensi clock dapat di hitung dengan rumus:

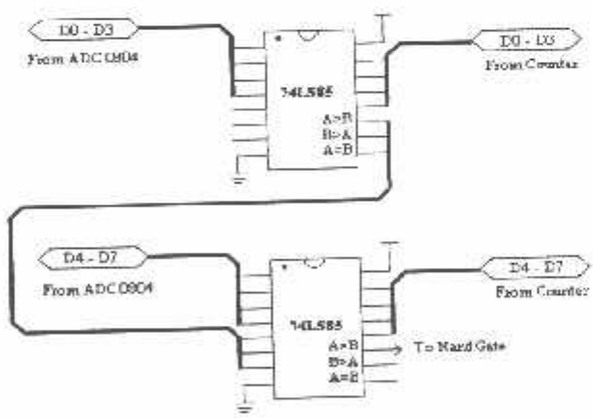
$$f_{clk} = \frac{1}{1.1RC}$$

Pada rangkaian diatas R terpasang besarnya adalah 10KΩ dan kapasitor besarnya 150 pF. $V_{IN(-)}$ dihubungkan ke ground $V_{IN(-)}$ sebagai inputan analog. Untuk mendapatkan konversi yang terus menerus sesuai perubahan input maka pin 3 WR dan pin 5 INTR pada chip di hubungkan, pada pin 1 CS dan 2 RD dihubungkan ke ground.

3.2.1.6. Komparator 4 bit 74 LS 85

Untuk menghentikan clock yang yang akan melewati gerbang AND, maka diperlukan komparator 4 bit yang disusun secara cascade, dengan tujuan agar dapat diperolch komparator 8 bit.

Komparator ini yang nantinya akan membandingkan data biner keluaran dari ADC dengan data biner keluaran dari IC GAL 22v10. Jika data biner yang berasal dari ADC lebih besar dari nilai biner yang berasal dari IC GAL 22v10 maka, pada pin 5 yaitu a>b akan bernilai high ('1'). Jika nilai biner dari ADC dan IC GAL 22v10 sudah sama maka pin 5 akan kembali kekondisi low ('0').



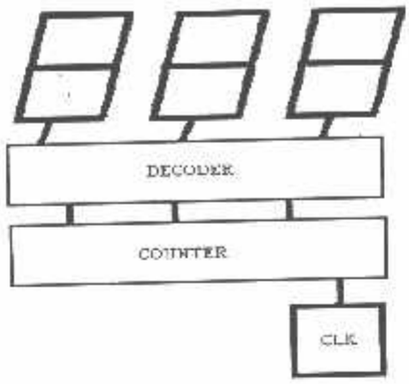
Gambar 3-7

Rangkaian Komparator 74LS85

Sumber : Perancangan

3.2.1.7. Perancangan Unit Display

Berikut ini adalah diagram blok dari rangkaian unit display



Gambar 3-8

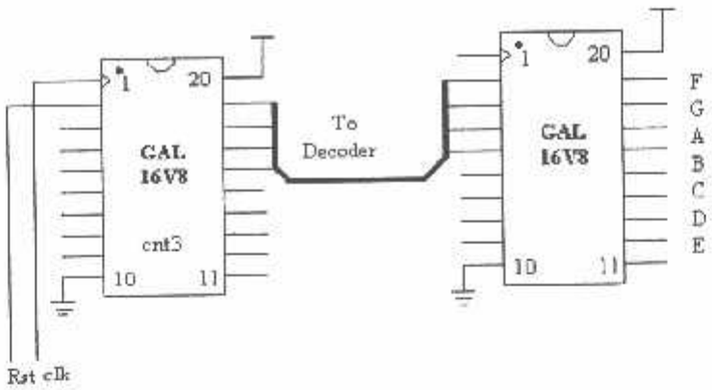
Blok diagram unit display

Sumber : Perancangan

Dari digram blok diatas nampak bahwa penampil 7-segment yang dipakai adalah 4 buah atau sama dengan digit mulai dari 0.00 s/d 10.0. dimana setiap 7-segment akan didrive oleh sebuah IC GAL16v8. Sinyal reset dan clock akan dihubungkan dengan rangkaian pemroses. Jika sinyal rest diaktifkan maka akan tampil tulisan Hal ini menandakan bahwa alat ukur sudah siap dipakai.

3.2.1.7.1. Perancangan Rangkaian Display D1

Rancangan rangkaian ini memiliki dua kondisi yaitu kondisi untuk membentuk huruf 'R' dan '0-9'. Setiap output dari a – g dihubungkan ke 7 segment agar dapat membentuk tampilan yang dinginkan. Rancangan ini nantinya akan dimplementasikan pada IC GAL16v8 dengan menggunakn bahasa penrograman VHDL dengan metode penulisan script menggunakan HDL editor.



Gambar 3-9

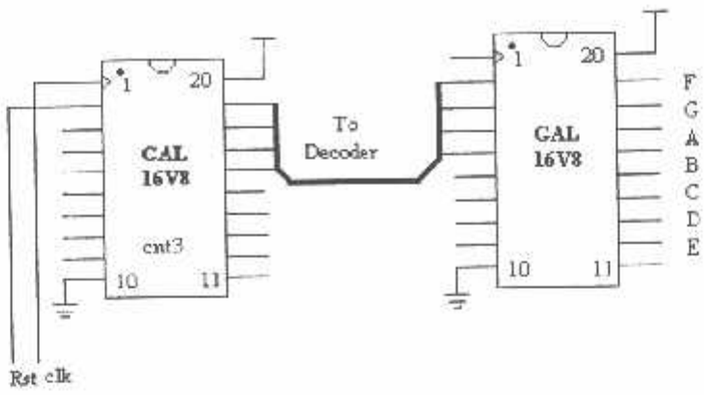
Rangkaian Unit Display D1

Sumber : Perancangan

Pada rangkaian diatas terlihat bahwa kondisi input diambil dari counter 4 bit. Clock diperoleh dari IC NE 555 yang difungsikan sebagai multivibrator astabil. Kaki yang dipakai untuk counter 4 bit ini adalah pin 1 dipakai untuk clock, pin 2 dipakai untuk reset. Untuk kaki keluaran yang dipakai adalah pin 19, pin 18, pin 17, pin 16. Kaki yang dipakai untuk input decoder adalah pin 2, pin 3, pin 4, pin 5. Kaki yang dipakai untuk output adalah pin 19, pin 18, pin 17, pin 16, pin15, pin 14, pin 13. Jika data masukan selain yang ditentukan, maka akan membentuk karakter 'R' jadi pada saat pertama kali dinyalakan, pada pin data diberikan data masukan selain data yang ditentukan yaitu 1011-111.

3.2.1.7.2.Perancangan rangkaian display D2

Rancangan rangkaian ini memiliki dua kondisi yaitu kondisi untuk membentuk huruf 'D' dan '0-9'. Setiap output dari a – g dihubungkan ke 7 segment agar dapat membentuk tampilan yang dinginkan. Rancangan ini nantinya akan dimplementasikan pada IC GAL16v8 dengan menggunakn bahasa penrograman VHDL dengan metode penulisan script menggunakan HDL editor.



Gambar 3-10

Rangkaian Unit Display D2

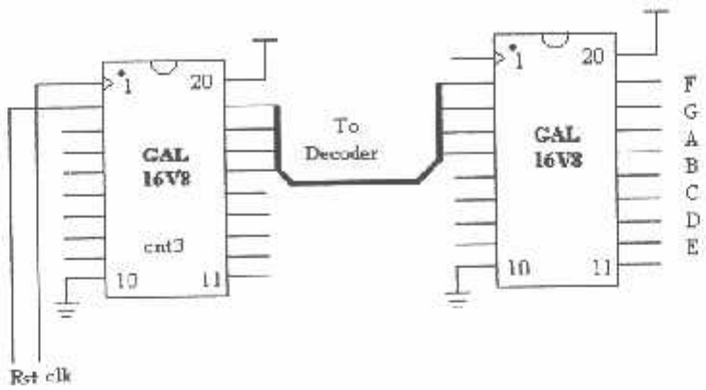
Sumber : Perancangan

Pada rangkaian diatas terlihat bahwa kondisi input diambil dari counter 4 bit. Clock diperoleh dari IC NE 555 yang difungsikan sebagai multivibrator astabil. Kaki yang dipakai untuk counter 4 bit ini adalah pin 1 dipakai untuk clock, pin 2 dipakai untuk reset. Untuk kaki keluaran yang dipakai adalah pin 19, pin 18, pin 17, pin 16. Kaki yang dipakai untuk input decoder adalah pin 2, pin 3, pin 4, pin 5. Kaki yang dipakai untuk output adalah pin 19, pin 18, pin 17, pin 16, pin15, pin 14, pin 13. Jika data masukan selain yang ditentukan, maka akan membentuk karakter 'D' jadi pada saat pertama kali dinyalakan, pada pin data diberikan data masukan selain data yang ditentukan yaitu 1011-111.

3.2.1.7.3. Perancangan Rangkaian Display D3

Rancangan rangkaian ini memiliki dua kondisi yaitu kondisi untuk membentuk huruf 'Y' dan '0-9'. Setiap output dari a – g dihubungkan ke 7 segment agar dapat membentuk tampilan yang dinginkan. Rancangan ini nantinya

akan dimplementasikan pada IC GAL16v8 dengan menggunakn bahasa pemrograman VHDL dengan metode penulisan script menggunakan HDL editor.



Gambar 3-11

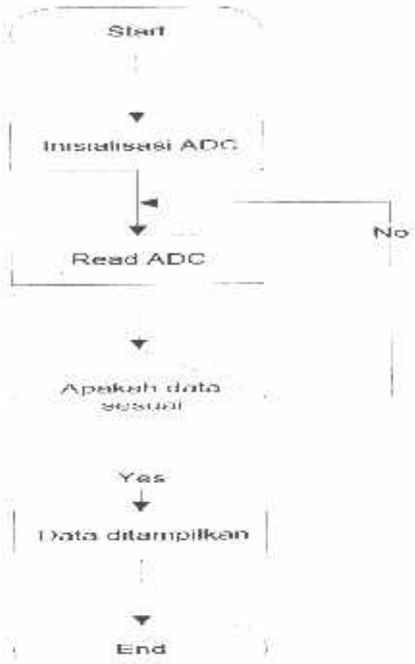
Rangkaian Unit Display D3

Sumber : Perancangan

Pada rangkaian diatas terlihat bahwa kondisi input diambil dari counter 4 bit. Clock diperoleh dari IC NE 555 yang difungsikan sebagai multivibrator astabil. Kaki yang dipakai untuk counter 4 bit ini adalah pin 1 dipakai untuk clock, pin 2 dipakai untuk reset. Untuk kaki keluaran yang dipakai adalah pin 19, pin 18, pin 17, pin 16. Kaki yang dipakai untuk input decoder adalah pin 2, pin 3, pin 4, pin 5. Kaki yang dipakai untuk output adalah pin 19, pin 18, pin 17, pin 16, pin15, pin 14, pin 13. Jika data masukan selain yang ditentukan, maka akan membentuk karakter 'R' jadi pada saat pertama kali dinyalakan, pada pin data diberikan data masukan selain data yang ditentukan yaitu 1011-111.

3.2.2 Perancangan Perangkat Lunak

Untuk perancangan perangkat lunak (software) menggunakan Warp 5.2. dengan bahasa pemrograman type behavioral dan arithmatic dimana tipe ini lebih efisien dalam mengoptimalkan fungsi dari sistem dengan mempelajari pengaruh input terhadap output. Diangam alir dari sistem adalah sebagai berikut:



Gambar 3-12

Diagram Alir untuk Tampilan

Sumber : Perancangan

Pada saat sistem dinyalakan sistem akan mendeteksi pada pin mana terdapat inputan dari ADC. Kemudian sistem akan membaca inputan yang diberikan oleh ADC dan memprosesnya untuk di tampilkan. Apabila data tidak tersedia maka sistem akan membaca kembali inputan ADC. Proses ini akan berlangsung terus menerus sehingga akan terjadi sebuah siklus. Setiap perubahan output ADC akan di baca kemudian akan ditampilkan.

3.2.2.1. Perancangan Perangkat Lunak Untuk D1

Rancangan software ini memiliki dua kondisi yaitu kondisi untuk membentuk huruf 'R' dan '0-9'. Setiap output dari a – g dihubungkan ke 7 segment agar dapat membentuk tampilan yang dinginkan. Rancangan ini nantinya akan dimplementasikan pada IC PALCE16v8 dengan menggunakn bahasa penrograman VHDL dengan metode penulisan script menggunakan HDL editor sebagai berikut :

```
library ieee;
use ieee.std_logic_1164.all;
entity decoder_R is
      port ( data: in std_logic_vector(3 downto 0);
             display: out std_logic_vector(7 downto 0));
Attribute Part_Name of DECODER_R: Entity is "16v8";
Attribute Pin_numbers of DECODER_R: Entity is
"data(3):6 data(2):2 data(1):3 data(0):7 "
&"display(7):19 display(6):18 display(5):17 "
&"display(4):16 display(3):15 display(2):14 "
&"display(1):13 display(0):12";
end DECODER_R;

architecture rtl of DECODER_R is

begin
 encode: process (data) begin
    case data is
    when "0000" =>display <= "01000000";
    when "0001" =>display <= "11100110";
    when "0010" =>display <= "10001000";
    when "0011" =>display <= "10000010";
    when "0100" =>display <= "00100110";
    when "0101" =>display <= "00010010";
    when "0110" =>display <= "00010000";
    when "0111" =>display <= "11000110";
    when "1000" =>display <= "00000000";
    when "1001" =>display <= "00000010";
    when "1010" =>display <= "01000001";
    when others =>display <= "01011101";--R
    end case;
   end process;
end rtl;
```

3.2.2.2. Perancangan Perangkat Lunak Untuk D2

Rancangan software ini memiliki dua kondisi yaitu kondisi untuk membentuk huruf 'D' dan '0-9'. Setiap output dari a – g dihubungkan ke 7 segment agar dapat membentuk tampilan yang dinginkan. Rancangan ini nantinya akan dimplementasikan pada IC PALCE16v8 dengan menggunakan bahasa penrograman VHDL dengan metode penulisan script menggunakan HDL editor sebagai berikut:

```
library ieee;
use ieee.std_logic_1164.all;
entity decoder_D is
      port ( data: in std_logic_vector(3 downto 0);
            display: out std_logic_vector(7 downto 0));
Attribute Part_Name of decoder_D: Entity is "16v8";
Attribute Pin_numbers of decoder_D: Entity is
"data(3):6 data(2):2 data(1):3 data(0):7 "
&"display(7):19 display(6):18 display(5):17 "
&"display(4):16 display(3):15 display(2):14 "
&"display(1):13 display(0):12";
end decoder_D;

architecture rtl of decoder_D is
begin
 encode: process (data) begin
  case data is
   when "0000" => display <= "01000000";
   when "0001" => display <= "11100110";
   when "0010" => display <= "10001000";
   when "0011" => display <= "10000010";
   when "0100" => display <= "00100110";
   when "0101" => display <= "00010010";
   when "0110" => display <= "00010000";
   when "0111" => display <= "11000110";
   when "1000" => display <= "00000000";
   when "1001" => display <= "00000010";
   when "1010" => display <= "01000001";
   when others => display <= "10100001";--D
   end case;
  end process;
end rtl;
```

3.2.2.3. Perancangan Perangkat Lunak Untuk D3

Rancangan software ini memiliki dua kondisi yaitu kondisi untuk membentuk huruf 'Y' dan '0-9'. Setiap output dari a – g dihubungkan ke 7 segment agar dapat membentuk tampilan yang dinginkan. Rancangan ini nantinya akan dimplementasikan pada IC PALCE16v8 dengan menggunakn bahasa pemrograman VHDL dengan metode penulisan script menggunakan HDL editor sebagai berikut :

```
library ieee;
use ieee.std_logic_1164.all;
entity decoder_y is
    port (data: in std_logic_vector(3 downto 0);
        display: out std_logic_vector(7 downto 0));
Attribute Part_Name of decoder_y: Entity is "16v8";
Attribute Pin_numbers of decoder_y: Entity is
"data(3):6 data(2):2 data(1):3 data(0):7 "
&"display(7):19 display(6):18 display(5):17 "
&"display(4):16 display(3):15 display(2):14 "
&"display(1):13 display(0):12";
end decoder_y;
architecture rtl of decoder_y is
begin
 encode: process (data) begin
  case data is
      when "0000" => display <= "01000000";
      when "0001" => display <= "11100110";
      when "0010" => display <= "10001000";
      when "0011" => display <= "10000010";
      when "0100" => display <= "00100110";
      when "0101" => display <= "00010010";
      when "0110" => display <= "00010000";
      when "0111" => display <= "11000110";
      when "1000" => display <= "00000000";
      when "1001" => display <= "00000010";
      when "1010" =>display <= "01000001";
      when others => display <= "00100011";--Y
      end case;
     end process;
 end rtl;
```

BAB IV

PENGUJIAN ALAT

4.1. Pendahuluan

Setelah melakukan perancangan alat dan pembuatan berdasarkan blok-blok dari sistem, maka dilakukan pengujian terhadap system tersebut apakah sitem rangkaian yang sudah dirangkai sudah sesuai dengan rancangan atau belum

- pengujian perangkat sensor
- pengujian op-amp
- pengujian clock 555
- pengujian multiplekser
- pengujian ADC
- pengujian IC GAL 16v8 dan GAL 22v10
- pengujian komparator 74ls85

Sedangkan alat-alat yang digunakan dalam pengujian ini adalah :

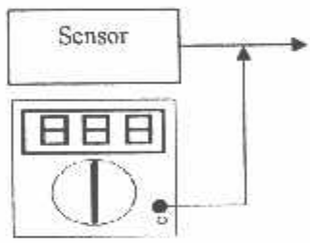
- Multimeter analog dan digital
- Logic probe
- Bar Led
- Binary (DIP) switch
- Komputer

4.2. Pengujian Perangkat Sensor

Pengujian perangkat sensor terdiri atas 2 bagian, yaitu pengujian rangkaian sensor dan pengujian op-amp. Pengujian rangkaian sensor bertujuan untuk menentukan jarak yang tepat antara sensor dengan kawat yang diukur arus listrik nya. Sedangkan pengujian op-amp bertujuan untuk melihat apakah rangkaian penguat berfungsi dengan baik atau tidak.

4.2.1. Pengujian sensor

Pengujian rangkaian sensor dilakukan dengan mengubah-ubah arus yang mengalir pada kawat yang diukur dengan cara merubah dayanya.



Gambar 4-1

Digram blok pengujian sensor

Hasil pengukuran sensor diatas diperlihatkan pada table 4-1.

No	P beban (Watt)	V beban (Volt)	I beban (Amper)	Vout Sensor (mVolt)
1	25	220	0.11	4.9
2	40	220	0.18	9.1
3	60	220	0.27	14.1
4	65	220	0.29	14.5
5	85	220	0.38	19.9
6	100	220	0.45	24.6
7	125	220	0.56	30.7

Tabel 4-1.

Pengukuran Tegangan Terhadap

Perubahan Arus Listrik

Tabel 4-1 memperlihatkan bahwa besar tagangan keluaran sensor linier terhadap perubahan beban listrik yang diukur arusnya.

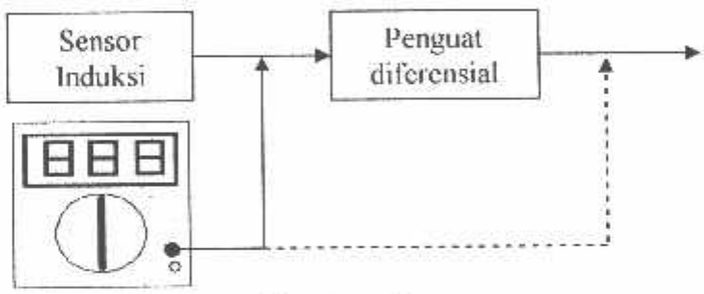
Gambar 4.2

Photo hasil pengukuran sensor

Sumber : pengujian

4.2.2. Pengujian Penguat differensial

Peranan unit rangkaian penguat sangat penting untuk memperkuat sinyal syarat yang kecil. Penguatan yang dibutuhkan adalah 39.6 kali.



Gambar 4-3

Digram blok pengujian sensor

Hasil perhitungan diperlihatkan pada table dibawah ini :

No	Vout Sensor (mVolt)	Penguatan (Av)	Vout opamp (mvolt)
1	4 9	39.6	193.99
2	9.1	39.6	350.27
3	14.1	39.6	520.22
4	14.5	39.6	568.06
5	19.9	39.6	742.84
6	24.6	39.6	970.92
7	30.7	39.6	1215.4

Tabel 4-2

Perhitungan Tegangan Terhadap

Perubahan Arus Listrik

Dari table 4-2 diatas memperlihatkan bahwa keluaran tegangan dari sensor dikuatkan sebesar 39.6 kali.

Hasil pengukuran diperlihatkan pada table dibawah ini :

No	Vout Sensor (mVolt)	Penguatan (Av)	Vout opamp (mvolt)
1	4.9	39.6	210
2	9.1	39.6	350
3	14.1	39.6	520
4	14.5	39.6	560
5	19.9	39.6	740
6	24.6	39.6	880
7	30.7	39.6	1060

Tabel 4-3

Pengukuran Tegangan Terhadap

Perubahan Arus Listrik

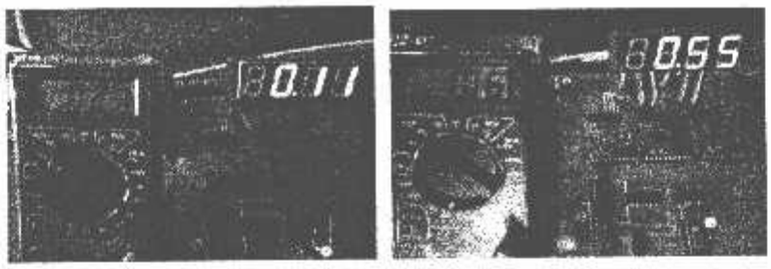
Dari hasil pengukuran terdapat perbedaan dengan hasil perhitungan, maka prosentase kesalahan dapat dicari dengan rumus sebagai berikut:

$$\% \text{ kesalahan} = \frac{\textit{Hasil Perhitungan} - \textit{Hasil Pengukuran}}{\textit{Hasil Perhitungan}} \text{ X } 100\%$$

Dari hasil pengujian dan pengukuran di atas maka didapat prosentase kesalahan sebagai berikut :

$$\% \text{ Kesalahan} = \frac{4.56 - 4.52}{4.56} \text{ X } 100\%$$

$$= 0{,}90\ \%$$



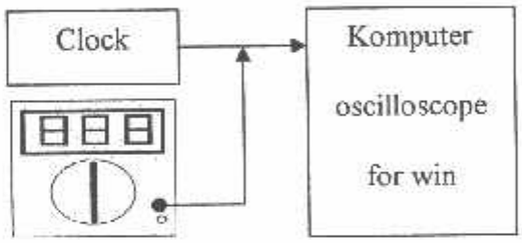
Gambar 4.4

Photo hasil pengukuran sensor

Sumber : pengujian

4.3. Pengujian Clock 555

Penggunaan clock sangat penting untuk mengeksekusi program yang ada pada rangkaian kontrol utama. Clock di bentuk dari IC NE555 yang di fungsikan sebagai multivibrator astabil dengan kecepatan clock 1.593k Khz.



Gambar 4-5

Digram blok pengujian clock

Hasil pengukuran diperlihatkan pada table dibawah ini :

No	R A (Ohm)	RB (Ohm)	C1 (uF)	F output (Hz)
1	1k	50k	0.1	142.1
2	1k	20k	0.1	349.9
3	1k	10k	0.1	683.1
4	1k	4k	0.1	1.593k Khz

Tabel 4-4

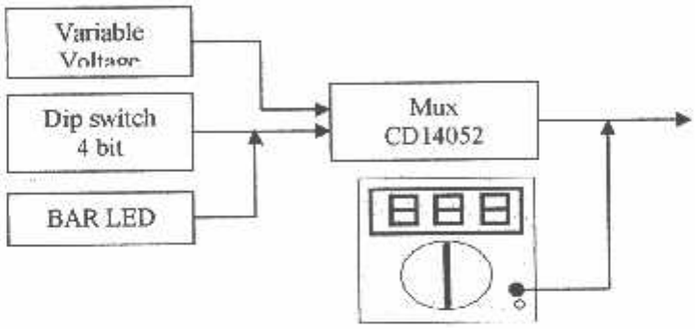
Pengukuran Frekuensi Clock

Terhadap Perubahan RB

4.4. Pengujian Multiplekser

Penggunaan multiplekser analog diperlukan untuk merubah penguatan pada op-amp. Karena jika penguatannya tidak dirubah maka keluaran dari penguat diferensial akan menjadi dua kali 5 volt. Maka keluaran tegangan ini akan merusak ADC.

Untuk melakukan pemilihan range, dapat dilakukan dengan memberikan data biner ke input data select pada multiplekser.



Gambar 4-5

Digram Blok Pengujian Multiplekser Analog

Dalam diagram blok diatas terlihat bahwa multiplekser analog diberi masukan tegangan yang dibuat variabel. Tegangan variabel ini diberikan pada inputan X1, X2, X3 dan binary switch dimasukan pada data select untuk memilih inputan mana yang akan dikeluarkan pada pin Y dan diukur dengan menggunakan voltmeter digital.

Hasil pengukuran diperlihatkan pada table dibawah ini :

No	Input (Volt)	Binary Switch	Output (Volt)
1	0.5	00	0.5
2	1.0	01	1.0
3	1.5	10	1.5
4	2.0	11	2.0

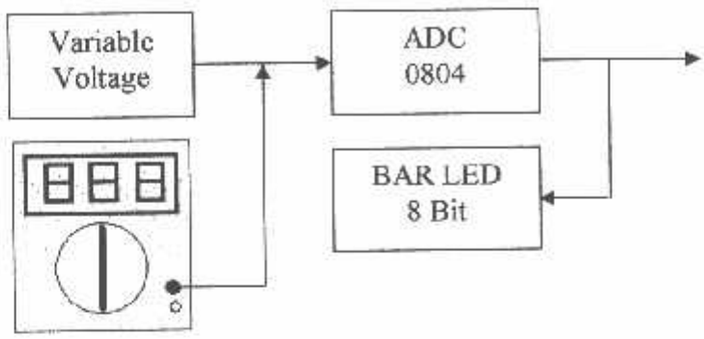
Tabel 4-5

Pengukuran Multiplekser Analog

Terhadap Variabel Input

4.5. Pengujian ADC

Analog to Digital Converter digunakan untuk mengubah tegangan analog menjadi data biner. Dalam perancangan alat ini digunakan ADC 0804 yang mempunyai data maksimal 8 bit



Gambar 4-6

Digram Blok Pengujian ADC 0804

Resolusi perubahan tiap bitnya ditentukan dengan memberikan tegangan referensi pada pin 9 (Vref/2). Tegangan referensi yang digunakan pada ADC ini adalah 2.5 volt. Dengan tegangan referensi sebesar 2.5 volt, maka resolusi perpindahan tiap lsb nya dapat dicari dengan persamaan sebagai berikut :

$$Vref/2 = 2.5 \text{ Volt}$$

$$Vref = 2*2.5 = 5 \text{ volt}$$

$$\text{Resolusi} - (Vref/2)/2^{n}-1$$

$$=5/256-1$$

$$=0.0196 \text{ volt}$$

Hasil pengukuran diperlihatkan pada table dibawah ini :

No	Output Diffr. (Volt)	Resulusi (Volt)	Output (Desimal)	Output (Biner)
1	210	0.0196	11.0	00001011
2	350	0.0196	17.8	00010001
3	520	0.0196	26.5	00011010
4	560	0.0196	28.5	00011100
5	740	0.0196	37.7	00100101
6	880	0.0196	44.8	00101101
7	1060	0.0196	54.1	00110110

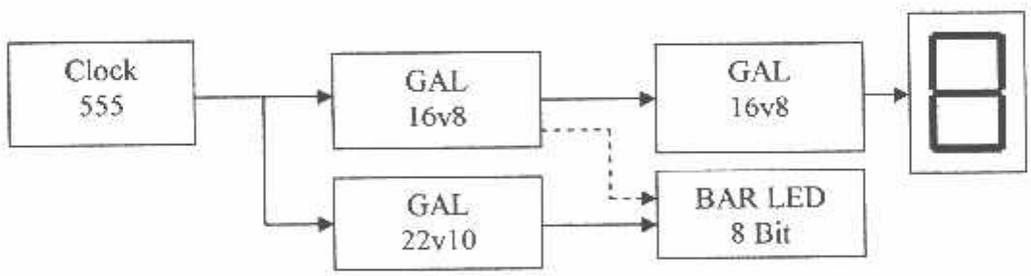
Tabel 4-6

Pengukuran output ADC 0804

Terhadap Variabel Input

4.6. Pengujian IC GAL 16v8 dan GAL 22v10

Untuk memproses dan menampilkan data input yang diukur, maka diperlukan IC GAL 22v10 dan GAL 16v8. Dalam pengujian alat ini, IC yang telah deprogram akan diberikan data input biner dan clock dari IC 555 seperti diagram blok dibawah ini:



Gambar 4-7

Digram Blok Pengujian

IC GAL 16v8 dan 22v10

Dari diagram blok diatas dapat dilihat bahwa IC gal 22v10 digunakan untuk counter 8 bit yang digunakan untuk dibandingkan dengan keluaran ADC 0804. Dan IC gal 16v8 digunakan sebagai counter 4 bit desimal.

Hasil dari pengujian IC GAL ini dapat dilihat dari table dibawah ini.

No	Clock	Output (22v10)	Output (16v8)	Output (Desimal)
1	0	00000000	0000	0
2	1	00000001	0001	1
3	2	00000010	0010	2
4	3	00000011	0011	3
5	4	00000100	0100	4
6	5	00000101	0101	5
7	6	00000110	0110	6
8	7	00000111	0111	7
9	8	00001000	1000	8
10	9	00001001	1001	9

Tabel 4-7

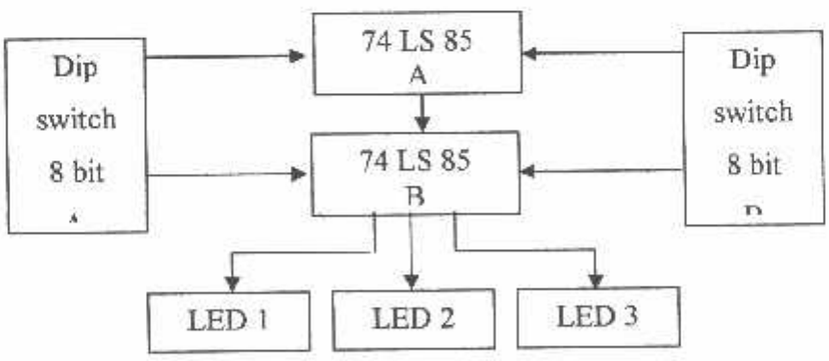
Pengujian IC Gal 22v10 dan IC Gal 16v8

Dari tabel diatas dapat dilihat bahwa keluaran dari IC GAL 22V10 adalah 8 Bit yang nantinya dapat digunakan untuk membandingkan dengan keluaran ADC.

4.7. Pengujian komparator 74LS85

Komparator (pembanding) yang digunakan dalam perencanaan dan pembuatan alat ini adalah komparator 4 bit yang disusun secara cascade dengan tujuan untuk membentuk kompoarator 8 bit.

Pengujian dari komparator ini dapat dillihat pada digram blok di bawah ini:



Gambar 4-8

Digram Blok Pengujian

Komparator 74ls85

Hasil dari pengujian multiplekser analog dapat dilihat pada tabel berikut:

No	Dip switch A	Dip switch B	Output (LED 1 A>B)	Output (LED 2 A<B)	Output (LED 3 A=B)
1	00000000	00000000	0	0	1
2	00000001	00000010	0	1	0
3	00000010	00000001	1	0	0
4	00000011	00000011	0	0	1
5	00000100	00000101	0	1	0

Tabel 4-8

Pengujian komparator 74LS85

Dari tabel diatas terlihat bahwa output dari komparotror 74LS85 yaitu led1 A>B, led2 A<B dan led3 A=B salah satu nya akan berkondisi high jika data yang yang dimasukan A>B atau A<B dan A=B.

4.8. Pengkalibrasian Alat Dengan Tang Ampere Meter.

Alat yang telah dibuat harus dikalibrasi terlebih dulu agar dapat diketahui keakuratan hasil pengukurannya. Pengkalibrasian alat ini menggunakan alat ukur sistem clamp (dikalungkan) yaitu manggunakan alat *Clamp meter* atau biasa disebut *Tang ampere meter.*

Hasil dari penkalibrasian dengan alat *tang ampere meter* seperti berikut :

No	P beban (Watt)	V beban (Volt)	I beban (Amper)	Hasil pada tang ampere	Hasil pada alat	Selisih pengukuran
1	25	220	0.11	0.10	0,11	0.01
2	40	220	0.18	0.15	0.17	0.02
3	60	220	0.27	0.25	0.26	0.00
4	65	220	0.29	0.28	0.30	0.02
5	85	220	0.38	0.34	0.36	0.02
6	100	220	0.45	0.46	0.45	0.01
7	125	220	0.56	0.56	0.55	0.01

Tabel 4-9

Hasil Pengkalibrasian Alat

Dengan Tang Ampere Meter

Dari hasil pengukuran terdapat perbedaan dengan hasil perhitungan, maka prosentase kesalahan rata-rata dapat dicari dengan rumus sebagai berikut:

$$\% \text{ kesalahan} = \frac{\textit{Hasil Perhitungan} - \textit{Hasil Pengukuran}}{\textit{Hasil Perhitungan}} \text{ X } 100\%$$

Dari hasil pengujian dan pengukuran di atas maka didapat prosentase kesalahan sebagai berikut :

$$\% \text{ Kesalahan} = \frac{0.32 - 0.31}{0.32} \text{ X } 100\%$$

$$= 3.1\ \%$$

Dari hasil pengkalibrasian di atas maka didapat prosentase kesalahan sebagai berikut :

$$\% \text{ kesalahan} = \frac{\textit{Hasil Tang ampere} - \textit{Hasil pada alat}}{\textit{Hasil Tang ampere}} \text{ X } 100\%$$

$$\% \text{ Kesalahan} = \frac{0.30 - 0.31}{0.30} \text{ X } 100\%$$

$$= 3.3\ \%$$

BAB V

PENUTUP

5.1. Kesimpulan

Dari perencanaan dan pembuatan alat ini dapat ditarik beberapa kesimpulan antara lain :

1. Pengambilan induksi arus listrik pada kawat yang dilalui oleh arus listrik dilakukan dengan cara mengalungkan sensor pada kawat tersebut. Jadi tidak perlu mengupas kawat yang akan di ukur.
2. Induksi arus listrik pada kawat penghantar dirubah menjadi tegangan terlebih dahulu sebelum dibaca oleh ADC. Perubahan induksi arus listrik ini sesuai dengan peraturan kaidah tangan kanan.
3. Cara menentukan range selector yaitu dengan cara menentukan berapa nilai maksimal arus yang akan diukur. Jika arus maksimal adalah 1 amper dan output sensor adalh 100 mV, maka diperlukan penguatan sebesar 50 kali untuk mendapatkan nilai 5000 mV (5 volt-nilai maksimal pengukuran ADC)
4. Perubahan tegangan dari sensor akan dibaca oleh ADC untuk dijadikan data biner terlebih dahulu kemudian diolah oleh IC GAL 22v10 dan GAL 16v8 kemudian ditampilkan dalam bentuk desimal.

5.2. Saran – saran

Perencanaan dan pembuatan alat ini masih jauh dari sempurna, maka dapat diberikan beberapa saran, antara lain :

1. Hasil pengukuran sebaiknya dapat dikirimkan melalui media Tone H/L, sebagai fungsi dari clock, sehingga dapat dipantau secara wireless dengan mudah .
2. Alat pengukur yang digunakan sebaiknya memiliki ukuran yang kecil (HANDY), sehingga mudah dalam pembawaannya.

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INSTITUT TEKNOLOGI NASIONAL
JL. BENDUNGAN SIGURA-GURA .2
MALANG

FORMULIR BIMBINGAN SKRIPSI

Nama : Ali Muntaha
Nim : 00.17.271
Masa Bimbingan : 8-Feb-2005 s/d 10-Aug-2005
Judul Skripsi : Perencanaan Dan Pembuatan Alat Pengukur Arus Listrik Dengan Sistem Induksi (Tang Ampere) Menggunakan Teknologi VHDL

No.	Tanggal	Uraian	Paraf Pembimbing
1.	07/03-05	Konsultasi Perenc. alat	
2.	21/03-05	Konsultasi Pemb. alat	
3.	16/04-05	Konsultasi bab IV.	
4.	25/05-05	Konsultasi Pengujian	
5.	06/06-05	Konsultasi bab I & II	
6.	18/06-05	Konsultasi bab III	
7.	10/07-05	Revisi bab IV	
8.	27/07-05	Pengujian alat	
9.	30/08-05	Konsultasi bab V	
10.	20/09-05	Acc seminar.	

Malang, 2005
Dosen Pembimbing

Ir. Teguh Herbasuki, MT

Form. S-4a

INSTITUT TEKNOLOGI NASIONAL MALANG
FAKULTAS TEKNOLOGI INDUSTRI
JURUSAN TEKNIK ELEKTRO S-1
KONSENTRASI TEKNIK ELEKTRONIKA

LEMBAR BIMBINGAN SKRIPSI

1.	Nama	: Ali Muntaha
2.	Nim	: 00.17.271
3.	Jurusan	: Teknik Elektro S-1
4.	Konsentrasi	: Teknik Elektronika
5.	Judul Skripsi	: Perancangan dan Pembuatan Alat Pengukur arus Listrik dengan Sistem Induksi (tang ampere) Menggunakan Teknologi VHDL
6.	Tanggal Pengajuan Skripsi	: 8 Februari 2005
7.	Selesai Pengajuan Skripsi	: 10 Agustus 2005
8.	Pembimbing	: Ir. Teguh Herbasuki, MT
9.	Telah Dievaluasi Dengan Nilai	: 85 (Delapan Puluh Lima)

Mengetahui,
Ketua Jurusan Elektro S-1

Ir. F. Yudi Limpraptono, MT
NIP.Y. 1 039 500 274

Disetujui,
Dosen Pembimbing

Ir. Teguh Herbasuki, MT
NIP.Y. 1 038 900 209

INSTITUT TEKNOLOGI NASIONAL MALANG
FAKULTAS TEKNOLOGI INDUSTRI
JURUSAN TEKNIK ELEKTRO S-1
KONSENTRASI TEKNIK ELEKTRONIKA

FORMULIR PERBAIKAN SKRIPSI

Nama : Ali Muntaha
Nim : 00.17.271
Masa Bimbingan : 8 Februari 2005 – 10 Agustus 2005
Judul : Perancangan dan Pembuatan Alat Pengukur arus Listrik dengan Sistem Induksi (tang ampere) Menggunakan Teknologi VHDL

No	Tanggal	Materi Perbaikan	Paraf Penguji
1	5 Oktober 2005	Analisis pembuatan inti besi, lilitan dan flux.	
2	5 Oktober 2005	Batasan masalah besarnya tegangan dan max.	
3	5 Oktober 2005	Kesimpulan diperbaiki.	
4	5 Oktober 2005	Buat layout tata letak komponen.	

Disetujui :

Penguji I

Ir. Usman Djuanda,MM
NIP. 1 029 800 324

Penguji II

Mimin Mustikawati, ST
NIP. 1 030 000 352

Mengetahui,
Dosen Pembimbing

Ir. Teguh Herbasuki, MT
NIP.Y. 1 038 900 209

INSTITUT TEKNOLOGI NASIONAL
JL. BENDUNGAN SIGURA-GURA 2
MALANG

Lampiran : 1 (satu) berkas
Pembimbing Skripsi

Kepada : Yth. **Ir. Teguh Herbasuki, MT**
Dosen Institut Teknologi Nasional
Malang

Yang bertanda tangan di bawah ini :

Nama	: Ali Muntaha
Nim	: 0017271
Jurusan	: Teknik Elektro S-1
Konsentrasi	: Teknik Elektronika

Dengan ini mengajukan permohonan, kiranya Bapak/Ibu bersedia menjadi Dosen Pembimbing Utama / ~~Pendamping~~ dari (1,) 2 orang pembimbing *), untuk penyusunan Skripsi dengan judul (Proposl terlampir) :

Perencanaan dan pembuatan alat pengukur arus listrik menggunakan sistem induksi (Tang Ampere Meter) menggunakan teknologi VHDL

Adapun tugas tersebut sebagai salah satu syarat untuk menempuh Ujian Akhir Sarjana Teknik.
Demikian permohonan kami dan atas kesediaan Bapak/Ibu kami ucapkan terima kasih.

Mengetahui
Ketua Jurusan T. Elektro S-1

Ir. I Made Wartana, MT
NIP 131 991 182

Malang, 4-Jan-2005
Hormat kami

Ali Muntaha
0017271

*) coret yang tidak perlu

Form S-3a

INSTITUT TEKNOLOGI NASIONAL
JL. BENDUNGAN SIGURA-GURA 2
MALANG

PERNYATAAN KESEDIAAN DALAM PEMBIMBINGAN SKRIPSI

Sesuai permohonan dari mahasiswa/i :

Nama	: Ali Muntaha
Nim	: 0017271
Semester	: VII
Jurusan	: Teknik Elektro S-1
Konsentrasi	: Teknik Elektronika

Dengan ini menyatakan bersedia/~~tidak bersedia~~ *) membimbing skripsi dari mahasiswa tersebut, dengan judul :

Perencanaan dan pembuatan alat pengukur arus listrik menggunakan sistem induksi (Tang Ampere Meter) menggunakan teknologi VHDL

Demikian surat pernyataan ini kami buat agar dapat digunakan seperlunya.

Malang, 4-Jan-2005

Hormat kami

Ir. Teguh Herbasuki, MT

NIP. P

Catatan:
Setelah disetujui agar formulir ini
Diserahkan mahasiswa/I yang bersangkutan
Kepada jurusan untuk diproses lebih lanjut
*) Coret yang tidak perlu

Form S-3b

LAMPIRAN

1. Gambar Rangkaian
2. Foto Alat
3. Listing Program
4. Data Sheet

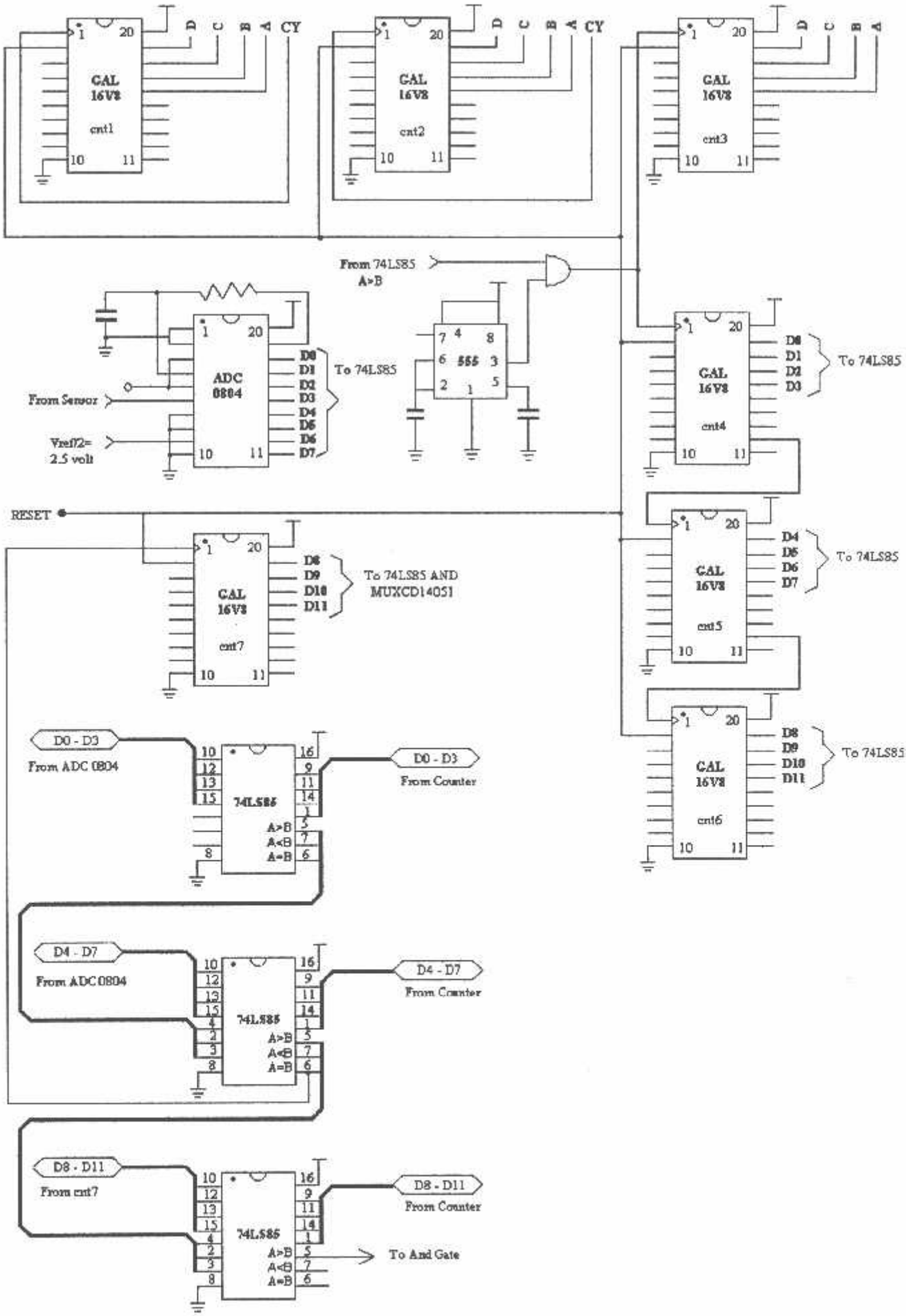

GAL 16V8
cnt1
cnt2
cnt3
cnt4
cnt5
cnt6
cnt7
D C B A CY
ADC 0804
From Sensor
Vref/2= 2.5 volt
D0 D1 D2 D3 D4 D5 D6 D7
To 74LS85
555
From 74LS85 A>B
RESET
D8 D9 D10 D11
To 74LS85 AND MUXCD14051
D0 - D3
From ADC 0804
From Counter
74LS85
A>B
A<B
A=B
D4 - D7
From ADC0804
D8 - D11
From cnt7
To And Gate

Photo Sensor Induksi

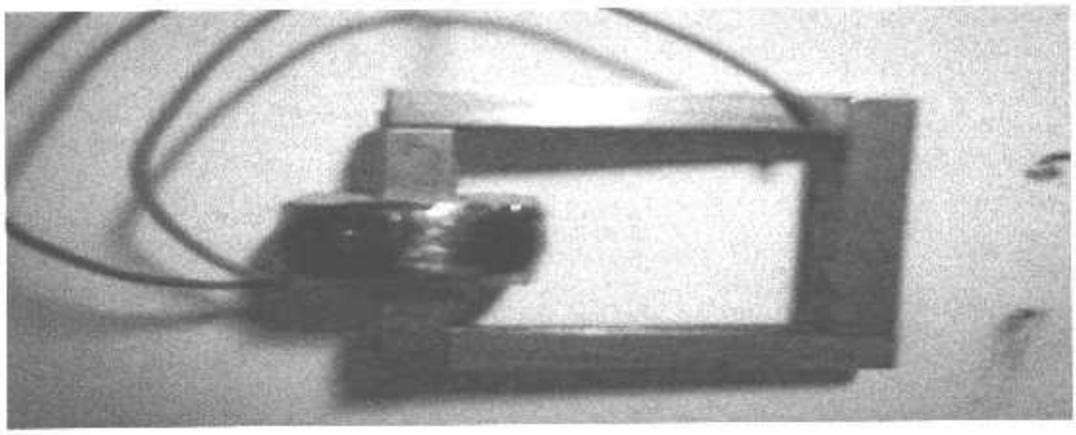


Photo Alat Tampak Dalam

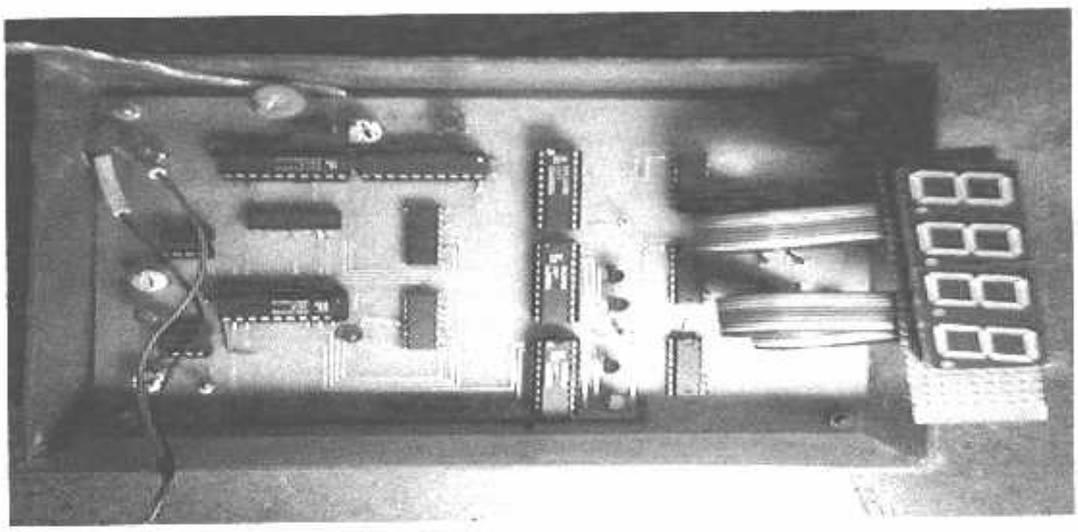
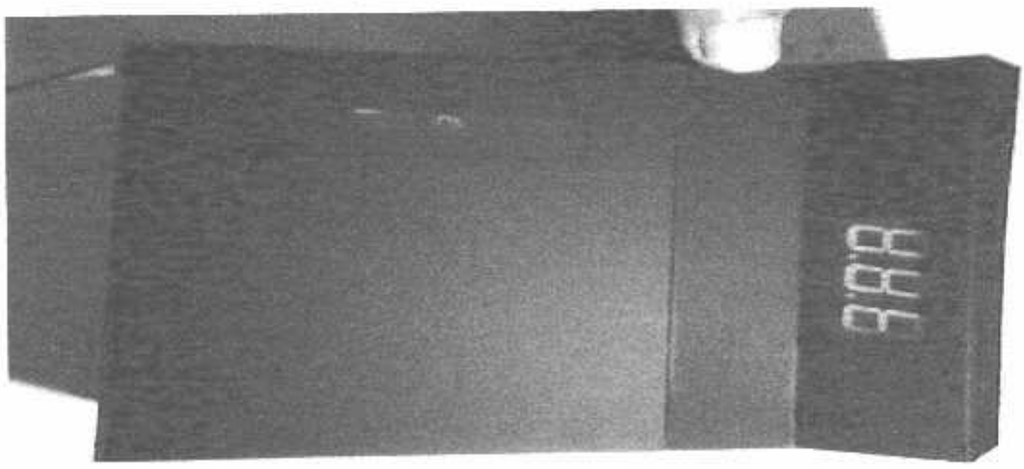
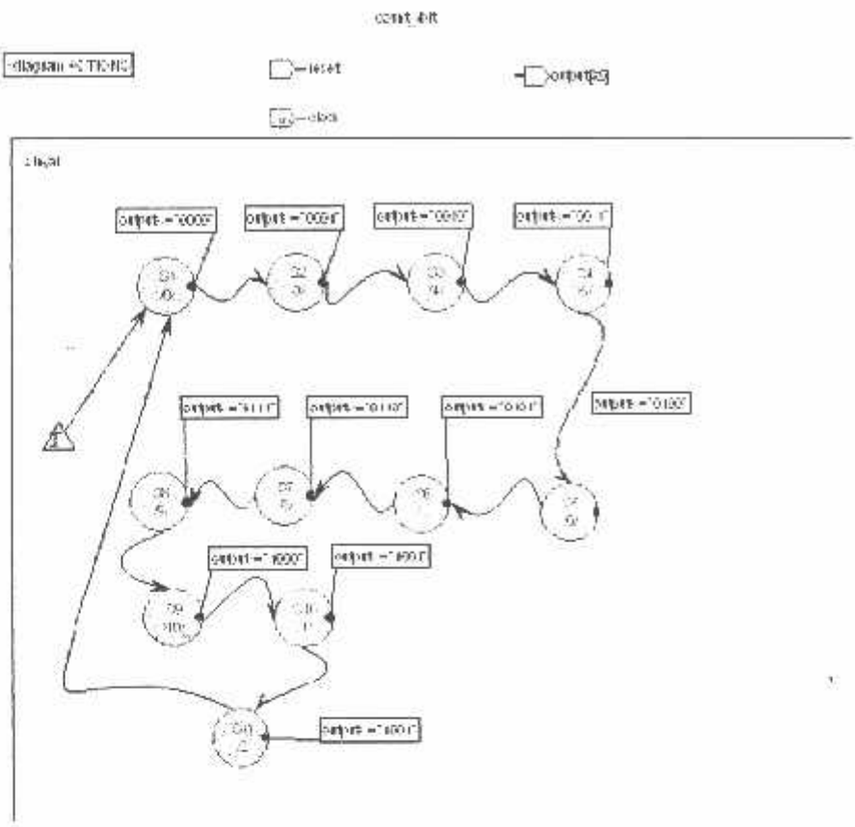


Photo Alat Tampak Luar

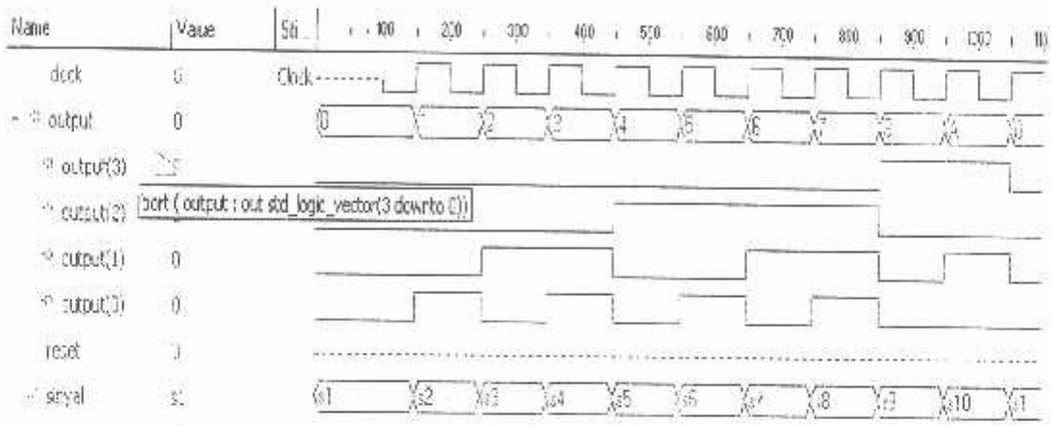





```
--
-- File: C:\Program Files\Aldec\count_4bit.vhd
-- created: 07/26/05 05:03:39
-- from: 'C:\Program Files\Aldec\count_4bit.asf'
-- by fsm2hdl - version: 2.0.1.45
--
library IEEE;
use IEEE.std_logic_1164.all;


entity count_4bit is
  port (clock: in STD_LOGIC;
        reset: in STD_LOGIC;
        output: out STD_LOGIC_VECTOR (3 downto 0));
Attribute Part_Name of count_4bit : Entity is "22v10";
Attribute Pin_numbers of count_4bit : Entity is
"clock:1 reset:2 "
&"output(3):17 output(2):15 output(1):16 output(0):18";
end;

architecture count_4bit_arch of count_4bit is


-- SYMBOLIC ENCODED state machine: sinyal
```

```
type sinyal_type is (S1, S2, S3, S4, S5, S6, S7, S8,s9,s10);
signal sinyal: sinyal_type;

begin
--concurrent signal assignments
--diagram ACTIONS;


sinyal_machine: process (clock)

begin

if clock'event and clock = '1' then
        if reset='0' then
                sinyal <= S1;
        else
        case sinyal is
                when S1 =>
                        sinyal <= S2;
                when S2 =>
                        sinyal <= S3;
                when S3 =>
                        sinyal <= S4;
                when S4 =>
                        sinyal <= S5;
                when S5 =>
                        sinyal <= S6;
                when S6 =>
                        sinyal <= S7;
                when S7 =>
                        sinyal <= S8;
                when S8 =>
                        sinyal <= S9;
                when S9 =>
                        sinyal <= S10;
                when S10 =>
                        sinyal <= S1;
                when others =>
                        null;
         end case;
         end if;
 end if;
 end process;

 -- signal assignment statements for combinatorial outputs
 output_assignment:
 output <= "0001" when (sinyal = S2) else
        "0010" when (sinyal = S3) else
        "0011" when (sinyal = S4) else
        "0100" when (sinyal = S5) else
```

```
        "0101" when (sinyal = S6) else
        "0110" when (sinyal = S7) else
        "0111" when (sinyal = S8) else
                "1000" when (sinyal = S9) else
                "1010" when (sinyal = S10) else
        "0000";
end count_4bit_arch;
```



```
library ieee;
use ieee.std_logic_1164.all;
entity decoder_s is
      port ( data: in std_logic_vector(3 downto 0);
             display: out std_logic_vector(7 downto 0));
Attribute Part_Name of decoder_s : Entity is "16v8";
Attribute Pin_numbers of decoder_s : Entity is
"data(3):4 data(2):2 data(1):3 data(0):5 "
&"display(7):19 display(6):18 display(5):17 "
&"display(4):16 display(3):15 display(2):14 "
&"display(1):13 display(0):12";
end decoder_s;

architecture rtl of decoder_s is

begin
 encode: process (data) begin
   case data is
    when "0000" =>
     display <= "01000001";--0
    when "0001" =>
     display <= "11100111";--1
    when "0010" =>
     display <= "10001001";--2
    when "0011" =>
     display <= "10000011";--3
    when "0100" =>
     display <= "00100111";--4
    when "0101" =>
     display <= "00010011";--5
    when "0110" =>
     display <= "00010001";--6
    when "0111" =>
     display <= "11000111";--7
   when "1000" =>
     display <= "00000001";--8
   when "1001" =>
     display <= "00000011";--9
   when "1010" =>
     display <= "01000000";--0
   when others =>
     display <= "00010011";--S
    end case;
  end process;
end rtl;
```

```
library ieee;
use ieee.std_logic_1164.all;
entity decoder_e is
      port ( data: in std_logic_vector(3 downto 0);
            display: out std_logic_vector(7 downto 0));
Attribute Part_Name of decoder_e : Entity is "16v8";
Attribute Pin_numbers of decoder_e : Entity is
"data(3):4 data(2):2 data(1):3 data(0):5 "
&"display(7):19 display(6):18 display(5):17 "
&"display(4):16 display(3):15 display(2):14 "
&"display(1):13 display(0):12";
end decoder_e;

architecture rtl of decoder_e is

begin
 encode: process (data) begin
  case data is
   when "0000" =>
    display <= "01000001";--0
   when "0001" =>
    display <= "11100111";--1
   when "0010" =>
    display <= "10001001";--2
   when "0011" =>
    display <= "10000011";--3
   when "0100" =>
    display <= "00100111";--4
   when "0101" =>
    display <= "00010011";--5
   when "0110" =>
    display <= "00010001";--6
   when "0111" =>
    display <= "11000111";--7
   when "1000" =>
    display <= "00000001";--8
   when "1001" =>
    display <= "00000011";--9
   when "1010" =>
    display <= "01000000";--0
   when others =>
    display <= "00011001";--E
   end case;
  end process;
end rtl;
```

```
library ieee;
use ieee.std_logic_1164.all;
entity decoder_y is
      port ( data: in std_logic_vector(3 downto 0);
             display: out std_logic_vector(7 downto 0));
Attribute Part_Name of decoder_y : Entity is "16v8";
Attribute Pin_numbers of decoder_y : Entity is
"data(3):4 data(2):2 data(1):3 data(0):5 "
&"display(7):19 display(6):18 display(5):17 "
&"display(4):16 display(3):15 display(2):14 "
&"display(1):13 display(0):12";
end decoder_y;

architecture rtl of decoder_y is

begin
 encode: process (data) begin
  case data is
   when "0000" =>
    display <= "01000001";--0
   when "0001" =>
    display <= "11100111";--1
   when "0010" =>
    display <= "10001001";--2
   when "0011" =>
    display <= "10000011";--3
   when "0100" =>
    display <= "00100111";--4
   when "0101" =>
    display <= "00010011";--5
   when "0110" =>
    display <= "00010001";--6
   when "0111" =>
    display <= "11000111";--7
   when "1000" =>
    display <= "00000001";--8
   when "1001" =>
    display <= "00000011";--9
   when "1010" =>
    display <= "01000000";--0
   when others =>
    display <= "00100011";--Y
  end case;
 end process;
end rtl;
```


```
Warp VHDL Synthesis Compiler: Version 5.2 IR 7
 Copyright (C) 1991, 1992, 1993,
 1994, 1995, 1996, 1997, 1998, 1999 Cypress
Semiconductor
```

```
=============================================================================
-
Compiling:  counter_16v8.vhd
Options:    -yu -e10 -w100 -o2 -ygs -fP -vl0 -dc16v8 -pPALCE16V8-
25PC/PI -u Wangset.hie counter_16v8.vhd
=============================================================================
=

vhdlfe V5.2 IR 17:  VHDL parser
Tue Jul 26 04:17:25 2005

Library 'work' => directory 'lc16v8'
Linking 'C:\warp\bin\std.vhd'.
Linking 'C:\warp\lib\common\cypress.vhd'.
Linking 'C:\warp\lib\common\work\cypress.vif'.
Library 'ieee' => directory 'C:\warp\lib\ieee\work'
Linking 'C:\warp\lib\ieee\work\stdlogic.vif'.
Linking 'C:\warp\lib\common\stdlogic\lpmpkg.vif'.
Linking 'C:\warp\lib\common\stdlogic\rtlpkg.vif'.
Linking 'C:\warp\lib\common\stdlogic\mod_cnst.vif'.
Linking 'C:\warp\lib\common\stdlogic\mod_mth.vif'.
Linking 'C:\warp\lib\common\stdlogic\mod_gen.vif'.
counter_16v8.vhd (line 23, col 22):  Note: Substituting module
'add_vi_ss' for '+'.

vhdlfe:  No errors.


tovif V5.2 IR 17:  High-level synthesis
Tue Jul 26 04:17:25 2005

Linking 'C:\warp\bin\std.vhd'.
Linking 'C:\warp\lib\common\cypress.vhd'.
Linking 'C:\warp\lib\common\work\cypress.vif'.
Linking 'C:\warp\lib\ieee\work\stdlogic.vif'.
Linking 'C:\warp\lib\common\stdlogic\lpmpkg.vif'.
Linking 'C:\warp\lib\common\stdlogic\rtlpkg.vif'.
Linking 'C:\warp\lib\common\stdlogic\mod_cnst.vif'.
Linking 'C:\warp\lib\common\stdlogic\mod_mth.vif'.
Linking 'C:\warp\lib\common\stdlogic\mod_gen.vif'.

tovif:  No errors.
```

```
topld V5.2 IR 17:  Synthesis and optimization
Tue Jul 26 04:17:25 2005

Linking 'C:\warp\bin\std.vhd'.
Linking 'C:\warp\lib\common\cypress.vhd'.
Linking 'C:\warp\lib\common\work\cypress.vif'.
Linking 'C:\warp\lib\ieee\work\stdlogic.vif'.
Linking 'C:\warp\lib\common\stdlogic\lpmpkg.vif'.
Linking 'C:\warp\lib\common\stdlogic\rtlpkg.vif'.
Linking 'C:\warp\lib\common\stdlogic\mod_cnst.vif'.
Linking 'C:\warp\lib\common\stdlogic\mod_mth.vif'.
Linking 'C:\warp\lib\common\stdlogic\mod_gen.vif'.
Linking 'C:\warp\lib\lc16v8\stdlogic\c16v8.vif'.

-------------------------------------------------------
Detecting unused logic.
-------------------------------------------------------



-------------------------------------------------------
Alias Detection
-------------------------------------------------------

-------------------------------------------------------
Aliased 0 equations, 8 wires.
-------------------------------------------------------

-------------------------------------------------------
Circuit simplification
-------------------------------------------------------

-------------------------------------------------------
Circuit simplification results:

      Expanded 8 signals.
      Turned 0 signals into soft nodes.
      Maximum expansion cost was set at 10.
-------------------------------------------------------

-------------------------------------------------------
Alias Detection
-------------------------------------------------------

-------------------------------------------------------
Aliased 0 equations, 0 wires.
-------------------------------------------------------
Created 31 PLD nodes.

topld:  No errors.

-------------------------------------------------------------------------
-------
PLD Optimizer Software:       DSGNOPT.EXE    02/APR/1999  [v4.02 ]
5.2 IR 17

DESIGN HEADER INFORMATION  (04:17:25)

Input File(s): counter_16v8.pla
Device       : c16v8
Package      : PALCE16V8-25PC/PI
```

```
ReportFile   : counter_16v8.rpt

Program Controls:
    COMMAND PROPERTY BUS_HOLD ENABLE

Signal Requests:
    GROUP FAST_SLEW ALL

Completed Successfully
-------------------------------------------------------------------------
-------
PLD Optimizer Software:        DSGNOPT.EXE     02/APR/1999  [v4.02 :
5.2 IR 17

OPTIMIZATION OPTIONS        (04:17:25)

Messages:
  Information: Process virtual 'count_0D' ... expanded.
  Information: Process virtual 'count_1D' ... expanded.
  Information: Process virtual 'count_2D' ... expanded.
  Information: Process virtual 'count_3D' ... expanded.
  Information: Process virtual 'count_0' ... converted to NODE.
  Information: Process virtual 'count_1' ... converted to NODE.
  Information: Process virtual 'count_2' ... converted to NODE.
  Information: Process virtual 'count_3' ... converted to NODE.
  Information: Optimizing logic using best output polarity for
signals:
        count_1.D count_2.D count_3.D

  Information: Selected logic optimization OFF for signals:
        count_out1(0) count_out1(1) count_out1(2) count_out1(3)
count_0.D
        count_0.C count_1.C count_2.C count_3.C


Summary:
                Error Count = 0      Warning Count = 0

Completed Successfully
-------------------------------------------------------------------------
-------
PLD Optimizer Software:        MINOPT.EXE      21/SEP/1998  [v4.02 ]
5.2 IR 17

LOGIC MINIMIZATION          ()

Messages:


Summary:
                Error Count = 0      Warning Count = 0

Completed Successfully
-------------------------------------------------------------------------
-------
PLD Optimizer Software:        DSGNOPT.EXE     02/APR/1999  [v4.02 ]
5.2 IR 17

OPTIMIZATION OPTIONS        (04:17:25)
```

```
Messages:

Summary:
                Error Count = 0      Warning Count = 0

Completed Successfully
-------------------------------------------------------------------------
-------
PLD Compiler Software:        PLA2JED.EXE    02/APR/1999  [v4.02 ]
5.2 IR 17

DESIGN EQUATIONS           (04:17:25)


    count_out1(0) =
          count_0.Q * oe

    count_out1(1) =
          count_1.Q * oe

    count_out1(2) =
          count_2.Q * oe

    count_out1(3) =
          count_3.Q * oe

    count_0.D =
          /count_0.Q * /rst

    count_0.C =
          clk

    count_3.D =
          /count_3.Q * count_2.Q * count_1.Q * count_0.Q * /rst
        + count_3.Q * /count_0.Q * /rst
        + count_3.Q * /count_1.Q * /rst
        + count_3.Q * /count_2.Q * /rst

    count_3.C =
          clk

    count_2.D =
          /count_2.Q * count_1.Q * count_0.Q * /rst
        + count_2.Q * /count_0.Q * /rst
        + count_2.Q * /count_1.Q * /rst

    count_2.C =
          clk

    count_1.D =
          count_1.Q * /count_0.Q * /rst
        + /count_1.Q * count_0.Q * /rst

    count_1.C =
          clk


Completed Successfully
-------------------------------------------------------------------------
-------
```

```
PLD Compiler Software:         PLA2JED.EXE    02/APR/1999  [v4.02 ]
5.2 IR 17

DESIGN RULE CHECK          (04:17:25)

Messages:
                 None.


Summary:
                 Error Count = 0      Warning Count = 0

Completed Successfully
-----------------------------------------------------------------------
-------
PLD Compiler Software:         PLA2JED.EXE    02/APR/1999  [v4.02 ]
5.2 IR 17

PINOUT INFORMATION     (04:17:25)

Messages:
  Information: Checking for duplicate NODE logic.
                 None.

                                C16V8C
                 __________________________________________
            clk =| 1|                                  |20|* not used
            rst =| 2|                                  |19|=
count_out1(3)
             oe =| 3|                                  |18|=
count_out1(2)
       not used *| 4|                                  |17|=
count_out1(1)
       not used *| 5|                                  |16|=
count_out1(0)
       not used *| 6|                                  |15|=
(count_0)
       not used *| 7|                                  |14|=
(count_1)
       not used *| 8|                                  |13|=
(count_2)
       not used *| 9|                                  |12|=
(count_3)
       not used *|10|                                  |11|* Reserved
                 __________________________________________


Summary:
                 Error Count = 0      Warning Count = 0

Completed Successfully
-----------------------------------------------------------------------
-------
PLD Compiler Software:         PLA2JED.EXE    02/APR/1999  [v4.02 ]
5.2 IR 17

RESOURCE UTILIZATION        (04:17:25)

  Information: Macrocell Utilization.
```

Description	Used	Max
Dedicated Inputs	2	8
Clock/Inputs	1	1
Enable/Inputs	0	1
Output Macrocells	8	8
	11 /	18 = 61 %

Information: Output Logic Product Term Utilization.

Node#	Output Signal Name	Used	Max
12	count_3	4	8
13	count_2	3	8
14	count_1	2	8
15	count_0	1	8
16	count_out1(0)	1	8
17	count_out1(1)	1	8
18	count_out1(2)	1	8
19	count_out1(3)	1	8
		14 /	64 = 21 %

Completed Successfully

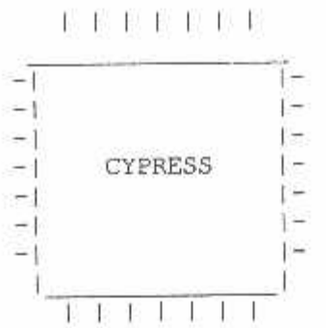
PLD Compiler Software: PLA2JED.EXE 02/APR/1999 [v4.02]
5.2 IR 17

JEDEC ASSEMBLE (04:17:25)

Messages:
  Information: Output file 'counter_16v8.jed' created.

Summary:
Error Count = 0 Warning Count = 0

Completed Successfully at 04:17:25



Warp VHDL Synthesis Compiler: Version 6.3 IR 35
Copyright (C) 1991-2001 Cypress Semiconductor

```
================================================================================
Compiling:  count_4bit.vhd
Options:    -m -yu -el0 -w100 -o2 -ygs -fP -v10 -dc22v10 -ppalce22v10-
25pc/pi -b count_4bit.vhd -u ate_down.hie
================================================================================

vhdlfe V6.3 IR 35:  VHDL parser
Sat Jul 30 14:15:11 2005

Library 'work' => directory 'lc22v10'
Linking 'C:\Program Files\Cypress\Warp\bin\std.vhd'.
Linking 'C:\Program Files\Cypress\Warp\lib\common\cypress.vhd'.
Linking 'C:\Program Files\Cypress\Warp\lib\common\work\cypress.vif'.
Library 'ieee' => directory 'C:\Program
Files\Cypress\Warp\lib\ieee\work'
Linking 'C:\Program Files\Cypress\Warp\lib\ieee\work\stdlogic.vif'.

vhdlfe:  No errors.


tovif V6.3 IR 35:  High-level synthesis
Sat Jul 30 14:15:11 2005

Linking 'C:\Program Files\Cypress\Warp\bin\std.vhd'.
Linking 'C:\Program Files\Cypress\Warp\lib\common\cypress.vhd'.
Linking 'C:\Program Files\Cypress\Warp\lib\common\work\cypress.vif'.
Linking 'C:\Program Files\Cypress\Warp\lib\ieee\work\stdlogic.vif'.

tovif:  No errors.


topld V6.3 IR 35:  Synthesis and optimization
Sat Jul 30 14:15:12 2005

Linking 'C:\Program Files\Cypress\Warp\bin\std.vhd'.
Linking 'C:\Program Files\Cypress\Warp\lib\common\cypress.vhd'.
Linking 'C:\Program Files\Cypress\Warp\lib\common\work\cypress.vif'.
Linking 'C:\Program Files\Cypress\Warp\lib\ieee\work\stdlogic.vif'.
State variable 'sinyal' is represented by a Bit_vector (0 to 3).
State encoding (sequential) for 'sinyal' is:
      s1 := b"0000";
      s2 := b"0001";
      s3 := b"0010";
      s4 := b"0011";
```

```
      s5 := b"0100";
      s6 := b"0101";
      s7 := b"0110";
      s8 := b"0111";
      s9 := b"1000";
      s10 :=      b"1001";

-------------------------------------------------------------
Detecting unused logic.
-------------------------------------------------------------


-------------------------------------------------------------
Alias Detection
-------------------------------------------------------------

-------------------------------------------------------------
Aliased 0 equations, 2 wires.
-------------------------------------------------------------

-------------------------------------------------------------
Circuit simplification
-------------------------------------------------------------

-------------------------------------------------------------
Circuit simplification results:

      Expanded 0 signals.
      Turned 0 signals into soft nodes.
      Maximum default expansion cost was set at 10.
-------------------------------------------------------------
Created 14 PLD nodes.

topld:  No errors.

-------------------------------------------------------------------------------
-----
PLD Optimizer Software:       DSGNOPT.EXE    31/03/2000  [v4.02 ] 6.3
IR 35

DESIGN HEADER INFORMATION  (14:15:13)

Input File(s): count_4bit.pla
Device       : C22V10
Package      : palce22v10-25pc/pi
ReportFile   : count_4bit.rpt

Program Controls:
    COMMAND LANGUAGE_VHDL
    COMMAND PROPERTY BUS_HOLD ENABLE

Signal Requests:
    GROUP USEPOL ALL
    GROUP FAST_SLEW ALL
```

```
Completed Successfully
------------------------------------------------------------------------
-----
PLD Optimizer Software:        DSGNOPT.EXE     31/03/2000  [v4.02 ] 6.3
IR 35

OPTIMIZATION OPTIONS        (14:15:13)

Messages:
  Information: Process virtual 'sinyalSBV_3D'sinyalSBV_3D ... expanded.
  Information: Process virtual 'sinyalSBV_2D'sinyalSBV_2D ... expanded.
  Information: Process virtual 'sinyalSBV_1D'sinyalSBV_1D ... expanded.
  Information: Process virtual 'sinyalSBV_0D'sinyalSBV_0D ... expanded.
  Information: Process virtual 'sinyalSBV_3' ... converted to NODE.
  Information: Process virtual 'sinyalSBV_2' ... converted to NODE.
  Information: Optimizing logic using best output polarity for signals:
         output(1) output(2).D output(3).D sinyalSBV_2.D

  Information: Selected logic optimization OFF for signals:
         output(0) output(2).C output(3).C sinyalSBV_2.C sinyalSBV_3.D
         sinyalSBV_3.C


Summary:
                  Error Count = 0      Warning Count = 0

Completed Successfully
------------------------------------------------------------------------
-----
PLD Optimizer Software:        MINOPT.EXE      01/NOV/1999  [v4.02 ] 6.3
IR 35

LOGIC MINIMIZATION          ()

Messages:


Summary:
                  Error Count = 0      Warning Count = 0

Completed Successfully
------------------------------------------------------------------------
-----
PLD Optimizer Software:        DSGNOPT.EXE     31/03/2000  [v4.02 ] 6.3
IR 35

OPTIMIZATION OPTIONS        (14:15:13)

Messages:
  Information: Optimizing Banked Preset/Reset requirements.


Summary:
                  Error Count = 0      Warning Count = 0
```

```
Completed Successfully
-------------------------------------------------------------------------------
-----
PLD Compiler Software:          PLA2JED.EXE    31/03/2000  [v4.02 ] 6.3
IR 35

<CYPRESSTAG name="Equations" icon=FILE_RPT_EQUATION>
DESIGN EQUATIONS            (14:15:13)
</CYPRESSTAG>

    output(0) =
          /output(3).Q * sinyalSBV_3.Q

    output(1) =
          output(3).Q * sinyalSBV_3.Q
        + sinyalSBV_2.Q

    output(2).D =
          /output(2).Q * reset * sinyalSBV_2.Q * sinyalSBV_3.Q
        + output(2).Q * reset * /sinyalSBV_2.Q
        + output(2).Q * reset * /sinyalSBV_3.Q

    output(2).AR =
          GND

    output(2).SP =
          GND

    output(2).C =
          clock

    output(3).D =
          output(2).Q * reset * sinyalSBV_2.Q * sinyalSBV_3.Q
        + output(3).Q * reset * /sinyalSBV_3.Q

    output(3).AR =
          GND

    output(3).SP =
          GND

    output(3).C =
          clock

    sinyalSBV_2.D =
          /output(3).Q * reset * /sinyalSBV_2.Q * sinyalSBV_3.Q
        + reset * sinyalSBV_2.Q * /sinyalSBV_3.Q

    sinyalSBV_2.AR =
          GND

    sinyalSBV_2.SP =
          GND

    sinyalSBV_2.C =
          clock
```

```
    sinyalSBV_3.D =
          reset * /sinyalSBV_3.Q

    sinyalSBV_3.AR =
          GND

    sinyalSBV_3.SP =
          GND

    sinyalSBV_3.C =
          clock


Completed Successfully
-------------------------------------------------------------------------------
-----
PLD Compiler Software:        PLA2JED.EXE    31/03/2000  [v4.02 ] 6.3
IR 35

DESIGN RULE CHECK          (14:15:14)

Messages:
                  None.


Summary:
                  Error Count = 0      Warning Count = 0

Completed Successfully
-------------------------------------------------------------------------------
-----
PLD Compiler Software:        PLA2JED.EXE    31/03/2000  [v4.02 ] 6.3
IR 35

<CYPRESSTAG name="Pinout" icon=FILE_RPT_PINOUT>
PINOUT INFORMATION   (14:15:14)
</CYPRESSTAG>
Messages:
  Information: Checking for duplicate NODE logic.
                  None.
```

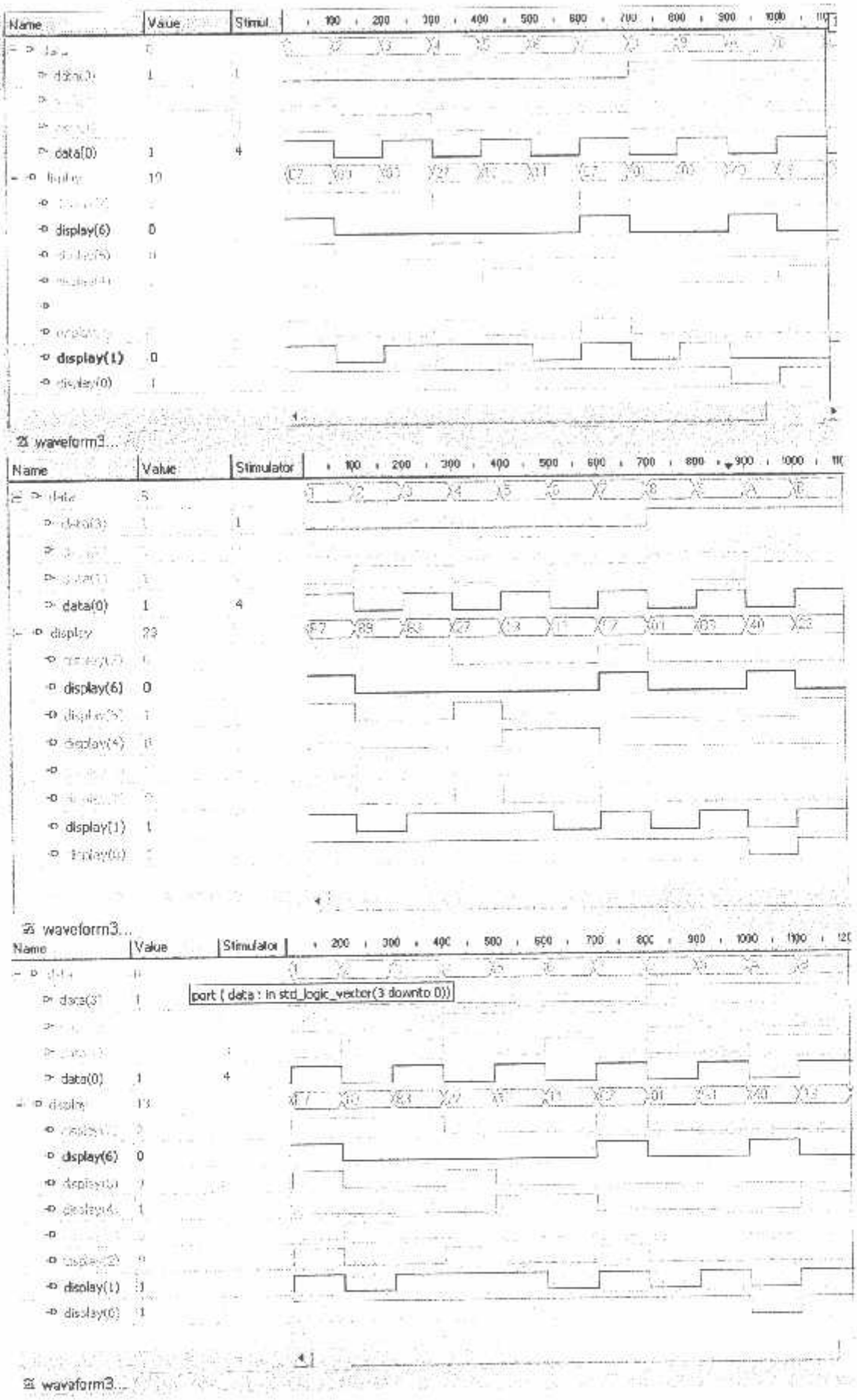
```
                              C22V10
               ____________________________________________
          clock =| 1|                                   |24|* not used
          reset =| 2|                                   |23|= output(3)
       not used *| 3|                                   |22|= output(2)
       not used *| 4|                                   |21|= output(1)
       not used *| 5|                                   |20|= output(0)
       not used *| 6|                                   |19|* not used
       not used *| 7|                                   |18|* not used
       not used *| 8|                                   |17|* not used
       not used *| 9|                                   |16|* not used
       not used *|10|                                   |15|-
(sinyalSBV_3)
       not used *|11|                                   |14|-
(sinyalSBV_2)
       not used *|12|                                   |13|* not used
               ____________________________________________


Summary:
                 Error Count = 0      Warning Count = 0

Completed Successfully
-----------------------------------------------------------------------
-----
PLD Compiler Software:        PLA2JED.EXE    31/03/2000  [v4.02 ] 6.3
IR 35

<CYPRESSTAG name="Utilization" icon=FILE_RPT_UTILIZATION>
RESOURCE UTILIZATION (14:15:14)
</CYPRESSTAG>
  Information: Macrocell Utilization.

                     Description          Used      Max
                 ______________________________________
                 | Dedicated Inputs     |    1  |   11  |
                 | Clock/Inputs         |    1  |    1  |
                 | I/O Macrocells       |    6  |   10  |
                 ______________________________________
                                             8  /   22   = 36  %


  Information: Output Logic Product Term Utilization.
```

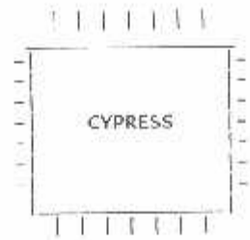
Node#	Output Signal Name	Used	Max
14	sinyalSBV_2	2	8
15	sinyalSBV_3	1	10
16	Unused	0	12
17	Unused	0	14
18	Unused	0	16
19	Unused	0	16
20	output(0)	1	14
21	output(1)	2	12
22	output(2)	3	10
23	output(3)	2	8
25	Unused	0	1

11 / 121 = 9 %

```
Completed Successfully
-------------------------------------------------------------------------
-----
PLD Compiler Software:          PLA2JED.EXE     31/03/2000  [v4.02 ] 6.3
IR 35

JEDEC ASSEMBLE                (14:15:14)

Messages:
  Information: Output file 'count_4bit.pin' created.
  Information: Output file 'count_4bit.jed' created.

  Usercode:
  Checksum:     4DD4


Summary:
                  Error Count = 0       Warning Count = 0

Completed Successfully at 14:15:14
```

Gambar hasil simulasi sofware





Warp VHDL Synthesis Compiler: Version 5.2 IR 17


```
============================================================================
Compiling:  counter_22v10_8bit.vhd
Options:    -m -yu -e10 -w100 -o2 -ygs -fP -v10 -yw -dc22v10 -pPALCE22V10-25PC/PI -u
Wangsel.bie counter_22v10_8bit.vhd
============================================================================

vhdlfe V5.2 IR 17:  VHDL parser
Tue Jul 26 04:39:03 2005

Library 'work' => directory 'lc22v10'
Linking 'C:\warp\bin\std.vhd'.
Linking 'C:\warp\lib\common\cypress.vhd'.
Linking 'C:\warp\lib\common\work\cypress.vif'.
Library 'ieee' => directory 'C:\warp\lib\ieee\work'
Linking 'C:\warp\lib\ieee\work\stdlogic.vif'.
Linking 'C:\warp\lib\common\stdlogic\lpmpkg.vif'.
Linking 'C:\warp\lib\common\stdlogic\rtlpkg.vif'.
Linking 'C:\warp\lib\common\stdlogic\mod_cnst.vif'.
Linking 'C:\warp\lib\common\stdlogic\mod_mth.vif'.
Linking 'C:\warp\lib\common\stdlogic\mod_gen.vif'.
counter_22v10_8bit.vhd (line 26, col 22):  Note: Substituting module 'add_vi_ss' for
'+'.

vhdlfe:  No errors.


tovif V5.2 IR 17:  High-level synthesis
Tue Jul 26 04:39:03 2005

Linking 'C:\warp\bin\std.vhd'.
Linking 'C:\warp\lib\common\cypress.vhd'.
Linking 'C:\warp\lib\common\work\cypress.vif'.
Linking 'C:\warp\lib\ieee\work\stdlogic.vif'.
Linking 'C:\warp\lib\common\stdlogic\lpmpkg.vif'.
Linking 'C:\warp\lib\common\stdlogic\rtlpkg.vif'.
Linking 'C:\warp\lib\common\stdlogic\mod_cnst.vif'.
Linking 'C:\warp\lib\common\stdlogic\mod_mth.vif'.
Linking 'C:\warp\lib\common\stdlogic\mod_gen.vif'.

tovif:  No errors.


topld V5.2 IR 17:  Synthesis and optimization
Tue Jul 26 04:39:04 2005

Linking 'C:\warp\bin\std.vhd'.
Linking 'C:\warp\lib\common\cypress.vhd'.
Linking 'C:\warp\lib\common\work\cypress.vif'.
Linking 'C:\warp\lib\ieee\work\stdlogic.vif'.
Linking 'C:\warp\lib\common\stdlogic\lpmpkg.vif'.
Linking 'C:\warp\lib\common\stdlogic\rtlpkg.vif'.
Linking 'C:\warp\lib\common\stdlogic\mod_cnst.vif'.
Linking 'C:\warp\lib\common\stdlogic\mod_mth.vif'.
Linking 'C:\warp\lib\common\stdlogic\mod_gen.vif'.
Linking 'C:\warp\lib\lc22v10\stdlogic\c22v10.vif'.

------------------------------------------------------------
Detecting unused logic.
------------------------------------------------------------
    User names
        count_7
        count_6
        count_5
        count_4
        count_3
        count_2
        count_1
        count_0


Deleted 8 user equations/components.
Deleted 8 Synthesized equations/components.
```

```
---------------------------------------------------
Alias Detection
---------------------------------------------------

---------------------------------------------------
Aliased 0 equations, 0 wires.
---------------------------------------------------

---------------------------------------------------
Circuit simplification
---------------------------------------------------

---------------------------------------------------
Circuit simplification results:

        Expanded 0 signals.
        Turned 0 signals into soft nodes.
        Maximum expansion cost was set at 10.
---------------------------------------------------
Created 59 PLD nodes.

topld:  No errors.

---------------------------------------------------
PLD Optimizer Software:       DSGNOPT.EXE    02/APR/1999  [v4.02 ] 5.2 IR 17

DESIGN HEADER INFORMATION  (04:39:04)

Input File(s): counter_22v10_8bit.pla
Device       : C22V10
Package      : PALCE22V10-25PC/P1
Reportfile   : counter_22v10_8bit.rpt

Program Controls:
    COMMAND PROPERTY BUS_HOLD ENABLE

Signal Requests:
    GROUP SLOW_SLEW ALL

Completed Successfully
---------------------------------------------------
PLD Optimizer Software:       DSGNOPT.EXE    02/APR/1999  [v4.02 ] 5.2 IR 17

OPTIMIZATION OPTIONS       (04:39:04)

Messages:
  Information: Selected logic optimization OFF for signals:
        count_out1(0) count_out1(1) count_out1(2) count_out1(3) count_out1(4)
        count_out1(5) count_out1(6) count_out1(7)


Summary:
                Error Count = 0      Warning Count = 0

Completed Successfully
---------------------------------------------------
PLD Optimizer Software:       MINOPT.EXE     21/SEP/1998  [v4.02 ] 5.2 IR 17

LOGIC MINIMIZATION         ()

Messages:


Summary:
                Error Count = 0      Warning Count = 0

Completed Successfully
---------------------------------------------------
PLD Optimizer Software:       DSGNOPT.EXE    02/APR/1999  [v4.02 ] 5.2 IR 17

OPTIMIZATION OPTIONS       (04:39:04)

Messages:
  Information: Optimizing Banked Preset/Reset requirements.


Summary:
                Error Count = 0      Warning Count = 0

Completed Successfully
---------------------------------------------------
PLD Compiler Software:        PLA2JED.EXE    02/APR/1999  [v4.02 ] 5.2 IR 17
```

DESIGN EQUATIONS (04:39:04)

```
    count_out1(0) =
          oe * count_out1(0)

    count_out1(1) =
          oe * count_out1(1)

    count_out1(2) =
          oe * count_out1(2)

    count_out1(3) =
          oe * count_out1(3)

    count_out1(4) =
          oe * count_out1(4)

    count_out1(5) =
          oe * count_out1(5)

    count_out1(6) =
          oe * count_out1(6)

    count_out1(7) =
          oe * count_out1(7)
```

Completed Successfully

PLD Compiler Software: PLA2JED.EXE 02/APR/1999 [v4.02] 5.2 IR 17

DESIGN RULE CHECK (04:39:04)

Messages:
None.

Summary:
Error Count = 0 Warning Count = 0

Completed Successfully

PLD Compiler Software: PLA2JED.EXE 02/APR/1999 [v4.02] 5.2 IR 17

PINOUT INFORMATION (04:39:04)

Messages:
Information: All signals pre-placed in user design.

```
                                  C22V10
                 __________________________________________
          clk =| 1|                                        |24|* not used
          rst =| 2|                                        |23|= count_out1(7)
           oe =| 3|                                        |22|= count_out1(6)
     not used *| 4|                                        |21|= count_out1(5)
     not used *| 5|                                        |20|= count_out1(4)
     not used *| 6|                                        |19|= count_out1(3)
     not used *| 7|                                        |18|= count_out1(2)
     not used *| 8|                                        |17|= count_out1(1)
     not used *| 9|                                        |16|= count_out1(0)
     not used *|10|                                        |15|* not used
     not used *|11|                                        |14|* not used
     not used *|12|                                        |13|* not used
                 __________________________________________
```

Summary:
Error Count = 0 Warning Count = 0

Completed Successfully
Information: Checking for duplicate NODE logic.

PLD Compiler Software: PLA2JED.EXE 02/APR/1999 [v4.02] 5.2 IR 17

RESOURCE UTILIZATION (04:39:04)

Information: Macrocell Utilization.

Description	Used	Max
Dedicated Inputs	1	11
Clock/Inputs	0	1
I/O Macrocells	8	10

9 / 22 = 40 %

Information: Output Logic Product Term Utilization.

Node#	Output Signal Name	Used	Max
14	Unused	0	8
15	Unused	0	10
16	count_out1(0)	1	12
17	count_out1(1)	1	14
18	count_out1(2)	1	16
19	count_out1(3)	1	16
20	count_out1(4)	1	14
21	count_out1(5)	1	12
22	count_out1(6)	1	10
23	count_out1(7)	1	8
25	unused	0	1

8 / 121 = 6 %

Completed Successfully

PLD Compiler Software: PLAZJED.EXE 02/APR/1999 [v4.02] 5.2 IR 17

JEDEC ASSEMBLE (04:39:04)

Messages:
Information: Output file 'counter 22v10_8bit.jed' created.

Summary:
Error Count = 0 Warning Count = 0

Completed Successfully at 04:39:04

November 1999

National Semiconductor

ADC0801/ADC0802/ADC0803/ADC0804/ADC0805
8-Bit µP Compatible A/D Converters

General Description

The ADC0801, ADC0802, ADC0803, ADC0804 and ADC0805 are CMOS 8-bit successive approximation A/D converters that use a differential potentiometric ladder—similar to the 256R products. These converters are designed to allow operation with the NSC800 and INS8080A derivative control bus with TRI-STATE output latches directly driving the data bus. These A/Ds appear like memory locations or I/O ports to the microprocessor and no interfacing logic is needed.

Differential analog voltage inputs allow increasing the common-mode rejection and offsetting the analog zero input voltage value. In addition, the voltage reference input can be adjusted to allow encoding any smaller analog voltage span to the full 8 bits of resolution.

Features

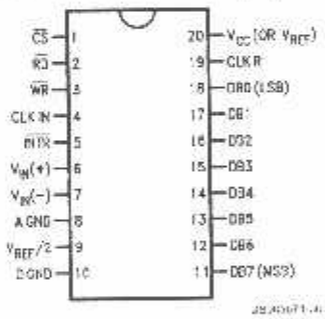
- Compatible with 8080 µP derivatives—no interfacing logic needed - access time - 135 ns
- Easy interface to all microprocessors, or operates 'stand alone'
- Differential analog voltage inputs
- Logic inputs and outputs meet both MOS and TTL voltage level specifications
- Works with 2.5V (LM336) voltage reference
- On-chip clock generator
- 0V to 5V analog input voltage range with single 5V supply
- No zero adjust required
- 0.3" standard width 20-pin DIP package
- 20-pin molded chip carrier or small outline package
- Operates ratiometrically or with 5 V_{DC}, 2.5 V_{DC}, or analog span adjusted voltage reference

Key Specifications

- Resolution: 8 bits
- Total error: ±¼ LSB, ±½ LSB and ±1 LSB
- Conversion time: 100 µs

Connection Diagram

ADC080X
Dual-In-Line and Small Outline (SO) Packages



See Ordering Information

Ordering Information

TEMP RANGE		0°C TO 70°C	0°C TO 70°C	−40°C TO +85°C
ERROR	±¼ Bit Adjusted			ADC0801LCN
	±½ Bit Unadjusted	ADC0802LCWM		ADC0802LCN
	±½ Bit Adjusted			ADC0803LCN
	±1Bit Unadjusted	ADC0804LCWM	ADC0804LCN	ADC0805LCN/ADC0804LCJ
PACKAGE OUTLINE		M20B—Small Outline	N20A—Molded DIP	

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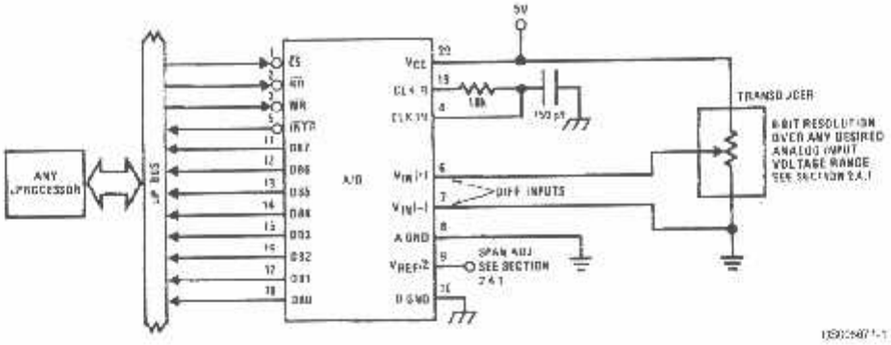
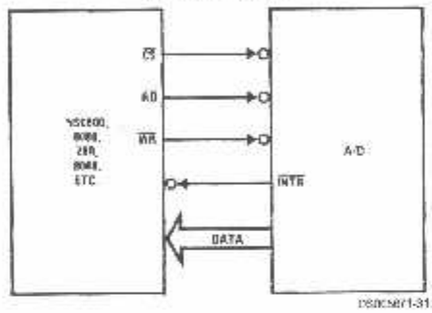
 DS005671

Typical Applications



8080 Interface



Error Specification (Includes Full-Scale, Zero Error, and Non-Linearity)			
Part Number	Full-Scale Adjusted	$V_{REF}/2$=2.500 V_{DC} (No Adjustments)	$V_{REF}/2$=No Connection (No Adjustments)
ADC0801	±¼ LSB		
ADC0802		±½ LSB	
ADC0803	±½ LSB		
ADC0804		±1 LSB	
ADC0805			±1 LSB

Absolute Maximum Ratings (Notes 1, 2)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Supply Voltage (V_{CC}) (Note 3)	6.5V
Voltage	
Logic Control Inputs	−0.3V to +18V
At Other Input and Outputs	−0.3V to (V_{CC}+0.3V)
Lead Temp. (Soldering, 10 seconds)	
Dual-In-Line Package (plastic)	260°C
Dual-In-Line Package (ceramic)	300°C
Surface Mount Package	
Vapor Phase (60 seconds)	215°C
Infrared (15 seconds)	220°C
Storage Temperature Range	−65°C to +150°C
Package Dissipation at T_A=25°C	875 mW
ESD Susceptibility (Note 10)	800V

Operating Ratings (Notes 1, 2)

Temperature Range	$T_{MIN} \le T_A \le T_{MAX}$
ADC0804LCJ	−40°C≤T_A≤+85°C
ADC0801/02/03/05LCN	−40°C≤T_A≤+85°C
ADC0804LCN	0°C≤T_A≤+70°C
ADC0802/04LCWM	0°C≤T_A≤+70°C
Range of V_{CC}	4.5 V_{DC} to 6.3 V_{DC}

Electrical Characteristics

The following specifications apply for V_{CC}=5 V_{DC}, $T_{MIN} \le T_A \le T_{MAX}$ and f_{CLK}=640 kHz unless otherwise specified.

Parameter	Conditions	Min	Typ	Max	Units
ADC0801: Total Adjusted Error (Note 8)	With Full Scale Adj (See Section 2.5.2)			±¼	LSB
ADC0802: Total Unadjusted Error (Note 8)	V_{REF}/2=2.500 V_{DC}			±½	LSB
ADC0803: Total Adjusted Error (Note 8)	With Full-Scale Adj (See Section 2.5.2)			±½	LSB
ADC0804: Total Unadjusted Error (Note 8)	V_{REF}/2=2.500 V_{DC}			±1	LSB
ADC0805: Total Unadjusted Error (Note 8)	V_{REF}/2-No Connection			±1	LSB
V_{REF}/2 Input Resistance (Pin 9)	ADC0801/02/03/05	2.5	8.0		kΩ
	ADC0804 (Note 9)	0.75	1.1		kΩ
Analog Input Voltage Range	(Note 4) V(+) or V(−)	Gnd−0.05		V_{CC}+0.05	V_{DC}
DC Common-Mode Error	Over Analog Input Voltage Range		±1/16	±⅛	LSB
Power Supply Sensitivity	V_{CC}=5 V_{DC} ±10% Over Allowed V_{IN}(+) and V_{IN}(−) Voltage Range (Note 4)		±1/16	±⅛	LSB

AC Electrical Characteristics

The following specifications apply for V_{CC}=5 V_{DC} and $T_{MIN} \le T_A \le T_{MAX}$ unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Units
T_C	Conversion Time	f_{CLK}=640 kHz (Note 6)	103		114	µs
T_C	Conversion Time	(Notes 5, 6)	66		73	1/f_{CLK}
f_{CLK}	Clock Frequency	V_{CC}=5V, (Note 5)	100	640	1460	kHz
	Clock Duty Cycle		40		60	%
CR	Conversion Rate in Free-Running Mode	$\overline{INTR}$ tied to $\overline{WR}$ with $\overline{CS}$ =0 V_{DC}, f_{CLK}=640 kHz	8770		9708	conv/s
$t_{W(WR)L}$	Width of $\overline{WR}$ Input (Start Pulse Width)	$\overline{CS}$ =0 V_{DC} (Note 7)	100			ns
t_{ACC}	Access Time (Delay from Falling Edge of $\overline{RD}$ to Output Data Valid)	C_L=100 pF		135	200	ns
t_{1H}, t_{0H}	TRI-STATE Control (Delay from Rising Edge of $\overline{RD}$ to Hi-Z State)	C_L=10 pF, R_L=10k (See TRI-STATE Test Circuits)		125	200	ns
t_{WI}, t_{RI}	Delay from Falling Edge of $\overline{WR}$ or $\overline{RD}$ to Reset of $\overline{INTR}$			300	450	ns
C_{IN}	Input Capacitance of Logic Control Inputs			5	7.5	pF

AC Electrical Characteristics (Continued)

The following specifications apply for V_{CC}=5 V_{DC} and $T_{MIN} \leq T_A \leq T_{MAX}$ unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Units
C_{OUT}	TRI-STATE Output Capacitance (Data Buffers)			5	7.5	pF
CONTROL INPUTS (Note: CLK IN (Pin 4) is the input of a Schmitt trigger circuit and is therefore specified separately)						
V_{IN} (1)	Logical "1" Input Voltage (Except Pin 4 CLK IN)	V_{CC}=5.25 V_{DC}	2.0		15	V_{DC}
V_{IN} (0)	Logical "0" Input Voltage (Except Pin 4 CLK IN)	V_{CC}=4.75 V_{DC}			0.8	V_{DC}
I_{IN} (1)	Logical "1" Input Current (All Inputs)	V_{IN}=5 V_{DC}		0.005	1	μA_{DC}
I_{IN} (0)	Logical "0" Input Current (All Inputs)	V_{IN}=0 V_{DC}	-1	-0.005		μA_{DC}
CLOCK IN AND CLOCK R						
V_T+	CLK IN (Pin 4) Positive Going Threshold Voltage		2.7	3.1	3.5	V_{DC}
V_T-	CLK IN (Pin 4) Negative Going Threshold Voltage		1.5	1.8	2.1	V_{DC}
V_H	CLK IN (Pin 4) Hysteresis $(V_T+)-(V_T-)$		0.6	1.3	2.0	V_{DC}
V_{OUT} (0)	Logical "0" CLK R Output Voltage	I_O=360 µA V_{CC}=4.75 V_{DC}			0.4	V_{DC}
V_{OUT} (1)	Logical "1" CLK R Output Voltage	I_O=-360 µA V_{CC}=4.75 V_{DC}	2.4			V_{DC}
DATA OUTPUTS AND INTR						
V_{OUT} (0)	Logical "0" Output Voltage Data Outputs INTR Output	 I_{OUT}=1.6 mA, V_{CC}=4.75 V_{DC} I_{OUT}=1.0 mA, V_{CC}=4.75 V_{DC}			 0.4 0.4	 V_{DC} V_{DC}
V_{OUT} (1)	Logical "1" Output Voltage	I_O= -360 µA, V_{CC}=4.75 V_{DC}	2.4			V_{DC}
V_{OUT} (1)	Logical "1" Output Voltage	I_O=-10 µA, V_{CC}=4.75 V_{DC}	4.5			V_{DC}
I_{OUT}	TRI-STATE Disabled Output Leakage (All Data Buffers)	V_{OUT}=0 V_{DC} V_{OUT}=5 V_{DC}	-3		 3	μA_{DC} μA_{DC}
I_{SOURCE}		V_{OUT} Short to Gnd, T_A=25°C	4.5	6		mA_{DC}
I_{SINK}		V_{OUT} Short to V_{CC}, T_A=25°C	9.0	16		mA_{DC}
POWER SUPPLY						
I_{CC}	Supply Current (Includes Ladder Current) ADC0801/02/03/04LCJ/C5 ADC0804LCN/LCWM	f_{CLK}=640 kHz, $V_{REF}/2$=NC, T_A=25°C and $\overline{CS}$ =5V		 1.1 .9	 1.8 2.5	 mA mA

Note 1: Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. DC and AC electrical specifications do not apply when operating the device beyond its specified operating conditions.

Note 2: All voltages are measured with respect to Gnd, unless otherwise specified. The separate A Gnd point should always be wired to the D Gnd.

Note 3: A zener diode exists, internally, from V_{CC} to Gnd and has a typical breakdown voltage of 7 V_{DC}.

Note 4: For $V_{IN}(-) \geq V_{IN}(+)$ the digital output code will be 0000 0000. Two on-chip diodes are tied to each analog input (see block diagram) which will forward conduct for analog input voltages one diode drop below ground or one diode drop greater than the V_{CC} supply. Be careful, during testing at low V_{CC} levels (4.5V), as high level analog inputs (5V) can cause this input diode to conduct—especially at elevated temperatures, and cause errors for analog inputs near full scale. The spec allows 50 mV forward bias of either diode. This means that as long as the analog V_{IN} does not exceed the supply voltage by more than 50 mV, the output code will be correct. To achieve an absolute 0 V_{DC} to 5 V_{DC} input voltage range will therefore require a minimum supply voltage of 4.950 V_{DC} over temperature variations, initial tolerance and loading.

Note 5: Accuracy is guaranteed at f_{CLK} = 640 kHz. At higher clock frequencies accuracy can degrade. For lower clock frequencies, the duty cycle limits can be extended so long as the minimum clock high time interval or minimum clock low time interval is no less than 275 ns.

Note 6: With an asynchronous start pulse, up to 8 clock periods may be required before the internal clock phases are proper to start the conversion process. The start request is internally latched, see *Figure 4* and section 2.0.

AC Electrical Characteristics (Continued)

Note 7: The $\overline{CS}$ input is assumed to bracket the $\overline{WR}$ strobe input and therefore timing is dependent on the $\overline{WR}$ pulse width. An arbitrarily wide pulse width will hold the converter in a reset mode and the start of conversion is initiated by the low to high transition of the $\overline{WR}$ pulse (see timing diagrams).

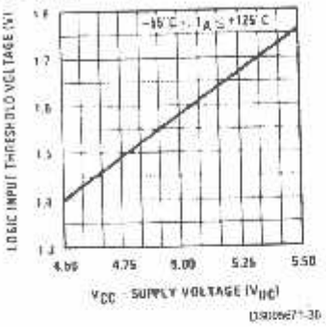
Note 8: None of these A/Ds requires a zero adjust (see section 2.5.1). To obtain zero code at other analog input voltages see section 2.5 and Figure 7.

Note 9: The $V_{IN}(-)/2$ pin is the center point of a two resistor divider connected from V_{CC} to ground. In all versions of the ADC0801, ADC0802, ADC0803, and ADC0805, and in the ADC0804LCJ, each resistor is typically 16 kΩ. In all versions of the ADC0804 except the ADC0804LCJ, each resistor is typically 2.2 kΩ.

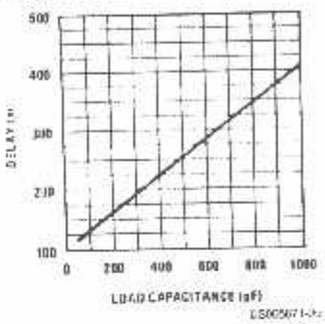
Note 10: Human body model, 100 pF discharged through a 1.5 kΩ resistor.

Typical Performance Characteristics

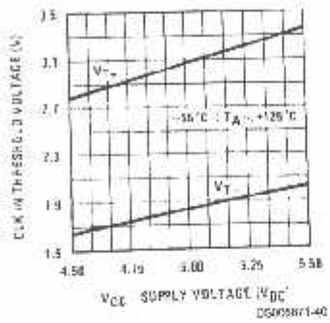
Logic Input Threshold Voltage vs. Supply Voltage



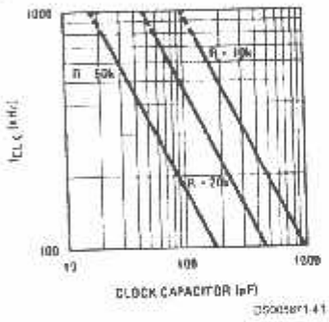
Delay From Falling Edge of $\overline{RD}$ to Output Data Valid vs. Load Capacitance



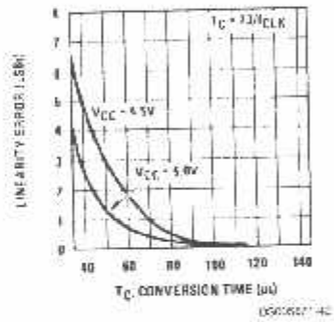
CLK IN Schmitt Trip Levels vs. Supply Voltage



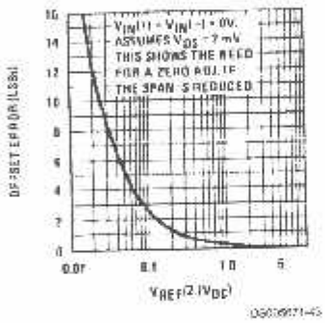
f_{CLK} vs. Clock Capacitor



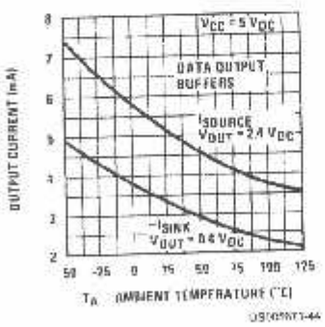
Full-Scale Error vs Conversion Time



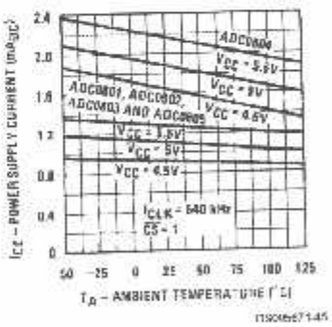
Effect of Unadjusted Offset Error vs. $V_{REF}/2$ Voltage



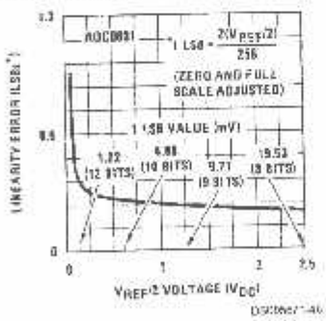
Output Current vs Temperature



Power Supply Current vs Temperature (Note 9)

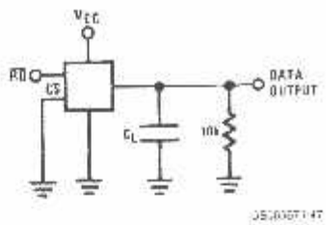


Linearity Error at Low $V_{REF}/2$ Voltages

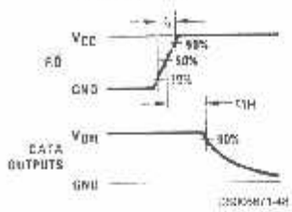


TRI-STATE Test Circuits and Waveforms

t_{1H}

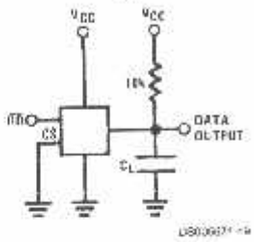


t_{1H}, C_L=10 pF

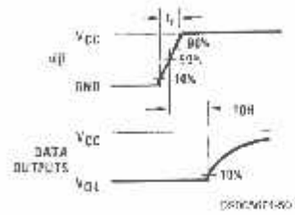


t_r=20 ns

t_{0H}

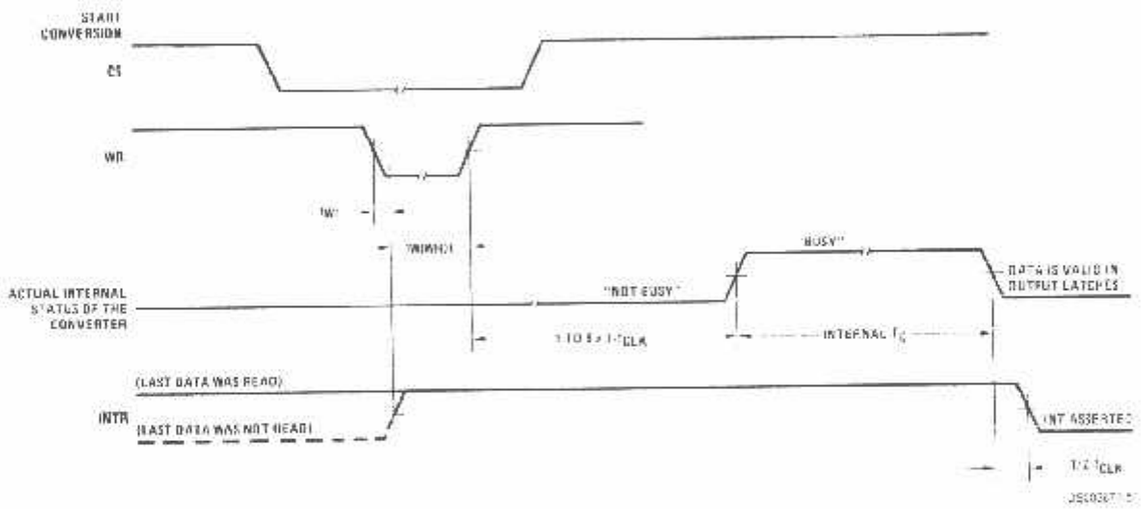


t_{0H}, C_L=10 pF



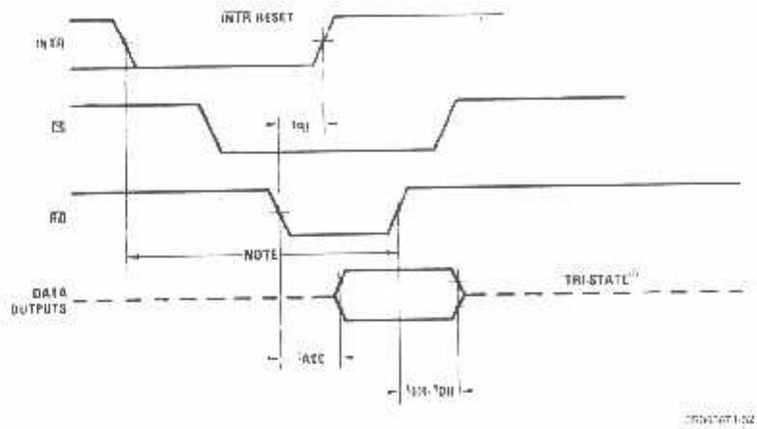
t_r=20 ns

Timing Diagrams (All timing is measured from the 50% voltage points)



Timing Diagrams (All timing is measured from the 50% voltage points) (Continued)

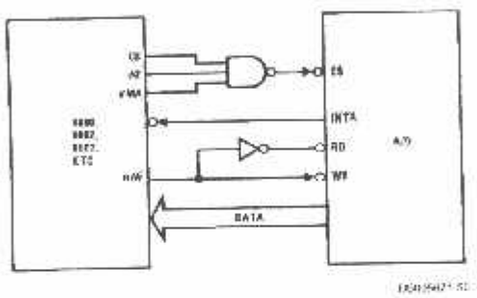
Output Enable and Reset with $\overline{INTR}$



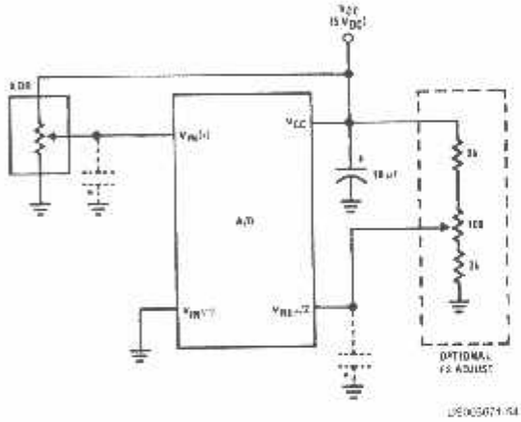
Note: Read strobe must occur 8 clock periods ($8/f_{CLK}$) after assertion of interrupt to guarantee reset of $\overline{INTR}$.

Typical Applications

6800 Interface



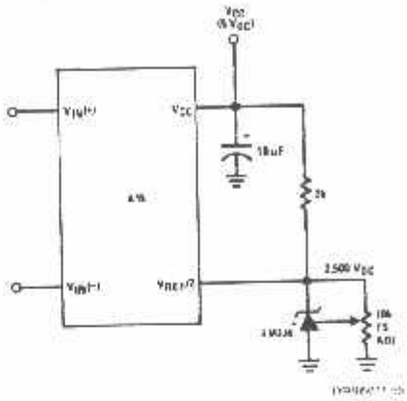
Ratiometeric with Full-Scale Adjust



Note: before using caps at V_{IN} or $V_{REF}/2$, see section 2.3.2 Input Bypass Capacitors

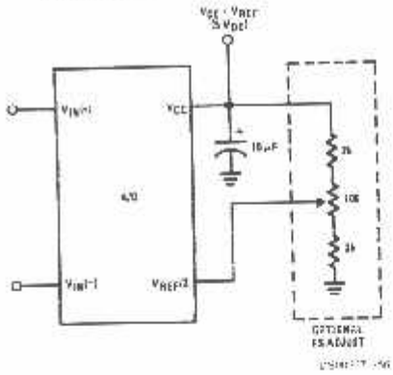
Typical Applications (Continued)

Absolute with a 2.500V Reference

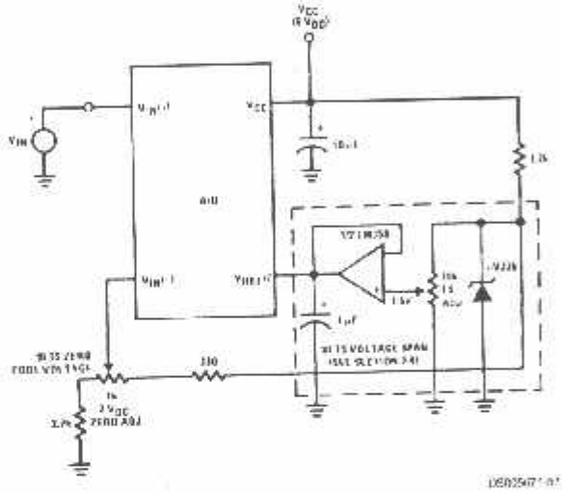


*For low power, see also LM385–2.5

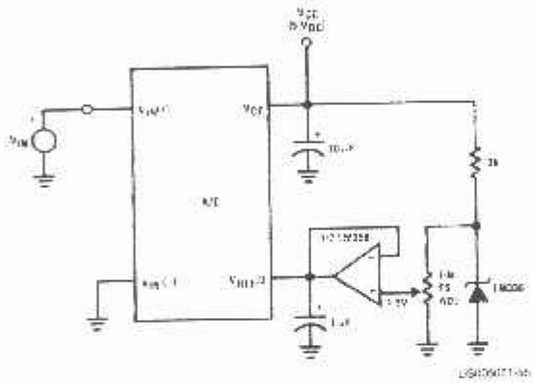
Absolute with a 5V Reference



Zero-Shift and Span Adjust: 2V ≤ V_{IN} ≤ 5V

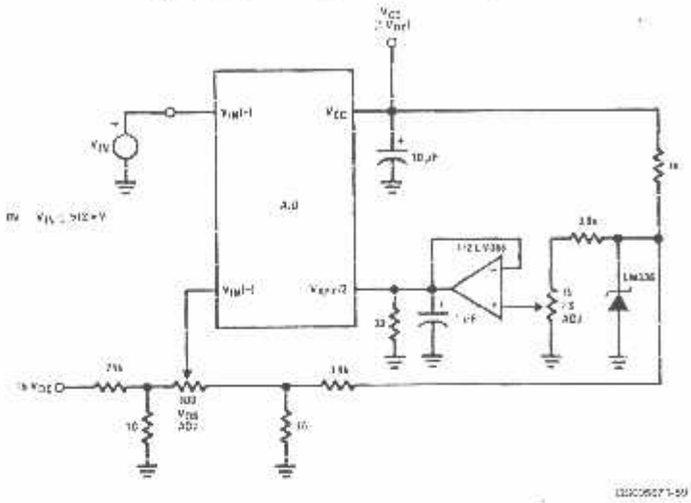


Span Adjust: 0V ≤ V_{IN} ≤ 3V



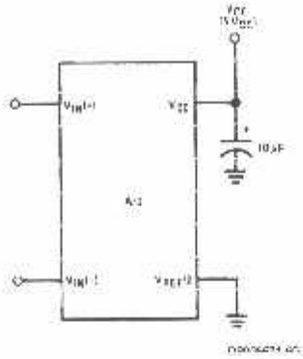
Typical Applications (Continued)

Directly Converting a Low-Level Signal



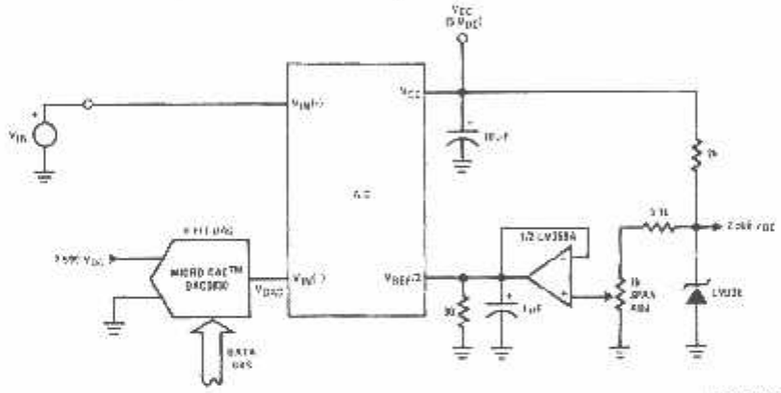
$V_{REF}/2 = 256$ mV

A µP Interfaced Comparator



For:
$V_{IN}(+) > V_{IN}(-)$
Output = FF HEX
For:
$V_{IN}(+) < V_{IN}(-)$
Output = 00 HEX

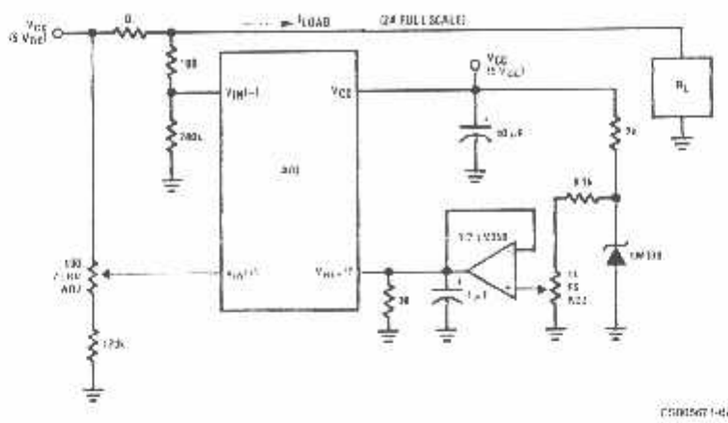
1 mV Resolution with µP Controlled Range



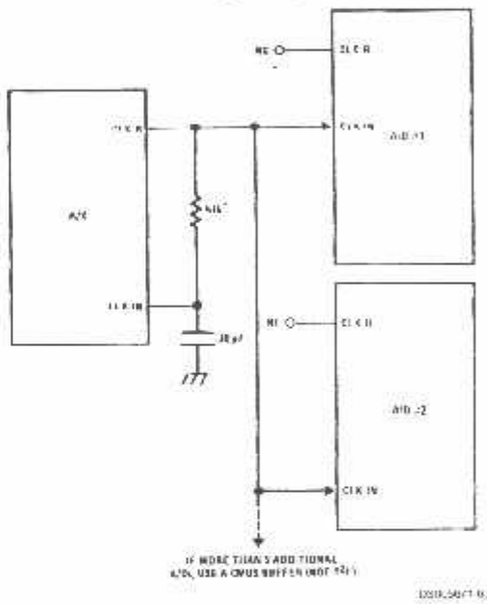
$V_{REF}/2 = 128$ mV
1 LSB = 1 mV
$V_{DAC} = V_{IN} (V_{DAC} = 256$ mV)
0 LI $V_{DAC} \leq 2.5$V

Typical Applications (Continued)

Digitizing a Current Flow

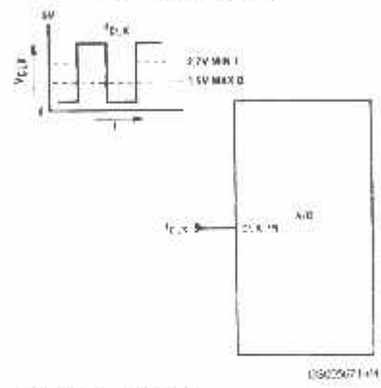


Self-Clocking Multiple A/Ds



* Use a large R value to reduce loading at CLK R output.

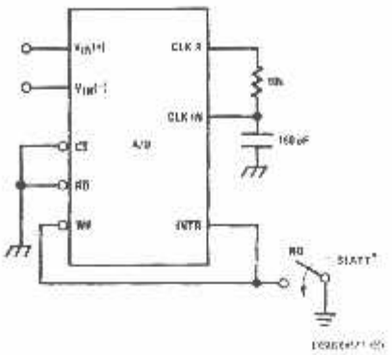
External Clocking



100 kHz ≤ f_{CLK} ≤ 1460 kHz

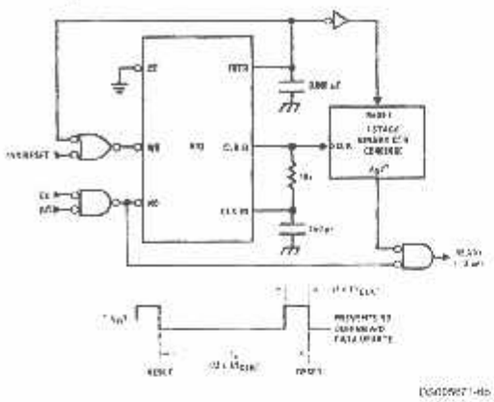
Typical Applications (Continued)

Self-Clocking in Free-Running Mode

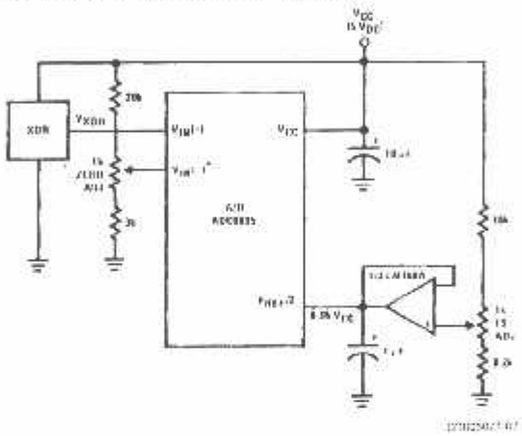


*After power-up, a momentary grounding of the $\overline{WR}$ input is needed to guarantee operation

µP Interface for Free-Running A/D

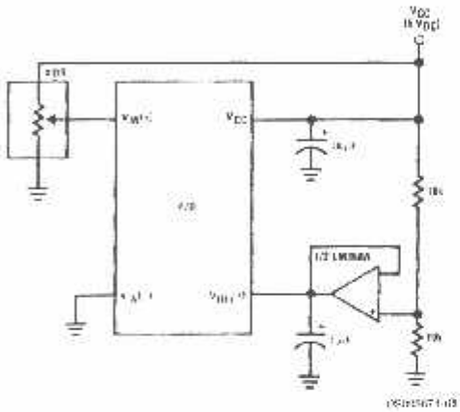


Operating with "Automotive" Ratiometric Transducers

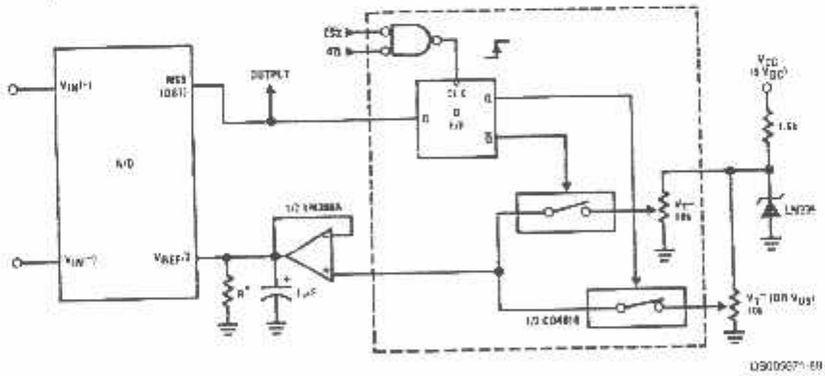


*$V_{IN}(-)=0.15\ V_{CC}$
15% of V_{CC} = V_{IOH}, 85% of V_{CC}

Ratiometric with $V_{REF}/2$ Forced



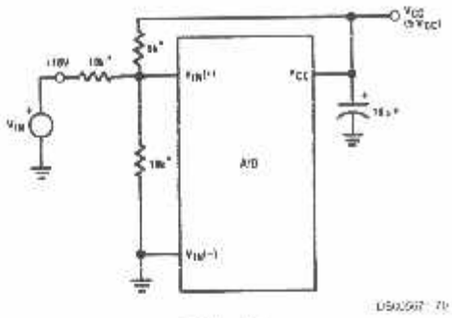
µP Compatible Differential-Input Comparator with Pre-Set V_{OS} (with or without Hysteresis)



*See Figure 5 to select R value
DB7="1" for $V_{IN}(+) > V_{IN}(-)+(V_{REF}/2)$
Omit circuitry within the dotted area if hysteresis is not needed

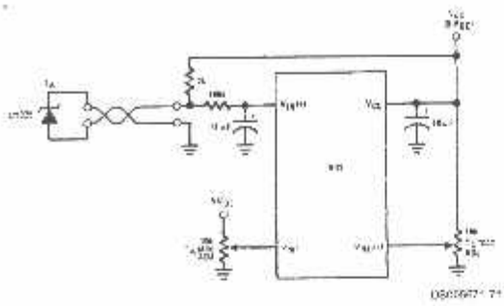
Typical Applications (Continued)

Handling ±10V Analog Inputs

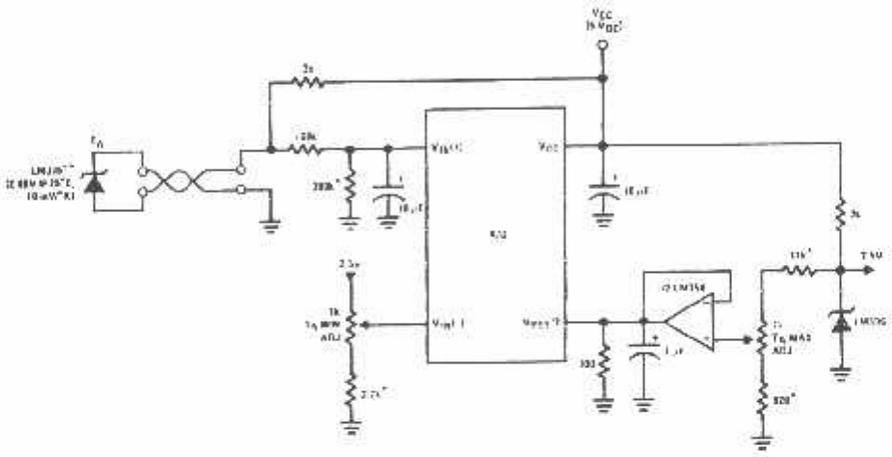


*Beckman Instruments #694-3-R10K resistor array

Low-Cost, µP Interfaced, Temperature-to-Digital Converter



µP Interfaced Temperature-to-Digital Converter

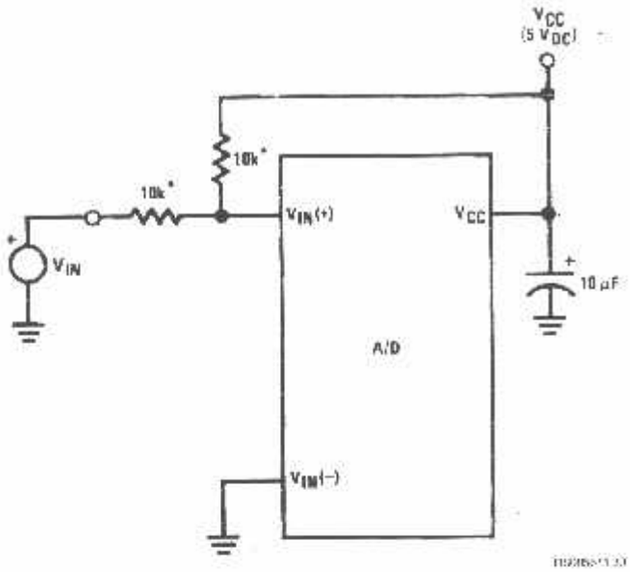


*Circuit values shown are for 0°C ≤ T_A ≤ +128°C

**Can calibrate each sensor to allow easy replacement, then A/D can be calibrated with a pre-set input voltage

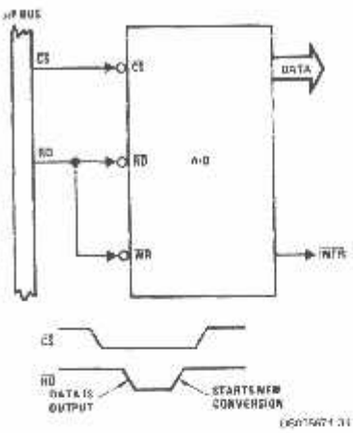
Typical Applications (Continued)

Handling ±5V Analog Inputs

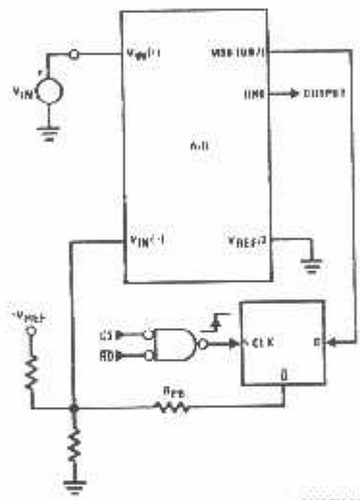


*Use precision instrument grade 0.1% R10K resistor only

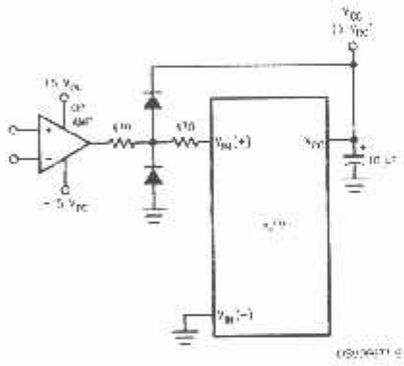
Read-Only Interface



µP Interfaced Comparator with Hysteresis



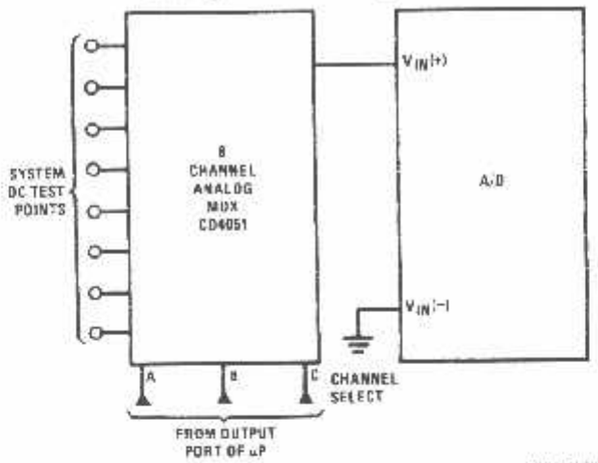
Protecting the Input



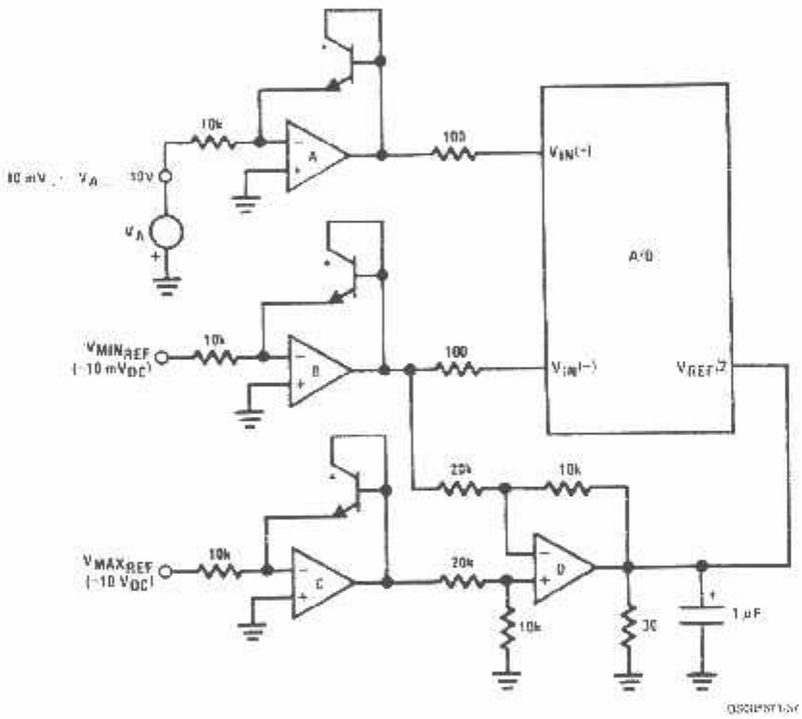
Diodes are 1N914

Typical Applications (Continued)

Analog Self-Test for a System



A Low-Cost, 3-Decade Logarithmic Converter

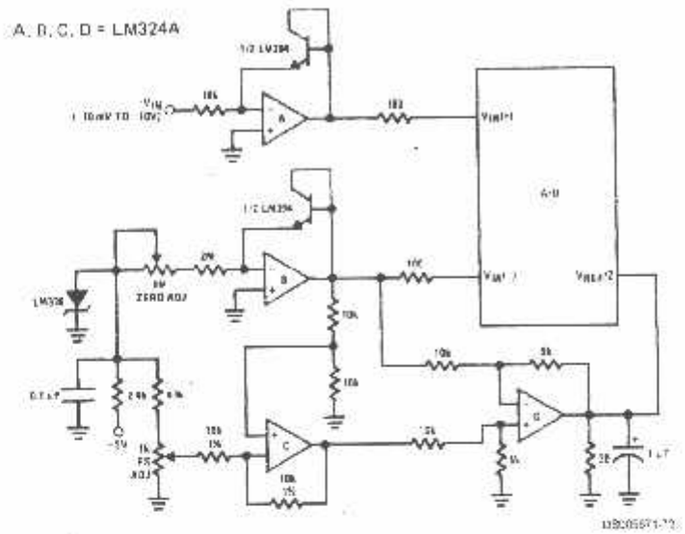


*LM389 transistors
A, B, C, D = LM324A quad op amp

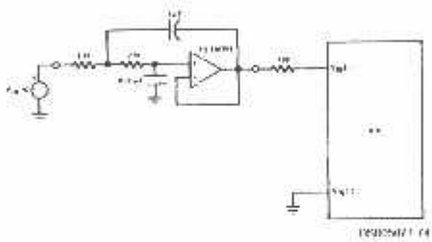
Typical Applications (Continued)

3-Decade Logarithmic A/D Converter

A, B, C, D = LM324A



Noise Filtering the Analog Input

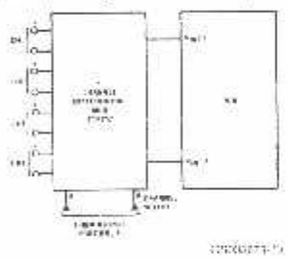


f_C = 20 Hz

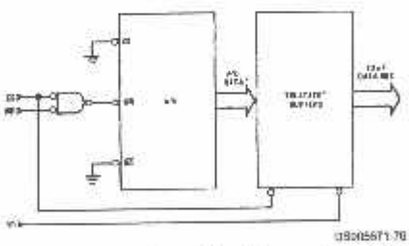
Uses Chebyshev implementation for steeper roll off unity-gain, 2nd order, low-pass filter

Adding a separate filter for each channel increases system response time if an analog multiplexer is used

Multiplexing Differential Inputs

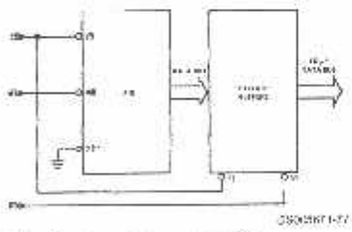


Output Buffers with A/D Data Enabled



*A/D output data is updated 1 CLK period prior to assertion of $\overline{INTR}$

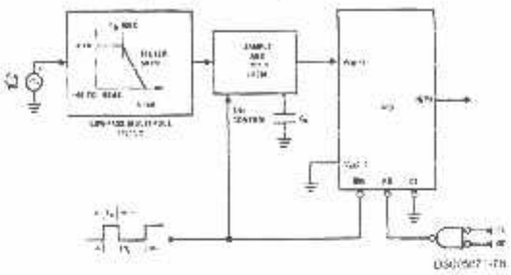
Increasing Bus Drive and/or Reducing Time on Bus



*Allows output data to set-up at falling edge of $\overline{CS}$

Typical Applications (Continued)

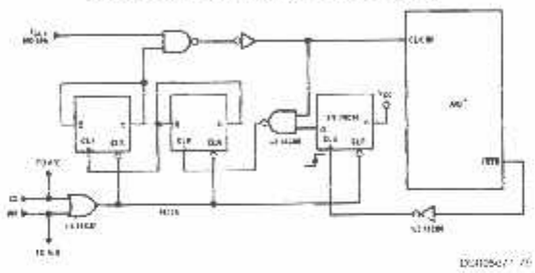
Sampling an AC Input Signal



Note 11: Oversample whenever possible (keep $f_S > 2(f_{-60})$) to eliminate input frequency folding (aliasing) and to allow for the skirt response of the filter.

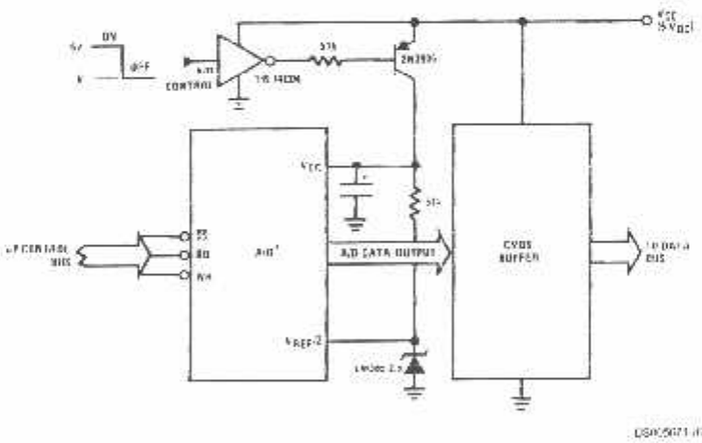
Note 12: Consider the amplitude errors which are introduced within the passband of the filter.

70% Power Savings by Clock Gating



(Complete shutdown takes ≈ 30 seconds.)

Power Savings by A/D and V_{REF} Shutdown



*Use ADC0801, 02, 03 or 05 for lowest power consumption.

Note: Logic inputs can be driven to V_{CC} with A/D supply at zero volts.

Buffer prevents data bus from overdriving output of A/D when in shutdown mode.

Functional Description

1.0 UNDERSTANDING A/D ERROR SPECS

A perfect A/D transfer characteristic (staircase waveform) is shown in *Figure 1*. The horizontal scale is analog input voltage and the particular points labeled are in steps of 1 LSB (19.53 mV with 2.5V tied to the $V_{REF}/2$ pin). The digital output codes that correspond to these inputs are shown as D−1, D, and D+1. For the perfect A/D, not only will center-value (A−1, A, A+1, ...) analog inputs produce the correct output digital codes, but also each riser (the transitions between adjacent output codes) will be located ±½ LSB away from each center-value. As shown, the risers are ideal and have no width. Correct digital output codes will be provided for a range of analog input voltages that extend

Functional Description (Continued)

±½ LSB from the ideal center-values. Each tread (the range of analog input voltage that provides the same digital output code) is therefore 1 LSB wide.

Figure 2 shows a worst case error plot for the ADC0801. All center-valued inputs are guaranteed to produce the correct output codes and the adjacent risers are guaranteed to be no closer to the center-value points than ±¼ LSB. In other words, if we apply an analog input equal to the center-value ±¼ LSB, *we guarantee* that the A/D will produce the correct digital code. The maximum range of the position of the code transition is indicated by the horizontal arrow and it is guaranteed to be no more than ½ LSB.

The error curve of *Figure 3* shows a worst case error plot for the ADC0802. Here we guarantee that if we apply an analog input equal to the LSB analog voltage center-value the A/D will produce the correct digital code.

Next to each transfer function is shown the corresponding error plot. Many people may be more familiar with error plots than transfer functions. The analog input voltage to the A/D is provided by either a linear ramp or by the discrete output steps of a high resolution DAC. Notice that the error is continuously displayed and includes the quantization uncertainty of the A/D. For example the error at point 1 of *Figure 1* is +½ LSB because the digital code appeared ½ LSB in advance of the center-value of the tread. The error plots always have a constant negative slope and the abrupt upside steps are always 1 LSB in magnitude.

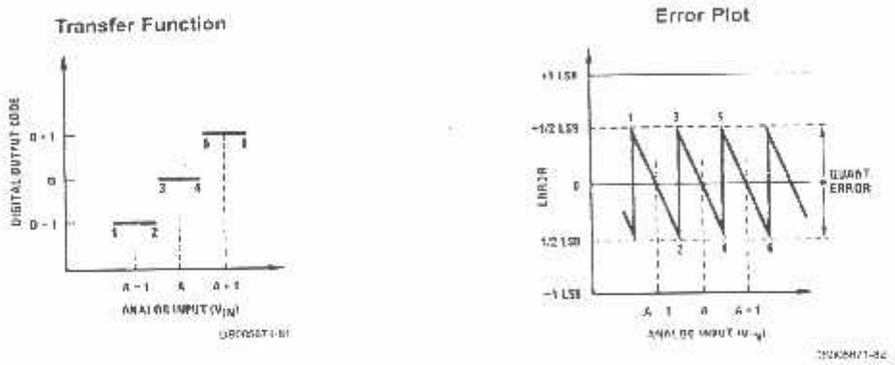


FIGURE 1. Clarifying the Error Specs of an A/D Converter Accuracy=±0 LSB: A Perfect A/D

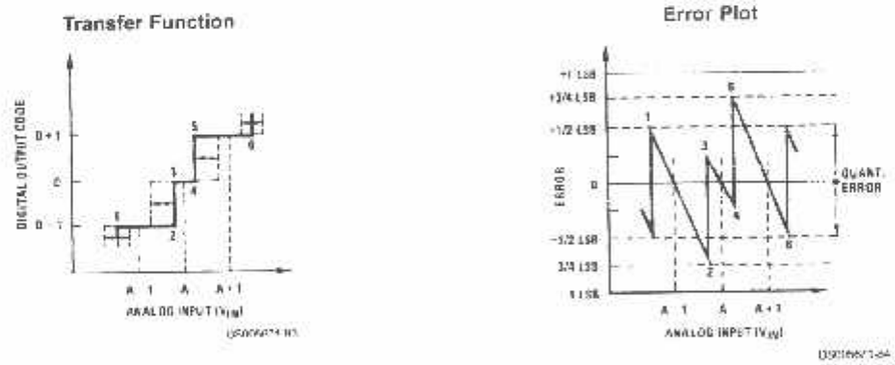


FIGURE 2. Clarifying the Error Specs of an A/D Converter Accuracy=±¼ LSB

Functional Description (Continued)

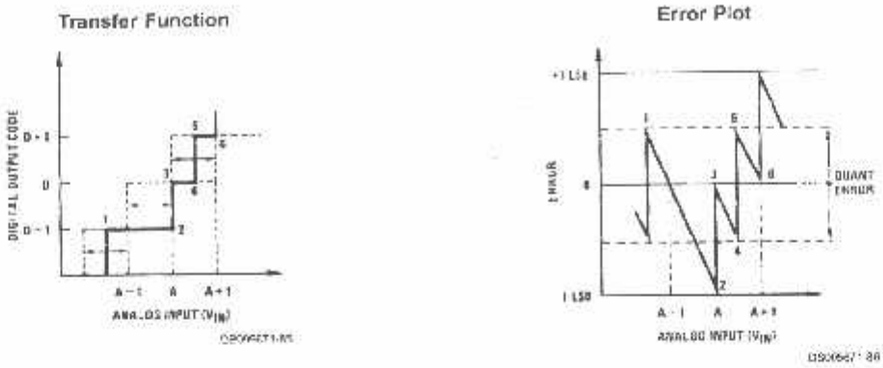


FIGURE 3. Clarifying the Error Specs of an A/D Converter
Accuracy=±½ LSB

2.0 FUNCTIONAL DESCRIPTION

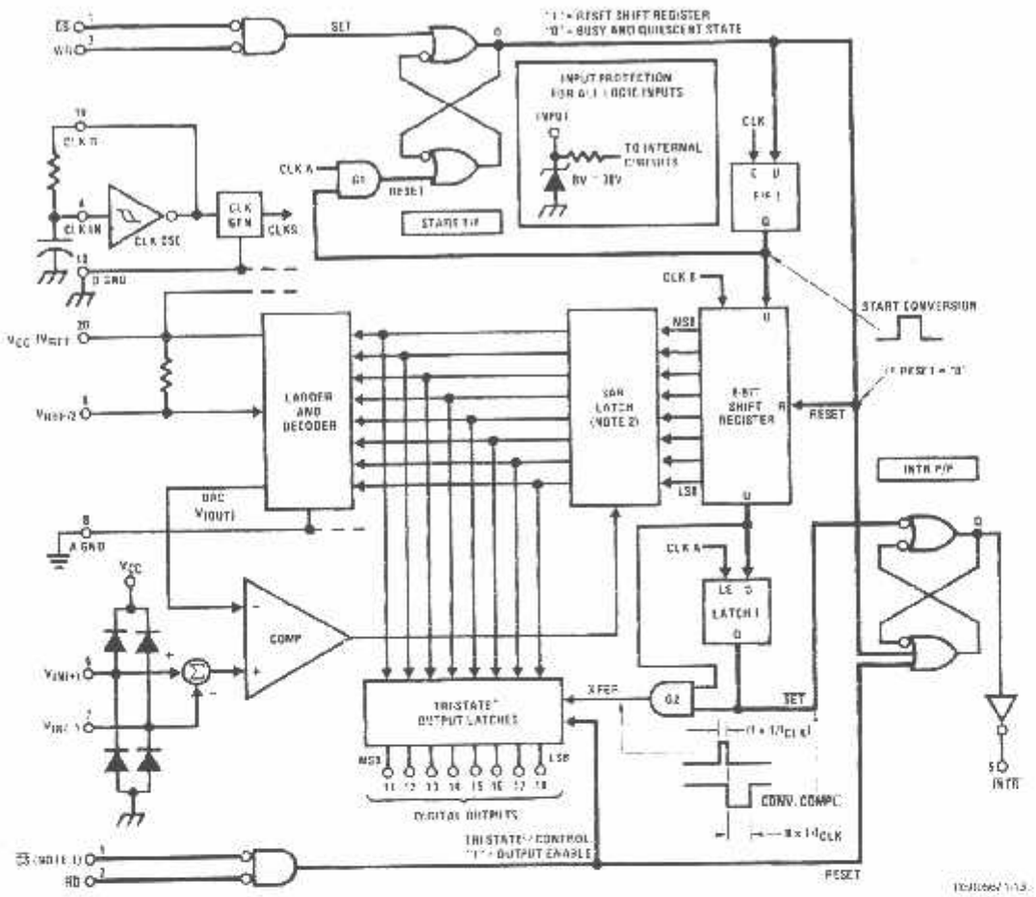
The ADC0801 series contains a circuit equivalent of the 256R network. Analog switches are sequenced by successive approximation logic to match the analog difference input voltage [$V_{IN}(+) - V_{IN}(-)$] to a corresponding tap on the R network. The most significant bit is tested first and after 8 comparisons (64 clock cycles) a digital 8-bit binary code (1111 1111 = full-scale) is transferred to an output latch and then an interrupt is asserted ($\overline{INTR}$ makes a high-to-low transition). A conversion in process can be interrupted by issuing a second start command. The device may be operated in the free-running mode by connecting $\overline{INTR}$ to the $\overline{WR}$ input with $\overline{CS}$ =0. To ensure start-up under all possible conditions, an external $\overline{WR}$ pulse is required during the first power-up cycle.

On the high-to-low transition of the $\overline{WR}$ input the internal SAR latches and the shift register stages are reset. As long as the $\overline{CS}$ input and $\overline{WR}$ input remain low, the A/D will remain in a reset state. *Conversion will start from 1 to 8 clock periods after at least one of these inputs makes a low to high transition.*

A functional diagram of the A/D converter is shown in *Figure 4*. All of the package pinouts are shown and the major logic control paths are drawn in heavier weight lines.

The converter is started by having $\overline{CS}$ and $\overline{WR}$ simultaneously low. This sets the start flip-flop (F/F) and the resulting "1" level resets the 8-bit shift register, resets the interrupt ($\overline{INTR}$) F/F and inputs a "1" to the D flop, F/F1, which is at the input end of the 8-bit shift register. Internal clock signals then transfer this "1" to the Q output of F/F1. The AND gate, G1, combines this "1" output with a clock signal to provide a reset signal to the start F/F. If the set signal is no longer present (either $\overline{WR}$ or $\overline{CS}$ is a "1") the start F/F is reset and the 8-bit shift register then can have the "1" clocked in, which starts the conversion process. If the set signal were to still be present, this reset pulse would have no effect (both outputs of the start F/F would momentarily be at a "1" level) and the 8-bit shift register would continue to be held in the reset mode. This logic therefore allows for wide $\overline{CS}$ and $\overline{WR}$ signals and the converter will start after at least one of these signals returns high and the internal clocks again provide a reset signal for the start F/F.

Functional Description (Continued)



Note 13: $\overline{CS}$ shown twice for clarity.

Note 14: SAR = Successive Approximation Register

FIGURE 4. Block Diagram

After the "1" is clocked through the 8-bit shift register (which completes the SAR search) it appears as the input to the D-type latch, LATCH 1. As soon as this "1" is output from the shift register, the AND gate, G2, causes the new digital word to transfer to the TRI-STATE output latches. When LATCH 1 is subsequently enabled, the Q output makes a high-to-low transition which causes the INTR F/F to set. An inverting buffer then supplies the $\overline{INTR}$ input signal.

Note that this $\overline{SET}$ control of the INTR F/F remains low for 3 of the external clock periods (as the internal clocks run at ¼ of the frequency of the external clock). If the data output is continuously enabled ($\overline{CS}$ and $\overline{RD}$ both held low), the $\overline{INTR}$ output will still signal the end of conversion (by a high-to-low transition), because the $\overline{SET}$ input can control the Q output of the INTR F/F even though the RESET input is constantly at a "1" level in this operating mode. This $\overline{INTR}$ output will therefore stay low for the duration of the $\overline{SET}$ signal, which is 8 periods of the external clock frequency (assuming the A/D is not started during this interval).

When operating in the free-running or continuous conversion mode ($\overline{INTR}$ pin tied to $\overline{WR}$ and $\overline{CS}$ wired low—see also section 2.8), the START F/F is SET by the high-to-low transition of the $\overline{INTR}$ signal. This resets the SHIFT REGISTER which causes the input to the D-type latch, LATCH 1, to go low. As the latch enable input is still present, the $\overline{Q}$ output will go high, which then allows the INTR F/F to be RESET. This reduces the width of the resulting $\overline{INTR}$ output pulse to only a few propagation delays (approximately 300 ns).

When data is to be read, the combination of both $\overline{CS}$ and $\overline{RD}$ being low will cause the INTR F/F to be reset and the TRI-STATE output latches will be enabled to provide the 8-bit digital outputs.

2.1 Digital Control Inputs

The digital control inputs ($\overline{CS}$, $\overline{RD}$, and $\overline{WR}$) meet standard I^2L logic voltage levels. These signals have been renamed when compared to the standard A/D Start and Output Enable labels. In addition, these inputs are active low to allow an easy interface to microprocessor control busses. For non-microprocessor based applications, the $\overline{CS}$ input (pin 1) can be grounded and the standard A/D Start function is obtained by an active low pulse applied at the $\overline{WR}$ input (pin 3) and the Output Enable function is caused by an active low pulse at the $\overline{RD}$ input (pin 2).

Functional Description (Continued)

2.2 Analog Differential Voltage Inputs and Common-Mode Rejection

This A/D has additional applications flexibility due to the analog differential voltage input. The $V_{IN}(-)$ input (pin 7) can be used to automatically subtract a fixed voltage value from the input reading (tare correction). This is also useful in 4 mA–20 mA current loop conversion. In addition, common-mode noise can be reduced by use of the differential input.

The time interval between sampling $V_{IN}(+)$ and $V_{IN}(-)$ is 4-½ clock periods. The maximum error voltage due to this slight time difference between the input voltage samples is given by:

$$\Delta V_a(MAX) = (V_P)(2\pi f_{cm})\left(\frac{4.5}{f_{CLK}}\right)$$

where:

ΔV_a is the error voltage due to sampling delay

V_P is the peak value of the common-mode voltage

f_{cm} is the common-mode frequency

As an example, to keep this error to ¼ LSB (⊐5 mV) when operating with a 60 Hz common-mode frequency, f_{cm}, and using a 640 kHz A/D clock, f_{CLK}, would allow a peak value of the common-mode voltage, V_P, which is given by:

$$V_P = \frac{[\Delta V_{a(MAX)}(f_{CLK})]}{(2\pi f_{cm})(4.5)}$$

or

$$V_P = \frac{(5 \times 10^{-3})(640 \times 10^3)}{(6.28)(60)(4.5)}$$

which gives

$V_P = 1.9V$

The allowed range of analog input voltages usually places more severe restrictions on input common-mode noise levels.

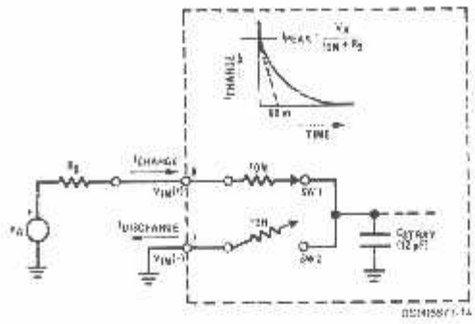
An analog input voltage with a reduced span and a relatively large zero offset can be handled easily by making use of the differential input (see section 2.4 Reference Voltage).

2.3 Analog Inputs

2.3.1 Input Current

Normal Mode

Due to the internal switching action, displacement currents will flow at the analog inputs. This is due to on-chip stray capacitance to ground as shown in *Figure 5*.



r_{ON} of SW 1 and SW 2 = 5 kΩ
$r_{ON} C_{STRAY}$ = 5 kΩ x 12 pF = 60 ns

FIGURE 5. Analog Input Impedance

The voltage on this capacitance is switched and will result in currents entering the $V_{IN}(+)$ input pin and leaving the $V_{IN}(-)$ input which will depend on the analog differential input voltage levels. These current transients occur at the leading edge of the internal clocks. They rapidly decay and *do not cause errors* as the on-chip comparator is strobed at the end of the clock period.

Fault Mode

If the voltage source applied to the $V_{IN}(+)$ or $V_{IN}(-)$ pin exceeds the allowed operating range of V_{CC}+50 mV, large input currents can flow through a parasitic diode to the V_{CC} pin. If these currents can exceed the 1 mA max allowed spec, an external diode (1N914) should be added to bypass this current to the V_{CC} pin (with the current bypassed with this diode, the voltage at the $V_{IN}(+)$ pin can exceed the V_{CC} voltage by the forward voltage of this diode).

2.3.2 Input Bypass Capacitors

Bypass capacitors at the inputs will average these charges and cause a DC current to flow through the output resistances of the analog signal sources. This charge pumping action is worse for continuous conversions with the $V_{IN}(+)$ input voltage at full-scale. For continuous conversions with a 640 kHz clock frequency with the $V_{IN}(+)$ input at 5V, this DC current is at a maximum of approximately 5 µA. Therefore, *bypass capacitors should not be used at the analog inputs or the $V_{REF}/2$ pin* for high resistance sources (> 1 kΩ). If input bypass capacitors are necessary for noise filtering and high source resistance is desirable to minimize capacitor size, the detrimental effects of the voltage drop across this input resistance, which is due to the average value of the input current, can be eliminated with a full-scale adjustment while the given source resistor and input bypass capacitor are both in place. This is possible because the average value of the input current is a precise linear function of the differential input voltage.

2.3.3 Input Source Resistance

Large values of source resistance where an input bypass capacitor is not used, *will not cause errors* as the input currents settle out prior to the comparison time. If a low pass filter is required in the system, use a low valued series resistor (⊐1 kΩ) for a passive RC section or add an op amp RC active low pass filter. For low source resistance applications, (⊐1 kΩ), a 0.1 µF bypass capacitor at the inputs will prevent noise pickup due to series lead inductance of a long

January 2000

National Semiconductor

LM158/LM258/LM358/LM2904
Low Power Dual Operational Amplifiers

General Description

The LM158 series consists of two independent, high gain, internally frequency compensated operational amplifiers which were designed specifically to operate from a single power supply over a wide range of voltages. Operation from split power supplies is also possible and the low power supply current drain is independent of the magnitude of the power supply voltage.

Application areas include transducer amplifiers, dc gain blocks and all the conventional op amp circuits which now can be more easily implemented in single power supply systems. For example, the LM158 series can be directly operated off of the standard +5V power supply voltage which is used in digital systems and will easily provide the required interface electronics without requiring the additional ±15V power supplies.

The LM358 is also available in a chip sized package (8-Bump micro SMD) using National's micro SMD package technology.

Unique Characteristics

- In the linear mode the input common-mode voltage range includes ground and the output voltage can also swing to ground, even though operated from only a single power supply voltage.
- The unity gain cross frequency is temperature compensated.
- The input bias current is also temperature compensated.

Advantages

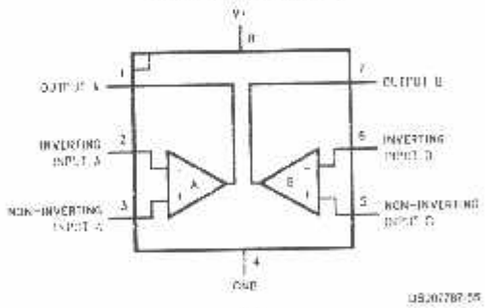
- Two internally compensated op amps
- Eliminates need for dual supplies
- Allows direct sensing near GND and V_{OUT} also goes to GND
- Compatible with all forms of logic
- Power drain suitable for battery operation
- Pin-out same as LM1558/LM1458 dual op amp

Features

- Available in 8-Bump micro SMD chip sized package, (See AN-1112)
- Internally frequency compensated for unity gain
- Large dc voltage gain: 100 dB
- Wide bandwidth (unity gain): 1 MHz (temperature compensated)
- Wide power supply range:
  - Single supply: 3V to 32V
  - or dual supplies: ±1.5V to ±16V
- Very low supply current drain (500 µA)—essentially independent of supply voltage
- Low input offset voltage: 2 mV
- Input common-mode voltage range includes ground
- Differential input voltage range equal to the power supply voltage
- Large output voltage swing: 0V to V+ − 1.5V

Connection Diagrams

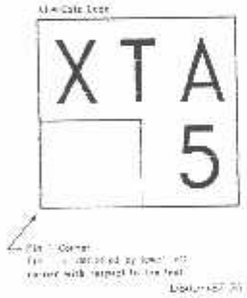
8-Bump micro SMD



DS007787-55

Top View
(Bump Side Down)

micro SMD Marking Orientation

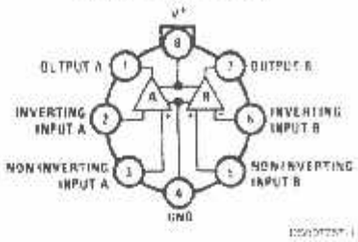


Bumps are numbered counter-clockwise

Top View

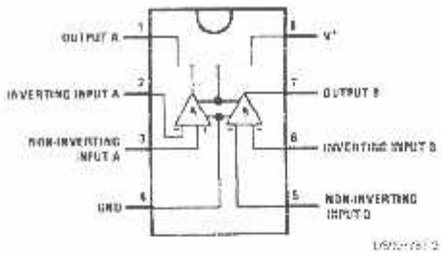
Connection Diagrams (Continued)

Metal Can Package



Top View

DIP/SO Package



Top View

Ordering Information

Package	Temperature Range				NSC Drawing
	−55°C to 125°C	−25°C to 85°C	0°C to 70°C	−40°C to 85°C	
SO-8			LM358AM LM358M	LM2904M	M08A
8-Pin Molded DIP			LM358AN LM358N	LM2904N	N08E
8-Pin Ceramic DIP	LM158AJ/883(Note 1) LM158J/883(Note 1) LM158J LM158AJLQML(Note 2) LM158AJQMLV(Note 2)				J08A
TO-5, 8-Pin Metal Can	LM158AH/883(Note 1) LM158H/883(Note 1) LM158AH LM158H LM158AHLQML(Note 2) LM158AHLQMLV(Note 2)	LM258H	LM358H		H08C
8-Bump micro SMD			LM358BP LM358BPX		BPA08AAA

Note 1: LM158 is available per SVID #5962-8771001.
LM158A is available per SMD #5962-8771002.
Note 2: See STD Mil DWG 5962L87710 for Radiation Tolerant Devices.

Absolute Maximum Ratings (Note 11)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

	LM158/LM258/LM358 LM158A/LM258A/LM358A	LM2904
Supply Voltage, V^+	32V	26V
Differential Input Voltage	32V	26V
Input Voltage	−0.3V to +32V	−0.3V to +26V
Power Dissipation (Note 3)		
Molded DIP	830 mW	830 mW
Metal Can	550 mW	
Small Outline Package (M)	530 mW	530 mW
micro SMD	435mW	
Output Short-Circuit to GND		
(One Amplifier) (Note 4)		
$V^+ \leq 15V$ and $T_A = 25°C$	Continuous	Continuous
Input Current ($V_{IN} < -0.3V$) (Note 5)	50 mA	50 mA
Operating Temperature Range		
LM358	0°C to +70°C	−40°C to +85°C
LM258	−25°C to +85°C	
LM158	−55°C to +125°C	
Storage Temperature Range	−65°C to +150°C	−65°C to +150°C
Lead Temperature, DIP		
(Soldering, 10 seconds)	260°C	260°C
Lead Temperature, Metal Can		
(Soldering, 10 seconds)	300°C	300°C
Soldering Information		
Dual-In-Line Package		
Soldering (10 seconds)	260°C	260°C
Small Outline Package		
Vapor Phase (60 seconds)	215°C	215°C
Infrared (15 seconds)	220°C	220°C
See AN-450 "Surface Mounting Methods and Their Effect on Product Reliability" for other methods of soldering surface mount devices.		
ESD Tolerance (Note 12)	250V	250V

Electrical Characteristics

$V^+ = +5.0V$, unless otherwise stated

Parameter	Conditions	LM158A			LM358A			LM158/LM258			Units
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
Input Offset Voltage	(Note 7), $T_A = 25°C$		1	2		2	3		2	5	mV
Input Bias Current	$I_{IN(+)}$ or $I_{IN(-)}$, $T_A = 25°C$, $V_{CM} = 0V$, (Note 8)		20	50		45	100		45	150	nA
Input Offset Current	$I_{IN(+)} - I_{IN(-)}$, $V_{CM} = 0V$, $T_A = 25°C$		2	10		5	30		3	30	nA
Input Common-Mode Voltage Range	$V^+ = 30V$, (Note 9) (LM2904, $V^+ = 26V$), $T_A = 25°C$	0		$V^+-1.5$	0		$V^+-1.5$	0		$V^+-1.5$	V
Supply Current	Over Full Temperature Range $R_L = \infty$ on All Op Amps										
	$V^+ = 30V$ (LM2904 $V^+ = 26V$)		1	2		1	2		1	2	mA
	$V^+ = 5V$		0.5	1.2		0.5	1.2		0.5	1.2	mA

Electrical Characteristics

V^+ = +5.0V, unless otherwise stated

Parameter	Conditions	LM358			LM2904			Units
		Min	Typ	Max	Min	Typ	Max	
Input Offset Voltage	(Note 7), T_A = 25°C		2	7		2	7	mV
Input Bias Current	$I_{IN(+)}$ or $I_{IN(-)}$, T_A = 25°C, V_{CM} = 0V, (Note 8)		45	250		45	250	nA
Input Offset Current	$I_{IN(+)} - I_{IN(-)}$, V_{CM} = 0V, T_A = 25°C		5	50		5	50	nA
Input Common-Mode Voltage Range	V^+ = 30V, (Note 9) (LM2904, V^+ = 26V), T_A = 25°C	0		$V^+-1.5$	0		$V^+-1.5$	V
Supply Current	Over Full Temperature Range, $R_L = \infty$ on All Op Amps							
	V^+ = 30V (LM2904 V^+ = 26V)		1	2		1	2	mA
	V^+ = 5V		0.5	1.2		0.5	1.2	mA

Electrical Characteristics

V^+ = +5.0V, (Note 6), unless otherwise stated

Parameter		Conditions	LM158A			LM358A			LM158/LM258			Units
			Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
Large Signal Voltage Gain		V^+ = 15V, T_A = 25°C, $R_L \geq 2\ k\Omega$, (For V_O = 1V to 11V)	50	100		25	100		50	100		V/mV
Common-Mode Rejection Ratio		T_A = 25°C, V_{CM} = 0V to $V^+-1.5V$	70	85		65	85		70	85		dB
Power Supply Rejection Ratio		V^+ = 5V to 30V (LM2904, V^+ = 5V to 26V), T_A = 25°C	65	100		65	100		65	100		dB
Amplifier-to-Amplifier Coupling		f = 1 kHz to 20 kHz, T_A = 25°C (Input Referred), (Note 10)		−120			−120			−120		dB
Output Current	Source	V_{IN}^- = 1V, V_{IN}^+ = 0V, V^+ = 15V, V_O = 2V, T_A = 25°C	20	40		20	40		20	40		mA
	Sink	V_{IN}^- = 1V, V_{IN}^+ = 0V, V^+ = 15V, T_A = 25°C, V_O = 2V	10	20		10	20		10	20		mA
		V_{IN}^- = 1V, V_{IN}^+ = 0V, T_A = 25°C, V_O = 200 mV, V^+ = 15V	12	50		12	50		12	50		µA
Short Circuit to Ground		T_A = 25°C, (Note 4), V^+ = 15V		40	60		40	60		40	60	mA
Input Offset Voltage		(Note 7)			4			5			7	mV
Input Offset Voltage Drift		R_S = 0Ω		7	15		7	20		7		µV/°C
Input Offset Current		$I_{IN(+)} - I_{IN(-)}$			30			75			100	nA
Input Offset Current Drift		R_S = 0Ω		10	200		10	300		10		pA/°C
Input Bias Current		$I_{IN(-)}$ or $I_{IN(+)}$		40	100		40	200		40	300	nA
Input Common-Mode Voltage Range		V^+ = 30 V, (Note 9) (LM2904, V^+ = 26V)	0		V^+-2	0		V^+-2	0		V^+-2	V

Electrical Characteristics (Continued)

V^+ = +5.0V, (Note 6), unless otherwise stated

Parameter		Conditions		LM158A			LM358A			LM158/LM258			Units
				Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
Large Signal Voltage Gain		V^+ = +15V (V_O = 1V to 11V) $R_L \geq 2\ k\Omega$		25			15			25			V/mV
Output Voltage	V_{OH}	V^+ = +30V	R_L = 2 kΩ	26			26			26			V
		(LM2904, V^+ = 26V)	R_L = 10 kΩ	27	28		27	28		27	28		V
Swing	V_{OL}	V^+ = 5V, R_L = 10 kΩ			5	20		5	20		5	20	mV
Output Current	Source	V_{IN}^+ = +1V, V_{IN}^- = 0V, V^+ = 15V, V_O = 2V		10	20		10	20		10	20		mA
	Sink	V_{IN}^- = +1V, V_{IN}^+ = 0V, V^+ = 15V, V_O = 2V		10	15		5	8		5	8		mA

Electrical Characteristics

V^+ = +5.0V, (Note 6), unless otherwise stated

Parameter		Conditions	LM358			LM2904			Units
			Min	Typ	Max	Min	Typ	Max	
Large Signal Voltage Gain		V^+ = 15V, T_A = 25°C, $R_L \geq 2\ k\Omega$, (For V_O = 1V to 11V)	25	100		25	100		V/mV
Common-Mode Rejection Ratio		T_A = 25°C, V_{CM} = 0V to V^+−1.5V	65	85		50	70		dB
Power Supply Rejection Ratio		V^+ = 5V to 30V (LM2904, V^+ = 5V to 26V), T_A = 25°C	65	100		50	100		dB
Amplifier-to-Amplifier Coupling		f = 1 kHz to 20 kHz, T_A = 25°C (Input Referred), (Note 10)		−120			−120		dB
Output Current	Source	V_{IN}^+ = 1V, V_{IN}^- = 0V, V^+ = 15V, V_O = 2V, T_A = 25°C	20	40		20	40		mA
	Sink	V_{IN}^- = 1V, V_{IN}^+ = 0V, V^+ = 15V, T_A = 25°C, V_O = 2V	10	20		10	20		mA
		V_{IN}^- = 1V, V_{IN}^+ = 0V, T_A = 25°C, V_O = 200 mV, V^+ = 15V	12	50		12	50		µA
Short Circuit to Ground		T_A = 25°C, (Note 4), V^+ = 15V		40	60		40	60	mA
Input Offset Voltage		(Note 7)			9			10	mV
Input Offset Voltage Drift		R_S = 0Ω		7			7		µV/°C
Input Offset Current		$I_{IN(+)} - I_{IN(-)}$			150		45	200	nA
Input Offset Current Drift		R_S = 0Ω		10			10		pA/°C
Input Bias Current		$I_{IN(+)}$ or $I_{IN(-)}$		40	500		40	500	nA
Input Common-Mode Voltage Range		V^+ = 30 V, (Note 9) (LM2904, V^+ = 26V)	0		V^+−2	0		V^+ −2	V

Electrical Characteristics (Continued)

V^+ = +5.0V, (Note 6), unless otherwise stated

Parameter		Conditions		LM358			LM2904			Units
				Min	Typ	Max	Min	Typ	Max	
Large Signal Voltage Gain		V^+ = +15V (V_O = 1V to 11V) $R_L \geq 2\ k\Omega$		15			15			V/mV
Output Voltage	V_{OH}	V^+ = +30V	R_L = 2 kΩ	26			22			V
		(LM2904, V^+ = 26V)	R_L = 10 kΩ	27	28		23	24		V
Swing	V_{OL}	V^+ = 5V, R_L = 10 kΩ			5	20		5	100	mV
Output Current	Source	V_{IN}^+ = +1V, V_{IN}^- = 0V, V^+ = 15V, V_O = 2V		10	20		10	20		mA
	Sink	V_{IN}^- = +1V, V_{IN}^+ = 0V, V^+ = 15V V_O = 2V		5	8		5	8		mA

Note 3: For operating at high temperatures, the LM358/LM358A, LM2904 must be derated based on a +125°C maximum junction temperature and a thermal resistance of 120°C/W for MDIP, 182°C/W for Metal Can, 189°C/W for Small Outline package, and 230°C/W for micro SMD, which applies for the device soldered in a printed circuit board, operating in a still air ambient. The LM258/LM258A and LM158/LM158A can be derated based on a +150°C maximum junction temperature. The dissipation is the total of both amplifiers — use external resistors, where possible, to allow the amplifier to saturate or to reduce the power which is dissipated in the integrated circuit.

Note 4: Short circuits from the output to V^+ can cause excessive heating and eventual destruction. When considering short circuits to ground, the maximum output current is approximately 40 mA independent of the magnitude of V^+. At values of supply voltage in excess of +15V, continuous short-circuits can exceed the power dissipation ratings and cause eventual destruction. Destructive dissipation can result from simultaneous shorts on all amplifiers.

Note 5: This input current will only exist when the voltage at any of the input leads is driven negative. It is due to the collector-base junction of the input PNP transistors becoming forward biased and thereby acting as input diode clamps. In addition to this diode action, there is also lateral NPN parasitic transistor action on the IC chip. This transistor action can cause the output voltages of the op amps to go to the V^+ voltage level (or to ground for a large overdrive) for the time duration that an input is driven negative. This is not destructive and normal output states will re-establish when the input voltage, which was negative, again returns to a value greater than −0.3V (at 25°C).

Note 6: These specifications are limited to −55°C ≤ T_A ≤ +125°C for the LM158/LM158A. With the LM258/LM258A, all temperature specifications are limited to −25°C ≤ T_A ≤ +85°C, the LM358/LM358A temperature specifications are limited to 0°C ≤ T_A ≤ +70°C, and the LM2904 specifications are limited to −40°C ≤ T_A ≤ +85°C.

Note 7: V_O = 1.4V, R_S = 0Ω with V^+ from 5V to 30V; and over the full input common-mode range (0V to V^+ −1.5V) at 25°C. For LM2904, V^+ from 5V to 26V.

Note 8: The direction of the input current is out of the IC due to the PNP input stage. This current is essentially constant, independent of the state of the output so no loading change exists on the input lines.

Note 9: The input common-mode voltage of either input signal voltage should not be allowed to go negative by more than 0.3V (at 25°C). The upper end of the common-mode voltage range is V^+ −1.5V (at 25°C), but either or both inputs can go to +32V without damage (+26V for LM2904), independent of the magnitude of V^+.

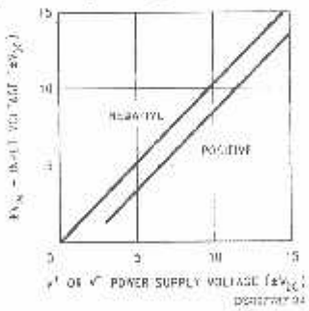
Note 10: Due to proximity of external components, ensure that coupling is not originating via stray capacitance between these external parts. This typically can be detected as this type of capacitance increases at higher frequencies.

Note 11: Refer to RETS158AX for LM158A military specifications and to RETS158X for LM158 military specifications.

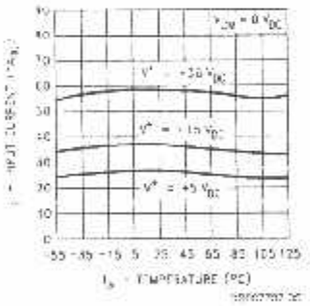
Note 12: Human body model, 1.5 kΩ in series with 100 pF.

Typical Performance Characteristics

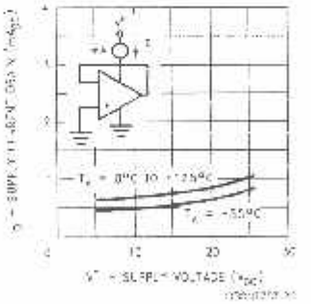
Input Voltage Range



Input Current

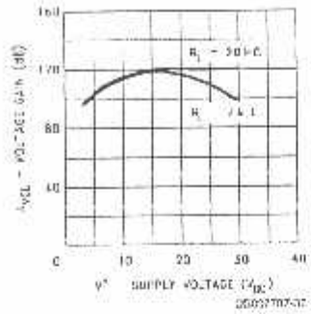


Supply Current

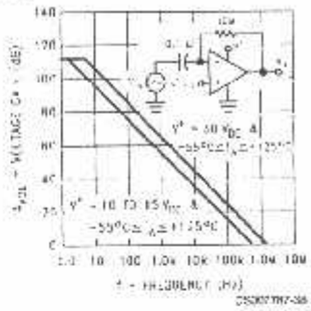


Typical Performance Characteristics (Continued)

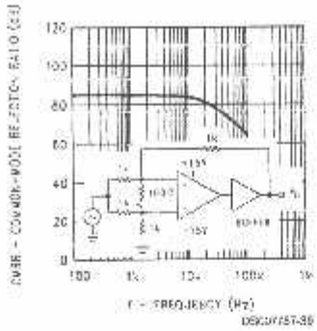
Voltage Gain



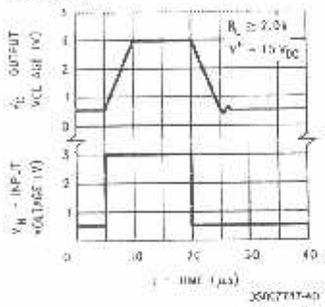
Open Loop Frequency Response



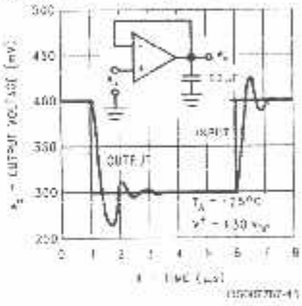
Common-Mode Rejection Ratio



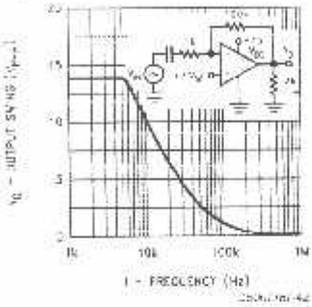
Voltage Follower Pulse Response



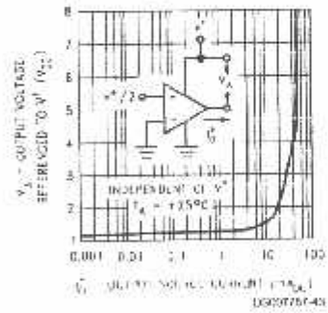
Voltage Follower Pulse Response (Small Signal)



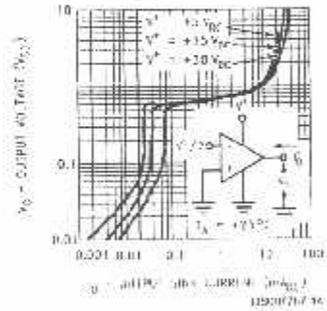
Large Signal Frequency Response



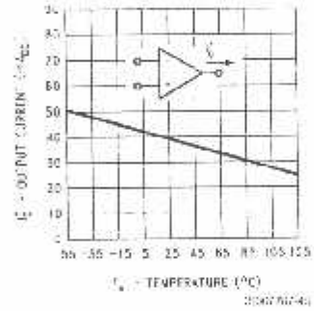
Output Characteristics Current Sourcing



Output Characteristics Current Sinking

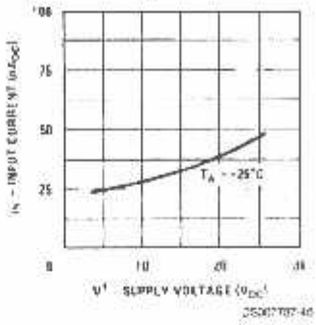


Current Limiting

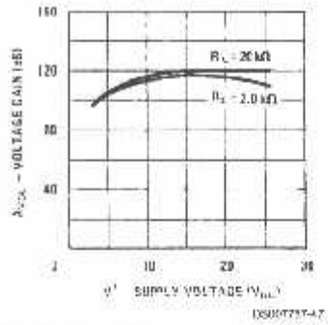


Typical Performance Characteristics (Continued)

Input Current (LM2902 only)



Voltage Gain (LM2902 only)



Application Hints

The LM158 series are op amps which operate with only a single power supply voltage, have true-differential inputs, and remain in the linear mode with an input common-mode voltage of 0 V_{DC}. These amplifiers operate over a wide range of power supply voltage with little change in performance characteristics. At 25°C amplifier operation is possible down to a minimum supply voltage of 2.3 V_{DC}.

Precautions should be taken to insure that the power supply for the integrated circuit never becomes reversed in polarity or that the unit is not inadvertently installed backwards in a test socket as an unlimited current surge through the resulting forward diode within the IC could cause fusing of the internal conductors and result in a destroyed unit.

Large differential input voltages can be easily accommodated and, as input differential voltage protection diodes are not needed, no large input currents result from large differential input voltages. The differential input voltage may be larger than V^+ without damaging the device. Protection should be provided to prevent the input voltages from going negative more than −0.3 V_{DC} (at 25°C). An input clamp diode with a resistor to the IC input terminal can be used.

To reduce the power supply current drain, the amplifiers have a class A output stage for small signal levels which converts to class B in a large signal mode. This allows the amplifiers to both source and sink large output currents. Therefore both NPN and PNP external current boost transistors can be used to extend the power capability of the basic amplifiers. The output voltage needs to raise approximately 1 diode drop above ground to bias the on-chip vertical PNP transistor for output current sinking applications.

For ac applications, where the load is capacitively coupled to the output of the amplifier, a resistor should be used from the output of the amplifier to ground to increase the class A bias current and prevent crossover distortion. Where the load is directly coupled, as in dc applications, there is no crossover distortion.

Capacitive loads which are applied directly to the output of the amplifier reduce the loop stability margin. Values of 50 pF can be accommodated using the worst-case non-inverting unity gain connection. Large closed loop gains or resistive isolation should be used if larger load capacitance must be driven by the amplifier.

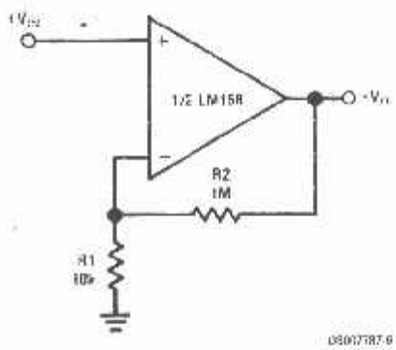
The bias network of the LM158 establishes a drain current which is independent of the magnitude of the power supply voltage over the range of 3 V_{DC} to 30 V_{DC}.

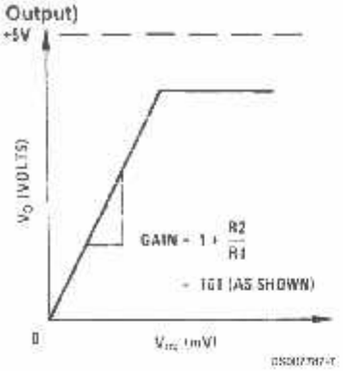
Output short circuits either to ground or to the positive power supply should be of short time duration. Units can be destroyed, not as a result of the short circuit current causing metal fusing, but rather due to the large increase in IC chip dissipation which will cause eventual failure due to excessive function temperatures. Putting direct short-circuits on more than one amplifier at a time will increase the total IC power dissipation to destructive levels, if not properly protected with external dissipation limiting resistors in series with the output leads of the amplifiers. The larger value of output source current which is available at 25°C provides a larger output current capability at elevated temperatures (see typical performance characteristics) than a standard IC op amp.

The circuits presented in the section on typical applications emphasize operation on only a single power supply voltage. If complementary power supplies are available, all of the standard op amp circuits can be used. In general, introducing a pseudo-ground (a bias voltage reference of $V^+/2$) will allow operation above and below this value in single power supply systems. Many application circuits are shown which take advantage of the wide input common-mode voltage range which includes ground. In most cases, input biasing is not required and input voltages which range to ground can easily be accommodated.

Typical Single-Supply Applications ($V^+ = 5.0\ V_{DC}$)

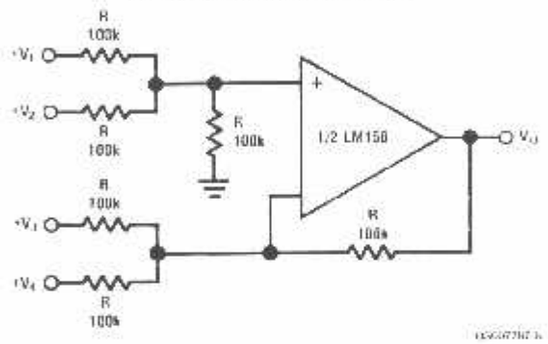
Non-Inverting DC Gain (0V Output)





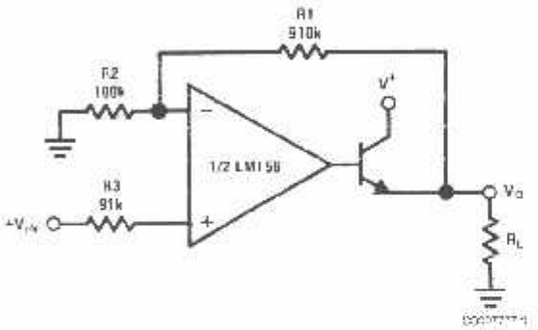
*R not needed due to temperature independent I_{IN}

DC Summing Amplifier
(V_{IN}'S ≥ 0 V_{DC} and V_O ≥ 0 V_{DC})



Where: $V_O = V_1 + V_2 - (V_3 + V_4)$
$(V_1 + V_2) \geq (V_3 + V_4)$ to keep $V_O \geq 0\ V_{DC}$

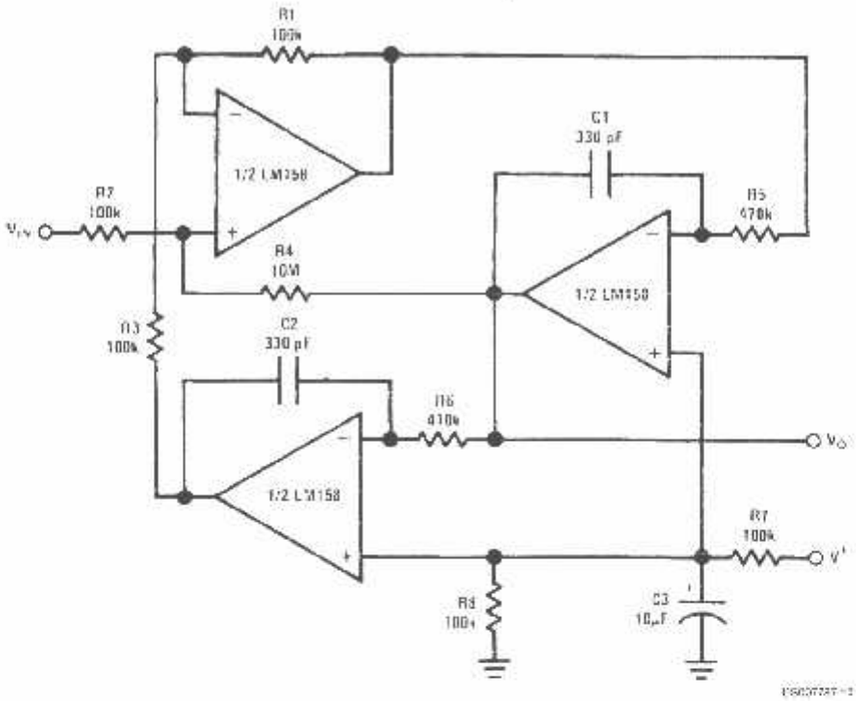
Power Amplifier



$V_O = 0\ V_{DC}$ for $V_{IN} = 0\ V_{DC}$
$A_V = 10$

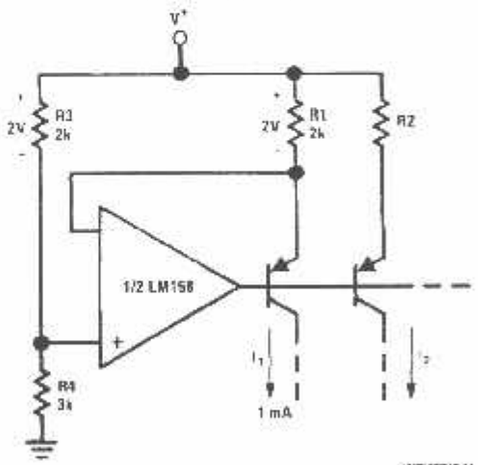
Typical Single-Supply Applications ($V^+ = 5.0\ V_{DC}$) (Continued)

"Bi-QUAD" RC Active Bandpass Filter



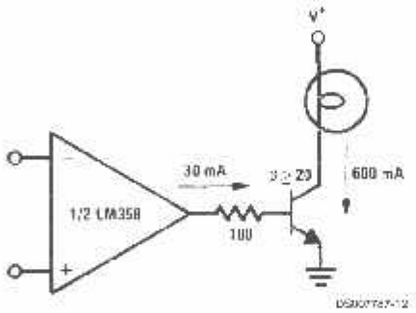
f_o = 1 kHz
Q = 50
A_v = 100 (40 dB)

Fixed Current Sources



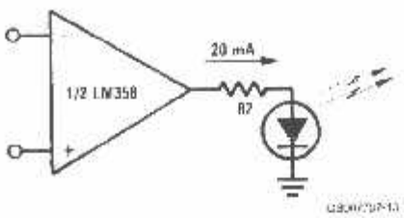
$$I_2 = \left(\frac{R1}{R2}\right) I_1$$

Lamp Driver

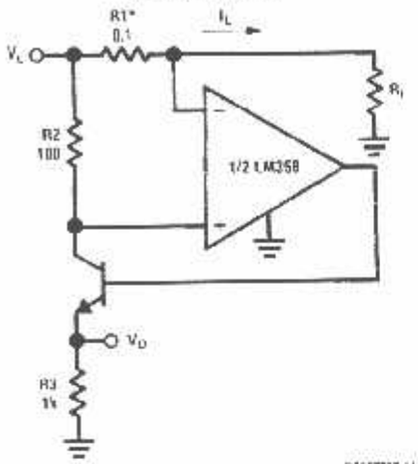


Typical Single-Supply Applications ($V^+ = 5.0\ V_{DC}$) (Continued)

LED Driver



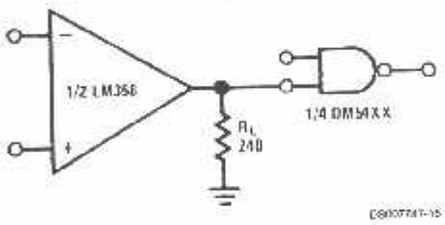
Current Monitor



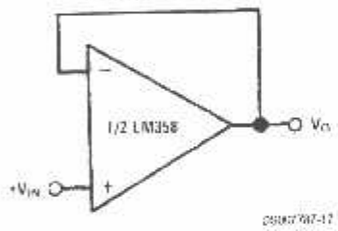
$$V_O = \frac{1V\ (I_L)}{1A}$$

*(Increase R1 for I_L small)
$V_L \leq V^+ - 2V$

Driving TTL

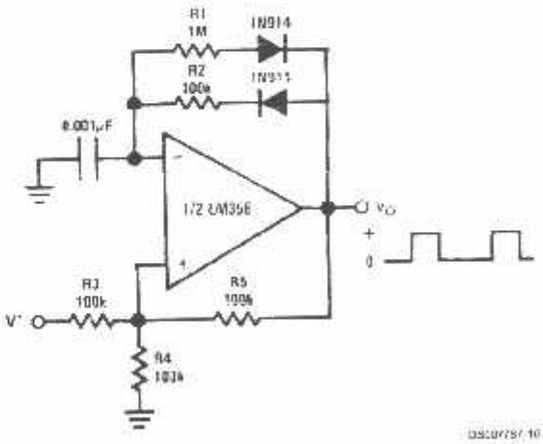


Voltage Follower



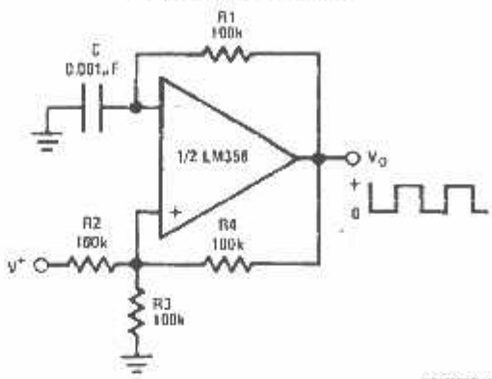
$V_O = V_{IN}$

Pulse Generator

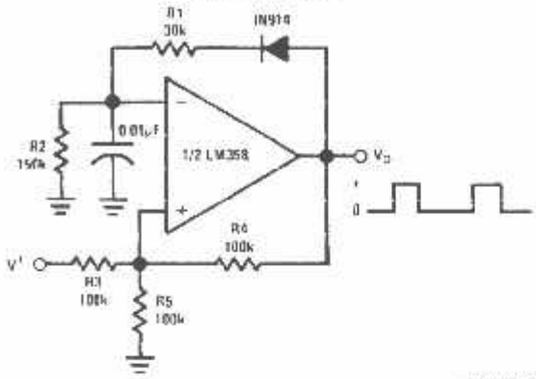


Typical Single-Supply Applications ($V^+ = 5.0\ V_{DC}$) (Continued)

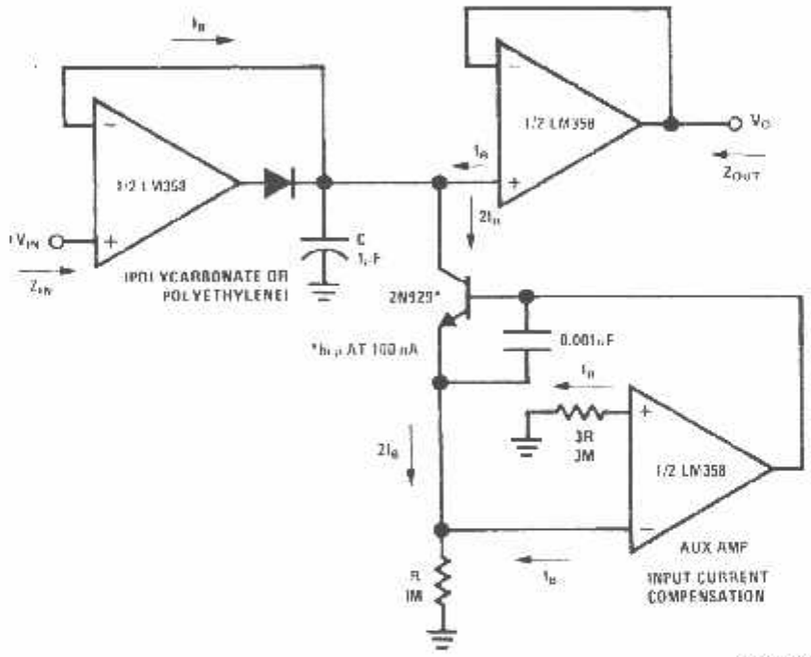
Squarewave Oscillator



Pulse Generator



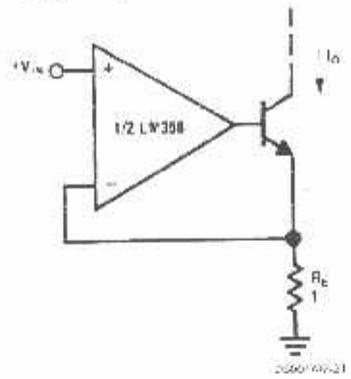
Low Drift Peak Detector



HIGH Z_{IN}
LOW Z_{OUT}

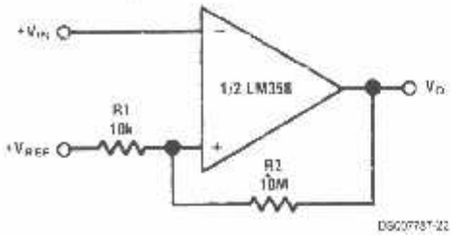
Typical Single-Supply Applications (V^+ = 5.0 V_{DC}) (Continued)

High Compliance Current Sink



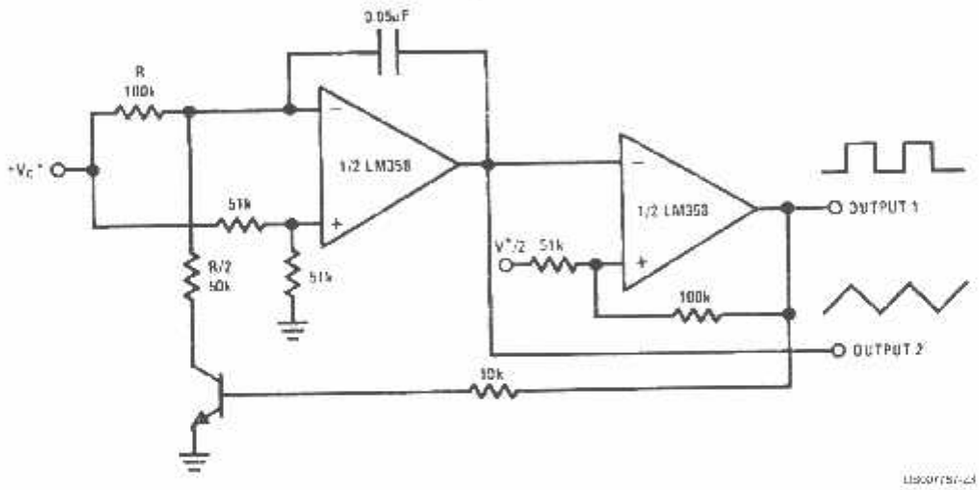
I_O = 1 amp/volt V_{IN}
(Increase R_E for I_O small)

Comparator with Hysteresis



DS007787-22

Voltage Controlled Oscillator (VCO)

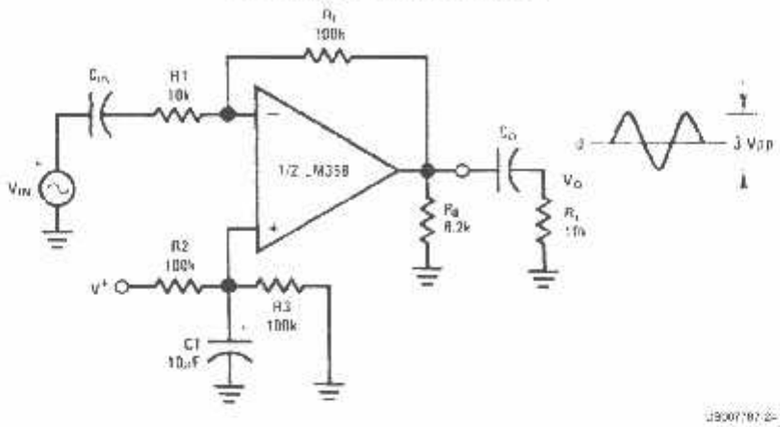


DS007787-23

*WIDE CONTROL VOLTAGE RANGE: 0 $V_{DC} \leq V_C \leq 2$ ($V^+ - 1.5V$ DC)

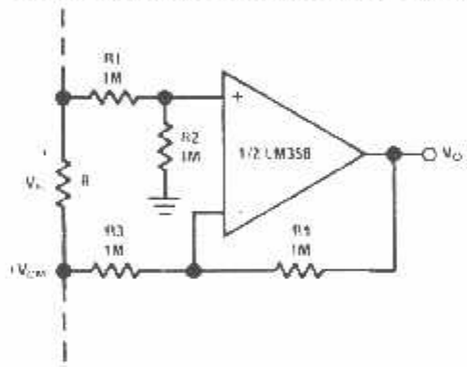
Typical Single-Supply Applications ($V^+ = 5.0\ V_{DC}$) (Continued)

AC Coupled Inverting Amplifier



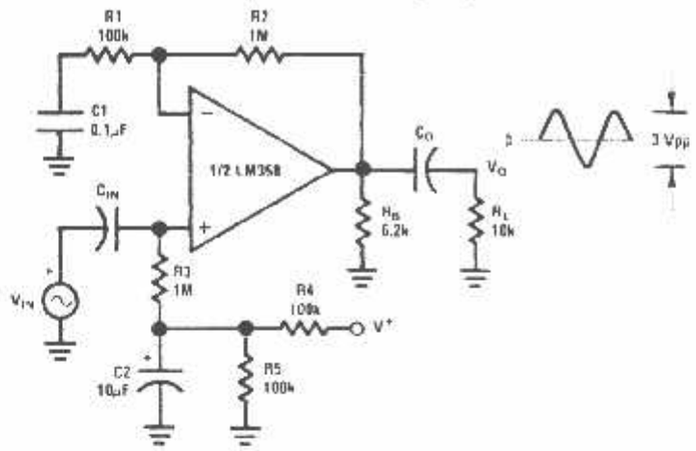
$A_V = -\frac{R_f}{R1}$ (As shown, $A_V = 10$)

Ground Referencing a Differential Input Signal



Typical Single-Supply Applications (V^+ = 5.0 V_{DC}) (Continued)

AC Coupled Non-Inverting Amplifier

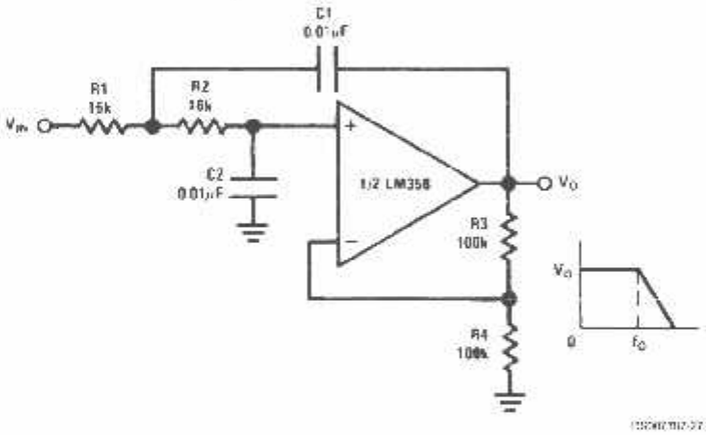


DS007707-26

$$A_V = 1 + \frac{R2}{R1}$$

A_V = 11 (As Shown)

DC Coupled Low-Pass RC Active Filter

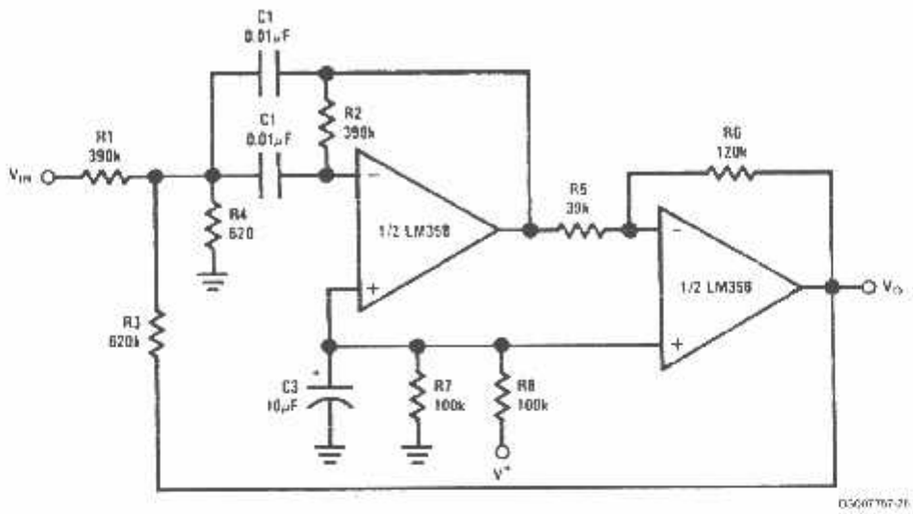


DS007707-27

f_o = 1 kHz
Q = 1
A_V = 2

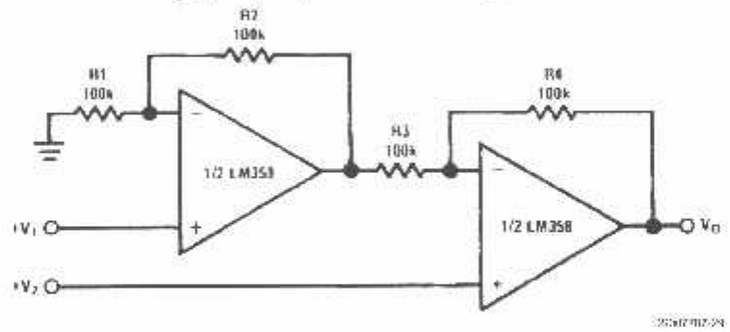
Typical Single-Supply Applications (V^+ = 5.0 V_{DC}) (Continued)

Bandpass Active Filter



f_o = 1 kHz
Q = 25

High Input Z, DC Differential Amplifier



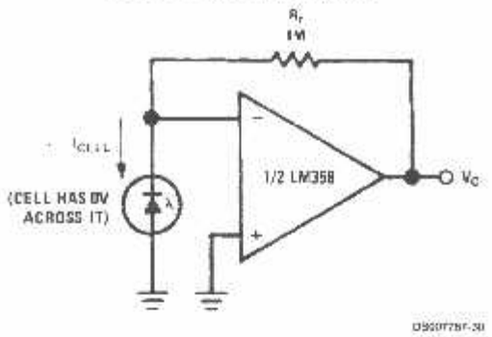
For $\frac{R1}{R2} = \frac{R4}{R3}$ (CMRR depends on this resistor ratio match)

$V_O = 1 + \frac{R4}{R3}(V_2 - V_1)$

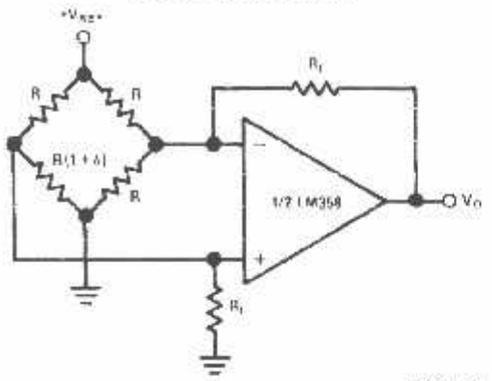
As Shown: $V_O = 2(V_2 - V_1)$

Typical Single-Supply Applications ($V^+ = 5.0\ V_{DC}$) (Continued)

Photo Voltaic-Cell Amplifier



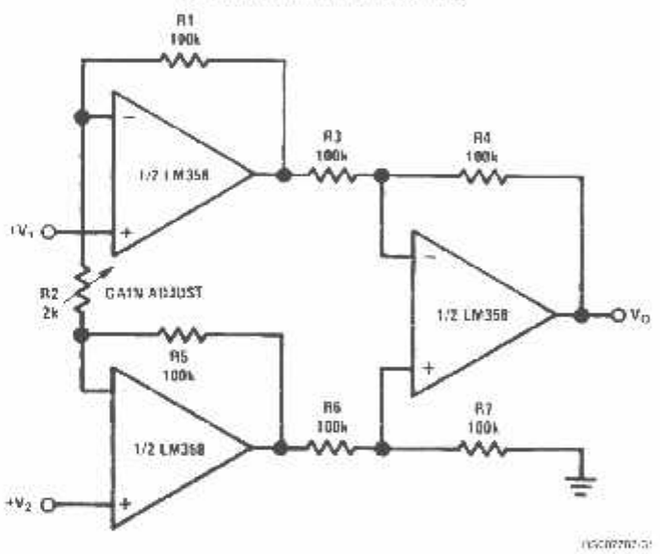
Bridge Current Amplifier



For $\delta << 1$ and $R_f >> R$

$$V_O \approx V_{REF}\left(\frac{\delta}{2}\right)\frac{R_f}{R}$$

High Input Z Adjustable-Gain DC Instrumentation Amplifier



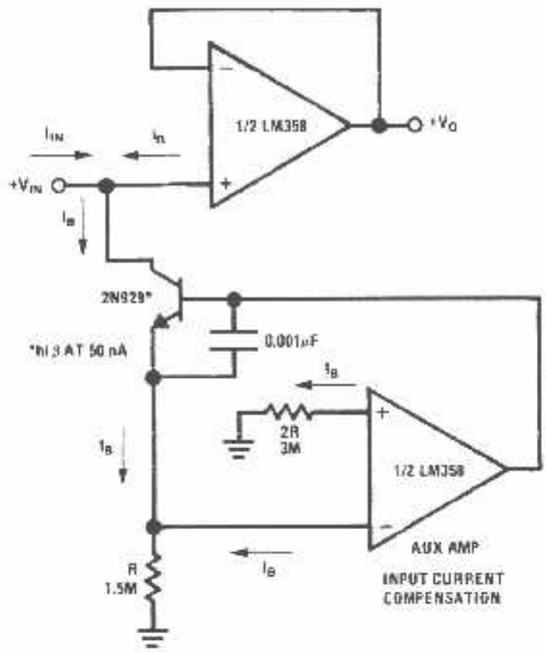
If R1 = R5 & R3 = R4 = R6 = R7 (CMRR depends on match)

$$V_O = 1 + \frac{2R1}{R2}(V_2 - V_1)$$

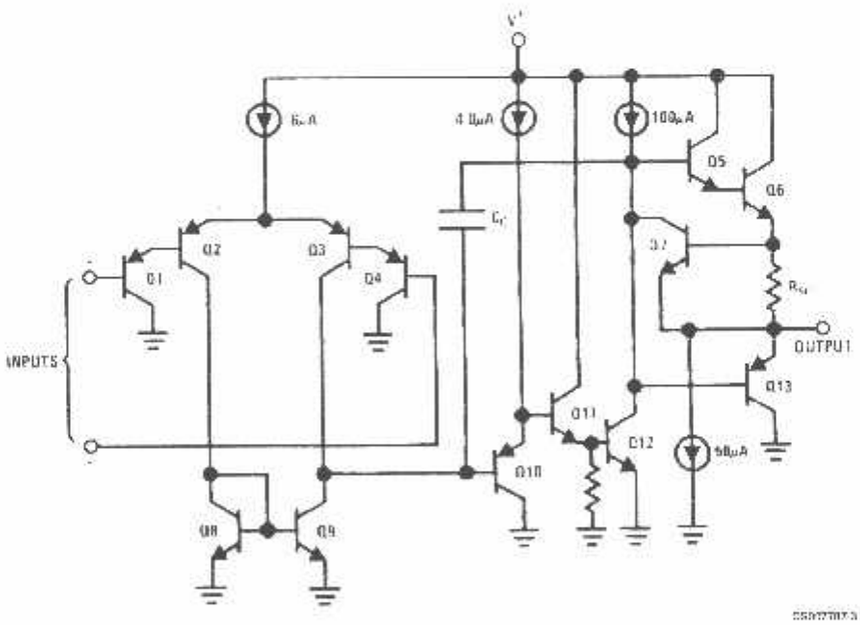
As shown $V_O = 101(V_2 - V_1)$

Typical Single-Supply Applications (V^+ = 5.0 V_{DC}) (Continued)

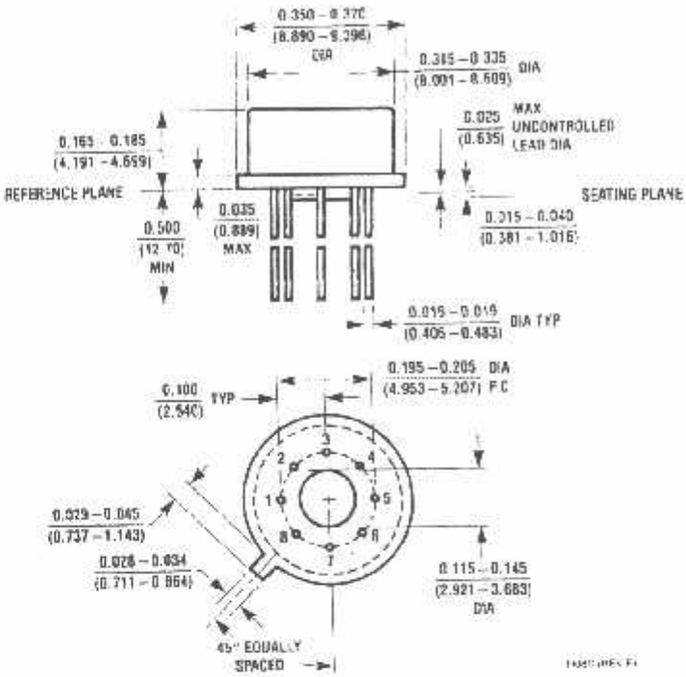
Using Symmetrical Amplifiers to
Reduce Input Current (General Concept)



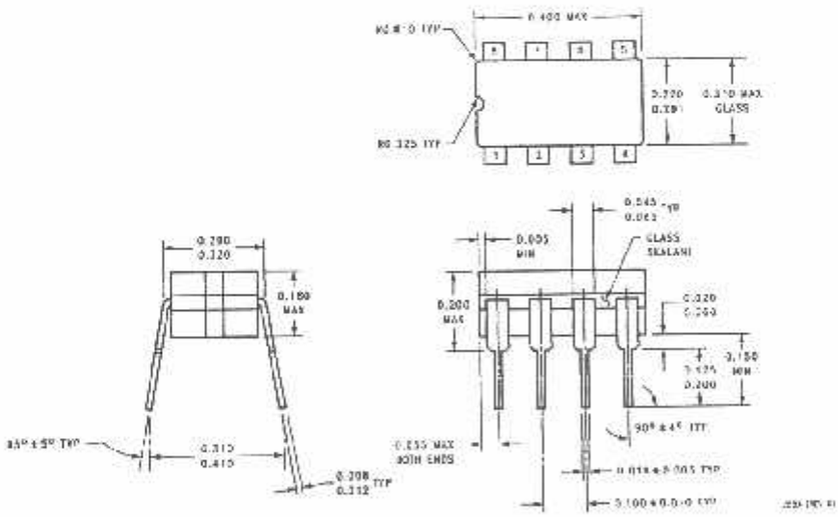
Schematic Diagram (Each Amplifier)



Physical Dimensions inches (millimeters) unless otherwise noted



Metal Can Package (H)
Order Number LM158AH, LM158AH/883, LM158H, LM158H/883, LM258H or LM358H
NS Package Number H08C



Cerdip Package (J)
Order Number LM158J, LM158J/883, LM158AJ or LM158AJ/883
NS Package Number J08A

MOTOROLA

SN54/74LS85

4-BIT MAGNITUDE COMPARATOR

4-BIT MAGNITUDE COMPARATOR

LOW POWER SCHOTTKY

The SN54/74LS85 is a 4-Bit Magnitude Comparator which compares two 4-bit words (A, B), each word having four Parallel Inputs (A_0–A_3, B_0–B_3); A_3, B_3 being the most significant inputs. Operation is not restricted to binary codes, the device will work with any monotonic code. Three Outputs are provided: "A greater than B" ($O_{A>B}$), "A less than B" ($O_{A<B}$), "A equal to B" ($O_{A=B}$). Three Expander Inputs, $I_{A>B}$, $I_{A<B}$, $I_{A=B}$, allow cascading without external gates. For proper compare operation, the Expander Inputs to the least significant position must be connected as follows: $I_{A<B} = I_{A>B} = L$, $I_{A=B} = H$. For serial (ripple) expansion, the $O_{A>B}$, $O_{A<B}$ and $O_{A=B}$ Outputs are connected respectively to the $I_{A>B}$, $I_{A<B}$, and $I_{A=B}$ Inputs of the next most significant comparator, as shown in Figure 1. Refer to Applications section of data sheet for high speed method of comparing large words.

The Truth Table on the following page describes the operation of the SN54/74LS85 under all possible logic conditions. The upper 11 lines describe the normal operation under all conditions that will occur in a single device or in a series expansion scheme. The lower five lines describe the operation under abnormal conditions on the cascading inputs. These conditions occur when the parallel expansion technique is used.

- Easily Expandable
- Binary or BCD Comparison
- $O_{A>B}$, $O_{A<B}$, and $O_{A=B}$ Outputs Available

J SUFFIX
CERAMIC
CASE 620-09

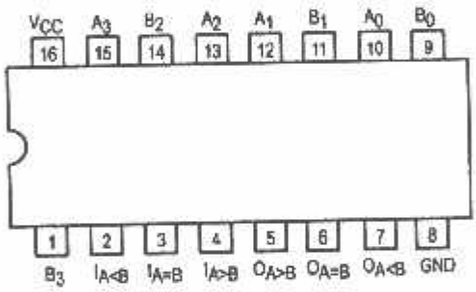
N SUFFIX
PLASTIC
CASE 648-08

D SUFFIX
SOIC
CASE 751B-03

ORDERING INFORMATION

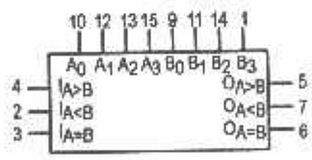
SN54LSXXJ	Ceramic
SN74LSXXN	Plastic
SN74LSXXD	SOIC

CONNECTION DIAGRAM DIP (TOP VIEW)



NOTE:
The Flatpak version has the same pinouts (Connection Diagram) as the Dual In-Line Package.

LOGIC SYMBOL



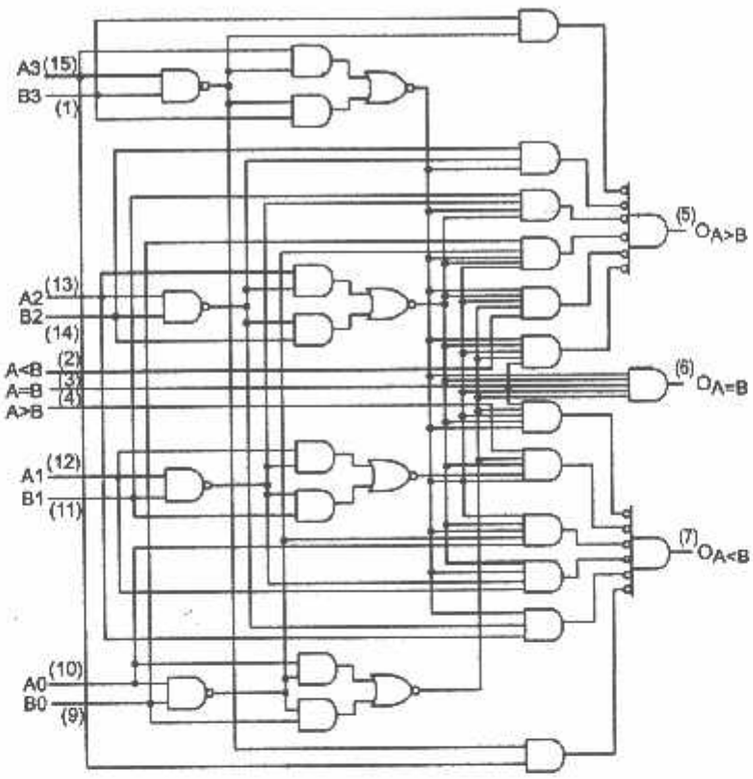
VCC = PIN 16
GND = PIN 8

PIN NAMES

		LOADING (Note a) HIGH	LOW
A_0–A_3, B_0–B_3	Parallel Inputs	1.5 U.L.	0.75 U.L.
$I_{A=B}$	A = B Expander Inputs	1.5 U.L.	0.75 U.L.
$I_{A<B}$, $I_{A>B}$	A < B, A > B, Expander Inputs	0.5 U.L.	0.25 U.L.
$O_{A>B}$	A Greater Than B Output (Note b)	10 U.L.	5 (2.5) U.L.
$O_{A<B}$	B Greater Than A Output (Note b)	10 U.L.	5 (2.5) U.L.
$O_{A=B}$	A Equal to B Output (Note b)	10 U.L.	5 (2.5) U.L.

NOTES:
a) 1 TTL Unit Load (U.L.) = 40 µA HIGH/1.6 mA LOW.
b) The Output LOW drive factor is 2.5 U.L. for Military (54) and 5 U.L. for Commercial (74) Temperature Ranges.

LOGIC DIAGRAM



TRUTH TABLE

COMPARING INPUTS				CASCADING INPUTS			OUTPUTS		
A_3,B_3	A_2,B_2	A_1,B_1	A_0,B_0	$I_{A>B}$	$I_{A<B}$	$I_{A=B}$	$O_{A>B}$	$O_{A<B}$	$O_{A=B}$
$A_3>B_3$	X	X	X	X	X	X	H	L	L
$A_3<B_3$	X	X	X	X	X	X	L	H	L
$A_3=B_3$	$A_2>B_2$	X	X	X	X	X	H	L	L
$A_3=B_3$	$A_2<B_2$	X	X	X	X	X	L	H	L
$A_3=B_3$	$A_2=B_2$	$A_1>B_1$	X	X	X	X	H	L	L
$A_3=B_3$	$A_2=B_2$	$A_1<B_1$	X	X	X	X	L	H	L
$A_3=B_3$	$A_2=B_2$	$A_1=B1$	$A_0>B_0$	X	X	X	H	L	L
$A_3=B_3$	$A_2=B_2$	$A_1=B_1$	$A_0<B_0$	X	X	X	L	H	L
$A_3=B_3$	$A_2=B_2$	$A_1=B_1$	$A_0=B_0$	H	L	L	H	L	L
$A_3=B_3$	$A_2=B_2$	$A_1=B_1$	$A_0=B_0$	L	H	L	L	H	L
$A_3=B_3$	$A_2=B_2$	$A_1=B_1$	$A_0=B_0$	X	X	H	L	L	H
$A_3=B_3$	$A_2=B_2$	$A_1=B_1$	$A_0=B_0$	H	H	L	L	L	L
$A_3=B_3$	$A_2=B_2$	$A_1=B_1$	$A_0=B_0$	L	L	L	H	H	L

H = HIGH Level
L = LOW Level
X = IMMATERIAL

GUARANTEED OPERATING RANGES

Symbol	Parameter		Min	Typ	Max	Unit
V_{CC}	Supply Voltage	54 74	4.5 4.75	5.0 5.0	5.5 5.25	V
T_A	Operating Ambient Temperature Range	54 74	−55 0	25 25	125 70	°C
I_{OH}	Output Current — High	54, 74			−0.4	mA
I_{OL}	Output Current — Low	54 74			4.0 8.0	mA

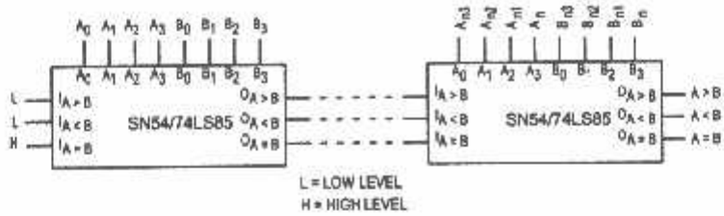


Figure 1. Comparing Two n-Bit Words

APPLICATIONS

Figure 2 shows a high speed method of comparing two 24-bit words with only two levels of device delay. With the technique shown in Figure 1, six levels of device delay result when comparing two 24-bit words. The parallel technique can be expanded to any number of bits, see Table 1.

Table 1

WORD LENGTH	NUMBER OF PKGS.
1–4 Bits	1
5–24 Bits	2–6
25–120 Bits	8–31

NOTE:
The SN54/74LS85 can be used as a 5-bit comparator only when the outputs are used to drive the A_0–A_3 and B_0–B_3 inputs of another SN54/74LS85 as shown in Figure 2 in positions #1, 2, 3, and 4.

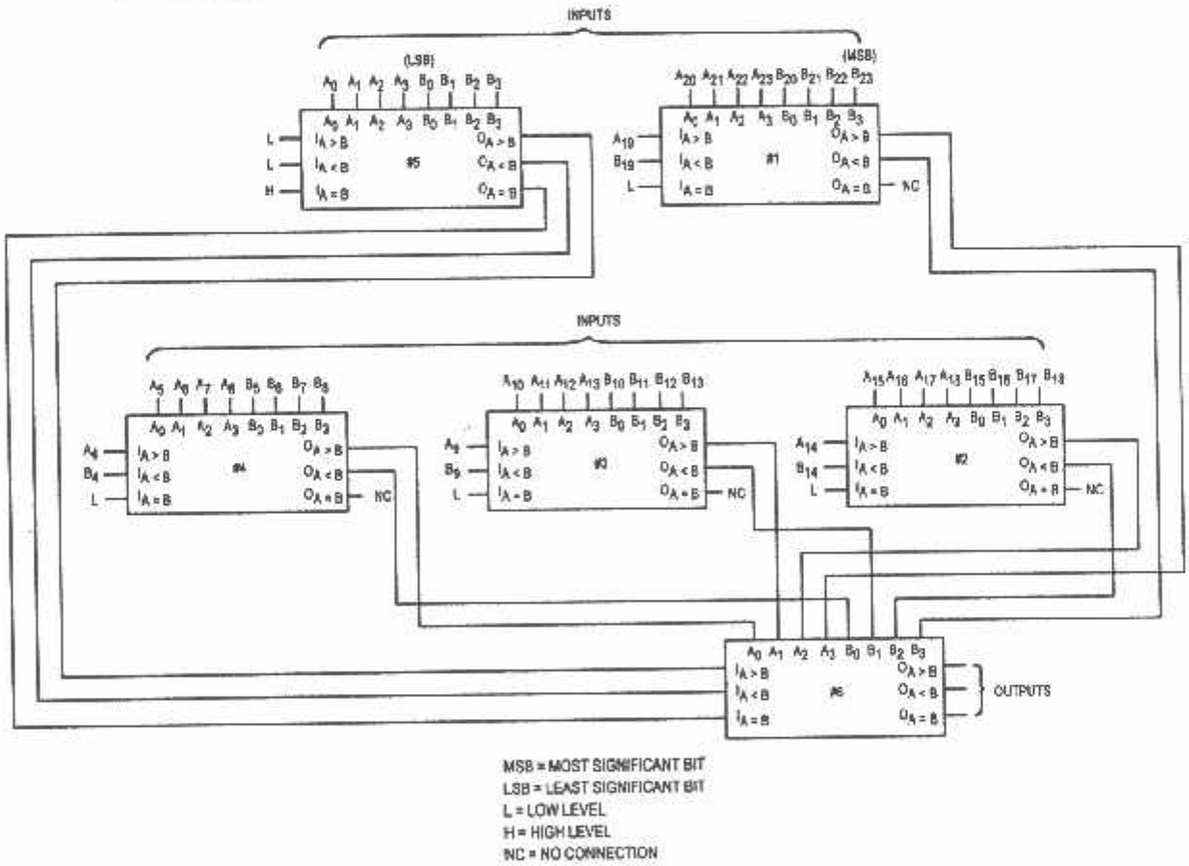


Figure 2. Comparison of Two 24-Bit Words

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

Symbol	Parameter		Limits Min	Typ	Max	Unit	Test Conditions	
V_{IH}	Input HIGH Voltage		2.0			V	Guaranteed Input HIGH Voltage for All Inputs	
V_{IL}	Input LOW Voltage	54			0.7	V	Guaranteed Input LOW Voltage for All Inputs	
		74			0.8			
V_{IK}	Input Clamp Diode Voltage			−0.65	−1.5	V	V_{CC} = MIN, I_{IN} = −18 mA	
V_{OH}	Output HIGH Voltage	54	2.5	3.5		V	V_{CC} = MIN, I_{OH} = MAX, V_{IN} = V_{IH} or V_{IL} per Truth Table	
		74	2.7	3.5		V		
V_{OL}	Output LOW Voltage	54, 74		0.25	0.4	V	I_{OL} = 4.0 mA	V_{CC} = V_{CC} MIN, V_{IN} = V_{IL} or V_{IH} per Truth Table
		74		0.35	0.5	V	I_{OL} = 8.0 mA	
I_{IH}	Input HIGH Current A < B, A > B Other Inputs				20 60	µA	V_{CC} = MAX, V_{IN} = 2.7 V	
	A < B, A > B Other Inputs				0.1 0.3	mA	V_{CC} = MAX, V_{IN} = 7.0 V	
I_{IL}	Input LOW Current A < B, A > B Other Inputs				−0.4 −1.2	mA	V_{CC} = MAX, V_{IN} = 0.4 V	
I_{OS}	Output Short Circuit Current (Note 1)		−20		−100	mA	V_{CC} = MAX	
I_{CC}	Power Supply Current				20	mA	V_{CC} = MAX	

Note 1: Not more than one output should be shorted at a time, nor for more than 1 second.

AC CHARACTERISTICS (T_A = 25°C, V_{CC} = 5.0 V)

Symbol	Parameter	Limits Min	Typ	Max	Unit	Test Conditions
t_{PLH} t_{PHL}	Any A or B to A < B, A > B		24 20	36 30	ns	V_{CC} = 5.0 V C_L = 15 pF
t_{PLH} t_{PHL}	Any A or B to A = B		27 23	45 45	ns	
t_{PLH} t_{PHL}	A < B or A = B to A > B		14 11	22 17	ns	
t_{PLH} t_{PHL}	A = B to A = B		13 13	20 26	ns	
t_{PLH} t_{PHL}	A > B or A = B to A < B		14 11	22 17	ns	

AC WAVEFORMS

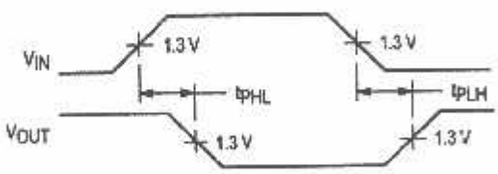


Figure 3

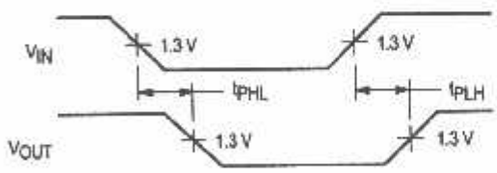


Figure 4

Timer

NE/SA/SE555/SE555C

DESCRIPTION

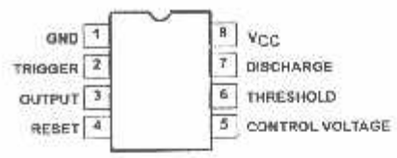
The 555 monolithic timing circuit is a highly stable controller capable of producing accurate time delays, or oscillation. In the time delay mode of operation, the time is precisely controlled by one external resistor and capacitor. For a stable operation as an oscillator, the free running frequency and the duty cycle are both accurately controlled with two external resistors and one capacitor. The circuit may be triggered and reset on falling waveforms, and the output structure can source or sink up to 200mA.

FEATURES

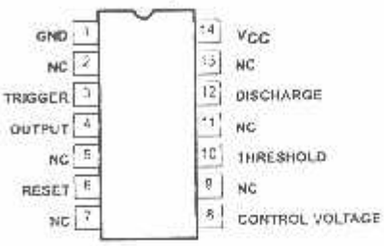
- Turn-off time less than 2µs
- Max. operating frequency greater than 500kHz
- Timing from microseconds to hours
- Operates in both astable and monostable modes
- High output current
- Adjustable duty cycle
- TTL compatible
- Temperature stability of 0.005% per °C

PIN CONFIGURATIONS

D, N, FE Packages



F Package



TOP VIEW

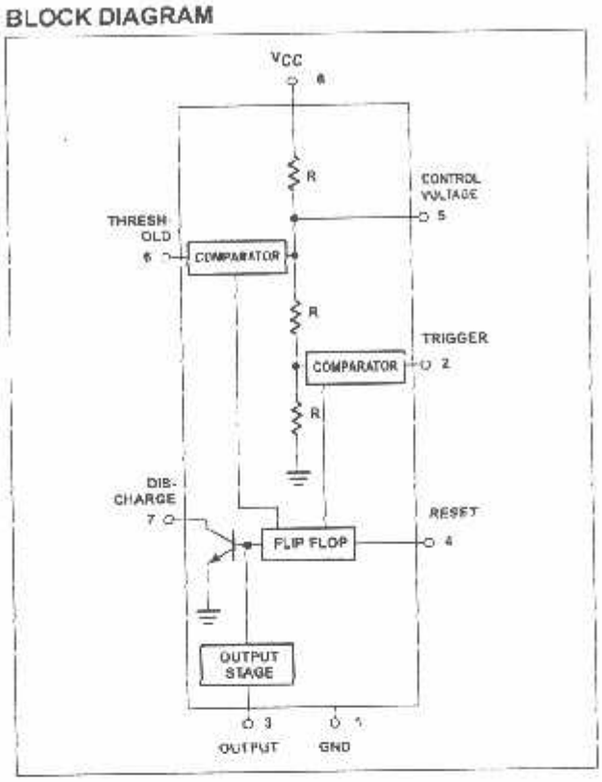
APPLICATIONS

- Precision timing
- Pulse generation
- Sequential timing
- Time delay generation
- Pulse width modulation

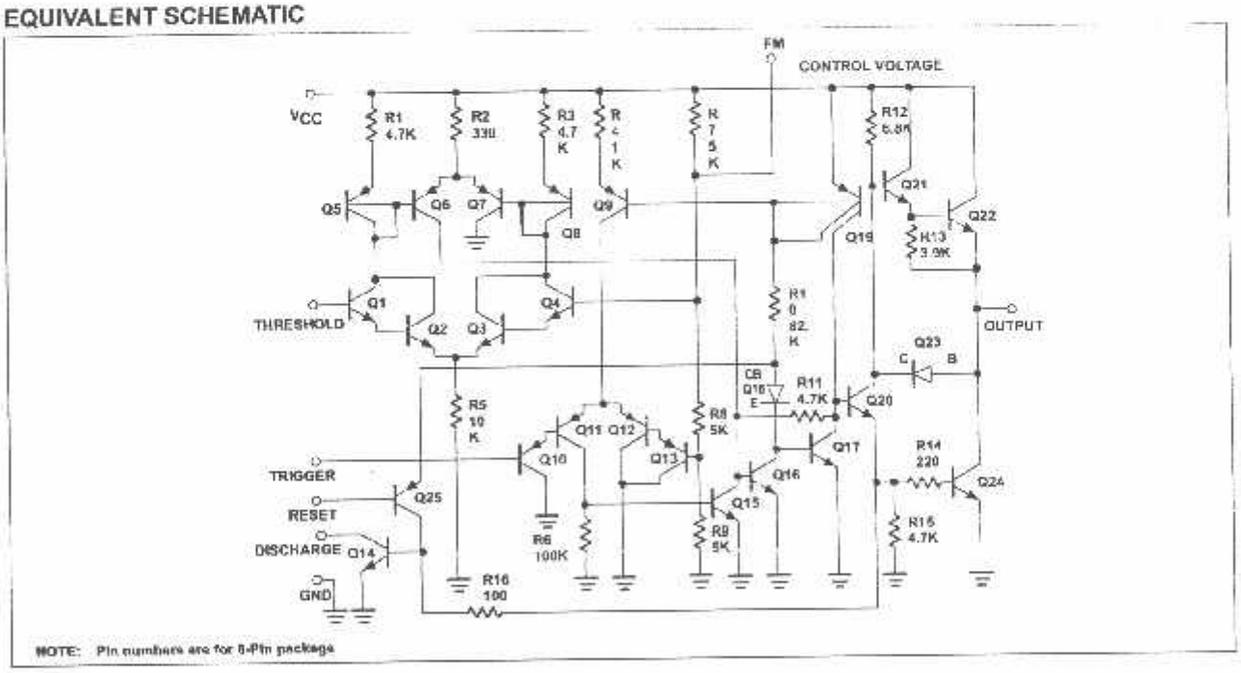
ORDERING INFORMATION

DESCRIPTION	TEMPERATURE RANGE	ORDER CODE	DWG #
8-Pin Plastic Small Outline (SO) Package	0 to +70°C	NE555D	0174C
8-Pin Plastic Dual In-Line Package (DIP)	0 to +70°C	NE555N	0404B
8-Pin Plastic Dual In-Line Package (DIP)	-40°C to +85°C	SA555N	0404B
8-Pin Plastic Small Outline (SO) Package	-40°C to +85°C	SA555D	0174C
8-Pin Hermetic Ceramic Dual In-Line Package (CERDIP)	-55°C to +125°C	SE555CFE	
8-Pin Plastic Dual In-Line Package (DIP)	-55°C to +125°C	SE555CN	0404B
14-Pin Plastic Dual In-Line Package (DIP)	-55°C to +125°C	SE555N	0405B
8-Pin Hermetic Cerdip	-55°C to +125°C	SE555FE	
14-Pin Ceramic Dual In-Line Package (CERDIP)	0 to +70°C	NE555F	0581B
14-Pin Ceramic Dual In-Line Package (CERDIP)	-55°C to +125°C	SE555F	0581B
14-Pin Ceramic Dual In-Line Package (CERDIP)	-55°C to +125°C	SE555CF	0581B

BLOCK DIAGRAM



EQUIVALENT SCHEMATIC



NOTE: Pin numbers are for 8-Pin package

ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Supply voltage		
	SE555	+18	V
	NE555, SE555C, SA555	+16	V
P_D	Maximum allowable power dissipation[1]	600	mW
T_A	Operating ambient temperature range		
	NE555	0 to +70	°C
	SA555	-40 to +85	°C
	SE555, SE555C	-55 to +125	°C
T_{STG}	Storage temperature range	-65 to +150	°C
T_{SOLD}	Lead soldering temperature (10sec max)	+300	°C

NOTES:

1. The junction temperature must be kept below 125°C for the D package and below 150°C for the FE, N and F packages. At ambient temperatures above 25°C, where this limit would be derated by the following factors:
   D package 160°C/W
   FE package 150°C/W
   N package 100°C/W
   F package 105°C/W

DC AND AC ELECTRICAL CHARACTERISTICS

T_A = 25°C, V_{CC} = +5V to +15 unless otherwise specified

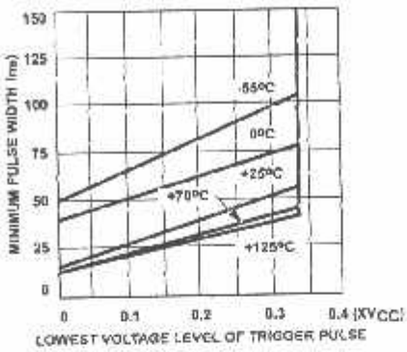
SYMBOL	PARAMETER	TEST CONDITIONS	SE555			NE555/SE555C			UNIT
			Min	Typ	Max	Min	Typ	Max	
V_{CC}	Supply voltage		4.5		18	4.5		16	V
I_{CC}	Supply current (low state)[1]	V_{CC}=5V, R_L=∞		3	5		3	6	mA
		V_{CC}=15V, R_L=∞		10	12		10	15	mA
	Timing error (monostable)	R_A=2kΩ to 100kΩ							
t_M	Initial accuracy[2]	C=0.1μF		0.5	2.0		1.0	3.0	%
$\Delta t_M/\Delta T$	Drift with temperature			30	100		50	150	ppm/°C
$\Delta t_M/\Delta V_S$	Drift with supply voltage			0.05	0.2		0.1	0.5	%/V
	Timing error (astable)	R_A, R_B=1kΩ to 100kΩ							
t_A	Initial accuracy[2]	C=0.1μF		4	6		5	13	%
$\Delta t_A/\Delta T$	Drift with temperature	V_{CC}=15V			500			500	ppm/°C
$\Delta t_A/\Delta V_S$	Drift with supply voltage			0.15	0.6		0.3	1	%/V
V_C	Control voltage level	V_{CC}=15V	9.6	10.0	10.4	9.0	10.0	11.0	V
		V_{CC}=5V	2.9	3.33	3.8	2.6	3.33	4.0	V
V_{TH}	Threshold voltage	V_{CC}=15V	9.4	10.0	10.6	8.8	10.0	11.2	V
		V_{CC}=5V	2.7	3.33	4.0	2.4	3.33	4.2	V
I_{TH}	Threshold current[3]			0.1	0.25		0.1	0.25	μA
V_{TRIG}	Trigger voltage	V_{CC}=15V	4.8	5.0	5.2	4.5	5.0	5.6	V
		V_{CC}=5V	1.45	1.67	1.9	1.1	1.67	2.2	V
I_{TRIG}	Trigger current	V_{TRIG}=0V		0.5	0.9		0.5	2.0	μA
V_{RESET}	Reset voltage[4]	V_{CC}=15V, V_{TH}=10.5V	0.3		1.0	0.3		1.0	V
I_{RESET}	Reset current	V_{RESET}=0.4V		0.1	0.4		0.1	0.4	mA
	Reset current	V_{RESET}=0V		0.4	1.0		0.4	1.5	mA
V_{OL}	Output voltage (low)	V_{CC}=15V							
		I_{SINK}=10mA		0.1	0.15		0.1	0.25	V
		I_{SINK}=50mA		0.4	0.5		0.4	0.75	V
		I_{SINK}=100mA		2.0	2.2		2.0	2.5	V
		I_{SINK}=200mA		2.5			2.5		V
		V_{CC}=5V							
		I_{SINK}=8mA		0.1	0.25		0.3	0.4	V
		I_{SINK}=5mA		0.05	0.2		0.25	0.35	V
V_{OH}	Output voltage (high)	V_{CC}=15V							
		I_{SOURCE}=200mA		12.5			12.5		V
		I_{SOURCE}=100mA	13.0	13.3		12.75	13.3		V
		V_{CC}=5V							
		I_{SOURCE}=100mA	3.0	3.3		2.75	3.3		V
t_{OFF}	Turn-off time[5]	V_{RESET}=V_{CC}		0.5	2.0		0.5	2.0	μs
t_R	Rise time of output			100	200		100	300	ns
t_F	Fall time of output			100	200		100	300	ns
	Discharge leakage current			20	100		20	100	nA

NOTES:

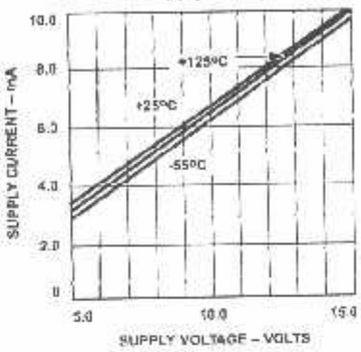
1. Supply current when output high typically 1mA less.
2. Tested at V_{CC}=5V and V_{CC}=15V.
3. This will determine the max value of R_A+R_B, for 15V operation, the max total R=10MΩ, and for 5V operation, the max. total R=3.4MΩ.
4. Specified with trigger input high.
5. Time measured from a positive going input pulse from 0 to 0.8×V_{CC} into the threshold to the drop from high to low of the output. Trigger is tied to threshold.

TYPICAL PERFORMANCE CHARACTERISTICS

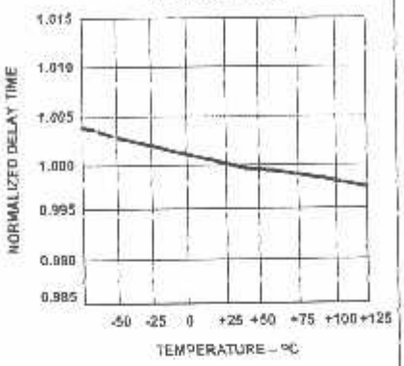
Minimum Pulse Width Required for Triggering



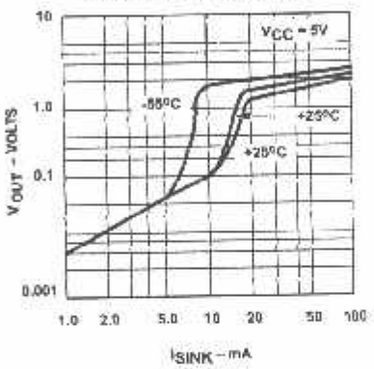
Supply Current vs Supply Voltage



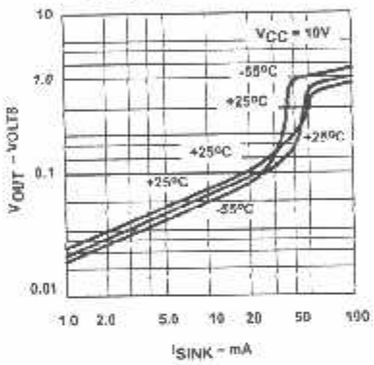
Delay Time vs Temperature



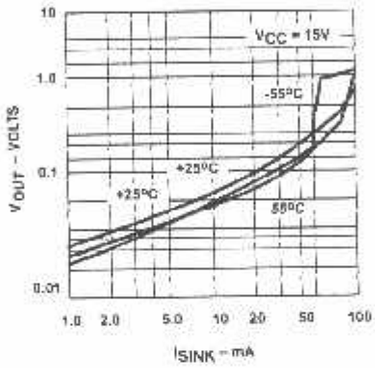
Low Output Voltage vs Output Sink Current



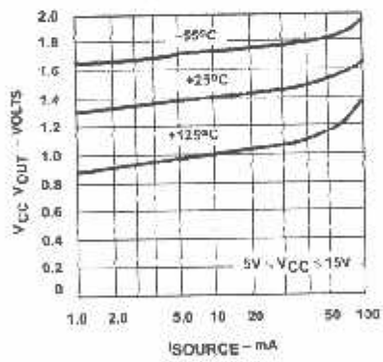
Low Output Voltage vs Output Sink Current



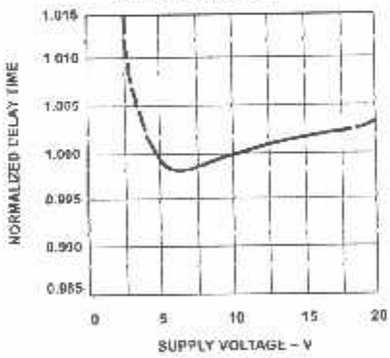
Low Output Voltage vs Output Sink Current



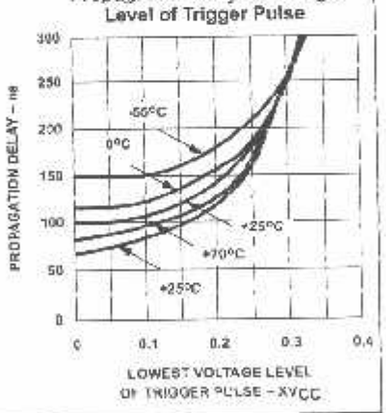
High Output Voltage Drop vs Output Source Current



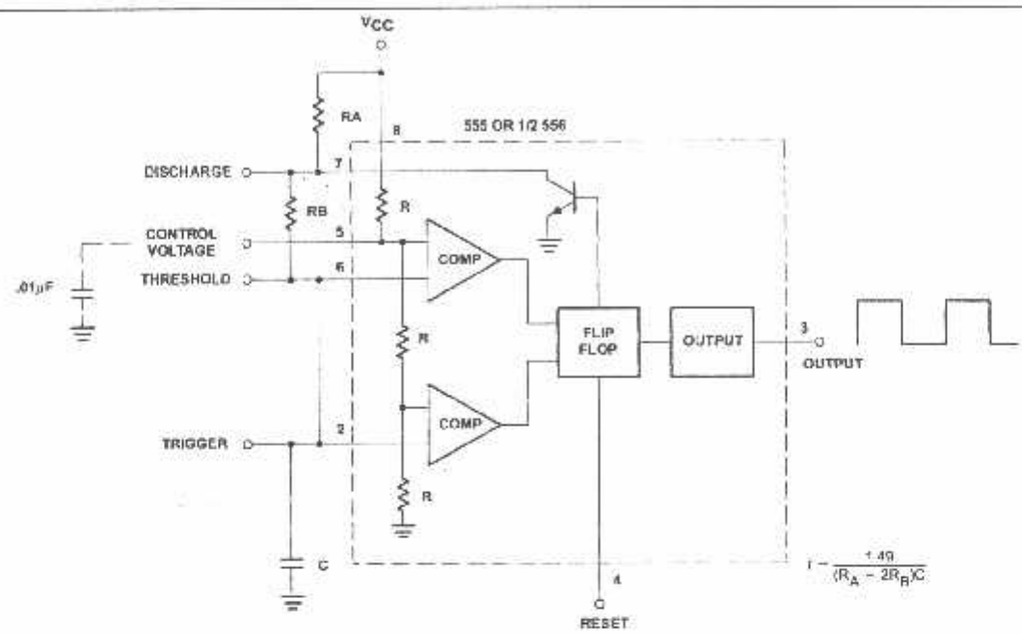
Delay Time vs Supply Voltage



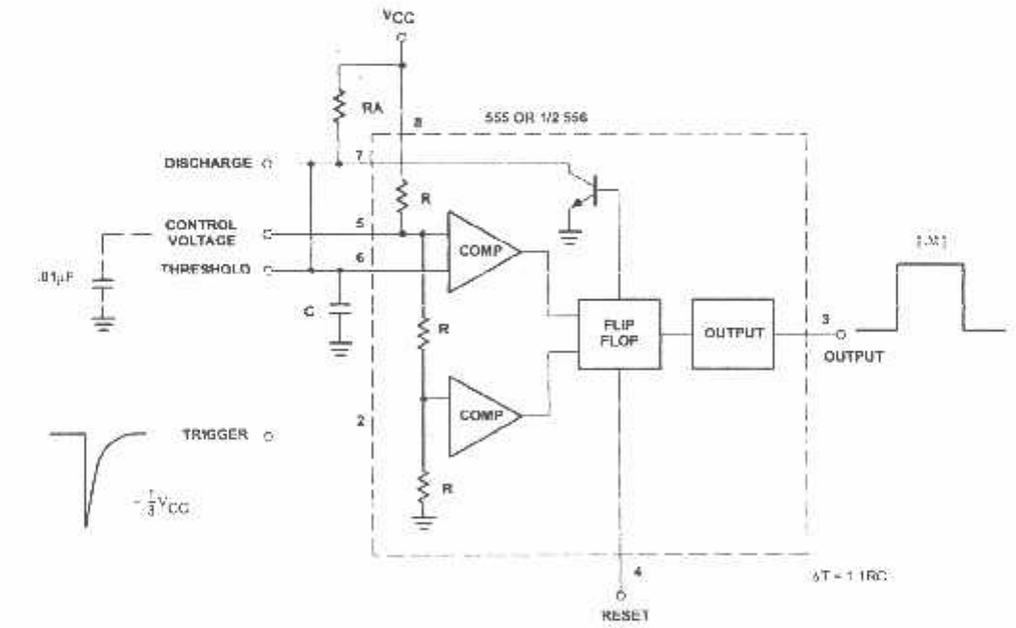
Propagation Delay vs Voltage Level of Trigger Pulse



TYPICAL APPLICATIONS



Astable Operation



Monostable Operation

TYPICAL APPLICATIONS

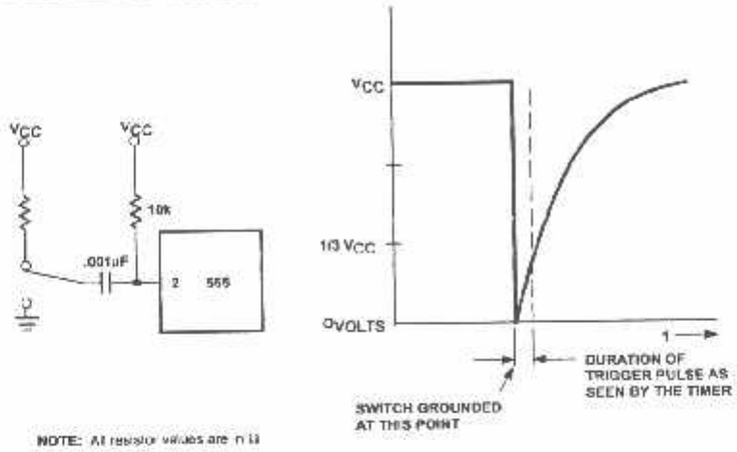


Figure 1. AC Coupling of the Trigger Pulse

Trigger Pulse Width Requirements and Time Delays

Due to the nature of the trigger circuitry, the timer will trigger on the negative going edge of the input pulse. For the device to time out properly, it is necessary that the trigger voltage level be returned to some voltage greater than one third of the supply before the time out period. This can be achieved by making either the trigger pulse sufficiently short or by AC coupling into the trigger. By AC coupling the trigger, see Figure 1, a short negative going pulse is achieved when the trigger signal goes to ground. AC coupling is most frequently used in conjunction with a switch or a signal that goes to ground which initiates the timing cycle. Should the trigger be held low, without AC coupling, for a longer duration than the timing cycle the output will remain in a high state for the duration of the low trigger signal, without regard to the threshold comparator state. This is due to the predominance of Q_{15} on the base of Q_{16}, controlling the state of the bi-stable flip-flop. When the trigger signal then returns to a high level, the output will fall immediately. Thus, the output signal will follow the trigger signal in this case.

Another consideration is the "turn-off time". This is the measurement of the amount of time required after the threshold reaches 2/3 V_{CC} to turn the output low. To explain further, Q_1 at the threshold input turns on after reaching 2/3 V_{CC}, which then turns on Q_5, which turns on Q_6. Current from Q_6 turns on Q_{16} which turns Q_{17} off. This allows current from Q_{19} to turn on Q_{20} and Q_{24} to given an output low. These steps cause the 2µs max. delay as stated in the data sheet.

Also, a delay comparable to the turn-off time is the trigger release time. When the trigger is low, Q_{10} is on and turns on Q_{11} which turns on Q_{15}. Q_{15} turns off Q_{16} and allows Q_{17} to turn on. This turns off current to Q_{20} and Q_{24}, which results in output high. When the trigger is released, Q_{10} and Q_{11} shut off, Q_{15} turns off, Q_{16} turns on and the circuit then follows the same path and time delay explained as "turn off time". This trigger release time is very important in designing the trigger pulse width so as not to interfere with the output signal as explained previously.

GlobalOptoisolator™

VDE | UL | CSA | SETI | SEMKO | DEMKO | NEMKO | RASI

6-Pin DIP Optoisolators Transistor Output

4N35*
4N36
4N37
[CTR = 100% Min]

*Motorola Preferred Device

The 4N35, 4N36 and 4N37 devices consist of a gallium arsenide infrared emitting diode optically coupled to a monolithic silicon phototransistor detector.

- Current Transfer Ratio — 100% Minimum @ Specified Conditions
- Guaranteed Switching Speeds
- Meets or Exceeds all JEDEC Registered Specifications
- ***To order devices that are tested and marked per VDE 0884 requirements, the suffix "V" must be included at end of part number. VDE 0884 is a test option.***

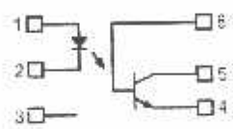
Applications

- General Purpose Switching Circuits
- Interfacing and coupling systems of different potentials and impedances
- Regulation Feedback Circuits
- Monitor & Detection Circuits
- Solid State Relays

STYLE 1 PLASTIC

STANDARD THRU HOLE
CASE 730A–04

SCHEMATIC



PIN 1. LED ANODE
2. LED CATHODE
3. N.C.
4. EMITTER
5. COLLECTOR
6. BASE

MAXIMUM RATINGS (T_A = 25°C unless otherwise noted)

Rating	Symbol	Value	Unit
INPUT LED			
Reverse Voltage	V_R	6	Volts
Forward Current — Continuous	I_F	60	mA
LED Power Dissipation @ T_A = 25°C with Negligible Power in Output Detector Derate above 25°C	P_D	120 1.41	mW mW/°C
OUTPUT TRANSISTOR			
Collector–Emitter Voltage	V_{CEO}	30	Volts
Emitter–Base Voltage	V_{EBO}	7	Volts
Collector–Base Voltage	V_{CBO}	70	Volts
Collector Current — Continuous	I_C	150	mA
Detector Power Dissipation @ T_A = 25°C with Negligible Power in Input LED Derate above 25°C	P_D	150 1.76	mW mW/°C
TOTAL DEVICE			
Isolation Source Voltage(1) (Peak ac Voltage, 60 Hz, 1 sec Duration)	V_{ISO}	7500	Vac(pk)
Total Device Power Dissipation @ T_A = 25°C Derate above 25°C	P_D	250 2.94	mW mW/°C
Ambient Operating Temperature Range(2)	T_A	−55 to +100	°C
Storage Temperature Range(2)	T_{stg}	−55 to +150	°C
Soldering Temperature (10 sec, 1/16" from case)	T_L	260	°C

1. Isolation surge voltage is an internal device dielectric breakdown rating.
   For this test, Pins 1 and 2 are common, and Pins 4, 5 and 6 are common.
2. Refer to Quality and Reliability Section in Opto Data Book for information on test conditions.

Preferred devices are Motorola recommended choices for future use and best overall value.

GlobalOptoisolator is a trademark of Motorola, Inc.

MOTOROLA

ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise noted)(1)

Characteristic		Symbol	Min	Typ(1)	Max	Unit
INPUT LED						
Forward Voltage (I_F = 10 mA)	T_A = 25°C T_A = −55°C T_A = 100°C	V_F	0.8 0.9 0.7	1.15 1.3 1.05	1.5 1.7 1.4	V
Reverse Leakage Current (V_R = 6 V)		I_R	—	—	10	μA
Capacitance (V = 0 V, f = 1 MHz)		C_J	—	18	—	pF
OUTPUT TRANSISTOR						
Collector–Emitter Dark Current (V_{CE} = 10 V, T_A = 25°C) (V_{CE} = 30 V, T_A = 100°C)		I_{CEO}	— —	1 —	50 500	nA μA
Collector–Base Dark Current (V_{CB} = 10 V)	T_A = 25°C T_A = 100°C	I_{CBO}	—	0.2 100	20 —	nA
Collector–Emitter Breakdown Voltage (I_C = 1 mA)		$V_{(BR)CEO}$	30	45	—	V
Collector–Base Breakdown Voltage (I_C = 100 μA)		$V_{(BR)CBO}$	70	100	—	V
Emitter–Base Breakdown Voltage (I_E = 100 μA)		$V_{(BR)EBO}$	7	7.8	—	V
DC Current Gain (I_C = 2 mA, V_{CE} = 5 V)		h_{FE}	—	400	—	—
Collector–Emitter Capacitance (f = 1 MHz, V_{CE} = 0)		C_{CE}		7	—	pF
Collector–Base Capacitance (f = 1 MHz, V_{CB} = 0)		C_{CB}	—	19	—	pF
Emitter–Base Capacitance (f = 1 MHz, V_{EB} = 0)		C_{EB}	—	9	—	pF
COUPLED						
Output Collector Current (I_F = 10 mA, V_{CE} = 10 V)	T_A = 25°C T_A = −55°C T_A = 100°C	I_C (CTR)(2)	10 (100) 4 (40) 4 (40)	30 (300) — —	— — —	mA (%)
Collector–Emitter Saturation Voltage (I_C = 0.5 mA, I_F = 10 mA)		$V_{CE(sat)}$	—	0.14	0.3	V
Turn–On Time	(I_C = 2 mA, V_{CC} = 10 V, R_L = 100 Ω)(3)	t_{on}	—	7.5	10	μs
Turn–Off Time		t_{off}	—	5.7	10	
Rise Time		t_r	—	3.2	—	
Fall Time		t_f	—	4.7	—	
Isolation Voltage (f = 60 Hz, t = 1 sec)		V_{ISO}	7500	—	—	Vac(pk)
Isolation Current(4) (V_{I-O} = 3550 Vpk) (V_{I-O} = 2500 Vpk) (V_{I-O} = 1500 Vpk)	4N35 4N36 4N37	I_{ISO}	— — —	— — 8	100 100 100	μA
Isolation Resistance (V = 500 V)(4)		R_{ISO}	10^{11}	—	—	Ω
Isolation Capacitance (V = 0 V, f = 1 MHz)(4)		C_{ISO}	—	0.2	2	pF

1. Always design to the specified minimum/maximum electrical limits (where applicable).
2. Current Transfer Ratio (CTR) = I_C/I_F x 100%.
3. For test circuit setup and waveforms, refer to Figure 11.
4. For this test, Pins 1 and 2 are common, and Pins 4, 5 and 6 are common.

TYPICAL CHARACTERISTICS

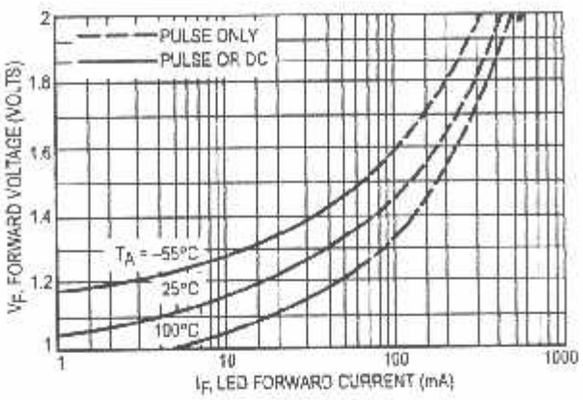


Figure 1. LED Forward Voltage versus Forward Current

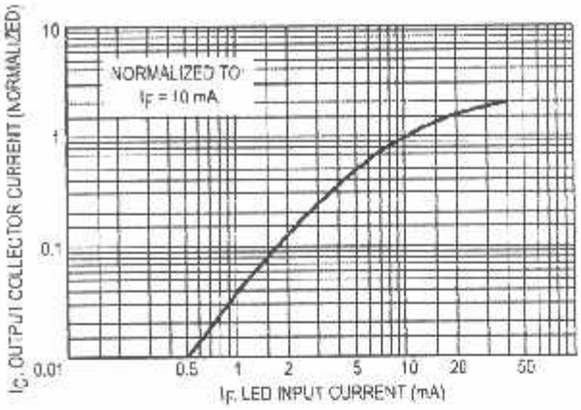


Figure 2. Output Current versus Input Current

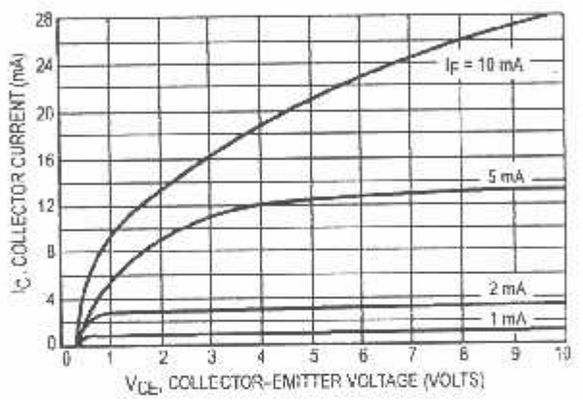


Figure 3. Collector Current versus Collector–Emitter Voltage

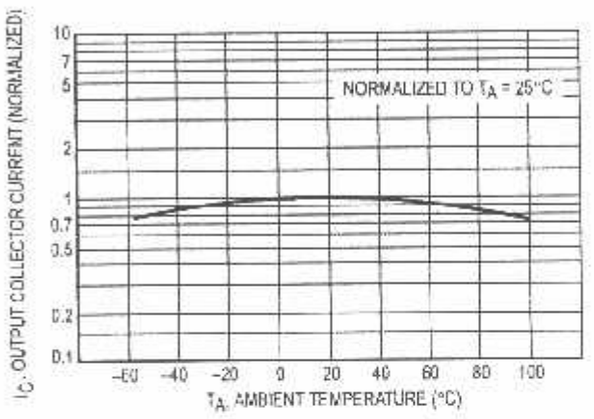


Figure 4. Output Current versus Ambient Temperature

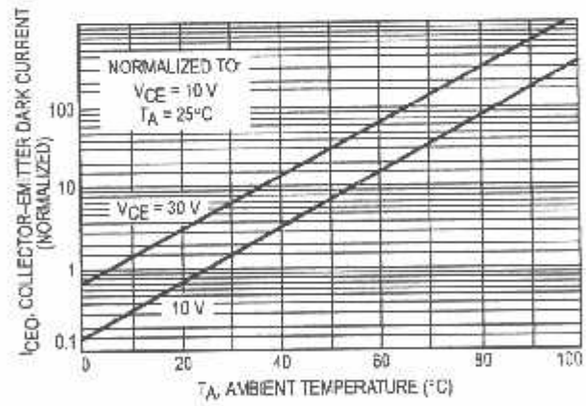


Figure 5. Dark Current versus Ambient Temperature

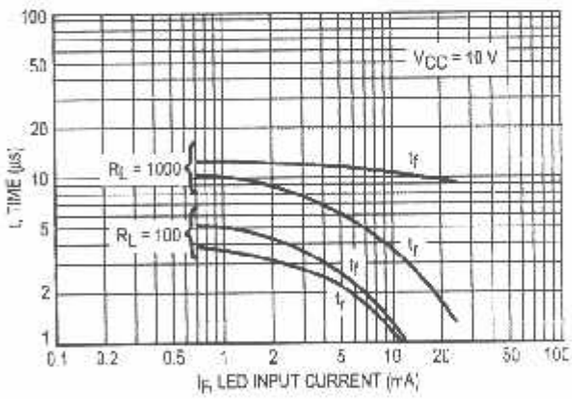


Figure 6. Rise and Fall Times (Typical Values)

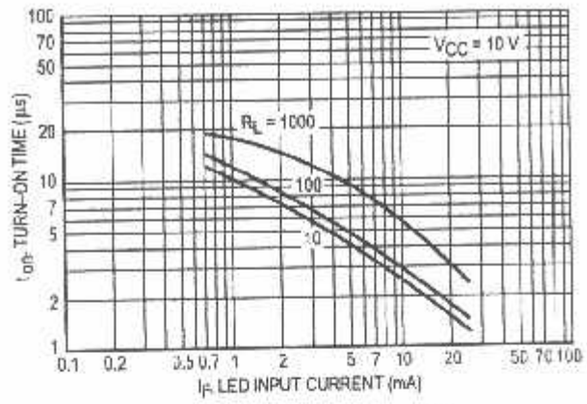


Figure 7. Turn–On Switching Times

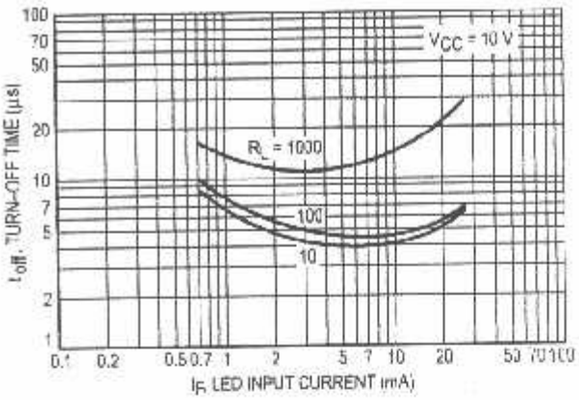


Figure 8. Turn–Off Switching Times

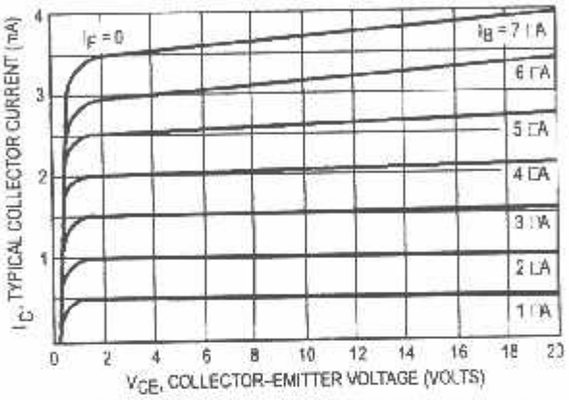


Figure 9. DC Current Gain (Detector Only)

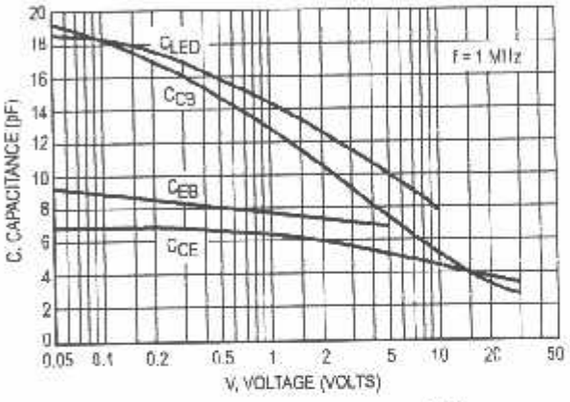


Figure 10. Capacitances versus Voltage

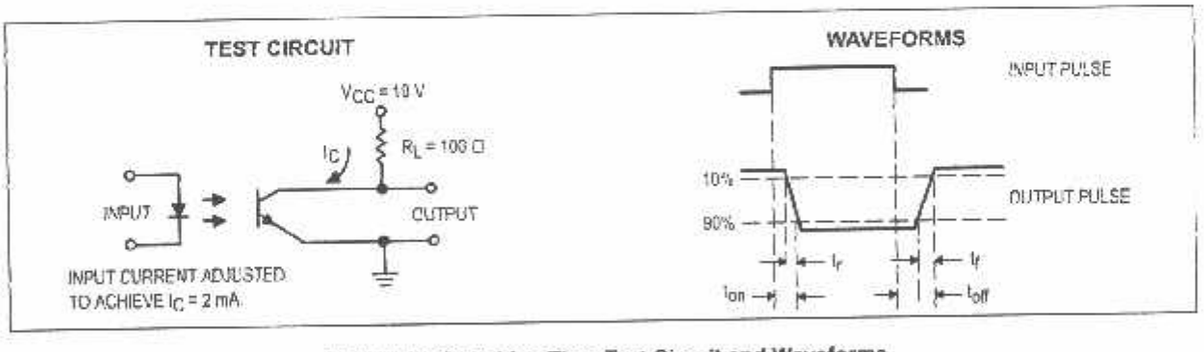
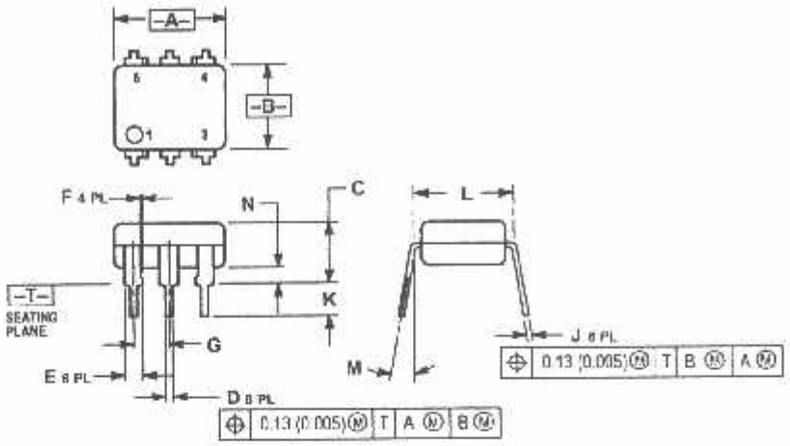


Figure 11. Switching Time Test Circuit and Waveforms

PACKAGE DIMENSIONS

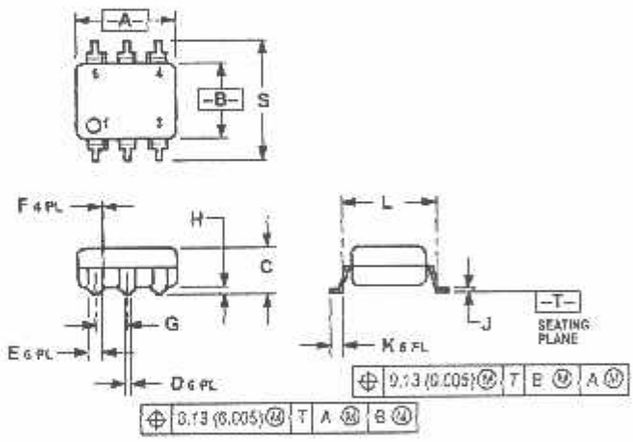


NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. DIMENSION L TO CENTER OF LEAD WHEN FORMED PARALLEL.

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.320	0.350	8.13	8.89
B	0.240	0.260	6.10	6.60
C	0.115	0.200	2.93	5.08
D	0.016	0.020	0.41	0.50
E	0.040	0.070	1.02	1.77
F	0.010	0.014	0.25	0.36
G	0.100 BSC		2.54 BSC	
J	0.008	0.012	0.21	0.30
K	0.100	0.150	2.54	3.81
L	0.300 BSC		7.62 BSC	
M	0°	15°	0°	15°
N	0.015	0.100	0.38	2.54

STYLE 1:
PIN 1. ANODE
2. CATHODE
3. NC
4. EMITTER
5. COLLECTOR
6. BASE

CASE 730A–04
ISSUE G

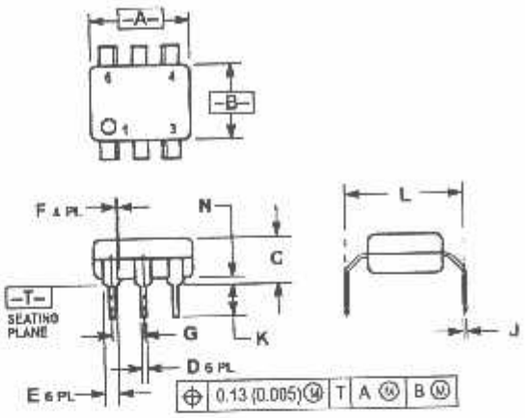


NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.320	0.350	8.13	8.89
B	0.240	0.260	6.10	6.60
C	0.115	0.200	2.93	5.08
D	0.016	0.020	0.41	0.50
E	0.040	0.070	1.02	1.77
F	0.010	0.014	0.25	0.36
G	0.100 BSC		2.54 BSC	
H	0.020	0.025	0.51	0.63
J	0.008	0.012	0.20	0.30
K	0.095	0.105	2.41	2.67
L	0.320 BSC		8.13 BSC	
S	0.332	0.360	8.43	9.14

***Consult factory for leadform option availability**

CASE 730C–04
ISSUE D



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. DIMENSION L TO CENTER OF LEAD WHEN FORMED PARALLEL.

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.320	0.350	8.13	8.89
B	0.240	0.260	6.10	6.60
C	0.115	0.200	2.93	5.08
D	0.016	0.022	0.41	0.56
E	0.040	0.070	1.02	1.77
F	0.010	0.014	0.25	0.36
G	0.100 BSC		2.54 BSC	
J	0.008	0.012	0.21	0.30
K	0.100	0.150	2.54	3.81
L	0.400	0.425	10.16	10.80
N	0.015	0.040	0.38	1.02

***Consult factory for leadform option availability**

CASE 730D–05
ISSUE D

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FAIRCHILD
SEMICONDUCTOR™

October 1989
Revised March 2000

DM74LS47
BCD to 7-Segment Decoder/Driver with Open-Collector Outputs

General Description

The DM74LS47 accepts four lines of BCD (8421) input data, generates their complements internally and decodes the data with seven AND/OR gates having open-collector outputs to drive indicator segments directly. Each segment output is guaranteed to sink 24 mA in the ON (LOW) state and withstand 15V in the OFF (HIGH) state with a maximum leakage current of 250 µA. Auxiliary inputs provided blanking, lamp test and cascadable zero-suppression functions.

Features

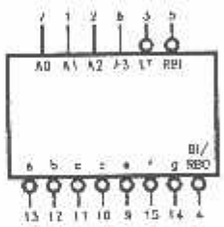
- Open-collector outputs
- Drive indicator segments directly
- Cascadable zero-suppression capability
- Lamp test input

Ordering Code:

Order Number	Package Number	Package Description
DM74LS47M	M16A	16-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-012, 0.150 Narrow
DM74LS47N	N16E	16-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300 Wide

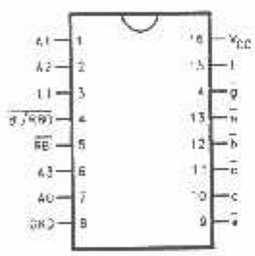
Devices also available in Tape and Reel. Specify by appending the suffix letter "X" to the ordering code.

Logic Symbol



V_{CC} = Pin 16
GND = Pin 8

Connection Diagram



Pin Descriptions

Pin Names	Description
A0–A3	BCD Inputs
$\overline{RBI}$	Ripple Blanking Input (Active LOW)
$\overline{LT}$	Lamp Test Input (Active LOW)
$\overline{BI/RBO}$	Blanking Input (Active LOW) or Ripple Blanking Output (Active LOW)
$\overline{a}$ – $\overline{g}$	Segment Outputs (Active LOW) (Note 1)

Note 1: OC—Open Collector

Truth Table

Decimal or Function	Inputs							Outputs							Note
	$\overline{LT}$	$\overline{RBI}$	A3	A2	A1	A0	$\overline{BI}/\overline{RBO}$	a	b	c	d	e	f	g	
0	H	H	L	L	L	L	H	L	L	L	L	L	L	H	(Note 2)
1	H	X	L	L	L	H	H	H	L	L	H	H	H	H	(Note 2)
2	H	X	L	L	H	L	H	L	L	H	L	L	H	L	
3	H	X	L	L	H	H	H	L	L	L	L	H	H	L	
4	H	X	L	H	L	L	H	H	L	L	H	H	L	L	
5	H	X	L	H	L	H	H	L	H	L	L	H	L	L	
6	H	X	L	H	H	L	H	H	H	L	L	L	L	L	
7	H	X	L	H	H	H	H	L	L	L	H	H	H	H	
8	H	X	H	L	L	L	H	L	L	L	L	L	L	L	
9	H	X	H	L	L	H	H	L	L	L	H	H	L	L	
10	H	X	H	L	H	L	H	H	H	H	L	L	H	L	
11	H	X	H	L	H	H	H	H	H	L	L	H	H	L	
12	H	X	H	H	L	L	H	H	L	H	H	L	L	L	
13	H	X	H	H	L	H	H	L	H	H	L	H	L	L	
14	H	X	H	H	H	L	H	H	H	H	L	L	L	L	
15	H	X	H	H	H	H	H	H	H	H	H	H	H	H	
$\overline{BI}$	X	X	X	X	X	X	L	H	H	H	H	H	H	H	(Note 3)
$\overline{RBI}$	H	L	L	L	L	L	L	H	H	H	H	H	H	H	(Note 4)
$\overline{LT}$	L	X	X	X	X	X	H	L	L	L	L	L	L	L	(Note 5)

Note 2: $\overline{BI}/\overline{RBO}$ is wire-AND logic serving as blanking input ($\overline{BI}$) and/or ripple-blanking output ($\overline{RBO}$). The blanking out $\overline{BI}$ must be open or held at a HIGH level when output functions 0 through 15 are desired, and ripple-blanking input ($\overline{RBI}$) must be open or at a HIGH level if blanking of a decimal 0 is not desired. X = input may be HIGH or LOW.

Note 3: When a LOW level is applied to the blanking input (forced condition) all segment outputs go to a HIGH level regardless of the state of any other input condition.

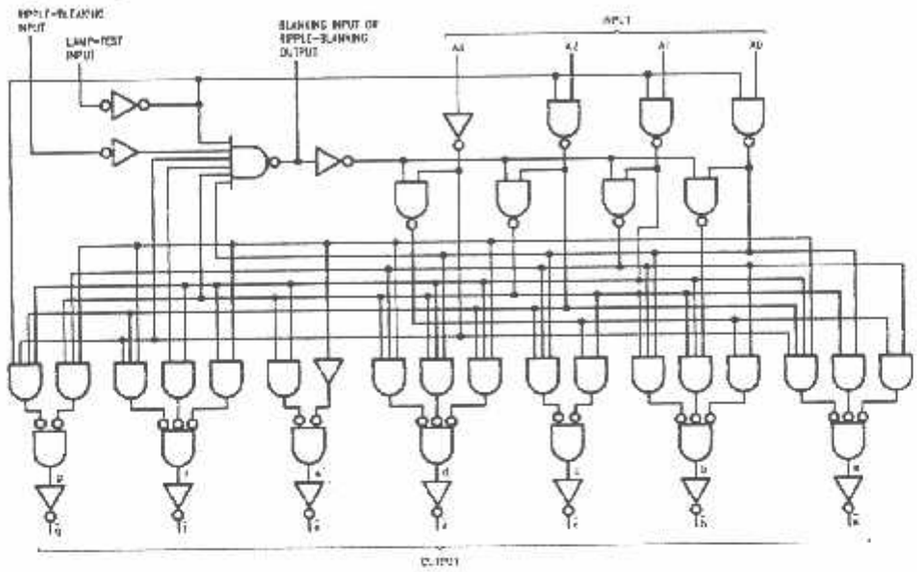
Note 4: When ripple-blanking input ($\overline{RBI}$) and inputs A0, A1, A2 and A3 are LOW level, with the lamp test input at HIGH level, all segment outputs go to a HIGH level and the ripple-blanking output ($\overline{RBO}$) goes to a LOW level (response condition).

Note 5: When the blanking input/ripple-blanking output ($\overline{BI}/\overline{RBO}$) is OPEN or held at a HIGH level, and a LOW level is applied to lamp test input, all segment outputs go to a LOW level.

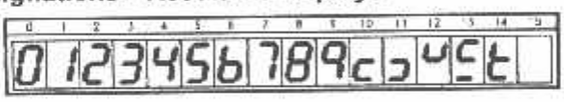
Functional Description

The DM74LS47 decodes the input data in the pattern indicated in the Truth Table and the segment identification illustration. If the input data is decimal zero, a LOW signal applied to the $\overline{RBI}$ blanks the display and causes a multi-digit display. For example, by grounding the $\overline{RBI}$ of the highest order decoder and connecting its $\overline{BI}/\overline{RBO}$ to $\overline{RBI}$ of the next lowest order decoder, etc., leading zeros will be suppressed. Similarly, by grounding $\overline{RBI}$ of the lowest order decoder and connecting its $\overline{BI}/\overline{RBO}$ to $\overline{RBI}$ of the next highest order decoder, etc., trailing zeros will be suppressed. Leading and trailing zeros can be suppressed simultaneously by using external gates, i.e., by driving $\overline{RBI}$ of a intermediate decoder from an OR gate whose inputs are $\overline{BI}/\overline{RBO}$ of the next highest and lowest order decoders. $\overline{BI}/\overline{RBO}$ also serves as an unconditional blanking input. The internal NAND gate that generates the $\overline{RBO}$ signal has a resistive pull-up, as opposed to a totem pole, and thus $\overline{BI}/\overline{RBO}$ can be forced LOW by external means, using wired-collector logic. A LOW signal thus applied to $\overline{BI}/\overline{RBO}$ turns off all segment outputs. This blanking feature can be used to control display intensity by varying the duty cycle of the blanking signal. A LOW signal applied to $\overline{LT}$ turns on all segment outputs, provided that $\overline{BI}/\overline{RBO}$ is not forced LOW.

Logic Diagram



Numerical Designations—Resultant Displays



Absolute Maximum Ratings(Note 6)

Supply Voltage	7V
Input Voltage	7V
Operating Free Air Temperature Range	0°C to +70°C
Storage Temperature Range	−65°C to +150°C

Note 6: The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the Electrical Characteristics tables are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

Recommended Operating Conditions

Symbol	Parameter	Min	Nom	Max	Units
V_{CC}	Supply Voltage	4.75	5	5.25	V
V_{IH}	HIGH Level Input Voltage	2			V
V_{IL}	LOW Level Input Voltage			0.8	V
I_{OH}	HIGH Level Output Current $\bar{a}-\bar{g}$ @ 15V − V_{OH} (Note 7)			-250	µA
I_{OH}	HIGH Level Output Current $\overline{BI}/\overline{RBO}$			-50	µA
I_{OL}	LOW Level Output Current			24	mA
T_A	Free Air Operating Temperature	0		70	°C

Note 7: OFF-State at $\bar{a}-\bar{g}$.

Electrical Characteristics

Over recommended operating free air temperature range (unless otherwise noted)

Symbol	Parameter	Conditions	Min	Typ (Note 8)	Max	Units
V_I	Input Clamp Voltage	V_{CC} = Min, I_I = −18 mA			−1.5	V
V_{OH}	HIGH Level Output Voltage	V_{CC} = Min, I_{OH} = Max, V_{IL} = Max, $\overline{BI}/\overline{RBO}$	2.7	3.4		V
$I_{O(H)}$	Output HIGH Current Segment Outputs	V_{CC} = 5.25V, V_O = 15V $\bar{a}-\bar{g}$			250	µA
V_{OL}	LOW Level Output Voltage	V_{CC} = Min, I_{OL} = Max, V_{IH} = Min, $\bar{a}-\bar{g}$		0.35	0.5	V
		I_{OL} = 3.2 mA, $\overline{BI}/\overline{RBO}$			0.5	
		I_{OL} = 12 mA, $\bar{a}-\bar{g}$		0.25	0.4	
		I_{OL} = 4.8 mA, $\overline{BI}/\overline{RBO}$			0.4	
I_I	Input Current @ Max Input Voltage	V_{CC} = Max, V_I = 7V			100	µA
		V_{CC} = Max, V_I = 10V			200	µA
I_{IH}	HIGH Level Input Current	V_{CC} = Max, V_I = 2.7V			20	µA
I_{IL}	LOW Level Input Current	V_{CC} = Max, V_I = 0.4V			-0.4	mA
I_{OS}	Short Circuit Output Current	V_{CC} = Max (Note 9), I_{OS} at $\overline{BI}/\overline{RBO}$	-0.3		-2.0	mA
I_{CC}	Supply Current	V_{CC} = Max			13	mA

Note 8: All typicals are at V_{CC} = 5V, T_A = 25°C.

Note 9: Not more than one output should be shorted at a time, and the duration should not exceed one second.

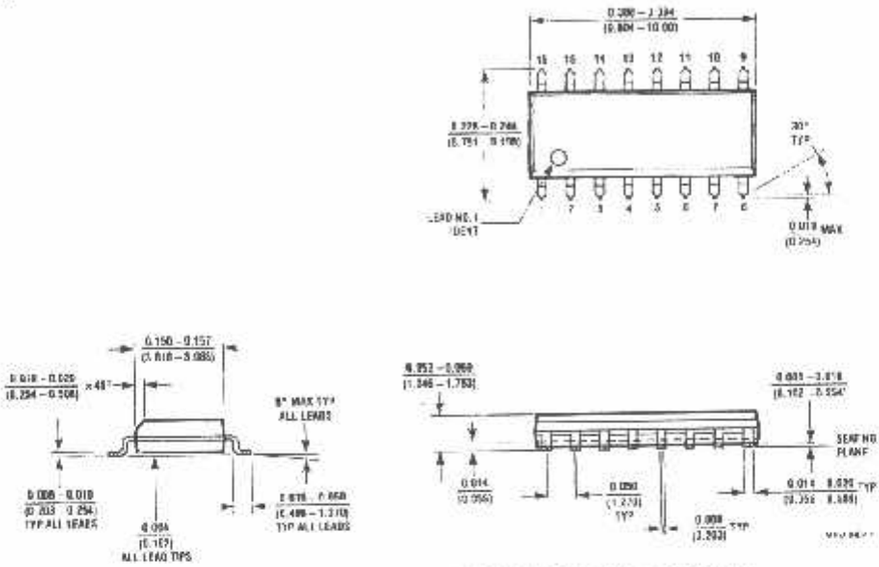
Switching Characteristics

at V_{CC} = +5.0V, T_A = +25°C

Symbol	Parameter	Conditions	R_L = 665Ω, C_L = 15 pF		Units
			Min	Max	
t_{PLH} t_{PHL}	Propagation Delay An to $\bar{a}-\bar{g}$			100 100	ns
t_{PLH} t_{PHL}	Propagation Delay $\overline{RBI}$ to $\bar{a}-\bar{g}$ (Note 10)			100 100	ns

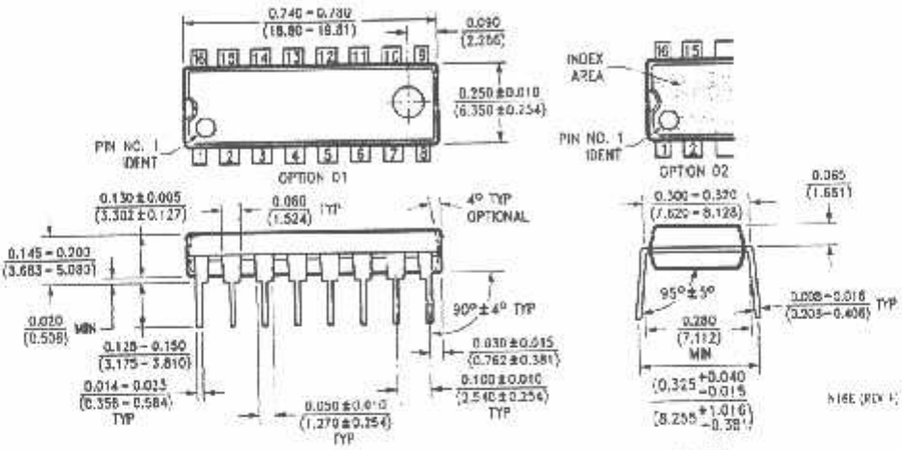
Note 10: $\overline{LT}$ = HIGH, All A's = LOW

Physical Dimensions inches (millimeters) unless otherwise noted



16-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-012, 0.150 Narrow
Package Number M16A

Physical Dimensions inches (millimeters) unless otherwise noted (Continued)



16-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300 Wide
Package Number N16E

Analog Multiplexers/Demultiplexers

MC14051B
MC14052B
MC14053B

The MC14051B, MC14052B, and MC14053B analog multiplexers are digitally–controlled analog switches. The MC14051B effectively implements an SP8T solid state switch, the MC14052B a DP4T, and the MC14053B a Triple SPDT. All three devices feature low ON impedance and very low OFF leakage current. Control of analog signals up to the complete supply voltage range can be achieved.

- Triple Diode Protection on Control Inputs
- Switch Function is Break Before Make
- Supply Voltage Range = 3.0 Vdc to 18 Vdc
- Analog Voltage Range ($V_{DD} - V_{EE}$) = 3.0 to 18 V
  Note: V_{EE} must be ≤ V_{SS}
- Linearized Transfer Characteristics
- Low–noise – 12 nV/√Cycle, f ≥ 1.0 kHz Typical
- Pin–for–Pin Replacement for CD4051, CD4052, and CD4053
- For 4PDT Switch, See MC14551B
- For Lower R_{ON}, Use the HC4051, HC4052, or HC4053 High–Speed CMOS Devices

L SUFFIX
CERAMIC
CASE 620

P SUFFIX
PLASTIC
CASE 648

D SUFFIX
SOIC
CASE 751B

ORDERING INFORMATION

MC14XXXBCP	Plastic
MC14XXXBCL	Ceramic
MC14XXXBD	SOIC

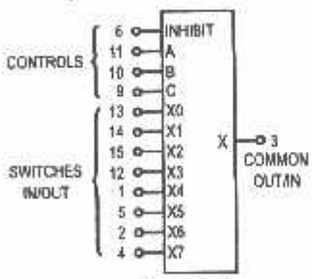
T_A = – 55° to 125°C for all packages.

MAXIMUM RATINGS*

Symbol	Parameter	Value	Unit
V_{DD}	DC Supply Voltage (Referenced to V_{EE}, $V_{SS} \geq V_{EE}$)	– 0.5 to + 18.0	V
V_{in}, V_{out}	Input or Output Voltage (DC or Transient) (Referenced to V_{SS} for Control Inputs and V_{EE} for Switch I/O)	– 0.5 to V_{DD} + 0.5	V
I_{in}	Input Current (DC or Transient), per Control Pin	± 10	mA
I_{sw}	Switch Through Current	± 25	mA
P_D	Power Dissipation, per Package†	500	mW
T_{stg}	Storage Temperature	– 65 to + 150	°C
T_L	Lead Temperature (8–Second Soldering)	260	°C

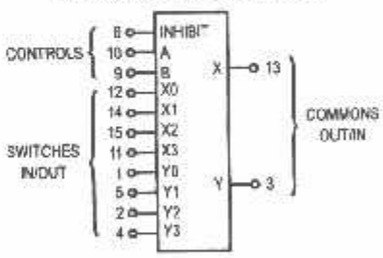
* Maximum Ratings are those values beyond which damage to the device may occur.
†Temperature Derating: "P and D/DW" Packages: – 7.0 mW/°C From 65°C To 125°C
Ceramic "L" Packages: – 12 mW/°C From 100°C To 125°C

MC14051B
8–Channel Analog Multiplexer/Demultiplexer



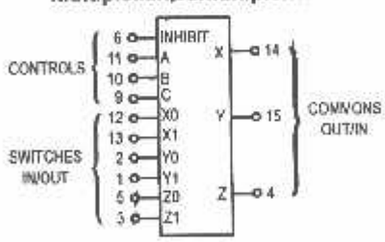
V_{DD} = PIN 16
V_{SS} = PIN 8
V_{EE} = PIN 7

MC14052B
Dual 4–Channel Analog Multiplexer/Demultiplexer



V_{DD} = PIN 16
V_{SS} = PIN 8
V_{EE} = PIN 7

MC14053B
Triple 2–Channel Analog Multiplexer/Demultiplexer



V_{DD} = PIN 16
V_{SS} = PIN 8
V_{EE} = PIN 7

Note: Control Inputs referenced to V_{SS}. Analog Inputs and Outputs reference to V_{EE}. V_{EE} must be ≤ V_{SS}.

ELECTRICAL CHARACTERISTICS

Characteristic	Symbol	V_{DD}	Test Conditions	−55°C Min	−55°C Max	25°C Min	25°C Typ #	25°C Max	125°C Min	125°C Max	Unit
SUPPLY REQUIREMENTS (Voltages Referenced to V_{EE})											
Power Supply Voltage Range	V_{DD}	—	$V_{DD} - 3.0 \geq V_{SS} \geq V_{EE}$	3.0	18	3.0	—	18	3.0	18	V
Quiescent Current Per Package	I_{DD}	5.0 10 15	Control Inputs: $V_{in} = V_{SS}$ or V_{DD}. Switch I/O: $V_{EE} \leq V_{I/O} \leq V_{DD}$, and $\Delta V_{switch} \leq 500$ mV**	— — —	5.0 10 20	— — —	0.005 0.010 0.015	5.0 10 20	— — —	150 300 600	µA
Total Supply Current (Dynamic Plus Quiescent, Per Package	$I_{D(AV)}$	5.0 10 15	$T_A = 25°C$ only (The channel component, $(V_{in} - V_{out})/R_{on}$, is not included.)	Typical			(0.07 µA/kHz) f + I_{DD} (0.20 µA/kHz) f + I_{DD} (0.36 µA/kHz) f + I_{DD}				µA
CONTROL INPUTS — INHIBIT, A, B, C (Voltages Referenced to V_{SS})											
Low–Level Input Voltage	V_{IL}	5.0 10 15	R_{on} = per spec, I_{off} = per spec	— — —	1.5 3.0 4.0	— — —	2.25 4.50 6.75	1.5 3.0 4.0	— — —	1.5 3.0 4.0	V
High–Level Input Voltage	V_{IH}	5.0 10 15	R_{on} = per spec, I_{off} = per spec	3.5 7.0 11	— — —	3.5 7.0 11	2.75 5.50 8.25	— — —	3.5 7.0 11	— — —	V
Input Leakage Current	I_{in}	15	V_{in} = 0 or V_{DD}	—	±0.1	—	±0.00001	±0.1	—	1.0	µA
Input Capacitance	C_{in}	—		—	—	—	5.0	7.5	—	—	pF
SWITCHES IN/OUT AND COMMONS OUT/IN — X, Y, Z (Voltages Referenced to V_{EE})											
Recommended Peak–to–Peak Voltage Into or Out of the Switch	$V_{I/O}$	—	Channel On or Off	0	V_{DD}	0	—	V_{DD}	0	V_{DD}	V_{PP}
Recommended Static or Dynamic Voltage Across the Switch** (Figure 5)	ΔV_{switch}	—	Channel On	0	600	0	—	600	0	300	mV
Output Offset Voltage	V_{OO}	—	V_{in} = 0 V, No Load	—	—	—	10	—	—	—	µV
ON Resistance	R_{on}	5.0 10 15	$\Delta V_{switch} \leq 500$ mV**, $V_{in} = V_{IL}$ or V_{IH} (Control), and V_{in} = 0 to V_{DD} (Switch)	— — —	800 400 220	— — —	250 120 80	1050 500 280	— — —	1200 520 300	Ω
ΔON Resistance Between Any Two Channels in the Same Package	ΔR_{on}	5.0 10 15		— — —	70 50 45	— — —	25 10 10	70 50 45	— — —	135 95 65	Ω
Off–Channel Leakage Current (Figure 10)	I_{off}	15	$V_{in} = V_{IL}$ or V_{IH} (Control) Channel to Channel or Any One Channel	—	±100	—	±0.05	±100	—	±1000	nA
Capacitance, Switch I/O	$C_{I/O}$	—	Inhibit = V_{DD}	—	—	—	10	—	—	—	pF
Capacitance, Common O/I	$C_{O/I}$	—	Inhibit = V_{DD} (MC14051B) (MC14052B) (MC14053B)	— — —	— — —	— — —	60 32 17	— — —	— — —	— — —	pF
Capacitance, Feedthrough (Channel Off)	$C_{I/O}$	— —	Pins Not Adjacent Pins Adjacent	— —	— —	— —	0.15 0.47	— —	— —	— —	pF

#Data labeled "Typ" is not to be used for design purposes, but is intended as an indication of the IC's potential performance.

* For voltage drops across the switch (ΔV_{switch}) > 600 mV (> 300 mV at high temperature), excessive V_{DD} current may be drawn, i.e. the current out of the switch may contain both V_{DD} and switch input components. The reliability of the device will be unaffected unless the Maximum Ratings are exceeded. (See first page of this data sheet.)

ELECTRICAL CHARACTERISTICS* (C_L = 50 pF, T_A = 25°C) ($V_{EE} \leq V_{SS}$ unless otherwise indicated)

Characteristic	Symbol	$V_{DD} - V_{EE}$ Vdc	Typ # All Types	Max	Unit
Propagation Delay Times (Figure 6) Switch Input to Switch Output (R_L = 10 kΩ)	t_{PLH}, t_{PHL}				ns
MC14051					
t_{PLH}, t_{PHL} = (0.17 ns/pF) C_L + 26.5 ns		5.0	35	90	
t_{PLH}, t_{PHL} = (0.08 ns/pF) C_L + 11 ns		10	15	40	
t_{PLH}, t_{PHL} = (0.06 ns/pF) C_L + 9.0 ns		15	12	30	
MC14052					ns
t_{PLH}, t_{PHL} = (0.17 ns/pF) C_L + 21.5 ns		5.0	30	75	
t_{PLH}, t_{PHL} = (0.08 ns/pF) C_L + 8.0 ns		10	12	30	
t_{PLH}, t_{PHL} = (0.06 ns/pF) C_L + 7.0 ns		15	10	25	
MC14053					ns
t_{PLH}, t_{PHL} = (0.17 ns/pF) C_L + 16.5 ns		5.0	25	65	
t_{PLH}, t_{PHL} = (0.08 ns/pF) C_L + 4.0 ns		10	8.0	20	
t_{PLH}, t_{PHL} = (0.06 ns/pF) C_L + 3.0 ns		15	6.0	15	
Inhibit to Output (R_L = 10 kΩ, $V_{EE} = V_{SS}$) Output "1" or "0" to High Impedance, or High Impedance to "1" or "0" Level	t_{PHZ}, t_{PLZ}, t_{PZH}, t_{PZL}				ns
MC14051B		5.0	350	700	
		10	170	340	
		15	140	280	
MC14052B		5.0	300	600	ns
		10	155	310	
		15	125	250	
MC14053B		5.0	275	550	ns
		10	140	280	
		15	110	220	
Control Input to Output (R_L = 10 kΩ, $V_{EE} = V_{SS}$)	t_{PLH}, t_{PHL}				ns
MC14051B		5.0	360	720	
		10	160	320	
		15	120	240	
MC14052B		5.0	325	650	ns
		10	130	260	
		15	90	180	
MC14053B		5.0	300	600	ns
		10	120	240	
		15	80	160	
Second Harmonic Distortion (R_L = 10KΩ, f = 1 kHz) V_{in} = 5 VPP	—	10	0.07	—	%
Bandwidth (Figure 7) (R_L = 1 kΩ, V_{in} = 1/2 (V_{DD}–V_{EE}) p–p, C_L = 50pF 20 Log (V_{out}/V_{in}) = – 3 dB)	BW	10	17	—	MHz
Off Channel Feedthrough Attenuation (Figure 7) R_L = 1KΩ, V_{in} = 1/2 ($V_{DD} - V_{EE}$) p–p	—	10	– 50	—	dB
f_{in} = 4.5 MHz — MC14051B					
f_{in} = 30 MHz — MC14052B					
f_{in} = 55 MHz — MC14053B					
Channel Separation (Figure 8) (R_L = 1 kΩ, V_{in} = 1/2 (V_{DD}–V_{EE}) p–p, f_{in} = 3.0 MHz	—	10	– 50	—	dB
Crosstalk, Control Input to Common O/I (Figure 9) (R_1 = 1 kΩ, R_L = 10 kΩ Control $t_{TLH} = t_{THL}$ = 20 ns, Inhibit = V_{SS})	—	10	75	—	mV

* The formulas given are for the typical characteristics only at 25°C.
#Data labelled "Typ" is not to be used for design purposes but is intended as an indication of the IC's potential performance.

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation, V_{in} and V_{out} should be constrained to the range $V_{SS} \leq (V_{in}$ or $V_{out}) \leq V_{DD}$.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either V_{SS}, V_{EE}, or V_{DD}). Unused outputs must be left open.

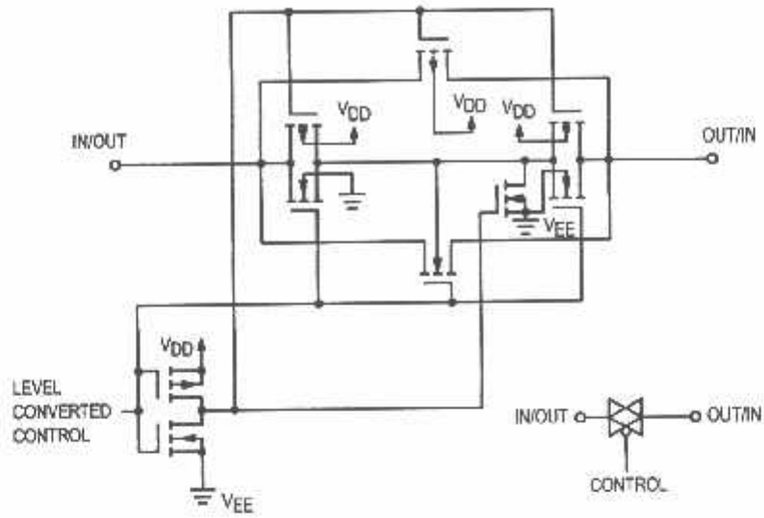


Figure 1. Switch Circuit Schematic

TRUTH TABLE

Control Inputs				ON Switches					
	Select								
Inhibit	C*	B	A	MC14051B	MC14052B		MC14053B		
0	0	0	0	X0	Y0	X0	Z0	Y0	X0
0	0	0	1	X1	Y1	X1	Z0	Y0	X1
0	0	1	0	X2	Y2	X2	Z0	Y1	X0
0	0	1	1	X3	Y3	X3	Z0	Y1	X1
0	1	0	0	X4			Z1	Y0	X0
0	1	0	1	X5			Z1	Y0	X1
0	1	1	0	X6			Z1	Y1	X0
0	1	1	1	X7			Z1	Y1	X1
1	x	x	x	None	None		None		

*Not applicable for MC14052
x = Don't Care

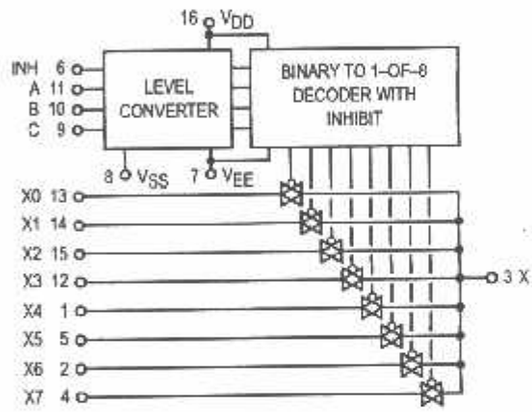


Figure 2. MC14051B Functional Diagram

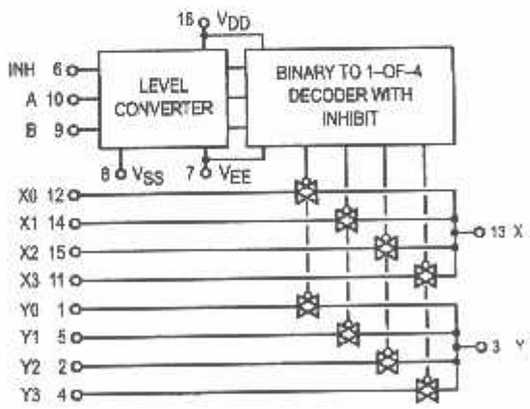


Figure 3. MC14052B Functional Diagram

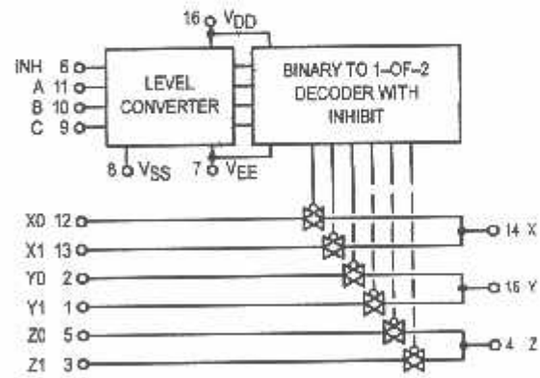


Figure 4. MC14053B Functional Diagram

TEST CIRCUITS

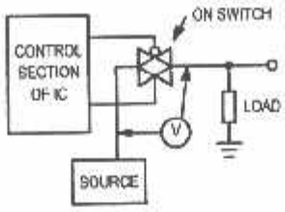


Figure 5. ΔV Across Switch

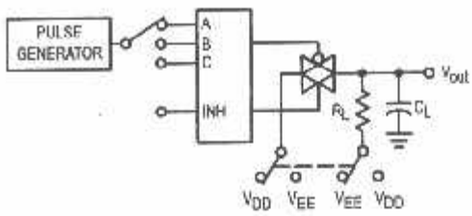


Figure 6. Propagation Delay Times, Control and Inhibit to Output

A, B, and C inputs used to turn ON or OFF the switch under test.

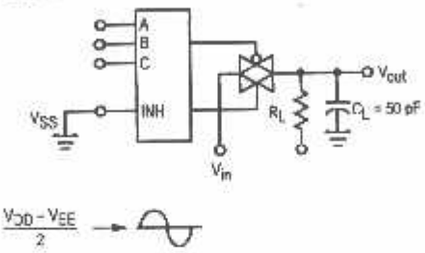


Figure 7. Bandwidth and Off–Channel Feedthrough Attenuation

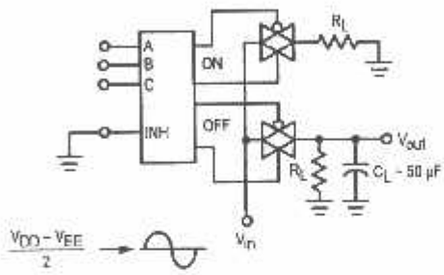


Figure 8. Channel Separation (Adjacent Channels Used For Setup)

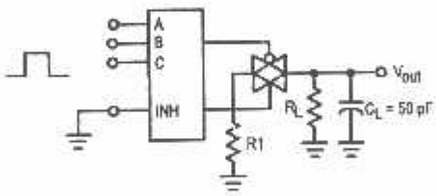


Figure 9. Crosstalk, Control Input to Common O/I

NOTE: See also Figures 7 and 8 on Page 6–51.

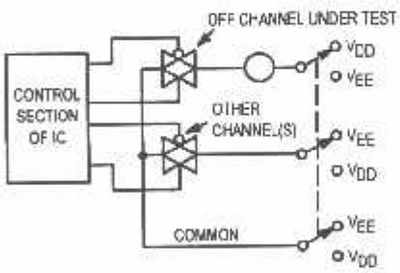


Figure 10. Off Channel Leakage

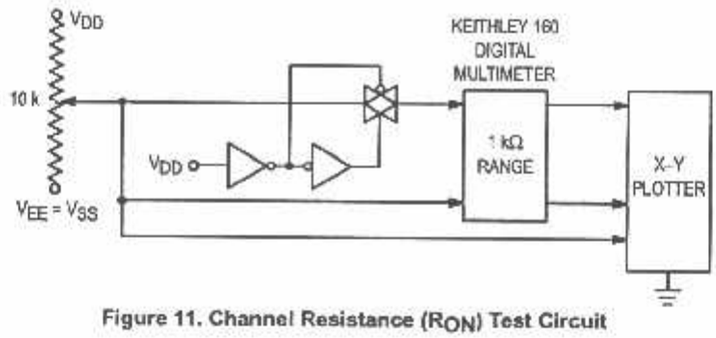


Figure 11. Channel Resistance (R_{ON}) Test Circuit

TYPICAL RESISTANCE CHARACTERISTICS

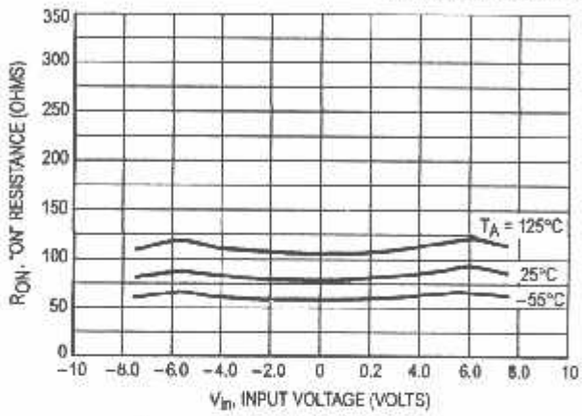


Figure 12. V_{DD} = 7.5 V, V_{EE} = – 7.5 V

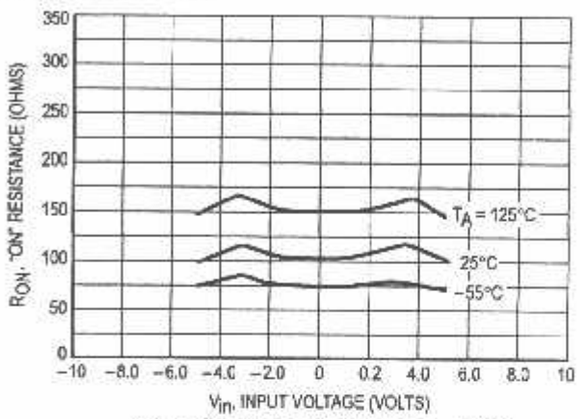


Figure 13. V_{DD} = 5.0 V, V_{EE} = – 5.0 V

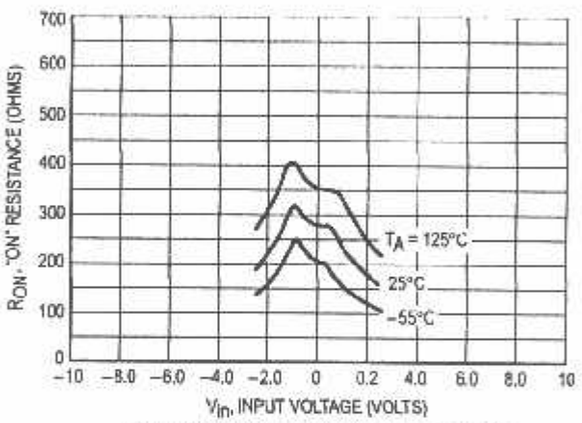


Figure 14. V_{DD} = 2.5 V, V_{EE} = – 2.5 V

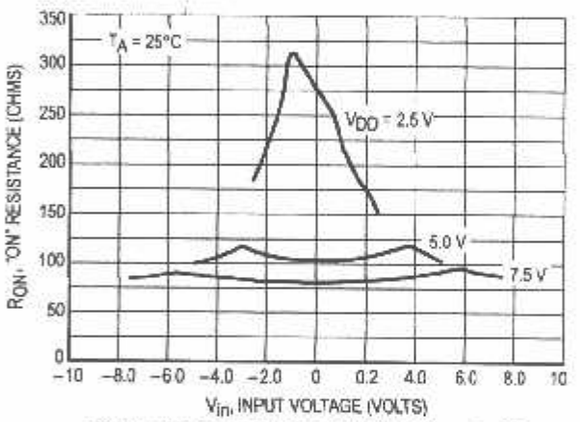
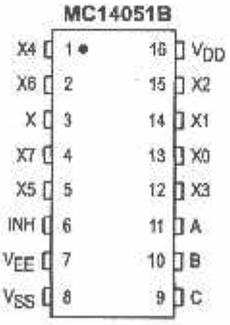


Figure 15. Comparison at 25°C, V_{DD} = –V_{EE}

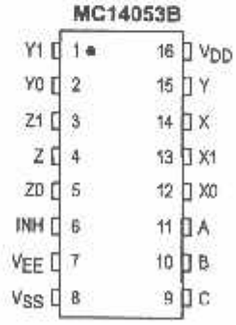
PIN ASSIGMENT

MC14051B



MC14052B

MC14053B



APPLICATIONS INFORMATION

Figure A illustrates use of the on–chip level converter detailed in Figures 2, 3, and 4. The 0–to–5 V Digital Control signal is used to directly control a 9 V_{p-p} analog signal.

The digital control logic levels are determined by V_{DD} and V_{SS}. The V_{DD} voltage is the logic high voltage; the V_{SS} voltage is logic low. For the example, V_{DD} = + 5 V = logic high at the control inputs; V_{SS} = GND = 0 V = logic low.

The maximum analog signal level is determined by V_{DD} and V_{EE}. The V_{DD} voltage determines the maximum recommended peak above V_{SS}. The V_{EE} voltage determines the maximum swing below V_{SS}. For the example, $V_{DD} - V_{SS}$ = 5 V maximum swing above V_{SS}; $V_{SS} - V_{EE}$ = 5 V maximum swing below V_{SS}. The example shows a ± 4.5 V signal which allows a 1/2 volt margin at each peak. If voltage transients above V_{DD} and/or below V_{EE} are anticipated on the analog channels, external diodes (Dx) are recommended as shown in Figure B. These diodes should be small signal types able to absorb the maximum anticipated current surges during clipping.

The *absolute* maximum potential difference between V_{DD} and V_{EE} is 18.0 V. Most parameters are specified up to 15 V which is the *recommended* maximum difference between V_{DD} and V_{EE}.

Balanced supplies are not required. However, V_{SS} must be greater than or equal to V_{EE}. For example, V_{DD} = + 10 V, V_{SS} = + 5 V, and V_{EE} = − 3 V is acceptable. See the Table below.

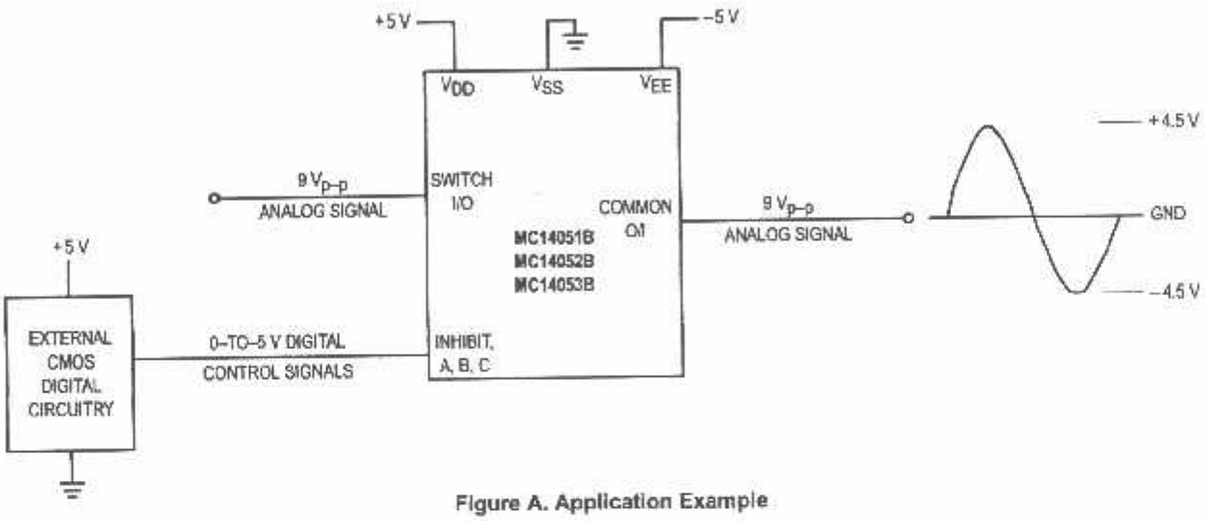


Figure A. Application Example

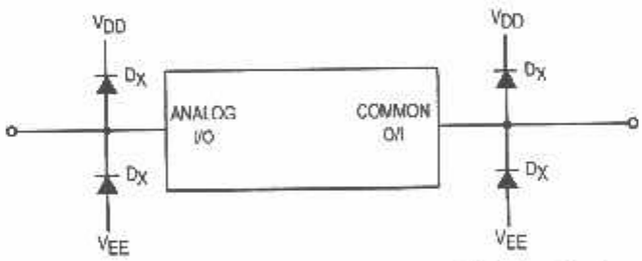


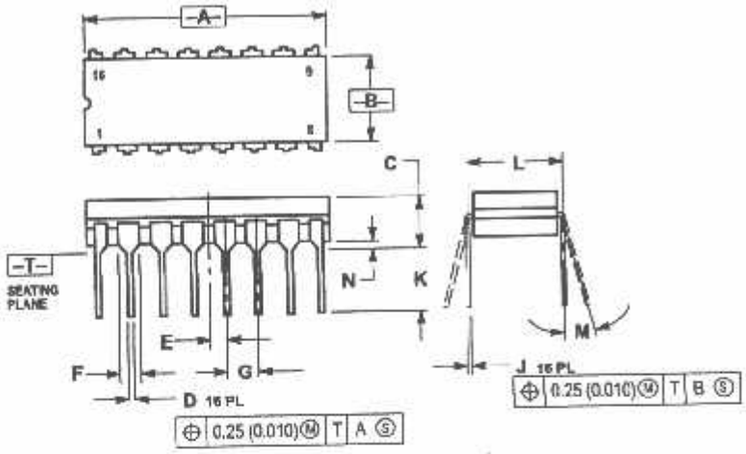
Figure B. External Germanium or Schottky Clipping Diodes

POSSIBLE SUPPLY CONNECTIONS

V_{DD} In Volts	V_{SS} In Volts	V_{EE} In Volts	Control Inputs Logic High/Logic Low In Volts	Maximum Analog Signal Range In Volts
+ 8	0	− 8	+ 8/0	+ 8 to − 8 = 16 V_{p-p}
+ 5	0	− 12	+ 5/0	+ 5 to − 12 = 17 V_{p-p}
+ 5	0	0	+ 5/0	+ 5 to 0 = 5 V_{p-p}
+ 5	0	− 5	+ 5/0	+ 5 to − 5 = 10 V_{p-p}
+ 10	+ 5	− 5	+ 10/ + 5	+ 10 to − 5 = 15 V_{p-p}

OUTLINE DIMENSIONS

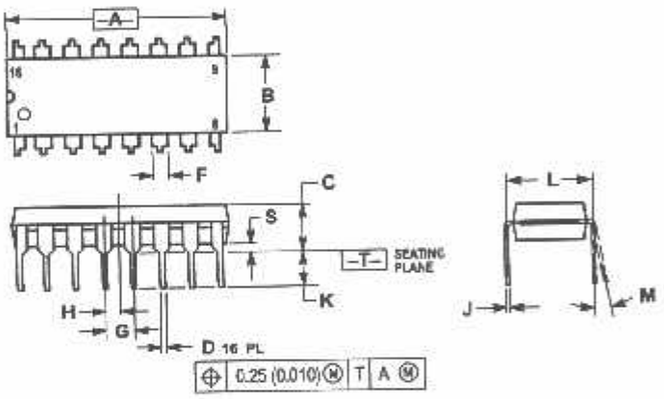
L SUFFIX
CERAMIC DIP PACKAGE
CASE 620–10
ISSUE V



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. DIMENSION L TO CENTER OF LEAD WHEN FORMED PARALLEL.
4. DIMENSION F MAY NARROW TO 0.76 (0.030) WHERE THE LEAD ENTERS THE CERAMIC BODY.

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.750	0.785	19.05	19.93
B	0.240	0.295	6.10	7.49
C	—	0.200	—	5.08
D	0.015	0.020	0.39	0.50
E	0.050 BSC		1.27 BSC	
F	0.055	0.065	1.40	1.65
G	0.100 BSC		2.54 BSC	
H	0.008	0.015	0.21	0.38
K	0.125	0.170	3.18	4.31
L	0.300 BSC		7.62 BSC	
M	0°	15°	0°	15°
N	0.020	0.040	0.51	1.01

P SUFFIX
PLASTIC DIP PACKAGE
CASE 648–08
ISSUE R

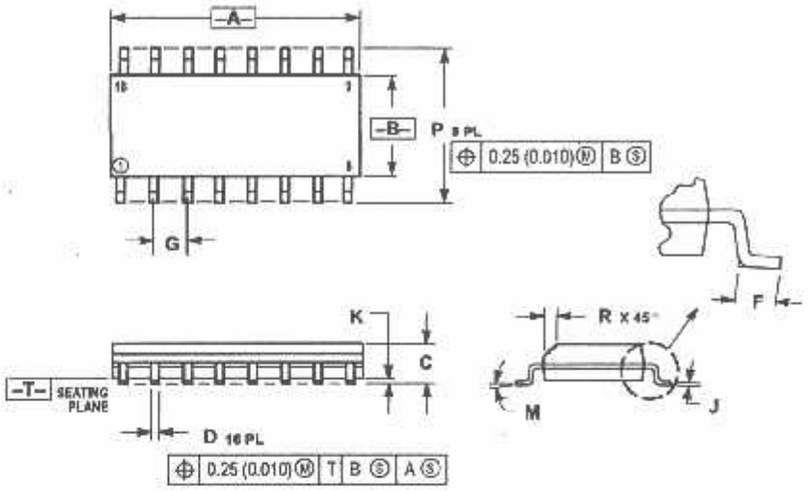


NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. DIMENSION L TO CENTER OF LEADS WHEN FORMED PARALLEL.
4. DIMENSION B DOES NOT INCLUDE MOLD FLASH.
5. ROUNDED CORNERS OPTIONAL.

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.740	0.770	18.80	19.55
B	0.250	0.270	6.35	6.85
C	0.145	0.175	3.69	4.44
D	0.015	0.021	0.39	0.53
F	0.040	0.70	1.02	1.77
G	0.100 BSC		2.54 BSC	
H	0.050 BSC		1.27 BSC	
J	0.008	0.015	0.21	0.38
K	0.110	0.130	2.80	3.30
L	0.295	0.305	7.50	7.74
M	0°	10°	0°	10°
S	0.020	0.040	0.51	1.01

OUTLINE DIMENSIONS

D SUFFIX
PLASTIC SOIC PACKAGE
CASE 751B–05
ISSUE J



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSIONS A AND B DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
5. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127 (0.005) TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	9.80	10.00	0.386	0.393
B	3.80	4.00	0.150	0.157
C	1.35	1.75	0.054	0.068
D	0.35	0.49	0.014	0.019
F	0.40	1.25	0.016	0.049
G	1.27 BSC		0.050 BSC	
J	0.19	0.25	0.008	0.009
K	0.10	0.25	0.004	0.009
M	0°	7°	0°	7°
P	5.80	6.20	0.229	0.244
R	0.25	0.50	0.010	0.019

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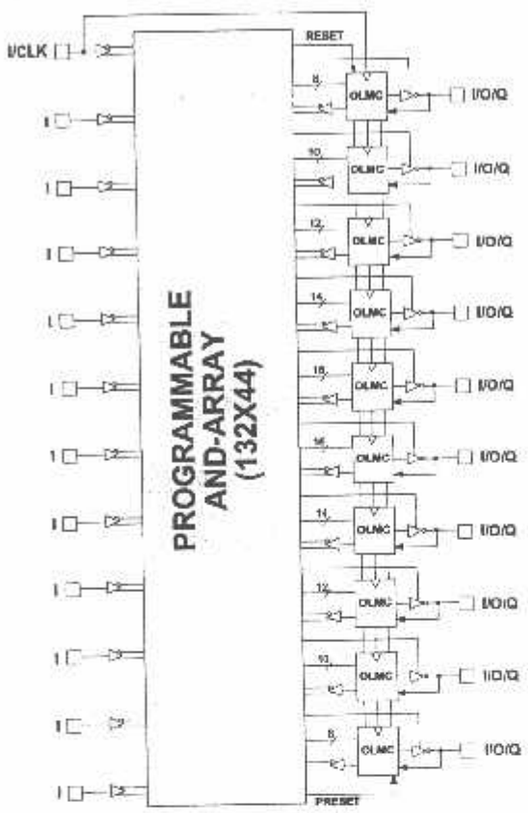
Low Voltage E²CMOS PLD Generic Array Logic™

Features

- HIGH PERFORMANCE E²CMOS® TECHNOLOGY
  - 4 ns Maximum Propagation Delay
  - Fmax = 250 MHz
  - 3 ns Maximum from Clock Input to Data Output
  - UltraMOS® Advanced CMOS Technology
- 3.3V LOW VOLTAGE 22V10 ARCHITECTURE
  - JEDEC-Compatible 3.3V Interface Standard
  - 5V Compatible Inputs
  - I/O Interfaces with Standard 5V TTL Devices (GAL22LV10C)
- ACTIVE PULL-UPS ON ALL PINS (GAL22LV10D)
- E² CELL TECHNOLOGY
  - Reconfigurable Logic
  - Reprogrammable Cells
  - 100% Tested/100% Yields
  - High Speed Electrical Erasure (<100ms)
  - 20 Year Data Retention
- TEN OUTPUT LOGIC MACROCELLS
  - Maximum Flexibility for Complex Logic Designs
  - Programmable Output Polarity
- PRELOAD AND POWER-ON RESET OF ALL REGISTERS
  - 100% Functional Testability
- APPLICATIONS INCLUDE:
  - Glue Logic for 3.3V Systems
  - DMA Control
  - State Machine Control
  - High Speed Graphics Processing
  - Standard Logic Speed Upgrade
- ELECTRONIC SIGNATURE FOR IDENTIFICATION

Functional Block Diagram



Description

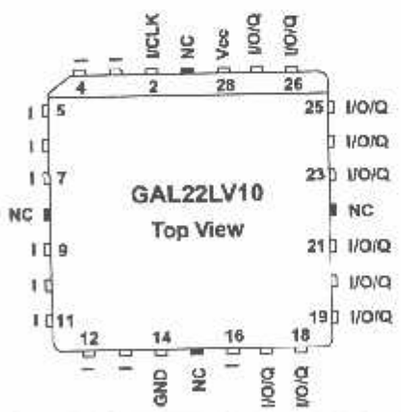
The GAL22LV10D, at 4 ns maximum propagation delay time, provides the highest speed performance available in the PLD market. The GAL22LV10C can interface with both 3.3V and 5V signal levels. The GAL22LV10 is manufactured using Lattice Semiconductor's advanced 3.3V E²CMOS process, which combines CMOS with Electrically Erasable (E²) floating gate technology. High speed erase times (<100ms) allow the devices to be reprogrammed quickly and efficiently.

The generic architecture provides maximum design flexibility by allowing the Output Logic Macrocell (OLMC) to be configured by the user.

Unique test circuitry and reprogrammable cells allow complete AC, DC, and functional testing during manufacture. As a result, Lattice Semiconductor delivers 100% field programmability and functionality of all GAL products. In addition, 100 erase/write cycles and data retention in excess of 20 years are specified.

Pin Configuration

PLCC



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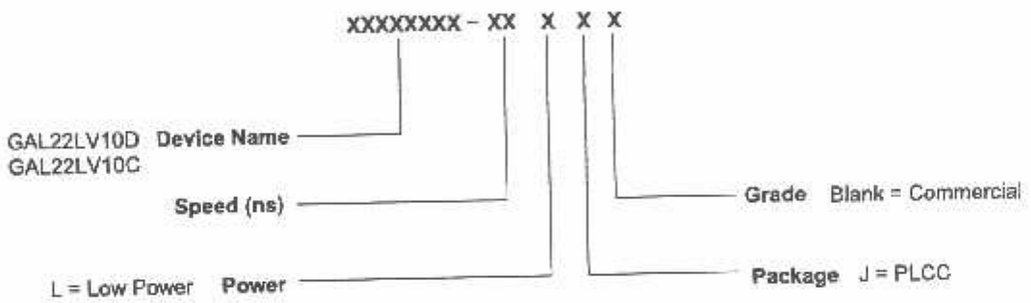
June 2002

GAL22LV10 Ordering Information

Commercial Grade Specifications

Tpd (ns)	Tsu (ns)	Tco (ns)	Icc (mA)	Ordering #	Package
4	3	3	130	GAL22LV10D-4LJ	28-Lead PLCC
5	3.5	3.5	130	GAL22LV10D-5LJ	28-Lead PLCC
7.5	6.5	5	75	GAL22LV10C-7LJ	28-Lead PLCC
10	7.5	6.5	75	GAL22LV10C-10LJ	28-Lead PLCC
15	10	10	75	GAL22LV10C-15LJ	28-Lead PLCC

Part Number Description



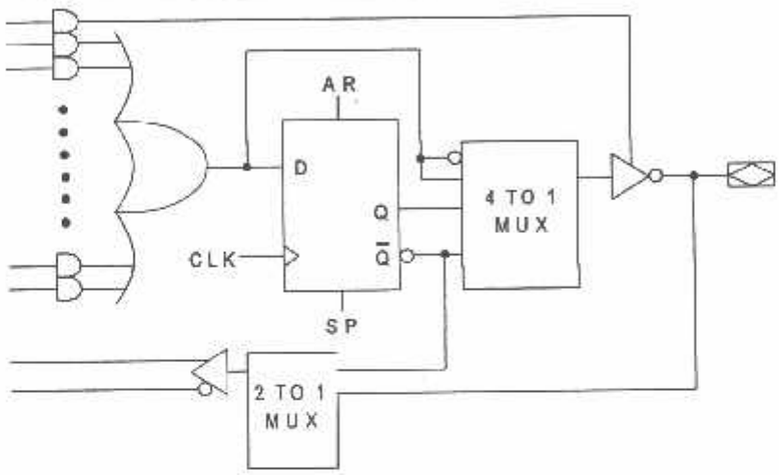
Output Logic Macrocell (OLMC)

The GAL22LV10 has a variable number of product terms per OLMC. Of the ten available OLMCs, two OLMCs have access to eight product terms (pins 17 and 27), two have ten product terms (pins 18 and 26), two have twelve product terms (pins 19 and 25), two have fourteen product terms (pins 20 and 24), and two OLMCs have sixteen product terms (pins 21 and 23). In addition to the product terms available for logic, each OLMC has an additional product-term dedicated to output enable control.

The output polarity of each OLMC can be individually programmed to be true or inverting, in either combinatorial or registered mode. This allows each output to be individually configured as either active high or active low.

The GAL22LV10 has a product term for Asynchronous Reset (AR) and a product term for Synchronous Preset (SP). These two product terms are common to all registered OLMCs. The Asynchronous Reset sets all registers to zero any time this dedicated product term is asserted. The Synchronous Preset sets all registers to a logic one on the rising edge of the next clock pulse after this product term is asserted.

NOTE: The AR and SP product terms will force the Q output of the flip-flop into the same state regardless of the polarity of the output. Therefore, a reset operation, which sets the register output to a zero, may result in either a high or low at the output pin, depending on the pin polarity chosen.



GAL22LV10 OUTPUT LOGIC MACROCELL (OLMC)

Output Logic Macrocell Configurations

Each of the Macrocells of the GAL22LV10 has two primary functional modes: registered, and combinatorial I/O. The modes and the output polarity are set by two bits (SO and S1), which are normally controlled by the logic compiler. Each of these two primary modes, and the bit settings required to enable them, are described below and on the following page.

REGISTERED

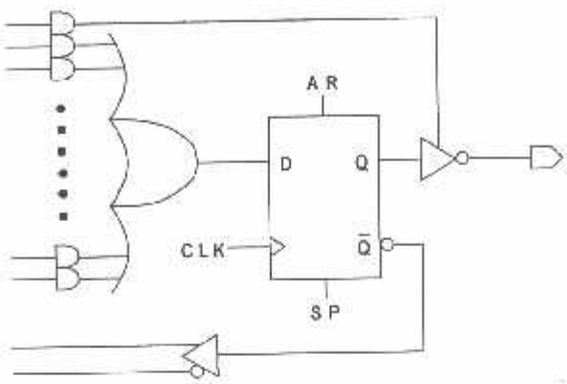
In registered mode the output pin associated with an individual OLMC is driven by the Q output of that OLMC's D-type flip-flop. Logic polarity of the output signal at the pin may be selected by specifying that the output buffer drive either true (active high) or inverted (active low). Output tri-state control is available as an individual product-term for each OLMC, and can therefore be defined by a logic equation. The D flip-flop's /Q output is fed back into the AND array, with both the true and complement of the feedback available as inputs to the AND array.

NOTE: In registered mode, the feedback is from the /Q output of the register, and not from the pin; therefore, a pin defined as registered is an output only, and cannot be used for dynamic I/O, as can the combinatorial pins.

COMBINATORIAL I/O

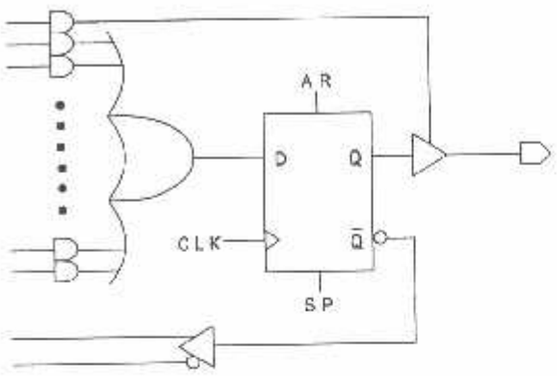
In combinatorial mode the pin associated with an individual OLMC is driven by the output of the sum term gate. Logic polarity of the output signal at the pin may be selected by specifying that the output buffer drive either true (active high) or inverted (active low). Output tri-state control is available as an individual product-term for each output, and may be individually set by the compiler as either "on" (dedicated output), "off" (dedicated input), or "product-term driven" (dynamic I/O). Feedback into the AND array is from the pin side of the output enable buffer. Both polarities (true and inverted) of the pin are fed back into the AND array.

Registered Mode



ACTIVE LOW

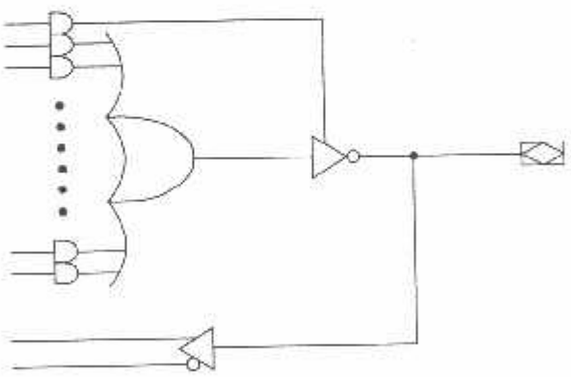
$S_0 = 0$
$S_1 = 0$



ACTIVE HIGH

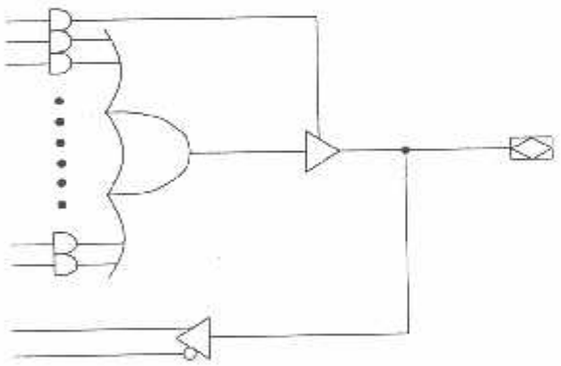
$S_0 = 1$
$S_1 = 0$

Combinatorial Mode



ACTIVE LOW

$S_0 = 0$
$S_1 = 1$

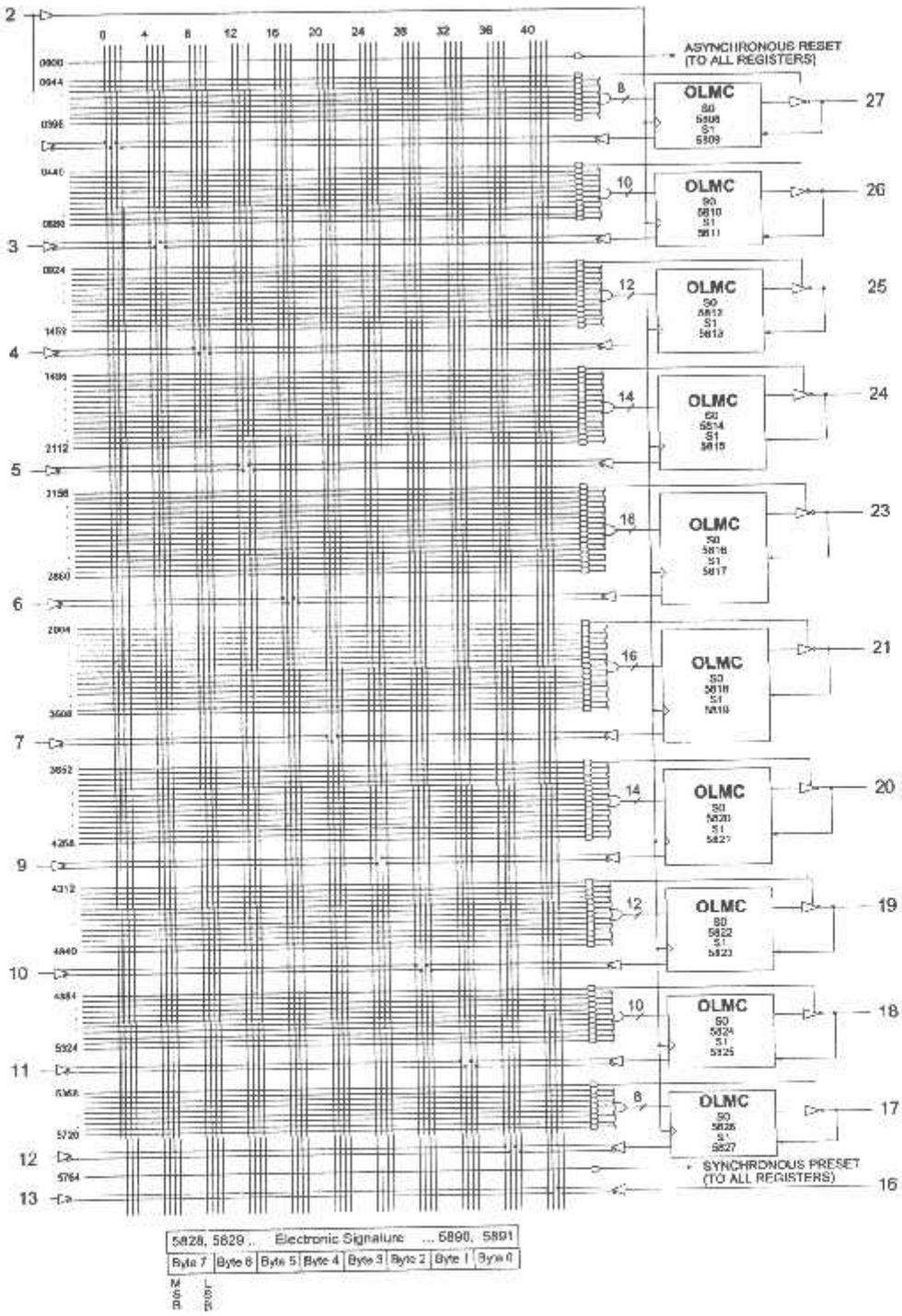


ACTIVE HIGH

$S_0 = 1$
$S_1 = 1$

GAL22LV10 Logic Diagram/JEDEC Fuse Map

PLCC Package Pinout



Absolute Maximum Ratings[1]

Supply voltage V_{CC} ..... -0.5 to +4.6V
Input voltage applied ..... -0.5 to +5.6V
I/O voltage applied ..... -0.5 to +4.6V
Off-state output voltage applied ..... -0.5 to +4.6V
Storage Temperature .....-65 to 150°C
Ambient Temperature with
Power Applied .....-55 to 125°C

1. Stresses above those listed under the "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress only ratings and functional operation of the device at these or at any other conditions above those indicated in the operational sections of this specification is not implied (while programming, follow the programming specifications).

Recommended Operating Conditions

Commercial Devices:
Ambient Temperature (T_A) ..... 0 to 75°C
Supply voltage (V_{CC})
with Respect to Ground ..... +3.0 to +3.6V

DC Electrical Characteristics

Over Recommended Operating Conditions (Unless Otherwise Specified)

SYMBOL	PARAMETER	CONDITION	MIN.	TYP.[3]	MAX.	UNITS
V_{IL}	Input Low Voltage		Vss - 0.3	—	0.8	V
V_{IH}	Input High Voltage		2.0	—	5.25	V
	I/O High Voltage		2.0	—	Vcc+0.5	V
I_{IL}	Input or I/O Low Leakage Current	$0V \le V_{IN} \le V_{IL}$ (MAX.)	—	—	-100	µA
I_{IH}	Input or I/O High Leakage Current	$(Vcc-0.2)V \le V_{IN} \le Vcc$	—	—	10	µA
	Input High Leakage Current	$Vcc \le V_{IN} \le 5.25V$	—	—	10	µA
	I/O High Leakage Current	$Vcc \le V_{IN} \le 4.6V$	—	—	20	mA
V_{OL}	Output Low Voltage	I_{OL} = MAX. Vin = V_{IL} or V_{IH}	—	—	0.4	V
		I_{CL} = 500µA Vin = V_{IL} or V_{IH}	—	—	0.2	V
V_{OH}	Output High Voltage	I_{CH} = MAX. Vin = V_{IL} or V_{IH}	2.4	—	—	V
		I_{OH} = -100µA Vin = V_{IL} or V_{IH}	Vcc-0.2V	—	—	V
I_{OL}	Low Level Output Current		—	—	8	mA
I_{OH}	High Level Output Current		—	—	-8	mA
I_{OS}[2]	Output Short Circuit Current	V_{CC} = 3.3V V_{OUT} = 0.5V T_A = 25°C	-15	—	-80	mA

COMMERCIAL

I_{CC}	Operating Power Supply Current	V_{IL} = 0V V_{IH} = 3.0V Unused Inputs at V_{IL} f_{toggle} = 1MHz Outputs Open	—	90	130	mA

1) The leakage current is due to the internal pull-up resistor on all pins. See **Input Buffer** section for more information.
2) One output at a time for a maximum duration of one second. Vout = 0.5V was selected to avoid test problems caused by tester ground degradation. Characterized but not 100% tested.
3) Typical values are at Vcc = 3.3V and T_A = 25 °C

AC Switching Characteristics

Over Recommended Operating Conditions

PARAMETER	TEST COND[1].	DESCRIPTION	COM -4 MIN.	COM -4 MAX.	COM -5 MIN.	COM -5 MAX.	UNITS
t_{pd}[2]	A	Input or I/O to Combinational Output	1	4	1	5	ns
t_{co}[2]	A	Clock to Output Delay	1	3	1	3.5	ns
t_{cf}[3]	—	Clock to Feedback Delay	—	2.5	—	3	ns
t_{su}	—	Setup Time, Input or Feedback before Clock↑	3	—	3.5	—	ns
t_h	—	Hold Time, Input or Feedback after Clock↑	0	—	0	—	ns
f_{max}[4]	A	Maximum Clock Frequency with External Feedback, 1/(tsu + tco)	167	—	143	—	MHz
	A	Maximum Clock Frequency with Internal Feedback, 1/(tsu + tcf)	182	—	154	—	MHz
	A	Maximum Clock Frequency with No Feedback	250	—	200	—	MHz
t_{wh}[4]	—	Clock Pulse Duration, High	2	—	2.5	—	ns
t_{wl}[4]	—	Clock Pulse Duration, Low	2	—	2.5	—	ns
t_{en}	B	Input or I/O to Output Enabled	1	5	1	6	ns
t_{dis}	C	Input or I/O to Output Disabled	1	5	1	6	ns
t_{ar}	A	Input or I/O to Asynchronous Reset of Register	1	4.5	1	5.5	ns
t_{arw}	—	Asynchronous Reset Pulse Duration	4.5	—	5.5	—	ns
t_{arr}	—	Asynchronous Reset to Clock↑ Recovery Time	3.5	—	4	—	ns
t_{spr}	—	Synchronous Preset to Clock↑ Recovery Time	3.5	—	4	—	ns

1) Refer to **Switching Test Conditions** section.
2) Minimum values for tpd and tco are not 100% tested but established by characterization.
3) Calculated from fmax with internal feedback. Refer to **fmax Descriptions** section.
4) Refer to **fmax Descriptions** section. Characterized but not 100% tested.

Capacitance (T_A = 25°C, f = 1.0 MHz)

SYMBOL	PARAMETER	TYPICAL	UNITS	TEST CONDITIONS
C_I	Input Capacitance	5	pF	V_{CC} = 3.3V, V_I = 0V
C_{VO}	I/O Capacitance	5	pF	V_{CC} = 3.3V, V_{VO} = 0V

Absolute Maximum Ratings[1]

Supply voltage V_{CC} ..... -0.5 to +5.6V
Input voltage applied ..... -0.5 to +5.6V
Off-state output voltage applied ..... -0.5 to +5.6V
Storage Temperature ..... -65 to 150°C
Ambient Temperature with
Power Applied ..... -55 to 125°C

1. Stresses above those listed under the "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress only ratings and functional operation of the device at these or at any other conditions above those indicated in the operational sections of this specification is not implied (while programming, follow the programming specifications).

Recommended Operating Conditions

Commercial Devices:
Ambient Temperature (T_A) ..... 0 to +75°C
Supply voltage (V_{CC})
with Respect to Ground ..... +3.0 to +3.6V

Industrial Devices:
Ambient Temperature (T_A) ..... -40 to +85°C
Supply voltage (V_{CC})
with Respect to Ground ..... +3.0 to +3.6V

DC Electrical Characteristics

Over Recommended Operating Conditions (Unless Otherwise Specified)

SYMBOL	PARAMETER	CONDITION	MIN.	TYP.[2]	MAX.	UNITS
V_{IL}	Input Low Voltage		Vss – 0.5	—	0.8	V
V_{IH}	Input High Voltage		2.0	—	5.25	V
I_{IL}	Input or I/O Low Leakage Current	$0V \le V_{IN} \le V_{IL}$ (MAX.)	—	—	-10	µA
I_{IH}	Input or I/O High Leakage Current	$(V_{CC} - 0.2)V \le V_{IN} \le V_{CC}$	—	—	10	µA
		$V_{CC} \le V_{IN} \le 5.25V$	—	—	30	mA
V_{OL}	Output Low Voltage	I_{OL} = 8mA Vin = V_{IL} or V_{IH}	—	—	0.4	V
		I_{OL} = 16 mA Vin = V_{IL} or V_{IH}	—	—	0.5	V
		I_{OL} = 0.5 mA Vin = V_{IL} or V_{IH}	—	—	0.2	V
V_{OH}	Output High Voltage	I_{OH} = MAX. Vin = V_{IL} or V_{IH}	2.4	—	—	V
		I_{OH} = -0.5 mA Vin = V_{IL} or V_{IH}	Vcc-0.45	—	—	V
		I_{OH} = -100 µA Vin = V_{IL} or V_{IH}	Vcc-0.2	—	—	V
I_{OL}	Low Level Output Current	V_{OL} = 0.4 V	—	—	8	mA
		V_{OL} = 0.5V	—	—	16	mA
I_{OH}	High Level Output Current		—	—	-4	mA
I_{OS}[1]	Output Short Circuit Current	V_{CC} = 3.3V V_{OUT} = 0.5V T_A = 25°C	-15	—	-60	mA

COMMERCIAL

I_{CC}	Operating Power Supply Current	V_{IL} = 0.0V V_{IH} = 3.0V f_{toggle} = 1MHz Outputs Open	—	45	75	mA

INDUSTRIAL

I_{CC}	Operating Power Supply Current	V_{IL} = 0.0V V_{IH} = 3.0V f_{toggle} = 1MHz Outputs Open	-15	—	65	95	mA

1) One output at a time for a maximum duration of one second. Vout = 0.5V was selected to avoid test problems by tester ground degradation. Characterized but not 100% tested.
2) Typical values are at Vcc = 3.3V and T_A = 25 °C

AC Switching Characteristics

Over Recommended Operating Conditions

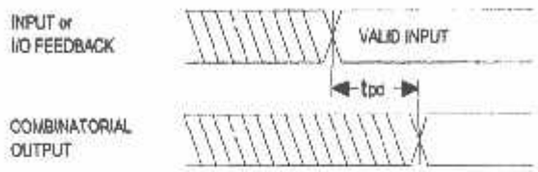
PARAM	TEST COND.[1]	DESCRIPTION	COM -7		COM -10		COM -15		UNITS
			MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
t_{pd}[2]	A	Input or I/O to Combinatorial Output	2	7.5	2	10	2	15	ns
t_{co}[2]	A	Clock to Output Delay	1	5	1	6.5	1	10	ns
t_{cf}[3]	—	Clock to Feedback Delay	—	3	—	5	—	5	ns
t_{su}	—	Setup Time, Input or Fdbk before Clk↑	6	—	7.5	—	10	—	ns
t_h	—	Hold Time, Input or Fdbk after Clk↑	0	—	0	—	0	—	ns
f_{max}[4]	A	Maximum Clock Frequency with External Feedback, 1/(tsu + tco)	91	—	71	—	50	—	MHz
	A	Maximum Clock Frequency with Internal Feedback, 1/(tsu + tcf)	111	—	80	—	66	—	MHz
	A	Maximum Clock Frequency with No Feedback	125	—	111	—	83	—	MHz
t_{wh}	—	Clock Pulse Duration, High	3.5	—	4	—	6	—	ns
t_{wl}	—	Clock Pulse Duration, Low	3.5	—	4	—	6	—	ns
t_{en}	B	Input or I/O to Output Enabled	2	10	2	12	2	15	ns
t_{dis}	C	Input or I/O to Output Disabled	2	10	2	12	2	15	ns
t_{ar}	A	Input or I/O to Asynch. Reset of Reg.	2	11	2	13	2	20	ns
t_{arw}	—	Asynch. Reset Pulse Duration	6	—	8	—	10	—	ns
t_{arr}	—	Asynch. Reset to Clk↑ Recovery Time	6	—	8	—	10	—	ns
t_{spr}	—	Synch. Preset to Clk↑ Recovery Time	6	—	8	—	10	—	ns

1) Refer to **Switching Test Conditions** section.
2) Minimum values for tpd and tco are not 100% tested but established by characterization.
3) Calculated from fmax with internal feedback. Refer to **fmax Description** section.
4) Refer to **fmax Description** section.

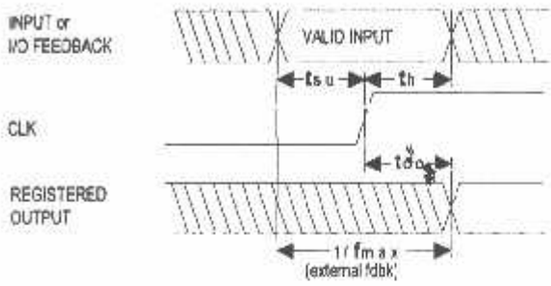
Capacitance (T_A = 25°C, f = 1.0 MHz)

SYMBOL	PARAMETER	TYPICAL	UNITS	TEST CONDITIONS
C_I	Input Capacitance	8	pF	V_{CC} = 3.3V, V_I = 0V
$C_{I/O}$	I/O Capacitance	8	pF	V_{CC} = 3.3V, $V_{I/O}$ = 0V

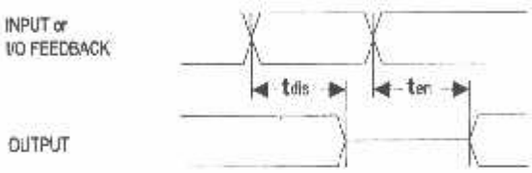
Switching Waveforms



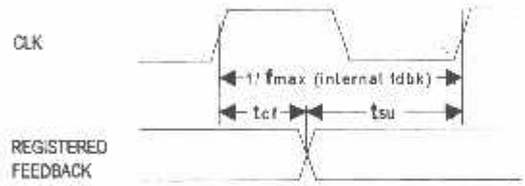
Combinatorial Output



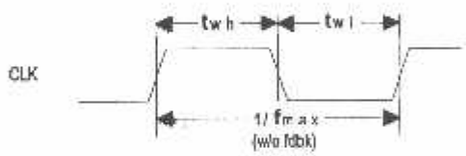
Registered Output



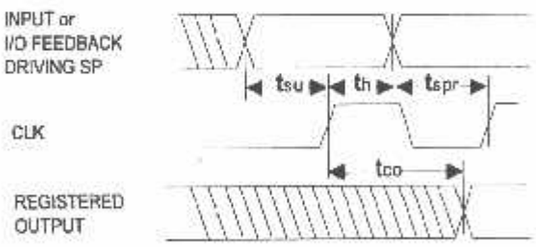
Input or I/O to Output Enable/Disable



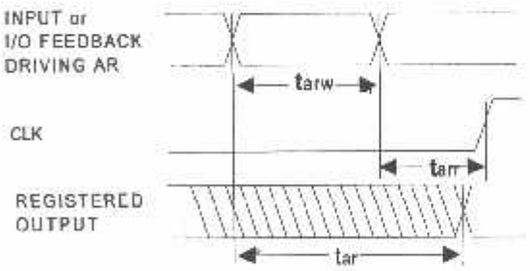
fmax with Feedback



Clock Width

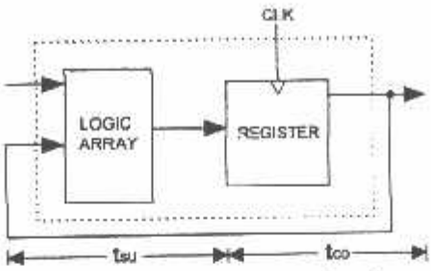


Synchronous Preset



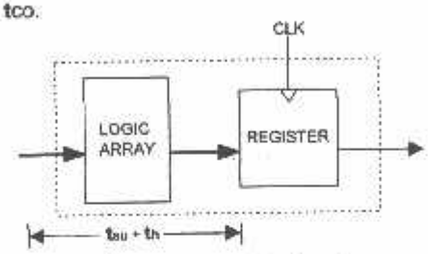
Asynchronous Reset

fmax Descriptions



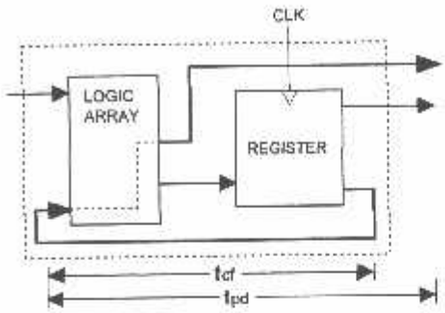
fmax with External Feedback 1/(tsu+tco)

Note: fmax with external feedback is calculated from measured tsu and tco.



fmax with No Feedback

Note: fmax with no feedback may be less than 1/(twh + twl). This is to allow for a clock duty cycle of other than 50%.



fmax with Internal Feedback 1/(tsu+tcf)

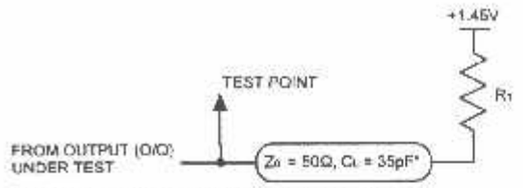
Note: tcf is a calculated value, derived by subtracting tsu from the period of fmax w/internal feedback (tcf = 1/fmax - tsu). The value of tcf is used primarily when calculating the delay from clocking a register to a combinatorial output (through registered feedback), as shown above. For example, the timing from clock to a combinatorial output is equal to tcf + tpd.

GAL22LV10D: Switching Test Conditions

Input Pulse Levels	GND to 3.0V
Input Rise and Fall Times	1.5ns 10% – 90%
Input Timing Reference Levels	1.5V
Output Timing Reference Levels	1.5V
Output Load	See Figure

Output Load Conditions (see figure)

Test Condition		R_1	C_L
A		50Ω	35pF
B	High Z to Active High at 1.9V	50Ω	35pF
	High Z to Active Low at 1.0V	50Ω	35pF
C	Active High to High Z at 1.9V	50Ω	35pF
	Active Low to High Z at 1.0V	50Ω	35pF



*C_L includes test fixture and probe capacitance.

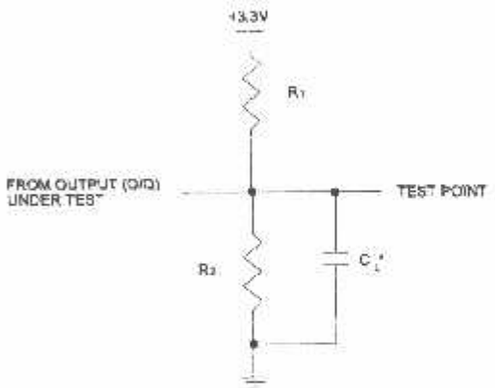
GAL22LV10C: Switching Test Conditions

Input Pulse Levels	GND to 3.0V
Input Rise and Fall Times	2.0ns 10% - 90%
Input Timing Reference Levels	1.5V
Output Timing Reference Levels	1.5V
Output Load	See Figure

3-state levels are measured 0.5V from steady-state active level.

Output Load Conditions (see figure)

Test Condition		R_1	R_2	C_L
A		316Ω	348Ω	35pF
B	Active High	316Ω	348Ω	35pF
	Active Low	316Ω	348Ω	35pF
C	Active High	316Ω	348Ω	5pF
	Active Low	316Ω	348Ω	5pF



*C_L INCLUDES TEST FIXTURE AND PROBE CAPACITANCE

Electronic Signature

An electronic signature (ES) is provided in every GAL22LV10 device. It contains 64 bits of reprogrammable memory that can contain user-defined data. Some uses include user ID codes, revision numbers, or inventory control. The signature data is always available to the user independent of the state of the security cell.

The electronic signature is an additional feature not present in other manufacturers' 22V10 devices. To use the extra feature of the user-programmable electronic signature it is necessary to choose a Lattice Semiconductor 22V10 device type when compiling a set of logic equations. In addition, many device programmers have two separate selections for the device, typically a GAL22LV10 and a GAL22V10-UES (UES = User Electronic Signature) or GAL22V10-ES. This allows users to maintain compatibility with existing 22V10 designs, while still having the option to use the GAL device's extra feature.

The JEDEC map for the GAL22LV10 contains the 64 extra fuses for the electronic signature, for a total of 5892 fuses. However, the GAL 22LV10 device can still be programmed with a standard 22V10 JEDEC map (5828 fuses) with any qualified device programmer.

Security Cell

A security cell is provided in every GAL22LV10 device to prevent unauthorized copying of the array patterns. Once programmed, this cell prevents further read access to the functional bits in the device. This cell can only be erased by reprogramming the device, so the original configuration can never be examined once this cell is programmed. The Electronic Signature is always available to the user, regardless of the state of this control cell.

Latch-Up Protection

GAL22LV10 devices are designed with an on-board charge pump to negatively bias the substrate. The negative bias is of sufficient magnitude to prevent input undershoots from causing the circuitry to latch.

Device Programming

GAL devices are programmed using a Lattice Semiconductor approved Logic Programmer, available from a number of manufacturers (see the the GAL Development/Tools section). Complete programming of the device takes only a few seconds. Erasing of the device is transparent to the user, and is done automatically as part of the programming cycle.

Output Register Preload

When testing state machine designs, all possible states and state transitions must be verified in the design, not just those required in the normal machine operations. This is because certain events may occur during system operation that force the logic into an illegal state (power-up, line voltage glitches, brown-outs, etc.). To test a design for proper treatment of these conditions, a way must be provided to break the feedback paths, and force any desired (i.e., illegal) state into the registers. Then the machine can be sequenced and the outputs tested for correct next state conditions.

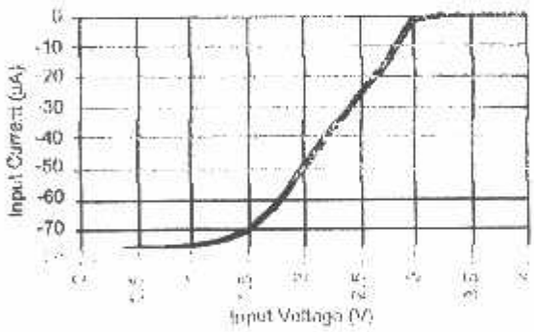
The GAL22LV10 device includes circuitry that allows each registered output to be synchronously set either high or low. Thus, any present state condition can be forced for test sequencing. If necessary, approved GAL programmers capable of executing test vectors perform output register preload automatically.

Input Buffers

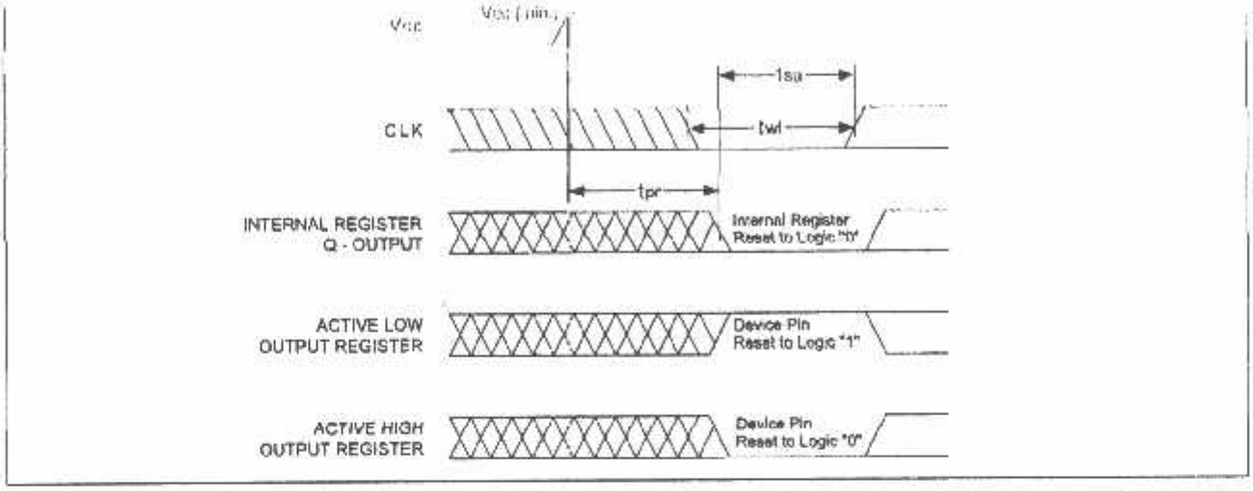
GAL22LV10 devices are designed with TTL level compatible input buffers. These buffers have a defined switching threshold and present a much lighter load to the driving logic than bipolar TTL devices.

The input and I/O pins on the GAL22LV10 also have built-in active pull-ups. As a result, floating inputs will float to a TTL high (logic 1). However, Lattice Semiconductor recommends that all unused inputs and tri-stated I/O pins be connected to an adjacent active input, Vcc, or ground. Doing so will tend to improve noise immunity and reduce Icc for the device. (For additional information, refer to the Designing with Low-Density PLDs application note on the following page.)

Typical Input Pull-up Characteristic



Power-Up Reset

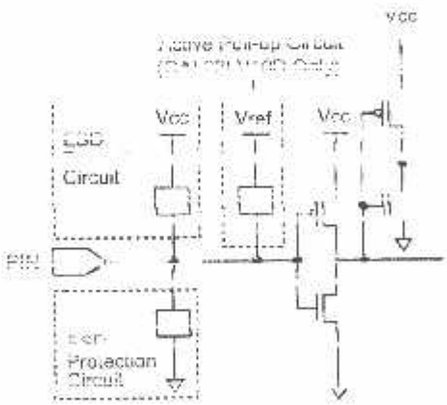


Circuitry within the GAL22V10 provides a reset signal to all registers during power-up. All internal registers will have their Q outputs set low after a specified time (tpr, 1µs MAX). As a result, the state on the registered output pins (if they are enabled) will be either high or low on power-up, depending on the programmed

chronous nature of system power-up, some conditions must be met to provide a valid power-up reset of the GAL22V10. First, the Vcc rise must be monotonic. Second, the clock input must be at

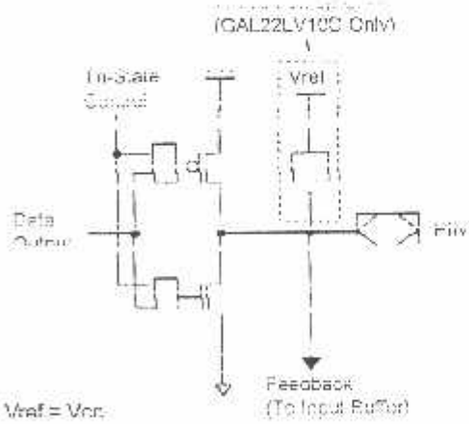
registers will reset within a maximum of

Electrical Characteristics



Typ. Vref = Vcc

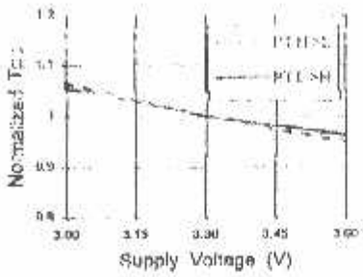
Typical Input

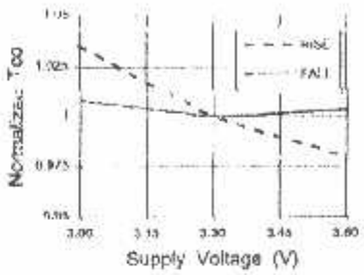


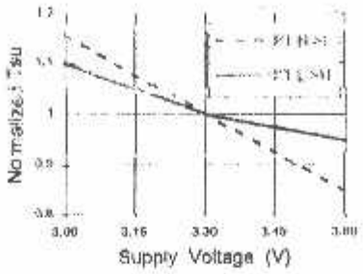
Typ. Vref = Vcc

Typical Output

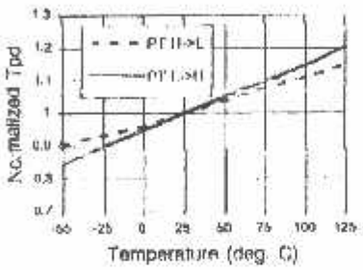
GAL22LV10D: Typical AC and DC Characteristic Diagrams



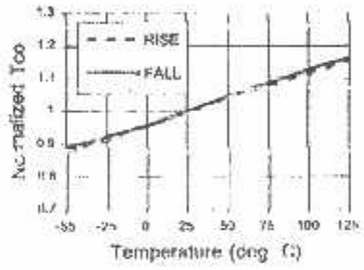




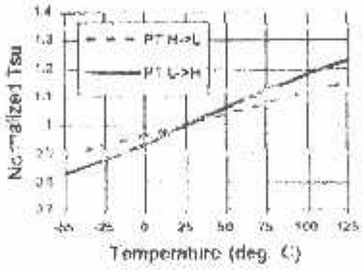
Normalized Tpd vs Temp



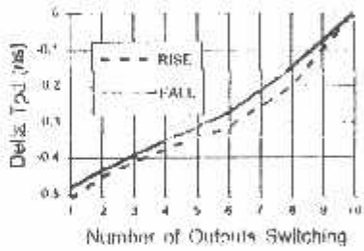
Normalized Tco vs Temp



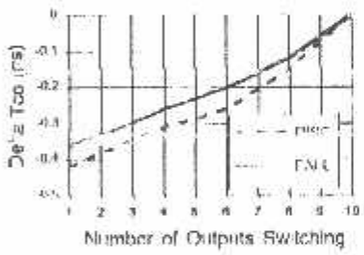
Normalized Tsu vs Temp



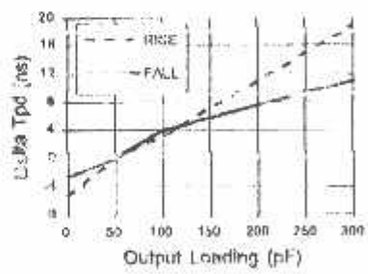
Delta Tpd vs # of Outputs Switching



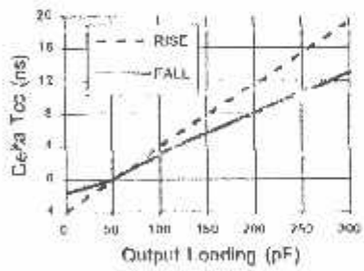
Delta Tco vs # of Outputs Switching



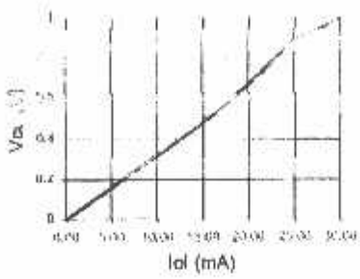
Delta Tpd vs Output Loading

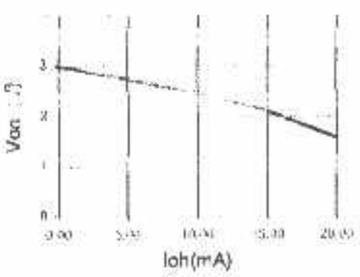


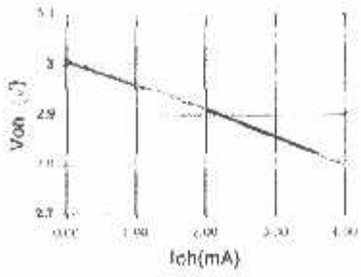
Delta Tco vs Output Loading



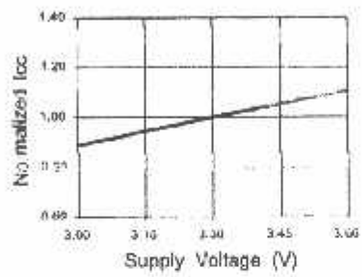
GAL22LV10D: Typical AC and DC Characteristic Graphs



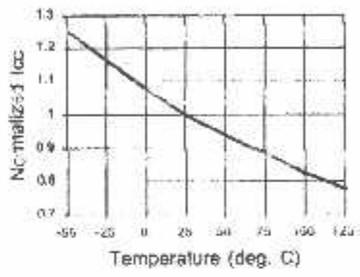




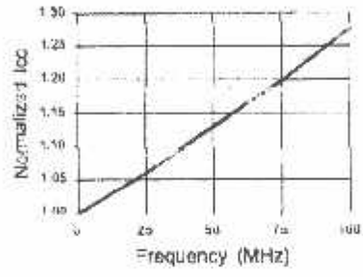
Normalized Icc vs Vcc



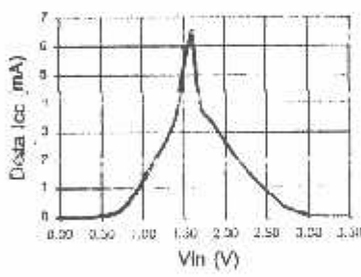
Normalized Icc vs Temp



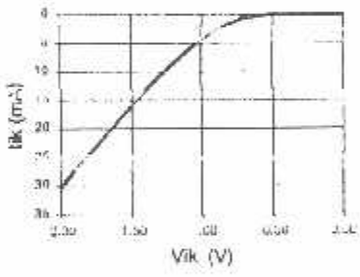
Normalized Icc vs Freq.



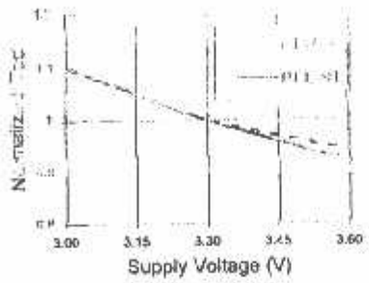
Delta Icc vs Vin (1 input)

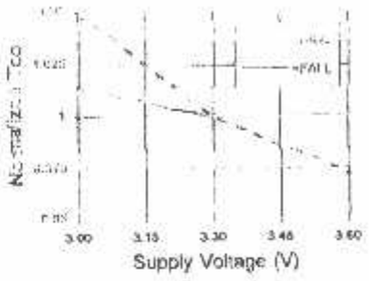


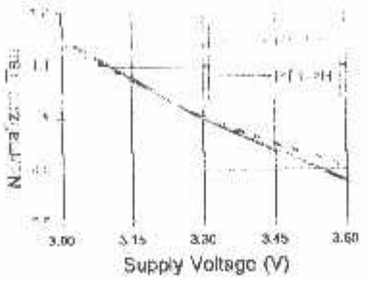
Input Clamp (Vik)

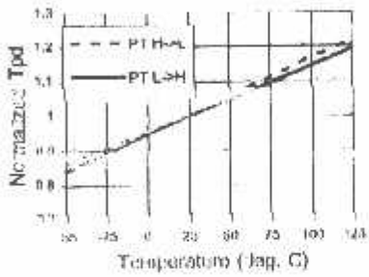


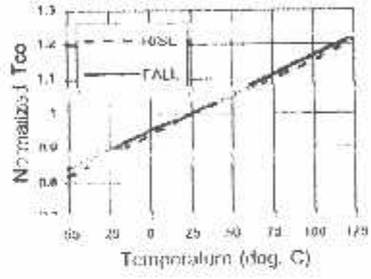
GAL22LV10 Typical AC and DC Characteristic Diagrams

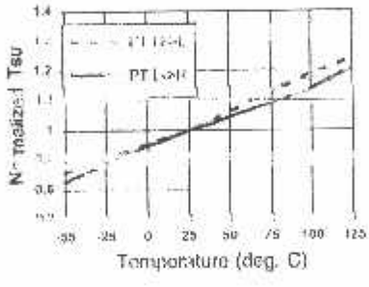


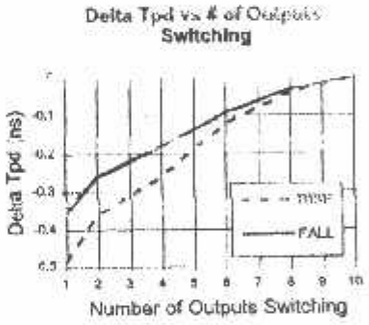


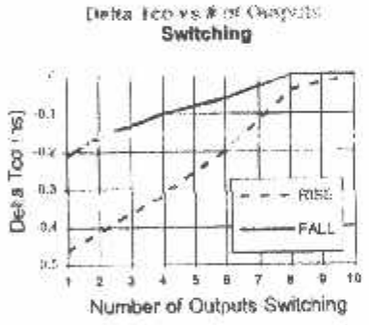


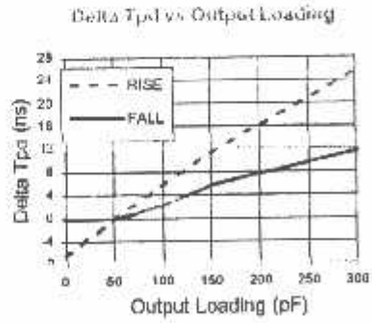


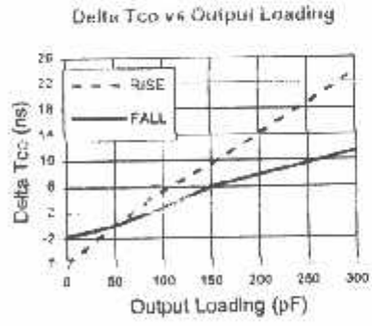




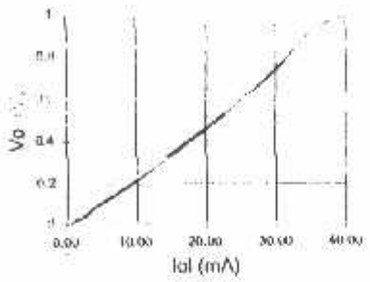


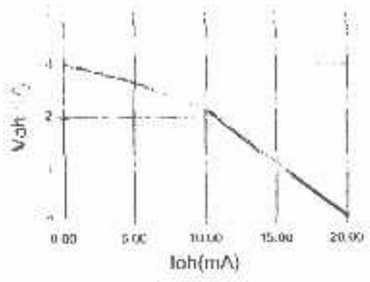


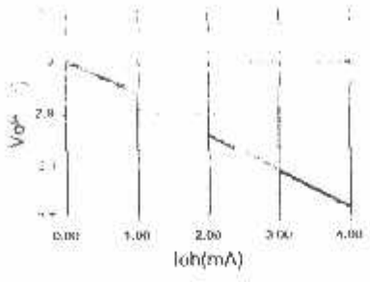


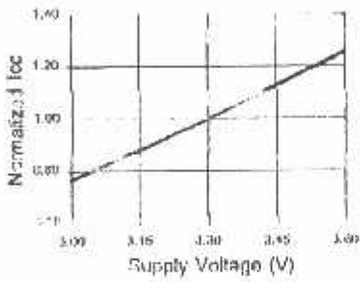


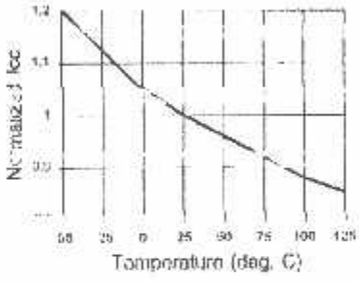
GAL22LV10 Typical AC and DC Characteristic Diagrams

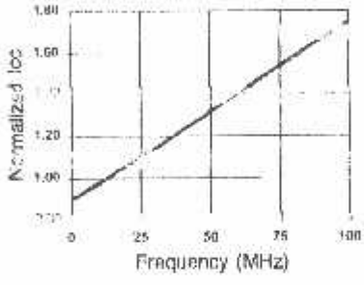


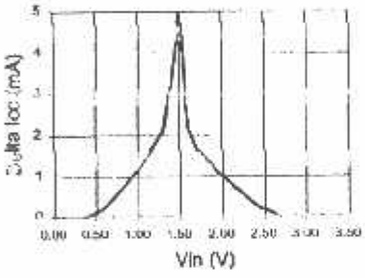


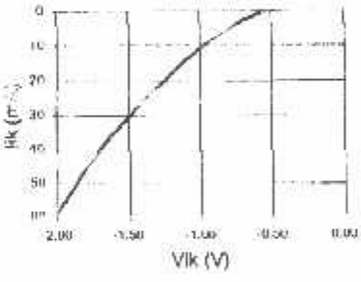












Lattice Semiconductor Corporation

New 5V Tolerant Inputs on 16LV8D

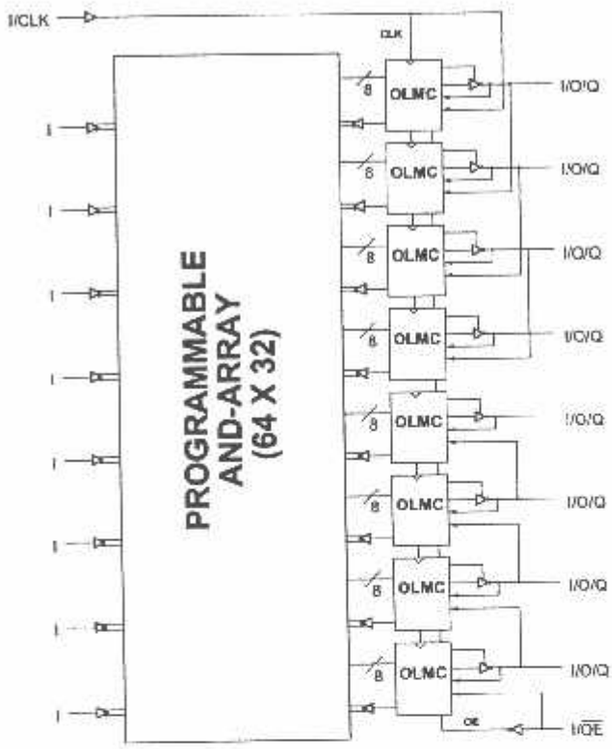
GAL16LV8

Low Voltage E²CMOS PLD Generic Array Logic™

Features

- HIGH PERFORMANCE E²CMOS® TECHNOLOGY
  - 3.5 ns Maximum Propagation Delay
  - Fmax = 250 MHz
  - 2.5 ns Maximum from Clock Input to Data Output
  - UltraMOS® Advanced CMOS Technology
- 3.3V LOW VOLTAGE 16V8 ARCHITECTURE
  - JEDEC-Compatible 3.3V Interface Standard
  - 5V Compatible Inputs
  - I/O Interfaces with Standard 5V TTL Devices (GAL16LV8C)
- ACTIVE PULL-UPS ON ALL PINS (GAL16LV8D Only)
- E² CELL TECHNOLOGY
  - Reconfigurable Logic
  - Reprogrammable Cells
  - 100% Tested/100% Yields
  - High Speed Electrical Erasure (<100ms)
  - 20 Year Data Retention
- EIGHT OUTPUT LOGIC MACROCELLS
  - Maximum Flexibility for Complex Logic Designs
  - Programmable Output Polarity
- PRELOAD AND POWER-ON RESET OF ALL REGISTERS
  - 100% Functional Testability
- APPLICATIONS INCLUDE:
  - Glue Logic for 3.3V Systems
  - DMA Control
  - State Machine Control
  - High Speed Graphics Processing
  - Standard Logic Speed Upgrade
- ELECTRONIC SIGNATURE FOR IDENTIFICATION

Functional Block Diagram



Description

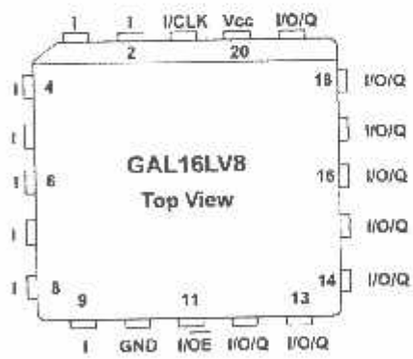
The GAL16LV8D, at 3.5 ns maximum propagation delay time, provides the highest speed performance available in the PLD market. The GAL16LV8C can interface with both 3.3V and 5V signal levels. The GAL16LV8 is manufactured using Lattice Semiconductor's advanced 3.3V E²CMOS process, which combines CMOS with Electrically Erasable (E²) floating gate technology. High speed erase times (<100ms) allow the devices to be reprogrammed quickly and efficiently.

The 3.3V GAL16LV8 uses the same industry standard 16V8 architecture as its 5V counterpart and supports all architectural features such as combinatorial or registered macrocell operations.

Unique test circuitry and reprogrammable cells allow complete AC, DC, and functional testing during manufacture. As a result, Lattice Semiconductor delivers 100% field programmability and functionality of all GAL products. In addition, 100 erase/write cycles and data retention in excess of 20 years are specified.

Pin Configuration

PLCC



LATTICE SEMICONDUCTOR CORP., 5555 Northeast Moore Ct. Hillsboro, Oregon 97124, U.S.A.
Tel. (503) 268-8000; 1-800-LATTICE; FAX (503) 268-8556; http://www.latticesemi.com

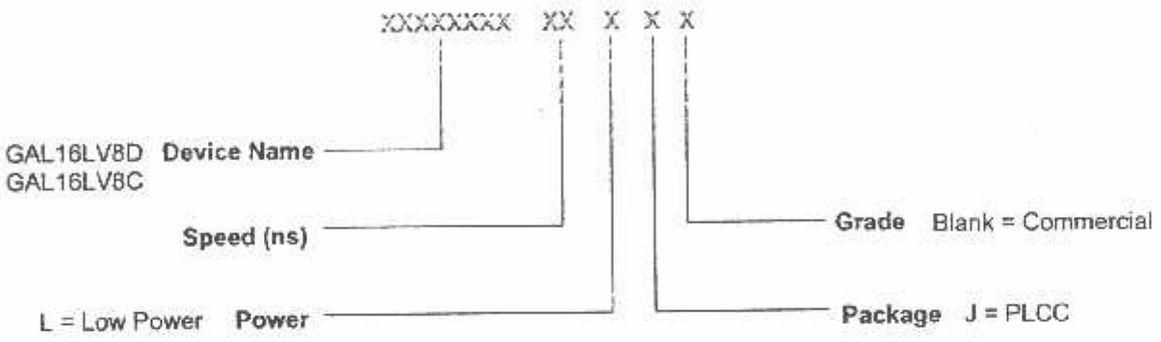
December 1997

GAL16LV8 Ordering Information

Commercial Grade Specifications

Tpd (ns)	Tsu (ns)	Tco (ns)	Icc (mA)	Ordering #	Package
3.5	3	2.5	70	GAL16LV8D-3LJ	20-Lead PLCC
5	4	3	70	GAL16LV8D-5LJ	20 Lead PLCC
7.5	6	5	65	GAL16LV8C-7LJ	20-Lead PLCC
10	7	7	65	GAL16LV8C-10LJ	20-Lead PLCC
15	12	10	65	GAL16LV8C-15LJ	20-Lead PLCC

Part Number Description



Output Logic Macrocell (OLMC)

The following discussion pertains to configuring the output macrocell. It should be noted that actual implementation is accomplished by development software/hardware and is completely transparent to the user.

There are three global OLMC configuration modes possible: **simple, complex,** and **registered.** Details of each of these modes are illustrated in the following pages. Two global bits, SYN and AC0, control the mode configuration for all macrocells. The XOR bit of each macrocell controls the polarity of the output in any of the three modes, while the AC1 bit of each of the macrocells controls the input/output configuration. These two global and 16 individual architecture bits define all possible configurations in a GAL16LV8. The information given on these architecture bits is only to give a better understanding of the device. Compiler software will transparently set these architecture bits from the pin definitions, so the user should not need to directly manipulate these architecture bits.

The following is a list of the PAL architectures that the GAL16LV8 can emulate. It also shows the OLMC mode under which the GAL16LV8 emulates the PAL architecture.

PAL Architectures Emulated by GAL16LV8	GAL16LV8 Global OLMC Mode
16D8	Registered
16R6	Registered
16R4	Registered
16RP8	Registered
16RP6	Registered
16RP4	Registered
16L8	Complex
16H8	Complex
16P8	Complex
10L8	Simple
12L6	Simple
14L4	Simple
16L2	Simple
10H8	Simple
12H6	Simple
14H4	Simple
16H2	Simple
10P8	Simple
12P6	Simple
14P4	Simple
16P2	Simple

Compiler Support for OLMC

Lattice compilers support the three different global OLMC modes as different device types. These device types are listed in the table below. Most compilers have the ability to automatically select the device type, generally based on the register usage and output enable (OE) usage. Register usage on the device forces the software to choose the registered mode. All combinatorial outputs with OE controlled by the product term will force the software to choose the complex mode. The software will choose the simple mode only when all outputs are dedicated combinatorial without OE control. The different device types listed in the table can be used to override the automatic device selection by the software. For further details, refer to the compiler software manuals.

When using compiler software to configure the device, the user must pay special attention to the following restrictions in each mode. In **registered mode** pin 1 and pin 11 are permanently configured as clock and output enable, respectively. These pins cannot be used as dedicated inputs in the registered mode.

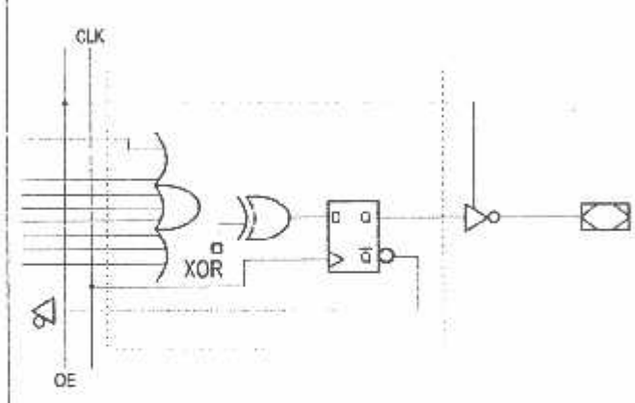
In **complex mode** pin 1 and pin 11 become dedicated inputs and use the feedback paths of pin 19 and pin 12 respectively. Because of this feedback path usage, pin 19 and pin 12 do not have the feedback option in this mode.

In **simple mode** all feedback paths of the output pins are routed via the adjacent pins. In doing so, the two inner most pins (pins 15 and 16) will not have the feedback option as these pins are always configured as dedicated combinatorial output.

	Registered	Complex	Simple	Auto Mode Select
ABEL	P16V8R	P16V8C	P16V8AS	P16v8
CUPL	G16V8MS	G16V8MA	G16V8AS	G16V8
LOG/iC	GAL16V8_R	GAL16V8_C7	GAL16V8_C5	GAL16V8
OrCAD-PLD	"Registered"[1]	"Complex"[1]	"Simple"[1]	GAL16V8A
PLDesigner	P16V8R[2]	P16V8C[2]	P16V8C[2]	P16V8A
TANGO-PLD	G16V8R	G16V8C	G16V8AS[3]	G16V8

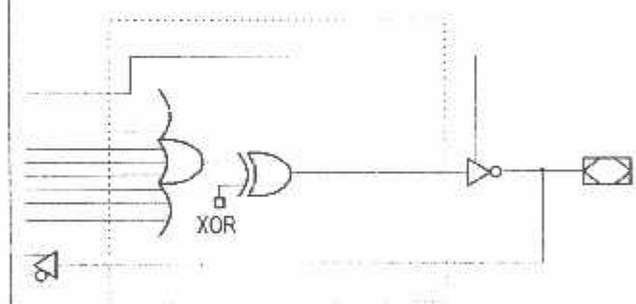
1) Used with **Configuration** keyword.
2) Prior to Version 2.0 support
3) Supported on Version 1.20 or later.

Registered Mode



Registered Configuration for Registered Mode

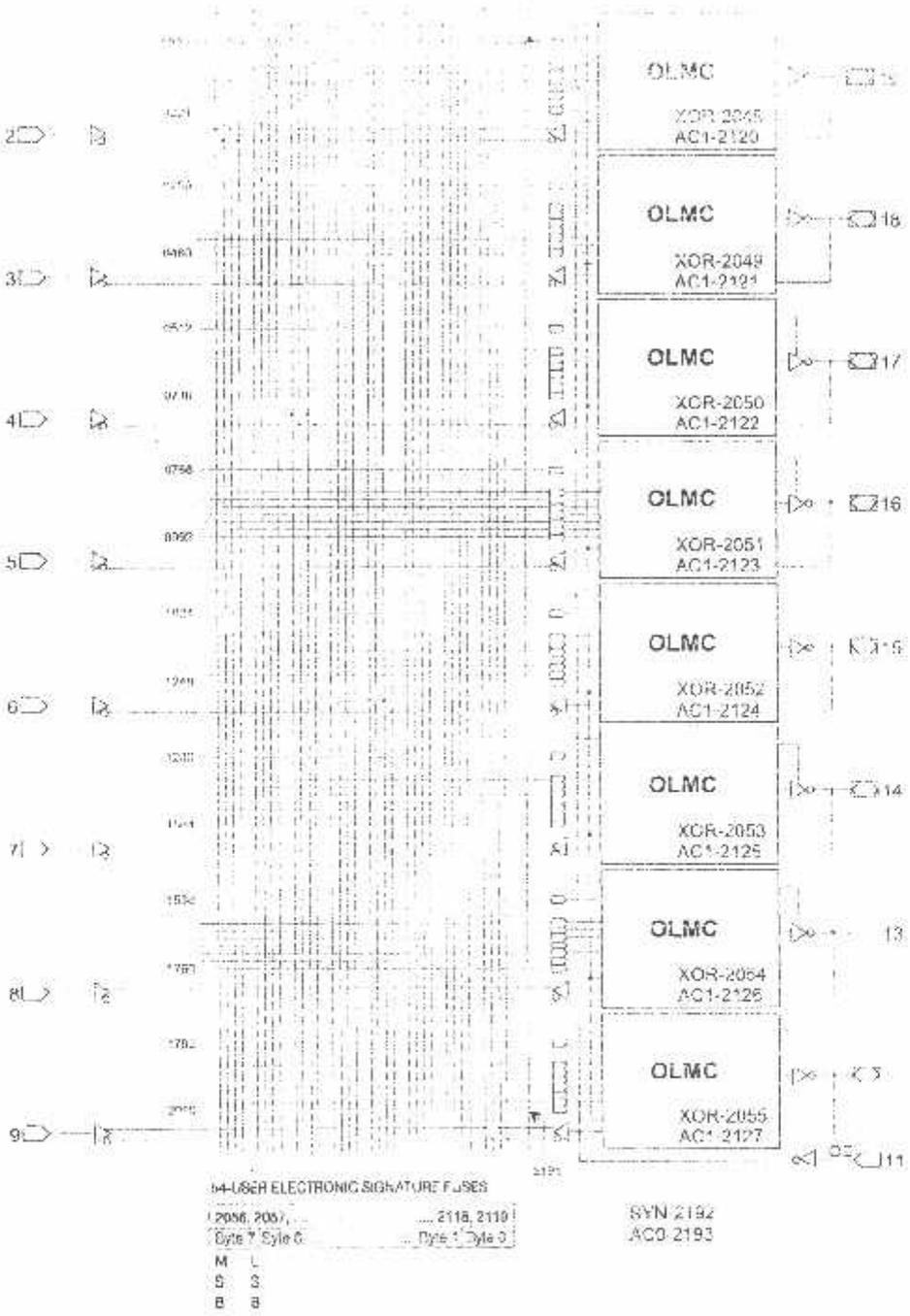
- SYN=0.
- AC0=1.
- XOR=0 defines Active Low Output.
- XOR=1 defines Active High Output.
- AC1=0 defines this output configuration.
- Pin 1 controls common CLK for the registered outputs.
- Pin 11 controls common $\overline{OE}$ for the registered outputs.
- Pin 1 & Pin 11 are permanently configured as CLK & $\overline{OE}$ for registered output configuration.



Combinatorial Configuration for Registered Mode

- SYN=0.
- AC0=1.
- XOR=0 defines Active Low Output.
- XOR=1 defines Active High Output.
- AC1=1 defines this output configuration.
- Pin 1 & Pin 11 are permanently configured as CLK & $\overline{OE}$ for registered output configuration.

Note: The development software configures all of the architecture control bits and checks for proper pin usage automatically.


OLMC
XOR-2048
AC1-2120
OLMC
XOR-2049
AC1-2121
OLMC
XOR-2050
AC1-2122
OLMC
XOR-2051
AC1-2123
OLMC
XOR-2052
AC1-2124
OLMC
XOR-2053
AC1-2125
OLMC
XOR-2054
AC1-2126
OLMC
XOR-2055
AC1-2127
2
3
4
5
6
7
8
9
18
17
16
15
14
13
12
11
64-USER ELECTRONIC SIGNATURE FUSES
(2056, 2057, ... 2118, 2119)
Byte 7 Byte 6 ... Byte 1 Byte 0
M L
S S
B B
SYN 2192
AC0 2193