

**INSTITUT TEKNOLOGI NASIONAL MALANG
FAKULTAS TEKNOLOGI INDUSTRI
JURUSAN TEKNIK ELEKTRO S-1
KONSENTRASI TEKNIK ELEKTRONIKA**



**PERANCANGAN DAN PEMBUATAN ALAT
PENTRANSFER DATA ARGOMETER TAKSI
BERBASIS MIKROKONTROLLER AT89S8252
YANG BISA DI UPLOAD KE KOMPUTER
MELALUI KOMUNIKASI RADIO**

SKRIPSI

Disusun Oleh:

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MARET 2006

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DEPARTMENT OF EDUCATION AND CULTURE
GENERAL DIRECTORATE OF HIGHER EDUCATION
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PERANCANGAN DAN PEMBUATAN ALAT PENTRANSFER DATA ARGOMETER TAKSI BERBASIS MIKROKONTROLLER AT89S8252 YANG BISA DI UPLOAD KE KOMPUTER MELALUI KOMUNIKASI RADIO

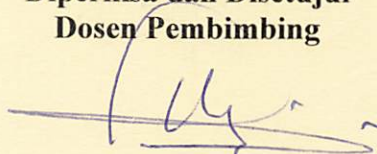
SKRIPSI

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Guna Mencapai Gelar Sarjana Teknik Elektro Strata Satu (S-1)*

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PERSEMBAHAN

بِسْمِ اللَّهِ الرَّحْمَنِ الرَّحِيمِ

"Hai orang-orang yang beriman,
bertakwalah kepada Allah dan hendaklah setiap diri memperhatikan apa yang
telah diperbuatnya untuk hari esok, dan bertakwalah kepada Allah Sesungguhnya
Allah maha mengetahui apa yang kamu kerjakan"

(Hasyr : 18)

"Hendaknya engkau bersyukur berterima kasih kepada-Ku
Dan kepada kedua orang tuamu"

(Luqman :14)

Kupersembahkan skrisiku ini kepada:

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apa yang nanda terima, Doain dadanx semoga dadanx sukses n bisa bahagiain
kalian..... amieeen.

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smoga kita bisa jadi anak-anak yang berbakti kepada orang tua n yang pasti k ita bisa
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ABSTRAKSI

PERANCANGAN DAN PEMBUATAN ALAT PENTRANSFER DATA PADA ARGOMETER TAKSI YANG BERBASIS MIKROKONTROLLER AT89S8252 YANG BISA DI UPLOAD KE KOMPUTER

Sekarang ini bisa dilihat bahwa system penghitungan kilometer pada mobil taksi sudah sedemikian praktisnya yang biasanya diusebut argometer, namun system untuk setoran perhari masih menggunakan atau menggunakan system setor standart harian. Seiring dengan kemajuan teknologi yang semakin canggih saat ini menuntut manusia mencari suatu metode system setor secara komputerisasi yang memudahkan dan meringankan bagi para sopir maupun operator taksi.

Alat ini menggunakan sistem komunikasi tertutup dengan metode half duplex, untuk menjamin keamanannya, selain itu alat ini juga disertai ID yang berbeda untuk setiap taksi. Frekuensi receive dan transmit akan dibuat berbeda. Laporan harian akan dilakukan jika ada permintaan atau requesting dari operator. Laporan harian ini bisa dilakukan dimana saja asalkan masih dalam jangkauan radio komunikasi pada taksi. Data yang diambil dari mikro pada argometer akan ditransferkan ke operator melalui radio komunikasi pada taksi. Data yang diambil dari mikro akan di modulasi oleh modem agar bisa dimodulasikan pada gelombang radio tersebut. Setelah data yang dimodulasi tadi sampai ke operator akan diubah kembali dengan menggunakan demodulator yang kemudian dimasukkan ke PC operator.

Laporan setoran harian tidak terbatas jarak dan waktu karena melalui gelombang radio selain itu transfer data ke kantor operator taksi lebih cepat. Jarak jangkauan tergantung pada jenis dan bentuk antenna dan daya RF masing-masing stasiun radio. Konsumsi daya yang diserap oleh peralatan yang ada di taksi hanya berkisar 8 watt, dan tegangan catu sesuai dengan tegangan catu daya yang ada di mobil taksi.

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Dengan mengucapkan syukur kehadiran ALLAH SWT atas segala rahmat dan hidayatnya .Penulis dapat menyelesaikan laporan skripsi ini dengan judul

PERANCANGAN DAN PEMBUATAN ALAT PENTRANSFER DATA PADA ARGOMETER TAKSI YANG BERBASIS MIKROKONTROLLER AT89S8252 YANG BISA DI UPLOAD KE KOMPUTER

Pada kesempatan ini penyusun ingin menyampaikan dan terima kasih yang sebesar-besarnya kepada pembimbing dan dosen kami

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BAB 1

PENDAHULUAN

1.1 LATAR BELAKANG

Seperti yang telah kita ketahui bersama dalam kehidupan yang serba modern seperti saat ini jalur lalu lintas sangatlah penting dalam kehidupan manusia, ini tidak lepas dari peran angkutan umum yang sangat dibutuhkan dalam kehidupan sehari-hari, salah satu angkutan umum yang paling populer adalah taksi. Karena itu taksi harus terus berkembang sesuai dengan kemajuan teknologi yaitu komputerisasi. Sekarang ini bisa dilihat bahwa system penghitungan kilometer pada mobil taksi sudah sedemikian praktisnya yang biasanya disebut argometer, namun system untuk setoran perhari masih menggunakan atau menggunakan system setor standart harian. Seiring dengan kemajuan teknologi yang semakin canggih saat ini menuntut manusia mencari suatu metode system setor secara komputerisasi yang memudahkan dan meringankan bagi para sopir maupun operator taksi.

Berlatar belakang hal ini maka dirasakan sangat perlu untuk menciptakan suatu perangkat interface yang menghubungkan perangkat mikrokontroler yang dilengkapi memori yang dapat diupload pada computer. Hal ini sangat menguntungkan baik para sopir taksi maupun para operator taksi sehingga memberikan kemudahan ataupun keringanan pada sopir taksi maupun para operator taksi pada metode penyeteran harian, karena para operator taksi tidak perlu lagi menghitung secara manual storan taksi harian karena laporannya

langsung diupload dan diproses di computer. Selain itu para sopir taksi tidak perlu menghasiskan waktu mereka untuk menunggu giliran untuk penghitungan penyeteroran harian.. Karena para sopir taksi bisa melakukan setoran harian dimana saja asal masih dalam jangkauan radio komunikasi yang dimiliki oleh taksi tersebut. Selain itu alat ini juga telah dilengkapi oleh system komunikasi dengan computer yang berupa radio komunikasi yang tidak lagi memerlukan kabel sehingga alat ini sangatlah praktis dan daya guna.

1.2 PERMASALAHAN

Permasalahan yang akan diangkat dalam laporan ini adalah sebagai berikut:

- Bagaimana mengirimkan data pada argometer ke computer operator taksi melalui radio komunikasi pada taksi. .
- Bagaimana merencanakan dan membuat perangkat lunak untuk penulisan informasi, penyimpanan informasi, dan pengiriman informasi ke bagian penerima (PC) melalui sistem komunikasi radio pada taksi.

1.3 BATASAN MASALAH

Agar perencanaan dan perancangan alat ini dapat dilakukan secara sistematis dan terarah, maka ruang lingkup pembahasan dan perancangan alat dibatasi sebagai berikut:

- Tidak membahas secara mendetail aspek teknis (elektronik) dari radio sebagai system komunikasi antara pc dan mikrokontroller yang

digunakan, melainkan hanya pada antarmuka untuk komunikasi data kedua perangkat tersebut dari/ke sistem mikrokontroler.

- o Tidak membahas catu daya dan catu daya dianggap konstan
- o Tidak membahas mekanik roda dan perhitungan harga pada taksi melainkan hanya system komunikasi antara mikrokontroller dengan PC

1.4 TUJUAN

Untuk mempelajari, merencanakan dan membuat suatu peralatan interfacing mikrokontroller dengan computer. Diperlukan inisialisasi parameter yang digunakan agar komunikasi data antara computer dengan mikrokontroller melalui radio komunikasi menjadi sinkron.

1.5 KONTRIBUSI PERANCANGAN

Melalui perancangan dan pembuatan alat ini diharapkan dapat memberikan manfaat dalam pengembangan dan pengaplikasian teknologi radio paket dan mikrokontroller dalam kehidupan sehari-hari.

1.6 SISTEMATIKA PENULISAN

Sistematika penulisan dan gambaran tentang hal-hal yang dibahas dalam setiap bab adalah sebagai berikut:

BAB I PENDAHULUAN

Memuat latar belakang, tujuan, permasalahan, ruang lingkup dan sistematika penulisan.

BAB II DASAR TEORI

Memuat tentang landasan-landasan teori yang diperlukan dalam realisasi pembuatan alat ini.

BAB III PERANCANGAN DAN PEMBUATAN ALAT

Menerangkan tentang perancangan dan pembuatan seluruh sistem peralatan, baik perangkat keras maupun perangkat lunak.

BAB IV ANALISIS DAN PENGUJIAN ALAT

Menerangkan tentang hasil pembuatan dan pengujian yang dilakukan terhadap alat yang telah dibuat serta menampilkan hasil-hasil pengujian.

BAB V PENUTUP

Memuat kesimpulan dan saran dari tema yang di analisa dalam skripsi ini

BAB II

LANDASAN TEORI

2.1. Pendahuluan

Dalam perancangan dan pembuatan alat pentransfer data pada argometer taksi ini di butuhkan beberapa teori yang mejadi landasan, yaitu teori yang berhubungan dengan komponen-komponen yang digunakan dalam perencanaan dan pembuatan sistem ini

2.2. Radio Komunikasi

Pada perancangan dan pembuatan alat pentransfer data pada argometer taksi menggunakan gelombang radio sebagai alat atau media untuk mentransmisikan data dari argometer ke computer operator. Karenanya kami menggunakan HT jenis ICOM 2N sebagai media komunikasinya.

2.3. Mikrokontroler AT89S8252

Mikrokontroler AT89S8252 merupakan versi CHMOS dari AT89S8252 yaitu versi NMOS. NMOS merupakan kependekan dari *N-Channel Metal Oxide Silicon* dan kompatibel dengan MCS-51 mikrokomputer yang merupakan produksi dari ATMEL. Seri AT89S8252 adalah mikrokontroller yang membutuhkan daya rendah, memiliki kemampuan yang tinggi, dan merupakan mikrokomputer 8 bit yang dilengkapi 8K *byte Flash PEROM (Programmable and Erasable Read Only Memory)* yaitu ROM yang dapat ditulis ulang atau

dihapus menggunakan sebuah perangkat programmer. Serta terdapat EEPROM *internal* sebesar 2K Byte.

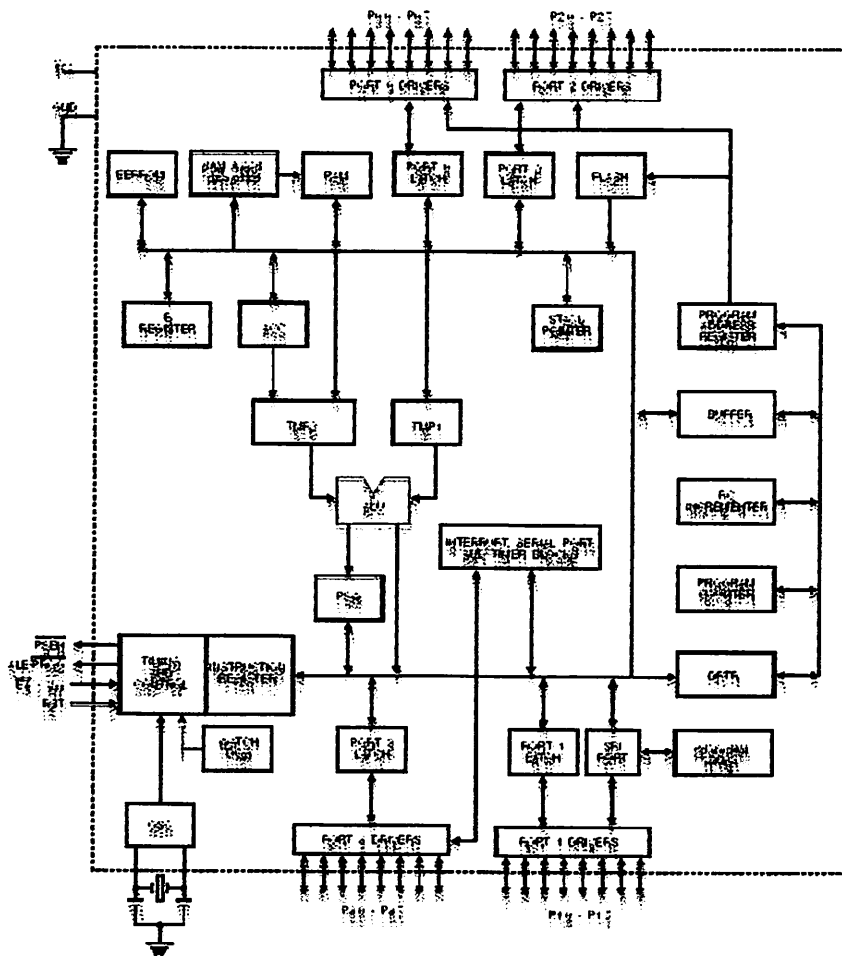
Flash PEROM dalam AT89S8252 menggunakan *Atmel's High-Density Non Volatile Technology* yang mempunyai kemampuan untuk ditulis ulang hingga 1000 kali dan berisikan perintah *standard* MCS-51. Selain itu juga dilengkapi RAM *internal* sebesar 256 byte. Dalam sistem Mikrokontroler terdapat dua hal yang mendasar, yaitu: perangkat keras dan perangkat lunak yang keduanya saling terkait dan mendukung. Mikrokontroler ini digunakan untuk beberapa keperluan mulai dari komersial, industri, otomotif, dan militer.

2.3.1. Fitur Mikrokontroler AT89S8252

Fitur Mikrokontroler AT89S8252 adalah sebagai berikut :

- Kompatibel dengan mikrokontroler MCS-51
- 8K byte In-System Programmable Downloadable Flash Memori
 - SPI Serial Interface for Program Downloading
 - Endurance: 1,000 Write/Erase Cycles
- 2K byte EEPROM
 - Edurance: 100,000 Write/Erase Cycles
- 3 Level program memori lock
- Memory 256 x 8 bit *Internal* RAM
- 32 Port I/O Lines yang dapat dipakai semua
- 3 buah Timer/Counter 16 bit
- Nine Interrupt Source

- Programmable UART (serial port)
- SPI Serial Interface
- Programmable Watchdog Timer
- Dual Data Pointer
- Frekuensi kerja 0 sampai 24 MHz
- Tegangan Operasi 4 Volt sampai 6 Volt
- *Power-Off Flag.*



Gambar 2-1. Blok Diagram AT89S8252

Sumber : Datasheet AT89S8252

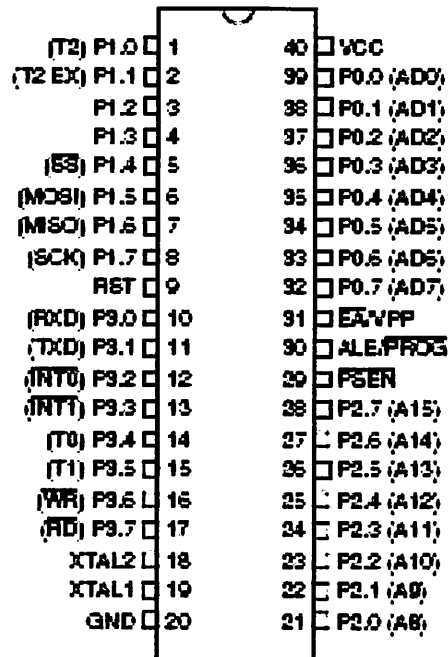
2.3.2. Arsitektur AT89S8252

Arsitektur Mikrokontroler AT89S8252 adalah sebagai berikut:

- 8 bit CPU (*Central Processing Unit*) dengan register A dan B.
- 16 bit *Program Counter* (PC) dengan *Data Pointer* (DPTR).
- 8 bit program status word (PSW).
- 8 bit stack pointer (SP).
- Internal EPROM dan ROM dari 0 sampai 4 Kb.
- 256 byte *Internal RAM*
 - ⇒ 4 register bank masing-masing 8 register.
 - ⇒ 16 byte yang dapat dialamatkan pada *bit level*.
 - ⇒ 208 byte *memory general purpose memory data*.
- 32 pin *input/output* tersusun sebagai 4 port masing-masing 8 bit (P0 – P3).
- 3 buah Timer (T0 & T1) dengan masing-masing 16-bit timer/counter.
- Data serial *receiver/transmitter full duplex* yaitu SBUF.
- *Control register* antara lain TCON, TMOD, SCON, PCON, IP dan ME.
- 2 eksternal dan 3 internal sumber *interrupt*.
- Rangkaian *oscillator* dan *clock*.

2.3.3. Konfigurasi Kaki-kaki MCU AT89S8252

Berikut ini adalah bentuk fisik dari AT89S8252:



Gambar 2-2. Bentuk fisik AT89S8252

Sumber : Datasheet AT89S8252

Fungsi-fungsi dari tiap-tiap pin sebagai berikut :

➤ **Pin 40: Vcc**

Dihubungkan dengan sumber tegangan + 5 V.

➤ **Pin 20: GND**

Dihubungkan dengan Ground rangkaian atau media pentanahan.

➤ **Pin 32-39 : Port 0 (P0.0 – P0.7)**

Port 0 merupakan port I/O 8 bit dua arah. Port ini digunakan sebagai multipleks bus alamat rendah dan bus data selama pengaksesan ke memori luar.

➤ **Pin 1-8 : Port 1 (P1.0 – P1.7)**

Port 1 dapat difungsikan sebagai masukan atau keluaran dan bekerja baik untuk operasi bit maupun *byte*, tergantung dari pengaturan program yang dibuat.

Tabel 2-1. Fungsi Alternatif Port 1

Port Pin	Fungsi
P1.0	T2 (masukan eksternal untuk Timer/Counter 2)
P1.1	T2EX (Timer/Counter 2 capture/reload trigger dan kontrol arah)
P1.2	-
P1.3	-
P1.4	SS (slave port select input)
P1.5	MOSI (master data output, slave data input untuk chanel SPI)
P1.6	MISO (maser data input, slave data output untuk chanel SPI)
P1.7	SCK (master clock output, slave clock input untuk chanel SPI)

➤ **Pin 21-28 : Port 2 (P2.0 – P2.7)**

Port 2 merupakan port input-output dengan internal pull-up. Port ini dapat digunakan sebagai alamat bus baik *byte* tinggi selama adanya akses ke memori program atau memori data luar. Mengeluarkan address tinggi selama pengambilan (fetching) program memory external. Selama pengaksesan ke external data memory, port 2 mengeluarkan isi P2 SFR. Menerima address dan beberapa control selama pemrograman dan verifikasi.

➤ **Port 3 (P3.0 – P3.7)**

Port 3 mempunyai fungsi sebagai I/O juga mempunyai fungsi khusus sebagai berikut :

- RD (P3.7), sinyal pembacaan memori data luar.
- WR (P3.6), sinyal penulisan memori data luar.
- T1 (P3.5), masukan dari pewaktu/pencacah 1.
- T0 (P3.4), masukan dari pewaktu/pencacah 0.
- INT1 (P3.3), masukan interrupt 1.
- INT0 (P3.2), masukan interrupt 0.
- TXD (P3.1), keluaran pengiriman data untuk serial *port* (*asynchronous*) atau sebagai keluaran *clock* (*sybchronous*).
- RXD (P3.0), masukan data serial atau sebagai keluaran data.

➤ **Pin 9 : RST/VPD.**

Merupakan pin input yang aktif jika pin aktif tinggi selama dua siklus mesin maka ketika osilator bekerja akan mereset peralatan.

➤ **Pin 30 : ALE (*Address Latch Enable*).**

Pin ALE (aktif tinggi) mengeluarkan pulsa output untuk menyangga (*latch*) satu byte alamat rendah selama mengakses ke memori eksternal. ALE dapat mengendalikan 8 beban TTL. Pin ini juga merupakan input pulsa program yang aktif rendah selama pemrograman EPROM. Pada operasi normal, ALE dikeluarkan pada suatu kecepatan yang konstan yaitu 1/6 dari frekuensi osilator dan dapat digunakan untuk *timing* eksternal atau untuk tujuan membuat *clock*.

➤ **Pin 29 : PSEN (*Program Strobe Enable*).**

Pin ini aktif rendah yang merupakan *strobe* pembacaan ke program memori eksternal.

➤ **Pin 18-19 : XTAL1&XTAL2.**

Pin XTAL1 merupakan pin input ke penguat osilator pembalik dan XTAL2 merupakan pin output dari penguat osilator pembalik.

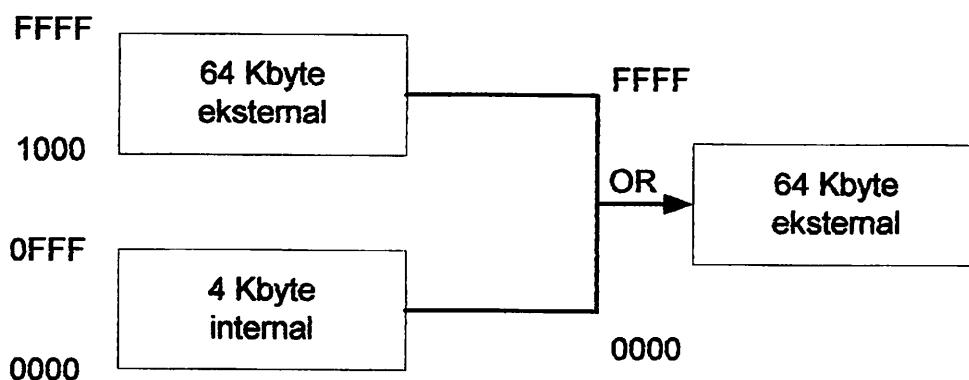
➤ **Pin 30 : EA,VPP (*External Access/Programming Supply Voltage*).**

Pin EA di Vcc agar 89S8252 dapat mengakses kode mesin dari program memori.

2.3.4. Organisasi Memori MCU AT89S8252

Mikrokontroler AT89S8252 termasuk keluarga MCS-51 yang memiliki memori program dan memori data yang terpisah. Pemisahan ini dilakukan secara logika sehingga CPU dapat mengakses sampai 64 *Kbyte* memori program dan 64 *Kbyte* memori data. Lebar memori data internal adalah 8 bit dan 16 bit (register PC dan register DPTR).

2.3.4.1. Memori Program



Gambar 2-3. Memori program MCS-51

Sumber : Advanced Microdevices, 1988, 32.

Memori program menggunakan alamat sepanjang 64 *Kbyte* dengan 4 *Kypte* (alamat \$0000 sampai dengan \$0FFF) yang merupakan memori internal sehingga 60 *Kbyte* merupakan memori eksternal. Dapat menggunakan 64 *Kbyte* memori eksternal sebagaimana yang ditunjukkan pada gambar memori data.

Memori program merupakan tempat penyimpanan data permanen. Memori program lebih dikenal dengan nama *Read Only Memory* (ROM). Data dalam ROM tidak akan terhapus meskipun catu daya dimatikan atau dikenal sebagai sifat *non-volatile*. Karena sifatnya yang demikian ROM dapat digunakan untuk menyimpan program.

Ada beberapa tipe ROM, antara lain :

- ROM (*Read Only Memory*)

Merupakan memori yang sudah diprogram oleh pabrik (ROM murni).

- PROM (*Programmable Read Only Memory*)

Merupakan memori yang dapat diprogram oleh pemakai tetapi tidak dapat diprogram ulang.

- EPROM (*Erasable Programmable Read Only Memory*)

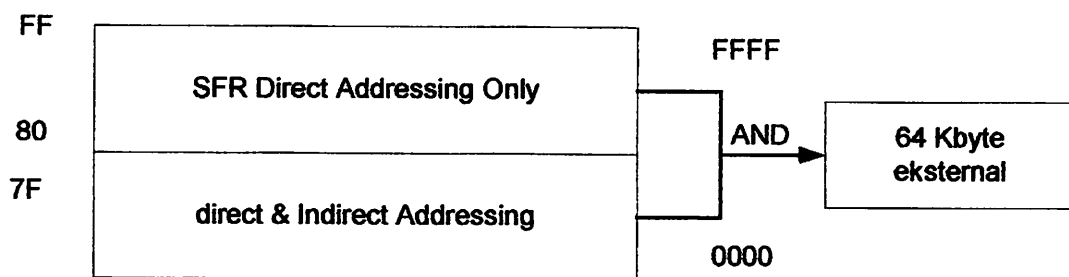
Merupakan PROM yang dapat diulang. ROM ini juga terdapat pada mikrokontroler 8751, hal ini ditandai dengan adanya jendela kaca pada konstruksi IC 8751 yang digunakan untuk menghapus atau memperbaiki program yang sudah ada.

- EEPROM (*Electrical Erasable Programmable Read Only Memory*)

Pada prinsipnya hampir sama dengan EPROM, tetapi perbedaannya terletak pada pengosongan atau penghapusan program. Untuk EPROM

dapat dihapus dengan menggunakan sinar *ultra violet*, sedangkan pada EEPROM pengisian program dapat dilakukan langsung atau menumpuk program lama dengan program yang baru. EEPROM lebih fleksibel dibandingkan EPROM.

2.3.4.2. Memori Data



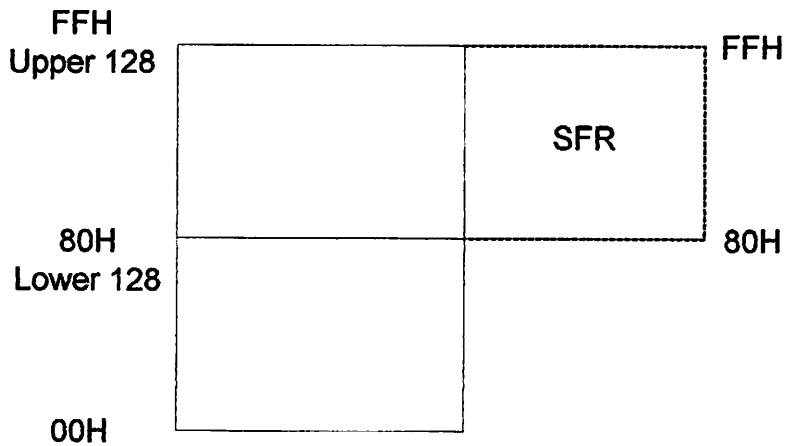
Gambar 2-4. Memori data MCS-51

Sumber : Advanced Microdevices, 1988,33.

Memori data merupakan tempat penyimpanan data yang bersifat sementara atau *volatile*. Dengan kata lain data akan hilang bila tidak dicatu. Memori data lebih dikenal dengan nama RAM (*Random Access Memory*), yaitu dapat dilakukan pembacaan dan penulisan data alamat yang tersedia.

Memori MCS-51 mempunyai 128 bytes - 256 byte RAM internal ditambah sejumlah register fungsi khusus atau *Special Function Register (SFR)*. (*Advanced Mikrodevides*, 1988.1.6). Selain mempunyai memori internal, MCU AT89S8252 mempunyai memori eksternal yang memiliki pengalamatan sampai 64 Kbytes.

Pada keluarga mikrokontroler MCS-51, ruang memori data eksternal terbagi menjadi 3 blok yang disebut *lower 128*, *upper 128* dan ruang SFR, sebagaimana ditunjukkan pada gambar di bawah ini.



Gambar 2-5. Memori Data Eksternal

Sumber : Advanced Microdevices, 1988,16

Pada *lower 128* lokasi memori dibagi menjadi 3 bagian :

1. Register bank 0 – 3

Lokasi bank register dimulai dari alamat 00h – 1h yang terdiri dari 32 *bytes*. Register bank ini terdiri dari 4 buah register 8 bit yang dapat dipilih melalui pengaturan *program status word* register.

2. Bit Addressing

Terdiri dari 16 *bytes* yang dimulai dari 20h – 2fh. Masing-masing dari 128 bit lokasi ini dapat dialamati secara langsung yaitu dari \$00h sampai \$7fh.

3. *Scratch Pad Area*

Lokasi dari alamat \$30h sampai \$7fh atau sebanyak 80 *bytes* yang dapat digunakan sebagai alamat bagi RAM.

Pada 128 *bytes* atas (*upper 128*) ditempati oleh register yang mempunyai fungsi khusus yang disebut dengan *Special Function Register* (SFR). Ruang dari register fungsi khusus ini adalah dari 80h sampai FFh. Berikut ini adalah contoh isi vector alamat pada *Special Function Register*.

- Akumulator (Acc) atau register A dan register B.

Kedua register tersebut digunakan untuk operasi perkalian dan pembagian.

- *Program Status Word*

Register ini meliputi bit-bit : CY (*Carry*), AC (*Auxillary Carry*), FO sebagai flag, RS0 dan RS1 untuk pemilih register bank, OV (*Over Flow*), dan *parity flag*.

- *Stack Pointer* (SP)

SP merupakan register yang digunakan untuk penunjuk alamat. Register ini berguna apabila digunakan suatu *routine* pada program utama.

- *Data Pointer High* (DPH) dan *Data Pointer Lower* (DPL)

DPTR adalah register yang digunakan untuk pengalamatan tidak langsung. Register ini digunakan untuk mengakses memori program baik internal maupun eksternal. DPTR dikontrol oleh 2 buah register 8 bit yaitu DPH dan DPL.

- *Port 0, Port 1, Port 2, Port 3*

Pada keluarga 8051 masing-masing *port* dapat dialamati langsung baik secara *byte* atau bit. Masing-masing *port* merupakan *port bi-directional (input/output)* :

1. *Port 0* digunakan sebagai pengalamatan memori dari luar.
2. *Port 1* digunakan sebagai I/O dari mikrokontroler.
3. *Port 2* digunakan sebagai pengalamatan memori dari luar.
4. *Port 3* berisi sinyal kontrol seperti *interrupt serial*, WR, dan RD.

- *Register Prioritas Interrupt (Interrupt Priority Register /IP).*

Merupakan register yang berisi bit-bit untuk mengaktifkan prioritas dari suatu *interrupt* yang ada pada mikrokontroler pada taraf yang diinginkan.

- *Interrupt Enable Register*

Merupakan register yang berisi bit-bit untuk menghidupkan atau mematikan sumber-sumber *interrupt*.

- *Timer/Counter Control Register*

TCON merupakan register yang berisi bit-bit memulai atau menghentikan pencacah atau pewaktu.

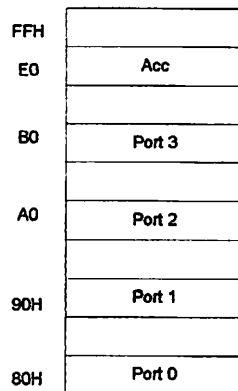
- *Serial Control Buffer*

Register ini digunakan untuk menampung data masukan (SBUF *in*) atau keluaran (SBUF *out*) dari *serial port*.

Tabel 2-2 Pembagian alamat pada SFR

SYMBOL	NAME	ADDRESS
ACC	ACCUMULATOR	0E0H
B	B REGISTER	0F0H
PSW	PROGRAM STATUS WORD	0D0H
SP	STACK POINTER	81H
DPTR	DATA POINTER 2 BYTE	
DPL	LOW BYTE	82H
DPH	HIGH BYTE	83H
P0	PORT 0	80H
P1	PORT 1	90H
P2	PORT 2	0A0H
P3	PORT 3	080H
IP	INTERRUPT PERIORITY CONTROL	088H
IE	INTERRUPT ENABLE CONTROL	0ABH
TMOD	TIMER/COUNTER MODE CONTROL	89H
TCON	TIMER/COUNTER CONTROL	88H
+TCON	TIMER/COUNTER 2 CONTROL	0CBH
TH0	TIMER/COUNTER 0 HIGH CONTROL	8CH
TL0	TIMER/COUNTER 0 LOW CONTROL	8DH
TH1	TIMER/COUNTER 1 HIGH CONTROL	8DH
TL1	TIMER/COUNTER 1 LOW CONTROL	8CH
TH2	TIMER/COUNTER 2 HIGH CONTROL	0CDH
TL2	TIMER/COUNTER 2 LOW CONTROL	0CCH
RCAP2H	T/C 2 CAPTURE REG. HIGH BYTE	0CBH
+RCAP2L	T/C 2 CAPTURE REG. LOW BYTE	0CAH
SCON	SERIAL CONTROL	98H
SBUF	SERIAL DATA BUFFER	99H
PCON	POWER CONTROL	87H

Adapun diagram blok dari SFR adalah sebagai berikut :



Gambar 2.6. Ruang *Special Function Register*

Sumber : Eksperimen dengan Mikrokontroler, 1999,13

2.3.4.3. SFR Tambahan Pada AT89S8252

Selain memiliki SFR (*Special Function Register*) seperti halnya pada MCS-51, mikrokontroler AT89S8252 memiliki tambahan SFR. Hal ini tak lain karena adanya fitur tambahan pada mikrokontroler AT89S8252.

SFR tambahan ini meliputi : T2CON (Timer 2 Register dengan alamat 0C8H), T2MOD (Timer 2 Mode dengan alamat 0C9H), WMCON (Watchdog and Memory Control Register dengan alamat 96H), SPCR (SPI Control Register dengan alamat D5H), SPSR (SPI Status Register dengan alamat AAH), SPDR (SPI Data Register dengan alamat 86H)

2.3.4.3.1. SFR Untuk Timer 2

Mikrokontroler AT89S8252 terdapat tambahan sebuah Timer/Counter yang diberi nama Timer 2 (sehingga AT89S8252 memiliki 3 Timer/Counter yaitu

Timer/Counter 0, Timer/Counter 1, Timer/Counter 2). Pada Timer/Counter 2 ini dikendalikan oleh SFR yang bernama T2CON (Timer 2 Control), T2MOD (Timer 2 Mode) dan sepasang register RCAP2H, RCAP2L yang merupakan register *capture/reload* untuk Timer 2 dalam 16-bit *capture mode/auto-reload mode*.

2.3.4.3.2. SFR Untuk Watchdog dan Memori

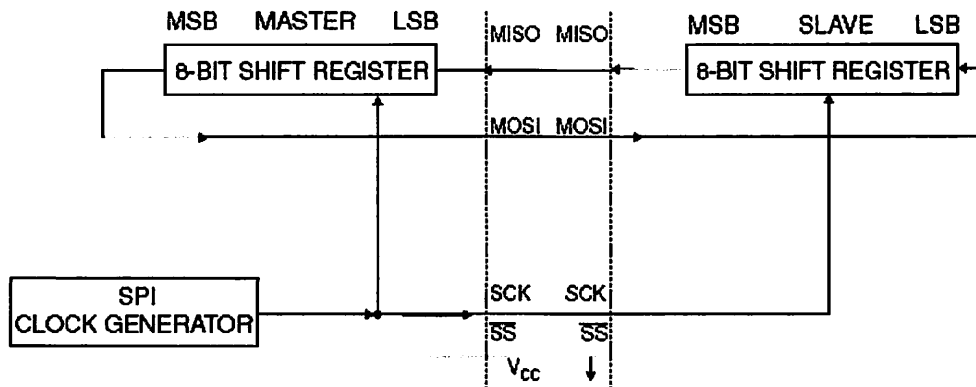
Untuk menggunakan Watchdog Timer/Memori, maka dapat dilakukan dengan mengatur SFR yang bernama WMCON dengan alamat 96_H.

2.3.4.3.3. SFR Pengontrol SPI

Berbeda dengan mikrokontroler MCS-51, AT89S8252 memiliki fasilitas SPI (*Serial Peripheral Interface*). Fasilitas ini memungkinkan transfer data kecepatan tinggi secara sinkron antara mikrokontroler dengan peripheral atau antar mikrokontroler AT89S8252. Fitur ini meliputi :

- a. *Full Duplex*, 3 kawat dengan transfer data secara sinkron
- b. Operasi Master atau Slave
- c. Frekuensi maksimum 6 MHz
- d. 4-bit rate terprogram
- e. Sistem data transfer MSB dahulu atau LSB
- f. *Write Collision Flag Protection*

Gambar berikut menunjukkan hubungan antara CPU master dan slave.



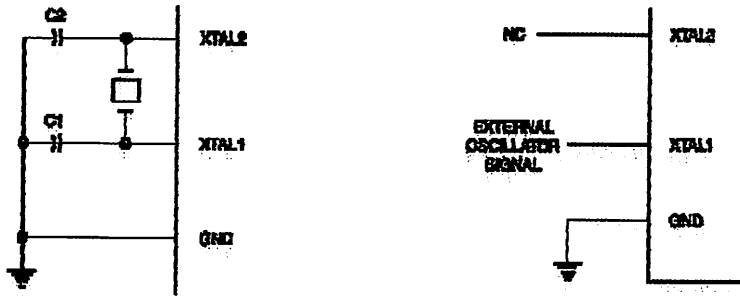
Gambar 2-7. SPI Master-slave Interconnection

Sumber : Datasheet Atmel

2.3.4.3.4. Osilator

Jantung dari AT89S8252 adalah rangkaian yang membangkitkan pulsa clock yang mensinkronkan semua operasi internal. Mikrokontroler AT89S8252 memiliki osilator internal (*on-chip oscillator*) yang dapat digunakan sebagai sumber pewaktu (clock) bagi CPU. Untuk menggunakan osilator internal diperlukan sebuah kristal atau resonator keramik antara pin XTAL₁ dan XTAL₂ dan sebuah kapasitor ke ground. XTAL₂ dan XTAL₁ secara berurutan merupakan input dan output dari sebuah inverting amplifier yang dapat dikonfigurasi penggunaannya sebagai *on-chip oscillator* seperti yang ditunjukkan pada gambar 2.12a.

Untuk memberikan IC AT89S8252 sumber clock eksternal, maka pin XTAL₂ dibiarkan tidak berhubungan dengan sumber clock eksternal dan XTAL₁ dihubungkan dengan sumber clock eksternal seperti pada gambar 2.12b.



a). Oscillator Connector

b). External Clock Drive Configuration

Gambar 2-8. Karakteristik Osilator

Sumber : Data Sheet AT89S8252

2.3.4.3.5. Timer dan Counter

Dalam mikrokontroler AT89S8252 terdapat 3 buah pewaktu/pencacah (Timer/Counter) 16-bit yang dapat diatur melalui perangkat lunak, yaitu pewaktu/pencacah 0 dan pewaktu/pencacah 1. Timer/Counter ini diatur oleh SFR (*Special Function Register*) yaitu Timer/Counter Control (TCON dengan alamat 88_H) dan Timer/Counter Mode Control (TMOD dengan alamat 89_H). Selain itu nilai byte bawah dan byte atas dari Timer/Counter disimpan dalam register TL dan TH.

Jika difungsikan sebagai Timer, maka akan menggunakan sistem clock sebagai sumber masukan pulsanya. Jika sebagai Counter (pencacah), maka akan menggunakan pulsa dari luar (eksternal) sebagai masukan pulsanya. Pada port 3 terdapat fungsi khusus yaitu T0 (masukan luar untuk Timer/Counter 0) dan T1 (masukan luar untuk Timer/Counter 1). Pemilihan mode Timer/Counter dikontrol oleh register TMOD. Dengan memberikan nilai tertentu pada register TMOD,

dapat dipilih mode operasi untuk Timer/Counter 0 dan Timer/Counter 1 seperti terlihat dalam tabel.

Tabel 2-3. Mode Operasi Timer/Counter 0 dan 1

Mode	Timer/Counter 0	Timer/Counter 1
0	13-bit Timer	13-bit Timer
1	16-bit Timer	16-bit Timer
2	8-bit auto-reload	8-bit auto-reload
3	Dua 8-bit Timer	Tidak bekerja

Pada mikrokontroler terdapat tambahan Timer 2. Timer yang lain adalah Timer 0 dan Timer 1. Timer 2 ini merupakan Timer/Counter 16-bit dan memiliki 3 mode operasi yaitu *capture*, *auto-reload (up-down counting)* dan *baund rate generator*. Untuk memilih mode ini dilakukan dengan mengatur bit pada SFR T2CON (Timer 2 Control Register). Timer 2 ini terdiri dari 2 buah Timer 8-bit register yaitu TH2 dan TL2. Pada fungsi Timer, register TL2 dinaikkan (*increament*) tiap siklus mesin. Karena siklus mesin terdiri dari 12 periode osilasi, maka *count rate* menjadi 1/12 dari frekuensi osilator. Sedangkan pada fungsi Counter, register dinaikkan berdasarkan tanggapan adanya transisi tinggi ke rendah pada pin yang bersesuaian (dalam hal ini pin T2 atau P1.0). Tabel berikut menunjukkan mode operasi yang dapat dijalankan pada Timer 2.

Tabel 2-4 Mode Operasi Timer 2

RCLK + TCLK	CP/RL2	TR2	MODE
0	0	1	16-bit auto-reload
0	1	1	16-bit capture
1	X	1	Baud Rate Generator
X	X	0	Off

Keterangan^[1] :

RCLK = *Receive Clock Enable*. Jika diset menyebabkan serial port menggunakan pulsa *overflow* Timer 2 sebagai detak penerimaan pada serial port. Jika RCLK = 0, maka Timer 1 yang digunakan

TCLK = *Transmit Clock Enable*. Jika diset menyebabkan serial port menggunakan pulsa *overflow* Timer 2 sebagai detak pengiriman. Jika TCLK = 0, maka pulsa *overflow* Timer 1 yang digunakan

CP/RL2 = Pemilihan *Capture/Reload*. Jika diset maka proses *capture* yang terjadi sedangkan jika bit ini diclear maka proses *reload*

2.3.4.3.6. Sistem Interrupt

AT89S8252 memiliki 6 buah sumber interupsi, 2 eksternal interupsi (INT0 dan INT1), 3 Timer interupsi (Timer 0,1 dan 2) dan satu serial port interupsi.

INT0 = interrupt pada P3.2 (kaki 12)

INT1 = interrupt pada P3.3 (kaki 13)

Timer 0 = Timer pada P3.4 (kaki 14)

Timer 1 = Timer pada P3.5 (kaki 15)

Port serial = jika pengiriman/penerimaan suatu frame telah lengkap

Saat terjadinya interupsi, mikrokontroler secara otomatis akan menuju *subroutine* pada alamat tersebut. Setelah interupsi servis selesai dikerjakan, mikrokontroler akan mengerjakan program semula. Dua sumber eksternal adalah INT0 dan INT1, kedua interupsi eksternal akan aktif, transisi tergantung isi IT0 dan IT1 pada register TCON. Interrupt T0 dan T1 aktif pada saat Timer yang sesuai mengalami *roll over*. Interupsi serial akan dibangkitkan dengan melakukan operasi OR pada R1 dan T1 tiap-tiap sumber interupsi dapat *enable* atau *disable* secara *software*. Tingkat prioritas semua sumber interupsi dapat diprogram sendiri-sendiri dengan set atau *clear bit* pada SFR IP (*interrupt priority*). Register yang akan berperan dalam mengatur aktif tidaknya interupsi adalah Interrupt Enable Register.

2.4.1 Metode Pengalamatan

Metode pengalamatan yang digunakan pada MCS-51 terbagi menjadi dua jenis, yaitu pengalamatan langsung dan pengalamatan tidak langsung. (Moh. Ibnu Malik, 1997:36)

φ Pengalamatan Tak Langsung

Operasi pengalamatan tak langsung menunjukkan ke sebuah register yang berisi lokasi alamat memori yang akan digunakan dalam suatu operasi. Lokasi

yang nyata tergantung dari isi register saat instruksi dijalankan. Untuk melakukan pengalamatan tak langsung digunakan simbol @. Misalnya :

- ADD A, @R0 : tambahkan isi R0 dengan Acc dan hasilnya di Acc
- DEC @R1 : kurangi isi dari alamat R1

φ Pengalamatan Langsung

Pengalamatan langsung dilakukan dengan memberikan nilai ke suatu register secara langsung. Untuk melakukan hal tersebut digunakan tanda #.

Misalnya:

- MOV A,#01H : isi Acc dengan data 01H
- MOV DPTR,#19H : isi DPTR dengan data 19H

Pengalamatan data langsung dari 0 sampai 127 akan mengakses RAM internal, sedangkan pengalamatan dari 128 sampai 255 akan mengakses register perangkat keras. Misalnya :

- MOV P3,A : pindahkan isi Acc ke alamat *Port* 3 (B0H)
- INC 50 : naikkan lokasi 50 (desimal) dalam memori

2.4.2 Bahasa Assembler MCS-51

Bahasa assembler digunakan dalam setiap operasi CPU dalam bentuk bahasa simbol yang disusun berurutan dalam pernyataannya. Masing-masing pernyataan akan diterjemahkan ke dalam instruksi bahasa mesin atau sering

disebut *operation code/opcode*. Dalam penulisan bahasa mesin ini, terdapat berbagai macam kelompok instruksi, diantaranya :

- **Perpindahan Data**

Instruksi ini digunakan untuk memindahkan data antar register, memori, register-memori, antar muka register dan antar muka memori.

Contohnya: **MOV A,R0** : memindahkan isi register R0 ke Acc.

MOV A,@R0 : memindahkan isi alamat R0 ke Acc.

- **Operasi Aritmatika**

Instruksi ini melaksanakan operasi aritmatika yang meliputi penjumlahan, pengurangan, perkalian, maupun pembagian.

Contohnya: **ADD A,#data** : menambah Acc dengan data.

ADC A,#data : menambah Acc dengan data dan carry.

INC R6 : menambah isi R6 dengan 1.

DEC R7 : mengurangi isi R7 dengan 1.

MUL AB : mengalikan isi Acc dengan isi register B.

DIV AB : membagi isi Acc dengan isi register B.

- **Operasi Percabangan**

Instruksi ini mengubah urutan normal pelaksanaan suatu program untuk melaksanakan pada lain tempat yang kita perlukan pada saat itu.

Contohnya:

1. CJNE (*Compare Jump Not Equal*)

Instruksi ini membandingkan isi lokasi memori tertentu dengan isi Acc, jika sama instruksi ini selanjutnya akan dieksekusi. Jika tidak sama eksekusi akan kembali ke alamat kode yang telah ditunjuk.

2. JB (*Jump if Bit Set*)

Instruksi ini akan menguji suatu alamat bit isi satu, eksekusi akan menuju ke alamat kode dan jika tidak instruksi akan dilanjutkan.

3. JNB (*Jump if Bit Not Set*)

Instruksi ini menguji suatu alamat bit. Jika berisi 0 maka eksekusi akan menuju ke alamat kode. Jika berisi 1 maka instruksi selanjutnya yang akan dieksekusi.

2.5 Komunikasi Serial

Dalam dunia komunikasi ada dua cara pemindahan data yaitu secara paralel dan serial. Perbedaan dua cara tersebut terletak pada jumlah bit yang dipindahkan. Setiap data merupakan kelompok dari bit-bit tersebut, dikenal dengan istilah *byte* yang merupakan kelompok yang terdiri dari 8 bit, serta *word* yaitu kelompok yang terdiri dari 16 bit.

Pada komunikasi serial terjadi pemindahan data satu bit pada satuan waktu, sedangkan pada komunikasi paralel terjadi pemindahan data secara berurutan dari sekelompok bit pada satuan waktu.

Ditinjau dari arah komunikasi data, dikenal ada tiga cara, yaitu: komunikasi *simplex*, *half duplex* dan *full duplex*.

1. Komunikasi *simplex* adalah sistem komunikasi data yang arah perpindahan datanya satu arah saja.
2. Komunikasi *half duplex* adalah sistem komunikasi data yang arah perpindahan datanya dua arah, namun proses pemindahannya tidak bersamaan.
3. Komunikasi *full duplex* adalah sistem komunikasi yang arah perpindahan datanya dua arah secara bersamaan.

Yang dimaksud dengan komunikasi secara serial adalah komunikasi dengan memanfaatkan hanya satu saluran sinyal untuk pengiriman dan penerimaan data. Untuk data digital yang merupakan serangkaian bit maka data dikirimkan bit per bit. Pengiriman akan dimulai dari LSB (*Least Significant Bit*), dan diakhiri dengan MSB (*Most Significant Bit*). Setiap karakter yang dikirimkan disusun sesuai dengan suatu urutan bit tertentu.

2.6 Metode Transmisi Serial

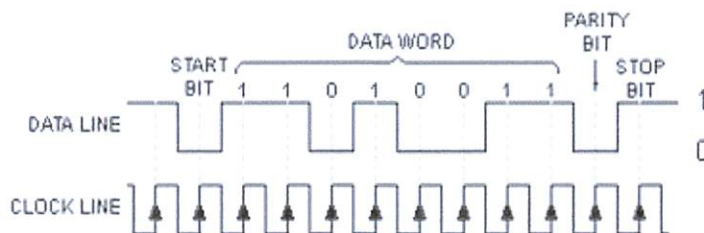
Ada dua metode transmisi serial yang digunakan yaitu:

1. Komunikasi Serial *Sinkron* (*Synchronous Serial Communication*)

Pada komunikasi metode ini, pengiriman dan penerimaan akhir komunikasi adalah secara sinkron atau serempak menggunakan *clock* yang tepat, waktu dalam periode terpisah tiap bit dengan pengecekan *clock* pada penerimaan akhir. Salah satu aspek penting pada metode ini jika akhir dari komunikasi kehilangan sinyal *clock*, maka komunikasi akan *terminasi*.

2. Komunikasi Serial *Asinkron* (*Asynchronous Serial Communication*)

Komunikasi metode ini sinyal *clock* pengirim dan penerima data tidak harus *sinkron* untuk setiap bit data yang ditransmisikan. Karena itu sinyal *clock* tidak perlu dikirimkan. Hal ini bukan berarti tidak ada usaha *sinkronisasi* sama sekali antara pengirim dan penerima data. *Sinkronisasi* dilakukan dengan pengiriman sebuah bit awal (*bit start*) sebelum serangkaian bit data dikirimkan. Agar selama penerimaan data, *clock* penerima tidak melesat jauh, maka jumlah bit data dalam satu kali pengiriman harus dibatasi. Umumnya batasan maksimal 8 bit data (*1 byte*) dalam satu kali pengiriman. Oleh sebab itu komunikasi serial *asinkron* biasanya digunakan pada perangkat yang menghasilkan data dengan laju rendah. Kemudian untuk menjamin adanya transisi sinyal minimal satu kali diantara dua pengiriman rangkaian bit data, maka pengiriman data perlu diakhiri dengan bit penutup (*bit stop*) yang memiliki polaritas yang berbeda dengan bit pembuka.



Gambar 2-9. Asynchronous Serial Data Frame (8E1)

(Sumber: www.google.com)

Bagian penting yang lain pada setiap sinyal serial *asinkronous* adalah *bit rate* pada data yang dikirimkan. Kecepatan data yang diterima didasarkan pada kecepatan minimum 300bps (*bit per second*).

2.7 Perencanaan Perangkat Keras Modulator Demodulator

Sinyal digital pada komputer(data) yang akan dikirimkan atau ditransmisikan secara jarak jauh harus dimadulasikan dengan sinyal analog. Pada dasarnya ada tiga metode atau teknik untuk memodulasi data ke gelombang pembawa, yaitu ASK, FSK dan PSK. Dalam tugas akhir ini kami hanya membahas teknik modulasi dan demodulasi FSK

Modulasi FSK (*Frekuensi Shift Keying*) adalah modulasi yang menyatakan sinyal digital 1 sebagai nilai tegangan dengan frekuensi tertentu (misalnya 1200Hz) sementara sinyal digital 0 dinyatakan sebagai suatu nilai tegangan dengan frekuensi tertentu yang berbeda (misalnya 2200Hz). Sistem FSK ini sangat berguna dan menguntungkan karena pengaruh desah dan interferensi sangatlah kecil.

2.7.1 XR-2206 (Modulator FSK)

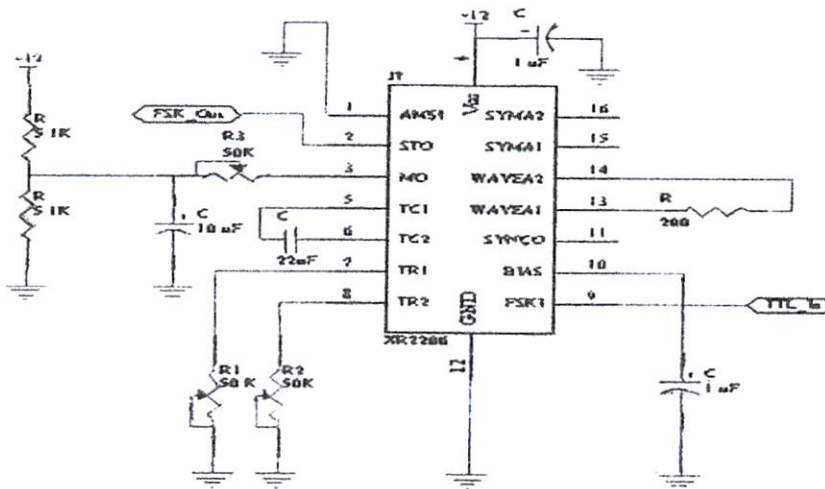
Rangkaian untuk membangkitkan FSK XR-2206 yang diaplikasikan sebagai FSK generator dengan kecepatan 1200bps menggunakan frekuensi *mark* 1200Hz dan *space* 2200Hz dapat bekerja dengan dua buah *timing resistor* R1 dan R2 yang dihubungkan pada pin 7 dan pin 8, dan ditentukan oleh pemilihan kapasitor eksternal yang dihubungkan antara pin 5 dan pin 6. *Timing resistor* ini bekerja bergantian sesuai dengan level tegangan pada pin 9. jika pin 9 diberi tegangan bias ≥ 2 V (logika 1), maka hanya R1 yang bekerja. Sebaliknya jika pin 9 diberi tegangan ≤ 1 V (logika 0), maka hanya R2 yang bekerja. Sehingga

frekuensi keluaran (pin no.2) berubah-ubah diantara dua frekuensi f_1 dan f_2 .

Besarnya f_1 dan f_2 dapat ditentukan dengan persamaan :

$$f_1 = 1/(R_1.C),$$

$$f_2 = 1/(R_2.C)$$



Gambar 2-10. Komponen modulator XR-2206

(Sumber: www.exar.com)

Frekuensi osilasi f_0 , ditentukan oleh timing kapasitor yang terhubung dengan pin 5 dan pin 6 serta oleh timing resistor R_1 dan R_2 yang terhubung dengan pin 7 dan pin 8, dengan ketentuan

$$f_0 = 1/RC \text{ Hz}$$

Mempertimbangka nilai R yang disarankan antara $4 \text{ K}\Omega - 20 \text{ K}\Omega$, diinginkan agar nilai timing resistor R_1 dan R_2 dengan frekuensi (*mark*) pada $f_1 = 1200 \text{ Hz}$ dan biner 0 (*space*) pada $f_2 = 2200 \text{ Hz}$ dalam jangkauan $10 \text{ k}\Omega$ sampai $50 \text{ k}\Omega$ Nilai kapasitor C diperoleh setelah memasukkan nilai-nilai variable yang

telah diketahui yaitu R1, R2, dan f dengan mempertimbangkan nilai komponen kapasitor yang disarankan pada datasheet dan nilai komponen standart.

Adapun perhitungan untuk menentukan nilai komponen eksternal dari modulator FSK sebagai berikut:

Untuk nilai R1=50KΩ dan f1=1200Hz

$$F1 = \frac{1}{R1.C}$$

Setelah memperoleh komponen C dengan f2 = 2200 Hz dapat menentukan nilai R2 senagai nerikut

$$R2 = \frac{1}{f2.C}$$

2.7.2 XR-2211 (Demodulator FSK)

Rangkaian demodulator berfungsi mengubah sinyal FSK yang diterima walky talky menjadi data biner. Untuk mendemodulasikan sinyal FSK tersebut digunakan IC XR-2211. XR-2211 adalah sebuah IC *monolithic phase locked loop* yang dirancang untuk komunikasi data khususnya aplikasi modem FSK.

Demodulator FSK dirancang untuk mendemodulasi sinyal FSK dengan frekuensi biner 1 (*mark*) 1200 Hz dan biner 0 (*space*) 2200 Hz dengan kecepatan 1200bps. Untuk mendemodulasi sinyal FSK dengan frekuensi tersebut maka pemilihan nilai-nilai komponen eksternal sntsr lain:Ro, R1, Co, C1, Cf.

Adapun perhitungan untuk sistem demodulator yang akan dibuat dikemukakan dalam perhitungan berikut:

1. Menentukan PLL counter frekuensi

$$F_o = \sqrt{f_1 \cdot f_2}$$

2. Menghitung timing resistor dengan $R_o = 10k$ dan $V_R R_x = 10k$

$$R_o = R_o + \frac{R_x}{2}$$

3. Menghitung nilai C_o

$$C_o = \frac{1}{R_o \cdot f_o}$$

4. Menghitung nilai R_1

$$R_1 = \frac{R_o \cdot f_o}{(f_1 - f_2)^2}$$

5. menghitung nilai C_1

$$C_1 = \frac{1250 \cdot C_o}{R_1 \cdot 2}$$

6. Menghitung nilai R_f (paling sedikit 5 kali nilai R_1)

$$R_f = R_1 \cdot 5$$

7. Menghitung nilai R_b (nilainya paling sedikit 5 kali nilai R_f)

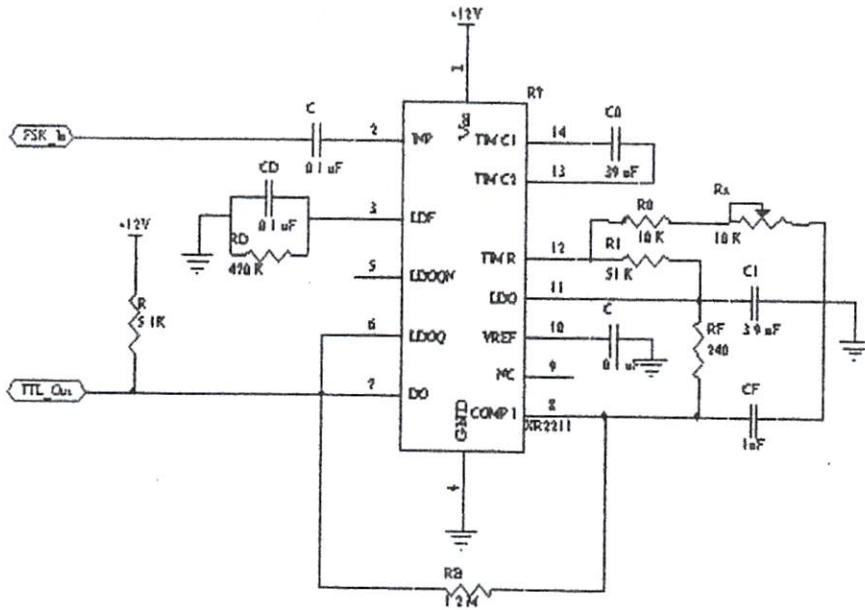
$$R_b = R_f \cdot 5$$

8. Menghitung R_{sum}

$$R_{sum} = \frac{(R_f + R_1) \cdot R_b}{(R_f + R_1 + R_b)}$$

9. Menghitung nilai C_r

$$C_r = \frac{0,25}{(R_{sum} \cdot Boudrate)}$$



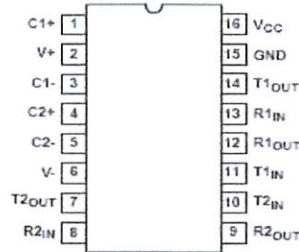
2-11. Komponen Demodulator XR-2211
(Sumber: www.exar.com)

Pada gambar di atas pin no. 2 (*FSK Input*) pada IC XR-2211 merupakan sinyal masukan demodulator yang berasal dari sinyal keluaran HT (*speaker*) dimana pada pin ini sinyal berupa sinyal FSK, dan pin no. 7 (*Data Output*) merupakan sinyal keluaran digital, disini mengalami proses demodulasi (data biner) yang dihubungkan pada komputer atau minimum sistem.

2.8 Interface RS-232

Interface jika diterjemahkan, mungkin akan mengandung arti sebagai antarmuka. Dalam suatu sistem komputer apabila ada alat yang dihubungkan akan dapat mengganggu komputer tersebut. Sinyal-sinyal yang tidak dikenal akan merusak rangkaian komputer. Untuk itu, dibutuhkan suatu *Interface* yang

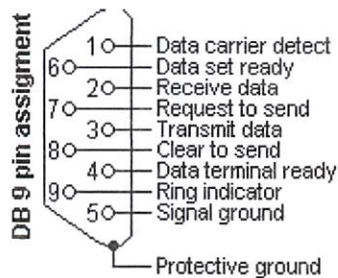
berfungsi sebagai antarmuka dua lingkungan yang berbeda. *Interface* merupakan semacam pintu gerbang dikenal sebagai *I/O Port*.



Gambar 2-12. IC RS 232

a) Konfigurasi Pin

Sebuah komputer atau peralatan lain akan dapat bertukar informasi melalui *Interface port I/O* serial yang disebut *Interface RS 232*. RS 232 merupakan suatu *Interface* antara terminal data dan peralatan komunikasi data yang menggunakan data biner serial sebagai data yang ditransmisikan. RS 232 mengirim dan menerima data dengan kecepatan di atas 120kbps, bahkan kecepatannya mampu mencapai 250 kbps. Salah satu konektor yang biasa digunakan adalah konektor DB 9 seperti ditunjukkan gambar berikut



Gambar 2-13. Konektor DB 9

(Sumber: www.dallas%20semiconductor.com)

Pada dasarnya semua pin-pin memiliki fungsi yang berbeda, tetapi tidak semua digunakan. Fungsi-fungsi pin konektor DB 9 tertera pada tabel 2.1. berikut.

Tabel 2-5. Konfigurasi Pin DB 9

DB-9 Pin	Signal	Function
2	RD	Received data
3	TD	Transmitted data
8	CTS	Clear to send
7	RTS	Request to send
6	DSR	Data set ready
5	SG	Signal ground
4	DTR	Data terminal ready
1	DCD	Data carrier detect

(Sumber: www.google.com)

Sinyal yang dikeluarkan oleh komputer serial secara DCE maupun DTE adalah:

- RTS (*Request To Send*)

Sinyal ini digunakan oleh PC untuk memberitahu kepada modem bahwa PC akan mengirim data. Apabila modem dalam kondisi siap, maka modem akan memberikan sinyal CTS.

- CTS (*Clear To Send*)

Sinyal yang dikirimkan modem untuk memberitahu kepada PC bahwa telah dapat dilakukan pengiriman data.

- DTR (*Data Terminal Ready*)

Sinyal yang digunakan oleh PC untuk memberitahu kepada modem bahwa PC siap menerima data dari modem.

- DSR (*Data Set Ready*)

Sinyal yang digunakan modem sebagai tanggapan dari sinyal DTR, dengan sinyal ini PC akan tahu modem dalam kondisi ON.

- RI (*Ring Indication*)

Sinyal indikator yang digunakan untuk memberitahu pada PC bahwa ada sinyal dering dari line telepon.

- TxD (*Transmitted Data*)

Sinyal yang digunakan modem untuk memberitahu bahwa data sudah dikirim.

- RxD (*Receive Data*)

Sinyal yang digunakan modem untuk memberitahu bahwa data sudah diterima.

b) Karakteristik Sinyal Listrik *Interface RS 232*

CCITT telah merekomendasikan karakteristik sinyal listrik pada rangkaian *Interface V-24* . Karakteristik sinyal listrik yang dimaksudkan adalah batas-batas tegangan yang digunakan. Dalam rekomendasi tersebut dibedakan antara sinyal

data dan sinyal kontrol, sinyal data sebagai logika '0' dan '1', sedangkan sinyal kontrol dinyatakan dengan ON dan OFF. Sinyal-sinyal tersebut mempunyai batas-batas (daerah) tegangan yang ditunjukkan pada tabel 2.2.

Tabel 2-6. Tabel Karakteristik Sinyal Listrik Protokol RS 232

Sinyal	Nilai	Daerah Tegangan
Sinyal data	1	$-3V \geq V_p \geq -15V$
	0	$+3V \leq V_p \leq +15V$
Sinyal control	ON	$+3V \leq V_p \leq +15V$
	OFF	$-3V \geq V_p \geq -15V$

(Sumber : P. C. Den Heijer, R. Tolsma, 1991: 133)

Dalam standar RS232, tegangan antara +3 sampai +15 Volt pada input *Line Receiver* dianggap sebagai *level* tegangan '0', dan tegangan antara -3 sampai -15 Volt dianggap sebagai *level* tegangan '1'.

Untuk mengurangi kemungkinan terjadinya gangguan '*cross talk*' antara kabel saluran sinyal RS 232, kecuraman perubahan tegangan sinyal dibatasi tidak boleh lebih dari 30 Volt/mikro-detik, makin besar kecuraman sinyal, makin besar pula kemungkinan terjadi '*cross talk*'. Di samping itu ditentukan pula kecepatan transmisi data seri tidak boleh lebih besar dari 20 KiloBit/Detik. Impedansi saluran dibatasi antara 3 Kilo-Ohm sampai 7 Kilo-Ohm, dalam standar RS232 yang pertama ditentukan pula panjang kabel tidak boleh lebih dari 15 Meter (50 feet), tapi ketentuan ini sudah di-revisi pada standar RS232 versi 'D'. Dalam ketentuan baru tidak lagi ditentukan panjang kabel maksimum, tapi ditentukan

nilai kapasitan dari kabel tidak boleh lebih besar dari 2500 pF, sehingga dengan menggunakan kabel kualitas baik bisa dicapai jarak yang lebih dari 50 *feet*.

c) Protokol Komunikasi pada RS 232

Beberapa protokol pada *Interface* RS 232 adalah:

- *Start Bits*

Merupakan sebuah bit dengan logic '0', bit ini yang menandakan bahwa akan ada karakter atau data yang mengikutinya. Bit ini langsung diberikan oleh sinyal *device* tanpa harus mengeset terlebih dahulu.

- *Data Bits*

Merupakan bit yang mewakili dari karakter yang diikutinya, data bit ini dapat diset sepanjang antara 5 sampai 8 bit.

- *Parity Bits*

Merupakan bit yang digunakan sebagai *error checking* pada *receiver*. *Parity bit* akan menghitung jumlah data yang berlogika '1' pada data bit. Perhitungan jumlah data bit tersebut tergantung dari jenis *parity* yang diset. Untuk *parity 'even'*, jumlah data bit yang berlogika '1' ditambah dengan *parity bit* akan menghasilkan jumlah yang ganjil. Sedangkan untuk *parity 'mark'*, merupakan *parity bit* yang selalu berlogika '1' begitu pula pada space, *parity bit* selalu berlogika '0' dan *parity 'none'* merupakan *parity bit* yang diabaikan.

- *Stop Bits*

Merupakan bit yang menandakan akhir dari suatu paket data (biasanya 1 byte data). Seperti pada data bit, bit ini langsung diberikan dari serial device. *Stop bit* ini dapat diset menjadi satu bit, satu setengah dan dua bit.

- *Boud Rate*

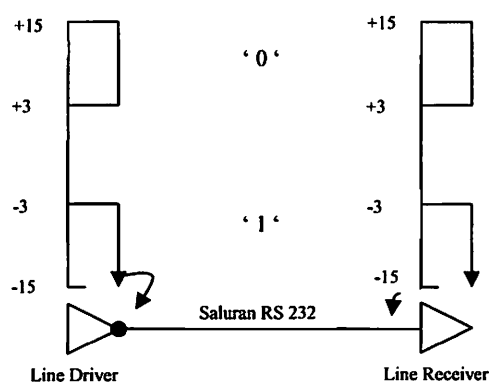
Baud Rate digunakan untuk menunjukkan kecepatan dari transmisi (bits per second)

RS MAX 232 tersusun 2 bagian yaitu : RS 232 line driver yang berfungsi mengubah level tegangan TTL ke level tegangan RS 232 dan RS 232 linereceiver yang berfungsi mengubah tegangan RS 232 ke level tegangan TTL.

Standard RS 232 ditetapkan oleh Electronic Industry Association dan Telecommunication Industry Association pada tahun 1962. Standard ini hanya menyangkut komunikasi data antara komputer (Data terminal Equipment – DTE) dengan alat-alat pelengkap lainnya (Data Circuit – terminating Equipment – DCE).

Ada 3 hal pokok yang diatur standard RS 232, antara lain adalah:

1. Bentuk sinyal dan level tegangan yang dipakai



Level tegangan sinyal RS 232 adalah seperti terlihat pada gambar. Dalam standard RS 232 ,tegangan antara +3 sampai +15 volt baik pada sinyal input line receiver maupun pada line driver dianggap sebagai tegangan '0', dan tegangan antara -3 sampai-15 volt dianggap sebagai tegangan '1'.

2. Penentuan jenis sinyal dan konektor yang dipakai, serta susunan sinyal pada kaki-kaki di konektor. Jenis-jenis sinyal yang dipakai mengatur pertukaran informasi antara DTE dan DCE, semuanya terdapat 24 jenis sinyal tetapi yang umum dipakai hanyalah 9 jenis sinyal.
3. Penentuan tata cara pertukaran antara computer dan alat-lat pelengkapya maupun alat-alat digital.

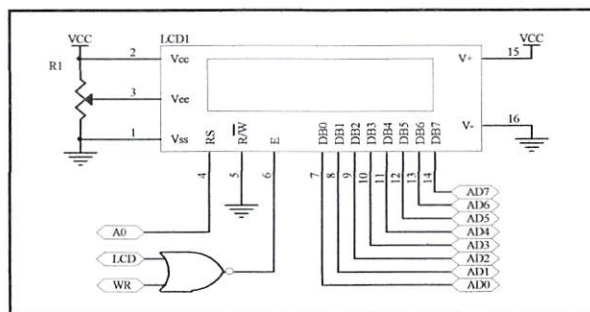
2.9. LCD

Liquid Crystal Display atau LCD merupakan komponen optoelektronik yaitu komponen yang bekerja atau dipengaruhi oleh sinar (optolistrik), komponen pembangkit cahaya (light emitting) dan komponen-komponen yang akan mengubah sinar. LCD terbuat dari bahan kristal cair yang merupakan suatu komponen organik dan mempunyai sifat optik seperti benda padat meskipun bahan tetap cair.

Sel kristal cair terdiri dari selapis bahan kristal cair yang diapit antara dua kaca tipis yang transparan. Antara dua lembar kaca tersebut diberi bahan kristal cair (*liquid crystal*) yang tembus cahaya. Permukaan luar dari masing-masing keping kaca mempunyai lapisan penghantar tembus cahaya seperti oksida timah (*tin oxide*) atau oksida indium (*indium oxide*). Sel mempunyai ketebalan sekitar 1×10^{-5} meter dan diisi dengan kristal cair.

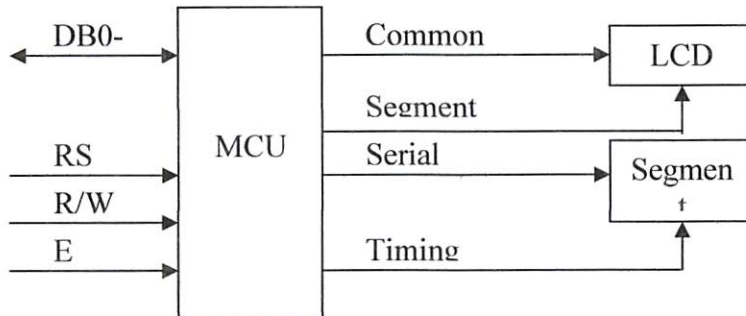
Karena sel-sel kristal cair merefleksikan cahaya dan bukan membangkitkan cahaya maka konsumsi daya yang dibutuhkan relatif rendah. Energi yang dipergunakan hanya untuk mengaktifkan kristal cair. Pada dasarnya LCD bekerja pada tegangan rendah (3 – 15 Vrms), frekuensi rendah (25 – 60 Hz) sinyal AC dan memakai arus listrik yang sangat kecil (25 - 300 μ A). LCD seringkali ditata sebagai tampilan *seven segment* untuk menampilkan angka tetapi juga memiliki keistimewaan lain, yaitu kemampuan untuk menampilkan karakter dan berbagai macam simbol.

Salah satu jenis LCD diantaranya adalah LCD M1632, suatu jenis piranti dengan konsumsi daya yang rendah, disusun dari dot matrik dan dikontrol oleh ROM atau RAM generator karakter dan RAM data display. Pengontrolan utamanya adalah pada ROM generator dan display data RAM yang menghasilkan kode ASCII jika padanya diberikan input ASCII. Untuk dapat difungsikan dengan baik maka perlu diperhatikan proses analisis yang telah ditentukan oleh pabrik pembuatnya. Timing penganalisan sangat dipertimbangkan, karena jika meleset sampai ordo *milisecon* maka dapat dipastikan LCD tidak dapat berfungsi.



Gambar 2-14. Konfigurasi Kaki LCD

(Sumber: www.google.com)



Gambar 2-15. Blok Diagram LCD

(Sumber: www.google.com)

Adapun karakteristik dari LCD M1632 antara lain :

- Dengan 16 karakter – 2 baris dalam bentuk dotmatrik 5x7 dan cursor
- *Duty ratio* 1/16
- Memiliki ROM pembangkitan karakter untuk 192 jenis karakter
- RAM untuk data display sebanyak 80x8 bit
- Dapat dirangkai dengan MPU 8 bit/4 bit
- RAM data display dan RAM pembangkit karakter dapat dibaca oleh MPU
- Memiliki fungsi instruksi antara lain *display on/off*, *Cursor on/off*, *display karakter blink*, *cursor shift* dan *display shift*
- Memiliki rangkaian osilator sendiri
- Catu tegangan tunggal yaitu ± 5 V
- Memiliki rangkaian reset otomatis pada catu daya yang dihidupkan
- Temperatur operasi $0^0 - 50^0$

LCD memiliki 16 pin yang masing-masing mempunyai fungsi sebagai berikut :

Tabel 2-7. Fungsi Tiap Pin LCD

No. Pin	Simbol	Level	Fungsi	
1	V _{SS}	-	Power Supply	0 V (GND)
2	V _{CC}	-		5 V ± 10%
3	V _{DD}	-		For LCD Drive
4	RS	H/L	Sinyal seleksi register H ; Data Input [register data (write/read)] L ; Instruction Input [register instruksi (write), busy flag dan address counter (read)]	
5	R/W	H/L	H ; Read L ; Write	
6	E	H	Enable Signal [sinyal penanda mulai operasi, aktif saat operasi write atau read]	
7	DB0	H/L	4 bit bus data lower 2 arah, dapat dibaca atau ditulis terhadap mikrokontroler	
8	DB1	H/L		
9	DB2	H/L		
10	DB3	H/L		
11	DB4	H/L	4 bit bus data upper 2 arah, dapat dibaca atau ditulis terhadap mikrokontroler, DB7 juga sebagai busy flag	
12	DB5	H/L		
13	DB6	H/L		
14	DB7	H/L		
15	V+BL	-	Back Light Supply	4 - 4,2 V
				50 – 200 Ma
16	V-BL	-		0 V (GND)

(Sumber: www.google.com)

Instruksi Operasi

Tabel 2-8. Instruksi Pada LCD

Instruksi	RS	RW	D7	D6	D5	D4	D3	D2	D1	D0
Display Clear	0	0	0	0	0	0	0	0	0	1
Cursor Home	0	0	0	0	0	0	0	0	1	*
Entry Mode Set	0	0	0	0	0	0	0	1	I/D	S
Display On/Off	0	0	0	0	0	0	1	D	C	B
Cursor Display Shift	0	0	0	0	0	1	S/C	R/L	*	*
Function Set	0	0	0	0	1	DL	1	*	*	*
CG RAM Address Set	0	0	0	1	A _{CG}					
DD RAM Address Set	0	0	1	A _{DD}						
BF/Address Read	0	1	BF	AC						
Data Write to CG RAM	1	0	Write Data							
Data Read from CG RAM	1	1	Read Data							

*Invalid Bit

A_{CG} ; CG RAM Address

A_{DD} ; DD RAM Address

➤ Operasi Dasar

- Register

Kontrol dari LCD memiliki 2 buah register 8 bit yaitu register instruksi (IR) dan register data (DR). IR memiliki instruksi seperti display, clear, cursor shift dan display data (DD RAM) serta karakter (CG RAM). DR menyimpan data untuk ditulis ke DD RAM ataupun membaca data dari DD RAM dan CG RAM. Ketika data ditulis ke DD RAM atau CG RAM maka DR secara otomatis menulis data ke DD RAM atau CG RAM. Ketika data pada CG RAM atau DD RAM akan dibaca maka alamat data

ditulis pada IR. Sedangkan data akan dimasukkan melalui DR sehingga dapat dibaca oleh mikrokontroler.

Tabel 2-9. Pemilihan Register Pada LCD

RS	RW	Operasi
0	0	Seleksi IR, IR Write Display Clear
0	1	Busy Flag (DB7), @ Counter (DB0-DB7) Read
1	0	Seleksi DR, DR Write
1	1	Seleksi DR, DR Read

- **Busy Flag**

Busy Flag menunjukkan bahwa modul siap untuk menerima instruksi selanjutnya sebagaimana terlihat pada tabel diatas. Register seleksi sinyal akan melalui DB7 jika RS=0 dan R/W=1. Jika bernilai 1 maka sedang melakukan kerja internal dan instruksi tidak akan dapat diterima, oleh karena itu status dari flag harus diperiksa sebelum melaksanakan instruksi selanjutnya.

- **Address Counter (AC)**

AC menunjukkan lokasi memori dalam modul LCD. Pemilihan lokasi alamat lewat Ac diberikan lewat register instruksi (IR) ketika data pada A, maka AC secara otomatis menaikkan atau menurunkan alamat tergantung dari Entry Mode Set.

- Display Data RAM

Pada LCD, masing-masing line memiliki range alamat tersendiri. Alamat itu diekspresikan dengan bilangan hexadesimal. Untuk line 1 range alamat berkisar antara 40_H - $4F_H$.

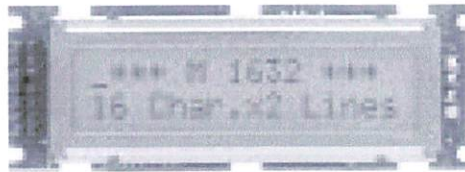
- Character Generator ROM (CG ROM)

CG ROM memiliki tipe dot matrik 5×7 , dimana pada LCD telah tersedian ROM sebagai pembangkit karakter dalam kode ASCII.

- Character Generator RAM (CG RAM)

CG RAM dipakai untuk pembuatan karakter tersendiri melalui program.

Adapun bentuk fisik dari LCD M1632 adalah pada gambar berikut :



Gambar 2-16. Liquid Crystal Display

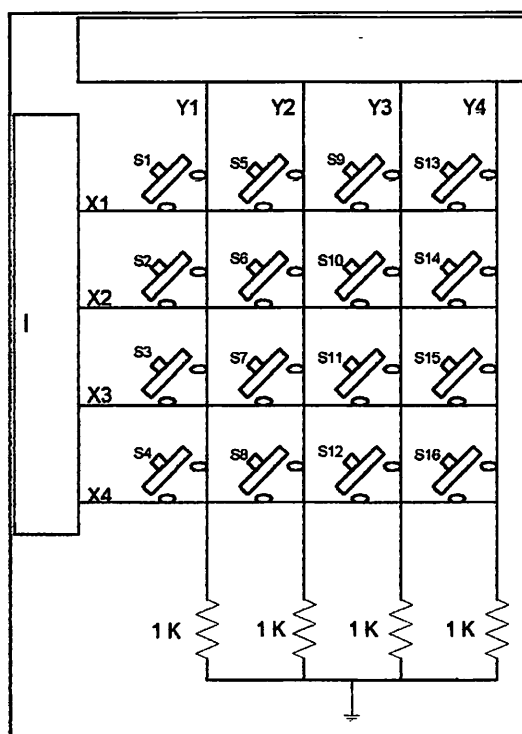
(Sumber: www.google.com)

2.10 Keypad (Papan Tombol)

Papan tombol ini digunakan untuk memasukkan data bila diinginkan. Untuk menterjemahkan informasi yang diterima dari papan tombol, maka keypad dihubungkan dengan port 1.

Papan tombol tersebut mempunyai matrix 3 baris dan 4 kolom. Deretan baris dan kolom dari papan tombol dihubungkan dengan port 1 yang difungsikan sebagai masukan dan keluaran. Deretan kolom dihubungkan dengan ground (berlogika 0) dan port 1 mikrokontroler yang difungsikan sebagai input

mikrokontroler. Sedangkan deretan baris dihubungkan ke port 1 yang telah diberi data 0001 dan secara kontinyu data tersebut bergeser satu bit ke kiri. Pergeseran data satu bit ini dimaksudkan untuk menentukan posisi tombol yang ditekan dalam satu kolom. Port ini difungsikan sebagai output dari mikrokontroler. Dengan demikian kalau tombol tidak ditekan maka masukan port 1 di pin yang terhubung tombol tersebut berlogika 0 dan bila tombol ditekan akan berlogika 1. Rangkaian papan tombol papan tersebut dapat dilihat pada gambar dibawah ini:



Gambar 2-17. Rangkaian Keypad 4x4

(Sumber: www.google.com)

2.10 Pemrograman Visual Basic 6.0

Visual Basic 6.0 merupakan bahasa pemrograman yang cukup populer dan mudah untuk dipelajari. pengguna dapat membuat program dengan aplikasi GUI

(Graphical User Interface) atau program yang memungkinkan pemakai komputer berkomunikasi dengan komputer tersebut dengan menggunakan modus grafik atau gambar.

Visual Basic 6.0 berawal dari bahasa pemrograman BASIC (*Beginners All-purpose Symbolic Instruction Code*). Karena bahasa BASIC cukup mudah dipelajari dan populer maka hampir setiap programmer menguasai bahasa ini.

Tahun 1980-an sistem operasi DOS cukup populer di kalangan pemakai PC karena di dalamnya disertakan bahasa BASIC yang dikenal dengan QBASIC (*QuickBasic*). Sistem tersebut sekarang sudah jarang digunakan. Di era Windows, Microsoft menciptakan Visual Basic yang terus mengalami penyempurnaan hingga Visual Basic 6.0 ini.

2.11.1 Memulai Visual Basic

Pada bagian ini akan dijelaskan bagaimana cara menjalankan Visual Basic 6.0 pada sistem operasi Windows. Cara pertama yang dapat dilakukan untuk memulai Microsoft Visual Basic 6.0 adalah:

1. Klik tombol Start pada Taskbar, kemudian pilih Program dari tampilan menu utama
2. Dari tampilan menu yang ada, pilih Visual Basic 6.0. Untuk memudahkan pemahaman. Perhatikan Gambar I. yang menunjukkan proses cara menjalankan Visual Basic 6.0 dengan menggunakan Windows.

2.11.2 Tampilan Awal Visual Basic

Secara otomatis, pada saat pertama kali menjalankan Visual Basic, akan tampil kotak dialog New Project. Pada kotak dialog tersebut terdapat tiga pilihan tabulasi dengan keterangan sebagai berikut:

Tabel 2-10. Pilihan Tabulasi

Tabulasi	Keterangan
New	Pilihan ini digunakan untuk membuat project baru dengan berbagai macam pilihan.
Existing	Pilihan ini digunakan untuk membuka project yang pernah dibuat sebelumnya dengan menentukan folder sekaligus nama file.
Recent	Pilihan ini digunakan untuk membuka project yang telah dibuat dan terakhir kali dibuka.

2.11.3 Komponen Visual Basic

1. Title Bar

Title bar merupakan batang judul dari program Visual Basic 6.0 yang terletak pada bagian paling atas dari jendela program yang berfungsi untuk menampilkan judul atau namajendela. Selain itu title bar juga berfungsi untuk:

- a. Memindah posisi jendela dengan menggunakan proses drag and drop pada posisi title bar tersebut.
- b. Mengatur ukuran jendela dari ukuran Maximize ke ukuran Restore ataupun sebaliknya dengan melakukan klik ganda pada posisi title bar tersebut.

2. Control Menu

Control Menu merupakan sebuah elemen yang terletak pada bagian sudut kiri atas dari jendela Visual Basic. Dalam sistem operasi Windows, elemen ini tampil dalam bentuk ikon program. Ketika meng-klik Control Menu, akan

tampil daftar menu perintah yang digunakan untuk mengubah ukuran jendela, memindah letak jendela dan juga dapat untuk keluar dari program Microsoft Visual Basic 6.0. Untuk lebih jelasnya, dapat dilihat fungsi dari masing-masing perintah pada tabel di bawah ini:

Tabel 2-11. Fungsi Perintah/Tombol

Tombol	Fungsi
Restore	Mengubah ukuran jendela Visual Basic ke ukuran relatif
Minimize	Mengubah ukuran jendela Visual Basic ke ukuran minimal.
Maximize	Mengubah ukuran jendela Visual Basic ke ukuran maksimal.
Move	Memindah posisi jendela Visual Basic.
Size	Mengatur ukuran jendela Visual Basic.
Close	Keluar dari program Visual Basic.

3. Menu Bar

Menu bar merupakan batang menu yang terletak di bawah title bar yang berfungsi untuk menampilkan pilihan menu atau perintah untuk mengoperasikan program Visual Basic. Saat pertama kali jendela program Visual Basic terbuka, ada tiga belas menu utama, yaitu: File, Edit, View, Project, Format, Debug, Run, Query, Diagram, Tools, Add-Ins, Windows dan Help.

Tampilan pilihan menu dalam program Visual Basic memiliki beberapa variasi yang masing-masing mempunyai pengertian yang berbeda dengan penjelasan sebagai berikut:

- a. Menu dengan tanda segitiga yang terletak pada bagian kanan, di mana apabila menu tersebut dipilih maka akan menampilkan submenu pilihan berikutnya.

- b. Menu yang secara langsung akan menjalankan suatu perintah yang dipilih.
- c. Menu dengan tanda titik tiga pada bagian kanan, apabila dipilih maka akan menampilkan kotak dialog perintah.
- d. Menu yang tampil redup yang mengindikasikan bahwa menu tersebut tidak dapat untuk dipilih.
- e. Menu dengan gambar ikon di sebelah kirinya yang menandakan bahwa selain dapat dengan menggunakan menu tersebut untuk menjalankan suatu perintah, Anda dapat menekan tombol yang ada di toolbar.
- f. Menu dengan Shortcut key di sebelah kanannya yang menandakan bahwa selain dengan menggunakan menu tersebut untuk menjalankan suatu perintah, Anda dapat menekan tombol kombinasi pada keyboard. Misalnya kombinasi antara tombol Shift + F7 untuk mewakili perintah menu View - Object.

4. Toolbar

Toolbar merupakan sebuah batang yang berisi kumpulan tombol yang terletak di bagian bawah menu bar yang dapat digunakan untuk menjalankan suatu perintah. Pada kondisi default program Visual Basic hanya menampilkan toolbar Standard.

Untuk lebih jelasnya tentang fungsi masing-masing tombol pada toolbar standard, perhatikan penjelasan berikut:

Tabel 2-12. Fungsi tombol pada toolbar Standard

Nama Tombol	Fungsi
Add Project	Menambahkan project baru, Dengan pilihan: <ul style="list-style-type: none"> • Standard EXE • ActiveX DLL • ActiveX EXE • ActiveX Control
Add Form	Menambahkan item, dengan pilthan: <ul style="list-style-type: none"> • Form • MDI Form • Module • Class Module • User Control • Property Page • Add File • User Document
Menu Editor	Menampilkan kotak dialog Menu Editor.
Open Project	Membuka project yang sudah pernah dibuat ebelumnya.
Save Project Group	Menyimpan project.
Cut	Memotong kontrol yang ada di jendela form atau teks yang ada di jendela code.
Copy	Menyalin kontrol yang ada di jendela form atau teks yang ada di Jendela code.
Paste	Menempelkan kontrol atau teks yang sudah dipotong dengan perintah Cut atau disalin dengan perintah Copy.
Find	Mencari teks pada jendela code.
Undo	Membatalkan suatu perintah an dialankan sebelumn a..
Redo	Mengulangi suatu perintah yang pernah dibatalkan
Start	Menjalankan program.
Break	Menghentikan program yang sedang jalan untuk Sementara.
End	Menghentikan program yang sedang dijalankan.
Project Explorer	Menampilkan jendela ProjectExplorer.
Properties Window	Menampilkan jendela Properties.
	Menampilkan jendela Form
Window	Layout.
Object	Menampilkan jendela Object
Browser	Browser.
Toolbox	Menampilkan jendela Toolbox.

5. Toolbox

Toolbox merupakan kotak perangkat yang berisi kumpulan tombol objek atau kontrol untuk mengatur desain dari aplikasi yang akan dibuat. Pada kondisi default, toolbox menampilkan tabulasi General dengan 21 tombol kontrol yang dapat ditampilkan dengan menggunakan prosedur:

1. Klik tombol Toolbox di bagian Toolbar Standard.
2. Pilih perintah View - Toolbox.

Untuk penjelasan tentang fungsi masing-masing kontrol, perhatikan tabel berikut:

Tabel 2-13. Fungsi masing-masing Kontrol pada Toolbox

Nama Pengontrol	Fungsi
Pointer	Memilih, mengatur ukuran dan memindah posisi kontrol yang terpasang pada bagian form.
PictureBox	Menampilkan file gambar.
Label	Menambahkan label atau teks tambahan.
TextBox	Menambahkan kotak teks.
Frame	Menambahkan kontrol yang dapat diisi dengan kontrol Option Button atau CheckBox.
Command Button	Menambahkan kontrol tombol perintah.
CheckBox	Menambahkan kontrol kotak periksa.
OptionButton	Menambahkan kontrol tombol pilihan.
ComboBox	Menambahkan kontrol kotak combo yang merupakan kontrol gabungan antara TextBox dan ListBox.
ListBox	Menambahkan kontrol daftar pilihan.
HscrollBar	Menambahkan kontrol batang penggulung horisontal.
VscrollBar	Menambahkan kontrol batang penggulung vertikal.
Timer	Menambahkan kontrol sebagai kontrol pencacah waktu.
DriveListBox	Menambahkan kontrol daftar disk drive pada komputer.
DirListBox	Menambahkan kontrol daftar direktori pada drive aktif.
FileListBox	Menambahkan kontrol daftar file pada direktori aktif.
Shape	Menambahkan kontrol gambar berupa lingkaran, oval, persegi panjang, bujur sangkar dan lain-lain.
Line	Menambahkan kontrol gambar garis lurus.
Image	Menambahkan file gambar dengan pilihan properti yang lebih sedikit dibandingkan kontrol pictureBox.
Data	Menambahkan kontrol yang berupa database
OLE	Menambahkan kontrol yang berhubungan dengan proses relasi antar program aplikasi.

6. Project

Project merupakan suatu kumpulan module atau merupakan program aplikasi itu sendiri. Dalam Visual Basic, file project disimpan dengan nama file berakhiran.VBP, di mana file ini berfungsi untuk menyimpan seluruh komponen program.

Apabila kita membuat suatu program aplikasi baru, maka secara otomatis project tersebut akan diisi dengan objek Form 1. Dalam jendela Project Explorer ditampilkan suatu struktur hirarki dari sebuah project itu sendiri yang berisi semua item yang terkandung di dalamnya. Dengan Project Explorer dapat dipilih objek yang akan dibuat dengan mudah. Untuk Menampilkan jendela Project Explorer, Gunakan Prosedur berikut:

1. Klik tombol Project Explorer pada bagian toolbar Standard.
2. Pilih perintah View-.Project Explorer.
3. Shorcut key Ctrl+R.

Selain menampilkan nama project dan form, pada jendela Project Explorer terdapat tiga tombol dengan penjelasan sebagai berikut:

Tabel 2-14. Tombol pada Project Explorer

Nama Tombol	Fungsi
View Code	Menampilkan jendela Code yang digunakan untuk menulis kode program yang terhubung dengan objek yang terpilih pada jendela form.
View Object	Menampilkan jendela Object untuk item yang terpilih pada form aktif.
Toggle Folders	Menampilkan atau menyembunyikan folder yang menampung nama form dari suatu project.

7. Properties Window

Properties Window merupakan sebuah jendela digunakan untuk menampung nama properti dari yang terpilih. Pengaturan properti pada program Basic merupakan hal yang sangat penting membedakan objek yang satu dengan yang lainnya.

Pada jendela properti ditampilkan jenis dan nama objek yang bisa dipilihurut berdasarkan abjad pada tab Alphanumeric atau berdasarkan kategori pada tab

Categorized. Untuk menampilkan jendela Properties, dapat menggunakan prosedur berikut:

1. Klik tombol Properties Window pada toolbar Standard.
2. Pilih perintah View - Properties Window.
3. Shortcut key F4.

8. Form Layout Window

Form Layout Window merupakan sebuah jendela yang digunakan untuk mengatur posisi dari form pada form saat program dijalankan. Pada saat mengarahkan pointer mouse ke bagian form, maka pointer mouse akan berubah menjadi anak panah empat arah (pointer pengatur posisi). Untuk memindah posisi form pada layar monitor dapat dilakukan dengan proses drag and drop.

Untuk menampilkan jendela Form Layout, dapat menggunakan prosedur berikut:

1. Klik tombol Form Layout Window pada toolbar Standard.
2. Pilih perintah View - Form Layout Window.

9. Immediate Window

Immediate Window merupakan sebuah jendela yang digunakan untuk mencoba beberapa perintah dengan mengetikkan baris program dan dapat secara langsung melihat hasilnya. Hal tersebut biasa dilakukan dan sangat membantu proses pengujian suatu perintah sebelum dipasang di dalam program.

Untuk menampilkan jendela Immediate, menggunakan prosedur berikut:

1. Pilih perintah View - Immediate Window.

2. Shortcut key Ctrl+G.
3. Klik tombol Immediate Window pada toolbar Debug.

10. Form Window

Form Window merupakan jendela desain dari sebuah program aplikasi. Kita dapat mendesain sebuah program aplikasi dengan menempatkan kontrol-kontrol yang ada di bagian toolbox pada area form.

Pada jendela form juga terdapat beberapa elemen yang dapat digunakan untuk mengatur tampilan. Untuk lebih jelasnya perhatikan Gambar I .29.

11. Code Window

Code Window merupakan sebuah jendela yang digunakan untuk menuliskan kode program dari kontrol yang dipasang pada jendela form dengan cara memilih terlebih dahulu kontrol tersebut pada kotak objek.

12. Event

Event merupakan suatu kejadian yang akan diterima oleh suatu objek. Event yang diterima oleh objek berfungsi untuk menjalankan kode program yang ada didalam objek tersebut.

13. Method

Method adalah suatu kumpulan perintah yang memiliki kegunaan yang hampir sama dengan suatu fungsi atau prosedur, tetapi perintah-perintah tersebut sudah disesuaikan dalam suatu objek.

Suatu method dapat dipanggil dengan cara menyebutkan nama objek dan diikuti dengan tanda titik dan nama metodenya. Method umumnya digunakan untuk menjalankan perintah khusus pada suatu objek tertentu.

14. Module

Module hampir sama fungsinya dengan form, tetapi module tidak berisi objek dan bentuk standar. Dan module berisi kode program atau prosedur yang dapat digunakan oleh program aplikasi.

2.11.4 Mengolah Toolbox

Pada kondisi default, pada bagian toolbox terdapat satu tabulasi yaitu tabulasi General. Saat menambahkan item kontrol baru secara otomatis akan ditampilkan pada tab yang aktif (General). Kita dapat mengelompokkan item-item yang akan ditambahkan ke bagian toolbox dengan menggunakan tabulasi buatan sendiri. Diharapkan semua item yang ditambahkan ke toolbox dapat terorganisasi sesuai dengan aplikasi yang dibuat.

1. Menambah Tabulasi

Untuk menambahkan tabulasi ke bagian toolbox, dapat menggunakan prosedur berikut:

1. Klik kanan pada bagian toolbox.
2. Pilih perintah Add Tab sehingga akan tampil sebuah kotak dialog.
3. Ketikkan nama tabulasi pada kotak New lab Name dan klik tombol OK.

2. Menghapus Tabulasi

Untuk menghapus tabulasi dari bagian toolbox. Dapat menggunakan prosedur berikut:

1. Klik kanan bagian tabulasi yang ingin dihapus.
2. Pilih perintah Delete Tab.

3. Mengganti Nama Tabulasi

Untuk mengganti nama tabulasi. dapat menggunakan prosedur berikut:

1. Klik kanan pada bagian tabulasi yang ingin diganti namanya.
2. Pilih perintah Rename Tab.
3. Ketikkan nama tabulasi yang baru dan klik tombol OK.

4. Memindah Posisi Tabulasi

Untuk memindah posisi tabulasi, dapat menggunakan prosedur berikut:

1. Klik kanan pada bagian tabulasi yang ingin Anda pindah posisinya.
2. Pilih perintah Move Up untuk memindah posisi ke atas atau Move Down untuk memindah posisi ke bawah.

5. Menambahkan Item Kontrol

Untuk menambahkan item kontrol, dapat menggunakan prosedur berikut:

1. Aktifkan tabulasi untuk menambahkan item pada bagian kontrol tersebut dengan cara klik.
2. Berikan salah satu perintah berikut:
 - a. Pilih perintah Project .Components.
 - b. Klik kanan pada bagian tabulasi toolbox dan pilih perintah Components.
 - c. Shortcut key Ctrl + y
3. Pada tabulasi Controls, aktifkan kotak periksa dari beberapa pilihan kontrol item yang ingin ditambahkan dan klik tombol Close.

6. Menghapus Item Kontrol

Untuk menghapus item kontrol, dapat menggunakan prosedur berikut:

1. Berikan salah satu perintah berikut:
 - a. Pilih perintah Project - Components.
 - b. Klik kanan pada bagian tabulasi toolbox dan pilih perintah Components.
 - c. Shorcut Key Ctrl + T.
2. Pada tabulasi kontrols, matikan kotak periksa dari beberapa pilihan kontrol item yang akan dihilangkan dari toolbox dan klik tombol close

BAB III

PERENCANAAN DAN PEMBUATAN ALAT

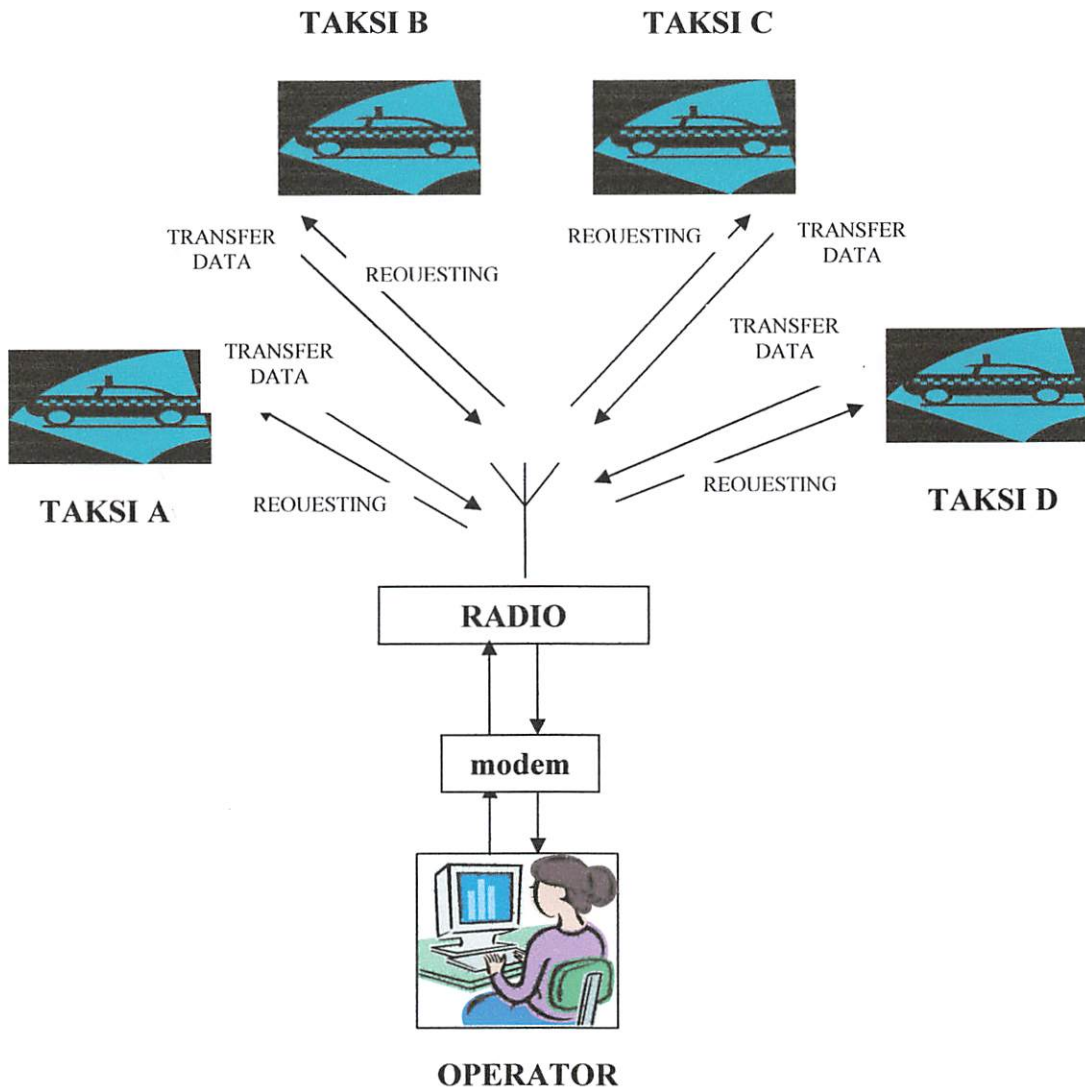
Dalam bab ini akan dijelaskan perencanaan dan pembuatan alat yang meliputi pembuatan perangkat keras dan perangkat lunak. Untuk memudahkan pemahaman pembuatan perangkat keras akan dimulai dengan menjelaskan secara blok diagram terlebih dahulu baru detail dari masing-masing peralatan.

3.1 Gambaran Umum Sistem.

Sistem yang dibuat adalah untuk diaplikasikan pada taksi agar taksi bisa melakukan lapanan setoran harian dimanapun asal masih dalam jangkauan radio komunikasi pada taksi kemudian akan dikirimkan ke PC (Personal Computer).

3.2 Blok Diagram

Berikut ini adalah gambar blok perancangan sistem secara keseluruhan :



Gambar 3-1. Block Diagram Sistem

Alat ini menggunakan sistem komunikasi tertutup dengan metode half duplex, untuk menjamin keamanannya, selain itu alat ini juga disertai ID yang berbeda untuk setiap taksi. Frekuensi receive dan transmit akan dibuat berbeda, pada taksi misalnya frekuensi receive-nya 150Hz dan transmit-nya 151Hz,

sedangkan pada operator frekuensinya merupakan kebalikan dari frekuensi yaitu 151Hz untuk receive dan 150Hz untuk transmitenya. Dengan demikian apabila operator transmits maka semua taksi akan bisa menerima, sedangkan apabila salah satu taksi transmits maka hanya operator yang bisa menerima. Laporan harian akan dilakukan jika ada permintaan atau requesting dari operator. Laporan harian ini bisa dilakukan dimana saja asalkan masih dalam jangkauan radio komunikasi pada taksi. Data yang diambil dari mikro pada argometer akan ditransferkan ke operator melalui radio komunikasi pada taksi. Data yang diambil dari mikro akan di modulasi oleh modem agar bisa dimodulasikan pada gelombang radio tersebut. Setelah data yang dimodulasi tadi sampai ke operator akan diubah kembali dengan menggunakan demodulator yang kemudian dimasukkan ke PC operator. Karena taksi tidak mungkin hanya satu maka setiap taksi diberikan address yang berbeda agar tidak terjadi kesalahan dalam penyusunan laporan harian.

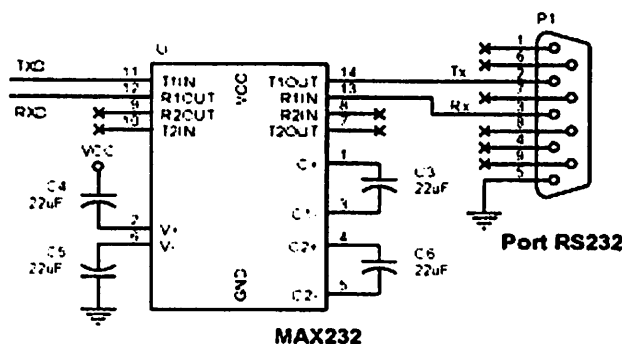
Fungsi masing-masing alat

1. PC operator: alat ini berfungsi untuk menampilkan secara penuh laporan harian taksi.
2. Modem (XR-2211 dan XR-2206) : Alat ini berfungsi sebagai pengubah data yang di ambil dari mikro pada argometer agar bisa di transferkan melalui gelombang radio atau sebaliknya
3. Radio paket: Alat ini berfungsi sebagai alat komunikasi para sopir taksi dengan para operator yang sekaligus merupakan alat yang digunakan sebagai sistem komunikasi yang digunakan untuk mentransfer data

4. Mikrokontroler AT89S8252 karena keunggulan alat ini yang mempunyai EEPROM maka digunakan sebagai penyimpan daftar harga yang nantinya akan ditransferkan ke operator.
5. Display LCD : berfungsi sebagai alat untuk menampilkan jumlah harga,waktu dan jarak yang ditempuh.

3.3 Rangkaian Inerface RS-232

Pada perencanaan hubungan antara komputer dengan modem adalah dipergunakan komunikasi data secara serial yaitu port 1 atau yang sering dikenal dengan COM 1. Adapun kaki atau pin-pin yang dipakai adalah pada pin no. 2 yang berfungsi untuk sambungan *receive data*, pin no. 3 untuk sambungan *transmit data* yang berguna sebagai input data pada modem FSK yang sebelumnya telah disesuaikan dulu level tegangannya dari RS-232 ke level tegangan TTL melalui sebuah IC MAX 232, dan pin no. 5 untuk *singal ground*. Rangkaian interface RS-232 diperlihatkan pada gambar 3.2.



Gambar 3-2. Rangkaian Interface RS-232

Data biner yang berasal dari komputer mempunyai level tegangan antara +3V sampai +15V dan -3V sampai -15V, sebelum masuk pada rangkaian modulator demodulator terlebih dahulu tegangannya melalui sebuah IC MAX 232 dan diubah menjadi tegangan TTL sebesar 0V sampai 5V yang sesuai dengan tegangan untuk mencatu kerja rangkaian modulator demodulator tersebut.

3.4 Perencanaan Perangkat Keras Modulator Demodulator

Sinyal digital pada komputer (data) yang akan dikirimkan atau ditransmisikan secara jarak jauh harus dimadulasikan dengan sinyal analog. Pada dasarnya ada tiga metode atau teknik untuk memodulasi data ke gelombang pembawa, yaitu ASK, FSK dan PSK. Dalam tugas akhir ini kami hanya membahas teknik modulasi dan demodulasi FSK

Modulasi FSK (*Frekuensi Shift Keying*) adalah modulasi yang menyatakan sinyal digital 1 sebagai nilai tegangan dengan frekuensi tertentu (misalnya 1200Hz) sementara sinyal digital 0 dinyatakan sebagai suatu nilai tegangan dengan frekuensi tertentu yang berbeda (misalnya 2200Hz). Sistem FSK ini sangat berguna dan menguntungkan karena pengaruh desah dan interfensi sangatlah kecil.

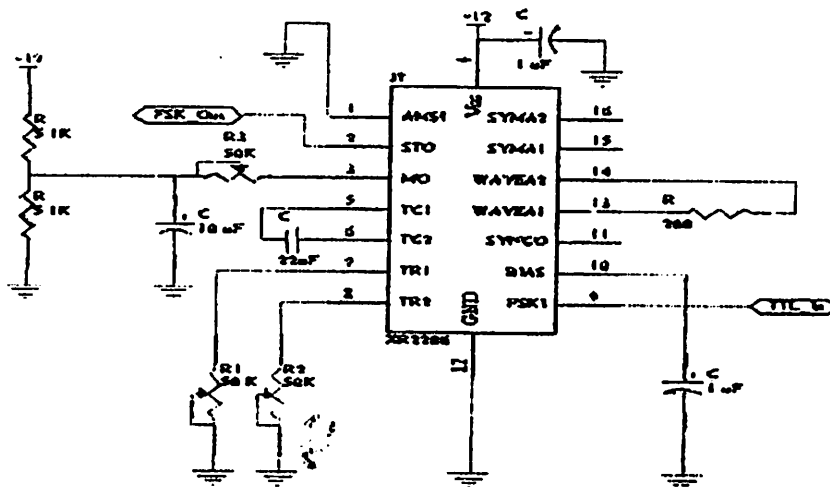
3.4.1 XR-2206 (Modulator FSK)

Rangkaian untuk membangkitkan FSK ditunjukkan dalam gambar 3.3. XR-2206 yang diaplikasikan sebagai FSK generator dengan kecepatan 1200bps menggunakan frekuensi *mark*1200Hz dan *space* 2200Hz dapat bekerja dengan

dua buah *timing resistor* R1 dan R2 yang dihubungkan pada pin 7 dan pin 8, dan ditentukan oleh pemilihan kapasitor eksternal yang dihubungkan antara pin 5 dan pin 6. *Timing resistor* ini bekerja bergantian sesuai dengan level tegangan pada pin 9. jika pin 9 diberi tegangan bias ≥ 2 V (logika 1), maka hanya R1 yang bekerja. Sebaliknya jika pin 9 diberi tegangan ≤ 1 V (logika 0), maka hanya R2 yang bekerja. Sehingga frekuensi keluaran (pin no.2) berubah-ubah diantara dua frekuensi f1 dan f2. Besarnya f1 dan f2 dapat ditentukan dengan persamaan :

$$f_1 = 1/(R_1.C),$$

$$f_2 = 1/(R_2.C)$$



Gambar 3-3. Komponen modulator XR-2206

Frekuensi osilasi f_0 , ditentukan oleh timing kapasitor yang terhubung dengan pin 5 dan pin 6 serta oleh timing resistor R1 dan R2 yang terhubung dengan pin 7 dan pin 8, dengan ketentuan

$$f_0 = 1/RC \text{ Hz}$$

Mempertimbangkan nilai R yang disarankan antara $4\text{ K}\Omega - 20\text{ K}\Omega$, diinginkan agar nilai timing resistor R1 dan R2 dengan frekuensi (*mark*) pada $f_1 = 1200\text{ Hz}$ dan biner 0 (*space*) pada $f_2 = 2200\text{ Hz}$ dalam jangkauan $10\text{ k}\Omega$ sampai $50\text{ k}\Omega$. Nilai kapasitor C diperoleh setelah memasukkan nilai-nilai variable yang telah diketahui yaitu R1, R2, dan f dengan mempertimbangkan nilai komponen kapasitor yang disarankan pada datasheet dan nilai komponen standart.

Adapun perhitungan untuk menentukan nilai komponen eksternal dari modulator FSK sebagai berikut:

Untuk nilai $R_1 = 50\text{ K}\Omega$ dan $f_1 = 1200\text{ Hz}$

$$f_1 = \frac{1}{R_1 \cdot C}$$

$$C = \frac{1}{f_1 \cdot R_1} = \frac{1}{1200 \cdot 50000}$$

$$= 1,66666666 \cdot 10^{-8} \text{ Farad} = 16 \text{ nF}$$

Setelah memperoleh komponen C dengan $f_2 = 2200\text{ Hz}$ dapat menentukan nilai R2 sebagai berikut

$$R_2 = \frac{1}{f_2 \cdot C}$$

$$= \frac{1}{2200 \cdot 16\text{ nF}}$$

$$= 27272,7 \Omega$$

Hasil perhitungan dapat diperlihatkan dalam table perhitungan nilai komponen eksternal pada table 3-1 berikut

Tabel 3-1. Hasil perhitungan Nilai Komponen Eksternal XR-2206 Untuk $f_1=1200\text{Hz}$ dan $f_2=2200\text{Hz}$

R1	R2	C	Nilai komponen yang digunakan
50000ohm	27272,7ohm	16666666869316E-8 Farad	16 nF
47500ohm	25909,1ohm	175438596983213E-8 Farad	17 nF
45000ohm	14545,5ohm	185185182743908E-8 Farad	18 nF
42500ohm	23181,8ohm	196078424608004E-8 Farad	19 nF
40000ohm	21818,2ohm	208333332807342E-8 Farad	20 nF
37500ohm	20454,5ohm	202222222845403E-8 Farad	22 nF
35000ohm	19090,9ohm	2380952324188E-8 Farad	23 nF
32500ohm	17727,3ohm	256410253030026E-8 Farad	25 nF
30000ohm	16363,6ohm	277777782997646E-8 Farad	27 nF
27500ohm	15000,0ohm	303030311954444E-8 Farad	30 nF
25000ohm	16363,6ohm	33333332538632E-8 Farad	33 nF
22500ohm	12292,9ohm	370370365487815E-8 Farad	37 nF
20000ohm	10909,1ohm	416666665614684E-8 Farad	41 nF

Dari hasil simulasi perhitungan diatas, digunakan nilai timing kapasitor C sebesar 22 nF, karena merupakan nilai standart dan umum dipakai dipasaran. Sedangkan nilai R1 dan R2 yang berada pada jangkauan $10\text{k}\Omega$ sampai $50\text{k}\Omega$ digunakan komponen variable resistor $10\text{k}\Omega$ dan $50\text{k}\Omega$.

3.4.2 XR-2211 (Demodulator FSK)

Rangkaian demodulator berfungsi mengubah sinyal FSK yang diterima walky talky menjadi data biner. Untuk mendemodulasikan sinyal FSK tersebut digunakan IC XR-2211. XR-2211 adalah sebuah IC *monolithic phase locked loop* yang dirancang untuk komunikasi data khususnya aplikasi modem FSK.

Demodulator FSK dirancang untuk mendemodulasi sinyal FSK dengan frekuensi biner 1 (*mark*) 1200 Hz dan biner 0 (*space*) 2200 Hz dengan kecepatan 1200bps. Untuk mendemodulasi sinyal FSK dengan frekuensi tersebut maka pemilihan nilai-nilai komponen eksternal sntsr lain:Ro,R1,Co,C1,Cf.

Adapun perhitungan untuk sistem demodulator yang akan dibuat dikemukakan dalam perhitungan berikut:

10. Menentukan PLL counter frekuensi

$$\begin{aligned} F_o &= \sqrt{f_1 \cdot f_2} \\ &= \sqrt{1200 \cdot 2200} \\ &= 1624\text{Hz} \end{aligned}$$

11. Menghitung timing resistor dengan Ro = 10k dan VR Rx = 10k

$$\begin{aligned} R_o &= R_o + \frac{R_x}{2} \\ &= 10 + \frac{10}{2} \\ &= 15000 \text{ ohm} \end{aligned}$$

12. Menghitung nilai Co

$$\begin{aligned} C_o &= \frac{1}{R_o \cdot C_o} \\ &= \frac{1}{15000 \cdot 1624} \\ &= 39 \text{ nF} \end{aligned}$$

13. Menghitung nilai R1

$$\begin{aligned}
 R1 &= \frac{Ro \cdot fo}{(f1 - f2)^2} \\
 &= \frac{15000 \cdot 1624}{(1200 - 2200)^2} \\
 &= 48720 \\
 &= 47 \text{ K}\Omega
 \end{aligned}$$

14. menghitung nilai C1

$$\begin{aligned}
 C1 &= \frac{1250 \cdot Co}{R1 \cdot f^2} \\
 &= \frac{1250 \cdot 39 \text{ nF}}{47000 \cdot 0,5^2} \\
 &= 4,1 \cdot 10^{-9} = 3,9 \text{ nF}
 \end{aligned}$$

15. Menghitung nilai Rf (paling sedikit 5 kali nilai R1)

$$\begin{aligned}
 Rf &= R1 \cdot 5 \\
 &= 47000 \cdot 5 \\
 &= 235000 \\
 &= 240 \text{ K}\Omega
 \end{aligned}$$

16. Menghitung nilai Rb (nilainya paling sedikit 5 kali nilai Rf)

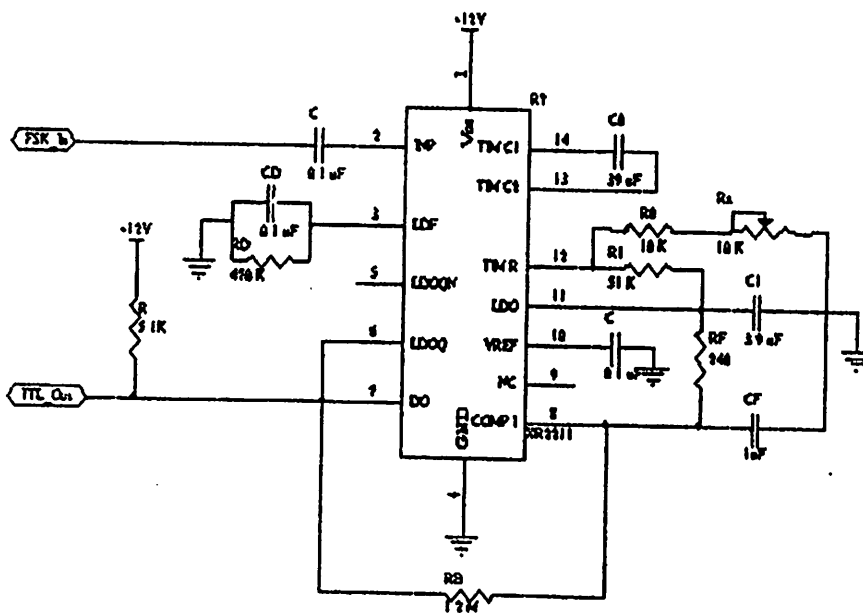
$$\begin{aligned}
 Rb &= Rf \cdot 5 \\
 &= 240000 \cdot 5 \\
 &= 1,2 \text{ M}\Omega
 \end{aligned}$$

17. Menghitung Rsum

$$\begin{aligned}
 R_{sum} &= \frac{(R_f + R_I) \cdot R_b}{(R_f + R_I + R_b)} \\
 &= \frac{(24000 + 47000)1200000}{24000 + 47000 + 1200000} \\
 &= 231607 \Omega
 \end{aligned}$$

18. Menghitung nilai Cr

$$\begin{aligned}
 C_r &= \frac{0,25}{(R_{sum} \cdot Boudrate)} \\
 &= \frac{0,25}{231607 \cdot 1200} = 8,99 \cdot 10^{-10} = 1 \text{ nF}
 \end{aligned}$$



Gambar 3-4. Komponen Demodulator XR-2211

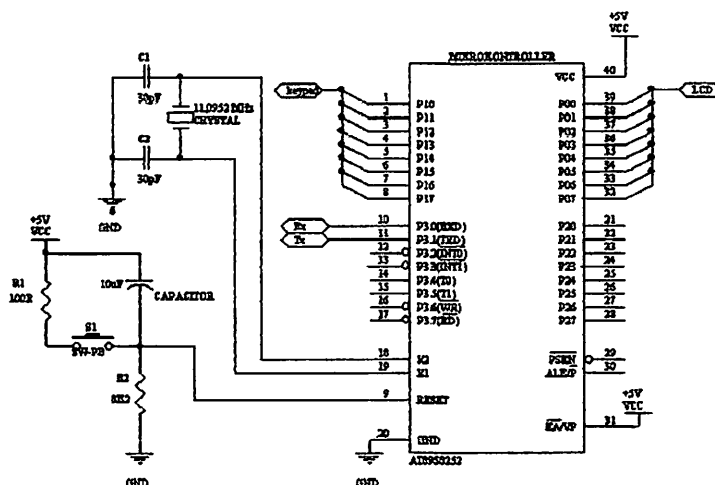
Pada gambar 3-4. di atas pin no. 2 (*FSK Input*) pada IC XR-2211 merupakan sinyal masukan demodulator yang berasal dari sinyal keluaran HT (*speaker*) dimana pada pin ini sinyal berupa sinyal FSK, dan pin no. 7 (*Data Output*) merupakan sinyal keluaran digital, disini mengalami proses demodulasi (data biner) yang dihubungkan pada komputer atau minimum sistem.

3.5 Perancangan Sistem Mikrokontroler

Sistem mikrokontroler terdiri atas mikrokontroler dan komponen-komponen pendukung agar sistem dapat bekerja dengan optimal.

3.5.1 Mikrokontroler 89S8252

Mikrokontroler 89S8252 harus didukung oleh beberapa rangkaian lain agar dapat melakukan prosesnya, yaitu berupa rangkaian clock dan reset. Selain itu juga harus ditentukan penggunaan port-portnya dan sinyal-sinyal yang digunakan untuk mendukung proses yang akan dilakukan.



Gambar 3-5. Skema Rangkaian Minimum Sistem

Mikrokontroler 89S8252 memiliki rangkaian osilator internal yang dapat digunakan sebagai sumber clock bagi CPU. Osilator internal dirancang dengan dua buah kapasitor dan satu kristal, sesuai dengan spesifikasi AT89S8252. Gambar 3.5 menunjukkan rangkaian mikrokontroler dengan osilator internal.

Rangkaian *power-on reset* dipergunakan untuk mereset mikrokontroler secara otomatis setiap awal catu daya dihidupkan. Saat catu daya diaktifkan, rangkaian reset akan menahan logika tinggi dari pin RST dengan jangka waktu tertentu hingga kapasitor terisi muatan hingga jenuh. Saat kapasitor jenuh, pin RST akan berlogika rendah, dan mikrokontroler telah mengalami proses reset.

3.5.2 Pembagian port

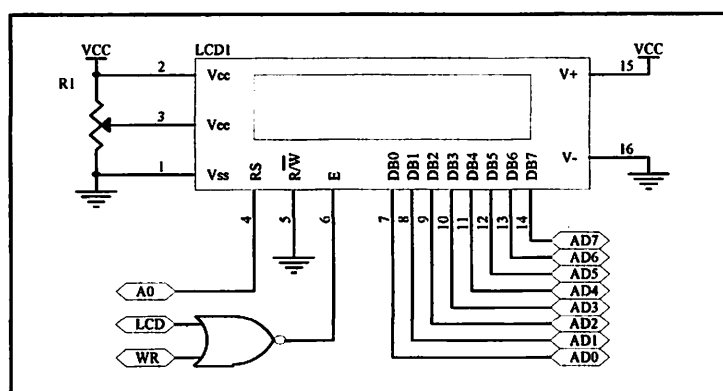
Dalam sistem mikrokontroler 89S8252 ini direncanakan menggunakan port-port yang tersedia. Port 0 digunakan untuk saluran data dan alamat bagian rendah yang dimultiplek (AD0-AD7), dan alamat bagian tinggi dikeluarkan pada port 2 (A8-A15). Karena menggunakan komunikasi serial pada sistem mikrokontrolernya maka beberapa bit port 3 digunakan sebagai pembangkit sinyal kontrol (TxD, RxD, RD dan WR).

3.6 LCD

Pada sistem yang direncanakan akan digunakan LCD (Liquid Crystal Display) sebagai tampilan. LCD yang digunakan adalah jenis TM1632 yang merupakan LCD dua baris dengan tiap barisnya terdiri dari 16 karakter.

LCD ini membutuhkan 3 sinyal kontrol, R/W (*read/write*) untuk menentukan apakah data akan dibaca atau ditulis, E (*Enable*) yang merupakan sinyal untuk meng-enable-kan dan RS (*Register Select*) untuk memilih register yang diakses. LCD TM1632 memiliki 2 register yaitu register data dan register instruksi.

Pin R/W dihubungkan ke *ground* atau selalu berlogika 0 karena dalam perancangan. LCD ini hanya selalu dalam operasi tulis dan pin RS dihubungkan ke pin A0 sistem mikrokontroler. Pengaktifan LCD ini selanjutnya tergantung pada pin E. Dimana pin E ini tergantung dari CS5 dari address dekoder dan perintah write mikrokontroler. Rangkaian LCD seperti terlihat dalam gambar 3.7

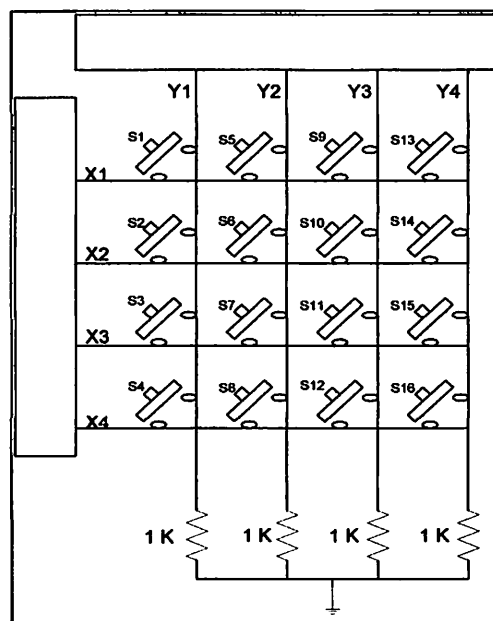


Gambar 3-6. Rangkaian LCD

3.7 Papan Tombol (*Keypad*)

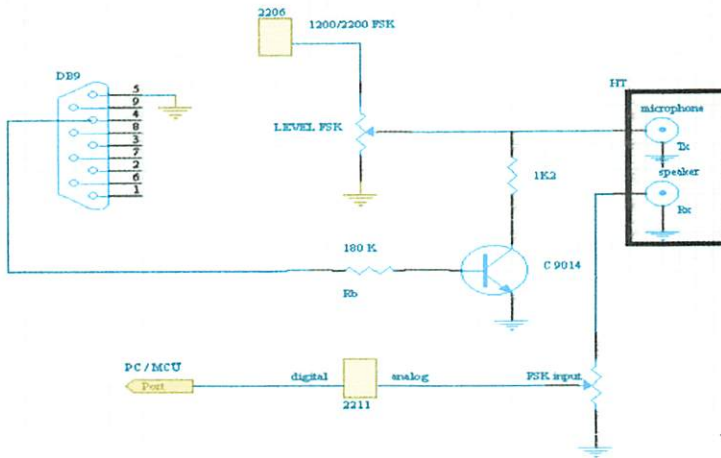
Papan tombol ini digunakan untuk memasukkan data referensi dan mengubah data bila diinginkan. Untuk menterjemahkan informasi yang diterima dari papan tombol, maka *keypad* dihubungkan dengan *port 1*.

Papan tombol tersebut mempunyai matrik 4 baris dan 4 kolom. Deretan baris dan kolom dari papan tombol dihubungkan dengan *port 1* yang difungsikan sebagai masukan dan keluaran. Deretan kolom dihubungkan dengan *ground* (berlogika 0) dan *port 1* (P14-P16) yang difungsikan sebagai *input* mikrokontroler. Sedangkan deretan baris dihubungkan ke *port 1* (P10-P13) yang telah diberi data 0001 dan secara kontinyu data tersebut bergeser satu bit ke kiri. Pergeseran data satu bit ini dimaksudkan untuk menentukan posisi tombol yang ditekan dalam satu kolom. *Port* ini difungsikan sebagai *output* dari mikrokontroler. Dengan demikian kalau tombol tidak ditekan maka masukan *port 1* (P14-P16) di pin yang terhubung tombol tersebut berlogika 0 dan bila tombol ditekan akan berlogika 1.



Gambar 3-7. Rangkaian Keypad

3.8 Koneksi antara modem dengan radio



Gambar 3-8. Rangkaian koneksi modem dengan radio

Transistor berfungsi sebagai saklar yang digunakan untuk memberikan logika high (untuk mengaktifkan PTT dalam proses transmits data) dan low (PTT tidak aktif). Dengan menggunakan transistor NPN 9014 telah cukup untuk menjalankan fungsi saklar pada rangkaian ini. Selain itu transistor 9014 ini harganya murah tetapi dilengkapi dengan mutu yang cukup handal. Ditentukan $V_{cc} = 12$ volt dan R_c yang digunakan 1,2 Kohm, pada rangkaian ini menggunakan resistansi yang kecil agar nilai I_c yang besar agar dapat arus basis pada transistor.

$$I_c = \frac{V_{cc} - V_{ce}}{R_c} = \frac{12 - 0}{1.2K} = 10 \text{ mA}$$

$B_{dc} = 150$ (dari data sheet)

$$\text{Maka } I_b \text{ bisa dicari: } I_b = \frac{I_c}{\beta_{dc}} = \frac{10\text{mA}}{150} = 66.66\mu\text{A}$$

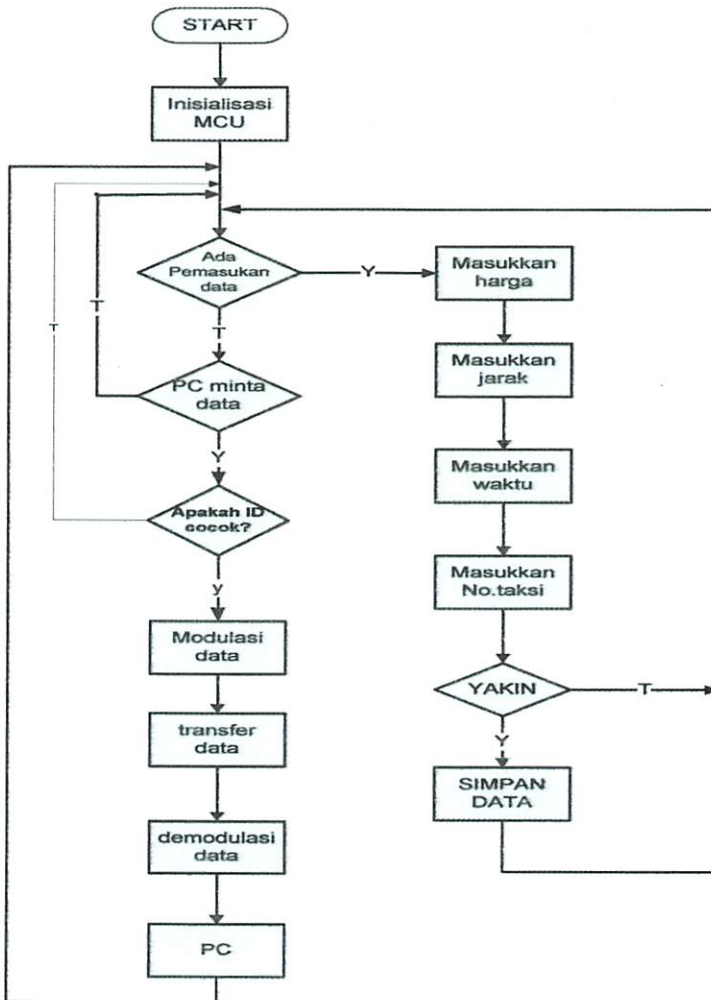
Maka R_b yang digunakan

$$R_b = \frac{V_{cc} - V_{be}}{I_b} = \frac{12 - 0,7}{66,66\mu\text{A}} = 169,5 \text{ K}\Omega$$

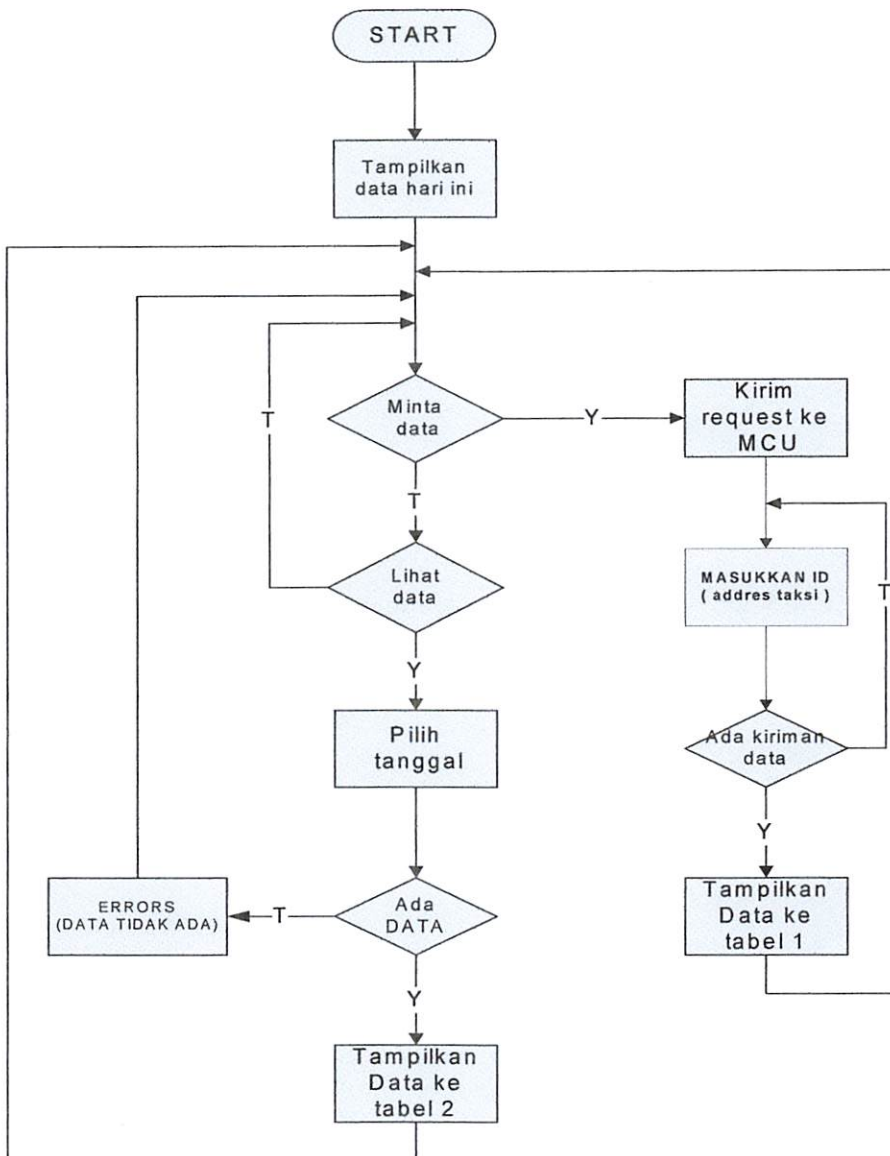
Karena nilai tahanan 169,5 K tidak ada dipasaran maka dapat diganti dengan nilai yang terdekat yaitu 180 K Ω .

3.9 Perencanaan Perangkat lunak

Karena menggunakan mikrokontroller AT89S8252 maka untuk mengontrol prosesnya menggunakan bahasa pemrograman assembly, sedangkan pada pc menggunakan visual basic. Oleh karena itu diperlukan urutan-urutan kerja yang digambarkan pada flowchat dibawah ini



Gambar 3-9. flowchart pada mikrokontroller



Gambar 3-10. flowchart pada PC menggunakan visual basic 6. 0

BAB IV

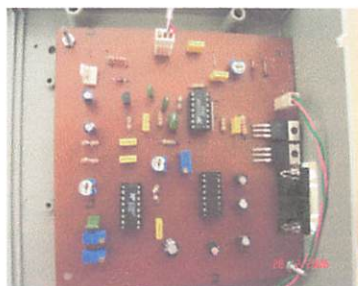
PENGUJIAN DAN ANALISIS

4.1 Tujuan

Bab ini membahas tentang pengujian dan analisis alat yang telah dibuat. Secara umum, pengujian ini bertujuan untuk mengetahui apakah alat yang telah direalisasikan dapat bekerja sesuai dengan spesifikasi perencanaan yang telah ditetapkan. Pengujian alat ini meliputi pengujian perangkat keras dan perangkat lunak. Pengujian dilakukan pada masing-masing blok terlebih dahulu, yang selanjutnya dilakukan pengujian untuk sistem secara keseluruhan.



Gambar 4-1. Gambar alat pada taksi



Gambar 4-2. Gambar alat pada operator

4.2 Pengujian Sistem Mikrokontroller.

➤ Tujuan

Untuk mengetahui kondisi awal dari mikrokontroler apakah sudah sesuai dengan yang direncanakan

➤ Prosedur Pengujian

1. Membuat program yang digunakan dalam pengujian mikrokontroler.

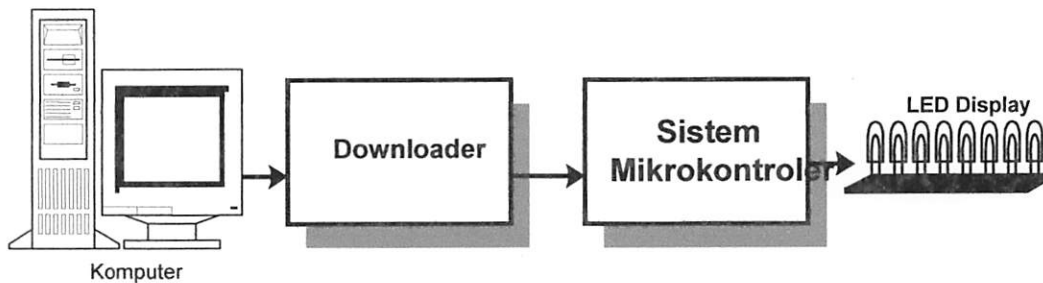
Program yang digunakan dalam pengujian mikrokontroler ini merupakan program sederhana yang meletakkan 0F_H dan F0_H pada ACC secara bergantian kemudian memindahkannya pada *Port 1* AT89S8252. Program yang dibuat adalah sebagai berikut :

```

                ORG 0000H
                JMP     START
START:         MOV     A,#0FH
                MOV     P1,A
                CALL   TUNDA
                MOV     A,#F0H
                MOV     P1,A
                JMP     START
TUNDA:        MOV     R3,#0FFH
TUNDA1:       MOV     R2,#0FFH
                DJNZ   R2,$
                MOV     R1,#0FH
                DJNZ   R1,$
                DJNZ   R3,TUNDA1
                RET
                END

```


2. Rangkaian dibuat seperti Gambar 4-3.
3. Memasang catu daya rangkaian sebesar 5 Volt DC
4. Download program diatas .
5. Mengamati keluaran pada LED Display .



Gambar 4-3. Diagram blok Pengujian Mikrokontroler

➤ Hasil Pengujian

Hasil pengujian pada sistem mikrokontroller ditunjukkan dalam Tabel 4.1 dibawah ini :

Tabel 4.1 Hasil Pengujian Sistem Mikrokontroler

Kondisi	Keluaran pada LED Display							
	Bit 0	Bit 1	Bit 2	Bit 3	Bit 4	Bit 5	Bit 6	Bit 7
Satu	0	0	0	0	1	1	1	1
Dua	1	1	1	1	0	0	0	0

➤ **Analisis Pengujian**

Dari hasil pengujian dalam tabel 4-1 dapat dilihat bahwa *port 1* memberikan logika $0F_H$ dan $F0_H$ secara bergantian sesuai dengan isi program.

4.3 Pengujian Komunikasi Serial

➤ **Tujuan**

Untuk mengetahui apakah data yang dikirim dari MCU ke *PC* dapat diterima dengan benar dengan melakukan simulasi pada komputer.

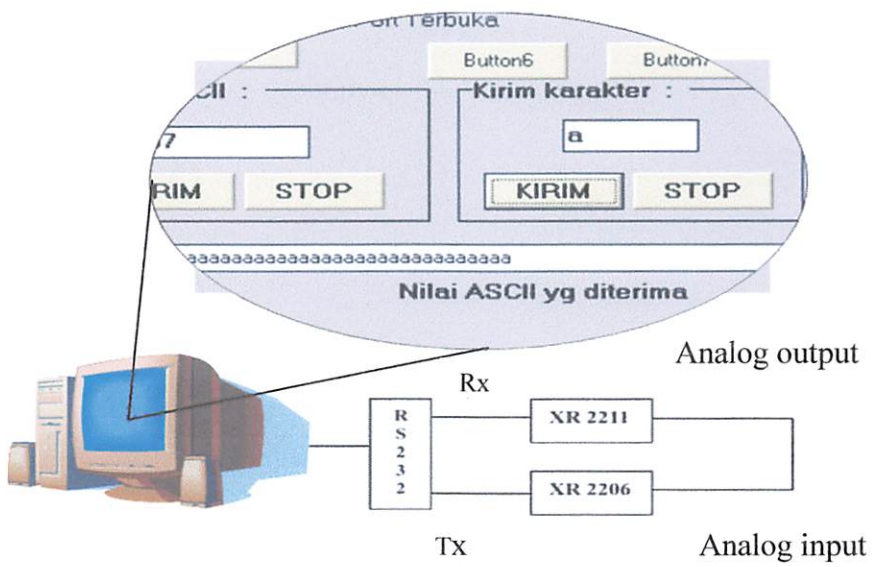
➤ **Peralatan yang digunakan**

- Komputer
- Rangkaian modem (XR 2211 dan XR2206)
- Frekuensi counter
- Catu daya 12 Volt DC
- Sistem mikrokontroller dengan antarmuka RS232.

a. Pengujian Rangkaian modem (XR 2211 dan XR2206)

➤ **Prosedur pengujian**

- 1 Menyusun rangkaian modem seperti pada gambar 4-4



Gambar 4-4. Rangkaian Pengujian modem

2. Mengaktifkan catu daya
3. Menyetel frekuensi mark (high) dengan frekuensi counter sampai pada 1200 Hz



Gambar 4-5. Tampilan frekuensi FSK pada logika high (mark)

3. Menyetel frekuensi space (low) dengan frekuensi counter pada frekuensi 2200 Hz



Gambar 4-6. Tampilan frekuensi FSK pada logika low(space)

b. Pengujian Sistem mikrokontroller dengan antarmuka RS232.

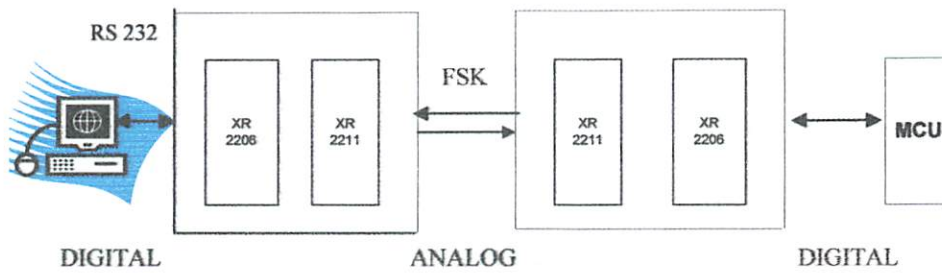
➤ **Prosedur pengujian**

Menyusun rangkaian seperti pada Gambar 4-7

Membuat program transfer data pada sistem mikrokontroller seperti yang ditunjukkan dalam program berikut. Dengan program tersebut komputer mengirim data '1234567890' ke alat dan oleh alat akan dikembalikan lagi ke komputer.

Download program ke Mikrokontroler dan eksekusi program.

Mencatat hasil yang terlihat dalam layar komputer.



Gambar 4-7. Rangkaian Pengujian Transfer Data

➤ Program Uji Komunikasi Data dari Mikrokontroler

```

B2400 EQU 232
MULAI: CALL INIT232
      CALL SERIAL
      JMP MULAI
PCON EQU 87H
      ORG 0000H
      JMP MULAI
      ORG 0023H
SERIAL: JBC TI, OUT232
      PUSH ACC
      MOV A, SBUF
      MOV SBUF, A
      POP ACC
OUT232: CLR TI
      CLR RI
      RETI
INIT232: MOV TH1, #B1200
      MOV TMOD, #22H
      ANL PCON, #7FH
      MOV SCON, #50H
      SETB PS
      SETB ES

```

Cuplikan program uji komunikasi data di komputer menggunakan program VB 6.0

MSComm1.Output = '1234567890'

Text1.Text = MSComm1.Input

➤ **Hasil Pengujian**

Hasil pengujian transfer data serial ini ditunjukkan Tabel 4 -2 dibawah ini:

Tabel 4-2. Hasil Pengujian Transfer Data Serial

Data yang dikirim komputer	Data yang diterima komputer
1234567890	1234567890

Hasil pengujian dalam Tabel 4-2. menunjukkan bahwa proses pengiriman data serial dengan menggunakan RS 232 ke alat telah benar.

4.4 Pengujian Rangkaian Keypad

➤ **Tujuan**

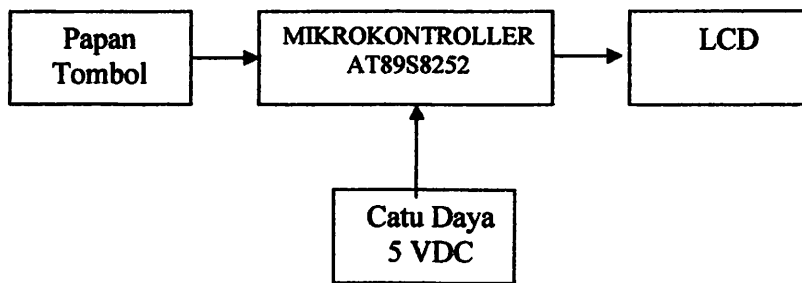
Untuk mengetahui apakah rangkaian ini dapat bekerja dengan baik agar alat yang direncanakan berjalan sesuai dengan yang diharapkan

➤ **Peralatan yang digunakan**

- ◆ Papan Tombol (keypad 4x4)
- ◆ MCU
- ◆ LCD
- ◆ Catu daya 5 Volt DC

➤ **Prosedur Pengujian**

1. Peralatan dirangkai seperti pada gambar 4-8
2. Menekan tombol pada papan tombol, mengamati dan mencatat keluaran yang ditampilkan ke LCD



Gambar 4-8. Diagram blok pengujian pengkode papan tombol (keypad)

3. Memasukkan program seperti dibawah ini pada mikro

Keypad4x4:

```

    Mov  keybounc,#100
    Mov  keyport,#0FFh
    Clr  kolom1      ;
;-----
ull:
    Jb  baris1,key1
    ;Djnz keybounc,$
    Mov  keydata,#'1'
    Ret
key1:
    Jb  baris2,key2
    ; Djnz keybounc,$
    Mov  keydata,#'4'
    Ret
key2:
    Jb  baris3,key3
    ; Djnz keybounc,$
    Mov  keydata,#'7'
    Ret
key3:
    Jb  baris4,key4
    ; Djnz keybounc,$
    Mov  keydata,#'e'
    Ret
;-----
key4:
    Setb kolom1
    Clr  kolom2
;-----
    Jb  baris1,key5
    ; Djnz keybounc,$
    Mov  keydata,#'2'
    Ret
  
```

```

key5:
  Jb  baris2,key6
;   Djnz keybounc,$
    Mov  keydata,#'5'
    Ret
key6:
  Jb  baris3,key7
;   Djnz keybounc,$
    Mov  keydata,#'8'
    Ret
key7:
  Jb  baris4,key8
;   Djnz keybounc,$
    Mov  keydata,#'0'
    Ret
;-----
key8:
  Setb kolom2
  Clr  kolom3
;-----
  Jb  baris1,key9
;   Djnz keybounc,$
    Mov  keydata,#'3'
    Ret
key9:
  Jb  baris2,key10
;   Djnz keybounc,$
    Mov  keydata,#'6'
    Ret
key10:
  Jb  baris3,key11
;   Djnz keybounc,$
    Mov  keydata,#'9'
    Ret
key11:
  Jb  baris4,key12
;   Djnz keybounc,$
    Mov  keydata,#'#'
    Ret
key12:
  Mov  keydata,#0FFh

```

➤ Hasil pengujian dan analisis

Hasil pengujian dan pengamatan rangkaian keypad ditunjukkan dalam tabel 4-3

Tabel 4-3. Hasil pengujian papan tombol (keypad)

Tombol	Tampilan LCD
0	0
1	1
2	2
3	3
4	4
5	5
6	6
7	7
8	8
9	9
*	*
#	#

Berdasarkan hasil pengujian yang diperlihatkan pada tabel 4.3 maka keypad dapat menghasilkan data biner yang berbeda untuk masing-masing tombol. Dengan demikian maka keypad dapat bekerja dengan baik sesuai perencanaan.

4.5 Pengujian Rangkaian LCD

Pengujian rangkaian LCD dilakukan dengan cara merangkainya seperti gambar dibawah kemudian dihubungkan ke rangkaian AT89S8252. Peralatan yang dibutuhkan adalah sebagai berikut:

- LCD M1632
- IC Mikrokontroler AT89S8252
- Supply +5 Volt

Dengan menggunakan Listing Program dibawah ini, bisa diketahui hasil dari pengujian rangkaian LCD.

Listing Program

```

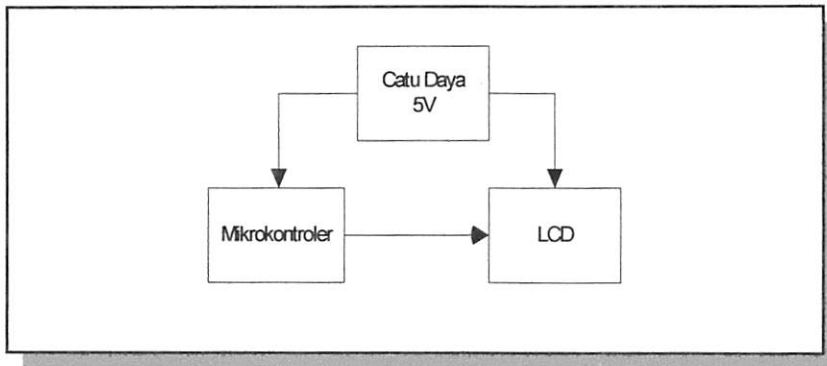
-----
;Program Demo untuk menjalankan LCD 16 x 2
;      Oleh: chairil iskandar
-----
;
;      org      0h
;      nop
;      ljmp     mulai
;
write_inst:
;      mov      P1,#0h ;untuk memuliskan
;      mov      P0,R1 ;intruksi ke LCD
;      setb     P1.1 ;module
;      clr      P1.1
;      acall    delay
;      ret
;
write_data:
;      mov      P1,#01 ;untuk menuliskan
;      mov      P0,R1 ;data ke LCD
;      setb     P1.1 ;module
;      clr      P1.1
;      acall    delay
;      ret
;
delay: mov      R0,#0
delay1: mov     R5,#50h
;      djnz     R5,$
;      djnz     R0,delay1
;      ret
;
Ldelay: mov     R2,#030h
Ld1:   acall    delay
;      djnz     R2,Ld1
;      ret
;
tulis: mov      R4,#3
;      mov      DPTR,#tampil
barisa: mov     R3,#16
;      mov      R1,#80h

```

```

        acall write_inst
tulisl: clr    A
        movc  A,@A+DPTR
        mov  R1,A
        Inc  DPTR
        acall write_data
        djnz R3,Tulis1
;
barisb: mov  R3,#16
        mov  R1,#0C0h
        acall write_inst
tulis2: clr    A
        movc  A,@A+DPTR
        mov  R1,A
        Inc  DPTR
        acall write_data
        djnz R3,Tulis2
        acall Ldelay
        djnz R4,barisa
        ret
;
mulai:  mov  R1,#03Fh
        acall write_inst
        acall write_inst
        mov  R1,#0Dh
        acall write_inst
        mov  R1,#06h
        acall write_inst
        mov  R1,#01h
        acall write_inst
        mov  R1,#0Ch
        acall write_inst
        acall tulis
        sjmp mulai
;
tampil: DB  ' CHAIRIL ISKANDAR '
        DB  ' - 0117080 - '
;
        End

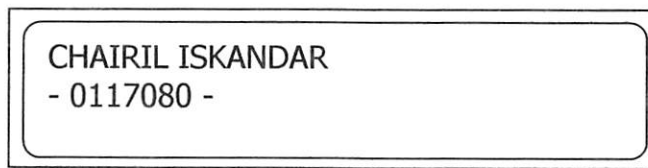
```



Gambar 4-9. BLOK DIAGRAM PENGUJIAN LCD

➤ Analisis Hasil Pengujian

Dengan program diatas maka LCD akan menampilkan seperti gambar dibawah ini:



Gambar 4-10. Hasil Pengujian LCD

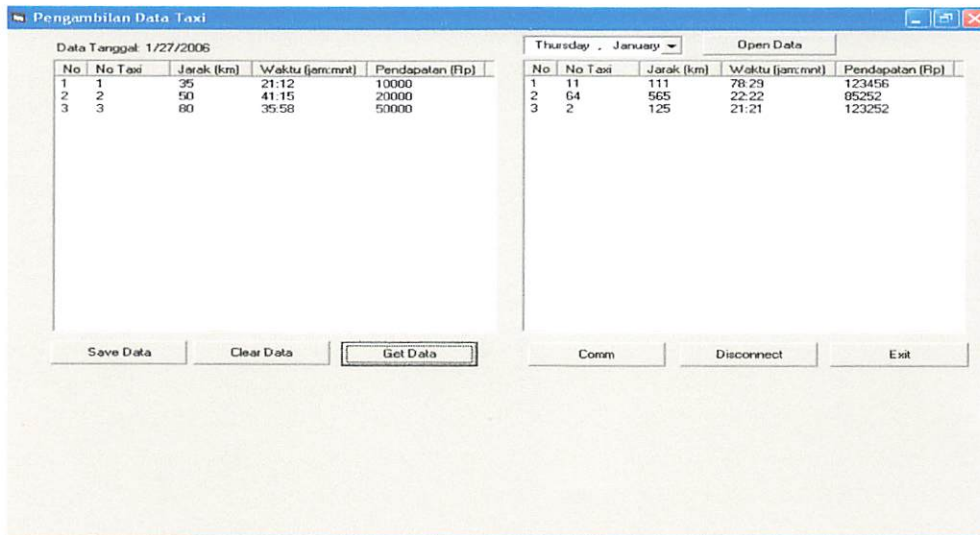
4.6 Pengujian Secara Keseluruhan

Pengujian ini dapat dilakukan setelah semua tahap pengujian perbagian telah dilakukan dengan baik. Adapun prosedur pengujian secara keseluruhan dapat dijelaskan sebagai berikut:

1. Pasang semua piranti perangkat keras.
2. Nyalakan piranti pada bagian taxi.

3. Masukkan data-data yang diperlukan melalui keypad. Data meliputi pendapatan, jarak tempuh, waktu operasi, dan nomor lambung taxi.
4. Buka program aplikasi di komputer.
5. Lakukan seting pada port serial.
6. Ambil data
7. Simpan data.

Jika semua langkah telah dilakukan dan tidak terdapat kesalahan maka pengujian secara keseluruhan telah dapat dilakukan dengan baik.



Gambar 4-11. Tampilan Interfacing pada komputer

BAB V

KESIMPULAN

5.1 KESIMPULAN

Kesimpulan yang dapat diambil dari perancangan dan pembuatan alat ini ialah:

- a) Transfer data ke kantor operator taksi lebih cepat
- b) Laporan setoran harian tidak terbatas jarak dan waktu karena melalui gelombang radio
- c) Jarak jangkauan tergantung pada jenis dan bentuk antenna dan daya RF masing-masing stasiun radio.
- d) Konsumsi daya yang diserap oleh peralatan yang ada ditaksi hanya berkisar 8 watt, dan tegangan catu sesuai dengan tegangan catu daya yang ada di mobil taksi.

5.2 Saran

Untuk selanjutnya diharapkan adanya perkembangan yang signifikan selain dilengkapi oleh perhitungan harga, juga dilengkapi oleh perhitungan mekanik roda.

DAFTAR PUSTAKA


1. *Data Sheet*
2. Abdul Yadi, *Aplikasi Visual Basic dalam Industri Manufaktur*, PT Elex Media Komputindo, 2000
3. Ario Suryo Kusumo, *Buku Latihan Microsoft Visual Basic 6.0*, PT Elex Media Komputindo, 2000
4. Wiryanto Dewobroto, *Aplikasi Sain dan Teknik Dengan Visual Basic 6.0*. PT Elex Media Komputindo, 2002
5. <http://www.exar.com>
6. Moh. Ibnu Malik, ST, *Belajar Mikrokontroller AT89S8252*, Gaya Media , Edisi Pertama, 2003
7. Eko Putra, Agfianto, 2002, *Belajar Mikrokontroler AT89C51/52/55*, Yogyakarta, Gramedia
8. <http://www.google.com/>
9. <http://www.maxim-ic.com.pdf>

LAMPIRAN



LEMBAR BIMBINGAN SKRIPSI

Nama : Chairil Iskandar
NIM : 01.17.080
Jurusan : Teknik Elektro S-1
Konsentrasi : Teknik Elektronika
Judul Skripsi : Perencanaan dan Pembuatan Alat Pentransfer
Data Argometer Taksi Berbasis Mikrokontroller
AT89S8252 Yang Bisa Diupload Kekomputer
Melalui Komunikasi Radio

Tanggal Pengajuan Skripsi : 9 Desember 2005
Selesai Penulisan Skripsi : 20 Maret 2006
Dosen Pembimbing : Ir. Sidik Noertjahjono, MT
Telah Dievaluasi Dengan Nilai : 85 (Delapan Puluh Lima) 

Mengetahui,
Ketua Jurusan Teknik Elektro S-1

(Ir. F. Yudi Limpraptono, MT)
NIP.Y 1039500274

Diperiksa dan Disetujui,
Dosen Pembimbing

(Ir. Sidik Noertjahjono, MT)
NIP.Y .1028700167



INSTITUT TEKNOLOGI NASIONAL
FAKULTAS TEKNOLOGI INDUSTRI
JURUSAN TEKNIK ELEKTRO

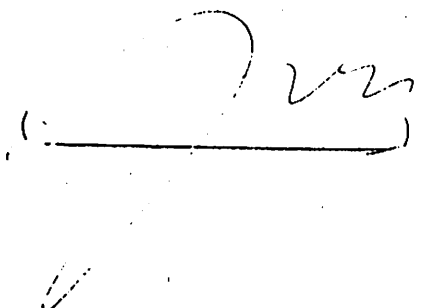
Formulir Perbaikan Ujian Skripsi

Dalam pelaksanaan Ujian Skripsi Janjang Strata 1 Jurusan Teknik Elektro Konsentrasi T. Energi Listrik / T. Elektronika, maka perlu adanya perbaikan skripsi untuk mahasiswa :

NAMA : CHINIL ISKANDAR
NIM : 01.17.080
Perbaikan meliputi :

- 1) MANU. RESET
 - 2) - KONEKSI MODUL
- BAH III
- 1) PENBUJIAN MILAR
 - 2) MANU. LENCUR DIPERJELAS
 - 3) Gambar 4-7
 - 4) PENBUJIAN WYPAD
 - 5) SOFTWAR & DEMONSTRASI LCD
 - 6) SUMBER BAH II

Malang,





FORMULIR PERBAIKAN SKRIPSI

Nama : Chairil Iskandar
NIM : 01.17.080
Masa Bimbingan : 9 Desember 2005 s/d 9 Mei 2006
Judul : Perencanaan dan Pembuatan Alat Pentransfer Data
Argometer Taksi Berbasis Mikrokontroller AT89S8252
Yang Bisa Diupload KeKomputer Melalui Komunikasi
Radio

No	Tanggal	Uraian	Paraf
1	22 Maret 2006	Sumber-sumber bab II	
2	22 Maret 2006	Rangkaian Reset dan koneksi Modem	
3	22 Maret 2006	Pengujian Mikrokontroller	
4	22 Maret 2006	Pengujian keypad	
5	22 Maret 2006	Pengujian dan software LCD	
6	22 Maret 2006	Gambar 4.7	
7	22 Maret 2006	Rangkaian keseluruhan	

Disetujui

Penguji I

(Joseph. D. Irawan, ST, MT)

Penguji II

(Sotybhadi, ST) 28/3/06

Mengetahui,
Dosen Pembimbing

(Ir. Sidik Noertjahjono, MT)
NIP.Y .1028700167

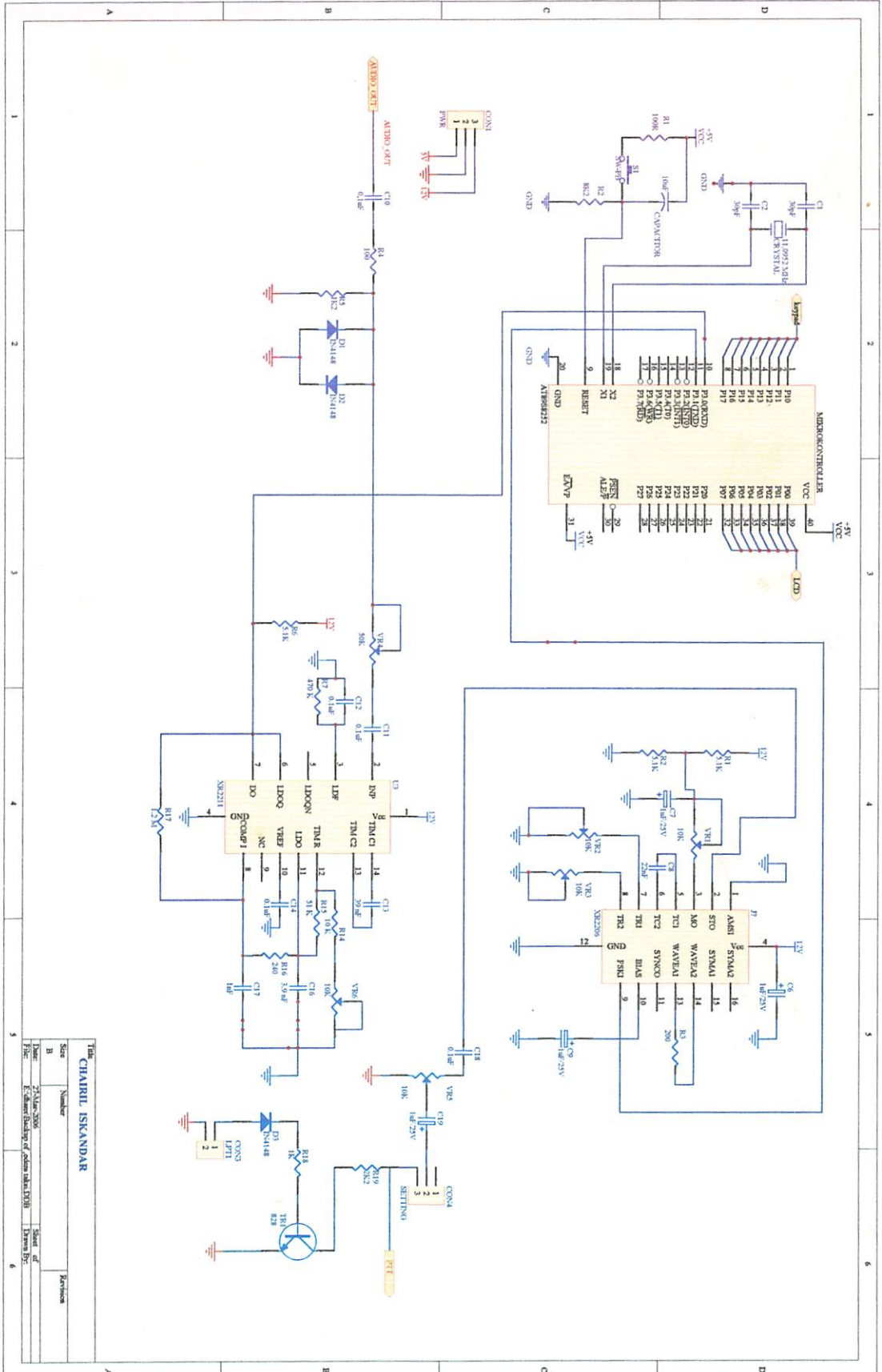
FORMULIR PEMBIMBING SKRIPSI

Nama : Chairil Iskandar
 Nim : 0117080
 Mas Bimbingan : 9 Desember- 10 Mei 2006
 Judul Skripsi : PERANCANGAN DAN PEMBUATAN ALAT
 PENTRANSFER DATA PADA ARGOMETER TAKSI YANG
 BERBASIS MIKROKONTROLLER AT89S8252 YANG BISA
 DI UPLOAD KE KOMPUTER

NO	TANGGAL	URAIAN	PARAF
1	10 12 05.	Konultasi judul & diagram blok	
2	5 1 06.	Realisasi diagram blok ke rangkaian elektronik.	
3	21 1 06.	Uji Modem, test FSK kirim/terima, software	
4	2 2 06.	Bab IV, uji coba awal kesimpulan, tulis Bab IV	
5	12 2 06.	Tulis makalah seminar persiapan.	
6	28 2 06.	Bab II, pada perencanaan, buat source Request pd. software	
7	2 3 06.	Bab II, Teori Uly parity bit dan BER.	
8	10 3 06.	Bab II, rangkaian key pad, Teori Modem, Bab I, ke	
9	17 3 06.	Revisi Abstract, hanya 3 paragraf, cubic dr. Bab I	
10	20 3 07.	Revisi lap, persiapan Ujian	

Malang,
 DOSEN PEMBIMBING

Ir. Sidik Noerhahjono, MT
 NIP. Y. 1028700167



Title		CHAIRIL ISKANDAR	
Start	Number	Start of	Revisi
27/11/2008			
Name		E-Systems Institute of Science (Indonesian)	
Date		November 2008	

1 2 3 4 5 6

LISTING PROGRAM

```
Dim FileName As String
Dim FileName1 As String
```

```
Private Sub cmdAmbilData_Click()
```

```
Dim a, b, c, d, e, f, g, h, i, j, k, l, m, n, o, p, q, r, s, t, u, v, w, x, y, z
```

```
Dim s0, s1, s2, s3, s4, s5, s6, s7, s8, s9
```

```
Dim s10, s11, s12, s13, s14, s15, s16, s17, s18, s19
```

```
Dim s20, s21, s22, s23, s24, s25, s26, s27, s28, s29
```

```
Dim s30, s31, s32, s33, s34, s35, s36, s37, s38, s39
```

```
Dim EA As Variant
```

```
Dim Rupiah As Long
```

```
Dim Km As Long
```

```
Dim Waktu As Long
```

```
Dim Taxi As Integer
```

```
FileName1 = App.Path & "\" & Replace(DTP1.Value, "/", "_") & ".txt"
```

```
If Dir(FileName1) = "" Then
```

```
    MsgBox "Data tidak ditemukan", vbCritical, "Error"
```

```
    LV2.ListItems.Clear
```

```
    Exit Sub
```

```
End If
```

```
CM1.OpenFile FileName1
```

```
LV2.ListItems.Clear
```

```
If CM1.Text = "" Then Exit Sub
```

```
For i = 0 To CM1.LineCount - 2
```

```
    a = CM1.GetLine(i)
```

```
    EA = Split(a, ";")
```

```
    LV2.ListItems.Add, "A" & Date & Time & i, LV2.ListItems.Count + 1
```

```
    LV2.ListItems(LV2.ListItems.Count).SubItems(1) = EA(0)
```

```
    LV2.ListItems(LV2.ListItems.Count).SubItems(2) = EA(1)
```

```
    LV2.ListItems(LV2.ListItems.Count).SubItems(3) = EA(2)
```

```
    LV2.ListItems(LV2.ListItems.Count).SubItems(4) = EA(3)
```

```
Next i
```

```
End Sub
```

```
Private Sub cmdClearData_Click()
```

```
    LV1.ListItems.Clear
```

```
End Sub
```

```
Private Sub cmdComm_Click()
```

```
frmProperties.Show vbModal  
End Sub
```

```
Private Sub cmdConnect_Click()  
If cmdConnect.Caption = "Connect" Then  
MSComm1.PortOpen = True  
cmdConnect.Caption = "Disconnect"  
Proses = Awal  
Else  
MSComm1.PortOpen = False  
cmdConnect.Caption = "Connect"  
End If  
End Sub
```

```
Private Sub cmdExit_Click()  
Unload Me  
End Sub
```

```
Private Sub cmdGetData_Click()  
  
If MSComm1.PortOpen = False Then  
MsgBox "Komunikasi belum diaktifkan", vbCritical, "Error "  
Exit Sub  
End If
```

```
If txtNo.Text = "" Then  
MsgBox "Isi nomor Labung 2 digit", vbCritical, "Error"  
Exit Sub  
End If
```

```
txtTerm.Text = ""
```

```
MSComm1.DTREnable = True  
Sleep 7000
```

```
MSComm1.Output = "RES"
```

```
'DoEvents  
'If txtTerm.Text <> "" Then Exit Do  
'Sleep 100  
'MSComm1.Output = "RES"
```

```
Sleep 100  
MSComm1.Output = txtNo.Text 'Send ID
```



```
    Sleep 500
'Loop
MSComm1.DTREnable = False
```

```
End Sub
```

```
Private Sub cmdSave_Click()
Dim a, b, c, d, e, f, g, h, i, j, k, l, m, n, o, p, q, r, s, t, u, v, w, x, y, z
Dim s0, s1, s2, s3, s4, s5, s6, s7, s8, s9
Dim s10, s11, s12, s13, s14, s15, s16, s17, s18, s19
Dim s20, s21, s22, s23, s24, s25, s26, s27, s28, s29
Dim s30, s31, s32, s33, s34, s35, s36, s37, s38, s39

If LV1.ListItems.Count = 0 Then
    If MsgBox("Anda yakin menyimpan data koso.ang?", vbOKCancel,
"Perhatian") = vbCancel Then Exit Sub
End If

s30 = App.Path & "\ " & Replace(lblTanggal.Caption, "/", "_") & ".txt"

CM1.Text = ""
For i = 1 To LV1.ListItems.Count
    a = LV1.ListItems(i).SubItems(1) & ";"
    b = LV1.ListItems(i).SubItems(2) & ";"
    c = LV1.ListItems(i).SubItems(3) & ";"
    d = LV1.ListItems(i).SubItems(4) & ";"
    CM1.Text = CM1.Text & a & b & c & d & vbCrLf
Next i

CM1.SaveFile s30, True
a = a
End Sub
```

```
Private Sub Form_Load()
Dim a, b, c, d, e, f, g, h, i, j, k, l, m, n, o, p, q, r, s, t, u, v, w, x, y, z
Dim s0, s1, s2, s3, s4, s5, s6, s7, s8, s9
Dim s10, s11, s12, s13, s14, s15, s16, s17, s18, s19
Dim s20, s21, s22, s23, s24, s25, s26, s27, s28, s29
Dim s30, s31, s32, s33, s34, s35, s36, s37, s38, s39
Dim EA As Variant
Dim Str1 As String
```

```
Dim CommPort As String, Handshaking As String, Settings As String
```

```
lblTanggal.Caption = Date
```

```
FileName1 = App.Path & "\\" & Replace(Date, "/", "_") & ".txt"
```

```
If Dir(FileName1) = "" Then
```

```
    LV1.ListItems.Clear
```

```
    Exit Sub
```

```
End If
```

```
CM1.OpenFile FileName1
```

```
LV1.ListItems.Clear
```

```
If CM1.Text = "" Then Exit Sub
```

```
For i = 0 To CM1.LineCount - 2
```

```
    a = CM1.GetLine(i)
```

```
    EA = Split(a, ";")
```

```
    LV1.ListItems.Add , "A" & Date & Time & i, LV1.ListItems.Count + 1
```

```
    LV1.ListItems(LV1.ListItems.Count).SubItems(1) = EA(0)
```

```
    LV1.ListItems(LV1.ListItems.Count).SubItems(2) = EA(1)
```

```
    LV1.ListItems(LV1.ListItems.Count).SubItems(3) = EA(2)
```

```
    LV1.ListItems(LV1.ListItems.Count).SubItems(4) = EA(3)
```

```
Next i
```

```
End Sub
```

```
Private Sub MSComm1_OnComm()
```

```
    Dim EVMsg$
```

```
    Dim ERMsg$
```

```
    ' Branch according to the CommEvent property.
```

```
    Select Case MSComm1.CommEvent
```

```
        ' Event messages.
```

```
        Case comEvReceive
```

```
            Dim Buffer As Variant
```

```
            Buffer = MSComm1.Input
```

```
            Debug.Print "Receive - " & StrConv(Buffer, vbUnicode)
```

```
            ShowData txtTerm, (StrConv(Buffer, vbUnicode))
```

```
        Case comEvSend
```

```
        Case comEvCTS
```

```
            EVMsg$ = "Change in CTS Detected"
```

```
        Case comEvDSR
```

```
            EVMsg$ = "Change in DSR Detected"
```

```
        Case comEvCD
```

```
            EVMsg$ := "Change in CD Detected"
```

```

    Case comEvRing
        EVMsg$ = "The Phone is Ringing"
    Case comEvEOF
        EVMsg$ = "End of File Detected"
    GoTo x1
' Error messages.
'
' Case comBreak
'     ERMsg$ = "Break Received"
' Case comCDTO
'     ERMsg$ = "Carrier Detect Timeout"
' Case comCTSTO
'     ERMsg$ = "CTS Timeout"
' Case comDCB
'     ERMsg$ = "Error retrieving DCB"
' Case comDSRTO
'     ERMsg$ = "DSR Timeout"
' Case comFrame
'     ERMsg$ = "Framing Error"
' Case comOverrun
'     ERMsg$ = "Overrun Error"
' Case comRxOver
'     ERMsg$ = "Receive Buffer Overflow"
' Case comRxParity
'     ERMsg$ = "Parity Error"
' Case comTxFull
'     ERMsg$ = "Transmit Buffer Full"
x1:
    Case Else
        Err.Clear
        ERMsg$ = "Unknown error or event"
    End Select

End Sub

Private Static Sub ShowData(Term As Control, Data As String)
    On Error GoTo Handler
    Const MAXTERMSIZE = 16000
    Dim TermSize As Long, i

    ' Make sure the existing text doesn't get too large.
    TermSize = Len(Term.Text)
    If TermSize > MAXTERMSIZE Then
        Term.Text = Mid$(Term.Text, 4097)
        TermSize = Len(Term.Text)
    End If

    ' Point to the end of Term's data.

```

```

Term.SelStart = TermSize

' Filter/handle BACKSPACE characters.
Do
  i = InStr(Data, Chr$(8))
  If i Then
    If i = 1 Then
      Term.SelStart = TermSize - 1
      Term.SelLength = 1
      Data = Mid$(Data, i + 1)
    Else
      Data = Left$(Data, i - 2) & Mid$(Data, i + 1)
    End If
  End If
Loop While i

' Eliminate line feeds.
Do
  i = InStr(Data, Chr$(10))
  If i Then
    Data = Left$(Data, i - 1) & Mid$(Data, i + 1)
  End If
Loop While i

' Make sure all carriage returns have a line feed.
i = 1
Do
  i = InStr(i, Data, Chr$(13))
  If i Then
    Data = Left$(Data, i) & Chr$(10) & Mid$(Data, i + 1)
    i = i + 1
  End If
Loop While i

' Add the filtered data to the SelText property.
Term.SelText = Data

' Log data to file if requested.
Term.SelStart = Len(Term.Text)
Exit Sub

Handler:
  MsgBox Error$
  Resume Next
End Sub

```

```

Private Sub txtTerm_Change()
Dim a, b, c, d, e, f, g, h, i, j, k, l, m, n, o, p, q, r, s, t, u, v, w, x, y, z
Dim s0, s1, s2, s3, s4, s5, s6, s7, s8, s9
Dim s10, s11, s12, s13, s14, s15, s16, s17, s18, s19
Dim s20, s21, s22, s23, s24, s25, s26, s27, s28, s29
Dim s30, s31, s32, s33, s34, s35, s36, s37, s38, s39
Dim Rupiah As Long
Dim Km As Long
Dim Waktu As Long
Dim Taxi As Integer

If txtTerm.Text = "" Then Exit Sub
a = InStr(1, txtTerm.Text, "LB")
If a <> 0 Then
    b = InStrRev(txtTerm.Text, "RP", -1, vbTextCompare)
    If b = 0 Then Exit Sub
    c = InStr(b, txtTerm.Text, "$", vbTextCompare)
    If c = 0 Then Exit Sub
    Rupiah = Mid(txtTerm.Text, b + 2, c - b - 2)
    '-----
    d = InStr(b, txtTerm.Text, "$W", vbTextCompare)
    If d = 0 Then Exit Sub
    e = InStr(d, txtTerm.Text, "&K", vbTextCompare)
    If e = 0 Then Exit Sub
    Waktu = Mid(txtTerm.Text, d + 2, e - d - 2)
    '-----
    b = InStr(d, txtTerm.Text, "&K", vbTextCompare)
    If b = 0 Then Exit Sub
    c = InStr(b, txtTerm.Text, "KM", vbTextCompare)
    If c = 0 Then Exit Sub
    Km = Mid(txtTerm.Text, b + 2, c - b - 2)
    '-----
    b = InStrRev(txtTerm.Text, "LB", -1, vbTextCompare)
    Taxi = Mid(txtTerm.Text, b - 2, 2)

    LV1.ListItems.Clear
    LV1.ListItems.Add, "A" & Date & Time, LV1.ListItems.Count + 1
    LV1.ListItems(LV1.ListItems.Count).SubItems(1) = Taxi
    LV1.ListItems(LV1.ListItems.Count).SubItems(2) = Km
    LV1.ListItems(LV1.ListItems.Count).SubItems(3) = Mid(Waktu, 1, 2) & ":"
    & Right(Waktu, 2)
    LV1.ListItems(LV1.ListItems.Count).SubItems(4) = Rupiah

    txtTerm.Text = ""
End If
End Sub

```

kolom1	Bit	P1.4	;	kiri (1,4,7,redial)
kolom2	Bit	P1.5	;	(2,5,8,0)
kolom3	Bit	P1.6	;	(3,3,9,#
kolom4	Bit	P1.7		

baris1	Bit	P1.0	;	atas (1,2,3)
baris2	Bit	P1.1	;	(4,5,6)
baris3	Bit	P1.2	;	(7,8,9)
baris4	Bit	P1.3	;	(* ,0,#)

keyport	Equ	P1		
relay	Bit	P2.5		

cd_rs	Bit	P2.7		
cd_ena	Bit	P2.6		
cd_Data	Equ	P0		

keydata	Data	20h		
keymp	Data	21h		

flagKey	Data	24h		
---------	------	-----	--	--

tekantombol	data	30h	30-46//	47,48=stack
mpnilai1	Data	50h	;	50-56

```

Clr EA
Mov SP,#80h

```

```

Call LCD_Inisialisasi
Call Serial_Initialization

```

```

start:
Call LCD_Inisialisasi
Call Serial_Initialization
Setb RI

```

```

lang:
Clr Relay

```

```

keyInGetmatrix1:
Clr kolom3
Jnb baris4,KeyInGetmatrix0

Jnb RI,KeyInGetmatrix1

Call Serial_Receive

Cjne A,#'R',KeyInGetmatrix1

Call Serial_Receive

```

```

                                Taxi ITN
Cjne    A,#'E',KeyInGetmatrix1
Call    Serial_Receive
Cjne    A,#'S',KeyInGetmatrix1
Call    Serial_Receive
Cjne    A,75h,KeyInGetmatrix1
Call    Serial_Receive
Cjne    A,#76h,KeyInGetmatrix1
Setb    Relay
Call    Delay_Fix_1s
Call    Outxx
Call    Delay_Fix_1s
Clr     Relay
Jmp     start
KeyInGetmatrix0:
Jmp     Key_masukan
Key_masukan:
Call    Delay_Fix_1s
Call    Delay_Fix_100ms
-----
setRupiah:
Call    LCD_Clear
Call    lcd_line_1
Mov     DPTR,#txt_setRP
Call    LCD_TampilKata

Call    LCD_Line_2
Mov     DPTR,#txt_setRP1
Call    LCD_TampilKata

Call    LCD_Blink_On
Mov     A,#0C5h
Call    LCD_Tulis_Inst
Mov     temp,#6
Mov     R0,#25h
Mov     @R0,#'R'
Inc     R0
Mov     @R0,#'p'
Inc     R0
ambilKeypad1:
Mov     FlagKey,#0

```

```

                                Taxi ITN
    Call    Keypad_KeyIn
    ;Mov    B,A

    Mov     @R0,A
    Cjne   A,#'#',AmbilKeypad2
    Mov     @R0,#'$'
    Jmp    Yakinxx
ambilKeypad2:

MBILKEYPAD3:

    Inc     R0
    Djnz   temp,AmbilKeypad1

    Mov     @R0,#'$'
    Jmp    Yakinxx

yakinxx:
    Call   LCD_Blink_Off
    Call   Delay_Fix_1s
    ;Jmp   outaa

setwaktu:
    Call   LCD_Clear
    Call   lcd_line_1
    Mov    DPTR,#txt_setwaktu
    Call   LCD_TampilKata
    Call   LCD_Line_2
    Mov    DPTR,#txt_setwaktu1
    Call   LCD_TampilKata

cek_rp:
    Mov    R0,#25h
cek_rp1:
    Mov    A,@R0
    Cjne  A,#'$',cek_rp2
    Inc    R0
    Jmp    Setwaktu1
cek_rp2:
    Inc    R0
    Jmp    cek_rp1

setwaktu1:
    Mov    @R0,#'w'
    Inc    R0
    Call   LCD_Blink_On
    ; masukan jam
    Mov    A,#0C4h
    Call   LCD_Tulis_Inst

    Mov    FlagKey,#0
    Call   Keypad_KeyIn
    Mov    @R0,A

```


Taxi ITN

```

Inc      R0
Mov      FlagKey,#0
Call     Keypad_KeyIn
Mov      @R0,A
Inc      R0
Mov      A,#':'
Call     LCD_Tulis_Data

```

```

Mov      FlagKey,#0
Call     Keypad_KeyIn
Mov      @R0,A
Inc      R0

```

```

Mov      FlagKey,#0
Call     Keypad_KeyIn
Mov      @R0,A
Inc      R0

```

```

Mov      @R0,#'&'
Call     LCD_Blink_Off
Call     Delay_Fix_1s

```

etkilo:

```

Call     LCD_Clear
Call     lcd_line_1
Mov      DPTR,#txt_setKM
Call     LCD_TampilKata

Call     LCD_Line_2
Mov      DPTR,#txt_setKM1
Call     LCD_TampilKata

```

ekwaktu:

```

Mov      R0,#25h

```

ekwaktu1:

```

Mov      A,@R0
Cjne    A,#'&',cekwaktu2
Inc      R0
Jmp     Setkilo1

```

ekwaktu2:

```

Inc      R0
Jmp     cekwaktu1

```

etkilo1:

```

Mov      @R0,#'K'
Inc      R0

Call     LCD_Blink_On
Mov      A,#0C2h

```

Taxi ITN

```

Call    LCD_Tulis_Inst
Mov     temp,#3
setkilo2:
Mov     FlagKey,#0
Call    Keypad_KeyIn

Mov     @R0,A
Cjne   A,#'#',AmbilKeypad2zz
Mov     @R0,'#K'
Inc     R0
Mov     @R0,'#M'
Jmp     setNo
ambilKeypad2zz:
Inc     R0
Djnz   temp,Setkilo2

Mov     @R0,'#K'
Inc     R0
Mov     @R0,'#M'

Jmp     setNo
setNo:

Call    LCD_Clear
Call    lcd_line_1
Mov     DPTR,#txt_lambung
Call    LCD_TampilKata

Call    LCD_Line_2
Mov     DPTR,#txt_lambung1
Call    LCD_TampilKata

Mov     R0,#25h

setNo1:
Mov     A,@R0
Cjne   A,'#M',SetNo2
Inc     R0
Jmp     Setno3

setNo2:
Inc     R0
Jmp     SetNo1

setNo3:

Call    LCD_Blink_On

Mov     A,#0C4h
Call    LCD_Tulis_Inst

Mov     FlagKey,#0
Call    Keypad_KeyIn

```

Taxi ITN

```
Mov 75h,A
Mov @R0,A
```

```
Inc R0
```

```
Mov FlagKey,#0
Call Keypad_KeyIn
Mov 75h,A
Mov @R0,A
Inc R0
```

```
Mov @R0,#'L'
```

```
Inc R0
Mov @R0,#'B'
Inc R0
```

Yakin1cx:

```
Call LCD_Blink_Off
Call Delay_Fix_1s
```

```
Call LCD_Clear
Call lcd_line_1
Mov DPTR,#txt_menuyakin
Call LCD_TampilKata
```

```
Call LCD_Line_2
Mov DPTR,#txt_menuyakin1
Call LCD_TampilKata
```

Yakin1C:

```
Mov FlagKey,#0
Call Keypad_KeyIn
Cjne A,#'1',Yakin2C
Call Simpan_data1
;Call Outxx
Call Delay_Fix_1s
Call Delay_Fix_1s
Call LCD_Clear
Jmp start
```

Yakin2C:

```
Cjne A,#'2',Yakin1C
Call LCD_Clear
Jmp start
```

Subroutine Outxx:

```
Call Delay_Fix_1s
Call LCD_Clear
```

Ang1:

```
Mov R0,#52h
Mov A,@R0
```

```

                                Taxi ITN
Cjne    A,#'B',TampilKandata
Call    Serial_Transmit

Ret
TampilKandata:
Call    Serial_Transmit
Inc     R0
Jmp     ulang1

ndSub

=====
Subroutine Simpan_data1:

Call    LCD_Clear
Call    lcd_line_1
Mov     DPTR,#txt_simpan
Call    LCD_TampilKata
Call    Delay_Fix_1s

Mov     47h,#25h
Mov     48h,#52h
SimpanData2:
Mov     R0,47h                ;r0=30h // r0=31h
Mov     A,@R0                ;a=30h  // a=31h
Cjne    A,#'B',SimpanData3
Mov     R0,48h                ;r0=52h // r0=53h
Mov     @R0,A                ;52h<=30h //53h<=31h

Ret                                     ;start
SimpanData3:
Inc     R0                    ;r0=31h //r0=32h
Mov     47h,R0                ;40h=31h //40h=32h
Mov     R0,48h                ;r0=52h // r0=53h
Mov     @R0,A                ;52h<=30h //53h<=31h
Inc     R0                    ;r0=53  // r0=54h
Mov     48h,R0                ;41h=53 //41=54h

Jmp     SimpanData2

ndSub

Subroutine Conversion_Hexa_BCD:
Push    B
Mov     B,#100
Mov     6,A
Mov     A,#10
Add     A,B
Mov     7,A
Pop     B
Ret

ndSub

```

Taxi ITN

```

subroutine Keypad_KeyIn:
    Push    B                ; amankan register B
KeyInGet1:
    Call    Keypad3x4        ; scan keypad
    Mov     A, keydata       ; isi keydata = data di rutin
Keypad:
    Cjne   A, #0FFh, KeyInGet0 ; jk isi a # 0ffh ==> lompat
    Jmp    KeyInGet1
KeyInGet0:
    Mov     B, A             ; simpan isi a to b
KeyInGet:
    Call    Keypad3x4
    Mov     A, keydata
    Cjne   A, B, KeyInOut    ; jk isi A # B lompat
    Jmp    KeyInGet
KeyInOut:
    Cjne   A, #0, KeyInOut1
    MOV    A, B
    Call    LCD_Tulis_Data
    Pop    B
    Ret
KeyInOut1:
    Mov     A, B
    Pop    B                ; idem
EndSub

```

```

=====
routine u/ baca keypad 3x4
output pd keydata(0-9,E=redial,F=#)
=====

```

subroutine Keypad3x4:

```

    Mov     keyport, #0FFh
    Clr     kolom1
-----
11:
    Jb     baris1, key1
    Mov     keydata, #'1'
    Ret
Key1:
    Jb     baris2, key2
    Mov     keydata, #'4'
    Ret
Key2:
    Jb     baris3, key3
    Mov     keydata, #'7'
    Ret
Key3:
    ;Jb     baris4, key4
    ;Mov     keydata, #'*'
    ;Ret
-----

```

Taxi ITN

ey4:

```

Setb   kolom1
Clr    kolom2
;-----
Jb     baris1,key5
Mov    keydata,#'2'
Ret
    
```

ey5:

```

Jb     baris2,key6
Mov    keydata,#'5'
Ret
    
```

ey6:

```

Jb     baris3,key7
Mov    keydata,#'8'
Ret
    
```

ey7:

```

Jb     baris4,key8
Mov    keydata,#'0'
Ret
;-----
    
```

ey8:

```

Setb   kolom2
Clr    kolom3
;-----
Jb     baris1,key9
Mov    keydata,#'3'
Ret
    
```

ey9:

```

Jb     baris2,key10
Mov    keydata,#'6'
Ret
    
```

ey10:

```

Jb     baris3,key11
Mov    keydata,#'9'
Ret
    
```

ey11:

```

Jb     baris4,key12
Mov    keydata,#'#'
Ret
    
```

ey12:

```

Mov    keydata,#0FFh
    
```

dSub

broutine Serial_Receive:

```

Jnb    RI,$
Clr    RI
Mov    A,SBUF
Clr    RI
    
```

dSub

broutine Serial_Transmit:

```

Mov    SBUF,A
    
```

Taxi ITN

```
Jnb    TI,$
Clr    TI
```

```
Ret
```

ndSub

ibroutine Serial_Initialization:

```
Mov    SCON,#50h
Mov    TH1,#208      ; BAUDRATE 1200
Mov    87h,#00h      ; PCON
Mov    TMOD,#21h
Mov    TCON,#01010000B ; RUN T1 AND T0
;Mov   IE,#10000010B
;Mov   IP,#00001000B
```

ndSub

ibroutine LCD_Clear:

```
Mov    A,#01h
Call   LCD_Tulis_Inst
```

ndSub

ibroutine LCD_Blink_Off:

```
Push   ACC
Mov    A,#00001100b ;
Lcall  LCD_Tulis_Inst
Pop    ACC
```

ndSub

ibroutine LCD_Blink_On:

```
Push   ACC
Mov    A,#00001101b ;
Lcall  LCD_Tulis_Inst
Pop    ACC
```

ndSub

ibroutine lcd_line_1:

```
Mov    A,#80h
Call   LCD_Tulis_Inst
```

ndSub

ibroutine LCD_Line_2:

```
Mov    A,#0C0h
Call   LCD_Tulis_Inst
```

ndSub

ibroutine LCD_Cursor_Position:

```
Push   ACC
Mov    A,R0      ;15    26
Anl    A,#0F0h  ;10    20
Cjne   A,#10h,lcd_cursor_position1
Mov    A,R0      ;15
Call   LCD_Tulis_Inst
Jmp    lcd_cursor_position_end
```

nd_cursor_position1:

```
Cjne   A,#20h,lcd_cursor_position_end
Mov    A,R0      ;26
Call   LCD_Tulis_Inst
```

nd_cursor_position_end:

Taxi ITN

```

ndSub
ubroutine LCD_TampilKata:
    Push    ACC
    Push    DPL
    Push    DPH
TampilKata1:
    Clr     A
    Movc    A,@A+DPTR
    Cjne    A,#0,TampilKata2          ;intinya
    Jmp     out
TampilKata2:
    Inc     DPTR
    Call    LCD_Tulis_Data
    Jmp     TampilKata1
ut:
    Pop     DPH
    Pop     DPL
    Pop     ACC
ndSub

ubroutine LCD_Inisialisasi:
    ;call   delayL
    Mov     A,#3Fh
    Call    LCD_Tulis_Inst
    Mov     A,#0Ch
    Call    LCD_Tulis_Inst
    Mov     A,#06h
    Call    LCD_Tulis_Inst
    Mov     A,#1Ch
    Call    LCD_Tulis_Inst
    Mov     A,#01h
    Call    LCD_Tulis_Inst
ndSub

ubroutine LCD_Tulis_Inst:
    Clr     Lcd_rs
    Mov     Lcd_Data,A
    Setb    Lcd_ena
    Clr     Lcd_ena
ndSub

ubroutine LCD_Tulis_Data:
    Setb    Lcd_rs
    Mov     Lcd_Data,A
    Setb    Lcd_ena
    Clr     Lcd_ena
ndSub

===== DELAY =====
ubroutine Delay_Var_1ms:
    Call    Delay_Fix_1ms
    Djnz    R0,Delay_Var_1ms
ndSub

```


Taxi ITN

```

ubroutine Delay_Var_10ms:
    Call    Delay_Fix_10ms
    Djnz    R0,Delay_Var_10ms
ndSub
ubroutine Delay_Var_100ms:
    Call    Delay_Fix_1ms
    Djnz    R0,Delay_Var_100ms
ndSub
ubroutine Delay_Var_1s:
    Call    Delay_Fix_1s
    Djnz    R0,Delay_Var_1s
ndSub
ubroutine Delay_Var_10s:
    Call    Delay_Fix_10s
    Djnz    R0,Delay_Var_10s
ndSub
ubroutine Delay_Var_10us:
    Call    Delay_Fix_10us
    Djnz    R0,Delay_Var_10us
ndSub
ubroutine Delay_Fix_10us:
    Push    1
    Mov     1,#20
    Djnz    1,$
    Pop     1
ndSub
ubroutine Delay_Fix_10s:
    Push    1
    Mov     1,#10C
delay_fix_10s_1:
    Call    Delay_Fix_100ms
    Djnz    1,delay_fix_10s_1
    Pop     1
ndSub
ubroutine Delay_Fix_1s:
    Push    1
    Mov     1,#100
delay_fix_1000ms_1:
    Call    Delay_Fix_10ms
    Djnz    1,delay_fix_1000ms_1
    Pop     1
ndSub
ubroutine Delay_Fix_100ms:
    Push    1
    Mov     1,#10
delay_fix_100ms_1:
    Call    Delay_Fix_10ms
    Djnz    1,delay_fix_100ms_1
    Pop     1
ndSub
ubroutine Delay_Fix_10ms:
    Mov     TMOD,#0000001b ; Timer 1 bekerja pada mode 1

```

Taxi ITN

```

Mov   TLO,#3Dh   ; siapkan waktu tunda 50 mili-detik
Mov   TH0,#0BCh
Clr   TFO                ; me-nol-kan bit limpahan
Setb  TR0            ; timer mulai bekerja
Jnb   TFO,$          ; tunggu di sini sampai melimpah
Clr   TR0            ; timer berhenti kerja
Ret

```

dSub

broutine Delay_Fix_1ms:

```

Mov   TMOD,#00000001b ; Timer 1 bekerja pada mode 1
Mov   TLO,#0EDh   ; siapkan waktu tunda 50 mili-detik
Mov   TH0,#78h
Clr   TFO                ; me-nol-kan bit limpahan
Setb  TR0            ; timer mulai bekerja
Jnb   TFO,$          ; tunggu di sini sampai melimpah
Clr   TR0            ; timer berhenti kerja
Ret

```

dSub

```

; '1234567890abcdef'
t_menu1:   Db      '1.Set Nilai',0
t_menu2:   Db      '2.Run',0
t_menu3:   Db      '3.Set Kilo',0
t_menu4:   Db      '4.Run',0
t_menu5:   Db      'Pilih satu',0
t_menu6:   Db      '(1-2-3-4):',0

t_setRP:   Db      'Masukkan Harga',0
t_setRP1:  Db      '  RP.',0
t_setwaktu: Db      'Masukkan waktu',0
t_setwaktu1: Db      '  --:--',0
t_setKM:   Db      'Masukkan KM',0
t_setKM1:  Db      '  --- Km',0
t_menuyakin: Db      'Yakin?',0
t_menuyakin1: Db      '  Y-1,T-2',0
t_menuRP:  Db      '1. Rupiah:',0
t_menuwaktu: Db      '2. Waktu:',0
t_menuKilo: Db      '3. Kilo Meter:',0
t_simpan:  Db      'simpan data',0
t_lambung: Db      'Masukkan No.Taxi',0
t_lambung1: Db      'No. --',0

```

June 1997-3

FEATURES

Low-Sine Wave Distortion, 0.5%, Typical
Excellent Temperature Stability, 20ppm/°C, Typ.
Wide Sweep Range, 2000:1, Typical
Low-Supply Sensitivity, 0.01%V, Typ.
Linear Amplitude Modulation
TTL Compatible FSK Controls
Wide Supply Range, 10V to 26V
Adjustable Duty Cycle, 1% TO 99%

APPLICATIONS

- Waveform Generation
- Sweep Generation
- AM/FM Generation
- V/F Conversion
- FSK Generation
- Phase-Locked Loops (VCO)

GENERAL DESCRIPTION

The XR-2206 is a monolithic function generator integrated circuit capable of producing high quality sine, square, triangle, ramp, and pulse waveforms of high-stability and accuracy. The output waveforms can be both amplitude and frequency modulated by an external voltage. Frequency of operation can be selected externally over a range of 0.01Hz to more than 1MHz.

The circuit is ideally suited for communications, instrumentation, and function generator applications requiring sinusoidal tone, AM, FM, or FSK generation. It has a typical drift specification of 20ppm/°C. The oscillator frequency can be linearly swept over a 2000:1 frequency range with an external control voltage, while maintaining low distortion.

ORDERING INFORMATION

Part No.	Package	Operating Temperature Range
XR-2206M	16 Lead 300 Mil CDIP	-55°C to +125°C
XR-2206P	16 Lead 300 Mil PDIP	-40°C to +85°C
XR-2206CP	16 Lead 300 Mil PDIP	0°C to +70°C
XR-2206D	16 Lead 300 Mil JEDEC SOIC	0°C to +70°C

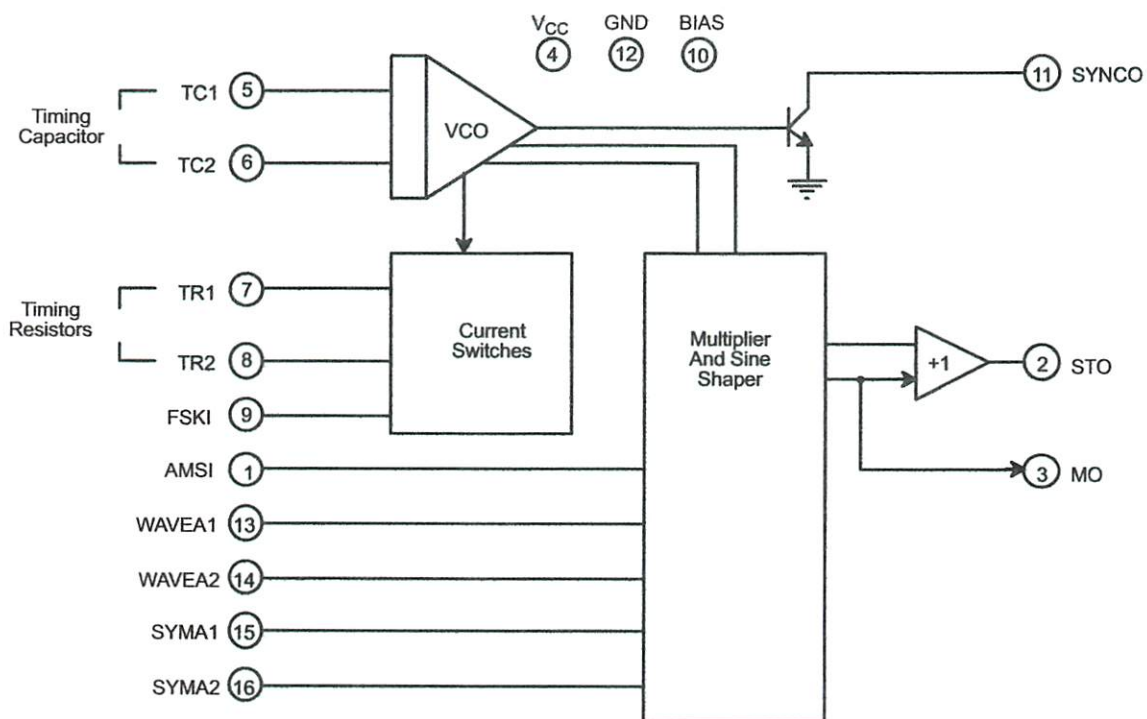
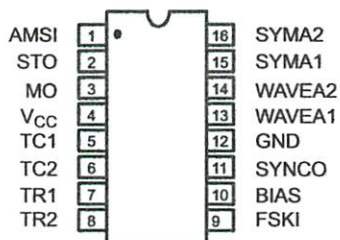
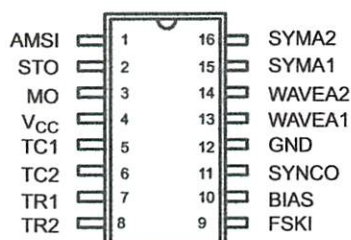


Figure 1. XR-2206 Block Diagram



16 Lead PDIP, CDIP (0.300")



16 Lead SOIC (Jedec, 0.300")

FUNCTION DESCRIPTION

Pin #	Symbol	Type	Description
1	AMSI	I	Amplitude Modulating Signal Input.
2	STO	O	Sine or Triangle Wave Output.
3	MO	O	Multiplier Output.
4	V _{CC}		Positive Power Supply.
5	TC1	I	Timing Capacitor Input.
6	TC2	I	Timing Capacitor Input.
7	TR1	O	Timing Resistor 1 Output.
8	TR2	O	Timing Resistor 2 Output.
9	FSKI	I	Frequency Shift Keying Input.
10	BIAS	O	Internal Voltage Reference.
11	SYNCO	O	Sync Output. This output is an open collector and needs a pull up resistor to V _{CC} .
12	GND		Ground pin.
13	WAVEA1	I	Wave Form Adjust Input 1.
14	WAVEA2	I	Wave Form Adjust Input 2.
15	SYMA1	I	Wave Symmetry Adjust 1.
16	SYMA2	I	Wave Symmetry Adjust 2.

ELECTRICAL CHARACTERISTICS

Test Conditions: Test Circuit of Figure 2 $V_{CC} = 12V$, $T_A = 25^\circ C$, $C = 0.01\mu F$, $R_1 = 100k\Omega$, $R_2 = 10k\Omega$, $R_3 = 25k\Omega$
 unless Otherwise Specified. S_1 open for triangle, closed for sine wave.

Parameters	XR-2206M/P			XR-2206CP/D			Units	Conditions
	Min.	Typ.	Max.	Min.	Typ.	Max.		
General Characteristics								
Single Supply Voltage	10		26	10		26	V	
Split-Supply Voltage	± 5		± 13	± 5		± 13	V	
Supply Current		12	17		14	20	mA	$R_1 \geq 10k\Omega$
Oscillator Section								
Max. Operating Frequency	0.5	1		0.5	1		MHz	$C = 1000pF$, $R_1 = 1k\Omega$
Lowest Practical Frequency		0.01			0.01		Hz	$C = 50\mu F$, $R_1 = 2M\Omega$
Frequency Accuracy		± 1	± 4		± 2		% of f_o	$f_o = 1/R_1 C$
Temperature Stability		± 10	± 50		± 20		ppm/ $^\circ C$	$0^\circ C \leq T_A \leq 70^\circ C$ $R_1 = R_2 = 20k\Omega$
Sine Wave Amplitude Stability ²		4800			4800		ppm/ $^\circ C$	
Supply Sensitivity		0.01	0.1		0.01		%/V	$V_{LOW} = 10V$, $V_{HIGH} = 20V$, $R_1 = R_2 = 20k\Omega$
Sweep Range	1000:1	2000:1			2000:1		$f_H = f_L$	$f_H @ R_1 = 1k\Omega$ $f_L @ R_1 = 2M\Omega$
Sweep Linearity								
10:1 Sweep		2			2		%	$f_L = 1kHz$, $f_H = 10kHz$
1000:1 Sweep		8			8		%	$f_L = 100Hz$, $f_H = 100kHz$
FM Distortion		0.1			0.1		%	$\pm 10\%$ Deviation
Recommended Timing Components								
Timing Capacitor: C	0.001		100	0.001		100	μF	Figure 5
Timing Resistors: R_1 & R_2	1		2000	1		2000	$k\Omega$	
Triangle Sine Wave Output¹								Figure 3
Triangle Amplitude		160			160		mV/ $k\Omega$	Figure 2, S_1 Open
Sine Wave Amplitude	40	60	80		60		mV/ $k\Omega$	Figure 2, S_1 Closed
Max. Output Swing		6			6		Vp-p	
Output Impedance		600			600		Ω	
Triangle Linearity		1			1		%	
Amplitude Stability		0.5			0.5		dB	For 1000:1 Sweep
Sine Wave Distortion								
Without Adjustment		2.5			2.5		%	$R_1 = 30k\Omega$
With Adjustment		0.4	1.0		0.5	1.5	%	See Figure 7 and Figure 8

Notes

¹Output amplitude is directly proportional to the resistance, R_3 , on Pin 3. See Figure 3.

²For maximum amplitude stability, R_3 should be a positive temperature coefficient resistor.

Bold face parameters are covered by production test and guaranteed over operating temperature range.

ELECTRICAL CHARACTERISTICS (CONT'D)

Parameters	XR-2206M/P			XR-2206CP/D			Units	Conditions
	Min.	Typ.	Max.	Min.	Typ.	Max.		
Amplitude Modulation								
Input Impedance	50	100		50	100		k Ω	
Modulation Range		100			100		%	
Carrier Suppression		55			55		dB	
Linearity		2			2		%	For 95% modulation
Square-Wave Output								
Amplitude		12			12		Vp-p	Measured at Pin 11.
Rise Time		250			250		ns	$C_L = 10\text{pF}$
Fall Time		50			50		ns	$C_L = 10\text{pF}$
Saturation Voltage		0.2	0.4		0.2	0.6	V	$I_L = 2\text{mA}$
Leakage Current		0.1	20		0.1	100	μA	$V_{CC} = 26\text{V}$
FSK Keying Level (Pin 9)	0.8	1.4	2.4	0.8	1.4	2.4	V	See section on circuit controls
Reference Bypass Voltage	2.9	3.1	3.3	2.5	3	3.5	V	Measured at Pin 10.

Notes

Output amplitude is directly proportional to the resistance, R_3 , on Pin 3. See Figure 3.

For maximum amplitude stability, R_3 should be a positive temperature coefficient resistor.

Old face parameters are covered by production test and guaranteed over operating temperature range.

Specifications are subject to change without notice

ABSOLUTE MAXIMUM RATINGS

Power Supply 26V
 Power Dissipation 750mW
 Operate Above 25°C 5mW/°C

Total Timing Current 6mA
 Storage Temperature -65°C to +150°C

SYSTEM DESCRIPTION

The XR-2206 is comprised of four functional blocks; a voltage-controlled oscillator (VCO), an analog multiplier and sine-shaper; a unity gain buffer amplifier; and a set of current switches.

The VCO produces an output frequency proportional to input current, which is set by a resistor from the timing

terminals to ground. With two timing pins, two discrete output frequencies can be independently produced for FSK generation applications by using the FSK input control pin. This input controls the current switches which select one of the timing resistor currents, and routes it to the VCO.

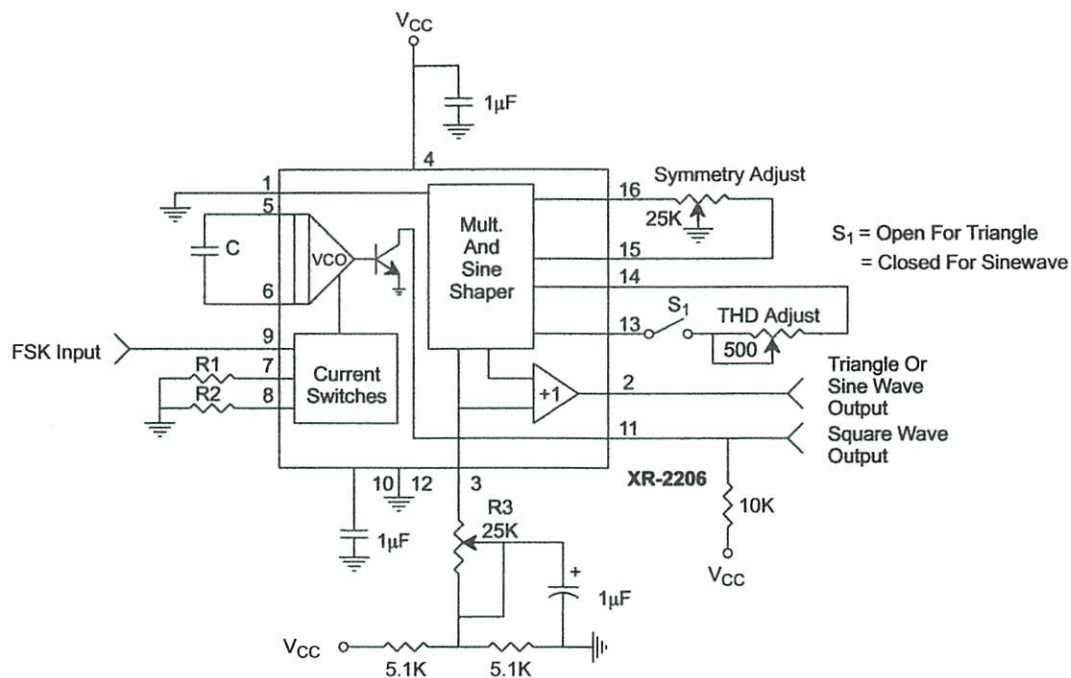


Figure 2. Basic Test Circuit

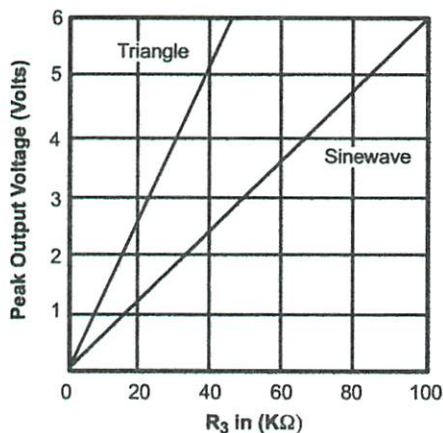


Figure 3. Output Amplitude as a Function of the Resistor, R_3 , at Pin 3

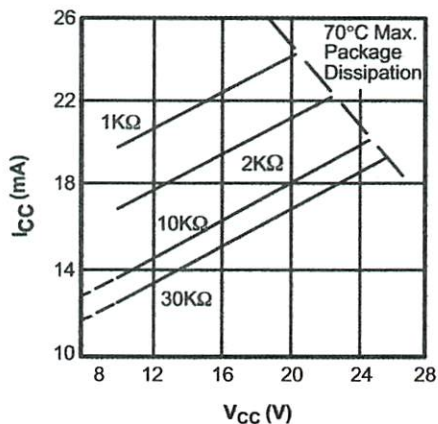


Figure 4. Supply Current vs Supply Voltage, Timing, R

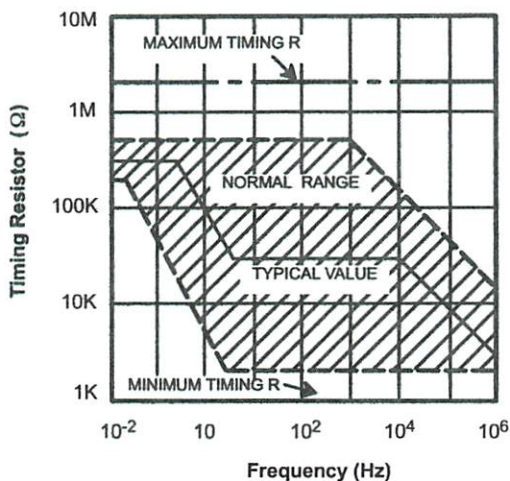


Figure 5. R versus Oscillation Frequency.

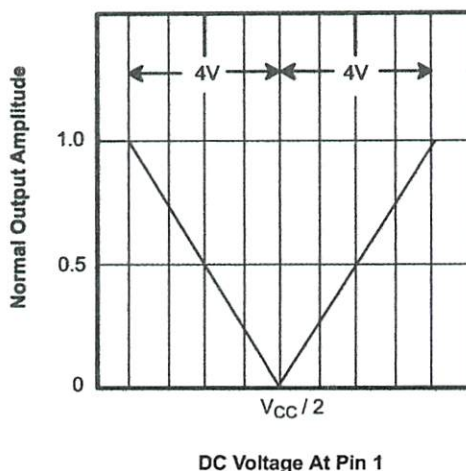


Figure 6. Normalized Output Amplitude versus DC Bias at AM Input (Pin 1)

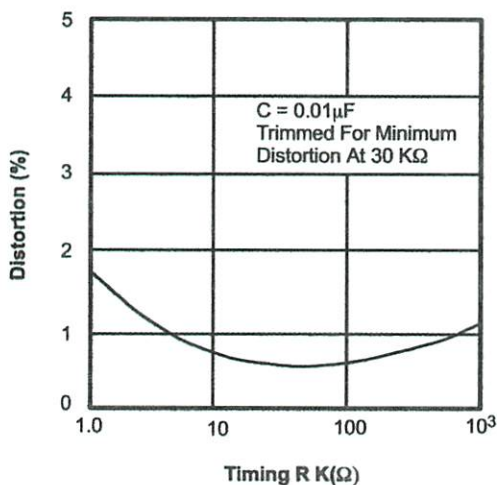


Figure 7. Trimmed Distortion versus Timing Resistor.

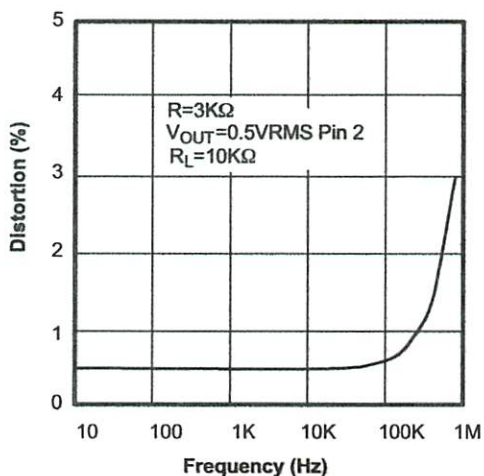


Figure 8. Sine Wave Distortion versus Operating Frequency with Timing Capacitors Varied.

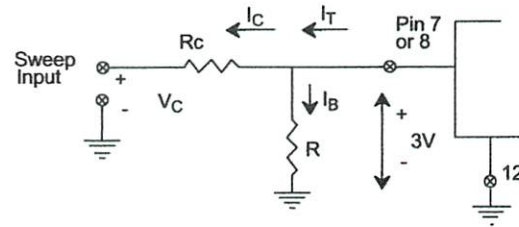
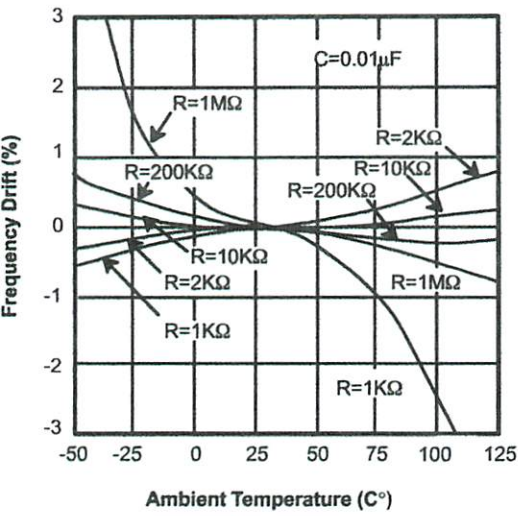


Figure 9. Frequency Drift versus Temperature.

Figure 10. Circuit Connection for Frequency Sweep.

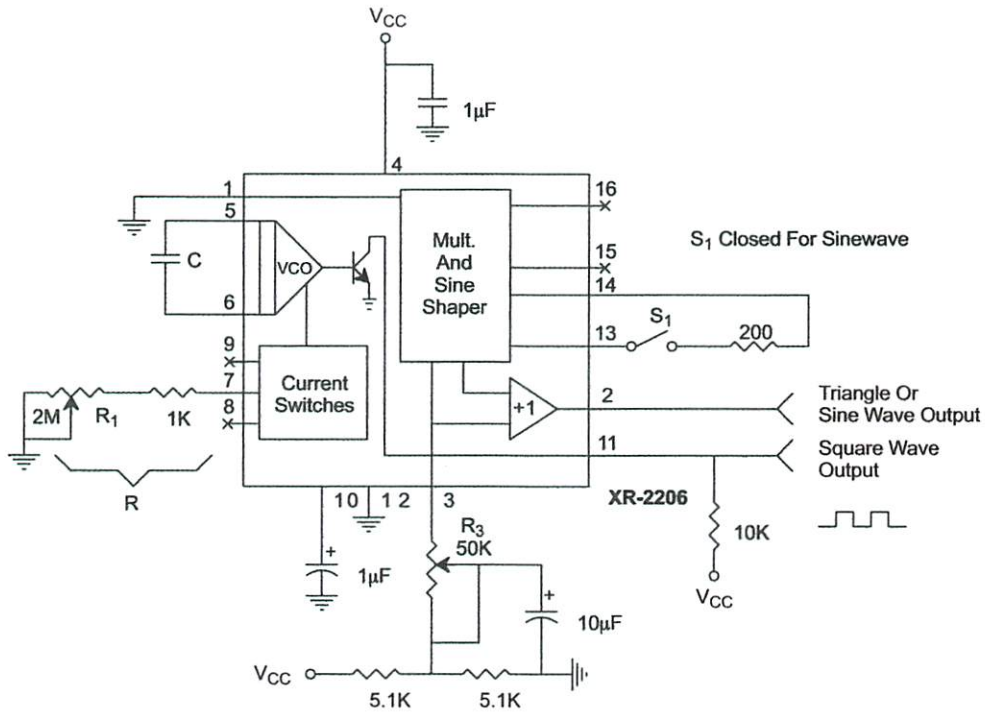


Figure 11. Circuit for Sine Wave Generation without External Adjustment. (See Figure 3 for Choice of R₃)

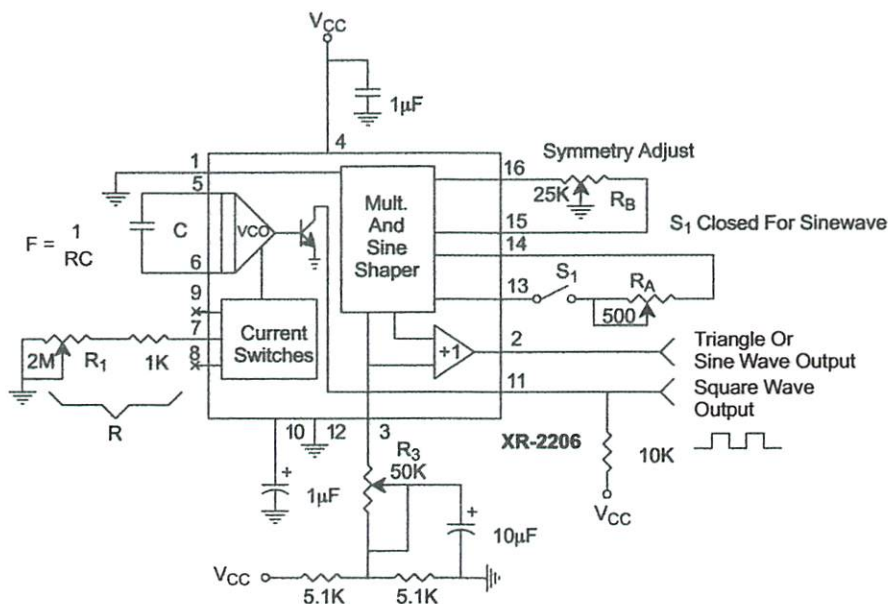


Figure 12. Circuit for Sine Wave Generation with Minimum Harmonic Distortion.
(R₃ Determines Output Swing - See Figure 3)

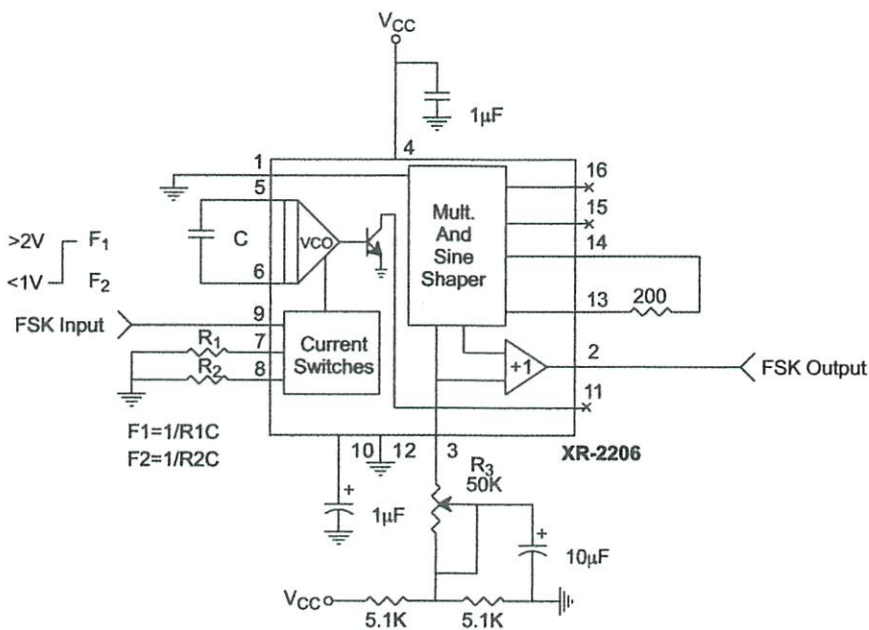


Figure 13. Sinusoidal FSK Generator

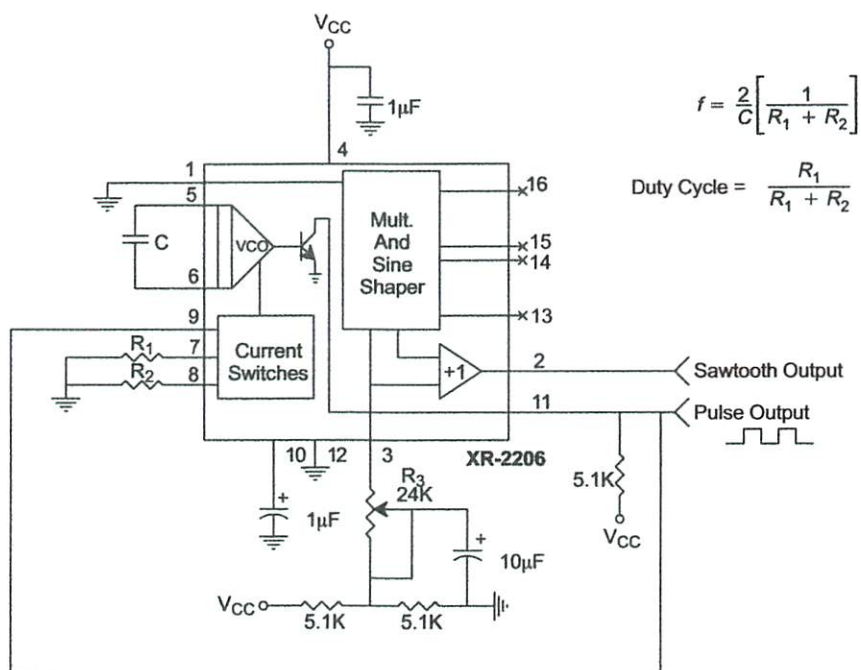


Figure 14. Circuit for Pulse and Ramp Generation.

Frequency-Shift Keying

The XR-2206 can be operated with two separate timing resistors, R_1 and R_2 , connected to the timing Pin 7 and 8, respectively, as shown in Figure 13. Depending on the polarity of the logic signal at Pin 9, either one or the other of these timing resistors is activated. If Pin 9 is open-circuited or connected to a bias voltage $\geq 2V$, only R_1 is activated. Similarly, if the voltage level at Pin 9 is $\leq 1V$, only R_2 is activated. Thus, the output frequency can be keyed between two levels, f_1 and f_2 , as:

$$f_1 = 1/R_1C \text{ and } f_2 = 1/R_2C$$

For split-supply operation, the keying voltage at Pin 9 is referenced to V^- .

Output DC Level Control

The dc level at the output (Pin 2) is approximately the same as the dc bias at Pin 3. In Figure 11, Figure 12 and Figure 13, Pin 3 is biased midway between V^+ and ground, to give an output dc level of $\approx V^+/2$.

APPLICATIONS INFORMATION

Sine Wave Generation

Without External Adjustment

Figure 11 shows the circuit connection for generating a sinusoidal output from the XR-2206. The potentiometer, R_1 at Pin 7, provides the desired frequency tuning. The maximum output swing is greater than $V^+/2$, and the typical distortion (THD) is $< 2.5\%$. If lower sine wave distortion is desired, additional adjustments can be provided as described in the following section.

The circuit of Figure 11 can be converted to split-supply operation, simply by replacing all ground connections with V^- . For split-supply operation, R_3 can be directly connected to ground.

With External Adjustment:

The harmonic content of sinusoidal output can be reduced to -0.5% by additional adjustments as shown in Figure 12. The potentiometer, R_A , adjusts the wave-shaping resistor, and R_B provides the fine adjustment for the waveform symmetry. The adjustment procedure is as follows:

Set R_B at midpoint and adjust R_A for minimum distortion.

With R_A set as above, adjust R_B to further reduce distortion.

Triangle Wave Generation

The circuits of Figure 11 and Figure 12 can be converted to triangle wave generation, by simply open-circuiting Pin 13 and 14 (i.e., S_1 open). Amplitude of the triangle is approximately twice the sine wave output.

FSK Generation

Figure 13 shows the circuit connection for sinusoidal FSK signal operation. Mark and space frequencies can be independently adjusted by the choice of timing resistors, R_1 and R_2 ; the output is phase-continuous during transitions. The keying signal is applied to Pin 9. The circuit can be converted to split-supply operation by simply replacing ground with V^- .

Pulse and Ramp Generation

Figure 14 shows the circuit for pulse and ramp waveform generation. In this mode of operation, the FSK keying terminal (Pin 9) is shorted to the square-wave output (Pin 10), and the circuit automatically frequency-shift keys itself between two separate frequencies during the positive-going and negative-going output waveforms. The pulse width and duty cycle can be adjusted from 1% to 99% by the choice of R_1 and R_2 . The values of R_1 and R_2 should be in the range of $1k\Omega$ to $2M\Omega$.

PRINCIPLES OF OPERATION**Description of Controls****Frequency of Operation:**

The frequency of oscillation, f_0 , is determined by the external timing capacitor, C , across Pin 5 and 6, and by the timing resistor, R , connected to either Pin 7 or 8. The frequency is given as:

$$f_0 = \frac{1}{RC} \text{ Hz}$$

and can be adjusted by varying either R or C . The recommended values of R , for a given frequency range, as shown in Figure 5. Temperature stability is optimum for $4k\Omega < R < 200k\Omega$. Recommended values of C are from $1000pF$ to $100\mu F$.

Frequency Sweep and Modulation:

Frequency of oscillation is proportional to the total timing current, I_T , drawn from Pin 7 or 8:

$$f = \frac{320I_T(\text{mA})}{C(\mu F)} \text{ Hz}$$

Timing terminals (Pin 7 or 8) are low-impedance points, and are internally biased at +3V, with respect to Pin 12. Frequency varies linearly with I_T , over a wide range of current values, from $1\mu A$ to $3mA$. The frequency can be controlled by applying a control voltage, V_C , to the activated timing pin as shown in Figure 10. The frequency of oscillation is related to V_C as:

$$f = \frac{1}{RC} \left(1 + \frac{R}{R_c} \left(1 - \frac{V_C}{3} \right) \right) \text{ Hz}$$

where V_C is in volts. The voltage-to-frequency conversion gain, K , is given as:

$$K = \partial f / \partial V_C = -\frac{0.32}{R_c C} \text{ Hz/V}$$

CAUTION: For safety operation of the circuit, I_T should be limited to $\leq 3mA$.

Output Amplitude:

Maximum output amplitude is inversely proportional to the external resistor, R_3 , connected to Pin 3 (see Figure 3). For sine wave output, amplitude is approximately 60mV peak per $k\Omega$ of R_3 ; for triangle, the peak amplitude is approximately 160mV peak per $k\Omega$ of R_3 . Thus, for example, $R_3 = 50k\Omega$ would produce approximately 13V sinusoidal output amplitude.

Amplitude Modulation:

Output amplitude can be modulated by applying a dc bias and a modulating signal to Pin 1. The internal impedance

at Pin 1 is approximately $100k\Omega$. Output amplitude varies linearly with the applied voltage at Pin 1, for values of dc bias at this pin, within 14 volts of $V_{CC}/2$ as shown in Figure 6. As this bias level approaches $V_{CC}/2$, the phase of the output signal is reversed, and the amplitude goes through zero. This property is suitable for phase-shift keying and suppressed-carrier AM generation. Total dynamic range of amplitude modulation is approximately 55dB.

CAUTION: AM control must be used in conjunction with a well-regulated supply, since the output amplitude now becomes a function of V_{CC} .

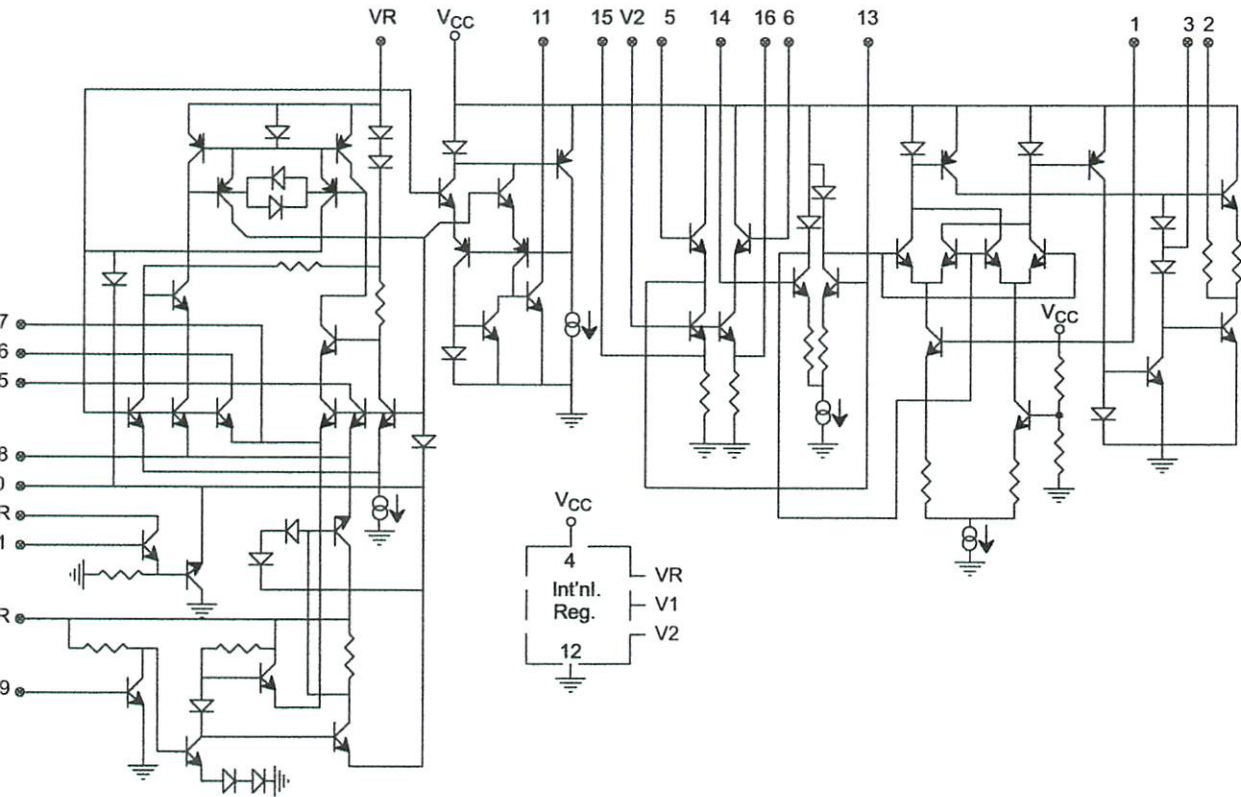
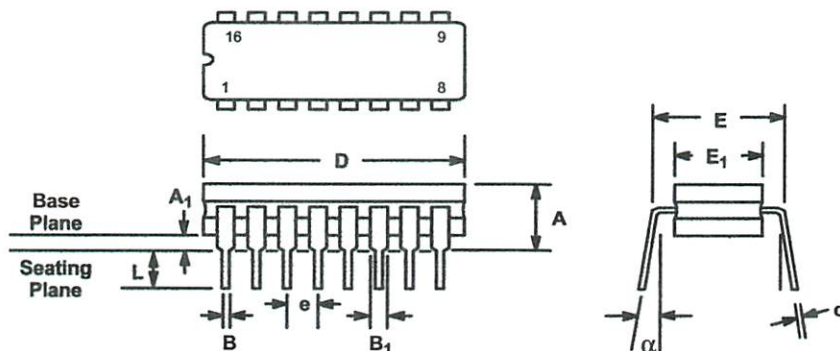


Figure 15. Equivalent Schematic Diagram

16 LEAD CERAMIC DUAL-IN-LINE
(300 MIL CDIP)

Rev. 1.00

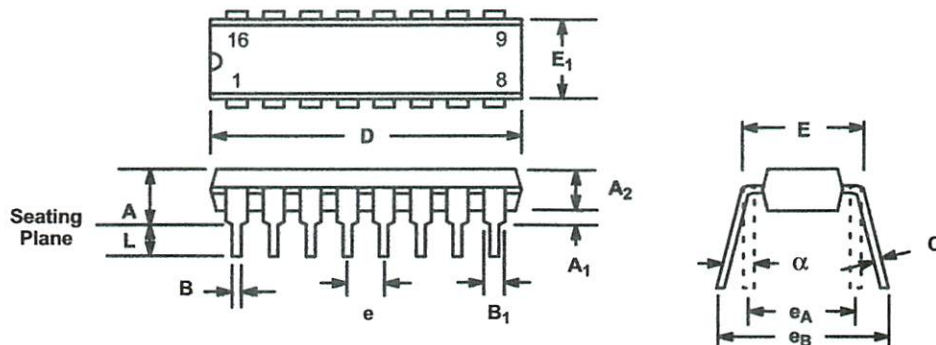


SYMBOL	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.100	0.200	2.54	5.08
A ₁	0.015	0.060	0.38	1.52
B	0.014	0.026	0.36	0.66
B ₁	0.045	0.065	1.14	1.65
c	0.008	0.018	0.20	0.46
D	0.740	0.840	18.80	21.34
E ₁	0.250	0.310	6.35	7.87
E	0.300 BSC		7.62 BSC	
e	0.100 BSC		2.54 BSC	
L	0.125	0.200	3.18	5.08
α	0°	15°	0°	15°

Note: The control dimension is the inch column

**16 LEAD PLASTIC DUAL-IN-LINE
(300 MIL PDIP)**

Rev. 1.00

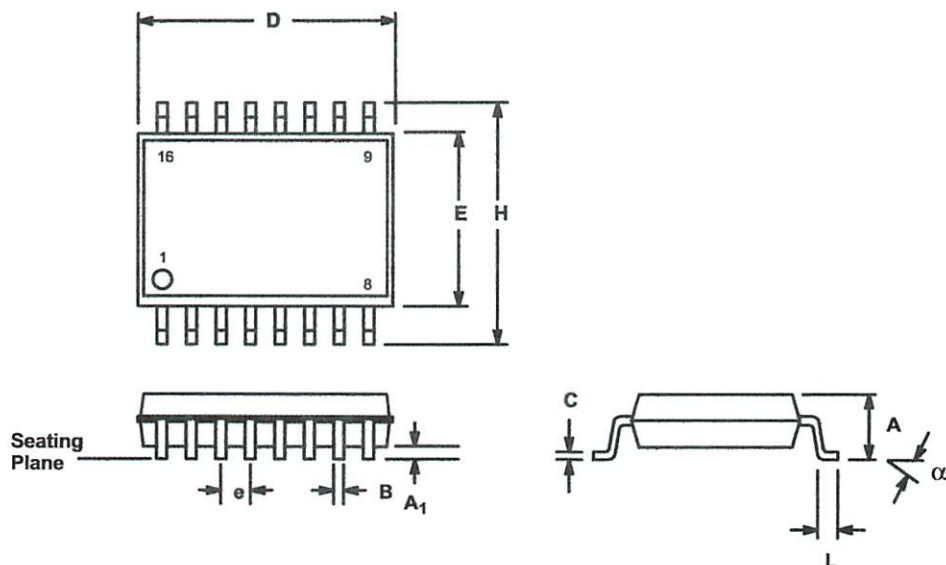


SYMBOL	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.145	0.210	3.68	5.33
A ₁	0.015	0.070	0.38	1.78
A ₂	0.115	0.195	2.92	4.95
B	0.014	0.024	0.36	0.56
B ₁	0.030	0.070	0.76	1.78
C	0.008	0.014	0.20	0.38
D	0.745	0.840	18.92	21.34
E	0.300	0.325	7.62	8.26
E ₁	0.240	0.280	6.10	7.11
e	0.100 BSC		2.54 BSC	
e _A	0.300 BSC		7.62 BSC	
e _B	0.310	0.430	7.87	10.92
L	0.115	0.160	2.92	4.06
α	0°	15°	0°	15°

Note: The control dimension is the inch column

**16 LEAD SMALL OUTLINE
(300 MIL JEDEC SOIC)**

Rev. 1.00



SYMBOL	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.093	0.104	2.35	2.65
A ₁	0.004	0.012	0.10	0.30
B	0.013	0.020	0.33	0.51
C	0.009	0.013	0.23	0.32
D	0.398	0.413	10.10	10.50
E	0.291	0.299	7.40	7.60
e	0.050 BSC		1.27 BSC	
H	0.394	0.419	10.00	10.65
L	0.016	0.050	0.40	1.27
α	0°	8°	0°	8°

Note: The control dimension is the millimeter column

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Features

- Compatible with MCS-51™ Products
- 8K Bytes of In-System Reprogrammable Downloadable Flash Memory
- 3-Wire SPI Serial Interface for Program Downloading
- Endurance: 1,000 Write/Erase Cycles
- 1K Bytes EEPROM
- Endurance: 100,000 Write/Erase Cycles
- 1.8V to 6V Operating Range
- Low-Power Static Operation: 0 Hz to 24 MHz
- Two-Level Program Memory Lock
- 64 x 8-bit Internal RAM
- 8 Programmable I/O Lines
- Three 16-bit Timer/Counters
- 6 Interrupt Sources
- Programmable UART Serial Channel
- 1-Wire Serial Interface
- Low-Power Idle and Power-down Modes
- Interrupt Recovery From Power-down
- Programmable Watchdog Timer
- 2 Data Pointers
- Power-off Flag

Description

AT89S8252 is a low-power, high-performance CMOS 8-bit microcomputer with 8K bytes of downloadable Flash programmable and erasable read only memory and 1K bytes of EEPROM. The device is manufactured using Atmel's high-density nonvolatile memory technology and is compatible with the industry-standard 80C51 instruction set and pinout. The on-chip downloadable Flash allows the program memory to be reprogrammed in-system through an SPI serial interface or by a conventional nonvolatile memory programmer. By combining a versatile 8-bit CPU with 8K bytes of downloadable Flash on a monolithic chip, the Atmel AT89S8252 is a powerful microcomputer which provides a highly-flexible and cost-effective solution to many embedded control applications.

AT89S8252 provides the following standard features: 8K bytes of downloadable Flash, 1K bytes of EEPROM, 256 bytes of RAM, 32 I/O lines, programmable watch-dog timer, two data pointers, three 16-bit timer/counters, a six-vector two-level interrupt architecture, a full duplex serial port, on-chip oscillator, and clock circuitry. In addition, the AT89S8252 is designed with static logic for operation down to zero frequency and supports two software selectable power saving modes. The Idle Mode allows the CPU to be shut down to greatly reduce power consumption while allowing the RAM, timer/counters, serial port, and interrupt system to continue functioning. The Power-down mode saves the RAM contents but disables the oscillator, disabling all other chip functions until the next interrupt or hardware reset.

The 8K bytes of downloadable Flash can be changed a single byte at a time and is accessible through the SPI serial interface. Holding RESET active forces the SPI bus into a serial programming interface and allows the program memory to be written to or read from. Once Lock Bit 2 has been activated.



8-bit Microcontroller with 8K Bytes Flash

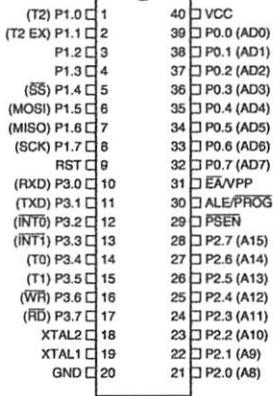
AT89S8252

Rev. 0401E-02/00

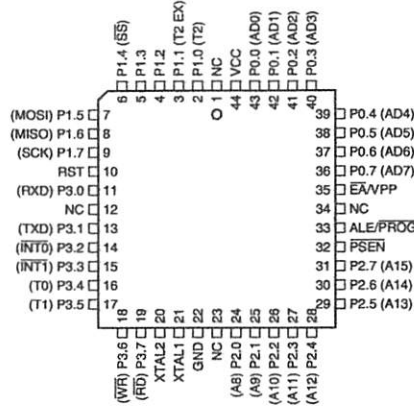


Configurations

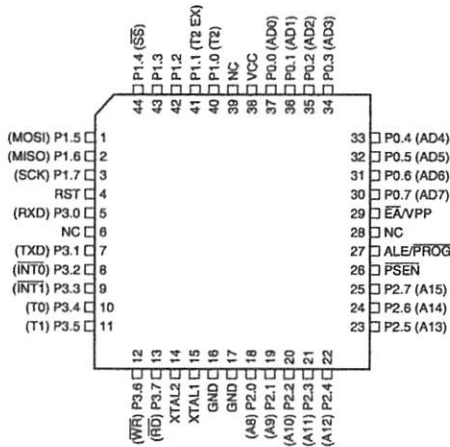
PDIP



PLCC



PQFP/TQFP



Description

ly voltage.

nd.

g

is an 8-bit open drain bi-directional I/O port. As an output port, each pin can sink eight TTL inputs. When 1s are written to port 0 pins, the pins can be used as high-impedance inputs.

can also be configured to be the multiplexed low-impedance address/data bus during accesses to external

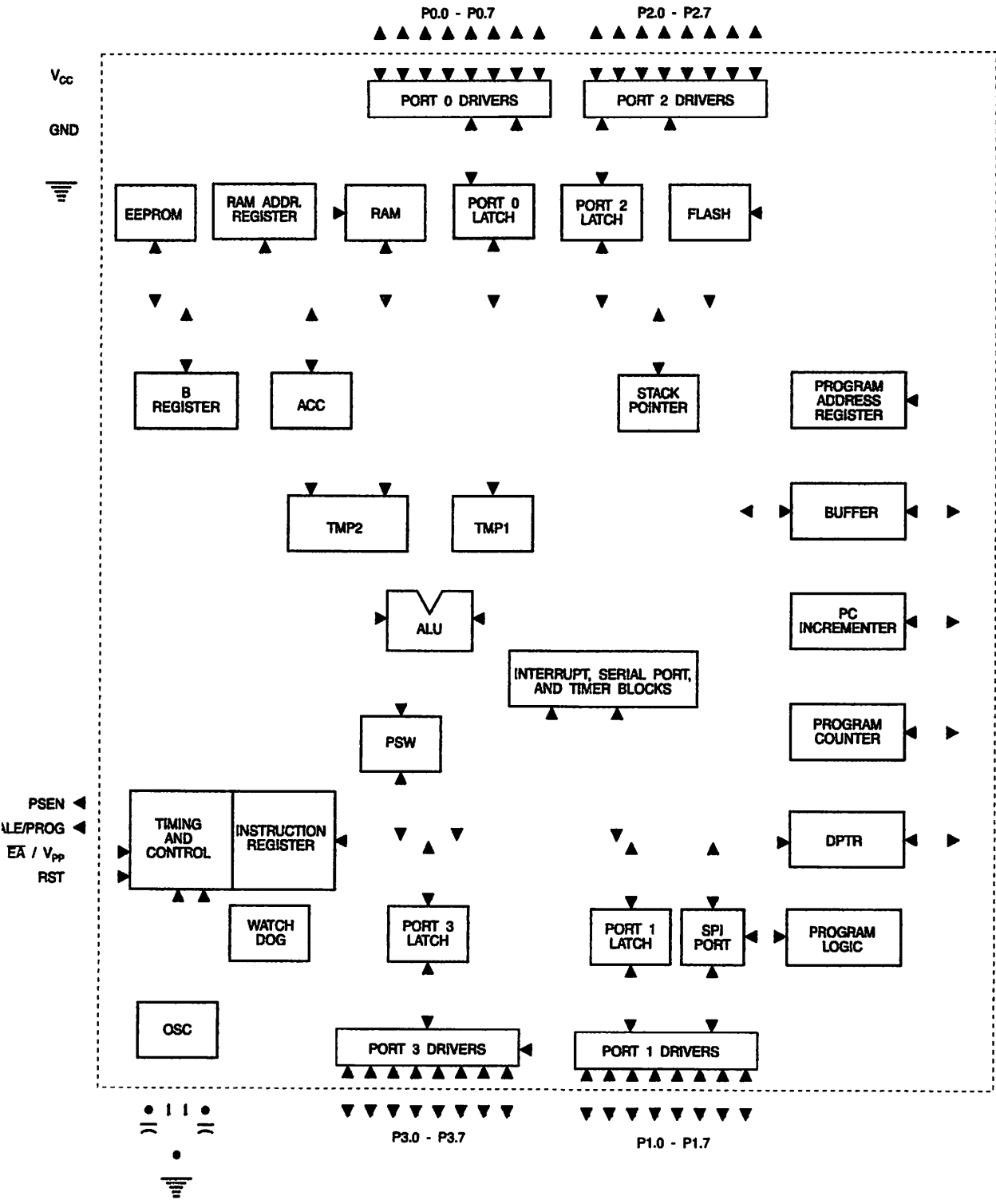
program and data memory. In this mode, P0 has internal pullups.

Port 0 also receives the code bytes during Flash programming and outputs the code bytes during program verification. External pullups are required during program verification.

Port 1

Port 1 is an 8-bit bi-directional I/O port with internal pullups. The Port 1 output buffers can sink/source four TTL inputs. When 1s are written to Port 1 pins, they are pulled high by the internal pullups and can be used as inputs. As inputs, Port 1 pins that are externally being pulled low will source current (I_{IL}) because of the internal pullups.

Block Diagram



Port 1 pins provide additional functions. P1.0 and P1.1 can be configured to be the timer/counter 2 external input (P1.0/T2) and the timer/counter 2 trigger input (P1.1/T2EX), respectively.

Description

Furthermore, P1.4, P1.5, P1.6, and P1.7 can be configured as the SPI slave port select, data input/output and shift clock input/output pins as shown in the following table.

Pin	Alternate Functions
P1.0	T2 (external count input to Timer/Counter 2), clock-out
P1.1	T2EX (Timer/Counter 2 capture/reload trigger and direction control)
P1.4	\overline{SS} (Slave port select input)
P1.5	MOSI (Master data output, slave data input pin for SPI channel)
P1.6	MISO (Master data input, slave data output pin for SPI channel)
P1.7	SCK (Master clock output, slave clock input pin for SPI channel)

Port 2 also receives the low-order address bytes during Flash programming and verification.

Port 2 is an 8-bit bi-directional I/O port with internal pullups. When Port 2 output buffers are sink/source four TTL inputs. When 1s are written to Port 2 pins, they are pulled high by internal pullups and can be used as inputs. As inputs, Port 2 pins that are externally being pulled low will source current (I_{IL}) because of the internal pullups.

Port 2 emits the high-order address byte during fetches from external program memory and during accesses to external data memory that use 16-bit addresses (MOVX @ DPTR). In this application, Port 2 uses strong internal pullups when emitting 1s. During accesses to external data memory that use 8-bit addresses (MOVX @ RI), Port 2 outputs the contents of the P2 Special Function Register.

Port 2 also receives the high-order address bits and some control signals during Flash programming and verification.

Port 3 is an 8 bit bi-directional I/O port with internal pullups. When Port 3 output buffers are sink/source four TTL inputs. When 1s are written to Port 3 pins, they are pulled high by internal pullups and can be used as inputs. As inputs,

Port 3 pins that are externally being pulled low will source current (I_{IL}) because of the pullups.

Port 3 also serves the functions of various special features of the AT89S8252, as shown in the following table.

Port 3 also receives some control signals for Flash programming and verification.

Port Pin	Alternate Functions
P3.0	RXD (serial input port)
P3.1	TXD (serial output port)
P3.2	$\overline{INT0}$ (external interrupt 0)
P3.3	$\overline{INT1}$ (external interrupt 1)
P3.4	T0 (timer 0 external input)
P3.5	T1 (timer 1 external input)
P3.6	\overline{WR} (external data memory write strobe)
P3.7	\overline{RD} (external data memory read strobe)

RST

Reset input. A high on this pin for two machine cycles while the oscillator is running resets the device.

ALE/PROG

Address Latch Enable is an output pulse for latching the low byte of the address during accesses to external memory. This pin is also the program pulse input (PROG) during Flash programming.

In normal operation, ALE is emitted at a constant rate of 1/6 the oscillator frequency and may be used for external timing or clocking purposes. Note, however, that one ALE pulse is skipped during each access to external data memory.

If desired, ALE operation can be disabled by setting bit 0 of SFR location 8EH. With the bit set, ALE is active only during a MOVX or MOVC instruction. Otherwise, the pin is weakly pulled high. Setting the ALE-disable bit has no effect if the microcontroller is in external execution mode.

\overline{PSEN}

Program Store Enable is the read strobe to external program memory.

When the AT89S8252 is executing code from external program memory, \overline{PSEN} is activated twice each machine cycle, except that two \overline{PSEN} activations are skipped during each access to external data memory.

\overline{EA}/VPP

External Access Enable. \overline{EA} must be strapped to GND in order to enable the device to fetch code from external pro-

memory locations starting at 0000H up to FFFFH. however, that if lock bit 1 is programmed, $\bar{E}A$ will be all latched on reset.

ould be strapped to V_{CC} for internal program execu- . This pin also receives the 12-volt programming e voltage (V_{pp}) during Flash programming when 12- rogramming is selected.

XTAL1

Input to the inverting oscillator amplifier and input to the internal clock operating circuit.

XTAL2

Output from the inverting oscillator amplifier.

1. AT89S8252 SFR Map and Reset Values

								0FFH
B 00000000								0F7H
								0EFH
ACC 00000000								0E7H
								0DFH
PSW 00000000					SPCR 000001XX			0D7H
T2CON 00000000	T2MOD XXXXXXXX00	RCAP2L 00000000	RCAP2H 00000000	TL2 00000000	TH2 00000000			0CFH
								0C7H
IP XX000000								0BFH
P3 11111111								0B7H
IE 0X000000		SPSR 00XXXXXX						0AFH
P2 11111111								0A7H
SCON 00000000	SBUF XXXXXXXX							9FH
P1 11111111						WMCON 00000010		97H
TCON 00000000	TMOD 00000000	TL0 00000000	TL1 00000000	TH0 00000000	TH1 00000000			8FH
P0 11111111	SP 00000111	DP0L 00000000	DP0H 00000000	DP1L 00000000	DP1H 00000000	SPDR XXXXXXXX	PCON 0XXX0000	87H



Special Function Registers

of the on-chip memory area called the Special Function Register (SFR) space is shown in Table 1.

That not all of the addresses are occupied, and unoccupied addresses may not be implemented on the chip. Accesses to these addresses will in general return random data, and write accesses will have an indeterminate effect.

Software should not write 1s to these unlisted

locations, since they may be used in future products to invoke new features. In that case, the reset or inactive values of the new bits will always be 0.

Timer 2 Registers Control and status bits are contained in registers T2CON (shown in Table 2) and T2MOD (shown in Table 9) for Timer 2. The register pair (RCAP2H, RCAP2L) are the Capture/Reload registers for Timer 2 in 16-bit capture mode or 16-bit auto-reload mode.

2. T2CON—Timer/Counter 2 Control Register

I/O Address = 0C8H						Reset Value = 0000 000B	
Addressable							
TF2	EXF2	RCLK	TCLK	EXEN2	TR2	C/̄T2	CP/̄RL2
7	6	5	4	3	2	1	0

Bit	Function
7	Timer 2 overflow flag set by a Timer 2 overflow and must be cleared by software. TF2 will not be set when either RCLK = 1 or TCLK = 1.
6	Timer 2 external flag set when either a capture or reload is caused by a negative transition on T2EX and EXEN2 = 1. When Timer 2 interrupt is enabled, EXF2 = 1 will cause the CPU to vector to the Timer 2 interrupt routine. EXF2 must be cleared by software. EXF2 does not cause an interrupt in up/down counter mode (DCEN = 1).
5	Receive clock enable. When set, causes the serial port to use Timer 2 overflow pulses for its receive clock in serial port Modes 1 and 3. RCLK = 0 causes Timer 1 overflows to be used for the receive clock.
4	Transmit clock enable. When set, causes the serial port to use Timer 2 overflow pulses for its transmit clock in serial port Modes 1 and 3. TCLK = 0 causes Timer 1 overflows to be used for the transmit clock.
3	Timer 2 external enable. When set, allows a capture or reload to occur as a result of a negative transition on T2EX if Timer 2 is not being used to clock the serial port. EXEN2 = 0 causes Timer 2 to ignore events at T2EX.
2	Start/Stop control for Timer 2. TR2 = 1 starts the timer.
1	Timer or counter select for Timer 2. C/̄T2 = 0 for timer function. C/̄T2 = 1 for external event counter (falling edge triggered).
0	Capture/Reload select. CP/̄RL2 = 1 causes captures to occur on negative transitions at T2EX if EXEN2 = 1. CP/̄RL2 = 0 causes automatic reloads to occur when Timer 2 overflows or negative transitions occur at T2EX when EXEN2 = 1. When either RCLK or TCLK = 1, this bit is ignored and the timer is forced to auto-reload on Timer 2 overflow.

Watchdog and Memory Control Register The WMCON register contains control bits for the Watchdog Timer (shown in Table 3). The EEMEN and EEMWE bits are used

to select the 2K bytes on-chip EEPROM, and to enable byte-write. The DPS bit selects one of two DPTR registers available.

3. WMCON—Watchdog and Memory Control Register

WMCON Address = 96H

Reset Value = 0000 0010B

PS2	PS1	PS0	EEMWE	EEMEN	DPS	WDTRST	WDTEN
7	6	5	4	3	2	1	0

Bit	Function
PS2, PS1, PS0	Prescaler Bits for the Watchdog Timer. When all three bits are set to "0", the watchdog timer has a nominal period of 16 ms. When all three bits are set to "1", the nominal period is 2048 ms.
EEMWE	EEPROM Data Memory Write Enable Bit. Set this bit to "1" before initiating byte write to on-chip EEPROM with the MOVX instruction. User software should set this bit to "0" after EEPROM write is completed.
EEMEN	Internal EEPROM Access Enable. When EEMEN = 1, the MOVX instruction with DPTR will access on-chip EEPROM instead of external data memory. When EEMEN = 0, MOVX with DPTR accesses external data memory.
DPS	Data Pointer Register Select. DPS = 0 selects the first bank of Data Pointer Register, DP0, and DPS = 1 selects the second bank, DP1
WDTRST RDY/ \overline{BSY}	Watchdog Timer Reset and EEPROM Ready/ \overline{Busy} Flag. Each time this bit is set to "1" by user software, a pulse is generated to reset the watchdog timer. The WDTRST bit is then automatically reset to "0" in the next instruction cycle. The WDTRST bit is Write-Only. This bit also serves as the RDY/ \overline{BSY} flag in a Read-Only mode during EEPROM write. RDY/ \overline{BSY} = 1 means that the EEPROM is ready to be programmed. While programming operations are being executed, the RDY/ \overline{BSY} bit equals "0" and is automatically reset to "1" when programming is completed.
WDTEN	Watchdog Timer Enable Bit. WDTEN = 1 enables the watchdog timer and WDTEN = 0 disables the watchdog timer.

Serial Peripheral Interface Registers Control and status bits for the Serial Peripheral Interface are contained in registers SPCR (shown in Table 4) and SPSR (shown in Table 5). The SPI data bits are contained in the SPDR register. Writing the SPI data register during serial data transfer sets the Write Collision Flag, WCOL, in the SPSR register. The SPDR is double buffered for writing and the values in SPDR are not changed by reads.

Interrupt Registers The global interrupt enable bit and the individual interrupt enable bits are in the IE register. In addition, the individual interrupt enable bit for the SPI is in the SPCR register. Two priorities can be set for each of the interrupt sources in the IP register.

Dual Data Pointer Registers To facilitate accessing both internal EEPROM and external data memory, two banks of 16 bit Data Pointer Registers are provided: DP0 at SFR address locations 82H-83H and DP1 at 84H-85H. Bit DPS = 0 in SFR WMCON selects DP0 and DPS = 1 selects DP1. The user should always initialize the DPS bit to the appropriate value before accessing the respective Data Pointer Register.

Power Off Flag The Power Off Flag (POF) is located at bit_4 (PCON.4) in the PCON SFR. POF is set to "1" during power up. It can be set and reset under software control and is not affected by RESET.





4. SPCR—SPI Control Register

Register Address = D5H

Reset Value = 0000 01XXB

SPIE	SPE	DORD	MSTR	CPOL	CPHA	SPR1	SPR0
7	6	5	4	3	2	1	0

Bit	Function
7	SPI Interrupt Enable. This bit, in conjunction with the ES bit in the IE register, enables SPI interrupts: SPIE = 1 and ES = 1 enable SPI interrupts. SPIE = 0 disables SPI interrupts.
6	SPI Enable. SPI = 1 enables the SPI channel and connects \overline{SS} , MOSI, MISO and SCK to pins P1.4, P1.5, P1.6, and P1.7. SPI = 0 disables the SPI channel.
5	Data Order. DORD = 1 selects LSB first data transmission. DORD = 0 selects MSB first data transmission.
4	Master/Slave Select. MSTR = 1 selects Master SPI mode. MSTR = 0 selects Slave SPI mode.
3	Clock Polarity. When CPOL = 1, SCK is high when idle. When CPOL = 0, SCK of the master device is low when not transmitting. Please refer to figure on SPI Clock Phase and Polarity Control.
2	Clock Phase. The CPHA bit together with the CPOL bit controls the clock and data relationship between master and slave. Please refer to figure on SPI Clock Phase and Polarity Control.
1:0	SPI Clock Rate Select. These two bits control the SCK rate of the device configured as master. SPR1 and SPR0 have no effect on the slave. The relationship between SCK and the oscillator frequency, F_{OSC} , is as follows: SPR1SPR0 SCK = F_{OSC} divided by 0 0 4 0 1 16 1 0 64 1 1 128

5. SPSR – SPI Status Register

Register Address = AAH

Reset Value = 00XX XXXXB

SPIF	WCOL	–	–	–	–	–	–
7	6	5	4	3	2	1	0

Bit	Function
7	SPI Interrupt Flag. When a serial transfer is complete, the SPIF bit is set and an interrupt is generated if SPIE = 1 and ES = 1. The SPIF bit is cleared by reading the SPI status register with SPIF and WCOL bits set, and then accessing the SPI data register.
6	Write Collision Flag. The WCOL bit is set if the SPI data register is written during a data transfer. During data transfer, the result of reading the SPDR register may be incorrect, and writing to it has no effect. The WCOL bit (and the SPIF bit) are cleared by reading the SPI status register with SPIF and WCOL set, and then accessing the SPI data register.

6. SPDR – SPI Data Register

Register Address = 86H

Reset Value = unchanged

SPD7	SPD6	SPD5	SPD4	SPD3	SPD2	SPD1	SPD0
7	6	5	4	3	2	1	0

AT89S8252

Memory – EEPROM and RAM

AT89S8252 implements 2K bytes of on-chip EEPROM data storage and 256 bytes of RAM. The upper 128 bytes of RAM occupy a parallel space to the Special Function Registers. That means the upper 128 bytes have the addresses as the SFR space but are physically separated from SFR space.

When an instruction accesses an internal location above address 7FH, the address mode used in the instruction defines whether the CPU accesses the upper 128 bytes of RAM or the SFR space. Instructions that use direct addressing access SFR space.

For example, the following direct addressing instruction accesses the SFR at location 0A0H (which is P2).

```
MOV 0A0H, #data
```

Instructions that use indirect addressing access the upper 128 bytes of RAM. For example, the following indirect addressing instruction, where R0 contains 0A0H, accesses data byte at address 0A0H, rather than P2 (whose address is 0A0H).

```
MOV @R0, #data
```

Stack operations are examples of indirect addressing, so the upper 128 bytes of data RAM are available as stack space.

On-chip EEPROM data memory is selected by setting the EEMEN bit in the WMCON register at SFR address location 96H. The EEPROM address range is from 000H to 0FFH. The MOVX instructions are used to access the external IOM. To access off-chip data memory with the MOVX instructions, the EEMEN bit needs to be set to "0".

The EEMWE bit in the WMCON register needs to be set to "1" before any byte location in the EEPROM can be written. After programming, software should reset EEMWE bit to "0" if no further IOM write is required. EEPROM write cycles in the programming mode are self-timed and typically take 100 μs. The progress of EEPROM write can be monitored by reading the RDY/BSY bit (read-only) in SFR WMCON. BSY = 0 means programming is still in progress and BSY = 1 means EEPROM write cycle is completed and no further write cycle can be initiated.

In addition, during EEPROM programming, an attempted read from the EEPROM will fetch the byte being written and the MSB complemented. Once the write cycle is completed, true data are valid at all bit locations.

Programmable Watchdog Timer

The Programmable Watchdog Timer (WDT) operates from an independent oscillator. The prescaler bits, PS0, PS1, and PS2 in SFR WMCON are used to set the period of the Watchdog Timer from 16 ms to 2048 ms. The available timer periods are shown in the following table and the

actual timer periods (at $V_{CC} = 5V$) are within $\pm 30\%$ of the nominal.

The WDT is disabled by Power-on Reset and during Power-down. It is enabled by setting the WDEN bit in SFR WMCON (address = 96H). The WDT is reset by setting the WDRST bit in WMCON. When the WDT times out without being reset or disabled, an internal RST pulse is generated to reset the CPU.

Table 7. Watchdog Timer Period Selection

WDT Prescaler Bits			Period (nominal)
PS2	PS1	PS0	
0	0	0	16 ms
0	0	1	32 ms
0	1	0	64 ms
0	1	1	128 ms
1	0	0	256 ms
1	0	1	512 ms
1	1	0	1024 ms
1	1	1	2048 ms

Timer 0 and 1

Timer 0 and Timer 1 in the AT89S8252 operate the same way as Timer 0 and Timer 1 in the AT89C51, AT89C52 and AT89C55. For further information, see the October 1995 Microcontroller Data Book, page 2-45, section titled, "Timer/Counters."

Timer 2

Timer 2 is a 16 bit Timer/Counter that can operate as either a timer or an event counter. The type of operation is selected by bit C/T2 in the SFR T2CON (shown in Table 2). Timer 2 has three operating modes: capture, auto-reload (up or down counting), and baud rate generator. The modes are selected by bits in T2CON, as shown in Table 8.

Timer 2 consists of two 8-bit registers, TH2 and TL2. In the Timer function, the TL2 register is incremented every machine cycle. Since a machine cycle consists of 12 oscillator periods, the count rate is 1/12 of the oscillator frequency.

In the Counter function, the register is incremented in response to a 1-to-0 transition at its corresponding external input pin, T2. In this function, the external input is sampled during S5P2 of every machine cycle. When the samples show a high in one cycle and a low in the next cycle, the count is incremented. The new count value appears in the register during S3P1 of the cycle following the one in which



transition was detected. Since two machine cycles (24 oscillator periods) are required to recognize a 1-to-0 transition, the maximum count rate is 1/24 of the oscillator frequency. To ensure that a given level is sampled at least once before it changes, the level should be held for at least two full machine cycles.

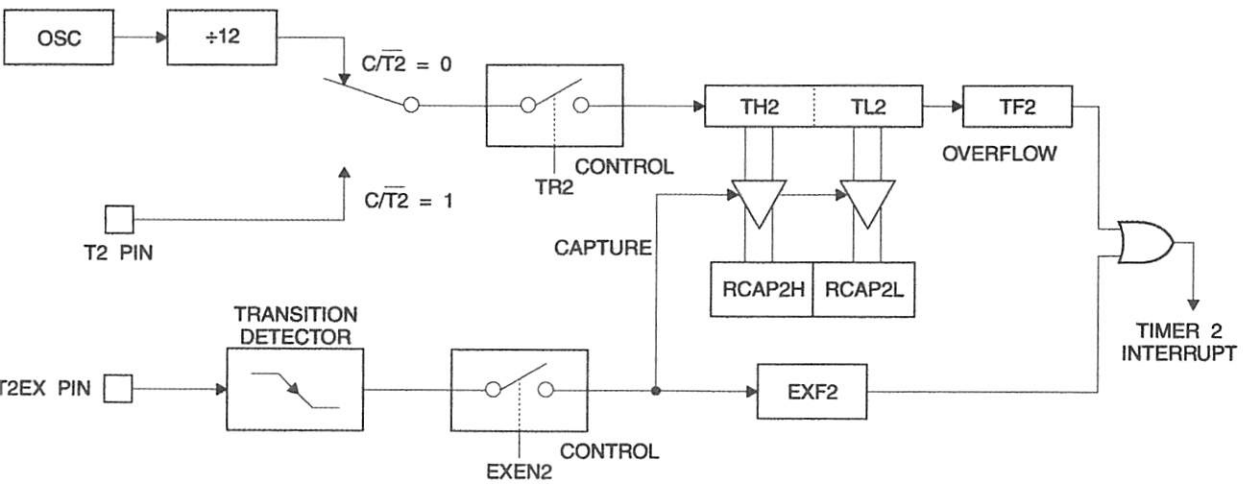
8. Timer 2 Operating Modes

CLK + TCLK	CP/RL2	TR2	MODE
0	0	1	16-bit Auto-reload
0	1	1	16-bit Capture
1	X	1	Baud Rate Generator
X	X	0	(Off)

Capture Mode

In the capture mode, two options are selected by bit EXEN2 in T2CON. If EXEN2 = 0, Timer 2 is a 16 bit timer or counter which upon overflow sets bit TF2 in T2CON. This bit can then be used to generate an interrupt. If EXEN2 = 1, Timer 2 performs the same operation, but a 1-to-0 transition at external input T2EX also causes the current value in TH2 and TL2 to be captured into RCAP2H and RCAP2L, respectively. In addition, the transition at T2EX causes bit EXF2 in T2CON to be set. The EXF2 bit, like TF2, can generate an interrupt. The capture mode is illustrated in Figure 1.

Figure 1. Timer 2 in Capture Mode



Auto-reload (Up or Down Counter)

Timer 2 can be programmed to count up or down when configured in its 16 bit auto-reload mode. This feature is enabled by the DCEN (Down Counter Enable) bit located in the T2MOD register (see Table 9). Upon reset, the DCEN bit is set to 0 so that timer 2 will default to count up. When DCEN is set, Timer 2 can count up or down, depending on the value of the T2EX pin.

Figure 2 shows Timer 2 automatically counting up when DCEN = 0. In this mode, two options are selected by bit TR2 in T2CON. If EXEN2 = 0, Timer 2 counts up to 0FFFFH and then sets the TF2 bit upon overflow. The overflow also causes the timer registers to be reloaded with the 16 bit value in RCAP2H and RCAP2L. The values in RCAP2H and RCAP2L are preset by software. If EXEN2 = 1, a 16 bit reload can be triggered either by an overflow or

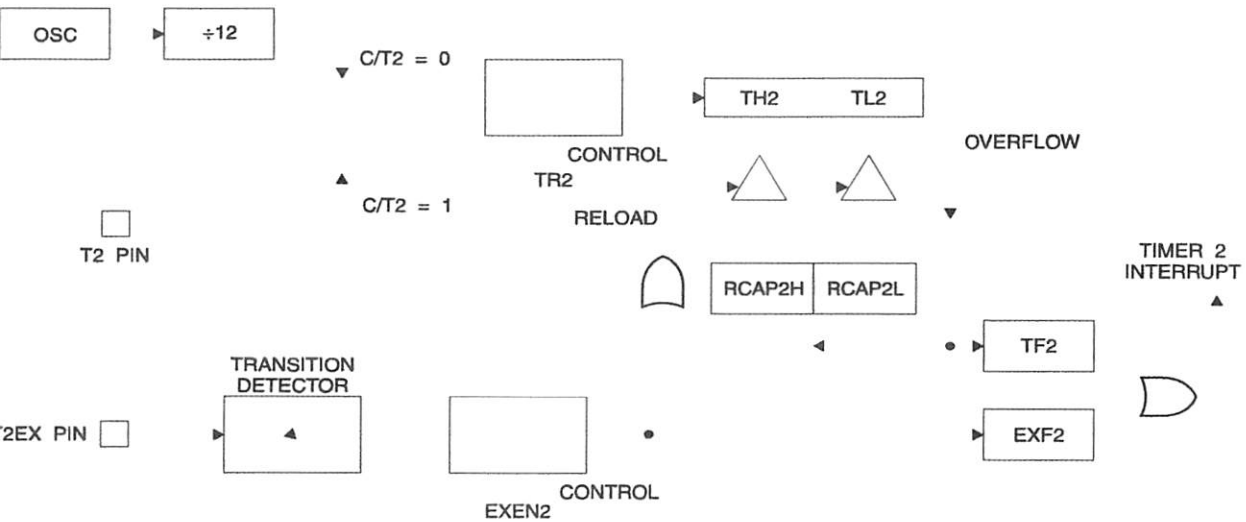
by a 1-to-0 transition at external input T2EX. This transition also sets the EXF2 bit. Both the TF2 and EXF2 bits can generate an interrupt if enabled.

Setting the DCEN bit enables Timer 2 to count up or down, as shown in Figure 3. In this mode, the T2EX pin controls the direction of the count. A logic 1 at T2EX makes Timer 2 count up. The timer will overflow at 0FFFFH and set the TF2 bit. This overflow also causes the 16 bit value in RCAP2H and RCAP2L to be reloaded into the timer registers, TH2 and TL2, respectively.

A logic 0 at T2EX makes Timer 2 count down. The timer underflows when TH2 and TL2 equal the values stored in RCAP2H and RCAP2L. The underflow sets the TF2 bit and causes 0FFFFH to be reloaded into the timer registers.

The EXF2 bit toggles whenever Timer 2 overflows or underflows and can be used as a 17th bit of resolution. In this operating mode, EXF2 does not flag an interrupt.

Figure 2. Timer 2 in Auto Reload Mode (DCEN = 0)



9. T2MOD – Timer 2 Mode Control Register

IO Address = 0C9H

Reset Value = XXXX XX00B

8-bit Addressable

7	6	5	4	3	2	1	0
-	-	-	-	-	-	T2OE	DCEN

Bit	Function
7	Not implemented, reserved for future use.
6	Timer 2 Output Enable bit.
DCEN	When set, this bit allows Timer 2 to be configured as an up/down counter.



Figure 3. Timer 2 Auto Reload Mode (DCEN = 1)

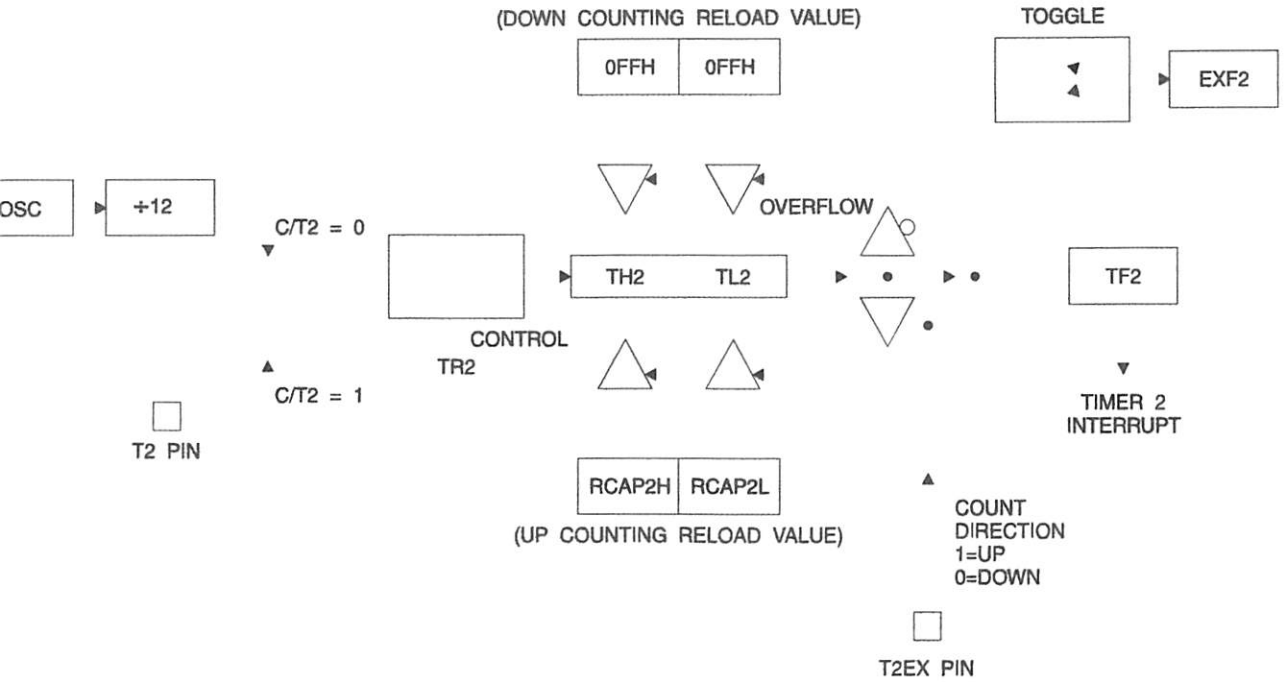
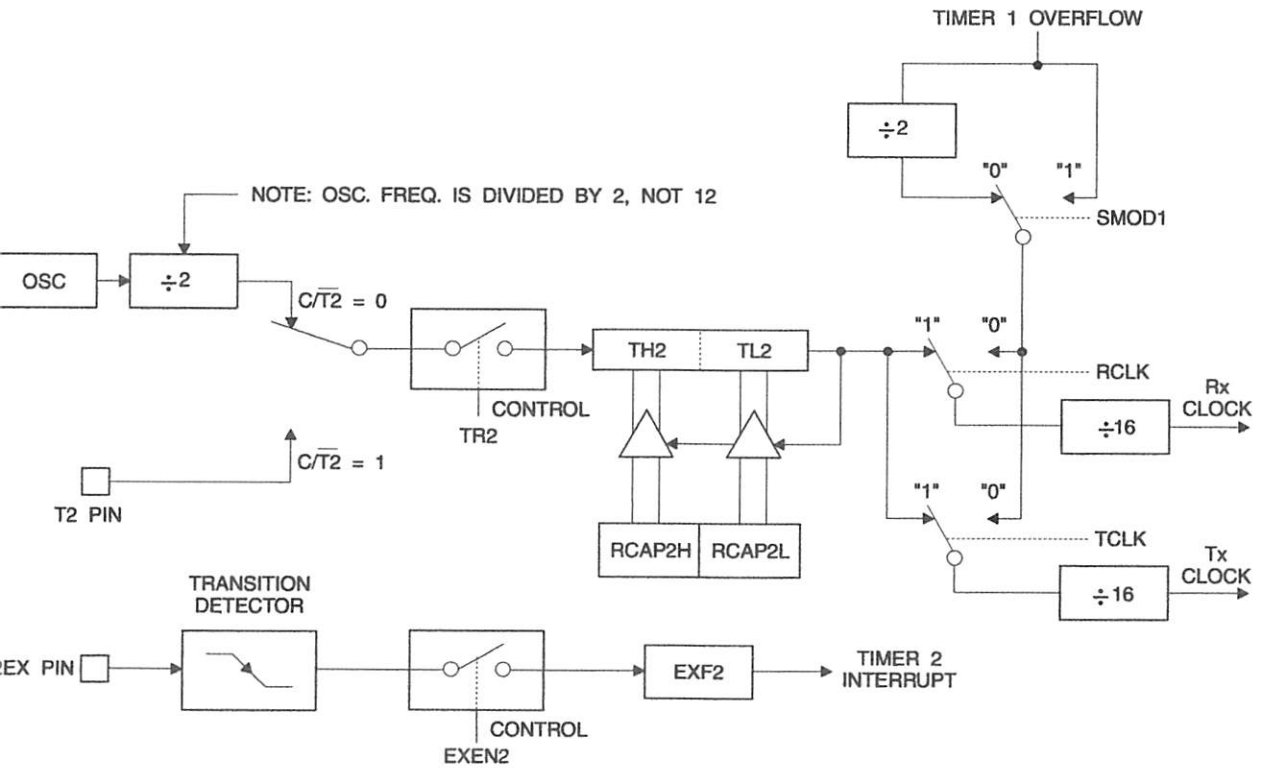


Figure 4. Timer 2 in Baud Rate Generator Mode



Baud Rate Generator

Timer 2 is selected as the baud rate generator by setting RCLK and/or TCLK in T2CON (Table 2). Note that the baud rates for transmit and receive can be different if Timer 2 is used for the receiver or transmitter and Timer 1 is used for the other function. Setting RCLK and/or TCLK puts Timer 2 into its baud rate generator mode, as shown in Figure 4.

The baud rate generator mode is similar to the auto-reload mode, in that a rollover in TH2 causes the Timer 2 registers to be reloaded with the 16 bit value in registers RCAP2H and RCAP2L, which are preset by software.

Baud rates in Modes 1 and 3 are determined by Timer 2 overflow rate according to the following equation.

$$\text{Modes 1 and 3 Baud Rates} = \frac{\text{Timer 2 Overflow Rate}}{16}$$

Timer 2 can be configured for either timer or counter operation. In most applications, it is configured for timer operation ($CP/\overline{T2} = 0$). The timer operation is different for Timer 2 when it is used as a baud rate generator. Normally, as a timer, it increments every machine cycle (at 1/12 the oscillator frequency). As a baud rate generator, however, it increments every state time (at 1/2 the oscillator frequency). The baud rate formula is given below.

$$\text{Modes 1 and 3 Baud Rate} = \frac{\text{Oscillator Frequency}}{32 \times [65536 - (\text{RCAP2H}, \text{RCAP2L})]}$$

(RCAP2H, RCAP2L) is the content of RCAP2H and RCAP2L taken as a 16 bit unsigned integer.

Timer 2 as a baud rate generator is shown in Figure 4. This mode is valid only if RCLK or TCLK = 1 in T2CON. Note that a rollover in TH2 does not set TF2 and will not generate an interrupt. Note also, that if EXEN2 is set, a 1-to-0 transition in T2EX will set EXF2 but will not cause a reload of (RCAP2H, RCAP2L) to (TH2, TL2). This timer timer

2 is in use as a baud rate generator, T2EX can be used as an extra external interrupt.

Note that when Timer 2 is running ($TR2 = 1$) as a timer in the baud rate generator mode, TH2 or TL2 should not be read from or written to. Under these conditions, the Timer is incremented every state time, and the results of a read or write may not be accurate. The RCAP2 registers may be read but should not be written to, because a write might overlap a reload and cause write and/or reload errors. The timer should be turned off (clear TR2) before accessing the Timer 2 or RCAP2 registers.

Programmable Clock Out

A 50% duty cycle clock can be programmed to come out on P1.0, as shown in Figure 5. This pin, besides being a regular I/O pin, has two alternate functions. It can be programmed to input the external clock for Timer/Counter 2 or to output a 50% duty cycle clock ranging from 61 Hz to 4 MHz at a 16 MHz operating frequency.

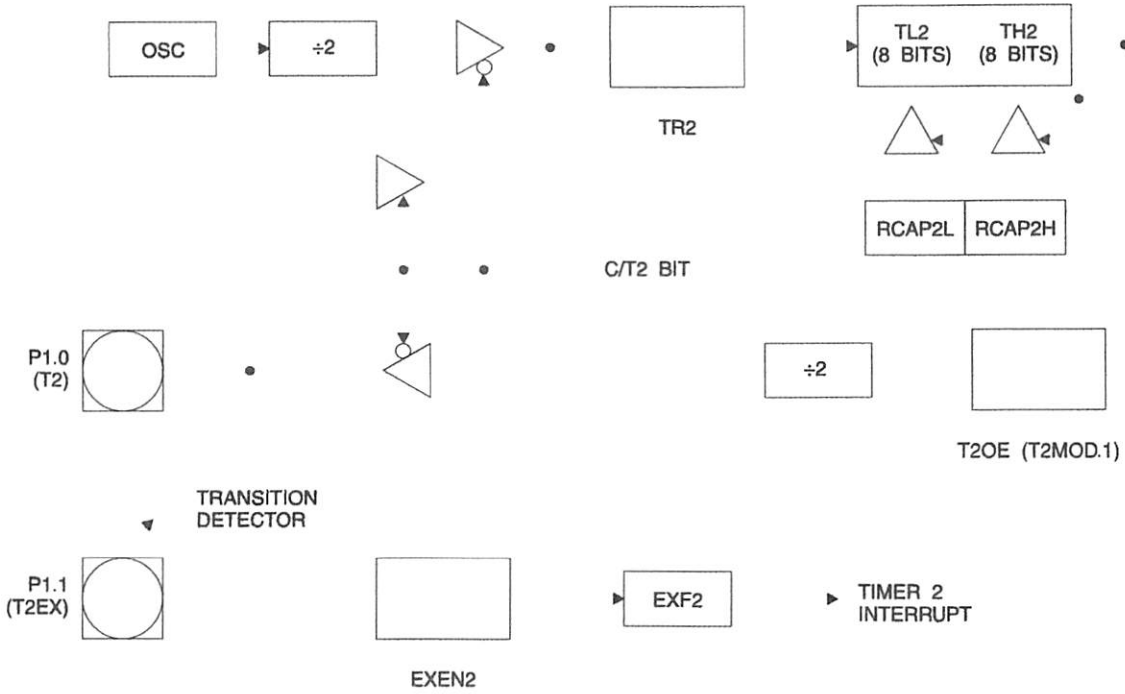
To configure the Timer/Counter 2 as a clock generator, bit $C/\overline{T2}$ (T2CON.1) must be cleared and bit T2OE (T2MOD.1) must be set. Bit TR2 (T2CON.2) starts and stops the timer.

The clock-out frequency depends on the oscillator frequency and the reload value of Timer 2 capture registers (RCAP2H, RCAP2L), as shown in the following equation.

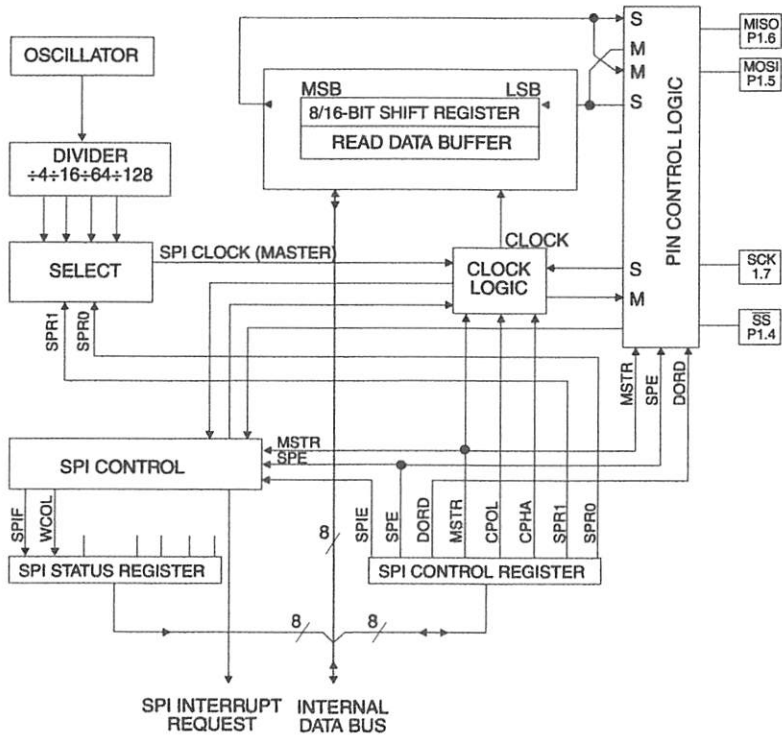
$$\text{Clock Out Frequency} = \frac{\text{Oscillator Frequency}}{4 \times [65536 - (\text{RCAP2H}, \text{RCAP2L})]}$$

In the clock-out mode, Timer 2 rollovers will not generate an interrupt. This behavior is similar to when Timer 2 is used as a baud-rate generator. It is possible to use Timer 2 as a baud-rate generator and a clock generator simultaneously. Note, however, that the baud-rate and clock-out frequencies cannot be determined independently from one another since they both use RCAP2H and RCAP2L.

e 5. Timer 2 in Clock-out Mode



e 6. SPI Block Diagram



RT

UART in the AT89S8252 operates the same way as UART in the AT89C51, AT89C52 and AT89C55. For more information, see the October 1995 Microcontroller Handbook, page 2-49, section titled, "Serial Interface."

Serial Peripheral Interface

The serial peripheral interface (SPI) allows high-speed synchronous data transfer between the AT89S8252 and other peripheral devices or between several AT89S8252 microcontrollers. The AT89S8252 SPI features include the following:

- Full-Duplex, 3-Wire Synchronous Data Transfer
- Master or Slave Operation
- 10 MHz Bit Frequency (max.)
- MSB First or MSB First Data Transfer
- Four Programmable Bit Rates
- End of Transmission Interrupt Flag

Figure 7. SPI Master-slave Interconnection

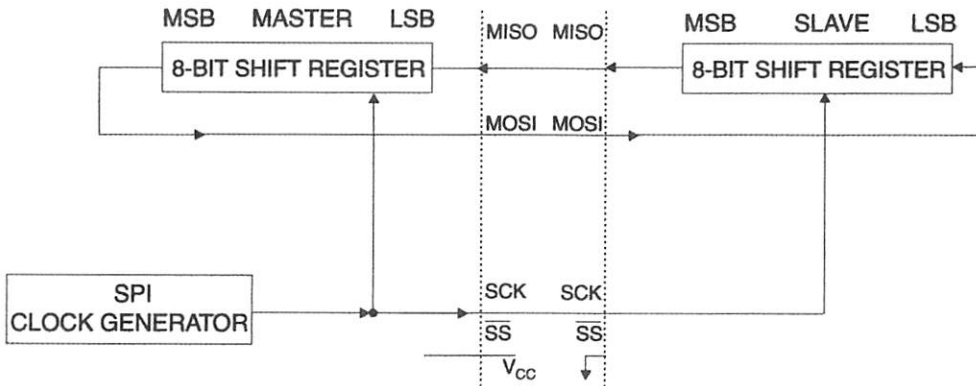
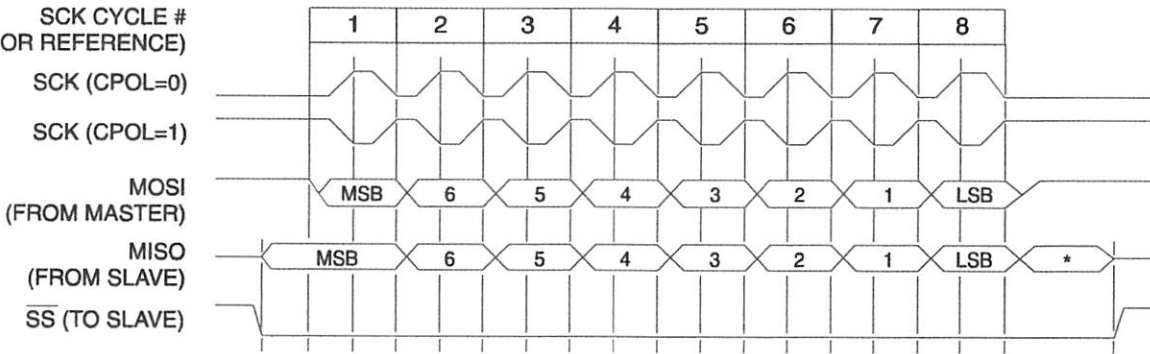


Figure 8. SPI transfer Format with CPHA = 0



defined but normally MSB of character just received

- Write Collision Flag Protection
- Wakeup from Idle Mode (Slave Mode Only)

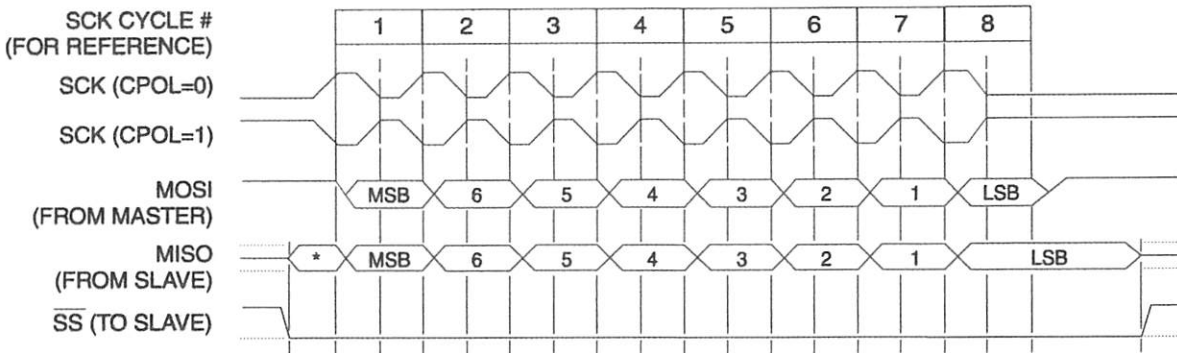
The interconnection between master and slave CPUs with SPI is shown in the following figure. The SCK pin is the clock output in the master mode but is the clock input in the slave mode. Writing to the SPI data register of the master CPU starts the SPI clock generator, and the data written shifts out of the MOSI pin and into the MISO pin of the slave CPU. After shifting one byte, the SPI clock generator stops, setting the end of transmission flag (SPIF). If both the SPI interrupt enable bit (SPIE) and the serial port interrupt enable bit (ES) are set, an interrupt is requested.

The Slave Select input, $\overline{SS}/P1.4$, is set low to select an individual SPI device as a slave. When $\overline{SS}/P1.4$ is set high, the SPI port is deactivated and the MOSI/P1.5 pin can be used as an input.

There are four combinations of SCK phase and polarity with respect to serial data, which are determined by control bits CPHA and CPOL. The SPI data transfer formats are shown in Figure 8 and Figure 9.



Figure 9. SPI Transfer Format with CPHA = 1



defined but normally LSB of previously transmitted character

Interrupts

The AT89S8252 has a total of six interrupt vectors: two external interrupts ($\overline{INT0}$ and $\overline{INT1}$), three timer interrupts (Timers 0, 1, and 2), and the serial port interrupt. These interrupts are all shown in Figure 10.

Each of these interrupt sources can be individually enabled or disabled by setting or clearing a bit in Special Function Register IE. IE also contains a global disable bit, EA, which disables all interrupts at once.

As Table 10 shows that bit position IE.6 is unimplemented. In the AT89C51, bit position IE.5 is also unimplemented. User software should not write 1s to these bit positions, since they may be used in future AT89 products.

Timer 2 interrupt is generated by the logical OR of bits TF2 and EXF2 in register T2CON. Neither of these flags is cleared by hardware when the service routine is vectored to the interrupt. In fact, the service routine may have to determine whether it was TF2 or EXF2 that generated the interrupt, and that bit will have to be cleared in software.

Timer 0 and Timer 1 flags, TF0 and TF1, are set at the beginning of the cycle in which the timers overflow. The values are then polled by the circuitry in the next cycle. However, the Timer 2 flag, TF2, is set at S2P2 and is polled in the cycle in which the timer overflows.

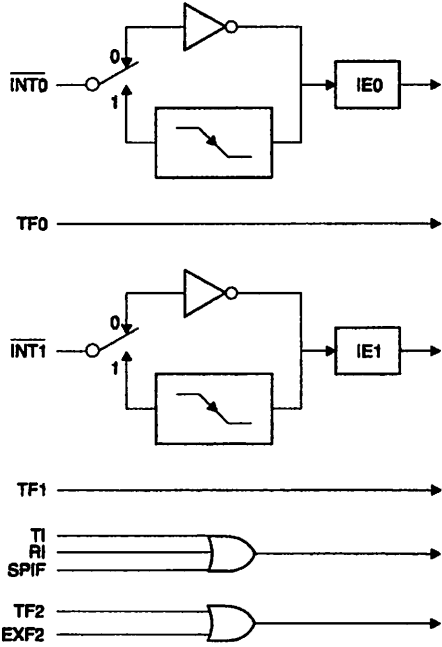
Table 10. Interrupt Enable (IE) Register

(MSB)(LSB)							
EA	—	ET2	ES	ET1	EX1	ET0	EX0
Enable Bit = 1 enables the interrupt.							
Enable Bit = 0 disables the interrupt.							

Symbol	Position	Function
EA	IE.7	Disables all interrupts. If EA = 0, no interrupt is acknowledged. If EA = 1, each interrupt source is individually enabled or disabled by setting or clearing its enable bit.
—	IE.6	Reserved.
ET2	IE.5	Timer 2 interrupt enable bit.
ES	IE.4	SPI and UART interrupt enable bit.
ET1	IE.3	Timer 1 interrupt enable bit.
EX1	IE.2	External interrupt 1 enable bit.
ET0	IE.1	Timer 0 interrupt enable bit.
EX0	IE.0	External interrupt 0 enable bit.

User software should never write 1s to unimplemented bits, because they may be used in future AT89 products.

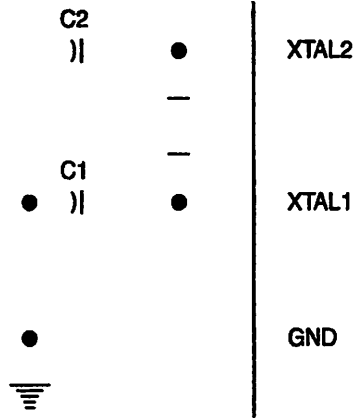
Figure 10. Interrupt Sources



Oscillator Characteristics

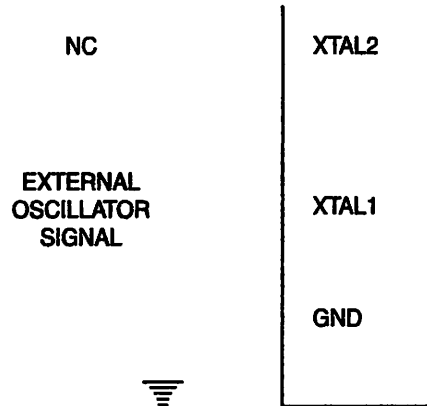
XTAL1 and XTAL2 are the input and output, respectively, of an internal inverting amplifier that can be configured for use as an on-chip oscillator, as shown in Figure 11. Either a quartz crystal or ceramic resonator may be used. To drive the oscillator from an external clock source, XTAL2 should be left unconnected while XTAL1 is driven, as shown in Figure 12. There are no requirements on the duty cycle of the external clock signal, since the input to the internal clocking circuitry goes through a divide-by-two flip-flop, but minimum and maximum voltage high and low time specifications must be observed.

Figure 11. Oscillator Connections



Note: Note: C1, C2 = 30 pF ± 10 pF for Crystals
= 40 pF ± 10 pF for Ceramic Resonators

Figure 12. External Clock Drive Configuration





Mode

In idle mode, the CPU puts itself to sleep while all the on-chip peripherals remain active. The mode is invoked by the instruction that invokes idle mode. The content of the on-chip RAM and all the special function registers remain unchanged during this mode. The idle mode can be terminated by any enabled external interrupt or by a hardware reset.

When idle mode is terminated by a hardware reset, the device normally resumes program execution from where it left off, up to two machine cycles before the internal reset algorithm takes control. On-chip hardware inhibits access to internal RAM in this event, but access to the port pins is not inhibited. To eliminate the possibility of an unexpected write to a port pin when idle mode is terminated by a reset, the instruction following the one that invokes idle mode should not write to a port pin or to external memory.

from where it left off, up to two machine cycles before the internal reset algorithm takes control. On-chip hardware inhibits access to internal RAM in this event, but access to the port pins is not inhibited. To eliminate the possibility of an unexpected write to a port pin when idle mode is terminated by a reset, the instruction following the one that invokes idle mode should not write to a port pin or to external memory.

Status of External Pins During Idle and Power-down Modes

Mode	Program Memory	ALE	PSEN	PORT0	PORT1	PORT2	PORT3
Idle	Internal	1	1	Data	Data	Data	Data
Idle	External	1	1	Float	Data	Address	Data
Power-down	Internal	0	0	Data	Data	Data	Data
Power-down	External	0	0	Float	Data	Data	Data

Power-down Mode

In power-down mode, the oscillator is stopped and the instruction that invokes power-down is the last instruction executed. The on-chip RAM and Special Function Registers retain their values until the power-down mode is terminated. Exit from power-down can be initiated either by a hardware reset or by an enabled external interrupt. Reset initializes the SFRs but does not change the on-chip RAM. Reset should not be activated before V_{CC} is restored to normal operating level and must be held active long enough to allow the oscillator to restart and stabilize.

When power-down is terminated via an interrupt, the external interrupt can be enabled as level sensitive before entering power-down. The interrupt service routine starts at 16 ms (nominal) after the enabled interrupt pin is activated.

Program Memory Lock Bits

The AT89S8252 has three lock bits that can be left unprogrammed (U) or can be programmed (P) to obtain the additional features listed in the following table.

When lock bit 1 is programmed, the logic level at the \overline{EA} pin is sampled and latched during reset. If the device is powered up without a reset, the latch initializes to a random value and holds that value until reset is activated. The latched value of \overline{EA} must agree with the current logic level at that pin in order for the device to function properly.

Once programmed, the lock bits can only be unprogrammed with the Chip Erase operations in either the parallel or serial modes.

Program Memory Lock Bit Protection Modes⁽¹⁾⁽²⁾

Program Lock Bits			Protection Type
LB1	LB2	LB3	
U	U	U	No internal memory lock feature.
P	U	U	MOVX instructions executed from external program memory are disabled from fetching code bytes from internal memory. \overline{EA} is sampled and latched on reset and further programming of the Flash memory (parallel or serial mode) is disabled.
P	P	U	Same as Mode 2, but parallel or serial verify are also disabled.
P	P	P	Same as Mode 3, but external execution is also disabled.

1. U = Unprogrammed

2. P = Programmed

AT89S8252

Programming the Flash and EEPROM

The AT89S8252 Flash Microcontroller offers 8K bytes of system reprogrammable Flash Code memory and 2K bytes of EEPROM Data memory.

The AT89S8252 is normally shipped with the on-chip Flash Code memory and EEPROM Data memory arrays in the erased state (i.e. contents = FFH) and ready to be programmed. The device supports a High-voltage (12V) Parallel programming mode and a Low-voltage (5V) Serial programming mode. The serial programming mode provides a convenient way to download the AT89S8252 inside the user's system. The parallel programming mode is compatible with conventional third party Flash or EPROM programmers.

Code and Data memory arrays are mapped via separate address spaces in the serial programming mode. In parallel programming mode, the two arrays occupy one contiguous address space: 0000H to 1FFFH for the Code array and 2000H to 27FFH for the Data array.

Code and Data memory arrays on the AT89S8252 are programmed byte-by-byte in either programming mode. An erase cycle is provided with the self-timed programming operation in the serial programming mode. There is no need to perform the Chip Erase operation to reprogram memory locations in the serial programming mode as long as any of the lock bits have not been programmed.

In parallel programming mode, there is no auto-erase cycle. To reprogram any non-blank byte, the user needs to perform the Chip Erase operation first to erase both arrays.

Parallel Programming Algorithm: To program and verify the AT89S8252 in the parallel programming mode, the following sequence is recommended:

1. Power-up sequence:

1.1. Apply power between V_{CC} and GND pins.

1.2. Set RST pin to "H".

1.3. Apply a 3 MHz to 24 MHz clock to XTAL1 pin and wait for at least 10 milliseconds.

1.4. Set \overline{PSEN} pin to "L".

1.5. Set LE pin to "H".

1.6. Set \overline{EA} pin to "H" and all other pins to "H".

1.7. Apply the appropriate combination of "H" or "L" logic levels to pins P2.6, P2.7, P3.6, P3.7 to select one of the programming operations shown in the Flash Programming Modes table.

1.8. Apply the desired byte address to pins P1.0 to P1.7 and P2.0 to P2.5.

1.9. Apply data to pins P0.0 to P0.7 for Write Code operation.

5. Raise \overline{EA}/V_{pp} to 12V to enable Flash programming, erase or verification.
6. Pulse ALE/ \overline{PROG} once to program a byte in the Code memory array, the Data memory array or the lock bits. The byte-write cycle is self-timed and typically takes 1.5 ms.
7. To verify the byte just programmed, bring pin P2.7 to "L" and read the programmed data at pins P0.0 to P0.7.
8. Repeat steps 3 through 7 changing the address and data for the entire 2K or 8K bytes array or until the end of the object file is reached.
9. Power-off sequence:
 - 9.1. Set XTAL1 to "L".
 - 9.2. Set RST and \overline{EA} pins to "L".
 - 9.3. Turn V_{CC} power off.

In the parallel programming mode, there is no auto-erase cycle and to reprogram any non-blank byte, the user needs to use the Chip Erase operation first to erase both arrays.

Data Polling: The AT89S8252 features \overline{DATA} Polling to indicate the end of a write cycle. During a write cycle in the parallel or serial programming mode, an attempted read of the last byte written will result in the complement of the written datum on P0.7 (parallel mode), and on the MSB of the serial output byte on MISO (serial mode). Once the write cycle has been completed, true data are valid on all outputs, and the next cycle may begin. \overline{DATA} Polling may begin any time after a write cycle has been initiated.

Ready/Busy: The progress of byte programming in the parallel programming mode can also be monitored by the RDY/BSY output signal. Pin P3.4 is pulled Low after ALE goes High during programming to indicate BUSY. P3.4 is pulled High again when programming is done to indicate READY.

Program Verify: If lock bits LB1 and LB2 have not been programmed, the programmed Code or Data byte can be read back via the address and data lines for verification. The state of the lock bits can also be verified directly in the parallel programming mode. In the serial programming mode, the state of the lock bits can only be verified indirectly by observing that the lock bit features are enabled.

Chip Erase: Both Flash and EEPROM arrays are erased electrically at the same time. In the parallel programming mode, chip erase is initiated by using the proper combination of control signals and by holding ALE/ \overline{PROG} low for 10 ms. The Code and Data arrays are written with all "1"s in the Chip Erase operation.



Serial programming mode, a chip erase operation is performed by issuing the Chip Erase instruction. In this mode, the erase is self-timed and takes about 16 ms.

During chip erase, a serial read from any address location returns 00H at the data outputs.

Parallel Programming Fuse: A programmable fuse is available to disable Serial Programming if the user needs maximum system security. The Serial Programming Fuse can only be programmed or erased in the Parallel Programming Mode.

AT89S8252 is shipped with the Serial Programming Fuse enabled.

Verifying the Signature Bytes: The signature bytes are verified by the same procedure as a normal verification of memory locations 030H and 031H, except that P3.6 and P3.7 must be pulled to a logic low. The values returned are as follows:

030H) = 1EH indicates manufactured by Atmel
031H) = 72H indicates 89S8252

Serial Programming Interface

Each code byte in the Flash and EEPROM arrays can be programmed, and the entire array can be erased, by using the appropriate combination of control signals. The write operation cycle is self-timed and once initiated, will automatically time itself to completion.

Major programming vendors offer worldwide support for the Atmel microcontroller series. Please contact your local programming vendor for the appropriate software revision.

Serial Downloading

The Code and Data memory arrays can be programmed using the serial SPI bus while RST is pulled to low. The serial interface consists of pins SCK, MOSI (input) and MISO (output). After RST is set high, the Programming Enable instruction needs to be executed first before program/erase operations can be executed.

A chip-erase cycle is built into the self-timed programming operation (in the serial mode ONLY) and there is no need to execute the Chip Erase instruction unless any of the memory bits have been programmed. The Chip Erase operation returns the content of every memory location in both the Code and Data arrays into FFH.

The Code and Data memory arrays have separate address ranges:

0000H to 1FFFFH for Code memory and 0000H to 7FFFH for Data memory.

Either an external system clock is supplied at pin XTAL1 or a crystal needs to be connected across pins XTAL1 and XTAL2. The maximum serial clock (SCK) frequency should be less than 1/40 of the crystal frequency. With a 24 MHz oscillator clock, the maximum SCK frequency is 600 kHz.

Serial Programming Algorithm

To program and verify the AT89S8252 in the serial programming mode, the following sequence is recommended:

1. Power-up sequence:

Apply power between VCC and GND pins.
Set RST pin to "H".

If a crystal is not connected across pins XTAL1 and XTAL2, apply a 3 MHz to 24 MHz clock to XTAL1 pin and wait for at least 10 milliseconds.

2. Enable serial programming by sending the Programming Enable serial instruction to pin MOSI/P1.5. The frequency of the shift clock supplied at pin SCK/P1.7 needs to be less than the CPU clock at XTAL1 divided by 40.
3. The Code or Data array is programmed one byte at a time by supplying the address and data together with the appropriate Write instruction. The selected memory location is first automatically erased before new data is written. The write cycle is self-timed and typically takes less than 2.5 ms at 5V.
4. Any memory location can be verified by using the Read instruction which returns the content at the selected address at serial output MISO/P1.6.
5. At the end of a programming session, RST can be set low to commence normal operation.

Power-off sequence (if needed):

Set XTAL1 to "L" (if a crystal is not used).
Set RST to "L".
Turn V_{CC} power off.

Serial Programming Instruction

The Instruction Set for Serial Programming follows a 3-byte protocol and is shown in the following table:

Instruction Set

Instruction	Input Format			Operation
	Byte 1	Byte 2	Byte 3	
Programming Enable	1010 1100	0101 0011	xxxx xxxx	Enable serial programming interface after RST goes high.
Chip Erase	1010 1100	xxxx x100	xxxx xxxx	Chip erase both 8K & 2K memory arrays.
Read Code Memory	aaaa a001	low addr	xxxx xxxx	Read data from Code memory array at the selected address. The 5 MSBs of the first byte are the high order address bits. The low order address bits are in the second byte. Data are available at pin MISO during the third byte.
Write Code Memory	aaaa a010	low addr	data in	Write data to Code memory location at selected address. The address bits are the 5 MSBs of the first byte together with the second byte.
Read Data Memory	00aa a101	low addr	xxxx xxxx	Read data from Data memory array at selected address. Data are available at pin MISO during the third byte.
Write Data Memory	00aa a110	low addr	data in	Write data to Data memory location at selected address.
Write Lock Bits	1010 1100	x x111	xxxx xxxx	Write lock bits. Set LB1, LB2 or LB3 = "0" to program lock bits.

1. DATA polling is used to indicate the end of a write cycle which typically takes less than 2.5 ms at 5V.

2. "aaaaa" = high order address.

3. "x" = don't care.



Flash and EEPROM Parallel Programming Modes

Mode	RST	PSEN	ALE/PROG	EA/V _{PP}	P2.6	P2.7	P3.6	P3.7	Data I/O P0.7:0	Address P2.5:0 P1.7:0
Parallel Prog. Modes	H	h ⁽¹⁾	h ⁽¹⁾	x						
Chip Erase	H	L		12V	H	L	L	L	X	X
16K (10K bytes) Memory	H	L		12V	L	H	H	H	DIN	ADDR
16K (10K bytes) Memory	H	L	H	12V	L	L	H	H	DOUT	ADDR
EEPROM Lock Bits:	H	L		12V	H	L	H	L	DIN	X
Bit - 1									P0.7 = 0	X
Bit - 2									P0.6 = 0	X
Bit - 3									P0.5 = 0	X
EEPROM Lock Bits:	H	L	H	12V	H	H	L	L	DOUT	X
Bit - 1									@P0.2	X
Bit - 2									@P0.1	X
Bit - 3									@P0.0	X
Parallel Atmel Code	H	L	H	12V	L	L	L	L	DOUT	30H
Parallel Device Code	H	L	H	12V	L	L	L	L	DOUT	31H
Parallel Prog. Enable	H	L		12V	L	H	L	H	P0.0 = 0	X
Parallel Prog. Disable	H	L		12V	L	H	L	H	P0.0 = 1	X
Parallel Serial Prog. Fuse	H	L	H	12V	H	H	L	H	@P0.0	X

Notes:
 1. "h" = weakly pulled "High" internally.
 2. Chip Erase and Serial Programming Fuse require a 10 ms $\overline{\text{PROG}}$ pulse. Chip Erase needs to be performed first before reprogramming any byte with a content other than FFH.

3. P3.4 is pulled Low during programming to indicate RDY/BSY.
 4. "X" = don't care

Figure 13. Programming the Flash/EEPROM Memory

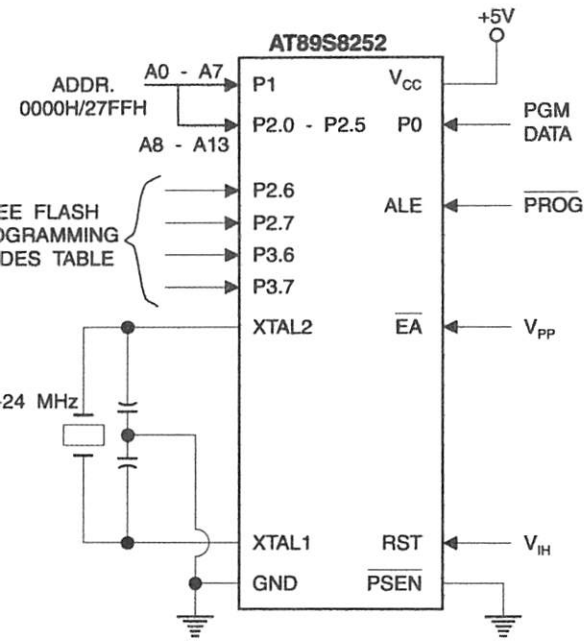


Figure 15. Flash/EEPROM Serial Downloading

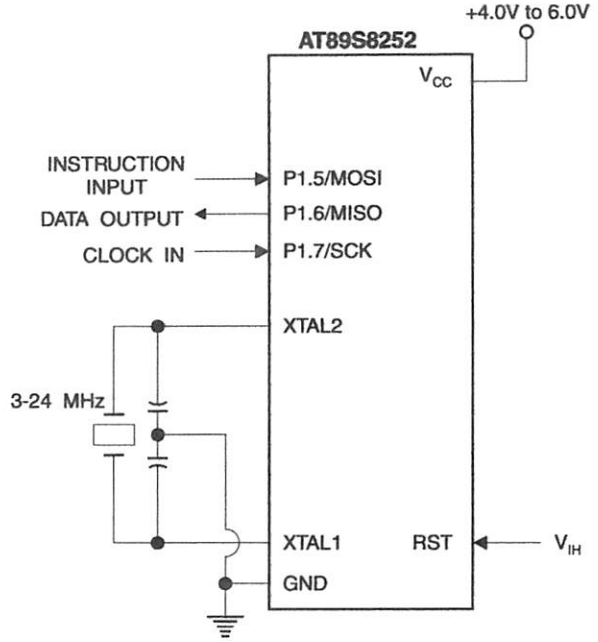
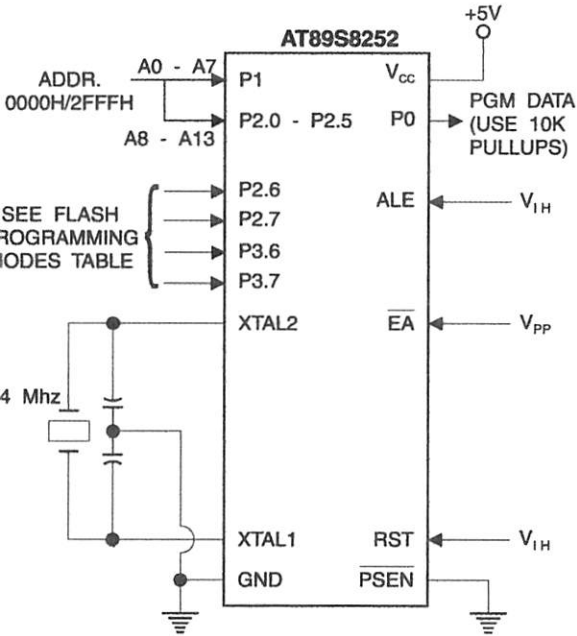


Figure 14. Verifying the Flash/EEPROM Memory



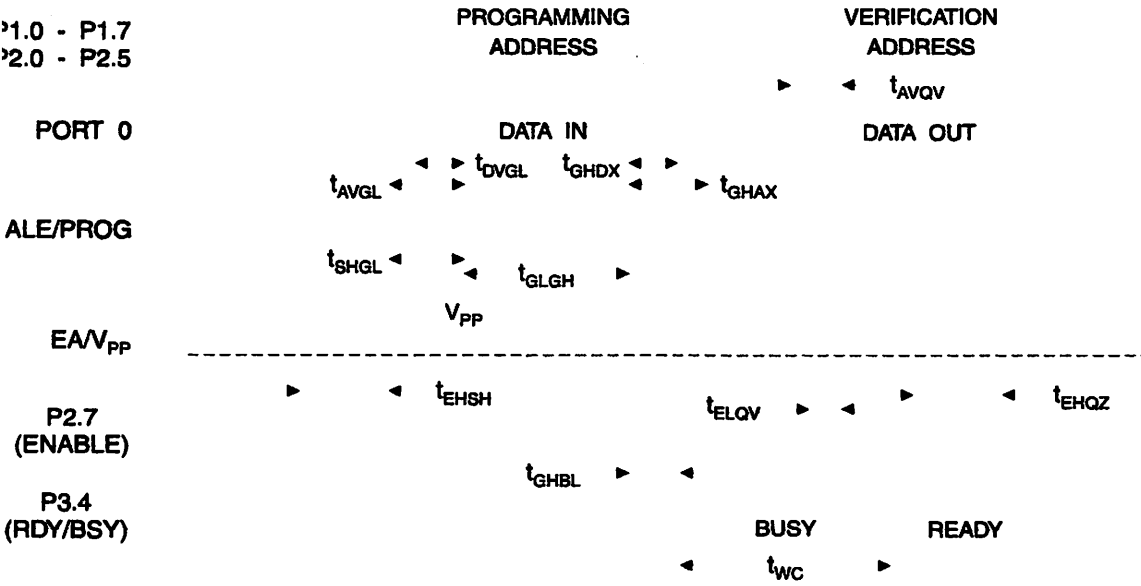


Flash Programming and Verification Characteristics – Parallel Mode

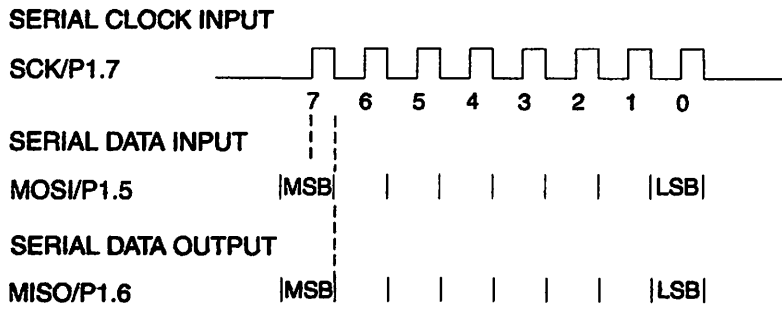
0°C to 70°C, $V_{CC} = 5.0V \pm 10\%$

Symbol	Parameter	Min	Max	Units
	Programming Enable Voltage	11.5	12.5	V
	Programming Enable Current		1.0	mA
f _{CL}	Oscillator Frequency	3	24	MHz
t _{CL}	Address Setup to $\overline{\text{PROG}}$ Low	$48t_{\text{CLCL}}$		
t _{CLX}	Address Hold after $\overline{\text{PROG}}$	$48t_{\text{CLCL}}$		
t _{DL}	Data Setup to $\overline{\text{PROG}}$ Low	$48t_{\text{CLCL}}$		
t _{DLX}	Data Hold after $\overline{\text{PROG}}$	$48t_{\text{CLCL}}$		
t _{PH}	P2.7 ($\overline{\text{ENABLE}}$) High to V_{PP}	$48t_{\text{CLCL}}$		
t _{PL}	V_{PP} Setup to $\overline{\text{PROG}}$ Low	10		μs
t _{PH}	$\overline{\text{PROG}}$ Width	1	110	μs
t _{AV}	Address to Data Valid		$48t_{\text{CLCL}}$	
t _{EV}	$\overline{\text{ENABLE}}$ Low to Data Valid		$48t_{\text{CLCL}}$	
t _{DZ}	Data Float after $\overline{\text{ENABLE}}$	0	$48t_{\text{CLCL}}$	
t _{PL}	$\overline{\text{PROG}}$ High to $\overline{\text{BUSY}}$ Low		1.0	μs
	Byte Write Cycle Time		2.0	ms

Flash/EEPROM Programming and Verification Waveforms – Parallel Mode



Serial Downloading Waveforms





Absolute Maximum Ratings*

Operating Temperature.....	-55°C to +125°C
Storage Temperature.....	-65°C to +150°C
Voltage on Any Pin with Respect to Ground.....	-1.0V to +7.0V
Maximum Operating Voltage.....	6.6V
Output Current.....	15.0 mA

***NOTICE:** Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Characteristics

Values shown in this table are valid for $T_A = -40^\circ\text{C}$ to 85°C and $V_{CC} = 5.0\text{V} \pm 20\%$, unless otherwise noted.

Symbol	Parameter	Condition	Min	Max	Units
	Input Low-voltage	(Except \overline{EA})	-0.5	$0.2 V_{CC} - 0.1$	V
	Input Low-voltage (\overline{EA})		-0.5	$0.2 V_{CC} - 0.3$	V
	Input High-voltage	(Except XTAL1, RST)	$0.2 V_{CC} + 0.9$	$V_{CC} + 0.5$	V
	Input High-voltage	(XTAL1, RST)	$0.7 V_{CC}$	$V_{CC} + 0.5$	V
	Output Low-voltage ⁽¹⁾ (Ports 1,2,3)	$I_{OL} = 1.6 \text{ mA}$		0.5	V
	Output Low-voltage ⁽¹⁾ (Port 0, ALE, PSEN)	$I_{OL} = 3.2 \text{ mA}$		0.5	V
	Output High-voltage (Ports 1,2,3, ALE, PSEN)	$I_{OH} = -60 \mu\text{A}, V_{CC} = 5\text{V} \pm 10\%$	2.4		V
		$I_{OH} = -25 \mu\text{A}$	$0.75 V_{CC}$		V
		$I_{OH} = -10 \mu\text{A}$	$0.9 V_{CC}$		V
	Output High-voltage (Port 0 in External Bus Mode)	$I_{OH} = -800 \mu\text{A}, V_{CC} = 5\text{V} \pm 10\%$	2.4		V
		$I_{OH} = -300 \mu\text{A}$	$0.75 V_{CC}$		V
		$I_{OH} = -80 \mu\text{A}$	$0.9 V_{CC}$		V
	Logical 0 Input Current (Ports 1,2,3)	$V_{IN} = 0.45\text{V}$		-50	μA
	Logical 1 to 0 Transition Current (Ports 1,2,3)	$V_{IN} = 2\text{V}, V_{CC} = 5\text{V} \pm 10\%$		-650	μA
	Input Leakage Current (Port 0, EA)	$0.45 < V_{IN} < V_{CC}$		± 10	μA
RST	Reset Pull-down Resistor		50	300	K Ω
	Pin Capacitance	Test Freq. = 1 MHz, $T_A = 25^\circ\text{C}$		10	pF
	Power Supply Current	Active Mode, 12 MHz		25	mA
		Idle Mode, 12 MHz		6.5	mA
	Power-down Mode ⁽²⁾	$V_{CC} = 6\text{V}$		100	μA
		$V_{CC} = 3\text{V}$		40	μA

1. Under steady state (non-transient) conditions, I_{OL} must be externally limited as follows:
 Maximum I_{OL} per port pin: 10 mA
 Maximum I_{OL} per 8-bit port:
 Port 0: 26 mA
 Ports 1, 2, 3: 15 mA

Maximum total I_{OL} for all output pins: 71 mA
 If I_{OL} exceeds the test condition, V_{OL} may exceed the related specification. Pins are not guaranteed to sink current greater than the listed test conditions.
 2. Minimum V_{CC} for Power-down is 2V

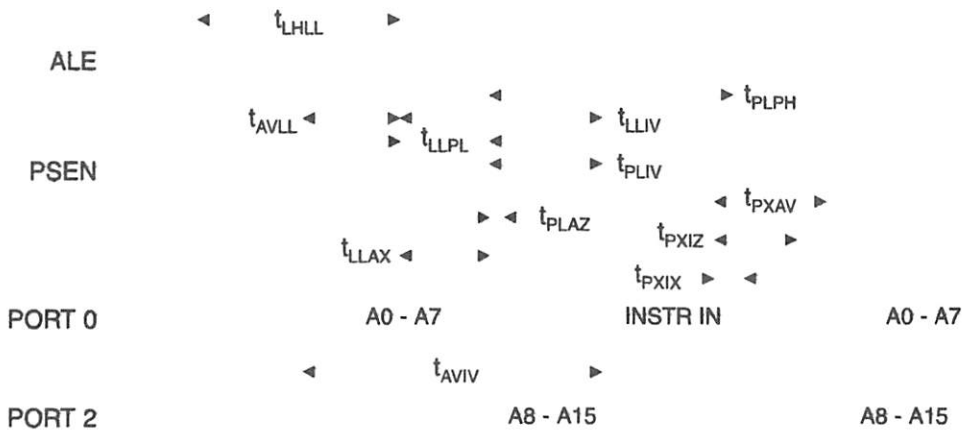
Characteristics

Under operating conditions, load capacitance for Port 0, ALE/ $\overline{\text{PROG}}$, and $\overline{\text{PSEN}}$ = 100 pF; load capacitance for all other ports = 80 pF.

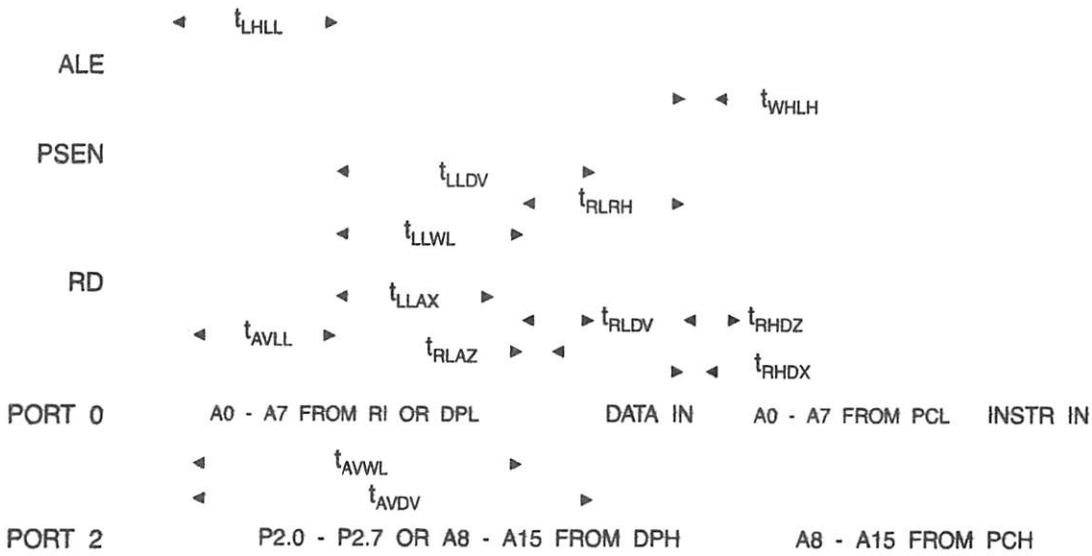
Internal Program and Data Memory Characteristics

Symbol	Parameter	Variable Oscillator		Units
		Min	Max	
f_{osc}	Oscillator Frequency	0	24	MHz
	ALE Pulse Width	$2t_{\text{CLCL}} - 40$		ns
	Address Valid to ALE Low	$t_{\text{CLCL}} - 13$		ns
	Address Hold after ALE Low	$t_{\text{CLCL}} - 20$		ns
	ALE Low to Valid Instruction In		$4t_{\text{CLCL}} - 65$	ns
	ALE Low to $\overline{\text{PSEN}}$ Low	$t_{\text{CLCL}} - 13$		ns
	$\overline{\text{PSEN}}$ Pulse Width	$3t_{\text{CLCL}} - 20$		ns
	$\overline{\text{PSEN}}$ Low to Valid Instruction In		$3t_{\text{CLCL}} - 45$	ns
	Input Instruction Hold after $\overline{\text{PSEN}}$	0		ns
	Input Instruction Float after $\overline{\text{PSEN}}$		$t_{\text{CLCL}} - 10$	ns
	$\overline{\text{PSEN}}$ to Address Valid	$t_{\text{CLCL}} - 8$		ns
	Address to Valid Instruction In		$5t_{\text{CLCL}} - 55$	ns
	$\overline{\text{PSEN}}$ Low to Address Float		10	ns
	$\overline{\text{RD}}$ Pulse Width	$6t_{\text{CLCL}} - 100$		ns
	$\overline{\text{WR}}$ Pulse Width	$6t_{\text{CLCL}} - 100$		ns
	$\overline{\text{RD}}$ Low to Valid Data In		$5t_{\text{CLCL}} - 90$	ns
	Data Hold after $\overline{\text{RD}}$	0		ns
	Data Float after $\overline{\text{RD}}$		$2t_{\text{CLCL}} - 28$	ns
	ALE Low to Valid Data In		$8t_{\text{CLCL}} - 150$	ns
	Address to Valid Data In		$9t_{\text{CLCL}} - 165$	ns
	ALE Low to $\overline{\text{RD}}$ or $\overline{\text{WR}}$ Low	$3t_{\text{CLCL}} - 50$	$3t_{\text{CLCL}} + 50$	ns
	Address to $\overline{\text{RD}}$ or $\overline{\text{WR}}$ Low	$4t_{\text{CLCL}} - 75$		ns
	Data Valid to $\overline{\text{WR}}$ Transition	$t_{\text{CLCL}} - 20$		ns
	Data Valid to $\overline{\text{WR}}$ High	$7t_{\text{CLCL}} - 120$		ns
	Data Hold after $\overline{\text{WR}}$	$t_{\text{CLCL}} - 20$		ns
	$\overline{\text{RD}}$ Low to Address Float		0	ns
	$\overline{\text{RD}}$ or $\overline{\text{WR}}$ High to ALE High	$t_{\text{CLCL}} - 20$	$t_{\text{CLCL}} + 25$	ns

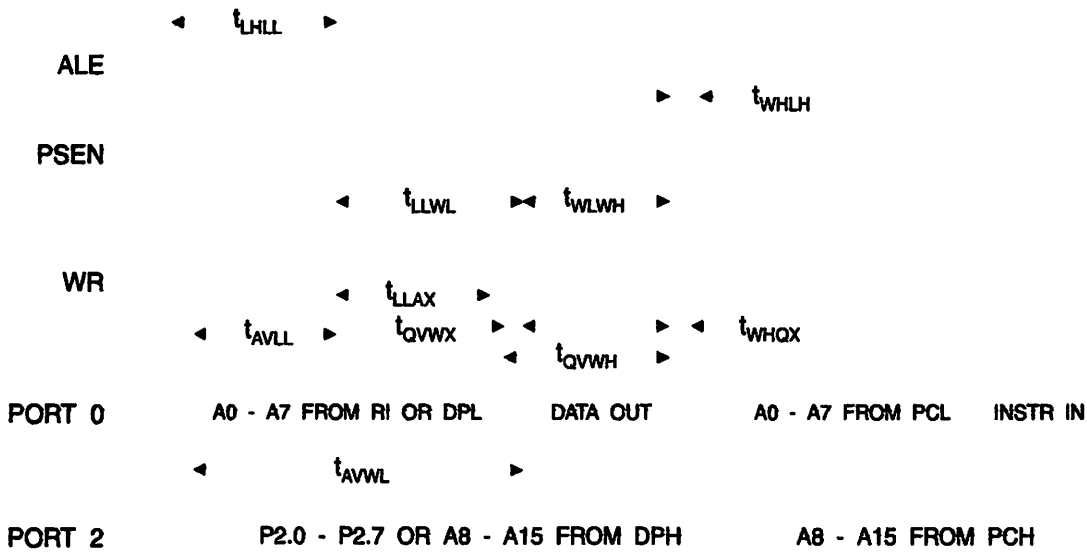
Internal Program Memory Read Cycle



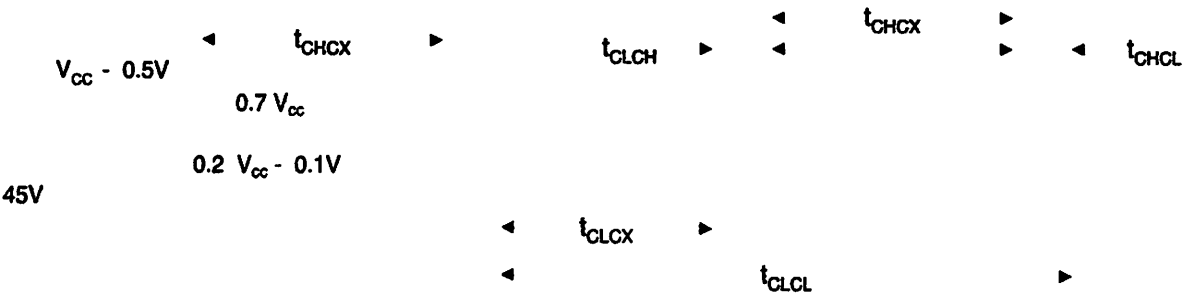
Internal Data Memory Read Cycle



External Data Memory Write Cycle



External Clock Drive Waveforms



External Clock Drive

Symbol	Parameter	$V_{CC} = 4.0V \text{ to } 6.0V$		Units
		Min	Max	
CL	Oscillator Frequency	0	24	MHz
	Clock Period	41.6		ns
	High Time	15		ns
	Low Time	15		ns
	Rise Time		20	ns
	Fall Time		20	ns



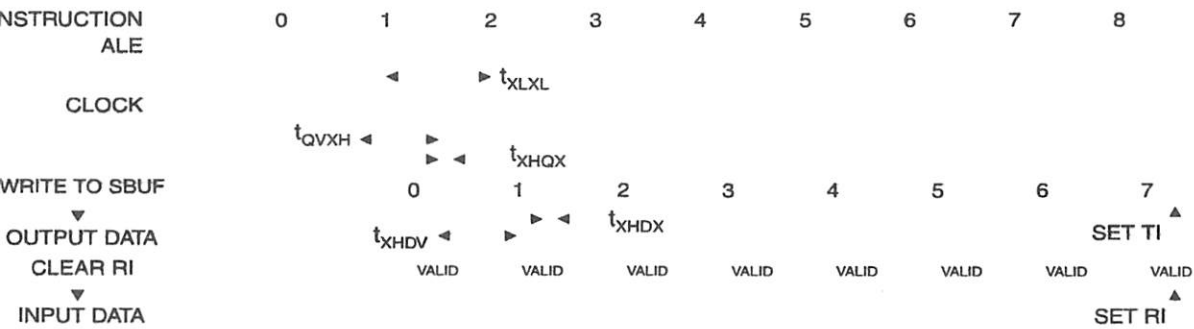


Serial Port Timing: Shift Register Mode Test Conditions

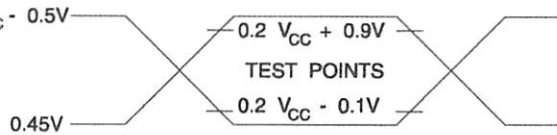
Values in this table are valid for $V_{CC} = 4.0V$ to $6V$ and Load Capacitance = 80 pF .

Symbol	Parameter	Variable Oscillator		Units
		Min	Max	
	Serial Port Clock Cycle Time	$12t_{CLCL}$		μs
	Output Data Setup to Clock Rising Edge	$10t_{CLCL} - 133$		ns
	Output Data Hold after Clock Rising Edge	$2t_{CLCL} - 117$		ns
	Input Data Hold after Clock Rising Edge	0		ns
	Clock Rising Edge to Input Data Valid		$10t_{CLCL} - 133$	ns

Shift Register Mode Timing Waveforms

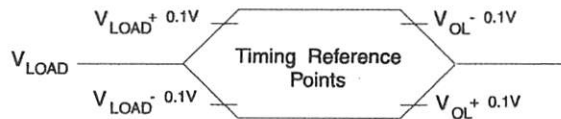


Testing Input/Output Waveforms⁽¹⁾

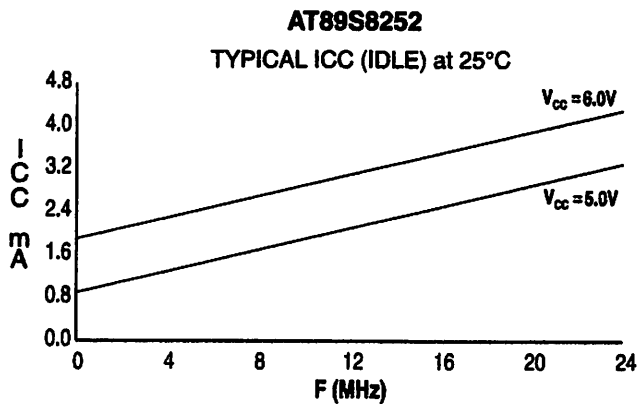
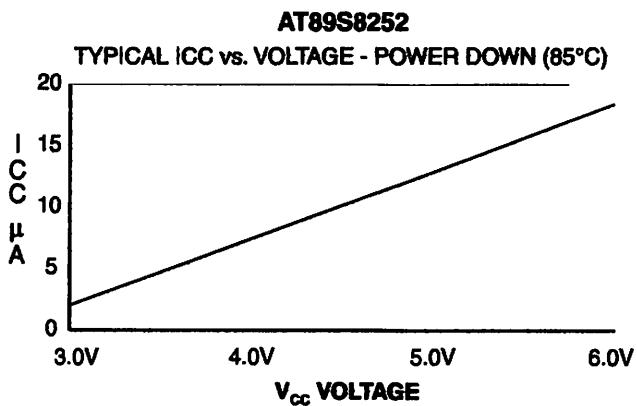
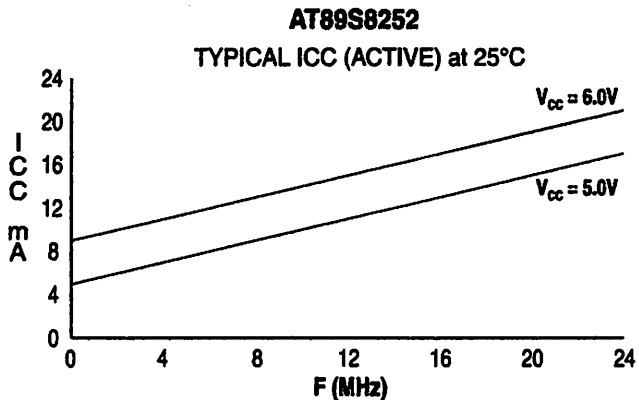


1. AC Inputs during testing are driven at $V_{CC} - 0.5V$ for a logic 1 and $0.45V$ for a logic 0. Timing measurements are made at V_{IH} min. for a logic 1 and V_{IL} max. for a logic 0.

Float Waveforms⁽¹⁾



- Notes: 1. For timing purposes, a port pin is no longer floating when a 100 mV change from load voltage occurs. A port pin begins to float when a 100 mV change from the loaded V_{OH}/V_{OL} level occurs.



- Notes: 1. XTAL1 tied to GND for I_{cc} (power-down)
2. Lock bits programmed





Ordering Information

Speed (MHz)	Power Supply	Ordering Code	Package	Operation Range
24	4.0V to 6.0V	AT89S8252-24AC	44A	Commercial (0°C to 70°C)
		AT89S8252-24JC	44J	
		AT89S8252-24PC	40P6	
		AT89S8252-24QC	44Q	
	4.0V to 6.0V	AT89S8252-24AI	44A	Industrial (-40°C to 85°C)
		AT89S8252-24JI	44J	
		AT89S8252-24PI	40P6	
		AT89S8252-24QI	44Q	
33	4.5V to 5.5V	AT89S8252-33AC	44A	Commercial (0°C to 70°C)
		AT89S8252-33JC	44J	
		AT89S8252-33PC	40P6	
		AT89S8252-33QC	44Q	

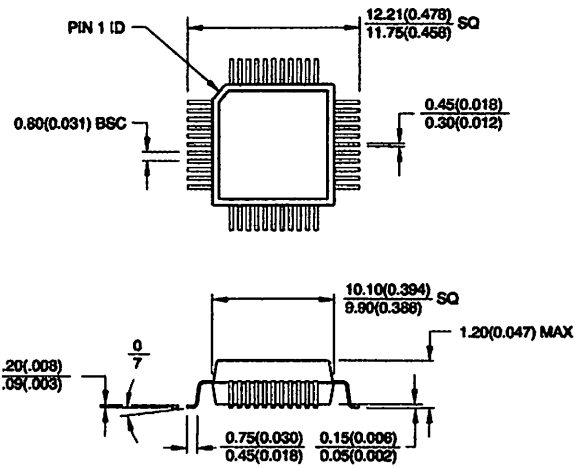
= Preliminary Information

Package Type
44-lead, Thin Plastic Gull Wing Quad Flatpack (TQFP)
44-lead, Plastic J-leaded Chip Carrier (PLCC)
40-lead, 0.600" Wide, Plastic Dual Inline Package (PDIP)
44-lead, Plastic Gull Wing Quad Flatpack (PQFP)

AT89S8252

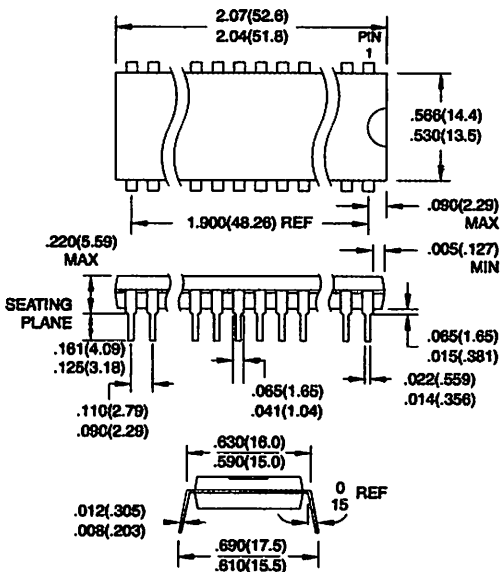
Packaging Information

44A, 44-lead, Thin (1.0 mm) Plastic Gull Wing Quad Flatpack (TQFP)
 Dimensions in Millimeters and (Inches)*
 JEDEC STANDARD MS-026 ACB

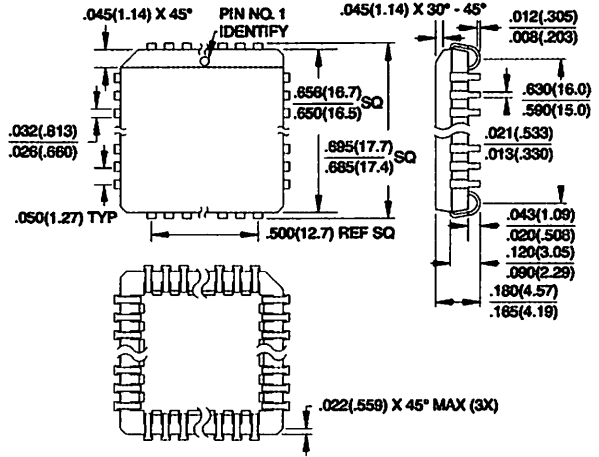


Controlling dimension: millimeters

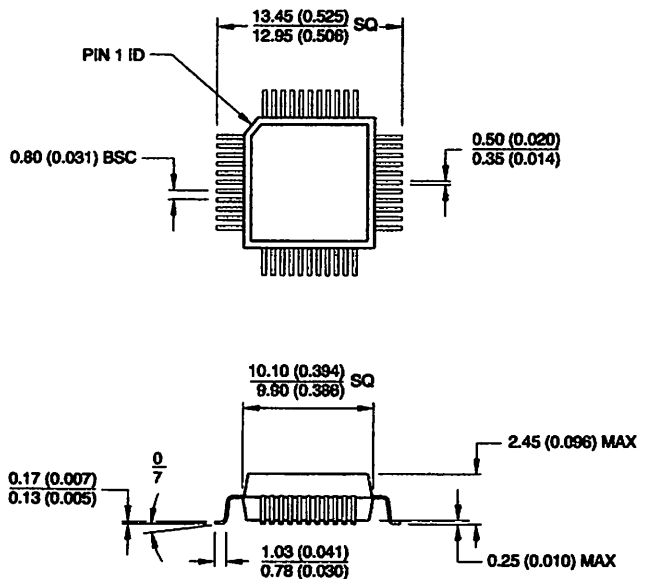
44P6, 40-lead, 0.600" Wide, Plastic Dual In-line Package (PDIP)
 Dimensions in Inches and (Millimeters)



44J, 44-lead, Plastic J-leaded Chip Carrier (PLCC)
 Dimensions in Inches and (Millimeters)
 JEDEC STANDARD MS-018 AC



44Q, 44-lead, Plastic Quad Flat Package (PQFP)
 Dimensions in Millimeters and (Inches)*
 JEDEC STANDARD MS-022 AB



Controlling dimension: millimeters





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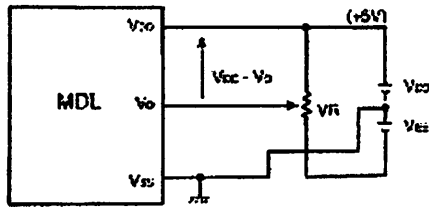
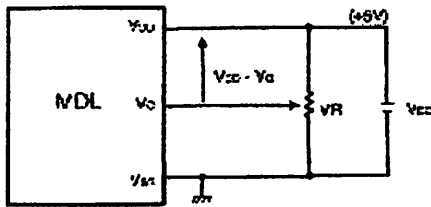
Printed on recycled paper.

0401E-02/00/xM

ITEM		VALUE	
		MIN	MAX
Power supply for controller	(V _{DD} - V _{SS})	0	7.0V
Power supply for LCD driver	(V _{DD} - V ₀)	0	13.5V
Input voltage for data and control signals	i@	V _{SS}	V _{DD}
Operating temperature	(-LV model)	-5°C	+50°C
Storage temperature	(-LV model)	-20°C	+60°C

POWER SUPPLY FOR SINGLE SUPPLY VOLTAGE TYPES

POWER SUPPLY FOR DUAL SUPPLY VOLTAGE TYPES



V_{DD} - V₀: LCD driving voltage
VR: 10kΩ - 20kΩ

V_{DD} - V₀: LCD driving voltage
VR: 10kΩ - 20kΩ

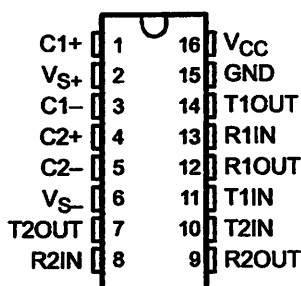
SYMBOL	I/O	FUNCTION
V _{SS}		Ground
V _{DD}		+5 Volt Power Supply
V ₀		Negative voltage supply for LCD driver (For non LV models)
RS	I	Register Select: H for data; L for instruction code
R/W	I	Read/Write: H-read from module; L-write into module
E		Enable (No connection for MDL-40466)
DB0 DB1 DB2 DB3	I/O	Data bus lines used only in 8 bit transfer
DB4 DB5 DB6	I/O	Data bus line used for both 4 and 8 bit transfer
DB7	I/O	Data bus lines used for both 4 and 8 bit transfer Also serves as Busy Flag for internal operations
E1	I	Enable for upper two rows
E2	I	Enable for lower two rows
A K	i@	+ve supply input for backlight -ve supply input for backlight

MAX232, MAX232I DUAL EIA-232 DRIVER/RECEIVER

SLLS047H – FEBRUARY 1989 – REVISED FEBRUARY 2002

- Operates With Single 5-V Power Supply
- LinBiCMOS™ Process Technology
- Two Drivers and Two Receivers
- ±30-V Input Levels
- Low Supply Current . . . 8 mA Typical
- Meets or Exceeds TIA/EIA-232-F and ITU Recommendation V.28
- Designed to be Interchangeable With Maxim MAX232
- ESD Protection Exceeds JESD 22 – 2000-V Human-Body Model (A114-A)
- Applications
 - TIA/EIA-232-F
 - Battery-Powered Systems
 - Terminals
 - Modems
 - Computers
- Package Options Include Plastic Small-Outline (D, DW, NS) Packages and Standard Plastic (N) DIPs

D, DW, N, OR NS PACKAGE
(TOP VIEW)



description

The MAX232 device is a dual driver/receiver that includes a capacitive voltage generator to supply EIA-232 voltage levels from a single 5-V supply. Each receiver converts EIA-232 inputs to 5-V TTL/CMOS levels. These receivers have a typical threshold of 1.3 V and a typical hysteresis of 0.5 V, and can accept ±30-V inputs. Each driver converts TTL/CMOS input levels into EIA-232 levels. The driver, receiver, and voltage-generator functions are available as cells in the Texas Instruments LinASIC™ library.

The MAX232 is characterized for operation from 0°C to 70°C. The MAX232I is characterized for operation from -40°C to 85°C.

AVAILABLE OPTIONS

T _A	PACKAGED DEVICES		
	SMALL OUTLINE (D, NS)	SMALL OUTLINE (DW)	PLASTIC DIP (N)
0°C to 70°C	MAX232D MAX232NS	MAX232DW	MAX232N
-40°C to 85°C	MAX232ID	MAX232IDW	MAX232IN

The D and DW packages are available taped and reeled by adding an R to the part number (i.e., MAX232DR). The NS package is only available taped and reeled.



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

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June 1997-3

FEATURES

- Wide Frequency Range, 0.01Hz to 300kHz
- Wide Supply Voltage Range, 4.5V to 20V
- HC MOS/TTL/Logic Compatibility
- FSK Demodulation, with Carrier Detection
- Wide Dynamic Range, 10mV to 3V rms
- Adjustable Tracking Range, $\pm 1\%$ to 80%
- Excellent Temp. Stability, ± 50 ppm/°C, max.

APPLICATIONS

- Caller Identification Delivery
- FSK Demodulation
- Data Synchronization
- Tone Decoding
- FM Detection
- Carrier Detection

GENERAL DESCRIPTION

The XR-2211 is a monolithic phase-locked loop (PLL) system especially designed for data communications applications. It is particularly suited for FSK modem applications. It operates over a wide supply voltage range of 4.5 to 20V and a wide frequency range of 0.01Hz to 300kHz. It can accommodate analog signals between 10mV and 3V, and can interface with conventional DTL, TTL, and ECL logic families. The circuit consists of a basic PLL for tracking an input signal within the pass band, a

quadrature phase detector which provides carrier detection, and an FSK voltage comparator which provides FSK demodulation. External components are used to independently set center frequency, bandwidth, and output delay. An internal voltage reference proportional to the power supply is provided at an output pin.

The XR-2211 is available in 14 pin packages specified for military and industrial temperature ranges.

ORDERING INFORMATION

Part No.	Package	Operating Temperature Range
XR-2211M	14 Pin CDIP (0.300")	-55°C to +125°C
XR-2211N	14 Pin CDIP (0.300")	-40°C to +85°C
XR-2211P	14 Pin PDIP (0.300")	-40°C to +85°C
XR-2211ID	14 Lead SOIC (Jedec, 0.150")	-40°C to +85°C

BLOCK DIAGRAM

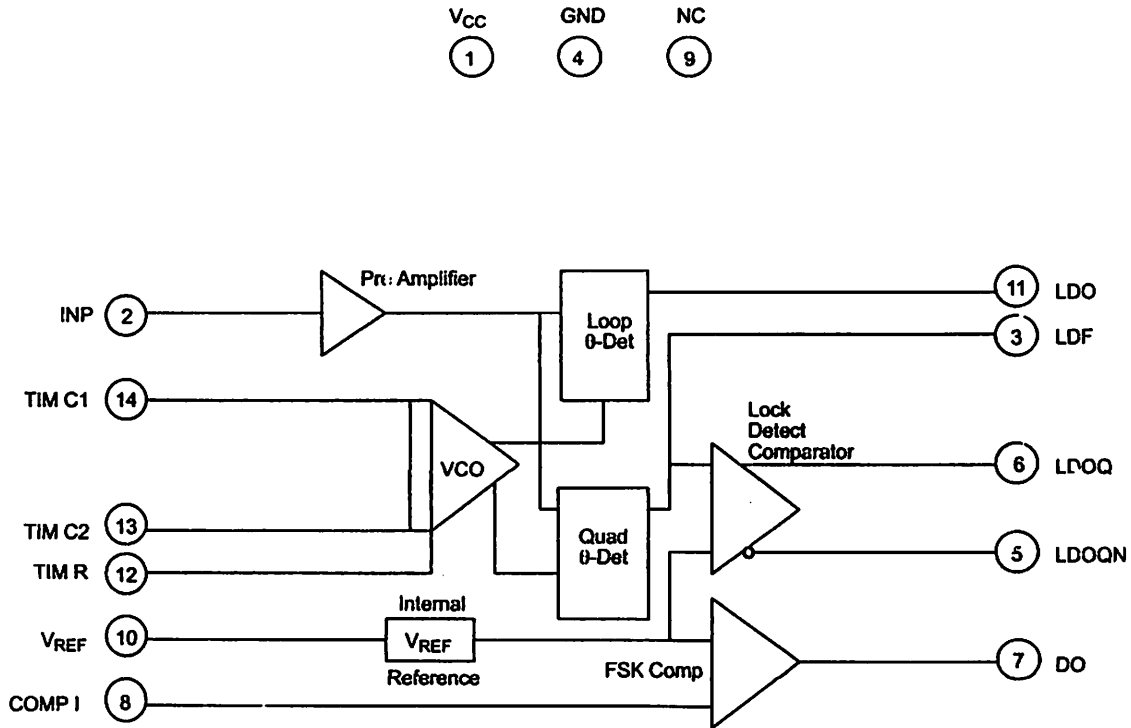
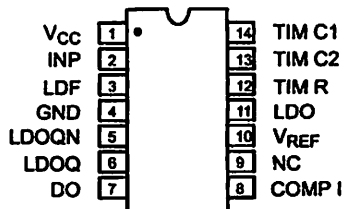
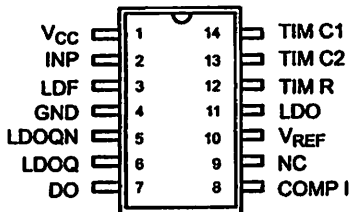


Figure 1. XR-2211 Block Diagram

CONFIGURATION



14 Lead CDIP, PDIP (0.300'')



14 Lead SOIC (Jedec, 0.150'')

DESCRIPTION

#	Symbol	Type	Description
	VCC		Positive Power Supply.
	INP	I	Receive Analog Input.
	LDF	O	Lock Detect Filter.
	GND		Ground Pin.
	LDOQN	O	Lock Detect Output Not. This output will be low if the VCO is in the capture range.
	LDOQ	O	Lock Detect Output. This output will be high if the VCO is in the capture range.
	DO	O	Data Output. Decoded FSK output.
	COMP I	I	FSK Comparator Input.
	NC		Not Connected.
	VREF	O	Internal Voltage Reference. The value of VREF is VCC/2 - 650mV.
	LDO	O	Loop Detect Output. This output provides the result of the quadrature phase detection.
	TIM R	I	Timing Resistor Input. This pin connects to the timing resistor of the VCO.
	TIM C2	I	Timing Capacitor Input. The timing capacitor connects between this pin and pin 14.
	TIM C1	I	Timing Capacitor Input. The timing capacitor connects between this pin and pin 13.

CRITICAL CHARACTERISTICS

Conditions: $V_{CC} = 12V$, $T_A = +25^\circ C$, $R_O = 30K\Omega$, $C_O = 0.033\mu F$, unless otherwise specified.

Parameter	Min.	Typ.	Max.	Unit	Conditions
General					
Supply Voltage	4.5		20	V	
Supply Current		4	7	mA	$R_O \geq 10K\Omega$. See <i>Figure 4</i> .
Oscillator Section					
Frequency Accuracy		± 1	± 3	%	Deviation from $f_O = 1/R_O C_O$
Frequency Stability					
Temperature		± 20	± 50	ppm/ $^\circ C$	See <i>Figure 8</i> .
Power Supply		0.05	0.5	%/V	$V_{CC} = 12 \pm 1V$. See <i>Figure 7</i> .
		0.2		%/V	$V_{CC} = \pm 5V$. See <i>Figure 7</i> .
Operating Frequency Limit	100	300		kHz	$R_O = 8.2K\Omega$, $C_O = 400pF$
Best Practical Operating Frequency			0.01	Hz	$R_O = 2M\Omega$, $C_O = 50\mu F$
Operating Resistor, R_O - See <i>Figure 5</i>					
Operating Range	5		2000	K Ω	
Recommended Range	5			K Ω	See <i>Figure 7</i> and <i>Figure 8</i> .
Phase Detector Section					
Output Current	± 150	± 200	± 300	μA	Measured at Pin 11
Output Offset Current		1		μA	
Output Impedance		1		M Ω	
Output Swing	± 4	± 5		V	Referenced to Pin 10
Temperature Phase Detector					
Measured at Pin 3					
Output Current	100	300		μA	
Output Impedance		1		M Ω	
Output Swing		11		V_{PP}	
Input Preempt Section					
Measured at Pin 2					
Input Impedance		20		K Ω	
Input Signal					
Voltage Required to Cause Limiting		2	10	mV rms	

Parameters are guaranteed over the recommended operating conditions, but are not 100% tested in production. All face parameters are covered by production test and guaranteed over operating temperature range.

ELECTRICAL CHARACTERISTICS (CONT'D)

Conditions: $V_{CC} = 12V$, $T_A = +25^{\circ}C$, $R_O = 30K\Omega$, $C_O = 0.033\mu F$, unless otherwise specified.

Parameter	Min.	Typ.	Max.	Unit	Conditions
Phase Comparator Section					
Input Impedance		2		MΩ	Measured at Pins 3 and 8
Input Bias Current		100		nA	
Phase Gain	55	70		dB	$R_L = 5.1K\Omega$
Output Voltage Low		300	500	mV	$I_C = 3mA$
Output Leakage Current		0.01	10	μA	$V_O = 20V$
Internal Reference					
Reference Voltage Level	4.9	5.3	5.7	V	Measured at Pin 10
Reference Output Impedance		100		Ω	AC Small Signal
Reference Maximum Source Current		80		μA	

Parameters are guaranteed over the recommended operating conditions, but are not 100% tested in production. Reference parameters are covered by production test and guaranteed over operating temperature range.

Specifications are subject to change without notice

ABSOLUTE MAXIMUM RATINGS

Power Supply	20V
Input Signal Level	3V rms
Power Dissipation	900mW

Package Power Dissipation Ratings

CDIP	750mW
Derate Above $T_A = 25^{\circ}C$	8mW/°C
PDIP	800mW
Derate Above $T_A = 25^{\circ}C$	60mW/°C
SOIC	390mW
Derate Above $T_A = 25^{\circ}C$	5mW/°C

FUNCTION DESCRIPTION

The main PLL within the XR-2211 is constructed from an input preamplifier, analog multiplier used as a phase detector and a precision voltage controlled oscillator (VCO). The preamplifier is used as a limiter such that signals above typically 10mV rms are amplified to a constant high level signal. The multiplying-type phase detector acts as a digital exclusive or gate. Its output (differential) produces sum and difference frequencies of the input and the VCO output. The VCO is actually a voltage controlled oscillator with its normal input current limited by a resistor (R_O) to ground and its driving current limited by a resistor (R_1) from the phase detector.

The output of the phase detector produces sum and difference of the input and the VCO frequencies

(internally connected). When in lock, these frequencies are $f_{IN} + f_{VCO}$ (2 times f_{IN} when in lock) and $f_{IN} - f_{VCO}$ (0Hz when lock). By adding a capacitor to the phase detector output, the 2 times f_{IN} component is reduced, leaving a DC voltage that represents the phase difference between the two frequencies. This closes the loop and allows the VCO to track the input frequency.

The FSK comparator is used to determine if the VCO is driven above or below the center frequency (FSK comparator). This will produce both active high and active low outputs to indicate when the main PLL is in lock (quadrature phase detector and lock detector comparator).

PRINCIPLES OF OPERATION

Signal Input (Pin 2): Signal is AC coupled to this terminal. The internal impedance at pin 2 is 20KΩ. Recommended input signal level is in the range of 10mV rms to 3V rms.

Quadrature Phase Detector Output (Pin 3): This is the high impedance output of quadrature phase detector and is internally connected to the input of lock detect voltage comparator. In tone detection applications, pin 3 is connected to ground through a parallel combination of R_D and C_D (see *Figure 3*) to eliminate the chatter at lock detect outputs. If the tone detect section is not used, pin 3 should be left open.

Lock Detect Output, Q (Pin 6): The output at pin 6 is at "low" state when the PLL is out of lock and goes to "high" state when the PLL is locked. It is an open collector type output and requires a pull-up resistor, R_L , to V_{CC} for proper operation. At "low" state, it can sink up to 5mA of load current.

Lock Detect Complement, (Pin 5): The output at pin 5 is the logic complement of the lock detect output at pin 6. Its output is also an open collector type stage which can sink 5mA of load current at low or "on" state.

FSK Data Output (Pin 7): This output is an open collector type stage which requires a pull-up resistor, R_L , to V_{CC} for proper operation. It can sink 5mA of load current. When encoding FSK signals, FSK data output is at "high" or "off" state for low input frequency, and at "low" or "on" state for high input frequency. If no input signal is present, the logic level at pin 7 is indeterminate.

FSK Comparator Input (Pin 8): This is the high impedance input to the FSK voltage comparator. Internally, an FSK post-detection or data filter is connected between this terminal and the PLL phase detector output (pin 11). This data filter is formed by R_F and C_F (see *Figure 3*.) The threshold voltage of the comparator is set by the internal reference voltage, V_{REF} , available at pin 10.

Reference Voltage, V_{REF} (Pin 10): This pin is internally biased at the reference voltage level, V_{REF} : $V_{REF} = V_{CC}/2$. The DC voltage level at this pin forms an internal reference for the voltage levels at pins 5, 8, 11 and 12. Pin

10 must be bypassed to ground with a 0.1μF capacitor for proper operation of the circuit.

Loop Phase Detector Output (Pin 11): This terminal provides a high impedance output for the loop phase detector. The PLL loop filter is formed by R_1 and C_1 connected to pin 11 (see *Figure 3*.) With no input signal, or with no phase error within the PLL, the DC level at pin 11 is very nearly equal to V_{REF} . The peak to peak voltage swing available at the phase detector output is equal to $2 \times V_{REF}$.

VCO Control Input (Pin 12): VCO free-running frequency is determined by external timing resistor, R_0 , connected from this terminal to ground. The VCO free-running frequency, f_0 , is:

$$f_0 = \frac{1}{R_0 \cdot C_0} \text{ Hz}$$

where C_0 is the timing capacitor across pins 13 and 14. For optimum temperature stability, R_0 must be in the range of 10KΩ to 100KΩ (see *Figure 9*.)

This terminal is a low impedance point, and is internally biased at a DC level equal to V_{REF} . The maximum timing current drawn from pin 12 must be limited to $\leq 3\text{mA}$ for proper operation of the circuit.

VCO Timing Capacitor (Pins 13 and 14): VCO frequency is inversely proportional to the external timing capacitor, C_0 , connected across these terminals (see *Figure 6*.) C_0 must be non-polar, and in the range of 200pF to 10μF.

VCO Frequency Adjustment: VCO can be fine-tuned by connecting a potentiometer, R_X , in series with R_0 at pin 12 (see *Figure 10*.)

VCO Free-Running Frequency, f_0 : XR-2211 does not have a separate VCO output terminal. Instead, the VCO outputs are internally connected to the phase detector sections of the circuit. For set-up or adjustment purposes, the VCO free-running frequency can be tuned by using the generalized circuit in *Figure 3*, and applying an alternating bit pattern of 0's and 1's at the known mark and space frequencies. By adjusting R_0 , the VCO can then be tuned to obtain a 50% duty cycle on the FSK output (pin 7). This will ensure that the VCO f_0 value is accurately referenced to the mark and space frequencies.

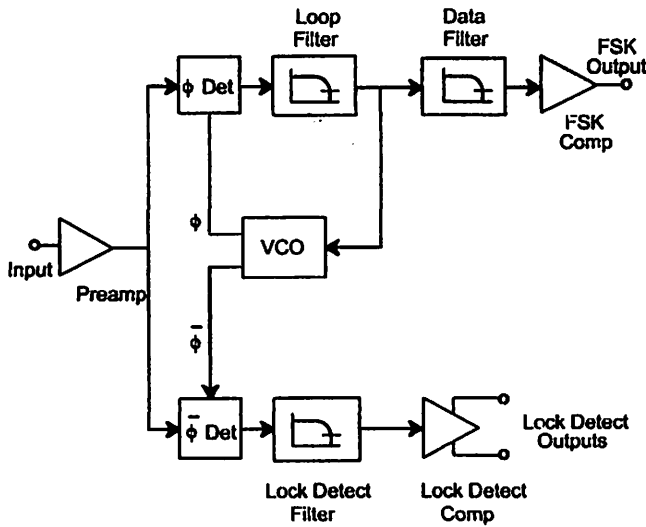


Figure 2. Functional Block Diagram of a Tone and FSK Decoding System Using XR-2211

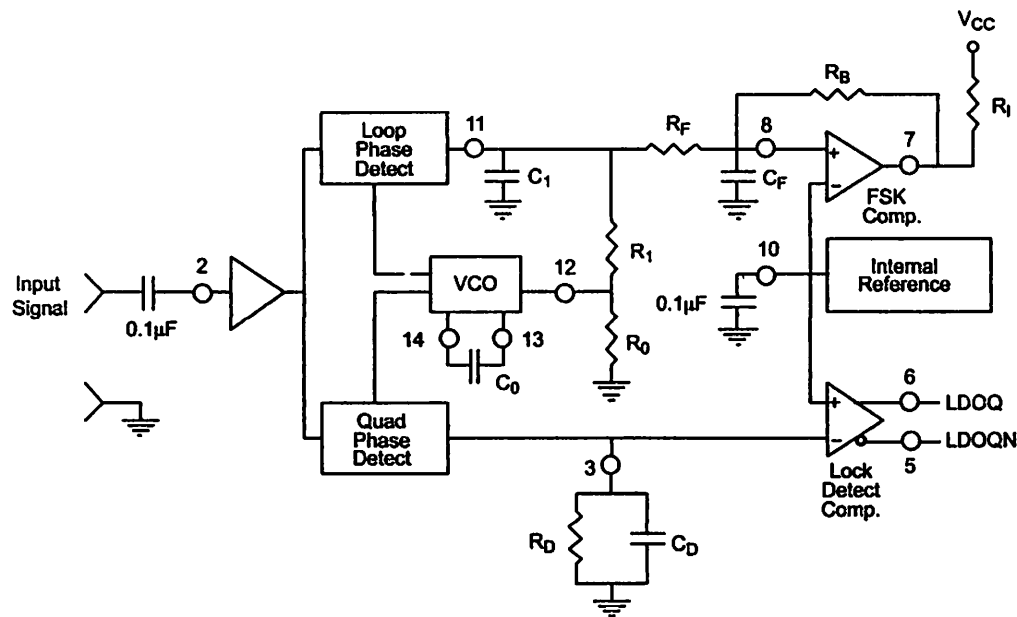


Figure 3. Generalized Circuit Connection for FSK and Tone Detection

SIGN EQUATIONS

resistance in Ω , all frequency in Hz and all capacitance in farads, unless otherwise specified)

(see *Figure 3* for definition of components)

VCO Center Frequency, f_0 :

$$f_0 = \frac{1}{R_0 \cdot C_0}$$

Internal Reference Voltage, V_{REF} (measured at pin 10):

$$V_{REF} = \left(\frac{V_{CC}}{2} \right) - 650mV \text{ in volts}$$

Loop Low-Pass Filter Time Constant, τ :

$$\tau = C_1 \cdot R_{PP} \text{ (seconds)}$$

where:

$$R_{PP} = \left(\frac{R_1 \cdot R_F}{R_1 + R_F} \right)$$

If R_F is ∞ or C_F reactance is ∞ , then $R_{PP} = R_1$

Loop Damping, ζ :

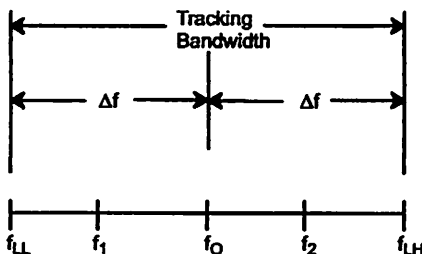
$$\zeta = \sqrt{\left(\frac{1250 \cdot C_0}{R_1 \cdot C_1} \right)}$$

Note: For derivation/explanation of this equation, please see TAN-011.

Loop-tracking

$$\text{Bandwidth, } \pm = \frac{\Delta f}{f_0}$$

$$\frac{\Delta f}{f_0} = \frac{R_0}{R_1}$$



FSK Data filter time constant, t_F :

$$\tau_F = \frac{R_B \cdot R_F}{(R_B + R_F)} \cdot C_F \text{ (seconds)}$$

Loop phase detector conversion gain, K_d : (K_d is the differential DC voltage across pin 10 and pin 11, per unit of phase error at phase detector input):

$$K_d = \frac{V_{REF} \cdot R_1}{10,000 \cdot \pi} \left[\frac{\text{volt}}{\text{radian}} \right]$$

e: For derivation/explanation of this equation, please see TAN-011.

VCO conversion gain, K_o : (K_o is the amount of change in VCO frequency, per unit of DC voltage change at pin 11):

$$K_o = \frac{-2\pi}{V_{REF} \cdot C_o \cdot R_1} = \left(\frac{\text{radian/second}}{\text{volt}} \right)$$

The filter transfer function:

$$F(s) = \frac{1}{1 + SR_1 \cdot C_1} \text{ at } 0 \text{ Hz.} \quad S = j\omega \text{ and } \omega = 0$$

Total loop gain, K_T :

$$K_T = K_o \cdot K_d \cdot F(s) = \left(\frac{R_F}{5,000 \cdot C_o \cdot (R_1 + R_F)} \right) \left[\frac{1}{\text{seconds}} \right]$$

Peak detector current I_A :

$$I_A = \frac{V_{REF}}{20,000} \text{ (} V_{REF} \text{ in volts and } I_A \text{ in amps)}$$

e: For derivation/explanation of this equation, please see TAN-011.

APPLICATIONS INFORMATION

FSK Decoding

Figure 10 shows the basic circuit connection for FSK decoding. With reference to Figure 3 and Figure 10, the functions of external components are defined as follows: R_0 and C_0 set the PLL center frequency, R_1 sets the system bandwidth, C_1 sets the loop filter time constant and the loop damping factor. C_F and R_F form a one-pole post-detection filter for FSK data output. The resistor R_B from pin 7 to pin 8 introduces positive feedback across the FSK comparator to facilitate rapid transition between output logic states.

Design Instructions:

The circuit of Figure 10 can be tailored for any FSK decoding application by the choice of five key circuit components: R_0 , C_0 , C_1 and C_F . For a given set of FSK mark and space frequencies, f_0 and f_1 , these parameters can be calculated as follows:

Resistance in Ω 's, all frequency in Hz and all capacitance in farads, unless otherwise specified)

Calculate PLL center frequency, f_0 :

$$f_0 = \sqrt{F_1 \cdot F_2}$$

Choose value of timing resistor R_0 , to be in the range of 10K Ω to 100K Ω . This choice is arbitrary. The recommended value is $R_0 = 20K\Omega$. The final value of R_0 is normally fine-tuned with the series potentiometer, R_X .

$$R_0 = R_0 + \frac{R_X}{2}$$

Calculate value of C_0 from design equation (1) or from Figure 7:

$$C_0 = \frac{1}{R_0 \cdot f_0}$$

Calculate R_1 to give the desired tracking bandwidth (See design equation 5).

$$R_1 = \frac{R_0 \cdot f_0}{(f_1 - f_2)} \cdot 2$$

Calculate C_1 to set loop damping. (See design equation 4):

Normally, $\zeta = 0.5$ is recommended.

$$C_1 = \frac{1250 \cdot C_0}{R_1 \cdot \zeta^2}$$

The input to the XR-2211 may sometimes be too sensitive to noise conditions on the input line. *Figure 4* illustrates a method of de-sensitizing the XR-2211 from such noisy line conditions by the use of a resistor, R_x , connected from pin 2 to ground. The value of R_x is chosen by the equation and the desired minimum signal threshold level.

$$V_{IN \text{ minimum (peak)}} = V_a - V_b = \Delta V \pm 2.8mV \text{ offset} = V_{REF} \frac{20,000}{(20,000 + R_x)} \text{ or } R_x = 20,000 \left(\frac{V_{REF}}{\Delta V} - 1 \right)$$

minimum (peak) input voltage must exceed this value to be detected (equivalent to adjusting V threshold)

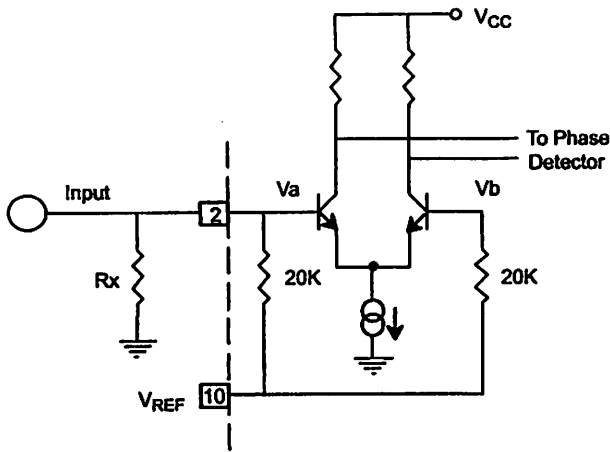


Figure 4. Desensitizing Input Stage

Calculate Data Filter Capacitance, C_F :

$$R_{sum} = \frac{(R_F + R_1) \cdot R_B}{(R_1 + R_F + R_B)}$$

$$C_F = \frac{0.25}{(R_{sum} \cdot \text{Baud Rate})} \quad \text{Baud rate in } \frac{1}{\text{seconds}}$$

: All values except R_0 can be rounded to nearest standard value.

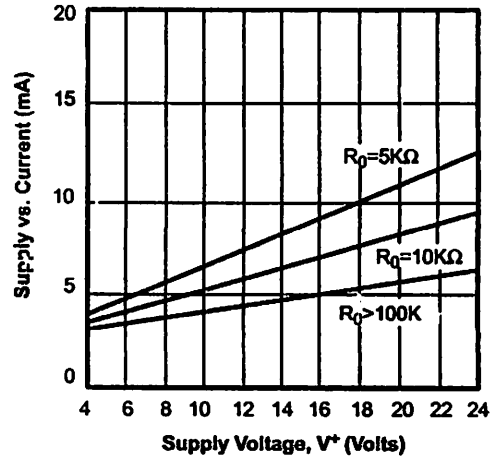


Figure 5. Typical Supply Current vs. V+ (Logic Outputs Open Circuited)

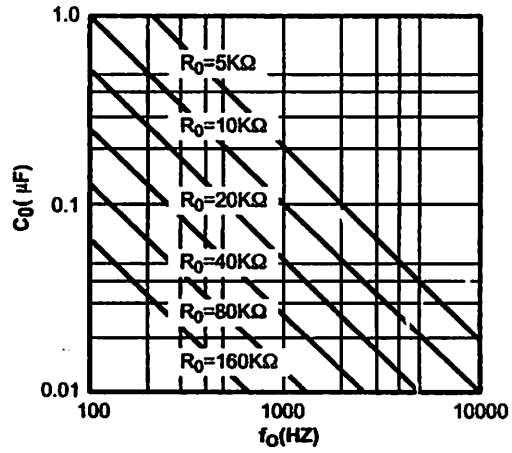


Figure 6. VCO Frequency vs. Timing Resistor

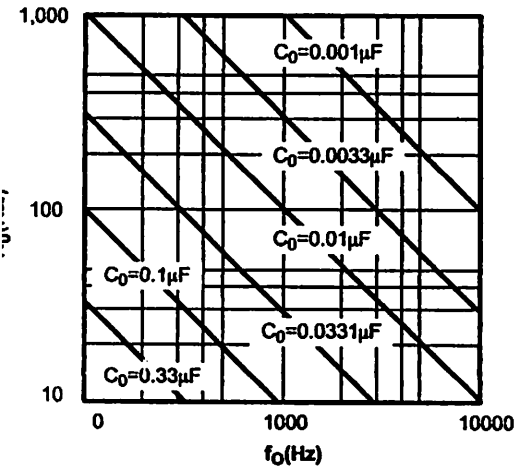


Figure 7. VCO Frequency vs. Timing Capacitor

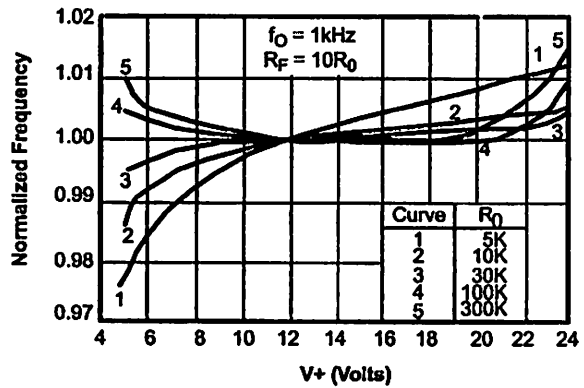


Figure 8. Typical f_0 vs. Power Supply Characteristics

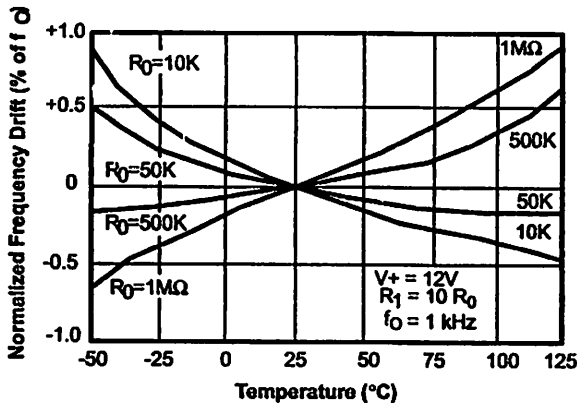


Figure 9. Typical Center Frequency Drift vs. Temperature

Design Example:

Design Example: Baud FSK demodulator with mark and space frequencies of 1200/2200.

1: Calculate f_0 : from design instructions

$$(a) f_0 = \sqrt{1200 \cdot 2200} = 1624$$

2: Calculate R_0 : $R_0 = 10K$ with a potentiometer of 10K. (See design instructions (b))

$$(b) R_T = 10 + \left(\frac{10}{2}\right) = 15K$$

3: Calculate C_0 from design instructions

$$(c) C_0 = \frac{1}{15000 \cdot 1624} = 39nF$$

4: Calculate R_1 : from design instructions

$$(d) R_1 = \frac{20000 \cdot 1624 \cdot 2}{(2200 - 1200)} = 51,000$$

5: Calculate C_1 : from design instructions

$$(e) C_1 = \frac{1250 \cdot 39nF}{51000 \cdot 0.5^2} = 3.9nF$$

6: Calculate R_F : R_F should be at least five times R_1 , $R_F = 51,000 \cdot 5 = 255 K\Omega$

7: Calculate R_B : R_B should be at least five times R_F , $R_B = 255,000 \cdot 5 = 1.2 M\Omega$

8: Calculate R_{SUM} :

$$R_{SUM} = \frac{(R_F + R_1) \cdot R_B}{(R_F + R_1 + R_B)} = 240K\Omega$$

9: Calculate C_F :

$$C_F = \frac{0.25}{(R_{SUM} \cdot \text{Baud Rate})} = 1nF$$

: All values except R_0 can be rounded to nearest standard value.

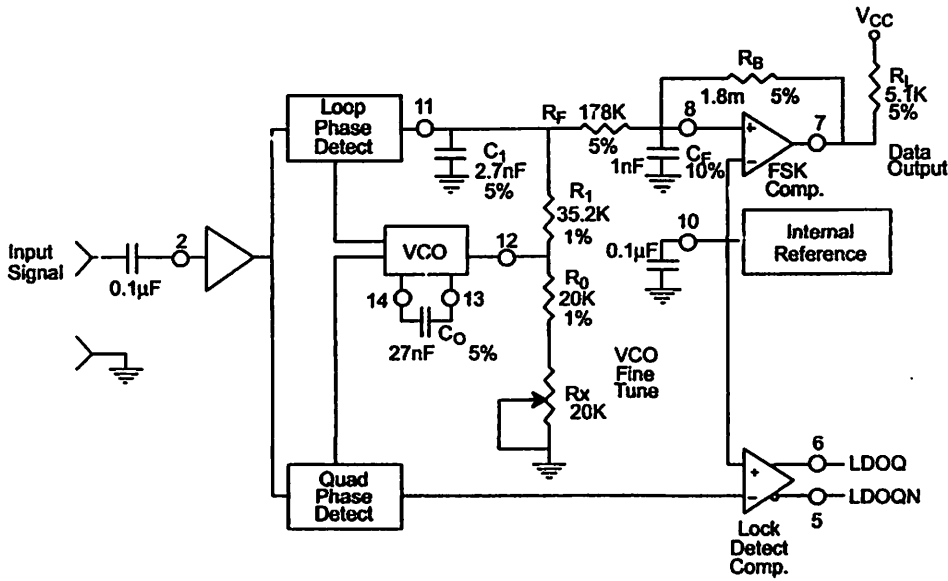


Figure 10. Circuit Connection for FSK Decoding of Caller Identification Signals (Bell 202 Format)

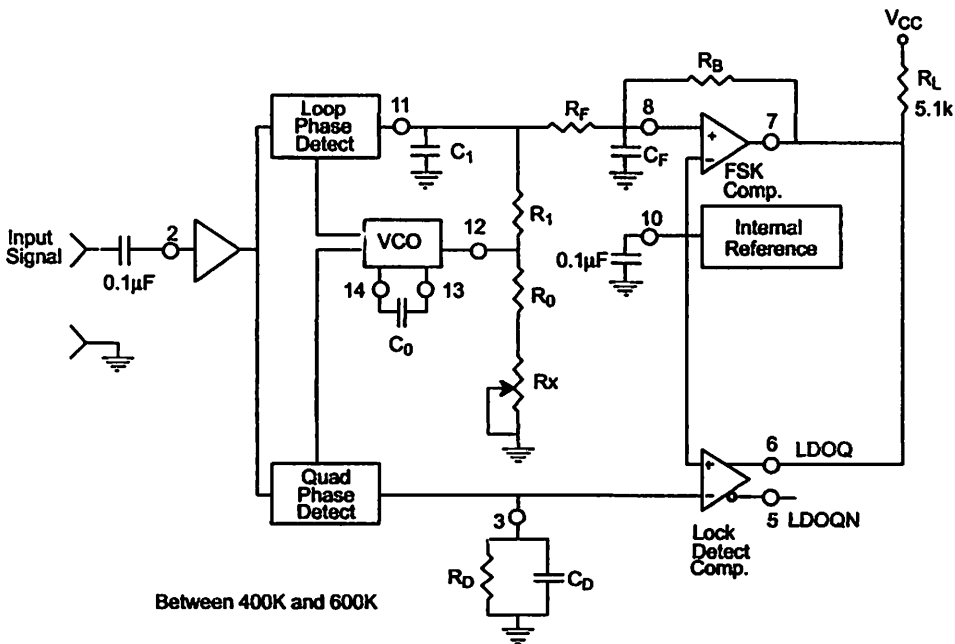


Figure 11. External Connectors for FSK Demodulation with Carrier Detect Capability

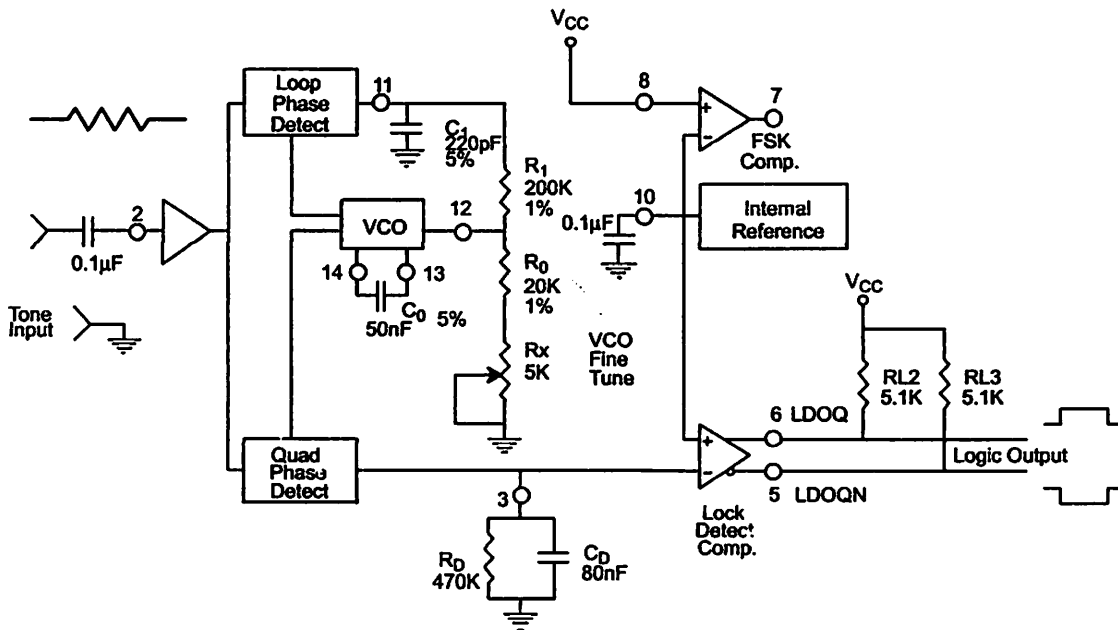


Figure 12. Circuit Connection for Tone Detection

Decoding with Carrier Detect

The lock detect section of XR-2211 can be used as a carrier detect option for FSK decoding. The recommended circuit connection for this application is shown in Figure 11. The open collector lock detect output, LDOQN, is shorted to data output (pin 7). Thus, data output is disabled at "low" state, until there is a carrier within the detection band of the PLL and the pin 6 output goes high to enable the data output.

Data Output is "Low" When No Carrier is Present.

The minimum value of the lock detect filter capacitance is inversely proportional to the capture range, $\pm\Delta f_c$, the range of incoming frequencies over which the PLL can acquire lock and is always less than the tracking range. It is further limited by C_D . For most applications, Δf_c is 1%. For $R_D = 470K\Omega$, the approximate minimum value can be determined by:

$$C_D > \frac{16}{\Delta f} \quad C \text{ in } \mu F \text{ and } f \text{ in Hz.}$$

C_D in μF and f in Hz.

Large values of C_D that are too small, chatter can be observed on the lock detect output as an incoming signal

frequency approaches the capture bandwidth. Excessively large values of C_D will slow the response time of the lock detect output. For Caller I.D. applications choose $C_D = 0.1\mu F$.

Tone Detection

Figure 12 shows the generalized circuit connection for tone detection. The logic outputs, LDOQN and LDOQ at pins 5 and 6 are normally at "high" and "low" logic states, respectively. When a tone is present within the detection band of the PLL, the logic state at these outputs become reversed for the duration of the input tone. Each logic output can sink 5mA of load current.

Both outputs at pins 5 and 6 are open collector type stages, and require external pull-up resistors R_{L2} and R_{L3} , as shown in Figure 12.

With reference to Figure 3 and Figure 12, the functions of the external circuit components can be explained as follows: R_0 and C_0 set VCO center frequency; R_1 sets the detection bandwidth; C_1 sets the low pass-loop filter time constant and the loop damping factor.

Design Instructions:

The circuit of Figure 12 can be optimized for any tone detection application by the choice of the 5 key circuit components: R_0 , C_0 , C_1 and C_D . For a given input, the tone frequency, f_S , these parameters are calculated as follows:

(Resistance in Ω 's, all frequency in Hz and all capacitance in farads, unless otherwise specified)

Choose value of timing resistor R_0 to be in the range of 10K Ω to 50K Ω . This choice is dictated by the max./min. current that the internal voltage reference can deliver. The recommended value is $R_0 = 20K\Omega$. The final value of R_0 is normally fine-tuned with the series potentiometer, R_X .

Calculate value of C_0 from design equation (1) or from Figure 7 $f_S = f_0$:

$$C_0 = \frac{1}{R_0 \cdot f_S}$$

Calculate R_1 to set the bandwidth $\pm \Delta f$ (See design equation 5):

$$R_1 = \frac{R_0 \cdot f_0 \cdot 2}{\Delta f}$$

The total detection bandwidth covers the frequency range of $f_0 \pm \Delta f$

Calculate value of C_1 for a given loop damping factor:

Normally, $\zeta = 0.5$ is recommended.

$$C_1 = \frac{1250 \cdot C_0}{R_1 \cdot \zeta^2}$$

Increasing C_1 improves the out-of-band signal rejection, but increases the PLL capture time.

Calculate value of the filter capacitor C_D . To avoid chatter at the logic output, with $R_D = 470K\Omega$, C_D must be:

$$C_D > \frac{16}{\Delta f} \quad C \text{ in } \mu F$$

Increasing C_D slows down the logic output response time.

Design Examples:

Detector with a detection band of $\pm 100\text{Hz}$:

Choose value of timing resistor R_0 to be in the range of 10K Ω to 50K Ω . This choice is dictated by the max./min. current that the internal voltage reference can deliver. The recommended value is $R_0 = 20K\Omega$. The final value of R_0 is normally fine-tuned with the series potentiometer, R_X .

Calculate value of C_0 from design equation (1) or from Figure 6 $f_S = f_0$:

$$C_0 = \frac{1}{R_0 \cdot f_S} = \frac{1}{20,000 \cdot 1,000} = 50\text{nF}$$

Calculate R_1 to set the bandwidth $\pm\Delta f$ (See design equation 5):

$$R_1 = \frac{R_0 \cdot f_0 \cdot 2}{\Delta f} = \frac{20,000 \cdot 1,000 \cdot 2}{100} = 400K$$

The total detection bandwidth covers the frequency range of $f_0 \pm \Delta f$

Calculate value of C_0 for a given loop damping factor:

Normally, $\zeta = 0.5$ is recommended.

$$C_1 = \frac{1250 \cdot C_0}{R_1 \cdot \zeta^2} = \frac{1250 \cdot 50 \cdot 10^{-9}}{400,000 \cdot 0.5^2} = 6.25pF$$

Increasing C_1 improves the out-of-band signal rejection, but increases the PLL capture time.

Calculate value of the filter capacitor C_D . To avoid chatter at the logic output, with $R_D = 470K\Omega$, C_D must be:

$$C_D = \frac{16}{\Delta f} \geq \frac{16}{200} \geq 80nF$$

Increasing C_D slows down the logic output response time.

Fine tune center frequency with $5K\Omega$ potentiometer, R_X .

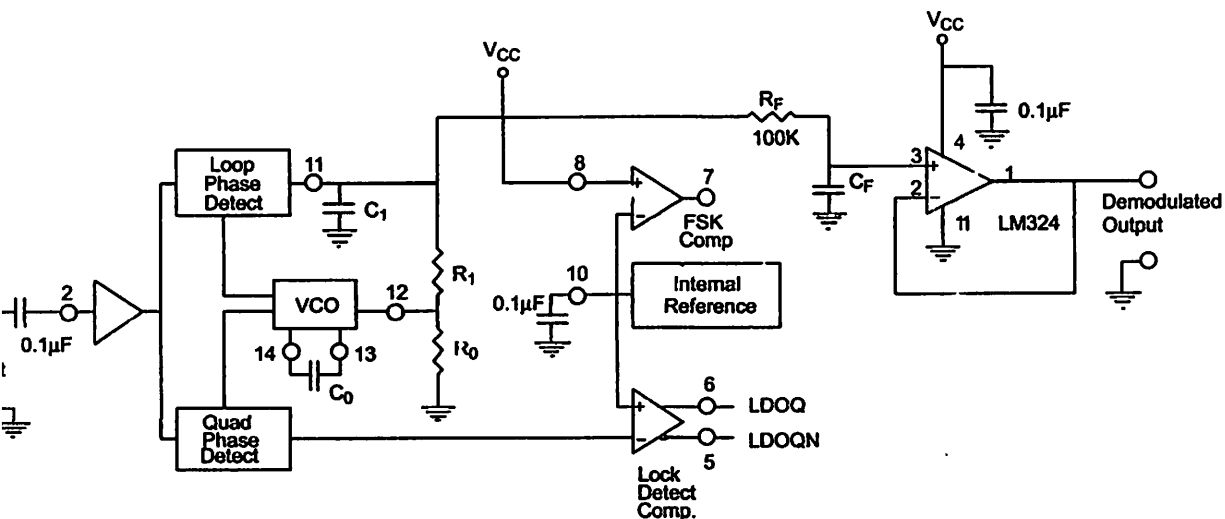


Figure 13. Linear FM Detector Using XR-2211 and an External Op Amp.
(See Section on Design Equation for Component Values.)

FM Detection

The R-2211 can be used as a linear FM detector for a wide range of analog communications and telemetry applications. The recommended circuit connection for this application is shown in Figure 13. The demodulated signal is taken from the loop phase detector output (pin 11) through a post-detection filter made up of R_F and C_F in an external buffer amplifier. This buffer amplifier is necessary because of the high impedance output at pin 11. Normally, a non-inverting unity gain op amp can be used as a buffer amplifier, as shown in Figure 13.

The FM detector gain, i.e., the output voltage change per unit of FM deviation can be given as:

$$V_{OUT} = \frac{R_1 \cdot V_{REF}}{100 \cdot R_0}$$

where V_R is the internal reference voltage ($V_{REF} = V_{CC}/2 - 650mV$). For the choice of external components R_1 , R_0 , C_D , C_1 and C_F , see the section on design equations.

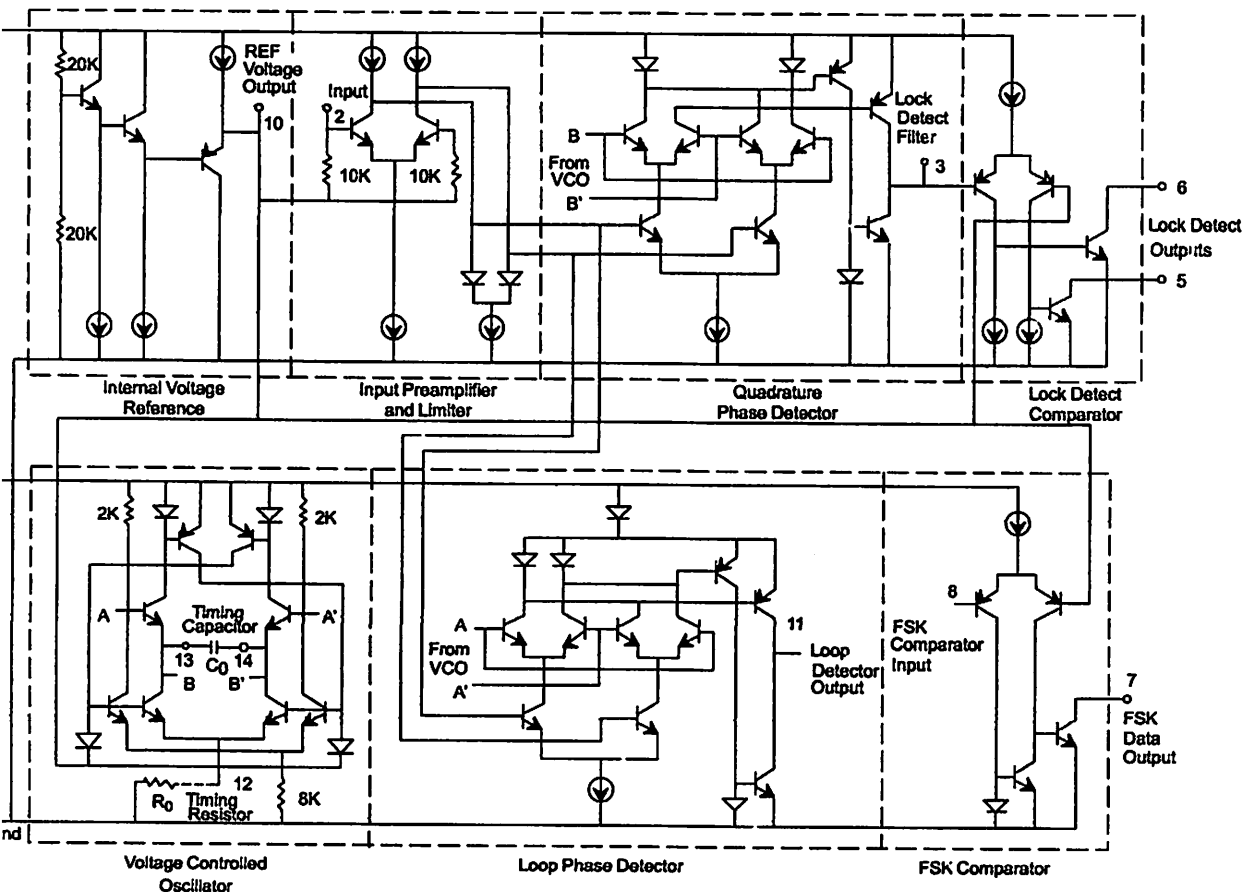
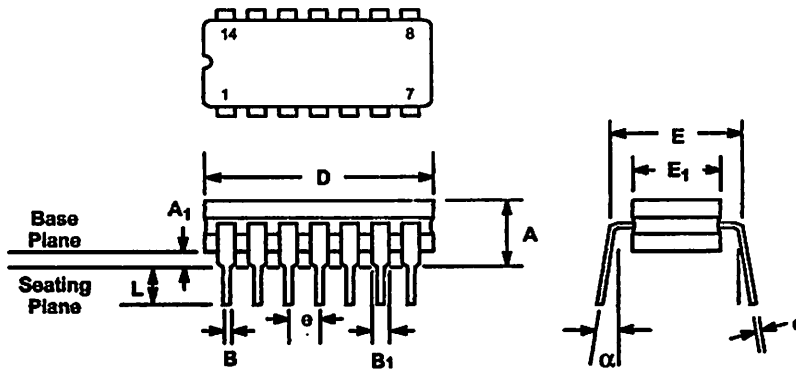


Figure 14. Equivalent Schematic Diagram

**14 LEAD CERAMIC DUAL-IN-LINE
(300 MIL CDIP)**

Rev. 1.00

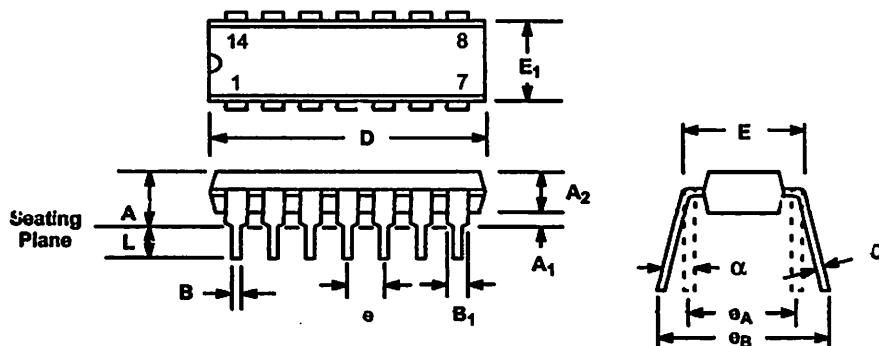


SYMBOL	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.100	0.200	2.54	5.08
A ₁	0.015	0.060	0.38	1.52
B	0.014	0.026	0.36	0.66
B ₁	0.045	0.065	1.14	1.65
c	0.008	0.018	0.20	0.46
D	0.685	0.785	17.40	19.94
E ₁	0.250	0.310	6.35	7.87
E	0.300 BSC		7.62 BSC	
e	0.100 BSC		2.54 BSC	
L	0.125	0.200	3.18	5.08
α	0°	15°	0°	15°

Note: The control dimension is the inch column

14 LEAD PLASTIC DUAL-IN-LINE (300 MIL PDIP)

Rev. 1.00

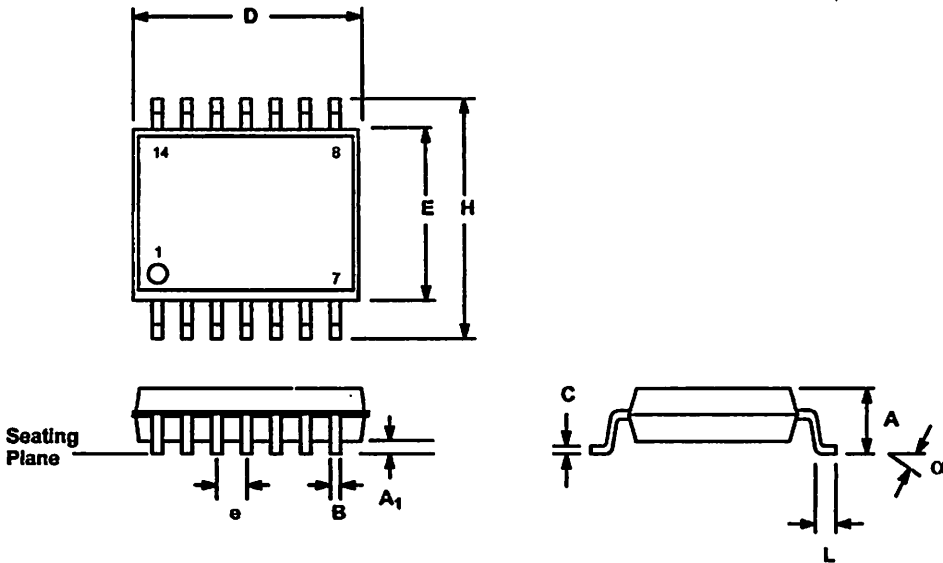


SYMBOL	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.145	0.210	3.68	5.33
A ₁	0.015	0.070	0.38	1.78
A ₂	0.115	0.195	2.92	4.95
B	0.014	0.024	0.36	0.56
B ₁	0.030	0.070	0.76	1.78
C	0.008	0.014	0.20	0.38
D	0.725	0.795	18.42	20.19
E	0.300	0.325	7.62	8.26
E ₁	0.240	0.280	6.10	7.11
e	0.100 BSC		2.54 BSC	
e _A	0.300 BSC		7.62 BSC	
e _B	0.310	0.430	7.87	10.92
L	0.115	0.160	2.92	4.06
α	0°	15°	0°	15°

Note: The control dimension is the inch column

**14 LEAD SMALL OUTLINE
(150 MIL JEDEC SOIC)**

Rev. 1.00



SYMBOL	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.053	0.069	1.35	1.75
A ₁	0.004	0.010	0.10	0.25
B	0.013	0.020	0.33	0.51
C	0.007	0.010	0.19	0.25
D	0.337	0.344	8.55	8.75
E	0.150	0.157	3.80	4.00
e	0.050 BSC		1.27 BSC	
H	0.228	0.244	5.80	6.20
L	0.016	0.050	0.40	1.27
α	0°	8°	0°	8°

Note: The control dimension is the millimeter column

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MM74C922 • MM74C923 16-Key Encoder • 20-Key Encoder

General Description

The MM74C922 and MM74C923 CMOS key encoders provide all the necessary logic to fully encode an array of SPST switches. The keyboard scan can be implemented by either an external clock or external capacitor. These encoders also have on-chip pull-up devices which permit switches with up to 50 kΩ on resistance to be used. No diodes in the switch array are needed to eliminate ghost switches. The internal debounce circuit needs only a single external capacitor and can be defeated by omitting the capacitor. A Data Available output goes to a high level when a valid keyboard entry has been made. The Data Available output returns to a low level when the entered key is released, even if another key is depressed. The Data Available will return high to indicate acceptance of the new key after a normal debounce period; this two-key roll-over is provided between any two switches.

An internal register remembers the last key pressed even after the key is released. The 3-STATE outputs provide for easy expansion and bus operation and are LPTTL compatible.

Features

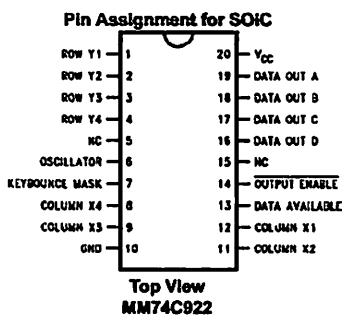
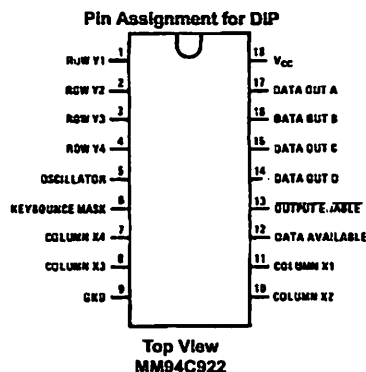
- 50 kΩ maximum switch on resistance
- On or off chip clock
- On-chip row pull-up devices
- 2 key roll-over
- Keybounce elimination with single capacitor
- Last key register at outputs
- 3-STATE output LPTTL compatible
- Wide supply range: 3V to 15V
- Low power consumption

Ordering Code:

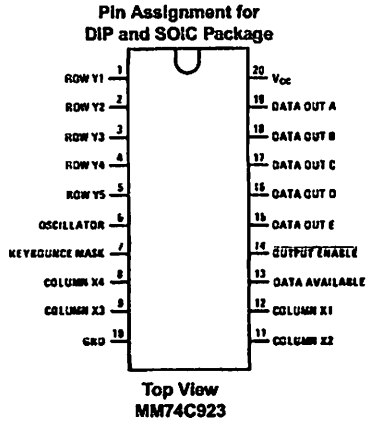
Order Number	Package Number	Package Description
MM74C922N	N18A	18-Lead Plastic Dual-in-Line Package (PDIP), JEDEC MS-001, 0.300" Wide
MM74C922WM	M20B	20-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-013, 0.300" Wide
MM74C923WM	M20B	20-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-013, 0.300" Wide
MM74C923N	N20A	20-Lead Plastic Dual-in-Line Package (PDIP), JEDEC MS-001, 0.300" Wide

Device also available in Tape and Reel. Specify by appending suffix letter "X" to the ordering code.

Connection Diagrams



Connection Diagrams (Continued)



Truth Tables

(Pins 0 through 11)

Switch Position	0	1	2	3	4	5	6	7	8	9	10	11
	Y1,X1	Y1,X2	Y1,X3	Y1,X4	Y2,X1	Y2,X2	Y2,X3	Y2,X4	Y3,X1	Y3,X2	Y3,X3	Y3,X4
D												
A A	0	1	0	1	0	1	0	1	0	1	0	1
T B	0	0	1	1	0	0	1	1	0	0	1	1
A C	0	0	0	0	1	1	1	1	0	0	0	0
O D	0	0	0	0	0	0	0	0	1	1	1	1
U E (Note 1)	0	0	0	0	0	0	0	0	0	0	0	0
T												

(Pins 12 through 19)

Switch Position	12	13	14	15	16	17	18	19
	Y4,X1	Y4,X2	Y4,X3	Y4,X4	Y5 (Note 1), X1	Y5 (Note 1), X2	Y5 (Note 1), X3	Y5 (Note 1), X4
D								
A A	0	1	0	1	0	1	0	1
T B	0	0	1	1	0	0	1	1
A C	1	1	1	1	0	0	0	0
O D	1	1	1	1	0	0	0	0
U E (Note 1)	0	0	0	0	1	1	1	1
T								

Note 1: Omk for MM74C922

Absolute Maximum Ratings(Note 2)

Voltage at Any Pin	$V_{CC} - 0.3V$ to $V_{CC} + 0.3V$
Operating Temperature Range	MM74C922, MM74C923 -40°C to +85°C
Storage Temperature Range	-65°C to +150°C
Power Dissipation (P_D)	
Dual-In-Line	700 mW
Small Outline	500 mW

Operating V_{CC} Range

3V to 15V

 V_{CC}

18V

Lead Temperature

(Soldering, 10 seconds)

260°C

Note 2: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Temperature Range" they are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

DC Electrical Characteristics

Min/Max limits apply across temperature range unless otherwise specified

Symbol	Parameter	Conditions	Min	Typ	Max	Units
CMOS TO CMOS						
V_{T+}	Positive-Going Threshold Voltage at Osc and KBM Inputs	$V_{CC} = 5V, I_{IN} \geq 0.7$ mA $V_{CC} = 10V, I_{IN} \geq 1.4$ mA $V_{CC} = 15V, I_{IN} \geq 2.1$ mA	3.0 6.0 9.0	3.6 6.8 10	4.3 8.6 12.9	V
V_{T-}	Negative-Going Threshold Voltage at Osc and KBM Inputs	$V_{CC} = 5V, I_{IN} \geq 0.7$ mA $V_{CC} = 10V, I_{IN} \geq 1.4$ mA $V_{CC} = 15V, I_{IN} \geq 2.1$ mA	0.7 1.4 2.1	1.4 3.2 5	2.0 4.0 6.0	V
$V_{IN(1)}$	Logical "1" Input Voltage, Except Osc and KBM Inputs	$V_{CC} = 5V$ $V_{CC} = 10V$ $V_{CC} = 15V$	3.5 8.0 12.5	4.5 9 13.5		V
$V_{IN(0)}$	Logical "0" Input Voltage, Except Osc and KBM Inputs	$V_{CC} = 5V$ $V_{CC} = 10V$ $V_{CC} = 15V$		0.5 1 1.5	1.5 2 2.5	V
I_P	Row Pull-Up Current at Y1, Y2, Y3, Y4 and Y5 Inputs	$V_{CC} = 5V, V_{IN} = 0.1 V_{CC}$ $V_{CC} = 10V$ $V_{CC} = 15V$		-2 -10 -22	-5 -20 -45	μA
$V_{OUT(1)}$	Logical "1" Output Voltage	$V_{CC} = 5V, I_O = -10$ μA $V_{CC} = 10V, I_O = -10$ μA $V_{CC} = 15V, I_O = -10$ μA	4.5 9 13.5			V
$V_{OUT(0)}$	Logical "0" Output Voltage	$V_{CC} = 5V, I_O = 10$ μA $V_{CC} = 10V, I_O = 10$ μA $V_{CC} = 15V, I_O = 10$ μA			0.5 1 1.5	V
R_{ON}	Column "ON" Resistance at X1, X2, X3 and X4 Outputs	$V_{CC} = 5V, V_O = 0.5V$ $V_{CC} = 10V, V_O = 1V$ $V_{CC} = 15V, V_O = 1.5V$		500 300 200	1400 700 500	Ω
I_{CC}	Supply Current Osc at 0V, (one Y low)	$V_{CC} = 5V$ $V_{CC} = 10V$ $V_{CC} = 15V$		0.55 1.1 1.7	1.1 1.9 2.6	mA
$I_{IN(1)}$	Logical "1" Input Current at Output Enable	$V_{CC} = 15V, V_{IN} = 15V$		0.005	1.0	μA
$I_{IN(0)}$	Logical "0" Input Current at Output Enable	$V_{CC} = 15V, V_{IN} = 0V$	-1.0	-0.005		μA
CMOS/LPTTL INTERFACE						
$V_{IN(1)}$	Except Osc and KBM Inputs	$V_{CC} = 4.75V$	$V_{CC} - 1.5$			V
$V_{IN(0)}$	Except Osc and KBM Inputs	$V_{CC} = 4.75V$			0.8	V
$V_{OUT(1)}$	Logical "1" Output Voltage	$I_O = -360$ μA $V_{CC} = 4.75V$ $I_O = -360$ μA	2.4			V
$V_{OUT(0)}$	Logical "0" Output Voltage	$I_O = -360$ μA $V_{CC} = 4.75V$ $I_O = -360$ μA			0.4	V

DC Electrical Characteristics (Continued)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
OUTPUT DRIVE (See Family Characteristics Data Sheet) (Short Circuit Current)						
I_{SOURCE}	Output Source Current (P-Channel)	$V_{CC} = 5V, V_{OUT} = 0V,$ $T_A = 25^\circ C$	-1.75	-3.3		mA
I_{SOURCE}	Output Source Current (P-Channel)	$V_{CC} = 10V, V_{OUT} = 0V,$ $T_A = 25^\circ C$	-8	-15		mA
I_{SINK}	Output Sink Current (N-Channel)	$V_{CC} = 5V, V_{OUT} = V_{CC},$ $T_A = 25^\circ C$	1.75	3.6		mA
I_{SINK}	Output Sink Current (N-Channel)	$V_{CC} = 10V, V_{OUT} = V_{CC},$ $T_A = 25^\circ C$	8	16		mA

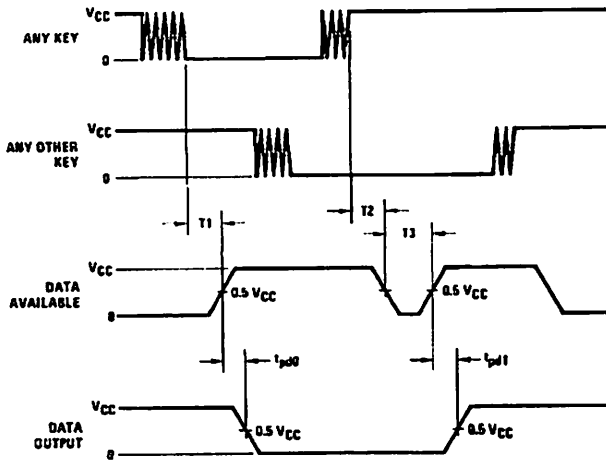
AC Electrical Characteristics (Note 3) $T_A = 25^\circ C, C_L = 50$ pF, unless otherwise noted

Symbol	Parameter	Conditions	Min	Typ	Max	Units
t_{PD}, t_{pD1}	Propagation Delay Time to Logical "0" or Logical "1" from D.A.	$C_L = 50$ pF (Figure 1) $V_{CC} = 5V$ $V_{CC} = 10V$ $V_{CC} = 15V$		60 35 25	150 80 60	ns ns ns
t_{QH}, t_{1H}	Propagation Delay Time from Logical "0" or Logical "1" into High Impedance State	$R_L = 10k, C_L = 10$ pF (Figure 2) $V_{CC} = 5V, R_L = 10k$ $V_{CC} = 10V, C_L = 10$ pF $V_{CC} = 15V$		80 65 50	200 150 110	ns ns ns
t_{HD}, t_{H1}	Propagation Delay Time from High Impedance State to a Logical "0" or Logical "1"	$R_L = 10k, C_L = 50$ pF (Figure 2) $V_{CC} = 5V, R_L = 10k$ $V_{CC} = 10V, C_L = 50$ pF $V_{CC} = 15V$		100 55 40	250 125 90	ns ns ns
C_{IN}	Input Capacitance	Any Input (Note 4)		5	7.5	pF
C_{OUT}	3-STATE Output Capacitance	Any Output (Note 4)		10		pF

Note 3: AC Parameters are guaranteed by DC correlated testing.

Note 4: Capacitance is guaranteed by periodic testing.

Switching Time Waveforms



$T1 = T2 = RC$, $T3 = 0.7 RC$, where $R = 10k$ and C is external capacitor at KBM input.

FIGURE 1.

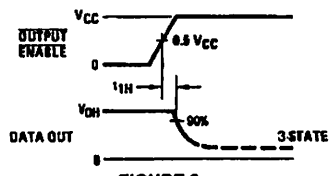
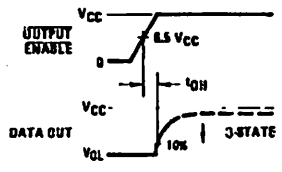
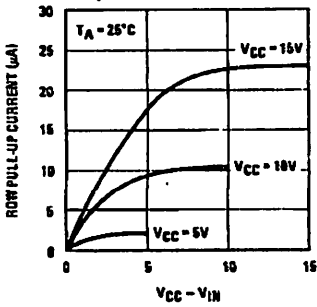


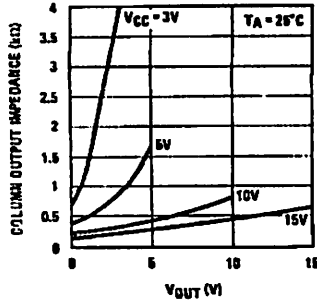
FIGURE 2.

Typical Performance Characteristics

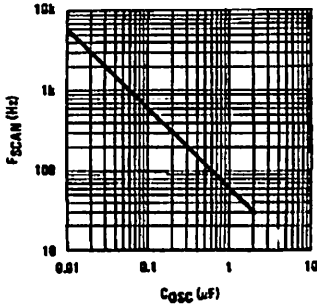
Typical I_{TP} vs V_{IN} at Any Y Input



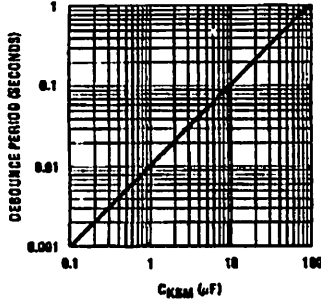
Typical R_{ON} vs V_{OUT} at Any X Output



Typical F_{SCAN} vs C_{OSC}

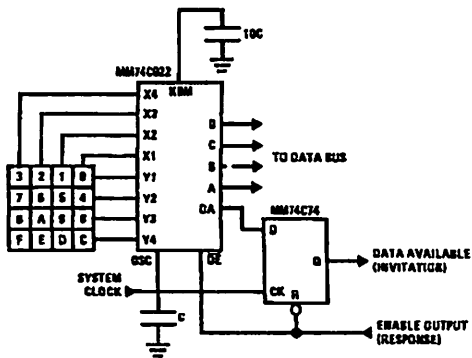


Typical Debounce Period vs C_{KBM}



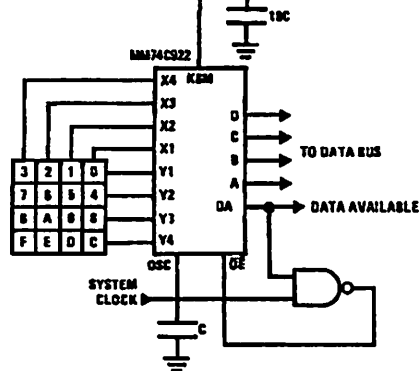
Typical Applications

Synchronous Handshake (MM74C922)



The keyboard may be synchronously scanned by omitting the capacitor at osc. and driving osc. directly if the system clock rate is lower than 10 kHz

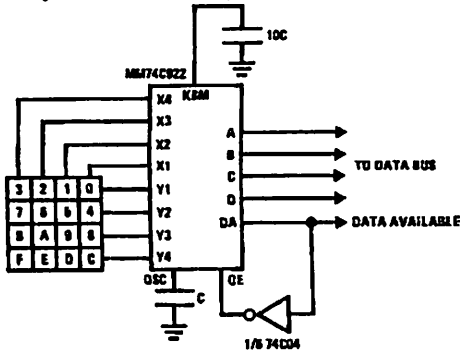
Synchronous Data Entry Onto Bus (MM74C922)



Outputs are enabled when valid entry is made and go into 3-STATE when key is released.

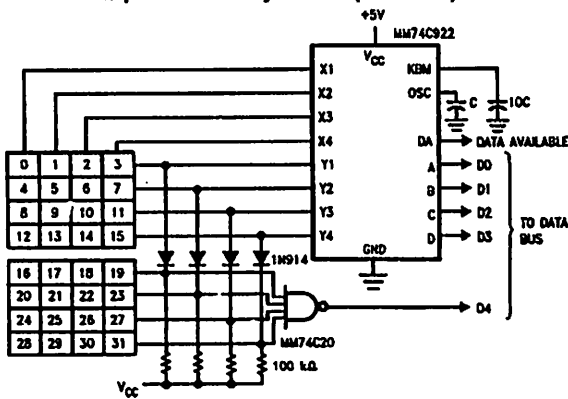
The keyboard may be synchronously scanned by omitting the capacitor at osc. and driving osc. directly if the system clock rate is lower than 10 kHz

Asynchronous Data Entry Onto Bus (MM74C922)



Outputs are in 3-STATE until key is pressed, then data is placed on bus. When key is released, outputs return to 3-STATE.

Expansion to 32 Key Encoder (MM74C922)



Theory of Operation

The MM74C922/MM74C923 Keyboard Encoders implement all the logic necessary to interface a 16 or 20 SPST key switch matrix to a digital system. The encoder will convert a key switch closure to a 4 (MM74C922) or 5 (MM74C923) bit nibble. The designer can control both the keyboard scan rate and the key debounce period by altering the oscillator capacitor, C_{OSC} , and the key bounce mask capacitor, C_{MSK} . Thus, the MM74C922/MM74C923's performance can be optimized for many keyboards.

The keyboard encoders connect to a switch matrix that is 4 rows by 4 columns (MM74C922) or 5 rows by 4 columns (MM74C923). When no keys are depressed, the row inputs are pulled high by internal pull-ups and the column outputs sequentially output a logic "0". These outputs are open drain and are therefore low for 25% of the time and otherwise off. The column scan rate is controlled by the oscillator input, which consists of a Schmitt trigger oscillator, a 2-bit counter, and a 2-4-bit decoder.

When a key is depressed, key 0, for example, nothing will happen when the X1 input is off, since Y1 will remain high. When the X1 column is scanned, X1 goes low and Y1 will go low. This disables the counter and keeps X1 low. Y1

going low also initiates the key bounce circuit timing and locks out the other Y inputs. The key code to be output is a combination of the frozen counter value and the decoded Y inputs. Once the key bounce circuit times out, the data is latched, and the Data Available (DAV) output goes high.

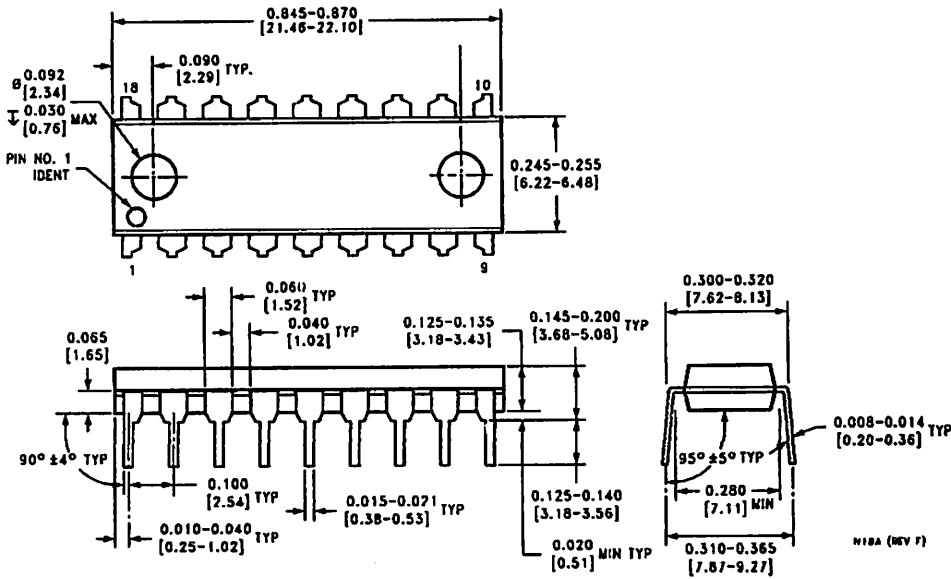
If, during the key closure the switch bounces, Y1 input will go high again, restarting the scan and resetting the key bounce circuitry. The key may bounce several times, but as soon as the switch stays low for a debounce period, the closure is assumed valid and the data is latched.

A key may also bounce when it is released. To ensure that the encoder does not recognize this bounce as another key closure, the debounce circuit must time out before another closure is recognized.

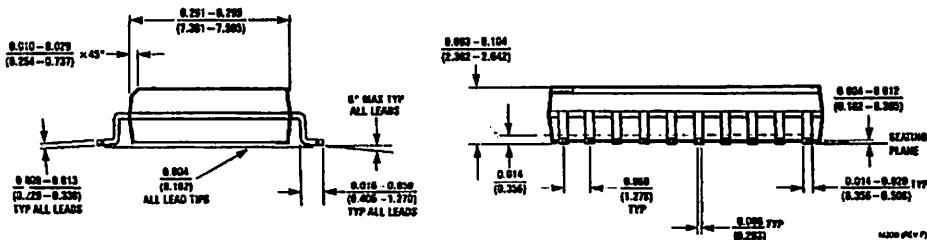
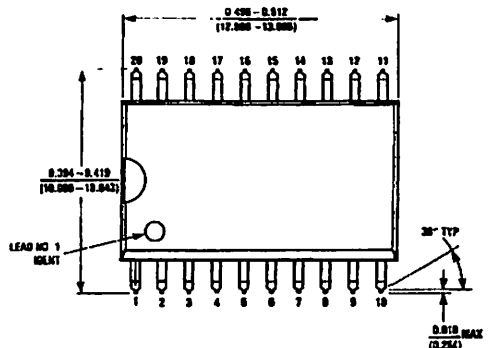
The two-key roll-over feature can be illustrated by assuming a key is depressed, and then a second key is depressed. Since all scanning has stopped, and all other Y inputs are disabled, the second key is not recognized until the first key is lifted and the key bounce circuitry has reset.

The output latches 3-STATE, which is enabled when the Output Enable (\overline{OE}) input is taken low.

Physical Dimensions inches (millimeters) unless otherwise noted

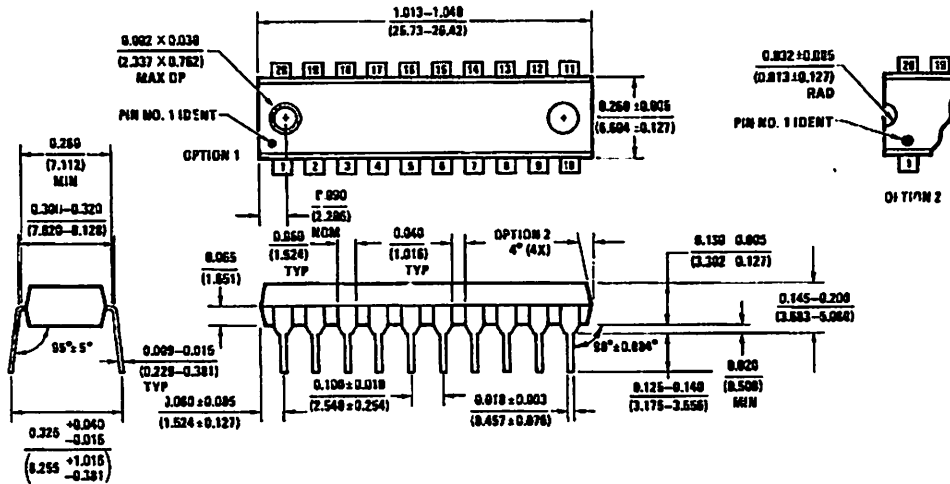


18-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300" Wide
Package Number N18A



20-Lead Plastic Small Outline L.C. Package (M)
Package Number M20B

Physical Dimensions inches (millimeters) unless otherwise noted (Continued)



20-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.310" Wide
Package Number N20A

LIFE SUPPORT POLICY

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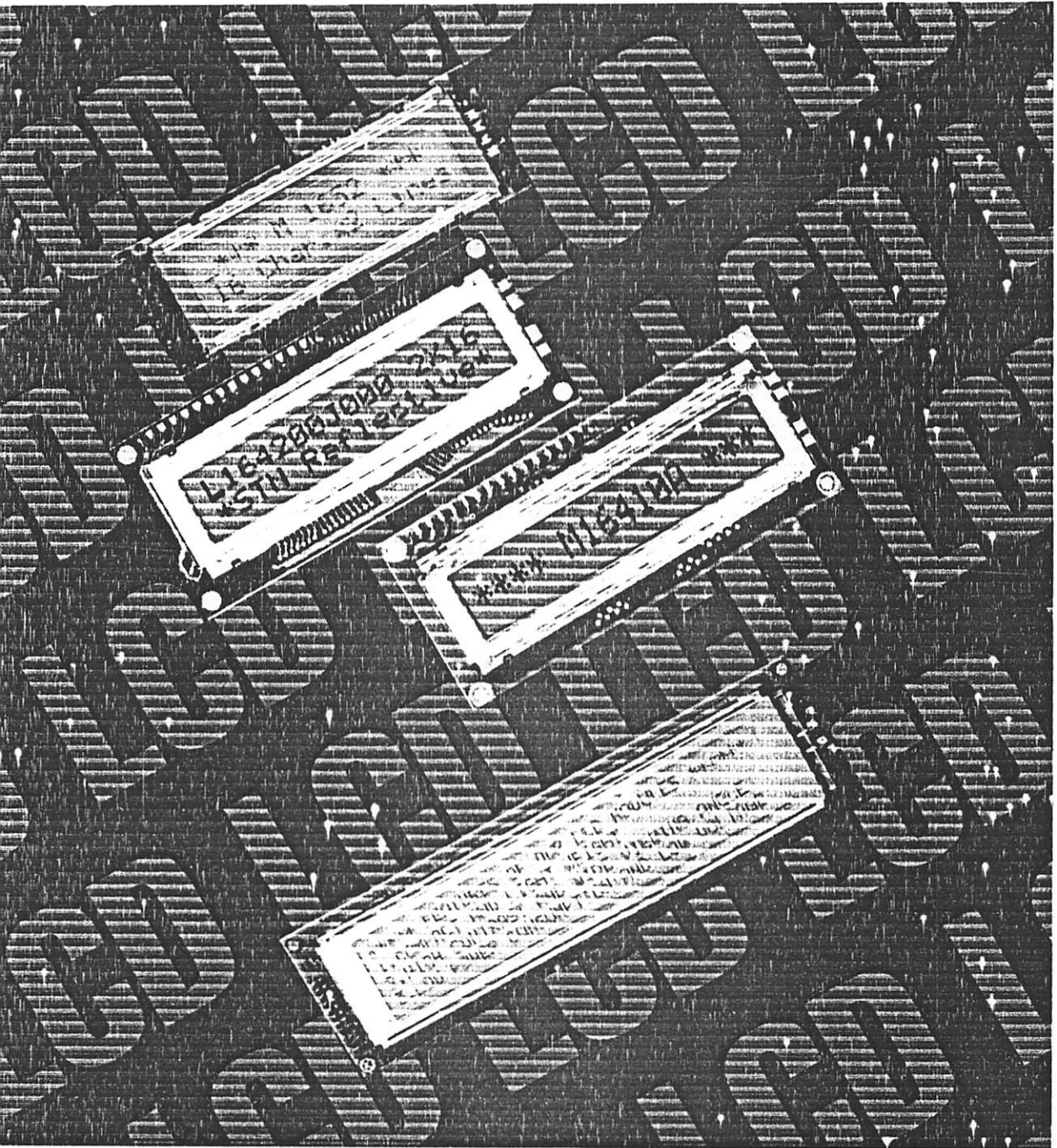
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2. A critical component in any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

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LCM

Liquid Crystal Display Modules

Seiko Instruments GmbH



Dot Matrix Liquid Crystal Display Modules

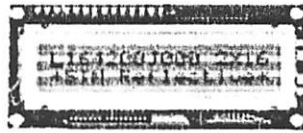
CHARACTER TYPE

• FEATURES :

- Slim, light weight and low power consumption
- High contrast and wide viewing angle
- Built-in controller for easy interfacing
- LCD modules with built-in EL or LED backlight



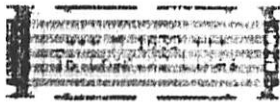
M1641



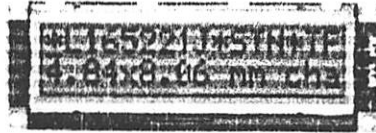
L1642



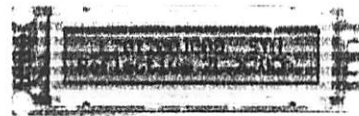
L1614



M1632



L1652



L2012

• SPECIFICATIONS :

Standard products

Products of optional specification

Character Format (character x line)		16 x 1	16 x 2	16 x 2	16 x 2	16 x 4	20 x 2
Model		M1641	M1632	L1642	L1652	L1614	L2012
Reflective		M16410AS	M16320AS	L16420J000S	L165200J200S	L161400J000S	L201200J000S
EL backlight		M16419DWS	M16329DWS	L164221J000S	L165221J200S	L161421J000S	L201221J000S
LED backlight		M16417DYS	M16327DYS	L1642B1J000S	L1652B1J200S	L1614B1J000S	L2012B1J000S
Reflective (wide temp)		M16410CS	M16320CS	L164200L000S	L165200L200S	L161400L000S	L201200L000S
LED backlight (wide temp)		M16417JYS	M16327JYS	L1642B1L000S	L1652B1L200S	L1614B1L000S	L2012B1L000S
Character font		5x7 dots + cursor	5x7 dots + cursor	5x7 dots + cursor	5x7 dots + cursor	5x7 dots + cursor	5x7 dots + cursor
Module size (HxVxT) mm	Reflective	80,0 x 36,0 x 11,3	85,0 x 30,0 x 10,1	80,0 x 36,0 x 11,3	122,0 x 44,0 x 11,3	87,0 x 60,0 x 11,6	116,0 x 37,0 x 11,3
	EL backlight	80,0 x 36,0 x 11,3	85,0 x 30,0 x 10,1	80,0 x 36,0 x 11,3	122,0 x 44,0 x 11,3	87,0 x 60,0 x 11,6	116,0 x 37,0 x 11,3
	LED backlight	80,0 x 36,0 x 15,8	85,0 x 30,0 x 15,8	80,0 x 36,0 x 15,8	122,0 x 44,0 x 15,8	87,0 x 60,0 x 15,8	116,0 x 37,0 x 15,8
Viewing area (HxV) mm		64,5 x 13,8	62,0 x 16,0	64,5 x 13,8	99,0 x 24,0	61,8 x 25,2	83,0 x 18,6
Character size (HxV) mm *1		3,07 x 5,73	2,78 x 4,27	2,95 x 3,80	4,84 x 8,06	2,95 x 4,15	3,20 x 4,85
Dot size (HxV) mm		0,55 x 0,75	0,50 x 0,55	0,50 x 0,55	0,92 x 1,10	0,55 x 0,55	0,60 x 0,60
Power supply voltage (VDD-VSS) V		+5 V	+5 V	+5 V	+5 V	+5 V	+5 V
Current consumption (mA typ)	IDD	1,5	2,0	1,6	2,0	2,7	2,0
	ILC *4	0,2	0,2	0,3	0,4	1,1	0,4
Driving method (duty)		1/16	1/16	1/16	1/16	1/16	1/16
Built-in LSI		KS0066 or equivalent	KS0066 or equivalent MSM5839	KS0066 or equivalent MSM5839	KS0066 or equivalent MSM5839	KS0066 or equivalent KS0063	KS0066 or equivalent KS0063
Operating temperature (°C)	normal temp.	0 to +50	0 to +50	0 to +50	0 to +50	0 to +50	0 to +50
	wide temp. *2	-20 to +70	-20 to +70	-20 to +70	-20 to +70	-20 to +70	-20 to +70
Storage temperature (°C)	normal temp.	-20 to +60	-20 to +60	-20 to +60	-20 to +60	-20 to +60	-20 to +60
	wide temp.	-30 to +80	-30 to +80	-30 to +80	-30 to +80	-30 to +80	-30 to +80
Weight (g. typ.)	Reflective	25	25	25	50	50	40
	EL backlight	30	30	30	55	55	45
	LED backlight	35	40	35	65	65	60
Inverters for EL	Model	5S	5S	5S	5C	5A	5A
	Power supply (V)	+5.0	+5.0	+5.0	+5.0	+5.0	+5.0
	current consumption (mA) *3	10	10	10	35	45	45
LED backlight	Forward current consumption (mA)	100	112	100	240	200	150
	Forward input voltage (V typ.)	+4,1	+4,1	+4,1	+4,1	+4,1	+4,1

*1 : Excluding cursor

*2 : With external temperature compensation

*3 : Including EL backlight

*4 : Based on normal temperature range

H : Horizontal

V : Vertical

T : Thickness (max)

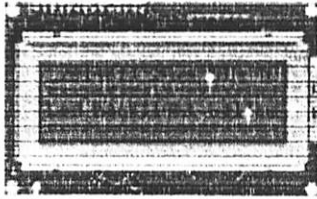
Since our policy is one of continuous improvements we reserve the right to change the specifications for the products in the catalogue without notice.



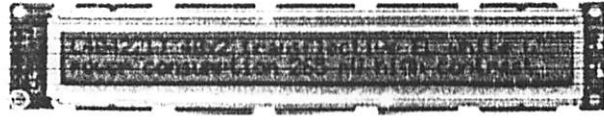
L2022



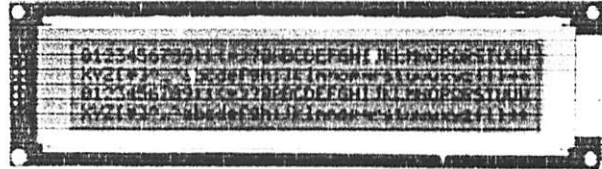
L2432



L2014



L4042



M4024

• SPECIFICATIONS :

□ : Standard products

□ : Products of optional specification

Character Form (character x line)	20 x 2	20 x 4	24 x 2	40 x 2	40 x 4	
Model	L2022	L2014	L2432	L4042	M4024	
Reflective	-	L201400J000S	L243200J000S	L404200J000S	M40240AS	
EL backlight	-	L201421J000S	L243221J000S	L404221J000S	M40249DWS	
LED backlight	-	L2014B1J000S	L2432B1J000S	L4042B1J000S	M40247DYS	
Reflective (wide temp)	L202200P000S	L201400L000S	L243200L000S	L404200L000S	M40240CS	
LED backlight (wide temp)	L2022B1P000S	L2014B1L000S	L2432B1L000S	L4042B1L000S	M40247JYS	
Character font	5x7 dots + cursor	5x7 dots + cursor	5x7 dots + cursor	5x7 dots + cursor	5x7 dots + cursor	
Module size (HxVxT) mm	Reflective	180,0 x 40,0 x 10,5	98,0 x 60,0 x 11,6	118,0 x 36,0 x 11,3	182,0 x 33,5 x 11,3	190,0 x 54,0 x 10,1
	EL backlight	180,0 x 40,0 x 10,5	98,0 x 60,0 x 11,6	118,0 x 36,0 x 11,3	182,0 x 33,5 x 11,3	190,0 x 54,0 x 10,1
	LED backlight	180,0 x 40,0 x 14,8	98,0 x 60,0 x 15,8	118,0 x 36,0 x 15,8	182,0 x 33,5 x 16,3	190,0 x 54,0 x 11,3
Viewing area (HxV) mm	149,0 x 23,0	76,0 x 25,2	94,5 x 17,8	154,4 x 15,8	147,0 x 29,5	
Character size (HxV) mm *1	6,00 x 9,66	2,95 x 4,15	3,20 x 4,85	3,20 x 4,85	2,78 x 4,27	
Dot size (HxV) mm	1,12 x 1,12	0,55 x 0,55	0,60 x 0,65	0,60 x 0,65	0,50 x 0,55	
Power supply voltage (VDD-VSS) V	+5 V	+5 V	+5 V	+5 V	+5 V	
Current consumption (mA, typ)	IDD	4,2	2,9	2,5	3,0	8,0
	ILC *4	2,6	1,2	0,5	1,0	3,0
Driving method (duty)	1/16	1/16	1/16	1/16	1/16	
Built-in LSI	KS0066	KS0066	KS0066	KS0066	KS0066	
	KS0063 or equivalent	MSM5839 or equivalent	KS0063 or equivalent	KS0063 or equivalent	MSM5839 or equivalent	
Operating temperature (°C)	normal temp.	-	0 to +50	0 to +50	0 to +50	
	wide temp. *2	-20 to +70	-20 to +70	-20 to +70	-20 to +70	-20 to +70
Storage temperature (°C)	normal temp.	-	-20 to +60	-20 to +60	-20 to +60	
	wide temp.	-30 to +80	-30 to +80	-30 to +80	-30 to +80	-30 to +80
Weight (g, typ.)	Reflective	80	55	40	70	90
	EL backlight	-	60	45	75	105
	LED backlight	110	70	60	95	140
Inverters for EL	Model	-	5A	5A	5C	5D
	Power supply (V)	+5.0	+5.0	+5.0	+5.0	+5.0
	current consumption (mA) *3	-	45	45	25	80
LED backlight	Forward current consumption (mA)	320	240	150	260	480
	Forward input voltage (V, typ.)	+4,1	+4,1	+4,1	+4,1	+4,1

*1 : Excluding cursor

*2 : With external temperature compensation

*3 : Including EL backlight

*4 : Based on normal temperature range

H : Horizontal

V : Vertical

T : Thickness (max)

Dot Matrix Liquid Crystal Display Modules

GRAPHIC TYPE

• FEATURES :

- Wide viewing angle and high contrast
- Slim, light weight and low power consumption
- Full dot configuration fits any application
- Available in STN and FSTN

• SPECIFICATIONS :

Dot format (HxV, dot)		97 x 32	128 x 32	128 x 64	128 x 64
Model		Y97031	G1213	G1216	G1228
STN type (Gray mode)	Reflective	built-in RAM	-	-	-
	Reflective wide temp.	built-in RAM	G121300N000S	G121600N000S	-
	LED backlight	built-in RAM	-	-	G1228B1J000S
	LED backlight wide temp.	built-in RAM	G1213B1N000S	G1216B1N000S	-
FSTN type (B&W mode)	Transmissive	-	-	-	-
	with CFL backlight	built-in controller	-	-	-
	Transmissive	built-in RAM	-	-	-
Module size (H x V x T) mm		Y97031LF60W	-	-	-
Viewing area (HxV) mm	Reflective (no backlight)	47,5 x 65,4 x 2,1	75,0 x 41,5 x 6,8	75,0 x 52,7 x 6,8	-
	LED backlight	-	75,0 x 41,5 x 8,9	75,0 x 52,7 x 8,9	93,0 x 70,0 x 11,4
	CFL backlight	-	-	-	-
Dot size (H x V) mm		0,35 x 0,48	0,40 x 0,48	0,40 x 0,40	0,44 x 0,44
Dot pitch (H x V) mm		0,39 x 0,52	0,43 x 0,51	0,43 x 0,43	0,48 x 0,48
Power supply voltage (V)	(VDD - VSS)	+5,0	+5,0	+5,0	+5,0
	(VLC - VSS)	-	-8,0	-8,1	-8,2
Current consumption (mA, typ.)	IDD	0,10	2,0	2,0	3,0
	IDD (built-in controller)	-	-	-	-
Driving method (duty)	LC	-	1/8	1/8	2/0
		1/33	1/64	1/64	1/64
Built-in LSI	Driver	SED1530 or equivalent	HD61202 HD61203 or equivalent	HD61202 HD61203 or equivalent	KS0107 KS0108 or equivalent
	Controller	-	-	-	-
Operating temperature range (°C)		-20 to +70	-20 to +70	-20 to +70	0 to +60
Storage temperature range (°C)		-30 to +80	-30 to +80	-30 to +80	-20 to +60
Weight (g, typ.)	Reflective (Transmissive no backlight)	10	23	35	-
	LED backlight	-	35	45	72
	CFL backlight	-	-	-	-
LED backlight	Forward current consumption (mA)	-	40	90	125
	Forward input voltage (V, typ.)	-	3,8	4,1	4,1
Inverter for CFL	Mode	-	-	-	-
	Power supply voltage (V)	-	-	-	-
Current consumption (mA, typ.)		-	-	-	-

*1 : built-in DC/DC converter (single power source)

*2 : Use with external temperature compensation circuit

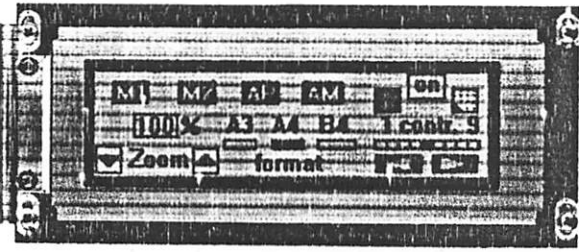
Since our policy is one of continuous improvements we reserve the right to change the specifications of the products in the catalogue without notice.

Dot format (HxV,dot)			240 x 64	240 x 128	320 x 200	320 x 240	640 x 200
Model			G2448	G242C	G321D	G324E	G640D
STN type (Gray mode)	Reflective	built-in RAM	-	-	-	-	-
	Reflective wide temp.	built-in RAM	-	-	-	-	-
	LED backlight	built-in RAM	-	-	-	-	-
	LED backlight wide temp.	built-in RAM	-	-	-	-	-
FBTN type (B&W mode)	Transmissive	-	G2448X5R1A08	G242CX5R1AC8	G321DX5R1A08	G324EX5R1A08	G640DX5R108
	with CFL backlight	built-in controller	G2448CX5R1AC8	G242CX5R1A08	G321DX5R1AC8	G324EX5R1AC8	-
	Transflective	built-in RAM	-	-	-	-	-
Module size (H x V x T) mm	Reflective (no backlight)	-	-	-	-	-	-
	LED backlight	-	-	-	-	-	-
	CFL backlight	191,0 x 79,0 x 15,1	180,0 x 110,0 x 15,1	166,0 x 134,0 x 15,1	166,0 x 134,0 x 15,1	260,0 x 122,0 x 15,7	
Viewing area (HxV) mm			134,0 x 41,0	134,0 x 76,0	126,0 x 110,0	126,0 x 110,0	216,0 x 83,0
Dot size (H x V) mm			0,49 x 0,49	0,47 x 0,47	0,34 x 0,48	0,32 x 0,39	0,30 x 0,39
Dot pitch (H x V) mm			0,53 x 0,53	0,51 x 0,51	0,38 x 0,52	0,38 x 0,43	0,33 x 0,39
Power supply voltage (V)	(VDD - VBS) ¹		+5,0	+5,0	+5,0	+5,0	+5,0
	(VLC - VBS) ²		*1	*1	-24,0	-24,0	-24,0
Current consumption (mA, typ.)	IDD		12	30	6	7,5	11
	IDD (built-in controller)		15	40	23	23	-
	ILC		-	-	6	6,5	9
Driving method (duty)			1/64	1/128	1/200	1/240	1/200
Built-in LSI	Driver		MSM5298	K90103	MSM5298	HD66204	MSM5298
			MSM5299	K90104	MSM5299	HD66205	MSM5299
	Controller		SED1330FB	SED1330FB	SED1330FB	SED1330FB	-
Operating temperature range (°C)			0 to +50	0 to +60	0 to +50	0 to +60	0 to +50
Storage temperature range (°C)			-20 to +80	-20 to +60	-20 to +60	-20 to +60	-20 to +60
Weight (g, typ.)	Reflective (Transflective no backlight)		-	-	-	-	-
	LED backlight		-	-	-	-	-
	CFL backlight		200	260	350	350	420
LED backlight	Forward current consumption (mA)		-	-	-	-	-
	Forward input voltage (V, typ.)		-	-	-	-	-
Inverter for CFL	Mode		4800210	4800210	4800210	4800210	4800120
	Power supply voltage (V)		+5,0	+5,0	+5,0	+5,0	+12,0
	Current consumption (mA, typ.)		250	350	365	365	390

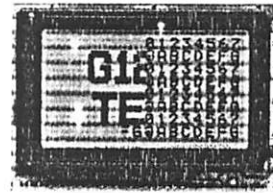
*1 : built-in DC/DC converter (single power source)

*2 : Use with external temperature compensation

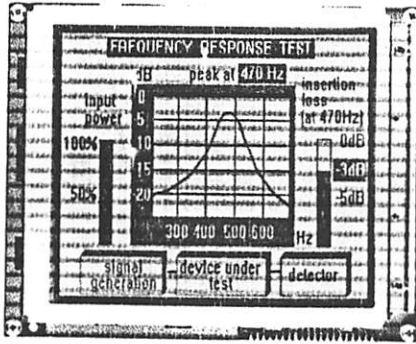
Since our policy is one of continuous improvement, we reserve the right to change the specifications of the products in the catalogue without notice.



G2446



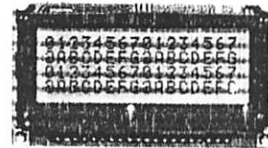
G1226



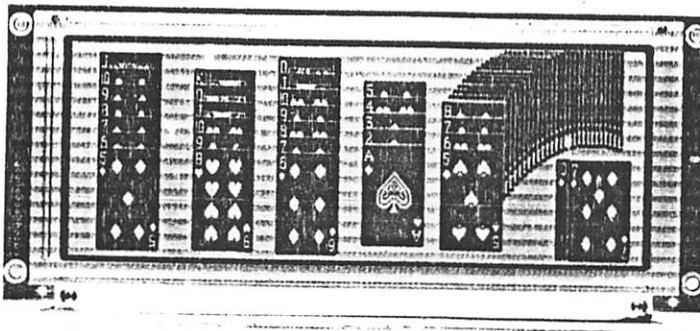
G321D



G1216



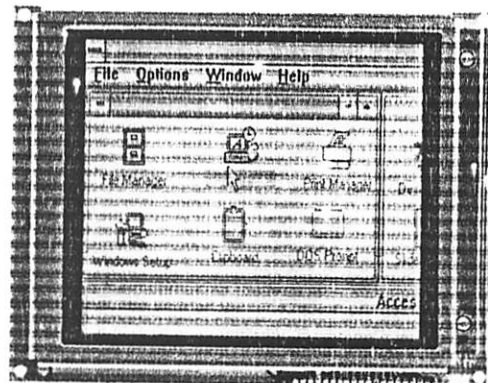
G1213



G649D



G242C



G324E

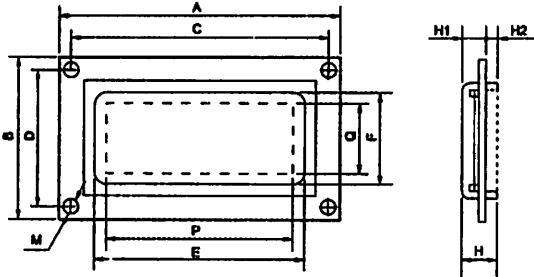
CHECK LIST FOR CUSTOM DESIGNED LCD MODULE

1. Company _____ 2. Application _____ 3. Customer Specified Part No. _____

4. Design

New Modified : Manufacturer _____, Part No. _____, Remarks _____
 Equivalent: Manufacturer _____, Part No. _____, Remarks _____

5. LCM Dimensions



A x B : Module size _____ x _____ mm
 E x F : Viewing area _____ x _____ mm
 P x Q : Active display area _____ x _____ mm
 C : Length between mounting holes _____ mm
 D : Length between mounting holes _____ mm
 M : Diameter of mounting hole _____ mm
 H : Total thickness _____ mm
 H1 : Upper thickness _____ mm
 H2 : Lower thickness _____ mm

6. Display Contents

Character type: _____ character; _____ lines
 Character font _____ x _____ dots + cursor
 Character pitch _____ x _____ mm
 Dot pitch _____ x _____ mm
 Dot size _____ x _____ mm
 Graphics (Full dot) type: _____ x _____ dots
 Dot pitch _____ x _____ mm
 Dot size _____ x _____ mm
 Segment type: _____ digits _____ lines
 Others _____

7. LCD Panel

Viewing angle: 6 o'clock 12 o'clock _____ o'clock
 Type: TN FSTN (Black and white)
 STN (Yellow green Gray Blue)
 Chromaticity coordinates
 (_____ ≤ x ≤ _____, _____ ≤ y ≤ _____)
 Positive type Negative type
 Reflective Transflective Transmissive
 Others _____
 Gray scale: Yes _____ gray scale No
 Preferential specifications:
 Response time t_{on} ms (_____ °C) t_{off} ms (_____ °C)
 Viewing angle _____ deg. (_____ °C) Contrast: _____ (_____ °C)
 Others _____

LCD surface finishing:

Normal Anti-glare _____
 Polarizer color: Normal (neutral gray) Red
 Green Blue _____

8. Driving Method

Multiplexing: 1/ _____ duty, 1/ _____ bias
 Frame frequency: _____ Hz

9. IC

LCD driver: Specified Unspecified
 Segment driver _____ (Manufacturer _____)
 Common driver _____ (Manufacturer _____)
 Controller: Internal External
 Type No. _____ (Manufacturer _____)
 MPU: Internal External
 Type No. _____ (Manufacturer _____)
 RAM: Internal External
 Type No. /Memory size _____ (Kbit) (Manufacturer _____)

10. Power Supply

Single power supply: 5V _____ V
 2 power supplies
 For logic: (V_{cc}-V_{ss}): 5V _____ V
 For LC drive: (V_{Lc}-V_{sa}): _____ V

11. Temperature Compensation Circuit

Internal External Unnecessary
 Compensation range: 0°C to 50°C _____ °C to _____ °C

12. Current Consumption

For logic: typ. _____ mA, max. _____ mA
 For LC drive: typ. _____ mA, max. _____ mA
 Others (_____): typ. _____ mA, max. _____ mA

13. Contrast Adjustment

Internal External Unnecessary
 Method: Temp. compensation circuit Volume _____

14. Temperature Range

Operating temperature range: 0°C to 50°C _____ °C to _____ °C
 Storage temperature range: - 20°C to 60°C _____ °C to _____ °C

15. Input/Output Terminals

Specifying allocation: Yes No
 Specifying position: Yes No

16. Weight

typ. _____ g, max. _____ g

17. Connector

Internal External Unnecessary
 Type No. _____ (Manufacturer _____)

18. Backlight

Internal External Unnecessary
 EL: Green White _____
 LED: Yellow green Amber _____
 CFL: White _____
 Incandescent lamp Others _____
 Backlight type Edge backlight type
 Brightness: _____ cd/m²
 Inverter: Internal External Unnecessary
 Power supply voltage _____ V
 Current consumption (backlight included) _____ mA
 Brightness control: Yes No

19. Others

20. Schedule

Estimate: _____
 Sample: Delivery _____, Quantity: _____ pcs
 Mass production: Target price: _____
 Delivery _____, Total quantity: _____ pcs
 Quantity per month _____ pcs

Liquid Crystal Displays

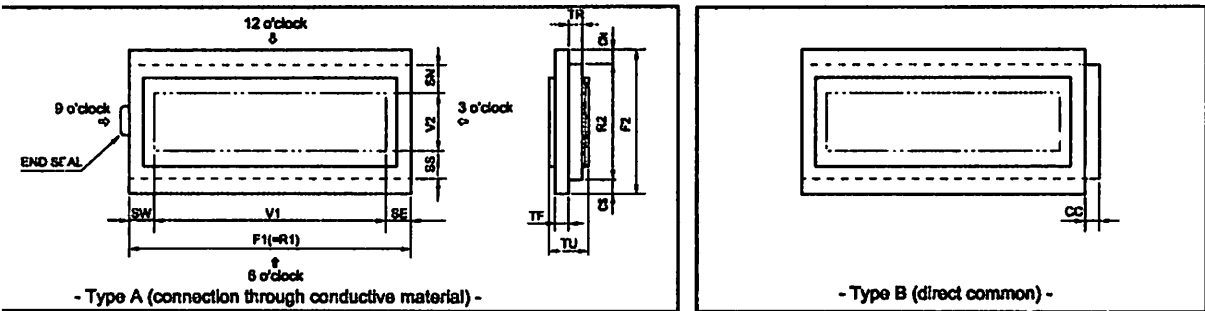
CHECK LIST FOR CUSTOM DESIGNED LCD

Company _____ 2. Application _____ 3. Customer Specified Part No. _____

Design

New Modified: Manufacturer _____, Part No. _____, Remarks _____
 Equivalent: Manufacturer _____, Part No. _____, Remarks _____

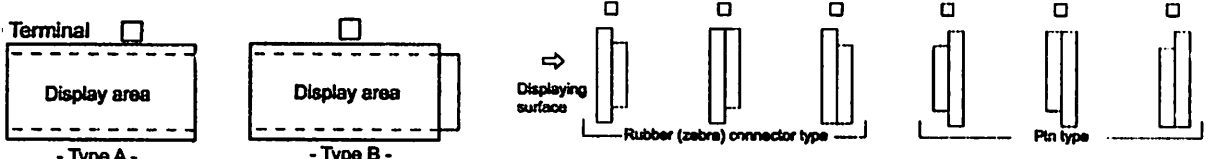
Panel Dimensions



V1: Horizontal length of upper glass _____ mm
 V2: Vertical length of upper glass _____ mm
 Horizontal length of lower glass the same as F1
 Vertical length of lower glass _____ mm
 F2 is generally longer than F1 when terminals are with pin.
 TR***: Thickness of glass _____ mm
 *Standard type: 1.1 mm or 0.7 mm
 Thickness of LCD _____ mm

V1: Horizontal length of viewing area _____ mm
 V2: Vertical length of viewing area _____ mm
 CN**: Terminal length _____ mm
 CS**: Terminal length _____ mm
 **CN or CS=0 in case of one side terminal type.
 CC: Terminal length _____ mm
 SE, SW, SN, SS: Seal width
 (According to design or manufacturing condition:
 about 2.0 mm to 4.0 mm)

Panel Form



Terminal
 Display area
 - Type A -
 - Type B -
 Chamfering Yes No
 Drilling Yes No

Display Mode
 Viewing angle: 6 o'clock 12 o'clock _____ o'clock
 Type: TN FSTN (Black and white)
 STN: (Yellow green Gray Blue)
 Chromaticity coordinates ($\bar{x} \leq x \leq \bar{y}$, $\bar{y} \leq y \leq \bar{z}$)
 Positive type Negative type
 Reflective Transflective Transmissive
 Referential specifications:
 Response time t_{on} ms (____ °C) t_{off} ms (____ °C)
 Viewing angle deg. (____ °C) Contrast (____ °C)
 Others _____

Polarizer
 Surface finishing: Normal Anti-glare _____
 Color: Normal (neutral gray) Red Green
 Blue _____
 Front polarizer: Attached type Separate type
 Rear polarizer: Attached type Separate type

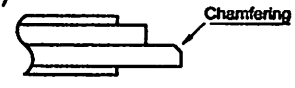
Driving Method
 Static Multiplexing: (1/____ duty, 1/____ bias)
 Operating voltage (V_{op}): _____ V
 Frame frequency: _____ Hz
 Driving IC: _____ (Manufacturer _____)
 Current consumption: _____ μA

10. Temperature Range
 Operating temperature range
 With temperature compensation circuit (or volume)
 (0°C to 50°C _____ °C to _____ °C)
 Without temperature compensation circuit
 (0°C to 50°C _____ °C to _____ °C)
 Storage temperature range
 (- 20°C to 60°C _____ °C to _____ °C)

11. Terminal Connecting Method
 Rubber connector (Zebra rubber)
 Pin: DIL SIL _____
 Pitch (2.54 _____ mm) Length (____ mm)
 Heat seal: Equipped Unnecessary

12. Others
 Print (Characters, lines, masks etc.): Yes No
 Protective film:
 Yes (Color: Red Translucent Transparent) No
 Chamfering (for heat-seal connector):
 Yes (Position: _____)
 (Quantity: _____)
 No

13. Schedule
 Estimate: _____
 Sample: Delivery _____, Quantity: _____ pcs
 Mass production: Target price: _____
 Delivery _____, Total quantity: _____ pcs
 Quantity per month: _____ pcs

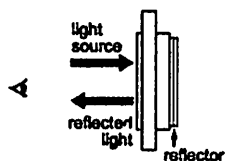


Liquid Crystal Display Modules

REFLECTIVE/TRANSFLECTIVE/TRANSMISSIVE LCD

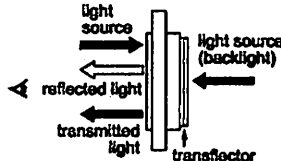
1 Reflective LCD

Reflector bonded to the rear polarizer reflects the incoming ambient light. Low power consumption because no backlight is required.



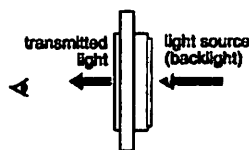
2 Transflective LCD

Transflector bonded to the rear polarizer reflects light from the front as well as enabling lights to pass through the back. Used with backlight off in bright light and with it on in low light to reduce power consumption.



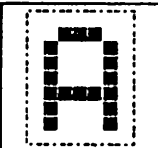
3 Transmissive LCD

Without reflector or transflector bonded to the rear polarizer. Backlight required. Most common is transmissive negative image.



POSITIVE/NEGATIVE MODE

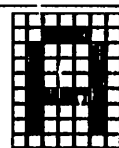
Positive type



Negative type



Negative type (inverse image) (when data is inverted)



TN TYPE/STN TYPE/FSTN TYPE

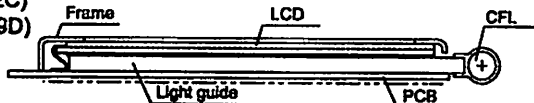
TN	(Background/dot color) Gray/Black	TN (Twisted Nematic) type is most conventional and economical. It is used for static drive LCD and low-duty drive LCD (watch, calculator, etc.)
STN	Yellowgreen/Dark blue Gray/Dark blue White/Blue	STN (Super Twisted Nematic) type has a higher twist angle, and thus provides clear visibility and wider viewing angle. This is suitable especially for high-duty drive LCD.
FSTN	White/Black	FSTN (Film Super Twisted Nematic) type utilizes RCF (Retardation Control Film) to remove the coloring of STN LCD. Thus FSTN type provides easy-to-read black-and-white display.

STRUCTURE AND FEATURE OF LCD MODULE WITH BACKLIGHT

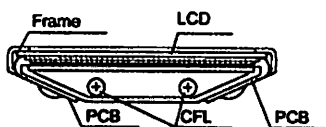
CFL (Cold Cathode Fluorescent Lamp) backlight

Features: high brightness, long service life, inverter required

- Edge backlight type (G2446, G242C) (G321D, G649D)

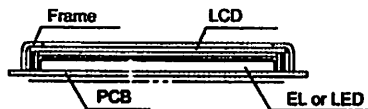


- Backlight type



EL (Electroluminescent Lamp) backlight LED (Light Emitting Diode) backlight

Features: EL: thin, inverter required
LED: long service life, low voltage driving, no inverter required

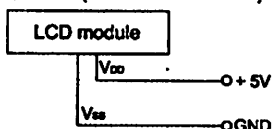
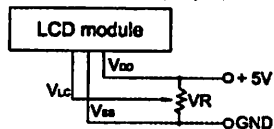


POWER SUPPLY

- Character modules (single power supply)

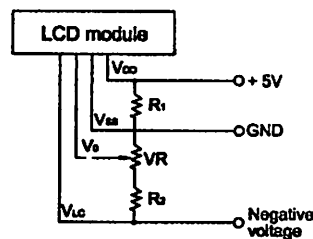
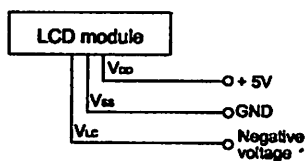
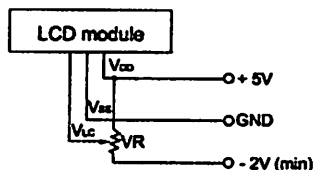
- G2446, G242C (Built-in DC-DC conv.)

- G321D, G324E and G649D



- Character Modules (Dual power supply)

- Y1206 and G1226



Note 1: Contrast can be adjusted by VR.
Note 2: For module with backlight, power supply for backlight is necessary.

• Negative voltage should be variable for contrast adjustment.

Precautions

Safety Instructions

- If the LCD panel is damaged, be careful not to get the liquid crystal in your mouth and not to be injured by crushed glasses.
- If you should swallow the liquid crystal, first, wash your mouth thoroughly with water, then, drink a lot of water and induce vomiting, and then, consult a physician.
- If the liquid crystal should get in your eye, flush your eye with running water for at least fifteen minutes.
- If the liquid crystal touches your skin or clothes, remove it and wash the affected part of your skin or clothes with soap and running water.
- EL or CFL backlight is driven by a high voltage with an inverter. Do not touch the connection part or the wiring pattern of the inverter.
- Do not use inverters without a load or in the short-circuit mode.
- Use the LCD module within the rated voltage to prevent overheating and/or damage. Also, take steps to ensure that the connector does not come off.

Handling Precautions

- Since the LCD panel has glass substrate, avoid applying mechanical shock or pressure on the module. Do not drop, bend, twist or press the module.
- Do not soil or damage LCD panel terminals.
- Since the polarizer is made of easily-scratched material, be careful not to touch or place objects on the display surface.
- Keep the display surface clean. Do not touch it with your skin.
- CMOS LSI is used in the LCD module. Be careful of static electricity.
- Do not disassemble the module or remove the liquid crystal panel or the panel frame.
- Do not damage the film surface of the EL lamp; otherwise the lamp will be damaged by humidity.
- To set an EL lamp in an LCD module, push the EL lamp with its emitting side up, without pushing the rubber connectors too hard. If you damage them, the LCD module may not work properly.

Mounting and Designing

- To protect the polarizer and the LCD panel, cover the display surface with a transparent plate (e.g., acrylic or glass) with a small gap between the transparent plate and the display surface.
- Keep the module dry. Avoid condensation to prevent the transparent electrodes from being damaged.
- Drive LCD panel with AC waveform in which DC element is not included to prevent deterioration in the LCD panel.
- Contrast of LCD varies depending on the ambient temperature. To offer the optimum contrast, LC drive voltage should be adjusted. LCD driven in a high duty ratio must be provided with drive voltage adjustment method.
- Mount a LCD module with the specified mounting part/holes.

- Design the equipment so that input signal is not applied to the LCD module while power supply voltage is not applied to it.
- Do not locate the CFL tube and the lamp lead wire close to a metal plate or a plated part inside the equipment. Otherwise stray capacity causes a drop in voltage, decreasing the brightness and the ability to start-up.

Cleaning

- Do not wipe the polarizer with a dry cloth, as it may scratch the surface.
- Wipe the LCD panel gently with a soft cloth soaked with a petroleum benzene.
- Do not use ketonic solvents (ketone and acetone) or aromatic solvents (toluene and xylene), as they may damage the polarizer.

Storing

- Store the LCD panel in a dark place, where the temperature is $25^{\circ}\text{C}\pm 10^{\circ}\text{C}$ and the relative humidity below 65%. If possible, store the LCD panel in the packaging situation when it was delivered.
- Do not store the module near organic solvents or corrosive gases.
- Keep the module (including accessories) safe from vibration, shock and pressure.
- Use an LCD module with built-in EL backlight within six months of delivery.
- EL backlight is easily affected by environmental conditions such as temperature and humidity; the quality may deteriorate if stored for an extended period of time. Contact Seiko Instruments GmbH for details.
- Some parts of the backlight and the inverter generate heat. Take care so that the heat does not affect the liquid crystal or any other parts.
- Dust particles attached to the surface of the LCD or the surface of the backlight degrade the display quality. Be careful to keep dust out in designing the structure as well as in handling the module.
- Black or white air-bubbles may be produced if the LCD panel is stored for long time in the lower temperature or mechanical shocks are applied onto the LCD panel.

On This Brochure

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MAX232, MAX232I EIA-232 DRIVER/RECEIVER

47H - FEBRUARY 1989 - REVISED FEBRUARY 2002

Absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Input supply voltage range, V_{CC} (see Note 1)	-0.3 V to 6 V
Positive output supply voltage range, V_{S+}	$V_{CC} - 0.3$ V to 15 V
Negative output supply voltage range, V_{S-}	-0.3 V to -15 V
Input voltage range, V_i : Driver	-0.3 V to $V_{CC} + 0.3$ V
Receiver	± 30 V
Output voltage range, V_o : T1OUT, T2OUT	$V_{S-} - 0.3$ V to $V_{S+} + 0.3$ V
R1OUT, R2OUT	-0.3 V to $V_{CC} + 0.3$ V
Short-circuit duration: T1OUT, T2OUT	Unlimited
Package thermal impedance, θ_{JA} (see Note 2): D package	73°C/W
DW package	57°C/W
N package	67°C/W
NS package	64°C/W
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds	260°C
Storage temperature range, T_{stg}	-65°C to 150°C

Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and normal operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not recommended. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- 1: All voltage values are with respect to network ground terminal.
- 2: The package thermal impedance is calculated in accordance with JESD 51-7.

Recommended operating conditions

		MIN	NOM	MAX	UNIT
Supply voltage		4.5	5	5.5	V
High-level input voltage (T1IN, T2IN)		2			V
Low-level input voltage (T1IN, T2IN)				0.8	V
R1IN, R2IN	Receiver input voltage			± 30	V
Operating free-air temperature	MAX232	0		70	°C
	MAX232I	-40		85	



POST OFFICE BOX 655303 • DALLAS, TEXAS 75265

MAX232, MAX232I DUAL EIA-232 DRIVER/RECEIVER

SLLS047H – FEBRUARY 1989 – REVISED FEBRUARY 2002

Electrical characteristics over recommended ranges of supply voltage and operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP†	MAX	UNIT
VOH	High-level output voltage	T1OUT, T2OUT	RL = 3 kΩ to GND	5	7		V
		R1OUT, R2OUT	I _{OH} = -1 mA	3.5			
VOL	Low-level output voltage‡	T1OUT, T2OUT	RL = 3 kΩ to GND		-7	-5	V
		R1OUT, R2OUT	I _{OL} = 3.2 mA			0.4	
VIT+	Receiver positive-going input threshold voltage	R1IN, R2IN	V _{CC} = 5 V, TA = 25°C		1.7	2.4	V
VIT-	Receiver negative-going input threshold voltage	R1IN, R2IN	V _{CC} = 5 V, TA = 25°C	0.8	1.2		V
V _{hys}	Input hysteresis voltage	R1IN, R2IN	V _{CC} = 5 V	0.2	0.5	1	V
r _i	Receiver input resistance	R1IN, R2IN	V _{CC} = 5, TA = 25°C	3	5	7	kΩ
r _o	Output resistance	T1OUT, T2OUT	V _{S+} = V _{S-} = 0, V _O = ±2 V	300			Ω
I _{OSS}	Short-circuit output current	T1OUT, T2OUT	V _{CC} = 5.5 V, V _O = 0		±10		mA
I _{IS}	Short-circuit input current	T1IN, T2IN	V _I = 0			200	μA
I _{CC}	Supply current		V _{CC} = 5.5 V, TA = 25°C, All outputs open,		8	10	mA

All typical values are at V_{CC} = 5 V, T_A = 25°C.

The algebraic convention, in which the least positive (most negative) value is designated minimum, is used in this data sheet for logic voltage levels only.

Not more than one output should be shorted at a time.

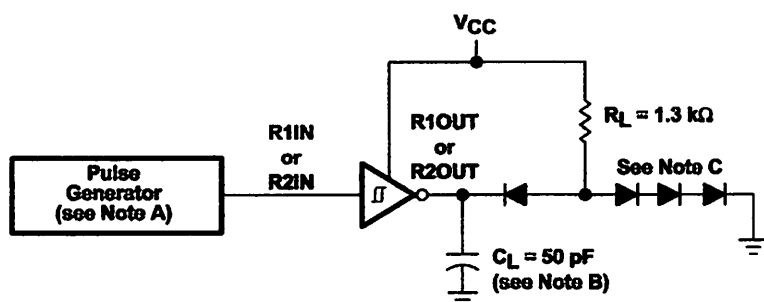
Switching characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t _{PLH(R)}	Receiver propagation delay time, low- to high-level output	See Figure 1		500		ns
t _{PHL(R)}	Receiver propagation delay time, high- to low-level output	See Figure 1		500		ns
SR	Driver slew rate	RL = 3 kΩ to 7 kΩ, See Figure 2			30	V/μs
SR(tr)	Driver transition region slew rate	See Figure 3		3		V/μs

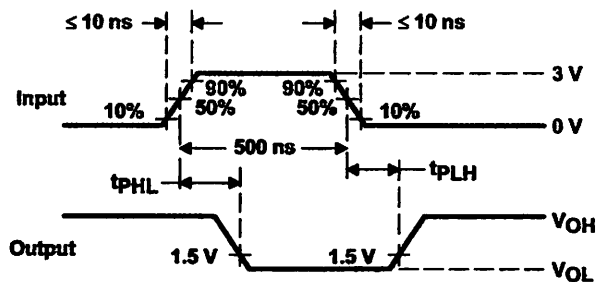


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PARAMETER MEASUREMENT INFORMATION



TEST CIRCUIT

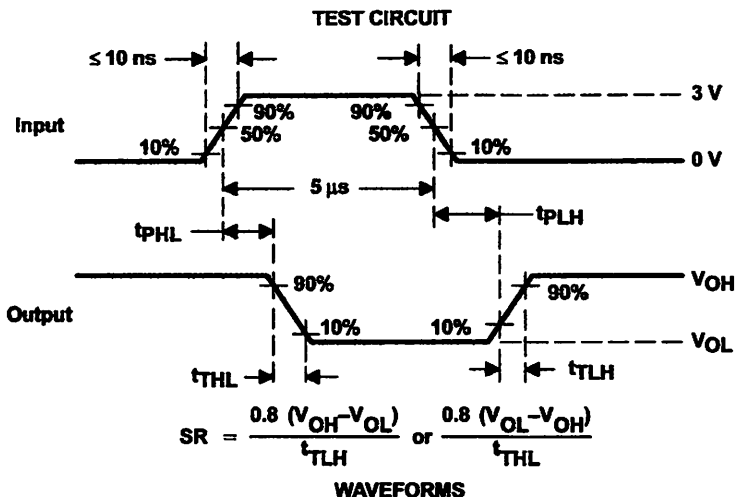
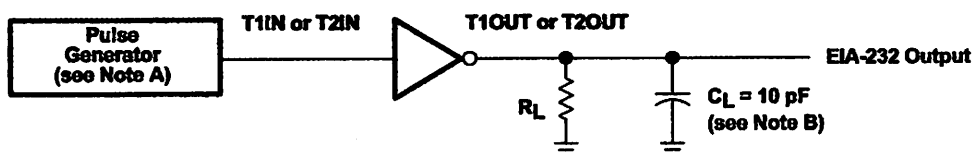


WAVEFORMS

- NOTES: A. The pulse generator has the following characteristics: $Z_O = 50\ \Omega$, duty cycle $\le 50\%$.
B. C_L includes probe and jig capacitance.
C. All diodes are 1N3064 or equivalent.

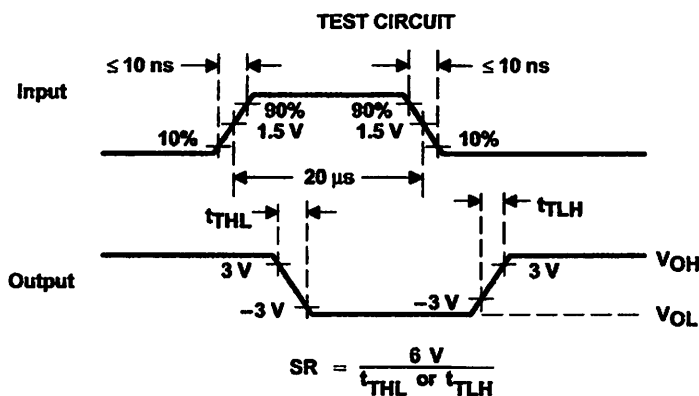
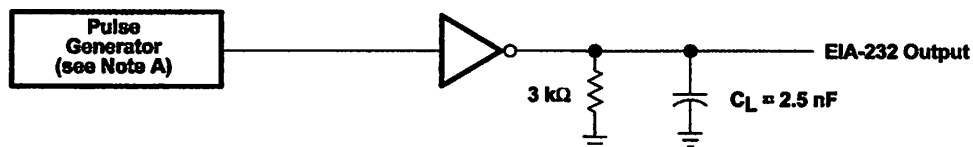
Figure 1. Receiver Test Circuit and Waveforms for t_{PHL} and t_{PLH} Measurements

PARAMETER MEASUREMENT INFORMATION



NOTES: A. The pulse generator has the following characteristics: $Z_0 = 50 \Omega$, duty cycle $\leq 50\%$.
B. C_L includes probe and jig capacitance.

Figure 2. Driver Test Circuit and Waveforms for t_{PHL} and t_{PLH} Measurements (5- μ s input)



NOTE A: The pulse generator has the following characteristics: $Z_0 = 50 \Omega$, duty cycle $\leq 50\%$.

Figure 3. Test Circuit and Waveforms for t_{THL} and t_{TLH} Measurements (20- μ s input)

K232, MAX232 AL EIA-232 DRIVER/RECEIVER

47H - FEBRUARY 1989 - REVISED FEBRUARY 2002

APPLICATION INFORMATION

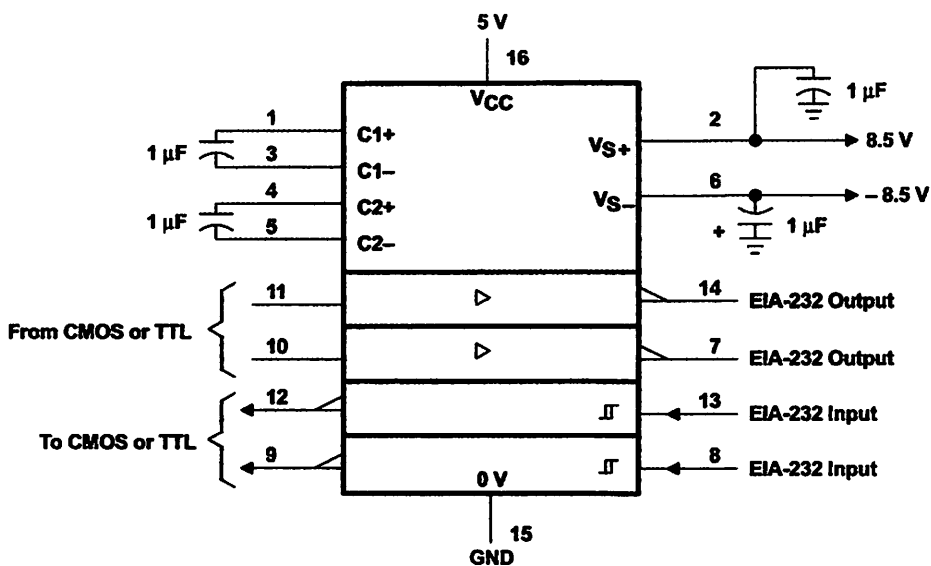


Figure 4. Typical Operating Circuit



**TEXAS
INSTRUMENTS**

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