PERENCANAAN DAN PEMBUATAN SISTEM PENERIMA TELEPON DAN PEMANGGIL OTOMATIS PADA RUMAH KOST MENGGUNAKAN MIKROKONTROLLER R8C/13 DAN AT 89S51

SKRIPSI

Disusun Oleh :

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KONSENTRASI TEKNIK ELEKTRONIKA
JURUSAN TEKNIK ELEKTRO S-1
FAKULTAS TEKNOLOGI INDUSTRI
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LEMBAR PERSETUJUAN

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SKRIPSI

Disusun Dan Diajukan Sebagai Salah Satu Syarat Untuk Memperoleh Gelar Sarjana Teknik Elektronika Strata Satu (S-1)

Disusun oleh:

HADI CAHYADI
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MARET 2007

HADI CAHYADI, 2007. Judul "Pererencanaan dan Pembuatan Sistem Penerima Telepon dan Pemanggil Otomatis pada Rumah Kost Menggunakan Mikrokontroller R8C/13 dan AT89S51", Skripsi Jurusan Teknik Elektro Strata 1, Program Studi Teknik Elektronika, Fakultas Teknologi Industri, Institut Teknologi Nasional Malang. Dosen Pembimbing Ir. F. Yudi Limpraptono, MT dan Ir. Mimien Mustikawati.

ABSTRAKSI

Kata kunci : Telepon, DTMF, ISD, Mikrokontroller

Pada rumah kost dengan banyak kamar dan mempunyai sebuah pesawat telepon untuk menghubungi penghuni rumah kost tersebut, akan menimbulkan masalah, yaitu penghuni disibukkan dengan menerima telepon yang bukan untuk dirinya dan memanggilkan orang yang ingin dihubungi oleh si penelpon. Dengan adanya IC DTMF receiver yang dapat mendeteksi tombol yang ditekan pada pesawat telepon, IC speech processor yang dapat mengubah sinyal suara menjadi data digital dan sebaliknya, maka memungkinkan pembuatan suatu sistem penerima telepon dan pemanggil otomatis pada rumah kost. Pada saat ada panggilan masuk, sistem ini akan menyampaikan menu tentang orang-orang yang menghuni rumah kost kepada si penelpon dengan suara, dan menunggu input penekanan tombol telepon dari si penelpon, lalu input tersebut diproses dan dilakukan pemanggilan nama orang yang ingin dihubungi sesuai dengan angka yang ditekan melalui speaker atau pengeras suara. Pada proses pemanggilan jika tidak ada yang menjawab panggilan tersebut, maka sistem akan memberitahukan kepada si penelpon bahwa tidak ada jawaban dari orang yang dituju atau orang yang dituju sedang tidak di tempat. Sistem ini hanya dapat digunakan pada sistem telepon tone, sistem ini bisa diubah data suaranya seandainya ada penghuni kost yang baru masuk atau keluar.

KATA PENGANTAR

Alhamdulillah, dengan memanjatkan puji syukur kehadirat Allah SWT, yang telah memberikan rahmat, hidayah serta segala karunia-Nya, akhirnya penyusun dapat menyelesaikan skripsi ini yang berjudul "Perencanaan Dan Pembuatan Sistem Penerima Telepon dan Pemanggil Otomatis Pada Rumah Kost Menggunakan Mikrokontroller R8C/13 Dan AT89S51". Laporan skripsi ini merupakan salah satu persyaratan kelulusan Srata 1 Jurusan Teknik Elektro Program Studi Elektronika, Institut Teknologi Nasional Malang.

Keberhasilan penyusunan laporan skripsi ini tidak lepas dari dukungan dan bantuan berbagai pihak. Untuk itu penyusun menyampaikan terima kasih kepada :

1. Allah SWT, yang telah memberikan segala kemudahan sehingga laporan skripsi ini dapat terselesaikan dengan baik.
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Dengan segala itikad, kemampuan dan saran yang ada, laporan skripsi ini dapat terselesaikan dengan sebaik-baiknya. Namun karena keterbatasan waktu dan faktor lain yang dihadapi sehingga menyebabkan laporan skripsi ini tidak lepas dari banyaknya kekurangan. Karena itu sejumlah koreksi dan masukan konstruktif diperlukan guna kesempurnaan laporan skripsi ini. Semoga laporan skripsi dari pemikiran sederhana ini akan menjadi cikal bakal dari karya yang lebih inovatif dan dapat bermanfaat untuk semua orang.

Malang, Maret 2007

Penyusun

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INSTITUT TEKNOLOGI NASIONAL
ITN
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BAB I

PENDAHULUAN

1.1. Latar Belakang

Seperti kita ketahui, kebanyakan fasilitas telepon pada rumah kost kebanyakan cukup minim atau sederhana. Hal ini disebabkan karena murahnya biaya kost perbulan atau pertahun pada rumah kost tersebut sehingga fasilitas telepon pada rumah kost tersebut juga cukup minim, yaitu sebuah pesawat telepon yang diletakan pada tempat umum yang dapat diakses oleh penghuni kost, dan telepon ini hanya bisa menerima telepon masuk saja, dan untuk melakukan hubungan telepon keluar biasanya penghuni kost harus memasukan koin. Dengan fasilitas yang minim tersebut akan menimbulkan masalah, dimana penghuni kost tersebut akan disibukan dengan menerima telepon yang bukan untuknya dan memanggilkan penghuni lain yang ingin dihubungi oleh penelpon.

Dengan berkembangnya teknologi, maka untuk mengatasi masalah seperti diatas tidaklah sulit. PABX (Privat Automatic Branch Exchanger) merupakan salah satu sistem yang dapat mengatasi masalah diatas, tetapi sistem ini relatif mahal Karena untuk tiap ekstensi diperlukan sebuah telepon. Sehingga sistem tersebut tidak ekonomis bila disediakan sebagai fasilitas telepon oleh pemilik rumah kost. Dengan adanya IC DTMF *Receiver* yang dapat mengubah frekuensi tone menjadi data digital dan IC ISD yang dapat melakukan konversi data suara menjadi data digital dan sebaliknya, maka hal ini merupakan salah satu alternatif yang memungkinkan untuk membuat suatu sitem sederhana yang dapat mengatasi masalah di atas.

1.2. Tujuan

Adapun tujuan dari penulisan skripsi ini adalah merencanakan dan membuat alat penerima telepon dan pemanggil otomatis yang ditujukan untuk rumah kost sehingga penghuni kost tidak disibukkan oleh panggilan telepon yang bukan untuk dirinya.

1.3. Rumusan Masalah

Mengacu pada permasalahan yang diuraikan dalam latar belakang, maka rumusan masalah dapat ditekankan pada:

1. Bagaimana merancang dan membuat sistem penerima telepon dan pemanggil otomatis pada rumah kost.
2. Bagaimana merancang dan membuat program mikrokontroller agar dapat menjalankan sistem
3. Bagaimana membuat rangkaian pendeteksi nomor yang ditekan oleh penelpon serta pendeteksi off hook dan on hook pada pesawat telepon lokal.
4. Bagaimana membuat rangkaian penyampai pesan dan pengisi suara pada ISD.

1.4. Batasan Masalah

Mengacu pada permasalahan yang ada, perancangan sebuah sistem penerima telepon dan pemanggil otomatis pada rumah kost ini dibatasi pada:

1. Membuat rangkaian pendeteksi ring dan pengaktif sistem.
2. Membuat rangkaian mikrokontroller R8C/13 dan AT89S51.

3. Membuat rangkaian pendeteksi nomor telepon yang ditekan oleh penelpon.
4. Membuat rangkaian penyampai pesan dan pemanggil otomatis.
5. Tidak membahas teori-teori frekuensi sambungan telepon.
6. Penghuni hanya dibatasi sampai 10 orang.

1.5. Metodologi Penulisan

Metodologi penulisan yang digunakan dalam penyusunan skripsi ini adalah:

1. Studi Literatur

   Yaitu mempelajari teori-teori dari literatur buku atau informasi yang berhubungan dengan pembuatan alat ini.

2. Perencanaan Serta Pembuatan alat

   Yaitu merancang sistem pengendali dan pendeteksi, baik hardware yang meliputi rangkaian elektronik serta software program sesuai dengan perencanaan.

3. Pengujian Alat dan Analisa

   Setelah hardware dan software yang menjadi sebuah sistem selesai dibuat, maka diadakan pengujian untuk mengetahui kinerja alat dan untuk mendapatkan keakuratan sistem yang telah dirancang.

4. Penyusunan Laporan

   Penyusunan laporan dibuat dengan mengikuti sistematika pembahasan yang telah ditetapkan.

1.6. Sistematika Penulisan

1. BAB I, PENDAHULUAN, menguraikan latar belakang, permasalahan, tujuan penulisan, dan sistematika penulisan.
2. BAB II, TINJAUAN PUSTAKA, pada bab ini dibahas tentang teori-teori yang mendukung dalam perencanaan dan pembuatan alat
3. BAB III, PERENCANAAN PERANGKAT KERAS, membahas perencanaan teknis dan proses pembuatan alat.
4. BAB IV, PENGUJIAN DAN ANALISIS, berisikan tentang analisa atau cara kerja dari alat yang dibuat
5. BAB V, PENUTUP, berisikan tentang kesimpulan dan saran-saran dari perencanaan dan pembuatan alat

BAB II

LANDASAN TEORI

2.1. Sistem Telepon

Telepon dalam bahasa asing berasal dari bahasa yunani yaitu Tele (jauh) dan Phone (suara). Jadi pengertian umum telepon meliputi konversi dari sinyal suara menjadi listrik dengan frekuensi audio yang kemudian dapat dipancarkan melalui suatu sistem transmisi listrik dan pada akhirnya dikonversikan kambali menjadi sinyal suara pada ujung penerima seperti suara aslinya.

Sistem telepon adalah sistem komunikasi percakapan dua arah (*full duplex*) dan merupakan komunikasi data secara nyata diantara beberapa tempat terpisah (Scheweber, 1996:468). Hubungan internal diantara telepon dikendalikan oleh sentral telepon lokal yang menghubungkan satu telepon dengan telepon lain dan juga menghubungkan ke sentral lain melalui saluran utamanya. Pengontrolan *switching* ini menggunakan sirkuit fungsi logika digital tertentu atau menggunakan komputer sistem pengontrol switching elektronik. Sistem telepon mempunyai sifat sederhana dan merupakan sistem komunikasi yang lebih kompleks dalam penggunaanya secara umum. Sederhana, karena mudah dalam penggunaanya dimana hubungan antar pelanggan dan pusat *switching* hanya melalui dua kabel pada *loop* lokal. Bersifat kompleks, karena sistem ini dapat mentransmisikan suara dan data sejauh ribuan kilometer.

Komponen-komponen utama dalam sistem telepon untuk melakukan proses komunikasi ini antara lain adalah:

1. Penerima (*receiver*)

2. Pengirim (*transmitter*)
3. Saklar *hook* (*switching hook*)
4. Pemilih nomor (*dialing number*)
5. Bel (*Ringer*)
6. Sentral

Masing-masing komponen dan proses *switching* pada sentral telepon akan dibahas secara singkat dan sederhana.

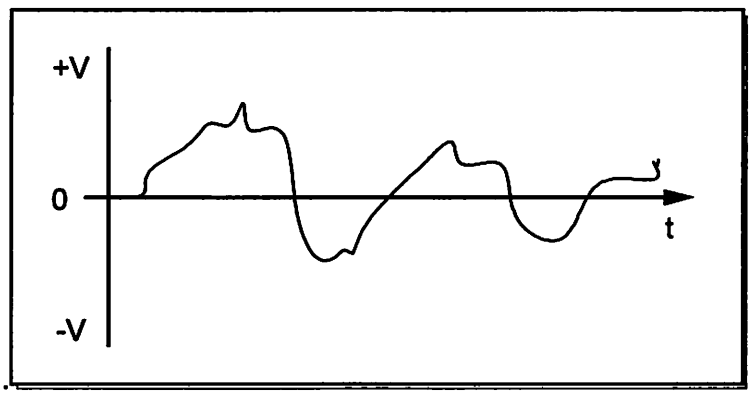
2.1.1. Penerima

Penerima (*receiver*) terdapat pada *handset* pesawat telepon yang bekerja mengubah sinyal listrik yang datang menjadi gelombang suara sehingga dapat didengar oleh penerima. Aliran sinyal listrik yang datang pada *receiver* menyebabkan arus pada lilitan (*coil*) *speaker* saling mempengaruhi dengan magnet sehingga menyebabkan lilitan itu bergerak. *Coil* bergerak menuju difragma yang biasa disebut dengan *speaker cone* (corong/kerucut *speaker*) dengan menimbulkan getaran yang selanjutnya berubah menjadi gelombang suara.

2.1.2. Pengirim

Pada *hanset* pesawat telepon juga terdapat pengirim (*transmitter*) yang berfungsi untuk mengubah gelombang suara menjadi sinyal listrik sehingga dapat ditransmisikan pada saluran telepon. Suara manusia menghasilkan gelombang bunyi atau getaran yang menggerakan udara disekitar diafragma yang terdapat pada mikropfon. Getaran udara ini menimbulkan tekanan pada bubuk karbon sehingga mengubah resistansi yang menyebabkan perubahan arus listrik pada hubungan listrik yang telah diberi tegangan. Selanjutnya gelombang suara yang telah diubah kedalam

sinyal listrik disebut sebagai sinyal analog yang diwakili dalam bentuk gelombang tegangan listrik sebagai fungsi waktu



Gambar 2.1.Gelombang suara yang diwakili tegangan sebagai fungsi waktu

Sumber : *Business Tele-Communication*, 1991: 5-137

2.1.3. Saklar *Hook*

Saklar *hook* terdapat pada pesawat telepon berupa sebuah tombol yang ditekan oleh *handset*. Pada saat *handset* diangkat maka arus listrik mengalir menuju sentral telepon. Arus listrik ini memberitahukan sentral bahwa sambungan telah dibuat, kondisi ini dinamakan *off hook*. Selanjutnya sentral akan menanggapi dengan nada pilih (*dial tone*) yang memberitahukan bahwa sentral telah siap menerima panggilan.

Penempatan kembali *handset* pada pesawat telepon akan menekan saklar *hook* sehingga menyebabkan putusnya hubungan antara sentral dan pelanggan telepon, kondisi ini dinamakan *on hook*.

2.1.4. Pemilihan Nomor

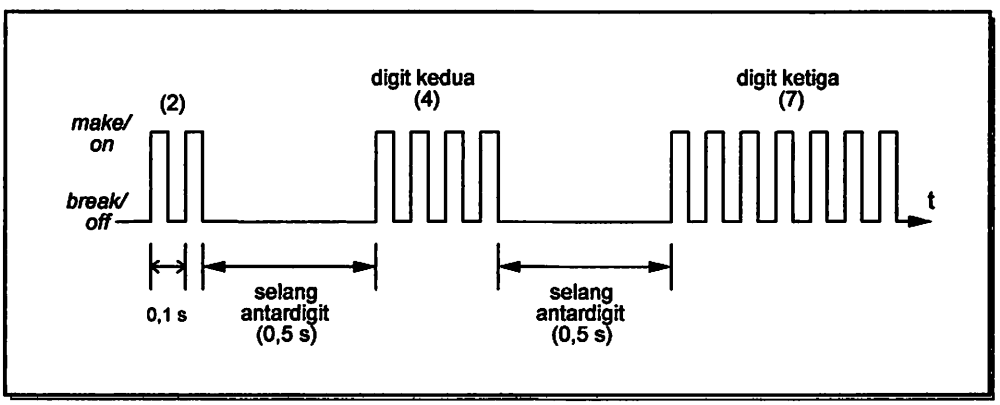
Pemilihan nomor (*dialing*) adalah proses untuk menghubungi pelangganlain melalui sentral telepon dan selanjutnya sentral melakukan proses *switching* untuk

membentuk *loop* tertutup antara pemanggil, sentral, dan yang dipanggil. Terdapat dua macam proses *dialing* yaitu *dialing* pulsa (*pulse dialing*) dan *dialing* nada (*tone dialing*) (Schweber, 1996:754).

2.1.4.1. *Dialing* Pulsa (*pulse dialing*)

Dialing dengan pulsa biasanya dilakukan oleh telepon jenis *rotary* yaitu dengan memutar piringan pemilih nomor maka akan menghasilkan pulsa pada saluran telepon.

Pulsa ini akan membuka rangkaian saat proses *dialing* disambungkan dan menutup rangkaian saat proses *dialing* diputus. Sejumlah pulsa ditentukan oleh seberapa banyak *dial* dilakukan. Pulsa- pulsa yang dihasilkan memiliki kecepatan 10 pulsa per detik. Contoh sinyal pulsa pada saat proses *dial* seperti dalam Gambar 2.2.



Gambar 2.2.Sinyal pada loop dari proses *dial* pulsa dan selang waktu antara digit

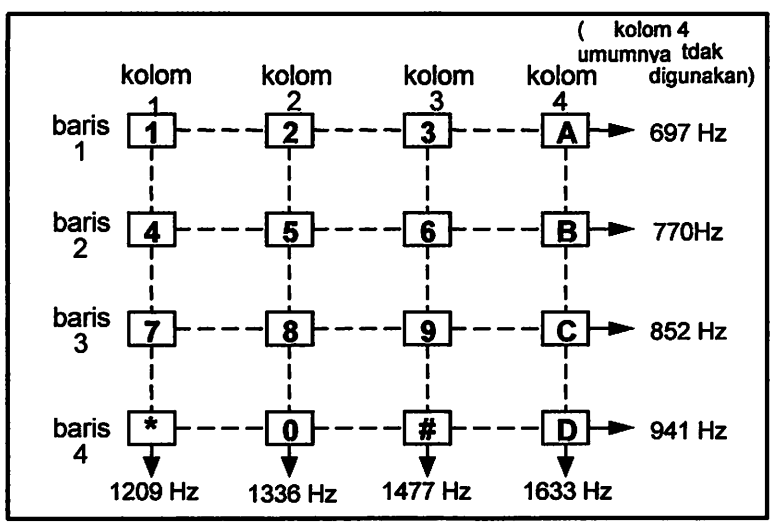
Sumber : *Electronic Communication System*, 1996: 16-475

2.1.4.2. *Dialing* Nada (*tone dialing*)

Teknik pensinyalan lain untuk mewakili pemilihan nomor untuk menghubungi sentral adalah dengan menggunakan *Dual-Tone-Multiple- Frequency.* Pensinyalan dilakukan dengan cara mengirimkan nada ke saluran telepon dan

kemudian akan diinisialisasi oleh sentral telepon. Pada *dialing* nada, masing-masing digit diwakili oleh sepasang nada seperti terdapat dalam Gambar 2.3. Terdapat empat kelompok nada rendah, satu untuk setiap baris dan tiga kelompok nada tinggi, satu untuk setiap kolom (sebenarnya terdapat empat kelompok kolom, untuk kolom ke empat biasanya tidak dipakai).

Saat memilih nomor, maka akan menghubungkan baris dan kolom sehingga akan menghasilkan sepasang nada yang akan dikirimkan ke sentral. Dialing dengan menggunakan DTMF mempunyai durasi waktu yang sama untuk semua digitnya sehingga nada yang dikirim mempunyai waktu sekitar 0,25 sampai 0,5 detik selama tombol ditekan (Schweber, 1996:475). Serta memiliki selang waktu antara nada selama 0,25 sampai 0,5 detik.



Gambar 2.3. Pasangan frekuensi nada DTMF untuk masing-masing nomor

Sumber : *Electronic Communication System*, 1996: 16-476

Keuntungan yang didapat dari penggunaan dialing dengan DTMF adalah DTMF lebih cepat dalam pengiriman sinyal dibanding dengan dialing dengan pulsa. Contoh perhitungannya adalah sebagai berikut :

Misalkan akan dihubungi nomor 564954 maka :

Dengan menggunakan *dialing* pulsa, telah ditetapkan bahwa kecepatannya adalah 10 pulsa per detik dan mempunyai selang waktu antar digit 0,5 detik. Sehingga untuk satu pulsa membutuhkan waktu selama 0,1 detik maka untuk menghubungi nomor 564954 membutuhkan waktu dialing (T_{dial}) selama :

$$T_{dial} = [\{\Sigma(0{,}1 \text{ x nomor})\}+\{0{,}5 \text{ x } \Sigma_{\text{selang waktu antar digit}}\}] \text{ detik}$$

maka :

$$T_{dial} = [3{,}3 + 2{,}5] \text{ detik} = 5{,}8 \text{ detik.}$$

Dial dengan pulsa untuk menghubungi nomor 564954 membutuhkan waktu selama 5,8 detik.

Dengan menggunakan DTMF dan ditetapkan bahwa untuk masing-masing nada membutuhkan waktu 0,5 detik dan selang waktu antar nada membutuhkan waktu 0,25 detik maka T_{dial} memerlukan waktu selama :

$$T_{dial} = [(0{,}5 \text{ x } \Sigma_{nomor})+(0{,}25 \text{ x } \Sigma_{\text{selang waktu antar digit}})] \text{ detik}$$

Maka :

$$T_{dial} = [3 + 1{,}25] \text{ detik} = 4{,}25 \text{ detik.}$$

Dial dengan DTMF untuk menghubungi nomor 564954 membutuhkan waktu selama 4,25 detik.

Sehingga nampak bahwa untuk contoh di atas dial dengan DTMF memerlukan waktu yang lebih cepat 1,55 detik dibandingkan dial dengan pulsa

2.1.5. Bel

Bel (*Ringer*) dipakai untuk menunjukan sinyal dering yang berupa sinyal AC dengan tegangan 90 V *rms* yang mempunyai frekuensi 20 Hz dengan periode 2 dt *"on"* dan 4 dt *"off"* (*Digital and Analog Communications System*, 1990:5-363).

2.1.6. Sentral Telepon

Salah satu fungsi sentral telepon adalah sebagai penghubung di antara loop lokal, loop lokal lain pada sentral yang sama dan saluran pada sentral lain. Hubungan menuju sebuah loop lokal dinamakan *Subscriber Loop Interface Circuit* (SLIC) atau Sirkuit Penghubung Loop Pelanggan yang bertanggungjawab menyediakan sinyal pada loop, memantau kerja loop, dan mengirimkan sinyal kontrol ke telepon pada saat loop selesai disambungkan. SLIC digunakan oleh setiap telepon untuk berhubungan dengan sentral (Schweber, 1996:475). Sinyal kontrol berada pada loop selama saklar hook berada pada *on-hook* atau *off-hook*, *dialing* (panggilan), percakapan, dan pengiriman sinyal bel. Parameter-parameter standar telepon untuk loop pelanggan terdapat dalam Tabel 2.1.

Tabel 2.1. Standard Telepon untuk Loop Pelanggan

Item	Standard
On-hook (idle status)	Line open circuit, minimum dc resistance 30 kΩ
Off-hook (busy status)	Line close circuit, maximum dc resistance 200 Ω
Battery voltage	48 V
Operating current	20-80 mA
Subscriber-loop resistance	0-1300 Ω, 3600 Ω (max)
Loop loss	8 dB (typical), 17 dB (max)
Ringing voltage	90 V rms, 20 Hz (typical usally pulsed on 2 sec, off 4 sec)
Pulse dialing	Momentary open-circuit loop
Pulsing rate	10 pulse/sec ± 10 %
Duty cicle	58-64 % break (open)
Time between digit	600msec minimum
Pulse code	1 pulse = 1, 2pulse = 2, ..., 10 pulse = 0
Touch-Tone[a] dialing	Uses two tone, a low frequency and a high frequency tone, to specify each digit :
Level each tone	-6 to -4 dBm
Maximum different in level	4 dB
Maximum level (pair)	+4 dBm
Frequency tolerance	± 1.5 %
Pulse width	50 msec
Time between digits	45 msec minimum
Dial tone	350-440 Hz
Busy signal	480-620 Hz, with 60 interuptions per minute
Ringing signal tone	440-480 Hz, 2 sec on, 4 sec off

	High Tone (Hz)		
Low Tone	1209	1336	1477
697	1	2	3
770	4	5	6

[a]Touch-tone was a registered trademark of AT&T. It is also known as *dual tone multiple frequency* (DTMF) *signaling.*

Sumber : Digital and Analog Communications System, 1990: 5-363

Beberapa hal yang perlu diperhatikan dalam pemakaian pesawat telepon dan diperlukan sebagai dasar perancangan sistem aplikasi adalah:

1.) Melalui panggilan

Saat *handset* telepon dalam keadaan ditekan (*on hook*) akan menyebabkan *hook* telepon tertekan kebawah. Hal ini menyebabkan rangkaian telepon terpisah dengan sentral, tetapi rangkaian bel telepon selalu dalam keadaan terhubung ke sentral. Tegangan saluran telepon dalam keaadaan ini adalah 48 V DC dan arus yang mengalir adalah 0mA karena *loop* pelanggan menjadi suatu rangkaian terbuka.

Apabila *handset* diangkat, mengakibatkan saklar *hook* berada pada posisi atas (*off hook*) sehingga rangkaian pesawat telepon terhubung dengan sentral dan rangkaian bel terputus dari sentral. Karena *loop* pelanggan menjadi tertutup, maka arus DC dari baterai mengalir serta memacu rangkaian pada pesawat telepon. Pada keadaan ini tegangan menjadi 48 V DC dan arus yang mengalir 20-80 mA. Aliran arus ini sekaligus memberitahu kepada sentral bahwa seseorang berusaha untuk melakukan suatu hubungan telepon. Sentral akan mengirimkan sebuah nada panggil (*dial tone*) dengan frekuensi 350-440 Hz secara kontinyu. Hal ini menunjukan kepada pelanggan bahwa sentral telah siap untuk menerima sebuah nomor telepon.

2.) Mengirimkan nomor telepon

Pengiriman nomor telepon menggunakan nada frekuensi audio ini hanya dapat dipergunakan pada sentral yang telah memiliki kemampuan memproses nada. Sistem DTMF terdiri atas dua kelompok frekuensi. Penekanan sebuah tombol akan menyebabkan sebuah rangkaian elektronik didalam pesawat

telepon mengeluarkan sepasang nada, yang terdiri dari sebuah kelompok frekuensi tinggi sebagai pengganti nomor angka.

3.) Menghubungkan telepon

Sentral telepon mempunyai sebuah saklar pemindah dan relai yang secara otomatis menghubungkan terpanggil dan pemanggil. Dalam keadaan ini, sentral mengusahakan suatu hubungan dengan pesawat telepon terpanggil, maka sebuah sinyal bel akan dikirimkan oleh sentral sebagai tanda panggil kepada pesawat telepon terpanggil. Jika pesawat telepon terpanggil dan telepon dalam keadaan tidak terpakai, maka pada saat yang sama sentral juga mengirimkan suatu nada kepada pesawat telepon pemanggil sebagai tanda bahwa pesawat telepon terpanggil sedang berdering. Apabila pesawat telepon terpanggil dalam keadaan terpakai maka sentral akan mengirimkan sebuah nada sibuk (*busy tone*) kepada pesawat telepon pemanggil.

4.) Penjawab panggilan

Pada proses pangilan yang dilakukan oleh sentral sedang berlangsung, pengangkatan *handset* telepon terpanggil akan memberikan respon terhadap panggilan tersebut. Saklar *hook* akan tertutup (*off hook*) dan loop arus DC mengalir dari baterai sentral menuju kerangkaian pesawat telepon terpanggil. Arus yang mengalir ini dideteksi oleh sentral, yang kemudian memperhatikan pengiriman sinyal *ring back tone* maupun sinyal bel, dan sentral menghubungkan kedua pesawat telepon tersebut dengan menggunakan saklar yang ada padanya.

5.) Mengakhiri panggilan

Hubungan telepon diakhiri dengan peletakan kembali *handset* pesawat telepon. Keadaan ini memberitahukan kepada sentral untuk memutuskan jalur hubungan antara kedua pesawat telepon.

2.1.7 *Audible Tone* dan *Current Signaling*

Audible tone dan *current signaling* merupakan sinyal yang diberikan oleh sentral ke pelanggan, agar pelanggan-pelanggan mengetahui kondisi peralatan disentral, atau kondisi-kondisi pelanggan yang dipanggil. Arti dan spesifikasi *audible tone* dan *current signaling* adalah sebagai berikut:

1) Ringing Current

Setelah saluran pelanggan yang dipanggil tersambung, segera dikirim arus bel kesaluran pelanggan tersebut. Arus bel: 20 Hz, 90V rms, dengan periode 2 dt *"on"*, 4 dt *"off"*. Lama pengiriman antra 30 sampai 60 dt.

2) Dial Tone

Saat pelanggan melakukan *off hook* untuk melakukan pengiriman, *dial tone* akan dikirimkan ke pelanggan segera setelah *receiver* dari sentral siap menerima nomor. Frekuensi *dial tone*: 350-440 Hz kontinyu sampai pelanggan mulai mengirimkan nomor.

3) Ringing Tone

Apabila hubungan telah terjadi, *ringing tone* akan dikirim ke pelanggan pemanggil, bersamaan dengan pengiriman *ringing current* ke pelanggan yang dipanggil. *Ringing tone* akan putus apbila pelanggan menjawab atau memutuskan hubungan.

4) *Busy Tone*

Busy Tone dikirim apabila:

a) Pelanggan yang dipanggil sibuk.

b) Pelanggan yang tidak melakukan panggilan setelah batas waktu 15-20 dt setelah menerima *dial tone*.

c) Melampaui batas waktu 15-20 dt setelah memutar nomor salah.

d) 30-60 dt setelah pelanggan yang dipanggil memutuskan hubungan.

e) Bila seluruh rangkaian *switch* disentral sibuk (*intercongestin*).

f) Setelah memutar 0 atau 00 pada koin blok untuk SLJJ atau SLI.

2.2. Mikrokontroler Renesas R8C/13 Tiny (R5F21134FP)

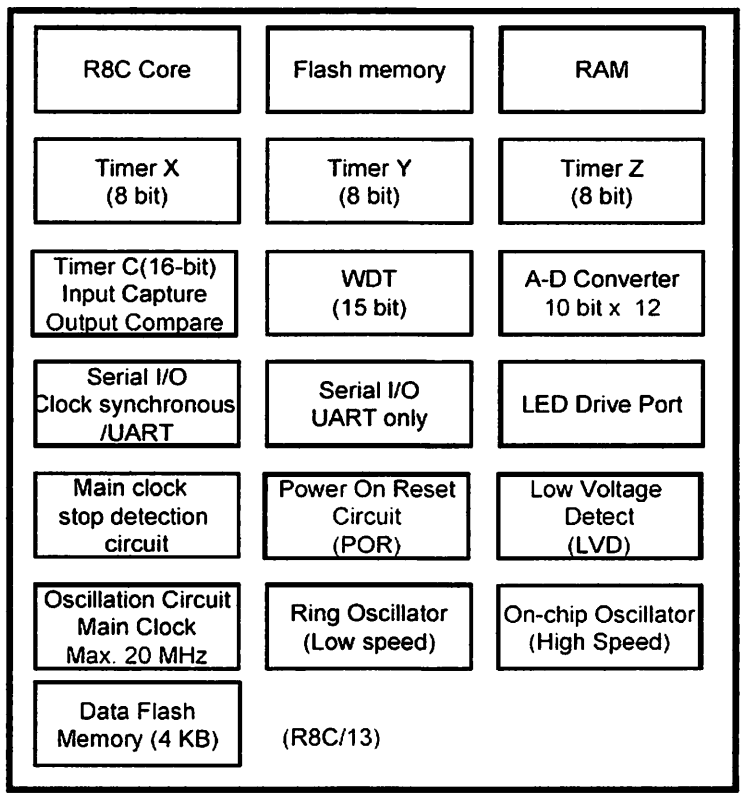
Renesas Technologi adlah produsen semikondoktor tingkat internasonal. Renesas merupakan gabungan dari dua produsen semikonduktor, yaitu Mitsubishi dan Hitachi. Sebagai produsen semikonduktor, renesas juga mengeluarakan berbagai jenis keluarga mikrokontroler (MK).

Renesas R8C adalah salah satu jenis seri dalam keluarga MK M16C. CPU R8C sama dengan CPU CISC 16-*bit* M16C. hanya saja lebar jalur data R8C adalah 8-*bit*. Karena menggunakan CPU yang sama maka R8C memiliki *instruction set* hamper sama dengan M16C. perbedaannya hanya terletak pada 2 instruksi, yaitu R8C tidak memiliki JMPS (*jump special page*) dan JSRS (*jump subroutine special page*). R8C/13 adalah salah satu tipe MK dalam seri R8C. MK ini memiliki kemasan 32-*pin* LQPF. Dalam perancangan pada skripsi ini menggunakan MK seri R5F21134, yaitu R8C/13 yang memiliki Flash ROM 16 KB (1000 E/W *cyles*) dan RAM sebesar 1 KB.

2.2.1. Spesifikasi R5F21134FP

Berikut adalah spesifikasi R5F21134FP dengan peta peripheral dan memori-memorinya:

- Mempunyai CPU *core* (16-*bit*) 1-20 MHz, 3.0-5.5 Volt dan 1-10 MHz, 2.7-5.5 Volt.
- Rangkaian *Clock*, kecepatan *low/ high on chip oscillator*. *Clock* utama dengan Xin/ Xout.
- Memori (ROM/RAM) 16 Kbytes/ 1Kbytes, 2 x 2 Kbytes Data Flash.
- Kemasan 32 pin LQPF (7mm x 7mm)



Gambar 2.4. Blok Diagram R8C/11, 13 dan Peta *Peripheral*-nya

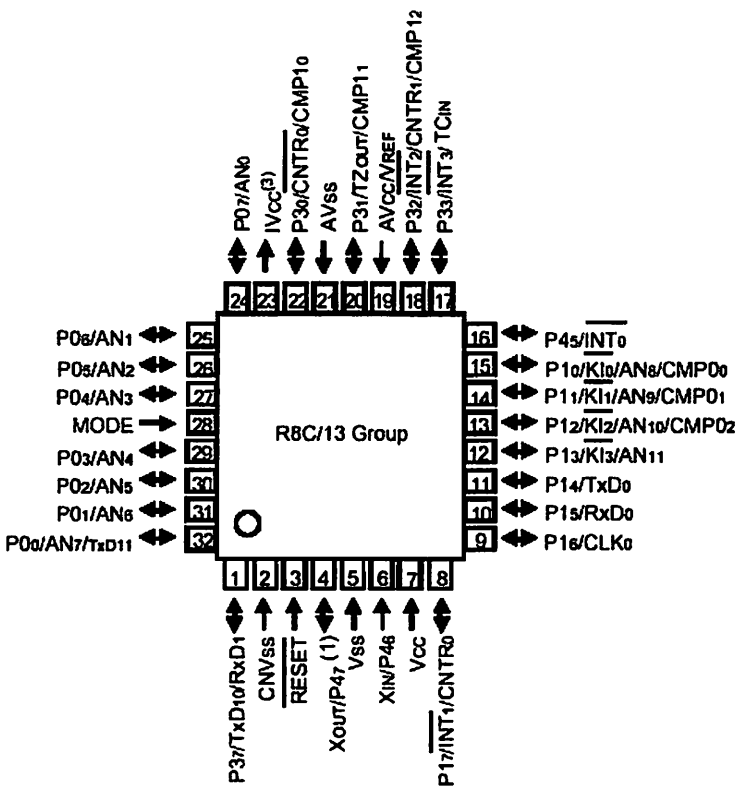
Sumber: www.renesas.com

Banyak kelebihan-kelebihan yang dimiliki oleh R8C/13 diantaranya adalah:

- Kompatibel dengan M16C yaitu kompatibel dalam instruksi dan kode.

- *Peripheral* lebih terintegrasi jadi lebih hemat.
- *Electromagnetic Compability* (EMC) mempunyai EMI rendah, EMS tinggi
- *Development tool* (*compiler* dan *debugger*) didapat dengan murah dan difasilitasi *on-chih debugger*.
- Mempunyai fitur *fail-safe* yaitu pengamanan terhadap kegagalan sistem.
- Konsumsi daya rendah.
- 16-bit CISC CPU dengan kecepatan maksimal 20 MHz (1:1).
- 89 Instruksi CISC lebih hemat ROM kira-kira 20%, RAM sampai 1 KB.
- Waktu konversi ADC hanya 3 uS

2.2.2. Konfigurasi Pin R8C/13 R5F21134FP



Gambar 2.5. Konfigurasi Pin R8C/13 R5F21134FP

Sumber: www.renesas.com

Gambar diatas adalah konfigurasi pin-pin dari R8C/13 R5F21134FP untuk lebih jelasnya dapat diamati pada tabel deskripsi pin-pin berikut ini:

Tabel 2.2 konfigurasi pin-pin dari R8C/13 R5F21134FP

Nama Sinyal	**Nama Pin**	**Tipe I/O**	**Fungsi**
Masukan Catu daya	Vcc, Vss	I	Tegangan 2.7 V-5.5 V pada pin Vcc.tegangan 0 V pada pin Vss
IVcc	IVcc	O	Pin ini untuk menstabilkan ccatu daya *internal*, pin ini dihubungkan pda Vss melalui kapasitor 100nF. Jangan dihubungkan pada Vcc.
Input catu daya analog	AVcc, AVss	I	Pin-Pin ini merupakan inputan Catu Daya Untuk ADC. AVcc dihubungkan pada Vcc, AVss dihubungkan ke Vss. Antara pin AVcc dengan AVss dihubungkan sebuah kapasitor
Input reset	$\overline{RESET}$	I	"L" pada inputan akan mereset MCU
CNVss	CNVss	I	Hubungkan pin ini pada Vss melalui sebuah resistor.
MODE	MODE	I	Hubungkan pin ini pada Vcc melalui sebuah resistor.
Input clock utama	Xin	I	Pin-pin ini disediakan untuk membangkitkan rangkaian I/O clock utama. Pin Xin dan Xout dihubungkan oleh sebuah resonator keramik atau osilator kristal. Jika menggunakan clock intermal maka pin Xin dan Xout dalam keadaan terbuka
Output clock utama	Xout	O	
Input interupsi $\overline{INT}$	$\overline{INT0 - INT3}$	I	Pin-pin ini sebagai masukan interupsi $\overline{INT}$
Input kunci interupsi	$\overline{KI0 - KI3}$	I	Pin-pin ini sebagai masukan kunci interupsi
Timer X	$CNTR_0$	I/O	Pin ini adalah I/O timer X
	$\overline{CNTR_0}$	O	Pin ini adalah output timer X

Timer Y	$CNTR_1$	I/O	Pin output untuk timer Y
Timer Z	TZout	O	Pin output untuk timer Z
Timer C	TC in	I	Pin input untuk timer C
	$CMP0_0$-$CMP0_3$, $CMP1_0$-$CMP1_3$	O	Pin output untuk timer C
Serial interface	CLK_0	I/O	Pin untuk memindahkan clock
	RxD_0, RxD_1	I	Pin input untuk data serial
	TxD_0, TxD_{10}, TxD_{11}	O	Pin output untuk data serial
Input tegangan referensi	Vref	I	Pin ini merupakan tegangan referensi untuk ADC. Hubungkan pin Vref ke pin Vcc
ADC, Pengubah dari analog ke digital	AN_0-AN_{11}	I	Pin-pin ini untuk masukan ADC
Port I/O	$P0_0$-$P0_7$, $P1_0$-$P1_7$, $P3_0$-$P3_3$, $P3_7$,$P4_5$	I/O	Merupakan I/O CMOS 8-bit. Setiap port mempunyai pilihan register pengarah sebagai input atau output. Tiap port dapat dialamati per bit. Dapat di-set menggunakan pull up resistor dengan program. Pin $P1_0$-$P1_7$ juga sebagai port pengendali LED
Port input	$P4_6$, $P4_7$	I	Pin ini hanya bisa digunakan sebagai input

Sumber: www.renesas.com

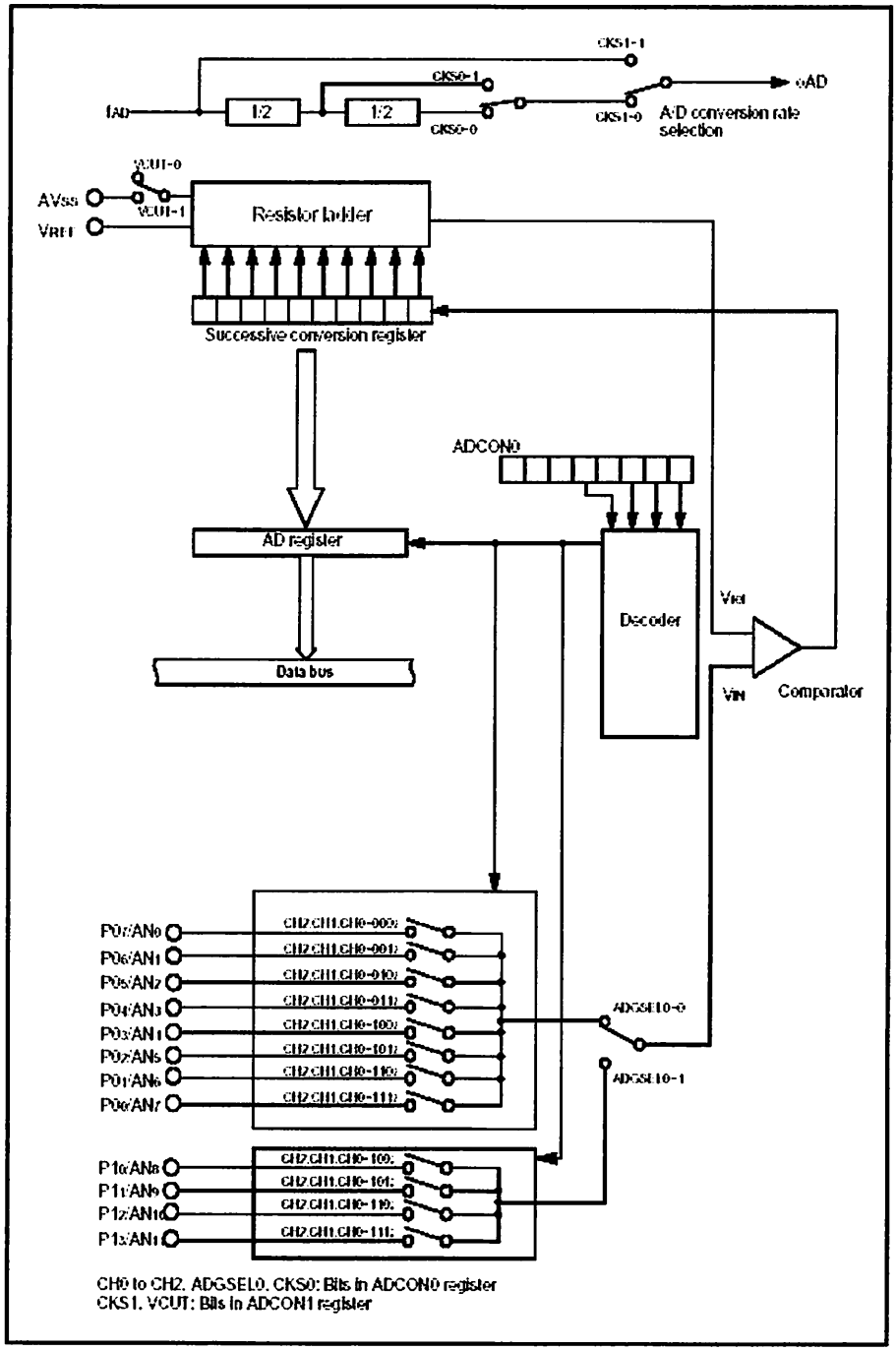
2.2.3. Peripheral R8C/13 R5F21134FP

Mikrokontroler R8C/13 R5F21134FP mempunyai beberapa *peripheral-peripheral* yang banyak digunakan pada beberapa aplikasi-aplikasi penting, diantaranya sebagai berikut:

- ***Analog To Digital Converter*** **(ADC)**

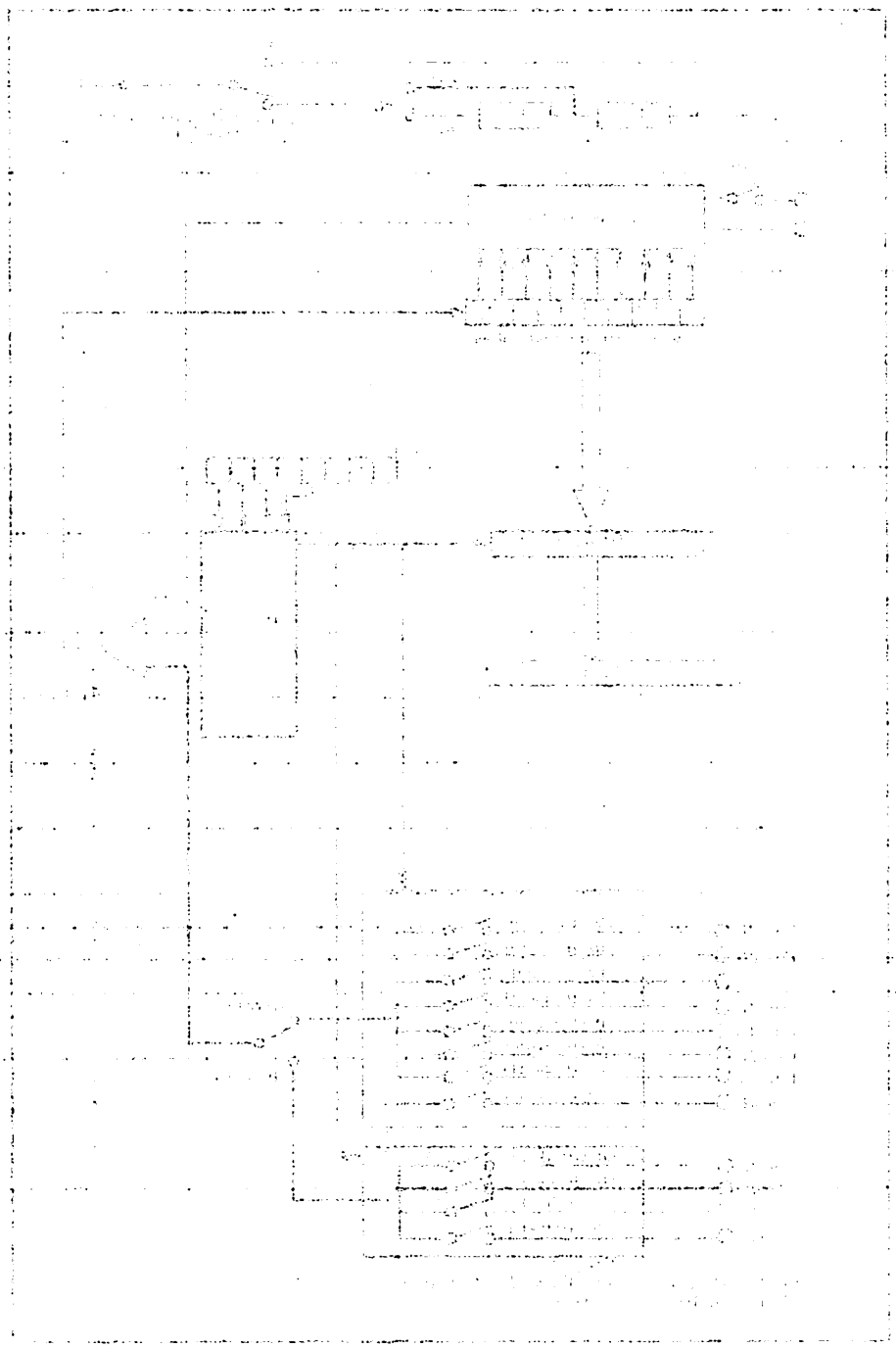
  Dengan 12 SAR ADC S/H yang mempunyai resolusi 8-bit atau 10-bit. Mode operasinya menggunakan *One-Shot* dan *Repeat* dengan waktu konversi 2.8 uS

(pada clock 10 Mhz). Berikut gambar diagram blok ADC *built-in* pada mikrokontroler ini:



Gambar 2.6. Diagram blok ADC

Sumber: www.renesas.com



- ***Timer* mode**

Mempunyai 4 buah *timer* yaitu *timer* X, Y, Z, C. berikut adalah mode-mode *timer*-nya:

Tabel 2.3. Mode mode *timer*

Item		Timer X	Timer Y	Timer Z	Timer C
Configuration		8-bit timer with 8-bit prescaler	8-bit timer with 8-bit prescaler	8-bit timer with 8-bit prescaler	16-bit free-run timer
Count		Down	Down	Down	Up
Count source		•f_1 •f_2 •f_8 •f_{32}	•f_1 •f_8 •f_{RING} •Input from CNTR1 pin	•f_1 •f_2 •f_8 •Timer Y underflow	•f_1 •f_8 •f_{32} •$f_{RING-fast}$
Function	Timer mode	provided	provided	provided	not provided
	Pulse output mode	provided	not provided	not provided	not provided
	Event counter mode	provided	provided[1]	not provided	not provided
	Pulse width measurement mode	provided	not provided	not provided	not provided
	Pulse period measurement mode	provided	not provided	not provided	not provided
	Programmable waveform generation mode	not provided	provided	provided	not provided
	Programmable one-shot generation mode	not provided	not provided	provided	not provided
	Programmable wait one-shot generation mode	not provided	not provided	provided	not provided
	Input capture mode	not provided	not provided	not provided	provided
	Output compare mode	not provided	not provided	not provided	provided
Input pin		CNTR0	CNTR1	INT0	TCIN
Output pin		CNTR0 CNTR0	CNTR1	TZOUT	CMP00 to CMP02 CMP10 to CMP12
Related interrupt		Timer X int INT1 int	Timer Y int INT2 int	Timer Z int INT0 int	Timer C int INT3 int compare 0 int compare 1 int
Timer stop		provided	provided	provided	provided

Sumber: www.renesas.com

- ***Low Votage Detect* (LVD)**

LVD adalah untuk mendeteksi Vcc kurang dari 3.8 V (± 0.5 V).

- ***Watchdog Timer***

  Watchdog berfungsi untuk mendeteksi ketika program diluar control.

- ***On Chip Debugger***

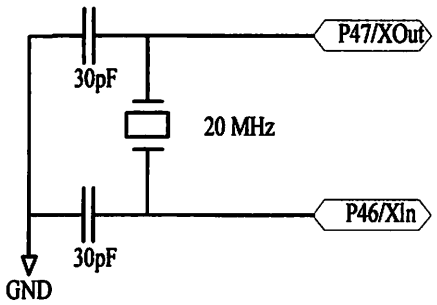
  Fasilitas ini mempunyai fungsi untuk dapat di-*debug* pda waktu MCU sedang berjalan. Antara PC dan MCU dapat berkomunikasi, PC akan mengetahui aktivitas MCU saat itu. Syarat-syarat *On Chip Debugger* adalah:

  1. Vektor *address match interrupt* harus dihindari .
  2. *Single step interrupt* tidak dapat digunakan bersamaan dengan *interrupt* lain.
  3. UART1 tidak boleh dipakai
  4. Instruksi BRK tidak boleh dipakai.
  5. Flash *address* C000H-C7FFH.
  6. PD 3.7 harus "0".
  7. B5 FMR 0 harus "1".
  8. menyiapkan 8 *Byte* untuk stack.
  9. *On Chip Debugger* berpengaruh dengan *timing run*

- **Rangkaian Osilator**

Pada rangkaian osilator utama dapat menggunakan keramik resonator atau kristal osilator antara 0-20 MHz, dengan fitur *Clock Stop Detect*. Kemudian untuk *On Chip Oscillator* disediakan kecepatan *Low* 125 KHz dan *High* 8 MHz. setelah reset, default *clock* adalah kecepatan rendah (*Low*).

Dalam minimun sistem ini menggunakan kristal 20Mhz dan C1=C2 sebesar 30pF. Dengan rangkaian sebagai berikut :



Gambar 2.7 Rangkaian *Clock* pada Mikrokontroler Renesas R8C/11

Dengan menggunakan nilai kristal dan kapasitor diatas maka dapat dihitung waktu yang diperlukan untuk satu siklus mesin.

Diketahui : F = 20 Mhz

$$T = \frac{1}{f} \tag{3-1}$$

Sehingga :

$$T \frac{1}{20\ Mhz} = \frac{1}{20} \mu s$$

Maka untuk satu siklus mesin dari mikrokontroler Renesas R8C/11 adalah sebesar :

$$Tm = 20 x T$$

$$Tm = 20 \times \frac{1}{20} \mu s = 1 \mu s$$

$$Tm = 1 \mu s$$

2.3. Mikrokontroler AT89S51

AT89S51 merupakan salah satu mikrokontroler dari buatan ATMEL keluarga MCS-51 yang mempunyai 4 kbyte Flash PEROM (*Flash Programmable and Erasable Read Only Memory*), 128 byte RAM, 32 pin I/O (4 buah *port* I/O bit) yang mana tiap pin tersebut dapat diprogram secara paralel dan tersendiri, mempunyai dua buah timer/counter 16 bit, mempunyai watchdog timer, serta dua data pointer.

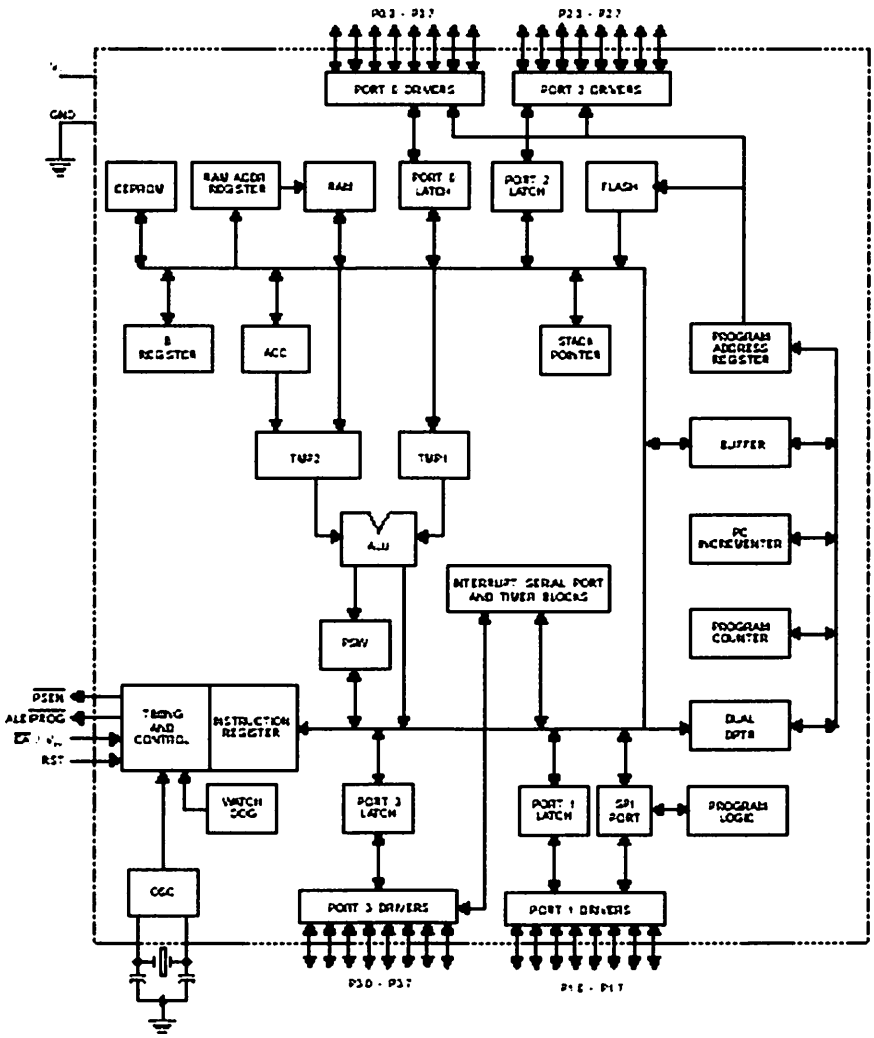
Pada dasarnya mikrokontroler adalah terdiri atas mikroprosesor, *timer*, dan *counter*, perangkat I/O dan internal memori. Mikrokontroler termasuk perangkat yang sudah didesain dalam bentuk *chip* tunggal. Mikrokontroler dikemas dalam satu *chip* (*single chip*). Mikrokontroler didesain dengan instruksi-instruksi lebih luas dan 8 bit instruksi yang digunakan membaca data instruksi dari internal memori ke ALU.

Sebagai suatu sistem kontrol mikrokontroler AT89S51 bila dibandingkan dengan mikroprosesor memiliki kemampuan dan segi ekonomis yang bisa diandalkan karena dalam mikrokontroler sudah terdapat RAM dan ROM sedangkan mikroprosesor didalamnya tidak terdapat keduanya. Secara umum konfigurasi yang dimiliki mikrokontroler AT89S51 adalah sebagai berikut : (Atmel, 1997: 4-29)

- Sebuah CPU 8 bit dengan menggunakan teknologi dari Atmel.
- Memiliki memori baca-tulis (RAM) sebesar 128 byte.
- Jalur dua arah (*bidirectional*) yang digunakan sebagai saluran masukan atau keluaran.
- Sebuah *port* serial dengan kontrol *full duplex* UART (*Universal Asynchronous Receiver Transmitter*).
- Dua buah *timer/counter* 16 bit.
- Osilator internal dan rangkaian pewaktu.

- Flash PEROM yang besarnya 4 kbyte untuk memori program
- Kemampuan melaksanakan operasi perkalian, pembagian, dan operasi *Boolean.*
- Mampu beroperasi sampai 24 MHz.

Sedangkan untuk blok diagram AT89S51 diperlihatkan dalam Gambar 2.7:

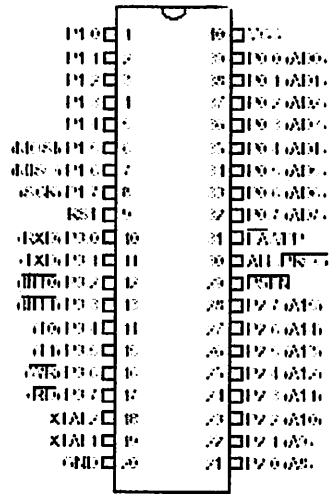


Gambar 2.7. Blok Diagram AT89S51

Sumber: www.atmel.com

2.3.1 Penjelasan Fungsi Pin AT89S51

Mikrokontroler AT89S51 mempunyai 40 pin seperti yang ditunjukkan dalam Gambar 2.8. Fungsi-fungsi pin dijelaskan sebagai berikut:



Gambar 2.8. Konfigurasi Pin AT89S51

Sumber: www.atmel.com

Fungsi kaki-kaki AT89S51 adalah:

- *Port* 1 (Pin 1..8), merupakan saluran masukan/keluaran dua arah.
- Pin 9 RST, merupakan saluran dua masukan untuk mereset mikrokontroler dengan cara memberi masukan logika tinggi.
- *Port* 3 (Pin 10..17), merupakan saluran masukan/keluaran dua arah dan mempunyai fungsi khusus. Fungsi khusus meliputi TXD (*Transmit Data*), RXD (*Receive Data*), $\overline{INT0}$ (*Interupt 0*), $\overline{INT1}$ (*Interupt 1*), T0 (*Timer 0*), T1 (*Timer 1*), $\overline{WR}$ (*Write*), $\overline{RD}$ (*Read*).
- Pin 18 dan 19 ($XTAL_1$ dan $XTAL_2$), merupakan saluran untuk mengatur pewaktuan sistem. Untuk pewaktuan dapat dapat menggunakan pewaktuan internal maupun eksternal.

- Pin 20 V_{SS}, merupakan hubungan ke *ground* dari rangkaian.
- *Port* 2 (Pin 21..28), merupakan saluran masukan/keluaran dua arah.
- Pin 29 $\overline{\text{PSEN}}$ (*Program Store Enable*), merupakan sinyal baca untuk mengaktifkan memori program eksternal.
- Pin 30 *ALE*/$\overline{\text{PROG}}$ (*Address Latch Enable*), merupakan pulsa yang berfungsi untuk menahan alamat rendah (A0-A7) dalam *port* 0, selama proses baca/tulis memori eksternal. Frekuensi ALE adalah $\frac{1}{6}$ kali frekuensi osilator, dan dapat digunakan sebagai pewaktu. Pin ini juga berfungsi sebagai saluran program selama dilakukan pemrograman jika menggunakan memori program internal.
- Pin 31 $\overline{\text{EA}}$/VPP (*External Access Enable*), untuk mengatur penggunaan memori program eksternal dan internal. Pin ini harus dihubungkan dengan *ground* bila menggunakan memori program eksternal dan dihubungkan dengan VPP sebesar 12 volt jika menggunakan memori program eksternal.
- *Port* 0 (Pin 32..39), merupakan saluran masukan/keluaran *open drain.*
- Pin 40 V_{CC}, merupakan saluran masukan untuk catu daya positif sebesar 5 volt DC dengan toleransi lebih kurang 10%.

2.2.2 Organisasi Memori Mikrokontroler AT89S51

AT 89S51 mempunyai struktur memori yang terdiri atas :

- RAM *Internal*

  Memori sebesar 128 *byte* yang biasanya digunakan untuk menyimpan variabel atau data yang bersifat permanen. RAM *internal* terdiri atas :

1. *Register Banks*

   AT89S51 mempunyai delapan buah *register* yang terdiri atas R0 hingga R7. Kedelapan *register* ini selalu terletak pada alamat 00H hingga 07H pada setiap kali sistem di*reset*. Namun posisi R0 hingga R7 dapat dipindah ke *Bank* 1 (08 H hingga 0FH), *Bank* 2 (10H hingga 17H) dan *Bank* 3 (18H hingga 1FH), dengan mengatur *bit* RS0 dan RS1.

2. *Bit* Addressable RAM

   RAM pada alamat 20H hingga 2FH dapat diakses secara pengalamatan *bit* (*bit addressable*) sehingga hanya dengan sebuah instruksi saja setiap *bit* dalam area ini dapat diset,*clear, AND, OR*.

- RAM keperluan umum

  RAM keperluan umum dimulai dari alamat 30H hingga 7FH dan dapat diakses dengan pengalamatan langsung maupun tak langsung. Pengalamatan langsung dilakukan ketika salah satu *operand* merupakan bilangan yang menunjukkan lokasi yang dialamati.

- *Special Function Register*

  Memori yang berisi *register-register* yang mempunyai fungsi-fungsi khusus yang disediakan oleh mikrokontroler tersebut, seperti *Timer*, *serial* dan lain-lain. 89S51 mempunyai 21 *Special Function Register* yang terletak pada alamat 80H hingga FFH. Alamat *register* fungsi khusus ditunjukkan pada tabel 2.12.

Tabel 2.4. *Special Function Register*

Simbol	**Nama *Register***	**Alamat**
ACC	*Accumulator*	$E0_H$
B	*Register B*	$F0_H$
PSW	*Program Status Word*	$D0_H$
SP	*Stack Pointer*	81_H
DPTR	*Data Pointer 2 Byte*	
DPL	*Bit rendah*	82_H
DPH	*Bit Tinggi*	83_H
P0	*Port 0*	80_H
P1	*Port 1*	90_H
P2	*Port 2*	$A0_H$
P3	*Port 3*	$B0_H$
IP	*Interupt Periority Control*	$D8_H$
IE	*Interupt Enable Control*	$A8_H$
TMOD	*Timer/Counter Mode Control*	89_H
TC*ON*	*Timer/Counter Control*	88_H
TH0	*Timer/Counter 0 High Control*	$8C_H$
TL0	*Timer/Counter 0 Low Control*	$8A_H$
TH1	*Timer/Counter 1 High Control*	$8D_H$
TL1	*Timer/Counter 1 Low Control*	$8B_H$
SC*ON*	*Serial Control*	98_H
SBUF	*Serial Data Buffer*	99_H
PC*ON*	*Power Control*	87_H

Sumber: www.atmel.com

Beberapa macam *register* fungsi khusus yang sering digunakan adalah sebagai berikut ini :

- *Accumulator* (ACC) merupakan *register* untuk penambahan dan pengurangan. Perintah *mnemonic* untuk mengakses akumulator disederhanakan sebagai A.
- *Register B* merupakan *register* khusus yang berfungsi melayani operasi perkalian dan pembagian.
- *Stack Pointer* (SP) merupakan *register* 8 bit yang dapat diletakkan di alamat manapun pada RAM *internal*.

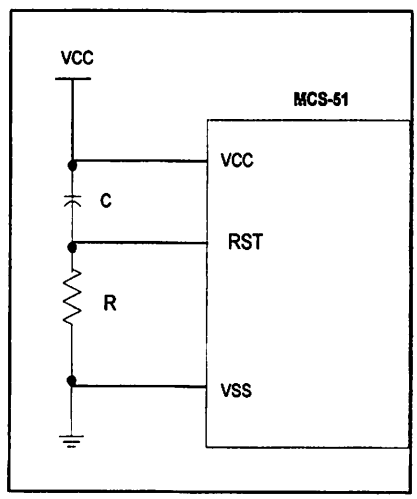
- *2 Data Pointer* (DPTR) terdiri dari dua *register*, yaitu untuk *byte* tinggi (*Data Pointer High*, DPH) dan *byte* rendah (*Data Pointer Low*, DPL) yang berfungsi untuk mengunci alamat 16 bit.
- *Port 0* sampai *Port 3* merupakan *register* yang berfungsi untuk membaca dan mengeluarkan data pada port 0, 1, 2, 3. Masing-masing *register* ini dapat dialamati per-*byte* maupun per-bit.
- *Control Register* terdiri dari *register* yang mempunyai fungsi kontrol. Untuk meng*on*trol sistem interupsi, terdapat dua *register* khusus, yaitu *register* IP (*Interupt Priority*) dan *register* IE (*Interupt Enable*). Untuk meng*on*trol pelayanan *Timer/Counter* terdapat *register* khusus, yaitu *register* TC*ON* (*Timer/Counter Control*) serta pelayanan port serial menggunakan *register* SC*ON* (*Serial Port Control*).
- *Flash* PEROM

  AT89S51 memiliki 4Kb *Flash* PEROM (*Programmable and Erassable Read Only Memori*), yaitu ROM yang dapat ditulis ulang atau dihapus menggunakan sebuah perangkat *programmer*. Program yang ada pada *Flash* PEROM akan dijalankan jika pada saat sistem di*reset*, pin EA/VP berlogika satu sehingga mikrokontroler aktif berdasarkan program yang ada pada *flash* PEROMnya. Namun, jika EA/VP berlogika nol, mikrokontroler aktif berdasarkan program yang berada pada memori eksternal.

Pada kondisi tertentu dapat juga terjadi dibutuhkan untuk memanggil program yang terletak pada memori *internal* walaupun saat pertama kali di*reset*, mikrokontroler memanggil program yang berada pada eksternal memori maupun sebaliknya.

2.3.3 Reset

Rangkaian *Power On Reset* diperlukan untuk mereset mikrokontroler secara otomatis setiap catu daya dinyalakan. ketika catu daya diaktifkan, rangkaian reset akan menahan logika tinggi pada penyemat RST dengan jangka waktu yang ditentukan oleh lamanya pengosongan muatan kapasitor. Untuk keabsahan reset, logika tinggi harus bertahan lebih lama dari dua siklus mesin ditambah waktu hidup *(start on)* oscilator . Gambar 2.9 menunjukkan rangkaian *Power On Reset.*

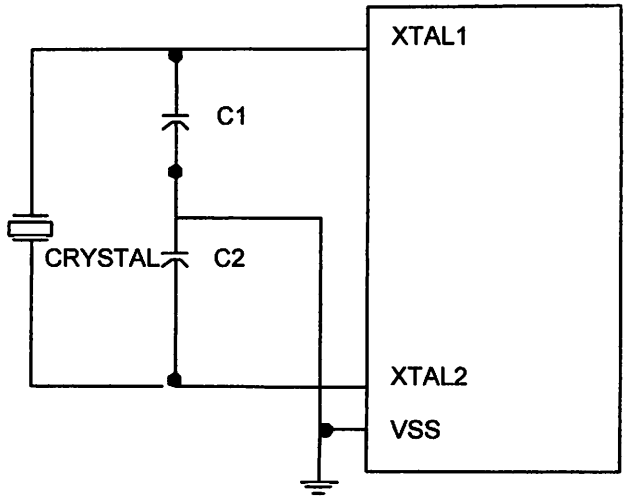


Gambar 2.9. Rangkaian Power On Reset

Sumber: www.atmel.com

2.3.4 Pewaktuan

Mikrokontroler AT89C51 memiliki rangkaian osilator internal dengan mengacu referensi frekuensi pada penyemat XTAL1 dan XTAL2. Referensi frekuensi berupa kristal dan kapasitor ditunjukkan pada Gambar 2.10.



Gambar 2.10 Rangkaian Pewaktuan dengan Osilator Eksternal

2.4 Tone Dekoder DTMF MT8870

DTMF (*Dual Tone Multi Frequency*) merupakan sistem signaling dengan frekuensi ganda. Dalam sistem ini signal tersusun atas sebuah kombinasi dari dua buah frekuensi yang dipilih satu demi satu dari tiap frekuensi dari dua kelompok frekuensi (lebih tinggi atau lebih rendah). Frekuensi tersebut masing-masing dialokasikan dan berhubungan dengan sebuah angka atau sebuah kode. Sebuah angka akan mewakili penggabungan dua *tone* tersebut.

Dalam DTMF, setiap angka dinyatakan oleh kombinasi dua frekuensi atas dan bawah seperti pada tabel berikut :

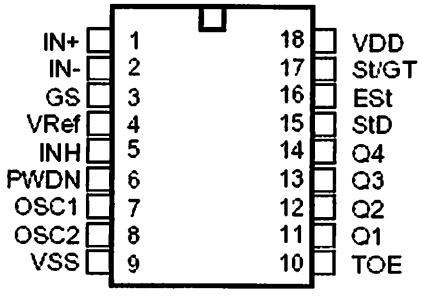
Tabel 2.5. Konfigurasi *Tone* Dialing Dan Angka

Low Group **(Hz)**	***High Group*** **(Hz)**			
	1209	1336	1447	1633
697	1	2	3	A
770	4	5	6	B
852	7	8	9	C
941	*	0	#	D

Sumber: www.zarlink.com

Dekoder DTMF adalah rangkaian yang mengkonversikan kode frekuensi menjadi kode data biner. Dekoder ini menggunakan teknik *counter* digital untuk mendeteksi nada DTMF 16 digit menjadi kode digital 4 bit.

Salah satu komponen DTMF adalah MT8870. MT8870 merupakan rangkaian yang didalamnya dilengkapi dengan filter yang menggunakan teknik *switched* kapasitor untuk membedakan pasangan frekuensi yang masuk. Sedangkan untuk dekoder digunakan teknik pencacahan secara digital untuk mendeteksi dan mengkode 16 buah pasangan frekuensi DTMF menjadi kode biner 4 *bit*. Selain itu, MT8870 juga dilengkapi dengan rangkaian-rangkaian internal *differensial amplifier, clock oscillator, band pass filter, tone dekoder*, rangkaian *latch* 3-*state* dan beberapa komponen lain. Di bawah ini akan digambarkan konfigurasi dekoder DTMF :



Gambar 2.11. Konfigurasi pin MT8870

Sumber: MITEL Corporation, USA

Adapun penjelasan kaki penyemat MT8870 adalah sebagai berikut :

- *Non inverting Op-Amp* (IN+)

  Sinyal masuk melalui kaki ini apabila tidak diperlukan pembalikan fasa.

- *Inverting* Op-amp (IN-)

  Sinyal masuk melalui kaki ini apabila diperlukan pembalikan fasa.

- GS *(Gain Select)*

  Kaki ini berfungsi sebagai pemilihan penguatan sinyal. Apabila memerlukan penguatan, maka diperlukan sebuah resistor yang dihubungkan ke kaki ini.

- Vref

  Tegangan referensi, nominal ½ VDD digunakan sebagai bias *input*.

- INH (*Inhibid)*

  Kaki ini diperlukan dalam mendeteksi nada DTMF yang mewakili karakter A, B, C, dan D. Bila diberikan logika *high*, akan dapat mendeteksi karakter tersebut tetapi bila diberikan logika *low*, karakter tersebut tidak bisa terdeteksi.

- PWDN (*Power Down*)

  Kaki ini diberikan logika *high* supaya daya yang diperlukan ditekan serendah-rendahnya pada saat keadaan menerima sinyal (*standby mode*). Kerja osilator dan penyaring pada saat *standby* akan dihentikan.

- OSC1 dan OSC2

  Pin ini dihubungkan dengan kristal sebesar 3,579545 MHz. OSC1 merupakan *clock input* dan OSC2 merupakan *clock output*.

- V_{SS} dan V_{DD}

Merupakan pin catu daya. V_{SS} dihubungkan dengan *ground* dan V_{DD} dihubungkan dengan catu daya positif.

- St/GT *[Steering Input/ GuardTime Output (Bidirectional)]*

  Tegangan yang dideteksi oleh St lebih besar dari tegangan V_{TSt} menyebabkan perangkat mencatat pasangan nada yang telah terdeteksi dan memperbarui keluaran *latch.* Apabila kurang dari tegangan V_{TSt} akan membebaskan perangkat untuk menerima pasangan nada baru. Keluaran GT berfungsi untuk m*ereset* konstanta waktu rangkaian *steering*, kondisi tersebut menyebabkan berfungsinya kembali ESt dan tegangan pada St.

- ESt (*Early Steering Output)*

  Kaki ini mengeluarkan logika *high*, apabila bagian digital algoritma dalam IC ini mendeteksi pasangan nada-nada DTMF (sinyal kondisi). Bila sinyal tersebut hilang seketika, akan mnyebabkan ESt kembali menuju logika *low.*

- StD (*Delayed Steering)*

  Bila pada masukan terdeteksi nada-nada DTMF, maka kaki ini akan mengeluarkan logika *high* dan bila tidak terdeteksi nada tersebut akan mengeluarkan logika *low*.

- $Q_1 - Q_4$

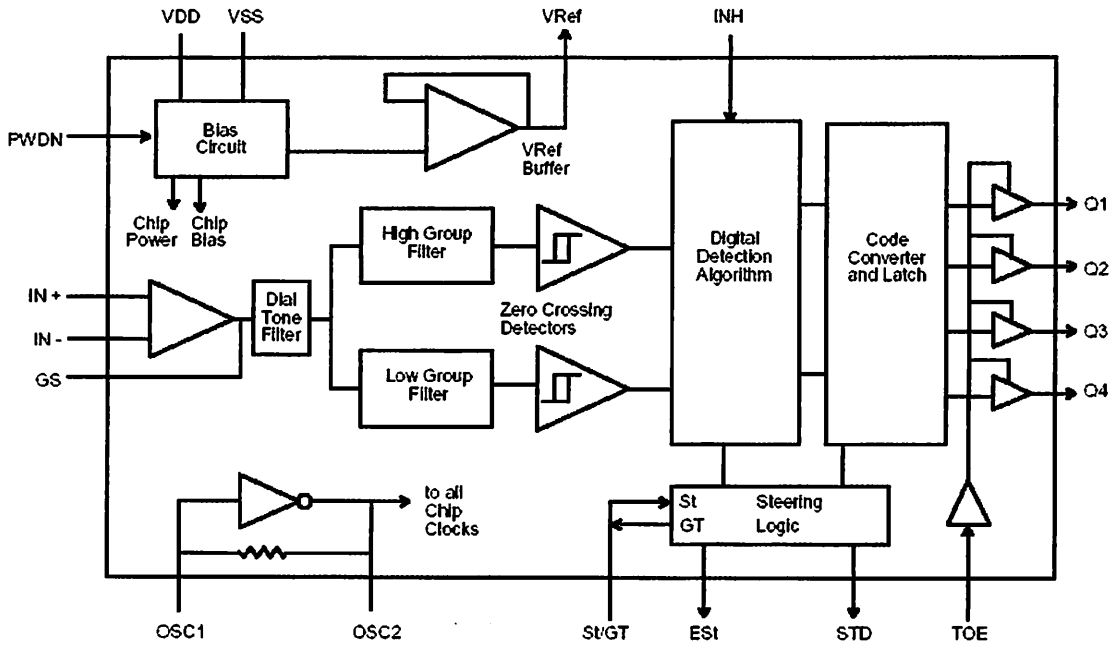
  Output data yang akan dikeluarkan.

- TOE (*Three State Output Enable)*

  Kaki ini berfungsi untuk mengendalikan data keluaran Q1, Q2, Q3, dan Q4. bila diberikan logika *high* maka Q1, Q2, Q3 dan Q4 akan

mengeluarkan data dan bila diberikan logika *low* maka impedansinya akan tinggi.

Blok diagram dari IC MT8870 seperti terlihat pada gambar 2.12 :



Gambar 2.12. Diagram Blok *Internal* MT8870

Sumber: MITEL Corporation, USA

IC MT8870 memerlukan komponen luar untuk dapat menerima nada-nada DTMF. Komponen tersebut digunakan sebagai penguat masukan, *clock oscillator*, dan rangkaian kendali.

Keterangan :

t_{GTA} = waktu pengosongan (*guard time absent*) dalam detik

t_{GTP} = waktu pengisian (*guard time present* dalam detik)

R = tahanan dalam ohm

C = kapasitor dalam farad

VDD = catu daya dalam volt

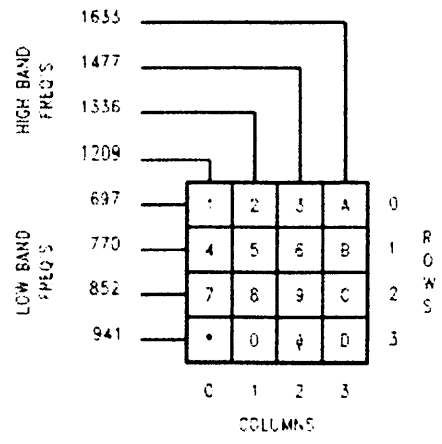
V_{TSt} = tegangan ambang St dalam volt

Fungsi dan pengaruh TOE, INH, dan EST terhadap data keluaran Q1, Q2, Q3 dan Q4 dapat terlihat pada tabel dibawah ini

Tabel 2.6. Tabel Kebenaran DTMF Dekoder MT8870

DIGIT	TOE	INH	EST	Q1	Q2	Q3	Q4
ANY	L	X	H	Z	Z	Z	Z
1	H	X	H	0	0	0	1
2	H	X	H	0	0	1	0
3	H	X	H	0	0	1	1
4	H	X	H	0	1	0	0
5	H	X	H	0	1	0	1
6	H	X	H	0	1	1	0
7	H	X	H	0	1	1	1
8	H	X	H	1	0	0	0
9	H	X	H	1	0	0	1
0	H	X	H	1	0	1	0
*	H	X	H	1	0	1	1
#	H	X	H	1	1	0	0
A	H	L	H	1	1	0	1
B	H	L	H	1	1	1	0
C	H	L	H	1	1	1	1
D	H	L	H	0	0	0	0
A	H	H	L	Undertected the *output* code will remain the same as the previous detected code			
B	H	H	L				
C	H	H	L				
D	H	H	L				

Sumber: MITEL Corporation, USA



Gambar 2.13. Matrik *Keyboard* DTMF

Sumber: MITEL Corporation, USA

2.5. LCD (*Liquid Crystal Display*)

Liquid Crystal Display atau LCD merupakan komponen optoelektronik yaitu komponen yang bekerja atau dipengaruhi oleh sinar (optolistrik), komponen pembangkit cahaya (*light emiting*) dan komponen-komponen yang akan mengubah sinar. LCD terbuat dari bahan kristal cair yang merupakan suatu komponen organik dan mempunyai sifat optik seperti benda padat meskipun bahan tetap cair.

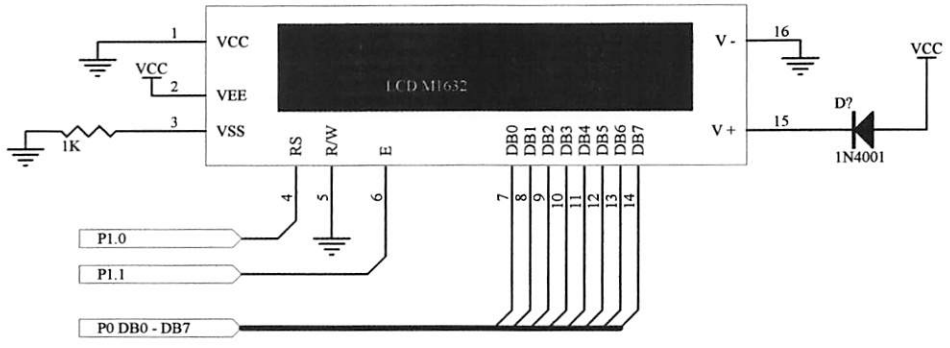
Sel kristal cair terdiri dari selapis bahan kristal cair yang diapit antara dua kaca tipis yang transparan. Antara dua lembar kaca tersebut diberi bahan kristal cair (*liquid crystal)* yang tembus cahaya. Permukaan luar dari masing-masing keping kaca mempunyai lapisan penghantar tembus cahaya seperti oxida timah (*tin oxide)* atau oxida indium (*indium oxide)*. Sel mempunyai ketebalan sekitar 1×10^{-5} meter dan diisi dengan kristal cair.

Karena sel-sel kristal cair merefleksikan cahaya dan bukan membangkitkan cahaya maka konsumsi daya yang dibutuhkan relatif rendah. Energi yang dipergunakan hanya untuk mengaktifkan kristal cair. Pada dasarnya LCD bekerja

pada tegangan rendah (3 – 15 Vrms), frekuensi rendah (25 – 60 Hz) sinyal AC dan memakai arus listrik yang sangat kecil (25 - 300μA). LCD seringkali ditata sebagai tampilan *seven segment* untuk menampilkan angka tetapi juga memiliki keistimewaan lain, yaitu kemampuan untuk menampilkan karakter dan berbagai macam simbol.

Salah satu jenis LCD diantaranya adalah LCD M1632, suatu jenis piranti dengan konsumsi daya yang rendah, disusun dari dot matrik dan dikontrol oleh ROM atau RAM generator karakter dan RAM data display. Pengontrolan utamanya adalah pada ROM generator dan display data RAM yang menghasilkan kode ASCII jika padanya diberikan *input* ASCII. Untuk dapat difungsikan dengan baik maka perlu diperhatikan proses analisasi yang telah ditentukan oleh pabrik pembuatnya. Timing penganalisasian sangat dipertimbangkan, karena jika meleset sampai ordo *milisecon* maka dapat dipastikan LCD tidak dapat berfungsi.

LCD Display Module M1632 buatan Seiko Instrument Inc. ini terdiri dari dua bagian, yang pertama merupakan panel LCD sebagai media penampil informasi dalam bentuk huruf/angka dua baris, masing-masing baris bisa menampung 16 huruf/angka. Bagian kedua merupakan sebuah sistem yang dibentuk dengan mikrokontroler yang ditempelkan dibalik pada panel LCD, berfungsi mengatur tampilan informasi serta berfungsi mengatur komunikasi M1632 dengan mikrokontroler yang memakai tampilan LCD itu. Dengan demikian pemakaian M1632 menjadi sederhana, sistem lain yang M1632 cukup mengirimkan kode-kode ASCII dari informasi yang ditampilkan seperti layaknya memakai sebuah printer.



Gambar 2.14. Rangkaian LCD M1632

Sumber : alds.stts.edu, rubrik analog, STTS Surabaya

Adapun karakteristik dari LCD M1632 antara lain :

- Dengan 16 karakter – 2 baris dalam bentuk dotmatrik 5x7 dan cursor
- *Duty ratio* 1/16
- Memiliki ROM pembangkitan karakter untuk 192 jenis karakter
- RAM untuk data display sebanyak 80x8 *bit*
- Dapat dirangkai dengan MPU 8 *bit*/4 *bit*
- RAM data display dan RAM pembangkit karakter dapat dibaca oleh MPU
- Memiliki fungsi instruksi antara lain *display on/off*, *Cursor on/off*, *display* karakter *blink*, *cursor shift* dan *display shift*
- Memiliki rangkaian osilator sendiri
- Catu tegangan tunggal yaitu ± 5 V
- Memiliki rangkaian *reset* otomatis pada catu daya yang dihidupkan
- Temperatur operasi 0^0 - 50^0

LCD memiliki 16 pin, masing-masing memiliki fungsi sebagai berikut :

Tabel 2.7. Fungsi Tiap Pin LCD

No. Pin	Simbol	Level	Fungsi	
1	V_{SS}	-	*Power* Supply	0 V (GND)
2	V_{CC}	-		5 V ± 10%
3	V_{EE}	-		For LCD Drive
4	RS	H/L	Sinyal seleksi *register* H ; Data *Input* [*register* data (*write/read*)] L ; Instruction *Input* [*register* instruksi (*write*), busy *flag* dan *address counter* (*read*)]	
5	R/W	H/L	H ; *Read* L ; *Write*	
6	E	H	*Enable* Signal [sinyal penanda mulai operasi, aktif saat operasi *write* atau *read*]	
7	DB0	H/L	4 *bit* bus data *lower* 2 arah, dapat dibaca atau ditulis terhadap mikrokontroler	
8	DB1	H/L		
9	DB2	H/L		
10	DB3	H/L		
11	DB4	H/L	4 *bit* bus data upper 2 arah, dapat dibaca atau ditulis terhadap mikrokontroler, DB7 juga sebagai busy *flag*	
12	DB5	H/L		
13	DB6	H/L		
14	DB7	H/L		
15	V+BL	-	Back Light Supply	4 - 4,2 V 50 – 200 mA
16	V-BL	-		0 V (GND)

Sumber: LCD Module M1632 user manual

2.5.1. Instruksi Operasi

Tabel 2.8. Instruksi Pada LCD

Instruksi	RS	RW	D 7	D 6	D 5	*D4*	D3	D2	D1	D 0
Display *Clear*	0	0	0	0	0	0	0	0	0	1
Cursor Home	0	0	0	0	0	0	0	0	1	*
Entry *Mode Set*	0	0	0	0	0	0	0	1	I/D	S
Display On/*Off*	0	0	0	0	0	0	1	D	C	B
Cursor Display Shift	0	0	0	0	0	1	S/C	R/L	*	*
Function *Set*	0	0	0	0	1	DL	1	*	*	*
CG RAM *Address Set*	0	0	0	1	A_{CG}					
DD RAM *Address Set*	0	0	1	A_{DD}						
BF/*Address Read*	0	1	B F	AC						
Data *Write* to CG RAM	1	0	*Write* Data							
Data *Read* from CG RAM	1	1	*Read* Data							

*Invalid *Bit*
A_{CG} ; CG RAM *Address* dan A_{DD}
DD RAM *Address*

Sumber: LCD Module M1632 user manual

Pada LCD juga terdapat instruksi – instruksi sebagai berikut :

1. Display *clear*

   Membersihkan tampilan yang ada pada LCD serta menyimpan, sedangkan kursor kembali ke posisi semula.

2. *Cursor home*

   Hanya membersihkan tampilan dan kursor kembali ke semula.

3. *Empty Mode Set* : layar beraksi sebagai tampilan tulis.

S : 1/0 = menggeser layar.

1/0 : 1 = kursor bergerak ke kanan dan layar bergerak ke kiri.

1/0 : 0 = kursor bergerak ke kiri dan layar bergerak ke kanan

4. *Display On/Off Control.*

   D : 1 = layar *on*

   D : 0 = layar *off*

   C : 1 = kursor *on*

   C : 0 = kursor *off*

   B : 1 = kursor berkedip-kedip

   B : 0 = kursor tidak berkedip – kedip

5. *Cursor Display Shift*

   S/C : 1 = LCD diidentifikasikan sebagai layar

   S/C : 0 = LCD diidentifikasikan sebagai kursor

   R/L : 1 = menggeser satu spasi ke kanan

   R/L : 0 = menggeser satu spasi ke kiri

6. *Fuction Set*

   DL : 1 = panjang data LCD pada 8 *bit*

   DL : 0 = panjang data LCD pada 4 *bit*

   Bit upper ditransfer terlebih dahulu kemudian diikuti dengan 4 *bit lower*.

   N : 1/0 = LCD menggunakan 2 atau 1 baris karakter

   P : 1/0 = LCD menggunakan 5 x 10 dot matrik

7. CG RAM *address set* : menulis alamat RAM ke karakter

8. DD RAM *address set* : menulis alamat RAM ke tampilan

9. BF/*address set* : BF = 1/0, LCD dalam keadaan sibuk atau tidak sibuk.

10. *Data write to* CG RAM *or* DD RAM : membaca *byte* dari alamat terakhir RAM yang dipilih.

2.5.2. Operasi Dasar

- *Register*

  Kontrol dari LCD memiliki 2 buah *register* 8 *bit* yaitu *register* instruksi (IR) dan *register* data (DR). IR memiliki instruksi seperti display, *clear*, cursor shift dan display data (DD RAM) serta karakter (CG RAM). DR menyimpan data untuk ditulis ke DD RAM ataupun membaca data dari DD RAM dan CG RAM. Ketika data ditulis ke DD RAM atau CG RAM maka DR secara otomatis menulis data ke DD RAM atau CG RAM. Ketika data pada CG RAM atau DD RAM akan dibaca maka alamat data ditulis pada IR. Sedangkan data akan dimasukkan melalui DR sehingga dapat dibaca oleh mikrokontroler.

Tabel 2.9. Pemilihan *Register* Pada LCD

RS	RW	Operasi
0	0	Seleksi IR, IR *Write Display Clear*
0	1	*Busy Flag* (DB7), @ *Counter* (DB0-DB7) *Read*
1	0	Seleksi DR, DR *Write*
1	1	Seleksi DR, DR *Read*

Sumber: LCD Module M1632 user manual

- *Busy Flag*

  Busy Flag menunjukkan bahwa modul siap untuk menerima instruksi selanjutnya sebagaimana terlihat pada tabel diatas. *Register* seleksi sinyal

akan melalui DB7 jika RS=0 dan R/W=1. Jika bernilai 1 maka sedang melakukan kerja *internal* dan instruksi tidak akan dapat diterima, oleh karena itu status dari *flag* harus diperiksa sebelum melaksanakan instruksi selanjutnya.

- *Address Counter* (AC)

  AC menunjukkan lokasi memori dalam modul LCD. Pemilihan lokasi alamat lewat Ac diberikan lewat *register* instruksi (IR) ketika data pada A, maka AC secara otomatis menaikkan atau menurunkan alamat tergantung dari Entry *Mode Set*.

- Display Data RAM

  Pada LCD, masing-masing *line* memiliki *range* alamat tersendiri. Alamat itu diekspresikan dengan bilangan hexadesimal. Untuk *line* 1 *range* alamat berkisar antara 40_H-$4F_H$.

- Character Generator ROM (CG ROM)

  CG ROM memiliki tipe dot matrik 5x7, dimana pada LCD telah tersedia ROM sebagai pembangkit karakter dalam kode ASCII.

- Character Generator RAM (CG RAM)

  CG RAM dipakai untuk pembuatan karakter tersendiri melalui program.

2.5.3. Sinyal *Interface* M1632

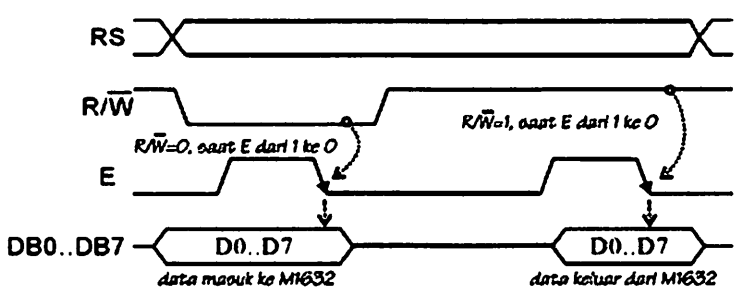
Untuk berhubungan dengan mikrokontroler pemakai, M1632 dilengkapi dengan 8 jalur data (**DB0 - DB7**) yang dipakai untuk menyalurkan kode ASCII maupun perintah pengatur kerjanya M1632. Selain itu dilengkapi pula dengan **E**, **R/W** dan **RS** seperti layaknya komponen yang kompatibel dengan mikroprosesor.

Kombinasi lainnya E dan **R/$\overline{W}$** merupakan sinyal standar pada komponen buatan Motorola. Sebaliknya sinyal-sinyal dari MCS51 merupakan sinyal khas Intel dengan kombinasi sinyal **WR** dan **RD**.

RS, singkatan dari *Register* Select, dipakai untuk membedakan jenis data yang dikirim ke M1632, kalau **RS**=0 data yang dikirim adalah perintah untuk mengatur kerja M1632, sebaliknya kalau **RS**=1 data yang dikirim adalah kode ASCII yang ditampilkan.

Demikian pula saat pengambilan data, saat **RS**=0 data yang diambil dari M1632 merupakan data status yang mewakili aktivitas M1632, dan saat **RS**=1 maka data yang diambil merupakan kode ASCII dari data yang ditampilkan.

Proses mengirim/mengambil data ke/dari M1632 bisa dijabarkan sebagai berikut :



Gambar 2.15. Mengirim/Mengambil Data Ke/Dari M1632

Sumber: alds.stts.edu,rubrik analog, STTS Surabaya

1. **RS** harus dipersiapkan dulu, untuk menentukan jenis data seperti yang telah dibicarakan di atas.
2. **R/$\overline{W}$** di-nol-kan untuk menandakan akan diadakan pengiriman data ke M1632. Data yang akan dikirim disiapkan di **DB0-DB7**, sesaat kemudian

sinyal **E** di-satu-kan dan di-nol-kan kembali. Sinyal **E** merupakan sinyal sinkronisasi, saat E berubah dari 1 menjadi 0 data di **DB0 - DB7** diterima oleh M1632.

3. Untuk mengambil data dari M1632 sinyal **R/$\overline{W}$** di-satu-kan, menyusul sinyal **E** di-satu-kan. Pada saat **E** menjadi 1, M1632 akan meletakkan datanya di DB0 .. DB7, data ini harus diambil sebelum sinyal **E** di-nol-kan kembali.

2.6. *Information storage device* (ISD) 25120

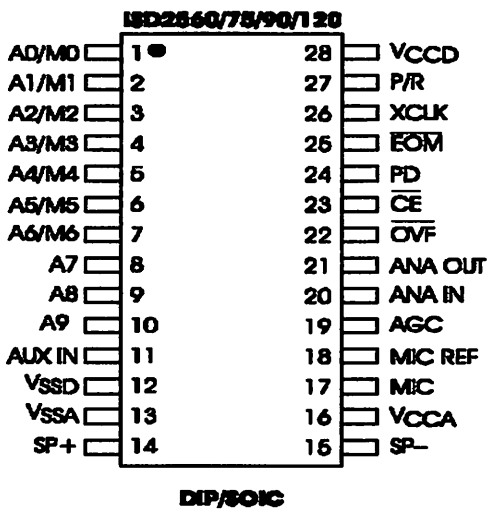
IC penyimpan suara yang digunakan merupakan jenisEEPROM (*Electrically Erasable Programable Read Only Memory*) yaitu ROM yang dapat deprogram, dihapus dan deprogram ulang secara elektrik dengan arus listrik. IC ISD (*Information storage device*) yang dipakai yaitu ISD 25120. IC ini dapat merekam pesan maksimal selama 120 detik dan dapat di kaskade sehingga pesan yang disimpan dapat diperpanjang sesuai dengan keinginan kita dengan alamat yang berbeda.

Didalam ISD 25120 dilengkapi dengan *internal amplifier*, *internal automatic gain control* (AGC), *filter antialiasing* (perata) dan *speaker* amplifier (penguat speaker). Secara keseluruhan seri ISD 25120 dapat melakukan sebuah perekaman atau pemutaran ulang pesan dengan komponen sederhana seperti mikrofon, speaker, beberapa komponen penunjang, dua buah saklar dan sumber tegangan.

Rekaman akan disimpan dalam sel memori yang tidak mudah hilang (*non volatile*). Cara unik ini yang membuat ISD disebut *Direct Analog Storage Technology* (DAST) atau teknik penyimpanan analog langsung, dengan jalan sinyal suara (*voice*) dan bunyi disimpan secara langsung dalam bentuk anaog kedalam

memori EEPROM. Penyimpanan analog langsung memungkinkan reproduksi suara secara alami dalam satu chip tunggal.

Susunan ISD 25120 DAST adalah dikelompokan dalam 160 segmen dari alamt A0 sampai A7 yang menunjukan akses tiap segmen dalam kesatuan untuk alamat pesan. Kemampuan pemberian atau penyediaan alamat yang berupa pesan yang disimpan dalam bentuk kalimat dan suara.



Gambar 2.16. IC ISD 25120

Sumber: *Data Sheet* ISD 25120 *Series*

Berikut adalah konfigurasi pin-pin ISD 25120:

- *Voltage Input* (VCCA, VCCD), untuk mengurangi noise, rangkaian analog dan digital dalam IC ISD2500 digunakan sebagai *power supply* tersendiri dalam pak.
- *Groung Input* (VSSA,VSSD), pin ini harus dihubungkan dalam *power supply ground* dengan impedansi rendah.

- *Power Down Input* (PD), ketika tidak sedang digunakan (*standby*) untuk merekamatau *playback*, pin PD harus diberi logika tinggi. Ketika pulsa *overflow* (OVF) rendah, PD harus dibawa ke logika tinggi untuk me-*reset address pointer* kembali ke awal perekaman atau *playback.*

- *Chip Enable Input* (CE), pin CE diberi logika rendah untuk membolehkan semua operasi perekaman dan *playback.* Alamat input dan *playback/record input* (P/R) ditahan dengan adanya transisi turun dari CE.

- *Playback/Record Input* (P/R), P/R *input* ditahan dengan adanya transisi turun dari pin CE. Logika tinggi akan memilih *playback cycle* dan logika rendah untuk memilih *record cycle.*. Untuk *record cycle,* alamat *input* menetapkan mulainya alamat dan merekam secara kontinyu sampai PD atau CE ke transisi tinggi atau adanya *overflow.* Ketika *record cycle* terhenti dengan adanya transisi tinggi dari PD atau CE, sinyal *End-of-Message* (EOM) disimpan di alamat dan akan memutar suara perekaman sampai alamat EOM ditemukan.

- *End-of-Message Run Output* (EOM), sebuah alamat akan dimasukkan secara otomatis di akhir masing-masing perekaman. Pulsa *output* EOM akan rendah untuk setiap periode dari T_{EOM} diakhir masing-masing perekaman.

- *Microphone Input* (MIC), digunakan untuk mentransfer sinyal suara ke *on-chip preamplifier.* Rangkaian *on-chip Automatic gain Control* (AGC) mengontrol penguatan dari *preamplifier* dari -15 sampai 24B.

- *Microphone Reference Ibput* (MIC REF), adalah *input* pembalik ke *microphonepreamplifire.* Ini untuk memberikan *noise-canceling* atau

common-mode rejection input ke IC ini ketika dihubungkan ke sebuah *microphone* diferensial.

- *Overflow Output* (OVF), sinyal pulsa rendah pada akhir tempat memori, mengindikasikan bahwa IC ini telah terpenuhi dan pesan telah melebihi kapasitas. Keluaran OVF kemudian diikuti masukan CE sampai pulsa PD telah me-*reset*. Pin ini juga dapat untuk menambah beberapa IC 25120 untuk menambah durasi *recrd/playback*.
- *Automatic Gain Control Input* (AGC), AGC secara dinamik mengubah penguatan dari *preanplifire* untuk mengimbangi dari lebar jarak dari level *microphone input.* AGC memberikan jarak secara penuh dari suara rendah ke tinggi untuk direkam dengan distorsi minimal.
- Analog *Output* (ANA OUT), pin ini memberikan *preamplifier output* ke pengguna. Tegangan penguatan dari *preamplifier* ditentukan oleh level tegangan dari pin AGC.
- Analaog *Input* (ANA IN), pin ini akan mentransfer sinyal ke dalam chip untuk perekaman. Untuk *microphe input,* pin ANA OUT harus dihubungkan ke kapasitor eksternal ke pin ANA IN. Jika permintaan *input* diperoleh dari sumber lain darai *microphone,* sinyal ini dapat langsung dikopel oleh kapasitor ke pin ANA IN.
- *External Clock Input* (XCLK), untuk ISD 25120 mempunyaoi sebuah internal *pull-down.* Frekuensi *clock* sampling internal kurang lebih 1& dari spesifikasi. Frekuensi ini bervariasi dari ± 2,25% berada pada suhu kamar dan tegangan kerja. Jika *power supply* yang digunakan mempunyai toleransi ± 5%

pada tempaeratur dan tegangan kerja. Jika *power supply* yang digunakan mempunyai presisi tinggi, maka alat ini dapat di-*clock* langsung pada pin XCLK. *Duty cyle* pada *input clock* tidak perlu dipermasalahkan karena *clock* dengan segera dibagi dua. Jika pin XCLK tidak digunakan, harus dihubungkan ke *ground.*

- *Speaker Output* (SP+/SP-), ISD 25120 telah mempunyai sebuah *driver on-chip* diferensial speaker, sanggup memikul beban 50 mW dalam 16 ohm dari AUX IN. Speaker *output* berada pada level VSSA selama proses *record* dan *power down.*

- *Auxilary Input* (AX/MX), dihubungkan langsung ke kaki keluaran *amplifier* dan keluaran speaker ketika CE, P/R berada pada logika tinggi dan *playback* tidak aktif.

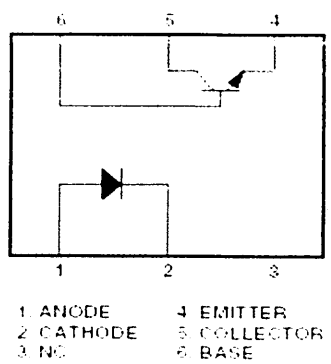
- *Address Mode Input* (AX/MX), mempunyai dua fungsi tergantung pada level dari dua *Most Significant Bit* (MSB) dari alamat tersebut (A_8 dan A_9) . Jika salah satu atau keduanya dari dua MSB berlogika rendah, semua input diaggap sebagai bit alamat dan digunakan sebagai awal alamat untuk proses *record* atau *playback cycle* terbaru. Alamat input ditahan oleh transisi turun dari CE. Jika kedua MSB, berlogika tinggi, *address/mode input* dianggap sebagai bit *mode*.

2.7. *Optocoupler* 4N25

Optocoupler disebut juga optoisolator merupakan gabungan dari LED (pada sisi input) dan Photodioda (pada sisi output) dalam satu kemasan. Fungsi dari

optocoupler adalah mengisolasi antara satu bagian rangkaian dengan bagian rangkaian yang lain. Tujuan dari pengisolasian ini adalah untuk mencegah agar tidak terjadi kerusakan komponen pada suatu bagian sebagai akibat dari munculnya tegangan tinggi yang tidak diinginkan pada bagian lainnya.

Keuntungan pokok dari *optocoupler* adalah terjadinya isolasi elektrik antara satu rangkaian input dan output. Dengan *optocoupler*, hanya terdapat kontak input dan output dalam bentuk pancaran sinar. Oleh karena itu, dimungkinkan untuk mengisolasi resistansi antara dua rangkaian dalam orde ribuan megaohm. Isolasi yang seperti itu berguna dalam aplikasi tegangan tinggi dimana beda potensial dua rangkaian sampai dengan ribuan volt. [Malvino, 2003:171]. Dalam tugas akhir ini digunakan *optocoupler* 4N25 yang dapat mengisolasi tegangan sampai dengan 5300 volt pada sisi photodioda.

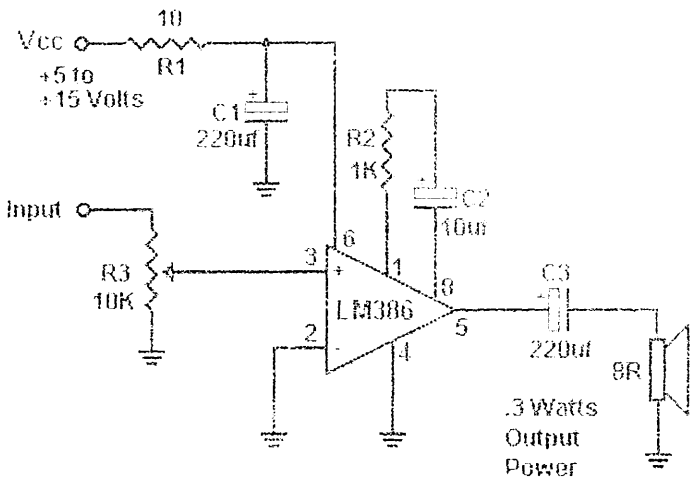


Gambar 2.17. Konfigurasi Pin 4N25

Sumber: Data Sheet 4N25

2.8. *Audio Amplifier* LM 386

IC LM 386 adalah komponen yang digunakan untuk *audio amplifier* dengan penguatan yang dapat diatur dari 20 sampai 200 dengan penambahan sedikit penambahan dari luar.



Gambar 2.18. Rangkaian LM 386

Sumber: data sheet LM386

2.9. Keypad 3 x 4

Untuk mempermudah pengunaan mikrokontroller sebagai alat proses, maka diperlukan sarana yang dapat menjadi penghubung penggunaan dengan alat kontrol, yaitu sebagai sarana input data yang nantinya akan diolah oleh mikrokontroller.

Peralatan input data yang dapat menunjang mikrokontroller adalah beberapa saklar tekan yang menyatakan angka dan karakter yang disusun berbentuk matrik 3 kolom dan 4 baris dengan total tombol 12 buah.

Rangkaian ini dapat dianalogikan dengan tiga buah kabel terbuka yang disilang dengan empat buah kabel yang lain (diletakan diatasnya). Perlakuan ini akan menyebabkan perolehan 12 titik persilangan. Bila pada suatu titik kabel persilangan itu bersentuhan (salah satu ditekan hingga menyentuh kabel yang lain dibawahnya), maka diasumsikan bahwa tombol keypad pada posisi bersilangan tersebut ditekan. Berikut ini adalah gambar konfigurasi tombol Keypad :

1	2	3
4	5	6
7	8	9
*	0	#

Gambar 2.19. Konfigurasi Tombol Keypad

BAB III

PERENCANAAN PERANGKAT KERAS

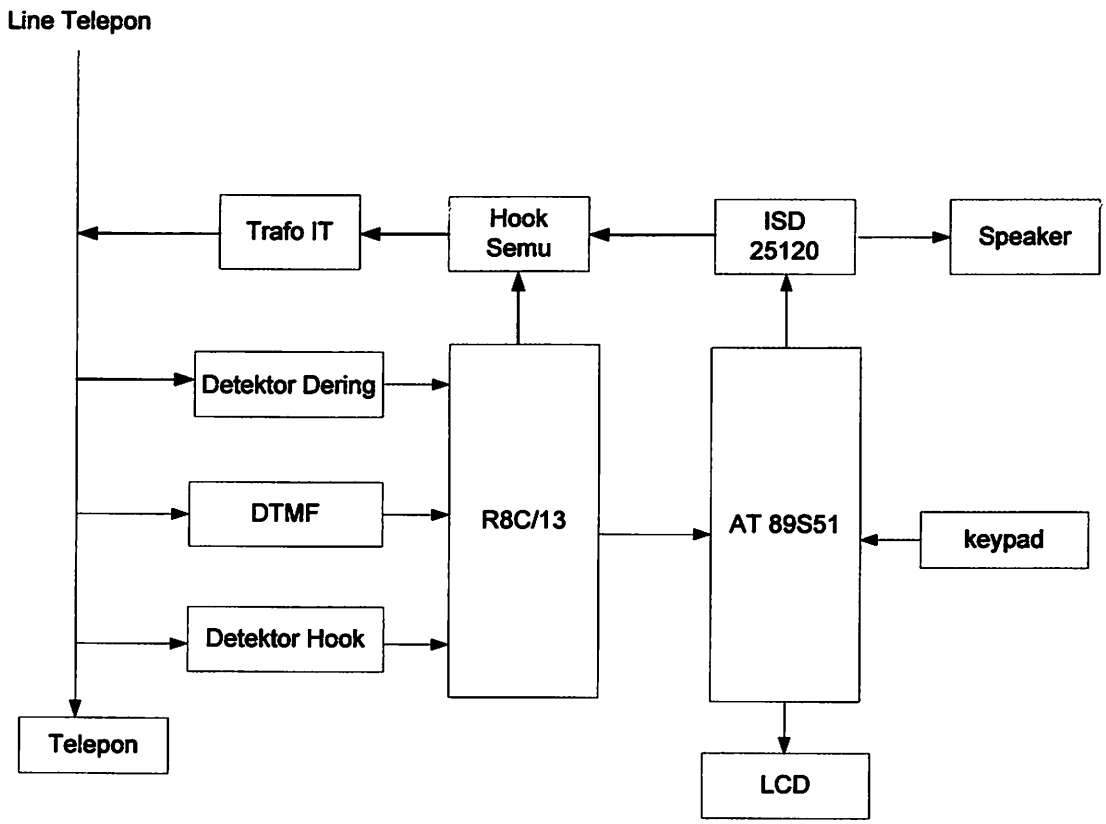
3.1. Umum

Pada bab ini akan dibahas mengenai perencanaan dan pembuatan sistem penerima telepon dan pemanggil otomatis pada rumah kost menggunakan mikrokontroller R8C/13 dan AT89S51. Perencanaan dan pembuatan alat ini secara garis besar dibagi atas dua bagian, yaitu:

1. Perencanaan perangkat keras
2. Perencanaan perangkat lunak

Pada perancangan perangkat keras diperlukan alat atau rangkaian penunjang antara lain rangkaian mikrokontroler Renesas R8C/13 Tiny Series, AT89S51, DTMF MT8870, Detektor Hook, Detektor Dering, ISD 25120, Keypad, dan LCD. Sedangkan perangkat lunak berupa program *software* sebagai pengendali dari cara kerja perangkat keras yang telah direncanakan yang meliputi flowchart software secara umum.

Adapun blok diagram sistem dari alat yang akan dirancang adalah sebagai berikut :



Gambar 3.1. Blok Diagram Sistem

Keterangan blok diagram :

1. ISD

   Komponen utama adalah ISD 25120 yang berfungsi untuk memberitahukan kepada si penelpon untuk menekan nomor orang yang dituju serta untuk melakukan panggilan kepada penghuni kost.

2. DTMF

   Berfungsi mengubah frekuensi tone dari tombol telepon sipenelpon ke dalam kode biner sebagai inputan pada mikrokontroller R8C/13.

3. Detektor dering

   Berfungsi untuk mendeteksi adanya panggilan telepon yang masuk.

4. Detektor Hook

   Berfungsi untuk mendeteksi bahwa orang yang ditelepon telah menerima telepon dan mengangkatnya.

5. Hook Semu

   Merupakan simulasi tutup dan angkat gagang telepon, dimana seolah-olah telepon diangkat oleh sistem pada saat ada panggilan yang masuk.

6. Trafo IT

   Berfungsi sebagai penyesuai impedansi antara sistem dan line telepon.

7. LCD

   Berfungsi sebagai menu tampilan untuk melakukan pengesetan ulang pada ISD

8. Keypad

   Berfungsi sebagai inputan pada sistem untuk melakukan pengesetan pada ISD

Prinsip Kerja Sistem

Prinsip kerja dari alat ini adalah pada saat ada sinyal yang masuk, yang menandakan adanya panggilan ke nomor yang dituju, maka ada sinyal AC yang dikirim dari sentral ke penelpon penerima. Sinyal ini akan dideteksi oleh detektor dering yang kemudian akan mengaktifkan sistem. Mikrokontroller R8C/13 akan mengaktifkan relay (hook semu) sehingga penelpon terhubung dengan beban tiruan yang seolah- olah pesawat telepon yang dituju dalam keadaan diangkat (*off hook*).

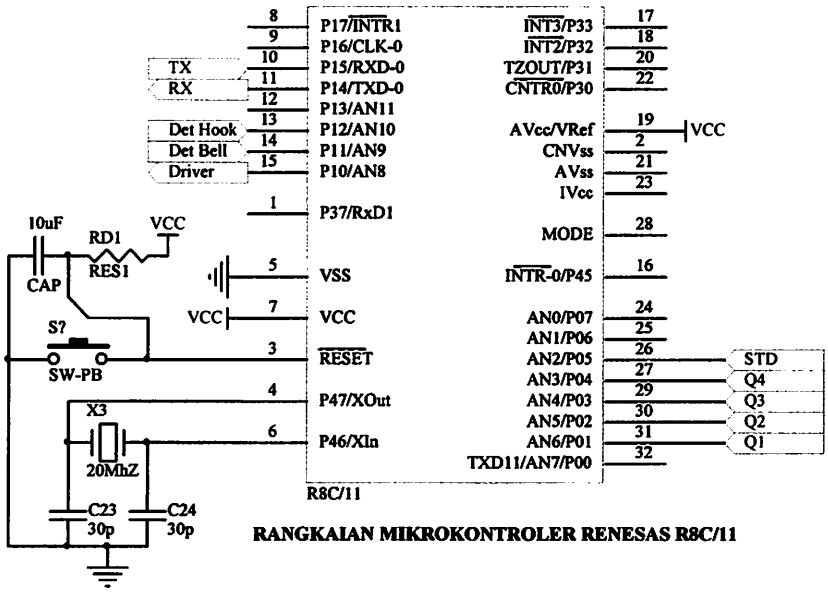
Seiring dengan aktifnya relay ini MCU R8C/13 memberi sinyal masukan pada MCU AT89S51 agar mengaktifkan ISD untuk memberikan menu dan informasi siapa yang ingin dihubungi kepada si penelpon. Misalkan untuk menghubung Hadi maka si penelpon harus menekan tombol 5 pada pesawat teleponnya, kemudian secara otomatis ISD akan melakukan panggilan kepada orang yang dituju.

Saat penelpon menekan tombol pada pesawat teleponnya maka penekanan tersebut menghasilkan nada dengan frekuensi tertentu yang kemudian dikonversi oleh IC DTMF *receiver* menjadi data biner, selanjutnya data tersebut di proses oleh MCU utama (R8C/13) dan kemudian dikirimkan ke MCU kedua (AT89S51). Oleh MCU kedua, data biner tadi digunakan untuk memanggil alamat yang dituju pada ISD. Jika orang yang dihubungi mengangkat telepon maka detektor *hook* akan bekerja dan otomatis memutuskan hubungan penelpon dengan beban tiruan. Sebaliknya, jika sampai beberapa saat telepon tidak diangkat sistem akan kembali memberikan informasi pada penelpon agar melakukan penekanan ulang tombol.

Jika terjadi pergantian penghuni kost, diman ada penghuni baru yang masuk dan penghuni lama yang keluar, maka dengan melakukan penekanan tanda pagar (#) dua kali berturut–turut pada keypad sistem akan mati walaupun ada panggilan telepon yang masuk. Setelah sistem mati, secara otomatis menu pengesetan ISD akan muncul pada LCD , dengan menekan tombol 1 pada keypad untuk melakukan pengesetan nama penghuni pada kamar satu dan seterusnya untuk 0 (nol) pada penghuni kamar 10. Untuk mengaktifkan kembali sistem maka tekan tombol bintang (*).

3.2. Perancangan Perangkat Keras

3.2.1. Mikrokontroller Renesas R8C/13



Gambar 3.2. Rangkaian Mikrokontroller Renesas R8C/13

Mikrokontroller Renesas R8C/13 merupakan mikrokontroller utama yang berfungsi sebagai pengendali sistem. Mikrokontroller ini mempunyai I/O port yaitu P0.0 – P0.7, P1.0 – P1.7, P3.0 – P3.3, P3.7 dan P4.5 sedangkan P4.6 dan P4.7 hanya bisa digunakan sebagai input saja bila konfigurasi ini memakai kristal *internal.* Dalam hal ini yang digunakan port I/O saj, nerikut adalah konfigurasi pin-pin mikrokontroller utama:

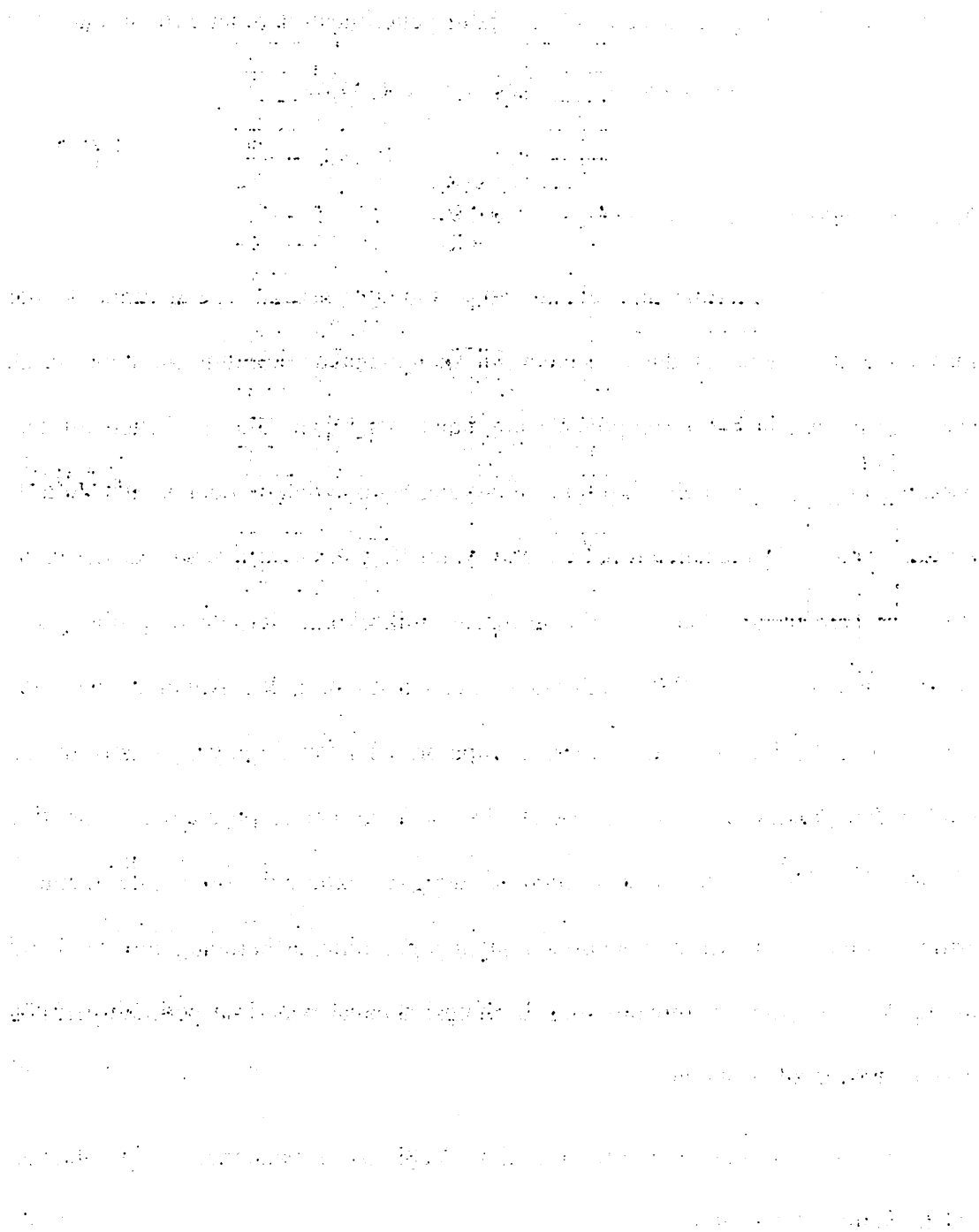
- P0.0 – P0.4 digunakan sebagai masukan rangkaian penerima DTMF MT8870.
- P1.1 digunakan sebagai masukan rangkaian detektor bel.
- P1.2 berfungsi sebagai inputan rangkaian detektor hook.
- P1.0 digunakan sebagai jalur kontrol penggerak relay.

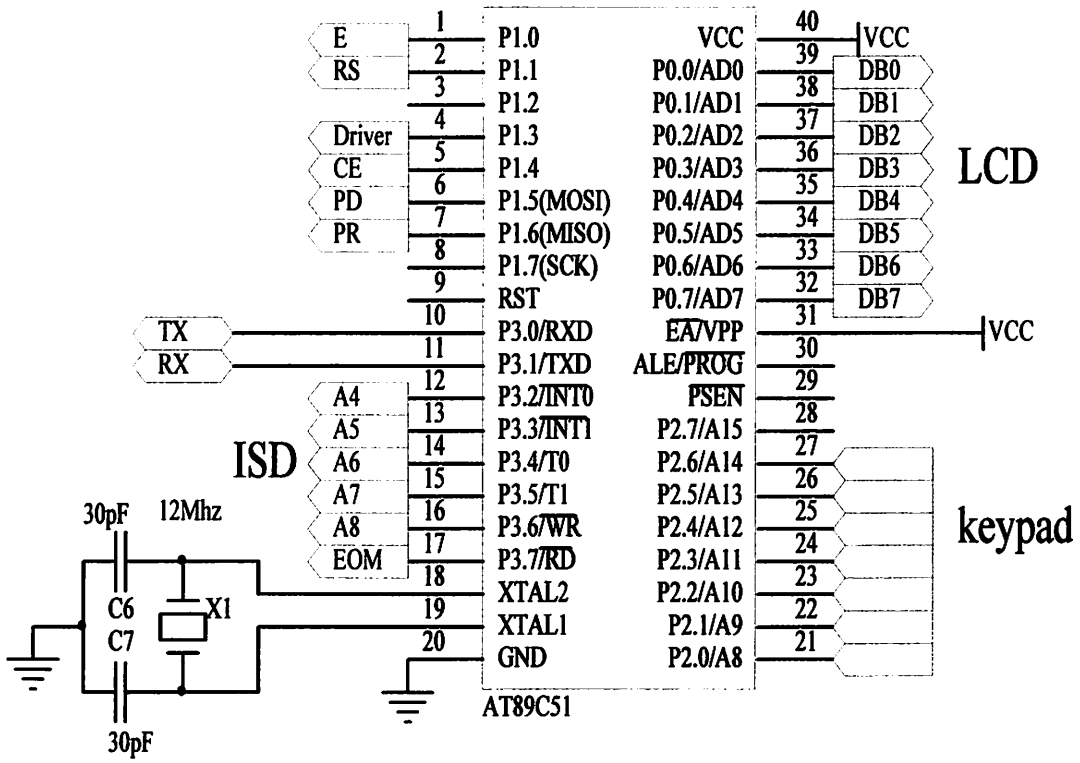
- P1.4 dan P1.5 digunakan sebagai jalur penerimaan dan pengiriman data dari mikrokontroller utama kemikrokontroller pembantu.

3.2.2. mikrokontroller AT 89S51

AT89S51 merupakan sebuah chip tunggal sebagai pengaturan keluar masuknya data. Karena dalam sistem ini menggunakan komunikasi data serial, sehingga harus ada suatu komponen yang dapat mengubah data serial menjadi data paralel untuk diproses oleh mikrokontroller yang bekerja dalam data paralel. Ada IC khusus yang dapat menangani hal tersebut yaitu IC UART (Universal Asyncronous Receiver Transmitter). Dalam berbagai macam mikrokontroller ada yang dilengkapi UART diantaranya AT89S51. Alasan menggunakan produksi Atmel dengan tipe AT89S51 adalah karena mudah diperoleh dipasaran dengan harga yang relatif murah, mudah dan praktis dalam pemrograman karena mempunyai program memori tipe EEPROM. AT89S51 merupakan memori dengan teknologi nonvolatile memori, artinya isi memori tersebut dapat diisi ulang ataupun dihapus berulang kali. MCU ini merupakan rangkaian pembantu yang berfungsi sebagai penerima perintah-perintah dari mikrokontroller utama.

Rangkaian sistem mikrokontroller AT89S51 sebagaimana diperlihatkan dalam gambar di bawah ini:





Gambar 3.3. Rangkaian Mikrokontroller AT89S51

Mikrokontroller AT89S51 digunakan sebagai MCU kedua yang mengontrol masukan dan keluaran data dalam sistem informasi ini adalah sebagai berikut:

- Port 0, (D0 – D7) berfungsi sebagai output dari mikrokontroler yang dihubungkan ke LCD untuk menampilkan data berupa daftar kamar dari kamar 1 sampai kamar 10.
- Pin P1.0 berfungsi sebagai outputan dari Mikrokontroller keLCD untuk operasi awal yang mengaktifkan data tulis atau baca.
- Pin P1.1 berfungsi untuk melakukan pemilihan register pada LCD, dimana sinyal low adalah tulis dan sinyal high adalah baca.

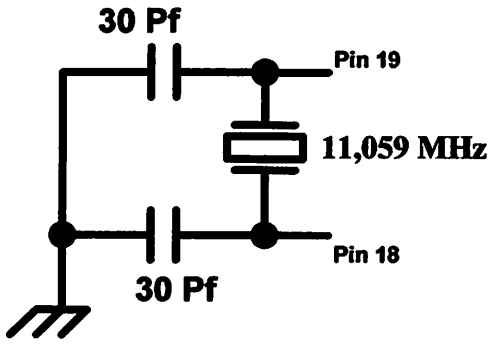
- Pin P1.4 memberikan pulsa pada pin CE (*chip* enable) ISD.
- Pin 1.5 memberikan pulsa pada pin PD (*Power Down Input*) pad ISD.
- Pin 1.6 memberikan pulsa pada pin P/R (*Playback/Record*) ISD.
- Pin P3.0 (RX) dan P3.1 (TX) merupakan pin koneksi untuk komunikasi serial dengan mikrokontroller utama.
- Pin P3.2 – P3.6 berfungsi sebagai kontrol *address* ISD.
- Pin P3.7 berfungsi sebagai kontrol EOM (*End-of-Message*) pada ISD.
- Pin 2.0 – 2.6 merupakan inputan untuk keypad .

3.2.3. Perencanaan Clock

Kecepatan proses pengolahan data pada mikrokontroller ditentukan oleh clock (pewaktu) yang dikendalikan oleh mikrokontroller tersebut. Pada mikrokontroller AT89S51 terdapat internal clock. Internal clock generator berfungsi sebagai sumber clock, tapi masih memerlukan rangkaian tambahan untuk membangkitkan clock yang diperlukan. Rangkaian clock ini terdiri dari dua buah kapasitor dan sebuah kristal yang dirangkai sedemikian rupa dan kemudian dihubungkan dengan Pin 18 dan 19 pada AT 89S51.

Dalam perancangan rangkaian ini menggunakan.

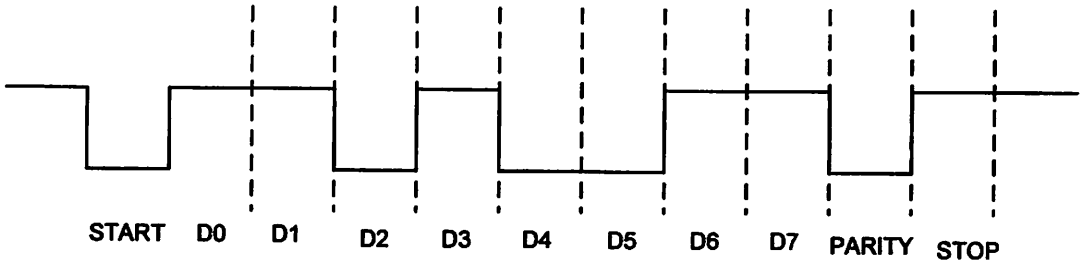
1. C = 30 ρF.Penentuan besarnya kapasitansi disesuaikan dengan spesifikasi pada data sheet AT 89S51.
2. Kristal 11,059 MHz digunakan untuk mensikronisasi hubungan dengan R8C/13. Adapun gambar rangkaian clock tampak seperti pada gambar 3-3.



Gambar 3.4 Rangkaian Clock Minimum Sistem

3.2.4. Komunikasi Serial

Pada perancangan, komunikasi serial antar mikro yang digunakan adalah komunikasi serial asinkron, yaitu dengan menetapkan kecepatan bit dan menyisipkan beberapa bit protocol yaitu START, PARITY bit dan STOP seperti pada gambar.



Gambar 3.5 Format Serial Asinkron

- Kecepatan bit disebut sebagai baud rate atau pesat bit, disingkat bps (bit persecond), pada standart komunikasi serial diantaranya adalah 1200, 4800, 9600 bps. Makin besar pesat bit, makin cepat data ditransmisikan. Dalam perencanaan ini baud rate yang dipakai adalah 9600.

- Saluran tanpa data berlogika high '1', START bit selebar 1 pulsa dan selalu berlogika low '0'.
- Setelah bit START, diikuti serial data, dan terdapat 8 bit data.
- Setelah data-data dapat diikuti (jika diperlukan) oleh PARITY bit, jika PARITY EVEN maka bit PARITY akan menggenapkan jumalah bit '1' nya. Jika dipilih PARITY ODD maka bit PARITY akan mengganjilkan jumlah bit '1' nya.
- Akhir data adalah STOP bit, yang selalu berlogika '1', dapat 1 atau 2 pulsa lebarnya
- Setelah itu jalur kembali '1' untuk siap dilalui oleh data lain.

Notasi format data untuk komunikasi serial pada perencanaan ini adalah sebagai berikut; 9600, 8, 1, N , artinya pesat bit adalah 9600 bps, START bit tidak ditulis karena lebar pulsa selalu 1, 8 bit data, 1 STOP bit dan tidak ada PARITY.

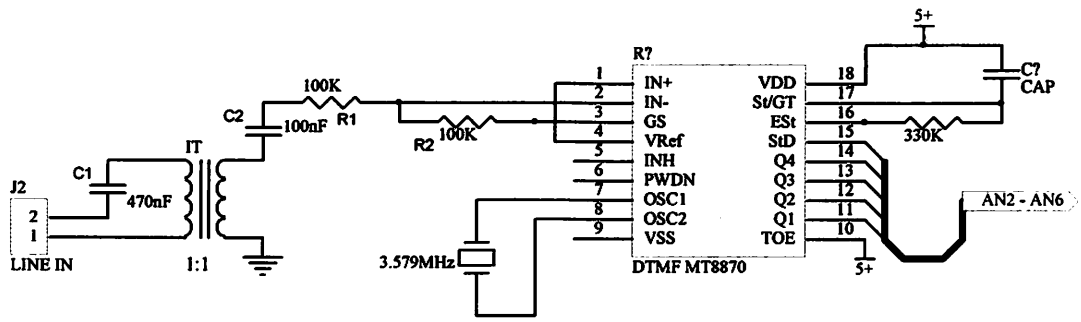
Dipenerima Tx yaitu Rx, harus mengetahui format data yang dikirimkan oleh Tx, begitu ada tegangan drop dari '1' ke '0' mengindikasikan START bit, Tx segera melakukan sinkronisasi sendiri dengan waktu yang telah disepakati bersama yitu 9600 bps. Pada penggunaan 9600 bps, Tx akan mengetahu bahwa setelah 10,42 ms setelah START bit adalah D0, 10,42 ms setelah D0 adalah D1 dan seterusnya hingga D7, PARITY bit dan STOP bit. 10,42 ms diperoleh dari hasil bagi 1 dengan baud rate yaitu 9600 bps. Penggunaan parity adalah untuk mengecek kesalahan dalam pengiriman data, seandainya data yang dikirim tidak sesuai maka dilakukan pengiriman ulang.

3.2.5. Rangkaian DTMF MT8870

Rangkaian DTMF *Receiver* digunakan untuk mendekode sinyal-sinyal DTMF menjadi kode biner 4-bit. Dalam perencanaan ini dipilih rangkaian dekoder yang menggunakan IC MT8870 dari MITEL karena hanya memerlukan rangkaian eksternal yang sedikit. Pada MT8870 terdapat XTAL 3.95 MHz, kapasitor C5 sebesar 100nF yang digunakan sebagai filter untuk menentukan waktu minimal dalam mengenali nada DTMF yang diterima, rangkaian penguat sinyal masukan dibentuk dengan sebuah kapasitor C6 sebesar 100nF dan dua buah resistor R4, R5 masing-masing sebesar 100KΩ.

IC ini menghasilkan kode biner hasil terjemahan dari sinyal DTMF yang masuk. Rangkaian ini menggunakan osilator kristal 3,95 MHz sebagai *clock*nya. Sebagai sinyal pengaktif IC ini digunakan TOE, apabila dalam kondisi *low* maka IC akan mempunyai impedansi yang tinggi pada *output*nya, sedangkan pada saat TOE dalam kondisi *high* maka IC akan aktif dan akan menterjemahkan sinyal DTMF yang masuk. Sedangkan *input* dimasukkan pada *input inverting* dengan penguatan satu kali, hal ini dapat diketahui dari nilai Rin dan Rf yang dimasukkan ke pin GS sebagai feed back. Sebagai indikator adanya sinyal yang masuk maka StD akan berlogika *high* dan data biner 4- bit akan keluar dari IC ini, dan *low* bila tidak ada sinyal yang masuk sehingga sinyal *output* akan terkunci dan data tidak akan keluar dari pin Q0-Q3. Data biner ini merupakan masukan ke mikrokontroler.

Sebagai *interface* antara saluran telepon dengan rangkaian yang ada dalam sistem ini digunakan sebuah transformator (IT) agar sinyal DC yang tidak diharapkan tidak ikut masuk dan juga sebagai penyesuai impedansi



Gambar 3.6 Perencanaan Rangkaian DTMF MT8870

Dipilih penguatan tegangan satu kali dengan mengatur kombinasi R1 dan R2. Dengan R2 = Rf dan R1 = Rin. Pengaturan penguatan dapat dilakukan dengan persamaan :

$$Av = R_F / R_{IN} \qquad (3\text{-}3)$$

$$= 100K/100K$$

$$= 1$$

Resistor R_3 dihubungkan antara penyemat EST dan penyemat St/GT, sedangkan C_3 dihubungkan pada penyemat St/GT dan penyemat T_{OE}. Kedua komponen ini digunakan untuk menentukan waktu tunda saat kombinasi nada DTMF diterima hingga dikeluarkan dalam bentuk bilangan biner 4 bit. Nilai R_{13} adalah 390 KΩ sedangkan nilai C_5 adalah 100 nF [Mitel. 1993:4-16]. Waktu yang diperlukan oleh penerima nada DTMF untuk mendeteksi adanya nada DTMF yang baru (T_{GTP}) (*Guard Time Tone Present*), dapat ditentukan dengan [Mitel. 1993:4-16]:

$$T_{GTP} = (R_{13} \cdot C_5) \ln \left(\frac{V_{DD}}{V_{DD} - V_{TSt}} \right) \qquad (3.11)$$

Nilai V_{TSt} minimal adalah 2,2 V [Mitel. 1993:4-17] maka nilai T_{GTP} minimal dapat ditentukan dengan menggunakan Persamaan (3.11), yaitu:

$$T_{GTPmin} = (390.10^3 . 100.10^{-9}) \ln\left(\frac{5}{5-2,2}\right)$$

$$= 22,613 \text{ ms}$$

Nilai V_{TSt} maksimal adalah 2,5 V [Mitel. 1993:4-17] maka nilai T_{GTP} maksimal dapat ditentukan dengan menggunakan Persamaan (3.11), yaitu:

$$T_{GTPmax} = (390.10^3 . 100.10^{-9}) \ln\left(\frac{5}{5-2,5}\right)$$

$$= 27,033 \text{ ms}$$

Waktu antara yang diperlukan untuk mendeteksi bahwa nada yang ditekan telah dilepaskan (T_{GTA}) *(Guard Time Tone Absent)* dapat ditentukan dengan [Mitel. 1993:4-16]:

$$T_{GTA} = (R_{13}. C_5) \ln\left(\frac{V_{DD}}{V_{TSt}}\right) \quad \text{..... (3.12)}$$

Maka nilai T_{GTA} minimal dapat ditentukan dengan menggunakan Persamaan (3.12), yaitu:

$$T_{GTAmin} = (390.10^3 . 100.10^{-9}) \ln\left(\frac{5}{2,2}\right)$$

$$= 32,018 \text{ ms}$$

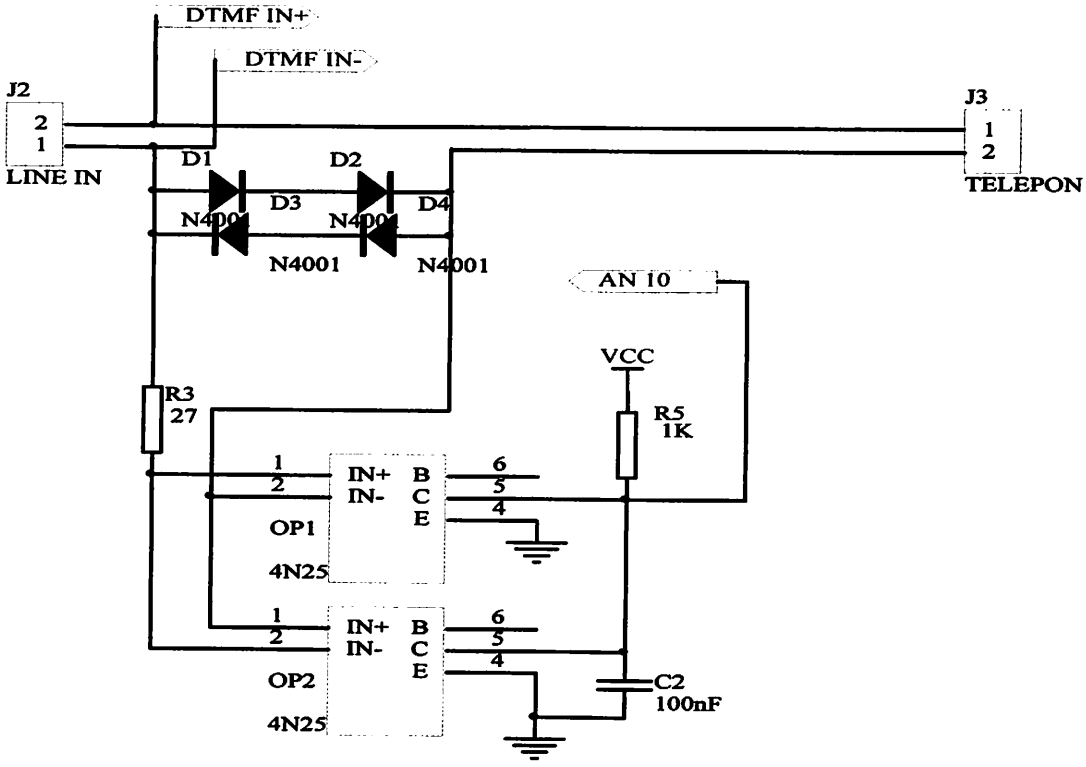
Sedangkan nilai T_{GTA} maksimal dapat ditentukan dengan menggunakan Persamaan (4.12), yaitu:

$$T_{GTAmax} = (390.10^3 . 100.10^{-9}) \ln\left(\frac{5}{2,5}\right)$$

$$= 27,033 \text{ ms}$$

3.2.6. Detektor *Hook*

Rangkaian detektor *hook serial* berfungsi untuk mendeteksi keadaan *handset* pada pesawat telepon sendiri, apakah dalam keadaan diangkat (*off-hook*) atau ditutup (*on-hook*). Pendeteksian keadaan tersebut berdasarkan pada tegangan di saluran. Pada saat *handset* diletakkan, tegangan pada saluran sebesar 48V tegangan searah dan tidak ada arus yang mengalir. Sedangkan apabila *handset* diangkat tegangan pada saluran telepon menjadi 7 - 9V tegangan searah dan arus yang mengalir adalah 16-20mA.



Gambar 3.7 Rangkaian Detektor Hook

Saat *handset* ditutup (*on-hook*) maka sentral telepon dan pelanggan menjadi *loop* terbuka. Pada keadaan ini tidak ada arus listrik yang mengalir sehingga LED pada *optocoupler* (4N25) yang berfungsi untuk mengaktifkan *fototransistor* tidak

menyala. *Fototransistor* yang tidak terbias ini mengakibatkan arus listrik tidak mengalir ke *ground* sehingga tegangan pada *port* sama dengan V_{CC}. Keadaan ini oleh Mikrokontroller akan dideteksi sebagai logika tinggi.

Sebaliknya pada saat *handset* diangkat maka sentral dan pelanggan menjadi *loop* tertutup. LED pada *optocoupler* (4N25) akan menyala dan mengaktifkan *fatotransistor*, sehingga arus listrik akan mengalir dari kolektor ke emitor. Akibatnya tegangan pada *port* sama dengan tegangan pada *ground*, hal ini dideteksi oleh Mikrokontroller sebagai keadaan logika rendah.

Dengan menganggap diode sebagai saklar yang diseri dengan sumber tegangan [Malvino. 1995:42], dapat ditentukan nilai tegangan pada resistor R_3. Sesuai dengan Hukum Kirchoff ke-2 yang menyatakan bahwa jumlah aljabar semua tegangan pada loop tertutup adalah nol, maka :

$$V_{loop} = 2V_{diode} + V_{LED} + V_{res} \quad (3.1)$$

Dengan menganggap diode silikon mempunyai tegangan 0,7V dan LED optocoupler mempunyai tegangan 1,15V [Motorola. 1995:2], maka :

$$V_{res} = (1{,}4 - 1{,}15)V$$

$$= 0{,}25V$$

Karena LED optocoupler mempunyai arus kerja sebesar 10mA [Motorola. 1998:2], dengan menggunakan Hukum Ohm diperoleh nilai resistansi R_3, sebesar:

$$R_3 = \frac{V_{res}}{I} \quad (3.2)$$

$$= \frac{0{,}25V}{0{,}01A}$$

$$= 25\Omega$$

Karena keterbatasan nilai Resistansi resistor yang ada di pasaran maka ditentukan nilai R_3 yang mendekati yaitu 27Ω.

3.2.7. LCD M1632

LCD (*Liquid Crystal Display*) digunakan sebagai tampilan menu untuk pengesetan suara. Sinyal-sinyal yang dipergunakan oleh LCD adalah data bus, RS, R/W dan E. Sinyal E dihubungkan ke P1.1 untuk mengaktifkan LCD. LCD akan aktif jika mikrokontroller AT89S51 memberikan instruksi tulis pada alamat LCD. Sedangkan P1.0 dipergunakan untuk memberikan sinyal RS yang membedakan data yang diberikan pada LCD. Sinyal RS diberikan ke LCD untuk membedakan sinyal antara instruksi program atau instruksi penulisan data. Untuk pin R/W akan berlogika *low* (0) apabila dihubungkan dengan *ground* maka LCD difungsikan hanya untuk menuliskan program atau data ke display. Untuk mengambil data dari mikrokontroler maka pin data DB0-DB7 dari IC ini dihubungkan dengan P0.0 – P0.7 yang merupakan pin data dari mikrokontroller AT89S51.

VR9 pada pin 3 (VEE) digunakan untuk mengatur contras dari karakter yang ditampilkan, sedangkan pin 15 (V+) diberi dioda gunanya agar tegangan yang masuk sesuai dengan data datasheet yaitu 4,5 V

Tegangan dioda = 0,6 V

VCC = 5 V

Jadi tegangan masuk = 5V – 0,6V

= 4,4 Volt

Pada lembaran *data sheet* modul LCD M1632 SEIKO INSTRUMENT INC. disebutkan bahwa :

Power suppluy LCD meliputi :

Vss = 0 V

Vcc = 5 V ± 10 % (2 mA)

Vee = Vcc – 13,5 V sampai Vcc = 0,3 V (1 mA pada Vee = 0,25 V)

Power suppluy Back Light :

V + BL = 4 V sampai 4,2 V (50 sampai 200 mA)

V – BL = 0 V (GND)

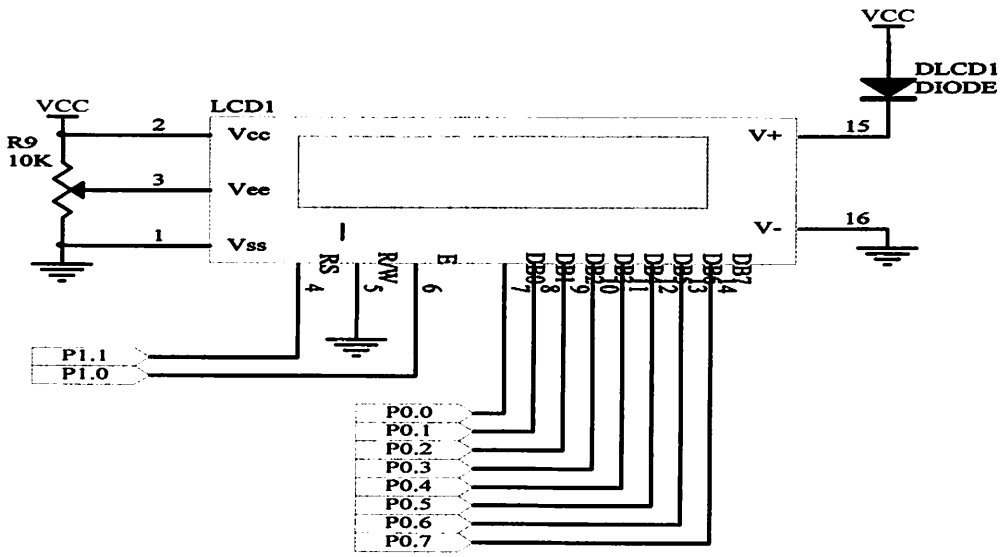
Pada input V + BL dipasang sebuah dioda 1N4001 (bahan silicon dengan Vd = 0,65 V sampai 0,7 V). Tujuannya adalah didapatkan tegangan V+ BL sebesar 4,3 V dengan perhitungan sebagai berikut :

$$Vcc = Vd + (V + BL)$$

$$= 0{,}7 + (V + BL)$$

$$(v + BL) = 5 - 0{,}7 = 4{,}3 \text{ Volt}$$

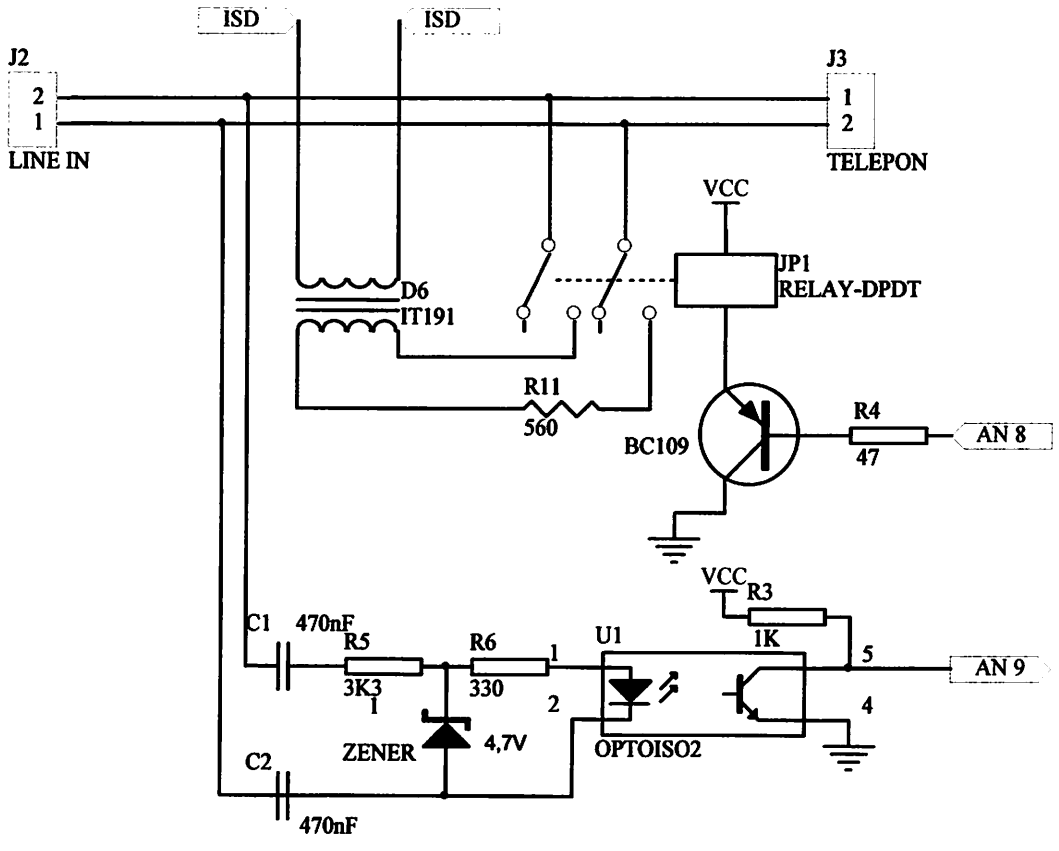
Dipilih dioda 1N4001 karena arus maksimum yang bias dilewatkan oleh dioda ini sebesar 1 A, berikut ini adalah rangkaian lengkap modul LCD yang digunakan dalam perancangan.



Gambar 3.8 Rangkaian LCD M1632

3.2.8. Detektor Dering

Rangkaian detektor dering berfungsi untuk mendeteksi adanya sambungan telepon yang masuk pada rangkaian telepon. Pada saat ada sinyal dering yang masuk, sinyal dering yang berupa sinyal AC ini kemudian dilewatkan melalui kapasitor dan resistor untuk mengaktifkan led pada *optocoupler*, jika led aktif maka optotransistor aktif dan memberi sinyal trigger pada pin P1.1 R8C/13 setelah ada satu kali sinyal yang masuk sehingga sistem aktif.



Gambar 3.9. Rangkaian Detektor Dering

Pada saat sinyal dering masuk, tegangan bisa mencapai 120 Vac. *Optocoupler* 4N25 mempunyai arus led maksimum sebesar 60 mA. Dalam hal ini led dibatasi sampai dengan 2 mA. Batas kemampuan arus zener maksimum dapat ditentukan dengan [Malvino. 1995:85]:

$$I_{ZM} = \frac{P_{ZM}}{V_Z} \quad \text{.....(3.3)}$$

dengan ketentuan sebagai berikut:

P_{ZM} : batas kemampuan daya zener maksimum (watt)

V_Z : tegangan zener (volt)

Karena batas kemampuan daya *zener* maksimum adalah 400 mW dan tegangan zenernya adalah 4,7V [Anonymous. 1993:251] maka batas kemampuan arus maksimum dapat ditentukan dengan menggunakan Persamaan (3.3), yaitu:

$$I_{ZM} = \frac{0{,}4W}{4{,}7V}$$

$$= 85{,}1 \text{ mA}$$

Sehingga nilai resistansi (R_5) dapat ditentukan dengan [Malvino. 1995:84]:

$$R_5 = \frac{V_S - V_Z}{I_S} \quad \text{.....(3.4)}$$

dengan ketentuan sebagai berikut:

V_S : tegangan sumber (volt)

I_S : arus yang mengalir (ampere)

Tegangan efektif bel adalah 90 V, sedangkan nilai tegangan maksimal dapat ditentukan dengan [Malvino. 1995:59]:

$$V_{MAX} = V_{EFEKTIF} . \sqrt{2} \quad \text{.....(3.5)}$$

$$= 90V . \sqrt{2}$$

$$= 127{,}28 \text{ V}$$

Tegangan maksimal bel ini merupakan tegangan sumber (V_S) bagi rangkaian. Arus (I_S) yang direncanakan adalah 35 mA. Sehingga resistansi (R_5) dapat ditentukan dengan menggunakan Persamaan (3.4), yaitu:

$$R_5 = \frac{(127{,}28 - 4{,}7)V}{(35.10^{-3})A}$$

$$= 3502{,}29 \ \Omega$$

Karena keterbatasan nilai komponen resistor yang ada di pasaran maka dipilih R_5 ke nilai yang terdekat yaitu 3,3 KΩ.

Kapasitor penggandeng dalam Gambar 3.8. berfungsi untuk meloloskan sinyal ac dan menahan sinyal dc. Impedansi total yang diperoleh dari hasil pengukuran adalah 15 KΩ maka nilai kapasitor penggandeng dapat ditentukan.

$$X_C = \frac{1}{2\pi.f.C} \quad \text{.....(3.6)}$$

$$C = \frac{1}{2\pi.50.15.10^3}$$

$$C = 212{,}314 \text{ nF}$$

Karena kapasitor terdiri atas dua buah kapasitor bernilai sama yang dipasang seri, maka besarnya dapat ditentukan dengan :

$$C = \frac{C1.C2}{C1+C2} \quad \text{.....(3.7)}$$

$$C_{1\cdot2} = 2C$$

$$= 424{,}628 \text{ nF}$$

Karena keterbatasan nilai komponen yang ada di pasaran maka dipilih C_1 dan C_2 ke nilai yang terdekat yaitu 470 nF.

Arus maju dioda cahaya (I_F) yang direncanakan 10 mA. Pada arus sebesar ini, tegangan maju dioda cahaya (V_F) adalah 1,15 V [Motorola. 1999:1-2]. Nilai komponen R_6 dapat ditentukan dengan:

$$R_6 = \frac{V - V_F}{I_F} \quad \text{.....(3.8)}$$

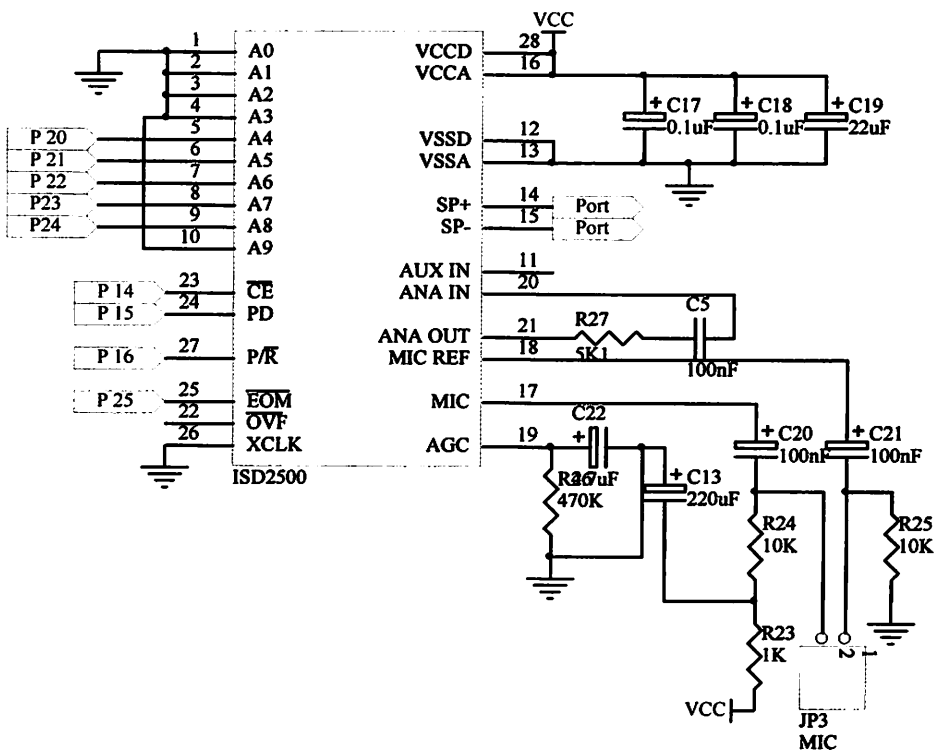
$$= \frac{(4{,}7 - 1{,}15)V}{10.10^{-3}A}$$

$= 355\ \Omega$

karena keterbatasan nilai resistor yang ada di pasaran maka dipilih R_6 ke nilai yang lebih kecil terdekat yaitu 330Ω.

3.2.9. IC Voice/Perekam ISD 25120

Peralatan penyimpan informasi suara, ISD 25120 mempunyai kualitas yang bagus, dengan durasi penyimpanan 120 detik Rangkaian alat dapat dilihat pada Gambar 3.9 di bawah ini:



Gambar 3.10 Rangkaian ISD 25120

Peralatan CMOS yang ada didalamnya adalah *chip oscillator, microphone preamplifier, automatic gain control, antialiasing filter, smouthing filter,* dan *speaker amplifier.* ISD 25120 adalah kompatibel dengan mikrokontroler. Alamat

dan jalur kendali dapat di hubungkan dengan mikrokontroler, sehingga mengijinkan penyimpanan dan pengalamatan yang komplek. Perekaman disimpan dalam suatu *chip* yang tidak mudah berubah dalam *cell* memori. Sinyal suara audio disimpan secara langsung ke memory pada tempat naturalnya dengan kualitas suara yang bagus.

Pin *address* data menerima masukan 5 bit dari mikrokontroller kedua pada port 2 (P2.0 –P2.4) untuk ISD. Alamat- alamat ini akan memilih data suara mana yang akan dipanggil. Kemudian untuk pin *Chip Enable* (CE) berfungsi sebagai pengktifan

Proses perekaman pada ISD 25120 adalah sebagai berikut:

1. Pin *Chip Enable* (CE) pada pin 23 diberi logika *low*.
2. memberiakn alamat dengan mengatur DIP *switch.*
3. Pin *Playback/ Record* pada pin 27 mendapat logika *low*.
4. perekaman dimulai dengan memasukan data suara pada mikrofon.
5. Pin *Playback/ Record* mendapat logika *high* kembali.
6. Mencari alamat terakhir yang ditandai pada *End Of Message* (EOM) terjadi pulsa *low* sesaat kemudian *high* kembali.
7. Demikian seterusnya, untuk melanjutkan perekaman alamat terakhir dari sebelumnya diberikan spasi dan memulai perekaman kembali sampai pada batas waktu dari kemampuan ISD.

Kemudian untuk prosedur pemanggilan data-data suara yang telah direkam adalah sebagai berikut:

1. Pin *Chip Enable* (CE) pada pin 23 diberi logika *low*.

2. Memanggil alamat suara yang diinginkan, pada waktu perekaman tadi.
3. Kemudian memberikan logika *high* pada *Playback/ Record* pin 27 yang berarti pemanggilan suara dimulai.
4. Menunggu *End Of Message* (EOM) terdapat pulsa *low* sesaat.
5. Bila sudah terdapat nilai pulsa *low* sesaat pada EOM, segera diberikan logika *high* pada pin CE, ini menandakan akhir dari data suara pada alamat tersebut.
6. demikian seterusnya pada alamat-alamat selanjutnya, sesuai dengan data suara yang diinginkan.

Berikut adalah data-data suara dan alamat-alamatnya yang telah direkam dengan lebar data 5 bit.

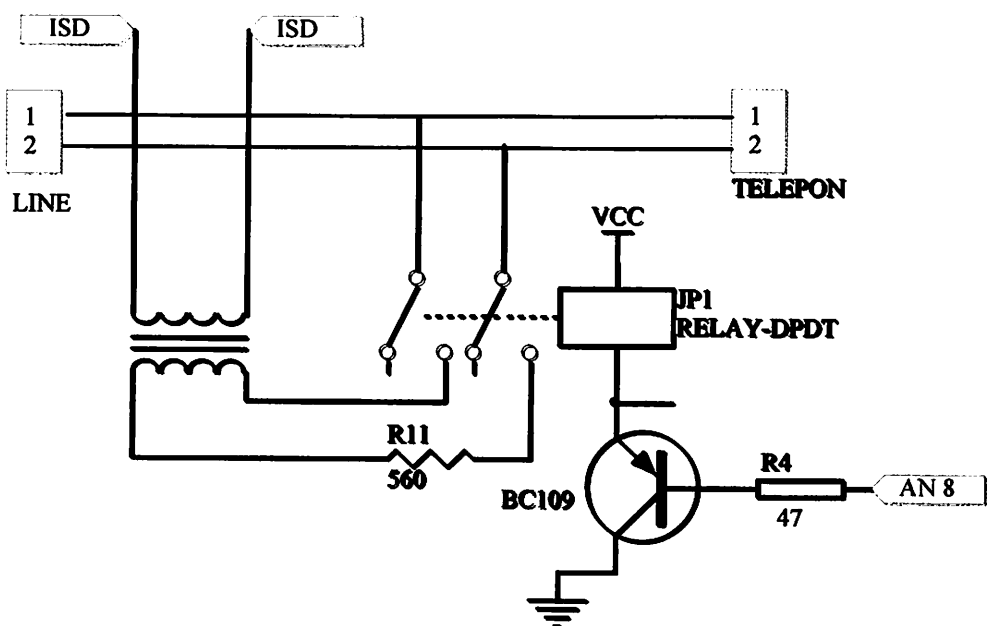
Tabel 3.1 Data Perekaman Suara pada ISD

No.	Data Suara ISD
1.	"Selamat datang dilayanan pemanggil otomatis silahkan tekan 0 sampai dengan 9 untuk melakukan pemanggilan"
2.	"Nol"
3.	"Satu"
4.	"Dua"
5.	"Tiga"
6.	"Empat"
7.	"Lima"
8.	"Enam"
9.	"Tujuh"
10.	"Delapan"
11.	"Sembilan"
12.	"Untuk"
13.	"Ada Telepon"
14.	"Andi"
15.	"Budi"
16.	"Azmi"
17.	"Yuda"
18.	"Imam"

19.	"Wira"
20.	"Deni"
21.	"Noval"
22.	"Rio"
23.	"Doni"
24.	"Tekan bintang untuk kembali ke awal"
25.	"Maaf orang yang anda panggil sedang keluar"

3.2.10. Perencanaan Driver Relay

Relay digunakan untuk menyambung dan memutus simulasi angkat telepon dengan beban tiruan dan memutus hubungan peasawat telepon dengan sentral pada saat pengesetan ulang ISD yang dikontrol oleh mikrokontroller Renesas R8C/13. Pada perencanaan digunakan relay jenis DPDT *(Dual Pole Dual Totem)* yang mempunyai resistansi sebesar 170 Ω dan bekerja pada tegangan catu sebesar +5 volt. Rangkaian ini digerakkan oleh transistor jenis BC 109 dengan β sebesar 250 dan V_{CE} dalam keadaan jenuh sebesar 0,2 volt.



Gambar 3.11. Rangkaian Driver Relay

Untuk perencanaan driver relay adalah sebagai berikut:

Besarnya arus Ic diperoleh dari

$$Ic = \frac{Vcc - Vce}{Rl}$$
$$= \frac{5 - 0,2}{170}$$
$$= 28,2mA$$

dan nilai I_B dapat dihitung sebagai berikut

$$I_B = \frac{I_C}{\beta}$$
$$= \frac{28,2 \times 10^{-3}}{250}$$
$$= 112,8x10^{-6} A$$

Dengan demikian nilai R_B dapat dihitung

$$R_B = \frac{V_H - V_{BE}}{I_\beta}$$
$$= \frac{5 - 0,7}{112,8.10^{-6}}$$
$$= 38,12\Omega$$

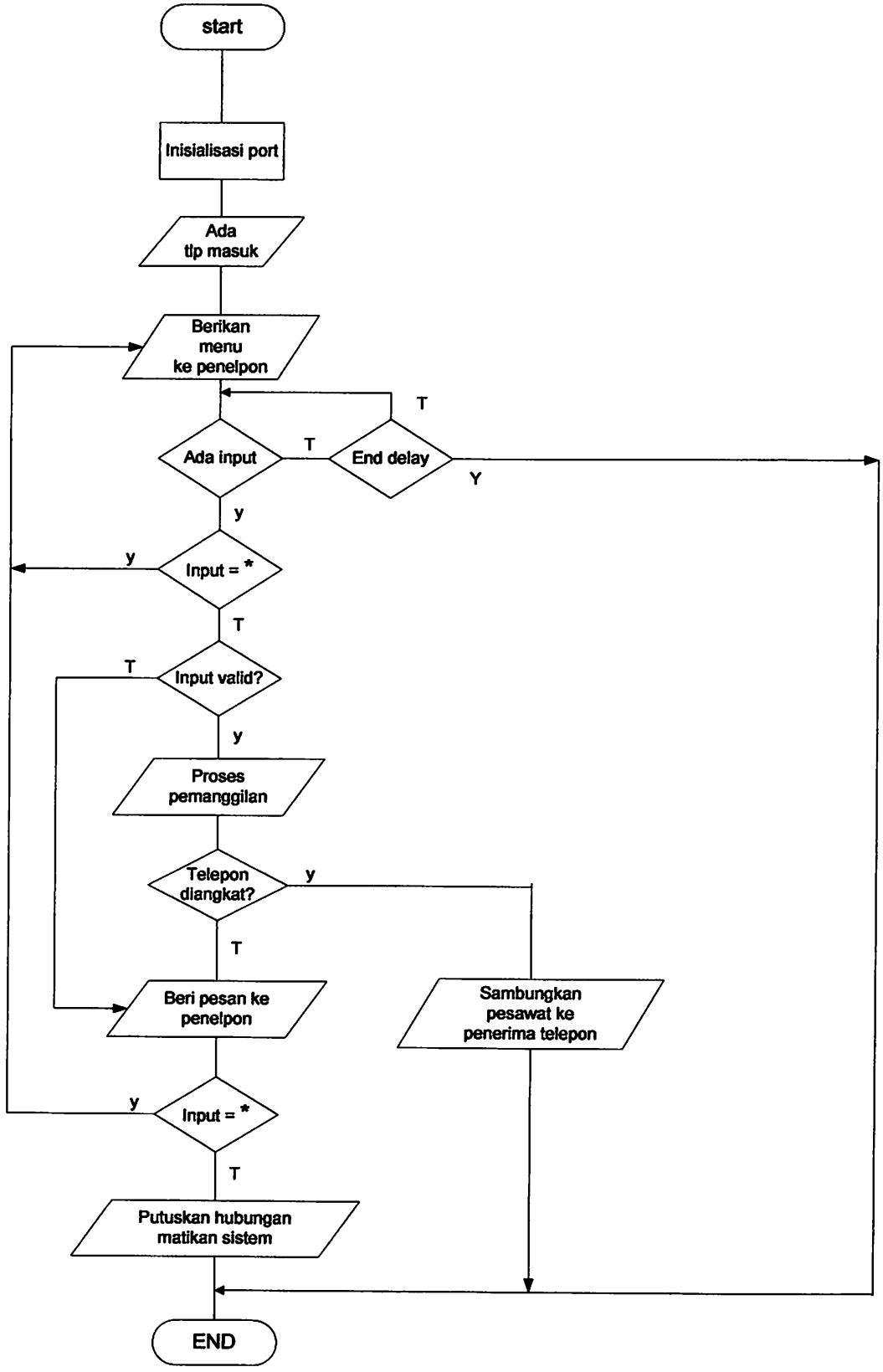
Jadi nilai R_B yang digunakan sebesar 4,7Ω yang ada di pasaran.

3.3. Perencanaan Perangkat Lunak

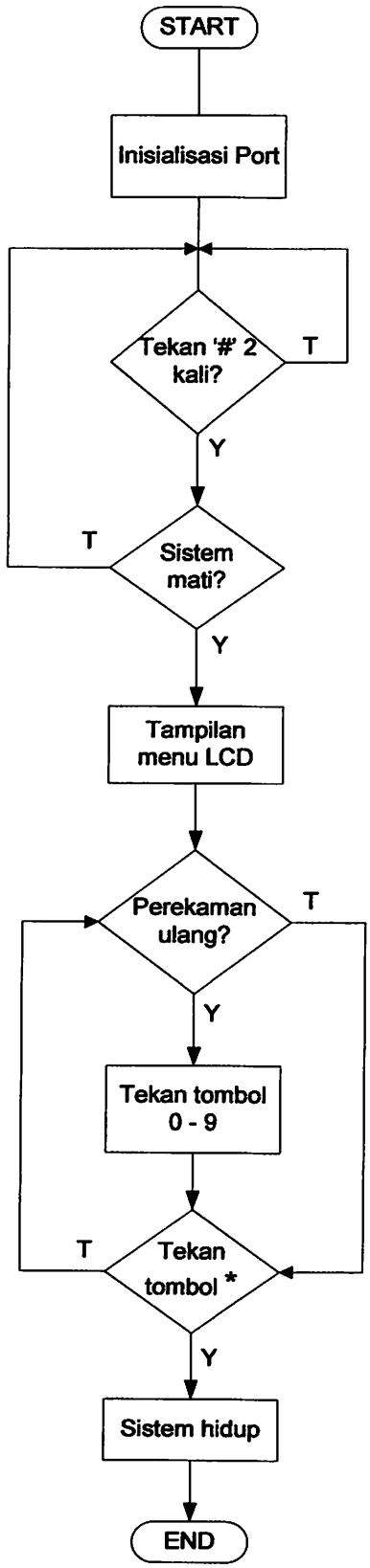
Setelah semua perangkat keras telah selesai dikerjakan pada tahap selanjutnya perangkat lunak (software) yang akan menangani sistem rangkaian. Pada perangkat

lunak inilah kita dapat menentukan bagaimana sistem rangkaian ini akan bekerja, pada bagian inilah semua tata kerja rangkaian ditentukan.

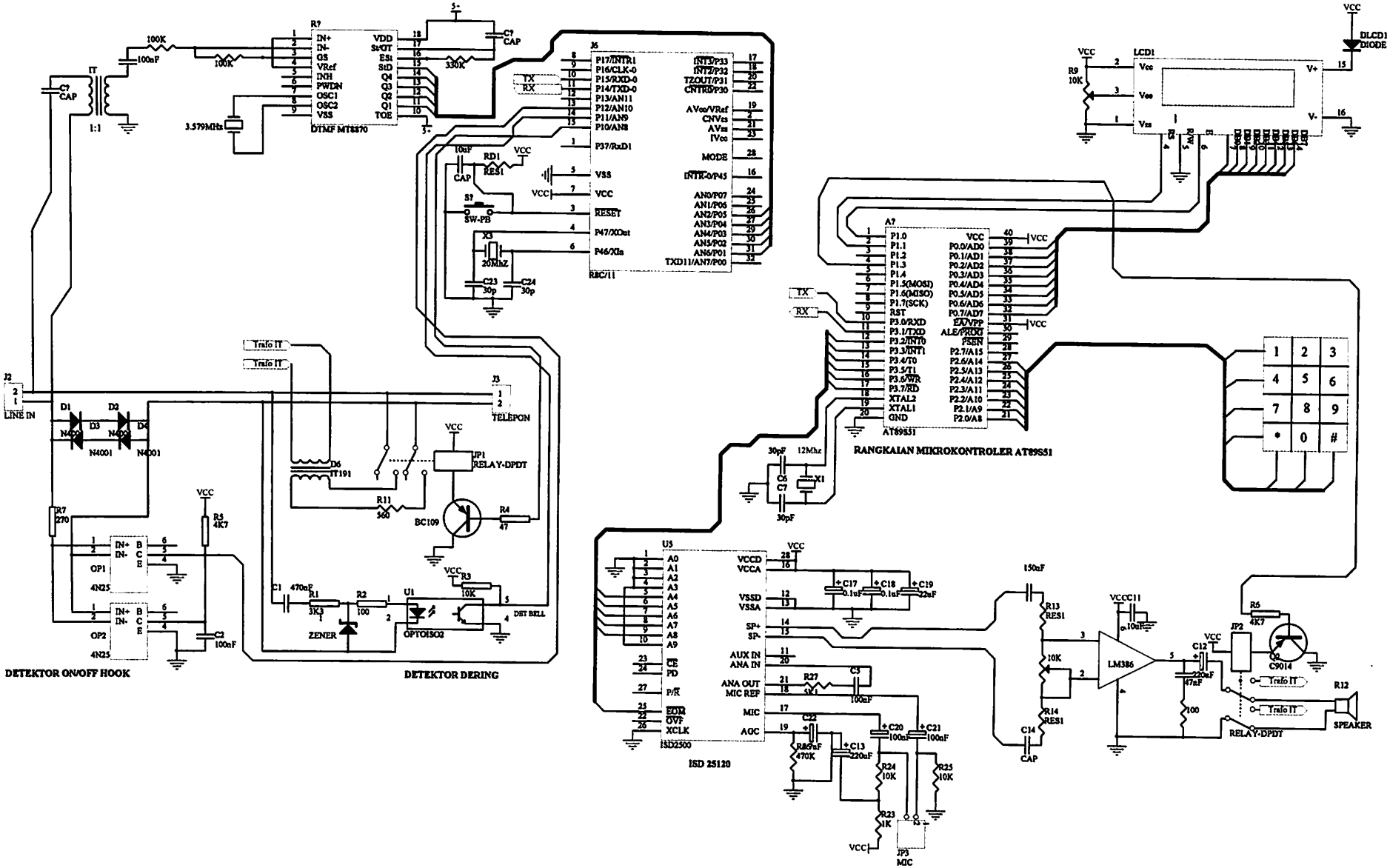
Sebelum kita membuat program, maka untuk mempermudah terlebih dahulu membuat diagram alir dari program yang akan dibuat, sehingga dengan begitu akan mempemudah dalam menentukan urutan kerja dari program. Adapun diagram alir dari program adalah sebagai berikut:



Gambar 3.12. Diagram Alir Penerima dan Pemanggil



Gambar 3.13. Diagram Alir Perekaman Ulang ISD



Gambar 3.13 Rangkaian Keseluruhan

BAB IV

PENGUJIAN ALAT

4.1. Umum

Untuk memestikan sistem dapat berjalan sesuai dengan spesifikasi perencanaan diperlukan serangkaian pengujian dan pengukuran. Bab pengujian dan pengukuran ini menguraikan tentang bagian alat yang diuji, tujuan pengujian, langkah- langkah pengujian dan hasil pengujian yang menunjukan unjuk kerja dari sub sistem alat apakah sesuai dengan yang direncanakan. Setelah dilakukan pengujian pada tiap - tiap bagian (sub sistem), selanjutnya dilakukan pengujian sistem secara keseluruhan.

Pengujian sub sistem meliputi pengujian relay, pengukuran line telepon, detektor hook, detektor dering, penerima DTMF, dan ISD 25120.

4.2. Pengujian Sub Sistem

4.2.1. Pengujian Rangkaian Relay

Tujuan pengujian rangkaian ini adalah untuk mengetahui unjuk kerja dari relay saat dioperasikan yang berfungsi menghubungkan atau memutuskan sistem dengan pesawat telepon lokal. Relay yang digunakan adalah relay DPDT (*Dual Pole Dual Totem*) yang memiliki dua keluaran yaitu NC (*Normally Close*) dan NO (*Normally open*) yang perlu diuji.

Peralatan yang digunakan

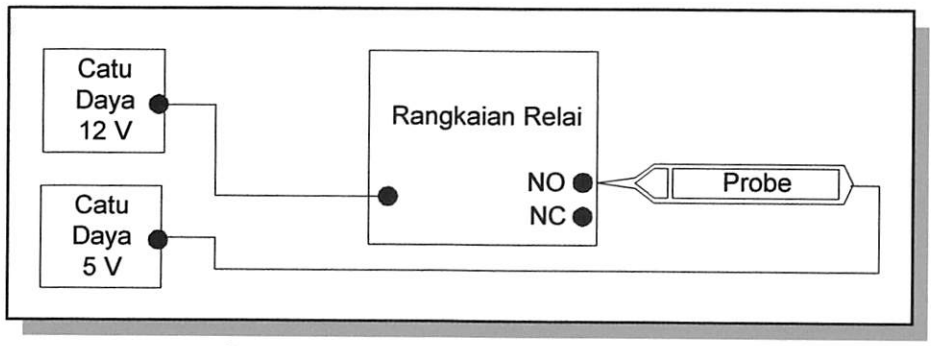
- *Logic Probe* model LP 3500.
- Catu daya 12 V dan 5 V.

Langkah – langkah pengujian

- Menghubungkan rangkaian catu daya dengan rangkaian relay.
- Menghubungkan *common* relay dengan kutub positif catu daya.

- Mengaktifkan catu daya dan memicu rangkaian relay.
- Mengamati perubahan indicator *logic probe* saat dihubungkan dengan keluaran NC dan NO rangkaian sebelum dan sesudah pemicuan.

Rangkaian pengujian relai ditunjukkan dalam Gambar 4.1.



Gambar 4.1 Rangkaian Pengujian Relay

Hasil pengujian

Hasil pengujian rangkaian relay ditunjukkan dalam Tabel 4.1

Tabel 4.1. Hasil Pengujian Rangkaian Relay

Keluaran	**Indikator *Logic Probe***	
	Sebelum Pemicuan	**Sesudah Pemicuan**
Normally Open (NO)	Hijau (rendah)	Merah (tinggi)
Normally Close (NC)	Merah (tinggi)	Hijau (rendah)

Berdasarkan hasil pengujian relay, maka dapat diambil kesimpulan bahwa pada saat terjadinya pemicuan, arus kolektor (I_C) pada transistor BC109 akan mengalir menuju *ground*. Pada keadaan *normally open* sebelum terjadinya pemicuan, *common* tidak terhubung dengan keluaran, sedangkan pada keadaan *normally close, common* terhubung dengan keluaran sebelum terjadinya pemicuan.

4.2.2. Pengukuran Saluran Telepon

Tujuan pengukuran line telepon adalah untuk mengetahui berapa besar tegangan yang dihasilkan pada saat ada panggilan masuk dan saat tidak ada panggilan.

Peralatan yang digunakan

- Voltmeter
- Line telepon

Langkah – langkah pengujian

- Menghubungkan logic probe tester dengan line telepon
- Mengamati hasil keluaran saat ada panggilan dan dan tidak ada panggilan

(a)

(b)

Gambar 4.2. Pengukuran Line Telepon Telepon

(a) saat tidak ada panggilan (VDC)

(b) saat ada panggilan (VAC)

Hasil pengujian

Tabel 4.2. Pengukuran Line Telepon

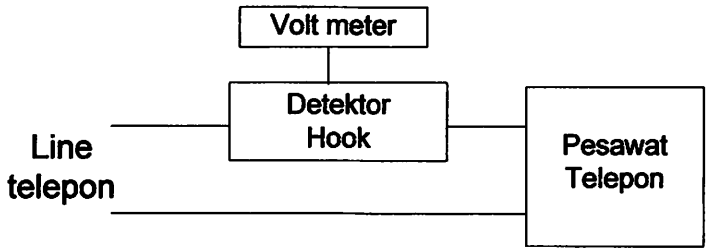
	Saat tidak ada panggilan	Saat ada panggilan
DC (V)	50 V	50 V
AC (V)	0 V	76,4 V

4.2.3. Pengujian Rangkaian Detektor Hook

Tujuan pengujian pada rangkaian ini adalah unutuk mengetahui bekerja tidaknya rangkaian detektor hook.

Peralatan yang digunakan

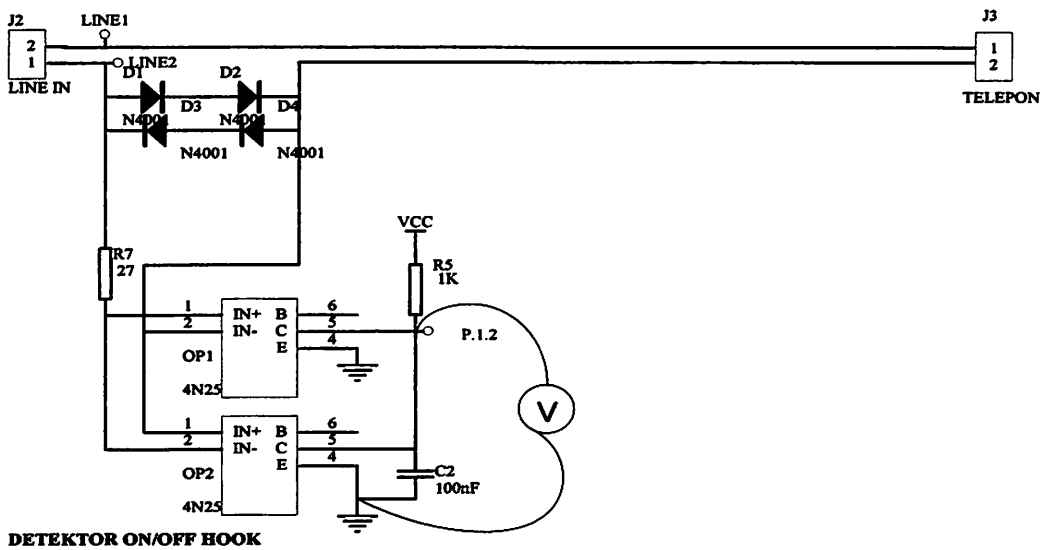
- Voltmeter.
- Line telepon.
- Pesawat telepon.



Gambar 4.2. Blok Pengujian Detektor Hook

Langkah pengujian

- Menghubungkan rangkaian detektor hook secara seri dengan line telepon dan pesawat telepon.
- Keluaran detektor hook dihubungkan dengan volt meter.
- Mengukur tegangan saat handset dalam keadaan on hook dan off hook.



Gambar 4.3. Pengujian Rangkaian Detektor Hook

Hasil pengujian

Tabel 4.2. Hasil Pengujian Rangkaian Detektor Hook

Posisi *Handset*	Output	
Off Hook	0 V	Low
On Hook	4,26 V	High

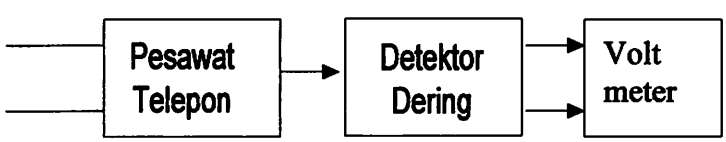
Dari hasil pengujian dapat diambil kesimpulan bahwa pada saat *on hook* detektor hook berlogika satu (*high*), sedangkan pada saat *off hook* detektor berlogika nol (*low*). Dari tabel 4.2. memperlihatkan respon keluaran dari detektor hook saat gagang diangkat memberikan respon yang sesuai dengan yang diharapkan dalam perencanaan yang merupakan masukan bagi mikrokontroller.

4.2.4. Pengujian Rangkaian Detektor Bell

Tujuan pengujian rangkaian ini adalah untuk mengetahui unjuk kerja rangkaian detektor dering pada saat ada sinyal yang masuk.

Peralatan yang digunakan

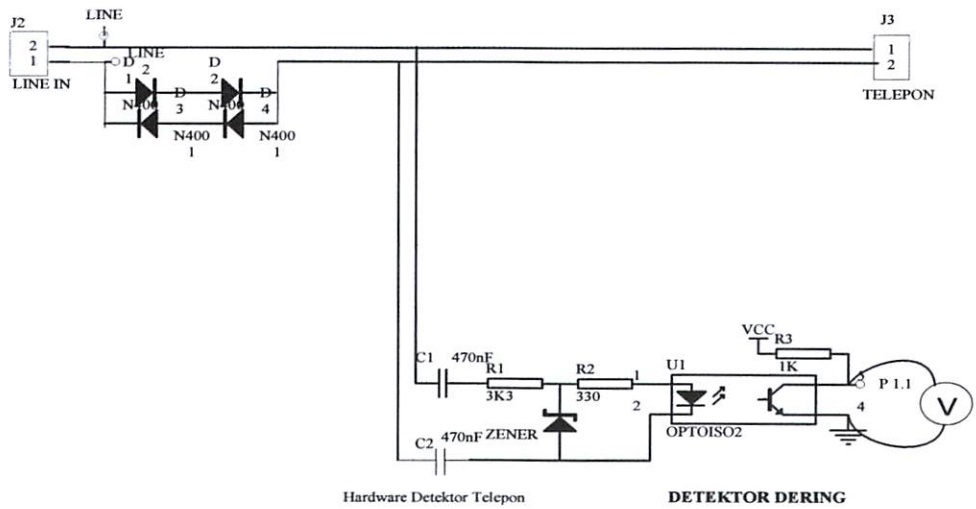
- Voltmeter digital.
- Rangkaian detektor dering.
- Saluran telepon.
- Catu daya 5 V.



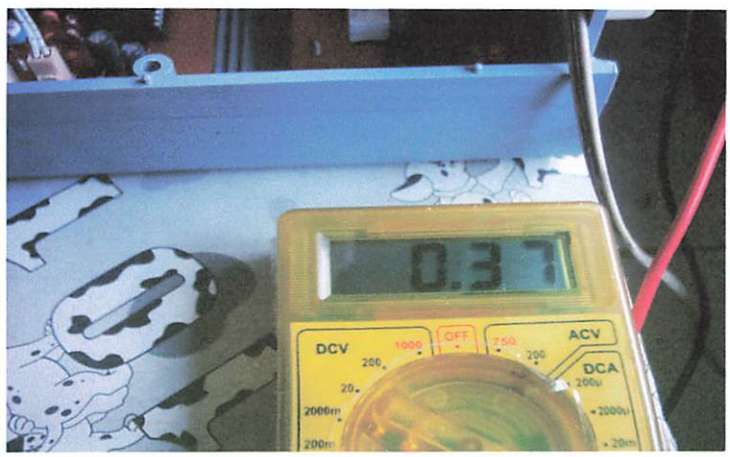
Gambar 4.4. Blok Pengujian Rangkaian Detektor Dering

Langkah pengujian

- Menghubungkan secara seri rangkaian detektor dering dengan line dari sentral telepon seperti pada gambar (a)
- Mengaktifkan catu daya.
- Keluaran detektor dering di ukur dengan voltmeter dan mengamati perubahan indikatornya pada saat telepon ada dering.



(a)



(b)

Gambar 4.5. Pengujian Rangkaian Detektor Dering

(a) rangkaian yang diuji

(b) tegangan saat ada panggilan masuk

Hasil pengujian

Tabel 4.3. Hasil Pengujian Rangkaian Detektor Dering

Keadaaan Sinyal	Tegangan
Tidak ada dering	4,89 V DC
Ada dering	0,37 V DC

Berdasarkan hasil pengujian detektor dering, bahwa saat tidak ada sinyal bel, tegangan saluran adalah ± 48V tegangan searah dan tidak ada arus yang mengalir, hal ini menyebabkan LED pada *optocoupler* tidak aktif sehingga tidak ada arus kolektor yang mengalir dari V_{CC} ke *ground* dan tegangan pada keluaran besarnya sama dengan tegangan V_{CC} yaitu 5V yang dideteksi sebagai logika tinggi oleh *logic probe*.

Sebaliknya pada saat ada sinyal bel, tegangan saluran mencapai ± 90V tegangan bolak-balik. Saat tegangan saluran berada pada tegangan *breakdown* dioda *zener*, tegangan pada masukan rangkaian *optocoupler* adalah 4,7V sesuai dengan karakteristik diode *zener* yang digunakan. Sedangkan saat tegangan saluran lebih kecil daripada tegangan *breakdown*-nya, tegangan pada masukan rangkaian *optocoupler* adalah –0,7V. Tegangan 4,7V pada masukan rangkaian *optocoupler* menyebabkan LED *optocoupler* aktif dan memicu transistor. Akibatnya arus kolektor akan mengalir dari V_{CC} ke *ground* sehingga tegangan pada keluaran sama dengan tegangan *ground* yaitu 0,37V dan oleh *logic probe* dideteksi sebagai logika rendah.

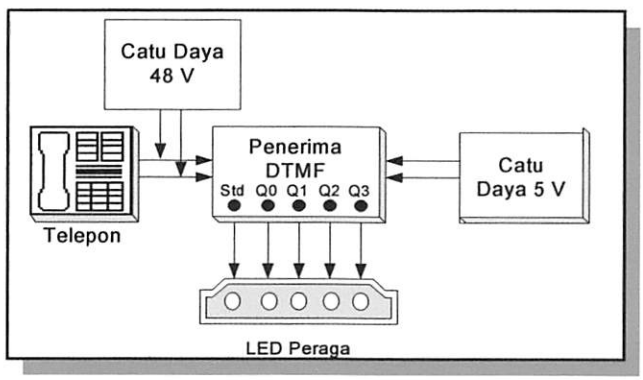
4.2.5. Pengujian Rangkaian Penerima DTMF

Tujuan dari pengujian rangkaian ini adalah untuk mengetahui respon penerima DTMF jika diberi masukan sinyal DTMF dari pesawat telepon.

Peralatan yang digunakan :

- Pesawat Telepon.
- LED peraga yang berfungsi untuk mengetahui keadaaan logika penyemat Std dan keluaran Q_0-Q_3.
- Catu daya 5V DC dan 48 V DC.

Rangkaian pengujian penerima DTMF ditunjukkan dalam Gambar 4.6.



Gambar 4.6. Rangkaian Pengujian Penerima DTMF

Langkah pengujian

1. Merangkai peralatan seperti dalam Gambar 4.6.
2. Menghubungkan secara paralel masukan rangkaian penerima nada DTMF dengan catu daya 48 V DC yang berfungsi sebagai simulasi line telepon menuju ke pesawat telepon .
3. Mengaktifkan catu daya.
4. Menekan salah satu tombol pada *keypad* telepon secara bergantian.
5. Mengamati dan mencatat keluaran LED peraga.

Hasil pengujian :

Dari hasil pengujian rangkaian penerima DTMF, saat ada penekanan tombol telepon maka penyemat StD akan berlogika 1. Keadaan ini bertahan selama tombol

telepon ditekan terus, sebaliknya bila tombol telepon dilepas maka kondisi logikanya akan berubah menjadi 0. Hal ini menunjukkan pengkondisian keadaan saat ada penekanan tombol telepon adalah sama dengan logika 1. Hasil pengujian rangkaian penerima DTMF ditunjukkan dalam Tabel 4.4.

Tabel 4.4. Hasil Pengujian Rangkaian Penerima DTMF

Tombol yang Ditekan	Keluaran DTMF				
	Std	Q3	Q2	Q1	Q0
1	1	0	0	0	1
2	1	0	0	1	0
3	1	0	0	1	1
4	1	0	1	0	0
5	1	0	1	0	1
6	1	0	1	1	0
7	1	0	1	1	1
8	1	1	0	0	0
9	1	1	0	0	1
0	1	1	0	1	0
*	1	1	0	1	1
#	1	1	1	0	0

Pada saat terjadi penekanan tombol telepon maka penyemat Q_0-Q_3 akan berlogika sesuai dengan tombol telepon yang dikodekan. Keadaan ini akan bertahan

sampai ada penekanan tombol telepon baru lagi, jadi kondisi logika pada penyemat Q_0-Q_3 ini tidak akan berubah jika tidak ada penekanan tombol telepon yang baru. Hal ini disebabkan karena pada rangkaian *internal* IC penerima nada DTMF 8870 terdapat rangkaian *latch* yang berfungsi untuk menahan data terakhir sampai ada data baru lagi.

4.2.6. Pengujian Rangkaian ISD 25120

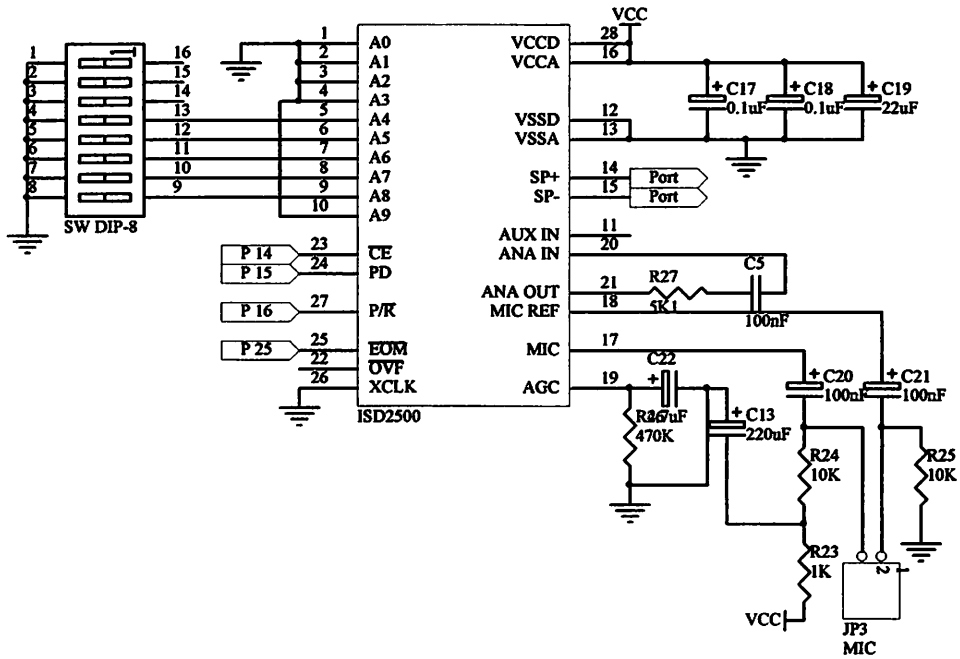
Tujuan dari pengujian ISD ini adalah untuk mengetahui apakah ISD 25120 bisa melakukan perekaman suara dengan baik atau tidak.

Peralatan yang digunakan

- *Dip Switch* 8 bit.
- Rangkaian ISD 25120.
- Catu daya 5 volt.
- Speaker 8 Ohm.

Langkah pengujian

- Memeberiakan alamat dengan memasukan data 5 bit pada *Dip Switch.*
- Menghubungkan pin P/R dengan ground untuk memulai merekam melalui mic.
- Mencatat alamat yang diberikan melalui *Dip Switch* dan di tabelkan.
- Menghubungkan pin P/R dengan Vcc untuk mendengarkan hasil suara.



Gambar 4.7. Rangkaian ISD 25120

Hasil pengujian

No.	Data Suara ISD
1.	"Selamat datang dilayanan pemanggil otomatis silahkan tekan 0 sampai dengan 9 untuk melakukan pemanggilan"
2.	"Nol"
3.	"Satu"
4.	"Dua"
5.	"Tiga"
6.	"Empat"
7.	"Lima"
8.	"Enam"
9.	"Tujuh"
10.	"Delapan"
11.	"Sembilan"
12.	"Untuk"
13.	"Ada Telepon"
14.	"Andi"
15.	"Budi"
16.	"Azmi"
17.	"Yuda"
18.	"Imam"
19.	"Wira"

20.	"Deni"
21.	"Noval"
22.	"Rio"
23.	"Doni"
24.	"Tekan bintang untuk kembali ke awal"
25.	"Maaf orang yang anda panggil sedang keluar"

4.3. Pengujian Keseluruhan

Tujuan dari pengujian keseluruhan ini adalah untuk mengetahui apakah setelah rangkaian keseluruhan dirangkai jadi satu sistem mampu bekerja dengan baik.

Untuk pengujian keseluruhan adalah dengan merangkai menjadi satu bagian blok – blok yang telah diuji sebelumnya dan mengisi MCU dengan *software.* Langkah –langkah pengujian rangkaian keseluruhan adalah sebagai berikut:

1. Untuk pengujian informasi yaitu dengan cara memasang sistem kesaluran telepon dan selanjutnya mencoba melakukan panggilan terhadap pesawat telepon yang sudah terpasang dengan sistem dan mendengarkan informasi yang ada.
2. Untuk pengujian dengan pemanggilan nama yaitu seperti pada langkah pertama, selanjutnya menekan tombol melalui pesawat telepon yang digunakan untuk menghubungi sistem, kemudian mendengarkan proses pemanggilan nama oleh sistem tersebut.
3. Mengulang langkah kedua untuk penekanan tombol yang lain.
4. Untuk pengesetan ulang nama yaitu dengan menekan tombol bintang (#) dua kali pada keypad, kemudian rekam nama yang baru dan mematikan sistem perekaman dengan menekan tanda pagar (*) di keypad satu kali, mengulangi langkah kedua dan ketiga untuk mengetahui hasilnya.

Hasil pengujian

Setelah dilakukan pengujian sistem secara keseluruhan maka didapat hasil bahwa penyampaian informasi oleh sistem berjalan dengan baik sesuai dengan perencanaan. Informasi ini menyampaikan nama dan kode nomor yang harus ditekan untuk menghubungi orang yang dituju. Proses pemanggilan juga bekerja sesuai dengan yang diharapkan, pemanggilan nama ini bekerja setelah ditekan tombol (kode nomor) di pesawat telepon (saat melakukan panggilan), penekanan tombol harus sesuai dengan yang ada di informasi. Pengesetan ulang nama dengan menekan tombol # pada keypad juga berjalan dengan baik setelah dilakukan pengujian dengan memanggil nama yang baru dimasukan.

.

BAB V

PENUTUP

5.1. Kesimpulan

Dari hasil perancangan dan pembuatan alat telah diadakan pengujian, sehingga dapat diambil kesimpulan sebagai berikut :

1. Alat ini hanya bisa digunakan di jaringan telepon dengan pesawat telepon pengirim menggunakan metode dial tone DTMF.
2. Alat ini tidak bisa digunakan pada sistem PABX, karena line PABX berbeda dengan line telepon biasa, kecuali dalam satu sentral PABX.
3. Pada saat melakukan panggilan, bel pada telepon yang dituju biasanya akan berbunyi selama dua kali, setelah itu barulah terhubung ke rangkaian hook semu.
4. Nada DTMF baru dapat terkirim oleh si penelpon setelah sistem selesai menyampaikan menu.
5. Ketika sistem sedang aktif, dimana telepon lokal dan saluran telepon terhubung dengan alat, jika gagang telepon lokal diangkat untuk beberapa saat maka terdengar suara penyampai pesan. Untuk hal tersebut agar sistem dapat bekerja dengan baik maka perlu dilakukan reset pada mikro AT89S51.

5.2. Saran

Untuk pengembangan alat ini lebih lanjut dapat ditambahkan dengan inovasi yang lebih jauh mengenai:

1. Penambahan kapasitas ISD, digunakan untuk media peninggal pesan oleh si penelpon seandainya orang yang dituju sedang tidak ada.
2. Sebaiknya ditambahkan password untuk mengakses perekaman ulang yang berfungsi mencegah adanya perubahan data yang tersimpan pada ISD diakibatkan oleh tangan jahil.

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LAMPIRAN

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FAKULTAS TEKNOLOGI INDUSTRI
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BERITA ACARA UJIAN SKRIPSI
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Konsentrasi : Teknik Elektronika
Judul skripsi : Perencanaan dan Pembuatan Sistem Penerima Telepon dan Pemanggil Otomatis pada Rumah Kost Menggunakan Mikrokontroller R8C/13 dan AT89S51

Dipertahankan dihadapan majelis penguji skripsi jenjang starta satu (S-1) pada:
Hari : Jum'at
Tanggal : 23 Maret 2007
Dengan nilai : 82,.2 (A)

Panitia ujian skripsi

Ketua	Sekretaris
Ir. Mochtar Asroni, MSME	Ir. F. Yudi Limpraptono, MT

Anggota penguji

Penguji I	Penguji II
DR. Cahyo Crysdian, MSc	I Komang Somawiranata, ST, MT

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JURUSAN TEKNIK ELEKTRO

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Dari hasil skripsi jurusan Teknik Elektronika jenjang Strata Satu (S-1), yang diselenggarakan pada:

Hari : Jum'at
Tanggal : 23 Maret 2007

Telah dilakukan perbaikan oleh:

Nama : Hadi Cahyadi
Nim : 0117112
Jurusan : Teknik Elektro S-1
Konsentrasi : Teknik Elektronika
Judul Skripsi : Perencanaan dan Pembuatan Sistem Penerima Telepon dan Pemanggil Otomatis pada Rumah Kost Menggunakan Mikrokontroller R8C/13 dan AT89S51

Perbaikan meliputi

No.	Materi Perbaikan	Paraf
1.	Integrasikan skema rangkaian	
2.	Ukur sinyal telepon saat tidak atau saat ada call in	
3.	Ukur keluaran sinyal optocoupler saat ada sinyal call in	
4.	Bahas komunikasi antara mikrokontroler Renesas dan AT89S51	

Penguji I

DR. Cahyo Crysdian, MSc

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LEMBAR PERSETUJUAN SKRIPSI

Dari hasil skripsi jurusan Teknik Elektronika jenjang Strata Satu (S-1), yang diselenggarakan pada:

Hari : Jum'at

Tanggal : 23 Maret 2007

Telah dilakukan perbaikan oleh:

Nama : Hadi Cahyadi

Nim : 0117112

Jurusan : Teknik Elektro S-1

Konsentrasi : Teknik Elektronika

Judul Skripsi : Perencanaan dan Pembuatan Sistem Penerima Telepon dan Pemanggil Otomatis pada Rumah Kost Menggunakan Mikrokontroller R8C/13 dan AT89S51

Perbaikan meliputi

No.	Materi Perbaikan	paraf
1.	Blok diagram disesuaikan dengan rangkaian	
2.	Gambar 3.6	
3.	Gambar dengan analisa disesuaikan	

Penguji II

I Komang Somawiranata, ST, MT

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FORMULIR BIMBINGAN SKRIPSI

NAMA : Hadi Cahyadi
NIM : 0117112
Masa Bimbingan : 27 Januari 2006 - 27 Juli 2007
Judul Skripsi : Perencanaan dan Pembuatan Sistem Penerima Telepon dan Pemanggil Otomatis pada Rumah Kost Menggunakan Mikrokontroller R8C/13 dan AT89S51

NO	Tanggal	Uraian	Paraf Pembimbing
1.		Bab IV + V	
2.		Demo	
3.	12/3 2007	Seminar	
4.	13/3 2007	Penyerahan Komputer	
5.			
6.			
7.			
8.			
9.			
10.			

Malang, ……..
Dosen Pembimbing I

Ir. F Yudi Limpraptono, MT
NIP.P 103.9500.127

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FAKULTAS TEKNOLOGI INDUSTRI
JURUSAN TEKNIK ELEKTRO

FORMULIR BIMBINGAN SKRIPSI

NAMA : Hadi Cahyadi
NIM : 0117112
Masa Bimbingan : 27 Januari 2006 - 27 Juli 2007
Judul Skripsi : Perencanaan dan Pembuatan Sistem Penerima Telepon dan Pemanggil Otomatis pada Rumah Kost Menggunakan Mikrokontroller R8C/13 dan AT89S51

NO	Tanggal	Uraian	Paraf Pembimbing
1.		Tambah dengan rangkaian lengkap yg terhubung jadi satu	
2.		Sempurnakan gbr - 2 di Bab III	
3.		Pelajari Bab III	
4.		Diagram alir diperbaiki	
5.		Bab II OK	
6.		Bab I OK	
7.		kerjakan Bab IV + V	
8.		ACC kompre	
9.			
10.			

Malang, ...
Dosen Pembimbing II

Ir. Mimien Mustikawati
NIP.P 103.0000.352

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FAKULTAS TEKNOLOGI INDUSTRI
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Formulir Perbaikan Ujian Skripsi

Dalam pelaksanaan Ujian Skripsi Janjang Strata 1 Jurusan Teknik Elektro Konsentasi T. Energi Listrik / T. Elektronika, maka perlu adanya perbaikan skripsi untuk mahasiswa :

NAMA : Hadi Cahyadi
NIM : 0117112
Perbaikan meliputi :

1) Justifikasi Nama Fuzzy nya kurang
2) Ukur sinyal telepon saat idle atau saat ada call in.
3) Ukur tuluan Optocoupler saat ada call in.
4) Bahas kompilasi antar per percobaan BAB IV

Malang,

(Dr. Cahyo C. MSc)

INSTITUT TEKNOLOGI NASIONAL
FAKULTAS TEKNOLOGI INDUSTRI
JURUSAN TEKNIK ELEKTRO

Formulir Perbaikan Ujian Skripsi

Dalam pelaksanaan Ujian Skripsi Janjang Strata 1 Jurusan Teknik Elektro Konsentasi T. Energi Listrik / T. Elektronika, maka perlu adanya perbaikan skripsi untuk mahasiswa :

NAMA : Hadi Cahyadi
NIM : 0117112
Perbaikan meliputi :

1) Blok. Diagram disesuaikan dgn Rangkaian
2) Gbr 3.6.
3) Gabr. dgn Analisa & Pembahasan

Malang,

(I. Komang S. ST, MT)

tures

- npatible with MCS-51® Products
- Bytes of In-System Programmable (ISP) Flash Memory
  - Endurance: 1000 Write/Erase Cycles
- V to 5.5V Operating Range
- y Static Operation: 0 Hz to 33 MHz
- ee-level Program Memory Lock
- x 8-bit Internal RAM
- Programmable I/O Lines
- 16-bit Timer/Counters
- Interrupt Sources
- Duplex UART Serial Channel
- -power Idle and Power-down Modes
- rrupt Recovery from Power-down Mode
- chdog Timer
- l Data Pointer
- ver-off Flag
- t Programming Time
- ible ISP Programming (Byte and Page Mode)

cription

T89S51 is a low-power, high-performance CMOS 8-bit microcontroller with 4K of in-system programmable Flash memory. The device is manufactured using 's high-density nonvolatile memory technology and is compatible with the indus-andard 80C51 instruction set and pinout. The on-chip Flash allows the program ory to be reprogrammed in-system or by a conventional nonvolatile memory pro-mer. By combining a versatile 8-bit CPU with in-system programmable Flash on a lithic chip, the Atmel AT89S51 is a powerful microcontroller which provides a -flexible and cost-effective solution to many embedded control applications.

T89S51 provides the following standard features: 4K bytes of Flash, 128 bytes of 32 I/O lines, Watchdog timer, two data pointers, two 16-bit timer/counters, a five- two-level interrupt architecture, a full duplex serial port, on-chip oscillator, and circuitry. In addition, the AT89S51 is designed with static logic for operation to zero frequency and supports two software selectable power saving modes. dle Mode stops the CPU while allowing the RAM, timer/counters, serial port, and upt system to continue functioning. The Power-down mode saves the RAM con-but freezes the oscillator, disabling all other chip functions until the next external upt or hardware reset.

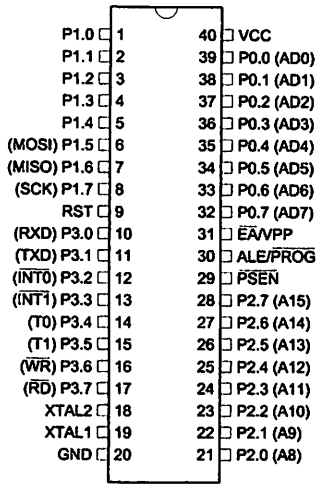
8-bit Microcontroller with 4K Bytes In-System Programmable Flash

AT89S51

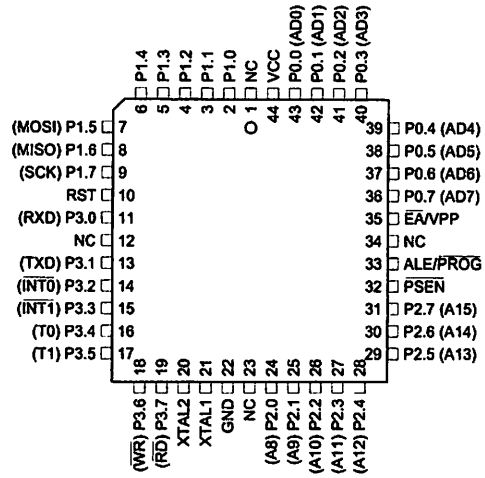
Rev. 2487A–10/01

Configurations

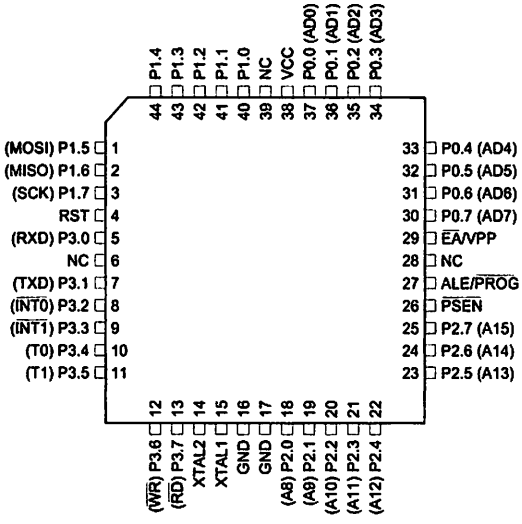
PDIP



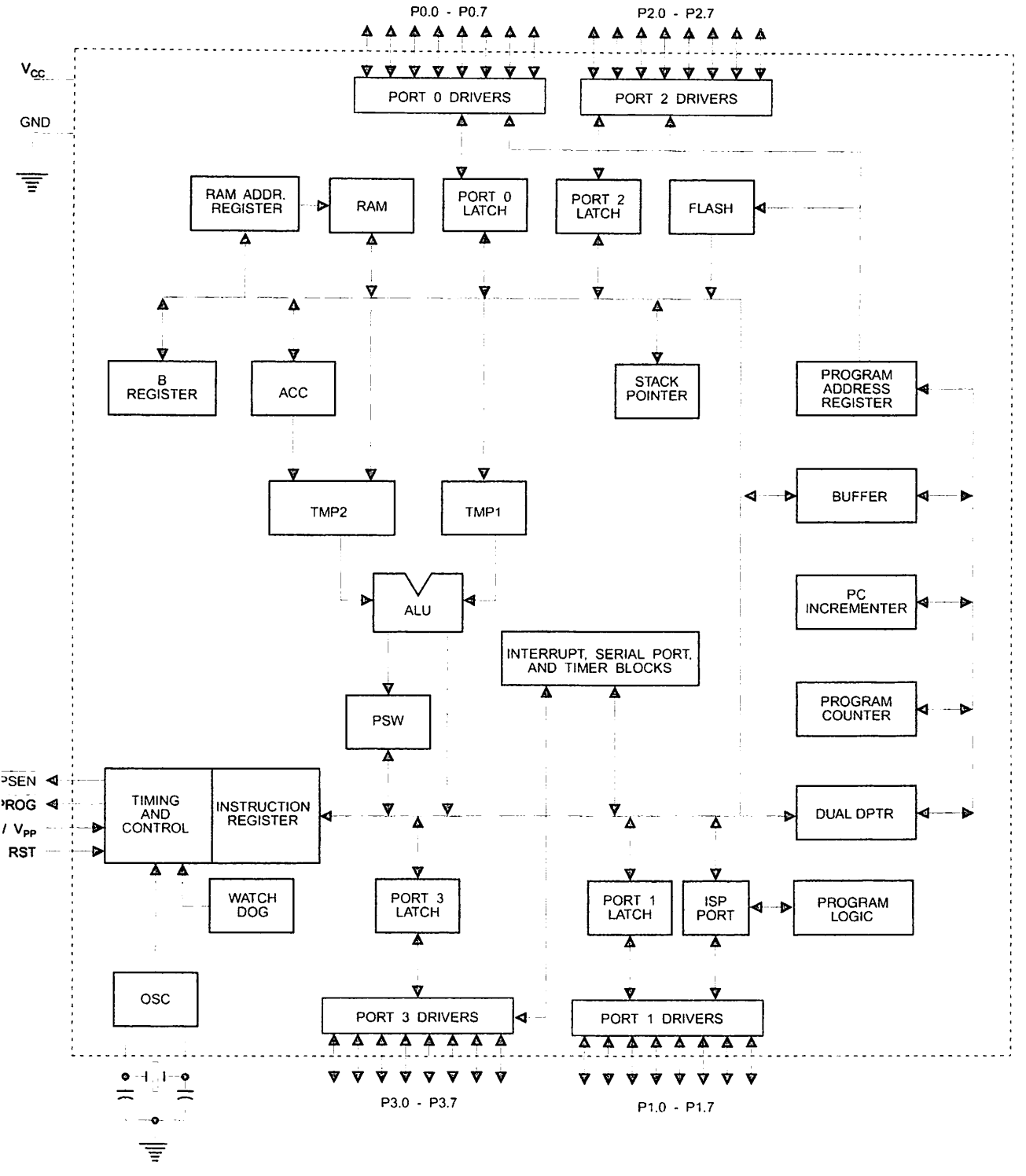
PLCC



TQFP



ck Diagram


P0.0 - P0.7
P2.0 - P2.7
V_{CC}
GND
PORT 0 DRIVERS
PORT 2 DRIVERS
RAM ADDR. REGISTER
RAM
PORT 0 LATCH
PORT 2 LATCH
FLASH
B REGISTER
ACC
STACK POINTER
PROGRAM ADDRESS REGISTER
TMP2
TMP1
BUFFER
ALU
PC INCREMENTER
INTERRUPT, SERIAL PORT, AND TIMER BLOCKS
PSW
PROGRAM COUNTER
PSEN
PROG
/ V_{PP}
RST
TIMING AND CONTROL
INSTRUCTION REGISTER
DUAL DPTR
WATCH DOG
PORT 3 LATCH
PORT 1 LATCH
ISP PORT
PROGRAM LOGIC
OSC
PORT 3 DRIVERS
PORT 1 DRIVERS
P3.0 - P3.7
P1.0 - P1.7

Description

Supply voltage.

Ground.

0

Port 0 is an 8-bit open drain bidirectional I/O port. As an output port, each pin can sink eight TTL inputs. When 1s are written to port 0 pins, the pins can be used as high-impedance inputs.

Port 0 can also be configured to be the multiplexed low-order address/data bus during accesses to external program and data memory. In this mode, P0 has internal pull-ups.

Port 0 also receives the code bytes during Flash programming and outputs the code bytes during program verification. **External pull-ups are required during program verification.**

1

Port 1 is an 8-bit bidirectional I/O port with internal pull-ups. The Port 1 output buffers can sink/source four TTL inputs. When 1s are written to Port 1 pins, they are pulled high by the internal pull-ups and can be used as inputs. As inputs, Port 1 pins that are externally being pulled low will source current (I_{IL}) because of the internal pull-ups.

Port 1 also receives the low-order address bytes during Flash programming and verification.

Port Pin	Alternate Functions
P1.5	MOSI (used for In-System Programming)
P1.6	MISO (used for In-System Programming)
P1.7	SCK (used for In-System Programming)

2

Port 2 is an 8-bit bidirectional I/O port with internal pull-ups. The Port 2 output buffers can sink/source four TTL inputs. When 1s are written to Port 2 pins, they are pulled high by the internal pull-ups and can be used as inputs. As inputs, Port 2 pins that are externally being pulled low will source current (I_{IL}) because of the internal pull-ups.

Port 2 emits the high-order address byte during fetches from external program memory and during accesses to external data memory that use 16-bit addresses (MOVX @ DPTR). In this application, Port 2 uses strong internal pull-ups when emitting 1s. During accesses to external data memory that use 8-bit addresses (MOVX @ RI), Port 2 emits the contents of the P2 Special Function Register.

Port 2 also receives the high-order address bits and some control signals during Flash programming and verification.

3

Port 3 is an 8-bit bidirectional I/O port with internal pull-ups. The Port 3 output buffers can sink/source four TTL inputs. When 1s are written to Port 3 pins, they are pulled high by the internal pull-ups and can be used as inputs. As inputs, Port 3 pins that are externally being pulled low will source current (I_{IL}) because of the pull-ups.

Port 3 receives some control signals for Flash programming and verification.

Port 3 also serves the functions of various special features of the AT89S51, as shown in the following table.

Port Pin	Alternate Functions
P3.0	RXD (serial input port)
P3.1	TXD (serial output port)
P3.2	$\overline{INT0}$ (external interrupt 0)
P3.3	$\overline{INT1}$ (external interrupt 1)
P3.4	T0 (timer 0 external input)
P3.5	T1 (timer 1 external input)
P3.6	$\overline{WR}$ (external data memory write strobe)
P3.7	$\overline{RD}$ (external data memory read strobe)

Reset input. A high on this pin for two machine cycles while the oscillator is running resets the device. This pin drives High for 98 oscillator periods after the Watchdog times out. The DISRTO bit in SFR AUXR (address 8EH) can be used to disable this feature. In the default state of bit DISRTO, the RESET HIGH out feature is enabled.

/$\overline{PROG}$

Address Latch Enable (ALE) is an output pulse for latching the low byte of the address during accesses to external memory. This pin is also the program pulse input ($\overline{PROG}$) during Flash programming.

In normal operation, ALE is emitted at a constant rate of 1/6 the oscillator frequency and may be used for external timing or clocking purposes. Note, however, that one ALE pulse is skipped during each access to external data memory.

If desired, ALE operation can be disabled by setting bit 0 of SFR location 8EH. With the bit set, ALE is active only during a MOVX or MOVC instruction. Otherwise, the pin is weakly pulled high. Setting the ALE-disable bit has no effect if the microcontroller is in external execution mode.

$\overline{N}$

Program Store Enable ($\overline{PSEN}$) is the read strobe to external program memory.

When the AT89S51 is executing code from external program memory, $\overline{PSEN}$ is activated twice each machine cycle, except that two $\overline{PSEN}$ activations are skipped during each access to external data memory.

/PP

External Access Enable. $\overline{EA}$ must be strapped to GND in order to enable the device to fetch code from external program memory locations starting at 0000H up to FFFFH. Note, however, that if lock bit 1 is programmed, $\overline{EA}$ will be internally latched on reset.

$\overline{EA}$ should be strapped to V_{CC} for internal program executions.

This pin also receives the 12-volt programming enable voltage (V_{PP}) during Flash programming.

L1

Input to the inverting oscillator amplifier and input to the internal clock operating circuit.

L2

Output from the inverting oscillator amplifier

ecial
nction
gisters

A map of the on-chip memory area called the Special Function Register (SFR) space is shown in Table 1.

Note that not all of the addresses are occupied, and unoccupied addresses may not be implemented on the chip. Read accesses to these addresses will in general return random data, and write accesses will have an indeterminate effect.

e 1. AT89S51 SFR Map and Reset Values

8H								0FFH
0H	B 00000000							0F7H
8H								0EFH
0H	ACC 00000000							0E7H
8H								0DFH
0H	PSW 00000000							0D7H
8H								0CFH
0H								0C7H
8H	IP XX000000							0BFH
0H	P3 11111111							0B7H
8H	IE 0X000000							0AFH
0H	P2 11111111		AUXR1 XXXXXXX0				WDTRST XXXXXXXX		0A7H
8H	SCON 00000000	SBUF XXXXXXXX							9FH
0H	P1 11111111								97H
8H	TCON 00000000	TMOD 00000000	TL0 00000000	TL1 00000000	TH0 00000000	TH1 00000000	AUXR XXX00XX0		8FH
0H	P0 11111111	SP 00000111	DP0L 00000000	DP0H 00000000	DP1L 00000000	DP1H 00000000		PCON 0XXX0000	87H

User software should not write 1s to these unlisted locations, since they may be used in future products to invoke new features. In that case, the reset or inactive values of the new bits will always be 0.

Interrupt Registers: The individual interrupt enable bits are in the IE register. Two priorities can be set for each of the five interrupt sources in the IP register.

Table 2. AUXR: Auxiliary Register

AUXR Address = 8EH Reset Value = XXX00XX0B

Not Bit Addressable

	–	–	–	WDIDLE	DISRTO	–	–	DISALE
Bit	7	6	5	4	3	2	1	0

–	Reserved for future expansion
DISALE	Disable/Enable ALE
	DISALE Operating Mode
	0 ALE is emitted at a constant rate of 1/6 the oscillator frequency
	1 ALE is active only during a MOVX or MOVC instruction
DISRTO	Disable/Enable Reset out
	DISRTO
	0 Reset pin is driven High after WDT times out
	1 Reset pin is input only
WDIDLE	Disable/Enable WDT in IDLE mode
WDIDLE	
0	WDT continues to count in IDLE mode
1	WDT halts counting in IDLE mode

Dual Data Pointer Registers: To facilitate accessing both internal and external data memory, two banks of 16-bit Data Pointer Registers are provided: DP0 at SFR address locations 82H-83H and DP1 at 84H-85H. Bit DPS = 0 in SFR AUXR1 selects DP0 and DPS = 1 selects DP1. The user should always initialize the DPS bit to the appropriate value before accessing the respective Data Pointer Register.

Power Off Flag: The Power Off Flag (POF) is located at bit 4 (PCON.4) in the PCON SFR. POF is set to "1" during power up. It can be set and rest under software control and is not affected by reset.

Table 3. AUXR1: Auxiliary Register 1

AUXR1

Address = A2H

Reset Value = XXXXXXX0B

Not Bit Addressable

Bit	7	6	5	4	3	2	1	0
	–	–	–	–	–	–	–	DPS

– Reserved for future expansion

DPS Data Pointer Register Select

DPS	
0	Selects DPTR Registers DP0L, DP0H
1	Selects DPTR Registers DP1L, DP1H

nory anization

MCS-51 devices have a separate address space for Program and Data Memory. Up to 64K bytes each of external Program and Data Memory can be addressed.

gram Memory

If the $\overline{EA}$ pin is connected to GND, all program fetches are directed to external memory.

On the AT89S51, if $\overline{EA}$ is connected to V_{CC}, program fetches to addresses 0000H through FFFH are directed to internal memory and fetches to addresses 1000H through FFFFH are directed to external memory.

l Memory

The AT89S51 implements 128 bytes of on-chip RAM. The 128 bytes are accessible via direct and indirect addressing modes. Stack operations are examples of indirect addressing, so the 128 bytes of data RAM are available as stack space.

chdog er e-time bled with et-out)

The WDT is intended as a recovery method in situations where the CPU may be subjected to software upsets. The WDT consists of a 14-bit counter and the Watchdog Timer Reset (WDTRST) SFR. The WDT is defaulted to disable from exiting reset. To enable the WDT, a user must write 01EH and 0E1H in sequence to the WDTRST register (SFR location 0A6H). When the WDT is enabled, it will increment every machine cycle while the oscillator is running. The WDT timeout period is dependent on the external clock frequency. There is no way to disable the WDT except through reset (either hardware reset or WDT overflow reset). When WDT overflows, it will drive an output RESET HIGH pulse at the RST pin.

ng the WDT

To enable the WDT, a user must write 01EH and 0E1H in sequence to the WDTRST register (SFR location 0A6H). When the WDT is enabled, the user needs to service it by writing 01EH and 0E1H to WDTRST to avoid a WDT overflow. The 14-bit counter overflows when it reaches 16383 (3FFFH), and this will reset the device. When the WDT is enabled, it will increment every machine cycle while the oscillator is running. This means the user must reset the WDT at least every 16383 machine cycles. To reset the WDT the user must write 01EH and 0E1H to WDTRST. WDTRST is a write-only register. The WDT counter cannot be read or written. When WDT overflows, it will generate an output RESET pulse at the RST pin. The RESET pulse duration is 98xTOSC, where TOSC=1/FOSC. To make the best use of the WDT, it

should be serviced in those sections of code that will periodically be executed within the time required to prevent a WDT reset.

T During ver-down l Idle

In Power-down mode the oscillator stops, which means the WDT also stops. While in Power-down mode, the user does not need to service the WDT. There are two methods of exiting Power-down mode: by a hardware reset or via a level-activated external interrupt, which is enabled prior to entering Power-down mode. When Power-down is exited with hardware reset, servicing the WDT should occur as it normally does whenever the AT89S51 is reset. Exiting Power-down with an interrupt is significantly different. The interrupt is held low long enough for the oscillator to stabilize. When the interrupt is brought high, the interrupt is serviced. To prevent the WDT from resetting the device while the interrupt pin is held low, the WDT is not started until the interrupt is pulled high. It is suggested that the WDT be reset during the interrupt service for the interrupt used to exit Power-down mode.

To ensure that the WDT does not overflow within a few states of exiting Power-down, it is best to reset the WDT just before entering Power-down mode.

Before going into the IDLE mode, the WDIDLE bit in SFR AUXR is used to determine whether the WDT continues to count if enabled. The WDT keeps counting during IDLE (WDIDLE bit = 0) as the default state. To prevent the WDT from resetting the AT89S51 while in IDLE mode, the user should always set up a timer that will periodically exit IDLE, service the WDT, and reenter IDLE mode.

With WDIDLE bit enabled, the WDT will stop to count in IDLE mode and resumes the count upon exit from IDLE.

RT

The UART in the AT89S51 operates the same way as the UART in the AT89C51. For further information on the UART operation, refer to the ATMEL Web site (http://www.atmel.com). From the home page, select 'Products', then '8051-Architecture Flash Microcontroller', then 'Product Overview'.

er 0 and 1

Timer 0 and Timer 1 in the AT89S51 operate the same way as Timer 0 and Timer 1 in the AT89C51. For further information on the timers' operation, refer to the ATMEL Web site (http://www.atmel.com). From the home page, select 'Products', then '8051-Architecture Flash Microcontroller', then 'Product Overview'.

rrupts

The AT89S51 has a total of five interrupt vectors: two external interrupts ($\overline{INT0}$ and $\overline{INT1}$), two timer interrupts (Timers 0 and 1), and the serial port interrupt. These interrupts are all shown in Figure 1.

Each of these interrupt sources can be individually enabled or disabled by setting or clearing a bit in Special Function Register IE. IE also contains a global disable bit, EA, which disables all interrupts at once.

Note that Table 4 shows that bit position IE.6 is unimplemented. In the AT89S51, bit position IE.5 is also unimplemented. User software should not write 1s to these bit positions, since they may be used in future AT89 products.

The Timer 0 and Timer 1 flags, TF0 and TF1, are set at S5P2 of the cycle in which the timers overflow. The values are then polled by the circuitry in the next cycle

Table 4. Interrupt Enable (IE) Register

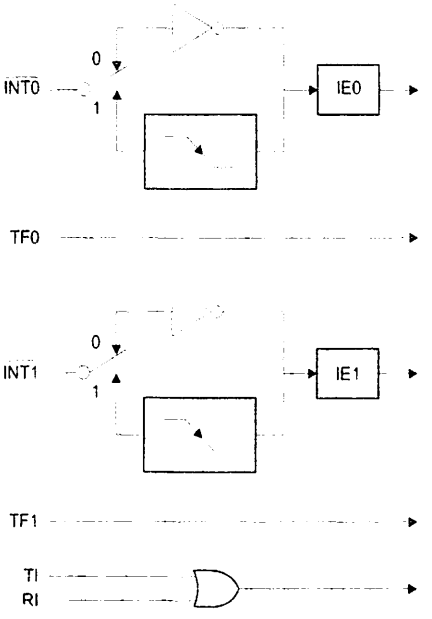
(MSB)							(LSB)
EA	–	–	ES	ET1	EX1	ET0	EX0

Enable Bit = 1 enables the interrupt.

Enable Bit = 0 disables the interrupt.

Symbol	Position	Function
EA	IE.7	Disables all interrupts. If EA = 0, no interrupt is acknowledged. If EA = 1, each interrupt source is individually enabled or disabled by setting or clearing its enable bit.
–	IE.6	Reserved
–	IE.5	Reserved
ES	IE.4	Serial Port interrupt enable bit
ET1	IE.3	Timer 1 interrupt enable bit
EX1	IE.2	External interrupt 1 enable bit
ET0	IE.1	Timer 0 interrupt enable bit
EX0	IE.0	External interrupt 0 enable bit
User software should never write 1s to reserved bits, because they may be used in future AT89 products.		

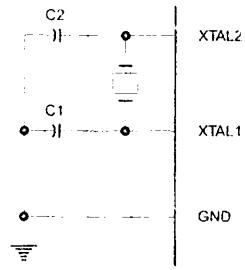
Figure 1. Interrupt Sources



cillator aracteristics

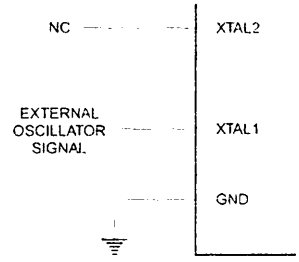
XTAL1 and XTAL2 are the input and output, respectively, of an inverting amplifier that can be configured for use as an on-chip oscillator, as shown in Figure 2. Either a quartz crystal or ceramic resonator may be used. To drive the device from an external clock source, XTAL2 should be left unconnected while XTAL1 is driven, as shown in Figure 3. There are no requirements on the duty cycle of the external clock signal, since the input to the internal clocking circuitry is through a divide-by-two flip-flop, but minimum and maximum voltage high and low time specifications must be observed.

Figure 2. Oscillator Connections



Note: C1, C2 = 30 pF ± 10 pF for Crystals = 40 pF ± 10 pF for Ceramic Resonators

Figure 3. External Clock Drive Configuration



Mode

In idle mode, the CPU puts itself to sleep while all the on-chip peripherals remain active. The mode is invoked by software. The content of the on-chip RAM and all the special function registers remain unchanged during this mode. The idle mode can be terminated by any enabled interrupt or by a hardware reset.

Note that when idle mode is terminated by a hardware reset, the device normally resumes program execution from where it left off, up to two machine cycles before the internal reset algorithm takes control. On-chip hardware inhibits access to internal RAM in this event, but access to the port pins is not inhibited. To eliminate the possibility of an unexpected write to a port pin when idle mode is terminated by a reset, the instruction following the one that invokes idle mode should not write to a port pin or to external memory.

ver-down de

In the Power-down mode, the oscillator is stopped, and the instruction that invokes Power-down is the last instruction executed. The on-chip RAM and Special Function Registers retain their values until the Power-down mode is terminated. Exit from Power-down mode can be initiated either by a hardware reset or by activation of an enabled external interrupt into $\overline{INT0}$ or $\overline{INT1}$. Reset redefines the SFRs but does not change the on-chip RAM. The reset should not be activated before V_{CC} is restored to its normal operating level and must be held active long enough to allow the oscillator to restart and stabilize.

Table 5. Status of External Pins During Idle and Power-down Modes

Mode	Program Memory	ALE	$\overline{PSEN}$	PORT0	PORT1	PORT2	PORT3
Idle	Internal	1	1	Data	Data	Data	Data
Idle	External	1	1	Float	Data	Address	Data
Power-down	Internal	0	0	Data	Data	Data	Data
Power-down	External	0	0	Float	Data	Data	Data

gram mory Lock s

The AT89S51 has three lock bits that can be left unprogrammed (U) or can be programmed (P) to obtain the additional features listed in the following table.

Table 6. Lock Bit Protection Modes

Program Lock Bits				
	LB1	LB2	LB3	Protection Type
1	U	U	U	No program lock features
2	P	U	U	MOVC instructions executed from external program memory are disabled from fetching code bytes from internal memory, $\overline{EA}$ is sampled and latched on reset, and further programming of the Flash memory is disabled
3	P	P	U	Same as mode 2, but verify is also disabled
4	P	P	P	Same as mode 3, but external execution is also disabled

When lock bit 1 is programmed, the logic level at the $\overline{EA}$ pin is sampled and latched during reset. If the device is powered up without a reset, the latch initializes to a random value and holds that value until reset is activated. The latched value of $\overline{EA}$ must agree with the current logic level at that pin in order for the device to function properly.

gramming Flash – allel Mode

The AT89S51 is shipped with the on-chip Flash memory array ready to be programmed. The programming interface needs a high-voltage (12-volt) program enable signal and is compatible with conventional third-party Flash or EPROM programmers.

The AT89S51 code memory array is programmed byte-by-byte.

Programming Algorithm: Before programming the AT89S51, the address, data, and control signals should be set up according to the Flash programming mode table and Figures 13 and 14. To program the AT89S51, take the following steps:

1. Input the desired memory location on the address lines.
2. Input the appropriate data byte on the data lines.
3. Activate the correct combination of control signals.
4. Raise $\overline{EA}/V_{PP}$ to 12V.
5. Pulse ALE/$\overline{PROG}$ once to program a byte in the Flash array or the lock bits. The byte-write cycle is self-timed and typically takes no more than 50 µs. Repeat steps 1 through 5, changing the address and data for the entire array or until the end of the object file is reached.

$\overline{Data}$ Polling: The AT89S51 features $\overline{Data}$ Polling to indicate the end of a byte write cycle. During a write cycle, an attempted read of the last byte written will result in the complement of the written data on P0.7. Once the write cycle has been completed, true data is valid on all outputs, and the next cycle may begin. $\overline{Data}$ Polling may begin any time after a write cycle has been initiated.

Ready/$\overline{\text{Busy}}$: The progress of byte programming can also be monitored by the RDY/$\overline{\text{BSY}}$ output signal. P3.0 is pulled low after ALE goes high during programming to indicate $\overline{\text{BUSY}}$. P3.0 is pulled high again when programming is done to indicate READY.

Program Verify: If lock bits LB1 and LB2 have not been programmed, the programmed code data can be read back via the address and data lines for verification. The status of the individual lock bits can be verified directly by reading them back.

Reading the Signature Bytes: The signature bytes are read by the same procedure as a normal verification of locations 000H, 100H, and 200H, except that P3.6 and P3.7 must be pulled to a logic low. The values returned are as follows.

(000H) = 1EH indicates manufactured by Atmel
(100H) = 51H indicates 89S51
(200H) = 06H

Chip Erase: In the parallel programming mode, a chip erase operation is initiated by using the proper combination of control signals and by pulsing ALE/$\overline{\text{PROG}}$ low for a duration of 200 ns - 500 ns.

In the serial programming mode, a chip erase operation is initiated by issuing the Chip Erase instruction. In this mode, chip erase is self-timed and takes about 500 ms.

During chip erase, a serial read from any address location will return 00H at the data output.

gramming Flash – ial Mode

The Code memory array can be programmed using the serial ISP interface while RST is pulled to V_{CC}. The serial interface consists of pins SCK, MOSI (input) and MISO (output). After RST is set high, the Programming Enable instruction needs to be executed first before other operations can be executed. Before a reprogramming sequence can occur, a Chip Erase operation is required.

The Chip Erase operation turns the content of every memory location in the Code array into FFH.

Either an external system clock can be supplied at pin XTAL1 or a crystal needs to be connected across pins XTAL1 and XTAL2. The maximum serial clock (SCK) frequency should be less than 1/16 of the crystal frequency. With a 33 MHz oscillator clock, the maximum SCK frequency is 2 MHz.

al ıramming ıithm

To program and verify the AT89S51 in the serial programming mode, the following sequence is recommended:

1. Power-up sequence:
   Apply power between VCC and GND pins.
   Set RST pin to "H".
   If a crystal is not connected across pins XTAL1 and XTAL2, apply a 3 MHz to 33 MHz clock to XTAL1 pin and wait for at least 10 milliseconds.
2. Enable serial programming by sending the Programming Enable serial instruction to pin MOSI/P1.5. The frequency of the shift clock supplied at pin SCK/P1.7 needs to be less than the CPU clock at XTAL1 divided by 16.
3. The Code array is programmed one byte at a time in either the Byte or Page mode. The write cycle is self-timed and typically takes less than 0.5 ms at 5V.
4. Any memory location can be verified by using the Read instruction that returns the content at the selected address at serial output MISO/P1.6.
5. At the end of a programming session, RST can be set low to commence normal device operation.

Power-off sequence (if needed):

Set XTAL1 to "L" (if a crystal is not used).

Set RST to "L".

Turn V_{CC} power off.

Data Polling: The Data Polling feature is also available in the serial mode. In this mode, during a write cycle an attempted read of the last byte written will result in the complement of the MSB of the serial output byte on MISO.

al gramming ruction Set

The Instruction Set for Serial Programming follows a 4-byte protocol and is shown in Table 8 on page 18.

gramming rface – allel Mode

Every code byte in the Flash array can be programmed by using the appropriate combination of control signals. The write operation cycle is self-timed and once initiated, will automatically time itself to completion.

All major programming vendors offer worldwide support for the Atmel microcontroller series. Please contact your local programming vendor for the appropriate software revision.

e 7. Flash Programming Modes

e	V_{CC}	RST	PSEN	ALE/ PROG	EA/ V_{PP}	P2.6	P2.7	P3.3	P3.6	P3.7	P0.7-0 Data	P2.3-0 Address	P1.7-0 Address
e Code Data	5V	H	L	(2)	12V	L	H	H	H	H	D_{IN}	A11-8	A7-0
d Code Data	5V	H	L	H	H	L	L	L	H	H	D_{OUT}	A11-8	A7-0
e Lock Bit 1	5V	H	L	(3)	12V	H	H	H	H	H	X	X	X
e Lock Bit 2	5V	H	L	(3)	12V	H	H	H	L	L	X	X	X
e Lock Bit 3	5V	H	L	(3)	12V	H	L	H	H	L	X	X	X
d Lock Bits 3	5V	H	L	H	H	H	H	L	H	L	P0.2, P0.3, P0.4	X	X
Erase	5V	H	L	(1)	12V	H	L	H	L	L	X	X	X
d Atmel ID	5V	H	L	H	H	L	L	L	L	L	1EH	0000	00H
d Device ID	5V	H	L	H	H	L	L	L	L	L	51H	0001	00H
d Device ID	5V	H	L	H	H	L	L	L	L	L	06H	0010	00H

:
1. Each PROG pulse is 200 ns - 500 ns for Chip Erase.
2. Each PROG pulse is 200 ns - 500 ns for Write Code Data.
3. Each PROG pulse is 200 ns - 500 ns for Write Lock Bits.
4. RDY/BSY signal is output on P3.0 during programming.
5. X = don't care.

Figure 4. Programming the Flash Memory (Parallel Mode)

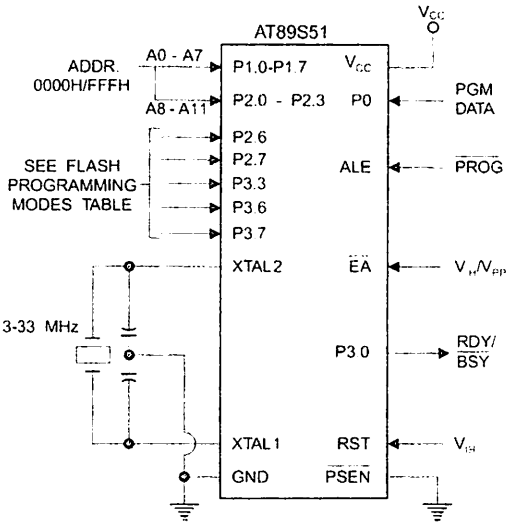
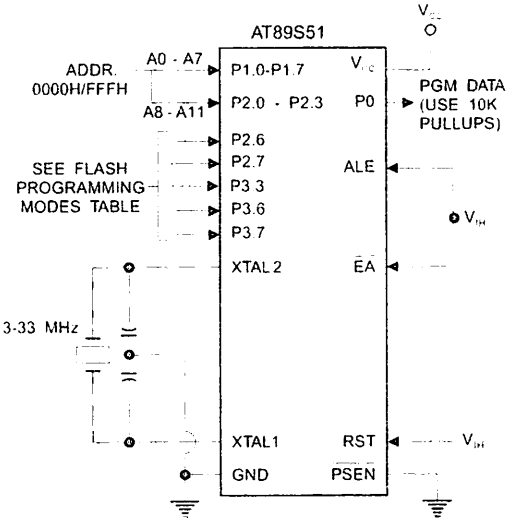


Figure 5. Verifying the Flash Memory (Parallel Mode)

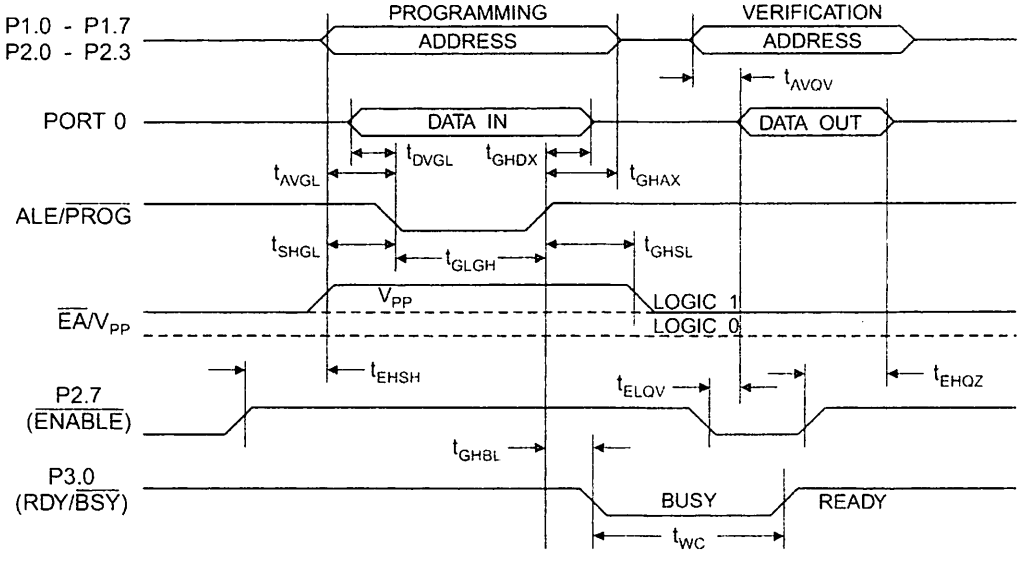


sh Programming and Verification Characteristics (Parallel Mode)

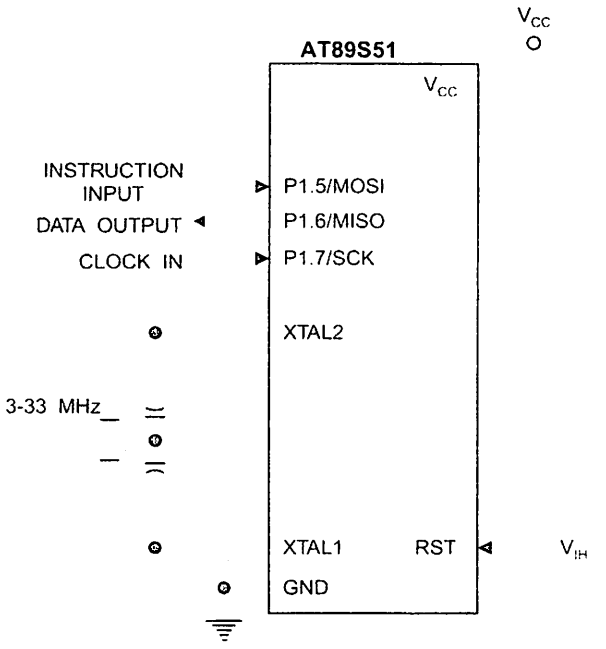
20°C to 30°C, V_{CC} = 4.5 to 5.5V

bol	Parameter	Min	Max	Units
	Programming Supply Voltage	11.5	12.5	V
	Programming Supply Current		10	mA
	V_{CC} Supply Current		30	mA
CL	Oscillator Frequency	3	33	MHz
L	Address Setup to $\overline{PROG}$ Low	$48t_{CLCL}$		
X	Address Hold After $\overline{PROG}$	$48t_{CLCL}$		
L	Data Setup to $\overline{PROG}$ Low	$48t_{CLCL}$		
X	Data Hold After $\overline{PROG}$	$48t_{CLCL}$		
H	P2.7 ($\overline{ENABLE}$) High to V_{PP}	$48t_{CLCL}$		
L	V_{PP} Setup to $\overline{PROG}$ Low	10		µs
L	V_{PP} Hold After $\overline{PROG}$	10		µs
H	$\overline{PROG}$ Width	0.2	1	µs
V	Address to Data Valid		$48t_{CLCL}$	
V	$\overline{ENABLE}$ Low to Data Valid		$48t_{CLCL}$	
Z	Data Float After $\overline{ENABLE}$	0	$48t_{CLCL}$	
L	$\overline{PROG}$ High to $\overline{BUSY}$ Low		1.0	µs
	Byte Write Cycle Time		50	µs

re 6. Flash Programming and Verification Waveforms – Parallel Mode

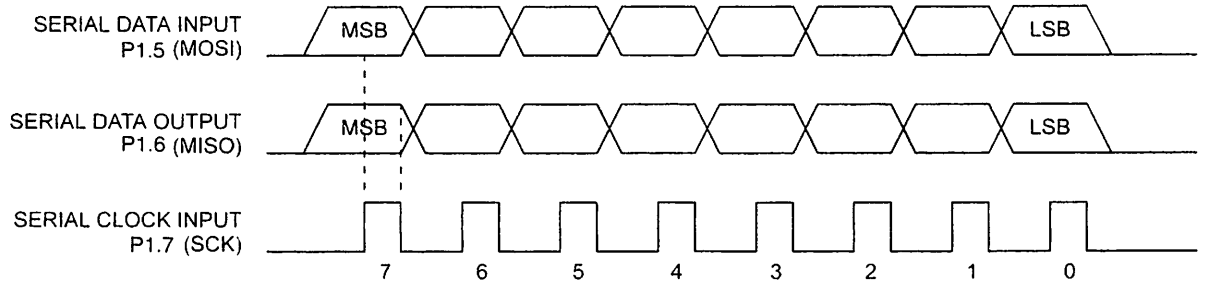


re 7. Flash Memory Serial Downloading



sh Programming and Verification Waveforms – Serial Mode

re 8. Serial Programming Waveforms



e 8. Serial Programming Instruction Set

ruction	Instruction Format Byte 1	Byte 2	Byte 3	Byte 4	Operation
gramming Enable	1010 1100	0101 0011	xxxx xxxx	xxxx xxxx 0110 1001 (Output)	Enable Serial Programming while RST is high
) Erase	1010 1100	100x xxxx	xxxx xxxx	xxxx xxxx	Chip Erase Flash memory array
d Program Memory e Mode)	0010 0000	xxxx A11 A10 A9 A8	A7 A6 A5 A4 A3 A2 A1 A0	D7 D6 D5 D4 D3 D2 D1 D0	Read data from Program memory in the byte mode
e Program Memory e Mode)	0100 0000	xxxx A11 A10 A9 A8	A7 A6 A5 A4 A3 A2 A1 A0	D7 D6 D5 D4 D3 D2 D1 D0	Write data to Program memory in the byte mode
e Lock Bits[2]	1010 1100	1110 00 B1 B2	xxxx xxxx	xxxx xxxx	Write Lock bits. See Note (2).
d Lock Bits	0010 0100	xxxx xxxx	xxxx xxxx	xx LB3 LB2 LB1 xx	Read back current status of the lock bits (a programmed lock bit reads back as a "1")
d Signature Bytes[1]	0010 1000	xxx A5 A4 A3 A2 A1	A0 xxx xxxx	Signature Byte	Read Signature Byte
d Program Memory ge Mode)	0011 0000	xxxx A11 A10 A9 A8	Byte 0	Byte 1... Byte 255	Read data from Program memory in the Page Mode (256 bytes)
e Program Memory ge Mode)	0101 0000	xxxx A11 A10 A9 A8	Byte 0	Byte 1... Byte 255	Write data to Program memory in the Page Mode (256 bytes)

1. The signature bytes are not readable in Lock Bit Modes 3 and 4.
2. B1 = 0, B2 = 0 → Mode 1, no lock protection
   B1 = 0, B2 = 1 → Mode 2, lock bit 1 activated
   B1 = 1, B2 = 0 → Mode 3, lock bit 2 activated
   B1 = 1, B1 = 1 → Mode 4, lock bit 3 activated

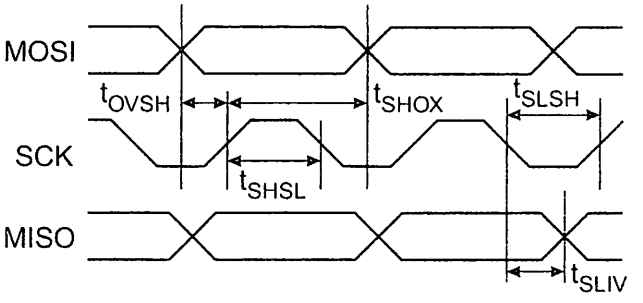
   } Each of the lock bits needs to be activated sequentially before Mode 4 can be executed.

After Reset signal is high, SCK should be low for at least 64 system clocks before it goes high to clock in the enable data bytes. No pulsing of Reset signal is necessary. SCK should be no faster than 1/16 of the system clock at XTAL1.

For Page Read/Write, the data always starts from byte 0 to 255. After the command byte and upper address byte are latched, each byte thereafter is treated as data until all 256 bytes are shifted in/out. Then the next instruction will be ready to be decoded.

ırial Programming Characteristics

ıure 9. Serial Programming Timing



ıle 9. Serial Programming Characteristics, T_A = -40° C to 85° C, V_{CC} = 4.0 - 5.5V (Unless Otherwise Noted)

ymbol	Parameter	Min	Typ	Max	Units
t_{CLCL}	Oscillator Frequency	0		33	MHz
LCL	Oscillator Period	30			ns
HSL	SCK Pulse Width High	8 t_{CLCL}			ns
LSH	SCK Pulse Width Low	8 t_{CLCL}			ns
VSH	MOSI Setup to SCK High	t_{CLCL}			ns
HOX	MOSI Hold after SCK High	2 t_{CLCL}			ns
LIV	SCK Low to MISO Valid	10	16	32	ns
RASE	Chip Erase Instruction Cycle Time			500	ms
WC	Serial Byte Write Cycle Time			64 t_{CLCL} + 400	µs

solute Maximum Ratings*

rating Temperature	-55°C to +125°C
age Temperature	-65°C to +150°C
age on Any Pin Respect to Ground	-1.0V to +7.0V
imum Operating Voltage	6.6V
Output Current	15.0 mA

*NOTICE: Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Characteristics

Values shown in this table are valid for T_A = -40°C to 85°C and V_{CC} = 4.0V to 5.5V, unless otherwise noted.

Symbol	Parameter	Condition	Min	Max	Units
	Input Low Voltage	(Except $\overline{EA}$)	-0.5	0.2 V_{CC}-0.1	V
	Input Low Voltage ($\overline{EA}$)		-0.5	0.2 V_{CC}-0.3	V
	Input High Voltage	(Except XTAL1, RST)	0.2 V_{CC}+0.9	V_{CC}+0.5	V
	Input High Voltage	(XTAL1, RST)	0.7 V_{CC}	V_{CC}+0.5	V
	Output Low Voltage[1] (Ports 1,2,3)	I_{OL} = 1.6 mA		0.45	V
	Output Low Voltage[1] (Port 0, ALE, $\overline{PSEN}$)	I_{OL} = 3.2 mA		0.45	V
	Output High Voltage (Ports 1,2,3, ALE, $\overline{PSEN}$)	I_{OH} = -60 µA, V_{CC} = 5V ±10%	2.4		V
		I_{OH} = -25 µA	0.75 V_{CC}		V
		I_{OH} = -10 µA	0.9 V_{CC}		V
I	Output High Voltage (Port 0 in External Bus Mode)	I_{OH} = -800 µA, V_{CC} = 5V ±10%	2.4		V
		I_{OH} = -300 µA	0.75 V_{CC}		V
		I_{OH} = -80 µA	0.9 V_{CC}		V
	Logical 0 Input Current (Ports 1,2,3)	V_{IN} = 0.45V		-50	µA
	Logical 1 to 0 Transition Current (Ports 1,2,3)	V_{IN} = 2V, V_{CC} = 5V ±10%		-650	µA
	Input Leakage Current (Port 0, $\overline{EA}$)	0.45 < V_{IN} < V_{CC}		±10	µA
ST	Reset Pulldown Resistor		50	300	KΩ
	Pin Capacitance	Test Freq. = 1 MHz, T_A = 25°C		10	pF
	Power Supply Current	Active Mode, 12 MHz		25	mA
		Idle Mode, 12 MHz		6.5	mA
	Power-down Mode[2]	V_{CC} = 5.5V		50	µA

1. Under steady state (non-transient) conditions, I_{OL} must be externally limited as follows:
   Maximum I_{OL} per port pin: 10 mA
   Maximum I_{OL} per 8-bit port:
   Port 0: 26 mA Ports 1, 2, 3: 15 mA
   Maximum total I_{OL} for all output pins: 71 mA
   If I_{OL} exceeds the test condition, V_{OL} may exceed the related specification. Pins are not guaranteed to sink current greater than the listed test conditions.
2. Minimum V_{CC} for Power-down is 2V.

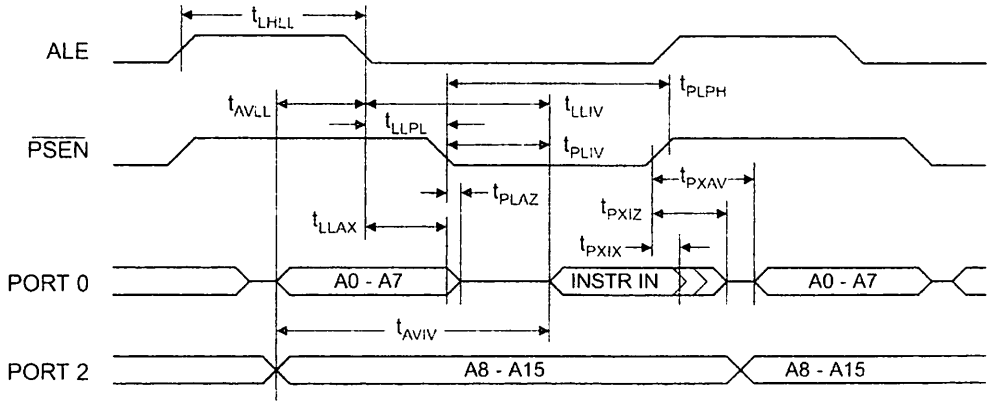
Characteristics

ır operating conditions, load capacitance for Port 0, ALE/$\overline{PROG}$, and $\overline{PSEN}$ = 100 pF; load capacitance for all other ıts = 80 pF.

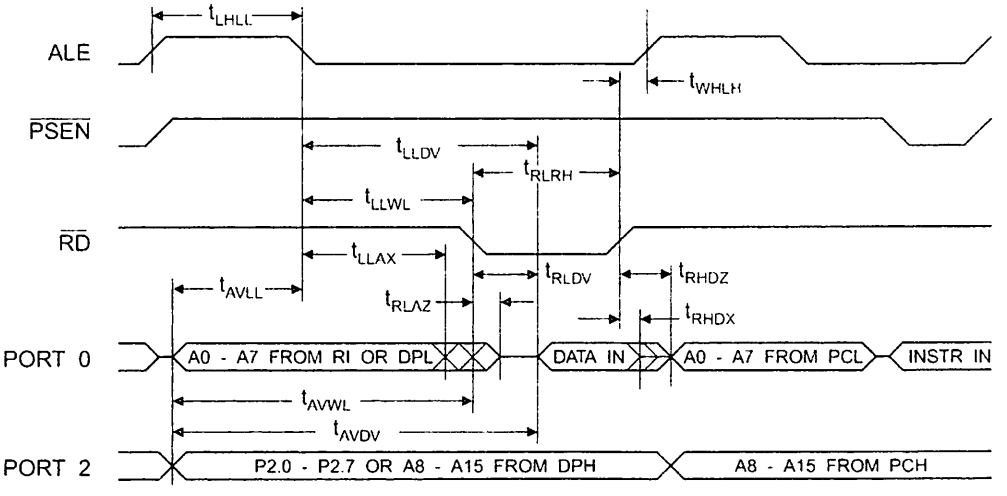
ernal Program and Data Memory Characteristics

ıbol	Parameter	12 MHz Oscillator		Variable Oscillator		Units
		Min	Max	Min	Max	
.CL	Oscillator Frequency			0	33	MHz
	ALE Pulse Width	127		$2t_{CLCL}$-40		ns
	Address Valid to ALE Low	43		t_{CLCL}-25		ns
	Address Hold After ALE Low	48		t_{CLCL}-25		ns
	ALE Low to Valid Instruction In		233		$4t_{CLCL}$-65	ns
	ALE Low to $\overline{PSEN}$ Low	43		t_{CLCL}-25		ns
	$\overline{PSEN}$ Pulse Width	205		$3t_{CLCL}$-45		ns
	$\overline{PSEN}$ Low to Valid Instruction In		145		$3t_{CLCL}$-60	ns
	Input Instruction Hold After $\overline{PSEN}$	0		0		ns
	Input Instruction Float After $\overline{PSEN}$		59		t_{CLCL}-25	ns
	$\overline{PSEN}$ to Address Valid	75		t_{CLCL}-8		ns
	Address to Valid Instruction In		312		$5t_{CLCL}$-80	ns
	$\overline{PSEN}$ Low to Address Float		10		10	ns
	$\overline{RD}$ Pulse Width	400		$6t_{CLCL}$-100		ns
'H	$\overline{WR}$ Pulse Width	400		$6t_{CLCL}$-100		ns
	$\overline{RD}$ Low to Valid Data In		252		$5t_{CLCL}$-90	ns
X	Data Hold After $\overline{RD}$	0		0		ns
Z	Data Float After $\overline{RD}$		97		$2t_{CLCL}$-28	ns
	ALE Low to Valid Data In		517		$8t_{CLCL}$-150	ns
	Address to Valid Data In		585		$9t_{CLCL}$-165	ns
	ALE Low to $\overline{RD}$ or $\overline{WR}$ Low	200	300	$3t_{CLCL}$-50	$3t_{CLCL}$+50	ns
L	Address to $\overline{RD}$ or $\overline{WR}$ Low	203		$4t_{CLCL}$-75		ns
'X	Data Valid to $\overline{WR}$ Transition	23		t_{CLCL}-30		ns
'H	Data Valid to $\overline{WR}$ High	433		$7t_{CLCL}$-130		ns
IX	Data Hold After $\overline{WR}$	33		t_{CLCL}-25		ns
	$\overline{RD}$ Low to Address Float		0		0	ns
H	$\overline{RD}$ or $\overline{WR}$ High to ALE High	43	123	t_{CLCL}-25	t_{CLCL}+25	ns

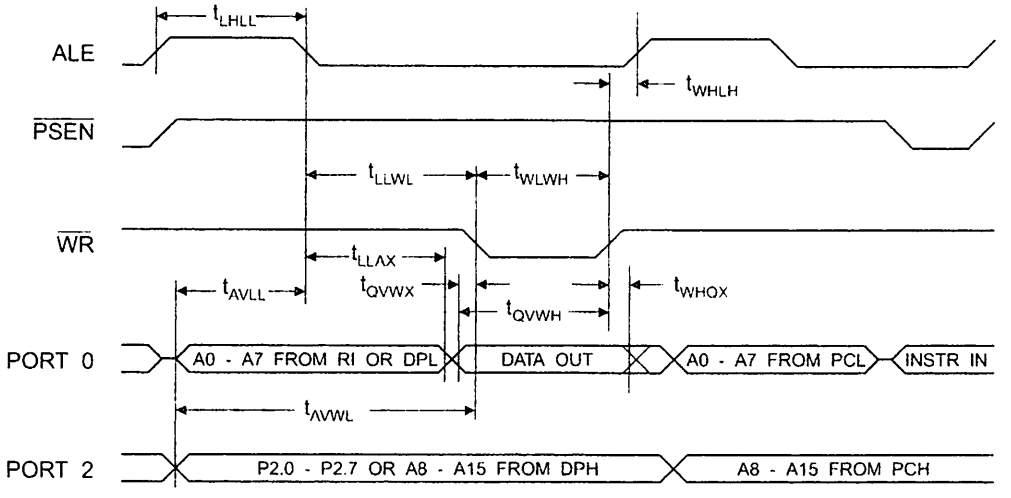
ernal Program Memory Read Cycle



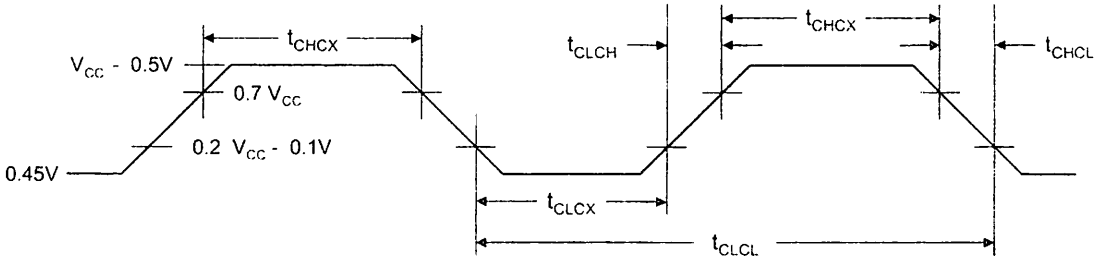
ernal Data Memory Read Cycle



ernal Data Memory Write Cycle



ernal Clock Drive Waveforms



ernal Clock Drive

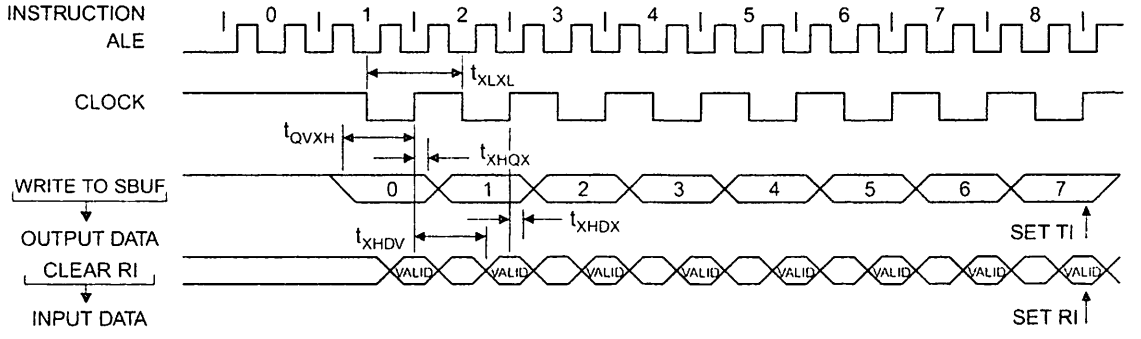
ıbol	Parameter	Min	Max	Units
CL	Oscillator Frequency	0	33	MHz
L	Clock Period	30		ns
X	High Time	12		ns
X	Low Time	12		ns
H	Rise Time		5	ns
L	Fall Time		5	ns

ial Port Timing: Shift Register Mode Test Conditions

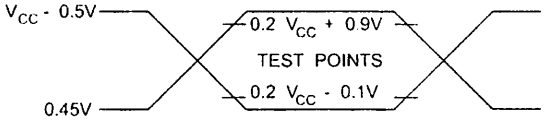
values in this table are valid for V_{CC} = 4.0V to 5.5V and Load Capacitance = 80 pF.

mbol	Parameter	12 MHz Osc		Variable Oscillator		Units
		Min	Max	Min	Max	
-	Serial Port Clock Cycle Time	1.0		$12t_{CLCL}$		µs
H	Output Data Setup to Clock Rising Edge	700		$10t_{CLCL}$-133		ns
X	Output Data Hold After Clock Rising Edge	50		$2t_{CLCL}$-80		ns
X	Input Data Hold After Clock Rising Edge	0		0		ns
V	Clock Rising Edge to Input Data Valid		700		$10t_{CLCL}$-133	ns

ft Register Mode Timing Waveforms

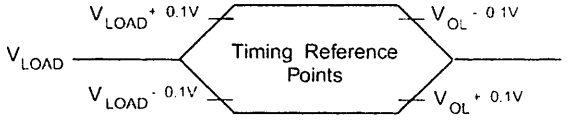


Testing Input/Output Waveforms[1]



1. AC Inputs during testing are driven at V_{CC} - 0.5V for a logic 1 and 0.45V for a logic 0. Timing measurements are made at V_{IH} min. for a logic 1 and V_{IL} max. for a logic 0.

at Waveforms[1]



1. For timing purposes, a port pin is no longer floating when a 100 mV change from load voltage occurs. A port pin begins to float when a 100 mV change from the loaded V_{OH}/V_{OL} level occurs.

lering Information

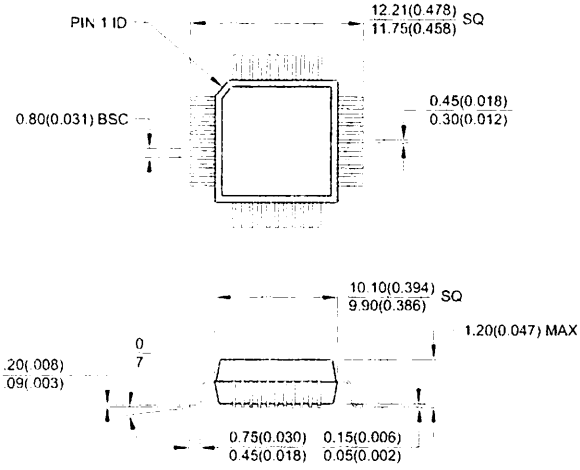
peed /Hz)	Power Supply	Ordering Code	Package	Operation Range
24	4.0V to 5.5V	AT89S51-24AC AT89S51-24JC AT89S51-24PC	44A 44J 40P6	Commercial (0° C to 70° C)
		AT89S51-24AI AT89S51-24JI AT89S51-24PI	44A 44J 40P6	Industrial (-40° C to 85° C)
33	4.5V to 5.5V	AT89S51-33AC AT89S51-33JC AT89S51-33PC	44A 44J 40P6	Commercial (0° C to 70° C)

☐ = Preliminary Availability

	Package Type
	44-lead, Thin Plastic Gull Wing Quad Flatpack (TQFP)
	44-lead, Plastic J-leaded Chip Carrier (PLCC)
6	40-pin, 0.600" Wide, Plastic Dual Inline Package (PDIP)

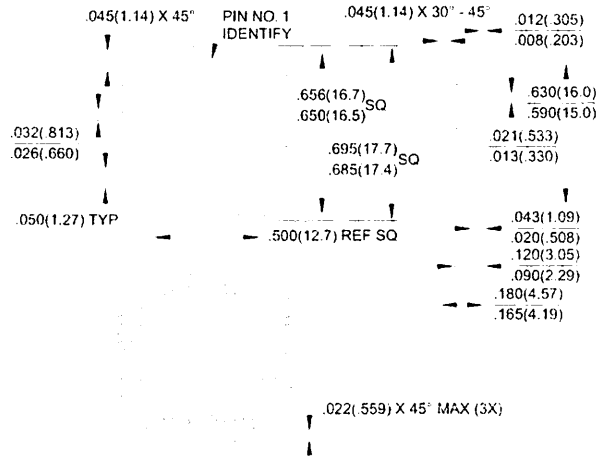
:kaging Information

4A, 44-lead, Thin (1.0 mm) Plastic Gull Wing Quad Flat Package (TQFP)
Dimensions in Millimeters and (Inches)*

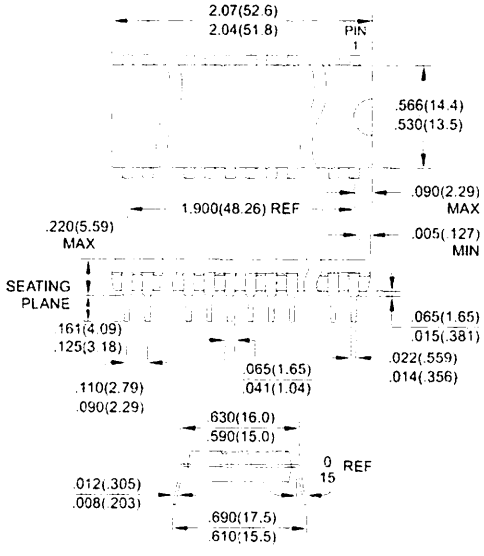


Controlling dimension: millimeters

44J, 44-lead, Plastic J-leaded Chip Carrier (PLCC)
Dimensions in Inches and (Millimeters)



0P6, 40-pin, 0.600" Wide, Plastic Dual Inline Package (PDIP)
Dimensions in Inches and (Millimeters)
JEDEC STANDARD MS-011 AC



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2487A–10/01/xM

R8C/13 Group

INGLE-CHIP 16-BIT CMOS MICROCOMPUTER

REJ03B0069-0110
Rev.1.10
Apr 27, 2005

1. Overview

This MCU is built using the high-performance silicon gate CMOS process using a R8C/Tiny Series CPU core and is packaged in a 32-pin plastic molded LQFP. This MCU operates using sophisticated instructions featuring a high level of instruction efficiency. With 1M bytes of address space, it is capable of executing instructions at high speed.
The data flash ROM (2 KB X 2 blocks) is embedded.

1.1 Applications

Electric household appliance, office equipment, housing equipment (sensor, security), general industrial equipment, audio, etc.

RENESAS

1.2 Performance Outline

Table 1.1. lists the performance outline of this MCU.

Table 1.1 Performance outline

Item		Performance
CPU	Number of basic instructions	89 instructions
	Shortest instruction execution time	50 ns (f(XIN) = 20 MHz, Vcc = 3.0 to 5.5 V) 100 ns (f(XIN) = 10 MHz, Vcc = 2.7 to 5.5 V)
	Operating mode	Single-chip
	Address space	1M bytes
	Memory capacity	See Table 1.2.
Peripheral function	Interrupt	Internal: 11 factors, External: 5 factors, Software: 4 factors, Priority level: 7 levels
	Watchdog timer	15 bits x 1 (with prescaler) Reset start function selectable
	Timer	Timer X: 8 bits x 1 channel, Timer Y: 8 bits x 1 channel, Timer Z: 8 bits x 1 channel (Each timer equipped with 8-bit prescaler) Timer C: 16 bits x 1 channel Circuits of input capture and output compare.
	Serial interface	•1 channel Clock synchronous, UART •1 channel UART
	A/D converter	10-bit A/D converter: 1 circuit, 12 channels
	Clock generation circuit	2 circuits •Main clock generation circuit (Equipped with a built-in feedback resistor) •On-chip oscillator (high-speed, low-speed) On high-speed on-chip oscillator the frequency adjustment function is usable.
	Oscillation stop detection function	Stop detection of main clock oscillation
	Voltage detection circuit	Included
	Power on reset circuit	Included
	Port	Input/Output: 22 (including LED drive port), Input: 2 (LED drive I/O port: 8)
Electrical characteristics	Power supply voltage	Vcc = 3.0 to 5.5V (f(XIN) = 20MHz) Vcc = 2.7 to 5.5V (f(XIN) = 10MHz)
	Power consumption	Typ.9 mA (Vcc = 5.0V, (f(XIN) = 20MHz,High-speed mode) Typ.5 mA (Vcc = 3.0V, (f(XIN) = 10MHz,High-speed mode) Typ.35 µA (Vcc = 3.0V, Wait mode, Peripheral clock stops) Typ.0.7 µA (Vcc = 3.0V, Stop mode)
Flash memory	Program/erase voltage	Vcc = 2.7 to 5.5 V
	Number of program/erase	10,000 times (Data area)
		1,000 times (Program area)
Operating ambient temperature		-20 to 85°C -40 to 85°C (D-version)
Package		32-pin plastic mold LQFP

1.3 Block Diagram

Figure 1.1 shows this MCU block diagram.

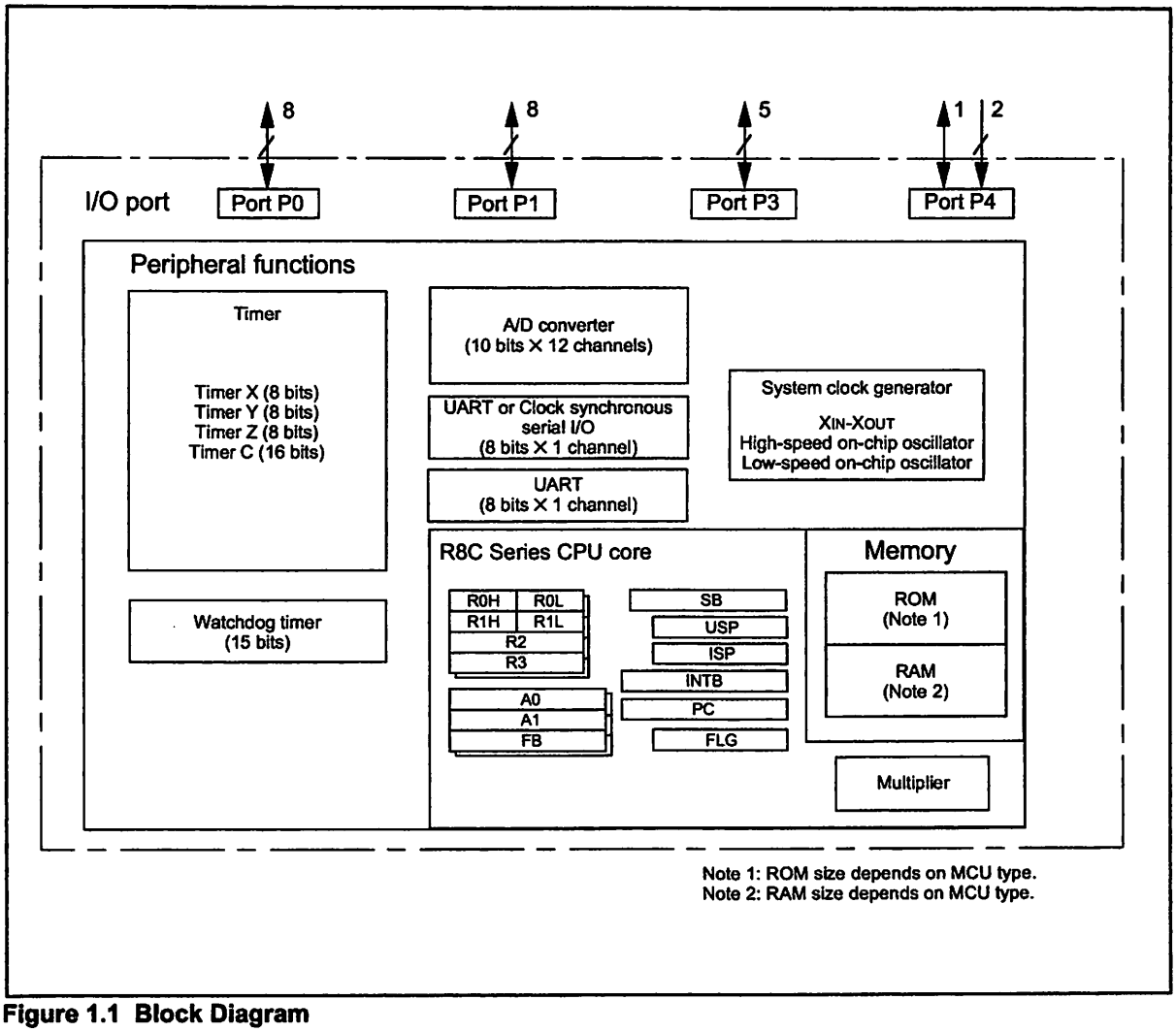


Figure 1.1 Block Diagram

1.4 Product Information

Table 1.2 lists the products.

Table 1.2 Product List

As of April 2005

Type No.	ROM capacity		RAM capacity	Package type	Remarks
	Program area	Data area			
R5F21132FP	8K bytes	2K bytes x 2	512 bytes	PLQP0032GB-A	Flash memory version
R5F21133FP	12K bytes	2K bytes x 2	768 bytes	PLQP0032GB-A	
R5F21134FP	16K bytes	2K bytes x 2	1K bytes	PLQP0032GB-A	
R5F21132DFP	8K bytes	2K bytes x 2	512 bytes	PLQP0032GB-A	D version
R5F21133DFP	12K bytes	2K bytes x 2	768 bytes	PLQP0032GB-A	
R5F21134DFP	16K bytes	2K bytes x 2	1K bytes	PLQP0032GB-A	

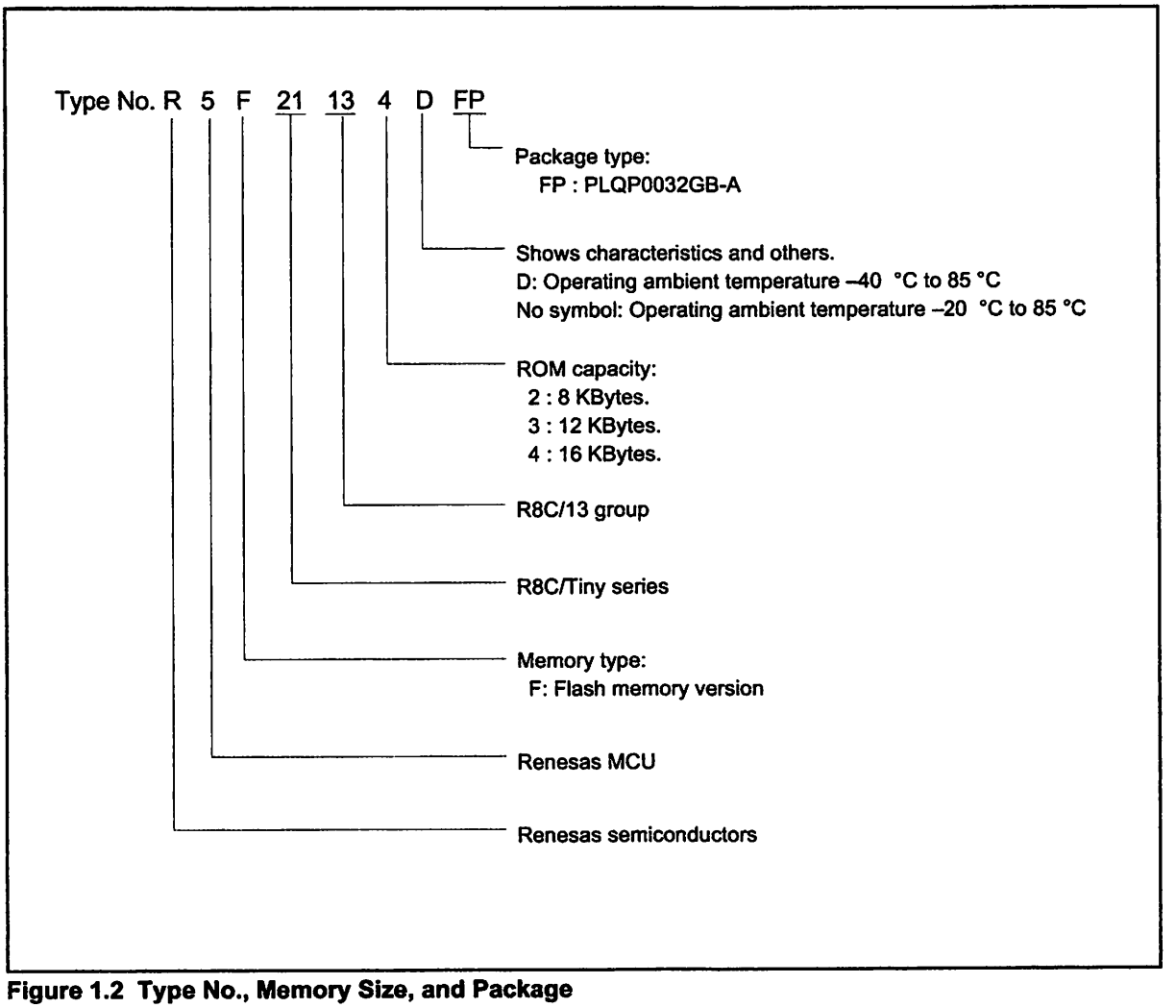


Figure 1.2 Type No., Memory Size, and Package

1.5 Pin Assignments

Figure 1.3 shows the pin configuration (top view).

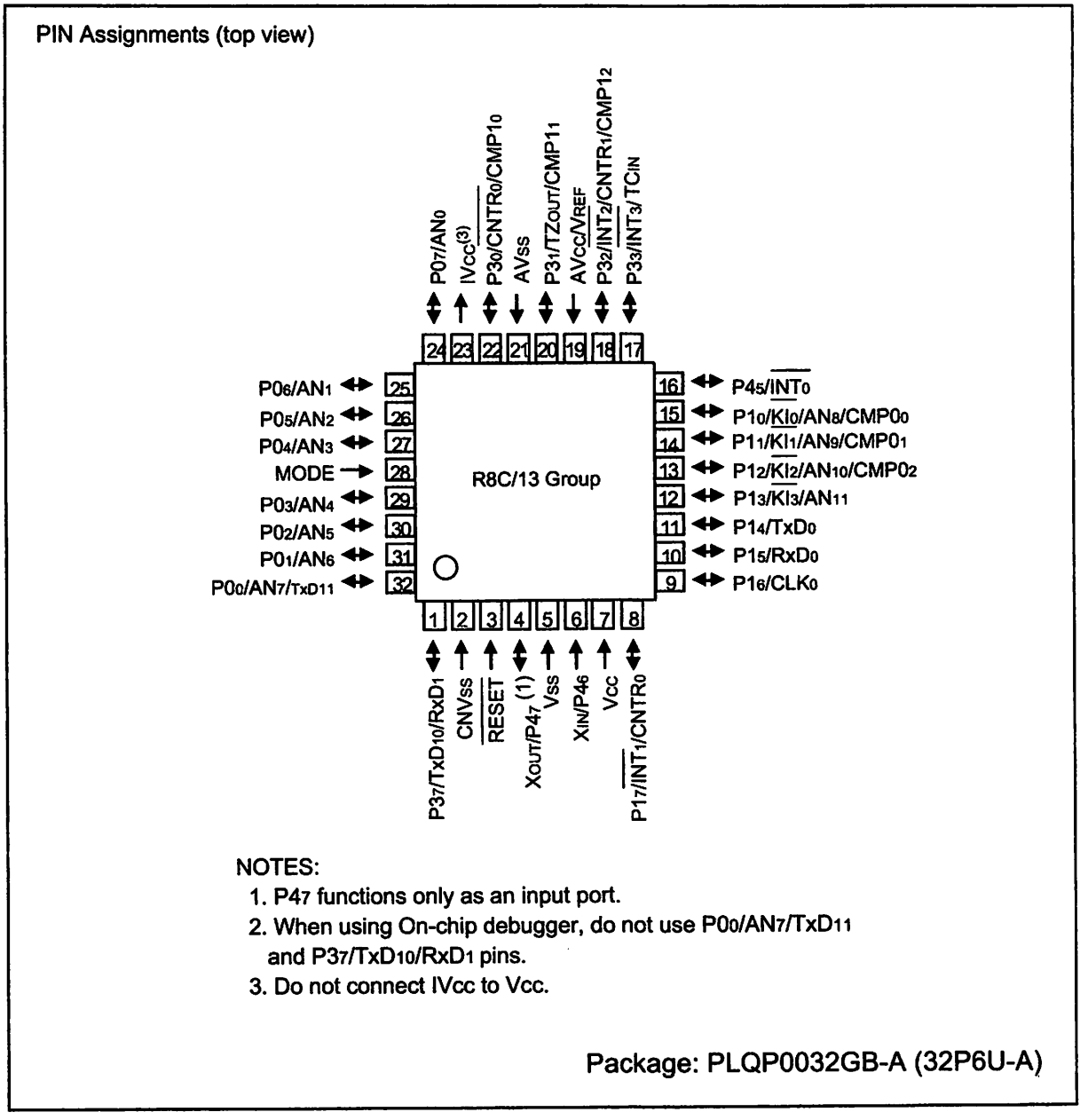


Figure 1.3 Pin Assignments (Top View)

1.6 Pin Description

Table 1.3 shows the pin description

Table 1.3 Pin description

Signal name	Pin name	I/O type	Function
Power supply input	Vcc, Vss	I	Apply 2.7 V to 5.5 V to the Vcc pin. Apply 0 V to the Vss pin.
IVcc	IVcc	O	This pin is to stabilize internal power supply Connect this pin to Vss via a capacitor (0.1 μF) Do not connect to Vcc
Analog power supply input	AVcc, AVss	I	These are power supply input pins for A/D converter. Connect the AVcc pin to Vcc. Connect the AVss pin to Vss. Connect a capacitor between pins AVcc and AVss.
Reset input	$\overline{\text{RESET}}$	I	"L" on this input resets the MCU.
CNVss	CNVss	I	Connect this pin to Vss via a resistor(1)
MODE	MODE	I	Connect this pin to Vcc via a resistor
Main clock input	XIN	I	These pins are provided for the main clock generating circuit I/O. Connect a ceramic resonator or a crystal oscillator between the XIN and XOUT pins. To use an externally derived clock, input it to the XIN pin and leave the XOUT pin open.
Main clock output	XOUT	O	
$\overline{\text{INT}}$ interrupt input	$\overline{\text{INT0}}$ to $\overline{\text{INT3}}$	I	These are $\overline{\text{INT}}$ interrupt input pins.
Key input interrupt input	$\overline{\text{KI0}}$ to $\overline{\text{KI3}}$	I	These are key input interrupt pins.
Timer X	CNTR0	I/O	This is the timer X I/O pin.
	$\overline{\text{CNTR0}}$	O	This is the timer X output pin.
Timer Y	CNTR1	I/O	This is the timer Y I/O pin.
Timer Z	$\overline{\text{TZOUT}}$	O	This is the timer Z output pin.
Timer C	TCIN	I	This is the timer C input pin.
	CMP00 to CMP03, CMP10 to CMP13	O	These are the timer C output pins.
Serial interface	CLK0	I/O	This is a transfer clock I/O pin.
	RxD0, RxD1	I	These are serial data input pins.
	TxD0, TxD10, TxD11	O	These are serial data output pins.
Reference voltage input	VREF	I	This is a reference voltage input pin for A/D converter. Connect the VREF pin to Vcc.
A/D converter	AN0 to AN11	I	These are analog input pins for A/D converter.
I/O port	P00 to P07, P10 to P17, P30 to P33, P37, P45	I/O	These are 8-bit CMOS I/O ports. Each port has an I/O select direction register, allowing each pin in that port to be directed for input or output individually. Any port set to input can select whether to use a pull-up resistor or not by program. P10 to P17 also function as LED drive ports.
Input port	P46, P47	I	These are input only pins.

2. Central Processing Unit (CPU)

Figure 2.1 shows the CPU registers. The CPU has 13 registers. Of these, R0, R1, R2, R3, A0, A1 and FB comprise a register bank. There are two register banks.

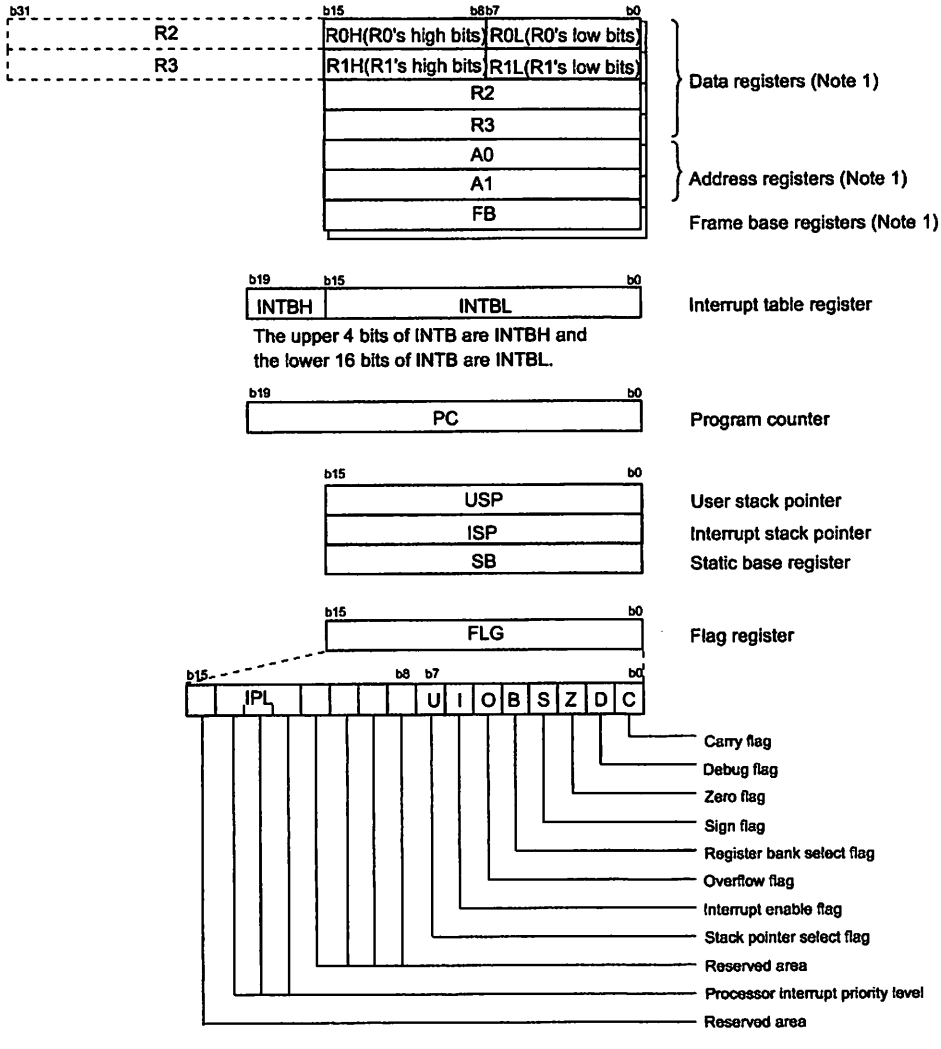


Figure 2.1 Central Processing Unit Register

2.1 Data Registers (R0, R1, R2 and R3)

The R0 register consists of 16 bits, and is used mainly for transfers and arithmetic/logic operations. R1 to R3 are the same as R0.

The R0 register can be separated between high (R0H) and low (R0L) for use as two 8-bit data registers. R1H and R1L are the same as R0H and R0L. Conversely, R2 and R0 can be combined for use as a 32-bit data register (R2R0). R3R1 is the same as R2R0.

2.2 Address Registers (A0 and A1)

The register A0 consists of 16 bits, and is used for address register indirect addressing and address register relative addressing. They also are used for transfers and logic/logic operations. A1 is the same as A0.

In some instructions, registers A1 and A0 can be combined for use as a 32-bit address register (A1A0).

2.3 Frame Base Register (FB)

FB is configured with 16 bits, and is used for FB relative addressing.

2.4 Interrupt Table Register (INTB)

INTB is configured with 20 bits, indicating the start address of an interrupt vector table.

2.5 Program Counter (PC)

PC is configured with 20 bits, indicating the address of an instruction to be executed.

2.6 User Stack Pointer (USP) and Interrupt Stack Pointer (ISP)

Stack pointer (SP) comes in two types: USP and ISP, each configured with 16 bits.

Your desired type of stack pointer (USP or ISP) can be selected by the U flag of FLG.

2.7 Static Base Register (SB)

SB is configured with 16 bits, and is used for SB relative addressing.

2.8 Flag Register (FLG)

FLG consists of 11 bits, indicating the CPU status.

2.8.1 Carry Flag (C Flag)

This flag retains a carry, borrow, or shift-out bit that has occurred in the arithmetic/logic unit.

2.8.2 Debug Flag (D Flag)

The D flag is used exclusively for debugging purpose. During normal use, it must be set to "0".

2.8.3 Zero Flag (Z Flag)

This flag is set to "1" when an arithmetic operation resulted in 0; otherwise, it is "0".

2.8.4 Sign Flag (S Flag)

This flag is set to "1" when an arithmetic operation resulted in a negative value; otherwise, it is "0".

2.8.5 Register Bank Select Flag (B Flag)

Register bank 0 is selected when this flag is "0" ; register bank 1 is selected when this flag is "1".

2.8.6 Overflow Flag (O Flag)

This flag is set to "1" when the operation resulted in an overflow; otherwise, it is "0".

2.8.7 Interrupt Enable Flag (I Flag)

This flag enables a maskable interrupt.

Maskable interrupts are disabled when the I flag is "0", and are enabled when the I flag is "1". The I flag is cleared to "0" when the interrupt request is accepted.

2.8.8 Stack Pointer Select Flag (U Flag)

ISP is selected when the U flag is "0"; USP is selected when the U flag is "1".

The U flag is cleared to "0" when a hardware interrupt request is accepted or an INT instruction for software interrupt Nos. 0 to 31 is executed.

2.8.9 Processor Interrupt Priority Level (IPL)

IPL is configured with three bits, for specification of up to eight processor interrupt priority levels from level 0 to level 7.

If a requested interrupt has priority greater than IPL, the interrupt is enabled.

2.8.10 Reserved Area

When write to this bit, write "0". When read, its content is indeterminate.

3. Memory

Figure 3.1 is a memory map of this MCU. The address space extends the 1M bytes from address 0000016 to FFFFF16.

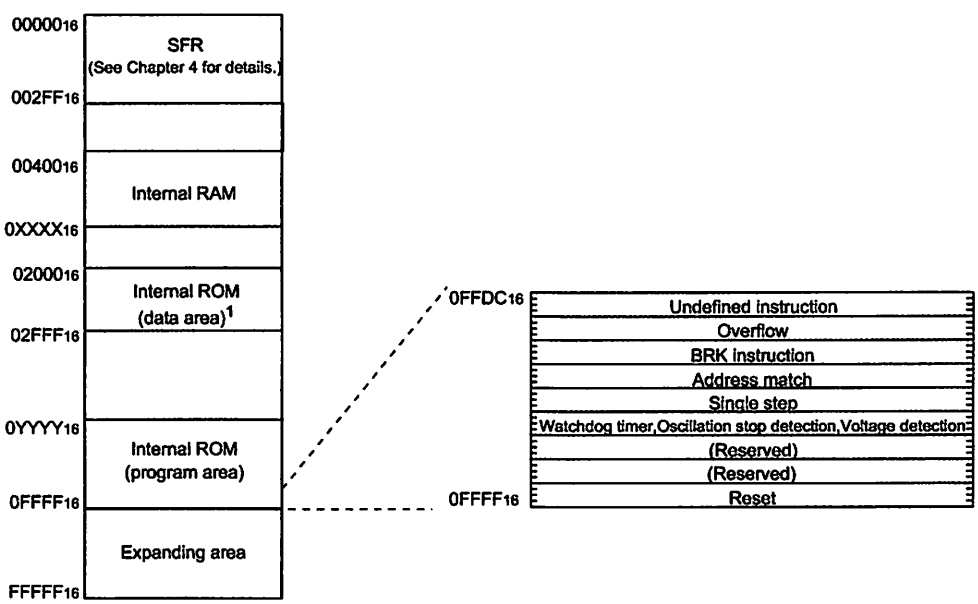
The internal ROM (program area) is allocated in a lower address direction beginning with address 0FFFF16. For example, a 16-Kbyte internal ROM is allocated to the addresses from 0C00016 to 0FFFF16.

The fixed interrupt vector table is allocated to the addresses from 0FFDC16 to 0FFFF16. Therefore, store the start address of each interrupt routine here.

The internal ROM (data area) is allocated to the addresses from 0200016 to 02FFF16.

The internal RAM is allocated in an upper address direction beginning with address 0040016. For example, a 1-Kbyte internal RAM is allocated to the addresses from 0040016 to 007FF16. In addition to storing data, the internal RAM also stores the stack used when calling subroutines and when interrupts are generated.

Special function registers (SFR) are allocated to the addresses from 0000016 to 002FF16. Peripheral function control registers are located here. Of the SFR, any space which has no functions allocated is reserved for future use and cannot be used by users.



NOTES:
1. The data flash ROM block A (2K bytes) and block B (2K bytes) are shown.
2. Blank spaces are reserved. No access is allowed.

Type name	Internal ROM		Internal RAM	
	Size	Address 0YYYY16	Size	Address 0XXXX16
R5F21134FP, R5F21134DFP	16K bytes	0C00016	1K bytes	007FF16
R5F21133FP, R5F21133DFP	12K bytes	0D00016	768 bytes	006FF16
R5F21132FP, R5F21132DFP	8K bytes	0E00016	512 bytes	005FF16

Figure 3.1 Memory Map

4. Special Function Register (SFR)

SFR(Special Function Register) is the control register of peripheral functions. Tables 4.1 to 4.4 list the SFR information

Table 4.1 SFR Information(1)(1)

Address	Register	Symbol	After reset
0000₁₆			
0001₁₆			
0002₁₆			
0003₁₆			
0004₁₆	Processor mode register 0 [1]	PM0	0016
0005₁₆	Processor mode register 1	PM1	0016
0006₁₆	System clock control register 0	CM0	011010002
0007₁₆	System clock control register 1	CM1	001000002
0008₁₆	High-speed on-chip oscillator control register 0	HR0	0016
0009₁₆	Address match interrupt enable register	AIER	XXXXXX002
000A₁₆	Protect register	PRCR	00XXX0002
000B₁₆	High-speed on-chip oscillator control register 1	HR1	4016
000C₁₆	Oscillation stop detection register	OCD	000001002
000D₁₆	Watchdog timer reset register	WDTR	XX16
000E₁₆	Watchdog timer start register	WDTS	XX16
000F₁₆	Watchdog timer control register	WDC	000111112
0010₁₆	Address match interrupt register 0	RMAD0	0016
0011₁₆			0016
0012₁₆			X016
0013₁₆			
0014₁₆	Address match interrupt register 1	RMAD1	0016
0015₁₆			0016
0016₁₆			X016
0017₁₆			
0018₁₆			
0019₁₆	Voltage detection register 1 [2]	VCR1	000010002
001A₁₆	Voltage detection register 2 [2]	VCR2	0016 [3] 100000002 [4]
001B₁₆			
001C₁₆			
001D₁₆			
001E₁₆	INT0 input filter select register	INT0F	XXXXX0002
001F₁₆	Voltage detection interrupt register [2]	D4INT	0016 [3] 010000012 [4]
0020₁₆			
0021₁₆			
0022₁₆			
0023₁₆			
0024₁₆			
0025₁₆			
0026₁₆			
0027₁₆			
0028₁₆			
0029₁₆			
002A₁₆			
002B₁₆			
002C₁₆			
002D₁₆			
002E₁₆			
002F₁₆			
0030₁₆			
0031₁₆			
0032₁₆			
0033₁₆			
0034₁₆			
0035₁₆			
0036₁₆			
0037₁₆			
0038₁₆			
0039₁₆			
003A₁₆			
003B₁₆			
003C₁₆			
003D₁₆			
003E₁₆			
003F₁₆			

X : Undefined

NOTES:

1. Blank columns are all reserved space. No access is allowed.
2. Software reset or the watchdog timer reset does not affect this register.
3. Owing to Reset input.
4. In the case of RESET pin = H retaining.

Table 4.2 SFR Information(2)[1]

Address	Register	Symbol	After reset
0040₁₆			
0041₁₆			
0042₁₆			
0043₁₆			
0044₁₆			
0045₁₆			
0046₁₆			
0047₁₆			
0048₁₆			
0049₁₆			
004A₁₆			
004B₁₆			
004C₁₆			
004D₁₆	Key input interrupt control register	KUPIC	XXXXX0002
004E₁₆	AD conversion interrupt control register	ADIC	XXXXX0002
004F₁₆			
0050₁₆	Compare 1 interrupt control register	CMP1IC	XXXXX0002
0051₁₆	UART0 transmit interrupt control register	S0TIC	XXXXX0002
0052₁₆	UART0 receive interrupt control register	S0RIC	XXXXX0002
0053₁₆	UART1 transmit interrupt control register	S1TIC	XXXXX0002
0054₁₆	UART1 receive interrupt control register	S1RIC	XXXXX0002
0055₁₆	INT2 interrupt control register	INT2IC	XXXXX0002
0056₁₆	Timer X interrupt control register	TXIC	XXXXX0002
0057₁₆	Timer Y interrupt control register	TYIC	XXXXX0002
0058₁₆	Timer Z interrupt control register	TZIC	XXXXX0002
0059₁₆	INT1 interrupt control register	INT1IC	XXXXX0002
005A₁₆	INT3 interrupt control register	INT3IC	XXXXX0002
005B₁₆	Timer C interrupt control register	TCIC	XXXXX0002
005C₁₆	Compare 0 interrupt control register	CMP0IC	XXXXX0002
005D₁₆	INT0 interrupt control register	INT0IC	XX00X0002
005E₁₆			
005F₁₆			
0060₁₆			
0061₁₆			
0062₁₆			
0063₁₆			
0064₁₆			
0065₁₆			
0066₁₆			
0067₁₆			
0068₁₆			
0069₁₆			
006A₁₆			
006B₁₆			
006C₁₆			
006D₁₆			
006E₁₆			
006F₁₆			
0070₁₆			
0071₁₆			
0072₁₆			
0073₁₆			
0074₁₆			
0075₁₆			
0076₁₆			
0077₁₆			
0078₁₆			
0079₁₆			
007A₁₆			
007B₁₆			
007C₁₆			
007D₁₆			
007E₁₆			
007F₁₆			

X : Undefined

NOTES:

1. Blank columns are all reserved space. No access is allowed.

Table 4.3 SFR Information(3)[1]

Address	Register	Symbol	After reset
008016	Timer Y, Z mode register	TYZMR	0016
008116	Prescaler Y	PREY	FF16
008216	Timer Y secondary	TYSC	FF16
008316	Timer Y primary	TYPR	FF16
008416	Timer Y, Z waveform output control register	PUM	0016
008516	Prescaler Z	PREZ	FF16
008616	Timer Z secondary	TZSC	FF16
008716	Timer Z primary	TZPR	FF16
008816			
008916			
008A16	Timer Y, Z output control register	TYZOC	0016
008B16	Timer X mode register	TXMR	0016
008C16	Prescaler X	PREX	FF16
008D16	Timer X register	TX	FF16
008E16	Count source set register	TCSS	0016
008F16			
009016 009116	Timer C register	TC	0016 0016
009216			
009316			
009416			
009516			
009616	External input enable register	INTEN	0016
009716			
009816	Key input enable register	KIEN	0016
009916			
009A16	Timer C control register 0	TCC0	0016
009B16	Timer C control register 1	TCC1	0016
009C16 009D16	Capture, compare 0 register	TM0	0016 0016[2]
009E16 009F16	Compare 1 register	TM1	FF16 FF16
00A016	UART0 transmit/receive mode register	U0MR	0016
00A116	UART0 bit rate register	U0BRG	XX16
00A216 00A316	UART0 transmit buffer register	U0TB	XX16 XX16
00A416	UART0 transmit/receive control register 0	U0C0	000010002
00A516	UART0 transmit/receive control register 1	U0C1	000000102
00A616 00A716	UART0 receive buffer register	U0RB	XX16 XX16
00A816	UART1 transmit/receive mode register	U1MR	0016
00A916	UART1 bit rate register	U1BRG	XX16
00AA16 00AB16	UART1 transmit buffer register	U1TB	XX16 XX16
00AC16	UART1 transmit/receive control register 0	U1C0	000010002
00AD16	UART1 transmit/receive control register 1	U1C1	000000102
00AE16 00AF16	UART1 receive buffer register	U1RB	XX16 XX16
00B016	UART transmit/receive control register 2	UCON	0016
00B116			
00B216			
00B316			
00B416			
00B516			
00B616			
00B716			
00B816			
00B916			
00BA16			
00BB16			
00BC16			
00BD16			
00BE16			
00BF16			

X : Undefined

NOTES:

1. Blank columns are all reserved space. No access is allowed.
2. When the output compare mode is selected (the TCC13 bit in the TCC1 register = 1), the value is set to FFFF16.

Table 4.4 SFR Information(4)(1)

Address	Register	Symbol	After reset
00C016	AD register	AD	XX16
00C116			XX16
00C216			
00C316			
00C416			
00C516			
00C616			
00C716			
00C816			
00C916			
00CA16			
00CB16			
00CC16			
00CD16			
00CE16			
00CF16			
00D016			
00D116			
00D216			
00D316			
00D416	AD control register 2	ADCON2	0016
00D516			
00D616	AD control register 0	ADCON0	00000XXX2
00D716	AD control register 1	ADCON1	0016
00D816			
00D916			
00DA16			
00DB16			
00DC16			
00DD16			
00DE16			
00DF16			
00E016	Port P0 register	P0	XX16
00E116	Port P1 register	P1	XX16
00E216	Port P0 direction register	PD0	0016
00E316	Port P1 direction register	PD1	0016
00E416			
00E516	Port P3 register	P3	XX16
00E616			
00E716	Port P3 direction register	PD3	0016
00E816	Port P4 register	P4	XX16
00E916			
00EA16	Port P4 direction register	PD4	0016
00EB16			
00EC16			
00ED16			
00EE16			
00EF16			
00F016			
00F116			
00F216			
00F316			
00F416			
00F516			
00F616			
00F716			
00F816			
00F916			
03FA16			
00FB16			
00FC16	Pull-up control register 0	PUR0	00XX00002
00FD16	Pull-up control register 1	PUR1	XXXXXX0X2
00FE16	Port P1 drive capacity control register	DRR	0016
00FF16	Timer C output control register	TCOUT	0016
≈			≈
01B316	Flash memory control register 4	FMR4	010000002
01B416			
01B516	Flash memory control register 1	FMR1	1000000X2
01B616			
01B716	Flash memory control register 0	FMR0	000000012

0FFFF16	Option function select register (2)	OFS	Note 2

X : Undefined

NOTES:

1. The blank areas, 010016 to 01B216 and 01B816 to 02FF16 are reserved and cannot be used by users.
2. The watchdog timer control bit is assigned. Refer to "Figure11.2 OFS, WDC, WDTR and WDTS registers" of Hardware Manual for details

5. Electrical Characteristics

Table 5.1 Absolute Maximum Ratings

Symbol	Parameter	Condition	Rated value	Unit
Vcc	Supply voltage	Vcc=AVcc	-0.3 to 6.5	V
AVcc	Analog supply voltage	Vcc=AVcc	-0.3 to 6.5	V
V_I	Input voltage		-0.3 to Vcc+0.3	V
Vo	Output voltage		-0.3 to Vcc+0.3	V
P_d	Power dissipation	Topr=25 °C	300	mW
T_{opr}	Operating ambient temperature		-20 to 85 / -40 to 85 (D version)	°C
T_{stg}	Storage temperature		-65 to 150	°C

Table 5.2 Recommended Operating Conditions

Symbol	Parameter		Conditions	Standard Min.	Standard Typ.	Standard Max.	Unit
Vcc	Supply voltage			2.7		5.5	V
AVcc	Analog supply voltage				Vcc[3]		V
Vss	Supply voltage				0	-----	V
AVss	Analog supply voltage				0		V
V_{IH}	"H" input voltage			0.8Vcc		Vcc	V
V_{IL}	"L" input voltage			0		0.2Vcc	V
$I_{OH\ (sum)}$	"H" peak all output currents	Sum of all pins' IOH (peak)				-60.0	mA
$I_{OH\ (peak)}$	"H" peak output current					-10.0	mA
$I_{OH\ (avg)}$	"H" average output current					-5.0	mA
$I_{OL\ (sum)}$	"L" peak all output currents	Sum of all pins' IOL (peak)				60	mA
$I_{OL\ (peak)}$	"L" peak output current	Except P1₀ to P1₇				10	mA
		P1₀ to P1₇	Drive ability HIGH		—	30	mA
			Drive ability LOW			10	mA
$I_{OL\ (avg)}$	"L" average output current	Except P1₀ to P1₇				5	mA
		P1₀ to P1₇	Drive ability HIGH			15	mA
			Drive ability LOW			5	mA
f(X_{IN})	Main clock input oscillation frequency		3.0V ≤ Vcc ≤ 5.5V	0		20	MHz
			2.7V ≤ Vcc < 3.0V	0		10	MHz

Note
1: Referenced to Vcc = AVcc = 2.7 to 5.5V at Topr = -20 to 85 °C / -40 to 85 °C unless otherwise specified.
2: The mean output current is the mean value within 100ms.
3: Set Vcc=AVcc

Table 5.3 A/D Conversion Characteristics

Symbol	Parameter		Measuring condition	Standard			Unit
				Min.	Typ.	Max.	
–	Resolution		Vref =Vcc		—	10	Bit
–	Absolute accuracy	10 bit mode	øAD=10 MHz, Vref=Vcc=5.0V			±3	LSB
		8 bit mode	øAD=10 MHz, Vref=Vcc=5.0V			±2	LSB
		10 bit mode	øAD=10 MHz, Vref=Vcc=3.3V[3]			±5	LSB
		8 bit mode	øAD=10 MHz, Vref=Vcc=3.3V[3]			±2	LSB
RLADDER	Ladder resistance		VREF=Vcc	10		40	kΩ
tCONV	Conversion time	10 bit mode	øAD=10 MHz, Vref=Vcc=5.0V	3.3	---		µs
		8 bit mode	øAD=10 MHz, Vref=Vcc=5.0V	2.8			µs
VREF	Reference voltage				Vcc[4]		V
VIA	Analog input voltage			0		Vref	V
–	A/D operation clock frequency[2]	Without sample & hold		0.25	—	10	MHz
		With sample & hold		1.0		10	MHz

Note
1: Referenced to Vcc=AVcc=2.7 to 5.5V at Topr = -20 to 85 °C / -40 to 85 °C unless otherwise specified.
2: When fAD is 10 MHz more, divide the fAD and make A/D operation clock frequency (ØAD) lower than 10 MHz.
3: When the AVcc is less than 4.2V, divide the fAD and make A/D operation clock frequency (ØAD) lower than fAD/2.
4: Set Vcc=Vref

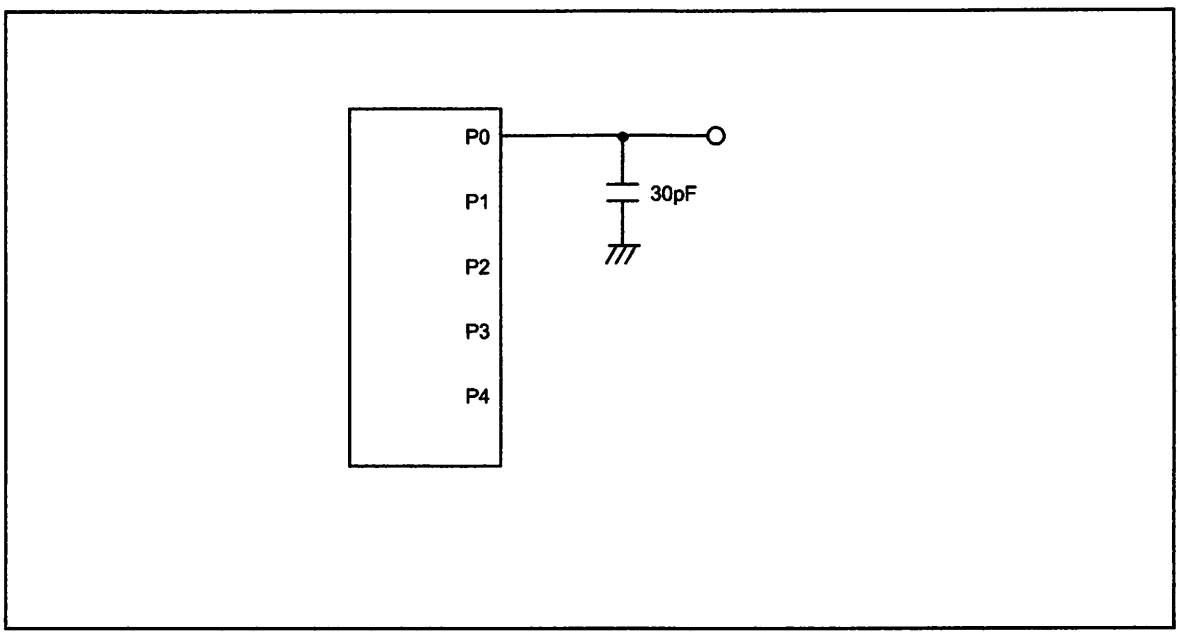


Figure 5.1 Port P0 to P4 measurement circuit

Table 5.4 Flash Memory (Program area) Electrical Characteristics

Symbol	Parameter	Measuring condition	Standard			Unit
			Min.	Typ.	Max	
–	Program/Erase cycle [2]		1000[3]	—	—	cycle
–	Byte program time	Vcc = 5.0 V at Topr = 25 °C	—	50	—	µs
–	Block erase time	Vcc = 5.0 V at Topr = 25 °C	—	0.4	—	s
td(SR-ES)	Time delay from Suspend Request until Erase Suspend		—	—	8	ms
–	Erase Suspend Request Interval		10	—	—	ms
–	Program, Erase Voltage		2.7	—	5.5	V
–	Read Voltage		2.7	—	5.5	V
–	Program, Erase Temperature		0	—	60	°C
–	Data-retention duration	Topr = 55 °C	20	—	—	year

Table 5.5 Flash Memory (Data area Block A, Block B) Electrical Characteristics [4]

Symbol	Parameter	Measuring condition	Standard			Unit
			Min.	Typ.	Max	
–	Program/Erase endurance[2]		10000 [3]	—	—	times
–	Byte program time(program/erase endurance ≤1000 times)	Vcc = 5.0 V at Topr = 25 °C	—	50	400	µs
–	Byte program time(program/erase endurance >1000 times)	Vcc = 5.0 V at Topr = 25 °C	—	65	—	µs
–	Block erase time(program/erase endurance ≤1000 times)	Vcc = 5.0 V at Topr = 25 °C	—	0.2	9	s
–	Block erase time(program/erase endurance >1000 times)	Vcc = 5.0 V at Topr = 25 °C	—	0.3	—	s
td(SR-ES)	Time delay from Suspend Request until Erase Suspend		—	—	8	ms
–	Erase Suspend Request Interval		10	—	—	ms
–	Program, Erase Voltage		2.7	—	5.5	V
–	Read Voltage		2.7	—	5.5	V
–	Program/Erase Temperature		-20(-40)[8]	—	85	°C
–	Data-retention duration	Topr = 55 °C	20	—	—	year

Note
1: Referenced to Vcc=AVcc=2.7 to 5.5V at Topr = 0°C to 60°C unless otherwise specified.
2: Definition of Program/Erase
The cycle of Program/Erase shows a cycle for each block.
If the program/erase number is "n" (n = 1000, 10000), "n" times erase can be performed for each block.
For example, if performing one-byte write to the distinct addresses on Block A of 2K-byte block 2048 times and then erasing that block, the number of Program/Erase cycles is one time.
However, performing multiple writes to the same address before an erase operation is prohibited (overwriting prohibited).
3: Maximum numbers of Program/Erase cycles for which all electrical characteristics is guaranteed.
4: Table 16.5 applies for Block A or B when the Program/Erase cycles are more than 1000. The byte program time up to 1000 cycles are the same as that of the program area (see Table 5.4).
5: To reduce the number of Program/Erase cycles, a block erase should ideally be performed after writing in series as many distinct addresses (only one time each) as possible. If programming a set of 16 bytes, write up to 128 sets and then erase them one time. This will result in ideally reducing the number of Program/Erase cycles. Additionally, averaging the number of Program/Erase cycles for Block A and B will be more effective. It is important to track the total number of block erases and restrict the number.
6: If error occurs during block erase, attempt to execute the clear status register command, then the block erase command at least three times until the erase error disappears.
7: Customers desiring Program/Erase failure rate information should contact their Renesas technical support representative.
8: -40 °C for D version.

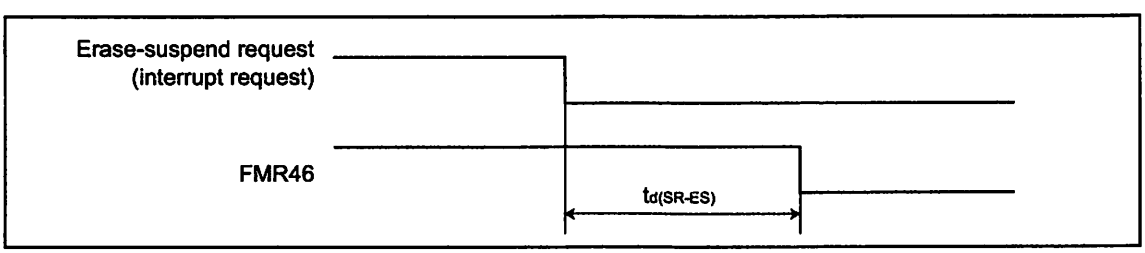


Figure 5.2 Time delay from Suspend Request until Erase Suspend

Table 5.6 Voltage Detection Circuit Electrical Characteristics

Symbol	Parameter	Measuring condition	Standard			Unit
			Min.	Typ.	Max.	
Vdet	Voltage detection level		3.3	3.8	4.3	V
	Voltage detection interrupt request generating time[2]			40		µs
	Voltage detection circuit self consumption current	VC27=1, VCC=5.0V		600		nA
td(E-A)	Waiting time until voltage detection circuit operation starts[3]				20	µs
Vccmin	Microcomputer operation voltage minimum value		2.7			V

NOTES:
1. The measuring condition is Vcc=AVcc=2.7V to 5.5V and Topr=-40°C to 85°C.
2. This shows the time until the voltage detection interrupt request is generated since the voltage passes Vdet.
3. This shows the required time until the voltage detection circuit operates when setting to "1" again after setting the VC27 bit in the VCR2 register to "0".

Table 5.7 Reset Circuit Electrical Characteristics (When Using Hardware Reset 2[1, 3])

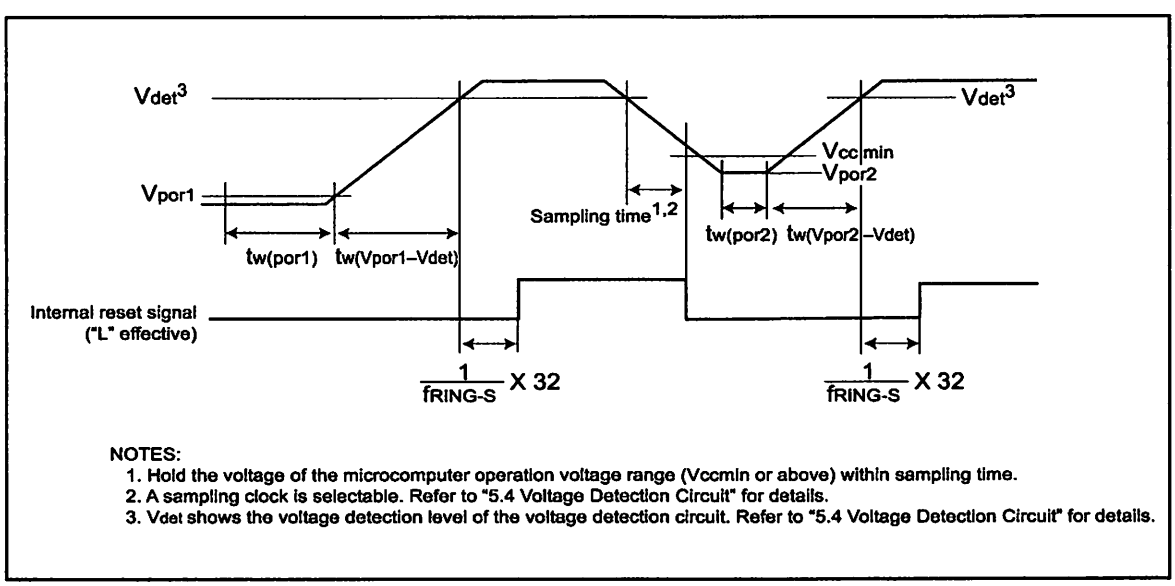
Symbol	Parameter	Measuring condition	Standard			Unit
			Min.	Typ.	Max.	
Vpor2	Power-on reset valid voltage	-20°C ≤ Topr < 85°C	—	—	Vdet	V
tw(Vpor2-Vdet)	Supply voltage rising time when power-on reset is canceled[2]	-20°C ≤ Topr < 85°C, tw(por2) ≥ 0s[4]	—	—	100	ms

NOTES:
1. The voltage detection circuit which is embedded in a microcomputer is a factor to generate the hardware reset 2. Refer to 5.1.2 Hardware Reset 2.
2. This condition is not applicable when using Vcc ≥ 1.0V.
3. When turning power on after the external power has been held below the valid voltage for greater than 10 seconds, refer to Table 16.8 Reset Circuit Electrical Characteristics (When Not Using Hardware Reset 2).
4. tw(por2) is time to hold the external power below effective voltage (Vpor2).

Table 5.8 Reset Circuit Electrical Characteristics (When Not Using Hardware Reset 2)

Symbol	Parameter	Measuring condition	Standard			Unit
			Min.	Typ.	Max.	
Vpor1	Power-on reset valid voltage	-20°C ≤ Topr < 85°C	—	—	0.1	V
tW(Vpor1-Vdet)	Supply voltage rising time when power-on reset is canceled	0°C ≤ Topr ≤ 85°C, tw(por1) ≥ 10s[2]	—	—	100	ms
tW(Vpor1-Vdet)	Supply voltage rising time when power-on reset is canceled	-20°C ≤ Topr < 0°C, tw(por1) ≥ 30s[2]	—	—	100	ms
tW(Vpor1-Vdet)	Supply voltage rising time when power-on reset is canceled	-20°C ≤ Topr < 0°C, tw(por1) ≥ 10s[2]	—	—	1	ms
tW(Vpor1-Vdet)	Supply voltage rising time when power-on reset is canceled	0°C ≤ Topr ≤ 85°C, tw(por1) ≥ 1s[2]	—	—	0.5	ms

NOTES:
1. When not using hardware reset 2, use with Vcc ≥ 2.7V.
2. tw(por1) is time to hold the external power below effective voltage (Vpor1).



NOTES:
1. Hold the voltage of the microcomputer operation voltage range (Vccmin or above) within sampling time.
2. A sampling clock is selectable. Refer to "5.4 Voltage Detection Circuit" for details.
3. Vdet shows the voltage detection level of the voltage detection circuit. Refer to "5.4 Voltage Detection Circuit" for details.

Figure 5.3 Reset Circuit Electrical Characteristics

Table 5.9 High-speed On-Chip Oscillator Circuit Electrical Characteristics

Symbol	Parameter	Measuring condition	Standard			Unit
			Min.	Typ.	Max.	
—	High-speed on-chip oscillator frequency 1 / {td(HRoffset)+td(HR)} when the reset is released	VCC=5.0V, Topr=25 °C Set "40$_{16}$" in the HR1 register	—	8	—	MHz
td(HRoffset)	Settable high-speed on-chip oscillator minimum period	VCC=5.0V, Topr=25 °C Set "00$_{16}$" in the HR1 register	—	61	—	ns
td(HR)	High-speed on-chip oscillator period adjusted unit	Differences when setting "01$_{16}$" and "00$_{16}$" in the HR register	—	1	—	ns
—	High-speed on-chip oscillator temperature dependence(1)	Frequency fluctuation in temperature range of -10 °C to 50 °C	—	±5	—	%
—	High-speed on-chip oscillator temperature dependence(2)	Frequency fluctuation in temperature range of -40 °C to 85 °C	—	±10	—	%

NOTES:
1. The measuring condition is Vcc=AVcc=5.0 V and Topr=25 °C.

Table 5.10 Power Circuit Timing Characteristics

Symbol	Parameter	Measuring condition	Standard			Unit
			Min.	Typ.	Max.	
td(P-R)	Time for internal power supply stabilization during powering-on[2]		1		2000	µs
td(R-S)	STOP release time[3]				150	µs

Note
1: The measuring condition is Vcc=AVcc=2.7 to 5.5 V and Topr=25 °C.
2: This shows the wait time until the internal power supply generating circuit is stabilized during power-on.
3: This shows the time until BCLK starts from the interrupt acknowledgement to cancel stop mode.

Table 5.11 Electrical Characteristics (1) [Vcc=5V]

Symbol	Parameter		Measuring condition		Standard			Unit
					Min.	Typ.	Max.	
V_{OH}	"H" output voltage	Except X_{OUT}	I_{OH}=-5mA		Vcc-2.0	—	Vcc	V
			I_{OH}=-200µA		Vcc-0.3	—	Vcc	V
		X_{OUT}	Drive capacity HIGH	I_{OH}=-1 mA	Vcc-2.0	—	Vcc	V
			Drive capacity LOW	I_{OH}=-500µA	Vcc-2.0	—	Vcc	V
V_{OL}	"L" output voltage	P10 to P17 Except X_{OUT}	I_{OL}= 5 mA		—	—	2.0	V
			I_{OL}= 200 µA		—	—	0.45	V
		P10 to P17	Drive capacity HIGH	I_{OL}= 15 mA	—	—	2.0	V
			Drive capacity LOW	I_{OL}= 5 mA	—	—	2.0	V
			Drive capacity LOW	I_{OL}= 200 µA	—	—	0.45	V
		X_{OUT}	Drive capacity HIGH	I_{OL}= 1 mA	—	—	2.0	V
			Drive capacity LOW	I_{OL}=500 µA	—	—	2.0	V
V_{T+}-V_{T-}	Hysteresis	INT0, INT1, INT2, INT3, KI0, KI1, KI2, KI3, CNTR0, CNTR1, TCIN, RxD0, RxD1, P45			0.2	—	1.0	V
		$\overline{RESET}$			0.2	—	2.2	V
I_{IH}	"H" input current		V_I=5V		—	—	5.0	µA
I_{IL}	"L" input current		V_I=0V		—	—	-5.0	µA
R_{PULLUP}	Pull-up resistance		V_I=0V		30	50	167	kΩ
R_{DIN}	Feedback resistance	X_{IN}			—	1.0	—	MΩ
f_{RING-S}	Low-speed on-chip oscillator frequency				40	125	250	kHz
V_{RAM}	RAM retention voltage		At stop mode		2.0	—	—	V

Note
1 : Referenced to Vcc=AVcc=4.2 to 5.5V at Topr = -20 to 85 °C / -40 to 85 °C, f(X_{IN})=20MHz unless otherwise specified.

Table 5.12 Electrical Characteristics (2) [Vcc=5V]

Symbol	Parameter	Measuring condition		Standard Min.	Standard Typ.	Standard Max.	Unit
Icc	Power supply current (Vcc=3.3 to 5.5V) In single-chip mode, the output pins are open and other pins are Vss	High-speed mode	XIN=20 MHz (square wave) High-speed on-chip oscillator off Low-speed on-chip oscillator on=125 kHz No division		9	15	mA
			XIN=16 MHz (square wave) High-speed on-chip oscillator off Low-speed on-chip oscillator on=125 kHz No division		8	14	mA
			XIN=10 MHz (square wave) High-speed on-chip oscillator off Low-speed on-chip oscillator on=125 kHz No division		5		mA
		Medium-speed mode	XIN=20 MHz (square wave) High-speed on-chip oscillator off Low-speed on-chip oscillator on=125 kHz Division by 8		4		mA
			XIN=16 MHz (square wave) High-speed on-chip oscillator off Low-speed on-chip oscillator on=125 kHz Division by 8		3		mA
			XIN=10 MHz (square wave) High-speed on-chip oscillator off Low-speed on-chip oscillator on=125 kHz Division by 8		2		mA
		High-speed on-chip oscillator mode	Main clock off High-speed on-chip oscillator on=8 MHz Low-speed on-chip oscillator on=125 kHz No division		4	8	mA
			Main clock off High-speed on-chip oscillator on=8 MHz Low-speed on-chip oscillator on=125 kHz Division by 8		1.5		mA
		Low-speed on-chip oscillator mode	Main clock off High-speed on-chip oscillator off Low-speed on-chip oscillator on=125 kHz Division by 8		470	900	µA
		Wait mode	Main clock off High-speed on-chip oscillator off Low-speed on-chip oscillator on=125 kHz When a WAIT instruction is executed[2] Peripheral clock operation VC27="0"		40	80	µA
		Wait mode	Main clock off High-speed on-chip oscillator off Low-speed on-chip oscillator on=125 kHz When a WAIT instruction is executed[2] Peripheral clock off VC27="0"		38	76	µA
		Stop mode	Main clock off High-speed on-chip oscillator off Low-speed on-chip oscillator off CM10="1" Peripheral clock off VC27="0"		0.8	3.0	µA

NOTES
1: The power supply current measuring is executed using the measuring program on frash memory.
2: Timer Y is operated with timer mode.

Timing requirements (Unless otherwise noted: Vcc = 5V, Vss = 0V at Ta = 25 °C) [Vcc=5V]

Table 5.13 XIN input

Symbol	Parameter	Standard		Unit
		Min.	Max.	
tC(XIN)	XIN input cycle time	50		ns
tWH(XIN)	XIN input HIGH pulse width	25		ns
tWL(XIN)	XIN input LOW pulse width	25		ns

Table 5.14 CNTR0 input, CNTR1 input, $\overline{\text{INT2}}$ input

Symbol	Parameter	Standard		Unit
		Min.	Max.	
tC(CNTR0)	CNTR0 input cycle time	100		ns
tWH(CNTR0)	CNTR0 input HIGH pulse width	40		ns
tWL(CNTR0)	CNTR0 input LOW pulse width	40		ns

Table 5.15 TCIN input, $\overline{\text{INT3}}$ input

Symbol	Parameter	Standard		Unit
		Min.	Max.	
tC(TCIN)	TCIN input cycle time	400 [1]		ns
tWH(TCIN)	TCIN input HIGH pulse width	200 [2]		ns
tWL(TCIN)	TCIN input LOW pulse width	200 [2]		ns

NOTES

1 :When using the Timer C input capture mode, adjust the cycle time above (1/ Timer C count source frequency x 3).

2 : When using the Timer C input capture mode, adjust the pulse width above (1/ Timer C count source frequency x 1.5).

Table 5.16 Serial Interface

Symbol	Parameter	Standard		Unit
		Min.	Max.	
tC(CK)	CLKi input cycle time	200		ns
tW(CKH)	CLKi input HIGH pulse width	100		ns
tW(CKL)	CLKi input LOW pulse width	100		ns
td(C-Q)	TxDi output delay time		80	ns
th(C-Q)	TxDi hold time	0		ns
tsu(D-C)	RxDi input setup time	35		ns
th(C-D)	RxDi input hold time	90		ns

Table 5.17 External interrupt $\overline{\text{INT0}}$ input

Symbol	Parameter	Standard		Unit
		Min.	Max.	
tW(INH)	$\overline{\text{INT0}}$ input HIGH pulse width	250 [1]		ns
tW(INL)	$\overline{\text{INT0}}$ input LOW pulse width	250 [2]		ns

NOTES

1 : When selecting the digital filter by the $\overline{\text{INT0}}$ input filter select bit, use the $\overline{\text{INT0}}$ input HIGH pulse width to the greater value,either (1/ digital filter clock frequency x 3) or the minimum value of standard.

2 : When selecting the digital filter by the $\overline{\text{INT0}}$ input filter select bit, use the $\overline{\text{INT0}}$ input LOW pusle width to the greater value,either (1/ digital filter clock frequency x 3) or the minimum value of standard.

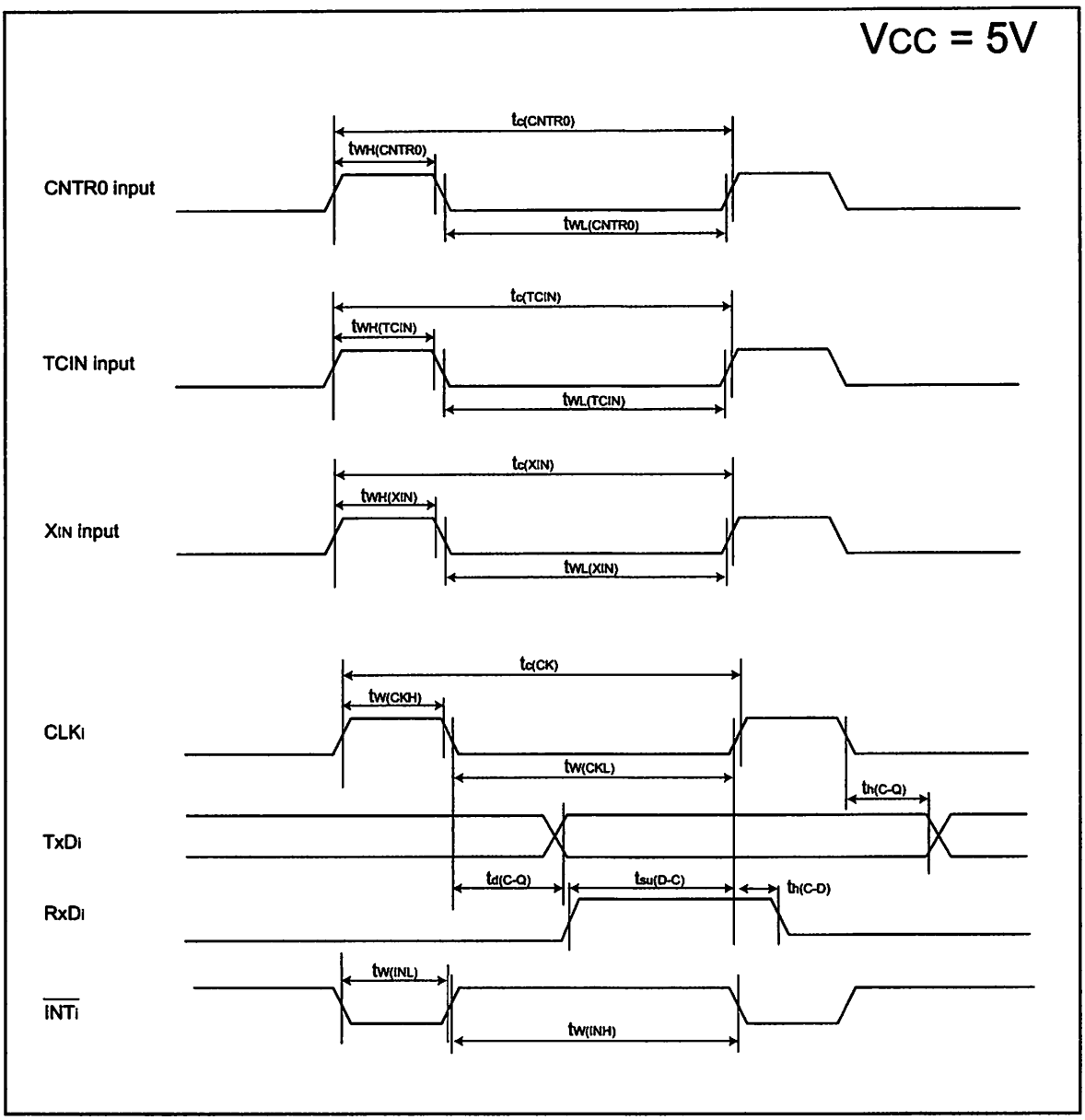


Figure 5.4 Vcc=5V timing diagram

Table 5.18 Electrical Characteristics (3) [Vcc=3V]

Symbol	Parameter		Measuring condition		Standard			Unit
					Min.	Typ.	Max.	
V_{OH}	"H" output voltage	Except X_{OUT}	I_{OH}=-1mA		Vcc-0.5	—	Vcc	V
		X_{OUT}	Drive capacity HIGH	I_{OH}=-0.1 mA	Vcc-0.5	—	Vcc	V
			Drive capacity LOW	I_{OH}=-50 µA	Vcc-0.5	—	Vcc	V
V_{OL}	"L" output voltage	P10 to P17 Except X_{OUT}	I_{OL}= 1 mA		—	—	0.5	V
		P10 to P17	Drive capacity HIGH	I_{OL}= 2 mA	—	—	0.5	V
			Drive capacity LOW	I_{OL}= 1 mA	—	—	0.5	V
		X_{OUT}	Drive capacity HIGH	I_{OL}= 0.1 mA	—	—	0.5	V
			Drive capacity LOW	I_{OL}=50 µA	—	—	0.5	V
V_{T+}-V_{T-}	Hysteresis	$\overline{INT0}$, $\overline{INT1}$, $\overline{INT2}$, $\overline{INT3}$, $\overline{KI0}$, $\overline{KI1}$, $\overline{KI2}$, $\overline{KI3}$, CNTR0, CNTR1, T_{CIN}, RxD0, RxD1, P45			0.2	—	0.8	V
		$\overline{RESET}$			0.2	—	1.8	V
I_{IH}	"H" input current		V_I=3V		—	—	4.0	µA
I_{IL}	"L" input current		V_I=0V		—	—	-4.0	µA
R_{PULLUP}	Pull-up resistance		V_I=0V		66	160	500	kΩ
R_{fXIN}	Feedback resistance	X_{IN}			—	3.0	—	MΩ
f_{RING-S}	Low-speed on-chip oscillator frequency				40	125	250	kHz
V_{RAM}	RAM retention voltage		At stop mode		2.0	—	—	V

Note
1 : Referenced to Vcc=AVcc=2.7 to 3.3V at Topr = -20 to 85 °C / -40 to 85 °C, f(X_{IN})=10MHz unless otherwise specified.

Table 5.19 Electrical Characteristics (4) [Vcc=3V]

Symbol	Parameter	Measuring condition		Standard Min.	Standard Typ.	Standard Max.	Unit
Icc	Power supply current (Vcc=2.7 to 3.3V) In single-chip mode, the output pins are open and other pins are Vss	High-speed mode	XIN=20 MHz (square wave) High-speed on-chip oscillator off Low-speed on-chip oscillator on=125 kHz No division		8	13	mA
			XIN=16 MHz (square wave) High-speed on-chip oscillator off Low-speed on-chip oscillator on=125 kHz No division		7	12	mA
			XIN=10 MHz (square wave) High-speed on-chip oscillator off Low-speed on-chip oscillator on=125 kHz No division		5		mA
		Medium-speed mode	XIN=20 MHz (square wave) High-speed on-chip oscillator off Low-speed on-chip oscillator on=125 kHz Division by 8		3		mA
			XIN=16 MHz (square wave) High-speed on-chip oscillator off Low-speed on-chip oscillator on=125 kHz Division by 8		2.5		mA
			XIN=10 MHz (square wave) High-speed on-chip oscillator off Low-speed on-chip oscillator on=125 kHz Division by 8		1.6		mA
		High-speed on-chip oscillator mode	Main clock off High-speed on-chip oscillator on=8 MHz Low-speed on-chip oscillator on=125 kHz No division		3.5	7.5	mA
			Main clock off High-speed on-chip oscillator on=8 MHz Low-speed on-chip oscillator on=125 kHz Division by 8		1.5	—	mA
		Low-speed on-chip oscillator mode	Main clock off High-speed on-chip oscillator off Low-speed on-chip oscillator on=125 kHz Division by 8		420	800	µA
		Wait mode	Main clock off High-speed on-chip oscillator off Low-speed on-chip oscillator on=125 kHz When a WAIT instruction is executed[2] Peripheral clock operation VC27="0"		37	74	µA
		Wait mode	Main clock off High-speed on-chip oscillator off Low-speed on-chip oscillator on=125 kHz When a WAIT instruction is executed[2] Peripheral clock off VC27="0"		35	70	µA
		Stop mode	Main clock off High-speed on-chip oscillator off Low-speed on-chip oscillator off CM10="1" Peripheral clock off VC27="0"		0.7	3.0	µA

NOTES
1: The power supply current measuring is executed using the measuring program on frash memory.
2: Timer Y is operated with timer mode.

Timing requirements (Unless otherwise noted: Vcc = 3V, Vss = 0V at Ta = 25 °C) [Vcc=3V]

Table 5.20 XIN input

Symbol	Parameter	Standard		Unit
		Min.	Max.	
tc(XIN)	XIN input cycle time	100		ns
twH(XIN)	XIN input HIGH pulse width	40		ns
twL(XIN)	XIN input LOW pulse width	40		ns

Table 5.21 CNTR0 input, CNTR1 input, $\overline{INT2}$ input

Symbol	Parameter	Standard		Unit
		Min.	Max.	
tc(CNTR0)	CNTR0 input cycle time	300		ns
twH(CNTR0)	CNTR0 input HIGH pulse width	120		ns
twL(CNTR0)	CNTR0 input LOW pulse width	120		ns

Table 5.22 TCIN input, $\overline{INT3}$ input

Symbol	Parameter	Standard		Unit
		Min.	Max.	
tc(TCIN)	TCIN input cycle time	1200 [1]		ns
twH(TCIN)	TCIN input HIGH pulse width	600 [2]		ns
twL(TCIN)	TCIN input LOW pulse width	600 [2]		ns

NOTES
1 :When using the Timer C input capture mode, adjust the cycle time above (1/ Timer C count source frequency x 3).
2 : When using the Timer C input capture mode, adjust the pulse width above (1/ Timer C count source frequency x 1.5).

Table 5.23 Serial Interface

Symbol	Parameter	Standard		Unit
		Min.	Max.	
tc(CK)	CLKi input cycle time	300		ns
tw(CKH)	CLKi input HIGH pulse width	150		ns
tw(CKL)	CLKi input LOW pulse width	150		ns
td(C-Q)	TxDi output delay time		160	ns
th(C-Q)	TxDi hold time	0		ns
tsu(D-C)	RxDi input setup time	55		ns
th(C-D)	RxDi input hold time	90		ns

Table 5.24 External interrupt $\overline{INT0}$ input

Symbol	Parameter	Standard		Unit
		Min.	Max.	
tw(INH)	$\overline{INT0}$ input HIGH pulse width	380 [1]		ns
tw(INL)	$\overline{INT0}$ input LOW pulse width	380 [2]		ns

NOTES
1 : When selecting the digital filter by the $\overline{INT0}$ input filter select bit, use the $\overline{INT0}$ input HIGH pulse width to the greater value,either (1/ digital filter clock frequency x 3) or the minimum value of standard.
2 : When selecting the digital filter by the $\overline{INT0}$ input filter select bit, use the $\overline{INT0}$ input LOW pusle width to the greater value,either (1/ digital filter clock frequency x 3) or the minimum value of standard.

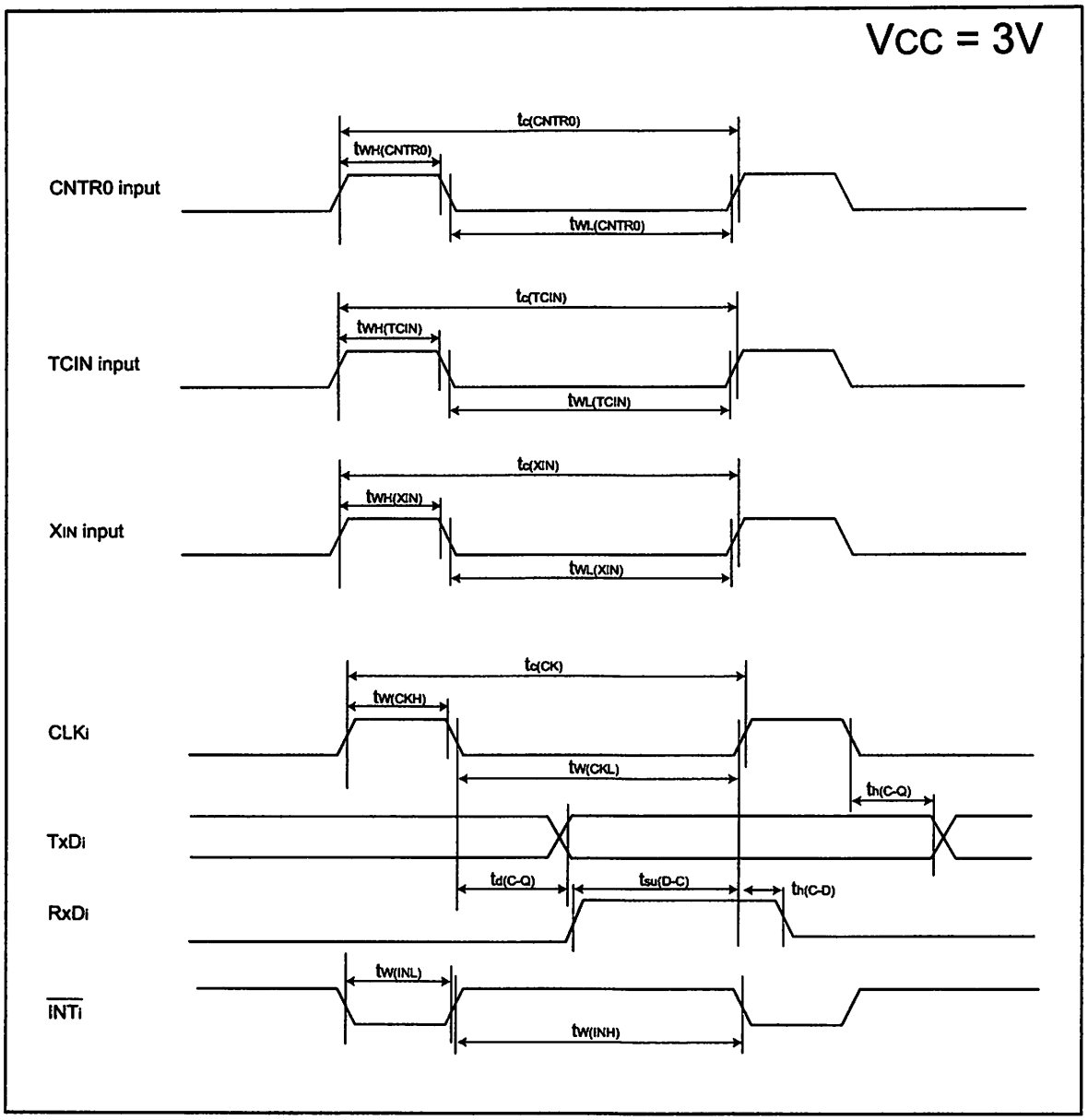
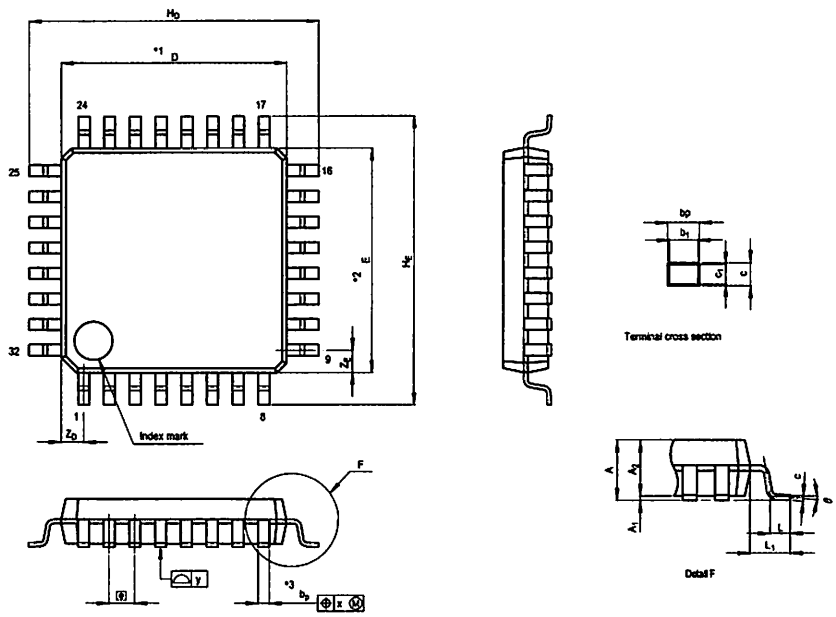


Figure 5.5 Vcc=3V timing diagram

Package Dimensions

JEITA Package Code	RENESAS Code	Previous Code	MASS[Typ.]
P-LQFP32-7x7-0.80	PLQP0032GB-A	32P6U-A	0.2g



NOTE)
1. DIMENSIONS "*1" AND "*2" DO NOT INCLUDE MOLD FLASH.
2. DIMENSION "*3" DOES NOT INCLUDE TRIM OFFSET.

Reference Symbol	Dimension in Millimeters		
	Min	Nom	Max
D	6.9	7.0	7.1
E	6.9	7.0	7.1
A_2	—	1.4	—
H_D	8.8	9.0	9.2
H_E	8.8	9.0	9.2
A	—	—	1.7
A_1	0	0.1	0.2
b_p	0.32	0.37	0.42
b_1	—	0.35	—
c	0.09	0.145	0.20
c_1	—	0.125	—
θ	0°	—	8°
ⓑ	—	0.8	—
x	—	—	0.20
y	—	—	0.10
Z_D	—	0.7	—
Z_E	—	0.7	—
L	0.3	0.5	0.7
L_1	—	1.0	—

Rev.	Date	Description	
		Page	Summary
0.10	Oct 28, 2003		First edition issued
0.20	Dec05, 2003	5	Figure 1.3 revised
		10	Chapter 4, NOTES revised
		16	Table 5.4 revised Table 5.5 revised
		17	Table 5.6 revised Figure 5.3 added
		18	Table 5.8 revised Table 5.10 revised
		21	Figure 5.3 revised to Figure 5.4
		22	Table 5.17 revised
		25	Figure 5.4 revised to Figure 5.5
1.00	Sep 30, 2004	All pages	Words standardized (on-chip oscillator, serial interface, A/D)
		2	Table 1.1 revised
		5	Figure 1.3, NOTES 3 added
		6	Table 1.3 revised
		9	Figure 3.1, NOTES added
		10-13	One body sentence in chapter 4 added ; Titles of Table 4.1 to 4.4 added
		12	Table 4.3 revised ; Table 4.4 revised
		14	Table 5.2 revised
		15	Table 5.3 revised
		16	Table 5.4 and Table 5.5 revised
		17	Table 5.6, 5.7 and 5.8 revised ; Figure 5.3 revised
		18	Table 5.9 and 5.11 revised
		19	Table 5.12 revised
		20	Table 5.13 revised
		22	Table 5.18 revised
		23	Table 5.19 revised
		24	Table 5.20 and Table 5.24 revised
1.10	Apr.27.2005	4	Table 1.2, Figure 1.2 package name revised
		5	Figure 1.3 package name revised
		10	Table 4.1 revised
		12	Table 4.3 revised
		15	Table 5.3 partly revised
		16	Table 5.4, Table 5.5 partly added

Rev.	Date	Description	
		Page	Summary
1.10	Apr.27.2005	17	Table 5.7, 5.8 revised
		18	Table 5.10, Table 5.11 partly revised
		22	Table 5.18 partly revised
		26	Package Dimensions revised

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Colophon 2.0

```
DOS 7.0 (038-N) MCS-51 MACRO ASSEMBLER, V2.2
OBJECT MODULE PLACED IN RENESAS.OBJ
ASSEMBLER INVOKED BY:  C:\HB2000\ASM51.EXE RENESAS.H51


LOC  OBJ             LINE     SOURCE

                        1     ;================================================
                        2     ; LISTING PROGRAM
                        3     ; JUDUL : PERANCANGAN DAN PEMBUATAN ALAT PENERIMA
                        4     ;         TELEPHON OTOMATIS DENGAN RENESAS R8C/13
                        5     ;         DAN AT 89S51
                        6     ; OLEH      : HADI CAHYADI
                        7     ; NIM       : 01.17.112
                        8     ; JURUSAN   : TEKNIK ELEKTRO /ELKA
                        9     ; FAKULTAS  : TEKNOLOGI INDUSTRI
                       10     ; INSTITUT TEKNOLOGI NASIONAL MALANG
                       11     ; TAHUN 2006/2007
                       12     ;================================================
                       13     ;
0000                   14             org     00h
0000 02028B            15             ljmp    MULAI
                       16     ;
                       17     ;----------------------------
                       18     ; baca vektor interupt serial
                       19     ;----------------------------
0075                   20             org     75h
0075 C2AF              21             clr     EA
0077 C2AC              22             clr     ES
0079 30980A            23             jnb     RI,E_S
007C E599              24             mov     A,sbuf
007E C298              25             clr     RI
0080 F8                26             mov     R0,A
0081 D2AF              27             setb    EA
0083 D2AC              28             setb    ES
0085 32                29             reti
                       30     ;
0086 7800              31     E_S:    mov     R0,#0
0088 D2AF              32             setb    EA
008A D2AC              33             setb    ES
008C 32                34             reti
                       35     ;
                       36
                       37     ;----------------------------
                       38     ; Inisialisasi port-port MCU
                       39     ;----------------------------
  0080                 40     LCD     EQU     P0
  0090                 41     ENABLE  BIT     P1.0
  0091                 42     RS      BIT     P1.1
  00A0                 43     ISD     EQU     P2
  00A6                 44     P_R     BIT     P2.6
  00A5                 45     EOM     BIT     P2.5
  00A7                 46     PD_CE   BIT     P2.7
  0092                 47     SOUND   BIT     P1.2
  0093                 48     LOAD    bit     P1.3
  0030                 49     BUFER   EQU     30h
  00B2                 50     X1      bit     P3.2
```

```
LOC  OBJ             LINE     SOURCE

  00B3                 51     X2      bit     P3.3
  00B4                 52     X3      bit     P3.4
  00B5                 53     X4      bit     P3.5
  00B6                 54     Y1      bit     P3.6
  00B7                 55     Y2      bit     P3.7
  0097                 56     Y3      bit     P1.7
                       57     ;
                       58     ;---------------------------
                       59     ; Prosedur delay u/ tampilan
                       60     ;---------------------------
008D 7E0A              61     DELAY:  mov     R6,#0Ah
008F 7FAF              62     DEL1:   mov     R7,#0AFh
0091 DFFE              63     DEL2:   djnz    R7,DEL2
0093 DEFA              64             djnz    R6,DEL1
0095 22                65             ret
                       66     ;
                       67     ;---------------------------
                       68     ; Prosedur delay panjang
                       69     ;---------------------------
0096 7E00              70     LDELAY: mov     R6,#0
0098 7F00              71     LDEL1:  mov     R7,#0
009A DFFE              72     LDEL2:  djnz    R7,LDEL2
009C DEFA              73             djnz    R6,LDEL1
009E 22                74             ret
                       75     ;
                       76     ;---------------------------
                       77     ; Prosedur inisialisasi LCD
                       78     ;---------------------------
                       79     INIT_LCD:
009F C0E0              80             push    ACC
00A1 C0D0              81             push    PSW
00A3 C083              82             push    DPH
00A5 C082              83             push    DPL
00A7 C291              84             clr     RS
00A9 75803F            85             mov     LCD,#3Fh
00AC 11C9              86             acall   SEND
00AE 75800D            87             mov     LCD,#0Dh
00B1 11C9              88             acall   SEND
00B3 758006            89             mov     LCD,#06h
00B6 1200C9            90             call    SEND
00B9 758001            91             mov     LCD,#01h
00BC 11C9              92             acall   SEND
00BE D291              93             setb    RS
00C0 D082              94             pop     DPL
00C2 D083              95             pop     DPH
00C4 D0D0              96             pop     PSW
00C6 D0E0              97             pop     ACC
00C8 22                98             ret
                       99     ;
                      100     ;---------------------------
                      101     ; Prosedur sinyal enable LCD
                      102     ;---------------------------
00C9 C290             103     SEND:   clr     ENABLE
00CB 118D             104             acall   DELAY
00CD D290             105             setb    ENABLE
```

```
LOC  OBJ             LINE     SOURCE

00CF 118D             106             acall   DELAY
00D1 22               107             ret
                      108     ;
                      109     ;----------------------------
                      110     ; Prosedur membersihkan tampilan
                      111     ;----------------------------
00D2 C0E0             112     CLEAR:  push    ACC
00D4 C291             113             clr     RS
00D6 758001           114             mov     LCD,#01h
00D9 11C9             115             acall   SEND
00DB D0E0             116             pop     ACC
00DD 22               117             ret
                      118     ;
                      119     ;----------------------------
                      120     ; Prosedur ke awal baris
                      121     ;----------------------------
00DE C0E0             122     HOME:   push    ACC
00E0 C291             123             clr     RS
00E2 758080           124             mov     LCD,#80h
00E5 11C9             125             acall   SEND
00E7 D0E0             126             pop     ACC
00E9 22               127             ret
                      128     ;
                      129     ;----------------------------
                      130     ; Prosedur ganti baris LCD
                      131     ;----------------------------
00EA C0E0             132     GANTI:  push    ACC
00EC C291             133             clr     RS
00EE 7580C0           134             mov     LCD,#0C0h
00F1 11C9             135             acall   SEND
00F3 D0E0             136             pop     ACC
00F5 22               137             ret
                      138     ;
                      139     ;----------------------------
                      140     ; Prosedur penulisan string
                      141     ;----------------------------
00F6 C0E0             142     STRING: push    ACC
00F8 C0D0             143             push    PSW
00FA 7A10             144             mov     R2,#16
00FC D291             145             setb    RS
00FE E4               146     AWAL:   clr     A
00FF 93               147             movc    A,@A+dptr
0100 A3               148             inc     dptr
0101 F580             149             mov     LCD,A
0103 11C9             150             acall   SEND
0105 DAF7             151             djnz    R2,AWAL
0107 1196             152             acall   LDELAY
0109 1196             153             acall   LDELAY
010B 1196             154             acall   LDELAY
010D D0D0             155             pop     PSW
010F D0E0             156             pop     ACC
0111 22               157             ret
                      158     ;
                      159     ;----------------------------
                      160     ; Set port serial & baut rate
```

```
LOC  OBJ            LINE     SOURCE

                     161     ;-----------------------------
0112 C0E0            162     S_SERI: push    ACC
0114 858130          163             mov     BUFER,SP
0117 758DFD          164             mov     TH1,#0FDh ; 9600bps
011A 758920          165             mov     TMOD,#20h
011D D28E            166             setb    TR1
011F 759850          167             mov     SCON,#50h
0122 C2AC            168             clr     ES
0124 C2AF            169             clr     EA
0126 D0E0            170             pop     ACC
0128 22              171             ret
                     172     ;
                     173     ;-----------------------------
                     174     ; Looping Data Masukan
                     175     ;-----------------------------
0129 75B0FB          176     TOMBOL: mov     P3,#11111011b
012C 20B603          177             jb      Y1,ANGKA2
012F 7B31            178             mov     R3,#31h
0131 22              179             ret
0132 20B703          180     ANGKA2: jb      Y2,ANGKA3
0135 7B32            181             mov     R3,#32h
0137 22              182             ret
0138 209703          183     ANGKA3: jb      Y3,ANGKA4
013B 7B33            184             mov     R3,#33h
013D 22              185             ret
013E 75B0F7          186     ANGKA4: mov     P3,#11110111b
0141 20B603          187             jb      Y1,ANGKA5
0144 7B34            188             mov     R3,#34h
0146 22              189             ret
0147 20B703          190     ANGKA5: jb      Y2,ANGKA6
014A 7B35            191             mov     R3,#35h
014C 22              192             ret
014D 209703          193     ANGKA6: jb      Y3,ANGKA7
0150 7B36            194             mov     R3,#36h
0152 22              195             ret
0153 75B0EF          196     ANGKA7: mov     P3,#11101111b
0156 20B603          197             jb      Y1,ANGKA8
0159 7B37            198             mov     R3,#37h
015B 22              199             ret
015C 20B703          200     ANGKA8: jb      Y2,ANGKA9
015F 7B38            201             mov     R3,#38h
0161 22              202             ret
0162 209703          203     ANGKA9: jb      Y3,ANGKA_A
0165 7B39            204             mov     R3,#39h
0167 22              205             ret
                     206     ANGKA_A:
0168 75B0DF          207             mov     P3,#11011111b
016B 20B603          208             jb      Y1,ANGKA0
016E 7B3A            209             mov     R3,#3Ah
0170 22              210             ret
0171 20B703          211     ANGKA0: jb      Y2,ANGKA_B
0174 7B30            212             mov     R3,#30h
0176 22              213             ret
                     214     ANGKA_B:
0177 2097AF          215             jb      Y3,TOMBOL
```

```
LOC  OBJ            LINE     SOURCE

017A 7B3B            216             mov     R3,#3Bh
017C 22              217             ret
                     218     ;
                     219     ;----------------------------
                     220     ; membaca kode dtmf
                     221     ;----------------------------
017D B83E02          222     CODES:  cjne    R0,#3Eh,CODEK
0180 6108            223             ajmp    ON_HOOK
                     224     ;
0182 B83C02          225     CODEK:  cjne    R0,#3Ch,CODE0
0185 41D9            226             ajmp    BEBAS
                     227     ;
0187 B8300B          228     CODE0:  cjne    R0,#30h,CODE1
018A C292            229             clr     SOUND
018C 75A0EE          230             mov     ISD,#0EEh
018F 5122            231             acall   PUTAR
0191 5118            232             acall   PUTAR2
0193 217D            233             ajmp    CODES
0195 B8310B          234     CODE1:  cjne    R0,#31h,CODE2
0198 C292            235             clr     SOUND
019A 75A0EF          236             mov     ISD,#0EFh
019D 5122            237             acall   PUTAR
019F 5118            238             acall   PUTAR2
01A1 217D            239             ajmp    CODES
01A3 B8320B          240     CODE2:  cjne    R0,#32h,CODE3
01A6 C292            241             clr     SOUND
01A8 75A0F0          242             mov     ISD,#0F0h
01AB 5122            243             acall   PUTAR
01AD 5118            244             acall   PUTAR2
01AF 217D            245             ajmp    CODES
01B1 B8330B          246     CODE3:  cjne    R0,#33h,CODE4
01B4 C292            247             clr     SOUND
01B6 75A0F1          248             mov     ISD,#0F1h
01B9 5122            249             acall   PUTAR
01BB 5118            250             acall   PUTAR2
01BD 217D            251             ajmp    CODES
01BF B8340B          252     CODE4:  cjne    R0,#34h,CODE5
01C2 C292            253             clr     SOUND
01C4 75A0F2          254             mov     ISD,#0F2h
01C7 5122            255             acall   PUTAR
01C9 5118            256             acall   PUTAR2
01CB 217D            257             ajmp    CODES
01CD B8350B          258     CODE5:  cjne    R0,#35h,CODE6
01D0 C292            259             clr     SOUND
01D2 75A0F3          260             mov     ISD,#0F3h
01D5 5122            261             acall   PUTAR
01D7 5118            262             acall   PUTAR2
01D9 217D            263             ajmp    CODES
01DB B8360B          264     CODE6:  cjne    R0,#36h,CODE7
01DE C292            265             clr     SOUND
01E0 75A0F4          266             mov     ISD,#0F4h
01E3 5122            267             acall   PUTAR
01E5 5118            268             acall   PUTAR2
01E7 217D            269             ajmp    CODES
01E9 B8370B          270     CODE7:  cjne    R0,#37h,CODE8
```

```
LOC  OBJ             LINE     SOURCE

01EC C292             271             clr     SOUND
01EE 75A0F5           272             mov     ISD,#0F5h
01F1 5122             273             acall   PUTAR
01F3 5118             274             acall   PUTAR2
01F5 217D             275             ajmp    CODES
01F7 B8380B           276     CODE8:  cjne    R0,#38h,CODE9
01FA C292             277             clr     SOUND
01FC 75A0F6           278             mov     ISD,#0F6h
01FF 5122             279             acall   PUTAR
0201 5118             280             acall   PUTAR2
0203 217D             281             ajmp    CODES
0205 B8390B           282     CODE9:  cjne    R0,#39h,E_CODE
0208 C292             283             clr     SOUND
020A 75A0F7           284             mov     ISD,#0F7h
020D 5122             285             acall   PUTAR
020F 5118             286             acall   PUTAR2
0211 217D             287     S_CODE: ajmp    CODES
                      288     ;
                      289     E_CODE:
0213 B83AFB           290             cjne    R0,#3Ah,S_CODE
0216 413C             291             ajmp    AREK
                      292     ;
                      293     ;----------------------------
                      294     ; panggilan bersama
                      295     ;----------------------------
0218 C0E0             296     PUTAR2: push    ACC
021A C0D0             297             push    PSW
021C 75A0F9           298             mov     ISD,#0F9h
021F 020226           299             jmp     PUTARAN
0222 C0E0             300     PUTAR:  push    ACC
0224 C0D0             301             push    PSW
                      302     PUTARAN:
0226 D2A6             303             setb    P_R
0228 D2A7             304             setb    PD_CE
022A 1196             305             acall   LDELAY
022C C2A7             306             clr     PD_CE
022E 20A5FD           307             jb      EOM,$
0231 D2A7             308             setb    PD_CE
0233 1196             309             acall   LDELAY
0235 1196             310             acall   LDELAY
0237 D0D0             311             pop     PSW
0239 D0E0             312             pop     ACC
023B 22               313             ret
                      314     ;
                      315     ;
                      316     ;----------------------------
                      317     ; dering panggilan
                      318     ;----------------------------
023C 7800             319     AREK:   mov     R0,#0
023E 9004FE           320             mov     dptr,#MENU2
0241 11DE             321             acall   HOME
0243 11F6             322             acall   STRING
0245 11EA             323             acall   GANTI
0247 11F6             324             acall   STRING
0249 D292             325             setb    SOUND
```

```
LOC  OBJ             LINE     SOURCE

024B D293             326             setb    LOAD
024D 75A0E0           327             mov     ISD,#0E0h
0250 5122             328             acall   PUTAR
0252 75A0EE           329             mov     ISD,#0EEh
0255 5122             330             acall   PUTAR
0257 75A0EF           331             mov     ISD,#0EFh
025A 5122             332             acall   PUTAR
025C 75A0F0           333             mov     ISD,#0F0h
025F 5122             334             acall   PUTAR
0261 75A0F1           335             mov     ISD,#0F1h
0264 5122             336             acall   PUTAR
0266 75A0F2           337             mov     ISD,#0F2h
0269 5122             338             acall   PUTAR
026B 75A0F3           339             mov     ISD,#0F3h
026E 5122             340             acall   PUTAR
0270 75A0F4           341             mov     ISD,#0F4h
0273 5122             342             acall   PUTAR
0275 75A0F5           343             mov     ISD,#0F5h
0278 5122             344             acall   PUTAR
027A 75A0F6           345             mov     ISD,#0F6h
027D 5122             346             acall   PUTAR
027F 75A0F7           347             mov     ISD,#0F7h
0282 5122             348             acall   PUTAR
0284 75A0FB           349             mov     ISD,#0FBh
0287 5122             350             acall   PUTAR
0289 217D             351             ajmp    CODES
                      352     ;
                      353     ;
                      354     ;----------------------------
                      355     ; Program Utama
                      356     ;----------------------------
028B C291             357     MULAI:  clr     RS
028D D290             358             setb    ENABLE
028F 75A0FF           359             mov     ISD,#0FFh
0292 D2A6             360             setb    P_R
0294 D2A7             361             setb    PD_CE
0296 C293             362             clr     LOAD
0298 C292             363             clr     SOUND
029A D2B2             364             setb    X1
029C D2B3             365             setb    X2
029E D2B4             366             setb    X3
02A0 D2B5             367             setb    X4
02A2 D2B6             368             setb    Y1
02A4 D2B7             369             setb    Y2
02A6 D297             370             setb    Y3
02A8 1196             371             acall   LDELAY
02AA 1196             372             acall   LDELAY
                      373     ;
                      374     ;----------------------------
                      375     ; Proses menampilkan judul
                      376     ;----------------------------
02AC 119F             377             acall   INIT_LCD
02AE 1196             378             acall   LDELAY
02B0 C2AF             379             clr     EA
02B2 C2AC             380             clr     ES
```

```
LOC  OBJ            LINE     SOURCE

02B4 C298            381             clr     RI
02B6 C299            382             clr     TI
02B8 7D05            383     PROSES: mov     R5,#5
02BA 90041E          384             mov     dptr,#JUDUL
02BD 11DE            385     NEXT1:  acall   HOME
02BF 11F6            386             acall   STRING
02C1 118D            387             acall   DELAY
02C3 11EA            388             acall   GANTI
02C5 11F6            389             acall   STRING
02C7 1196            390             acall   LDELAY
02C9 1196            391             acall   LDELAY
02CB DDF0            392             djnz    R5,NEXT1
02CD 1196            393             acall   LDELAY
02CF 1196            394             acall   LDELAY
02D1 3112            395             acall   S_SERI
02D3 D2AF            396             setb    EA
02D5 D2AC            397             setb    ES
02D7 7800            398             mov     R0,#0
                     399     ;
                     400     ;----------------------------
                     401     ; posisi menunggu panggilan
                     402     ;----------------------------
02D9 9004BE          403     BEBAS:  mov     dptr,#MENU
02DC 11D2            404             acall   CLEAR
02DE 11F6            405             acall   STRING
02E0 11EA            406             acall   GANTI
02E2 11F6            407             acall   STRING
02E4 D2A7            408             setb    PD_CE
02E6 D2AF            409             setb    EA
02E8 D2AC            410             setb    ES
02EA D2A6            411             setb    P_R
02EC 7800            412             mov     R0,#0
                     413     ;
02EE 75B0DF          414     TUNGGU: mov     P3,#11011111b
02F1 209705          415             jb      Y3,DERING
02F4 3097FD          416             jnb     Y3,$
02F7 611B            417             ajmp    AUDIO
                     418     ;
                     419     DERING:
02F9 B83E02          420             cjne    R0,#3Eh,SPEAK
02FC 6108            421             ajmp    ON_HOOK
                     422     ;
                     423     SPEAK:
02FE B83B02          424             cjne    R0,#3Bh,NETRAL
0301 413C            425             ajmp    AREK
                     426     ;
                     427     NETRAL:
0303 B83CE8          428             cjne    R0,#3Ch,TUNGGU
0306 41D9            429             ajmp    BEBAS
                     430     ;
                     431     ;----------------------------
                     432     ; hook diangkat
                     433     ;----------------------------
                     434     ON_HOOK:
0308 9004DE          435             mov     dptr,#BREAK
```

```
LOC  OBJ             LINE     SOURCE

030B 11DE             436              acall   HOME
030D 11F6             437              acall   STRING
030F 11EA             438              acall   GANTI
0311 11F6             439              acall   STRING
0313 7800             440              mov     R0,#0
0315 00               441     DLH:     nop
0316 B83CFC           442              cjne    R0,#3Ch,DLH
0319 41D9             443              ajmp    BEBAS
                      444     ;
                      445     ;----------------------------
                      446     ; prosedur set suara isd
                      447     ;----------------------------
031B C2AF             448     AUDIO:   clr     EA
031D C2AC             449              clr     ES
031F 90054E           450              mov     dptr,#MENU6
0322 11DE             451              acall   HOME
0324 11F6             452              acall   STRING
0326 11EA             453              acall   GANTI
0328 11F6             454              acall   STRING
032A 75B0DF           455     AUDI1:   mov     P3,#11011111b
032D 20B602           456              jb      Y1,AUDI2
0330 41D9             457              ajmp    BEBAS
                      458     ;
                      459
0332 75B0DF           460     AUDI2:   mov     P3,#11011111b
0335 20B702           461              jb      Y2,AUDI3
0338 61A9             462              ajmp    INFO
033A 75B0DF           463     AUDI3:   mov     P3,#11011111b
033D 2097EA           464              jb      Y3,AUDI1
0340 90053E           465              mov     dptr,#MENU5
0343 11DE             466              acall   HOME
0345 11F6             467              acall   STRING
0347 90052E           468              mov     dptr,#MENU4
034A 11EA             469              acall   GANTI
034C 11F6             470              acall   STRING
034E 7C00             471              mov     R4,#0
                      472     ;
                      473     E_AUDIO:
0350 3129             474              acall   TOMBOL
0352 BB3005           475              cjne    R3,#30h,AUDIO1
0355 75A0EE           476              mov     ISD,#0EEh
0358 61D8             477              ajmp    RECORD
035A BB3105           478     AUDIO1:  cjne    R3,#31h,AUDIO2
035D 75A0EF           479              mov     ISD,#0EFh
0360 61D8             480              ajmp    RECORD
0362 BB3205           481     AUDIO2:  cjne    R3,#32h,AUDIO3
0365 75A0F0           482              mov     ISD,#0F0h
0368 61D8             483              ajmp    RECORD
036A BB3305           484     AUDIO3:  cjne    R3,#33h,AUDIO4
036D 75A0F1           485              mov     ISD,#0F1h
0370 61D8             486              ajmp    RECORD
0372 BB3405           487     AUDIO4:  cjne    R3,#34h,AUDIO5
0375 75A0F2           488              mov     ISD,#0F2h
0378 61D8             489              ajmp    RECORD
037A BB3505           490     AUDIO5:  cjne    R3,#35h,AUDIO6
```

```
LOC  OBJ            LINE     SOURCE

037D 75A0F3          491             mov     ISD,#0F3h
0380 61D8            492             ajmp    RECORD
0382 BB3605          493     AUDIO6: cjne    R3,#36h,AUDIO7
0385 75A0F4          494             mov     ISD,#0F4h
0388 61D8            495             ajmp    RECORD
038A BB3705          496     AUDIO7: cjne    R3,#37h,AUDIO8
038D 75A0F5          497             mov     ISD,#0F5h
0390 61D8            498             ajmp    RECORD
0392 BB3805          499     AUDIO8: cjne    R3,#38h,AUDIO9
0395 75A0F6          500             mov     ISD,#0F6h
0398 61D8            501             ajmp    RECORD
039A BB3905          502     AUDIO9: cjne    R3,#39h,AUDIOAA
039D 75A0F7          503             mov     ISD,#0F7h
03A0 61D8            504             ajmp    RECORD
                     505     AUDIOAA:
03A2 BB3A02          506             cjne    R3,#3Ah,AUT
03A5 41D9            507             ajmp    BEBAS
                     508     ;
03A7 6150            509     AUT:    ajmp    E_AUDIO
                     510     ;
                     511     ;-----------------------------
                     512     ; perekaman info
                     513     ;-----------------------------
03A9 90056E          514     INFO:   mov     dptr,#MENU7
03AC 11DE            515             acall   HOME
03AE 11F6            516             acall   STRING
03B0 90052E          517             mov     dptr,#MENU4
03B3 11EA            518             acall   GANTI
03B5 11F6            519             acall   STRING
03B7 7C01            520             mov     R4,#1
                     521     E_INFO:
03B9 3129            522             acall   TOMBOL
03BB BB3105          523             cjne    R3,#31h,INFO1
03BE 75A0E0          524             mov     ISD,#0E0h
03C1 61D8            525             ajmp    RECORD
03C3 BB3205          526     INFO1:  cjne    R3,#32h,INFO2
03C6 75A0F9          527             mov     ISD,#0F9h
03C9 61D8            528             ajmp    RECORD
03CB BB3305          529     INFO2:  cjne    R3,#33h,E_INFO2
03CE 75A0FB          530             mov     ISD,#0FBh
03D1 61D8            531             ajmp    RECORD
                     532     E_INFO2:
03D3 BB3AE3          533             cjne    R3,#3Ah,E_INFO
03D6 41D9            534             ajmp    BEBAS
                     535     ;
                     536     ;-----------------------------
                     537     ; perekaman suara
                     538     ;-----------------------------
03D8 C292            539     RECORD: clr     SOUND
03DA C293            540             clr     LOAD
03DC 11D2            541             acall   CLEAR
03DE 7904            542             mov     R1,#4
03E0 D291            543             setb    RS
03E2 758020          544     PL:     mov     LCD,#20h
03E5 11C9            545             acall   SEND
```

```
LOC  OBJ            LINE     SOURCE

03E7 D9F9            546              djnz    R1,PL
03E9 75804E          547              mov     LCD,#4Eh
03EC 11C9            548              acall   SEND
03EE 75804F          549              mov     LCD,#4Fh
03F1 11C9            550              acall   SEND
03F3 758020          551              mov     LCD,#20h
03F6 11C9            552              acall   SEND
03F8 8B80            553              mov     LCD,R3
03FA 11C9            554              acall   SEND
03FC C2A6            555              clr     P_R
03FE C2A7            556              clr     PD_CE
0400 75B0DF          557              mov     P3,#11011111b
0403 2097FD          558              jb      Y3,$
0406 D2A7            559              setb    PD_CE
0408 D2A6            560              setb    P_R
040A 1196            561              acall   LDELAY
040C 1196            562              acall   LDELAY
040E 1196            563              acall   LDELAY
0410 C2A7            564              clr     PD_CE
0412 20A5FD          565     PLY:     jb      EOM,$
0415 D2A7            566              setb    PD_CE
                     567     ;
0417 BC0002          568              cjne    R4,#0,E_PLY
041A 6150            569              ajmp    E_AUDIO
                     570     ;
041C 61B9            571     E_PLY:   ajmp    E_INFO
                     572     ;
                     573     ;----------------------------
                     574     ; Data-data Tulisan dan String
                     575     ;----------------------------
                     576     ;
041E 20414C41        577     JUDUL:   DB      ' ALAT  PENJAWAB '
0422 54202050
0426 454E4A41
042A 57414220
042E 54454C50        578              DB      'TELPHONE OTOMAT '
0432 484F4E45
0436 204F544F
043A 4D415420
043E 20202020        579              DB      '    BERBASIS    '
0442 42455242
0446 41534953
044A 20202020
044E 4D435520        580              DB      'MCU AT89S51 DAN '
0452 41543839
0456 53353120
045A 44414E20
045E 2052454E        581              DB      ' RENESAS R8C/13 '
0462 45534153
0466 20523843
046A 2F313320
046E 20484144        582              DB      ' HADI CAHYADI   '
0472 49204341
0476 48594144
047A 49202020
```

```
LOC  OBJ            LINE     SOURCE

047E 20202030        583            DB      '   01.17.112    '
0482 312E3137
0486 2E313132
048A 20202020
048E 20542E45        584            DB      ' T.ELEKTRONIKA  '
0492 4C454B54
0496 524F4E49
049A 4B412020
049E 20204954        585            DB      '  ITN   MALANG  '
04A2 4E202020
04A6 4D414C41
04AA 4E472020
04AE 54414855        586            DB      'TAHUN 2006/2007 '
04B2 4E203230
04B6 30362F32
04BA 30303720
04BE 20202052        587     MENU:  DB      '   READY !!!    '
04C2 45414459
04C6 20212121
04CA 20202020
04CE 20202020        588            DB      '                '
04D2 20202020
04D6 20202020
04DA 20202020
04DE 53454441        589     BREAK: DB      'SEDANG MELAKUKAN'
04E2 4E47204D
04E6 454C414B
04EA 554B414E
04EE 20205045        590            DB      '  PEMBICARAAN   '
04F2 4D424943
04F6 41524141
04FA 4E202020
04FE 50414E47        591     MENU2: DB      'PANGGILAN MASUK '
0502 47494C41
0506 4E204D41
050A 53554B20
050E 53494C41        592            DB      'SILAHKAN TUNGGU '
0512 484B414E
0516 2054554E
051A 47475520
051E 47414E54        593     MENU3: DB      'GANTI PERSONIL ?'
0522 49205045
0526 52534F4E
052A 494C203F
052E 4F4B2028        594     MENU4: DB      'OK (#)  ESC (*) '
0532 23292020
0536 45534320
053A 282A2920
053E 20205445        595     MENU5: DB      '  TEKAN 0 - 9   '
0542 4B414E20
0546 30202D20
054A 39202020
054E 52454B41        596     MENU6: DB      'REKAM NAMA (#)  '
0552 4D204E41
0556 4D412028
```

```
LOC  OBJ            LINE     SOURCE

055A 23292020
055E 494E464F        597             DB      'INFO (0) ESC (*)'
0562 20283029
0566 20455343
056A 20282A29
056E 54454B41        598     MENU7:  DB      'TEKAN 1, 2 DAN 3'
0572 4E20312C
0576 20322044
057A 414E2033
                     599     ;
                     600             End
```

SYMBOL TABLE LISTING
------ ----- -------

N A M E	T Y P E	V A L U E	A T T R I B U T E S
ACC. . . .	D ADDR	00E0H	A
ANGKA_A. .	C ADDR	0168H	A
ANGKA_B. .	C ADDR	0177H	A
ANGKA0 . .	C ADDR	0171H	A
ANGKA2 . .	C ADDR	0132H	A
ANGKA3 . .	C ADDR	0138H	A
ANGKA4 . .	C ADDR	013EH	A
ANGKA5 . .	C ADDR	0147H	A
ANGKA6 . .	C ADDR	014DH	A
ANGKA7 . .	C ADDR	0153H	A
ANGKA8 . .	C ADDR	015CH	A
ANGKA9 . .	C ADDR	0162H	A
AREK . . .	C ADDR	023CH	A
AUDI1. . .	C ADDR	032AH	A
AUDI2. . .	C ADDR	0332H	A
AUDI3. . .	C ADDR	033AH	A
AUDIO. . .	C ADDR	031BH	A
AUDIO1 . .	C ADDR	035AH	A
AUDIO2 . .	C ADDR	0362H	A
AUDIO3 . .	C ADDR	036AH	A
AUDIO4 . .	C ADDR	0372H	A
AUDIO5 . .	C ADDR	037AH	A
AUDIO6 . .	C ADDR	0382H	A
AUDIO7 . .	C ADDR	038AH	A
AUDIO8 . .	C ADDR	0392H	A
AUDIO9 . .	C ADDR	039AH	A
AUDIOAA. .	C ADDR	03A2H	A
AUT. . . .	C ADDR	03A7H	A
AWAL . . .	C ADDR	00FEH	A
BEBAS. . .	C ADDR	02D9H	A
BREAK. . .	C ADDR	04DEH	A
BUFER. . .	NUMB	0030H	A
CLEAR. . .	C ADDR	00D2H	A
CODE0. . .	C ADDR	0187H	A
CODE1. . .	C ADDR	0195H	A
CODE2. . .	C ADDR	01A3H	A
CODE3. . .	C ADDR	01B1H	A
CODE4. . .	C ADDR	01BFH	A
CODE5. . .	C ADDR	01CDH	A
CODE6. . .	C ADDR	01DBH	A
CODE7. . .	C ADDR	01E9H	A
CODE8. . .	C ADDR	01F7H	A
CODE9. . .	C ADDR	0205H	A
CODEK. . .	C ADDR	0182H	A
CODES. . .	C ADDR	017DH	A
DEL1 . . .	C ADDR	008FH	A
DEL2 . . .	C ADDR	0091H	A
DELAY. . .	C ADDR	008DH	A
DERING . .	C ADDR	02F9H	A
DLH. . . .	C ADDR	0315H	A
DPH. . . .	D ADDR	0083H	A

N A M E	T Y P E	V A L U E	A T T R I B U T E S
DPL. . . .	D ADDR	0082H	A
E_AUDIO. .	C ADDR	0350H	A
E_CODE . .	C ADDR	0213H	A
E_INFO . .	C ADDR	03B9H	A
E_INFO2. .	C ADDR	03D3H	A
E_PLY. . .	C ADDR	041CH	A
E_S. . . .	C ADDR	0086H	A
EA	B ADDR	00A8H.7	A
ENABLE . .	B ADDR	0090H.0	A
EOM. . . .	B ADDR	00A0H.5	A
ES	B ADDR	00A8H.4	A
GANTI. . .	C ADDR	00EAH	A
HOME . . .	C ADDR	00DEH	A
INFO . . .	C ADDR	03A9H	A
INFO1. . .	C ADDR	03C3H	A
INFO2. . .	C ADDR	03CBH	A
INIT_LCD .	C ADDR	009FH	A
ISD. . . .	D ADDR	00A0H	A
JUDUL. . .	C ADDR	041EH	A
LCD. . . .	D ADDR	0080H	A
LDEL1. . .	C ADDR	0098H	A
LDEL2. . .	C ADDR	009AH	A
LDELAY . .	C ADDR	0096H	A
LOAD . . .	B ADDR	0090H.3	A
MENU . . .	C ADDR	04BEH	A
MENU2. . .	C ADDR	04FEH	A
MENU3. . .	C ADDR	051EH	A
MENU4. . .	C ADDR	052EH	A
MENU5. . .	C ADDR	053EH	A
MENU6. . .	C ADDR	054EH	A
MENU7. . .	C ADDR	056EH	A
MULAI. . .	C ADDR	028BH	A
NETRAL . .	C ADDR	0303H	A
NEXT1. . .	C ADDR	02BDH	A
ON_HOOK. .	C ADDR	0308H	A
P_R. . . .	B ADDR	00A0H.6	A
P0	D ADDR	0080H	A
P1	D ADDR	0090H	A
P2	D ADDR	00A0H	A
P3	D ADDR	00B0H	A
PD_CE. . .	B ADDR	00A0H.7	A
PL	C ADDR	03E2H	A
PLY. . . .	C ADDR	0412H	A
PROSES . .	C ADDR	02B8H	A
PSW. . . .	D ADDR	00D0H	A
PUTAR. . .	C ADDR	0222H	A
PUTAR2 . .	C ADDR	0218H	A
PUTARAN. .	C ADDR	0226H	A
RECORD . .	C ADDR	03D8H	A
RI	B ADDR	0098H.0	A
RS	B ADDR	0090H.1	A
S_CODE . .	C ADDR	0211H	A
S_SERI . .	C ADDR	0112H	A
SBUF . . .	D ADDR	0099H	A
SCON . . .	D ADDR	0098H	A

N A M E	T Y P E	V A L U E	A T T R I B U T E S
SEND . . .	C ADDR	00C9H	A
SOUND. . .	B ADDR	0090H.2	A
SP	D ADDR	0081H	A
SPEAK. . .	C ADDR	02FEH	A
STRING . .	C ADDR	00F6H	A
TH1. . . .	D ADDR	008DH	A
TI	B ADDR	0098H.1	A
TMOD . . .	D ADDR	0089H	A
TOMBOL . .	C ADDR	0129H	A
TR1. . . .	B ADDR	0088H.6	A
TUNGGU . .	C ADDR	02EEH	A
X1	B ADDR	00B0H.2	A
X2	B ADDR	00B0H.3	A
X3	B ADDR	00B0H.4	A
X4	B ADDR	00B0H.5	A
Y1	B ADDR	00B0H.6	A
Y2	B ADDR	00B0H.7	A
Y3	B ADDR	0090H.7	A

REGISTER BANK(S) USED: 0

ASSEMBLY COMPLETE, NO ERRORS FOUND

```
/************************************************************
*  FILE        : Main Acuan
*
*  Hadi@ITN MAlang
*  T. Elektro/Elka
*
*  DATE        :01-03-2007
************************************************************/

/************************************************************
*   Tempat deklarasi include
************************************************************/
#include    <stdio.h>
#include    "sfr_r813.h"                    /* Definition of the R8C/13 SFR
*/
#include    "inputan.h"                     /* Definisi dari fungsi kaki mcu
yang digunakan */


char data;
int Tanda;
//char lama;


/************************************************************
*   Tempat Subrutin /deklarasi prototype subrutin
************************************************************/
   // contoh: void Delay(void) {..source code Subrutin Delay..}

   // UART mode transfer

void uart1_init()
   {

      u1mr = 0x05;      //UART1 8 bits,1 stop bit,no parity, 9600 bps

    u1c0 = 0x00;

    ucon = 0x20;

    u1brg = 129;

      te_u1c1 = 1;      //transmit enabled

      }

void delay(char lama)
   {              // waktu tunda

      while ( lama-- > 0 )
      {

            asm("nop");
      }
      }

void transmit()
   {
```

```
      u1tb = data;                          //transmit buffer = data

      while ( ti_u1c1 == 0 );       // tunggu sampai semua data terkirim

      }


/***********************************************************************
*       Function : main()
*       program section
***********************************************************************/
void main()
{
      asm("FCLR I");                        /* Interrupt disable */
      prcr = 1;                             /* Protect off */
      cm13 = 1;                             /* X-in X-out */
      cm15 = 1;                             /* XCIN-XCOUT drive capacity
select bit : HIGH */
      cm05 = 0;                             /* X-in on */
      cm16 = 0;                             /* Main clock = No division mode
*/
      cm17 = 0;
      cm06 = 0;                             /* CM16 and CM17 enable */
      asm("nop");
      asm("nop");
      asm("nop");
      asm("nop");
      ocd2 = 0;                             /* Main clock change */
      prcr = 0;                             /* Protect on */


      // inisialisasi / panggilan ke subrutin inisialisasi
      // Contoh : pd1 = 0xFF; // direction port 1 diset sbg output semua

      uart1_init();

      asm("FSET I"); /* Interrupt enable */

//          p0_1 = HIGH;
//          p0_2 = HIGH;

        while (1)
            {
            // Taruh souce code main loop Anda di sini


             if (Hook == HIGH)
                {
                  delay (1000);
                  if (Hook == HIGH)
                  {
                    data = 0x3C;
                  transmit();
                    delay (1000);

                    while (Hook == HIGH)
                        {

                  if (Ring == LOW)
```

```
                {
                        data = 0x3B;
                              transmit();
                              delay (1000);

                              while (Ring == LOW)
                                    {    delay (200);    }

                        }


                        if (Std == HIGH)
                        {
                              data = DTMF;
                              data = data & 0x0F;
                              data = data | 0x30;
                              transmit();
                              delay (1000);

                              while (Std == HIGH)
                                    {    delay (200);     }
                        }

                        }
                }
                }



          if (Hook == LOW)

                {     delay (1000);

                      if (Hook == LOW)
                      {
                            data = 0x3E;
                            transmit();
                            delay (1000);

                            while (Hook == LOW)

                                  {   delay (200);        }

                      }

                  }

      }
}
```

Winbond Electronics Corp.

ISD2560/75/90/120

SINGLE-CHIP, MULTIPLE-MESSAGES, VOICE RECORD/PLAYBACK DEVICE 60-, 75-, 90-, AND 120-SECOND DURATION

Publication Release Date: May 2003
Revision 1.0

Winbond Electronics Corp.

1. GENERAL DESCRIPTION

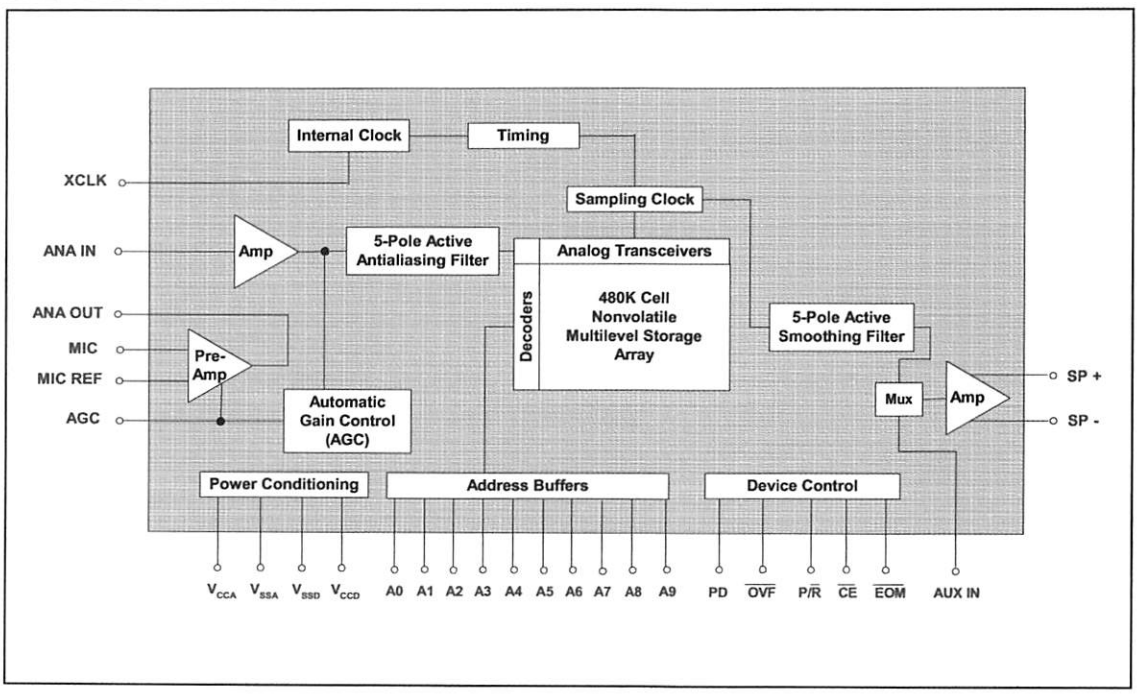
Winbond's ISD2500 ChipCorder® Series provide high-quality, single-chip, Record/Playback solutions for 60- to 120-second messaging applications. The CMOS devices include an on-chip oscillator, microphone preamplifier, automatic gain control, antialiasing filter, smoothing filter, speaker amplifier, and high density multi-level storage array. In addition, the ISD2500 is microcontroller compatible, allowing complex messaging and addressing to be achieved. Recordings are stored into on-chip nonvolatile memory cells, providing zero-power message storage. This unique, single-chip solution is made possible through Winbond's patented multilevel storage technology. Voice and audio signals are stored directly into memory in their natural form, providing high-quality, solid-state voice reproduction.

2. FEATURES

- Easy-to-use single-chip, voice record/playback solution
- High-quality, natural voice/audio reproduction
- Single-chip with duration of 60, 75, 90, or 120 seconds.
- Manual switch or microcontroller compatible
- Playback can be edge- or level-activated
- Directly cascadable for longer durations
- Automatic power-down (push-button mode)
  - Standby current 1 µA (typical)
- Zero-power message storage
  - Eliminates battery backup circuits
- Fully addressable to handle multiple messages
- 100-year message retention (typical)
- 100,000 record cycles (typical)
- On-chip clock source
- Programmer support for play-only applications
- Single +5 volt power supply
- Available in die form, PDIP, SOIC and TSOP packaging
- Temperature = die (0°C to +50°C) and package (0°C to +70°C)

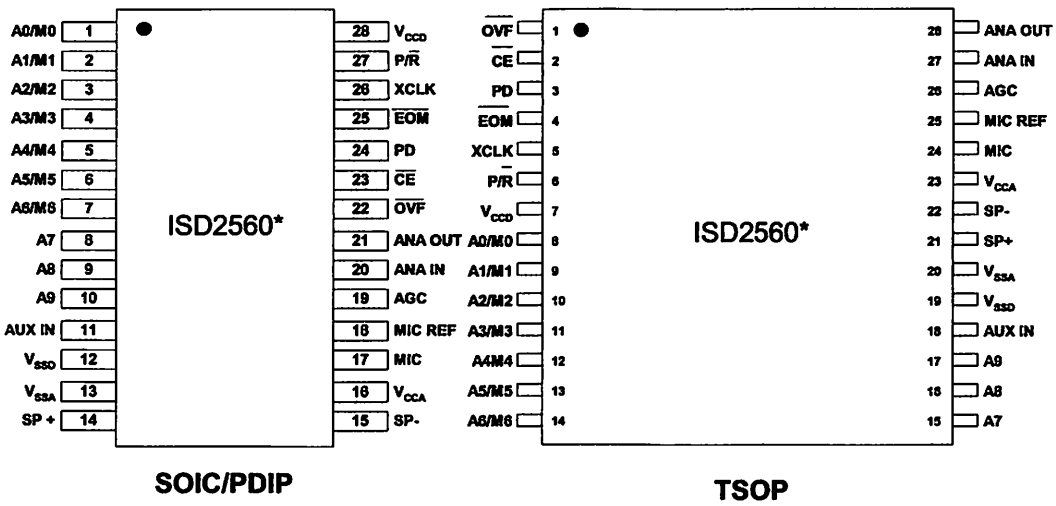
Winbond Electronics Corp.

3. BLOCK DIAGRAM



4. TABLE OF CONTENTS

5. PIN CONFIGURATION



* Same pinouts for ISD2575 / 2590 / 25120 products

6. PIN DESCRIPTION

PIN NAME	PIN NO.		FUNCTION
	SOIC/ PDIP	TSOP	
Ax/Mx	1-10/ 1-7	8-17/ 8-14	**Address/Mode Inputs**: The Address/Mode Inputs have two functions depending on the level of the two Most Significant Bits (MSB) of the address pins (A8 and A9). If either or both of the two MSBs are LOW, the inputs are all interpreted as address bits and are used as the start address for the current record or playback cycle. The address pins are inputs only and do not output any internal address information during the operation. Address inputs are latched by the falling edge of $\overline{CE}$. If both MSBs are HIGH, the Address/Mode inputs are interpreted as Mode bits according to the Operational Mode table on page 12. There are six operational modes (M0...M6) available as indicated in the table. It is possible to use multiple operational modes simultaneously. Operational Modes are sampled on each falling edge of $\overline{CE}$, and thus Operational Modes and direct addressing are mutually exclusive.
AUX IN	11	18	**Auxiliary Input:** The Auxiliary Input is multiplexed through to the output amplifier and speaker output pins when $\overline{CE}$ is HIGH, $\overline{P/R}$ is HIGH, and playback is currently not active or if the device is in playback overflow. When cascading multiple ISD2500 devices, the AUX IN pin is used to connect a playback signal from a following device to the previous output speaker drivers. For noise considerations, it is suggested that the auxiliary input not be driven when the storage array is active.
V_{SSA}, V_{SSD}	13, 12	20, 19	**Ground**: The ISD2500 series of devices utilizes separate analog and digital ground busses. These pins should be connected separately through a low-impedance path to power supply ground.
SP+/SP-	14/15	21/22	**Speaker Outputs**: All devices in the ISD2500 series include an on-chip differential speaker driver, capable of driving 50 mW into 16 Ω from AUX IN (12.2mW from memory). [1] The speaker outputs are held at V_{SSA} levels during record and power down. It is therefore not possible to parallel speaker outputs of multiple ISD2500 devices or the outputs of other speaker drivers. [2] A single-end output may be used (including a coupling capacitor between the SP pin and the speaker). These outputs may be used individually with the output signal taken from either pin. However, the use of single-end output results in a 1 to 4 reduction in its output power.

[1] Connection of speaker outputs in parallel may cause damage to the device.
[2] Never ground or drive an unused speaker output.

PIN NAME	PIN NO.		FUNCTION
	SOIC/ PDIP	TSOP	
V_{CCA}, V_{CCD}	16, 28	23, 7	**Supply Voltage**: To minimize noise, the analog and digital circuits in the ISD2500 series devices use separate power busses. These voltage busses are brought out to separate pins and should be tied together as close to the supply as possible. In addition, these supplies should be decoupled as close to the package as possible.
MIC	17	24	**Microphone**: The microphone pin transfers input signal to the on-chip preamplifier. A built-in Automatic Gain Control (AGC) circuit controls the gain of this preamplifier from –15 to 24dB. An external microphone should be AC coupled to this pin via a series capacitor. The capacitor value, together with the internal 10 KΩ resistance on this pin, determines the low-frequency cutoff for the ISD2500 series passband. See Winbond's Application Information for additional information on low-frequency cutoff calculation.
MIC REF	18	25	**Microphone Reference**: The MIC REF input is the inverting input to the microphone preamplifier. This provides a noise-canceling or common-mode rejection input to the device when connected to a differential microphone.
AGC	19	26	**Automatic Gain Control**: The AGC dynamically adjusts the gain of the preamplifier to compensate for the wide range of microphone input levels. The AGC allows the full range of whispers to loud sounds to be recorded with minimal distortion. The "attack" time is determined by the time constant of a 5 KΩ internal resistance and an external capacitor (C2 on the schematic of Figure 5 in section 11) connected from the AGC pin to V_{SSA} analog ground. The "release" time is determined by the time constant of an external resistor (R2) and an external capacitor (C2) connected in parallel between the AGC pin and V_{SSA} analog ground. Nominal values of 470 KΩ and 4.7 µF give satisfactory results in most cases.
ANA IN	20	27	**Analog Input**: The analog input transfers analog signal to the chip for recording. For microphone inputs, the ANA OUT pin should be connected via an external capacitor to the ANA IN pin. This capacitor value, together with the 3.0 KΩ input impedance of ANA IN, is selected to give additional cutoff at the low-frequency end of the voice passband. If the desired input is derived from a source other than a microphone, the signal can be fed, capacitively coupled, into the ANA IN pin directly.
ANA OUT	21	28	**Analog Output**: This pin provides the preamplifier output to the user. The voltage gain of the preamplifier is determined by the voltage level at the AGC pin.

PIN NAME	PIN NO.		FUNCTION
	SOIC/ PDIP	TSOP	
$\overline{OVF}$	22	1	**Overflow**: This signal pulses LOW at the end of memory array, indicating the device has been filled and the message has overflowed. The $\overline{OVF}$ output then follows the $\overline{CE}$ input until a PD pulse has reset the device. This pin can be used to cascade several ISD2500 devices together to increase record/playback durations.
$\overline{CE}$	23	2	**Chip Enable**: The $\overline{CE}$ input pin is taken LOW to enable all playback and record operations. The address pins and playback/record pin (P/$\overline{R}$) are latched by the falling edge of $\overline{CE}$. $\overline{CE}$ has additional functionality in the M6 (Push-Button) Operational Mode as described in the Operational Mode section.
PD	24	3	**Power Down**: When neither record nor playback operation, the PD pin should be pulled HIGH to place the part in standby mode (see I_{SB} specification). When overflow ($\overline{OVF}$) pulses LOW for an overflow condition, PD should be brought HIGH to reset the address pointer back to the beginning of the memory array. The PD pin has additional functionality in the M6 (Push-Button) Operation Mode as described in the Operational Mode section.
$\overline{EOM}$	25	4	**End-Of-Message**: A nonvolatile marker is automatically inserted at the end of each recorded message. It remains there until the message is recorded over. The $\overline{EOM}$ output pulses LOW for a period of T_{EOM} at the end of each message. In addition, the ISD2500 series has an internal V_{CC} detect circuit to maintain message integrity should V_{CC} fall below 3.5V. In this case, $\overline{EOM}$ goes LOW and the device is fixed in Playback-only mode. When the device is configured in Operational Mode M6 (Push-Button Mode), this pin provides an active-HIGH signal, indicating the device is currently recording or playing. This signal can conveniently drive an LED for visual indicator of a record or playback operation in process.

<table>
<tr><th rowspan="2">PIN NAME</th><th colspan="2">PIN NO.</th><th rowspan="2">FUNCTION</th></tr>
<tr><th>SOIC/ PDIP</th><th>TSOP</th></tr>
<tr><td>XCLK</td><td>26</td><td>5</td><td>External Clock: The external clock input has an internal pull-down device. The device is configured at the factory with an internal sampling clock frequency centered to ±1 percent of specification. The frequency is then maintained to a variation of ±2.25 percent over the entire commercial temperature and operating voltage ranges. If greater precision is required, the device can be clocked through the XCLK pin as follows:
<table>
<tr><th>Part Number</th><th>Sample Rate</th><th>Required Clock</th></tr>
<tr><td>ISD2560</td><td>8.0 kHz</td><td>1024 kHz</td></tr>
<tr><td>ISD2575</td><td>6.4 kHz</td><td>819.2 kHz</td></tr>
<tr><td>ISD2590</td><td>5.3 kHz</td><td>682.7 kHz</td></tr>
<tr><td>ISD25120</td><td>4.0 kHz</td><td>512 kHz</td></tr>
</table>
These recommended clock rates should not be varied because the antialiasing and smoothing filters are fixed, and aliasing problems can occur if the sample rate differs from the one recommended. The duty cycle on the input clock is not critical, as the clock is immediately divided by two. If the XCLK is not used, this input must be connected to ground.</td></tr>
<tr><td>P/$\overline{R}$</td><td>27</td><td>6</td><td>Playback/Record: The P/$\overline{R}$ input pin is latched by the falling edge of the $\overline{CE}$ pin. A HIGH level selects a playback cycle while a LOW level selects a record cycle. For a record cycle, the address pins provide the starting address and recording continues until PD or $\overline{CE}$ is pulled HIGH or an overflow is detected (i.e. the chip is full). When a record cycle is terminated by pulling PD or $\overline{CE}$ HIGH, then End-Of-Message ($\overline{EOM}$) marker is stored at the current address in memory. For a playback cycle, the address inputs provide the starting address and the device will play until an $\overline{EOM}$ marker is encountered. The device can continue to pass an $\overline{EOM}$ marker if $\overline{CE}$ is held LOW in address mode, or in an Operational Mode. (See Operational Modes section)</td></tr>
</table>

7. FUNCTIONAL DESCRIPTION

7.1. DETAILED DESCRIPTION

Speech/Sound Quality

The Winbond's ISD2500 series includes devices offered at 4.0, 5.3, 6.4, and 8.0 kHz sampling frequencies, allowing the user a choice of speech quality options. Increasing the duration within a product series decreases the sampling frequency and bandwidth, which affects the sound quality. Please refer to the ISD2560/75/90/120 Product Summary table below to compare the duration, sampling frequency and filter pass band.

The speech samples are stored directly into the on-chip nonvolatile memory without any digitization and compression associated like other solutions. Direct analog storage provides a very true, natural sounding reproduction of voice, music, tones, and sound effects not available with most solid state digital solutions.

Duration

To meet various system requirements, the ISD2560/75/90/120 products offer single-chip solutions at 60, 75, 90, and 120 seconds. Parts may also be cascaded together for longer durations.

TABLE 1: ISD2560/75/90/120 PRODUCT SUMMARY

Part Number	Duration (Seconds)	Input Sample Rate (kHz)	Typical Filter Pass Band * (kHz)
ISD2560	60	8.0	3.4
ISD2575	75	6.4	2.7
ISD2590	90	5.3	2.3
ISD25120	120	4.0	1.7

* 3db roll-off point

EEPROM Storage

One of the benefits of Winbond's ChipCorder® technology is the use of on-chip nonvolatile memory, providing zero-power message storage. The message is retained for up to 100 years typically without power. In addition, the device can be re-recorded typically over 100,000 times.

Microcontroller Interface

In addition to its simplicity and ease of use, the ISD2500 series includes all the interfaces necessary for microcontroller-driven applications. The address and control lines can be interfaced to a microcontroller and manipulated to perform a variety of tasks, including message assembly, message concatenation, predefined fixed message segmentation, and message management.

Programming

The ISD2500 series is also ideal for playback-only applications, where single or multiple messages are referenced through buttons, switches, or a microcontroller. Once the desired message configuration is created, duplicates can easily be generated via a gang programmer.

7.2. OPERATIONAL MODES

The ISD2500 series is designed with several built-in Operational Modes that provide maximum functionality with minimum external components. These modes are described in details as below. The Operational Modes are accessed via the address pins and mapped beyond the normal message address range. When the two Most Significant Bits (MSB), A8 and A9, are HIGH, the remaining address signals are interpreted as mode bits and not as address bits. Therefore, Operational Modes and direct addressing are not compatible and cannot be used simultaneously.

There are two important considerations for using Operational Modes. First, all operations begin initially at address 0 of its memory. Later operations can begin at other address locations, depending on the Operational Mode(s) chosen. In addition, the address pointer is reset to 0 when the device is changed from record to playback, playback to record (except M6 mode), or when a Power-Down cycle is executed.

Second, Operational Modes are executed when $\overline{CE}$ goes LOW. This Operational Mode remains in effect until the next LOW-going $\overline{CE}$ signal, at which point the current mode(s) are sampled and executed.

TABLE 2: OPERATIONAL MODES

Mode [1]	Function	Typical Use	Jointly Compatible [2]
M0	Message cueing	Fast-forward through messages	M4, M5, M6
M1	Delete $\overline{EOM}$ markers	Position $\overline{EOM}$ marker at the end of the last message	M3, M4, M5, M6
M2	Not applicable	Reserved	N/A
M3	Looping	Continuous playback from Address 0	M1, M5, M6
M4	Consecutive addressing	Record/playback multiple consecutive messages	M0, M1, M5
M5	$\overline{CE}$ level-activated	Allows message pausing	M0, M1, M3, M4
M6	Push-button control	Simplified device interface	M0, M1, M3

[1] Besides mode pin needed to be "1", A8 and A9 pin are also required to be "1" in order to enter into the related operational mode.

[2] Indicates additional Operational Modes which can be used simultaneously with the given mode.

7.2.1. Operational Modes Description

The Operational Modes can be used in conjunction with a microcontroller, or they can be hardwired to provide the desired system operation.

M0 – Message Cueing

Message Cueing allows the user to skip through messages, without knowing the actual physical addresses of each message. Each $\overline{CE}$ LOW pulse causes the internal address pointer to skip to the next message. This mode is used for playback only, and is typically used with the M4 Operational Mode.

M1 – Delete $\overline{EOM}$ Markers

The M1 Operational Mode allows sequentially recorded messages to be combined into a single message with only one $\overline{EOM}$ marker set at the end of the final message. When this Operational Mode is configured, messages recorded sequentially are played back as one continuous message.

M2 – Unused

When Operational Modes are selected, the M2 pin should be LOW.

M3 – Message Looping

The M3 Operational Mode allows for the automatic, continuously repeated playback of the message located at the beginning of the address space. A message can completely fill the ISD2500 device and will loop from beginning to end without $\overline{OVF}$ going LOW.

M4 – Consecutive Addressing

During normal operation, the address pointer will reset when a message is played through an $\overline{EOM}$ marker. The M4 Operational Mode inhibits the address pointer reset on $\overline{EOM}$, allowing messages to be played back consecutively.

M5 - $\overline{CE}$-Level Activated

The default mode for ISD2500 devices is for $\overline{CE}$ to be edge-activated on playback and level-activated on record. The M5 Operational Mode causes the $\overline{CE}$ pin to be interpreted as level-activated as opposed to edge-activated during playback. This is especially useful for terminating playback operations using the $\overline{CE}$ signal. In this mode, $\overline{CE}$ LOW begins a playback cycle, at the beginning of the device memory. The playback cycle continues as long as $\overline{CE}$ is held LOW. When $\overline{CE}$ goes HIGH, playback will immediately end. A new $\overline{CE}$ LOW will restart the message from the beginning unless M4 is also HIGH.

M6 – Push-Button Mode

The ISD2500 series contain a Push-Button Operational Mode. The Push-Button Mode is used primarily in very low-cost applications and is designed to minimize external circuitry and components, thereby reducing system cost. In order to configure the device in Push-Button Operational Mode, the two most significant address bits must be HIGH, and the M6 mode pin must also be HIGH. A device in this mode always powers down at the end of each playback or record cycle after $\overline{CE}$ goes HIGH.

When this operational mode is implemented, three of the pins on the device have alternate functionality as described in the table below.

TABLE 3: ALTERNATE FUNCTIONALITY IN PINS

Pin Name	Alternate Functionality in Push-Button Mode
$\overline{CE}$	Start/Pause Push-Button (LOW pulse-activated)
PD	Stop/Reset Push-Button (HIGH pulse-activated)
$\overline{EOM}$	Active-HIGH Run Indicator

$\overline{CE}$ (START/PAUSE)

In Push-Button Operational Mode, $\overline{CE}$ acts as a LOW-going pulse-activated START/PAUSE signal. If no operation is currently in progress, a LOW-going pulse on this signal will initiate a playback or record cycle according to the level on the P/$\overline{R}$ pin. A subsequent pulse on the $\overline{CE}$ pin, before an $\overline{EOM}$ is reached in playback or an overflow condition occurs, will pause the current operation, and the address counter is not reset. Another $\overline{CE}$ pulse will cause the device to continue the operation from the place where it is paused.

PD (STOP/RESET)

In Push-Button Operational Mode, PD acts as a HIGH-going pulse-activated STOP/RESET signal. When a playback or record cycle is in progress and a HIGH-going pulse is observed on PD, the current cycle is terminated and the address pointer is reset to address 0, the beginning of the message space.

$\overline{EOM}$ (RUN)

In Push-Button Operational Mode, $\overline{EOM}$ becomes an active-HIGH RUN signal which can be used to drive an LED or other external device. It is HIGH whenever a record or playback operation is in progress.

Recording in Push-Button Mode

1. The PD pin should be LOW, usually using a pull-down resistor.

2. The P/$\overline{R}$ pin is taken LOW.
3. The $\overline{CE}$ pin is pulsed LOW. Recording starts, $\overline{EOM}$ goes HIGH to indicate an operation in progress.
4. When the $\overline{CE}$ pin is pulsed LOW. Recording pauses, $\overline{EOM}$ goes back LOW. The internal address pointers are not cleared, but the $\overline{EOM}$ marker is stored in memory to indicate as the message end. The P/$\overline{R}$ pin may be taken HIGH at this time. Any subsequent $\overline{CE}$ would start a playback at address 0.
5. The $\overline{CE}$ pin is pulsed LOW. Recording starts at the next address after the previous set $\overline{EOM}$ marker. $\overline{EOM}$ goes back HIGH.[3]
6. When the recording sequences are finished, the final $\overline{CE}$ pulse LOW will end the last record cycle, leaving a set $\overline{EOM}$ marker at the message end. Recording may also be terminated by a HIGH level on PD, which will leave a set $\overline{EOM}$ marker.

Playback in Push-Button Mode

1. The PD pin should be LOW.
2. The P/$\overline{R}$ pin is taken HIGH.
3. The $\overline{CE}$ pin is pulsed LOW. Playback starts, $\overline{EOM}$ goes HIGH to indicate an operation in progress.
4. If the $\overline{CE}$ pin is pulsed LOW or an $\overline{EOM}$ marker is encountered during an operation, the part will pause. The internal address pointers are not cleared, and $\overline{EOM}$ goes back LOW. The P/$\overline{R}$ pin may be changed at this time. A subsequent record operation would not reset the address pointers and the recording would begin where playback ended.
5. $\overline{CE}$ is again pulsed LOW. Playback starts where it left off, with $\overline{EOM}$ going HIGH to indicate an operation in progress.
6. Playback continues as in steps 4 and 5 until PD is pulsed HIGH or overflow occurs.
7. If in overflow, pulling $\overline{CE}$ LOW will reset the address pointer and start playback from the beginning. After a PD pulse, the part is reset to address 0.

Note: Push-Button Mode can be used in conjunction with modes M0, M1, and M3.

[3] If the M1 Operational Mode pin is also HIGH, the just previously written $\overline{EOM}$ bit is erased, and recording starts at that address.

Good Audio Design Practices

Winbond products are very high-quality single-chip voice recording and playback systems. To ensure the highest quality voice reproduction, it is important that good audio design practices on layout and power supply decoupling be followed. See Application Information or below links for details.

Good Audio Design Practices

http://www.winbond-usa.com/products/isd_products/chipcorder/applicationinfo/apin11.pdf

Single-Chip Board Layout Diagrams

http://www.winbond-usa.com/products/isd_products/chipcorder/applicationinfo/apin12.pdf

Winbond Electronics Corp.

8. TIMING DIAGRAMS

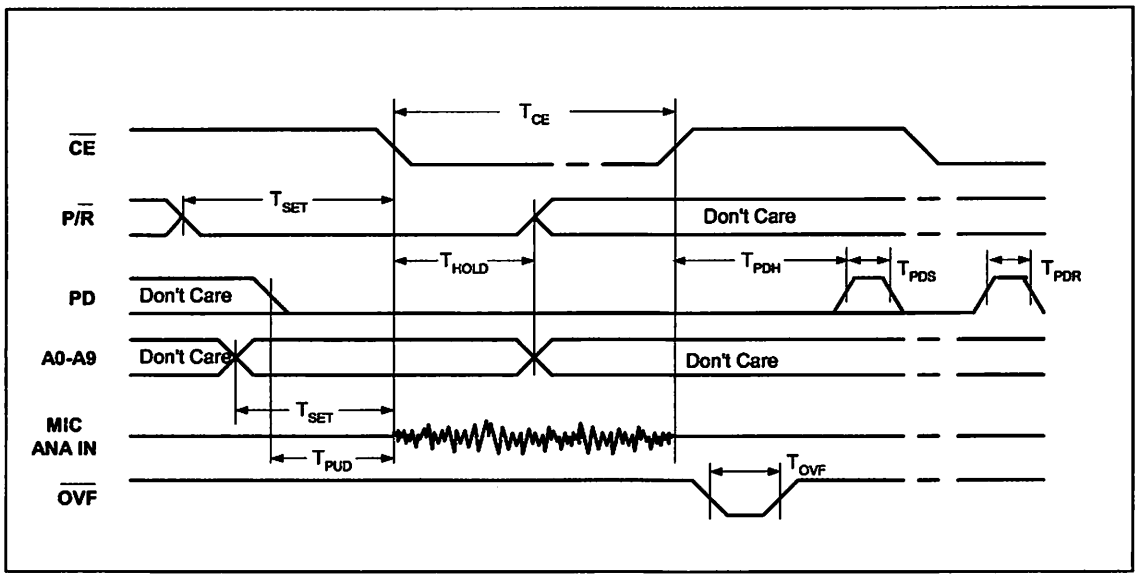


FIGURE 1: RECORD

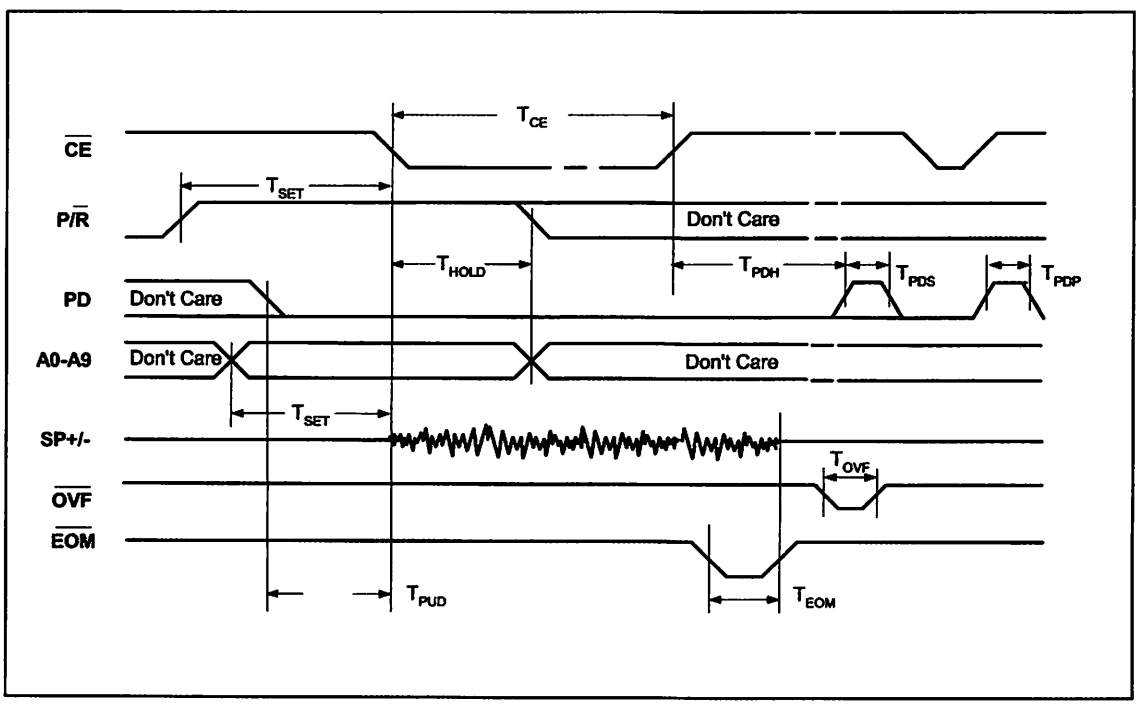


FIGURE 2: PLAYBACK

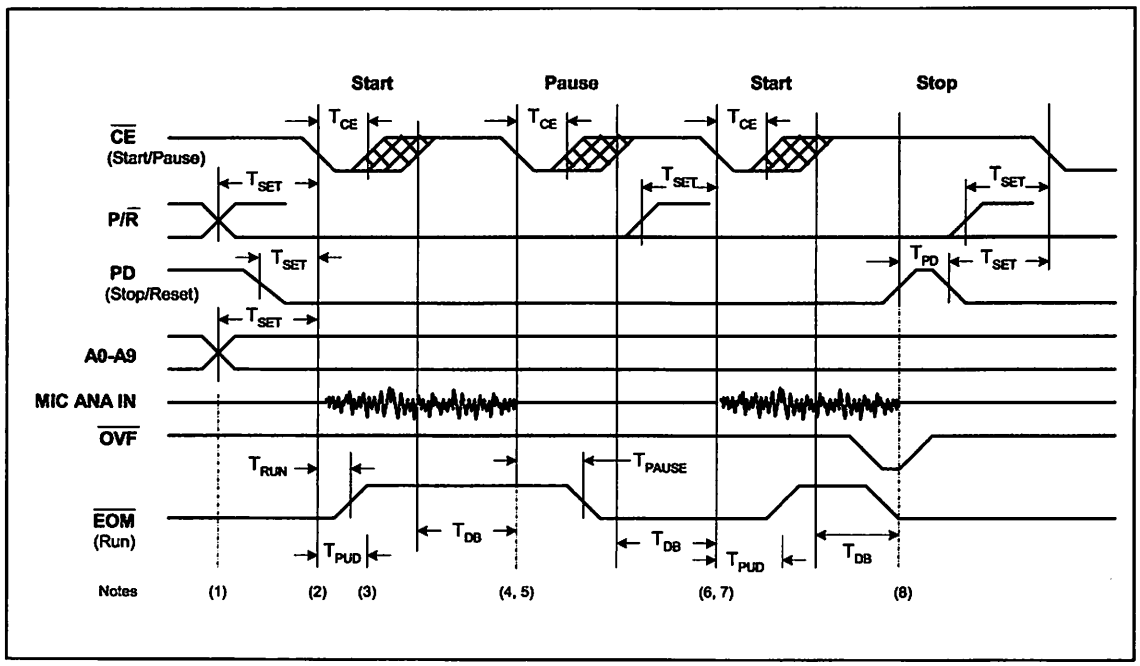


FIGURE 3: PUSH-BUTTON MODE RECORD

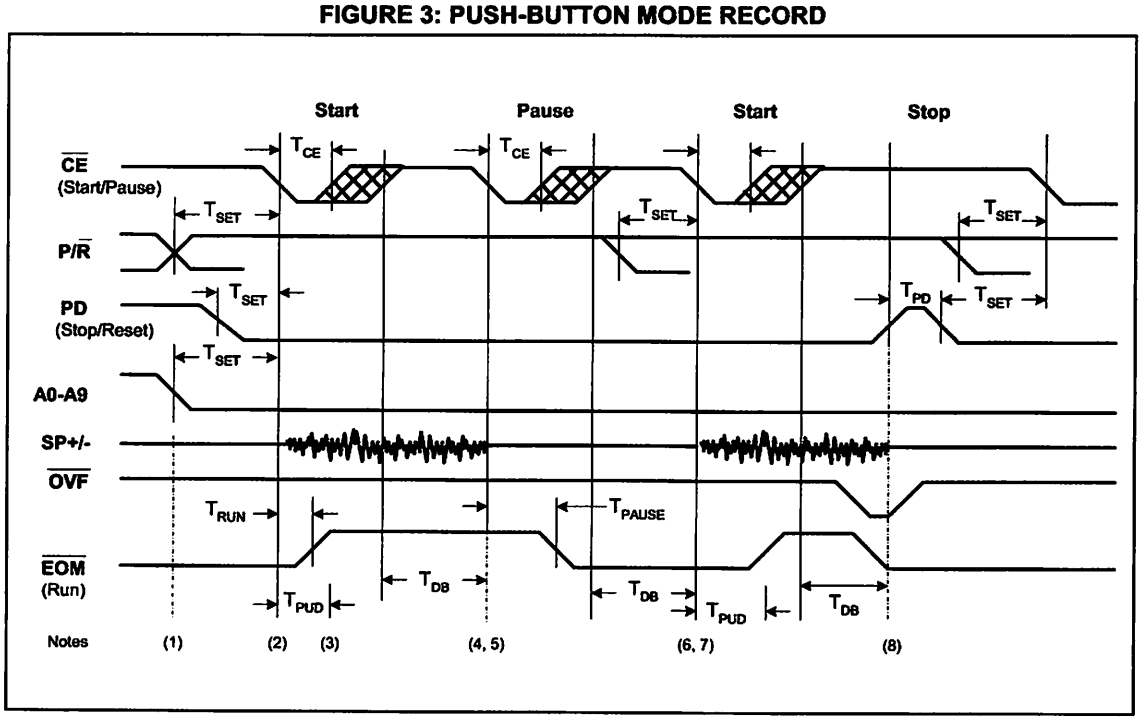


FIGURE 4: PUSH-BUTTON MODE PLAYBACK

Notes for Push-Button modes:

1. A9, A8, and A6 = 1 for push-button operation.
2. The first $\overline{CE}$ LOW pulse performs a start function.
3. The part will begin to play or record after a power-up delay T_{PUD}.
4. The part must have $\overline{CE}$ HIGH for a debounce period T_{DB} before it will recognize another falling edge of $\overline{CE}$ and pause.
5. The second $\overline{CE}$ LOW pulse, and every even pulse thereafter, performs a Pause function.
6. Again, the part must have $\overline{CE}$ HIGH for a debounce period T_{DB} before it will recognize another falling edge of $\overline{CE}$, which would restart an operation. In addition, the part will not do an internal power down until $\overline{CE}$ is HIGH for the T_{DB} time.
7. The third $\overline{CE}$ LOW pulse, and every odd pulse thereafter, performs a Resume function.
8. At any time, a HIGH level on PD will stop the current function, reset the address counter, and power down the device.

9. ABSOLUTE MAXIMUM RATINGS

TABLE 4: ABSOLUTE MAXIMUM RATINGS (DIE)

CONDITION	VALUE
Junction temperature	150°C
Storage temperature range	-65°C to +150°C
Voltage applied to any pad	(V_{SS} –0.3V) to (V_{CC} +0.3V)
Voltage applied to any pad (Input current limited to ±20mA)	(V_{SS} –1.0V) to (V_{CC} +1.0V)
$V_{CC} - V_{SS}$	-0.3V to +7.0V

TABLE 5: ABSOLUTE MAXIMUM RATINGS (PACKAGED PARTS)

CONDITION	VALUE
Junction temperature	150°C
Storage temperature range	-65°C to +150°C
Voltage applied to any pin	(V_{SS} –0.3V) to (V_{CC} +0.3V)
Voltage applied to any pin (Input current limited to ±20 mA)	(V_{SS} –1.0V) to (V_{CC} +1.0V)
Lead temperature (Soldering – 10sec)	300°C
$V_{CC} - V_{SS}$	-0.3V to +7.0V

Note: Stresses above those listed may cause permanent damage to the device. Exposure to the absolute maximum ratings may affect device reliability and performance. Functional operation is not implied at these conditions.

9.1 OPERATING CONDITIONS

TABLE 6: OPERATING CONDITIONS (DIE)

CONDITION	VALUE
Commercial operating temperature range	0°C to +50°C
Supply voltage (V_{CC}) [1]	+4.5V to +6.5V
Ground voltage (V_{SS}) [2]	0V

TABLE 7: OPERATING CONDITIONS (PACKAGED PARTS)

CONDITION	VALUE
Commercial operating temperature range [3]	0°C to +70°C
Supply voltage (V_{CC}) [1]	+4.5V to +5.5V
Ground voltage (V_{SS}) [2]	0V

[1] $V_{CC} = V_{CCA} = V_{CCD}$

[2] $V_{SS} = V_{SSA} = V_{SSD}$

[3] Case Temperature

10. ELECTRICAL CHARACTERISTICS

10.1. PARAMETERS FOR PACKAGED PARTS

TABLE 8: DC PARAMETERS – Packaged Parts

PARAMETER	SYMBOL	MIN[2]	TYP[1]	MAX[2]	UNITS	CONDITIONS
Input Low Voltage	V_{IL}			0.8	V	
Input High Voltage	V_{IH}	2.0			V	
Output Low Voltage	V_{OL}			0.4	V	I_{OL} = 4.0 mA
Output High Voltage	V_{OH}	V_{CC} - 0.4			V	I_{OH} = -10 µA
$\overline{OVF}$ Output High Voltage	V_{OH1}	2.4			V	I_{OH} = -1.6 mA
$\overline{EOM}$ Output High Voltage	V_{OH2}	V_{CC} – 1.0	V_{CC} - 0.8		V	I_{OH} = -3.2 mA
V_{CC} Current (Operating)	I_{CC}		25	30	mA	R_{EXT} = ∞ [3]
V_{CC} Current (Standby)	I_{SB}		1	10	µA	[3]
Input Leakage Current	I_{IL}			±1	µA	
Input Current HIGH w/Pull Down	I_{ILPD}			130	µA	Force V_{CC} [4]
Output Load Impedance	R_{EXT}	16			Ω	Speaker Load
Preamp Input Resistance	R_{MIC}	4	9	15	KΩ	MIC and MIC REF Pins
AUX IN Input Resistance	R_{AUX}	5	11	20	KΩ	
ANA IN Input Resistance	$R_{ANA\ IN}$	2.3	3	5	KΩ	
Preamp Gain 1	A_{PRE1}	21	24	26	dB	AGC = 0.0V
Preamp Gain 2	A_{PRE2}		-15	5	dB	AGC = 2.5V
AUX IN/SP+ Gain	A_{AUX}		0.98	1.0	V/V	
ANA IN to SP+/- Gain	A_{ARP}	21	23	26	dB	
AGC Output Resistance	R_{AGC}	2.5	5	9.5	KΩ	

Notes:

[1] Typical values @ T_A = 25° and V_{CC} = 5.0V.

[2] All Min/Max limits are guaranteed by Winbond via electrical testing or characterization. Not all specifications are 100 percent tested.

[3] V_{CCA} and V_{CCD} connected together.

[4] XCLK pin only.

TABLE 9: AC PARAMETERS – Packaged Parts

CHARACTERISTIC	SYMBOL	MIN[2]	TYP[1]	MAX[2]	UNITS	CONDITIONS
Sampling Frequency	F_S					
ISD2560			8.0		kHz	[7]
ISD2575			6.4		kHz	[7]
ISD2590			5.3		kHz	[7]
ISD25120			4.0		kHz	[7]
Filter Pass Band	F_{CF}					
ISD2560			3.4		kHz	3 dB Roll-Off Point[3][8]
ISD2575			2.7		kHz	3 dB Roll-Off Point[3][8]
ISD2590			2.3		kHz	3 dB Roll-Off Point[3][8]
ISD25120			1.7		kHz	3 dB Roll-Off Point[3][8]
Record Duration	T_{REC}					
ISD2560		58.1	60.0	62.0	sec	Commercial Operation[7]
ISD2575		72.6	75.0	77.5	sec	Commercial Operation[7]
ISD2590		87.1	90.0	93.0	sec	Commercial Operation[7]
ISD25120		116.1	120.0	123.9	sec	Commercial Operation[7]
Playback Duration	T_{PLAY}					
ISD2560		58.1	60.0	62.0	sec	Commercial Operation
ISD2575		72.6	75.0	77.5	sec	Commercial Operation
ISD2590		87.1	90.0	93.0	sec	Commercial Operation
ISD25120		116.1	120.0	123.9	sec	Commercial Operation
$\overline{CE}$ Pulse Width	T_{CE}		100		nsec	
Control/Address Setup Time	T_{SET}		300		nsec	
Control/Address Hold Time	T_{HOLD}		0		nsec	
Power-Up Delay	T_{PUD}					
ISD2560		24.1	25.0	27.8	msec	Commercial Operation
ISD2575		30.2	31.3	34.3	msec	Commercial Operation
ISD2590		36.2	37.5	40.8	msec	Commercial Operation
ISD25120		48.2	50.0	53.6	msec	Commercial Operation
PD Pulse Width (record)	T_{PDR}					
ISD2560			25.0		msec	
ISD2575			31.25		msec	
ISD2590			37.5		msec	
ISD25120			50.0		msec	

TABLE 9: AC PARAMETERS – Packaged Parts (Cont'd)

CHARACTERISTIC	SYMBOL	MIN[2]	TYP[1]	MAX[2]	UNITS	CONDITIONS
PD Pulse Width (Play)	T_{PDP}					
ISD2560			12.5		msec	
ISD2575			15.625		msec	
ISD2590			18.75		msec	
ISD25120			25.0		msec	
PD Pulse Width (Static)	T_{PDS}		100		nsec	[6]
Power Down Hold	T_{PDH}		0		nsec	
$\overline{EOM}$ Pulse Width	T_{EOM}					
ISD2560			12.5		msec	
ISD2575			15.625		msec	
ISD2590			18.75		msec	
ISD25120			25.0		msec	
Overflow Pulse Width	T_{OVF}		6.5		µsec	
Total Harmonic Distortion	THD		1	2	%	@ 1 kHz
Speaker Output Power	P_{OUT}		12.2	50	mW	R_{EXT} = 16 Ω[4]
Voltage Across Speaker Pins	V_{OUT}			2.5	V p-p	R_{EXT} = 600 Ω
MIC Input Voltage	V_{IN1}			20	mV	Peak-to-Peak[5]
ANA IN Input Voltage	V_{IN2}			50	mV	Peak-to-Peak
AUX Input Voltage	V_{IN3}			1.25	V	Peak-to-Peak; R_{EXT} = 16 Ω

Notes:

[1] Typical values @ T_A = 25°C and V_{CC} = 5.0V.

[2] All Min/Max limits are guaranteed by Winbond via electrical testing or characterization. Not all specifications are 100 percent tested.

[3] Low-frequency cutoff depends upon the value of external capacitors (see Pin Descriptions)

[4] From AUX IN; if ANA IN is driven at 50 mV p-p, the P_{OUT} = 12.2 mW, typical.

[5] With 5.1 K Ω series resistor at ANA IN.

[6] T_{PDS} is required during a static condition, typically overflow.

[7] Sampling Frequency and playback Duration can vary as much as ±2.25 percent over the commercial temperature range. For greater stability, an external clock can be utilized (see Pin Descriptions)

[8] Filter specification applies to the antialiasing filter and the smoothing filter. Therefore, from input to output, expect a 6 dB drop by nature of passing through both filters.

10.1.1. Typical Parameter Variation with Voltage and Temperature (Packaged Parts)

Chart 1: Record Mode Operating Current (I_{CC})

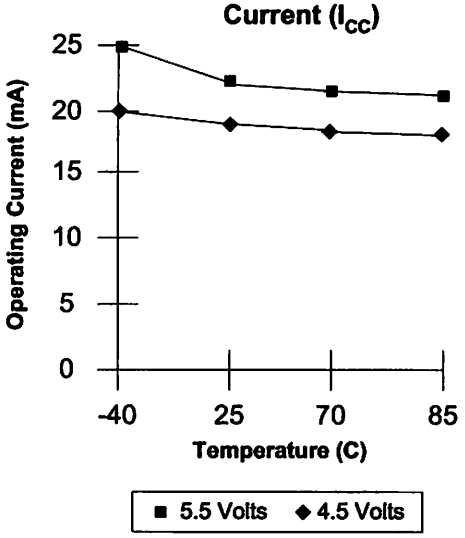


Chart 3: Standby Current (I_{SB})

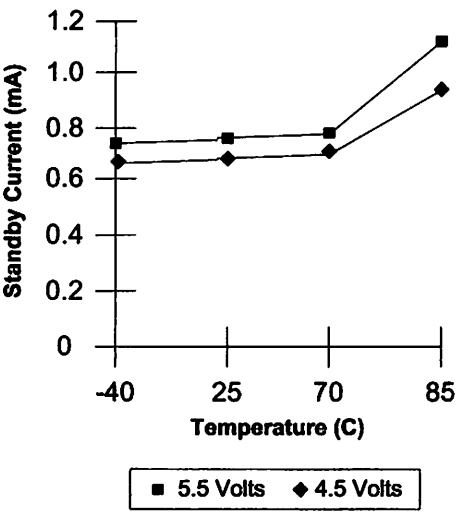


Chart 2: Total Harmonic Distortion

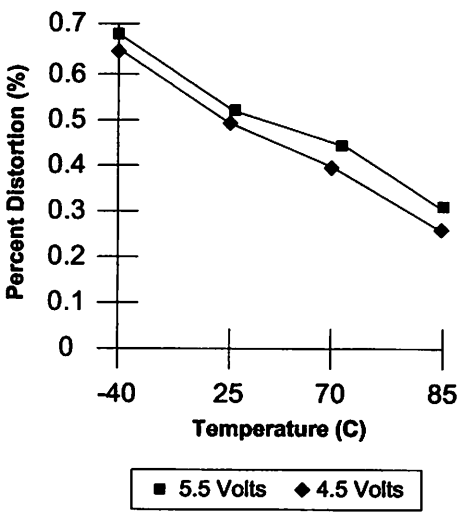
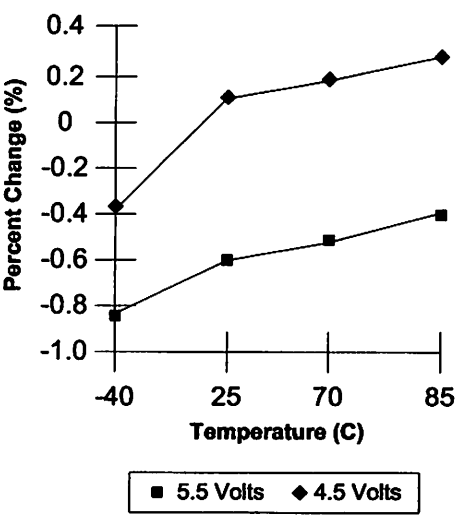


Chart 4: Oscillator Stability



10.2. PARAMETERS FOR DIE

TABLE 10: DC PARAMETERS – Die

PARAMETER	SYMBOL	MIN[2]	TYP[1]	MAX[2]	UNITS	CONDITIONS
Input Low Voltage	V_{IL}			0.8	V	
Input High Voltage	V_{IH}	2.0			V	
Output Low Voltage	V_{OL}			0.4	V	I_{OL} = 4.0 mA
Output High Voltage	V_{OH}	V_{CC} - 0.4			V	I_{OH} = -10 µA
$\overline{OVF}$ Output High Voltage	V_{OH1}	2.4			V	I_{OH} = -1.6 mA
$\overline{EOM}$ Output High Voltage	V_{OH2}	V_{CC} – 1.0	V_{CC} - 0.8		V	I_{OH} = -3.2 mA
V_{CC} Current (Operating)	I_{CC}		25	30	mA	R_{EXT} = ∞ [3]
V_{CC} Current (Standby)	I_{SB}		1	10	µA	[2]
Input Leakage Current	I_{IL}			±1	µA	
Input Current HIGH w/Pull Down	I_{ILPD}			130	µA	Force V_{CC} [4]
Output Load Impedance	R_{EXT}	16			Ω	Speaker Load
Preamp IN Input Resistance	R_{MIC}	4	9	15	KΩ	MIC and MIC REF Pads
AUX IN Input Resistance	R_{AUX}	5	11	20	KΩ	
ANA IN Input Resistance	$R_{ANA\ IN}$	2.3	3	5	KΩ	
Preamp Gain 1	A_{PRE1}	21	24	26	dB	AGC = 0.0V
Preamp Gain 2	A_{PRE2}		-15	5	dB	AGC = 2.5V
AUX IN/SP+ Gain	A_{AUX}		0.98	1.0	V/V	
ANA IN to SP+/- Gain	A_{ARP}	21	23	26	dB	
AGC Output Resistance	R_{AGC}	2.5	5	9.5	KΩ	

Notes:

[1] Typical values @ T_A = 25°C and V_{CC} = 5.0V.

[2] All Min/Max limits are guaranteed by Winbond via electrical testing or characterization. Not all specifications are 100 percent tested.

[3] V_{CCA} and V_{CCD} connected together.

[4] XCLK pad only.

TABLE 11: AC PARAMETERS – Die

CHARACTERISTIC	SYMBOL	MIN[2]	TYP[1]	MAX[2]	UNITS	CONDITIONS
Sampling Frequency	F_S					
ISD2560			8.0		kHz	[7]
ISD2575			6.4		kHz	[7]
ISD2590			5.3		kHz	[7]
ISD25120			4.0		kHz	[7]
Filter Pass Band	F_{CF}					
ISD2560			3.4		kHz	3 dB Roll-Off Point[3][8]
ISD2575			2.7		kHz	3 dB Roll-Off Point[3][8]
ISD2590			2.3		kHz	3 dB Roll-Off Point[3][8]
ISD25120			1.7		kHz	3 dB Roll-Off Point[3][8]
Record Duration	T_{REC}					
ISD2560		58.1	60.0	62.0	sec	Commercial Operation[7]
ISD2575		72.6	75.0	77.5	sec	Commercial Operation[7]
ISD2590		87.1	90.0	93.0	sec	Commercial Operation[7]
ISD25120		116.1	120.0	123.9	sec	Commercial Operation[7]
Playback Duration	T_{PLAY}					
ISD2560		58.1	60.0	62.0	sec	Commercial Operation[7]
ISD2575		72.6	75.0	77.5	sec	Commercial Operation[7]
ISD2590		87.1	90.0	93.0	sec	Commercial Operation[7]
ISD25120		116.1	120.0	123.9	sec	Commercial Operation[7]
$\overline{CE}$ Pulse Width	T_{CE}		100		nsec	
Control/Address Setup Time	T_{SET}		300		nsec	
Control/Address Hold Time	T_{HOLD}		0		nsec	
Power-Up Delay	T_{PUD}					
ISD2560		24.1	25.0	27.8	msec	Commercial Operation
ISD2575		30.2	31.3	34.3	msec	Commercial Operation
ISD2590		36.2	37.5	40.8	msec	Commercial Operation
ISD25120		48.2	50.0	53.6	msec	Commercial Operation
PD Pulse Width (Record)	T_{PDR}					
ISD2560			25.0		msec	
ISD2575			31.25		msec	
ISD2590			37.5		msec	
ISD25120			50.0		msec	

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TABLE 11: AC PARAMETERS – Die (Cont'd)

CHARACTERISTIC	SYMBOL	MIN[2]	TYP[1]	MAX[2]	UNITS	CONDITIONS
PD Pulse Width (Play)	T_{PDP}					
ISD2560			12.5		msec	
ISD2575			15.625		msec	
ISD2590			18.75		msec	
ISD25120			25.0		msec	
PD Pulse Width (Static)	T_{PDS}		100		nsec	[6]
Power Down Hold	T_{PDH}		0		nsec	
$\overline{EOM}$ Pulse Width	T_{EOM}					
ISD2560			12.5		msec	
ISD2575			15.625		msec	
ISD2590			18.75		msec	
ISD25120			25.0		msec	
Overflow Pulse Width	T_{OVF}		6.5		µsec	
Total Harmonic Distortion	THD		1	3	%	@ 1 kHz
Speaker Output Power	P_{OUT}		12.2	50	mW	R_{EXT} = 16 Ω[4]
Voltage Across Speaker Pins	V_{OUT}			2.5	V p-p	R_{EXT} = 600 Ω
MIC Input Voltage	V_{IN1}			20	mV	Peak-to-Peak[5]
ANA IN Input Voltage	V_{IN2}			50	mV	Peak-to-Peak
AUX Input Voltage	V_{IN3}			1.25	V	Peak-to-Peak; R_{EXT} = 16 Ω

Notes:

[1] Typical values @ T_A = 25°C and V_{CC} = 5.0V.

[2] All Min/Max limits are guaranteed by Winbond via electrical testing or characterization. Not all specifications are 100 percent tested.

[3] Low-frequency cutoff depends upon the value of external capacitors (see Pin Descriptions)

[4] From AUX IN; if ANA IN is driven at 50 mV p-p, the P_{OUT} = 12.2 mW, typical.

[5] With 5.1 K Ω series resistor at ANA IN.

[6] T_{PDS} is required during a static condition, typically overflow.

[7] Sampling Frequency and playback Duration can vary as much as ±2.25 percent over the commercial temperature range. For greater stability, an external clock can be utilized (see Pin Descriptions)

[8] Filter specification applies to the antialiasing filter and the smoothing filter. Therefore, from input to output, expect a 6 dB drop by nature of passing through both filters.

10.2.1. Typical Parameter Variation with Voltage and Temperature (Die)

Chart 5: Record Mode Operating Current (I_{CC})

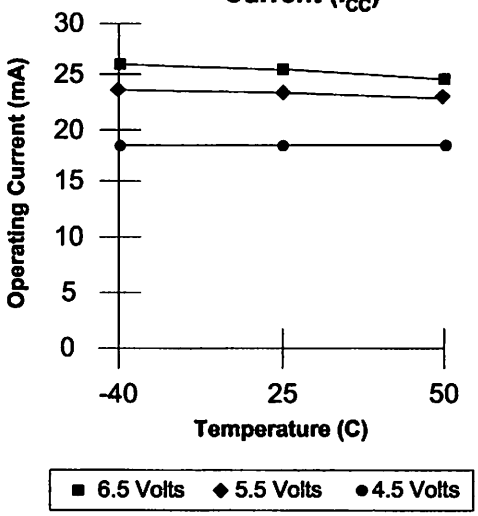


Chart 7: Standby Current (I_{SB})

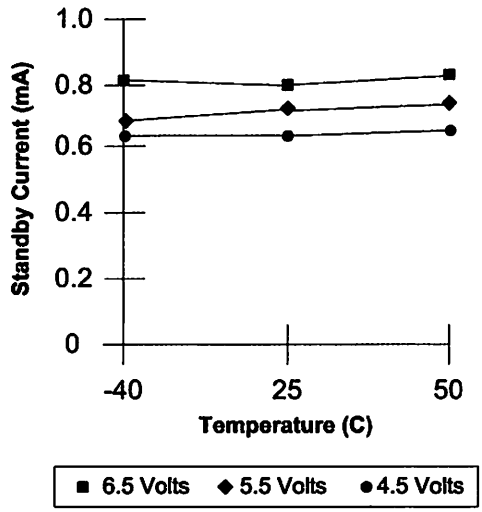


Chart 6: Total Harmonic Distortion

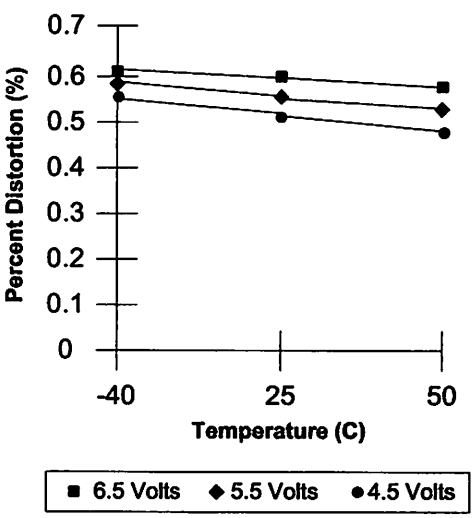
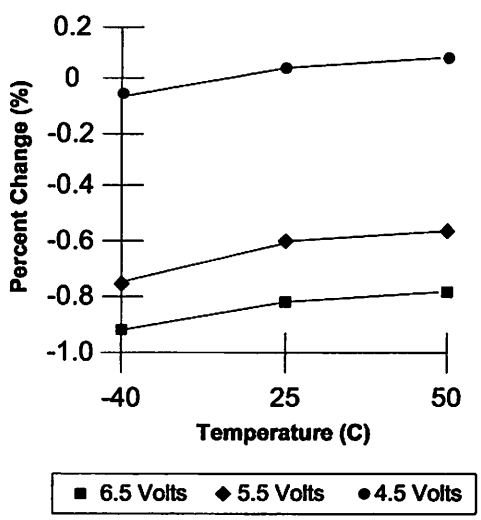


Chart 8: Oscillator Stability



10.3. PARAMETERS FOR PUSH-BUTTON MODE

TABLE 12: PARAMETERS FOR PUSH-BUTTON MODE

PARAMETER	SYMBOL	MIN[2]	TYP[1]	MAX[2]	UNITS	CONDITIONS
$\overline{CE}$ Pulse Width (Start/Pause)	T_{CE}		300		nsec	
Control/Address Setup Time	T_{SET}		300		nsec	
Power-Up Delay	T_{PUD}					
ISD2560			25.0		msec	
ISD2575			31.25		msec	
ISD2590			37.25		msec	
ISD25120			50.0		msec	
PD Pulse Width (Stop/Restart)	T_{PD}		300		nsec	
$\overline{CE}$ to $\overline{EOM}$ HIGH	T_{RUN}	25		400	nsec	
$\overline{CE}$ to $\overline{EOM}$ LOW	T_{PAUSE}	50		400	nsec	
$\overline{CE}$ HIGH Debounce	T_{DB}					
ISD2560		70		105	msec	
ISD2575		85		135	msec	
ISD2590		105		160	msec	
ISD25120		135		215	msec	

Notes:

[1] Typical values @ T_A = 25°C and V_{CC} = 5.0V.

[2] All Min/Max limits are guaranteed by Winbond via electrical testing or characterization. Not all specifications are 100 percent tested.

11. TYPICAL APPLICATION CIRCUIT

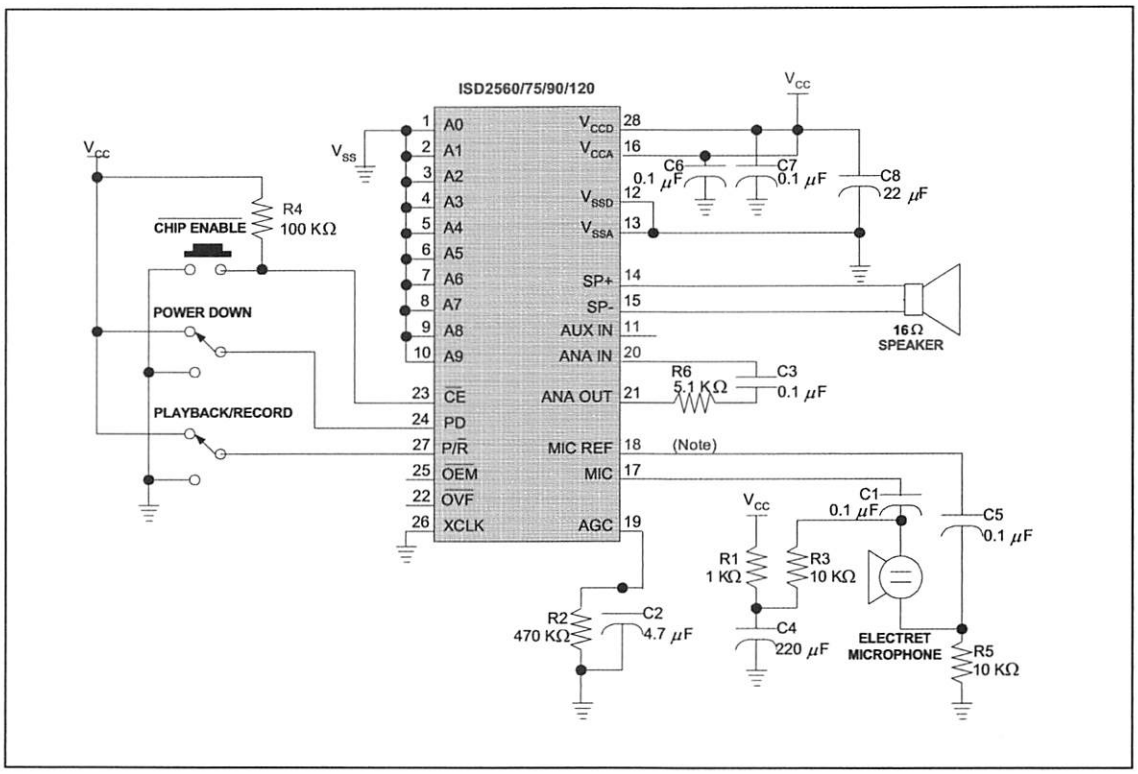


FIGURE 5: DESIGN SCHEMATIC

Note: If desired, pin 18 (PDIP package) may be left unconnected (microphone preamplifier noise will be higher). In this case, pin 18 must not be tied to any other signal or voltage. Additional design example schematics are provided below.

TABLE 13: APPLICATION EXAMPLE – BASIC DEVICE CONTROL

Control Step	Function	Action
1	Power up chip and select Record/Playback Mode	1. PD = LOW, 2. P/$\overline{R}$ = As desired
2	Set message address for record/playback	Set addresses A0-A9
3A	Begin playback	P/$\overline{R}$ = HIGH, $\overline{CE}$ = Pulse LOW
3B	Begin record	P/$\overline{R}$ = LOW, $\overline{CE}$ = LOW
4A	End playback	Automatic
4B	End record	PD or $\overline{CE}$ = HIGH

TABLE 14: APPLICATION EXAMPLE – PASSIVE COMPONENT FUNCTIONS

Part	Function	Comments
R1	Microphone power supply decoupling	Reduces power supply noise
R2	Release time constant	Sets release time for AGC
R3, R5	Microphone biasing resistors	Provides biasing for microphone operation
R4	Series limiting resistor	Reduces level to prevent distortion at higher supply voltages
R6	Series limiting resistor	Reduces level to high supply voltages
C1, C5	Microphone DC-blocking capacitor Low-frequency cutoff	Decouples microphone bias from chip. Provides single-pole low-frequency cutoff and command mode noise rejection.
C2	Attack/Release time constant	Sets attack/release time for AGC
C3	Low-frequency cutoff capacitor	Provides additional pole for low-frequency cutoff
C4	Microphone power supply decoupling	Reduces power supply noise
C6, C7, C8	Power supply capacitors	Filter and bypass of power supply

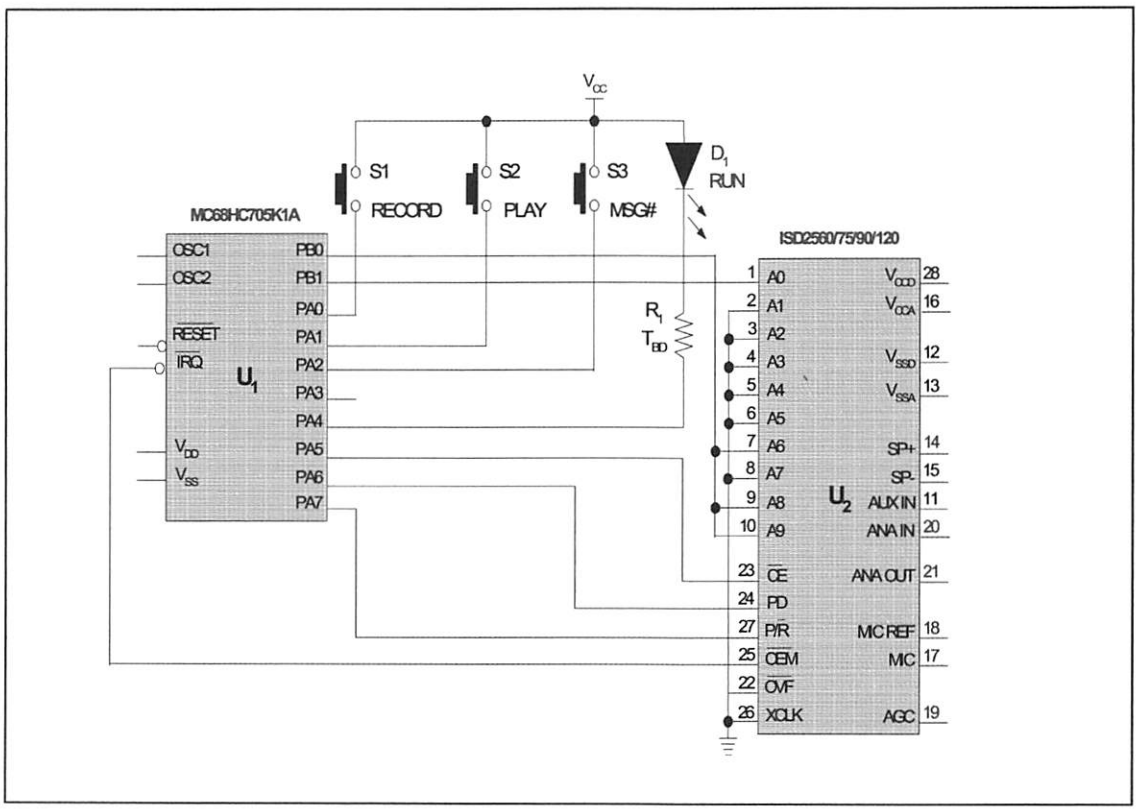


FIGURE 6: ISD2560/75/90/120 APPLICATION EXAMPLE – MICROCONTROLLER/ISD2500 INTERFACE

In this simplified block diagram of a microcontroller application, the Push-Button Mode and message cueing are used. The microcontroller is a 16-pin version with enough port pins for buttons, an LED, and the ISD2500 series device. The software can be written to use three buttons: one each for play and record, and one for message selection. Because the microcontroller is interpreting the buttons and commanding the ISD2500 device, software can be written for any function desired in a particular application.

Note: Winbond does not recommend connecting address lines directly to a microprocessor bus. Address lines should be externally latched.

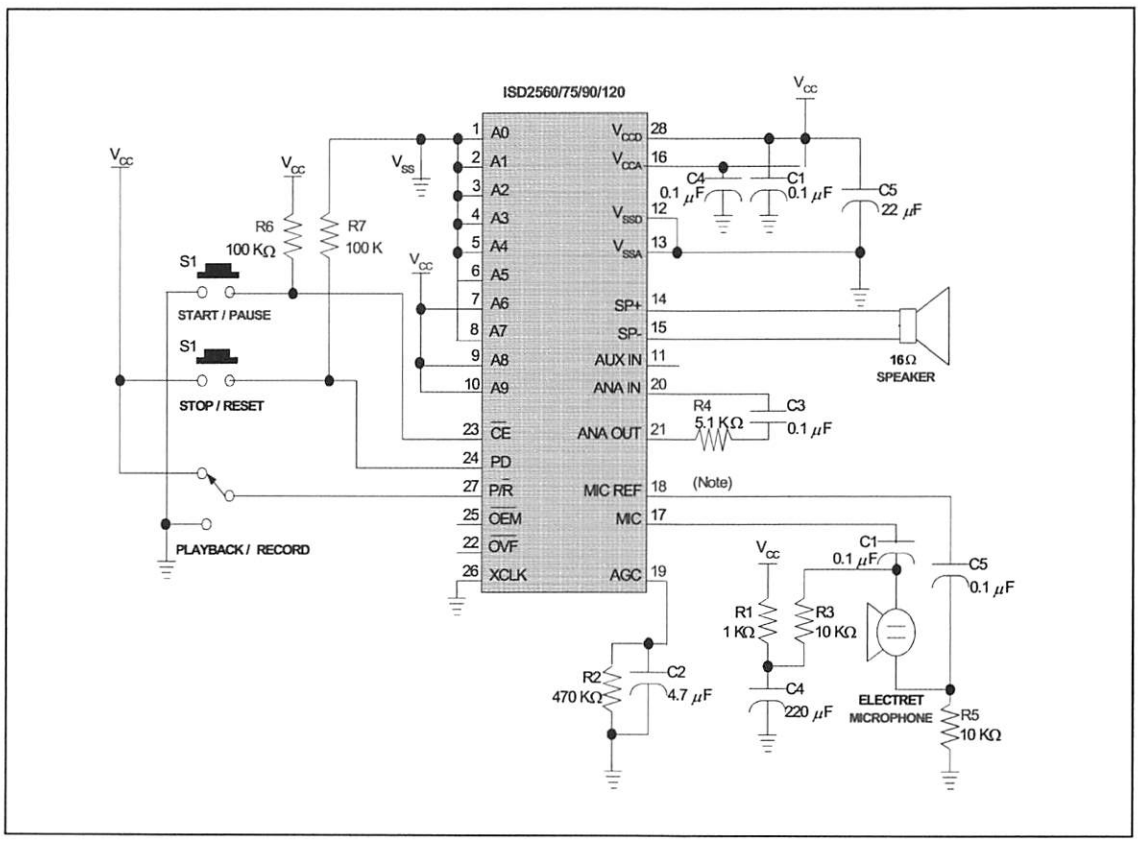


FIGURE 7: ISD2560/75/90/120 APPLICATION EXAMPLE – PUSH-BUTTON

Note: Please refer to page 13 for more details.

TABLE 15: APPLICATION EXAMPLE – PUSH-BUTTON CONTROL

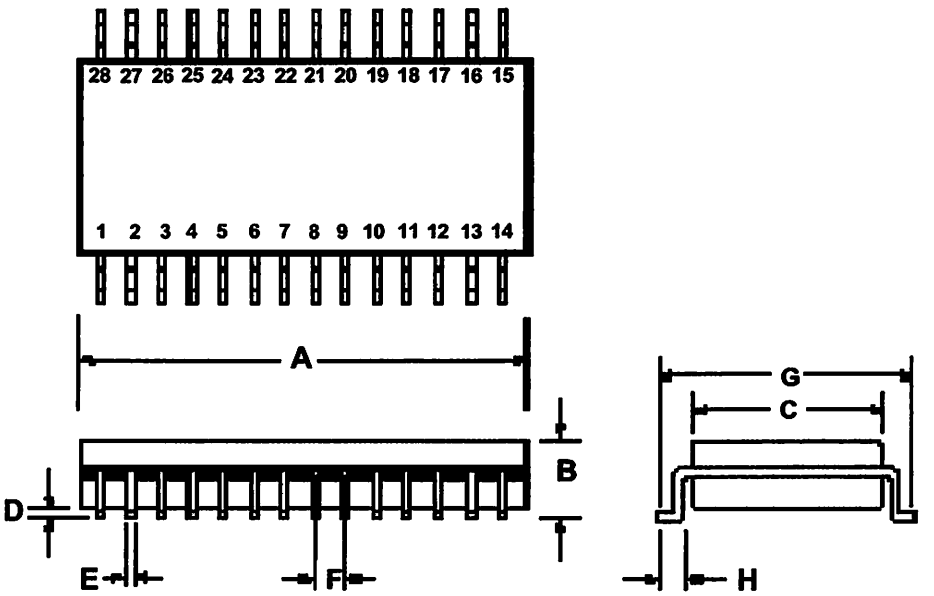
Control Step	Function	Action
1	Select Record/Playback Mode	$P/\overline{R}$ = As desired
2A	Begin playback	$P/\overline{R}$ = HIGH, $\overline{CE}$ = Pulse LOW
2B	Begin record	$P/\overline{R}$ = LOW, $\overline{CE}$ = Pulse LOW
3	Pause record or playback	$\overline{CE}$ = Pulsed LOW
4A	End playback	Automatic at $\overline{EOM}$ marker or PD = Pulsed HIGH
4B	End record	PD = Pulsed HIGH

TABLE 16: APPLICATION EXAMPLE – PASSIVE COMPONENT FUNCTIONS

Part	Function	Comments
R2	Release time constant	Sets release time for AGC
R4	Series limiting resistor	Reduces level to prevent distortion at higher supply voltages
R6, R7	Pull-up and pull-down resistors	Defines static state of inputs
C1, C4, C5	Power supply capacitors	Filters and bypass of power supply
C2	Attack/Release time constant	Sets attack/release time for AGC
C3	Low-frequency cutoff capacitor	Provides additional pole for low-frequency cutoff

12. PACKAGE DRAWING AND DIMENSIONS

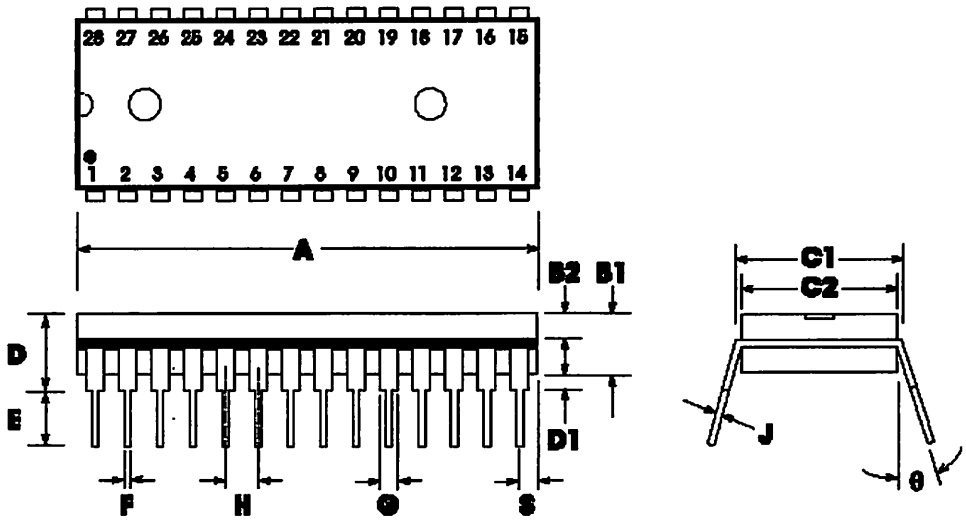
12.1. 28-LEAD 300-MIL PLASTIC SMALL OUTLINE IC (SOIC)



	INCHES			MILLIMETERS		
	Min	Nom	Max	Min	Nom	Max
A	0.701	0.706	0.711	17.81	17.93	18.06
B	0.097	0.101	0.104	2.46	2.56	2.64
C	0.292	0.296	0.299	7.42	7.52	7.59
D	0.005	0.009	0.0115	0.127	0.22	0.29
E	0.014	0.016	0.019	0.35	0.41	0.48
F		0.050			1.27	
G	0.400	0.406	0.410	10.16	10.31	10.41
H	0.024	0.032	0.040	0.61	0.81	1.02

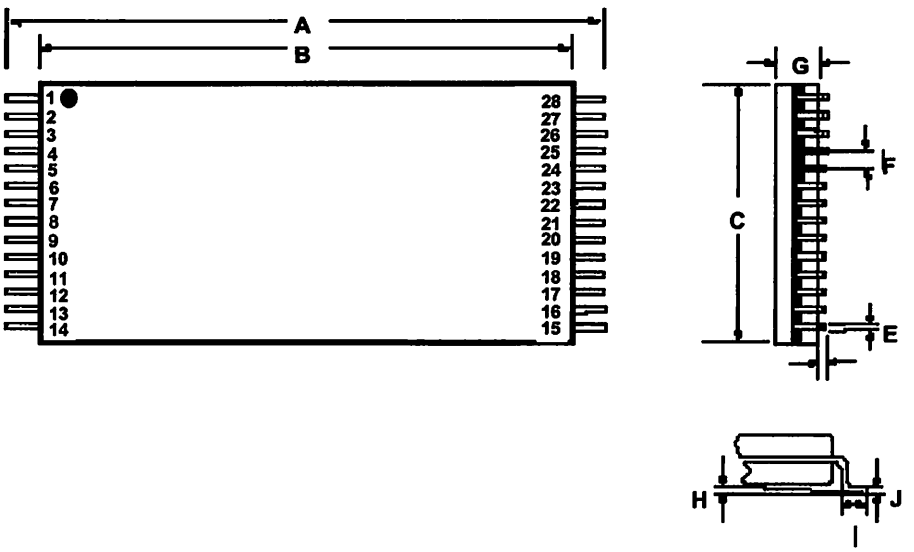
Note: Lead coplanarity to be within 0.004 inches.

12.2. 28-LEAD 600-MIL PLASTIC DUAL INLINE PACKAGE (PDIP)



	INCHES			MILLIMETERS		
	Min	Nom	Max	Min	Nom	Max
A	1.445	1.450	1.455	36.70	36.83	36.96
B1		0.150			3.81	
B2	0.065	0.070	0.075	1.65	1.78	1.91
C1	0.600		0.625	15.24		15.88
C2	0.530	0.540	0.550	13.46	13.72	13.97
D			0.19			4.83
D1	0.015			0.38		
E	0.125		0.135	3.18		3.43
F	0.015	0.018	0.022	0.38	0.46	0.56
G	0.055	0.060	0.065	1.40	1.52	1.62
H		0.100			2.54	
J	0.008	0.010	0.012	0.20	0.25	0.30
S	0.070	0.075	0.080	1.78	1.91	2.03
q	0°		15°	0°		15°

12.3. 28-LEAD 8X13.4MM PLASTIC THIN SMALL OUTLINE PACKAGE (TSOP) TYPE 1



Plastic Thin Small Outline Package (TSOP) Type 1 Dimensions

	INCHES			MILLIMETERS		
	Min	Nom	Max	Min	Nom	Max
A	0.520	0.528	0.535	13.20	13.40	13.60
B	0.461	0.465	0.469	11.70	11.80	11.90
C	0.311	0.315	0.319	7.90	8.00	8.10
D	0.002		0.006	0.05		0.15
E	0.007	0.009	0.011	0.17	0.22	0.27
F		0.0217			0.55	
G	0.037	0.039	0.041	0.95	1.00	1.05
H	0^0	3^0	6^0	0^0	3^0	6^0
I	0.020	0.022	0.028	0.50	0.55	0.70
J	0.004		0.008	0.10		0.21

Note: *Lead coplanarity to be within 0.004 inches.*

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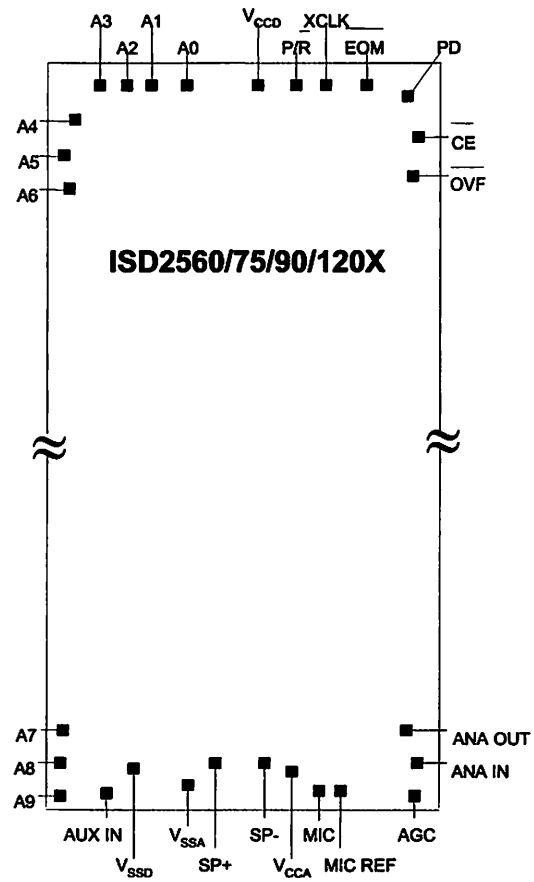
12.4. ISD2560/75/95/120 PRODUCT BONDING PHYSICAL LAYOUT (DIE) [1]

ISD2560/75/95/120

- Die Dimensions
  X: 149.5 ± 1 mils
  Y: 262.0 ± 1 mils
- Die Thickness [2]
  11.8 ± .4 mils
- Pad Opening
  111 x 111 microns
  4.4 x 4.4 mils



Notes:

[1] The backside of die is internally connected to V_{SS}. It **MUST NOT** be connected to any other potential or damage may occur.

[2] Die thickness is subject to change, please contact Winbond factory for status and availability.

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ISD2560/75/90/120 PRODUCT PAD DESIGNATIONS

(with respect to die center)

Pad	Pad Name	X Axis (µm)	Y Axis (µm)
A0	Address 0	-897.9	3135.2
A1	Address 1	-1115.4	3135.2
A2	Address 2	-1331.0	3135.2
A3	Address 3	-1544.0	3135.2
A4	Address 4	-1640.4	2888.9
A5	Address 5	-1698.2	2671.0
A6	Address 6	-1698.2	2441.5
A7	Address 7	-1731.2	-2583.2
A8	Address 8	-1731.2	-2768.4
A9	Address 9	-1731.2	-3050.8
AUX IN	Auxiliary Input	-1410.2	-3115.7
V_{SSD}	V_{SS} Digital Power Supply	-1112.4	-3096.5
V_{SSA}	V_{SS} Analog Power Supply	-408.2	-3138.9
SP+	Speaker Output +	-46.65	-3068.4
SP-	Speaker Output -	386.1	-3068.4
V_{CCA}	V_{CC} Analog Power Supply	746.9	-3110.8
MIC	Microphone Input	1101.2	-3146.0
MIC REF	Microphone Reference	1294.7	-3146.0
AGC	Automatic Gain Control	1666.4	-3130.3
ANA IN	Analog Input	1728.6	-2654.0
ANA OUT	Analog Output	1700.9	-2411.0
$\overline{OVF}$	Overflow Output	1674.6	2489.5
$\overline{CE}$	Chip Enable Input	1726.7	2824.4
PD	Power Down Input	1730.5	3094.0
$\overline{EOM}$	End of Message	1341.2	3122.1
XCLK	No Connect (optional)	986.5	3160.7
P/$\overline{R}$	Playback/Record	807.2	3163.4
V_{CCD}	V_{CC} Digital Power Supply	544.4	3159.6

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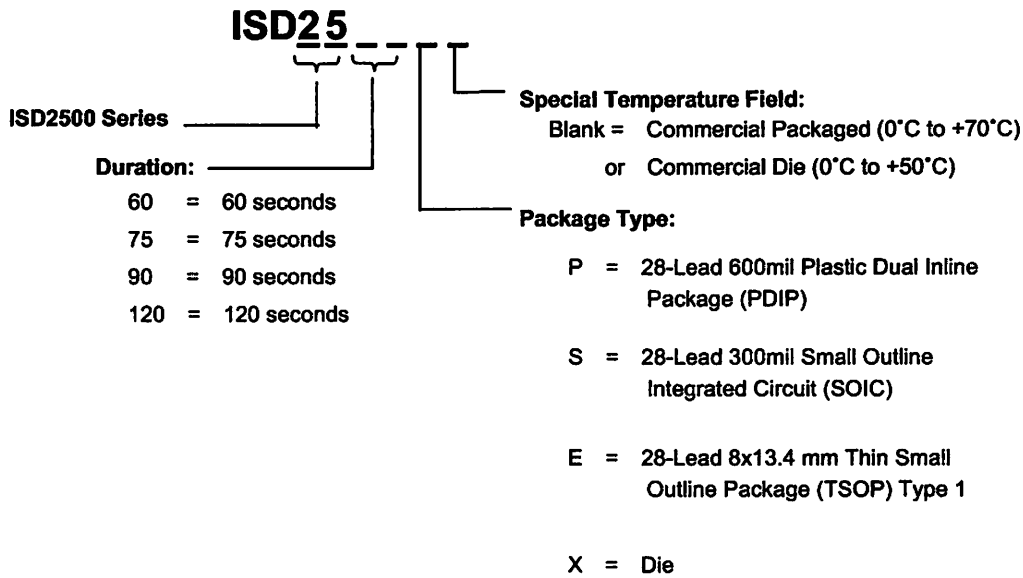
13. ORDERING INFORMATION

Product Number Descriptor Key



When ordering ISD2560/75/90/120 products refer to the following part numbers which are supported in volume for this product series. Consult the local Winbond Sales Representative or Distributor for availability information.

Part Number	Part Number	Part Number	Part Number
ISD2560P	ISD2575P	ISD2590P	ISD25120P
ISD2560S	ISD2575S	ISD2590S	ISD25120S
ISD2560E	ISD2575E	ISD2590E	
ISD2560X	ISD2575X	ISD2590X	ISD25120X

For the latest product information, access Winbond's worldwide website at http://www.winbond-usa.com

14. VERSION HISTORY

VERSION	DATE	PAGE	DESCRIPTION
0	Apr. 1998	All	Preliminary Specifications
1.0	May 2003	All	Re-format the document. Update TSOP pin configuration. Revise Overflow pad designation.

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FAX: 852-27552064

ZARLINK SEMICONDUCTOR

MT8870D/MT8870D-1
ISO²-CMOS Integrated DTMF Receiver

Data Sheet

October 2006

eatures

- Complete DTMF Receiver
- Low power consumption
- Internal gain setting amplifier
- Adjustable guard time
- Central office quality
- Power-down mode
- Inhibit mode
- Backward compatible with MT8870C/MT8870C-1

pplications

- Receiver system for British Telecom (BT) or CEPT Spec (MT8870D-1)
- Paging systems
- Repeater systems/mobile radio
- Credit card systems
- Remote control
- Personal computers
- Telephone answering machine

Ordering Information

MT8870DE	18 Pin PDIP	Tubes
MT8870DS	18 Pin SOIC	Tubes
MT8870DN	20 Pin SSOP	Tubes
MT8870DSR	18 Pin SOIC	Tape & Reel
MT8870DNR	20 Pin SSOP	Tape & Reel
MT8870DN1	20 Pin SSOP*	Tubes
MT8870DE1	18 Pin PDIP*	Tubes
MT8870DS1	18 Pin SOIC*	Tubes
MT8870DNR1	20 Pin SSOP*	Tape & Reel
MT8870DSR1	18 Pin SOIC*	Tape & Reel
MT8870DE1-1	18 Pin PDIP*	Tubes
MT8870DS1-1	18 Pin SOIC*	Tubes
MT8870DSR1-1	18 Pin SOIC*	Tape & Reel

*Pb Free Matte Tin

-40°C to +85°C

Description

The MT8870D/MT8870D-1 is a complete DTMF receiver integrating both the bandsplit filter and digital decoder functions. The filter section uses switched capacitor techniques for high and low group filters; the decoder uses digital counting techniques to detect and decode all 16 DTMF tone-pairs into a 4-bit code.

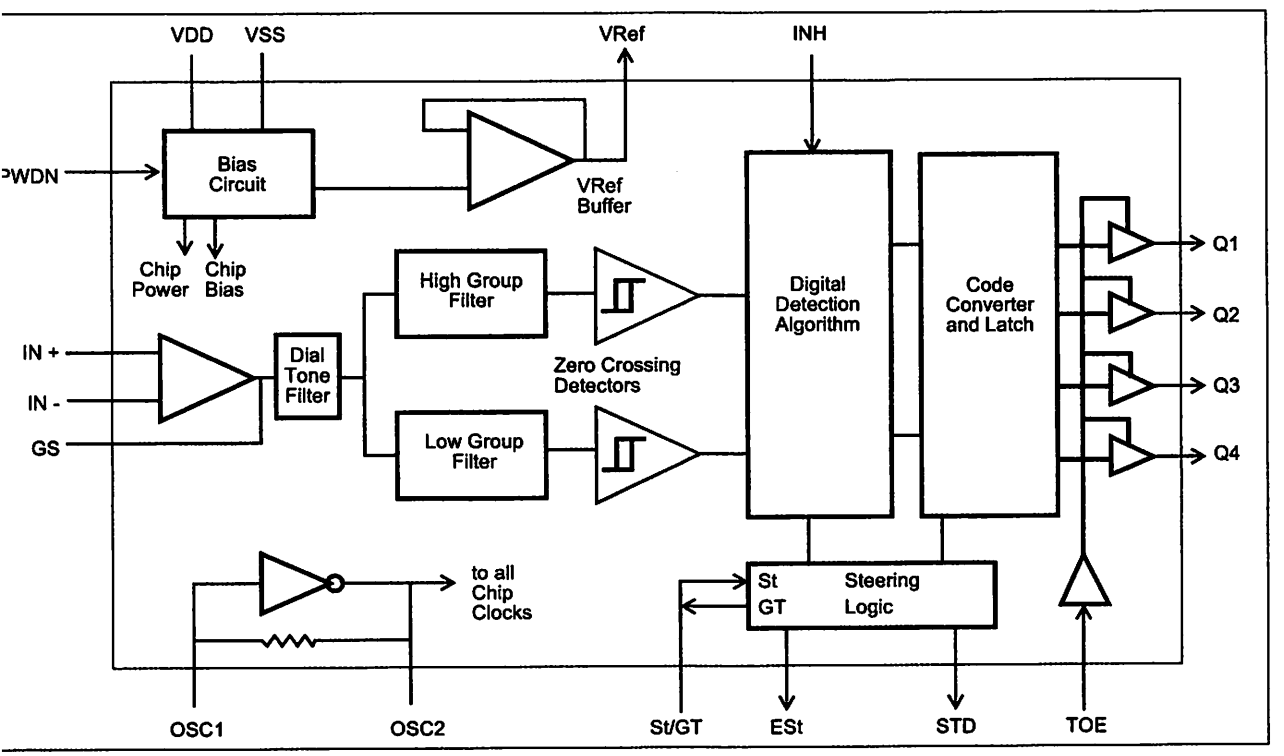


Figure 1 - Functional Block Diagram

xternal component count is minimized by on chip provision of a differential input amplifier, clock oscillator and tched three-state bus interface.

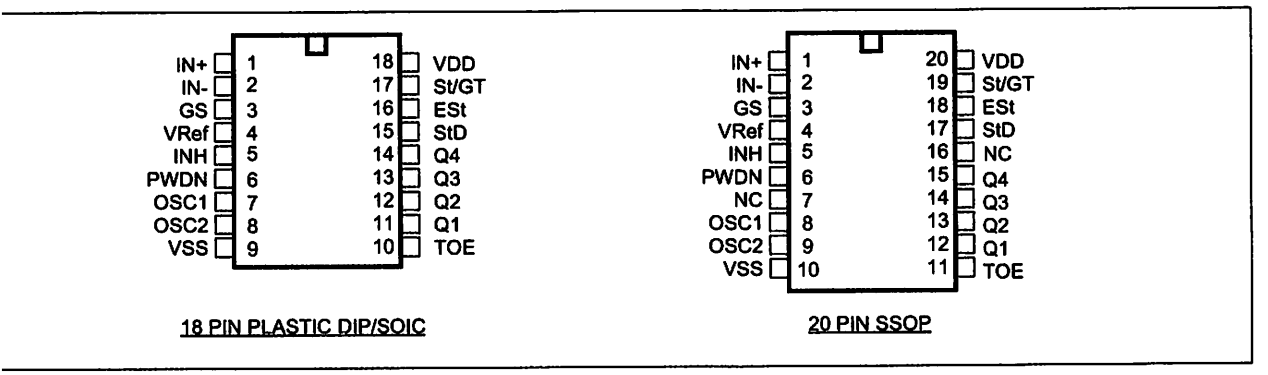


Figure 2 - Pin Connections

in Description

Pin #		Name	Description
18	20		
1	1	IN+	**Non-Inverting Op-Amp (Input).**
2	2	IN-	**Inverting Op-Amp (Input).**
3	3	GS	**Gain Select.** Gives access to output of front end differential amplifier for connection of feedback resistor.
4	4	V_{Ref}	**Reference Voltage (Output).** Nominally $V_{DD}/2$ is used to bias inputs at mid-rail (see Fig. 6 and Fig. 10).
5	5	INH	**Inhibit (Input).** Logic high inhibits the detection of tones representing characters A, B, C and D. This pin input is internally pulled down.
6	6	PWDN	**Power Down (Input).** Active high. Powers down the device and inhibits the oscillator. This pin input is internally pulled down.
7	8	OSC1	**Clock (Input).**
8	9	OSC2	**Clock (Output).** A 3.579545 MHz crystal connected between pins OSC1 and OSC2 completes the internal oscillator circuit.
9	10	V_{SS}	**Ground (Input).** 0 V typical.
10	11	TOE	**Three State Output Enable (Input).** Logic high enables the outputs Q1-Q4. This pin is pulled up internally.
11-14	12-15	Q1-Q4	**Three State Data (Output).** When enabled by TOE, provide the code corresponding to the last valid tone-pair received (see Table 1). When TOE is logic low, the data outputs are high impedance.
15	17	StD	**Delayed Steering (Output).**Presents a logic high when a received tone-pair has been registered and the output latch updated; returns to logic low when the voltage on St/GT falls below V_{TSt}.
16	18	ESt	**Early Steering (Output).** Presents a logic high once the digital algorithm has detected a valid tone pair (signal condition). Any momentary loss of signal condition will cause ESt to return to a logic low.

in Description

Pin #		Name	Description
18	20		
17	19	St/GT	**Steering Input/Guard time (Output) Bidirectional.** A voltage greater than V_{TSt} detected at St causes the device to register the detected tone pair and update the output latch. A voltage less than V_{TSt} frees the device to accept a new tone pair. The GT output acts to reset the external steering time-constant; its state is a function of ESt and the voltage on St.
18	20	V_{DD}	**Positive power supply (Input).** +5 V typical.
	7, 16	NC	No Connection.

unctional Description

he MT8870D/MT8870D-1 monolithic DTMF receiver offers small size, low power consumption and high erformance. Its architecture consists of a bandsplit filter section, which separates the high and low group tones, llowed by a digital counting section which verifies the frequency and duration of the received tones before passing ie corresponding code to the output bus.

ilter Section

eparation of the low-group and high group tones is achieved by applying the DTMF signal to the inputs of two xth-order switched capacitor bandpass filters, the bandwidths of which correspond to the low and high group equencies. The filter section also incorporates notches at 350 and 440 Hz for exceptional dial tone rejection (see igure 3). Each filter output is followed by a single order switched capacitor filter section which smooths the signals rior to limiting. Limiting is performed by high-gain comparators which are provided with hysteresis to prevent etection of unwanted low-level signals. The outputs of the comparators provide full rail logic swings at the equencies of the incoming DTMF signals.

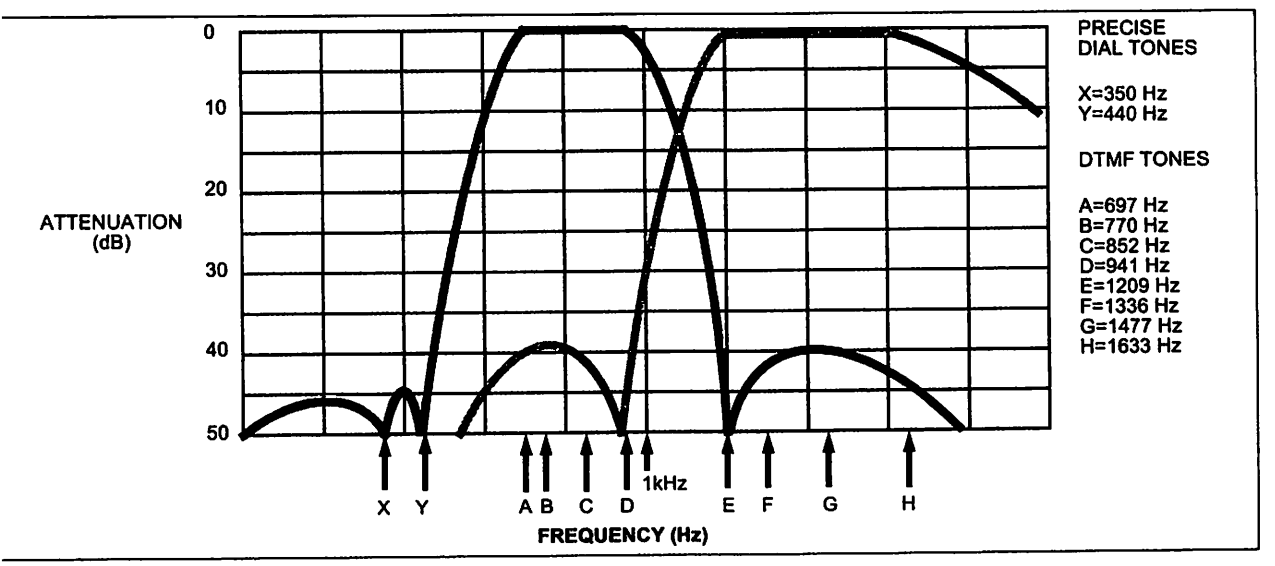


Figure 3 - Filter Response

ecoder Section

ollowing the filter section is a decoder employing digital counting techniques to determine the frequencies of the ıcoming tones and to verify that they correspond to standard DTMF frequencies. A complex averaging algorithm rotects against tone simulation by extraneous signals such as voice while providing tolerance to small frequency eviations and variations. This averaging algorithm has been developed to ensure an optimum combination of ınmunity to talk-off and tolerance to the presence of interfering frequencies (third tones) and noise. When the etector recognizes the presence of two valid tones (this is referred to as the "signal condition" in some industry pecifications) the "Early Steering" (ESt) output will go to an active state. Any subsequent loss of signal condition ill cause ESt to assume an inactive state (see "Steering Circuit").

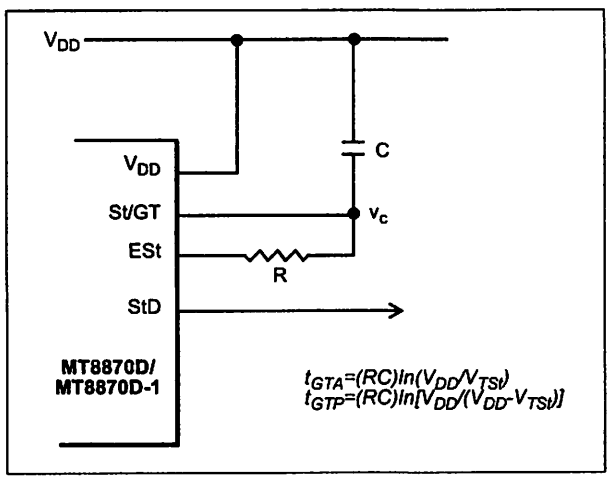


Figure 4 - Basic Steering Circuit

teering Circuit

efore registration of a decoded tone pair, the receiver checks for a valid signal duration (referred to as character ecognition condition). This check is performed by an external RC time constant driven by ESt. A logic high on ESt auses v_c (see Figure 4) to rise as the capacitor discharges. Provided signal condition is maintained (ESt remains igh) for the validation period (t_{GTP}), v_c reaches the threshold (V_{TSt}) of the steering logic to register the tone pair, itching its corresponding 4-bit code (see Table 1) into the output latch. At this point the GT output is activated and rives v_c to V_{DD}. GT continues to drive high as long as ESt remains high. Finally, after a short delay to allow the utput latch to settle, the delayed steering output flag (StD) goes high, signalling that a received tone pair has been egistered. The contents of the output latch are made available on the 4-bit output bus by raising the three state ontrol input (TOE) to a logic high. The steering circuit works in reverse to validate the interdigit pause between ignals. Thus, as well as rejecting signals too short to be considered valid, the receiver will tolerate signal nterruptions (dropout) too short to be considered a valid pause. This facility, together with the capability of selecting ıe steering time constants externally, allows the designer to tailor performance to meet a wide variety of system equirements.

uard Time Adjustment

ı many situations not requiring selection of tone duration and interdigital pause, the simple steering circuit shown ı Figure 4 is applicable. Component values are chosen according to the formula:

$$t_{REC}=t_{DP}+t_{GTP}$$
$$t_{ID}=t_{DA}+t_{GTA}$$

ıe value of t_{DP} is a device parameter (see Figure 11) and t_{REC} is the minimum signal duration to be recognized by e receiver. A value for C of 0.1 µF is recommended for most applications, leaving R to be selected by the ɜsigner.

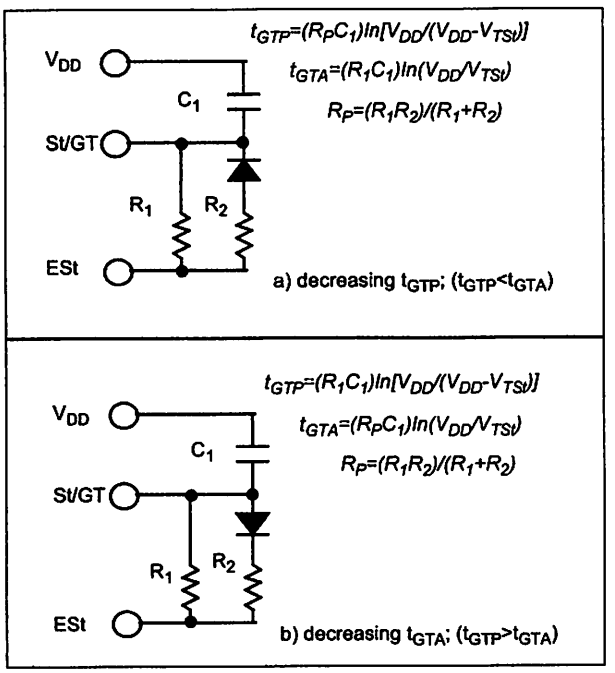


Figure 5 - Guard Time Adjustment

Digit	TOE	INH	ESt	Q_4	Q_3	Q_2	Q_1
ANY	L	X	H	Z	Z	Z	Z
1	H	X	H	0	0	0	1
2	H	X	H	0	0	1	0
3	H	X	H	0	0	1	1
4	H	X	H	0	1	0	0
5	H	X	H	0	1	0	1
6	H	X	H	0	1	1	0
7	H	X	H	0	1	1	1
8	H	X	H	1	0	0	0
9	H	X	H	1	0	0	1
0	H	X	H	1	0	1	0
*	H	X	H	1	0	1	1
#	H	X	H	1	1	0	0
A	H	L	H	1	1	0	1
B	H	L	H	1	1	1	0
C	H	L	H	1	1	1	1
D	H	L	H	0	0	0	0
A	H	H	L	undetected, the output code will remain the same as the previous detected code .			
B	H	H	L				
C	H	H	L				
D	H	H	L				

Table 1 - Functional Decode Table

L=LOGIC LOW, H=LOGIC HIGH, Z=HIGH IMPEDANCE
X = DON'T CARE

ifferent steering arrangements may be used to select independently the guard times for tone present (t_{GTP}) and ıne absent (t_{GTA}). This may be necessary to meet system specifications which place both accept and reject limits n both tone duration and interdigital pause. Guard time adjustment also allows the designer to tailor system ɜrameters such as talk off and noise immunity. Increasing t_{REC} improves talk-off performance since it reduces the robability that tones simulated by speech will maintain signal condition long enough to be registered. Alternatively, relatively short t_{REC} with a long t_{DO} would be appropriate for extremely noisy environments where fast acquisition ne and immunity to tone drop-outs are required. Design information for guard time adjustment is shown in Figure

ower-down and Inhibit Mode

logic high applied to pin 6 (PWDN) will power down the device to minimize the power consumption in a standby ıode. It stops the oscillator and the functions of the filters.

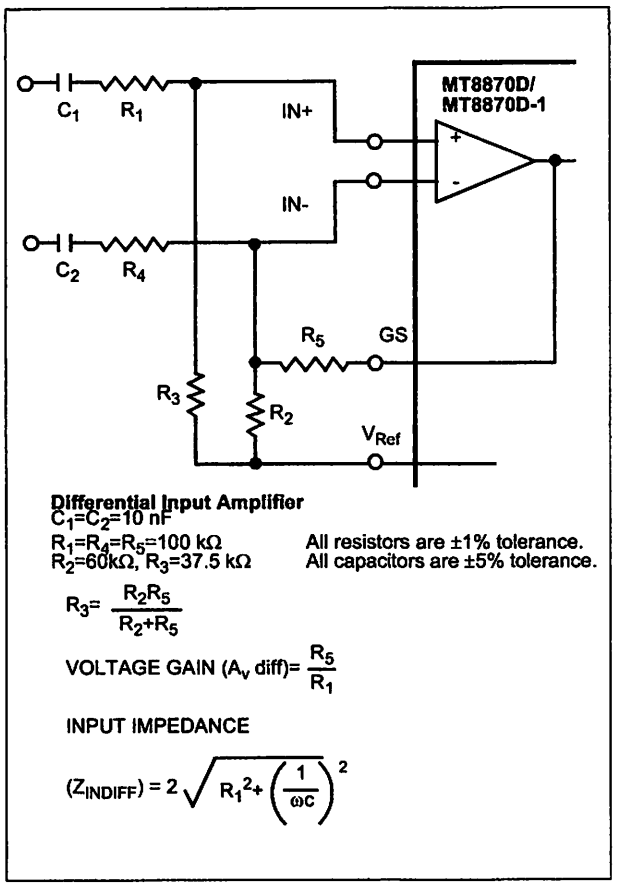
ıhibit mode is enabled by a logic high input to the pin 5 (INH). It inhibits the detection of tones representing ıaracters A, B, C, and D. The output code will remain the same as the previous detected code (see Table 1).

ifferential Input Configuration

he input arrangement of the MT8870D/MT8870D-1 provides a differential-input operational amplifier as well as a ias source (V_{Ref}) which is used to bias the inputs at mid-rail. Provision is made for connection of a feedback ɜsistor to the op-amp output (GS) for adjustment of gain. In a single-ended configuration, the input pins are ɔnnected as shown in Figure 10 with the op-amp connected for unity gain and V_{Ref} biasing the input at $^1/_2V_{DD}$. igure 6 shows the differential configuration, which permits the adjustment of gain with the feedback resistor R_5.

rystal Oscillator

he internal clock circuit is completed with the addition of an external 3.579545 MHz crystal and is normally ɔnnected as shown in Figure 10 (Single-Ended Input Configuration). However, it is possible to configure several IT8870D/MT8870D-1 devices employing only a single oscillator crystal. The oscillator output of the first device in ıe chain is coupled through a 30 pF capacitor to the oscillator input (OSC1) of the next device. Subsequent evices are connected in a similar fashion. Refer to Figure 7 for details. The problems associated with unbalanced ıading are not a concern with the arrangement shown, i.e., precision balancing capacitors are not required.



Differential Input Amplifier
$C_1=C_2=10$ nF
$R_1=R_4=R_5=100$ kΩ
$R_2=60$kΩ, $R_3=37.5$ kΩ

All resistors are ±1% tolerance.
All capacitors are ±5% tolerance.

$$R_3=\frac{R_2R_5}{R_2+R_5}$$

VOLTAGE GAIN (A_v diff)= $\frac{R_5}{R_1}$

INPUT IMPEDANCE

$$(Z_{INDIFF}) = 2\sqrt{R_1^2+\left(\frac{1}{\omega C}\right)^2}$$

Figure 6 - Differential Input Configuration

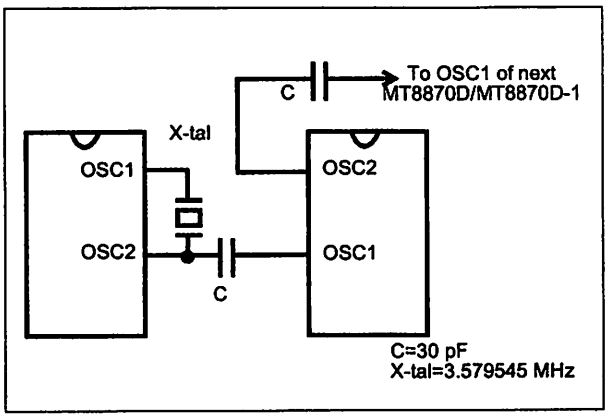


Figure 7 - Oscillator Connection

Parameter	Unit	Resonator
R1	Ohms	10.752
L1	mH	.432
C1	pF	4.984
C0	pF	37.915
Qm	-	896.37
Δf	%	±0.2%

Table 2 - Recommended Resonator Specifications

Note: Qm=quality factor of RLC model, i.e., 1/2ΠfR1C1.

ıpplications

:eceiver System for British Telecom Spec POR 1151

he circuit shown in Fig. 9 illustrates the use of MT8870D-1 device in a typical receiver system. BT Spec defines ıe input signals less than -34 dBm as the non-operate level. This condition can be attained by choosing a suitable alues of R_1 and R_2 to provide 3 dB attenuation, such that -34 dBm input signal will correspond to -37 dBm at the ain setting pin GS of MT8870D-1. As shown in the diagram, the component values of R_3 and C_2 are the guard me requirements when the total component tolerance is 6%. For better performance, it is recommended to use the on-symmetric guard time circuit in Fig. 8.

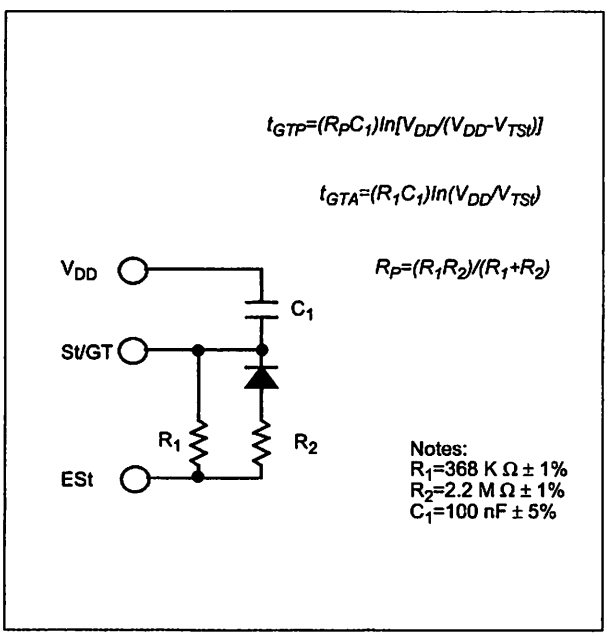
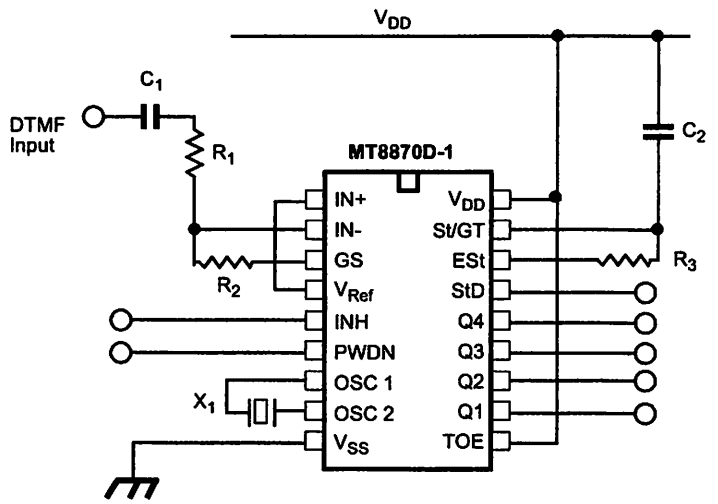


Figure 8 - Non-Symmetric Guard Time Circuit



NOTES:
R_1 = 102 KΩ ± 1%
R_2 = 71.5 KΩ ± 1%
R_3 = 390 KΩ ±1%
C_1,C_2 = 100 nF ± 5%
X_1 = 3.579545 MHz ± 0.1%
V_{DD} = 5.0 V ± 5%

Figure 9 - Single-Ended Input Configuration for BT or CEPT Spec

Absolute Maximum Ratings†

	Parameter	Symbol	Min.	Max.	Units
1	DC Power Supply Voltage	V_{DD}		7	V
2	Voltage on any pin	V_I	V_{SS}-0.3	V_{DD}+0.3	V
3	Current at any pin (other than supply)	I_I		10	mA
4	Storage temperature	T_{STG}	-65	+150	°C
5	Package power dissipation	P_D		500	mW

† Exceeding these values may cause permanent damage. Functional operation under these conditions is not implied.
erate above 75°C at 16 mW / °C. All leads soldered to board.

Recommended Operating Conditions - Voltages are with respect to ground (V_{SS}) unless otherwise stated.

	Parameter	Sym.	Min.	Typ.‡	Max.	Units	Test Conditions
1	DC Power Supply Voltage	V_{DD}	4.75	5.0	5.25	V	
2	Operating Temperature	T_O	-40		+85	°C	
3	Crystal/Clock Frequency	fc		3.579545		MHz	
4	Crystal/Clock Freq.Tolerance	Δfc		±0.1		%	

Typical figures are at 25°C and are for design aid only: not guaranteed and not subject to production testing.

IC Electrical Characteristics - V_{DD}=5.0V± 5%, V_{SS}=0V, -40°C ≤ T_O ≤ +85°C, unless otherwise stated.

		Characteristics	Sym.	Min.	Typ.‡	Max.	Units	Test Conditions
1	SUPPLY	Standby supply current	I_{DDQ}		10	25	µA	PWDN=V_{DD}
2		Operating supply current	I_{DD}		3.0	9.0	mA	
3		Power consumption	P_O		15		mW	fc=3.579545 MHz
4	INPUTS	High level input	V_{IH}	3.5			V	V_{DD}=5.0 V
5		Low level input voltage	V_{IL}			1.5	V	V_{DD}=5.0 V
6		Input leakage current	I_{IH}/I_{IL}		0.1		µA	V_{IN}=V_{SS} or V_{DD}
7		Pull up (source) current	I_{SO}		7.5	20	µA	TOE (pin 10)=0, V_{DD}=5.0 V
8		Pull down (sink) current	I_{SI}		15	45	µA	INH=5.0 V, PWDN=5.0 V, V_{DD}=5.0 V
9		Input impedance (IN+, IN-)	R_{IN}		10		MΩ	@ 1 kHz
10		Steering threshold voltage	V_{TSt}	2.2	2.4	2.5	V	V_{DD} = 5.0 V

)C Electrical Characteristics - V_{DD}=5.0V± 5%, V_{SS}=0V, -40°C ≤ T_O ≤ +85°C, unless otherwise stated.

		Characteristics	Sym.	Min.	Typ.‡	Max.	Units	Test Conditions
11	OUTPUTS	Low level output voltage	V_{OL}			V_{SS}+0.03	V	No load
12		High level output voltage	V_{OH}	V_{DD}-0.03			V	No load
13		Output low (sink) current	I_{OL}	1.0	2.5		mA	V_{OUT}=0.4 V
14		Output high (source) current	I_{OH}	0.4	0.8		mA	V_{OUT}=4.6 V
15		V_{Ref} output voltage	V_{Ref}	2.3	2.5	2.7	V	No load, V_{DD} = 5.0V
16		V_{Ref} output resistance	R_{OR}		1		kΩ	

Typical figures are at 25°C and are for design aid only: not guaranteed and not subject to production testing.

)perating Characteristics - V_{DD}=5.0V±5%, V_{SS}=0V, -40°C ≤ T_O ≤ +85°C,unless otherwise stated.
ain Setting Amplifier

	Characteristics	Sym.	Min.	Typ.‡	Max.	Units	Test Conditions
1	Input leakage current	I_{IN}			100	nA	$V_{SS} \le V_{IN} \le V_{DD}$
2	Input resistance	R_{IN}	10			MΩ	
3	Input offset voltage	V_{OS}			25	mV	
4	Power supply rejection	PSRR	50			dB	1 kHz
5	Common mode rejection	CMRR	40			dB	0.75 V ≤ V_{IN} ≤ 4.25 V biased at V_{Ref} =2.5 V
6	DC open loop voltage gain	A_{VOL}	32			dB	
7	Unity gain bandwidth	f_C	0.30			MHz	
8	Output voltage swing	V_O	4.0			V_{pp}	Load ≥ 100 kΩ to V_{SS} @ GS
9	Maximum capacitive load (GS)	C_L			100	pF	
10	Resistive load (GS)	R_L			50	kΩ	
11	Common mode range	V_{CM}	2.5			V_{pp}	No Load

IT8870D AC Electrical Characteristics -V_{DD}=5.0V ±5%, V_{SS}=0V, -40°C ≤ T_O ≤ +85°C, using Test Circuit shown in Figure 10.

	Characteristics	Sym.	Min.	Typ.‡	Max.	Units	Notes*
1	Valid input signal levels (each tone of composite signal)		-29		+1	dBm	1,2,3,5,6,9
			27.5		869	mV_{RMS}	1,2,3,5,6,9
2	Negative twist accept				8	dB	2,3,6,9,12
3	Positive twist accept				8	dB	2,3,6,9,12
4	Frequency deviation accept		±1.5% ± 2 Hz				2,3,5,9
5	Frequency deviation reject		±3.5%				2,3,5,9
6	Third tone tolerance			-16		dB	2,3,4,5,9,10
7	Noise tolerance			-12		dB	2,3,4,5,7,9,10
8	Dial tone tolerance			+22		dB	2,3,4,5,8,9,11

Typical figures are at 25°C and are for design aid only: not guaranteed and not subject to production testing.

NOTES
. dBm= decibels above or below a reference power of 1 mW into a 600 ohm load.
. Digit sequence consists of all DTMF tones.
. Tone duration= 40 ms, tone pause= 40 ms.
. Signal condition consists of nominal DTMF frequencies.
. Both tones in composite signal have an equal amplitude.
. Tone pair is deviated by ±1.5%± 2 Hz.
. Bandwidth limited (3 kHz) Gaussian noise.
. The precise dial tone frequencies are (350 Hz and 440 Hz) ± 2%.
. For an error rate of better than 1 in 10,000.
). Referenced to lowest level frequency component in DTMF signal.
l. Referenced to the minimum valid accept level.
?. Guaranteed by design and characterization.

MT8870D-1 AC Electrical Characteristics -V_{DD}=5.0V±5%, V_{SS}=0V, -40°C ≤ T_O ≤ +85°C, using Test Circuit shown in Figure 10.

	Characteristics	Sym.	Min.	Typ.‡	Max.	Units	Notes*
1	Valid input signal levels (each tone of composite signal)		-31		+1	dBm	Tested at V_{DD}=5.0 V 1,2,3,5,6,9
			21.8		869	mV_{RMS}	
2	Input Signal Level Reject		-37			dBm	Tested at V_{DD}=5.0 V 1,2,3,5,6,9
			10.9			mV_{RMS}	
3	Negative twist accept				8	dB	2,3,6,9,13
4	Positive twist accept				8	dB	2,3,6,9,13
5	Frequency deviation accept		±1.5%± 2 Hz				2,3,5,9
6	Frequency deviation reject		±3.5%				2,3,5,9
7	Third zone tolerance			-18.5		dB	2,3,4,5,9,12
8	Noise tolerance			-12		dB	2,3,4,5,7,9,10
9	Dial tone tolerance			+22		dB	2,3,4,5,8,9,11

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. Tone pair is deviated by ±1.5%± 2 Hz.
. Bandwidth limited (3 kHz) Gaussian noise.
. The precise dial tone frequencies are (350 Hz and 440 Hz) ± 2%.
. For an error rate of better than 1 in 10,000.
). Referenced to lowest level frequency component in DTMF signal.
I. Referenced to the minimum valid accept level.
2. Referenced to Fig. 10 input DTMF tone level at -25dBm (-28dBm at GS Pin) interference frequency range between 480-3400Hz.
3. Guaranteed by design and characterization.

AC Electrical Characteristics - V_{DD}=5.0V±5%, V_{SS}=0V, -40°C ≤ To ≤ +85°C, using Test Circuit shown in Figure 10.

		Characteristics	Sym.	Min.	Typ.‡	Max.	Units	Conditions
1	TIMING	Tone present detect time	t_{DP}	5	11	14	ms	Note 1
2		Tone absent detect time	t_{DA}	0.5	4	8.5	ms	Note 1
3		Tone duration accept	t_{REC}			40	ms	Note 2
4		Tone duration reject	$t_{\overline{REC}}$	20			ms	Note 2
5		Interdigit pause accept	t_{ID}			40	ms	Note 2
6		Interdigit pause reject	t_{DO}	20			ms	Note 2
7	OUTPUTS	Propagation delay (St to Q)	t_{PQ}		8	11	µs	TOE=V_{DD}
8		Propagation delay (St to StD)	t_{PStD}		12	16	µs	TOE=V_{DD}
9		Output data set up (Q to StD)	t_{QStD}		3.4		µs	TOE=V_{DD}
10		Propagation delay (TOE to Q ENABLE)	t_{PTE}		50		ns	load of 10 kΩ, 50 pF
11		Propagation delay (TOE to Q DISABLE)	t_{PTD}		300		ns	load of 10 kΩ, 50 pF
12	PDWN	Power-up time	t_{PU}		30		ms	Note 3
13		Power-down time	t_{PD}		20		ms	
14	CLOCK	Crystal/clock frequency	f_C	3.5759	3.5795	3.5831	MHz	
15		Clock input rise time	t_{LHCL}			110	ns	Ext. clock
16		Clock input fall time	t_{HLCL}			110	ns	Ext. clock
17		Clock input duty cycle	DC_{CL}	40	50	60	%	Ext. clock
18		Capacitive load (OSC2)	C_{LO}			30	pF	

Typical figures are at 25°C and are for design aid only: not guaranteed and not subject to production testing.

NOTES:

1. Used for guard-time calculation purposes only.
2. These, user adjustable parameters, are not device specifications. The adjustable settings of these minimums and maximums are recommendations based upon network requirements.
3. With valid tone present at input, t_{PU} equals time from PDWN going low until ESt going high.

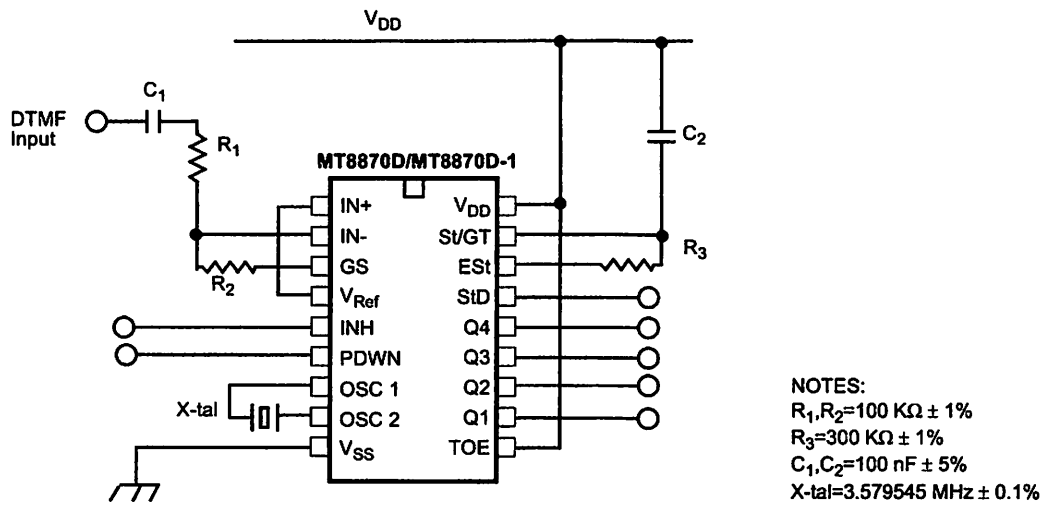
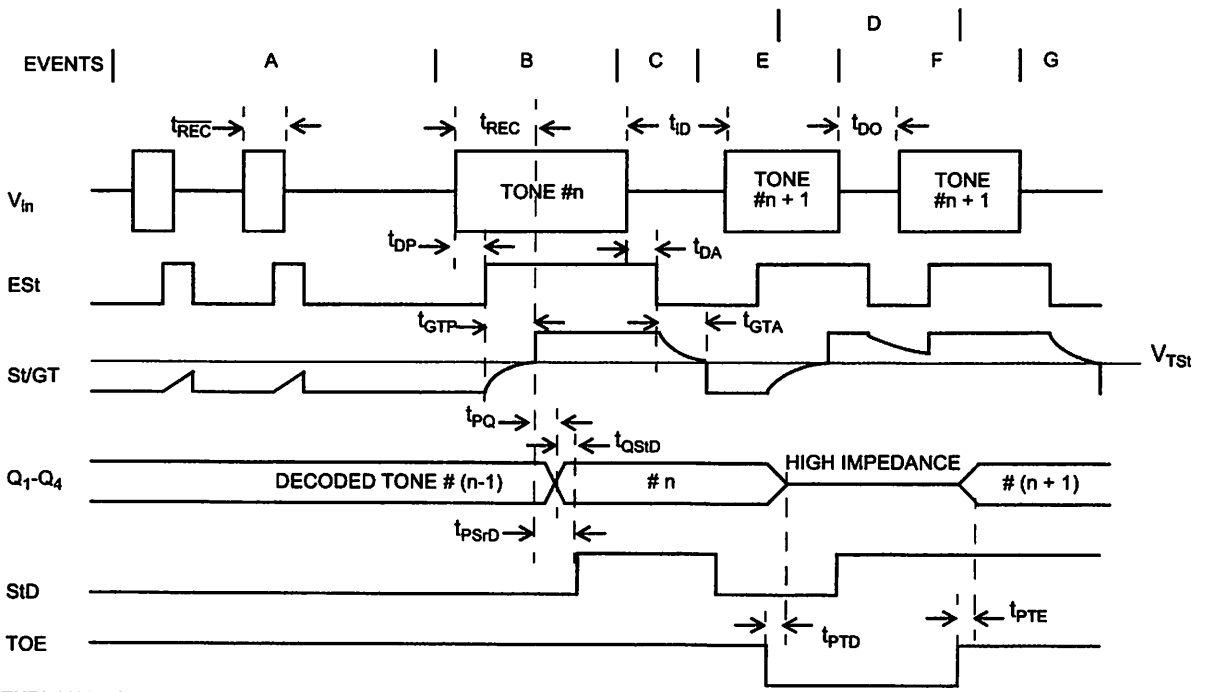


Figure 10 - Single-Ended Input Configuration



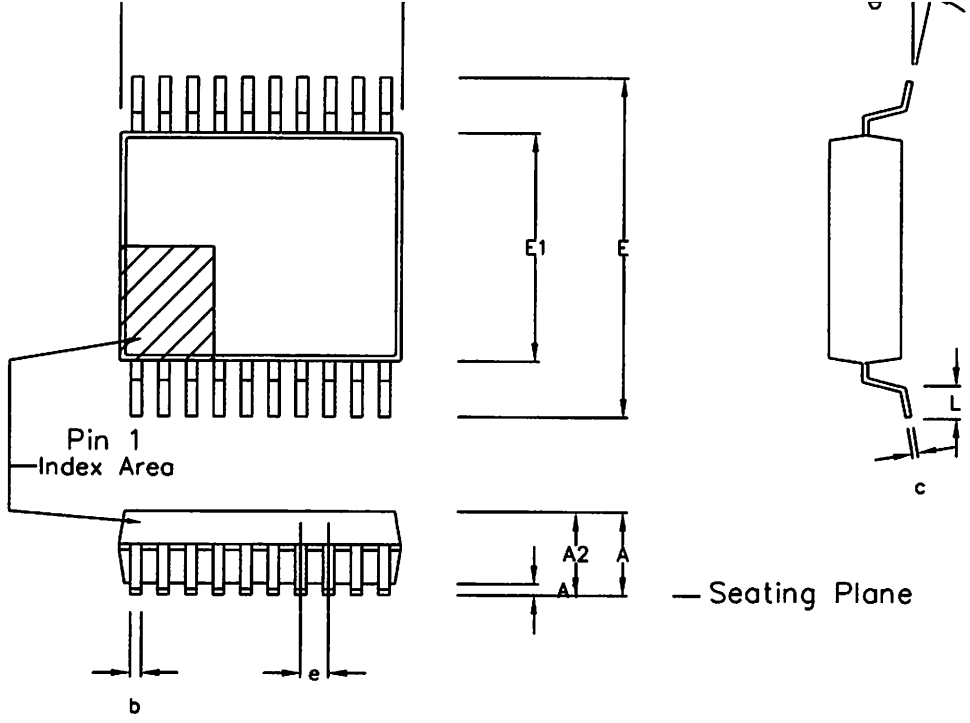
EXPLANATION OF EVENTS

A)	TONE BURSTS DETECTED, TONE DURATION INVALID, OUTPUTS NOT UPDATED.
B)	TONE #n DETECTED, TONE DURATION VALID, TONE DECODED AND LATCHED IN OUTPUTS
C)	END OF TONE #n DETECTED, TONE ABSENT DURATION VALID, OUTPUTS REMIAN LATCHED UNTIL NEXT VALID TONE.
D)	OUTPUTS SWITCHED TO HIGH IMPEDANCE STATE.
E)	TONE #n + 1 DETECTED, TONE DURATION VALID, TONE DECODED AND LATCHED IN OUTPUTS (CURRENTLY HIGH IMPEDANCE).
F)	ACCEPTABLE DROPOUT OF TONE #n + 1, TONE ABSENT DURATION INVALID, OUTPUTS REMAIN LATCHED.
G)	END OF TONE #n + 1 DETECTED, TONE ABSENT DURATION VALID, OUTPUTS REMAIN LATCHED UNTIL NEXT VALID TONE.

EXPLANATION OF SYMBOLS

V_{in}	DTMF COMPOSITE INPUT SIGNAL.
ESt	EARLY STEERING OUTPUT. INDICATES DETECTION OF VALID TONE FREQUENCIES.
St/GT	STEERING INPUT/GUARD TIME OUTPUT. DRIVES EXTERNAL RC TIMING CIRCUIT.
Q_1-Q_4	4-BIT DECODED TONE OUTPUT.
StD	DELAYED STEERING OUTPUT. INDICATES THAT VALID FREQUENCIES HAVE BEEN PRESENT/ABSENT FOR THE REQUIRED GUARD TIME THUS CONSTITUTING A VALID SIGNAL.
TOE	TONE OUTPUT ENABLE (INPUT). A LOW LEVEL SHIFTS Q_1-Q_4 TO ITS HIGH IMPEDANCE STATE.
$t_{\overline{REC}}$	MAXIMUM DTMF SIGNAL DURATION NOT DETECED AS VALID
t_{REC}	MINIMUM DTMF SIGNAL DURATION REQUIRED FOR VALID RECOGNITION
t_{ID}	MAXIMUM TIME BETWEEN VALID DTMF SIGNALS.
t_{DO}	MAXIMUM ALLOWABLE DROP OUT DURING VALID DTMF SIGNAL.
t_{DP}	TIME TO DETECT THE PRESENCE OF VALID DTMF SIGNALS.
t_{DA}	TIME TO DETECT THE ABSENCE OF VALID DTMF SIGNALS.
t_{GTP}	GUARD TIME, TONE PRESENT.
t_{GTA}	GUARD TIME, TONE ABSENT.

Figure 11 - Timing Diagram



Symbol	Control Dimensions in millimetres				Altern. Dimensions in inches		
	MIN	Nominal	MAX		MIN	Nominal	MAX
A	1.70		2.00		0.067		0.079
A1	0.05		0.20		0.002		0.008
A2	1.65		1.85		0.065		0.073
D	6.90		7.50		0.272		0.295
E	7.40		8.20		0.291		0.323
E1	5.00		5.60		0.197		0.220
L	0.55		0.95		0.022		0.037
e	0.65 BSC.				0.026 BSC.		
b	0.22		0.38		0.009		0.015
c	0.09		0.25		0.004		0.010
θ	0°		8°		0°		8°
	Pin features						
N	20						
Conforms to JEDEC MO-150 AE Iss. B							

This drawing supersedes:-
418/ED/51481/002 (Swindon/Plymouth)

Notes:
1. A visual index feature, e.g. a dot, must be located within the cross-hatched area.
2. Controlling dimension are in millimeters.
3. Dimensions D and E1 do not include mould flash or protusion. Mould flash or protusion shall not exceed 0.20 mm per side. D and E1 are maximum plastic body size dimensions including mould mismatch.
4. Dimension b does not include dambar protusion/intrusion. Allowable dambar protusion shall be 0.13 mm total in excess of b dimension. Dambar intrusion shall not reduce dimension b by more than 0.07 mm.

ISSUE	1	2	3	
ACN	201933	205234	212477	
DATE	27Feb97	25Sep98	3Apr02	
APPRD.				

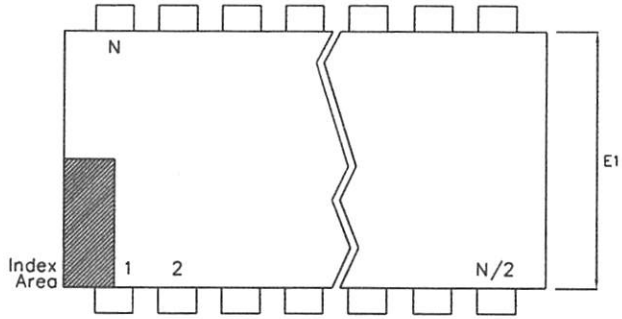
ZARLINK SEMICONDUCTOR

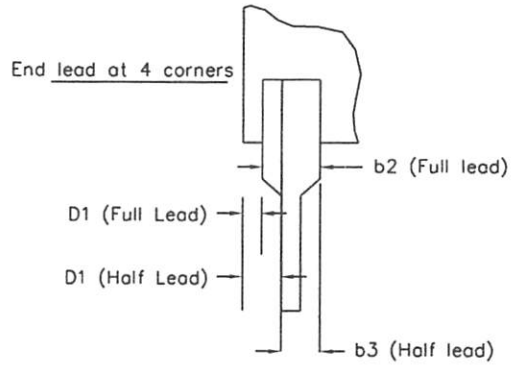
Previous package codes
NP / N

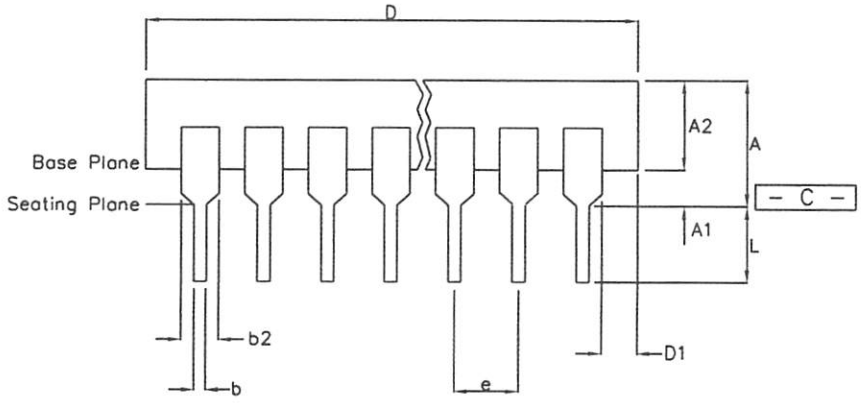
Package Code DD

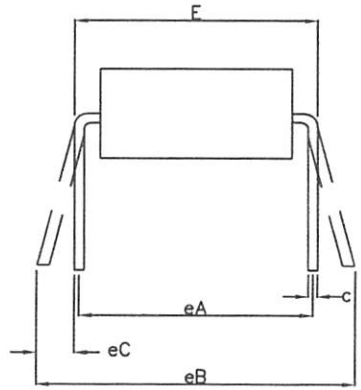
Package Outline for 20 lead SSOP (5.3mm Body Width)

GPD00294









	Min mm	Max mm	Min Inches	Max Inches
A		5.33		0.210
A1	0.38		0.015	
A2	2.92	4.95	0.115	0.195
b	0.36	0.56	0.014	0.022
b2	1.14	1.78	0.045	0.070
b3	n/a	n/a	n/a	n/a
c	0.20	0.36	0.008	0.014
D	22.35	23.37	0.880	0.920
D1	0.13		0.005	
E	7.62	8.26	0.300	0.325
E1	6.10	7.11	0.240	0.280
e	2.54 BSC		0.100 BSC	
eA	7.62 BSC		0.300 BSC	
eB		10.92		0.430
eC	0.00	1.52	0.000	0.060
L	2.92	3.81	0.115	0.150
N	18		18	
Conforms to Jedec MS-001AC Issue D				

Notes:
1. Leadframe Material: Copper
2. Leadframe finish: Solder Plate
3. Dimensions D, D1 & E1 do not include mould flash or protrusions.
4. Dimensions E & eA are measured with leads constrained to be perpendicular to datum - C -
5. Dimensions eB & eC are measured with the leads unconstrained
6. Controlling dimensions are Inches. Millimeter conversions are not necessarily exact.
7. N is the maximum of terminal positions.

This drawing supersedes: -
Plymouth/Swindon drawing # 418/ED/39502/004

ISSUE	1	2		
ACN	202563	212483		
DATE	9Jun97	5Apr02		
APPRD.				

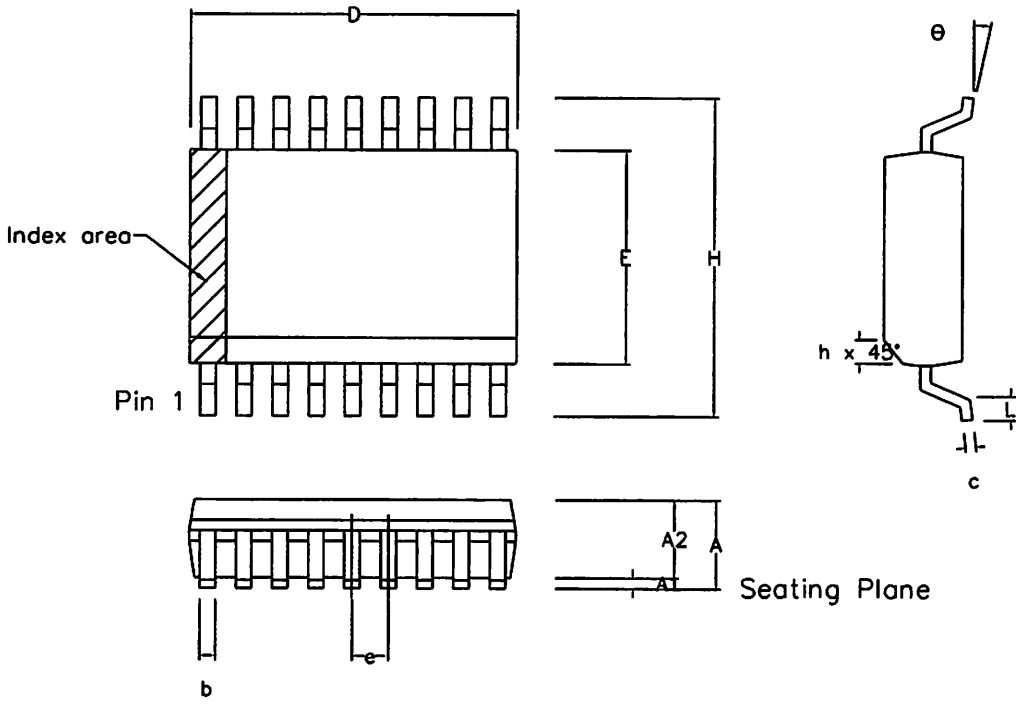
ZARLINK SEMICONDUCTOR

Previous package codes
DP / E

Package Code DA

Package Outline for
18 Lead PDIP

GPD00348



Symbol	Control Dimensions in millimetres				Altern. Dimensions in inches		
	MIN	Nominal	MAX		MIN	Nominal	MAX
A	2.35		2.65		0.093		0.104
A1	0.10		0.30		0.004		0.012
A2	2.25		2.35		0.089		0.092
D	11.35		11.75		0.447		0.463
H	10.00		10.65		0.394		0.419
E	7.40		7.60		0.291		0.299
L	0.40		1.27		0.016		0.050
e	1.27 BSC.				0.050 BSC.		
b	0.33		0.51		0.013		0.020
c	0.23		0.32		0.009		0.013
θ	0°		8°		0°		8°
h	0.25		0.75		0.010		0.029
	Pin features						
N	18						
Conforms to JEDEC MS-013AB Iss. C							

Notes:

1. The chamfer on the body is optional. If not present, a visual index feature, e.g. a dot, must be located within the cross-hatched area.
2. Controlling dimensions are in millimeters
3. Dimension D do not include mould flash, protusion or gate burrs. These shall not exceed 0.006" per side.
4. Dimension E1 do not include inter-lead flash or protusion. These shall not exceed 0.010" per side.
5. Dimension b does not include dambar protusion / intrusion. Allowable dambar protusion shall be 0.004" total in excess of b dimension.

ISSUE	1	2	3	
ACN	6746	201940	212432	
DATE	7Apr95	27Feb97	25Mar02	
APPRD.				

ZARLINK SEMICONDUCTOR

Previous package codes

MP / S

Package Code DC

Package Outline for 18 lead SOIC (0.300" Body Width)

GPD00014

For more information about all Zarlink products visit our Web Site at

www.zarlink.com

SII

Seiko Instruments

M1632

LIQUID CRYSTAL DISPLAY MODULE

USER'S MANUAL

1. GENERAL

1.1 General

The M1632 is a low-power-consumption dot-matrix liquid crystal display (LCD) module with a high-contrast wide-view LCD panel and a CMOS LCD drive controller built in. The controller has a built-in character generator ROM/RAM, and display data RAM. All the display functions are controlled by instructions and the module can easily be interfaced with an MPU. This makes the module applicable to a wide range of purposes including terminal display units for microcomputers and display units for measuring gages.

1.2 Features

- 16-character, two-line liquid crystal display of 5 x 7 dot matrix + cursor
- Duty ratio: 1/16
- Character generator ROM for 192 character types
  (character font: 5 x 7 dot matrix)
- Character generator RAM for eight character types (program write)
  (character font: 5 x 7 dot matrix)
- 80 x 8 bit display data RAM (80 characters maximum)
- Interface with four-bit and eight-bit MPUs possible
- Display data RAM and character generator RAM readable from MPU
- Many instruction functions

  Display Clear, Cursor Home, Display ON/OFF, Cursor ON/OFF, Display Character Blink, Cursor Shift, and Display Shift
- Built-in oscillator circuit
- +5 V single power supply
- Built-in automatic reset circuit at power-on
- CMOS process
- Operating temperature range: 0°C to 50°C

1.3 Block Diagram

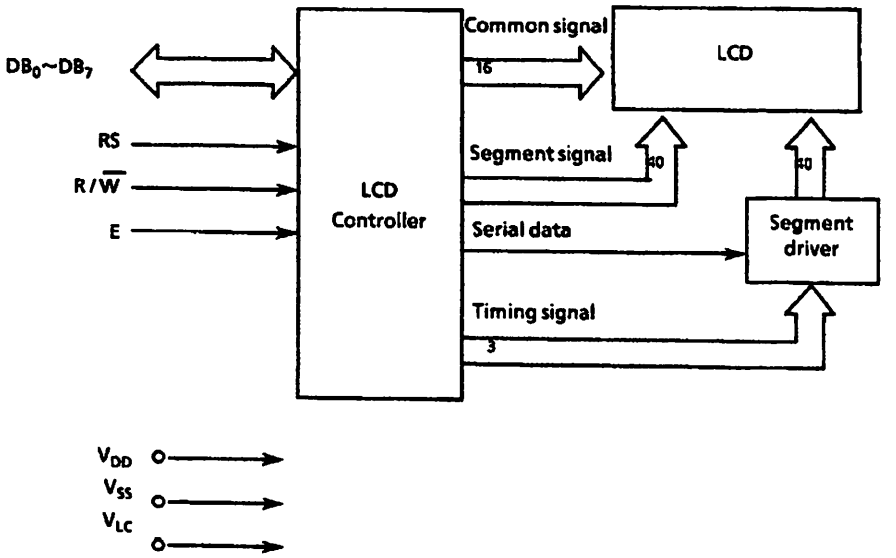


Figure 1

1.4 Absolute Maximum Ratings

V_{SS} = 0 V

Item	Symbol	Standard	Unit	Remarks
Power supply voltage	V_{DD}	− 0.3 to + 7.0	V	
	V_{LC}	V_{DD} − 13.5 to V_{DD} + 0.3	V	
Input voltage	V_{in}	− 0.3 to V_{DD} + 0.3	V	
Operating temperature	T_{opr}	0 to + 50	°C	
Storage temperature	T_{stg}	− 20 to + 60	°C	At 50% RH

1.5 Electrical Characteristics

V_{DD} = 5 V ± 5%, V_{SS} = 0 V, Ta = 0°C to 50°C

Item		Symbol	Condition	Min.	Typ.	Max.	Unit
Input voltage*	High	V_{IH1}		2.2	−	V_{DD}	V
	Low	V_{IL1}		0	−	0.6	V
Output voltage**	High	V_{OH1}	$-I_{OH}$ = 0.205 mA	2.4	−	−	V
	Low	V_{OL1}	I_{OL} = 1.2 mA	−	−	0.4	V
Power supply voltage		V_{DD}		4.75	5.00	5.25	V
		V_{DD}-V_{LC}		1.5	−	−	V
Current consumption		I_{DD}		−	2.0	3.0	mA
		I_{LC}	V_{LC} = 0.25V	−	0.2	1.0	mA
Clock oscillation freq.		f_{osc}	Resistance oscillation	190	270	350	kHz

* Applied to DB_0 to DB_7, E, R/$\overline{W}$, and RS
** Applied to DB_0 to DB_7

Remark: Recommended operating voltage

The viewing angle and screen contrast of the LCD panel can be varied by changing the liquid crystal operating voltage (V_{Opr}), that is V_{LC}.
The optical characteristics is influenced by an ambient temperature. The recommended value of V_{Opr} for an ambient temperatures are shown below.

Temperature (°C)	0	10	25	40	50
V_{opr} (V)	5.00	4.90	4.75	4.60	4.50

$V_{opr} = V_{DD} - V_{LC}$

1.6 Timing Characteristics

1.6.1 Write operation

V_{DD} = 5.0 V ± 5%, V_{SS} = 0 V, Ta = 0°C to 50°C

Item		Symbol	Min.	Max.	Unit
Enable cycle time		$t_{CYC}E$	1000	–	ns
Enable pulse width	High level	PW_{EH}	450	–	ns
Enable rise and fall time		t_{Er},t_{Ef}	–	25	ns
Setup time	RS, R/$\overline{W}$ → E	t_{AS}	140	–	ns
Address hold time		t_{AH}	10	–	ns
Data setup time		t_{DSW}	195	–	ns
Data hold time		t_H	10	–	ns

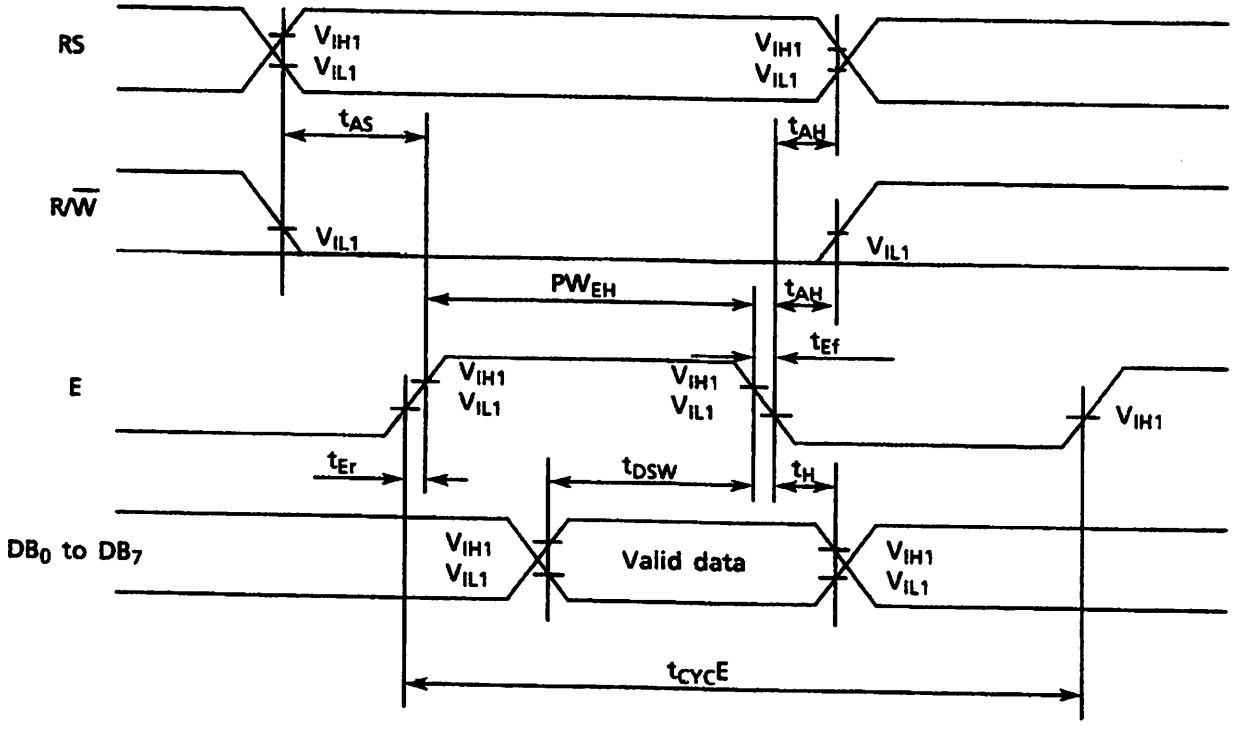


Figure 2 Data write from MPU to module

1.6.2 Read operation

V_{DD} = 5.0 V ± 5%, V_{SS} = 0 V, Ta = 0°C to 50°C

Item		Symbol	Min.	Max.	Unit
Enable cycle time		$t_{CYC}E$	1000	–	ns
Enable pulse width	High level	PW_{EH}	450	–	ns
Enable rise and fall time		t_{Er},t_{Ef}	–	25	ns
Setup time	RS, R/$\overline{W}$→E	t_{AS}	140	–	ns
Address hold time		t_{AH}	10	–	ns
Data delay time		t_{DDR}	–	320	ns
Data hold time		t_H	20	–	ns

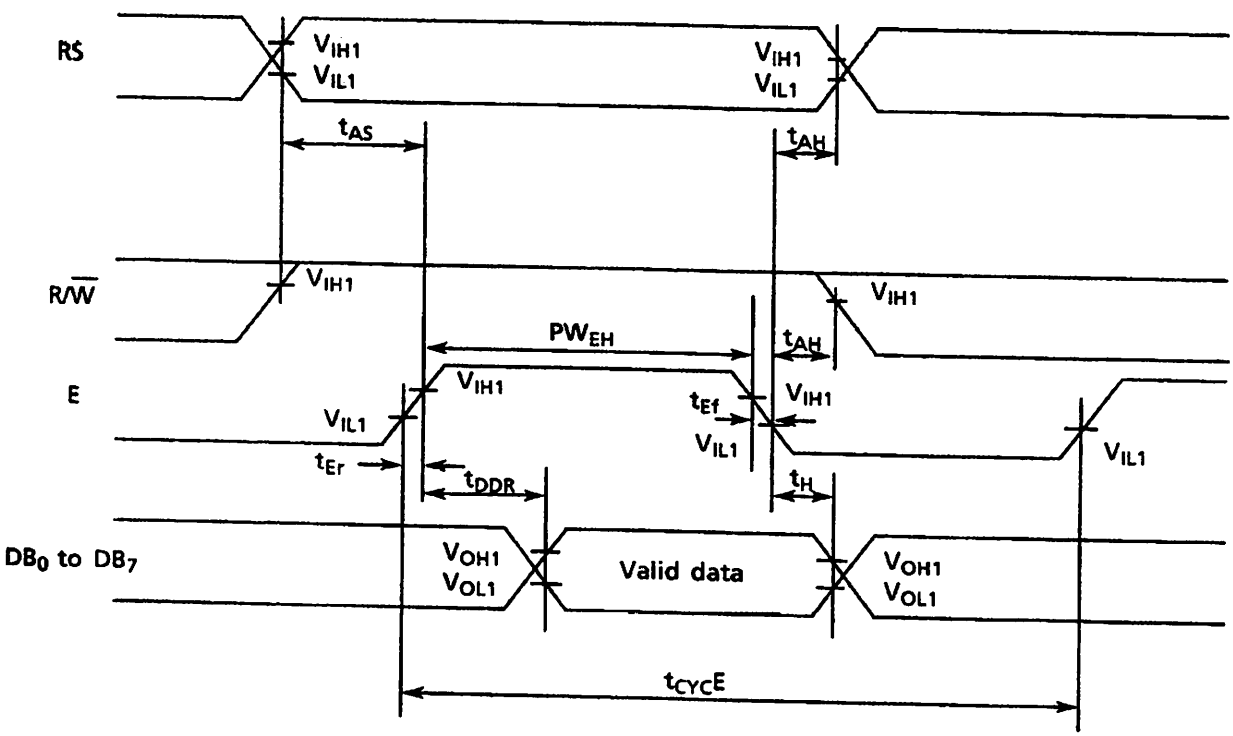


Figure 3 Data read from module to MPU

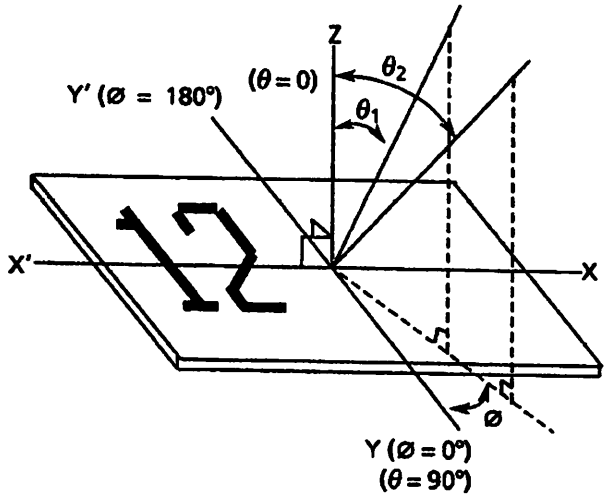
1.7 Optical Characteristics

1.7.1 Optical characteristics (TN LCD)

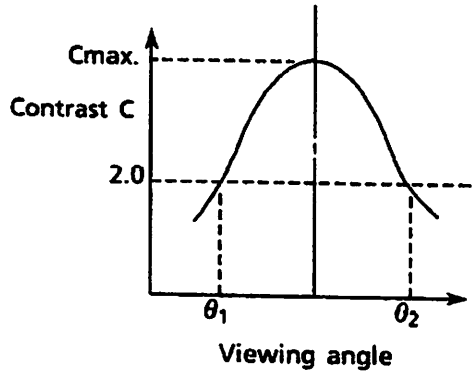
Viewing angle: 6 o'clock ($\varnothing$ = 0°)
Ta = 25°C, V_{opr} = 4.75 V

Item	Symbol	Conditions	Min.	Typ.	Max.	Remarks
Viewing angle	$\theta_2 - \theta_1$	$C \geq 2.0$, $\varnothing = 0°$	35	–	–	See Notes 1 and 2.
Contrast	C	$\theta = 25°$, $\varnothing = 0°$	5	8	–	See Note 3.
Response time (rise)	t_{on}	$\theta = 25°$, $\varnothing = 0°$	–	60 ms	70 ms	See Note 4.
Response time (fall)	t_{off}	$\theta = 25°$, $\varnothing = 0°$	–	150 ms	170 ms	See Note 4.

Note 1: Definition of angles $\varnothing$ and θ

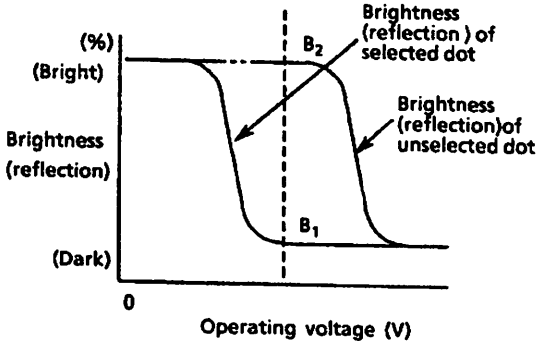


Note 2: Definition of viewing angles θ_1 and θ_2

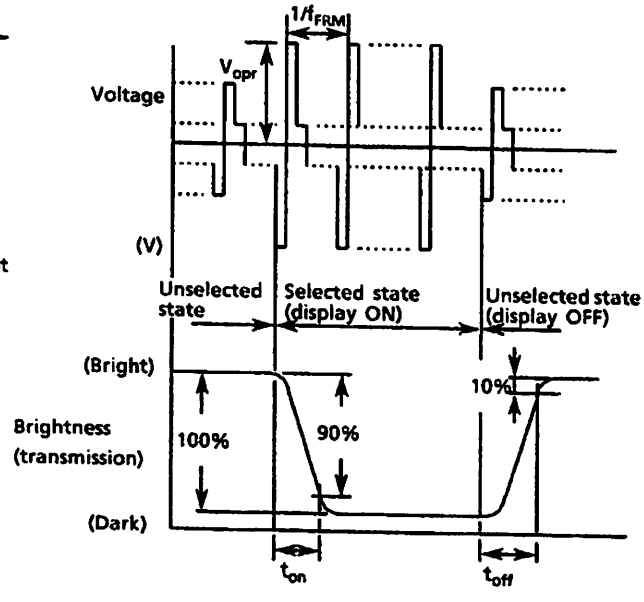


Note 3: Definition of contrast C

$$C = \frac{\text{Brightness (reflection) of unselected dot (B2)}}{\text{Brightness (reflection) of selected dot (B1)}}$$

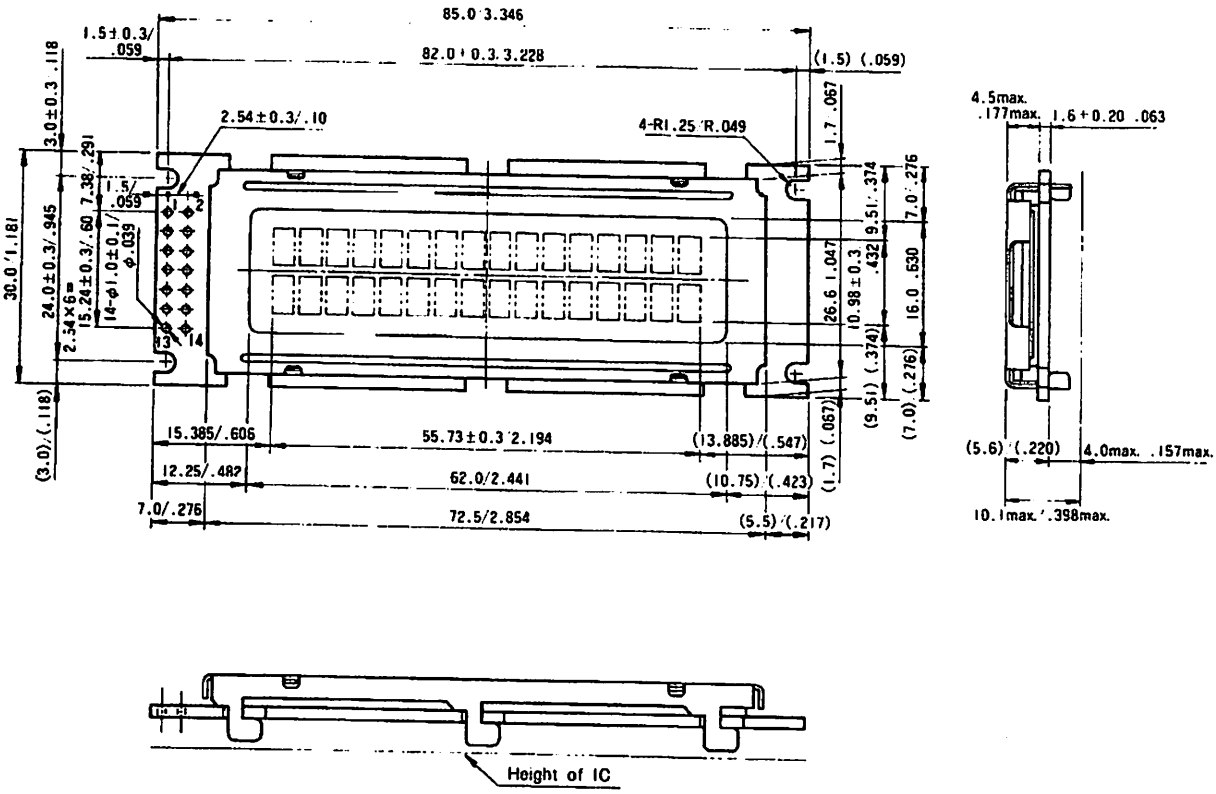


Note 4: Definition of response time



V_{opr} : Operating voltage
f_{FRM} : Frame frequency
t_{on} : Response time (rise)
t_{off} : Response time (fall)

1.8 Dimensions



I/O terminal symbol

No.	Symbol
1	DB_7
2	DB_6
3	DB_5
4	DB_4
5	DB_3
6	DB_2
7	DB_1
8	DB_0
9	E
10	$R/\overline{W}$
11	RS
12	V_{LC}
13	V_{SS}
14	V_{DD}

Figure 4

2. OPERATING INSTRUCTIONS

2.1 Terminal Functions

Table 1 Terminal functions

Signal name	No. of terminals	I/O	Destination	Function
DB_0 to DB_3	4	I/O	MPU	Tristate bidirectional lower four data buses: Data is read from the module to the MPU or written to the module from the MPU through the buses. If the interface data is 4 bits, the signals are not used.
DB_4 to DB_7	4	I/O	MPU	Tristate bidirectional upper four data buses: Data is read from the module to the MPU or written to the module from the MPU through the buses. DB_7 is also used as a busy flag.
E	1	Input	MPU	Operation start signal: The signal activates data write or read.
R/$\overline{W}$	1	Input	MPU	Read (R) and Write ($\overline{W}$) selection signals 0 : Write 1 : Read
RS	1	Input	MPU	Register selection signals 0 : Instruction register (Write) Busy flag and address counter (Read) 1 : Data register (Write and Read)
V_{LC}	1	–	Power supply	Power supply terminal for driving liquid crystal display: The screen contrast can be varied by changing V_{LC}.
V_{DD}	1	–	Power supply	+5 V
V_{SS}	1	–	Power supply	Ground terminal: 0 V

2.2 Basic Operations

2.2.1 Registers

The controller has two kinds of eight-bit registers: the instruction register (IR) and the data register (DR). They are selected by the register select (RS) signal as shown in Table 2.

The IR stores instruction codes such as Display Clear and Cursor Shift, and the address information of display data RAM (DD RAM) and character generator RAM (CG RAM). They can be written from the MPU, but cannot be read to the MPU.

The DR temporarily stores data to be written into DD RAM or CG RAM, or read from DD RAM or CG RAM. When data is written into DD RAM or CG RAM from the MPU, the data in the DR is automatically written into DD RAM or CG RAM by internal operation. However, when data is read from DD RAM or CG RAM, the necessary data address is written into the IR. The specified data is read out to the DR and then the MPU reads it from the DR. After the read operation, the next address is set and DD RAM or CG RAM data at the address is read into the DR for the next read operation.

Table 2 Register selection

RS	R/$\overline{W}$	Operation
0	0	IR selection, IR write. Internal operation : Display clear
0	1	Busy flag (DB_7) and address counter (DB_0 to DB_6) read
1	0	DR selection, DR write. Internal operation : DR to DD RAM or CG RAM
1	1	DR selection, DR read. Internal operation : DD RAM or CG RAM to DR

2.2.2 Busy flag (BF)

The flag indicates whether the module is ready to accept the next instruction. As shown in Table 2, the signal is output to DB_7 if RS = 0 and R/$\overline{W}$ = 1. If the value is 1, the module is working internally and the instruction cannot be accepted. If the value is 0, the next instruction can be written. Therefore, the flag status needs to be checked before executing an instruction. If an instruction is executed without checking the flag status, wait for more than the execution time shown by 2.4 Instruction Outline.

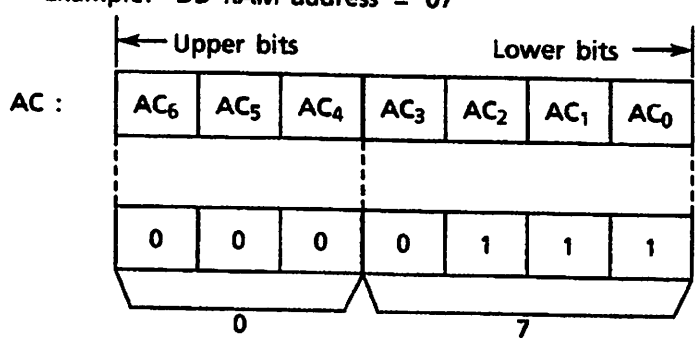
2.2.3 Address counter (AC)

The counter specifies an address when data is written into DD RAM or CG RAM and the data stored in DD RAM or CG RAM is read out. If an Address Set instruction (for DD RAM or CG RAM) is written in the IR, the address information is transferred from the IR to the AC. When display data is written into or read from DD RAM or CG RAM, the AC is automatically incremented or decremented by one according to the Entry Mode Set. The contents of the AC are output to DB_0 to DB_6 as shown in Table 2 if RS = 0 and $R/\overline{W} = 1$.

2.2.4 Display data RAM (DD RAM)

DD RAM has a capacity of up to 80 × 8 bits and stores display data of 80 eight-bit character codes. Some storage areas of DD RAM which are not used for display can be used as general data RAM.
A DD RAM address to be set in the AC is expressed in hexadecimal form as follows.

Example: DD RAM address = 07



DD RAM addresses 00_H to $0F_H$ are set in the line 1, and 40_H to $4F_H$ in the line 2.

Note : The addresses in the digit 16 of line 1 and the digit 1 of line 2 are not consecutive.

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	Display digit
Line 1	00	01	02	03	04	05	06	07	08	09	0A	0B	0C	0D	0E	0F	DD RAM address
Line 2	40	41	42	43	44	45	46	47	48	49	4A	4B	4C	4D	4E	4F	

If the display is shifted, DD RAM addresses 00_H to 27_H are displayed in line 1 and 40_H to 67_H in line 2. The following figures are examples of display shifts.

*Left shift

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	Display digit
Line 1	01	02	03	04	05	06	07	08	09	0A	0B	0C	0D	0E	0F	10	DD RAM address
Line 2	41	42	43	44	45	46	47	48	49	4A	4B	4C	4D	4E	4F	50	

*Right shift

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	Display digit
Line 1	27	00	01	02	03	04	05	06	07	08	09	0A	0B	0C	0D	0E	DD RAM address
Line 2	67	40	41	42	43	44	45	46	47	48	49	4A	4B	4C	4D	4E	

2.2.5 Character generator ROM (CG ROM)

Character generator ROM generates 192 types of 5 x 7 dot-matrix character patterns from eight-bit character codes.

Table 3 shows the correspondence between the CG ROM character codes and character patterns.

2.2.6 Character generator RAM (CG RAM)

CG RAM is used to create character patterns freely by programming. Eight types of character patterns can be written.

Table 4 shows the character patterns created from CG RAM addresses and data. To display a created character pattern, the character code in the left column of the table is written into DD RAM corresponding to the display position (digit). The areas not used for display are available as general data RAM.

Table 3 Correspondence between character codes and character patterns

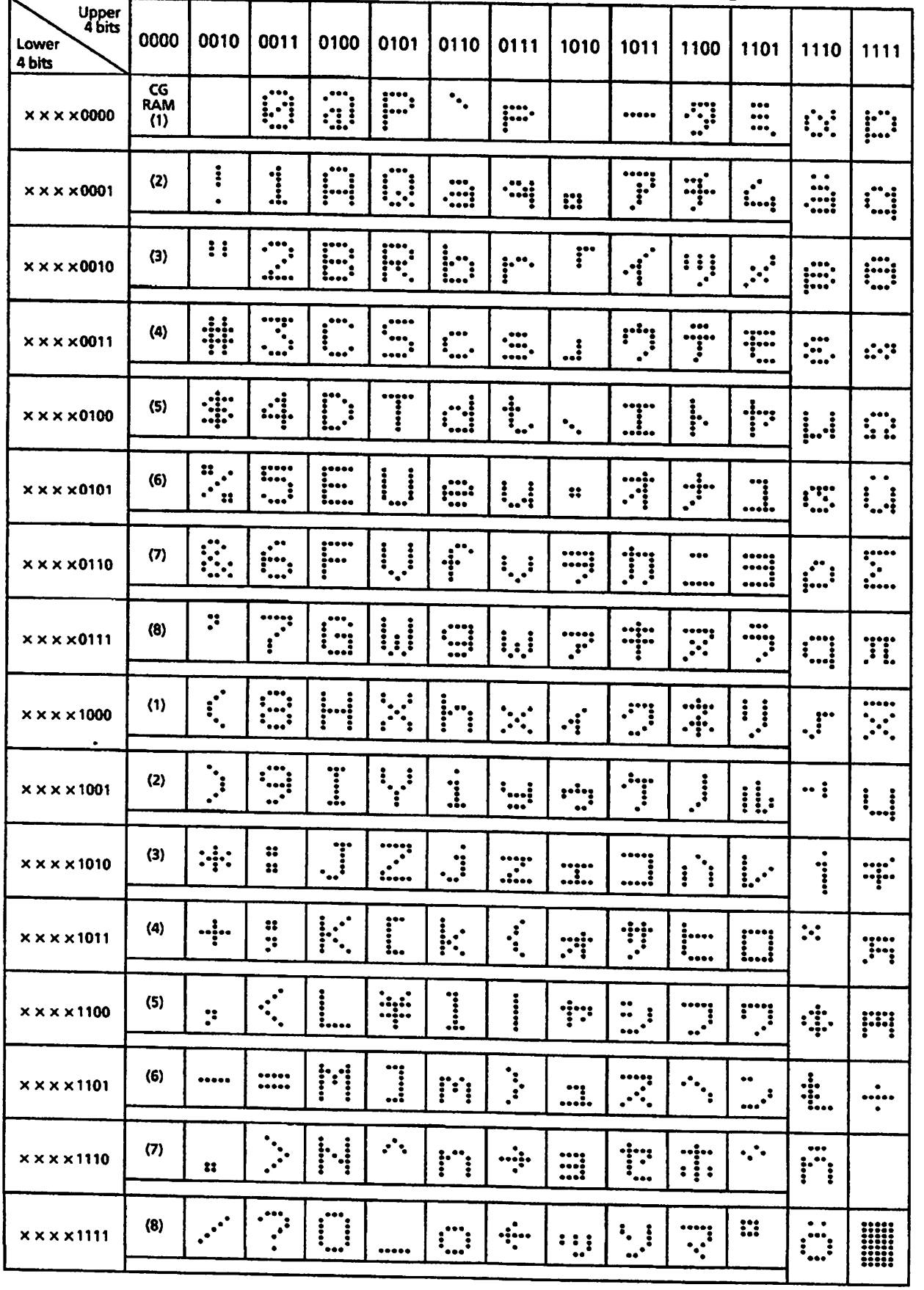


Table 4 Relationships between CG RAM addresses and character codes (DD RAM) and character patterns (CG RAM data)

Character code (DD RAM data) 7 6 5 4 3 2 1 0 (Upper bit ← Lower bit →)	CG RAM address 5 4 3 2 1 0 (Upper bit ← Lower bit →)	Character pattern (CG RAM data) 7 6 5 4 3 2 1 0 (Upper bit ← Lower bit →)
0 0 0 0 * 0 0 0	0 0 0	* * * 0 0 0 0 1 / 0 0 0 1 / 0 0 0 1 / 0 1 1 1 0 / 0 0 1 0 0 / 0 0 0 1 0 / 0 0 0 0 1 / * * * 0 0 0 0 0
0 0 0 0 * 0 0 1	0 0 1	* * * 0 0 0 1 / 0 1 0 1 0 / 1 1 1 1 1 / 0 0 1 0 0 / 0 0 1 0 0 / 0 0 1 0 0 / * * * 0 0 0 0 0
	0 1 0	* * *
0 0 0 0 * 1 1 1	1 1 1	1 0 0 / 1 0 1 / 1 1 0 / 1 1 1 / * * *

Example of character pattern (R)

← Cursor position

Example of character pattern (¥)

Notes: • In CG RAM data, 1 corresponds to Selection and 0 to Non-selection on the display.

- Character code bits 0 to 2 and CG RAM address bits 3 to 5 correspond with each other (three bits, eight types).
- CG RAM address bits 0 to 2 specify a line position for a character pattern. Line 8 of a character pattern is the cursor position where the logical sum of the cursor and CG RAM data is displayed. Set the data of line 8 to 0 to display the cursor. If the data is changed to 1, one bit lights, regardless of the cursor.
- The character pattern column positions correspond to CG RAM data bits 0 to 4 and bit 4 comes to the left end. CG RAM data bits 5 to 7 are not displayed but can be used as general data RAM.
- When reading a character pattern from CG RAM, set to 0 all of character code bits 4 to 7. Bits 0 to 2 determine which pattern will be read out. Since bit 3 is not valid, 00_H and 08_H select the same character.

2.3 Instruction Outline

Table 5 List of instructions

Instruction	Code										Function	Execution time*
	RS	R/$\overline{W}$	DB_7	DB_6	DB_5	DB_4	DB_3	DB_2	DB_1	DB_0		
(1) Display clear	0	0	0	0	0	0	0	0	0	1	Clears all display and returns cursor to home position (address 0)	1.64 ms
(2) Cursor Home	0	0	0	0	0	0	0	0	1	*	Returns cursor to home position. Shifted display returns to home position and DD RAM contents do not change.	1.64 ms
(3) Entry Mode Set	0	0	0	0	0	0	0	1	I/D	S	Sets direction of cursor movement and whether display will be shifted when data is written or read	40 µs
(4) Display ON/OFF control	0	0	0	0	0	0	1	D	C	B	Turns ON/OFF total display (D) and cursor (C), and makes cursor position column start blinking (B)	40 µs
(5) Cursor/Display Shift	0	0	0	0	0	1	S/C	R/L	*	*	Moves cursor and shifts display without changing DD RAM contents	40 µs
(6) Function Set	0	0	0	0	1	DL	N	F	*	*	Sets interface data length (DL), the number of display lines (N), and character fonts (F)	40 µs
(7) CG RAM Address Set	0	0	0	1	A_{CG}						Sets CG RAM address to start transmitting or receiving CG RAM data	40 µs
(8) DD RAM Address Set	0	0	1	A_{DD}							Sets DD RAM address to start transmitting or receiving DD RAM data	40 µs
(9) BF/Address Read	0	1	BF	AC							Reads BF indicating module in internal operation and AC contents (used for both CG RAM and DD RAM)	0 µs
(10) Data Write to CG RAM or DD RAM	1	0	Write Data								Writes data into DD RAM or CG RAM	40 µs
(11) Data Read from CG RAM or DD RAM	1	1	Read Data								Reads data from DD RAM or CG RAM	40 µs

* : Invalid bit
A_{CG} : CG RAM address
A_{DD} : DD RAM address
AC : Address counter

I/D = 1 : Increment
I/D = 0 : Decrement

S = 1 : Display shift
S = 0 : No display shift

D = 1 : Display ON
D = 0 : Display OFF

C = 1 : Cursor ON
C = 0 : Cursor OFF

B = 1 : Blink ON
B = 0 : Blink OFF

S/C = 1 : Display shift
S/C = 0 : Cursor movement

R/L = 1 : Right shift
R/L = 0 : Left shift

DL = 1 : 8 bits
DL = 0 : 4 bits

N = 1 : 2 lines
N = 0 : 1 line

F = 1 : 5×10 dot matrix
F = 0 : 5×7 dot matrix

BF = 1 : Internal operation in progress
BF = 0 : Instruction can be accepted

* An execution time indicates maximum value when f_{osc} is 250 kHz. It changes at the inverse proportion of f_{osc}.

2.4 Instruction Details

(1) Display Clear

	RS	R/$\overline{W}$	DB_7							DB_0
Code	0	0	0	0	0	0	0	0	0	1

Display Clear clears all display and returns cursor to home position (address 0). Space code 20 (hexadecimal) is written into all the addresses of DD RAM, and DD RAM address 0 is set to the AC. If shifted, the display returns to the original position. After execution of the Display Clear instruction, the entry mode is incremented.

Note : When executing the Display Clear instruction, follow the restrictions listed in Table 6.

(2) Cursor Home

	RS	R/$\overline{W}$	DB_7							DB_0
Code	0	0	0	0	0	0	0	0	1	*

* : Don't care bit

Cursor Home returns cursor to home position (address 0).
DD RAM address 0 is set to the AC. The cursor returns to the home position. If shifted, the display returns to the original position. The DD RAM contents do not change. If the cursor or blinking is ON, it returns to the left side.

Note : When executing the Cursor Home instruction, follow the restrictions listed in Table 6.

Table 6 Restrictions on execution of Display Clear and Cursor Home instructions

Conditions of use	Restrictions
When executing the Display Clear or Cursor Home instruction when the display is shifted (after execution of Display Shift instruction)	The Cursor Home instruction should be executed again immediately after the Display Clear or Cursor Home instruction is executed. Do not leave an interval of a multiple of $400/f_{osc}$* second after the first execution. Example: 1.5 ms, 3 ms, 4.5 ms for f_{osc} = 270 kHz *f_{osc}: Oscillation frequency
When 23_H, 27_H, 63_H, or 67_H is used as a DD RAM address to execute Cursor Home instruction	Before executing the Cursor Home instruction, the data of the four DD RAM addresses given at the left should be read and saved. After execution, write the data again in DD RAM. (This restriction is necessary to prevent the contents of the DD RAM addresses from being destroyed after the Cursor Home instruction has been executed.)

(3) Entry Mode Set

	RS	R/$\overline{W}$	DB_7							DB_0
Code	0	0	0	0	0	0	0	1	I/D	S

Entry Mode Set sets the direction of cursor movement and whether display will be shifted.

I/D : The DD RAM address is incremented or decremented by one when a character code is written into or read from DD RAM. This is also true for writing into or reading from CG RAM.

When I/D = 1, the address is incremented by one and the cursor or blink moves to the right.

When I/D = 0, the address is decremented by one and the cursor or blink moves to the left.

S : If S = 1, the entire display is shifted either to the right or left for writing into DD RAM. The cursor position does not change, only the display moves. There is no display shift for reading from DD RAM.

When S = 1 and I/D = 1, the display shifts to the left.
When S = 1 and I/D = 0, the display shifts to the right.

If S = 0, the display does not shift.

(4) Display ON/OFF Control

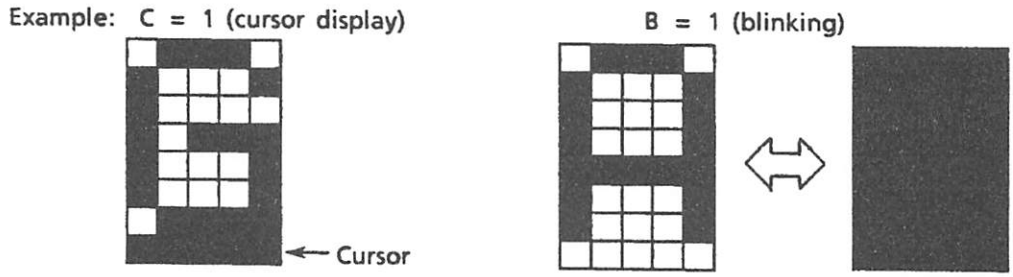
	RS	R/$\overline{W}$	DB_7							DB_0
Code	0	0	0	0	0	0	1	D	C	B

Display ON/OFF Control turns the total display and the cursor ON and OFF, and makes the cursor position start blinking. Cursor ON/OFF and blinking is done at the column indicated by the specified DD RAM address by the AC.

D : When D = 1, the display is turned ON.
When D = 0, the display is turned OFF.
If D = 0 is used, display data remains in DD RAM. Change 0 to 1 to display data.

C : When C = 1, the cursor is displayed.
When C = 0, the cursor is not displayed.
The cursor is displayed in the dot line below the character fonts.

B : When B = 1, the character at the cursor position starts blinking.
When B = 0, it does not blink.
For blinking, all-black dots and the character are switched about every 0.4 seconds when f_{osc} is 250 kHz. The cursor and blinking can be set at the same time.



(5) Cursor/Display Shift

	RS	R/$\overline{W}$	DB_7							DB_0
Code	0	0	0	0	0	1	S/C	R/L	*	*

* : Don't care bit

Cursor/Display Shift moves the cursor and shifts the display without changing the DD RAM contents.
The cursor position and the AC contents match. This instruction is available for display correction and retrieval because the cursor position or display can be shifted without writing or reading display data. Since the DD RAM capacity is 40-character by two lines, the cursor is shifted from digit 40 of line 1 to digit 1 of line 2. Displays of lines 1 and 2 are shifted at the same time. Therefore, the display pattern of line 2 is not shifted to line 1.

S/C	R/L	Operation
0	0	The cursor position is shifted to the left (the AC decrements one)
0	1	The cursor position is shifted to the right (the AC increments one)
1	0	The entire display is shifted to the left with the cursor
1	1	The entire display is shifted to the right with the cursor

Note: If only display shift is done, the AC contents do not change.

(6) Function Set

	RS	R/$\overline{W}$	DB_7						DB_0	
Code	0	0	0	0	1	DL	N	F	*	*

* : Don't care bit

Function Set sets the interface data length, the number of display lines, and the character font.

DL : Interface data length
When DL = 1, the data length is set at eight bits (DB_7 to DB_0).
When DL = 0, the data length is set at four bits (DB_7 to DB_4).
The upper four bits are transferred first, then the lower four bits follow.

N : Number of display lines
When N = 1, the display line is set to two lines.
When N = 0, the display line is set to one line.
For M1632, set N to 1.

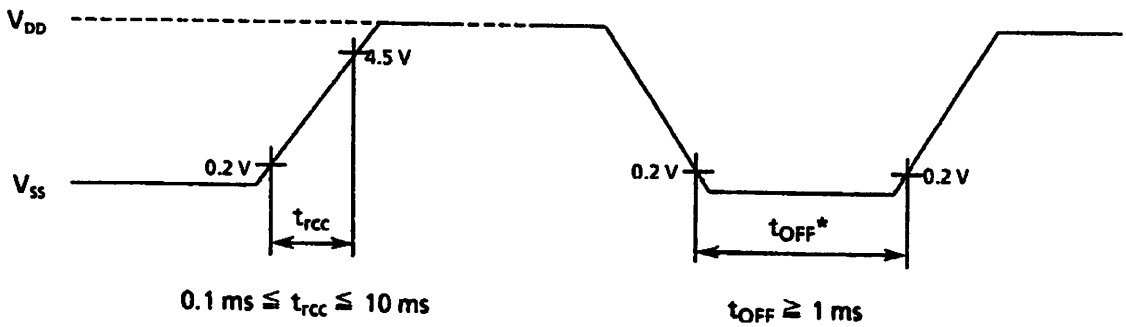
F : Character font
When F = 1, the character font is set to 5×10 dot matrix.
When F = 0, the character font is set to 5×7 dot matrix.
If N is set to 1, F becomes "Don't care bit". For M1632, set F to 0 or 1.

The Function Set instruction must be executed prior to all other instructions except for Busy Flag/Address Read. If another instruction is executed first, no function instruction except changing the interface data length can be executed.

Remarks: Initialization

1. Automatic initialization

The system is automatically initialized at power-on if the following power supply conditions are satisfied.



0.1 ms ≦ t_{rcc} ≦ 10 ms

t_{OFF} ≧ 1 ms

*t_{OFF}: Time when power supply is OFF if cut instantaneously or turned ON and OFF repeatedly

The following instructions are executed for initialization.

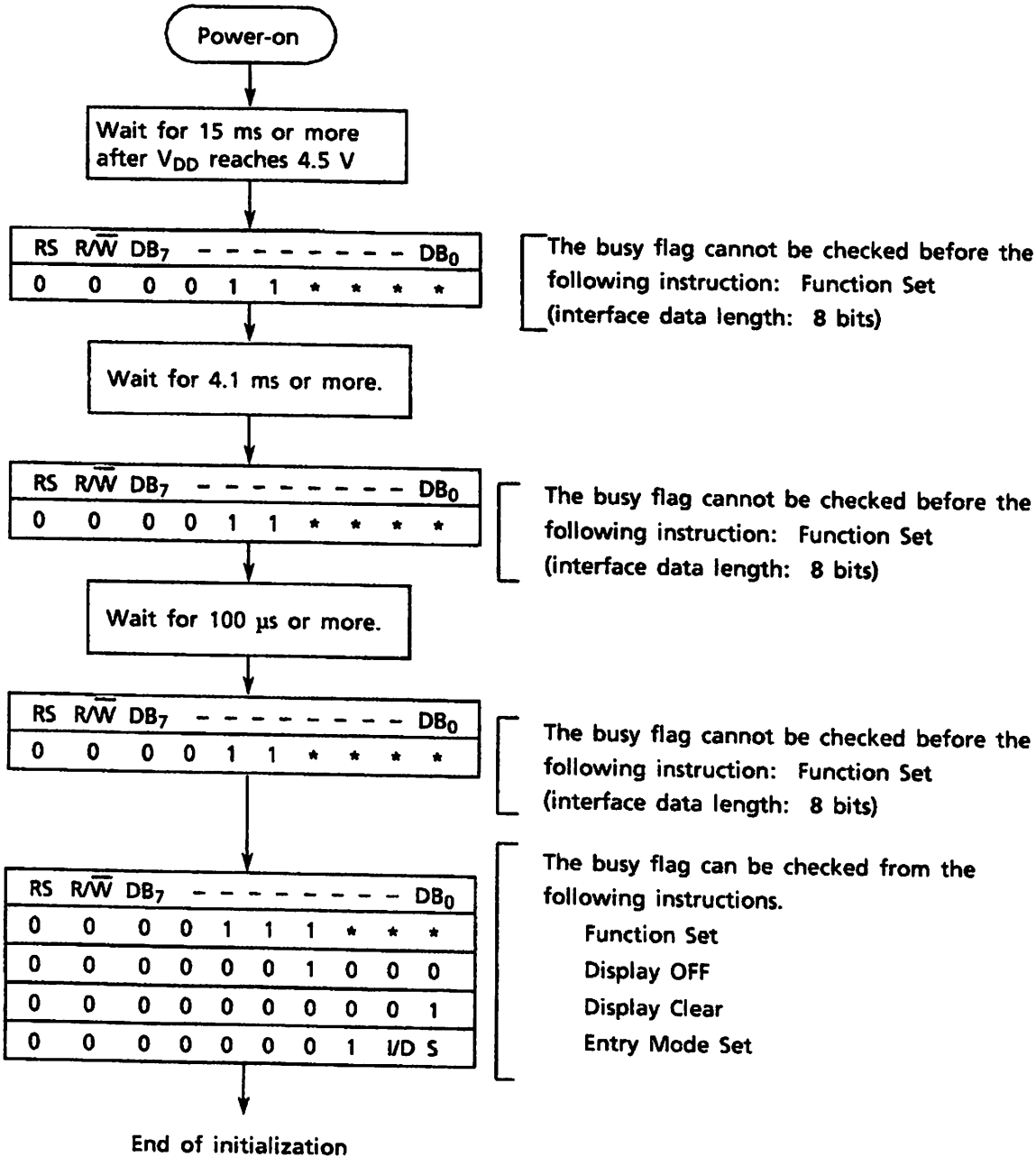
- **Display Clear**
- **Function Set** — **DL = 1: Interface data length: Eight bits**
  N=0: One line display
  F=0: Character font: 5×7 dot matrix
- **Display ON/OFF Control** — **D = 0: Display OFF**
  C = 0: Cursor OFF
  B = 0: Blink OFF
- **Entry Mode Set** — **I/O = 1: Increment**
  S = 0: No display shift

Since the condition is not suitable for the M1632, further Function Set instruction is necessary.

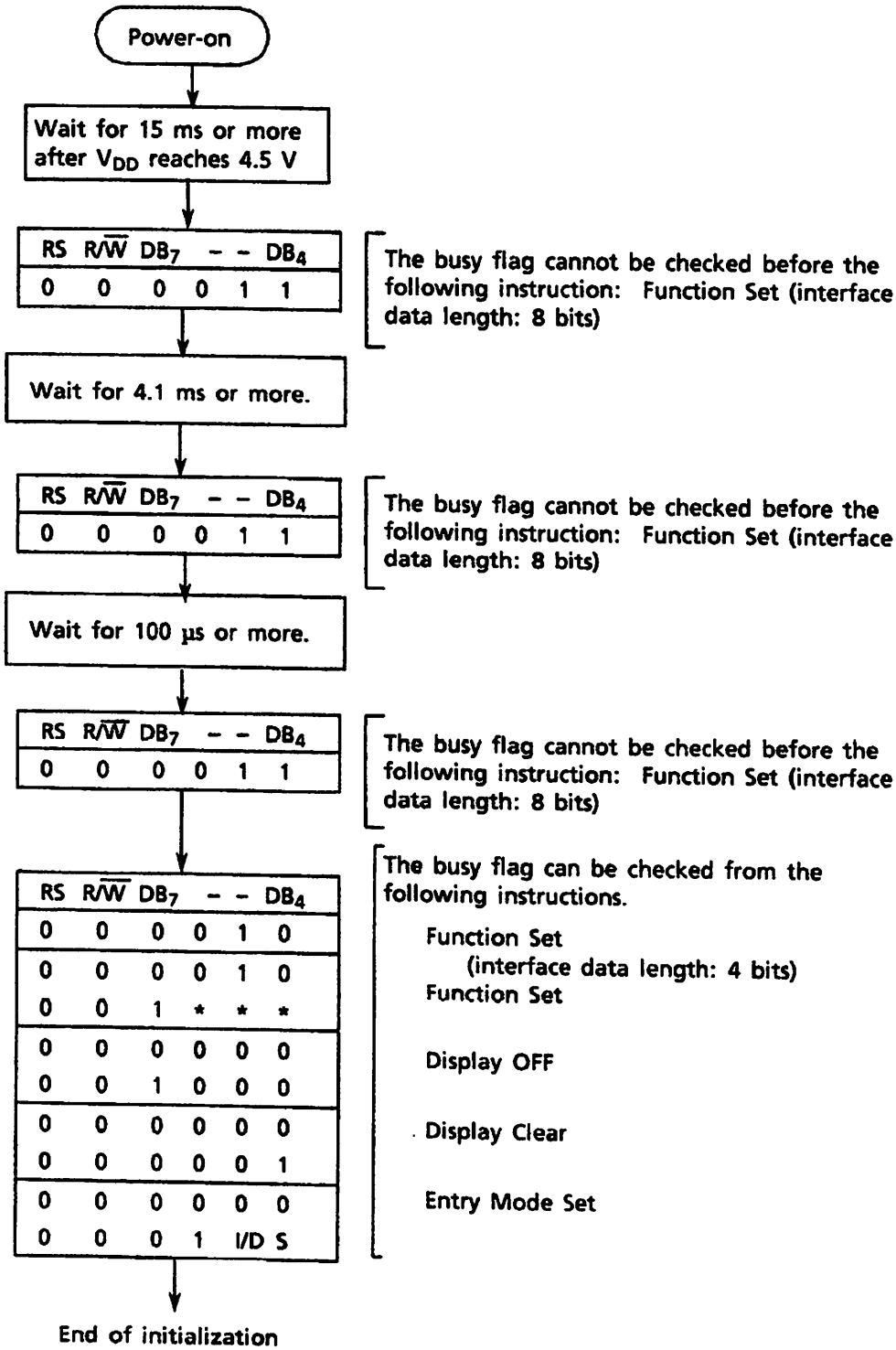
2. Initialization by instructions

If automatic initialization is not executed because the above power supply conditions are not satisfied, use the following instructions. Since it is unknown whether the interface data length is set to eight bits or four bits at power on, execute Function Set twice to set the interface data length to eight bits. And then for setting the required interface data length execute further Function Set instruction.

(a) Interface data length : Eight bits



(b) **Interface data length: Four bits**



(7) CG RAM Address Set

	RS	R/$\overline{W}$	DB_7							DB_0
Code	0	0	0	1	A	A	A	A	A	A
					←Upper bit				Lower bit →	

CG RAM addresses expressed as binary AAAAAA are set to the AC. Then data in CG RAM is written from or read to the MPU.

(8) DD RAM Address Set

	RS	R/$\overline{W}$	DB_7							DB_0
Code	0	0	1	A	A	A	A	A	A	A
				←Upper bit					Lower bit →	

DD RAM addresses expressed as binary AAAAAAA are set to the AC. Then data in DD RAM is written from or read to the MPU. The addresses used for display in line 1 (AAAAAAA) are 00_H to 27_H and those for line 2 (AAAAAAA) are 40_H to 67_H.

(9) Busy Flag/Address Read

	RS	R/$\overline{W}$	DB_7							DB_0
Code	0	1	BF	A	A	A	A	A	A	A
				←Upper bit					Lower bit →	

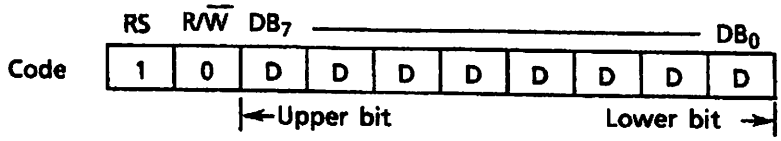
The BF signal is read out, indicating that the module is working internally because of the previous instruction.

When BF = 1, the module is working internally and the next instruction cannot be accepted until the BF value becomes 0.

When BF = 0, the next instruction can be accepted.

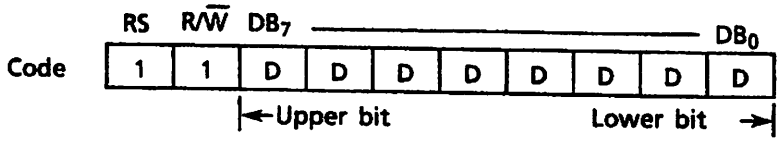
Therefore, make sure that BF = 0 before writing the next instruction. The AC values of binary AAAAAAA are read out at the same time as reading the busy flag. The AC addresses are used for both CG RAM and DD RAM but the address set before execution of the instruction determines which address is to be used.

(10) Data Write to CG RAM or DD RAM



Binary eight-bit data DDDDDDDD is written into CG RAM or DD RAM. The CG RAM Address Set instruction of (7) or the DD RAM Address Set instruction of (8) before this instruction selects either RAM. After the write operation, the address and display shift are determined by the entry mode setting.

(11) Data Read from CG RAM or DD RAM



Binary eight-bit data DDDDDDDD is read from CG RAM or DD RAM. The CG RAM Address Set instruction of (7) or the DD RAM Address Set instruction of (8) before this instruction selects either RAM. In addition, either instruction (7) or (8) must be executed immediately before this instruction. If no address set instruction is executed before a read instruction, the first data read becomes invalid. If read instructions are executed consecutively, data is normally read from the second time. However, if the cursor is shifted by the Cursor Shift instruction when reading DD RAM, there is no need to execute an address set instruction because the Cursor Shift instruction does this.
After the read operation, the address is automatically incremented or decremented by one according to the entry mode, but the display is not shifted.

Note : The AC is automatically incremented or decremented by one according to the entry mode after a write instruction is executed to write data in CG RAM or DD RAM. However, the data of the RAM selected by the AC are not read out even if a read instruction is executed immediately afterwards.

Correct data is read out under the following conditions.

- An address set instruction is executed immediately before readout.
- For DD RAM, the Cursor Shift instruction is executed immediately before readout.
- The second, or later, instruction is executed in consecutive execution of read instructions.

2.5 Examples of Instruction Use

2.5.1 Interface data length: Eight bits

No.	Instruction	Display	Operation
1	Power-on RS: —, R/W: —, DB_7 —— DB_0: —		The built-in reset circuit initializes the module.
2	Function Set RS: 0, R/W: 0, DB_7 —— DB_0: 0 0 1 1 1 * * *		The interface data length is set to 8 bits. The character format becomes 5 x 7 dot-matrix at 1/16 duty cycle.
3	Display ON/OFF Control RS: 0, R/W: 0, DB_7 —— DB_0: 0 0 0 0 1 1 1 0	_	The display and cursor are turned ON, but nothing is displayed.
4	Entry Mode Set RS: 0, R/W: 0, DB_7 —— DB_0: 0 0 0 0 0 1 1 0	_	The address is incremented by one and the cursor shifts to the right in a write operation to internal RAM. The display is not shifted.
5	Write to CG RAM or DD RAM RS: 1, R/W: 0, DB_7 —— DB_0: 0 1 0 0 1 1 0 0	L_	L is written. The AC is incremented by one and the cursor shifts to the right.
6	Write to CG RAM or DD RAM RS: 1, R/W: 0, DB_7 —— DB_0: 0 1 0 0 0 0 1 1	LC_	C is written.
7	⋮	⋮	
8	Write to CG RAM or DD RAM RS: 1, R/W: 0, DB_7 —— DB_0: 0 0 1 1 0 0 1 0	LCD MODULE M1632	2 is written in digit 16. Cursor disappears.

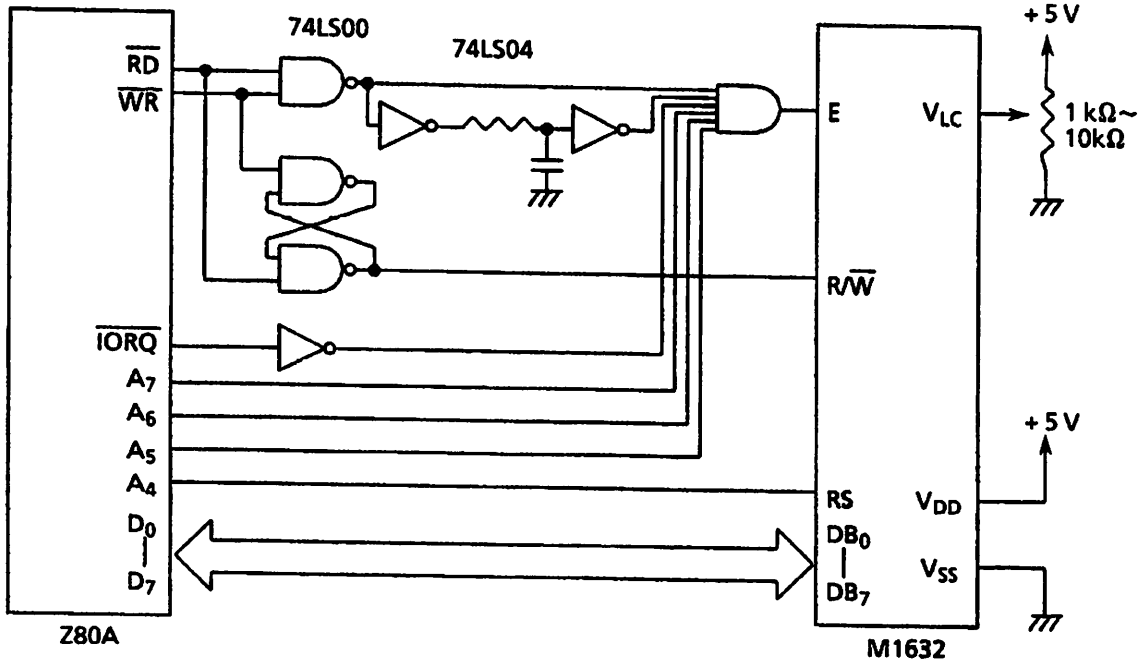
No.	Instruction	Display	Operation
9	DD RAM address set RS: 0, R/W: 0, DB_7 —— DB_0: 1 1 0 0 0 0 0 0	LCD MODULE M1632 _	The DD RAM address is set so that the cursor appears at digit 1 of line 2.
10	Write to CG RAM or DD RAM RS: 1, R/W: 0, DB_7 —— DB_0: 0 0 1 1 0 0 0 1	LCD MODULE M1632 1_	1 is written.
11	Write to CG RAM or DD RAM RS: 1, R/W: 0, DB_7 —— DB_0: 0 0 1 1 0 1 1 0	LCD MODULE M1632 16_	6 is written.
12	⋮	⋮	
13	Write to CG RAM or DD RAM RS: 1, R/W: 0, DB_7 —— DB_0: 0 1 0 1 0 0 1 1	LCD MODULE M1632 16DIGITS,2LINES	S is written.
14	DD RAM address set RS: 0, R/W: 0, DB_7 —— DB_0: 1 0 0 0 0 0 0 0	LCD MODULE M1632 16DIGITS,2LINES	The cursor returns to the home position.
15	Display clear RS: 0, R/W: 0, DB_7 —— DB_0: 0 0 0 0 0 0 0 1	_	All the display disappears and the cursor remains at the home position.
16	⋮	⋮	

2.5.2 Interface data length: Four bits

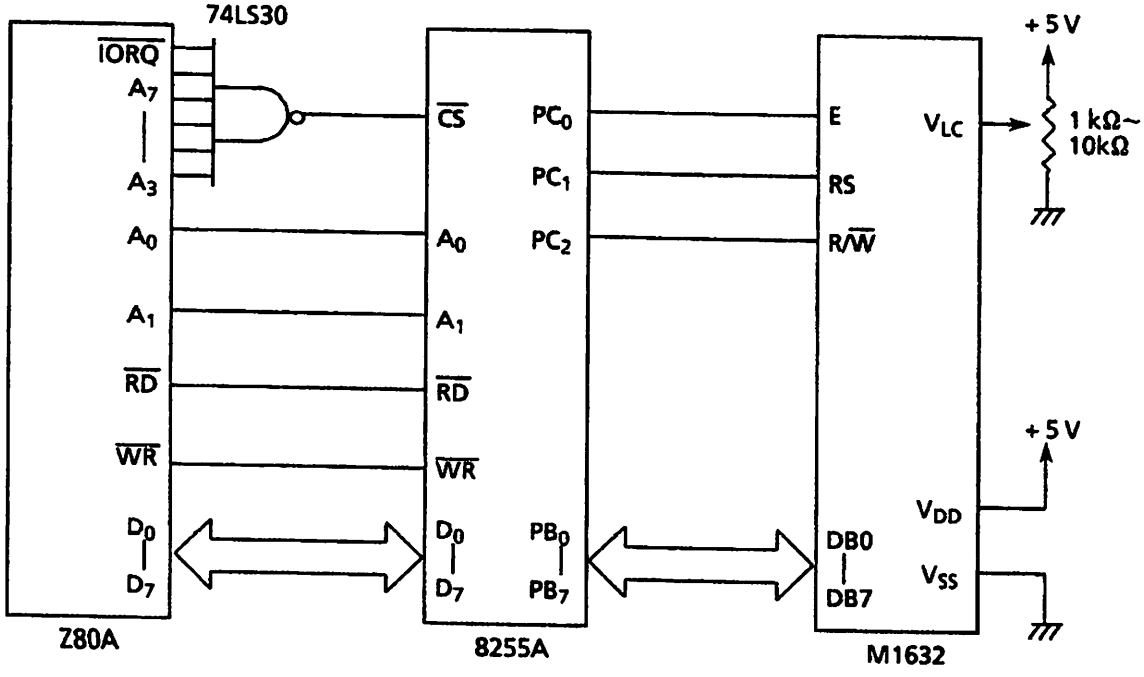
No.	Instruction	Display	Operation
1	Power-on RS | R/W | DB7 — DB4		The built-in reset circuit initializes the module.
2	Function Set RS | R/W | DB7 — DB4 0 | 0 | 0 0 1 0		Four-bit operation mode is set. *Eight-bit operation mode is set by initialization, and the instruction is executed only once.
3	Function Set RS | R/W | DB7 — DB4 0 | 0 | 0 0 1 0 0 | 0 | 1 * * *		The 4-bit operation mode, 1/16 duty cycle, and 5 x 7 dot-matrix character format are selected. Then 4-bit operation mode starts.
4	Display ON/OFF Control RS | R/W | DB7 — DB4 0 | 0 | 0 0 0 0 0 | 0 | 1 1 1 0	_	The display and cursor are turned ON, but nothing is displayed.
5	Entry Mode Set RS | R/W | DB7 — DB4 0 | 0 | 0 0 0 0 0 | 0 | 0 1 1 0	_	The address is incremented by one and the cursor shifts to the right in a write operation to internal RAM. The display is not shifted.
6	Write to CG RAM or DD RAM RS | R/W | DB7 — DB4 1 | 0 | 0 1 0 0 1 | 0 | 1 1 0 0	L_	L is written. the AC is incremented by one and the cursor shifts to the right.
7			

2.6 MPU Connection Diagrams

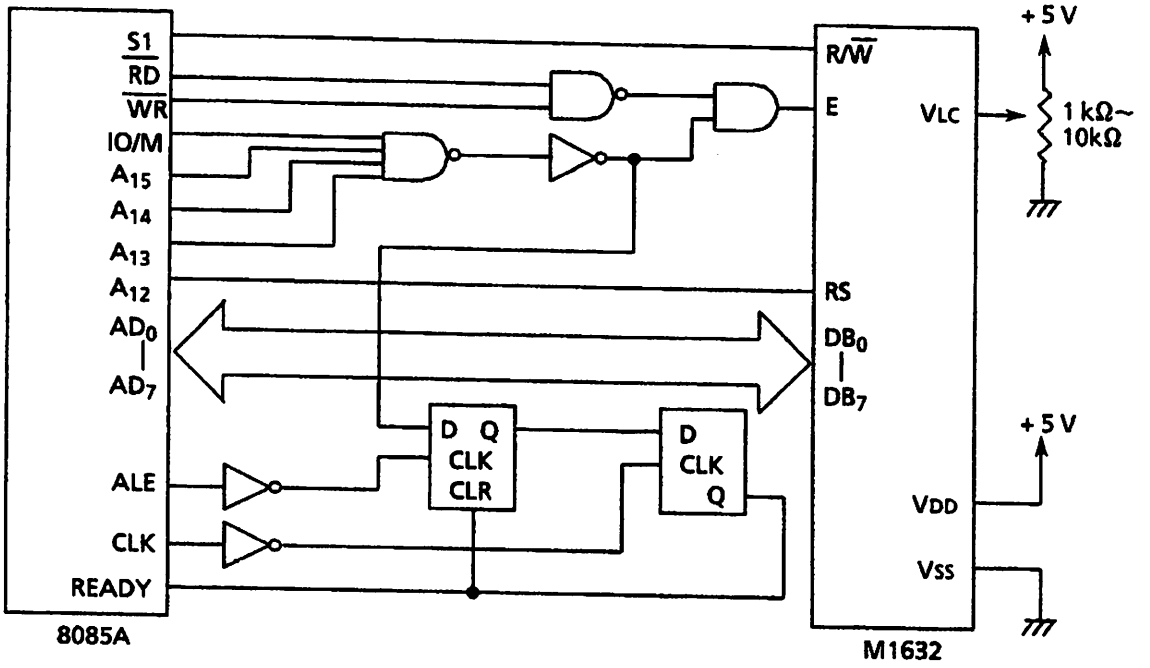
2.6.1 Z80A



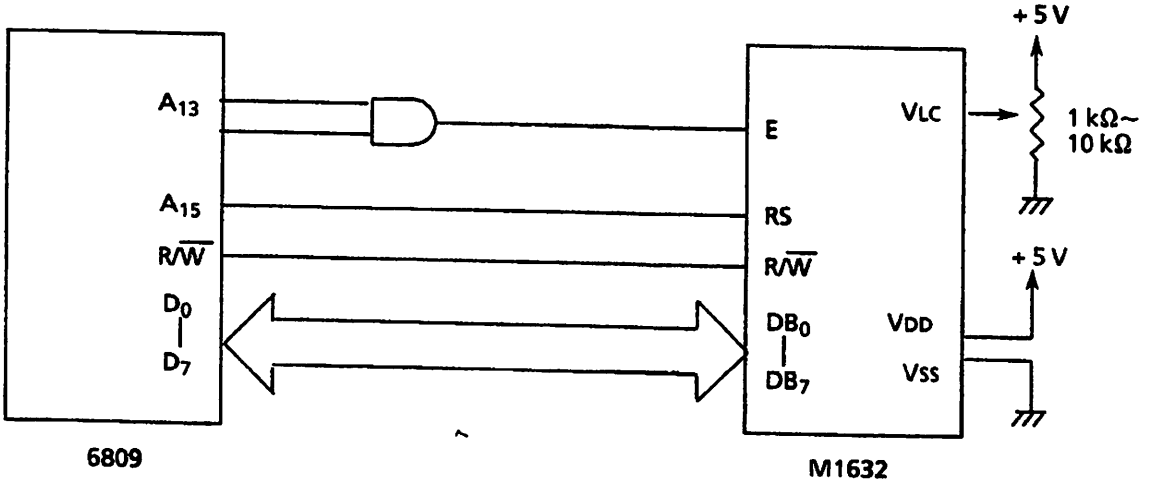
2.6.2 Z80A and 8255A



2.6.3 8085A



2.6.4 6809



3. NOTES

Safety

- If the LCD panel breaks, be careful not to get the liquid crystal in your mouth. If the liquid crystal touches your skin or clothes, wash it off immediately using soap and plenty of water.

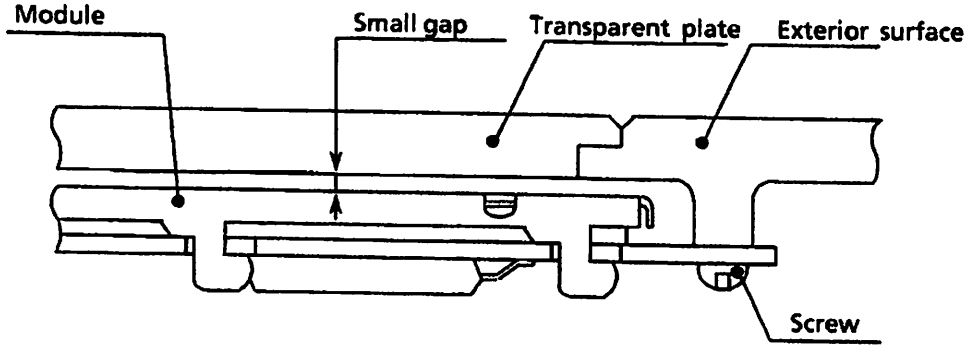
Handling

- Avoid static electricity as this can damage the CMOS LSI.
- The LCD panel is plate glass; do not hit or crush it.
- Do not remove the panel or frame from the module.
- The polarizer of the display is very fragile; handle it very carefully.

Mounting and esign

- Mount the module by using the specified mounting part and holes.
- Connect a 10-μF capacitor between the power supply terminals to eliminate noise.
- To protect the module from external pressure, place a transparent plates (e.g. acrylic or glass), leaving a small gap, over the display surface, frame, and polarizer.

☆Example



- Design the system so that no input signal is given unless the power-supply voltage is applied.
- Keep the module dry. Avoid condensation, otherwise the transparent electrodes may break.

Storage

- Store the module in a dark place where the temperature is 25°C ±10°C and the humidity below 65% RH.
- Do not store the module near organic solvents or corrosive gases.
- Do not crush, shake, or jolt the module (including accessories).

Cleaning

- Do not wipe the polarizer with a dry cloth, as it may scratch the surface.
- Wipe the module gently with a soft cloth soaked with a petroleum benzine.
- Do not use ketonic solvents (ketone and acetone) or aromatic solvents (toluene and xylene), as they may damage the polarizing plate.