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PERANCANGAN DAN PEMBUATAN ALAT PORTABLE DATA ENTRY UNTUK KWH METER DIGITAL MELALUI MEDIA INFRA MERAH YANG DAPAT DIAKSES PADA PC

SKRIPSI

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FAKULTAS TEKNOLOGI INDUSTRI
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2008

ABSTRAKSI

PERANCANGAN DAN PEMBUATAN ALAT PORTABLE DATA ENTRY UNTUK KWH METER DIGITAL MELALUI MEDIA INFRA MERAH YANG DAPAT DIAKSES PADA PC

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Kata Kunci : Mikrokontroler AT89S51, Infra Merah, Max232, LCD, *Push Button*, EEPROM.

Sampai saat ini, PT PLN dalam mengukur konsumsi energi listrik pada sebagian besar pelanggannya, masih menggunakan KWH meter analog atau disebut KWH meter elektromekanik. Salah satu kelemahannya adalah dalam pembacaan hasil pengukuran energi, karena petugas pembaca meter harus mendatangi satu per satu pada alat tersebut, dan mencatatnya secara manual. Hal ini akan berdampak pada pelayanan pelanggan, karena seringnya terjadi kesalahan *entry* dan kendala petugas pencatat meter tidak bisa membaca dari jarak dekat, karena terhalang pagar atau posisi KWH meter yang sulit untuk dijangkau.

Dengan melihat dan mengamati fenomena yang terjadi di atas tadi maka penulis berkeinginan dan berinisiatif "Bagaimana membuat sebuah alat PDE untuk mencatat data KWH meter digital pelanggan dari jarak jauh yaitu menggunakan infra merah dan mengirimkan data pada PC", sehingga dapat memudahkan petugas pembaca meter dalam mengambil data dari pelanggan.

KATA PENGANTAR

Alhamdulillah, puji syukur kehadirat-Mu Ya Allah yang telah memberikan rahmat dan hidayah-Nya, sehingga penyusun dapat menyelesaikan skripsi yang berjudul "Perancangan dan Pembuatan Alat *Portable Data Entry* untuk KWH Meter Digital Melalui Media Infra Merah yang Dapat Diakses pada PC" ini dengan lancar. Skripsi ini merupakan persyaratan kelulusan Studi di Jurusan Teknik Elektro S-1 Konsentrasi Teknik Elektronika ITN Malang dan untuk mencapai gelar Sarjana Teknik.

Keberhasilan peyelesaian laporan skripsi ini tidak lepas dari dukungan dan bantuan berbagai pihak. Untuk itu penyusun menyampaikan terima kasih kepada :

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4. Bapak petugas tera di PT. PLN yang telah membantu pengkalibrasian KWH meter digital.
5. Ayah dan Ibu serta saudara-saudara kami yang telah memberikan do'a restu, dorongan, semangat, dan biaya.
6. Semua yang telah membantu dalam penyelesaian penyusunan skripsi ini.

Penyusun telah berusaha semaksimal mungkin dan menyadari sepenuhnya akan keterbatasan pengetahuan dalam menyelasaikan laporan ini. Untuk itu

penyusun mengharapkan saran dan kritik yang membangun dari pembaca demi kesempurnaan laporan ini.

Harapan penyusun semoga laporan skripsi ini dapat memberikan manfaat bagi perkembangan ilmu pengetahuan dan pembaca.

Malang, Maret 2008

Penyusun

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BAB I

PENDAHULUAN

1.1. Latar Belakang

Pengukuran energi listrik dengan menggunakan alat KWH meter, digunakan oleh perusahaan penyelenggara jasa layanan pendistribusian energi listrik, seperti di PLN. Sampai saat ini, PLN dalam mengukur konsumsi energi listrik pada sebagian besar pelanggannya, masih menggunakan KWH meter analog atau disebut KWH meter elektromekanik.

Salah satu kelemahannya adalah dalam pembacaan hasil pengukuran energi, karena petugas pembaca meter harus mendatangi satu per satu pada alat tersebut, dan mencatatnya secara manual. Hal ini akan berdampak pada pelayanan pelanggan, karena seringnya terjadi kesalahan *entry* dan kendala petugas pencatat meter tidak bisa membaca dari jarak dekat, karena terhalang pagar atau posisi KWH meter yang sulit untuk dijangkau.

Sistem pembacaan jauh elektronik (SPJ-e) merupakan salah satu solusi terhadap permasalahan tersebut, sehingga disamping akan memudahkan petugas dalam pembacaaan alat ini juga bisa mengurangi kesalahan *entry*.

Dengan melihat dan mengamati fenomena yang terjadi di atas maka penyusun berkeinginan, "bagaimana membuat alat yang dapat memudahkan petugas pembaca meter?", dalam hal ini penyusun akan merancang sebuah alat yang bisa mencatat data KWH meter dari jarak jauh dengan menggunakan media infra merah dan mengirimkan data pada PC *server*. Selain itu perancangan ini

merupakan salah satu cara untuk mengantisipasi adanya manipulasi biaya pemakaian energi listrik yang dapat merugikan pelanggan PLN.

1.2. Tujuan

Tujuan dari penulisan skripsi ini adalah :

Membuat alat *Portable Data Entry* untuk KWH meter digital dengan menggunakan media infra merah yang dapat diakses pada PC secara serial.

1.3. Rumusan Masalah

Melihat dari apa yang telah dijabarkan pada latar belakang, maka dapat dibuat rumusan masalah sebagai berikut :

1. Bagaimana merancang dan membuat alat PDE (*portable data entry)* yang bisa digunakan untuk mengambil data pemakaian energi listrik pada kwh meter digital ?
2. Bagaimana cara pengambilan data dengan menggunakan PDE (*portable data entry)* yang kemudian di*upload*kan pada PC ?

1.4. Batasan Masalah

Untuk menjaga konsistensi dan agar cakupan pembahasan dari perancangan dan pembuatan alat ini tidak terlalu meluas maka penyusun perlu membuat batasan-batasan masalah yang meliputi :

1. Alat ini dirancang untuk digunakan pada KWH meter 1 fasa pada rumah tangga dengan daya 450 VA.
2. Dalam perancangan alat ini akan dibahas tentang perangkat keras (*hardware*), sedangkan untuk perangkat lunaknya (*software*) dibahas secara garis besarnya saja.
3. Hanya membahas tentang PDE (*portable data entry)* dan proses pengambilan data pada KWH meter digital serta pengiriman data ke PC.
4. KWH meter digital yang digunakan hanya dibahas secara garis besarnya saja.
5. Tidak membahas catu daya.

1.5. Metodologi Penulisan

Beberapa metode yang penyusun gunakan dalam menyusun dan menganalisa laporan Tugas Akhir ini adalah :

1. Studi Literatur

   Dengan mencari referensi-referensi yang berhubungan dengan perencanaan dan pembuatan alat yang akan dibuat.

2. *Field Research*

   Dengan melakukan penelitian secara langsung mengenai objek-objek yang berhubungan langsung dengan perencanaan alat yang akan dibuat.

3. Perencanaan Dan Pembuatan Alat

   Dalam pembuatan alat ini menggunakan konsep sebagai berikut :

   - Perencanaan sistem secara keseluruhan (pembuatan blok diagram

sistem).

- Mendeskripsikan fungsi dari masing-masing blok diagram.
- Membuat perangkat keras *(hardware)* dan perangkat lunaknya *(software)*.

4. Pengujian Alat

   Dengan melakukan pengujian perblok rangkaian dan kerja seluruh sistem pada alat tersebut.

5. Penyusunan Laporan Skripsi

   Membuat laporan yang terdiri dari: Pendahuluan, Landasan Teori, Perencanaan dan Pembuatan Alat, Pengujian Alat dan Penutup.

1.6. Sistematika Pembahasan

Sistematika pembahasan dari skripsi ini terdiri dari pokok pembahasan yang saling berkaitan antara satu dengan lainnya, yaitu :

BAB I Pendahuluan

Memuat latar belakang, rumusan masalah, tujuan, batasan masalah, metodologi pembahasan, dan sistematika pembahasan.

BAB II Teori Penunjang

Membahas teori-teori yang mendukung dalam perencanaan dan pembuatan alat.

BAB III Perencanaan dan Pembuatan Alat

Perancangan dan perealisasian alat yang meliputi spesifikasi, perencanaan blok diagram, prinsip kerja dan realisasi alat.

BAB IV Pengujian Alat

Memuat hasil pengujian terhadap alat yang telah direalisasikan.

BAB V Kesimpulan dan Saran

Memuat kesimpulan dan saran-saran.

BAB II

TEORI PENUNJANG

Untuk memudahkan dalam memahami cara kerja rangkaian maupun dasar-dasar pembuatan alat PDE (*Portable Data Entry*), maka perlu penjelasan dan uraian teori penunjang yang digunakan dalam tugas akhir ini.

Teori-teori penunjang yang dijelaskan dalam bab ini meliputi:

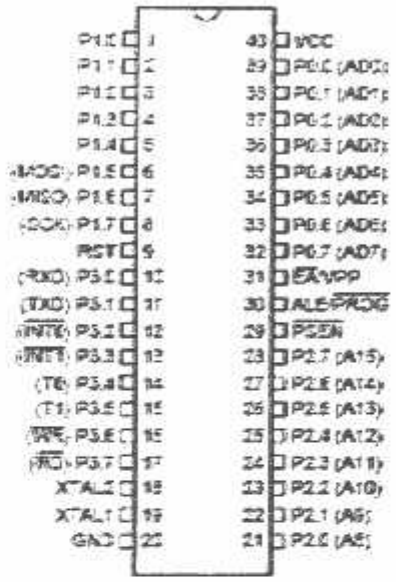
1. Mikrokontroler AT89S51
2. LCD M1632
3. Memori AT24C64
4. Standar RS232
5. Komunikasi Infra Merah
6. KWH Meter Digital (secara garis besarnya saja)

2.1. Mikrokontroler AT89S51

Mikrokontroler AT89S51 adalah mikrokontroler CMOS 8 bit keluaran Atmel dengan 4K *bytes Flash* PEROM (*Programmable and Eraseable Read Only Memory*). Memori ini digunakan untuk menyimpan perintah (instruksi) berstandar MCS-51, sehingga memungkinkan mikrokontroler ini untuk bekerja dalam mode *single chip operation* (mode operasi keping tunggal) yang tidak memerlukan *external memory* (memori luar) untuk menyimpan *source code* tersebut.

2.1.1. Arsitektur Mikrokontroler AT89S51

Gambar 2-1 di bawah ini merupakan susunan pin dari mikrokontroler AT89S51:



Gambar 2-1
Susunan Pin AT89S51

Secara fisik, mikrokontroler AT89S51 mempunyai 40 pin, 32 pin di antaranya adalah pin untuk keperluan *port* masukan/keluaran. Satu *port* paralel terdiri dari 8 pin, dengan demikian 32 pin tersebut membentuk 4 buah *port* paralel, yang masing-masing dikenal dengan *Port* 0, *Port* 1, *Port* 2 *dan Port* 3.

Berikut penjelasan dari masing-masing pin yang digunakan dalam perancangan PDE:

- Pin 1 sampai 4 (P1.0 - P1.3)

  Pin 1 sampai 4 dihubungkan dengan *push button* sebagai masukan pada mikrokontroler.

- Pin 9 (Reset)

  Pin 9 Merupakan masukan reset bagi mikrokontroler. Reset akan aktif dengan memberikan input *high* selama 2 *machine cycle*. Reset pada mikrokontroler merupakan masukan aktif *high* '1'. Pulsa transisi dari rendah '0' ke tinggi '1' akan mereset mikrokontroler menuju alamat 0000H. Pin reset dihubungkan dengan rangkaian *power-on reset*.

- Pin 10 (RXD) dan 11 (TXD)

  Pin pada *port* 3 merupakan saluran I/O 8 bit dua arah dengan *internal pullup*. Di samping sebagai saluran I/O, *port* ini memiliki fungsi pengganti seperti terlihat pada tabel 2-1. Bila fungsi pengganti tidak dipakai maka dapat digunakan sebagai *port* paralel 8 bit serbaguna

Tabel 2-1 Fungsi Alternatif *Port*

Bit	Nama	Fungsi Alternatif
P3.0	RXD	Untuk menerima data *port* serial
P3.1	TXD	Untuk mengirim data *port* serial
P3.2	INT0	Interupsi *external* 0
P3.3	INT1	Interupsi *external* 1
P3.4	T0	Input *external* Pewaktu/Pencacah 0
P3.5	T1	Input *external* Pewaktu/Pencacah 1
P3.6	WR	Jalur menulis memori data *external*
P3.7	RD	Jalur membaca memori data *external*

- Pin 18 (XTAL2) dan 19 (XTAL1)

  Pin 18 dan 19 merupakan masukan untuk rangkaian osilasi mikrokontroler. Kecepatan proses pengolahan data dari mikrokontroler ditentukan oleh *clock* yang dirangkai pada mikrokontroler, karena kristal yang

digunakan mempunyai frekuensi sebesar 11,0592 MHz maka untuk satu periode membutuhkan waktu sebesar:

$$Tosc = \frac{1}{f_{osc}}$$

$$= \frac{1}{11{,}0592\,MHz} S$$

$$= 9{,}042 \times 10^{-8}\ S$$

- Pin 20 (GND)

  Pin 20 merupakan *ground* dari sumber tegangan.

- Pin 21 (P2.0) dan 22 (P2.1)

  Pin 21 dan 22 merupakan saluran I/O dua arah dengan *internal pullup*. Dalam perancangan P2.0 dan P2.1 digunakan sebagai jalur untuk mengakses memori eksternal.

- Pin 28 (P2.7)

  Pada perancangan, pin ini digunakan sebagai lampu indikator.

- Pin 31 ($\overline{EA}$/VPP)

  Pada kondisi *low*, pin ini akan berfungsi sebagai *External Access Enable* ($\overline{EA}$) yaitu mikrokontroler akan menjalankan program yang ada pada memori *external*. Jika berkondisi *high*, pin ini akan berfungsi untuk menjalankan program yang ada pada memori *internal*. Pin ini juga berfungsi sebagai masukan tegangan pemrograman selama proses pemrograman.

- Pin 32 sampai 39 (P0.7 - P0.0)

  Pin 32 sampai 39 ialah *Port* 0 yang merupakan saluran I/O 8 bit *open collector* dan dapat juga digunakan sebagai multipleks bus alamat rendah dan bus data selama adanya akses ke memori program *external*. Pada perancangan ini, *port* 0 dihubungkan dengan LCD sebagai tampilan.

- Pin 40 (VCC)

  Pin 40 merupakan masukan sumber tegangan positif bagi mikrokontroler sebesar 5V.

2.1.2. Struktur Memori AT89S51

AT89S51 mempunyai struktur memori yang terdiri atas:

- RAM *internal*, memori sebesar 128 *bytes* yang digunakan untuk menyimpan variabel atau data yang bersifat sementara.
- *Special Function Register* (Register Fungsi Khusus), memori yang berisi register-register yang mempunyai fungsi-fungsi khusus yang disediakan oleh mikrokontroler seperti *timer*, *serial port* dan lain-lain.
- *Flash* PEROM, memori yang digunakan untuk menyimpan instruksi-instruksi MCS-51 sebesar 4K*bytes*.

2.2. LCD (*Liquid Crystal Display*) M1632

LCD *(Liquid Crystal Display)* banyak digunakan pada alat–alat elektronika yang memerlukan penampil, sehingga pemakai dapat mengerti dengan informasi yang ditampilkan oleh alat. Keunggulan dari LCD adalah bentuknya yang kecil

dan dapat menampilkan karakter ASCII pada tampilannya juga membutuhkan daya yang kecil, schingga sangat praktis apabila digunakan pada peralatan yang hemat daya.

2.2.1. Deskripsi M1632

LCD (liquid Crystal Display) adalah suatu jenis piranti *output* yang menggunakan daya rendah dengan pengontrol kontras dan kecerahan. Pengontrol utamanya dan karakter ada pada ROM generator (CGROM) dan *display* data RAM (DDRAM) yang akan menghasilkan *extended key codes* (kode tombol / *keyboard* standar internasional dalam Hexa) jika diberikan masukan. Untuk mendapatkan fungsi dengan baik maka perlu diperhatikan proses inisialisasi yang telah ditentukan oleh pabrik pembuatnya.

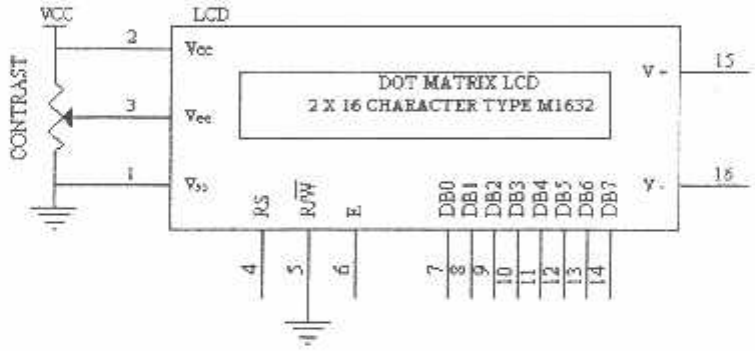
Ada dua jenis register yang terdapat dalam LCD M1632 ini, yaitu data register dan instruksi register. Dengan menggunakan pin RS (*Register Select*) pada LCD, pemakaian kedua register dapat dipilih. Pemilihan register dapat dipilih pada LCD, ditunjukkan dalam tabel berikut ini :

Tabel 2-2 Pemilihan Register Pada LCD M1632

Nama Sinyal	No. Terminal	I/O	Tujuan	Keterangan Sinyal
RS	4	*Input*	MPU	0 : *Instruction Register* 1 : Data Register

Jika bagian yang dipilih adalah instruksi register maka *output* yang dihasilkan adalah meliputi operasional dari LCD, misalnya fungsi *display clear, cursor home, entry mode set, display on/off, cursor shift*, dan sejenisnya. Sebaliknya, jika bagian yang dipilih adalah data register, *output* yang dihasilkan adalah meliputi karakter yang tabelnya terdapat pada lampiran data sheet LCD.

Berikut adalah gambar dari LCD dengan pin-pin yang terhubung dengan mikrokontroler AT89S51:



Gambar 2-2

Modul LCD 2 ×16 karakter

LCD M1632 mempunyai spesifikasi sebagai berikut :

- 16 karakter 2 baris dalam bentuk dot matrik 5 × 7 dan kursor.
- *Duty ratio* 1/16.
- Memiliki ROM pembangkit karakter untuk 192 jenis karakter.
- RAM untuk data *display* sebanyak 80 × 8 bit (80 karakter maksimum).
- Dapat dirangkai dengan MPU (*Mikroprocessor Unit*) 8 bit atau 4 bit.
- RAM data *display* dan RAM pembangkit karakter dibaca oleh MPU.

- Memiliki fungsi intruksi : *display ON/OFF, cursor ON/OFF, display character blink, cursor shift dan display shift.*
- Memiliki rangkaian *oscillator* sendiri.
- Sumber tegangan tunggal +5 volt.
- Memiliki rangkaian reset otomatis pada catu daya dihidupkan.
- Suhu operasi 0^{o}-50^{o} C.

LCD modul M1632 mempunyai 16 pin dengan fungsi sebagai berikut :

Tabel 2-3 Fungsi Pin – Pin LCD

No. PIN	Nama PIN	Fungsi
1	Vss	*Terminal Ground*
2	Vcc	Tegangan Catu + 5 volt
3	Vee	Mengendalikan kecerahan LCD
4	RS	Sinyal pemilihan register 0 = *Instruction Register* 1 = Data Register
5	$R/\overline{W}$	Sinyal seleksi tulis atau baca 0 = Tulis 1 = Baca
6	E	Sinyal operasi awal yang mengaktifkan data tulis atau baca
7 – 14	DB0 – DB7	Merupakan saluran data berisi perintah data yang akan ditampilkan
15	V + BL	Back Light Supply
16	V – BL	Back Ligth Supply (Ground)

2.2.2 Sinyal *Interface* M1632

Untuk berhubungan dengan mikrokontroler pemakai M1632 dilengkapi dengan 8 jalur pada data (DB0....DB7) yang dipakai untuk menyalurkan kode ASCII maupun perintah pengatur kerja M1632. Selain itu dilengkapi pula dengan E, R/$\overline{W}$, RS seperti layaknya komponen yang *compatibel* dengan mikrokontroler. Kombinasi sinyal E dan R/$\overline{W}$ merupakan sinyal standar pada komponen buatan *Motorolla*. Sebaliknya sinyal-sinyal dari mikrokontroler merupakan sinyal khas *Intel* dengan kombinasi sinyal WR dan RD. RS singkatan dari *register Select*, dipakai untuk membedakan jenis data yang dikirim ke M1632. Jika RS = 0 maka data yang dikirim adalah perintah untuk mengatur kerja M1632. Sebaliknya jika RS = 1 maka data yang dikirim oleh kode ASCII yang ditampilkan. Demikian pula saat pengambilan data, saat RS = 0, data yang diambil dari M1632 merupakan data status yang mewakili aktivitas M1632. Saat RS = 1, maka data yang diambil merupakan kode ASCII dari data yang ditampilkan.

Proses mengirim atau mengambil data dari atau ke M1632 adalah sebagai berikut:

1. **RS** harus dipersiapkan dulu, untuk menentukan jenis data seperti yang telah dibicarakan di atas.
2. **R/$\overline{W}$** di-nol-kan untuk menandakan akan diadakan pengiriman data ke M1632. Data yang akan dikirim disiapkan di **DB0..DB7**, sesaat kemudian sinyal E di-satu-kan dan di-nol-kan kembali. Sinyal **E** merupakan sinyal sinkronisasi, saat **E** berubah dari 1 menjadi 0 data di **DB0 .. DB7** diterima oleh M1632.

3. Untuk mengambil data dari M1632 sinyal **R/$\overline{W}$** di-satu-kan, menyusul sinyal **E** di-satu-kan. Pada saat **E** menjadi 1, M1632 akan meletakkan datanya di **DB0 .. DB7**, data ini harus diambil sebelum sinyal **E** di-nol-kan kembali.

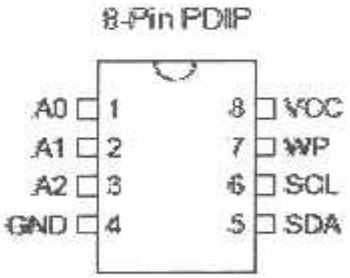
2.3. Memori AT24C64

Fasilitas dan keistimewaan dari AT24C64 berkaki 8 pin adalah:

- *2-Wire Serial Interface*
- *Low-Power Devices* (ISB = **25 mA** @,5V)
- *High Reliability: – Endurance:* 1 *Million Write Cycles*

  – Data Retention: 100 *Years*

AT24C64 mempunyai 1 jalur WP (*Write Protect*), 1 jalur SCL (*Serial Clock*), 1 jalur SDA (*Serial Data*), dan 3 pin jalur alamat. Gambar 2-3 menunjukkan susunan pin yang dimiliki oleh AT24C64:



Gambar 2-3
Susunan Pin AT24C64

2.4. Standar RS-232

Secara umum, RS-232 didefinisikan sebagai antar muka antara peralatan terminal data dengan peralatan komunikasi data menggunakan data biner secara secara serial. Pada prinsipnya proses transfer data dengan menggunakan *serial interface* ini sangat sederhana. Komunikasi serial merupakan komunikasi data dengan pengiriman data secara satu per satu dengan menggunakan satu jalur kabel data. Sehingga komunikasi serial hanya menggunakan 2 kabel data yaitu kabel data untuk pengiriman yang disebut *transmite* (Tx) dan kabel data untuk penerimaan yang disebut *receive* (Rx). Kelebihan dari komunikasi serial adalah jarak pengiriman dan penerimaan dapat dilakukan dalam jarak yang cukup jauh dibandingan dengan komunikasi *parallel* tetapi kekurangannya adalah kecepatan lebih lambat daripada komunikasi *parallel*.

Jenis data yang yang akan ditransfer adalah dalam bentuk biner. Dalam merancang sistem komunikasi serial, *hand-shake* disempurnakan dengan menambahkan karakter pengendali dalam deretan data yang dikirim yang biasa disebut sebagai *start* bit atau *stop* bit.

Kabel RS-232 biasanya terdiri dari 4, 9, atau 25 pin. Kabel 25 pin menghubungkan setiap pin, sedangkan kabel 4 pin merupakan hubungan yang minimum.

Tabel 2-4 Fungsi pin-pin RS-232

D-Type-25 pin NO.	D-Type-9 pin No.	Abbreviation	Full Name
Pin2	Pin3	TD	Transmit Data
Pin3	Pin2	RD	Receive Data
Pin4	Pin7	RTS	Request To Send
Pin5	Pin8	CST	Clear To Send
Pin6	Pin6	DSR	Data Set Ready
Pin7	Pin5	SG	Signal Ground
Pin8	Pin 1	CD	Carrier Detect
Pin20	Pin4	DTR	Data Terminal Ready
Pin 22	Pin9	RI	Ring Indicator

2.4.1. Spesifikasi RS- 232

Spesifikasi antar muka RS-232 akan dijelaskan berikut ini. Pada sinyal yang dikirim, level tegangannya adalah +5 Vdc sampai +15 Vdc untuk biner '0' dan -5 Vdc sampai -15 Vdc untuk biner '1'. Sedangkan untuk data yang diterima, level tegangannya adalah +3 Vdc sampai +13 Vdc untuk biner '0' dan -3 Vdc sampai -13 Vdc untuk biner '1'. Kecepatan pengiriman data yaitu 50 bps sampai 19200 bps (*bit per second* atau bit per detik). Sedangkan untuk membangkitkan *baudrate* yang diinginkan, maka timer 1 dapat dicari dengan menggunakan persamaan berikut:

$$TH1 = 256 - \frac{2^{SMOD} \times F_{osc}}{12 \times 32 \times Baudrate}$$

2.5. Komunikasi Infra Merah

Komunikasi infra merah dilakukan dengan menggunakan dioda infra merah sebagai pemancar dan modul penerima infra merah sebagai penerimanya. Untuk jarak yang cukup jauh, yaitu kurang lebih tiga sampai lima meter. Pancaran data infra merah harus dimodulasikan terlebih dahulu untuk menghindari kerusakan data akibat *noise*.

Proses modulasi dilakukan dengan mengubah kondisi logika '0' dan '1' menjadi kondisi ada dan tidak ada sinyal *carrier* infra merah yang berkisar antara 30 KHz sampai 50 KHz.

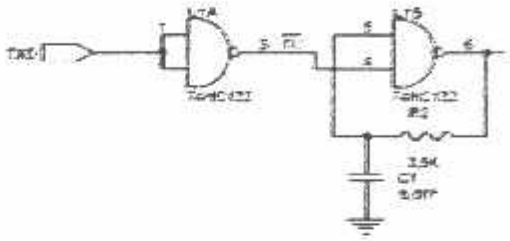
Gambar 2-4
Modulasi Sinyal Infra Merah

2.5.1. Bagian Pemancar

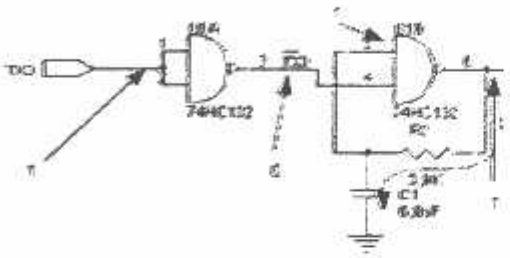
Pemancar terdiri dari bagian modulator, bagian penguat dan diode infra merah.

Gambar 2-5
Blok Diagram Pemancar

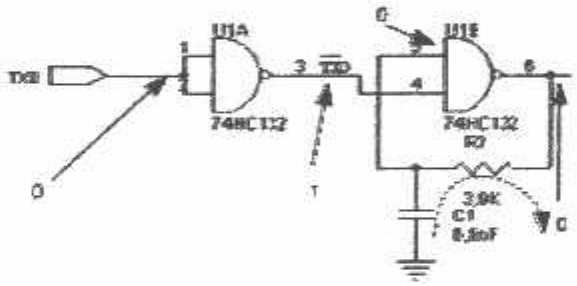
Proses modulasi dilakukan dengan mencampur sinyal *carrier* infra merah dengan sinyal data yang diperoleh dari *port* serial DST-51. Rangkaian **Modulator** yang terdiri dari sebuah gerbang dan rangkaian **R-C** sebagai ***oscillator***.



Gambar 2-6a Rangkaian Modulator



Gambar 2-6b Saat Data Logika 1 atau *Idle*



Gambar 2-6c Saat Data Logika 0

Gerbang tersebut menggunakan IC 74HC132 di mana pada saat pin TXD berkondisi logika '1' maka *output* dari IC ini sesuai dengan tabel kebenaran yang ada pada *datasheet* adalah logika '1'. Namun bila sebaliknya TXD berkondisi logika '0' maka sesaat *output* dari IC ini (pin 6) berubah ke logika '0', sehingga kapasitor C1 akan membuang muatannya melalui R2. Bila tegangan C1 terbuang hingga di bawah **tegangan ambang** 74HC132 maka *input* pin nomor 5 dari IC ini akan dianggap berkondisi logika '0' sehingga outputnya (pin 6) berubah menjadi logika '1'.

Arus akan mengalir dari pin 6 menuju ke C1 melalui R1 hingga tegangan pada kapasitor ini melebihi tegangan ambang dan input pin nomor 5 dianggap berkondisi logika '1' (gambar 2-6b). Bila pada saat itu TXD masih berkondisi *high* maka *output* dari gerbang ini yaitu pin nomor 6 akan berkondisi *low* dan C1 akan membuang muatannya melalui R1 sehingga tegangan pada pin 5 berada di bawah tegangan ambang atau berlogika '0' (gambar 2-6c). *Output* pada pin 6 kembali berlogika '1' dan arus mengalir lagi mengisi C1 melalui R1.

Proses pembuangan dan pengisian kapasitor C1 ini menyebabkan adanya osilasi pada pin 6 IC 74HC132 sehingga terbentuk sinyal *carrier* dengan frekuensi yang dapat dihitung dengan menggunakan rumus berikut:

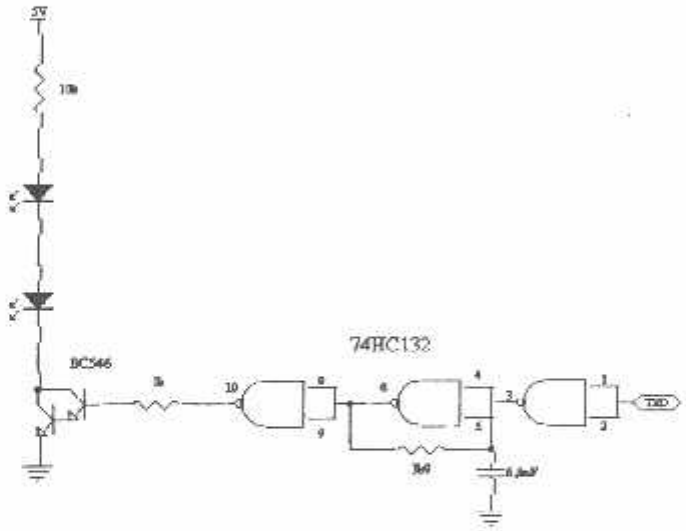
$$T = 2RC\left[\ln\left[\frac{Vs - VT-}{Vs}\right] - \ln\left[\frac{Vs - VT+}{Vs}\right]\right]$$

$$F = \frac{1}{T}$$

Jadi pada intinya apabila input TXD berkondisi *high* maka frekuensi *carrier* yang terjadi pada pin nomor 4 akan dilewatkan ke *output*nya dengan frekuensi yang sama persis, namun bila TXD berkondisi *low* maka osilasi pada pin nomor 4 akan berhenti dan output dari gerbang adalah *high*.

Ayunan sinyal ini diperkuat lagi oleh gerbang lain dari 74HC132 yang dibentuk menjadi *inverter* dan diteruskan ke transistor BC546 yang mengalirkan sinyal-sinyal frekuensi hasil dari *modulator* tersebut ke diode Infra merah. Diode infra merah membutuhkan arus kurang lebih 100 mA dan tegangan kurang lebih 2 Volt untuk memancarkan sinar secara maksimum.

Output dari IC 74HC132 yang hanya mengeluarkan arus maksimal 4mA tentu saja tidak cukup kuat untuk mengendalikan LED tersebut. Transistor BC546 adalah sebuah transistor dengan konfigurasi *darlington* dan penguatan minimal 100 x (HFE). Oleh karena itu, untuk membangkitkan arus kolektor sebesar 100 mA, maka hanya dibutuhkan arus sebesar 1 mA saja pada basis. Output 74HC132 yang dapat mengeluarkan arus 4 mA dapat dihubungkan ke transistor tersebut melalui resistor R3.



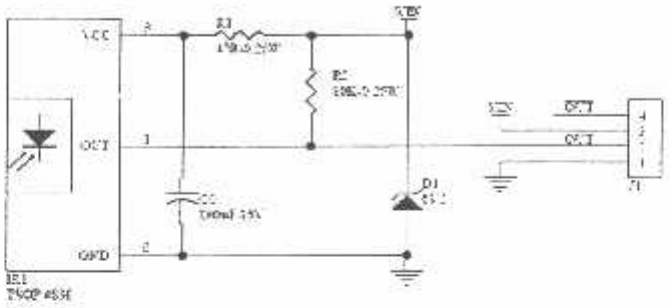
Gambar 2-7
Bagian Penguat Infra Merah

Osilasi yang telah dikuatkan oleh bagian penguat ini akan mengakibatkan adanya pancaran sinyal infra merah dengan frekuensi seperti pada gambar 2-7.

2.5.2. Bagian Penerima

Bagian Penerima seperti yang telah disebutkan sebelumnya, adalah merupakan modul penerima infra merah yang terdiri dari *photo diode* yang sudah dilengkapi dengan rangkaian *hand pass filter* yang hanya melewatkan frekuensi

antara 30 KHz sampai 50 KHz saja. Bagian penerima menggunakan modul DT I/O *reciver infra red* seperti pada gambar di bawah:



Gambar 2-8
Modul Penerima Infra Merah

Output dari modul ini berupa logika '0' dan '1' sehingga dapat langsung dihubungkan ke DST-51 di bagian pemancar. Frekuensi 47,13 KHz yang diterima dari pancaran diode infra merah diubah menjadi logika '0' dan tidak adanya frekuensi sebagai logika '1' seperti pada timing diagram berikut.

Gambar 2-9
Timing Diagram Penerima

Dengan adanya rangkaian pemancar dan penerima ini, maka kondisi logika '0' dan '1' pada pin TXD akan diterima pada pin RXD dengan kondisi yang sama pula, sehingga proses transmisi data secara serial dapat terjadi.

- **Komunikasi Data**

  Komunikasi data serial antara sebuah pemancar dan sebuah penerima pada

media infra merah, hanya menggunakan satu jalur saja yaitu jalur data tanpa memerlukan sinyal *clock* sebagai *sinkronisasi*. Oleh karena itu transmisi serial harus dilakukan secara asinkron di mana setiap paket data harus diawali dengan *start bit* ('0') dan diakhiri dengan *stop bit* ('1').

Komunikasi serial *asinkron* pada AT89S51 terjadi dengan mengirimkan *start bit*, LSB terlebih dahulu dan diakhiri dengan MSB lalu *stop bit*.

Sebelum proses pengiriman dan penerimaan data dilakukan, maka ada beberapa register yang mengatur proses komunikasi serial pada AT89S51 yang harus diinisial agar komunikasi asinkron dengan *baudrate* 600 bps dapat dilakukan.

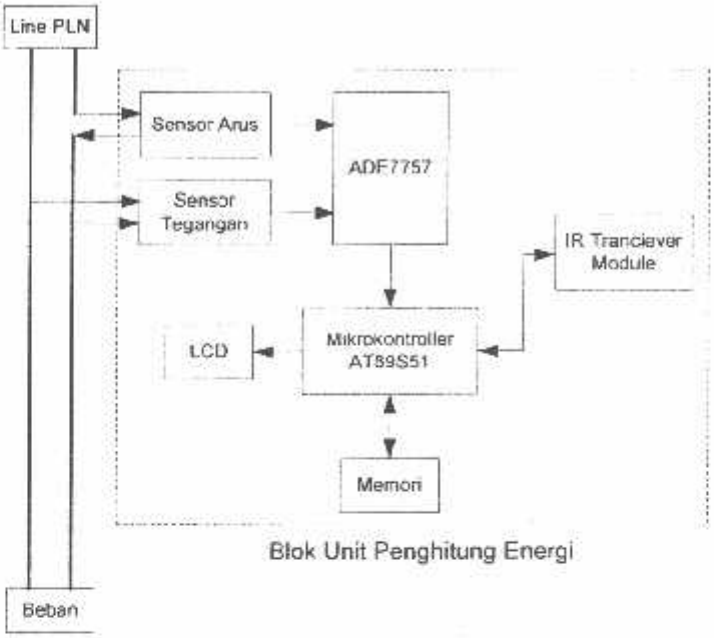
Untuk mengatur *baudrate* dari port serial AT89S51 maka Timer 1 dari AT89S51 diatur sebagai mode 8 *bit auto reload* di mana timer tersebut akan digunakan sebagai *pre scaler* dari *baudrate*.

Sedangkan untuk membangkitkan *baudrate*, maka dapat dicari dengan menggunakan persamaan berikut:

$$TH1 = 256 - \frac{F_{osc}}{12x32xBaudrate}$$

2.6. KWH Meter Digital

Perancangan KWH meter digital dapat ditunjukkan pada diagram blok berikut:



Gambar 2-10

Diagram Blok KWH Meter Digital

- **Sensor Arus**

Pada perancangan sensor arus yang digunakan adalah berupa kawat tembaga. Pada *datasheet* IC ADE7757, kawat tembaga yang dipakai harus memiliki nilai tahanan sebesar 350 μΩ. Untuk menentukan berapa panjang kawat yang dibutuhkan dengan menentukan diameter kawat sebesar 1,7 mm dan $\rho_{tembaga}$ sebesar 16,8 μΩmm, maka digunakan persamaan sebagai berikut:

$$R = \rho \frac{\ell}{A}$$

$$350x10^{-6} = 16,8x10^{-6} \times \frac{\ell}{3,14x0,85^2}$$

$$\ell = 47,3 \text{ mm}$$

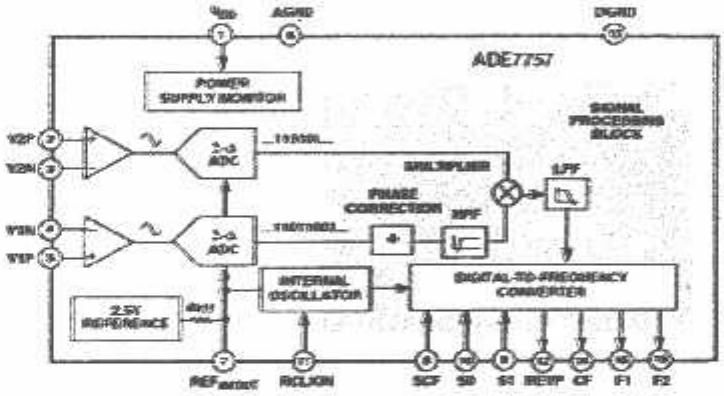
R : Tahanan, ρ : Tahanan Jenis, ℓ : Panjang kawat, A : Luas penampang kawat

- **Sensor Tegangan**

Pada perancangan, sensor tegangan menggunakan rangkaian pembagi tegangan dengan tegangan masukan maksimal 165 mV.

- **IC ADE7757**

IC ini digunakan untuk memproses pemakaian energi dengan masukan dari sensor arus dan tegangan, seperti pada gambar diagram blok di bawah ini:



Gambar 2-11
Diagram Blok IC ADE7757

Sinyal keluaran dari IC ADE7757 yang menjadi masukan bagi mikrokontroler adalah pada pin F1 yang berupa pulsa dengan kalibrasi 100 pulsa per kWh, sehingga untuk 1 pulsa sama dengan 0,01 kWh.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BAB III

PERENCANAAN DAN PEMBUATAN ALAT

3.1. Pendahuluan

Dalam bab ini akan dibahas mengenai perencanaan dan pembuatan alat PDE (*Portable Data Entry*) untuk KWH meter digital melalui media infra merah yang dapat diakses pada PC. Pembahasan akan dilakukan pada setiap blok rangkaian, terdiri atas pemilihan komponen, cara kerja masing - masing blok rangkaian, perhitungan dan fungsi masing - masing blok rangkaian tersebut. Secara garis besar terdapat dua bagian perangkat yang ada, yaitu :

- Perencanaan perangkat keras (*Hardware*)
- Perencanaan perangkat lunak (*Software*)

Pada perencanaan perangkat keras meliputi seluruh *peripheral* yang digunakan pada sistem ini. Sedangkan pada perencanaan perangkat lunak meliputi *flowchart* dan *software* secara umum. Akan tetapi kedua perangkat tersebut dalam kerjanya akan saling menunjang satu sama lain.

3.2. Perancangan Perangkat Keras (*Hardware*)

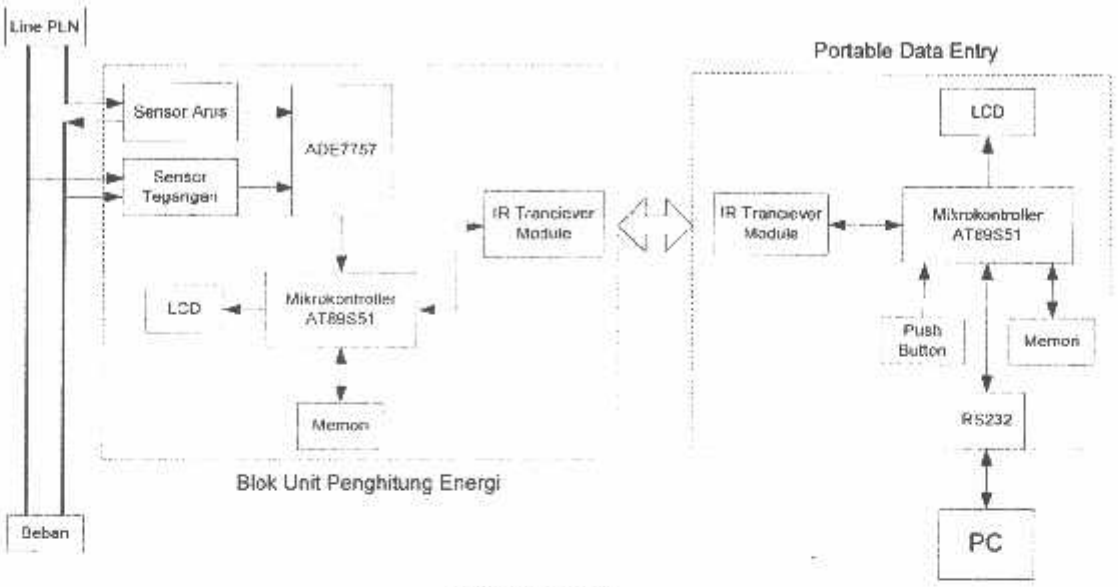
3.2.1. Spesifikasi Alat

Spesifikasi "perencanaan dan pembuatan alat PDE (*Portable Data Entry*) untuk KWH meter digital melalui media infra merah yang dapat diakses pada PC" yang dirancang adalah sebagai berikut:

1. Alat ini menggunakan sistem minimum mikrokontroler AT89S51 sebagai pengontrol utama dan EEPROM AT24C64 sebagai memori eksternal.
2. Menggunakan infra merah, sebagai media untuk pengambilan data pada KWH meter digital yang berupa nomor pelanggan dan jumlah pemakaian energi.
3. Menggunakan LCD sebagai tampilan.
4. Menggunakan *push button* untuk menjalankan proses pengambilan data dari KWH meter digital dan pengiriman data pada PC serta untuk menghapus memori pada KWH meter digital dan PDE.
5. Komunikasi PDE dengan PC menggunakan komunikasi serial RS232.

3.2.2. Blok Diagram Keseluruhan Alat

Perancangan dan pembuatan PDE agar dapat dilakukan secara sistematis dan terstruktur maka perlu dibuat blok diagram yang menjelaskan dari sistem yang dirancang. Secara garis besar sistem perancangan ditunjukkan pada blok diagram dari Gambar 3-1.



Gambar 3-1

Blok Diagram Keseluruhan Sistem

Keterangan fungsi dari masing-masing blok diagram pada blok PDE di atas adalah sebagai berikut :

1. Mikrokontroler AT89S51

   Berfungsi sebagai unit pemroses data dari *push button*, infra merah, dan pada saat meng*upload* data ke PC serta mengendalikan mekanisme kerja seluruh sistem.

2. EEPROM AT24C64

   Berfungsi sebagai unit penyimpan data.

3. Infra merah

   Berfungsi sebagai komunikasi antara PDE dengan KWH meter digital.

4. LCD (*Liquid Crystal Display*)

   Berfungsi untuk menampilkan informasi data tentang berapa pemakaian energi listrik, nomor pelanggan, *load Ok, Memori Full* dan sebagainya.

5. RS232

   Berfungsi sebagai komunikasi serial antara PDE dengan PC.

6. *Push Button*

   Berfungsi untuk menjalankan proses pengambilan data dari KWH meter digital dan pengiriman data pada PC serta untuk menghapus memori pada KWH meter digital dan PDE.

7. PC (*Personal Computer*)

   Berfungsi sebagai pengolah data pelanggan listrik untuk menampilkan berapa pemakaian energi listrik dan nomor pelanggan.

8. Blok unit penghitung energi

   Berfungsi untuk mengukur jumlah pemakaian energi pelanggan listrik dan sebagai obyek dalam pengambilan data dengan menggunakan PDE.

3.2.3. Prinsip Kerja PDE

Alat ini digunakan untuk pengambilan data yang berupa jumlah pemakaian daya dan nomor pelanggan dari KWH meter digital. Alat ini bekerja sesuai dengan fungsi dari masing-masing tombol. Adapun fungsi dari masing-masing tombol adalah sebagai berikut:

1. Tombol 4

   Tombol ini berfungsi untuk mengambil data dari KWH meter. Prinsip kerjanya adalah, pada saat tombol 4 ditekan, mikrokontroler AT89S51 memberikan perintah pada KWH meter digital untuk mengirimkan data

pada PDE, lalu data tersebut disimpan pada EEPROM dan ditampilkan pada LCD.

2. Tombol 3

   Tombol ini berfungsi untuk mengirimkan data dari PDE ke PC secara *serial*. Prinsip kerjanya adalah, pada saat tombol 3 ditekan maka PDE dalam kondisi *standby*, menunggu perintah dari PC untuk melanjutkan proses pengiriman data.

3. Tombol 2

   Tombol ini mempunyai 2 fungsi:

   - Pada saat mode normal tombol ini berfungsi untuk mereset KWH meter digital.
   - Juga bisa berfungsi sebagai tombol *exit* dan kembali pada mode normal.

4. Tombol 1

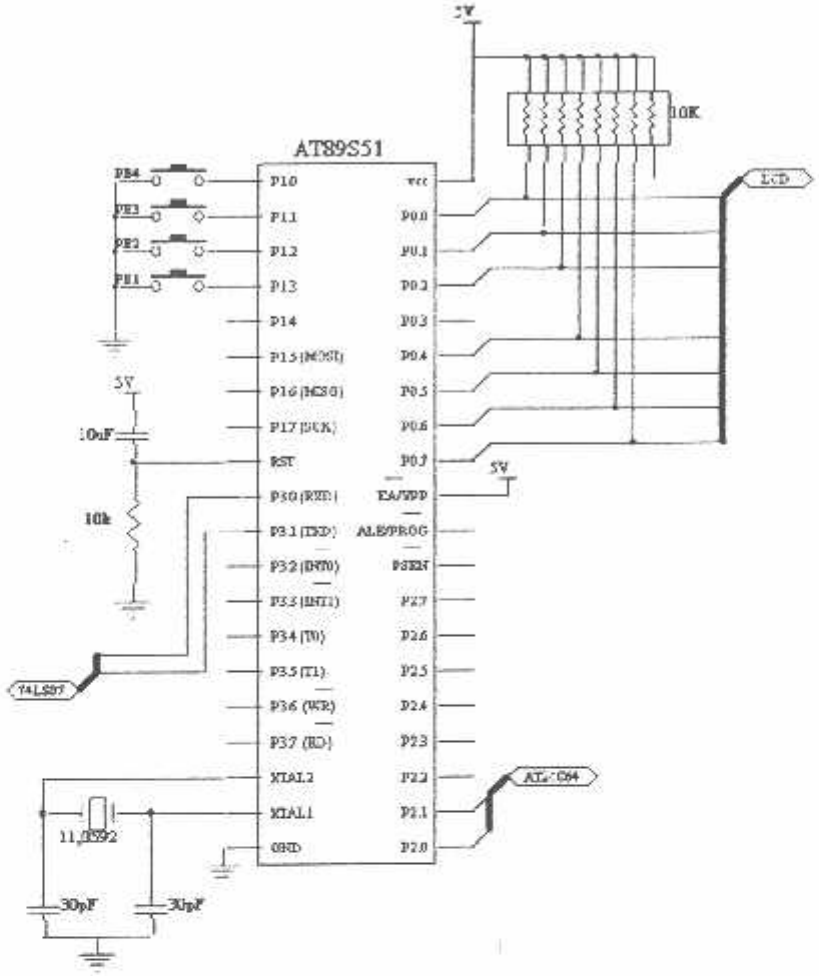
   Tombol ini berfungsi untuk mereset data pada EEPROM. Bila tombol ditekan maka mikrokontroler akan menjadikan identitas data yang disimpan pada EEPROM menjadi '0'

3.2.4. Perancangan Mikrokontroler AT89S51 pada PDE

Dalam hal ini cara kerja mikrokontroler AT89S51 hampir sama dengan otak manusia, mikrokontroler akan mengendalikan seluruh rangkaian pada PDE. Agar dapat mengerjakan suatu perintah maka mikrokontroler harus diisi program terlebih dahulu.

Mikrokontroler AT89S51 memerlukan kristal dengan frekuensi 11,0592MHz dan dua buah kapasitor 33pF di pakai untuk melengkapi rangkaian *oscillator* pembentuk *clock* yang menentukan kecepatan kerja mikrokontroler. Kapasitor 10μF dan resistor 10KΩ dipakai untuk membentuk rangkaian *reset* dimana rangkaian ini pada saat pertama kali catu daya dihidupkan, akan me*reset* rangkaian mikrokontroler sehingga program dipastikan akan bekerja dari awal. Prinsip kerja rangkaian reset adalah proses pengisian kapasitor yang ditunda oleh sebuah resistor sehingga pada saat pengisian kapasitor akan terjadi proses keadaan dari tegangan rendah (*low*) ke tegangan tinggi (*high*), keadaan inilah yang akan mereset rangkaian mikrokontroler.

Port 0 mikrokontroler AT89S51 merupakan keluaran untuk alamat (*address* AD0-AD7) yang tidak mempunyai tahanan *pull-up*, seperti pada konstruksi *port-port* yang lain. Pada saat P0 di pakai sebagai *port output* tegangan pada kaki P0 tidak mungkin menjadi *high* (tegangan ambang), untuk mengatasi hal ini maka harus dipasangkan *R-Pack* seperti pada skema rangkaian mikrokontroler AT89S51 yang diperlihatkan pada gambar 3-2.



Gambar 3-2

Rangkaian Mikrokontroler AT89S51

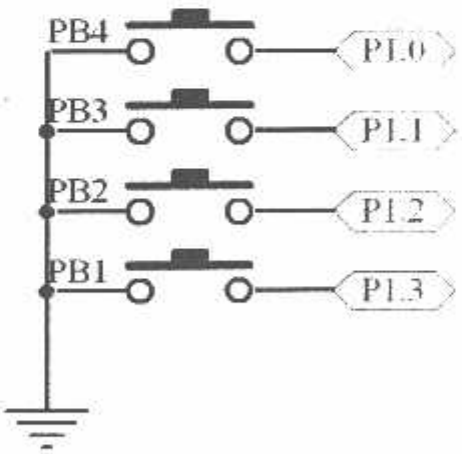
Agar sebuah mikrokontroler dapat bekerja sebagai pengontrol, maka kaki-kaki/*port* mikrokontroler dihubungkan dalam rangkaian-rangkaian eksternal. Dalam perancangan ini, *port* yang digunakan adalah sebagai berikut:

1. Pin 1 – 4 (P1.0 – P1.3) digunakan untuk *push button*.
2. Pin 9 digunakan untuk reset.
3. Pin 10 – 11 (P3.0 – P3.1) digunakan sebagai komunikasi serial pada PC dan komunikasi pada infra merah.

4. Pin 18 – 19 digunakan untuk XTAL2 dan XTAL1.
5. Pin 20 (GND) dihubungkan pada *ground*.
6. Pin 21 (P2.0) dihubungkan ke pin SDA pada EEPROM.
7. Pin 22 (P2.1) dihubungkan ke pin SCL pada EEPROM.
8. Pin 32 – 39 (P0.7 – P0.0) digunakan sebagai keluaran untuk LCD M1632.
9. Pin 31 (EA) dan 40 (VCC) dihubungkan pada tegangan +5V.

3.2.4.1. Perancangan Rangkaian *Push Button*

Dalam perancangan ini mikrokontroler AT89S51 telah diatur untuk mengirimkan data ke infra merah, meng*upload* data ke PC, mereset KWH meter digital dan mereset data pada PDE. Oleh karena itu, untuk melakukan proses pengiriman, pengambilan dan mereset data tersebut maka dibutuhkan *push button*. Perancangan *push button* seperti pada gambar 3-3 berikut:



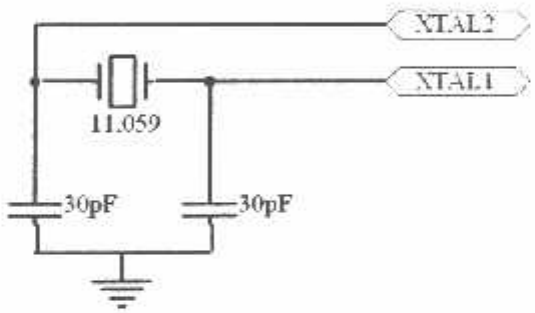
Gambar 3-3

Rangkaian *Push Button*

Jika tombol-tombol tersebut ditekan maka akan memberikan masukan *ground* pada mikrokontroler.

3.2.4.2. Perancangan Rangkaian *Clock*

Pada mikrokontroler AT89S51 terdapat *oscillator* sebagai pembangkit pulsa. Untuk mengaktifkan *Oscillator*, *port* XTAL1 dan XTAL2 harus dihubungkan ke sebuah *crystal* 11Mhz dan dua buah *ceramic capacitor* masing-masing 30pF atau sesuai dengan yang dispesifikasikan. Kecepatan proses pengolahan data dari mikrokontroler ditentukan oleh *clock* yang dirangkai pada mikrokontroler tersebut seperti pada gambar berikut:



Gambar 3-4
Rangkaian *Clock*

Untuk menghitung waktu T_{osc} dapat menggunakan persamaan sebagai berikut:

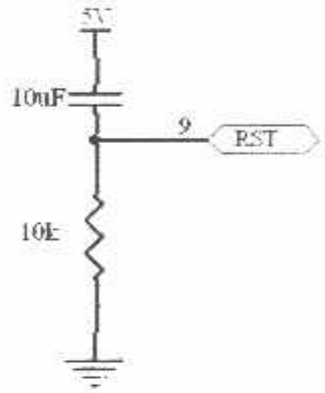
$$T_{osc} = \frac{1}{f_{osc}}$$

$$= \frac{1}{11{,}0592 \times 10^{6}}$$

$$= 9{,}042 \times 10^{-8}\,\mathrm{S}$$

3.2.4.3. Perancangan Rangkaian Reset

Pin reset pada mikrokontroler merupakan masukan aktif tinggi '1'. Pulsa transisi dari rendah '0' ke tinggi '1' akan mereset mikrokontroler menuju alamat 0000H. Pin reset dihubungkan dengan rangkaian *power on reset* yang diperlihatkan pada gambar 3-4 berikut ini :



Gambar 3-5

Rangkaian *Power On Reset* AT89S51

Sehingga waktu minimal logika tinggi yang dibutuhkan untuk mereset mikrokontroler adalah :

$$\text{Reset (min)} = T_{osc} \times \text{periode yang dibutuhkan}$$

$$= 9{,}042 \times 10^{-8} \times 24 = 2{,}170\ \mu s$$

Jadi mikrokontroler membutuhkan waktu minimal 2,170 μs untuk mereset. Waktu minimal inilah yang dijadikan pedoman untuk menentukan nilai R dan C. Dari persamaan konstanta waktu $\tau = R \times C$ (William H Hyat, 1998, h132 [1]) dan jika nilai R ditentukan sebesar 10 kΩ, maka nilai C adalah :

$$C = \frac{\tau}{R}$$

$$= \frac{2{,}170 \times 10^{-6}}{10 \times 10^{3}}$$

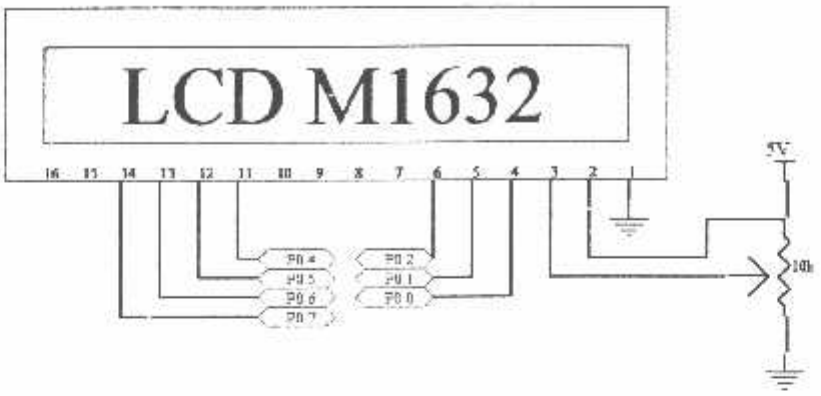
$$= 2{,}170 \times 10^{-12} \text{F}$$

Kapasitor minimal yang dibutuhkan adalah 2,170 pF. Dengan menggunakan kapasitor sebesar 10 μF, maka akan menjamin waktu reset di atas nilai minimal waktu yang dibutuhkan untuk mereset mikrokontroller.

3.2.5. Perancangan Rangkaian LCD (*Liquid Crystal Display*)

Sebagai penampil data digunakan *display* LCD dot matrik 2 X 16 karakter. Sinyal-sinyal yang dipergunakan oleh LCD adalah data bus, RS, R/W dan E. Sinyal E dihubungkan ke P0.2 untuk mengaktifkan LCD. LCD akan aktif jika mikrokontroler memberi intruksi tulis pada alamat LCD. Sedang P0.0 untuk memberikan sinyal RS yang membedakan sinyal antara instruksi program atau instruksi penulisan data.

Untuk pin R/W difungsikan untuk menuliskan program jika diberi logika '0' dan untuk membaca jika diberi logika '1'. Untuk menampilkan data dari mikrokontroler maka pin-pin LCD dihubungkan dengan P0.0 sampai P0.7 seperti pada gambar berikut:



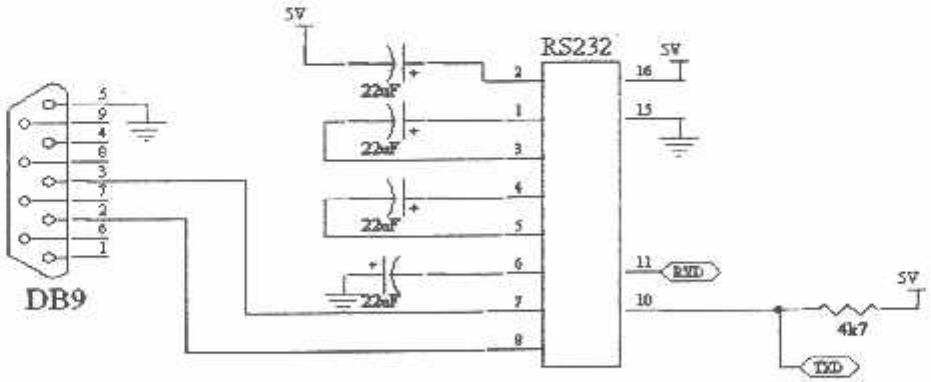
Gambar 3-6

Rangkaian LCD

VR pada pin 3 (VEE) digunakan untuk mengatur kontras dari karakter yang ditampilkan.

3.2.6. Perancangan Rangkaian RS232

Pada perancangan komunikasi data antara mikrokontroler dengan PC secara serial dengan menggunakan RS232 seperti pada gambar 3-7 berikut ini:



Gambar 3-7

Rangkaian Komunikasi *Serial* RS232

Serial control (SCON) merupakan register khusus pengontrol kerja *port serial*, diset untuk mentransmisikan 8 bit data UART (*Universal Asynchronous Reciever Transmitter)* yang merupakan standar komunikasi data dengan *baud rate* yang dapat diatur *(variable)*. Spesifikasi antar muka RS-232 akan dijelaskan berikut ini.

Pada sinyal yang dikirim, level tegangannya adalah +5 Vdc sampai +15 Vdc untuk biner '0' dan -5 Vdc sampai -15 Vdc untuk biner '1'. Sedangkan untuk data yang diterima, level tegangannya adalah +3 Vdc sampai +13 Vdc untuk biner '0' dan -3 Vdc sampai -13 Vdc untuk biner '1'. Pada perancangan digunakan *baudrate* sebesar 19200 bps, maka :

$$\text{Baud Rate} = \frac{2^{SMOD} \times \text{Frekuensi Osilator}}{32 \times 12[256 - TH1]}$$

$$19200 \text{ bps} = \frac{2^1 \times 11{,}0592.10^6}{32 \times 12[256 - TH1]}$$

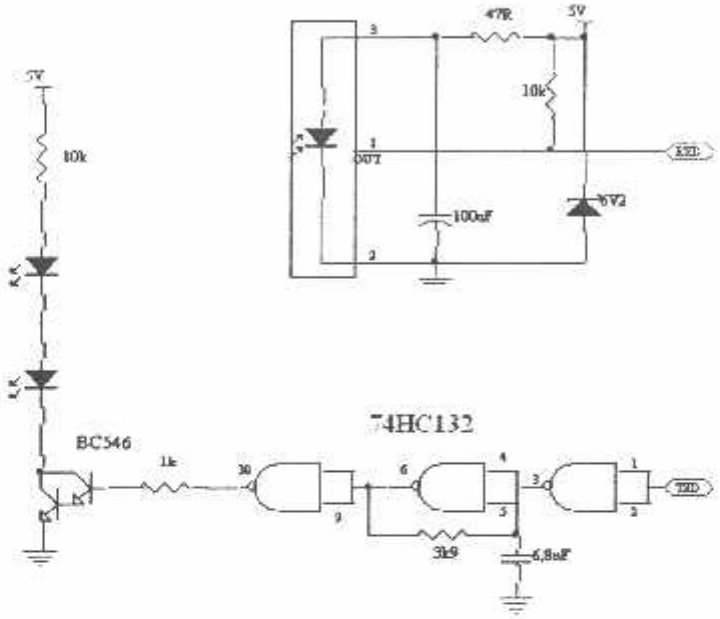
TH1 = 253 d = 0FDH

Dengan *baudrate* 19200 bps, maka untuk memproses satu bit data membutuhkan waktu 52,08 μs. Jadi untuk satu karakter yang terdiri atas 8 bit membutuhkan waktu sebesar: $8 \times 52{,}08 \times 10^{-6} - 0{,}42$ ms.

3.2.7. Perancangan Rangkaian Infra Merah

Pada rangkaian infra merah terdiri dari dua bagian yaitu bagian pemancar (*transmitter*) dan bagian penerima (*Reciever*). Pada bagian penerima, menggunakan DT I/O *Reciever* untuk menerima data dari KWH meter digital yang kemudian diproses pada mikrokontroler AT89S51 seperti pada gambar 3-8.

Pada bagian pemancar menggunakan DST-51 yang terdiri dari bagian modulator, bagian penguat dan diode infra merah seperti pada gambar 3-8.



Gambar 3-8

Rangkaian Infra Merah

Pancaran data infra merah harus dimodulasikan terlebih dahulu untuk menghindari kerusakan data akibat *noise*. Pada perancangan digunakan R sebesar 3,9 kΩ dan C sebesar 6,8 nF untuk membentuk frekuensi *carrier*, di mana VT- adalah batas bawah tegangan ambang 74HC132 yaitu sekitar 2 Volt dan VT+ adalah batas atas dari tegangan ambang 74HC132 yaitu sekitar 3 Volt. Sehingga frekuensi *carrier* yang terbentuk sebesar:

$$T = 2RC\left[\ln\left[\frac{Vs - VT-}{Vs}\right] - \ln\left[\frac{Vs - VT+}{Vs}\right]\right]$$

$$= 2 \times 3{,}9k \times 6{,}8n\ [\ \ln(3/5) - \ln(2/5)\ ] = 2{,}175\times10^{-5}\ s$$

$$F = \frac{1}{T} = \frac{1}{2{,}175\times10^{-5}}$$

= 45,98 kHz

Jadi frekuensi *carrier* yang digunakan untuk modulasi data yang dikirim adalah sebesar 45,98 kHz.

Pada perancangan digunakan *baudrate* sebesar 600 bps, maka :

$$\text{Baud Rate} = \frac{2^{SMOD} \text{ x Frekuensi Osilator}}{32 \text{ x } 12[256 - TH1]}$$

$$600 \text{ bps} = \frac{2^{1} x 11,0592.10^{6}}{32x12[256 - TH1]}$$

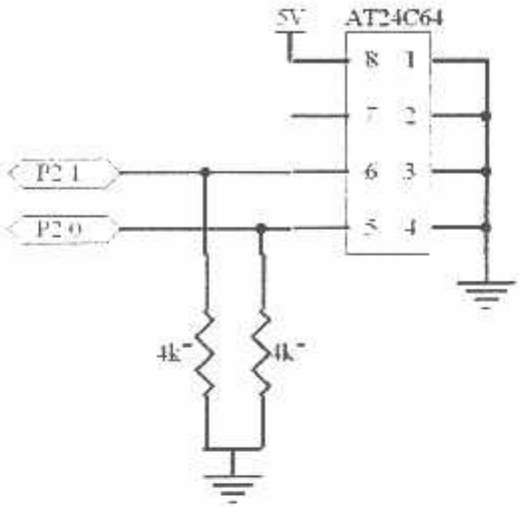
TH1 = 160 d = 0A0H

Dengan *baudrate* 600 bps, maka untuk memproses satu bit data membutuhkan waktu 1,67 ms. Jadi untuk satu karakter yang terdiri atas 8 bit membutuhkan waktu sebesar: $8 \times 1,67 \times 10^{-3} = 13,36$ ms.

3.2.8. Perancangan EEPROM AT24C64

Pada perancangan EEPROM AT24C64 yang mempunyai kapasitas 8 k*bytes* ini, untuk komunikasi dengan mikrokontroler menggunakan sistem I2C. Fitur utama I2C bus adalah sebagai berikut :

- Hanya melibatkan dua kabel yaitu *serial data line* (selanjutnya disebut SDA) dan *serial clock line* (selanjutnya disebut SCL).
- I2C merupakan serial bus dengan orientasi data 8 bit, komunikasi 2 arah, dengan kecepatan transfer data sampai 100 kbps pada mode standart dan 3,4 Mbps pada mode kecepatan tinggi.



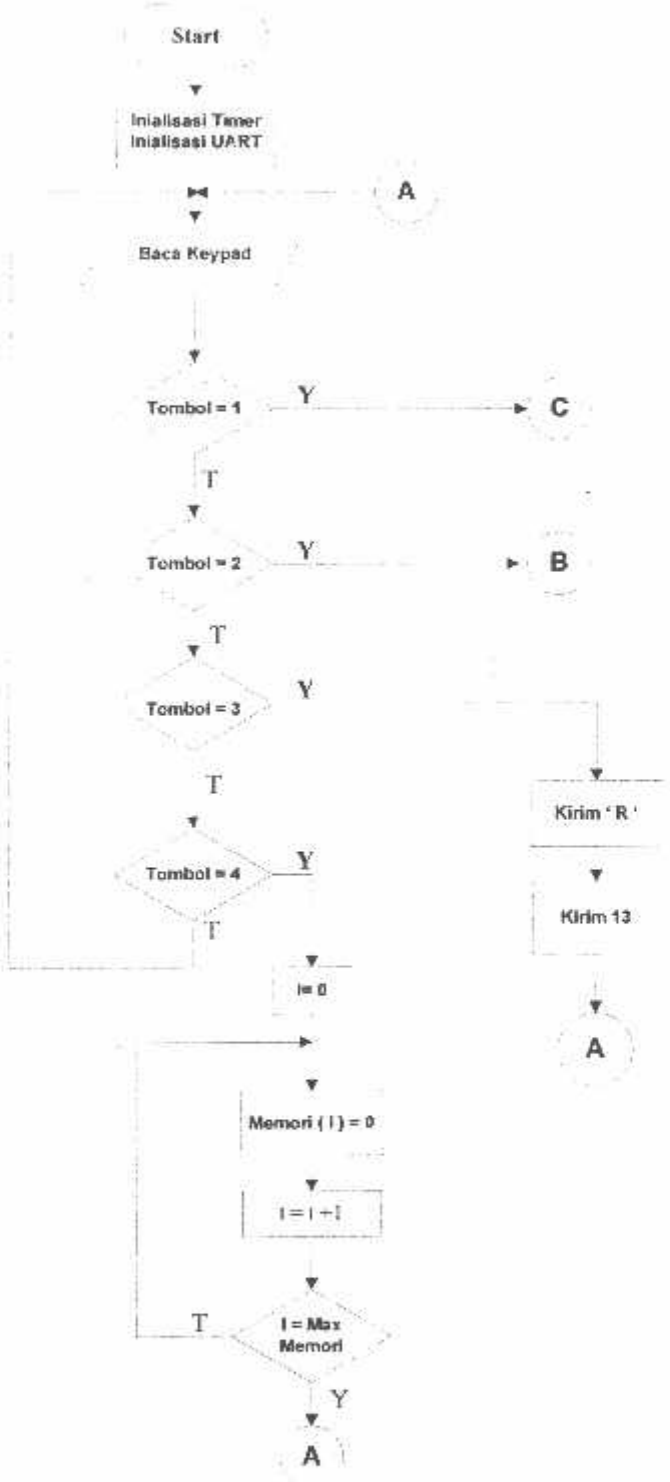
Gambar 3-9
Rangkaian EEPROM AT24C64

3.3. Perencanaan Perangkat Lunak

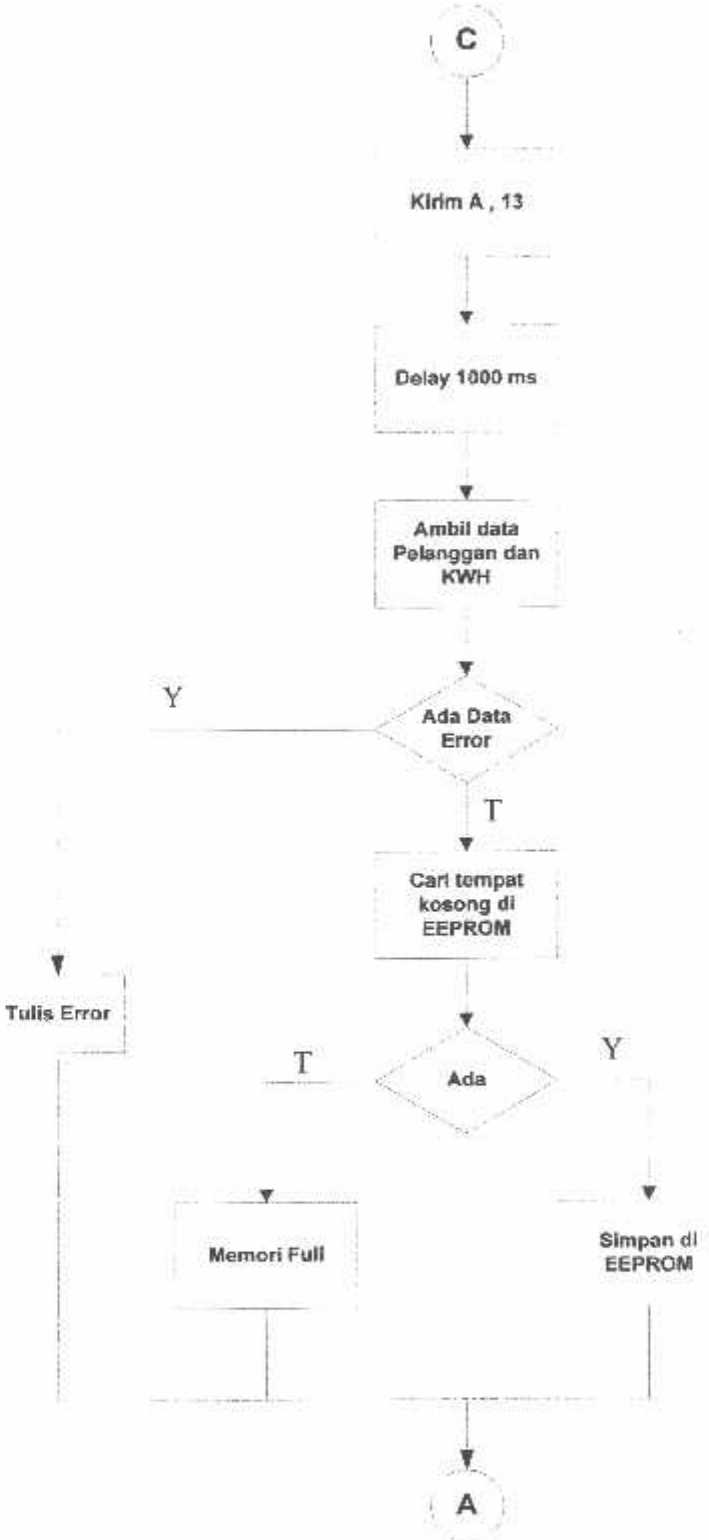
Untuk mendukung agar perangkat keras berfungsi sesuai dengan perencanaan, maka diperlukan perangkat lunak sebagai penunjangnya. Perangkat lunak ini sendiri maksudnya adalah suatu program yang kita buat yang nantinya akan ditanam ke dalam mikrokontroler AT89S51. Setelah mikrokontroler tersebut diprogram, maka akan diketahui apakah program yang telah kita buat bekerja sesuai dengan yang kita rencanakan ataukah masih memiliki kesalahan.

Sistem aplikasi mikrokontroller AT89S51 ini dapat mengatur dan mengendalikan keseluruhan sistem apabila ada urutan instruksi yang mendefinisikan secara jelas urutan tugas yang harus dikerjakan. Urutan instruksi ini sangat penting untuk didefinisikan, karena mikrokontroler dapat bekerja secara pasti sesuai dengan instruksi yang telah dibuat.

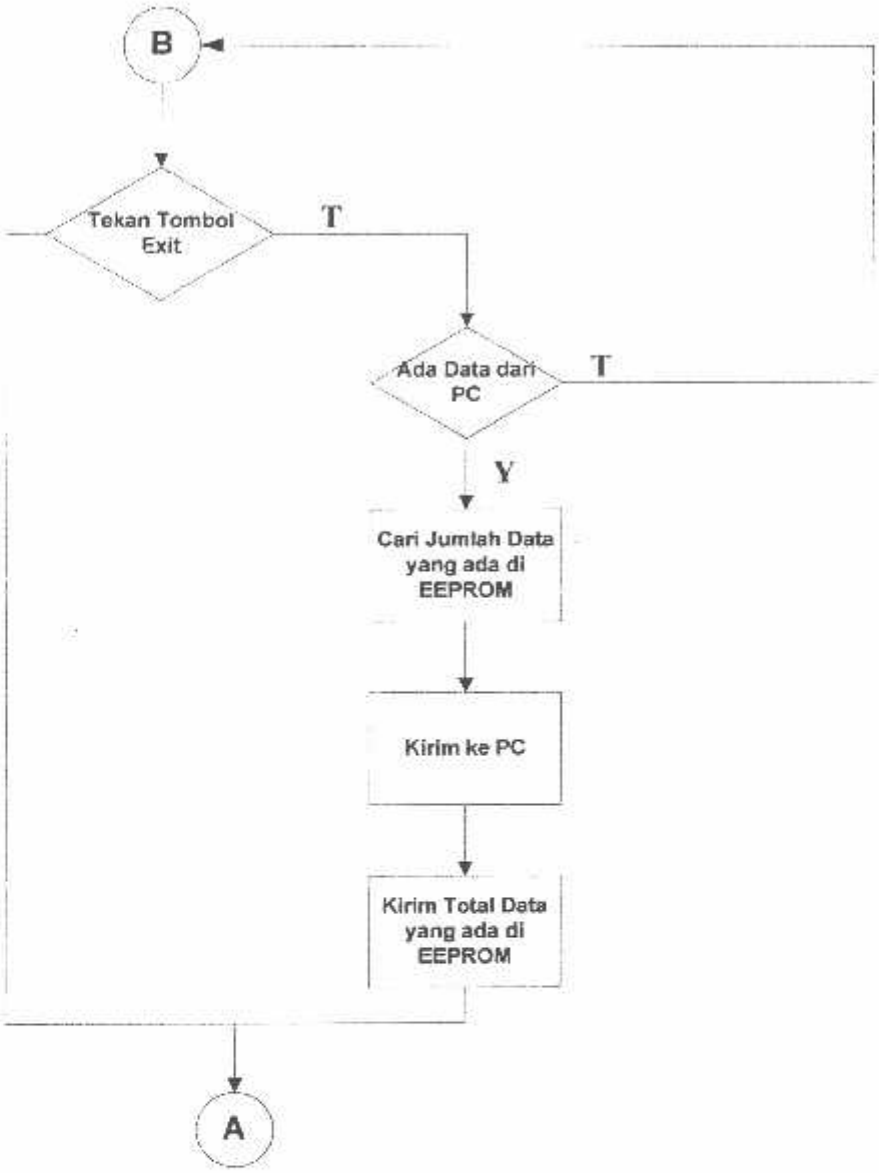
3.3.1. Perancangan Diagram Alir (*Flowchart*) pada PDE



Gambar 3-10 (a)
Diagram Alir Saat Penekanan Tombol 1 (Hapus Data PDE)
dan 2 (Reset KWH Meter Digital)



Gambar 3-10 (b)
Diagram Alir Saat Penekanan Tombol 4 (*Download*)



Gambar 3-10 (c)
Diagram alir Saat Penekanan tombol 3 (*Upload* ke PC)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BAB IV

HASIL PENGUJIAN ALAT

Untuk mendapatkan hasil yang maksimal setelah melaksanakan perancangan dan pembuatan alat, maka perlu dilakukan suatu pengujian terhadap alat yang telah dibuat. Pengujian ini bertujuan untuk mengetahui apakah alat yang telah dibuat telah dapat bekerja sesuai dengan perencanaan.

Bagian-bagian yang diuji dari peralatan ini adalah :

1. Pengkalibrasian KWH Meter Digital.
2. Pengujian pengambilan data pada KWH meter digital dengan menggunakan PDE.
3. Pengujian jarak yang bisa dijangkau pada saat pengambilan data.
4. Pengujian pengiriman data ke PC.

4.1. Pengkalibrasian KWH Meter Digital

4.1.1. Tujuan Pengkalibrasian

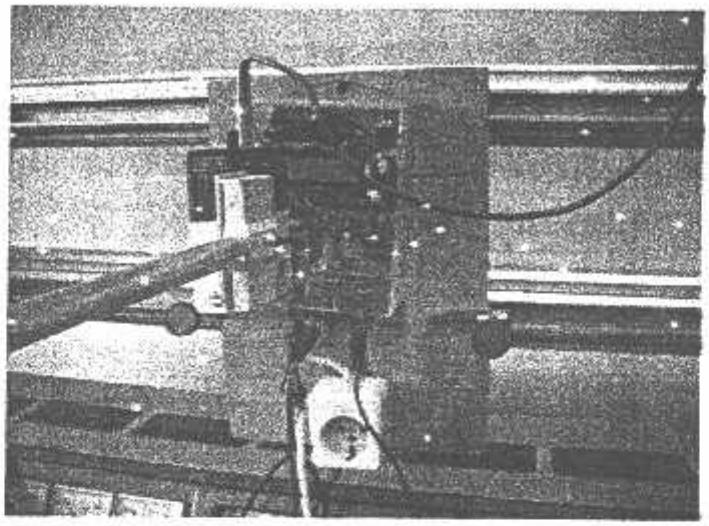
Untuk mengetahui berapa *error* dari KWH meter digital yang telah dibuat menurut standar dari PLN. Proses pengkalibrasian alat ini dilakukan di PLN Malang dan dilakukan oleh petugas tera PLN Malang.

4.1.2. Alat dan Bahan

1. KWH meter digital
2. Sensor impuls
3. Meja Tera
4. PC

4.1.3. Langkah Pengkalibrasian

1. Persiapan untuk mengaktifkan rangkaian
2. Menentukan tegangan dan arus pada meja tera
3. Menyalakan KWH meter digital selama 30 menit sebelum pengkalibrasian (standar PLN)
4. Pengkalibrasian KWH meter digital dengan menggunakan sensor impuls
5. PC digunakan untuk menghitung *error* (dengan menggunakan *software* pengkalibrasian) dengan masukan dari sensor impuls
6. Pengkalibrasian dilakukan sampai mendapatkan nilai *error* yang relatif kecil



Gambar 4-1

Pengkalibrasian KWH Meter Digital dengan Menggunakan Sensor Impuls

4.1.4. Hasil Pengkalibrasian

Dari pengkalibrasian KWH meter digital yang dibuat didapatkan *error* sebesar 2,86%, sehingga alat ini mempunyai tingkat keakuratan sebesar 97,14%. Faktor penyebab *error* antara lain sebagai berikut:

- Kualitas kawat tembaga (nilai tahanan jenis tembaga)
- Pemasangan sensor arus yang kurang tepat

Menentukan *error* dengan menggunakan perhitungan:

Diketahui: V = 220 v , I = 0,45 A, Cos φ = 1 (diset oleh petugas PLN)

$P_1 = V \times I \times \cos \varphi$

$= 220 \times 0{,}45 \times 1$

$= 0{,}99$ kWh

Diketahui: I (jumlah impuls yang dihitung) = 2 impuls

T (waktu yang diperlukan) = 70,65 detik

Ri (konstanta impuls) = 100 impuls/kWh

P_2 = (I x 3600) / (T x Ri)

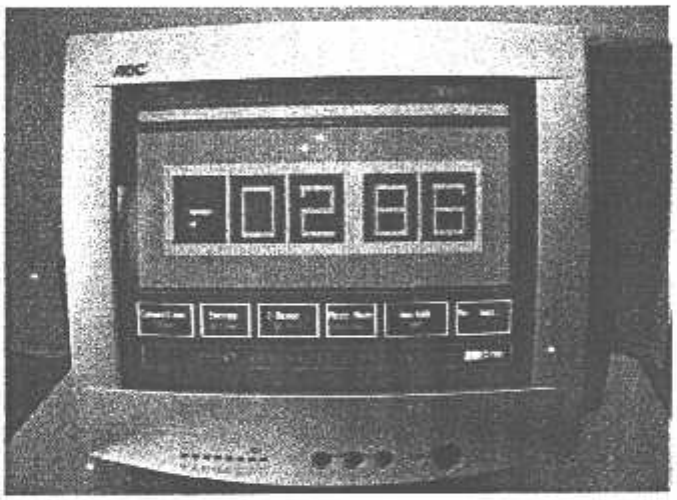
= (2 x 3600) / (70,65 x 100)

= 1,019 kWh

E = [(P1/P2)-1] x 100%

= [(0,99/1,019) – 1] x 100% = - 2,92%

Menentukan *error* dengan menggunakan PC (*software*):



Gambar 4-2

Tampilan Nilai *Error* pada PC

Terjadi perbedaan nilai *error* antara metode perhitungan dengan *software*, hal ini disebabkan oleh adanya pembulatan angka dalam perhitungan.

4.2. Pengujian Pengambilan Data pada KWH Meter Digital dengan Menggunakan PDE

4.2.1. Tujuan Pengujian

Tujuan dari pengujian ini adalah untuk menguji keakuratan data yang diambil dengan menggunakan PDE.

4.2.2. Peralatan Yang Digunakan

1. KWH meter digital
2. Beban berupa lampu dan heater
3. Catu daya AC 220 volt untuk sumber tegangan KWH meter digital
4. PDE (*Portable Data Entry*)

4.2.3. Langkah Pengujian

1. Persiapan untuk mengaktifkan peralatan
2. KWH meter dihubungkan dengan tegangan sumber AC 220 volt dan diberi beban
3. Mengatur nomor pelanggan (tersedia 4 nomor pelanggan dalam satu KWH meter untuk simulasi)
4. Setelah terjadi perubahan jumlah pemakaian energi yang ditunjukkan pada LCD KWH meter digital kemudian aktifkan PDE
5. *Download* data dari KWH meter digital dengan menggunakan PDE
6. Bandingkan data pada KWh meter digital dengan data pada PDE

7. Mengulangi kembali langkah 3, 4, 5, dan 6 sesuai dengan nomor pelanggan yang digunakan.

4.2.4. Hasil Pengujian

Hasil pengujian pengambilan data pada KWH meter digital dengan menggunakan PDE seperti terlihat pada tabel berikut ini:

Tabel 4-1 Hasil Pengujian Pengambilan Data

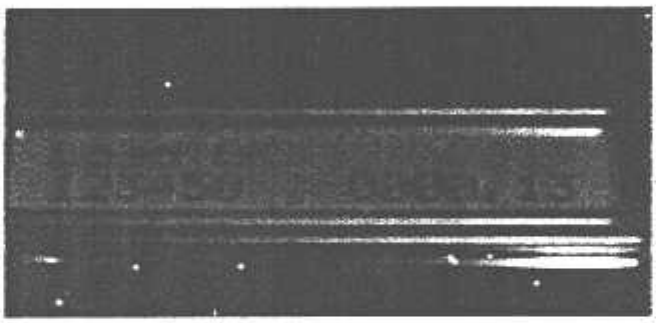
Nomor Pelanggan	Data pada LCD KWH meter digital (kWh)	Data pada LCD PDE (kWh)
123450	0000,13	0000,13
123450	0000,24	0000,24
123451	0000,05	0000,05
123451	0000,26	0000,26
123452	0000,27	0000,27
123452	0000,33	0000,33
123453	0000,10	0000,10
123453	0000,21	0000,21

Data diambil pada jarak 1m

Dari tabel di atas dapat disimpulkan bahwa data yang ditampilkan pada KWH meter digital sama dengan data yang ditampilkan pada PDE.

Gambar 4-3

Tampilan LCD pada KWH Meter Digital



Gambar 4-4

Tampilan LCD PDE

4.3. Pengujian Jarak pada Saat Pengambilan Data

4.3.1. Tujuan

Tujuan dari pengujian ini adalah untuk mengetahui berapa jarak maksimal yang dapat dijangkau oleh PDE dalam mengambil data dari KWH meter digital.

4.3.2. Alat dan Bahan

1. KWH meter digital
2. Beban berupa lampu dan heater

3. Catu daya AC 220 volt untuk sumber tegangan KWH meter digital
4. PDE (*Portable Data Entry*)
5. *Professional Tape* (Meteran)

4.3.3. Langkah Pengujian

1. Persiapan untuk mengaktifkan peralatan
2. KWH meter dihubungkan dengan tegangan sumber AC 220 volt dan diberi beban
3. Setelah terjadi perubahan jumlah pemakaian energi yang ditunjukkan pada LCD KWH meter digital kemudian aktifkan PDE
4. *Download* data dari KWH meter digital dengan mengatur jarak antara KWH meter digital dan PDE
5. Ulangi sampai pada jarak maksimal yang dapat dijangkau oleh PDE

4.3.4. Hasil Pengujian

Hasil pengujian jarak pada saat pengambilan data pada KWH meter digital dengan menggunakan PDE seperti terlihat pada tabel berikut ini:

Tabel 4-2 Hasil Pengujian Jarak yang Dapat Dijangkau Oleh PDE

No	Jarak (m)	KET
1	1	Sukses
2	1,5	Sukses
3	2	Sukses
4	2,5	Sukses
5	3	Sukses

6	3,5	Sukses
7	4	Gagal
8	4,5	Gagal

Pengujian dengan menggunakan baterai dalam keadaan baru

Dari hasil pengujian di atas dapat disimpulkan bahwa jangkauan maksimal dari PDE adalah 3,5 m. Hal ini disebabkan oleh kemampuan infra merah dalam mengirim dan menerima data hanya berkisar antara 3 sampai 5 m. Setelah dilakukan pengujian berulang kali ternyata kondisi baterai juga dapat mempengaruhi jangkauan dari alat ini.

4.4. Pengujian Pengiriman Data dari PDE ke PC

4.4.1. Tujuan

Tujuan dari pengujian ini adalah untuk mengetahui keakuratan PDE dalam mengirim data pada PC.

4.4.2. Alat dan Bahan

1. PDE (*Portable Data Entry*)
2. Kabel serial DB9
3. PC

4.4.3. Langkah Pengujian

1. Hubungkan PDE dan PC secara serial dengan menggunakan kabel DB9

2. Tekan tombol *upload* pada PDE (untuk pengiriman data ke PC)
3. Tekan *setport* untuk menentukan *port*, *baudrate*, dan jumlah bit yang digunakan
4. Tekan *open* (untuk membuka jalur data) lalu tekan *download* pada program tampilan Delphi (untuk mengambil data dari PDE)

4.4.4. Hasil Pengujian

Gambar 4-5

Tampilan Program Delphi

Dari hasil pengujian didapatkan data yang ditampilkan oleh form1 sebagai berikut:

021234500000081234500000000

Maka dapat diartikan sebagai berikut:

02 : kode jumlah data yang diambil

123450 : Nomor pelanggan

000008 : Jumlah pemakaian energi

123450 : Nomor pelanggan

000000 : Jumlah pemakaian energi

Dari 6 angka jumlah pemakaian energi, 2 angka terakhir adalah 1/100 kWh (2 angka setelah koma).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BAB V

KESIMPULAN DAN SARAN

5.1. Kesimpulan

Dari hasil perancangan dan pembuatan alat *portable data entry* untuk KWH meter digital melalui media infra merah yang dapat diakses pada PC, maka dapat diambil kesimpulan sebagai berikut:

1. Dari hasil pengkalibrasian dapat diketahui bahwa KWH meter digital memiliki *error* sebesar 2,86%.
2. Dari hasil pengujian alat, dapat diketahui bahwa jarak maksimal PDE dalam pengambilan data pada KWH meter digital adalah 3,5 meter, sehingga bila dalam pengambilan data jaraknya melebihi 3,5 meter maka PDE tidak dapat mengambil data dan tampilan pada LCD PDE adalah '*LOAD ERROR*'.
3. Dari hasil pengujian, dapat diketahui bahwa kondisi baterai yang dipakai juga dapat mempengaruhi jangkauan.

5.2. Saran

1. Perangkat yang dibuat akan lebih akurat dan lebih presisi lagi jika menggunakan komponen-komponen yang kualitas dan kemampuannya lebih baik.

2. Untuk pengembangan selanjutnya dari alat ini diharapkan menggunakan *transceiver* infra merah yang memiliki jangkauan yang lebih jauh.
3. Untuk mempertahankan jangkauan sebaiknya digunakan baterai yang memiliki arus yang lebih besar.
4. Untuk pengembangan selanjutnya dari alat ini, apabila dinginkan untuk menyimpan data pelanggan yang lebih banyak, maka sebaiknya digunakan memori yang berkapasitas lebih besar.

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LAMPIRAN

INSTITUT TEKNOLOGI NASIONAL
Jl. Raya Karanglo Km 2
MALANG

FORM BIMBINGAN SKRIPSI

Nama : Dwi Adimas Putro Siswoyo
NIM : 02.17.158
Masa Bimbingan : 15 Desember 2007 s/d 15 Juni 2008
Judul : Perancangan dan Pembuatan Alat *Portable Data Entry* untuk KWH Meter Digital Melalui Media Infra Merah yang Dapat Diakses pada PC

NO	Tanggal	Uraian	Paraf
1	04-02-08	Konsultasi Awal	
2	12-02-08	Konsultasi Bab I, II, III	
3	15-02-08	Revisi Bab II, III	
4	20-02-08	ACC Bab I, II, III & Konsultasi IV, V	
5	01-03-08	Revisi Bab IV	
6	03-03-08	ACC Bab IV & V	
7	05-03-08	ACC Makalah & Demo Alat	
8	14-03-08	ACC Laporan skripsi	
9			
10			

Malang,
Dosen Pembimbing

Ir. Widodo Pudji M, MT
NIP .P. 1028700171

Form S-4b

INSTITUT TEKNOLOGI NASIONAL
Jl. Raya Karanglo Km 2
MALANG

FORM BIMBINGAN SKRIPSI

Nama : Dwi Adimas Putro Siswoyo
NIM : 02.17.158
Masa Bimbingan : 15 Desember 2007 s/d 15 Juni 2008
Judul : Perancangan dan Pembuatan Alat *Portable Data Entry* untuk KWH Meter Digital Melalui Media Infra Merah yang Dapat Diakses pada PC

NO	Tanggal	Uraian	Paraf
1	04-02-08	Konsultasi Awal	
2	12-02-08	Konsultasi Bab I, II, III	
3	15-02-08	Revisi Bab II, III	
4	20-02-08	Acc Bab I, II, III dan konsultasi Bab IV, V	
5	01-03-08	Revisi Bab IV	
6	03-03-08	Acc Bab IV dan V	
7	05-03-08	Acc. Seminar Hasil	
8	14-03-08	Acc Laporan skripsi	
9			
10			

Malang,
Dosen Pembimbing 21/4 '08

Sotyohadi, ST, MSc.

Form S-4b

INSTITUT TEKNOLOGI NASIONAL
FAKULTAS TEKNOLOGI INDUSTRI
JURUSAN TEKNIK ELEKTRO

Formulir Perbaikan Ujian Skripsi

Dalam pelaksanaan Ujian Skripsi Janjang Strata 1 Jurusan Teknik Elektro Konsentasi T. Energi Listrik / T. Elektronika, maka perlu adanya perbaikan skripsi untuk mahasiswa :

NAMA : Dwi Arisman, PJ
N I M : 02.17.158
Perbaikan meliputi :

1) Kesimpulan pengujian infra red salah (ada kalinya dkm. jarak 1 m) harap ubah pikiran ttg pengujian infra red.

2) Ganti 74LS07 yg multiplexer (cir gambar rangkaian saja).

Malang, 17 march '08

(____________)

INSTITUT TEKNOLOGI NASIONAL
FAKULTAS TEKNOLOGI INDUSTRI
JURUSAN TEKNIK ELEKTRO

Formulir Perbaikan Ujian Skripsi

Dalam pelaksanaan Ujian Skripsi Janjang Strata 1 Jurusan Teknik Elektro Konsentasi T. Energi Listrik / T Elektronika, maka perlu adanya perbaikan skripsi untuk mahasiswa :

NAMA : DWI AGUNG
NIM : 02.17.150
Perbaikan meliputi :

1) PERTIMBANGKAN MULTIPLEX
2)

Malang,

(_____)

INSTITUT TEKNOLOGI NASIONAL MALANG
FAKULTAS TEKNOLOGI INDUSTRI
JURUSAN TEKNIK ELEKTRO S-1
KONSENTRASI ELEKTRONIKA

LEMBAR PERSETUJUAN PERBAIKAN SKRIPSI

Dari hasil ujian skripsi jurusan Teknik Elektro jenjang strata satu (S-1), yang diselenggarakan pada:

Hari : Senin
Tanggal : 17 Maret 2008

Telah dilakukan perbaikan oleh:

Nama : Dwi Adimas Putro S.
N.I.M : 02.17.158
Jurusan : TEKNIK ELEKTRO S-1
Konsentrasi : ELEKTRONIKA
Judul Skripsi : **Perancangan dan Pembuatan Alat Portable Data Entry untuk KWH Meter Digital Melalui Media Infra Merah yang Dapat Diakses pada PC**

Perbaikan meliputi:

No.	Materi Perbaikan	Keterangan
1.	Hanya mengubah tulisan tentang pengujian infra merah pada kesimpulan	
2.	Ganti 74LS07 dengan multiplexer (gambar rangkaian saja)	

Anggota Penguji

Penguji I

Joseph Dedy Irawan, ST. MT
NIP.132315178

Penguji II

Dr. Cahya Crisdian, MSc
NIP.1030400412

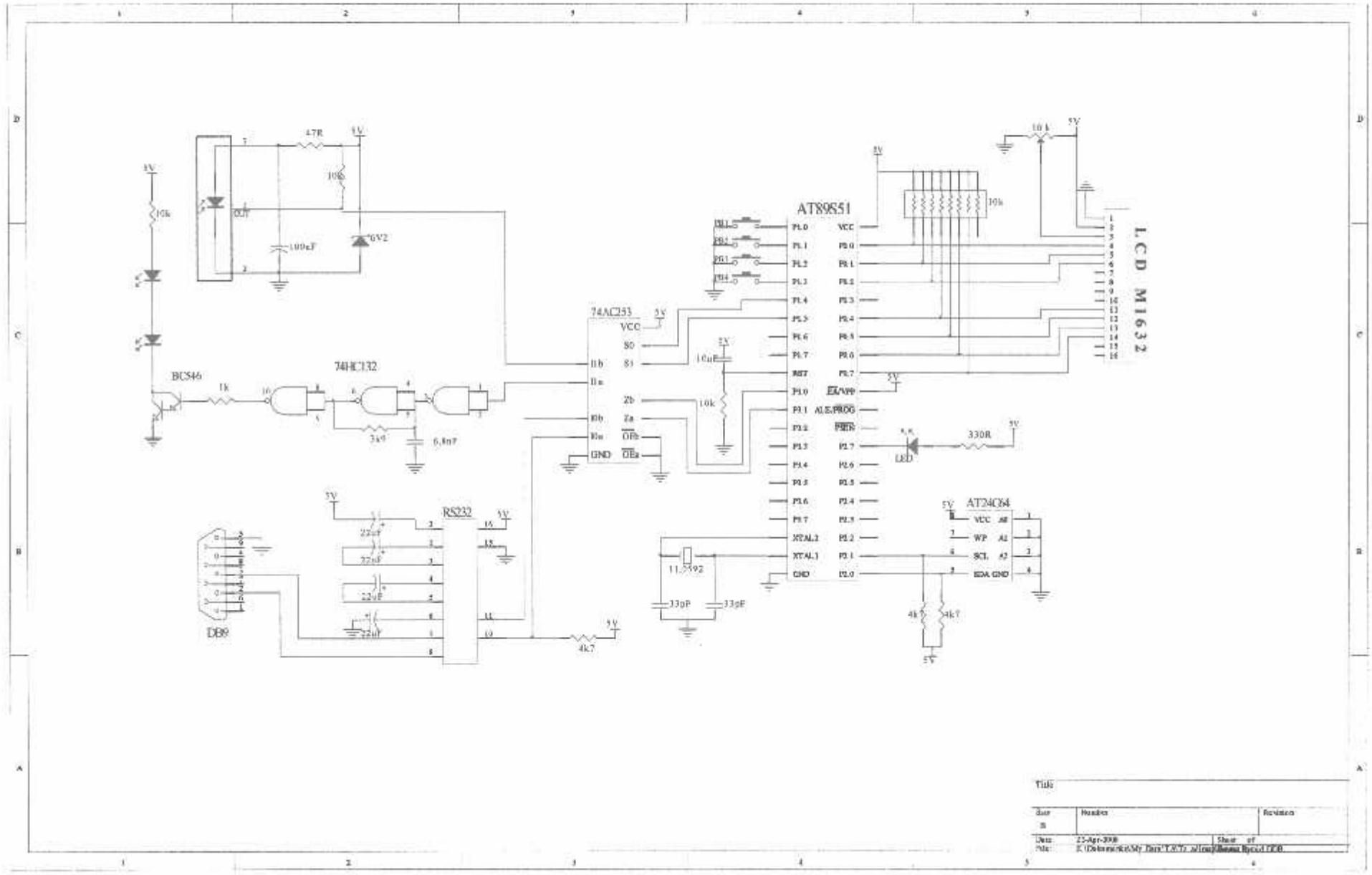
Diperiksa dan Disetujui,

Dosen Pembimbing I

Ir. Widodo Pudji M, MT
NIP .P. 1028700171

Dosen Pembimbing II

Sotyohadi, ST. MSc


AT89S51
74AC253
74HC132
RS232
DB9
LCD M1632
AT24C64
BC546
LED
330R
47R
10k
100nF
6V2
1k
3k9
6.8nF
22nF
4k7
11.5592
33pF
10uF
5V
VCC
GND
P1.0
P1.1
P1.2
P1.3
P1.4
P1.5
P1.6
P1.7
RST
P3.0
P3.1
P3.2
P3.3
P3.4
P3.5
P3.6
P3.7
XTAL2
XTAL1
P2.7
P2.6
P2.5
P2.4
P2.3
P2.2
P2.1
P2.0
P0.0
P0.1
P0.2
P0.3
P0.4
P0.5
P0.6
P0.7
EA/VPP
ALE/PROG
PSEN
SCL
SDA
WP
A0
A1
A2

```
/*=============================================================================*/
/* mapping memori                                                              */
/* 0 12345 6789012345                                                          */
/*=============================================================================*/


/*=============================================================================*/
/* Deklarasi interface mikrokontroller AT89S51                                 */
/*=============================================================================*/
#include <at89x51.h>
#include <stdbool.h>
#include <stdrlib.h>
#include "PENDING.c"
/*=============================================================================*/
/* Deklarasi interface LCD                                                     */
/* remark:                                                                     */
/*    menggunakan interface 4 bit                                              */
/*    RS  P0.0                                                                 */
/*    RW  P0.1                                                                 */
/*    EN  P0.2                                                                 */
/*    D4  P0.4                                                                 */
/*    D5  P0.5                                                                 */
/*    D6  P0.6                                                                 */
/*    D7  P0.7                                                                 */
/*=============================================================================*/
#define  lcd_port    P0
#include <lcd4b.h>

/*=============================================================================*/
/* Deklarasi interface serial EEPROM                                           */
/* remark:                                                                     */
/*    SDA P2.3                                                                 */
/*    SDL P2.2                                                                 */
/*=============================================================================*/
#define EEPROM_ADDR              0xA0
#define SCL P2_2
#define SDA P2_3
#include "twi.c"


/*=============================================================================*/
/* Deklarasi interface                                                         */
/*=============================================================================*/
#define  tb_download             P1_0
#define  tb_transfer             P1_1
#define  tb_free                 P1_2
#define  tb_hapus                P1_3
#define  led_kedip               P2_4


#define  sbuf_size               30
#define  EOS_buf                 serbuf[ser_dig-1]
#define  EOS                     3
#define  total_member            10
#define  member_dig_size         6
#define  kWh_dig_size            6
//#define  record_size             16
#define  record_size             ((member_dig_size + kWh_dig_size) + 1 )


/*=============================================================================*/
/* Deklarasi variable                                                          */
/*=============================================================================*/
unsigned char          serbuf[sbuf_size],serial_current,ser_dig,tmp,tombol,
                       no_pelanggan[member_dig_size],data_kwh[kwh_dig_size],
                       tmp_kosong;
unsigned int           tick_kedip,tick_ambil;
bool                   loop_ambil,exit_upload,exit_cari,exit,errorser;
```

```
/*=============================================================================*/
/* Deklarasi prototype function                                                */
/*=============================================================================*/
void InitHardware();
void serial_reset();
void putchar(unsigned char dt);
unsigned char read_EEPROM16(unsigned char chip_addr,unsigned int address);
void write_EEPROM16(unsigned char chip_addr,unsigned int address, unsigned char
nilai);
char baca_keypad();
void proc_download();
void proc_upload();
void proc_reset();
void main_view();
unsigned char  cari_tempat();
void hapus_memori();
void proc_hapus();

void TimerInterrupt (void) interrupt 1 using 1
{
        TH0 = 0xFC; //1mS
        TL0 = 0x66;
        if (++tick_kedip>1000)
        {
      tick_kedip=0;
      led_kedip=!led_kedip;
   }
}

void it_Serial () interrupt 4
{
        RI=0    ;
        serbuf[ser_dig]=SBUF;
        if (++ser_dig>=sbuf_size) ser_dig =0;
}


/*****************************************************************************/
void main()
{
InitHardware()    ;  //Serial,timer
lcd_init()        ;  //inisialisasi lcd
lcd_command(0x0C) ;  //cursor off
serial_reset()    ;
main_view()       ;
while (1)
{
   tombol=baca_keypad();
   if(tombol==1)        proc_download();
   else if (tombol==2)  proc_upload();
   else if (tombol==3)  proc_reset();
   else if (tombol==4)  proc_hapus();
}
}
/*****************************************************************************/

void InitHardware()
{
        TMOD    =0x21   ;
        SCON    =0x50   ;
        PCON    |= 0x80;//double speed
   TH1     =160   ;//300bps @11,059200Hz double speed jadi 600 bps
        EA      =true   ;
        ET0     =true   ;
```

```
        TR0     =true  ;
        TR1     =true  ;
        ES      =true  ;
        PS      =true  ;
}

void serial_reset()
{
   char i;
   serial_current=ser_dig=0;
   for(i=0;i<sbuf_size;i++) serbuf[i]=0;
}

void putchar(unsigned char dt)
{
        SBUF    = dt;
        while(!TI){;}
        TI              = 0;
}


unsigned char read_EEPROM16(unsigned char chip_addr,unsigned int address)
{
     unsigned char datax                                        ;
     unsigned char addresshi                                ;
     unsigned char addresslo                                ;
     unsigned char chip                                         ;
          addresshi     = address >> 8                          ;
          addresslo     = address                                       ;
          chip          = chip_addr << 1                        ;
     i2c_start()                                                        ;
     i2c_write(EEPROM_ADDR | chip )             ;
     i2c_write(addresshi)                                       ;
     i2c_write(addresslo)                                       ;
          i2c_stop()                                                                    ;
     i2c_start()                                                        ;
     i2c_write(EEPROM_ADDR | (chip | 1 ))       ;
     datax = i2c_read(0)                                        ;
     i2c_stop()                                                         ;
     return datax                                                       ;
}

void write_EEPROM16(unsigned char chip_addr,unsigned int address, unsigned char
nilai)
{
     unsigned char addresshi                                ;
     unsigned char addresslo                                ;
     unsigned char chip                                         ;
     addresshi  = address >> 8                              ;
          addresslo     = address                                       ;
          chip          = chip_addr << 1                        ;
          i2c_start()                                                   ;
     i2c_write(EEPROM_ADDR | chip )     ;
     i2c_write(addresshi)                                       ;
     i2c_write(addresslo)                                       ;
     i2c_write(nilai)                                           ;
     i2c_stop()                                                         ;
     delay_ms(10)                                                       ;
}

char baca_keypad()
{
 char tb;
 tb=0;
 if (!tb_download)    tb=1;
 else if(!tb_transfer) tb=2;
 else if(!tb_free)     tb=3;
 else if(!tb_hapus)    tb=4;
```

```
 return tb;
}

void proc_download()
{
char i,j;
   lcd_clear();
   lcd_putsf("Load ");
   serial_reset();
   ES=false;
   putchar('A');
   putchar(13);
   ES=true;
   delay_ms(200);
   if(ser_dig<4)
   {
      delay_ms(200);
      serial_reset();
      ES=false;
      putchar('A');
      putchar(13);
      ES=true;
   }
   delay_ms(500);


   strclr(no_pelanggan,member_dig_size);
   strclr(data_kWh,kWh_dig_size);

   //lcd_gotoxy(0,0);
   //for (i=0;i<16;i++) lcd_putchar(serbuf[i]);

   for (i=0;i<member_dig_size;i++)  no_pelanggan[i] = serbuf[i+2];
   for (i=0;i<kWh_dig_size;i++)  data_kWh[i] = serbuf[i+8];

   j=0;
   errorser=false;
   for(i=0;i<6;i++)
   {
      if( (no_pelanggan[i]<0x30) || (no_pelanggan[i]>0x39) ) errorser=true;
   }
   for(i=0;i<6;i++)
   {
      if( (data_kWh[i]<0x30) || (data_kWh[i]>0x39) ) errorser=true;
   }


   if ( errorser )
   {
      lcd_putsf("ERROR");
   }
   else
   {
      lcd_putsf("OK");
      tmp_kosong= cari_tempat();
      if(tmp_kosong!=255)
      {
         lcd_gotoxy(0,1);
         for (i=0;i<member_dig_size;i++) lcd_putchar(no_pelanggan[i]);
         lcd_putchar(' ');
         lcd_putchar(' ');
         lcd_putchar(' ');
         for (i=0;i<kWh_dig_size;i++)
         {
            lcd_putchar(data_kWh[i]);
            if (i==3)lcd_putchar(',');
         }
         tmp_kosong=tmp_kosong*record_size;
```

```
            write_EEPROM16(0,tmp_kosong,1);
            for (i=0;i<member_dig_size;i++)
write_EEPROM16(0,tmp_kosong+i+1,no_pelanggan[i]);
            for (i=0;i<kWh_dig_size;i++)
write_EEPROM16(0,tmp_kosong+i+7,data_kWh[i]);
         }
         else
         {
            lcd_gotoxy(0,1);
            lcd_putsf("Memori Full !!!!");
         }
      }
      delay_ms(2000);
      //while(baca_keypad()!=0);
      lcd_clear();
      main_view();
}

void proc_upload()
{
   char i,j,posisi,header,jml;

   lcd_clear();
   lcd_putsf("PC UpLoad");
   TH1   =253     ;//9600bps @11,059200Hz double speed jadi 19200 bps
   serial_reset() ;
   exit_upload=false;
   while(!exit_upload)
   {
      if(baca_keypad()==3)
      {
        exit_upload=true;
        while(baca_keypad()!=0);
      }
      if(ser_dig!=0)
      {
         jml=0;
         for (i=0;i<total_member;i++)
         {
            posisi=i*record_size;
            header=read_EEPROM16(0,posisi);
            if(header==1) jml++;
         }
         putchar(jml/10%10|0x30);
         putchar(jml%10|0x30);
         for (i=0;i<total_member;i++)
         {
            posisi=i*record_size;
            header=read_EEPROM16(0,posisi);
            if(header==1)
            {
               for(j=0;j<12;j++)
               {
                  putchar(read_EEPROM16(0,posisi+j+1));
                  //if(j==9) putchar(',');
               }
               //putchar(' ');
            }
         }
         putchar(13);putchar(10);
         exit_upload=true;
      }

   }
   lcd_clear();
   main_view();
   TH1   =160     ;//300bps @11,059200Hz double speed jadi 600 bps
}
```

```
void proc_reset()
{
   lcd_clear();
   lcd_putsf("Reset kWh");
   ES=false;
   putchar('R');
   putchar(13);
   ES=true;
   while(baca_keypad()!=0);
   lcd_clear();
   main_view();
}

void main_view()
{
   lcd_gotoxy(0,0);lcd_putsf("main view");
   lcd_gotoxy(0,1);lcd_putsf("main view");
}

unsigned char  cari_tempat()
{
   unsigned char i,posisi,hasil,tmp;

   i=0;
   hasil=255;
   exit_cari=false;
   while(!exit_cari)
   {
      posisi=i*record_size;
      tmp=read_EEPROM16(0,posisi);
      if (tmp==0)
      {
         hasil=i;
         exit_cari=true;
      }
      i++;
      if (i>=total_member) exit_cari=true;
   }
   return hasil;
}

void hapus_memori()
{
   char i,posisi;
   for (i=0;i<total_member;i++)
   {
      posisi=i*record_size;
      write_EEPROM16(0,posisi,0);
   }
}

void proc_hapus()
{
   lcd_clear();
   lcd_putsf("Hapus data...");
   hapus_memori();
   delay_ms(1000);
   lcd_putsf("OK");
   delay_ms(1000);
   lcd_clear();
   main_view();
}
```

Features

- Compatible with MCS-51® Products
- 4K Bytes of In-System Programmable (ISP) Flash Memory
  - Endurance: 1000 Write/Erase Cycles
- 4.0V to 5.5V Operating Range
- Fully Static Operation: 0 Hz to 33 MHz
- Three-level Program Memory Lock
- 128 x 8-bit Internal RAM
- 32 Programmable I/O Lines
- Two 16-bit Timer/Counters
- Six Interrupt Sources
- Full Duplex UART Serial Channel
- Low-power Idle and Power-down Modes
- Interrupt Recovery from Power-down Mode
- Watchdog Timer
- Dual Data Pointer
- Power-off Flag
- Fast Programming Time
- Flexible ISP Programming (Byte and Page Mode)

Description

The AT89S51 is a low-power, high-performance CMOS 8-bit microcontroller with 4K bytes of in-system programmable Flash memory. The device is manufactured using Atmel's high-density nonvolatile memory technology and is compatible with the industry-standard 80C51 instruction set and pinout. The on-chip Flash allows the program memory to be reprogrammed in-system or by a conventional nonvolatile memory programmer. By combining a versatile 8-bit CPU with in-system programmable Flash on a monolithic chip, the Atmel AT89S51 is a powerful microcontroller which provides a highly-flexible and cost-effective solution to many embedded control applications.

The AT89S51 provides the following standard features: 4K bytes of Flash, 128 bytes of RAM, 32 I/O lines, Watchdog timer, two data pointers, two 16-bit timer/counters, a five-vector two-level interrupt architecture, a full duplex serial port, on-chip oscillator, and clock circuitry. In addition, the AT89S51 is designed with static logic for operation down to zero frequency and supports two software selectable power saving modes. The Idle Mode stops the CPU while allowing the RAM, timer/counters, serial port, and interrupt system to continue functioning. The Power-down mode saves the RAM contents but freezes the oscillator, disabling all other chip functions until the next external interrupt or hardware reset.

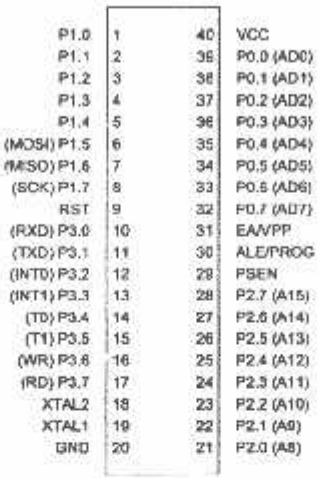
8-bit Microcontroller with 4K Bytes In-System Programmable Flash

AT89S51

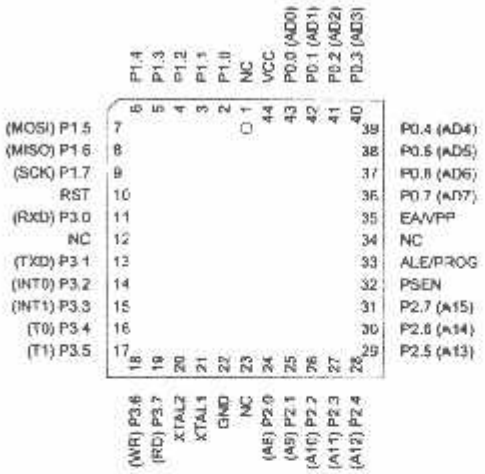
Rev. 2487A–10/01

Pin Configurations

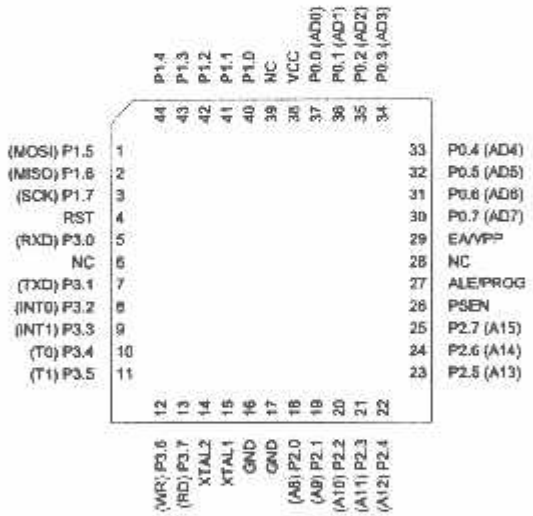
PDIP



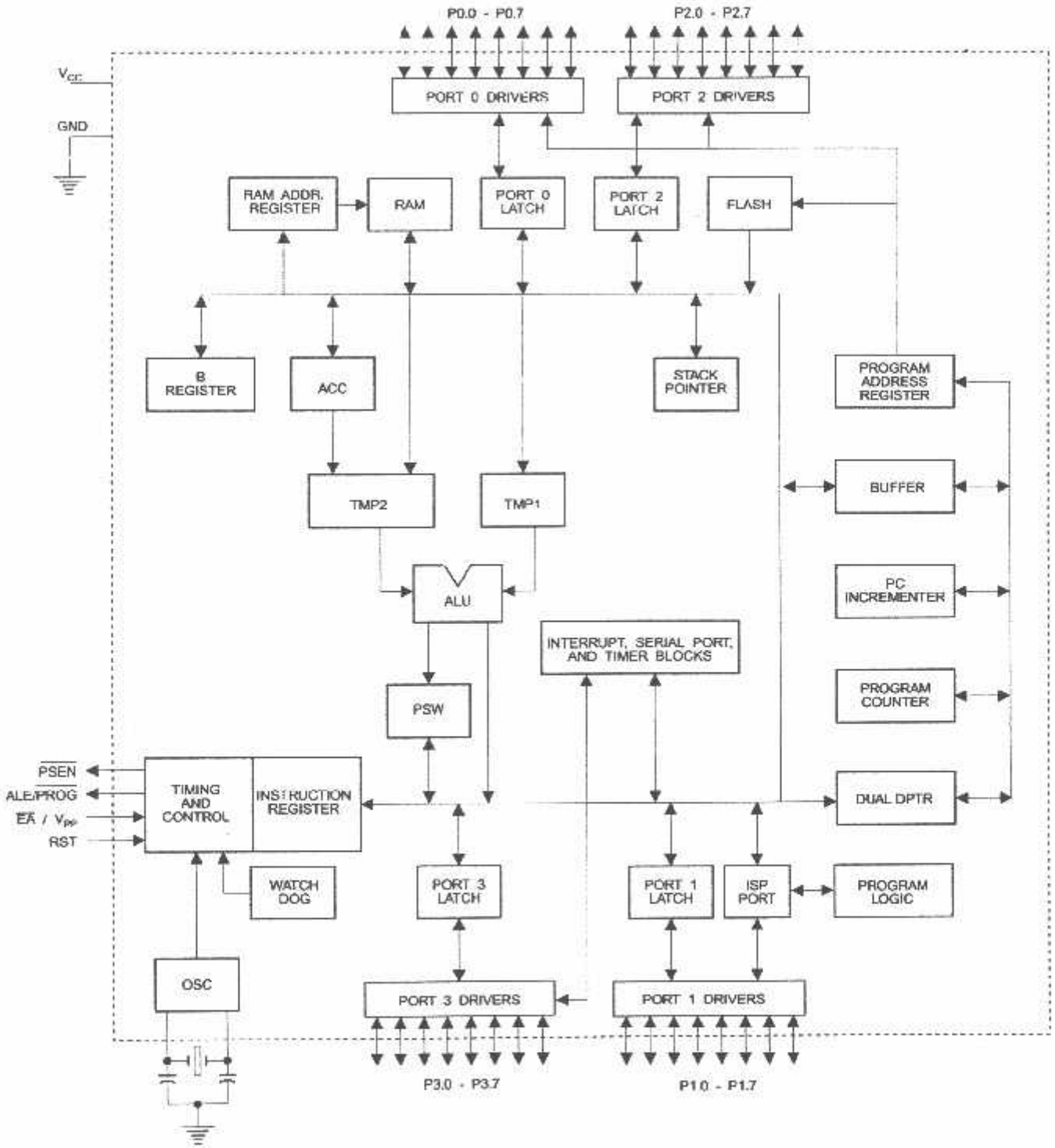
PLCC



TQFP



Block Diagram



Pin Description

VCC

Supply voltage.

GND

Ground.

Port 0

Port 0 is an 8-bit open drain bidirectional I/O port. As an output port, each pin can sink eight TTL inputs. When 1s are written to port 0 pins, the pins can be used as high-impedance inputs.

Port 0 can also be configured to be the multiplexed low-order address/data bus during accesses to external program and data memory. In this mode, P0 has internal pull-ups.

Port 0 also receives the code bytes during Flash programming and outputs the code bytes during program verification. **External pull-ups are required during program verification.**

Port 1

Port 1 is an 8-bit bidirectional I/O port with internal pull-ups. The Port 1 output buffers can sink/source four TTL inputs. When 1s are written to Port 1 pins, they are pulled high by the internal pull-ups and can be used as inputs. As inputs, Port 1 pins that are externally being pulled low will source current (I_{IL}) because of the internal pull-ups.

Port 1 also receives the low-order address bytes during Flash programming and verification.

Port Pin	Alternate Functions
P1.5	MOSI (used for In-System Programming)
P1.6	MISO (used for In-System Programming)
P1.7	SCK (used for In-System Programming)

Port 2

Port 2 is an 8-bit bidirectional I/O port with internal pull-ups. The Port 2 output buffers can sink/source four TTL inputs. When 1s are written to Port 2 pins, they are pulled high by the internal pull-ups and can be used as inputs. As inputs, Port 2 pins that are externally being pulled low will source current (I_{IL}) because of the internal pull-ups.

Port 2 emits the high-order address byte during fetches from external program memory and during accesses to external data memory that use 16-bit addresses (MOVX @ DPTR). In this application, Port 2 uses strong internal pull-ups when emitting 1s. During accesses to external data memory that use 8-bit addresses (MOVX @ RI), Port 2 emits the contents of the P2 Special Function Register.

Port 2 also receives the high-order address bits and some control signals during Flash programming and verification.

Port 3

Port 3 is an 8-bit bidirectional I/O port with internal pull-ups. The Port 3 output buffers can sink/source four TTL inputs. When 1s are written to Port 3 pins, they are pulled high by the internal pull-ups and can be used as inputs. As inputs, Port 3 pins that are externally being pulled low will source current (I_{IL}) because of the pull-ups.

Port 3 receives some control signals for Flash programming and verification.

Port 3 also serves the functions of various special features of the AT89S51, as shown in the following table.

Port Pin	Alternate Functions
P3.0	RXD (serial input port)
P3.1	TXD (serial output port)
P3.2	$\overline{INT0}$ (external interrupt 0)
P3.3	$\overline{INT1}$ (external interrupt 1)
P3.4	T0 (timer 0 external input)
P3.5	T1 (timer 1 external input)
P3.6	$\overline{WR}$ (external data memory write strobe)
P3.7	$\overline{RD}$ (external data memory read strobe)

RST

Reset input. A high on this pin for two machine cycles while the oscillator is running resets the device. This pin drives High for 98 oscillator periods after the Watchdog times out. The DISRTO bit in SFR AUXR (address 8EH) can be used to disable this feature. In the default state of bit DISRTO, the RESET HIGH out feature is enabled.

ALE/$\overline{PROG}$

Address Latch Enable (ALE) is an output pulse for latching the low byte of the address during accesses to external memory. This pin is also the program pulse input ($\overline{PROG}$) during Flash programming.

In normal operation, ALE is emitted at a constant rate of 1/6 the oscillator frequency and may be used for external timing or clocking purposes. Note, however, that one ALE pulse is skipped during each access to external data memory.

If desired, ALE operation can be disabled by setting bit 0 of SFR location 8EH. With the bit set, ALE is active only during a MOVX or MOVC instruction. Otherwise, the pin is weakly pulled high. Setting the ALE-disable bit has no effect if the microcontroller is in external execution mode.

$\overline{PSEN}$

Program Store Enable ($\overline{PSEN}$) is the read strobe to external program memory.

When the AT89S51 is executing code from external program memory, $\overline{PSEN}$ is activated twice each machine cycle, except that two $\overline{PSEN}$ activations are skipped during each access to external data memory.

$\overline{EA}$/VPP

External Access Enable. $\overline{EA}$ must be strapped to GND in order to enable the device to fetch code from external program memory locations starting at 0000H up to FFFFH. Note, however, that if lock bit 1 is programmed, $\overline{EA}$ will be internally latched on reset.

$\overline{EA}$ should be strapped to V_{CC} for internal program executions.

This pin also receives the 12-volt programming enable voltage (V_{PP}) during Flash programming.

XTAL1

Input to the inverting oscillator amplifier and input to the internal clock operating circuit.

XTAL2

Output from the inverting oscillator amplifier

Special Function Registers

A map of the on-chip memory area called the Special Function Register (SFR) space is shown in Table 1.

Note that not all of the addresses are occupied, and unoccupied addresses may not be implemented on the chip. Read accesses to these addresses will in general return random data, and write accesses will have an indeterminate effect.

Table 1. AT89S51 SFR Map and Reset Values

0F8H									0FFH
0F0H	B 00000000								0F7H
0E8H									0EFH
0E0H	ACC 00000000								0E7H
0D8H									0DFH
0D0H	PSW 00000000								0D7H
0C8H									0CFH
0C0H									0C7H
0B8H	IP XX000000								0BFH
0B0H	P3 11111111								0B7H
0A8H	IE 0X000000								0AFH
0A0H	P2 11111111		AUXR1 XXXXXXX0				WDTRST XXXXXXXX		0A7H
98H	SCON 00000000	SBUF XXXXXXXX							9FH
90H	P1 11111111								97H
88H	TCON 00000000	TMOD 00000000	TL0 00000000	TL1 00000000	TH0 00000000	TH1 00000000	AUXR XXX00XX0		8FH
80H	P0 11111111	SP 00000111	DP0L 00000000	DP0H 00000000	DP1L 00000000	DP1H 00000000		PCON 0XXX0000	87H

User software should not write 1s to these unlisted locations, since they may be used in future products to invoke new features. In that case, the reset or inactive values of the new bits will always be 0.

Interrupt Registers: The individual interrupt enable bits are in the IE register. Two priorities can be set for each of the five interrupt sources in the IP register.

Table 2. AUXR: Auxiliary Register

AUXR Address = 8EH Reset Value = XXX00XX0B

Not Bit Addressable

Bit	7	6	5	4	3	2	1	0
	–	–	–	WDIDLE	DISRTO	–	–	DISALE

– Reserved for future expansion

DISALE Disable/Enable ALE

DISALE Operating Mode

0 ALE is emitted at a constant rate of 1/6 the oscillator frequency

1 ALE is active only during a MOVX or MOVC instruction

DISRTO Disable/Enable Reset out

DISRTO

0 Reset pin is driven High after WDT times out

1 Reset pin is input only

WDIDLE Disable/Enable WDT in IDLE mode

WDIDLE

0 WDT continues to count in IDLE mode

1 WDT halts counting in IDLE mode

Dual Data Pointer Registers: To facilitate accessing both internal and external data memory, two banks of 16-bit Data Pointer Registers are provided: DP0 at SFR address locations 82H-83H and DP1 at 84H-85H. Bit DPS = 0 in SFR AUXR1 selects DP0 and DPS = 1 selects DP1. The user should always initialize the DPS bit to the appropriate value before accessing the respective Data Pointer Register.

Power Off Flag: The Power Off Flag (POF) is located at bit 4 (PCON.4) in the PCON SFR. POF is set to "1" during power up. It can be set and rest under software control and is not affected by reset.

Table 3. AUXR1: Auxiliary Register 1

AUXR1

Address = A2H

Reset Value = XXXXXXX0B

Not Bit Addressable

	–	–	–	–	–	–	–	DPS
Bit	7	6	5	4	3	2	1	0

– Reserved for future expansion

DPS Data Pointer Register Select

DPS	
0	Selects DPTR Registers DP0L, DP0H
1	Selects DPTR Registers DP1L, DP1H

Memory Organization

MCS-51 devices have a separate address space for Program and Data Memory. Up to 64K bytes each of external Program and Data Memory can be addressed.

Program Memory

If the $\overline{EA}$ pin is connected to GND, all program fetches are directed to external memory.

On the AT89S51, if $\overline{EA}$ is connected to V_{CC}, program fetches to addresses 0000H through FFFH are directed to internal memory and fetches to addresses 1000H through FFFFH are directed to external memory.

Data Memory

The AT89S51 implements 128 bytes of on-chip RAM. The 128 bytes are accessible via direct and indirect addressing modes. Stack operations are examples of indirect addressing, so the 128 bytes of data RAM are available as stack space.

Watchdog Timer (One-time Enabled with Reset-out)

The WDT is intended as a recovery method in situations where the CPU may be subjected to software upsets. The WDT consists of a 14-bit counter and the Watchdog Timer Reset (WDTRST) SFR. The WDT is defaulted to disable from exiting reset. To enable the WDT, a user must write 01EH and 0E1H in sequence to the WDTRST register (SFR location 0A6H). When the WDT is enabled, it will increment every machine cycle while the oscillator is running. The WDT timeout period is dependent on the external clock frequency. There is no way to disable the WDT except through reset (either hardware reset or WDT overflow reset). When WDT overflows, it will drive an output RESET HIGH pulse at the RST pin.

Using the WDT

To enable the WDT, a user must write 01EH and 0E1H in sequence to the WDTRST register (SFR location 0A6H). When the WDT is enabled, the user needs to service it by writing 01EH and 0E1H to WDTRST to avoid a WDT overflow. The 14-bit counter overflows when it reaches 16383 (3FFFH), and this will reset the device. When the WDT is enabled, it will increment every machine cycle while the oscillator is running. This means the user must reset the WDT at least every 16383 machine cycles. To reset the WDT the user must write 01EH and 0E1H to WDTRST. WDTRST is a write-only register. The WDT counter cannot be read or written. When WDT overflows, it will generate an output RESET pulse at the RST pin. The RESET pulse duration is 98xTOSC, where TOSC=1/FOSC. To make the best use of the WDT, it

should be serviced in those sections of code that will periodically be executed within the time required to prevent a WDT reset.

WDT During Power-down and Idle

In Power-down mode the oscillator stops, which means the WDT also stops. While in Power-down mode, the user does not need to service the WDT. There are two methods of exiting Power-down mode: by a hardware reset or via a level-activated external interrupt, which is enabled prior to entering Power-down mode. When Power-down is exited with hardware reset, servicing the WDT should occur as it normally does whenever the AT89S51 is reset. Exiting Power-down with an interrupt is significantly different. The interrupt is held low long enough for the oscillator to stabilize. When the interrupt is brought high, the interrupt is serviced. To prevent the WDT from resetting the device while the interrupt pin is held low, the WDT is not started until the interrupt is pulled high. It is suggested that the WDT be reset during the interrupt service for the interrupt used to exit Power-down mode.

To ensure that the WDT does not overflow within a few states of exiting Power-down, it is best to reset the WDT just before entering Power-down mode.

Before going into the IDLE mode, the WDIDLE bit in SFR AUXR is used to determine whether the WDT continues to count if enabled. The WDT keeps counting during IDLE (WDIDLE bit = 0) as the default state. To prevent the WDT from resetting the AT89S51 while in IDLE mode, the user should always set up a timer that will periodically exit IDLE, service the WDT, and reenter IDLE mode.

With WDIDLE bit enabled, the WDT will stop to count in IDLE mode and resumes the count upon exit from IDLE.

UART

The UART in the AT89S51 operates the same way as the UART in the AT89C51. For further information on the UART operation, refer to the ATMEL Web site (http://www.atmel.com). From the home page, select 'Products', then '8051-Architecture Flash Microcontroller', then 'Product Overview'.

Timer 0 and 1

Timer 0 and Timer 1 in the AT89S51 operate the same way as Timer 0 and Timer 1 in the AT89C51. For further information on the timers' operation, refer to the ATMEL Web site (http://www.atmel.com). From the home page, select 'Products', then '8051-Architecture Flash Microcontroller', then 'Product Overview'.

Interrupts

The AT89S51 has a total of five interrupt vectors: two external interrupts ($\overline{INT0}$ and $\overline{INT1}$), two timer interrupts (Timers 0 and 1), and the serial port interrupt. These interrupts are all shown in Figure 1.

Each of these interrupt sources can be individually enabled or disabled by setting or clearing a bit in Special Function Register IE. IE also contains a global disable bit, EA, which disables all interrupts at once.

Note that Table 4 shows that bit position IE.6 is unimplemented. In the AT89S51, bit position IE.5 is also unimplemented. User software should not write 1s to these bit positions, since they may be used in future AT89 products.

The Timer 0 and Timer 1 flags, TF0 and TF1, are set at S5P2 of the cycle in which the timers overflow. The values are then polled by the circuitry in the next cycle

Table 4. Interrupt Enable (IE) Register

(MSB) (LSB)

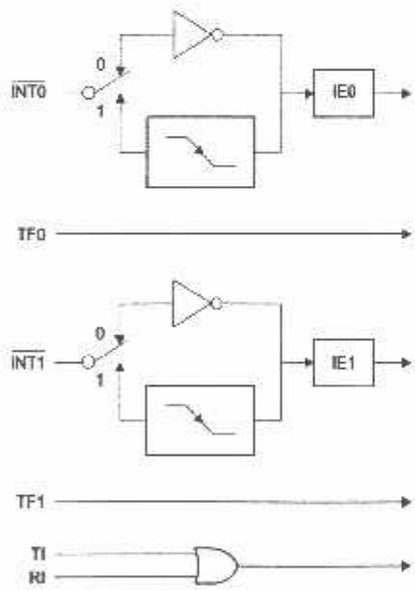
EA	–	–	ES	ET1	EX1	ET0	EX0

Enable Bit = 1 enables the interrupt.

Enable Bit = 0 disables the interrupt.

Symbol	Position	Function
EA	IE.7	Disables all interrupts. If EA = 0, no interrupt is acknowledged. If EA = 1, each interrupt source is individually enabled or disabled by setting or clearing its enable bit.
–	IE.6	Reserved
–	IE.5	Reserved
ES	IE.4	Serial Port interrupt enable bit
ET1	IE.3	Timer 1 interrupt enable bit
EX1	IE.2	External interrupt 1 enable bit
ET0	IE.1	Timer 0 interrupt enable bit
EX0	IE.0	External interrupt 0 enable bit
User software should never write 1s to reserved bits, because they may be used in future AT89 products.		

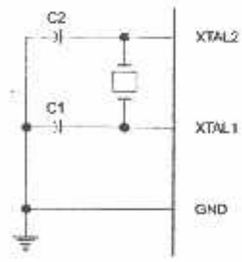
Figure 1. Interrupt Sources



Oscillator Characteristics

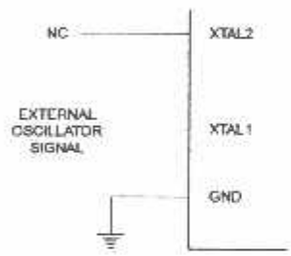
XTAL1 and XTAL2 are the input and output, respectively, of an inverting amplifier that can be configured for use as an on-chip oscillator, as shown in Figure 2. Either a quartz crystal or ceramic resonator may be used. To drive the device from an external clock source, XTAL2 should be left unconnected while XTAL1 is driven, as shown in Figure 3. There are no requirements on the duty cycle of the external clock signal, since the input to the internal clocking circuitry is through a divide-by-two flip-flop, but minimum and maximum voltage high and low time specifications must be observed.

Figure 2. Oscillator Connections



Note: C1, C2 = 30 pF ± 10 pF for Crystals = 40 pF ± 10 pF for Ceramic Resonators

Figure 3. External Clock Drive Configuration



Idle Mode

In idle mode, the CPU puts itself to sleep while all the on-chip peripherals remain active. The mode is invoked by software. The content of the on-chip RAM and all the special function registers remain unchanged during this mode. The idle mode can be terminated by any enabled interrupt or by a hardware reset.

Note that when idle mode is terminated by a hardware reset, the device normally resumes program execution from where it left off, up to two machine cycles before the internal reset algorithm takes control. On-chip hardware inhibits access to internal RAM in this event, but access to the port pins is not inhibited. To eliminate the possibility of an unexpected write to a port pin when idle mode is terminated by a reset, the instruction following the one that invokes idle mode should not write to a port pin or to external memory.

Power-down Mode

In the Power-down mode, the oscillator is stopped, and the instruction that invokes Power-down is the last instruction executed. The on-chip RAM and Special Function Registers retain their values until the Power-down mode is terminated. Exit from Power-down mode can be initiated either by a hardware reset or by activation of an enabled external interrupt into $\overline{INT0}$ or $\overline{INT1}$. Reset redefines the SFRs but does not change the on-chip RAM. The reset should not be activated before V_{CC} is restored to its normal operating level and must be held active long enough to allow the oscillator to restart and stabilize.

Table 5. Status of External Pins During Idle and Power-down Modes

Mode	Program Memory	ALE	$\overline{PSEN}$	PORT0	PORT1	PORT2	PORT3
Idle	Internal	1	1	Data	Data	Data	Data
Idle	External	1	1	Float	Data	Address	Data
Power-down	Internal	0	0	Data	Data	Data	Data
Power-down	External	0	0	Float	Data	Data	Data

Program Memory Lock Bits

The AT89S51 has three lock bits that can be left unprogrammed (U) or can be programmed (P) to obtain the additional features listed in the following table.

Table 6. Lock Bit Protection Modes

Program Lock Bits				
	LB1	LB2	LB3	Protection Type
1	U	U	U	No program lock features
2	P	U	U	MOVC instructions executed from external program memory are disabled from fetching code bytes from internal memory, $\overline{EA}$ is sampled and latched on reset, and further programming of the Flash memory is disabled
3	P	P	U	Same as mode 2, but verify is also disabled
4	P	P	P	Same as mode 3, but external execution is also disabled

When lock bit 1 is programmed, the logic level at the $\overline{EA}$ pin is sampled and latched during reset. If the device is powered up without a reset, the latch initializes to a random value and holds that value until reset is activated. The latched value of $\overline{EA}$ must agree with the current logic level at that pin in order for the device to function properly.

Programming the Flash – Parallel Mode

The AT89S51 is shipped with the on-chip Flash memory array ready to be programmed. The programming interface needs a high-voltage (12-volt) program enable signal and is compatible with conventional third-party Flash or EPROM programmers.

The AT89S51 code memory array is programmed byte-by-byte.

Programming Algorithm: Before programming the AT89S51, the address, data, and control signals should be set up according to the Flash programming mode table and Figures 13 and 14. To program the AT89S51, take the following steps:

1. Input the desired memory location on the address lines.
2. Input the appropriate data byte on the data lines.
3. Activate the correct combination of control signals.
4. Raise $\overline{EA}/V_{PP}$ to 12V.
5. Pulse ALE/$\overline{PROG}$ once to program a byte in the Flash array or the lock bits. The byte-write cycle is self-timed and typically takes no more than 50 µs. Repeat steps 1 through 5, changing the address and data for the entire array or until the end of the object file is reached.

$\overline{Data}$ Polling: The AT89S51 features $\overline{Data}$ Polling to indicate the end of a byte write cycle. During a write cycle, an attempted read of the last byte written will result in the complement of the written data on P0.7. Once the write cycle has been completed, true data is valid on all outputs, and the next cycle may begin. $\overline{Data}$ Polling may begin any time after a write cycle has been initiated.

Ready/$\overline{\text{Busy}}$: The progress of byte programming can also be monitored by the RDY/$\overline{\text{BSY}}$ output signal. P3.0 is pulled low after ALE goes high during programming to indicate $\overline{\text{BUSY}}$. P3.0 is pulled high again when programming is done to indicate READY.

Program Verify: If lock bits LB1 and LB2 have not been programmed, the programmed code data can be read back via the address and data lines for verification. The status of the individual lock bits can be verified directly by reading them back.

Reading the Signature Bytes: The signature bytes are read by the same procedure as a normal verification of locations 000H, 100H, and 200H, except that P3.6 and P3.7 must be pulled to a logic low. The values returned are as follows.

(000H) = 1EH indicates manufactured by Atmel
(100H) = 51H indicates 89S51
(200H) = 06H

Chip Erase: In the parallel programming mode, a chip erase operation is initiated by using the proper combination of control signals and by pulsing ALE/$\overline{\text{PROG}}$ low for a duration of 200 ns - 500 ns.

In the serial programming mode, a chip erase operation is initiated by issuing the Chip Erase instruction. In this mode, chip erase is self-timed and takes about 500 ms.

During chip erase, a serial read from any address location will return 00H at the data output.

Programming the Flash – Serial Mode

The Code memory array can be programmed using the serial ISP interface while RST is pulled to V_{CC}. The serial interface consists of pins SCK, MOSI (input) and MISO (output). After RST is set high, the Programming Enable instruction needs to be executed first before other operations can be executed. Before a reprogramming sequence can occur, a Chip Erase operation is required.

The Chip Erase operation turns the content of every memory location in the Code array into FFH.

Either an external system clock can be supplied at pin XTAL1 or a crystal needs to be connected across pins XTAL1 and XTAL2. The maximum serial clock (SCK) frequency should be less than 1/16 of the crystal frequency. With a 33 MHz oscillator clock, the maximum SCK frequency is 2 MHz.

Serial Programming Algorithm

To program and verify the AT89S51 in the serial programming mode, the following sequence is recommended:

1. Power-up sequence:
   Apply power between VCC and GND pins.
   Set RST pin to "H".
   If a crystal is not connected across pins XTAL1 and XTAL2, apply a 3 MHz to 33 MHz clock to XTAL1 pin and wait for at least 10 milliseconds.
2. Enable serial programming by sending the Programming Enable serial instruction to pin MOSI/P1.5. The frequency of the shift clock supplied at pin SCK/P1.7 needs to be less than the CPU clock at XTAL1 divided by 16.
3. The Code array is programmed one byte at a time in either the Byte or Page mode. The write cycle is self-timed and typically takes less than 0.5 ms at 5V.
4. Any memory location can be verified by using the Read instruction that returns the content at the selected address at serial output MISO/P1.6.
5. At the end of a programming session, RST can be set low to commence normal device operation.

Power-off sequence (if needed):

Set XTAL1 to "L" (if a crystal is not used).

Set RST to "L".

Turn V_{CC} power off.

Data Polling: The Data Polling feature is also available in the serial mode. In this mode, during a write cycle an attempted read of the last byte written will result in the complement of the MSB of the serial output byte on MISO.

Serial Programming Instruction Set

The Instruction Set for Serial Programming follows a 4-byte protocol and is shown in Table 8 on page 18.

Programming Interface – Parallel Mode

Every code byte in the Flash array can be programmed by using the appropriate combination of control signals. The write operation cycle is self-timed and once initiated, will automatically time itself to completion.

All major programming vendors offer worldwide support for the Atmel microcontroller series. Please contact your local programming vendor for the appropriate software revision.

Table 7. Flash Programming Modes

Mode	V_{CC}	RST	PSEN	ALE/ PROG	EA/ V_{PP}	P2.6	P2.7	P3.3	P3.6	P3.7	P0.7-0 Data	P2.3-0 Address	P1.7-0 Address
Write Code Data	5V	H	L	(2)	12V	L	H	H	H	H	D_{IN}	A11-8	A7-0
Read Code Data	5V	H	L	H	H	L	L	L	H	H	D_{OUT}	A11-8	A7-0
Write Lock Bit 1	5V	H	L	(3)	12V	H	H	H	H	H	X	X	X
Write Lock Bit 2	5V	H	L	(3)	12V	H	H	H	L	L	X	X	X
Write Lock Bit 3	5V	H	L	(3)	12V	H	L	H	H	L	X	X	X
Read Lock Bits 1, 2, 3	5V	H	L	H	H	H	H	L	H	L	P0.2, P0.3, P0.4	X	X
Chip Erase	5V	H	L	(1)	12V	H	L	H	L	L	X	X	X
Read Atmel ID	5V	H	L	H	H	L	L	L	L	L	1EH	0000	00H
Read Device ID	5V	H	L	H	H	L	L	L	L	L	51H	0001	00H
Read Device ID	5V	H	L	H	H	L	L	L	L	L	06H	0010	00H

Notes:
1. Each PROG pulse is 200 ns - 500 ns for Chip Erase.
2. Each PROG pulse is 200 ns - 500 ns for Write Code Data.
3. Each PROG pulse is 200 ns - 500 ns for Write Lock Bits.
4. RDY/BSY signal is output on P3.0 during programming.
5. X = don't care.

Figure 4. Programming the Flash Memory (Parallel Mode)

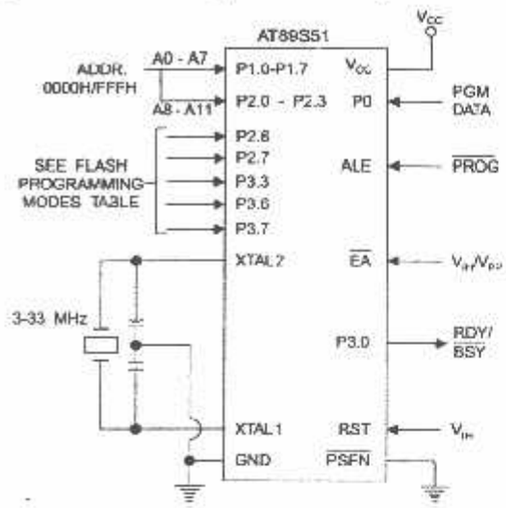
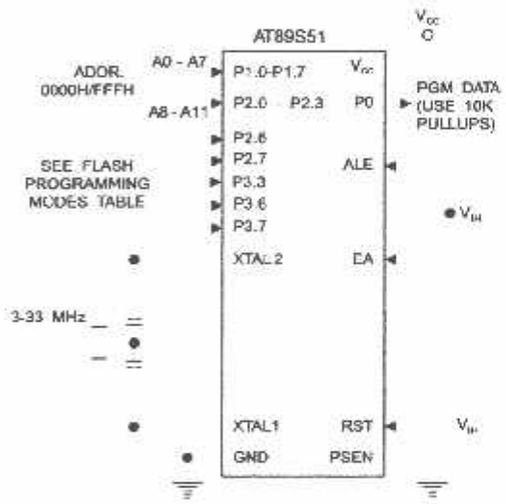


Figure 5. Verifying the Flash Memory (Parallel Mode)



Flash Programming and Verification Characteristics (Parallel Mode)

T_A = 20°C to 30°C, V_{CC} = 4.5 to 5.5V

Symbol	Parameter	Min	Max	Units
V_{PP}	Programming Supply Voltage	11.5	12.5	V
I_{PP}	Programming Supply Current		10	mA
I_{CC}	V_{CC} Supply Current		30	mA
$1/t_{CLCL}$	Oscillator Frequency	3	33	MHz
t_{AVGL}	Address Setup to $\overline{PROG}$ Low	$48t_{CLCL}$		
t_{GHAX}	Address Hold After $\overline{PROG}$	$48t_{CLCL}$		
t_{DVGL}	Data Setup to $\overline{PROG}$ Low	$48t_{CLCL}$		
t_{GHDX}	Data Hold After $\overline{PROG}$	$48t_{CLCL}$		
t_{EHSH}	P2.7 ($\overline{ENABLE}$) High to V_{PP}	$48t_{CLCL}$		
t_{SHGL}	V_{PP} Setup to $\overline{PROG}$ Low	10		µs
t_{GHSL}	V_{PP} Hold After $\overline{PROG}$	10		µs
t_{GLGH}	$\overline{PROG}$ Width	0.2	1	µs
t_{AVQV}	Address to Data Valid		$48t_{CLCL}$	
t_{ELQV}	$\overline{ENABLE}$ Low to Data Valid		$48t_{CLCL}$	
t_{EHQZ}	Data Float After $\overline{ENABLE}$	0	$48t_{CLCL}$	
t_{GHBL}	$\overline{PROG}$ High to $\overline{BUSY}$ Low		1.0	µs
t_{WC}	Byte Write Cycle Time		50	µs

Figure 6. Flash Programming and Verification Waveforms – Parallel Mode

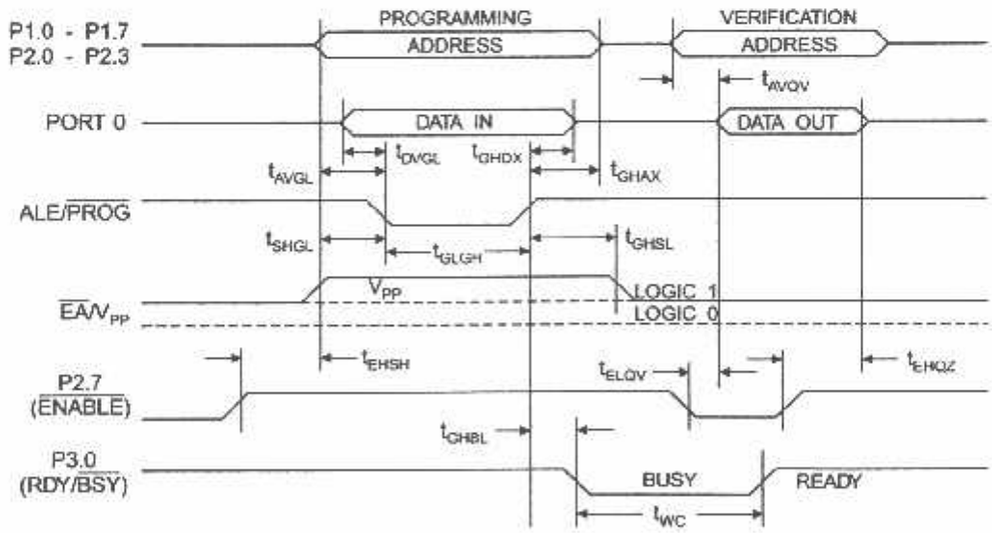
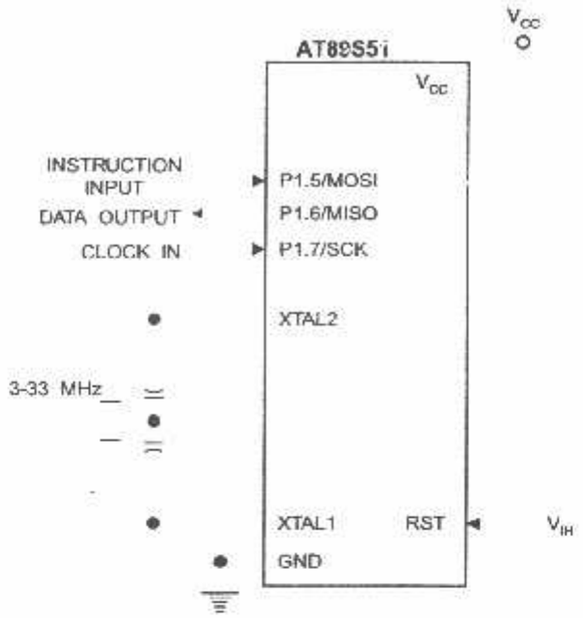


Figure 7. Flash Memory Serial Downloading



Flash Programming and Verification Waveforms – Serial Mode

Figure 8. Serial Programming Waveforms

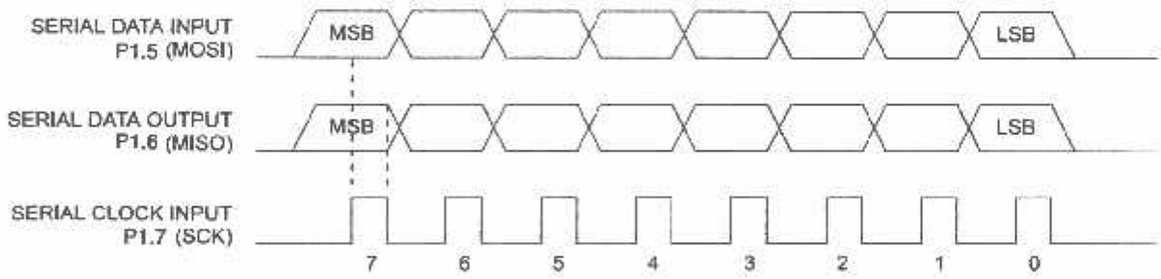


Table 8. Serial Programming Instruction Set

Instruction	Instruction Format Byte 1	Byte 2	Byte 3	Byte 4	Operation
Programming Enable	1010 1100	0101 0011	xxxx xxxx	xxxx xxxx 0110 1001 (Output)	Enable Serial Programming while RST is high
Chip Erase	1010 1100	100x xxxx	xxxx xxxx	xxxx xxxx	Chip Erase Flash memory array
Read Program Memory (Byte Mode)	0010 0000	xxxx A11 A10 A9 A8	A7 A6 A5 A4 A3 A2 A1 A0	D7 D6 D5 D4 D3 D2 D1 D0	Read data from Program memory in the byte mode
Write Program Memory (Byte Mode)	0100 0000	xxxx A11 A10 A9 A8	A7 A6 A5 A4 A3 A2 A1 A0	D7 D6 D5 D4 D3 D2 D1 D0	Write data to Program memory in the byte mode
Write Lock Bits[2]	1010 1100	1110 00 B1 B2	xxxx xxxx	xxxx xxxx	Write Lock bits. See Note (2).
Read Lock Bits	0010 0100	xxxx xxxx	xxxx xxxx	xx LB3 LB2 LB1 xx	Read back current status of the lock bits (a programmed lock bit reads back as a "1")
Read Signature Bytes[1]	0010 1000	xxx A5 A4 A3 A2 A1	A0 xxx xxxx	Signature Byte	Read Signature Byte
Read Program Memory (Page Mode)	0011 0000	xxxx A11 A10 A9 A8	Byte 0	Byte 1... Byte 255	Read data from Program memory in the Page Mode (256 bytes)
Write Program Memory (Page Mode)	0101 0000	xxxx A11 A10 A9 A8	Byte 0	Byte 1... Byte 255	Write data to Program memory in the Page Mode (256 bytes)

Notes: 1. The signature bytes are not readable in Lock Bit Modes 3 and 4.

2. B1 = 0, B2 = 0 → Mode 1, no lock protection
   B1 = 0, B2 = 1 → Mode 2, lock bit 1 activated
   B1 = 1, B2 = 0 → Mode 3, lock bit 2 activated
   B1 = 1, B1 = 1 → Mode 4, lock bit 3 activated

   } Each of the lock bits needs to be activated sequentially before Mode 4 can be executed.

After Reset signal is high, SCK should be low for at least 64 system clocks before it goes high to clock in the enable data bytes. No pulsing of Reset signal is necessary. SCK should be no faster than 1/16 of the system clock at XTAL1.

For Page Read/Write, the data always starts from byte 0 to 255. After the command byte and upper address byte are latched, each byte thereafter is treated as data until all 256 bytes are shifted in/out. Then the next instruction will be ready to be decoded.

Serial Programming Characteristics

Figure 9. Serial Programming Timing

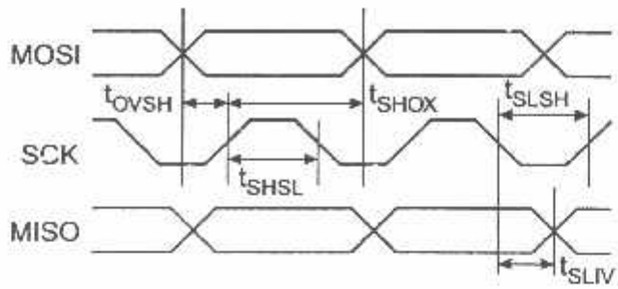


Table 9. Serial Programming Characteristics, T_A = -40° C to 85° C, V_{CC} = 4.0 - 5.5V (Unless Otherwise Noted)

Symbol	Parameter	Min	Typ	Max	Units
$1/t_{CLCL}$	Oscillator Frequency	0		33	MHz
t_{CLCL}	Oscillator Period	30			ns
t_{SHSL}	SCK Pulse Width High	8 t_{CLCL}			ns
t_{SLSH}	SCK Pulse Width Low	8 t_{CLCL}			ns
t_{OVSH}	MOSI Setup to SCK High	t_{CLCL}			ns
t_{SHOX}	MOSI Hold after SCK High	2 t_{CLCL}			ns
t_{SLIV}	SCK Low to MISO Valid	10	16	32	ns
t_{ERASE}	Chip Erase Instruction Cycle Time			500	ms
t_{SWC}	Serial Byte Write Cycle Time			64 t_{CLCL} + 400	µs

Absolute Maximum Ratings*

Operating Temperature	-55°C to +125°C
Storage Temperature	-65°C to +150°C
Voltage on Any Pin with Respect to Ground	-1.0V to +7.0V
Maximum Operating Voltage	6.6V
DC Output Current	15.0 mA

*NOTICE: Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC Characteristics

The values shown in this table are valid for T_A = -40°C to 85°C and V_{CC} = 4.0V to 5.5V, unless otherwise noted.

Symbol	Parameter	Condition	Min	Max	Units
V_{IL}	Input Low Voltage	(Except $\overline{EA}$)	-0.5	0.2 V_{CC}-0.1	V
V_{IL1}	Input Low Voltage ($\overline{EA}$)		-0.5	0.2 V_{CC}-0.3	V
V_{IH}	Input High Voltage	(Except XTAL1, RST)	0.2 V_{CC}+0.9	V_{CC}+0.5	V
V_{IH1}	Input High Voltage	(XTAL1, RST)	0.7 V_{CC}	V_{CC}+0.5	V
V_{OL}	Output Low Voltage[1] (Ports 1,2,3)	I_{OL} = 1.6 mA		0.45	V
V_{OL1}	Output Low Voltage[1] (Port 0, ALE, $\overline{PSEN}$)	I_{OL} = 3.2 mA		0.45	V
V_{OH}	Output High Voltage (Ports 1,2,3, ALE, $\overline{PSEN}$)	I_{OH} = -60 µA, V_{CC} = 5V ± 10%	2.4		V
		I_{OH} = -25 µA	0.75 V_{CC}		V
		I_{OH} = -10 µA	0.9 V_{CC}		V
V_{OH1}	Output High Voltage (Port 0 in External Bus Mode)	I_{OH} = -800 µA, V_{CC} = 5V ± 10%	2.4		V
		I_{OH} = -300 µA	0.75 V_{CC}		V
		I_{OH} = -80 µA	0.9 V_{CC}		V
I_{IL}	Logical 0 Input Current (Ports 1,2,3)	V_{IN} = 0.45V		-50	µA
I_{TL}	Logical 1 to 0 Transition Current (Ports 1,2,3)	V_{IN} = 2V, V_{CC} = 5V ± 10%		-650	µA
I_{LI}	Input Leakage Current (Port 0, $\overline{EA}$)	0.45 < V_{IN} < V_{CC}		±10	µA
RRST	Reset Pulldown Resistor		50	300	KΩ
C_{IO}	Pin Capacitance	Test Freq. = 1 MHz, T_A = 25°C		10	pF
I_{CC}	Power Supply Current	Active Mode, 12 MHz		25	mA
		Idle Mode, 12 MHz		6.5	mA
	Power-down Mode[2]	V_{CC} = 5.5V		50	µA

Notes: 1. Under steady state (non-transient) conditions, I_{OL} must be externally limited as follows:
Maximum I_{OL} per port pin: 10 mA
Maximum I_{OL} per 8-bit port:
Port 0: 26 mA Ports 1, 2, 3: 15 mA
Maximum total I_{OL} for all output pins: 71 mA
If I_{OL} exceeds the test condition, V_{OL} may exceed the related specification. Pins are not guaranteed to sink current greater than the listed test conditions.
2. Minimum V_{CC} for Power-down is 2V.

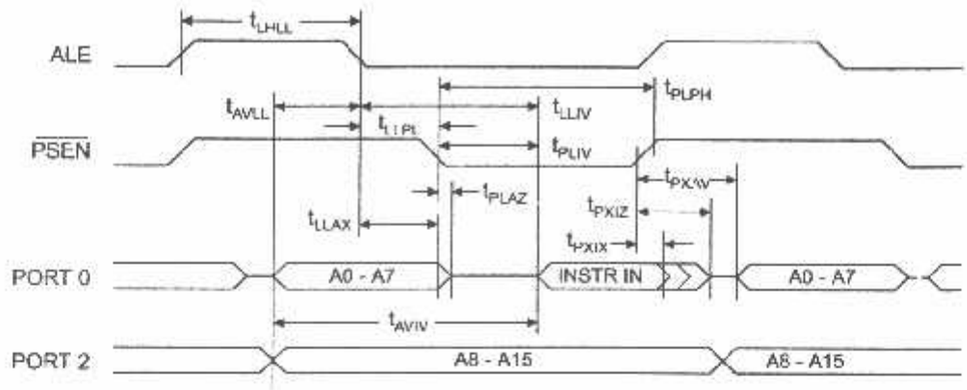
AC Characteristics

Under operating conditions, load capacitance for Port 0, ALE/$\overline{PROG}$, and $\overline{PSEN}$ = 100 pF; load capacitance for all other outputs = 80 pF.

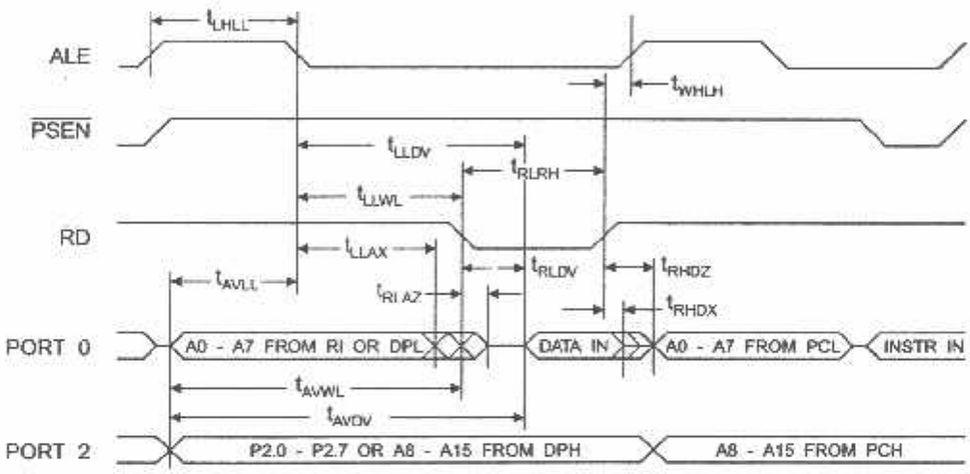
External Program and Data Memory Characteristics

Symbol	Parameter	12 MHz Oscillator		Variable Oscillator		Units
		Min	Max	Min	Max	
$1/t_{CLCL}$	Oscillator Frequency			0	33	MHz
t_{LHLL}	ALE Pulse Width	127		$2t_{CLCL}$-40		ns
t_{AVLL}	Address Valid to ALE Low	43		t_{CLCL}-25		ns
t_{LLAX}	Address Hold After ALE Low	48		t_{CLCL}-25		ns
t_{LLIV}	ALE Low to Valid Instruction In		233		$4t_{CLCL}$-65	ns
t_{LLPL}	ALE Low to $\overline{PSEN}$ Low	43		t_{CLCL}-25		ns
t_{PLPH}	$\overline{PSEN}$ Pulse Width	205		$3t_{CLCL}$-45		ns
t_{PLIV}	$\overline{PSEN}$ Low to Valid Instruction In		145		$3t_{CLCL}$-60	ns
t_{PXIX}	Input Instruction Hold After $\overline{PSEN}$	0		0		ns
t_{PXIZ}	Input Instruction Float After $\overline{PSEN}$		59		t_{CLCL}-25	ns
t_{PXAV}	$\overline{PSEN}$ to Address Valid	75		t_{CLCL}-8		ns
t_{AVIV}	Address to Valid Instruction In		312		$5t_{CLCL}$-80	ns
t_{PLAZ}	$\overline{PSEN}$ Low to Address Float		10		10	ns
t_{RLRH}	$\overline{RD}$ Pulse Width	400		$6t_{CLCL}$-100		ns
t_{WLWH}	$\overline{WR}$ Pulse Width	400		$6t_{CLCL}$-100		ns
t_{RLDV}	$\overline{RD}$ Low to Valid Data In		252		$5t_{CLCL}$-90	ns
t_{RHDX}	Data Hold After $\overline{RD}$	0		0		ns
t_{RHDZ}	Data Float After $\overline{RD}$		97		$2t_{CLCL}$-28	ns
t_{LLDV}	ALE Low to Valid Data In		517		$8t_{CLCL}$-150	ns
t_{AVDV}	Address to Valid Data In		585		$9t_{CLCL}$-165	ns
t_{LLWL}	ALE Low to $\overline{RD}$ or $\overline{WR}$ Low	200	300	$3t_{CLCL}$-50	$3t_{CLCL}$+50	ns
t_{AVWL}	Address to $\overline{RD}$ or $\overline{WR}$ Low	203		$4t_{CLCL}$-75		ns
t_{QVWX}	Data Valid to $\overline{WR}$ Transition	23		t_{CLCL}-30		ns
t_{QVWH}	Data Valid to $\overline{WR}$ High	433		$7t_{CLCL}$-130		ns
t_{WHQX}	Data Hold After $\overline{WR}$	33		t_{CLCL}-25		ns
t_{RLAZ}	$\overline{RD}$ Low to Address Float		0		0	ns
t_{WHLH}	$\overline{RD}$ or $\overline{WR}$ High to ALE High	43	123	t_{CLCL}-25	t_{CLCL}+25	ns

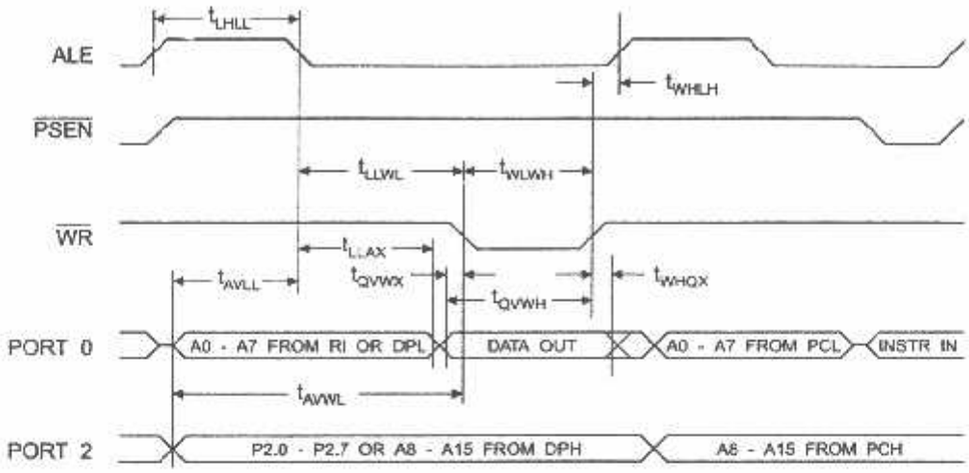
External Program Memory Read Cycle



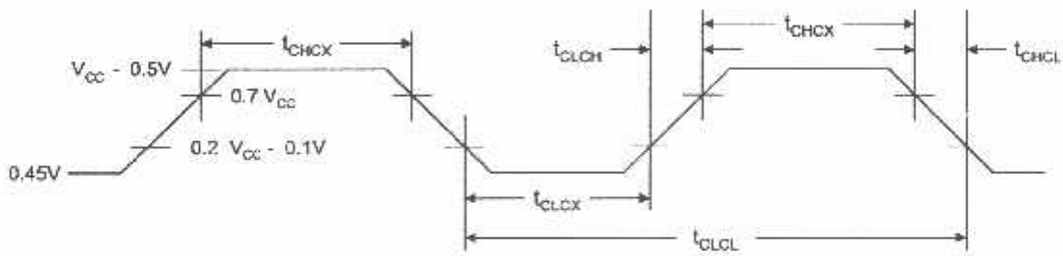
External Data Memory Read Cycle



External Data Memory Write Cycle



External Clock Drive Waveforms



External Clock Drive

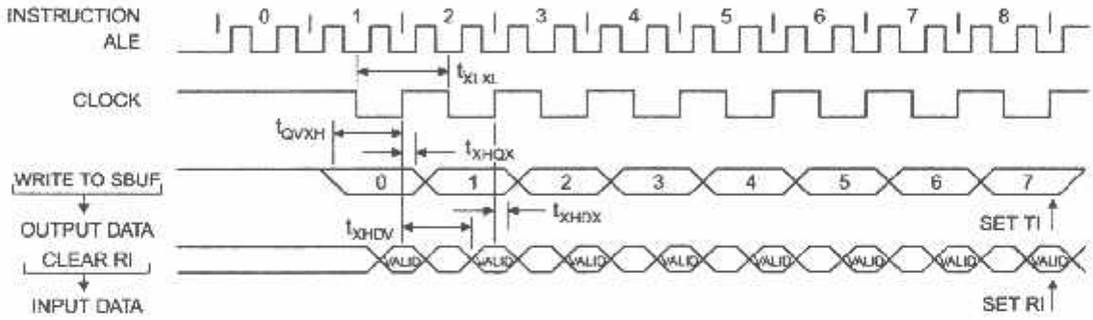
Symbol	Parameter	Min	Max	Units
$1/t_{CLCL}$	Oscillator Frequency	0	33	MHz
t_{CLCL}	Clock Period	30		ns
t_{CHCX}	High Time	12		ns
t_{CLCX}	Low Time	12		ns
t_{CLCH}	Rise Time		5	ns
t_{CHCL}	Fall Time		5	ns

Serial Port Timing: Shift Register Mode Test Conditions

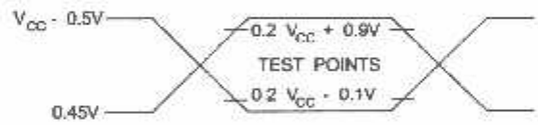
The values in this table are valid for V_{CC} = 4.0V to 5.5V and Load Capacitance = 80 pF.

Symbol	Parameter	12 MHz Osc		Variable Oscillator		Units
		Min	Max	Min	Max	
t_{XLXL}	Serial Port Clock Cycle Time	1.0		$12t_{CLCL}$		µs
t_{QVXH}	Output Data Setup to Clock Rising Edge	700		$10t_{CLCL}$-133		ns
t_{XHQX}	Output Data Hold After Clock Rising Edge	50		$2t_{CLCL}$-80		ns
t_{XHDX}	Input Data Hold After Clock Rising Edge	0		0		ns
t_{XHDV}	Clock Rising Edge to Input Data Valid		700		$10t_{CLCL}$-133	ns

Shift Register Mode Timing Waveforms

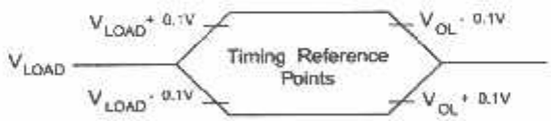


AC Testing Input/Output Waveforms[1]



Note: 1. AC Inputs during testing are driven at V_{CC} - 0.5V for a logic 1 and 0.45V for a logic 0. Timing measurements are made at V_{IH} min. for a logic 1 and V_{IL} max. for a logic 0.

Float Waveforms[1]



Note: 1. For timing purposes, a port pin is no longer floating when a 100 mV change from load voltage occurs. A port pin begins to float when a 100 mV change from the loaded V_{OH}/V_{OL} level occurs.

Ordering Information

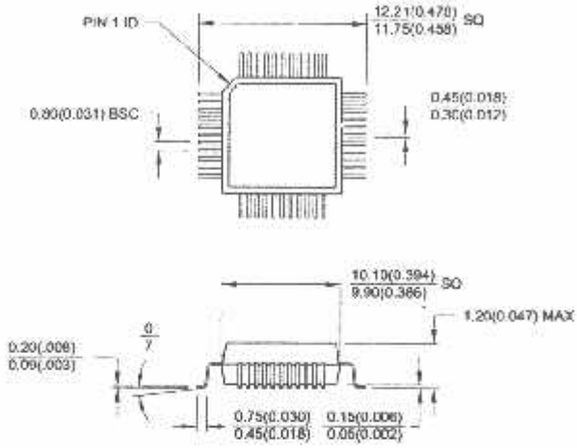
Speed (MHz)	Power Supply	Ordering Code	Package	Operation Range
24	4.0V to 5.5V	AT89S51-24AC AT89S51-24JC AT89S51-24PC	44A 44J 40P6	Commercial (0° C to 70° C)
		AT89S51-24AI AT89S51-24JI AT89S51-24PI	44A 44J 40P6	Industrial (-40° C to 85° C)
33	4.5V to 5.5V	AT89S51-33AC AT89S51-33JC AT89S51-33PC	44A 44J 40P6	Commercial (0° C to 70° C)

[ ] = Preliminary Availability

Package Type	
44A	44-lead, Thin Plastic Gull Wing Quad Flatpack (TQFP)
44J	44-lead, Plastic J-leaded Chip Carrier (PLCC)
40P6	40-pin, 0.600" Wide, Plastic Dual Inline Package (PDIP)

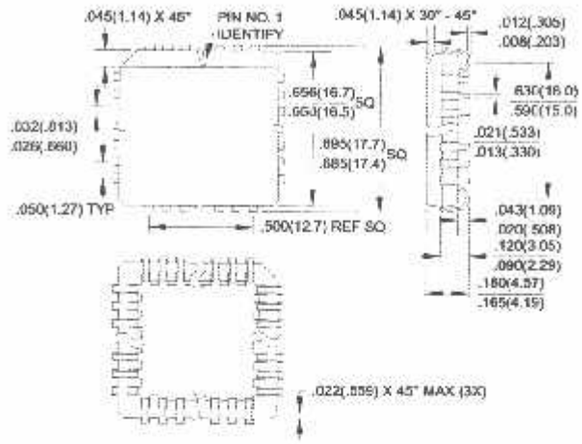
Packaging Information

44A, 44-lead, Thin (1.0 mm) Plastic Gull Wing Quad Flat Package (TQFP)
Dimensions in Millimeters and (Inches)*

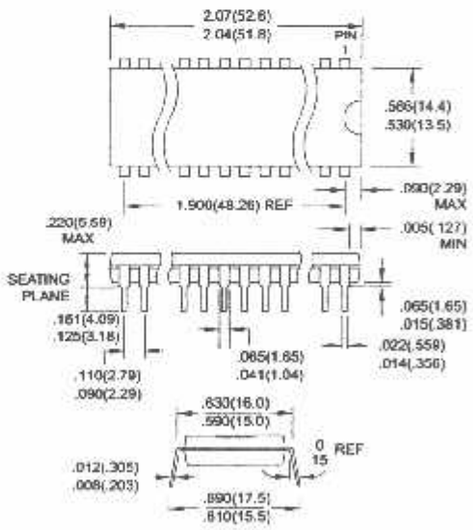


*Controlling dimension: millimeters

44J, 44-lead, Plastic J-leaded Chip Carrier (PLCC)
Dimensions in Inches and (Millimeters)



40P6, 40-pin, 0.600" Wide, Plastic Dual Inline Package (PDIP)
Dimensions in Inches and (Millimeters)
JEDEC STANDARD MS-011 AC



Features

- Low-Voltage and Standard-Voltage Operation
  - 5.0 (V_{CC} = 4.5V to 5.5V)
  - 2.7 (V_{CC} = 2.7V to 5.5V)
  - 2.5 (V_{CC} = 2.5V to 5.5V)
  - 1.8 (V_{CC} = 1.8V to 5.5V)
- Low-Power Devices (I_{SB} = 2 µA @ 5.5V) Available
- Internally Organized 4096 x 8, 8192 x 8
- 2-Wire Serial Interface
- Schmitt Trigger, Filtered Inputs for Noise Suppression
- Bidirectional Data Transfer Protocol
- 100 kHz (1.8V, 2.5V, 2.7V) and 400 kHz (5V) Compatibility
- Write Protect Pin for Hardware Data Protection
- 32-Byte Page Write Mode (Partial Page Writes Allowed)
- Self-Timed Write Cycle (10 ms max)
- High Reliability
  - Endurance: 1 Million Write Cycles
  - Data Retention: 100 Years
  - ESD Protection: >3,000V
- Automotive Grade and Extended Temperature Devices Available
- 8-Pin JEDEC PDIP, 8-Pin and 14-Pin JEDEC SOIC, 8-Pin EIAJ SOIC, and 8-pin TSSOP Packages

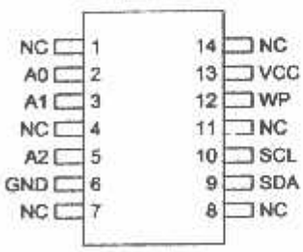
Description

The AT24C32/64 provides 32,768/65,536 bits of serial electrically erasable and programmable read only memory (EEPROM) organized as 4096/8192 words of 8 bits each. The device's cascadable feature allows up to 8 devices to share a common 2-wire bus. The device is optimized for use in many industrial and commercial applications where low power and low voltage operation are essential. The AT24C32/64 is available in space saving 8-pin JEDEC PDIP, 8-pin and 14-pin JEDEC SOIC, 8-pin EIAJ SOIC, and 8-pin TSSOP packages and is accessed via a 2-wire serial interface. In addition, the entire family is available in 5.0V (4.5V to 5.5V), 2.7V (2.7V to 5.5V), 2.5V (2.5V to 5.5V) and 1.8V (1.8V to 5.5V) versions.

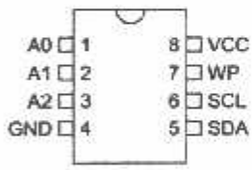
Pin Configurations

Pin Name	Function
A0 to A2	Address Inputs
SDA	Serial Data
SCL	Serial Clock Input
WP	Write Protect

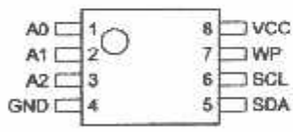
14-Pin SOIC



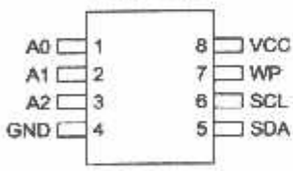
8-Pin PDIP



8-Pin TSSOP



8-Pin SOIC



2-Wire Serial EEPROM

32K (4096 x 8)

64K (8192 x 8)

AT24C32
AT24C64

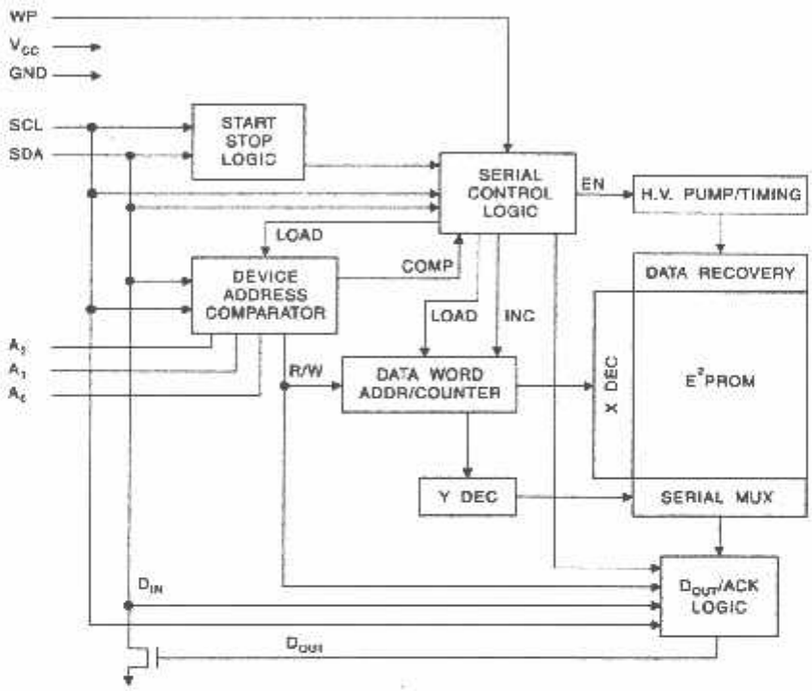
Rev. 0336F–08/98

Absolute Maximum Ratings*

Operating Temperature	-55°C to +125°C
Storage Temperature	-65°C to +150°C
Voltage on Any Pin with Respect to Ground	-1.0V to +7.0V
Maximum Operating Voltage	6.25V
DC Output Current	5.0 mA

*NOTICE: Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Block Diagram



Pin Description

SERIAL CLOCK (SCL): The SCL input is used to positive edge clock data into each EEPROM device and negative edge clock data out of each device.

SERIAL DATA (SDA): The SDA pin is bidirectional for serial data transfer. This pin is open-drain driven and may be wire-ORed with any number of other open-drain or open collector devices.

DEVICE/PAGE ADDRESSES (A2, A1, A0): The A2, A1 and A0 pins are device address inputs that are hard wired or left not connected for hardware compatibility with AT24C16. When the pins are hardwired, as many as eight 32K/64K devices may be addressed on a single bus system (device addressing is discussed in detail under the Device Addressing section). When the pins are not hardwired, the default A_2, A_1, and A_0 are zero.

WRITE PROTECT (WP): The write protect input, when tied to GND, allows normal write operations. When WP is tied high to V_{CC}, all write operations to the upper quandrant (8/16K bits) of memory are inhibited. If left unconnected, WP is internally pulled down to GND.

Memory Organization

AT24C32/64, 32K/64K SERIAL EEPROM: The 32K/64K is internally organized as 256 pages of 32 bytes each. Random word addressing requires a 12/13 bit data word address.

Pin Capacitance[1]

Applicable over recommended operating range from T_A = 25°C, f = 1.0 MHz, V_{CC} = +1.8V.

Symbol	Test Condition	Max	Units	Conditions
$C_{I/O}$	Input/Output Capacitance (SDA)	8	pF	$V_{I/O}$ = 0V
C_{IN}	Input Capacitance (A_0, A_1, A_2, SCL)	6	pF	V_{IN} = 0V

Note: 1. This parameter is characterized and is not 100% tested.

DC Characteristics

Applicable over recommended operating range from: T_{AI} = -40°C to +85°C, V_{CC} = +1.8V to +5.5V, T_{AC} = 0°C to +70°C, V_{CC} = +1.8V to +5.5V (unless otherwise noted).

Symbol	Parameter		Test Condition	Min	Typ	Max	Units
V_{CC1}	Supply Voltage			1.8		5.5	V
V_{CC2}	Supply Voltage			2.5		5.5	V
V_{CC3}	Supply Voltage			2.7		5.5	V
V_{CC4}	Supply Voltage			4.5		5.5	V
I_{CC1}	Supply Current V_{CC} = 5.0V		READ at 100 kHz		0.4	1.0	mA
I_{CC2}	Supply Current V_{CC} = 5.0V		WRITE at 100 kHz		2.0	3.0	mA
I_{SB1}	Standby Current (1.8V option)	V_{CC} = 1.8V	V_{IN} = V_{CC} or V_{SS}			0.1	µA
		V_{CC} = 5.5V				2.0	
I_{SB2}	Standby Current (2.5V option)	V_{CC} = 2.5V	V_{IN} = V_{CC} or V_{SS}			0.5	µA
		V_{CC} = 5.5V				2.0	
I_{SB3}	Standby Current (2.7V option)	V_{CC} = 2.7V	V_{IN} = V_{CC} or V_{SS}			0.5	µA
		V_{CC} = 5.5V				2.0	
I_{SB4}	Standby Current (5V option)	V_{CC} = 4.5 - 5.5V	V_{IN} = V_{CC} or V_{SS}		20	35	µA
I_{LI}	Input Leakage Current		V_{IN} = V_{CC} or V_{SS}		0.10	3.0	µA
I_{LO}	Output Leakage Current		V_{OUT} = V_{CC} or V_{SS}		0.05	3.0	µA
V_{IL}	Input Low Level[1]			-0.6		V_{CC} x 0.3	V
V_{IH}	Input High Level[1]			V_{CC} x 0.7		V_{CC} + 0.5	V
V_{OL2}	Output Low Level V_{CC} = 3.0V		I_{OL} = 2.1 mA			0.4	V
V_{OL1}	Output Low Level V_{CC} = 1.8V		I_{OL} = 0.15 mA			0.2	V

Notes: 1. V_{IL} min and V_{IH} max are reference only and are not tested.

AC Characteristics

Applicable over recommended operating range from T_A = -40°C to +85°C, V_{CC} = +1.8V to +5.5V, CL = 1 TTL Gate and 100 pF (unless otherwise noted).

Symbol	Parameter	1.8-volt		2.7-, 2.5-volt		5.0-volt		Units
		Min	Max	Min	Max	Min	Max	
f_{SCL}	Clock Frequency, SCL		100		100		400	kHz
t_{LOW}	Clock Pulse Width Low	4.7		4.7		1.2		µs
t_{HIGH}	Clock Pulse Width High	4.0		4.0		0.6		µs
t_I	Noise Suppression Time[1]		100		100		50	ns
t_{AA}	Clock Low to Data Out Valid	0.1	4.5	0.1	4.5	0.1	0.9	µs
t_{BUF}	Time the bus must be free before a new transmission can start[1]	4.7		4.7		1.2		µs
$t_{HD.STA}$	Start Hold Time	4.0		4.0		0.6		µs
$t_{SU.STA}$	Start Set-up Time	4.7		4.7		0.6		µs
$t_{HD.DAT}$	Data In Hold Time	0		0		0		µs
$t_{SU.DAT}$	Data In Set-up Time	200		200		100		ns
t_R	Inputs Rise Time[1]		1.0		1.0		0.3	µs
t_F	Inputs Fall Time[1]		300		300		300	ns
$t_{SU.STO}$	Stop Set-up Time	4.7		4.7		0.6		µs
t_{DH}	Data Out Hold Time	100		100		50		ns
t_{WR}	Write Cycle Time		20		10		10	ms
Endurance[1]	5.0V, 25°C, Page Mode	1M		1M		1M		Write Cycles

Note: 1. This parameter is characterized and is not 100% tested.

Device Operation

CLOCK and DATA TRANSITIONS: The SDA pin is normally pulled high with an external device. Data on the SDA pin may change only during SCL low time periods (refer to Data Validity timing diagram). Data changes during SCL high periods will indicate a start or stop condition as defined below.

START CONDITION: A high-to-low transition of SDA with SCL high is a start condition which must precede any other command (refer to Start and Stop Definition timing diagram).

STOP CONDITION: A low-to-high transition of SDA with SCL high is a stop condition. After a read sequence, the stop command will place the EEPROM in a standby power mode (refer to Start and Stop Definition timing diagram).

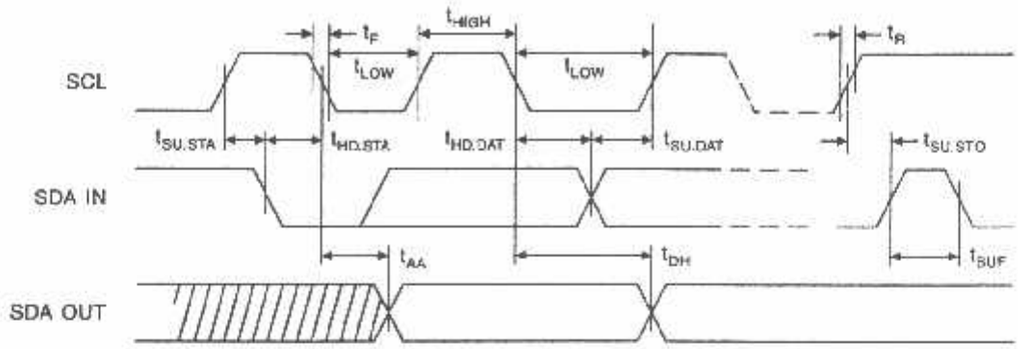
ACKNOWLEDGE: All addresses and data words are serially transmitted to and from the EEPROM in 8-bit words. The EEPROM sends a zero during the ninth clock cycle to acknowledge that it has received each word.

STANDBY MODE: The AT24C32/64 features a low power standby mode which is enabled: a) upon power-up and b) after the receipt of the STOP bit and the completion of any internal operations.

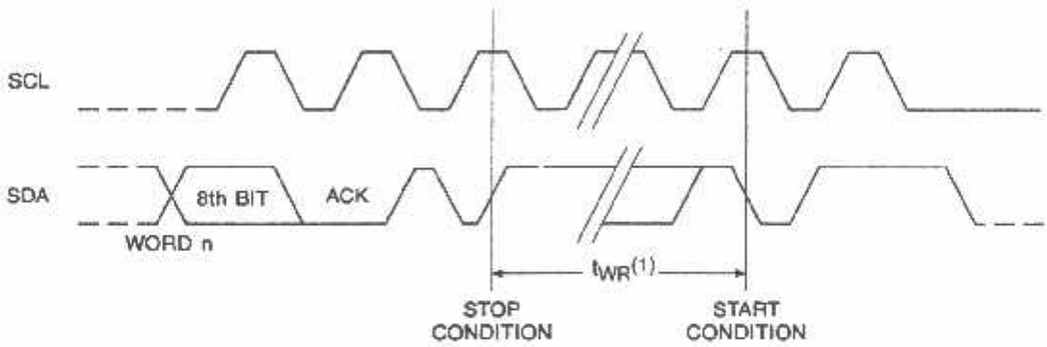
MEMORY RESET: After an interruption in protocol, power loss or system reset, any 2-wire part can be reset by following these steps:

(a) Clock up to 9 cycles, (b) look for SDA high in each cycle while SCL is high and then (c) create a start condition as SDA is high.

Bus Timing
SCL: Serial Clock, SDA: Serial Data I/O

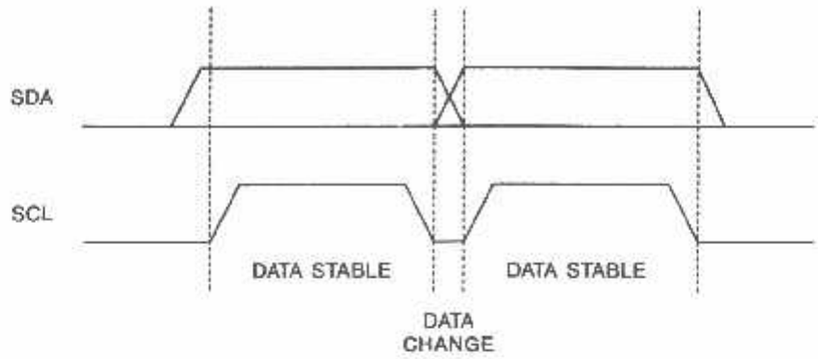


Write Cycle Timing
SCL: Serial Clock, SDA: Serial Data I/O

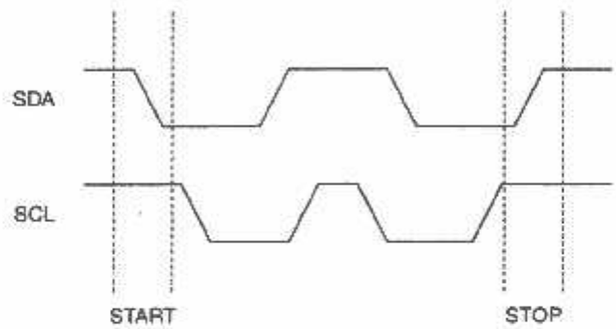


Note: 1. The write cycle time t_{WR} is the time from a valid stop condition of a write sequence to the end of the internal clear/write cycle.

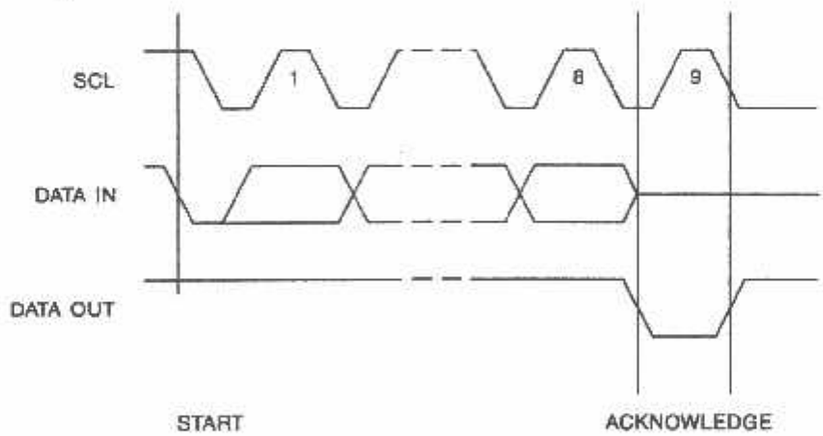
Data Validity



Start and Stop Definition



Output Acknowledge



Device Addressing

The 32K/64K EEPROM requires an 8-bit device address word following a start condition to enable the chip for a read or write operation (refer to Figure 1). The device address word consists of a mandatory one, zero sequence for the first four most significant bits as shown. This is common to all 2-wire EEPROM devices.

The 32K/64K uses the three device address bits A2, A1, A0 to allow as many as eight devices on the same bus. These bits must compare to their corresponding hardwired input pins. The A2, A1, and A0 pins use an internal proprietary circuit that biases them to a logic low condition if the pins are allowed to float.

The eighth bit of the device address is the read/write operation select bit. A read operation is initiated if this bit is high and a write operation is initiated if this bit is low.

Upon a compare of the device address, the EEPROM will output a zero. If a compare is not made, the device will return to standby state.

NOISE PROTECTION: Special internal circuitry placed on the SDA and SCL pins prevent small noise spikes from activating the device. A low-V_{CC} detector (5-volt option) resets the device to prevent data corruption in a noisy environment.

DATA SECURITY: The AT24C32/64 has a hardware data protection scheme that allows the user to write protect the upper quadrant (8/16K bits) of memory when the WP pin is at V_{CC}.

Write Operations

BYTE WRITE: A write operation requires two 8-bit data word addresses following the device address word and acknowledgment. Upon receipt of this address, the EEPROM will again respond with a zero and then clock in the first 8-bit data word. Following receipt of the 8-bit data word, the EEPROM will output a zero and the addressing device, such as a microcontroller, must terminate the write sequence with a stop condition. At this time the EEPROM enters an internally-timed write cycle, t_{WR}, to the nonvolatile memory. All inputs are disabled during this write cycle and the EEPROM will not respond until the write is complete (refer to Figure 2).

PAGE WRITE: The 32K/64K EEPROM is capable of 32-byte page writes.

A page write is initiated the same way as a byte write, but the microcontroller does not send a stop condition after the first data word is clocked in. Instead, after the EEPROM acknowledges receipt of the first data word, the microcontroller can transmit up to 31 more data words. The EEPROM will respond with a zero after each data word received. The microcontroller must terminate the page write sequence with a stop condition (refer to Figure 3).

The data word address lower 5 bits are internally incremented following the receipt of each data word. The higher data word address bits are not incremented, retaining the memory page row location. When the word address, internally generated, reaches the page boundary, the following byte is placed at the beginning of the same page. If more than 32 data words are transmitted to the EEPROM, the data word address will "roll over" and previous data will be overwritten.

ACKNOWLEDGE POLLING: Once the internally-timed write cycle has started and the EEPROM inputs are disabled, acknowledge polling can be initiated. This involves sending a start condition followed by the device address word. The read/write bit is representative of the operation desired. Only if the internal write cycle has completed will the EEPROM respond with a zero, allowing the read or write sequence to continue.

Read Operations

Read operations are initiated the same way as write operations with the exception that the read/write select bit in the device address word is set to one. There are three read operations: current address read, random address read and sequential read.

CURRENT ADDRESS READ: The internal data word address counter maintains the last address accessed during the last read or write operation, incremented by one. This address stays valid between operations as long as the chip power is maintained. The address "roll over" during read is from the last byte of the last memory page, to the first byte of the first page. The address "roll over" during write is from the last byte of the current page to the first byte of the same page.

Once the device address with the read/write select bit set to one is clocked in and acknowledged by the EEPROM, the current address data word is serially clocked out. The microcontroller does not respond with an input zero but does generate a following stop condition (refer to Figure 4).

RANDOM READ: A random read requires a "dummy" byte write sequence to load in the data word address. Once the device address word and data word address are clocked in and acknowledged by the EEPROM, the microcontroller must generate another start condition. The microcontroller now initiates a current address read by sending a device address with the read/write select bit high. The EEPROM acknowledges the device address and serially clocks out the data word. The microcontroller does not respond with a zero but does generate a following stop condition (refer to Figure 5).

SEQUENTIAL READ: Sequential reads are initiated by either a current address read or a random address read. After the microcontroller receives a data word, it responds with an acknowledge. As long as the EEPROM receives an

acknowledge, it will continue to increment the data word address and serially clock out sequential data words. When the memory address limit is reached, the data word address will "roll over" and the sequential read will continue. The sequential read operation is terminated when the microcontroller does not respond with a zero but does generate a following stop condition (refer to Figure 6).

Figure 1. Device Address

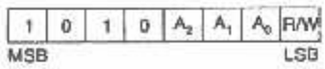


Figure 2. Byte Write

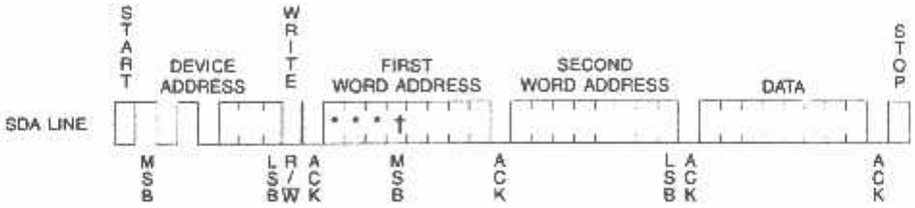
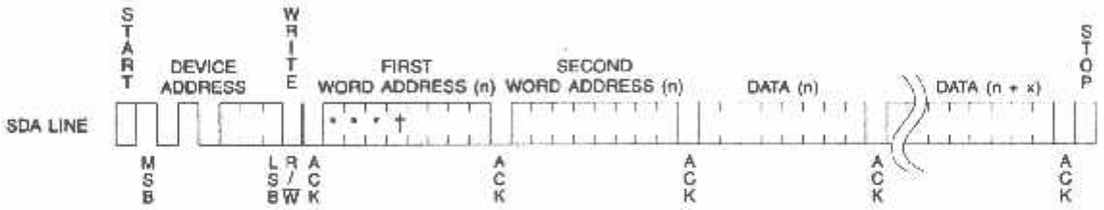


Figure 3. Page Write



Notes: 1. * = DON'T CARE bits 2. † = DON'T CARE bits for the 32K

Figure 4. Current Address Read

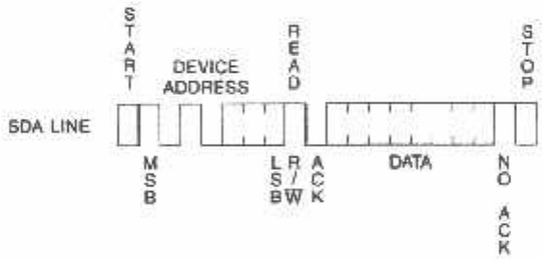
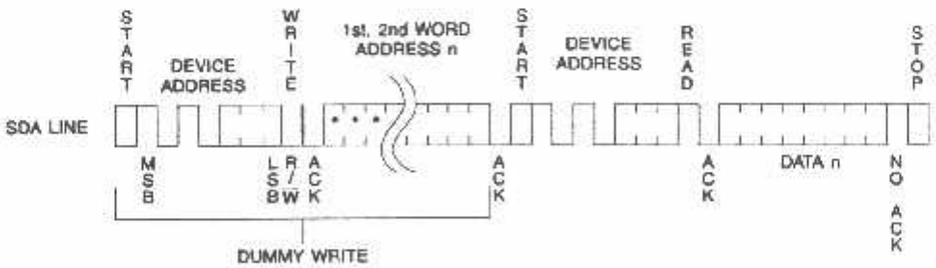
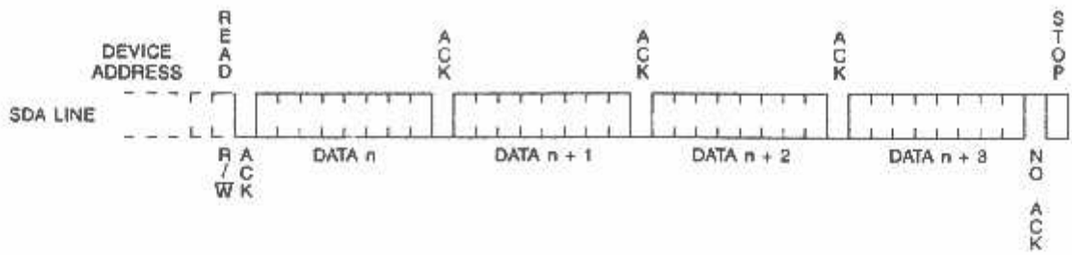


Figure 5. Random Read



Note: 1. * = DON'T CARE bits

Figure 6. Sequential Read



AT24C32 Ordering Information

t_{WR} (max) (ms)	I_{CC} (max) (µA)	I_{SB} (max) (µA)	f_{MAX} (kHz)	Ordering Code	Package	Operation Range
10	3000	35	400	AT24C32-10PC AT24C32N-10SC AT24C32W-10SC AT24C32-10TC AT24C32-10SC	8P3 8S1 8S2 8T 14S	Commercial (0°C to 70°C)
	3000	35	400	AT24C32-10PI AT24C32N-10SI AT24C32W-10SI AT24C32-10TI AT24C32-10SI	8P3 8S1 8S2 8T 14S	Industrial (-40°C to 85°C)
10	1500	0.5	100	AT24C32-10PC-2.7 AT24C32N-10SC-2.7 AT24C32W-10SC-2.7 AT24C32-10TC-2.7 AT24C32-10SC-2.7	8P3 8S1 8S2 8T 14S	Commercial (0°C to 70°C)
	1500	0.5	100	AT24C32-10PI-2.7 AT24C32N-10SI-2.7 AT24C32W-10SI-2.7 AT24C32-10TI-2.7 AT24C32-10SI-2.7	8P3 8S1 8S2 8T 14S	Industrial (-40°C to 85°C)

Package Type	
8P3	8-Lead, 0.300" Wide, Plastic Dual Inline Package (PDIP)
8S1	8-Lead, 0.150" Wide, Plastic Gull Wing Small Outline (JEDEC SOIC)
8S2	8-Lead, 0.200" Wide, Plastic Gull Wing Small Outline (EIAJ SOIC)
8T	8-Lead, 0.170" Wide, Plastic Gull Wing Small Outline (TSSOP)
14S	14-Lead, 0.150" Wide, Plastic Gull Wing Small Outline (SOIC)
Options	
Blank	Standard Operation (4.5V to 5.5V)
-2.7	Low Voltage (2.7V to 5.5V)
-2.5	Low Voltage (2.5V to 5.5V)
-1.8	Low Voltage (1.8V to 5.5V)

AT24C32 Ordering Information (Continued)

t_{WR} (max) (ms)	I_{CC} (max) (µA)	I_{SB} (max) (µA)	f_{MAX} (kHz)	Ordering Code	Package	Operation Range
10	1000	0.5	100	AT24C32-10PC-2.5 AT24C32N-10SC-2.5 AT24C32W-10SC-2.5 AT24C32-10TC-2.5 AT24C32-10SC-2.5	8P3 8S1 8S2 8T 14S	Commercial (0°C to 70°C)
	1000	0.5	100	AT24C32-10PI-2.5 AT24C32N-10SI-2.5 AT24C32W-10SI-2.5 AT24C32-10TI-2.5 AT24C32-10SI-2.5	8P3 8S1 8S2 8T 14S	Industrial (-40°C to 85°C)
10	800	0.1	100	AT24C32-10PC-1.8 AT24C32N-10SC-1.8 AT24C32W-10SC-1.8 AT24C32-10TC-1.8 AT24C32-10SC-1.8	8P3 8S1 8S2 8T 14S	Commercial (0°C to 70°C)
	800	0.1	100	AT24C32-10PI-1.8 AT24C32N-10SI-1.8 AT24C32W-10SI-1.8 AT24C32-10TI-1.8 AT24C32-10SI-1.8	8P3 8S1 8S2 8T 14S	Industrial (-40°C to 85°C)

Package Type	
8P3	8-Lead, 0.300" Wide, Plastic Dual Inline Package (PDIP)
8S1	8-Lead, 0.150" Wide, Plastic Gull Wing Small Outline (JEDEC SOIC)
8S2	8-Lead, 0.200" Wide, Plastic Gull Wing Small Outline (EIAJ SOIC)
8T	8-Lead, 0.170" Wide, Plastic Gull Wing Small Outline (TSSOP)
14S	14-Lead, 0.150" Wide, Plastic Gull Wing Small Outline (SOIC)
Options	
Blank	Standard Operation (4.5V to 5.5V)
-2.7	Low Voltage (2.7V to 5.5V)
-2.5	Low Voltage (2.5V to 5.5V)
-1.8	Low Voltage (1.8V to 5.5V)

AT24C64 Ordering Information

t_{WR} (max) (ms)	I_{CC} (max) (µA)	I_{SB} (max) (µA)	f_{MAX} (kHz)	Ordering Code	Package	Operation Range
10	3000	35	400	AT24C64-10PC AT24C64N-10SC AT24C64W-10SC AT24C64-10TC AT24C64-10SC	8P3 8S1 8S2 8T 14S	Commercial (0°C to 70°C)
	3000	35	400	AT24C64-10PI AT24C64N-10SI AT24C64W-10SI AT24C64-10TI AT24C64-10SI	8P3 8S1 8S2 8T 14S	Industrial (-40°C to 85°C)
10	1500	0.5	100	AT24C64-10PC-2.7 AT24C64N-10SC-2.7 AT24C64W-10SC-2.7 AT24C64-10TC-2.7 AT24C64-10SC-2.7	8P3 8S1 8S2 8T 14S	Commercial (0°C to 70°C)
	1500	0.5	100	AT24C64-10PI-2.7 AT24C64N-10SI-2.7 AT24C64W-10SI-2.7 AT24C64-10TI-2.7 AT24C64-10SI-2.7	8P3 8S1 8S2 8T 14S	Industrial (-40°C to 85°C)

Package Type	
8P3	8-Lead, 0.300" Wide, Plastic Dual Inline Package (PDIP)
8S1	8-Lead, 0.150" Wide, Plastic Gull Wing Small Outline (JEDEC SOIC)
8S2	8-Lead, 0.200" Wide, Plastic Gull Wing Small Outline (EIAJ SOIC)
8T	8-Lead, 0.170" Wide, Plastic Gull Wing Small Outline (TSSOP)
14S	14-Lead, 0.150" Wide, Plastic Gull Wing Small Outline (SOIC)
Options	
Blank	Standard Operation (4.5V to 5.5V)
-2.7	Low Voltage (2.7V to 5.5V)
-2.5	Low Voltage (2.5V to 5.5V)
-1.8	Low Voltage (1.8V to 5.5V)

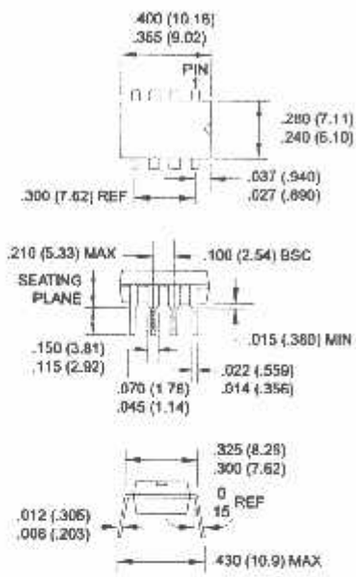
AT24C64 Ordering Information (Continued)

t_{WR} (max) (ms)	I_{CC} (max) (µA)	I_{SB} (max) (µA)	f_{MAX} (kHz)	Ordering Code	Package	Operation Range
10	1000	0.5	100	AT24C64-10PC-2.5 AT24C64N-10SC-2.5 AT24C64W-10SC-2.5 AT24C64-10TC-2.5 AT24C64-10SC-2.5	8P3 8S1 8S2 9T 14S	Commercial (0°C to 70°C)
	1000	0.5	100	AT24C64-10PI-2.5 AT24C64N-10SI-2.5 AT24C64W-10SI-2.5 AT24C64-10TI-2.5 AT24C64-10SI-2.5	8P3 8S1 8S2 8T 14S	Industrial (-40°C to 85°C)
10	800	0.1	100	AT24C64-10PC-1.8 AT24C64N-10SC-1.8 AT24C64W-10SC-1.8 AT24C64-10TC-1.8 AT24C64-10SC-1.8	8P3 8S1 8S2 8T 14S	Commercial (0°C to 70°C)
	800	0.1	100	AT24C64-10PI-1.8 AT24C64N-10SI-1.8 AT24C64W-10SI-1.8 AT24C64-10TI-1.8 AT24C64-10SI-1.8	8P3 8S1 8S2 8T 14S	Industrial (-40°C to 85°C)

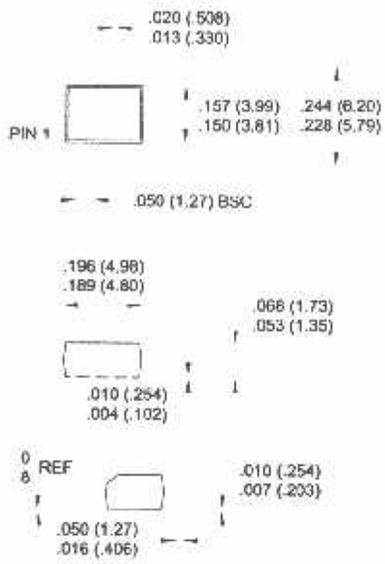
Package Type	
8P3	8-Lead, 0.300" Wide, Plastic Dual Inline Package (PDIP)
8S1	8-Lead, 0.150" Wide, Plastic Gull Wing Small Outline (JEDEC SOIC)
8S2	8-Lead, 0.200" Wide, Plastic Gull Wing Small Outline (EIAJ SOIC)
8T	8-Lead, 0.170" Wide, Plastic Gull Wing Small Outline (TSSOP)
14S	14-Lead, 0.150" Wide, Plastic Gull Wing Small Outline (SOIC)
Options	
Blank	Standard Operation (4.5V to 5.5V)
-2.7	Low Voltage (2.7V to 5.5V)
-2.5	Low Voltage (2.5V to 5.5V)
-1.8	Low Voltage (1.8V to 5.5V)

Packaging Information

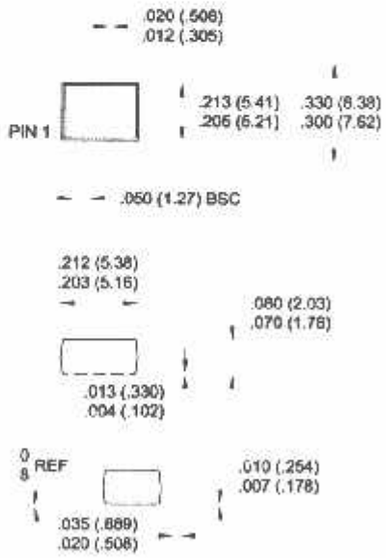
8P3, 8-Lead, 0.300" Wide, Plastic Dual Inline Package (PDIP)
Dimensions in Inches and (Millimeters)
JEDEC STANDARD MS-001 BA



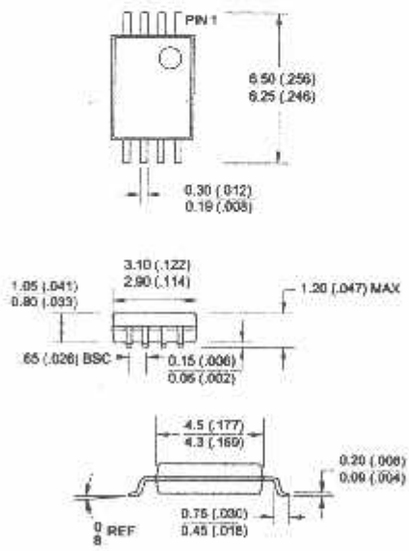
8S1, 8-Lead, 0150" Wide, Plastic Gull Wing Small Outline (JEDEC SOIC)
Dimensions in Inches and (Millimeters)



8S2, 8-Lead, 0.200" Wide, Plastic Gull Wing Small Outline (EIAJ SOIC)
Dimensions in Inches and (Millimeters)



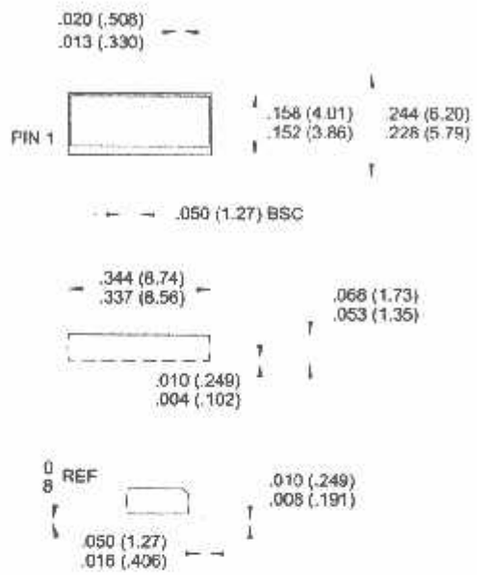
8T, 8-Lead, Plastic Thin Small Outline Package (TSSOP)
Dimensions in Millimeters and (Inches)*



*Controlling dimension: millimeters

Packaging Information

14S, 14-Lead, 0.150" Wide, Plastic Gull Wing Small Outline (SOIC)
Dimensions in Inches and (Millimeters)



Energy Metering IC with Integrated Oscillator

ADE7757*

FEATURES

- On-Chip Oscillator as Clock Source
- High Accuracy, Supposes 50 Hz/60 Hz IEC 521/1036
- Less than 0.1% Error Over a Dynamic Range of 500 to 1
- The ADE7757 Supplies *Average Real Power* on the Frequency Outputs F1 and F2
- The High Frequency Output CF Is Intended for Calibration and Supplies *Instantaneous Real Power*
- The Logic Output REVP Can Be Used to Indicate a Potential Miswiring or Negative Power
- Direct Drive for Electromechanical Counters and Two Phase Stepper Motors (F1 and F2)
- Proprietary ADCs and DSP Provide High Accuracy over Large Variations in Environmental Conditions and Time
- On-Chip Power Supply Monitoring
- On-Chip Creep Protection (No Load Threshold)
- On-Chip Reference 2.5 V ± 8% (20 ppm/°C Typical) with External Overdrive Capability
- Single 5 V Supply, Low Power (20 mW Typical)
- Low Cost CMOS Process
- AC Input only

GENERAL DESCRIPTION

The ADE7757 is a high accuracy electrical energy measurement IC. It is a pin reduction version of AD7755 with an enhancement of a precise oscillator circuit that serves as a clock source to the chip. The ADE7757 eliminates the cost of an external crystal or resonator, thus reducing the overall cost of a meter built with this IC. The chip directly interfaces with the shunt resistor and operates only with ac input.

The ADE7757 specifications surpass the accuracy requirements as quoted in the IEC1036 standard. Due to the similarity between the ADE7757 and AD7755, the Application Note AN-559 can be used as a basis for a description of an IEC1036 low cost watt-hour meter reference design.

The only analog circuitry used in the ADE7757 is in the sigma-delta ADCs and reference circuit. All other signal processing (e.g., multiplication and filtering) is carried out in the digital domain. This approach provides superior stability and accuracy over time and extreme environmental conditions.

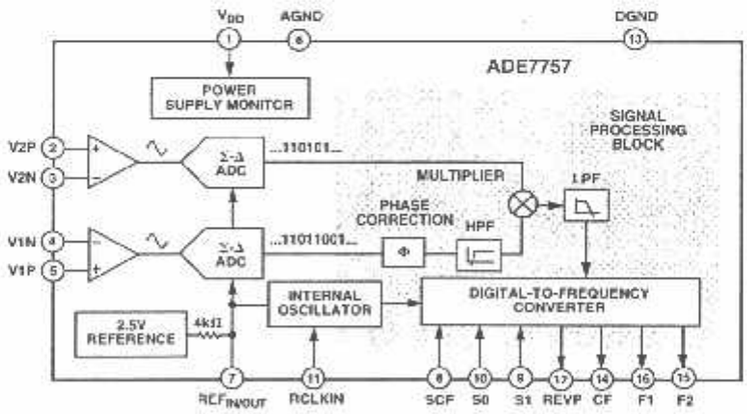
The ADE7757 supplies average real power information on the low frequency outputs F1 and F2. These outputs may be used to directly drive an electromechanical counter or interface with an MCU. The high frequency CF logic output, ideal for calibration purposes, provides instantaneous real power information.

The ADE7757 includes a power supply monitoring circuit on the V_{DD} supply pin. The ADE7757 will remain inactive until the supply voltage on V_{DD} reaches approximately 4 V. If the supply falls below 4 V, the ADE7757 will also remain inactive and the F1, F2, and CF outputs will be in their nonactive modes.

Internal phase matching circuitry ensures that the voltage and current channels are phase matched while the HPF in the current channel eliminates dc offsets. An internal no-load threshold ensures that the ADE7757 does not exhibit creep when no load is present.

The ADE7757 is available in a 16-lead SOIC narrow-body package.

FUNCTIONAL BLOCK DIAGRAM



*U.S. Patents 5,745,323; 5,760,617; 5,862,069; 5,872,469; others pending.

REV. 0

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Tel: 781/329-4700 www.analog.com
Fax: 781/326-8703

ADE7757—SPECIFICATIONS

(V_{DD} = 5 V ± 5%, AGND = DGND = 0 V, On-Chip Reference, RCKLIN = 6.2 kΩ 0.1% ±15ppm/°C, T_{MIN} to T_{MAX} = –40°C to +85°C, unless otherwise noted.)

Parameter	Value	Unit	Test Conditions/Comments
ACCURACY[1,2]			
Measurement Error[1] on Channel V1	0.1	% Reading typ	Channel V2 with Full-Scale Signal (±165 mV), 25°C Over a Dynamic Range 500 to 1 Line Frequency = 45 Hz to 65 Hz
Phase Error[1] Between Channels V1 Phase Lead 37° (PF = 0.8 Capacitive)	±0.1	Degrees(°) max	
V1 Phase Lag 60° (PF = 0.5 Inductive)	±0.1	Degrees(°) max	
AC Power Supply Rejection[1] Output Frequency Variation (CF)	0.2	% Reading typ	S0 = S1 = 1 V1 = 21.2 mV rms, V2 = 116.7 mV rms @ 50 Hz Ripple on V_{DD} of 200 mV rms @ 100 Hz
DC Power Supply Rejection[1] Output Frequency Variation (CF)	±0.3	% Reading typ	S0 = S1 = 1, V1 = 21.2 mV rms, V2 = 116.7 mV rms, V_{DD} = 5 V ±250 mV
ANALOG INPUTS			See Analog Inputs section
Channel V1 Maximum Signal Level	±30	mV max	V1P and V1N to AGND
Channel V2 Maximum Signal Level	±165	mV max	V2P and V2N to AGND
Input Impedance (DC)	320	kΩ min	OSC = 450 kHz, RCKLIN = 6.2 kΩ 0.1% ±15ppm/°C
Bandwidth (–3 dB)	7	kHz nominal	OSC = 450 kHz, RCKLIN = 6.2 kΩ 0.1% ±15ppm/°C
ADC Offset Error[1,2]	±18	mV max	See Terminology Section and Typical Performance Characteristics.
Gain Error[1]	±4	% Ideal typ	External 2.5 V Reference V1 = 21.2 mV rms, V2 = 116.7 mV rms
OSCILLATOR FREQUENCY (OSC)	450	kHz nominal	RCKLIN = 6.2 kΩ 0.1% ±15ppm/°C
Oscillator Frequency Tolerance[1]	±12	% Reading typ	
Oscillator Frequency Stability[1]	±30	ppm/°C typ	
REFERENCE INPUT			
$REF_{IN/OUT}$ Input Voltage Range	2.7	V max	2.5 V + 8%
	2.3	V min	2.5 V – 8%
Input Capacitance	10	pF max	
ON-CHIP REFERENCE			Nominal 2.5 V
Reference Error	±200	mV max	
Temperature Coefficient	±20	ppm/°C typ	
LOGIC INPUTS[3]			
SCF, S0, S1,			
Input High Voltage, V_{INH}	2.4	V min	V_{DD} = 5 V ± 5%
Input Low Voltage, V_{INL}	0.8	V max	V_{DD} = 5 V ± 5%
Input Current, I_{IN}	±1	µA max	Typically 10 nA, V_{IN} = 0 V to V_{DD}
Input Capacitance, C_{IN}	10	pF max	
LOGIC OUTPUTS[3]			
F1 and F2			
Output High Voltage, V_{OH}	4.5	V min	I_{SOURCE} = 10 mA V_{DD} = 5 V
Output Low Voltage, V_{OL}	0.5	V max	I_{SINK} = 10 mA V_{DD} = 5 V
CF			
Output High Voltage, V_{OH}	4	V min	I_{SOURCE} = 5 mA V_{DD} = 5 V
Output Low Voltage, V_{OL}	0.5	V max	I_{SINK} = 5 mA V_{DD} = 5 V
Frequency Output Error[1,2] (CF)	±10	% Ideal typ	External 2.5 V Reference, V1 = 21.2 mV rms, V2 = 116.7 mV rms
POWER SUPPLY			For Specified Performance
V_{DD}	4.75	V min	5 V – 5%
	5.25	V max	5 V + 5%
I_{DD}	5	mA max	Typically 4 mA

NOTES

[1]See Terminology section for explanation of specifications.

[2]See plots in Typical Performance Characteristics.

[3]Sample tested during initial release and after any redesign or process change that may affect this parameter.

Specifications subject to change without notice.

TIMING CHARACTERISTICS[1, 2] (V_{DD} = 5 V ± 5%, AGND = DGND = 0 V, On-Chip Reference, RCKLIN = 6.2 kΩ 0.1% ±15ppm/°C. T_{MIN} to T_{MAX} = –40°C to +85°C, unless otherwise noted.)

Parameter	A, B Versions	Unit	Test Conditions/Comments
t_1[3]	244	ms	F1 and F2 Pulsewidth (Logic Low)
t_2	See Table II	sec	Output Pulse Period. See Transfer Function section.
t_3	1/2 t_2	sec	Time between F1 Falling Edge and F2 Falling Edge
t_4[3, 4]	173	ms	CF Pulsewidth (Logic High)
t_5	See Table III	sec	CF Pulse Period. See Transfer Function section.
t_6	2	µs	Minimum Time between F1 and F2 Pulse

NOTES
[1]Sample tested during initial release and after any redesign or process change that may affect this parameter.
[2]See Figure 1.
[3]The pulsewidths of F1, F2, and CF are not fixed for higher output frequencies. See Frequency Outputs section.
[4]The CF pulse is always 35 µs in the high frequency mode. See Frequency Outputs section and Table III.
Specifications subject to change without notice.

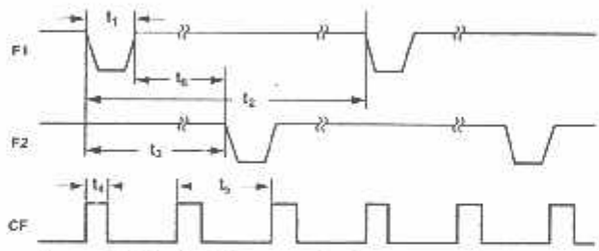


Figure 1. Timing Diagram for Frequency Outputs

ABSOLUTE MAXIMUM RATINGS[1]

(T_A = 25°C, unless otherwise noted.)

V_{DD} to AGND	−0.3 V to +7 V
V_{DD} to DGND	−0.3 V to +7 V
Analog Input Voltage to AGND	
V1P, V1N, V2P, and V2N	−6 V to +6 V
Reference Input Voltage to AGND	−0.3 V to V_{DD} + 0.3 V
Digital Input Voltage to DGND	−0.3 V to V_{DD} + 0.3 V
Digital Output Voltage to DGND	−0.3 V to V_{DD} + 0.3 V
Operating Temperature Range	
Industrial (A, B Versions)	−40°C to +85°C
Storage Temperature Range	−65°C to +150°C
Junction Temperature	150°C
16-Lead Plastic SOIC, Power Dissipation	350 mW
θ_{JA} Thermal Impedance[2]	124.9°C/W
Lead Temperature, Soldering	
Vapor Phase (60 sec)	215°C
Infrared (15 sec)	220°C

[1] Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those listed in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

[2] JEDEC 1S Standard (2-layer) Board Data

ORDERING GUIDE

Model	Package Description	Package Options
ADE7757ARN	SOIC Narrow-Body	RN-16
ADE7757ARNRL	SOIC Narrow-Body in Reel	RNRL-16
EVAL-ADE7757EB	Evaluation Board	Evaluation Board

TERMINOLOGY

Measurement Error

The error associated with the energy measurement made by the ADE7757 is defined by the following formula:

$$\%Error = \frac{Energy\ registered\ by\ ADE7757 - True\ Energy}{True\ Energy} \times 100\%$$

Phase Error Between Channels

The HPF (High-Pass Filter) in the current channel (Channel V1) has a phase lead response. To offset this phase response and equalize the phase response between channels, a phase correction network is also placed in Channel V1. The phase correction network matches the phase to within ±0.1° over a range of 45 Hz to 65 Hz, and ±0.2° over a range 40 Hz to 1 kHz. See Figures 11 and 12.

Power Supply Rejection

This quantifies the ADE7757 measurement error as a percentage of reading when the power supplies are varied.

For the ac PSR measurement, a reading at nominal supplies (5 V) is taken. A 200 mV rms/100 Hz signal is then introduced onto the supplies and a second reading is obtained under the same input signal levels. Any error introduced is expressed as a percentage of reading—see Measurement Error definition.

For the dc PSR measurement, a reading at nominal supplies (5 V) is taken. The supplies are then varied ±5% and a second reading is obtained with the same input signal levels. Any error introduced is again expressed as a percentage of reading.

ADC Offset Error

This refers to the small dc signal (offset) associated with the analog inputs to the ADCs. However, the HPF in Channel V1 eliminates the offset in the circuitry. Therefore, the power calculation is not affected by this offset.

Frequency Output Error (CF)

The frequency output error of the ADE7757 is defined as the difference between the measured output frequency (minus the offset) and the ideal output frequency. The difference is expressed as a percentage of the ideal frequency. The ideal frequency is obtained from the ADE7757 transfer function (see Transfer Function section).

Gain Error

The gain error of the ADE7757 is defined as the difference between the measured output frequency (minus the offset) and the ideal output frequency. The difference is expressed as a percentage of the ideal frequency. The ideal frequency is obtained from the ADE7757 transfer function (see Transfer Function section).

Oscillator Frequency Tolerance

The oscillator frequency tolerance of the ADE7757 is defined as part-to-part frequency variation in terms of percentage at room temperature (25°C). It is measured by taking the difference between the measured oscillator frequency and the nominal frequency defined in the Specifications section.

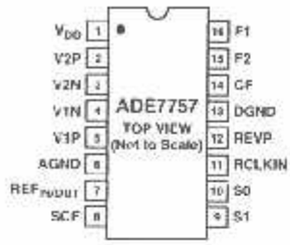
Oscillator Frequency Stability

Oscillator frequency stability is defined as frequency variation in terms of percentage drift per million over the operating temperature range. In a metering application, the temperature range is −40°C to +85°C. Oscillator frequency stability is measured by taking the difference between the measured oscillator frequency at −40°C and +85°C and the measured oscillator frequency at +25°C.

CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although the ADE7757 features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.

PIN CONFIGURATION



PIN FUNCTION DESCRIPTIONS

Pin No.	Mnemonic	Description
1	V_{DD}	Power Supply. This pin provides the supply voltage for the circuitry in the ADE7757. The supply voltage should be maintained at 5 V ± 5% for specified operation. This pin should be decoupled with a 10 µF capacitor in parallel with a ceramic 100 nF capacitor.
2, 3	V2P, V2N	Analog Inputs for Channel V2 (voltage channel). These inputs provide a fully differential input pair. The maximum differential input voltage is ± 165 mV for specified operation. Both inputs have internal ESD protection circuitry; an overvoltage of ± 6 V can be sustained on these inputs without risk of permanent damage.
4, 5	V1N, V1P	Analog Inputs for Channel V1 (current channel). These inputs are fully differential voltage inputs with a maximum signal level of ± 30 mV with respect to pin V1N for specified operation. Both inputs have internal ESD protection circuitry and, in addition, an overvoltage of ± 6 V can be sustained on these inputs without risk of permanent damage.
6	AGND	This provides the ground reference for the analog circuitry in the ADE7757, i.e., ADCs and reference. This pin should be tied to the analog ground plane of the PCB. The analog ground plane is the ground reference for all analog circuitry, e.g., antialiasing filters, current and voltage sensors, and so forth. For accurate noise suppression, the analog ground plane should only be connected to the digital ground plane at one point. A star ground configuration will help to keep noisy digital currents away from the analog circuits.
7	REF_{INOUT}	This pin provides access to the on-chip voltage reference. The on-chip reference has a nominal value of 2.5 V ± 8% and a typical temperature coefficient of 20 ppm/°C. An external reference source may also be connected at this pin. In either case, this pin should be decoupled to AGND with a 1 µF tantalum capacitor and 100 nF ceramic capacitor. The internal reference cannot be used to drive an external load.
8	SCF	Select Calibration Frequency. This logic input is used to select the frequency on the calibration output CF. Table III shows calibration frequencies selection.
9, 10	S1, S0	These logic inputs are used to select one of four possible frequencies for the digital-to-frequency conversion. With this logic input, designers have greater flexibility when designing an energy meter. See Selecting a Frequency for an Energy Meter Application section.
11	RCLKIN	To enable the internal oscillator as a clock source to the chip, a precise low temperature drift resistor at nominal value of 6.2 kΩ must be connected from this pin to DGND.
12	REVP	This logic output will go high when negative power is detected, i.e., when the phase angle between the voltage and current signals is greater than 90°. This output is not latched and will be reset when positive power is once again detected. The output will go high or low at the same time as a pulse is issued on CF.
13	DGND	This provides the ground reference for the digital circuitry in the ADE7757, i.e., multiplier, filters, and digital-to-frequency converter. This pin should be tied to the digital ground plane of the PCB. The digital ground plane is the ground reference for all digital circuitry, e.g., counters (mechanical and digital), MCUs, and indicator LEDs. For accurate noise suppression, the analog ground plane should be connected to the digital ground plane at one point only, e.g., a star ground.
14	CF	Calibration Frequency Logic Output. The CF logic output provides instantaneous real power information. This output is intended for calibration purposes. Also see SCF pin description.
15, 16	F2, F1	Low Frequency Logic Outputs. F1 and F2 supply *average real power* information. The logic outputs can be used to directly drive electromechanical counters and two phase stepper motors. See Transfer Function section.

ADE7757–Typical Performance Characteristics

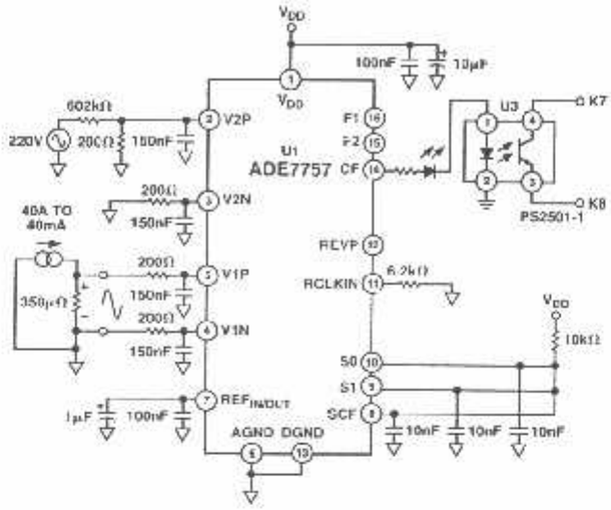
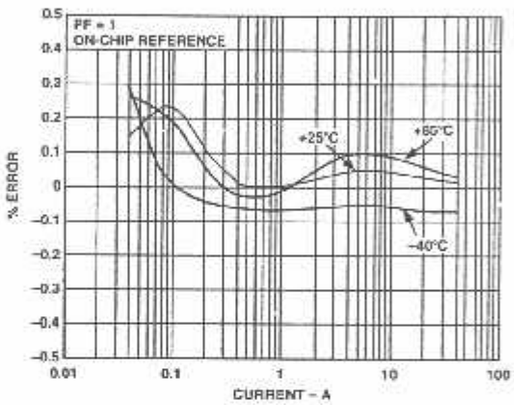
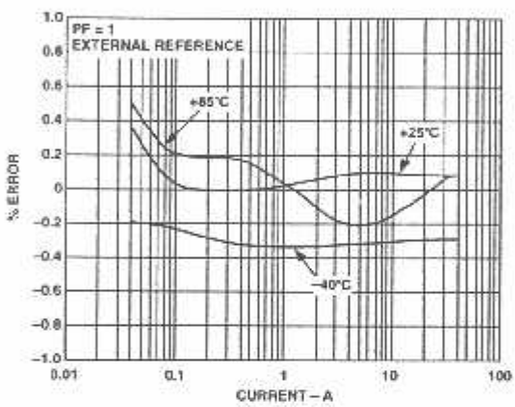


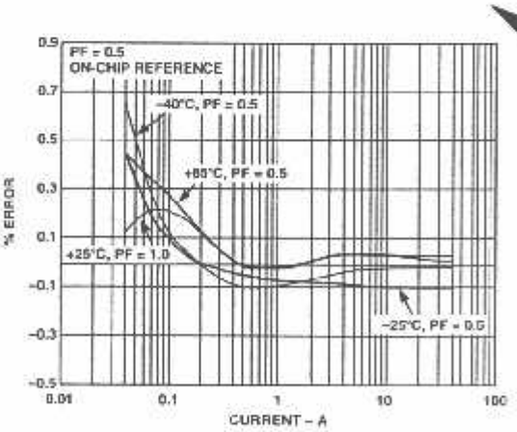
Figure 2. Test Circuit for Performance Curves



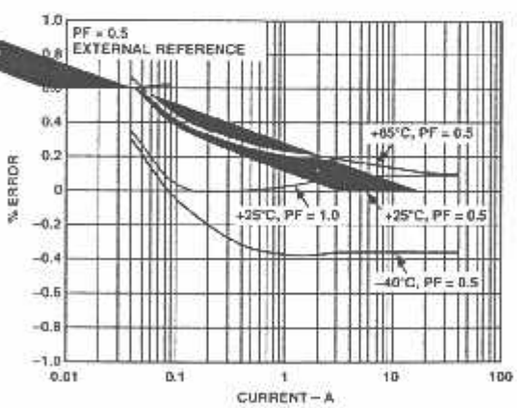
TPC 1. Error as a % of Reading over Temperature with On-Chip Reference (PF = 1)



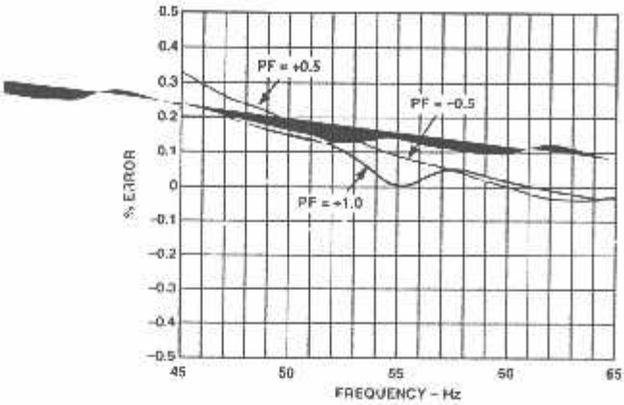
TPC 3. Error as a % of Reading over Temperature with External Reference (PF = 1)



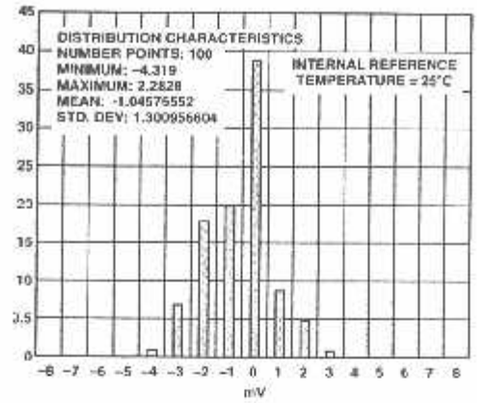
TPC 2. Error as a % of Reading over Temperature with On-Chip Reference (PF = 0.5)



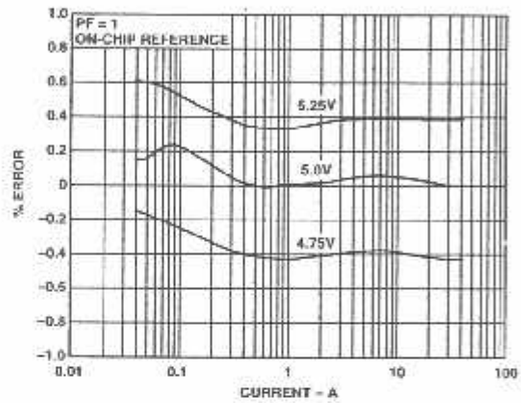
TPC 4. Error as a % of Reading over Temperature with External Reference (PF = 0.5)



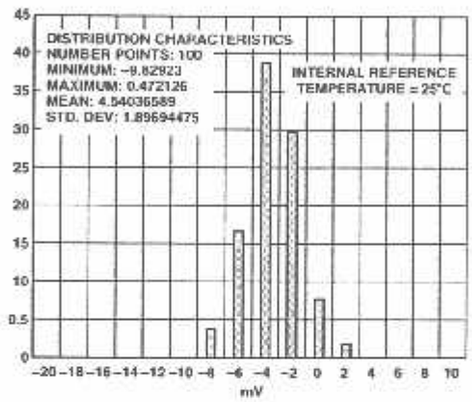
TPC 5. Error as a % of Reading over Input Frequency



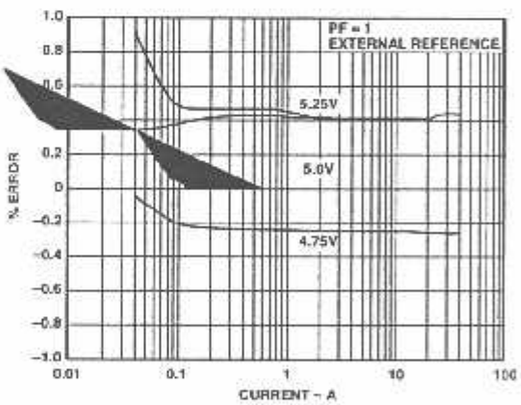
TPC 8. Channel V1 Offset Distribution



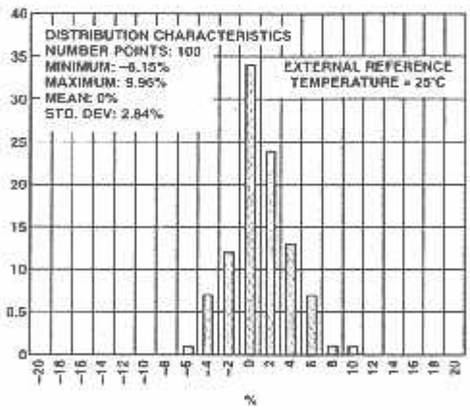
TPC 6. PSR with Internal Reference



TPC 9. Channel V2 Offset Distribution



TPC 7. PSR with External Reference



TPC 10. Part-to-Part CF Distribution From Mean

THEORY OF OPERATION

The two ADCs digitize the voltage signals from the current and voltage sensors. These ADCs are 16-bit sigma-delta with an oversampling rate of 450 kHz. This analog input structure greatly simplifies sensor interfacing by providing a wide dynamic range for direct connection to the sensor and also simplifies the antialiasing filter design. A high-pass filter in the current channel removes any dc component from the current signal. This eliminates any inaccuracies in the real power calculation due to offsets in the voltage or current signals. Because the HPF is always enabled, the IC will operate only with ac input (see HPF and Offset Effects section).

The real power calculation is derived from the instantaneous power signal. The instantaneous power signal is generated by a direct multiplication of the current and voltage signals. In order to extract the real power component (i.e., the dc component), the instantaneous power signal is low-pass filtered. Figure 3 illustrates the instantaneous real power signal and shows how the real power information can be extracted by low-pass filtering the instantaneous power signal. This scheme correctly calculates real power for sinusoidal current and voltage waveforms at all power factors. All signal processing is carried out in the digital domain for superior stability over temperature and time.

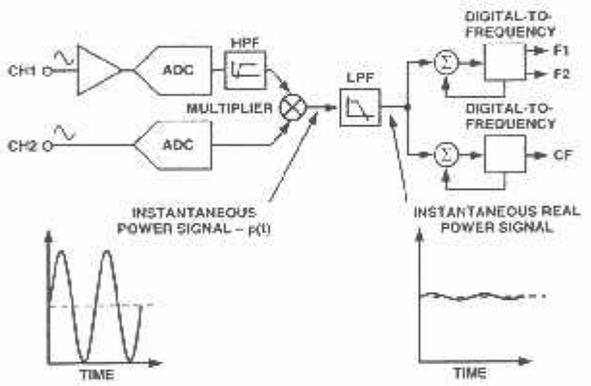


Figure 3. Signal Processing Block Diagram

The low frequency outputs (F1, F2) of the ADE7757 are generated by accumulating this real power information. This low frequency inherently means a long accumulation time between output pulses. Consequently, the resulting output frequency is proportional to the average real power. This average real power information is then accumulated (e.g., by a counter) to generate real energy information. Conversely, due to its high output frequency and hence shorter integration time, the CF output frequency is proportional to the instantaneous real power. This is useful for system calibration, which can be done faster under steady load conditions.

Power Factor Considerations

The method used to extract the real power information from the instantaneous power signal (i.e., by low-pass filtering) is still valid even when the voltage and current signals are not in phase. Figure 4 displays the unity power factor condition and a DPF (Displacement Power Factor) = 0.5, i.e., current signal lagging the voltage by 60°. If we assume the voltage and current waveforms are sinusoidal, the real power component of the instantaneous power signal (i.e., the dc term) is given by:

$$\left(\frac{V \times I}{2}\right) \times \cos(60°)$$

This is the correct real power calculation..

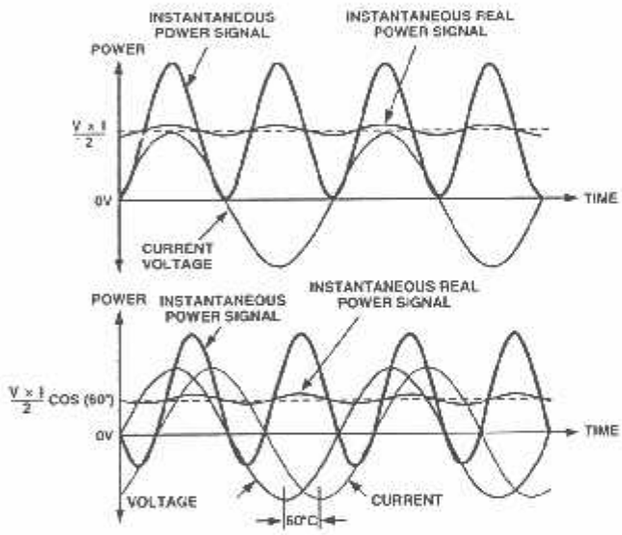


Figure 4. DC Component of Instantaneous Power Signal Conveys Real Power Information PF < 1

Nonsinusoidal Voltage and Current

The real power calculation method also holds true for nonsinusoidal current and voltage waveforms. All voltage and current waveforms in practical applications will have some harmonic content. Using the Fourier Transform, instantaneous voltage and current waveforms can be expressed in terms of their harmonic content.

$$v(t) = V_0 + \sqrt{2} \times \sum_{h=0}^{\infty} V_h \times \sin(h\omega t + \alpha_h) \quad (1)$$

where:

$v(t)$ is the instantaneous voltage
V_0 is the average value
V_h is the rms value of voltage harmonic h, and
α_h is the phase angle of the voltage harmonic.

$$i(t) = I_0 + \sqrt{2} \times \sum_{h=0}^{\infty} I_h \times \sin(h\omega t + \beta_h) \quad (2)$$

where:

$i(t)$ is the instantaneous current
I_0 is the dc component
I_h is the rms value of current harmonic h, and
β_h is the phase angle of the current harmonic.

Using Equations 1 and 2, the real power P can be expressed in terms of its fundamental real power (P_1) and harmonic real power (P_H).

$$P = P_1 + P_H$$

where:

$$P_1 = V_1 \times I_1 \cos\phi_1$$
$$\phi_1 = \alpha_1 - \beta_1 \quad (3)$$

and

$$P_H = \sum_{h \neq 1}^{\infty} V_h \times I_h \cos\phi_h$$
$$\phi_h = \alpha_h - \beta_h \quad (4)$$

As can be seen from Equation 4, a harmonic real power component is generated for every harmonic, provided that harmonic is present in both the voltage and current waveforms. The power factor calculation has previously been shown to be accurate in the case of a pure sinusoid. Therefore the harmonic real power must also correctly account for power factor since it is made up of a series of pure sinusoids.

Note that the input bandwidth of the analog inputs is 7 kHz at the nominal internal oscillator frequency of 450 kHz.

ANALOG INPUTS

Channel V1 (Current Channel)

The voltage output from the current sensor is connected to the ADE7757 here. Channel V1 is a fully differential voltage input. V1P is the positive input with respect to V1N.

The maximum peak differential signal on Channel V1 should be less than ±30 mV (21 mV rms for a pure sinusoidal signal) for specified operation.

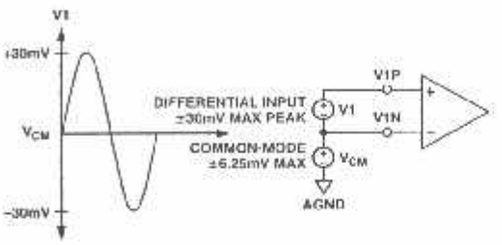


Figure 5. Maximum Signal Levels, Channel V1

The diagram in Figure 5 illustrates the maximum signal levels on V1P and V1N. The maximum differential voltage is ±30 mV. The differential voltage signal on the inputs must be referenced to a common mode, e.g., AGND. The maximum common-mode signal is ±6.25 mV, as shown in Figure 5.

Channel V2 (Voltage Channel)

The output of the line voltage sensor is connected to the ADE7757 at this analog input. Channel V2 is a fully differential voltage input with a maximum peak differential signal of ±165 mV. Figure 6 illustrates the maximum signal levels that can be connected to the ADE7757 Channel V2.

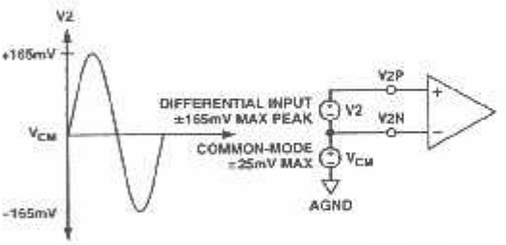


Figure 6. Maximum Signal Levels, Channel V2

Channel V2 is usually driven from a common-mode voltage, i.e., the differential voltage signal on the input is referenced to a common mode (usually AGND). The analog inputs of the ADE7757 can be driven with common-mode voltages of up to 25 mV with respect to AGND. However best results are achieved using a common mode equal to AGND.

Typical Connection Diagrams

Figure 7 shows a typical connection diagram for Channel V1. A shunt is the current sensor selected for this example because of its low cost compared to other current sensors such as the CT (current transformer). This IC is ideal for low current meters.

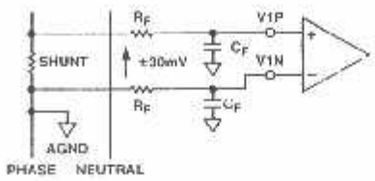


Figure 7. Typical Connection for Channel V1

Figure 8 shows a typical connection for Channel V2. Typically, the ADE7757 is biased around the neutral wire, and a resistor divider is used to provide a voltage signal that is proportional to the line voltage. Adjusting the ratio of R_A, R_B, and R_F is also a convenient way of carrying out a gain calibration on a meter.

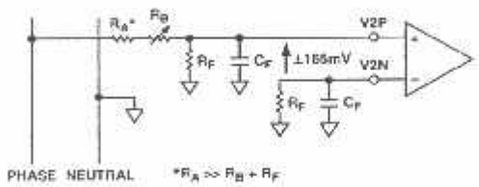


Figure 8. Typical Connections for Channel V2

POWER SUPPLY MONITOR

The ADE7757 contains an on-chip power supply monitor. The power supply (V_{DD}) is continuously monitored by the ADE7757. If the supply is less than 4 V, the ADE7757 becomes inactive. This is useful to ensure proper device operation at power-up and power-down. The power supply monitor has built in hysteresis and filtering that provide a high degree of immunity to false triggering from noisy supplies.

As can be seen from Figure 9, the trigger level is nominally set at 4 V. The tolerance on this trigger level is within ±5%. The power supply and decoupling for the part should be such that the ripple at V_{DD} does not exceed 5 V ± 5% as specified for normal operation.

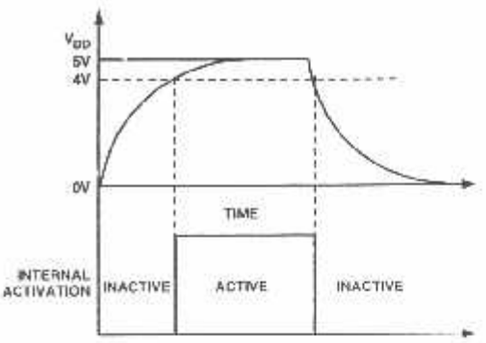


Figure 9. On-Chip Power Supply Monitor

HPF and Offset Effects

Figure 10 illustrates the effect of offsets on the real power calculation. As can be seen, offsets on Channel V1 and Channel V2 will contribute a dc component after multiplication. Since this dc component is extracted by the LPF and used to generate the real power information, the offsets will contribute a constant error to the real power calculation. This problem is easily avoided by the built-in HPF in Channel V1. By removing the offsets from at least one channel, no error component can be generated at dc by the multiplication. Error terms at the line frequency (ω) are removed by the LPF and the digital-to-frequency conversion (see Digital-to-Frequency Conversion section).

The equation below shows how power calculation is affected by the dc offsets in the current and voltage channels:

$$\left\{V\cos(\omega t)+V_{OS}\right\}\times\left\{I\cos(\omega t)-I_{OS}\right\}=$$
$$\frac{V\times I}{2}+V_{OS}\times I_{OS}+V_{OS}\times I\cos(\omega t)+I_{OS}\times V\cos(\omega t)$$
$$+\frac{V\times I}{2}\times\cos(2\omega t)$$

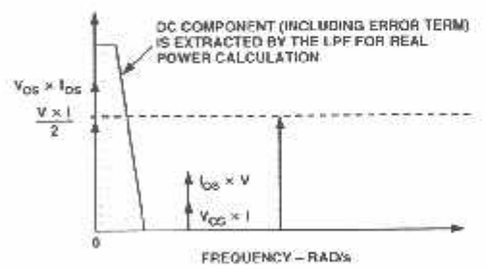


Figure 10. Effect of Channel Offset on the Real Power Calculation

The HPF in Channel V1 has an associated phase response that is compensated for on-chip. Figures 11 and 12 show the phase error between channels with the compensation network activated. The ADE7757 is phase compensated up to 1 kHz as shown. This will ensure correct active harmonic power calculation even at low power factors.

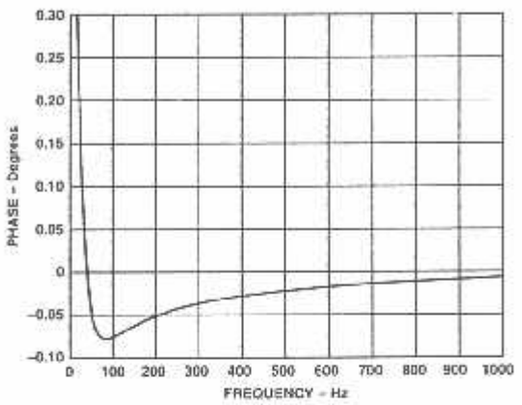


Figure 11. Phase Error between Channels (0 Hz to 1 kHz)

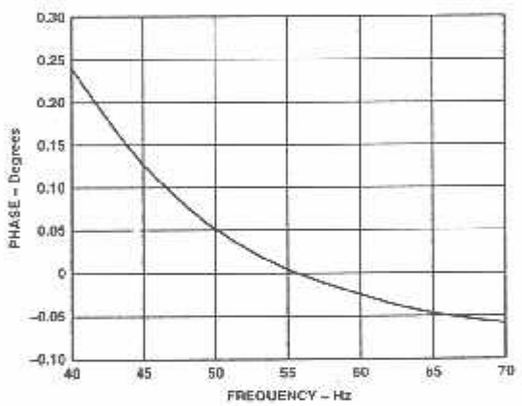


Figure 12. Phase Error between Channels (40 Hz to 70 Hz)

DIGITAL-TO-FREQUENCY CONVERSION

As previously described, the digital output of the low-pass filter after multiplication contains the real power information. However, since this LPF is not an ideal "brick wall" filter implementation, the output signal also contains attenuated components at the line frequency and its harmonics, i.e., cos(hwt) where h = 1, 2, 3, . . . and so on.

The magnitude response of the filter is given by:

$$|H(f)| = \frac{1}{\sqrt{1+\frac{f^2}{4.45^2}}} \qquad (5)$$

For a line frequency of 50 Hz, this would give an attenuation of the 2ω (100 Hz) component of approximately 22 dB. The dominating harmonic will be at twice the line frequency (2ω) due to the instantaneous power calculation.

Figure 13 shows the instantaneous real power signal at the output of the LPF that still contains a significant amount of instantaneous power information, i.e., cos(2ωt). This signal is then passed to the digital-to-frequency converter where it is integrated (accumulated) over time in order to produce an output frequency. The accumulation of the signal will suppress or average out any non-dc components in the instantaneous real power signal. The average value of a sinusoidal signal is zero. Thus the frequency generated by the ADE7757 is proportional to the average real power. Figure 13 shows the digital-to-frequency conversion for steady load conditions, i.e., constant voltage and current.

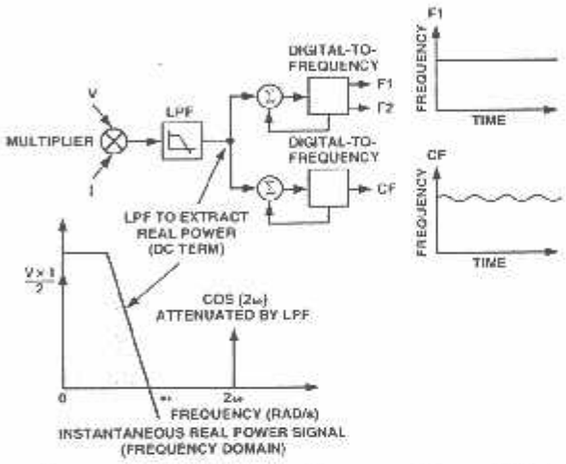


Figure 13. Real Power-to-Frequency Conversion

As can be seen in the diagram, the frequency output CF is seen to vary over time, even under steady load conditions. This frequency variation is primarily due to the cos(2ωt) component in the instantaneous real power signal. The output frequency on CF can be up to 2048 times higher than the frequency on F1 and F2. This higher output frequency is generated by accumulating the instantaneous real power signal over a much shorter time while converting it to a frequency. This shorter accumulation period means less averaging of the cos(2ωt) component. Consequently, some of this instantaneous power signal passes through the digital-to-frequency conversion. This will not be a problem in the application. Where CF is used for calibration purposes, the frequency should be averaged by the frequency counter, which will remove any ripple. If CF is being used to measure energy, for example in a microprocessor-based application, the CF output should also be averaged to calculate power.

Because the outputs F1 and F2 operate at a much lower frequency, a lot more averaging of the instantaneous real power signal is carried out. The result is a greatly attenuated sinusoidal content and a virtually ripple-free frequency output.

Interfacing the ADE7757 to a Microcontroller for Energy Measurement

The easiest way to interface the ADE7757 to a microcontroller is to use the CF high frequency output with the output frequency scaling set to 2048 × F1, F2. This is done by setting SCF = 0 and S0 = S1 = 1 (see Table III). With full-scale ac signals on the analog inputs, the output frequency on CF will be approximately 2.867 kHz. Figure 14 illustrates one scheme that could be used to digitize the output frequency and carry out the necessary averaging mentioned in the previous section.

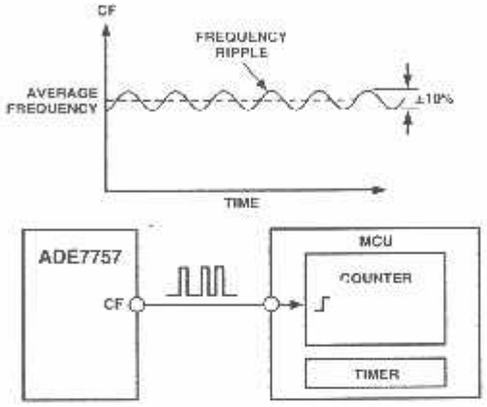


Figure 14. Interfacing the ADE7757 to an MCU

As shown, the frequency output CF is connected to an MCU counter or port. This will count the number of pulses in a given integration time, which is determined by an MCU internal timer. The average power proportional to the average frequency is given by:

$$Average\ Frequency = Average\ Power = \frac{Counter}{Time}$$

The energy consumed during an integration period is given by:

$$Energy = Average\ Power \times Time = \frac{Counter}{Time} \times Time = Counter$$

For the purpose of calibration, this integration time could be 10 to 20 seconds in order to accumulate enough pulses to ensure correct averaging of the frequency. In normal operation, the integration time could be reduced to one or two seconds depending, for example, on the required update rate of a display. With shorter integration times on the MCU, the amount of energy in each update may still have some small amount of ripple, even under steady load conditions. However, over a minute or more the measured energy will have no ripple.

Power Measurement Considerations

Calculating and displaying power information will always have some associated ripple that will depend on the integration period used in the MCU to determine average power, and also the load. For example, at light loads the output frequency may be 10 Hz. With an integration period of two seconds, only about 20 pulses will be counted. The possibility of missing one pulse always exists as the ADE7757 output frequency is running asynchronously to the MCU timer. This would result in a one-in-twenty or 5% error in the power measurement.

INTERNAL OSCILLATOR (OSC)

The nominal internal oscillator frequency is 450 kHz when used with RCKLIN with nominal value of 6.2 kΩ. The frequency outputs are directly proportional to the oscillator frequency, thus RCKLIN must have low tolerance and low temperature drift to ensure stability and linearity of the chip. The oscillator frequency is inversely proportional to the RCKLIN as shown in Figure 15. Although the internal oscillator operates when used with RCKLIN values between 5.5 kΩ and 20 kΩ, it is recommended to choose a value within the range of the nominal value as shown in Figure 15.

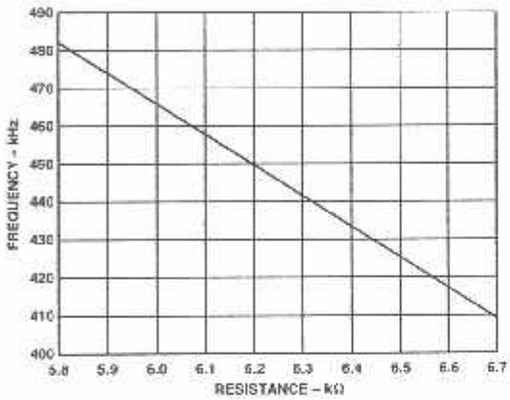


Figure 15. Effect of RCKLIN on Internal Oscillator Frequency (OSC)

TRANSFER FUNCTION

Frequency Outputs F1 and F2

The ADE7757 calculates the product of two voltage signals (on Channel V1 and Channel V2) and then low-pass filters this product to extract real power information. This real power information is then converted to a frequency. The frequency information is output on F1 and F2 in the form of active low pulses. The pulse rate at these outputs is relatively low, e.g., 0.175 Hz maximum for ac signals with S0 = S1 = 0—see Table II. This means that the frequency at these outputs is generated from real power information accumulated over a relatively long period of time. The result is an output frequency that is proportional to the average real power. The averaging of the real power signal is implicit to the digital-to-frequency conversion. The output frequency or pulse rate is related to the input voltage signals by the following equation:

$$Freq = \frac{515.84 \times V1_{rms} \times V2_{rms} \times F_{1\text{-}4}}{V_{ref}^{\ 2}}$$

where:

$Freq$ = Output frequency on F1 and F2 (Hz)

$V1_{rms}$ = Differential rms voltage signal on Channel V1 (volts)

$V2_{rms}$ = Differential rms voltage signal on Channel V2 (volts)

V_{ref} = The reference voltage (2.5 V ± 8%) (volts)

$F_{1\text{-}4}$ = One of four possible frequencies selected by using the logic inputs S0 and S1—see Table I.

Table I. F_{1-4} Frequency Selection

S1	S0	OSC Relation[1]	F_{1-4} at nominal OSC(Hz)[2]
0	0	OSC/2^{19}	0.86
0	1	OSC/2^{18}	1.72
1	0	OSC/2^{17}	3.44
1	1	OSC/2^{16}	6.86

[1]F_{1-4} is a binary fraction of the internal oscillator frequency (OSC).
[2]Values are generated using the nominal frequency of 450 kHz.

Example

In this example, with ac voltages of ±30 mV peak applied to V1 and ±165 mV peak applied to V2, the expected output frequency is calculated as follows:

F_{1-4} = $OSC/2^{19}$ Hz, $S0 = S1 = 0$

$V1_{rms}$ = $0.03/\sqrt{2}$ V

$V2_{rms}$ = $0.165/\sqrt{2}$ V

V_{ref} = 2.5 V (nominal reference value).

NOTE: If the on-chip reference is used, actual output frequencies may vary from device to device due to reference tolerance of ±8%.

$$Freq = \frac{515.85 \times 0.03 \times 0.165 \times F_1}{\sqrt{2} \times \sqrt{2} \times 2.5^2} = 0.204 \times F_1 = 0.175$$

Table II. Maximum Output Frequency on F1 and F2

S1	S0	OSC Relation	Max Frequency* for AC Inputs (Hz)
0	0	$0.204 \times F_1$	0.175
0	1	$0.204 \times F_2$	0.35
1	0	$0.204 \times F_3$	0.70
1	1	$0.204 \times F_4$	1.40

*Values are generated using the nominal frequency of 450 kHz

Frequency Output CF

The pulse output CF (Calibration Frequency) is intended for calibration purposes. The output pulse rate on CF can be up to 2048 times the pulse rate on F1 and F2. The lower the F_{1-4} frequency selected, the higher the CF scaling (except for the high frequency mode SCF = 0, S1 = S0 = 1). Table III shows how the two frequencies are related, depending on the states of the logic inputs S0, S1, and SCF. Due to its relatively high pulse rate, the frequency at CF logic output is proportional to the instantaneous real power. As with F1 and F2, CF is derived from the output of the low-pass filter after multiplication. However, because the output frequency is high, this real power information is accumulated over a much shorter time. Therefore less averaging is carried out in the digital-to-frequency conversion. With much less averaging of the real power signal, the CF output is much more responsive to power fluctuations (see Signal Processing Block in Figure 3).

Table III. Maximum Output Frequency on CF

SCF	S1	S0	CF Max for AC Signals (Hz)*
1	0	0	128 × F1, F2 = 22.4
0	0	0	64 × F1, F2 = 11.2
1	0	1	64 × F1, F2 = 22.4
0	0	1	32 × F1, F2 = 11.2
1	1	0	32 × F1, F2 = 22.4
0	1	0	16 × F1, F2 = 11.2
1	1	1	16 × F1, F2 = 22.4
0	1	1	2048 × F1, F2 = 2.867 kHz

*Values are generated using the nominal frequency of 450 kHz

SELECTING A FREQUENCY FOR AN ENERGY METER APPLICATION

As shown in Table I, the user can select one of four frequencies. This frequency selection determines the maximum frequency on F1 and F2. These outputs are intended for driving an energy register (electromechanical or others). Since only four different output frequencies can be selected, the available frequency selection has been optimized for a meter constant of 100 imp/kWhr with a maximum current of between 10 A and 120 A. Table IV shows the output frequency for several maximum currents (I_{MAX}) with a line voltage of 220 V. In all cases, the meter constant is 100 imp/kWhr.

Table IV. F1 and F2 Frequency at 100 imp/kWhr

I_{MAX} (A)	F1 and F2 (Hz)
12.5	0.076
25.0	0.153
40.0	0.244
60.0	0.367
80.0	0.489
120.0	0.733

The F_{1-4} frequencies allow complete coverage of this range of output frequencies (F1, F2). When designing an energy meter, the nominal design voltage on Channel V2 (voltage) should be set to half-scale to allow for calibration of the meter constant. The current channel should also be no more than half-scale when the meter sees maximum load. This will allow overcurrent signals and signals with high crest factors to be accommodated. Table V shows the output frequency on F1 and F2 when both analog inputs are half-scale. The frequencies listed in Table V align very well with those listed in Table IV for maximum load.

Table V. F1 and F2 Frequency with Half-Scale AC Inputs

S1	S0	F_{1-4} (Hz)*	Frequency on F1 and F2– CH1 and CH2 Half-Scale AC Input*	
0	0	0.86	$0.051 \times F_1$	0.044 Hz
0	1	1.72	$0.051 \times F_2$	0.088 Hz
1	0	3.44	$0.051 \times F_3$	0.176 Hz
1	1	6.86	$0.051 \times F_4$	0.352 Hz

*Values are generated using the nominal frequency of 450 kHz

When selecting a suitable F_{1-4} frequency for a meter design, the frequency output at I_{MAX} (maximum load) with a meter constant of 100 imp/kWhr should be compared with column four of Table V. The closest frequency in Table V will determine the best choice of frequency (F_{1-4}). For example, if a meter with a maximum current of 25 A is being designed, the output frequency on F1 and F2 with a meter constant of 100 imp/kWhr is 0.153 Hz at 25 A and 220 V (from Table IV). Looking at Table V, the closest frequency to 0.153 Hz in column four is 0.176 Hz. Therefore, F_3 (3.44 Hz—see Table I) is selected for this design.

Frequency Outputs

Figure 1 shows a timing diagram for the various frequency outputs. The outputs F1 and F2 are the low frequency outputs that can be used to directly drive a stepper motor or electromechanical impulse counter. The F1 and F2 outputs provide two alternating low frequency pulses. The F1 and F2 pulsewidths (t_1) are set such that if it falls below 1062 ms (0.942 Hz) they are set to half of their period. The maximum output frequencies for F1 and F2 are shown in Table II.

The high frequency CF output is intended to be used for communications and calibration purposes. CF produces a 173 ms-wide active high pulse (t_4) at a frequency proportional to active power. The CF output frequencies are given in Table III. As in the case of F1 and F2, if the period of CF (t_5) falls below 346 ms, the CF pulsewidth is set to half the period. For example, if the CF frequency is 20 Hz, the CF pulsewidth is 25 ms.

NOTE: When the high frequency mode is selected, (i.e., SCF = 0, S1 = S0 = 1) the CF pulsewidth is fixed at 35 µs. Therefore t_4 will always be 35 µs, regardless of output frequency on CF.

NO LOAD THRESHOLD

The ADE7757 also includes a "no-load threshold" and "start-up current" feature that will eliminate any creep effects in the meter. The ADE7757 is designed to issue a minimum output frequency. Any load generating a frequency lower than this minimum frequency will not cause a pulse to be issued on F1, F2, or CF. The minimum output frequency is given as 0.0014% of the full-scale output frequency for each of the F_{1-4} frequency selections (see Table I). For example, for an energy meter with a meter constant of 100 imp/kWhr on F1, F2 using F_3 (3.44 Hz), the minimum output frequency at F1 or F2 would be 0.0014% of 3.44 Hz or 4.81×10^{-5} Hz. This would be 3.08×10^{-3} Hz at CF ($64 \times$ F1 Hz) when SCF = S0 = 1, S1 = 0. In this example, the no-load threshold would be equivalent to 1.7 W of load or a start-up current of 8 mA at 220 V. Compare this value to the IEC1036 specification which states that the meter must start up with a load equal to or less than 0.4% Ib. For a 5A (Ib) meter, 0.4% of Ib is equivalent to 20 mA.

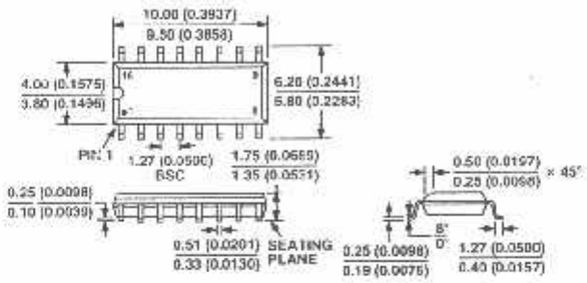
NEGATIVE POWER INFORMATION

The ADE7757 detects when the current and voltage channels have a phase shift greater than 90°. This mechanism can detect wrong connection of the meter or generation of negative power. The REVP pin output will go active high when negative power is detected and active low if positive power is detected. The REVP pin output changes state as a pulse is issued on CF. The REVP pin is not functional in the current version and will only work in the A version (ADE7757A).

OUTLINE DIMENSIONS

16-Lead Standard Small Outline Package
Narrow Body
(RN-16)

Dimensions shown in millimeters and (inches)



CONTROLLING DIMENSIONS ARE IN MILLIMETERS; INCH DIMENSIONS (IN PARENTHESES) ARE ROUNDED-OFF MILLIMETER EQUIVALENTS FOR REFERENCE ONLY AND ARE NOT APPROPRIATE FOR USE IN DESIGN

COMPLIANT TO JEDEC STANDARDS MS-012AC

C02898-0-8/0210

PRINTED IN U.S.A.

FAIRCHILD
SEMICONDUCTOR®

April 2007

74AC253, 74ACT253
Dual 4-Input Multiplexer with 3-STATE Outputs

Features

- I_{CC} and I_{OZ} reduced by 50%
- Multifunction capability
- Non inverting 3-STATE outputs
- Outputs source/sink 24mA
- ACT253 has TTL-compatible inputs

General Description

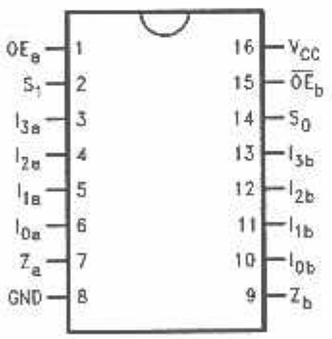
The AC/ACT253 is a dual 4-input multiplexer with 3-STATE outputs. It can select two bits of data from four sources using common select inputs. The outputs may be individually switched to a high impedance state with a HIGH on the respective Output Enable ($\overline{OE}$) inputs, allowing the outputs to interface directly with bus oriented systems.

Ordering Information

Order Number	Package Number	Package Description
74AC253SC	M16A	16-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-012, 0.150" Narrow
74AC253SJ	M16D	16-Lead Small Outline Package (SOP), EIAJ TYPE II, 5.3mm Wide
74AC253PC	N16E	16-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300" Wide
74ACT253SC	M16A	16-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-012, 0.150" Narrow
74ACT253SJ	M16D	16-Lead Small Outline Package (SOP), EIAJ TYPE II, 5.3mm Wide
74ACT253MTC	MTC16	16-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 4.4mm Wide

Device also available Tape and Reel. Specify by appending suffix letter "X" to the ordering number.

Connection Diagram



Pin Descriptions

Pin Names	Description
I_{0a}–I_{3a}	Side A Data Inputs
I_{0b}–I_{3b}	Side B Data Inputs
S_0, S_1	Common Select Inputs
$\overline{OE}_a$	Side A Output Enable Input
$\overline{OE}_b$	Side B Output Enable Input
Z_a, Z_b	3-STATE Outputs

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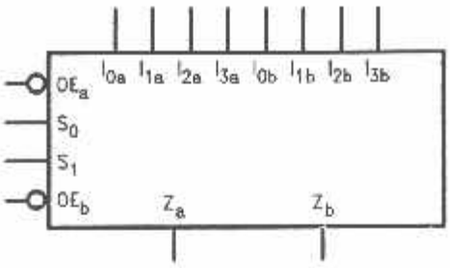
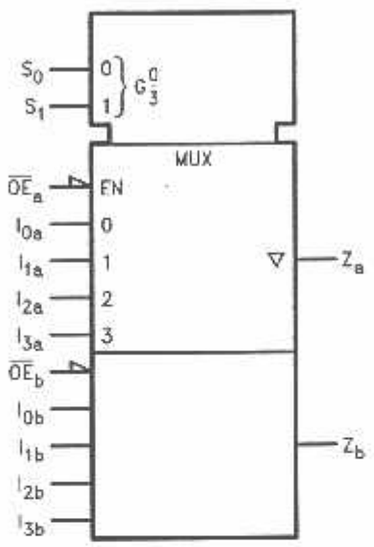
Logic Diagram



IEEE/IEC



Functional Description

The AC/ACT253 contains two identical 4-input multiplexers with 3-STATE outputs. They select two bits from four sources selected by common Select inputs (S_0, S_1). The 4-input multiplexers have individual Output Enable ($\overline{OE}_a$, $\overline{OE}_b$) inputs which, when HIGH, force the outputs to a high impedance (High Z) state. This device is the logic implementation of a 2-pole, 4-position switch, where the position of the switch is determined by the logic levels supplied to the two select inputs. The logic equations for the outputs are shown:

$$Z_a = \overline{OE}_a \cdot (I_{0a} \cdot \overline{S}_1 \cdot \overline{S}_0 + I_{1a} \cdot \overline{S}_1 \cdot S_0 + I_{2a} \cdot S_1 \cdot \overline{S}_0 + I_{3a} \cdot S_1 \cdot S_0)$$

$$Z_b = \overline{OE}_b \cdot (I_{0b} \cdot \overline{S}_1 \cdot \overline{S}_0 + I_{1b} \cdot \overline{S}_1 \cdot S_0 + I_{2b} \cdot S_1 \cdot \overline{S}_0 + I_{3b} \cdot S_1 \cdot S_0)$$

If the outputs of 3-STATE devices are tied together, all but one device must be in the high impedance state to avoid high currents that would exceed the maximum ratings. Designers should ensure that Output Enable signals to 3-STATE devices whose outputs are tied together are designed so that there is no overlap.

Truth Table

Select Inputs		Data Inputs				Output Enable	Outputs
S_0	S_1	I_0	I_1	I_2	I_3	$\overline{OE}$	Z
X	X	X	X	X	X	H	Z
L	L	L	X	X	X	L	L
L	L	H	X	X	X	L	H
H	L	X	L	X	X	L	L
H	L	X	H	X	X	L	H
L	H	X	X	L	X	L	L
L	H	X	X	H	X	L	H
H	H	X	X	X	L	L	L
H	H	X	X	X	H	L	H

Address Inputs S_0 and S_1 are common to both sections.

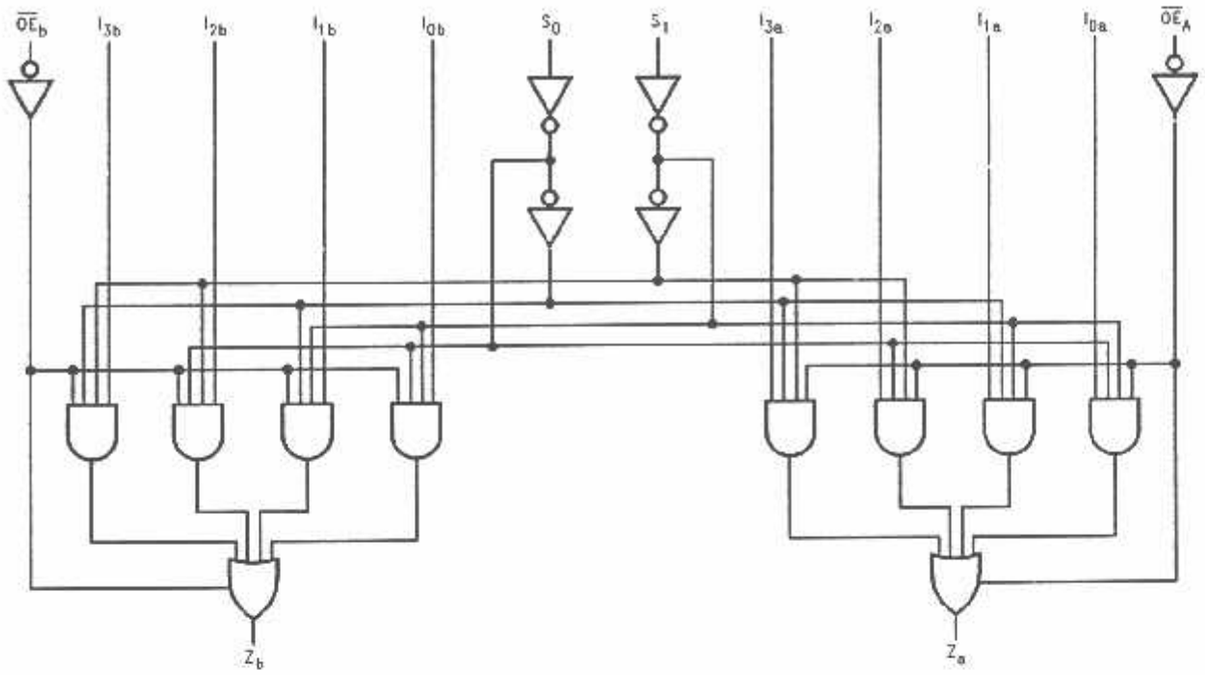
H = HIGH Voltage Level

L = LOW Voltage Level

X = Immaterial

Z = High Impedance

Logic Diagram



Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

Figure 1.

Absolute Maximum Ratings

Stresses exceeding the absolute maximum ratings may damage the device. The device may not function or be operable above the recommended operating conditions and stressing the parts to these levels is not recommended. In addition, extended exposure to stresses above the recommended operating conditions may affect device reliability. The absolute maximum ratings are stress ratings only.

Symbol	Parameter	Rating
V_{CC}	Supply Voltage	−0.5V to +7.0V
I_{IK}	DC Input Diode Current	
	$V_I = -0.5V$	−20mA
	$V_I = V_{CC} + 0.5V$	+20mA
V_I	DC Input Voltage	−0.5V to V_{CC} + 0.5V
I_{OK}	DC Output Diode Current	
	$V_O = -0.5V$	−20mA
	$V_O = V_{CC} + 0.5V$	+20mA
V_O	DC Output Voltage	−0.5V to V_{CC} + 0.5V
I_O	DC Output Source or Sink Current	±50mA
I_{CC} or I_{GND}	DC V_{CC} or Ground Current per Output Pin	±50mA
T_{STG}	Storage Temperature	−65°C to +150°C
T_J	Junction Temperature	140°C

Recommended Operating Conditions

The Recommended Operating Conditions table defines the conditions for actual device operation. Recommended operating conditions are specified to ensure optimal performance to the datasheet specifications. Fairchild does not recommend exceeding them or designing to absolute maximum ratings.

Symbol	Parameter	Rating
V_{CC}	Supply Voltage	
	AC	2.0V to 6.0V
	ACT	4.5V to 5.5V
V_I	Input Voltage	0V to V_{CC}
V_O	Output Voltage	0V to V_{CC}
T_A	Operating Temperature	−40°C to +85°C
$\Delta V / \Delta t$	Minimum Input Edge Rate, AC Devices:	125mV/ns
	V_{IN} from 30% to 70% of V_{CC}, V_{CC} @ 3.3V, 4.5V, 5.5V	
$\Delta V / \Delta t$	Minimum Input Edge Rate, ACT Devices:	125mV/ns
	V_{IN} from 0.8V to 2.0V, V_{CC} @ 4.5V, 5.5V	

DC Electrical Characteristics for AC

Symbol	Parameter	V_{CC} (V)	Conditions	T_A = +25°C	T_A = −40°C to +85°C		Units
				Typ.	Guaranteed Limits		
V_{IH}	Minimum HIGH Level Input Voltage	3.0	V_{OUT} = 0.1V or V_{CC} − 0.1V	1.5	2.1	2.1	V
		4.5		2.25	3.15	3.15	
		5.5		2.75	3.85	3.85	
V_{IL}	Maximum LOW Level Input Voltage	3.0	V_{OUT} = 0.1V or V_{CC} − 0.1V	1.5	0.9	0.9	V
		4.5		2.25	1.35	1.35	
		5.5		2.75	1.65	1.65	
V_{OH}	Minimum HIGH Level Output Voltage	3.0	I_{OUT} = −50μA	2.99	2.9	2.9	V
		4.5		4.49	4.4	4.4	
		5.5		5.49	5.4	5.4	
		3.0	V_{IN} = V_{IL} or V_{IH}; I_{OH} = −12mA		2.56	2.46	
		4.5	I_{OH} = −24mA		3.86	3.76	
		5.5	I_{OH} = −24mA[1]		4.86	4.76	
V_{OL}	Maximum LOW Level Output Voltage	3.0	I_{OUT} = 50μA	0.002	0.1	0.1	V
		4.5		0.001	0.1	0.1	
		5.5		0.001	0.1	0.1	
		3.0	V_{IN} = V_{IL} or V_{IH}; I_{OL} = 12mA		0.36	0.44	
		4.5	I_{OL} = 24mA		0.36	0.44	
		5.5	I_{OL} = 24mA[1]		0.36	0.44	
I_{IN}[3]	Maximum Input Leakage Current	5.5	V_I = V_{CC}, GND		±0.1	±1.0	μA
I_{OZ}	Maximum 3-STATE Current	5.5	V_I (OE) = V_{IL}, V_{IH}; V_I = V_{CC}, GND; V_O = V_{CC}, GND		±0.25	±2.5	μA
I_{OLD}	Minimum Dynamic Output Current[2]	5.5	V_{OLD} = 1.65V Max.			75	mA
I_{OHD}		5.5	V_{OHD} = 3.85V Min.			−75	mA
I_{CC}[3]	Maximum Quiescent Supply Current	5.5	V_{IN} = V_{CC} or GND		4.0	40.0	μA

Notes:

1. All outputs loaded; thresholds on input associated with output under test.
2. Maximum test duration 2.0ms, one output loaded at a time.
3. I_{IN} and I_{CC} @ 3.0V are guaranteed to be less than or equal to the respective limit @ 5.5V V_{CC}.

DC Electrical Characteristics for ACT

Symbol	Parameter	V_{CC} (V)	Conditions	$T_A = +25°C$	$T_A = -40°C$ to $+85°C$		Units
				Typ.	Guaranteed Limits		
V_{IH}	Minimum HIGH Level Input Voltage	4.5	$V_{OUT} = 0.1V$ or $V_{CC} - 0.1V$	1.5	2.0	2.0	V
		5.5		1.5	2.0	2.0	
V_{IL}	Maximum LOW Level Input Voltage	4.5	$V_{OUT} = 0.1V$ or $V_{CC} - 0.1V$	1.5	0.8	0.8	V
		5.5		1.5	0.8	0.8	
V_{OH}	Minimum HIGH Level Output Voltage	4.5	$I_{OUT} = -50\mu A$	4.49	4.4	4.4	V
		5.5		5.49	5.4	5.4	
		4.5	$V_{IN} = V_{IL}$ or V_{IH}; $I_{OH} = -24mA$		3.86	3.76	
		5.5	$I_{OH} = -24mA$[4]		4.86	4.76	
V_{OL}	Maximum LOW Level Output Voltage	4.5	$I_{OUT} = 50\mu A$	0.001	0.1	0.1	V
		5.5		0.001	0.1	0.1	
		4.5	$V_{IN} = V_{IL}$ or V_{IH}; $I_{OL} = 24mA$		0.36	0.44	
		5.5	$I_{OL} = 24mA$[4]		0.36	0.44	
I_{IN}	Maximum Input Leakage Current	5.5	$V_I = V_{CC}$, GND		±0.1	±1.0	μA
I_{OZ}	Maximum 3-STATE Current	5.5	$V_I = V_{IL}, V_{IH}$; $V_O = V_{CC}$, GND		±0.25	±2.5	μA
I_{CCT}	Maximum I_{CC}/Input	5.5	$V_I = V_{CC} - 2.1V$	0.6		1.5	mA
I_{OLD}	Minimum Dynamic Output Current[5]	5.5	$V_{OLD} = 1.65V$ Max.			75	mA
I_{OHD}		5.5	$V_{OHD} = 3.85V$ Min.			−75	mA
I_{CC}	Maximum Quiescent Supply Current	5.5	$V_{IN} = V_{CC}$ or GND		4.0	40.0	μA

Notes:

4. All outputs loaded; thresholds on input associated with output under test.

5. Maximum test duration 2.0ms, one output loaded at a time.

AC Electrical Characteristics for AC

Symbol	Parameter	V_{CC} (V)[6]	T_A = +25°C, C_L = 50pF			T_A = –40°C to +85°C, C_L = 50pF		Units
			Min.	Typ.	Max.	Min	Max	
t_{PLH}	Propagation Delay, S_n to Z_n	3.3	2.0	8.5	15.5	2.0	17.5	ns
		5.0	2.0	6.5	11.0	1.5	12.5	
t_{PHL}	Propagation Delay, S_n to Z_n	3.3	2.5	9.5	16.0	2.0	18.0	ns
		5.0	2.0	7.0	11.5	1.5	13.0	
t_{PLH}	Propagation Delay, I_n to Z_n	3.3	1.5	7.0	14.5	1.5	17.0	ns
		5.0	1.5	5.5	10.0	1.5	11.5	
t_{PHL}	Propagation Delay, I_n to Z_n	3.3	2.0	7.5	13.0	1.5	15.0	ns
		5.0	1.5	5.5	9.5	1.5	11.0	
t_{PZH}	Output Enable Time	3.3	1.5	4.5	8.0	1.0	8.5	ns
		5.0	1.5	3.5	6.0	1.0	6.5	
t_{PZL}	Output Enable Time	3.3	1.5	5.0	8.0	1.0	9.0	ns
		5.0	1.5	3.5	6.0	1.0	7.0	
t_{PHZ}	Output Disable Time	3.3	2.0	5.5	9.5	1.5	10.0	ns
		5.0	2.0	5.0	8.0	1.5	8.5	
t_{PLZ}	Output Disable Time	3.3	1.5	5.0	8.0	1.0	9.0	ns
		5.0	1.5	4.0	7.0	1.0	7.5	

Note:

6. Voltage range 3.3 is 3.3V ± 0.3V. Voltage range 5.0 is 5.0V ± 0.5V.

AC Electrical Characteristics for ACT

Symbol	Parameter	V_{CC} (V)[7]	T_A = +25°C, C_L = 50pF			T_A = –40°C to +85°C, C_L = 50pF		Units
			Min.	Typ.	Max.	Min.	Max.	
t_{PLH}	Propagation Delay, S_n to Z_n	5.0	2.0	7.0	11.5	2.0	13.0	ns
t_{PHL}	Propagation Delay, S_n to Z_n	5.0	3.0	7.5	13.0	2.5	14.5	ns
t_{PLH}	Propagation Delay, I_n to Z_n	5.0	2.5	5.5	10.0	2.0	11.0	ns
t_{PHL}	Propagation Delay, I_n to Z_n	5.0	3.5	6.5	11.0	3.0	12.5	ns
t_{PZH}	Output Enable Time	5.0	2.0	4.5	7.5	1.5	8.5	ns
t_{PZL}	Output Enable Time	5.0	2.0	5.0	8.0	1.5	9.0	ns
t_{PHZ}	Output Disable Time	5.0	3.0	6.0	9.5	2.5	10.0	ns
t_{PLZ}	Output Disable Time	5.0	2.5	4.5	7.5	2.0	8.5	ns

Note:

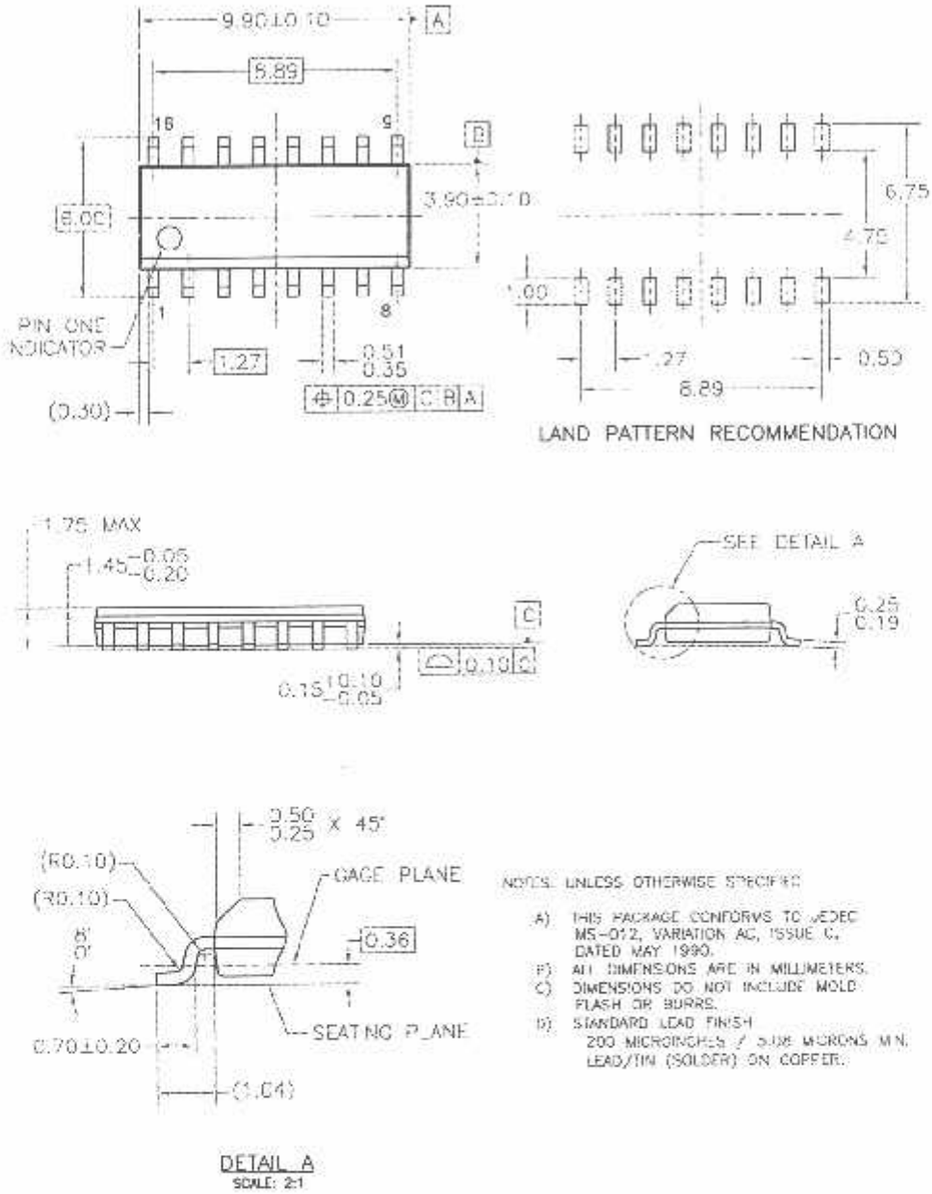
7. Voltage range 5.0 is 5.0V ± 0.5V.

Capacitance

Symbol	Parameter	Conditions	Typ.	Units
C_{IN}	Input Capacitance	V_{CC} = OPEN	4.5	pF
C_{PD}	Power Dissipation Capacitance	V_{CC} = 5.0V	50.0	pF

Physical Dimensions

Dimensions are in millimeters unless otherwise noted.

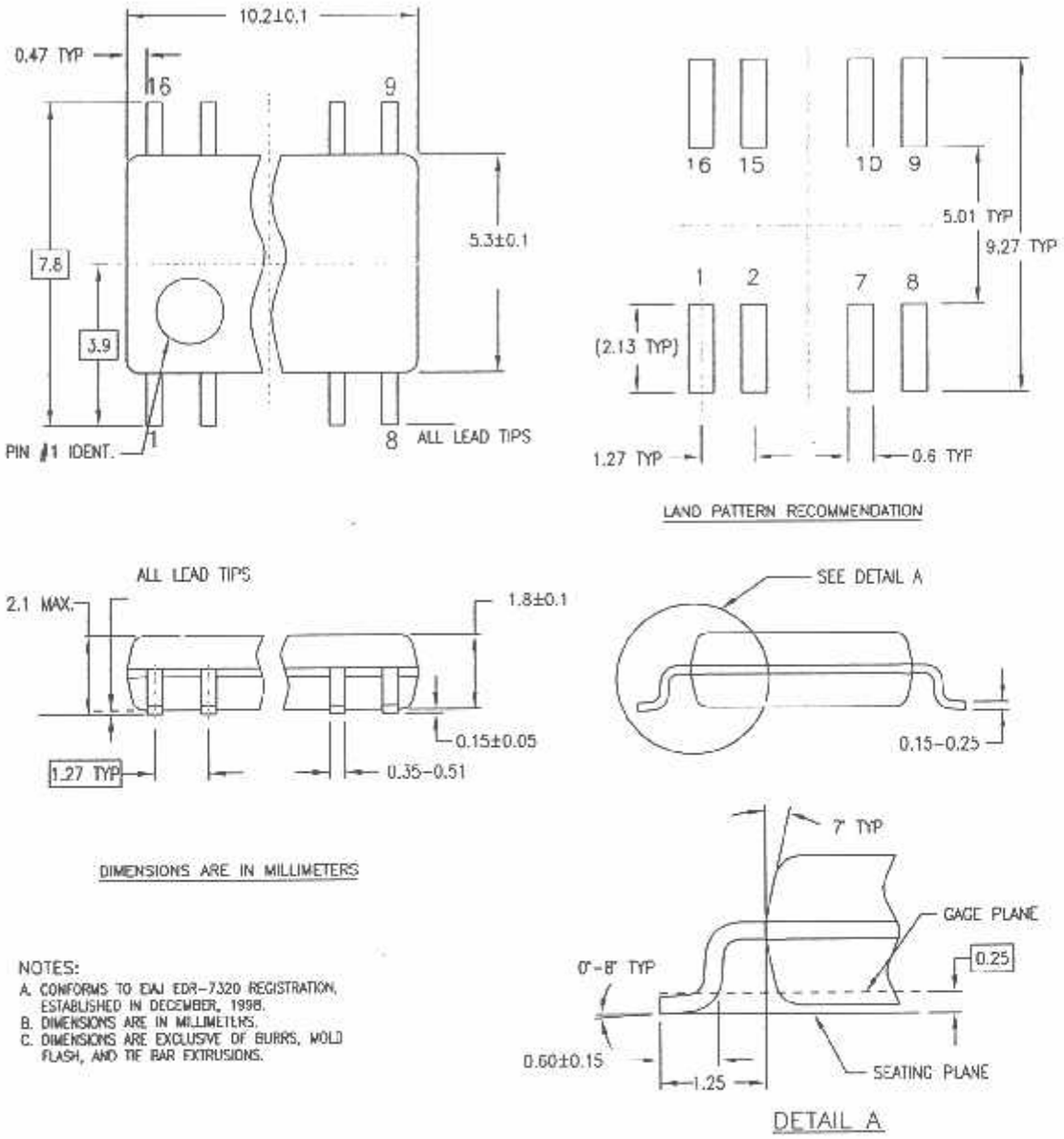


M16AREVK

Figure 2. 16-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-012, 0.150" Narrow
Package Number M16A

Physical Dimensions (Continued)

Dimensions are in millimeters unless otherwise noted.



NOTES:

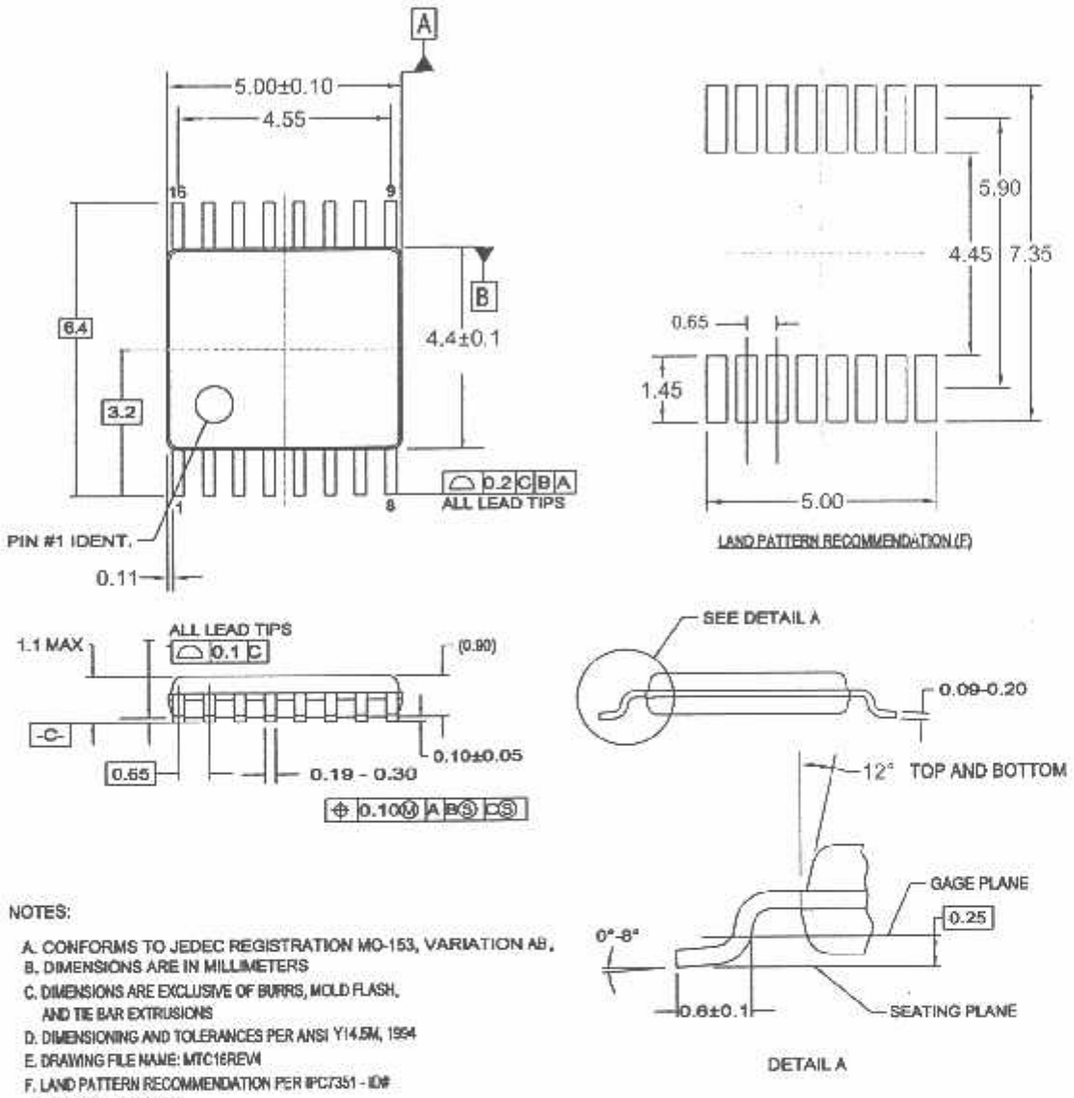
A. CONFORMS TO EIAJ EDR-7320 REGISTRATION, ESTABLISHED IN DECEMBER, 1998.
B. DIMENSIONS ARE IN MILLIMETERS.
C. DIMENSIONS ARE EXCLUSIVE OF BURRS, MOLD FLASH, AND TIE BAR EXTRUSIONS.

M16DREVC

Figure 3. 16-Lead Small Outline Package (SOP), EIAJ TYPE II, 5.3mm Wide
Package Number M16D

Physical Dimensions (Continued)

Dimensions are in millimeters unless otherwise noted.



NOTES:

A. CONFORMS TO JEDEC REGISTRATION MO-153, VARIATION AB,
B. DIMENSIONS ARE IN MILLIMETERS
C. DIMENSIONS ARE EXCLUSIVE OF BURRS, MOLD FLASH, AND TIE BAR EXTRUSIONS
D. DIMENSIONING AND TOLERANCES PER ANSI Y14.5M, 1994
E. DRAWING FILE NAME: MTC16REVH
F. LAND PATTERN RECOMMENDATION PER IPC7351 - ID# TSOP65P640X110-16N

MTC16rev4

Figure 4. 16-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 4.4mm Wide
Package Number MTC16

Physical Dimensions (Continued)

Dimensions are in inches (millimeters) unless otherwise noted.

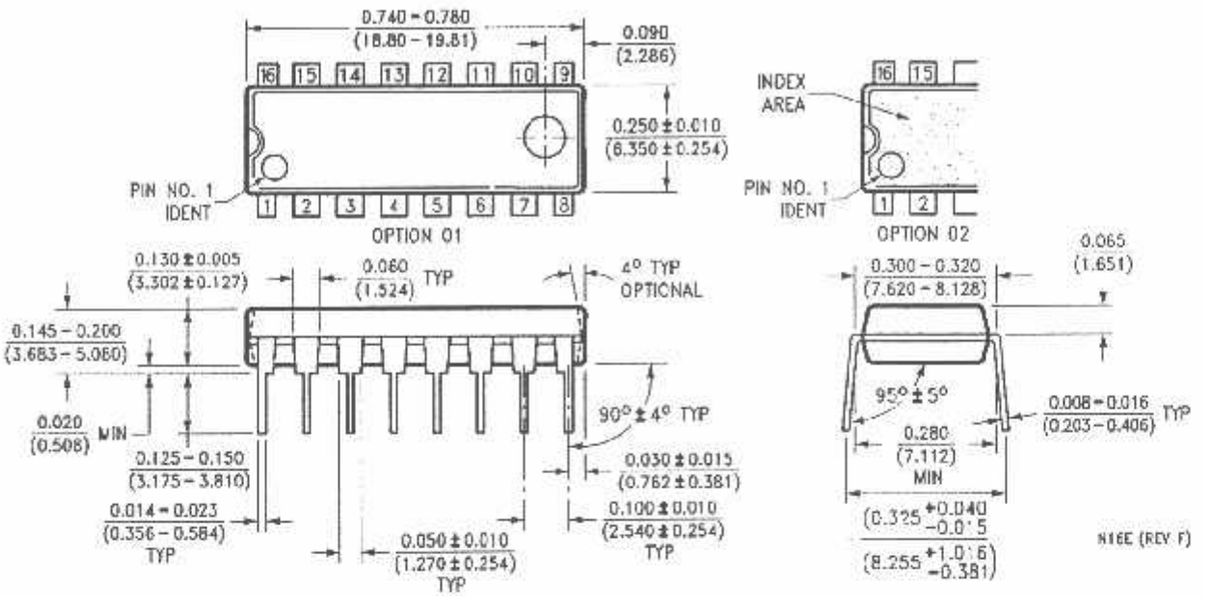


Figure 5. 16-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300" Wide
Package Number N16E

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Definition of Terms

Datasheet Identification	Product Status	Definition
Advance Information	Formative or In Design	This datasheet contains the design specifications for product development. Specifications may change in any manner without notice.
Preliminary	First Production	This datasheet contains preliminary data; supplementary data will be published at a later date. Fairchild Semiconductor reserves the right to make changes at any time without notice to improve design.
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Rev. I24

FAIRCHILD
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April 2007

74AC253, 74ACT253
Dual 4-Input Multiplexer with 3-STATE Outputs

Features

- I_{CC} and I_{OZ} reduced by 50%
- Multifunction capability
- Non inverting 3-STATE outputs
- Outputs source/sink 24mA
- ACT253 has TTL-compatible inputs

General Description

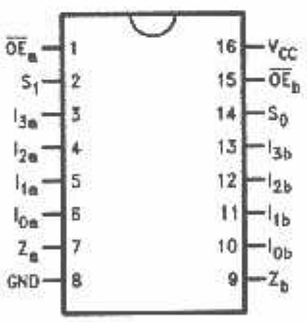
The AC/ACT253 is a dual 4-input multiplexer with 3-STATE outputs. It can select two bits of data from four sources using common select inputs. The outputs may be individually switched to a high impedance state with a HIGH on the respective Output Enable ($\overline{OE}$) inputs, allowing the outputs to interface directly with bus oriented systems.

Ordering Information

Order Number	Package Number	Package Description
74AC253SC	M16A	16-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-012, 0.150" Narrow
74AC253SJ	M16D	16-Lead Small Outline Package (SOP), EIAJ TYPE II, 5.3mm Wide
74AC253PC	N16E	16-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300" Wide
74ACT253SC	M16A	16-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-012, 0.150" Narrow
74ACT253SJ	M16D	16-Lead Small Outline Package (SOP), EIAJ TYPE II, 5.3mm Wide
74ACT253MTC	MTC16	16-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 4.4mm Wide

Device also available Tape and Reel. Specify by appending suffix letter "X" to the ordering number.

Connection Diagram



Pin Descriptions

Pin Names	Description
I_{0a}–I_{3a}	Side A Data Inputs
I_{0b}–I_{3b}	Side B Data Inputs
S_0, S_1	Common Select Inputs
$\overline{OE}_a$	Side A Output Enable Input
$\overline{OE}_b$	Side B Output Enable Input
Z_a, Z_b	3-STATE Outputs

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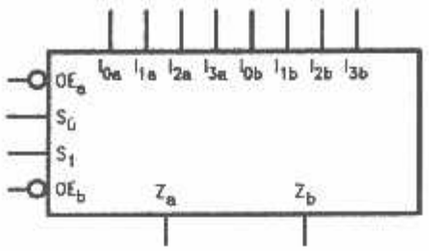
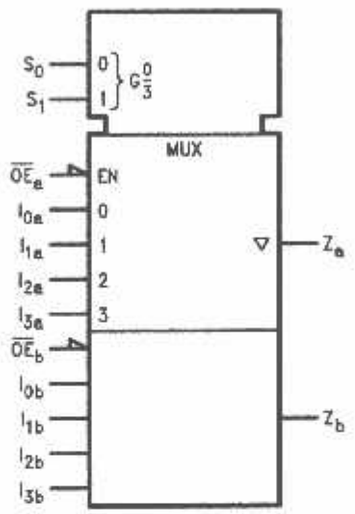
Logic Diagram



IEEE/IEC



Functional Description

The AC/ACT253 contains two identical 4-input multiplexers with 3-STATE outputs. They select two bits from four sources selected by common Select inputs (S_0, S_1). The 4-input multiplexers have individual Output Enable ($\overline{OE}_a$, $\overline{OE}_b$) inputs which, when HIGH, force the outputs to a high impedance (High Z) state. This device is the logic implementation of a 2-pole, 4-position switch, where the position of the switch is determined by the logic levels supplied to the two select inputs. The logic equations for the outputs are shown:

$$Z_a = \overline{OE}_a \cdot (I_{0a} \cdot \overline{S}_1 \cdot \overline{S}_0 + I_{1a} \cdot \overline{S}_1 \cdot S_0 + I_{2a} \cdot S_1 \cdot \overline{S}_0 + I_{3a} \cdot S_1 \cdot S_0)$$

$$Z_b = \overline{OE}_b \cdot (I_{0b} \cdot \overline{S}_1 \cdot \overline{S}_0 + I_{1b} \cdot \overline{S}_1 \cdot S_0 + I_{2b} \cdot S_1 \cdot \overline{S}_0 + I_{3b} \cdot S_1 \cdot S_0)$$

If the outputs of 3-STATE devices are tied together, all but one device must be in the high impedance state to avoid high currents that would exceed the maximum ratings. Designers should ensure that Output Enable signals to 3-STATE devices whose outputs are tied together are designed so that there is no overlap.

Truth Table

Select Inputs		Data Inputs				Output Enable	Outputs
S_0	S_1	I_0	I_1	I_2	I_3	$\overline{OE}$	Z
X	X	X	X	X	X	H	Z
L	L	L	X	X	X	L	L
L	L	H	X	X	X	L	H
H	L	X	L	X	X	L	L
H	L	X	H	X	X	L	H
L	H	X	X	L	X	L	L
L	H	X	X	H	X	L	H
H	H	X	X	X	L	L	L
H	H	X	X	X	H	L	H

Address Inputs S_0 and S_1 are common to both sections.

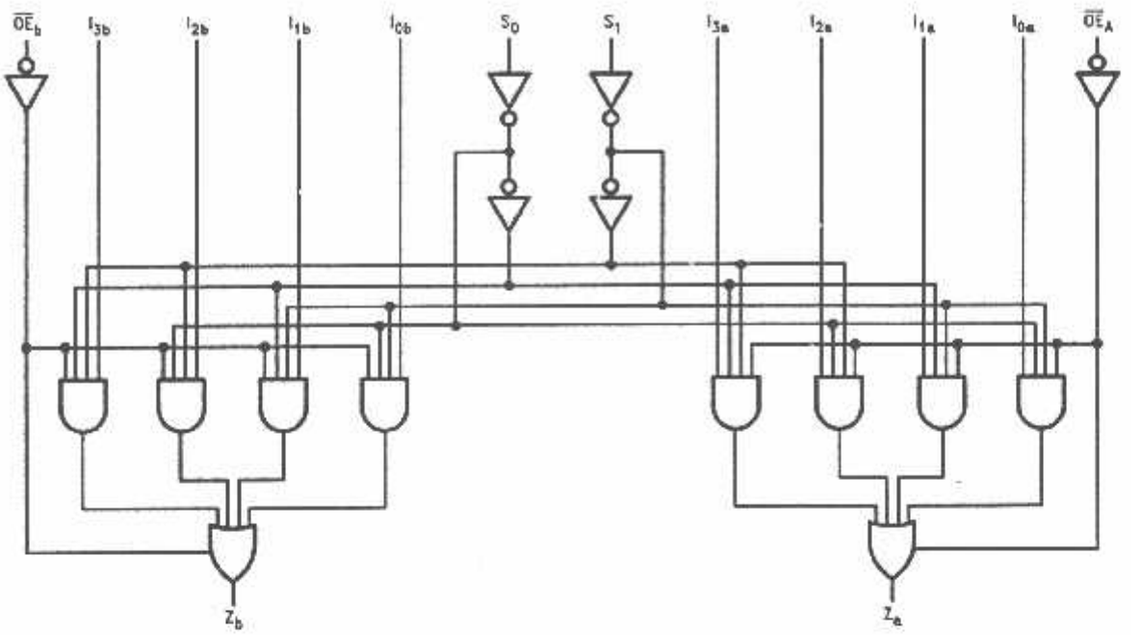
H = HIGH Voltage Level

L = LOW Voltage Level

X = Immaterial

Z = High Impedance

Logic Diagram



Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

Figure 1.

Absolute Maximum Ratings

Stresses exceeding the absolute maximum ratings may damage the device. The device may not function or be operable above the recommended operating conditions and stressing the parts to these levels is not recommended. In addition, extended exposure to stresses above the recommended operating conditions may affect device reliability. The absolute maximum ratings are stress ratings only.

Symbol	Parameter	Rating
V_{CC}	Supply Voltage	−0.5V to +7.0V
I_{IK}	DC Input Diode Current	
	$V_I = -0.5V$	−20mA
	$V_I = V_{CC} + 0.5V$	+20mA
V_I	DC Input Voltage	−0.5V to V_{CC} + 0.5V
I_{OK}	DC Output Diode Current	
	$V_O = -0.5V$	−20mA
	$V_O = V_{CC} + 0.5V$	+20mA
V_O	DC Output Voltage	−0.5V to V_{CC} + 0.5V
I_O	DC Output Source or Sink Current	±50mA
I_{CC} or I_{GND}	DC V_{CC} or Ground Current per Output Pin	±50mA
T_{STG}	Storage Temperature	−65°C to +150°C
T_J	Junction Temperature	140°C

Recommended Operating Conditions

The Recommended Operating Conditions table defines the conditions for actual device operation. Recommended operating conditions are specified to ensure optimal performance to the datasheet specifications. Fairchild does not recommend exceeding them or designing to absolute maximum ratings.

Symbol	Parameter	Rating
V_{CC}	Supply Voltage	
	AC	2.0V to 6.0V
	ACT	4.5V to 5.5V
V_I	Input Voltage	0V to V_{CC}
V_O	Output Voltage	0V to V_{CC}
T_A	Operating Temperature	−40°C to +85°C
$\Delta V / \Delta t$	Minimum Input Edge Rate, AC Devices:	125mV/ns
	V_{IN} from 30% to 70% of V_{CC}, V_{CC} @ 3.3V, 4.5V, 5.5V	
$\Delta V / \Delta t$	Minimum Input Edge Rate, ACT Devices:	125mV/ns
	V_{IN} from 0.8V to 2.0V, V_{CC} @ 4.5V, 5.5V	

DC Electrical Characteristics for AC

Symbol	Parameter	V_{CC} (V)	Conditions	$T_A = +25°C$	$T_A = -40°C$ to $+85°C$		Units
				Typ.	Guaranteed Limits		
V_{IH}	Minimum HIGH Level Input Voltage	3.0	$V_{OUT} = 0.1V$ or $V_{CC} - 0.1V$	1.5	2.1	2.1	V
		4.5		2.25	3.15	3.15	
		5.5		2.75	3.85	3.85	
V_{IL}	Maximum LOW Level Input Voltage	3.0	$V_{OUT} = 0.1V$ or $V_{CC} - 0.1V$	1.5	0.9	0.9	V
		4.5		2.25	1.35	1.35	
		5.5		2.75	1.65	1.65	
V_{OH}	Minimum HIGH Level Output Voltage	3.0	$I_{OUT} = -50\mu A$	2.99	2.9	2.9	V
		4.5		4.49	4.4	4.4	
		5.5		5.49	5.4	5.4	
		3.0	$V_{IN} = V_{IL}$ or V_{IH}: $I_{OH} = -12mA$		2.56	2.46	
		4.5	$I_{OH} = -24mA$		3.86	3.76	
		5.5	$I_{OH} = -24mA$[1]		4.86	4.76	
V_{OL}	Maximum LOW Level Output Voltage	3.0	$I_{OUT} = 50\mu A$	0.002	0.1	0.1	V
		4.5		0.001	0.1	0.1	
		5.5		0.001	0.1	0.1	
		3.0	$V_{IN} = V_{IL}$ or V_{IH}: $I_{OL} = 12mA$		0.36	0.44	
		4.5	$I_{OL} = 24mA$		0.36	0.44	
		5.5	$I_{OL} = 24mA$[1]		0.36	0.44	
I_{IN}[3]	Maximum Input Leakage Current	5.5	$V_I = V_{CC}$, GND		±0.1	±1.0	μA
I_{OZ}	Maximum 3-STATE Current	5.5	V_I (OE) = V_{IL}, V_{IH}; $V_I = V_{CC}$, GND; $V_O = V_{CC}$, GND		±0.25	±2.5	μA
I_{OLD}	Minimum Dynamic Output Current[2]	5.5	$V_{OLD} = 1.65V$ Max.			75	mA
I_{OHD}		5.5	$V_{OHD} = 3.85V$ Min.			-75	mA
I_{CC}[3]	Maximum Quiescent Supply Current	5.5	$V_{IN} = V_{CC}$ or GND		4.0	40.0	μA

Notes:

1. All outputs loaded; thresholds on input associated with output under test.
2. Maximum test duration 2.0ms, one output loaded at a time.
3. I_{IN} and I_{CC} @ 3.0V are guaranteed to be less than or equal to the respective limit @ 5.5V V_{CC}.

DC Electrical Characteristics for ACT

Symbol	Parameter	V_{CC} (V)	Conditions	$T_A = +25°C$	$T_A = -40°C$ to $+85°C$		Units
				Typ.	Guaranteed Limits		
V_{IH}	Minimum HIGH Level Input Voltage	4.5	$V_{OUT} = 0.1V$ or $V_{CC} - 0.1V$	1.5	2.0	2.0	V
		5.5		1.5	2.0	2.0	
V_{IL}	Maximum LOW Level Input Voltage	4.5	$V_{OUT} = 0.1V$ or $V_{CC} - 0.1V$	1.5	0.8	0.8	V
		5.5		1.5	0.8	0.8	
V_{OH}	Minimum HIGH Level Output Voltage	4.5	$I_{OUT} = -50\mu A$	4.49	4.4	4.4	V
		5.5		5.49	5.4	5.4	
		4.5	$V_{IN} = V_{IL}$ or V_{IH}; $I_{OH} = -24mA$		3.86	3.76	
		5.5	$I_{OH} = -24mA$[4]		4.86	4.76	
V_{OL}	Maximum LOW Level Output Voltage	4.5	$I_{OUT} = 50\mu A$	0.001	0.1	0.1	V
		5.5		0.001	0.1	0.1	
		4.5	$V_{IN} = V_{IL}$ or V_{IH}; $I_{OL} = 24mA$		0.36	0.44	
		5.5	$I_{OL} = 24mA$[4]		0.36	0.44	
I_{IN}	Maximum Input Leakage Current	5.5	$V_I = V_{CC}$, GND		±0.1	±1.0	µA
I_{OZ}	Maximum 3-STATE Current	5.5	$V_I = V_{IL}, V_{IH}$; $V_O = V_{CC}$, GND		±0.25	±2.5	µA
I_{CCT}	Maximum I_{CC}/Input	5.5	$V_I = V_{CC} - 2.1V$	0.6		1.5	mA
I_{OLD}	Minimum Dynamic Output Current[5]	5.5	$V_{OLD} = 1.65V$ Max.			75	mA
I_{OHD}		5.5	$V_{OHD} = 3.85V$ Min.			−75	mA
I_{CC}	Maximum Quiescent Supply Current	5.5	$V_{IN} = V_{CC}$ or GND		4.0	40.0	µA

Notes:

4. All outputs loaded; thresholds on input associated with output under test.

5. Maximum test duration 2.0ms, one output loaded at a time.

AC Electrical Characteristics for AC

Symbol	Parameter	V_{CC} (V)[6]	T_A = +25°C, C_L = 50pF			T_A = –40°C to +85°C, C_L = 50pF		Units
			Min.	Typ.	Max.	Min	Max	
t_{PLH}	Propagation Delay, S_n to Z_n	3.3	2.0	8.5	15.5	2.0	17.5	ns
		5.0	2.0	6.5	11.0	1.5	12.5	
t_{PHL}	Propagation Delay, S_n to Z_n	3.3	2.5	9.5	15.0	2.0	18.0	ns
		5.0	2.0	7.0	11.5	1.5	13.0	
t_{PLH}	Propagation Delay, I_n to Z_n	3.3	1.5	7.0	14.5	1.5	17.0	ns
		5.0	1.5	5.5	10.0	1.5	11.5	
t_{PHL}	Propagation Delay, I_n to Z_n	3.3	2.0	7.5	13.0	1.5	15.0	ns
		5.0	1.5	5.5	9.5	1.5	11.0	
t_{PZH}	Output Enable Time	3.3	1.5	4.5	8.0	1.0	8.5	ns
		5.0	1.5	3.5	6.0	1.0	6.5	
t_{PZL}	Output Enable Time	3.3	1.5	5.0	8.0	1.0	9.0	ns
		5.0	1.5	3.5	6.0	1.0	7.0	
t_{PHZ}	Output Disable Time	3.3	2.0	5.5	9.5	1.5	10.0	ns
		5.0	2.0	5.0	8.0	1.5	8.5	
t_{PLZ}	Output Disable Time	3.3	1.5	5.0	8.0	1.0	9.0	ns
		5.0	1.5	4.0	7.0	1.0	7.5	

Note:
6. Voltage range 3.3 is 3.3V ± 0.3V. Voltage range 5.0 is 5.0V ± 0.5V.

AC Electrical Characteristics for ACT

Symbol	Parameter	V_{CC} (V)[7]	T_A = +25°C, C_L = 50pF			T_A = –40°C to +85°C, C_L = 50pF		Units
			Min.	Typ.	Max.	Min.	Max.	
t_{PLH}	Propagation Delay, S_n to Z_n	5.0	2.0	7.0	11.5	2.0	13.0	ns
t_{PHL}	Propagation Delay, S_n to Z_n	5.0	3.0	7.5	13.0	2.5	14.5	ns
t_{PLH}	Propagation Delay, I_n to Z_n	5.0	2.5	5.5	10.0	2.0	11.0	ns
t_{PHL}	Propagation Delay, I_n to Z_n	5.0	3.5	6.5	11.0	3.0	12.5	ns
t_{PZH}	Output Enable Time	5.0	2.0	4.5	7.5	1.5	8.5	ns
t_{PZL}	Output Enable Time	5.0	2.0	5.0	8.0	1.5	9.0	ns
t_{PHZ}	Output Disable Time	5.0	3.0	6.0	9.5	2.5	10.0	ns
t_{PLZ}	Output Disable Time	5.0	2.5	4.5	7.5	2.0	8.5	ns

Note:
7. Voltage range 5.0 is 5.0V ± 0.5V.

Capacitance

Symbol	Parameter	Conditions	Typ.	Units
C_{IN}	Input Capacitance	V_{CC} = OPEN	4.5	pF
C_{PD}	Power Dissipation Capacitance	V_{CC} = 5.0V	50.0	pF

Physical Dimensions

Dimensions are in millimeters unless otherwise noted.

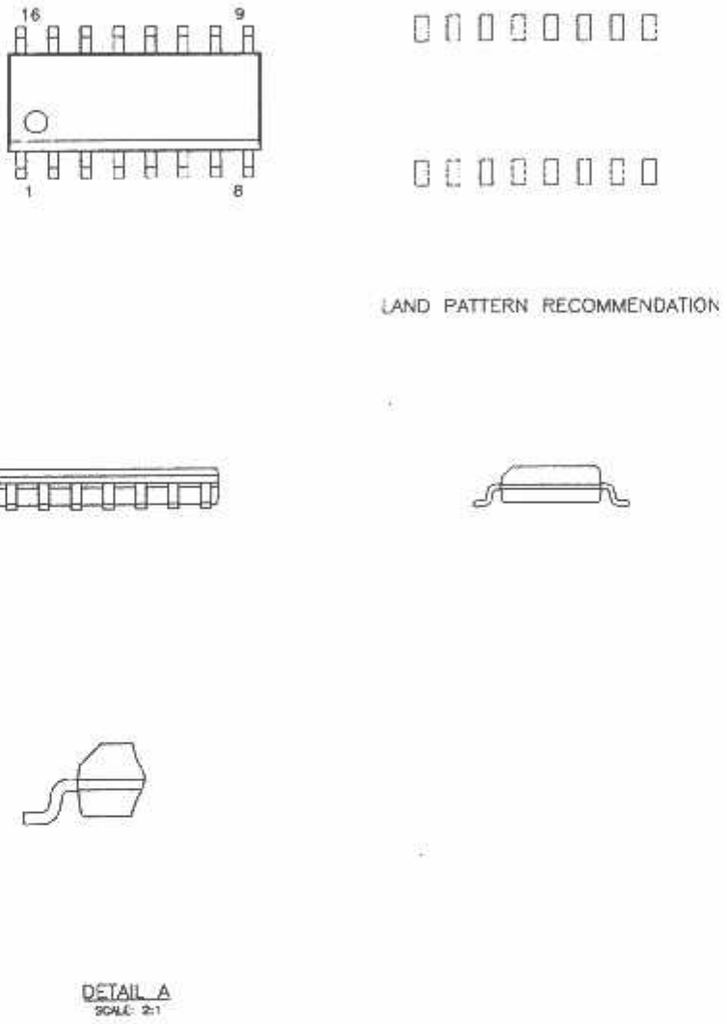
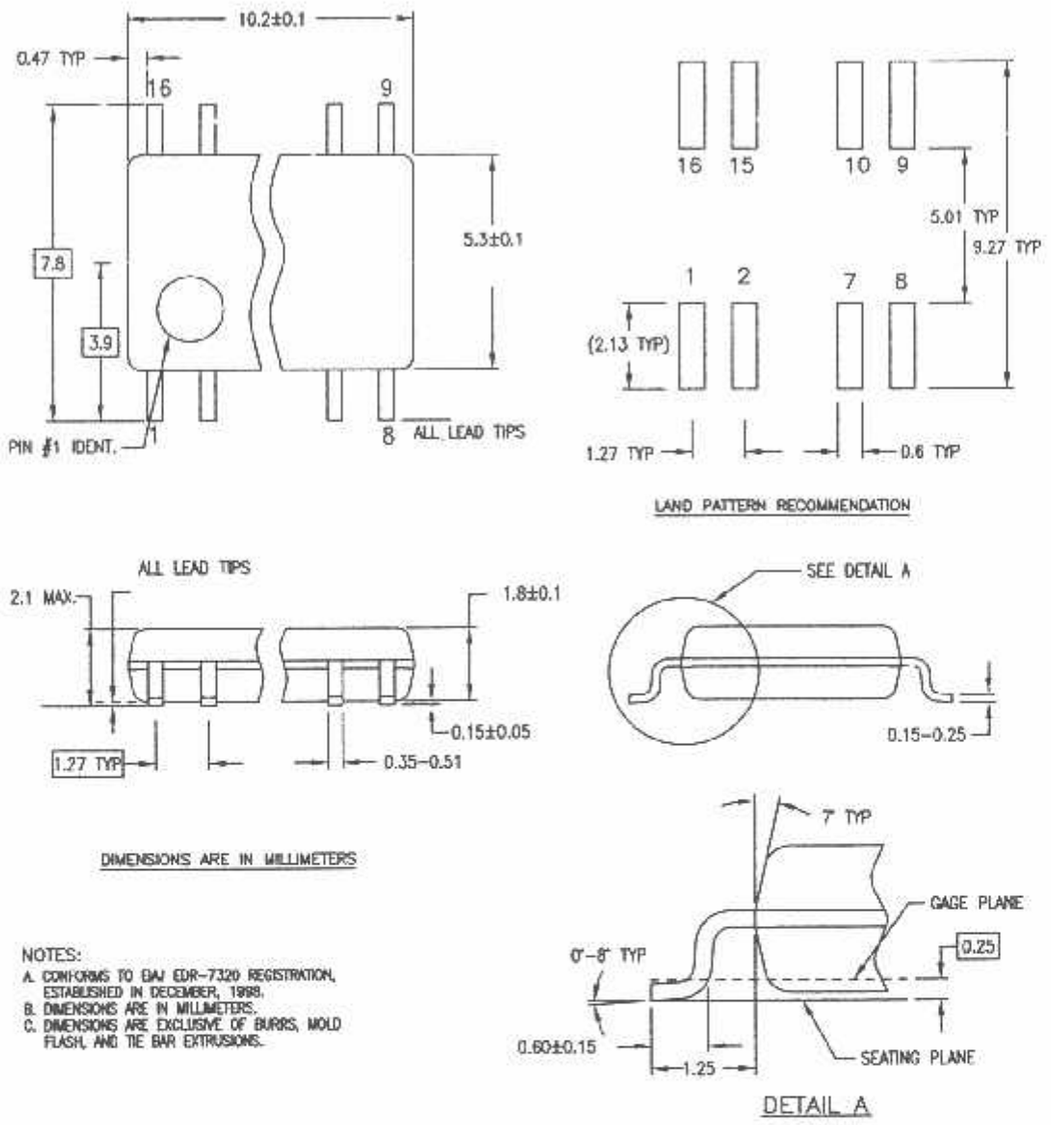


Figure 2. 16-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-012, 0.150" Narrow
Package Number M16A

Physical Dimensions (Continued)

Dimensions are in millimeters unless otherwise noted.



NOTES:

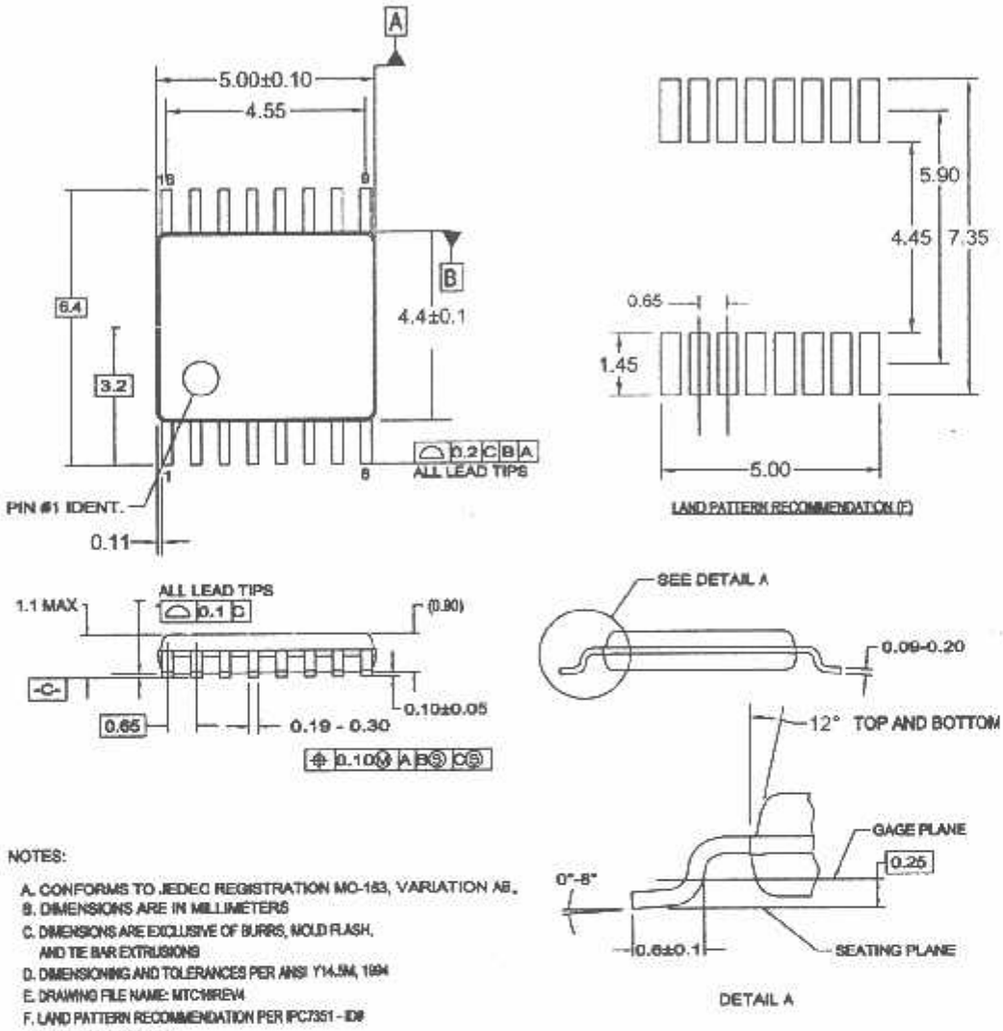
A. CONFORMS TO EIAJ EDR-7320 REGISTRATION, ESTABLISHED IN DECEMBER, 1998.
B. DIMENSIONS ARE IN MILLIMETERS.
C. DIMENSIONS ARE EXCLUSIVE OF BURRS, MOLD FLASH, AND TIE BAR EXTRUSIONS.

M16DREVC

Figure 3. 16-Lead Small Outline Package (SOP), EIAJ TYPE II, 5.3mm Wide
Package Number M16D

Physical Dimensions (Continued)

Dimensions are in millimeters unless otherwise noted.



NOTES:

A. CONFORMS TO JEDEC REGISTRATION MO-153, VARIATION AB.
B. DIMENSIONS ARE IN MILLIMETERS
C. DIMENSIONS ARE EXCLUSIVE OF BURRS, MOLD FLASH, AND TIE BAR EXTRUSIONS
D. DIMENSIONING AND TOLERANCES PER ANSI Y14.5M, 1994
E. DRAWING FILE NAME: MTC16REV4
F. LAND PATTERN RECOMMENDATION PER IPC7351 - ID# TSOP65P640X110-16N

MTC16rev4

Figure 4. 16-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 4.4mm Wide
Package Number MTC16

Physical Dimensions (Continued)

Dimensions are in inches (millimeters) unless otherwise noted.

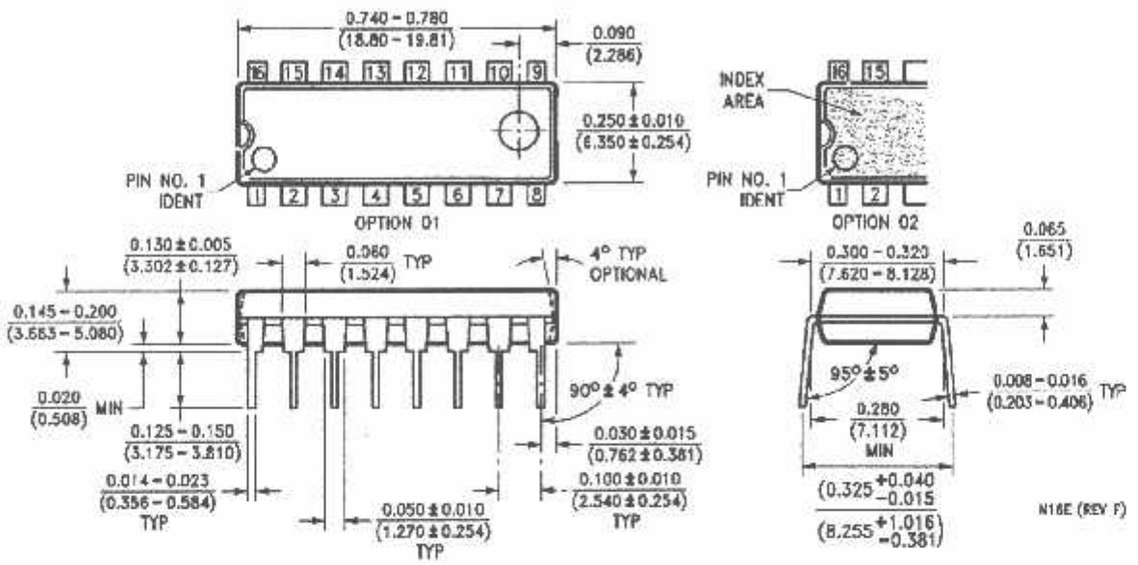


Figure 5. 16-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300" Wide
Package Number N16E

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Rev. I24

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