INSTITUT TEKNOLOGI NASIONAL MALANG
FAKULTAS TEKNOLOGI INDUSTRI
JURUSAN TEKNIK ELEKTRO S-1
KONSENTRASI TEKNIK ELEKTRONIKA

PERANCANGAN DAN PEMBUATAN SISTEM RUANGAN MULTIFUNGSI BERBASIS MIKROKONTROLLER AT89S51

SKRIPSI

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SEPTEMBER 2009

D/A conversion

e third byte sent to a PCF8591 device is stored in the
C data register and is converted to the corresponding
alog voltage using the on-chip D/A converter. This D/A
nverter consists of a resistor divider chain connected to
external reference voltage with 256 taps and selection
itches. The tap-decoder switches one of these taps to
DAC output line (see Fig.6).

e analog output voltage is buffered by an auto-zeroed
ty gain amplifier. This buffer amplifier may be switched
or off by setting the analog output enable flag of the control register. In the active state the output voltage is held until a further data byte is sent.

The on-chip D/A converter is also used for successive approximation A/D conversion. In order to release the DAC for an A/D conversion cycle the unity gain amplifier is equipped with a track and hold circuit. This circuit holds the output voltage while executing the A/D conversion.

The output voltage supplied to the analog output AOUT is given by the formula shown in Fig.7. The waveforms of a D/A conversion sequence are shown in Fig.8.

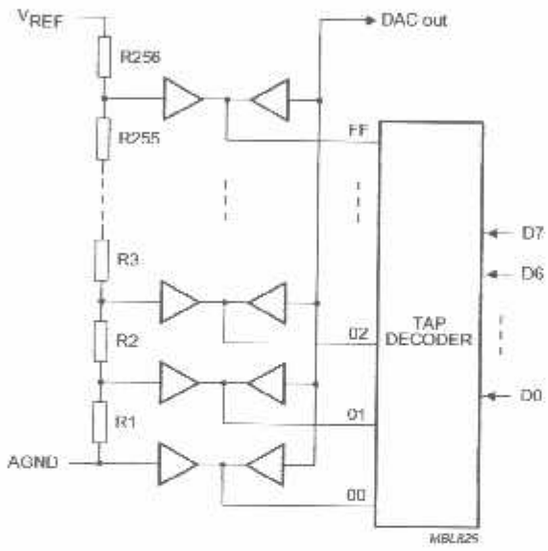


Fig.6 DAC resistor divider chain.

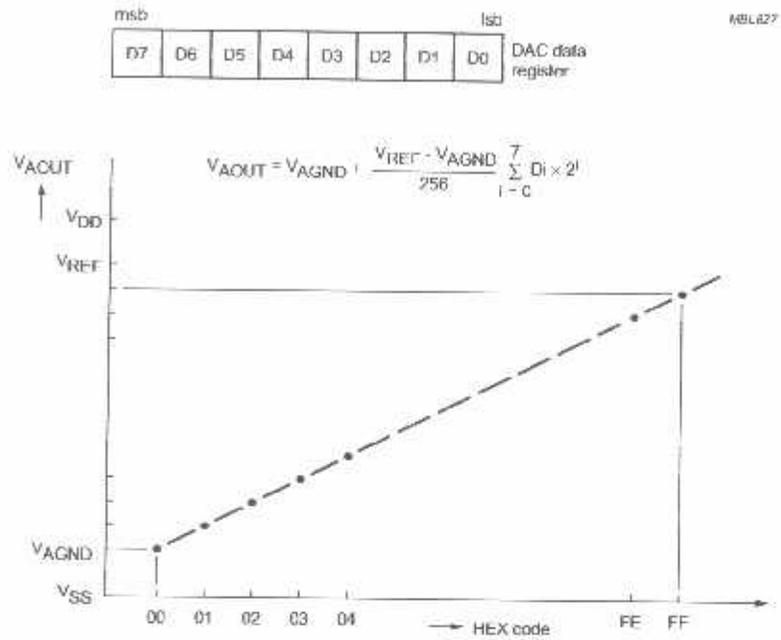


Fig.7 DAC data and DC conversion characteristics.

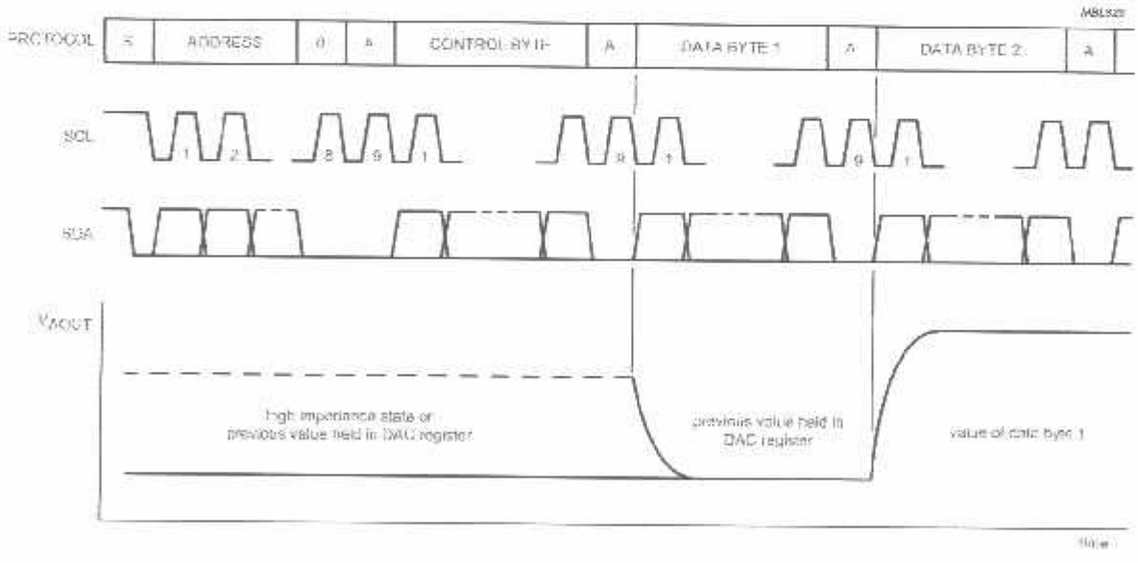


Fig.8 D/A conversion sequence.

A/D conversion

3 A/D converter makes use of the successive oroximation conversion technique. The on-chip D/A iverter and a high-gain comparator are used nporarily during an A/D conversion cycle.

A/D conversion cycle is always started after sending a id read mode address to a PCF8591 device. The A/D iversion cycle is triggered at the trailing edge of the nowledge clock pulse and is executed while nsmitting the result of the previous conversion (see .9).

ce a conversion cycle is triggered an input voltage nple of the selected channel is stored on the chip and is converted to the corresponding 8-bit binary code. Samples picked up from differential inputs are converted to an 8-bit twos complement code (see Figs 10 and 11).

The conversion result is stored in the ADC data register and awaits transmission. If the auto-increment flag is set the next channel is selected.

The first byte transmitted in a read cycle contains the conversion result code of the previous read cycle. After a Power-on reset condition the first byte read is a hexadecimal 80. The protocol of an I²C-bus read cycle is shown in Chapter 8, Figs 16 and 17.

The maximum A/D conversion rate is given by the actual speed of the I²C-bus.

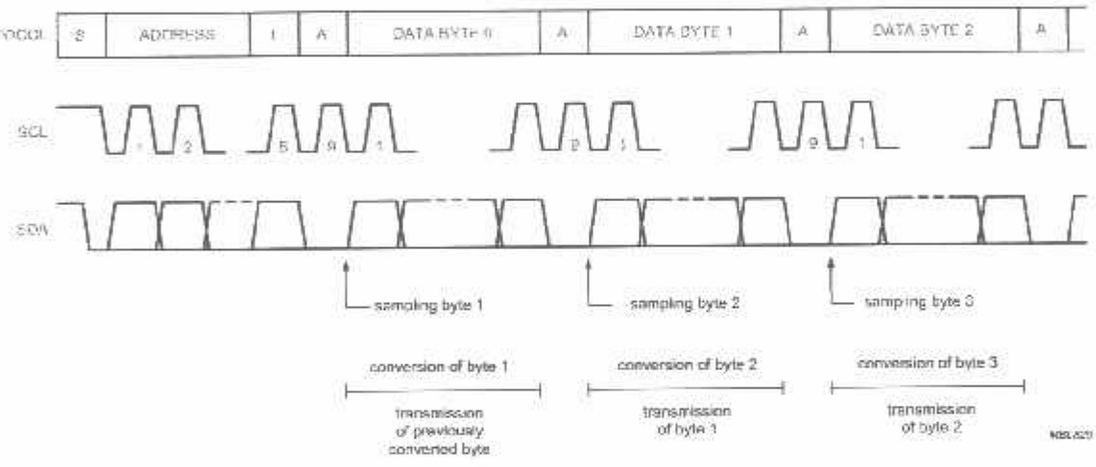


Fig.9 A/D conversion sequence.

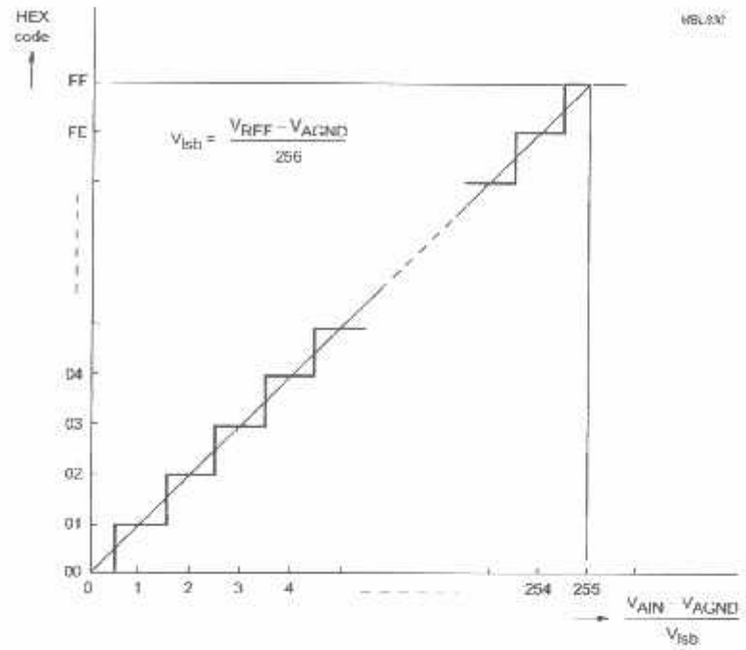


Fig.10 A/D conversion characteristics of single-ended inputs.

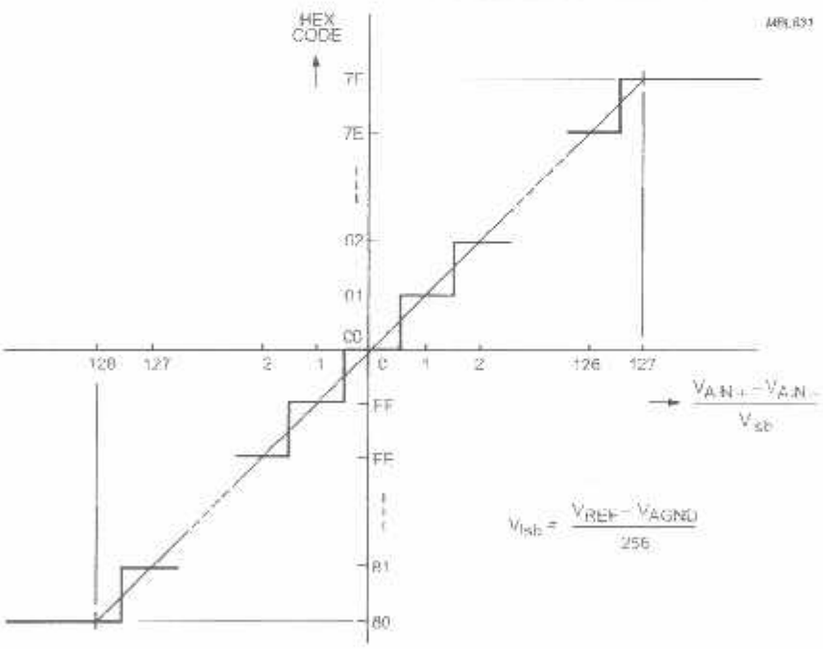


Fig.11 A/D conversion characteristics of differential inputs.

7.5 Reference voltage

For the D/A and A/D conversion either a stable external voltage reference or the supply voltage has to be applied to the resistor divider chain (pins V_{REF} and AGND). The AGND pin has to be connected to the system analog ground and may have a DC off-set with reference to V_{SS}.

A low frequency may be applied to the V_{REF} and AGND pins. This allows the use of the D/A converter as a one-quadrant multiplier; see Chapter 15 and Fig.7.

The A/D converter may also be used as a one or two quadrant analog divider. The analog input voltage is divided by the reference voltage. The result is converted to a binary code. In this application the user has to keep the reference voltage stable during the conversion cycle.

7.6 Oscillator

An on-chip oscillator generates the clock signal required for the A/D conversion cycle and for refreshing the auto-zeroed buffer amplifier. When using this oscillator the EXT pin has to be connected to V_{SS}. At the OSC pin the oscillator frequency is available.

If the EXT pin is connected to V_{DD} the oscillator output OSC is switched to a high-impedance state allowing the user to feed an external clock signal to OSC.

3 CHARACTERISTICS OF THE I²C-BUS

The I²C-bus is for bidirectional, two-line communication between different ICs or modules. The two lines are a serial data line (SDA) and a serial clock line (SCL). Both lines must be connected to a positive supply via a pull-up resistor. Data transfer may be initiated only when the bus is not busy.

3.1 Bit transfer

One data bit is transferred during each clock pulse. The data on the SDA line must remain stable during the HIGH period of the clock pulse as changes in the data line at this time will be interpreted as a control signal.

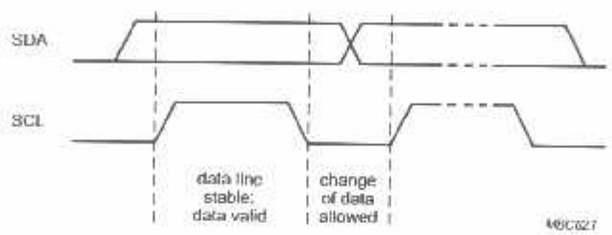


Fig.12 Bit transfer.

3.2 Start and stop conditions

Both data and clock lines remain HIGH when the bus is not busy. A HIGH-to-LOW transition of the data line, while the clock is HIGH, is defined as the start condition (S). A LOW-to-HIGH transition of the data line while the clock is HIGH, is defined as the stop condition (P).

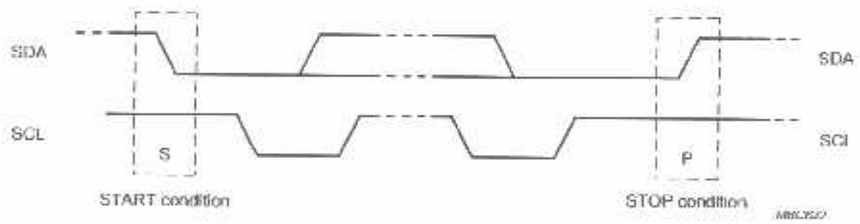


Fig.13 Definition of START and STOP condition.

3.3 System configuration

A device generating a message is a 'transmitter', a device receiving a message is the 'receiver'. The device that controls the message is the 'master' and the devices which are controlled by the master are the 'slaves'.

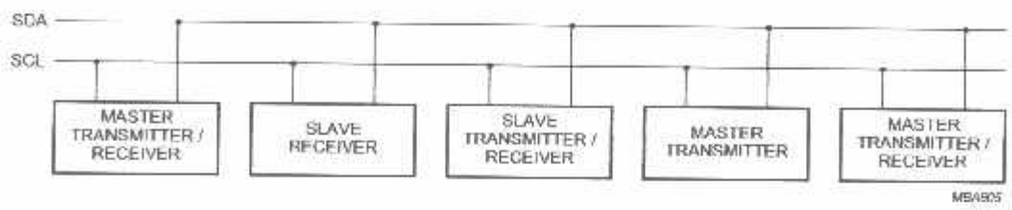


Fig.14 System configuration.

3.4 Acknowledge

The number of data bytes transferred between the start and stop conditions from transmitter to receiver is not limited. Each data byte of eight bits is followed by one acknowledge bit. The acknowledge bit is a HIGH level put on the bus by the transmitter whereas the master also generates an extra acknowledge related clock pulse. A slave receiver which is addressed must generate an acknowledge after the reception of each byte. Also a master must generate an acknowledge after the reception of each byte that has been clocked out of the slave transmitter. The device that acknowledges has to pull down the SDA line during the acknowledge clock pulse, so that the SDA line is stable LOW during the HIGH period of the acknowledge related clock pulse. A master receiver must signal an end of data to the transmitter by **not** generating an acknowledge on the last byte that has been clocked out of the slave. In this event the transmitter must leave the data line HIGH to enable the master to generate a stop condition.

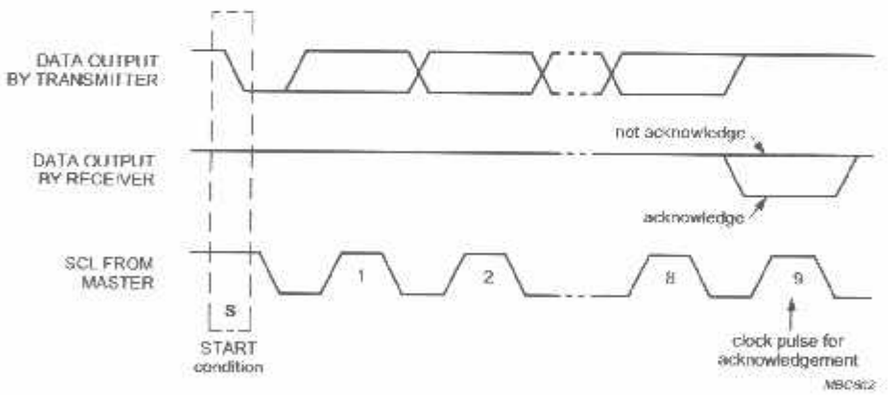


Fig.15 Acknowledgement on the I²C-bus.

8.5 I²C-bus protocol

After a start condition a valid hardware address has to be sent to a PCF8591 device. The read/write bit defines the direction of the following single or multiple byte data transfer. For the format and the timing of the start condition (S), the stop condition (P) and the acknowledge bit (A) refer to the I²C-bus characteristics. In the write mode a data transfer is terminated by sending either a stop condition or the start condition of the next data transfer.

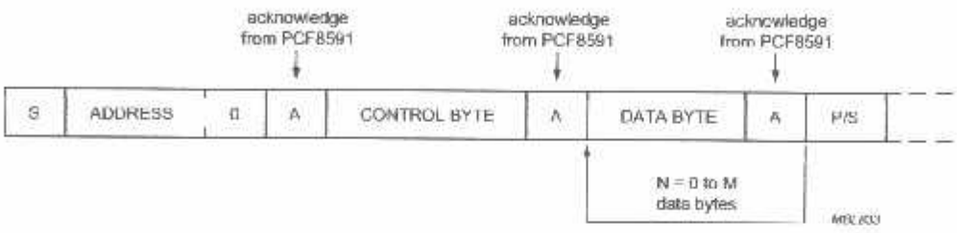


Fig.16 Bus protocol for write mode, D/A conversion.

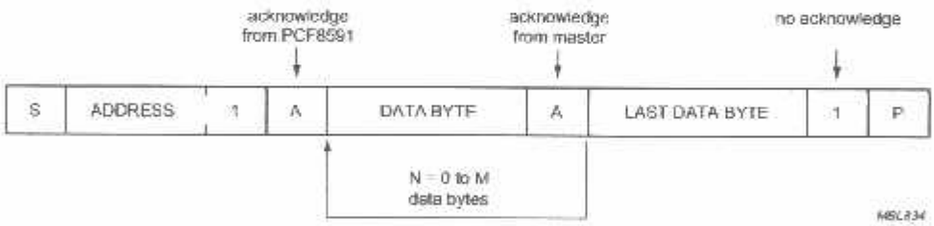


Fig.17 Bus protocol for read mode, A/D conversion.

9 LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 60134).

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
V_{DD}	supply voltage (pin 16)	−0.5	+8.0	V
V_I	input voltage (any input)	−0.5	V_{DD} + 0.5	V
I_I	DC input current	–	±10	mA
I_O	DC output current	–	±20	mA
I_{DD}; I_{SS}	V_{DD} or V_{SS} current		±50	mA
P_{tot}	total power dissipation per package	–	300	mW
P_O	power dissipation per output	–	100	mW
T_{amb}	operating ambient temperature	−40	+85	°C
T_{stg}	storage temperature	−65	+150	°C

10 HANDLING

Inputs and outputs are protected against electrostatic discharge in normal handling. However it is good practice to take normal precautions appropriate to handling MOS devices (see *"Handling MOS devices"*).

11 DC CHARACTERISTICS

V_{DD} = 2.5 V to 6 V; V_{SS} = 0 V; T_{amb} = −40 °C to −85 °C unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Supply						
V_{DD}	supply voltage (operating)		2.5	–	6.0	V
I_{DD}	supply current					
	standby	$V_I = V_{SS}$ or V_{DD}; no load	–	1	15	µA
	operating, AOUT off	f_{SCL} = 100 kHz	–	125	250	µA
	operating, AOUT active	f_{SCL} = 100 kHz	–	0.45	1.0	mA
V_{POR}	Power-on reset level	note 1	0.8		2.0	V
Digital inputs/output: SCL, SDA, A0, A1, A2						
V_{IL}	LOW level input voltage		0	–	$0.3 \times V_{DD}$	V
V_{IH}	HIGH level input voltage		$0.7 \times V_{DD}$	–	V_{DD}	V
I_L	leakage current					
	A0, A1, A2	$V_I = V_{SS}$ to V_{DD}	−250	–	+250	nA
	SCL, SDA	$V_I = V_{SS}$ to V_{DD}	−1	–	+1	µA
C_i	input capacitance		–	–	5	pF
I_{OL}	LOW level SDA output current	V_{OL} = 0.4 V	3.0	–	–	mA
Reference voltage inputs						
V_{REF}	reference voltage	$V_{REF} > V_{AGND}$; note 2	V_{SS} + 1.6	–	V_{DD}	V
V_{AGND}	analog ground voltage	$V_{REF} > V_{AGND}$; note 2	V_{SS}	–	V_{DD} − 0.8	V
I_{LI}	input leakage current		−250	–	+250	nA
R_{REF}	input resistance	pins V_{REF} and AGND	–	100	–	kΩ
Oscillator: OSC, EXT						
I_{LI}	input leakage current		–	–	250	nA
f_{OSC}	oscillator frequency		0.75	–	1.25	MHz

Notes

1. The power on reset circuit resets the I²C-bus logic when V_{DD} is less than V_{POR}.
2. A further extension of the range is possible, if the following conditions are fulfilled:

$$\frac{V_{REF} + V_{AGND}}{2} \geq 0.8\,V, V_{DD} - \frac{V_{REF} + V_{AGND}}{2} \geq 0.4\,V$$

I2 D/A CHARACTERISTICS

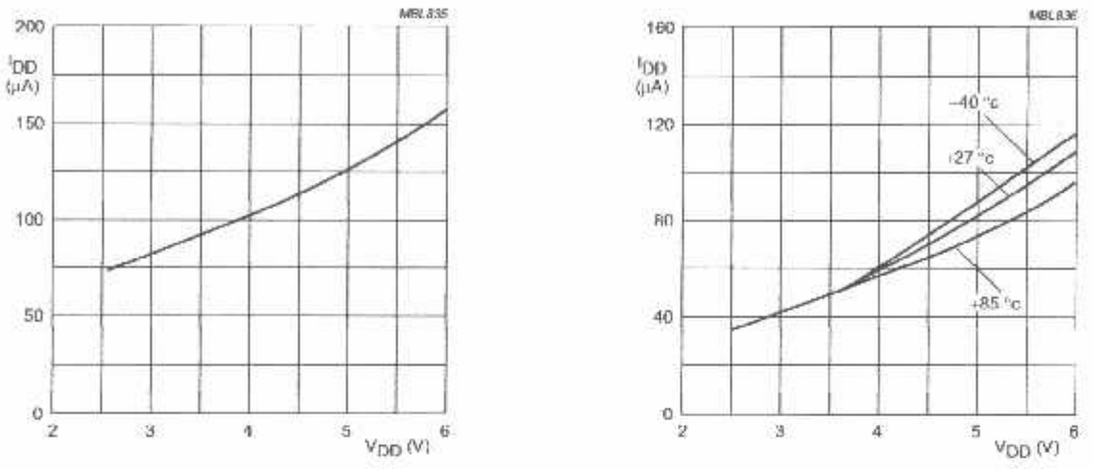
V_{DD} = 5.0 V; V_{SS} = 0 V; V_{REF} = 5.0 V; V_{AGND} = 0 V; R_L = 10 kΩ; C_L = 100 pF; T_{amb} = −40 °C to +85 °C unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Analog output						
V_{OA}	output voltage	no resistive load	V_{SS}	–	V_{DD}	V
		R_L = 10 kΩ	V_{SS}	–	0.9 × V_{DD}	V
I_{LO}	output leakage current	AOUT disabled	–	–	250	nA
Accuracy						
OS_e	offset error	T_{amb} = 25 °C		–	50	mV
L_e	linearity error		–	–	±1.5	LSB
G_e	gain error	no resistive load	–	–	1	%
t_{DAC}	settling time	to ½ LSB full scale step	–	–	90	µs
f_{DAC}	conversion rate		–	–	11.1	kHz
SNRR	supply noise rejection ratio	f = 100 Hz; V_{DDN} = 0.1 × V_{PP}	–	40	–	dB

3 A/D CHARACTERISTICS

V_{DD} = 5.0 V; V_{SS} = 0 V; V_{REF} = 5.0 V; V_{AGND} = 0 V; R_S = 10 kΩ; T_{amb} = −40 °C to +85 °C unless otherwise specified.

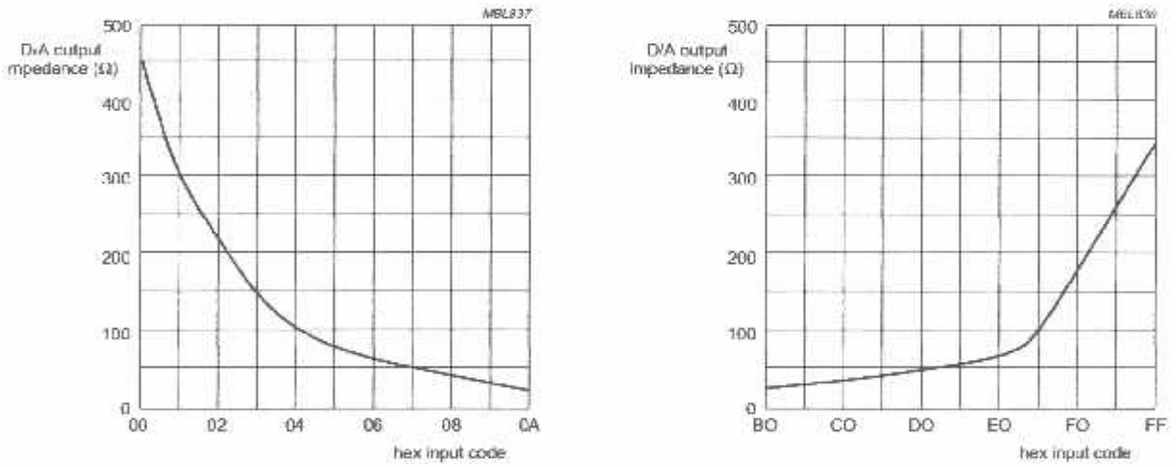
SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Analog inputs						
V_{IA}	analog input voltage		V_{SS}	–	V_{DD}	V
I_{LIA}	analog input leakage current		–	–	100	nA
C_{IA}	analog input capacitance		–	10	–	pF
C_{ID}	differential input capacitance		–	10	–	pF
V_{IS}	single-ended voltage	measuring range	V_{AGND}	–	V_{REF}	V
V_{ID}	differential voltage	measuring range; $V_{FS} = V_{REF} - V_{AGND}$	$\frac{-V_{FS}}{2}$	–	$\frac{+V_{FS}}{2}$	V
Accuracy						
OS_e	offset error	T_{amb} = 25 °C		–	20	mV
L_e	linearity error		–	–	±1.5	LSB
G_e	gain error		–	–	1	%
GS_e	small-signal gain error	ΔV_i = 16 LSB	–	–	5	%
CMRR	common-mode rejection ratio		–	60		dB
SNRR	supply noise rejection ratio	f = 100 Hz; V_{DDN} = 0.1 × V_{PP}	–	40	–	dB
t_{ACC}	conversion time		–	–	90	µs
f_{ACC}	sampling/conversion rate		–	–	11.1	kHz



a. Internal oscillator; T_{amb} = +27° C.

b. External oscillator.

Fig.18 Operating supply current as a function of supply voltage (analog output disabled).



a. Output impedance near negative power rail; T_{amb} = +27 °C.

b. Output impedance near positive power rail; T_{amb} = +27 °C.

The x-axis represents the hex input-code equivalent of the output voltage.

Fig.19 Output impedance of analog output buffer (near power rails).

14 AC CHARACTERISTICS

All timing values are valid within the operating supply voltage and ambient temperature range and reference to V_{IL} and V_{IH} with an input voltage swing of V_{SS} to V_{DD}.

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
I²C-bus timing (see Fig.20; note 1)					
f_{SCL}	SCL clock frequency	–	–	100	kHz
t_{SP}	tolerable spike width on bus	–	–	100	ns
t_{BUF}	bus free time	4.7	–	–	µs
$t_{SU;STA}$	START condition set-up time	4.7	–	–	µs
$t_{HD;STA}$	START condition hold time	4.0	–	–	µs
t_{LOW}	SCL LOW time	4.7	–	–	µs
t_{HIGH}	SCL HIGH time	4.0	–	–	µs
t_r	SCL and SDA rise time	–	–	1.0	µs
t_f	SCL and SDA fall time	–	–	0.3	µs
$t_{SU;DAT}$	data set-up time	250	–	–	ns
$t_{HD;DAT}$	data hold time	0	–	–	ns
$t_{VD;DAT}$	SCL LOW-to-data out valid	–	–	3.4	µs
$t_{SU;STO}$	STOP condition set up time	4.0	–	–	µs

Note

1. A detailed description of the I²C-bus specification, with applications, is given in brochure *"The I²C-bus and how to use it"*. This brochure may be ordered using the code 9398 393 40011.

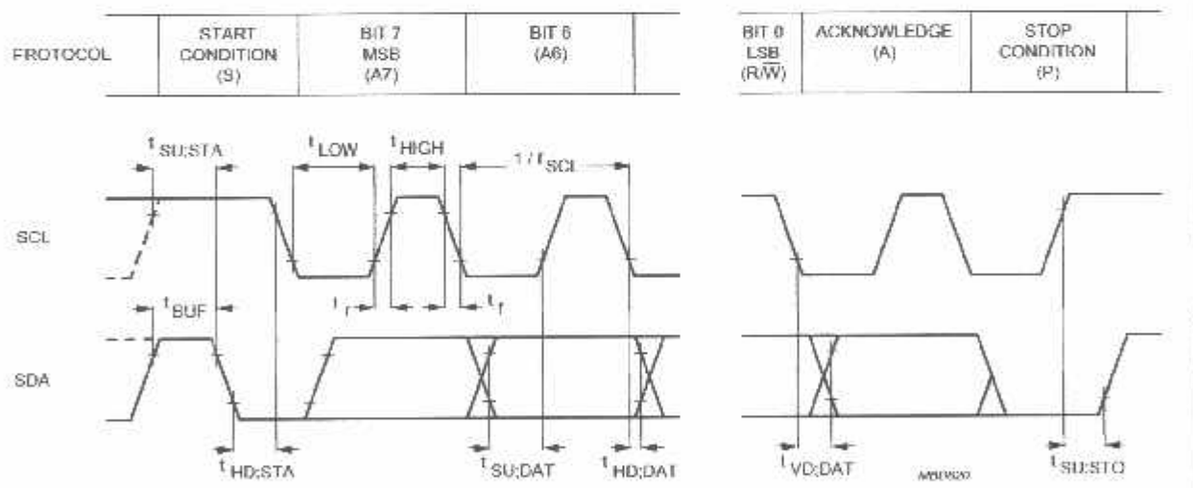


Fig.20 I²C-bus timing diagram; rise and fall times refer to V_{IL} and V_{IH}.

15 APPLICATION INFORMATION

Inputs must be connected to V_{SS} or V_{DD} when not in use. Analog inputs may also be connected to AGND or V_{REF}.

In order to prevent excessive ground and supply noise and to minimize cross-talk of the digital to analog signal paths the user has to design the printed-circuit board layout very carefully. Supply lines common to a PCF8591 device and noisy digital circuits and ground loops should be avoided. Decoupling capacitors (>10 μF) are recommended for power supply and reference voltage inputs.

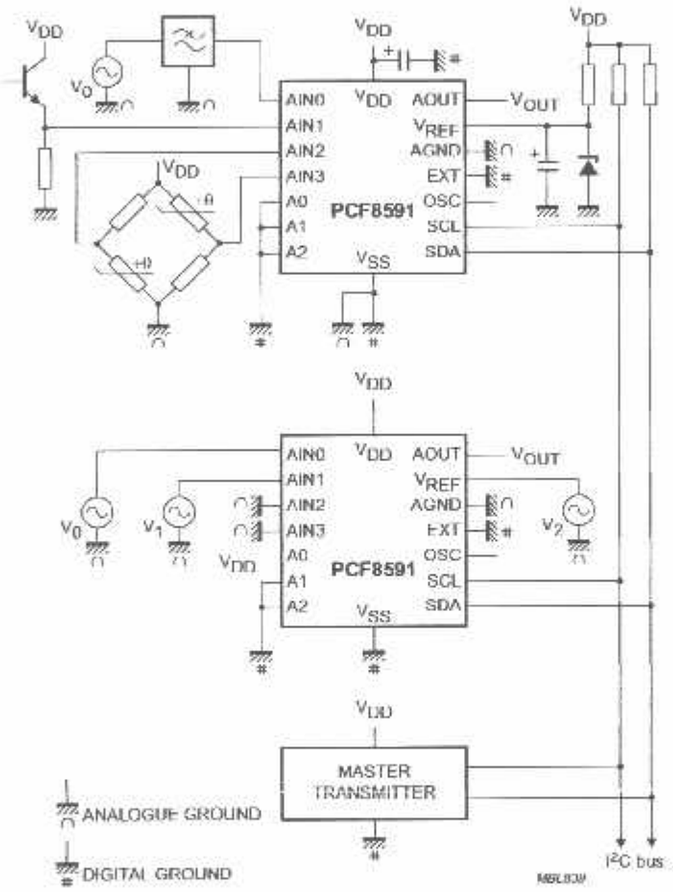
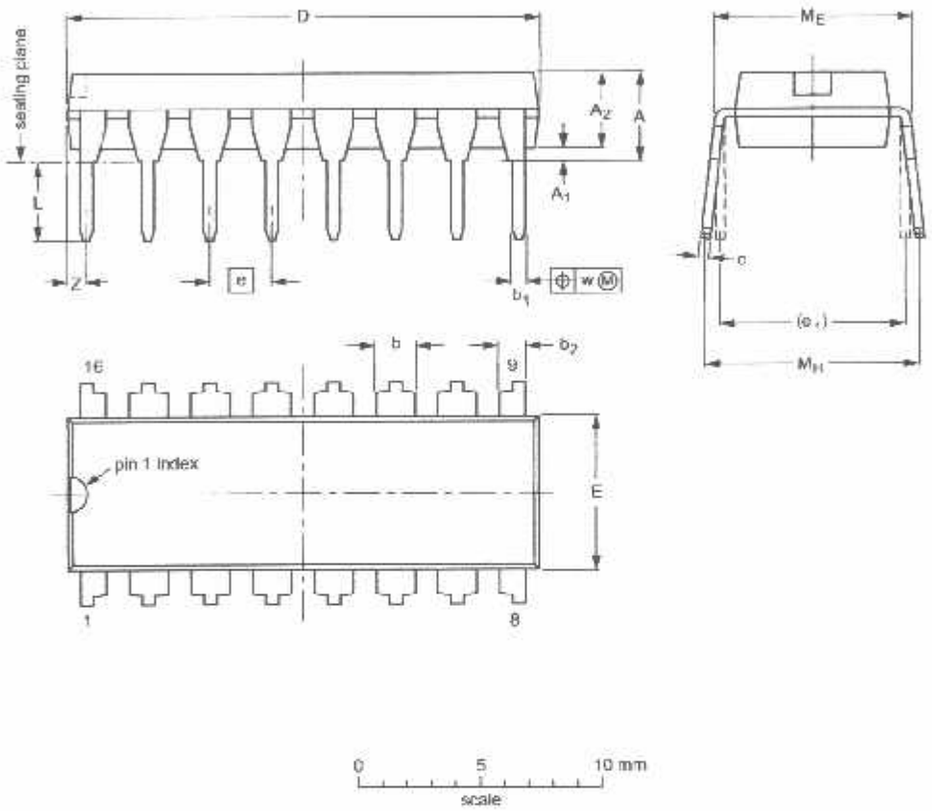


Fig.21 Application diagram.

16 PACKAGE OUTLINES

DIP16: plastic dual in-line package; 16 leads (300 mil) **SOT38-4**



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

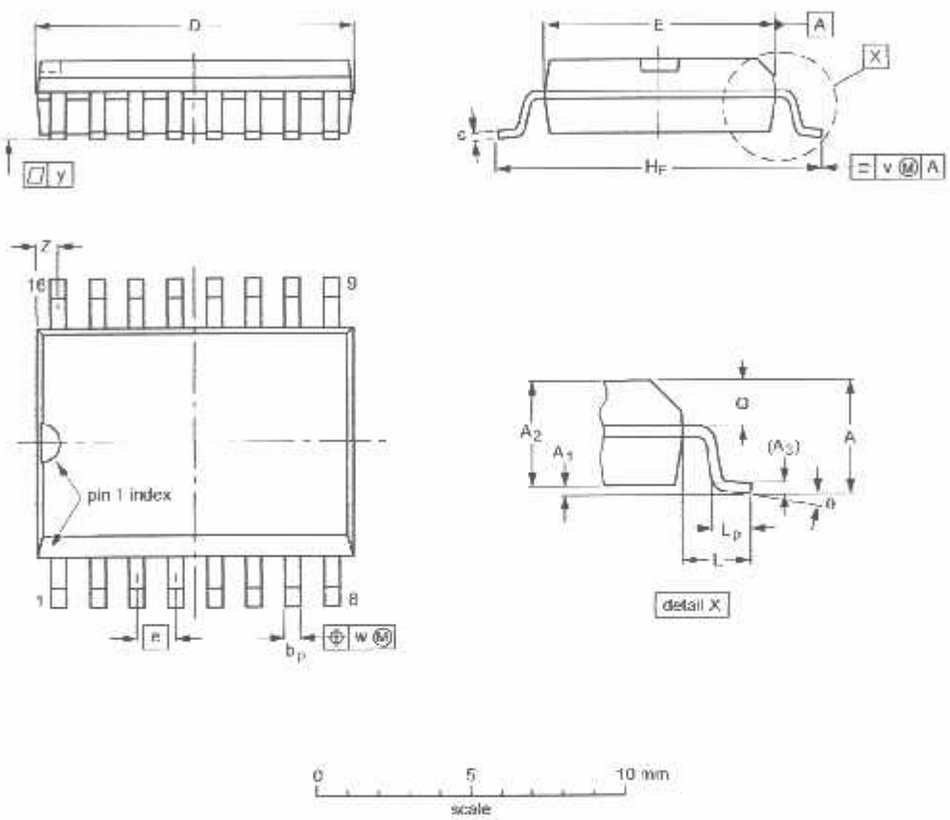
UNIT	A max.	A_1 min.	A_2 max.	b	b_1	b_2	c	$D^{(1)}$	$E^{(1)}$	e	e_1	L	M_E	M_H	w	$Z^{(1)}$ max.
mm	4.2	0.51	3.2	1.73 1.30	0.53 0.38	1.25 0.85	0.36 0.23	19.50 18.55	6.48 6.20	2.54	7.62	3.60 3.05	8.25 7.80	10.0 8.3	0.254	0.76
inches	0.17	0.020	0.13	0.068 0.051	0.021 0.015	0.049 0.033	0.014 0.009	0.77 0.73	0.26 0.24	0.10	0.30	0.14 0.12	0.32 0.31	0.39 0.33	0.01	0.030

Note

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT38-4						~~92-11-17~~ 95-01-14

SO16: plastic small outline package; 16 leads; body width 7.5 mm **SOT162-1**



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(1)}$	e	H_E	L	L_p	Q	v	w	y	$Z^{(1)}$	θ
mm	2.65	0.30 0.10	2.45 2.25	0.25	0.49 0.36	0.32 0.23	10.5 10.1	7.6 7.4	1.27	10.65 10.00	1.4	1.1 0.4	1.1 1.0	0.25	0.25	0.1	0.9 0.4	8° 0°
inches	0.10	0.012 0.004	0.096 0.089	0.01	0.019 0.014	0.013 0.009	0.41 0.40	0.30 0.29	0.050	0.419 0.394	0.055	0.043 0.016	0.043 0.039	0.01	0.01	0.004	0.035 0.016	

Note

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT162-1	075E03	MS-013				-97-06-22 99-12-27

17 SOLDERING

17.1 Introduction to soldering through-hole mount packages

This text gives a brief insight to wave, dip and manual soldering. A more in-depth account of soldering ICs can be found in our *"Data Handbook IC26; Integrated Circuit Packages"* (document order number 9398 652 90011).

Wave soldering is the preferred method for mounting of through-hole mount IC packages on a printed-circuit board.

17.2 Soldering by dipping or by solder wave

The maximum permissible temperature of the solder is 260 °C; solder at this temperature must not be in contact with the joints for more than 5 seconds.

The total contact time of successive solder waves must not exceed 5 seconds.

The device may be mounted up to the seating plane, but the temperature of the plastic body must not exceed the specified maximum storage temperature ($T_{stg(max)}$). If the printed-circuit board has been pre-heated, forced cooling may be necessary immediately after soldering to keep the temperature within the permissible limit.

17.3 Manual soldering

Apply the soldering iron (24 V or less) to the lead(s) of the package, either below the seating plane or not more than 2 mm above it. If the temperature of the soldering iron bit is less than 300 °C it may remain in contact for up to 10 seconds. If the bit temperature is between 300 and 400 °C, contact may be up to 5 seconds.

17.4 Suitability of through-hole mount IC packages for dipping and wave soldering methods

PACKAGE	SOLDERING METHOD	
	DIPPING	WAVE
DBS, DIP, HDIP, SDIP, SIL	suitable	suitable[1]

Note

1. For SDIP packages, the longitudinal axis must be parallel to the transport direction of the printed-circuit board.

18 DATA SHEET STATUS

LEVEL	DATA SHEET STATUS[1]	PRODUCT STATUS[2][3]	DEFINITION
I	Objective data	Development	This data sheet contains data from the objective specification for product development. Philips Semiconductors reserves the right to change the specification in any manner without notice.
II	Preliminary data	Qualification	This data sheet contains data from the preliminary specification. Supplementary data will be published at a later date. Philips Semiconductors reserves the right to change the specification without notice, in order to improve the design and supply the best possible product.
III	Product data	Production	This data sheet contains data from the product specification. Philips Semiconductors reserves the right to make changes at any time in order to improve the design, manufacturing and supply. Relevant changes will be communicated via a Customer Product/Process Change Notification (CPCN).

Notes

1. Please consult the most recently issued data sheet before initiating or completing a design.
2. The product status of the device(s) described in this data sheet may have changed since this data sheet was published. The latest information is available on the Internet at URL http://www.semiconductors.philips.com.
3. For data sheets describing multiple type numbers, the highest-level product status determines the data sheet status.

19 DEFINITIONS

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Limiting values definition — Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 60134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.

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21 PURCHASE OF PHILIPS I²C COMPONENTS

Purchase of Philips I²C components conveys a license under the Philips' I²C patent to use the components in the I²C system provided the system conforms to the I²C specification defined by Philips. This specification can be ordered using the code 9398 393 40011.

NOTES

NOTES

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Printed in The Netherlands 403512/06/pp28 Date of release: 2003 Jan 27 Document order number: 9397 750 10464

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DATA SHEET

PCF8574
Remote 8-bit I/O expander for I²C-bus

Product specification
Supersedes data of 2002 Jul 29

2002 Nov 22

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PURCHASE OF PHILIPS I²C COMPONENTS

Remote 8-bit I/O expander for I²C-bus PCF8574

FEATURES

Operating supply voltage 2.5 to 6 V

Low standby current consumption of 10 µA maximum

I²C-bus to parallel port expander

Open-drain interrupt output

8-bit remote I/O port for the I²C-bus

Compatible with most microcontrollers

Latched outputs with high current drive capability for directly driving LEDs

Address by 3 hardware address pins for use of up to 8 devices (up to 16 with PCF8574A)

DIP16, or space-saving SO16 or SSOP20 packages.

GENERAL DESCRIPTION

ıe PCF8574 is a silicon CMOS circuit. It provides general ırpose remote I/O expansion for most microcontroller milies via the two-line bidirectional bus (I²C-bus).

The device consists of an 8-bit quasi-bidirectional port and an I²C-bus interface. The PCF8574 has a low current consumption and includes latched outputs with high current drive capability for directly driving LEDs. It also possesses an interrupt line ($\overline{INT}$) which can be connected to the interrupt logic of the microcontroller. By sending an interrupt signal on this line, the remote I/O can inform the microcontroller if there is incoming data on its ports without having to communicate via the I²C-bus. This means that the PCF8574 can remain a simple slave device.

The PCF8574 and PCF8574A versions differ only in their slave address as shown in Fig.10.

ORDERING INFORMATION

YPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
CF8574P; CF8574AP	DIP16	plastic dual in-line package; 16 leads (300 mil)	SOT38-4
'CF8574T; 'CF8574AT	SO16	plastic small outline package; 16 leads; body width 7.5 mm	SOT162-1
CF8574TS; CF8574ATS	SSOP20	plastic shrink small outline package; 20 leads; body width 4.4 mm	SOT266-1

BLOCK DIAGRAM

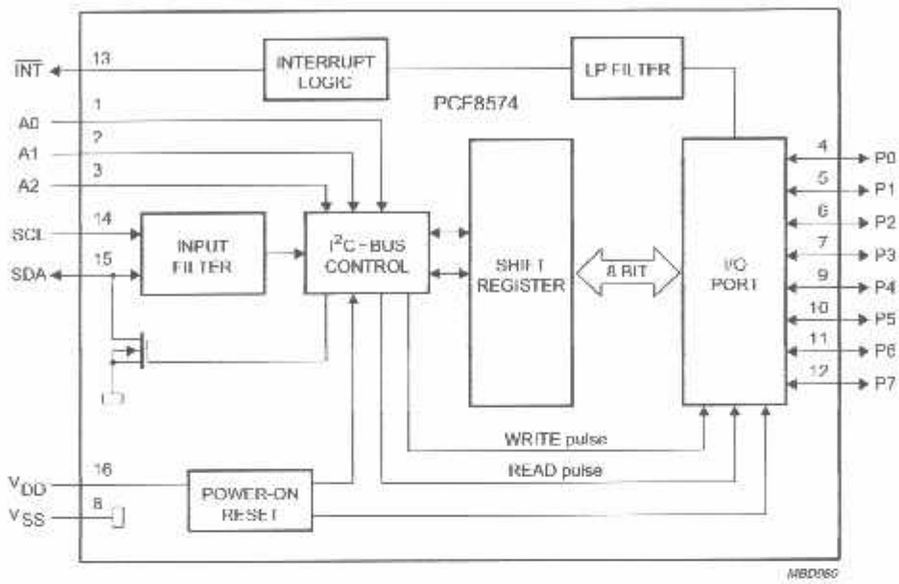


Fig.1 Block diagram (pin numbers apply to DIP16 and SO16 packages).

PINNING

1 DIP16 and SO16 packages

SYMBOL	PIN	DESCRIPTION
0	1	address input 0
1	2	address input 1
2	3	address input 2
0	4	quasi-bidirectional I/O 0
1	5	quasi-bidirectional I/O 1
2	6	quasi-bidirectional I/O 2
3	7	quasi-bidirectional I/O 3
SS	8	supply ground
4	9	quasi-bidirectional I/O 4
5	10	quasi-bidirectional I/O 5
6	11	quasi-bidirectional I/O 6
7	12	quasi-bidirectional I/O 7
$\overline{NT}$	13	interrupt output (active LOW)
CL	14	serial clock line
DA	15	serial data line
DD	16	supply voltage

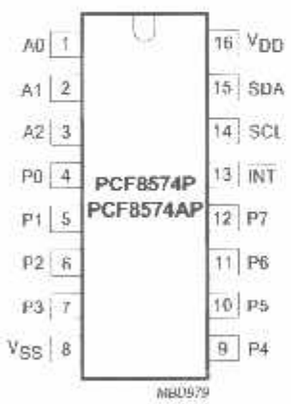


Fig.2 Pin configuration (DIP16).

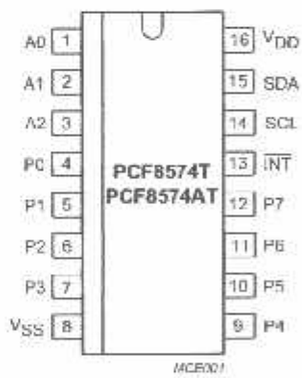


Fig.3 Pin configuration (SO16).

.2 SSOP20 package

SYMBOL	PIN	DESCRIPTION
$\overline{INT}$	1	interrupt output (active LOW)
SCL	2	serial clock line
n.c.	3	not connected
SDA	4	serial data line
V_{DD}	5	supply voltage
A0	6	address input 0
A1	7	address input 1
n.c.	8	not connected
A2	9	address input 2
P0	10	quasi-bidirectional I/O 0
P1	11	quasi-bidirectional I/O 1
P2	12	quasi-bidirectional I/O 2
n.c.	13	not connected
P3	14	quasi-bidirectional I/O 3
V_{SS}	15	supply ground
P4	16	quasi-bidirectional I/O 4
P5	17	quasi-bidirectional I/O 5
n.c.	18	not connected
P6	19	quasi-bidirectional I/O 6
P7	20	quasi-bidirectional I/O 7

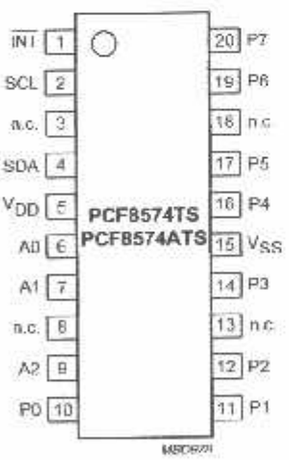


Fig.4 Pin configuration (SSOP20).

CHARACTERISTICS OF THE I²C-BUS

The I²C-bus is for 2-way, 2-line communication between different ICs or modules. The two lines are a serial data line (SDA) and a serial clock line (SCL). Both lines must be connected to a positive supply via a pull-up resistor when connected to the output stages of a device. Data transfer may be initiated only when the bus is not busy.

6.1 Bit transfer

One data bit is transferred during each clock pulse. The data on the SDA line must remain stable during the HIGH period of the clock pulse as changes in the data line at this time will be interpreted as control signals (see Fig.5).

6.2 Start and stop conditions

Both data and clock lines remain HIGH when the bus is not busy. A HIGH-to-LOW transition of the data line, while the clock is HIGH is defined as the start condition (S).
A LOW-to-HIGH transition of the data line while the clock is HIGH is defined as the stop condition (P) (see Fig.6).

6.3 System configuration

A device generating a message is a 'transmitter', a device receiving is the 'receiver'. The device that controls the message is the 'master' and the devices which are controlled by the master are the 'slaves' (see Fig.7).

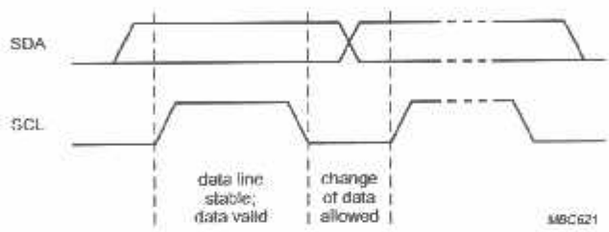


Fig.5 Bit transfer.

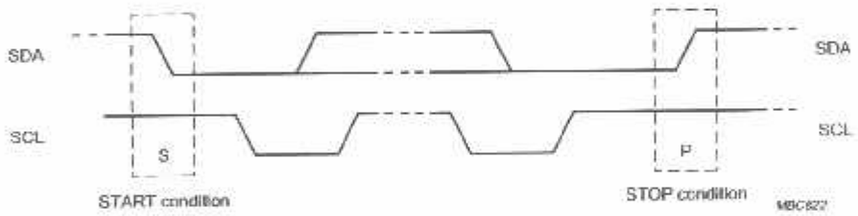


Fig.6 Definition of start and stop conditions.

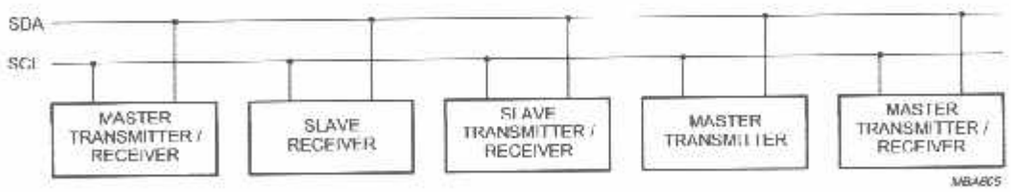


Fig.7 System configuration.

8.4 Acknowledge

The number of data bytes transferred between the start and the stop conditions from transmitter to receiver is not limited. Each byte of eight bits is followed by one acknowledge bit (see Fig.8). The acknowledge bit is a HIGH level put on the bus by the transmitter whereas the master generates an extra acknowledge related clock pulse.

A slave receiver which is addressed must generate an acknowledge after the reception of each byte. Also a master must generate an acknowledge after the reception of each byte that has been clocked out of the slave transmitter. The device that acknowledges has to pull down the SDA line during the acknowledge clock pulse, so that the SDA line is stable LOW during the HIGH period of the acknowledge related clock pulse, set-up and hold times must be taken into account.

A master receiver must signal an end of data to the transmitter by **not** generating an acknowledge on the last byte that has been clocked out of the slave. In this event the transmitter must leave the data line HIGH to enable the master to generate a stop condition.

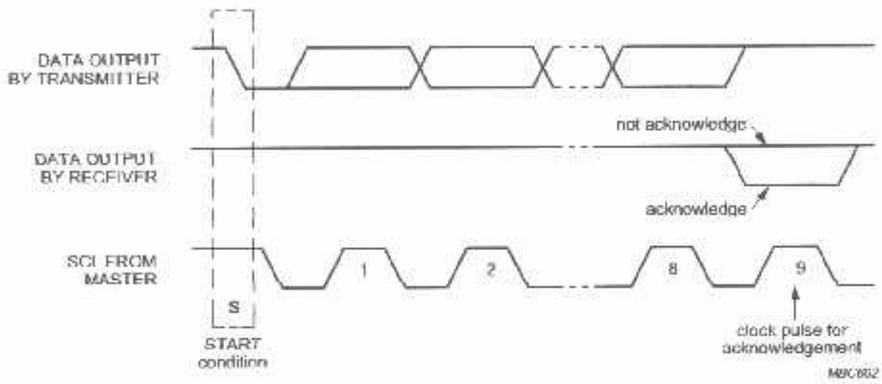


Fig.8 Acknowledgment on the I²C-bus.

FUNCTIONAL DESCRIPTION

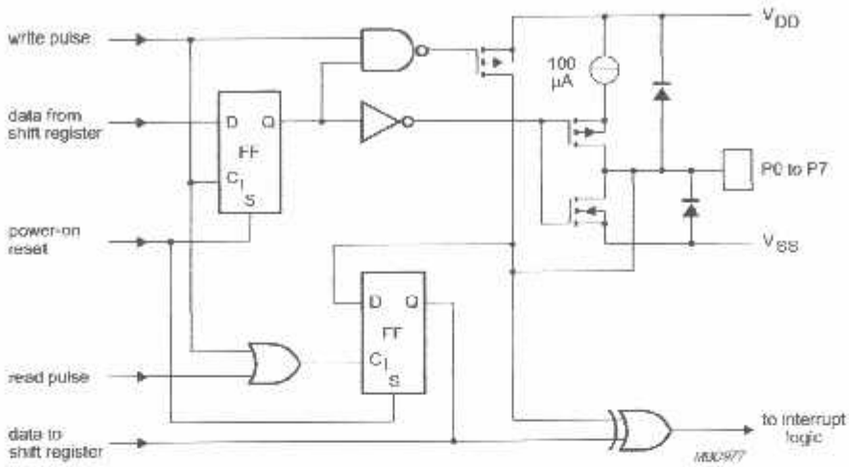


Fig.9 Simplified schematic diagram of each I/O.

.1 Addressing

or addressing see Figs 10, 11 and 12.

a. PCF8574.

b. PCF8574A.

Fig.10 PCF8574 and PCF8574A slave addresses.

ach of the PCF8574's eight I/Os can be independently used as an input or output. Input data is transferred from the ort to the microcontroller by the READ mode (see Fig.12). Output data is transmitted to the port by the WRITE mode see Fig.11).

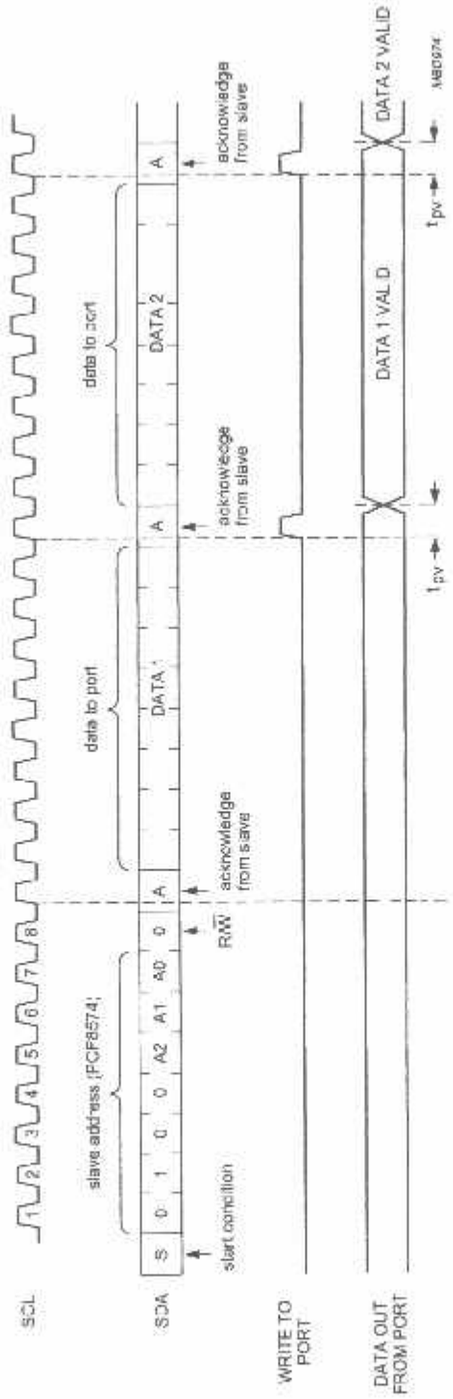
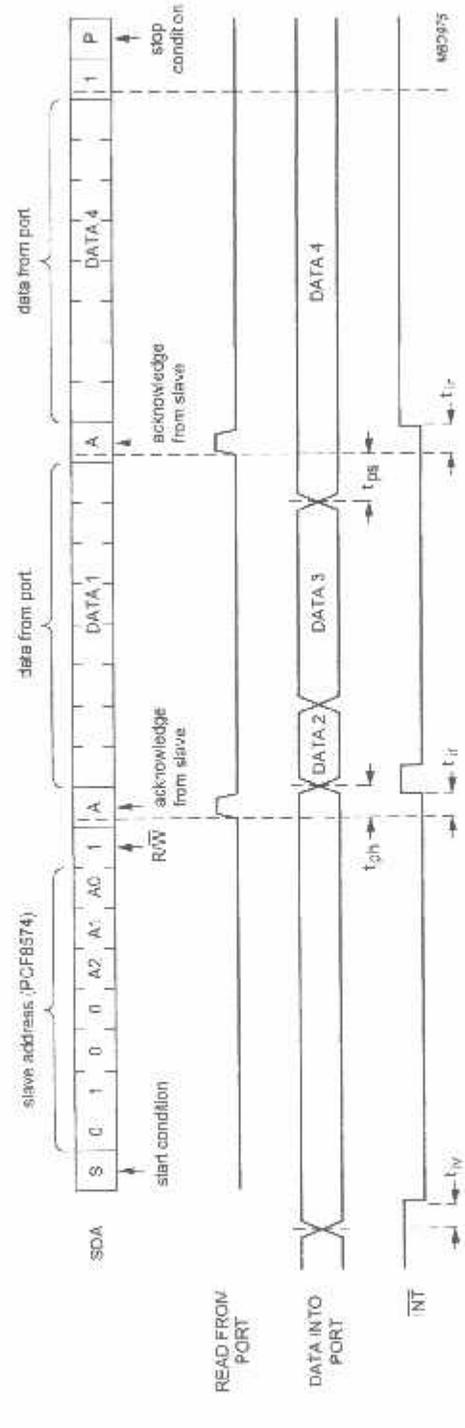


Fig.11 WRITE mode (output).



A LOW-to-HIGH transition of SDA, while SCL is HIGH is defined as the stop condition (P). Transfer of data can be stopped at any moment by a stop condition. When this occurs, data present at the last acknowledge phase is valid (output mode). Input data is lost.

Fig.12 READ mode (input).

.2 Interrupt output

The PCF8574 provides an open-drain output ($\overline{INT}$) which an be fed to a corresponding input of the microcontroller see Figs 13 and 14). This gives these chips a type of laster function which can initiate an action elsewhere in he system.

An interrupt is generated by any rising or falling edge of the ort inputs in the input mode. After time t_{iv} the signal $\overline{INT}$ is alid.

Resetting and reactivating the interrupt circuit is achieved hen data on the port is changed to the original setting or ata is read from or written to the port which has generated he interrupt.

Resetting occurs as follows:

- In the READ mode at the acknowledge bit after the rising edge of the SCL signal
- In the WRITE mode at the acknowledge bit after the HIGH-to-LOW transition of the SCL signal
- Interrupts which occur during the acknowledge clock pulse may be lost (or very short) due to the resetting of the interrupt during this pulse.

Each change of the I/Os after resetting will be detected and, after the next rising clock edge, will be transmitted as $\overline{INT}$. Reading from or writing to another device does not affect the interrupt circuit.

7.3 Quasi-bidirectional I/Os

A quasi-bidirectional I/O can be used as an input or output without the use of a control signal for data direction (see Fig.15). At power-on the I/Os are HIGH. In this mode only a current source to V_{DD} is active. An additional strong pull-up to V_{DD} allows fast rising edges into heavily loaded outputs. These devices turn on when an output is written HIGH, and are switched off by the negative edge of SCL. The I/Os should be HIGH before being used as inputs.

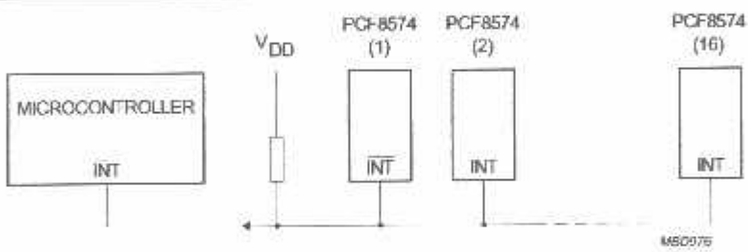


Fig.13 Application of multiple PCF8574s with interrupt.

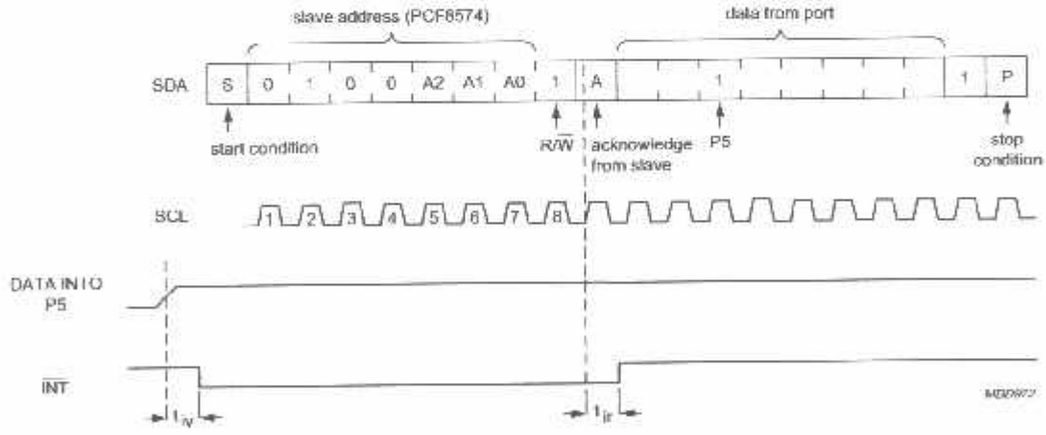


Fig.14 Interrupt generated by a change of input to I/O P5.

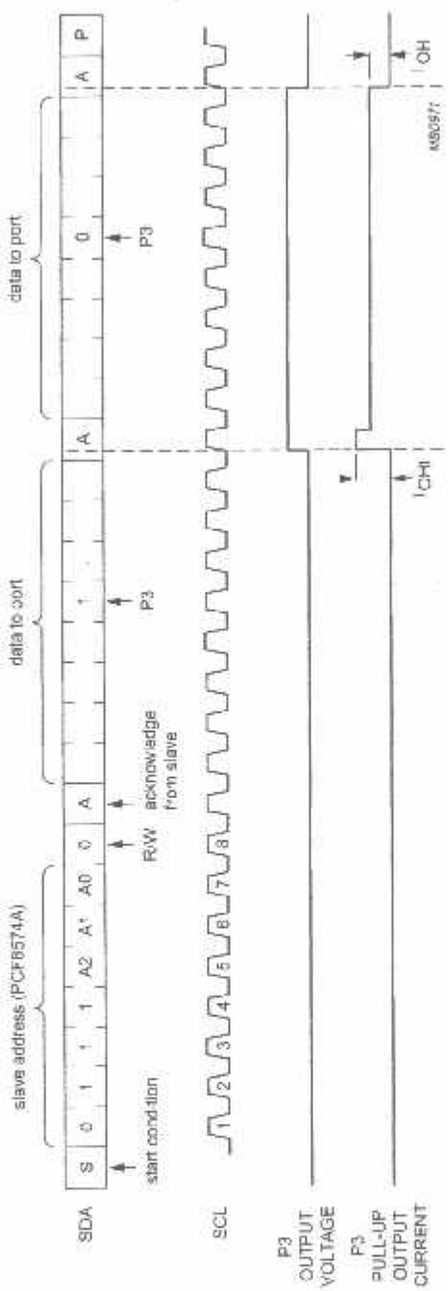


Fig.15 Transient pull-up current I_{OHL} while P3 changes from LOW-to-HIGH and back to LOW.

LIMITING VALUES

accordance with the Absolute Maximum Rating System (IEC 60134).

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
V_{DD}	supply voltage	−0.5	+7.0	V
V_I	input voltage	V_{SS} − 0.5	V_{DD} + 0.5	V
I_I	DC input current	–	±20	mA
I_O	DC output current	–	±25	mA
I_{DD}	supply current	–	±100	mA
I_{SS}	supply current	–	±100	mA
P_{tot}	total power dissipation	–	400	mW
P_O	power dissipation per output	–	100	mW
T_{stg}	storage temperature	−65	+150	°C
T_{amb}	ambient temperature	−40	+85	°C

HANDLING

puts and outputs are protected against electrostatic discharge in normal handling. However it is good practice to take ormal precautions appropriate to handling MOS devices (see *"Handling MOS devices"*).

DC CHARACTERISTICS

V_{DD} = 2.5 to 6 V; V_{SS} = 0 V; T_{amb} = −40 to +85 °C; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
upply						
V_{DD}	supply voltage		2.5	–	6.0	V
I_{DD}	supply current	operating mode; V_{DD} = 6 V; no load; V_I = V_{DD} or V_{SS}; f_{SCL} = 100 kHz	–	40	100	µA
I_{stb}	standby current	standby mode; V_{DD} = 6 V; no load; V_I = V_{DD} or V_{SS}	–	2.5	10	µA
V_{POR}	Power-on reset voltage	V_{DD} = 6 V; no load; V_I = V_{DD} or V_{SS}; note 1	–	1.3	2.4	V
put SCL; input/output SDA						
V_{IL}	LOW level input voltage		−0.5	–	+0.3V_{DD}	V
V_{IH}	HIGH level input voltage		0.7V_{DD}	–	V_{DD} + 0.5	V
I_{OL}	LOW level output current	V_{OL} = 0.4 V	3	–	–	mA
I_L	leakage current	V_I = V_{DD} or V_{SS}	−1	–	+1	µA
C_i	input capacitance	V_I = V_{SS}		–	7	pF

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
'Os						
$'_{IL}$	LOW level input voltage		−0.5	−	$+0.3V_{DD}$	V
$'_{IH}$	HIGH level input voltage		$0.7V_{DD}$	−	V_{DD} + 0.5	V
$_{HL(max)}$	maximum allowed input current through protection diode	$V_I \geq V_{DD}$ or $V_I \leq V_{SS}$	−	−	±400	µA
$_{OL}$	LOW level output current	V_{OL} = 1 V; V_{DD} = 5 V	10	25	−	mA
$_{OH}$	HIGH level output current	$V_{OH} = V_{SS}$	30	−	300	µA
$_{OHt}$	transient pull-up current	HIGH during acknowledge (see Fig.15); $V_{OH} = V_{SS}$; V_{DD} = 2.5 V	−	−1	−	mA
$_i$	input capacitance		−	−	10	pF
$_{io}$	output capacitance		−	−	10	pF
'ort timing; $C_L \leq$ 100 pF (see Figs 11 and 12)						
$_{v}$	output data valid		−	−	4	µs
$_{su}$	input data set-up time		0	−	−	µs
$_h$	input data hold time		4	−	−	µs
nterrupt $\overline{INT}$ (see Fig.14)						
$_{IL}$	LOW level output current	V_{OL} = 0.4 V	1.6	−	−	mA
$_{iL}$	leakage current	$V_I = V_{DD}$ or V_{SS}	−1	−	+1	µA
IMING; $C_i \leq$ 100 pF						
$_v$	input data valid time		−	−	4	µs
$_r$	reset delay time			−	4	µs
elect inputs A0 to A2						
$_{IL}$	LOW level input voltage		−0.5	−	$+0.3V_{DD}$	V
$_{IH}$	HIGH level input voltage		$0.7V_{DD}$	−	V_{DD} + 0.5	V
$_{LI}$	input leakage current	pin at V_{DD} or V_{SS}	−250		+250	nA

ote

The Power-on reset circuit resets the I²C-bus logic at $V_{DD} < V_{POR}$ and sets all I/Os to logic 1 (with current source to V_{DD}).

1 I²C-BUS TIMING CHARACTERISTICS

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
²C-bus timing (see Fig.16; note 1)					
SCL	SCL clock frequency		–	100	kHz
SW	tolerable spike width on bus	–	–	100	ns
BUF	bus free time	4.7	–		µs
SU;STA	START condition set-up time	4.7	–	–	µs
HD;STA	START condition hold time	4.0	–		µs
LOW	SCL LOW time	4.7	–	–	µs
H GH	SCL HIGH time	4.0	–		µs
-	SCL and SDA rise time	–	–	1.0	µs
f	SCL and SDA fall time	–		0.3	µs
SU;DAT	data set-up time	250	–	–	ns
HD;DAT	data hold time	0	–	–	ns
VD;DAT	SCL LOW to data out valid	–		3.4	µs
SU;STO	STOP condition set-up time	4.0	–		µs

ote

All the timing values are valid within the operating supply voltage and ambient temperature range and refer to V_{IL} and V_{IH} with an input voltage swing of V_{SS} to V_{DD}.

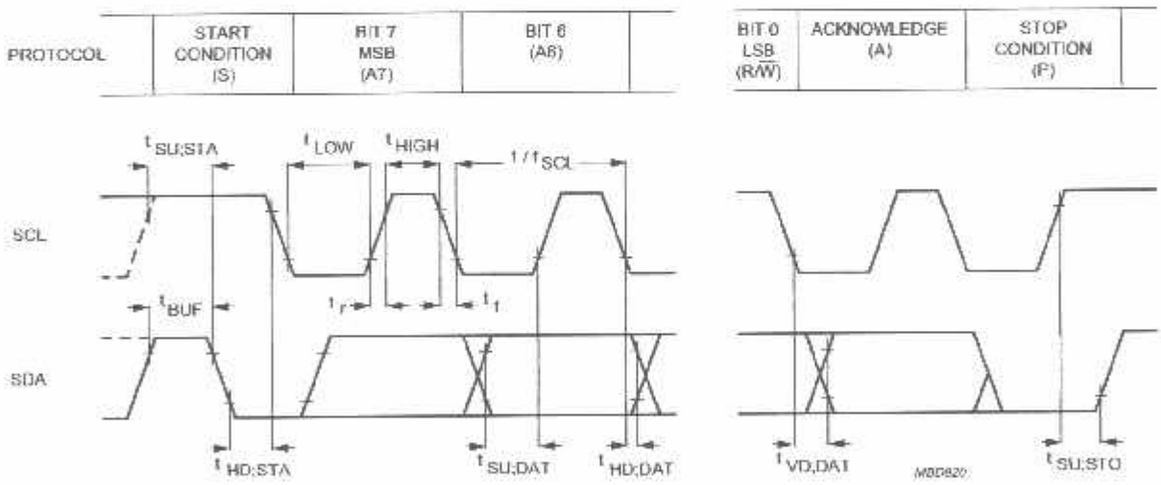
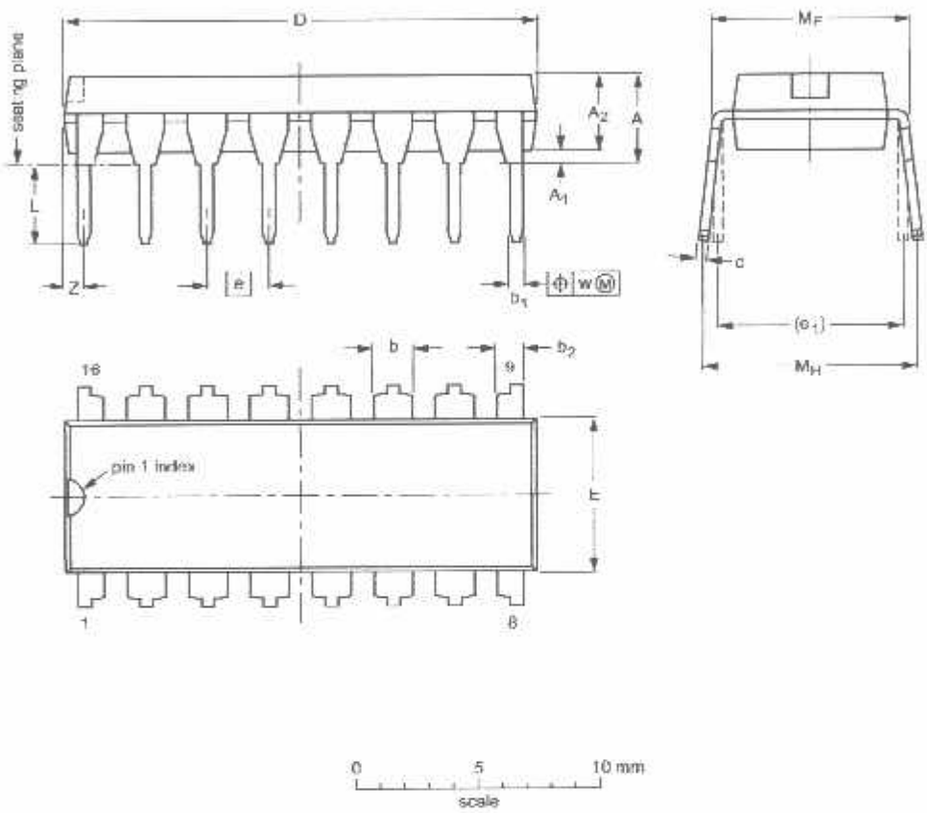


Fig.16 I²C-bus timing diagram.

? PACKAGE OUTLINES

IP16: plastic dual in-line package; 16 leads (300 mil) **SOT38-4**



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

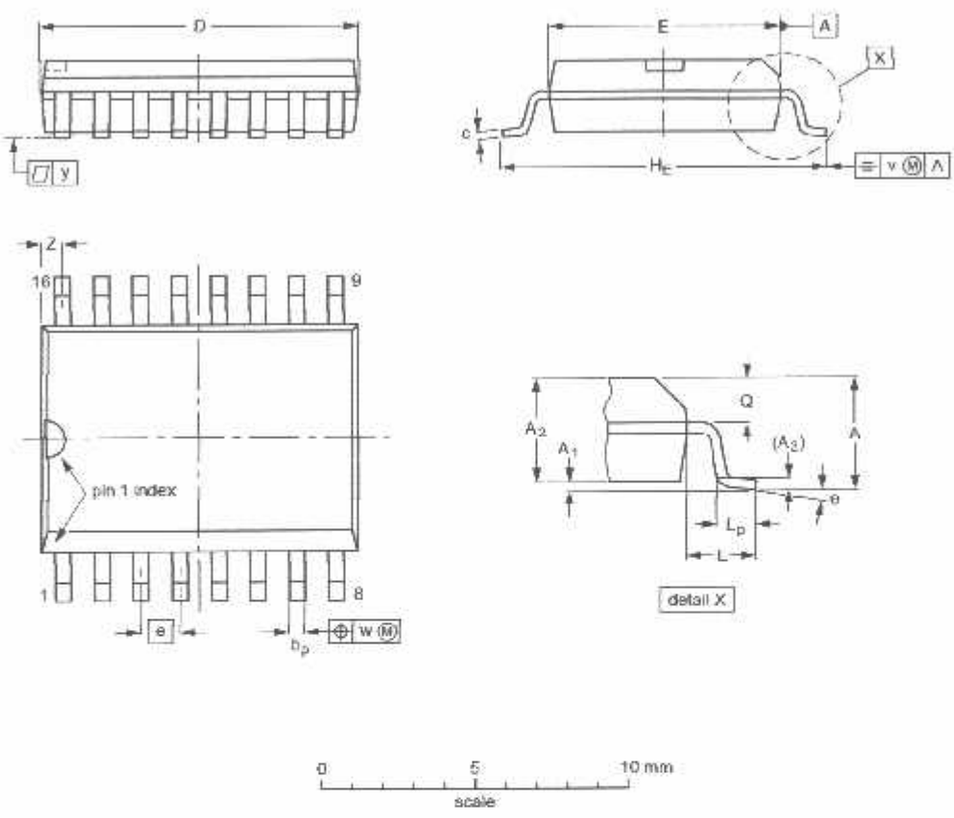
UNIT	A max.	A_1 min.	A_2 max.	b	b_1	b_2	c	$D^{(1)}$	$E^{(1)}$	e	e_1	L	M_E	M_H	w	$Z^{(1)}$ max.
mm	4.2	0.51	3.2	1.73 1.30	0.53 0.38	1.25 0.85	0.36 0.23	19.50 18.55	6.48 6.20	2.54	7.62	3.60 3.05	8.25 7.80	10.0 8.3	0.254	0.76
inches	0.17	0.020	0.13	0.068 0.051	0.021 0.015	0.049 0.033	0.014 0.009	0.77 0.73	0.26 0.24	0.10	0.30	0.14 0.12	0.32 0.31	0.39 0.33	0.01	0.030

Note

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT38-4						~~92-11-17~~ 95-01-14

SO16: plastic small outline package; 16 leads; body width 7.5 mm **SOT162-1**



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

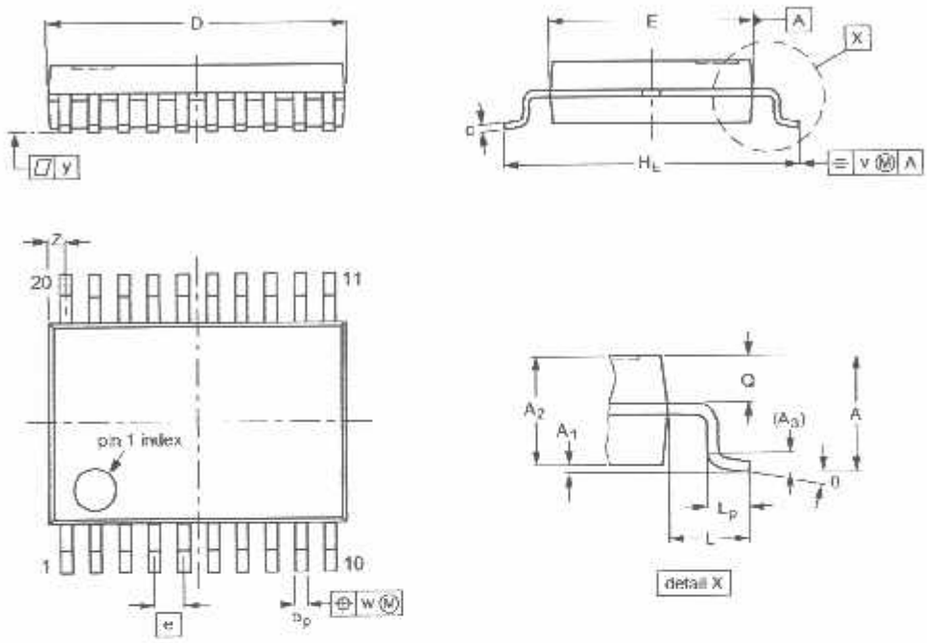
UNIT	A max.	A_1	A_2	A_3	b_p	c	D(1)	E(1)	e	H_E	L	L_p	Q	v	w	y	Z(1)	θ
mm	2.65	0.30 0.10	2.45 2.25	0.25	0.49 0.36	0.32 0.23	10.5 10.1	7.6 7.4	1.27	10.65 10.00	1.4	1.1 0.4	1.1 1.0	0.25	0.25	0.1	0.9 0.4	8° 0°
inches	0.10	0.012 0.004	0.096 0.089	0.01	0.019 0.014	0.013 0.009	0.41 0.40	0.30 0.29	0.050	0.419 0.394	0.055	0.043 0.016	0.043 0.039	0.01	0.01	0.004	0.035 0.016	

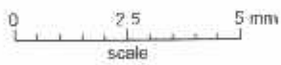
Note

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT162-1	075E03	MS-013				~~97-05-22~~ 99-12-27

SSOP20: plastic shrink small outline package; 20 leads; body width 4.4 mm **SOT266-1**





DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(1)}$	e	H_E	L	L_p	Q	v	w	y	$Z^{(1)}$	θ
mm	1.5	0.15 0	1.4 1.2	0.25	0.32 0.20	0.20 0.13	6.6 6.4	4.5 4.3	0.65	6.6 6.2	1.0	0.75 0.45	0.65 0.45	0.2	0.13	0.1	0.48 0.18	10° 0°

Note

1. Plastic or metal protrusions of 0.20 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES					EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ				
SOT266-1		MO-152					~~95-02-22~~ 99-12-27

3 SOLDERING

3.1 Introduction

This text gives a very brief insight to a complex technology. A more in-depth account of soldering ICs can be found in our *"Data Handbook IC26; Integrated Circuit Packages"* (document order number 9398 652 90011).

There is no soldering method that is ideal for all IC packages. Wave soldering is often preferred when through-hole and surface mount components are mixed on one printed-circuit board. Wave soldering can still be used for certain surface mount ICs, but it is not suitable for fine pitch SMDs. In these situations reflow soldering is recommended.

3.2 Through-hole mount packages

3.2.1 SOLDERING BY DIPPING OR BY SOLDER WAVE

The maximum permissible temperature of the solder is 260 °C; solder at this temperature must not be in contact with the joints for more than 5 seconds. The total contact time of successive solder waves must not exceed 5 seconds.

The device may be mounted up to the seating plane, but the temperature of the plastic body must not exceed the specified maximum storage temperature ($T_{stg(max)}$). If the printed-circuit board has been pre-heated, forced cooling may be necessary immediately after soldering to keep the temperature within the permissible limit.

3.2.2 MANUAL SOLDERING

Apply the soldering iron (24 V or less) to the lead(s) of the package, either below the seating plane or not more than 2 mm above it. If the temperature of the soldering iron bit is less than 300 °C it may remain in contact for up to 10 seconds. If the bit temperature is between 300 and 400 °C, contact may be up to 5 seconds.

3.3 Surface mount packages

3.3.1 REFLOW SOLDERING

Reflow soldering requires solder paste (a suspension of fine solder particles, flux and binding agent) to be applied to the printed-circuit board by screen printing, stencilling or pressure-syringe dispensing before package placement.

Several methods exist for reflowing; for example, convection or convection/infrared heating in a conveyor type oven. Throughput times (preheating, soldering and cooling) vary between 100 and 200 seconds depending on heating method.

Typical reflow peak temperatures range from 215 to 250 °C. The top-surface temperature of the packages should preferable be kept below 220 °C for thick/large packages, and below 235 °C for small/thin packages.

13.3.2 WAVE SOLDERING

Conventional single wave soldering is not recommended for surface mount devices (SMDs) or printed-circuit boards with a high component density, as solder bridging and non-wetting can present major problems.

To overcome these problems the double-wave soldering method was specifically developed.

If wave soldering is used the following conditions must be observed for optimal results:

- Use a double-wave soldering method comprising a turbulent wave with high upward pressure followed by a smooth laminar wave.
- For packages with leads on two sides and a pitch (e):
  - larger than or equal to 1.27 mm, the footprint longitudinal axis is **preferred** to be parallel to the transport direction of the printed-circuit board;
  - smaller than 1.27 mm, the footprint longitudinal axis **must** be parallel to the transport direction of the printed-circuit board.

  The footprint must incorporate solder thieves at the downstream end.
- For packages with leads on four sides, the footprint must be placed at a 45° angle to the transport direction of the printed-circuit board. The footprint must incorporate solder thieves downstream and at the side corners.

During placement and before soldering, the package must be fixed with a droplet of adhesive. The adhesive can be applied by screen printing, pin transfer or syringe dispensing. The package can be soldered after the adhesive is cured.

Typical dwell time is 4 seconds at 250 °C.
A mildly-activated flux will eliminate the need for removal of corrosive residues in most applications.

13.3.3 MANUAL SOLDERING

Fix the component by first soldering two diagonally-opposite end leads. Use a low voltage (24 V or less) soldering iron applied to the flat part of the lead. Contact time must be limited to 10 seconds at up to 300 °C. When using a dedicated tool, all other leads can be soldered in one operation within 2 to 5 seconds between 270 and 320 °C.

13.4 Suitability of IC packages for wave, reflow and dipping soldering methods

MOUNTING	PACKAGE[1]	SOLDERING METHOD		
		WAVE	REFLOW[2]	DIPPING
Through-hole mount	DBS, DIP, HDIP, SDIP, SIL	suitable[3]	–	suitable
Surface mount	BGA, LBGA, LFBGA, SQFP, TFBGA, VFBGA	not suitable	suitable	–
	HBCC, HBGA, HLQFP, HSQFP, HSOP, HTQFP, HTSSOP, HVQFN, HVSON, SMS	not suitable[4]	suitable	–
	PLCC[5], SO, SOJ	suitable	suitable	–
	LQFP, QFP, TQFP	not recommended[5][6]	suitable	–
	SSOP, TSSOP, VSO	not recommended[7]	suitable	–

Notes

1. For more detailed information on the BGA packages refer to the *"(LF)BGA Application Note"* (AN01026); order a copy from your Philips Semiconductors sales office.
2. All surface mount (SMD) packages are moisture sensitive. Depending upon the moisture content, the maximum temperature (with respect to time) and body size of the package, there is a risk that internal or external package cracks may occur due to vaporization of the moisture in them (the so called popcorn effect). For details, refer to the Drypack information in the *"Data Handbook IC26; Integrated Circuit Packages; Section: Packing Methods"*.
3. For SDIP packages, the longitudinal axis must be parallel to the transport direction of the printed-circuit board.
4. These packages are not suitable for wave soldering. On versions with the heatsink on the bottom side, the solder cannot penetrate between the printed-circuit board and the heatsink. On versions with the heatsink on the top side, the solder might be deposited on the heatsink surface.
5. If wave soldering is considered, then the package must be placed at a 45° angle to the solder wave direction. The package footprint must incorporate solder thieves downstream and at the side corners.
6. Wave soldering is suitable for LQFP, QFP and TQFP packages with a pitch (e) larger than 0.8 mm; it is definitely not suitable for packages with a pitch (e) equal to or smaller than 0.65 mm.
7. Wave soldering is suitable for SSOP and TSSOP packages with a pitch (e) equal to or larger than 0.65 mm; it is definitely not suitable for packages with a pitch (e) equal to or smaller than 0.5 mm.

DATA SHEET STATUS

LEVEL	DATA SHEET STATUS[1]	PRODUCT STATUS[2][3]	DEFINITION
	Objective data	Development	This data sheet contains data from the objective specification for product development. Philips Semiconductors reserves the right to change the specification in any manner without notice.
	Preliminary data	Qualification	This data sheet contains data from the preliminary specification. Supplementary data will be published at a later date. Philips Semiconductors reserves the right to change the specification without notice, in order to improve the design and supply the best possible product.
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otes

Please consult the most recently issued data sheet before initiating or completing a design.

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For data sheets describing multiple type numbers, the highest-level product status determines the data sheet status.

5 DEFINITIONS

hort-form specification — The data in a short-form ›ecification is extracted from a full data sheet with the ime type number and title. For detailed information see e relevant data sheet or data handbook.

imiting values definition — Limiting values given are in ccordance with the Absolute Maximum Rating System EC 60134). Stress above one or more of the limiting alues may cause permanent damage to the device. hese are stress ratings only and operation of the device these or at any other conditions above those given in the haracteristics sections of the specification is not implied. xposure to limiting values for extended periods may ffect device reliability.

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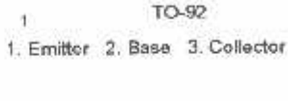
SS9012

1W Output Amplifier of Potable Radios in Class B Push-pull Operation.

- High total power dissipation. (P_T=625mW)
- High Collector Current. (I_C= -500mA)
- Complementary to SS9013
- Excellent h_{FE} linearity.



1. Emitter 2. Base 3. Collector

PNP Epitaxial Silicon Transistor

Absolute Maximum Ratings T_a=25°C unless otherwise noted

Symbol	Parameter	Ratings	Units
V_{CBO}	Collector-Base Voltage	-40	V
V_{CEO}	Collector-Emitter Voltage	-20	V
V_{EBO}	Emitter-Base Voltage	-5	V
I_C	Collector Current	-500	A
P_C	Collector Power Dissipation	625	W
T_J	Junction Temperature	150	°C
T_{STG}	Storage Temperature	-55 ~ 150	°C

Electrical Characteristics T_a=25°C unless otherwise noted

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Units
BV_{CBO}	Collector-Base Breakdown Voltage	I_C = -100μA, I_E =0	-40			V
BV_{CEO}	Collector-Emitter Breakdown Voltage	I_C = -1mA, I_B =0	-20			V
BV_{EBO}	Emitter-Base Breakdown Voltage	I_E = -100μA, I_C =0	-5			V
I_{CBO}	Collector Cut-off Current	V_{CB} = -25V, I_E =0			-100	nA
I_{EBO}	Emitter Cut-off Current	V_{EB} = -3V, I_C =0			-100	nA
h_{FE1} h_{FE2}	DC Current Gain	V_{CE} = -1V, I_C = -50mA V_{CE} = -1V, I_C = -500mA	64 40	120 90	202	
V_{CE} (sat)	Collector-Emitter Saturation Voltage	I_C = -500mA, I_B = -50mA		-0.18	-0.6	V
V_{BE} (sat)	Base-Emitter Saturation Voltage	I_C = -500mA, I_B = -50mA		-0.95	-1.2	V
V_{BE} (on)	Base-Emitter On Voltage	V_{CE} = -1V, I_C = -10mA	-0.6	-0.67	0.7	V

h_{FE} Classification

Classification	D	E	F	G	H
h_{FE1}	64 ~ 91	78 ~ 112	96 ~ 135	112 ~ 166	144 ~ 202

Typical Characteristics

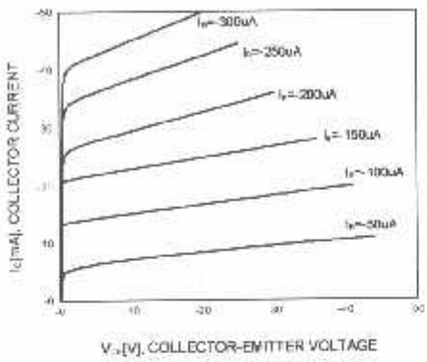


Figure 1. Static Characteristic

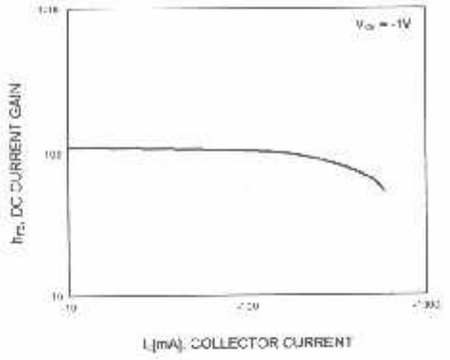


Figure 2. DC current Gain

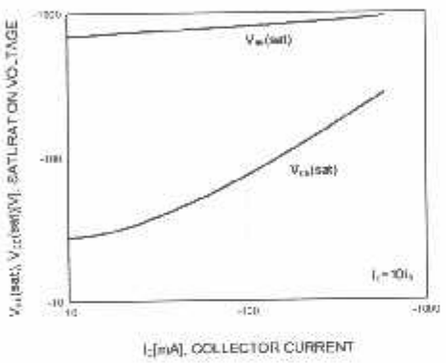


Figure 3. Base-Emitter Saturation Voltage
Collector-Emitter Saturation Voltage

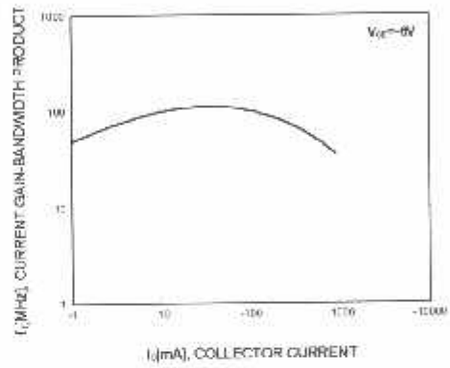
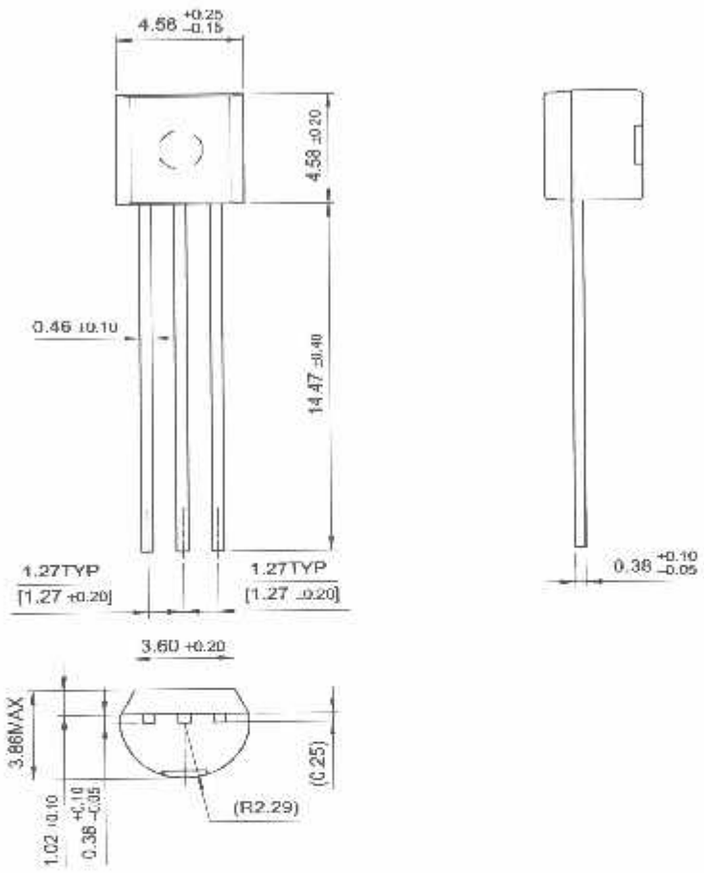


Figure 4. Current Gain Bandwidth Product

Package Demensions

TO-92



Dimensions in Millimeters

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PRODUCT STATUS DEFINITIONS

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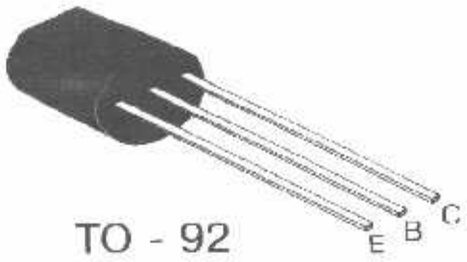
NPN Epitaxial Silicon Transistor

revised October 1999

1W OUTPUT AMPLIFIER OF PORTABLE RADIOS IN CLASS B PUSH-PULL OPERATION

- High total power dissipation (PT=625mW)
- High Collector Current (I_C =500mA)
- Excellent h_{FE} linearity.



TO - 92

CLASSIFICATION h_{FE} (1)

Classification	D	E	F	G	H
h_{FE} (1)	64-91	78-112	96-135	112-166	144-202

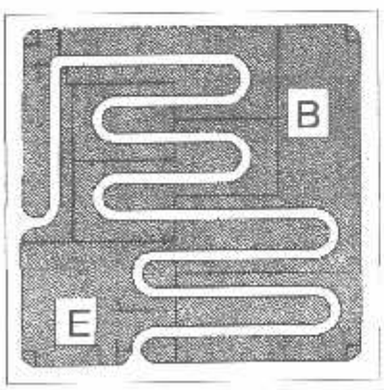
Absolute Maximum Ratings (Ta=25°C)

Symbol	Parameter	Rating	Units
V_{CBO}	Collector-Base Voltage	40	V
V_{CEO}	Collector-Emitter Voltage	20	V
V_{EBO}	Emitter-Base Voltage	5	V
I_C	Collector Current	500	mA
P_C	Collector Dissipation	625	mW
T_j	Junction Temperature	150	°C
T_{stg}	Storage Temperature	-55 ~ 150	°C

Electrical Characteristics (T_a = 25°C)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
BV_{CBO}	Collector-Base Breakdown Voltage	I_C =100μA, I_E =0	40			V
BV_{CEO}	Collector-Emitter Breakdown Voltage	I_C =1mA, I_B =0	20			V
BV_{EBO}	Emitter-Base Breakdown Voltage	I_E =100μA, I_C =0	5			V
I_{CBO}	Collector Cutoff Current	V_{CB}=25V, I_E =0			100	nA
I_{EBO}	Emitter Cutoff Current	V_{EB}=3V, I_C =0			100	nA
$h_{FE}1$	DC Current Gain	V_{CE}=1V, I_C =50mA	64	120	202	
$h_{FE}2$		V_{CE}=1V, I_C =500mA	40	120		
V_{CE}(sat)	Collector-Emitter Saturation Voltage	I_C =500mA, I_B =50mA		0.16	0.6	V
V_{BE}(sat)	Base-Emitter Saturation Voltage	I_C =500mA, I_B =50mA		0.91	1.2	V
$V_{BE(on)}$	Base-Emitter On Voltage	V_{CE}=1V, I_C =10mA	0.6	0.67	0.7	V

Pad Location



- DIE SIZE 495 X 495μm
- DIE THICKNESS Typ. 470 μm

- BONDING PAD SIZE
  - Emitter 85 x 114 μm
  - Base 85 x 154 μm

GAS SENSORS : TYPE AF30

CIGARETTE SMOKE SENSOR

DESCRIPTION:

Gas sensor made with thick film element.

FEATURES:

- Constant heater voltage
- Tight resistance tolerance
- High sensitivity
- Typical applications include air purifier

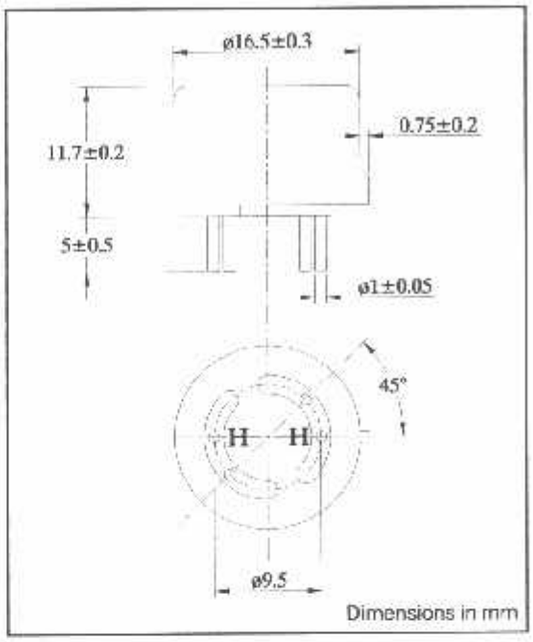
DATA:

Operating conditions:
Operating temperature ..... -10 to +55°C
Storage temperature ..... -30 to +60°C
Load Resistor R_L ..... Variable
Heater resistance ..... 27Ω (nom)
Rated power consumption P_s ..... <15mW
Rated working voltage of circuit V_c .....
..... 5V d.c. or 5V rms a.c. (max 12V)
Rated working voltage of heater .....
..... 5 ±0.2V d.c.
..... 5 ±0.2 V rms a.c.
Parts and material:
Sensing element ..... Semi-conducting oxide
Thick film heater ..... Platinum
Case ..... Nylon 66
Pin ..... Nickel alloy
Flame arrestor .....
... Double 100-mesh stainless gauze (SUS316)

Sensitivity characteristics:

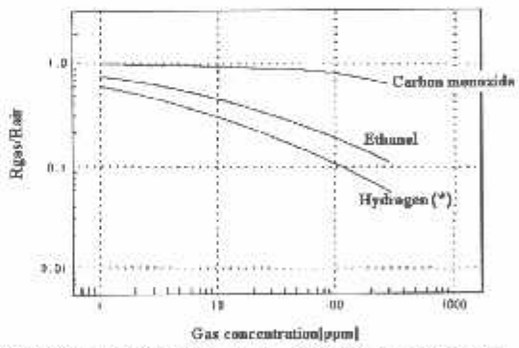
	Specification	Conditions
Sensor resistance Rgas	15k to 35k Ω	In clean air
Gas sensitivity Rgas/Rair	0.2 to 0.4	Resistance ratio at 10ppm H_2 to clean air (*)
Power consumption	535mW (max)	

DIMENSIONS:



Dimensions in mm

Typical gas sensitivity:



(*) Correlation between H_2 and cigarette smoke

Mechanical characteristics:

Test	Condition		Performance
Vibration	Frequency:	10 - 500 Hz	Should satisfy the specifications shown in the sensitivity characteristics
	Amplitude (10 - 50Hz):	2 mm	
	Acceleration (50 - 500 Hz)	10G	
	Recipricol scanning time:	5 min	
	Test time: 2 hours each for X, Y and Z directions		
Shock	Acceleration:	100G	
	Number of impacts:	5	

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Fax +44 (0) 823 332637

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Fax +1 (732) 287 8847

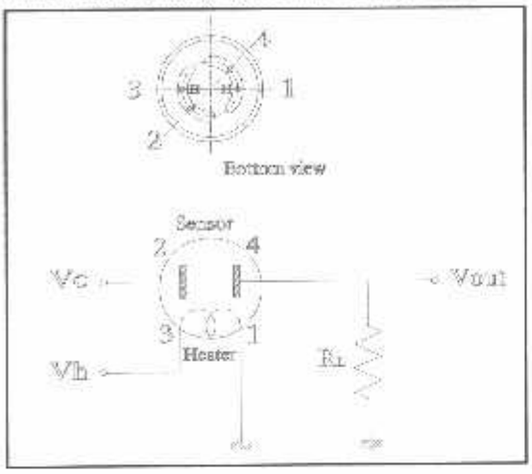
967 Windfall Road
St Marys, Pennsylvania 15857-3397 USA
Tel +1 (814) 834 9140
Fax +1 (814) 781 7969

GAS SENSORS : TYPE AF30

SMOKE SENSOR

NOTES:

Pin allocation and standard test circuit:



Test conditions:

Atmosphere

Clean air at 25± 2°C and 50±5% RH without noise gas.

Circuit condition

Vc (circuit voltage) ..... 5±0.05V
Vh (heater voltage) ..... 5±0.05V
Preheat time ..... 48 hours

Test gas

Hydrogen 10ppm

WARNING:

Do not use if the case or wire netting is damaged, otherwise built-in heater may cause explosions or fires.
Do not disassemble or change any parts.
Use only within specified conditions.

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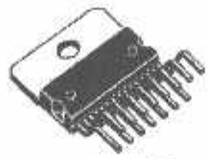
L298

DUAL FULL-BRIDGE DRIVER

- OPERATING SUPPLY VOLTAGE UP TO 46 V
- TOTAL DC CURRENT UP TO 4 A
- LOW SATURATION VOLTAGE
- OVERTEMPERATURE PROTECTION
- LOGICAL "0" INPUT VOLTAGE UP TO 1.5 V (HIGH NOISE IMMUNITY)



Multiwatt15

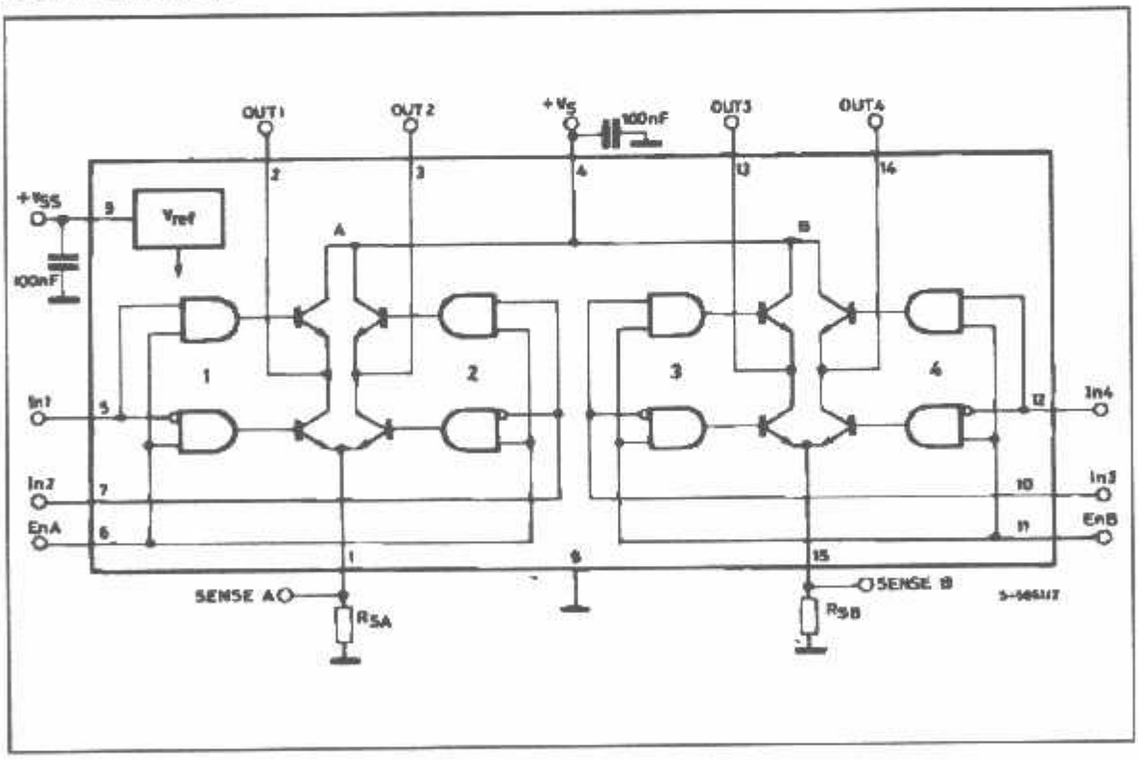
PowerSO20

ORDERING NUMBERS : L298N (Multiwatt Vert.)
L298HN (Multiwatt Horiz.)
L298P (PowerSO20)

DESCRIPTION

The L298 is an integrated monolithic circuit in a 15-lead Multiwatt and PowerSO20 packages. It is a high voltage, high current dual full-bridge driver designed to accept standard TTL logic levels and drive inductive loads such as relays, solenoids, DC and stepping motors. Two enable inputs are provided to enable or disable the device independently of the input signals. The emitters of the lower transistors of each bridge are connected together and the corresponding external terminal can be used for the connection of an external sensing resistor. An additional supply input is provided so that the logic works at a lower voltage.

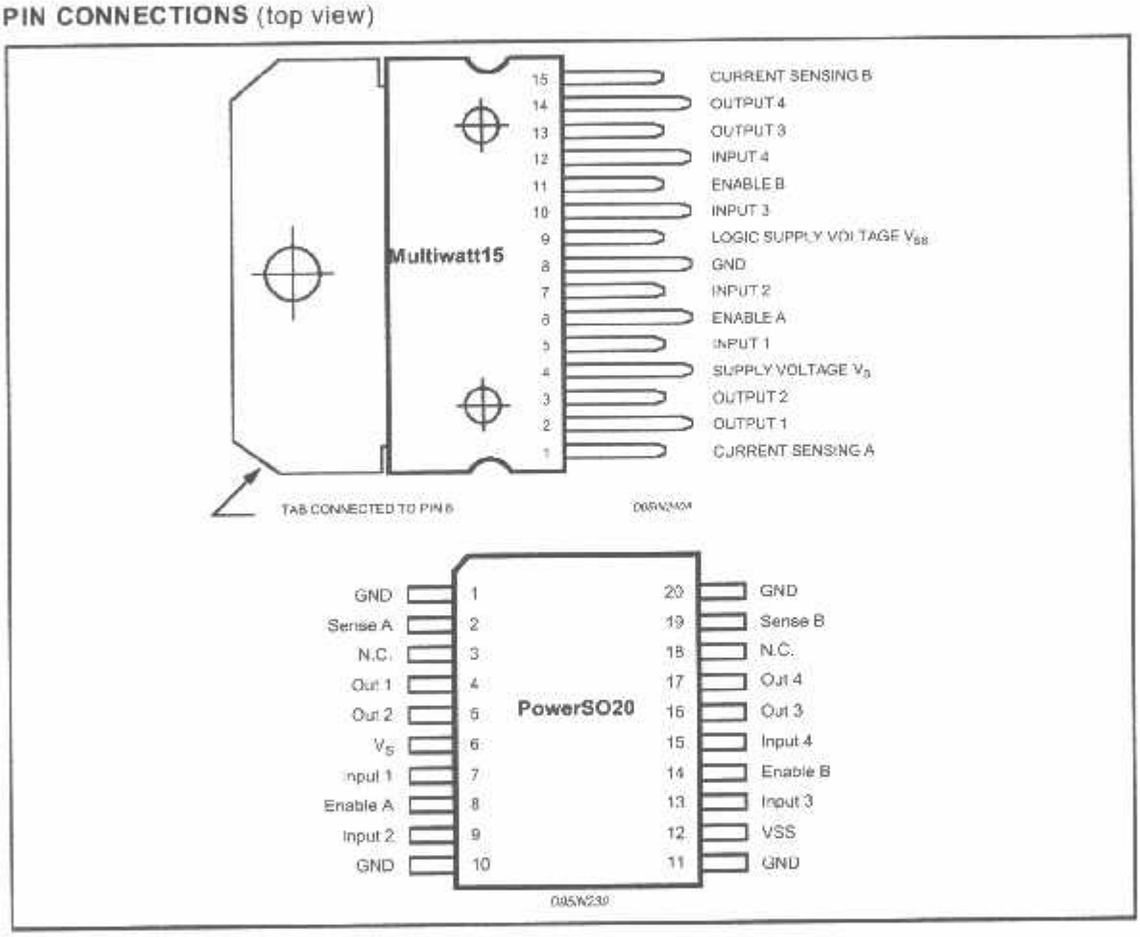
BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_S	Power Supply	50	V
V_{SS}	Logic Supply Voltage	7	V
V_i, V_{en}	Input and Enable Voltage	–0.3 to 7	V
I_O	Peak Output Current (each Channel) – Non Repetitive (t = 100µs) –Repetitive (80% on –20% off; t_{on} = 10ms) –DC Operation	 3 2.5 2	 A A A
V_{sens}	Sensing Voltage	–1 to 2.3	V
P_{tot}	Total Power Dissipation (T_{case} = 75°C)	25	W
T_{op}	Junction Operating Temperature	–25 to 130	°C
T_{stg}, T_j	Storage and Junction Temperature	–40 to 150	°C

PIN CONNECTIONS (top view)



THERMAL DATA

Symbol	Parameter		PowerSO20	Multiwatt15	Unit
$R_{th\ j\text{-}case}$	Thermal Resistance Junction-case	Max.	–	3	°C/W
$R_{th\ j\text{-}amb}$	Thermal Resistance Junction-ambient	Max.	13 (*)	35	°C/W

(*) Mounted on aluminum substrate

PIN FUNCTIONS (refer to the block diagram)

MW.15	PowerSO	Name	Function
1;15	2;19	Sense A; Sense B	Between this pin and ground is connected the sense resistor to control the current of the load.
2;3	4;5	Out 1; Out 2	Outputs of the Bridge A; the current that flows through the load connected between these two pins is monitored at pin 1.
4	6	V_S	Supply Voltage for the Power Output Stages. A non-inductive 100nF capacitor must be connected between this pin and ground.
5;7	7;9	Input 1; Input 2	TTL Compatible Inputs of the Bridge A.
6;11	8;14	Enable A; Enable B	TTL Compatible Enable Input: the L state disables the bridge A (enable A) and/or the bridge B (enable B).
8	1,10,11,20	GND	Ground.
9	12	VSS	Supply Voltage for the Logic Blocks. A100nF capacitor must be connected between this pin and ground.
10; 12	13;15	Input 3; Input 4	TTL Compatible Inputs of the Bridge B.
13; 14	16;17	Out 3; Out 4	Outputs of the Bridge B. The current that flows through the load connected between these two pins is monitored at pin 15.
–	3;18	N.C.	Not Connected

ELECTRICAL CHARACTERISTICS (V_S = 42V; V_{SS} = 5V, T_j = 25°C; unless otherwise specified)

Symbol	Parameter	Test Conditions		Min.	Typ.	Max.	Unit
V_S	Supply Voltage (pin 4)	Operative Condition		V_{IH} +2.5		46	V
V_{SS}	Logic Supply Voltage (pin 9)			4.5	5	7	V
I_S	Quiescent Supply Current (pin 4)	V_{en} = H; I_L = 0	V_i = L V_i = H		13 50	22 70	mA mA
		V_{en} = L	V_i = X			4	mA
I_{SS}	Quiescent Current from V_{SS} (pin 9)	V_{en} = H; I_L = 0	V_i = L V_i = H		24 7	36 12	mA mA
		V_{en} = L	V_i = X			6	mA
V_{IL}	Input Low Voltage (pins 5, 7, 10, 12)			–0.3		1.5	V
V_{IH}	Input High Voltage (pins 5, 7, 10, 12)			2.3		VSS	V
I_{IL}	Low Voltage Input Current (pins 5, 7, 10, 12)	V_i = L				–10	µA
I_{IH}	High Voltage Input Current (pins 5, 7, 10, 12)	V_i = H ≤ V_{SS} –0.6V			30	100	µA
V_{en} = L	Enable Low Voltage (pins 6, 11)			–0.3		1.5	V
V_{en} = H	Enable High Voltage (pins 6, 11)			2.3		V_{SS}	V
I_{en} = L	Low Voltage Enable Current (pins 6, 11)	V_{en} = L				–10	µA
I_{en} = H	High Voltage Enable Current (pins 6, 11)	V_{en} = H ≤ V_{SS} –0.6V			30	100	µA
$V_{CEsat(H)}$	Source Saturation Voltage	I_L = 1A I_L = 2A		0.95	1.35 2	1.7 2.7	V V
$V_{CEsat(L)}$	Sink Saturation Voltage	I_L = 1A (5) I_L = 2A (5)		0.85	1.2 1.7	1.6 2.3	V V
V_{CEsat}	Total Drop	I_L = 1A (5) I_L = 2A (5)		1.80		3.2 4.9	V V
V_{sens}	Sensing Voltage (pins 1, 15)			–1 (1)		2	V

LEMBAR PERSETUJUAN

PERANCANGAN DAN PEMBUATAN SISTEM RUANGAN MULTIFUNGSI BERBASIS MIKROKONTROLLER AT89S51

SKRIPSI

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disusun oleh :
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FAKULTAS TEKNOLOGI INDUSTRI
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PERANCANGAN DAN PEMBUATAN SISTEM RUANGAN MULTIFUNGSI BERBASIS MIKROKONTROLLER AT89S51

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ABSTRAK

Perkembangan teknologi terutama di bidang elektronika mengalami kemajuan yang pesat Di dunia elektronika ada yang dikenal dengan mikrokontroller.Ada beberapa jenis mikrokontroller salah satunya adalah jenis ATMEL tipe AT89S51. Kerena mikrokontroller jenis ini memiliki keistimewaan dan kesederhanaan di dalamnya,untuk merancang dan membuat alat pengontrol suatu benda dengan menggunakan remote sebagai pengendali.Penulis mencoba mengembangkan ide untuk membuat alat yang diaplikasikan pada ruangan Tv agar bisa menjadikan ruangan multifungsi,tidak lepas dari merubah interior dan menambahkan beberapa fasilitas agar memberikan kesan canggih dan unik. Seperti merubah interior Tv menjadi ruang kerja,membuka dan menutup korden menyalakan dan mematikan lampu secara otomatis yang di control dengan remote dan terahir sebagai tambahan di berikan juga pendeteksi asap rokok untuk kebersihan udara dalam ruangan.

Kata kunci:Mikrokontroller,Motor Dc,Relay dan Sensor Asap.

KATA PENGANTAR

Dengan memanjatkan puji syukur kehadirat Allah SWT, atas limpahan Rahmat dan Hidayah-Nya, sehingga penyusun dapat menyelesaikan skripsi ini dengan judul :

"PERANCANGAN DAN PEMBUATAN SISTEM RUANGAN MULTIFUNGSI BERBASIS MIKROKONTROLLER AT89S51"

Skripsi ini disusun sebagai salah satu persyaratan dalam menyelesaikan studi program strata satu (S-1) Jurusan Teknik Elektro/Konsentrasi Teknik Elektronika, Fakultas Teknologi Industri, Institut Teknologi Nasional Malang.

Sebelum dan selama penyusunan skripsi ini, penyusun telah banyak mendapatkan bantuan dan bimbingan dari berbagai pihak. Untuk itu pada kesempatan ini penyusun menyampaikan terima kasih yang sebesar-besarnya kepada:

1. Bapak Dr. Ir. Abraham Lomi, MSEE, selaku Rektor Institut Teknologi Nasional Malang
2. Bapak Ir. H. Sidik Noercahyono, MT, selaku Dekan Fakultas Teknologi Industri, Institut Teknologi Nasional Malang
3. Bapak Ir. F. Yudi Limpraptono, MT, selaku Ketua Jurusan Teknik Elektro S-1 Institut Teknologi Nasional Malang
4. Bapak Ir. Yusuf Ismail Nakoda, MT, selaku Sekretaris Jurusan Teknik Elektro S-1 Konsentrasi Elektronika Institut Teknologi Nasional Malang
5. Bapak Joseph Deddy Irawan, ST, MT, selaku Dosen Pembimbing atas segala bimbingan, pengertian, dan waktu untuk penulis

6. Seluruh Dosen pengajar di Jurusan Teknik Elektronika atas segala ilmu, pengetahuan, dan pengalaman yang telah diberikan dan diajarkan
7. Teman-teman angkatan 2003 atas dukungan moril, bantuan, dan saran-saran
8. Semua pihak yang terlibat langsung maupun tidak langsung yang telah membantu terwujudnya skripsi ini.

Akhirnya penulis tidak lupa mohon maaf yang sebesar-besarnya bila dalam penulisan skripsi ini masih terdapat kesalahan baik sengaja maupun tidak disengaja. Dan akhirnya semoga skripsi ini dapat bermanfaat bagi semua pihak.

Malang, September 2009

Penulis

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BAB I

PENDAHULUAN

1.1 Latar Belakang

Di dalam perkembangannya, mikrokontroller banyak diterapkan dalam perancangan elektronika karena mikrokontroller memiliki sistem pengaturan dan pengontrolan yang otomatis dan praktis. Keefektifan mikrokontroller inilah yang diperlukan manusia dalam menunjang rutinitas, baik dalam proses produksi maupun dalam kehidupan sehari – hari pada umumnya. Seperti.memanfaatkan ilmu elektronika pada ruangan yang mana ruangan ini di jadikan ruangan multifungsi, dengan pengubahan interior Tv menjadi ruang kerja berbasis mikrokontroller AT89S51 dengan spesifikasi interior – interior didalam ruangan untuk mendukung ruangan multifungsi ini menjadi layak tanpa merubah suatu konstruksi bangunan.

Penggunaan remote kontrol sendiri berfungsi agar sang pemilik tidak perlu mondar – mandir dalam menjalankan fungsi dari masing – masing interior yang dimilikinya. Hanya menekan tombol yang ada pada remote kontrol semua dapat dilakukan dari manapun juga bahkan dari tempat duduk sekalipun.

Dengan semakin pesatnya perkembangan teknologi saat ini, hal itu sangat mungkin dilakukan. Dengan memanfaatkan remote kontrol IR dan module IR yang digunakan sebagai inputan dari rangkaian mikrokontroller AT89S51. outputan dari rangkaian mikrokontroller ini kemudian diteruskan untuk mengatur sistem kerja dari masing – masing fungsi

Sedangkan untuk mencegah terjadinya penumpukan asap pada ruangan maka digunakan sesor asap yang berfungsi untuk mendeteksi asap rokok yang kemudian asap

tersebut akan dihisap oleh fan keluar ruangan.tentunya ada setpoin penumpukan asap yang sudah ditentukan,setelah itu fan akan bekerja untuk menghisap.

1.2 Rumusan Masalah

Dalam perancangan dan pembuatan sistem ruangan multi fungsi berbasis mikrokontrooler AT89S51. Maka permasalahanya adalah bagaimana membuat suatu alat yang dapat merubah suatu ruangan single menjadi ruangan multifungsi secara otomatis atau terkontrol.

1. Bagaimana merancang dan membuat rangkaian yang menunjang dalam sistem ini.
2. Bagaimana merancang dan membuat perangkat lunak atau *software* pada mikrokontroler yang mengendalikan semua kerja sistem.
3. Bagaimana merancang,memperhitungkan konstruksi bangunan dan ruangan.

1.3 Tujuan

Adapun tujuan dari pembuatan alat ini adalah untuk mengubah ruangan single menjadi ruangan multifungsi (mengubah ruangan TV menjadi ruangan kerja dengan cara kerjanya berputar) yang dilengkapi dengan fasilitas-fasiltas dan kenyamanannya.

1.4 Batasan Masalah.

Agar pembahasan dari perancangan dan pembuatan system ruangan multifungsi berbasis mikrokontroller AT89S51 ini tidak terlalu meluas maka penyusun perlu membuat batasan-batasan masalah yang meliputi :

1. Tidak membahas konstursi bangunan.
2. Tidak membahas motor yang di gunakan secara lengkap.
3. Tidak membahas interior Tv.

1.5 Metodologi Penulisan

Metodologi penulisan yang dipakai dalam pembuatan skripsi ini adalah:

1. Study literatur
2. Perancangan dan Pembuatan alat
3. Pelaksanaan uji coba alat
4. Analisa Software dan Hardware
5. Penyusunan laporan skripsi.

1.6 Sistematika Penulisan

Penulisan skripsi ini terbagi menjadi lima bab dengan sistematika penulisan sebagai berikut:

BAB I PENDAHULUAN

Berisi latar belakang, tujuan, permasalahan, batasan masalah, metodologi, dan sistematika penulisan.

BAB II TEORI PENUNJANG

Membahas teori–teori dasar penunjang perancangan dan pembuatan alat.

BAB III PERANCANGAN DAN PEMBUATAN ALAT

Membahas tentang perancangan alat baik perangkat keras maupun perangkat lunak dan cara kerja blok diagram.

BAB IV PENGUJIAN ALAT

Mencakup pembahasan tentang proses pengujian alat yang terdiri dari peralatan yang digunakan, langkah kerja, dan analisa hasil pengujian.

BAB V PENUTUP

Berisi kesimpulan dan saran.

BAB II

DASAR TEORI

2.2. Minimum Sistem AT89S51

2.2.1. Mikrokontroler AT89S51

Perbedaan mendasar antara mikrokontroller dan mikroprosesor adalah mikrokontroler selain memiliki CPU juga dilengkapi memori dan *input output* yang merupakan kelengkapan sebagai sistem minimum mikrokomputer sehingga sebuah mikrokontroller dapat dikatakan sebagai mikrokomputer dalam keping tunggal *(Single Chip Microcomputer)* yang dapat berdiri sendiri.

Mikrokontroller AT89S51 adalah mikrokontroler ATMEL yang kompatibel penuh dengan mikrokontroler keluarga MCS – 51, membutuhkan daya rendah, memiliki performance yang tinggi dan merupakan *microcomputer* 8 bit yang dilengkapi 4Kbyte EEPROM *(Electrical Erasable and Programmable Read Only Memory)* dan 128 *Byte* RAM *internal*. Program memori yang dapat diprogram ulang dalam sistem atau menggunakan programmer *Nonvolatile* memori konvensional. Dalam sistem mikrokontroler terdapat dua hal yang mendasar, yaitu: perangkat lunak dan perangkat keras yang keduanya saling terkait dan mendukung.

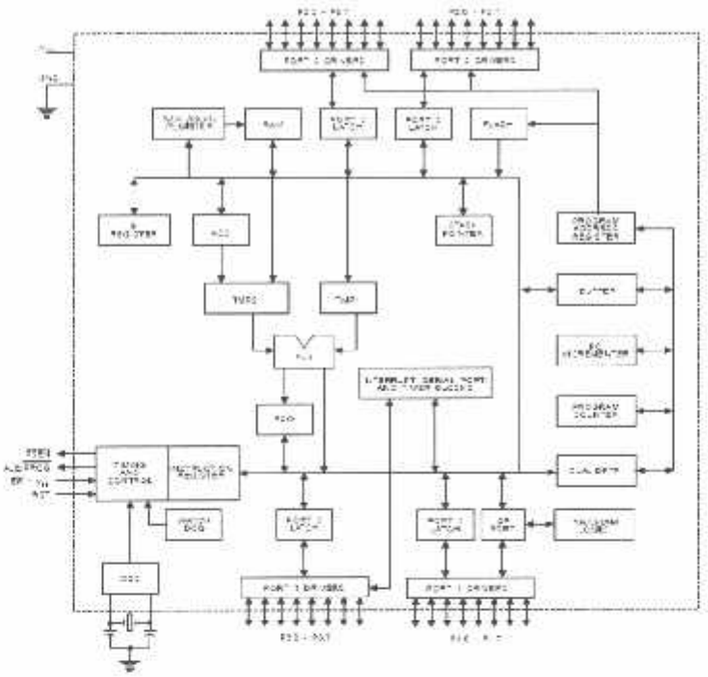
2.2.2.Perangkat keras mikrokontroler AT89S51

Secara umum Mikrokontroller AT89S51 memiliki :

- CPU 8 bit termasuk keluarga MCS-51

- 4 Kb *Flash* memory
- 128 *byte Internal* RAM
- 4 bank register, masing – masing berisi 8 register.
- 16 byte yang dapat dialamati pada bit level.
- 80 byte *general purpose memory data.*
- 32 buah Port I/O, tersusun atas P0 – P3, masing – masing 8 bit.
- 2 *Timer/ counter* 16 bit
- 2 *Serial Port Full Duplex*
- Kecepatan pelaksanaan intruksi per siklus 1 us pada frekuensi clock 12 Mhz
- 2 DPTR (*Data Pointer*)
- *Watchdog Timer*
- Fleksibel ISP Programming

Dengan keistimewaan Di atas pembuatan alat menggunakan AT89S51 menjadi lebih sederhana dan tidak memerlukan IC pendukung yang banyak. Adapun blok diagram dari Mikrokontroller AT89S51 adalah sebagai berikut :

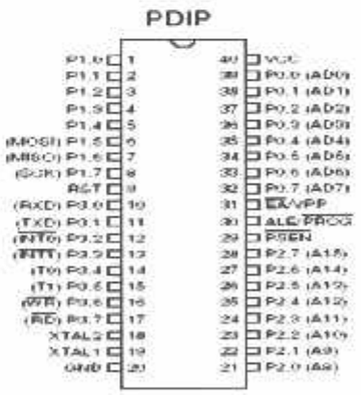


Gambar 2.1 Diagram Blok Mikrokontroller AT89S51

Sumber : Data Sheet Atmel AT89S51, halaman 3

2.2.3. Konfigurasi Pin Mikrokontroller AT89S51

Mikrokontroller AT89S51 terdiri dari 40 pin dengan konfigurasi sebagai berikut :



Gambar 2.2 IC AT89S51

Sumber : Data Sheet Atmel AT89S51, halaman 2

Fungsi tiap pin-nya adalah sebagai berikut :

1. Pin 1 sampai 8, **Port 1**

   Merupakan 8 bit I/O Bi-directional yang dilengkapi dengan internal Pull - Up. Ketika diberikan logika '1' pin ini akan di *Pull-Up* secara *internal* sehingga dapat digunakan sebagai *input*. Sebagai masukan jika pin – pin ini dihubungkan ke ground maka masing – masing pin ini dapat menghantarkan arus karena di *Pull-High* secara internal. Port 1 juga menerima *Low Order Address Bytes* selama melakukan verifikasi program.

   Pada *port* 1 di AT89S51 pin ini mempunyai alternatif seperti pada tabel berikut ini:

Tabel 2.1 Fungsi – Fungsi Alternative Port 1

Sumber : Data Sheet Atmel AT89S51,halaman 4

Port Pin	**Alternative Functions**
P1.5	MOSI (Master Output Sleve Input)
P1.6	MISO ((Master Input Sleve Output)
P1.7	SCK (Serial Clock)

2. Pin 9, **RST (*Reset*)**

Merupakan pin yang aktif tinggi (*high*), pin ini aktif tinggi selama dua siklus mesin yang akan membuat mikrokontroler AT 89S51 menjalankan rutin *reset*.

3. Pin 10 sampai 17, **Port 3**

Port 3 sebagai 8 bit I/O Bi-directional yang dilengkapi dengan *Pull-Up Internal*. Penyangga keluaran port 3 dapat memberikan atau menyerap arus empat masukan TTL (sekitar 1,6 mA). Jika diberikan logika '1' pada pin - pin port 3, maka masing – masing pin akan di *Pull High* oleh *Pull-Up internal* sehingga dapat digunakan sebagai *input*-an. Sebagai inputan, jika pin – pin port 3 dihubungkan ke *ground*, maka masing – masing kaki akan memberikan arus karena di *Pull High* secara internal, dimana Port 3 juga mempunyai fungsi-fungsi khusus yang dimiliki oleh keluarga MCS-51. Fungsi tersebut dapat dilihat dalam berikut ini :

Tabel 2.2 Fungsi Khusus Pada Port 3

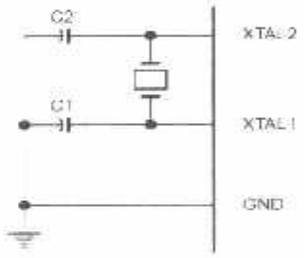
Sumber : Data Sheet Atmel AT89S51, halaman 5

Nama Penyemat	**Fungsi Khusus**
Port 3.0	RxD (port masukan serial)
Port 3.1	TxD (port keluaran serial)
Port 3.2	/INT0 (masukan interupsi eksternal 0)
Port 3.3	/INT1 (masukan interupsi eksternal 1)
Port 3.4	T0 (masukan pewaktu eksternal 0)

Port 3.5	T1	(masukan pewaktu eksternal 1)
Port 3.6	/WR	(sinyal tulis memori data eksternal)
Port 3.7	/RD	(sinyal baca memori data eksternal)

4. Pin 18 sampai 19, ***X-TAL 1 dan X-TAL 2***

   X-TAL 1 merupakan masukan ke rangkaian osilator *internal* sedangkan X-TAL 2 keluaran dari rangkaian osilator *internal*. Untuk keperluan ini diperlukan kapasitor penstabil sebesar 30pF. Dan nilai dari X-TAL tersebut antara 3 – 33 Mhz. Untuk lebih jelasnya dapat dilihat gambar pemasangan X-TAL serta kapasitor yang digunakannya.



Gambar 2.3 Osilator Eksternal AT89S51

5. Pin 20, **GND (*Ground*)**

   Dihubungkan dangan *ground* rangkaian.

6. Pin 21 sampai 28, **Port 2**

   Port 2 berfungsi sebagai 8 bit I/O Bi-directional yang dilengkapi dengan internal *Pull-Up* Penyangga keluaran port 2 dapat memberikan atau menyerap arus empat masukan TTL (sekitar 1,6 mA) Jika diberikan logika '1' pada pin – pin port 2, maka masing – masing pin akan di *Pull High*

secara *internal* sehingga dapat digunakan sebagai *input*-an. Sebagai *input*-an jika pin – pin port 2 dihubungkan ke *ground* (di *Pull-Low*), maka, masing – masing pin dapat menghantarkan arus karena di *Pull High* secara *internal*. Port 2 mengeluarkan alamat bagian tinggi (A8-A15), selama pengambilan instruksi dari memori program eksternal dan selama pengaksesan memori data eksternal yang menggunakan perintah dengan alamat 16-bit (dengan perintah "MOVX @DPTR").

7. Pin 29, **$\overline{\text{PSEN}}$ (*Program Store Enable*)**

   Pin ini aktif rendah yang merupakan *strobe* pembacaan ke program memori eksternal.

8. Pin 30, **ALE (*Address Latch Enable*) / *$\overline{\text{PROG}}$***

   Keluaran ALE menghasilkan pulsa – pulsa untuk menahan alamat rendah (A0-A7) pada port 0, selama dilakukan proses baca atau tulis memori *external*. Pin ini juga berfungsi sebagai masukan pulsa program (*PROG*) selama pemrograman EEPROM *external*. Pada operasi normal, ALE akan berpulsa dengan laju 1/6 dari frekuensi kristal dan dapat digunakan sebagai pewaktuan atau pendetakan (*clocking*).

9. Pin 31, ***$\overline{\text{EA}}$* / VPP (*External Access*)**

   Dapat diberikan logika rendah (*ground*) atau logika tinggi (+5V). Jika diberikan logika tinggi maka mikrokontroller akan mengakses program dari ROM *internal* (EEPROM/*Flash Memori*), dan jika diberikan logika rendah maka mikrokontroler akan mengakses program dari memori *external* yang berlokasi 0000h sampai FFFFh.

10. Pin 32 sampai 32, **Port 0**

Port 0 terdiri dari 8 saluran *input* atau *output* dua arah, tanpa internal *pull-up*. Port 0 merupakan bus alamat rendah ($A_0 - A_7$), yang dimultipleks dengan saluran bus data (D0-D7), yang digunakan pada saat mengakses memori data *external* dan memori program *external*.

11. Pin 40,**VCC**

Merupakan masukan catu daya 5 volt dengan toleransi kurang lebih 10%.

2.2.4. Organisasi Memori

Organisasi yang dimiliki oleh AT89S51 yang terdiri atas :

1. RAM Internal

Memori sebesar 128 *byte* yang biasanya digunakan untuk menyimpan variabel atau data yang bersifat sementara. RAM *internal* terdiri atas :

- ***Register Banks***

AT89S51 mempunyai delapan buah register yang terdiri atas R0 hingga R7. Kedelapan register ini selalu terletak pada alamat 00H hingga 07H pada setiap kali sistem direset. Namun posisi R0 hingga R7 dapat dipindah ke bank 1 (08 H hingga 0FH), bank 2 (10H hingga 17H) dan bank 3 (18H hingga 1FH), dengan mengatur bit RS0 dan RS1.

- ***Bit Addressable*** RAM

RAM pada alamat 20H hingga 2FH dapat diakses secara pengalamatan *bit* (*bit addressable*) sehingga hanya dengan sebuah

instruksi saja setiap *bit* dalam arca ini dapat *diset, clear, AND, OR.*

- **RAM keperluan umum**

RAM keperluan umum dimulai dari alamat 30H hingga 7FH dan dapat diakses dengan pengalamatan langsung maupun tak langsung. Pengalamatan langsung dilakukan ketika salah satu *operand* merupakan bilangan yang menunjukkan lokasi yang dialamati.

2. Special Function Register

Register fungsi khusus (*Special Function Register*) terletak pada 128 *byte* bagian atas memori data internal dan berisi *register-register* untuk pelayanan *latch port, timer, program status words, control peripheral* dan sebagainya. Alamat register fungsi khusus ditunjukkan pada Tabel 2-3.

Register-register ini hanya dapat diakses dengan pengalamatan langsung. Enam belas alamat pada register fungsi khusus dapat dialamati per*bit* maupun per-*byte* dan terletak pada alamat 80_H-FF_H. Secara perangkat keras, register fungsi khusus ini dibedakan dengan memori data internal.

Tabel 2.3 Special Function Register

Sumber : Hafindo *Elektronic & Education,* Malang, 2001

Simbol	**Nama Register**	**Nilai Pada Saat Reset**	**Alamat**
ACC	Accumulator	00_H	$E0_H$

B	Register B	00_H	$F0_H$
PSW	Program Status Word	00_H	$D0_H$
SP	Stack Pointer	07_H	81_H
DPTR	Data Pointer 2 Byte		
DPL	Bit rendah	0000_H	82_H
DPH	Bit Tinggi	0000_H	83_H
P0	Port 0	$0FF_H$	80_H
P1	Port 1	$0FF_H$	90_H
P2	Port 2	$0FF_H$	$A0_H$
P3	Port 3	$0FF_H$	$B0_H$
IP	Interupt Periority Control	$XXX00000_B$	$D8_H$
IE	Interupt Enable Control	$0XX00000_B$	$A8_H$
TMOD	Timer/Counter Mode	00_H	89_H
TCON	Control	00_H	88_H
TH0	Timer/Counter Control	00_H	$8C_H$
TL0	Timer/Counter 0 High	00_H	$8A_H$
TH1	Control	00_H	$8D_H$
TL1	Timer/Counter 0 Low	00_H	$8B_H$
SCON	Control	00_H	98_H
SBUF	Timer/Counter 1 High	Independen	99_H
PCON	Control		87_H
	Timer/Counter 1 Low		
	Control		

	Serial Control Serial Data Buffer Power Control		

Beberapa macam register fungsi khusus yang sering digunakan adalah sebagai berikut ini :

- *Accumulator* (ACC) merupakan register untuk penambahan dan pengurangan. Perintah *mnemonic* untuk mengakses akumulator disederhanakan sebagai A.
- Register B merupakan register khusus yang berfungsi melayani operasi perkalian dan pembagian.
- *Program Status Word* (PSW) yang terletak pada alamat D0H terdiri dari beberapa *bit* status yang menggambarkan kejadian di akumulator sebelumnya. Yaitu *carry bit*, *auxiliary carry*, dua *bit* pemilih bank, bendera *overflow*, *parity bit*, dan dua bendera yang dapat didefinisikan sendiri oleh pemakai. Keterangannya sebagai berikut :

▪ Flag Carry

Flag Carry (terletak pada alamat D7H) mempunyai fungsi sebagai pendeteksi terjadinya kelebihan pada operasi penjumlahan atau terjadi pinjam (*borrow*) pada operasi pengurangan. Misalnya jika data pada accumulator adalah FFH dan dijumlahkan dengan bilangan satu atau lebih, akan terjadi kelebihan dan membuat carry menjadi Set, sedangkan jika

data pada accumulator adalah 00H dan dikurangkan dengan bilanagan satu atau lebih, akan terjadi pemimjaman dan membuat carry juga menjadi set.

- Flag Auxilary Carry

  Flag Auxilary Carry akan selalu Set pada saat proses penjumlahan terjadi carry dari bit ketiga hingga bit keempat.

- Flag 0

  Flag 0 digunakan untuk tujuan umum bergantung pada kebutuhan pemakai.

- Bit Pemilih Register Bank

  Register Bank Select Bits (RS0 dan RS1) atau Bit Pemilih Register Bank digunakan untuk menentukan lokasi dari Register Bank (R0 hingga R7) pada memori. RS0 dan RS1 selalu bernilai nol setiap kali system direset sehingga lokasi dari R0 hingga R7 akan berada di alamat 00H hingga 07H.

- Flag Overflow

  Flag Overflow akan diset jika pada operasi aritmatik menghasilkan bilangan yang lebih besar dari pada 128 atau lebih kecil dari – 128.

- Bit Pariti

  Bit Pariti akan diset jika jumlah bit 1 dalam accumulator adalah ganjil dan akan clear jika jumlah bit 1 dalam accumulator genap. Jika data dalam accumulator adalah 10101110b atau AEH pariti akan diset. Data AEH mempunyai lima bit yang berkondisi 1 atau dapat disebut mempunyai bit 1

dalam jumlah yang ganjil. Bit pariti ini digunakan untuk proses yang berhubungan dengan serial port yaitu sebagai *Check sum*.

- *Stack Pointer* (SP) merupakan register 8 bit yang dapat diletakkan di alamat manapun pada RAM *internal*. Isi *register* ini ditambah sebelum data disimpan, selama instruksi PUSH dan CALL. Pada saat *reset*, *register* SP diinisialisasi pada alamat 07_H, sehingga *stack* akan dimulai pada lokasi 08_H.
- *Data Pointer* (DPTR) terdiri dari dua register, yaitu untuk *byte* tinggi (*Data Pointer High*, DPH) dan byte rendah (*Data Pointer Low*, DPL) yang berfungsi untuk pengalamatan alamat 16 bit.
- Port 0 sampai Port 3 merupakan register yang berfungsi untuk membaca dan mengeluarkan data pada port 0, 1, 2, 3. Masing-masing register ini dapat dialamati per-*byte* maupun per-*bit*.
- *Serial data buffer* (SBUF) merupakan dua *register* yang terpisah, *register buffer* pengirim dan sebuah *register buffer* penerima. Meletakkan data pada SBUF berarti meletakkan pada *buffer* pengirim yang akan mengirimkan data melalui transmisi serial. Membaca data SBUF berarti menerima data dari *buffer* penerima
- *Control Register* terdiri dari register yang mempunyai fungsi kontrol. Untuk mengontrol sistem interupsi, terdapat dua register khusus, yaitu *register* IP (*Interupt Priority*) dan *register* IE (*Interupt Enable*). Untuk mengontrol pelayanan *timer/counter* terdapat *register* khusus, yaitu

register TCON (*timer/counter control*) serta pelayanan port serial menggunakan register SCON (*Serial Port Control*).

- Register Timer

  AT89S51 mempunyai dua buah 16 bit Timer/Counter, yaitu Timer 0 dan Timer 1. Timer 0 terletak pada alamat 8AH untuk TL0 dan 8CH untuk TH0 dan Timer 1 terletak pada alamat 8BH untuk TL1 dan 8DH untuk TH1.

- Register Interupt

  89S51 mempunyai lima buah interupsi dengan sua level prioritas interupsi. Interupsi akan selalu nonaktif setiap kali system di – reset. Register – register yang berhubungan dengan interrupt adalah *Interrupt Enable Register* (IE) atau Register Pengaktif Interupsi pada alamat A8H untuk mengatur keaktifan tiap – tiap interrupt dan Interrupt Priority Register (IP) atau Register Prioritas Interupsi pada alamat B8H.

- Register Port Serial

  AT89S51 mempunyai sebuah *on chip serial port* (serial port dalam keping) yang dapat digunakan untuk berkomunikasi dengan peralatan lain yang menggunakan serial port juga seperti modem, shift register dan lain – lain.

  Buffer (Penyangga) untuk proses pengiriman maupun pengambilan data terletak pada register SBUF, yaitu pada alamat 99H. Sedangkan untuk

mengatur mode serial dapat dilakukan dengan mengubah isi dari SCON yang terletak pada alamat 98H.

3. Flash PEROM

AT89S51 memiliki 4Kb *Flash* PEROM (*Programmable and Erassable Read Only Memori*), yaitu ROM yang dapat ditulis ulang atau dihapus menggunakan sebuah perangkat programmer hingga 1000 kali. Program yang ada pada *Flash* PEROM akan dijalankan jika pada saat sistem di-*reset*, pin EA/VP berlogika satu sehingga mikrokontroler aktif berdasarkan program yang ada pada *flash* PEROMnya. Namun, jika EA/VP berlogika nol, mikrokontroller aktif berdasarkan program yang berada pada memori *external*.

2.2.5. Mode Pengalamatan.

Mode pengalamatan yang digunakan pada AT89S51 adalah sebagai berikut:

a) Mode pengalamatan segera (*immediate addressing mode)*.

Cara ini menggunakan konstanta, misalnya: **MOV A, #20H.** Data konstanta merupakan data yang menyatu dengan instruksi, contoh instruksi tersebut diatas mempunyai arti bahwa data konstantanya yaitu 20H, (sebagai data konstanta harus diawali dengan '#') disalin ke akumulator A.

b) Mode pengalamatan langsung (*direct addressing mode*).

Cara ini dipakai untuk menunjuk data yang berada di suatu lokasi memori dengan cara menyebut lokasi (alamat) memori tempat data

tersebut berada, misalnya: **MOV A, 30H.** Instruksi ini mempunyai arti bahwa data yang berada di dalam memori dengan lokasi 30h disalin ke akumulator. Bedanya dengan pengalamatan segera yaitu jika pada pengalamatan segera menggunakan tanda '#' yang menandai 20H sebagai data konstan, sedangkan pada instruksi ini tidak menggunakan '#' sehingga 30H diartikan sebagai suatu lokasi memori.

c) Mode pengalamatan tidak langsung (*indirect addressing mode*).

Cara ini dipakai untuk mengakses data yang berada di dalam memori, tetapi lokasi memori tidak disebut secara langsung tapi di-'titip'-kan ke register lain, misalnya: **MOV A, @R0.** R0 adalah register serba guna yang dipakai untuk menyimpan lokasi memori, sehingga instruksi ini mempunyai arti memori yang alamat lokasinya tersimpan dalam R0 isinya disalin ke akumulator A. Tanda '@' dipakai untuk menandai lokasi memori yang tersimpan di dalam R0. *Register* serba guna R0 berfungsi sebagai register penyimpan alamat (*indirect address*), selain R0 register serba guna lainnya, R1 juga bisa dipakai sebagai register penampung alamat.

d) Mode pengalamatan register (*register addressing mode*).

Misalnya: **MOV A, R5** ,instruksi ini mempunyai arti bahwa data dalam register serba guna R5 disalin ke akumulator A. Instruksi ini menjadikan register serba guna R0 sampai R7 sebagai tempat penyimpanan data yang praktis dan kerjanya sangat cepat.

e) Mode pengalamatan kode tidak langsung (*code indirect addressing mode*).

MCS51 mempunyai cara penyebutan data dalam memori program yang dilakukan secara tak langsung, misalnya: **MOVC A, @A+DPTR.** Instruksi MOV diganti dengan MOVC, tambahan huruf C tersebut dimaksud untuk membedakan bahwa instruksi ini digunakan untuk memori program (MOV tanpa huruf C artinya digunakan untuk memori data). Tanda '@' digunakan untuk menandai A+DPTR yang berfungsi untuk menyatakan lokasi memori yang isinya disalin ke Akumulator A, dalam hal ini nilai yang tersimpan dalam DPTR (*Data Pointer Register* – 2 byte) ditambah dengan nilai yang tersimpan dalam akumulator A (1 byte) sama dengan lokasi memori program yang diakses.

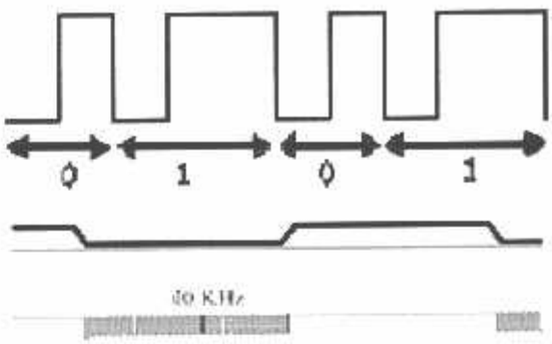
2.3. Remote

Berfungsi sebagai Sebagai pengontrol. Dan Remote yang di gunakan Remote dengan format data Sony yang mempunyai panjang data sebanyak 12 bit. Sinyal control inilah yang nantinya akan menjadi masukan untuk unit pemproses AT89S51. Penerima sinyal Remote menggunakan IR receiver pabrikasi yang telah berfungsi untuk menerima sinyal dengan frekwensi sinyal Remote Tv Sony yaitu 40 KHz.

Tabel 2.4 Data Remote Sony

Tombol	Hexa	Tombol	Hexa
1	#080	Vol-	#093
2	#081	Power(toggle)	#095
3	#082	PIC Mode	#096
4	#083	A/B	#097
5	#084	TV/Video	#0A5
6	#085	Sleep	#0B6
7	#086	+	#0F4
8	#087	-	#0F5
9	#088	Select	#0FC
0	#089		
Prog+	#090		
Prog-	#091		
Vol+	#092		

Dimana data yang untuk di gunakan untuk menembak oleh modul ini adalah sama dengan penekanan tombol "1" pada remote sony. Pengguna dapat mencoba dengan menembakan tombol "1" pada sensor. Oleh karna itu data yang harus dimodulasikan oleh modul adalah data 80h. Data tersebut di kirim secara serial dalam bentuk pulse code modulation dimana logika 0 di wakili oleh logika 0 dan logika 1 yang pendek sedangkan logika 0 diwakili oleh logika 0 panjang dan logika 1 untuk yang pendek seperti pada gambar 2-3 berikut:



Gambar 2.4 Bentuk Sinyal Remote Tv Sony

Namun sinyal PCM ini tidk dapat di kirimkan langsung ke LED infrared melainkan terlebih dahulu melalui proses modulasi dengan sinyal carrier 40 KHz sehingga tampak seperti pada gambar di atas logika 0 dari hasil PCM akan diubah menjadi sinyal 40 KHz dan logika 1 diubah jadi logika 1 biasa.

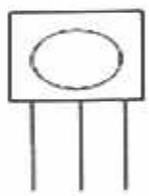
2.4.IRM (Infra Red Receiver Module)

Inframerah Receiver Module yang lebih dikenal dengan modul infra merah, menerima gelombang infra merah dengan panjang gelombang $10^{-3} - 10^{-6}$ m dan frekwensi sebesar $10^{11} - 10^{14}$ Hz, dengan frekwensi carrier 38 40 Khz.

Proses penerimaan pada prinsipnya sama dengan proses fotodioda dan sudah terintegrasi bersama satu komponen IC, dimana pada fotodioda terdapat suatu jendela kecil yang memungkinkan cahaya luar dapat masuk dan mengenai PN junction. Pada keadaan normal fotodioda berlaku sebagai dioda biasa yang dapat menghantarkan arus listrik dari anoda ke katoda, namun mempunyai tahanan balik yang besar. Bila cahaya luar mengenai junction fotodioda, maka tahanan balik

akan mengecil dan menimbulkan arus balik, sehingga fotodioda berlaku sebagai dioda yang balik atau dibias reverse.

Semakin besar intensitas cahaya yang diterima, maka semakin besar pula arus balik yang ditimbulkannya. Bila energi foton diserap dalam suatu semikonduktor, maka akan dihasilkan pasangan elektron-elektron dan hole-hole yang telah dibangkitkan oleh foton yang saling memisahkan diri karena pengaruh medan listrik. Dimana elektron-elektron akan menuju sisi N dan hole-hole menuju ke sisi P, sehingga dihasilkan arus dari katoda menuju anoda. Arus balik yang dihasilkan sebanding dengan sinar yang diserap. Karena pengaruh suhu junction yang lebih tinggi menciptakan lebih banyak pasangan elektron-hole, sehingga mengakibatkan aliran arus balik yang melewati junction bertambah.



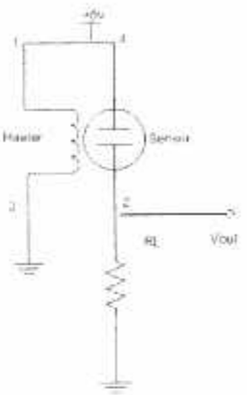
Gambar 2.5 Simbol Infra Red Receiver Modul (IRM)

2.5.Limit switch Max – Min

Limit switch ini adalah suatu komponen detector manual atau panic switch, Komponen ini merupakan yang paling sederhana sekali dimana dalam memperoleh respon dariluar sangat mudah dan hanya mempunyai dua posisi yaitu NO (normaly open) jika hanya dalam posisi normal artinya tidak ada respon dari luar dia akan mempunyai kondisi terbuka (off), dan jika NC (normaly close) adalah dalam posisi normal dia akan terkondisi (on).

2.6. Sensor Asap Rokok AF 30

Berfungsi sebagai Pendeteksi asap rokok dalam ruangan. Sensor asap AF30 memiliki sensisifitas tinggi atau kepekaan yang tinggi dan rangkaian yang simple seperti pada gambar berikut:



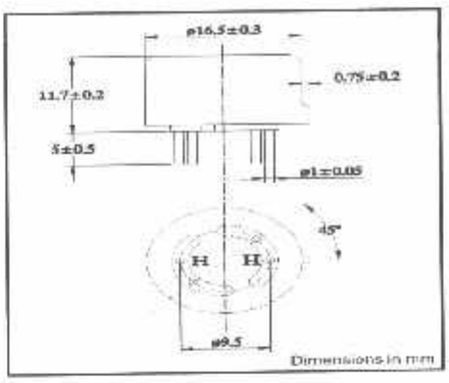
Gambar 2.6 Rangkaian Sensor AF30

Deskripsi :

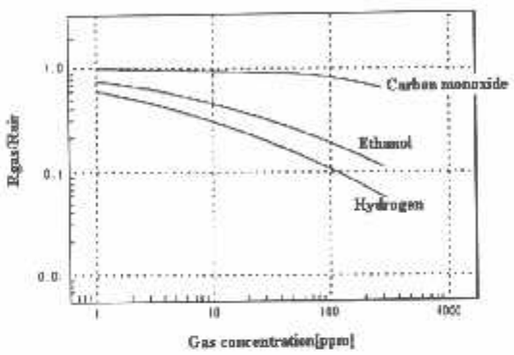
- Sensor gas ini terbuat dari element film yang tebal.

Kelebihan :

- Konstant Heater Voltage.
- Tahanan Yang Kecil.
- Sensivitas yang Tinggi.
- Dengan Type aplikasi sebagai pembersih udara.
- Bekerja pada temperatur -10 ~ +55°C.
- Pada circuit VC bekerja pada voltage 5V Dc.
- Tahanan Heater 27 Ohm.
- Resistor RL Variabel.



Gambar 2.7 Dimensi Dan Configurasi Pin



Gambar 2.8 Grafik kerja pembacaan sensor

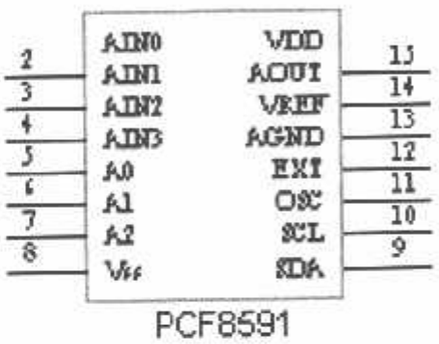
2.7. PCF8591

PCF8591 adalah suatu chip tunggal buatan philip semikonduktor,dengan empat inputan analog data 8 bit CMOS dengan power supplay rendah, satu out putan analog dan suatu serial penghubung I2C bus. Tiga empat pin A0,A1 dan A2 di gunakan untuk memprogram perangkat keras (hard ware). Dan pada perencanaan ini Ic PCF8591 digunakan sebagai ADC untuk sensor AF30. Adapun bagian spesifikasinya berikut:

- Serial I/O via I2C bus.
- Terdapat 3 pin alamat dari hard ware.

- Inputanya Diffrensial.
- Analog input 4 chanel 8 bit.
- Analog output 1 chanel 8 bit.
- Input range tegangan 0V – 2,5V.

Adapun gambar dari Ic PCF5891 seperti pada gambar berikut :

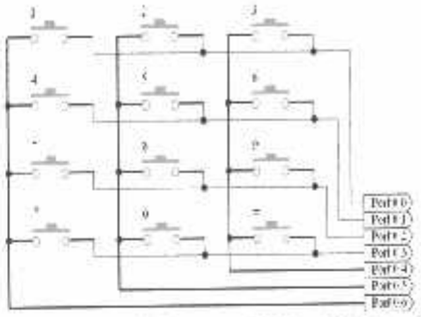


Gambar 2.8 Pin PCF8951

2.8. Keypad

Keypad merupakan salah satu sarana untuk memasukkan suatu data ke komputer atau minimum sistem. Untuk rangkaian keypad dalam tugas ahkir ini digunakan keypad matrik 4 x 3.

Keypad matrik 4 x 3 merupakan susunan 12 tombol membentuk keypad sebagai sarana masukan ke mikrokontroller, meskipun jumlah tombol ada 12 tapi hanya memerlukan 7 jalur port pararel, seperti terlihat dalam Gambar 2-8 berikut:



Gambar 2.9 Keypad Matrik 4 x 3

2.9. LCD *(Liquid Cristal Display)*

Liquid Cristal Display adalah modul tampilan yang mempunyai konsumsi daya yang relatif rendah dan terdapat sebuah kontroler CMOS didalamnya. Kontroler tersebut berfungsi sebagai pembangkit ROM / RAM dan *display* data RAM. Semua fungsi tampilan dikontrol oleh suatu instruksi, modul LCD dapat dengan mudah di*interface*kan dengan MPU.

LCD yang digunakan dalam skripsi ini adalah LCD yang memiliki kemampuan sebagai berikut:

- Meliputi 32 karakter yang dibagi menjadi 2 baris dengan *display dot matrik* 5 x 7 ditambah *cursor*.
- Karakter generator ROM dengan 192 karakter.
- Karakter generator RAM dengan 8 tipe karakter.
- Dilengkapi fungsi tambahan yaitu *display clear, cursor home, display ON/OFF, cursor ON/OFF, display character blink, cursor shift* dan *display shift*.
- Internal data.

- 80 x 8 *bit display* data RAM.
- Dapat diinterfacekan dengan µC 8 atau 4 *bit*.
- Internal otomatis dan *reset* pada *power ON*.
- + 5 volt *power supply* tunggal.

Gambar 2.10 Bentuk fisik dari LCD (Liquid Cristal Display)

2.10. Motor DC

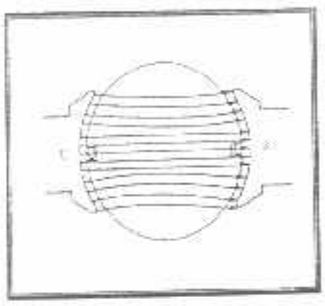
Motor arus searah (DC) adalah suatu mesin yang berfungsi mengubah energi listrik menjadi energi mekanik. Dasar prinsip kerja motor DC sebenarnya sangat mudah, hanya saja kita sering dibingungkan dengan konstruksi mesin yang agak rumit.

2.10.1. Prinsip kerja Motor DC Satu Arah

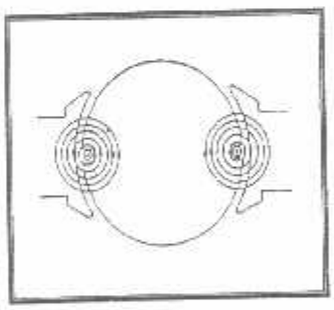
Prinsip kerja motor arus searah didasarkan pada penghantar yang membawa arus ditempatkan dalam suatu medan magnet, maka penghantar tersebut akan mengalami gaya. Gaya menimbulkan torsi yang menimbulkan torsi yang

menghasilkan rotasi mekanik, schingga motor akan berputar. Dalam sistematika kerjanya bisa disimpulkan sebagai berikut:

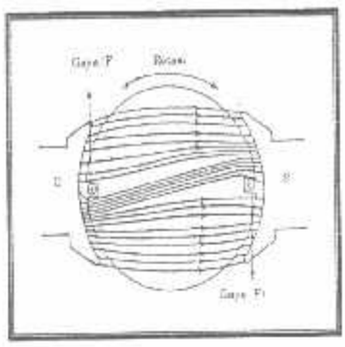
1. Adanya garis – garis gaya medan magnet (fluks) anatara kutub yang berada di stator
2. Penghantar dialiri arus ditempatkan pada jangkar dalam medan magnet
3. Pada penghantar timbul gaya yang menghasilkan torsi



Gambar 2.11 Medan yang dihasilkan oleh kutub



Gambar 2.12 Medan sebagai hasil arus yang mengalir pada penghantar



Gambar 2.13 Interaksi kedua medan menghasilkan gaya

Gambar di atas yaitu Terjadinya rotasi motor arus searah sebagai interaksi antara medan magnet yang dihasilkan oleh kutub pada stator dan medan magnet yang dihasilkan oleh arus yang mengalir pada penghantar.

Persamaan yang mendasari prinsip kerja motor DC :

1. Persamaan gaya pada kawat berarus listrik dalam medan magnet.

   $$F = i\,(l \times B)$$

   dimana :

   F = gaya pada kawat

   I = arus yang mengalir pada kawat

   L = panjang kawat

   B = medan magnet

2. Persamaan tegangan induksi pada kawat berarus listrik yang bergerak dalam medan magnet

   $$e_{ind} = (v \times B)\,l$$

   dimana

   e_{ind} = tegangan induksi pada kawat

   v = kecepatan putar kawat

B = vector medan magnet

L = panjang konduktor dalam medan magnet

3. Hukum tegangan Kirchoff

$$V_b - iR - e_{ind} = 0$$

$$V_b = e_{ind} + iR$$

Pada proses kerja motor DC, keempat persamaan tersebut saling terkait dan berkesinambungan. Proses kerja dapat disimpulkan sebagai berikut :

1. Penutup saklar (memberi tegangan) menghasilkan aliran listrik

   $I = V_B / R$

2. Mengalirnya arus menghasilkan gaya pada lilitan kawat $F = Bil$

3. Lilitan kawat bergerak kesamping (kanan), menghasilkan tegangan induksi yang berimbas pada kecepatan

4. Tegangan induksi menaikan arus $i = (V_B - e_{ind}) / R$

5. Gaya induksi menurun ($F = i l B$) , sampai mendekati $F = 0$. Pada keadaan tersebut, $e_{ind} = V_B$, $i = 0$, dan lilitan berputar konstan dengan kecepatan tanpa beban $V_{SS} = V_B / B l$

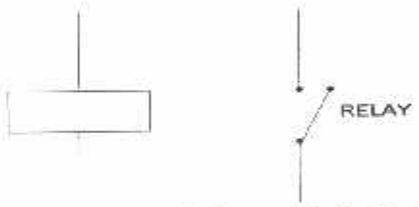
2.11. RELAY

Relay adalah suatu perangkat switch yang dioperasikan gaya elektromaknetik (magnet permanen) atau di sebut juga komponen elektromekanis.

Relay biasanya digunakan untuk pensaklaran khusus (misalnya pemutusan daya dengan remotc). Keuntungan dari pemakaian relay umumnya terletak pada pengaturan switching daya / tegangan tinggi, dengan catu daya rendah sehingga terdapat isolasi antara catu daya relay yang relative rendah dengan catu beban yang tinggi yang akan di putus sambungkan. Kerugian relay umumnya terjadi efek 'bouncing' dan tanggapan waktu (respon time) saat on tau off yang relative lebih lambat, kontroksi relay :

Semua relay elektromaknetik terdapat tiga bagian utama, yaitu :

a. Koil magnet (Kumparan penggerak magnetisasi)
b. Hubungan dari kumparan transformasi keterminal keluaran (out put)
c. Perubahan kondisi saklar (on atau off), selama kumparan berenergi.



Gambar 2.14 Dasar Kerja Relay

Bagian kontak relay dapat dipakai sebagai :

a.Pole (kutub utama)

b.Trow (Kutub Pelepasan)

c.Posisi Normal (Normally Open atau Normally Closed).

Misalnya sebuah relay dengan parameter SPST (Singgle Pole Singgel Throw), NO, (Normally Open), DM (Double Male), artinya : relay dengan 1

induk 1 anak, pada keadaan normalnya terbuka (OFF), dengan kontak penyambungan ganda. Klasifikasi Relay :

Relay di kelompokan dalam tiga bagian menurut pemakaian dan kegunaannya, Yaitu :

1. Pemakaian umum : (General Purpose), contoh : Relay AC, relay DC
2. Pemakaian khusus : (Specific Puspose), contoh : DLL relay.
3. Pemakian Terbatas : (Define Purpose), contoh : reed relay, kontaktor.

Sedangkan menurut kemampuan yang spesifik, relay dapat di kelompokkan sebagai berikut:

a. Margina : Kemampuan yang baik dalam mengambil atau melepasmkan arus listrik (Pick up and drop –out carrent).

b. Timing : Kemampuan dalam waktu pelepasan kontak (release time), waktu perlambatan (delay time), dan waktu lainya.

c. Sensitivity : Kemampuan dalam sensitifitas (kepekaan) dalam mengambil atau melepas arus listrik pada operasi normal.

d. Latching : Kemampuan dalam urutan perioda switctingnya.

e. Sequencing : Kemampuan dalam urutan perioda switctingnya.

f. Frequency sensitivity : Kepekaan perioda frekwensikerja relay (Khususnya relay AC).

g. Thermal Response : Kemampuan akan temperaturnya akan kerja dari kumparan saat operasi.

BAB III

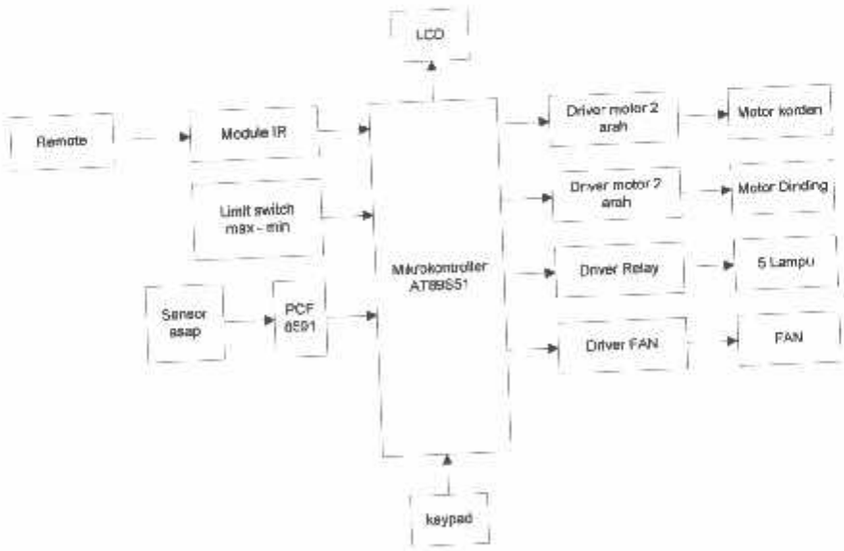
PERANCANGAN HARDWARE DAN SOFTWARE

Bab ini akan membahas tentang perencanaan dan perancangan alat yang meliputi perencanaan perangkat keras (Hardware) dan perangkat lunak (Software) dari sistem pengaturan kerja motor untuk dinding Interoir Tv dan Meja kerja, Buka dan tutup korden. Pengaturan sistem kerja sensor asap dan Pengaturan Hidup matinya lima lampu dalam ruangan. Perancangan secara keseluruhan dapat dibagi menjadi dua bagian, yaitu :

1. Perancangan Hardware
2. Perancangan Software

3.1 PERANCANGAN HARDWARE

Blok diagram sistem sebagai berikut :



Gambar 3.1 Diagram Blok Sistem

Dari gambar blok diagram 3.1 dapat dijelaskan cara kerjanya secara umum

Komponen - komponen dan Fasilitas pada blok diagram secara kesluruhan dapat di kontrol dengan remote dan sebagian Fasilitas dapat diatur secara manual.

Dan fungsi dari masing – blok sebagai berikut:

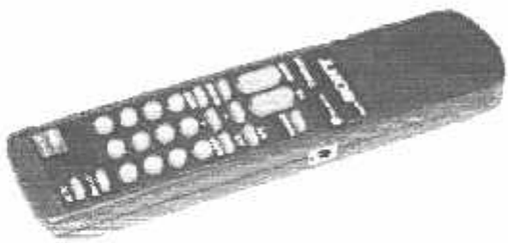
1. Remote sebagai pengontrol atau pengirim intruksi dengan menggunakan remote Tv sony.
2. Module IR rangkaian penerima intruksi dari remote untuk menjalankan system atau perintah pada tiap – tiap fasilitas sesuai dengan perintah yang di terima.
3. Limit Switch Max-Min sebagai pengatur motor pengerak pada motor dinding dan motor korden jelasnya untuk pembatasan pergerakan motor kapan harus bekerja dan berhenti.
4. Sensor Asap AF30 digunakan sebagai pendeteksi adanya asap dalam ruangan.
5. PCF 8591 digunakan untuk mengubah tegangan analog menjadi tegangan digital sebagai inputan dari sensor asap AF30 untuk proses penerimaan pada Mikrokontroller.
6. Keypad digunakan untuk tombol pengaturan intruksi dan seting point batas pendeteksian ketebalan asap dalam ruangan yang di terima dari sensor asap AF30 untuk menjalankan proses kerja FAN sebagai penganti blower.

7. Liquid Crystal Display (LCD) digunakan untuk menampilkan data yang telah diproses oleh mikrokontroler AT89S51 dan intruksi dari Keypad.
8. Driver Motor Dua Arah sebuah rangkaian penggerak motor satu arah di jadikan duarah putar searah jarum jam dan kebalikan arah jarum jam dengan system kerja rangkain ini membalikan polaritas.
9. Motor Korden digunakan sebagai pengerak korden,dengan cara kerjanya buka tutup korden.
10. Motor Pemutar Dinding Interior Tv menjadi Ruang kerja, putaran roda pada motor mengerakan dinding Interior Tv dan Meja Kerja dalam satu dinding yang saling membelakangi berputar berputar dengan menapak pada lantai.
11. Driver Relay suatu rangkaian pengatur proses kerja relay.
12. Relay suatu perangkat switch yang dioprasikan gaya elektromagnetik, pada blok system ini relay digunakan untuk pensaklaran khusus mematikan dan menghidupkan lampu menggunakan remote.
13. Lampu digunakan untuk penerangan ruangan yang melanjutkan proses ahir dari driver relay yang di intruksikan dari remote.
14. Driver Fan berfungsi sebagai rangkaian pengatur kerja fan untuk menghisap, apabila terdeteksi adanya asap dalam ruangan.
15. Fan digunakan untuk menghisap asap dalam ruangan yang bekerja setelah melalui proses dari driver fan dan intruksi dari proses awal pendeteksian sensor asap.

16. Mikrokontroler AT89S51 digunakan sebagai pengolah data hasil pembacaan dari intruksi yang diterima kemudian dikirimkan pada tiap – tiap blok sesuai intruksi yang diterima.

3.2. Perencanaan Penggunaan Remote Tv Sony Triniton 827 s.

Dalam perencanaan alat ini mengunakan remote Tv Sony Triniton 827 s karena remote Tv Sony lebih mudah untuk mendukung kebutuhan alat ini. Pada perencanaan ini membutuhkan beberapa tombol untuk mengendalikan fitur – fitur alat sesuai kebutuhan, demikian gambar remote Tv sony:



Gambar 3.2 Remote Tv Sony

Tabel 3.1 Fungsi Tombol Remote

TOMBOL	FUNGSI TOMBOL
1	Lampu On 1
2	Lampu On 2
3	Lampu On 3
4	Lampu On 4
5	Lampu On 5
6	Lampu Off 1
7	Lampu Off 2

8	Lampu Off 3
9	Lampu Off 4
0	Lampu Off 5
+ Prog	Buka Korden
- Prog	Tutup Korden
+ Vol	Putar Ruang Meja Kerja
- Vol	Tutup Ruang Meja Kerja
1-	Lampu Semua On
2-	Lampu Semua Off

Dari perencanaan penggunaan remoto Tv Sony demikian setingan tombol – tombol yang akan dipergunakan, untuk mengendalikan fitur – fitur yang ada pada alat tanpa harus mengendalikan secara manual.cukuc dengan jarak jauh.

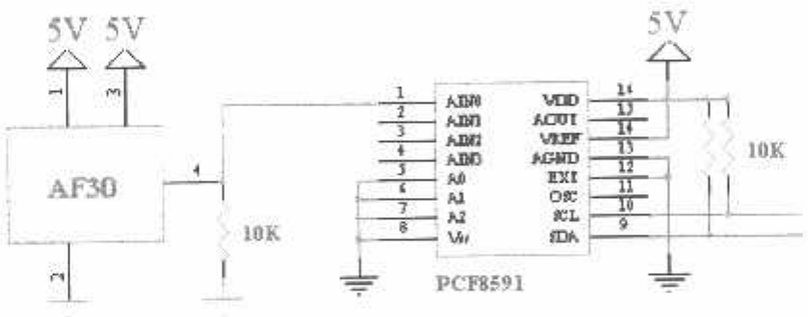
3.3. Perencanaan Rangkaian Sensor Asap AF30 Dan IC PCF 8591 Sebagai ADC (Analog to Digital Converter)

Sensor asap tipe AF30 pada perancangan alat ini berfungsi untuk pendeteksi adanya asap rokok yang tujuaanya agar menjaga kebersihan udara dalam ruangan apabila pengguna merokok dalam ruangan tidak terjadi pemenuhan asap rokok dalam ruangan. Karena terdeteksi oleh sensor AF30 berupa tegangan Analog.

Dan pada perancangan rangkaian sensor ini dibutuhkan ADC (Analog to Digital Converter) untuk pengolahan data pada Mikrokontroler AT89S51 maka

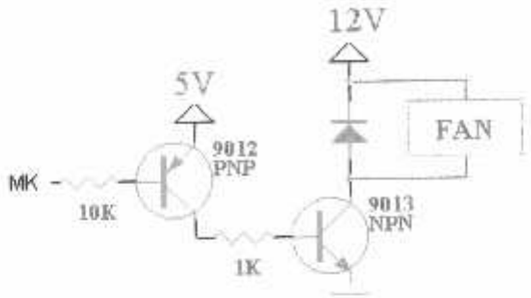
digunakan Ic PCF8591 yang memiliki empat inputan analog data 8 bit CMOS satu chanel outputan analog 8 bit dengan power suplay rendah dan suatu serial penghubung I2C bus. Sensor asap AF30 memiliki 4 pin, pin 1 dan 3 diberi tegangan inputan 5V pin 2 terhubung dengan ground dan pin 4 diberi tahanan luar 10K kemudian dihubungkan pada pin input Ic PCF8591.

Pembacaan intruksi yang di terima sensor dan di proses oleh ADC kemudian dilanjutkan oleh Mikrokontroler AT89S51. dari gambar Ic PCF8591 kaki keluaran yang diberi tahanan luar dari pin VDD masing – masing 10K, Vref dan VDD diberi tegangan 5V kemudian dihubungkan pada Mikrokontroler pada pin 16-17. dan rangkaian dari sensor AF30 dan ADC Ic PCF8591 seperti pada gambar berikut :



Gambar 3.3 Rangkaian Sensor Asap AF30 Dan ADC

Dalam mikrokontroler data yang diterima lalu diolah untuk dilajutkan oleh rangkaian Fan (Driver Fan) untuk menjalankan Fan agar berputar menghisap asap dalam ruangan. pada rangkaian menggunakan Transistor 9012 PNP dan 9013 NPN dua tahanan 10K dan 1K kemudian dioda 1A untuk pengaman apabila ada arus balik. Demikian gambar perencanaan rangkaian driver Fan:



Gambar 3.4 Driver Fan

Rangkaian driver fan ini sama dengan rangkaian pendukung lainnya untuk menghubungkan fan dengan mikrokontroller yang di hubungkan dengan port2 pada mikrokontroller.

Mencari I dari R yang telah ditentukan pada driver fan :

Dik :

Rb1 = 10 kΩ

Rb2 – 1 kΩ

Tr1 PNP 9012 (Hfe -70)

Tr2 NPN 9013(Hfe -70)

Vbe (saturasi) = 60 (data sheet)

$$Ib1 = \frac{V - V_{be\ saturasi}}{Rb1}$$

$$= \frac{5 - 0{,}7}{10\ k\Omega}$$

$$= 0{,}43mA$$

Ic1 = Ib1 . Hfe

= 0,43 . 60(data sheet)

= 25,8mA

$$Ib2 = \frac{V - V_{be\ saturasi}}{Rb2}$$

$$= \frac{5 - 0{,}7}{1\ k\Omega}$$

– 4,3mA

Ic2 = Ib2 . Hfe

= 4,3 . 60(data sheet)

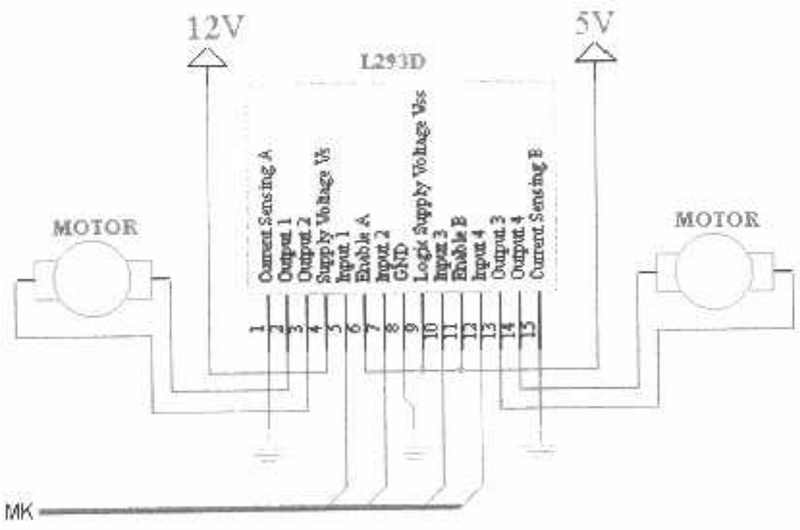
= 258m

3.4. Perencanaan Driver Motor Dc

Untuk motor Dc satu arah memiliki prinsip dasar dengan mengubah energi listrik menjadi energi mekanik, sesuai kebutuhan alat ini mengunakan motor Dc dua arah maka dari itu di rancang sebuah rangkaian untuk membalikan polaritas agar motor Dc dapat berputat searah jarum jam dan berlawanan arah jarum jam dengan ini rangkaian mengunakan Ic L298 untuk merubah system kerja motor Dc.

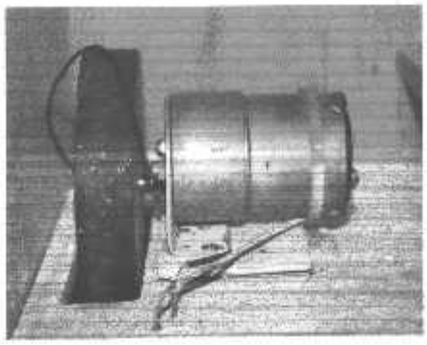
Pada rangkaian driver motor Dc port Vs diberi tegangan masukan 12V untuk port Anable A-B dan Vss Tegangan masukanya 5V Port Input 1-4 pada Ic L298 dihubungkan pada mikrokontroler. Dan port output 1-4 dihubungkan untuk motor pemutar dinding Interior Tv dan meja kerja yang menapak pada lantai, dan Untuk motor pengerak buka tutup korden.

Untuk jelasnya tiap – tiap port Ic L298 dapat dilihat pada skema driver motor Dc pada gambar berikut :

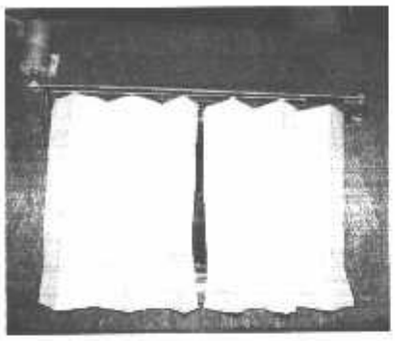


Gambar 3.5 Driver Motor Dc

Demikian gambar perencanaan motor dc untuk pemutar dinding :



Gambar 3.6 Motor Pemutar Dinding



Gambar 3.7 Motor Pengerak Korden

Demikian karakteristik Ic L298 :

1.operasi tegangan hingga 46v

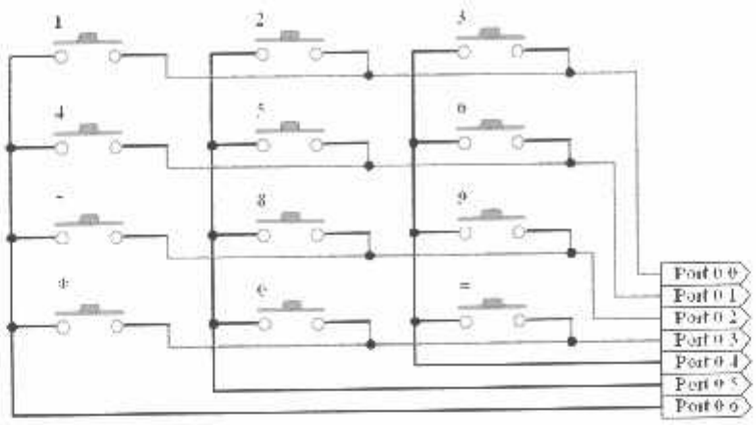
2.total current DC hingga 4A

3.overtempcratur proteksi

4.logic"0" input hingga 1,5v (high nois immunity)

3.5. Perencanaan Rangkaian Keypad 3x4

Untuk memasukkan data pada Mikrokontroler AT89S51 keypad. Keypad matrik 4x3 merupakan susunan 12 tombol membentuk keypad sebagai sarana masukan ke Mikrokontroler, meskipun jumblah tombol ada 12 tapi hanya memerlukan 7 jalur port pararel, seperti pada gambar berikut :

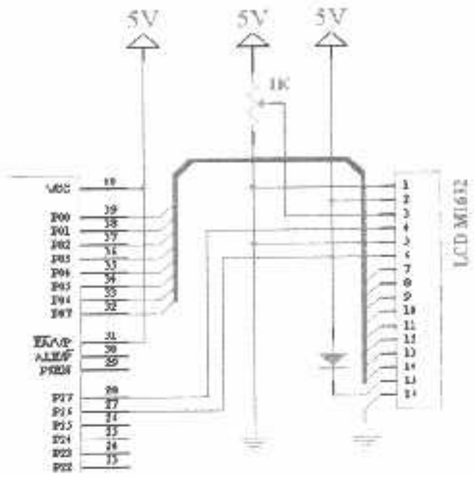


Gambar 3.8 Keypad Matrix 3 x 4

Dari gambar di atas dapat diperoleh 12 kemungkinan output dapat ditentukan fungsi dari setiap tombol. Keluaran data dari penekanan tombol dihubungkan langsung pada Mikrokontroler AT89S51 untuk pilihan pengaturan seting point pada keypad tombol (*) digunakan sebagai tombol cancel, (#) digunakan untuk tombol menu atau enter untuk seting point dan ADC. Kemudian tombol (1,2,3,4,5,6,7,8,9,0) tetap untuk memasukan nilai atau angka.

3.6. Perencanaan LCD (Liquid Crystal Display)

Untuk menampilkan semua intruksi dari keypad, maka dalam perencanaan ini digunakan LCD M1632 karena LCD adalah modul tampilan yang mempunyai konsumsi daya yang relative rendah dan terdapat sebuah kontroler CMOS didalamnya dan kontroler tersebut berfungsi sebagai pembangkit ROM/RAM dan display data RAM.karena fungsi tampilan dikontrol oleh suatu intruksi, agar modul LCD dapat dengan mudah di interfacekandengan MPU.dan perencanaan LCD seperti pada gambar berikut :



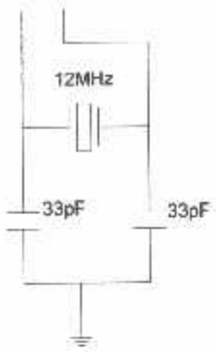
Gambar 3.9 LCD M1632

Pada gambar diatas kaki-kaki LCD M1632 yang terhubung dari port Mikrokontroler P0 – P7 ke kaki DB0 – DB7 pada LCD kemudian port 26 – 27 dari mikro terhubung dengan kaki Rs dan E pada LCD. Tambahan dioda external yang terhubung ke V-BL pada LCD dengan tegangan masukan 5V port V-BL dihubungkan ke ground kemudian kaki Vss dan RW diberikan tahanan eksternal 1K dengan tegangan masukan 5V.

3.7. Perencanaan Rangkaian Clock

Mikrokontroller AT89S51 membutuhkan sinyal clock untuk berpindah dari satu kondisi ke kondisi yang lain, sebab dalam perancangan perangkat lunaknya perpindahan dari satu state ke state yang lain dieksekusi jika ada clock.

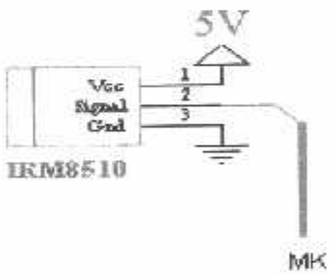
Perencanaan clock ini menggunakan Crystal 12MHz dua buah capasitor 33pF yang terhubung dengan kaki dari Crystal dan rangkaian ini dihubungkan ke kaki 18 – 19 pada Mikrokontroller. dalam perencanaan alat ini clock diprogram pada 12 KHz. rangkaian clok ini digunakan sebagai pemicunya. Dan rangkaian clock seperti pada gambar berikut :



Gambar 3.10 Rangkaian Clock

3.8. Perencanaan IRM (Infra Red Receiver Modul).

Untuk perancangan IRM digunakan IRM 8510 karena IRM dapat menerima panjang gelombang infra merah 10 – 10 m dan frekwensi sebesar 10 – 10 Hz, dengan frekwensi carrier 38 – 40 KHz. Karena proses pencrimaannya pada prinsipnya sama dengan proses fotodioda yang terintegrasi bersama satu komponen Ic. Perencanaan IRM dapat dilihat pada gambar berikut :



Gambar 3.11 IRM 8510

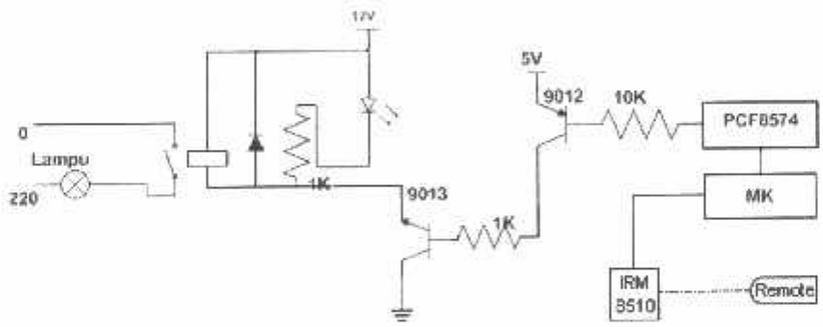
3.9. Perencanaan Rangkaian Driver Relay Menggunakan Ic PCF8574

Rangkaian ini merupakan rangkain tambahan untk mengontrol Relay karena terbatasnya port pada mikrokontroller sehingga dapat dihubungkan dengan mikrokontroller AT89S51.

Rangkaian ini mempunyai Spesifikasi sebagai nberikut:

1. Operating supply 2.5V to 6V
2. Low Standby current
3. I2C to parallel port
4. Open drain interrupt output
5. Kompotibel penuh terhadap mikrokontroller
6. Address by 3 hardware address pin

Dan rangkaian ini berfungsi untuk mengontrol nyala lampu dan mematikan lampu melalui Remote. Dan Rangkaian driver ini menggunakan Ic PCF 8574 yang terhubung ke mikrokontroller. Seperti pada gambar berikut:



Gambar 3.12 Rangkaian Driver Relay Menggunakan Ic PCF8574

Relay dihubungkan pada IC PCF8574 sebagai rangkaian tambahan karena kurangnya port mikrokontroller yang dihubungkan pada port 3.0 dan port 3.1.

Rb1 = 10 kΩ

Rb2 = 1 kΩ

Tr1 PNP 9012 (Hfe -70)

Tr2 NPN 9013(Hfe -70)

Vbe (saturasi) = 60 (data sheet)

Ib1 $= \frac{V - Vbe\ (saturasi)}{Rb1}$

$= \frac{5 - 0,7}{10\ k\Omega}$

= 0,43mA

Ic1 = Ib1 . Hfe

= 0,43 . 60(data sheet)

– 25,8mA

Ib2 $= \frac{V - Vbe\ (saturasi)}{Rb2}$

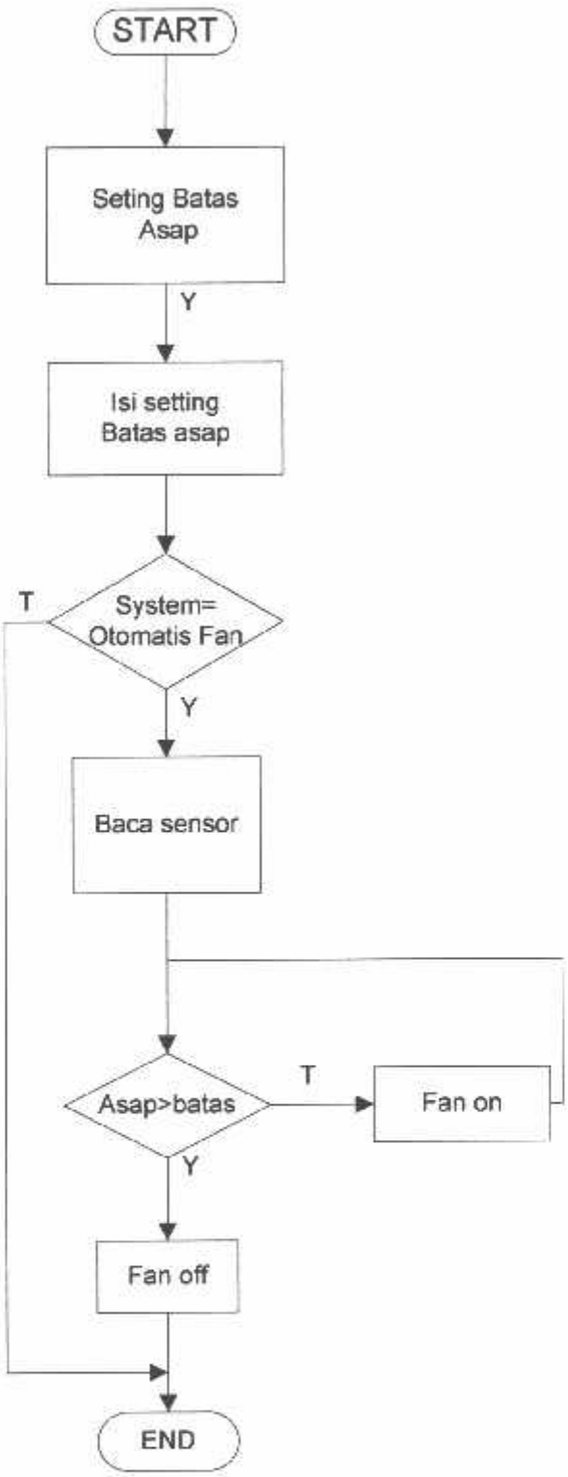
$= \frac{5 - 0,7}{1\ k\Omega}$

= 4,3mA

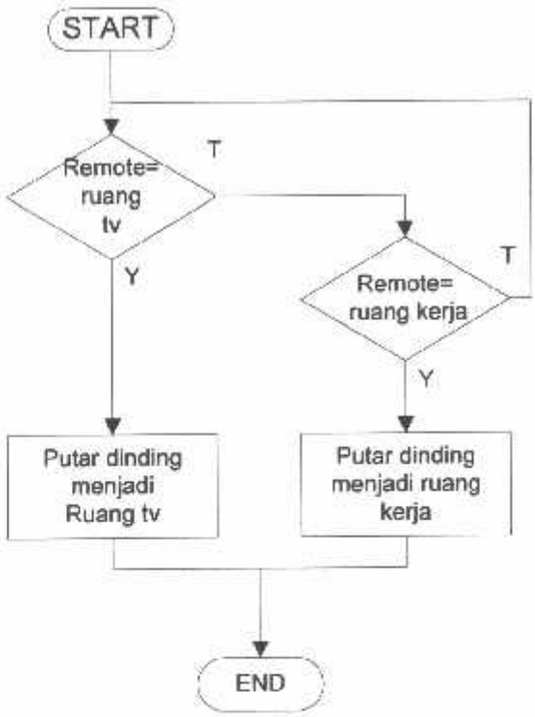
Ic2 = Ib2 . Hfe

= 4,3 . 60(data sheet)

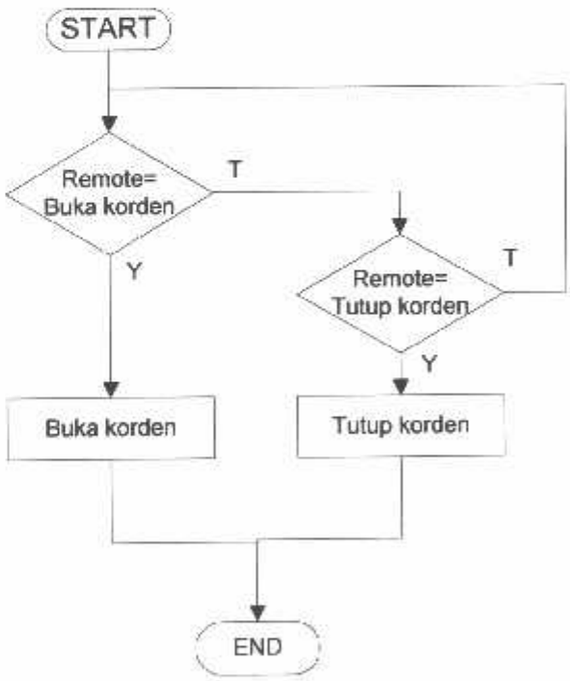
= 258mA



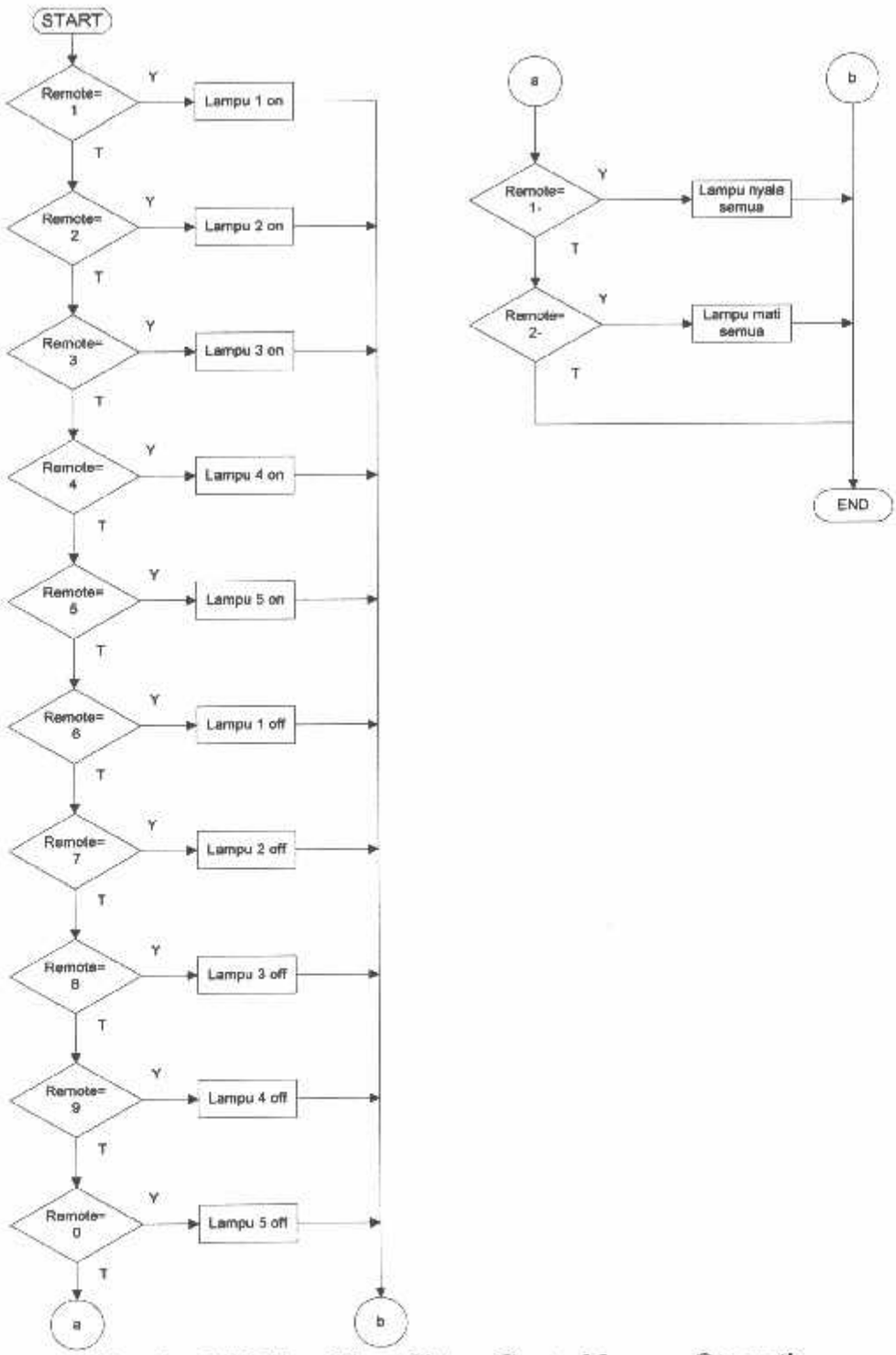
Gambar 3.13 Flowchart Sistem Sensor Asap AF30



Gambar 3.14 Flowchart system Putar Dinding Interior Tv dan Meja Kerja



Gambar 3.15 Flowchart Sistem Buka Tutup Korden



Gambar 3.16 Flow Chart Sistem Control Lampu Otomatis.

BAB IV

PENGUJIAN DAN ANALISA

Pada bab ini membahas cara pegujian dan analisa dari alat yang dirancang, sehingga dapat diketahui apakah alat tersebut dapat bekerja sesuai dengan yang telah direncanakan. Dalam rangka pengujian alat tersebut diuraikan percobaan yang dilakukan untuk mengetahui respon dari keseluruhan alat yang telah dirancang.

Untuk mengetahui kemampuan alat dan sistem kerja sesuai dengan program yang telah dibuat maka dilakukan pengujian pada alat dan sistem kerja alat dengan prosedur pengujian sebagai berikut:

1. Pengujian perangkat keras (Hardware)
2. Pengujian perangkat lunak (Software)

4.1. Pengujian Perangkat Keras

Tujuan pengujian yang dilakukan terhadap sistem adalah sebagai berikut:

1) Mengetahui unjuk kerja Sensor AF30 dan Ic PCF8591 sebagai ADC *(Analog To Digital Converter)* sampai dengan kerja Driver Fan.
2) Mengetahui unjuk kerja Driver Motor Dc.
3) Mengetahui unjuk IRM *(Infra Red Receiver Modul)*.
4) Mengetahui unjuk kerja Rangkaian Driver Relay Menggunakan Ic PCF8574.
5) Pengujian Mikrokontroller sebagai minimum system.

4.1.1. Pengujian Rangkaian kerja Sensor AF30 dan Ic PCF8591 sebagai ADC *(Analog To Digital Converter)* sampai dengan kerja Driver Fan.

1. Tujuan

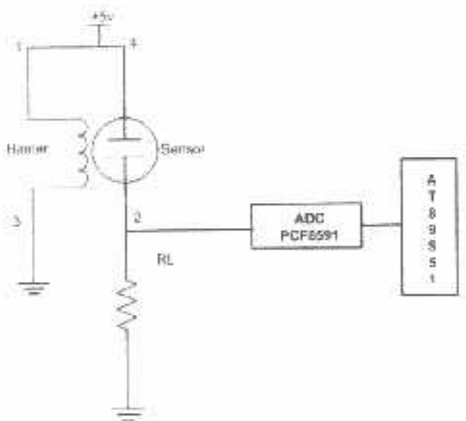
Untuk mengetahui besarnya tegangan output dari sensor Asap AF30 berdasarkan perubahan kebersihan udara pada ruangan saat mendeteksi adanya asap rokok dan diterima oleh ADC kemudian di lanjutkan oleh Fan.

2. Peralatan Yang Digunakan

1. Multimeter Digital Range RE830D.
2. Rangkaian yang akan diuji.
3. Catu Daya 5 Volt DC.
4. Asap rokok.

3. Prosedur Pengujian

1. Merangkai rangkaian seperti pada gambar dibawah ini:



Gambar 4.1 Pengujian Rangkaian Sensor Asap AF30 dan Ic PCF8591 sebagai ADC *(Analog To Digital Converter)*

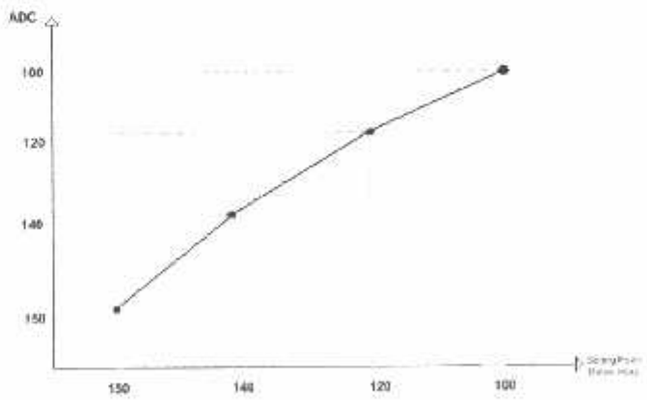
2. Menghubungkan IC PCF8591 dengan tegangan DC 5 Volt pada kaki untuk Vref
3. Menghubungkan kaki lainnya pada ground.
4. Menguji sensor dengan di beri asap rokok pada ruangan.
5. Analisa hasil pengujian.

Dari percobaan pendeteksian asap telah ditentukan setingan dalam program sesuai batas yang ditentukan, seperti pada tabel di bawah ini:

Tabel 4.1 Range Pendeteksian Sensor Af30

Seting Point Batas Asap	ADC	Keterangan
150	153	Low
140	142	Low
120	121	High
100	100	High

Pada range setingan batas asap diatas didapat grafik sebagai berikut:



Grafik 4.1 Pembacaan Pendeteksian Asap

Berdasarkan pengujian setingan batas asap dapat didefinisikan pada saat setingan batas asap rendah maka respon sensitifitas pembacaan asap semakin tinggi, dan jika setingan batas asap tinggi maka kepekaan pembacaan asap semakin low atau rendah.

4.1.2. Pengujian Rangkaian Driver Motor Dc.

1. Tujuan

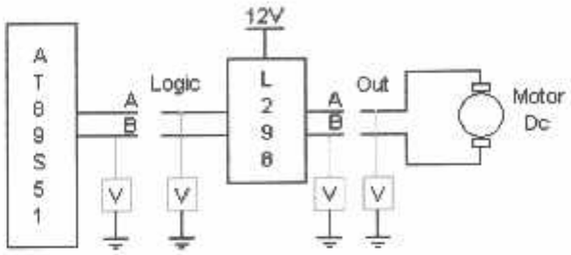
Pengujian ini bertujuan untuk mengetahui apakah driver motor DC dapat berfungsi dengan baik sebagai penggerak dan pembalik arah putaran dan untuk mengetahui kecepatan respon dari driver motor DC terhadap kecepatan perubahan arah putaran. Dalam pengujian ini hal yang perlu dilakukan adalah, pertama beritegangan 12Volt pada konektor rangkaian penggerak, pasangkan motor pada rangkaian driver dan beri tegangan 5Volt pada kaki yang akan dikoneksikan ke mikrokontroler sebagai pembalik arah putaran maupun sebagai PWM. Kemudian hubungkan ground sebagai logika '0' Bila logika '0' diberikan pada kaki PWM maka motor akan begerak dan bila logika '0' diberikan pada kaki pengubah arah putaran maka putaran motor akan berbalik.

2. Peralatan Yang Digunakan

1. Multimeter SUNWA YX-360TRD
2. Rangkaian driver motor Dc yang akan diuji.
3. Catu Daya 12 Volt DC dan 5 Volt.
4. Motor Dc.

3. Prosedur Pengujian

1. Merangkai rangkaian driver motor Dc seperti pada gambar di bawah ini:



Gambar 4.2 Pengujian Rangkaian Driver Motor Dc

Menghubungkan rangkaian driver motor Dc dengan tegangan DC 12 Volt untuk catu daya pada IC L293D untuk suplai tegangan,5 Volt untuk penyedia tegangan dan Vss.

2. Menghubungkan motor Dc untuk memutar dinding interior Tv dan meja kerja pada pin output1,2 kemudian untuk motor Dc pengerak buka tutup korden dihubungkan kc output 3,4 pada Ic L298.
3. Mengamati hasil pengukuran tegangan output rangkaian driver motor Dc.

Melakukan pengukuran output dari rangkaian driver motor Dc seperti pada tebel 4-2 berikut:

Tabel 4.2 Arah Putaran Motor DC

logic		V logic		V out		I		Ket
A	B	A	B	A	B	A	B	
0	0	0,04	0,03	0,06	0,05	0,01	0,00	Stop

0	1	0,03	4,70	0,05	11,55	0,02	154	Kiri
1	0	4,98	0,03	11,75	0,05	165	0,00	Kanan
1	1	4,98	4,70	11,75	11,55	165	154	Break

Analisa:

Dari tabel diatas dapat diketahui bahwa untuk membalik polaritas gerakan motor apabila logika A dan B diberikan logika '0' maka motor akan berhenti, kemudian logika A diberi logika '0' B diberi logika '1' maka motor akan berputar kekiri. Lalu logika A diberi logika '1' B diberi logika '0' maka motor akan berputar kekanan, dan jika logika A dan B diberi logika '1' maka kondisi motor akan berhenti.

4.1.3. Pengujian Penerima Intruksi Remote Tv Sony IRM8510

1. Tujuan

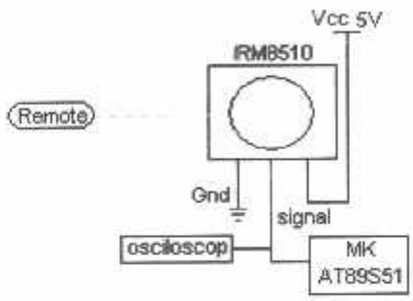
Tujuan dari pengujian remote ini adalah untuk mengetahui kerja keseluruhan tombol pada remote yang digunakan.

2. Peralatan Yang Digunakan

1. Rangkaian Driver IRM (Infra red receiver modul).
2. Catu Daya 5 Volt DC.
3. Remote Tv Sony.
4. Osciloscop.

3. Prosedur Pengujian

1. Merangkai rangkaian penerima intruksi Remote Tv Sony IRM8510 seperti pada gambar berikut:



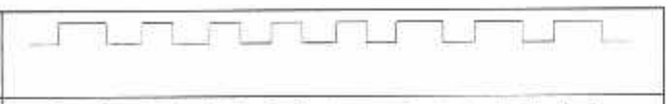
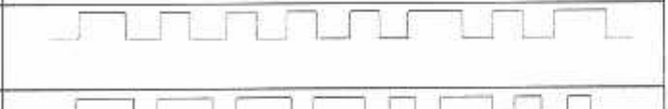
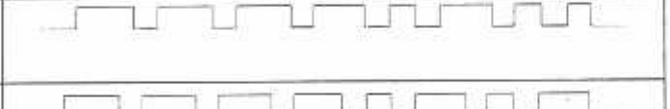
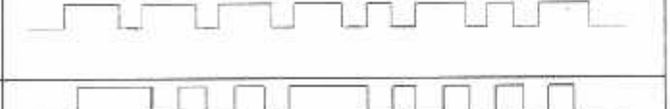
Gambar 4.3 Pengujian Rangkaian IRM8510

Kode yang dikembangkan oleh perusahaan SONY ini menggunakan frekuensi *sub-carrier* 40 kHz dan selang waktu minimum antara 2 data = 25 ms.

Demikian tabel Pengujian Rangkaian IRM8510:

Tabel 4.3 Pengujian Rangkaian IRM8510

Tombol	Hexa	Biner	Bentuk sinyal
1	#080	1000 0000	
2	#081	1000 0001	
3	#082	1000 0010	
4	#083	1000 0011	
5	#084	1000 0100	
6	#085	1000 0101	
7	#086	1000 0110	

8	#087	1000 0111	
9	#088	1000 1000	
0	#089	1000 1001	
1-	#0F4	1111 0100	
2-	#0F5	1111 0101	
+ Prog	#090	1001 0000	
- Prog	#091	1001 0001	
+ Vol	#092	1001 0010	
- Vol	#093	1001 0011	

Analisa pengujian remote membuktikan bahwa intruksi yang di kirimkan ke IRM8510 berupa bilangan hexa yang diterima oleh IRM dan diubah dalam bentuk pulsa untuk pembacaan pada mikrokontroler.seperti pada tabel pengujian diatas.

4.1.4. Pengujian Rangkaian Driver Relay

1. Tujuan

Untuk mengetahui apakah rangkaian Driver Relay dapat bekerja sesuai dengan yang diharapkan.

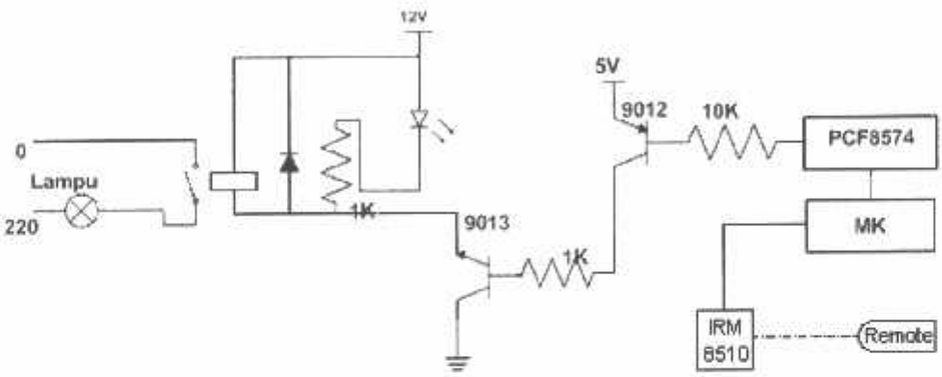
2. Peralatan Yang Digunakan.

1. Multimeter SUNWA YX-360TRD
2. Rangkaian driver yang akan diuji.

3. Catu Daya 5 Volt DC.
4. Relay 12 volt (8 pin Omron + Led).
5. 5 Buah Bolam 5 Watt.

3. Prosedur Pengujian

1. Merangkai rangkaian Driver Relay seperti pada gambar dibawah ini:



Gambar 4.4 Pengujian Rangkaian Driver Relay

2. Memberi tegangan masukan 5 Volt pada Ic PCF8574 Yang terhubung pada rangkaian Driver Relay.
4. Menghubungkan bolam pada relay dan diberi tegangan masukan untuk bolam 220 Volt.

Tabel 4.4 Pengujian Rangkaian Relay Sesuai Intruksi Dari Remote.

Tombol remote	Relay					Kondisi Lampu				
	1	2	3	4	5	1	2	3	4	5
1	1	*	*	*	*	1	*	*	*	*
2	*	1	*	*	*	*	1	*	*	*
3	*	*	1	*	*	*	*	1	*	*

4	*	*	*	1	*	*	*	*	1	*
5	*	*	*	*	1	*	*	*	*	1
6	0	*	*	*	*	0	*	*	*	*
7	*	0	*	*	*	*	0	*	*	*
8	*	*	0	*	*	*	*	0	*	*
9	*	*	*	0	*	*	*	*	0	*
0	*	*	*	*	0	*	*	*	*	0
1-	1	1	1	1	1	1	1	1	1	1
2-	0	0	0	0	0	0	0	0	0	0

Keterangan :

0 = Off

1 = On

* = Diabaikan

Analisa pada tabel pengujian rangkaian relay diatas membuktikan bahwa fungsi relay dari tiap – tiap rangkaian bekerja dengan baik sesuai dengan intruksi penekanan tombol pada remote, karena fungsi rangkaian relay ini hanya untuk pemicu saklar nyala dan matinya lampu secara terkontrol menggunakan remote.

4.1.5. Pengujian Fungsi *Limit Switch*

1. Tujuan

Tujuan dari pengujian ini adalah untuk mengetahui seberapa besar fungsi peranan *limit switch* dalam pengamanan proses kerja dari motor dc, dalam hal ini yang kita lihat pengaruhnya terhadap dua motor yang digunakan pada system ini. Pada system putar kanan-kiri dinding interior TV dan buka tutup korden ini mengunakan empat *limit switch* yang bersifat *normaly open* dan

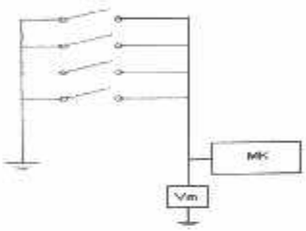
terletak pada tiap sisi, adapun cara pengujiannya dengan menjalankan alat setelah itu kita amati fungsi dari tiap – tiap *limit switch* yaitu dengan menekan satu persatu *limit switch.*

2. Peralatan yang digunakan

1. Rangkaian *Limit Switch* yang akan diuji.
2. 4 buah *Limit Switch*, 2 buah limit untuk lantai dan 2 buah limit untuk korden.

2. Prosedur Pengujian

1. Merangkai rangkaian *Limit Switch* seperti pada gambar dibawah ini:



Gambar 4.5 Pengujian Rangkaian *Limit Switch*

Dan dari hasil pengujian tersebut diperoleh data seperti pada table berikut :

logic		V Logic		Ket
A	B	A	B	
0	0	0,04	0,02	Min
0	1	0,03	4,74	kanan
1	0	4,73	0,04	kiri
1	1	4,75	4,73	Max

Tabel 4.5 Data Hasil Pengujian *Limit Switch*
Pada motor dinding

logic		V Logic		Ket
A	B	A	B	
0	0	0,04	0,02	Min
0	1	0,03	4,74	Buka
1	0	4,73	0,04	Tutup
1	1	4,75	4,73	Max

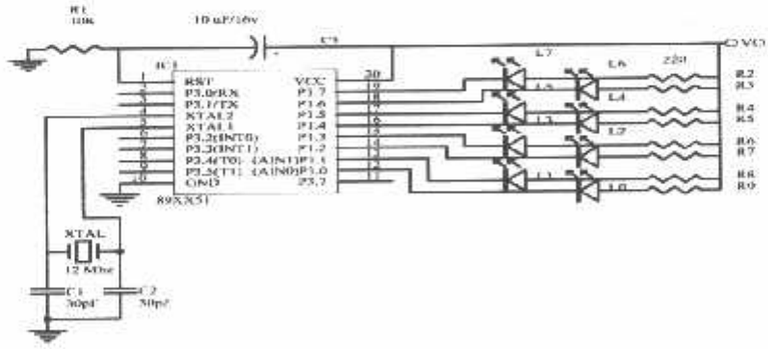
Tabel 4.6 Data Hasil Pengujian *Limit Switch*

Pada motor korden

4.1.6. Pengujian Mikrokontroler sebagai Sistem Minimum

1. Pengujian Mikrokontroler sebagai Output (Keluaran)

Pengujian ini bertujuan untuk mengetahui apakah *port-port* pada mikrokontroler yang digunakan dapat berjalan dengan baik. Dalam pengujian ini kaki-kaki pada *Port* 1 dihubungkan dengan LED . Dalam keadaan normal *port* berlogika 1 (LED mati). Pada saat *port* 1 diberi logika 0, maka LED menyala.



Gambar 4.6 Pengujian Mikrokontroler sebagai Output

Pada pengujian ini, setelah alat dirangkai seperti pada Gambar 4.1, kemudian dilanjutkan dengan pengisian program pada mikrokontroler. Setelah program dikompiler, maka akan tampak perubahan LED pada *port* 1.

Listing Program :

```
        org 0h
start:  mov p1,#00000000b
        call delay
        mov p1,#11110000b
        call delay
        mov p1,#00001111b
        call delay
        mov p1,#11111111b
        call delay
        jmp start
delay:  mov R0, #255
loop1:  mov R1, #255
loop2:  DJNZ R0, loop2
        DJNZ R1, loop1
        ret
end
```

Tabel 4.7

Pengujian Mikrokontroler sebagai Output

Waktu	Logika pada Port 1	LED pada Port 1							
		L7	L6	L5	L4	L3	L2	L1	L0
1	00000000b	H	H	H	H	H	H	H	H
2	11110000b	M	M	M	M	H	H	H	H
3	00001111b	H	H	H	H	M	M	M	M
4	11111111b	M	M	M	M	M	M	M	M

Keterangan :

H : Hidup

M : Mati

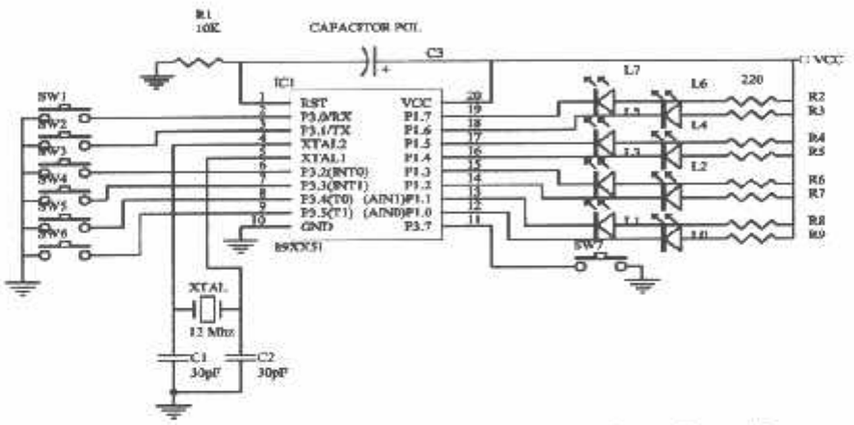
Dari tabel pengujian di atas, dapat dilihat percobaan pertama degan memberi perintah *mov p1,#00000000b* (isikan *p1* dengan data 00000000b) kepada mikrokontroler akan megaktifkan semua led. Oleh karena itu, dapat diambil kesimpulan bahwa mikrokontroler dapat dijadikan sebagai output. Adapun variasi nyala LED tergantung pada perintah-perintah pada program yang telah dibuat. Pada program dibawah ini, dibuat variasi nyala lampu LED dimana hasil dari pengujian ini, ditunjukan pada Tabel 4.1.

4.1.2. Pengujian Mikrokontroler sebagai Input (Masukan)

Pengujian ini untuk membuktikan bahwa *port* pada mikrokontroler dapat dijadikan sebagai input (masukan) untuk *port* lain. Dalam keadaan normal, *port-port* pada mikrokontroler berlogika 1 atau bila dihubungkan dengan LED, maka

dalam keadaan mati. Dalam gambar di bawah, kaki-kaki pada *port* 3 masing-masing dihubungkan dengan *switch* dan kaki-kaki pada *port* 1 masing-masing dihubungkan dengan LED. Bila salah satu *switch* pada kaki *port* 3 ini ditekan, maka menyebabkan kaki tersebut berlogika 0. Saat kaki tersebut

berlogika 0, maka ia menjadi inputan kaki-kaki pada *port* 1, yang menyebabkan kaki pada *port* 1 juga berlogika 0 sehingga LED menyala.



Gambar 4.7 Pengujian Mikrokontroler sebagai Input

Pengujian tersebut diawali dengan pengisian program pada mikrokontroler setelah alat dirangkai seperti pada Gambar 4.2. Setelah mikrokontroler diprogram, mulai dilakukan pengujian dengan menekan salah satu switch yang ada pada port 3. Saat itu pula, terjadi perubahan pada LED pada Port 1. Adapun hasil dari pengujian ini dapat dilihat dalam Tabel 4.2. Hasil dari pengujian tersebut disesuaikan dengan program yang telah dibuat.

Listing Program :

```
        org 0h
start:  jnb p3.0,uji1           ; jnb : jump not bit
        jnb p3.1,uji2
        jnb p3.2,uji3
        jnb p3.3,uji4
        jnb p3.4,uji5
        jnb p3.5,uji6
        jmp mulai
uji1:   mov p1,#11111110b
        jmp start
uji2:   mov p1,#11111101b
        jmp start
uji3:   mov p1,#11111011b
        jmp start
uji4:   mov p1,#11110111b
        jmp start
uji5:   mov p1,#11101111b
        jmp start
uji6:   mov p1,#10111111b
        jmp start
        end
```

Tabel 4.8

Tabel Pengujian Mikrokontroler sebagai Input

KONDISI SWITCH (SW)	LED							
	P1.7	P1.6	P1.5	P1.4	P1.3	P1.2	P1.1	P1.0
P3.0 ditekan	1	1	1	1	1	1	1	0
P3.1 ditekan	1	1	1	1	1	1	0	1
P3.2 ditekan	1	1	1	1	1	0	1	1
P3.3 ditekan	1	1	1	1	0	1	1	1
P3.4 ditekan	1	1	1	0	1	1	1	1
P3.5 ditekan	1	1	0	1	1	1	1	1

Keterangan :

1 : LED Mati

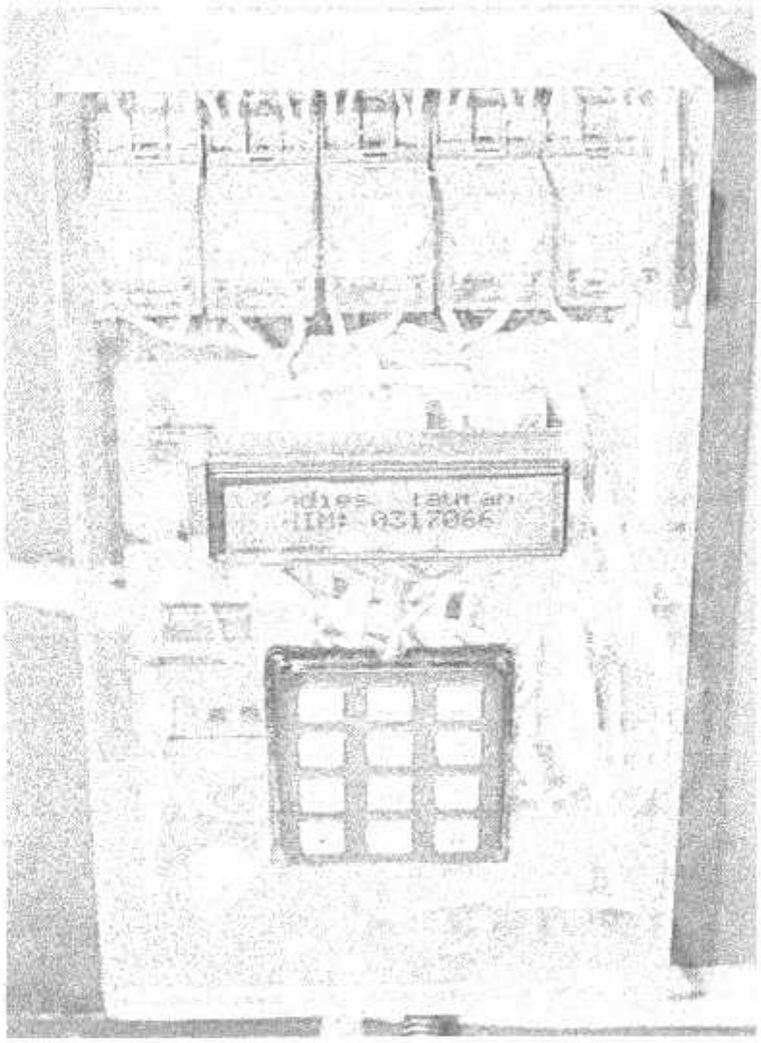
0 : LED Nyala

Program listning di atas digunakan untuk menghidupkan LED melalui tombol-tekan di P3.0-P3.5. Dengan demikian akan dilakukan proses *polling* (pengecekan terus menerus) pada port 3 apakah ada tombol yang ditekan atau tidak?

Jika tombol pada P3.0 ditekan maka akan terbaca P1=11111110b, hal ini sesuai instruksi program *mov p1,#11111110b* yang akan menyebabkan LED pada P1.0 akan menyala sesuai dengan tabel 4.2. Oleh karena itu, dapat diambil kesimpulan bahwa mikrokontroler dapat dijadikan input (masukan). Adapun dari

percobaan yang telah dilakukan, dapat dikatakan bahwa sebuah input (masukan) dapat mempengaruhi output (keluaran).

Demikian gambar pengontrol keseluruhan alat :



Gambar 4.8 Alat Pengontrol

BAB V

KESIMPULAN DAN SARAN

5.1. Kesimpulan

Berdasarkan pembuatan alat ruangan multi fungsi berbasis mikrokontroller AT89S51 dapat diambil kesimpulan sebagai berikut:

1. Pengujian pada Sensor asap dapat diatur sesuai dengan setingan batas asap yang diinginkan karena apabila setingan pada point tertinggi maka ADC mendeteksi adanya asap juga makin tinggi sampi diatas batas setpoint.
2. Pada rangkaian penerima intruksi IRM memiliki kepekaan yang tinggi jadi pada saat menekan tombol pada remote tidak sejajar dengan IRM sering terjadi pengacakan penerimaan jadi tidak sesuai dengan perintah dari remote.
3. Pada rangkaian driver relay diberi didoda eksternal sebai pengaman apabila ada arus balik dan Led untuk mengetahui kerja relay yang pada kondisi aktif.
4. Driver Fan disimulasikan sebagai blower untuk mengeluarkan asap dalam ruangan yang secara fungsionalnya bekerja setelah mendapat intruksi dari pembacaan sensor asap.
5. Pergerakan kerja motor korden dihentikan oleh limit switch untuk buka dan tutupnya tetapi limit tidak berfungsi penuh pada rangkaian

ini maka untuk menghindari terjadinya selip maka diberi timer dalam progam.

5.2. Saran

Tujuan utama dari penulisan adalah bagaimana membuat alat untuk mengatur suatu ruangan single menjadi ruangan multifungsi atau merubah ruang santai menjadi ruangan kerja dengan system kerjanya merubah pada dinding interior Tv dan ditambahkan fitur – fitur lain untuk memberikan konsep ruangan pada rumah moderen yang berbasis mikrokontroller dan elektro mekanik. Saran-saran yang bisa digunakan untuk pengembangan alat ini secara lanjut antara lain:

1. Dalam penggunaan motor Dc gearbox perlu diperhatikan perbandingan gear atau gigi transmisi pada motor Dc untuk pergarakan yang lebih akurat dan memperkecil kemungkinan error, karena berpengaruh pada kekuatan dan putaran motor.
2. Dalam perancangan software dengan menggunakan Mikrokontroller perlu diperhatikan seberapa besar memory yang diperlukan untuk perancangan alat, sehingga kita dapat menggunakan pilihan pemograman sesuai kebtuhan alat.
3. Pada saat pengerjaan perancangan mekaniuk disarankan agar memperhitungkan tiap – tiap penataan mekanik untuk hasil yang maksimal dan tidak menganggu aktifitas kerja alat lain.
4. Sebelum Software kita downlodkan perlu kita simulasikan dalam Logic Simulator untuk melihat hasilnya.

5. Agar pengontrolan lebih akurat maka antara remote control dan modul IR perlu tegak lurus ataau sama rata, perlunya untuk menghindari penerimaan intruksi yang mengacak atau pembacaan perintah yang tidak sesuai.

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Data sheet D-AF30-1

GAS SENSORS : TYPE AF30

LAMPIRAN

PERKUMPULAN PENGELOLA PENDIDIKAN UMUM DAN TEKNOLOGI NASIONAL MALANG

INSTITUT TEKNOLOGI NASIONAL MALANG

FAKULTAS TEKNOLOGI INDUSTRI
FAKULTAS TEKNIK SIPIL DAN PERENCANAAN
PROGRAM PASCASARJANA MAGISTER TEKNIK

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Malang, 01 Juli 2009

Nomor : ITN- 020/7/TA /2009
Lampiran :
Perihal : ***Bimbingan Skripsi***

Kepada : Yth. Sdr. **JOSEPH DEDY IRAWAN, ST, MT**
Dosen Pembimbing
Jurusan Teknik Elektro S-1
di
Malang

Dengan hormat,
Sesuai dengan permohonan dan persetujuan dalam proposal skipsi untuk mahasiswa:

Nama	: **Andies Taufan Unggul Nurmansyah**
Nim	: **03 17 066**
Fakultas	: **Teknologi Industri**
Jurusan	: **Teknik Elektro S-1**
Konsentrasi	: **Teknik Elektronika**

Maka dengan ini pembimbingan tersebut kami serahkan sepenuhnya kepada Saudara/i selama masa waktu 6 (enam) bulan. terhitung mulai ,tanggal:

23 JUNI 2009 s/d 23 DESEMBER 2009

Sebagai satu syarat untuk menempuh Ujian sarjana.
Demikian atas perhatian serta kerjasama yang baik kami ucapkan terima kasih

Ketua Jurusan
Teknik Elektro S-1

Ir. Yudi Limpraptono, MT
NIP. Y. 1039500274

Tindasan:
1. Mahasiswa yang Bersangkutan
2. Arsip

Form S-4a

INSTITUT TEKNOLOGI NASIONAL
JL. RAYA KARANGLO, KM 2
MALANG

FORMULIR BIMBINGAN SKRIPSI

Nama : **ANDIES TAUFAN UNGGUL NURMANSYAH**
Nim : **03 17 066**
Masa Bimbingan : **23 JUNI 2009 s/d 23 DESEMBER 2009**
Judul Skripsi : **Perancangan dan Pembuatan Sistem Ruangan Multifungsi Mikrokontroller AT89S51**

NO.	TANGGAL	URAIAN	PARAF PEMBIMBING
1.	2-9-2009	Susun Bab 1 s/d 3	
2.	10-9-2009	Bab I, II	
3.	19-9-2009	Bab III, IV	
4.	23-9-2009	Driver motor, Relay	
5.	25-9-2009	Acc Bab I, II, III	
6.	28-9-2009	Acc Bab IV V,	
7.	1-10-2009	Acc kompre	
8.			
9.			
10.			

Malang,
Dosen Pembmbing.

Joseph Dedy Irawan, ST, MT
NIP. 132315178

Form S-4 B

LCD M1632
MOTOR
MOTOR

Listing Program

```
org   00h                ; system reset
;
      Kbr2   Bit P1.0    ; keypad baris 2
      Kbr3   Bit P1.1    ; keypad baris 3
      Kcl3   Bit P1.2    ; keypad colom 3
      Kbr4   Bit P1.3    ; keypad baris 4
      Kcl1   Bit P1.4    ; keypad colom 1
      Kbr1   Bit P1.5    ; keypad baris 1
      Kcl2   Bit P1.6    ; keypad colom 2

      Ltkr   Bit P2.2    ; lantai kiri
      Ltkn   Bit P2.3    ; lantai kanan
      Krbk   Bit P2.4    ; korden buka
      Krtt   Bit P2.5    ; korden tutup
      Rest   Bit P2.6    ; RS LCD
      Enbl   Bit P2.7    ; E LCD

      IRRX   Bit P3.0    ; infra red module
      Lkbk   Bit P3.2    ; limit korden buka
      Lktt   Bit P3.3    ; limit korden tutup
      Llkn   Bit P3.4    ; limit lantai kanan
      Llkr   Bit P3.5    ; limit lantai kiri

      ISCL   Bit P3.6    ; I2C clock
      ISDA   Bit P3.7    ; I2C data

      Dasp   Equ 30h     ; data sensor asap
      Stpn   Equ 31h     ; data seting point
      Dlmp   Equ 32h     ; data lampu
```

```
    Dtrm   Equ 33h                  ; data remote
    Dtr0   Equ 34h                  ; data remote bit 0
    Dtr1   Equ 35h                  ; data remote bit 1
    Dtr2   Equ 36h                  ; data remote bit 2
    Dtr3   Equ 37h                  ; data remote bit 3
    Dtr4   Equ 38h                  ; data remote bit 4
    Dtr5   Equ 39h                  ; data remote bit 5
    Dtr6   Equ 3Ah                  ; data remote bit 6
    Dtr7   Equ 3Bh                  ; data remote bit 7

    Char   Equ 40h                  ; character LCD
    Tmo0   Equ 41h                  ; timeout 0
    Tmo1   Equ 42h                  ; timeout 1
    Bufr   Equ 43h                  ; buffer
    Buf0   Equ 44h                  ; buffer 0
    Buf1   Equ 45h                  ; buffer 1
    Buf2   Equ 46h                  ; buffer 2
    Dly0   Equ 47h                  ; delay 0
    Dly1   Equ 48h                  ; delay 1
    Dly2   Equ 49h                  ; delay 2
    Dly3   Equ 4Ah                  ; delay 3
;
init:  acall  lcd_in                ; inisialisasi LCD
       acall  tmr_in                ; inisialisasi timer
       mov    Dlmp,#0FFh    ; reset data lampu
       mov    Stpn,#150     ; set awal seting point
       mov    R1,#0FFh      ; reset data IR receive
;
mulai: mov    DPTR,#nama            ;\
       acall  line1                 ; | tulis data pointer nama
```

```
    mov   Char,#16          ; | pd line 1 sebanyak 16 char
    acall tulis             ;/
    mov   DPTR,#nim         ;\
    acall line2             ; | tulis data pointer nim
    mov   Char,#16          ; | pd line 2 sebanyak 16 char
    acall tulis             ;/
    acall delay2                    ; tunda waktu
    mov   DPTR,#jur         ;\
    acall line1             ; | tulis data pointer jur
    mov   Char,#16          ; | pd line 1 sebanyak 16 char
    acall tulis             ;/
    mov   DPTR,#univ        ;\
    acall line2             ; | tulis data pointer univ
    mov   Char,#16          ; | pd line 2 sebanyak 16 char
    acall tulis             ;/
    acall delay2                    ; tunda waktu
;
mesrmn: acall lcdclr                ; hapus layar LCD
    mov   DPTR,#tpstad              ;\
    acall line1             ; | tulis data pointer tpstad
    mov   Char,#16          ; | pd line 1 sebanyak 16 char
    acall tulis             ;/
    mov   DPTR,#angka               ;\
    acall bcasap                    ; |
    mov   P0,#0C2h          ; |
    acall w_ins                     ; |
    mov   A,Stpn                    ; |
    acall nilai             ; | tulis data seting point
    mov   P0,#0CBh          ; | & data asap
    acall w_ins                     ; |
```

```
      mov   A,Dasp                  ; |
      acall  nilai                  ; |
      mov   P0,#0D0h                ; |
      acall  w_ins                  ;/
      acall  bdgdta                 ; banding data Stpn dg Dasp
      acall  scnrmt                 ; scan remote
      acall  delay1                 ; tunda waktu
      sjmp   mesrmn                 ; loop
;
stgpnt: mov   DPTR,#tpstpn          ;\
      acall  line1                  ; | tulis data pointer tpstpn
      mov   Char,#16                ; | pd line 1 sebanyak 16 char
      acall  tulis                  ;/
      mov   DPTR,#tpadcn            ;\
      acall  line2                  ; | tulis data pointer tpadcn
      mov   Char,#16                ; | pd line 1 sebanyak 16 char
      acall  tulis                  ;/
      mov   Bufr,Stpn               ; simpan data seting point
stpnt0: mov   DPTR,#angka           ;\
      mov   P0,#0C9h                ; |
      acall  w_ins                  ; |
      mov   A,Bufr                  ; | tulis data nilai interval
      acall  nilai                  ; | line 1 colom 4
      mov   P0,#0D0h                ; |
      acall  w_ins                  ; |
      acall  tg_lps                 ;/
stpnt1: acall  scnkpd               ;\
      cjne   R0,#10,stpnt2          ; |
      sjmp   stpnt1                 ; |
stpnt2: cjne   R0,#11,stpnt3        ; | konvirmasi
```

```
      mov   SP,#07h                    ; |
      ljmp  mulai                      ; | can/ent/rubah data
stpnt3: cjne  R0,#12,stpnt4            ; | nilai interval
      mov   Stpn,Bufr            ; |
      mov   SP,#07h                    ; |
      ljmp  mulai                      ;/
stpnt4: mov   P0,#0C9h                 ;\
      acall w_ins                      ; |
      mov   A,R0                       ; |
      mov   Buf0,A                     ; |
      acall wr_chr                     ; |
      acall tg_lps                     ; |
      acall tg_tkn                     ; |
      mov   A,R0                       ; | pengisian data
      mov   Buf1,A                     ; | nilai seting point
      acall wr_chr                     ; |
      acall tg_lps                     ; |
      acall tg_tkn                     ; |
      mov   A,R0                       ; |
      mov   Buf2,A                     ; |
      acall wr_chr                     ; |
      acall tg_lps                     ;/
      mov   A,Buf0                     ;\
      mov   B,#100                     ; |
      mul   AB                   ; |
      mov   Buf0,A                     ; |
      mov   A,Buf1                     ; |
      mov   B,#10                      ; | pembulatan data
      mul   AB                   ; | nilai interval
      mov   B,Buf2                     ; |
```

```
    add   A,B                ; |
    mov   B,Buf0                    ; |
    add   A,B                ; |
    mov   Bufr,A                    ; |
    ljmp  stpnt0                    ;/
;
bcasap: mov   A,#90h                ; address PCF8591 write address
    acall adrtx              ; kirim
    mov   A,#00h                    ; adc ch-0
    acall dtatx              ; kirim
    mov   A,#91h                    ; address PCF8591 read address
    acall adrtx              ; kirim
    acall dtarx              ; baca data
    acall givack                    ; beri ack
    acall dtarx              ; baca data
    acall i2cstp                    ; i2c stop
    mov   Dasp,A                    ; simpan data sensor
    ret
;
bdgdta: mov   A,Dasp                ;\
    mov   B,Stpn                    ; |
    div   AB                 ; |
    jz    bddta0                    ; |
    mov   A,Dlmp                    ; |
    clr   Acc.6              ; | banding data seting point
    mov   Dlmp,A                    ; | dg data asap
    sjmp  bddta1                    ; | if lebih besar -> fan on
bddta0: mov   A,Dlmp                ; |   not      -> fan off
    setb  Acc.6                     ; |
    mov   Dlmp,A                    ; |
```

```
bddta1: acall  drvlmp                ; |
    ret                              ;/
;
drvlmp: mov    A,#70h                ;\
    acall  adrtx                     ; |
    mov    A,Dlmp                    ; | drive
    acall  dtatx                     ; | lampu
    acall  i2cstp                    ; |
    ret                              ;/
;
adrtx: acall  i2cstr                 ; kirim address
    acall  putbit                    ; kirim data
    ret                              ; back
;
dtatx: acall  putbit                 ; kirim data
    ret                              ; back
;
dtarx: acall  getbit                 ; terima data
    ret                              ; back
;
putbit: mov    R7,#8                 ;\
putbt: RLC    A                      ; |
    mov    ISDA,C                    ; |
    setb   ISCL                      ; |
    clr    ISCL                      ; | kirim bit
    djnz   R7,putbt                  ; |
    setb   ISDA                      ; |
    acall  getack                    ; |
    ret                              ;/
;
```

```
getbit: mov   R7,#8                ;\
getbt:  setb  ISCL                 ; |
        mov   C,ISDA               ; |
        RLC   A                    ; | terima bit
        clr   ISCL                 ; |
        djnz  R7,getbt             ; |
        setb  ISDA                 ; |
        ret                        ;/
;
getack: setb  ISDA                 ;\
        setb  ISCL                 ; |
ackbit: mov   C,ISDA               ; | tunggu ack
        jc    ackbit               ; | D=1, C=1D=0, C=0
        clr   ISCL                 ; |
        ret                        ;/
;
givack: clr   ISDA                 ;\
        setb  ISCL                 ; |
        clr   ISCL                 ; | kirim ack -> D=0, C=1, C=0, D=1
        setb  ISDA                 ; |
        ret                        ;/
;
i2cstr: setb  ISCL                 ;\
        setb  ISDA                 ; |
        clr   ISDA                 ; | i2c start -> C=1, D=1, D=0, C=0
        clr   ISCL                 ; |
        ret                        ;/
;
i2cstp: clr   ISDA                 ;\
        setb  ISCL                 ; |
```

```
    setb  ISDA              ; | i2c stop -> D=0, C=1, D=1, C=0
    clr   ISCL              ; |
    ret                     ;/
;
scnrmt: cjne  R1,#255,scrmt0        :\
    ljmp  scrmtl                    ; |
scrmt0: cjne  R1,#000,scrmt1        ; |
    mov   A,Dlmp                    ; |
    clr   Acc.0             ; |
    mov   Dlmp,A                    ; |
    ljmp  scrmtG                    ; |
scrmt1: cjne  R1,#001,scrmt2        ; |
    mov   A,Dlmp                    ; |
    clr   Acc.1             ; |
    mov   Dlmp,A                    ; |
    ljmp  scrmtG                    ; |
scrmt2: cjne  R1,#002,scrmt3        ; |
    mov   A,Dlmp                    ; |
    clr   Acc.2             ; |
    mov   Dlmp,A                    ; |
    ljmp  scrmtG                    ; |
scrmt3: cjne  R1,#003,scrmt4        ; |
    mov   A,Dlmp                    ; |
    clr   Acc.3             ; |
    mov   Dlmp,A                    ; |
    ljmp  scrmtG                    ; |
scrmt4: cjne  R1,#004,scrmt5        ; |
    mov   A,Dlmp                    ; |
    clr   Acc.7             ; |
    mov   Dlmp,A                    ; |
```

```
        sjmp   scrmtG                   ; |
scrmt5: cjne   R1,#005,scrmt6           ; |
        mov    A,Dlmp                   ; |
        setb   Acc.0                    ; |
        mov    Dlmp,A                   ; |
        sjmp   scrmtG                   ; |
scrmt6: cjne   R1,#006,scrmt7           ; |
        mov    A,Dlmp                   ; |
        setb   Acc.1                    ; |
        mov    Dlmp,A                   ; |
        sjmp   scrmtG                   ; |
scrmt7: cjne   R1,#007,scrmt8           ; |
        mov    A,Dlmp                   ; |
        setb   Acc.2                    ; | scan remote
        mov    Dlmp,A                   ; |
        sjmp   scrmtG                   ; |
scrmt8: cjne   R1,#008,scrmt9           ; |
        mov    A,Dlmp                   ; |
        setb   Acc.3                    ; |
        mov    Dlmp,A                   ; |
        sjmp   scrmtG                   ; |
scrmt9: cjne   R1,#009,scrmtA           ; |
        mov    A,Dlmp                   ; |
        setb   Acc.7                    ; |
        mov    Dlmp,A                   ; |
        sjmp   scrmtG                   ; |
scrmtA: cjne   R1,#012,scrmtB           ; |
        mov    A,Dlmp                   ; |
        clr    Acc.0                    ; |
        clr    Acc.1                    ; |
```

```
        clr   Acc.2                ;|
        clr   Acc.3                ;|
        clr   Acc.7                ;|
        mov   Dlmp,A               ;|
        sjmp  scrmtG               ;|
scrmtB: cjne  R1,#013,scrmtC       ;|
        mov   A,Dlmp               ;|
        setb  Acc.0                ;|
        setb  Acc.1                ;|
        setb  Acc.2                ;|
        setb  Acc.3                ;|
        setb  Acc.7                ;|
        mov   Dlmp,A               ;|
        sjmp  scrmtG               ;|
scrmtC: cjne  R1,#016,scrmtD       ;|
        acall krdbka               ;|
        sjmp  scrmtH               ;|
scrmtD: cjne  R1,#017,scrmtE       ;|
        acall krdttp               ;|
        sjmp  scrmtH               ;|
scrmtE: cjne  R1,#018,scrmtF       ;|
        acall lntknn               ;|
        sjmp  scrmtH               ;|
scrmtF: cjne  R1,#019,scrmtH       ;|
        acall lntkrr               ;|
        sjmp  scrmtH               ;|
scrmtG: acall drvlmp               ;|
scrmtH: mov   R1,#0FFh             ;|
scrmtl: ret                        ;/
;
```

```
bc_rmt: jb    IRRX,bcrmt0          ;\
    setb  TR0                  ; |
    jnb   IRRX,$               ; |
    clr   TR0                  ; |
    mov   A,TH0                ; | baca start remote
    mov   B,#8                 ; |
    div   AB                   ; |
    jnz   bcrmt1               ; |
bcrmt0: sjmp  bcrmt5           ;/
;
bcrmt1: acall  bcbtrm          ;\
    mov   Dtr0,A               ; |
    acall bcbtrm               ; |
    mov   Dtr1,A               ; |
    acall bcbtrm               ; |
    mov   Dtr2,A               ; |
    acall bcbtrm               ; |
    mov   Dtr3,A               ; |
    acall bcbtrm               ; | baca bit remote
    mov   Dtr4,A               ; |
    acall bcbtrm               ; |
    mov   Dtr5,A               ; |
    acall bcbtrm               ; |
    mov   Dtr6,A               ; |
    acall bcbtrm               ; |
    mov   Dtr7,#0              ; |
    acall bcbtrm               ;/
;
    mov   R1,#0                ;\
    mov   A,Dtr0               ; |
```

```
acall  ckbtrm                ; |
mov    A,R1                  ; |
RRC    A                ; |
mov    R1,A                  ; |
mov    A,Dtr1                ; |
acall  ckbtrm                ; |
mov    A,R1                  ; |
RRC    A                ; |
mov    R1,A                  ; |
mov    A,Dtr2                ; |
acall  ckbtrm                ; |
mov    A,R1                  ; |
RRC    A                ; |
mov    R1,A                  ; |
mov    A,Dtr3                ; |
acall  ckbtrm                ; |
mov    A,R1                  ; |
RRC    A                ; |
mov    R1,A                  ; | kalibrasi data remote
mov    A,Dtr4                ; | ke data binary
acall  ckbtrm                ; |
mov    A,R1                  ; |
RRC    A                ; |
mov    R1,A                  ; |
mov    A,Dtr5                ; |
acall  ckbtrm                ; |
mov    A,R1                  ; |
RRC    A                ; |
mov    R1,A                  ; |
mov    A,Dtr6                ; |
```

```
    acall  ckbtrm                    ; |
    mov    A,R1                      ; |
    RRC    A                  ; |
    mov    R1,A                      ; |
    mov    A,Dtr7                    ; |
    acall  ckbtrm                    ; |
    mov    A,R1                      ; |
    RRC    A                  ; |
    mov    R1,A                      ;/
    mov    TL0,#00                   ;\
    mov    TH0,#00                   ; | reset timer
bcrmt5: ret                          ;/
;
ckbtrm: cjne   A,#0,cbtrm0           ;\
      clr    C                ; |
      sjmp   cbtrm5                  ; |
cbtrm0: cjne   A,#1,cbtrm1           ; |
      clr    C                ; |
      sjmp   cbtrm5                  ; |
cbtrm1: cjne   A,#2,cbtrm2           ; |
      clr    C                ; |
      sjmp   cbtrm5                  ; | remap data
cbtrm2: cjne   A,#3,cbtrm3           ; | remote
      setb   C                ; |
      sjmp   cbtrm5                  ; |
cbtrm3: cjne   A,#4,cbtrm4           ; |
      setb   C                ; |
      sjmp   cbtrm5                  ; |
cbtrm4: cjne   A,#5,cbtrm5           ; |
      setb   C                ; |
```

```
cbtrm5: ret                         ;/
;
bcbtrm: mov   TL0,#00               ;\
        mov   TH0,#00               ; |
        jb    IRRX,$                ; |
        setb  TR0                   ; | baca bit
        jnb   IRRX,$                ; | remote
        clr   TR0                   ; |
        mov   A,TH0                 ; |
        ret                         ;/
;
krdbka: mov   Tmo0,#0               ;\
        mov   Tmo1,#25              ; |
        clr   Krbk                  ; |
        setb  Krtt                  ; |
krbka0: djnz  Dly0,krbka0           ; |
        jnb   Lkbk,krbka1           ; | korden buka
        sjmp  krbka2                ; |
krbka1: djnz  Tmo0,krbka0           ; |
        djnz  Tmo1,krbka0           ; |
krbka2: setb  Krbk                  ; |
        setb  Krtt                  ; |
        ret                         ;/
;
krdttp: mov   Tmo0,#0               ;\
        mov   Tmo1,#25              ; |
        setb  Krbk                  ; |
        clr   Krtt                  ; |
krttp0: djnz  Dly0,krttp0           ; |
        jnb   Lktt,krttp1           ; | korden tutup
```

```
    sjmp   krttp2                ; |
krttp1: djnz   Tmo0,krttp0       ; |
    djnz   Tmo1,krttp0           ; |
krttp2: setb   Krbk              ; |
    setb   Krtt                  ; |
    ret                          ;/
;
Intknn: mov    Tmo0,#0           ;\
    mov    Tmo1,#25              ; |
    setb   Ltkn                  ; |
    clr    Ltkr                  ; |
Inknn0: djnz   Dly0,Inknn0       ; |
    jnb    Llkn,Inknn1           ; | lantai kanan
    sjmp   Inknn2                ; |
Inknn1: djnz   Tmo0,Inknn0       ; |
    djnz   Tmo1,Inknn0           ; |
Inknn2: setb   Ltkn              ; |
    setb   Ltkr                  ; |
    ret                          ;/
;
Intkrr: mov    Tmo0,#0           ;\
    mov    Tmo1,#25              ; |
    clr    Ltkn                  ; |
    setb   Ltkr                  ; |
Inkrr0: djnz   Dly0,Inkrr0       ; |
    jnb    Llkr,Inkrr1           ; | lantai kiri
    sjmp   Inkrr2                ; |
Inkrr1: djnz   Tmo0,Inkrr0       ; |
    djnz   Tmo1,Inkrr0           ; |
Inkrr2: setb   Ltkn              ; |
```

```
    setb  Ltkr              ; |
    ret                     ;/
;
tmr_in: mov   Dly3,#1           ;\
    acall  delay3               ; | inisialisasi
    mov   TMOD,#11h         ; | timer
    ret                     ;/
;
nilai: mov   B,#100             ;\
    div   AB                ; |
    acall  wr_chr               ; |
    mov   A,B               ; |
nil:  mov   B,#10               ; | cacah nilai
    div   AB                ; |
    acall  wr_chr               ; |
    mov   A,B               ; |
    acall  wr_chr               ; |
    ret                     ;/
;
scnkpd: acall  delay0           ;\
    mov   R0,#10                ; |
b1c0:  clr   Kbr1               ; |
    setb  Kbr2              ; |
    setb  Kbr3              ; |
    setb  Kbr4              ; |
b1c1:  jb    Kcl1,b1c2          ; |
    mov   R0,#1                 ; |
b1c2:  jb    Kcl2,b1c3          ; |
    mov   R0,#2                 ; |
b1c3:  jb    Kcl3,b2c0          ; |
```

```
    mov   R0,#3                ;|
b2c0: setb  Kbr1               ;|
    clr   Kbr2             ;|
    setb  Kbr3             ;|
    setb  Kbr4             ;|
b2c1: jb    Kcl1,b2c2      ;|
    mov   R0,#4                ;|
b2c2: jb    Kcl2,b2c3      ;|
    mov   R0,#5                ;|
b2c3: jb    Kcl3,b3c0      ;|
    mov   R0,#6                ;|
b3c0: setb  Kbr1               ;|
    setb  Kbr2             ;| scan keypad
    clr   Kbr3             ;|
    setb  Kbr4             ;|
b3c1: jb    Kcl1,b3c2      ;|
    mov   R0,#7                ;|
b3c2: jb    Kcl2,b3c3      ;|
    mov   R0,#8                ;|
b3c3: jb    Kcl3,b4c0      ;|
    mov   R0,#9                ;|
b4c0: setb  Kbr1               ;|
    setb  Kbr2             ;|
    setb  Kbr3             ;|
    clr   Kbr4             ;|
b4c1: jb    Kcl1,b4c2      ;|
    mov   R0,#11               ;|
b4c2: jb    Kcl2,b4c3      ;|
    mov   R0,#0                ;|
b4c3: jb    Kcl3,back      ;|
```

```
    mov   R0,#12                    ; |
back: setb  Kbr1                    ; |
    setb  Kbr2                ; |
    setb  Kbr3                ; |
    setb  Kbr4                ; |
    ret                       ;/
;
tg_tkn: acall  scnkpd             ;\
tg_tk0: cjne   R0,#10,tg_tk1      ; |
    sjmp  tg_tkn                  ; |
tg_tk1: cjne   R0,#11,tg_tk2      ; |
    mov   SP,#07h                 ; | tunggu tekan angka
    ljmp  mulai                   ; |
tg_tk2: cjne   R0,#12,tg_tk3      ; |
    sjmp  tg_tkn                  ; |
tg_tk3: ret                       ;/
;
tg_lps: acall  scnkpd             ;\
    cjne  R0,#10,tg_lps           ; | tunggu lepas tombol
    ret                       ;/
;
line1: mov   P0,#080h         ;\
    acall  w_ins                  ; | line 1
    ret                       ;/
;
line2: mov   P0,#0C0h         ;\
    acall  w_ins                  ; | line 2
    ret                       ;/
;
tulis: clr   A                ;\
```

```
    acall  wr_chr                ; |
    inc    DPTR                  ; | tulis deret character LCD
    djnz   Char,tulis            ; |
    ret                          ;/
;
wr_chr: movc   A,@A+DPTR         ;\
    mov    P0,A                  ; | tulis character angka
    acall  w_chr                 ; | dari tabel angka
    ret                          ;/
;
w_ins: clr   Enbl                ;\
    clr    Rest                  ; |
    setb   Enbl                  ; | tulis
    clr    Enbl                  ; | instruksi LCD
wins:  djnz  Dly0,wins           ; |
    ret                          ;/
;
w_chr: clr   Enbl                ;\
    setb   Rest                  ; |
    setb   Enbl                  ; | tulis
    clr    Enbl                  ; | character LCD
wchr:  djnz  Dly0,wchr           ; |
    ret                          ;/
;
lcd_in: mov   Dly3,#1            ;\
    acall  delay3                ; |
    mov    P0,#01h               ; | Display Clear
    acall  w_ins                 ; |
    mov    P0,#38h               ; | Function Set
    acall  w_ins                 ; |
```

```
    mov   P0,#0Dh                ; | Display On, Cursor, Blink
    acall  w_ins                 ; |
    mov   P0,#06h                ; | Entry Mode
    acall  w_ins                 ; |
    mov   P0,#02h                ; | Cursor Home
    acall  w_ins                 ; |
    ret                         :/
;
lcdclr: mov   P0,#01h            :\
    acall  w_ins                 ; |
lcdcl0: djnz  Dly0,lcdcl0        ; | Display Clear
lcdcl1: djnz  Dly0,lcdcl1        ; |
    ret                         :/
;
delay0: djnz  Dly0,delay0        :\
    acall  bc_rmt                ; |
    ret                         :/
;
delay1: acall  scnkpd            :\
    cjne  R0,#12,dely10          ; | tunda waktu
    ljmp  stgpnt                 ; | dg loop register Dly1 dan delay0
dely10: djnz  Dly1,delay1        ; | scnkpd if 12 -> lompat stgpnt
    ret                         :/
;
delay2: mov   Dly2,#20           :\
dely20: acall  delay1            ; | tunda waktu
    djnz  Dly2,dely20            ; | dg loop register Dly2 dan delay1
    ret                         :/
;
delay3: djnz  Dly0,delay3        :\
```

```
    djnz   Dly1,delay3          ; | tunda waktu
    djnz   Dly3,delay3          ; | dg loop register Dly0, Dly1 & Dly3
    ret                         ;/
;
nama:  DB    ' Andies  Taufan ' ;\
nim:   DB    ' NIM: 0317066 '   ; |
jur:   DB    ' Teknik Elektro '  ; |
univ:  DB    '  ITN Malang  '    ; | string
tpstad: DB   ' Stp    ADC '     ; |
tpstpn: DB   ' Seting Point '   ; |
tpadcn: DB   '  ADC:     '      ; |
angka:  DB   '0123456789    '   ;/
;
    end
```

ıtures

- mpatible with MCS®-51 Products
- Bytes of In-System Programmable (ISP) Flash Memory
  - Endurance: 1000 Write/Erase Cycles
- V to 5.5V Operating Range
- ly Static Operation: 0 Hz to 33 MHz
- ee-level Program Memory Lock
- x 8-bit Internal RAM
- Programmable I/O Lines
- 16-bit Timer/Counters
- Interrupt Sources
- l Duplex UART Serial Channel
- v-power Idle and Power-down Modes
- rrupt Recovery from Power-down Mode
- chdog Timer
- al Data Pointer
- ver-off Flag
- t Programming Time
- ible ISP Programming (Byte and Page Mode)
- en (Pb/Halide-free) Packaging Option

Description

T89S51 is a low-power, high-performance CMOS 8-bit microcontroller with 4K of In-System Programmable Flash memory. The device is manufactured using 's high-density nonvolatile memory technology and is compatible with the industandard 80C51 instruction set and pinout. The on-chip Flash allows the program ory to be reprogrammed in-system or by a conventional nonvolatile memory prner. By combining a versatile 8-bit CPU with In-System Programmable Flash on nolithic chip, the Atmel AT89S51 is a powerful microcontroller which provides a -flexible and cost-effective solution to many embedded control applications.

T89S51 provides the following standard features: 4K bytes of Flash, 128 bytes M, 32 I/O lines, Watchdog timer, two data pointers, two 16-bit timer/counters, a ector two-level interrupt architecture, a full duplex serial port, on-chip oscillator, ock circuitry. In addition, the AT89S51 is designed with static logic for operation to zero frequency and supports two software selectable power saving modes. dle Mode stops the CPU while allowing the RAM, timer/counters, serial port, and upt system to continue functioning. The Power-down mode saves the RAM conbut freezes the oscillator, disabling all other chip functions until the next external upt or hardware reset.

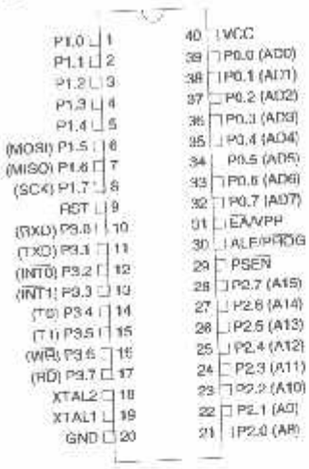
8-bit Microcontroller with 4K Bytes In-System Programmable Flash

AT89S51

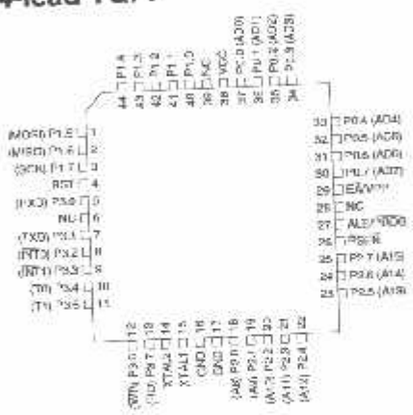
2487C–MICRO–03/05

Pin Configurations

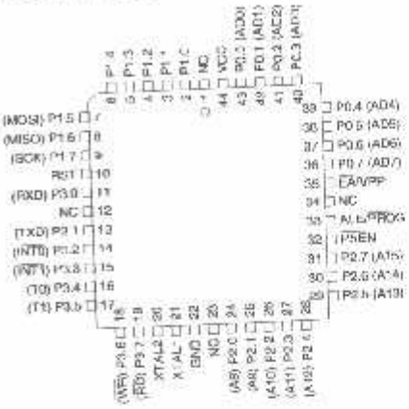
40-lead PDIP



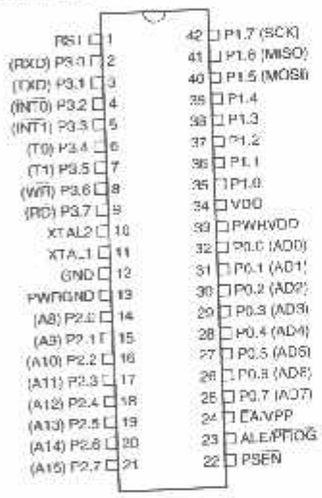
44-lead TQFP



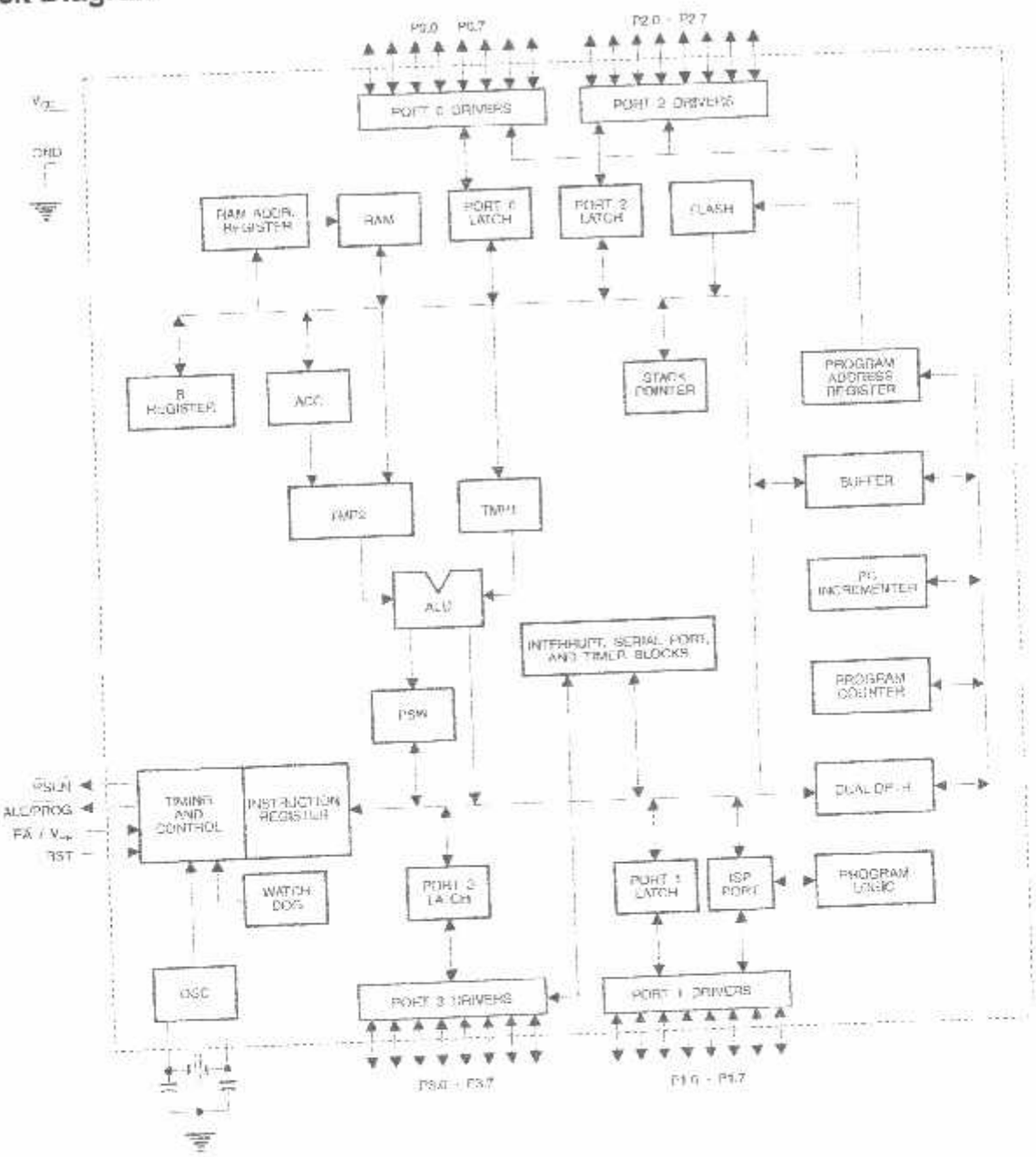
2.3 44-lead PLCC



2.4 42-lead PDIP



Block Diagram



Pin Description

VCC

Supply voltage (all packages except 42-PDIP).

GND

Ground (all packages except 42-PDIP; for 42-PDIP GND connects only the logic core and the embedded program memory).

VDD

Supply voltage for the 42-PDIP which connects only the logic core and the embedded program memory.

PWRVDD

Supply voltage for the 42-PDIP which connects only the I/O Pad Drivers. The application board **MUST** connect both VDD and PWRVDD to the board supply voltage.

PWRGND

Ground for the 42-PDIP which connects only the I/O Pad Drivers. PWRGND and GND are weakly connected through the common silicon substrate, but not through any metal link. The application board **MUST** connect both GND and PWRGND to the board ground.

Port 0

Port 0 is an 8-bit open drain bi-directional I/O port. As an output port, each pin can sink eight TTL inputs. When 1s are written to port 0 pins, the pins can be used as high-impedance inputs.

Port 0 can also be configured to be the multiplexed low-order address/data bus during accesses to external program and data memory. In this mode, P0 has internal pull-ups.

Port 0 also receives the code bytes during Flash programming and outputs the code bytes during program verification. **External pull-ups are required during program verification.**

Port 1

Port 1 is an 8-bit bi-directional I/O port with internal pull-ups. The Port 1 output buffers can sink/source four TTL inputs. When 1s are written to Port 1 pins, they are pulled high by the internal pull-ups and can be used as inputs. As inputs, Port 1 pins that are externally being pulled low will source current (I_{IL}) because of the internal pull-ups.

Port 1 also receives the low-order address bytes during Flash programming and verification.

Port Pin	Alternate Functions
P1.5	MOSI (used for In-System Programming)
P1.6	MISO (used for In-System Programming)
P1.7	SCK (used for In-System Programming)

Port 2

Port 2 is an 8-bit bi-directional I/O port with internal pull-ups. The Port 2 output buffers can sink/source four TTL inputs. When 1s are written to Port 2 pins, they are pulled high by the internal pull-ups and can be used as inputs. As inputs, Port 2 pins that are externally being pulled low will source current (I_{IL}) because of the internal pull-ups.

Port 2 emits the high-order address byte during fetches from external program memory and during accesses to external data memory that use 16-bit addresses (MOVX @ DPTR). In this application, Port 2 uses strong internal pull-ups when emitting 1s. During accesses to external data memory that use 8-bit addresses (MOVX @ RI), Port 2 emits the contents of the P2 Special Function Register.

Port 2 also receives the high-order address bits and some control signals during Flash programming and verification.

Port 3

Port 3 is an 8-bit bi-directional I/O port with internal pull-ups. The Port 3 output buffers can sink/source four TTL inputs. When 1s are written to Port 3 pins, they are pulled high by the internal pull-ups and can be used as inputs. As inputs, Port 3 pins that are externally being pulled low will source current (I_{IL}) because of the pull-ups.

Port 3 receives some control signals for Flash programming and verification.

Port 3 also serves the functions of various special features of the AT89S51, as shown in the following table.

Port Pin	Alternate Functions
P3.0	RXD (serial input port)
P3.1	TXD (serial output port)
P3.2	$\overline{INT0}$ (external interrupt 0)
P3.3	$\overline{INT1}$ (external interrupt 1)
P3.4	T0 (timer 0 external input)
P3.5	T1 (timer 1 external input)
P3.6	$\overline{WR}$ (external data memory write strobe)
P3.7	$\overline{RD}$ (external data memory read strobe)

RST

Reset input. A high on this pin for two machine cycles while the oscillator is running resets the device. This pin drives High for 98 oscillator periods after the Watchdog times out. The DISRTO bit in SFR AUXR (address 8EH) can be used to disable this feature. In the default state of bit DISRTO, the RESET HIGH out feature is enabled.

ALE/$\overline{PROG}$

Address Latch Enable (ALE) is an output pulse for latching the low byte of the address during accesses to external memory. This pin is also the program pulse input ($\overline{PROG}$) during Flash programming.

In normal operation, ALE is emitted at a constant rate of 1/6 the oscillator frequency and may be used for external timing or clocking purposes. Note, however, that one ALE pulse is skipped during each access to external data memory.

If desired, ALE operation can be disabled by setting bit 0 of SFR location 8EH. With the bit set, ALE is active only during a MOVX or MOVC instruction. Otherwise, the pin is weakly pulled high. Setting the ALE-disable bit has no effect if the microcontroller is in external execution mode.

$\overline{\text{PSEN}}$

Program Store Enable ($\overline{\text{PSEN}}$) is the read strobe to external program memory.

When the AT89S51 is executing code from external program memory, $\overline{\text{PSEN}}$ is activated twice each machine cycle, except that two $\overline{\text{PSEN}}$ activations are skipped during each access to external data memory.

$\overline{\text{EA}}$/VPP

External Access Enable. $\overline{\text{EA}}$ must be strapped to GND in order to enable the device to fetch code from external program memory locations starting at 0000H up to FFFFH. Note, however, that if lock bit 1 is programmed, $\overline{\text{EA}}$ will be internally latched on reset.

$\overline{\text{EA}}$ should be strapped to V_{CC} for internal program executions.

This pin also receives the 12-volt programming enable voltage (V_{PP}) during Flash programming.

XTAL1

Input to the inverting oscillator amplifier and input to the internal clock operating circuit.

XTAL2

Output from the inverting oscillator amplifier

Special Function Registers

A map of the on-chip memory area called the Special Function Register (SFR) space is shown in Table 5-1.

Note that not all of the addresses are occupied, and unoccupied addresses may not be implemented on the chip. Read accesses to these addresses will in general return random data, and write accesses will have an indeterminate effect.

e 5-1. AT89S51 SFR Map and Reset Values

8H								0FFH
								0F7H
0H	B 00000000							0EFH
								0E7H
8H	ACC 00000000							0DFH
								0D7H
0H	PSW 00000000							0CFH
								0C7H
8H	IP XX000000							0BFH
	P3 11111111							0B7H
0H	IE 0X000000							0AFH
8H	P2 11111111		AUXR1 XXXXXXX0				WDTRST XXXXXXXX	0A7H
0H	SCON 00000000	SBUF XXXXXXXX						9FH
8H	P1 11111111							97H
0H	TCON 00000000	TMOD 00000000	TL0 00000000	TL1 00000000	TH0 00000000	TH1 00000000	AUXR XXX00XX0	8FH
8H	P0 11111111	SP 00000111	DP0L 00000000	DP0H 00000000	DP1L 00000000	DP1H 00000000	PCON 0XXX0000	87H

software should not write 1s to these unlisted locations, since they may be used in future products to invoke new fea-
In that case, the reset or inactive values of the new bits will always be 0.

upt Registers: The individual interrupt enable bits are in the IE register. Two priorities can be set for each of the five
ıpt sources in the IP register.

Table 5-2. AUXR: Auxiliary Register

AUXR — Address = 8EH — Reset Value = XXX00XX0B

Not Bit Addressable

Bit	7	6	5	4	3	2	1	0
	–	–	–	WDIDLE	DISRTO	–	–	DISALE

–	Reserved for future expansion
DISALE	Disable/Enable ALE

DISALE Operating Mode

0	ALE is emitted at a constant rate of 1/6 the oscillator frequency
1	ALE is active only during a MOVX or MOVC insiruction

DISRTO	Disable/Enable Reset-out

DISRTO

0	Reset pin is driven High after WDT times out
1	Reset pin is input only

WDIDLE	Disable/Enable WDT in IDLE mode

WDIDLE

0	WDT continues to count in IDLE mode
1	WDT halts counting in IDLE mode

Dual Data Pointer Registers: To facilitate accessing both internal and external data memory, two banks of 16-bit Data Pointer Registers are provided: DP0 at SFR address locations 82H-83H and DP1 at 84H-85H. Bit DPS = 0 in SFR AUXR1 selects DP0 and DPS = 1 selects DP1. The user should **ALWAYS** initialize the DPS bit to the appropriate value before accessing the respective Data Pointer Register.

Power Off Flag: The Power Off Flag (POF) is located at bit 4 (PCON.4) in the PCON SFR. POF is set to "1" during power up. It can be set and rest under software control and is not affected by reset.

Table 5-3. AUXR1: Auxiliary Register 1

AUXR1 Address = A2H — Reset Value = XXXXXXX0B

Not Bit Addressable

Bit	7	6	5	4	3	2	1	0
	–	–	–	–	–	–	–	DPS

– Reserved for future expansion

DPS Data Pointer Register Select

DPS	
0	Selects DPTR Registers DP0L, DP0H
1	Selects DPTR Registers DP1L, DP1H

Memory Organization

MCS-51 devices have a separate address space for Program and Data Memory. Up to 64K bytes each of external Program and Data Memory can be addressed.

Program Memory

If the $\overline{EA}$ pin is connected to GND, all program fetches are directed to external memory.

On the AT89S51, if $\overline{EA}$ is connected to V_{CC}, program fetches to addresses 0000H through FFFH are directed to internal memory and fetches to addresses 1000H through FFFFH are directed to external memory.

Data Memory

The AT89S51 implements 128 bytes of on-chip RAM. The 128 bytes are accessible via direct and indirect addressing modes. Stack operations are examples of indirect addressing, so the 128 bytes of data RAM are available as stack space.

Watchdog Timer (One-time Enabled with Reset-out)

The WDT is intended as a recovery method in situations where the CPU may be subjected to software upsets. The WDT consists of a 14-bit counter and the Watchdog Timer Reset (WDTRST) SFR. The WDT is defaulted to disable from exiting reset. To enable the WDT, a user must write 01EH and 0E1H in sequence to the WDTRST register (SFR location 0A6H). When the WDT is enabled, it will increment every machine cycle while the oscillator is running. The WDT timeout period is dependent on the external clock frequency. There is no way to disable the WDT except through reset (either hardware reset or WDT overflow reset). When WDT overflows, it will drive an output RESET HIGH pulse at the RST pin.

Using the WDT

To enable the WDT, a user must write 01EH and 0E1H in sequence to the WDTRST register (SFR location 0A6H). When the WDT is enabled, the user needs to service it by writing 01EH and 0E1H to WDTRST to avoid a WDT overflow. The 14-bit counter overflows when it reaches 16383 (3FFFH), and this will reset the device. When the WDT is enabled, it will increment every machine cycle while the oscillator is running. This means the user must reset the WDT at least

every 16383 machine cycles. To reset the WDT the user must write 01EH and 0E1H to WDTRST. WDTRST is a write-only register. The WDT counter cannot be read or written. When WDT overflows, it will generate an output RESET pulse at the RST pin. The RESET pulse duration is 98xTOSC, where TOSC = 1/FOSC. To make the best use of the WDT, it should be serviced in those sections of code that will periodically be executed within the time required to prevent a WDT reset.

WDT During Power-down and Idle

In Power-down mode the oscillator stops, which means the WDT also stops. While in Power-down mode, the user does not need to service the WDT. There are two methods of exiting Power-down mode: by a hardware reset or via a level-activated external interrupt, which is enabled prior to entering Power-down mode. When Power-down is exited with hardware reset, servicing the WDT should occur as it normally does whenever the AT89S51 is reset. Exiting Power-down with an interrupt is significantly different. The interrupt is held low long enough for the oscillator to stabilize. When the interrupt is brought high, the interrupt is serviced. To prevent the WDT from resetting the device while the interrupt pin is held low, the WDT is not started until the interrupt is pulled high. It is suggested that the WDT be reset during the interrupt service for the interrupt used to exit Power-down mode.

To ensure that the WDT does not overflow within a few states of exiting Power-down, it is best to reset the WDT just before entering Power-down mode.

Before going into the IDLE mode, the WDIDLE bit in SFR AUXR is used to determine whether the WDT continues to count if enabled. The WDT keeps counting during IDLE (WDIDLE bit = 0) as the default state. To prevent the WDT from resetting the AT89S51 while in IDLE mode, the user should always set up a timer that will periodically exit IDLE, service the WDT, and reenter IDLE mode.

With WDIDLE bit enabled, the WDT will stop to count in IDLE mode and resumes the count upon exit from IDLE.

UART

The UART in the AT89S51 operates the same way as the UART in the AT89C51. For further information on the UART operation, please click on the document link below:

http://www.atmel.com/dyn/resources/prod_documents/DOC4316.PDF

Timer 0 and 1

Timer 0 and Timer 1 in the AT89S51 operate the same way as Timer 0 and Timer 1 in the AT89C51. For further information on the timers' operation, please click on the document link below:

http://www.atmel.com/dyn/resources/prod_documents/DOC4316.PDF

Interrupts

The AT89S51 has a total of five interrupt vectors: two external interrupts ($\overline{INT0}$ and $\overline{INT1}$), two timer interrupts (Timers 0 and 1), and the serial port interrupt. These interrupts are all shown in Figure 10-1.

Each of these interrupt sources can be individually enabled or disabled by setting or clearing a bit in Special Function Register IE. IE also contains a global disable bit, EA, which disables all interrupts at once.

Note that Table 10-1 shows that bit positions IE.6 and IE.5 are unimplemented. User software should not write 1s to these bit positions, since they may be used in future AT89 products.

The Timer 0 and Timer 1 flags, TF0 and TF1, are set at S5P2 of the cycle in which the timers overflow. The values are then polled by the circuitry in the next cycle.

Table 10-1. Interrupt Enable (IE) Register

(MSB)							(LSB)
EA	–	–	ES	ET1	EX1	ET0	EX0

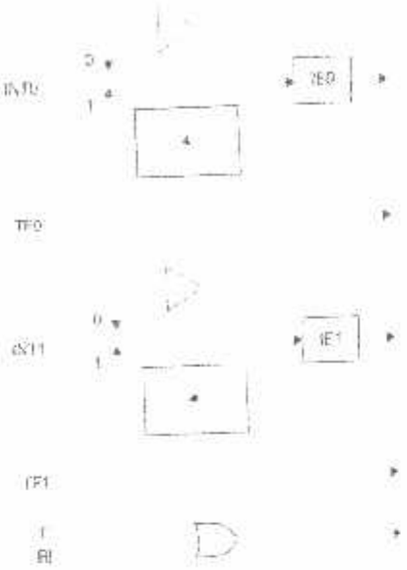
Enable Bit = 1 enables the interrupt.

Enable Bit = 0 disables the interrupt.

Symbol	Position	Function
EA	IE.7	Disables all interrupts. If EA = 0, no interrupt is acknowledged. If EA = 1, each interrupt source is individually enabled or disabled by setting or clearing its enable bit.
–	IE.6	Reserved
–	IE.5	Reserved
ES	IE.4	Serial Port interrupt enable bit
ET1	IE.3	Timer 1 interrupt enable bit
EX1	IE.2	External interrupt 1 enable bit
ET0	IE.1	Timer 0 interrupt enable bit
EX0	IE.0	External interrupt 0 enable bit

User software should never write 1s to reserved bits, because they may be used in future AT89 products.

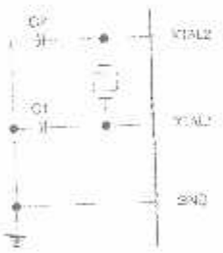
Figure 10-1. Interrupt Sources



Oscillator Characteristics

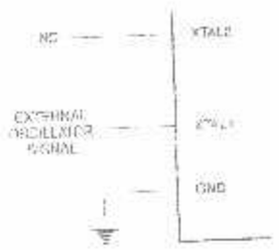
XTAL1 and XTAL2 are the input and output, respectively, of an inverting amplifier that can be configured for use as an on-chip oscillator, as shown in Figure 11-1. Either a quartz crystal or ceramic resonator may be used. To drive the device from an external clock source, XTAL2 should be left unconnected while XTAL1 is driven, as shown in Figure 11-2. There are no requirements on the duty cycle of the external clock signal, since the input to the internal clocking circuitry is through a divide-by-two flip-flop, but minimum and maximum voltage high and low time specifications must be observed.

Figure 11-1. Oscillator Connections



Note: C1, C2 = 30 pF ± 10 pF for Crystals
= 40 pF ± 10 pF for Ceramic Resonators

Figure 11-2. External Clock Drive Configuration



Idle Mode

In idle mode, the CPU puts itself to sleep while all the on-chip peripherals remain active. The mode is invoked by software. The content of the on-chip RAM and all the special function registers remain unchanged during this mode. The idle mode can be terminated by any enabled interrupt or by a hardware reset.

Note that when idle mode is terminated by a hardware reset, the device normally resumes program execution from where it left off, up to two machine cycles before the internal reset algorithm takes control. On-chip hardware inhibits access to internal RAM in this event, but access to the port pins is not inhibited. To eliminate the possibility of an unexpected write to a port pin when idle mode is terminated by a reset, the instruction following the one that invokes idle mode should not write to a port pin or to external memory.

Power-down Mode

In the Power-down mode, the oscillator is stopped, and the instruction that invokes Power-down is the last instruction executed. The on-chip RAM and Special Function Registers retain their values until the Power-down mode is terminated. Exit from Power-down mode can be initiated either by a hardware reset or by activation of an enabled external interrupt ($\overline{INT0}$ or $\overline{INT1}$). Reset redefines the SFRs but does not change the on-chip RAM. The reset should not be activated before V_{CC} is restored to its normal operating level and must be held active long enough to allow the oscillator to restart and stabilize.

Table 13-1. Status of External Pins During Idle and Power-down Modes

Mode	Program Memory	ALE	$\overline{PSEN}$	PORT0	PORT1	PORT2	PORT3
Idle	Internal	1	1	Data	Data	Data	Data
Idle	External	1	1	Float	Data	Address	Data
Power-down	Internal	0	0	Data	Data	Data	Data
Power-down	External	0	0	Float	Data	Data	Data

Program Memory Lock Bits

The AT89S51 has three lock bits that can be left unprogrammed (U) or can be programmed (P) to obtain the additional features listed in Table 14-1.

Table 14-1. Lock Bit Protection Modes

Program Lock Bits				Protection Type
	LB1	LB2	LB3	
1	U	U	U	No program lock features
2	P	U	U	MOVC instructions executed from external program memory are disabled from fetching code bytes from internal memory, $\overline{EA}$ is sampled and latched on reset, and further programming of the Flash memory is disabled
3	P	P	U	Same as mode 2, but verify is also disabled
4	P	P	P	Same as mode 3, but external execution is also disabled

When lock bit 1 is programmed, the logic level at the $\overline{EA}$ pin is sampled and latched during reset. If the device is powered up without a reset, the latch initializes to a random value and holds that value until reset is activated. The latched value of $\overline{EA}$ must agree with the current logic level at that pin in order for the device to function properly.

Programming the Flash – Parallel Mode

The AT89S51 is shipped with the on-chip Flash memory array ready to be programmed. The programming interface needs a high-voltage (12-volt) program enable signal and is compatible with conventional third-party Flash or EPROM programmers.

The AT89S51 code memory array is programmed byte-by-byte.

Programming Algorithm: Before programming the AT89S51, the address, data, and control signals should be set up according to the Flash Programming Modes table (Table 17-1) and Figure 17-1 and Figure 17-2. To program the AT89S51, take the following steps:

1. Input the desired memory location on the address lines.
2. Input the appropriate data byte on the data lines.
3. Activate the correct combination of control signals.
4. Raise $\overline{EA}/V_{PP}$ to 12V.
5. Pulse ALE/$\overline{PROG}$ once to program a byte in the Flash array or the lock bits. The byte-write cycle is self-timed and typically takes no more than 50 µs. Repeat steps 1 through 5, changing the address and data for the entire array or until the end of the object file is reached.

$\overline{Data}$ Polling: The AT89S51 features $\overline{Data}$ Polling to indicate the end of a byte write cycle. During a write cycle, an attempted read of the last byte written will result in the complement of the written data on P0.7. Once the write cycle has been completed, true data is valid on all outputs, and the next cycle may begin. $\overline{Data}$ Polling may begin any time after a write cycle has been initiated.

Ready/$\overline{Busy}$: The progress of byte programming can also be monitored by the RDY/$\overline{BSY}$ output signal. P3.0 is pulled low after ALE goes high during programming to indicate $\overline{BUSY}$. P3.0 is pulled high again when programming is done to indicate READY.

Program Verify: If lock bits LB1 and LB2 have not been programmed, the programmed code data can be read back via the address and data lines for verification. **The status of the individual lock bits can be verified directly by reading them back.**

Reading the Signature Bytes: The signature bytes are read by the same procedure as a normal verification of locations 000H, 100H, and 200H, except that P3.6 and P3.7 must be pulled to a logic low. The values returned are as follows.

(000H) = 1EH indicates manufactured by Atmel
(100H) = 51H indicates AT89S51
(200H) = 06H

Chip Erase: In the parallel programming mode, a chip erase operation is initiated by using the proper combination of control signals and by pulsing ALE/$\overline{PROG}$ low for a duration of 200 ns - 500 ns.

In the serial programming mode, a chip erase operation is initiated by issuing the Chip Erase instruction. In this mode, chip erase is self-timed and takes about 500 ms.

During chip erase, a serial read from any address location will return 00H at the data output.

Programming the Flash – Serial Mode

The Code memory array can be programmed using the serial ISP interface while RST is pulled to V_{CC}. The serial interface consists of pins SCK, MOSI (input) and MISO (output). After RST is set high, the Programming Enable instruction needs to be executed first before other operations can be executed. Before a reprogramming sequence can occur, a Chip Erase operation is required.

The Chip Erase operation turns the content of every memory location in the Code array into FFH.

Either an external system clock can be supplied at pin XTAL1 or a crystal needs to be connected across pins XTAL1 and XTAL2. The maximum serial clock (SCK) frequency should be less than 1/16 of the crystal frequency. With a 33 MHz oscillator clock, the maximum SCK frequency is 2 MHz.

Serial Programming Algorithm

To program and verify the AT89S51 in the serial programming mode, the following sequence is recommended:

1. Power-up sequence:
   a. Apply power between VCC and GND pins.
   b. Set RST pin to "H".

   If a crystal is not connected across pins XTAL1 and XTAL2, apply a 3 MHz to 33 MHz clock to XTAL1 pin and wait for at least 10 milliseconds.
2. Enable serial programming by sending the Programming Enable serial instruction to pin MOSI/P1.5. The frequency of the shift clock supplied at pin SCK/P1.7 needs to be less than the CPU clock at XTAL1 divided by 16.
3. The Code array is programmed one byte at a time in either the Byte or Page mode. The write cycle is self-timed and typically takes less than 0.5 ms at 5V.
4. Any memory location can be verified by using the Read instruction that returns the content at the selected address at serial output MISO/P1.6.

5. At the end of a programming session, RST can be set low to commence normal device operation.

Power-off sequence (if needed):

1. Set XTAL1 to "L" (if a crystal is not used).
2. Set RST to "L".
3. Turn V_{CC} power off.

Data Polling: The $\overline{\text{Data}}$ Polling feature is also available in the serial mode. In this mode, during a write cycle an attempted read of the last byte written will result in the complement of the MSB of the serial output byte on MISO.

Serial Programming Instruction Set

The Instruction Set for Serial Programming follows a 4-byte protocol and is shown in the "Serial Programming Instruction Set" on page 20.

Programming Interface – Parallel Mode

Every code byte in the Flash array can be programmed by using the appropriate combination of control signals. The write operation cycle is self-timed and once initiated, will automatically time itself to completion.

Most major worldwide programming vendors offer worldwide support for the Atmel AT89 microcontroller series. Please contact your local programming vendor for the appropriate software revision.

17-1. Flash Programming Modes

	V_{CC}	RST	$\overline{\text{PSEN}}$	ALE/$\overline{\text{PROG}}$	$\overline{\text{EA}}$/V_{PP}	P2.6	P2.7	P3.3	P3.6	P3.7	P0.7-0 Data	P2.3-0 Address	P1.7-0 Address
Code Data	5V	H	L	(2)	12V	L	H	H	H	H	D_N	A11-8	A7-0
Code Data	5V	H	L	H	H	L	L	L	H	H	D_{OUT}	A11-8	A7-0
Lock Bit 1	5V	H	L	(3)	12V	H	H	H	H	H	X	X	X
Lock Bit 2	5V	H	L	(3)	12V	H	H	H	L	L	X	X	X
Lock Bit 3	5V	H	L	(3)	12V	H	L	H	H	L	X	X	X
Lock Bits 1	5V	H	L	H	H	H	H	L	H	L	P0.2, P0.3, P0.4	X	X
Erase	5V	H	L	(1)	12V	H	L	H	L	L	X	X	X
Atmel ID	5V	H	L	H	H	L	L	L	L	L	1EH	0000	00H
Device ID	5V	H	L	H	H	L	L	L	L	L	51H	0001	00H
Device ID	5V	H	L	H	H	L	L	L	L	L	06H	0010	00H

1. Each $\overline{\text{PROG}}$ pulse is 200 ns - 500 ns for Chip Erase.
2. Each $\overline{\text{PROG}}$ pulse is 200 ns - 500 ns for Write Code Data.
3. Each $\overline{\text{PROG}}$ pulse is 200 ns - 500 ns for Write Lock Bits.
4. RDY/$\overline{\text{BSY}}$ signal is output on P3.0 during programming.
5. X = don't care.

Figure 17-1. Programming the Flash Memory (Parallel Mode)

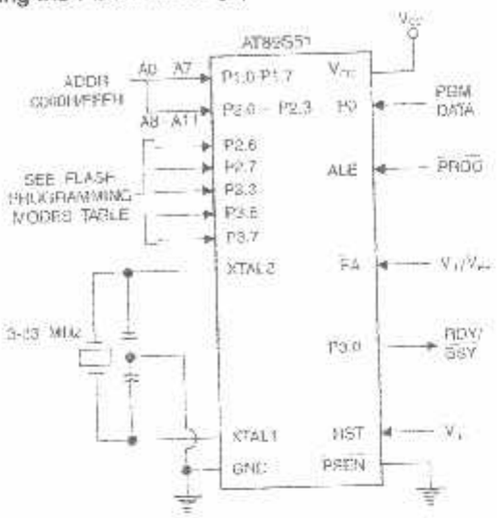
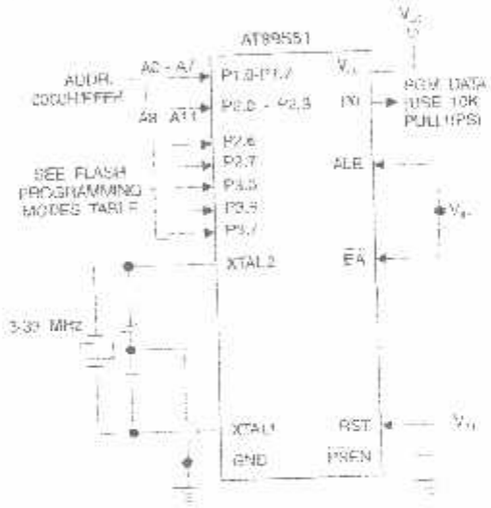


Figure 17-2. Verifying the Flash Memory (Parallel Mode)

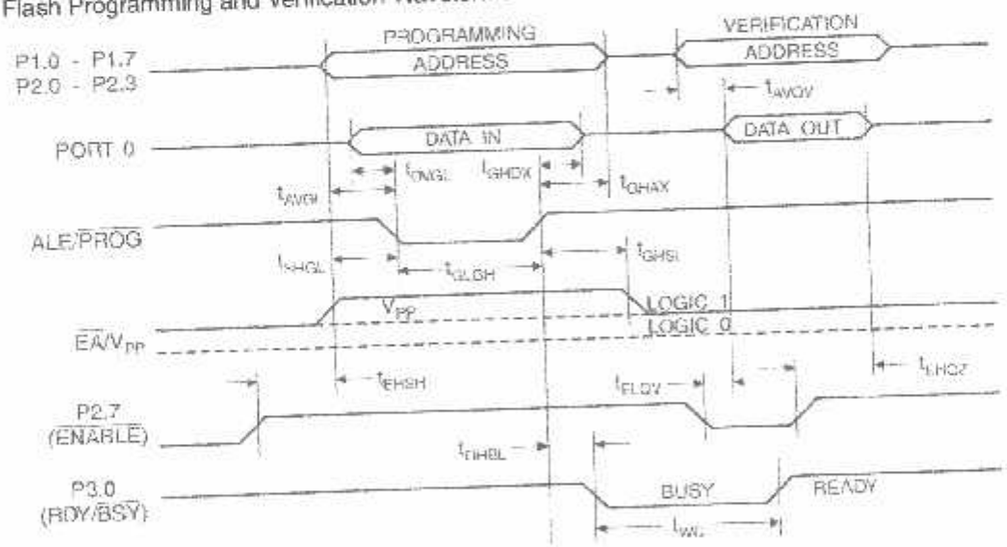


Flash Programming and Verification Characteristics (Parallel Mode)

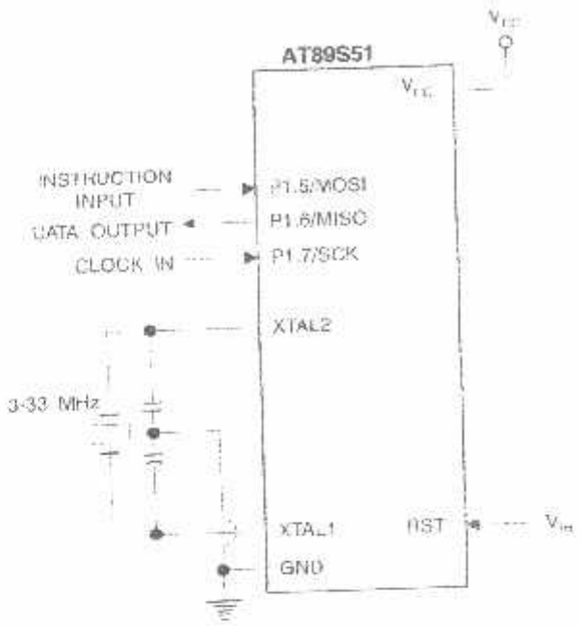
20°C to 30°C, V_{CC} = 4.5 to 5.5V

bol	Parameter	Min	Max	Units
	Programming Supply Voltage	11.5	12.5	V
	Programming Supply Current		10	mA
	V_{CC} Supply Current		30	mA
CL	Oscillator Frequency	3	33	MHz
	Address Setup to $\overline{PROG}$ Low	48 t_{CLCL}		
	Address Hold After $\overline{PROG}$	48 t_{CLCL}		
	Data Setup to $\overline{PROG}$ Low	48 t_{CLCL}		
	Data Hold After $\overline{PROG}$	48 t_{CLCL}		
	P2.7 (ENABLE) High to V_{PP}	48 t_{CLCL}		
	V_{PP} Setup to $\overline{PROG}$ Low	10		µs
	V_{PP} Hold After $\overline{PROG}$	10		µs
	$\overline{PROG}$ Width	0.2	1	µs
	Address to Data Valid		48t_{CLCL}	
	$\overline{ENABLE}$ Low to Data Valid		48t_{CLCL}	
	Data Float After $\overline{ENABLE}$	0	48t_{CLCL}	
	$\overline{PROG}$ High to $\overline{BUSY}$ Low		1.0	µs
	Byte Write Cycle Time		50	µs

e 18-1. Flash Programming and Verification Waveforms – Parallel Mode

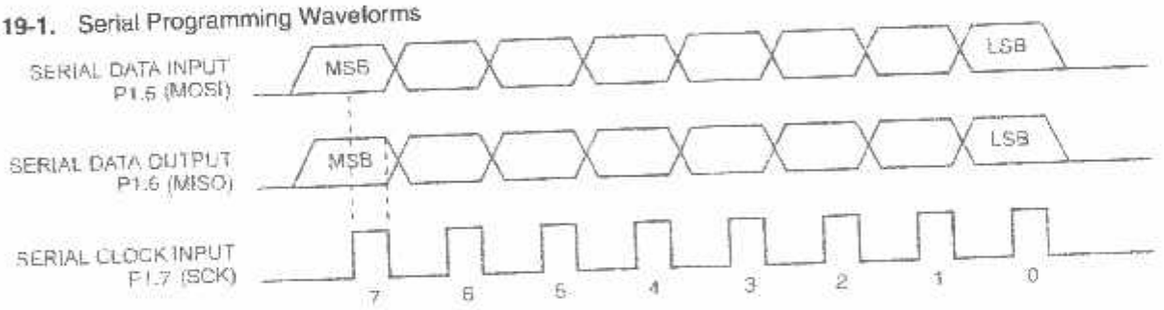


re 18-2. Flash Memory Serial Downloading



Flash Programming and Verification Waveforms – Serial Mode

e 19-1. Serial Programming Waveforms



Serial Programming Instruction Set

ruction	Instruction Format Byte 1	Byte 2	Byte 3	Byte 4	Operation
ıramming Enable	1010 1100	0101 0011	xxxx xxxx	xxxx xxxx 0110 1001 (Output on MISO)	Enable Serial Programming while RST is high
Erase	1010 1100	100x xxxx	xxxx xxxx	xxxx xxxx	Chip Erase Flash memory array
d Program Memory e Mode)	0010 0000	xxxx A11 A10 A9 A8	A7 A6 A5 A4 A3 A2 A1 A0	D7 D6 D5 D4 D3 D2 D1 D0	Read data from Program memory in the byte mode
e Program Memory e Mode)	0100 0000	xxxx A11 A10 A9 A8	A7 A6 A5 A4 A3 A2 A1 A0	D7 D6 D5 D4 D3 D2 D1 D0	Write data to Program memory in the byte mode
e Lock Bits[1]	1010 1100	1110 00 B1 B2	xxxx xxxx	xxxx xxxx	Write Lock bits. See Note (1).
d Lock Bits	0010 0100	xxxx xxxx	xxxx xxxx	xx B3 LB2 LB1 xx	Read back current status of the lock bits (a programmed lock bit reads back as a "1")
d Signature Bytes	0010 1000	xxxx A11 A10 A9 A8	A7 xxx xxx0	Signature Byte	Read Signature Byte
d Program Memory e Mode)	0011 0000	xxxx A11 A10 A9 A8	Byte 0	Byte 1... Byte 255	Read data from Program memory in the Page Mode (256 bytes)
e Program Memory e Mode)	0101 0000	xxxx A11 A10 A9 A8	Byte 0	Byte 1... Byte 255	Write data to Program memory in the Page Mode (256 bytes)

1. B1 = 0, B2 = 0 → Mode 1, no lock protection
   B1 = 0, B2 = 1 → Mode 2, lock bit 1 activated
   B1 = 1, B2 = 0 → Mode 3, lock bit 2 activated
   B1 = 1, B2 = 1 → Mode 4, lock bit 3 activated

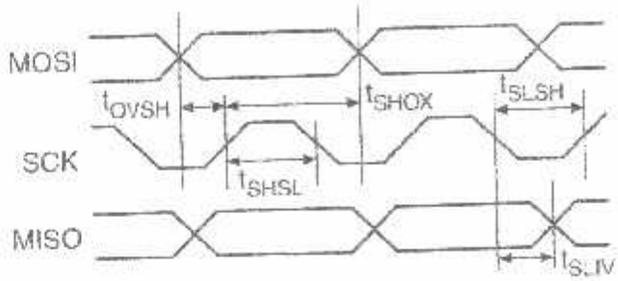
   } Each of the lock bit modes need to be activated sequentially before Mode 4 can be executed.

Reset signal is high, SCK should be low for at least 64 system clocks before it goes high to clock in the enable data No pulsing of Reset signal is necessary. SCK should be no faster than 1/16 of the system clock at XTAL1.

age Read/Write, the data always starts from byte 0 to 255. After the command byte and upper address byte are d, each byte thereafter is treated as data until all 256 bytes are shifted in/out. Then the next instruction will be ready decoded.

Serial Programming Characteristics

re 21-1. Serial Programming Timing



21-1. Serial Programming Characteristics, T_A = -40°C to 85°C, V_{CC} = 4.0 - 5.5V (Unless Otherwise Noted)

bol	Parameter	Min	Typ	Max	Units
CL	Oscillator Frequency	3		33	MHz
	Oscillator Period	30			ns
	SCK Pulse Width High	8 t_{CLCL}			ns
	SCK Pulse Width Low	8 t_{CLCL}			ns
	MOSI Setup to SCK High	t_{CLCL}			ns
	MOSI Hold after SCK High	2 t_{CLCL}			ns
	SCK Low to MISO Valid	10	16	32	ns
	Chip Erase Instruction Cycle Time			500	ms
SE	Serial Byte Write Cycle Time			64 t_{CLCL} + 400	µs

Absolute Maximum Ratings*

ating Temperature	-55°C to +125°C
ige Temperature	-65°C to +150°C
ge on Any Pin Respect to Ground	-1.0V to +7.0V
num Operating Voltage	6.6V
Output Current	15.0 mA

*NOTICE: Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC Characteristics

Values shown in this table are valid for T_A = -40°C to 85°C and V_{CC} = 4.0V to 5.5V, unless otherwise noted.

Symbol	Parameter	Condition	Min	Max	Units
	Input Low Voltage	(Except $\overline{EA}$)	-0.5	0.2 V_{CC}-0.1	V
	Input Low Voltage ($\overline{EA}$)		-0.5	0.2 V_{CC}-0.3	V
	Input High Voltage	(Except XTAL1, RST)	0.2 V_{CC}+0.9	V_{CC}+0.5	V
	Input High Voltage	(XTAL1, RST)	0.7 V_{CC}	V_{CC}+0.5	V
	Output Low Voltage[1] (Ports 1,2,3)	I_{OL} = 1.6 mA		0.45	V
	Output Low Voltage[1] (Port 0, ALE, $\overline{PSEN}$)	I_{OL} = 3.2 mA		0.45	V
	Output High Voltage (Ports 1,2,3, ALE, $\overline{PSEN}$)	I_{OH} = -60 µA, V_{CC} = 5V ± 10%	2.4		V
		I_{OH} = -25 µA	0.75 V_{CC}		V
		I_{OH} = -10 µA	0.9 V_{CC}		V
	Output High Voltage (Port 0 in External Bus Mode)	I_{OH} = -800 µA, V_{CC} = 5V ± 10%	2.4		V
		I_{OH} = -300 µA	0.75 V_{CC}		V
		I_{OH} = -80 µA	0.9 V_{CC}		V
	Logical 0 Input Current (Ports 1,2,3)	V_{IN} = 0.45V		-50	µA
	Logical 1 to 0 Transition Current (Ports 1,2,3)	V_{IN} = 2V, V_{CC} = 5V ± 10%		-300	µA
	Input Leakage Current (Port 0, EA)	0.45 < V_{IN} < V_{CC}		±10	µA
T	Reset Pulldown Resistor		50	300	KΩ
	Pin Capacitance	Test Freq. = 1 MHz, T_A = 25°C		10	pF
	Power Supply Current	Active Mode, 12 MHz		25	mA
		Idle Mode, 12 MHz		6.5	mA
	Power-down Mode[2]	V_{CC} = 5.5V		50	µA

1. Under steady state (non-transient) conditions, I_{OL} must be externally limited as follows:
   Maximum I_{OL} per port pin: 10 mA
   Maximum I_{OL} per 8-bit port:
   Port 0: 26 mA Ports 1, 2, 3: 15 mA
   Maximum total I_{OL} for all output pins: 71 mA
   If I_{OL} exceeds the test condition, V_{OL} may exceed the related specification. Pins are not guaranteed to sink current greater than the listed test conditions.
2. Minimum V_{CC} for Power-down is 2V.

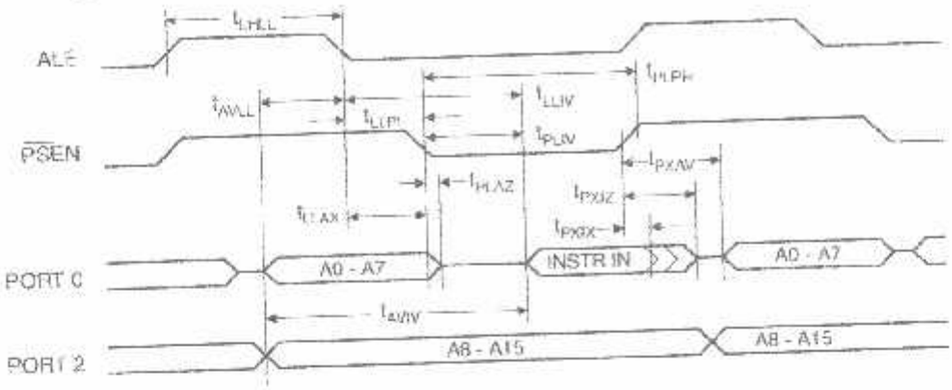
AC Characteristics

r operating conditions, load capacitance for Port 0, ALE/$\overline{PROG}$, and $\overline{PSEN}$ = 100 pF; load capacitance for all other ıts = 80 pF.

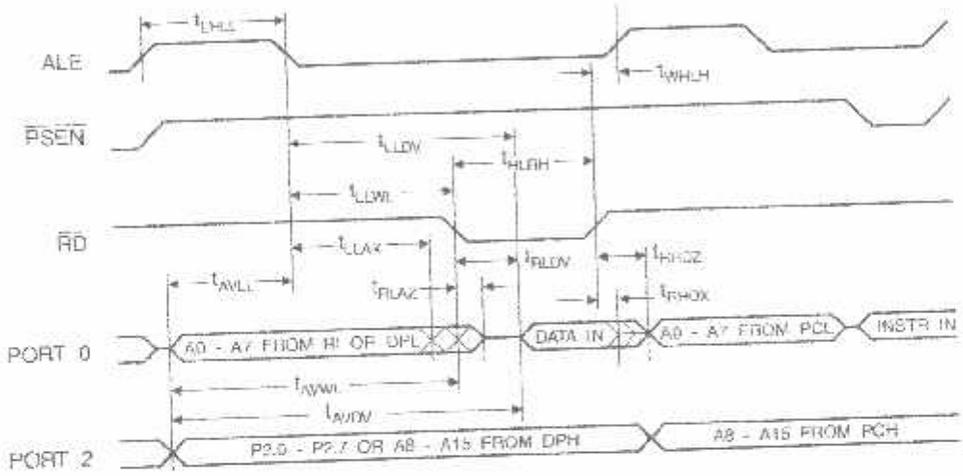
External Program and Data Memory Characteristics

ıbol	Parameter	12 MHz Oscillator		Variable Oscillator		Units
		Min	Max	Min	Max	
CL	Oscillator Frequency			0	33	MHz
	ALE Pulse Width	127		$2\ t_{CLCL}$-40		ns
	Address Valid to ALE Low	43		t_{CLCL}-25		ns
	Address Hold After ALE Low	48		t_{CLCL}-25		ns
	ALE Low to Valid Instruction In		233		$4\ t_{CLCL}$-65	ns
	ALE Low to $\overline{PSEN}$ Low	43		t_{CLCL}-25		ns
	$\overline{PSEN}$ Pulse Width	205		$3\ t_{CLCL}$-45		ns
	$\overline{PSEN}$ Low to Valid Instruction In		145		$3\ t_{CLCL}$-60	ns
	Input Instruction Hold After $\overline{PSEN}$	0		0		ns
	Input Instruction Float After $\overline{PSEN}$		59		t_{CLCL}-25	ns
	$\overline{PSEN}$ to Address Valid	75		t_{CLCL}-8		ns
	Address to Valid Instruction In		312		$5\ t_{CLCL}$-80	ns
	$\overline{PSEN}$ Low to Address Float		10		10	ns
	$\overline{RD}$ Pulse Width	400		$6\ t_{CLCL}$-100		ns
	$\overline{WR}$ Pulse Width	400		$6\ t_{CLCL}$-100		ns
	$\overline{RD}$ Low to Valid Data In		252		$5\ t_{CLCL}$-90	ns
	Data Hold After $\overline{RD}$	0		0		ns
	Data Float After $\overline{RD}$		97		$2\ t_{CLCL}$-28	ns
	ALE Low to Valid Data In		517		$8\ t_{CLCL}$-150	ns
	Address to Valid Data In		585		$9\ t_{CLCL}$-165	ns
	ALE Low to $\overline{RD}$ or $\overline{WR}$ Low	200	300	$3\ t_{CLCL}$-50	$3\ t_{CLCL}$+50	ns
	Address to $\overline{RD}$ or $\overline{WR}$ Low	203		$4\ t_{CLCL}$-75		ns
	Data Valid to $\overline{WR}$ Transition	23		t_{CLCL}-30		ns
	Data Valid to $\overline{WR}$ High	433		$7\ t_{CLCL}$-130		ns
	Data Hold After $\overline{WR}$	33		t_{CLCL}-25		ns
	$\overline{RD}$ Low to Address Float		0		0	ns
	$\overline{RD}$ or $\overline{WR}$ High to ALE High	43	123	t_{CLCL}-25	t_{CLCL}+25	ns

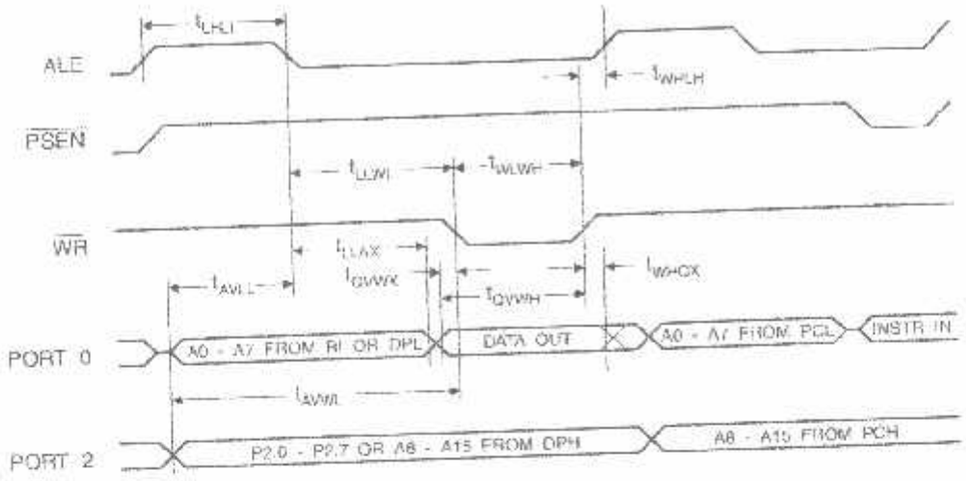
External Program Memory Read Cycle



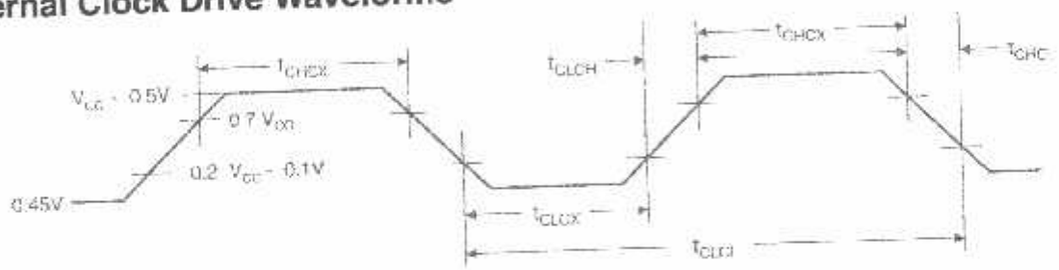
External Data Memory Read Cycle



External Data Memory Write Cycle



External Clock Drive Waveforms



External Clock Drive

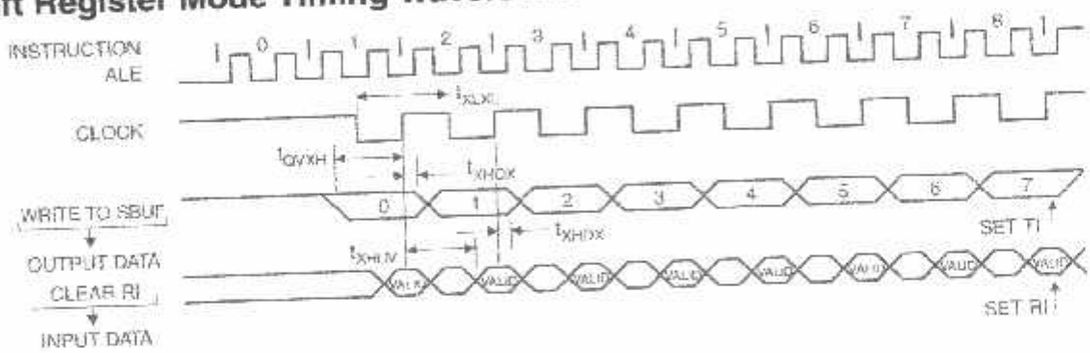
Symbol	Parameter	Min	Max	Units
1/t_CLCL	Oscillator Frequency	0	33	MHz
t_CLCL	Clock Period	30		ns
t_CHCX	High Time	12		ns
t_CLCX	Low Time	12		ns
t_CLCH	Rise Time		5	ns
t_CHCL	Fall Time		5	ns

Serial Port Timing: Shift Register Mode Test Conditions

Values in this table are valid for V_{CC} = 4.0V to 5.5V and Load Capacitance = 80 pF.

Symbol	Parameter	12 MHz Osc		Variable Oscillator		Units
		Min	Max	Min	Max	
	Serial Port Clock Cycle Time	1.0		12 t_{CLCL}		µs
	Output Data Setup to Clock Rising Edge	700		10 t_{CLCL}-133		ns
	Output Data Hold After Clock Rising Edge	50		2 t_{CLCL}-80		ns
	Input Data Hold After Clock Rising Edge	0		0		ns
	Clock Rising Edge to Input Data Valid		700		10 t_{CLCL}-133	ns

Shift Register Mode Timing Waveforms



AC Testing Input/Output Waveforms(1)

1. AC Inputs during testing are driven at V_{CC} - 0.5V for a logic 1 and 0.45V for a logic 0. Timing measurements are made at V_{IH} min. for a logic 1 and V_{IL} max. for a logic 0.

Float Waveforms(1)

1. For timing purposes, a port pin is no longer floating when a 100 mV change from load voltage occurs. A port pin begins to float when a 100 mV change from the loaded V_{OH}/V_{OL} level occurs.

Ordering Information

Standard Package

peed MHz)	Power Supply	Ordering Code	Package	Operation Range
24	4.0V to 5.5V	AT89S51-24AC AT89S51-24JC AT89S51-24PC AT89S51-24SC	44A 44J 40P6 42PS6	Commercial (0°C to 70°C)
		AT89S51-24AI AT89S51-24JI AT89S51-24PI AT89S51-24SI	44A 44J 40P6 42PS6	Industrial (-40°C to 85°C)
33	4.5V to 5.5V	AT89S51-33AC AT89S51-33JC AT89S51-33PC AT89S51-33SC	44A 44J 40P6 42PS6	Commercial (0°C to 70°C)

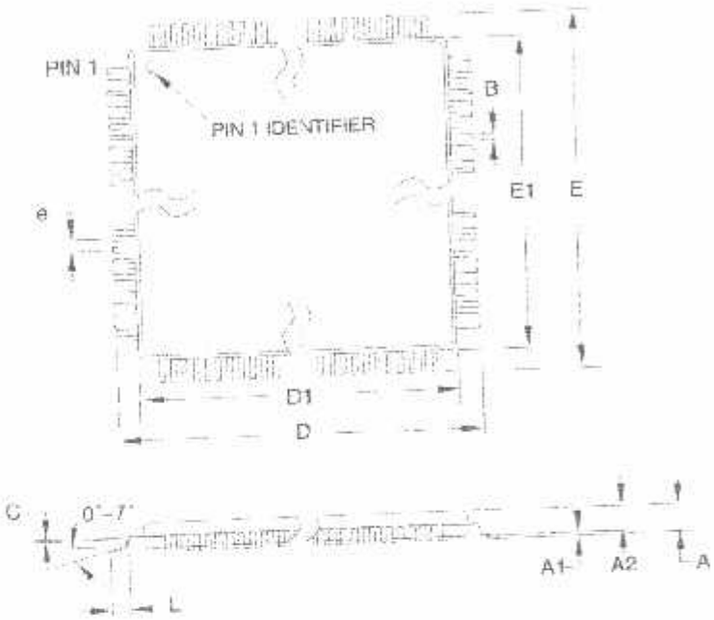
Green Package Option (Pb/Halide-free)

peed MHz)	Power Supply	Ordering Code	Package	Operation Range
24	4.0V to 5.5V	AT89S51-24AU AT89S51-24JU AT89S51-24PU	44A 44J 40P6	Industrial (-40°C to 85°C)

	Package Type
	44-lead, Thin Plastic Gull Wing Quad Flatpack (TQFP)
	44-lead, Plastic J-leaded Chip Carrier (PLCC)
	40-pin, 0.600" Wide, Plastic Dual Inline Package (PDIP)
6	42-pin, 0.600" Wide, Plastic Dual Inline Package (PDIP)

Packaging Information

44A – TQFP



COMMON DIMENSIONS
(Unit of Measure = mm)

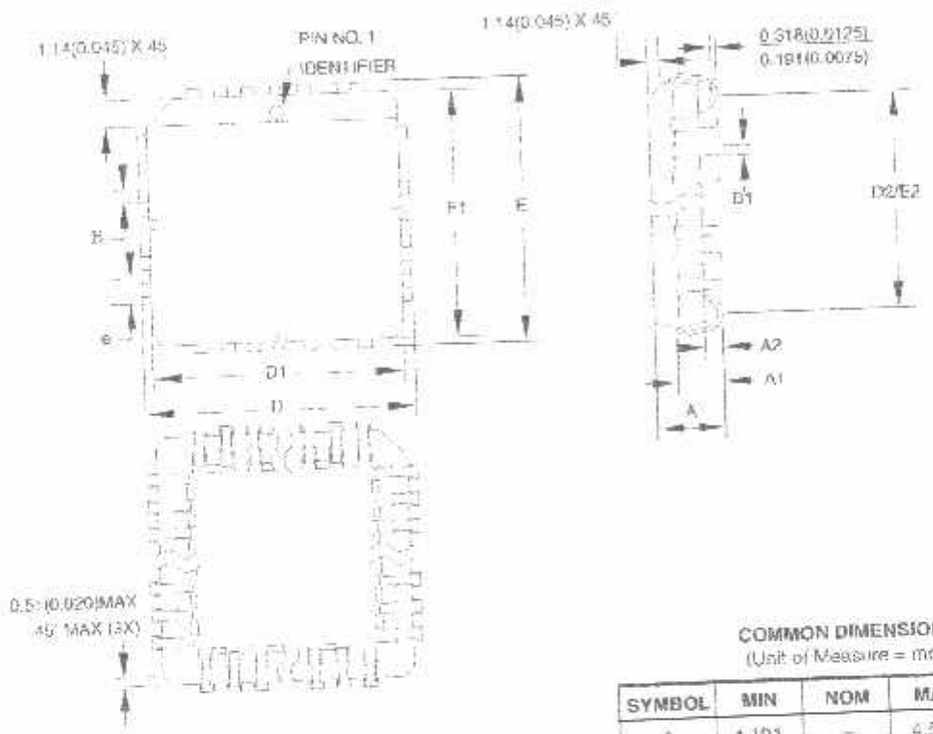
SYMBOL	MIN	NOM	MAX	NOTE
A	–	–	1.20	
A1	0.05	–	0.15	
A2	0.95	1.00	1.05	
D	11.75	12.00	12.25	
D1	9.90	10.00	10.10	Note 2
E	11.75	12.00	12.25	
E1	9.90	10.00	10.10	Note 2
B	0.30	–	0.45	
C	0.09	–	0.20	
L	0.45	–	0.75	
e	0.80 TYP			

Notes:
1. This package conforms to JEDEC reference MS-026, Variation ACB.
2. Dimensions D1 and E1 do not include mold protrusion. Allowable protrusion is 0.25 mm per side. Dimensions D1 and E1 are maximum plastic body size dimensions including mold mismatch.
3. Lead coplanarity is 0.10 mm maximum.

10/5/2001

	TITLE	DRAWING NO.	REV.
2325 Orchard Parkway San Jose, CA 95131	**44A**, 44-lead, 10 x 10 mm Body Size, 1.0 mm Body Thickness, 0.8 mm Lead Pitch, Thin Profile Plastic Quad Flat Package (TQFP)	44A	B

44J – PLCC



COMMON DIMENSIONS
(Unit of Measure = mm)

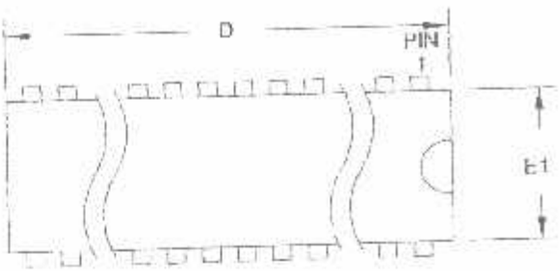
SYMBOL	MIN	NOM	MAX	NOTE
A	4.191	–	4.572	
A1	2.286	–	3.048	
A2	0.508	–		
D	17.399	–	17.653	
D1	16.510	–	16.662	Note 2
E	17.399	–	17.653	
E1	16.510	–	16.662	Note 2
D2/E2	14.986	–	16.002	
B	0.660	–	0.813	
B1	0.330	–	0.533	
e	1.270 TYP			

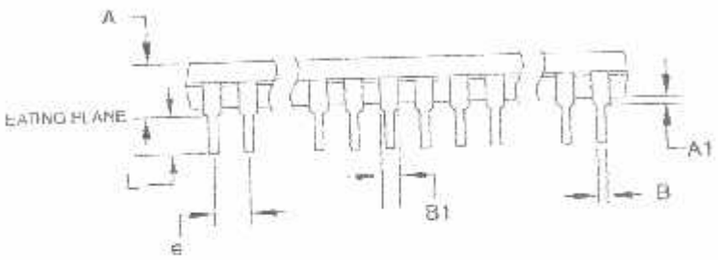
Notes:
1. This package conforms to JEDEC reference MS-018, Variation AC.
2. Dimensions D1 and E1 do not include mold protrusion. Allowable protrusion is .010"(0.254 mm) per side. Dimension D1 and E1 include mold mismatch and are measured at the extreme material condition at the upper or lower parting line.
3. Lead coplanarity is 0.004" (0.102 mm) maximum.

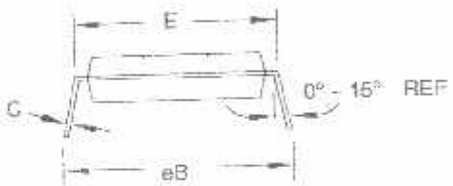
10/04/01

	TITLE	DRAWING NO.	REV.
2325 Orchard Parkway San Jose, CA 95131	**44J**, 44-lead, Plastic J-leaded Chip Carrier (PLCC)	44J	B

40P6 – PDIP







COMMON DIMENSIONS
(Unit of Measure = mm)

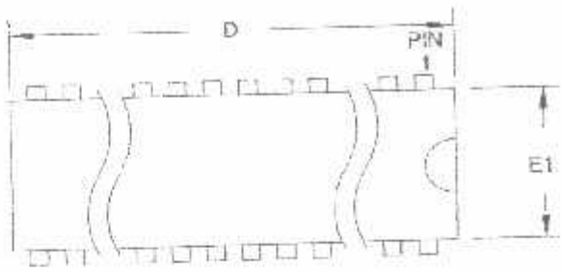
SYMBOL	MIN	NOM	MAX	NOTE
A	–	–	4.826	
A1	0.381	–	–	
D	52.070	–	52.578	Note 2
E	15.240	–	15.875	
E1	13.462	–	13.970	Note 2
B	0.356	–	0.559	
B1	1.041	–	1.651	
L	3.048	–	3.556	
C	0.203	–	0.381	
eB	15.494	–	17.526	
e	2.540 TYP			

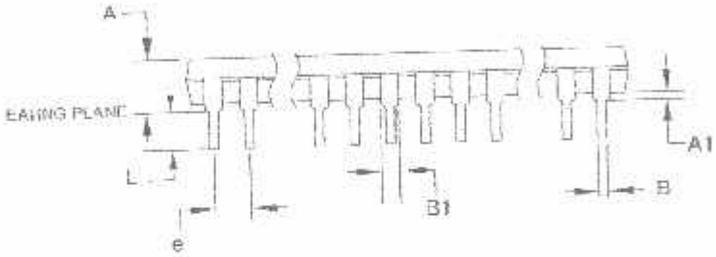
Notes:
1. This package conforms to JEDEC reference MS-011, Variation AC.
2. Dimensions D and E1 do not include mold Flash or Protrusion. Mold Flash or Protrusion shall not exceed 0.25 mm (0.010").

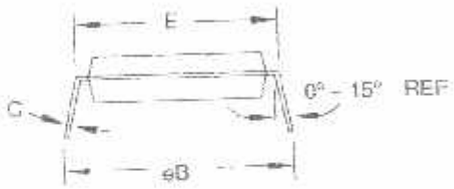
09/28/01

	TITLE	DRAWING NO.	REV.
2325 Orchard Parkway San Jose, CA 95131	**40P6**, 40-lead (0.600"/15.24 mm Wide) Plastic Dual Inline Package (PDIP)	40P6	B

42PS6 – PDIP







COMMON DIMENSIONS
(Unit of Measure = mm)

SYMBOL	MIN	NOM	MAX	NOTE
A	–	–	4.83	
A1	0.51	–	–	
D	36.70	–	36.96	Note 2
E	15.24	–	15.88	
E1	13.46	–	13.97	Note 2
B	0.38	–	0.56	
B1	0.76	–	1.27	
L	3.05	–	3.43	
C	0.20	–	0.30	
eB		–	15.55	
e	1.78 TYP			

Notes:
1. This package conforms to JEDEC reference MS-011, Variation AC.
2. Dimensions D and E1 do not include mold Flash or Protrusion. Mold Flash or Protrusion shall not exceed 0.25 mm (0.010").

11/6/03

	TITLE	DRAWING NO.	REV.
2325 Orchard Parkway San Jose, CA 95131	**42PS6**, 42-lead (0.600"/15.24 mm Wide) Plastic Dual Inline Package [PDIP]	42PS6	A

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DATA SHEET

PCF8591
8-bit A/D and D/A converter

2003 Jan 27

Product specification
Supersedes data of 2001 Dec 13

Philips
Semiconductors

PHILIPS

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FEATURES

Single power supply

Operating supply voltage 2.5 V to 6 V

Low standby current

Serial input/output via I^2C-bus

Address by 3 hardware address pins

Sampling rate given by I^2C-bus speed

4 analog inputs programmable as single-ended or differential inputs

Auto-incremented channel selection

Analog voltage range from V_{SS} to V_{DD}

On-chip track and hold circuit

8-bit successive approximation A/D conversion

Multiplying DAC with one analog output.

APPLICATIONS

Closed loop control systems

Low power converter for remote data acquisition

Battery operated equipment

Acquisition of analog values in automotive, audio and TV applications.

3 GENERAL DESCRIPTION

The PCF8591 is a single-chip, single-supply low power 8-bit CMOS data acquisition device with four analog inputs, one analog output and a serial I^2C-bus interface. Three address pins A0, A1 and A2 are used for programming the hardware address, allowing the use of up to eight devices connected to the I^2C-bus without additional hardware. Address, control and data to and from the device are transferred serially via the two-line bidirectional I^2C-bus.

The functions of the device include analog input multiplexing, on-chip track and hold function, 8-bit analog-to-digital conversion and an 8-bit digital-to-analog conversion. The maximum conversion rate is given by the maximum speed of the I^2C-bus.

ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
CF8591P	DIP16	plastic dual in-line package; 16 leads (300 mil)	SOT38-4
CF8591T	SO16	plastic small outline package; 16 leads; body width 7.5 mm	SOT162-1

BLOCK DIAGRAM

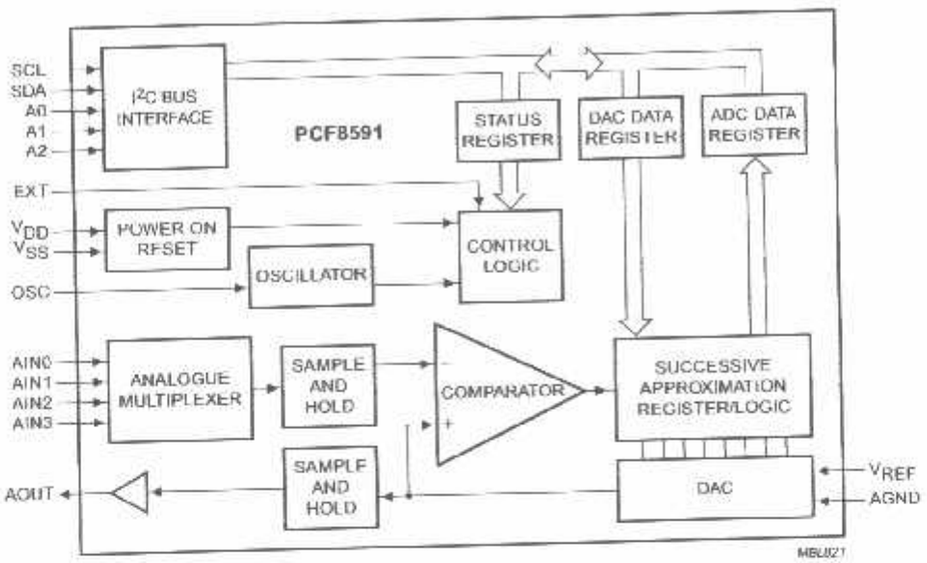

Fig.1 Block diagram.

PINNING

SYMBOL	PIN	DESCRIPTION
IN0	1	analog inputs (A/D converter)
IN1	2	
IN2	3	
IN3	4	
0	5	hardware address
1	6	
2	7	
SS	8	negative supply voltage
DA	9	I²C-bus data input/output
CL	10	I²C-bus clock input
SC	11	oscillator input/output
XT	12	external/internal switch for oscillator input
GND	13	analog ground
REF	14	voltage reference input
OUT	15	analog output (D/A converter)
DD	16	positive supply voltage

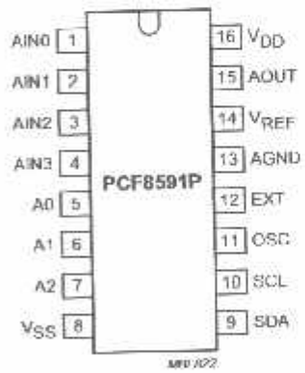

Fig.2 Pinning diagram (DIP16).

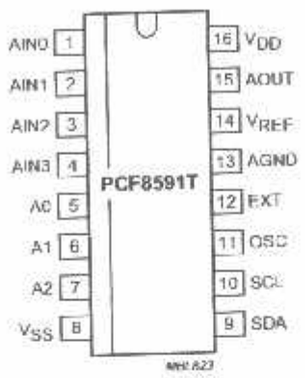

Fig.3 Pinning diagram (SO16).

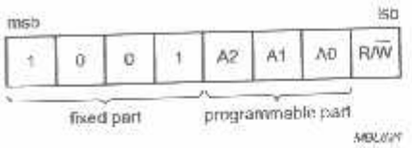

Fig.4 Address byte.

FUNCTIONAL DESCRIPTION

Addressing

ch PCF8591 device in an I²C-bus system is activated by ɔding a valid address to the device. The address ɔsists of a fixed part and a programmable part. The ɔgrammable part must be set according to the address ıs A0, A1 and A2. The address always has to be sent as ; first byte after the start condition in the I²C-bus ɔtocol. The last bit of the address byte is the ıd/write-bit which sets the direction of the following data nsfer (see Figs 4, 16 and 17).

7.2 Control byte

The second byte sent to a PCF8591 device will be stored in its control register and is required to control the device function. The upper nibble of the control register is used for enabling the analog output, and for programming the analog inputs as single-ended or differential inputs. The lower nibble selects one of the analog input channels defined by the upper nibble (see Fig.5). If the auto-increment flag is set, the channel number is incremented automatically after each A/D conversion.

If the auto-increment mode is desired in applications where the internal oscillator is used, the analog output enable flag in the control byte (bit 6) should be set. This allows the internal oscillator to run continuously, thereby preventing conversion errors resulting from oscillator start-up delay. The analog output enable flag may be reset at other times to reduce quiescent power consumption.

The selection of a non-existing input channel results in the highest available channel number being allocated. Therefore, if the auto-increment flag is set, the next selected channel will be always channel 0. The most significant bits of both nibbles are reserved for future functions and have to be set to logic 0. After a Power-on reset condition all bits of the control register are reset to logic 0. The D/A converter and the oscillator are disabled for power saving. The analog output is switched to a high-impedance state.

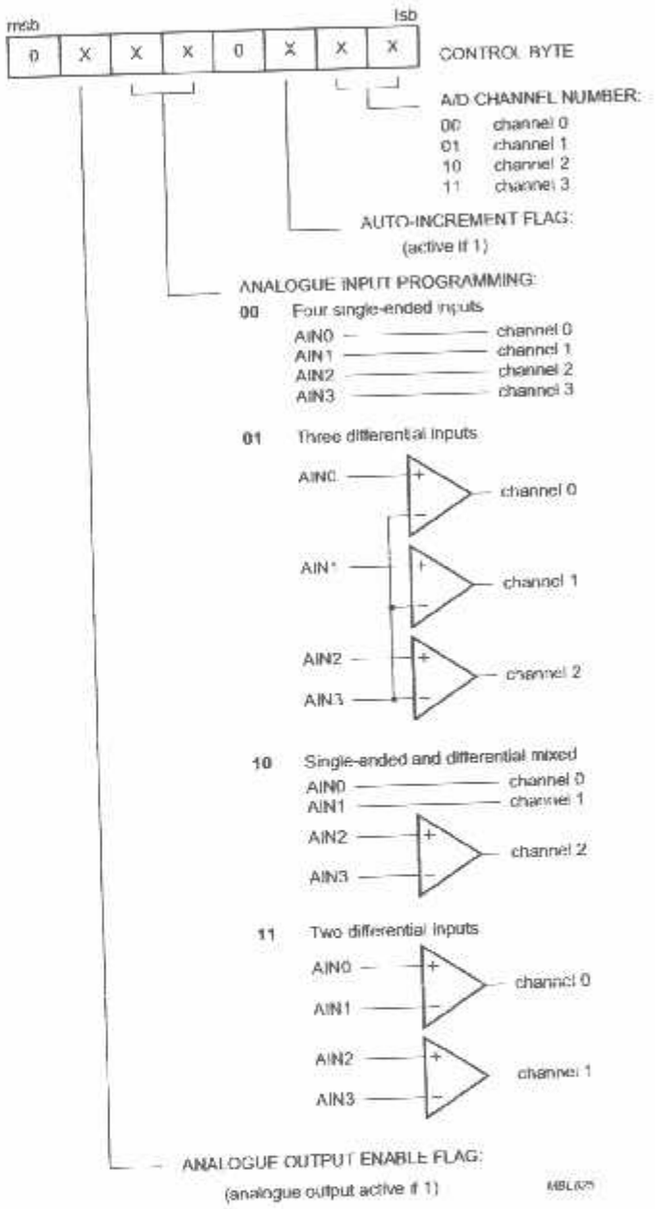

Fig.5 Control byte.