SKRIPSI

PERANCANGAN DAN PEMBUATAN KOMUNIKASI MENGGUNAKAN SANDI MORSE BERBASIS MIKROKONTROLLER AT89S51

Disusun Oleh :

YURI DARMAWAN

03.17.099

JURUSAN TEKNIK ELEKTRO S-1
KONSENTRASI TEKNIK ELEKTRONIKA
FAKULTAS TEKNOLOGI INDUSTRI
INSTITUT TEKNOLOGI NASIONAL MALANG

2009

LEMBAR PERSETUJUAN

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SKRIPSI

Disusun Dan Diajukan Sebagai Salah Satu Syarat Untuk Memperoleh Gelar Sarjana Teknik Elektronika Strata Satu (S-1)

Disusun Oleh:

YURI DARMAWAN

03.17.099

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INSTITUT TEKNOLOGI NASIONAL
FAKULTAS TEKNOLOGI INDUSTRI
JURUSAN TEKNIK ELEKTRO S-1
KONSENTRASI TEKNIK ELEKTRONIKA

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PENDAHULUAN

1.1. Latar Belakang

Dampak perkembangan teknologi dibidang elektronika telah banyak membawa perubahan dan kemajuan yang begitu cepat dan canggih. Hal ini dibuktikan dengan adanya penemuan – penemuan baru di segala bidang teknologi mulai dari peralatan rumah tangga, industri, sampai pada teknologi bidang luar angkasa. Pesatnya perkembangan teknologi menghasilkan berbagai penemuan dan terobosan – terobosan baru dibidang mikrokontroller yang semakin banyak membantu tugas – tugas para ilmuan dalam melakukan penelitian – penelitian di berbagai bidang.

Di dalam perkembangannya, mikrokontroller banyak diterapkan dalam perancangan elektronika karena mikrokontroller memiliki sistem pengaturan dan pengontrolan yang otomatis dan praktis. Keefektifan mikrokontroller inilah yang diperlukan manusia dalam menunjang rutinitas, baik dalam proses produksi maupun dalam kehidupan schari – hari pada umumnya. Misalnya pada kepramukaan yaitu adanya sandi *morse* yang berfungsi untuk memberikan tanda dengan bunyi suara.

Untuk itu penulis berusaha untuk merancang dan membuat suatu alat yang berfungsi untuk berkomunikasi dengan menggunakan sandi *morse* secara digital. Sandi *morse* adalah suatu sandi yang dimana mempunyai karakter huruf yang direpresentasikan dengan bunyi, huruf yang berbeda bunyinya berbeda juga. Kebanyakan orang pada saat ini banyak yang kurang mengerti dengan sandi

Berikut ini adalah sandi *morse* yang telah disepakati bersama.

Kode representasi sandi *morse* :

Alfabet :

- Huruf **A** direpresentasikan dengan .-
- Huruf **B** direpresentasikan dengan -...
- Huruf **C** direpresentasikan dengan -.-.
- Huruf **D** direpresentasikan dengan -..
- Huruf **E** direpresentasikan dengan .
- Huruf **F** direpresentasikan dengan ..-.
- Huruf **G** direpresentasikan dengan --.
- Huruf **H** direpresentasikan dengan ....
- Huruf **I** direpresentasikan dengan ..
- Huruf **J** direpresentasikan dengan .---
- Huruf **K** direpresentasikan dengan -.-
- Huruf **L** direpresentasikan dengan .-..
- Huruf **M** direpresentasikan dengan --
- Huruf **N** direpresentasikan dengan -.
- Huruf **O** direpresentasikan dengan ---
- Huruf **P** direpresentasikan dengan .--.
- Huruf **Q** direpresentasikan dengan --.-
- Huruf **R** direpresentasikan dengan .-.
- Huruf **S** direpresentasikan dengan ...
- Huruf **T** direpresentasikan dengan -
- Huruf **U** direpresentasikan dengan ..-

- Huruf **V** direpresentasikan dengan ...-
- Huruf **W** direpresentasikan dengan .--
- Huruf **X** direpresentasikan dengan -..-
- Huruf **Y** direpresentasikan dengan -.--
- Huruf **Z** direpresentasikan dengan --..

Tanda Baca :

- Tanda . direpresentasikan dengan .-.-.-
- Tanda , direpresentasikan dengan --..--
- Tanda : direpresentasikan dengan ---...
- Tanda - direpresentasikan dengan -....-
- Tanda / direpresentasikan dengan -..-.

Angka :

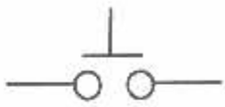
- 1 direpresentasikan dengan .----
- 2 direpresentasikan dengan ..---
- 3 direpresentasikan dengan ...--
- 4 direpresentasikan dengan ....-
- 5 direpresentasikan dengan .....
- 6 direpresentasikan dengan -....
- 7 direpresentasikan dengan --...
- 8 direpresentasikan dengan ---..
- 9 direpresentasikan dengan ----.
- 0 direpresentasikan dengan -----

Samuel Finley Breese Morse dilahirkan 218 tahun yang lalu atau tepatnya pada tanggal 27 April 1791 di *Charlestown, Massachusetts*. Selain dikenal sebagai penemu, *Morse* juga seorang pelukis. Ia dikenal atas penemuan telegraf listrik. Bersama asistennya, *Alexander Bain*, ia menciptakan alfabet khusus untuk digunakan di telegraf yang disebut sandi *Morse*. *Morse* mendapat ilham untuk membuat telegrafi elektrik ketika melihat seorang penumpang di kapal yang ia tumpangi memperagakan elektromagnet. Ia memproduksi telegraf listrik pertama yang digunakan pada 1835. Pada 24 Mei 1844 ia mengirimkan pesan pertama melalui telegraf Amerika, dari Washington ke Baltimore. Sandi *Morse*-nya adalah *What hath God wrought*, yang berarti 'Apakah Tuhan telah menulis?' *Morse* hidup sampai usia lanjut. Ia sempat menyaksikan saluran telegraf dipasang di seluruh bagian dunia termasuk kabel-kabel bawah laut. Pada ulang tahunnya yang kedelapan puluh, sebuah patung dirinya diresmikan di *Central Park, New York*, sebagai penghargaan atas jasa-jasanya.

Dengan berkembang pesatnya alat komunikasi dan teknologi saat ini, maka tidak heran jika sandi *morse* sangat dikenal disceluruh dunia untuk keperluan navigasi pelayaran, pesawat udara, serta komunikasi militer dan bahkan Hams Radio operator. Sebegitu pentingnya peranan sandi *morse* dalam dunia komunikasi baik itu dunia pelayaran, udara, radio – radio, maupun komunikasi militer, maka tak heran kalau kita sebagai anggota Pramuka seharusnya bangga karena dalam ilmu kepramukaan, anggota Pramuka diharuskan untuk memahami dan menerapkan sandi *morse* sebagai salah satu cara untuk menyampaikan berita.

2.2 *Switch Push Button*

Push button merupakan *mikro switch* yang digunakan sebagai inputan atau pemberi sinyal sandi *morse* kepada mikrokontroller untuk diproses sesuai dengan program yang telah dibuat.



Gambar 2.1 *Push Button*

2.3. Mikrokontroler AT89S51

2.3.1. Pendahuluan

Perbedaan mendasar antara mikrokontroller dan mikroprosesor adalah mikrokontroller selain memiliki CPU juga dilengkapi memori dan *input output* yang merupakan kelengkapan sebagai sistem minimum mikrokomputer, sehingga sebuah mikrokontroller dapat dikatakan sebagai mikrokomputer dalam keping tunggal *(Single Chip Microcomputer)* yang dapat berdiri sendiri.

Mikrokontroller AT89S51 adalah mikrokontroller ATMEL yang kompatibel penuh dengan mikrokontroler keluarga MCS – 51, membutuhkan daya rendah, memiliki performance yang tinggi dan merupakan mikrokomputer 8 bit yang dilengkapi 4 Kbyte EEPROM *(Electrical Erasable and Programmable Read Only Memory)* dan 128 Byte RAM *internal*. Program memori dapat diprogram berulang–ulang atau dengan menggunakan *Programmer Nonvolatile Memory*.

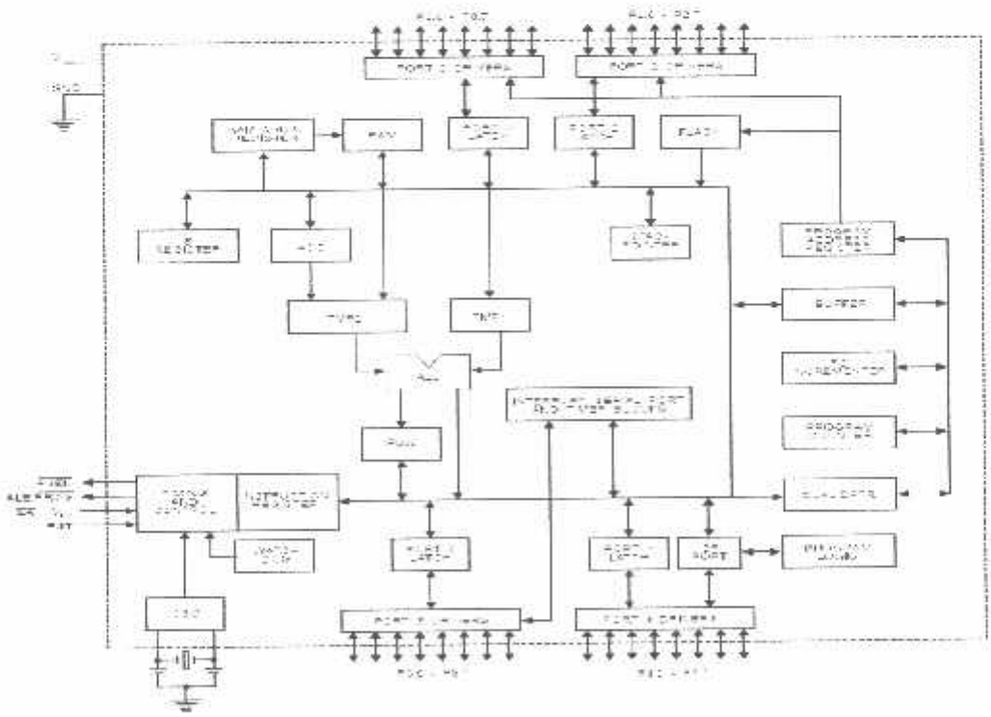
Dalam sistem mikrokontroller terdapat dua hal yang mendasar, yaitu: perangkat lunak dan perangkat keras yang keduanya saling terkait dan mendukung.

2.3.2. Perangkat keras mikrokontroler AT89S51

Secara umum Mikrokontroller AT89S51 memiliki :

- CPU 8 bit termasuk keluarga MCS-51
- 4 Kb *Flash memory*
- 128 *byte Internal* RAM
- 4 buah *Port* I/O, masing – masing terdiri atas 8 jalur I/O
- 2 *Timer/ counter* 16 bit
- 1 *Serial Port Full Duplex*
- Kecepatan pelaksanaan intruksi per siklus 1 µs pada frekuensi *clock* 12 Mhz

Dengan keistimewaan diatas pembuatan alat menggunakan AT89S51 menjadi lebih sederhana dan tidak memerlukan IC pendukung yang banyak. Adapun Blok Diagram dari Mikrokontroler AT89S51 adalah sebagai berikut:



Gambar 2.2 Blok Diagram Mikrokontroler AT89S51[7]

2.3.3. Konfigurasi Pin-Pin Mikrokontroler AT89S51.

Mikrokontroller AT89S51 terdiri dari 40 pin dengan konfigurasi sebagai berikut:

Gambar 2.3 Konfigurasi Pin-Pin AT89S51[7]

Fungsi tiap pin-nya adalah sebagai berikut :

1. **GND** (Pin 20)

   Dihubungkan dengan *Ground* Rangkaian.

2. **VCC** (Pin 40)

   Dihubungkan dengan sumber tegangan +5V.

3. **Port 0** (P0.0-P0.7) (Pin 32-39)

   Port 0 (P0.0 – P0.7) merupakan port I/O 8 bit dua arah. Port ini digunakan sebagai multipleks bus alamat rendah (A0 – A7) dan bus data selama pengaksesan ke memori eksternal.

4. **Port 1** (P1.0 -P1.7) (Pin 1-8)

   Merupakan port *input – output* dua arah dengan *pull-up*. Port ini berfungsi sebagai *input* atau *output* dan bekerja baik untuk operasi bit maupun *byte*, tergantung dari pengaturan *software*.

5. **Port 2** (P2.0 -P2.7) (Pin 21-28)

Port 2 (P2.0 – P2.7) merupakan *input – output* dua arah dengan *pull-up*. Port 2 mengeluarkan *high order address byte* selama pengambilan (*fetch*) program memori eksternal dan selama mengakses data memori eksternal. Port 2 juga menerima *high order address bit* dan beberapa sinyal kontrol selama pemrograman dan verifikasi.

6. **Port 3** (P3.0-P3.7) (Pin 10-17)

Merupakan port input-output dengan internal pull-up, dimana Port 3 juga memiliki fungsi khusus dan dapat dilihat pada tabel berikut ini:

Tabel 2.1 Fungsi Khusus Pada Port 3.

Pin Port	**Fungsi Khusus**
Port 3.0	RxD (Port masukan serial)
Port 3.1	TxD (Port keluaran Serial)
Port 3.2	$\overline{\text{INT0}}$ (Masukan Interupsi Eksternal 0)
Port 3.3	$\overline{\text{INT1}}$ (Masukan Interupsi Eksternal 1)
Port 3.4	T0 (Masukan Pewaktu Eksternal 0)
Port 3.5	T1 (Masukan Pewaktu Eksternal 1)
Port 3.6	$\overline{\text{WR}}$ (sinyal tulis memori data eksternal)
Port 3.7	$\overline{\text{RW}}$ (sinyal baca memori data eksternal)

7. **RST (Reset),** pin 9.

Input *reset* merupakan *reset master* untuk AT89S51.

8. **ALE / Prog (*Address Latch Enable*)**, pin 30.

   Digunakan untuk menahan alamat memori eksternal selama pelaksanaan intruksi.

9. **PSEN (Program *Strobe Enable*)**, pin 29.

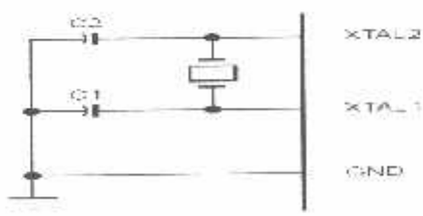
   Merupakan sinyal pengontrol yang memperbolehkan program memori eksternal masuk kedalam bus.

10. **EA / VPP (*External Access*)**, pin 31.

    Dapat diberikan logika rendah (*Ground)* atau logika tinggi (+5V). Jika diberikan logika tinggi maka mikrokontroler akan mengakses program dari ROM internal (EEPROM/*Flash* Memori), dan jika diberikan logika rendah maka mikrokontroler akan mengakses program dari memori eksternal.

11. **X-TAL 1 dan X-TAL 2,** pin 19, 18.

    Pin ini dihubungkan dengan kristal bila menggunakan osilator internal. X-TAL 1 merupakan masukan ke rangkaian osilator internal sedangkan X-TAL 2 keluaran dari rangkaian osilator internal . Untuk keperluan ini diperlukan kapasitor penstabil sebesar 30pF. Dan nilai dari X-TAL tersebut antara 4 – 24 Mhz. Untuk lebih jelasnya dapat dilihat gambar pemasangan X-TAL serta kapasitor yang digunakannya.



Gambar 2.4 Osilator AT89S51[7]

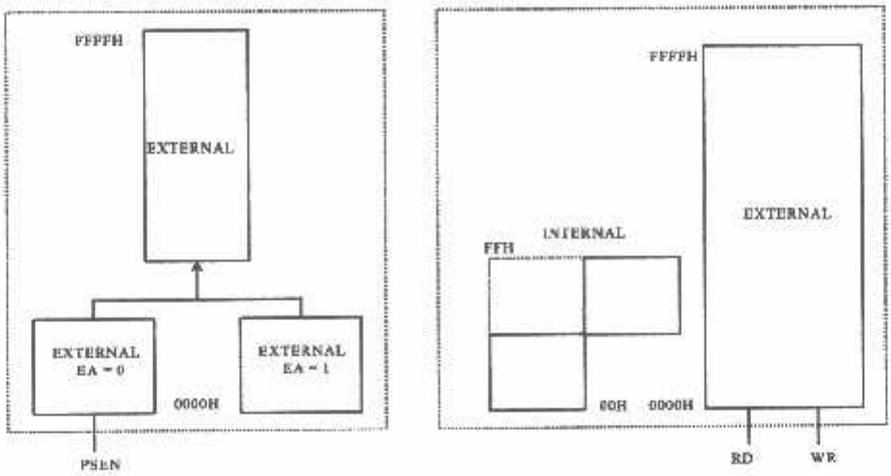
2.3.4. Organisasi Memory.

Organisasi memori pada mikrokontroler AT89S51 dapat dibagi menjadi dua bagian besar yaitu memori program dan memori data. Pembagian tersebut didasarkan atas fungsi dari penyimpanan data maupun program. Memori program digunakan untuk menyimpan instruksi-instruksi yang akan dijalankan oleh mikrokontroler, sedangkan memori data digunakan sebagai tempat yang sedang diolah mikrokontroler.

Program mikrokontroler disimpan dalam memori program berupa ROM. Mikrokontroler 89S51 dilengkapi dengan ROM internal, sehingga untuk menyimpan program tidak digunakan ROM eksternal yang terpisah dari mikrokontroler. Agar tidak menggunakan memori program eksternal, EA (*Eksternal Address enable*) dihubungkan dengan Vcc.

Memori program mikrokontroler menggunakan alamat 16 bit mulai 0000H-FFFFH, sehingga kapasitas penyimpanan program maksimal adalah 4Kb. Sinyal /PSEN (*Program Store Enable*) tidak digunakan jika digunakan memori program internal.

Selain memory program mikrokontroler 89S51 juga memiliki data internal 128 *byte* dan mampu mengakses memori data eksternal sebesar 64 Kb. Semua memori data internal dapat dialamati dengan data langsung atau tidak langsung. Ciri dari pengalamatan langsung adalah *operand* alamat *register* yang berisi alamat data yang akan diolah. Sebagian memori tersebut dapat dialamati dengan pengalamatan register, dan sebagian lagi dapat dialamati dengan memori satu bit. Untuk membaca data digunakan sinyal /RD sedangkan untuk menulis digunakan sinyal /RW.

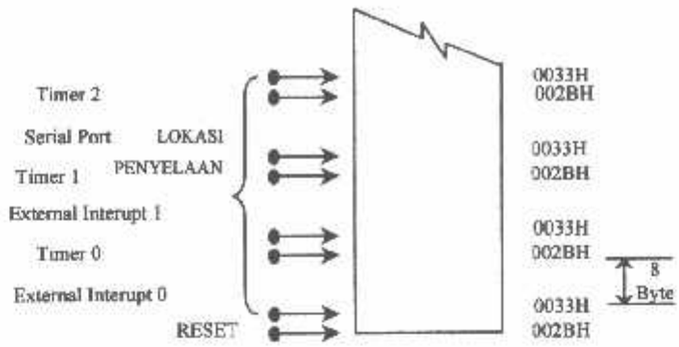


Gambar 2.5 Struktur memori AT89S51

Memori program dalam hanya dapat dibaca dan dapat mencapai 4 Kbyte dengan jenis *flash ISP (In-System Programing)* yang dapat diprogram. Kapasitas memori bagian dalam AT89S51 sebanyak 128 byte, terdiri dari memori (*RAM*) dan register fungsi khusus (*Special Fungtion Register/SFR*).

2.3.5. Memori Program

AT89S51 memiliki memori program dalam 4 Kbyte dengan alamat 0000H s/d FFFFH yang dapat diaktifkan jika EA dihubungkan ke Vcc, alamat selebihnya secara otomatis dibaca dari luar, bagian terendah memori program dipakai untuk vektor penyelaan seperti gambar 2.6.



Gambar 2.6 Arah penyelaan pada memori program[14]

Batas ruang yang diberikan dari masing-masing arah penyelaan sebesar 8 byte. Untuk mengakses memori program luar dipakai $\overline{\text{PSEN}}$ sedangkan pada pengaksesan memori dalam tidak digunakan.

16 buah I/O (P0 dan P2) dipakai sebagai bus selama berhubungan dengan memori program luar. P0 untuk bus data/alamat *byte* rendah secara bergantian (*multipleks*), awalnya mengeluarkan *byte* rendah dari program counter sebagai alamat kemudian menjadi ambang sambil menunggu *byte* kode dari memori program.

Saat *byte* rendah sudah siap di P0 sinyal $\overline{\text{ALE}}$ akan memindahkan kode *byte* ke penahan alamat *(address latch)*. Pada saat yang sama P2 mengeluarkan Program Counter *byte* tinggi, kemudian $\overline{\text{PSEN}}$ mengirim sinyal sehingga mikro membaca kode *byte*. Alamat program memori yang dikeluarkan selalu 16 bit meskipun jumlah memori program yang digunakan kurang dari 64 Kbyte.

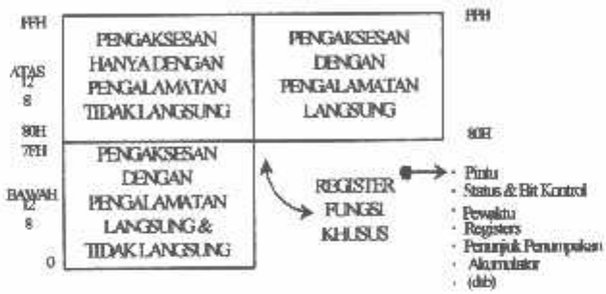
2.3.6. Memori Data

Memori data mikrokontroler AT89S51 memungkinkan memori data untuk diakses alamat 8 bit. Sekalipun demikian, alamat data memori 16 bit dapat

dihasilkan melalui register *DPTR* (*Data Pointer Register*). Memori data terbagi menjadi dua, yaitu memori data dalam dan memori data luar :

2.3.6.1. Memori Data Dalam

Memori data dalam dibagi menjadi 3 blok yaitu meliputi 128 byte rendah, 128 byte tinggi dan SFR seperti ditunjukkan pada gambar 2.7.



Gambar 2.7 Pembagian blok memori data dalam[14]

Pengalamatan memori data dalam selalu menggunakan 1 byte sehingga alamat memori maksimal yang dapat dihubungkan hanya sebatas 256 byte.

RAM dalam 128 byte bagian bawah dibagi atas 3 bagian :

1. Empat register bank, masing-masing terdiri 8 register yang diberi nama R0...R7 dengan alamat 00H s/d 1FH.
2. Bit alamat sebanyak 16 byte yaitu RAM dalam yang dapat dialamati secara byte atau bit dengan alamat 20H sampai dengan 1FH.
3. RAM serbaguna 80 byte dengan alamat 30H s/d 7FH.

RAM internal bagian atas digunakan sebagai register fungsi khusus yang disebut SFR (*Special Function Register*) yaitu register yang berhubungan dengan fasilitas-fasilitas perangkat keras pada mikrokontroler AT89S51. Register fungsi

khusus (SFR) hanya dapat dialamati secara pengalamatan langsung dan sebagian register SFR dapat dialamati secara byte maupun bit.

Berikut ini dibahas secara singkat fungsi dan sifat masing-masing register dalam register fungsi khusus (SFR):

1. Port 0, Port 1, Port 2, dan Port 3

   P0, P1, P2 dan P3 masing-masing menempati lokasi 80H, 90H, A0H, dan B0H, merupakan pengunci (*latches*), yang digunakan untuk menyimpan data yang akan dibaca atau ditulis dari atau ke Port, untuk masing-masing P0, P1, P2 dan P3.

2. SP (*Stack Pointer*)

   Merupakan register 8 bit (lokasi 81H) digunakan dalam proses simpan dan ambil dari atau ke *stack*. Nilai dari *stack pointer* akan bertambah bila diberi perintah *push* dan akan berkurang bila diberi perintah *pop*. Lokasi dari *stack pointer* ditentukan dengan *software*.

3. DPTR (*Data Pointer*)

   Merupakan register 16 bit yang berfungsi untuk mengakses lokasi kode alamat dan lokasi alamat memori eksternal. DPTR terdiri dari dua buah register yaitu DPH untuk bit tinggi dan DPL untuk bit rendah, masing-masing berada di lokasi 83H dan 82H.

4. PCON (*Power Control*)

   Merupakan register yang berguna untuk mengatur kebutuhan daya yang memungkinkan mikrokontroler ke dalam mode *idle* atau *sleep* yang mana akan lebih menghemat pemakaian daya. Selain itu pada PCON juga terdapat register untuk mengatur *Baud Rate* pada serial port.

5. Register Timer

Merupakan register yang berfungsi sebagai pengatur ragam kerja pewaktu/pencacah pada mikrokontroler AT89S51. Register ini mempunyai dua buah 16 bit *timer/counter*, yaitu timer 0dan timer 1. timer 0 terletak di alamat 8AH untuk TL0 dan 8CH untuk TH0 dan timer 1 terletak di alamat 8BH untuk TL1 dan 8DH untuk TH1.

6. AUXR (*Auxiliary Register*)

Merupakan register tambahan dengan lokasi 8EH, yang digunakan untuk mengatur sendiri bit *Interrupt Enable* pada register IE (*Interrupt Enable*). Register ini berisi Bit (*Diseble/Enable ALE*), DISTRO (*Diseble/Enable Reset Out*) dan WDIDLE (*Diseble/Enable* WDT dalam Mode *Idle*)

7. Serial Port UART (*Universal Asynchronous Receiver/Transmiter*)

Serial Port ini di kontrol oleh beberapa registrasi yaiatu SCON (*Serial Port Control*) yang beralamat di 98H SBUF berlokasi pada alamat 99H, yang berfungsi menampung data sementara dari hasil penerimaan atau pengiriman data serial dari atau ke terminal data serial. Setelah serial port di konfigurasi (mode operasi dan *baut rate*), maka penulisan ke SBUF akan memulai pengiriman secara serial. Untuk dapat menggunakan serial port ini maka harus mengetahi bit-bit SFR yang bersangkutan.

8. AUXR1 (*Auxiliary Register 1*)

Merupakan register tambahan berlokasi A2H, digunakan untuk memilih DPTR (*Data Pointer Register Select*), bila DPS=0, maka DPTR yang digunakan DP0L, DP0H, dan bila DPS=1, yang digunakan DP1L, DP1H.

2.3.6.2. Memori Data Luar

Mikrokontroler AT89S51 memiliki program yang di baca dari *Flash* memori data luar, oleh karena itu Port 0 berfungsi sebagai alamat atau data yang terpilih untuk RAM dan baris 3 port 2 digunakan sebagai alamat jumlah dari RAM CPU mengeluarkan sinyal RD dan WR selama berhubungan dengan memori data luar. Kapasitas dari memori data luar yang di hubungkan dapat mencapai 64Kbyte.

2.3.7. Metode Pemprograman

Mikrokontroler AT89S51 mampu di program pada mode *high voltage* (12V) melalui mode *parallel programming*, adapun mode *low voltage* (5V) melalui mode *serial programming*. Pemprograman *Flash* mode serial dapat di program menggunakan antar muka ISP serial dengan menghubungkan RST ke VCC. Antarmuka ini terdiri dari SCK, MOSI sebagai masukan dan MISO sebagai keluaran . setelah RST di set tinggi, interupt pengaktifan pemprograman perlu untuk dieksekusi sebelum operasi lain dapat dieksekusi. Frekuensi serial SCK maksimum kurang dari 1/16 dari frekuensi kristal. Apabila detak osilator 33 MHz frekuensi SCK maksimum adalah 2 MHz. Pemprograman mode serial dapat di lihat pada gambar 2.8.

Proses pemprogaman secara serial adalah sebagai berikut :

1. Urutan Power-Up

   Berikan catu daya pada penyemat VCC dan Ground, set penyemat reset ke tinggi, jika kristal tidak di pasang pada XTAL1 dan XTAL2 maka diberi detak 3MHz sampai 33 MHz dan tunggu selama 10 milidetik sampai detak siap.

2. Pengaktifan

Aktifkan *Serial Programming* dengan mengirim instruksi pengktif pemprograman serial pada penyemat MOSI/P1.5. Frekuensi untuk penggeseran (*shift)*) diberikan pada penyemat SCK/P1.7.

3. Pemprograman

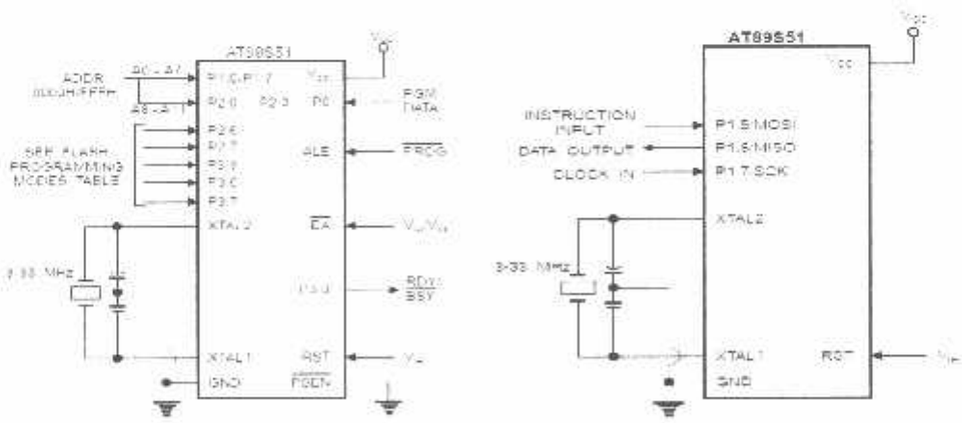
Array kode di program 1 byte pada waktu yang sama dalam mode byte atau *page* manapun.

4. Vertifikasi

Suatu lokasi memori dapat di verifikasi sendiri dengan menggunakan instruksi pembacaan yang mengirimkan data pada alamat tepilih melalui penyemat MISO/P1.6 secara serial.

5. Urutan Power-Off

Set XTAL1 ke rendah (jika tidak ada kristal yang terpasang). Buat RST ke rendah untuk membuat operasi mikrokontroler menjadi normal serta matikan catu daya.

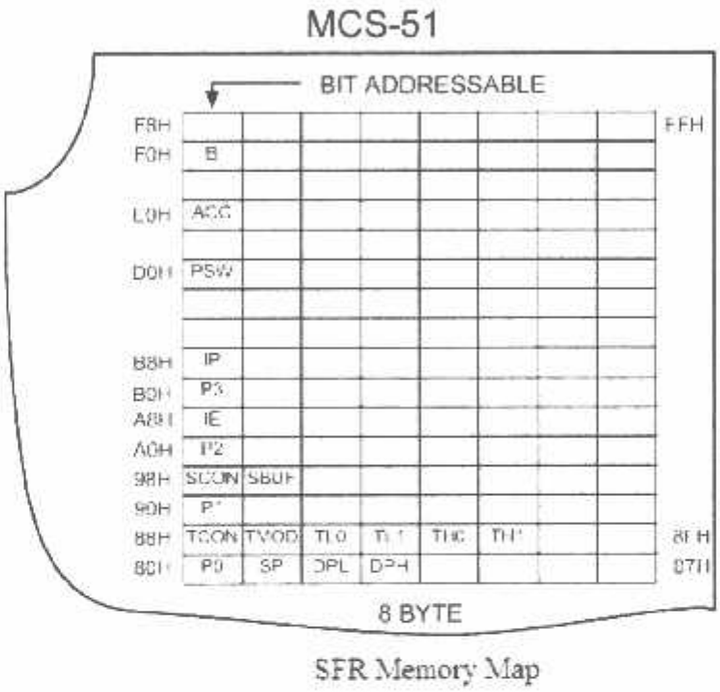


Pemprograman Paralel Pemprograman Serial

Gambar 2.8 Pemprograman Mode Parallel dan Mode Serial AT89S51[7]

2.3.8. SFR (Special Function Register).

Register fungsi khusus (*Special Function Register*) terletak pada 128 byte bagian atas memori data internal dan berisi register-register untuk pelayanan latch port, timer, program status words, control peripheral dan sebagainya. Alamat register fungsi khusus ditunjukkan pada tabel 2.2.



SFR Memory Map

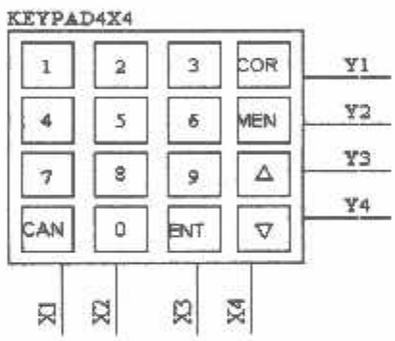
Gambar 2.9 SFR Memori Map Mikrokontroler AT89S51[7]

Beberapa macam register fungsi khusus yang sering digunakan adalah sebagai berikut ini:

- *Accumulator* (ACC) merupakan register untuk penambahan dan pengurangan. Perintah *mnemonic* untuk mengakses akumulator disederhanakan sebagai A.
- *Register B* merupakan register khusus yang berfungsi melayani operasi perkalian dan pembagian.
- *Stack Pointer* (SP) merupakan register 8 bit yang dapat diletakkan di alamat manapun pada RAM internal.
- *Data Pointer* (DPTR) terdiri dari dua register, yaitu untuk byte tinggi (Data Pointer High, DPH) dan byte rendah (Data Pointer Low, DPL) yang berfungsi untuk mengunci alamat 16 bit.
- *Port 0* sampai *Port 3* merupakan register yang berfungsi untuk membaca dan mengeluarkan data pada port 0, 1, 2, 3. Masing-masing register ini dapat dialamati per-byte maupun per-bit.
- *Control Register* terdiri dari register yang mempunyai fungsi kontrol. Untuk mengontrol sistem interupsi, terdapat dua register khusus, yaitu register IP (*Interupt Priority*) dan register IE (*Interupt Enable*). Untuk mengontrol pelayanan timer/counter terdapat register khusus, yaitu register TCON (*timer/counter control*) serta pelayanan port serial menggunakan register SCON (*Serial Port Control*).

2.5 *Keypad Matrik* 4X4

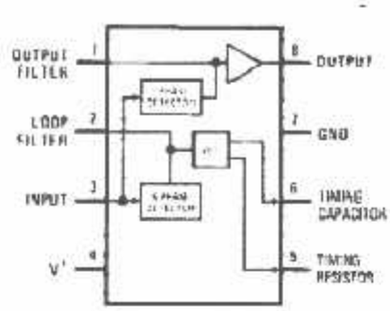
Berfungsi sebagai pengkode data dari papan keypad ke BCD untuk diolah menjadi data digital. Data digital ini nantinya digunakan sebagai masukan bagi mikrokontroler sebagai pengisi *lesson* pembelajaran tentang sandi morse dan keypad ini juga berfungsi untuk melihat penjelasan tentang huruf yang diaplikasikan ke bentuk sandi morse yang ditampilkan ke LCD. Banyaknya kode digital yang dapat dikonversikan tergantung dari jumlah baris dan kolom masukan dari papan keypad atau bisa dikatakan jumlah data yang dikonversikan dalam perkalian baris dan kolom masukan. Adapun keypad tersebut dapat kita lihat seperti Gambar 2.7 di bawah ini :



Gambar 2.12 Keypad 4 x 4

2.6 *Tone Encoder* (LM567)

IC LM 567 selain sebagai IC *tone decoder* juga bisa digunakan sebagai IC *tone encoder*, yang didalamnya sudah dibangun sebuah band pass filter yang cukup sempit dengan Q yang baik. *Tone encoder* atau penghasil nada, karena dapat menghasilkan sinyal pendetak/sinyal kotak. Skematik dari IC LM567 beserta deskripsi pin-nya sendiri bisa dilihat di data sheetnya, sebagai berikut :



Gambar 2.13 Konfigurasi Pin LM 567[5]

Definisi dan fungsi masing-masing pin :

1. *Ground*, adalah pin input dari sumber tegangan DC paling negative.

2. *Loop Filter* atau filter tertutup, Port B (PB0-PB7: Port dua arah I/O 8-bit dengan resistor pull-up internal, digunakan pada fungsi-fungsi khusus dari karakteristik mikrokontroller AT89S51

3. Output Filter : Port A (PA0-PA7): Port dua arah I/O 8-bit, kaki portnya dapat menyediakan resistor pull-up internal (dipilih untuk masing-masing bit). Port A juga dapat mengendalikan tampilan LED secara langsung.

4. Input : Port C (PC0-PC7): Port dua arah I/O 8-bit dengan resistor pull-up internal, digunakan sebagai alamat keluaran saat SRAM eksternal digunakan.

5. Output : Port D (PD0-PD7): Port dua arah /O 8-bit dengan resistor pull-up internal, digunakan untuk berbagai karakteristik khusus dari mikrokontroller AT89S51.

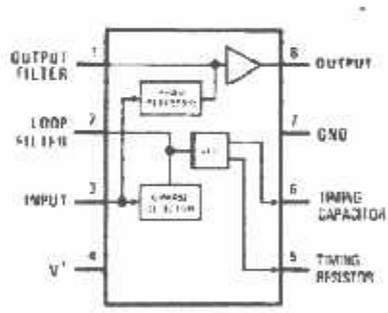
6. Timing Capasitor : RESET: Input reset, jika kaki pinnya mendapat input 0 (low) dalam jangka waktu lebih dari 50 ns maka akan menghasilkan kondisi reset, hal ini terjadi jika clock tidak berfungsi.

7. Timing Resistor : XTAL1: Input untuk inverting oscillator amplifier.

8. Vcc: Tegangan Supply

2.7 *Tone Decoder* (LM567)

IC LM 567 merupakan IC *tone decoder* yang didalamnya sudah dibangun sebuah band pass filter yang cukup sempit dengan Q yang baik. Tone dekoder atau penyalin nada adalah rangkaian yang berfungsi untuk mendeteksi adanya suatu sinyal dengan nada tertentu, LM 567 akan mendeteksi ada/tidaknya sinyal dengan frekuensi tertentu. Skematik dari IC LM567 deskripsi pin-nya sendiri bisa dilihat di datasheetnya, sebagai berikut :



Gambar 2.14 Konfigurasi Pin LM 567[5]

Definisi dan fungsi masing-masing pin :

1. *Ground*, adalah pin input dari sumber tegangan DC paling negative.

2. *Loop Filter* atau filter tertutup, Port B (PB0-PB7: Port dua arah I/O 8-bit dengan resistor pull-up internal, digunakan pada fungsi-fungsi khusus dari karakteristik mikrokontroller AT89S51

3. Output Filter : Port A (PA0-PA7): Port dua arah I/O 8-bit, kaki portnya dapat menyediakan resistor pull-up internal (dipilih untuk masing-masing bit). Port A juga dapat mengendalikan tampilan LED secara langsung.

4. Input : Port C (PC0-PC7): Port dua arah I/O 8-bit dengan resistor pull-up internal, digunakan sebagai alamat keluaran saat SRAM eksternal digunakan.

5. Output : Port D (PD0-PD7): Port dua arah /O 8-bit dengan resistor pull-up internal, digunakan untuk berbagai karakteristik khusus dari mikrokontroller AT89S51.

6. Timing Capasitor : RESET: Input reset, jika kaki pinnya mendapat input 0 (low) dalam jangka waktu lebih dari 50 ns maka akan menghasilkan kondisi reset, hal ini terjadi jika clock tidak berfungsi.

7. Timing Resistor : XTAL1: Input untuk inverting oscillator amplifier.

8. Vcc: Tegangan Supply

2.8 *Walky Talky*

Walky talky merupakan 2 way radio yang dapat melakukan pembicaraan dua arah alias berbicara dan mendengar lawan bicara secara bergantian. Alat ini bisa digunakan untuk komunikasi 2 orang atau lebih dalam jarak hingga 0,5 - 2,5 Km secara hemat (tanpa memikirkan biaya pulsa). Alat ini sangat cocok untuk pekerjaaan yang butuh koordinasi banyak orang (seperti : instalasi kabel networking, pemasangan antena TV, Parabola, pekerja pabrik, sekuriti, panitia acara, pergi ramai-ramai/konvoi kendaraan ke luar kota, permainan anak-anak, dll.).

Dapat digunakan berbarengan lebih dari 1 pasang, jadi bisa sekaligus komunikasi 3 orang atau lebih menggunakan channel yang sama. Walkie Talkie berbeda dengan HT, HT perlu ijin untuk menggunakannya, Walkie Talkie tidak perlu ijin. HT memiliki range frekuensi yang besar dan pemakai bebas memilih frekuensi dalam range tersebut. Sedangkan Walkie Talkie memiliki fixed frekuensi yang telah di tentukan biasanya berjumlah 12 s/d 40 channel/Frekuensi.

Pengguna hanya dapat memilih channel-channel fixed tersebut yang biasanya sama/standar walaupun merek produk berbeda. Baterei Alkaline sampai 8 hari standby atau s/d 3 hari standby + bicara, sedangkan Baterei biasa sampai 4 hari standby atau s/d 1,5 hari standby + bicara. Ketahanan baterei sangat tergantung dari berapa lamanya kita berbicara, mendengar pembicaraan dan banyaknya frekuensi/noise yang masuk pada saat unit dalam keadaan stanby.

2.8.1 Sfesifikasi *Walky Talky* KC-FR860

- *Walky Talky* System
- *Clear One-to-One or Group Communication with family or friends up to* 2,5 Km *away.*
- 22 *Channels* (8 GMRS, 7 GMRS/FRS, 7 FRS)
- *Easy find to an open channel*
- Unlimited airtime
- *No Fees or monthly charges*
- *Audio/Visual*
- *Low Battery Alert*
- *Auto Scan*

BAB III

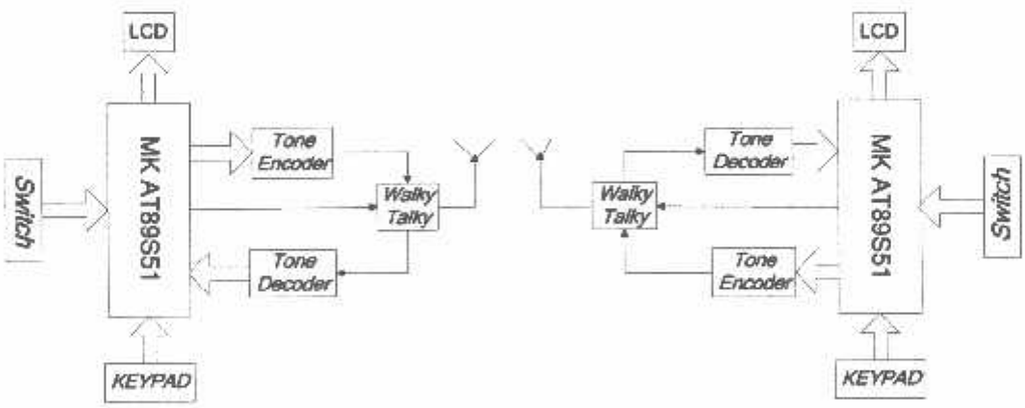
PERENCANAAN DAN PEMBUATAN ALAT

Bab ini akan membahas tentang perencanaan dan perancangan alat yang meliputi perencanaan perangkat keras (*Hardware*) dan perangkat lunak (*Software*) mikrokontroler. Perancangan secara keseluruhan dapat dibagi menjadi dua bagian,yaitu:

1. Perancangan Perangkat Keras (*Hardware*).
2. Perancangan Perangkat Lunak (*Software*).

3.1. Perancangan Perangkat Keras (*Hardware*).

Digram blok sistem sebagai berikut:



Gambar 3.1 Diagram Blok Sistem.

Dari gambar blok diagram 3.1 dapat dijelaskan cara kerjanya sebagai berikut :

Saklar ditekan sesuai sandi morse dengan bunyi misalnya :

\- --- .-.. --- -. --.
T O L O N G

Kemudian dikirimkan melalui walky talky dengan frekuensi carrier sebesar 400 Mhz, dan di terima oleh walky talky tujuan kemudian tone tersebut disalin mengunakan tone decoder, setelah disalin diproses di mikrokontroller untuk diterjemahkan kedalam huruf yang hasilnya sebuah kalimat TOLONG, ditampilkan di LCD. Bunyi terjadi karena adanya perubahan data digital, untuk logika 0 yang mewakili dot (bunyi pendek) perubahan data digital terjadi setiap 0,5 s = 500ms dengan frekuensi tones 1 KHz. Untuk logika 1 yang mewakili dash (bunyi panjang) perubahan data digital terjadi setiap 1,0 s = 1000ms, dengan frekuensi tones 1 KHz.

Keterangan dari diagram blok :

- Mikrokontroller AT89S51

  Berfungsi sebagai pengendali kerja sistem keseluruhan

- *Walky Talky*

  Berfungsi sebagai pengirim dan penerima sandi *morse.*

- *Switch Push Button*

  Berfungsi untuk inputan sandi *morse.*

- *Keypad*

  Berfungsi sebagai pereset sandi *morse* setelah dibaca dan sebagai penekanan huruf *lesson* yang terlihat di LCD, dan inputan sandi *morse*.

- *Tone Encoder* (LM567)

  Berfungsi sebagai penghasil *tone* sandi *morse*.

- *Tone Decoder* (LM567)

  Berfungsi untuk menyalin *tone* sandi *morse* yang diterima.

- LCD

  Untuk menampilkan sandi *morse*.

3.1.1 Rangkaian Mikrokontroler AT89S51

Mikrokontroller AT89S51 dirancang untuk berdiri sendiri, karena sudah terdapat EEPROM, RAM, serta Port I/O internal. Untuk berhubungan dengan piranti luar terbagi atas 3 bus, yaitu :

- Data *Bus*

  Yaitu jalur untuk *input-output* data yang lebarnya sesuai lebar data yang di peroleh oleh mikrokontroller, yaitu 8 bit.

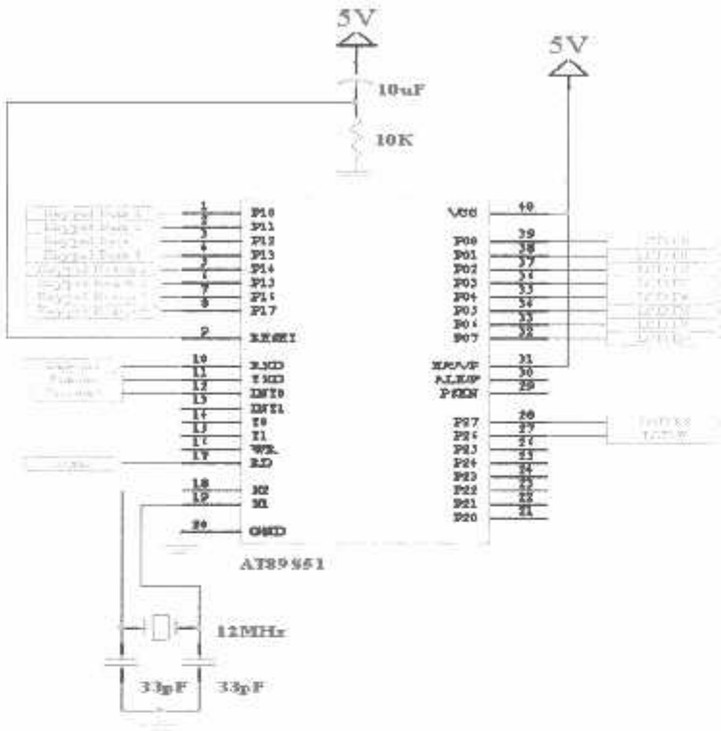
- *Address Bus*

  Yaitu jalur alamat dari *input-output* atau memori yang di hubungkan sehingga suatu saat hanya ada satu *device* yang berhubungan dengan CPU, lebar *address bus* mekrokontroller adalah 16 bit (A0-A15).

- Kontrol *Bus*

  Kontrol bus berfungsi untuk mengatur sinkronisasi hubungan antara MCU dengan luar.

Rangkaian mikrokontroler AT89S51 ini berfungsi sebagai pengolah data inputan yang dimasukkan melalui tombol menu untuk memilih kelas perlombaan renang, dan tombol inputan saat *start* maupun saat *finish*, yang kemudian ditampilkan melalui *seven segment*. Pembacaan data *input/output* pada mikrokontroler melalui port-port I/O yang disediakan selebar 32 bit. Pengaturan jalur *input* dan *output* pada rangkaian mikrokontroler untuk sebuah rancangan terprogram, sangat berkaitan erat dengan program yang dibuat. Dengan adanya penggunaan jalur *input-output* pada mikrokontroler perlu kiranya menentukan terlebih dahulu jalur tersebut, agar tidak terjadi kesalahan saat pembacaan data. Mikrokontroler menyediakan jalur-jalur khusus untuk operasi tersebut. Untuk lebih jelasnya hubungan mikrokontroler dengan perangkat pendukungnya dapat dilihat pada gambar 3.2 di bawah ini:



Gambar 3.2. Interfacing Mikrokontroler Dengan Rangkaian Diluarnya

Kecepatan proses pengolahan data pada mikrokontroler ditentukan oleh *Clock* (pewaktu) yang dikendalikan oleh mikrokontroller tersebut. Pada Mikrokontroler AT89S51 terdapat *internal clock* generator yang berfungsi sebagai sumber *clock*, tapi masih memerlukan rangkaian tambahan untuk membangkitkan *clock* yang diperlukan.

Rangkaian *clock* ini terdiri atas dua buah kapasitor, dan sebuah Kristal yang terangkai sedemikian rupa dan kemudian dihubungkan dengan chip yang tersedia pada AT89S51.

Dalam perencanaan ini menggunakan :

- ✓ C = 33 pF. Penentuan besarnya kapasitansi disesuaikan dengan spesifikasi lembar data AT89S51
- ✓ X-Tal 12 MHz.

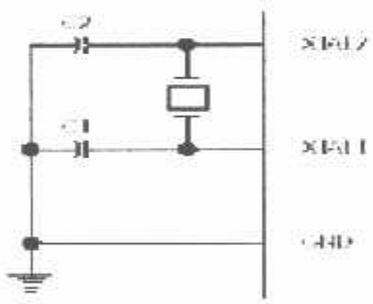
3.1.1.1. Rangkaian *Clock*

Kecepatan proses pengolahan data pada mikrokontroler ditentukan oleh *Clock* (pewaktu) yang dikendalikan oleh mikrokontroller tersebut. Pada Mikrokontroler AT89S51 terdapat *internal clock* generator yang berfungsi sebagai sumber *clock*, tapi masih memerlukan rangkaian tambahan untuk membangkitkan *clock* yang diperlukan.

Rangkaian *clock* ini terdiri atas dua buah kapasitor, dan sebuah Kristal yang terangkai sedemikian rupa dan kemudian dihubungkan dengan chip yang tersedia pada AT89S51.

Dalam perencanaan ini menggunakan :

- ✓ C = 33 pF. Penentuan besarnya kapasitansi disesuaikan dengan spesifikasi lembar data AT89S51
- ✓ X-Tal 12 MHz.



Gambar 3.3 Rangkaian *Clock*

Dengan menggunakan nilai kristal diatas maka dapat dihitung waktu yang diperlukan untuk satu siklus mesin.

Diketahui : F = 12 Mhz

$$T = \frac{1}{F}$$

Sehingga :

$$T = \frac{1}{12\,\text{MHz}} = \frac{1}{12}\mu s$$

Maka untuk satu siklus mesin dari mikrokontroller AT89S51 adalah sebesar :

$$Tme = 12xT$$

$$Tme = 12x\frac{1}{12}\mu s = 1\mu s$$

$$Tme = 1\ \mu s$$

3.1.1.2 Rangkaian Reset.

Rangkaian *reset* dalam mikrokontroller AT89S51 akan melakukan *reset* setelah catu daya dihidupkan. Pada saat kondisi *reset* maka faktor reset pada alamat 0000H akan dituju oleh mikrokontroller AT89S51 (dalam hal ini program counter) agar program yang terdapat didalam mikrokontroller kembali ke kondisi semula atau dengan kata lain mikrokontroller mengakses awal dari program yang telah diisi didalamnya. Didalam *reset* ini akan mengunakan beberapa macam cara untuk mereset miktrokontroller AT89S51. Cara pertama mengunakan *switch* (manual), dimana *user* yang akan mengoperasikan *switch* ini. Cara ke dua mengunakan capasitor 47 uF, dimana capasitor tersebut akan berkondisi aktif *high* selama beberapa detik.

Besarnya nilai tahanan dan kapasitor pada rangkaian reset akan menentukan lamanya waktu pulsa reset.

Dengan rumus :

t = R x C

Agar reset dapat terjadi secara normal maka nilai 't' harus jauh lebih besar dari waktu satu kali siklus mesin. Dengan mengambil nilai R dan C sebesar 10 KΩ dan 47 uF maka besarnya 'T' dapat dicari sebagai berikut :

$t = R \times C$

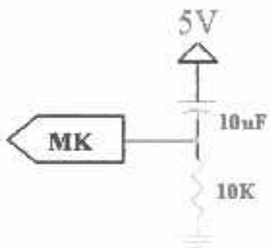
$= 10K\Omega \times 10\ \mu F$

$= (10 \times 10^{3}) \times (10 \times 10^{-6}) = 100 \times 10^{-3}$ second

$t = 0{,}1$ second

Maka dengan demikian :

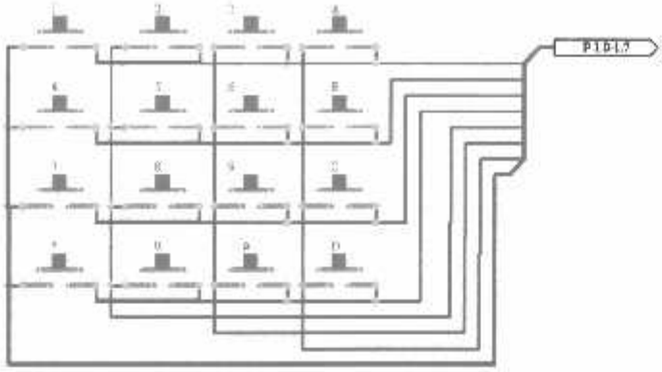
Nilai 't' jauh lebih besar dibandingkan dengan nilai minimalnya seperti pada gambar 3.4 :



Gambar 3.4 Rangkaian Reset.

3.1.2 Rangkaian Antarmuka *Keypad*

Keypad yang digunakan adalah *keypad* matriks 4x4. Port yang digunakan untuk sinyal port 1.4 – port 1.7 dari mikrokontroller masuk ke kelompok baris keypad, sedangkan kelompok kolom keypad dihubungkan ke port 1.0 – port 1.3 mikrokontroller. Untuk fungsi dari tombol-tombol keypad tergantung pada pemrogram. Berikut gambar dari penyambungan keypad ke mikrokontroller.

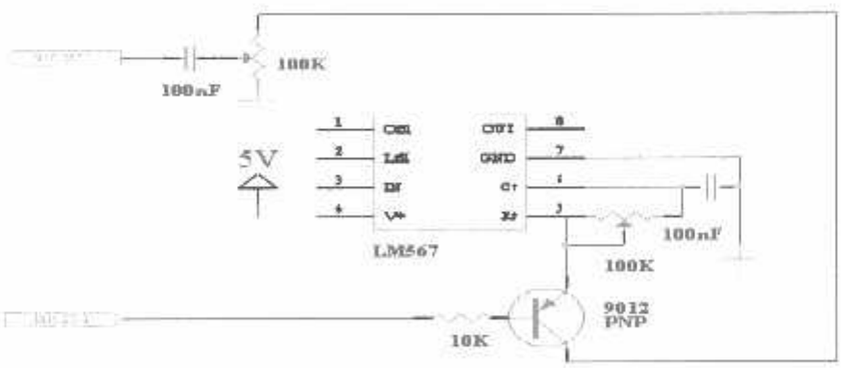


Gambar 3.5 Rangkaian Input *Keypad*

Apabila terjadi penekanan tombol maka data yang dihasilkan dalam bentuk hexadesimal akan diterjemahkan oleh mikrokontroller menjadi desimal. Dari kombinasi penekanan tersebut menghasilkan 16 tombol atau kemungkinan yang akan terbentuk karakter angka dan simbol. Teknik pembacaan pada *keypad* ini, yaitu model *scaning* 4 jalur baris dan 4 jalur kolom. Bila baris dan kolom ini disilangkan maka akan terbentuk titik-titik potong yang membentuk *matrik* 4x 4.

3.1.3 Perancangan Rangkaian *Tone Encoder* LM567

Rangkaian *tone encoder* ini menggunakan LM567 yang berfungsi untuk menghasilkan *tone morse* yang akan dikirim.



Gambar 3.6 Rangkaian *Tone Encoder* LM567.

4.2.4. Hasil pengujian

Dari hasil pengujian maka didapatkan tampilan seperti yang terlihat pada gambar berikut ini :

Gambar 4.2 Hasil Pengujian LCD.

Cara menampilkan data diatas adalah dengan memasukan progam seperti dibawah ini :

```
dltone: lcall   delay0
        djnz    Dly4,dltone
        ret
nama:   DB      '  Yuri Darmawan  '
nim:    DB      'NIM: 03.17.099'
jurs:   DB      'Teknik Elektro'
univ:   DB      '  ITN Malang  '
```

dan pada waktu pertama dinyalakan maka akan keluar seperti gambar

Tabel 4.1 Hasil Pengukuran Pengujian Rangkaian LCD

No	Tegangan Awal LCD (Volt)	Tegangan Setelah Melewati Dioda (Volt)
1	4,87	4,25

Gambar 4.3 Pengukuran Tegangan Awal LCD

Gambar 4.4 Pengukuran Tegangan Setelah Melewati Dioda

Perubahan nilai tegangan dari 4,87 V menjadi 4,25 V sesuai dengan tegangan yang direkomendasikan oleh data sheet LCD sebesar 4,2 V - 4,3 V.

4.3. Pengujian *Keypad* 4 x 4

4.3.1. Tujuan

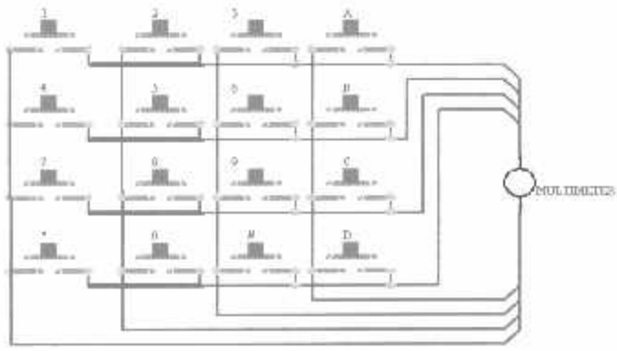
Untuk menguji apakah tombol keypad dapat bekerja sebagai inputan,dan mensimulasikan tombol yang ditekan melalui suara buzzer pada multimeter digital.

4.3.2. Alat yang digunakan

- Multimeter digital
- *Keypad*

4.3.3. Prosedur Pengujian

1. Menyusun rangkaian pengujian keypad seperti pada gambar 4.5.



Gambar 4.5 Pengujian Rangkaian *Keypad.*

2. Memberikan kombinasi masukan dengan menekan tombol-tombol *keypad* dengan memasukan program sebagai berikut:

```
klmpk0: DB    '.1'          ; 2
klmpk1: DB    'abc2'        ; 4
klmpk2: DB    'def3'        ; 4
klmpk3: DB    'ghi4'        ; 4
klmpk4: DB    'jkl5'        ; 4
klmpk5: DB    'mno6'        ; 4
klmpk6: DB    'pqrs7'       ; 5
klmpk7: DB    'tuv8'        ; 4
klmpk8: DB    'wxyz9'       ; 5
klmpk9: DB    ' 0'          ; 2
```

3. Mengamati hasil penekanan *keypad.* Kemudian mencatat hasil pengamatan pada tabel 4.1

4.3.4. Hasil Pengujian

Tabel 4.1 Hasil Pengujian *Keypad.*

TOMBOL	BARIS				KOLOM			
	1	2	3	4	1	2	3	4
1	1	0	0	0	1	0	0	0
2	1	0	0	0	0	1	0	0
3	1	0	0	0	0	0	1	0
A	1	0	0	0	0	0	0	1
4	0	1	0	0	1	0	0	0
5	0	1	0	0	0	1	0	0
6	0	1	0	0	0	0	1	0
B	0	1	0	0	0	0	0	1
7	0	0	1	0	1	0	0	0
8	0	0	1	0	0	1	0	0
9	0	0	1	0	0	0	1	0
C	0	0	1	0	0	0	0	1
#	0	0	0	1	1	0	0	0
0	0	0	0	1	0	1	0	0
*	0	0	0	1	0	0	1	0
D	0	0	0	1	0	0	0	1

* Keterangan : Cara membaca tabel diatas adalah jika antara baris dan kolom terhubung (1) maka akan membentuk matrik baris dan kolom sesuai penekanan tombol *keypad.*

Gambar 4.6 Pengecekan Jalur *Keypad* Dengan Multimeter.

- Analisa Hasil Pengujian

Dari rangkaian pengujian didapatkan bahwa untuk membentuk satu karakter penekanan keypad maka baris dan kolom harus terhubung. Sebagai contoh: jika angka 1 ditekan kemudian mengeceknya menggunakan multimeter pada baris 1 dan kolom 1 maka akan terdengar suara buzzer pada multimeter, begitu seterusnya pada penekanan keypad yang lain sesuai tabel 4.1.

4.4. Pengujian *Tone Encoder* LM567

4.4.1. Tujuan

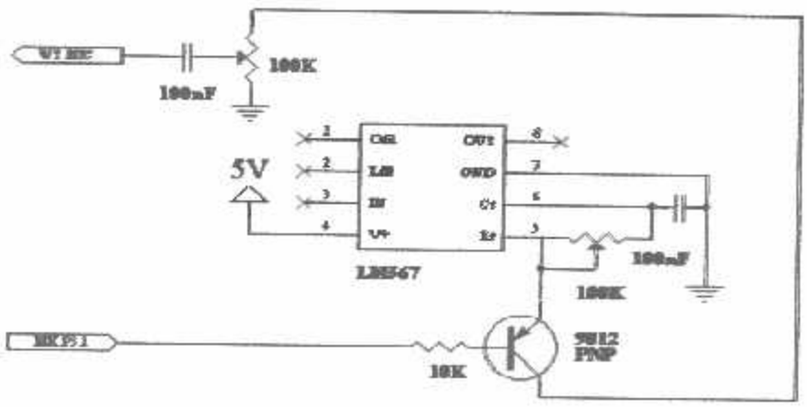
Adapun tujuan dari pengujian rangkaian ini untuk mengetahui, apakah *tone* encoder LM567 bekerja dengan baik, dengan mengirimkan frekuensi *tone* sebesar 1 kHz, sehingga dapat mengirimkan sandi morse.

4.4.2. Alat-alat Yang Digunakan

- Rangkaian *tone encoder* LM567.
- Catu daya.
- Multimeter digital.

4.4.3. Prosedur Pengujian.

1. Menyusun rangkaian pengujian seperti pada gambar 4.7.

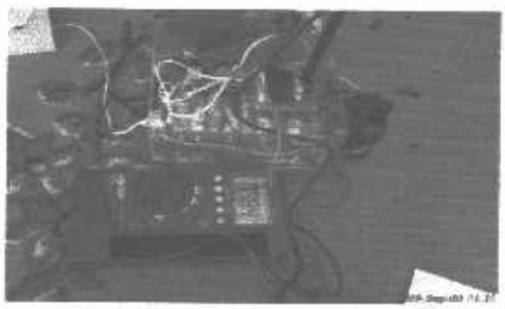


Gambar 4.7 Rangkaian Pengujian *tone encoder* LM567

2. Mengaktifkan catu daya.
3. Menghubungkan kutub positif multimeter digital pada pin 5 LM567, sedangkan kutub negatif ke ground.
4. Mengamati hasil pengukuran, pada tampilan LCD multimeter.

4.4.4. Prosedur Pengujian *tone encoder* LM567 sebelum di *jammer*

1. Melakukan pengujian seperti pada gambar 4.8.



Gambar 4.8 Hasil pengujian *tone encoder* LM567 sebelum di *jammer*.

4.4.5. Analisa

Frekuensi *tone* = 1 KHz

Didapat dari perhitungan : $f = \frac{1}{R..C}$

R = 10 KΩ

C = 100 nF = 0.1 mF

Jadi : : $f = \frac{1}{R..C} = \frac{1}{10 \times 0.1} = \frac{1}{1} = 1$ KHz

Untuk mengetahui frekuensi *tone encoder* sebelum di jammer dilakukan lima kali pengukuran :

Pengukuran 1 : 0.984 KHz

Pengukuran 2 : 0.982 KHz

Pengukuran 3 : 0.985 KHz

Pengukuran 4 : 0.988 KHz

Pengukuran 5 : 0.987 KHz

Untuk % kesalahan dapat dihitung dari hasil pengukuran dan perhitungan sebagai berikut: $\%\ \text{kesalahan} = \frac{(perhitungan - pengukuran)}{perhitungan} x100\%$

Contoh : Frekuensi *tone* perhitungan = 1 KHz

Frekuensi *tone* pengukuran = 0,984 KHz

% kesalahan = $\frac{1\ \text{KHz} - 0.984\ \text{KHz}}{1\ \text{KHz}} \times 100\%$ = jadi % kesalahan = 1.6 %

Tabel 4.2

Data Hasil Pengukuran Dan Perhitungan Rangkaian *Tone Encoder* LM567 Sebelum Di *Jammer*

NO	*Tone Encoder* LM567		
	PERHITUNGAN (KHz)	PENGUKURAN (KHz)	% KESALAHAN (%)
1	1	0.984	1.6
2	1	0.982	1.8
3	1	0.985	1.5
4	1	0.988	1.2
5	1	0.987	1.3

- Analisa Hasil Pengujian

  Dari rangkaian pengujian yang dilakukan 5 kali percobaan, didapatkan bahwa persentase error di bawah 5%, ini membuktikan bahwa alat dapat bekerja dengan baik.

4.4.6. Prosedur Pengujian *tone encoder* LM567 sesudah di *jammer*.

1. Melakukan pengujian seperti pada gambar 4.9.

Gambar 4.9 Hasil pengujian *tone encoder* LM567 sesudah di *jammer*.

4.4.7. Analisa

Frekuensi *tone* = 1 KHz

Didapat dari perhitungan : $f = \frac{1}{R..C}$

R = 10 KΩ

C = 100 nF = 0.1 mF

Jadi : : $f = \frac{1}{R..C} = \frac{1}{10 \times 0.1} = \frac{1}{1} = 1$ KHz

Untuk mengetahui frekuensi *tone encoder* sesudah di *jammer* dilakukan lima kali pengukuran :

Pengukuran 1 : 1.026 KHz

Pengukuran 2 : 1.030 KHz

Pengukuran 3 : 1.028 KHz

Pengukuran 4 : 1.032 KHz

Pengukuran 5 : 1.029 KHz

Untuk % kesalahan dapat dihitung dari hasil pengukuran dan perhitungan sebagai berikut: $\%\ \text{kesalahan} = \frac{(perhitungan - pengukuran)}{perhitungan} x100\%$

Contoh : Frekuensi *tone* perhitungan = 1 KHz

Frekuensi *tone* pengukuran = 0,984 KHz

$\%\ \text{kesalahan} = \frac{1\ \text{KHz} - 1.026\ \text{KHz}}{1\ \text{KHz}} \times 100\%$ = jadi % kesalahan = 2.6 %

Tabel 4.3

Data Hasil Pengukuran Dan Perhitungan Rangkaian *Tone Encoder* LM567 Sesudah Di *Jammer*

NO	*Tone Encoder* LM567		
	PERHITUNGAN (KHz)	PENGUKURAN (KHz)	% KESALAHAN (%)
1	1	1.026	2.6
2	1	1.030	3
3	1	1.028	2.8
4	1	1.032	3.2
5	1	1.029	2.9

- Analisa Hasil Pengujian

  Dari rangkaian pengujian yang dilakukan 5 kali percobaan, didapatkan bahwa persentase error di bawah 5%, ini membuktikan bahwa alat dapat bekerja dengan baik.

- Selisih antara *tone encoder* sebelum dan sesudah di *di jammer* terjadi karena adanya GGL antena mempengaruhi alat karena dekat.

4.5. Pengujian *Tone Decoder* LM567

4.5.1. Tujuan

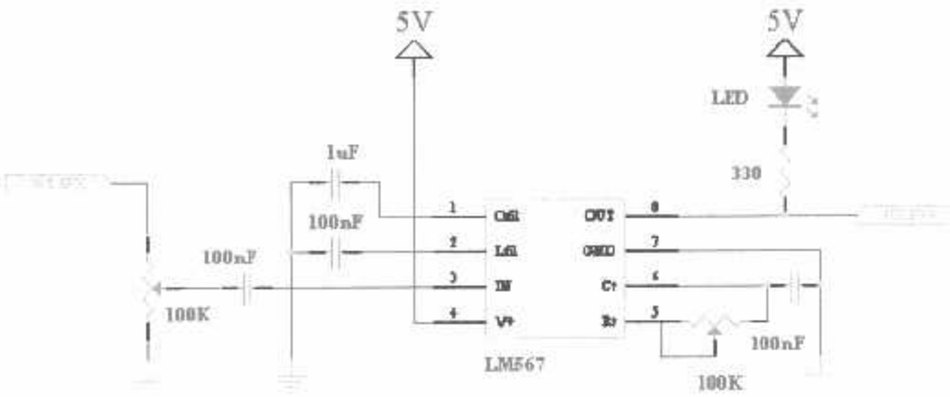
Adapun tujuan dari pengujian rangkaian ini untuk mengetahui, apakah *tone decoder* LM567 bekerja dengan baik, dengan menerima frekuensi *tone* sebesar 1 KHz, sehingga dapat mendecoder sandi morse, untuk ditampilkan oleh LCD.

4.5.2. Alat-alat Yang Digunakan

- Rangkaian *tone decoder* LM567.
- Catu daya.
- Multimeter digital.

4.5.3. Prosedur Pengujian

1. Menyusun rangkaian pengujian seperti pada gambar 5.0.

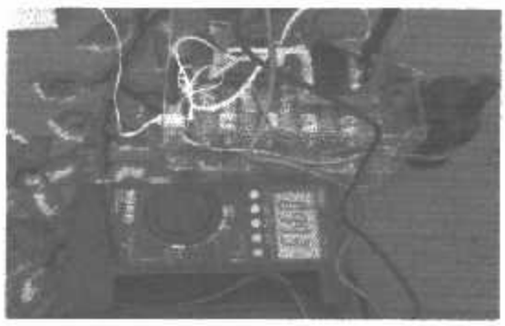


Gambar 5.0. Rangkaian Pengujian *tone decoder* LM567

2. Mengaktifkan catu daya.
3. Menghubungkan kutub positif multimeter digital pada pin 1 LM567, sedangkan kutub negatif ke ground.
4. Mengamati hasil pengukuran, pada tampilan LCD multimeter.

4.5.4 Prosedur Pengujian *tone decoder* LM567.

1. Melakukan pengujian seperti pada gambar 5.1.



Gambar 5.1 Hasil pengujian *tone decoder* LM567.

4.5.5. Analisa

Frekuensi *tone* – 1 KHz

Didapat dari perhitungan : $f = \frac{1}{R..C}$

$R = 10\ K\Omega$

$C = 100\ nF = 0.1\ mF$

Jadi : : $f = \frac{1}{R..C} = \frac{1}{10 \times 0.1} = \frac{1}{1} = 1\ KHz$

Untuk mengetahui penerimaan frekuensi *tone* dilakukan lima kali pengukuran :

Pengukuran 1 : 0.993 KHz

Pengukuran 2 : 0.998 KHz

Pengukuran 3 : 0.996 KHz

Pengukuran 4 : 0.997 KHz

Pengukuran 5 : 0.995 KHz

Untuk % kesalahan dapat dihitung dari hasil pengukuran dan perhitungan sebagai berikut: $\%\ \text{kesalahan} = \frac{(perhitungan - pengukuran)}{perhitungan} x100\%$

Contoh : Frekuensi *tone* perhitungan = 1 KHz

Frekuensi *tone* pengukuran = 0,993 KHz

% kesalahan = $\frac{1\ \text{KHz} - 0.993\ \text{KHz}}{1\ \text{KHz}}$ x 100% = jadi % kesalahan = 0.7 %

Tabel 4.4

Data Hasil Pengukuran Dan Perhitungan Rangkaian *Tone Decoder*

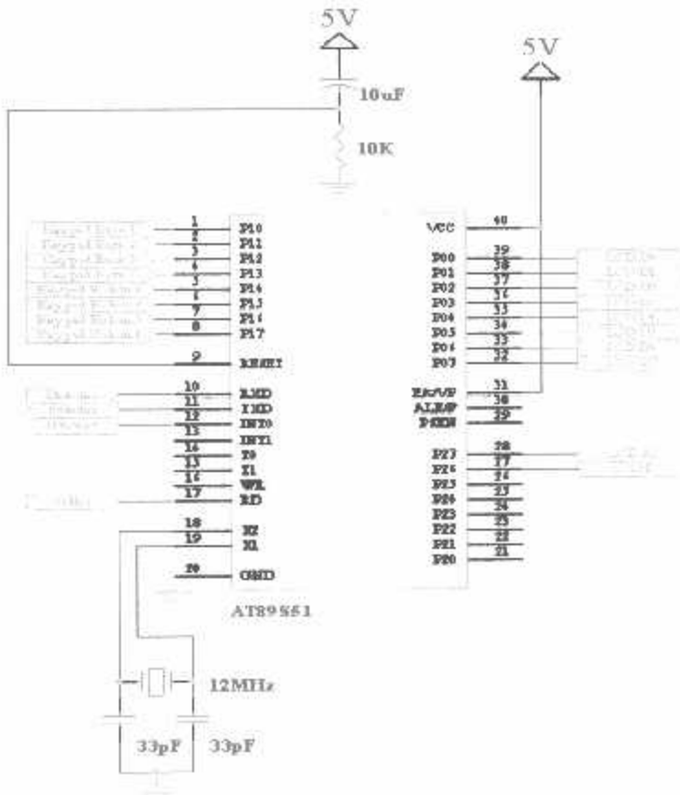
NO	*Tone Decoder* LM567		
	PERHITUNGAN (KHz)	PENGUKURAN (KHz)	% KESALAHAN (%)
1	1	0.993	0.7
2	1	0.998	0.2
3	1	0.996	0.4
4	1	0.997	0.3
5	1	0.995	0.5

- Analisa Hasil Pengujian

  Dari rangkaian pengujian yang dilakukan 5 kali percobaan, didapatkan bahwa persentase error di bawah 5%, ini membuktikan bahwa alat dapat bekerja dengan baik.

4.6. Pengujian Sistem Secara Menyeluruh

Pengujian rangkaian secara keseluruhan dilakukan dengan menghubungkan Masing-masing rangkaian atau blok dan menjalankan perangkat lunak yang dibuat Pengujian ini dimaksudkan untuk mengetahui apakah peralatan yang dibuat telah sesuai dengan perecanaan.

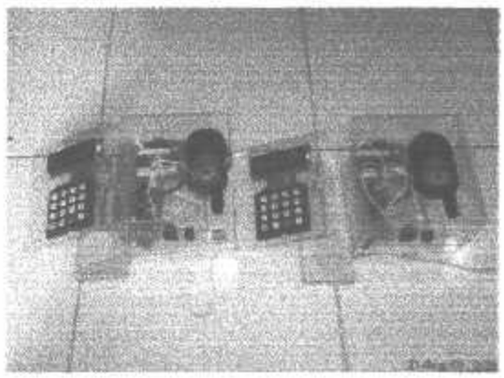


Gambar 5.2. Rangkaian keseluruhan sistem

Langkah-langkah pengujian alat secara keseluruhan :

1. Pengujian alat dilakukan dengan beberapa kali pengetesan.
2. Memberi tegangan catu daya 12 Volt DC, dapat berupa baterai, aki dan lain-lain
3. Menghidupkan saklar dengan mengamati LCD

4. Menghidupkan saklar *walky talky*.
5. Melakukan pengiriman sandi *morse* dengan menekan switch dan keypad.
6. Mengamati tampilan LCD pada alat penerima.



Gambar 5.3 Alat Secara keseluruhan

Pada pengujian alat diatas dilakukan dengan melakukan penekanan pada switch, sesuai tabel 4.5 kemudian dilakukan pengamatan pada tampilan LCD di alat penerima, setelah dilakukan beberapa kali pengetesan, ada beberapa kesalahan yang terjadi, yaitu karakter sandi *morse* yang dikirim tidak sesuai dengan yang harapkan, di akibatkan penekanan *switch* yang tidak sesuai, dan keterlambatan penekanan.

Untuk penekanan pengiriman sandi morse dengan menggunakan keypad dilakukan pengetesan sesuai dengan tabel 4.5, pada pengetesan ini tidak terdapat kesalahan karena penekanan pada *keypad* sesuai.

Tabel 4.5 Pengetesan Alat Secara Keseluruhan

Huruf / Angka	Saklar	Tampilan LCD
MAKAN	— .- -.- .- -. M A K A N	MAKAN
MINUM	— .. -. .. — M I N U M	MINUM
PERGI	.—. . .-. —. .. P E R G I	PERGI
1234	.—— ..— ...— ....- 1 2 3 4	1234
4567	....- ..... -.... —... 4 5 6 7	4567

BAB V

KESIMPULAN DAN SARAN

5.1. Kesimpulan.

Berdasarkan hasil pengujian dan evaluasi dari perancangan dan pembuatan komunikasi menggunakan sandi *morse* berbasis mikrokontroller at89s51 diaplikasikan secara langsung, diambil kesimpulan sebagai berikut:

- Dalam pengujian pengiriman dan penerimaan data, dari 5 kali percobaan dengan karakter yang berbeda, terdapat kesalahan, ini disebabkan karena pada waktu penekanan *switch* inputan sandi *morse* yang tidak sesuai.
- Penekanan *switch* harus benar-benar sesuai, keterlambatan dan kesalahan penekanan *switch* , membuat karakter huruf menjadi berubah.
- Alat ini menggunakan IC LM567 sebagai *tone encoder dan tone decoder*.
- Jarak komunikasi yang tertera di spesifikasi panduan *walky talky,* antara 0-2.5km, dengan antena *walky talky* saling berhadapan. Jarak *walky talky* bisa berubah apabila ada penghalang seperti dinding, hal ini diakibatkan karena antena *walky talky,* yang pendek.
- Pengiriman karakter, harus disesuaikan dengan waktu jammer *walky talky* yaitu selama 50 *second.*

5.2. Saran- Saran Pengembangan.

- Untuk kedepan agar alat mudah dibawa perlu kiranya dibuat dalam ukuran yang kecil.
- Sebaiknya penggunaan *keypad* sebagai inputan sandi *morse* lebih baik, dari pada menggunakan switch, karena harus berhati-hati dalam penekanan, untuk memasukan inputan.
- Menggunakan sarana komunikasi yang jauh jarak jangkauanya melebihi *walky talky*, misalnya HT (*handy talky*).

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LAMPIRAN-LAMPIRAN

INSTITUT TEKNOLOGI NASIONAL
FAKULTAS TEKNOLOGI INDUSTRI
JURUSAN TEKNIK ELEKTRO
JL.Raya Karanglo Km 2
MALANG

PERSETUJUAN PERBAIKAN SKRIPSI

Dari hasil Ujian Kompreherensip Jenjang Strata Satu (S1) Jurusan Teknik Elektro Konsentrasi Elektronika yang diselenggarakan pada :

Hari : Selasa
Tanggal : 29 September 2009

Telah dilaksanakan perbaikan skripsi oleh saudara :

Nama : Yuri Darmawan
NIM : 03.17.099
Judul Skripsi : Perancangan Dan Pembuatan Komunikasi Menggunakan Sandi Morse Berbasis Mikrokontroller At89s51

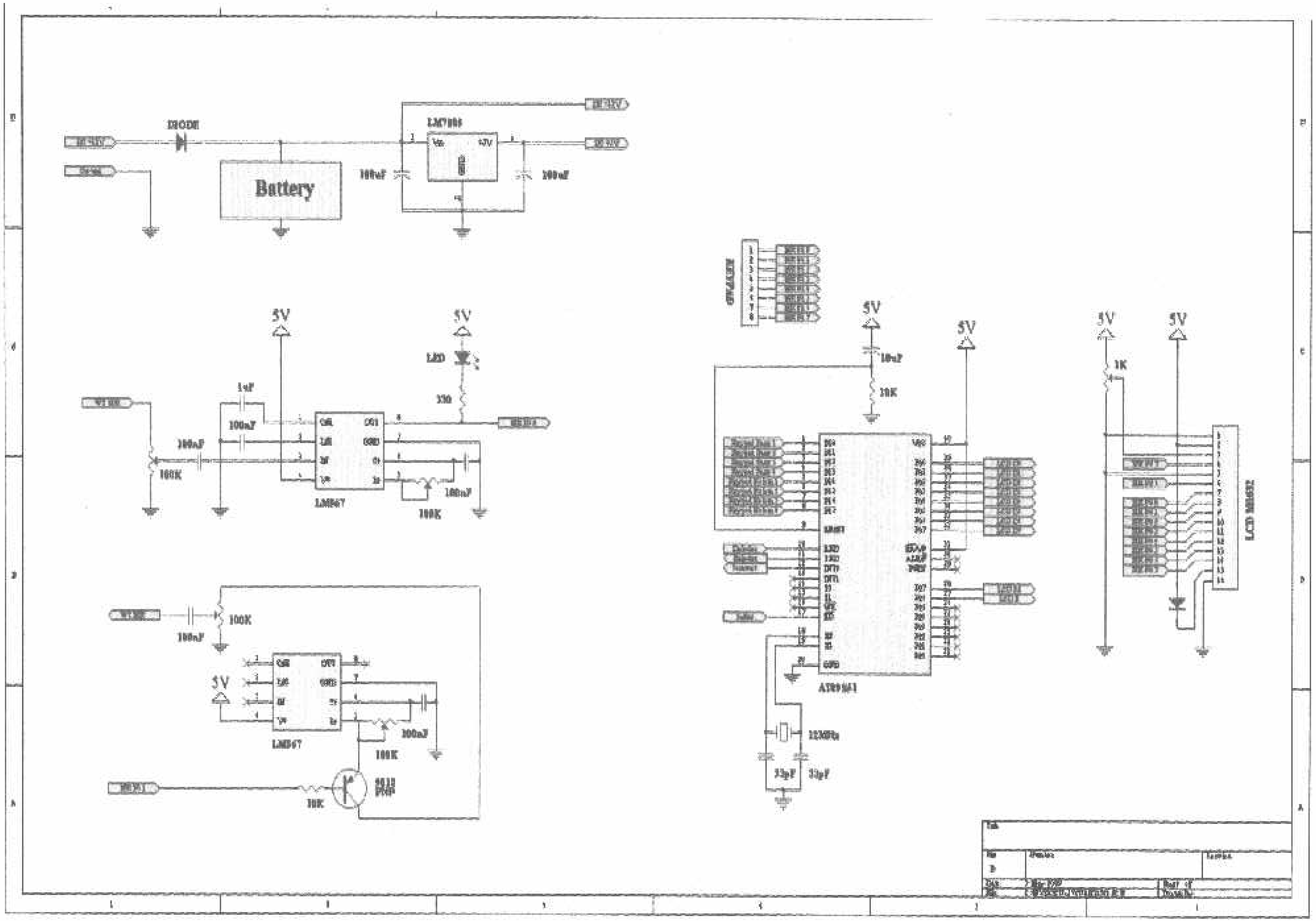
Perbaikan tersebut meliputi :

No	Materi Perbaikan	Paraf Dosen
1	Memori Map Untuk Penyimpanan Sandi Morse	

Malang, Oktober 2009
Dosen Penguji II

Satyohadi, ST
NIP. Y. 1039700309

SCHEMATIK


DIODE
Battery
LM7805
100uF
100uF
5V
LED
330
1uF
100nF
100nF
100K
100nF
100K
LM567
100K
100nF
LM567
10K
100K
100nF
100K
KEYPAD
10uF
10K
AT89S51
12MHz
33pF
33pF
1K
LCD 16X2

LISTING PROGRAM

```
        org     00h
        ljmp    init                    ; lompat

        org     0Bh                     ; interupt timer 0
        ljmp    cntdwn

;
Rest    Bit P2.6
Enbl    Bit P2.7
Mrrx    Bit P3.0                        ; morse receive
Mrtx    Bit P3.1                        ; morse transmit
Mrjm    Bit P3.2                        ; morse jammer
Mrtb    Bit P3.7                        ; morse tombol

Stts    Bit 20h.0                       ; status cek sandi
Stgs    Bit 20h.1                       ; status geser
Stch    Bit 20h.2                       ; status tulis character

Ch00    Equ 30h
Ch01    Equ 31h
Ch02    Equ 32h
Ch03    Equ 33h
Ch04    Equ 34h
Ch05    Equ 35h
Ch06    Equ 36h
Ch07    Equ 37h
Ch08    Equ 38h
Ch09    Equ 39h
Ch0A    Equ 3Ah
Ch0B    Equ 3Bh
Ch0C    Equ 3Ch
Ch0D    Equ 3Dh
Ch0E    Equ 3Eh
Ch0F    Equ 3Fh

Tmot    Equ 50h
CTmo    Equ 51h
Ping    Equ 52h
Chsn    Equ 53h                         ; character sandi
Gser    Equ 54h                         ; geser character
Sndi    Equ 55h                         ; data sandi
Snd0    Equ 56h                         ; data sandi 0
Snd1    Equ 57h                         ; data sandi 1
Snd2    Equ 58h                         ; data sandi 2
Snd3    Equ 59h                         ; data sandi 3
Snd4    Equ 5Ah                         ; data sandi 4
Snd5    Equ 5Bh                         ; data sandi 5

Char    Equ 60h
Cntr    Equ 61h
Tmc0    Equ 62h
Tmc1    Equ 63h
Dtkp    Equ 64h
Jum1    Equ 65h
Colm    Equ 66h
Dly0    Equ 67h
Dly1    Equ 68h
Dly2    Equ 69h
```

```
        Dly2    Equ 6Ah
;
init:   lcall   lcd_in
        lcall   tmr_in
;
mulai:  mov     DPTR,#nama
        lcall   line1
        mov     Char,#16
        lcall   tulis
        mov     DPTR,#nim
        lcall   line2
        mov     Char,#16
        lcall   tulis
        lcall   delay2
        mov     DPTR,#jur
        lcall   line1
        mov     Char,#16
        lcall   tulis
        mov     DPTR,#univ
        lcall   line2
        mov     Char,#16
        lcall   tulis
        lcall   delay2
        ljmp    mulai
;
kr_mrs: lcall   lcdclr
        mov     DPTR,#tpkrmr
        lcall   line1
        mov     Char,#16
        lcall   tulis
        mov     Dly3,#5
        lcall   delay3
        mov     DPTR,#tptmot
        lcall   line1
        mov     Char,#16
        lcall   tulis
        mov     DPTR,#tpsand
        lcall   line2
        mov     Char,#16
        lcall   tulis
        setb    TR0
        clr     Mrjm
        mov     Tmot,#50
        mov     DPTR,#angka
krmrs0: mov     Pjng,#0
krmrs1: mov     P0,#08Ch
        lcall   w_ins
        mov     A,Tmot
        lcall   nil
        mov     P0,#0D0h
        lcall   w_ins
;
        inc     Pjng
        lcall   delay4
;       mov     P0,#0C2h            ; smntr utk klbrs
;       lcall   w_ins               ; smntr utk klbrs
;       mov     A,Pjng              ; smntr utk klbrs
```

```
;         lcall   nil                 ; smntr utk klbrs
;
          mov     A,Pjng
          mov     B,#25
          div     AB
          jz      krmrs2
          mov     P0,#0C8h
          lcall   w_ins
          mov     P0,#'S'
          lcall   w_chr
          mov     P0,#0D0h
          lcall   w_ins
krmrs2:   mov     A,Tmot
          jz      krmrs8
;
          jb      Mrtb,krmrs1
          clr     Mrtx
          mov     Pjng,#0
krmrs3:   inc     Pjng
          lcall   delay4
;          mov     P0,#0C0h          ; smntr utk klbrs
;          lcall   w_ins             ; smntr utk klbrs
;          mov     A,Pjng            ; smntr utk klbrs
;          lcall   nil               ; smntr utk klbrs
          jnb     Mrtb,krmrs3
          setb    Mrtx
;
          mov     A,Pjng
          mov     B,#1
          div     AB
krmrs4:   jnz     krmrs5
          mov     Sndi,#' '
          ljmp    krmrs7
krmrs5:   mov     A,Pjng
          mov     B,#5
          div     AB
          jnz     krmrs6
          mov     Sndi,#'.'
          ljmp    krmrs7
krmrs6:   mov     Sndi,#'-'
krmrs7:   mov     P0,#0C8h
          lcall   w_ins
          mov     P0,Sndi
          lcall   w_chr
          mov     P0,#0D0h
          lcall   w_ins
          ljmp    krmrs3
;
krmrs8:   clr     TR0               ; stop timer
          mov     Dly3,#1
          lcall   delay3
          setb    Mrjm              ; lepas jammer
          mov     SP,#07h
          ljmp    mulai
;
tr_mrs:   lcall   lcdclr            ;\
          mov     DPTR,#tptrmr      ;
```

```
        lcall   linel                   ; |
        mov     Char,#16                ; |
        lcall   tulis                   ; |
        mov     Dly3,#5                 ; | tulis terima morse
        lcall   delay3                  ; |       sandi :
        mov     DPTR,#tpsand            ; | reset geser
        lcall   linel                   ; | reset panjang
        mov     Char,#16                ; |
        lcall   tulis                   ; |
        mov     Cntr,#0                 ; | reset counter
        lcall   rstsnd                  ; | reset sandi
        mov     DPTR,#angka             ; |
        mov     Gser,#0C0h              ; |
trmr00: mov     Pjng,#0                 ;/
trmr01: lcall   scnkpd                  ;\
        cjne    R0,#11,trmr02           ; | if cancel
        mov     SP,#07h                 ; | then back
        ljmp    mulai                   ;/
trmr02: inc     Pjng                    ;\
        lcall   delay4                  ; |
        mov     A,Pjng                  ; |
        mov     B,#25                   ; |
        div     AB                      ; |
        jz      trmr03                  ; | if sangat panjang
        mov     P0,#08Bh                ; | then tulis sandi ' '
        lcall   w_ins                   ; |
        mov     P0,#' '                 ; |
        lcall   w_chr                   ; |
        mov     P0,#0DCh                ; |
        lcall   w_ins                   ;/
;
        jb      Stgs,trmr03             ;\
        lcall   bdgdta                  ; |
        mov     P0,Gser                 ; |
        lcall   w_ins                   ; | tulis
        mov     P0,Chsn                 ; | character
        lcall   w_chr                   ; |
        mov     P0,#0D0h                ; |
        lcall   w_ins                   ;/
        inc     Gser                    ; geser 1 colom
        setb    Stgs                    ; set status geser
        mov     Cntr,#0                 ; reset counter
        lcall   rstsnd                  ; reset sandi
;
trmr03: jb      Mrrx,trmr01             ;\
        clr     Stgs                    ; | if ada RX rst stts gsr & pnjg
        mov     Pjng,#0                 ;/
trmr04: inc     Pjng                    ;\
        lcall   delay4                  ; | it mash ada RX inc pnjg waktu
        jnb     Mrrx,trmr04             ;/
;
        mov     A,Pjng                  ;\
        mov     B,#1                    ;
        div     AB                      ; |
        jnz     trmr05                  ; |
        mov     Sndi,#' '               ; |
        ljmp    trmr07                  ; | if pendek sekali then ' '
```

```
tlkt03: mov     P0,Colm
        lcall   w_ins
        lcall   wr_chr
        lcall   bfchr0
        mov     P0,Colm
        lcall   w_ins
        lcall   tg_lps
        mov     Tmo0,#10
        mov     Tmo1,#0
tlkt04: lcall   scnkpd
        cjne    R0,#10,tlkt05
        djnz    Tmo1,tlkt04
        djnz    Tmo0,tlkt04
        ljmp    tlkt12
tlkt05: cjne    R0,#11,tlkt06
        mov     SP,#07h
        ljmp    mulai
tlkt06: cjne    R0,#12,tlkt07
        ljmp    tlkt13                  ; jump next section
tlkt07: cjne    R0,#13,tlkt08
        ljmp    tlkt04                  ; not recomended
tlkt08: cjne    R0,#14,tlkt09
        ljmp    tlkt04                  ; not recomended
tlkt09: cjne    R0,#15,tlkt10
        ljmp    tlkt04                  ; not recomended
tlkt10: cjne    R0,#16,tlkt11
        ljmp    tlkt04                  ; not recomended
tlkt11: lcall   scnchr
        jnb     Stch,tlkt03
        inc     Colm
        djnz    Jum1,tlkt03
        ljmp    tlkt13
tlkt12: inc     Colm
        mov     P0,Colm
        lcall   w_ins
        djnz    Jum1,lompat
        ljmp    tlkt13
lompat: ljmp    tlkt00
;
tlkt13: mov     DPTR,#tpkirm
        lcall   line2
        mov     Char,#16
        lcall   tulis
        lcall   tg_lps
tlkt14: lcall   scnkpd
        cjne    R0,#11,tlkt15
        mov     SP,#07h
        ljmp    mulai
tlkt15: cjne    R0,#12,tlkt14
;
        clr     Mrjm
        mov     Dly3,#8
        lcall   delay3
tlkt16: mov     A,Ch00
        cjne    A,#' ',tlkt17
        ljmp    tlkt18
tlkt17: lcall   chrsnd
```

```
;
tlkt18: mov     A,Ch01
        cjne    A,#' ',tlkt19
        ljmp    tlkt20
tlkt19: lcall   chrsnd
;
tlkt20: mov     A,Ch02
        cjne    A,#' ',tlkt21
        ljmp    tlkt22
tlkt21: lcall   chrsnd
;
tlkt22: mov     A,Ch03
        cjne    A,#' ',tlkt23
        ljmp    tlkt24
tlkt23: lcall   chrsnd
;
tlkt24: mov     A,Ch04
        cjne    A,#' ',tlkt25
        ljmp    tlkt26
tlkt25: lcall   chrsnd
;
tlkt26: mov     A,Ch05
        cjne    A,#' ',tlkt27
        ljmp    tlkt28
tlkt27: lcall   chrsnd
;
tlkt28: mov     A,Ch06
        cjne    A,#' ',tlkt29
        ljmp    tlkt30
tlkt29: lcall   chrsnd
;
tlkt30: mov     A,Ch07
        cjne    A,#' ',tlkt31
        ljmp    tlkt32
tlkt31: lcall   chrsnd
;
tlkt32: mov     A,Ch08
        cjne    A,#' ',tlkt33
        ljmp    tlkt34
tlkt33: lcall   chrsnd
;
tlkt34: mov     A,Ch09
        cjne    A,#' ',tlkt35
        ljmp    tlkt36
tlkt35: lcall   chrsnd
;
tlkt36: mov     A,Ch0A
        cjne    A,#' ',tlkt37
        ljmp    tlkt38
tlkt37: lcall   chrsnd
;
tlkt38: mov     A,Ch0B
        cjne    A,#' ',tlkt39
        ljmp    tlkt40
tlkt39: lcall   chrsnd
;
tlkt40: mov     A,Ch0C
```

```
        cjne    A,#' ',tlkt41
        ljmp    tlkt42
tlkt41: lcall   chrsnd
;
tlkt42: mov     A,Ch0D
        cjne    A,#' ',tlkt43
        ljmp    tlkt44
tlkt43: lcall   chrsnd
;
tlkt44: mov     A,Ch0E
        cjne    A,#' ',tlkt45
        ljmp    tlkt46
tlkt45: lcall   chrsnd
;
tlkt46: mov     A,Ch0F
        cjne    A,#' ',tlkt47
        ljmp    tlkt46
tlkt47: lcall   chrsnd
;
tlkt48: mov     Dly3,#2
        lcall   delay3
        setb    Mrjm
        mov     SP,#07h
        ljmp    mulai
;
lesons: lcall   lcdclr
        mov     DPTR,#tpdtsm
        lcall   line1
        mov     Char,#16
        lcall   tulis
        lcall   tg lps
        mov     R2,#1
lsns00: cjne    R2,#01,lsns01
        mov     DPTR,#tpchrA
lsns01: cjne    R2,#02,lsns02
        mov     DPTR,#tpchrB
lsns02: cjne    R2,#03,lsns03
        mov     DPTR,#tpchrC
lsns03: cjne    R2,#04,lsns04
        mov     DPTR,#tpchrD
lsns04: cjne    R2,#05,lsns05
        mov     DPTR,#tpchrE
lsns05: cjne    R2,#06,lsns06
        mov     DPTR,#tpchrF
lsns06: cjne    R2,#07,lsns07
        mov     DPTR,#tpchrG
lsns07: cjne    R2,#08,lsns08
        mov     DPTR,#tpchrH
lsns08: cjne    R2,#09,lsns09
        mov     DPTR,#tpchrI
lsns09: cjne    R2,#10,lsns10
        mov     DPTR,#tpchrJ
lsns10: cjne    R2,#11,lsns11
        mov     DPTR,#tpchrK
lsns11: cjne    R2,#12,lsns12
        mov     DPTR,#tpchrL
lsns12: cjne    R2,#13,lsns13
```

```
        lcall   cekchr
        jnb     Stts,bddt07
        mov     Chsn,#'H'
        ljmp    bddt99
bddt07: mov     DPTR,#tpchrI
        lcall   cekchr
        jnb     Stts,bddt08
        mov     Chsn,#'I'
        ljmp    bddt99
bddt08: mov     DPTR,#tpchrJ
        lcall   cekchr
        jnb     Stts,bddt09
        mov     Chsn,#'J'
        ljmp    bddt99
bddt09: mov     DPTR,#tpchrK
        lcall   cekchr
        jnb     Stts,bddt10
        mov     Chsn,#'K'
        ljmp    bddt99
bddt10: mov     DPTR,#tpchrL
        lcall   cekchr
        jnb     Stts,bddt11
        mov     Chsn,#'L'
        ljmp    bddt99
bddt11: mov     DPTR,#tpchrM
        lcall   cekchr
        jnb     Stts,bddt12
        mov     Chsn,#'M'
        ljmp    bddt99
bddt12: mov     DPTR,#tpchrN
        lcall   cekchr
        jnb     Stts,bddt13
        mov     Chsn,#'N'
        ljmp    bddt99
bddt13: mov     DPTR,#tpchrO
        lcall   cekchr
        jnb     Stts,bddt14
        mov     Chsn,#'O'
        ljmp    bddt99
bddt14: mov     DPTR,#tpchrP
        lcall   cekchr
        jnb     Stts,bddt15
        mov     Chsn,#'P'
        ljmp    bddt99
bddt15: mov     DPTR,#tpchrQ
        lcall   cekchr
        jnb     Stts,bddt16
        mov     Chsn,#'Q'
        ljmp    bddt99
bddt16: mov     DPTR,#tpchrR
        lcall   cekchr
        jnb     Stts,bddt17
        mov     Chsn,#'R'
        ljmp    bddt99
bddt17: mov     DPTR,#tpchrS
        lcall   cekchr
        jnb     Stts,bddt18
```

```
        mov     Chsn,#'S'
        ljmp    bddt99
bddt18: mov     DPTR,#tpchrT
        lcall   cekchr
        jnb     Stts,bddt19
        mov     Chsn,#'T'
        ljmp    bddt99
bddt19: mov     DPTR,#tpchrU
        lcall   cekchr
        jnb     Stts,bddt20
        mov     Chsn,#'U'
        ljmp    bddt99
bddt20: mov     DPTR,#tpchrV
        lcall   cekchr
        jnb     Stts,bddt21
        mov     Chsn,#'V'
        ljmp    bddt99
bddt21: mov     DPTR,#tpchrW
        lcall   cekchr
        jnb     Stts,bddt22
        mov     Chsn,#'W'
        ljmp    bddt99
bddt22: mov     DPTR.#tpchrX
        lcall   cekchr
        jnb     Stts,bddt23
        mov     Chsn,#'X'
        ljmp    bddt99
bddt23: mov     DPTR,#tpchrY
        lcall   cekchr
        jnb     Stts,bddt24
        mov     Chsn,#'Y'
        ljmp    bddt99
bddt24: mov     DPTR,#tpchrZ
        lcall   cekchr
        jnb     Stts,bddt25
        mov     Chsn,#'Z'
        ljmp    bddt99
;
bddt25: mov     DPTR,#tpchr0
        lcall   cekchr
        jnb     Stts,bddt26
        mov     Chsn,#'0'
        ljmp    bddt99
bddt26: mov     DPTR,#tpchr1
        lcall   cekchr
        jnb     Stts,bddt27
        mov     Chsn,#'1'
        ljmp    bddt99
bddt27: mov     DPTR,#tpchr2
        lcall   cekchr
        jnb     Stts,bddt28
        mov     Chsn,#'2'
        ljmp    bddt99
bddt28: mov     DPTR,#tpchr3
        lcall   cekchr
        jnb     Stts,bddt29
        mov     Chsn,#'3'
```

```
        ljmp    bddt99
bddt29: mov     DPTR,#tpchr4
        lcall   cekchr
        jnb     Stts,bddt30
        mov     Chsn,#'4'
        ljmp    bddt99
bddt30: mov     DPTR,#tpchr5
        lcall   cekchr
        jnb     Stts,bddt31
        mov     Chsn,#'5'
        ljmp    bddt99
bddt31: mov     DPTR,#tpchr6
        lcall   cekchr
        jnb     Stts,bddt32
        mov     Chsn,#'6'
        ljmp    bddt99
bddt32: mov     DPTR,#tpchr7
        lcall   cekchr
        jnb     Stts,bddt33
        mov     Chsn,#'7'
        ljmp    bddt99
bddt33: mov     DPTR,#tpchr8
        lcall   cekchr
        jnb     Stts,bddt34
        mov     Chsn,#'8'
        ljmp    bddt99
bddt34: mov     DPTR,#tpchr9
        lcall   cekchr
        jnb     Stts,bddt35
        mov     Chsn,#'9'
        ljmp    bddt99
;
bddt35: mov     DPTR,#tpchtt
        lcall   cekchr
        jnb     Stts,bddt36
        mov     Chsn,#'.'
        ljmp    bddt99
bddt36: mov     DPTR,#tpchkm
        lcall   cekchr
        jnb     Stts,bddt37
        mov     Chsn,#','
        ljmp    bddt99
bddt37: mov     DPTR,#tpchtd
        lcall   cekchr
        jnb     Stts,bddt38
        mov     Chsn,#':'
        ljmp    bddt99
bddt38: mov     DPTR,#tpchmn
        lcall   cekchr
        jnb     Stts,bddt39
        mov     Chsn,#'-'
        ljmp    bddt99
bddt39: mov     DPTR,#tpchgm
        lcall   cekchr
        jnb     Stts,bddt40
        mov     Chsn,#'/'
        ljmp    bddt99
```

```
;
bddt40: mov     DPTR,#tpchks
        lcall   cekchr
        jnb     Stts,bddt99
        mov     Chsn,#' '
        ljmp    bddt99
;
bddt99: ret
;
cekchr: inc     DPTR
        inc     DPTR
        inc     DPTR
        inc     DPTR
        inc     DPTR
        inc     DPTR
        inc     DPTR
        inc     DPTR
        inc     DPTR
        clr     Stts
        clr     A
        movc    A,@A+DPTR
        mov     B,Snd0
        clr     C
        subb    A,B
        jnz     ckchr
        inc     DPTR
        clr     A
        movc    A,@A+DPTR
        mov     B,Snd1
        clr     C
        subb    A,B
        jnz     ckchr
        inc     DPTR
        clr     A
        movc    A,@A+DPTR
        mov     B,Snd2
        clr     C
        subb    A,B
        jnz     ckchr
        inc     DPTR
        clr     A
        movc    A,@A+DPTR
        mov     B,Snd3
        clr     C
        subb    A,B
        jnz     ckchr
        inc     DPTR
        clr     A
        movc    A,@A+DPTR
        mov     B,Snd4
        clr     C
        subb    A,B
        jnz     ckchr
        inc     DPTR
        clr     A
        movc    A,@A+DPTR
        mov     B,Snd5
```

```
        clr     C
        subb    A,B
        jnz     ckchr
        setb    Stts
ckchr:  ret
;
bfchr0: mov     R4,Colm
        cjne    R4,#080h,bfch00
        mov     Ch00,A
bfch00: cjne    R4,#081h,bfch01
        mov     Ch01,A
bfch01: cjne    R4,#082h,bfch02
        mov     Ch02,A
bfch02: cjne    R4,#083h,bfch03
        mov     Ch03,A
bfch03: cjne    R4,#084h,bfch04
        mov     Ch04,A
bfch04: cjne    R4,#085h,bfch05
        mov     Ch05,A
bfch05: cjne    R4,#086h,bfch06
        mov     Ch06,A
bfch06: cjne    R4,#087h,bfch07
        mov     Ch07,A
bfch07: cjne    R4,#088h,bfch08
        mov     Ch08,A
bfch08: cjne    R4,#089h,bfch09
        mov     Ch09,A
bfch09: cjne    R4,#08Ah,bfch0A
        mov     Ch0A,A
bfch0A: cjne    R4,#08Bh,bfch0B
        mov     Ch0B,A
bfch0B: cjne    R4,#08Ch,bfch0C
        mov     Ch0C,A
bfch0C: cjne    R4,#08Dh,bfch0D
        mov     Ch0D,A
bfch0D: cjne    R4,#08Eh,bfch0E
        mov     Ch0E,A
bfch0E: cjne    R4,#08Fh,bfch0F
        mov     Ch0F,A
bfch0F: ret
;
scnchr: clr     Stch
        mov     A,R0
        mov     B,Dtkp
        clr     C
        subb    A,B
        jnz     scchr0
        ljmp    scchr1
scchr0: setb    Stch
        ljmp    scchr3
scchr1: djnz    R1,scchr2
        mov     R1,Cntr
        ljmp    scchr3
scchr2: inc     DPTR
        ljmp    scchr4
scchr3: mov     Dtkp,R0
        mov     A,Dtkp
```

```
        lcall   sklmpk
scchr4: clr     A
        ret
;
sklmpk: cjne    A,#1,sklmp0
        mov     DPTR,#klmpk0
        mov     Cntr,#2
        mov     R1,Cntr
sklmp0: cjne    A,#2,sklmp1
        mov     DPTR,#klmpk1
        mov     Cntr,#4
        mov     R1,Cntr
sklmp1: cjne    A,#3,sklmp2
        mov     DPTR,#klmpk2
        mov     Cntr,#4
        mov     R1,Cntr
sklmp2: cjne    A,#4,sklmp3
        mov     DPTR,#klmpk3
        mov     Cntr,#4
        mov     R1,Cntr
sklmp3: cjne    A,#5,sklmp4
        mov     DPTR,#klmpk4
        mov     Cntr,#4
        mov     R1,Cntr
sklmp4: cjne    A,#6,sklmp5
        mov     DPTR,#klmpk5
        mov     Cntr,#4
        mov     R1,Cntr
sklmp5: cjne    A,#7,sklmp6
        mov     DPTR,#klmpk6
        mov     Cntr,#5
        mov     R1,Cntr
sklmp6: cjne    A,#8,sklmp7
        mov     DPTR,#klmpk7
        mov     Cntr,#4
        mov     R1,Cntr
sklmp7: cjne    A,#9,sklmp8
        mov     DPTR,#klmpk8
        mov     Cntr,#5
        mov     R1,Cntr
sklmp8: cjne    A,#0,sklmp9
        mov     DPTR,#klmpk9
        mov     Cntr,#2
        mov     R1,Cntr
sklmp9: ret
;
chrsnd: cjne    A,#'A',chsn00       ; character to send
        mov     DPTR,#tpchrA
chsn00: cjne    A,#'B',chsn01
        mov     DPTR,#tpchrB
chsn01: cjne    A,#'C',chsn02
        mov     DPTR,#tpchrC
chsn02: cjne    A,#'D',chsn03
        mov     DPTR,#tpchrD
chsn03: cjne    A,#'E',chsn04
        mov     DPTR,#tpchrE
chsn04: cjne    A,#'F',chsn05
```

```
        mov     DPTR,#tpchrF
chsn05: cjne    A,#'G',chsn06
        mov     DPTR,#tpchrG
chsn06: cjne    A,#'H',chsn07
        mov     DPTR,#tpchrH
chsn07: cjne    A,#'I',chsn08
        mov     DPTR,#tpchrI
chsn08: cjne    A,#'J',chsn09
        mov     DPTR,#tpchrJ
chsn09: cjne    A,#'K',chsn10
        mov     DPTR,#tpchrK
chsn10: cjne    A,#'L',chsn11
        mov     DPTR,#tpchrL
chsn11: cjne    A,#'M',chsn12
        mov     DPTR,#tpchrM
chsn12: cjne    A,#'N',chsn13
        mov     DPTR,#tpchrN
chsn13: cjne    A,#'O',chsn14
        mov     DPTR,#tpchrO
chsn14: cjne    A,#'P',chsn15
        mov     DPTR,#tpchrP
chsn15: cjne    A,#'Q',chsn16
        mov     DPTR,#tpchrQ
chsn16: cjne    A,#'R',chsn17
        mov     DPTR,#tpchrR
chsn17: cjne    A,#'S',chsn18
        mov     DPTR,#tpchrS
chsn18: cjne    A,#'T',chsn19
        mov     DPTR,#tpchrT
chsn19: cjne    A,#'U',chsn20
        mov     DPTR,#tpchrU
chsn20: cjne    A,#'V',chsn21
        mov     DPTR,#tpchrV
chsn21: cjne    A,#'W',chsn22
        mov     DPTR,#tpchrW
chsn22: cjne    A,#'X',chsn23
        mov     DPTR,#tpchrX
chsn23: cjne    A,#'Y',chsn24
        mov     DPTR,#tpchrY
chsn24: cjne    A,#'Z',chsn25
        mov     DPTR,#tpchrZ
;
chsn25: cjne    A,#'0',chsn26
        mov     DPTR,#tpchr0
chsn26: cjne    A,#'1',chsn27
        mov     DPTR,#tpchr1
chsn27: cjne    A,#'2',chsn28
        mov     DPTR,#tpchr2
chsn28: cjne    A,#'3',chsn29
        mov     DPTR,#tpchr3
chsn29: cjne    A,#'4',chsn30
        mov     DPTR,#tpchr4
chsn30: cjne    A,#'5',chsn31
        mov     DPTR,#tpchr5
chsn31: cjne    A,#'6',chsn32
        mov     DPTR,#tpchr6
chsn32: cjne    A,#'7',chsn33
```

```
        mov     DPTR,#tpchr7
chsn33: cjne    A,#'8',chsn34
        mov     DPTR,#tpchr8
chsn34: cjne    A,#'9',chsn35
        mov     DPTR,#tpchr9
;
chsn35: cjne    A,#',',chsn36
        mov     DPTR,#tpchkm
chsn36: cjne    A,#' ',chsn37
        mov     DPTR,#tpchks
;
chsn37: inc     DPTR
        inc     DPTR
        inc     DPTR
        inc     DPTR
        inc     DPTR
        inc     DPTR
        inc     DPTR
        inc     DPTR
        inc     DPTR
chsn38: clr     A
        movc    A,@A+DPTR
        cjne    A,#' ',chsn39
        ljmp    chsn41
chsn39: cjne    A,#'.',chsn40
        clr     Mrtx
        mov     Dly3,#1
        lcall   delay3
        setb    Mrtx
        mov     Dly3,#2
        lcall   delay3
        inc     DPTR
        ljmp    chsn38
chsn40: cjne    A,#'-',chsn41
        clr     Mrtx
        mov     Dly3,#2
        lcall   delay3
        setb    Mrtx
        mov     Dly3,#2
        lcall   delay3
        inc     DPTR
        ljmp    chsn38
;
chsn41: mov     Dly3,#8
        lcall   delay3
        ret
;
pnggil: jb      Mrtn,pnggl1
        clr     Mrjm
        mov     Dly3,#3
        lcall   delay3
pngg10: clr     Mrtx
        lcall   delay4
        setb    Mrtx
        lcall   delay4
        jnb     Mrtb,pngg10
        mov     Dly3,#1
```

```
        lcall   delay3
        setb    Mrjm
pnggll: ret
;
rstsnd: mov     Snd0,#' '
        mov     Snd1,#' '
        mov     Snd2,#' '
        mov     Snd3,#' '
        mov     Snd4,#' '
        mov     Snd5,#' '
        ret
;
rstchr: mov     Ch00,#' '
        mov     Ch01,#' '
        mov     Ch02,#' '
        mov     Ch03,#' '
        mov     Ch04,#' '
        mov     Ch05,#' '
        mov     Ch06,#' '
        mov     Ch07,#' '
        mov     Ch08,#' '
        mov     Ch09,#' '
        mov     Ch0A,#' '
        mov     Ch0B,#' '
        mov     Ch0C,#' '
        mov     Ch0D,#' '
        mov     Ch0E,#' '
        mov     Ch0F,#' '
        ret
;
nilai:  mov     B,#100
        div     AB
        lcall   wr_chr
        mov     A,B
nil:    mov     B,#10
        div     AB
        lcall   wr_chr
        mov     A,B
        lcall   wr_chr
        ret
;
cntdwn: mov     TL0,#0B0h           ; reset timer 0 low
        mov     TH0,#03Ch           ; reset timer 0 high
        clr     TF0                 ; reset flag timer 0
        djnz    CTmo,ctdwn0
        mov     CTmo,#20
        dec     Tmot
ctdwn0: reti
;
tmr_in: mov     Dly3,#1
        lcall   delay3
        mov     TMOD,#11h           ; mode timer 16 bit
        mov     TL0,#0B0h           ; set timer 0 low
        mov     TH0,#03Ch           ; set timer 0 high
        clr     TF0                 ; reset flag timer 0
        setb    ET0                 ; enable interupt timer 0
        setb    EA                  ; enable interupt flag
```

```
        ret
;
line1:  mov     P0,#0B0h
        lcall   w_ins
        ret
;
line2:  mov     P0,#0C0h
        lcall   w_ins
        ret
;
tulis:  clr     A
        lcall   wr_chr
        inc     DPTR
        djnz    Char,tulis
        ret
;
wr_chr: movc    A,@A+DPTR
        mov     P0,A
        lcall   w_chr
        ret
;
w_ins:  clr     Enbl
        clr     Rest
        setb    Enbl
        clr     Enbl
        lcall   delay0
        ret
;
w_chr:  clr     Enbl
        setb    Rest
        setb    Enbl
        clr     Enbl
        lcall   delay0
        ret
;
lcd_in: mov     Dly3,#1
        lcall   delay3
        mov     P0,#01h         ; Display Clear
        lcall   w_ins
        mov     P0,#38h         ; Function Set
        lcall   w_ins
        mov     P0,#0Eh         ; Display On, Cursor, Blink
        lcall   w_ins
        mov     P0,#06h         ; Entry Mode
        lcall   w_ins
        mov     P0,#02h         ; Cursor Home
        lcall   w_ins
        ret
;
lcdclr: mov     P0,#01h         ; Display Clear
        lcall   w_ins
        lcall   delay0
        lcall   delay0
        lcall   delay0
        ret
;
scnkpd: mov     R0,#10
```

```
        lcall   delay0
col1:   mov     P1,#11111110b
        mov     A,P1
c1b1:   cjne    A,#11101110b,c1b2
        mov     R0,#1
c1b2:   cjne    A,#11011110b,c1b3
        mov     R0,#2
c1b3:   cjne    A,#10111110b,c1b4
        mov     R0,#3
c1b4:   cjne    A,#01111110b,col2
        mov     R0,#13
;
col2:   mov     P1,#11111101b
        mov     A,P1
c2b1:   cjne    A,#11101101b,c2b2
        mov     R0,#4
c2b2:   cjne    A,#11011101b,c2b3
        mov     R0,#5
c2b3:   cjne    A,#10111101b,c2b4
        mov     R0,#6
c2b4:   cjne    A,#01111101b,col3
        mov     R0,#14
;
col3:   mov     P1,#11111011b
        mov     A,P1
c3b1:   cjne    A,#11101011b,c3b2
        mov     R0,#7
c3b2:   cjne    A,#11011011b,c3b3
        mov     R0,#8
c3b3:   cjne    A,#10111011b,c3b4
        mov     R0,#9
c3b4:   cjne    A,#01111011b,col4
        mov     R0,#15
;
col4:   mov     P1,#11110111b
        mov     A,P1
c4b1:   cjne    A,#11100111b,c4b2
        mov     R0,#11
c4b2:   cjne    A,#11010111b,c4b3
        mov     R0,#0
c4b3:   cjne    A,#10110111b,c4b4
        mov     R0,#12
c4b4:   cjne    A,#01110111b,back
        mov     R0,#16
back:   ret
;
tg_tkn: lcall   pnggil
        lcall   scnkpd
tgtkn0: cjne    R0,#16,tgtkn1
        ljmp    tg_tkn
tgtkn1: cjne    R0,#15,tgtkn2
        ljmp    tg_tkn
tgtkn2: cjne    R0,#14,tgtkn3
        ljmp    tg_tkn
tgtkn3: cjne    R0,#13,tgtkn4
        ljmp    tg_tkn
tgtkn4: cjne    R0,#10,tgtkn5
```

```
        ljmp    tg_tkn
tgtkn5: ret
;
tg_lps: lcall   scnkpd
        cjne    R0,#10,tg_lps
        ret
;
delay0: djnz    Dly0,delay0
        ret
;
delay1: lcall   scnkpd
        cjne    R0,#13,dely10
        ljmp    kr_mrs
dely10: cjne    R0,#14,dely11
        ljmp    tr_mrs
dely11: cjne    R0,#15,dely12
        ljmp    tlskta
dely12: cjne    R0,#16,dely13
        ljmp    lesons
dely13: lcall   pnggil
        djnz    Dly1,delay1
        ret
;
delay2: mov     Dly2,#20
dely2:  lcall   delay1
        djnz    Dly2,dely2
        ret
;
delay3: lcall   delay0
        djnz    Dly1,dclay3
        djnz    Dly3,delay3
        ret
;
delay4: mov     Dly1,#75
dely40: lcall   delay0
        djnz    Dly1,dely40
        ret
;
nama:   DB      ' Yuri  Darmawan '
nim:    DB      ' NIM: 03.17.099 '
jur:    DB      ' Teknik Elektro '
univ:   DB      '   ITN Malang   '
tpkrmr: DB      '  Kirim  Morse  '
tptmot: DB      '  Time Out: 00  '
tpsand: DB      '    Sandi:      '
tptrmr: DB      '  Terima Morse  '
tptlkl: DB      ' Tulis  Kalimat '
tpkirm: DB      '    Kirim  ?    '
angka:  DB      '0123456789      '
;
tpdtsm: DB      'Data Sandi Morse'
tpchrA: DB      ' Char A  .-     '
tpchrB: DB      ' Char B  -...   '
tpchrC: DB      ' Char C  -.-.   '
tpchrD: DB      ' Char D  -..    '
tpchrE: DB      ' Char E  .      '
tpchrF: DB      ' Char F  ..-.   '
```

```
tpchrG: DB      ' Char G  --.     '
tpchrH: DB      ' Cnar H  ....    '
tpchrI: DB      ' Char I  ..      '
tpchrJ: DB      ' Char J  .---    '
tpchrK: DB      ' Char K  -.-     '
tpchrL: DB      ' Char L  .-..    '
tpchrM: DB      ' Char M  --      '
tpchrN: DB      ' Char N  -.      '
tpchrO: DB      ' Char O  ---     '
tpchrP: DB      ' Char P  .--.    '
tpchrQ: DB      ' Char Q  --.-    '
tpchrR: DB      ' Char R  .-.     '
tpchrS: DB      ' Char S  ...     '
tpchrT: DB      ' Char T  -       '
tpchrU: DB      ' Char U  ..-     '
tpchrV: DB      ' Char V  ...-    '
tpchrW: DB      ' Char W  .--     '
tpchrX: DB      ' Char X  -..-    '
tpchrY: DB      ' Char Y  -.--    '
tpchrZ: DB      ' Char Z  --..    '
tpchtt: DB      ' Char .  .-.-.-  '
tpchkm: DB      ' Char ,  --..--  '
tpchtd: DB      ' Char :  ---...  '
tpchmn: DB      ' Char -  -....-  '
tpchgm: DB      ' Char /  -..-.   '
tpchr0: DB      ' Char 0  .----   '
tpchr1: DB      ' Char 1  ..---   '
tpchr2: DB      ' Char 2  ...--   '
tpchr3: DB      ' Char 3  ....-   '
tpchr4: DB      ' Char 4  .....   '
tpchr5: DB      ' Char 5  -....   '
tpchr6: DB      ' Char 6  --...   '
tpchr7: DB      ' Char 7  ---..   '
tpchr8: DB      ' Char 8  ----.   '
tpchr9: DB      ' Char 9  -----   '
tpchks: DB      ' Char            '
;
klmpk0: DB      ',1'              ; 2
klmpk1: DB      'ABC2'            ; 4
klmpk2: DB      'DEF3'            ; 4
klmpk3: DB      'GHI4'            ; 4
klmpk4: DB      'JKL5'            ; 4
klmpk5: DB      'MNO6'            ; 4
klmpk6: DB      'PQRS7'           ; 5
klmpk7: DB      'TUV8'            ; 4
klmpk8: DB      'WXYZ9'           ; 5
klmpk9: DB      ' 0'              ; 2
;
        end
```

DATA SHEET

tures

- npatible with MCS-51® Products
- 3ytes of In-System Programmable (ISP) Flash Memory
  - Endurance: 1000 Write/Erase Cycles
- / to 5.5V Operating Range
- y Static Operation: 0 Hz to 33 MHz
- ee level Program Memory Lock
- x 8-bit Internal RAM
- Programmable I/O Lines
- 16-bit Timer/Counters
- Interrupt Sources
- l Duplex UART Serial Channel
- v-power Idle and Power-down Modes
- rrupt Recovery from Power-down Mode
- tchdog Timer
- al Data Pointer
- wer-off Flag
- t Programming Time
- xible ISP Programming (Byte and Page Mode)

scription

AT89S51 is a low-power, high-performance CMOS 8-bit microcontroller with 4K s of in-system programmable Flash memory. The device is manufactured using el's high-density nonvolatile memory technology and is compatible with the industandard 80C51 instruction set and pinout. The on-chip Flash allows the program nory to be reprogrammed in-system or by a conventional nonvolatile memory prommer. By combining a versatile 8-bit CPU with in-system programmable Flash on a olithic chip, the Atmel AT89S51 is a powerful microcontroller which provides a ly-flexible and cost-effective solution to many embedded control applications.

AT89S51 provides the following standard features: 4K bytes of Flash, 128 bytes of M, 32 I/O lines, Watchdog timer, two data pointers, two 16-bit timer/counters, a fiveor two-level interrupt architecture, a full duplex serial port, on-chip oscillator, and ck circuitry. In addition, the AT89S51 is designed with static logic for operation wn to zero frequency and supports two software selectable power saving modes. e Idle Mode stops the CPU while allowing the RAM, timer/counters, serial port, and rrupt system to continue functioning. The Power-down mode saves the RAM conts but freezes the oscillator, disabling all other chip functions until the next external errupt or hardware reset.

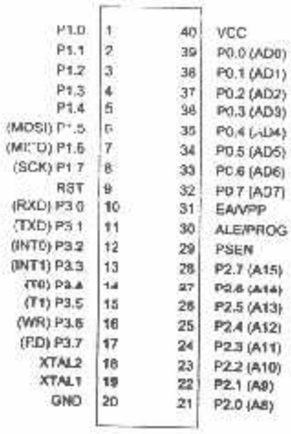
8-bit Microcontroller with 4K Bytes In-System Programmable Flash

AT89S51

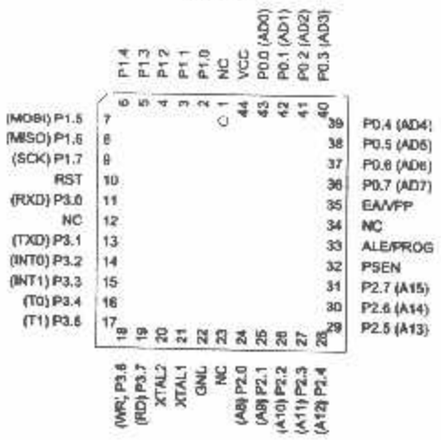
Rev. 2487A–10/01

Configurations

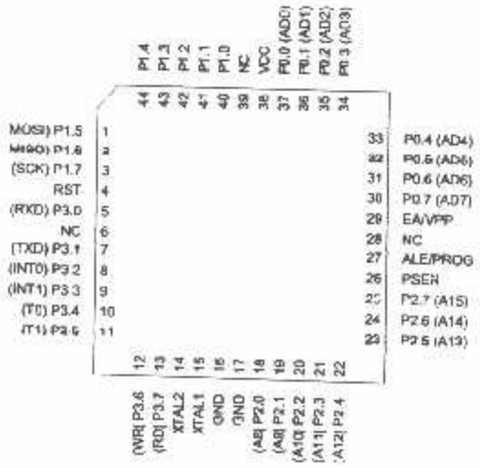
PDIP



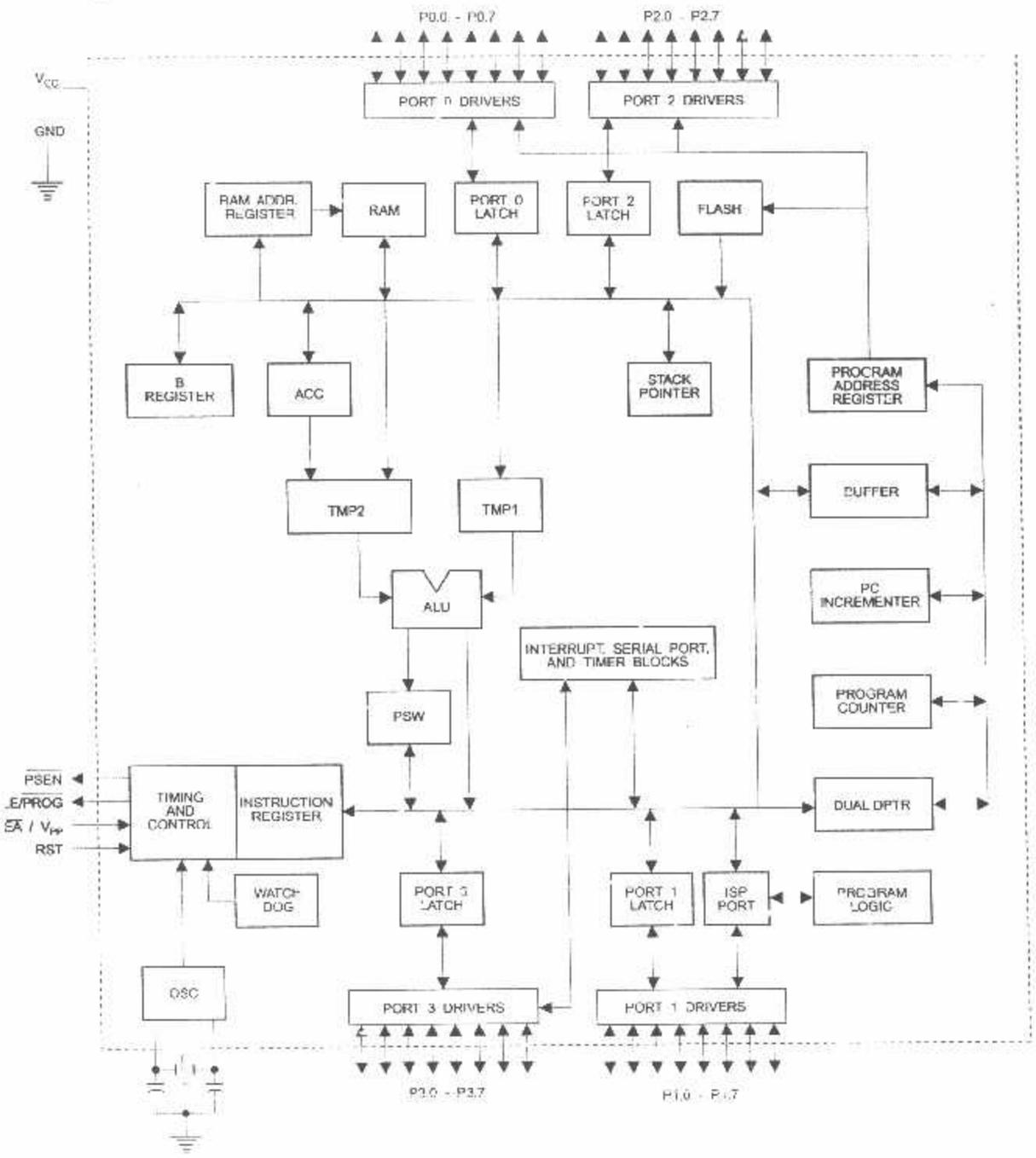
PLCC



TQFP



ck Diagram


P0.0 - P0.7
P2.0 - P2.7
V_{CC}
GND
PORT 0 DRIVERS
PORT 2 DRIVERS
RAM ADDR. REGISTER
RAM
PORT 0 LATCH
PORT 2 LATCH
FLASH
B REGISTER
ACC
STACK POINTER
PROGRAM ADDRESS REGISTER
BUFFER
TMP2
TMP1
ALU
PC INCREMENTER
INTERRUPT, SERIAL PORT, AND TIMER BLOCKS
PROGRAM COUNTER
PSW
PSEN
ALE/PROG
EA / V_{PP}
RST
TIMING AND CONTROL
INSTRUCTION REGISTER
DUAL DPTR
WATCH DOG
PORT 3 LATCH
PORT 1 LATCH
ISP PORT
PROGRAM LOGIC
OSC
PORT 3 DRIVERS
PORT 1 DRIVERS
P3.0 - P3.7
P1.0 - P1.7

1 Description

C Supply voltage.

D Ground.

rt 0 Port 0 is an 8-bit open drain bidirectional I/O port. As an output port, each pin can sink eight TTL inputs. When 1s are written to port 0 pins, the pins can be used as high-impedance inputs.

Port 0 can also be configured to be the multiplexed low-order address/data bus during accesses to external program and data memory. In this mode, P0 has internal pull-ups.

Port 0 also receives the code bytes during Flash programming and outputs the code bytes during program verification. **External pull-ups are required during program verification.**

rt 1 Port 1 is an 8-bit bidirectional I/O port with internal pull-ups. The Port 1 output buffers can sink/source four TTL inputs. When 1s are written to Port 1 pins, they are pulled high by the internal pull-ups and can be used as inputs. As inputs, Port 1 pins that are externally being pulled low will source current (I_{IL}) because of the internal pull-ups.

Port 1 also receives the low-order address bytes during Flash programming and verification.

Port Pin	Alternate Functions
P1.5	MOSI (used for In-System Programming)
P1.6	MISO (used for In-System Programming)
P1.7	SCK (used for In-System Programming)

rt 2 Port 2 is an 8-bit bidirectional I/O port with internal pull-ups. The Port 2 output buffers can sink/source four TTL inputs. When 1s are written to Port 2 pins, they are pulled high by the internal pull-ups and can be used as inputs. As inputs, Port 2 pins that are externally being pulled low will source current (I_{IL}) because of the internal pull-ups.

Port 2 emits the high-order address byte during fetches from external program memory and during accesses to external data memory that use 16-bit addresses (MOVX @ DPTR). In this application, Port 2 uses strong internal pull-ups when emitting 1s. During accesses to external data memory that use 8-bit addresses (MOVX @ RI), Port 2 emits the contents of the P2 Special Function Register.

Port 2 also receives the high-order address bits and some control signals during Flash programming and verification.

ort 3 Port 3 is an 8-bit bidirectional I/O port with internal pull-ups. The Port 3 output buffers can sink/source four TTL inputs. When 1s are written to Port 3 pins, they are pulled high by the internal pull-ups and can be used as inputs. As inputs, Port 3 pins that are externally being pulled low will source current (I_{IL}) because of the pull-ups.

Port 3 receives some control signals for Flash programming and verification.

Port 3 also serves the functions of various special features of the AT89S51, as shown in the following table.

Port Pin	Alternate Functions
P3.0	RXD (serial input port)
P3.1	TXD (serial output port)
P3.2	$\overline{INT0}$ (external interrupt 0)
P3.3	$\overline{INT1}$ (external interrupt 1)
P3.4	T0 (timer 0 external input)
P3.5	T1 (timer 1 external input)
P3.6	$\overline{WR}$ (external data memory write strobe)
P3.7	$\overline{RD}$ (external data memory read strobe)

Reset input. A high on this pin for two machine cycles while the oscillator is running resets the device. This pin drives High for 98 oscillator periods after the Watchdog times out. The DISRTO bit in SFR AUXR (address 8EH) can be used to disable this feature. In the default state of bit DISRTO, the RESET HIGH out feature is enabled.

/$\overline{PROG}$

Address Latch Enable (ALE) is an output pulse for latching the low byte of the address during accesses to external memory. This pin is also the program pulse input ($\overline{PROG}$) during Flash programming.

In normal operation, ALE is emitted at a constant rate of 1/6 the oscillator frequency and may be used for external timing or clocking purposes. Note, however, that one ALE pulse is skipped during each access to external data memory.

If desired, ALE operation can be disabled by setting bit 0 of SFR location 8EH. With the bit set, ALE is active only during a MOVX or MOVC instruction. Otherwise, the pin is weakly pulled high. Setting the ALE-disable bit has no effect if the microcontroller is in external execution mode.

$\overline{EN}$

Program Store Enable ($\overline{PSEN}$) is the read strobe to external program memory.

When the AT89S51 is executing code from external program memory, $\overline{PSEN}$ is activated twice each machine cycle, except that two $\overline{PSEN}$ activations are skipped during each access to external data memory.

V/VPP

External Access Enable. $\overline{EA}$ must be strapped to GND in order to enable the device to fetch code from external program memory locations starting at 0000H up to FFFFH. Note, however, that if lock bit 1 is programmed, $\overline{EA}$ will be internally latched on reset.

$\overline{EA}$ should be strapped to V_{CC} for internal program executions.

This pin also receives the 12-volt programming enable voltage (V_{PP}) during Flash programming.

TAL1

Input to the inverting oscillator amplifier and input to the internal clock operating circuit.

TAL2

Output from the inverting oscillator amplifier

cial ction isters

A map of the on-chip memory area called the Special Function Register (SFR) space is shown in Table 1.

Note that not all of the addresses are occupied, and unoccupied addresses may not be implemented on the chip. Read accesses to these addresses will in general return random data, and write accesses will have an indeterminate effect.

1. AT89S51 SFR Map and Reset Values

8H								0FFH
0H	B 00000000							0F7H
8H								0EFH
0H	ACC 00000000							0E7H
8H								0DFH
0H	PSW 00000000							0D7H
8H								0CFH
0H								0C7H
8H	IP XX000000							0BFH
0H	P3 11111111							0B7H
8H	IE 0X000000							0AFH
A0H	P2 11111111		AUXR1 XXXXXXX0				WDTRST XXXXXXXX	0A7H
98H	SCON 00000000	SBUF XXXXXXXX						9FH
90H	P1 11111111							97H
88H	TCON 00000000	TMOD 00000000	TL0 00000000	TL1 00000000	TH0 00000000	TH1 00000000	AUXR XXX00XX0	8FH
80H	P0 11111111	SP 00000111	DP0L 00000000	DP0H 00000000	DP1L 00000000	DP1H 00000000	PCON 0XXX0000	87H

User software should not write 1s to these unlisted locations, since they may be used in future products to invoke new features. In that case, the reset or inactive values of the new bits will always be 0.

Interrupt Registers: The individual interrupt enable bits are in the IE register. Two priorities can be set for each of the five interrupt sources in the IP register.

Table 2. AUXR: Auxiliary Register

AUXR Address = 8EH Reset Value = XXX00XX0B

Not Bit Addressable

Bit	7	6	5	4	3	2	1	0
	–	–	–	WDIDLE	DISRTO	–	–	DISALE

– Reserved for future expansion

DISALE Disable/Enable ALE

DISALE Operating Mode

0 ALE is emitted at a constant rate of 1/6 the oscillator frequency

1 ALE is active only during a MOVX or MOVC instruction

DISRTO Disable/Enable Reset out

DISRTO

0 Reset pin is driven High after WDT times out

1 Reset pin is input only

WDIDLE Disable/Enable WDT in IDLE mode

WDIDLE

0 WDT continues to count in IDLE mode

1 WDT halts counting in IDLE mode

Dual Data Pointer Registers: To facilitate accessing both internal and external data memory, two banks of 16-bit Data Pointer Registers are provided: DP0 at SFR address locations 82H-83H and DP1 at 84H-85H. Bit DPS = 0 in SFR AUXR1 selects DP0 and DPS = 1 selects DP1. The user should always initialize the DPS bit to the appropriate value before accessing the respective Data Pointer Register.

Power Off Flag: The Power Off Flag (POF) is located at bit 4 (PCON.4) in the PCON SFR. POF is set to "1" during power up. It can be set and rest under software control and is not affected by reset.

Table 3. AUXR1: Auxiliary Register 1

AUXR1

Address = A2H

Reset Value = XXXXXXX0B

Not Bit Addressable

	–	–	–	–	–	–	–	DPS
Bit	7	6	5	4	3	2	1	0

– Reserved for future expansion

DPS Data Pointer Register Select

DPS	
0	Selects DPTR Registers DP0L, DP0H
1	Selects DPTR Registers DP1L, DP1H

mory ganization

MCS-51 devices have a separate address space for Program and Data Memory. Up to 64K bytes each of external Program and Data Memory can be addressed.

gram Memory

If the $\overline{EA}$ pin is connected to GND, all program fetches are directed to external memory.

On the AT89S51, if $\overline{EA}$ is connected to V_{CC}, program fetches to addresses 0000H through FFFH are directed to internal memory and fetches to addresses 1000H through FFFFH are directed to external memory.

ta Memory

The AT89S51 implements 128 bytes of on-chip RAM. The 128 bytes are accessible via direct and indirect addressing modes. Stack operations are examples of indirect addressing, so the 128 bytes of data RAM are available as stack space.

atchdog mer)ne-time nabled with eset-out)

The WDT is intended as a recovery method in situations where the CPU may be subjected to software upsets. The WDT consists of a 14-bit counter and the Watchdog Timer Reset (WDTRST) SFR. The WDT is defaulted to disable from exiting reset. To enable the WDT, a user must write 01EH and 0E1H in sequence to the WDTRST register (SFR location 0A6H). When the WDT is enabled, it will increment every machine cycle while the oscillator is running. The WDT timeout period is dependent on the external clock frequency. There is no way to disable the WDT except through reset (either hardware reset or WDT overflow reset). When WDT overflows, it will drive an output RESET HIGH pulse at the RST pin.

sing the WDT

To enable the WDT, a user must write 01EH and 0E1H in sequence to the WDTRST register (SFR location 0A6H). When the WDT is enabled, the user needs to service it by writing 01EH and 0E1H to WDTRST to avoid a WDT overflow. The 14-bit counter overflows when it reaches 16383 (3FFFH), and this will reset the device. When the WDT is enabled, it will increment every machine cycle while the oscillator is running. This means the user must reset the WDT at least every 16383 machine cycles. To reset the WDT the user must write 01EH and 0E1H to WDTRST. WDTRST is a write-only register. The WDT counter cannot be read or written. When WDT overflows, it will generate an output RESET pulse at the RST pin. The RESET pulse duration is 98xTOSC, where TOSC=1/FOSC. To make the best use of the WDT, it

should be serviced in those sections of code that will periodically be executed within the time required to prevent a WDT reset.

r During er-down Idle

In Power-down mode the oscillator stops, which means the WDT also stops. While in Power-down mode, the user does not need to service the WDT. There are two methods of exiting Power-down mode: by a hardware reset or via a level-activated external interrupt, which is enabled prior to entering Power-down mode. When Power-down is exited with hardware reset, servicing the WDT should occur as it normally does whenever the AT89S51 is reset. Exiting Power-down with an interrupt is significantly different. The interrupt is held low long enough for the oscillator to stabilize. When the interrupt is brought high, the interrupt is serviced. To prevent the WDT from resetting the device while the interrupt pin is held low, the WDT is not started until the interrupt is pulled high. It is suggested that the WDT be reset during the interrupt service for the interrupt used to exit Power-down mode.

To ensure that the WDT does not overflow within a few states of exiting Power-down, it is best to reset the WDT just before entering Power-down mode.

Before going into the IDLE mode, the WDIDLE bit in SFR AUXR is used to determine whether the WDT continues to count if enabled. The WDT keeps counting during IDLE (WDIDLE bit = 0) as the default state. To prevent the WDT from resetting the AT89S51 while in IDLE mode, the user should always set up a timer that will periodically exit IDLE, service the WDT, and reenter IDLE mode.

With WDIDLE bit enabled, the WDT will stop to count in IDLE mode and resumes the count upon exit from IDLE.

RT

The UART in the AT89S51 operates the same way as the UART in the AT89C51. For further information on the UART operation, refer to the ATMEL Web site (http://www.atmel.com). From the home page, select 'Products', then '8051-Architecture Flash Microcontroller', then 'Product Overview'.

ner 0 and 1

Timer 0 and Timer 1 in the AT89S51 operate the same way as Timer 0 and Timer 1 in the AT89C51. For further information on the timers' operation, refer to the ATMEL Web site (http://www.atmel.com). From the home page, select 'Products', then '8051-Architecture Flash Microcontroller', then 'Product Overview'.

terrupts

The AT89S51 has a total of five interrupt vectors: two external interrupts ($\overline{INT0}$ and $\overline{INT1}$), two timer interrupts (Timers 0 and 1), and the serial port interrupt. These interrupts are all shown in Figure 1.

Each of these interrupt sources can be individually enabled or disabled by setting or clearing a bit in Special Function Register IE. IE also contains a global disable bit, EA, which disables all interrupts at once.

Note that Table 4 shows that bit position IE.6 is unimplemented. In the AT89S51, bit position IE.5 is also unimplemented. User software should not write 1s to these bit positions, since they may be used in future AT89 products.

The Timer 0 and Timer 1 flags, TF0 and TF1, are set at S5P2 of the cycle in which the timers overflow. The values are then polled by the circuitry in the next cycle

Table 4. Interrupt Enable (IE) Register

(MSB)							(LSB)
EA	–	–	ES	ET1	EX1	ET0	EX0

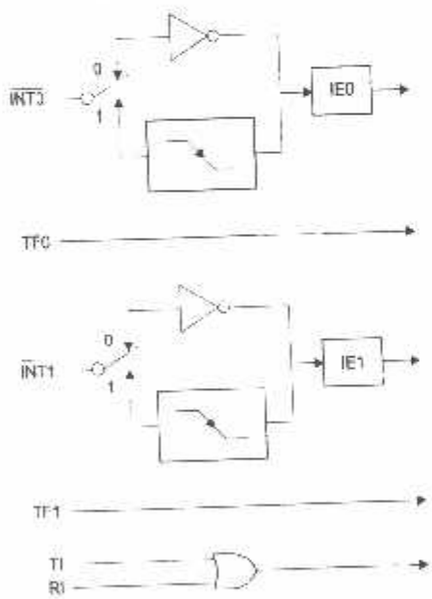
Enable Bit = 1 enables the interrupt.

Enable Bit = 0 disables the interrupt.

Symbol	Position	Function
EA	IE.7	Disables all interrupts. If EA = 0, no interrupt is acknowledged. If EA = 1, each interrupt source is individually enabled or disabled by setting or clearing its enable bit.
–	IE.6	Reserved
–	IE.5	Reserved
ES	IE.4	Serial Port interrupt enable bit
ET1	IE.3	Timer 1 interrupt enable bit
EX1	IE.2	External interrupt 1 enable bit
ET0	IE.1	Timer 0 interrupt enable bit
EX0	IE.0	External interrupt 0 enable bit

User software should never write 1s to reserved bits, because they may be used in future AT89 products.

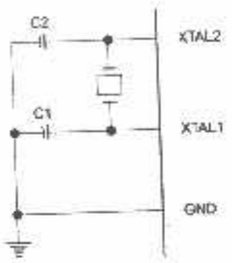
Figure 1. Interrupt Sources



illator racteristics

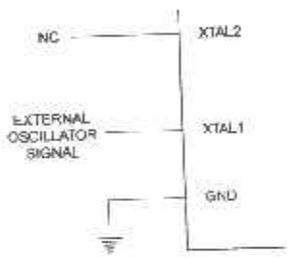
XTAL1 and XTAL2 are the input and output, respectively, of an inverting amplifier that can be configured for use as an on-chip oscillator, as shown in Figure 2. Either a quartz crystal or ceramic resonator may be used. To drive the device from an external clock source, XTAL2 should be left unconnected while XTAL1 is driven, as shown in Figure 3. There are no requirements on the duty cycle of the external clock signal, since the input to the internal clocking circuitry is through a divide-by-two flip-flop, but minimum and maximum voltage high and low time specifications must be observed.

Figure 2. Oscillator Connections



Note: C1, C2 = 30 pF ± 10 pF for Crystals = 40 pF ± 10 pF for Ceramic Resonators

Figure 3. External Clock Drive Configuration



e Mode

In idle mode, the CPU puts itself to sleep while all the on-chip peripherals remain active. The mode is invoked by software. The content of the on-chip RAM and all the special function registers remain unchanged during this mode. The idle mode can be terminated by any enabled interrupt or by a hardware reset.

Note that when idle mode is terminated by a hardware reset, the device normally resumes program execution from where it left off, up to two machine cycles before the internal reset algorithm takes control. On-chip hardware inhibits access to internal RAM in this event, but access to the port pins is not inhibited. To eliminate the possibility of an unexpected write to a port pin when idle mode is terminated by a reset, the instruction following the one that invokes idle mode should not write to a port pin or to external memory.

ower-down ode

In the Power-down mode, the oscillator is stopped, and the instruction that invokes Power-down is the last instruction executed. The on-chip RAM and Special Function Registers retain their values until the Power-down mode is terminated. Exit from Power-down mode can be initiated either by a hardware reset or by activation of an enabled external interrupt into $\overline{INT0}$ or $\overline{INT1}$. Reset redefines the SFRs but does not change the on-chip RAM. The reset should not be activated before V_{CC} is restored to its normal operating level and must be held active long enough to allow the oscillator to restart and stabilize.

Table 5. Status of External Pins During Idle and Power-down Modes

Mode	Program Memory	ALE	$\overline{PSEN}$	PORT0	PORT1	PORT2	PORT3
Idle	Internal	1	1	Data	Data	Data	Data
Idle	External	1	1	Float	Data	Address	Data
Power-down	Internal	0	0	Data	Data	Data	Data
Power-down	External	0	0	Float	Data	Data	Data

gram nory Lock

The AT89S51 has three lock bits that can be left unprogrammed (U) or can be programmed (P) to obtain the additional features listed in the following table.

Table 6. Lock Bit Protection Modes

Program Lock Bits				Protection Type
	LB1	LB2	LB3	
1	U	U	U	No program lock features
2	P	U	U	MOVC instructions executed from external program memory are disabled from fetching code bytes from internal memory, $\overline{EA}$ is sampled and latched on reset, and further programming of the Flash memory is disabled
3	P	P	U	Same as mode 2, but verify is also disabled
4	P	P	P	Same as mode 3, but external execution is also disabled

When lock bit 1 is programmed, the logic level at the $\overline{EA}$ pin is sampled and latched during reset. If the device is powered up without a reset, the latch initializes to a random value and holds that value until reset is activated. The latched value of $\overline{EA}$ must agree with the current logic level at that pin in order for the device to function properly.

ogramming : Flash – rallel Mode

The AT89S51 is shipped with the on-chip Flash memory array ready to be programmed. The programming interface needs a high-voltage (12-volt) program enable signal and is compatible with conventional third-party Flash or EPROM programmers.

The AT89S51 code memory array is programmed byte-by-byte.

Programming Algorithm: Before programming the AT89S51, the address, data, and control signals should be set up according to the Flash programming mode table and Figures 13 and 14. To program the AT89S51, take the following steps:

1. Input the desired memory location on the address lines.
2. Input the appropriate data byte on the data lines.
3. Activate the correct combination of control signals.
4. Raise $\overline{EA}/V_{PP}$ to 12V.
5. Pulse ALE/$\overline{PROG}$ once to program a byte in the Flash array or the lock bits. The byte-write cycle is self-timed and typically takes no more than 50 µs. Repeat steps 1 through 5, changing the address and data for the entire array or until the end of the object file is reached.

$\overline{Data}$ Polling: The AT89S51 features $\overline{Data}$ Polling to indicate the end of a byte write cycle. During a write cycle, an attempted read of the last byte written will result in the complement of the written data on P0.7. Once the write cycle has been completed, true data is valid on all outputs, and the next cycle may begin. $\overline{Data}$ Polling may begin any time after a write cycle has been initiated.

Ready/Busy: The progress of byte programming can also be monitored by the RDY/$\overline{BSY}$ output signal. P3.0 is pulled low after ALE goes high during programming to indicate $\overline{BUSY}$. P3.0 is pulled high again when programming is done to indicate READY.

Program Verify: If lock bits LB1 and LB2 have not been programmed, the programmed code data can be read back via the address and data lines for verification. The status of the individual lock bits can be verified directly by reading them back.

Reading the Signature Bytes: The signature bytes are read by the same procedure as a normal verification of locations 000H, 100H, and 200H, except that P3.6 and P3.7 must be pulled to a logic low. The values returned are as follows.

(000H) = 1EH indicates manufactured by Atmel
(100H) = 51H indicates 89S51
(200H) = 06H

Chip Erase: In the parallel programming mode, a chip erase operation is initiated by using the proper combination of control signals and by pulsing ALE/$\overline{PROG}$ low for a duration of 200 ns - 500 ns.

In the serial programming mode, a chip erase operation is initiated by issuing the Chip Erase instruction. In this mode, chip erase is self-timed and takes about 500 ms.

During chip erase, a serial read from any address location will return 00H at the data output.

ıgramming · Flash – ·ial Mode

The Code memory array can be programmed using the serial ISP interface while RST is pulled to V_{CC}. The serial interface consists of pins SCK, MOSI (input) and MISO (output). After RST is set high, the Programming Enable instruction needs to be executed first before other operations can be executed. Before a reprogramming sequence can occur, a Chip Erase operation is required.

The Chip Erase operation turns the content of every memory location in the Code array into FFH.

Either an external system clock can be supplied at pin XTAL1 or a crystal needs to be connected across pins XTAL1 and XTAL2. The maximum serial clock (SCK) frequency should be less than 1/16 of the crystal frequency. With a 33 MHz oscillator clock, the maximum SCK frequency is 2 MHz.

rial ɔgramming gorithm

To program and verify the AT89S51 in the serial programming mode, the following sequence is recommended:

1. Power-up sequence:
   Apply power between VCC and GND pins.
   Set RST pin to "H".
   If a crystal is not connected across pins XTAL1 and XTAL2, apply a 3 MHz to 33 MHz clock to XTAL1 pin and wait for at least 10 milliseconds.
2. Enable serial programming by sending the Programming Enable serial instruction to pin MOSI/P1.5. The frequency of the shift clock supplied at pin SCK/P1.7 needs to be less than the CPU clock at XTAL1 divided by 16.
3. The Code array is programmed one byte at a time in either the Byte or Page mode. The write cycle is self-timed and typically takes less than 0.5 ms at 5V.
4. Any memory location can be verified by using the Read instruction that returns the content at the selected address at serial output MISO/P1.6.
5. At the end of a programming session, RST can be set low to commence normal device operation.

Power-off sequence (if needed):

Set XTAL1 to "L" (if a crystal is not used).

Set RST to "L".

Turn V_{CC} power off.

Data Polling: The Data Polling feature is also available in the serial mode. In this mode, during a write cycle an attempted read of the last byte written will result in the complement of the MSB of the serial output byte on MISO.

al
gramming
ruction Set

The Instruction Set for Serial Programming follows a 4-byte protocol and is shown in Table 8 on page 18.

gramming
rface –
allel Mode

Every code byte in the Flash array can be programmed by using the appropriate combination of control signals. The write operation cycle is self-timed and once initiated, will automatically time itself to completion.

All major programming vendors offer worldwide support for the Atmel microcontroller series. Please contact your local programming vendor for the appropriate software revision.

e 7. Flash Programming Modes

le	V_{CC}	RST	PSEN	ALE/PROG	EA/V_{PP}	P2.6	P2.7	P3.3	P3.6	P3.7	P0.7-0 Data	P2.3-0 Address	P1.7-0 Address
e Code Data	5V	H	L	(2)	12V	L	H	H	H	H	D_{IN}	A11-8	A7-0
d Code Data	5V	H	L	H	H	L	L	L	H	H	D_{OUT}	A11-8	A7-0
le Lock Bit 1	5V	H	L	(3)	12V	H	H	H	H	H	X	X	X
te Lock Bit 2	5V	H	L	(3)	12V	H	H	H	L	L	X	X	X
te Lock Bit 3	5V	H	L	(3)	12V	H	L	H	H	L	X	X	X
ad Lock Bits 2, 3	5V	H	L	H	H	H	H	L	H	L	P0.2, P0.3, P0.4	X	X
hip Erase	5V	H	L	(1)	12V	H	L	H	L	L	X	X	X
ead Atmel ID	5V	H	L	H	H	L	L	L	L	L	1EH	0000	00H
ead Device ID	5V	H	L	H	H	L	L	L	L	L	51H	0001	00H
ead Device ID	5V	H	L	H	H	L	L	L	L	L	06H	0010	00H

tes:
1. Each PROG pulse is 200 ns - 500 ns for Chip Erase.
2. Each PROG pulse is 200 ns - 500 ns for Write Code Data.
3. Each PROG pulse is 200 ns - 500 ns for Write Lock Bits.
4. RDY/BSY signal is output on P3.0 during programming.
5. X = don't care.

Figure 4. Programming the Flash Memory (Parallel Mode)

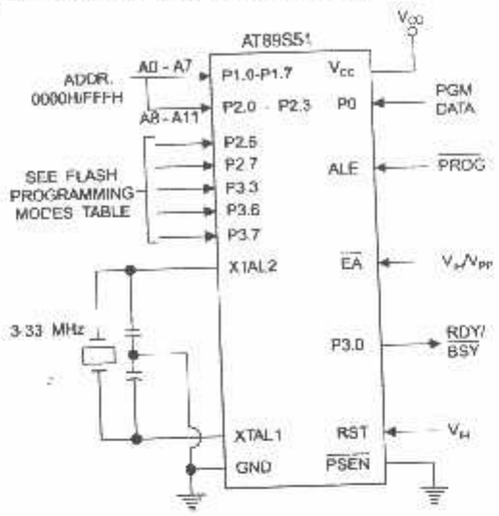
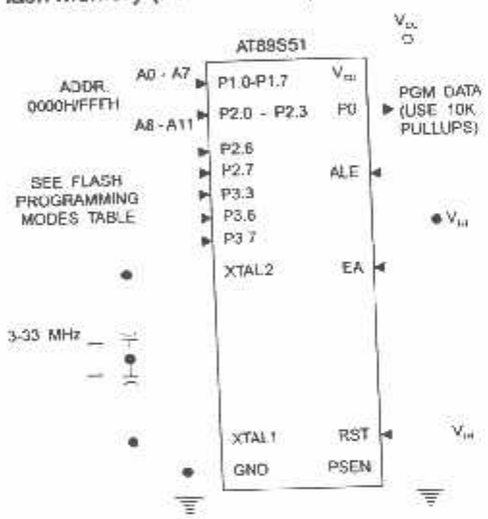


Figure 5. Verifying the Flash Memory (Parallel Mode)

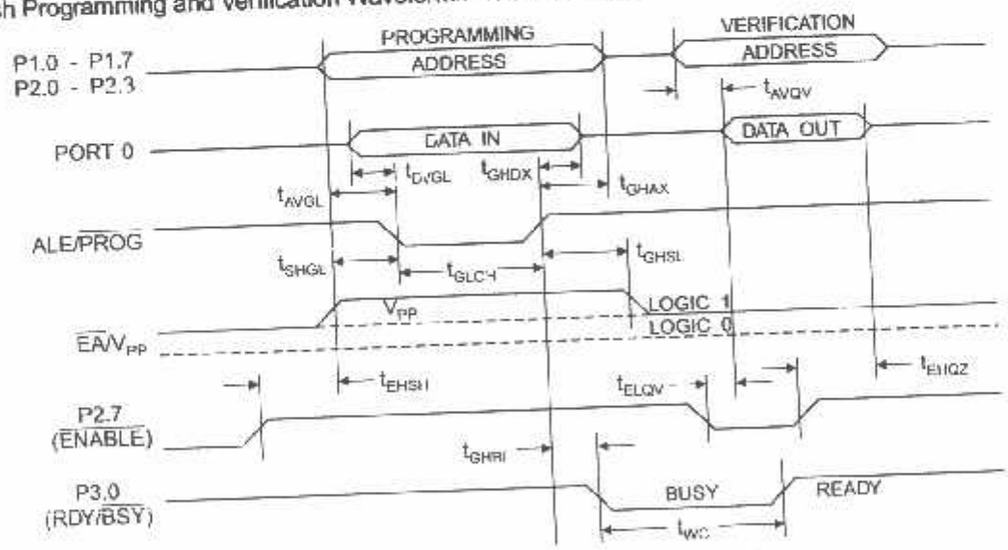


h Programming and Verification Characteristics (Parallel Mode)

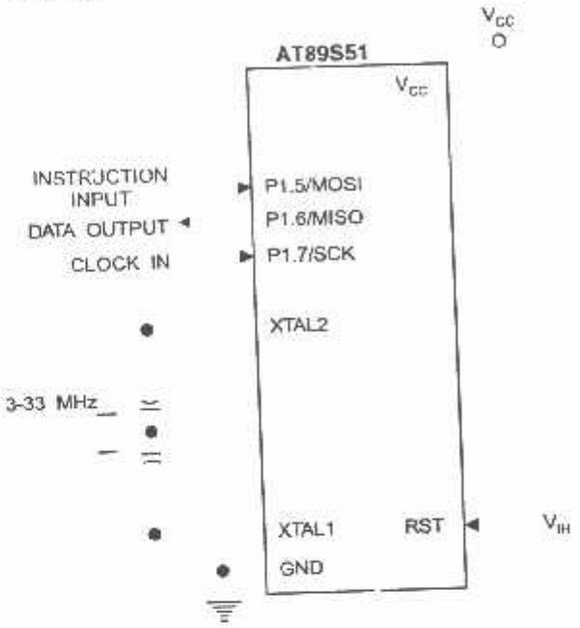
20°C to 30°C, V_{CC} = 4.5 to 5.5V

ol	Parameter	Min	Max	Units
	Programming Supply Voltage	11.5	12.5	V
	Programming Supply Current		10	mA
	V_{CC} Supply Current		30	mA
	Oscillator Frequency	3	33	MHz
CL	Address Setup to $\overline{PROG}$ Low	$48t_{CLCL}$		
	Address Hold After $\overline{PROG}$	$48t_{CLCL}$		
K	Data Setup to $\overline{PROG}$ Low	$48t_{CLCL}$		
	Data Hold After $\overline{PROG}$	$48t_{CLCL}$		
X	P2.7 ($\overline{ENABLE}$) High to V_{PP}	$48t_{CLCL}$		
H	V_{PP} Setup to $\overline{PROG}$ Low	10		µs
L	V_{PP} Hold After $\overline{PROG}$	10		µs
L	$\overline{PROG}$ Width	0.2	1	µs
H	Address to Data Valid		$48t_{CLCL}$	
V	$\overline{ENABLE}$ Low to Data Valid		$48t_{CLCL}$	
V	Data Float After $\overline{ENABLE}$	0	$48t_{CLCL}$	
IZ	$\overline{PROG}$ High to $\overline{BUSY}$ Low		1.0	µs
WL	Byte Write Cycle Time		50	µs

ıre 6. Flash Programming and Verification Waveforms – Parallel Mode

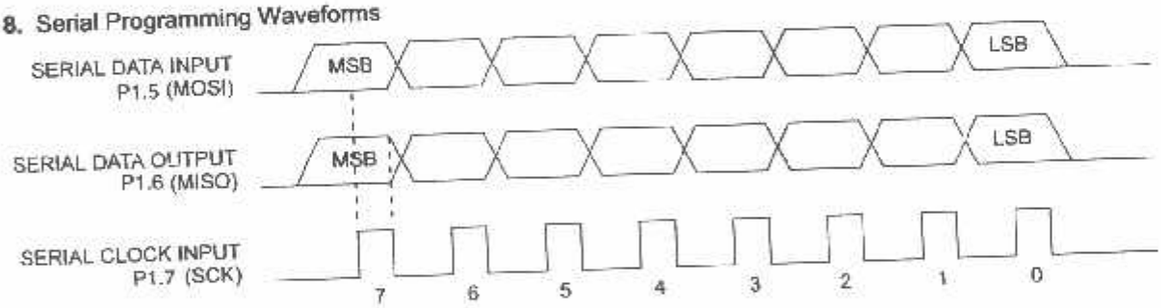


e 7. Flash Memory Serial Downloading



sh Programming and Verification Waveforms – Serial Mode

re 8. Serial Programming Waveforms



8. Serial Programming Instruction Set

uction	Instruction Format Byte 1	Byte 2	Byte 3	Byte 4	Operation
ramming Enable	1010 1100	0101 0011	xxxx xxxx	xxxx xxxx 0110 1001 (Output)	Enable Serial Programming while RST is high
Erase	1010 1100	100x xxxx	xxxx xxxx	xxxx xxxx	Chip Erase Flash memory array
l Program Memory e Mode)	0010 0000	xxxx A11 A10 A9 A8	A7 A6 A5 A4 A3 A2 A1 A0	D7 D6 D5 D4 D3 D2 D1 D0	Read data from Program memory in the byte mode
e Program Memory e Mode)	0100 0000	xxxx A11 A10 A9 A8	A7 A6 A5 A4 A3 A2 A1 A0	D7 D6 D5 D4 D3 D2 D1 D0	Write data to Program memory in the byte mode
e Lock Bits[2]	1010 1100	1110 00 B1 B2	xxxx xxxx	xxxx xxxx	Write Lock bits. See Note (2).
d Lock Bits	0010 0100	xxxx xxxx	xxxx xxxx	xx LB3 LB2 LB1 xx	Read back current status of the lock bits (a programmed lock bit reads back as a "1")
d Signature Bytes[1]	0010 1000	xxx A5 A4 A3 A2 A1	A0 xxx xxxx	Signature Byte	Read Signature Byte
d Program Memory ge Mode)	0011 0000	xxxx A11 A10 A9 A8	Byte 0	Byte 1... Byte 255	Read data from Program memory in the Page Mode (256 bytes)
e Program Memory ge Mode)	0101 0000	xxxx A11 A10 A9 A8	Byte 0	Byte 1... Byte 255	Write data to Program memory in the Page Mode (256 bytes)

s: 1. The signature bytes are not readable in Lock Bit Modes 3 and 4.
2. B1 = 0, B2 = 0 → Mode 1, no lock protection
B1 = 0, B2 = 1 → Mode 2, lock bit 1 activated
B1 = 1, B2 = 0 → Mode 3, lock bit 2 activated
B1 = 1, B1 = 1 → Mode 4, lock bit 3 activated

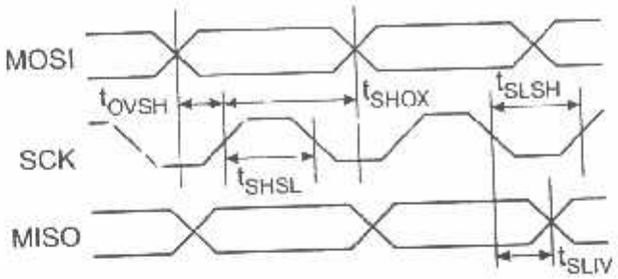
} Each of the lock bits needs to be activated sequentially before Mode 4 can be executed.

After Reset signal is high, SCK should be low for at least 64 system clocks before it goes high to clock in the enable data bytes. No pulsing of Reset signal is necessary. SCK should be no faster than 1/16 of the system clock at XTAL1.

For Page Read/Write, the data always starts from byte 0 to 255. After the command byte and upper address byte are latched, each byte thereafter is treated as data until all 256 bytes are shifted in/out. Then the next instruction will be ready to be decoded.

·ial Programming Characteristics

ıre 9. Serial Programming Timing



ole 9. Serial Programming Characteristics, T_A = -40° C to 85° C, V_{CC} = 4.0 - 5.5V (Unless Otherwise Noted)

ymbol	Parameter	Min	Typ	Max	Units
t_{CLCL}	Oscillator Frequency	0		33	MHz
LCL	Oscillator Period	30			ns
HSL	SCK Pulse Width High	8 t_{CLCL}			ns
LSH	SCK Pulse Width Low	8 t_{CLCL}			ns
OVSH	MOSI Setup to SCK High	t_{CLCL}			ns
SHOX	MOSI Hold after SCK High	2 t_{CLCL}			ns
SLIV	SCK Low to MISO Valid	10	16	32	ns
ERASE	Chip Erase Instruction Cycle Time			500	ms
SWC	Serial Byte Write Cycle Time			64 t_{CLCL} + 400	µs

olute Maximum Ratings*

ating Temperature	-55°C to +125°C
ge Temperature	-65°C to +150°C
ge on Any Pin Respect to Ground	-1.0V to +7.0V
mum Operating Voltage	6.6V
Output Current	15.0 mA

*NOTICE: Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Characteristics

alues shown in this table are valid for T_A = -40°C to 85°C and V_{CC} = 4.0V to 5.5V, unless otherwise noted.

bol	Parameter	Condition	Min	Max	Units
	Input Low Voltage	(Except $\overline{EA}$)	-0.5	0.2 V_{CC}-0.1	V
	Input Low Voltage ($\overline{EA}$)		-0.5	0.2 V_{CC}-0.3	V
	Input High Voltage	(Except XTAL1, RST)	0.2 V_{CC}+0.9	V_{CC}+0.5	V
	Input High Voltage	(XTAL1, RST)	0.7 V_{CC}	V_{CC}+0.5	V
	Output Low Voltage[1] (Ports 1,2,3)	I_{OL} = 1.6 mA		0.45	V
	Output Low Voltage[1] (Port 0, ALE, $\overline{PSEN}$)	I_{OL} = 3.2 mA		0.45	V
	Output High Voltage (Ports 1,2,3, ALE, $\overline{PSEN}$)	I_{OH} = -60 µA, V_{CC} = 5V ±10%	2.4		V
		I_{OH} = -25 µA	0.75 V_{CC}		V
		I_{OH} = -10 µA	0.9 V_{CC}		V
	Output High Voltage (Port 0 in External Bus Mode)	I_{OH} = -800 µA, V_{CC} = 5V ±10%	2.4		V
		I_{OH} = -300 µA	0.75 V_{CC}		V
		I_{OH} = -80 µA	0.9 V_{CC}		V
	Logical 0 Input Current (Ports 1,2,3)	V_{IN} = 0.45V		-50	µA
	Logical 1 to 0 Transition Current (Ports 1,2,3)	V_{IN} = 2V, V_{CC} = 5V ±10%		-650	µA
	Input Leakage Current (Port 0, $\overline{EA}$)	0.45 < V_{IN} < V_{CC}		±10	µA
RST	Reset Pulldown Resistor		50	300	KΩ
	Pin Capacitance	Test Freq. = 1 MHz, T_A = 25°C		10	pF
	Power Supply Current	Active Mode, 12 MHz		25	mA
		Idle Mode, 12 MHz		6.5	mA
	Power-down Mode[2]	V_{CC} = 5.5V		50	µA

tes: 1. Under steady state (non-transient) conditions, I_{OL} must be externally limited as follows:
Maximum I_{OL} per port pin: 10 mA
Maximum I_{OL} per 8-bit port:
Port 0: 26 mA Ports 1, 2, 3: 15 mA
Maximum total I_{OL} for all output pins: 71 mA
If I_{OL} exceeds the test condition, V_{OL} may exceed the related specification. Pins are not guaranteed to sink current greater than the listed test conditions.
2. Minimum V_{CC} for Power-down is 2V.

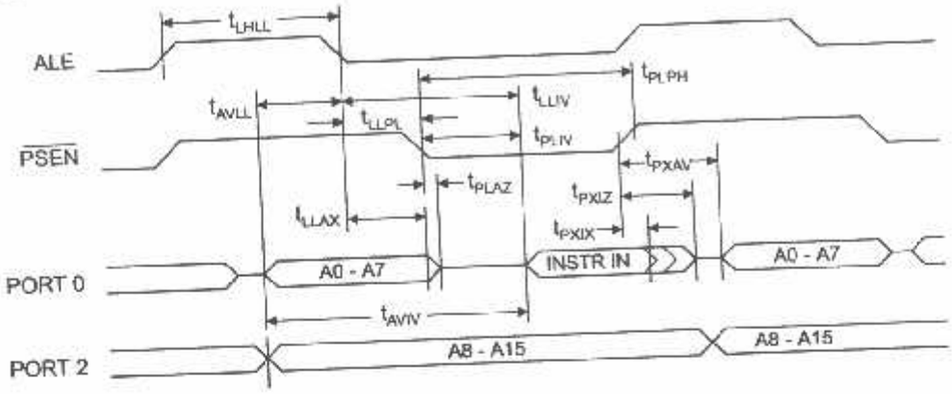
Characteristics

· operating conditions, load capacitance for Port 0, ALE/$\overline{PROG}$, and $\overline{PSEN}$ = 100 pF; load capacitance for all other ts = 80 pF.

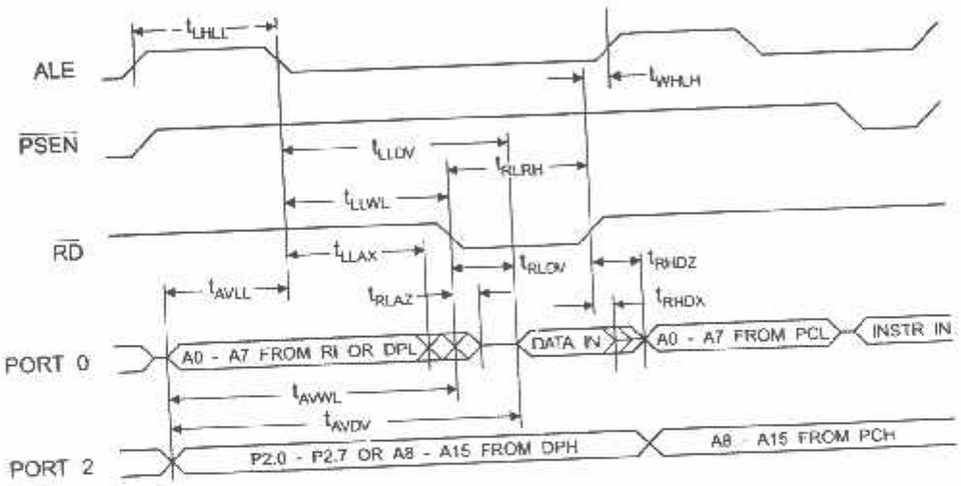
ernal Program and Data Memory Characteristics

bol	Parameter	12 MHz Oscillator		Variable Oscillator		Units
		Min	Max	Min	Max	
CL	Oscillator Frequency			0	33	MHz
	ALE Pulse Width	127		$2t_{CLCL}$-40		ns
	Address Valid to ALE Low	43		t_{CLCL}-25		ns
	Address Hold After ALE Low	48		t_{CLCL}-25		ns
	ALE Low to Valid Instruction In		233		$4t_{CLCL}$-65	ns
	ALE Low to $\overline{PSEN}$ Low	43		t_{CLCL}-25		ns
	$\overline{PSEN}$ Pulse Width	205		$3t_{CLCL}$-45		ns
	$\overline{PSEN}$ Low to Valid Instruction In		145		$3t_{CLCL}$-60	ns
	Input Instruction Hold After $\overline{PSEN}$	0		0		ns
	Input Instruction Float After $\overline{PSEN}$		59		t_{CLCL}-25	ns
	$\overline{PSEN}$ to Address Valid	75		t_{CLCL}-8		ns
	Address to Valid Instruction In		312		$5t_{CLCL}$-80	ns
	$\overline{PSEN}$ Low to Address Float		10		10	ns
H	$\overline{RD}$ Pulse Width	400		$6t_{CLCL}$-100		ns
WH	$\overline{WR}$ Pulse Width	400		$6t_{CLCL}$-100		ns
W	$\overline{RD}$ Low to Valid Data In		252		$5t_{CLCL}$-90	ns
DX	Data Hold After $\overline{RD}$	0		0		ns
DZ	Data Float After $\overline{RD}$		97		$2t_{CLCL}$-28	ns
W	ALE Low to Valid Data In		517		$8t_{CLCL}$-150	ns
DV	Address to Valid Data In		585		$9t_{CLCL}$-165	ns
WL	ALE Low to $\overline{RD}$ or $\overline{WR}$ Low	200	300	$3t_{CLCL}$-50	$3t_{CLCL}$+50	ns
AWL	Address to $\overline{RD}$ or $\overline{WR}$ Low	203		$4t_{CLCL}$-75		ns
QWX	Data Valid to $\overline{WR}$ Transition	23		t_{CLCL}-30		ns
QWH	Data Valid to $\overline{WR}$ High	433		$7t_{CLCL}$-130		ns
WHQX	Data Hold After $\overline{WR}$	33		t_{CLCL}-25		ns
LAZ	$\overline{RD}$ Low to Address Float		0		0	ns
WLH	$\overline{RD}$ or $\overline{WR}$ High to ALE High	43	123	t_{CLCL}-25	t_{CLCL}+25	ns

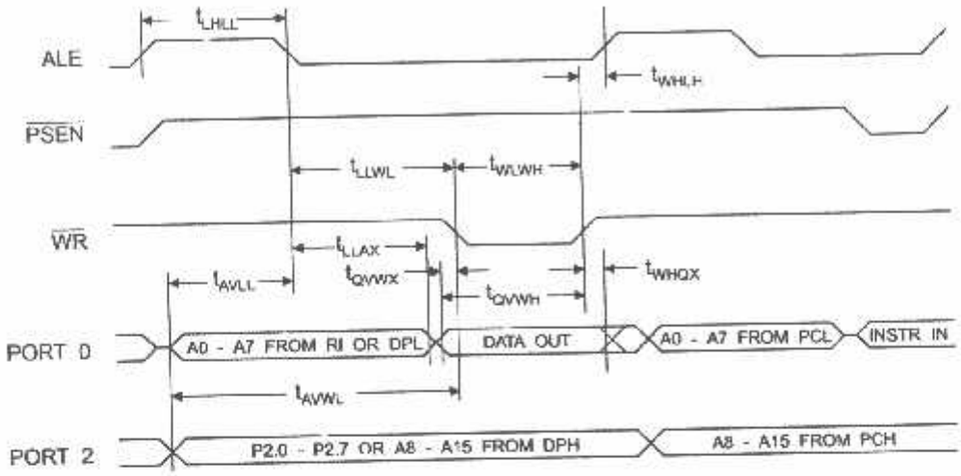
rnal Program Memory Read Cycle



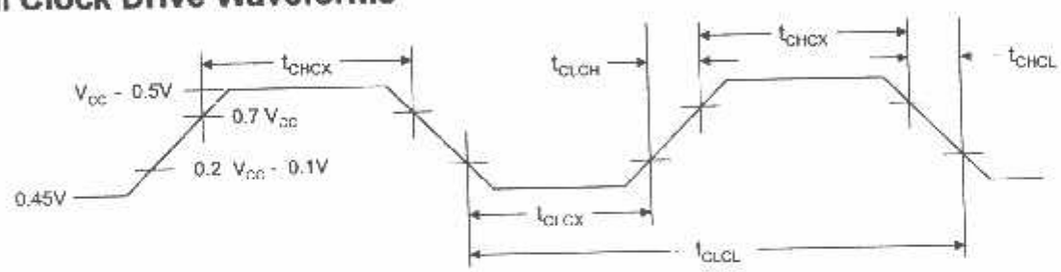
ernal Data Memory Read Cycle



ernal Data Memory Write Cycle



ernal Clock Drive Waveforms



ternal Clock Drive

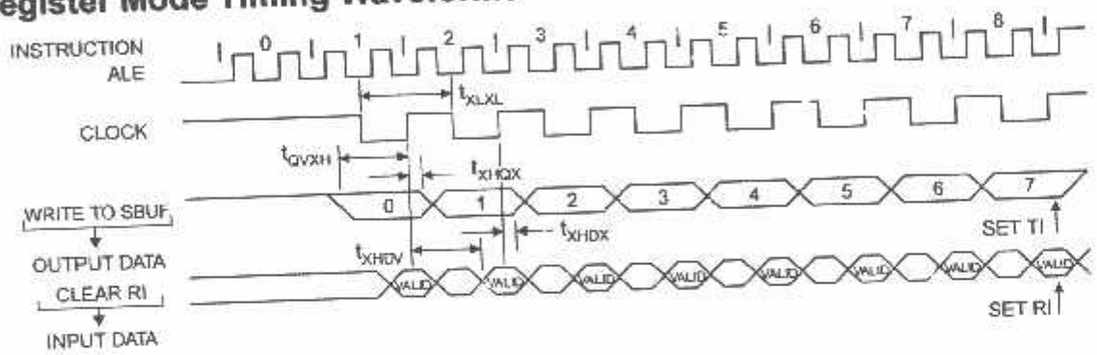
mbol	Parameter	Min	Max	Units
CLCL	Oscillator Frequency	0	33	MHz
CL	Clock Period	30		ns
HCX	High Time	12		ns
LCX	Low Time	12		ns
LCH	Rise Time		5	ns
HCL	Fall Time		5	ns

al Port Timing: Shift Register Mode Test Conditions

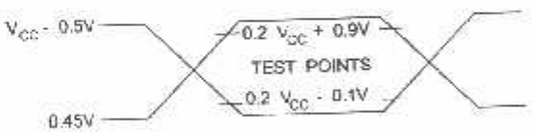
alues in this table are valid for V_{CC} = 4.0V to 5.5V and Load Capacitance = 80 pF.

bol	Parameter	12 MHz Osc		Variable Oscillator		Units
		Min	Max	Min	Max	
	Serial Port Clock Cycle Time	1.0		$12t_{CLCL}$		µs
	Output Data Setup to Clock Rising Edge	700		$10t_{CLCL}$-133		ns
	Output Data Hold After Clock Rising Edge	50		$2t_{CLCL}$-80		ns
	Input Data Hold After Clock Rising Edge	0		0		ns
	Clock Rising Edge to Input Data Valid		700		$10t_{CLCL}$-133	ns

it Register Mode Timing Waveforms

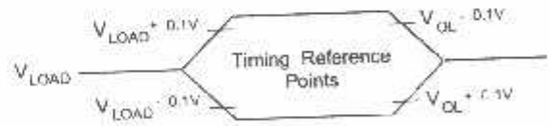


Testing Input/Output Waveforms[1]



: 1. AC Inputs during testing are driven at V_{CC} - 0.5V for a logic 1 and 0.45V for a logic 0. Timing measurements are made at V_{IH} min. for a logic 1 and V_{IL} max. for a logic 0.

oat Waveforms[1]



te: 1. For timing purposes, a port pin is no longer floating when a 100 mV change from load voltage occurs. A port pin begins to float when a 100 mV change from the loaded V_{OH}/V_{OL} level occurs.

ering Information

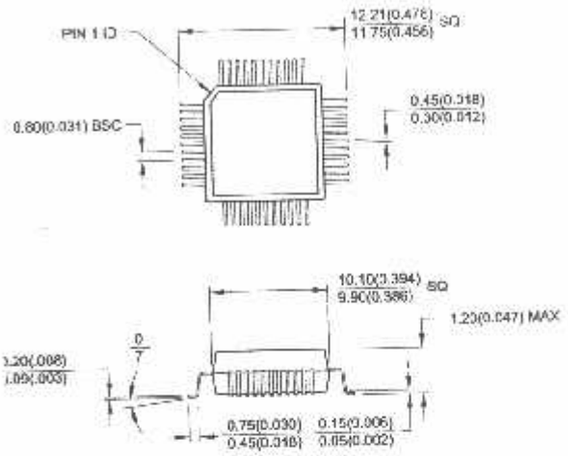
eed Hz)	Power Supply	Ordering Code	Package	Operation Range
24	4.0V to 5.5V	AT89S51-24AC AT89S51-24JC AT89S51-24PC	44A 44J 40P6	Commercial (0° C to 70° C)
		AT89S51-24AI AT89S51-24JI AT89S51-24PI	44A 44J 40P6	Industrial (-40° C to 85° C)
33	4.5V to 5.5V	AT89S51-33AC AT89S51-33JC AT89S51-33PC	44A 44J 40P6	Commercial (0° C to 70° C)

= Preliminary Availability

	Package Type
4A	44-lead, Thin Plastic Gull Wing Quad Flatpack (TQFP)
4J	44-lead, Plastic J-leaded Chip Carrier (PLCC)
0P6	40-pin, 0.600" Wide, Plastic Dual Inline Package (PDIP)

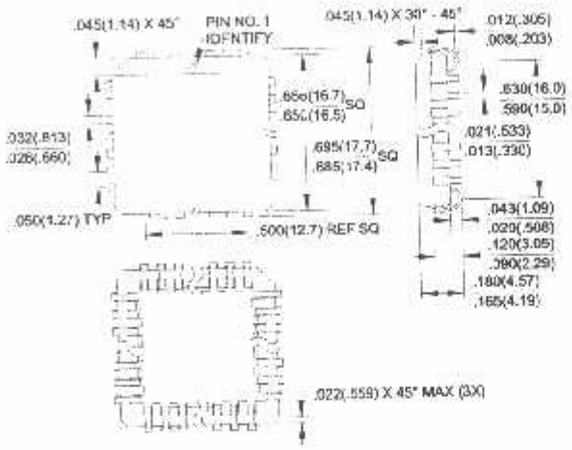
kaging Information

4A, 44-lead, Thin (1.0 mm) Plastic Gull Wing Quad
lat Package (TQFP)
imensions in Millimeters and (Inches)*

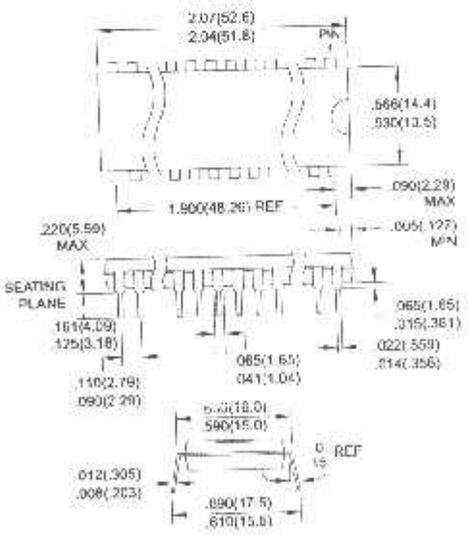


*Controlling dimension: millimeters

44J, 44-lead, Plastic J-leaded Chip Carrier (PLCC)
Dimensions in Inches and (Millimeters)



40P6, 40-pin, 0.600" Wide, Plastic Dual Inline
Package (PDIP)
Dimensions in Inches and (Millimeters)
JEDEC STANDARD MS-011 AC



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2487A–10/01/xM

February 2003

National Semiconductor

LM567/LM567C
Tone Decoder

General Description

The LM567 and LM567C are general purpose tone decoders designed to provide a saturated transistor switch to ground when an input signal is present within the passband. The circuit consists of an I and Q detector driven by a voltage controlled oscillator which determines the center frequency of the decoder. External components are used to independently set center frequency, bandwidth and output delay.

Features

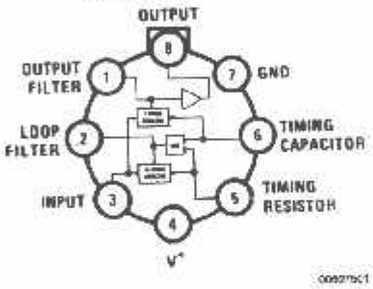
- 20 to 1 frequency range with an external resistor
- Logic compatible output with 100 mA current sinking capability
- Bandwidth adjustable from 0 to 14%
- High rejection of out of band signals and noise
- Immunity to false signals
- Highly stable center frequency
- Center frequency adjustable from 0.01 Hz to 500 kHz

Applications

- Touch tone decoding
- Precision oscillator
- Frequency monitoring and control
- Wide band FSK demodulation
- Ultrasonic controls
- Carrier current remote controls
- Communications paging decoders

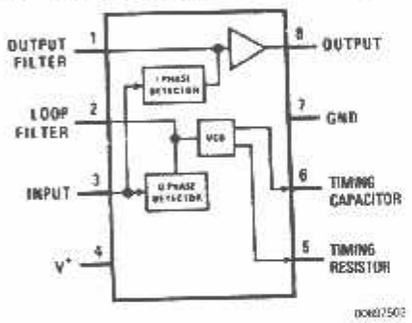
Connection Diagrams

Metal Can Package



Top View
Order Number LM567H or LM567CH
See NS Package Number H08C

Dual-In-Line and Small Outline Packages



Top View
Order Number LM567CM
See NS Package Number M08A
Order Number LM567CN
See NS Package Number N08E

 DS006975

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Supply Voltage Pin	9V
Power Dissipation (Note 2)	1100 mW
V_{in}	15V
V_3	−10V
V_5	V_4 + 0.5V
Storage Temperature Range	−65°C to +150°C
Operating Temperature Range	
LM567H	−55°C to +125°C
LM567CH, LM567CM, LM567CN	0°C to +70°C
Soldering Information	
Dual-In-Line Package	
Soldering (10 sec.)	260°C
Small Outline Package	
Vapor Phase (60 sec.)	215°C
Infrared (15 sec.)	220°C

See AN-450 "Surface Mounting Methods and Their Effect on Product Reliability" for other methods of soldering surface mount devices.

Electrical Characteristics

AC Test Circuit, T_A = 25°C, V^+ = 5V

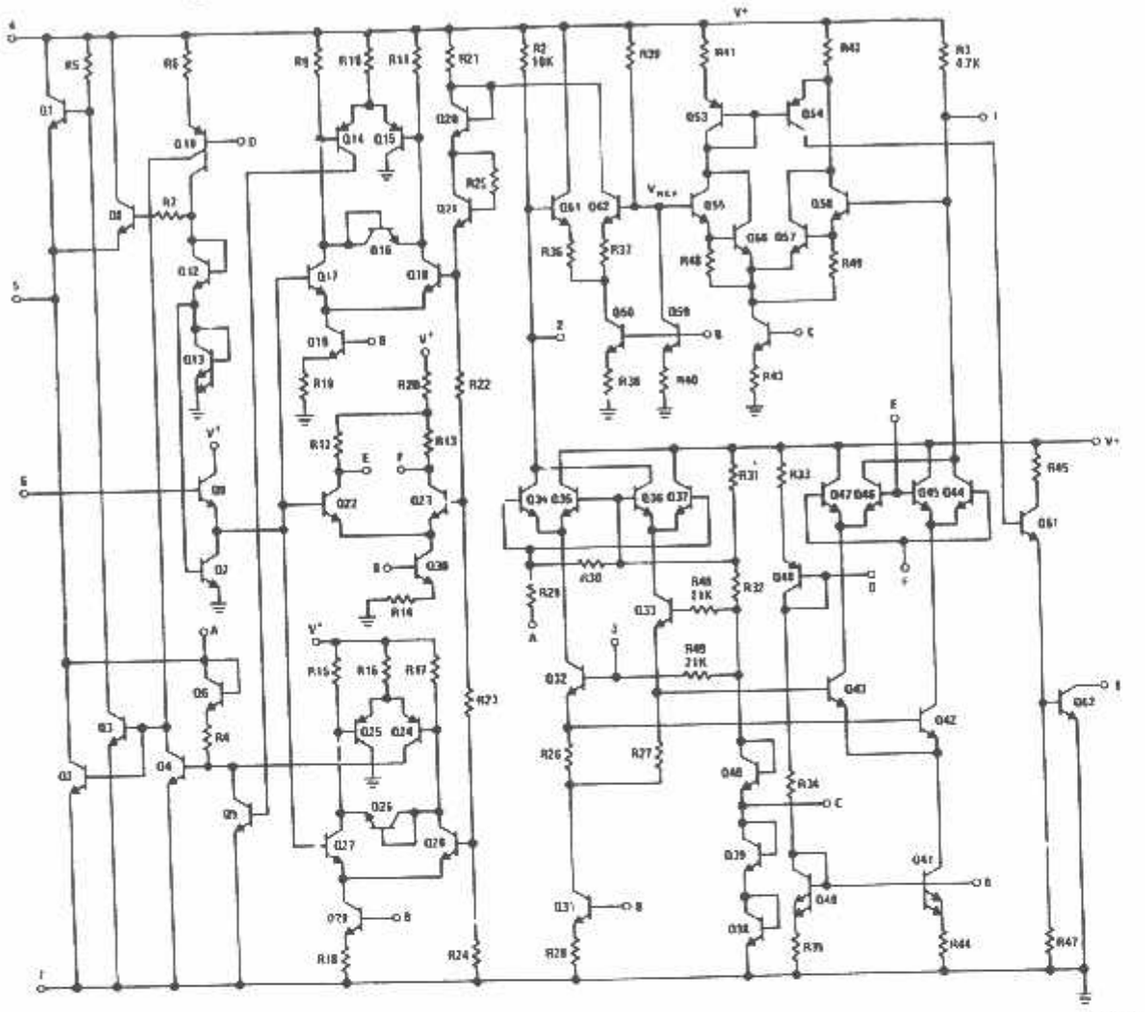
Parameters	Conditions	LM567			LM567C/LM567CM			Units
		Min	Typ	Max	Min	Typ	Max	
Power Supply Voltage Range		4.75	5.0	9.0	4.75	5.0	9.0	V
Power Supply Current Quiescent	R_L = 20k		6	8		7	10	mA
Power Supply Current Activated	R_L = 20k		11	13		12	15	mA
Input Resistance		18	20		15	20		kΩ
Smallest Detectable Input Voltage	I_L = 100 mA, $f_i = f_o$		20	25		20	25	mVrms
Largest No Output Input Voltage	I_C = 100 mA, $f_i = f_o$	10	15		10	15		mVrms
Largest Simultaneous Outband Signal to Inband Signal Ratio			6			6		dB
Minimum Input Signal to Wideband Noise Ratio	B_n = 140 kHz		−6			−6		dB
Largest Detection Bandwidth		12	14	16	10	14	18	% of f_o
Largest Detection Bandwidth Skew			1	2		2	3	% of f_o
Largest Detection Bandwidth Variation with Temperature			±0.1			±0.1		%/°C
Largest Detection Bandwidth Variation with Supply Voltage	4.75–6.75V		±1	±2		±1	±5	%V
Highest Center Frequency		100	500		100	500		kHz
Center Frequency Stability (4.75–5.75V)	0 < T_A < 70 −55 < T_A < +125		35 ± 60 35 ± 140			35 ± 60 35 ± 140		ppm/°C ppm/°C
Center Frequency Shift with Supply Voltage	4.75V–6.75V 4.75V–9V		0.5	1.0 2.0		0.4	2.0 2.0	%/V %/V
Fastest ON-OFF Cycling Rate			f_o/20			f_o/20		
Output Leakage Current	V_8 = 15V		0.01	25		0.01	25	µA
Output Saturation Voltage	e_i = 25 mV, I_8 = 30 mA e_i = 25 mV, I_8 = 100 mA		0.2 0.6	0.4 1.0		0.2 0.6	0.4 1.0	V
Output Fall Time			30			30		ns
Output Rise Time			150			150		ns

Note 1: Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is functional, but do not guarantee specific performance limits. Electrical Characteristics state DC and AC electrical specifications under particular test conditions which guarantee specific performance limits. This assumes that the device is within the Operating Ratings. Specifications are not guaranteed for parameters where no limit is given, however, the typical value is a good indication of device performance.

Note 2: The maximum junction temperature of the LM567 and LM567C is 150°C. For operating at elevated temperatures, devices in the TO-5 package must be derated based on a thermal resistance of 150°C/W, junction to ambient or 45°C/W, junction to case. For the DIP the device must be derated based on a thermal resistance of 110°C/W, junction to ambient. For the Small Outline package, the device must be derated based on a thermal resistance of 160°C/W, junction to ambient.

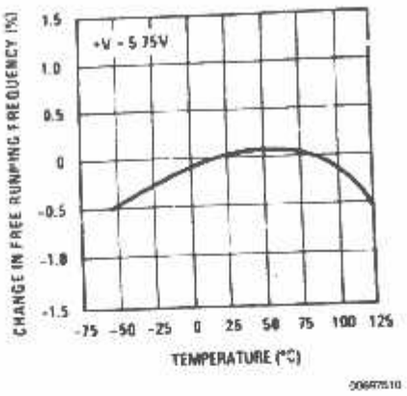
Note 3: Refer to RETS567X drawing for specifications of military LM567H version.

:hematic Diagram

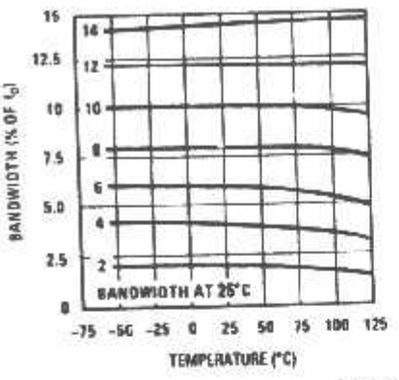


Typical Performance Characteristics

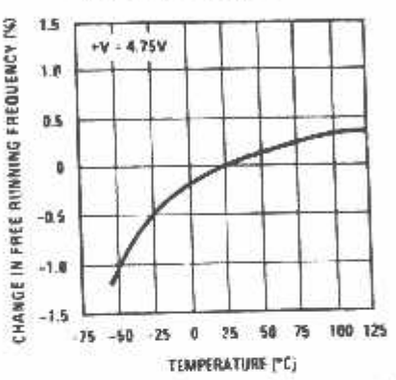
Typical Frequency Drift



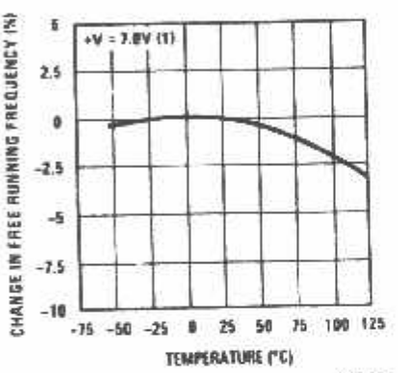
Typical Bandwidth Variation



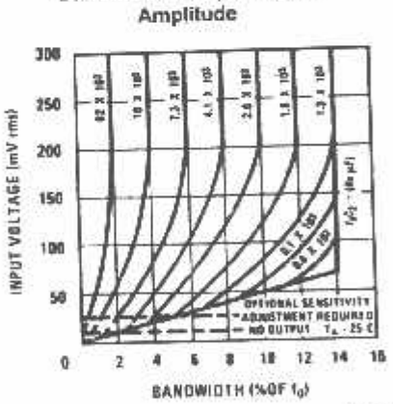
Typical Frequency Drift



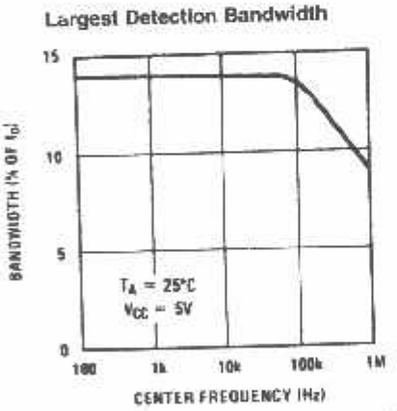
Typical Frequency Drift



Bandwidth vs Input Signal Amplitude

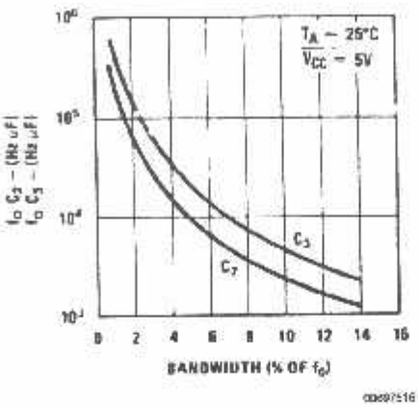


Largest Detection Bandwidth



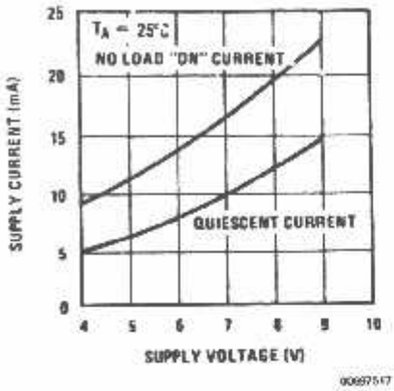
ypical Performance Characteristics (Continued)

Detection Bandwidth as a Function of C_2 and C_3



00697516

Typical Supply Current vs Supply Voltage



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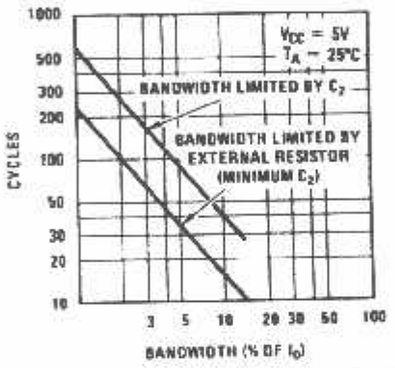
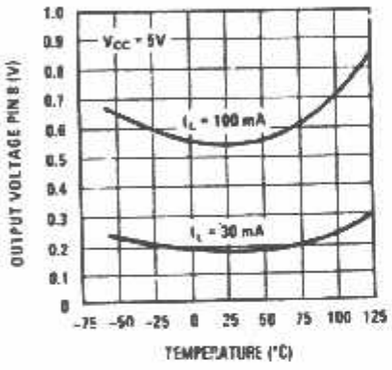
Greatest Number of Cycles Before Output



00697518

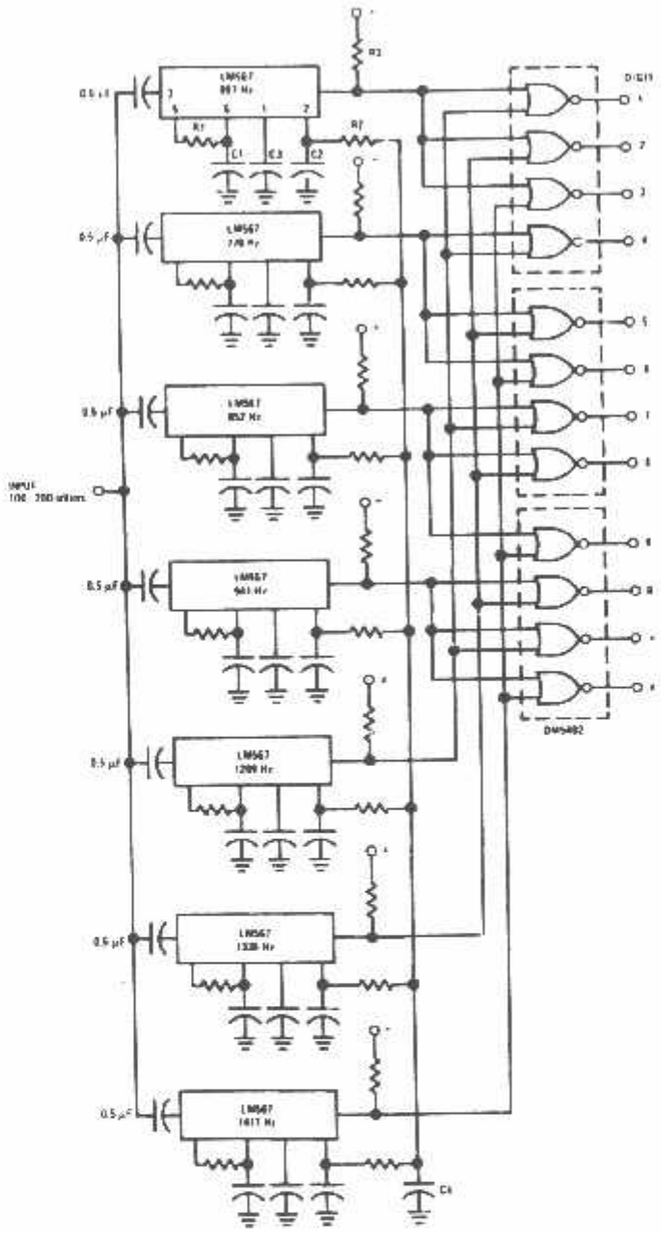
Typical Output Voltage vs Temperature



00697519

Typical Applications

Touch-Tone Decoder



00807506

Component values (typ)

R1 6.8 to 15k

R2 4.7k

R3 20k

C1 0.10 mfd

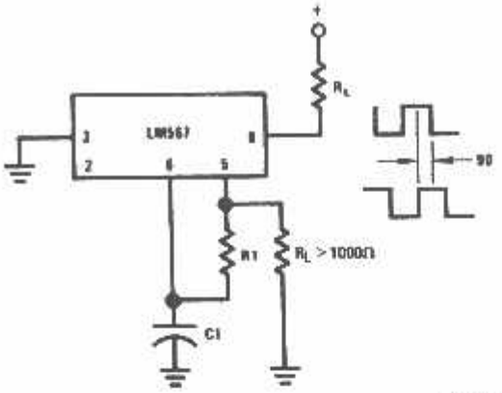
C2 1.0 mfd 6V

C3 2.2 mfd 6V

C4 250 mfd 6V

ypical Applications (Continued)

Oscillator with Quadrature Output



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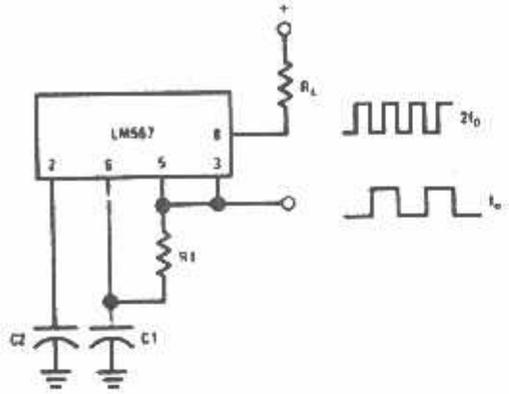
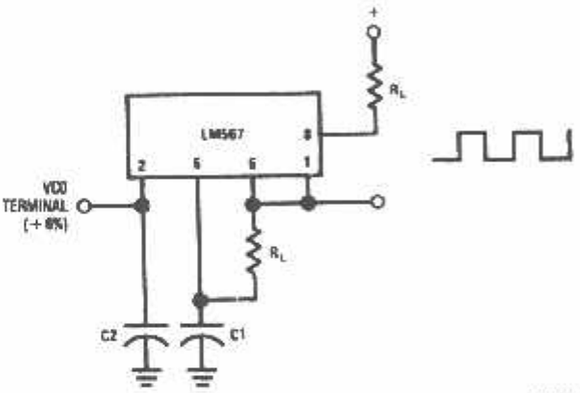
nnect Pin 3 to 2.8V to Invert Output

Oscillator with Double Frequency Output



00697507

Precision Oscillator Drive 100 mA Loads



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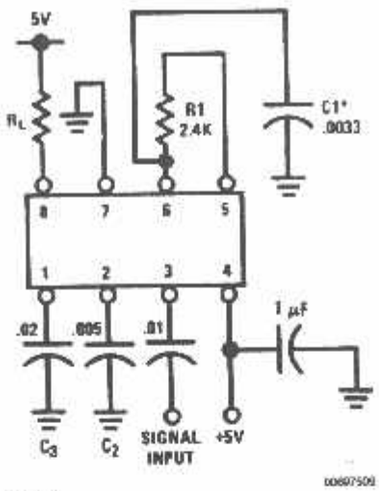
AC Test Circuit



00697509

f_i = 100 kHz + 5V

*Note: Adjust for f_o = 100 kHz.

Applications Information

The center frequency of the tone decoder is equal to the free running frequency of the VCO. This is given by

$$f_o \cong \frac{1}{1.1\ R_1 C_1}$$

The bandwidth of the filter may be found from the approximation

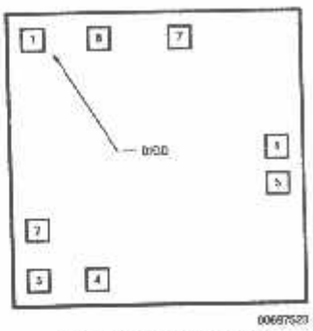
$$BW = 1070 \sqrt{\frac{V_i}{f_o C_2}} \text{ in \% of } f_o$$

Where:

V_i = Input voltage (volts rms). $V_i \leq 200mV$

C_2 = Capacitance at Pin 2(µF)

M567C MDC MWC
ONE DECODER



Die Layout (C - Step)

IE/WAFER CHARACTERISTICS

Fabrication Attributes		General Die Information	
hysical Die Identification	LM567C	Bond Pad Opening Size (min)	91µm x 91µm
ie Step	C	Bond Pad Metalization	0.5% COPPER_BAL. ALUMINUM
Physical Attributes		Passivation	VOM NITRIDE
Vafer Diameter	150mm	Back Side Metal	BARE BACK
ise Size (Drawn)	1600µm x 1626µm 63.0mils x 64.0mils	Back Side Connection	Floating
hickness	406µm Nominal		
Min Pitch	198µm Nominal		

Special Assembly Requirements:

Note: Actual die size is rounded to the nearest micron.

Die Bond Pad Coordinate Locations (C - Step)

(Referenced to die center, coordinates in µm) NC = No Connection, N.U. = Not Used

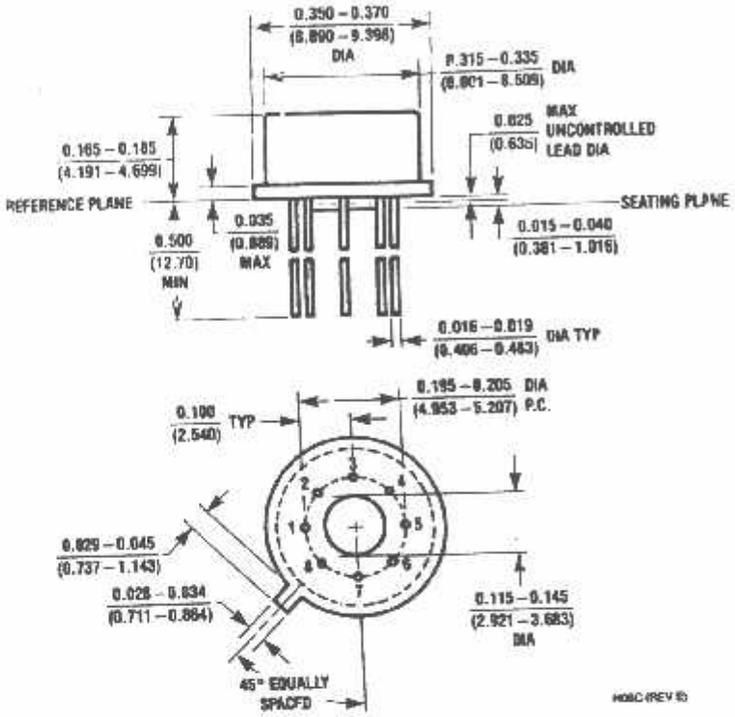
SIGNAL NAME	PAD# NUMBER	X/Y COORDINATES		PAD SIZE		
		X	Y	X		Y
OUTPUT FILTER	1	-673	686	91	x	91
LOOP FILTER	2	-673	-419	91	x	91
INPUT	3	-673	-686	91	x	91
V+	4	-356	-686	91	x	91
TIMING RES	5	673	-122	91	x	91
TIMING CAP	6	673	76	91	x	91
GND	7	178	686	117	x	91
OUTPUT	8	-318	679	117	x	104

LM567C MDC MWC TONE DECODER (Continued)

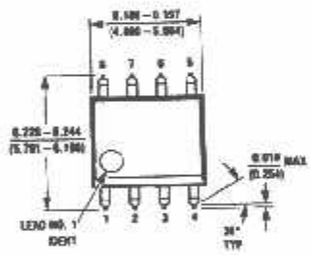
IN U.S.A	
Tel #:	1 877 Dial Die 1 877 342 5343
Fax:	1 207 541 8140
IN EUROPE	
Tel:	49 (0) 8141 351492 / 1495
Fax:	49 (0) 8141 351470
IN ASIA PACIFIC	
Tel:	(852) 27371701
IN JAPAN	
Tel:	81 043 299 2308

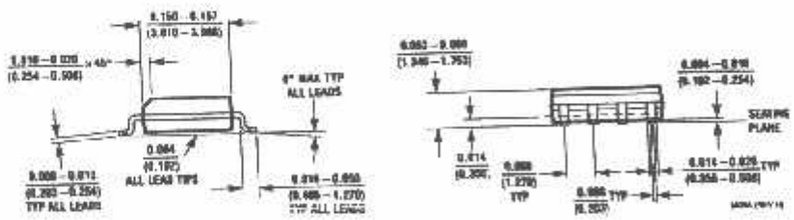
ıysical Dimensions inches (millimeters)

ɔss otherwise noted



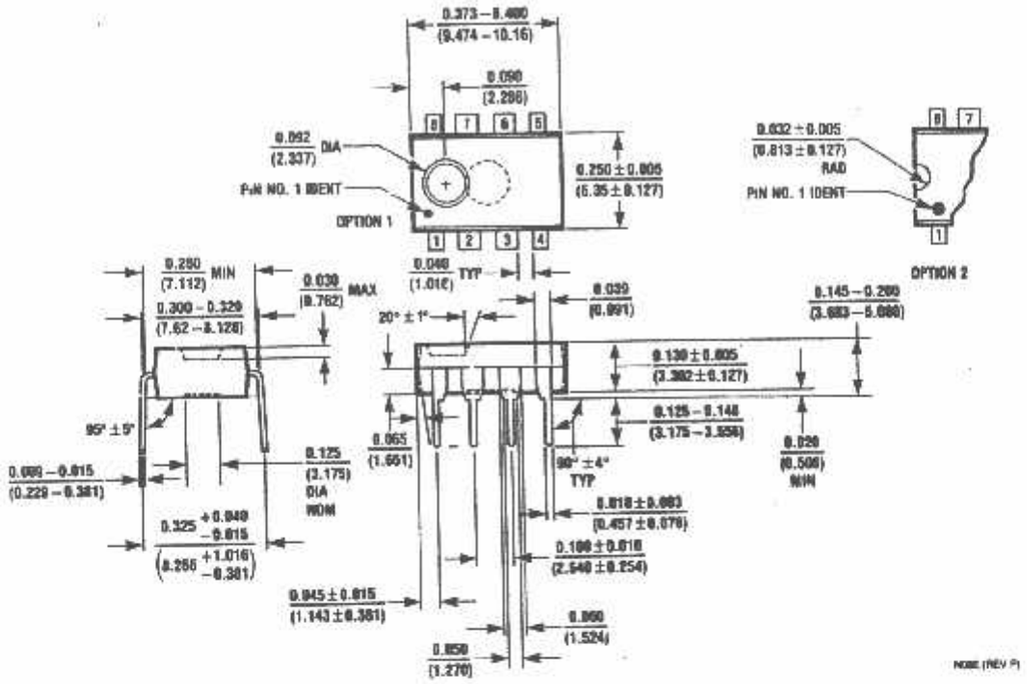
Metal Can Package (H)
Order Number LM567H or LM567CH
NS Package Number H08C





Small Outline Package (M)
Order Number LM567CM
NS Package Number M08A

Physical Dimensions inches (millimeters) unless otherwise noted (Continued)



Molded Dual-In-Line Package (N)
Order Number LM567CN
NS Package Number N08E

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LCM

Liquid Crystal Display Modules

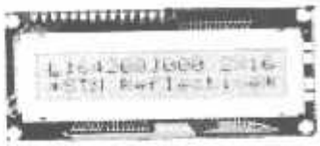
Seiko Instruments GmbH

Dot Matrix Liquid Crystal Display Modules

CHARACTER TYPE

- **FEATURES :**
  - Slim, light weight and low power consumption
  - High contrast and wide viewing angle
  - Built-in controller for easy interfacing
  - LCD modules with built-in EL or LED backlight

M1641



L1642

L1614

M1632

L1652

L2012

- **SPECIFICATIONS :**

: Standard products : Products of optional specification

racter Format (character x line)		16 x 1	16 x 2	16 x 2	16 x 2	16 x 4	20 x 2
del		M1641	M1632	L1642	L1652	L1614	L2012
ective		M16410AS	M16320AS	L164200J000S	L165200J200S	L161400J000S	L201200J000S
acklight		M16419DWS	M16329DWS	L164221J000S	L165221J200S	L161421J000S	L201221J000S
backlight		M16417DYS	M16327DYS	L1642B1J000S	L1652B1J200S	L1614B1J000S	L2012B1J000S
ective (wide temp)		M16410CS	M16320CS	L164200L000S	L165200L200S	L161400L000S	L201200L000S
backlight (wide temp)		M16417JYS	M16327JYS	L1642B1L000S	L1652B1L200S	L1614B1L000S	L2012B1L000S
racter font		5x7 dots + cursor	5x7 dots + cursor	5x7 dots + cursor	5x7 dots + cursor	5x7 dots + cursor	5x7 dots + cursor
dule	Reflective	80,0 x 36,0 x 11,3	85,0 x 30,0 x 10,1	80,0 x 36,0 x 11,3	122,0 x 44,0 x 11,3	87,0 x 60,0 x 11,6	116,0 x 37,0 x 11,3
	EL backlight	80,0 x 36,0 x 11,3	85,0 x 30,0 x 10,1	80,0 x 36,0 x 11,3	122,0 x 44,0 x 11,3	87,0 x 60,0 x 11,6	116,0 x 37,0 x 11,3
(WxT) mm	LED backlight	80,0 x 36,0 x 15,8	80,0 x 30,0 x 15,8	80,0 x 36,0 x 15,8	122,0 x 44,0 x 15,8	87,0 x 60,0 x 15,9	116,0 x 37,0 x 15,8
wing area (HxV) mm		64,5 x 13,8	62,0 x 16,0	64,5 x 13,8	99,0 x 24,0	61,8 x 25,2	83,0 x 18,6
racter size (HxV) mm *1		3,07 x 5,73	2,78 x 4,27	2,95 x 3,80	4,84 x 8,06	2,95 x 4,15	3,20 x 4,85
size (HxV) mm		0,55 x 0,75	0,50 x 0,55	0,50 x 0,55	0,92 x 1,10	0,55 x 0,55	0,60 x 0,65
wer supply voltage (VDD-VSS) V		+ 5 V	+ 5 V	+ 5 V	+ 5 V	+ 5 V	+ 5 V
rrent consumption	IDD	1,5	2,0	1,6	2,0	2,7	2,0
A,typ)	ILC *4	0,2	0,2	0,3	0,4	1,1	0,4
iving method (duty)		1/16	1/16	1/16	1/16	1/16	1/16
uilt-in LSI		KS0066 or equivalent	KS0066 MSM5839 or equivalent	KS0066 MSM5839 or equivalent	KS0066 MSM5839 or equivalent	KS0066 KS0063 or equivalent	KS0066 KS0053 or equivalent
perating temperature (°C)	normal temp.	0 to + 50	0 to + 50	0 to + 50	0 to + 50	0 to + 50	0 to + 50
	wide temp. *2	- 20 to + 70	- 20 to + 70	- 20 to + 70	- 20 to + 70	- 20 to + 70	- 20 to + 70
torage temperature (°C)	normal temp.	- 20 to + 60	- 20 to + 60	- 20 to + 60	- 20 to + 60	- 20 to + 60	- 20 to + 60
	wide temp.	- 30 to + 80	- 30 to + 80	- 30 to + 80	- 30 to + 80	- 30 to + 80	- 30 to + 80
Weight	Reflective	25	25	25	50	50	40
g, typ.)	EL backlight	30	30	30	55	55	45
	LED backlight	35	40	35	65	65	60
	Model	5S	5S	5S	5C	5A	5A
nverters	Power supply (V)	+ 5.0	+ 5.0	- 5.0	+ 5.0	+ 5.0	+ 5.0
or EL	current consumption (mA) *3	10	10	10	35	45	45
LED	Forward current consumption (mA)	100	112	100	240	200	154
backlight	Forward input voltage (V,typ.)	+ 4,1	+ 4,1	+ 4,1	+ 4,1	+ 4,1	+ 4,1

H : Horizontal V : Vertical T : Thickness (max)

*1 : Excluding cursor

*2 : With external temperature compensation

*3 : Including EL backlight

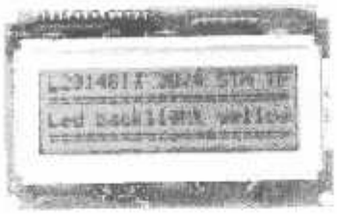
*4 : Based on normal temperature range

Since our policy is one of continues improvements we reserve the right to change the specifications for the products in the catalogue without notice.

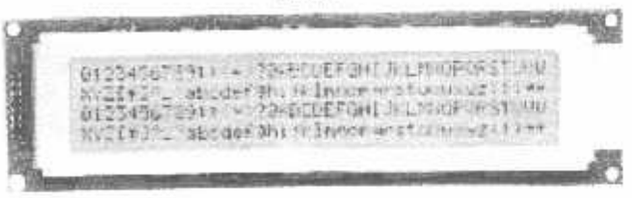
L2022

L2432

L4042



L2014



M4024

• SPECIFICATIONS :

[ ] : Standard products [ ] : Products of optional specification

Character Format (character x line)		20 x 2	20 x 4	24 x 2	40 x 2	40 x 4
Model		L2022	L2014	L2432	L4042	M4024
Reflective		-	L201400J000S	L243200J000S	L404200J000S	M40240AS
EL backlight		-	L201421J000S	L243221J000S	L404221J000S	M40249DWS
LED backlight		-	L2014B1J000S	L2432B1J000S	L4042B1J000S	M40247DYS
Reflective (wide temp)		L202200P000S	L201400L000S	L243200L000S	L404200L000S	M4024DCS
LED backlight (wide temp)		L2022B1P000S	L2014B1L000S	L2432B1L000S	L4042B1L000S	M40247JYS
Character font		5x7 dots + cursor	5x7 dots + cursor	5x7 dots + cursor	5x7 dots + cursor	5x7 dots + cursor
Module size (HxVxT) mm	Reflective	180,0 x 40,0 x 10,5	98,0 x 60,0 x 11,6	118,0 x 36,0 x 11,3	182,0 x 33,5 x 11,3	190,0 x 54,0 x 10,1
	EL backlight	180,0 x 40,0 x 10,5	98,0 x 60,0 x 11,6	118,0 x 36,0 x 11,3	182,0 x 33,5 x 11,3	190,0 x 54,0 x 10,1
	LED backlight	180,0 x 40,0 x 14,8	98,0 x 60,0 x 15,8	118,0 x 36,0 x 15,8	182,0 x 33,5 x 16,3	190,0 x 54,0 x 16,3
Viewing area (HxV) mm		149,0 x 23,0	76,0 x 25,2	94,5 x 17,8	154,4 x 15,8	147,0 x 29,5
Character size (HxV) mm *1		6,00 x 9,66	2,95 x 4,15	3,20 x 4,85	3,20 x 4,85	2,78 x 4,27
Dot size (HxV) mm		1,12 x 1,12	0,55 x 0,55	0,60 x 0,65	0,60 x 0,65	0,50 x 0,55
Power supply voltage (VDD-VSS) V		+5 V	+5 V	+5 V	+5 V	+5 V
Current consumption (mA,typ)	IDD	4,2	2,9	2,5	3,0	8,0
	ILC *4	2,6	1,2	0 5	1,0	3,0
Driving method (duty)		1/16	1/16	1/16	1/16	1/16
Built-in LSI		KS0066 KS0063 or equivalent	KS0066 MSM5839 or equivalent	KS0066 KS0063 or equivalent	KS0066 KS0063 or equivalent	KS0066 MSM5839 or equivalent
Operating temperature (°C)	normal temp.	-	0 to + 50	0 to + 50	0 to + 50	0 to + 50
	wide temp. *2	20 to + 70	- 20 to + 70	- 20 to - 70	- 20 to + 70	- 20 to + 70
Storage temperature (°C)	normal temp.	-	- 20 to + 60	- 20 to + 60	- 20 to + 60	- 20 to + 60
	wide temp.	- 30 to + 80	- 30 to + 80	- 30 to + 80	- 30 to + 80	- 30 to + 80
Weight (g. typ.)	Reflective	80	55	40	70	90
	EL backlight	-	60	45	75	105
	LED backlight	110	70	60	95	140
Inverters for EL	Model	-	5A	5A	5C	5D
	Power supply (V)	+ 5.0	+ 5.0	+ 5.0	+ 5.0	+ 5.0
	current consumption (mA) *3	-	45	45	25	80
LED backlight	Forward current consumption (mA)	320	240	150	260	480
	Forward input voltage (V,typ.)	+ 4,1	+ 4,1	+ 4,1	+ 4,1	+ 4,1

H : Horizontal V : Vertical T : Thickness (max)

*1 : Excluding cursor

*2 : With external temperature compensation

*3 : Including EL backlight

*4 : Based on normal temperature range

Dot Matrix Liquid Crystal Display Modules

GRAPHIC TYPE

- **FEATURES :**
  - •Wide viewing angle and high contrast
  - •Full dot configuration fits any application
  - •Slim, light weight and low power consumption
  - •Available in STN and FSTN

- **SPECIFICATIONS :**

format (HxV,dot)			97 x 32	128 x 32	128 x 64	128 x 64
			Y97031	G1213	G1216	G1226
el			-	-	-	-
l type	Reflective	built-in RAM	-	-	-	-
ay mode)	Reflective wide temp.	built-in RAM	-	G121300N000S	G121600N000S	-
	LED backlight	built-in RAM	-	-	-	G1226B1J000S
	LED backlight wide temp	built-in RAM	-	G1213B1N000S	G1216B1N000S	-
TN type	Transmissive	-	-	-	-	-
W mode)	with CFL backlight	built-in controller	-	-	-	-
	Transflective	built-in RAM	Y97031LF00W	-	-	-
dule size	Reflective (no backlight)		47,5 x 65,4 x 2,1	75,0 x 41,5 x 6,8	75,0 x 52,7 x 6,8	-
x V x T)	LED backlight		-	75,0 x 41,5 x 8,9	75,0 x 52,7 x 8,9	93,0 x 70,0 x 11,4
	CFL backlight		-	-	-	-
wing area (HxV) mm			43,5 x 23,9	60,0 x 21,3	60,0 x 32,5	70,7 x 38,8
size (H x V) mm			0,35 x 0,48	0,40 x 0,48	0,40 x 0,40	0,44 x 0,44
pitch (H x V) mm			0,39 x 0,52	0,43 x 0,51	0,43 x 0,43	0,48 x 0,48
wer supply voltage (V)		(VDD - VSS)	+5,0	+5,0	+5,0	+5,0
		(VLC - VSS)	-	-8,0	-8,1	-8,2
rrent consumption		IDD	0,10	2,0	2,0	3,0
		IDD (built-in controller)	-	-	-	-
A, typ.)		ILC	-	1,8	1,8	2,0
Driving method (duty)			1/33	1/64	1/64	1/64
lt-in LSI		Driver	SED1530 or equivalent	HD61202 HD61203 or equivalent	HD61202 HD61203 or equivalent	KS0107 KS0108 or equivalent
		Controller	-	-	-	-
erating temperature range (°C)			- 20 to + 70	- 20 to + 70	- 20 to + 70	0 to + 50
orage temperature range (°C)			- 30 to + 80	- 30 to + 80	- 30 to + 80	- 20 to + 60
eight	Reflective (Transflective no backlight)		10	23	35	-
typ.)	LED backlight		-	35	45	72
	CFL backlight		-	-	-	-
ED backlight	Forward current consumption (mA)		-	40	90	125
	Forward input voltage (V, typ.)		-	3,8	4,1	4,1
	Mode		-	-	-	-
verter for CFL	Power supply voltage (V)		-	-	-	-
	Current consumption (mA, typ.)		-	-	-	-

1 : built-in DC/DC converter (single power source)

2 : Use with external temperature compensation circuit

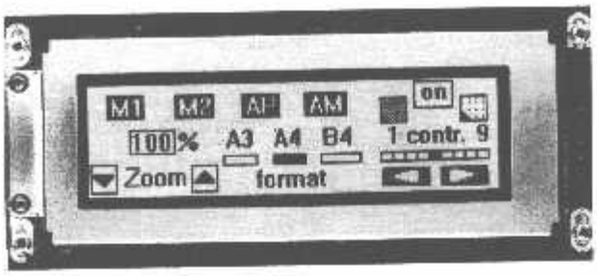
Since our policy is one of continues improvements we reserve the right to change the specifications of the products in the catalogue without notice.

Dot format (HxV,dot)			240 x 64	240 x 128	320 x 200	320 x 240	640 x 200
Model			G2446	G242C	G321D	G324E	G649D
STN type (Gray mode)	Reflective	built-in RAM	-	-	-	-	-
	Reflective wide temp.	built-in RAM	-	-	-	-	-
	LED backlight	built-in RAM	-	-	-	-	-
	LED backlight wide temp.	built-in RAM	-	-	-	-	-
FSTN type (B&W mode)	Transmissive	-	G2446X5R1A0S	G242CX5R1ACS	G321DX5R1A0S	G324EX5R1A0S	G649DX5R010S
	with CFL backlight	built-in controller	G2446X5R1ACS	G242CX5R1A0S	G321DX5R1ACS	G324EX5R1ACS	-
	Transflective	built-in RAM	-	-	-	-	-
Module size (H x V x T) mm	Reflective (no backlight)			-	-	-	-
	LED backlight			-	-	-	-
	CFL backlight		151,0 x 79,0 x 15,1	180,0 x 110,0 x 15,1	166,0 x 134,0 x 15,1	166,0 x 134,0 x 15,1	260,0 x 122,0 x 15,7
Viewing area (HxV) mm			134,0 x 41,0	134,0 x 76,0	128,0 x 110,0	128,0 x 110,0	216,0 x 83,0
Dot size (H x V) mm			0,49 x 0,49	0,47 x 0,47	0,34 x 0,48	0,32 x 0,39	0,30 x 0,36
Dot pitch (H x V) mm			0,53 x 0,53	0,51 x 0,51	0,38 x 0,52	0,36 x 0,43	0,33 x 0,39
Power supply voltage (V)		(VDD - VSS)	+ 5,0	+ 5,0	+ 5,0	+ 5,0	+ 5,0
		(VLC - VSS)	*1	*1	-24,0	-24,0	-24,0
Current consumption (mA, typ.)		IDD	12	30	8	7,5	11
		IDD (built-in controller)	15	40	23	23	-
		ILC	-	-	6	6,5	9
Driving method (duty)			1/64	1/128	1/200	1/240	1/200
Built-in LSI		Driver	MSM5298 MSM5299 or equivalent	KS0103 KS0104 or equivalent	MSM5298 MSM5299 or equivalent	HD66204 HD66205 or equivalent	MSM5298 MSM5299 or equivalent
		Controller	SED1330FB	SED1330FB	SED1330FB	SED1330FB	-
Operating temperature range (°C)			0 to + 50	0 to + 50	0 to + 50	0 to + 50	0 to + 50
Storage temperature range (°C)			- 20 to + 60	- 20 to + 60	- 20 to + 60	- 20 to + 60	- 20 to + 60
Weight (g, typ.)	Reflective (Transflective no backlight)		-	-	-	-	-
	LED backlight		-	-	-	-	-
	CFL backlight		200	280	350	350	420
LED backlight	Forward current consumption (mA)		-	-	-	-	-
	Forward input voltage (V, typ.)		-	-	-	-	-
Inverter for CFL	Mode		4800210	4800210	4800210	4800210	4800120
	Power supply voltage (V)		+ 5,0	+ 5,0	+ 5,0	+ 5,0	+ 12,0
	Current consumption (mA, typ.)		250	350	365	365	390

*1 built-in DC/DC converter (single power source)

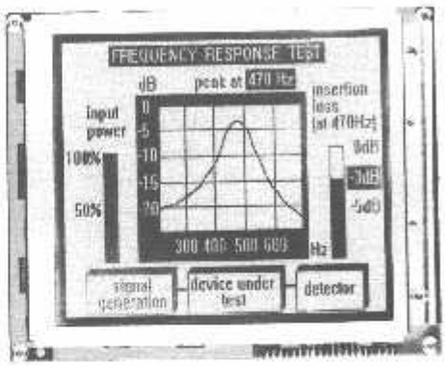
*2 Use with external temperature compensation

Since our policy is one of continous improvement, we reserve the right to change the specifications of the products in the catalogue without notice.



G2446

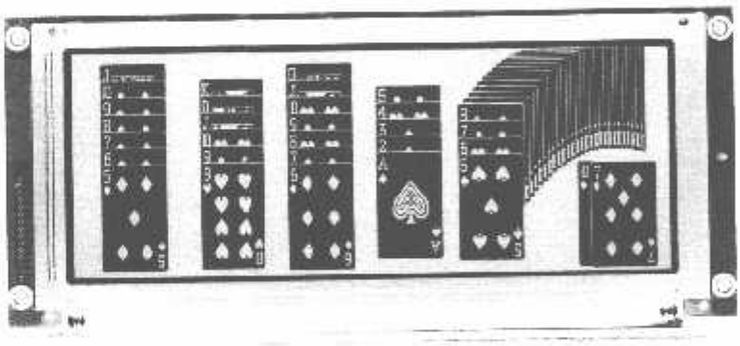
G1226



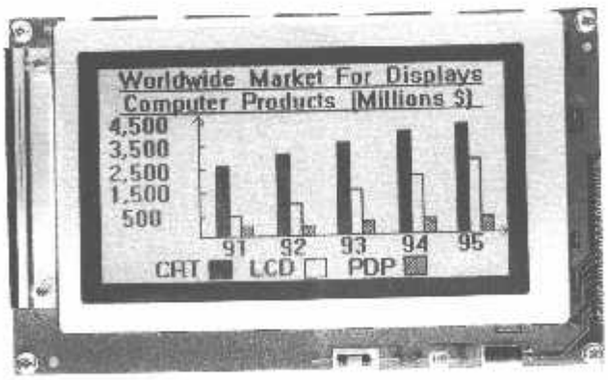
G321D

G1216

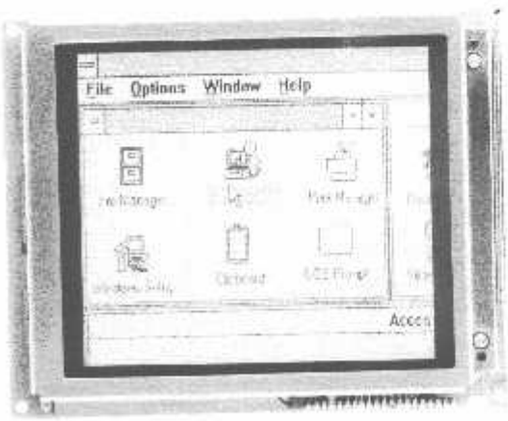
G1213



G649D



G242C



G324E

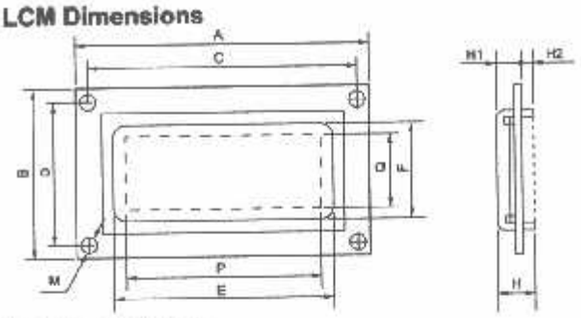
;HECK LIST FOR CUSTOM DESIGNED LCD MODULE

. Company_____ **2. Application**_____ **3. Customer Specified Part No.**_____

. Design

☐ New ☐ Modified : Manufacturer_____ , Part No._____ , Remarks _____
☐ Equivalent: Manufacturer_____ , Part No._____ , Remarks _____

. LCM Dimensions



A x B : Module size _____ x _____ mm
E x F : Viewing area _____ x _____ mm
P x Q : Active display area _____ x _____ mm
C : Length between mounting holes _____ mm
D : Length between mounting holes _____ mm
M : Diameter of mounting hole _____ mm
H : Total thickness _____ mm
H1 : Upper thickness _____ mm
H2 : Lower thickness _____ mm

. Display Contents

☐ Character type: _____ characters _____ lines
Character font _____ x _____ dots + cursor
Character pitch _____ x _____ mm
Dot pitch _____ x _____ mm
Dot size _____ x _____ mm
☐ Graphics (Full dot) type: _____ x _____ dots
Dot pitch _____ x _____ mm
Dot size _____ x _____ mm
☐ Segment type: _____ digits _____ lines
☐ Others _____

'. LCD Panel

Viewing angle: ☐ 6 o'clock ☐ 12 o'clock ☐ _____ o'clock
Type: ☐ TN ☐ FSTN (Black and white)
☐ STN (☐ Yellow green ☐ Gray ☐ Blue)
Chromaticity coordinates
(_____ ≦ x ≦ _____ , _____ ≦ y ≦ _____)
☐ Positive type ☐ Negative type
☐ Reflective ☐ Transflective ☐ Transmissive
☐ Others _____
Gray scale: ☐ Yes _____ gray scale ☐ No
Preferential specifications:
☐ Response time t_{on} ____ ms (____ °C) t_{off} ____ ms (____ °C)
☐ Viewing angle ____ deg. (____ °C) ☐ Contrast ____ (____ °C)
☐ Others _____
LCD surface finishing:
☐ Normal ☐ Anti-glare ☐ _____
Polarizer color: ☐ Normal (neutral gray) ☐ Red
☐ Green ☐ Blue ☐ _____

8. Driving Method

Multiplexing: 1/ _____ duty, 1/ _____ bias
Frame frequency: _____ Hz

9. IC

LCD driver: ☐ Specified ☐ Unspecified
Segment driver _____ (Manufacturer _____)
Common driver _____ (Manufacturer _____)
Controller: ☐ Internal ☐ External
Type No. _____ (Manufacturer _____)
MPU: ☐ Internal ☐ External
Type No. _____ (Manufacturer _____)
RAM: ☐ Internal ☐ External
Type No. /Memory size _____ (Kbit) (Manufacturer _____)

10. Power Supply

☐ Single power supply: ☐ 5V ☐ _____ V
☐ 2 power supplies
For logic: (V_{DD}-V_{SS}) : ☐ 5V ☐ _____ V
For LC drive: (V_{LC}-V_{SS}) : ☐ _____ V

11. Temperature Compensation Circuit

☐ Internal ☐ External ☐ Unnecessary
Compensation range: ☐ 0°C to 50°C ☐ ___°C to ___°C

12. Current Consumption

For logic: typ. _____ mA, max. _____ mA
For LC drive: typ. _____ mA, max. _____ mA
Others ( ) : typ. _____ mA, max. _____ mA

13. Contrast Adjustment

☐ Internal ☐ External ☐ Unnecessary
Method: ☐ Temp. compensation circuit ☐ Volume ☐ ____

14. Temperature Range

Operating temperature range: ☐ 0°C to 50°C ☐ ____ °C to ____ °C
Storage temperature range: ☐ - 20°C to 60°C ☐ ____ °C to ____ °C

15. Input/Output Terminals

Specifying allocation: ☐ Yes ☐ No
Specifying position: ☐ Yes ☐ No

16. Weight

typ. _____ g, max. _____ g

17. Connector

☐ Internal ☐ External ☐ Unnecessary
Type No. _____ (Manufacturer _____)

18. Backlight

☐ Internal ☐ External ☐ Unnecessary
☐ EL: ☐ Green ☐ White ☐ _____
☐ LED: ☐ Yellow green ☐ Amber ☐ _____
☐ CFL: ☐ White ☐ _____
☐ Incandescent lamp ☐ Others _____
☐ Backlight type ☐ Edge backlight type
Brightness: _____ cd/m^2
Inverter: ☐ Internal ☐ External ☐ Unnecessary
Power supply voltage _____ V
Current consumption (backlight included) _____ mA
Brightness control: ☐ Yes ☐ No

19. Others

_____
_____
_____

20. Schedule

Estimate: _____
Sample: Delivery _____ , Quantity: _____ pcs
Mass production: Target price: _____
Delivery _____ , Total quantity: _____ pcs
Quantity per month _____ pcs

Precautions

Safety Instructions

If the LCD panel is damaged, be careful not to get the liquid crystal in your mouth and not to be injured by crushed glasses.

If you should swallow the liquid crystal, first, wash your mouth thoroughly with water, then, drink a lot of water and induce vomiting, and then, consult a physician.

If the liquid crystal should get in your eye, flush your eye with running water for at least fifteen minutes.

If the liquid crystal touches your skin or clothes, remove it and wash the affected part of your skin or clothes with soap and running water.

EL or CFL backlight is driven by a high voltage with an inverter. Do not touch the connection part or the wiring pattern of the inverter.

Do not use inverters without a load or in the short-circuit mode.

Use the LCD module within the rated voltage to prevent overheating and/or damage. Also, take steps to ensure that the connector does not come off.

Handling Precautions

- Since the LCD panel has glass substrate, avoid applying mechanical shock or pressure on the module. Do not drop, bend, twist or press the module.
- Do not soil or damage LCD panel terminals.
- Since the polarizer is made of easily-scratched material, be careful not to touch or place objects on the display surface.
- Keep the display surface clean. Do not touch it with your skin.
- CMOS LSI is used in the LCD module. Be careful of static electricity.
- Do not disassemble the module or remove the liquid crystal panel or the panel frame.
- Do not damage the film surface of the EL lamp; otherwise the lamp will be damaged by humidity.
- To set an EL lamp in an LCD module, push the EL lamp with its emitting side up, without pushing the rubber connectors too hard. If you damage them, the LCD module may not work properly.

Mounting and Designing

- To protect the polarizer and the LCD panel, cover the display surface with a transparent plate (e.g., acrylic or glass) with a small gap between the transparent plate and the display surface.
- Keep the module dry. Avoid condensation to prevent the transparent electrodes from being damaged.
- Drive LCD panel with AC waveform in which DC element is not included to prevent deterioration in the LCD panel.
- Contrast of LCD varies depending on the ambient temperature. To offer the optimum contrast, LC drive voltage should be adjusted. LCD driven in a high duty ratio must be provided with drive voltage adjustment method.
- Mount a LCD module with the specified mounting part/ holes.
- Design the equipment so that input signal is not applied to the LCD module while power supply voltage is not applied to it.
- Do not locate the CFL tube and the lamp lead wire close to a metal plate or a plated part inside the equipment. Otherwise stray capacity causes a drop in voltage, decreasing the brightness and the ability to start-up.

Cleaning

- Do not wipe the polarizer with a dry cloth, as it may scratch the surface.
- Wipe the LCD panel gently with a soft cloth soaked with a petroleum benzine.
- Do not use ketonic solvents (ketone and acetone)or aromatic solvents (toluene and xylene), as they may damage the polarizer.

Storing

- Store the LCD panel in a dark place, where the temperature is 25°C±10°C and the relative humidity below 65%. If possible, store the LCD panel in the packaging situation when it was delivered.
- Do not store the module near organic solvents or corrosive gases.
- Keep the module (including accessories) safe from vibration, shock and pressure.
- Use an LCD module with built-in EL backlight within six months of delivery.
- EL backlight is easily affected by environmental conditions such as temperature and humidity; the quality may deteriorate if stored for an extended period of time. Contact Seiko Instruments GmbH for details.
- Some parts of the backlight and the inverter generate heat. Take care so that the heat does not affect the liquid crystal or any other parts.
- Dust particles attached to the surface of the LCD or the surface of the backlight degrade the display quality. Be careful to keep dust out in designing the structure as well as in handling the module.
- Black or white air-bubbles may be produced if the LCD panel is stored for long time in the lower temperature or mechanical shocks are applied onto the LCD panel.

On This Brochure

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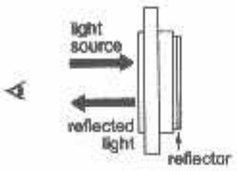
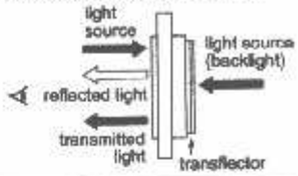
iquid Crystal Display Modules

REFLECTIVE/TRANSFLECTIVE/TRANSMISSIVE LCD

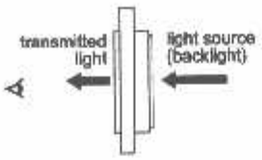
Reflective LCD
Reflector bonded to the rear polarizer reflects the incoming ambient light. Low power consumption because no backlight is required.



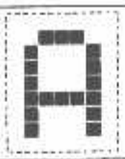
❷ Transflective LCD
Transflector bonded to the rear polarizer reflects light from the front as well as enabling lights to pass through the back. Used with backlight off in bright light and with it on in low light to reduce power consumption.

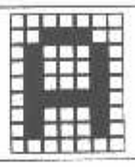


❸ Transmissive LCD
Without reflector or transflector bonded to the rear polarizer. Backlight required. Most common is transmissive negative image.



POSITIVE/NEGATIVE MODE

Positive type	

Negative type		Negative type (inverse image) (when data is inverted)	

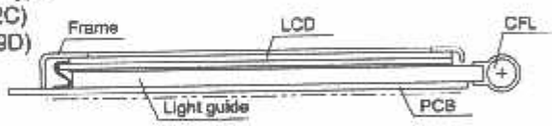
TN TYPE/STN TYPE/FSTN TYPE

TN	(Background/dot color) Gray/Black	TN(Twisted Nematic) type is most conventional and economical. It is used for static drive LCD and low-duty drive LCD (watch,calculator, etc.)
STN	Yellowgreen/Dark blue Gray/Dark blue White/Blue	STN (Super Twisted Nematic) type has a higher twist angle, and thus provides clear visibility and wider viewing angle. This is suitable especially for high-duty drive LCD.
FSTN	White/Black	FSTN (Film Super Twisted Nematic) type utilizes RCF (Retardation Control Film) to remove the coloring of STN LCD. Thus FSTN type provides easy-to-read black-and-white display.

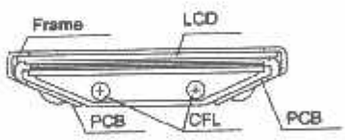
STRUCTURE AND FEATURE OF LCD MODULE WITH BACKLIGHT

CFL (Cold Cathode Fluorescent Lamp) backlight
Features: high brightness, long service life, inverter required

- Edge backlight type
  (G2446,G242C)
  (G321D,G649D)

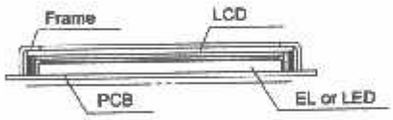


- Backlight type



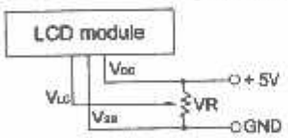
EL (Electroluminescent Lamp) backlight
LED (Light Emitting Diode) backlight

Features: EL: thin, inverter required
LED: long service life, low voltage driving, no inverter required

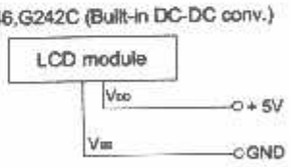


POWER SUPPLY

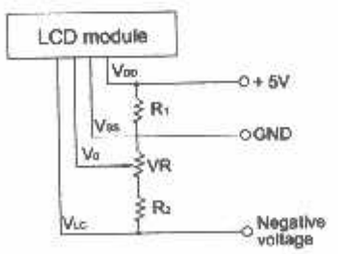
- Character modules (single power supply)



- G2446,G242C (Built-in DC-DC conv.)

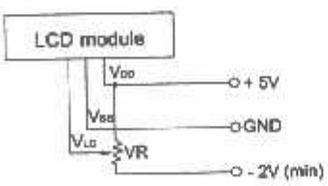


- G321D, G324E and G649D

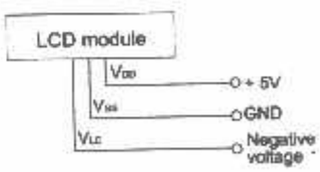


Note 1:Contrast can be adjusted by VR.
Note 2:For module with backlight, power supply for backlight is necessary.

- Character Modules(Dual power supply)



- Y1206 and G1226



-Negative voltage should be variable for contrast adjustment.

HECK LIST FOR CUSTOM DESIGNED LCD

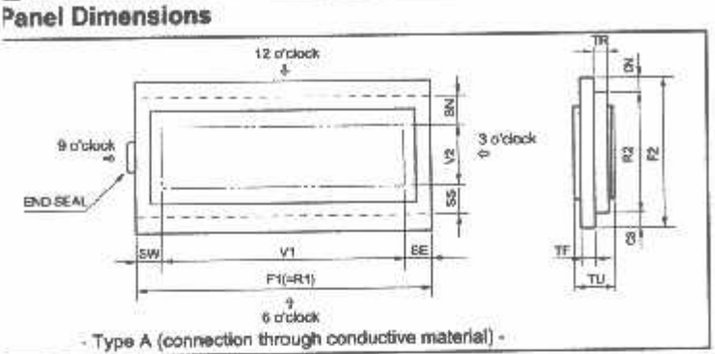
Company_____ **2. Application**_____ **3. Customer Specified Part No.**_____

Design

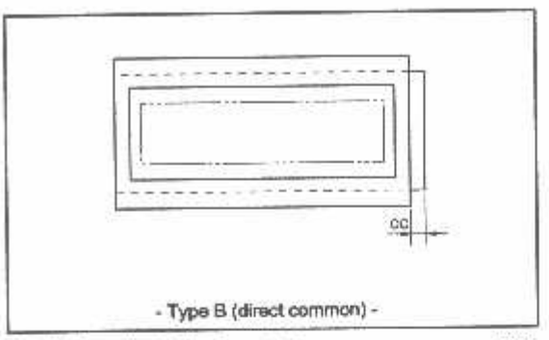
☐New ☐Modified: Manufacturer _____ , Part No._____ , Remarks_____

☐Equivalent: Manufacturer_____ , Part No._____ , Remarks_____

Panel Dimensions



- Type A (connection through conductive material) -



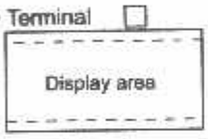
- Type B (direct common) -

: Horizontal length of upper glass _____ mm
: Vertical length of upper glass _____ mm
: Horizontal length of lower glass _____ the same as F1
*: Vertical length of lower glass _____ mm
R2 is generally longer than F2 when terminals are with pin.
: TR***: Thickness of glass _____ mm
**Standard type: 1.1 mm or 0.7 mm
J: Thickness of LCD _____ mm
id seal: ☐Right ☐Left ☐Right or Left

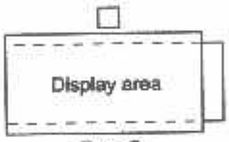
V1 :Horizontal length of viewing area _____ mm
V2 :Vertical length of viewing area _____ mm
CN**: Terminal length _____ mm
CS**:Terminal length _____ mm
**CN or CS=0 in case of one side terminal type.
CC: Terminal length _____ mm
SE,SW,SN,SS : Seal width
(According to design or manufacturing condition:
about 2.0 mm to 4.0 mm)

Panel Form

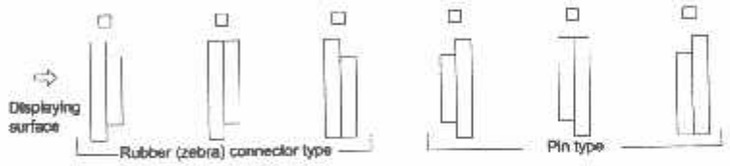
• Terminal ☐



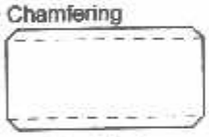
- Type A -



- Type B -

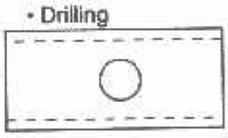


• Chamfering



☐ Yes
☐ No

• Drilling



☐ Yes
☐ No

. Display Mode

Viewing angle : ☐6 o'clock ☐12 o'clock ☐_____o'clock
Type: ☐TN ☐FSTN (Black and white)
☐STN: (☐ Yellow green ☐ Gray ☐ Blue)
Chromaticity coordinates (____≦x≦____, ____≦y≦____)
☐Positive type ☐Negative type
☐Reflective ☐Transflective ☐Transmissive
Preferential specifications:
☐Response time t_{on} ____ ms (____ °C) t_{off} ____ ms (____ °C)
☐Viewing angle ____ deg. (____ °C) ☐Contrast ____ (____ °C)
☐Others _____

3. Polarizer

Surface finishing: ☐Normal ☐Anti-glare ☐_____
Color: ☐Normal (neutral gray) ☐Red ☐Green
☐Blue ☐_____
Front polarizer : ☐Attached type ☐Separate type
Rear polarizer : ☐Attached type ☐Separate type

9. Driving Method

☐Static ☐Multiplexing: (1/_____duty, 1/_____bias)
Operating voltage (V_{OP}) :_____V
Frame frequency:_____Hz
Driving IC: _____(Manufacturer _____)
Current consumption:_____μA

10. Temperature Range

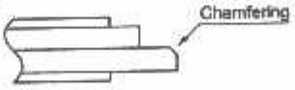
Operating temperature range
☐With temperature compensation circuit (or volume)
(☐ 0°C to 50°C ☐ _____°C to_____°C)
☐Without temperature compensation circuit
(☐ 0°C to 50°C ☐ _____°C to_____°C)
Storage temperature range
(☐ - 20°C to 60°C ☐ _____°C to_____°C)

11. Terminal Connecting Method

☐Rubber connector (Zebra rubber)
☐Pin: ☐DIL ☐SIL ☐_____
Pitch (☐2.54 ☐_____mm) Length (_____mm)
☐Heat seal: ☐Equipped ☐Unnecessary

12. Others

Print (Characters, lines, masks etc.) : ☐Yes ☐No
Protective film:
☐Yes (Color: ☐ Red ☐Translucent ☐Transparent) ☐No
Chamfering (for heat-seal connector) :
☐Yes (Position:_____)
(Quantity:_____)
☐No



13. Schedule

Estimate :_____
Sample : Delivery_____ , Quantity :_____pcs
Mass production : Target price : _____
Delivery _____ , Total quantity:_____pcs
Quantity per month:_____pcs