TUGAS AKHIR

PERENCANAAN DAN PEMBUATAN ALAT PENGUKUR TEKANAN DARAH DIGITAL BERBASIS MK AT89S51

Disusun Oleh:

OKTAVIANTO

03.52.010

KONSENTRASI TEKNIK ENERGI LISTRIK
JURUSAN TEKNIK ELEKTRO D-III
FAKULTAS TEKNOLOGI INDUSTRI
INSTITUT TEKNOLOGI NASIONAL MALANG

Maret 2007

LEMBAR PERSETUJUAN

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Disusun Oleh :

Oktavianto

0352010

Mengetahui
Ketua jurusan elektro DIII

(Ir. Choirul saleh, MT)

Diperiksa dan Disetujui
Dosen Pembimbing

(Bambang Prio H,ST, MT)

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ABSTRAK

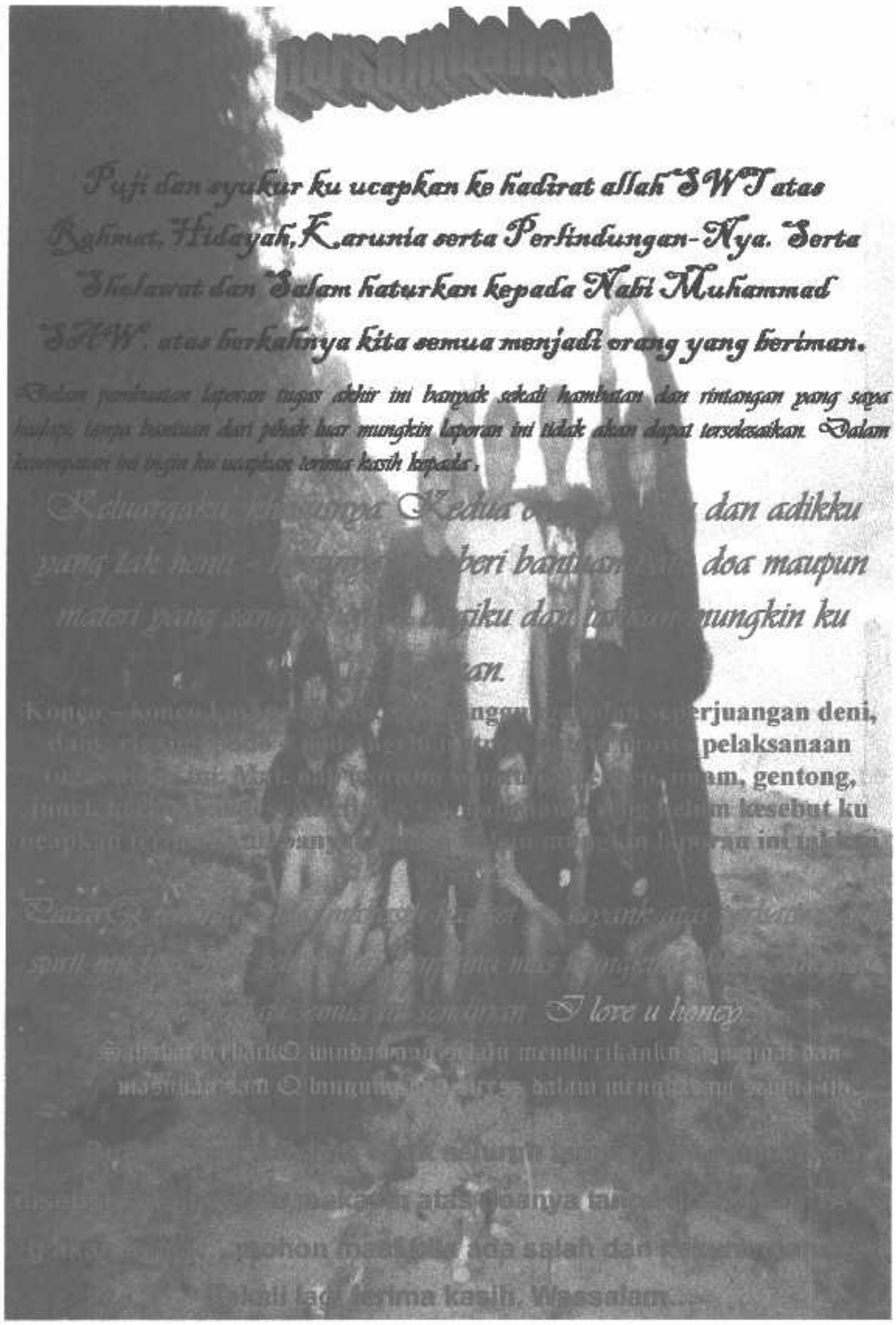
" Perencanaan Dan Pembuatan Alat Pengukur Tekanan Darah Digital Berbasis MK 89S51" Oktavianto, 0352010, Tugas Akhir, Teknik Energi Listrik DIII, institut Teknologi Nasional Malang. Pembimbing Bambang Prio Hartanto, ST, MT.

Pada manusia normalnya range kondisi tekanan darah systole 120 mmHg dan nilai diastole 80 mmHg. Untuk mempermudah mengetahui nilai tersebut di buat alat pengukur tekanan darah digital. Alat ini mengguanakn sensor kondensor sebagai pembangkit frekwensi yang sangat kecil. Selain itu juga menggunakan sensor LDR, yaitu sebuah tranduser yang mengubah intensitas cahaya menjadi besaran listrik.Nilai yang di hasilkan dari alat ini berupa nilai systole dan diastole dengan keterangan yang muncul beberapa saat dari nilai tersebut, sehingga kita dapat mengetahui masuk dalam kategori manakah nilai tekanan darah orang yang kita ukur. Kelebihan dari alat ini adalah dapat mengukur nilai tekanan dengan keakuratan yang besar di banding menggunakan pengukur analog.perancangan alat ukur tekanan darah di atas menyangkut pembuatan simulasi, mengguinakan MK AT89S51, dan pembuatan sensor suara untuk mendeteksi denyut jantung. Tujuannya pembuatan alat ukur ini agar dapat di gunakan dengan mudah oleh para pengukur tekanan darah dan mengurangi kesalahan dari pengukur analog.

Alat ukur yang di gunakan untuk mendeteksi suara dalam frekwensi yang sangat rendah mengguanakan kondensor yang kemudian dikuatkan agar dapat di baca oleh MK 89S51. untuk menentukan besarnya nilai menggunakan LDR yang kemudian nilai out putan di konversikan oleh ADDA PCF 8591 agar dapat diproses oleh MK 89S51 sebagai pengolah data yang kemudian di tampilkan oleh LCD.LCD yang di gunakan type M1632.

Dari studi yang di lakukan didapat keterangan klasifikasi tekanan darah orang dewasa, data ini di gunakan untuk menentukan dalam kategori mana nilai orang yang di ukur. Perencanaan pembuatan alat ini di antaranya merancang sensor I untuk mendeteksi suara agar dapat di olah oleh mikrokontroler. Selain itu merencanakan sensor II unutk menentukan berapa basar nilainya yang kemudian di masukkan ke dalam mikrokontroler setelah di konversi oleh ADDA. Pembuatan simulasi alat pengukur tekanan darah digital ini berpedoman pada alat pengukur tekanan darah analog dengan mengetahui cara kerjanya yang kemudian di konversikan kedalam bentuk digital. Penggunaan mikrokontroler AT89S51 menggunakan yaitu bahasa assembly. Perencanaan sensor suara untuk mendeteksi denyut jantung menggunakan kondensor dengan out putan sebesar 0.015 volt yang kemudian di kuatkan menjadi 3 volt agar dapat di terima oleh mikrokontroler setelah melalui proses pentrigeran.

Kata Kunci : LDR, LCD, MK AT89S51, ADDA PCF 8591, Tekanan Darah, sensor.



persembahan

Puji dan syukur ku ucapkan ke hadirat allah SWT atas Rahmat, Hidayah, Karunia serta Perlindungan-Nya. Serta Sholawat dan Salam haturkan kepada Nabi Muhammad SAW. atas berkatnya kita semua menjadi orang yang beriman.

Dalam pembuatan laporan tugas akhir ini banyak sekali hambatan dan rintangan yang saya hadapi, tanpa bantuan dari pihak luar mungkin laporan ini tidak akan dapat terselesaikan. Dalam kesempatan ini ingin ku ucapkan terima kasih kepada :

Keluargaku tercinta, Ayah, Ibu, Kedua [illegible] dan adikku yang [illegible] memberi bantuan [illegible] doa maupun materi yang [illegible] kepadaku dan [illegible] mungkin ku [illegible]

[illegible] perjuangan deni, [illegible] pelaksanaan [illegible] am, gentong, [illegible] kesebut ku

I love u honey

[illegible] atas segala [illegible]

[illegible] mohon maaf [illegible] ada salah dan [illegible]

[illegible] terima kasih. Wassalam.....

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Puji syukur ke hadirat Tuhan Yang Maha Esa atas rahmat yang telah di berikan kepada saya sehingga saya dapat menyelasaikan penyusunan laporan Tugas Akhir dengan judul " Pemcanaan Dan Pembuatan Alat Pengukur Tekanan Darah Digital Berbasis Mikrokotroler AT89S51 ". Tugas akhir ini di susun untuk memenuhi syarat kelulusan untuk memperoleh gelar Ahli Madya Teknik Elektro Konsentrasi Energi Listrik Institut Teknologi Nasional Malang.

Dalam penyusunan laporan tugas akhir ini banyak sekali pengalaman dan pelajaran yang saya dapatkan, terutama dari dosen pembimbing yang telah banyak sekali meluangkan waktunya. Oleh sebab itu dengan terselesaikannya Tugas Akhir ini, saya mengucapkan terimakasih kepada semua pihak yang telah membantu penyusunan laporan Tugas Akhir ini. Secara khusus penyusun mengucapkan terima kasih kepada :

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DAFTAR ISI

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BAB I

PENDAHULUAN

1.1 Latar Belakang

Sebagian besar instrumen - instrumen medis di rumah sakit umum digunakan untuk mengukur keluhan - keluhan dari si pasien. Misalnya di rumah sakit tertentu mengukur tekanan darah tetapi penggunaan alat pengukurannya masih bersifat manual sehingga ke efektifan dalam pengukurannya masih kurang. Dalam hal ini tekanan darah sangat bermanfaat bagi seorang dokter untuk menentukan penyakit – penyakit yang mungkin di derita oleh seorang pasien. Dengan adanya perkembangan teknologi yang semakin maju dan modern, teknologi tercipta untuk membantu meringankan pekerjaan manusia.

Pada manusia normalnya range kondisi tekanan darah Diastole 80 mmHg dan kondisi systole 120 mgHg. Untuk dapat mendukung alat ini kami menggunakan mikrokontroler AT89S51, terlihat bahwa mikrokontroler AT89S51 memiliki banyak fitur yang menguntunkan. Dipakainya *downloadable flas memori* memungkinkan mikrokontroler ini bekerja sendiri tanpa di perlukan tambahan *chip* lainnya. Sementara *flash memory*nya mampu di program hingga seribu kali.

Sensor yang di pakai ialah berupa kondensor yang di gunakan sebagai pembangkit frekwensi yang sangat kecil. Kondensor merupakan suatu mikropone yang mengkorversi gelombang suara ke dalam sinyal listrik. Yang nantinya akan di kuatkan oleh Amplifier. Selain itu alat ini juga menggunakan sensor LDR, yaitu

sebuah tranduser yang menguibah intesitas cahaya menjadi besaran listrik dengan perubahan resistansinya.

1.2 Rumusan Masalah

Dengan melihat dan memperhatikan latar belakang dari perancangan tekanan darah di atas maka di dapat rumusan masalah sebagai berikut :

1. Bagaimana pembuatan simulasi untuk pembuatan pengukuran tekanan darah ?
2. Bagaimana menggunakan mikrokontroler ATMEL AT89S51 yang digunakan untuk mengontrol semua instrumen ?
3. Bagaiman merencanakan dan membuat sensor suara untuk mendeteksi denyut jantung ?

1.3 Tujuan

Tujuan penulisan untuk membuat alat pengkur tekanan darah secar digital agar dapat di gunakan dengan mudah oleh para pengguna atau para medis dalam pengukuran tekanan darah sehingga dapat mengurangi kesalahan pengukuran yang dilakukan dengan menggunakan peralatan yang masih bersifat manual.

1.4 Batasan Masalah

Agar permasalahan yang akan dibahas ini lebih terarah, maka tugas akhir ini dibatasi hanya pada hal – hal berikut :

1. Hal – hal yang akan diperhatikan dan dipantau adalah tekanan darah pasien normal.

2. Kurang mendetail membahas tentang frekuensi.
3. Penguatan yang digunakan adalah LM386, di gunakan untuk menguatkan tegangan sebesar 200 kali dari tegangan semula.

1.5 Metodologi Penelitian

Metode penelitian atau langkah – langkah yang dilakukan untuk menyelesaikan tugas akhir ini, dapat dilalui melalui tahapan – tahapan sebagai berikut :

1. Survei literature yang mempelajari teori – teori yang berkaitan mengenai cara kerja komponen – komponen yang digunakan dalam perancangan dan pembuatan alat pengukur tekanan darah digital berbasis MK AT89S51.
2. Perancangan dan pembuatan alat untuk mengaplikasikan pada sebuah alat dari dasar – dasar teori penunjang.
3. Pelaksanaan uji coba alat dari hasil perancangan dan pembuatan alat pengukur tekanan darah dengan tampilan LCD berbasis MK AT89S51.
4. Penyusunan laporan menyimpulkan hasil perancangan dan pembuatan alat.

1.6 Sistematika Penulisan

Pada penulisan tugas akhir ini, ditulis sedemikian rupa sehingga diperoleh hubungan yang jelas antara bagian yang satu dengan bagian yang lainnya,maka diperlukan sistematika penulisan sebagai berikut :

Bab I : Merupakan pendahuluan yang berisi tentang latar belakang permasalahan, tujuan, metodologi pembahasan dan sistematika penulisan.

Bab II : Membahas teori penunjang yang membahas teori dasar tentang mikrokontroler dan teori dasar tentang peralatan elektronika pendukung lainnya dalam perancangan tugas akhir ini.

Bab III : Membahas tentang Metodologi penelitian.

Bab IV : Membahas tentang pengujian alat.

Bab V : Merupakan bagian penutup yang berisi kesimpulan dan saran dari hasil tugas akhir ini.

BAB II

TEORI PENUNJANG

2.1 Jantung

Jantung dalam tubuh manusia berfungsi untuk memompa darah yang mengandung oksigen (O_2) ke seluruh sistem sirkulasi. Sistem sirkulasi ini terbentuk dari saluran – saluran pembuluh nandi (arteri), pembuluh balik (vena) dan pembuluh kapiler. Jantung secara fisis terdiri dari empat buah ruang, yaitu dua buah ruang serambi (atrium) dan dua buah bilik (ventrikel). Ruang ini diisi oleh darah pada saat ekpansi dan dikosongkan pada saat kontraksi. Terjadinya kontraksi pada dinding ventrikel ini dikenal dengan istilah *systole*, kemudian diikuti oleh proses ekspansi pada dinding ventrikel yang dikenal dengan istilah *diastole*, dan dilanjutkan dengan proses relaksasi. Setelah masa istirahat (relaksasi) kemudian jantung mengalami kembali *sistole* dan *diastole* begitu proses seterusnya.

2.2 Tekanan Darah

Dalam sistem sirkulasi darah, tekanan darah merupakan parameter yang sanagat penting, karena selalu diperlukan untuk daya dorong mengalirnya darah di dalam pembuluh arteri, arteriola, kapiler dan sistem vena. Dengan adanya aktifitas jantung, maka terjadilah aliran darah dari pembuluh vena ke pembuluh arteri pada sistem sirkulasi tertutup.

Tekanan darah biasanya diukur secara tidak langsung menggunakan sfigmomanometer raksa / jarum dan metode dengar bunyi atau metode auskultasi.

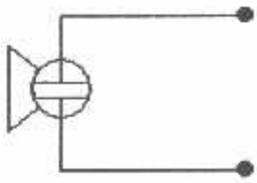
Sebelum pengukuran dilakukan, pasien sebaiknya duduk beberapa menit dalam ruangan sepi pada kursi yang sandarannya nyaman. Tekanan pada saat bunyi pertama kali terdengar atau pada waktu jantung mengucup itulah tekanan darah sistolik (TDS = SBP = Systolic Blood Pressure), tekanan darah diastolik (TDD) ialah tekanan pada saat bunyi hilang atau pada saat jantung mengendor (fase V).

Tekanan darah sistolik dan diastolik pada orang dewasa sangat bervariasi yaitu berkisar antara 95 mmHg – 140 mmHg, tekanan ini dapat meningkat dengan bertambahnya usia. Dilain pihak tekanan diastolik berkisar antara 60 mmHg – 90 mmHg. Namun tekanan darah normal biasanya berkisar antara 120 mmHg untuk tekanan sistolik dan 80 mmHg untuk tekanan diastolik.Tekanan darah normal dipengaruhi oleh beberapa faktor antara lain usia, jenis kelamin, perjalanan waktu dalam sehari semalam yang membentuk perubahan tekanan darah.

2.3 SENSOR 1

2.3.1 Kondensor

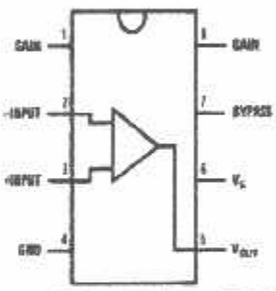
Kondensor merupakan suatu mikropon yang mengkonversi gelombang suara ke dalam sinyal listrik. Sekat rongga yang bergetar menyebabkan suatu komponen listrik menghasilkan aliran arus keluaran pada suatu frekwensi yang sebanding gelombang suara itu. Out put dari kondensor berupa tegangan yang angat rendah yang nantinya akan di kuatkan oleh amplifier.



Gambar 2.1 Rangkaian Kondensor
Sumber : Laporan Tugas Akhir, Andik Winanto, 2004

2.3.2 Pre Amplifier

Pada perancangan ini digunakan amplifier dengan seri LM 386, dimana Op-Amp ini digunakan dalam tegangan yang rendah, dan bisa juga di gunakan batrei sebagai sumber tegangannya, tegangan yang disupplynya sekitar 6V, hanya saja untuk Op-Amp ini di tambahkan kapasitor dan resistor pada kaki 1 dan 8 yang akan sangat kompetibel dengan penguatan yang dihasilkan antara 20 sampai 200 kali.



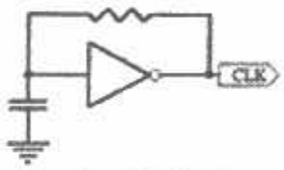
Gambar 2.2 Op-Amp LM 386
Sumber : www.national.com

2.3.3 Komparator Regeneratif (Schmitt Trigger)

Komparator regeneratif merupakan suatu rangkaian yang menunjukan terjadinya histeresis, yaitu suatu perbedaan besar tegangan pindah pada saat tegangan masuk naik dan teganagn masuk turun. Komparator regeneratif ini juga memiliki input tegangan dengan batas maksimum yaitu UTL (upper trigger level)

sebesar 1.8V dan batas minimum yaitu LTL (lower trigger level) sebesar1.0V yang berbentuk gelombang sinusoidal atau gelombang sembarang.

Salah satu kegunaan dari penyulut Schmitt Trigger adalah untuk mengubah tegangan yang berubah lambat menjadi bentuk gelombang keluaran yang berubah cepat bahkan sangat mendadak dan menghasilkan gelombang yang berbentuk persegi dari sinyal masukan yang sembarang atau sinusoidal.



Gambar 2.3 Trigger
Sumber : Sutanto - Rangkaian Elektronika

2.4 SENSOR 2

2.4.1 LDR

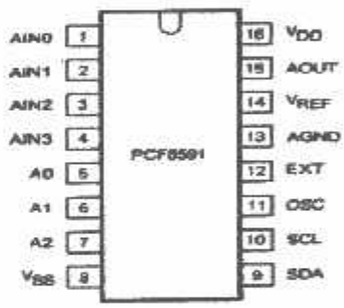
LDR adalah suatu komponen yang peka terhadap cahaya. Di gunakan untuk mengemudikan sebuah rangkaian pada perubahan kekuatan cahaya Prinsip kerjanya yaitu apabila permukaan LDR terkena cahaya maka resistansinya akan berkurang dan apabila permukaannya di tutup, maka resistansinya akan lebih besar. Pencahayaan yang di gunakan adalah lampu LED, di mana LDR di sini di pakai dalam penentu putaran jarum pada jarum penunjuk tekanan darah.

Gambar 2.4 Rangkaian LDR
Sumber : Buku Pelajaran Elektronika Jilid 1, Erlangga, 1982

2.5 ADDA PCF 8591

ADDA merupakan Analog Input Output add-on board untuk 89C51 Development Tools DT51 menggunakan I^2C-bus. DT51 I^2C ADDA digunakan untuk mengubah sinyal analog menjadi digital atau sebaliknya. Spesifikasi yang dimiliki oleh DT51 I^2C ADDA adalah :

1. Kompatibel penuh dengan 89C51 development Tools DT51.
2. Hanya perlu dua jalur kabel untuk interface dengan mikrokontroler.
3. Analog input 4 chanel 8 bit.
4. Digital output 1 chanel 8 bit.
5. Input range tegangan 0 V – 2,5 V.
6. Spesifikasi ADDA PCF 8591 adalah 10mV/bit.



Gambar 2.5 Pin ADDA PCF 8591
Sumber : www.datasheetarchive.com

Dengan rumus :

$$N = \frac{VAin}{2,5} \times 256$$

Tabel 2.1
Fungsi Pin ADDA PCF 8591

SYMBOL	PIN	DESCRIPTION
AIN0	1	analog inputs (A/D converter)
AIN1	2	
AIN2	3	
AIN3	4	
A0	5	hardware address
A1	6	
A2	7	
V_{SS}	8	negative supply voltage
SDA	9	I^2C-bus data input/output
SCL	10	I^2C-bus clock input
OSC	11	oscillator input/output
EXT	12	external/internal switch for oscillator input
AGND	13	analog ground
V_{REF}	14	voltage reference input
AOUT	15	analog output (D/A converter)
V_{DD}	16	positive supply voltage

2.6 Mikrokontroler AT89S51

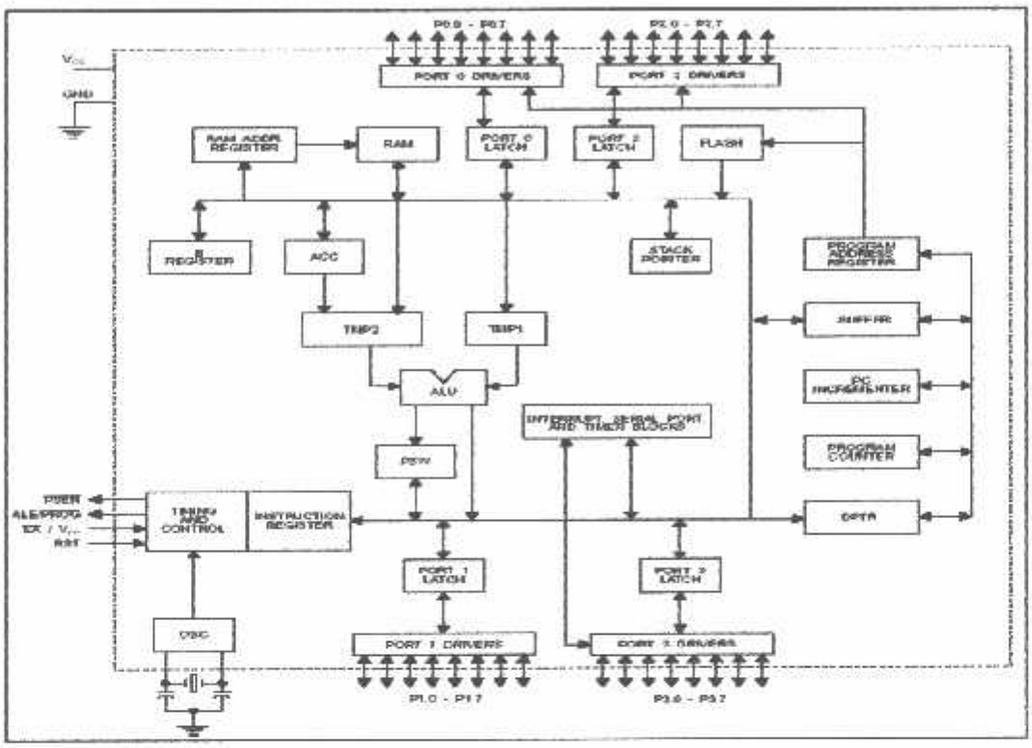
Mikrokontroler AT89S51 merupakan salah satu produk buatan ATMEL.Adapun fitur kelebihan dari mikrokontroler ATMEL AT89S51 antara lain sebagai berikut :

1. 4K byte *Downloadable Flash Memori*
2. 256 byte RAM internal
3. 32 I/O yang dapat dipakai semua
4. 2 buah *Timer / Counter* 16 bit
5. *Programmable* UART (*serial port*)
6. SPI *Serial Interface*
7. *Programmable Wtachdog Timer*
8. *Dual Data Pointer* (DPTR)
9. Frekuensi kerja 0 sampai 24 MHz
10. Tegangan operasi 2,7 sampai 6 volt

Terlihat bahwa mikrokontroler Atmel AT89S51 memiliki banyak fitur yang menguntungkan. Dipakainya *downloadable flash memori* memungkinkan mikrokontroler ini bekerja sendiri tanpa diperlukan tambahan *chip* lainnya. Sementara *flash* memorinya mampu diprogram hingga seribu kali. Hal lain yang menguntungkan adalah sistem pemrograman menjadi lebih sederhana dan tidak

memerlukan rangkaian yang rumit seperti rangkaian untuk memrogram produk Atmel yang lainnya yaitu AT89C51.

Adapun blok diagram dari mikrokontroler AT89S51 adalah sebagai berikut :

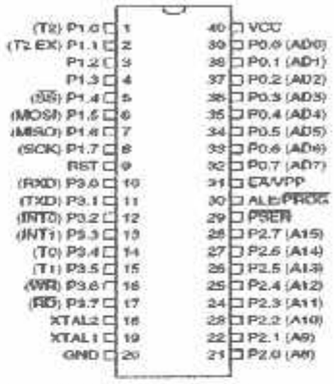


Gambar 2.6 Diagram Blok AT89S51

Sumber: *www.atmel.com*

2.6.1 Fungsi Pin AT89S51

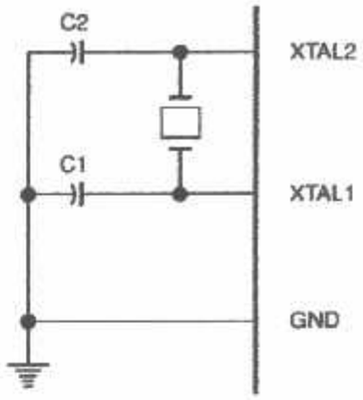
AT89S51 mempunyai pin sebanyak 40 pin dengan konfigurasi sebagai berikut:



Gambar 2.7 Konfigurasi Pin AT89S51
Sumber: *www.atmel.com*

Fungsi kaki-kaki AT89C51 adalah:

- *Port* 1 (Pin 1..8), berfungsi sebagai *port I/O* biasa.
- Pin 9 (*RST*), pulsa transisi dari rendah ke tinggi yang diumpankan ke pin *RST* akan mereset AT89C51. Pin ini dihubungkan dengan rangkaian *power on reset*.
- *Port* 3 (Pin 10..17), *port* paralel 8 bit dua arah yang memiliki fungsi pengganti. Fungsi pengganti meliputi TXD (*Transmit Data*), RXD (*Receive Data*), $\overline{INT0}$(*Interupt 0*), $\overline{INT1}$(*Interupt 1*), T0 (*Timer 0*), T1 (*Timer 1*), $\overline{WR}$ (*Write*), $\overline{RD}$ (*Read*). Apabila fungsi pengganti tidak digunakan, pin-pin ini dapat digunakan sebagai port I/O biasa.
- Pin 18 (XTAL1), merupakan *pin* masukan ke rangkaian osilator internal. Osilator kristal dan sumber osilator luar dapat digunakan.
- Pin 19 (XTAL2), merupakan pin masukan ke rangkaian osilator internal. Pin ini dipakai bila menggunakan osilator kristal.



Gambar 2.8 Rangkaian Pewaktuan dengan Osilator Internal
Sumber: www.atmel.com

- Pin 20 (*Ground*), dihubungkan ke V_{SS} atau *ground*.
- Port 2 (Pin 21..28), port paralel 8 bit dua arah, dapat digunakan sebagai *port I/O* 8 bit biasa dan digunakan untuk mengirim *upper byte* alamat bila digunakan untuk mengakses memori eksternal.
- Pin 29 ($\overline{PSEN}$ /*Program* Store *Enable*), merupakan pengontrol yang digunakan untuk mengakses program memori eksternal masuk ke dalam bus selama proses pemberian/pengambilan instruksi.
- Pin 30 (*ALE*), digunakan untuk menahan (*latch*) alamat memori eksternal selama pelaksanaan instruksi.
- Pin 31 ($\overline{EA}$), bila pin diberikan logika tinggi, maka mikrokontroler akan melaksanakan instruksi dari *ROM/EPROM* internal. Bila diberikan logika rendah, mikrokontroler akan melaksanakan instruksi dari memori program luar.
- *Port* 0 (Pin 32..39), merupakan *port* paralel 8 bit *open drain* dua arah. *Port* 0 dapat digunakan sebagai *port I/O* biasa dan dapat juga

digunakan untuk memultiplek alamat dengan data pada waktu mengakses memori eksternal.

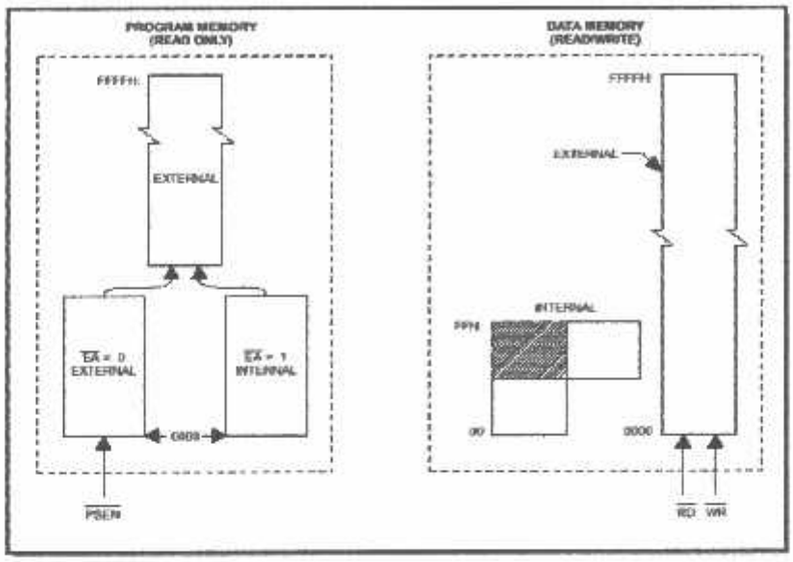
- Pin 40 (VCC), dihubungkan ke VCC (+5 volt).

2.6.2 Organisasi Memori Mikrokontroler AT89S51

Mikrokontroler MCS-51 memiliki pembagian ruang alamat untuk program dan data. Memori data diakses oleh alamat 8 bit, tetapi alamat data 16 bit juga dapat dihasilkan mikrokontroler melalui register DPTR (*Data Pointer Register*). Alamat data dan program yang bisa dialamati oleh mikrokontroler adalah sebesar 64 *kilobyte* yaitu dari alamat 0000_H-$FFFF_H$.

$\overline{PSEN}$ adalah sinyal yang digunakan untuk pembacaan memori program eksternal. Mikrokontroler MCS-51 mempunyai dua buah alternatif untuk pembacaan memori program yaitu internal dan eksternal. Pembacaan memori program eksternal dengan men-set pin $\overline{EA}$ pada logika 0 dan pembacaan memori program internal pin $\overline{EA}$ diset pada logika 1.

Adapun struktur dari memori mikrokontroler MCS 51 ditunjukkan dalam Gambar 2.9 berikut.



Gambar 2.9 Struktur Memori MCS-51.
Sumber: Data Sheets AT89S51

AT89S51 memiliki *RAM* internal 256 *byte* (00_H-$7F_H$) yang dapat digunakan untuk menampung data-data yang diperlukan dalam pemrograman. *RAM* internal tersebut dapat diklasifikasikan sebagai berikut : 80 *byte general purpose* (30_H-$7F_H$), 32 *byte* (00_H – $1F_H$) sebagai *register bank* yang dapat dimanfaatkan seperti *RAM* biasa, dan 16 *byte* (20_H-$2F_H$) *bit addresable*.

Byte Address	Alamat Bit Bit Address							
7F 30	GENERAL PURPOSE RAM (RAM UNTUK SEGALA KEPERLUAN)							
2F	7F	7E	7D	7C	7B	7A	79	78
2E	77	76	75	74	73	72	71	70
2D	6F	6E	6D	6C	6B	6A	69	68
2C	67	66	65	64	63	62	61	60
2B	5F	5E	5D	5C	5B	5A	59	58
2A	57	56	55	54	53	52	51	50
29	4F	4E	4D	4C	4B	4A	49	48
28	47	46	45	44	43	42	41	40
27	3F	3E	3D	3C	3B	3A	39	38
26	37	36	35	34	33	32	31	30
25	2F	2E	2D	2C	2B	2A	29	28
24	27	26	25	24	23	22	21	20
23	1F	1E	1D	1C	1B	1A	19	18
22	17	16	15	14	13	12	11	10
21	0F	0E	0D	0C	0B	0A	9	8
20	7	6	5	4	3	2	1	0
1F 18	REGISTER BANK 3							
17 10	REGISTER BANK 2							
0F 8	REGISTER BANK 1							
7 0	Default Register Bank Untuk R0-R7							

Gambar 2.10 RAM AT89S51
Sumber: *www.atmel.com*

Tabel 2.2
Pengaturan RS0-RS1 *Bank Register*

RS1	RS0	Register Bank Select Bits
0	0	*Bank* 0
0	1	*Bank* 1
1	0	*Bank* 2
1	1	*Bank* 3

2.6.3 SFR (*Special Function Registers*)

Register Fungsi Khusus terletak pada 128 Byte bagian atas memori data internal dan berisi register – register untuk pelayanan latch port, timer, program status word, control peripheral, dan sebagainya. Alamat register fungsi khusus ini ditunjukan pada tabel dibawah ini :

Tabel 2.3 Special Function Register

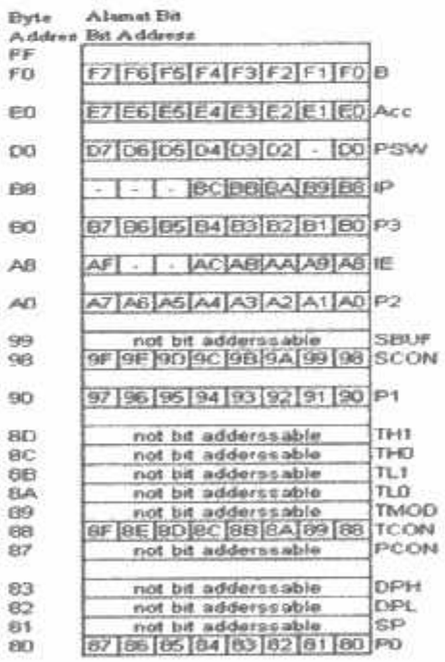
Simbol	Nama Register	Alamat
ACC	Accumulator	E0H
B	Register B	F0H
PSW	Program Status Word	D0H
SP	Stack Pointer	81H
DPL	Bit Rendah	82H
DPH	Bit Tinggi	83H
P0	Port 0	80H
P1	Port 1	90H
P2	Port 2	A0H
P3	Port 3	B0H
IP	Interupt Peiority Control	D8H
IE	Interupt Enable Control	A8H
TMOD	Timer/Counter Mode Control	89H
TCON	Timer/Counter Control	88H
TH0	Timer/Counter 0 High Control	8CH
TL0	Timer/Counter 0 Low Control	8AH
TH1	Timer/Counter 1 High Control	8DH
TL1	Timer/Counter 1 LowControl	8BH
SCON	Serial Control	98H
SBUF	Serial Data Buffer	99H
PCON	Power Control	87H

Sumber : Data Sheet Atmel AT89S51

Beberapa macam register fungsi khusus yang sering digunakan adalah sebagai berikut :

1. *Accumulator* (ACC) merupakan register untuk penambahan dan pengurangan. Untuk mengakses akumulator disederhanakan sebagai A.
2. *Register* B Merupakan register khusus yang berfungsi melayani operasi perkalian dan pembagian.
3. *Stack Pointer* (SP) merupakan register 8 bit yang dapat diletakkan dialamat manapun pada RAM internal.

4. *2 Data Pointer* (DPTR) terdiri atas dua register, yaitu byte untuk tinggi (Data Pointer High, DPH) dan byte rendah (Data Pointer Low, DPL) yang berfungsi untuk mengunci alamat 16 Bit.
5. *Port 0 sampai Port 3* merupakan register yang berfungsi untuk membaca dan mengeluarkan data pada port 0,1,2,3. Masing – masing register ini dapat dialamati per-byte maupun per-bit
6. Control Register terdiri dari register yang mempunyai fungsi kontrol. Untuk mengontrol sistem intrupsi, terdapat dua register khusus, yaitu register IP (*Interupt Priority)* dan Register IE (*Interupt Enable)*. Untuk mengontrol pelayanan timer/counter terdapat register khusus, yaitu register TCON (*Timer/Counter Control)* serta pelayanan port serial menggunakan register SCON (*Serial Port Control).*



Gambar 2.11 Special Function Registers AT89S51
Sumber: *www.atmel.com*

2.6.4 Sistem Interupsi

Mikrokontroler AT89S51 mempunyai 5 buah sumber interupsi yang dapat membangkitkan permintaan interupsi, yaitu INT0, ITN1,T0,T1 dan Port Serial. Saat terjadinya interupsi, maka mikrokontroler secara otomatis akan menuju ke subrutim pada alamat tersebut. Setelah interupsi selesai dikerjakan, mikrokontroler akan mengerjakan program semula. Tiap – tiap sumber interupsi dapat *enable* atau *disable* secara software.

Tingkat prioritas semua sumber dapat diprogram sendiri – sendiri dengan set atau clear bit pada (*Interupt Priority)*. Jika dua permintaan interupsi dengan tingkat prioritas yang berbeda diterima secara bersamaan, permintaan interupsi dengan prioritas yang sama diterima bersamaan, akan dilakukan poling untuk menentukan mana yang akan dilayani.

Tabel 2.4 Alamat Sumber Interupsi

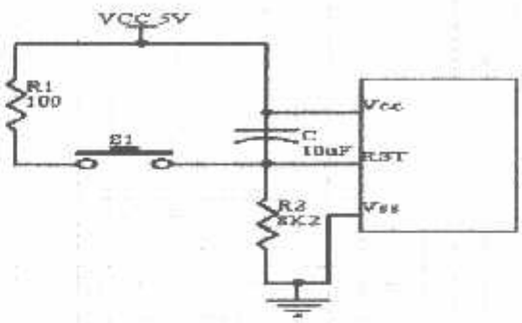
Sumber Interupsi	Alamat Awal
Interupt Luar 0 (INT 0)	03H
Pewaktu / Pencacah 0 (T0)	0BH
Interupt Luar 1(INT 0)	13H
Pewaktu / Pencacah 1 (T1)	01H
Port Serial	23H
Power On Reset	00H

(Sumber : Data Sheet Atmel AT89S51)

2.6.5 Reset

Rangkaian *Power On Reset* diperlukan untuk mereset mikrokontroler secara otomatis setiap catu daya dinyalakan.Ketika catu daya diaktifkan, rangkaian reset akan menahan logika tinggi pada penyemat RST dengan jangka waktu yang ditentukan oleh lamanya pengosongan muatan kapasitor. Untuk

keabsahan reset, logika tinggi harus bertahan lebih lama dari dua siklus mesin ditambah waktu hidup (*start on*) osilator.



Gambar 2.12 Rangkaian *Power On Reset*
Sumber: www.atmel.com

2.7 LCD (*Liquid Crystal Dispplay)*

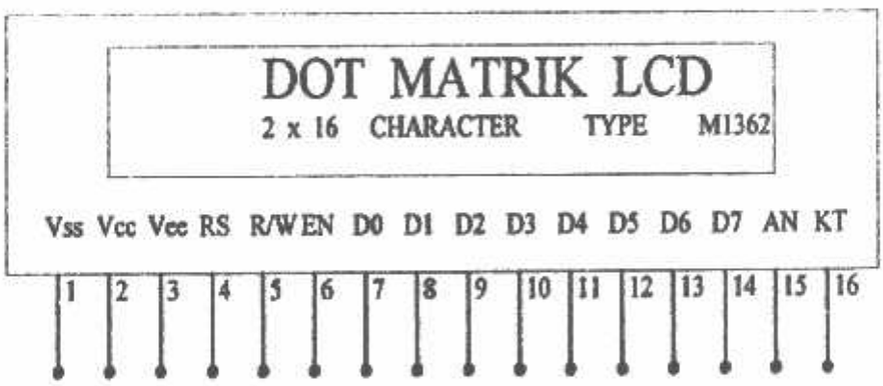
Dalam perancangan ini digunakan LCD (Liquid Crystal Display) tipe M1632 yaitu sebuah LCD dot matrix 16 x 2 baris dengan konsumsi daya rendah. Adapun fitur dari LCD tipe M1632 ini adalah sebagi berikut :

1. 16 Karakter, 2 baris LCD dot matrik
2. Karakter generator ROM untuk 192 karakter
3. Data RAM display maksimum 80 karakter
4. Memungkinkan antarmuka dengan 4 bit datassss atau 8 bit data
5. +5 V single power supply.

Tabel 2.5 Fungsi terminal

Nama Signal	No. Terminal	I/O	Fungsi
DBO–DB3	4	I/O	Data bus 4 bit bawah. Bus ini dipakai untuk membaca atau menulis data. Jika interface data menggunakan 4 bit maka signal ini tidak digunakan.
DB4 - DB7	4	I/O	Data bus 4 bit atas. Bus idata ini dipakai untuk membaca atau menulis.
E	1	I	Enable Signal. Signal untuk mengaktifkan tulis data atau baca data.
R/W	1	I	Signal pemilih mode read atau write 0 : Write 1 : Read
RS	1	I	Register selection signal 0 : Instruction register (read) 1 : Data register (write and read)

Sumber : www.delta-electronic.com



Gambar 2.13 Pin LCD

Sumber : www.delta-electronic.com

BAB III

METODOLOGI PENELITIAN

3.1 Studi Literatur

Tekanan darah adalah menunjukkan keadaan di mana tekanan yang dikenakan oleh darah pada pembuluh arteri ketika darah dipompa oleh jantung ke seluruh anggota tubuh. Tekanan darah dapat dilihat dengan mengambil dua ukuran dan biasanya ditunjukkan dengan angka seperti berikut - 120 /80 mmHg. Angka 120 menunjukkan tekanan pada pembuluh arteri ketika jantung berkontraksi yang di sebut dengan tekanan sistolik. Angka 80 menunjukkan tekanan ketika jantung sedang berelaksasi. Yang disebut dengan tekanan diastolik. Dari survey yang telah di lakukan di dapat Tips pengukuran tekanan darah yang benar :

1. Duduk yang nyaman dan letakkan lengan Anda dekat dan sejajar dengan posisi jantung.
2. Tarik nafas dalam-dalam 5 sampai 6 kali sebelum pengukuran.
3. Jangan bergerak atau bicara selama pengukuran.
4. Istirahatkan 5 sampai 10 menit antara pengukuran pertama dan selanjutnya.

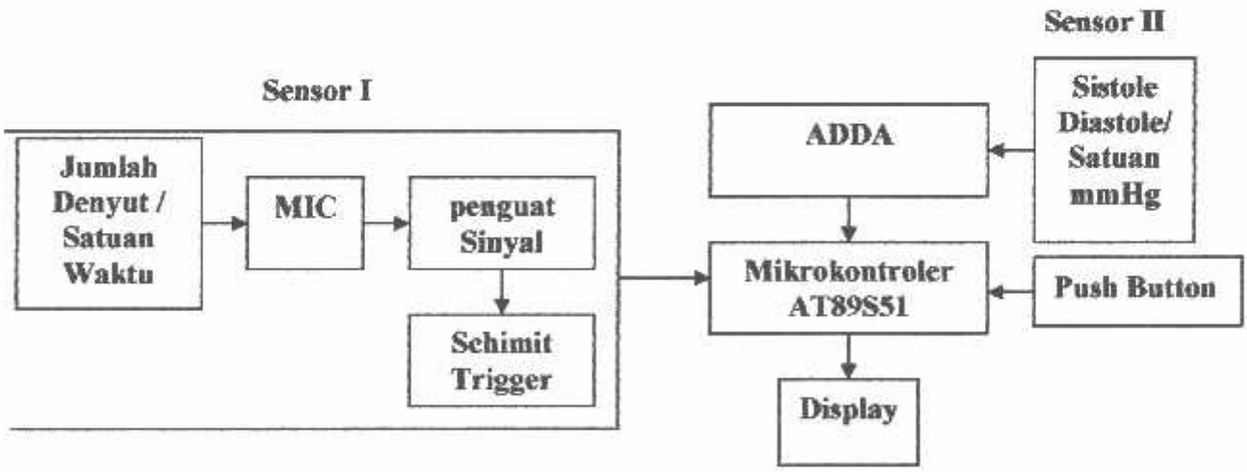
Table 3.1 Klasifikasi Tekanan Darah Orang Dewasa

Kategori	Tekanan Darah Sistolik	Tekanan Darah Diastolik
Rendah	Di bawah 99 mmHg	Di bawah 69 mmhg
Normal Minimal	100 – 119 mm Hg	70 – 79 mm Hg
Normal Ideal	120 – 139 mm Hg	80 – 89 mm Hg
Normal Maximal	140 – 149 mm Hg	90 – 99 mm Hg
Stadium 1 (Hipertensi Ringan)	150 – 159 mm Hg	100 – 109 mmhg
Stadium 2 (Hipertensi Sedang)	160 – 179 mm Hg	110 – 119 mmhg
Stadium 3 (Hipertensi Berat)	180 – 209 mm Hg	120 – 129 mmhg
Stadium 4 (Hipertensi Maligna)	210 mm Hg atau lebih	130 mmhg atau lebih

Sumber : HKKI (Himpunan Kimia Klinik Indonesia) 2007

3.2 Perencanaan dan pembuatan alat

Perancangan dan pembuatan alat pengukur tekanan darah dengan tampilan LCD berbasis mikrokontroler AT89S51. Adapun blok diagram alat ini adalah sebagai berikut :

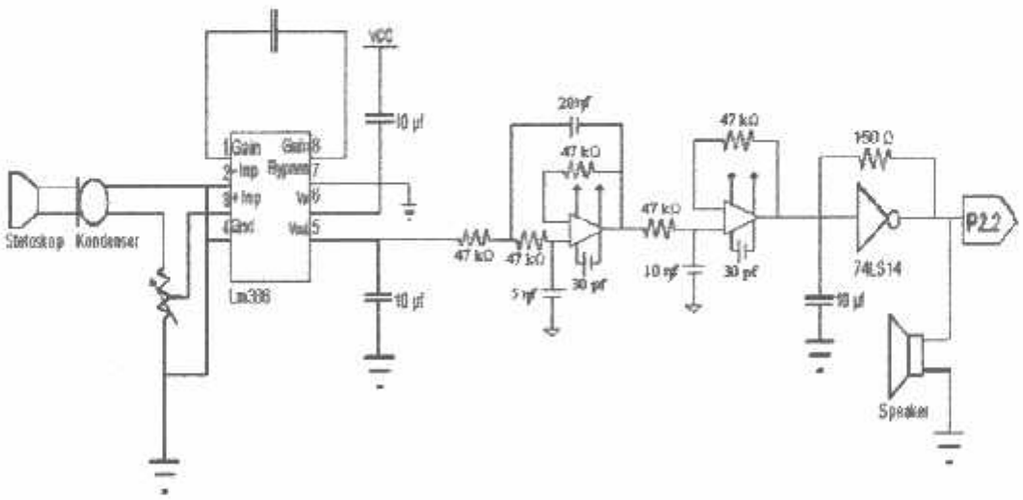


Gambar 3.1 Blok Diagram

Dari blok diagram diatas dapat dijelaskan dari masing – masing blok sebagai berikut:

1. Sensor I

Sensor atau inputan ini berfungsi untuk mendeteksi jumlah denyut persatuan waktu, diamana digunakan stetoskop sebagai pendeteksinya. Selanjutnya Mic disini berupa codensor yang dipasang pada selang stetoskop, dimana stetoskop akan menerima suara yang berupa suara detak jantung pada pengukuran denyut jantung dan detak nadi pada pengukuran tekanan darah. Output dari kondensor berupa tegangan. Amplifier merupakan suatu penguat yang menguatkan outputan kondensor, yang dimana hasil dari penguatan tersebut dapat diterima oleh mikrokontroler melalui proses pentriggeran terlebih dahulu dengan range tegangan 0 - 5 V.



Gambar 3.2 rangkaian sensor 1

Untuk perhitungan low pass :

R1 = R2 = Rf = 47 KΩ

$C1 = \frac{1}{2}C3$

C2 = 2 C3

$C3 = \frac{1}{\omega_c R}$

$C3 = \frac{1}{2 \times 3.14 \times 350 \times 47000}$

C3 = 10 Df

C2 = 20 Df

C1 = 5 Df

Untuk Perhitungan Scihmit Trigger :

T = 100 µs C = 10 µf

$T = \frac{1}{1.1 \times 2\pi C}$

$100 = \frac{1}{1.1 \times 2 \times 3.14 \times R \times 10^{-5}}$

$R = \frac{1}{1.1 \times 2 \times 3.14 \times 100 \times 10^{-5}}$

$R = \frac{1}{0.006908}$

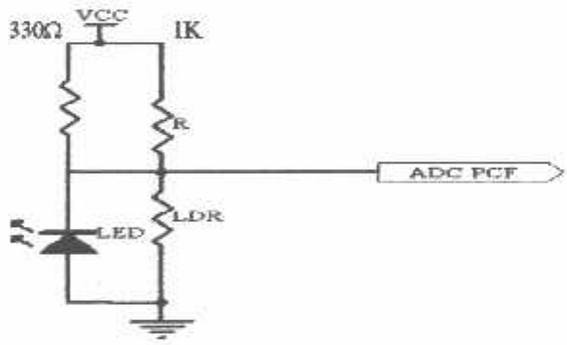
R = 144.7

R =150 Ω

2. Sensor II

Sensor yang digunakan adalah LDR, yaitu sebuah tranducer yang mengubah intensitas cahaya menjadi besaran listrik dengan perubahan resistansinya. Prinsip kerjanya, apabila permukaan LDR terkena cahaya maka resistasinya akan berkurang dan apabila permukaan ditutup maka resistansinya akan lebih besar.

Pencahayaan yang digunakan adalah lampu led. Dimana LDR disini dipakai dalam penentuan putaran jarum pada penunjuk jarum penunjuk tekanan darah. Setelah itu akan dihubungkan dengan ADDA PCF 8591 yang berfungsi untuk mengubah sinyal analog menjadi digital yang akan diproses selanjutnya pada mikrokontroler.



Gambar 3.3 Rangkaian LDR

3. Mikrokontroler AT89S51

AT89S51 disini berfungsi sebagai pengontrol semua sistem yang ada pada pembuatan alat termometer badan ini.

4. Push Button

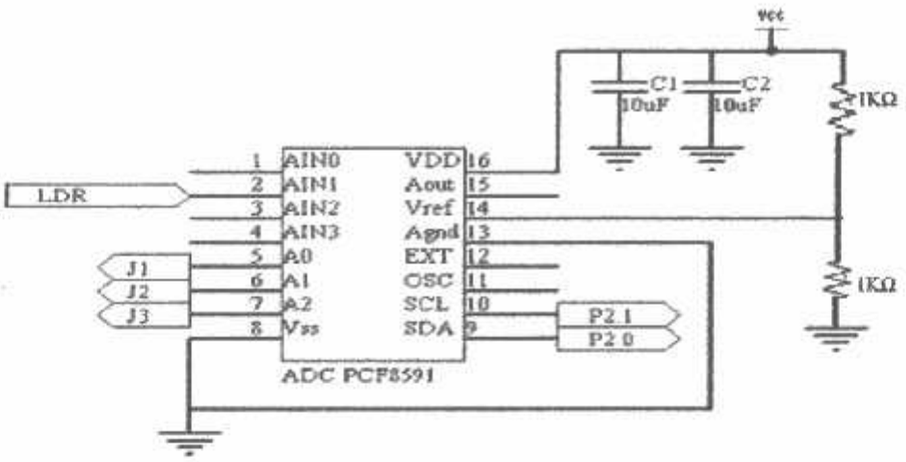
Push button berfungsi untuk memilih sensor mana yang akan diaktifkan atau bekerja.

5. Display

Display yang digunakan disini adalah LCD tipe M1632 yaitu sebuah LCD dot matrix 16 x 2 baris dengan konsumsi daya rendah. Dimana LCD disini berfungsi sebagai penampil data yang kita peroleh dalam mengukur tekanan darah seseorang.

3.3 Perencanaan Rangkaian ADDA PCF8591

Agar nilai yang dikeluarkan oleh sensor LDR dapat dibaca oleh mikrokontroler AT89S51, nilai tegangan tersebut harus diubah menjadi bentuk data digital 8 bit. Untuk itu digunakan konverter analog ke digital atau digital to analog (ADDA). Type yang dipakai dalam perancangan ini adalah type ADDA PCF8591 yang merupakan ADC dengan empat inputan analog yang dimultiplex menjadi data 8 bit digital.



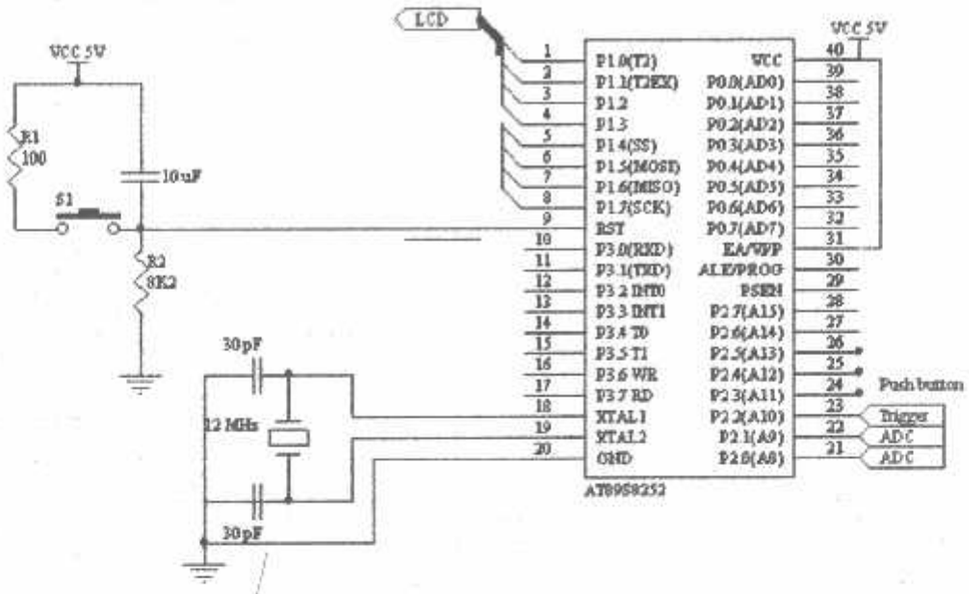
Gambar 3.4 Rangkaian ADDA PCF8591
Sumber : *www.datasheetarchive.com*

3.4 Mikrokontroler AT89S51

Mikrokontroler AT89S51 adalah suatu chip IC yang terdiri dari 40 pin, dalam perancangan alat ini pin – pin yang digunakan adalah sebagai berikut :

1. Port 2.0 sampai 2.1 merupakan port yang digunakan sebagai data input dari ADDA PCF8591.
2. Port 1.0 sampai port 1.3 merupakan port yang digunakan oleh LCD.
3. Port 2.2 merupakan pin inputan dari data trigger.
4. Port 2.4merupakan push button.
5. Pin 9 (Reset), reset aktif tinggi terhubung dengan rangkaian power on reset dan jika diaktifkan mereset mikrokontroler AT89S51.

   $$VR2 = \frac{R2xVcc}{R1+R2} = 4{,}94 \text{ volt.}$$ (Pada saat saklar ditekan maka akan high).
6. Pin 20 digunakn sebagai ground.
7. Pin 40 digunakan sebagai VCC sumber.

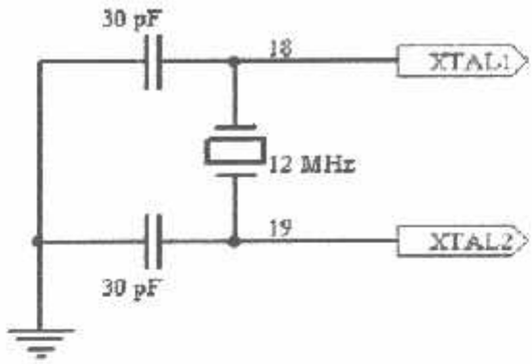


Gambar 3.5 Rangkaian Mikrokontroler AT89S51

3.5 Sistem Pewaktuan Mikrokontroler

Kecepatan proses yang dilakukan oleh mikrokontroler ditentukan oleh sumber *clock* (pewaktuan) yang mengendalikan mikrokontroler tersebut. Sistem yang dirancang ini akan menggunakan osilator internal yang sudah tersedia di dalam chip mikrokontroler. Untuk menentukan frekuensi osilatornya cukup dengan cara menghubungkan kristal pada pin XTAL1 dan XTAL2 serta dua buah kapasitor ke ground. Besar kapasitansinya dengan spesifikasi pada lembar data mikrokontroler yaitu 30 pF.

Pemilihan besar frekuensi kristal disesuaikan dengan pemilihan kecepatan yang diharapkan untuk transfer data melalui pin *serial interface* mikrokontroler tersebut. Dengan memakai kristal 11,059 MHz, maka satu siklus mesin membutuhkan waktu selama 1,08 µdetik atau $\frac{1}{11{,}059}$ x12 periode.



Gambar 3.6 Rangkaian Pewaktuan
Sumber : *www.atmel.com*

3.6 Perencanaan Sensor Sistole Diastole Per Satuan Waktu

Sensor ini merupakan sutau rangkaian yang digunakan untuk mengukur tekanan darah. Prinsip kerja dari alat ini adalah untuk menghasilkan tegangan, dimana tegangan yang dihasilkan tergantung dari besarnya resistor pada LDR.

Dengan rumus $Vout = \frac{R\ bottom}{R\ bottom + R\ top} \times Vin$

3.7 Perencanaan Sensor Jumlah Denyut Per Satuan Waktu

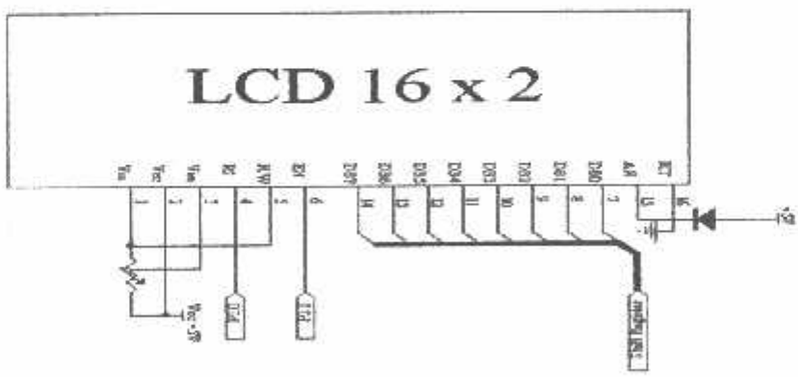
Dalam perencanaan tranduser ini dirancangn suatu alat yang dapat mendeteksi denyut jantung dan detak nadi, dimana semuanya itu menjadi satu kesatuan dalam perancangan saat ini. Pendeteksi suara yang digunakan adalah stetoskop, dari stetoskop itu akan didapatkan suara detak nadi dan denyut jantung yang berupa frekuensi suara, dari outputan stetoskop akan dimasukan atau sebagai inputan bagi kondensor, kondensor akan merubah menjadikan tegangan, setelah itu baru dikuatkan dengan penguat LM386 yang penguatanya bisa mencapai

sampai 200 kali, hal ini dilakukan agar komparator regeneratif (Schmitt Trigger) dapat membuat pulsa atau clock.

3.8 Perencanaan LCD

Dalam aplikasi ini menggunakan sebuah layar LCD (*Liquid Crystal Display*)yaitu jenis M1632 yang merupakan LCD dua baris dengan setiap barisnya terdiri atas 16 karakter. Masukan yang diperlukan untuk mengendalikan modul ini berupa bus data yang masih termultiplek dengan bus alamat. Sementara pengendalian dot metrik LCD dilakukan secra internal oleh kontroler yang sudah terpasang pada modul LCD.

Rangkaian display ditunjukkan dalam Gambar 3.9. Saluran data DB_0 – DB_7 dihubungkan pada pin shift register. Sedangkan penyemat Enable dan RS dihubngkan pada port 1.0 dan port 1.1 mikrokontroler AT89S51. Penyemat V_{ee} dihubungkan pada potensiometer 1 KΩ, untuk mengatur kecerahan LCD.



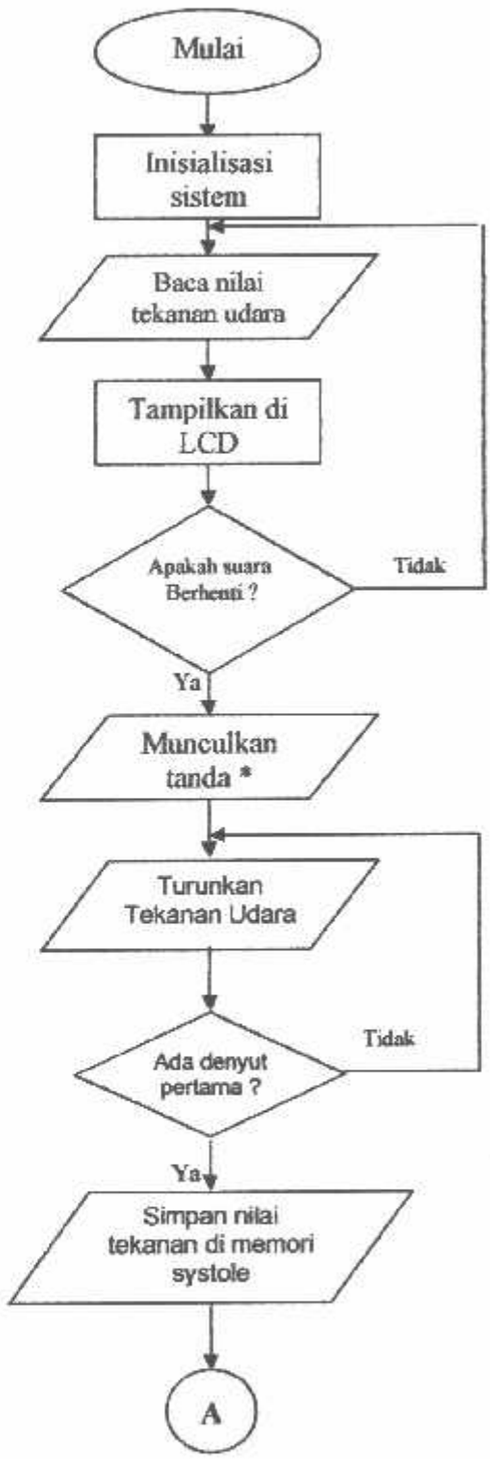
Gambar 3.7 Rangkaian LCD

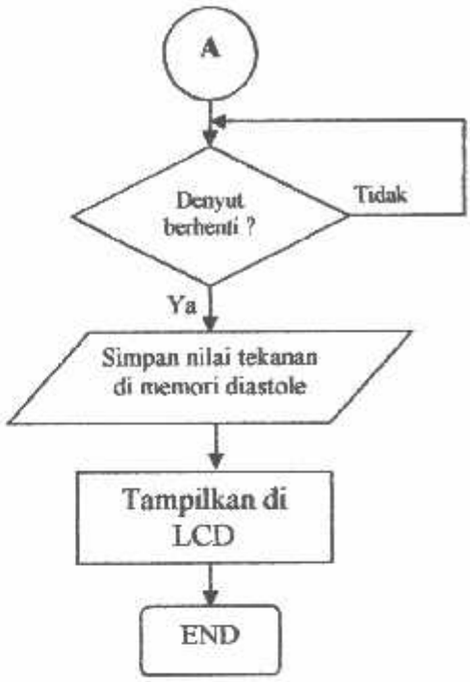
Untuk menjalankan peralatan yang dirancang diperlukan perangkat lunak (software) yang disusun dengan flowchart dan ditulis dengan menggunakan bahasa assembler.

Program adalah kumpulan dari instruksi untuk mengendalikan atau mengoprasikan sistem perangkat keras (Hardware). Adapun software-nya adalah sebagai berikut :

1. Membuat diagram alir (flowchart) dari program yang akan dibuat.
2. Mengubah diagram aliran tersebut ke dalam bahasa pemrograman.
3. Mengkomplikasikan program yang telah dibuat ke dalam memori, sampai menghasilkan program yang paling sesuai.
4. Kemudian memasukkan program yang telah selesai, berikut ini merupakan flowchart dari alat pengukur tekanan darah dengan tampilan LCD berbasis mikrokontroler AT89S51.

FLOW CHART


Mulai
Inisialisasi sistem
Baca nilai tekanan udara
Tampilkan di LCD
Apakah suara Berhenti ?
Tidak
Ya
Munculkan tanda *
Turunkan Tekanan Udara
Ada denyut pertama ?
Tidak
Ya
Simpan nilai tekanan di memori systole
A



Gambar 3.8 Diagram Alir Program

3.9 Pengujian sensor suara

3.9.1 Tujuan

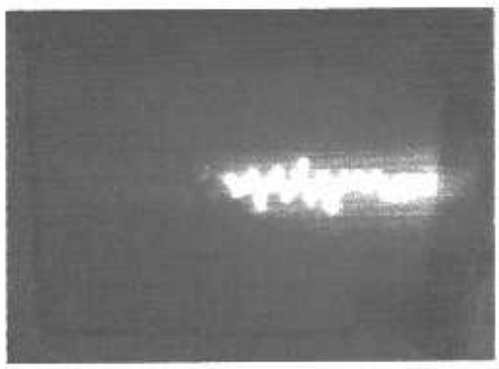
Pengujian senor ini bertujuan untuk mengetahui apakah sensor sudah bekerja sesuai dengan yang diharapkan.

3.9.2 Peralatan yang di gunakan

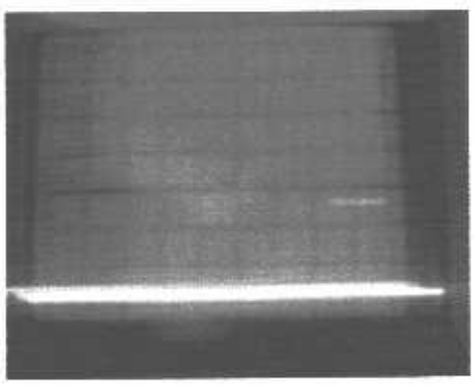
1. Power Suply
2. Osilator

3.9.3 Hasil Pengujian Sensor Suara

Dari pengujian sensor di dapatkan hasil sebagai berikut :



Gambar 3.9 Hasil Pengujian sensor suara analog Pada Osiloscope Dengan Volt/DIV adalah V/DIV



Gambar 3.10 Hasil Pengujian Sensor Suara Digital Pada Osiloscipe Dengan Volt/DIV adalah V/DIV

3.9.4 Analisa Pengujian

Sinyal suara yang di terima kondensor dari stetoskope adalah frekwensi rendah antara 0 – 4000 Hz. karena out putan kondensor sangat kecil sekali sekitar 0.015 volt, maka di kuatkan oleh Op – Amp lm 386 sebesar 200 kali maka di dapatkan tegangan sebesar 3 volt. hal ini di lakukan agar dapat memenuhi batasan schimit trigger antara 0 – 3 volt agar dapat di baca oleh schimit trigger. Out putan dari schimit trigger berupa high and low yang kemudian dapat di olah oleh mikrokontroler.

BAB IV

PENGUJIAN ALAT DAN ANALISIS

4.1. Pengujian Sistem Secara Keseluruhan

Bab ini membahas tentang pengujian dan analisis alat yang telah dibuat. Secara umum, pengujian ini bertujuan untuk mengetahui apakah sistem alat ukur yang di buat sudah sesuai dengan perencanaan awal yang telah ditetapkan.

4.1.1. Peralatan Yang Digunakan

1. Power supplay
2. Stetoskop
3. Rangkaian lengkap alat pengukur tekanan darah berbasis mikrokontroler AT89S51.

4.1.2. Prosedur Pengujian

1. Alat – alat dirangkai lengkap seperti pada gambar rangkain total
2. Catu daya tegangan 5 Volt.
3. Membuat program yang di gunakan dalam pengujian mikrokontroler

4.1.3. Hasil Pengujian

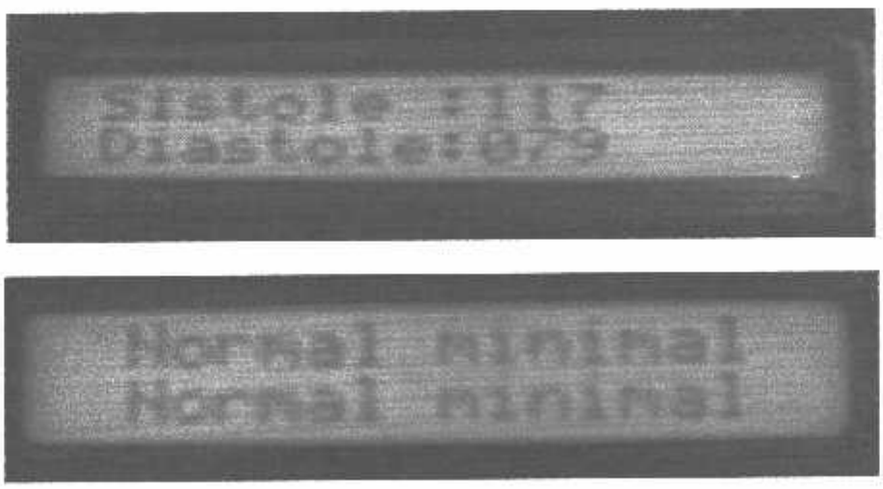
Dari pengujian yang dilakukan akan didapatkan nilai – nilai pengukuran yang sangat sesuai dengan apa yang diharapkan. Yang pada akhirnya nilai yang

diperoleh adalah dalam bentuk digital. Hal ini membuktikan proses pengukuran dapat berjalan dengan baik. Walaupun terkadang ada error yang terjadi.

4.2. Pengujian Alat Keseluruhan Pada Pengukuran Tekanan Darah

Pengujian alat ini adalah pengujian yang sangat sulit dilakukan, Karena pada kondisi ruangan yang tidak tenang atau ramai, akan menimbulkan error pada pengukuran, karena alat ini merupakan suatu pengembangan dari teori – teori sebelumnya. Range yang didapat dalam pengujian alat ini sangatlah berpariasi, tergantung umur, faktor keturunan, dan kebiasan hidup.

Pengukuran biasanya dilakukan 1 sampai 2 kali. Hal ini dilakuakan agar mendapatkan nilai – nilai yang mendekati kondisi si pasien. Dan nilai yang dipakai adalah nilai yang terendah. Hasil pengujian alat ini dapat dilihat pada gambar 4.1 dibawah ini.



Gambar 4.1 Hasil Pengujian Alat Pengukur Tekanan Darah.

4.3. Data Percobaan Alat

Data percobaan alat di bawah ini menunjukkan perbandingan antara alat pengukur tekanan darah digital dengan alat pengukur tekanan darah analog. Data di bawah ini telah di periksa dan di setujui oleh pihak yang berwenang. Data percobaan di ambil dari beberapa orang, antara lain sebagai berikut :

Tabel 4.1
Data percobaan alat

Nama	Umur (Thn)	Alat pengukur tekanan darah digital		Alat pengukur tekanan darah analog		Ket
		Systole (mmhg)	Diastole (mmhg)	Systole (mmhg)	Diastole (mmhg)	
Deny S	22	142	92	140	90	Normal max
Okta	22	96	65	90	60	Rendah
Rohmat	23	124	85	120	80	Normal ideal
Umar	24	113	76	110	70	Normal min
Ristanto	24	121	83	120	80	Normal ideal
Himawan	23	124	82	120	80	Normal ideal

4.4. Analisa Pengujian

Dari percobaan di atas, dapat di analisa bahwa alat ini telah menghasilkan out putan yang sesuai dengan yang di inginkan. Keterangan yang muncul telah sesuai dengan nilai systole dan diastole, sesuai dengan program yang ada. Percobaan di atas juga memperlihatkan perbandingan antara alat pengukur tekanan darah secara digital dengan alat pengukur tekanan darah secara analog di mana nilai – nilai yang di hasilkan oleh keduanya tidak memperlihatkan perbedaan yang begitu jauh. Alat ini juga mempunyai kelebihan dapat mendeteksi

dengan nilai keluaran yang lebih teliti di bandingkan alat pengukur tekanan darah secara analog.

Dari pengujian yang dilakukan sebanyak 6 kali pada pengukuran tekanan darah didapatkan persentase kesalahan sebagai berikut :

$$\text{Kesalahan} = \left(\frac{data\ pengukuran - data\ pengujian}{data\ pengukuran} \right) \times 100\ \%$$

Tabel 4.2
Data Perhitungan Persentase Kesalahan

NO	HASIL PENGUKURAN TEKANAN DARAH DIGITAL		HASIL PENGUJIAN TEKANAN DARAH ANALOG		ERROR	
	SISTOLE (mm Hg)	DIASTOLE (mm Hg)	SISTOLE (mm Hg)	DIASTOLE (mm Hg)	SISTOLE (%)	DIASTOLE (%)
1	142	92	140	90	0.01 %	0.02 %
2	96	65	90	60	0.06 %	0.08 %
3	124	85	120	80	0.03 %	0.06 %
4	113	76	110	70	0.02 %	0.07 %
5	121	83	120	80	0.01 %	0.03 %
6	124	82	120	80	0.03 %	0.03 %

Sedangkan untuk menentukan kesalahan rata – rata pada sistole dan diastole adalah sebagai berikut : $\frac{jumlah\ kesalahan\ rata - rata}{banyaknya\ sampel}$

kesalahan rata – rata pada sistole adalah $= \frac{0.16\%}{6} = 0{,}02\ \%$

Sedangkan kesalahan rata – rata pada tekanan darah diastole adalah : $\frac{0.29\%}{6} =$ 0,048 %

Spesifikasi Alat

No	Nama Alat	Banyak (x)	Harga (Rp)	Jumlah (Rp)
1	Minimum Sistem MCS51	1	60.000	60.000
2	MK 89S51	1	15.000	15.000
3	LCD	1	100.000	100.000
4	Keypad	1	35.000	35.000
5	Kondensor Mic	1	1000	1000
6	Pre Amp	1	4.500	4.500
7	Turbo Bas	1	10.000	10.000
8	Pengukur tensi + stetoskop	1	75.000	75.000
9	Modul ADDA	1	80.000	80.000
10	Filter	1	45.000	45.000
11	Schimit trigger	1	10.000	10.000
12	Power Supply (Adaptor 1A)	1	17.000	17.000
Jumlah				452.500

BAB V

PENUTUP

5.1 Kesimpulan

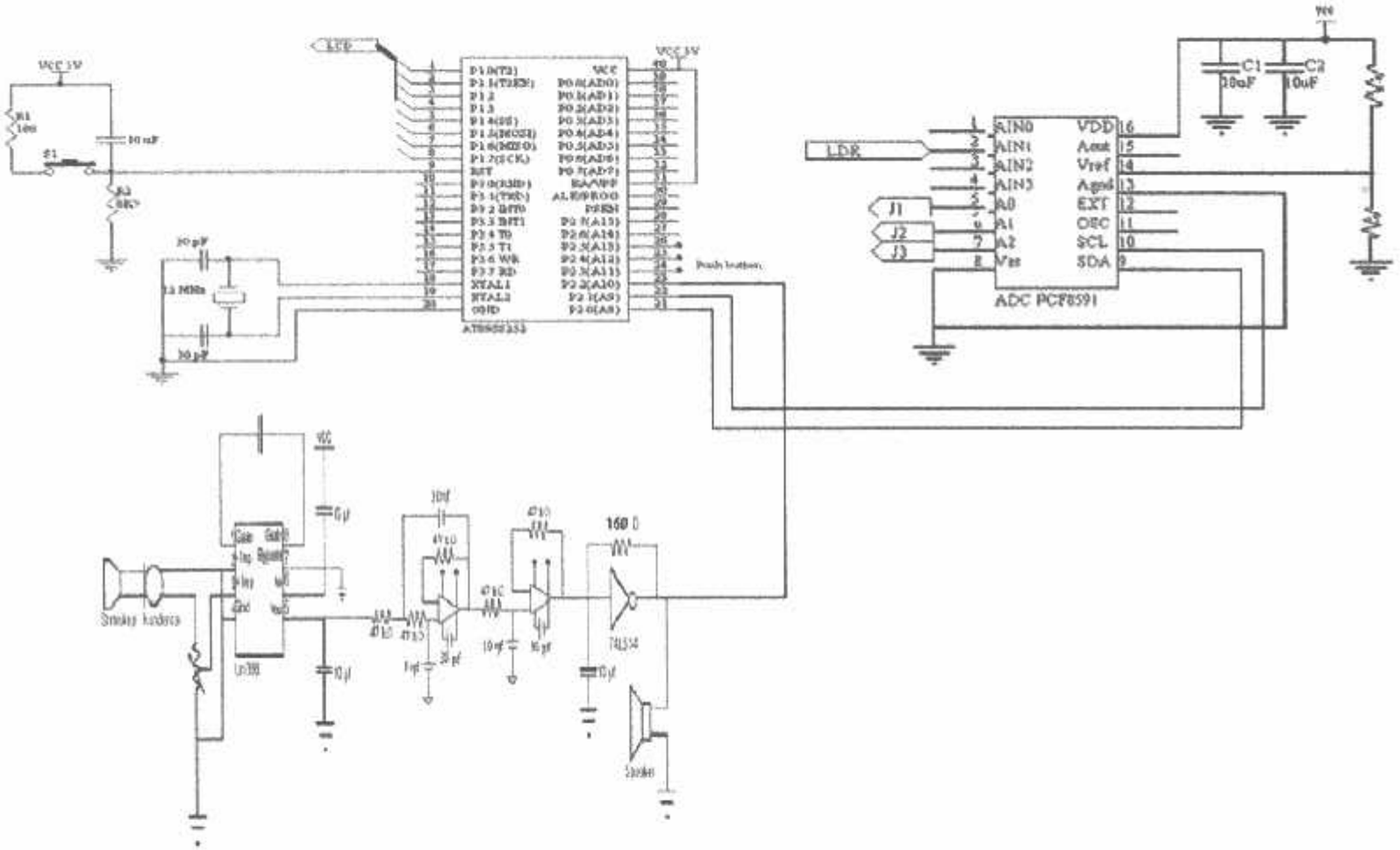
Setelah melakukan perencanaan dan pembuatan Alat Penghitung Tekanan darah secara digital berbasis Mikrokontroler AT89S51 maka pada bab ini diberikan kesimpulan :

1. Pembuatan simulasi alat pengukur tekanan darah digital ini berpedoman pada alat pengukur tekanan darah analog yang telah ada, dengan mengetahui cara kerja dari pengukur tekanan darah analog maka dapat di konversikan kc dalam alat pengukur tekanan darah digital dengan program yang ada.
2. Penggunaan mikrokontroler ATMEL AT89S51 untuk mengontrol semua system, di gunakan bahasa pemrograman yaitu bahasa assembly.
3. Perencanaan sensor suara untuk mendeteksi denyut jantung menggunakan kondensor dengan out putannya sebesar 0.015 volt kemudian di kuatkan oleh Op – Amp sebesar 200 kali sehingga menjadi 3 volt agar dapat di terima oleh mikrokontrler setelah melalui proses pentrigeran.

5.2 Saran

Meskipun dari hasil pengujian dan analisa terhadap performansi alat sudah mencapai kedaan yang diharakan, namun masih banyak perbaikan atau pengembangan yang dapat dilakuan untuk lebih meningkatkan lagi performansi alat. Beberapa saran yang kiranya dapat meningkatkan performansi alat antara lain:

1. Untuk lebih mempermudah user dalam pengoprasian alat ini maka perlu untuk ditambahkan suatu komponen atau alat yang lebih peka didalam mendeteksi adanya denyut.
2. Disamping itu juga sebaiknya dalam pengoprasian alat ini ditambahkan pemompa otomatis dari cuff yang dipakai.



Gambar Rangkaian Keseluruhan

DAFTAR PUSTAKA

1. Data Sheet www.archive.com
2. Data Sheet www.atmel.com
3. Data Sheet www.delta-electronic.com
4. Data Sheet www.national.com
5. HKKI , 2007
6. http://www.nhlbi.nih.gov//cml
7. Moh. Ibnu Malik, ST, *Belajar Mikrokontroler ATMEL AT89S51*, edisi pertama, Yogyakarta, Gava Media 2003.
8. Winarto Andik, Laporan Tugas Akhir.2004

INSTITUT TEKNOLOGI NASIONAL MALANG
FAKULTAS TENIK INDUSTRI
JURUSAN TEKNIK ENERGI LISTRIK DIII

Lembar Asistensi Bimbungan Tugas Akhir

Nama : Oktavianto
NIM : 0352010
Waktu Bimbingan :12/12/2006 s/d 12/04/2007
Judul : Perencanaan Dan Pembuatan Alat Pengukur Tekanan Darah Digital Berbasis MC AT89S51

No	Tanggal	Materi	Paraf
1	5/1 '07	BAB I, BAB II, BAB III	diperbaiki
2	26/1 '07	Perbaiki latar belakang dan BAB III	
3	18/2 07	Tambahkan Gambar dan flow alat	
4	27/2 07	BAB II tinjauan kondensor? Pustaka. BAB III diperbaiki?	
5	6/3 07	BAB IV, BAB III lengkap	
6	7/3 07	BAB IV spesifikasi Alat Perincian biaya	
7		Abstrak. ACC maju	
8			

Mengetahui
Dosen Pembimbing

(Bambang Prio H, ST, MT)

INSTITUT TEKNOLOGI NASIONAL MALANG
FAKULTAS TENIK INDUSTRI
JURUSAN TEKNIK ENERGI LISTRIK DIII
KONSENTRASI TEKNIK ENERGI LISTRIK

LEMBAR PERBAIKAN TUGAS AKHIR

Nama : Oktavianto
NIM : 0352010
JURUSAN : T.ELEKTRO D III
KONSENTRASI : T.ENERGI LISTRIK
HARI / TANGGAL : RABU, 21 MARET 2007

NO	Materi Perbaikan	Paraf
1	Rumus yang di gunakan di perbaiki untuk perhitungannya, sesuai dengan alat yang ada	
2	Perbaiki untuk spesifikasi alat	
3	Rangkaian keseluruhan di cantumkan dan harus sesuai dengan alat yang di buat	

Telah Diperiksa dan Disetujui

Penguji I

(Ir. Choirul Saleh, MT)

Penguji II

(Ir. Eko Nurcahyo)

Mengetahui
Dosen Pembimbing

(Bambang Prio H, ST, MT)

INSTITUT TEKNOLOGI NASIONAL
Jl. Bendungan Sigura-gura No. 2
MALANG

LEMBAR PERBAIKAN TUGAS AKHIR

NAMA : NOVINDO OKTAVIANTO
NIM : 03.2010
JURUSAN : TEKNIK ELKTRO D- III
PROGRAM STUDI : ENERGI LISTRIK / ELEKTRONIKA *)
HARI / TANGGAL : .....

No.	MATERI PERBAIKAN
	→ Rangkaian keseluruhan di cantumkan dan harus sesuai dg alat yang dibuat.

DOSEN PENGUJI

(.....)

INSTITUT TEKNOLOGI NASIONAL
Jl. Bendungan Sigura-gura No. 2
MALANG

LEMBAR PERBAIKAN TUGAS AKHIR

NAMA : Oktavianto
N I M : 0352010
JURUSAN : TEKNIK ELKTRO D- III
PROGRAM STUDI : ENERGI LISTRIK / ELEKTRONIKA *)
HARI / TANGGAL : RABU/21-03-2007

No.	MATERI PERBAIKAN
1.	Ramur yg digunakan di perbaiki utk perbaikan tugasnya.
	Sesuaikan yg alat-yg ada.
2.	Perbaiki untuk spesifikasi alat

DOSEN PENGUJI

( )

INSTITUT TEKNOLOGI NASIONAL MALANG
FAKULTAS TENIK INDUSTRI
JURUSAN TEKNIK ENERGI LISTRIK DIII
KONSENTRASI TEKNIK ENERGI LISTRIK

BERITA ACARA UJIAN TUGAS AKHIR

FAKULTAS TEKNOLOGI INDUSTRI

Nama	: Oktavianto
NIM	: 0352010
JURUSAN	: T.ELEKTRO D III
KONSENTRASI	: T.ENERGI LISTRIK
Judul TA	: Perencanaan Dan Pembuatan Alat Pengukur Tekanan Darah Digital Berbasis MK 89S51

Di Pertahankan Di Hadapan Team Penguji Tugas Akhir Jenjang Diploma (D III)

Pada :

Hari : RABU

Tanggal : 21 Maret 2007

Dengan Nilai : 80,68 (A)

Panitia Ujian tugas Akhir

Ketua

(Ir. Mochtar Asroni, MSME)

Sekretaris

(Ir. H.Choirul Saleh, MT)

Anggota Penguji

Pertama

(Ir. H.Choirul Saleh, MT)

Kedua

(Ir. Eko Nurcahyo)

LAMPIRAN

Foto alat tampak dari luar

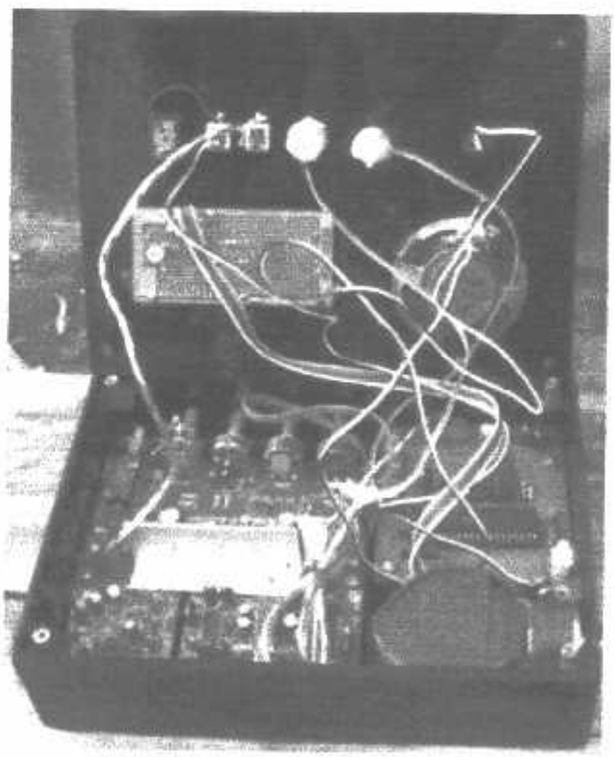


Foto alat tampak dari dalam

Data percobaan alat

Data percobaan di bawah ini menunjukkan perbandingan alat antara tensi digital dengan tensi analog yang telah di periksa dan di setujui oleh pihak yang berwenang dalam bidang kesehatan (Dr. Herlina). Data percobaan di ambil dari beberapa orang, antara lain sebagai berikut :

Nama	Umur (Thn)	Alat pengukur tekanan darah digital		Alat pengukur tekanan darah analog		Ket
		Systole (mmhg)	Diastole (mmhg)	Systole (mmhg)	Diastole (mmhg)	
Deny S	22	142	92	140	90	normal max
Okta	22	96	65	90	60	Rendah
Rohmat	23	124	85	120	80	normal ideal
Umar	24	113	76	110	70	normal min
Ristanto	24	121	83	120	80	normal ideal
Himawan	23	124	82	120	80	normal ideal

Mengetahui

Dr. Herlina

dr. HERLINA

Sip.446/DU/SIP-21/422-202/2004

PERTEMUAN ILMIAH TAHUNAN NASIONAL IV
PERHIMPUNAN DOKTER SPESIALIS PATOLOGI KLINIK INDONESIA
KONFERENSI KERJA X
HIMPUNAN KIMIA KLINIK INDONESIA

KLASIFIKASI TEKANAN DARAH

Kategori	Systolik (mm Hg)	Diastolik (mm Hg)
Rendah	< 99	< 69
Normal Minimal	100 – 119	70 – 79
Normal Ideal	120 – 139	80 – 89
Normal Maximal	140 – 149	90 – 99
HIPERTENSI		
Tahap I	150 – 159	100 – 109
Tahap II	160 – 179	110 – 119
Tahap III	180 – 209	120 – 129
Tahap IV	> 210	> 130

Spesifikasi Alat

Nama	: Alat Pengukur Tekanan Darah Digital Berbasis MK AT89S51
Catu Daya	: 12 V
Frekwensi	: > 300 Hz
Temperatur Range	: 15 – 35 °C
Ukuran	: 1537,5 Cm^2
Berat	: 1 Kg
Display	: 16 x 2

```
;$include (reg51.inc)

;LCD constanta
;                01234567
;===KEYPAD : P2
dispclear     equ    00000001b
funcset       equ    00111000b
entrmod       equ    00000110b
dispon        equ    00001100b
cusor         equ    00001110b
blink         equ    00001101b
E             equ    p1.1
RS            equ    p1.0
con_lcd       equ    p1.2
data_lcd      equ    p1.3
play          equ    p1.4
eom           equ    p2.7
Flag          equ    0021H
FACK          equ    Flag.0
fsready       equ    Flag.1
FLB           equ    Flag.2
AutoInc       equ    Flag.3
OutputEnb     equ    Flag.4
InitDoneequ   Flag.5
MCOk          equ    Flag.6
First         equ    Flag.7
sda           equ    p2.0
scl           equ    p2.1
detak         equ    p2.2;aktif low
tombol1       equ    p2.5
tombol2       equ    p2.4
tombol3       equ    p2.3
buffer        equ    22h
Ch0           equ    30H
Ch1           equ    31H
Ch2           equ    32H
Ch3           equ    33H
Mode          equ    34H            ;0-3
Channel       equ    35H            ;0-3
ADDACB                equ    36H
NCh           equ    37H
LCh           equ    38H
tke1          equ    39h
tke2          equ    3ah
tke3          equ    3bh
buffer2       equ    3ch
datasis       equ    3dh
bdetak        equ    3eh
bdistole equ  3fh
bsistole equ  40h
satu          equ    0h
dua           equ    8h
tiga          equ    10h
empat         equ    18h
lima          equ    20h
enam          equ    28h
tujuh         equ    30h
delapan       equ    38h
```

```
sembilan        equ     40h
puluh           equ     48h
se              equ     50h
belas           equ     58h
kosong          equ     60h
suhututubuh     equ     68h
normal          equ     90h
kurang          equ     98h
sistoles  equ   0a8h
tekdarah equ    0b0h
mmhg            equ     0c0h
distoles  equ   0d0h
derajat         equ     0e0h
ratus           equ     0f8h
detaks          equ     0ffh
        org     0h
        jmp     mulai

    ORG   0BH
    JMP   TIMER0

;-------------------------------------------------
; PROSEDURE LAYANAN INTERUP TIMER 0
; 1 KALI INTERUP TIMER = 1 MS
TIMER0      PUSH   ACC
        PUSH   PSW
        MOV    A,R0
        PUSH   ACC
        CALL   INIT_TIMER2
        CALL   TIMER50
        ;CALL   TIMER1MS
ETIMER0     POP    ACC
        MOV    R0,A
        POP    PSW
        POP    ACC
        RETI

;-------------------------------------------------
;PROSEDUR YANG MASUK PADA INT. TIMER 100 mS
TIMER50     INC    tke1
        MOV    A,tke1
        CJNE   A,#100,A50END
A50END      JC     T50END
        MOV    tke1,#0
        inc tke2
T50END      RET
;==program utama

mulai:
                lcall inittlcd
                lcall inittimer
                mov buffer,#0
                mov tke1,#0
                mov tke2,#0
                lcall tampilawal
                MOV    P1,#0FFH
                MOV    SP,#40H
                MOV    Flag,#00H
```

```
                MOV     Ch0,#00H
                MOV     Ch1,#00H
                MOV     Ch2,#00H
                MOV     Ch3,#00H
                MOV     A,#00H          ;Slave Addr=0
                MOV     Mode,#0         ;Mode=0
                MOV     Channel,#0      ;Ch=0
                LCALL   InitADDA        ;Init ADDA
                JB      InitDone,coba
                CLR     P1.0            ;Indicate init fail
                AJMP    $
coba:
                MOV     B,#00H          ;Data=0
mulai1:         MOV     A,#00H          ;Slave Addr=0
                jnb tombol3,dtekanan
                ajmp mulai1
dtekanan:       ;lcall busek
                mov r5,#1
                mov dptr,#tek1
                lcall cetak1
                mov r5,#1
                mov dptr,#tek2
                lcall cetak2
                MOV     P1,#0FFH
                MOV     SP,#40H
                MOV     Flag,#00H
                MOV     Ch0,#00H
                MOV     Ch1,#00H
                MOV     Ch2,#00H
                MOV     Ch3,#00H
                MOV     A,#00H          ;Slave Addr=0
                MOV     Mode,#0         ;Mode=0
                MOV     Channel,#1      ;Ch=0
                LCALL   InitADDA        ;Init ADDA
dtekanan1:
                lcall bacatek
                mov a,buffer2
                cjne a,#70,dtekanan20
dtekanan20      jc dtekanan1
                lcall bacadetak
                lcall sistole
                lcall distole
dakhir:
                jnb tombol3,dtekanan
                ajmp dakhir
;ddetakj1:      ljmp ddetak
                nop
                nop
                nop
                AJMP    mulai1
                AJMP    $
;===subprogram
;===subroutin
;-----------------------------------------------
;ROUTINE INISIALISATION OF INTERNAL TIMER
INITTIMER       SETB    EA              ;ENABLE INTERUP
                SETB    ET0             ;ENABLE INT. TIMER 0
                SETB    TR0             ;TIMER 0 COUNTER ON
```

```
        MOV   TMOD,#00000001B ;MODE TIMER
INIT_TIMER2  MOV   TL0,#017H     ;T = 1 MS XTAL = 12 MHZ
        MOV   TH0,#0FCH
        RET
;-------------------------------------------------
Delaypcf:       PUSH  02H
                PUSH  03H
                MOV   R3,#0FH
Del:            MOV   R2,#0FFH
                DJNZ  R2,$
                DJNZ  R3,Del
                POP   03H
                POP   02H
                RET
dly2mnt:        mov r3,#55
dly2mnt1:       lcall dly1000ms
                djnz r3,dly2mnt1
                ret
bacadetak:      lcall busek
                mov tke1,#0
                mov tke2,#0
                mov r5,#1
                mov dptr,#detak0
                lcall cetak1
bacadetak0
                jb detak,bacadetak1
                mov tke1,#0
                mov tke2,#0
bacadetak1      mov a,tke2
                cjne a,#15,bacadetak3
bacadetak3:
                jc bacadetak0
                mov a,#"*"
                lcall dataout
                lcall dly1000ms
                lcall dly1000ms
                ;lcall dly1000ms
                ;lcall dly1000ms
                ;lcall dly1000ms
                ;lcall dly1000ms
                ret

sistole:  lcall bacatek
                jb detak,sistole
                lcall busek
                mov r5,#1
                mov dptr,#tsistole
                lcall cetak1
                ;subb a,#29
                mov a,buffer2
                cjne a,#220,lanjut1
lanjut1:  jc lanjut10
                sjmp sistole
lanjut10:;mov b,#14
                ;div ab
                ,mov b,#10
                ;mul ab
                ;add a,#57
```

```
                    mov datasis,a
                    lcall konversi
                    ret

distole:  mov tke1,#0
                    mov tke2,#0
                    lcall bacatek
                    mov r5,#1
                    mov dptr,#tdistole
                    lcall cetak2
distole0: jb detak,distole1
                    lcall bacatek
                    mov tke1,#0
                    mov tke2,#0
distole1: mov a,tke2
                    cjne a,#13,distole2
distole2: jc distole0
                    mov a,buffer2
                    mov bdistole,a
scandis:
   mov a,datasis
   cjne a,#75,scandis11
scandis11: jnc scandis20
   mov a,bdistole
   mov b,#7
   div ab
   mov a,b
   ;add a,#62
   mov a,#0
   lcall konversi
   lcall dly1000mS
   lcall busek
   mov r5,#1
                    mov dptr,#pe
                    lcall cetak1
            ;mov r5,#1
                    ;mov dptr,#dr
                    ;lcall cetak2
   ljmp scandisak
scandis20:
   cjne a,#100,scandis21
scandis21: jnc scandis30
   mov a,bdistole
   mov b,#10
   div ab
   mov a,b
   add a,#60
   lcall konversi
   lcall dly1000mS
   lcall busek
   mov r5,#1
                    mov dptr,#dr
                    lcall cetak1
            mov r5,#1
                    mov dptr,#dr
                    lcall cetak2
   ljmp scandisak
scandis30:
```

```
    cjne a,#120,scandis31
  scandis31: jnc scandis40
    mov a,bdistole
    mov b,#10
    div ab
    mov a,b
    add a,#70
    lcall konversi
    lcall dly1000mS
    lcall busek
    mov r5,#1
                    mov dptr,#nm
                    lcall cetak1
              mov r5,#1
                    mov dptr,#nm
                    lcall cetak2
    ljmp scandisak
  scandis40:
    cjne a,#140,scandis41
  scandis41: jnc scandis50
    mov a,bdistole
    mov b,#10
    div ab
    mov a,b
    add a,#80
    lcall konversi
    lcall dly1000mS
    lcall busek
    mov r5,#1
                    mov dptr,#ni
                    lcall cetak1
              mov r5,#1
                    mov dptr,#ni
                    lcall cetak2
    ljmp scandisak
  scandis50:
    cjne a,#150,scandis51
  scandis51: jnc scandis60
    mov a,bdistole
    mov b,#10
    div ab
    mov a,b
    add a,#90
    lcall konversi
    lcall dly1000mS
    lcall busek
    mov r5,#1
                    mov dptr,#nx
                    lcall cetak1
              mov r5,#1
                    mov dptr,#nx
                    lcall cetak2
    ljmp scandisak
  scandis60:
    cjne a,#160,scandis61
  scandis61: jnc scandis70
    mov a,bdistole
    mov b,#10
```

```
      div ab
      mov a,b
      add a,#100
      lcall konversi
      lcall dly1000mS
      lcall busek
      mov r5,#1
                        mov dptr,#ht1
                        lcall cetak1
                mov r5,#1
                        mov dptr,#ht1
                        lcall cetak2
      ljmp scandisak
  scandis70:
      cjne a,#180,scandis71
  scandis71: jnc scandis80
      mov a,bdistole
      mov b,#10
      div ab
      mov a,b
      add a,#110
      lcall konversi
      lcall dly1000mS
      lcall busek
      mov r5,#1
                        mov dptr,#ht2
                        lcall cetak1
              mov r5,#1
                        mov dptr,#ht2
                        lcall cetak2
      ljmp scandisak
  scandis80:
      cjne a,#210,scandis81
  scandis81: jnc scandis90
      mov a,bdistole
      mov b,#10
      div ab
      mov a,b
      add a,#120
      lcall konversi
      lcall dly1000mS
      lcall busek
      mov r5,#1
                        mov dptr,#ht3
                        lcall cetak1
              mov r5,#1
                        mov dptr,#ht3
                        lcall cetak2
      ljmp scandisak
scandis90:
      mov a,bdistole
      mov b,#10
      div ab
      mov a,b
      add a,#130
      lcall konversi
      lcall dly1000mS
      lcall busek
```

```
    mov r5,#1
                    mov dptr,#ht4
                    lcall cetak1
              mov r5,#1
                    mov dptr,#ht4
                    lcall cetak2
    ljmp scandisak
scandisak:
                    ;lcall konversi
                    ret

bacatek:
                    MOV    A,#00H
                    LCALL readadC
                    ;mov r5,#1
                    ;mov dptr,#tekanan
                    ;lcall cetak1
                    ;mov a,#255
                    ;subb a,ch1
                    ;add a,#60
                    ;mov buffer,a
                    ;subb a,#120
                    ;jc dtekanan2
                    ;add a,#60
                    mov a,ch1
                    lcall scandata
                    sjmp dtekanan3
dtekanan2:
                    mov a,buffer
dtekanan3:
                    mov buffer2,a
                    ;lcall konversi
                    ret
tampilawal:
          mov r5,#1
          mov dptr,#twal1
          lcall cetak1
          mov r5,#1
          mov dptr,#twal2
          lcall cetak2
          lcall dly1000ms
          ;mov r5,#1
          ;mov dptr,#twal3
          ;lcall cetak1
          ;mov r5,#1
          ;mov dptr,#twal4
          ;lcall cetak2
          ;lcall dly1000ms
          mov r5,#1
          mov dptr,#twal5
          lcall cetak1
          mov r5,#1
          mov dptr,#twal6
          lcall cetak2
          lcall dly1000ms
          mov r5,#1
          mov dptr,#twal7
          lcall cetak1
```

```
        mov r5,#1
        mov dptr,#twal8
        lcall cetak2
        lcall dly1000ms
        mov r5,#1
        mov dptr,#twal9
        lcall cetak1
        lcall dly1000ms
        mov r5,#1
        mov dptr,#tawal1
        lcall cetak1
        mov r5,#1
        mov dptr,#tawal2
        lcall cetak2
        RET

scandata:
        cjne a,#255,sel1
        mov a,#20
        ljmp akhirscan
sel1:   cjne a,#254,sel2
        mov a,#23
        ljmp akhirscan
sel2:   cjne a,#253,sel3
        mov a,#24
        ljmp akhirscan
sel3:   cjne a,#252,sel4
        mov a,#27
        ljmp akhirscan
sel4:   cjne a,#251,sel5
        mov a,#28
        ljmp akhirscan
sel5:   cjne a,#250,sel6
        mov a,#29
        ljmp akhirscan
sel6:   cjne a,#249,sel7
        mov a,#29
        ljmp akhirscan
sel7:   cjne a,#248,sel8
        mov a,#30
        ljmp akhirscan
sel8:   cjne a,#247,sel9
        mov a,#30
        ljmp akhirscan
sel9:   cjne a,#246,sel10
        mov a,#31
        ljmp akhirscan
sel10:  cjne a,#245,sel11
        mov a,#31
        ljmp akhirscan
sel11:  cjne a,#244,sel12
        mov a,#32
        ljmp akhirscan
sel12:  cjne a,#243,sel13
        mov a,#32
        ljmp akhirscan
sel13:  cjne a,#242,sel14
        mov a,#33
```

```
sel33:  cjne a,#224,sel34
        mov a,#43
        ljmp akhirscan
sel34:  cjne a,#223,sel35
        mov a,#44
        ljmp akhirscan
sel35:  cjne a,#222,sel36
        mov a,#44
        ljmp akhirscan
sel36:  cjne a,#221,sel37
        mov a,#45
        ljmp akhirscan
sel37:  cjne a,#220,sel38
        mov a,#46
        ljmp akhirscan
sel38:  cjne a,#219,sel39
        mov a,#47
        ljmp akhirscan
sel39:  cjne a,#218,sel40
        mov a,#47
        ljmp akhirscan
sel40:  cjne a,#217,sel41
        mov a,#48
        ljmp akhirscan
sel41:  cjne a,#216,sel42
        mov a,#48
        ljmp akhirscan
sel42:  cjne a,#215,sel43
        mov a,#49
        ljmp akhirscan
sel43:  cjne a,#214,sel44
        mov a,#49
        ljmp akhirscan
sel44:  cjne a,#213,sel45
        mov a,#50
        ljmp akhirscan
sel45:  cjne a,#212,sel46
        mov a,#50
        ljmp akhirscan
sel46:  cjne a,#211,sel47
        mov a,#50
        ljmp akhirscan
sel47:  cjne a,#210,sel48
        mov a,#50
        ljmp akhirscan
sel48:  cjne a,#209,sel49
        mov a,#51
        ljmp akhirscan
sel49:  cjne a,#209,sel50
        mov a,#52
        ljmp akhirscan
sel50:  cjne a,#208,sel51
        mov a,#53
        ljmp akhirscan
sel51:  cjne a,#207,sel52
        mov a,#54
        ljmp akhirscan
sel52:  cjne a,#206,sel53
```

```
        ljmp akhirscan
sel14:  cjne a,#241,sel15
        mov a,#33
        ljmp akhirscan
sel15:  cjne a,#242,sel16
        mov a,#34
        ljmp akhirscan
sel16:  cjne a,#241,sel17
        mov a,#34
        ljmp akhirscan
sel17:  cjne a,#240,sel18
        mov a,#35
        ljmp akhirscan
sel18:  cjne a,#239,sel19
        mov a,#36
        ljmp akhirscan
sel19:  cjne a,#238,sel20
        mov a,#36
        ljmp akhirscan
sel20:  cjne a,#237,sel21
        mov a,#37
        ljmp akhirscan
sel21:  cjne a,#236,sel22
        mov a,#37
        ljmp akhirscan
sel22:  cjne a,#235,sel23
        mov a,#38
        ljmp akhirscan
sel23:  cjne a,#234,sel24
        mov a,#38
        ljmp akhirscan
sel24:  cjne a,#233,sel25
        mov a,#39
        ljmp akhirscan
sel25:  cjne a,#232,sel26
        mov a,#39
        ljmp akhirscan
sel26:  cjne a,#231,sel27
        mov a,#40
        ljmp akhirscan
sel27:  cjne a,#230,sel28
        mov a,#40
        ljmp akhirscan
sel28:  cjne a,#229,sel29
        mov a,#41
        ljmp akhirscan
sel29:  cjne a,#228,sel30
        mov a,#41
        ljmp akhirscan
sel30:  cjne a,#227,sel31
        mov a,#42
        ljmp akhirscan
sel31:  cjne a,#226,sel32
        mov a,#42
        ljmp akhirscan
sel32:  cjne a,#225,sel33
        mov a,#43
        ljmp akhirscan
```

```
        mov a,#55
        ljmp akhirscan
sel53:  cjne a,#205,sel54
        mov a,#56
        ljmp akhirscan
sel54:  cjne a,#204,sel55
        mov a,#57
        ljmp akhirscan
sel55:  cjne a,#203,sel56
        mov a,#58
        ljmp akhirscan
sel56:  cjne a,#202,sel57
        mov a,#59
        ljmp akhirscan
sel57:  cjne a,#201,sel58
        mov a,#60
        ljmp akhirscan
sel58:  cjne a,#200,sel59
        mov a,#60
        ljmp akhirscan
sel59:  cjne a,#199,sel60
        mov a,#61
        ljmp akhirscan
sel60:  cjne a,#198,sel61
        mov a,#61
        ljmp akhirscan
sel61:  cjne a,#197,sel62
        mov a,#62
        ljmp akhirscan
sel62:  cjne a,#196,sel63
        mov a,#62
        ljmp akhirscan
sel63:  cjne a,#195,sel64
        mov a,#63
        ljmp akhirscan
sel64:  cjne a,#194,sel65
        mov a,#63
        ljmp akhirscan
sel65:  cjne a,#193,sel66
        mov a,#64
        ljmp akhirscan
sel66:  cjne a,#192,sel67
        mov a,#64
        ljmp akhirscan
sel67:  cjne a,#191,sel68
        mov a,#65
        ljmp akhirscan
sel68:  cjne a,#190,sel69
        mov a,#65
        ljmp akhirscan
sel69:  cjne a,#189,sel70
        mov a,#66
        ljmp akhirscan
sel70:  cjne a,#188,sel71
        mov a,#66
        ljmp akhirscan
sel71:  cjne a,#187,sel72
        mov a,#67
```

```
        ljmp akhirscan
sel72:  cjne a,#186,sel73
        mov a,#67
        ljmp akhirscan
sel73:  cjne a,#185,sel74
        mov a,#68
        ljmp akhirscan
sel74:  cjne a,#184,sel75
        mov a,#69
        ljmp akhirscan
sel75:  cjne a,#183,sel76
        mov a,#69
        ljmp akhirscan
sel76:  cjne a,#182,sel77
        mov a,#70
        ljmp akhirscan
sel77:  cjne a,#181,sel78
        mov a,#70
        ljmp akhirscan
sel78:  cjne a,#180,sel79
        mov a,#70
        ljmp akhirscan
sel79:  cjne a,#179,sel80
        mov a,#71
        ljmp akhirscan
sel80:  cjne a,#178,sel81
        mov a,#72
        ljmp akhirscan
sel81:  cjne a,#177,sel82
        mov a,#73
        ljmp akhirscan
sel82:  cjne a,#176,sel83
        mov a,#74
        ljmp akhirscan
sel83:  cjne a,#175,sel84
        mov a,#75
        ljmp akhirscan
sel84:  cjne a,#174,sel85
        mov a,#76
        ljmp akhirscan
sel85:  cjne a,#173,sel86
        mov a,#77
        ljmp akhirscan
sel86:  cjne a,#172,sel87
        mov a,#78
        ljmp akhirscan
sel87:  cjne a,#171,sel88
        mov a,#79
        ljmp akhirscan
sel88:  cjne a,#170,sel89
        mov a,#80
        ljmp akhirscan
sel89:  cjne a,#169,sel90
        mov a,#81
        ljmp akhirscan
sel90:  cjne a,#168,sel91
        mov a,#81
        ljmp akhirscan
```

```
sel91:   cjne a,#167,sel92
         mov a,#82
         ljmp akhirscan
sel92:   cjne a,#166,sel93
         mov a,#82
         ljmp akhirscan
sel93:   cjne a,#165,sel94
         mov a,#83
         ljmp akhirscan
sel94.   cjne a,#164,sel95
         mov a,#83
         ljmp akhirscan
sel95:   cjne a,#163,sel96
         mov a,#84
         ljmp akhirscan
sel96:   cjne a,#162,sel97
         mov a,#84
         ljmp akhirscan
sel97:   cjne a,#161,sel98
         mov a,#85
    ljmp akhirscan
sel98:   cjne a,#160,sel99
         mov a,#85
         ljmp akhirscan
sel99:   cjne a,#159,sel100
         mov a,#86
         ljmp akhirscan
sel100:  cjne a,#158,sel101
         mov a,#86
         ljmp akhirscan
sel101:  cjne a,#157,sel102
         mov a,#87
         ljmp akhirscan
sel102:  cjne a,#156,sel103
         mov a,#87
         ljmp akhirscan
sel103:  cjne a,#155,sel104
         mov a,#88
         ljmp akhirscan
sel104:  cjne a,#154,sel105
         mov a,#88
         ljmp akhirscan
sel105:  cjne a,#153,sel106
         mov a,#89
         ljmp akhirscan
sel106:  cjne a,#152,sel107
         mov a,#89
         ljmp akhirscan
sel107:  cjne a,#151,sel108
         mov a,#90
         ljmp akhirscan
sel108:  cjne a,#150,sel109
         mov a,#90
         ljmp akhirscan
sel109:  cjne a,#149,sel110
         mov a,#91
         ljmp akhirscan
sel110:  cjne a,#148,sel111
```

```
        mov a,#91
        ljmp akhirscan
sel111: cjne a,#147,sel112
        mov a,#92
        ljmp akhirscan
sel112: cjne a,#146,sel113
        mov a,#92
        ljmp akhirscan
sel113: cjne a,#145,sel114
        mov a,#93
        ljmp akhirscan
sel114: cjne a,#144,sel115
        mov a,#93
        ljmp akhirscan
sel115: cjne a,#143,sel116
        mov a,#93
        ljmp akhirscan
sel116: cjne a,#142,sel117
        mov a,#94
        ljmp akhirscan
sel117: cjne a,#141,sel118
        mov a,#94
        ljmp akhirscan
sel118: cjne a,#140,sel119
        mov a,#94
        ljmp akhirscan
sel119: cjne a,#139,sel120
        mov a,#95
        ljmp akhirscan
sel120: cjne a,#138,sel121
        mov a,#95
        ljmp akhirscan
sel121: cjne a,#137,sel122
        mov a,#95
        ljmp akhirscan
sel122: cjne a,#136,sel123
        mov a,#96
        ljmp akhirscan
sel123: cjne a,#135,sel124
        mov a,#96
        ljmp akhirscan
sel124: cjne a,#134,sel125
        mov a,#96
        ljmp akhirscan
sel125: cjne a,#133,sel126
        mov a,#97
        ljmp akhirscan
sel126: cjne a,#132,sel127
        mov a,#97
        ljmp akhirscan
sel127: cjne a,#131,sel128
        mov a,#97
        ljmp akhirscan
sel128: cjne a,#130,sel129
        mov a,#98
        ljmp akhirscan
sel129: cjne a,#129,sel130
        mov a,#98
```

```
        ljmp akhirscan
sel130: cjne a,#128,sel131
        mov a,#99
        ljmp akhirscan
sel131: cjne a,#127,sel132
        mov a,#99
        ljmp akhirscan
sel132: cjne a,#126,sel133
        mov a,#100
        ljmp akhirscan
sel133: cjne a,#125,sel134
        mov a,#100
        ljmp akhirscan
sel134: cjne a,#124,sel135
        mov a,#101
        ljmp akhirscan
sel135: cjne a,#123,sel136
        mov a,#101
        ljmp akhirscan
sel136: cjne a,#122,sel137
        mov a,#102
        ljmp akhirscan
sel137: cjne a,#121,sel138
        mov a,#102
        ljmp akhirscan
sel138: cjne a,#120,sel139
        mov a,#103
        ljmp akhirscan
sel139: cjne a,#119,sel140
        mov a,#103
        ljmp akhirscan
sel140: cjne a,#118,sel141
        mov a,#103
        ljmp akhirscan
sel141: cjne a,#117,sel142
        mov a,#104
        ljmp akhirscan
sel142: cjne a,#116,sel143
        mov a,#104
        ljmp akhirscan
sel143: cjne a,#115,sel144
        mov a,#104
        ljmp akhirscan
sel144: cjne a,#114,sel145
        mov a,#105
        ljmp akhirscan
sel145: cjne a,#113,sel146
        mov a,#105
        ljmp akhirscan
sel146: cjne a,#112,sel147
        mov a,#105
        ljmp akhirscan
sel147: cjne a,#111,sel148
        mov a,#106
        ljmp akhirscan
sel148: cjne a,#110,sel149
        mov a,#106
        ljmp akhirscan
```

```
sel149:  cjne a,#109,sel150
         mov a,#106
         ljmp akhirscan
sel150:  cjne a,#108,sel151
         mov a,#107
         ljmp akhirscan
sel151:  cjne a,#107,sel152
         mov a,#107
         ljmp akhirscan
sel152:  cjne a,#106,sel153
         mov a,#107
         ljmp akhirscan
sel153:  cjne a,#105,sel154
         mov a,#108
         ljmp akhirscan
sel154:  cjne a,#104,sel155
         mov a,#108
         ljmp akhirscan
sel155:  cjne a,#103,sel156
         mov a,#109
         ljmp akhirscan
sel156:  cjne a,#102,sel157
         mov a,#109
         ljmp akhirscan
sel157:  cjne a,#101,sel158
         mov a,#110
         ljmp akhirscan
sel158:  cjne a,#100,sel159
         mov a,#110
         ljmp akhirscan
sel159:  cjne a,#99,sel160
         mov a,#111
         ljmp akhirscan
sel160:  cjne a,#98,sel161
         mov a,#111
         ljmp akhirscan
sel161:  cjne a,#97,sel162
         mov a,#112
         ljmp akhirscan
sel162:  cjne a,#96,sel163
         mov a,#112
         ljmp akhirscan
sel163:  cjne a,#95,sel164
         mov a,#113
         ljmp akhirscan
sel164:  cjne a,#94,sel165
         mov a,#113
         ljmp akhirscan
sel165:  cjne a,#93,sel166
         mov a,#114
         ljmp akhirscan
sel166:  cjne a,#92,sel167
         mov a,#114
         ljmp akhirscan
sel167:  cjne a,#91,sel168
         mov a,#115
         ljmp akhirscan
sel168:  cjne a,#90,sel169
```

```
        mov a,#115
        ljmp akhirscan
sel169: cjne a,#89,sel170
        mov a,#116
        ljmp akhirscan
sel170: cjne a,#88,sel171
        mov a,#116
        ljmp akhirscan
sel171: cjne a,#87,sel172
        mov a,#117
        ljmp akhirscan
sel172: cjne a,#86,sel173
        mov a,#117
        ljmp akhirscan
sel173: cjne a,#85,sel174
        mov a,#118
        ljmp akhirscan
sel174: cjne a,#84,sel175
        mov a,#119
        ljmp akhirscan
sel175: cjne a,#83,sel176
        mov a,#119
        ljmp akhirscan
sel176: cjne a,#82,sel177
        mov a,#119
        ljmp akhirscan
sel177: cjne a,#81,sel178
        mov a,#120
        ljmp akhirscan
sel178: cjne a,#82,sel179
        mov a,#120
        ljmp akhirscan
sel179: cjne a,#81,sel180
        mov a,#121
        ljmp akhirscan
sel180: cjne a,#80,sel181
        mov a,#122
        ljmp akhirscan
sel181: cjne a,#79,sel182
        mov a,#123
        ljmp akhirscan
sel182: cjne a,#78,sel183
        mov a,#124
        ljmp akhirscan
sel183: cjne a,#77,sel184
        mov a,#125
        ljmp akhirscan
sel184: cjne a,#76,sel185
        mov a,#126
        ljmp akhirscan
sel185: cjne a,#75,sel186
        mov a,#127
        ljmp akhirscan
sel186: cjne a,#74,sel187
        mov a,#128
        ljmp akhirscan
sel187: cjne a,#73,sel188
        mov a,#129
```

```
        ljmp akhirscan
sel188: cjne a,#72,sel189
        mov a,#129
        ljmp akhirscan
sel189: cjne a,#71,sel190
        mov a,#130
        ljmp akhirscan
sel190: cjne a,#70,sel191
        mov a,#130
        ljmp akhirscan
sel191: cjne a,#69,sel192
        mov a,#131
        ljmp akhirscan
sel192: cjne a,#68,sel193
        mov a,#132
        ljmp akhirscan
sel193: cjne a,#67,sel194
        mov a,#133
        ljmp akhirscan
sel194: cjne a,#66,sel195
        mov a,#134
    ljmp akhirscan
sel195: cjne a,#65,sel196
        mov a,#135
        ljmp akhirscan
sel196: cjne a,#64,sel197
        mov a,#136
        ljmp akhirscan
sel197: cjne a,#63,sel198
        mov a,#137
        ljmp akhirscan
sel198: cjne a,#62,sel199
        mov a,#138
        ljmp akhirscan
sel199: cjne a,#61,sel200
        mov a,#139
        ljmp akhirscan
sel200: cjne a,#60,sel201
        mov a,#140
        ljmp akhirscan
sel201: cjne a,#59,sel202
        mov a,#141
        ljmp akhirscan
sel202: cjne a,#58,sel203
        mov a,#141
        ljmp akhirscan
sel203: cjne a,#57,sel204
        mov a,#142
        ljmp akhirscan
sel204: cjne a,#56,sel205
        mov a,#142
        ljmp akhirscan
sel205: cjne a,#55,sel206
        mov a,#143
        ljmp akhirscan
sel206: cjne a,#54,sel207
        mov a,#143
        ljmp akhirscan
```

```
sel207:  cjne a,#53,sel208
         mov a,#144
         ljmp akhirscan
sel208:  cjne a,#52,sel209
         mov a,#145
    ljmp akhirscan

sel209:  mov a,#145
akhirscan:
         ret

busek:   mov r5,#1
         mov dptr,#hapu
         lcall cetak1
         mov r5,#1
         mov dptr,#hapu
         lcall cetak2
         ret

konversi:
         mov b,#100
         div ab
         mov r1,b
         orl a,#30h
         lcall dataout
         mov a,r1
         mov b,#10
         div ab
         mov r1,b
         orl a,#30h
         lcall dataout
         mov a,r1
         orl a,#30h
         lcall dataout
         ret

kon:

         mov b,#100
         div ab
         mov r0,b
         cjne a,#0,kon000
         sjmp kon102
kon000:
         cjne a,#1,kon100
         mov a,#se
         lcall suara
         sjmp kon101
kon100:  lcall scan
kon101:
         mov a,#ratus
         lcall suara
kon102:
         mov a,r0
         mov b,#10
         div ab
         mov r0,b
         cjne a,#1,kon1
```

```
        cjne r0,#1,kon10
        mov a,#se
        lcall suara
        mov a,#belas
        lcall suara
        ret
kon10:  cjne r0,#0,kon11
        mov a,#se
        lcall suara
        mov a,#puluh
        lcall suara
        ret
kon11:  mov a,r0
        lcall scan
        mov a,#belas
        lcall suara
        ret
kon1:   cjne a,#0,kon2
        mov a,r0
        lcall scan
        ret
kon2:   lcall scan
        mov a,#puluh
        lcall suara
        mov a,r0
        lcall scan
        ret


scan:   cjne a,#1,scan2
        mov a,#satu
        ljmp scanakhir
scan2:  cjne a,#2,scan3
        mov a,#dua
        ljmp scanakhir
scan3:  cjne a,#3,scan4
        mov a,#tiga
        ljmp scanakhir
scan4:  cjne a,#4,scan5
        mov a,#empat
        ljmp scanakhir
scan5:  cjne a,#5,scan6
        mov a,#lima
        ljmp scanakhir
scan6:  cjne a,#6,scan7
        mov a,#enam
        ljmp scanakhir
scan7:  cjne a,#7,scan8
        mov a,#tujuh
        ljmp scanakhir
scan8:  cjne a,#8,scan9
        mov a,#delapan
        ljmp scanakhir
scan9:  cjne a,#9,scan10
        mov a,#sembilan
        ljmp scanakhir
scan10:
```

```
        ;mov a,#kosong
        ljmp scanakhir1
scanakhir:
        lcall suara
scanakhir1:
        ret

suara:
        mov p3,a
        lcall dly100ms
        lcall dly100ms
        clr play
        nop
        nop
        setb play
        jb eom,$
        ret


;-------------------
;Check SCL Line Routine
;Input  : none
;Output : fsready=0/1
;-------------------
ChkSCLCon:  JB      scl,SlvRdy          ;Check SCL
            CLR     fsready
            RET
SlvRdy:     SETB    fsready
            RET
;-------------------
;Start Condition Routine
;Input  : none
;Output : none
;-------------------
StartCon:   CLR     scl                 ;SCL Low
            SETB    sda                 ;SDA High
            SETB    scl                 ;SCL High
            CLR     sda                 ;SDA -|_ when SCL High
            LCALL   Delay5us            ;
            RET
;-------------------
;Delay Routine For I2C
;Input  : none
;Output : none
;-------------------
Delay5us:   NOP
            RET
Delay3us:   RET
;-----------------------------------
;Master Transmitter Routine
;Input  : ACC <- Data/Address/Control byte
;Output : none
;-----------------------------------
Mtx:        PUSH    07H
            PUSH    ACC
            MOV     R7,#8
NexBit:     CLR     scl                 ;SCL Low ----------\
            RLC     A                   ;(1) Data MSB first  |
```

```
                JNC     TxL                     ;(2) Data Bit Low    |
TxH:            SETB    sda                     ;(2) SDA High        |-1 CLK
                AJMP    Clock                   ;(2)                 |
TxL:            CLR     sda                     ;(2) SDA Low         |
Clock:          SETB    scl                     ;SCL High            |
                ACALL   Delay3us                ;                    |
                DJNZ    R7,NexBit               ;(2) ----------------/

AckPhaseClk:    CLR     scl                     ;SCL Low ------------\
                SETB    sda                     ;(2) release SDA high |
                ACALL   Delay3us                ;                    |
                SETB    scl                     ;SCL High            |-CLK
                JNB     sda,Ack         ;(3) Chck SDA ACK/NACK | ACK
Nack:           CLR     FACK                    ;(2)                 |
                AJMP    EOMtx1                          ;(2)                 |
Ack:            SETB    FACK                    ;(2)                 |
EOMtx1:                 POP     ACC                             ;(2)                 |
                POP     07H                     ;(2)                 |

                RET                             ;(1) ----------------/
;---------------------
;Stop Condition Routine
;Input  : none
;Output : none
;---------------------
StopCon:        CLR     scl                     ;SCL Low-------------------\
                CLR     sda                     ;(2) SDA Low               |
                ACALL   Delay3us                ;                          |
                SETB    scl                     ;SCL High                  |-STOP
                SETB    sda                     ;(2) SDA _|~ when SCL High|
                NOP                             ;(1)                       |
                NOP                             ;(1)                       |
                RET                             ;(1) ----------------------/
;---------------------
;Master Receiver Routine
;Input  : FLB <- 1/0
;Output : ACC
;---------------------
MRx:            PUSH    07H
RdData:         MOV     R7,#8
                CLR     C
NextBit: CLR    scl                     ;SCL Low -------\
                SETB    sda                     ;(2)For input        |
                ACALL   Delay3us                ;                    |
                SETB    scl                     ;SCL High            |
                JB      sda,HiBit               ;(3) Chk SDA H/L     |
LoBit:          CLR     C                       ;(1)                 |-1 CLK
                AJMP    SaveBit                 ;(2)                 |
HiBit:          SETB    C                       ;(1)                 |
SaveBit: RLC    A                       ;(1)                 |
                DJNZ    R7,NextBit              ;(2) ----------/
AckPhsClk:      CLR     scl                     ;SCL Low ----\
                JB      FLB,NAckd               ;(3)         |
Ackd:           CLR     sda                     ;(2)         |
                AJMP    ClkHigh                 ;(2)         |-ACK Related
NAckd:          SETB    sda                     ;(2)         | CLK
ClkHigh:        SETB    scl                     ;SCL High    |
                ACALL   Delay3us                ; ----------/
```

```
EOMRx:          POP     07H                     ;(2)
                RET                             ;(1)

;-------------------------
;Check Valid Channel and Mode
;Input  : Mode,Channel
;Output : Channel, MCOk Flag
;-------------------------
ChkMC:          PUSH    ACC
                MOV     A,Mode
CM0:            CJNE    A,#0,CM1
Mode0:          MOV     NCh,#3
                MOV     LCh,#Mode
                MOV     A,Channel
                CJNE    A,#4,$+3
                JC      ValidMC
                MOV     Channel,#3
                LJMP    ValidMC
CM1:            CJNE    A,#1,CM2
Mode1:          MOV     NCh,#2
                MOV     LCh,#Ch3
                MOV     A,Channel
                CJNE    A,#3,$+3
                JC      ValidMC
                MOV     Channel,#2
                LJMP    ValidMC
CM2:            CJNE    A,#2,CM3
Mode2:          MOV     NCh,#2
                MOV     LCh,#Ch3
                MOV     A,Channel
                CJNE    A,#3,$+3
                JC      ValidMC
                MOV     Channel,#2
                LJMP    ValidMC
CM3:            CJNE    A,#3,InvalidMC
Mode3:          MOV     NCh,#1
                MOV     LCh,#Ch2
                MOV     A,Channel
                CJNE    A,#2,$+3
                JC      ValidMC
                MOV     Channel,#1
                LJMP    ValidMC
InvalidMC:      CLR     MCOk
                POP     ACC
                RET
ValidMC:        SETB    MCOk
                POP     ACC
                RET

;-------------------------
;Init ADDA Mode Routine
;Input  : Mode,Channel,AutoInc,OutputEnb
;         A <- Slave Address (0-7)
;Output : ADDACB,InitDone Flag
;-------------------------
InitADDA:       PUSH    ACC
                PUSH    B
                LCALL   ChkMC
```

```
                JNB     MCOk,InitADDAbort
                XCH     A,B
                MOV     A,Mode
                SWAP    A
                ORL     A,Channel
ChkAutoInc:     JNB     AutoInc,ChkOutputEnb
                SETB    ACC.6
                SETB    ACC.2
ChkOutputEnb:   JNB     OutputEnb,NextInit
                SETB    ACC.6
NextInit:       XCH     A,B
                RL      A
                ANL     A,#0EH                  ;0000XXX0B
                ORL     A,#90H                  ;1001XXX0B
                LCALL   StartCon
                LCALL   MTx
                JNB     FACK,InitADDAbort
                XCH     A,B
                LCALL   MTx
                JNB     FACK,InitADDAbort
InitADDASucc:   LCALL   StopCon
                MOV     ADDACB,A
                SETB    InitDone
                POP     B
                POP     ACC
                RET
InitADDAbort:   LCALL   StopCon
                CLR     InitDone
                POP     B
                POP     ACC
                RET

;-------------------------------
;Read ADC Routine
;Input  : A <- Slave Address (0-7)
;Output : Ch0-Ch3
;-------------------------------
ReadADC:        PUSH    ACC
                PUSH    00H
                PUSH    07H
                JNB     InitDone,ExitReadADC
                LCALL   ChkSCLCon
                JNB     fsready,ExitReadADC
                RL      A
                ANL     A,#0FH                  ;0000XXXXB
                ORL     A,#91H                  ;1001XXX1B
                JNB     AutoInc,ReadADCChx
ReadADCAI:      PUSH    ACC
                MOV     R0,#Ch0
                MOV     A,Channel
                ADD     A,R0
                MOV     R0,A
                POP     ACC
                LCALL   StartCon
                LCALL   MTx
                JNB     FACK,ReadADCAbort
                CLR     FLB
                LCALL   MRx
```

```
                MOV     R7,NCh
NxtCh:          LCALL   MRx
                MOV     @R0,A
                INC     R0
                MOV     A,R0
                CJNE    A,LCh,GoAhead
                MOV     R0,#Ch0
GoAhead:        DJNZ    R7,NxtCh
                SETB    FLB
                LCALL   MRx
                MOV     @R0,A
                LCALL   StopCon
                AJMP    ExitReadADC
ReadADCChx:     MOV     R0,#Channel
                LCALL   StartCon
                LCALL   MTx
                JNB     FACK,ReadADCAbort
                CLR     FLB
                LCALL   MRx
                SETB    FLB
                LCALL   MRx
                LCALL   StopCon
ChkCh0:                 CJNE    @R0,#0,ChkCh1
                MOV     Ch0,A
                AJMP    ExitReadADC
ChkCh1:                 CJNE    @R0,#1,ChkCh2
                MOV     Ch1,A
                AJMP    ExitReadADC
ChkCh2:                 CJNE    @R0,#2,ADCCh3
                MOV     Ch2,A
                AJMP    ExitReadADC
ADCCh3:                 MOV     Ch3,A
                AJMP    ExitReadADC
ReadADCAbort:   LCALL   StopCon
ExitReadADC:    POP     07H
                POP     00H
                POP     ACC
                RET

;-----------------------------
;Write to DAC Routine
;Input  : A <- Slave Address (0-7)
;         B <- DAC Data
;Output : Output Enable Flag Set
;-----------------------------
WriteDAC:       PUSH    ACC
                PUSH    B
                JNB     InitDone,ExitWriteDAC
                LCALL   ChkSCLCon
                JNB     fsready,ExitWriteDAC
                RL      A
                ANL     A,#0EH                  ;0000XXX0B
                ORL     A,#90H                  ;1001XXX0B
                LCALL   StartCon
                LCALL   Mtx
                JNB     FACK,WriteDACAbort
                MOV     A,ADDACB
                SETB    ACC.6
```

```
                    LCALL Mtx
                    JNB   FACK,WriteDACAbort
                    XCH   A,B
                    LCALL MTx
WriteDACAbort:      LCALL StopCon
ExitWriteDAC:       POP   B
                    POP   ACC
                    RET

;=========routine lcd
baris2:
      mov a,r5
      add a,#0c0h ;11000000b
      sjmp posisisub
baris1:
      mov a,r5
      add a,#80h; 10000000b
posisisub:
      dec  a
      lcall controlout
      ret
cetak2:
      lcall baris2
      sjmp ansa
cetak1:
      lcall baris1
ansa:
      sjmp outstring
loop:
      lcall dataout
      inc dptr
outstring:
      clr a
      movc a,@a+dptr
      cjne a,#'$',loop
      ret
controlout:
      push dph
      push dpl
      clr rs
      sjmp out
dataout:
      push dph
      push dpl
      setb rs
out:
      setb e
      lcall geser
      mov r6,#250
      djnz r6,$
      pop dpl
      pop dph
      clr e
      ret

geser:
      clr con_lcd
      mov   b,#8
```

```
a1:
        rrc a
        mov data_lcd,c
        nop
        nop
        nop
        nop
        setb con_lcd
        nop
        nop
        nop
        nop
        clr con_lcd
        djnz b,a1
        ret
delay:
        mov r6,#00h
dlylcdlp:
        mov r7,#00h
        djnz r7,$
        djnz r6,dlylcdlp
        ret
ldelay:
ldelay2:
        mov r3,#00h
ldelay1:
        lcall tdelay
        djnz r3,ldelay1
        djnz r2, ldelay2
        ret
tdelay:
        mov r7,#00h
        djnz r7,$
        ret
initlcd:
        mov  a,#dispclear
        lcall controlout
        lcall delay
        mov a,#funcset
        lcall controlout
        mov a,#dispon
        lcall controlout
        mov a,#entrmod
        lcall controlout
        ret
;-- Routine delay --
d50ms:  push     tmod
        mov tmod,#21h
        mov th0,#03fh  ;3cb0
        mov tl0,#0f0h
        setb tr0
t50ms:  jbc tf0,sudah
        jb detak,lewat
        jnb detak,$
        inc buffer
lewat:
        ajmp t50ms
sudah:  clr tr0
```

```
            pop tmod
            ret

d1det:      mov r7,#200;20
d1det1:     call d50ms
            djnz r7,d1det1
            ret

hitung:     jb detak,lom0
            jnb detak,$
            lcall dly100ms
            lcall dly100ms
            lcall dly100ms
            lcall dly100ms
            inc buffer
lom0:       mov a,tke2
            cjne a,#200,terus;100
terus:      jc hitung
            mov tke2,#0
            ret

;=============================
;rutin delay
;=============================
dly1000mS:
            mov    r2,#10
UlDel:
            lcall  dly100mS
      djnz   r2,UlDel
      ret
dly100mS:
            mov r6,#200
      ljmp   waktu
dly10mS:
            mov  r6,#20
      ljmp    waktu

; Timer 0,5 mS
; R6 = perkalian
waktu:
            mov      r7,#247
      djnz   r7,$
      djnz   r6,Waktu
      ret
dr:
            db '  Darah rendah  $'
nm:
            db ' Normal minimal $'
ni:
            db '  Normal ideal  $'
nx:
            db ' Normal Maximal $'
ht1:
            db '  Hip. tahap I  $'
ht2:
            db ' Hip. tahap II  $'
ht3:
            db ' Hip. tahap III $'
```

```
ht4:
        db ' Hip. tahap IV  $'
pe:
        db 'Pembacaan error $'
hapu:
        db '                $'

detak0:
        db 'Tanda:$'
detak1:
        db 'Detak/menit.$'
tekanan:
        db 'Tekanan:$'
twal1:
        db 'Alat Pendeteksi $'
twal2:
        db ' Tekanan Darah  $'
twal3:
        db '  Suhu Badan,   $'
twal4:
        db ' Denyut Jantung $'
twal5:
        db '    Oleh:     $'
twal6:
        db '  OKTAVIANTO   $'
twal7:
        db '     NIM      $'
twal8:
        db '  03.52.010    $'
twal9:
        db 'T.ELEKTRO D-III $'
tawal1:
        db '  Pengontrol    $'
tawal2:
        db '  Kesehatan     $'
tek1:
        db '  Pengukuran    $'
tek2:
        db ' Tekanan Darah  $'
tsistole:
        db 'Sistole :$'
tdistole:
        db 'Diastole:$'

        end
```

atures

ompatible with MCS-51® Products
K Bytes of In-System Programmable (ISP) Flash Memory
– Endurance: 1000 Write/Erase Cycles
.0V to 5.5V Operating Range
ully Static Operation: 0 Hz to 33 MHz
hree-level Program Memory Lock
28 x 8-bit Internal RAM
2 Programmable I/O Lines
wo 16-bit Timer/Counters
ix Interrupt Sources
ull Duplex UART Serial Channel
ow-power Idle and Power-down Modes
terrupt Recovery from Power-down Mode
atchdog Timer
ual Data Pointer
ower-off Flag
st Programming Time
exible ISP Programming (Byte and Page Mode)

scription

AT89S51 is a low-power, high-performance CMOS 8-bit microcontroller with 4K s of in-system programmable Flash memory. The device is manufactured using el's high-density nonvolatile memory technology and is compatible with the indus- tandard 80C51 instruction set and pinout. The on-chip Flash allows the program nory to be reprogrammed in-system or by a conventional nonvolatile memory pro- mer. By combining a versatile 8-bit CPU with in-system programmable Flash on a olithic chip, the Atmel AT89S51 is a powerful microcontroller which provides a ly-flexible and cost-effective solution to many embedded control applications.

AT89S51 provides the following standard features: 4K bytes of Flash, 128 bytes of I, 32 I/O lines, Watchdog timer, two data pointers, two 16-bit timer/counters, a five- or two-level interrupt architecture, a full duplex serial port, on-chip oscillator, and c circuitry. In addition, the AT89S51 is designed with static logic for operation n to zero frequency and supports two software selectable power saving modes. Idle Mode stops the CPU while allowing the RAM, timer/counters, serial port, and rupt system to continue functioning. The Power-down mode saves the RAM con- but freezes the oscillator, disabling all other chip functions until the next external rupt or hardware reset.

8-bit Microcontroller with 4K Bytes In-System Programmable Flash

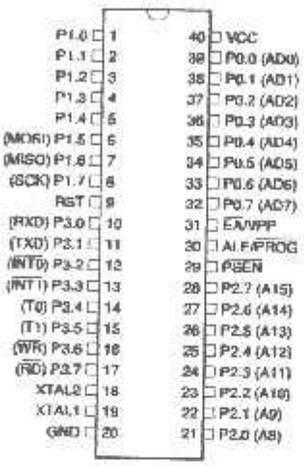
AT89S51

Preliminary

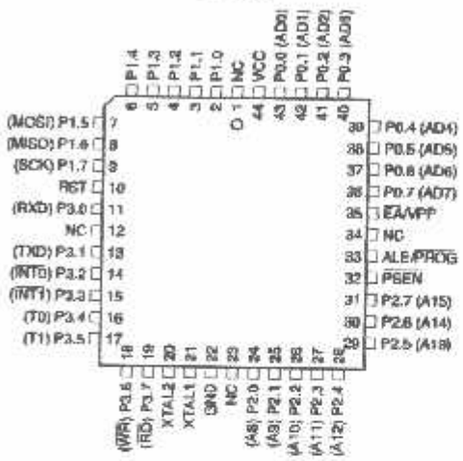
Rev. 2487A–10/01

n Configurations

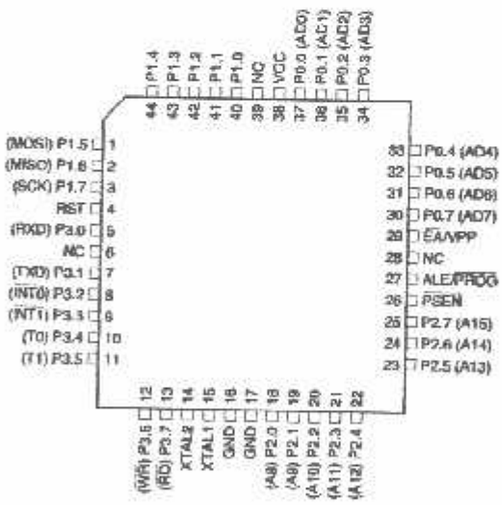
PDIP



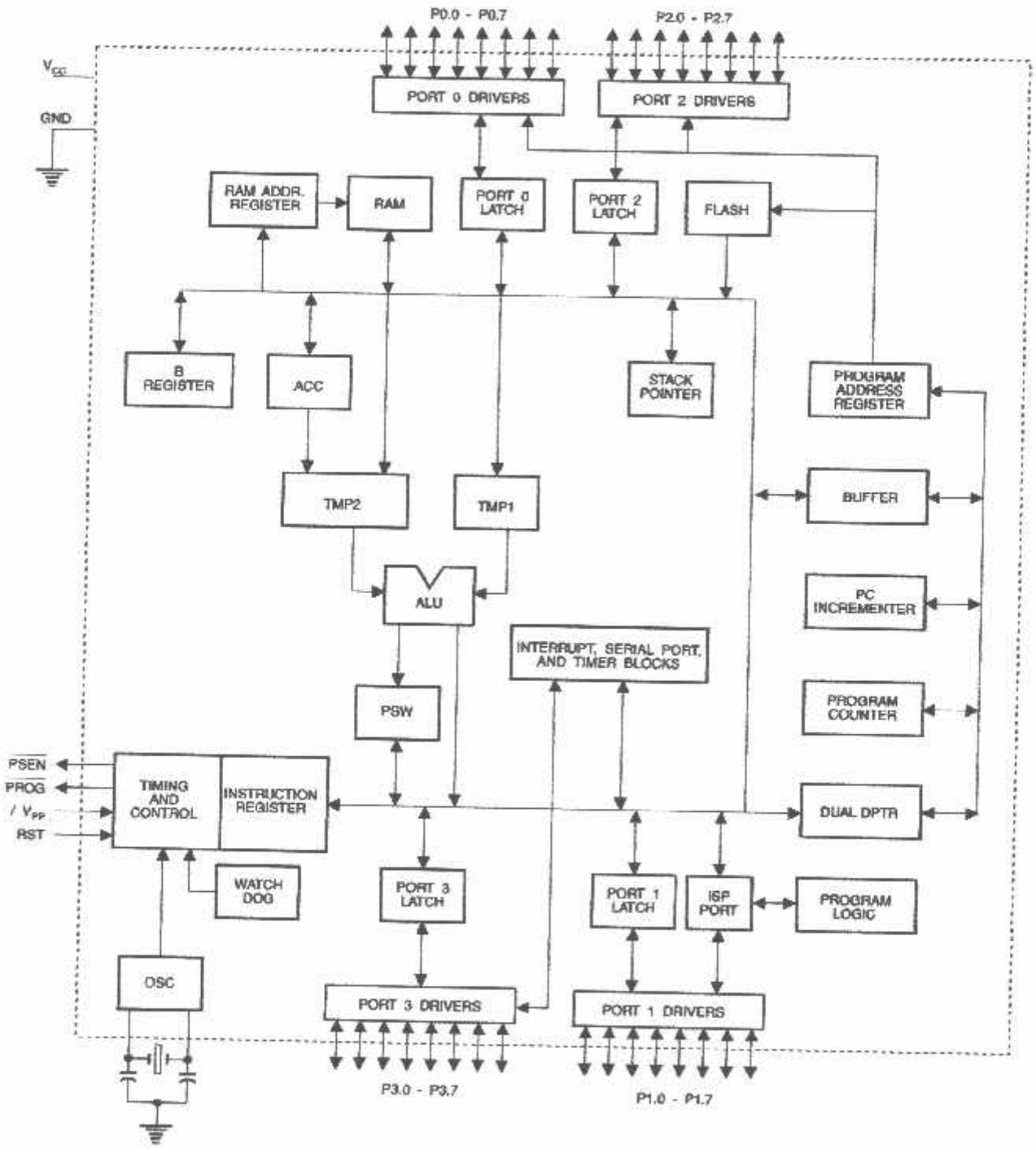
PLCC



TQFP



ock Diagram


P0.0 - P0.7
P2.0 - P2.7
V_{CC}
GND
PORT 0 DRIVERS
PORT 2 DRIVERS
RAM ADDR. REGISTER
RAM
PORT 0 LATCH
PORT 2 LATCH
FLASH
B REGISTER
ACC
STACK POINTER
PROGRAM ADDRESS REGISTER
TMP2
TMP1
BUFFER
ALU
PC INCREMENTER
INTERRUPT, SERIAL PORT, AND TIMER BLOCKS
PSW
PROGRAM COUNTER
PSEN
PROG
/ V_{PP}
RST
TIMING AND CONTROL
INSTRUCTION REGISTER
DUAL DPTR
WATCH DOG
PORT 3 LATCH
PORT 1 LATCH
ISP PORT
PROGRAM LOGIC
OSC
PORT 3 DRIVERS
PORT 1 DRIVERS
P3.0 - P3.7
P1.0 - P1.7

n Description

:C Supply voltage.

ID Ground.

rt 0 Port 0 is an 8-bit open drain bidirectional I/O port. As an output port, each pin can sink eight TTL inputs. When 1s are written to port 0 pins, the pins can be used as high-impedance inputs.

Port 0 can also be configured to be the multiplexed low-order address/data bus during accesses to external program and data memory. In this mode, P0 has internal pull-ups.

Port 0 also receives the code bytes during Flash programming and outputs the code bytes during program verification. **External pull-ups are required during program verification.**

t 1 Port 1 is an 8-bit bidirectional I/O port with internal pull-ups. The Port 1 output buffers can sink/source four TTL inputs. When 1s are written to Port 1 pins, they are pulled high by the internal pull-ups and can be used as inputs. As inputs, Port 1 pins that are externally being pulled low will source current (I_{IL}) because of the internal pull-ups.

Port 1 also receives the low-order address bytes during Flash programming and verification.

Port Pin	Alternate Functions
P1.5	MOSI (used for In-System Programming)
P1.6	MISO (used for In-System Programming)
P1.7	SCK (used for In-System Programming)

t 2 Port 2 is an 8-bit bidirectional I/O port with internal pull-ups. The Port 2 output buffers can sink/source four TTL inputs. When 1s are written to Port 2 pins, they are pulled high by the internal pull-ups and can be used as inputs. As inputs, Port 2 pins that are externally being pulled low will source current (I_{IL}) because of the internal pull-ups.

Port 2 emits the high-order address byte during fetches from external program memory and during accesses to external data memory that use 16-bit addresses (MOVX @ DPTR). In this application, Port 2 uses strong internal pull-ups when emitting 1s. During accesses to external data memory that use 8-bit addresses (MOVX @ RI), Port 2 emits the contents of the P2 Special Function Register.

Port 2 also receives the high-order address bits and some control signals during Flash programming and verification.

3 Port 3 is an 8-bit bidirectional I/O port with internal pull-ups. The Port 3 output buffers can sink/source four TTL inputs. When 1s are written to Port 3 pins, they are pulled high by the internal pull-ups and can be used as inputs. As inputs, Port 3 pins that are externally being pulled low will source current (I_{IL}) because of the pull-ups.

Port 3 receives some control signals for Flash programming and verification.

Port 3 also serves the functions of various special features of the AT89S51, as shown in the following table.

Port Pin	Alternate Functions
P3.0	RXD (serial input port)
P3.1	TXD (serial output port)
P3.2	$\overline{INT0}$ (external interrupt 0)
P3.3	$\overline{INT1}$ (external interrupt 1)
P3.4	T0 (timer 0 external input)
P3.5	T1 (timer 1 external input)
P3.6	$\overline{WR}$ (external data memory write strobe)
P3.7	$\overline{RD}$ (external data memory read strobe)

T

Reset input. A high on this pin for two machine cycles while the oscillator is running resets the device. This pin drives High for 98 oscillator periods after the Watchdog times out. The DISRTO bit in SFR AUXR (address 8EH) can be used to disable this feature. In the default state of bit DISRTO, the RESET HIGH out feature is enabled.

E/$\overline{PROG}$

Address Latch Enable (ALE) is an output pulse for latching the low byte of the address during accesses to external memory. This pin is also the program pulse input ($\overline{PROG}$) during Flash programming.

In normal operation, ALE is emitted at a constant rate of 1/6 the oscillator frequency and may be used for external timing or clocking purposes. Note, however, that one ALE pulse is skipped during each access to external data memory.

If desired, ALE operation can be disabled by setting bit 0 of SFR location 8EH. With the bit set, ALE is active only during a MOVX or MOVC instruction. Otherwise, the pin is weakly pulled high. Setting the ALE-disable bit has no effect if the microcontroller is in external execution mode.

:N

Program Store Enable ($\overline{PSEN}$) is the read strobe to external program memory.

When the AT89S51 is executing code from external program memory, $\overline{PSEN}$ is activated twice each machine cycle, except that two $\overline{PSEN}$ activations are skipped during each access to external data memory.

/PP

External Access Enable. $\overline{EA}$ must be strapped to GND in order to enable the device to fetch code from external program memory locations starting at 0000H up to FFFFH. Note, however, that if lock bit 1 is programmed, $\overline{EA}$ will be internally latched on reset.

$\overline{EA}$ should be strapped to V_{CC} for internal program executions.

This pin also receives the 12-volt programming enable voltage (V_{PP}) during Flash programming.

L1

Input to the inverting oscillator amplifier and input to the internal clock operating circuit.

L2

Output from the inverting oscillator amplifier

›ecial inction ›egisters

A map of the on-chip memory area called the Special Function Register (SFR) space is shown in Table 1.

Note that not all of the addresses are occupied, and unoccupied addresses may not be implemented on the chip. Read accesses to these addresses will in general return random data, and write accesses will have an indeterminate effect.

ıle 1. AT89S51 SFR Map and Reset Values

)F8H								0FFH
)F0H	B 00000000							0F7H
E8H								0EFH
E0H	ACC 00000000							0E7H
D8H								0DFH
D0H	PSW 00000000							0D7H
C8H								0CFH
C0H								0C7H
B8H	IP XX000000							0BFH
B0H	P3 11111111							0B7H
A8H	IE 0X000000							0AFH
A0H	P2 11111111		AUXR1 XXXXXXX0				WDTRST XXXXXXXX	0A7H
98H	SCON 00000000	SBUF XXXXXXXX						9FH
90H	P1 11111111							97H
88H	TCON 00000000	TMOD 00000000	TL0 00000000	TL1 00000000	TH0 00000000	TH1 00000000	AUXR XXX00XX0	8FH
80H	P0 11111111	SP 00000111	DP0L 00000000	DP0H 00000000	DP1L 00000000	DP1H 00000000	PCON 0XXX0000	87H

User software should not write 1s to these unlisted locations, since they may be used in future products to invoke new features. In that case, the reset or inactive values of the new bits will always be 0.

Interrupt Registers: The individual interrupt enable bits are in the IE register. Two priorities can be set for each of the five interrupt sources in the IP register.

Table 2. AUXR: Auxiliary Register

AUXR — Address = 8EH — Reset Value = XXX00XX0B

Not Bit Addressable

Bit	7	6	5	4	3	2	1	0
	–	–	–	WDIDLE	DISRTO	–	–	DISALE

– Reserved for future expansion

DISALE Disable/Enable ALE

DISALE Operating Mode

0 ALE is emitted at a constant rate of 1/6 the oscillator frequency

1 ALE is active only during a MOVX or MOVC instruction

DISRTO Disable/Enable Reset out

DISRTO

0 Reset pin is driven High after WDT times out

1 Reset pin is input only

WDIDLE Disable/Enable WDT in IDLE mode

WDIDLE

0 WDT continues to count in IDLE mode

1 WDT halts counting in IDLE mode

Dual Data Pointer Registers: To facilitate accessing both internal and external data memory, two banks of 16-bit Data Pointer Registers are provided: DP0 at SFR address locations 82H-83H and DP1 at 84H-85H. Bit DPS = 0 in SFR AUXR1 selects DP0 and DPS = 1 selects DP1. The user should always initialize the DPS bit to the appropriate value before accessing the respective Data Pointer Register.

Power Off Flag: The Power Off Flag (POF) is located at bit 4 (PCON.4) in the PCON SFR. POF is set to "1" during power up. It can be set and rest under software control and is not affected by reset.

Table 3. AUXR1: Auxiliary Register 1

AUXR1

Address = A2H

Reset Value = XXXXXXX0B

Not Bit Addressable

	–	–	–	–	–	–	–	DPS
Bit	7	6	5	4	3	2	1	0

– Reserved for future expansion

DPS Data Pointer Register Select

DPS	
0	Selects DPTR Registers DP0L, DP0H
1	Selects DPTR Registers DP1L, DP1H

mory ganization

MCS-51 devices have a separate address space for Program and Data Memory. Up to 64K bytes each of external Program and Data Memory can be addressed.

gram Memory

If the $\overline{EA}$ pin is connected to GND, all program fetches are directed to external memory.

On the AT89S51, if $\overline{EA}$ is connected to V_{CC}, program fetches to addresses 0000H through FFFH are directed to internal memory and fetches to addresses 1000H through FFFFH are directed to external memory.

a Memory

The AT89S51 implements 128 bytes of on-chip RAM. The 128 bytes are accessible via direct and indirect addressing modes. Stack operations are examples of indirect addressing, so the 128 bytes of data RAM are available as stack space.

tchdog ier e-time ibled with et-out)

The WDT is intended as a recovery method in situations where the CPU may be subjected to software upsets. The WDT consists of a 14-bit counter and the Watchdog Timer Reset (WDTRST) SFR. The WDT is defaulted to disable from exiting reset. To enable the WDT, a user must write 01EH and 0E1H in sequence to the WDTRST register (SFR location 0A6H). When the WDT is enabled, it will increment every machine cycle while the oscillator is running. The WDT timeout period is dependent on the external clock frequency. There is no way to disable the WDT except through reset (either hardware reset or WDT overflow reset). When WDT overflows, it will drive an output RESET HIGH pulse at the RST pin.

ng the WDT

To enable the WDT, a user must write 01EH and 0E1H in sequence to the WDTRST register (SFR location 0A6H). When the WDT is enabled, the user needs to service it by writing 01EH and 0E1H to WDTRST to avoid a WDT overflow. The 14-bit counter overflows when it reaches 16383 (3FFFH), and this will reset the device. When the WDT is enabled, it will increment every machine cycle while the oscillator is running. This means the user must reset the WDT at least every 16383 machine cycles. To reset the WDT the user must write 01EH and 0E1H to WDTRST. WDTRST is a write-only register. The WDT counter cannot be read or written. When WDT overflows, it will generate an output RESET pulse at the RST pin. The RESET pulse duration is 98xTOSC, where TOSC=1/FOSC. To make the best use of the WDT, it

should be serviced in those sections of code that will periodically be executed within the time required to prevent a WDT reset.

DT During wer-down d Idle

In Power-down mode the oscillator stops, which means the WDT also stops. While in Power-down mode, the user does not need to service the WDT. There are two methods of exiting Power-down mode: by a hardware reset or via a level-activated external interrupt, which is enabled prior to entering Power-down mode. When Power-down is exited with hardware reset, servicing the WDT should occur as it normally does whenever the AT89S51 is reset. Exiting Power-down with an interrupt is significantly different. The interrupt is held low long enough for the oscillator to stabilize. When the interrupt is brought high, the interrupt is serviced. To prevent the WDT from resetting the device while the interrupt pin is held low, the WDT is not started until the interrupt is pulled high. It is suggested that the WDT be reset during the interrupt service for the interrupt used to exit Power-down mode.

To ensure that the WDT does not overflow within a few states of exiting Power-down, it is best to reset the WDT just before entering Power-down mode.

Before going into the IDLE mode, the WDIDLE bit in SFR AUXR is used to determine whether the WDT continues to count if enabled. The WDT keeps counting during IDLE (WDIDLE bit = 0) as the default state. To prevent the WDT from resetting the AT89S51 while in IDLE mode, the user should always set up a timer that will periodically exit IDLE, service the WDT, and reenter IDLE mode.

With WDIDLE bit enabled, the WDT will stop to count in IDLE mode and resumes the count upon exit from IDLE.

RT

The UART in the AT89S51 operates the same way as the UART in the AT89C51. For further information on the UART operation, refer to the ATMEL Web site (http://www.atmel.com). From the home page, select 'Products', then '8051-Architecture Flash Microcontroller', then 'Product Overview'.

ıer 0 and 1

Timer 0 and Timer 1 in the AT89S51 operate the same way as Timer 0 and Timer 1 in the AT89C51. For further information on the timers' operation, refer to the ATMEL Web site (http://www.atmel.com). From the home page, select 'Products', then '8051-Architecture Flash Microcontroller', then 'Product Overview'.

ırrupts

The AT89S51 has a total of five interrupt vectors: two external interrupts ($\overline{INT0}$ and $\overline{INT1}$), two timer interrupts (Timers 0 and 1), and the serial port interrupt. These interrupts are all shown in Figure 1.

Each of these interrupt sources can be individually enabled or disabled by setting or clearing a bit in Special Function Register IE. IE also contains a global disable bit, EA, which disables all interrupts at once.

Note that Table 4 shows that bit position IE.6 is unimplemented. In the AT89S51, bit position IE.5 is also unimplemented. User software should not write 1s to these bit positions, since they may be used in future AT89 products.

The Timer 0 and Timer 1 flags, TF0 and TF1, are set at S5P2 of the cycle in which the timers overflow. The values are then polled by the circuitry in the next cycle

Table 4. Interrupt Enable (IE) Register

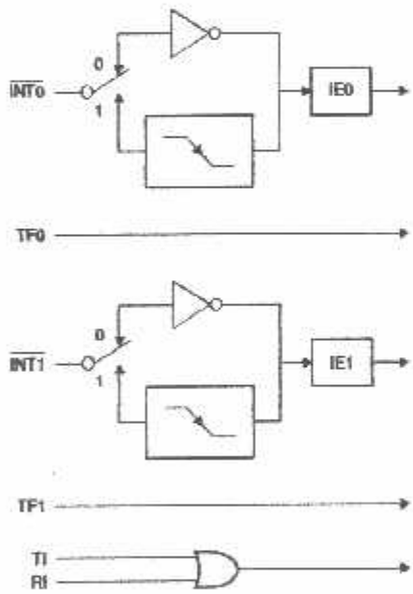
(MSB)							(LSB)
EA	–	–	ES	ET1	EX1	ET0	EX0

Enable Bit = 1 enables the interrupt.

Enable Bit = 0 disables the interrupt.

Symbol	Position	Function
EA	IE.7	Disables all interrupts. If EA = 0, no interrupt is acknowledged. If EA = 1, each interrupt source is individually enabled or disabled by setting or clearing its enable bit.
–	IE.6	Reserved
–	IE.5	Reserved
ES	IE.4	Serial Port interrupt enable bit
ET1	IE.3	Timer 1 interrupt enable bit
EX1	IE.2	External interrupt 1 enable bit
ET0	IE.1	Timer 0 interrupt enable bit
EX0	IE.0	External interrupt 0 enable bit
User software should never write 1s to reserved bits, because they may be used in future AT89 products.		

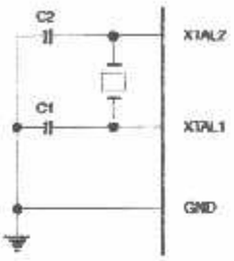
Figure 1. Interrupt Sources



ɔcillator ıaracteristics

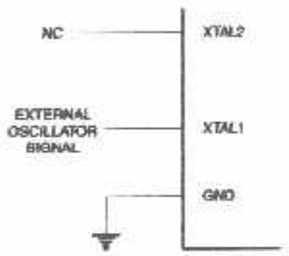
XTAL1 and XTAL2 are the input and output, respectively, of an inverting amplifier that can be configured for use as an on-chip oscillator, as shown in Figure 2. Either a quartz crystal or ceramic resonator may be used. To drive the device from an external clock source, XTAL2 should be left unconnected while XTAL1 is driven, as shown in Figure 3. There are no requirements on the duty cycle of the external clock signal, since the input to the internal clocking circuitry is through a divide-by-two flip-flop, but minimum and maximum voltage high and low time specifications must be observed.

Figure 2. Oscillator Connections



Note: C1, C2 = 30 pF ± 10 pF for Crystals = 40 pF ± 10 pF for Ceramic Resonators

Figure 3. External Clock Drive Configuration



Mode

In idle mode, the CPU puts itself to sleep while all the on-chip peripherals remain active. The mode is invoked by software. The content of the on-chip RAM and all the special function registers remain unchanged during this mode. The idle mode can be terminated by any enabled interrupt or by a hardware reset.

Note that when idle mode is terminated by a hardware reset, the device normally resumes program execution from where it left off, up to two machine cycles before the internal reset algorithm takes control. On-chip hardware inhibits access to internal RAM in this event, but access to the port pins is not inhibited. To eliminate the possibility of an unexpected write to a port pin when idle mode is terminated by a reset, the instruction following the one that invokes idle mode should not write to a port pin or to external memory.

ʻer-down le

In the Power-down mode, the oscillator is stopped, and the instruction that invokes Power-down is the last instruction executed. The on-chip RAM and Special Function Registers retain their values until the Power-down mode is terminated. Exit from Power-down mode can be initiated either by a hardware reset or by activation of an enabled external interrupt into $\overline{INT0}$ or $\overline{INT1}$. Reset redefines the SFRs but does not change the on-chip RAM. The reset should not be activated before V_{CC} is restored to its normal operating level and must be held active long enough to allow the oscillator to restart and stabilize.

Table 5. Status of External Pins During Idle and Power-down Modes

Mode	Program Memory	ALE	$\overline{PSEN}$	PORT0	PORT1	PORT2	PORT3
Idle	Internal	1	1	Data	Data	Data	Data
Idle	External	1	1	Float	Data	Address	Data
Power-down	Internal	0	0	Data	Data	Data	Data
Power-down	External	0	0	Float	Data	Data	Data

ɔgram emory Lock :s

The AT89S51 has three lock bits that can be left unprogrammed (U) or can be programmed (P) to obtain the additional features listed in the following table.

Table 6. Lock Bit Protection Modes

Program Lock Bits				
	LB1	LB2	LB3	Protection Type
1	U	U	U	No program lock features
2	P	U	U	MOVC instructions executed from external program memory are disabled from fetching code bytes from internal memory, $\overline{EA}$ is sampled and latched on reset, and further programming of the Flash memory is disabled
3	P	P	U	Same as mode 2, but verify is also disabled
4	P	P	P	Same as mode 3, but external execution is also disabled

When lock bit 1 is programmed, the logic level at the $\overline{EA}$ pin is sampled and latched during reset. If the device is powered up without a reset, the latch initializes to a random value and holds that value until reset is activated. The latched value of $\overline{EA}$ must agree with the current logic level at that pin in order for the device to function properly.

gramming Flash – allel Mode

The AT89S51 is shipped with the on-chip Flash memory array ready to be programmed. The programming interface needs a high-voltage (12-volt) program enable signal and is compatible with conventional third-party Flash or EPROM programmers.

The AT89S51 code memory array is programmed byte-by-byte.

Programming Algorithm: Before programming the AT89S51, the address, data, and control signals should be set up according to the Flash programming mode table and Figures 13 and 14. To program the AT89S51, take the following steps:

1. Input the desired memory location on the address lines.
2. Input the appropriate data byte on the data lines.
3. Activate the correct combination of control signals.
4. Raise $\overline{EA}/V_{PP}$ to 12V.
5. Pulse ALE/$\overline{PROG}$ once to program a byte in the Flash array or the lock bits. The byte-write cycle is self-timed and typically takes no more than 50 µs. Repeat steps 1 through 5, changing the address and data for the entire array or until the end of the object file is reached.

$\overline{Data}$ Polling: The AT89S51 features $\overline{Data}$ Polling to indicate the end of a byte write cycle. During a write cycle, an attempted read of the last byte written will result in the complement of the written data on P0.7. Once the write cycle has been completed, true data is valid on all outputs, and the next cycle may begin. $\overline{Data}$ Polling may begin any time after a write cycle has been initiated.

Ready/Busy: The progress of byte programming can also be monitored by the RDY/$\overline{BSY}$ output signal. P3.0 is pulled low after ALE goes high during programming to indicate $\overline{BUSY}$. P3.0 is pulled high again when programming is done to indicate READY.

Program Verify: If lock bits LB1 and LB2 have not been programmed, the programmed code data can be read back via the address and data lines for verification. The status of the individual lock bits can be verified directly by reading them back.

Reading the Signature Bytes: The signature bytes are read by the same procedure as a normal verification of locations 000H, 100H, and 200H, except that P3.6 and P3.7 must be pulled to a logic low. The values returned are as follows.

(000H) = 1EH indicates manufactured by Atmel
(100H) = 51H indicates 89S51
(200H) = 06H

Chip Erase: In the parallel programming mode, a chip erase operation is initiated by using the proper combination of control signals and by pulsing ALE/$\overline{PROG}$ low for a duration of 200 ns - 500 ns.

In the serial programming mode, a chip erase operation is initiated by issuing the Chip Erase instruction. In this mode, chip erase is self-timed and takes about 500 ms.

During chip erase, a serial read from any address location will return 00H at the data output.

›gramming · Flash – ·ial Mode

The Code memory array can be programmed using the serial ISP interface while RST is pulled to V_{cc}. The serial interface consists of pins SCK, MOSI (input) and MISO (output). After RST is set high, the Programming Enable instruction needs to be executed first before other operations can be executed. Before a reprogramming sequence can occur, a Chip Erase operation is required.

The Chip Erase operation turns the content of every memory location in the Code array into FFH.

Either an external system clock can be supplied at pin XTAL1 or a crystal needs to be connected across pins XTAL1 and XTAL2. The maximum serial clock (SCK) frequency should be less than 1/16 of the crystal frequency. With a 33 MHz oscillator clock, the maximum SCK frequency is 2 MHz.

al ›ramming ›rithm

To program and verify the AT89S51 in the serial programming mode, the following sequence is recommended:

1. Power-up sequence:
   Apply power between VCC and GND pins.
   Set RST pin to "H".
   If a crystal is not connected across pins XTAL1 and XTAL2, apply a 3 MHz to 33 MHz clock to XTAL1 pin and wait for at least 10 milliseconds.
2. Enable serial programming by sending the Programming Enable serial instruction to pin MOSI/P1.5. The frequency of the shift clock supplied at pin SCK/P1.7 needs to be less than the CPU clock at XTAL1 divided by 16.
3. The Code array is programmed one byte at a time in either the Byte or Page mode. The write cycle is self-timed and typically takes less than 0.5 ms at 5V.
4. Any memory location can be verified by using the Read instruction that returns the content at the selected address at serial output MISO/P1.6.
5. At the end of a programming session, RST can be set low to commence normal device operation.

Power-off sequence (if needed):

Set XTAL1 to "L" (if a crystal is not used).

Set RST to "L".

Turn V_{CC} power off.

Data Polling: The Data Polling feature is also available in the serial mode. In this mode, during a write cycle an attempted read of the last byte written will result in the complement of the MSB of the serial output byte on MISO.

ial gramming truction Set

The Instruction Set for Serial Programming follows a 4-byte protocol and is shown in Table 8 on page 18.

ogramming erface – rallel Mode

Every code byte in the Flash array can be programmed by using the appropriate combination of control signals. The write operation cycle is self-timed and once initiated, will automatically time itself to completion.

All major programming vendors offer worldwide support for the Atmel microcontroller series. Please contact your local programming vendor for the appropriate software revision.

a 7. Flash Programming Modes

e	V_{CC}	RST	PSEN	ALE/PROG	EA/V_{PP}	P2.6	P2.7	P3.3	P3.6	P3.7	P0.7-0 Data	P2.3-0 Address	P1.7-0 Address
e Code Data	5V	H	L	(2)	12V	L	H	H	H	H	D_{IN}	A11-8	A7-0
d Code Data	5V	H	L	H	H	L	L	L	H	H	D_{OUT}	A11-8	A7-0
e Lock Bit 1	5V	H	L	(3)	12V	H	H	H	H	H	X	X	X
e Lock Bit 2	5V	H	L	(3)	12V	H	H	H	L	L	X	X	X
e Lock Bit 3	5V	H	L	(3)	12V	H	L	H	H	L	X	X	X
e Lock Bits 3	5V	H	L	H	H	H	H	L	H	L	P0.2, P0.3, P0.4	X	X
Erase	5V	H	L	(1)	12V	H	L	H	L	L	X	X	X
Atmel ID	5V	H	L	H	H	L	L	L	L	L	1EH	0000	00H
Device ID	5V	H	L	H	H	L	L	L	L	L	51H	0001	00H
Device ID	5V	H	L	H	H	L	L	L	L	L	06H	0010	00H

1. Each PROG pulse is 200 ns - 500 ns for Chip Erase.
2. Each PROG pulse is 200 ns - 500 ns for Write Code Data.
3. Each PROG pulse is 200 ns - 500 ns for Write Lock Bits.
4. RDY/BSY signal is output on P3.0 during programming.
5. X = don't care.

Figure 4. Programming the Flash Memory (Parallel Mode)

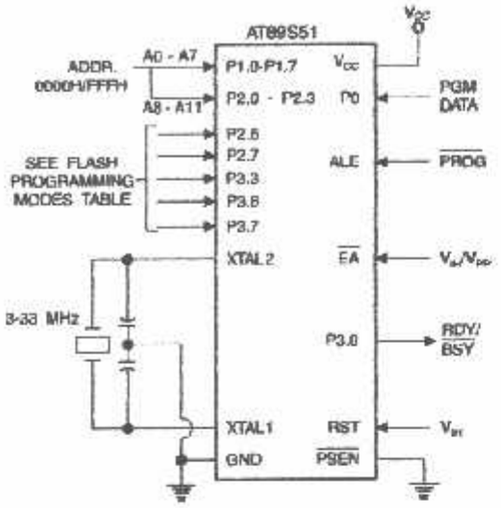
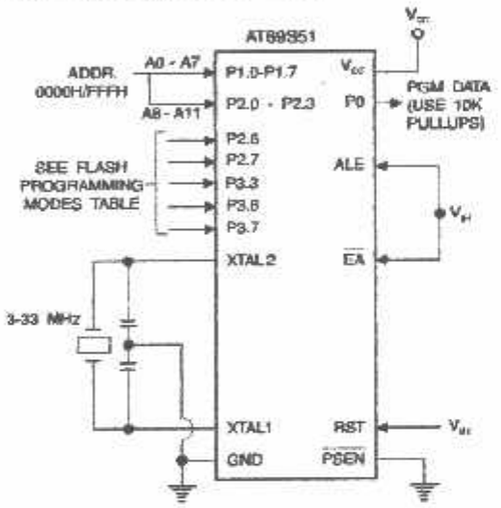


Figure 5. Verifying the Flash Memory (Parallel Mode)

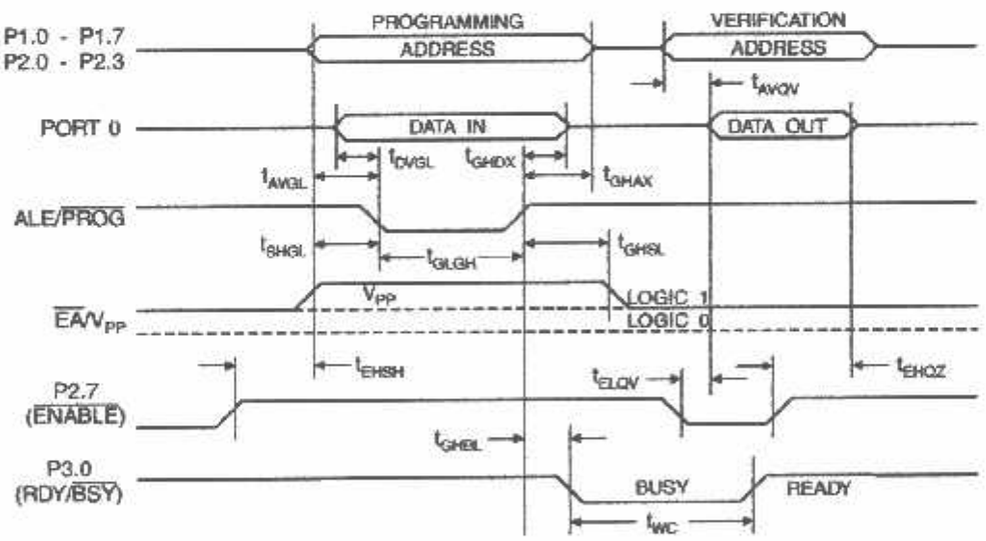


ash Programming and Verification Characteristics (Parallel Mode)

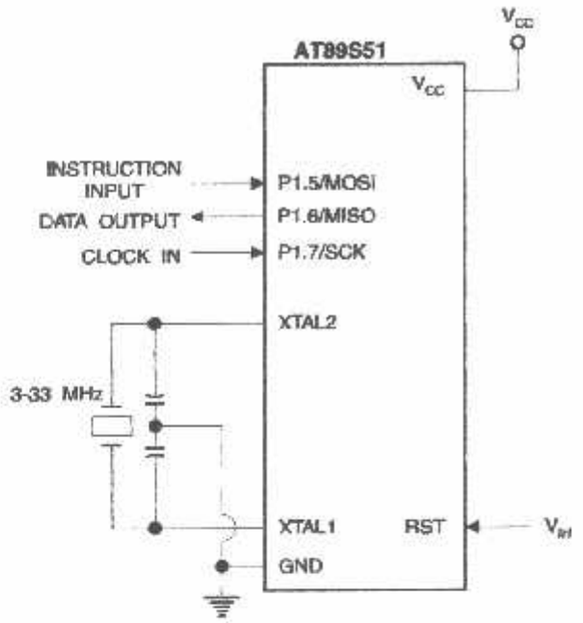
= 20°C to 30°C, V_{CC} = 4.5 to 5.5V

mbol	Parameter	Min	Max	Units
P	Programming Supply Voltage	11.5	12.5	V
	Programming Supply Current		10	mA
	V_{CC} Supply Current		30	mA
CLCL	Oscillator Frequency	3	33	MHz
VL	Address Setup to $\overline{PROG}$ Low	$48t_{CLCL}$		
AX	Address Hold After $\overline{PROG}$	$48t_{CLCL}$		
DVL	Data Setup to $\overline{PROG}$ Low	$48t_{CLCL}$		
DX	Data Hold After $\overline{PROG}$	$48t_{CLCL}$		
EHP	P2.7 ($\overline{ENABLE}$) High to V_{PP}	$48t_{CLCL}$		
PHL	V_{PP} Setup to $\overline{PROG}$ Low	10		µs
PLH	V_{PP} Hold After $\overline{PROG}$	10		µs
PLPH	$\overline{PROG}$ Width	0.2	1	µs
AV	Address to Data Valid		$48t_{CLCL}$	
LV	$\overline{ENABLE}$ Low to Data Valid		$48t_{CLCL}$	
HZ	Data Float After $\overline{ENABLE}$	0	$48t_{CLCL}$	
BVL	$\overline{PROG}$ High to $\overline{BUSY}$ Low		1.0	µs
WC	Byte Write Cycle Time		50	µs

re 6. Flash Programming and Verification Waveforms – Parallel Mode

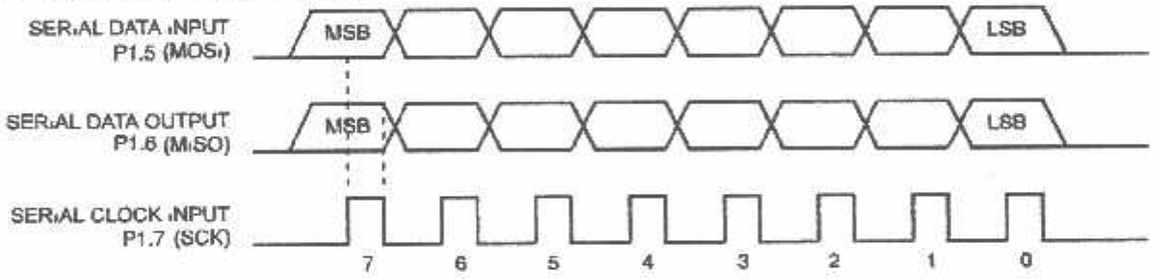


ure 7. Flash Memory Serial Downloading



sh Programming and Verification Waveforms – Serial Mode

re 8. Serial Programming Waveforms



le 8. Serial Programming Instruction Set

truction	Instruction Format Byte 1	Byte 2	Byte 3	Byte 4	Operation
ogramming Enable	1010 1100	0101 0011	xxxx xxxx	xxxx xxxx 0110 1001 (Output)	Enable Serial Programming while RST is high
ip Erase	1010 1100	100x xxxx	xxxx xxxx	xxxx xxxx	Chip Erase Flash memory array
ad Program Memory te Mode)	0010 0000	xxxx A11 A10 A9 A8	A7 A6 A5 A4 A3 A2 A1 A0	D7 D6 D5 D4 D3 D2 D1 D0	Read data from Program memory in the byte mode
te Program Memory te Mode)	0100 0000	xxxx A11 A10 A9 A8	A7 A6 A5 A4 A3 A2 A1 A0	D7 D6 D5 D4 D3 D2 D1 D0	Write data to Program memory in the byte mode
te Lock Bits[2]	1010 1100	1110 00 B1 B2	xxxx xxxx	xxxx xxxx	Write Lock bits. See Note (2).
ad Lock Bits	0010 0100	xxxx xxxx	xxxx xxxx	xx LB3 LB2 LB1 xx	Read back current status of the lock bits (a programmed lock bit reads back as a "1")
ad Signature Bytes[1]	0010 1000	xxx A5 A4 A3 A2 A1	A0 xxx xxxx	Signature Byte	Read Signature Byte
d Program Memory ge Mode)	0011 0000	xxxx A11 A10 A9 A8	Byte 0	Byte 1... Byte 255	Read data from Program memory in the Page Mode (256 bytes)
e Program Memory ge Mode)	0101 0000	xxxx A11 A10 A9 A8	Byte 0	Byte 1... Byte 255	Write data to Program memory in the Page Mode (256 bytes)

1. The signature bytes are not readable in Lock Bit Modes 3 and 4.
2. B1 = 0, B2 = 0 → Mode 1, no lock protection
   B1 = 0, B2 = 1 → Mode 2, lock bit 1 activated
   B1 = 1, B2 = 0 → Mode 3, lock bit 2 activated
   B1 = 1, B1 = 1 → Mode 4, lock bit 3 activated

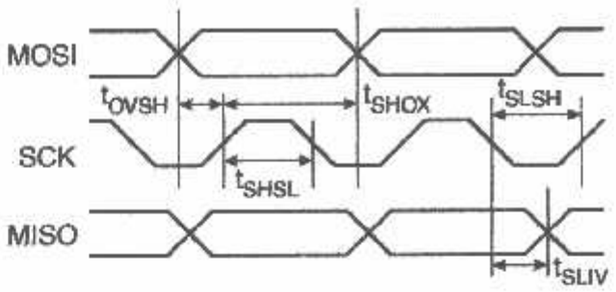
   } Each of the lock bits needs to be activated sequentially before Mode 4 can be executed.

After Reset signal is high, SCK should be low for at least 64 system clocks before it goes high to clock in the enable data bytes. No puleing of Reset signal is necessary. SCK should be no faster than 1/16 of the system clock at XTAL1.

For Page Read/Write, the data always starts from byte 0 to 255. After the command byte and upper address byte are latched, each byte thereafter is treated as data until all 256 bytes are shifted in/out. Then the next instruction will be ready to be decoded.

erial Programming Characteristics

igure 9. Serial Programming Timing



ble 9. Serial Programming Characteristics, T_A = -40°C to 85°C, V_{CC} = 4.0 - 5.5V (Unless Otherwise Noted)

ymbol	Parameter	Min	Typ	Max	Units
$^1/_{tCLCL}$	Oscillator Frequency	0		33	MHz
LCL	Oscillator Period	30			ns
HSL	SCK Pulse Width High	8 t_{CLCL}			ns
LSH	SCK Pulse Width Low	8 t_{CLCL}			ns
VSH	MOSI Setup to SCK High	t_{CLCL}			ns
HOX	MOSI Hold after SCK High	2 t_{CLCL}			ns
LIV	SCK Low to MISO Valid	10	16	32	ns
RASE	Chip Erase Instruction Cycle Time			500	ms
WC	Serial Byte Write Cycle Time			64 t_{CLCL} + 400	µs

ıbsolute Maximum Ratings*

ıerating Temperature	-55°C to +125°C
ɔrage Temperature	-65°C to +150°C
tage on Any Pin h Respect to Ground	-1.0V to +7.0V
ximum Operating Voltage	6.6V
Output Current	15.0 mA

*NOTICE: Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

: Characteristics

values shown in this table are valid for T_A = -40°C to 85°C and V_{CC} = 4.0V to 5.5V, unless otherwise noted.

nbol	Parameter	Condition	Min	Max	Units
	Input Low Voltage	(Except $\overline{EA}$)	-0.5	0.2 V_{CC}-0.1	V
	Input Low Voltage ($\overline{EA}$)		-0.5	0.2 V_{CC}-0.3	V
	Input High Voltage	(Except XTAL1, RST)	0.2 V_{CC}+0.9	V_{CC}+0.5	V
	Input High Voltage	(XTAL1, RST)	0.7 V_{CC}	V_{CC}+0.5	V
	Output Low Voltage[1] (Ports 1,2,3)	I_{OL} = 1.6 mA		0.45	V
	Output Low Voltage[1] (Port 0, ALE, $\overline{PSEN}$)	I_{OL} = 3.2 mA		0.45	V
	Output High Voltage (Ports 1,2,3, ALE, $\overline{PSEN}$)	I_{OH} = -60 µA, V_{CC} = 5V ± 10%	2.4		V
		I_{OH} = -25 µA	0.75 V_{CC}		V
		I_{OH} = -10 µA	0.9 V_{CC}		V
	Output High Voltage (Port 0 in External Bus Mode)	I_{OH} = -800 µA, V_{CC} = 5V ± 10%	2.4		V
		I_{OH} = -300 µA	0.75 V_{CC}		V
		I_{OH} = -80 µA	0.9 V_{CC}		V
	Logical 0 Input Current (Ports 1,2,3)	V_{IN} = 0.45V		-50	µA
	Logical 1 to 0 Transition Current (Ports 1,2,3)	V_{IN} = 2V, V_{CC} = 5V ± 10%		-650	µA
	Input Leakage Current (Port 0, $\overline{EA}$)	0.45 < V_{IN} < V_{CC}		±10	µA
T	Reset Pulldown Resistor		50	300	KΩ
	Pin Capacitance	Test Freq. = 1 MHz, T_A = 25°C		10	pF
	Power Supply Current	Active Mode, 12 MHz		25	mA
		Idle Mode, 12 MHz		6.5	mA
	Power-down Mode[2]	V_{CC} = 5.5V		50	µA

1. Under steady state (non-transient) conditions, I_{OL} must be externally limited as follows:
   Maximum I_{OL} per port pin: 10 mA
   Maximum I_{OL} per 8-bit port:
   Port 0: 26 mA Ports 1, 2, 3: 15 mA
   Maximum total I_{OL} for all output pins: 71 mA
   If I_{OL} exceeds the test condition, V_{OL} may exceed the related specification. Pins are not guaranteed to sink current greater than the listed test conditions.
2. Minimum V_{CC} for Power-down is 2V.

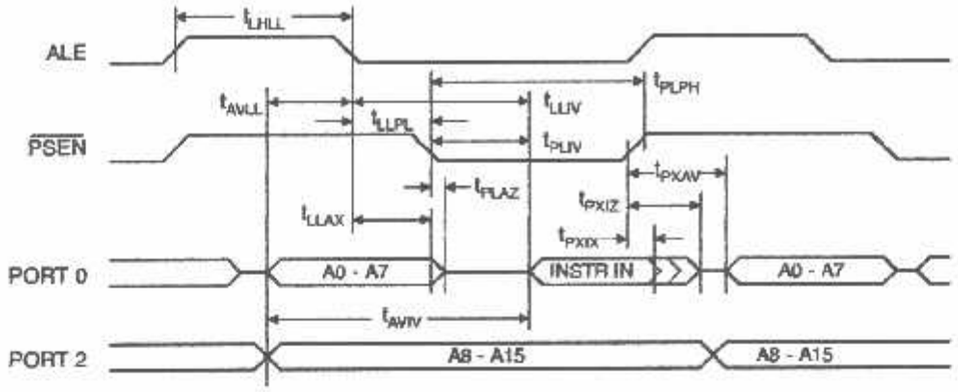
: Characteristics

ler operating conditions, load capacitance for Port 0, ALE/$\overline{PROG}$, and $\overline{PSEN}$ = 100 pF; load capacitance for all other uts = 80 pF.

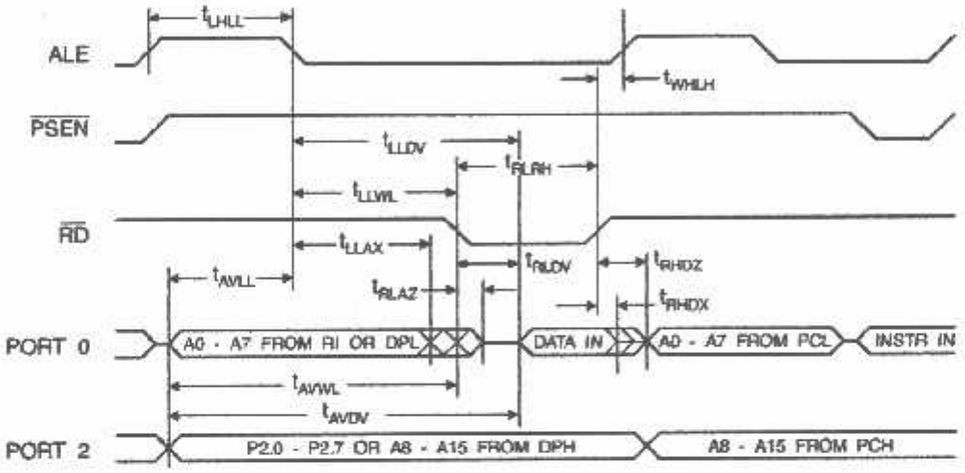
ternal Program and Data Memory Characteristics

mbol	Parameter	12 MHz Oscillator		Variable Oscillator		Units
		Min	Max	Min	Max	
LCL	Oscillator Frequency			0	33	MHz
L	ALE Pulse Width	127		$2t_{CLCL}$-40		ns
L	Address Valid to ALE Low	43		t_{CLCL}-25		ns
K	Address Hold After ALE Low	48		t_{CLCL}-25		ns
	ALE Low to Valid Instruction In		233		$4t_{CLCL}$-65	ns
	ALE Low to $\overline{PSEN}$ Low	43		t_{CLCL}-25		ns
H	$\overline{PSEN}$ Pulse Width	205		$3t_{CLCL}$-45		ns
	$\overline{PSEN}$ Low to Valid Instruction In		145		$3t_{CLCL}$-60	ns
	Input Instruction Hold After $\overline{PSEN}$	0		0		ns
	Input Instruction Float After $\overline{PSEN}$		59		t_{CLCL}-25	ns
	$\overline{PSEN}$ to Address Valid	75		t_{CLCL}-8		ns
	Address to Valid Instruction In		312		$5t_{CLCL}$-80	ns
	$\overline{PSEN}$ Low to Address Float		10		10	ns
	$\overline{RD}$ Pulse Width	400		$6t_{CLCL}$-100		ns
H	$\overline{WR}$ Pulse Width	400		$6t_{CLCL}$-100		ns
	$\overline{RD}$ Low to Valid Data In		252		$5t_{CLCL}$-90	ns
	Data Hold After $\overline{RD}$	0		0		ns
	Data Float After $\overline{RD}$		97		$2t_{CLCL}$-28	ns
	ALE Low to Valid Data In		517		$8t_{CLCL}$-150	ns
	Address to Valid Data In		585		$9t_{CLCL}$-165	ns
	ALE Low to $\overline{RD}$ or $\overline{WR}$ Low	200	300	$3t_{CLCL}$-50	$3t_{CLCL}$+50	ns
	Address to $\overline{RD}$ or $\overline{WR}$ Low	203		$4t_{CLCL}$-75		ns
	Data Valid to $\overline{WR}$ Transition	23		t_{CLCL}-30		ns
I	Data Valid to $\overline{WR}$ High	433		$7t_{CLCL}$-130		ns
	Data Hold After $\overline{WR}$	33		t_{CLCL}-25		ns
	$\overline{RD}$ Low to Address Float		0		0	ns
	$\overline{RD}$ or $\overline{WR}$ High to ALE High	43	123	t_{CLCL}-25	t_{CLCL}+25	ns

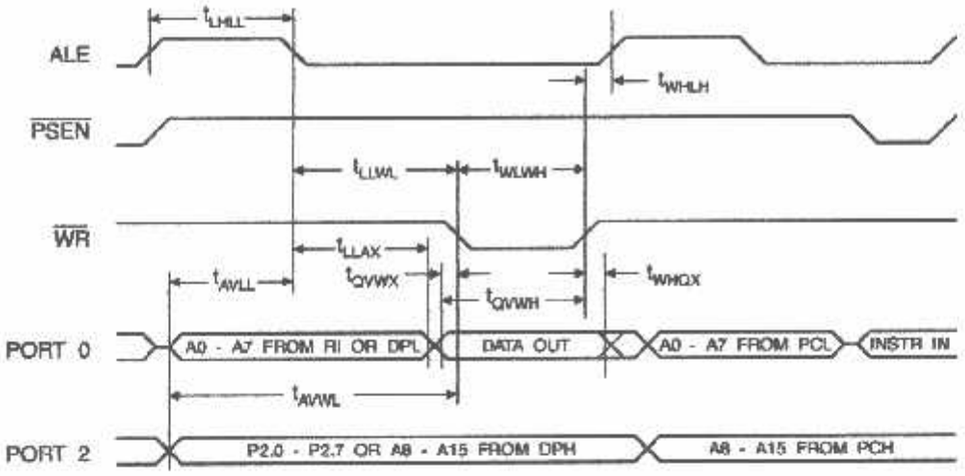
ternal Program Memory Read Cycle



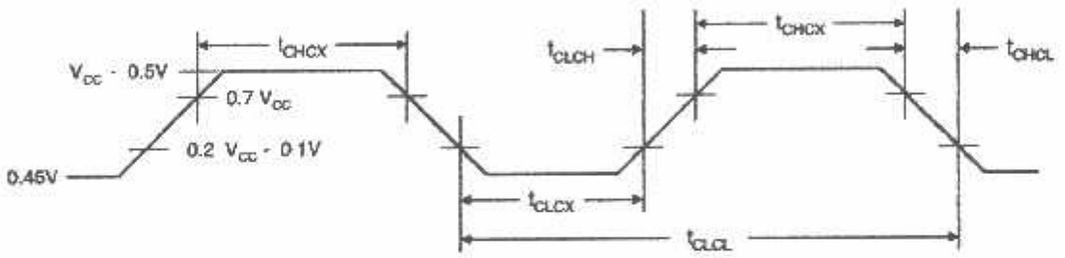
ernal Data Memory Read Cycle



ternal Data Memory Write Cycle



ernal Clock Drive Waveforms



ernal Clock Drive

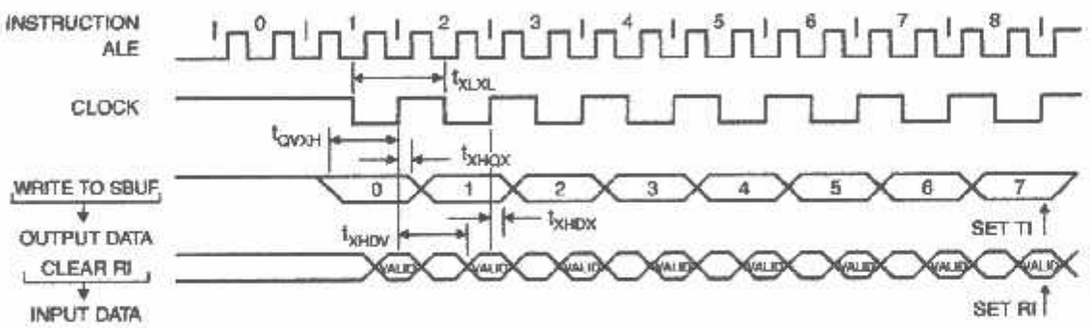
bol	Parameter	Min	Max	Units
CL	Oscillator Frequency	0	33	MHz
	Clock Period	30		ns
	High Time	12		ns
	Low Time	12		ns
	Rise Time		5	ns
	Fall Time		5	ns

rial Port Timing: Shift Register Mode Test Conditions

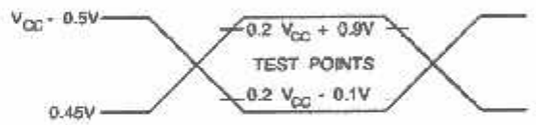
values in this table are valid for V_{CC} = 4.0V to 5.5V and Load Capacitance = 80 pF.

mbol	Parameter	12 MHz Osc		Variable Oscillator		Units
		Min	Max	Min	Max	
:L	Serial Port Clock Cycle Time	1.0		$12t_{CLCL}$		µs
QH	Output Data Setup to Clock Rising Edge	700		$10t_{CLCL}$-133		ns
QX	Output Data Hold After Clock Rising Edge	50		$2t_{CLCL}$-80		ns
XX	Input Data Hold After Clock Rising Edge	0		0		ns
IV	Clock Rising Edge to Input Data Valid		700		$10t_{CLCL}$-133	ns

ift Register Mode Timing Waveforms

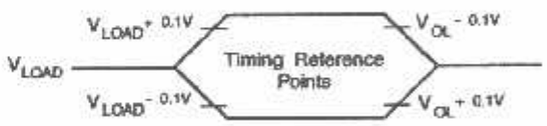


Testing Input/Output Waveforms[1]



1. AC Inputs during testing are driven at V_{CC} - 0.5V for a logic 1 and 0.45V for a logic 0. Timing measurements are made at V_{IH} min. for a logic 1 and V_{IL} max. for a logic 0.

it Waveforms[1]



1. For timing purposes, a port pin is no longer floating when a 100 mV change from load voltage occurs. A port pin begins to float when a 100 mV change from the loaded V_{OH}/V_{OL} level occurs.

dering Information

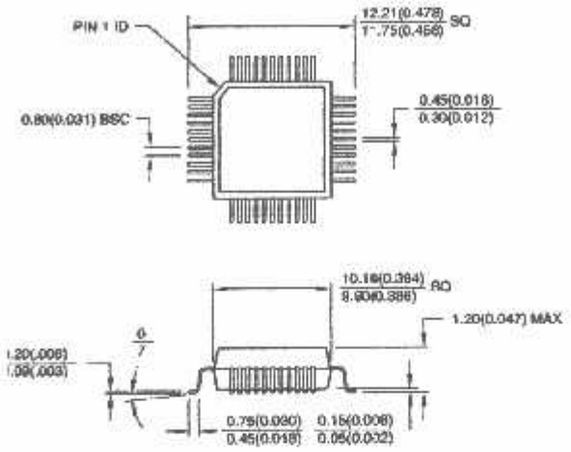
Speed (MHz)	Power Supply	Ordering Code	Package	Operation Range
24	4.0V to 5.5V	AT89S51-24AC AT89S51-24JC AT89S51-24PC	44A 44J 40P6	Commercial (0°C to 70°C)
		AT89S51-24AI AT89S51-24JI AT89S51-24PI	44A 44J 40P6	Industrial (-40°C to 85°C)
33	4.5V to 5.5V	AT89S51-33AC AT89S51-33JC AT89S51-33PC	44A 44J 40P6	Commercial (0°C to 70°C)

= Preliminary Availability

Package Type	
	44-lead, Thin Plastic Gull Wing Quad Flatpack (TQFP)
	44-lead, Plastic J-leaded Chip Carrier (PLCC)
	40-pin, 0.600" Wide, Plastic Dual Inline Package (PDIP)

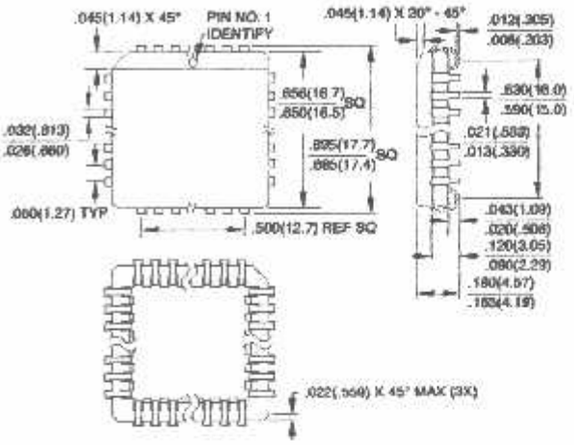
ckaging Information

44A, 44-lead, Thin (1.0 mm) Plastic Gull Wing Quad Flat Package (TQFP)
Dimensions in Millimeters and (Inches)*

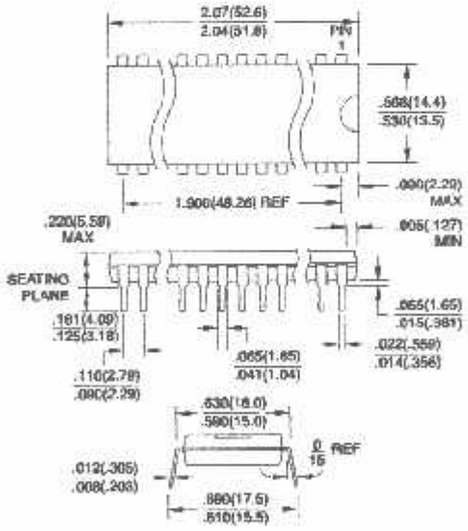


Controlling dimension: millimeters

44J, 44-lead, Plastic J-leaded Chip Carrier (PLCC)
Dimensions in Inches and (Millimeters)



0P6, 40-pin, 0.600" Wide, Plastic Dual Inline
ackage (PDIP)
imensions in Inches and (Millimeters)
EDEC STANDARD MS-011 AC



mel Headquarters

rporate Headquarters
325 Orchard Parkway
ian Jose, CA 95131
EL (408) 441-0311
AX (408) 487-2600

rope
tmel SarL
loute des Arsenaux 41
asa Postale 80
H-1705 Fribourg
witzerland
EL (41) 26-426-5555
AX (41) 26-426-5500

a
tmel Asia, Ltd.
oom 1219
hinachem Golden Plaza
7 Mody Road Tsimhatsui
ast Kowloon
ong Kong
EL (852) 2721-9778
AX (852) 2722-1369

an
mel Japan K.K.
, Tonetsu Shinkawa Bldg.
24-8 Shinkawa
uo-ku, Tokyo 104-0033
pan
EL (81) 3-3523-3551
X (81) 3-3523-7581

Atmel Product Operations

Atmel Colorado Springs
1150 E. Cheyenne Mtn. Blvd.
Colorado Springs, CO 80906
TEL (719) 576-3300
FAX (719) 540-1759

Atmel Grenoble
Avenue de Rochepleine
BP 123
38521 Saint-Egreve Cedex, France
TEL (33) 4-7658-3000
FAX (33) 4-7658-3480

Atmel Heilbronn
Theresienstrasse 2
POB 3535
D-74025 Heilbronn, Germany
TEL (49) 71 31 67 25 94
FAX (49) 71 31 67 24 23

Atmel Nantes
La Chantrerie
BP 70602
44306 Nantes Cedex 3, France
TEL (33) 0 2 40 18 18 18
FAX (33) 0 2 40 18 19 60

Atmel Rousset
Zone Industrielle
13106 Rousset Cedex, France
TEL (33) 4-4253-6000
FAX (33) 4-4253-6001

Atmel Smart Card ICs
Scottish Enterprise Technology Park
East Kilbride, Scotland G75 0QR
TEL (44) 1355-357-000
FAX (44) 1355-242-743

e-mail
literature@atmel.com

Web Site
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2487A–10/01/xM

Data Sheet

Light dependent resistors

NORP12 RS stock number 651-507
NSL19-M51 RS stock number 596-141

Two cadmium sulphide (cdS) photoconductive cells with spectral responses similar to that of the human eye. The cell resistance falls with increasing light intensity. Applications include smoke detection, automatic lighting control, batch counting and burglar alarm systems.

Guide to source illuminations

Light source	Illumination (Lux)
Moonlight	0.1
60W bulb at 1m	50
1W MES bulb at 0.1m	100
Fluorescent lighting	500
Bright sunlight	30,000

Circuit symbol

Light memory characteristics

Light dependent resistors have a particular property in that they remember the lighting conditions in which they have been stored. This memory effect can be minimised by storing the LDRs in light prior to use. Light storage reduces equilibrium time to reach steady resistance values.

NORP12 (RS stock no. 651-507)

Absolute maximum ratings

Voltage, ac or dc peak	320V
Current	75mA
Power dissipation at 30°C	250mW
Operating temperature range	-60°C to +75°C

Electrical characteristics

T_A = 25°C. 2854°K tungsten light source

Parameter	Conditions	Min.	Typ.	Max.	Units
Cell resistance	1000 lux	-	400	-	Ω
	10 lux	-	9	-	kΩ
Dark resistance	-	1.0	-	-	MΩ
Dark capacitance	-	-	3.5	-	pF
Rise time 1	1000 lux	-	2.8	-	ms
	10 lux	-	18	-	ms
Fall time 2	1000 lux	-	48	-	ms
	10 lux	-	120	-	ms

1. Dark to 110% R_L
2. To 10 × R_L
R_L = photocell resistance under given illumination.

Features

- Wide spectral response
- Low cost
- Wide ambient temperature range

Dimensions

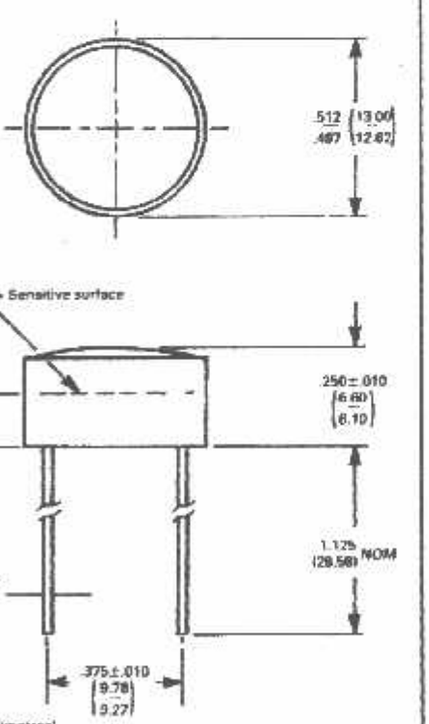


Figure 1 Power dissipation derating

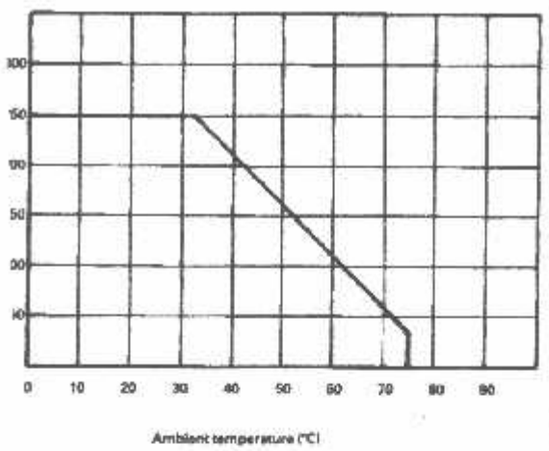
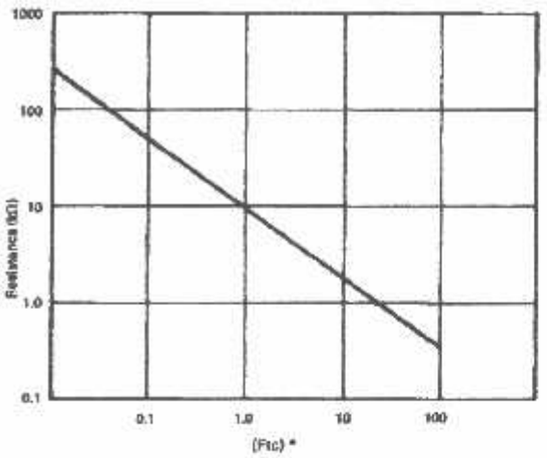
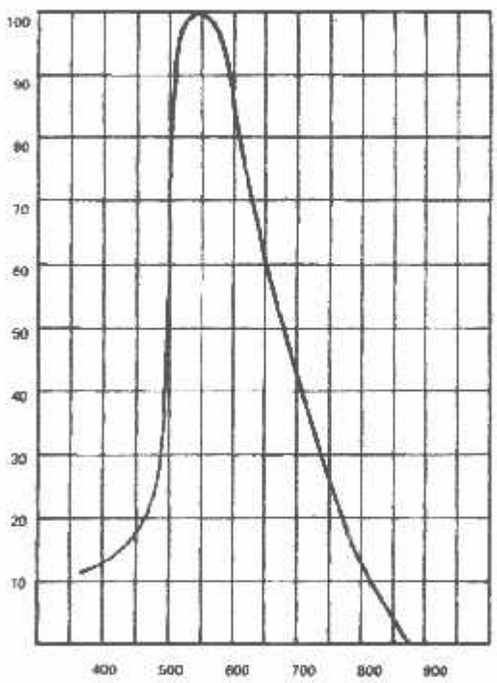


Figure 3 Resistance as a function of illumination



*1Ftc=10.764 lumens

gure 2 Spectral response



Absolute maximum ratings

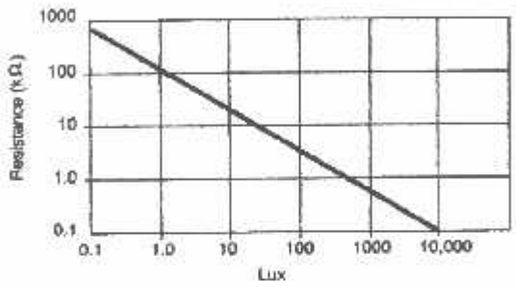
Voltage, ac or dc peak _____ 100V
Current _____ 5mA
Power dissipation at 25°C _____ 50mW*
Operating temperature range _____ -25°C +75°C

*Derate linearly from 50mW at 25°C to 0W at 75°C.

Electrical characteristics

Parameter	Conditions	Min.	Typ.	Max.	Units
Cell resistance	10 lux 100 lux	20 -	- 8	100 -	kΩ kΩ
Dark resistance	10 lux after 10 sec	20	-	-	MΩ
Spectral response	-	-	550	-	nm
Rise time	10ftc	-	45	-	ms
Fall time	10ftc	-	55	-	ms

Figure 4 Resistance as a function illumination



Dimensions

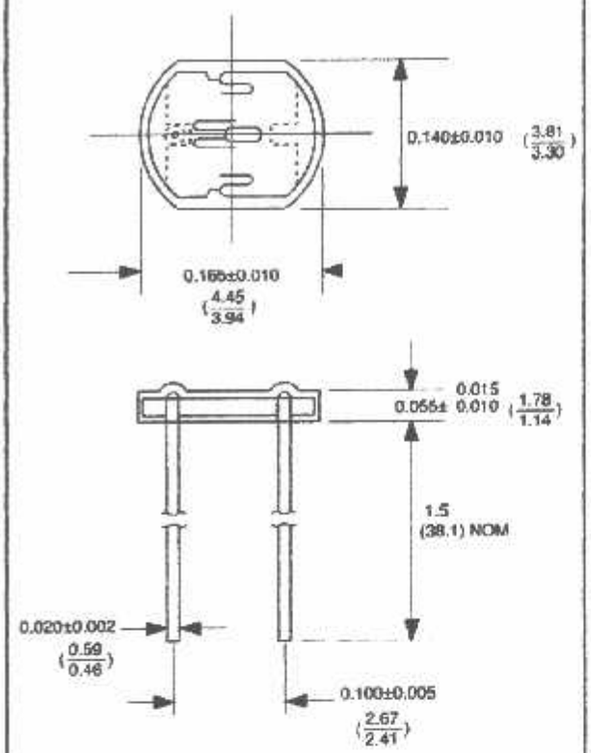
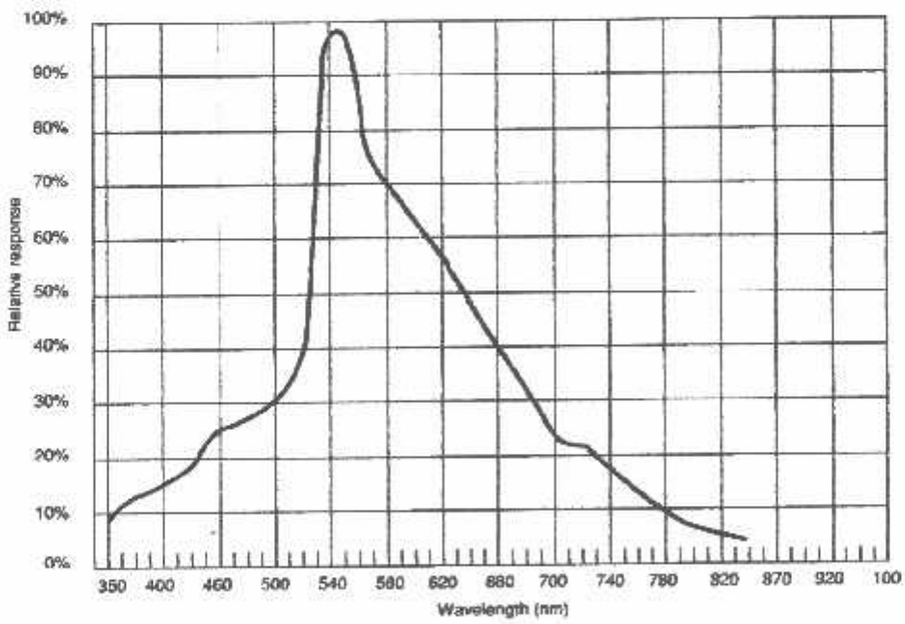
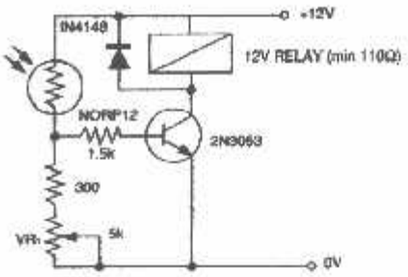


Figure 5 Spectral response



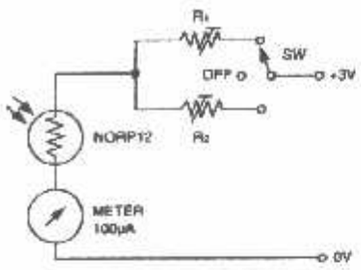
/pical application circuits

Figure 6 Sensitive light operated relay



elay energised when light level increases above the evel set by VR_1

Figure 9 Logarithmic law photographic light meter



Typical value $R^1 = 100k\Omega$
$R^2 = 200k\Omega$ preset to give two overlapping ranges.
(Calibration should be made against an accurate meter.)

Figure 7 Light interruption detector

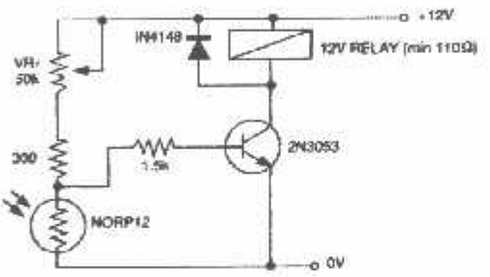
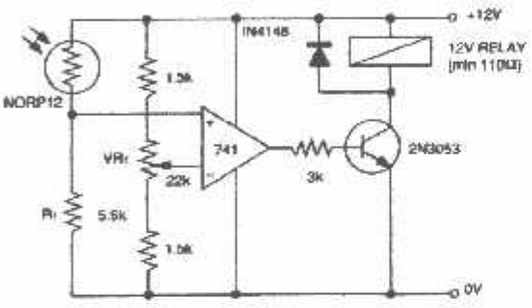


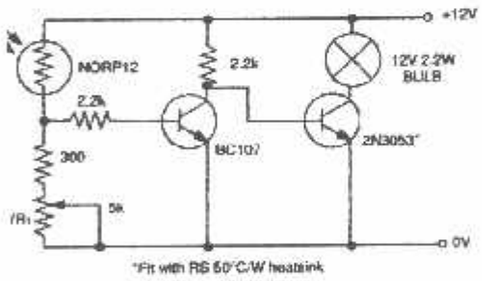
Figure 6 relay energised when light level drops low the level set by VR_1

Figure 10 Extremely sensitive light operated relay



(Relay energised when light exceeds preset level.)
Incorporates a balancing bridge and op-amp. R_1 and NORP12 may be interchanged for the reverse function.

Figure 8 Automatic light circuit



just turn-on point with VR_1

omponents, PO Box 99, Corby, Northants, NN17 9RS
An Electrocomponents Company
Telephone: 01536 201234

National Semiconductor

August 2000

LM386
Low Voltage Audio Power Amplifier

General Description

The LM386 is a power amplifier designed for use in low voltage consumer applications. The gain is internally set to 20 to keep external part count low, but the addition of an external resistor and capacitor between pins 1 and 8 will increase the gain to any value from 20 to 200.

The inputs are ground referenced while the output automatically biases to one-half the supply voltage. The quiescent power drain is only 24 milliwatts when operating from a 6 volt supply, making the LM386 ideal for battery operation.

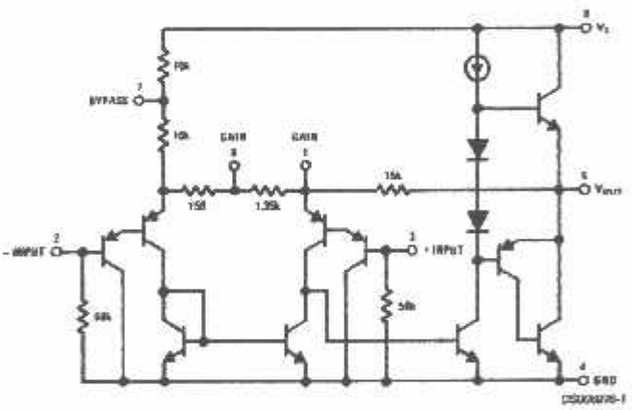
Features

- Battery operation
- Minimum external parts
- Wide supply voltage range: 4V–12V or 5V–18V
- Low quiescent current drain: 4mA
- Voltage gains from 20 to 200
- Ground referenced input
- Self-centering output quiescent voltage
- Low distortion: 0.2% (A_V = 20, V_S = 6V, R_L = 8Ω, P_O = 125mW, f = 1kHz)
- Available in 8 pin MSOP package

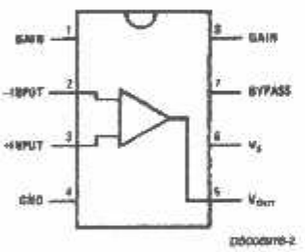
Applications

- AM-FM radio amplifiers
- Portable tape player amplifiers
- Intercoms
- TV sound systems
- Line drivers
- Ultrasonic drivers
- Small servo drivers
- Power converters

Equivalent Schematic and Connection Diagrams



Small Outline, Molded Mini Small Outline, and Dual-In-Line Packages



Top View
Order Number LM386M-1, LM386MM-1, LM386N-1, LM386N-3 or LM386N-4
See NS Package Number M08A, MUA08A or N08E

Absolute Maximum Ratings (Note 2)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Supply Voltage	
(LM386N-1, -3, LM386M-1)	15V
Supply Voltage (LM386N-4)	22V
Package Dissipation (Note 3)	
(LM386N)	1.25W
(LM386M)	0.73W
(LM386MM-1)	0.595W
Input Voltage	±0.4V
Storage Temperature	−65°C to +150°C
Operating Temperature	0°C to +70°C
Junction Temperature	+150°C
Soldering Information	
Dual-In-Line Package	
Soldering (10 sec)	+260°C
Small Outline Package	
(SOIC and MSOP)	
Vapor Phase (60 sec)	+215°C
Infrared (15 sec)	+220°C

See AN-450 "Surface Mounting Methods and Their Effect on Product Reliability" for other methods of soldering surface mount devices.

Thermal Resistance	
θ_{JC} (DIP)	37°C/W
θ_{JA} (DIP)	107°C/W
θ_{JC} (SO Package)	35°C/W
θ_{JA} (SO Package)	172°C/W
θ_{JA} (MSOP)	210°C/W
θ_{JC} (MSOP)	56°C/W

Electrical Characteristics (Notes 1, 2)

T_A = 25°C

Parameter	Conditions	Min	Typ	Max	Units
Operating Supply Voltage (V_S)					
LM386N-1, -3, LM386M-1, LM386MM-1		4		12	V
LM386N-4		5		18	V
Quiescent Current (I_Q)	V_S = 6V, V_{IN} = 0		4	8	mA
Output Power (P_{OUT})					
LM386N-1, LM386M-1, LM386MM-1	V_S = 6V, R_L = 8Ω, THD = 10%	250	325		mW
LM386N-3	V_S = 9V, R_L = 8Ω, THD = 10%	500	700		mW
LM386N-4	V_S = 16V, R_L = 32Ω, THD = 10%	700	1000		mW
Voltage Gain (A_V)	V_S = 6V, f = 1 kHz		26		dB
	10 µF from Pin 1 to 8		46		dB
Bandwidth (BW)	V_S = 6V, Pins 1 and 8 Open		300		kHz
Total Harmonic Distortion (THD)	V_S = 6V, R_L = 8Ω, P_{OUT} = 125 mW		0.2		%
	f = 1 kHz, Pins 1 and 8 Open				
Power Supply Rejection Ratio (PSRR)	V_S = 6V, f = 1 kHz, C_{BYPASS} = 10 µF		50		dB
	Pins 1 and 8 Open, Referred to Output				
Input Resistance (R_{IN})			50		kΩ
Input Bias Current (I_{BIAS})	V_S = 6V, Pins 2 and 3 Open		250		nA

Note 1: All voltages are measured with respect to the ground pin, unless otherwise specified.

Note 2: Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is functional, but do not guarantee specific performance limits. Electrical Characteristics state DC and AC electrical specifications under particular test conditions which guarantee specific performance limits. This assumes that the device is within the Operating Ratings. Specifications are not guaranteed for parameters where no limit is given, however, the typical value is a good indication of device performance.

Note 3: For operation in ambient temperatures above 25°C, the device must be derated based on a 150°C maximum junction temperature and 1) a thermal resistance of 107°C/W junction to ambient for the dual-in-line package and 2) a thermal resistance of 170°C/W for the small outline package.

Application Hints

GAIN CONTROL

To make the LM386 a more versatile amplifier, two pins (1 and 8) are provided for gain control. With pins 1 and 8 open the 1.35 kΩ resistor sets the gain at 20 (26 dB). If a capacitor is put from pin 1 to 8, bypassing the 1.35 kΩ resistor, the gain will go up to 200 (46 dB). If a resistor is placed in series with the capacitor, the gain can be set to any value from 20 to 200. Gain control can also be done by capacitively coupling a resistor (or FET) from pin 1 to ground.

Additional external components can be placed in parallel with the internal feedback resistors to tailor the gain and frequency response for individual applications. For example, we can compensate poor speaker bass response by frequency shaping the feedback path. This is done with a series RC from pin 1 to 5 (paralleling the internal 15 kΩ resistor). For 6 dB effective bass boost: R ≈ 15 kΩ, the lowest value for good stable operation is R = 10 kΩ if pin 8 is open. If pins 1 and 8 are bypassed then R as low as 2 kΩ can be used. This restriction is because the amplifier is only compensated for closed-loop gains greater than 9.

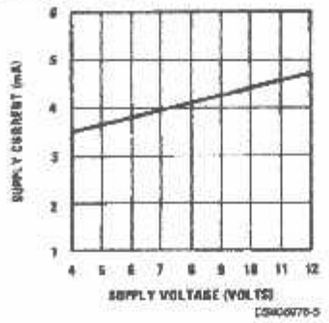
INPUT BIASING

The schematic shows that both inputs are biased to ground with a 50 kΩ resistor. The base current of the input transistors is about 250 nA, so the inputs are at about 12.5 mV when left open. If the dc source resistance driving the LM386 is higher than 250 kΩ it will contribute very little additional offset (about 2.5 mV at the input, 50 mV at the output). If the dc source resistance is less than 10 kΩ, then shorting the unused input to ground will keep the offset low (about 2.5 mV at the input, 50 mV at the output). For dc source resistances between these values we can eliminate excess offset by putting a resistor from the unused input to ground, equal in value to the dc source resistance. Of course all offset problems are eliminated if the input is capacitively coupled.

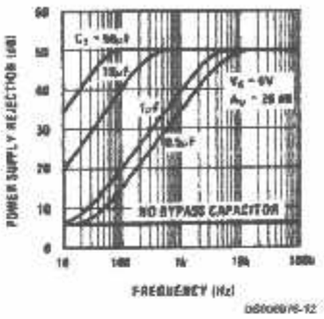
When using the LM386 with higher gains (bypassing the 1.35 kΩ resistor between pins 1 and 8) it is necessary to bypass the unused input, preventing degradation of gain and possible instabilities. This is done with a 0.1 µF capacitor or a short to ground depending on the dc source resistance on the driven input.

Typical Performance Characteristics

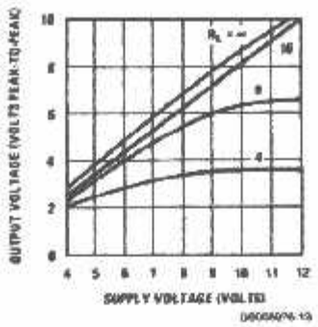
Quiescent Supply Current vs Supply Voltage



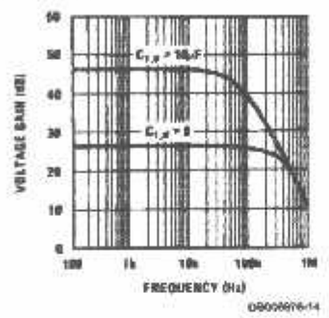
Power Supply Rejection Ratio (Referred to the Output) vs Frequency



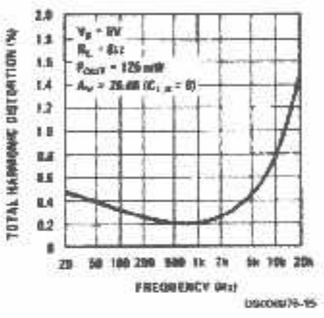
Peak-to-Peak Output Voltage Swing vs Supply Voltage



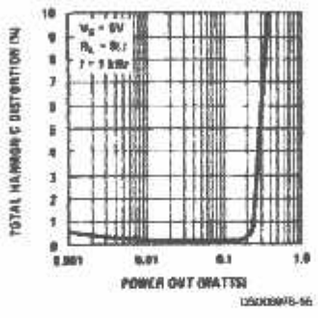
Voltage Gain vs Frequency



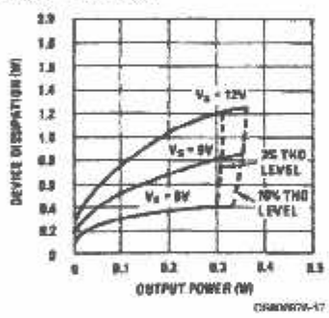
Distortion vs Frequency



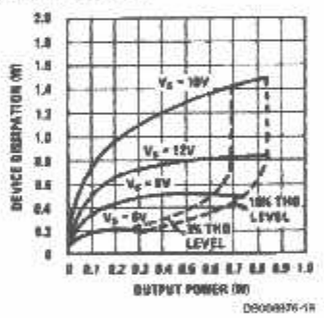
Distortion vs Output Power



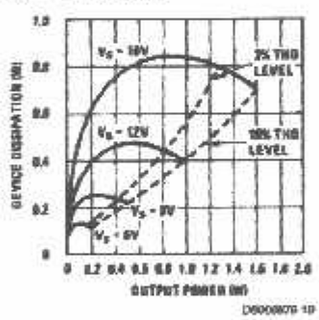
Device Dissipation vs Output Power—4Ω Load



Device Dissipation vs Output Power—8Ω Load

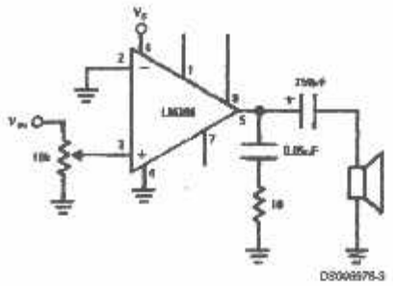


Device Dissipation vs Output Power—16Ω Load

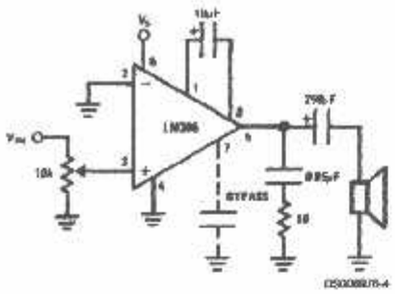


Typical Applications

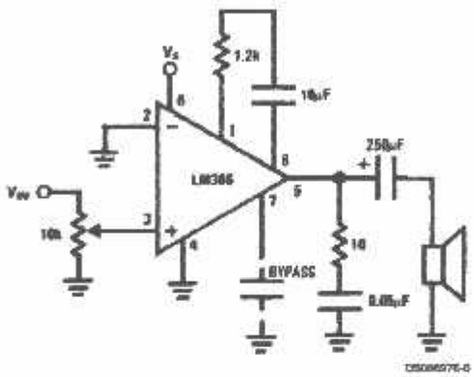
Amplifier with Gain = 20 Minimum Parts



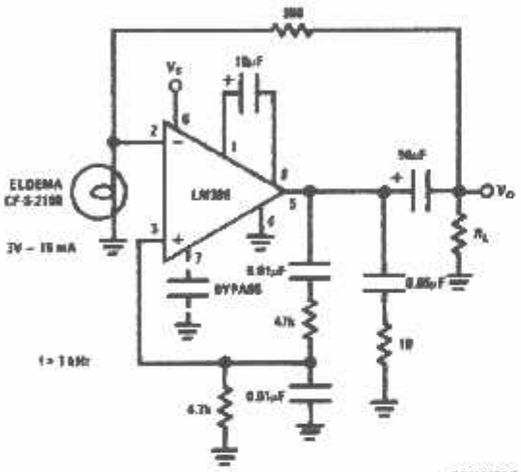
Amplifier with Gain = 200



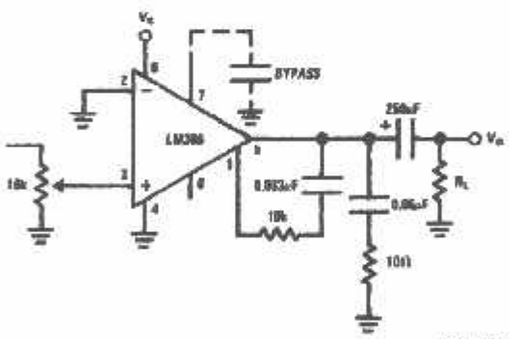
Amplifier with Gain = 50



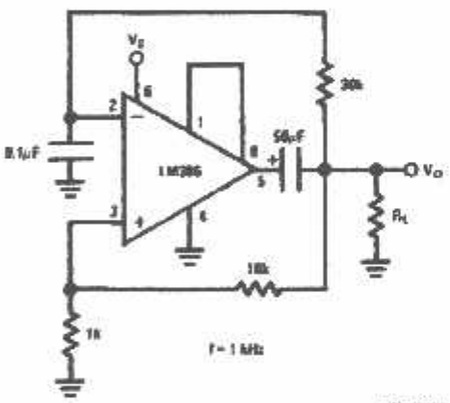
Low Distortion Power Wienbridge Oscillator



Amplifier with Bass Boost

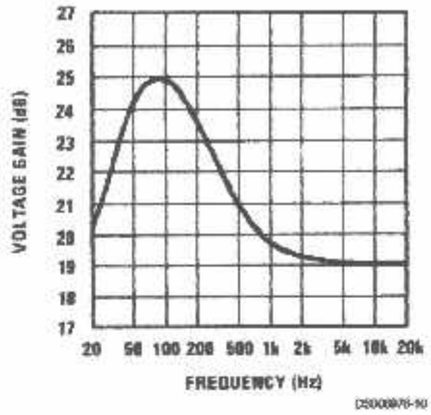


Square Wave Oscillator



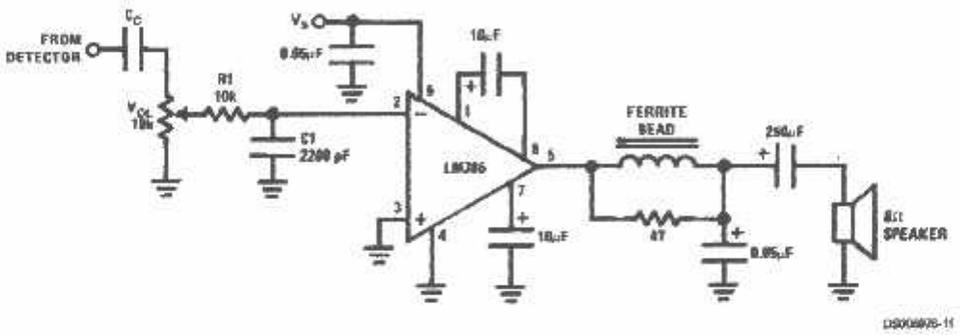
Typical Applications (Continued)

Frequency Response with Bass Boost



D5000976-10

AM Radio Power Amplifier



D5000976-11

Note 4: Twist Supply lead and supply ground very tightly.

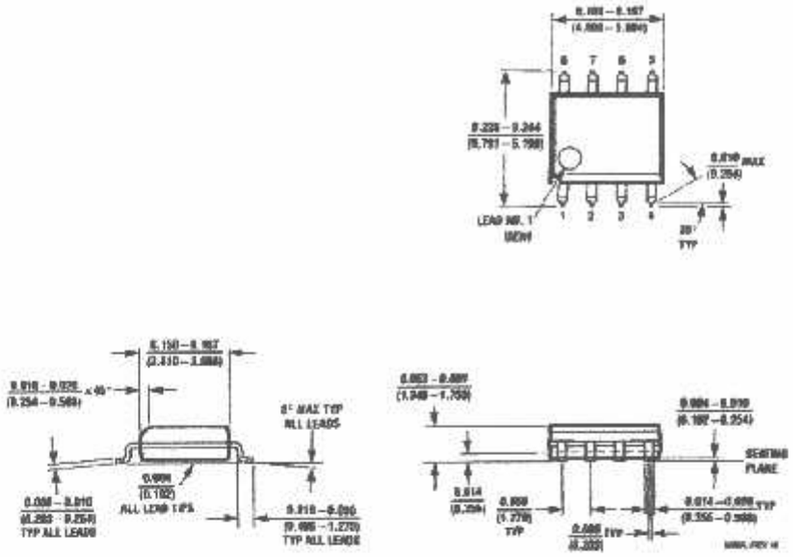
Note 5: Twist speaker lead and ground very tightly.

Note 6: Ferrite bead in Ferroxcube K5-001-001/3B with 3 turns of wire.

Note 7: R1C1 band limits input signals.

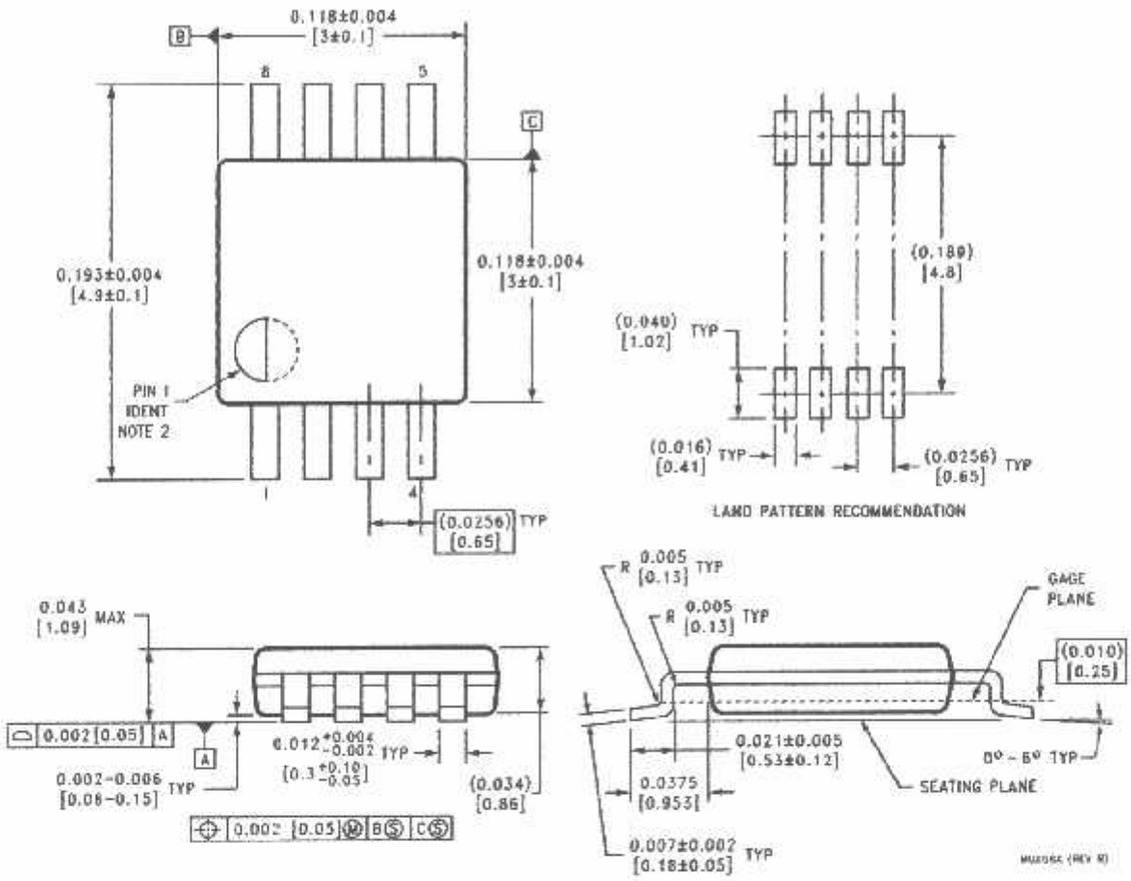
Note 8: All components must be spaced very closely to IC.

Physical Dimensions inches (millimeters) unless otherwise noted



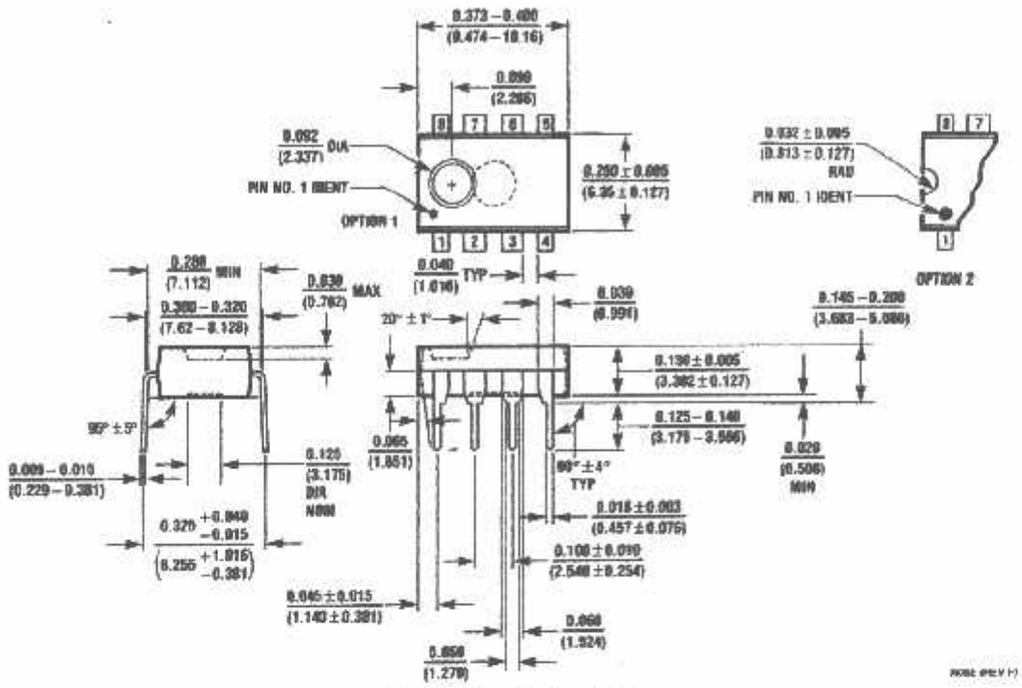
SO Package (M)
Order Number LM386M-1
NS Package Number M08A

Physical Dimensions inches (millimeters) unless otherwise noted (Continued)



8-Lead (0.118" Wide) Molded Mini Small Outline Package
Order Number LM386MM-1
NS Package Number MUA08A

Physical Dimensions inches (millimeters) unless otherwise noted (Continued)



Dual-In-Line Package (N)
Order Number LM386N-1, LM386N-3 or LM386N-4
NS Package Number N08E

E SUPPORT POLICY

TIONAL'S PRODUCTS ARE NOT AUTHORIZED FOR USE AS CRITICAL COMPONENTS IN LIFE SUPPORT VICES OR SYSTEMS WITHOUT THE EXPRESS WRITTEN APPROVAL OF THE PRESIDENT AND GENERAL UNSEL OF NATIONAL SEMICONDUCTOR CORPORATION. As used herein:

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Email: europe.support@nsc.com
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DATA SHEET

PCF8591
8-bit A/D and D/A converter

roduct specification
upersedes data of 1997 Apr 02
ile under Integrated Circuits, IC12

1998 Jul 02

ilips
miconductors

PHILIPS

ONTENTS

FEATURES

Single power supply

Operating supply voltage 2.5 V to 6 V

Low standby current

Serial input/output via I^2C-bus

Address by 3 hardware address pins

Sampling rate given by I^2C-bus speed

4 analog inputs programmable as single-ended or differential inputs

Auto-incremented channel selection

Analog voltage range from V_{SS} to V_{DD}

On-chip track and hold circuit

8-bit successive approximation A/D conversion

Multiplying DAC with one analog output.

APPLICATIONS

Closed loop control systems

Low power converter for remote data acquisition

Battery operated equipment

Acquisition of analog values in automotive, audio and TV applications.

3 GENERAL DESCRIPTION

The PCF8591 is a single-chip, single-supply low power 8-bit CMOS data acquisition device with four analog inputs, one analog output and a serial I^2C-bus interface. Three address pins A0, A1 and A2 are used for programming the hardware address, allowing the use of up to eight devices connected to the I^2C-bus without additional hardware. Address, control and data to and from the device are transferred serially via the two-line bidirectional I^2C-bus.

The functions of the device include analog input multiplexing, on-chip track and hold function, 8-bit analog-to-digital conversion and an 8-bit digital-to-analog conversion. The maximum conversion rate is given by the maximum speed of the I^2C-bus.

ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
CA8591P	DIP16	plastic dual in-line package; 16 leads (300 mil); long body	SOT38-1
CA8591T	SO16	plastic small outline package; 16 leads; body width 7.5 mm	SOT162-1

5 BLOCK DIAGRAM

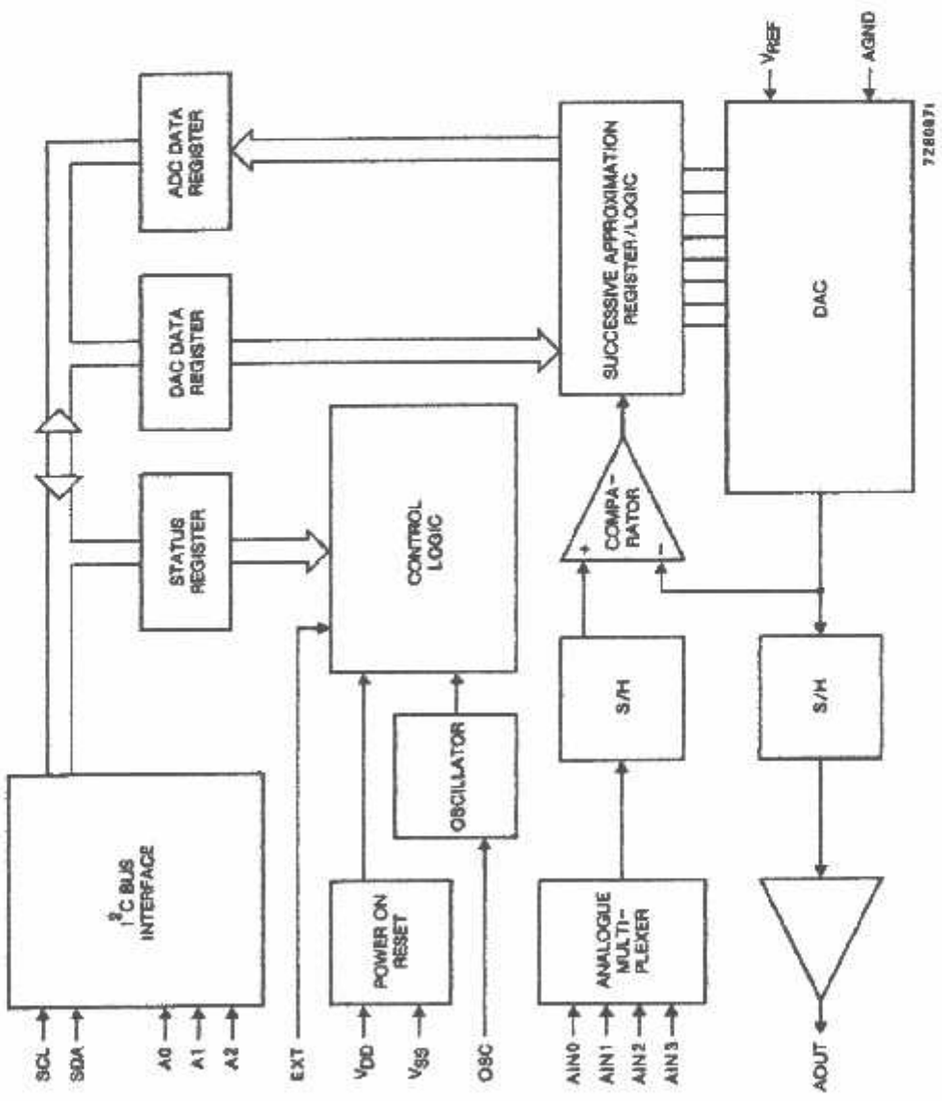


Fig.1 Block diagram.

PINNING

SYMBOL	PIN	DESCRIPTION
AIN0	1	analog inputs (A/D converter)
AIN1	2	
AIN2	3	
AIN3	4	
A0	5	hardware address
A1	6	
A2	7	
VSS	8	negative supply voltage
SDA	9	I²C-bus data input/output
SCL	10	I²C-bus clock input
OSC	11	oscillator input/output
EXT	12	external/internal switch for oscillator input
AGND	13	analog ground
VREF	14	voltage reference input
AOUT	15	analog output (D/A converter)
VDD	16	positive supply voltage

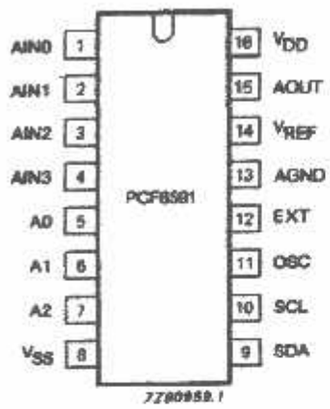


Fig.2 Pinning diagram.

FUNCTIONAL DESCRIPTION

1 Addressing

ach PCF8591 device in an I²C-bus system is activated by nding a valid address to the device. The address nsists of a fixed part and a programmable part. ie programmable part must be set according to the ldress pins A0, A1 and A2. The address always has to sent as the first byte after the start condition in the C-bus protocol. The last bit of the address byte is the ad/write-bit which sets the direction of the following data nsfer (see Figs 3, 15 and 16).

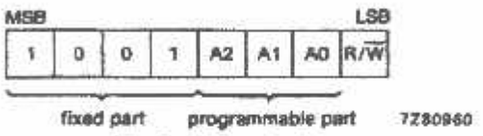


Fig.3 Address byte.

7.2 Control byte

The second byte sent to a PCF8591 device will be stored in its control register and is required to control the device function.

The upper nibble of the control register is used for enabling the analog output, and for programming the analog inputs as single-ended or differential inputs. The lower nibble selects one of the analog input channels defined by the upper nibble (see Fig.4). If the auto-increment flag is set the channel number is incremented automatically after each A/D conversion.

If the auto-increment mode is desired in applications where the internal oscillator is used, the analog output enable flag in the control byte (bit 6) should be set. This allows the internal oscillator to run continuously, thereby preventing conversion errors resulting from oscillator start-up delay. The analog output enable flag may be reset at other times to reduce quiescent power consumption.

The selection of a non-existing input channel results in the highest available channel number being allocated. Therefore, if the auto-increment flag is set, the next selected channel will be always channel 0. The most significant bits of both nibbles are reserved for future functions and have to be set to 0. After a Power-on reset condition all bits of the control register are reset to 0. The D/A converter and the oscillator are disabled for power saving. The analog output is switched to a high-impedance state.

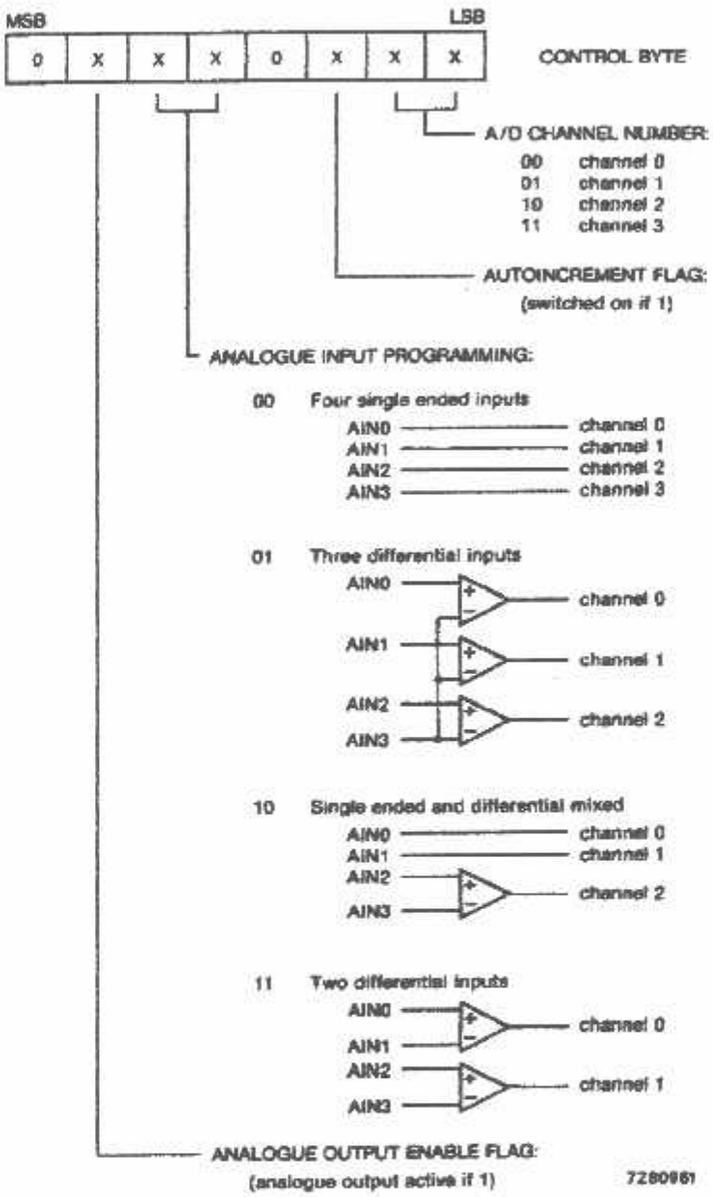


Fig.4 Control byte.

3 D/A conversion

ıe third byte sent to a PCF8591 device is stored in the AC data register and is converted to the corresponding ıalog voltage using the on-chip D/A converter. This D/A ınverter consists of a resistor divider chain connected to e external reference voltage with 256 taps and selection vitches. The tap-decoder switches one of these taps to e DAC output line (see Fig.5).

ıe analog output voltage is buffered by an auto-zeroed ılty gain amplifier. This buffer amplifier may be switched or off by setting the analog output enable flag of the ntrol register. In the active state the output voltage is ld until a further data byte is sent.

The on-chip D/A converter is also used for successive approximation A/D conversion. In order to release the DAC for an A/D conversion cycle the unity gain amplifier is equipped with a track and hold circuit. This circuit holds the output voltage while executing the A/D conversion.

The output voltage supplied to the analog output AOUT is given by the formula shown in Fig.6. The waveforms of a D/A conversion sequence are shown in Fig.7.

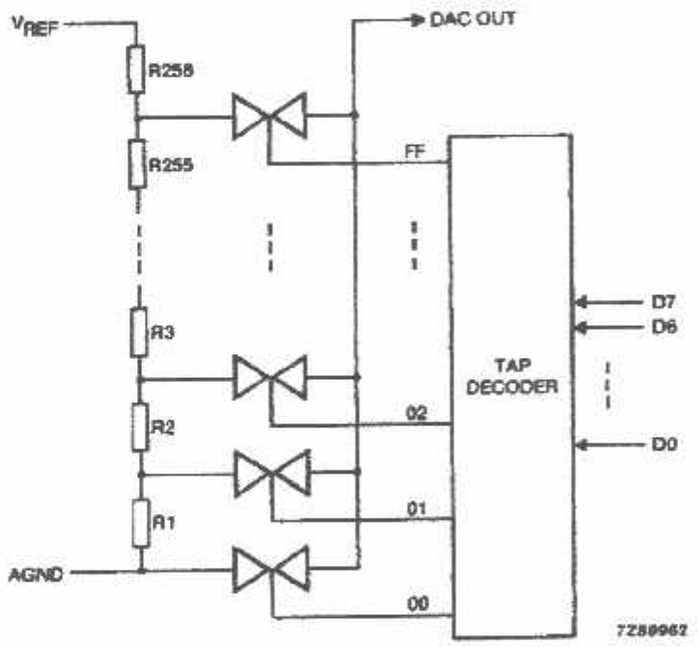


Fig.5 DAC resistor divider chain.

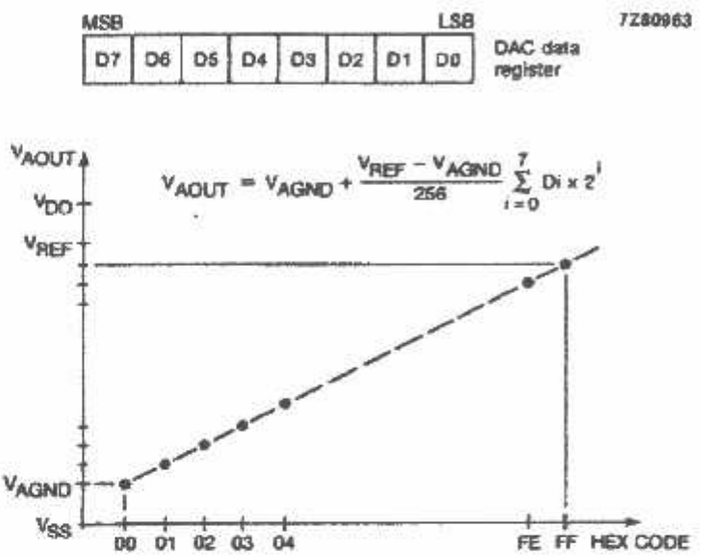


Fig.6 DAC data and DC conversion characteristics.

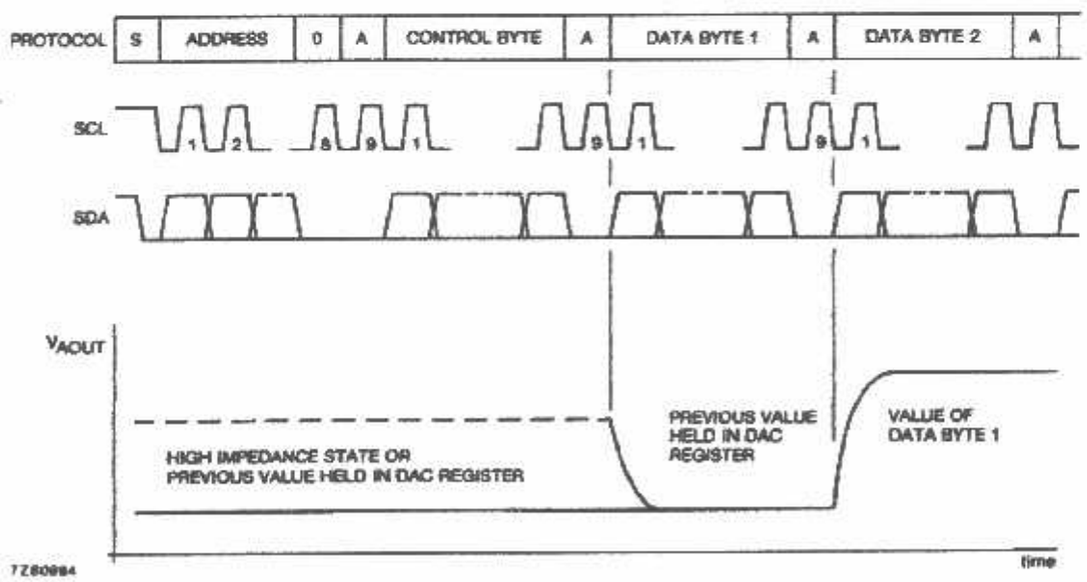


Fig.7 D/A conversion sequence.

4 A/D conversion

ıe A/D converter makes use of the successive ɔproximation conversion technique. The on-chip D/A ınverter and a high-gain comparator are used mporarily during an A/D conversion cycle.

ı A/D conversion cycle is always started after sending a lid read mode address to a PCF8591 device. The A/D nversion cycle is triggered at the trailing edge of the knowledge clock pulse and is executed while ınsmitting the result of the previous conversion (see ɜ.8).

ıce a conversion cycle is triggered an input voltage mple of the selected channel is stored on the chip and is nverted to the corresponding 8-bit binary code. Samples ked up from differential inputs are converted to an 8-bit ɔ's complement code (see Figs 9 and 10).

The conversion result is stored in the ADC data register and awaits transmission. If the auto-increment flag is set the next channel is selected.

The first byte transmitted in a read cycle contains the conversion result code of the previous read cycle. After a Power-on reset condition the first byte read is a hexadecimal 80. The protocol of an I²C-bus read cycle is shown in Chapter 8, Figs 15 and 16.

The maximum A/D conversion rate is given by the actual speed of the I²C-bus.

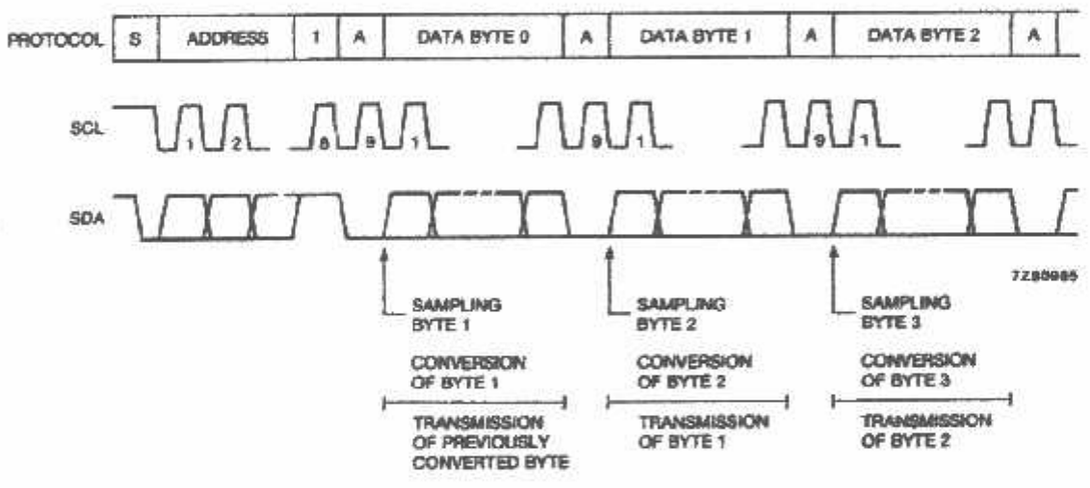


Fig.8 A/D conversion sequence.

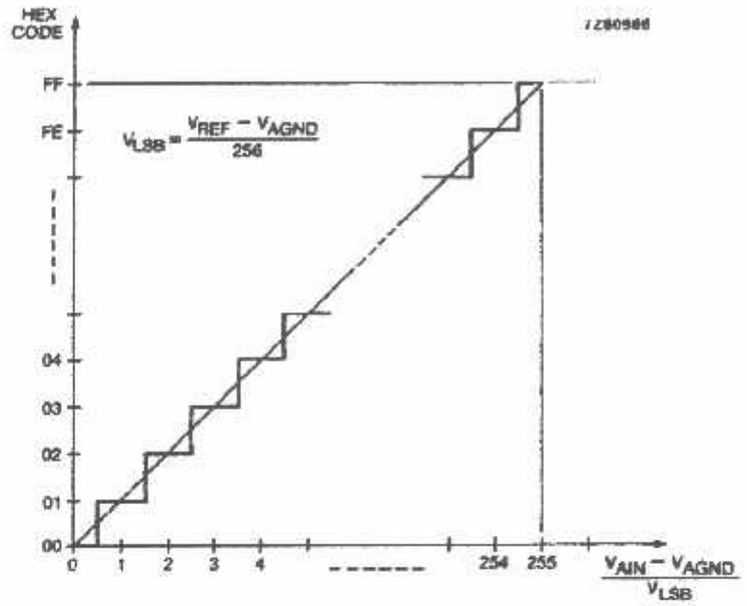


Fig.9 A/D conversion characteristics of single-ended inputs.

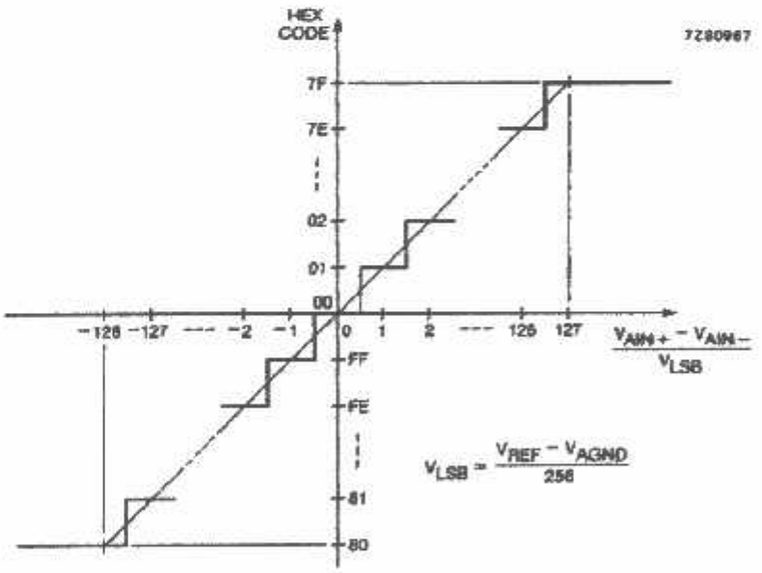


Fig.10 A/D conversion characteristics of differential inputs.

5 Reference voltage

or the D/A and A/D conversion either a stable external oltage reference or the supply voltage has to be applied the resistor divider chain (pins V_{REF} and AGND). ie AGND pin has to be connected to the system analog ound and may have a DC off-set with reference to V_{SS}.

low frequency may be applied to the V_{REF} and AGND ns. This allows the use of the D/A converter as a ie-quadrant multiplier; see Chapter 15 and Fig.6.

ie A/D converter may also be used as a one or two adrant analog divider. The analog input voltage is ided by the reference voltage. The result is converted to inary code. In this application the user has to keep the erence voltage stable during the conversion cycle.

7.6 Oscillator

An on-chip oscillator generates the clock signal required for the A/D conversion cycle and for refreshing the auto-zeroed buffer amplifier. When using this oscillator the EXT pin has to be connected to V_{SS}. At the OSC pin the oscillator frequency is available.

If the EXT pin is connected to V_{DD} the oscillator output OSC is switched to a high-impedance state allowing the user to feed an external clock signal to OSC.

CHARACTERISTICS OF THE I²C-BUS

ıe I²C-bus is for bidirectional, two-line communication between different ICs or modules. The two lines are a serial data ıe (SDA) and a serial clock line (SCL). Both lines must be connected to a positive supply via a pull-up resistor. Data ınsfer may be initiated only when the bus is not busy.

1 Bit transfer

ıe data bit is transferred during each clock pulse. The data on the SDA line must remain stable during the HIGH period the clock pulse as changes in the data line at this time will be interpreted as a control signal.

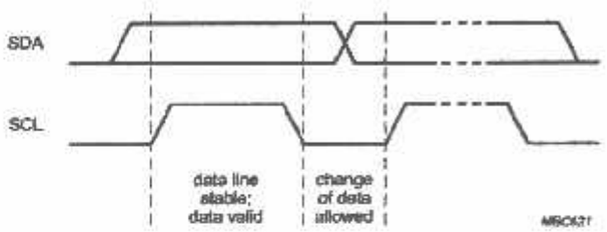


Fig.11 Bit transfer.

Start and stop conditions

h data and clock lines remain HIGH when the bus is not busy. A HIGH-to-LOW transition of the data line, while the :k is HIGH, is defined as the start condition (S). A LOW-to-HIGH transition of the data line while the clock is HIGH, is ned as the stop condition (P).

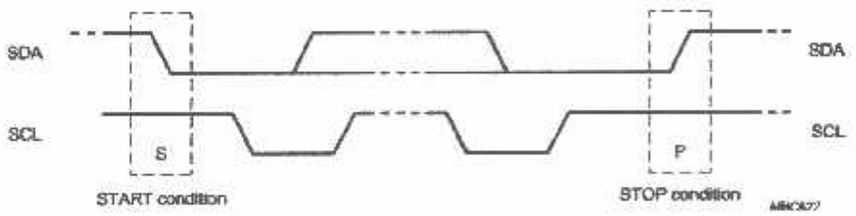


Fig.12 Definition of START and STOP condition.

3 System configuration

device generating a message is a 'transmitter', a device receiving a message is the 'receiver'. The device that controls e message is the 'master' and the devices which are controlled by the master are the 'slaves'.

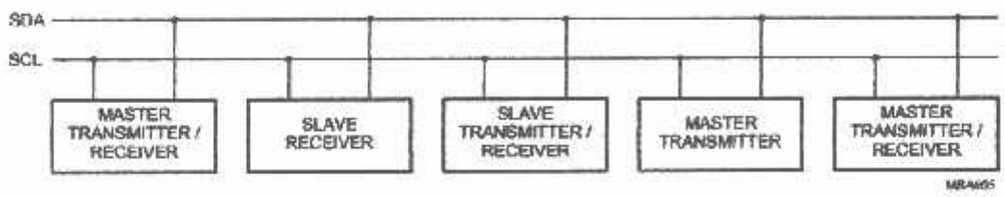


Fig.13 System configuration.

Acknowledge

number of data bytes transferred between the start and stop conditions from transmitter to receiver is not limited. ch data byte of eight bits is followed by one acknowledge bit. The acknowledge bit is a HIGH level put on the bus by transmitter whereas the master also generates an extra acknowledge related clock pulse. A slave receiver which is lressed must generate an acknowledge after the reception of each byte. Also a master must generate an nowledge after the reception of each byte that has been clocked out of the slave transmitter. The device that nowledges has to pull down the SDA line during the acknowledge clock pulse, so that the SDA line is stable LOW ng the HIGH period of the acknowledge related clock pulse. A master receiver must signal an end of data to the smitter by **not** generating an acknowledge on the last byte that has been clocked out of the slave. In this event the smitter must leave the data line HIGH to enable the master to generate a stop condition.

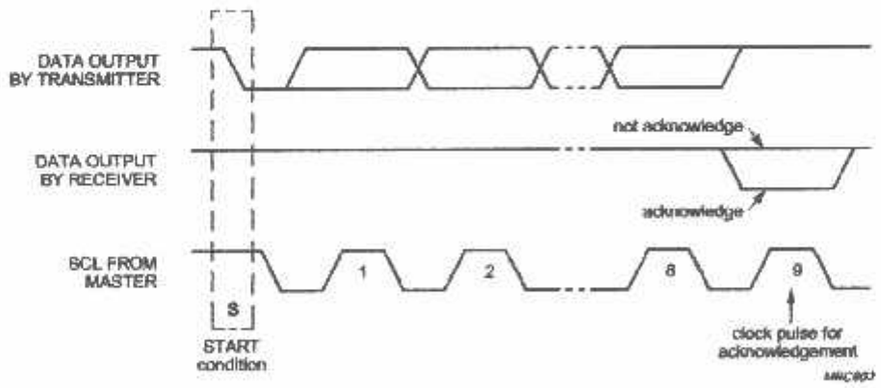


Fig.14 Acknowledgement on the I^2C-bus.

5 I²C-bus protocol

ter a start condition a valid hardware address has to be sent to a PCF8591 device. The read/write bit defines the ection of the following single or multiple byte data transfer. For the format and the timing of the start condition (S), the op condition (P) and the acknowledge bit (A) refer to the I²C-bus characteristics. In the write mode a data transfer is minated by sending either a stop condition or the start condition of the next data transfer.

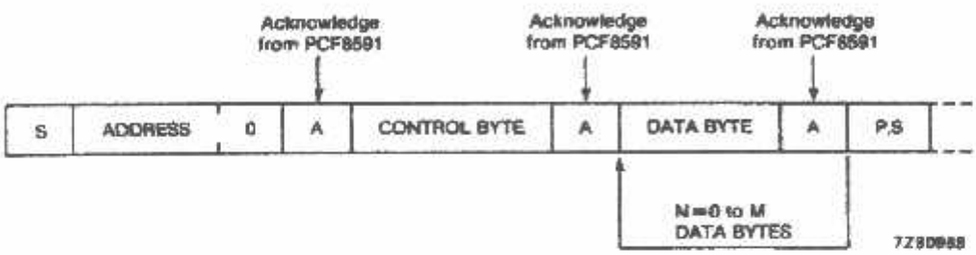


Fig.15 Bus protocol for write mode, D/A conversion.

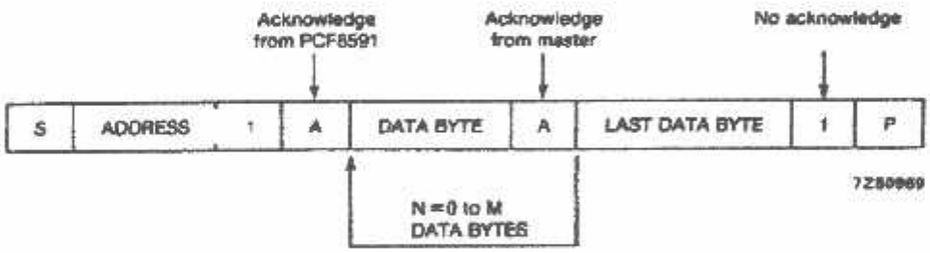


Fig.16 Bus protocol for read mode, A/D conversion.

LIMITING VALUES

accordance with the Absolute Maximum Rating System (IEC 134).

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
DD	supply voltage (pin 16)	−0.5	+8.0	V
I	input voltage (any input)	−0.5	V_{DD} + 0.5	V
	DC input current	–	±10	mA
O	DC output current	–	±20	mA
DD, ISS	V_{DD} or V_{SS} current	–	±50	mA
tot	total power dissipation per package	–	300	mW
O	power dissipation per output	–	100	mW
amb	operating ambient temperature	−40	+85	°C
stg	storage temperature	−65	+150	°C

HANDLING

uts and outputs are protected against electrostatic discharge in normal handling. However, to be totally safe, it is sirable to take precautions appropriate to handling MOS devices. Advice can be found in Data Handbook IC12 under *ndling MOS Devices"*.

DC CHARACTERISTICS

$_{DD}$ = 2.5 V to 6 V; V_{SS} = 0 V; T_{amb} = –40 °C to +85 °C unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
upply						
DD	supply voltage (operating)		2.5	–	6.0	V
D	supply current					
	standby	$V_I = V_{SS}$ or V_{DD}; no load	–	1	15	µA
	operating, AOUT off	f_{SCL} = 100 kHz	–	125	250	µA
	operating, AOUT active	f_{SCL} = 100 kHz	–	0.45	1.0	mA
POR	Power-on reset level	note 1	0.8	–	2.0	V
igital inputs/output: SCL, SDA, A0, A1, A2						
L	LOW level input voltage		0	–	$0.3 \times V_{DD}$	V
H	HIGH level input voltage		$0.7 \times V_{DD}$	–	V_{DD}	V
	leakage current					
	A0, A1, A2	$V_I = V_{SS}$ to V_{DD}	–250	–	+250	nA
	SCL, SDA	$V_I = V_{SS}$ to V_{DD}	–1	–	+1	µA
	input capacitance		–	–	5	pF
	LOW level SDA output current	V_{OL} = 0.4 V	3.0	–	–	mA
ference voltage inputs						
EF	reference voltage	$V_{REF} > V_{AGND}$; note 2	V_{SS} + 1.6	–	V_{DD}	V
GND	analog ground voltage	$V_{REF} > V_{AGND}$; note 2	V_{SS}	–	V_{DD} – 0.8	V
	input leakage current		–250	–	+250	nA
EF	input resistance	pins V_{REF} and AGND	–	100	–	kΩ
cillator: OSC, EXT						
	input leakage current		–	–	250	nA
C	oscillator frequency		0.75	–	1.25	MHz

es

The power on reset circuit resets the I²C-bus logic when V_{DD} is less than V_{POR}.

A further extension of the range is possible, if the following conditions are fulfilled:

$$\frac{V_{REF} + V_{AGND}}{2} \geq 0.8V, V_{DD} - \frac{V_{REF} + V_{AGND}}{2} \geq 0.4V$$

: D/A CHARACTERISTICS

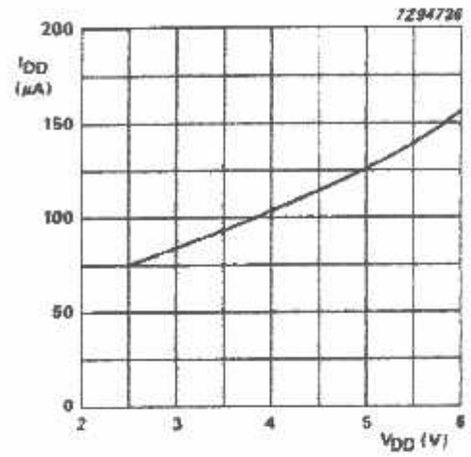
)D = 5.0 V; V_{SS} = 0 V; V_{REF} = 5.0 V; V_{AGND} = 0 V; R_L = 10 kΩ; C_L = 100 pF; T_{amb} = –40 °C to +85 °C unless otherwise ecified.

YMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
nalog output						
OA	output voltage	no resistive load	V_{SS}	–	V_{DD}	V
		R_L = 10 kΩ	V_{SS}	–	0.9 × V_{DD}	V
O	output leakage current	AOUT disabled	–	–	250	nA
ccuracy						
S_e	offset error	T_{amb} = 25 °C	–	–	50	mV
	linearity error		–	–	±1.5	LSB
	gain error	no resistive load	–	–	1	%
AC	settling time	to ½ LSB full scale step	–	–	90	µs
AC	conversion rate		–	–	11.1	kHz
NRR	supply noise rejection ratio	f = 100 Hz; V_{DDN} = 0.1 × V_{PP}	–	40	–	dB

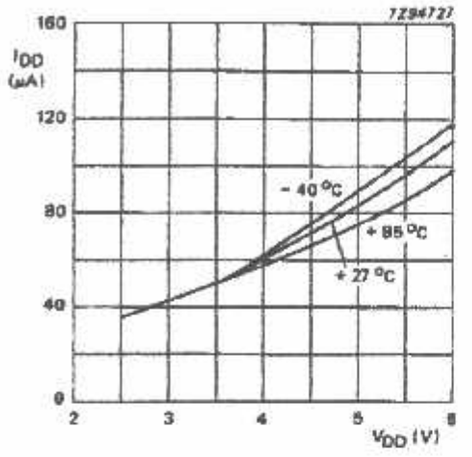
A/D CHARACTERISTICS

) = 5.0 V; V_{SS} = 0 V; V_{REF} = 5.0 V; V_{AGND} = 0 V; R_S = 10 kΩ; T_{amb} = –40 °C to +85 °C unless otherwise specified.

MBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
alog inputs						
	analog input voltage		V_{SS}	–	V_{DD}	V
	analog input leakage current		–	–	100	nA
	analog input capacitance		–	10	–	pF
	differential input capacitance		–	10	–	pF
	single-ended voltage	measuring range	V_{AGND}	–	V_{REF}	V
	differential voltage	measuring range; $V_{FS} = V_{REF} - V_{AGND}$	$\frac{-V_{FS}}{2}$	–	$\frac{+V_{FS}}{2}$	V
curacy						
	offset error	T_{amb} = 25 °C	–	–	20	mV
	linearity error		–	–	±1.5	LSB
	gain error		–	–	1	%
	small-signal gain error	ΔV_i = 16 LSB	–	–	5	%
RR	common-mode rejection ratio		–	60	–	dB
RR	supply noise rejection ratio	f = 100 Hz; V_{DDN} = 0.1 × V_{PP}	–	40	–	dB
	conversion time		–	–	90	µs
	sampling/conversion rate		–	–	11.1	kHz

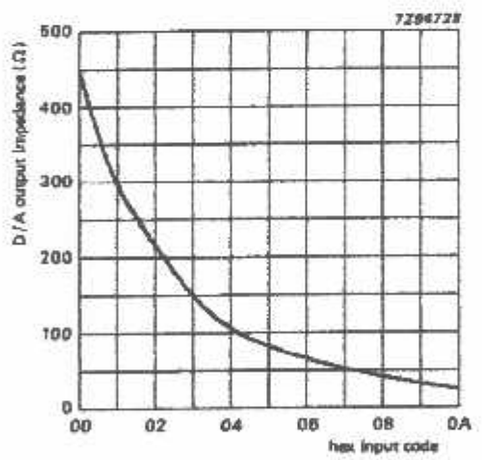


(a) Internal oscillator; T_{amb} = +27 °C.

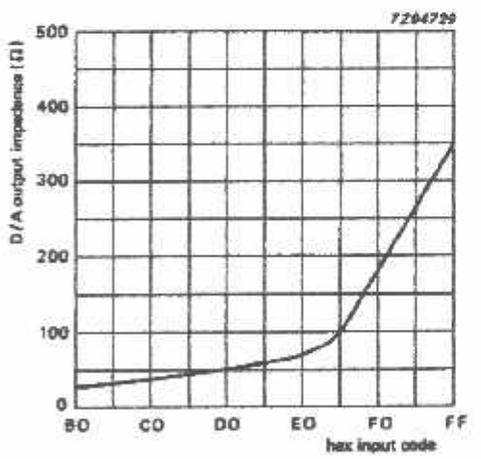


(b) External oscillator.

Fig.17 Operating supply current as a function of supply voltage (analog output disabled).



) Output impedance near negative power rail; T_{amb} = +27 °C.



(b) Output impedance near positive power rail; T_{amb} = +27 °C.

ie x-axis represents the hex input-code equivalent of the output voltage.

Fig.18 Output impedance of analog output buffer (near power rails).

AC CHARACTERISTICS

l timing values are valid within the operating supply voltage and ambient temperature range and reference to V_{IL} and $_H$ with an input voltage swing of V_{SS} to V_{DD}.

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
C-bus timing (see Fig.19; note 1)					
CL	SCL clock frequency	–	–	100	kHz
P	tolerable spike width on bus	–	–	100	ns
UF	bus free time	4.7	–	–	µs
U;STA	START condition set-up time	4.7	–	–	µs
D;STA	START condition hold time	4.0	–	–	µs
OW	SCL LOW time	4.7	–	–	µs
OH	SCL HIGH time	4.0	–	–	µs
	SCL and SDA rise time	–	–	1.0	µs
	SCL and SDA fall time	–	–	0.3	µs
U;DAT	data set-up time	250	–	–	ns
D;DAT	data hold time	0	–	–	ns
D;DAT	SCL LOW-to-data out valid	–	–	3.4	µs
U;STO	STOP condition set-up time	4.0	–	–	µs

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A detailed description of the I²C-bus specification, with applications, is given in brochure *"The I²C-bus and how to use it"*. This brochure may be ordered using the code 9398 393 40011.

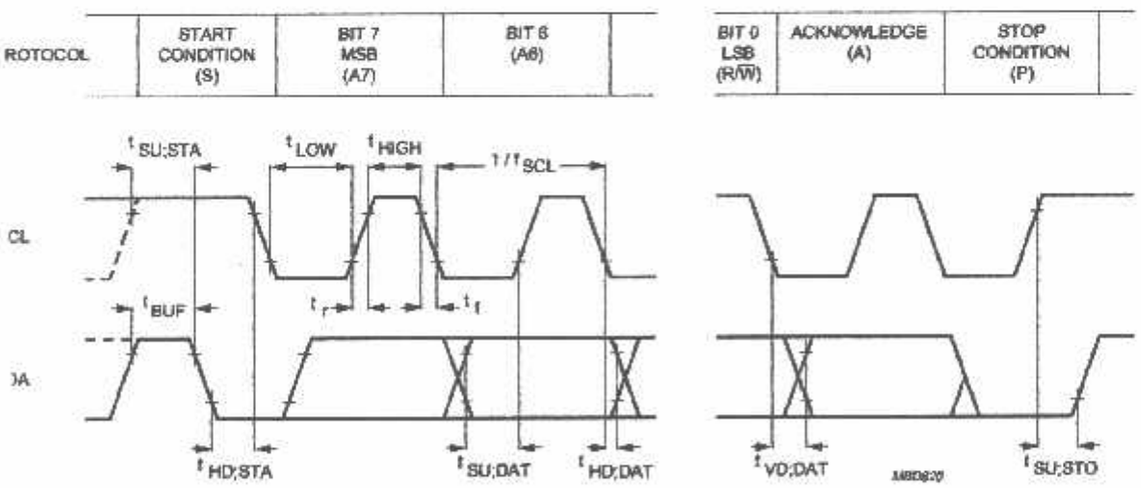


Fig.19 I²C-bus timing diagram; rise and fall times refer to V_{IL} and V_{IH}.

APPLICATION INFORMATION

puts must be connected to V_{SS} or V_{DD} when not in use. Analog inputs may also be connected to AGND or V_{REF}.

order to prevent excessive ground and supply noise and to minimize cross-talk of the digital to analog signal paths the er has to design the printed-circuit board layout very carefully. Supply lines common to a PCF8591 device and noisy gital circuits and ground loops should be avoided. Decoupling capacitors (>10 µF) are recommended for power supply d reference voltage inputs.

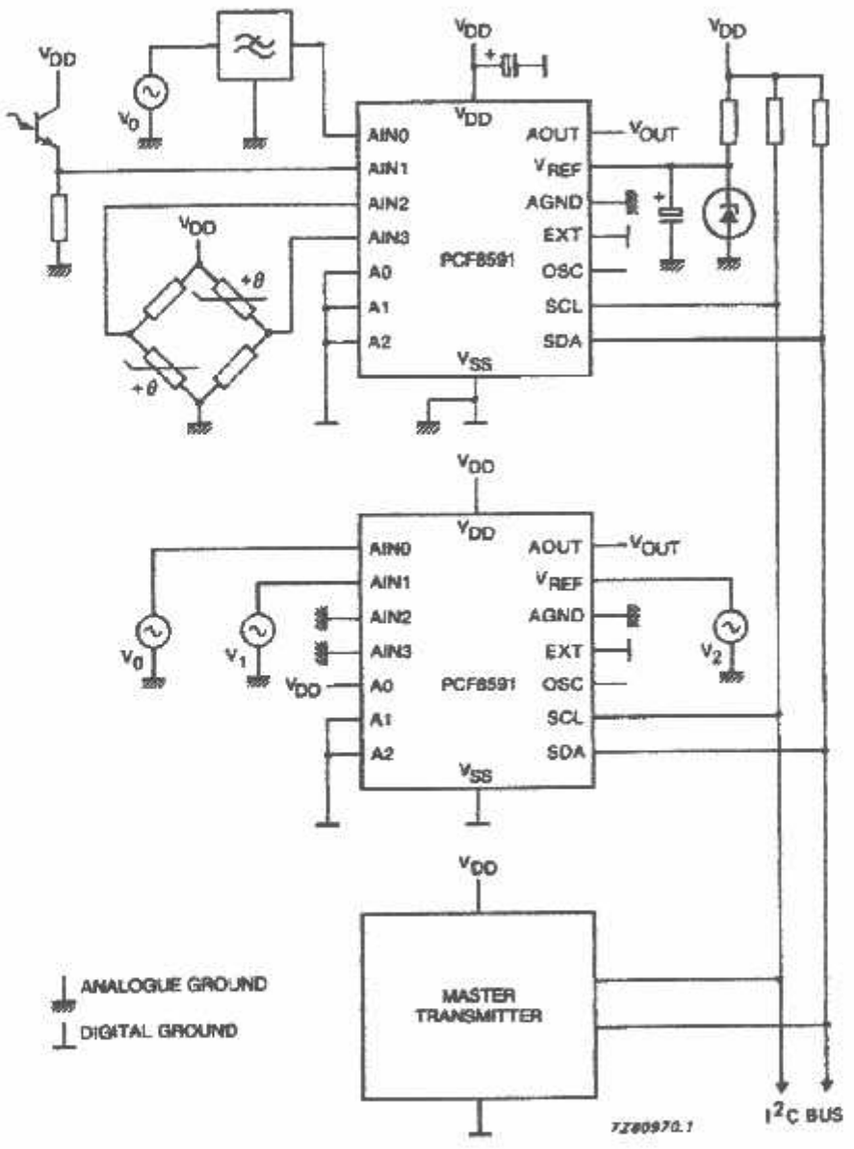
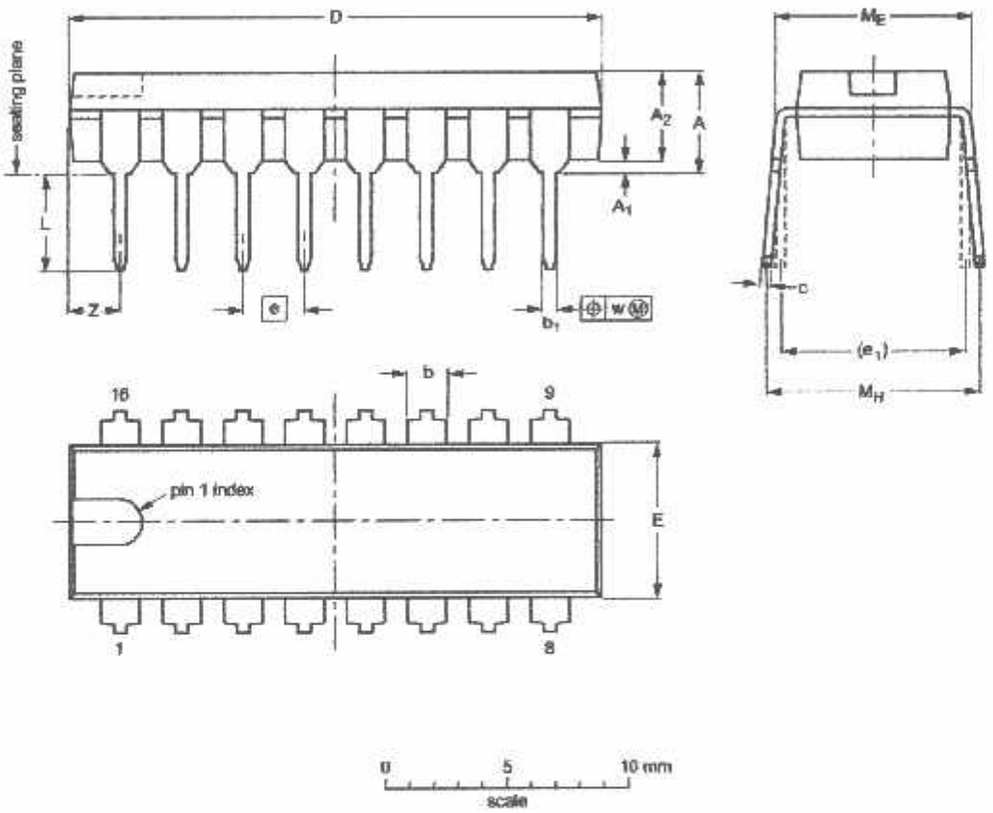


Fig.20 Application diagram.

I PACKAGE OUTLINES

P16: plastic dual in-line package; 16 leads (300 mil); long body **SOT38-1**



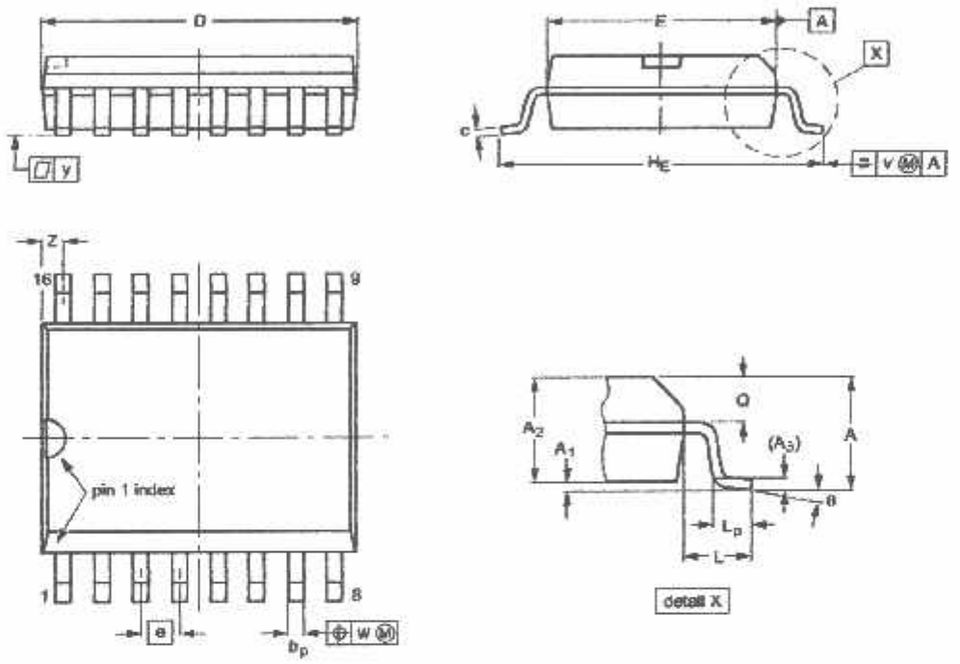
MENSIONS (inch dimensions are derived from the original mm dimensions)

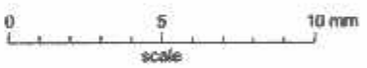
UNIT	A max.	A_1 min.	A_2 max.	b	b_1	c	D (1)	E (1)	e	e_1	L	M_E	M_H	w	Z (1) max.
mm	4.7	0.51	3.7	1.40 1.14	0.53 0.38	0.32 0.23	21.8 21.4	6.48 6.20	2.54	7.62	3.9 3.4	8.25 7.80	9.5 8.3	0.254	2.2
nches	0.19	0.020	0.15	0.055 0.045	0.021 0.015	0.013 0.009	0.86 0.84	0.26 0.24	0.10	0.30	0.15 0.13	0.32 0.31	0.37 0.33	0.01	0.087

te
Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT38-1	050G09	MO-001AE				~~92-10-02~~ 95-01-19

016: plastic small outline package; 16 leads; body width 7.5 mm **SOT162-1**





MENSIONS (Inch dimensions are derived from the original mm dimensions)

JNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(1)}$	e	H_E	L	L_p	Q	v	w	y	$Z^{(1)}$	θ
mm	2.65	0.30 0.10	2.45 2.25	0.25	0.49 0.36	0.32 0.23	10.5 10.1	7.6 7.4	1.27	10.65 10.00	1.4	1.1 0.4	1.1 1.0	0.25	0.25	0.1	0.9 0.4	8° 0°
ches	0.10	0.012 0.004	0.096 0.089	0.01	0.019 0.014	0.013 0.009	0.41 0.40	0.30 0.29	0.050	0.419 0.394	0.055	0.043 0.016	0.043 0.039	0.01	0.01	0.004	0.035 0.016	

te

Plastic or metal protrusions of 0.15 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT162-1	075E03	MS-013AA				~~95-01-24~~ 97-05-22

' SOLDERING

'.1 Introduction

ıere is no soldering method that is ideal for all IC ıckages. Wave soldering is often preferred when ough-hole and surface mounted components are mixed one printed-circuit board. However, wave soldering is t always suitable for surface mounted ICs, or for nted-circuits with high population densities. In these ıations reflow soldering is often used.

is text gives a very brief insight to a complex technology. nore in-depth account of soldering ICs can be found in *"Data Handbook IC26; Integrated Circuit Packages"* der code 9398 652 90011).

2 DIP

2.1 Soldering by dipping or by wave

maximum permissible temperature of the solder is °C; solder at this temperature must not be in contact the joint for more than 5 seconds. The total contact e of successive solder waves must not exceed conds.

device may be mounted up to the seating plane, but temperature of the plastic body must not exceed the cified maximum storage temperature ($T_{stg\ max}$). If the ted-circuit board has been pre-heated, forced cooling be necessary immediately after soldering to keep the perature within the permissible limit.

'.2 Repairing soldered joints

ly a low voltage soldering iron (less than 24 V) to the (s) of the package, below the seating plane or not than 2 mm above it. If the temperature of the ering iron bit is less than 300 °C it may remain in act for up to 10 seconds. If the bit temperature is een 300 and 400 °C, contact may be up to 5 seconds.

SO

.1 Reflow soldering

w soldering techniques are suitable for all SO ages.

w soldering requires solder paste (a suspension of older particles, flux and binding agent) to be applied printed-circuit board by screen printing, stencilling or ure-syringe dispensing before package placement.

Several techniques exist for reflowing; for example, thermal conduction by heated belt. Dwell times vary between 50 and 300 seconds depending on heating method. Typical reflow temperatures range from 215 to 250 °C.

Preheating is necessary to dry the paste and evaporate the binding agent. Preheating duration: 45 minutes at 45 °C.

17.3.2 Wave soldering

Wave soldering techniques can be used for all SO packages if the following conditions are observed:

- A double-wave (a turbulent wave with high upward pressure followed by a smooth laminar wave) soldering technique should be used.
- The longitudinal axis of the package footprint must be parallel to the solder flow.
- The package footprint must incorporate solder thieves at the downstream end.

During placement and before soldering, the package must be fixed with a droplet of adhesive. The adhesive can be applied by screen printing, pin transfer or syringe dispensing. The package can be soldered after the adhesive is cured.

Maximum permissible solder temperature is 260 °C, and maximum duration of package immersion in solder is 10 seconds, if cooled to less than 150 °C within 6 seconds. Typical dwell time is 4 seconds at 250 °C.

A mildly-activated flux will eliminate the need for removal of corrosive residues in most applications.

17.3.3 Repairing soldered joints

Fix the component by first soldering two diagonally-opposite end leads. Use only a low voltage soldering iron (less than 24 V) applied to the flat part of the lead. Contact time must be limited to 10 seconds at up to 300 °C. When using a dedicated tool, all other leads can be soldered in one operation within 2 to 5 seconds between 270 and 320 °C.

DEFINITIONS

ata sheet status	
bjective specification	This data sheet contains target or goal specifications for product development.
reliminary specification	This data sheet contains preliminary data; supplementary data may be published later.
roduct specification	This data sheet contains final product specifications.

imiting values

miting values given are in accordance with the Absolute Maximum Rating System (IEC 134). Stress above one or ore of the limiting values may cause permanent damage to the device. These are stress ratings only and operation the device at these or at any other conditions above those given in the Characteristics sections of the specification not implied. Exposure to limiting values for extended periods may affect device reliability.

pplication information

here application information is given, it is advisory and does not form part of the specification.

LIFE SUPPORT APPLICATIONS

ese products are not designed for use in life support appliances, devices, or systems where malfunction of these ducts can reasonably be expected to result in personal injury. Philips customers using or selling these products for in such applications do so at their own risk and agree to fully indemnify Philips for any damages resulting from such roper use or sale.

PURCHASE OF PHILIPS I²C COMPONENTS

Purchase of Philips I²C components conveys a license under the Philips' I²C patent to use the components in the I²C system provided the system conforms to the I²C specification defined by Philips. This specification can be ordered using the code 9398 393 40011.

DATA SHEET

For a complete data sheet, please also download:

- The IC06 74HC/HCT/HCU/HCMOS Logic Family Specifications
- The IC06 74HC/HCT/HCU/HCMOS Logic Package Information
- The IC06 74HC/HCT/HCU/HCMOS Logic Package Outlines

74HC/HCT132
Quad 2-input NAND Schmitt trigger

Product specification
File under Integrated Circuits, IC06

September 1993

Philips Semiconductors

PHILIPS

Quad 2-input NAND Schmitt trigger | 74HC/HCT132

FEATURES

- Output capability: standard
- I_{CC} category: SSI

GENERAL DESCRIPTION

The 74HC/HCT132 are high-speed Si-gate CMOS devices and are pin compatible with low power Schottky TTL (LSTTL). They are specified in compliance with JEDEC standard no. 7A.

The 74HC/HCT132 contain four 2-input NAND gates which accept standard input signals. They are capable of transforming slowly changing input signals into sharply defined, jitter-free output signals.

The gate switches at different points for positive and negative-going signals. The difference between the positive voltage V_{T+} and the negative voltage V_{T-} is defined as the hysteresis voltage V_H.

QUICK REFERENCE DATA

GND = 0 V; T_{amb} = 25 °C; $t_r = t_f$ = 6 ns

SYMBOL	PARAMETER	CONDITIONS	TYPICAL		UNIT
			HC	HCT	
t_{PHL}/t_{PLH}	propagation delay nA, nB to nY	C_L = 15 pF; V_{CC} = 5 V	11	17	ns
C_I	input capacitance		3.5	3.5	pF
C_{PD}	power dissipation capacitance per gate	notes 1 and 2	24	20	pF

Notes

1. C_{PD} is used to determine the dynamic power dissipation (P_D in µW):

   $P_D = C_{PD} \times V_{CC}^2 \times f_i + \sum (C_L \times V_{CC}^2 \times f_o)$ where:

   f_i = input frequency in MHz

   f_o = output frequency in MHz

   $\sum (C_L \times V_{CC}^2 \times f_o)$ = sum of outputs

   C_L = output load capacitance in pF

   V_{CC} = supply voltage in V

   For HC the condition is V_I = GND to V_{CC}

   For HCT the condition is V_I = GND to V_{CC} – 1.5 V

ORDERING INFORMATION

See *"74HC/HCT/HCU/HCMOS Logic Package Information"*.

PIN DESCRIPTION

PIN NO.	SYMBOL	NAME AND FUNCTION
1, 4, 9, 12	1A to 4A	data inputs
2, 5, 10, 13	1B to 4B	data inputs
3, 6, 8, 11	1Y to 4Y	data outputs
7	GND	ground (0 V)
14	V_{CC}	positive supply voltage

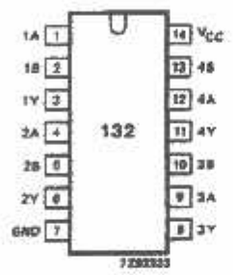


Fig.1 Pin configuration.

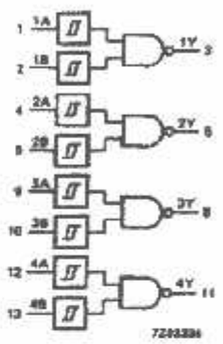


Fig.2 Logic symbol.

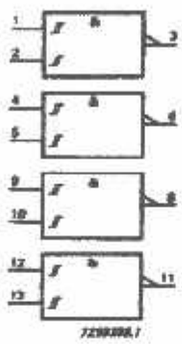


Fig.3 IEC logic symbol.

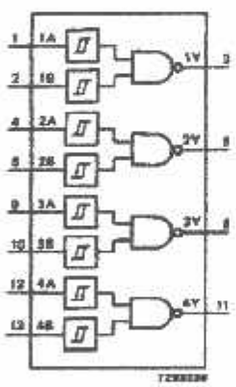


Fig.4 Functional diagram.

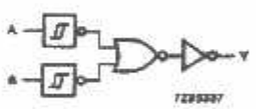


Fig.5 Logic diagram (one Schmitt trigger).

FUNCTION TABLE

INPUTS		OUTPUT
nA	nB	nY
L	L	H
L	H	H
H	L	H
H	H	L

Notes

1. H = HIGH voltage level
   L = LOW voltage level

APPLICATIONS

- **Wave and pulse shapers**
- **Astable multivibrators**
- **Monostable multivibrators**

DC CHARACTERISTICS FOR 74HC

For the DC characteristics see *"74HC/HCT/HCU/HCMOS Logic Family Specifications"*. Transfer characteristics are given below.

Output capability: standard
I_{CC} category: SSI

Transfer characteristics for 74HC

Voltages are referenced to GND (ground = 0 V)

SYMBOL	PARAMETER	T_{amb} (°C)							UNIT	TEST CONDITIONS	
		74HC								V_{CC} (V)	WAVEFORMS
		+25			−40 to +85		−40 to +125				
		min.	typ.	max.	min.	max.	min.	max.			
V_{T+}	positive-going threshold	0.7	1.18	1.5	0.7	1.5	0.7	1.5	V	2.0	Figs 6 and 7
		1.7	2.38	3.15	1.7	3.15	1.7	3.15		4.5	
		2.1	3.14	4.2	2.1	4.2	2.1	4.2		6.0	
V_{T-}	negative-going threshold	0.3	0.63	1.0	0.3	1.0	0.3	1.0	V	2.0	Figs 6 and 7
		0.9	1.67	2.2	0.9	2.2	0.9	2.2		4.5	
		1.2	2.26	3.0	1.2	3.0	1.2	3.0		6.0	
V_H	hysteresis ($V_{T+} - V_{T-}$)	0.2	0.55	1.0	0.2	1.0	0.2	1.0	V	2.0	Figs 6 and 7
		0.4	0.71	1.4	0.4	1.4	0.4	1.4		4.5	
		0.6	0.88	1.6	0.6	1.6	0.6	1.6		6.0	

C CHARACTERISTICS FOR 74HC

ND = 0 V; $t_r = t_f$ = 6 ns; C_L = 50 pF

SYMBOL	PARAMETER	T_{amb} (°C)							UNIT	TEST CONDITIONS	
		74HC								V_{CC} (V)	WAVEFORMS
		+25			−40 TO +85		−40 TO +125				
		min.	typ.	max.	min.	max.	min.	max.			
$_{PHL}$/ t_{PLH}	propagation delay nA, nB to nY		36	125		155		190	ns	2.0	Fig.13
			13	25		31		38		4.5	
			10	21		26		32		6.0	
$_{THL}$/ t_{TLH}	output transition time		19	75		95		110	ns	2.0	Fig.13
			7	15		19		22		4.5	
			6	13		16		19		6.0	

DC CHARACTERISTICS FOR 74HCT

For the DC characteristics see *"74HC/HCT/HCU/HCMOS Logic Family Specifications"*. Transfer characteristics are given below.

Output capability: standard
I_{CC} category: SSI

Notes to HCT types

The value of additional quiescent supply current (ΔI_{CC}) for a unit load of 1 is given in the family specifications. To determine ΔI_{CC} per input, multiply this value by the unit load coefficient shown in the table below.

INPUT	UNIT LOAD COEFFICIENT
nA, nB	0.3

Transfer characteristics for 74HCT

Voltages are referenced to GND (ground = 0 V)

SYMBOL	PARAMETER	T_{amb} (°C)							UNIT	TEST CONDITIONS	
		74HCT								V_{CC} (V)	WAVEFORMS
		+25			−40 to +85		−40 to +125				
		min.	typ.	max.	min.	max.	min.	max.			
V_{T+}	positive-going threshold	1.2	1.41	1.9	1.2	1.9	1.2	1.9	V	4.5	Figs 6 and 7
		1.4	1.59	2.1	1.4	2.1	1.4	2.1		5.5	
V_{T-}	negative-going threshold	0.5	0.85	1.2	0.5	1.2	0.5	1.2	V	4.5	Figs 6 and 7
		0.6	0.99	1.4	0.6	1.4	0.6	1.4		5.5	
V_H	hysteresis ($V_{T+} - V_{T-}$)	0.4	0.56	–	0.4	–	0.4	–	V	4.5	Figs 6 and 7
		0.4	0.60	–	0.4	–	0.4	–		5.5	

C CHARACTERISTICS FOR 74HCT

ND = 0 V; $t_r = t_f$ = 6 ns; C_L = 50 pF

YMBOL	PARAMETER	T_{amb} (°C)							UNIT	TEST CONDITIONS	
		74HCT								V_{CC} (V)	WAVEFORMS
		+25			−40 to +85		−40 to +125				
		min.	typ.	max.	min.	max.	min.	max.			
$_{HL}$/ t_{PLH}	propagation delay nA, nB to nY		20	33		41		50	ns	4.5	Fig.13
$_{HL}$/ t_{TLH}	output transition time		7	15		19		22	ns	4.5	Fig.13

TRANSFER CHARACTERISTIC WAVEFORMS

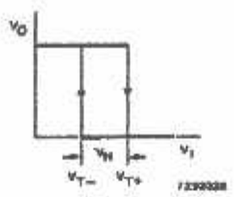


Fig.6 Transfer characteristic.

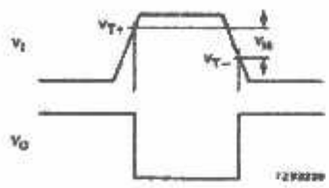


Fig.7 Waveforms showing the definition of V_{T+}, V_{T-} and V_H; where V_{T+} and V_{T-} are between limits of 20% and 70%.

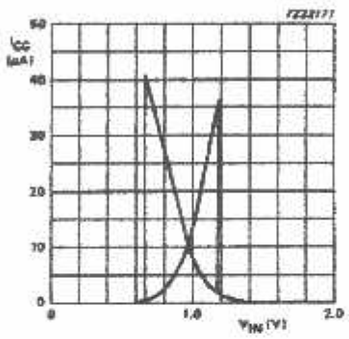


Fig.8 Typical HC transfer characteristics; V_{CC} = 2 V.

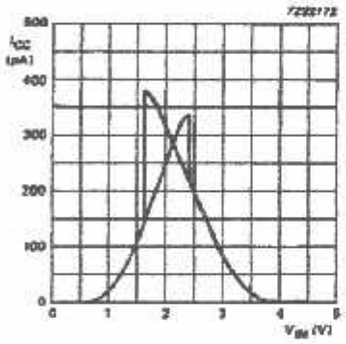


Fig.9 Typical HC transfer characteristics; V_{CC} = 4.5 V.

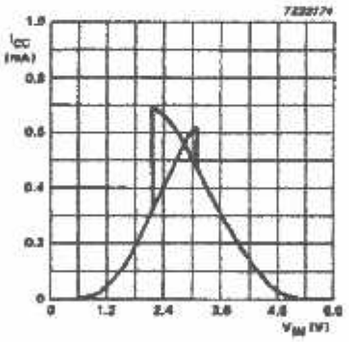


Fig.10 Typical HC transfer characteristics; V_{CC} = 6 V.

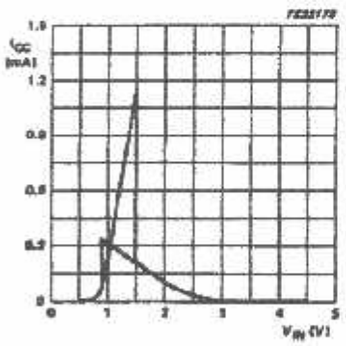


Fig.11 Typical HCT transfer characteristics; V_{CC} = 4.5 V.

Application information

The slow input rise and fall times cause additional power dissipation, this can be calculated using the following formula:

$P_{ad} = f_i \times (t_r \times I_{CCa} + t_f \times I_{CCa}) \times V_{CC}$,

Where:

P_{ad} = additional power dissipation (μW)
f_i = input frequency (MHz)
t_r = input rise time (ns); 10% – 90%
t_f = input fall time (ns); 10% – 90%
I_{CCa} = average additional supply current (μA)

Average I_{CCa} differs with positive or negative input transitions, as shown in Figs 14 and 15.

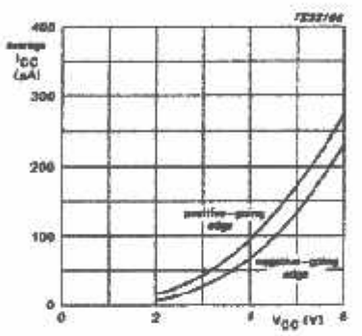


Fig.14 Average I_{CC} for HC Schmitt trigger devices; linear change of V_I between 0.1 V_{CC} to 0.9 V_{CC}.

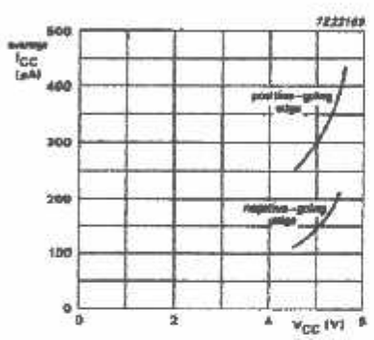


Fig.15 Average I_{CC} for HCT Schmitt trigger devices; linear change of V_I between 0.1 V_{CC} to 0.9 V_{CC}.

C/HCT132 used in a relaxation oscillator circuit, see Fig.16.

HC: $f = \frac{1}{T} \approx \frac{1}{0.8RC}$

HCT: $f = \frac{1}{T} \approx \frac{1}{0.67\ RC}$

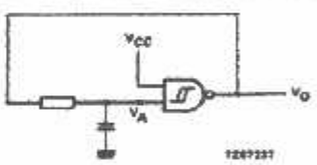


Fig.16 Relaxation oscillator using HC/HCT132.

ote to Application information

values given are typical unless otherwise specified.

CKAGE OUTLINES

e *"74HC/HCT/HCU/HCMOS Logic Package Outlines"*.

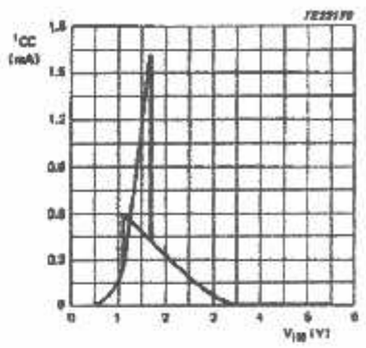
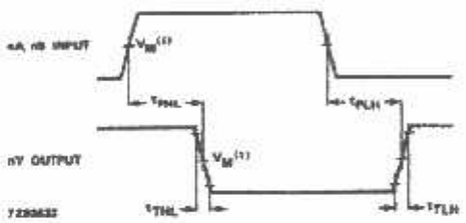


Fig.12 Typical HCT transfer characteristics; V_{CC} = 5.5 V.

AC WAVEFORMS



(1) HC : V_M = 50%; V_I = GND to V_{CC}.
HCT: V_M = 1.3 V; V_I = GND to 3 V.

Fig.13 Waveforms showing the input (nA, nB) to output (nY) propagation delays and the output transition times.