PERENCANAAN DAN PEMBUATAN ALAT TELEMETRI SUHU DENGAN FASILITAS PENCATATAN PADA KOMPUTER

TUGAS AKHIR

Disusun Oleh :

NAMA : YAN BENYAMIN
NIM : 03.57.022

KONSENTRASI TEKNIK ELEKTRONIKA
JURUSAN TEKNIK ELEKTRO DIPLOMA III
FAKULTAS TEKNOLOGI INDUSTRI
INSTITUT TEKNOLOGI NASIONAL MALANG

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LEMBAR PENGESAHAN

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PADA KOMPUTER

TUGAS AKHIR

Disusun dan diajukan sebagai salah satu syarat untuk memperoleh gelar
Ahli Madya Teknik Elektronika (D-III)

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2007

ABSTRAKSI

Perencanaan dan Pembuatan Alat Telemetri Suhu Dengan Fasilitas Pencatatan pada Komputer, Yan Benyamin, 0357022, Konsentrasi Teknik Elektronika, Jurusan Teknik Elektro D-III, Institut Teknologi Nasional Malang, Dosen Pembimbing: Joseph Dedy Irawan, ST. MT.

Kata kunci: Sensor Suhu LM35, LM358, AT89S51, Atmega16,

Ilmu pengetahuan dan teknologi ditujukan agar manusia meningkatkan kualitas hidupnya. Beberapa tugas manusia dilakukan secara rutin, sehingga mengurangi efisiensi waktu. Selain itu, tugas-tugas tersebut juga terkadang membahayakan keselamatan manusia. Salah satunya adalah pengukuran suhu di tempat-tempat yang berbahaya. Bagaimana agar efisiensi waktu dan keselamatan manusia tetap terjamin? Bagaimana cara untuk mengukur kondisi temperatur di tempat yang jauh, untuk kemudian dikirimkan ke komputer untuk dicatat? Dalam laporan dibahas cara membuat alat telemetri suhu dengan fasilitas pencatatan pada komputer, dengan tujuan akhir meningkatkan efisiensi waktu dan mempertahankan tingkat keselamatan manusia.

Untuk pembuatan alat ini, dirancang modul-modul yang diperlukan, yaitu modul sensor suhu dan pengkondisi sinyal, konverter analog ke digital, mikrokontroler, modulator dan demodulator FS, serta antarmuka ke komputer. Sensor suhu menggunakan IC LM35, pengkondisi sinyal menggunakan *operational amplifier* LM358, digunakan dua jenis mikrokontroler yaitu Atmega16 karena memiliki ADC internal, dan AT89S51 yang dihubungkan dengan IC MAX233 untuk antarmuka ke komputer. Modul-modul tersebut dirancang, dibuat, dan diuji per modul dan sebagai suatu keseluruhan sistem.

Penggunaan IC LM35 menunjukkan tingkat *error* rata-rata sebesar 5,19%. Pengkondisi sinyal dengan IC LM358 menunjukkan tingkat *error* rata-rata pada gain sebesar 4,475%. ADC internal Atmega16 menunjukkan tingkat sensitifitas yang tinggi dengan hasil yang akurat. Untuk pengembangan selanjutnya, disarankan agar membuat modul-modul yang lebih hemat daya agar mengurangi kebutuhan pemeliharaan, dan penggunaan teknik-teknik pengurangan *noise* agar data yang dikirim lebih baik.

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Puji syukur penulis persembahkan hanya pada Yesus Kristus, sebab hanya karena Dia-lah, Sang Causa Prima, maka semua ini bisa terjadi. Atas bimbingan dan berkat-Nya, penulis dapat menyelesaikan laporan pembuatan Tugas Akhir dengan judul "Perencanaan dan Pembuatan Alat Telemetri Suhu Dengan Fasilitas Pencatatan Pada Komputer" ini, di mana laporan ini merupakan salah satu syarat kelulusan pada Jurusan Teknik Elektro D-III Institut Teknologi Nasional Malang.

Terima kasih sebesar-besarnya penulis haturkan atas bimbingan, petunjuk, dan bantuan barik moral maupun material, kepada:

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5. Instruktur Laboratorium Perancangan Elektronika ITN Malang.
6. Teman-teman Elka D-III angkatan 2003.
7. Teman-teman, dan pihak-pihak lainnya yang tidak dapat disebutkan satu per satu.

Penulis mengakui bahwa masih banyak kekurangan dalam penyusunan laporan ini. Oleh karena itu kritik dan saran serta masukan-masukan lainnya yang bertujuan membangun akan diterima demi penyempurnaan karya penulis lainnya. Semoga laporan ini menjadi bermanfaat bagi kita semua.

September 2007

Penulis

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BAB I
PENDAHULUAN

1.1. Latar Belakang

Ilmu pengetahuan dan teknologi ditujukan agar manusia dapat meningkatkan kualitas hidupnya. Salah satu yang ingin dicapai adalah agar manusia dapat menggunakan waktunya seefektif dan seefisien mungkin. Untuk hal-hal yang rutin, misalnya, diharapkan agar pekerjaan-pekerjaan rutin dapat dilakukan oleh suatu alat yang otomatis sehingga manusia dapat menggunakan waktunya untuk melakukan hal-hal yang lain. Hal lain lagi adalah keselamatan manusia tetap terjaga. Untuk hal ini, kegiatan-kegiatan yang dapat membahayakan fisik manusia diharapkan dapat digantikan oleh suatu alat yang lain, yang bisa dipantau atau dikendalikan oleh manusia. Perkembangan teknologi sudah sampai pada tahap ini. Penggunaan komputer atau mikrokontroler sudah dapat melakukan kedua hal di atas, melakukan tugas-tugas rutin dan memungkinkan manusia menempatkan suatu alat lain untuk menghindari ancaman bahaya fisik manusia.

Terinspirasi dari beberapa tayangan iptek di televisi, penulis memiliki ide untuk membuat suatu alat yang berguna untuk mendapatkan data temperatur dari suatu tempat untuk dilihat dan dipantau dari komputer di tempat yang nyaman. Sistem ini nantinya akan mengambil data yang diinginkan, kemudian dipancarkan ke komputer agar dapat dipantau dan dicatat tanpa harus mendatangi lokasi secara langsung.

Harapan penulis adalah agar sistem yang digunakan dalam Tugas Akhir penulis ini dapat menjadi suatu hal yang berguna bagi kita di bidang pendidikan maupun di bidang-bidang lainnya.

1.2. Rumusan Masalah

Berdasarkan uraian yang dikemukakan di atas, maka permasalahan dirumuskan sebagai berikut:

1. Bagaimana cara untuk mengukur kondisi temperatur di tempat yang jauh, untuk kemudian dikirimkan ke komputer.
2. Bagaimana mengirimkan data suhu dari sensor suhu ke komputer. Tujuan

Tujuan dari pembuatan alat ini adalah untuk merancang dan membuat suatu alat berbasis mikrokontroler untuk mengukur temperatur di suatu tempat, yang kemudian dikirimkan ke komputer untuk dicatat.

1.3. Batasan Masalah

Mengingat banyaknya hal yang dapat dibahas dalam pembuatan Tugas Akhir ini, membahas keseluruhan secara mendetil menjadi tidak mungkin. Oleh karena itu, masalah yang akan dibahas penulis batasi sebagai berikut:

- Membahas teknik pengambilan data temperatur.
- Membahas cara pengiriman data dari satu tempat ke tempat lainnya.
- Tidak membahas detil teknik pemancar dan penerima FM.
- Memfokuskan pada penggunaan modulasi FSK dalam pengiriman data.
- Tidak membahas catu daya alat.

1.4. Metodologi Penelitian

Metode yang digunakan dalam pembuatan alat ini adalah metode praktis, yaitu pembuatan alat secara nyata berdasarkan teori-teori yang telah diperoleh selama perkuliahan. Tahap-tahap penelitian adalah sebagai berikut:

- Studi Pustaka : Mempelajari cara kerja pendeteksian suhu dengan sensor suhu, memperlajari dasar komuniasi serial, mempelajari teknik-teknik modulasi untuk sinyal digital.
- Perencanaan alat : merancang rangkaian sensor suhu serta pengkondisian sinyal, rangkaian modulator dan demodulator data, serta antarmuka mikrokontroler ke komputer.
- Pembuatan alat, baik *hardware* maupun *software.*
- Pengujian alat
- Kesimpulan

1.5. Sistematika Pembahasan

Tulisan dalam Tugas Akhir ini terdiri dari 5 bab yaitu :

BAB I : PENDAHULUAN

Berisi latar belakang masalah, perumusan masalah, tujuan pembahasan, batasan masalah, metodologi penelitian, sistimatika penulisan, dan relevansi dari penulisan tugas akhir ini

BAB II : DASAR TEORI

Membahas tentang teori dasar sensor suhu, mikrokontroler ATmega16, modulasi, modulator dan demodulator, serta *software PC.*

BAB III : PERENCANAAN DAN PEMBUATAN ALAT

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BAB III : PERENCANAAN DAN PEMBUATAN ALAT

Membahas penyusunan dan perhitungan rancangan dan pembuatan alat, baik perangkat keras maupun perangkat lunak.

BAB IV : PENGUJIAN ALAT

Berisi tentang uji coba, cara pengoperasian, spesifikasi, serta hasil kalibrasi dari alat yang telah dibuat.

BAB V : PENUTUP

Merupakan kesimpulan dari pembahasan pada bab-bab sebelumnya dan saran serta kemungkinan pada pengembangan alat tersebut.

BAB II
DASAR TEORI

2.1. Sistem Pengukuran

Hampir dalam setiap aplikasi teknis terdapat kebutuhan untuk mengukur suatu besaran fisik, seperti gaya, tekanan, temperatur, atau aliran. Pengukuran ini menggunakan alat-alat fisik yang disebut sensor dan tranduser, yang memiliki kemampuan untuk mengubah suatu besaran fisik menjadi besaran elektrik yang lebih mudah untuk diolah. Sensor, yaitu tranducer yang digunakan pada bagian input, mengubah besaran fisik (seperti tekanan atau temperatur) menjadi suatu besaran listrik yang biasanya proporsional dengan besaran masukannya. Untuk beberapa hal, pengunaan sensor memerlukan pengaturan tambahan sebelum besaran elektrisnya dapat digunakan. Pengaturan ini diperlukan agar keluaran dari sensor sesuai untuk digunakan dalam tahap selanjutnya. Tahap pengaturan ini disebut sebagai tahap pengkondisi sinyal.

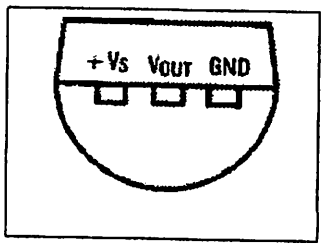
Komputer dan mikrokontroler adalah perangkat yang bekerja secara digital. Oleh karena itu, semua masukan harus dirubah dari bentuk analognya menjadi bentuk digital, melalui proses konversi analog ke digital. Proses ini dilakukan oleh perangkat yang disebut ADC (*Analog to Digital Converter*). Dalam bentuk digital inilah data kemudian diolah (ditransmisikan, dicatat, dll.).

2.1.1. Sensor Suhu LM35

Sensor suhu yang penulis gunakan adalah *IC* LM35 keluaran National Semiconductor. *IC* LM35 disebut sebagai sensor suhu presisi celcius, di mana *IC* ini mengubah besaran suhu menjadi tegangan dengan tingkat akurasi

terkalibrasi seesar 10mV / °C +- 0.2°C. Dengan kata lain, tiap perubahan suhu sebesar 1 °C maka akan terjadi perubahan tegangan keluaran sebesar 10 mV.

Sensor suhu LM35 memiliki konfigurasi pin yang sangat sederhana, dimana hanya terdapat 3 terminal, yaitu untuk catu positif, *ground*, serta keluaran data. Ini menyebabkan sensor ini menjadi sangat mudah untuk digunakan.



Gambar 2.1
Pinout Sensor Suhu LM35
Sumber: Datasheet LM35

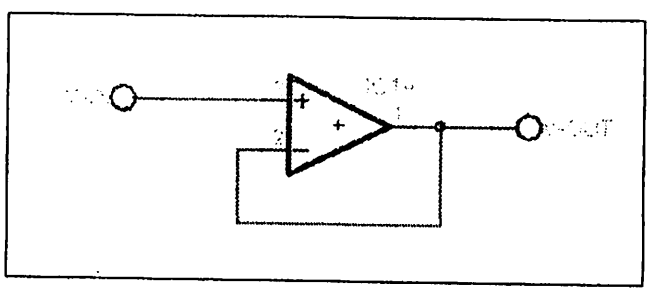
2.2. Pengkondisi Sinyal

Tahap selanjutnya dari sebuah sistem pengukuran adalah sebuah pengkondisi sinyal yang mungkin diperlukan untuk memanipulasi keluaran sensor ke dalam bentuk yang sesuai dengan tujuan yang diinginkan. Seringkali, keluaran dari sensor harus dimasukkan ke dalam sistem komputer digital. Dalam hal ini, sinyal harus dikondisikan agar cocok dengan proses pengambilan data. Dua fungsi yang paling penting dari pengkondisian sinyal adalah penguatan dan *filter*.

Penguat instrumentasi (*instrumentation amplifier, IA*) adalah rangkaian dengan impedansi input yang sangat tinggi, arus bias yang rendah, dan tingkat penguatan yang dapat diatur. Situasi ini terjadi cukup sering, di mana sinyal sebuah tranduser harus dikuatkan terlebih dahulu, sebelum melalui pengkondisian selanjutnya (seperti

filtering). Penguat instrumentasi dijalankan oleh rangkaian *operation amplifier* (*op-amp*).

Op-amp dapat digunakan sebagai penyangga, penguat, pembanding, penjumlah tegangan, penguat differensial, integrator, differensiator, dan lain-lain, namun penggunaan *op-amp* sebagai pengkondisi sinyal biasanya hanya meliputi penyangga, penguat, atau pembanding.



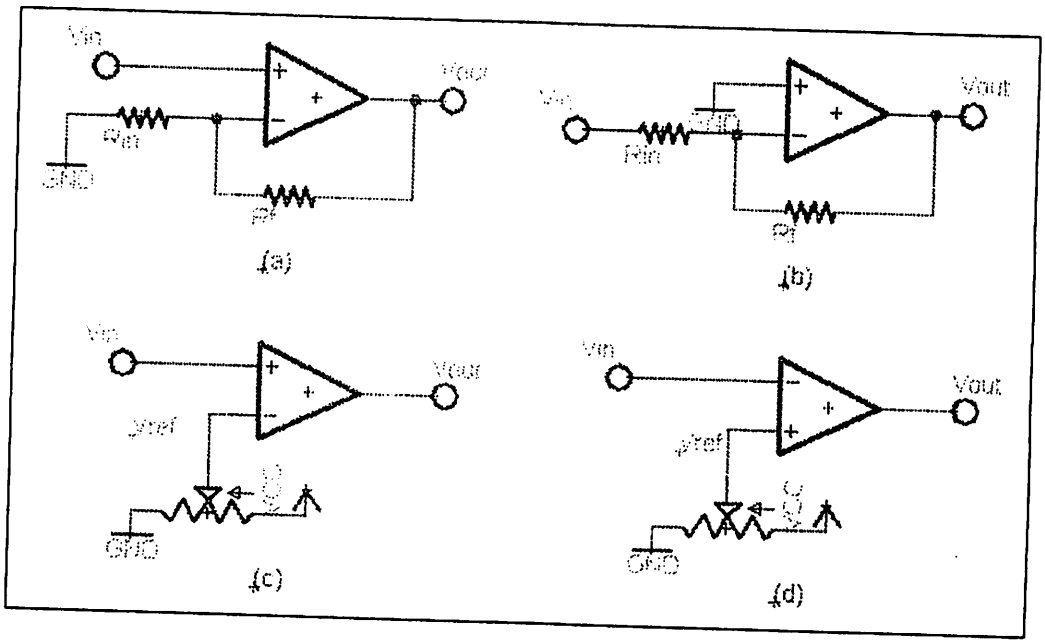
Gambar 2.2
Rangkaian *Op-Amp* Sebagai Penyangga
Sumber: Malvino, Prinsip-Prinsip Elektronika

Penggunaan sebagai buffer adalah dengan menghubungkan rangkaian ke masukan tak membalik, kemudian menghubungkan keluaran ke masukan tak membalik sebagai umpan balik, seperti pada Gambar 2.1. Selanjutnya, Gambar 2.2 menunjukkan rangkaian *op-amp* sebagai: (a) penguat tak membalik, (b) penguat membalik, (c) komparator dengan *set-point* negatif, dan (d) komparator dengan *set-point* positif. Tegangan keluaran masing-masing rangkaian adalah:

- $V_{out} = \left(\frac{R_f}{R_i} + 1\right).V_{in}$
- $V_{out} = \frac{R_f}{R_i}.V_{in}$

- Bila Vin > Vref maka Vout adalah +Vsat, sedangkan bila Vin < Vref maka Vout adalah –Vsat.
- Bila Vin < Vref maka Vout adalah +Vsat, sedangkan bila Vin > Vref maka Vout adalah –Vsat.

+Vsat adalah tegangan catu positif dikurangi tegangan saturasi, -Vsat adalah tegangan catu negatif ditambah tegangan saturasi.



Gambar 2.3
Rangkaian *Op-Amp* Sebagai Penguat dan Pembanding
Sumber: Malvino, Prinsip-Prinsip Elektronika

2.3. Mikrokontroler

Mikrokontroler sering disebut sebagai suatu komputer dalam satu keping. Hal ini disebabkan oleh keringkasan dari mikrokontroler, di mana bagian CPU, memori program, memori data, dan perangkat *I/O* semua sudah terangkum dalam suatu keping *IC*. Beberapa jenis mikrokontroler bahkan telah menambahkan beberapa komponen tambahan seperti ADC, perangkat koneksi serial (UART, I^2C, SPI), RTC, PWM, dan lain-lain. Penggunaannya pun sudah merambah ke berbagai bidang, mulai dari *consumer electronics*, industri, hingga untuk penelitian-penelitian ilmiah.

Terdapat banyak jenis mikrokontroler di pasaran saat ini. Beberapa produsen mikrokontroler yang umum digunakan adalah Atmel, Microchip, Renesas, Fairchild (dari Motorola), dan Dallas-Maxim. Dalam alat ini, penulis menggunakan dua jenis mikrokontroler dari dua keluarga berbeda, yaitu mikrokontroler ATmega16 dari keluarga Atmel AVR dan AT89S51 dari keluarga Intel 8051.

2.3.1. Mikrokontroler ATmega16

ATmega16 adalah mikrokontroler dari keluarga Atmel AVR, yaitu keluarga mikrokontroler dengan arsitektur RISC 8-bit. Keluarga AVR memiliki waktu eksekusi instruksi rata-rata 1 instruksi per siklus *clock*, hingga keluarannya dapat mencapai 1 juta instruksi per MHz. ATmega16 memiliki fitur-fitur sebagai berikut:

- 8K Byte memori program berbentuk *flash memory*.
- 512 Byte memori data berbentuk EEPROM.
- 32 buah jalur I/O independen, tersusun dalam 4 port, masing-masing 8 bit.
- 1K Byte memori SRAM internal.
- Dua buah *timer / counter* 8-bit.
- Empat kanal PWM.
- 8 kanal ADC 10-bit
- Antarmuka serial 2 kabel (I^2C)

- Antarmuka UART
- Antarmuka SPI
- Pembanding analog

ATmega16 beroperasi dengan catu tegangan 4.5 – 5.5 V, 12mA (aktif, 8 MHz , Vcc = 5V), dengan kecepatan maksimum 16 MHz.

2.3.1.1. Konfigurasi Pin Mikrokontroler ATmega16

Gambar II-1 menunjukkan simbol skematik untuk ATmega16 tipe 40-pin *PDIP* pada program Eagle versi 4.16r1. Tipe ini memiliki 40 pin, yang terbagi atas:

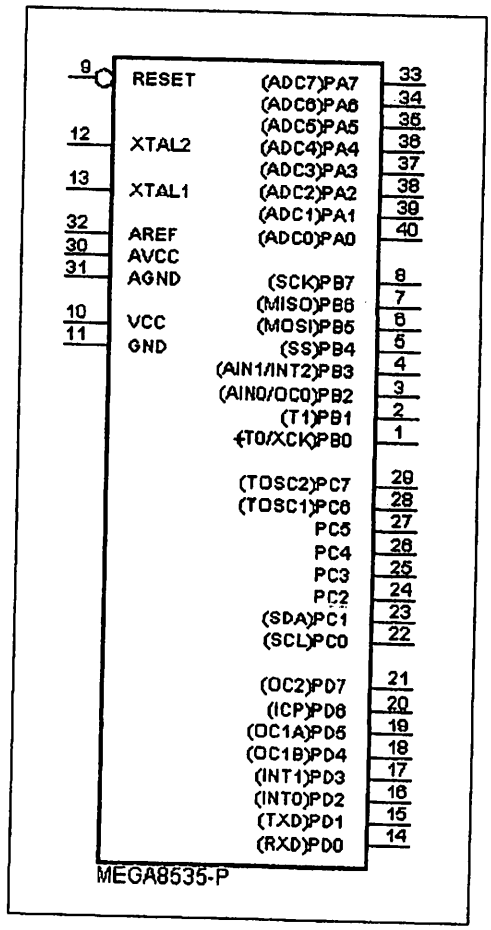
Tabel 2.1
Konfigurasi Pin Mikrokontroler Amega8535 versi PDIP

Nomor Pin	Nama	Fungsi
10	VCC	Catu tegangan digital
11	GND	Ground
40 s.d. 33	PORTA (PORTA0 s.d. PORTA7)	Port A adalah port *input/output* dua arah. Fungsi lain dari Port A adalah sebagai masukan dari ADC (ADC0 s.d. ADC7)
1 s.d. 8	PORTB (PORTB0 s.d. PORTB7)	Port B adalah port *input/output* dua arah. Port B Juga merupakan koneksi untuk beberapa fungsi ATmega16, seperti untuk fasilitas SPI, pembanding analog, dan masukan untuk pencacah.
22 s.d. 29	PORTC (PORTC0 s.d. PORTC7)	Port C adalah port *input/output* dua arah. PORTC0 dan PORTC1 berfungsi sebagai port Serial Clock dan Serial Data apabila menggunakan fungsi I^2C.

14 s.d. 21	PORTD (PORTD0 s.d. PORTD7)	Port D adalah port *input/output* dua arah. Beberapa pin Port D memiliki fungsi-fungsi lain seperti komunikasi UART. masukan *interrupt*.
9	RESET	Masukan Reset. Logika 0 pada pin ini selama dua siklus *clock* akan me-*reset* mikrokontroller ATmega16.
13	XTAL1	Masukan untuk penguat pembalik *oscillator* dan masukan ke rangkaian *clock* internal.
12	XTAL2	Keluaran dari penguat pembalik *oscillator*.
30	AVCC	Catu tegangan analog untuk pemakaian ADC internal.
31	AGND	Ground tegangan analog.
32	AREF	Tegangan referensi untuk ADC internal.

Sumber: Datasheet ATmega16

Fungsi-fungsi lain dari pin-pin mikrokontroller ATmega16 diaktifkan melalui program, dengan memberi konfigurasi tertentu pada *special function register*.



Gambar 2.4
Simbol Skematik ATmega16
Sumber: Program EAGLE 4.16r2

2.3.1.2. Organisasi Memori ATmega16

Bagian ini menjelaskan memori-memori yang berbeda yang dimiliki oleh ATmega16. Arsitektur AVR memiliki dua jenis memori, yaitu memori program dan memori data. ATmega16 memiliki tambahan EEPROM yang digunakan sebagai memori penyimpan data. Semua memori ini adalah linear.

Memori program dari ATmega16 berjenis Flash memori, yang memiliki kemanpuan *in system programmable*, yang berarti dapat diprogram tanpa dilepas dari sistem, dengan menggunakan koneksi SPI. Hal ini juga yang membuat ATmega16 mudah diprogram, karena hanya memerlukan empat kabel data untuk memprogramnya. Memori program ini memiliki kapasitas 8Kb, yang diatur dalam konfigurasi 4K x 16, karena instruksi-instruksi pada arsitektur AVR memiliki lebar 16 atau 32 bit. Memori program ini memiliki dua bagian, yaitu bagian aplikasi *flash*, dan bagian *boot flash*, yang memungkinkan *Read-While-Write Self Programming*. Memori ini memiliki daya tahan sebesar 10.000 kali pemrograman dan penghapusan.

Memori data pada ATmega16 berupa SRAM, dengan 608 alamat lokasi. Pada 96 alamat lokasi yang pertama terdapat *register-register* dan memori *I/O*, sedangkan 512 sisanya adalah memori data internal. Terdapat lima cara pengalamatan memori yang didukung oleh ATmega16, yaitu: langsung, tidak langsung, tidak langsung dengan *displacement*, tidak langsung dengan pengurangan sebelumnya, dan tidak langsung dengan penambahan setelahnya. Seluruh 32 register serba guna, 64 register *I/O*, dan 512 byte memori data internal dapat diakses menggunakan kelima cara ini.

ATmega16 memiliki EEPROM untuk penyimpanan data sebesar 512 byte, dengan daya tahan 100.000 kali pemrograman dan penghapusan, yang diatur dengan cara yang berbeda hingga tiap byte dapat diprogram atau dihapus secara individu. Akses menuji EEPROM ini adalah dengan melalui register alamat EEPROM, register data EEPROM, dan register kontrol EEPROM.

2.3.1.3. Internal ADC

Salah satu alasan pemilihan ATmega16 adalah karena ATmega16 memiliki *Analog to Digital Converter* internal dengan resolusi 10-bit. ADC ini dikombinasikan dengan *multiplexer* analog 8 bit sehingga memiliki 8 input yang dibentuk olek pin-pin pada Port A. ADC ini memiliki rangkaian *sample-and-hold* yang memastikan agar

masukan ADC tetap konstan selama konversi berlangsung. ADC internal pada ATmega16 memiliki masukan catu daya tersendiri, yang tidak boleh memiliki perbedaan lebih dari +-0.3V dari VCC ATmega16. Tegangan referensi sebesar 2.56V disediakan oleh ATmega16, dan dapat ditentukan dari luar melalui pin AREF.

ADC ini mengkonversi tegangan masukan analog menjadi nilai 10-bit melalui *succesive approximation*. Nilai minimum mewaliki GND dan nilai maksimum adalah AVCC dikurangi 1 LSB. Tegangan referensi pada AREF dapat dihubungkan ke catu tegangan 2.56V internal, AVCC, atau dihubungkan pada sumber tegangan dari luar.

2.3.2. Mikrokontroler AT89S51

Mikrokontroller AT89S51 adalah mikrokontroller buatan ATMEL yang kompatibel penuh dengan mikrokontroler keluarga MCS - 51, hanya membutuhkan daya rendah, memiliki performance yang tinggi dan merupakan mikrokomputer 8 bit yang dilengkapi 4Kbyte EEPROM *(Electrical Erasable and Programmable Read Only Memory)* dan 128 Byte RAM internal. Program memori dapat diprogram dalam sistem atau menggunakan programmer *Nonvolatile* Memory konvensional. Dalam sistem mikrokontroller terdapat dua hal yang mendasar, yaitu: perangkat lunak dan perangkat keras yang keduanya saling terkait dan mendukung.

Secara umum Mikrokontroller AT89S51 memiliki :

- CPU 8 bit termasuk keluarga MCS-S I
- 4 Kb Flash memory
- 128 byte Internal RAM
- 32 buah Port I/O,masing - masing terdiri atas 8 jalur I/O
- 2 Timer / counter 16 bit
- 2 Serial Port Full Duplex
- 2 DPTR (Data pointer)

- *System Interrupt* dengan 2 sumber *Interrupt* eksternal dan 4 sumber *Interrupt* internal.
- Fleksibel ISP Programming

Dengan keistimewaan diatas pembuatan alat menggunakan AT89S51 menjadi lebih sederhana dan tidak memerlukan IC pendukung yang banyak.

2.3.2.1. Konfigurasi Pin AT89S51

Fungsi tiap-tiap pin-nya adalah sebagai berikut :

Tabel 2.2
Konfigurasi Pin Mikrokontroler AT89S51 Versi PDIP

Nomor *Pin*	Nama	Fungsi
40	VCC	Catu tegangan mikrokontroller
20	GND	Ground
39 s.d. 32	PORT0	Port 0 adalah port *I/O* 8-bit dua arah. Port 0 juga dapat dikonfigurasikan sebagai bagian bawah dari bus alamat/data saat mengakses memori eksternal.
1 s.d. 8	PORT1	Port 1 adalah port *I/O* 8-bit dua arah, dengan *pull-up* internal. Port 1 juga menerima alamat bagian bawah saat pemrograman *Flash*. Port 1.5 hingga Port 1.7 juga digunakan untuk fasilitas ISP, yang ditunjukkan pada tabel II-3.
21 s.d. 28	PORT2	Port 2 adalah port *I/O* 8-bit dua arah, dengan *pull-up* internal. Port 2 juga dapat dikonfigurasiikan sebagai bagian atas dari *address bus* saat mengakses memori eksternal.
10 s.d. 17	PORT3	Port 3 adalah port *I/O* 8-bit dua arah, dengan *pull-up* internal. Port 3 juga memiliki fungsi-fungsi lain yang ditunjukkan pada tabel II-3.
19	XTAL1	XTAL1 adalah masukan bagi penguat pembalik

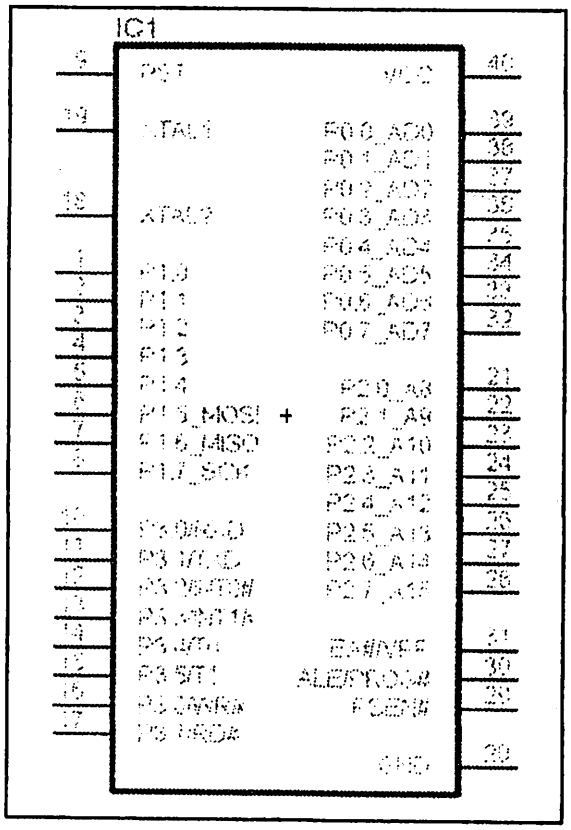
		oscillator dan masukan untuk rangkaian *clock* internal.
18	XTAL2	XTAL2 adalah keluaran dari penguat pembalik *oscillator*.
31	$\overline{EA}$/VPP	*External Access Enable*. $\overline{EA}$ harus dihubungkan ke GND bila ingin menjalankan program pada memori eksternal. $\overline{EA}$ harus dihubungkan ke VCC untuk mengeksekusi program internal. Pin ini juga menerima tegangan +12V saat pemrograman *Flash*.
30	ALE/$\overline{PROG}$	ALE mengeluarkan pulsa untuk mengunci alamat rendah saat mengakses memori eksternal.
29	$\overline{PSEN}$	$\overline{PSEN}$ adalah *strobe* baca untuk memori eksternal.
9	RST	Masukan reset. Pulsa tinggi pada pin ini selama dua siklus mesin akan me-reset mikrokontoler.

Sumber: Datasheet AT89S51

Tabel 2.3
Fungsi Alternatif Pin-Pin AT89S51

Nomor Pin	Nama Pin	Fungsi Alternatif
6	P1.5	MOSI (untuk fungsi ISP)
7	P1.6	MISO (untuk fungsi ISP)
8	P1.7	SCK (untuk fungsi ISP)
10	P3.0	RXD, port masukan serial
11	P3.1	TXD, port keluaran serial
12	P3.2	$\overline{\text{INT0}}$, *interrupt* eksternal 0
13	P3.3	$\overline{\text{INT1}}$, *interrupt* eksternal 1
14	P3.4	T0, input eksternal timer 0
15	P3.5	T1, input eksternal timer 1
16	P3.6	$\overline{\text{WR}}$, external data memory write strobe
17	P3.7	$\overline{\text{RD}}$, external data memory read strobe

Sumber: Datasheet AT89S51



Gambar 2.5
Simbol Skematik AT89S51
Sumber: Program Eagle 4.16r2

2.3.3. Pemetaan Memori AT89S51

Mikrokontoller AT89S51 memiliki ruang alamat memori data dan memori program yang terpisah. Pemisahan memori program dan memori data tersebut membolehkan memori data diakses dengan alamat 8-bit, sehingga dapat dengan cepat dan mudah disimpan dan dimanipulasi oleh CPU 8-bit. Namun demikian, alamat memori data 16-bit bisa juga dihasilkan melalui register DPTR.

2.3.3.1. Program Memory

Program memori hanya dapat dibaca, tidak dapat ditulis. Disini tersimpan program yang akan dijalankan oleh AT89S51 dan data-data konstanta. Sinyal pembacaan EPROM eksternal adalah dari pin-PSEN. Pada AT89S51 ada dua tipe organisasi memori dari program memori, yaitu :

- Pengaksesan program memori sebagian berasal dari internal EPROM yang menempati alamat terendah dan alamat berikutnya dari EPROM eksternal. Sebagai contoh alamat 4 Kbyte program memori terendah adalah ROM internal dan alamat berikutnya adalah pada EPROM.
- Pengaksesan program memori yang semuanya dari eksternal EPROM.

2.3.3.2. Data Memori

Data memori menempati alamat yang terpisah dari program memori. Data memori merupakan tempat penyimpanan data variabel, operasi *stack* dan sebagainya. Data memori dapat dibaca dan ditulis. Sinyal pembacaan untuk emsternal RAM berasal dari pin –RD dan untuk penulisan berasal dari pin –RW.

Alamat 00H-FFH merupakan alamat dari internal RAM yang dapat dialamati dalam dua mode. Pada alamat 00H-7FH dapat dialamati dalam *mode direct* maupun *indirect addressing*. Alamat 80H-FFH hanya dapat dialamati dalam *mode direct addressing*. Diluar alat tersebut merupakan alamat eksternal RAM. 32 byte terendah data memori terbagi atas 4 buah bank yang masing-masing terdiri aas 8 buah register. Kombinasi dari bank ini ditentukan oleh register PSW. Register-register tersebut adalah R0 sampai R7 yang menempati alamat 00H-1FH. Diatasnya merupakan segmen bit *addresable* yang besarnya 16 byte, menempati alamat 20H sampai 2FH. Alamat berikutnya yaitu mulai 30H sampai 7FH dapat dipakai sebagai data RAM.

Setelah kondisi reset, kondisi baku register SP (*stack pointer)* akan menuju alamat 07H dan begitu program dijalankan isi register SP akan ditambah 1 (menunjuk ke alamat 08H). Dan ini merupakan register bank 1 register R0. Bila memakai lebih dari satu bank register maka SP harus diinisialisasikan ke lokasi yang lain.

2.3.3.3. SFR (Special Function Register)

Register Fungsi Khusus *(Special Function Register)* terletak pada 128 byte bagian atas memori data internal dan berisi register-register untuk pelayanan latch port, timer, program status words, control peripheral, dan sebagainya.

Tabel 2.4 Special Function Register

Simbol	Nama Register	Alamat
ACC	Accumulator	E0H
B	Register B	F0H
PSW	Program Status Word	D0H
SP	Stack Pointer	81H
DPTR	Data Pointer	
DPL	DPTR Byte Rendah	82H
DPH	DPTR Byte Tinggi	83H
P0	Port 0	80H
P1	Port 1	90H
P2	Port 2	A0H
P3	Port 3	B0H
IP	Interrupt Periority Control	D8H
IE	Interrupt Enable Control	A8H
TMOD	Timer/Counter Mode Control	89H
TCON	Timer/Counter Control	88H
TH0	Timer/Counter High 0	8CH
TL0	Timer/Counter Low 0	8AH
TH1	Timer/Counter High 1	8DH
TL1	Timer/Counter Low 1	8BH
SCON	Serial Control	98H
SBUF	Serial Data Buffer	99H
PCON	Power Control	87H

Sumber: Datasheet AT89S51

Beberapa register fungsi khusus yang sering digunakan adalah sebagai berikut ini :

- *Accumulator* (ACC) merupakan register untuk penambahan dan pengurangan, selain sebagai register serbaguna (*scratchpad register*). Perintah *mnemonic* untuk mengakses akumulator disederhanakan sebagai A.
- *Register B* merupakan register khusus yang berfungsi melayani operasi perkalian dan pembagian. Selain itu, register ini dapat digunakan sebagai register serbaguna (*scratchpad register*).
- *Stack Pointer* (SP) merupakan register 8 bit yang menunjukkan posisi awal dari stack pada RAM.
- *Data Pointer* (DPTR) terdiri dari dua register, yaitu untuk byte tinggi *(Data Pointer High,* DPH) dan byte rendah *(Data Pointer Low,* DPL) yang berfungsi untuk menunjuk alamat 16 bit.
- *Port 0* sampai *Port 3* merupakan register yang berfungsi untuk membaca dan mengeluarkan data pada port 0, 1, 2, 3. Masing-masing register ini dapat di alamati per-*byte* maupun per-bit.
- *Control Register* terdiri dari register yang mempunyai fungsi kontrol. Untuk mengontrol sistem interupsi, terdapat dua register khusus, yaitu register IP *(Interupt Priority)* dan register IE *(Interupt Enable).* Untuk mengontrol pelayanan timer/counter terdapat register khusus, yaitu register TCON *(timer/counter control)* serta pelayanan port serial menggunakan register SCON *(Serial Port Control).*

2.4. Teknik Modulasi

Dalam sistem telekomunikasi, modulasi adalah proses mengubah sebuah sinyal gelombang, seperti nada, dengan tujuan menggunakan sinyal tersebut untuk membawa suatu informasi. Biasanya, sebuah frekuensi tinggi digunakan sebagai

sinyal pembawa. Tiga hal penting dalam sinyal sinusoudal adalah amplitudo (tegangan), fasa (pewaktuan), dan frekuensi (nada), di mana ketiganya dapat diubah sesuai dengan frekuensi rendah yang merupakan sinyal informasi. Sebuah alat yang melakukan modulasi disebut modulator, sedangkan alat yang mengambil informasi dari sinyal pembawa disebut demodulator. Alat yang melakukan keduanya, modulasi dan demodulasi, disebut sebagai modem.

Dalam modulasi digital, sebuah sinyal analog pembawa dimodulasikan oleh aliran bit digital yang memiliki panjang sama atau berubah-ubah. Hal ini dapat dianggap sebagai perubahan dari analog ke digital. Perubahan pada sinyal pembawa ditentukan oleh simbol-simbol alternatif yang disebut alfabet modulasi.

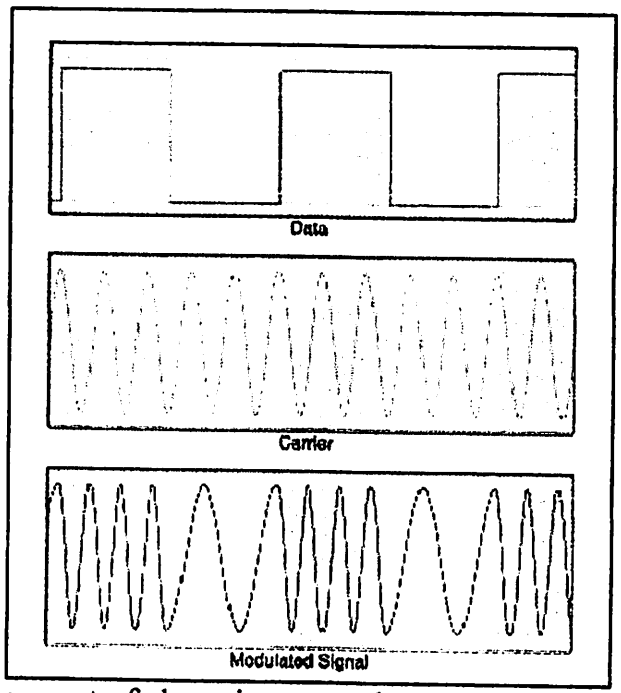
Tiga tipe modulasi digital yang paling umum adalah:

- Amplitude Shift Keying (ASK), di mana karakter yang diubah dari sinyal pembawa adalah amplitudo atau level tegangannya.
- Phase Shift Keying (PSK), di mana karakter yang diubah dari sinyal pembawa adalah fasa atau pewaktuannya.
- Frequency Shift Keying (FSK), di mana karakter yang diubah dari sinyal pembawa adalah frekuensi atau nadanya.

  Selain itu, terdapat pula teknik-teknik modulasi digital lainnya, seperti QAM, dan CW.

2.4.1. Modulasi FSK

Frequency Shift Keying (FSK) adalah sistem modulasi di mana suatu sinyal pembawa diubah frekuensinya sesuai dengan bit digital. Kedua bit digital, 0 dan 1, diasosiasikan dengan suatu frekuensi tertentu dengan periode yang sama. Frekuensi untuk bit 0 disebut sebagai *Space* sedangkan untuk bit 1 disebut sebagai *Mark*.



Gambar 2.6
Modulasi *Frequency Shift Keying*
Sumber: http://en.wikipedia.org/wiki/Frequency_Shift_Keying

2.4.2. IC XR-2206 dan XR-2211

IC XR-2206 adalah IC *function generator* satu keping. Dengan penggunaan satu kapasitor dan 2 resistor tambahan, maka IC ini dapat menjadi sebuah modulator FSK. IC XR-2211 adalah sebuah FSK demodulator/*tone decoder*. Penggunaan kedua IC ini

akan membentuk sebuah modem FSK, di mana XR-2206 adalah sebagai modulator dan XR-2211 sebagai demodulator.

2.5. Komunikasi Serial

Hubungan dari satu alat ke alat yang lain terdiri atas kabel atau media lainnya yang membawa informasi dari satu titik ke titik lainnya, dan antarmuka yang menghubungkan media tersebut ke alat. Kebutuhan dari hubungan ini menentukan antarmuka apa dan media apa yang digunakan untuk menghubungkan titik-titik koneksi tersebut. Koneksi paralel adalah koneksi yang sangat populer. Dengan menggunakan beberapa jalur data, koneksi paralel bisa sangat cepat, karena informasi dikirim tidak per bit. Namun dengan jarak yang jauh dan lebih dari dua alat yang terkoneksi, pengkabelan untuk koneksi paralel menjadi sangat mahal sehingga tidak praktis. Di lain sisi, koneksi serial mengirimkan data per bit, sehingga sangat menghemat kabel, karena untuk komunikasi dua arah hanya diperlukan 2 kabel, yaitu untuk pengiriman data (TX) dan penerimaan data (RX). Tabel II-1 menunjukkan beberapa tipe antarmuka yang sering digunakan.

Tabel 2.5
Tipe Antarmuka Yang Sering Digunakan

Antarmuka	Bentuk	Jumlah alat maksimum	Jarak maksimum dalam feet	Kecepatan maksimum dalam bit / detik
RS-232 (EIA/TIA-232)	Serial asinkron	2	50 - 100	20k 115k dengan beberapa driver
RS-485 (EIA/TIA-485)	Serial asinkron	32 beban unit	4000	10M
IrDA	Infra merah	2	6	115k

	serial asinkron			
Microwire	Serial sinkron	8	10	2M
SPI	Serial sinkron	8	10	2,1M
I^2C	Serial sinkron	40	18	400k
USB	Serial asinkron	127	16	12M
Firewire	Serial	64	15	400M
IEEE-488 (GPIB)	Paralel	15	60	1M
Ethernet	Serial	1024	1600	1G
MIDI	Serial	2	15	31,5k
Port Printer Paralel	Paralel	2, atau 8 dengan dukungan *daisy chain*	10-30	1M

Sumber: Jan Axelson, *Serial Port Complete*, p.6

2.5.1. Antarmuka RS-232

RS-232 adalah salah satu antarmuka komputer yang paling terkenal. Koneksi paling umum yang menggunakan RS-232 adalah untuk menghubungkan modem, tetapi banyak sekali peralatan yang juga menggunakan koneksi ini, seperti untuk printer, modul pengambilan data, alat ukur, dan rangkaian kontrol. RS-232 juga dapat digunakan untuk menghubungkan dua komputer secara sederhana.

RS-232 dirancang untuk komunikasi antar dua alat, dengan batas jarak antara 50 hingga 100 kaki, tergantung pada *bit-rate* dan tipe kabel. Karena RS-232 sangatlah populer, salah satu koneksi yang umum adalah untuk menghubungkan *adapter* untuk tipe antarmuka yang lain.

Keunggulan dari RS-232 adalah:

- Ada di mana-mana. Setiap komputer memiliki satu atau lebih *port* RS-232, walaupun spesifikasi PC98 dari Microsoft menyarankan penggunaan USB.
- Pada mikrokontroler, IC-IC antarmuka memudahkan untuk mengubah level tegangan TTL ke RS-232, contohnya adalah IC MAX232 dan MAX233.
- Jarak hubungan bisa mencapai 50 hingga 100 kaki. Kebanyakan alat tidak memerlukan hubungan jarak jauh. Antarmuka USB dan paralel hanya menjangkau jarak hingga 30 kaki.
- Hanya diperlukan 3 kabel untuk berkomunikasi 2 arah. Komunikasi paralel memerlukan 8 kabel untuk berkomunikasi 8-bit.

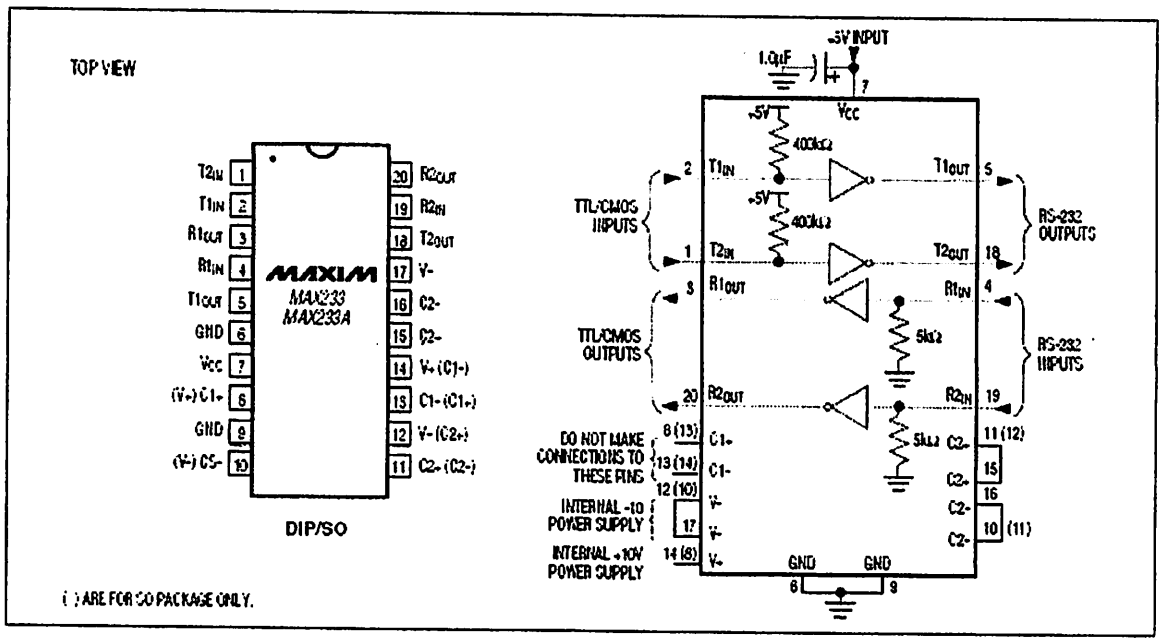
Kekurangan dari RS-232 adalah:

- Bila salah satu ujung koneksi memerlukan data paralel, data serial harus diubah menjadi data paralel. Hal ini mudah dilakukan dengan menggunakan UART.
- Dibatasi dua alat untuk satu hubungan.
- Dalam spesifikasinya, kecepatan maksimum data adalah 20,000 bit per detik. Banyak IC antarmuka dapat melebihi batasan ini, terutama untuk hubungan jarak pendek.
- Jarak yang sangat jauh memerlukan antarmuka yang lain, contohnya RS-485.

Dalam antarmuka RS-232, dikenal istilah DTE dan DCE. DTE adalah *Data Terminal Equipment*, yaitu bagian pengirim data. Bagian modem disebut DCE atau *Data Circuit-terminating Equipment*. Komunikasi RS-232 memerlukan 3 signal, yaitu TX (atau TD atau TXD) yang membawa data dari DTE ke DCE, RX (atau RD

atau RXD) yang membawa data dari DCE ke DTE, dan SG (atau SGND atau GND) yaitu *signal ground*. Level logika RS-232 adalah sbb: logika 1 adalah sama dengan atau lebih rendah dari -5V, dan logika 0 adalah sama dengan atau lebih tinggi dari +5V. Bila koneksi sangat panjang, level tegangan dapat menurun akibat resistansi kabel. Oleh karena itu, batas ini ditoleransi hingga -3V dan +3V.

2.5.2. IC MAX233



Gambar 2.7
***Pinout* IC MAX233**
Sumber: Datasheet MAX233

Dalam *datasheet*, IC MAX232 disebut sebagai *+5V Powered, Multichannel RS-232 Driver/Receiver*, atau IC driver RS-232 multikanal dengan sumber +5V. IC ini ditujukan untuk komunikasi RS-232 di mana tegangan +12 tidak tersedia. Fitur utama dari IC MAX233 adalah tidak diperlukannya kapasitor eksternal, tidak seperti IC MAX232 yang membutuhkan empat kapasitor 1uF.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BAB III
PERENCANAAN DAN PEMBUATAN ALAT

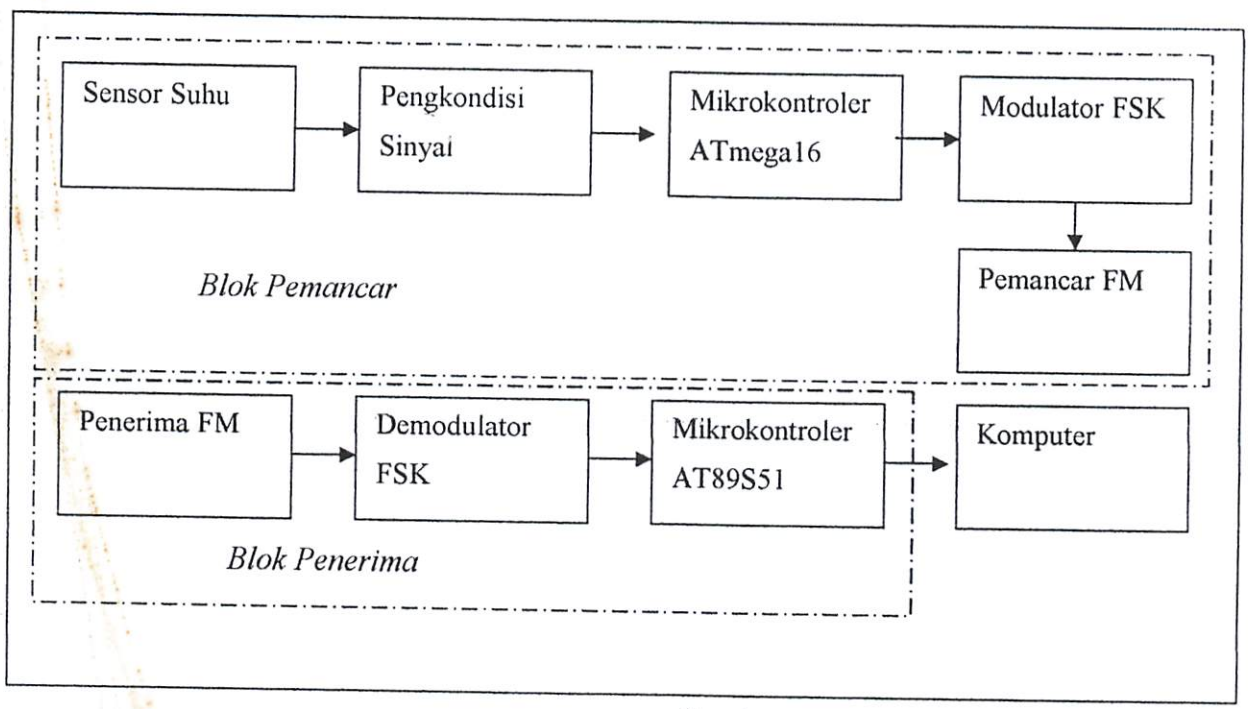
3.1. Pendahuluan

Alat telemetri suhu dengan fasilitas pencatatan pada komputer ini memiliki dua bagian, yaitu:

Pemancar, yang terdiri atas sensor suhu, pengkondisi sinyal, mikrokontroler ATmega16, modulator FSK, dan pemancar FM.

- Penerima, yang terdiri atas penerima radio FM, demodulator FSK, mikrokontroler AT89S51, antarmuka RS-232.

3.2. Blok Diagram



Gambar 3.1
Blok Diagram Sistem

3.3. Perencanaan Sensor Suhu

Dalam perencanaan alat ini, sensor suhu menggunakan IC LM35. Penggunaannya sederhana sekali karena tidak memerlukan komponen-komponen tambahan, dengan catu tegangan cukup +5V dapat mendeteksi tegangan hingga 100°C. Hal ini dirasa sudah cukup, sehingga IC LM35 ini langsung dihubungkan ke rangkaian pengkondisi sinyal.

3.4. Perencanaan Pengkondisi Sinyal

Rangkaian pengkondisi sinyal terdiri atas dua bagian, yaitu rangkaian penyangga dan rangkaian penguatan, untuk keduanya menggunakan satu IC LM358. Rangkaian penyangga menghubungkan IC LM35 agar tidak terbebani oleh rangkaian lainnya.

Keluaran dari rangkaian penyangga dihubungkan pada penguat tak membalik. Fungsi dari rangkaian penguatan adalah mengatur agar batas tegangan keluaran sensor LM35 sesuai dengan jangkauan ADC dari ATmega16. Dalam rangkaian ini, jangkauan suhu yang ingin dicatat adalah antara 10°C hingga 100°C. Keluaran dari LM35 adalah 10mV/°C, oleh karena itu, tegangan keluaran maksimum dan minimum LM35 adalah:

$$Vmax = 100 \times 0{,}01$$
$$= 1V$$

$$Vmin = 10 \times 0.01$$

$$= 0.1V$$

Agar tegangan maksimum mencapai batas tertinggi dari ADC, yaitu Vref = 2.56V, maka diperlukan penguatan.

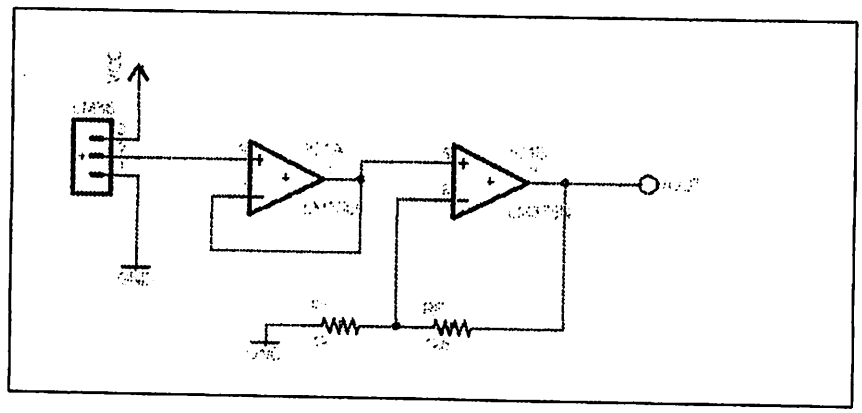
$$2.56 = AV \times Vmax$$
$$AV = 2.56/1$$
$$= 2.56$$

Oleh karena itu, penguatan dirancang dengan penguatan kira-kira 2.5 kali.

$$AV = \frac{R_2}{R_1} + 1$$
$$AV = \frac{1500}{1000} + 1$$
$$= 1.5 + 1$$
$$= 2.5$$

Dengan penguatan sebesar ini, maka tegangan keluaran maksimum dan minimum menjadi:

$$Vout = AV \times Vin$$
$$Vmax = 2{,}5 \times 1$$
$$= 2{,}5V$$
$$Vmin = 2{,}5 \times 0.1$$
$$= 0{,}25V$$



Gambar 3.2
Perencanaan Sensor Suhu dan Pengkondisi Sinyal

3.5. Perencanaan Mikrokontroler ATmega16

Mikrokontroler ATmega16 digunakan sebagai pengambil data dari sensor suhu, yang kemudian diolah ke bentuk digital, untuk dikirimkan ke mikrokontroler AT89S51 melalui radio FM dengan modulasi data FSK. Fitur dari ATmega16 yang digunakan adalah ADC internal dan USART.

3.5.1. Rangkaian ADC

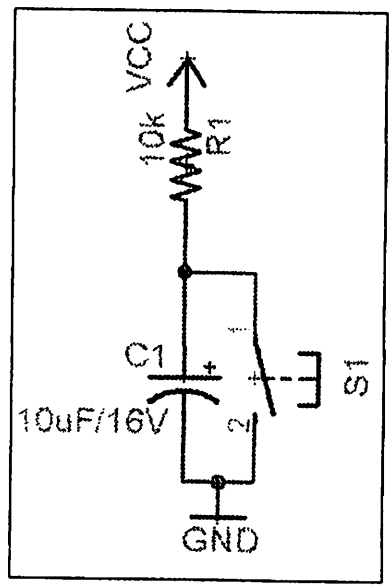
ATmega16 memiliki ADC internal 8 jalur dengan resolusi 10-bit. Fitur ini memerlukan catu tegangan pada pin AVCC dan AGND, di mana tiap pin tidak boleh memiliki perbedaan lebih dari 0.3V dari VCC dan GND mikrokontroler. Tegangan referensi ADC yang digunakan adalah tegangan referensi internal 2.56V, yang dipilih dengan cara mengaktifkan bit REFS1:0 pada register ADMUX. Untuk itu, diperlukan kapasitor sebagai penstabil tegangan pada pin AREF.

3.5.2. Rangkaian Serial

Rangkaian serial menghubungkan ATmega16 ke modulator FSK, melalui sebuah resistor *pull-up*. Selebihnya dilakukan secara software.

3.5.3. Rangkaian Reset

Mikrokontroler ATmega16 dapat di-reset dengan cara memberikan logika rendah pada pin 9 selama dua siklus mesin. Untuk mencegah agar hal ini tidak terjadi tanpa disengaja, maka diperlukan rangkaian yang dapat menahan logika tinggi pada pin 9 selama lebih dari dua siklus mesin. Untuk memungkinkan reset manual, diberikan sebuah push-button.

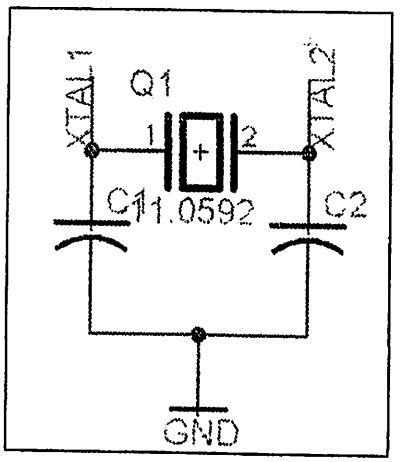


Gambar 3.3
Perencanaan Rangkaian Reset ATmega16

3.5.4. Rangkaian *Oscillator*

Mikrokontroler ATmega16 mendukung *clock speed* hingga 16 MHz dengan penggunaan *oscillator* eksternal. *Oscillator* yang digunakan dalam rangkaian ini adalah *crystal oscillator* 11,0592 MHz, dengan pertimbangan untuk memudahkan

perhitungan *baud rate* untuk komunikasi serialnya. Menurut *AVR Design Consideration*, nilai kapasitor pada kristal yang digunakan sebaiknya berada dalam rentang 22 – 33 pF.



Gambar 3.4
Perencanaan Rangkaian Oscillator ATmega16

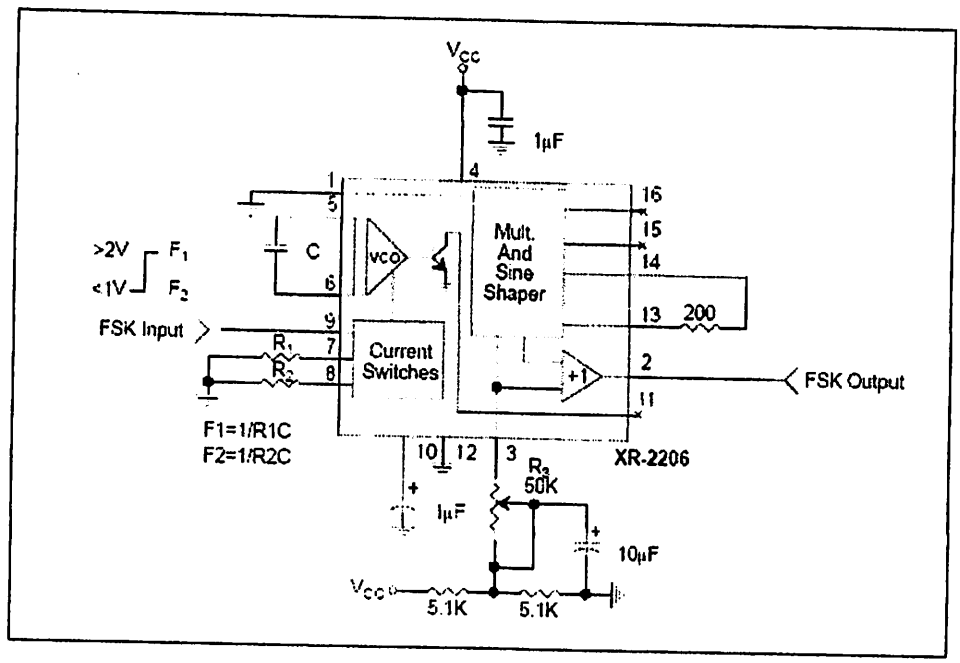
3.6. Perencanaan Modulator FSK

Untuk modulator FSK, digunakan IC XR-2206. Dari datasheet, rangkaian XR-2206 sebagai FSK *generator* adalah seperti pada gambar III-2.

Frekuensi *mark* dan *space* ditentukan oleh komponen-komponen C_1 pada pin 5-6, dan R_1 pada pin 7 dan R_2 pada pin 8.

$$Fmark = 1/R_1C$$
$$Fspace = 1/R_2C$$

Tabel III-1 menunjukkan kombinasi komponen yang menentukan frekuensi mark dan space, dengan memperhatikan ketersediaan nilai-nilai komponen yang tersedia di pasaran.

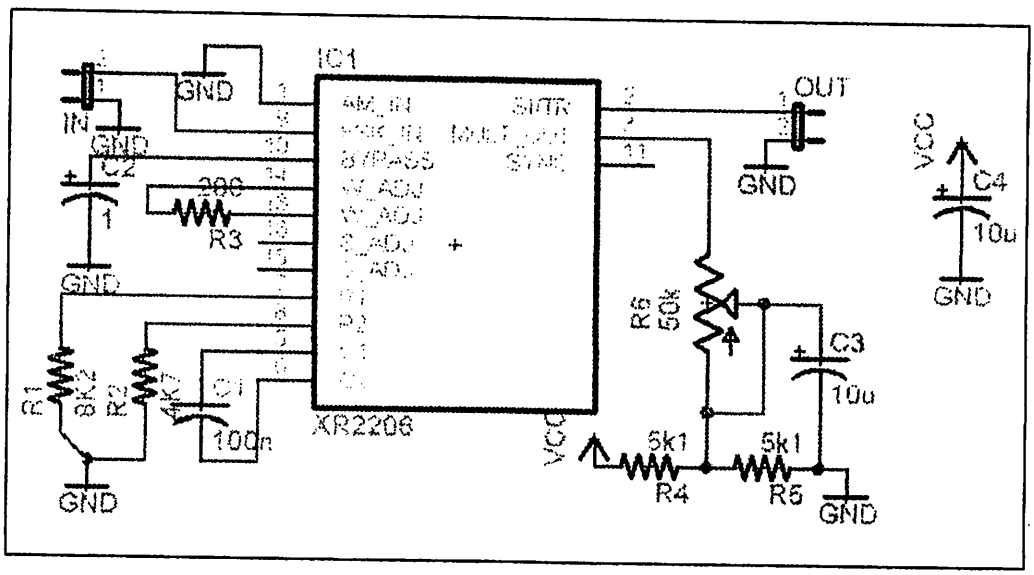


Gambar 3.5
Penggunaan XR-2206 Sebagai Sinusoidal FSK Generator
Sumber: Datasheet

Tabel 3.1
Kombinasi Komponen Penentu Frekuensi *Mark* dan *Space*

No	Fmark (Hz)	Fspace (Hz)	C (uF)	R1 (kOhm)	R2 (kOhm)
1	96.71	212.77	4.70	2.20	1.00
2	31.29	45.27	4.70	6.80	4.70
3	259.47	967.12	0.47	8.20	2.20
4	379.94	967.12	0.47	5.60	2.20
5	2127.66	9090.91	0.10	4.70	1.10
6	1724.14	4545.45	0.10	5.80	2.20
7	1200.00	2200.00	0.10	8.33	4.55
8	1219.51	2127.66	0.10	8.20	4.70

Berdasarkan tabel tersebut, untuk mendapatkan frekuensi *mark* sekitar 1 kHz dan frekuensi *space* sekitar 2 kHz, dengan memperhatikan ketersediaan komponen, maka kombinasi yang dipilih adalah kombinasi 8.



Gambar 3.6
Perencanaan FSK Modulator

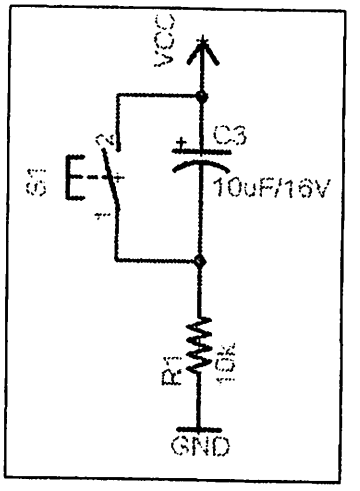
Perencanaan Mikrokontroler AT89S51

Fitur dari IC AT89S51 yang diperlukan dalam sistem ini adalah fitur komunikasi serialnya, yang digunakan untuk menterjemahkan data serial kiriman dari ATmega16, yang kemudian dikirimkan ke komputer. Agar mikrokontroler ini dapat bekerja, diperlukan beberapa komponen untuk membentuk minimum system. Rangkaian-rangkaian yang diperlukan adalah rangkaian reset, rangkaian oscillator, dan rangkaian antarmuka RS-232.

3.6.1. Rangkaian Reset

Mikrokontroler AT89S51 dapat di-*reset* dengan cara memberikan logika tinggi pada pin 10 selama dua siklus mesin. Untuk mencegah agar hal ini tidak terjadi tanpa

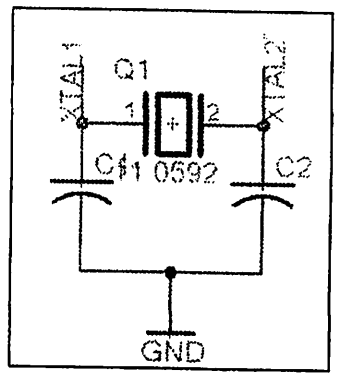
disengaja, maka diperlukan rangkaian yang dapat menahan logika tinggi pada pin 10 selama lebih dari dua siklus mesin. Untuk memungkinkan *reset* manual, diberikan sebuah *push-button*.



Gambar 3.7
Perencanaan Rangkaian Reset AT89S51

3.6.2. Rangkaian Oscillator

Mikrokontroler AT89S51 mendukung *clock speed* hingga 24 MHz dengan penggunaan *oscillator* eksternal. *Oscillator* yang digunakan dalam rangkaian ini adalah *crystal oscillator* 11,0592 MHz, dengan pertimbangan untuk memudahkan perhitungan *baud rate* untuk komunikasi serialnya. Menurut *AVR Design Consideration*, nilai kapasitor pada kristal yang digunakan sebaiknya berada dalam rentang 22 – 33 pF.



Gambar 3.8
Perancangan Rangkaian Oscillator AT89S51

3.7. Perencanaan Demodulator FSK

Untuk mengambil data yang termodulasi dalam bentuk FSK dibutuhkan sebuah demodulator. Dalam perancangan ini, digunakan IC Exar XR2211, dengan alasan diproduksi oleh produsen yang sama dengan modulator FSK yang digunakan.

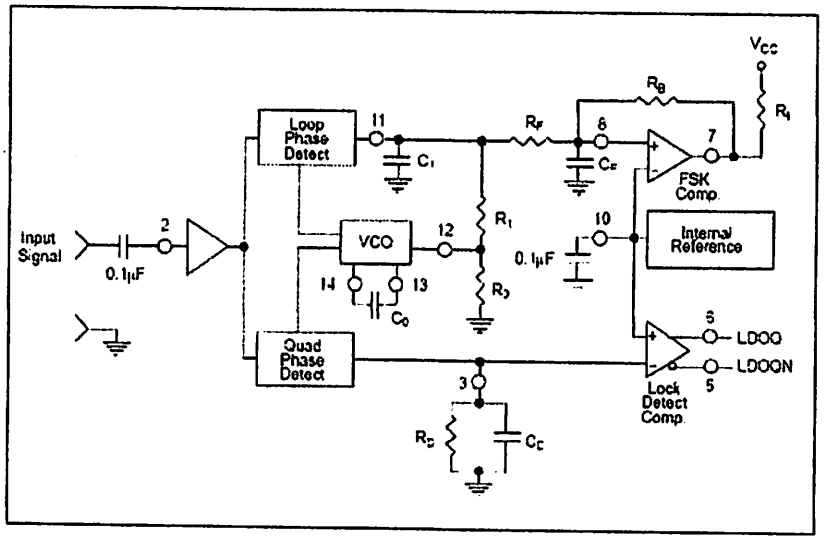
Menurut *Design Instruction* pada *datasheet* IC XR2211, ada beberapa hal yang harus dihitung.

- Menghitung frekuensi tengah dari PLL.

$$f_0 = \sqrt{F_1 F_2}$$

$$f_0 = \sqrt{1219.51x2127.66}$$

$$= 1610.80Hz$$



Gambar 3.9
XR2211 Sebagai Demodulator FSK
Sumber: datasheet XR2211

- Menghitung nilai resistor *timing* R_0, yang harus berukuran antara 10kohm hingga 100kohm. Nilai yang disarankan adalah 20 kOhm. Nilai akhirnya biasanya diatur lebih lanjut dengan potensiometer. Dalam hal ini digunakan resistor 10 kOhm dengan potensiometer 10 kOhm.
- $R_0 = 10 + \left(\frac{10}{2}\right) = 15k\Omega$
- Menghitung nilai C_0.
- $C_0 = \frac{1}{15000x1610.80} = 41.4nF$

  Untuk ini maka digunakan kapasitor yang mendekati, yaitu 47nF.
- Menghitung R1 untuk mendapatkan *bandwidth* yang diinginkan.
- $R_1 = \frac{R_0 \cdot f_0}{(f_1 - f_2)} \cdot 2$

$$= \frac{15000x1610.80}{(2127.67 - 1219.51)} \cdot 2$$

$$= 53210\Omega$$

Untuk ini digunakan R1 sebesar 54kOhm.

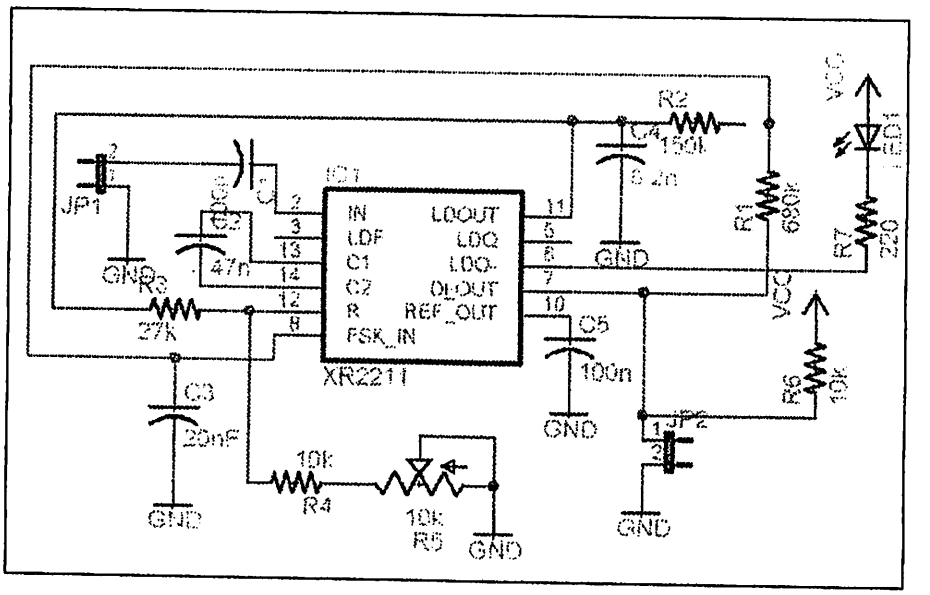
- Menghitung C_1 untuk mengatur peredaman *loop*.
- $C_1 = \frac{1250xC_0}{R1.\zeta^2}$

$$= \frac{1250x47nF}{54000x0.5^2}$$
$$= 8.7nF$$

- Untuk ini digunakan kapasitor 4.7nF.
- Menghitung kapasitansi filter data.
- $R_F = 5.R_1$

$$= 5.27000 = 135000\Omega$$
$$R_B = 5.R_F$$
$$= 5.135000$$
$$= 675000\Omega$$
$$R_{SUM} = \frac{(R_F + R_1).R_B}{(R_1 + R_F + R_B)}$$
$$= \frac{(135 + 21).675}{27 + 135 + 675}$$
$$= 125806\Omega$$
$$C_F = \frac{0.25}{(R_{SUM}.baud\ rate)}$$
$$= \frac{0.25}{125806.9600}$$
$$= 20{,}7nF$$

- Dengan pembulatan, R_B = 680k, R_f= 150k, C_F = 20nF.

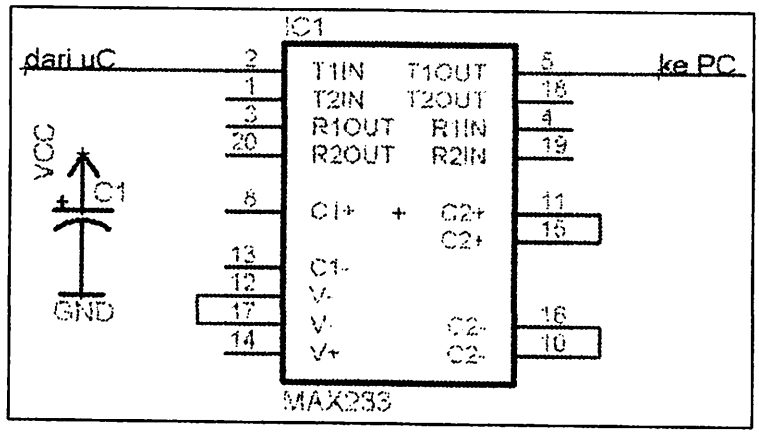


Gambar 3.10
Perencanaan Rangkaian Demodulator FSK

3.8. Perencanaan Antarmuka RS232 dengan IC MAX233

IC MAX233 adalah *level converter* TTL dan RS-232. Fitur utama dari IC ini adalah tidak diperlukannya kapasitor-kapasitor eksternal seperti pada IC MAX232. Oleh karena itu, tidak diperlukan rangkaian komponen apapun untuk dapat bekerja.

Dalam perencanaan, rangkaian MAX233 digunakan untuk komunikasi *simplex*, yaitu hanya digunakan untuk mengirimkan data dari mikrokontroler AT89S51 ke komputer, dan tidak sebaliknya. Oleh karena itu, pin *TXD* pada mikrokontroler dihubungkan ke pin TTL input dari IC max233. Kedua pin C2+ dihubungkan, demikian juga kedua pin C2- dan kedua pin V- (pin 12 dan 17), sesuai instruksi dari *datasheet*.



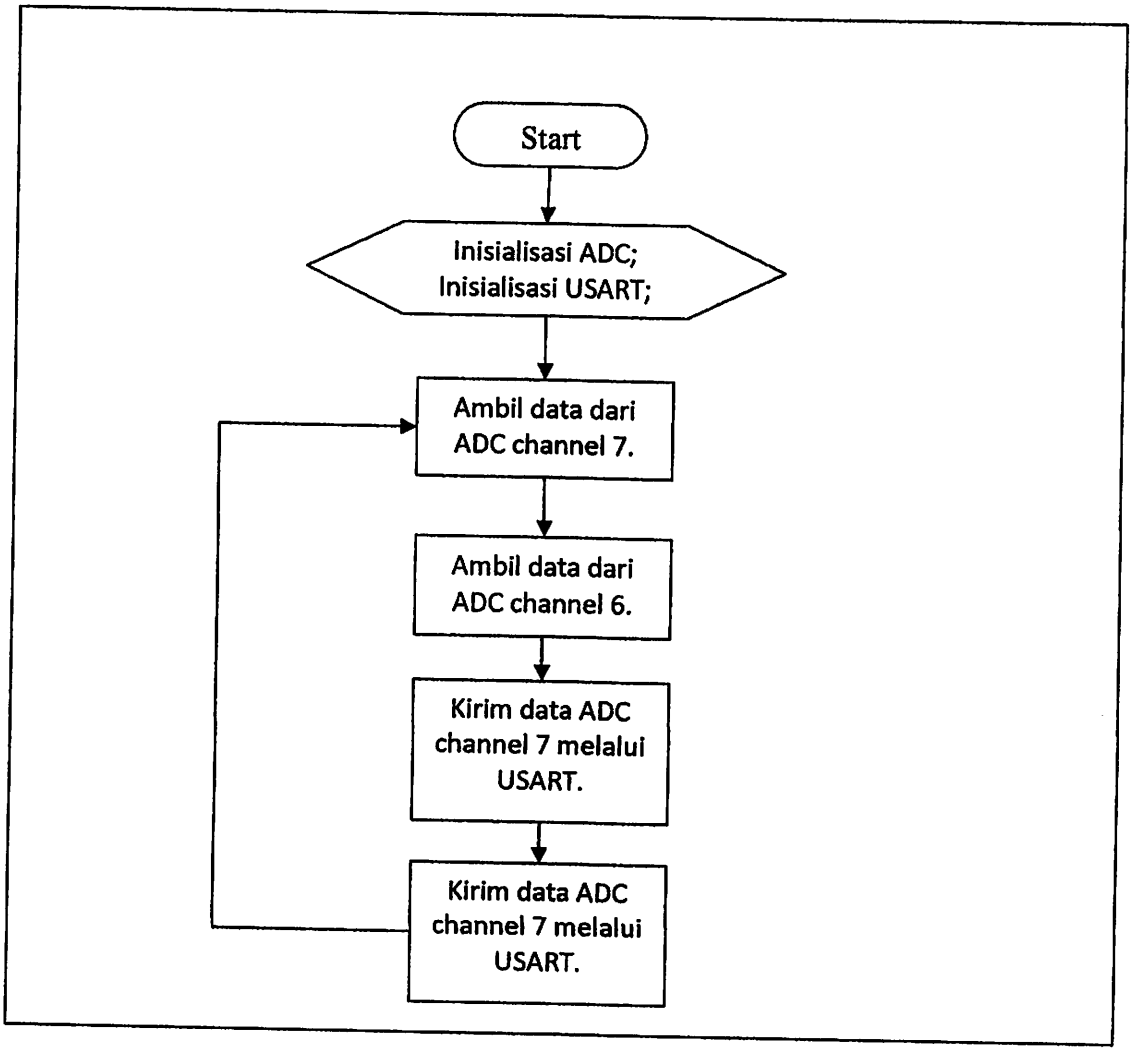
Gambar 3.11
Perencanaan Antarmuka RS232 dengan IC MAX233

3.9. Perencanaan Perangkat Lunak Sistem

Tiap blok dari alat ini memiliki satu software yang bekerja sendiri-sendiri, oleh karena itu diperlukan tiga buah diagram alir, satu untuk setiap blok.

3.9.1. Diagram Alir Blok Pemancar

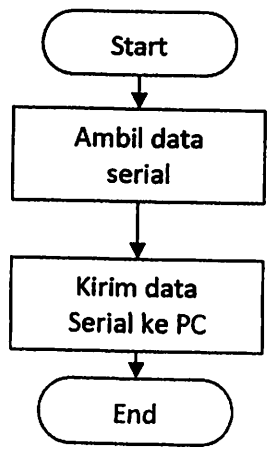
Blok pemancar memiliki mikrokontroler ATmega16 sebagai *CPU*, dengan tugas utama mengambil data dari ADC untuk kemudian dikirimkan melalui pemancar FM dengan modulasi FSK. ADC internal diatur agar menggunakan tegangan referensi (Vref) internal 2.56 V, *left-adjusted*, dengan resolusi yang diambil sebesar 8-bit. Komunikasi serial menggunakan USART, dengan pengaturan 8-bit data, 1-bit stop, tanpa *parity*, dengan kecepatan transfer 4800bps.



Gambar 3.12
Diagram Alir Blok Pemancar

3.9.2. Diagram Alir Blok Penerima

Blok penerima memiliki mikrokontroler AT89S51 sebagai *CPU*, dengan fungsi utama sebagai *buffer*, dengan tugas mengambil data UART, untuk kemudian dikirimkan kembali ke PC melalui UART. UART diatur agar bekerja dengan 8-bit data, 1-bit stop, tanpa *parity*, dengan kecepatan transfer data 4800 bps, agar sesuai dengan blok pemancar.



Gambar 3.13
Diagram Alir Blok Penerima

3.9.3. Cara Kerja Program Komputer

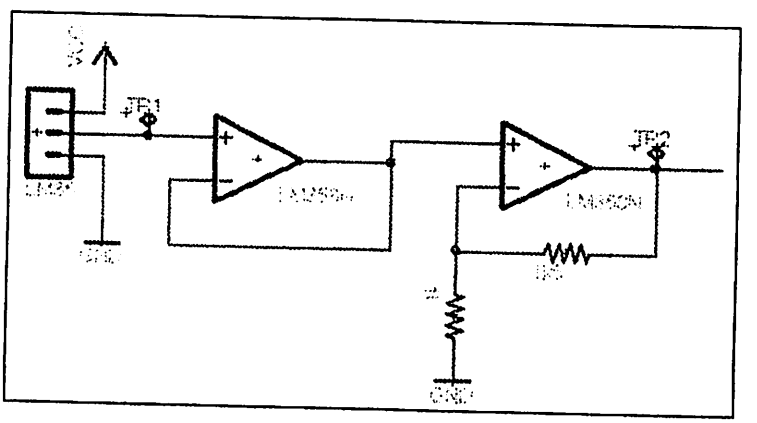
Komputer bertugas untuk menerima data dari blok penerima, untuk kemudian ditampilkan di monitor, dan kemudian dilakukan pencatatan. Dalam simulasi ini, data disimpan tiap 30 detik.

BAB IV
PENGUJIAN ALAT

4.1. Pendahuluan

Dalam bab ini akan diuraikan pengujian terhadap alat untuk melihat kesesuaian antara dasar teori dan perencanaan, kinerja, dan kehandalan dari alat yang dibuat. Pengujian dilakukan atas modul sensor, pengkondisi sinyal, ADC.

4.2. Pengujian Sensor LM35



Gambar 4.1
Rangkaian Pengujian Sensor Suhu dan Pengkondisi Sinyal

Pengujian sensor suhu dilakukan dengan cara mencatat keluaran suhu pada beberapa suhu uji yang berada dalam rentang batas suhu perencanaan. Rangkaian pengujian ditunjukkan pada gambar 4.1, di mana TP1 adalah *test pin* untuk mengukur tegangan keluaran IC LM35.

Tabel 4.1
Hasil Pengujian Sensor dan Pengkondisi Sinyal

Suhu (°C)	Tegangan TP1 (V)	Tegangan TP2 (V)	Gain (kali)
24	0,26	0,67	2,58
29	0,31	0,81	2,61
38	0,40	0,97	2,43
44	0,47	1,01	2,15
53	0,55	1,26	2,29
59	0,61	1,54	2,56
80	0,83	2,01	2,42
91	0,94	2,36	2,51

Dari tabel, terlihat bahwa tegangan keluaran dari IC LM35 tidak sesuai dengan yang tertera pada datasheet, dengan selisih rata-rata 0,023 V. Tabel 4.2 menunjukkan perbedaan perhitungan dan pengukuran sensor suhu.

Tabel 4.2
Perbandingan Hasil Pengukuran dan Perhitungan Sensor Suhu

Suhu	Perhitungan V TP1 (V)	Pengukuran V TP1 (V)	Error TP1 (%)
24	0.24	0,26	8,33
29	0.29	0,31	6,90
38	0.38	0,40	5,26
44	0.44	0,47	6,82
53	0.53	0,55	3,77
59	0.59	0,61	3,39
80	0.80	0,83	3,75
91	0.91	0,94	3,30

Dari tabel, terlihat bahwa keluaran sensor suhu memiliki selisih pengukuran dan perhitungan antara 0.2 – 0.3 v untuk masing-masing suhu, sehingga memiliki tingkat *error* rata-rata sebesar 5.19%.

4.3. Pengujian Pengkondisi Sinyal

Pengujian pengkondisi sinyal dilakukan untuk melihat gain yang dihasilkan atas input dari LM35 sebelum masuk ke ADC. Pengujian ini dilakukan bersamaan dengan pengujian sensor suhu.

Gambar 4.1 menunjukkan rangkaian pengujian sensor suhu dan pengkondisi sinyal. TP2 adalah *test pin* untuk mengukur tegangan keluaran dari pengkondisi sinyal. Tegangan pada TP2 dan TP1 dibandingkan untuk melihat gain yang dihasilkan pada pengkondisi sinyal.

Tabel 4.3
Perbandingan Perhitungan dan Pengukuran Pengkondisi Signal

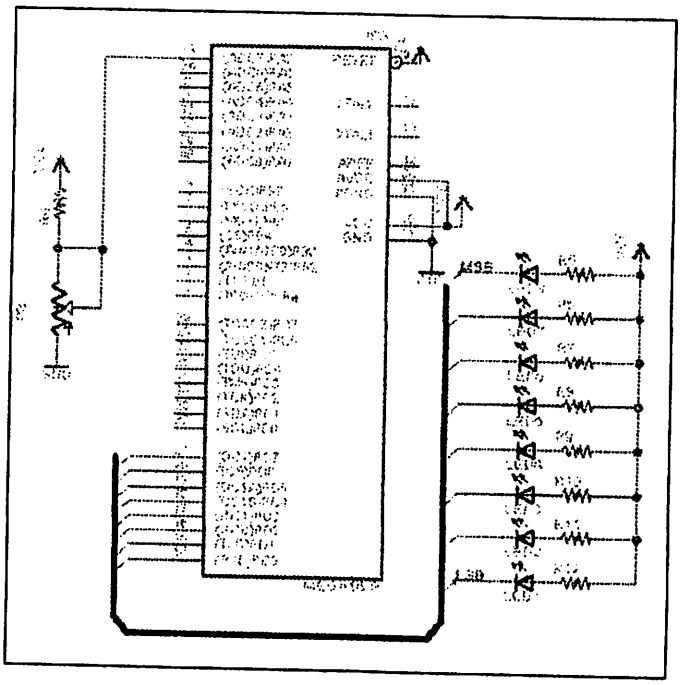
Perhitungan			Pengukuran			Error	
V TP1	V TP2	Gain	V TP1	V TP2	Gain	V TP2	Gain
0.24	0.60	2.56	0,26	0,67	2,58	11,.67	0,78
0.29	0.73	2.56	0,31	0,81	2,61	10,.96	1,95
0.38	0.98	2.56	0,40	0,97	2,43	1,02	5,08
0.44	1.10	2.56	0,47	1,01	2,15	8,18	10,.02
0.53	1.33	2.56	0,55	1,26	2,29	5,26	10,.55
0.59	1.48	2.56	0,61	1,54	2,56	4,05	0,00
0.80	2.00	2.56	0,83	2,01	2,42	0,50	5,47
0.91	2.28	2,56	0,94	2,36	2.51	3,51	1,95

Tingkat *error* dari gain adalah sebesar 5.19%, yang menunjukkan bahwa pengkondisi sinyal ini cukup dapat diandalkan. *Error* terbesar terjadi pada pengukuran antara 0.44V hingga 0.53, yang kemungkinan merupakan *human error*,

karena hanya digunakan satu alat ukur untuk menguji tegangan keluaran dan tegangan masukan.

4.4. Pengujian ADC

Pengujian ADC dilakukan untuk melihat keluaran dari ADC terhadap sinyal analog yang dimasukkan, dengan menggunakan rangkaian yang ditunjukkan pada gambar 4. ADC yang digunakan adalah ADC internal dari mikrokontroler ATmega16, yang dikonfigurasikan sbb: VCC = 5V, Vref = internal Vref 2.56V, Input = ADC7 (PORTA7), *left adjusted result*. Dengan konfigurasi seperti ini, ADC akan memberikan nilai 0x00 pada masukan 0 V dan 0xFF pada masukan 2.56V (tegangan Vref). Keluaran dihubungkan dengan LED yang terhubung pada PORT D. Digunakan tambahan resistor pada bagian input yang dihubungkan secara seri dengan potensiometer agar keluaran dari potensiometer tidak melebihi tegangan referensi internal 2.56V, sehingga nilai maksimum 0xFF tidak terlampaui.



Gambar 4.2
Rangkaian Pengujian ADC

Program yang digunakan dalam pengujian adalah sbb:

```
init:
   ldi r16,0xff
   out DDRD,r16
   ldi r16,0xff
   out PORTD, r16

get_adc_data:
   ; Aktifkan ADC
   sbi ADCSRA,ADEN

loop:
   ; Internal vref, left adjusted, channel 7 as input
   ldi r16,(2<<REFS0) | (1<<ADLAR) | (7<<MUX0)
   out ADMUX,r16
   ; Mulai konversi
   sbi ADCSRA,ADSC
   ; wait until conversion ends
```

```
wait7:
  sbis ADCSRA,ADIF
  jmp wait7
  ; Get conversion data, high byte (8 MSBs)
  in r27,ADCH
  out PORTD,r27
  rcall delay
  jmp loop
```

Tabel 4.4
Hasil Pengujian ADC

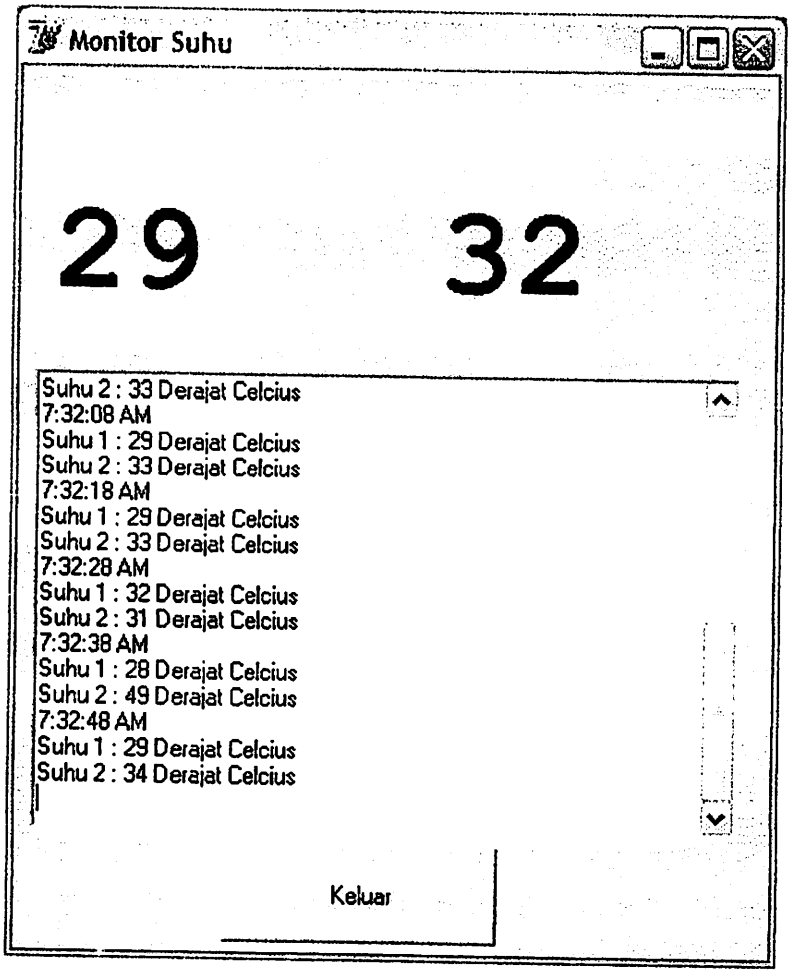
V Input	Keluaran ADC	Nilai Desimal
0.24	00011000	24
0.45	00101101	45
0.68	01000100	68
0.95	01011111	95
1.15	01110010	115
1.58	10011110	158
1.92	11000000	192
2.34	11101001	234
2.45	11110101	245

Terlihat bahwa tiap kenaikan satu bit dari ADC mewakili kenaikan tegangan 0.1 V dari input. Tidak terdapat *error* pada pengujian ini, yang menunjukkan bahwa ADC dari ATmega16 dapat diandalkan.

4.5. Pengujian Program Komputer

Pengujian selanjutnya adalah pengujian perangkat keseluruhan untuk melihat tampilan keseluruhan pada komputer. Metode pengujian adalah dengan mengaktifkan seluruh bagian blok pemancar dan blok penerima, kemudian menghubungkan blok penerima dengan komputer. Pengamatan dilakukan pada program di komputer, yang

menampilkan data yang telah diolah dari bentuk biner menjadi nilai suhu kembali. Gambar 4.3 menunjukkan tampilan suhu pada program komputer.



Gambar 4.3
Tampilan Pada Program Monitor Suhu

Terlihat banyak perubahan suhu dalam waktu hanya 40 detik. Kemungkinan ini disebabkan oleh banyaknya data yang tidak *valid*, yang rusak saat transmisi walaupun sudah menggunakan teknik *checksum*. Untuk mendapatkan validitas data yang lebih baik, maka blok penerima harus melakukan *error-checking*, yang kemudian dikoreksi kembali dengan cara meminta pengiriman kembali ke blok pemancar. Hal ini tidak mungkin karena dalam perancangan, komunikasi yang dirancang adalah satu arah,

sedangkan untuk melakukan *ECC (error-checking and correction)* diperlukan komunikasi dua arah. Hal ini juga akhirnya menurunkan kehandalan alat ini.

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Kedua

National Semiconductor

December 1994

LM35/LM35A/LM35C/LM35CA/LM35D Precision Centigrade Temperature Sensors

General Description

The LM35 series are precision integrated-circuit temperature sensors, whose output voltage is linearly proportional to the Celsius (Centigrade) temperature. The LM35 thus has an advantage over linear temperature sensors calibrated in ° Kelvin, as the user is not required to subtract a large constant voltage from its output to obtain convenient Centigrade scaling. The LM35 does not require any external calibration or trimming to provide typical accuracies of ±¼°C at room temperature and ±¾°C over a full −55 to +150°C temperature range. Low cost is assured by trimming and calibration at the wafer level. The LM35's low output impedance, linear output, and precise inherent calibration make interfacing to readout or control circuitry especially easy. It can be used with single power supplies, or with plus and minus supplies. As it draws only 60 µA from its supply, it has very low self-heating, less than 0.1°C in still air. The LM35 is rated to operate over a −55° to +150°C temperature range, while the LM35C is rated for a −40° to +110°C range (−10° with improved accuracy). The LM35 series is available packaged in hermetic TO-46 transistor packages, while the LM35C, LM35CA, and LM35D are also available in the plastic TO-92 transistor package. The LM35D is also available in an 8-lead surface mount small outline package and a plastic TO-202 package.

Features

- Calibrated directly in ° Celsius (Centigrade)
- Linear + 10.0 mV/°C scale factor
- 0.5°C accuracy guaranteeable (at +25°C)
- Rated for full −55° to +150°C range
- Suitable for remote applications
- Low cost due to wafer-level trimming
- Operates from 4 to 30 volts
- Less than 60 µA current drain
- Low self-heating, 0.08°C in still air
- Nonlinearity only ±¼°C typical
- Low impedance output, 0.1 Ω for 1 mA load

Connection Diagrams

TO-46
Metal Can Package*

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*Case is connected to negative pin (GND)

Order Number LM35H, LM35AH, LM35CH, LM35CAH or LM35DH
See NS Package Number H03H

TO-92
Plastic Package

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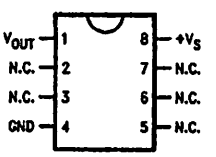
Order Number LM35CZ, LM35CAZ or LM35DZ
See NS Package Number Z03A

SO-8
Small Outline Molded Package



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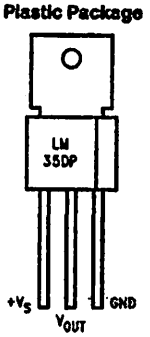
Top View
N.C. = No Connection

Order Number LM35DM
See NS Package Number M08A

TO-202
Plastic Package



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Order Number LM35DP
See NS Package Number P03A

Typical Applications

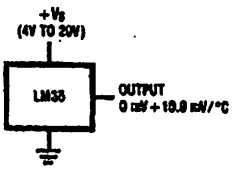

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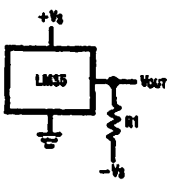
FIGURE 1. Basic Centigrade Temperature Sensor (+2°C to +150°C)



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Choose $R_1 = -V_S/50\ \mu A$

$V_{OUT} = +1{,}500$ mV at +150°C
$= +250$ mV at +25°C
$= -550$ mV at −55°C

FIGURE 2. Full-Range Centigrade Temperature Sensor

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RRD-B30M75/Printed in U. S. A.

Absolute Maximum Ratings (Note 10)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage	+35V to −0.2V
Output Voltage	+6V to −1.0V
Output Current	10 mA
Storage Temp., TO-46 Package,	−60°C to +180°C
TO-92 Package,	−60°C to +150°C
SO-8 Package,	−65°C to +150°C
TO-202 Package,	−65°C to +150°C
Lead Temp.:	
TO-46 Package, (Soldering, 10 seconds)	300°C
TO-92 Package, (Soldering, 10 seconds)	260°C
TO-202 Package, (Soldering, 10 seconds)	+230°C

SO Package (Note 12):	
Vapor Phase (60 seconds)	215°C
Infrared (15 seconds)	220°C
ESD Susceptibility (Note 11)	2500V
Specified Operating Temperature Range: T_{MIN} to T_{MAX} (Note 2)	
LM35, LM35A	−55°C to +150°C
LM35C, LM35CA	−40°C to +110°C
LM35D	0°C to +100°C

Electrical Characteristics (Note 1) (Note 6)

Parameter	Conditions	LM35A			LM35CA			Units (Max.)
		Typical	Tested Limit (Note 4)	Design Limit (Note 5)	Typical	Tested Limit (Note 4)	Design Limit (Note 5)	
Accuracy (Note 7)	T_A = +25°C	±0.2	±0.5		±0.2	±0.5		°C
	T_A = −10°C	±0.3			±0.3		±1.0	°C
	T_A = T_{MAX}	±0.4	±1.0		±0.4	±1.0		°C
	T_A = T_{MIN}	±0.4	±1.0		±0.4		±1.5	°C
Nonlinearity (Note 8)	$T_{MIN} \le T_A \le T_{MAX}$	**±0.18**		**±0.35**	**±0.15**		**±0.3**	°C
Sensor Gain (Average Slope)	$T_{MIN} \le T_A \le T_{MAX}$	**+10.0**	**+9.9, +10.1**		**+10.0**		**+9.9, +10.1**	mV/°C
Load Regulation (Note 3) $0 \le I_L \le 1$ mA	T_A = +25°C	±0.4	±1.0		±0.4	±1.0		mV/mA
	$T_{MIN} \le T_A \le T_{MAX}$	**±0.5**		**±3.0**	**±0.5**		**±3.0**	mV/mA
Line Regulation (Note 3)	T_A = +25°C	±0.01	±0.05		±0.01	±0.05		mV/V
	4V ≤ V_S ≤ 30V	**±0.02**		**±0.1**	**±0.02**		**±0.1**	mV/V
Quiescent Current (Note 9)	V_S = +5V, +25°C	56	67		56	67		µA
	V_S = +5V	**105**		**131**	**91**		**114**	µA
	V_S = +30V, +25°C	56.2	68		56.2	68		µA
	V_S = +30V	**105.5**		**133**	**91.5**		**116**	µA
Change of Quiescent Current (Note 3)	4V ≤ V_S ≤ 30V, +25°C	0.2	1.0		0.2	1.0		µA
	4V ≤ V_S ≤ 30V	**0.5**		**2.0**	**0.5**		**2.0**	µA
Temperature Coefficient of Quiescent Current		**+0.39**		**+0.5**	**+0.39**		**+0.5**	µA/°C
Minimum Temperature for Rated Accuracy	In circuit of *Figure 1*, I_L = 0	+1.5		+2.0	+1.5		+2.0	°C
Long Term Stability	T_J = T_{MAX}, for 1000 hours	±0.08			±0.08			°C

Note 1: Unless otherwise noted, these specifications apply: −55°C ≤ T_J ≤ +150°C for the LM35 and LM35A; −40° ≤ T_J ≤ +110°C for the LM35C and LM35CA; and 0° ≤ T_J ≤ +100°C for the LM35D. V_S = +5Vdc and I_{LOAD} = 50 µA, in the circuit of *Figure 2*. These specifications also apply from +2°C to T_{MAX} in the circuit of *Figure 1*. Specifications in boldface apply over the full rated temperature range.

Note 2: Thermal resistance of the TO-46 package is 400°C/W, junction to ambient, and 24°C/W junction to case. Thermal resistance of the TO-92 package is 180°C/W junction to ambient. Thermal resistance of the small outline molded package is 220°C/W junction to ambient. Thermal resistance of the TO-202 package is 65°C/W junction to ambient. For additional thermal resistance information see table in the Applications section.

Electrical Characteristics (Note 1) (Note 6) (Continued)

Parameter	Conditions	LM35			LM35C, LM35D			Units (Max.)
		Typical	Tested Limit (Note 4)	Design Limit (Note 5)	Typical	Tested Limit (Note 4)	Design Limit (Note 5)	
Accuracy, LM35, LM35C (Note 7)	T_A = +25°C	±0.4	±1.0		±0.4	±1.0		°C
	T_A = −10°C	±0.5			±0.5		±1.5	°C
	T_A = T_{MAX}	±0.8	±1.5		±0.8		±1.5	°C
	T_A = T_{MIN}	±0.8		±1.5	±0.8		±2.0	°C
Accuracy, LM35D (Note 7)	T_A = +25°C				±0.6	±1.5		°C
	T_A = T_{MAX}				±0.9		±2.0	°C
	T_A = T_{MIN}				±0.9		±2.0	°C
Nonlinearity (Note 8)	$T_{MIN} \le T_A \le T_{MAX}$	**±0.3**		**±0.5**	**±0.2**		**±0.5**	°C
Sensor Gain (Average Slope)	$T_{MIN} \le T_A \le T_{MAX}$	**+10.0**	**+9.8, +10.2**		**+10.0**		**+9.8, +10.2**	mV/°C
Load Regulation (Note 3) $0 \le I_L \le 1$ mA	T_A = +25°C	±0.4	±2.0		±0.4	±2.0		mV/mA
	$T_{MIN} \le T_A \le T_{MAX}$	**±0.5**		**±5.0**	**±0.5**		**±5.0**	mV/mA
Line Regulation (Note 3)	T_A = +25°C	±0.01	±0.1		±0.01	±0.1		mV/V
	$4V \le V_S \le 30V$	**±0.02**		**±0.2**	**±0.02**		**±0.2**	mV/V
Quiescent Current (Note 9)	V_S = +5V, +25°C	56	80		56	80		µA
	V_S = +5V	**105**		**158**	**91**		**138**	µA
	V_S = +30V, +25°C	56.2	82		56.2	82		µA
	V_S = +30V	**105.5**		**161**	**91.5**		**141**	µA
Change of Quiescent Current (Note 3)	$4V \le V_S \le 30V$, +25°C	0.2	2.0		0.2	2.0		µA
	$4V \le V_S \le 30V$	**0.5**		**3.0**	**0.5**		**3.0**	µA
Temperature Coefficient of Quiescent Current		**+0.39**		**+0.7**	**+0.39**		**+0.7**	µA/°C
Minimum Temperature for Rated Accuracy	In circuit of *Figure 1*, I_L = 0	+1.5		+2.0	+1.5		+2.0	°C
Long Term Stability	T_J = T_{MAX}, for 1000 hours	±0.08			±0.08			°C

Note 3: Regulation is measured at constant junction temperature, using pulse testing with a low duty cycle. Changes in output due to heating effects can be computed by multiplying the internal dissipation by the thermal resistance.

Note 4: Tested Limits are guaranteed and 100% tested in production.

Note 5: Design Limits are guaranteed (but not 100% production tested) over the indicated temperature and supply voltage ranges. These limits are not used to calculate outgoing quality levels.

Note 6: Specifications in **boldface** apply over the full rated temperature range.

Note 7: Accuracy is defined as the error between the output voltage and 10mv/°C times the device's case temperature, at specified conditions of voltage, current, and temperature (expressed in °C).

Note 8: Nonlinearity is defined as the deviation of the output-voltage-versus-temperature curve from the best-fit straight line, over the device's rated temperature range.

Note 9: Quiescent current is defined in the circuit of *Figure 1*.

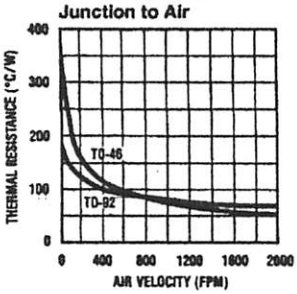
Note 10: Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. DC and AC electrical specifications do not apply when operating the device beyond its rated operating conditions. See Note 1.

Note 11: Human body model, 100 pF discharged through a 1.5 kΩ resistor.

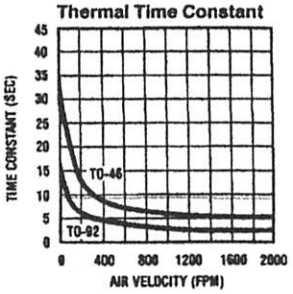
Note 12: See AN-450 "Surface Mounting Methods and Their Effect on Product Reliability" or the section titled "Surface Mount" found in a current National Semiconductor Linear Data Book for other methods of soldering surface mount devices.

Typical Performance Characteristics

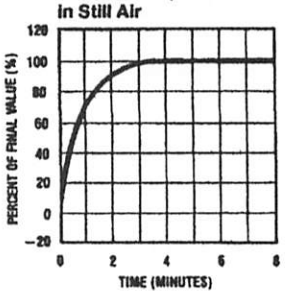
Thermal Resistance Junction to Air



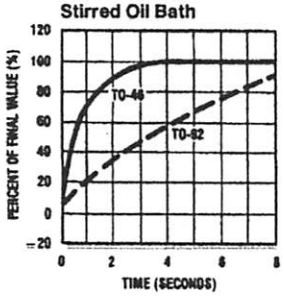
Thermal Time Constant



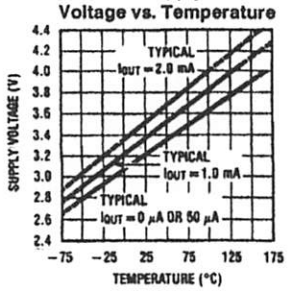
Thermal Response in Still Air



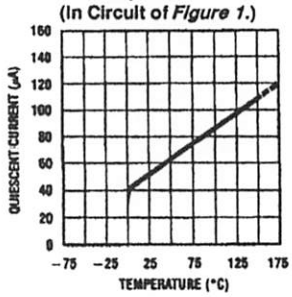
Thermal Response in Stirred Oil Bath



Minimum Supply Voltage vs. Temperature



Quiescent Current vs. Temperature (In Circuit of *Figure 1*.)



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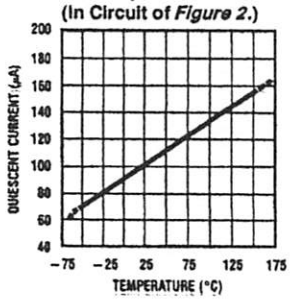
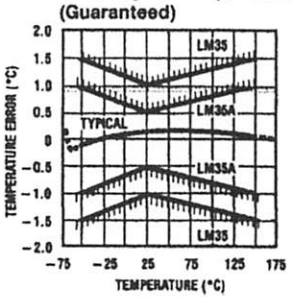
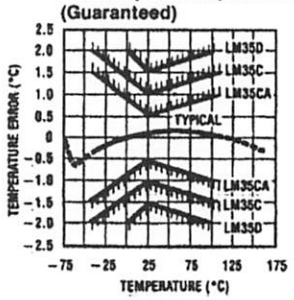
Quiescent Current vs. Temperature (In Circuit of *Figure 2*.)



Accuracy vs. Temperature (Guaranteed)



Accuracy vs. Temperature (Guaranteed)



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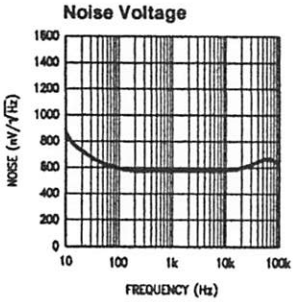
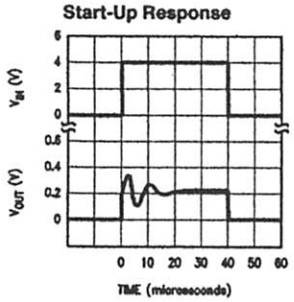
Noise Voltage



Start-Up Response



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Applications

The LM35 can be applied easily in the same way as other integrated-circuit temperature sensors. It can be glued or cemented to a surface and its temperature will be within about 0.01°C of the surface temperature.

This presumes that the ambient air temperature is almost the same as the surface temperature; if the air temperature were much higher or lower than the surface temperature, the actual temperature of the LM35 die would be at an intermediate temperature between the surface temperature and the air temperature. This is expecially true for the TO-92 plastic package, where the copper leads are the principal thermal path to carry heat into the device, so its temperature might be closer to the air temperature than to the surface temperature.

To minimize this problem, be sure that the wiring to the LM35, as it leaves the device, is held at the same temperature as the surface of interest. The easiest way to do this is to cover up these wires with a bead of epoxy which will insure that the leads and wires are all at the same temperature as the surface, and that the LM35 die's temperature will not be affected by the air temperature.

The TO-46 metal package can also be soldered to a metal surface or pipe without damage. Of course, in that case the V− terminal of the circuit will be grounded to that metal. Alternatively, the LM35 can be mounted inside a sealed-end metal tube, and can then be dipped into a bath or screwed into a threaded hole in a tank. As with any IC, the LM35 and accompanying wiring and circuits must be kept insulated and dry, to avoid leakage and corrosion. This is especially true if the circuit may operate at cold temperatures where condensation can occur. Printed-circuit coatings and varnishes such as Humiseal and epoxy paints or dips are often used to insure that moisture cannot corrode the LM35 or its connections.

These devices are sometimes soldered to a small lightweight heat fin, to decrease the thermal time constant and speed up the response in slowly-moving air. On the other hand, a small thermal mass may be added to the sensor, to give the steadiest reading despite small deviations in the air temperature.

Temperature Rise of LM35 Due To Self-heating (Thermal Resistance)

	TO-46, no heat sink	TO-46, small heat fin*	TO-92, no heat sink	TO-92, small heat fin**	SO-8 no heat sink	SO-8 small heat fin**	TO-202 no heat sink	TO-202 *** small heat fin
Still air	400°C/W	100°C/W	180°C/W	140°C/W	220°C/W	110°C/W	65°C/W	60°C/W
Moving air	100°C/W	40°C/W	90°C/W	70°C/W	105°C/W	90°C/W	25°C/W	40°C/W
Still oil	100°C/W	40°C/W	90°C/W	70°C/W				
Stirred oil	50°C/W	30°C/W	45°C/W	40°C/W				
(Clamped to metal, Infinite heat sink)	(24°C/W)				(55°C/W)		(23°C/W)	

* Wakefield type 201, or 1" disc of 0.020" sheet brass, soldered to case, or similar.

** TO-92 and SO-8 packages glued and leads soldered to 1" square of 1/16" printed circuit board with 2 oz. foil or similar.

Typical Applications (Continued)

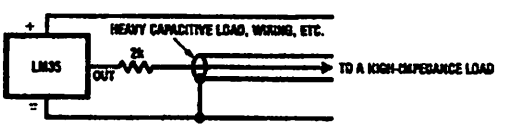

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FIGURE 3. LM35 with Decoupling from Capacitive Load

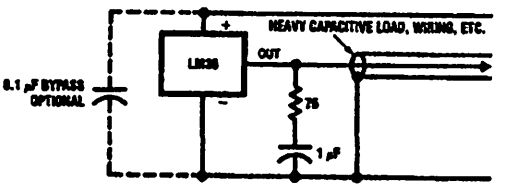

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FIGURE 4. LM35 with R-C Damper

CAPACITIVE LOADS

Like most micropower circuits, the LM35 has a limited ability to drive heavy capacitive loads. The LM35 by itself is able to drive 50 pf without special precautions. If heavier loads are anticipated, it is easy to isolate or decouple the load with a resistor; see *Figure 3*. Or you can improve the tolerance of capacitance with a series R-C damper from output to ground; see *Figure 4*.

When the LM35 is applied with a 200Ω load resistor as shown in *Figure 5, 6,* or *8*, it is relatively immune to wiring capacitance because the capacitance forms a bypass from ground to input, not on the output. However, as with any linear circuit connected to wires in a hostile environment, its performance can be affected adversely by intense electromagnetic sources such as relays, radio transmitters, motors with arcing brushes, SCR transients, etc, as its wiring can act as a receiving antenna and its internal junctions can act as rectifiers. For best results in such cases, a bypass capacitor from V_{IN} to ground and a series R-C damper such as 75Ω in series with 0.2 or 1 μF from output to ground are often useful. These are shown in *Figures 13, 14,* and *16*.

Typical Applications (Continued)

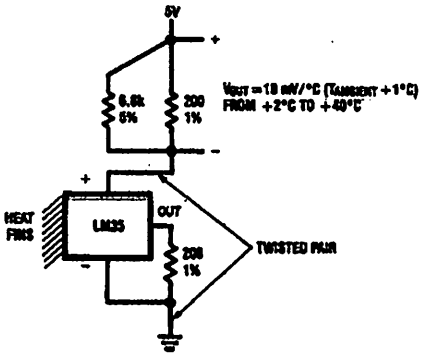

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FIGURE 5. Two-Wire Remote Temperature Sensor (Grounded Sensor)

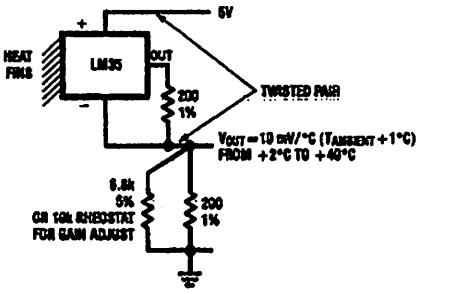

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FIGURE 6. Two-Wire Remote Temperature Sensor (Output Referred to Ground)

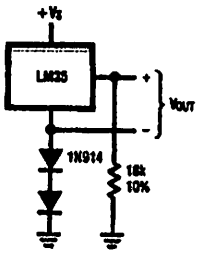

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FIGURE 7. Temperature Sensor, Single Supply, −55° to +150°C

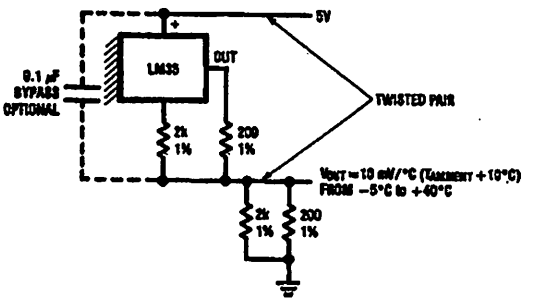

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FIGURE 8. Two-Wire Remote Temperature Sensor (Output Referred to Ground)

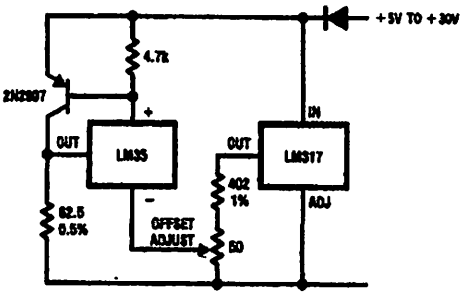

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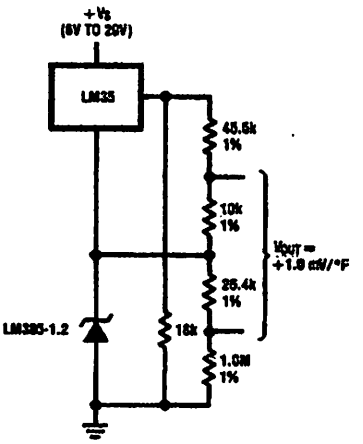
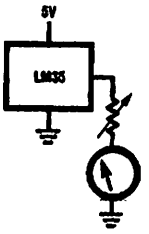
FIGURE 9. 4-To-20 mA Current Source (0°C to +100°C)



TL/H/5516–10

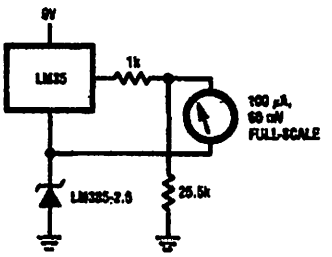
FIGURE 10. Fahrenheit Thermometer

Typical Applications (Continued)



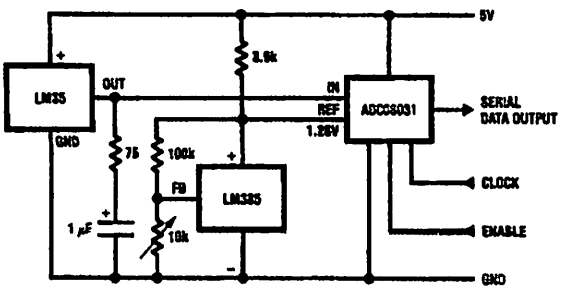
TL/H/5516–11

FIGURE 11. Centigrade Thermometer (Analog Meter)



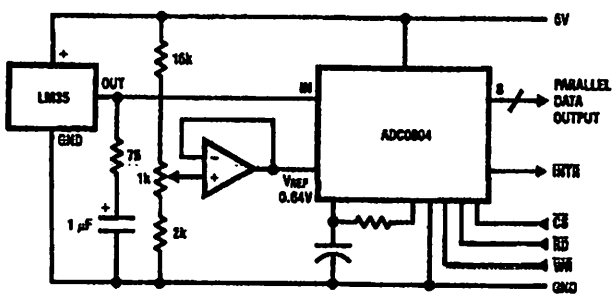
TL/H/5516–12

FIGURE 12. Expanded Scale Thermometer (50° to 80° Fahrenheit, for Example Shown)



TL/H/5516–13

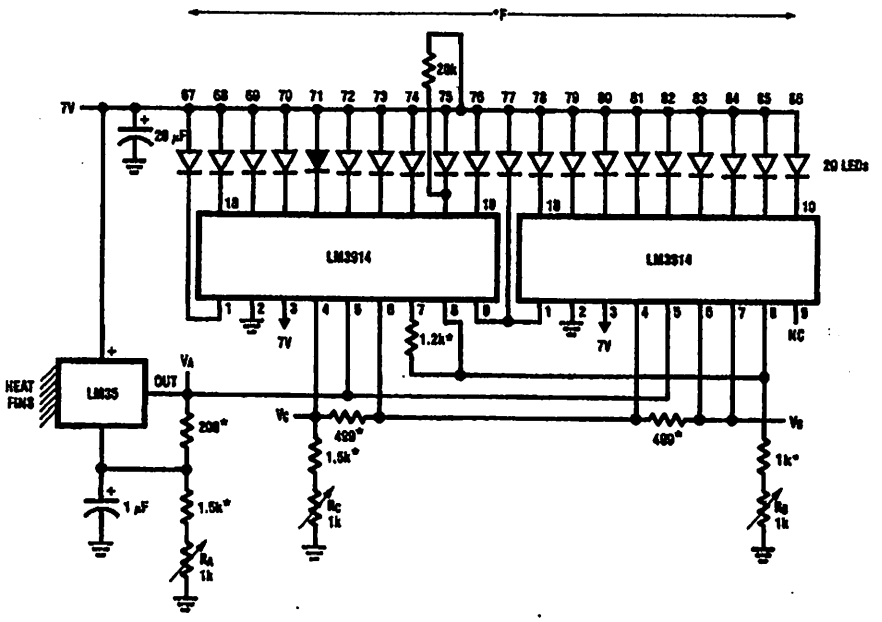
FIGURE 13. Temperature To Digital Converter (Serial Output) (+ 128°C Full Scale)



TL/H/5516–14

FIGURE 14. Temperature To Digital Converter (Parallel TRI-STATE® Outputs for Standard Data Bus to μP Interface) (128°C Full Scale)

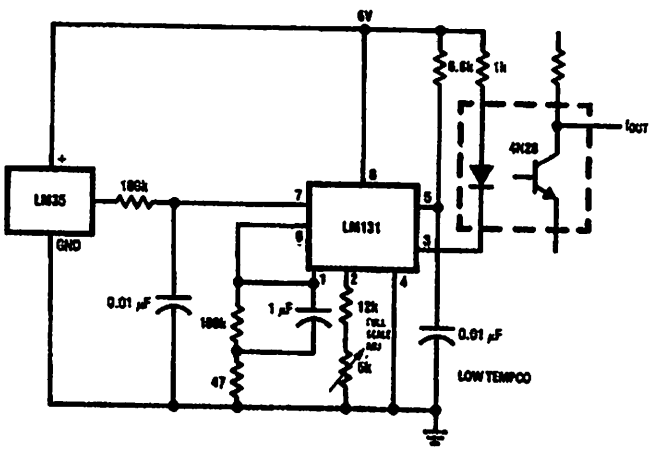
Typical Applications (Continued)



TL/H/5516–16

*=1% or 2% film resistor
-Trim R_B for V_B = 3.075V
-Trim R_C for V_C = 1.955V
-Trim R_A for V_A = 0.075V + 100mV/°C × $T_{ambient}$
-Example, V_A = 2.275V at 22°C

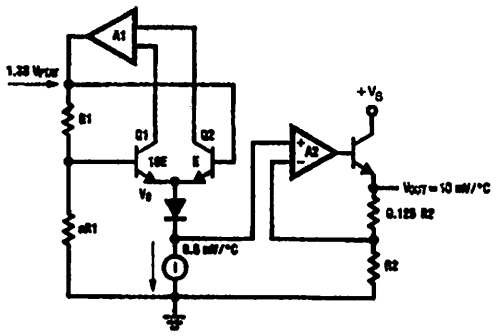
FIGURE 15. Bar-Graph Temperature Display (Dot Mode)



TL/H/5516–15

FIGURE 16. LM35 With Voltage-To-Frequency Converter And Isolated Output (2°C to +150°C; 20 Hz to 1500 Hz)

Block Diagram



TL/H/5516–23

National Semiconductor

December 1994

LM158/LM258/LM358/LM2904
Low Power Dual Operational Amplifiers

General Description

The LM158 series consists of two independent, high gain, internally frequency compensated operational amplifiers which were designed specifically to operate from a single power supply over a wide range of voltages. Operation from split power supplies is also possible and the low power supply current drain is independent of the magnitude of the power supply voltage.

Application areas include transducer amplifiers, dc gain blocks and all the conventional op amp circuits which now can be more easily implemented in single power supply systems. For example, the LM158 series can be directly operated off of the standard +5V power supply voltage which is used in digital systems and will easily provide the required interface electronics without requiring the additional ±15V power supplies.

Unique Characteristics

- In the linear mode the input common-mode voltage range includes ground and the output voltage can also swing to ground, even though operated from only a single power supply voltage.
- The unity gain cross frequency is temperature compensated.
- The input bias current is also temperature compensated.

Advantages

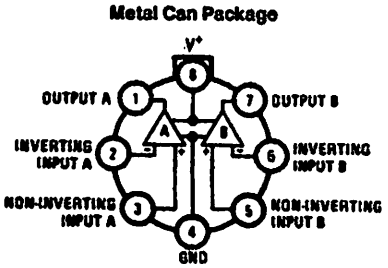
- Two internally compensated op amps in a single package
- Eliminates need for dual supplies
- Allows directly sensing near GND and V_{OUT} also goes to GND
- Compatible with all forms of logic
- Power drain suitable for battery operation
- Pin-out same as LM1558/LM1458 dual operational amplifier

Features

- Internally frequency compensated for unity gain
- Large dc voltage gain 100 dB
- Wide bandwidth (unity gain) 1 MHz (temperature compensated)
- Wide power supply range:
  - Single supply 3V to 32V
  - or dual supplies ±1.5V to ±16V
- Very low supply current drain (500 μA)—essentially independent of supply voltage
- Low input offset voltage 2 mV
- Input common-mode voltage range includes ground
- Differential input voltage range equal to the power supply voltage
- Large output voltage swing 0V to V^+ − 1.5V

Connection Diagrams (Top Views)

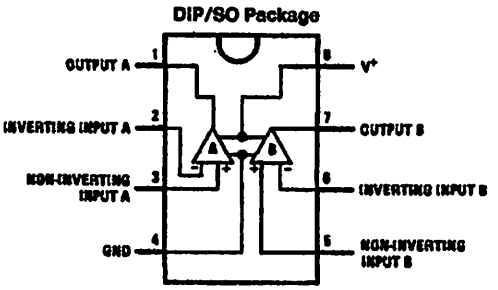
Metal Can Package



TL/H/7787–1

Order Number LM158AH, LM158AH/883*, LM158H, LM158H/883*, LM258H or LM358H
See NS Package Number H08C

DIP/SO Package



TL/H/7787–2

Order Number LM158J, LM158J/883*, LM158AJ or LM158AJ/883*
See NS Package Number J08A
Order Number LM358M, LM358AM or LM2904M
See NS Package Number M08A
Order Number LM358AN, LM358N or LM2904N
See NS Package Number N08E

*LM158 is available per SMD #5962-9771001
LM158A is available per SMD #5962-9771002

RRD-B30M115/Printed in U. S. A.

Absolute Maximum Ratings

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications. (Note 9)

	LM158/LM258/LM358 LM158A/LM258A/LM358A	LM2904
Supply Voltage, V^+	32V	26V
Differential Input Voltage	32V	26V
Input Voltage	−0.3V to +32V	−0.3V to +26V
Power Dissipation (Note 1)		
Molded DIP	830 mW	830 mW
Metal Can	550 mW	
Small Outline Package (M)	530 mW	530 mW
Output Short-Circuit to GND (One Amplifier) (Note 2) $V^+ \leq 15V$ and $T_A = 25°C$	Continuous	Continuous
Input Current ($V_{IN} < -0.3V$) (Note 3)	50 mA	50 mA

	LM158/LM258/LM358 LM158A/LM258A/LM358A	LM2904
Operating Temperature Range		
LM358	0°C to +70°C	−40°C to +85°C
LM258	−25°C to +85°C	
LM158	−55°C to +125°C	
Storage Temperature Range	−65°C to +150°C	−65°C to +150°C
Lead Temperature, DIP (Soldering, 10 seconds)	260°C	260°C
Lead Temperature, Metal Can (Soldering, 10 seconds)	300°C	300°C
Soldering Information		
Dual-In-Line Package		
Soldering (10 seconds)	260°C	260°C
Small Outline Package		
Vapor Phase (60 seconds)	215°C	215°C
Infrared (15 seconds)	220°C	220°C
See AN-450 "Surface Mounting Methods and Their Effect on Product Reliability" for other methods of soldering surface mount devices.		
ESD Tolerance (Note 10)	250V	250V

Electrical Characteristics $V^+ = +5.0V$, unless otherwise stated

Parameter	Conditions	LM158A			LM358A			LM158/LM258			LM358			LM2904			Units
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
Input Offset Voltage	(Note 5), $T_A = 25°C$		1	2		2	3		2	5		2	7		2	7	mV
Input Bias Current	$I_{IN(+)}$ or $I_{IN(-)}$, $T_A = 25°C$, $V_{CM} = 0V$, (Note 6)		20	50		45	100		45	150		45	250		45	250	nA
Input Offset Current	$I_{IN(+)} - I_{IN(-)}$, $V_{CM} = 0V$, $T_A = 25°C$		2	10		5	30		3	30		5	50		5	50	nA
Input Common-Mode Voltage Range	$V^+ = 30V$, (Note 7) (LM2904, $V^+ = 26V$), $T_A = 25°C$	0		$V^+ - 1.5$	0		$V^+ - 1.5$	0		$V^+ - 1.5$	0		$V^+ - 1.5$	0		$V^+ - 1.5$	V
Supply Current	Over Full Temperature Range $R_L = \infty$ on All Op Amps $V^+ = 30V$ (LM2904 $V^+ = 26V$) $V^+ = 5V$		1 0.5	2 1.2		1 0.5	2 1.2		1 0.5	2 1.2		1 0.5	2 1.2		1 0.5	2 1.2	mA mA

Electrical Characteristics (Continued) $V^+ = +5.0V$, Note 4, unless otherwise stated

Parameter		Conditions	LM158A			LM358A			LM158/LM258			LM358			LM2904			Units
			Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
Large Signal Voltage Gain		$V^+ = 15V$, $T_A = 25°C$, $R_L \geq 2 k\Omega$, (For $V_O = 1V$ to 11V)	50	100		25	100		50	100		25	100		25	100		V/mV
Common-Mode Rejection Ratio		$T_A = 25°C$, $V_{CM} = 0V$ to $V^+ - 1.5V$	70	85		65	85		70	85		65	85		50	70		dB
Power Supply Rejection Ratio		$V^+ = 5V$ to 30V (LM2904, $V^+ = 5V$ to 26V), $T_A = 25°C$	65	100		65	100		65	100		65	100		50	100		dB
Amplifier-to-Amplifier Coupling		f = 1 kHz to 20 kHz, $T_A = 25°C$ (Input Referred), (Note 8)		−120			−120			−120			−120			−120		dB
Output Current	Source	$V_{IN}^+ = 1V$, $V_{IN}^- = 0V$, $V^+ = 15V$, $V_O = 2V$, $T_A = 25°C$	20	40		20	40		20	40		20	40		20	40		mA
	Sink	$V_{IN}^- = 1V$, $V_{IN}^+ = 0V$ $V^+ = 15V$, $T_A = 25°C$, $V_O = 2V$	10	20		10	20		10	20		10	20		10	20		mA
		$V_{IN}^- = 1V$, $V_{IN}^+ = 0V$ $T_A = 25°C$, $V_O = 200$ mV, $V^+ = 15V$	12	50		12	50		12	50		12	50		12	50		µA
Short Circuit to Ground		$T_A = 25°C$, (Note 2), $V^+ = 15V$		40	60		40	60		40	60		40	60		40	60	mA
Input Offset Voltage		(Note 5)			4			5			7			9			10	mV
Input Offset Voltage Drift		$R_S = 0\Omega$		7	15		7	20		7			7			7		µV/°C
Input Offset Current		$I_{IN(+)} - I_{IN(-)}$			30			75			100			150		45	200	nA
Input Offset Current Drift		$R_S = 0\Omega$		10	200		10	300		10			10			10		pA/°C
Input Bias Current		$I_{IN(+)}$ or $I_{IN(-)}$		40	100		40	200		40	300		40	500		40	500	nA

Electrical Characteristics (Continued) $V^+ = +5.0V$, Note 4, unless otherwise stated

Parameter		Conditions		LM158A			LM358A			LM158/LM258			LM358			LM2904			Units
				Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
Input Common-Mode Voltage Range		$V^+ = 30V$, (Note 7) (LM2904, $V^+ = 26V$)		0		$V^+ - 2$	0		$V^+ - 2$	0		$V^+ - 2$	0		$V^+ - 2$	0		$V^+ - 2$	V
Large Signal Voltage Gain		$V^+ = +15V$ ($V_O = 1V$ to $11V$) $R_L \geq 2 k\Omega$		25			15			25			15			15			V/mV
Output Voltage Swing	V_{OH}	$V^+ = +30V$ (LM2904, $V^+ = 26V$)	$R_L = 2 k\Omega$	26			26			26			26			22			V
			$R_L = 10 k\Omega$	27	28		27	28		27	28		27	28		23	24		V
	V_{OL}	$V^+ = 5V$, $R_L = 10 k\Omega$			5	20		5	20		5	20		5	20		5	100	mV
Output Current	Source	$V_{IN}^+ = +1V$, $V_{IN}^- = 0V$, $V^+ = 15V$, $V_O = 2V$		10	20		10	20		10	20		10	20		10	20		mA
	Sink	$V_{IN}^- = +1V$, $V_{IN}^+ = 0V$, $V^+ = 15V$, $V_O = 2V$		10	15		5	8		5	8		5	8		5	8		mA

Note 1: For operating at high temperatures, the LM358/LM358A, LM2904 must be derated based on a +125°C maximum junction temperature and a thermal resistance of 120°C/W which applies for the device soldered in a printed circuit board, operating in a still air ambient. The LM258/LM258A and LM158/LM158A can be derated based on a +150°C maximum junction temperature. The dissipation is the total of both amplifiers—use external resistors, where possible, to allow the amplifier to saturate or to reduce the power which is dissipated in the integrated circuit.

Note 2: Short circuits from the output to V^+ can cause excessive heating and eventual destruction. When considering short circuits to ground, the maximum output current is approximately 40 mA independent of the magnitude of V^+. At values of supply voltage in excess of +15V, continuous short-circuits can exceed the power dissipation ratings and cause eventual destruction. Destructive dissipation can result from simultaneous shorts on all amplifiers.

Note 3: This input current will only exist when the voltage at any of the input leads is driven negative. It is due to the collector-base junction of the input PNP transistors becoming forward biased and thereby acting as input diode clamps. In addition to this diode action, there is also lateral NPN parasitic transistor action on the IC chip. This transistor action can cause the output voltages of the op amps to go to the V^+ voltage level (or to ground for a large overdrive) for the time duration that an input is driven negative. This is not destructive and normal output states will re-establish when the input voltage, which was negative, again returns to a value greater than −0.3V (at 25°C).

Note 4: These specifications are limited to $-55°C \leq T_A \leq +125°C$ for the LM158/LM158A. With the LM258/LM258A, all temperature specifications are limited to $-25°C \leq T_A \leq +85°C$, the LM358/LM358A temperature specifications are limited to $0°C \leq T_A \leq +70°C$, and the LM2904 specifications are limited to $-40°C \leq T_A \leq +85°C$.

Note 5: $V_O = 1.4V$, $R_S = 0\Omega$ with V^+ from 5V to 30V; and over the full input common-mode range (0V to $V^+ - 1.5V$) at 25°C. For LM2904, V^+ from 5V to 26V.

Note 6: The direction of the input current is out of the IC due to the PNP input stage. This current is essentially constant, independent of the state of the output so no loading change exists on the input lines.

Note 7: The input common-mode voltage of either input signal voltage should not be allowed to go negative by more than 0.3V (at 25°C). The upper end of the common-mode voltage range is $V^+ - 1.5V$ (at 25°C), but either or both inputs can go to +32V without damage (+26V for LM2904), independent of the magnitude of V^+.

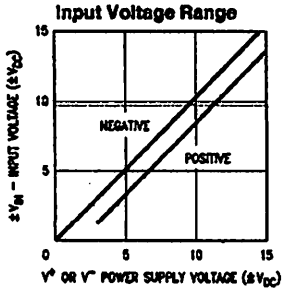
Note 8: Due to proximity of external components, insure that coupling is not originating via stray capacitance between these external parts. This typically can be detected as this type of capacitance increases at higher frequencies.

Note 9: Refer to RETS158AX for LM158A military specifications and to RETS158X for LM158 military specifications.

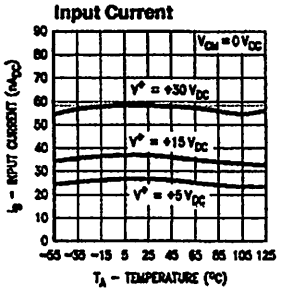
Note 10: Human body model, 1.5 kΩ in series with 100 pF.

Typical Performance Characteristics

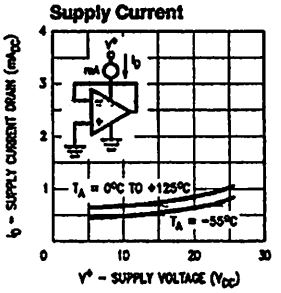
Input Voltage Range



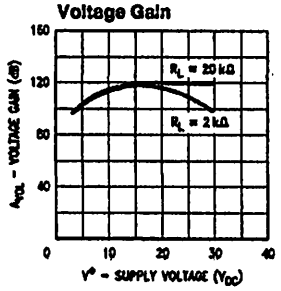
Input Current



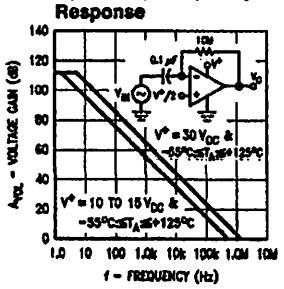
Supply Current



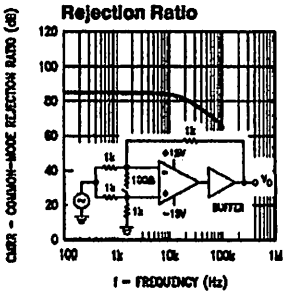
Voltage Gain



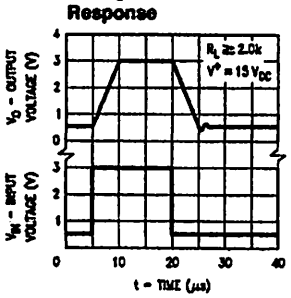
Open Loop Frequency Response



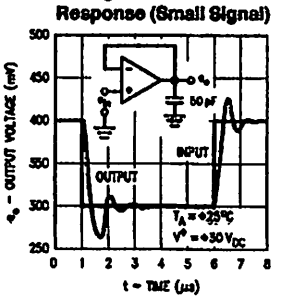
Common-Mode Rejection Ratio



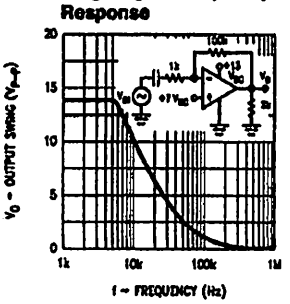
Voltage Follower Pulse Response



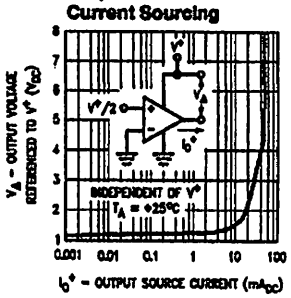
Voltage Follower Pulse Response (Small Signal)



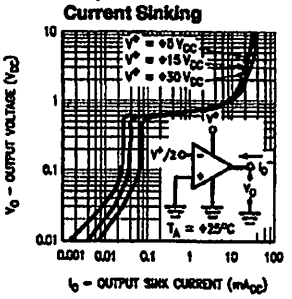
Large Signal Frequency Response



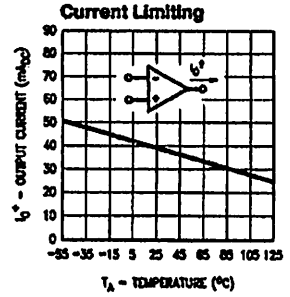
Output Characteristics Current Sourcing



Output Characteristics Current Sinking



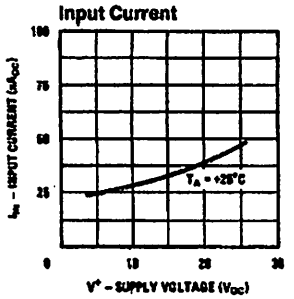
Current Limiting



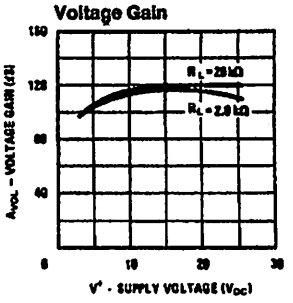
TL/H/7787–4

Typical Performance Characteristics (Continued) (LM2902 only)

Input Current



Voltage Gain



TL/H/7787–5

Application Hints

The LM158 series are op amps which operate with only a single power supply voltage, have true-differential inputs, and remain in the linear mode with an input common-mode voltage of 0 V_{DC}. These amplifiers operate over a wide range of power supply voltage with little change in performance characteristics. At 25°C amplifier operation is possible down to a minimum supply voltage of 2.3 V_{DC}.

Precautions should be taken to insure that the power supply for the integrated circuit never becomes reversed in polarity or that the unit is not inadvertently installed backwards in a test socket as an unlimited current surge through the resulting forward diode within the IC could cause fusing of the internal conductors and result in a destroyed unit.

Large differential input voltages can be easily accomodated and, as input differential voltage protection diodes are not needed, no large input currents result from large differential input voltages. The differential input voltage may be larger than V^+ without damaging the device. Protection should be provided to prevent the input voltages from going negative more than −0.3 V_{DC} (at 25°C). An input clamp diode with a resistor to the IC input terminal can be used.

To reduce the power supply current drain, the amplifiers have a class A output stage for small signal levels which converts to class B in a large signal mode. This allows the amplifiers to both source and sink large output currents. Therefore both NPN and PNP external current boost transistors can be used to extend the power capability of the basic amplifiers. The output voltage needs to raise approximately 1 diode drop above ground to bias the on-chip vertical PNP transistor for output current sinking applications.

For ac applications, where the load is capacitively coupled to the output of the amplifier, a resistor should be used, from the output of the amplifier to ground to increase the class A bias current and prevent crossover distortion. Where the load is directly coupled, as in dc applications, there is no crossover distortion.

Capacitive loads which are applied directly to the output of the amplifier reduce the loop stability margin. Values of 50 pF can be accomodated using the worst-case non-inverting unity gain connection. Large closed loop gains or resistive isolation should be used if larger load capacitance must be driven by the amplifier.

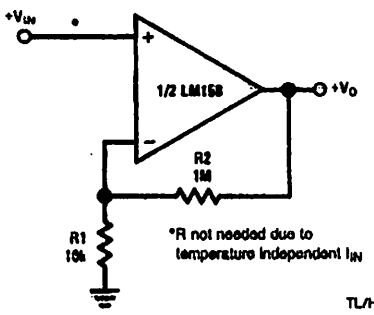
The bias network of the LM158 establishes a drain current which is independent of the magnitude of the power supply voltage over the range of 3 V_{DC} to 30 V_{DC}.

Output short circuits either to ground or to the positive power supply should be of short time duration. Units can be destroyed, not as a result of the short circuit current causing metal fusing, but rather due to the large increase in IC chip dissipation which will cause eventual failure due to excessive function temperatures. Putting direct short-circuits on more than one amplifier at a time will increase the total IC power dissipation to destructive levels, if not properly protected with external dissipation limiting resistors in series with the output leads of the amplifiers. The larger value of output source current which is available at 25°C provides a larger output current capability at elevated temperatures (see typical performance characteristics) than a standard IC op amp.

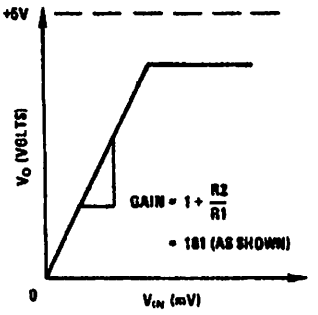
The circuits presented in the section on typical applications emphasize operation on only a single power supply voltage. If complementary power supplies are available, all of the standard op amp circuits can be used. In general, introducing a pseudo-ground (a bias voltage reference of $V^+/2$) will allow operation above and below this value in single power supply systems. Many application circuits are shown which take advantage of the wide input common-mode voltage range which includes ground. In most cases, input biasing is not required and input voltages which range to ground can easily be accommodated.

Typical Single-Supply Applications ($V^+ = 5.0\ V_{DC}$)

Non-Inverting DC Gain (0V Input = 0V Output)

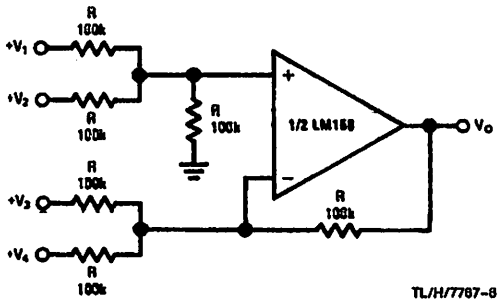


TL/H/7787–6



TL/H/7787–7

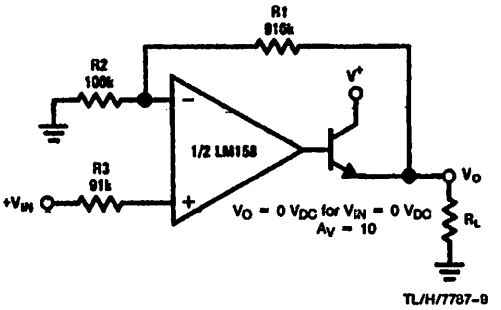
DC Summing Amplifier
(V_{IN}'S ≥ 0 V_{DC} and V_O ≥ 0 V_{DC})



TL/H/7787–8

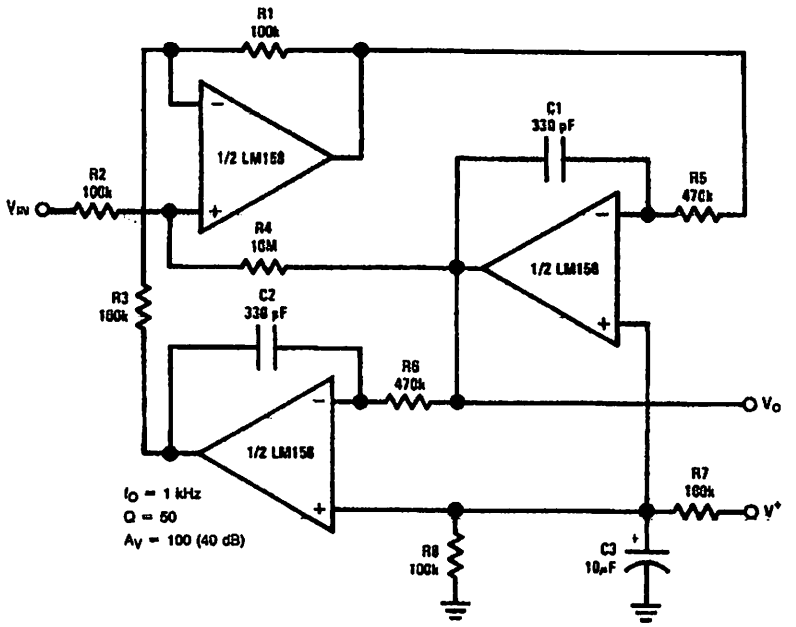
Where: $V_O = V_1 + V_2 + V_3 + V_4$
$(V_1 + V_2) \geq (V_3 + V_4)$ to keep $V_O > 0\ V_{DC}$

Power Amplifier



TL/H/7787–9

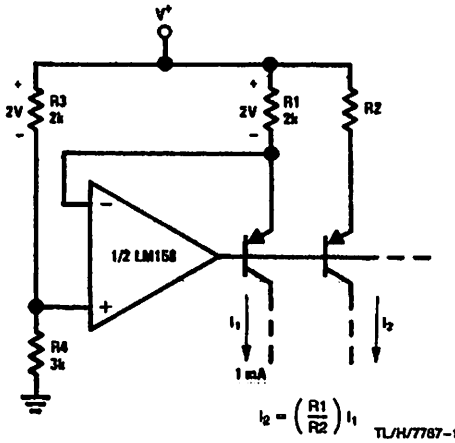
"BI-QUAD" RC Active Bandpass Filter



TL/H/7787–10

Typical Single-Supply Applications ($V^+ = 5.0\ V_{DC}$) (Continued)

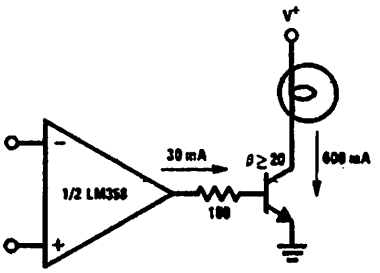
Fixed Current Sources



$$I_2 = \left(\frac{R1}{R2}\right) I_1$$

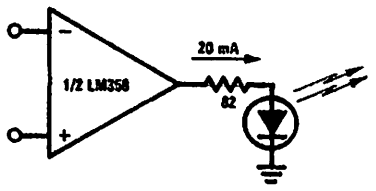
TL/H/7787–11

Lamp Driver



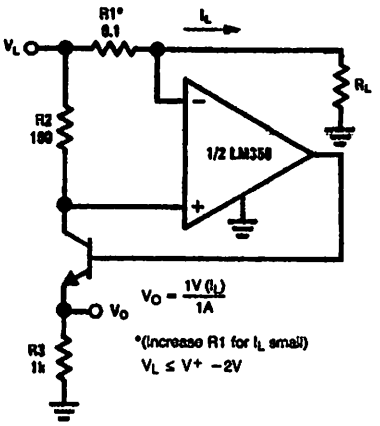
TL/H/7787–12

LED Driver



TL/H/7787–13

Current Monitor



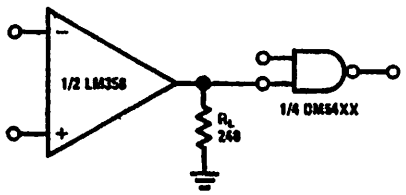
$$V_O = \frac{1V\ (I_L)}{1A}$$

*(Increase R1 for I_L small)

$V_L \leq V^+ - 2V$

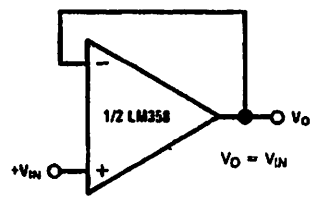
TL/H/7787–14

Driving TTL



TL/H/7787–15

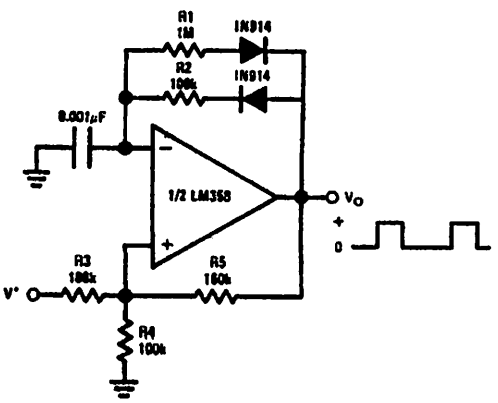
Voltage Follower



$V_O = V_{IN}$

TL/H/7787–17

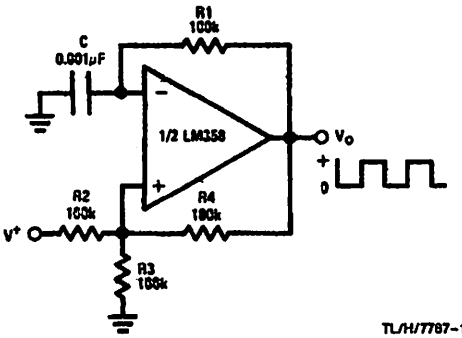
Pulse Generator



TL/H/7787–18

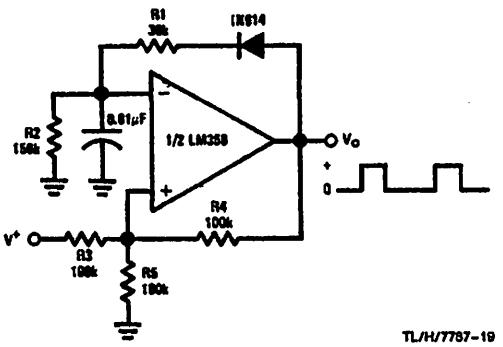
Typical Single-Supply Applications (V^+ = 5.0 V_{DC}) (Continued)

Squarewave Oscillator



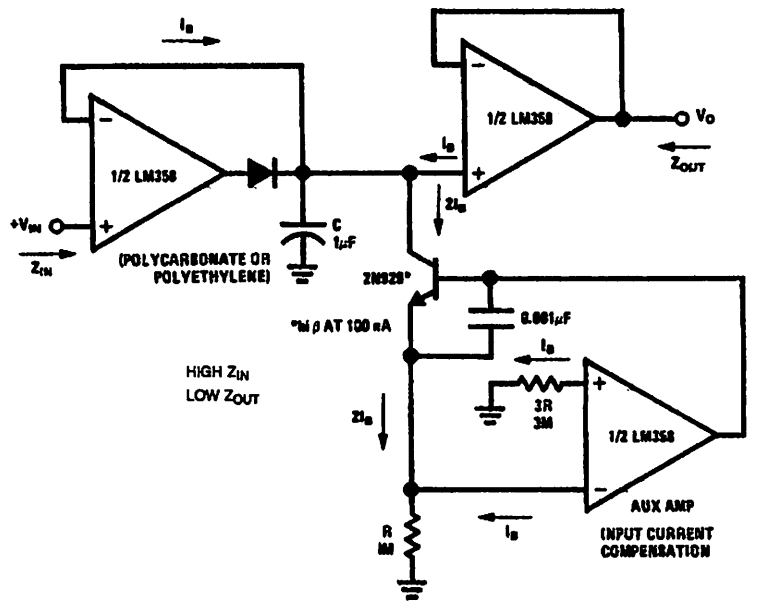
TL/H/7787–18

Pulse Generator



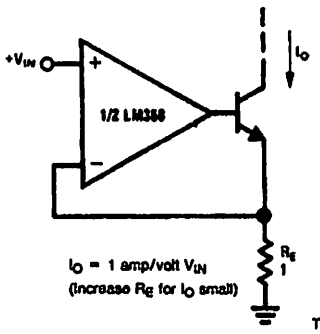
TL/H/7787–19

Low Drift Peak Detector



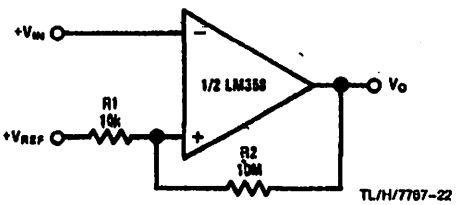
TL/H/7787–20

High Compliance Current Sink



TL/H/7787–21

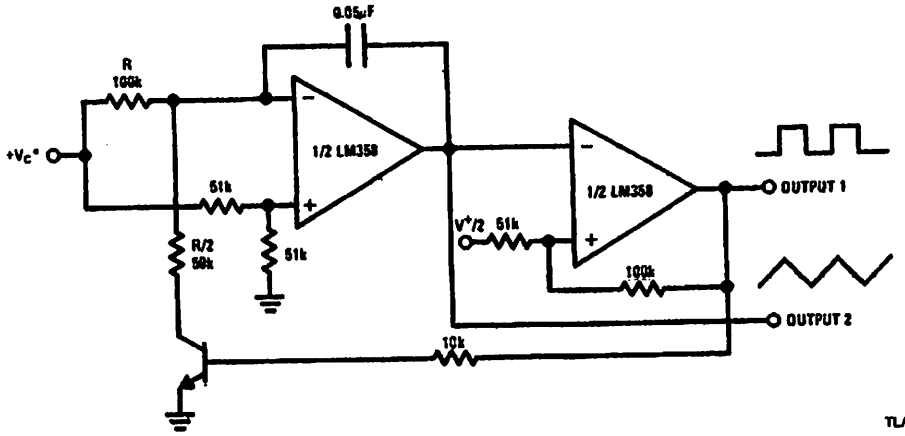
Comparator with Hysteresis



TL/H/7787–22

Typical Single-Supply Applications ($V^+ = 5.0\ V_{DC}$) (Continued)

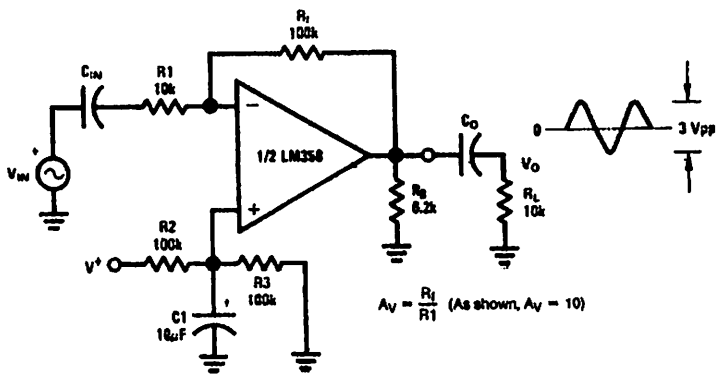
Voltage Controlled Oscillator (VCO)



TL/H/7767–23

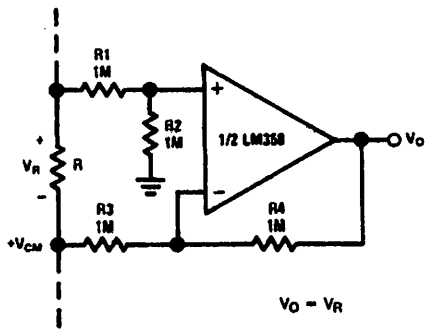
*WIDE CONTROL VOLTAGE RANGE: $0\ V_{DC} \leq V_C \leq 2\ (V^+ - 1.5V_{DC})$

AC Coupled Inverting Amplifier



TL/H/7767–24

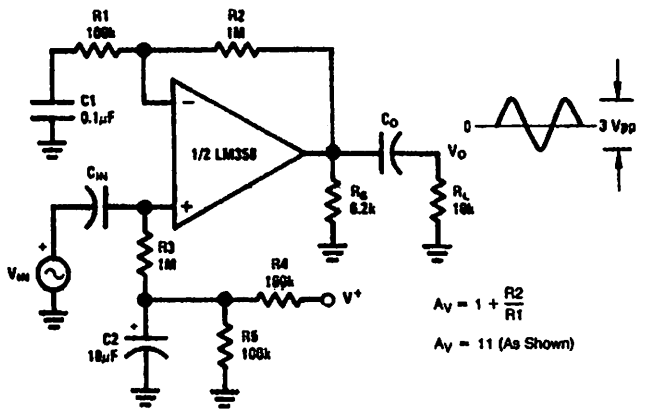
Ground Referencing a Differential Input Signal



TL/H/7767–25

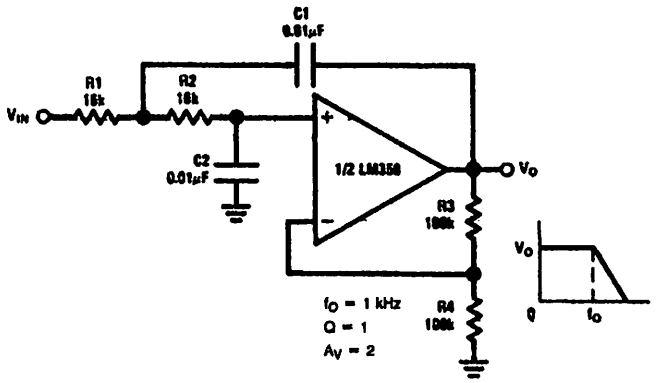
Typical Single-Supply Applications (V^+ = 5.0 V_{DC}) (Continued)

AC Coupled Non-Inverting Amplifier



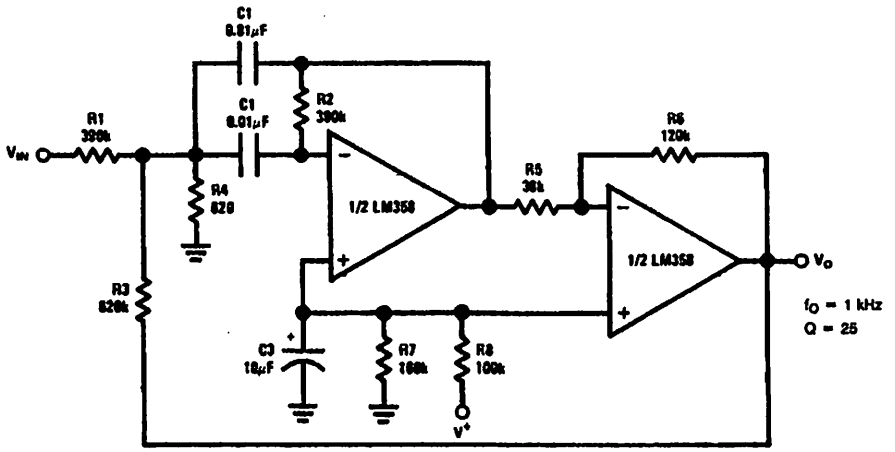
TL/H/7787–26

DC Coupled Low-Pass RC Active Filter



TL/H/7787–27

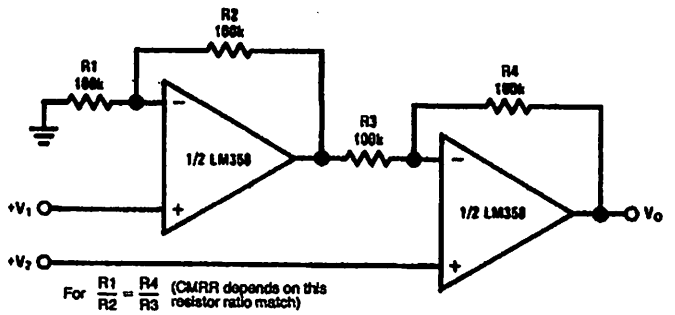
Bandpass Active Filter



TL/H/7787–28

Typical Single-Supply Applications ($V^+ = 5.0\ V_{DC}$) (Continued)

High Input Z, DC Differential Amplifier



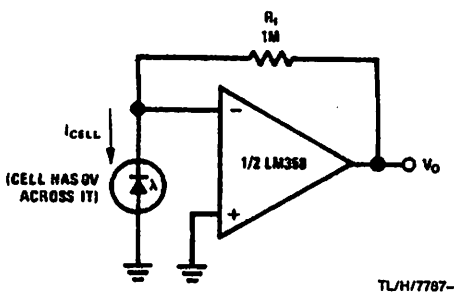
TL/H/7787–29

For $\frac{R1}{R2} = \frac{R4}{R3}$ (CMRR depends on this resistor ratio match)

$V_O = 1 + \frac{R4}{R3}(V_2 - V_1)$

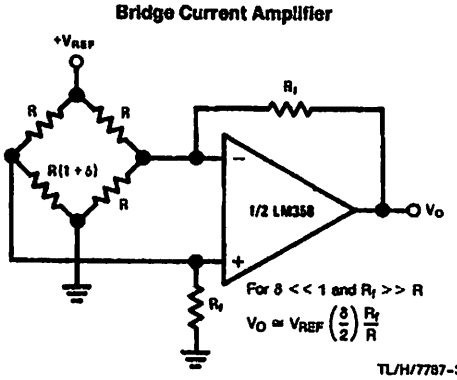
As Shown: $V_O = 2(V_2 - V_1)$

Photo Voltaic-Cell Amplifier



TL/H/7787–30

Bridge Current Amplifier

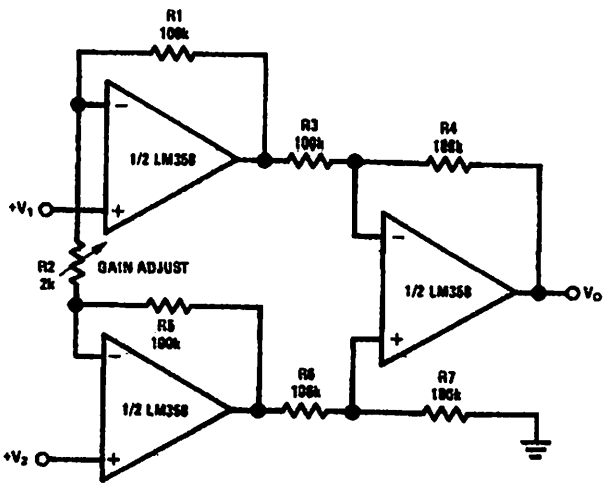


For $\delta << 1$ and $R_f >> R$

$V_O \cong V_{REF}\left(\frac{\delta}{2}\right)\frac{R_f}{R}$

TL/H/7787–33

High Input Z Adjustable-Gain DC Instrumentation Amplifier



TL/H/7787–31

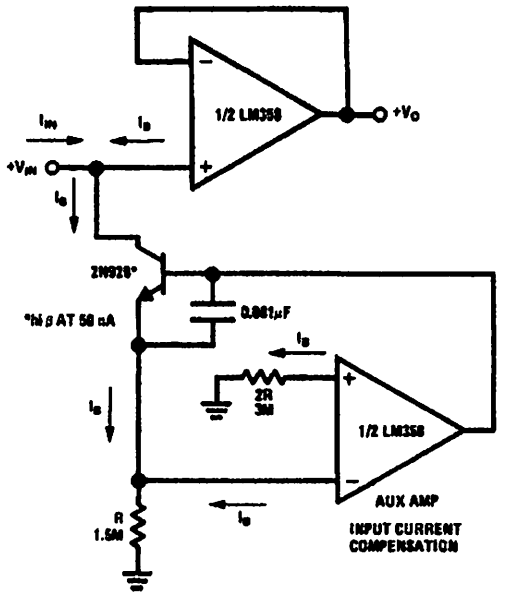
If R1 = R5 & R3 = R4 = R6 = R7 (CMRR depends on match)

$V_O = 1 + \frac{2R1}{R2}(V_2 - V_1)$

As shown $V_O = 101(V_2 - V_1)$

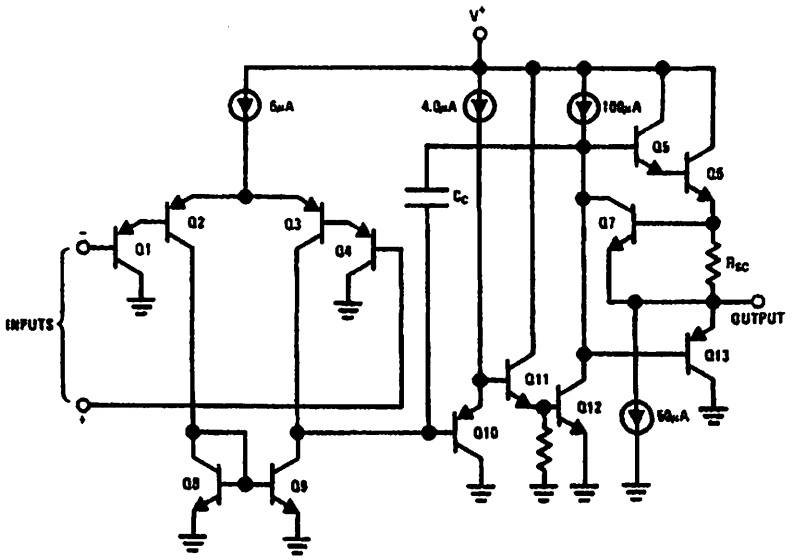
Typical Single-Supply Applications ($V^+ = 5.0\ V_{DC}$) (Continued)

Using Symmetrical Amplifiers to Reduce Input Current (General Concept)



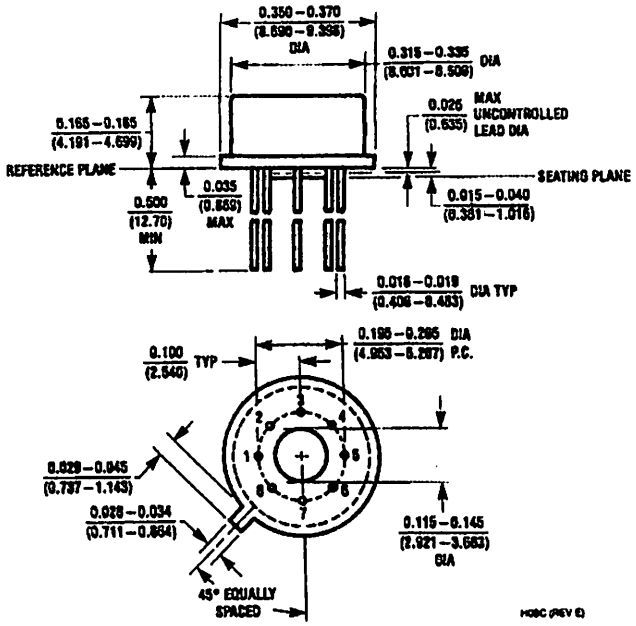
TL/H/7787–32

Schematic Diagram (Each Amplifier)



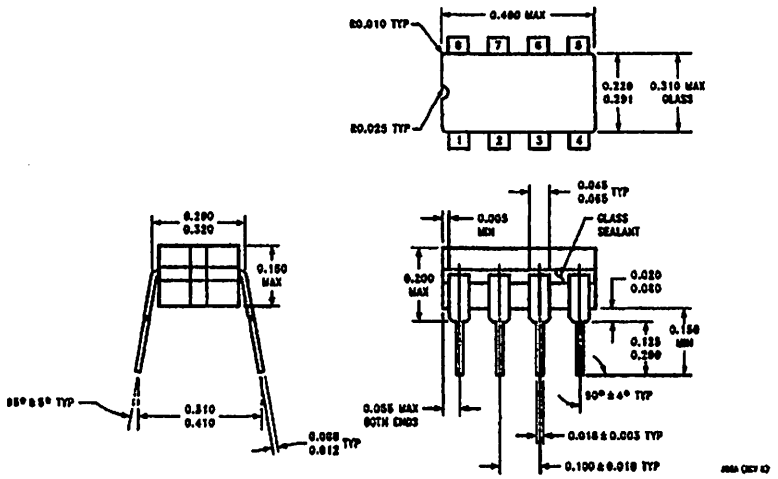
TL/H/7787–3

Physical Dimensions inches (millimeters)

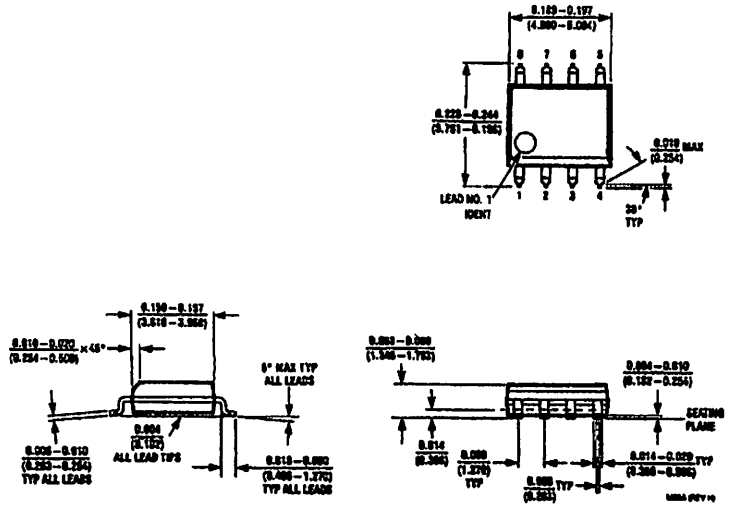


Metal Can Package (H)
Order Number LM158AH, LM158AH/883, LM158H, LM158H/883, LM258H or LM358H
NS Package Number H08C

Physical Dimensions inches (millimeters) (Continued)

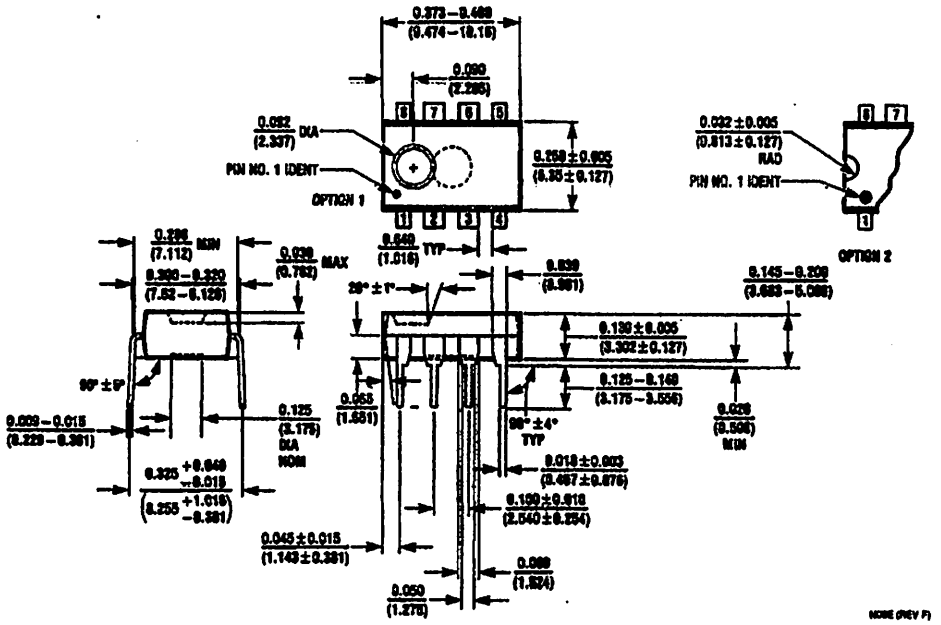


Cerdip Package (J)
Order Number LM158J, LM158J/883, LM158AJ or LM158AJ/883
NS Package Number J08A



S.O. Package (M)
Order Number LM358M, LM358AM or LM2904M
NS Package Number M08A

Physical Dimensions inches (millimeters) (Continued)



Molded Dip Package (N)
Order Number LM358AN, LM358N or LM2904N
NS Package Number N08E

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tures

h-performance, Low-power AVR® 8-bit Microcontroller
vanced RISC Architecture
131 Powerful Instructions – Most Single-clock Cycle Execution
32 x 8 General Purpose Working Registers
Fully Static Operation
Up to 16 MIPS Throughput at 16 MHz
On-chip 2-cycle Multiplier
nvolatile Program and Data Memories
16K Bytes of In-System Self-Programmable Flash
Endurance: 10,000 Write/Erase Cycles
Optional Boot Code Section with Independent Lock Bits
In-System Programming by On-chip Boot Program
True Read-While-Write Operation
512 Bytes EEPROM
Endurance: 100,000 Write/Erase Cycles
1K Byte Internal SRAM
Programming Lock for Software Security
AG (IEEE std. 1149.1 Compliant) Interface
Boundary-scan Capabilities According to the JTAG Standard
Extensive On-chip Debug Support
Programming of Flash, EEPROM, Fuses, and Lock Bits through the JTAG Interface
ripheral Features
Two 8-bit Timer/Counters with Separate Prescalers and Compare Modes
One 16-bit Timer/Counter with Separate Prescaler, Compare Mode, and Capture Mode
Real Time Counter with Separate Oscillator
Four PWM Channels
8-channel, 10-bit ADC
8 Single-ended Channels
7 Differential Channels in TQFP Package Only
2 Differential Channels with Programmable Gain at 1x, 10x, or 200x
Byte-oriented Two-wire Serial Interface
Programmable Serial USART
Master/Slave SPI Serial Interface
Programmable Watchdog Timer with Separate On-chip Oscillator
On-chip Analog Comparator
ecial Microcontroller Features
Power-on Reset and Programmable Brown-out Detection
Internal Calibrated RC Oscillator
External and Internal Interrupt Sources
Six Sleep Modes: Idle, ADC Noise Reduction, Power-save, Power-down, Standby and Extended Standby
and Packages
32 Programmable I/O Lines
40-pin PDIP, 44-lead TQFP, and 44-pad QFN/MLF
erating Voltages
2.7 - 5.5V for ATmega16L
4.5 - 5.5V for ATmega16
ed Grades
0 - 8 MHz for ATmega16L
0 - 16 MHz for ATmega16
wer Consumption @ 1 MHz, 3V, and 25°C for ATmega16L
Active: 1.1 mA
Idle Mode: 0.35 mA
Power-down Mode: < 1 µA

8-bit AVR® Microcontroller with 16K Bytes In-System Programmable Flash

ATmega16
ATmega16L

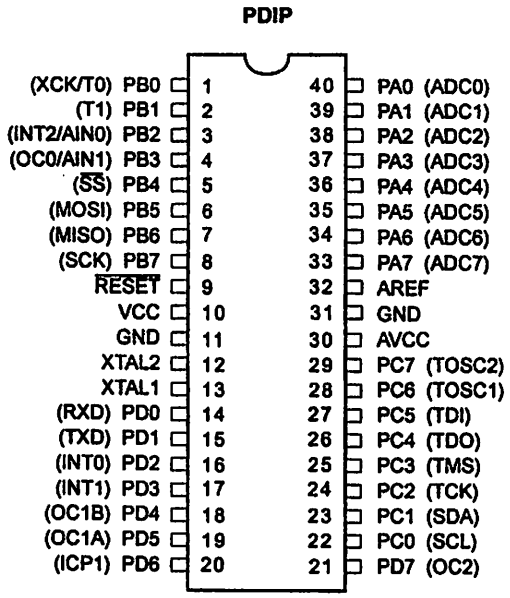
Summary

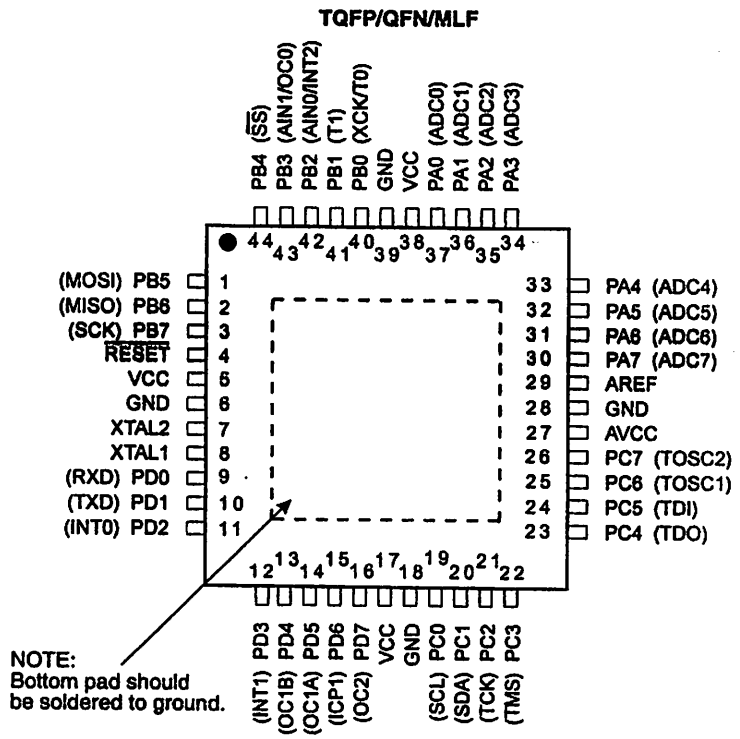
2466LS–AVR–06/05

Note: This is a summary document. A complete document is available on our Web site at www.atmel.com.

Configurations

Figure 1. Pinout ATmega16





Disclaimer

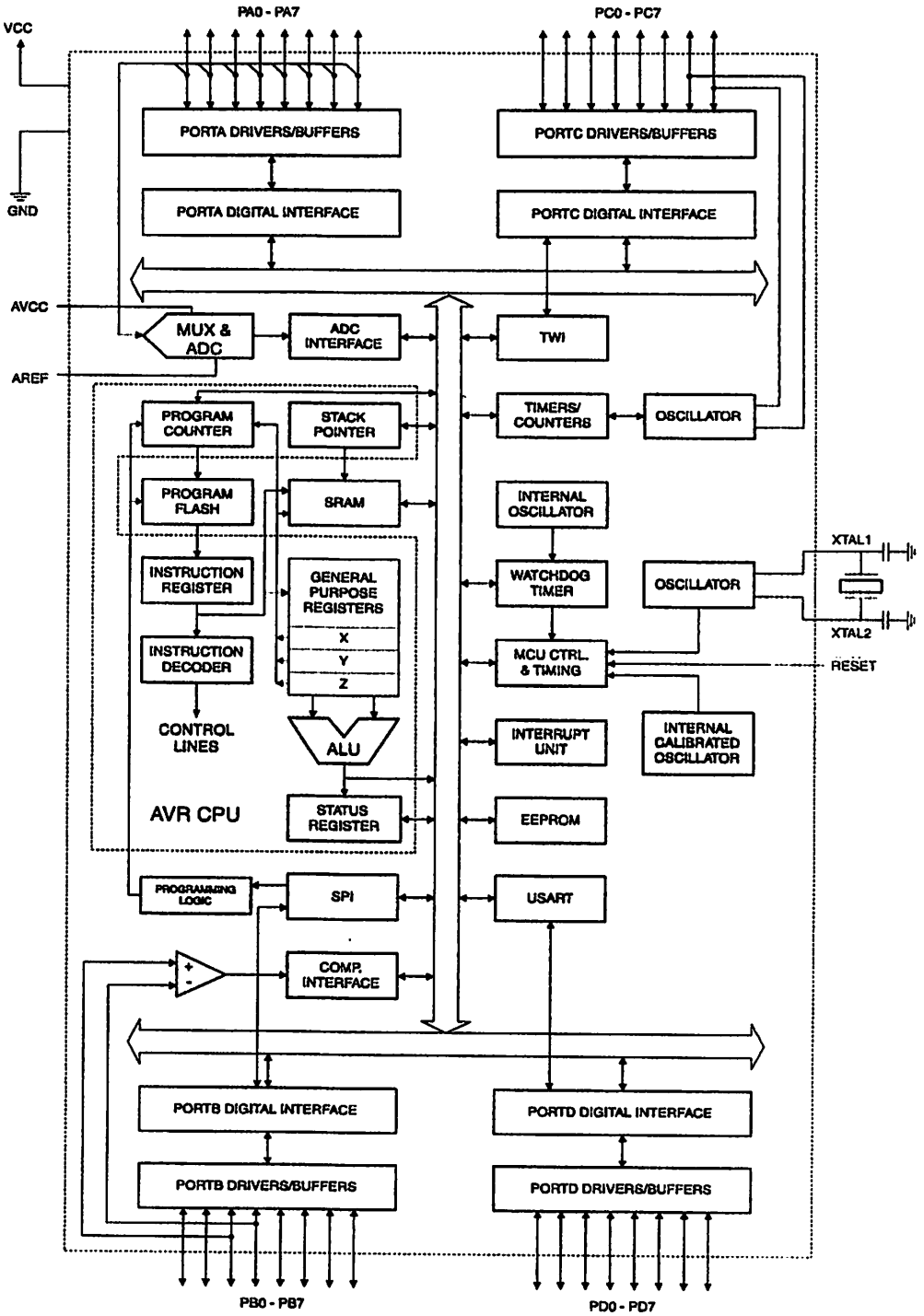
Typical values contained in this datasheet are based on simulations and characterization of other AVR microcontrollers manufactured on the same process technology. Min and Max values will be available after the device is characterized.

rview

The ATmega16 is a low-power CMOS 8-bit microcontroller based on the AVR enhanced RISC architecture. By executing powerful instructions in a single clock cycle, the ATmega16 achieves throughputs approaching 1 MIPS per MHz allowing the system designer to optimize power consumption versus processing speed.

k Diagram

Figure 2. Block Diagram



The AVR core combines a rich instruction set with 32 general purpose working registers. All the 32 registers are directly connected to the Arithmetic Logic Unit (ALU), allowing two independent registers to be accessed in one single instruction executed in one clock cycle. The resulting architecture is more code efficient while achieving throughputs up to ten times faster than conventional CISC microcontrollers.

The ATmega16 provides the following features: 16K bytes of In-System Programmable Flash Program memory with Read-While-Write capabilities, 512 bytes EEPROM, 1K byte SRAM, 32 general purpose I/O lines, 32 general purpose working registers, a JTAG interface for Boundary-scan, On-chip Debugging support and programming, three flexible Timer/Counters with compare modes, Internal and External Interrupts, a serial programmable USART, a byte oriented Two-wire Serial Interface, an 8-channel, 10-bit ADC with optional differential input stage with programmable gain (TQFP package only), a programmable Watchdog Timer with Internal Oscillator, an SPI serial port, and six software selectable power saving modes. The Idle mode stops the CPU while allowing the USART, Two-wire interface, A/D Converter, SRAM, Timer/Counters, SPI port, and interrupt system to continue functioning. The Power-down mode saves the register contents but freezes the Oscillator, disabling all other chip functions until the next External Interrupt or Hardware Reset. In Power-save mode, the Asynchronous Timer continues to run, allowing the user to maintain a timer base while the rest of the device is sleeping. The ADC Noise Reduction mode stops the CPU and all I/O modules except Asynchronous Timer and ADC, to minimize switching noise during ADC conversions. In Standby mode, the crystal/resonator Oscillator is running while the rest of the device is sleeping. This allows very fast start-up combined with low-power consumption. In Extended Standby mode, both the main Oscillator and the Asynchronous Timer continue to run.

The device is manufactured using Atmel's high density nonvolatile memory technology. The On-chip ISP Flash allows the program memory to be reprogrammed in-system through an SPI serial interface, by a conventional nonvolatile memory programmer, or by an On-chip Boot program running on the AVR core. The boot program can use any interface to download the application program in the Application Flash memory. Software in the Boot Flash section will continue to run while the Application Flash section is updated, providing true Read-While-Write operation. By combining an 8-bit RISC CPU with In-System Self-Programmable Flash on a monolithic chip, the Atmel ATmega16 is a powerful microcontroller that provides a highly-flexible and cost-effective solution to many embedded control applications.

The ATmega16 AVR is supported with a full suite of program and system development tools including: C compilers, macro assemblers, program debugger/simulators, in-circuit emulators, and evaluation kits.

)escriptions

Digital supply voltage.

Ground.

ı (PA7..PA0)

Port A serves as the analog inputs to the A/D Converter.

Port A also serves as an 8-bit bi-directional I/O port, if the A/D Converter is not used. Port pins can provide internal pull-up resistors (selected for each bit). The Port A output buffers have symmetrical drive characteristics with both high sink and source capability. When pins PA0 to PA7 are used as inputs and are externally pulled low, they will source current if the internal pull-up resistors are activated. The Port A pins are tri-stated when a reset condition becomes active, even if the clock is not running.

3 (PB7..PB0)

Port B is an 8-bit bi-directional I/O port with internal pull-up resistors (selected for each bit). The Port B output buffers have symmetrical drive characteristics with both high sink and source capability. As inputs, Port B pins that are externally pulled low will source current if the pull-up resistors are activated. The Port B pins are tri-stated when a reset condition becomes active, even if the clock is not running.

Port B also serves the functions of various special features of the ATmega16 as listed on page 56.

C (PC7..PC0)

Port C is an 8-bit bi-directional I/O port with internal pull-up resistors (selected for each bit). The Port C output buffers have symmetrical drive characteristics with both high sink and source capability. As inputs, Port C pins that are externally pulled low will source current if the pull-up resistors are activated. The Port C pins are tri-stated when a reset condition becomes active, even if the clock is not running. If the JTAG interface is enabled, the pull-up resistors on pins PC5(TDI), PC3(TMS) and PC2(TCK) will be activated even if a reset occurs.

Port C also serves the functions of the JTAG interface and other special features of the ATmega16 as listed on page 59.

D (PD7..PD0)

Port D is an 8-bit bi-directional I/O port with internal pull-up resistors (selected for each bit). The Port D output buffers have symmetrical drive characteristics with both high sink and source capability. As inputs, Port D pins that are externally pulled low will source current if the pull-up resistors are activated. The Port D pins are tri-stated when a reset condition becomes active, even if the clock is not running.

Port D also serves the functions of various special features of the ATmega16 as listed on page 61.

RESET

Reset Input. A low level on this pin for longer than the minimum pulse length will generate a reset, even if the clock is not running. The minimum pulse length is given in Table 15 on page 36. Shorter pulses are not guaranteed to generate a reset.

XTAL1

Input to the inverting Oscillator amplifier and input to the internal clock operating circuit.

XTAL2

Output from the inverting Oscillator amplifier.

AVCC

AVCC is the supply voltage pin for Port A and the A/D Converter. It should be externally connected to V_{CC}, even if the ADC is not used. If the ADC is used, it should be connected to V_{CC} through a low-pass filter.

AREF

AREF is the analog reference pin for the A/D Converter.

ources

A comprehensive set of development tools, application notes and datasheets are available for download on http://www.atmel.com/avr.

ister Summary

ress	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Page
($5F)	SREG	I	T	H	S	V	N	Z	C	7
($5E)	SPH	–	–	–	–	–	SP10	SP9	SP8	10
($5D)	SPL	SP7	SP6	SP5	SP4	SP3	SP2	SP1	SP0	10
($5C)	OCR0	Timer/Counter0 Output Compare Register								83
($5B)	GICR	INT1	INT0	INT2	–	–	–	IVSEL	IVCE	46, 67
($5A)	GIFR	INTF1	INTF0	INTF2	–	–	–	–	–	68
($59)	TIMSK	OCIE2	TOIE2	TICIE1	OCIE1A	OCIE1B	TOIE1	OCIE0	TOIE0	83, 114, 132
($58)	TIFR	OCF2	TOV2	ICF1	OCF1A	OCF1B	TOV1	OCF0	TOV0	84, 115, 132
($57)	SPMCR	SPMIE	RWWSB	–	RWWSRE	BLBSET	PGWRT	PGERS	SPMEN	250
($56)	TWCR	TWINT	TWEA	TWSTA	TWSTO	TWWC	TWEN	–	TWIE	178
($55)	MCUCR	SM2	SE	SM1	SM0	ISC11	ISC10	ISC01	ISC00	30, 66
($54)	MCUCSR	JTD	ISC2	–	JTRF	WDRF	BORF	EXTRF	PORF	39, 67, 229
($53)	TCCR0	FOC0	WGM00	COM01	COM00	WGM01	CS02	CS01	CS00	81
($52)	TCNT0	Timer/Counter0 (8 Bits)								83
($51)[1]	OSCCAL	Oscillator Calibration Register								28
	OCDR	On-Chip Debug Register								225
($50)	SFIOR	ADTS2	ADTS1	ADTS0	–	ACME	PUD	PSR2	PSR10	55,86,133,199,219
($4F)	TCCR1A	COM1A1	COM1A0	COM1B1	COM1B0	FOC1A	FOC1B	WGM11	WGM10	109
($4E)	TCCR1B	ICNC1	ICES1	–	WGM13	WGM12	CS12	CS11	CS10	112
($4D)	TCNT1H	Timer/Counter1 – Counter Register High Byte								113
($4C)	TCNT1L	Timer/Counter1 – Counter Register Low Byte								113
($4B)	OCR1AH	Timer/Counter1 – Output Compare Register A High Byte								113
($4A)	OCR1AL	Timer/Counter1 – Output Compare Register A Low Byte								113
($49)	OCR1BH	Timer/Counter1 – Output Compare Register B High Byte								113
($48)	OCR1BL	Timer/Counter1 – Output Compare Register B Low Byte								113
($47)	ICR1H	Timer/Counter1 – Input Capture Register High Byte								114
($46)	ICR1L	Timer/Counter1 – Input Capture Register Low Byte								114
($45)	TCCR2	FOC2	WGM20	COM21	COM20	WGM21	CS22	CS21	CS20	127
($44)	TCNT2	Timer/Counter2 (8 Bits)								129
($43)	OCR2	Timer/Counter2 Output Compare Register								129
($42)	ASSR	–	–	–	–	AS2	TCN2UB	OCR2UB	TCR2UB	130
($41)	WDTCR	–	–	–	WDTOE	WDE	WDP2	WDP1	WDP0	41
($40)[2]	UBRRH	URSEL	–	–	–	UBRR[11:8]				165
	UCSRC	URSEL	UMSEL	UPM1	UPM0	USBS	UCSZ1	UCSZ0	UCPOL	164
($3F)	EEARH	–	–	–	–	–	–	–	EEAR8	17
($3E)	EEARL	EEPROM Address Register Low Byte								17
($3D)	EEDR	EEPROM Data Register								17
($3C)	EECR	–	–	–	–	EERIE	EEMWE	EEWE	EERE	17
($3B)	PORTA	PORTA7	PORTA6	PORTA5	PORTA4	PORTA3	PORTA2	PORTA1	PORTA0	64
($3A)	DDRA	DDA7	DDA6	DDA5	DDA4	DDA3	DDA2	DDA1	DDA0	64
($39)	PINA	PINA7	PINA6	PINA5	PINA4	PINA3	PINA2	PINA1	PINA0	64
($38)	PORTB	PORTB7	PORTB6	PORTB5	PORTB4	PORTB3	PORTB2	PORTB1	PORTB0	64
($37)	DDRB	DDB7	DDB6	DDB5	DDB4	DDB3	DDB2	DDB1	DDB0	64
($36)	PINB	PINB7	PINB6	PINB5	PINB4	PINB3	PINB2	PINB1	PINB0	64
($35)	PORTC	PORTC7	PORTC6	PORTC5	PORTC4	PORTC3	PORTC2	PORTC1	PORTC0	65
($34)	DDRC	DDC7	DDC6	DDC5	DDC4	DDC3	DDC2	DDC1	DDC0	65
($33)	PINC	PINC7	PINC6	PINC5	PINC4	PINC3	PINC2	PINC1	PINC0	65
($32)	PORTD	PORTD7	PORTD6	PORTD5	PORTD4	PORTD3	PORTD2	PORTD1	PORTD0	65
($31)	DDRD	DDD7	DDD6	DDD5	DDD4	DDD3	DDD2	DDD1	DDD0	65
($30)	PIND	PIND7	PIND6	PIND5	PIND4	PIND3	PIND2	PIND1	PIND0	65
($2F)	SPDR	SPI Data Register								140
($2E)	SPSR	SPIF	WCOL	–	–	–	–	–	SPI2X	140
($2D)	SPCR	SPIE	SPE	DORD	MSTR	CPOL	CPHA	SPR1	SPR0	138
($2C)	UDR	USART I/O Data Register								161
($2B)	UCSRA	RXC	TXC	UDRE	FE	DOR	PE	U2X	MPCM	162
($2A)	UCSRB	RXCIE	TXCIE	UDRIE	RXEN	TXEN	UCSZ2	RXB8	TXB8	163
($29)	UBRRL	USART Baud Rate Register Low Byte								165
($28)	ACSR	ACD	ACBG	ACO	ACI	ACIE	ACIC	ACIS1	ACIS0	200
($27)	ADMUX	REFS1	REFS0	ADLAR	MUX4	MUX3	MUX2	MUX1	MUX0	215
($26)	ADCSRA	ADEN	ADSC	ADATE	ADIF	ADIE	ADPS2	ADPS1	ADPS0	217
($25)	ADCH	ADC Data Register High Byte								218
($24)	ADCL	ADC Data Register Low Byte								218
($23)	TWDR	Two-wire Serial Interface Data Register								180
($22)	TWAR	TWA6	TWA5	TWA4	TWA3	TWA2	TWA1	TWA0	TWGCE	180

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Page
($21)	TWSR	TWS7	TWS6	TWS5	TWS4	TWS3	–	TWPS1	TWPS0	179
($20)	TWBR	Two-wire Serial Interface Bit Rate Register								178

: 1. When the OCDEN Fuse is unprogrammed, the OSCCAL Register is always accessed on this address. Refer to the debugger specific documentation for details on how to use the OCDR Register.
2. Refer to the USART description for details on how to access UBRRH and UCSRC.
3. For compatibility with future devices, reserved bits should be written to zero if accessed. Reserved I/O memory addresses should never be written.
4. Some of the Status Flags are cleared by writing a logical one to them. Note that the CBI and SBI instructions will operate on all bits in the I/O Register, writing a one back into any flag read as set, thus clearing the flag. The CBI and SBI instructions work with registers $00 to $1F only.

ruction Set Summary

nonics	Operands	Description	Operation	Flags	#Clocks
METIC AND LOGIC INSTRUCTIONS					
	Rd, Rr	Add two Registers	Rd ← Rd + Rr	Z,C,N,V,H	1
	Rd, Rr	Add with Carry two Registers	Rd ← Rd + Rr + C	Z,C,N,V,H	1
	Rdl,K	Add Immediate to Word	Rdh:Rdl ← Rdh:Rdl + K	Z,C,N,V,S	2
	Rd, Rr	Subtract two Registers	Rd ← Rd - Rr	Z,C,N,V,H	1
	Rd, K	Subtract Constant from Register	Rd ← Rd - K	Z,C,N,V,H	1
	Rd, Rr	Subtract with Carry two Registers	Rd ← Rd - Rr - C	Z,C,N,V,H	1
	Rd, K	Subtract with Carry Constant from Reg.	Rd ← Rd - K - C	Z,C,N,V,H	1
	Rdl,K	Subtract Immediate from Word	Rdh:Rdl ← Rdh:Rdl - K	Z,C,N,V,S	2
	Rd, Rr	Logical AND Registers	Rd ← Rd • Rr	Z,N,V	1
	Rd, K	Logical AND Register and Constant	Rd ← Rd • K	Z,N,V	1
	Rd, Rr	Logical OR Registers	Rd ← Rd v Rr	Z,N,V	1
	Rd, K	Logical OR Register and Constant	Rd ← Rd v K	Z,N,V	1
	Rd, Rr	Exclusive OR Registers	Rd ← Rd ⊕ Rr	Z,N,V	1
	Rd	One's Complement	Rd ← $FF – Rd	Z,C,N,V	1
	Rd	Two's Complement	Rd ← $00 – Rd	Z,C,N,V,H	1
	Rd,K	Set Bit(s) in Register	Rd ← Rd v K	Z,N,V	1
	Rd,K	Clear Bit(s) in Register	Rd ← Rd • ($FF - K)	Z,N,V	1
	Rd	Increment	Rd ← Rd + 1	Z,N,V	1
	Rd	Decrement	Rd ← Rd – 1	Z,N,V	1
	Rd	Test for Zero or Minus	Rd ← Rd • Rd	Z,N,V	1
	Rd	Clear Register	Rd ← Rd ⊕ Rd	Z,N,V	1
	Rd	Set Register	Rd ← $FF	None	1
	Rd, Rr	Multiply Unsigned	R1:R0 ← Rd x Rr	Z,C	2
	Rd, Rr	Multiply Signed	R1:R0 ← Rd x Rr	Z,C	2
)	Rd, Rr	Multiply Signed with Unsigned	R1:R0 ← Rd x Rr	Z,C	2
	Rd, Rr	Fractional Multiply Unsigned	R1:R0 ← (Rd x Rr) << 1	Z,C	2
;	Rd, Rr	Fractional Multiply Signed	R1:R0 ← (Rd x Rr) << 1	Z,C	2
U	Rd, Rr	Fractional Multiply Signed with Unsigned	R1:R0 ← (Rd x Rr) << 1	Z,C	2
H INSTRUCTIONS					
	k	Relative Jump	PC ← PC + k + 1	None	2
		Indirect Jump to (Z)	PC ← Z	None	2
	k	Direct Jump	PC ← k	None	3
	k	Relative Subroutine Call	PC ← PC + k + 1	None	3
		Indirect Call to (Z)	PC ← Z	None	3
	k	Direct Subroutine Call	PC ← k	None	4
		Subroutine Return	PC ← STACK	None	4
		Interrupt Return	PC ← STACK	I	4
	Rd,Rr	Compare, Skip if Equal	if (Rd = Rr) PC ← PC + 2 or 3	None	1/2/3
	Rd,Rr	Compare	Rd – Rr	Z, N,V,C,H	1
	Rd,Rr	Compare with Carry	Rd – Rr – C	Z, N,V,C,H	1
	Rd,K	Compare Register with Immediate	Rd – K	Z, N,V,C,H	1
	Rr, b	Skip if Bit in Register Cleared	if (Rr(b)=0) PC ← PC + 2 or 3	None	1/2/3
	Rr, b	Skip if Bit in Register is Set	if (Rr(b)=1) PC ← PC + 2 or 3	None	1/2/3
	P, b	Skip if Bit in I/O Register Cleared	if (P(b)=0) PC ← PC + 2 or 3	None	1/2/3
	P, b	Skip if Bit in I/O Register is Set	if (P(b)=1) PC ← PC + 2 or 3	None	1/2/3
	s, k	Branch if Status Flag Set	if (SREG(s) = 1) then PC←PC+k + 1	None	1/2
	s, k	Branch if Status Flag Cleared	if (SREG(s) = 0) then PC←PC+k + 1	None	1/2
	k	Branch if Equal	if (Z = 1) then PC ← PC + k + 1	None	1/2
	k	Branch if Not Equal	if (Z = 0) then PC ← PC + k + 1	None	1/2
	k	Branch if Carry Set	if (C = 1) then PC ← PC + k + 1	None	1/2
	k	Branch if Carry Cleared	if (C = 0) then PC ← PC + k + 1	None	1/2
	k	Branch if Same or Higher	if (C = 0) then PC ← PC + k + 1	None	1/2
	k	Branch if Lower	if (C = 1) then PC ← PC + k + 1	None	1/2
	k	Branch if Minus	if (N = 1) then PC ← PC + k + 1	None	1/2
	k	Branch if Plus	if (N = 0) then PC ← PC + k + 1	None	1/2
	k	Branch if Greater or Equal, Signed	if (N ⊕ V= 0) then PC ← PC + k + 1	None	1/2
	k	Branch if Less Than Zero, Signed	if (N ⊕ V= 1) then PC ← PC + k + 1	None	1/2
	k	Branch if Half Carry Flag Set	if (H = 1) then PC ← PC + k + 1	None	1/2
	k	Branch if Half Carry Flag Cleared	if (H = 0) then PC ← PC + k + 1	None	1/2
	k	Branch if T Flag Set	if (T = 1) then PC ← PC + k + 1	None	1/2
	k	Branch if T Flag Cleared	if (T = 0) then PC ← PC + k + 1	None	1/2
	k	Branch if Overflow Flag is Set	if (V = 1) then PC ← PC + k + 1	None	1/2
	k	Branch if Overflow Flag is Cleared	if (V = 0) then PC ← PC + k + 1	None	1/2

ionics	Operands	Description	Operation	Flags	#Clocks
	k	Branch if Interrupt Enabled	if (I = 1) then PC ← PC + k + 1	None	1 / 2
	k	Branch if Interrupt Disabled	if (I = 0) then PC ← PC + k + 1	None	1 / 2
TRANSFER INSTRUCTIONS					
	Rd, Rr	Move Between Registers	Rd ← Rr	None	1
	Rd, Rr	Copy Register Word	Rd+1:Rd ← Rr+1:Rr	None	1
	Rd, K	Load Immediate	Rd ← K	None	1
	Rd, X	Load Indirect	Rd ← (X)	None	2
	Rd, X+	Load Indirect and Post-Inc.	Rd ← (X), X ← X + 1	None	2
	Rd, - X	Load Indirect and Pre-Dec.	X ← X - 1, Rd ← (X)	None	2
	Rd, Y	Load Indirect	Rd ← (Y)	None	2
	Rd, Y+	Load Indirect and Post-Inc.	Rd ← (Y), Y ← Y + 1	None	2
	Rd, - Y	Load Indirect and Pre-Dec.	Y ← Y - 1, Rd ← (Y)	None	2
	Rd,Y+q	Load Indirect with Displacement	Rd ← (Y + q)	None	2
	Rd, Z	Load Indirect	Rd ← (Z)	None	2
	Rd, Z+	Load Indirect and Post-Inc.	Rd ← (Z), Z ← Z+1	None	2
	Rd, -Z	Load Indirect and Pre-Dec.	Z ← Z - 1, Rd ← (Z)	None	2
	Rd, Z+q	Load Indirect with Displacement	Rd ← (Z + q)	None	2
	Rd, k	Load Direct from SRAM	Rd ← (k)	None	2
	X, Rr	Store Indirect	(X) ← Rr	None	2
	X+, Rr	Store Indirect and Post-Inc.	(X) ← Rr, X ← X + 1	None	2
	- X, Rr	Store Indirect and Pre-Dec.	X ← X - 1, (X) ← Rr	None	2
	Y, Rr	Store Indirect	(Y) ← Rr	None	2
	Y+, Rr	Store Indirect and Post-Inc.	(Y) ← Rr, Y ← Y + 1	None	2
	- Y, Rr	Store Indirect and Pre-Dec.	Y ← Y - 1, (Y) ← Rr	None	2
	Y+q,Rr	Store Indirect with Displacement	(Y + q) ← Rr	None	2
	Z, Rr	Store Indirect	(Z) ← Rr	None	2
	Z+, Rr	Store Indirect and Post-Inc.	(Z) ← Rr, Z ← Z + 1	None	2
	-Z, Rr	Store Indirect and Pre-Dec.	Z ← Z - 1, (Z) ← Rr	None	2
	Z+q,Rr	Store Indirect with Displacement	(Z + q) ← Rr	None	2
	k, Rr	Store Direct to SRAM	(k) ← Rr	None	2
		Load Program Memory	R0 ← (Z)	None	3
	Rd, Z	Load Program Memory	Rd ← (Z)	None	3
	Rd, Z+	Load Program Memory and Post-Inc	Rd ← (Z), Z ← Z+1	None	3
		Store Program Memory	(Z) ← R1:R0	None	-
	Rd, P	In Port	Rd ← P	None	1
	P, Rr	Out Port	P ← Rr	None	1
	Rr	Push Register on Stack	STACK ← Rr	None	2
	Rd	Pop Register from Stack	Rd ← STACK	None	2
D BIT-TEST INSTRUCTIONS					
	P,b	Set Bit in I/O Register	I/O(P,b) ← 1	None	2
	P,b	Clear Bit in I/O Register	I/O(P,b) ← 0	None	2
	Rd	Logical Shift Left	Rd(n+1) ← Rd(n), Rd(0) ← 0	Z,C,N,V	1
	Rd	Logical Shift Right	Rd(n) ← Rd(n+1), Rd(7) ← 0	Z,C,N,V	1
	Rd	Rotate Left Through Carry	Rd(0)←C,Rd(n+1)← Rd(n),C←Rd(7)	Z,C,N,V	1
	Rd	Rotate Right Through Carry	Rd(7)←C,Rd(n)← Rd(n+1),C←Rd(0)	Z,C,N,V	1
	Rd	Arithmetic Shift Right	Rd(n) ← Rd(n+1), n=0..6	Z,C,N,V	1
	Rd	Swap Nibbles	Rd(3..0)←Rd(7..4),Rd(7..4)←Rd(3..0)	None	1
	s	Flag Set	SREG(s) ← 1	SREG(s)	1
	s	Flag Clear	SREG(s) ← 0	SREG(s)	1
	Rr, b	Bit Store from Register to T	T ← Rr(b)	T	1
	Rd, b	Bit load from T to Register	Rd(b) ← T	None	1
		Set Carry	C ← 1	C	1
		Clear Carry	C ← 0	C	1
		Set Negative Flag	N ← 1	N	1
		Clear Negative Flag	N ← 0	N	1
		Set Zero Flag	Z ← 1	Z	1
		Clear Zero Flag	Z ← 0	Z	1
		Global Interrupt Enable	I ← 1	I	1
		Global Interrupt Disable	I ← 0	I	1
		Set Signed Test Flag	S ← 1	S	1
		Clear Signed Test Flag	S ← 0	S	1
		Set Twos Complement Overflow.	V ← 1	V	1
		Clear Twos Complement Overflow	V ← 0	V	1
		Set T in SREG	T ← 1	T	1
		Clear T in SREG	T ← 0	T	1
		Set Half Carry Flag in SREG	H ← 1	H	1

ıonics	Operands	Description	Operation	Flags	#Clocks
		Clear Half Carry Flag in SREG	H ← 0	H	1
CONTROL INSTRUCTIONS					
		No Operation		None	1
		Sleep	(see specific descr. for Sleep function)	None	1
		Watchdog Reset	(see specific descr. for WDR/timer)	None	1
K		Break	For On-Chip Debug Only	None	N/A

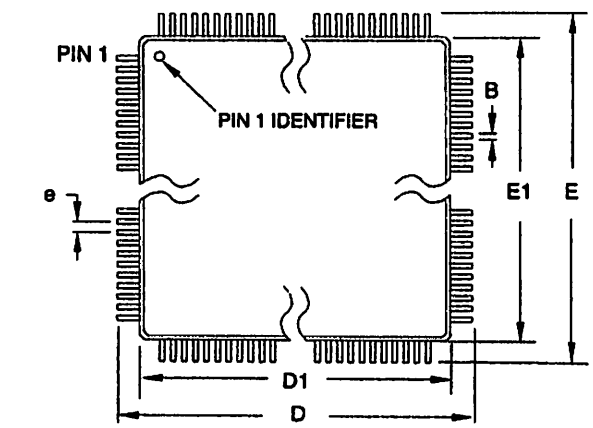
ering Information

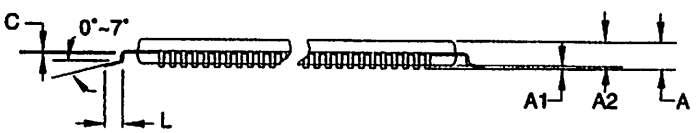
peed (MHz)	Power Supply	Ordering Code	Package	Operation Range
8	2.7 - 5.5V	ATmega16L-8AC ATmega16L-8PC ATmega16L-8MC	44A 40P6 44M1	Commercial (0°C to 70°C)
		ATmega16L-8AI ATmega16L-8AU[1] ATmega16L-8PI ATmega16L-8PU[1] ATmega16L-8MI ATmega16L-8MU[1]	44A 44A 40P6 40P6 44M1 44M1	Industrial (-40°C to 85°C)
16	4.5 - 5.5V	ATmega16-16AC ATmega16-16PC ATmega16-16MC	44A 40P6 44M1	Commercial (0°C to 70°C)
		ATmega16-16AI ATmega16-16AU[1] ATmega16-16PI ATmega16-16PU[1] ATmega16-16MI ATmega16-16MU[1]	44A 44A 40P6 40P6 44M1 44M1	Industrial (-40°C to 85°C)

1. Pb-free packaging alternative, complies to the European Directive for Restriction of Hazardous Substances (RoHS directive). Also Halide free and fully Green.

	Package Type
	44-lead, Thin (1.0 mm) Plastic Gull Wing Quad Flat Package (TQFP)
	40-pin, 0.600" Wide, Plastic Dual Inline Package (PDIP)
	44-pad, 7 x 7 x 1.0 mm body, lead pitch 0.50 mm, Quad Flat No-Lead/Micro Lead Frame Package (QFN/MLF)

kaging Information





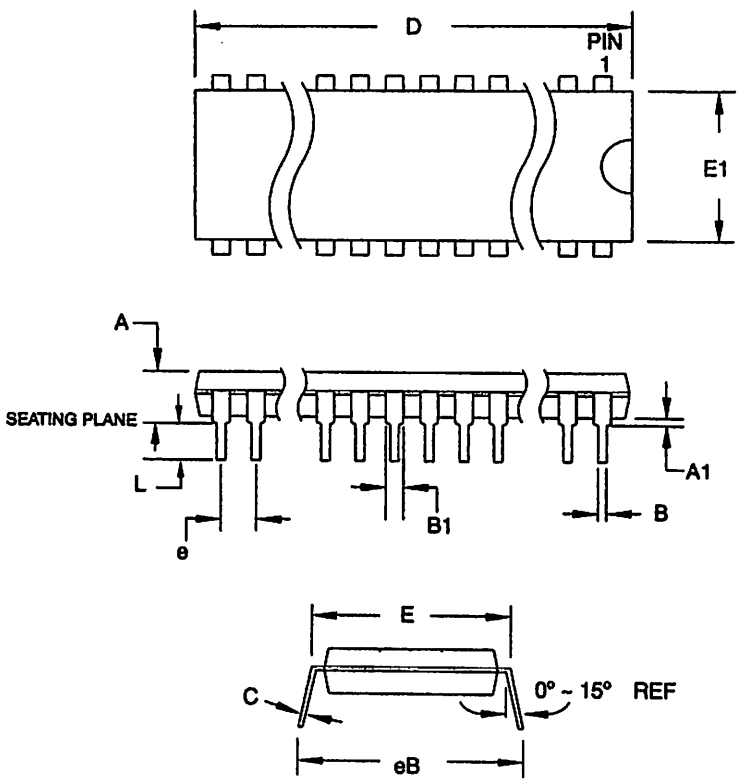
COMMON DIMENSIONS
(Unit of Measure = mm)

SYMBOL	MIN	NOM	MAX	NOTE
A	–	–	1.20	
A1	0.05	–	0.15	
A2	0.95	1.00	1.05	
D	11.75	12.00	12.25	
D1	9.90	10.00	10.10	Note 2
E	11.75	12.00	12.25	
E1	9.90	10.00	10.10	Note 2
B	0.30	–	0.45	
C	0.09	–	0.20	
L	0.45	–	0.75	
e	0.80 TYP			

Notes:
1. This package conforms to JEDEC reference MS-026, Variation ACB.
2. Dimensions D1 and E1 do not include mold protrusion. Allowable protrusion is 0.25 mm per side. Dimensions D1 and E1 are maximum plastic body size dimensions including mold mismatch.
3. Lead coplanarity is 0.10 mm maximum.

10/5/2001

	TITLE	DRAWING NO.	REV.
2325 Orchard Parkway San Jose, CA 95131	44A, 44-lead, 10 x 10 mm Body Size, 1.0 mm Body Thickness, 0.8 mm Lead Pitch, Thin Profile Plastic Quad Flat Package (TQFP)	44A	B



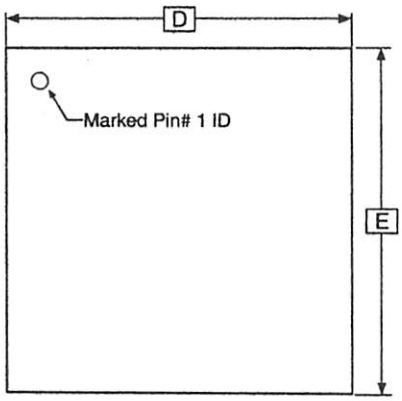
COMMON DIMENSIONS
(Unit of Measure = mm)

SYMBOL	MIN	NOM	MAX	NOTE
A	–	–	4.826	
A1	0.381	–	–	
D	52.070	–	52.578	Note 2
E	15.240	–	15.875	
E1	13.462	–	13.970	Note 2
B	0.356	–	0.559	
B1	1.041	–	1.651	
L	3.048	–	3.556	
C	0.203	–	0.381	
eB	15.494	–	17.526	
e	2.540 TYP			

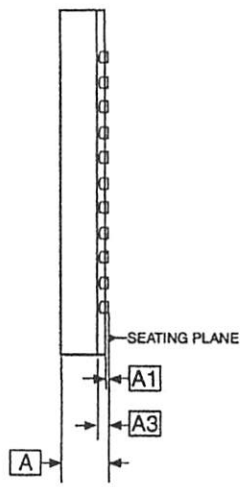
Notes:
1. This package conforms to JEDEC reference MS-011, Variation AC.
2. Dimensions D and E1 do not include mold Flash or Protrusion. Mold Flash or Protrusion shall not exceed 0.25 mm (0.010").

09/28/01

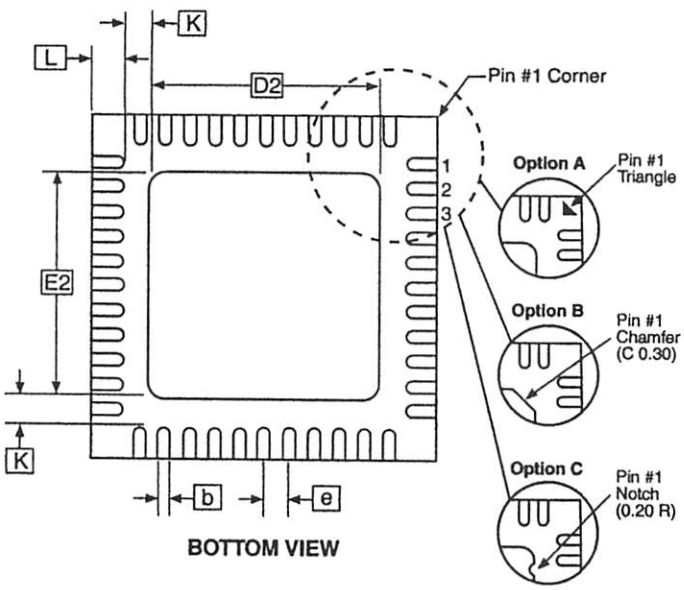
2325 Orchard Parkway San Jose, CA 95131	TITLE **40P6**, 40-lead (0.600"/15.24 mm Wide) Plastic Dual Inline Package (PDIP)	DRAWING NO. 40P6	REV. B



TOP VIEW



SIDE VIEW



BOTTOM VIEW

Note: JEDEC Standard MO-220, Fig. 1 (SAW Singulation) VKKD-3.

COMMON DIMENSIONS
(Unit of Measure = mm)

SYMBOL	MIN	NOM	MAX	NOTE
A	0.80	0.90	1.00	
A1	–	0.02	0.05	
A3		0.25 REF		
b	0.18	0.23	0.30	
D		7.00 BSC		
D2	5.00	5.20	5.40	
E		7.00 BSC		
E2	5.00	5.20	5.40	
e		0.50 BSC		
L	0.59	0.64	0.69	
K	0.20	0.26	0.41	

3/18/05

	TITLE	DRAWING NO.	REV.
2325 Orchard Parkway San Jose, CA 95131	**44M1**, 44-pad, 7 x 7 x 1.0 mm Body, Lead Pitch 0.50 mm, 5.20 mm Exposed Pad, Micro Lead Frame Package (MLF)	44M1	F

ta

The revision letter in this section refers to the revision of the ATmega16 device.

ega16(L) Rev. I

- IDCODE masks data from TDI input

1. **IDCODE masks data from TDI input**

   The JTAG instruction IDCODE is not working correctly. Data to succeeding devices are replaced by all-ones during Update-DR.

   Problem Fix / Workaround

   - If ATmega16 is the only device in the scan chain, the problem is not visible.
   - Select the Device ID Register of the ATmega16 by issuing the IDCODE instruction or by entering the Test-Logic-Reset state of the TAP controller to read out the contents of its Device ID Register and possibly data from succeeding devices of the scan chain. Issue the BYPASS instruction to the ATmega16 while reading the Device ID Registers of preceding devices of the boundary scan chain.
   - If the Device IDs of all devices in the boundary scan chain must be captured simultaneously, the ATmega16 must be the fist device in the chain.

ega16(L) Rev. H

- IDCODE masks data from TDI input

1. **IDCODE masks data from TDI input**

   The JTAG instruction IDCODE is not working correctly. Data to succeeding devices are replaced by all-ones during Update-DR.

   Problem Fix / Workaround

   - If ATmega16 is the only device in the scan chain, the problem is not visible.
   - Select the Device ID Register of the ATmega16 by issuing the IDCODE instruction or by entering the Test-Logic-Reset state of the TAP controller to read out the contents of its Device ID Register and possibly data from succeeding devices of the scan chain. Issue the BYPASS instruction to the ATmega16 while reading the Device ID Registers of preceding devices of the boundary scan chain.
   - If the Device IDs of all devices in the boundary scan chain must be captured simultaneously, the ATmega16 must be the fist device in the chain.

ega16(L) Rev. G

- IDCODE masks data from TDI input

1. **IDCODE masks data from TDI input**

   The JTAG instruction IDCODE is not working correctly. Data to succeeding devices are replaced by all-ones during Update-DR.

   Problem Fix / Workaround

   - If ATmega16 is the only device in the scan chain, the problem is not visible.
   - Select the Device ID Register of the ATmega16 by issuing the IDCODE instruction or by entering the Test-Logic-Reset state of the TAP controller to read out the contents of its Device ID Register and possibly data from succeeding devices of the scan chain. Issue the BYPASS instruction to the ATmega16 while reading the Device ID Registers of preceding devices of the boundary scan chain.
   - If the Device IDs of all devices in the boundary scan chain must be captured simultaneously, the ATmega16 must be the fist device in the chain.

sheet Revision ory

Please note that the referring page numbers in this section are referred to this document. The referring revision in this section are referring to the document revision.

2466L-06/05

1. Updated note in "Bit Rate Generator Unit" on page 176.
2. Updated values for V_{INT} in "ADC Characteristics" on page 297.
3. Updated "Serial Programming Instruction set" on page 276.
4. Updated USART init C-code example in "USART" on page 142.

2466K-04/05

1. Updated "Ordering Information" on page 11.
2. MLF-package alternative changed to "Quad Flat No-Lead/Micro Lead Frame Package QFN/MLF".
3. Updated "Electrical Characteristics" on page 291.

2466J-10/04

1. Updated "Ordering Information" on page 11.

2466I-10/04

1. Removed references to analog ground.
2. Updated Table 7 on page 26, Table 15 on page 36, Table 16 on page 40, Table 81 on page 208, Table 116 on page 276, and Table 119 on page 293.
3. Updated "Pinout ATmega16" on page 2.
4. Updated features in "Analog to Digital Converter" on page 202.
5. Updated "Version" on page 227.
6. Updated "Calibration Byte" on page 261.
7. Added "Page Size" on page 262.

2466H-12/03

1. Updated "Calibrated Internal RC Oscillator" on page 27.

2466G-10/03

1. Removed "Preliminary" from the datasheet.
2. Changed ICP to ICP1 in the datasheet.
3. Updated "JTAG Interface and On-chip Debug System" on page 34.
4. Updated assembly and C code examples in "Watchdog Timer Control Register – WDTCR" on page 41.
5. Updated Figure 46 on page 101.
6. Updated Table 15 on page 36, Table 82 on page 215 and Table 115 on page 276.

7. Updated "Test Access Port – TAP" on page 220 regarding JTAGEN.
8. Updated description for the JTD bit on page 229.
9. Added note 2 to Figure 126 on page 252.
10. Added a note regarding JTAGEN fuse to Table 105 on page 260.
11. Updated Absolute Maximum Ratings* and DC Characteristics in "Electrical Characteristics" on page 291.
12. Updated "ATmega16 Typical Characteristics" on page 299.
13. Fixed typo for 16 MHz QFN/MLF package in "Ordering Information" on page 11.
14. Added a proposal for solving problems regarding the JTAG instruction IDCODE in "Errata" on page 15.

2466F-02/03

1. Added note about masking out unused bits when reading the Program Counter in "Stack Pointer" on page 10.
2. Added Chip Erase as a first step in "Programming the Flash" on page 288 and "Programming the EEPROM" on page 289.
3. Added the section "Unconnected pins" on page 53.
4. Added tips on how to disable the OCD system in "On-chip Debug System" on page 34.
5. Removed reference to the "Multi-purpose Oscillator" application note and "32 kHz Crystal Oscillator" application note, which do not exist.
6. Added information about PWM symmetry for Timer0 and Timer2.
7. Added note in "Filling the Temporary Buffer (Page Loading)" on page 253 about writing to the EEPROM during an SPM Page Load.
8. Removed ADHSM completely.
9. Added Table 73, "TWI Bit Rate Prescaler," on page 180 to describe the TWPS bits in the "TWI Status Register – TWSR" on page 179.
10. Added section "Default Clock Source" on page 23.
11. Added note about frequency variation when using an external clock. Note added in "External Clock" on page 29. An extra row and a note added in Table 118 on page 293.
12. Various minor TWI corrections.
13. Added "Power Consumption" data in "Features" on page 1.

14. **Added section "EEPROM Write During Power-down Sleep Mode" on page 20.**

15. **Added note about Differential Mode with Auto Triggering in "Prescaling and Conversion Timing" on page 205.**

16. **Added updated "Packaging Information" on page 12.**

2466E-10/02

1. **Updated "DC Characteristics" on page 291.**

2466D-09/02

1. **Changed all Flash write/erase cycles from 1,000 to 10,000.**

2. **Updated the following tables: Table 4 on page 24, Table 15 on page 36, Table 42 on page 83, Table 45 on page 110, Table 46 on page 110, Table 59 on page 141, Table 67 on page 165, Table 90 on page 234, Table 102 on page 258, "DC Characteristics" on page 291, Table 119 on page 293, Table 121 on page 295, and Table 122 on page 297.**

3. **Updated "Errata" on page 15.**

2466C-03/02

1. **Updated typical EEPROM programming time, Table 1 on page 18.**

2. **Updated typical start-up time in the following tables:**
   Table 3 on page 23, Table 5 on page 25, Table 6 on page 26, Table 8 on page 27, Table 9 on page 27, and Table 10 on page 28.

3. **Updated Table 17 on page 41 with typical WDT Time-out.**

4. **Added Some Preliminary Test Limits and Characterization Data.**
   Removed some of the TBD's in the following tables and pages:
   Table 15 on page 36, Table 16 on page 40, Table 116 on page 272 (table removed in document review #D), "Electrical Characteristics" on page 291, Table 119 on page 293, Table 121 on page 295, and Table 122 on page 297.

5. **Updated TWI Chapter.**
   Added the note at the end of the "Bit Rate Generator Unit" on page 176.

6. **Corrected description of ADSC bit in "ADC Control and Status Register A – ADCSRA" on page 217.**

7. **Improved description on how to do a polarity check of the ADC doff results in "ADC Conversion Result" on page 214.**

8. **Added JTAG version number for rev. H in Table 87 on page 227.**

9. **Added not regarding OCDEN Fuse below Table 105 on page 260.**

10. **Updated Programming Figures:**
    Figure 127 on page 262 and Figure 136 on page 274 are updated to also reflect that AVCC must be connected during Programming mode. Figure 131 on page 270 added to illustrate how to program the fuses.

11. **Added a note regarding usage of the "PROG_PAGELOAD ($6)" on page 280 and "PROG_PAGEREAD ($7)" on page 280.**

12. **Removed alternative algortihm for leaving JTAG Programming mode.**
    See "Leaving Programming Mode" on page 288.

13. **Added Calibrated RC Oscillator characterization curves in section "ATmega16 Typical Characteristics" on page 299.**

14. **Corrected ordering code for QFN/MLF package (16MHz) in "Ordering Information" on page 11.**

15. **Corrected Table 90, "Scan Signals for the Oscillators(1)(2)(3)," on page 234.**

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2466LS–AVR–06/05

XR-2206

Monolithic
Function Generator

EXAR ...the analog plus company™

June 1997-3

ATURES

Low-Sine Wave Distortion, 0.5%, Typical
Excellent Temperature Stability, 20ppm/°C, Typ.
Wide Sweep Range, 2000:1, Typical
Low-Supply Sensitivity, 0.01%V, Typ.
Linear Amplitude Modulation
TTL Compatible FSK Controls
Wide Supply Range, 10V to 26V
Adjustable Duty Cycle, 1% TO 99%

APPLICATIONS

- Waveform Generation
- Sweep Generation
- AM/FM Generation
- V/F Conversion
- FSK Generation
- Phase-Locked Loops (VCO)

NERAL DESCRIPTION

e XR-2206 is a monolithic function generator grated circuit capable of producing high quality sine, uare, triangle, ramp, and pulse waveforms of h-stability and accuracy. The output waveforms can be h amplitude and frequency modulated by an external tage. Frequency of operation can be selected ernally over a range of 0.01Hz to more than 1MHz.

The circuit is ideally suited for communications, instrumentation, and function generator applications requiring sinusoidal tone, AM, FM, or FSK generation. It has a typical drift specification of 20ppm/°C. The oscillator frequency can be linearly swept over a 2000:1 frequency range with an external control voltage, while maintaining low distortion.

DERING INFORMATION

Part No.	Package	Operating Temperature Range
XR-2206M	16 Lead 300 Mil CDIP	-55°C to +125°C
XR-2206P	16 Lead 300 Mil PDIP	–40°C to +85°C
XR-2206CP	16 Lead 300 Mil PDIP	0°C to +70°C
XR-2206D	16 Lead 300 Mil JEDEC SOIC	0°C to +70°C

TQM™

EXAR Corporation, 48720 Kato Road, Fremont, CA 94538 ◆ (510) 668-7000 ◆ (510) 668-7017

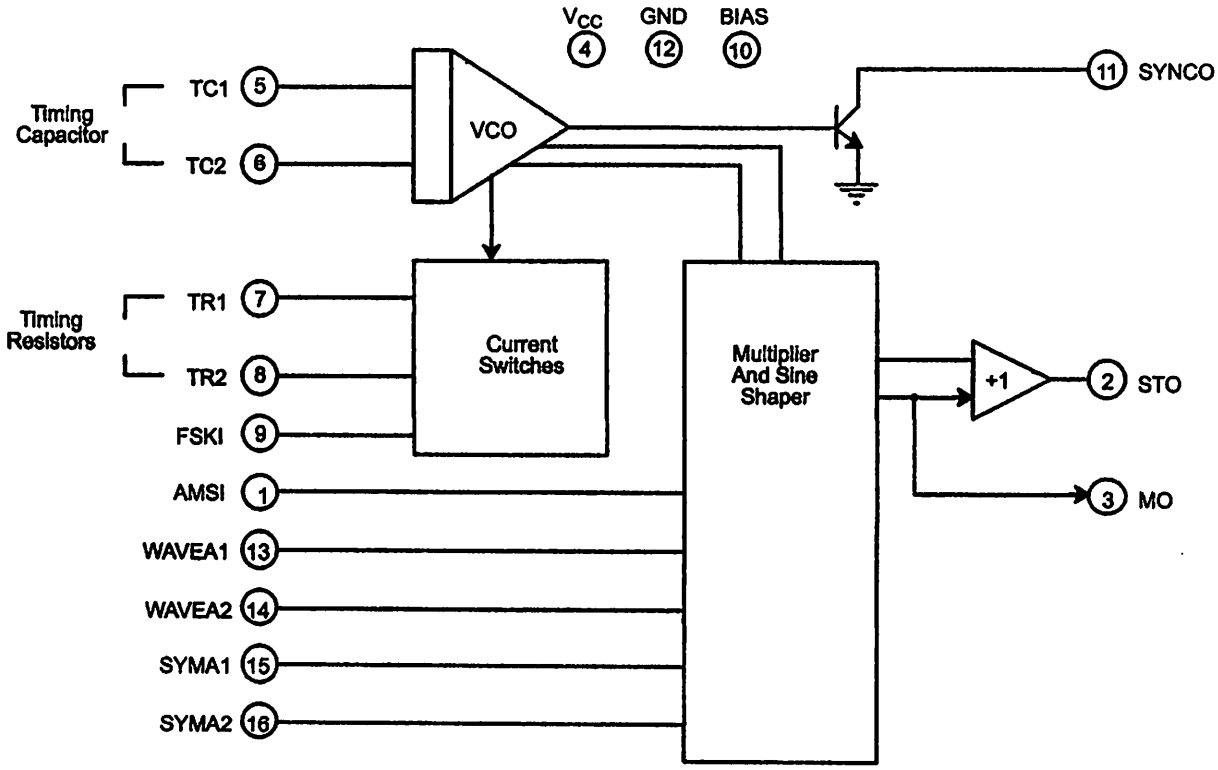
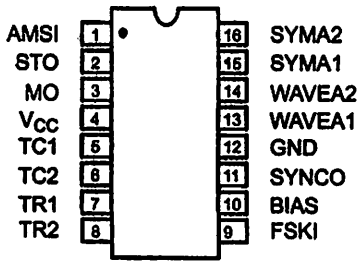
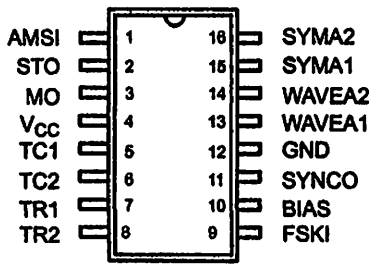


Figure 1. XR-2206 Block Diagram



16 Lead PDIP, CDIP (0.300")



16 Lead SOIC (Jedec, 0.300")

N DESCRIPTION

in #	Symbol	Type	Description
1	AMSI	I	**Amplitude Modulating Signal Input.**
2	STO	O	**Sine or Triangle Wave Output.**
3	MO	O	**Multiplier Output.**
4	V_{CC}		**Positive Power Supply.**
5	TC1	I	**Timing Capacitor Input.**
6	TC2	I	**Timing Capacitor Input.**
7	TR1	O	**Timing Resistor 1 Output.**
8	TR2	O	**Timing Resistor 2 Output.**
9	FSKI	I	**Frequency Shift Keying Input.**
10	BIAS	O	**Internal Voltage Reference.**
11	SYNCO	O	**Sync Output.** This output is a open collector and needs a pull up resistor to V_{CC}.
12	GND		**Ground pin.**
13	WAVEA1	I	**Wave Form Adjust Input 1.**
14	WAVEA2	I	**Wave Form Adjust Input 2.**
15	SYMA1	I	**Wave Symetry Adjust 1.**
16	SYMA2	I	**Wave Symetry Adjust 2.**

ELECTRICAL CHARACTERISTICS

st Conditions: Test Circuit of *Figure 2* Vcc = 12V, T_A = 25°C, C = 0.01µF, R_1 = 100kΩ, R_2 = 10kΩ, R_3 = 25kΩ
ıless Otherwise Specified. S_1 open for triangle, closed for sine wave.

Parameters	XR-2206M/P			XR-2206CP/D			Units	Conditions
	Min.	Typ.	Max.	Min.	Typ.	Max.		
eneral Characteristics								
ingle Supply Voltage	10		26	10		26	V	
plit-Supply Voltage	±5		±13	±5		±13	V	
upply Current		12	17		14	20	mA	$R_1 \geq 10k\Omega$
scillator Section								
ax. Operating Frequency	0.5	1		0.5	1		MHz	C = 1000pF, R_1 = 1kΩ
ɔwest Practical Frequency		0.01			0.01		Hz	C = 50µF, R_1 = 2MΩ
'equency Accuracy		±1	±4		±2		% of f_o	$f_o = 1/R_1C$
ɜmperature Stability 'equency		±10	±50		±20		ppm/°C	0°C ≤ T_A ≤ 70°C $R_1 = R_2$ = 20kΩ
ine Wave Amplitude Stability[2]		4800			4800		ppm/°C	
upply Sensitivity		0.01	0.1		0.01		%/V	V_{LOW} = 10V, V_{HIGH} = 20V, $R_1 = R_2$ = 20kΩ
weep Range	1000:1	2000:1			2000:1		$f_H = f_L$	f_H @ R_1 = 1kΩ f_L @ R_1 = 2MΩ
weep Linearity								
10:1 Sweep		2			2		%	f_L = 1kHz, f_H = 10kHz
1000:1 Sweep		8			8		%	f_L = 100Hz, f_H = 100kHz
FM Distortion		0.1			0.1		%	±10% Deviation
ecommended Timing Components								
Timing Capacitor: C	0.001		100	0.001		100	µF	*Figure 5*
Timing Resistors: R_1 & R_2	1		2000	1		2000	kΩ	
iangle Sine Wave Output[1]								*Figure 3*
Triangle Amplitude		160			160		mV/kΩ	*Figure 2*, S_1 Open
Sine Wave Amplitude	40	60	80		60		mV/kΩ	*Figure 2*, S_1 Closed
Max. Output Swing		6			6		Vp-p	
Output Impedance		600			600		Ω	
Triangle Linearity		1			1		%	
Amplitude Stability		0.5			0.5		dB	For 1000:1 Sweep
ne Wave Distortion								
Without Adjustment		2.5			2.5		%	R_1 = 30kΩ
With Adjustment		0.4	1.0		0.5	1.5	%	See *Figure 7* and *Figure 8*

tes
)utput amplitude is directly proportional to the resistance, R_3, on Pin 3. See Figure 3.
'or maximum amplitude stability, R_3 should be a positive temperature coefficient resistor.
***ld face parameters** are covered by production test and guaranteed over operating temperature range.*

ELECTRICAL CHARACTERISTICS (CONT'D)

Parameters	XR-2206M/P Min.	XR-2206M/P Typ.	XR-2206M/P Max.	XR-2206CP/D Min.	XR-2206CP/D Typ.	XR-2206CP/D Max.	Units	Conditions
Amplitude Modulation								
Output Impedance	50	100		50	100		kΩ	
Modulation Range		100			100		%	
Carrier Suppression		55			55		dB	
Linearity		2			2		%	For 95% modulation
Square-Wave Output								
Amplitude		12			12		Vp-p	Measured at Pin 11.
Rise Time		250			250		ns	C_L = 10pF
Fall Time		50			50		ns	C_L = 10pF
Saturation Voltage		0.2	0.4		0.2	0.6	V	I_L = 2mA
Leakage Current		0.1	20		0.1	100	µA	V_{CC} = 26V
FSK Keying Level (Pin 9)	0.8	1.4	2.4	0.8	1.4	2.4	V	See section on circuit controls
Reference Bypass Voltage	2.9	3.1	3.3	2.5	3	3.5	V	Measured at Pin 10.

Notes
Output amplitude is directly proportional to the resistance, R_3, on Pin 3. See Figure 3.
For maximum amplitude stability, R_3 should be a positive temperature coefficient resistor.
***Bold face parameters** are covered by production test and guaranteed over operating temperature range.*

Specifications are subject to change without notice

ABSOLUTE MAXIMUM RATINGS

Power Supply 26V
Power Dissipation 750mW
Derate Above 25°C ..... 5mW/°C
Total Timing Current 6mA
Storage Temperature ..... -65°C to +150°C

SYSTEM DESCRIPTION

The XR-2206 is comprised of four functional blocks; a voltage-controlled oscillator (VCO), an analog multiplier and sine-shaper; a unity gain buffer amplifier; and a set of current switches.

The VCO produces an output frequency proportional to input current, which is set by a resistor from the timing terminals to ground. With two timing pins, two discrete output frequencies can be independently produced for FSK generation applications by using the FSK input control pin. This input controls the current switches which select one of the timing resistor currents, and routes it to the VCO.

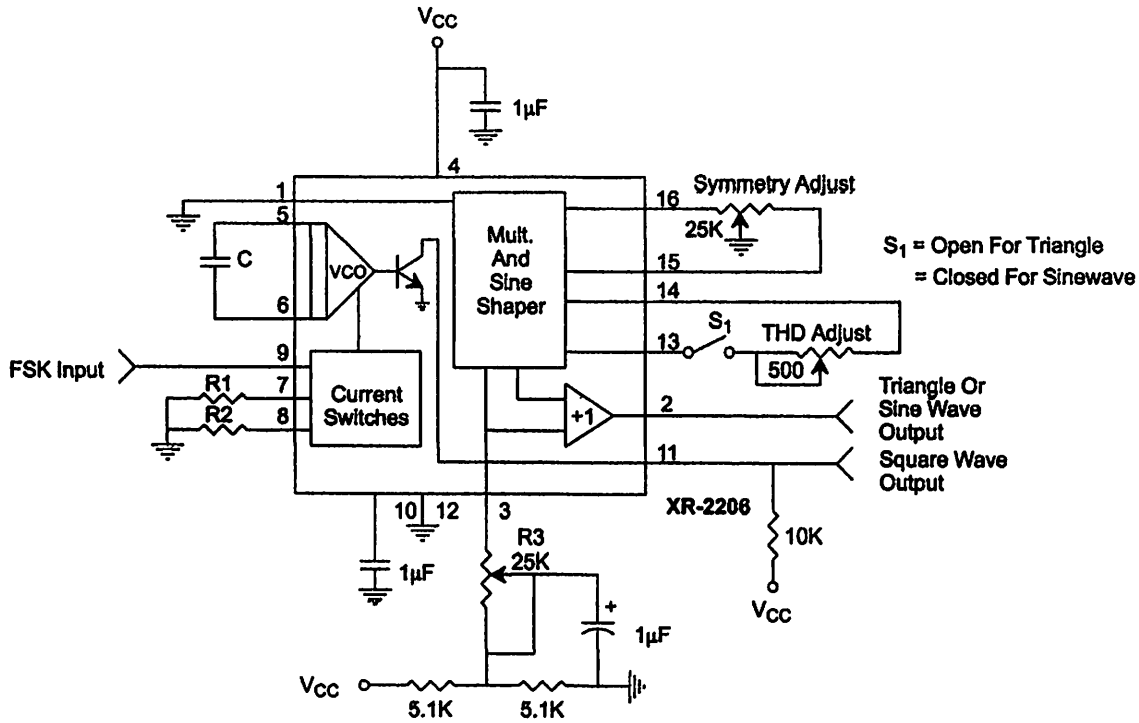


Figure 2. Basic Test Circuit

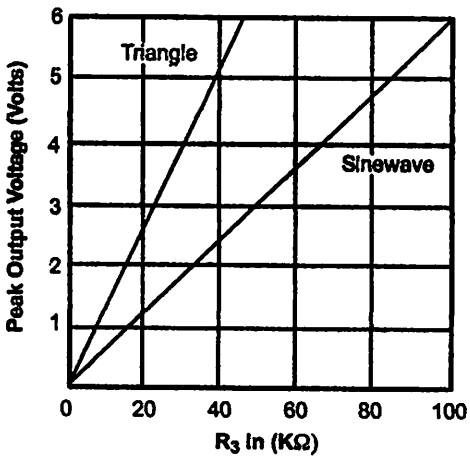


Figure 3. Output Amplitude as a Function of the Resistor, R3, at Pin 3

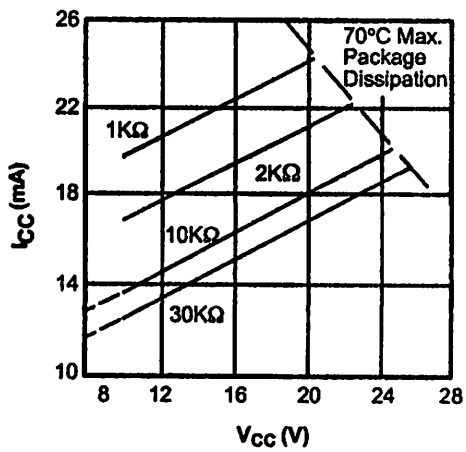


Figure 4. Supply Current vs Supply Voltage, Timing, R

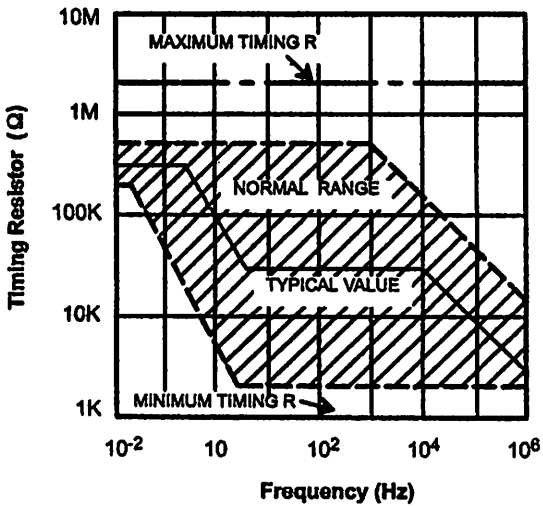


Figure 5. R versus Oscillation Frequency.

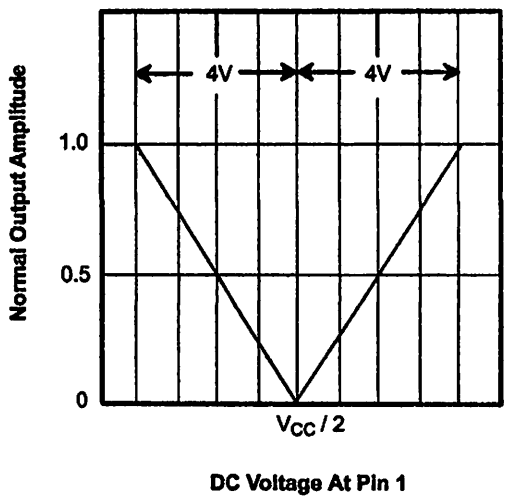


Figure 6. Normalized Output Amplitude versus DC Bias at AM Input (Pin 1)

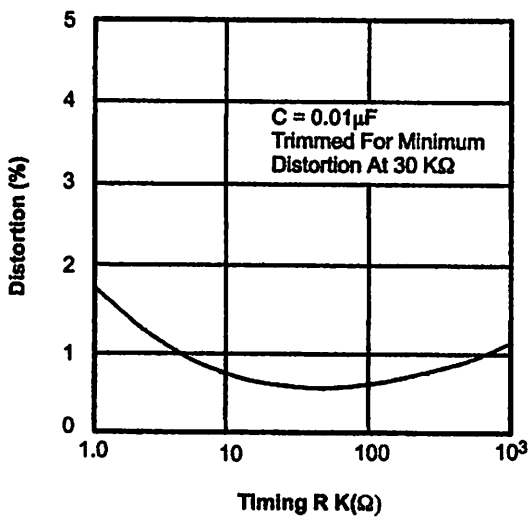


Figure 7. Trimmed Distortion versus Timing Resistor.

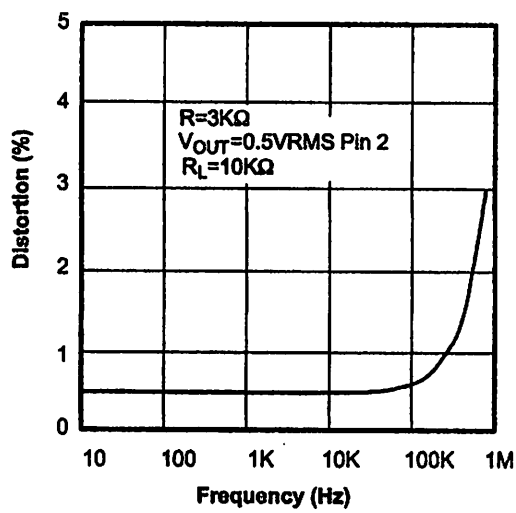


Figure 8. Sine Wave Distortion versus Operating Frequency with Timing Capacitors Varied.

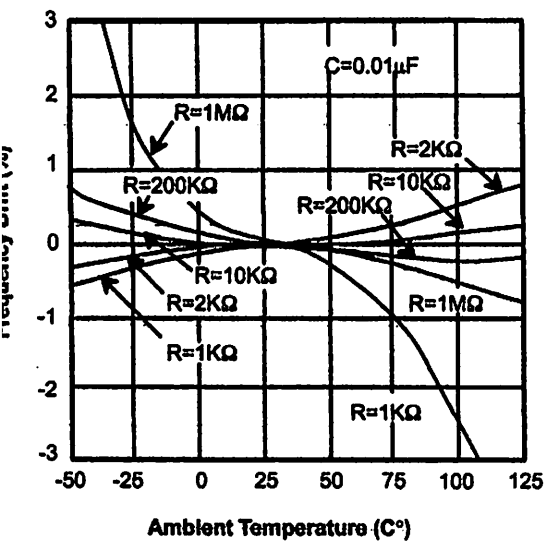


Figure 9. Frequency Drift versus Temperature.

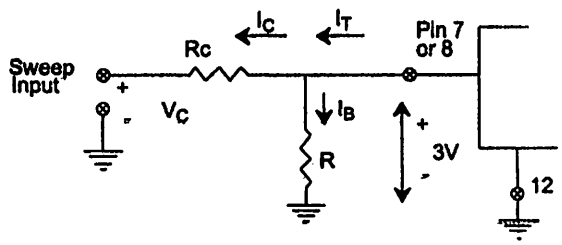


Figure 10. Circuit Connection for Frequency Sweep.

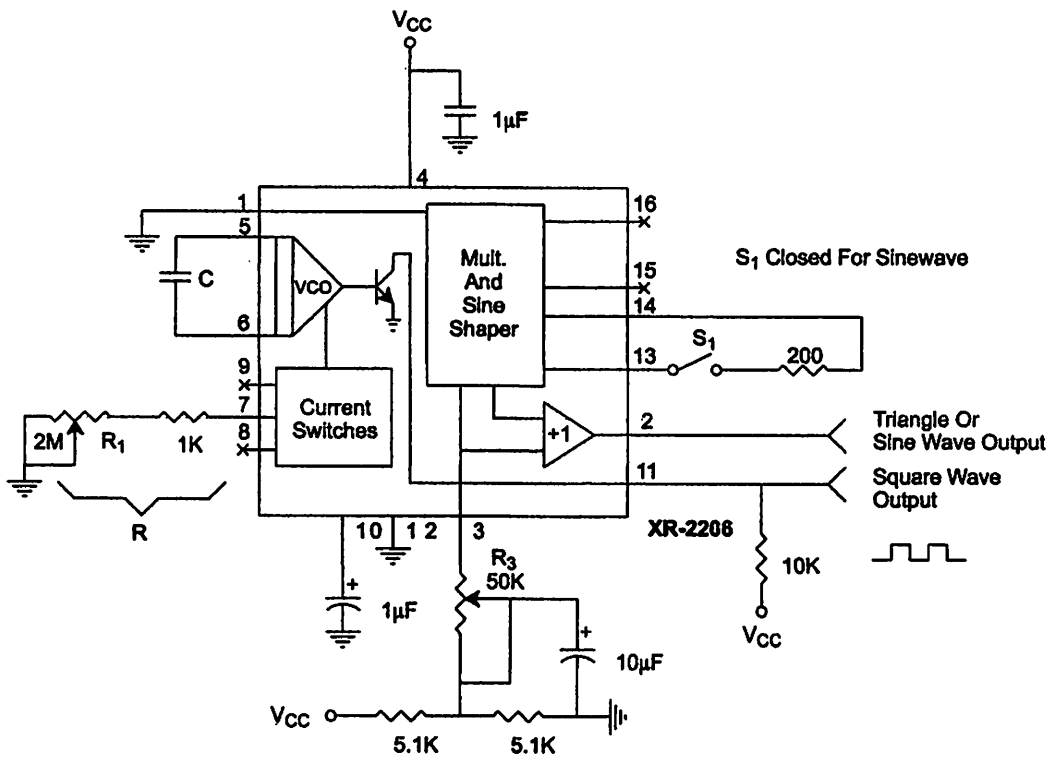


Figure 11. Circuit tor Sine Wave Generation without External Adjustment. (See *Figure 3* for Choice of R_3)

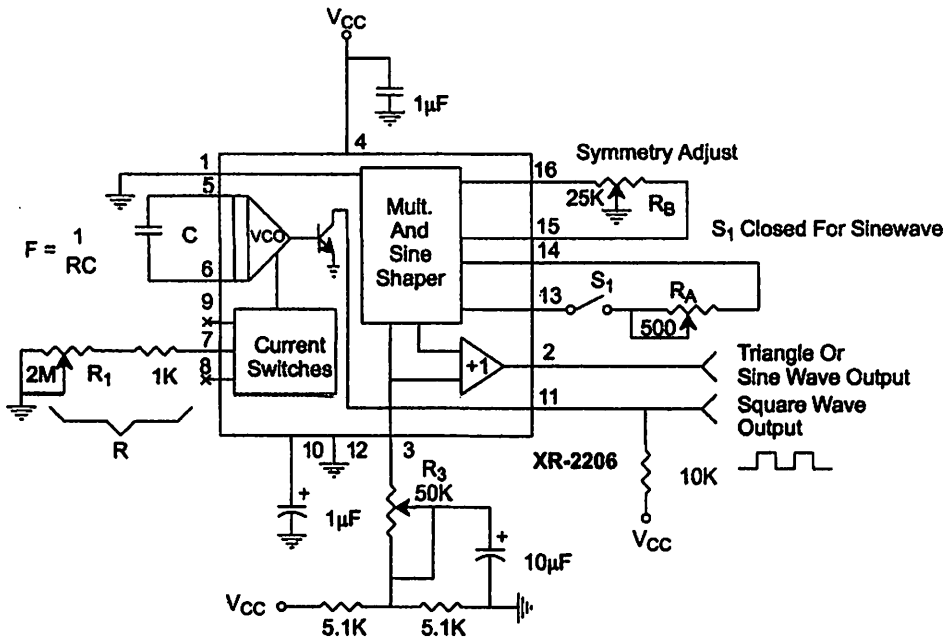


Figure 12. Circuit for Sine Wave Generation with Minimum Harmonic Distortion. (R_3 Determines Output Swing - See *Figure 3*)

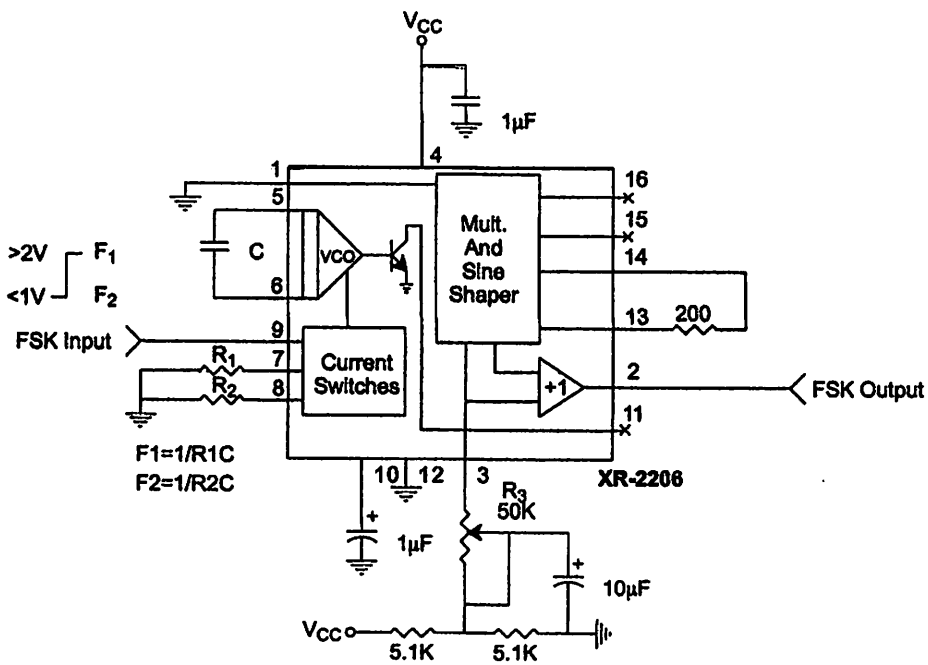


Figure 13. Sinusoidal FSK Generator

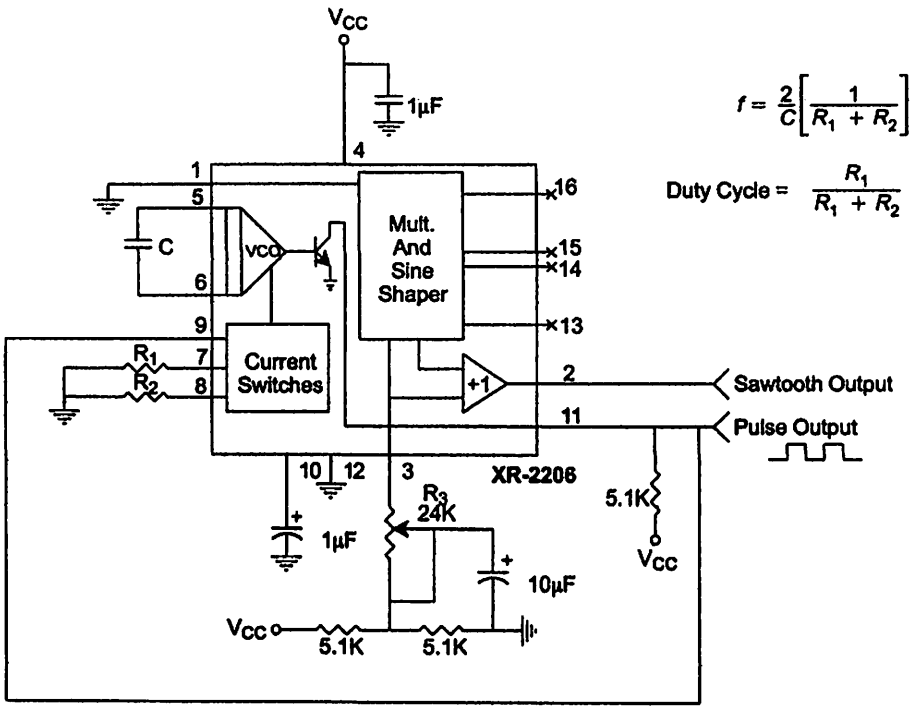


Figure 14. Circuit for Pulse and Ramp Generation.

ɔquency-Shift Keying

e XR-2206 can be operated with two separate timing ɨistors, R_1 and R_2, connected to the timing Pin 7 and 8, ɨpectively, as shown in *Figure 13*. Depending on the larity of the logic signal at Pin 9, either one or the other these timing resistors is activated. If Pin 9 is ən-circuited or connected to a bias voltage $\geq$ 2V, only is activated. Similarly, if the voltage level at Pin 9 is IV, only R_2 is activated. Thus, the output frequency can keyed between two levels. f_1 and f_2, as:

= $1/R_1C$ and $f_2 = 1/R_2C$

r split-supply operation, the keying voltage at Pin 9 is ərenced to V⁻.

ɨtput DC Level Control

ə dc level at the output (Pin 2) is approximately the ne as the dc bias at Pin 3. In *Figure 11*, *Figure 12* and *ure 13*, Pin 3 is biased midway between V+ and ɨund, to give an output dc level of $\approx V^+/2$.

APPLICATIONS INFORMATION

Sine Wave Generation

Without External Adjustment

Figure 11 shows the circuit connection for generating a sinusoidal output from the XR-2206. The potentiometer, R_1 at Pin 7, provides the desired frequency tuning. The maximum output swing is greater than $V^+/2$, and the typical distortion (THD) is < 2.5%. If lower sine wave distortion is desired, additional adjustments can be provided as described in the following section.

The circuit of *Figure 11* can be converted to split-supply operation, simply by replacing all ground connections with V⁻. For split-supply operation, R_3 can be directly connected to ground.

th External Adjustment:

e harmonic content of sinusoidal output can be luced to -0.5% by additional adjustments as shown in *jure 12*. The potentiometer, R_A, adjusts the ie-shaping resistor, and R_B provides the fine justment for the waveform symmetry. The adjustment ocedure is as follows:

Set R_B at midpoint and adjust R_A for minimum distortion.

With R_A set as above, adjust R_B to further reduce distortion.

langle Wave Generation

e circuits of *Figure 11* and *Figure 12* can be converted triangle wave generation, by simply open-circuiting Pin and 14 (i.e., S_1 open). Amplitude of the triangle is proximately twice the sine wave output.

iK Generation

jure 13 shows the circuit connection for sinusoidal FSK inal operation. Mark and space frequencies can be lependently adjusted by the choice of timing resistors, and R_2; the output is phase-continuous during nsitions. The keying signal is applied to Pin 9. The cuit can be converted to split-supply operation by nply replacing ground with V⁻.

lse and Ramp Generation

jure 14 shows the circuit for pulse and ramp waveform neration. In this mode of operation, the FSK keying minal (Pin 9) is shorted to the square-wave output (Pin), and the circuit automatically frequency-shift keys elf between two separate frequencies during the sitive-going and negative-going output waveforms. e pulse width and duty cycle can be adjusted from 1% 99% by the choice of R_1 and R_2. The values of R_1 and should be in the range of 1kΩ to 2MΩ.

PRINCIPLES OF OPERATION

Description of Controls

Frequency of Operation:

The frequency of oscillation, f_0, is determined by the external timing capacitor, C, across Pin 5 and 6, and by the timing resistor, R, connected to either Pin 7 or 8. The frequency is given as:

$$f_0 = \frac{1}{RC}\ Hz$$

and can be adjusted by varying either R or C. The recommended values of R, for a given frequency range, as shown in *Figure 5*. Temperature stability is optimum for 4kΩ < R < 200kΩ. Recommended values of C are from 1000pF to 100μF.

Frequency Sweep and Modulation:

Frequency of oscillation is proportional to the total timing current, I_T, drawn from Pin 7 or 8:

$$f = \frac{320 I_T(mA)}{C(\mu F)}\ Hz$$

Timing terminals (Pin 7 or 8) are low-impedance points, and are internally biased at +3V, with respect to Pin 12. Frequency varies linearly with IT, over a wide range of current values, from 1μA to 3mA. The frequency can be controlled by applying a control voltage, V_C, to the activated timing pin as shown in *Figure 10*. The frequency of oscillation is related to VC as:

$$f = \frac{1}{RC}\left(1 + \frac{R}{R_c}\left(1 - \frac{V_c}{3}\right)\right) Hz$$

where V_C is in volts. The voltage-to-frequency conversion gain, K, is given as:

$$K = \partial f / \partial V_c = -\frac{0.32}{R_c C}\ \ Hz/V$$

CAUTION: *For safety operation of the circuit, I_T should be limited to ≤ 3mA.*

tput Amplitude:

ximum output amplitude is inversely proportional to external resistor, R_3, connected to Pin 3 (see *ure 3*). For sine wave output, amplitude is roximately 60mV peak per kΩ of R_3; for triangle, the ak amplitude is approximately 160mV peak per kΩ of Thus, for example, R_3 = 50kΩ would produce roximately 13V sinusoidal output amplitude.

plitude Modulation:

tput amplitude can be modulated by applying a dc bias d a modulating signal to Pin 1. The internal impedance at Pin 1 is approximately 100kΩ. Output amplitude varies linearly with the applied voltage at Pin 1, for values of dc bias at this pin, within 14 volts of $V_{CC}/2$ as shown in *Figure 6.* As this bias level approaches $V_{CC}/2$, the phase of the output signal is reversed, and the amplitude goes through zero. This property is suitable for phase-shift keying and suppressed-carrier AM generation. Total dynamic range of amplitude modulation is approximately 55dB.

CAUTION: *AM control must be used in conjunction with a well-regulated supply, since the output amplitude now becomes a function of* V_{CC}.

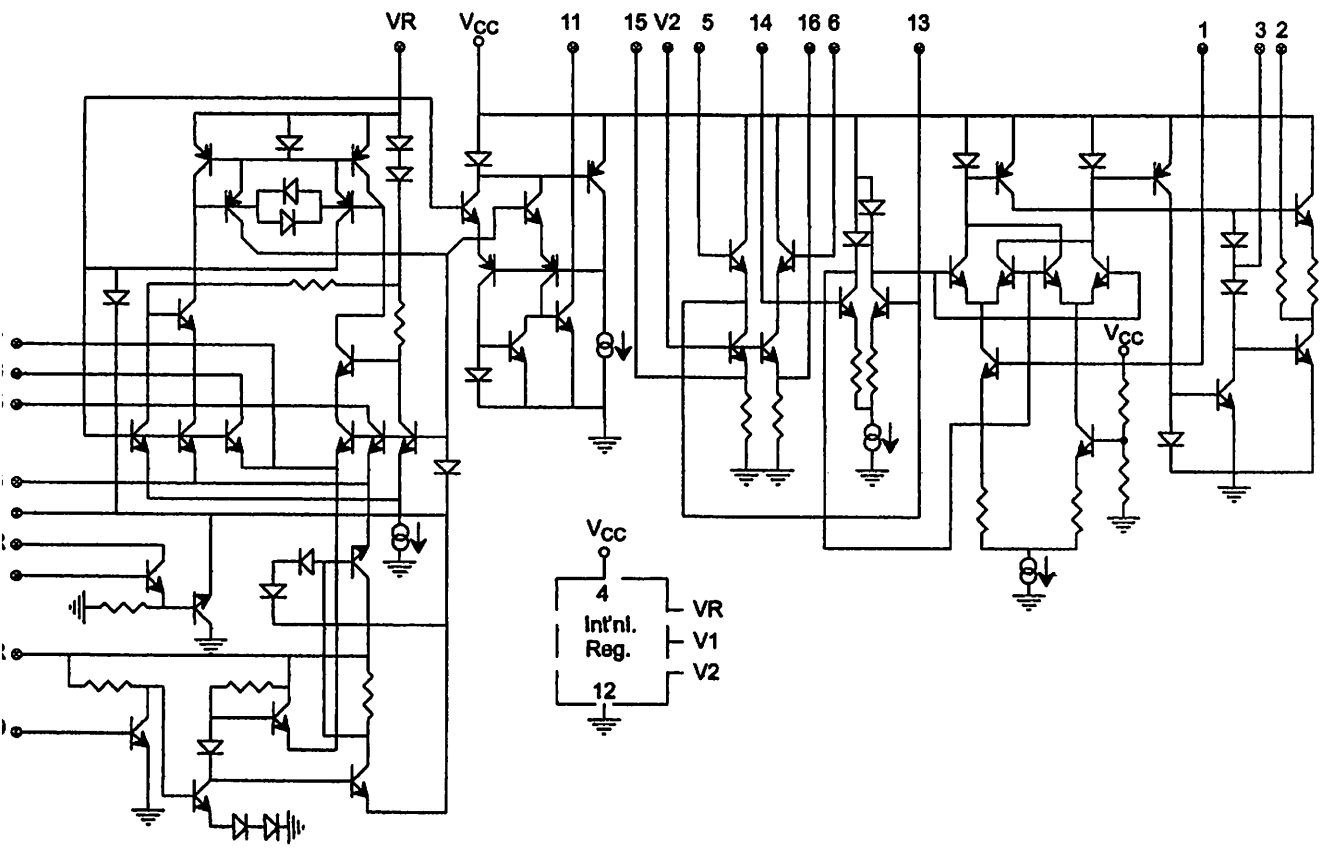
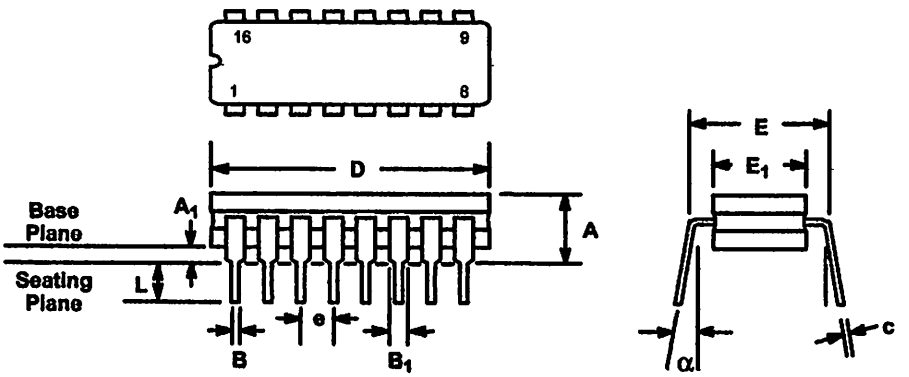


Figure 15. Equivalent Schematic Diagram

16 LEAD CERAMIC DUAL-IN-LINE (300 MIL CDIP)

Rev. 1.00

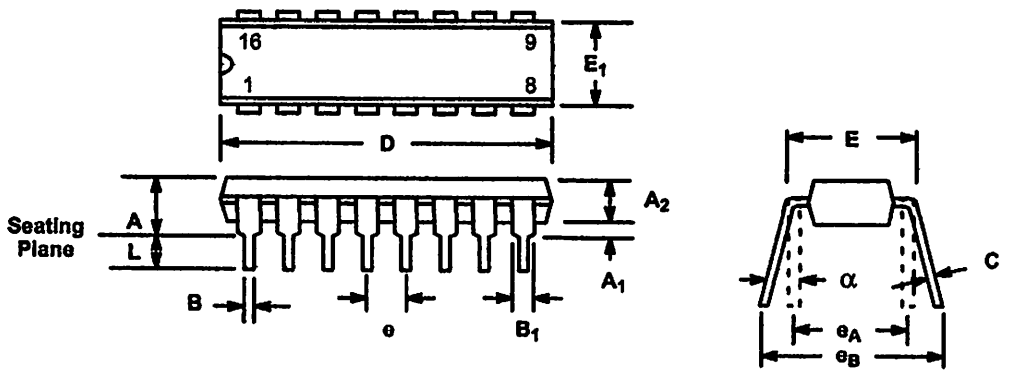


SYMBOL	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.100	0.200	2.54	5.08
A_1	0.015	0.060	0.38	1.52
B	0.014	0.026	0.36	0.66
B_1	0.045	0.065	1.14	1.65
c	0.008	0.018	0.20	0.46
D	0.740	0.840	18.80	21.34
E_1	0.250	0.310	6.35	7.87
E	0.300 BSC		7.62 BSC	
e	0.100 BSC		2.54 BSC	
L	0.125	0.200	3.18	5.08
α	0°	15°	0°	15°

Note: The control dimension is the inch column

16 LEAD PLASTIC DUAL-IN-LINE (300 MIL PDIP)

Rev. 1.00

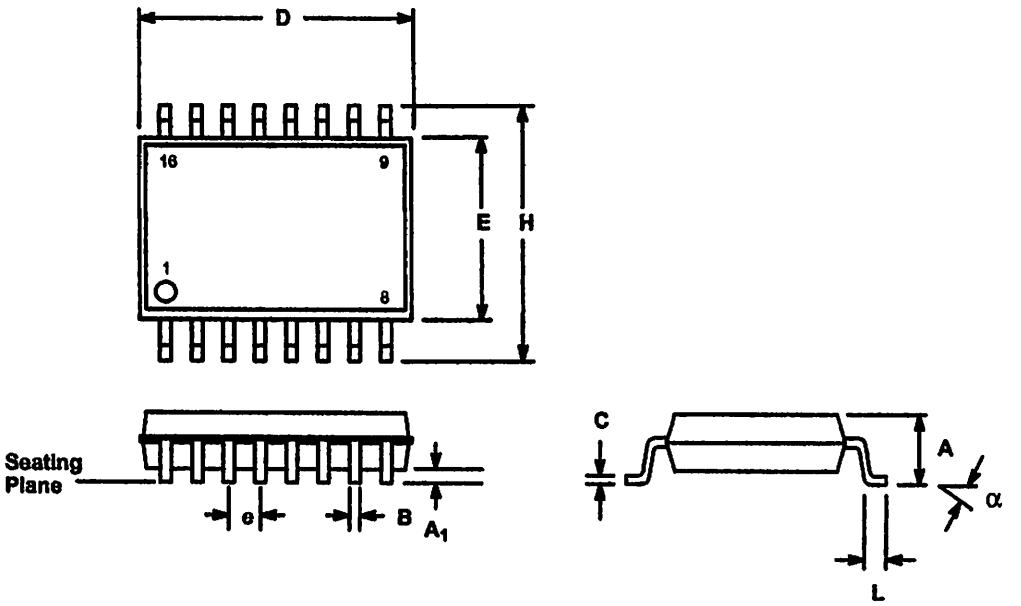


SYMBOL	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.145	0.210	3.68	5.33
A_1	0.015	0.070	0.38	1.78
A_2	0.115	0.195	2.92	4.95
B	0.014	0.024	0.36	0.56
B_1	0.030	0.070	0.76	1.78
C	0.008	0.014	0.20	0.38
D	0.745	0.840	18.92	21.34
E	0.300	0.325	7.62	8.26
E_1	0.240	0.280	6.10	7.11
e	0.100 BSC		2.54 BSC	
e_A	0.300 BSC		7.62 BSC	
e_B	0.310	0.430	7.87	10.92
L	0.115	0.160	2.92	4.06
α	0°	15°	0°	15°

Note: The control dimension is the inch column

16 LEAD SMALL OUTLINE (300 MIL JEDEC SOIC)

Rev. 1.00



SYMBOL	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.093	0.104	2.35	2.65
A_1	0.004	0.012	0.10	0.30
B	0.013	0.020	0.33	0.51
C	0.009	0.013	0.23	0.32
D	0.398	0.413	10.10	10.50
E	0.291	0.299	7.40	7.60
e	0.050 BSC		1.27 BSC	
H	0.394	0.419	10.00	10.65
L	0.016	0.050	0.40	1.27
α	0°	8°	0°	8°

Note: The control dimension is the millimeter column

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Datasheet June 1997

XR-2211

FSK Demodulator/
Tone Decoder

EXAR ...the analog plus company™

June 1997-3

EATURES

Wide Frequency Range, 0.01Hz to 300kHz
Wide Supply Voltage Range, 4.5V to 20V
HCMOS/TTL/Logic Compatibility
FSK Demodulation, with Carrier Detection
Wide Dynamic Range, 10mV to 3V rms
Adjustable Tracking Range, ±1% to 80%
Excellent Temp. Stability, ±50ppm/°C, max.

APPLICATIONS

- Caller Identification Delivery
- FSK Demodulation
- Data Synchronization
- Tone Decoding
- FM Detection
- Carrier Detection

ENERAL DESCRIPTION

ıe XR-2211 is a monolithic phase-locked loop (PLL) stem especially designed for data communications ıplications. It is particularly suited for FSK modem ıplications. It operates over a wide supply voltage range 4.5 to 20V and a wide frequency range of 0.01Hz to 10kHz. It can accommodate analog signals between mV and 3V, and can interface with conventional DTL, L, and ECL logic families. The circuit consists of a basic L for tracking an input signal within the pass band, a quadrature phase detector which provides carrier detection, and an FSK voltage comparator which provides FSK demodulation. External components are used to independently set center frequency, bandwidth, and output delay. An internal voltage reference proportional to the power supply is provided at an output pin.

The XR-2211 is available in 14 pin packages specified for military and industrial temperature ranges.

RDERING INFORMATION

Part No.	Package	Operating Temperature Range
XR-2211M	14 Pin CDIP (0.300")	-55°C to +125°C
XR-2211N	14 Pin CDIP (0.300")	-40°C to +85°C
XR-2211P	14 Pin PDIP (0.300")	-40°C to +85°C
XR-2211ID	14 Lead SOIC (Jedec, 0.150")	-40°C to +85°C

TQM™

EXAR Corporation, 48720 Kato Road, Fremont, CA 94538 ◆ (510) 668-7000 ◆ FAX (510) 668-7017

BLOCK DIAGRAM

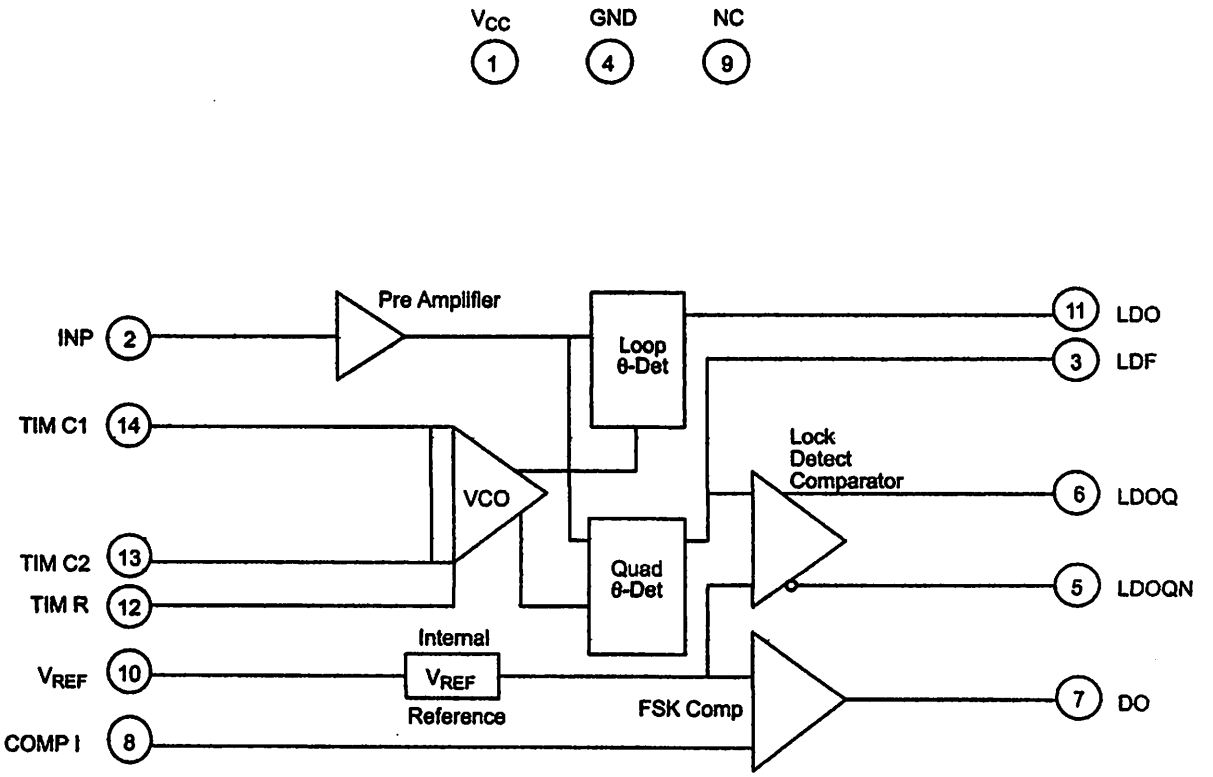
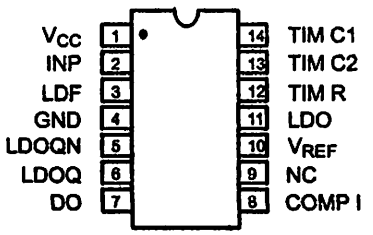
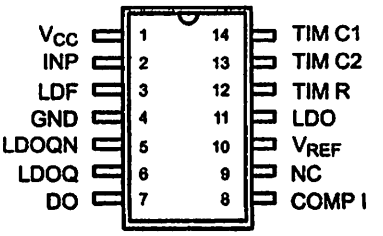


Figure 1. XR-2211 Block Diagram

N CONFIGURATION



14 Lead CDIP, PDIP (0.300")



14 Lead SOIC (Jedec, 0.150")

N DESCRIPTION

Pin #	Symbol	Type	Description
1	V_{CC}		**Positive Power Supply.**
2	INP	I	**Receive Analog Input.**
3	LDF	O	**Lock Detect Filter.**
4	GND		**Ground Pin.**
5	LDOQN	O	**Lock Detect Output Not.** This output will be low if the VCO is in the capture range.
6	LDOQ	O	**Lock Detect Output.** This output will be high if the VCO is in the capture range.
7	DO	O	**Data Output.** Decoded FSK output.
8	COMP I	I	**FSK Comparator Input.**
9	NC		**Not Connected.**
10	V_{REF}	O	**Internal Voltage Reference.** The value of V_{REF} is $V_{CC}/2$ - 650mV.
11	LDO	O	**Loop Detect Output.** This output provides the result of the quadrature phase detection.
12	TIM R	I	**Timing Resistor Input.** This pin connects to the timing resistor of the VCO.
13	TIM C2	I	**Timing Capacitor Input.** The timing capacitor connects between this pin and pin 14.
14	TIM C1	I	**Timing Capacitor Input.** The timing capacitor connects between this pin and pin 13.

.ECTRICAL CHARACTERISTICS

st Conditions: V_{CC} = 12V, T_A = +25°C, R_O = 30KΩ, C_O = 0.033µF, unless otherwise specified.

arameter	Min.	Typ.	Max.	Unit	Conditions
eneral					
upply Voltage	4.5		20	V	
upply Current		4	7	mA	$R_0 \geq$ 10KΩ. See *Figure 4.*
scillator Section					
requency Accuracy		±1	±3	%	Deviation from $f_O = 1/R_0 C_0$
requency Stability					
Temperature		±20	±50	ppm/°C	See *Figure 8.*
Power Supply		0.05	0.5	%/V	V_{CC} = 12 ±1V. See *Figure 7.*
		0.2		%/V	V_{CC} = ± 5V. See *Figure 7.*
pper Frequency Limit	100	300		kHz	R_0 = 8.2KΩ, C_0 = 400pF
owest Practical Operating requency			0.01	Hz	R_0 = 2MΩ, C_0 = 50µF
iming Resistor, R_0 - See *igure 5*					
Operating Range	5		2000	KΩ	
Recommended Range	5			KΩ	See *Figure 7* and *Figure 8.*
oop Phase Dectector Section					
eak Output Current	±150	±200	±300	µA	Measured at Pin 11
utput Offset Current		1		µA	
utput Impedance		1		MΩ	
aximum Swing	±4	± 5		V	Referenced to Pin 10
uadrature Phase Detector					Measured at Pin 3
eak Output Current	100	300		µA	
utput Impedance		1		MΩ	
aximum Swing		11		V_{PP}	
put Preampt Section					Measured at Pin 2
put Impedance		20		KΩ	
put Signal					
Voltage Required to Cause Limiting		2	10	mV rms	

tes

rameters are guaranteed over the recommended operating conditions, but are not 100% tested in production.
***ld face parameters** are covered by production test and guaranteed over operating temperature range.*

: ELECTRICAL CHARACTERISTICS (CONT'D)

st Conditions: V_{CC} = 12V, T_A = +25°C, R_O = 30KΩ, C_O = 0.033µF, unless otherwise specified.

arameter	Min.	Typ.	Max.	Unit	Conditions
oltage Comparator Section					
put Impedance		2		MΩ	Measured at Pins 3 and 8
put Bias Current		100		nA	
oltage Gain	55	70		dB	R_L = 5.1KΩ
utput Voltage Low		300	500	mV	I_C = 3mA
utput Leakage Current		0.01	10	µA	V_O = 20V
ternal Reference					
oltage Level	4.9	5.3	5.7	V	Measured at Pin 10
utput Impedance		100		Ω	AC Small Signal
laximum Source Current		80		µA	

otes

rameters are guaranteed over the recommended operating conditions, but are not 100% tested in production.
***old face parameters** are covered by production test and guaranteed over operating temperature range.*

Specifications are subject to change without notice

BSOLUTE MAXIMUM RATINGS

wer Supply 20V
ut Signal Level ..... 3V rms
wer Dissipation 900mW

Package Power Dissipation Ratings
CDIP 750mW
Derate Above T_A = 25°C ..... 8mW/°C
PDIP 800mW
Derate Above T_A = 25°C ..... 60mW/°C
SOIC 390mW
Derate Above T_A = 25°C ..... 5mW/°C

'STEM DESCRIPTION

e main PLL within the XR-2211 is constructed from an ut preamplifier, analog multiplier used as a phase tector and a precision voltage controlled oscillator CO). The preamplifier is used as a limiter such that ut signals above typically 10mV rms are amplified to a nstant high level signal. The multiplying-type phase tector acts as a digital exclusive or gate. Its output filtered) produces sum and difference frequencies of input and the VCO output. The VCO is actually a rrent controlled oscillator with its normal input current) set by a resistor (R_0) to ground and its driving current h a resistor (R_1) from the phase detector.

e output of the phase detector produces sum and ference of the input and the VCO frequencies (internally connected). When in lock, these frequencies are f_{IN}+ f_{VCO} (2 times f_{IN} when in lock) and f_{IN} - f_{VCO} (0Hz when lock). By adding a capacitor to the phase detector output, the 2 times f_{IN} component is reduced, leaving a DC voltage that represents the phase difference between the two frequencies. This closes the loop and allows the VCO to track the input frequency.

The FSK comparator is used to determine if the VCO is driven above or below the center frequency (FSK comparator). This will produce both active high and active low outputs to indicate when the main PLL is in lock (quadrature phase detector and lock detector comparator).

:INCIPLES OF OPERATION

ɜnal Input (Pin 2): Signal is AC coupled to this minal. The internal impedance at pin 2 is 20KΩ. commended input signal level is in the range of 10mV s to 3V rms.

ıadrature Phase Detector Output (Pin 3): This is the ıh impedance output of quadrature phase detector and nternally connected to the input of lock detect voltage mparator. In tone detection applications, pin 3 is nnected to ground through a parallel combination of R_D d C_D (see *Figure 3*) to eliminate the chatter at lock tect outputs. If the tone detect section is not used, pin 3 n be left open.

ck Detect Output, Q (Pin 6): The output at pin 6 is at w" state when the PLL is out of lock and goes to "high" ıte when the PLL is locked. It is an open collector type tput and requires a pull-up resistor, R_L, to V_{CC} for ɔper operation. At "low" state, it can sink up to 5mA of ıd current.

ck Detect Complement, (Pin 5): The output at pin 5 is logic complement of the lock detect output at pin 6. is output is also an open collector type stage which can ık 5mA of load current at low or "on" state.

K Data Output (Pin 7): This output is an open collector ɟic stage which requires a pull-up resistor, R_L, to V_{CC} for ɔper operation. It can sink 5mA of load current. When coding FSK signals, FSK data output is at "high" or "off" ıte for low input frequency, and at "low" or "on" state for ɟh input frequency. If no input signal is present, the logic ıte at pin 7 is indeterminate.

K Comparator Input (Pin 8): This is the high pedance input to the FSK voltage comparator. rmally, an FSK post-detection or data filter is nnected between this terminal and the PLL phase tector output (pin 11). This data filter is formed by R_F d C_F (see *Figure 3.*) The threshold voltage of the mparator is set by the internal reference voltage, V_{REF}, ailable at pin 10.

ference Voltage, V_{REF} (Pin 10): This pin is internally ısed at the reference voltage level, V_{REF}: $V_{REF} = V_{CC}/2$ 50mV. The DC voltage level at this pin forms an internal erence for the voltage levels at pins 5, 8, 11 and 12. Pin 10 must be bypassed to ground with a 0.1µF capacitor for proper operation of the circuit.

Loop Phase Detector Output (Pin 11): This terminal provides a high impedance output for the loop phase detector. The PLL loop filter is formed by R_1 and C_1 connected to pin 11 (see *Figure 3.*) With no input signal, or with no phase error within the PLL, the DC level at pin 11 is very nearly equal to V_{REF}. The peak to peak voltage swing available at the phase detector output is equal to 2 x V_{REF}.

VCO Control Input (Pin 12): VCO free-running frequency is determined by external timing resistor, R_0, connected from this terminal to ground. The VCO free-running frequency, f_0, is:

$$f_o = \frac{1}{R_0 \cdot C_0} \; Hz$$

where C_0 is the timing capacitor across pins 13 and 14. For optimum temperature stability, R_0 must be in the range of 10KΩ to 100KΩ (see *Figure 9.*)

This terminal is a low impedance point, and is internally biased at a DC level equal to V_{REF}. The maximum timing current drawn from pin 12 must be limited to ≤ 3mA for proper operation of the circuit.

VCO Timing Capacitor (Pins 13 and 14): VCO frequency is inversely proportional to the external timing capacitor, C_0, connected across these terminals (see *Figure 6.*) C_0 must be non-polar, and in the range of 200pF to 10µF.

VCO Frequency Adjustment: VCO can be fine-tuned by connecting a potentiometer, R_X, in series with R_0 at pin 12 (see *Figure 10.*)

VCO Free-Running Frequency, f_0: XR-2211 does not have a separate VCO output terminal. Instead, the VCO outputs are internally connected to the phase detector sections of the circuit. For set-up or adjustment purposes, the VCO free-running frequency can be tuned by using the generalized circuit in *Figure 3*, and applying an alternating bit pattern of 0's and 1's at the known mark and space frequencies. By adjusting R_0, the VCO can then be tuned to obtain a 50% duty cycle on the FSK output (pin 7). This will ensure that the VCO f_0 value is accurately referenced to the mark and space frequencies.

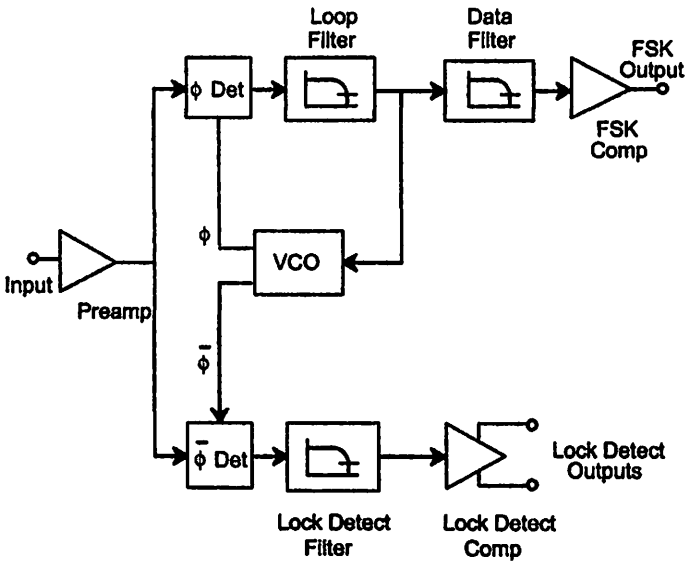


Figure 2. Functional Block Diagram of a Tone and FSK Decoding System Using XR-2211

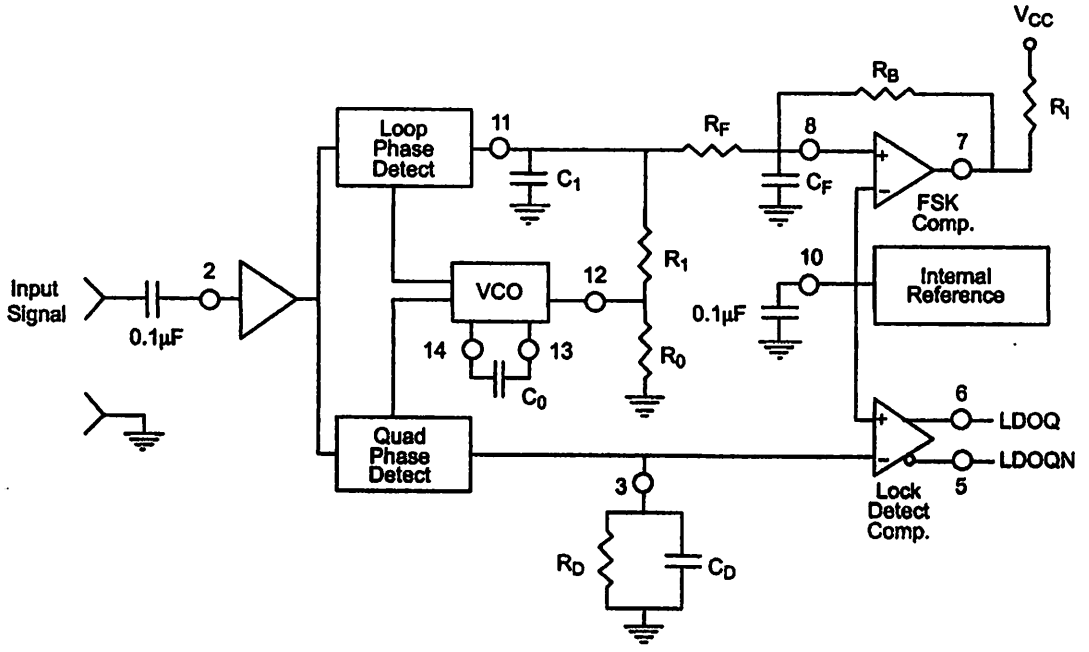


Figure 3. Generalized Circuit Connection for FSK and Tone Detection

:SIGN EQUATIONS

ll resistance in Ω, all frequency in Hz and all capacitance in farads, unless otherwise specified)

ee *Figure 3* for definition of components)

VCO Center Frequency, f_O:

$$f_O = \frac{1}{R_0 \cdot C_0}$$

Internal Reference Voltage, V_{REF} (measured at pin 10):

$$V_{REF} = \left(\frac{V_{CC}}{2}\right) - 650mV \text{ in volts}$$

Loop Low-Pass Filter Time Constant, τ:

$$\tau = C_1 \cdot R_{PP} \text{ (seconds)}$$

ıere:

$$R_{PP} = \left(\frac{R_1 \cdot R_F}{R_1 + R_F}\right)$$

R_F is ∞ or C_F reactance is ∞, then R_{PP} = R1

Loop Damping, ς:

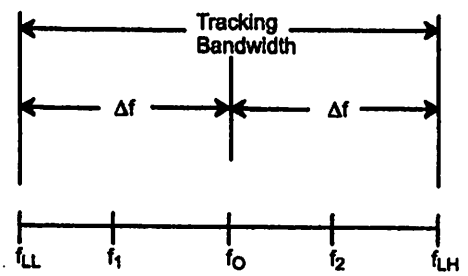
$$\zeta = \sqrt{\left(\frac{1250 \cdot C_0}{R_1 \cdot C_1}\right)}$$

ıte: For derivation/explanation of this equation, please see TAN-011.

Loop-tracking

ndwidth, $\pm = \frac{\Delta f}{f_0}$

$$\frac{\Delta f}{f_0} = \frac{R_0}{R_1}$$



FSK Data filter time constant, tF:

$$\tau_F = \frac{R_B \cdot R_F}{(R_B + R_F)} \cdot C_F \ (seconds)$$

Loop phase detector conversion gain, Kd: (Kd is the differential DC voltage across pin 10 and pin11, per unit of phase error at phase detector input):

$$K_d = \frac{V_{REF} \cdot R_1}{10,000 \cdot \pi} \left[\frac{volt}{radian}\right]$$

ote: For derivation/explanation of this equation, please see TAN-011.

VCO conversion gain, Ko: (Ko is the amount of change in VCO frequency, per unit of DC voltage change at pin 11):

$$K_0 = \frac{-2\pi}{V_{REF} \cdot C_0 \cdot R_1} = \left(\frac{radian/second}{volt}\right)$$

The filter transfer function:

$$F(s) = \frac{1}{1 + SR_1 \cdot C_1} \ at\ 0\ Hz. \qquad S = J\omega \ and \ \omega = 0$$

). Total loop gain. K_T:

$$K_T = K_O \cdot K_d \cdot F(s) = \left(\frac{R_F}{5,000 \cdot C_0 \cdot (R_1 + R_F)}\right)\left[\frac{1}{seconds}\right]$$

. Peak detector current I_A:

$$I_A = \frac{V_{REF}}{20,000} \ (V_{REF} \ in \ volts \ and \ I_A \ in \ amps)$$

ote: For derivation/explanation of this equation, please see TAN-011.

PPLICATIONS INFORMATION

SK Decoding

igure 10 shows the basic circuit connection for FSK decoding. With reference to *Figure 3* and *Figure 10*, the functions external components are defined as follows: R_0 and C_0 set the PLL center frequency, R_1 sets the system bandwidth, nd C_1 sets the loop filter time constant and the loop damping factor. C_F and R_F form a one-pole post-detection filter for e FSK data output. The resistor R_B from pin 7 to pin 8 introduces positive feedback across the FSK comparator to cilitate rapid transition between output logic states.

esign Instructions:

ne circuit of *Figure 10* can be tailored for any FSK decoding application by the choice of five key circuit components: R_0, $_1$, C_0, C_1 and C_F. For a given set of FSK mark and space frequencies, f_O and f_1, these parameters can be calculated as llows:

ll resistance in Ω's, all frequency in Hz and all capacitance in farads, unless otherwise specified)

Calculate PLL center frequency, f_O:

$$f_o = \sqrt{F_1 \cdot F_2}$$

Choose value of timing resistor R_0, to be in the range of 10KΩ to 100KΩ. This choice is arbitrary. The recommended value is R_0 = 20KΩ. The final value of R_0 is normally fine-tuned with the series potentiometer, R_X.

$$R_o = R_o + \frac{R_x}{2}$$

Calculate value of C0 from design equation (1) or from *Figure 7*:

$$C_o = \frac{1}{R_0 \cdot f_0}$$

Calculate R1 to give the desired tracking bandwidth (See design equation 5).

$$R_1 = \frac{R_0 \cdot f_0}{(f_1 - f_2)} \cdot 2$$

Calculate C1 to set loop damping. (See design equation 4):

Normally, $\varsigma = 0.5$ is recommended.

$$C_1 = \frac{1250 \cdot C_0}{R_1 \cdot \varsigma^2}$$

The input to the XR-2211 may sometimes be too sensitive to noise conditions on the input line. *Figure 4* illustrates a method of de-sensitizing the XR-2211 from such noisy line conditions by the use of a resistor, Rx, connected from pin 2 to ground. The value of Rx is chosen by the equation and the desired minimum signal threshold level.

$$V_{IN}\ minimum\ (peak) = V_a - V_b = \Delta V \pm 2.8mV\ offset = V_{REF}\frac{20,000}{(20,000 + R_x)}\ or\ R_x = 20,000\left(\frac{V_{REF}}{\Delta V} - 1\right)$$

$_{IN}$ minimum (peak) input voltage must exceed this value to be detected (equivalent to adjusting V threshold)

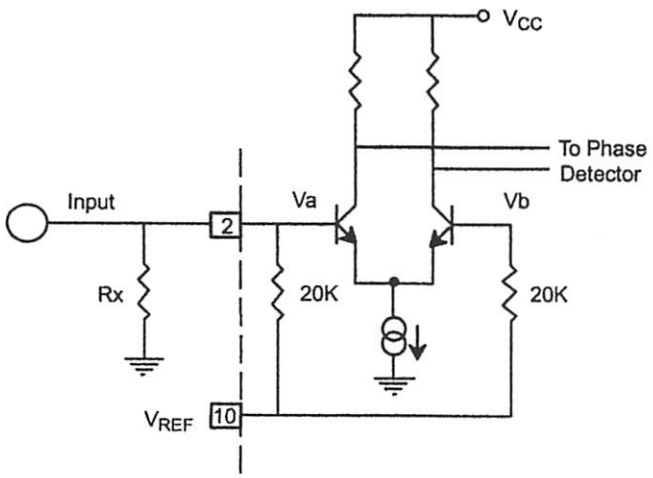


Figure 4. Desensitizing Input Stage

Calculate Data Filter Capacitance, C_F:

$$R_{sum} = \frac{(R_F + R_1)\cdot R_B}{(R_1 + R_F + R_B)}$$

$$C_F = \frac{0.25}{(R_{sum}\cdot Baud\ Rate)} \qquad Baud\ rate\ in\ \frac{1}{seconds}$$

ote: *All values except R_0 can be rounded to nearest standard value.*

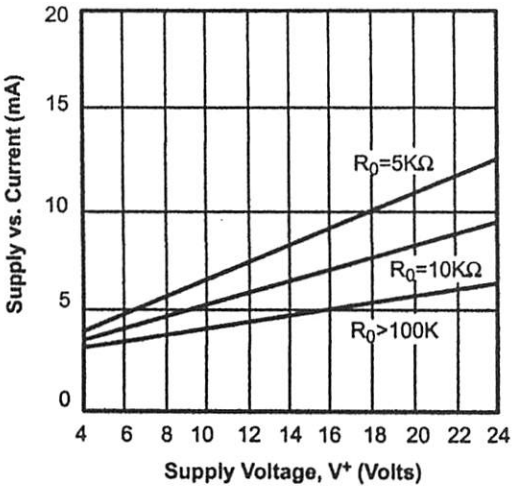


Figure 5. Typical Supply Current vs. V+ (Logic Outputs Open Circuited)

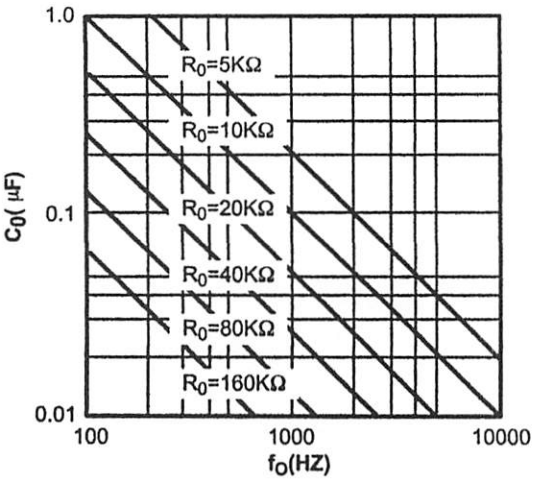


Figure 6. VCO Frequency vs. Timing Resistor

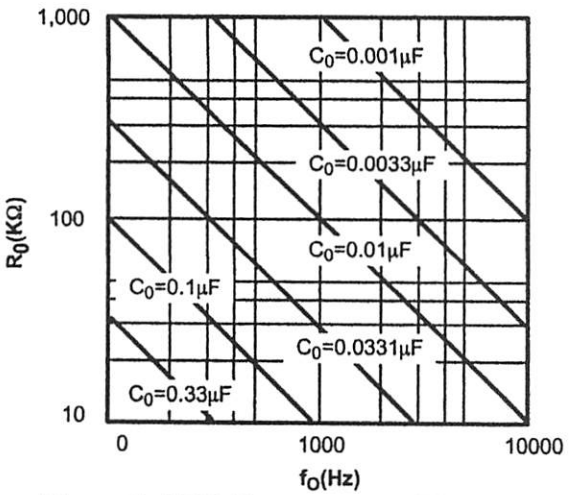


Figure 7. VCO Frequency vs. Timing Capacitor

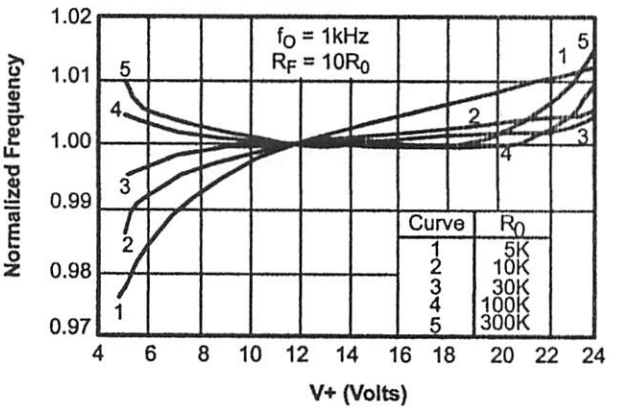


Figure 8. Typical f_O vs. Power Supply Characteristics

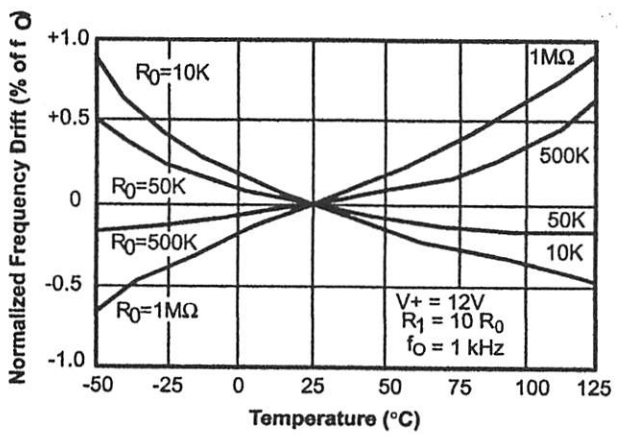


Figure 9. Typical Center Frequency Drift vs. Temperature

esign Example:

:00 Baud FSK demodulator with mark and space frequencies of 1200/2200.

:ep 1: Calculate f_O: from design instructions

(a) $f_o = \sqrt{1200 \cdot 2200} = 1624$

:ep 2: Calculate R_0 : R_0 =10K with a potentiometer of 10K. (See design instructions (b))

(b) $R_T = 10 + \left(\frac{10}{2}\right) = 15K$

:ep 3: Calculate C_0 from design instructions

(c) $C_o = \frac{1}{15000 \cdot 1624} = 39nF$

:ep 4: Calculate R_1 : from design instructions

(d) $R_1 = \frac{20000 \cdot 1624 \cdot 2}{(2200-1200)} = 51,000$

:ep 5: Calculate C_1 : from design instructions

(e) $C_1 = \frac{1250 \cdot 39nF}{51000 \cdot 0.5^2} = 3.9nF$

:ep 6: Calculate R_F : R_F should be at least five times R_1, R_F = 51,000·5 = 255 KΩ

:ep 7: Calculate R_B : R_B should be at least five times R_F, R_B = 255,000·5 = 1.2 MΩ

:ep 8: Calculate R_{SUM} :

$$R_{SUM} = \frac{(R_F + R_1) \cdot R_B}{(R_F + R_1 + R_B)} = 240K\Omega$$

:ep 9: Calculate C_F :

$$C_F = \frac{0.25}{(R_{SUM} \cdot Baud\ Rate)} = 1nF$$

:te: All values except R_0 can be rounded to nearest standard value.

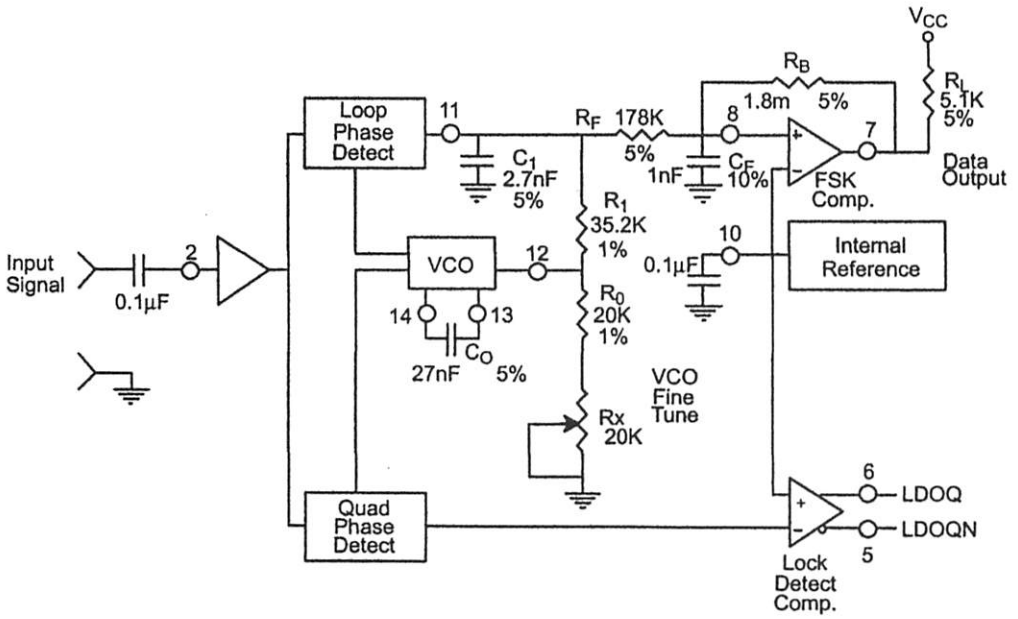


Figure 10. Circuit Connection for FSK Decoding of Caller Identification Signals (Bell 202 Format)

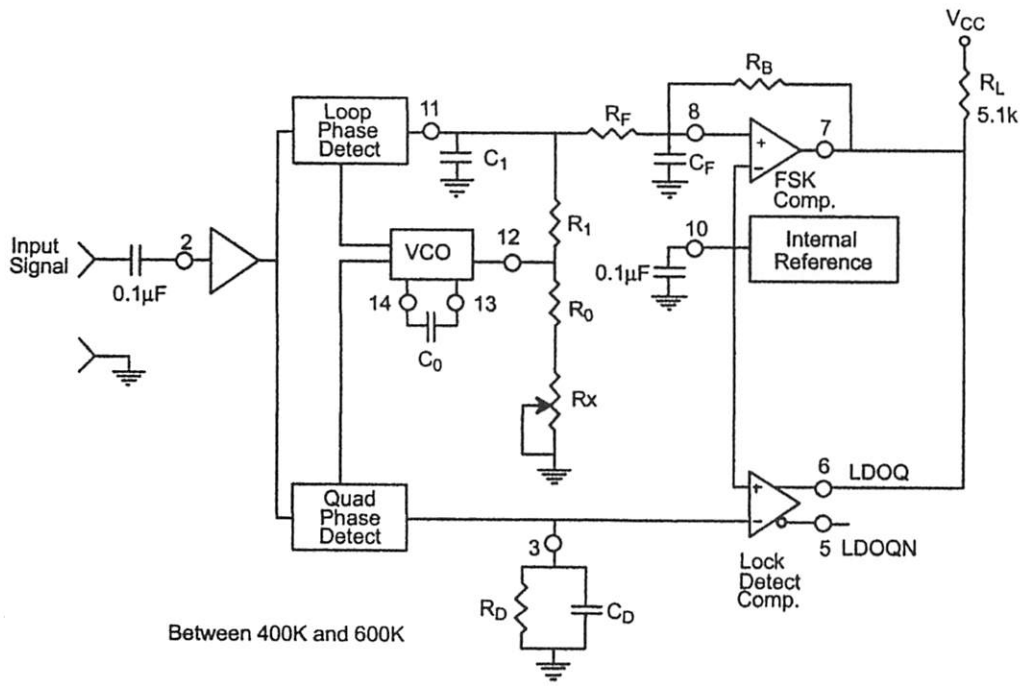


Figure 11. External Connectors for FSK Demodulation with Carrier Detect Capability

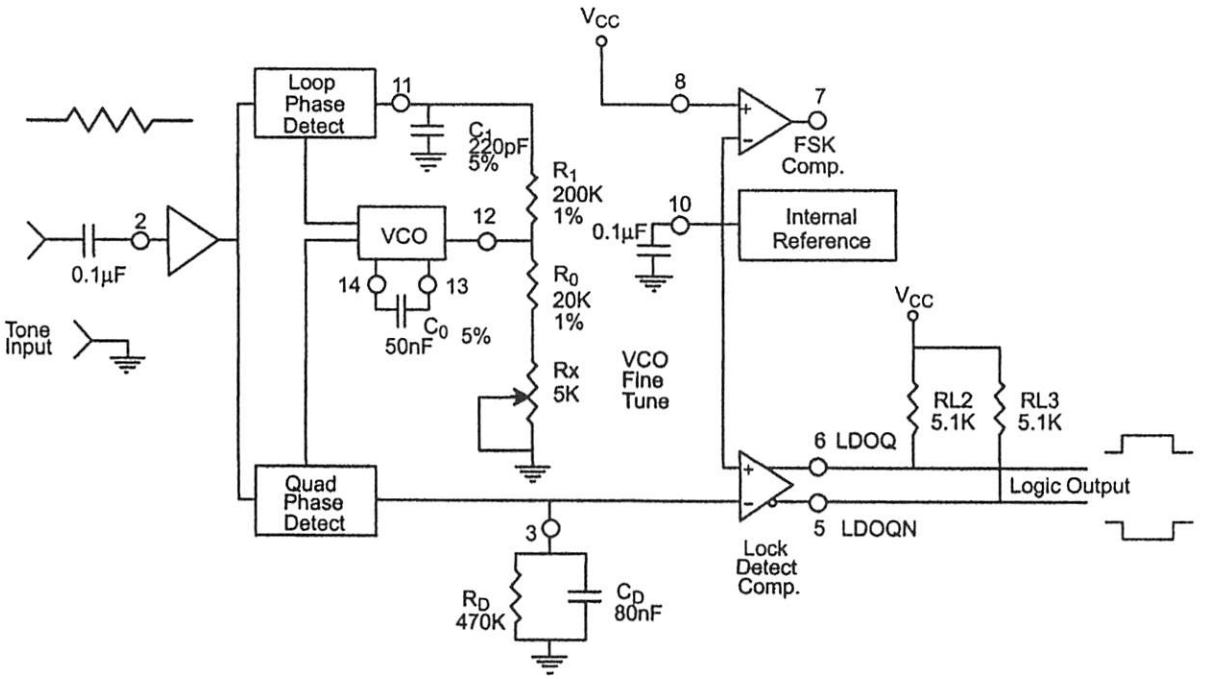


Figure 12. Circuit Connection for Tone Detection

SK Decoding with Carrier Detect

ıe lock detect section of XR-2211 can be used as a ırrier detect option for FSK decoding. The commended circuit connection for this application is ıown in *Figure 11*. The open collector lock detect output, ı 6, is shorted to data output (pin 7). Thus, data output ll be disabled at "low" state, until there is a carrier within e detection band of the PLL and the pin 6 output goes igh" to enable the data output.

***ote:** Data Output is "Low" When No Carrier is Present.*

ıe minimum value of the lock detect filter capacitance ɔ is inversely proportional to the capture range, ±Δfc. ıis is the range of incoming frequencies over which the ɔp can acquire lock and is always less than the tracking ıge. It is further limited by C_1. For most applications, Δfc Δf/2. For R_D = 470KΩ, the approximate minimum value C_D can be determined by:

$$C_D > \frac{16}{\Delta f} \quad C \text{ in } \mu F \text{ and } f \text{ in Hz.}$$

C in µF and f in Hz.

ith values of C_D that are too small, chatter can be ɔserved on the lock detect output as an incoming signal frequency approaches the capture bandwidth. Excessively large values of C_D will slow the response time of the lock detect output. For Caller I.D. applications choose C_D = 0.1µF.

Tone Detection

Figure 12 shows the generalized circuit connection for tone detection. The logic outputs, LDOQN and LDOQ at pins 5 and 6 are normally at "high" and "low" logic states, respectively. When a tone is present within the detection band of the PLL, the logic state at these outputs become reversed for the duration of the input tone. Each logic output can sink 5mA of load current.

Both outputs at pins 5 and 6 are open collector type stages, and require external pull-up resistors R_{L2} and R_{L3}, as shown in *Figure 12.*

With reference to *Figure 3* and *Figure 12*, the functions of the external circuit components can be explained as follows: R_0 and C_0 set VCO center frequency; R_1 sets the detection bandwidth; C_1 sets the low pass-loop filter time constant and the loop damping factor.

esign Instructions:

ne circuit of *Figure 12* can be optimized for any tone detection application by the choice of the 5 key circuit components: $_0$, R_1, C_0, C_1 and C_D. For a given input, the tone frequency, f_S, these parameters are calculated as follows:

ll resistance in Ω's, all frequency in Hz and all capacitance in farads, unless otherwise specified)

) Choose value of timing resistor R_0 to be in the range of 10KΩ to 50KΩ. This choice is dictated by the max./min. current that the internal voltage reference can deliver. The recommended value is $R_0 = 20K\Omega$. The final value of R_0 is normally fine-tuned with the series potentiometer, R_X.

) Calculate value of C_0 from design equation (1) or from *Figure 7* $f_S = f_O$:

$$C_O = \frac{1}{R_0 \cdot fs}$$

Calculate R_1 to set the bandwidth $\pm\Delta f$ (See design equation 5):

$$R_1 = \frac{R_0 \cdot f_0 \cdot 2}{\Delta f}$$

ote: *The total detection bandwidth covers the frequency range of* $f_O \pm \Delta f$

) Calculate value of C_1 for a given loop damping factor:

Normally, $\varsigma = 0.5$ is recommended.

$$C_1 = \frac{1250 \cdot C_0}{R_1 \cdot \varsigma^2}$$

Increasing C_1 improves the out-of-band signal rejection, but increases the PLL capture time.

Calculate value of the filter capacitor C_D . To avoid chatter at the logic output, with $R_D = 470K\Omega$, C_D must be:

$$C_D > \frac{16}{\Delta f} \quad C \text{ in } \mu F$$

Increasing C_D slows down the logic output response time.

esign Examples:

ne detector with a detection band of ± 100Hz:

Choose value of timing resistor R_0 to be in the range of 10KΩ to 50KΩ. This choice is dictated by the max./min. current that the internal voltage reference can deliver. The recommended value is $R_0 = 20\ K\Omega$. The final value of R_0 is normally fine-tuned with the series potentiometer, R_X.

Calculate value of C_0 from design equation (1) or from *Figure 6* $f_S = f_O$:

$$C_0 = \frac{1}{R_0 \cdot f_s} = \frac{1}{20,000 \cdot 1,000} = 50nF$$

) Calculate R_1 to set the bandwidth $\pm\Delta f$ (See design equation 5):

$$R_1 = \frac{R_0 \cdot f_O \cdot 2}{\Delta f} = \frac{20,000 \cdot 1,000 \cdot 2}{100} = 400K$$

ote: The total detection bandwidth covers the frequency range of $f_O \pm \Delta f$

) Calculate value of C_0 for a given loop damping factor:

Normally, $\varsigma = 0.5$ is recommended.

$$C_1 = \frac{1250 \cdot C_0}{R_1 \cdot \varsigma^2} = \frac{1250 \cdot 50 \cdot 10^{-9}}{400,000 \cdot 0.5^2} = 6.25pF$$

Increasing C_1 improves the out-of-band signal rejection, but increases the PLL capture time.

) Calculate value of the filter capacitor C_D . To avoid chatter at the logic output, with R_D = 470KΩ, C_D must be:

$$C_D = \frac{16}{\Delta f} \geq \frac{16}{200} \geq 80nF$$

Increasing C_D slows down the logic output response time.

Fine tune center frequency with 5KΩ potentiometer, R_X.

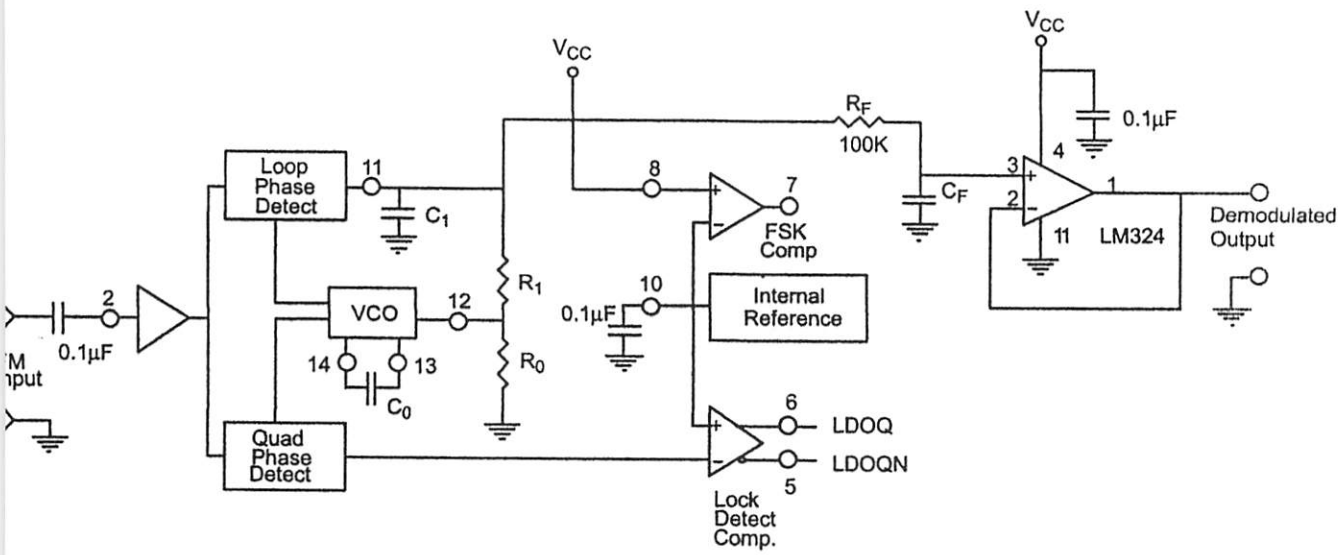


Figure 13. Linear FM Detector Using XR-2211 and an External Op Amp. (See Section on Design Equation for Component Values.)

inear FM Detection

R-2211 can be used as a linear FM detector for a wide ınge of analog communications and telemetry ɔplications. The recommended circuit connection for is application is shown in *Figure 13.* The demodulated ıtput is taken from the loop phase detector output (pin), through a post-detection filter made up of R_F and C_F, ıd an external buffer amplifier. This buffer amplifier is ecessary because of the high impedance output at pin . Normally, a non-inverting unity gain op amp can be sed as a buffer amplifier, as shown in *Figure 13.*

The FM detector gain, i.e., the output voltage change per unit of FM deviation can be given as:

$$V_{OUT} = \frac{R_1 \cdot V_{REF}}{100 \cdot R_0}$$

where VR is the internal reference voltage ($V_{REF} = V_{CC}/2$ - 650mV). For the choice of external components R_1, R_0, C_D, C_1 and C_F, see the section on design equations.

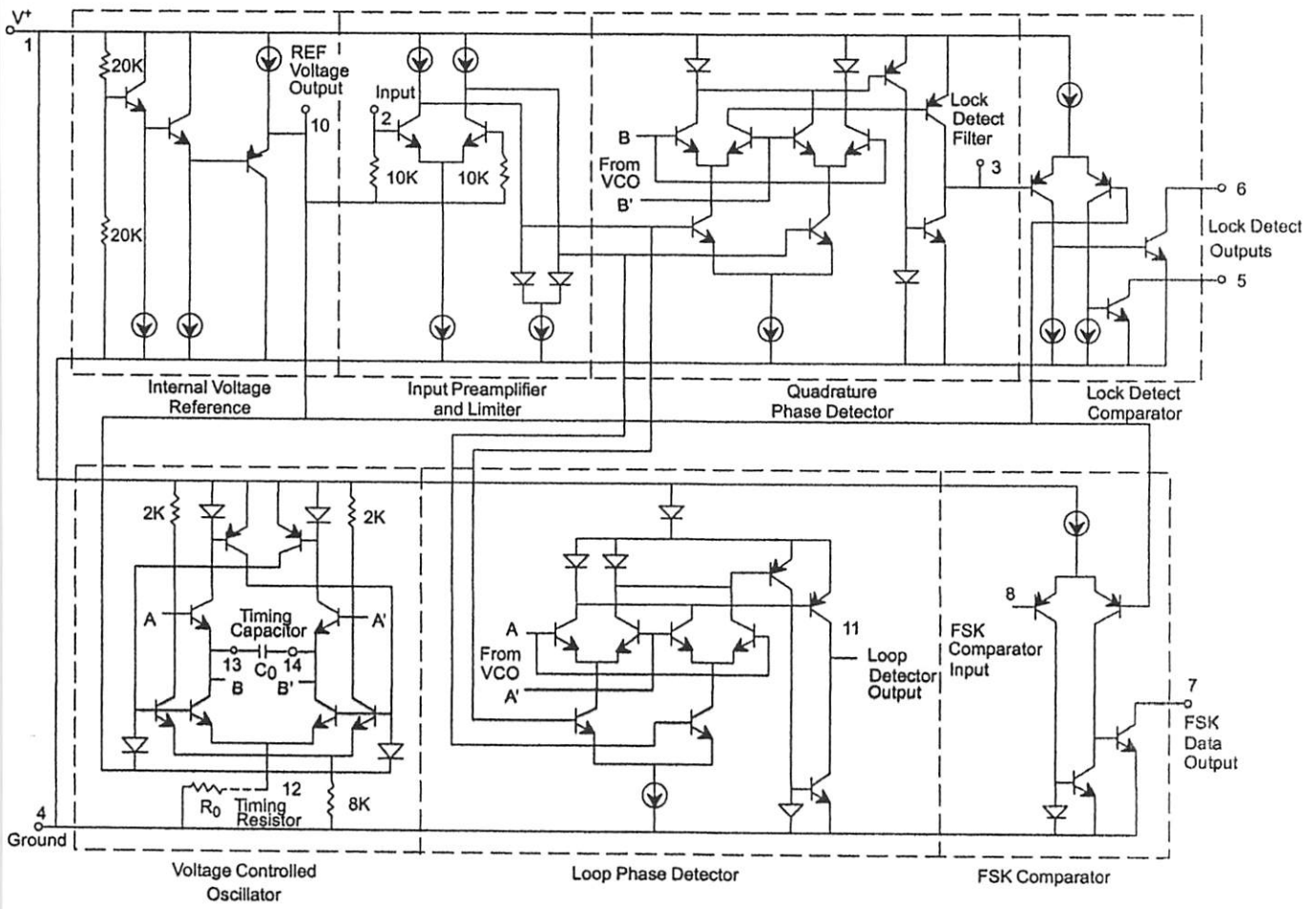
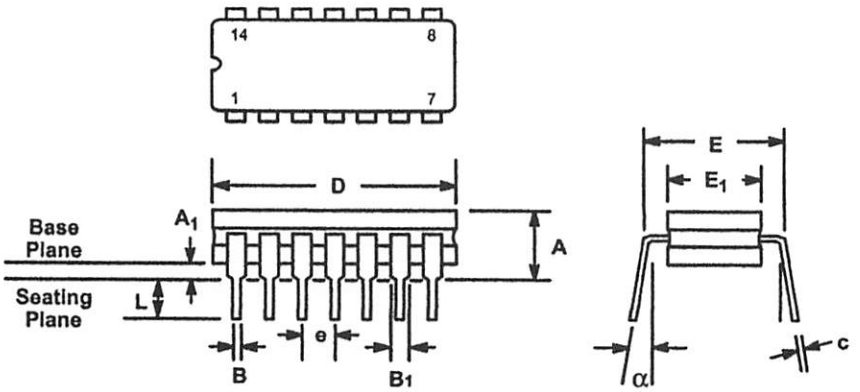


Figure 14. Equivalent Schematic Diagram

14 LEAD CERAMIC DUAL-IN-LINE (300 MIL CDIP)

Rev. 1.00

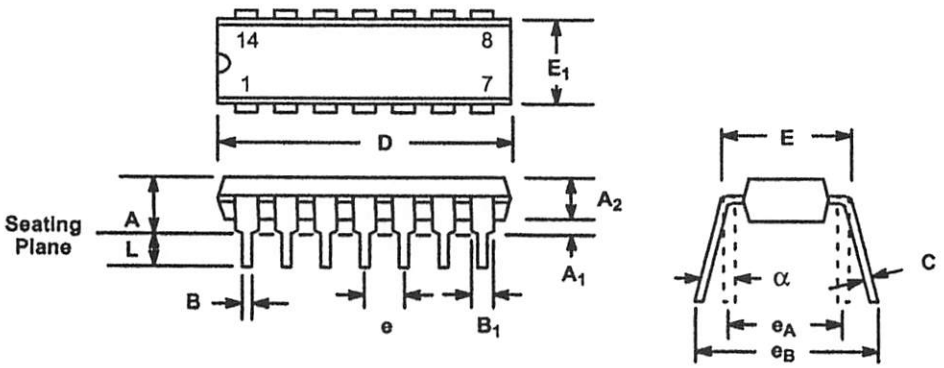


SYMBOL	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.100	0.200	2.54	5.08
A_1	0.015	0.060	0.38	1.52
B	0.014	0.026	0.36	0.66
B_1	0.045	0.065	1.14	1.65
c	0.008	0.018	0.20	0.46
D	0.685	0.785	17.40	19.94
E_1	0.250	0.310	6.35	7.87
E	0.300 BSC		7.62 BSC	
e	0.100 BSC		2.54 BSC	
L	0.125	0.200	3.18	5.08
α	0°	15°	0°	15°

Note: The control dimension is the inch column

14 LEAD PLASTIC DUAL-IN-LINE (300 MIL PDIP)

Rev. 1.00

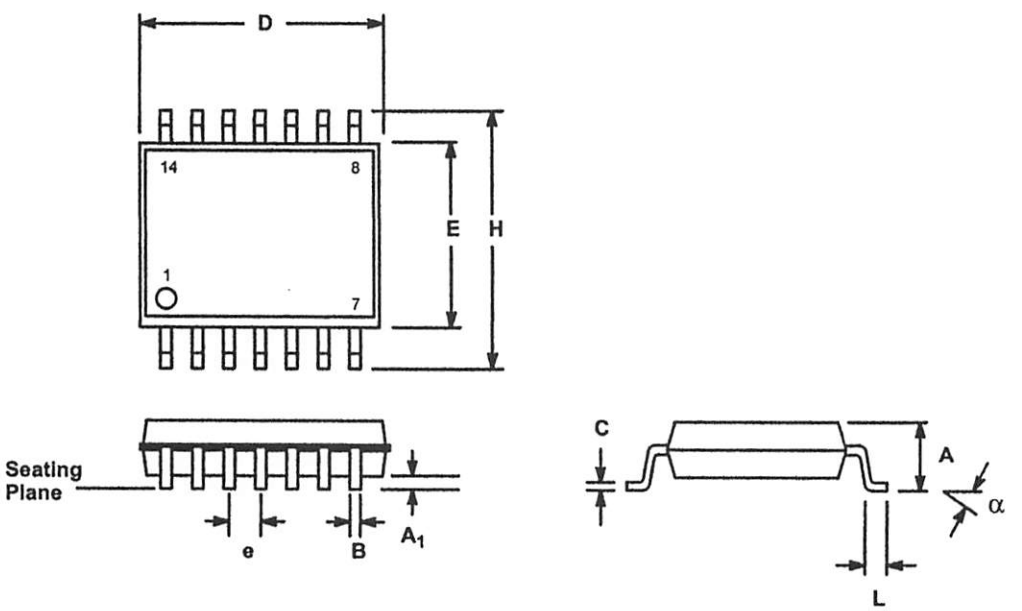


SYMBOL	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.145	0.210	3.68	5.33
A_1	0.015	0.070	0.38	1.78
A_2	0.115	0.195	2.92	4.95
B	0.014	0.024	0.36	0.56
B_1	0.030	0.070	0.76	1.78
C	0.008	0.014	0.20	0.38
D	0.725	0.795	18.42	20.19
E	0.300	0.325	7.62	8.26
E_1	0.240	0.280	6.10	7.11
e	0.100 BSC		2.54 BSC	
e_A	0.300 BSC		7.62 BSC	
e_B	0.310	0.430	7.87	10.92
L	0.115	0.160	2.92	4.06
α	0°	15°	0°	15°

Note: The control dimension is the inch column

14 LEAD SMALL OUTLINE (150 MIL JEDEC SOIC)

Rev. 1.00



SYMBOL	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.053	0.069	1.35	1.75
A_1	0.004	0.010	0.10	0.25
B	0.013	0.020	0.33	0.51
C	0.007	0.010	0.19	0.25
D	0.337	0.344	8.55	8.75
E	0.150	0.157	3.80	4.00
e	0.050 BSC		1.27 BSC	
H	0.228	0.244	5.80	6.20
L	0.016	0.050	0.40	1.27
α	0°	8°	0°	8°

Note: The control dimension is the millimeter column

Notes

Notes

NOTICE

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FAKULTAS TEKNOLOGI INDUSTRI
JURUSAN TEKNIK ELEKTRO D-III
PROGRAM STUDI TEKNIK ELEKTRONIKA
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1	Perbaikan Abstraksi	
2	Perbaikan Tata Tulis	

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Dosen Pembimbing : Joseph Dedy Irawan, ST, MT

No	Tanggal	Assistensi	Paraf
1	20/8 - 2007	Revisi bab II : Sumber gambar	
2	23/8 - 2007	ACC Bab I, II	
3	27/8 - 2007	Revisi Bab III : Judul gambar	
4	3/9 - 2007	ACC Bab III Revisi bab IV : Tambahkan Error	
5	9/9 - 2007	ACC Bab IV Revisi bab V : Tambahkan kesimpulan	
6	12 - 9 - 2007	ACC UJIAN	

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