PERENCANAAN DAN PEMBUATAN ALAT PEMANTAU KEBOCORAN GAS LPG BERBASIS MIKROKONTROLLER AT89s51

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JURUSAN TEKNIK ELEKTRO D-III

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INSTITUT TEKNOLOGI NASIONAL MALANG

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Alhamdulillah Tugas Akhir dengan judul "PERENCANAAN DAN PEMBUATAN ALAT PEMANTAU KEBOCORAN GAS LPG ini dapat diselesaikan dengan baik. Tugas Akhir ini merupakan salah satu syarat kelulusan Program D-III Teknik Elektro, Konsentrasi Teknik Elektronika, Fakultas Teknologi Industri, Institut Teknologi Nasional Malang.

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Penulis

ABSTRAKSI

PURWANTI, VENY. Judul, Perencanaan dan pembuatan Alat Pemantau Kebocoran Gas LPG Berbasis Mikrokontroler AT89s51, 03.57.039, Tugas Akhir, Jurusan Teknik Elektronika, Fakultas Teknologi Industri Institut Teknologi Nasional Malang, Dosen Pembimbing, Bambang Prio Hartono, STMT.

Kata-kunci : bas, lpg, kebocoran, perencanaan alat, sensor.

Karena sifatnya yang mudah terbakar, sering kita mendengar berita tentang kebakaran rumah akibat kebocoran tabung gas LPG dan bisa menimbulkan efek anaesthetic (hilang kesadaran), maka Bagaimana merancang dan membuat unit control berbasis mikrokontroller AT89S51 serta Bagaimana Penggunaan sensor yang digunakan (kalibrasi sensor). Jadi disini bertujuan untuk merancang dan membuat alat pemantau dan pengontrol kadar gas LPG dengan menggunakan mikrokontroller AT 89s51 sebagai basis kontrolnya.

Dengan metode penulisan secara dua metode yaitu memperoleh data dengan cara praktek secara langsung untuk menunjang pembuatan alat dan memperoleh data dengan cara membaca dan mempelajari buku literature yang berhubungan serta mengolah data dengan jalan membuat analisa dan menarik kesimpulan dari hasil pengujian yang ada.

Maka keluaran yang di hasilkan oleh TGS 2610 sudah sesuai dengan yang di harapkan,sehingga dapat diproses pengkondisi sinyal dan pada dasarnya alat ini daat bekerja dengan baik dan benar, namun masalah perbedaan tegangan dari hasil perhtungan dan pengukuran dapat di sebabkan oleh toleransi dari komponen yang digunakan.

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BAB I

PENDAHULUAN

1.1. Latar belakang

Telah kita ketahui semua bahwa kemajuan teknologi dewasa ini begitu cepat, dengan bertambah cepatnya kemajuan teknologi tersebut menjadikan kehidupan ini semakin baik, sebab semua teknologi tersebut diciptakan demi kemudahan dan kehidupan manusia yang lebih baik. Salah satu perkembangan teknologi adalah dibidang elektronika.

Supaya bisa dicairkan, propana dan buatana ditekan hingga 5 - 6 bar, volumenya pun menyusut hingga 200 kali lebih kecil di dalam tabung LPG. Keduanya tidak berbau, tak berwarna, dan amat mudah terbakar. Itu sebabnya LPG suka ditambahi pewangi dari senyawa sulfur, supaya keberadaan atau kebocorannya gampang dideteksi. Pernah pula diciptakan beragam aroma pewangi, termasuk efek bau durian, untuk gas tak beracun tapi bisa menimbulkan efek anaesthetic (hilang kesadaran). Karena sifatnya yang mudah terbakar, sering kita mendengar berita tentang kebakaran ruimah akibat kebocoran tabung gas LPG. *(http://www.departemenkesehatan_indonesia.co.id)*

Maka dari itulah didesain alat yang mampu mendeteksi serta melakukan pengamanan terhadap ruang yang ditengarai sebagai tempat penyimpanan tabung gas LPG. Selain itu, alat ini dilengkapi dengan indicator lampu dan buzzer sebagai tanda peringatan agar bisa melakukan langkah pengamanan lebih lanjut.

Dengan adanya alat ini diharapkan mampu nmengurangi tingkat kelalaian manusia dalam melakukan aktivitas pekerjaan dan juga mampu mengatasi berbagai masalah pemborosan yang kerap terjadi mengenai pemakaian gas LPG.

1.2. Rumusan masalah

Mengacu pada latar belakang diatas, maka rumusan masalah dapat dijabarkan sebagai berikut :

1. Bagaimana merancang dan membuat unit control berbasis mikrokontroller AT89S51.
2. Bagaimana Penggunaan sensor yang digunakan (kalibrasi sensor)

1.3. Tujuan

Adapun tujuan dari penulisan tugas akhir ini adalah merancang dan membuat alat pemantau dan pengontrol kadar gas LPG dengan menggunakan mikrokontroller AT 89s51 sebagai basis kontrolnya.

1.4. Batasan Masalah

Dalam penyususnan tugas akhir ini diperlukan batasan masalah agar tidak menyimpang dari ruang lingkup yang akan dibahas. Adapun batasan masalahnya adalah sebagai berikut :

1. Alat ini menggunakan sensor gas TGS 2610 yang mempunyai out put tegangan antara 0 – 4 volt.
2. Pengendalian dan pemantauan kadar gas menggunakan indicator lampu dan buzzer.

1. Alat ini menggunakan sensor gas TGS 2610 yang mempunyai out put tegangan antara 0 – 4 volt.
2. Pengendalian dan pemantauan kadar gas menggunakan indicator lampu dan buzzer.
3. Hanya membahas perangkat kerasnya, sedangkan perancangan perangkat lunaknya hanya dibahas secara garis besar.
4. Tidak membahas catu daya.Gas yang dikontrol hanya sebatas gas LPG.

1.5. Metodologi Penulisan

Metode yang digunakan dalam penulisan tugas akhir ini adalah :

1. Study Pustaka
2. Memperoleh data dengan cara membaca dan mempelajari buku literature yang ada hubungannya dengan penyusunan tugas akhir ini.
3. Studi Lapangan
4. Memperoleh data dengan cara praktek secara langsung untuk menunjang pembuatan alat.
5. Pengolahan Data

   Mengolah data dengan jalan membuat analisa dan menarik kesimpulan dari hasil pengujian yang ada.

1.6. Sistematika Pembahasan

Pada penulisan laporan tugas akhir ini ditulis sedemikian rupa sehingga diperoleh hubungan yang jelas antara bagian yang satu dengan yang lainnya.

Sistematika penulisan dari laporan ini adalah sebagai berikut :

BAB I PENDAHULUAN

Berisi latar belakang permasalahan, batasan masalah, metodologi dan sistematika penulisan.

BAB II TEORI PENUNJANG

Berisi landasan teori yang berhubungan dengan pembuatan alat.

BAB III PERANCANGAN DAN PEMBUATAN ALAT

Meliputi tentang penjelasan dan tata cara perencanaan dan pembuatan alat.

BAB IV PENGUJIAN ALAT

Meliputi proses pengujian alat yang terdiri dari peralatan yang digunakan, langkah kerja dan analisa hasil pengujian.

BAB V PENUTUP

Meliputi kesimpulan dan saran.

BAB II

LANDASAN TEORI

Landasan teori sangat membantu untuk dapat memahami suatu system. Disamping itu dapat juga dijadikan sebagai bahan acuan didalam merencanakan suatu sitem. Dengan pertimbangan hal-hal tersebut, maka landasan teori merupakan bagian yang harus dipahami untuk pembahasan selanjutnya.

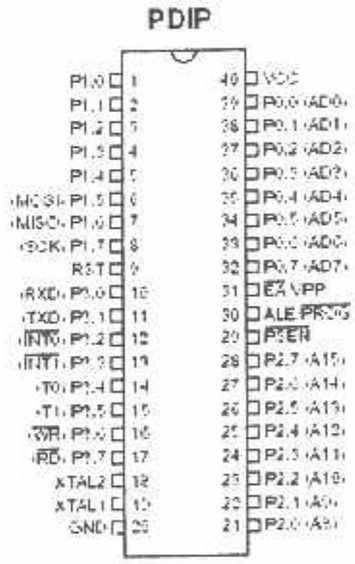
2.1. Umum

Pendeteksi kebocoran gas pada suatu ruangan ini direncanakan terdiri dari susunan perangkat penguat serta driver-driver yang digunakan untuk pengaturan on dan off. Pengendali ini menggunakan sebuah sensor yang sangat sensitive terhadap gas LPG dengan menggunakan sebuah op-amp. Sehingga untuk penempatan sensor harus diperhatikan betul agar alat dapat bekerja dengan sempurna.

2.2. Mikrokontroller AT89s51

Mikrokontroler AT89s51 merupakan salah satu anggota keluarga dari MCS-51. yaitu suatu komponen produksi ATMEL yang berorientasi control (mikrokontroller). Intel mengklarifikasikan dalam kelompok embedded mikrokontroler, yang artinya adalah mikrokontroller yang dapat diprogram ulang (reprogrammable). Didalam chip mikrokontroler AT89s51 ini sudah tersedia berbagai macam peralatan pendukung mikroprosesor seperti RAM, serial port, bus-bus data pendukung. Spesifikasi perangkat keras dari mikrokontroler AT89s51 adalah sebagai berikut :

- CPU (Central Prosessing Unit) dengan lebar data 8 bit.
- Prosesor Boolean untuk operasi logika 1 bit.
- Pembangkit *clock* internal.
- Tiga buah *timer/counter 16 bit.*
- Dua buah saluran interupsi eksternal.
- Jalan I/O dua arah (*bidirection*) 32 buah.
- Memori program terpisah dari memori data.
- Memori data internal 128 byte.
- Alamat memori program eksternal 64 kilobyte.
- Alamat memori data eksternal 64 kilobyte.
- Memori program internal sebesar 8 kilobyte.



Gambar 2.1. Konfigurasi Mikrokontroller AT89S51

Sumber: Data sheet Mikrokontroller AT89S51

Berikut ini adalah penjelasan dari masing-masing pin mikrokontroller AT89s51:

- Pin 1 sampai 8

  Port 1 : Merupakan 8-*bit* saluran masukan atau keluaran dua arah, setiap saluran mampu melayani 4 masukan.

- Pin 9

  RST : Merupakan masukan reset. Logika high yang akan membuat mikrokontroller AT89S51 menjalani test rutin.

- Pin 10 sampai 17

  Port 3 : Port 3 terdiri dari 8 saluran masukan atau keluaran dua arah. Setiap salurannya mampu melayani 4 masukan. Selain sebagai port masukan atau keluaran, port 3 juga mempunyai fungsi-fungsi khusus yang dimiliki oleh keluarga MCS-51.

- Pin18 dan 19

  X1 (XTAL 1) dan X2 (XTAL2) : jika dikonfigurasikan bersama sebuah kristal akan membentuk rangkaian osilator on-chip pada mikrokontroller.

- Pin 20 sampai 27

  Port2 : Port 2 terdiri dari 8 saluran masukan dan keluaran dua arah. Setiap salurannya mampu melayani 4 masukan. Port 2 mengeluarkan alamat bagian high (A8-A15), selama pengambilan instruksi dari memori program eksternal dan pengambilan data dari memori data eksternal yang menggunakan mode pengalamatan 16-bit.

- Pin 29

  PSEN : *Program Store Enable* merupakan sinyal baca yang mengeksekusi memori program eksternal.

- Pin 30

  ALE/PROG : Address Latch Enable merupakan pulsa yang berfungsi menahan alamat rendah (A0 –A7) pada port 0, selama dilakukan proses baca dan tulis memori eksternal. Pin ini juga berfungsi sebagai masukan pulsa program (PROG), selama dilakukan pemrograman pada *EEPROM eksternal.*

- Pin 31

  EA/VP : *Eksternal Acces.* EA dihubungkan dengan vss untuk memungkinkan pengambilan instruksi pada memori program eksternal yang berlokasi 0000H sampai FFFFH. Jika diinginkan menggunakan program internal, maka EA dihubungkan VCC.

- Pin 32 sampai 39

  Port 0 : Port 0 terdiri dari 8 saluran masukan dan keluaran dua arah. Setiap saluran mampu melayani 8 masukan. Port 0 merupakan saluran alamat bagian low (A0-A7), yang dimultipleks dengan saluran bus data (D0-D7), yang digunakan pada saat mengakses memori data eksternal dan memori program eksternal.

- Pin 40

  VCC : Merupakan masukan catu daya 5 volt, dengan toleransi kurang lebih 10 µs.

Tabel 2-1. Keluarga MCS 51

Type	Tipe tanpa EPROM	tipe ber EPROM	Kapasitas ROM	Kapasitas RAM	Port I/O	Pewaktu
8031	8031	-	4K	128	4	2
8051AH	8031AH	8751H	4K	128	4	2
8052AH	8032AH	8752BH	8K	256	4	3
80C52BH	80C31BH	87C51	4K	128	4	2
80C52	80C32	-	8K	256	4	3
83C51FA	80C51BH	87C51FA	8K	256	4	3
83C51FB	80C51FB	87C51FB	16K	256	4	3
83C152	80C152	-	8K	256	5	3
89S52	-	89S52	8K	256	4	3

Sumber: Data sheet Mikrokontroller AT89S51:12

Keluarga MCS-51 yang diproduksi Intel mempunyai konfigurasi yang berbeda – beda sesuai dengan jenisnya. Masing- masing jenis saling kompatibel serta mempunyai kelebihan tersendiri. Misalnya mikrokontroller AT89S51 merupakan padanan dari Mikrokontroller 8051. Tabel tersebut memperlihatkan sebagian dari keluarga MCS-51.

2.2.1. Organisasi Memori

Organisasi memori pada mikrokontroler AT89s51dapat dibagi menjadi dua bagian besar yaitu memori program dan memori data. Pembagian tersebut didasarkan atas fungsi dari penyimpanan data maupun program. Memori program digunakan untuk menyimpan instruksi-intruksi yang akan dijalankan oleh mikrokontroller, sedangkan memori data digunakan sebagai tempat penyimpanan data yang sedang diolah mikrokontroller.

Program mikrontroller disimpan dalam memori program berupa ROM. Mikrokontroller AT89s51 dilengkapi dengan ROM internal namun untuk program yang besar digunakan ROM eksternal yang terpisah dari mikrokontroller. Untuk dapat

menggunakan memori program eksternal ini penyemat / EA dihubungkan dengan penyemat Vss (logika 0).

Memori program mikrokontroller menggunakan alamat 16 bit mulai 0000_H-$FFFF_H$, sehingga kapasitas penyimpanan program maksimal adalah 2^{16} *byte* atau 64 Kb. Sinyal yang digunakan untuk membaca memori program eksternal adalah sinyal/PSEN (Program Store Enable).

Selain memori program mikrokontroler AT89s51 juga memiliki memori data internal berkapasitas 128 *byte* dan mampu mengakses memori data eksternal sebesar 64 Kb. Semua memori data internal dapat dialamati dengan pengalamatan langsung atau tidak langsung. Ciri dari pengalamatan langsung adalah *operand* berisi alamat data yang diolah. Sedangkan ciri dari pengalamatan tidak langsung adalah operand alamat register yang berisi alamat data yang akan diolah. Sebagian memori tersebut dapat dialamati dengan pengalamatan register, dan sebagian lagi dapat dialamati dengan memori satu bit. Untuk membaca data digunakan sinyal / RD, sedangkan untuk menulis data digunakan sinyal / WR.

2.2.2. Registrasi Fungsi Khusus

Register fungsi khusus (*Special Function Register*) terletak pada 128 *byte* bagian atas memori data internal dan berisi *register-register* untuk pelayanan *latch port, timer, program status words, control peripheral* dan sebagainya. Alamat register fungsi khusus ditunjukkan pada table 2-2.

Register-register ini hanya dapat diakses dengan pengalamatan langsung. Enam belas alamat pada register fungsi khusus dapat dialamati per-bit maupun per-byte dan

terletak pada alamat 80_H-FF_H. Secara perangkat keras, register fungsi khusus ini dibedakan dengan memori data internal.

Tabel 2-2. Nama dan Alamat Register pada Register Fungsi Khusus

Simbol	Nama Register	Nilai pada saat reset	Alamat
ACC	Accumulator	0000H	0E0H
B	Register B	00H	0F0H
PSW	Program Status Word	00H	0D0H
SP	Stack Pointer	07H	81H
DPTR	Data Pointer 2 byte	–	–
DPL	Low bytes	0000H	82H
DPH	High bytes	0000H	83H
P0	Port 0	FFH	80H
P1	Port 1	FFH	90H
P2	Port 2	FFH	0A0H
P3	Port 3	FFH	0B0H
IP	Interupt Priority control	XXX00000B	0B8H
IE	Interupt Enable control	0XX00000B	0A8H
TMOD	Timer/counter Mode control	00H	89H
TCON	Timer/counter control	00H	88H
TH0	Timer/counter 0 high byte	00H	8CH
TL0	Timer/counter 0 low byte	00H	8AH
TH1	Timer/counter 1 high byte	00H	8DH
TL1	Timer/counter 1 low byte	00H	8BH
SCON	Serial Control	00H	9BH
SBUF	Serial Data Buffer	Independen	99H
PCON	Power Control	HMOS 0XXXXXXXB CHMOS 0XXX0000B	87H

Sumber: Data sheet Mikrokontroller AT89S51

Beberapa macam register fungsi khusus yang sering digunakan, dijelaskan sebagai berikut:

- *Accumulator* (ACC) merupakan *register* untuk penambahan dan pengurangan. Perintah *Mnemonic* untuk mengakses akumulator disederhanakan sebagai A.
- *Register* B merupakan *register* khusus yang berfungsi melayani operasi perkalian dan pembagian.

- *Program Status Word* (PSW) terdiri dari beberapa *bit* status yang menggambarkan kejadian di akumulator sebelumnya. Yaitu *carry bit, auxiliary carry,* dua *bit* pemilih bank, bendera *overflow, parity bit,* dan dua bendera yang dapat didefinisikan sendiri oleh pemakai.
- *Stack Pointer* (SP) merupakan *register* 8 bit yang dapat diletakkan di alamat manapun pada RAM internal. Isi *register* ini ditambah sebelum disimpan, selama instruksi *PUSH* dan *CALL.* Pada saat *reset, register* SP diinisialisasikan pada alamat 07_H, sehingga stack akan dimulai pada lokasi 08_H.
- *Data Pointer* (DPTR) terdiri dari dua *register,* yaitu untuk *byte* tinggi (*Data Pointer High,* DPH) dan *byte* rendah (*Data Pointer Low,* DPL) yang berfungsi untuk mengunci alamat 16 *bit.*
- *Port 0* sampai *port3* merupakan *register* yang berfungsi untuk membaca dan mengeluarkan data pada *port* 0, 1, 2, 3. Masing-masing register ini dapat dialamati per-*byte* maupun per-*bit.*
- *Serial Data Buffer* (SBUF) merupakan dua *register* yang terpisah, *register buffer* pengirim dan sebuah *register penerima.* Meletakkan data pada SBUF berarti meletakkan pada *buffer* pengirim yang akan mengirimkan data dari *buffer penerima.*
- *Control Register* terdiri dari *register* yang mempunyai fungsi kontrol. Untuk mengontrol system interupsi, terdapat dua register khusus, yaitu register IP (*interrupt priority*) dan register IE (*interrupt enable*). Untuk mengontrol pelayanan timer counter terdapat register khusus, yaitu register TCON (*Timer*

Counter Control) serta untuk pelayanan port serial menggunakan register SCON (*Serial Port Control*).

2.2.3. Port Masukan dan Keluaran

Mikrokontroller AT89s51 mempunyai 4 port dan masing-masing port terdiri dari 8 saluran *bit*. Ke empat port ini bersifat bi-directional yaitu dapat digunakan sebagai masukan atau keluaran.

Port 0 digunakan sebagai saluran data yang di multipleks dengan saluran alamat rendah untuk mengakses memori eksternal, baik memori program maupun memori data. Port 2 mengeluarkan bagian alamat high untuk mode pengalamatan memori 16 bit. Port 1 dan 3 berfungsi sebagai saluran masukan dan keluaran multi fungsi. Jika dibutuhkan port 3 mempunyai fungsi khusus seperti ditunjukkan pada table berikut :

Tabel 2.3. Fungsi khusus port 3

Nama Penyemat	Fungsi Khusus
Port 3,0	RXD (port masukan serial)
Port 3,1	TXD (port keluaran serial)
Port 3,2	/INT0 (masukan interupsi eksternal 0)
Port 3.3	/INT1 (masukan interupsi)
Port 3.4	T0 (masukan pewaktu eksternal 0)
Port 3.5	T1 (masukan pewaktu eksternal 1)
Port 3.6	/WR (sinyal tulis memori data eksternal)
Port 3.7	/RD (sinyal baca memori data eksternal)

2.2.4. System Interupsi

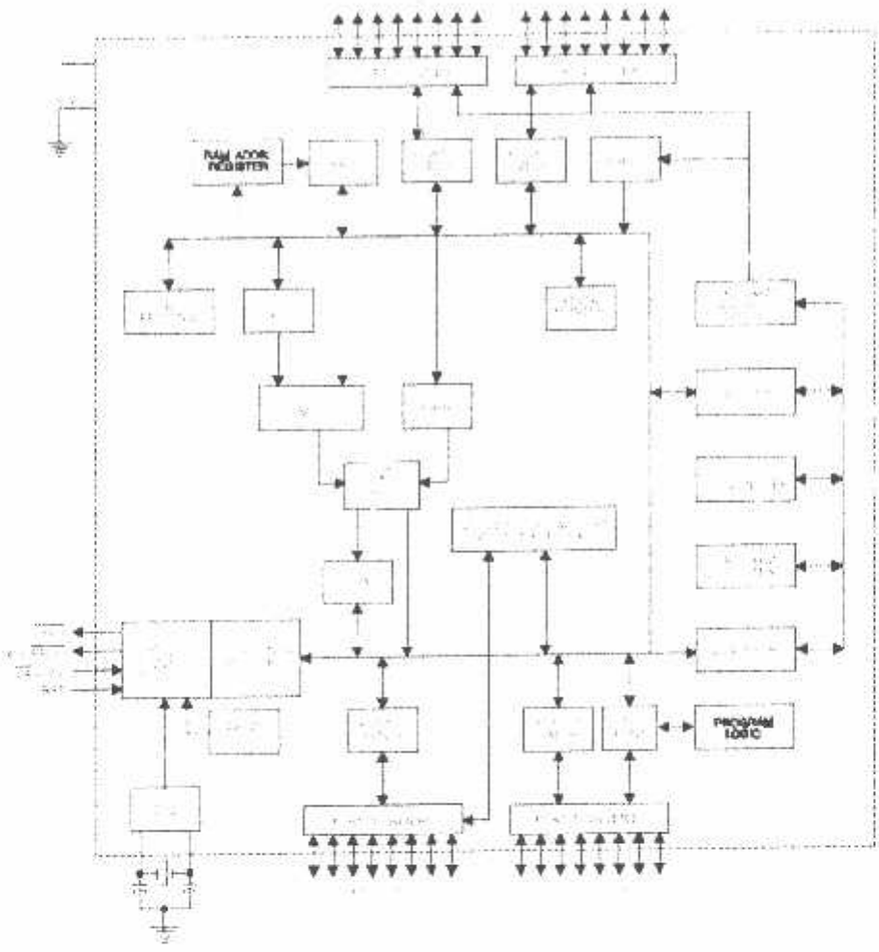
Mikrokontroler AT89s51 mempunyai dua sumber interupsi eksternal dan sumber interupsi internal yang dapat diprogram agar sensitive terhadap perubahan level atau transisi. Interupsi timer aktif saat register timer yang bersangkutan mengalami *rollover*. Interupsi serial akan aktif pada saat mikrokontroler mengirimkan/menerima data. Setiap sumber interupsi dapat diaktifkan/dimatikan melalui perangkat lunak.

Tabel 2.4. Tingkatan prioritas interupsi

Prioritas Interupsi	Sumber Interupsi	Alamat Vektor
1	IE0 (Interupsi eksternal 0)	0003H
2	TF0 (Timer overflow flag 0)	000BH
3	IE1 (Interupsi eksternal 1)	0013H
4	TF1 (Timer overflow flag 1)	001BH
5	R1 dan T1	0023H
6	TF2 dan EXF2	002BH

Hirarki tingkatan prioritas interupsi dapat dilihat dalam table diatas. Interupsi yang mempunyai tingkatan prioritas lebih tinggi tidak dapat diinterupsi oleh yang lebih rendah. Meskipun demikian melalui perangkat lunak hirarki tersebut dapat diubah, yaitu dalam register *interrupt priority* (IP).

Block Diagram



Gambar 2.2. Blok Diagram Mikrokontroller AT89S51

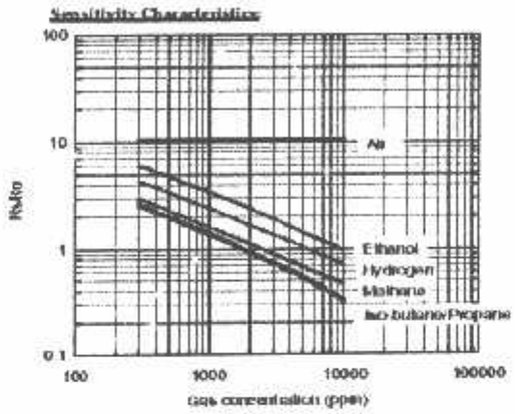
Sumber: Data sheet Mikrokontroller AT89S51:3

2.3. Sensor Gas

Sensor gas merupakan suatu komponen yang mudah untuk mengalami perubahan tegangan dan arus, apabila terjadi perubahan konsentrasi gas pada suatu kondisi tertentu. Sensor gas yang dipakai adalah TGS2610 yang nilai hambatannya

berubah terhadap perubahan konsentrasi gas. Tegangan out put pada TGS2610 adalah sebanding dengan konsentrasi gas serta menghasilkan kenaikan tegangan sekitar 0,2 volt pada setiap kenaikan 0,2%gas.

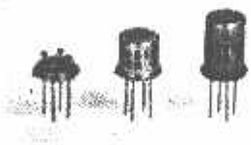
Perbandingan hambatan yang dihasilkan terhadap konsentrasi gas ditunjukan pada grafik berikut :

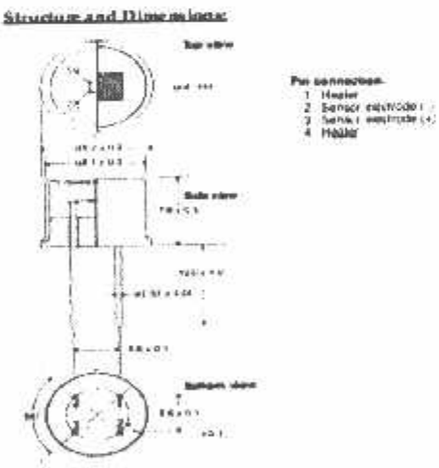


Grafik 2.1. Perbandingan tahanan dengan konsentrasi gas

Sumber: *www.google.com* (Gas)

Beberapa jenis TGS 2610 antara lain : TGS 2610 JOO dan TGS 2610 BOO



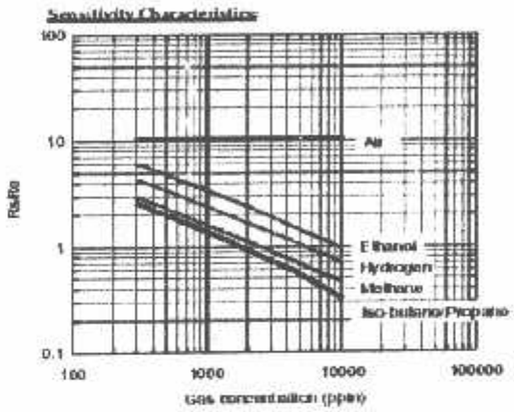


Gambar 2.3. Konfigurasi Pin TGS 2610

Sumber: www.google.com (Gas)

berubah terhadap perubahan konsentrasi gas. Tegangan out put pada TGS2610 adalah sebanding dengan konsentrasi gas serta menghasilkan kenaikan tegangan sekitar 0,2 volt pada setiap kenaikan 0,2%gas.

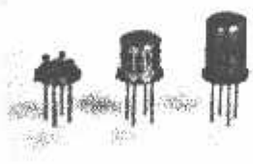
Perbandingan hambatan yang dihasilkan terhadap konsentrasi gas ditunjukan pada grafik berikut :

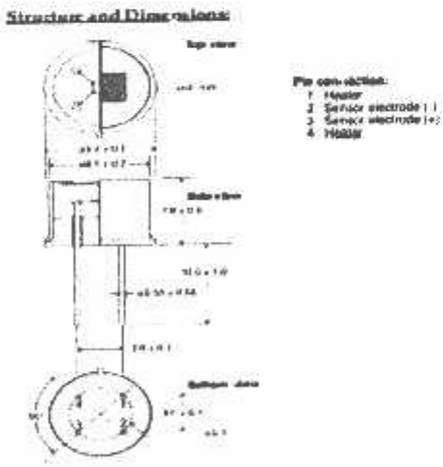


Grafik 2.1. Perbandingan tahanan dengan konsentrasi gas

Sumber: *www.google.com* (Gas)

Beberapa jenis TGS 2610 antara lain : TGS 2610 JOO dan TGS 2610 BOO





Gambar 2.3. Konfigurasi Pin TGS 2610

Sumber: www.google.com (Gas)

Adapun karakteristik umum dari TGS 2610 adalah sebagai berikut :

1. Setiap kenaikan gas 0.2 %, maka V out akan bertambah 0.2 V
2. Dapat ditampilkan langsung dalam % gas.
3. Jangkauan gas yang dapat diukur adalah 0-6 %.

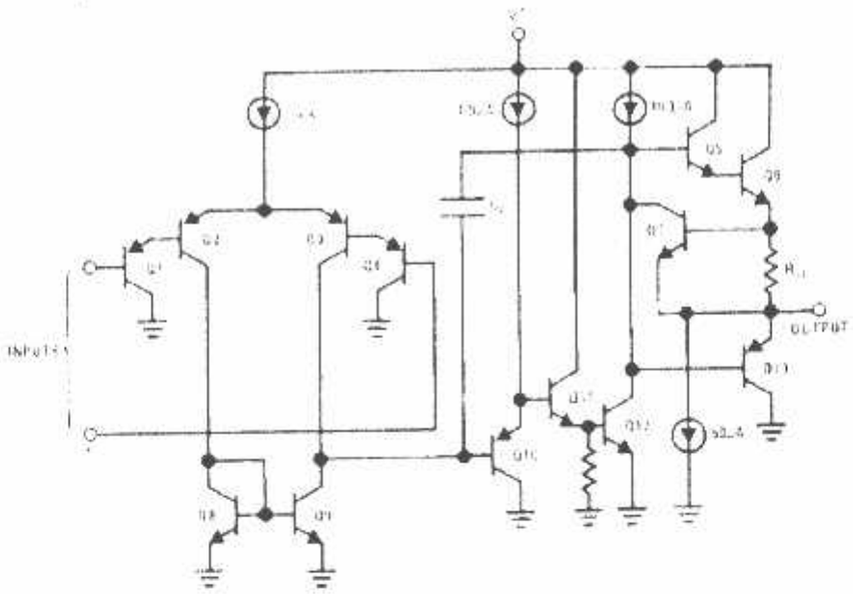
2.4. Operasional Amplifier (OP-Amp)

2.4.1. Sekilas Tentang Op-Amp

Operasional amplifier adalah penguat gain tinggi yang dirancang untuk melaksanakan tugas-tugas matematis seperti penjumlahan, pengurangan, perkalian, dan pembagian. Pada saat ini Op-Amp rangkaian terpadu linier dapat bekerja dengan tegangan yang rendah dan dengan hasil yang tidak kalah baiknya dengan pendahulunya. Dengan harga yang relatif murah dan mudah diganti-ganti serta sifatnya yang dapat di andalkan, maka tidak heran kalau setiap tahunnya berjuta-juta Op-Amp digunakan. Dari kelebihan yang dimiliki Op-Amp telah memperluas penggunaan Op-Amp sampai jauh melampaui kegunaannya saat pertama dirancang. Beberapa penggunaan Op-Amp adalah di bidang pengendalian proses, komunikasi, komputer, sumberdaya dan isyarat, system peraga dan system pengukuran atau system pengujian.

Pada Op-Amp mempunyai lima terminal dasar yang terbagi dalam dua untuk mensuplay daya, dua untuk isarat masukan, dan satu untuk keluarannya. Bagian dalam dari Op-Amp itu sendiri rumit, gambar sekematik dari Op-Amp dapat dilihat dalam gambar 2-4. Untuk dapat menggunakan Op-Amp, tidak perlu mengetahui hal apapun tentang cara kerja bagian dalam dari Op-Amp, karena Op-Amp telah dirancang

sedemikian rupa sehingga komponen luarlah yang akan menentukan kegunaan dari Op-Amp

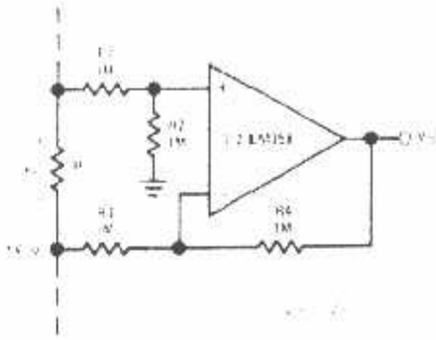


Gambar 2.4 . Skematik OP-Amp

Sumber: Data Sheet Op-Amp:16

2.4.2. Op-Amp Sebagai Penguat Differensial Dasar

Sebuah Op-Amp, tiga tahanan yang sama, dan sebuah tranduser membentuk suatu penguat jembatan dasar. Dalam hal ini tranduser merupakan alat yang merubah perubahan arus listrik menjadi tegangan. Sifat penguat ini memungkinkan suatu sinyal kecil di ambil dari sinyal yang lebih besar dengan rangkaian yang di tujukan pada gambar 2.5. sinyal yang kecil merupakan masukan diferensial dan keluarannya berupa tegangan masukan diferensial yang diperkuat.



Gambar 2.5. Rangkaian Penguat Differensial Dasar

Sumber: Data Sheet Op-Amp:12

2.5. Analog to Digital Converter

Untuk mengubah data analog dari keluaran sensor induksi menjadi data digital agar dapat di olah program mikrokontroler maka diperlukan perangkat ADC. ADC yang dipergunakan adalah ADC0804 yang mempunyai resolusi 8 bit dan mempunyai 8 jalur output satu jalur input serta mempunyai clock internal dengan cara menghubungkan tahanan luar dan sebuah capasitor pada clock out dan clock in dan ground.

$$F\ clock = 1/1.1 \times R.c$$

Tegangan referenci yang digunakan pada ADC ini untuk menentukan besarnya resolusi yang diinginkan, adalah:

$$\text{Resolusi maksimal} = 2^n - 1$$

$$= 2^8 - 1$$

$$= 256 - 1$$

$$= 255$$

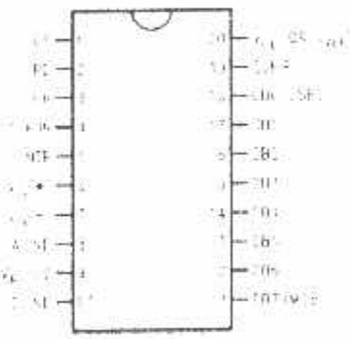
Dengan tegangan referensi 2.5 volt maka resolusi perpindahan tiap bitnya adalah:

Resolusi =Vref/2^n-1

=2.5/255

=0.009 volt

Tegangan yang dapat diterima oleh ADC 0804 ini berkisar antara 0-5 volt. Tegangan masukan ini diperoleh dari output penguat yang nantinya akan dikonversi menjadi biner untuk dioleh pada Mikrokontroler.



Gambar 2.6. Analog to Digital Converter 0804

Sumber: Data Shee ADC 0804:32

BAB III

PERANCANGAN DAN PEMBUATAN ALAT

3.1 Pendahuluan

Pada pembuatan alat ini, digunakan sebuah mikrokontroller. Prosentase kadar gas diterjemahkan oleh sensor menghasilkan level tegangan yang berubah-ubah. Dengan level tegangan yang masih linear dibutuhkan sebuah converter agar mikrokontroller dapat mengolah tegangan yang linear tersebut menjadi bentuk digital agar dapat dibaca. ADC adalah alat yang berfungsi menerjemahkan level tegangan yang linear tersebut menjadi data digital 8 bit.

Data kadar gas dari ADC dimasukkan ke mikrokontroller yang akan menerjemahkan data tersebut. Setelah data diolah, mikrokontroller akan memberi tampilan berupa 2 buah lampu indicator dan sebuah buzzer sebagai tanda bahaya.

3.2. Prinsip Kerja

Perancangan dan pembuatan alat ini dibagi menjadi empat bagian yaitu :

a. Perancangan dan pembuatan mikrokontroller

b. Perancangan dan pembuatan sensor dan op-amp

c. Perancangan dan pembuatan driver indicator

d. Perancangan dan pembuatan software

3.3. Perancangan Alat

3.3.1. Perancangan dan pembuatan alat sisi sensor

Untuk mendeteksi kadar gas pada ruangan secara keseluruhan harus diperhatikan secara detail. Misalnya untuk peletakan sensor gas tidak boleh terlalu dekat dan tdak boleh terlalu jauh dari tabung gas. Hal ini dapat mengakibatkan perubahan tegangan yang berubah-ubah secara drastic.

Sensor gas disini menggunakan TGS 2610 case TO-5 metal can yang mempunyai kadar kerja mulai 0-6% kadar gas LPG. Dengan spesifikasi kadar gas diatas maka diharapkan mampu mendeteksi perubahan kadar gas dalam ruangan. Alat ini akan terpasang pada ruang-ruang yang ditengarai sebagai tempat penyimpanan/penempatan tabung gas LPG.

3.3.3.1. Penguat Penyangga

Penguat penyangga merupakan penguat yang kegunaannya untuk penguatan tanpa pembalikan fasa. Artinya sinyal output penguat, sefasa dengan sinyal input penguat yang diberikan. Seperti ditunjukkan dalam Gambar 3.3 bahwa tahanan umpan baliknya tidak ada sehingga seluruh tegangan keluaran akan diumpan balikkan ke masukan. Penguat tegangan dari penguat penyangga ini sama dengan satu, dimana :

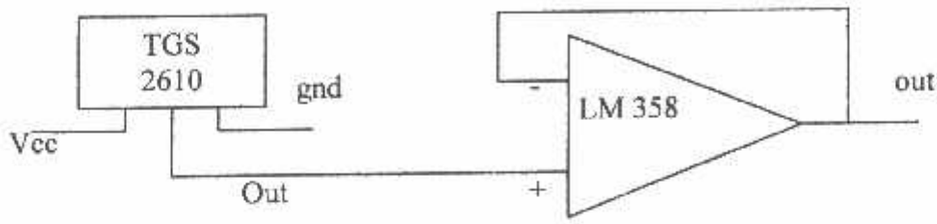
$$A = Vo/Vi = 1 \quad \ldots\ldots(1)$$

Vi = Tegangan masukan

Vo : Tegangan keluaran

Oleh karena itu penguat penyangga disebut juga dengan pengikut tegangan keluaran. Penguat mengikuti tegangan masukan baik besarnya maupun fasanya.

Penguat penyangga ini digunakan untuk mengisolasi suatu tingkat penguat dari penguat berikutnya agar tidak terbebani. Selain itu penguat penyangga juga dipakai untuk penyesuaian impedansi yang biasanya mempunyai impedansi input yang tinggi dan impedansi output yang rendah.

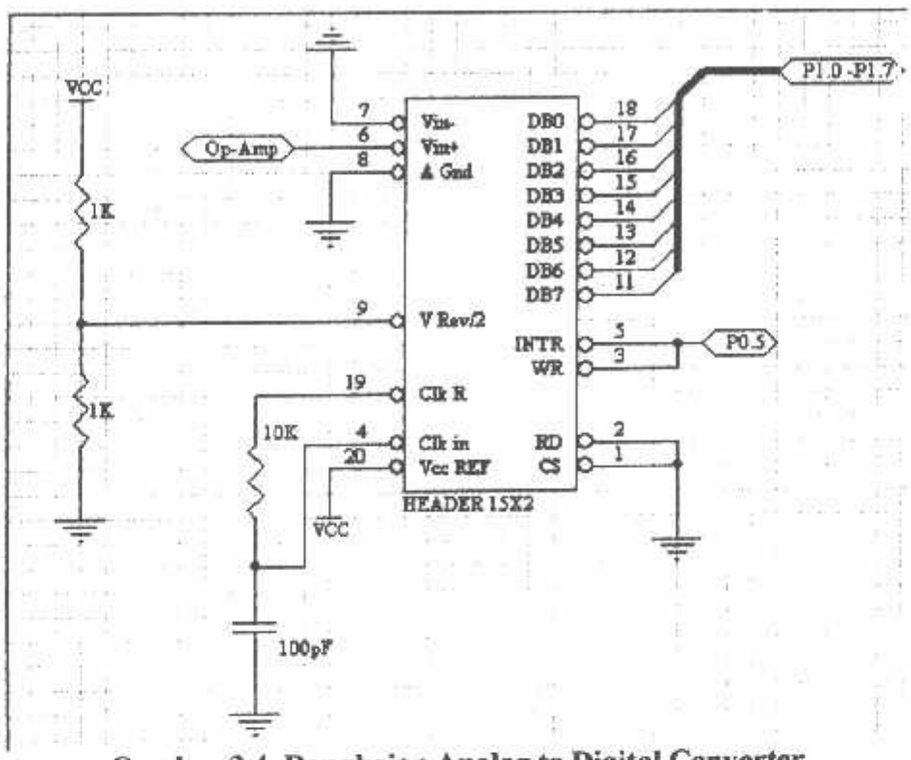


Gambar 3.3. Rangkaian Sensor dan Pengkondisi Sinyal

Sumber: Perencanaan

3.3.1.2. Pengubah Analog ke Digital ADC 0804

Pengubah analog ke digital(*Analog to digital converter /ADC)* mengubah sinyal analog (kontinyu) ke bentuk sinyal digital dengan pendekatan sesuai jumlah digit yang digunakan. Pada prinsipnya ADC adalah mengukur sinyal analog dan mengubahnya menjadi bilangan biner. Beberapa teknik pengubah telah diciptakan untuk pengubahan analog ke digital. Masing-masing mempunyai kelebihan dan kekurangan parameter utama yang dipakai untuk menilai keunggulan tiap teknik biasanya adalah kecepatan, harga dan kecepatan. Yang mana dalam rangkaian tersebut terdapat pin-pin yang mempunyai fungsi masing-masing.



Gambar 3.4. Rangkaian Analog to Digital Converter
Sumber: Perencanaan

Pin 11 sampai 18 adalah keluaran digital. Apabila pin CS dan RD tidak aktif, keluaran digital akan berlogika tinggi. Sedangkan bila CS dan RD diberi logika rendah, akan menghasilkan keluaran.

Pin WR bila dibuat aktif bersamaan CS akan memulai konversi. Bila WR=0 konversi akan direset. Setelah WR berubah ke 1 konversi langsung dimulai. Pin 4 merupakan sinyal clock masukan. Clock ini dapat berupa eksternal, atau internal dengan menambahkan rangkaian RC antara CLK *in* dan CLK *out*.

V in (+) dan Vin (-) adalah sinyal masukan differsial. Jika Vin (+) dihubungkan ke ground, Vin (-) digunakan untuk masukan negative. Sedangkan jika Vin (-) yang dihubungkan ke ground, Vin (+) dihubungkan ke masukan positif.

Pin 9 adalah tegangan referensi maksimum sinyal analog. Bila sinyal ini tidak dihubungkan, tegangan referensinya sama dengan Vcc. Jika ingin menggunakan tegangan maksimum yang berbeda dengan Vcc, pin ini dihubungkan dengan tegangan ½ kali tegangan maksimum yang diinginkan.

Pin 5 (INTR) akan menunjukkan bahwa konversi telah selesai. Ketika dimulai konversi INTR akan mengeluarkan logika tinggi. Jika konversi selesai INTR akan mengeluarkan logika rendah.

Untuk mengetahui resolusi ADC 0804 maka digunakan rumus :

$$\text{Resolusi} = \frac{\text{Vref} / 2}{2^n - 1}$$

Vref = 5Volt

Vref/2 =2,5 Volt

$$\text{Resolusi} = \frac{5}{256-1} = \frac{5}{255} = 0{,}0196$$

$$\text{Vout ADC} = \frac{\text{Vin}}{\text{Res}}$$

Untuk V input 5volt maka Vout ADC sama dengan

$$\text{Vout ADC} = \frac{5}{0{,}02} = 250$$

$$2\frac{250}{} = 0$$

$$2\frac{125}{} = 1$$

$$2\frac{62}{} = 0$$

$$2\frac{31}{} = 1$$

$$2\frac{15}{} = 1$$

$$2 \overline{)\ 7} = 1$$

$$2 \overline{)\ 3} = 1$$

$$1$$

Output ADC = 11111010

= FAh

Untuk output ADC dengan Vin lainnya dapat dilihat pada table berikut ini:

Tabel 3.1. Tabel Konversi Data Op-Amp Diferensial ke Biner

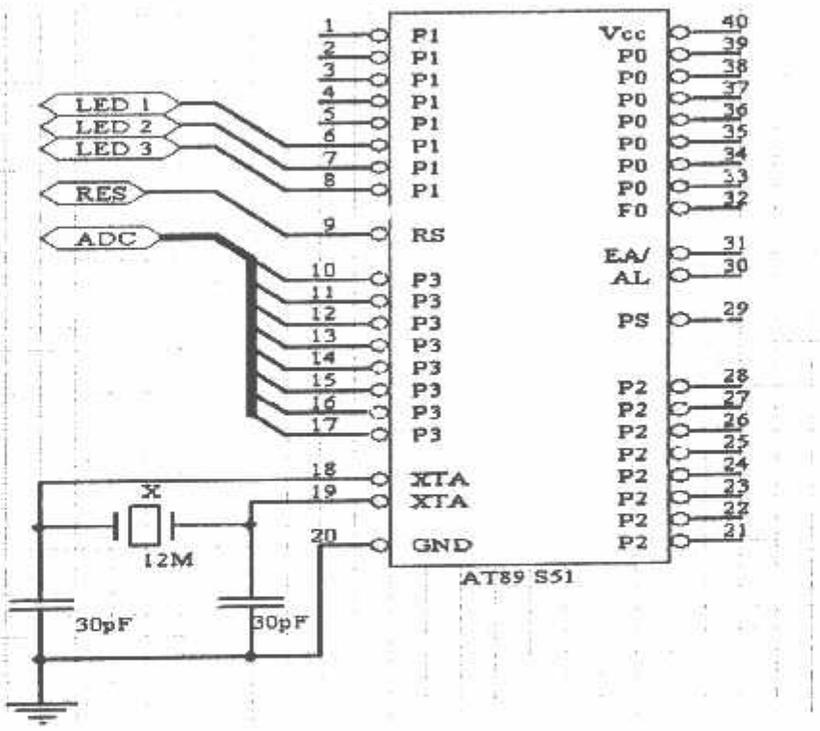
Tabel Perhitungan Kadar gas											
Gas %	TGS 2610 Volt	Buffer Volt	ADC								Data Hexa
			D0	D1	D2	D3	D4	D5	D6	D7	
0	0	0	0	0	0	0	0	0	0	0	00 H
0.2	0.2	0.2	0	0	0	0	1	0	1	0	0A H
0.4	0.4	0.4	0	0	0	1	0	1	0	0	14 H
0.6	0.6	0.6	0	0	0	1	1	1	1	0	1E H
0.8	0.8	0.8	0	0	1	0	1	0	0	0	28 H
1	1	1	0	0	1	1	0	0	1	0	32 H
1.2	1.2	1.2	0	0	1	1	1	1	0	0	3C H
1.4	1.4	1.4	0	1	0	0	0	1	1	0	46 H
1.6	1.6	1.6	0	1	0	1	0	0	0	0	50 H
1.8	1.8	1.8	0	1	0	1	1	0	1	0	5A H
2	2	2	0	1	1	0	0	1	0	0	64 H
2.2	2.2	2.2	0	1	1	0	1	1	1	0	6E H
2.4	2.4	2.4	0	1	1	1	1	0	0	0	78 H
2.6	2.6	2.6	1	0	0	0	0	0	1	0	82 H
2.8	2.8	2.8	1	0	0	0	1	1	0	0	8C H
3	3	3	1	0	0	1	0	1	1	0	96 H
3.2	3.2	3.2	1	0	1	0	0	0	0	0	A0 H
3.4	3.4	3.4	1	0	1	0	1	0	1	0	AA H
3.6	3.6	3.6	1	0	1	1	0	1	0	0	B4 H
3.8	3.8	3.8	1	0	1	1	1	1	1	0	BE H
4	4	4	1	1	0	0	1	0	0	0	C8 H
4.2	4.2	4.2	1	1	0	1	0	0	1	0	D2 H
4.4	4.4	4.4	1	1	0	1	1	1	0	0	DC H
4.6	4.6	4.6	1	1	1	0	0	1	1	0	E6 H
4.8	4.8	4.8	1	1	1	1	0	0	0	0	F0 H
5	5	5	1	1	1	1	1	1	1	1	FF H

Mikrokontroller AT89S51 dirancang untuk dapat berdiri sendiri karena terdapat EEPROM, RAM serta port input/output dan perlengkapan lainnya dengan tujuan menambah kemudahan dalam aplikasinya dan juga dalam softwarenya.

Mikrokontroller yang digunakan pada system adalah mikrokontroller jenis AT89S51 yang merupakan IC CMOS 8bit internal RAM, 40 pin dan 3 port *I/O*.

3.3.2. Perancangan Mikrokontroller Sisi Sensor

Dalam perancangan system ini pin-pin yang digunakan adalah sebagai berikut :



Gambar 3.5. Skematik Mikrokontroller

Sumber: Perencanaan

Keterangan Pin:

1. Pin 6 (P1.5) sampai dengan Pin 8 (P1.7) adalah jalur driver indicator
2. Pin 10 – 17 (P3.0 – P 3.7) adalah jalur data dari ADC
3. Pin 9 untuk jalur reset

4. Pin 18 (Xtal 2) untuk clock pada Mikrokontroller AT 89S51

5. Pin 19 (Xtal 1) untuk clock pada Mikrokontroller AT 89S51

6. Pin 20 (GND) Untuk Vss pada Mikrokontroller AT89S51

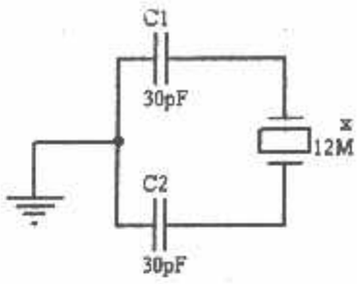
7. Pin 40 (Vcc) berfungsi sebagai Vcc 5 Volt

3.3.3.1. Rangkaian Clock Minimum Sistem

Kecepatan proses pengolahan data pada mikrokontroller ditentukan oleh clock (pewaktu) yang dikendalikan oleh mikrokontroller tersebut. Pada mikrokontroller AT89S51 terdapat internal clock. Internal clock generator berfungsi sebagai sumber clock, tapi masih memerlukan rangkaian tambahan untuk membangkitkan clock yang diperlukan. Rangkaian clock ini terdiri dari dua buah capasitor dan sebuah kristal yang dirangkai sedemikian rupa dan kemudian dihubungkan dengan pin 18 dan 19 pada AT 89S51.

Dalam perancangan rangkaian ini menggunakan :

1. C=30 pF. Penentuan besarnya kapasitansi disesuaikan dengan spesifikasi pada data sheet AT 89S51.
2. Kristal 12 MHz (berdasarkan data sheet AT 89S51), adapun gambar rangkaian clock tampak seperti pada gambar 3.7.



Gambar 3.7. Rangkaian Clock
Sumber: Perencanaan

Dengan menggunakan kristal diatas maka dapat dihitung waktu yang diperlukan untuk satu siklus mesin.

F = 12 MHz

Sehingga T = 1/f

T = 1/ 12 *MHz* = 1/12 µs

Maka untuk satu siklus mesin dari mikrokontroller besarnya adalah :

Time = 12 x T

Time = 12 x 1/12 µs

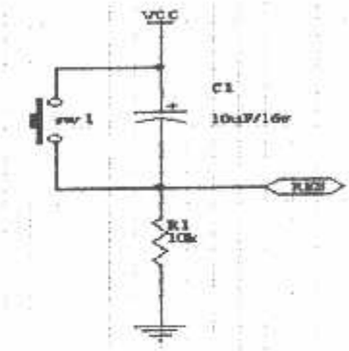
Time = 1 µs

Mikrokontroller memiliki oscillator internal (*On Chip Oscilator*) yang dapat digunakan sebagai clock bagi CPU. Untuk menggukan oscillator internal diperlukan sebuah kristal atau resonator keramik antara pin X'tal 1 dan X'tal 2 dan sebuah capasitor ke ground.

Untuk kristalnya dapat digunakan frekuensi dari 6 sampai 12 MHz. Sedangkan kapasitor bernilai antara 27 pF sampai 33 pF.

3.3.3.2. Rangkaian Reset

Reset pada mikrokontroller merupakan masukan aktif High ' 1 '. Pulsa transisi dari rendah ' 0 ' ke tinggi " 1 ' akan mereset mikrokontroller menuju alamat 0000H. Pin Reset dihubungkan dengan rangkaian power on reset seperti pada gambar 3-4.



Gambar 3.8. Rangkaian Reset

Sumber: Perencanaan

Rangkaian reset bertujuan agar mikrokontroller dapat menjalankan proses dari awal. Rangkaian reset untuk mikrokontroller dirancang agar mempunyai kemampuan power on reset, yaitu reset yang terjadi pada saat system dinyalakan untuk pertama kalinya. Reset juga dapat dilakukan secara manual dengan menekan tombol reset yang berupa switch push button.

Rangkaian rest terbentuk oleh komponen R dan C yang sudah baku (ditetapkan oleh perusahaan pembuat IC AT 89S51). Nilai R yang dipakai adalah 10 KΩ dan C 10 µF. Besarnya nilai tahanan dan kapasitor pada rangkaian rest akan menentukan waktu/lama pulsa reset.

Dengan rumus :

$t = R \times C$

Agar dapt terjadi secara normal maka nilai t harus lebih besar dari 30 siklus mesin.

$t >> 30 \times Time$

Karena nilai Time diatas adalah 1 μs maka :

$t >> 30 \times 1\mu s$

$t >> 30\ \mu s$

Dengan mengambil nilai R dan C sebesar 10 KΩ dan 10 μF maka besarnya t dapat dicari sebagai berikut :

$t = R \times C$

$t = 10K\Omega \times 10\ \mu F$

$t = 10.10^{3} \times 10.10^{-6}$

$t = 100 \times 10^{-3}$

$t = 0.1\ \mu s$

Dengan demikian nilai t jauh lebih besar dibanding nilai minimumnya.

3.4. Perancangan Perangkat Lunak (Software)

Program adalah kumpulan dari instruksi untuk mengendalikan atau mengoperasikan system perangkat keras (Hardware). Adapun langkah-langkah pembuatan program ini adalah sebagai berikut :

a. Membuat dagram alir (*flowchart*) program yang akan dibuat.

b. Mengubah diagram alir tersebut ke dalam bahasa pemrograman .

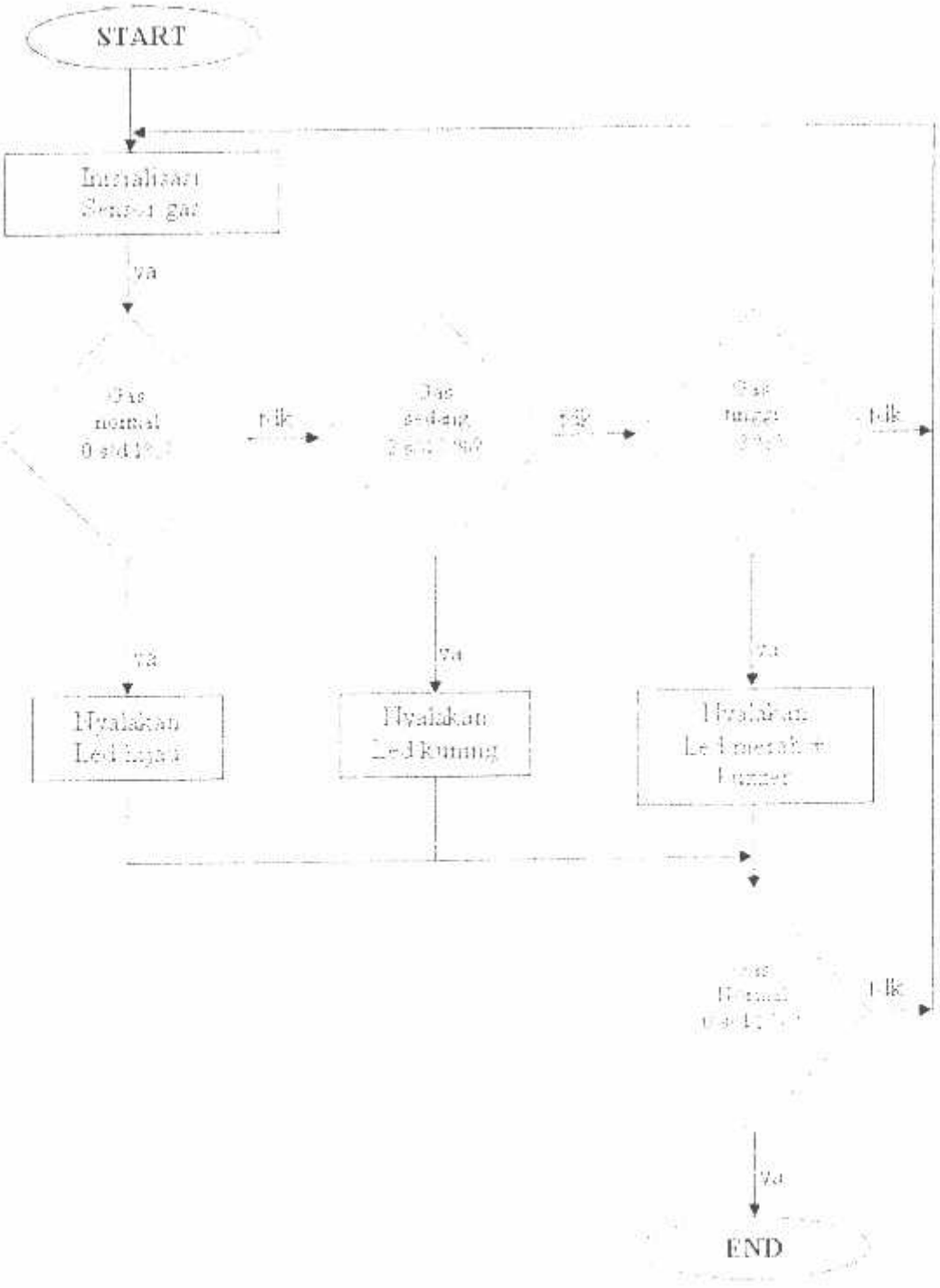
c. Penulisan program dengan menggunakan teks editor atau edit plus dan disimpan dengan eksistensi H51.

d. Mengkompilasikan program yang telah dibuat ke dalam memory, sampai menghasilkan program dengan ekstensi HEX.

e. Merubah file berekstensi HEX menjadi file berekstensi BIN.

f. Men-*download* file berekstensi BIN ke dalam PEROM mikrokontroller AT89S51. Kemudian memasukkan program yang telah selesai, dan system akan bekerja dengan baik jika perancangan perangkat lunak (software) sesuai dengan perangkat keras (hardware) yang mendukung.

3.4.1. Flowchart system



Gambar 3.9. Flowchart

Sumber: Perencanaan

BAB IV

PENGUJIAN ALAT

4.1. Pendahuluan

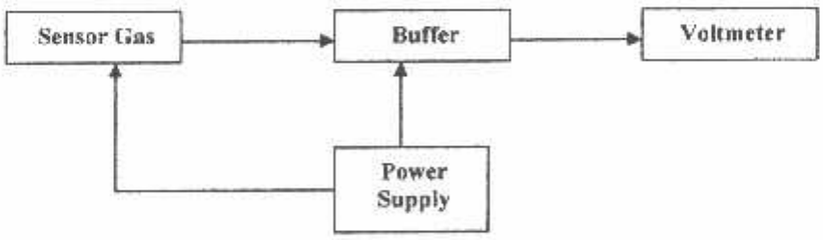
Setelah semua alat telah terangkai, maka perlu diadakan pengujian yang bertujuan untuk mengetahui apakah system yang telah terangkai dapat bekerja sesuai dengan yang diharapkan atau tidak. Pengujian dilakukan pada tiap sub system yang meliputi :

- Sensor gas
- Rangkaian penguat
- Rangkaian ADC
- Simulasi pada ruangan berisi gas LPG

Dari sub system diatas dilakukan proses pengujian secara lengkap untuk mengetahui fungsi dari masing-masing blok.

4.1.1. Pengujian Rangkaian Sensor dan Penguat

Dari pengujian ini bertujuan untuk mengetahui nilai tegangan yang keluar dari sensor.



Gambar 4.1. Blok Diagram Pengujian Sensor dan Penguat
Sumber: Hasil Pengujian

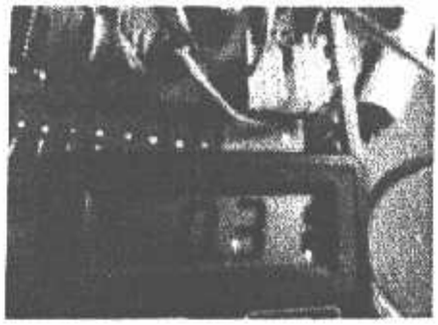
Dengan demikian dapat dilihat hasil pengujian dari blok rangkaian diatas dan hasil pengukuran dapat dibandingkan dengan hasil perhitungan seperti yang diperlihatkan pada table 4-1 berikut ini :

Misalkan kadar gas LPG dalam ruangan tersebut adalah 0-5 % maka :

Tabel 4.1. Perbandingan Hasil Pengujian dan Hasil Perhitungan

	PENGUKURAN		PERHITUNGAN	
GAS	Output TGS 2610	Output Buffer	Output TGS 2610	Output Buffer
(%)	(Volt)	(Volt)	(Volt)	(Volt)
0	0.2	0.2	0	0
0.2	1.3	1.3	0.2	0.2
0.4	1.7	1.7	0.4	0.4
0.6	2	2	0.6	0.6
8	2.3	2.3	0.8	0.8
1	2.5	2.5	1	1
2	3	3	2	2
3	3.1	3.1	3	3
4	3.2	3.2	4	4
5	3.3	3.3	5	5

Dari hasil pengujian tersebut terlihat bahwa tegangan output terhadap kadar gas LPG tidaklah linear. Sensor mengalami titik kejenuhan pada saat kadar gas LPG di udara mencapai 5%.

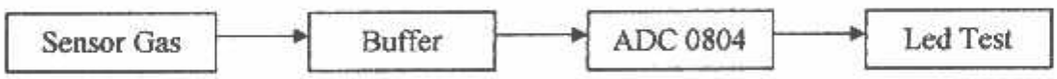


Gambar 4.2. Pengujian Sensor dan Penguat

Sumber: Hasil Pengujian

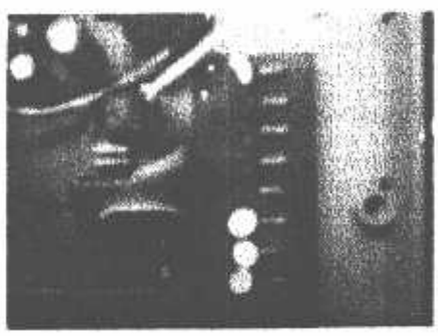
4.1.2. Pengujian Rangkaian ADC 0804

Pengujian rangkaian ADC dilakukan dengan memasangkan 8 buah LED Test sesuai dengan jumlah keluaran ADC yaitu 8 bit. Keluaran ADC adlah biner 8 bit yang dikombinasi bitnya tergantung dari input ADC yang berasal dari penguat differensial.



Gambar 4.3. Blok Diagram Pengujian ADC 0804

Sumber: Hasil Pengujian



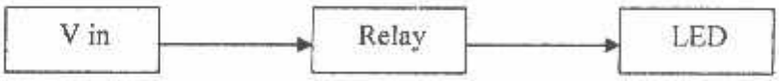
Gambar 4.4. Pengujian Rangkaian ADC 0804

Sumber: Hasil Pengujian

4.1.3. Pengujian Rangkaian Driver Relay

Yang perlu diketahui dalam pengujian rangkaian driver relay ini adalah apakah rangkaian tersebut bisa bekerja sebagaimana mestinya, yaitu menghubungkan dan memutus secara otomatis antara perangkat dengan beban apabila perangkat diaktifkan.

Pengujian Dilakukan dengan menggunakan tegangan 5 volt sebagai trigger untuk menggerakkan relay.



Gambar 4.11. Blok Diagram Pengujian Driver Relay

Sumber: Hasil Pengujian

Hasil pengujian dari rangkaian driver relay dapat dilihat pada table dibawah ini :

Tabel 4-5 Hasil Pengujian Driver Relay

V in	Kondisi Relay
0 Volt	Off
5 Volt	On

Sumber: Hasil Pengujian

Hasil pengujian relay yang dilakukan dengan simulasi peraga led yaitu pada saat relay tersambung, maka led akan menyala atau berlogika 1, dan pada saat relay terputus maka led akan mati atau berlogika 0.

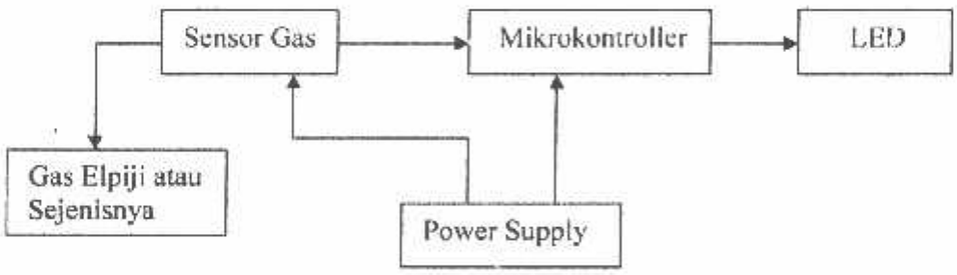
4.2. Pengujian Dengan Software

Setelah pengujian yang dilakukan secara perblok rangkaian, selanjutnya dilakukan pengujian secara system keseluruhan. Untuk itu maka kita harus menyediakan alat dan komponen yang nantinya diperlukan.

Pengujian yang dilakukan harus melalui prosedur dan urutan yang telah ditentukan. Hal ini dilakukan untuk menjaga dan merawat alat yang telah dibuat agar tahan lama.

Alat dan komponen :

- Rangkaian mikrokontroller
- Konektor
- Power supply
- Miniature ruangan kosong
- Gas elpiji secukupnya.



Gambar 4.12. Diagram Pengujian Sistem Secara Keseluruhan

Sumber: Hasil Pengujian

BAB V

PENUTUP

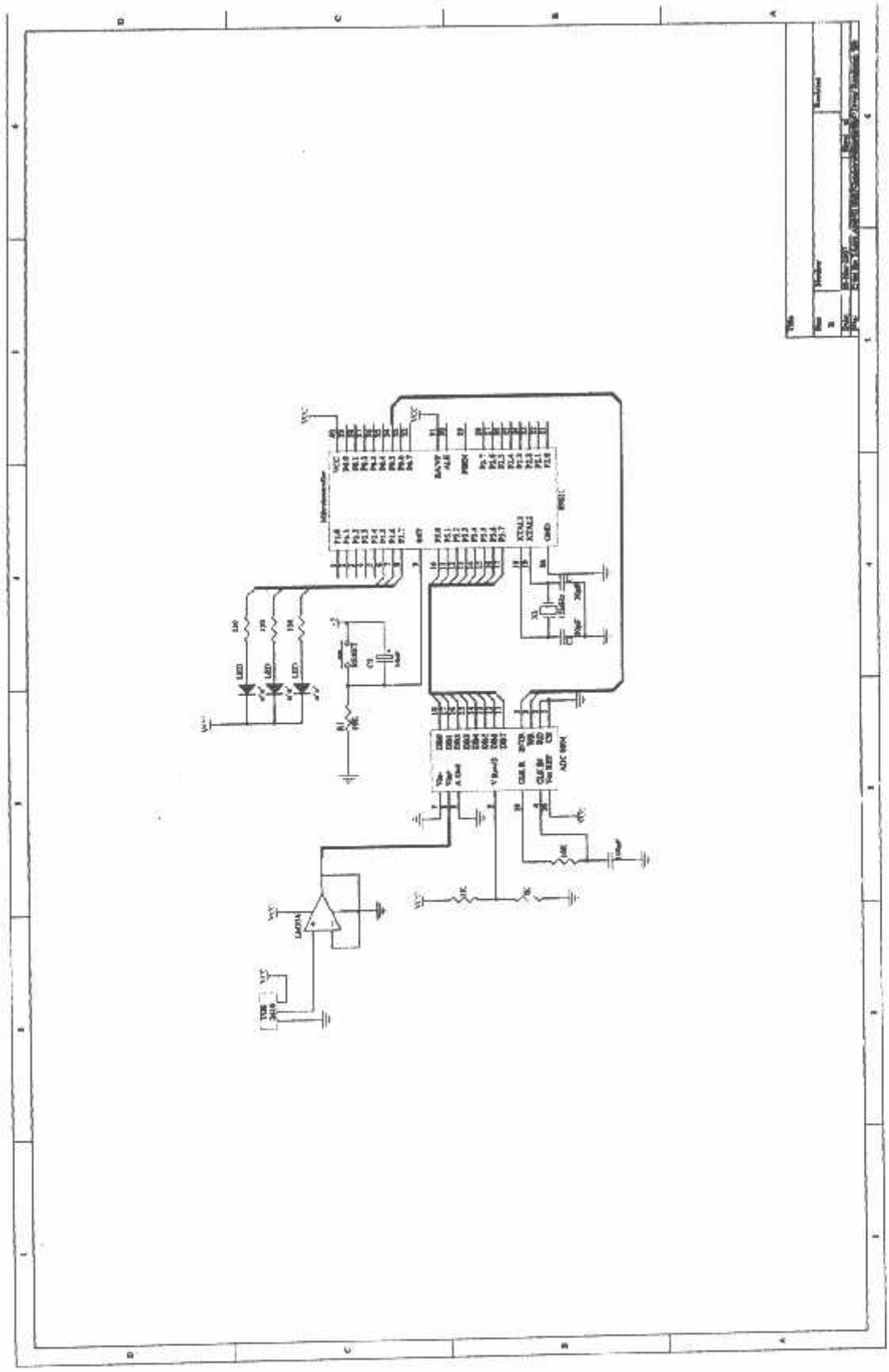
5.1. Kesimpulan

Dari hasil pengujian dan analisa dari alat yamg telah dibuat maka, dapat ditarik kesimpulan :

1. Keluaran yang di hasilkan oleh TGS 2610 sudah sesuai dengan yang di harapkan,sehingga dapat diproses pengkondisi sinyal.
2. Pada dasarnya alat ini daat bekerja dengan baik dan benar,masalah perbedaan tegangan dari hasil perhtungan dan pengukuran dapat di sebabkan oleh karena toleransi dari komponen yang digunakan

5.2. Saran-saran

1. Kemampuan alat ini akan lebeh baik jika digunakankonponen yang lebih presisi dan berkualitas baik
2. Untuk bagian indikator sebaiknya akan lebik baik jika digunakan indicator lampu led jenis super brihgt agar lebih terang kuantitas cahayanya.



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DataSheet TGS 2610

INSTITUT TEKNOLOGI NASIONAL MALANG
FAKULTAS TEKNOLOGI INDUSTRI
JURUSAN TEKNIK ELEKTRO D-III

LEMBAR ASISTENSI TUGAS AKHIR

Nama	:	Venny Purwanti Khasanah
NIM	:	0357039
Jurusan	:	T. Elektronika D-III
Judul Tugas Akhir	:	Perencanaan dan Pembuatan Alat Pemantau Kebocoran Gas LPG

NO	TANGGAL	REVISI	TTD
1	21-02-2007	BAB I – II Revisi	
2	12-03-2007	BAB – III Perbaikan	
3	15-03-2007	BAB – IV Acc	
4	21-03-2007	BAB – V Acc	
5	21-03-2007	Uji alat	
6.	21-3-2007	Acc maju	

Malang, 21 Maret '07
Dosen Pembimbing,

Bambang Priyohartono, ST MT

LAMPIRAN

FIGARO

PRODUCT INFORMATION

TGS 2610 - for the detection of LP Gas

Features:

* Low power consumption
* High sensitivity to LP and its component gases (e.g. propane and butane)
* Long life and low cost
* Uses simple electrical circuit

Applications:

* Residential LP leak detectors and alarms
* Portable LP detectors
* LP gas and vapor detection

TGS2610 is a semiconductor type gas sensor which combines very high sensitivity to LP gas with low power consumption and long life. Due to miniaturization of its sensing chip, TGS2610 requires a heater current of only 56mA and the device is housed in a standard TO-5 package.

The TGS2610 is available in two different models which have different external housings but identical sensitivity to LP gas. Both models are able to satisfy the requirements of performance standards such as UL1484 and EN50194.

TGS2610-J00 possesses small size and quick gas response, making it suitable for gas leakage checkers.

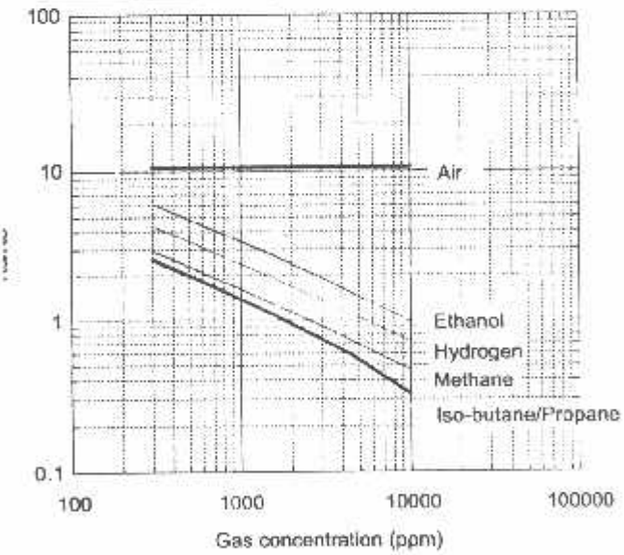
TGS2610-B00 uses filter material in its housing which eliminates the influence of interference gases such as alcohol, resulting in highly selective response to LP gas. This feature makes the sensor ideal for residential gas leakage detectors which require durability and resistance against interference gas.

The figure below represents typical sensitivity characteristics, all data having been gathered at standard test conditions (see reverse side of this sheet). The Y-axis is indicated as *sensor resistance ratio* (Rs/Ro) which is defined as follows.

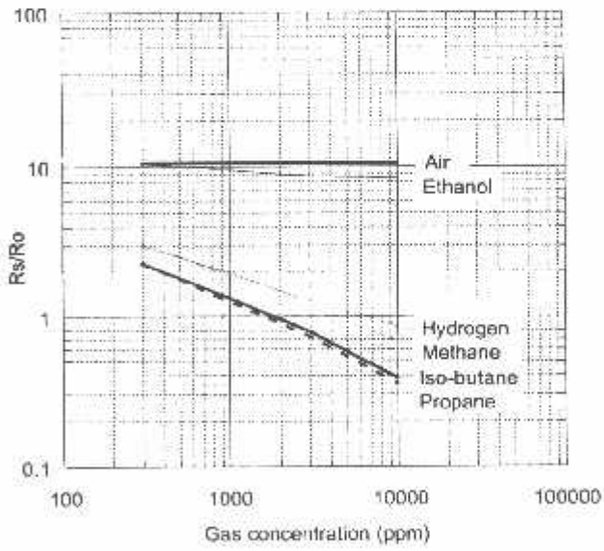
Rs = Sensor resistance in displayed gases at various concentrations

Ro = Sensor resistance in 1800ppm of iso-butane

TGS2610-J00 Sensitivity Characteristics:



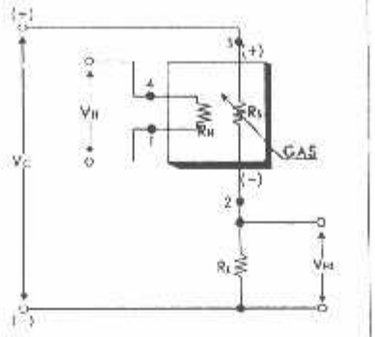
TGS2610-B00 Sensitivity Characteristics:



Basic Measuring Circuit:

The sensor requires two voltage inputs: heater voltage (V_H) and circuit voltage (V_C). The heater voltage (V_H) is applied to the integrated heater in order to maintain the sensing element at a specific temperature which is optimal for sensing. Circuit voltage (V_C) is applied to allow measurement of voltage (V_{RL}) across a load resistor (R_L) which is connected in series with the sensor.

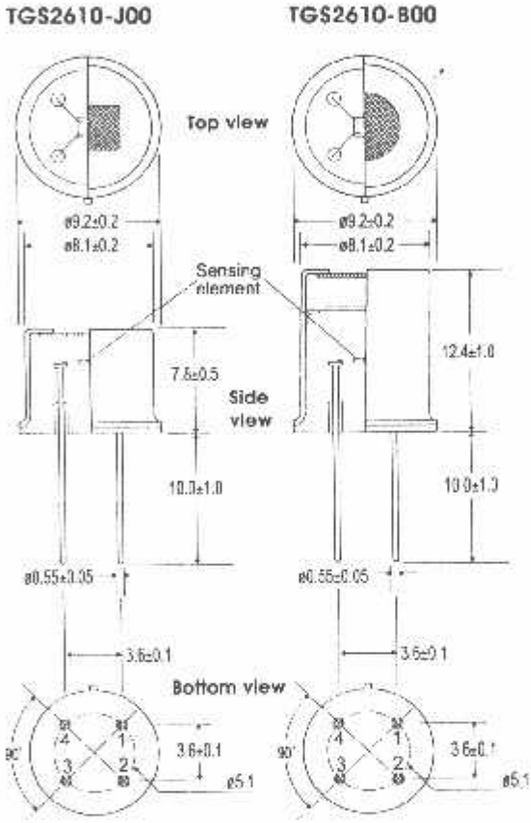
A common power supply circuit can be used for both V_C and V_H to fulfill the sensor's electrical requirements. The value of the load resistor (R_L) should be chosen to optimize the alarm threshold value, keeping power dissipation (P_S) of the semiconductor below a limit of 15mW. Power dissipation (P_S) will be highest when the value of Rs is equal to R_L on exposure to gas.



Specifications:

Model number			TGS 2610	
Sensing element type			D1	
Standard package			TO-5 metal can	
Target gases			Butane, LP gas	
Typical detection range			500 - 10,000 ppm	
Standard circuit conditions	Heater Voltage	V_H	5.0±0.2V DC/AC	
	Circuit voltage	V_C	5.0±0.2V DC/AC	$P_S \leq 15mW$
	Load resistance	R_L	Variable	0.45kΩ min.
Electrical characteristics under standard test conditions	Heater resistance	R_H	approx. 59Ω at room temp.	
	Heater current	I_H	56 ± 5mA	
	Heater power consumption	P_H	280mW	V_H = 5.0V DC
	Sensor resistance	Rs	0.68–6.8kΩ in 1800ppm iso-butane	
	Sensitivity (change ratio of Rs)		0.56 ± 0.06	Rs (3000ppm) / Rs (1000ppm)
Standard test conditions	Test gas conditions		Iso-butane in air at 20-2°C, 65+5%RH	
	Circuit conditions		V_C = 5.0±0.01V DC, V_H = 5.0±0.05V DC	
	Conditionning period before test		7 days	

Structure and Dimensions:



Pin connection:
1: Heater
2: Sensor electrode (-)
3: Sensor electrode (+)
4: Heater

The value of power dissipation (Ps) can be calculated by utilizing the following formula:

$$P_S = \frac{(V_C - V_{RL})^2}{R_S}$$

Sensor resistance (Rs) is calculated with a measured value of V_{RL} by using the following formula:

$$R_S = \frac{V_C - V_{RL}}{V_{RL}} \times R_L$$

All sensor characteristics shown in this brochure represent typical characteristics. Actual characteristics vary from sensor to sensor. The only characteristics warranted are those in the Specification table above.

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email: figaro@figaro.co.jp

REV: 08/03

atures

- ompatible with MCS®-51 Products
- K Bytes of In-System Programmable (ISP) Flash Memory
  - Endurance: 1000 Write/Erase Cycles
- .0V to 5.5V Operating Range
- ully Static Operation: 0 Hz to 33 MHz
- hree-level Program Memory Lock
- 28 x 8-bit Internal RAM
- 2 Programmable I/O Lines
- wo 16-bit Timer/Counters
- ix Interrupt Sources
- ull Duplex UART Serial Channel
- ow-power Idle and Power-down Modes
- terrupt Recovery from Power-down Mode
- 'atchdog Timer
- ual Data Pointer
- ower-off Flag
- ast Programming Time
- lexible ISP Programming (Byte and Page Mode)
- reen (Pb/Halide-free) Packaging Option

Description

e AT89S51 is a low-power, high-performance CMOS 8-bit microcontroller with 4K es of In-System Programmable Flash memory. The device is manufactured using nel's high-density nonvolatile memory technology and is compatible with the indus- standard 80C51 instruction set and pinout. The on-chip Flash allows the program mory to be reprogrammed in-system or by a conventional nonvolatile memory pro- mmer. By combining a versatile 8-bit CPU with In-System Programmable Flash on nonolithic chip, the Atmel AT89S51 is a powerful microcontroller which provides a hly-flexible and cost-effective solution to many embedded control applications.

e AT89S51 provides the following standard features: 4K bytes of Flash, 128 bytes RAM, 32 I/O lines, Watchdog timer, two data pointers, two 16-bit timer/counters, a e-vector two-level interrupt architecture, a full duplex serial port, on-chip oscillator, d clock circuitry. In addition, the AT89S51 is designed with static logic for operation wn to zero frequency and supports two software selectable power saving modes. ie Idle Mode stops the CPU while allowing the RAM, timer/counters, serial port, and errupt system to continue functioning. The Power-down mode saves the RAM con- nts but freezes the oscillator, disabling all other chip functions until the next external errupt or hardware reset.

ATMEL®

8-bit Microcontroller with 4K Bytes In-System Programmable Flash

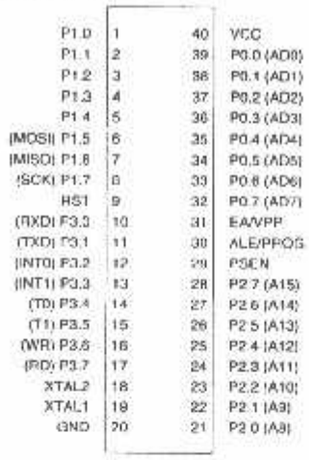
AT89S51

2487C–MICRO–03/05

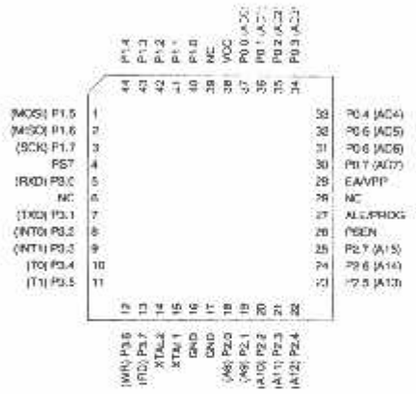
ATMEL

2. Pin Configurations

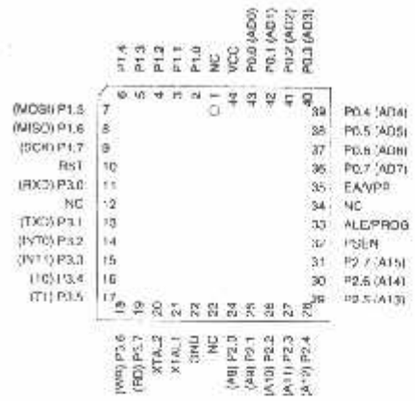
2.1 40-lead PDIP



2.2 44-lead TQFP



2.3 44-lead PLCC



2.4 42-lead PDIP

. Pin Description

.1 VCC

Supply voltage (all packages except 42-PDIP).

2 GND

Ground (all packages except 42-PDIP; for 42-PDIP GND connects only the logic core and the embedded program memory).

3 VDD

Supply voltage for the 42-PDIP which connects only the logic core and the embedded program memory.

4 PWRVDD

Supply voltage for the 42-PDIP which connects only the I/O Pad Drivers. The application board **MUST** connect both VDD and PWRVDD to the board supply voltage.

5 PWRGND

Ground for the 42-PDIP which connects only the I/O Pad Drivers. PWRGND and GND are weakly connected through the common silicon substrate, but not through any metal link. The application board **MUST** connect both GND and PWRGND to the board ground.

6 Port 0

Port 0 is an 8-bit open drain bi-directional I/O port. As an output port, each pin can sink eight TTL inputs. When 1s are written to port 0 pins, the pins can be used as high-impedance inputs.

Port 0 can also be configured to be the multiplexed low-order address/data bus during accesses to external program and data memory. In this mode, P0 has internal pull-ups.

Port 0 also receives the code bytes during Flash programming and outputs the code bytes during program verification. **External pull-ups are required during program verification.**

7 Port 1

Port 1 is an 8-bit bi-directional I/O port with internal pull-ups. The Port 1 output buffers can sink/source four TTL inputs. When 1s are written to Port 1 pins, they are pulled high by the internal pull-ups and can be used as inputs. As inputs, Port 1 pins that are externally being pulled low will source current (I_{IL}) because of the internal pull-ups.

Port 1 also receives the low-order address bytes during Flash programming and verification.

Port Pin	Alternate Functions
P1.5	MOSI (used for In-System Programming)
P1.6	MISO (used for In-System Programming)
P1.7	SCK (used for In-System Programming)

In normal operation, ALE is emitted at a constant rate of 1/6 the oscillator frequency and may be used for external timing or clocking purposes. Note, however, that one ALE pulse is skipped during each access to external data memory.

If desired, ALE operation can be disabled by setting bit 0 of SFR location 8EH. With the bit set, ALE is active only during a MOVX or MOVC instruction. Otherwise, the pin is weakly pulled high. Setting the ALE-disable bit has no effect if the microcontroller is in external execution mode.

12 $\overline{\text{PSEN}}$

Program Store Enable ($\overline{\text{PSEN}}$) is the read strobe to external program memory.

When the AT89S51 is executing code from external program memory, $\overline{\text{PSEN}}$ is activated twice each machine cycle, except that two $\overline{\text{PSEN}}$ activations are skipped during each access to external data memory.

.13 $\overline{\text{EA}}$/VPP

External Access Enable. $\overline{\text{EA}}$ must be strapped to GND in order to enable the device to fetch code from external program memory locations starting at 0000H up to FFFFH. Note, however, that if lock bit 1 is programmed, $\overline{\text{EA}}$ will be internally latched on reset.

$\overline{\text{EA}}$ should be strapped to V_{CC} for internal program executions.

This pin also receives the 12-volt programming enable voltage (V_{PP}) during Flash programming.

.14 XTAL1

Input to the inverting oscillator amplifier and input to the internal clock operating circuit.

.15 XTAL2

Output from the inverting oscillator amplifier

5. Special Function Registers

A map of the on-chip memory area called the Special Function Register (SFR) space is shown in Table 5-1.

Note that not all of the addresses are occupied, and unoccupied addresses may not be implemented on the chip. Read accesses to these addresses will in general return random data, and write accesses will have an indeterminate effect.

Table 5-2. AUXR: Auxiliary Register

AUXR Address = 8EH Reset Value = XXX00XX0B

Not Bit Addressable

	–	–	–	WDIDLE	DISRTO	–	–	DISALE
Bit	7	6	5	4	3	2	1	0

–	Reserved for future expansion
DISALE	Disable/Enable ALE
	DISALE Operating Mode
	0 ALE is emitted at a constant rate of 1/6 the oscillator frequency
	1 ALE is active only during a MOVX or MOVC instruction
DISRTO	Disable/Enable Reset-out
	DISRTO
	0 Reset pin is driven High after WDT times out
	1 Reset pin is input only
WDIDLE	Disable/Enable WDT in IDLE mode
WDIDLE	
0	WDT continues to count in IDLE mode
1	WDT halts counting in IDLE mode

Dual Data Pointer Registers: To facilitate accessing both internal and external data memory, two banks of 16-bit Data Pointer Registers are provided: DP0 at SFR address locations 82H-83H and DP1 at 84H-85H. Bit DPS = 0 in SFR AUXR1 selects DP0 and DPS = 1 selects DP1. The user should **ALWAYS** initialize the DPS bit to the appropriate value before accessing the respective Data Pointer Register.

Power Off Flag: The Power Off Flag (POF) is located at bit 4 (PCON.4) in the PCON SFR. POF is set to "1" during power up. It can be set and rest under software control and is not affected by reset.

Table 5-3. AUXR1: Auxiliary Register 1

AUXR1 Address = A2H Reset Value = XXXXXXX0B

Not Bit Addressable

	–	–	–	–	–	–	–	DPS
Bit	7	6	5	4	3	2	1	0

– Reserved for future expansion

DPS Data Pointer Register Select

DPS	
0	Selects DPTR Registers DP0L, DP0H
1	Selects DPTR Registers DP1L, DP1H

›. Memory Organization

MCS-51 devices have a separate address space for Program and Data Memory. Up to 64K bytes each of external Program and Data Memory can be addressed.

›.1 Program Memory

If the $\overline{EA}$ pin is connected to GND, all program fetches are directed to external memory.

On the AT89S51, if $\overline{EA}$ is connected to V_{CC}, program fetches to addresses 0000H through FFFH are directed to internal memory and fetches to addresses 1000H through FFFFH are directed to external memory.

›.2 Data Memory

The AT89S51 implements 128 bytes of on-chip RAM. The 128 bytes are accessible via direct and indirect addressing modes. Stack operations are examples of indirect addressing, so the 128 bytes of data RAM are available as stack space.

'. Watchdog Timer (One-time Enabled with Reset-out)

The WDT is intended as a recovery method in situations where the CPU may be subjected to software upsets. The WDT consists of a 14-bit counter and the Watchdog Timer Reset (WDTRST) SFR. The WDT is defaulted to disable from exiting reset. To enable the WDT, a user must write 01EH and 0E1H in sequence to the WDTRST register (SFR location 0A6H). When the WDT is enabled, it will increment every machine cycle while the oscillator is running. The WDT timeout period is dependent on the external clock frequency. There is no way to disable the WDT except through reset (either hardware reset or WDT overflow reset). When WDT overflows, it will drive an output RESET HIGH pulse at the RST pin.

'.1 Using the WDT

To enable the WDT, a user must write 01EH and 0E1H in sequence to the WDTRST register (SFR location 0A6H). When the WDT is enabled, the user needs to service it by writing 01EH and 0E1H to WDTRST to avoid a WDT overflow. The 14-bit counter overflows when it reaches 16383 (3FFFH), and this will reset the device. When the WDT is enabled, it will increment every machine cycle while the oscillator is running. This means the user must reset the WDT at least

every 16383 machine cycles. To reset the WDT the user must write 01EH and 0E1H to WDTRST. WDTRST is a write-only register. The WDT counter cannot be read or written. When WDT overflows, it will generate an output RESET pulse at the RST pin. The RESET pulse duration is 98xTOSC, where TOSC = 1/FOSC. To make the best use of the WDT, it should be serviced in those sections of code that will periodically be executed within the time required to prevent a WDT reset.

2 WDT During Power-down and Idle

In Power-down mode the oscillator stops, which means the WDT also stops. While in Power-down mode, the user does not need to service the WDT. There are two methods of exiting Power-down mode: by a hardware reset or via a level-activated external interrupt, which is enabled prior to entering Power-down mode. When Power-down is exited with hardware reset, servicing the WDT should occur as it normally does whenever the AT89S51 is reset. Exiting Power-down with an interrupt is significantly different. The interrupt is held low long enough for the oscillator to stabilize. When the interrupt is brought high, the interrupt is serviced. To prevent the WDT from resetting the device while the interrupt pin is held low, the WDT is not started until the interrupt is pulled high. It is suggested that the WDT be reset during the interrupt service for the interrupt used to exit Power-down mode.

To ensure that the WDT does not overflow within a few states of exiting Power-down, it is best to reset the WDT just before entering Power-down mode.

Before going into the IDLE mode, the WDIDLE bit in SFR AUXR is used to determine whether the WDT continues to count if enabled. The WDT keeps counting during IDLE (WDIDLE bit = 0) as the default state. To prevent the WDT from resetting the AT89S51 while in IDLE mode, the user should always set up a timer that will periodically exit IDLE, service the WDT, and reenter IDLE mode.

With WDIDLE bit enabled, the WDT will stop to count in IDLE mode and resumes the count upon exit from IDLE.

i. UART

The UART in the AT89S51 operates the same way as the UART in the AT89C51. For further information on the UART operation, please click on the document link below:

http://www.atmel.com/dyn/resources/prod_documents/DOC4316.PDF

i. Timer 0 and 1

Timer 0 and Timer 1 in the AT89S51 operate the same way as Timer 0 and Timer 1 in the AT89C51. For further information on the timers' operation, please click on the document link below:

http://www.atmel.com/dyn/resources/prod_documents/DOC4316.PDF

0. Interrupts

The AT89S51 has a total of five interrupt vectors: two external interrupts ($\overline{INT0}$ and $\overline{INT1}$), two timer interrupts (Timers 0 and 1), and the serial port interrupt. These interrupts are all shown in Figure 10-1.

Each of these interrupt sources can be individually enabled or disabled by setting or clearing a bit in Special Function Register IE. IE also contains a global disable bit, EA, which disables all interrupts at once.

Note that Table 10-1 shows that bit positions IE.6 and IE.5 are unimplemented. User software should not write 1s to these bit positions, since they may be used in future AT89 products.

The Timer 0 and Timer 1 flags, TF0 and TF1, are set at S5P2 of the cycle in which the timers overflow. The values are then polled by the circuitry in the next cycle.

Table 10-1. Interrupt Enable (IE) Register

(MSB)							(LSB)
EA	–	–	ES	ET1	EX1	ET0	EX0

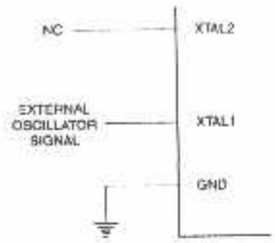
Enable Bit = 1 enables the interrupt.

Enable Bit = 0 disables the interrupt.

Symbol	Position	Function
EA	IE.7	Disables all interrupts. If EA = 0, no interrupt is acknowledged. If EA = 1, each interrupt source is individually enabled or disabled by setting or clearing its enable bit.
–	IE.6	Reserved
–	IE.5	Reserved
ES	IE.4	Serial Port interrupt enable bit
ET1	IE.3	Timer 1 interrupt enable bit
EX1	IE.2	External interrupt 1 enable bit
ET0	IE.1	Timer 0 interrupt enable bit
EX0	IE.0	External interrupt 0 enable bit

User software should never write 1s to reserved bits, because they may be used in future AT89 products.

Figure 11-2. External Clock Drive Configuration



2. Idle Mode

In idle mode, the CPU puts itself to sleep while all the on-chip peripherals remain active. The mode is invoked by software. The content of the on-chip RAM and all the special function registers remain unchanged during this mode. The idle mode can be terminated by any enabled interrupt or by a hardware reset.

Note that when idle mode is terminated by a hardware reset, the device normally resumes program execution from where it left off, up to two machine cycles before the internal reset algorithm takes control. On-chip hardware inhibits access to internal RAM in this event, but access to the port pins is not inhibited. To eliminate the possibility of an unexpected write to a port pin when idle mode is terminated by a reset, the instruction following the one that invokes idle mode should not write to a port pin or to external memory.

3. Power-down Mode

In the Power-down mode, the oscillator is stopped, and the instruction that invokes Power-down is the last instruction executed. The on-chip RAM and Special Function Registers retain their values until the Power-down mode is terminated. Exit from Power-down mode can be initiated either by a hardware reset or by activation of an enabled external interrupt ($\overline{INT0}$ or $\overline{INT1}$). Reset redefines the SFRs but does not change the on-chip RAM. The reset should not be activated before V_{CC} is restored to its normal operating level and must be held active long enough to allow the oscillator to restart and stabilize.

Table 13-1. Status of External Pins During Idle and Power-down Modes

Mode	Program Memory	ALE	$\overline{PSEN}$	PORT0	PORT1	PORT2	PORT3
Idle	Internal	1	1	Data	Data	Data	Data
Idle	External	1	1	Float	Data	Address	Data
Power-down	Internal	0	0	Data	Data	Data	Data
Power-down	External	0	0	Float	Data	Data	Data

4. Program Memory Lock Bits

The AT89S51 has three lock bits that can be left unprogrammed (U) or can be programmed (P) to obtain the additional features listed in Table 14-1.

Table 14-1. Lock Bit Protection Modes

Program Lock Bits				
	LB1	LB2	LB3	Protection Type
1	U	U	U	No program lock features
2	P	U	U	MOVC instructions executed from external program memory are disabled from fetching code bytes from internal memory, $\overline{EA}$ is sampled and latched on reset, and further programming of the Flash memory is disabled
3	P	P	U	Same as mode 2, but verify is also disabled
4	P	P	P	Same as mode 3, but external execution is also disabled

When lock bit 1 is programmed, the logic level at the $\overline{EA}$ pin is sampled and latched during reset. If the device is powered up without a reset, the latch initializes to a random value and holds that value until reset is activated. The latched value of $\overline{EA}$ must agree with the current logic level at that pin in order for the device to function properly.

5. Programming the Flash – Parallel Mode

The AT89S51 is shipped with the on-chip Flash memory array ready to be programmed. The programming interface needs a high-voltage (12-volt) program enable signal and is compatible with conventional third-party Flash or EPROM programmers.

The AT89S51 code memory array is programmed byte-by-byte.

Programming Algorithm: Before programming the AT89S51, the address, data, and control signals should be set up according to the Flash Programming Modes table (Table 17-1) and Figure 17-1 and Figure 17-2. To program the AT89S51, take the following steps:

1. Input the desired memory location on the address lines.
2. Input the appropriate data byte on the data lines.
3. Activate the correct combination of control signals.
4. Raise $\overline{EA}/V_{PP}$ to 12V.
5. Pulse ALE/$\overline{PROG}$ once to program a byte in the Flash array or the lock bits. The byte-write cycle is self-timed and typically takes no more than 50 µs. Repeat steps 1 through 5, changing the address and data for the entire array or until the end of the object file is reached.

$\overline{Data}$ Polling: The AT89S51 features $\overline{Data}$ Polling to indicate the end of a byte write cycle. During a write cycle, an attempted read of the last byte written will result in the complement of the written data on P0.7. Once the write cycle has been completed, true data is valid on all outputs, and the next cycle may begin. $\overline{Data}$ Polling may begin any time after a write cycle has been initiated.

Ready/$\overline{Busy}$: The progress of byte programming can also be monitored by the RDY/$\overline{BSY}$ output signal. P3.0 is pulled low after ALE goes high during programming to indicate $\overline{BUSY}$. P3.0 is pulled high again when programming is done to indicate READY.

Program Verify: If lock bits LB1 and LB2 have not been programmed, the programmed code data can be read back via the address and data lines for verification. **The status of the individual lock bits can be verified directly by reading them back.**

Reading the Signature Bytes: The signature bytes are read by the same procedure as a normal verification of locations 000H, 100H, and 200H, except that P3.6 and P3.7 must be pulled to a logic low. The values returned are as follows.

(000H) = 1EH indicates manufactured by Atmel
(100H) = 51H indicates AT89S51
(200H) = 06H

Chip Erase: In the parallel programming mode, a chip erase operation is initiated by using the proper combination of control signals and by pulsing ALE/$\overline{PROG}$ low for a duration of 200 ns - 500 ns.

In the serial programming mode, a chip erase operation is initiated by issuing the Chip Erase instruction. In this mode, chip erase is self-timed and takes about 500 ms.

During chip erase, a serial read from any address location will return 00H at the data output.

16. Programming the Flash – Serial Mode

The Code memory array can be programmed using the serial ISP interface while RST is pulled to V_{CC}. The serial interface consists of pins SCK, MOSI (input) and MISO (output). After RST is set high, the Programming Enable instruction needs to be executed first before other operations can be executed. Before a reprogramming sequence can occur, a Chip Erase operation is required.

The Chip Erase operation turns the content of every memory location in the Code array into FFH.

Either an external system clock can be supplied at pin XTAL1 or a crystal needs to be connected across pins XTAL1 and XTAL2. The maximum serial clock (SCK) frequency should be less than 1/16 of the crystal frequency. With a 33 MHz oscillator clock, the maximum SCK frequency is 2 MHz.

16.1 Serial Programming Algorithm

To program and verify the AT89S51 in the serial programming mode, the following sequence is recommended:

1. Power-up sequence:
   a. Apply power between VCC and GND pins.
   b. Set RST pin to "H".

   If a crystal is not connected across pins XTAL1 and XTAL2, apply a 3 MHz to 33 MHz clock to XTAL1 pin and wait for at least 10 milliseconds.
2. Enable serial programming by sending the Programming Enable serial instruction to pin MOSI/P1.5. The frequency of the shift clock supplied at pin SCK/P1.7 needs to be less than the CPU clock at XTAL1 divided by 16.
3. The Code array is programmed one byte at a time in either the Byte or Page mode. The write cycle is self-timed and typically takes less than 0.5 ms at 5V.
4. Any memory location can be verified by using the Read instruction that returns the content at the selected address at serial output MISO/P1.6.

5. At the end of a programming session, RST can be set low to commence normal device operation.

Power-off sequence (if needed):

1. Set XTAL1 to "L" (if a crystal is not used).
2. Set RST to "L".
3. Turn V_{CC} power off.

Data Polling: The $\overline{\text{Data}}$ Polling feature is also available in the serial mode. In this mode, during a write cycle an attempted read of the last byte written will result in the complement of the MSB of the serial output byte on MISO.

6.2 Serial Programming Instruction Set

The Instruction Set for Serial Programming follows a 4-byte protocol and is shown in the "Serial Programming Instruction Set" on page 20.

7. Programming Interface – Parallel Mode

Every code byte in the Flash array can be programmed by using the appropriate combination of control signals. The write operation cycle is self-timed and once initiated, will automatically time itself to completion.

Most major worldwide programming vendors offer worldwide support for the Atmel AT89 microcontroller series. Please contact your local programming vendor for the appropriate software revision.

able 17-1. Flash Programming Modes

Mode	V_{CC}	RST	$\overline{\text{PSEN}}$	ALE/ $\overline{\text{PROG}}$	$\overline{\text{EA}}$/ V_{PP}	P2.6	P2.7	P3.3	P3.6	P3.7	P0.7-0 Data	P2.3-0	P1.7-0
												Address	
Write Code Data	5V	H	L	(2)	12V	L	H	H	H	H	D_{IN}	A11-8	A7-0
Read Code Data	5V	H	L	H	H	L	L	L	H	H	D_{OUT}	A11-8	A7-0
Write Lock Bit 1	5V	H	L	(3)	12V	H	H	H	H	H	X	X	X
Write Lock Bit 2	5V	H	L	(3)	12V	H	H	H	L	L	X	X	X
Write Lock Bit 3	5V	H	L	(3)	12V	H	L	H	H	L	X	X	X
Read Lock Bits 1, 2, 3	5V	H	L	H	H	H	H	L	H	L	P0.2, P0.3, P0.4	X	X
Chip Erase	5V	H	L	(1)	12V	H	L	H	L	L	X	X	X
Read Atmel ID	5V	H	L	H	H	L	L	L	L	L	1EH	0000	00H
Read Device ID	5V	H	L	H	H	L	L	L	L	L	51H	0001	00H
Read Device ID	5V	H	L	H	H	L	L	L	L	L	06H	0010	00H

Notes:
1. Each $\overline{\text{PROG}}$ pulse is 200 ns - 500 ns for Chip Erase.
2. Each $\overline{\text{PROG}}$ pulse is 200 ns - 500 ns for Write Code Data.
3. Each $\overline{\text{PROG}}$ pulse is 200 ns - 500 ns for Write Lock Bits.
4. RDY/$\overline{\text{BSY}}$ signal is output on P3.0 during programming.
5. X = don't care.

Figure 17-1. Programming the Flash Memory (Parallel Mode)

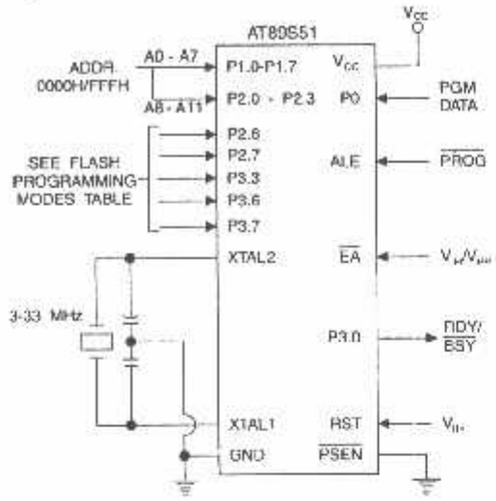
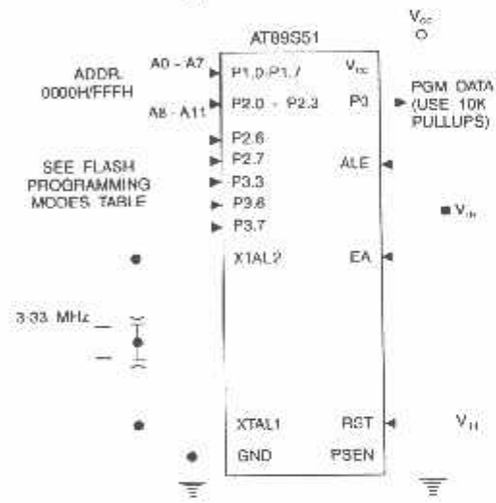


Figure 17-2. Verifying the Flash Memory (Parallel Mode)

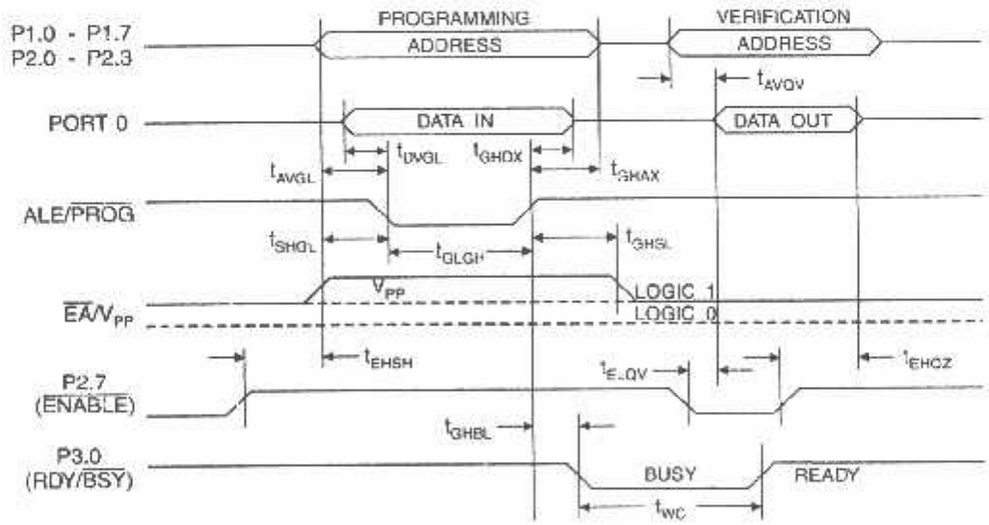


8. Flash Programming and Verification Characteristics (Parallel Mode)

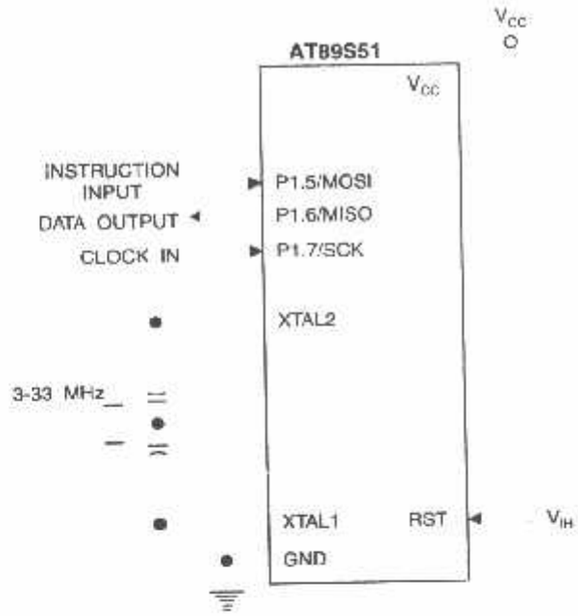
T_A = 20°C to 30°C, V_{CC} = 4.5 to 5.5V

Symbol	Parameter	Min	Max	Units
V_{PP}	Programming Supply Voltage	11.5	12.5	V
I_{PP}	Programming Supply Current		10	mA
I_{CC}	V_{CC} Supply Current		30	mA
$1/t_{CLCL}$	Oscillator Frequency	3	33	MHz
t_{AVGL}	Address Setup to $\overline{PROG}$ Low	48 t_{CLCL}		
t_{GHAX}	Address Hold After $\overline{PROG}$	48 t_{CLCL}		
t_{DVGL}	Data Setup to $\overline{PROG}$ Low	48 t_{CLCL}		
t_{GHDX}	Data Hold After $\overline{PROG}$	48 t_{CLCL}		
t_{EHSH}	P2.7 ($\overline{ENABLE}$) High to V_{PP}	48 t_{CLCL}		
t_{SHGL}	V_{PP} Setup to $\overline{PROG}$ Low	10		µs
t_{GHSL}	V_{PP} Hold After $\overline{PROG}$	10		µs
t_{GLGH}	$\overline{PROG}$ Width	0.2	1	µs
t_{AVQV}	Address to Data Valid		48t_{CLCL}	
t_{ELQV}	$\overline{ENABLE}$ Low to Data Valid		48t_{CLCL}	
t_{EHQZ}	Data Float After $\overline{ENABLE}$	0	48t_{CLCL}	
t_{GHBL}	$\overline{PROG}$ High to $\overline{BUSY}$ Low		1.0	µs
t_{WC}	Byte Write Cycle Time		50	µs

Figure 18-1. Flash Programming and Verification Waveforms – Parallel Mode

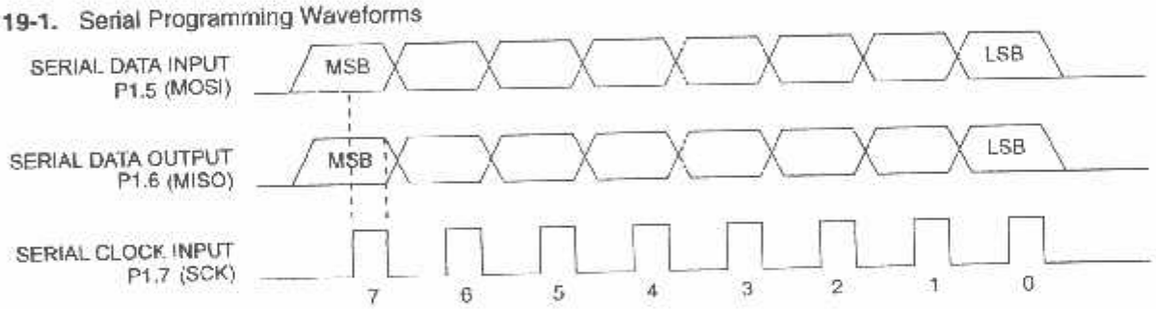


gure 18-2. Flash Memory Serial Downloading



9. Flash Programming and Verification Waveforms – Serial Mode

Igure 19-1. Serial Programming Waveforms



0. Serial Programming Instruction Set

nstruction	Instruction Format				Operation
	Byte 1	Byte 2	Byte 3	Byte 4	
'rogramming Enable	1010 1100	0101 0011	xxxx xxxx	xxxx xxxx 0110 1001 (Output on MISO)	Enable Serial Programming while RST is high
:hip Erase	1010 1100	100x xxxx	xxxx xxxx	xxxx xxxx	Chip Erase Flash memory array
lead Program Memory Byte Mode)	0010 0000	xxxx A11 A10 A9 A8	A7 A6 A5 A4 A3 A2 A1 A0	D7 D6 D5 D4 D3 D2 D1 D0	Read data from Program memory in the byte mode
Vrite Program Memory Byte Mode)	0100 0000	xxxx A11 A10 A9 A8	A7 A6 A5 A4 A3 A2 A1 A0	D7 D6 D5 D4 D3 D2 D1 D0	Write data to Program memory in the byte mode
Vrite Lock Bits[1]	1010 1100	1110 00 B1 B2	xxxx xxxx	xxxx xxxx	Write Lock bits. See Note (1).
lead Lock Bits	0010 0100	xxxx xxxx	xxxx xxxx	xx LB3 LB2 LB1 xx	Read back current status of the lock bits (a programmed lock bit reads back as a "1")
lead Signature Bytes	0010 1000	xxxx A11 A10 A9 A8	A7 xxx xxx0	Signature Byte	Read Signature Byte
Read Program Memory (Page Mode)	0011 0000	xxxx A11 A10 A9 A8	Byte 0	Byte 1... Byte 255	Read data from Program memory in the Page Mode (256 bytes)
Write Program Memory (Page Mode)	0101 0000	xxxx A11 A10 A9 A8	Byte 0	Byte 1... Byte 255	Write data to Program memory in the Page Mode (256 bytes)

ole: 1. B1 = 0, B2 = 0 → Mode 1, no lock protection
B1 = 0, B2 = 1 → Mode 2, lock bit 1 activated
B1 = 1, B2 = 0 → Mode 3, lock bit 2 activated
B1 = 1, B2 = 1 → Mode 4, lock bit 3 activated

} Each of the lock bit modes need to be activated sequentially before Mode 4 can be executed.

fter Reset signal is high, SCK should be low for at least 64 system clocks before it goes high to clock in the enable data ytes. No pulsing of Reset signal is necessary. SCK should be no faster than 1/16 of the system clock at XTAL1.

or Page Read/Write, the data always starts from byte 0 to 255. After the command byte and upper address byte are atched, each byte thereafter is treated as data until all 256 bytes are shifted in/out. Then the next instruction will be ready o be decoded.

23. DC Characteristics

The values shown in this table are valid for T_A = -40°C to 85°C and V_{CC} = 4.0V to 5.5V, unless otherwise noted.

Symbol	Parameter	Condition	Min	Max	Units
V_{IL}	Input Low Voltage	(Except $\overline{EA}$)	-0.5	0.2 V_{CC}-0.1	V
V_{IL1}	Input Low Voltage ($\overline{EA}$)		-0.5	0.2 V_{CC}-0.3	V
V_{IH}	Input High Voltage	(Except XTAL1, RST)	0.2 V_{CC}+0.9	V_{CC}+0.5	V
V_{IH1}	Input High Voltage	(XTAL1, RST)	0.7 V_{CC}	V_{CC}+0.5	V
V_{OL}	Output Low Voltage[1] (Ports 1,2,3)	I_{OL} = 1.6 mA		0.45	V
V_{OL1}	Output Low Voltage[1] (Port 0, ALE, $\overline{PSEN}$)	I_{OL} = 3.2 mA		0.45	V
V_{OH}	Output High Voltage (Ports 1,2,3, ALE, $\overline{PSEN}$)	I_{OH} = -60 µA, V_{CC} = 5V ± 10%	2.4		V
		I_{OH} = -25 µA	0.75 V_{CC}		V
		I_{OH} = -10 µA	0.9 V_{CC}		V
V_{OH1}	Output High Voltage (Port 0 in External Bus Mode)	I_{OH} = -800 µA, V_{CC} = 5V ± 10%	2.4		V
		I_{OH} = -300 µA	0.75 V_{CC}		V
		I_{OH} = -80 µA	0.9 V_{CC}		V
I_{IL}	Logical 0 Input Current (Ports 1,2,3)	V_{IN} = 0.45V		-50	µA
I_{TL}	Logical 1 to 0 Transition Current (Ports 1,2,3)	V_{IN} = 2V, V_{CC} = 5V ± 10%		-300	µA
I_{LI}	Input Leakage Current (Port 0, $\overline{EA}$)	0.45 < V_{IN} < V_{CC}		±10	µA
RRST	Reset Pulldown Resistor		50	300	KΩ
C_{IO}	Pin Capacitance	Test Freq. = 1 MHz, T_A = 25°C		10	pF
I_{CC}	Power Supply Current	Active Mode, 12 MHz		25	mA
		Idle Mode, 12 MHz		6.5	mA
	Power-down Mode[2]	V_{CC} = 5.5V		50	µA

Notes:
1. Under steady state (non-transient) conditions, I_{OL} must be externally limited as follows:
   Maximum I_{OL} per port pin: 10 mA
   Maximum I_{OL} per 8-bit port:
   Port 0: 26 mA Ports 1, 2, 3: 15 mA
   Maximum total I_{OL} for all output pins: 71 mA
   If I_{OL} exceeds the test condition, V_{OL} may exceed the related specification. Pins are not guaranteed to sink current greater than the listed test conditions.
2. Minimum V_{CC} for Power-down is 2V.

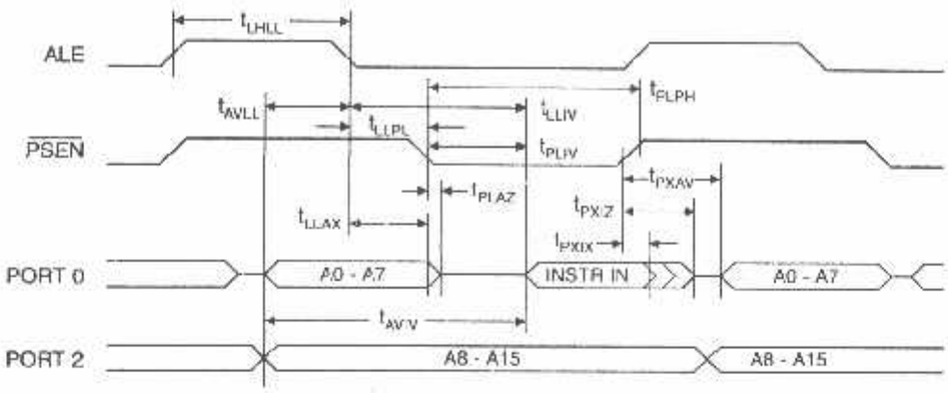
4. AC Characteristics

Under operating conditions, load capacitance for Port 0, ALE/$\overline{PROG}$, and $\overline{PSEN}$ = 100 pF; load capacitance for all other outputs = 80 pF.

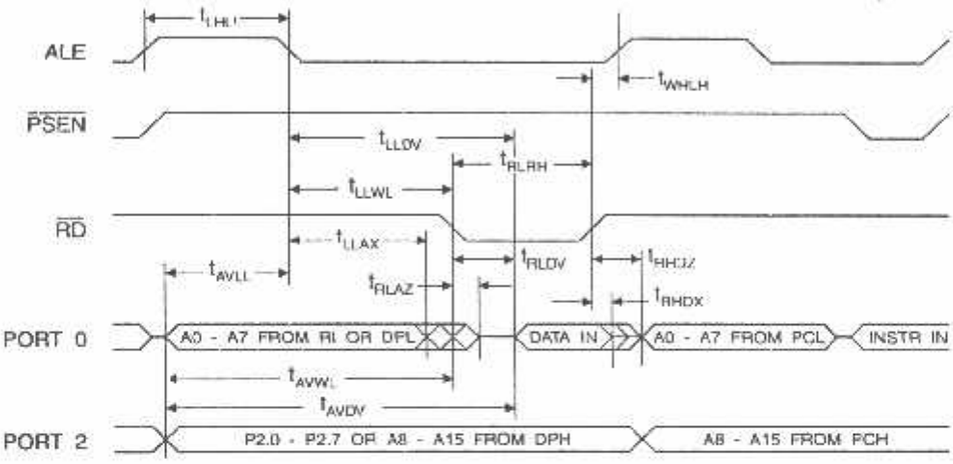
4.1 External Program and Data Memory Characteristics

Symbol	Parameter	12 MHz Oscillator		Variable Oscillator		Units
		Min	Max	Min	Max	
$1/t_{CLCL}$	Oscillator Frequency			0	33	MHz
t_{LHLL}	ALE Pulse Width	127		$2\,t_{CLCL}$-40		ns
t_{AVLL}	Address Valid to ALE Low	43		t_{CLCL}-25		ns
t_{LLAX}	Address Hold After ALE Low	48		t_{CLCL}-25		ns
t_{LLIV}	ALE Low to Valid Instruction In		233		$4\,t_{CLCL}$-65	ns
t_{LLPL}	ALE Low to $\overline{PSEN}$ Low	43		t_{CLCL}-25		ns
t_{PLPH}	$\overline{PSEN}$ Pulse Width	205		$3\,t_{CLCL}$-45		ns
t_{PLIV}	$\overline{PSEN}$ Low to Valid Instruction In		145		$3\,t_{CLCL}$-60	ns
t_{PXIX}	Input Instruction Hold After $\overline{PSEN}$	0		0		ns
t_{PXIZ}	Input Instruction Float After $\overline{PSEN}$		59		t_{CLCL}-25	ns
t_{PXAV}	$\overline{PSEN}$ to Address Valid	75		t_{CLCL}-8		ns
t_{AVIV}	Address to Valid Instruction In		312		$5\,t_{CLCL}$-80	ns
t_{PLAZ}	$\overline{PSEN}$ Low to Address Float		10		10	ns
t_{RLRH}	$\overline{RD}$ Pulse Width	400		$6\,t_{CLCL}$-100		ns
t_{WLWH}	$\overline{WR}$ Pulse Width	400		$6\,t_{CLCL}$-100		ns
t_{RLDV}	$\overline{RD}$ Low to Valid Data In		252		$5\,t_{CLCL}$-90	ns
t_{RHDX}	Data Hold After $\overline{RD}$	0		0		ns
t_{RHDZ}	Data Float After $\overline{RD}$		97		$2\,t_{CLCL}$-28	ns
t_{LLDV}	ALE Low to Valid Data In		517		$8\,t_{CLCL}$-150	ns
t_{AVDV}	Address to Valid Data In		585		$9\,t_{CLCL}$-165	ns
t_{LLWL}	ALE Low to $\overline{RD}$ or $\overline{WR}$ Low	200	300	$3\,t_{CLCL}$-50	$3\,t_{CLCL}$+50	ns
t_{AVWL}	Address to $\overline{RD}$ or $\overline{WR}$ Low	203		$4\,t_{CLCL}$-75		ns
t_{QVWX}	Data Valid to $\overline{WR}$ Transition	23		t_{CLCL}-30		ns
t_{QVWH}	Data Valid to $\overline{WR}$ High	433		$7\,t_{CLCL}$-130		ns
t_{WHQX}	Data Hold After $\overline{WR}$	33		t_{CLCL}-25		ns
t_{RLAZ}	$\overline{RD}$ Low to Address Float		0		0	ns
t_{WHLH}	$\overline{RD}$ or $\overline{WR}$ High to ALE High	43	123	t_{CLCL}-25	t_{CLCL}+25	ns

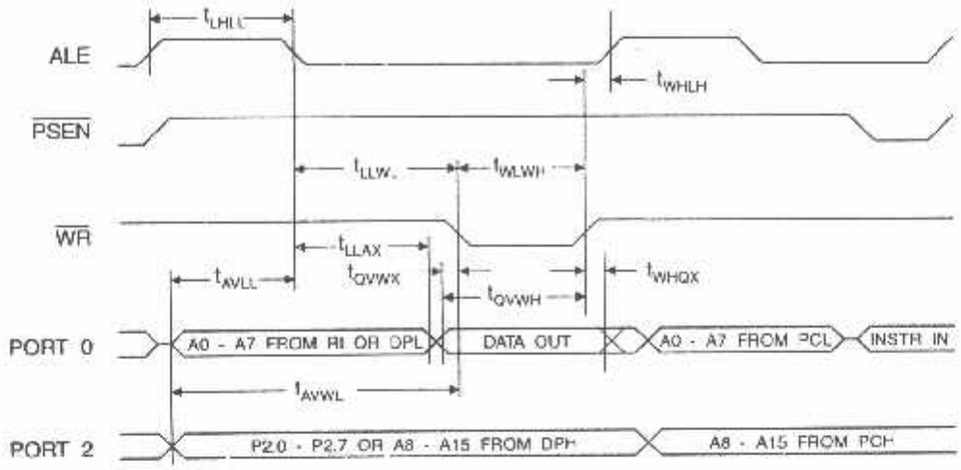
25. External Program Memory Read Cycle



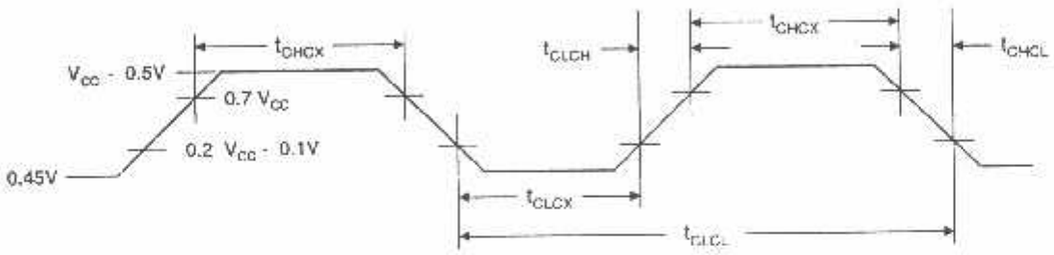
26. External Data Memory Read Cycle



7. External Data Memory Write Cycle



8. External Clock Drive Waveforms



9. External Clock Drive

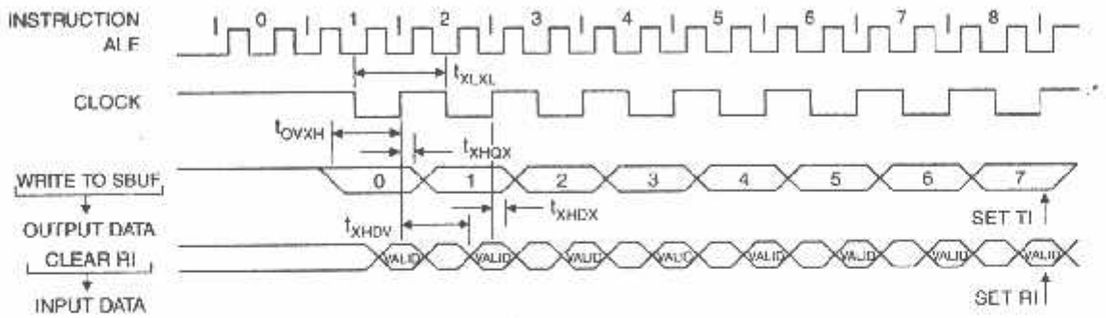
Symbol	Parameter	Min	Max	Units
$1/t_{CLCL}$	Oscillator Frequency	0	33	MHz
t_{CLCL}	Clock Period	30		ns
t_{CHCX}	High Time	12		ns
t_{CLCX}	Low Time	12		ns
t_{CLCH}	Rise Time		5	ns
t_{CHCL}	Fall Time		5	ns

0. Serial Port Timing: Shift Register Mode Test Conditions

he values in this table are valid for V_{CC} = 4.0V to 5.5V and Load Capacitance = 80 pF.

Symbol	Parameter	12 MHz Osc		Variable Oscillator		Units
		Min	Max	Min	Max	
XLXL	Serial Port Clock Cycle Time	1.0		12 t_{CLCL}		µs
QVXH	Output Data Setup to Clock Rising Edge	700		10 t_{CLCL}-133		ns
XHQX	Output Data Hold After Clock Rising Edge	50		2 t_{CLCL}-80		ns
XHDX	Input Data Hold After Clock Rising Edge	0		0		ns
XHDV	Clock Rising Edge to Input Data Valid		700		10 t_{CLCL}-133	ns

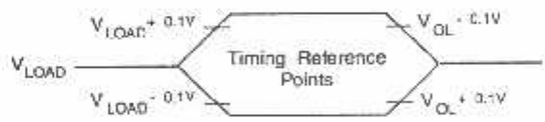
1. Shift Register Mode Timing Waveforms



2. AC Testing Input/Output Waveforms[1]

lote: 1. AC Inputs during testing are driven at V_{CC} - 0.5V for a logic 1 and 0.45V for a logic 0. Timing measurements are made at V_{IH} min. for a logic 1 and V_{IL} max. for a logic 0.

3. Float Waveforms[1]



lote: 1. For timing purposes, a port pin is no longer floating when a 100 mV change from load voltage occurs. A port pin begins to float when a 100 mV change from the loaded V_{OH}/V_{OL} level occurs.

March 1998

National Semiconductor

LM158/LM258/LM358/LM2904
Low Power Dual Operational Amplifiers

General Description

The LM158 series consists of two independent, high gain, internally frequency compensated operational amplifiers which were designed specifically to operate from a single power supply over a wide range of voltages. Operation from split power supplies is also possible and the low power supply current drain is independent of the magnitude of the power supply voltage.

Application areas include transducer amplifiers, dc gain blocks and all the conventional op amp circuits which now can be more easily implemented in single power supply systems. For example, the LM158 series can be directly operated off of the standard +5V power supply voltage which is used in digital systems and will easily provide the required interface electronics without requiring the additional ±15V power supplies.

Unique Characteristics

- In the linear mode the input common-mode voltage range includes ground and the output voltage can also swing to ground, even though operated from only a single power supply voltage.
- The unity gain cross frequency is temperature compensated.
- The input bias current is also temperature compensated.

Advantages

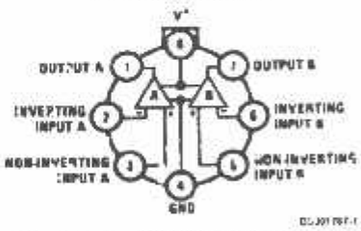
- Two internally compensated op amps in a single package
- Eliminates need for dual supplies
- Allows directly sensing near GND and V_{OUT} also goes to GND
- Compatible with all forms of logic
- Power drain suitable for battery operation
- Pin-out same as LM1558/LM1458 dual operational amplifier

Features

- Internally frequency compensated for unity gain
- Large dc voltage gain: 100 dB
- Wide bandwidth (unity gain): 1 MHz (temperature compensated)
- Wide power supply range:
  - Single supply: 3V to 32V
  - or dual supplies: ±1.5V to ±16V
- Very low supply current drain (500 µA) — essentially independent of supply voltage
- Low input offset voltage: 2 mV
- Input common-mode voltage range includes ground
- Differential input voltage range equal to the power supply voltage
- Large output voltage swing: 0V to V+ − 1.5V

Connection Diagrams (Top Views)

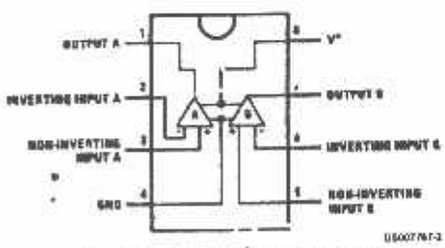
Metal Can Package



DS007787-1

Order Number LM158AH, LM158AH/883 (Note 1), LM158H, LM158H/883 (Note 1), LM258H or LM358H
See NS Package Number H08C

DIP/SO Package



DS007787-2

Order Number LM158J, LM158J/883 (Note 1), LM158AJ or LM158AJ/883 (Note 1)
See NS Package Number J08A
Order Number LM358M, LM358AM or LM2904M
See NS Package Number M08A
Order Number LM358AN, LM358N or LM2904N
See NS Package Number N08E

Note 1: LM158 is available per SMD #5962-8771301
LM158A is available per SMD #5962-8771002

Electrical Characteristics

V^+ = +5.0V, unless otherwise stated

Parameter	Conditions	LM358			LM2904			Units
		Min	Typ	Max	Min	Typ	Max	
Input Offset Voltage	(Note 6), T_A = 25°C		2	7		2	7	mV
Input Bias Current	$I_{IN(+)}$ or $I_{IN(-)}$, T_A = 25°C, V_{CM} = 0V, (Note 7)		45	250		45	250	nA
Input Offset Current	$I_{IN(+)} - I_{IN(-)}$, V_{CM} = 0V, T_A = 25°C		5	50		5	50	nA
Input Common-Mode Voltage Range	V^+ = 30V, (Note 8) (LM2904, V^+ = 26V), T_A = 25°C	0		$V^+-1.5$	0		$V^+-1.5$	V
Supply Current	Over Full Temperature Range $R_L = \infty$ on All Op Amps							
	V^+ = 30V (LM2904 V^+ = 26V)		1	2		1	2	mA
	V^+ = 5V		0.5	1.2		0.5	1.2	mA

Electrical Characteristics

V^+ = +5.0V, (Note 5), unless otherwise stated

Parameter		Conditions	LM158A			LM358A			LM158/LM258			Units
			Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
Large Signal Voltage Gain		V^+ = 15V, T_A = 25°C, $R_L \geq 2$ kΩ, (For V_O = 1V to 11V)	50	100		25	100		50	100		V/mV
Common-Mode Rejection Ratio		T_A = 25°C, V_{CM} = 0V to $V^+-1.5$V	70	85		65	85		70	85		dB
Power Supply Rejection Ratio		V^+ = 5V to 30V (LM2904, V^+ = 5V to 26V), T_A = 25°C	65	100		65	100		65	100		dB
Amplifier-to-Amplifier Coupling		f = 1 kHz to 20 kHz, T_A = 25°C (Input Referred), (Note 9)		−120			−120			−120		dB
Output Current	Source	V_{IN}^+ = 1V, V_{IN}^- = 0V, V^+ = 15V, V_O = 2V, T_A = 25°C	20	40		20	40		20	40		mA
	Sink	V_{IN}^- = 1V, V_{IN}^+ = 0V, V^+ = 15V, T_A = 25°C, V_O = 2V	10	20		10	20		10	20		mA
		V_{IN}^- = 1V, V_{IN}^+ = 0V, T_A = 25°C, V_O = 200 mV, V^+ = 15V	12	50		12	50		12	50		µA
Short Circuit to Ground		T_A = 25°C, (Note 3), V^+ = 15V		40	60		40	60		40	60	mA
Input Offset Voltage		(Note 6)			4			5			7	mV
Input Offset Voltage Drift		R_S = 0Ω		7	15		7	20		7		µV/°C
Input Offset Current		$I_{IN(+)} - I_{IN(-)}$			30			75			100	nA
Input Offset Current Drift		R_S = 0Ω		10	200		10	300		10		pA/°C
Input Bias Current		$I_{IN(+)}$ or $I_{IN(-)}$		40	100		40	200		40	300	nA
Input Common-Mode Voltage Range		V^+ = 30 V, (Note 8) (LM2904, V^+ = 26V)	0		V^+-2	0		V^+-2	0		V^+-2	V

Electrical Characteristics (Continued)

V^+ = +5.0V, (Note 5), unless otherwise stated

Parameter		Conditions		LM158A			LM358A			LM158/LM258			Units
				Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
Large Signal Voltage Gain		V^+ = +15V (V_O = 1V to 11V) $R_L \geq 2\ k\Omega$		25			15			25			V/mV
Output Voltage Swing	V_{OH}	V^+ = +30V	R_L = 2 kΩ	26			26			26			V
		(V^+ = 26V)	R_L = 10 kΩ	27	28		27	28		27	28		V
	V_{OL}	V^+ = 5V, R_L = 10 kΩ			5	20		5	20		5	20	mV
Output Current	Source	V_{IN}^+ = +1V, V_{IN}^- = 0V, V^+ = 15V, V_O = 2V		10	20		10	20		10	20		mA
	Sink	V_{IN}^- = +1V, V_{IN}^+ = 0V, V^+ = 15V, V_O = 2V		10	15		5	8		5	8		mA

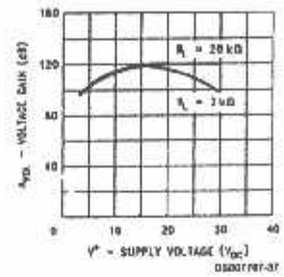
Electrical Characteristics

V^+ = +5.0V, (Note 5), unless otherwise stated

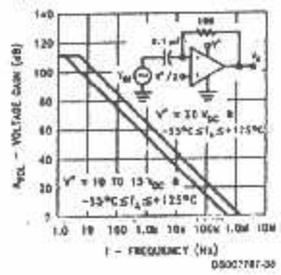
Parameter		Conditions	LM358			LM2904			Units
			Min	Typ	Max	Min	Typ	Max	
Large Signal Voltage Gain		V^+ = 15V, T_A = 25°C, $R_L \geq 2\ k\Omega$, (For V_O = 1V to 11V)	25	100		25	100		V/mV
Common-Mode Rejection Ratio		T_A = 25°C, V_{CM} = 0V to V^+−1.5V	65	85		50	70		dB
Power Supply Rejection Ratio		V^+ = 5V to 30V (LM2904, V^+ = 5V to 26V), T_A = 25°C	65	100		50	100		dB
Amplifier-to-Amplifier Coupling		f = 1 kHz to 20 kHz, T_A = 25°C (Input Referred), (Note 9)		−120			−120		dB
Output Current	Source	V_{IN}^+ = 1V, V_{IN}^- = 0V, V^+ = 15V, V_O = 2V, T_A = 25°C	20	40		20	40		mA
	Sink	V_{IN}^- = 1V, V_{IN}^+ = 0V V^+ = 15V, T_A = 25°C, V_O = 2V	10	20		10	20		mA
		V_{IN}^- = 1V, V_{IN}^+ = 0V T_A = 25°C, V_O = 200 mV, V^+ = 15V	12	50		12	50		µA
Short Circuit to Ground		T_A = 25°C, (Note 3), V^+ = 15V		40	60		40	60	mA
Input Offset Voltage		(Note 6)			9			10	mV
Input Offset Voltage Drift		R_S = 0Ω		7			7		µV/°C
Input Offset Current		$I_{IN(+)} - I_{IN(-)}$			150		45	200	nA
Input Offset Current Drift		R_S = 0Ω		10			10		pA/°C
Input Bias Current		$I_{IN(+)}$ or $I_{IN(-)}$		40	500		40	500	nA
Input Common-Mode Voltage Range		V^+ = 30 V, (Note 8) (LM2904, V^+ = 26V)	0		V^+−2	0		V^+ −2	V

Typical Performance Characteristics (Continued)

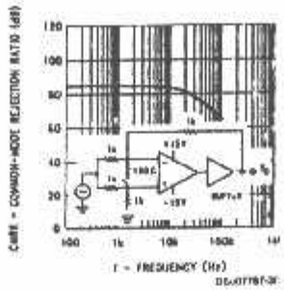
Voltage Gain



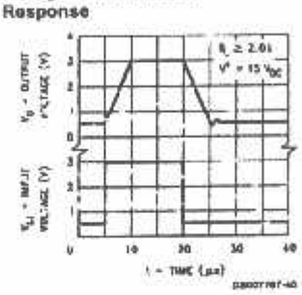
Open Loop Frequency Response



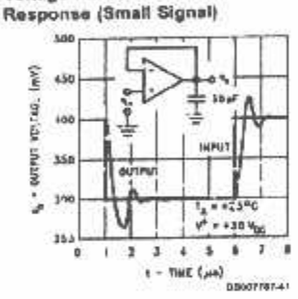
Common-Mode Rejection Ratio



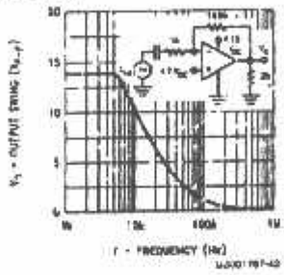
Voltage Follower Pulse Response



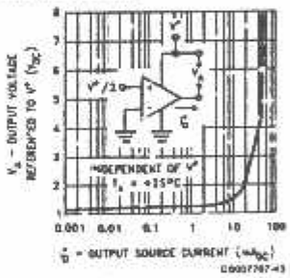
Voltage Follower Pulse Response (Small Signal)



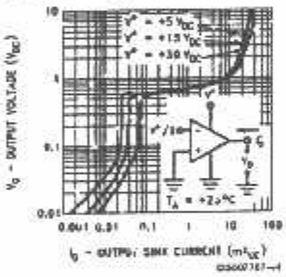
Large Signal Frequency Response



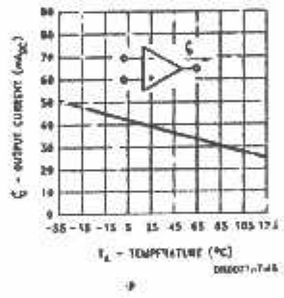
Output Characteristics Current Sourcing



Output Characteristics Current Sinking

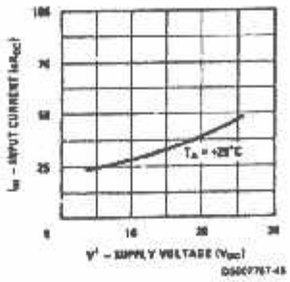


Current Limiting

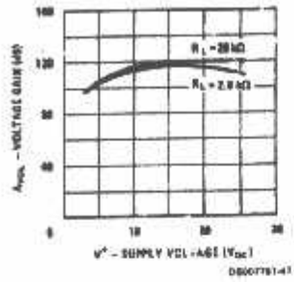


Typical Performance Characteristics (Continued)

Input Current (LM2902 only)



Voltage Gain (LM2902 only)



Application Hints

The LM158 series are op amps which operate with only a single power supply voltage, have true-differential inputs, and remain in the linear mode with an input common mode voltage of 0 V_{DC}. These amplifiers operate over a wide range of power supply voltage with little change in performance characteristics. At 25°C amplifier operation is possible down to a minimum supply voltage of 2.3 V_{DC}.

Precautions should be taken to insure that the power supply for the integrated circuit never becomes reversed in polarity or that the unit is not inadvertently installed backwards in a test socket as an unlimited current surge through the resulting forward diode within the IC could cause fusing of the internal conductors and result in a destroyed unit.

Large differential input voltages can be easily accomodated and, as input differential voltage protection diodes are not needed, no large input currents result from large differential input voltages. The differential input voltage may be larger than V+ without damaging the device. Protection should be provided to prevent the input voltages from going negative more than −0.3 V_{DC} (at 25°C). An input clamp diode with a resistor to the IC input terminal can be used.

To reduce the power supply current drain, the amplifiers have a class A output stage for small signal levels which converts to class B in a large signal mode. This allows the amplifiers to both source and sink large output currents. Therefore both NPN and PNP external current boost transistors can be used to extend the power capability of the basic amplifiers. The output voltage needs to raise approximately 1 diode drop above ground to bias the on-chip vertical PNP transistor for output current sinking applications.

For ac applications, where the load is capacitively coupled to the output of the amplifier, a resistor should be used, from the output of the amplifier to ground to increase the class A bias current and prevent crossover distortion. Where the load is directly coupled, as in dc applications, there is no crossover distortion.

Capacitive loads which are applied directly to the output of the amplifier reduce the loop stability margin. Values of 50 pF can be accomodated using the worst-case non-inverting unity gain connection. Large closed loop gains or resistive isolation should be used if larger load capacitance must be driven by the amplifier.

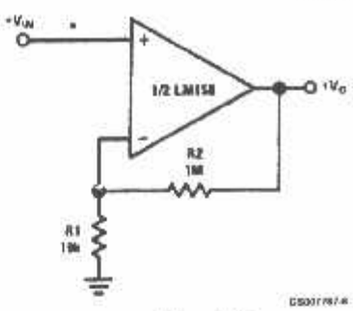
The bias network of the LM158 establishes a drain current which is independent of the magnitude of the power supply voltage over the range of 3 V_{DC} to 30 V_{DC}.

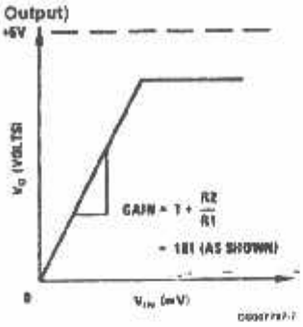
Output short circuits either to ground or to the positive power supply should be of short time duration. Units can be destroyed, not as a result of the short circuit current causing metal fusing, but rather due to the large increase in IC chip dissipation which will cause eventual failure due to excessive function temperatures. Putting direct short-circuits on more than one amplifier at a time will increase the total IC power dissipation to destructive levels, if not properly protected with external dissipation limiting resistors in series with the output leads of the amplifiers. The larger value of output source current which is available at 25°C provides a larger output current capability at elevated temperatures (see typical performance characteristics) than a standard IC op amp.

The circuits presented in the section on typical applications emphasize operation on only a single power supply voltage. If complementary power supplies are available, all of the standard op amp circuits can be used. In general, introducing a pseudo-ground (a bias voltage reference of V+/2) will allow operation above and below this value in single power supply systems. Many application circuits are shown which take advantage of the wide input common-mode voltage range which includes ground. In most cases, input biasing is not required and input voltages which range to ground can easily be accommodated.

Typical Single-Supply Applications ($V^+ = 5.0\ V_{DC}$)

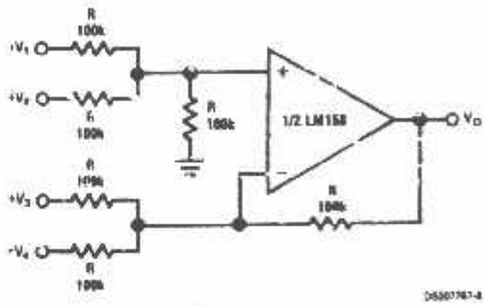
Non-Inverting DC Gain (0V Output)





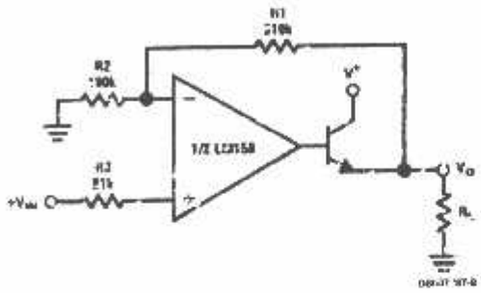
*R not needed due to temperature independent I_{IN}

DC Summing Amplifier
(V_{IN}'s ≥ 0 V_{DC} and V_O ≥ 0 V_{DC})



Where: $V_O = V_1 + V_2 + V_3 + V_4$
$(V_1 + V_2) \geq (V_3 + V_4)$ to keep $V_O \geq 0\ V_{DC}$

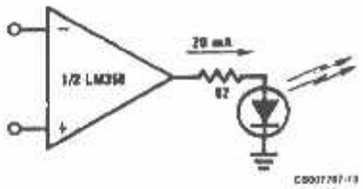
Power Amplifier



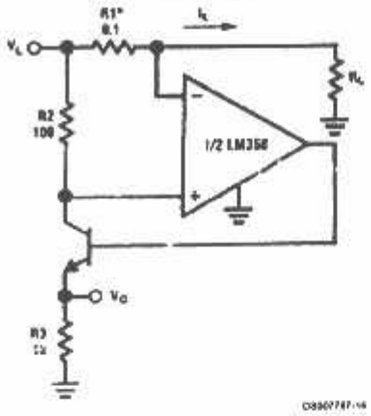
$V_O = 0\ V_{DC}$ for $V_{IN} = 0\ V_{DC}$
$A_V = 10$

Typical Single-Supply Applications ($V^+ = 5.0\ V_{DC}$) (Continued)

LED Driver



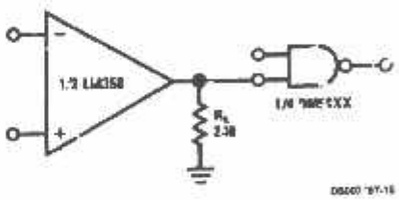
Current Monitor



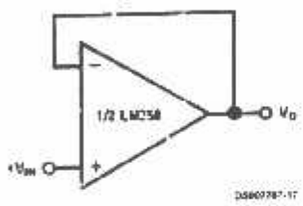
$$V_O = \frac{1V\ (I_L)}{1A}$$

*(Increase R1 for I_L small)
$V_L \leq V^+ - 2V$

Driving TTL

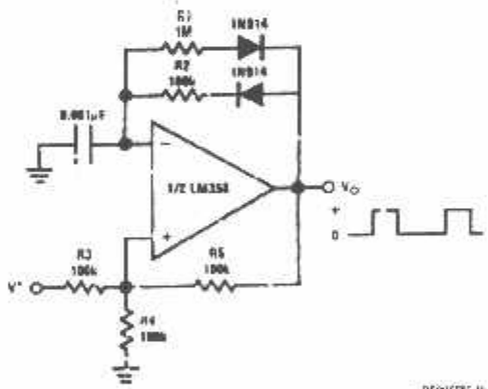


Voltage Follower



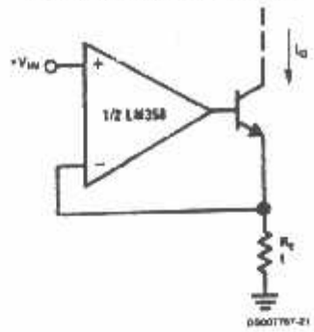
$V_O = V_{IN}$

Pulse Generator



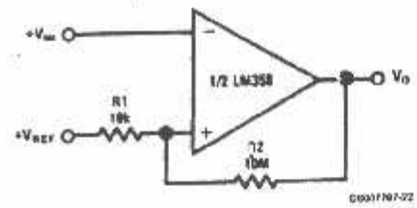
Typical Single-Supply Applications (V^+ = 5.0 V_{DC}) (Continued)

High Compliance Current Sink

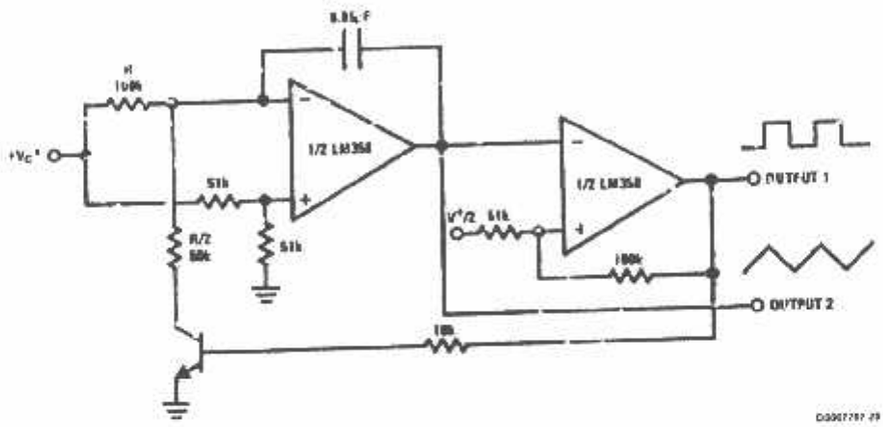


I_O = 1 amp/volt V_{IN}
(Increase R_E for I_O small)

Comparator with Hysteresis



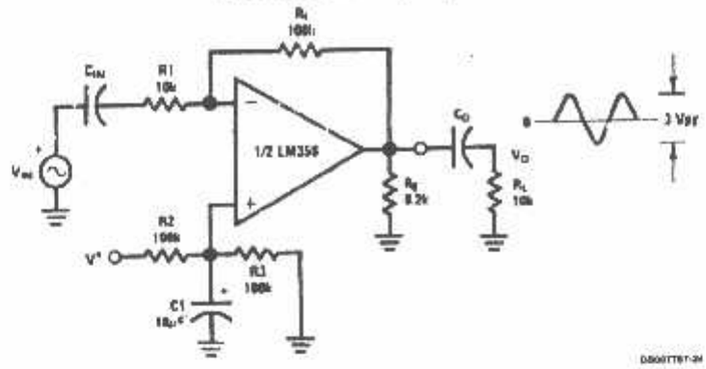
Voltage Controlled Oscillator (VCO)



*WIDE CONTROL VOLTAGE RANGE: 0 $V_{DC} \leq V_C \leq 2$ ($V^+ - 1.5V_{DC}$)

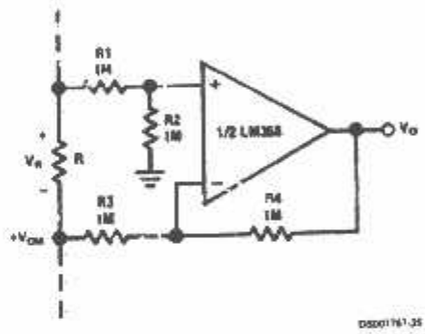
Typical Single-Supply Applications ($V^+ = 5.0\ V_{DC}$) (Continued)

AC Coupled Inverting Amplifier



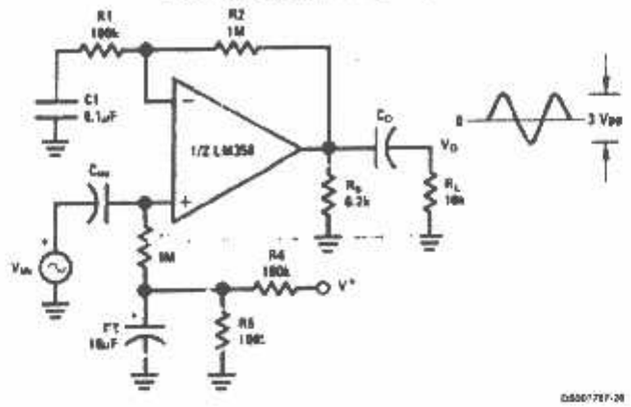
$$A_V = -\frac{R_f}{R1} \quad \text{(As shown, } A_V = 10\text{)}$$

Ground Referencing a Differential Input Signal



Typical Single-Supply Applications (V^+ = 5.0 V_{DC}) (Continued)

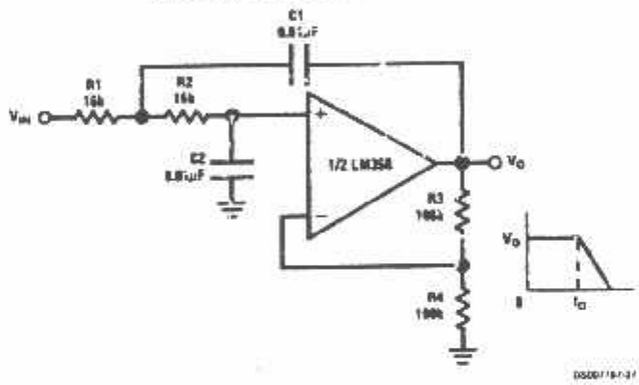
AC Coupled Non-Inverting Amplifier



$$A_V = 1 + \frac{R2}{R1}$$

A_V = 11 (As Shown)

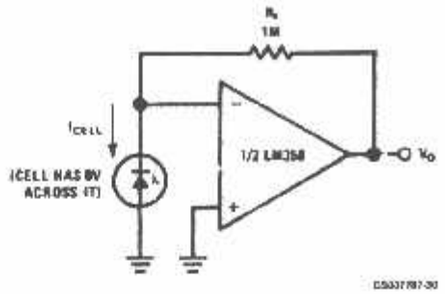
DC Coupled Low-Pass RC Active Filter



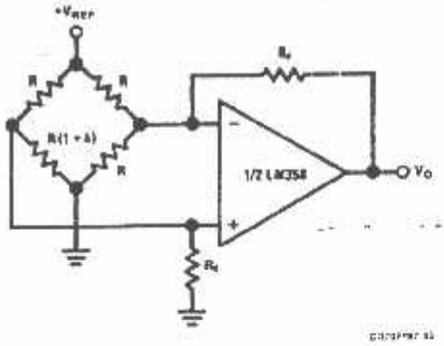
f_O = 1 kHz
Q = 1
A_V = 2

Typical Single-Supply Applications (V^+ = 5.0 V_{DC}) (Continued)

Photo Voltaic-Cell Amplifier



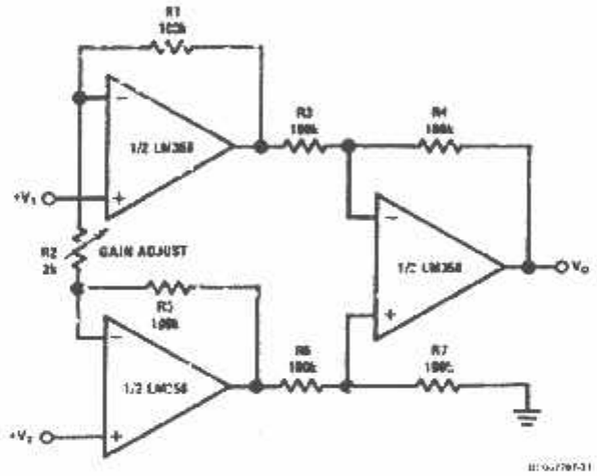
Bridge Current Amplifier



For $\delta << 1$ and $R_f >> R$

$$V_O \approx V_{REF}\left(\frac{\delta}{2}\right)\frac{R_f}{R}$$

High Input Z Adjustable-Gain DC Instrumentation Amplifier



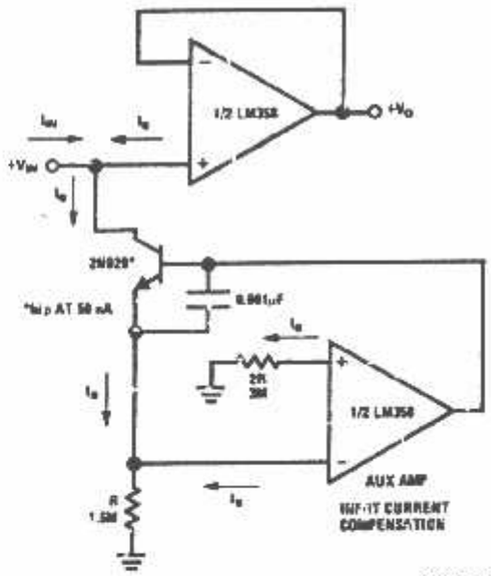
If R1 = R5 & R3 = R4 = R6 = R7 (CMRR depends on match)

$$V_O = 1 + \frac{2R1}{R2}(V_2 - V_1)$$

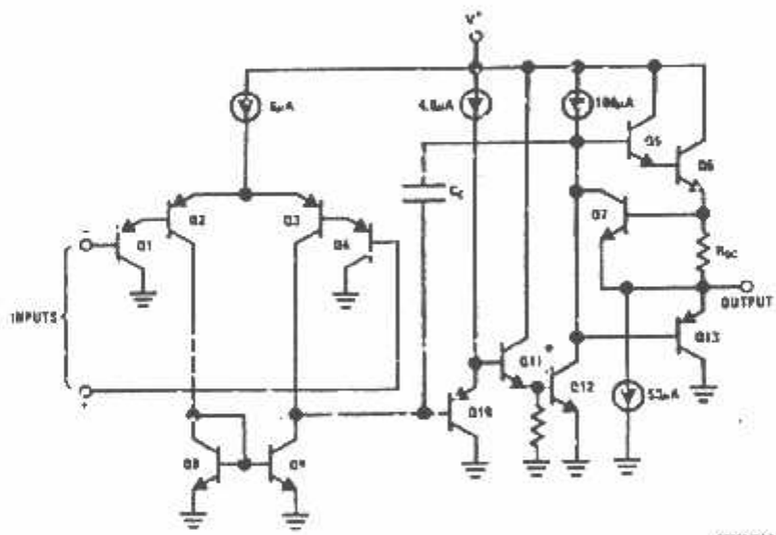
As shown $V_O = 101(V_2 - V_1)$

Typical Single-Supply Applications (V^+ = 5.0 V_{DC}) (Continued)

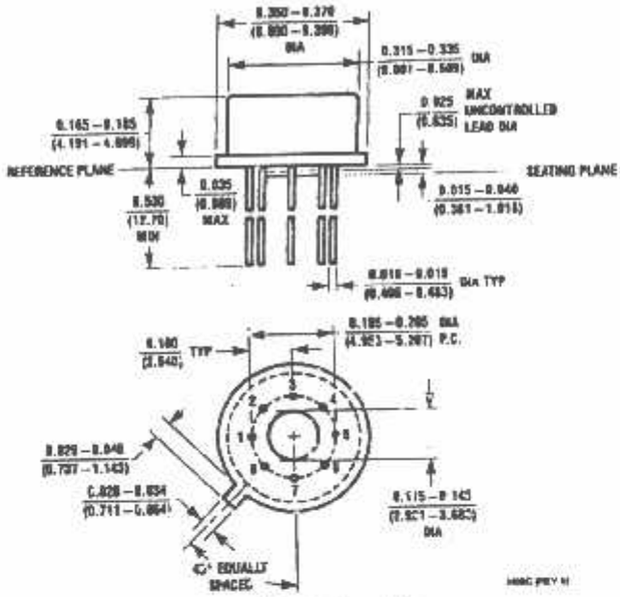
Using Symmetrical Amplifiers to Reduce Input Current (General Concept)



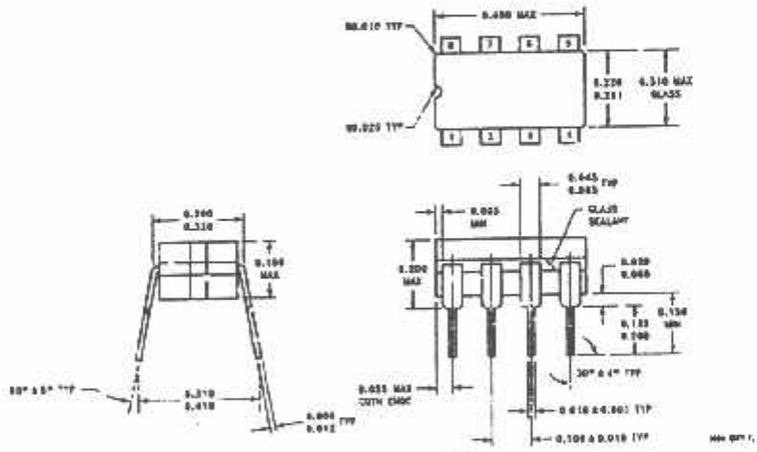
Schematic Diagram (Each Amplifier)



Physical Dimensions inches (millimeters) unless otherwise noted



Metal Can Package (H)
Order Number LM158AH, LM158AH/883, LM158H,
LM158H/883, LM258H or LM358H
NS Package Number H08C



Cerdip Package (J)
Order Number LM158J, LM158J/883, LM158AJ or LM158AJ/883
NS Package Number J08A

Notes

LIFE SUPPORT POLICY

NATIONAL'S PRODUCTS ARE NOT AUTHORIZED FOR USE AS CRITICAL COMPONENTS IN LIFE SUPPORT DEVICES OR SYSTEMS WITHOUT THE EXPRESS WRITTEN APPROVAL OF THE PRESIDENT OF NATIONAL SEMICONDUCTOR CORPORATION. As used herein:

1. Life support devices or systems are devices or systems which, (a) are intended for surgical implant into the body, or (b) support or sustain life, and whose failure to perform when properly used in accordance with instructions for use provided in the labeling, can be reasonably expected to result in a significant injury to the user.

2. A critical component is any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

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Absolute Maximum Ratings (Notes 1 & 2)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage (V_{CC}) (Note 3)	6.5V
Voltage	
Logic Control Inputs	−0.3V to +18V
At Other Input and Outputs	−0.3V to (V_{CC} +0.3V)
Lead Temp. (Soldering, 10 seconds)	
Dual-In-Line Package (plastic)	260°C
Dual-In-Line Package (ceramic)	300°C
Surface Mount Package	
Vapor Phase (60 seconds)	215°C
Infrared (15 seconds)	220°C
Storage Temperature Range	−65°C to +150°C
Package Dissipation at T_A = 25°C	875 mW
ESD Susceptibility (Note 10)	800V

Operating Ratings (Notes 1 & 2)

Temperature Range	$T_{MIN} \le T_A \le T_{MAX}$
ADC0801/02LJ, ADC0802LJ/883	$-55°C \le T_A \le +125°C$
ADC0801/02/03/04LCJ	$-40°C \le T_A \le +85°C$
ADC0801/02/03/05LCN	$-40°C \le T_A \le +85°C$
ADC0804LCN	$0°C \le T_A \le +70°C$
ADC0802/03/04LCV	$0°C \le T_A \le +70°C$
ADC0802/03/04LCWM	$0°C \le T_A \le +70°C$
Range of V_{CC}	4.5 V_{DC} to 6.3 V_{DC}

Electrical Characteristics

The following specifications apply for V_{CC} = 5 V_{DC}, $T_{MIN} \le T_A \le T_{MAX}$ and f_{CLK} = 640 kHz unless otherwise specified.

Parameter	Conditions	Min	Typ	Max	Units
ADC0801: Total Adjusted Error (Note 9)	With Full-Scale Adj. (See Section 2.5.2)			±¼	LSB
ADC0802: Total Unadjusted Error (Note 8)	$V_{REF}/2$ = 2.500 V_{DC}			±½	LSB
ADC0803: Total Adjusted Error (Note 8)	With Full-Scale Adj. (See Section 2.5.2)			±½	LSB
ADC0804: Total Unadjusted Error (Note 8)	$V_{REF}/2$ = 2.500 V_{DC}			±1	LSB
ADC0805: Total Unadjusted Error (Note 8)	$V_{REF}/2$ = No Connection			±1	LSB
$V_{REF}/2$ Input Resistance (Pin 9)	ADC0801/02/03/05 ADC0804 (Note 9)	2.5 0.75	8.0 1.1		kΩ kΩ
Analog Input Voltage Range	(Note 4) V(+) or V(−)	Gnd−0.05		V_{CC} +0.05	V_{DC}
DC Common-Mode Error	Over Analog Input Voltage Range		±1/16	±⅛	LSB
Power Supply Sensitivity	V_{CC} = 5 V_{DC} ±10% Over Allowed $V_{IN}(+)$ and $V_{IN}(-)$ Voltage Range (Note 4)		±1/16	±⅛	LSB

AC Electrical Characteristics

The following specifications apply for V_{CC} = 5 V_{DC} and T_A = 25°C unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Units
T_C	Conversion Time	f_{CLK} = 640 kHz (Note 6)	103		114	μs
T_C	Conversion Time	(Note 5, 6)	66		73	$1/f_{CLK}$
f_{CLK}	Clock Frequency Clock Duty Cycle	V_{CC} = 5V, (Note 5) (Note 5)	100 40	640	1460 60	kHz %
CR	Conversion Rate in Free-Running Mode	$\overline{INTR}$ tied to $\overline{WR}$ with $\overline{CS}$ = 0 V_{DC}, f_{CLK} = 640 kHz	8770		9708	conv/s
$t_{W(\overline{WR})L}$	Width of $\overline{WR}$ Input (Start Pulse Width)	$\overline{CS}$ = 0 V_{DC} (Note 7)	100			ns
t_{ACC}	Access Time (Delay from Falling Edge of $\overline{RD}$ to Output Data Valid)	C_L = 100 pF		135	200	ns
t_{1H}, t_{0H}	TRI-STATE Control (Delay from Rising Edge of $\overline{RD}$ to Hi-Z State)	C_L = 10 pF, R_L = 10k (See TRI-STATE Test Circuits)		125	200	ns
t_{WI}, t_{RI}	Delay from Falling Edge of $\overline{WR}$ or $\overline{RD}$ to Reset of $\overline{INTR}$			300	450	ns
C_{IN}	Input Capacitance of Logic Control Inputs			5	7.5	pF
C_{OUT}	TRI-STATE Output Capacitance (Data Buffers)			5	7.5	pF
CONTROL INPUTS [Note: CLK IN (Pin 4) is the input of a Schmitt trigger circuit and is therefore specified separately]						
V_{IN} (1)	Logical "1" Input Voltage (Except Pin 4 CLK IN)	V_{CC} = 5.25 V_{DC}	2.0		15	V_{DC}

AC Electrical Characteristics (Continued)

The following specifications apply for V_{CC} = 5V_{DC} and $T_{MIN} \le T_A \le T_{MAX}$, unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Units
CONTROL INPUTS [Note: CLK IN (Pin 4) is the input of a Schmitt trigger circuit and is therefore specified separately]						
V_{IN} (0)	Logical "0" Input Voltage (Except Pin 4 CLK IN)	V_{CC} = 4.75 V_{DC}			0.8	V_{DC}
I_{IN} (1)	Logical "1" Input Current (All Inputs)	V_{IN} = 5 V_{DC}		0.005	1	μA_{DC}
I_{IN} (0)	Logical "0" Input Current (All Inputs)	V_{IN} = 0 V_{DC}	−1	−0.005		μA_{DC}
CLOCK IN AND CLOCK R						
V_T+	CLK IN (Pin 4) Positive Going Threshold Voltage		2.7	3.1	3.5	V_{DC}
V_T-	CLK IN (Pin 4) Negative Going Threshold Voltage		1.5	1.8	2.1	V_{DC}
V_H	CLK IN (Pin 4) Hysteresis $(V_T+)-(V_T-)$		0.6	1.3	2.0	V_{DC}
V_{OUT} (0)	Logical "0" CLK R Output Voltage	I_O = 360 μA, V_{CC} = 4.75 V_{DC}			0.4	V_{DC}
V_{OUT} (1)	Logical "1" CLK R Output Voltage	I_O = −360 μA, V_{CC} = 4.75 V_{DC}	2.4			V_{DC}
DATA OUTPUTS AND $\overline{INTR}$						
V_{OUT} (0)	Logical "0" Output Voltage Data Outputs $\overline{INTR}$ Output	I_{OUT} = 1.6 mA, V_{CC} = 4.75 V_{DC} I_{OUT} = 1.0 mA, V_{CC} = 4.75 V_{DC}			0.4 0.4	V_{DC} V_{DC}
V_{OUT} (1)	Logical "1" Output Voltage	I_O = −360 μA, V_{CC} = 4.75 V_{DC}	2.4			V_{DC}
V_{OUT} (1)	Logical "1" Output Voltage	I_O = −10 μA, V_{CC} = 4.75 V_{DC}	4.5			V_{DC}
I_{OUT}	TRI-STATE Disabled Output Leakage (All Data Buffers)	V_{OUT} = 0 V_{DC} V_{OUT} = 5 V_{DC}	−3		3	μA_{DC} μA_{DC}
I_{SOURCE}		V_{OUT} Short to Gnd, T_A = 25°C	4.5	6		mA_{DC}
I_{SINK}		V_{OUT} Short to V_{CC}, T_A = 25°C	9.0	16		mA_{DC}
POWER SUPPLY						
I_{CC}	Supply Current (Includes Ladder Current) ADC0801/02/03/04LCJ/05 ADC0804LCN/LCV/LCWM	f_{CLK} = 640 kHz, $V_{REF}/2$ = NC, T_A = 25°C and $\overline{CS}$ = 5V		1.1 1.9	1.8 2.5	mA mA

Note 1: Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. DC and AC electrical specifications do not apply when operating the device beyond its specified operating conditions.

Note 2: All voltages are measured with respect to Gnd, unless otherwise specified. The separate A Gnd point should always be wired to the D Gnd.

Note 3: A zener diode exists, internally, from V_{CC} to Gnd and has a typical breakdown voltage of 7 V_{DC}.

Note 4: For $V_{IN}(-) \ge V_{IN}(+)$ the digital output code will be 0000 0000. Two on-chip diodes are tied to each analog input (see block diagram) which will forward conduct for analog input voltages one diode drop below ground or one diode drop greater than the V_{CC} supply. Be careful, during testing at low V_{CC} levels (4.5V), as high level analog inputs (5V) can cause this input diode to conduct—especially at elevated temperatures, and cause errors for analog inputs near full-scale. The spec allows 50 mV forward bias of either diode. This means that as long as the analog V_{IN} does not exceed the supply voltage by more than 50 mV, the output code will be correct. To achieve an absolute 0 V_{DC} to 5 V_{DC} input voltage range will therefore require a minimum supply voltage of 4.950 V_{DC} over temperature variations, initial tolerance and loading.

Note 5: Accuracy is guaranteed at f_{CLK} = 640 kHz. At higher clock frequencies accuracy can degrade. For lower clock frequencies, the duty cycle limits can be extended so long as the minimum clock high time interval or minimum clock low time interval is no less than 275 ns.

Note 6: With an asynchronous start pulse, up to 8 clock periods may be required before the internal clock phases are proper to start the conversion process. The start request is internally latched, see *Figure 2* and section 2.0.

Note 7: The $\overline{CS}$ input is assumed to bracket the $\overline{WR}$ strobe input and therefore timing is dependent on the $\overline{WR}$ pulse width. An arbitrarily wide pulse width will hold the converter in a reset mode and the start of conversion is initiated by the low to high transition of the $\overline{WR}$ pulse (see timing diagrams).

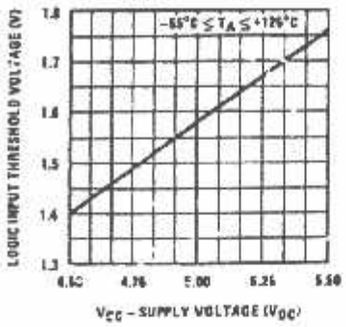
Note 8: None of these A/Ds requires a zero adjust (see section 2.5.1). To obtain zero code at other analog input voltages see section 2.5 and *Figure 5*.

Note 9: The $V_{REF}/2$ pin is the center point of a two-resistor divider connected from V_{CC} to ground. In all versions of the ADC0801, ADC0802, ADC0803, and ADC0805, and in the ADC0804LCJ, each resistor is typically 16 kΩ. In all versions of the ADC0804 except the ADC0804LCJ, each resistor is typically 2.2 kΩ.

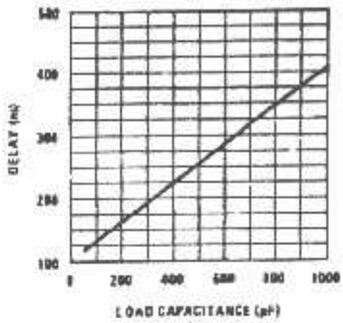
Note 10: Human body model, 100 pF discharged through a 1.5 kΩ resistor.

Typical Performance Characteristics

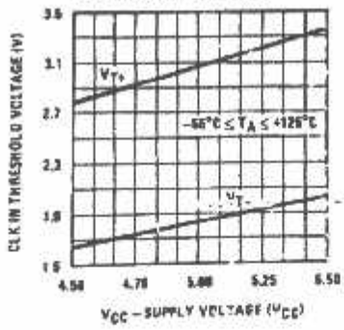
Logic Input Threshold Voltage vs. Supply Voltage



Delay From Falling Edge of $\overline{RD}$ to Output Data Valid vs. Load Capacitance

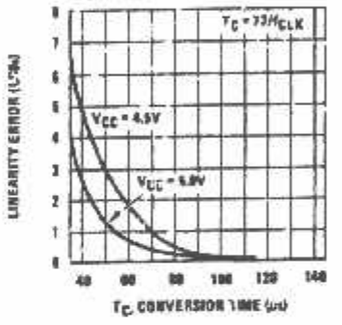


CLK IN Schmitt Trip Levels vs. Supply Voltage

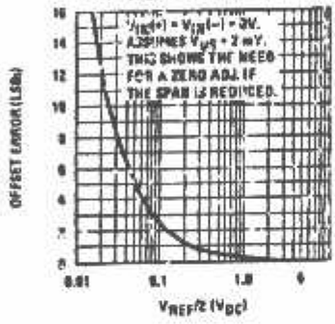


f_{CLK} vs. Clock Capacitor

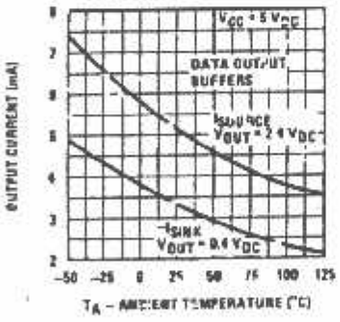
Full-Scale Error vs Conversion Time



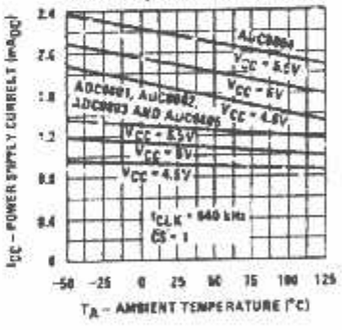
Effect of Unadjusted Offset Error vs. $V_{REF}/2$ Voltage



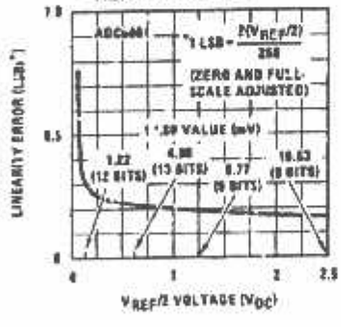
Output Current vs Temperature



Power Supply Current vs Temperature (Note 9)

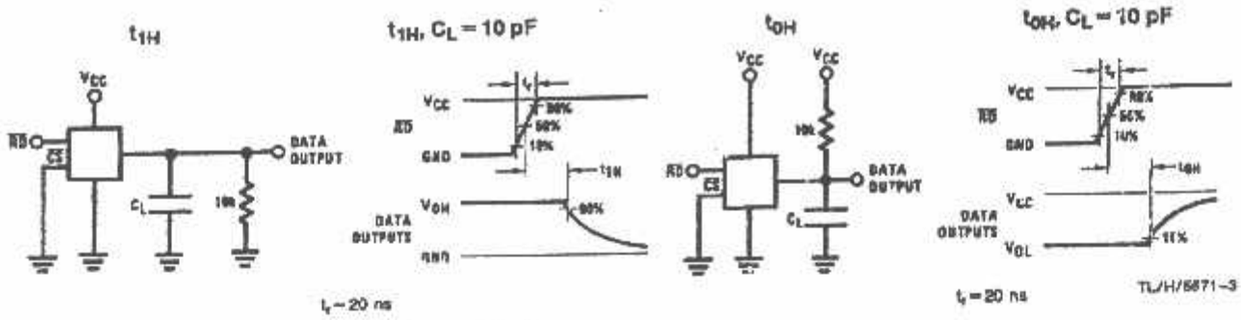


Linearity Error at Low $V_{REF}/2$ Voltages

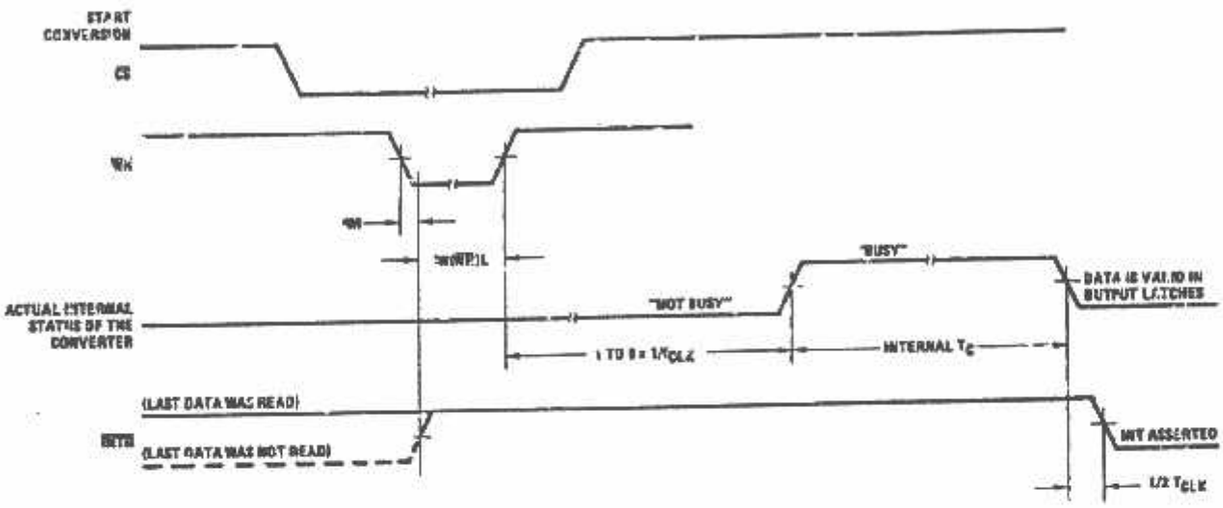


TL/H/5471–2

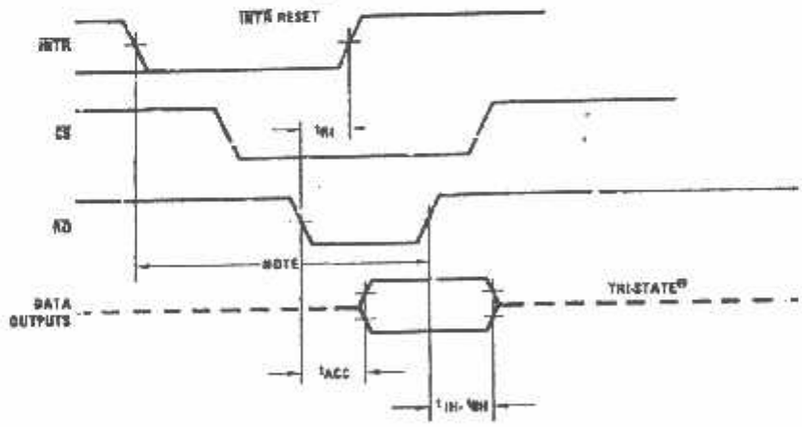
TRI-STATE Test Circuits and Waveforms



Timing Diagrams (All timing is measured from the 50% voltage points)



Output Enable and Reset $\overline{INTR}$

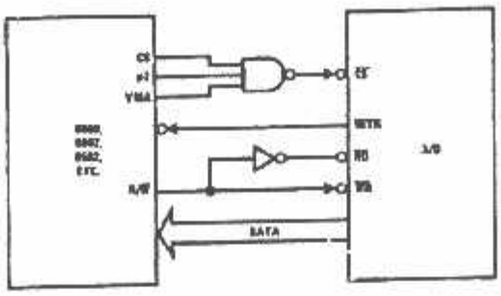


TL/H/5671–4

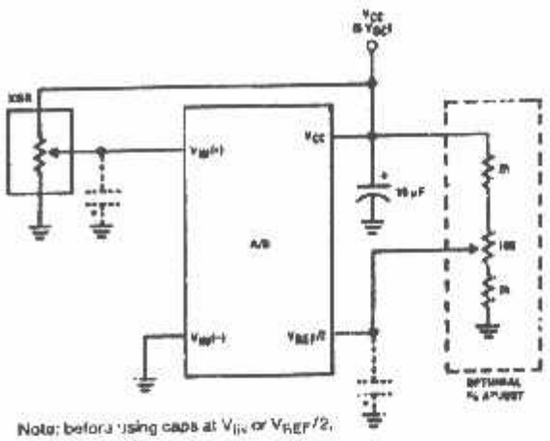
Note: Read strobe must occur 8 clock periods ($8/f_{CLK}$) after assertion of interrupt to guarantee reset of $\overline{INTR}$.

Typical Applications (Continued)

6800 Interface

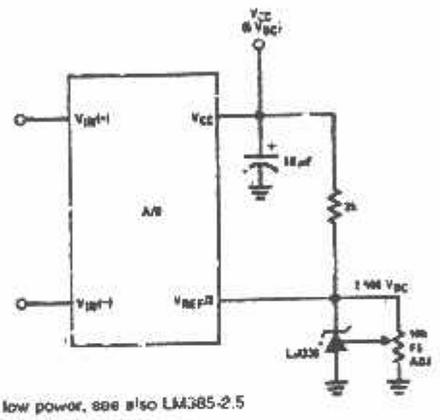


Ratiometric with Full-Scale Adjust



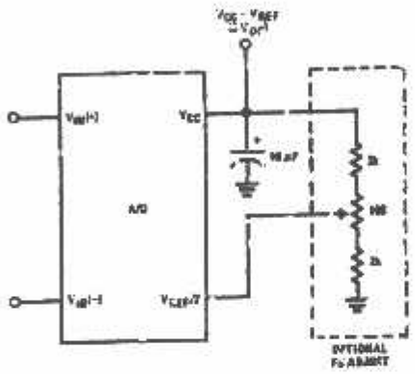
Note: before using caps at V_{IN} or $V_{REF}/2$, see section 2.3.2 Input Bypass Capacitors.

Absolute with a 2.500V Reference

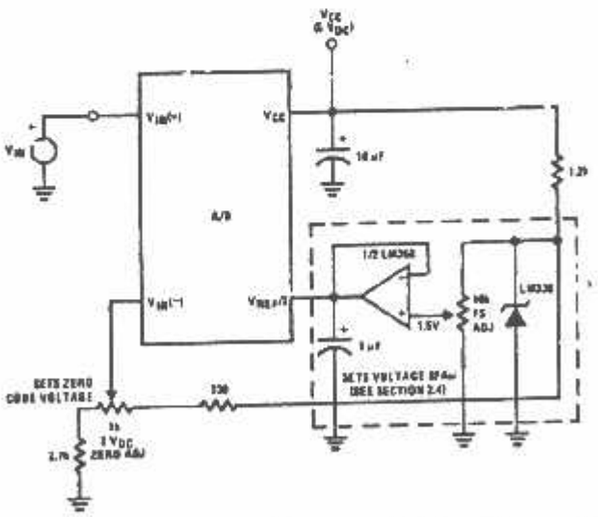


*For low power, see also LM385-2.5

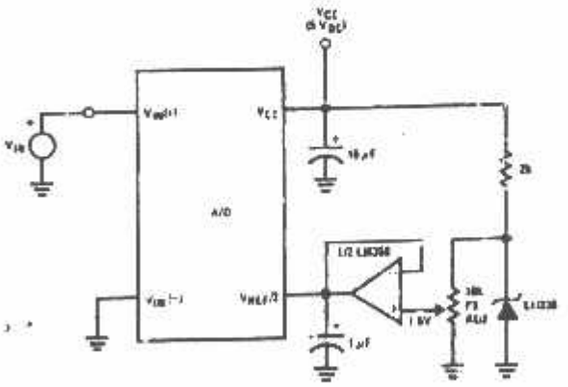
Absolute with a 5V Reference



Zero-Shift and Span Adjust: $2V \leq V_{IN} \leq 5V$



Span Adjust: $0V \leq V_{IN} \leq 3V$



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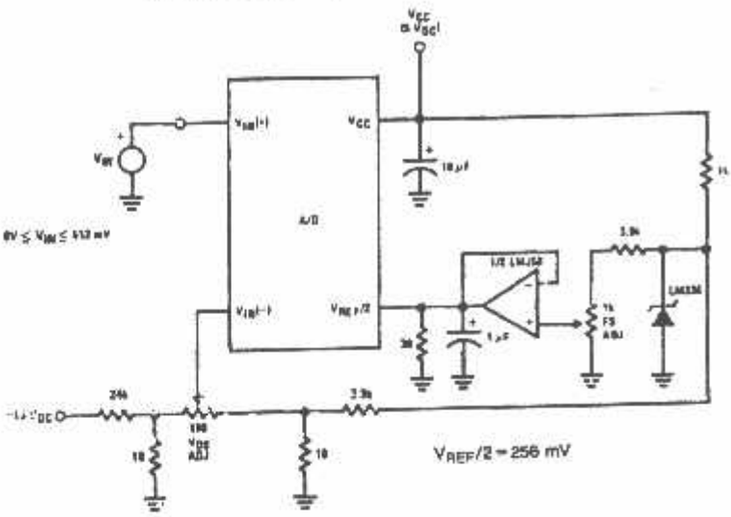
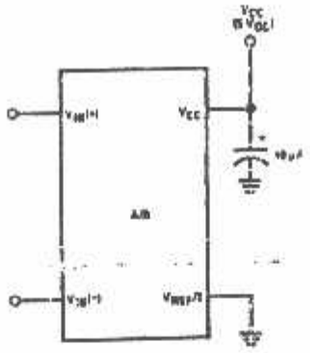
Typical Applications (Continued)

Directly Converting a Low-Level Signal



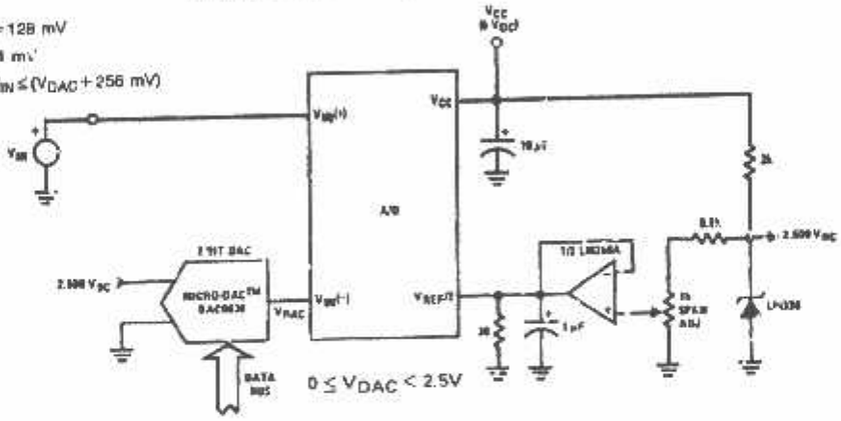
A µP Interfaced Comparator



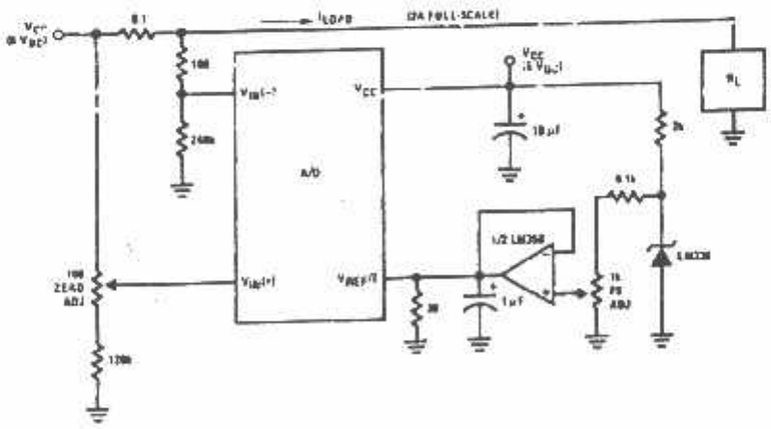
For: $V_{IN}(+) > V_{IN}(-)$
Output = FF_{HEX}
For: $V_{IN}(+) < V_{IN}(-)$
Output = 00_{HEX}

1 mV Resolution with µP Controlled Range

$V_{REF}/2 = 128$ mV
1 LSB = 1 mV
$V_{DAC} \leq V_{IN} \leq (V_{DAC} + 256$ mV)



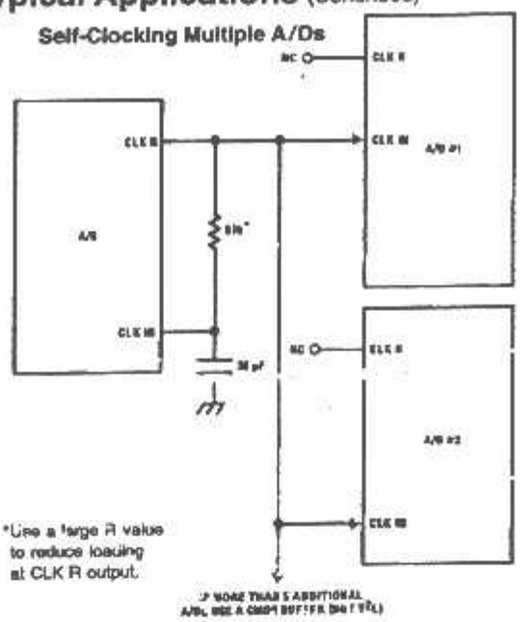
Digitizing a Current Flow



TL/H/5671–6

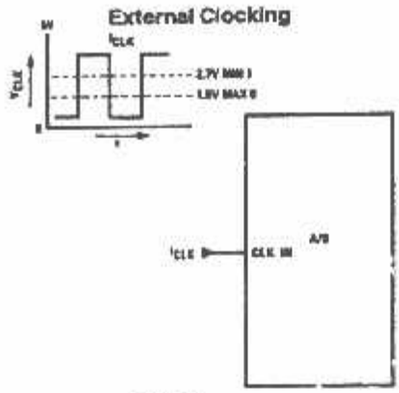
Typical Applications (Continued)

Self-Clocking Multiple A/Ds



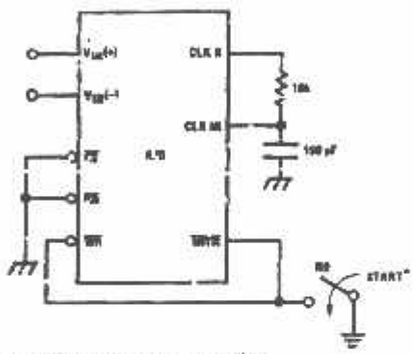
*Use a large R value to reduce loading at CLK R output.

External Clocking



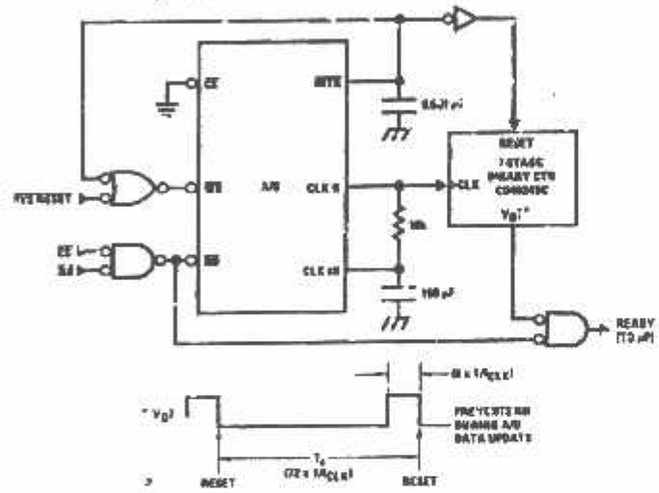
100 kHz ≤ f_{CLK} ≤ 1460 kHz

Self-Clocking in Free-Running Mode

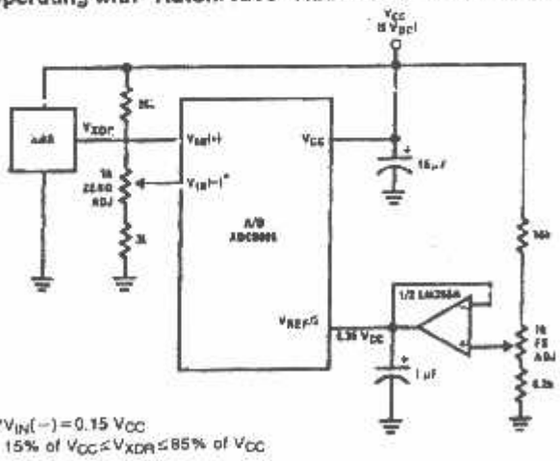


*After power-up, a momentary grounding of the $\overline{WR}$ input is needed to guarantee operation.

µP Interface for Free-Running A/D

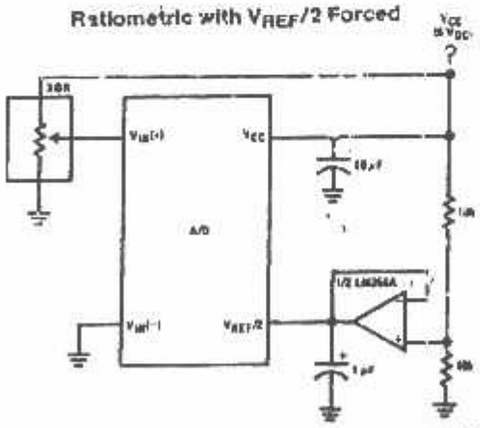


Operating with "Automotive" Ratiometric Transducers



*$V_{IN}(-) = 0.15\ V_{CC}$
15% of $V_{CC} \leq V_{XDR} \leq 85\%$ of V_{CC}

Ratiometric with $V_{REF}/2$ Forced



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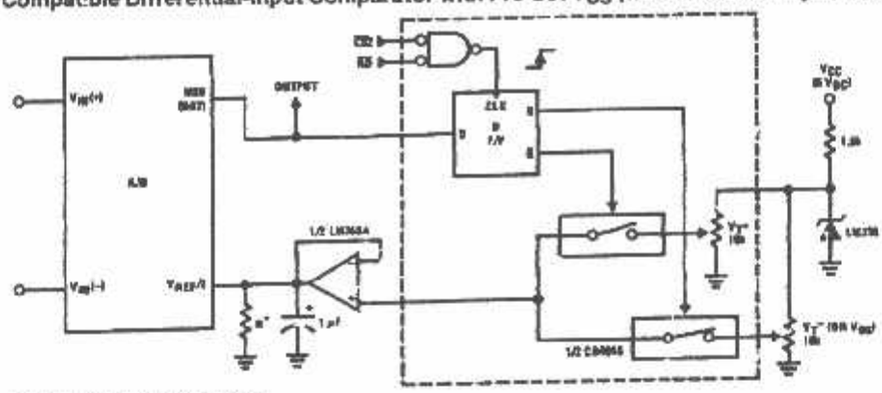
Typical Applications (Continued)

µP Compatible Differential-Input Comparator with Pre-Set V_{OS} (with or without Hysteresis)

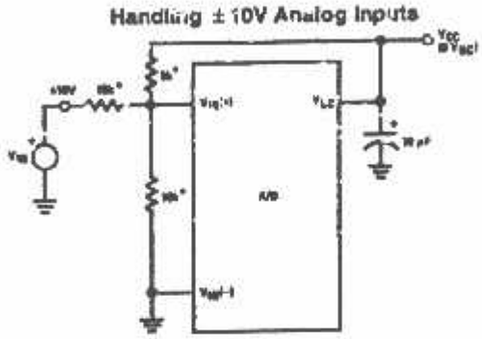


*See *Figure 5* to select R value

DB7 = "1" for $V_{IN}(+) > V_{IN}(-) + (V_{REF}/2)$

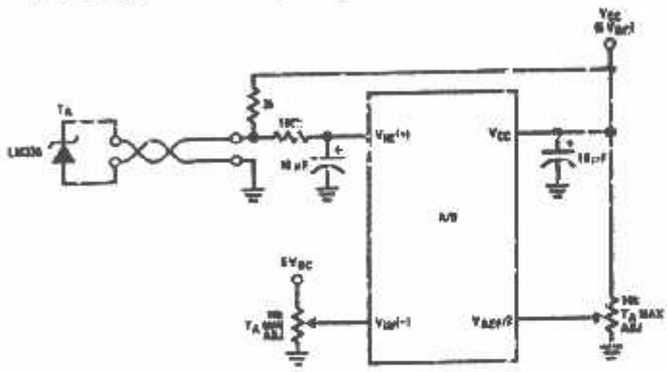
Omit circuitry within the dotted area if hysteresis is not needed

Handling ±10V Analog Inputs

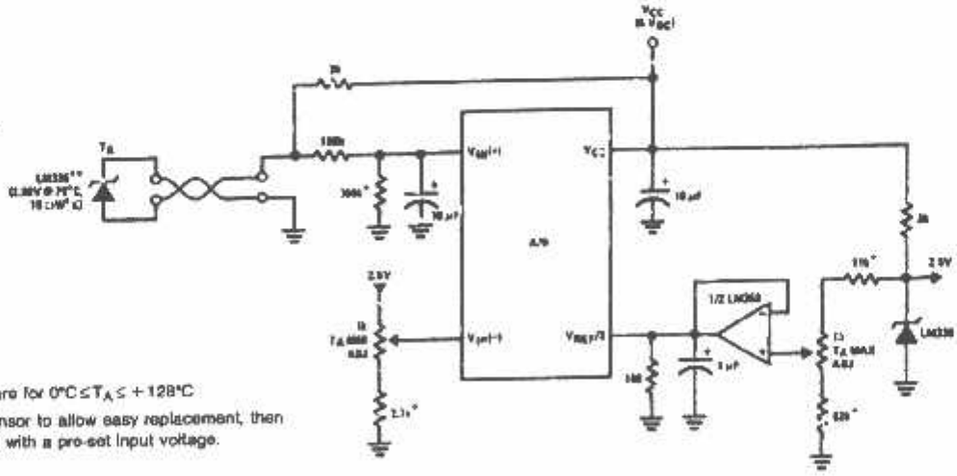


*Beckman Instruments #694-3-R10K resistor array

Low-Cost, µP Interfaced, Temperature-to-Digital Converter



µP Interfaced Temperature-to-Digital Converter



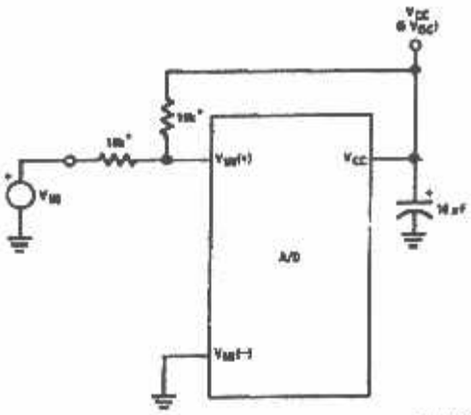
*Circuit values shown are for $0°C \leq T_A \leq +128°C$

**Can calibrate each sensor to allow easy replacement, then A/D can be calibrated with a pre-set input voltage.

TL/H/5671–8

Typical Applications (Continued)

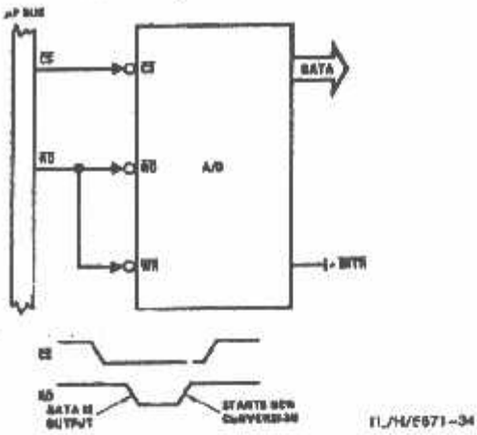
Handling ±5V Analog Inputs



TL/H/5671–33

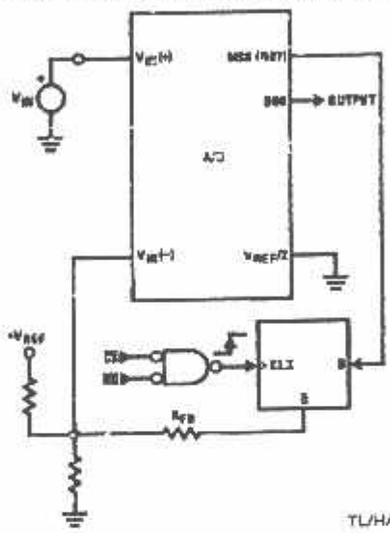
*Beckman Instruments #694-3-R10K resistor array

Read-Only Interface



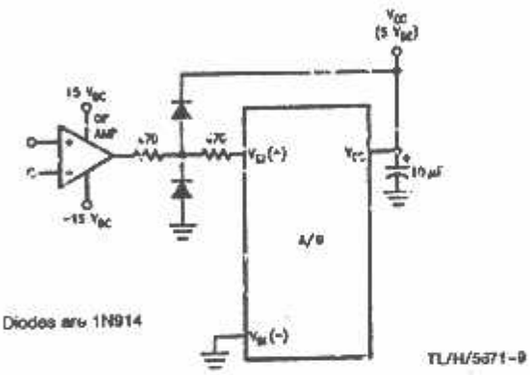
TL/H/5671–34

µP Interfaced Comparator with Hysteresis



TL/H/5671–35

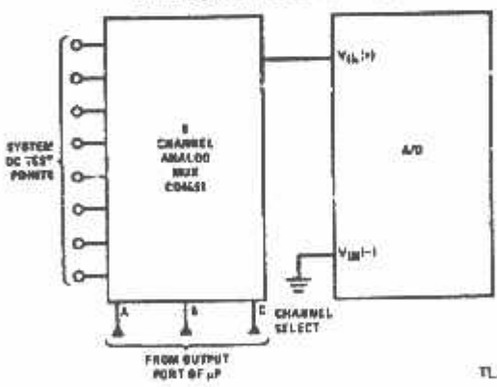
Protecting the Input



Diodes are 1N914

TL/H/5671–9

Analog Self-Test for a System



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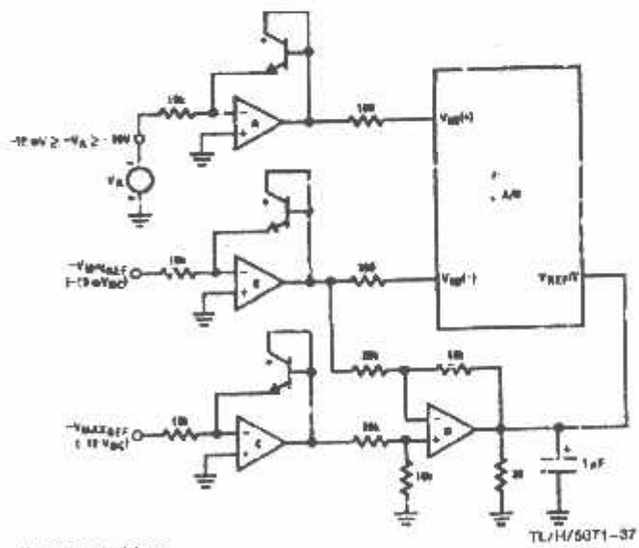
A Low-Cost, 3-Decade Logarithmic Converter



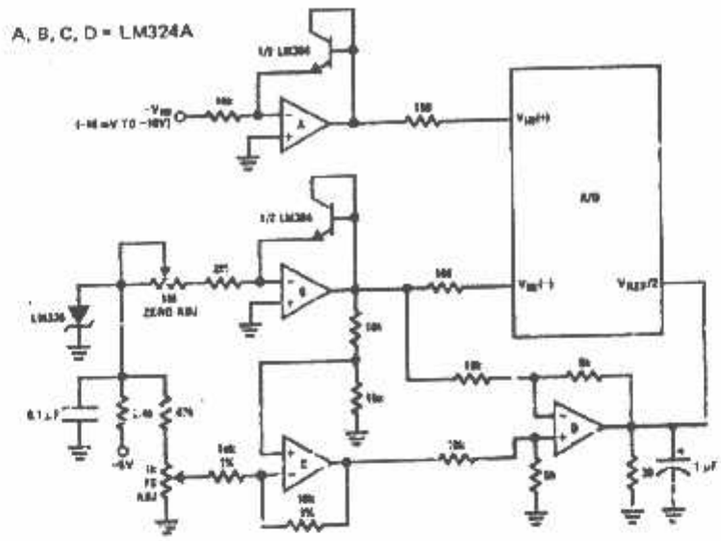
TL/H/5671–37

*LM389 transistors

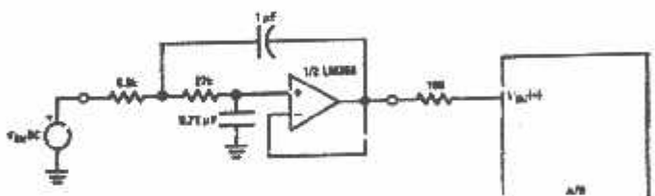
A, B, C, D = LM324A quad op amp

Typical Applications (Continued)

3-Decade Logarithmic A/D Converter



Noise Filtering the Analog Input

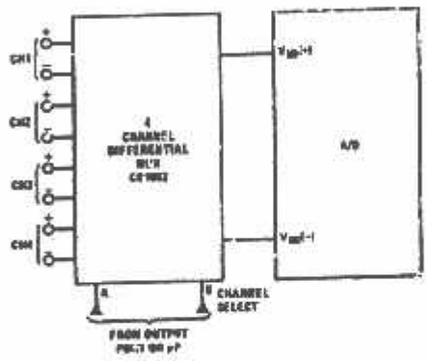


$f_C = 20$ Hz

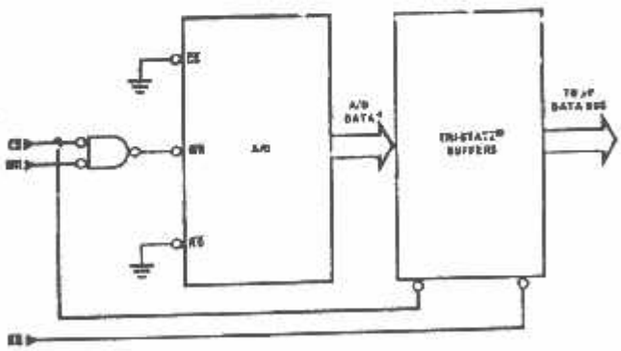
Uses Chebyshev implementation for steeper roll-off unity-gain, 2nd order, low-pass filter

Adding a separate filter for each channel increases system response time if an analog multiplexer is used

Multiplexing Differential Inputs

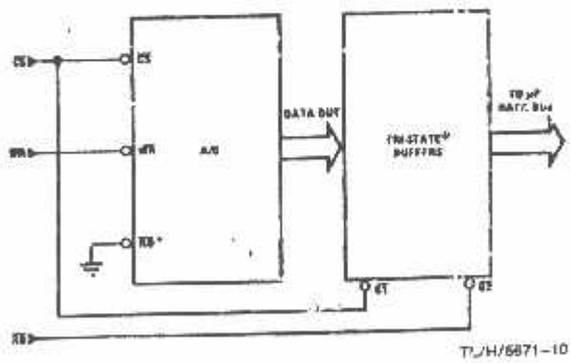


Output Buffers with A/D Data Enabled



*A/D output data is updated 1 CLK period prior to assertion of $\overline{INTR}$

Increasing Bus Drive and/or Reducing Time on Bus

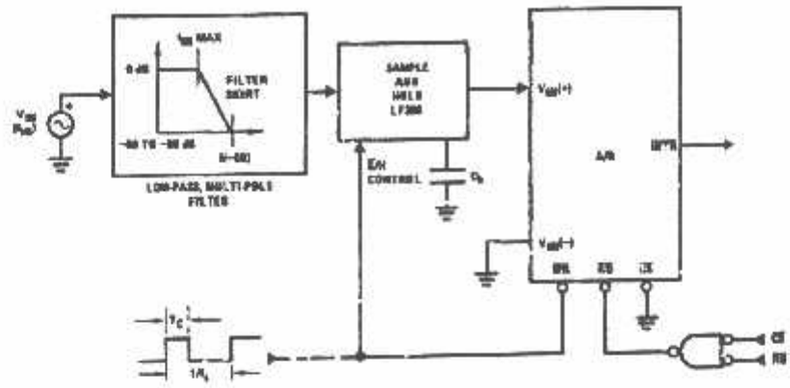


TL/H/5671–10

*Allows output data to set-up at falling edge of $\overline{CS}$

Typical Applications (Continued)

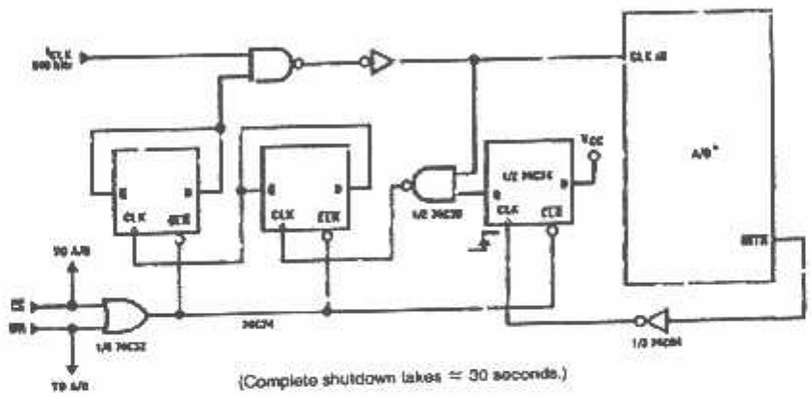
Sampling an AC Input Signal



Note 1: Oversample whenever possible (keep $f_S > 2(f - 50)$) to eliminate input frequency folding (aliasing) and to allow for the skirt response of the filter.

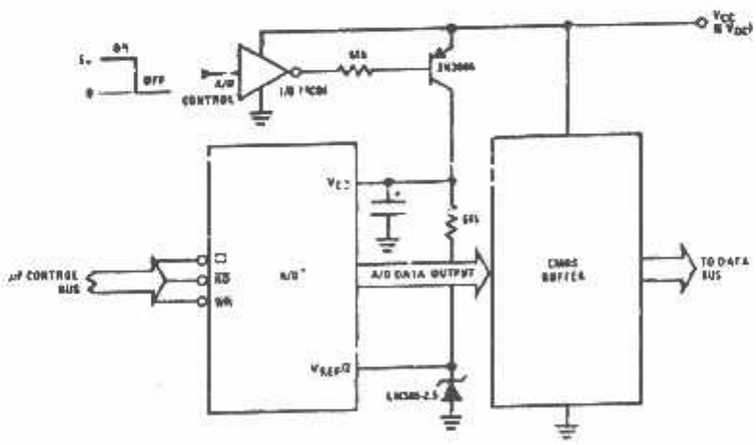
Note 2: Consider the amplitude errors which are introduced within the passband of the filter.

70% Power Savings by Clock Gating



(Complete shutdown takes ≈ 30 seconds.)

Power Savings by A/D and V_{REF} Shutdown



TL/H/5671-11

*Use ADC0801, 02, 03 or 05 for lowest power consumption.

Note: Logic inputs can be driven to V_{CC} with A/D supply at zero volts.

Buffer prevents data bus from overdriving output of A/D when in shutdown mode.

Functional Description

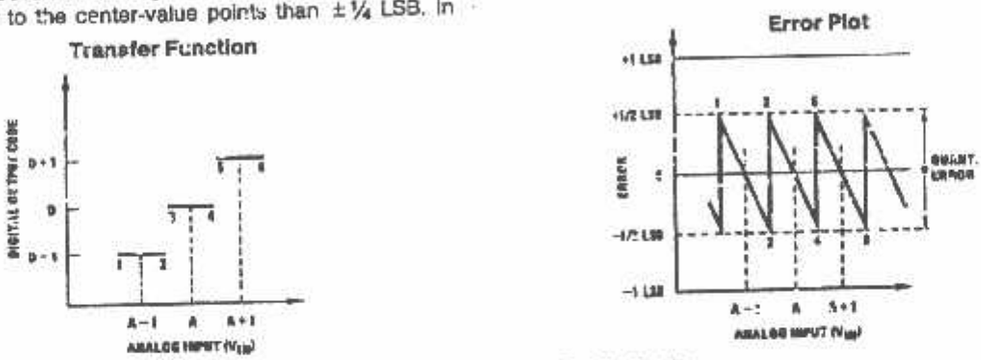
1.0 UNDERSTANDING A/D ERROR SPECS

A perfect A/D transfer characteristic (staircase waveform) is shown in *Figure 1a*. The horizontal scale is analog input voltage and the particular points labeled are in steps of 1 LSB (19.53 mV with 2.5V tied to the $V_{REF}/2$ pin). The digital output codes that correspond to these inputs are shown as D−1, D, and D+1. For the perfect A/D, not only will center-value (A−1, A, A+1, ...) analog inputs produce the correct output ditigal codes, but also each riser (the transitions between adjacent output codes) will be located ±½ LSB away from each center-value. As shown, the risers are ideal and have no width. Correct digital output codes will be provided for a range of analog input voltages that extend ±½ LSB from the ideal center-values. Each tread (the range of analog input voltage that provides the same digital output code) is therefore 1 LSB wide.

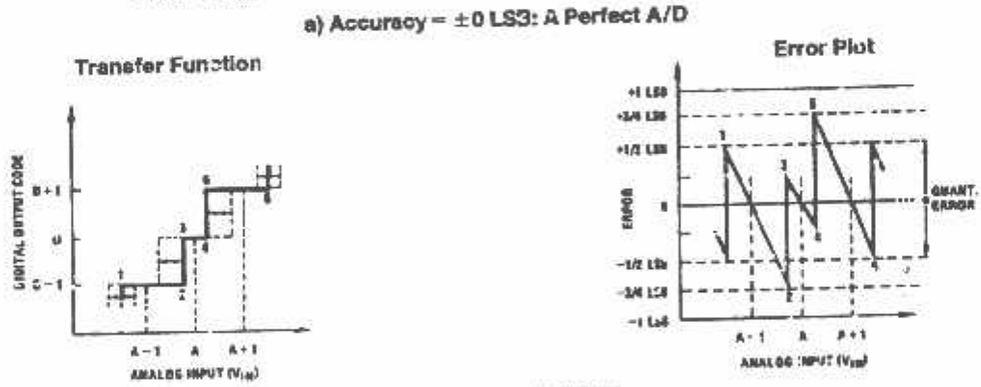
Figure 1b shows a worst case error plot for the ADC0801. All center-valued inputs are guaranteed to produce the correct output codes and the adjacent risers are guaranteed to be no closer to the center-value points than ±¼ LSB. In other words, if we apply an analog input equal to the center-value ±¼ LSB, *we guarantee* that the A/D will produce the correct digital code. The maximum range of the position of the code transition is indicated by the horizontal arrow and it is guaranteed to be no more than ½ LSB.

The error curve of *Figure 1c* shows a worst case error plot for the ADC0802. Here we guarantee that if we apply an analog input equal to the LSB analog voltage center-value the A/D will produce the correct digital code.

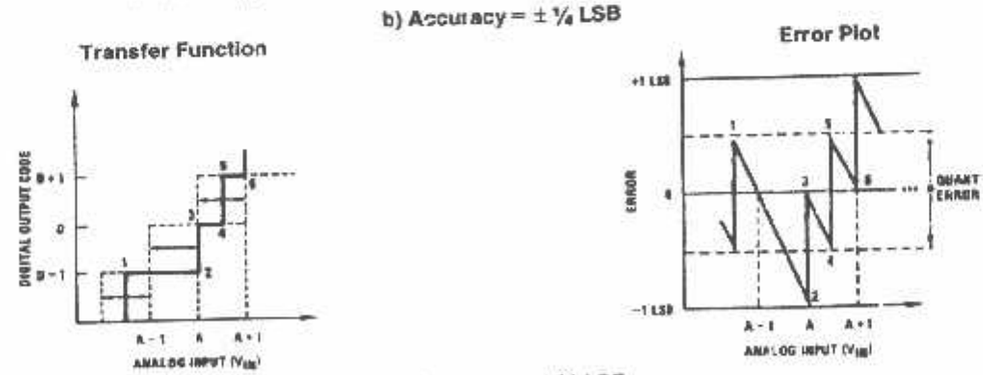
Next to each transfer function is shown the corresponding error plot. Many people may be more familiar with error plots than transfer functions. The analog input voltage to the A/D is provided by either a linear ramp or by the discrete output steps of a high resolution DAC. Notice that the error is continuously displayed and includes the quantization uncertainty of the A/D. For example the error at point 1 of *Figure 1a* is +½ LSB because the digital code appeared ½ LSB in advance of the center-value of the tread. The error plots always have a constant negative slope and the abrupt upside steps are always 1 LSB in magnitude.



a) Accuracy = ±0 LSB: A Perfect A/D



b) Accuracy = ±¼ LSB



c) Accuracy = ±½ LSB

TL/H/5871–12

FIGURE 1. Clarifying the Error Specs of an A/D Converter

Functional Description (Continued)

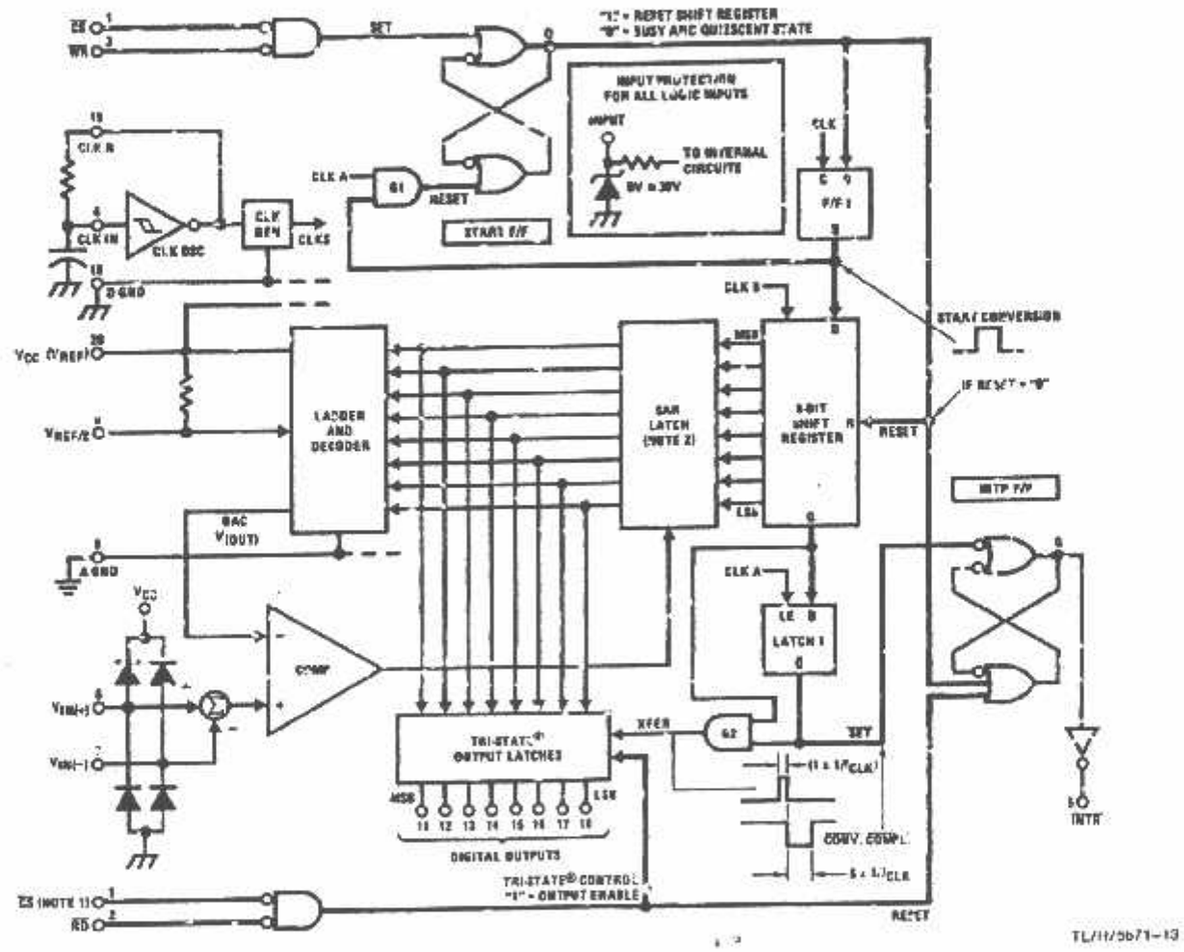
2.0 FUNCTIONAL DESCRIPTION

The ADC0801 series contains a circuit equivalent of the 256R network. Analog switches are sequenced by successive approximation logic to match the analog difference input voltage $[V_{IN}(+) - V_{IN}(-)]$ to a corresponding tap on the R network. The most significant bit is tested first and after 8 comparisons (64 clock cycles) a digital 8-bit binary code (1111 1111 = full-scale) is transferred to an output latch and then an interrupt is asserted ($\overline{INTR}$ makes a high-to-low transition). A conversion in process can be interrupted by issuing a second start command. The device may be operated in the free-running mode by connecting $\overline{INTR}$ to the $\overline{WR}$ input with $\overline{CS} = 0$. To ensure start-up under all possible conditions, an external $\overline{WR}$ pulse is required during the first power-up cycle.

On the high-to-low transition of the $\overline{WR}$ input the internal SAR latches and the shift register stages are reset. As long as the $\overline{CS}$ input and $\overline{WR}$ input remain low, the A/D will remain in a reset state. *Conversion will start from 1 to 9 clock periods after at least one of these inputs makes a low-to-high transition.*

A functional diagram of the A/D converter is shown in *Figure 2*. All of the package pinouts are shown and the major logic control paths are drawn in heavier weight lines.

The converter is started by having $\overline{CS}$ and $\overline{WR}$ simultaneously low. This sets the start flip-flop (F/F) and the resulting "1" level resets the 8-bit shift register, resets the Interrupt ($\overline{INTR}$) F/F and inputs a "1" to the D flop, F/F1, which is at the input end of the 8-bit shift register. Internal clock signals then transfer this "1" to the Q output of F/F1. The AND gate, G1, combines this "1" output with a clock signal to provide a reset signal to the start F/F. If the set signal is no longer present (either $\overline{WR}$ or $\overline{CS}$ is a "1") the start F/F is reset and the 8-bit shift register then can have the "1" clocked in, which starts the conversion process. If the set signal were to still be present, this reset pulse would have no effect (both outputs of the start F/F would momentarily be at a "1" level) and the 8-bit shift register would continue to be held in the reset mode. This logic therefore allows for wide $\overline{CS}$ and $\overline{WR}$ signals and the converter will start after at least one of those signals returns high and the internal clocks again provide a reset signal for the start F/F.



Note 1: $\overline{CS}$ shown twice for clarity.

Note 2: SAR = Successive Approximation Register.

FIGURE 2. Block Diagram

Functional Description (Continued)

After the "1" is clocked through the 8-bit shift register (which completes the SAR search) it appears as the input to the D-type latch, LATCH 1. As soon as this "1" is output from the shift register, the AND gate, G2, causes the new digital word to transfer to the TRI-STATE output latches. When LATCH 1 is subsequently enabled, the Q output makes a high-to-low transition which causes the INTR F/F to set. An inverting buffer then supplies the $\overline{INTR}$ input signal.

Note that this $\overline{SET}$ control of the INTR F/F remains low for 8 of the external clock periods (as the internal clocks run at 1/8 of the frequency of the external clock). If the data output is continuously enabled ($\overline{CS}$ and $\overline{RD}$ both held low), the $\overline{INTR}$ output will still signal the end of conversion (by a high-to-low transition), because the $\overline{SET}$ input can control the Q output of the INTR F/F even though the RESET input is constantly at a "1" level in this operating mode. This $\overline{INTR}$ output will therefore stay low for the duration of the $\overline{SET}$ signal, which is 8 periods of the external clock frequency (assuming the A/D is not started during this interval).

When operating in the free-running or continuous conversion mode ($\overline{INTR}$ pin tied to $\overline{WR}$ and $\overline{CS}$ wired low—see also section 2.8), the START F/F is SET by the high-to-low transition of the $\overline{INTR}$ signal. This resets the SHIFT REGISTER which causes the input to the D-type latch, LATCH 1, to go low. As the latch enable input is still present, the $\overline{Q}$ output will go high, which then allows the INTR F/F to be RESET. This reduces the width of the resulting $\overline{INTR}$ output pulse to only a few propagation delays (approximately 300 ns).

When data is to be read, the combination of both $\overline{CS}$ and $\overline{RD}$ being low will cause the INTR F/F to be reset and the TRI-STATE output latches will be enabled to provide the 8-bit digital outputs.

2.1 Digital Control Inputs

The digital control inputs ($\overline{CS}$, $\overline{RD}$, and $\overline{WR}$) meet standard T²L logic voltage levels. These signals have been renamed when compared to the standard A/D Start and Output Enable labels. In addition, these inputs are active low to allow an easy interface to microprocessor control busses. For non-microprocessor based applications, the $\overline{CS}$ input (pin 1) can be grounded and the standard A/D Start function is obtained by an active low pulse applied at the $\overline{WR}$ input (pin 3) and the Output Enable function is caused by an active low pulse at the $\overline{RD}$ input (pin 2).

2.2 Analog Differential Voltage Inputs and Common-Mode Rejection

This A/D has additional applications flexibility due to the analog differential voltage input. The $V_{IN}(-)$ input (pin 7) can be used to automatically subtract a fixed voltage value from the input reading (tare correction). This is also useful in 4 mA–20 mA current loop conversion. In addition, common-mode noise can be reduced by use of the differential input.

The time interval between sampling $V_{IN}(+)$ and $V_{IN}(-)$ is 4-½ clock periods. The maximum error voltage due to this slight time difference between the input voltage samples is given by:

$$\Delta V_e(MAX) = (V_P)(2\pi f_{cm})\left(\frac{4.5}{f_{CLK}}\right),$$

where:

ΔV_e is the error voltage due to sampling delay

V_P is the peak value of the common-mode voltage

f_{cm} is the common-mode frequency

As an example, to keep this error to ¼ LSB (~5 mV) when operating with a 60 Hz common-mode frequency, f_{cm}, and using a 640 kHz A/D clock, f_{CLK}, would allow a peak value of the common-mode voltage, V_P, which is given by:

$$V_P = \frac{[\Delta V_{e(MAX)}(f_{CLK})]}{(2\pi f_{cm})(4.5)}$$

or

$$V_P = \frac{(5 \times 10^{-3})(640 \times 10^3)}{(6.28)(60)(4.5)}$$

which gives

$V_P \simeq 1.9V$.

The allowed range of analog input voltages usually places more severe restrictions on input common-mode noise levels.

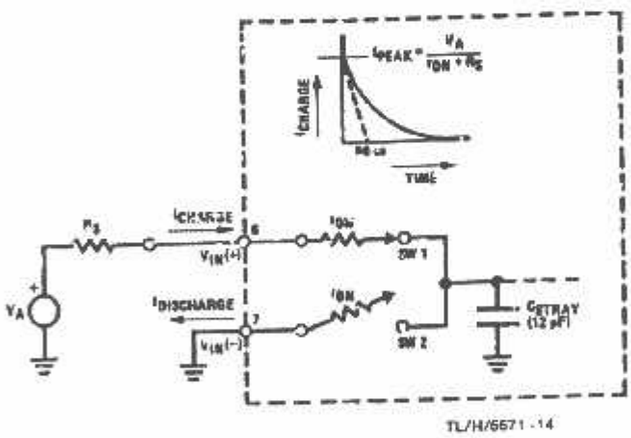
An analog input voltage with a reduced span and a relatively large zero offset can be handled easily by making use of the differential input (see section 2.4 Reference Voltage).

2.3 Analog Inputs

2.3.1 Input Current

Normal Mode

Due to the internal switching action, displacement currents will flow at the analog inputs. This is due to on-chip stray capacitance to ground as shown in *Figure 3*.



r_{ON} of SW 1 and SW 2 ≈ 5 kΩ

$\tau = r_{ON} C_{STRAY} \approx 5\ k\Omega \times 12\ pF = 60\ ns$

FIGURE 3. Analog Input Impedance

Functional Description (Continued)

The voltage on this capacitance is switched and will result in currents entering the $V_{IN}(+)$ input pin and leaving the $V_{IN}(-)$ input which will depend on the analog differential input voltage levels. These current transients occur at the leading edge of the internal clocks. They rapidly decay and *do not cause errors* as the on-chip comparator is strobed at the end of the clock period.

Fault Mode

If the voltage source applied to the $V_{IN}(+)$ or $V_{IN}(-)$ pin exceeds the allowed operating range of V_{CC} + 50 mV, large input currents can flow through a parasitic diode to the V_{CC} pin. If these currents can exceed the 1 mA max allowed spec, an external diode (1N914) should be added to bypass this current to the V_{CC} pin (with the current bypassed with this diode, the voltage at the $V_{IN}(+)$ pin can exceed the V_{CC} voltage by the forward voltage of this diode).

2.3.2 Input Bypass Capacitors

Bypass capacitors at the inputs will average these charges and cause a DC current to flow through the output resistances of the analog signal sources. This charge pumping action is worse for continuous conversions with the $V_{IN}(+)$ input voltage at full-scale. For continuous conversions with a 640 kHz clock frequency with the $V_{IN}(+)$ input at 5V, this DC current is at a maximum of approximately 5 μA. Therefore, *bypass capacitors should not be used at the analog inputs or the $V_{REF}/2$ pin* for high resistance sources (> 1 kΩ). If input bypass capacitors are necessary for noise filtering and high source resistance is desirable to minimize capacitor size, the detrimental effects of the voltage drop across this input resistance, which is due to the average value of the input current, can be eliminated with a full-scale adjustment while the given source resistor and input bypass capacitor are both in place. This is possible because the average value of the input current is a precise linear function of the differential input voltage.

2.3.3 Input Source Resistance

Large values of source resistance where an input bypass capacitor is not used, *will not cause errors* as the input currents settle out prior to the comparison time. If a low pass filter is required in the system, use a low valued series resistor (≤ 1 kΩ) for a passive RC section or add an op amp RC active low pass filter. For low source resistance applications, (≤ 1 kΩ), a 0.1 μF bypass capacitor at the inputs will prevent noise pickup due to series lead inductance of a long wire. A 100Ω series resistor can be used to isolate this capacitor—both the R and C are placed outside the feedback loop—from the output of an op amp, if used.

2.3.4 Noise

The leads to the analog inputs (pin 6 and 7) should be kept as short as possible to minimize input noise coupling. Both noise and undesired digital clock coupling to these inputs can cause system errors. The source resistance for these inputs should, in general, be kept below 5 kΩ. Larger values of source resistance can cause undesired system noise pickup. Input bypass capacitors, placed from the analog inputs to ground, will eliminate system noise pickup but can create analog scale errors as these capacitors will average the transient input switching currents of the A/D (see section 2.3.1.). This scale error depends on both a large source resistance and the use of an input bypass capacitor. This error can be eliminated by doing a full-scale adjustment of the A/D (adjust $V_{REF}/2$ for a proper full-scale reading—see section 2.5.2 on Full-Scale Adjustment) with the source resistance and input bypass capacitor in place.

2.4 Reference Voltage

2.4.1 Span Adjust

For maximum applications flexibility, these A/Ds have been designed to accommodate a 5 V_{DC}, 2.5 V_{DC} or an adjusted voltage reference. This has been achieved in the design of the IC as shown in *Figure 4*.

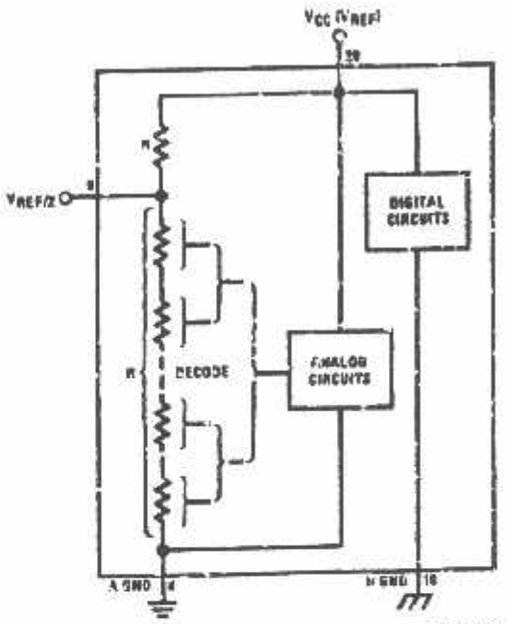


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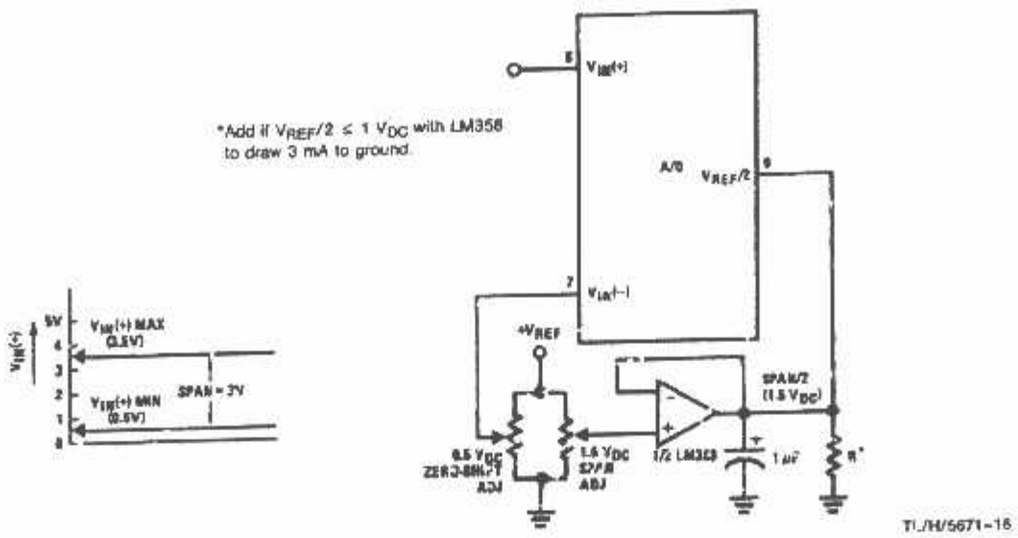
FIGURE 4. The $V_{REFERENCE}$ Design on the IC

Notice that the reference voltage for the IC is either ½ of the voltage applied to the V_{CC} supply pin, or is equal to the voltage that is externally forced at the $V_{REF}/2$ pin. This allows for a ratiometric voltage reference using the V_{CC} supply, a 5 V_{DC} reference voltage can be used for the V_{CC} supply or a voltage less than 2.5 V_{DC} can be applied to the $V_{REF}/2$ input for increased application flexibility. The internal gain to the $V_{REF}/2$ input is 2, making the full-scale differential input voltage twice the voltage at pin 9.

An example of the use of an adjusted reference voltage is to accommodate a reduced span—or dynamic voltage range of the analog input voltage. If the analog input voltage were to range from 0.5 V_{DC} to 3.5 V_{DC}, instead of 0V to 5 V_{DC}, the span would be 3V as shown in *Figure 5*. With 0.5 V_{DC} applied to the $V_{IN}(-)$ pin to absorb the offset, the reference voltage can be made equal to ½ of the 3V span or 1.5 V_{DC}. The A/D now will encode the $V_{IN}(+)$ signal from 0.5V to 3.5 V with the 0.5V input corresponding to zero and the 3.5 V_{DC} input corresponding to full-scale. The full 8 bits of resolution are therefore applied over this reduced analog input voltage range.

Functional Description (Continued)



a) Analog Input Signal Example

b) Accommodating an Analog Input from 0.5V (Digital Out = 00_{HEX}) to 5.5V (Digital Out = FF_{HEX})

FIGURE 5. Adapting the A/D Analog Input Voltages to Match an Arbitrary Input Signal Range

2.4.2 Reference Accuracy Requirements

The converter can be operated in a ratiometric mode or an absolute mode. In ratiometric converter applications, the magnitude of the reference voltage is a factor in both the output of the source transducer and the output of the A/D converter and therefore cancels out in the final digital output code. The ADC0805 is specified particularly for use in ratiometric applications with no adjustments required. In absolute conversion applications, both the initial value and the temperature stability of the reference voltage are important factors in the accuracy of the A/D converter. For $V_{REF}/2$ voltages of 2.4 V_{DC} nominal value, initial errors of ±10 mV_{DC} will cause conversion errors of ±1 LSB due to the gain of 2 of the $V_{REF}/2$ input. In reduced span applications, the initial value and the stability of the $V_{REF}/2$ input voltage become even more important. For example, if the span is reduced to 2.5V, the analog input LSB voltage value is correspondingly reduced from 20 mV (5V span) to 10 mV and 1 LSB at the $V_{REF}/2$ input becomes 5 mV. As can be seen, this reduces the allowed initial tolerance of the reference voltage and requires correspondingly less absolute change with temperature variations. Note that spans smaller than 2.5V place even tighter requirements on the initial accuracy and stability of the reference source.

In general, the magnitude of the reference voltage will require an initial adjustment. Errors due to an improper value of reference voltage appear as full-scale errors in the A/D transfer function. IC voltage regulators may be used for references if the ambient temperature changes are not excessive. The LM336B 2.5V IC reference diode (from National Semiconductor) has a temperature stability of 1.8 mV typ (6 mV max) over $0°C \leq T_A \leq +70°C$. Other temperature range parts are also available.

2.5 Errors and Reference Voltage Adjustments

2.5.1 Zero Error

The zero of the A/D does not require adjustment. If the minimum analog input voltage value, $V_{IN(MIN)}$, is not ground, a zero offset can be done. The converter can be made to output 0000 0000 digital code for this minimum input voltage by biasing the A/D $V_{IN}(-)$ input at this $V_{IN(MIN)}$ value (see Applications section). This utilizes the differential mode operation of the A/D.

The zero error of the A/D converter relates to the location of the first riser of the transfer function and can be measured by grounding the $V_{IN}(-)$ input and applying a small magnitude positive voltage to the $V_{IN}(+)$ input. Zero error is the difference between the actual DC input voltage that is necessary to just cause an output digital code transition from 0000 0000 to 0000 0001 and the ideal ½ LSB value (½ LSB = 9.8 mV for $V_{REF}/2 = 2.500\ V_{DC}$).

2.5.2 Full-Scale

The full-scale adjustment can be made by applying a differential input voltage that is 1½ LSB less than the desired analog full-scale voltage range and then adjusting the magnitude of the $V_{REF}/2$ input (pin 9 or the V_{CC} supply if pin 9 is not used) for a digital output code that is just changing from 1111 1110 to 1111 1111.

Functional Description (Continued)

2.5.3 Adjusting for an Arbitrary Analog Input Voltage Range

If the analog zero voltage of the A/D is shifted away from ground (for example, to accommodate an analog input signal that does not go to ground) this new zero reference should be properly adjusted first. A $V_{IN}(+)$ voltage that equals this desired zero reference plus ½ LSB (where the LSB is calculated for the desired analog span, 1 LSB = analog span/256) is applied to pin 6 and the zero reference voltage at pin 7 should then be adjusted to just obtain the 00_{HEX} to 01_{HEX} code transition.

The full-scale adjustment should then be made (with the proper $V_{IN}(-)$ voltage applied) by forcing a voltage to the $V_{IN}(+)$ input which is given by:

$$V_{IN}(+) \text{ fs adj} = V_{MAX} - 1.5\left[\frac{(V_{MAX} - V_{MIN})}{256}\right],$$

where:

V_{MAX} = The high end of the analog input range

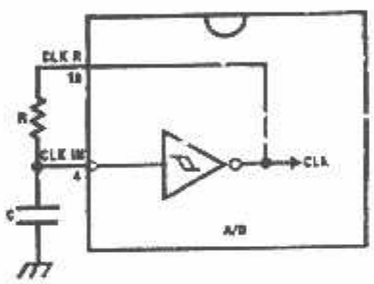
and

V_{MIN} = the low end (the offset zero) of the analog range. (Both are ground referenced.)

The $V_{REF}/2$ (or V_{CC}) voltage is then adjusted to provide a code change from FE_{HEX} to FF_{HEX}. This completes the adjustment procedure.

2.6 Clocking Option

The clock for the A/D can be derived from the CPU clock or an external RC can be added to provide self-clocking. The CLK IN (pin 4) makes use of a Schmitt trigger as shown in *Figure 6*.



$$f_{CLK} \cong \frac{1}{1.1\,RC}$$

$$R \cong 10\ k\Omega$$

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FIGURE 6. Self-Clocking the A/D

Heavy capacitive or DC loading of the clock R pin should be avoided as this will disturb normal converter operation. Loads less than 50 pF, such as driving up to 7 A/D converter clock inputs from a single clock R pin of 1 converter, are allowed. For larger clock line loading, a CMOS or low power TTL buffer or PNP input logic should be used to minimize the loading on the clock R pin (do not use a standard TTL buffer).

2.7 Restart During a Conversion

If the A/D is restarted ($\overline{CS}$ and $\overline{WR}$ go low and return high) during a conversion, the converter is reset and a new conversion is started. The output data latch is not updated if the conversion in process is not allowed to be completed, therefore the data of the previous conversion remains in this latch. The $\overline{INTR}$ output simply remains at the "1" level.

2.8 Continuous Conversions

For operation in the free-running mode an initializing pulse should be used, following power-up, to ensure circuit operation. In this application, the $\overline{CS}$ input is grounded and the $\overline{WR}$ input is tied to the $\overline{INTR}$ output. This $\overline{WR}$ and $\overline{INTR}$ node should be momentarily forced to logic low following a power-up cycle to guarantee operation.

2.9 Driving the Data Bus

This MOS A/D, like MOS microprocessors and memories, will require a bus driver when the total capacitance of the data bus gets large. Other circuitry, which is tied to the data bus, will add to the total capacitive loading, even in TRI-STATE (high impedance mode). Backplane bussing also greatly adds to the stray capacitance of the data bus.

There are some alternatives available to the designer to handle this problem. Basically, the capacitive loading of the data bus slows down the response time, even though DC specifications are still met. For systems operating with a relatively slow CPU clock frequency, more time is available in which to establish proper logic levels on the bus and therefore higher capacitive loads can be driven (see typical characteristics curves).

At higher CPU clock frequencies time can be extended for I/O reads (and/or writes) by inserting wait states (8080) or using clock extending circuits (6800).

Finally, if time is short and capacitive loading is high, external bus drivers must be used. These can be TRI-STATE buffers (low power Schottky such as the DM74LS240 series is recommended) or special higher drive current products which are designed as bus drivers. High current bipolar bus drivers with PNP inputs are recommended.

2.10 Power Supplies

Noise spikes on the V_{CC} supply line can cause conversion errors as the comparator will respond to this noise. A low inductance tantalum filter capacitor should be used close to the converter V_{CC} pin and values of 1 μF or greater are recommended. If an unregulated voltage is available in the system, a separate LM340LAZ-5.0, TO-92, 5V voltage regulator for the converter (and other analog circuitry) will greatly reduce digital noise on the V_{CC} supply.

2.11 Wiring and Hook-Up Precautions

Standard digital wire wrap sockets are not satisfactory for breadboarding this A/D converter. Sockets on PC boards can be used and all logic signal wires and leads should be grouped and kept as far away as possible from the analog signal leads. Exposed leads to the analog inputs can cause undesired digital noise and hum pickup, therefore shielded leads may be necessary in many applications.

Functional Description (Continued)

A single point analog ground that is separate from the logic ground points should be used. The power supply bypass capacitor and the self-clocking capacitor (if used) should both be returned to digital ground. Any $V_{REF}/2$ bypass capacitors, analog input filter capacitors, or input signal shielding should be returned to the analog ground point. A test for proper grounding is to measure the zero error of the A/D converter. Zero errors in excess of ¼ LSB can usually be traced to improper board layout and wiring (see section 2.5.1 for measuring the zero error).

3.0 TESTING THE A/D CONVERTER

There are many degrees of complexity associated with testing an A/D converter. One of the simplest tests is to apply a known analog input voltage to the converter and use LEDs to display the resulting digital output code as shown in *Figure 7*.

For ease of testing, the $V_{REF}/2$ (pin 9) should be supplied with 2.560 V_{DC} and a V_{CC} supply voltage of 5.12 V_{DC} should be used. This provides an LSB value of 20 mV.

If a full-scale adjustment is to be made, an analog input voltage of 5.090 V_{DC} (5.120−1½ LSB) should be applied to the $V_{IN}(+)$ pin with the $V_{IN}(-)$ pin grounded. The value of the $V_{REF}/2$ input voltage should then be adjusted until the digital output code is just changing from 1111 1110 to 1111 1111. This value of $V_{REF}/2$ should then be used for all the tests.

The digital output LED display can be decoded by dividing the 8 bits into 2 hex characters, the 4 most significant (MS) and the 4 least significant (LS). Table I shows the fractional binary equivalent of these two 4-bit groups. By adding the voltages obtained from the "VMS" and "VLS" columns in Table I, the nominal value of the digital display (when $V_{REF}/2$ = 2.560V) can be determined. For example, for an output LED display of 1011 0110 or B6 (in hex), the voltage values from the table are 3.520 + 0.120 or 3.640 V_{DC}. These voltage values represent the center-values of a perfect A/D converter. The effects of quantization error have to be accounted for in the interpretation of the test results.

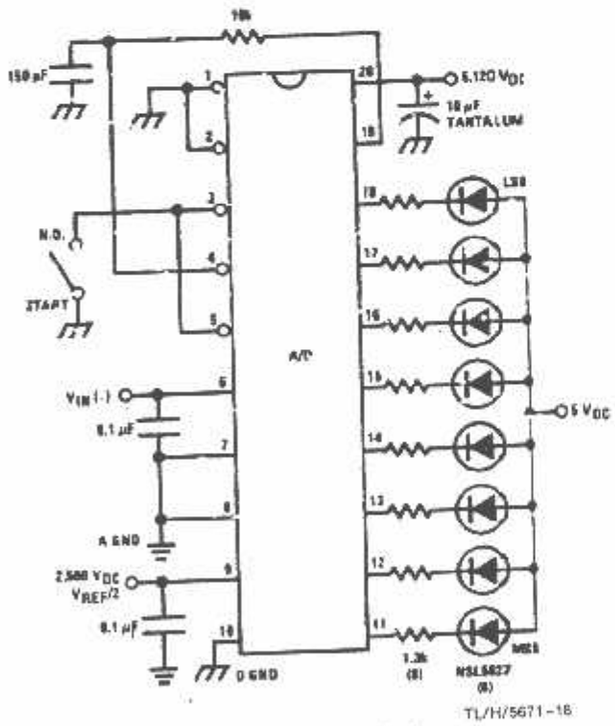

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FIGURE 7. Basic A/D Tester

For a higher speed test system, or to obtain plotted data, a digital-to-analog converter is needed for the test set-up. An accurate 10-bit DAC can serve as the precision voltage source for the A/D. Errors of the A/D under test can be expressed as either analog voltages or differences in 2 digital words.

A basic A/D tester that uses a DAC and provides the error as an analog output voltage is shown in *Figure 8*. The 2 op amps can be eliminated if a lab DVM with a numerical subtraction feature is available to read the difference voltage, "A−C", directly. The analog input voltage can be supplied by a low frequency ramp generator and an X-Y plotter can be used to provide analog error (Y axis) versus analog input (X axis).

For operation with a microprocessor or a computer-based test system, it is more convenient to present the errors digitally. This can be done with the circuit of *Figure 9*, where the output code transitions can be detected as the 10-bit DAC is incremented. This provides ¼ LSB steps for the 8-bit A/D under test. If the results of this test are automatically plotted with the analog input on the X axis and the error (in LSB's) as the Y axis, a useful transfer function of the A/D under test results. For acceptance testing, the plot is not necessary and the testing speed can be increased by establishing internal limits on the allowed error for each code.

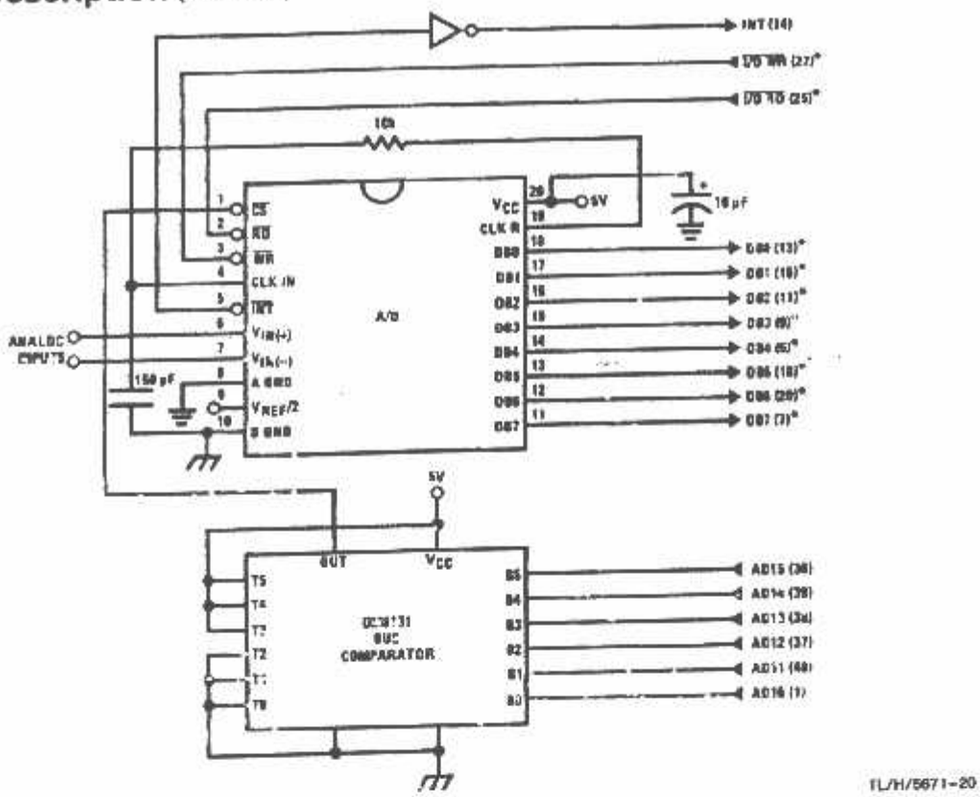
4.0 MICROPROCESSOR INTERFACING

To discuss the interface with 8080A and 6800 microprocessors, a common sample subroutine structure is used. The microprocessor starts the A/D, reads and stores the results of 16 successive conversions, then returns to the user's program. The 16 data bytes are stored in 16 successive memory locations. All Data and Addresses will be given in hexadecimal form. Software and hardware details are provided separately for each type of microprocessor.

4.1 Interfacing 8080 Microprocessor Derivatives (8048, 8085)

This converter has been designed to directly interface with derivatives of the 8080 microprocessor. The A/D can be mapped into memory space (using standard memory address decoding for $\overline{CS}$ and the $\overline{MEMR}$ and $\overline{MEMW}$ strobes) or it can be controlled as an I/O device by using the $\overline{I/O\ R}$ and $\overline{I/O\ W}$ strobes and decoding the address bits A0 → A7 (or address bits A8 → A15 as they will contain the same 8-bit address information) to obtain the $\overline{CS}$ input. Using the I/O space provides 256 additional addresses and may allow a simpler 8-bit address decoder but the data can only be input to the accumulator. To make use of the additional memory reference instructions, the A/D should be mapped into memory space. An example of an A/D in I/O space is shown in *Figure 10*.

Functional Description (Continued)



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Note 1: *Pin numbers for the DP8228 system controller, others are INS8060A.

Note 2: Pin 23 of the INS8228 must be tied to +12V through a 1 kΩ resistor to generate the RST 7 instruction when an interrupt is acknowledged as required by the accompanying sample program.

FIGURE 10. ADC0801–INS8060A CPU Interface

SAMPLE PROGRAM FOR *FIGURE 10* ADC0801–INS8080A CPU INTERFACE

```
0038    C3 00 03    RST 7:      JMP     LD DATA
   •        •           •
   •        •           •
0100    21 00 02    START:      LXI H 0200H     ;HL pair will point to
                                                ;data storage locations
0103    31 00 04    RETURN:     LXI SP 0400H    ;Initialize stack pointer (Note 1)
0106    7D                      MOV A, L        ;Test # of bytes entered
0107    FE 0F                   CPI 0F H        ;If # = 16, JMP to
0109    CA 13 01                JZ CONT         ;user program
010C    D3 E0                   OUT E0 H        ;Start A/D
010E    FB                      EI              ;Enable interrupt
010F    00          LOOP:       NOP             ;Loop until end of
0110    C3 0F 01                JMP LOOP        ;conversion
0113       •        CONT:          •
   •       •           •           •
   •       •        (User program to           •
   •       •        process data)              •
   •       •           •                       •
   •       •           •                       •
0300    DB E0       LD DATA:    IN E0 H         ;Load data into accumulator
0302    77                      MOV M, A        ;Store data
0303    23                      INX H           ;Increment storage pointer
0304    C3 03 01                JMP RETURN
```

Note 1: The stack pointer must be dimensioned because a RST 7 instruction pushes the PC onto the stack.

Note 2: All address used were arbitrarily chosen.

Functional Description (Continued)

The standard control bus signals of the 8080 $\overline{CS}$, $\overline{RD}$ and $\overline{WR}$) can be directly wired to the digital control inputs of the A/D and the bus timing requirements are met to allow both starting the converter and outputting the data onto the data bus. A bus driver should be used for larger microprocessor systems where the data bus leaves the PC board and/or must drive capacitive loads larger than 100 pF.

4.1.1 Sample 8080A CPU Interfacing Circuitry and Program

The following sample program and associated hardware shown in *Figure 10* may be used to input data from the converter to the INS8080A CPU chip set (comprised of the INS8080A microprocessor, the INS8228 system controller and the INS8224 clock generator). For simplicity, the A/D is controlled as an I/O device, specifically an 8-bit bi-directional port located at an arbitrarily chosen port address, E0. The TRI-STATE output capability of the A/D eliminates the need for a peripheral interface device, however address decoding is still required to generate the appropriate $\overline{CS}$ for the converter.

It is important to note that in systems where the A/D converter is 1-of-8 or less I/O mapped devices, no address decoding circuitry is necessary. Each of the 8 address bits (A0 to A7) can be directly used as $\overline{CS}$ inputs—one for each I/O device.

4.1.2 INS8048 Interface

The INS8048 interface technique with the ADC0801 series (see *Figure 11*) is simpler than the 8080A CPU interface. There are 24 I/O lines and three test input lines in the 8048. With these extra I/O lines available, one of the I/O lines (bit 0 of port 1) is used as the chip select signal to the A/D, thus eliminating the use of an external address decoder. Bus control signals $\overline{RD}$, $\overline{WR}$ and $\overline{INT}$ of the 8048 are tied directly to the A/D. The 16 converted data words are stored at on-chip RAM locations from 20 to 2F (Hex). The $\overline{RD}$ and $\overline{WR}$ signals are generated by reading from and writing into a dummy address, respectively. A sample interface program is shown below.

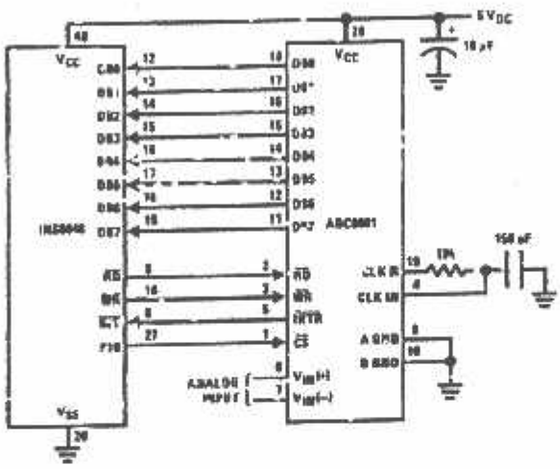

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FIGURE 11. INS8048 Interface

SAMPLE PROGRAM FOR *FIGURE 11* INS8048 INTERFACE

```
04 10                  JMP   10H        ; Program starts at addr 10
                       ORG   3H
04 50                  JMP   50H        ; Interrupt jump vector
                       ORG   10H        ; Main program
99 FE                  ANL   P1, #0FEH  ; Chip select
81                     MOVX  A, @R1     ; Read in the 1st data
                                        ; to reset the intr
89 01        START:    ORL   P1, #1     ; Set port pin high
B8 20                  MOV   R0, #20H   ; Data address
B9 FF                  MOV   R1, #0FFH  ; Dummy address
BA 10                  MOV   R2, #10H   ; Counter for 16 bytes
23 FF        AGAIN:    MOV   A, #0FFH   ; Set ACC for intr loop
99 FE                  ANL   P1, #0FEH  ; Send CS (bit 0 of P1)
91                     MOVX  @R1, A     ; Send WR out
05                     EN    I          ; Enable interrupt
96 21        LOOP:     JNZ   LOOP       ; Wait for interrupt
EA 1E                  DJNZ  R2, AGAIN  ; If 16 bytes are read
00                     NOP              ; go to user's program
00                     NOP
                       ORG   50H
81           INDATA:   MOVX  A, @R1     ; Input data, CS still low
A0                     MOV   @R0, A     ; Store in memory
18                     INC   R0         ; Increment storage counter
89 01                  ORL   P1, #1     ; Reset CS signal
27                     CLR   A          ; Clear ACC to get out of
93                     RETR             ; the interrupt loop
```

Functional Description (Continued)

4.2 Interfacing the Z-80

The Z-80 control bus is slightly different from that of the 8080. General $\overline{RD}$ and $\overline{WR}$ strobes are provided and separate memory request, $\overline{MREQ}$, and I/O request, $\overline{IORQ}$, signals are used which have to be combined with the generalized strobes to provide the equivalent 8080 signals. An advantage of operating the A/D in I/O space with the Z-80 is that the CPU will automatically insert one wait state (the $\overline{RD}$ and $\overline{WR}$ strobes are extended one clock period) to allow more time for the I/O devices to respond. Logic to map the A/D in I/O space is shown in *Figure 13*.

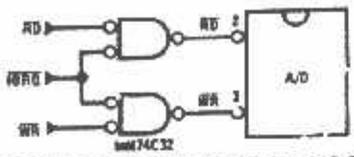


FIGURE 13. Mapping the A/D as an I/O Device for Use with the Z-80 CPU

Additional I/O advantages exist as software DMA routines are available and use can be made of the output data transfer which exists on the upper 8 address lines (A8 to A15) during I/O input instructions. For example, MUX channel selection for the A/D can be accomplished with this operating mode.

4.3 Interfacing 6800 Microprocessor Derivatives (6502, etc.)

The control bus for the 6800 microprocessor derivatives does not use the $\overline{RD}$ and $\overline{WR}$ strobe signals. Instead it employs a single R/$\overline{W}$ line and additional timing, if needed, can be derived fom the $\phi 2$ clock. All I/O devices are memory mapped in the 6800 system, and a special signal, VMA, indicates that the current address is valid. *Figure 14* shows an interface schematic where the A/D is memory mapped in the 6800 system. For simplicity, the $\overline{CS}$ decoding is shown using ½ DM8092. Note that in many 6800 systems, an already decoded $\overline{4/5}$ line is brought out to the common bus at pin 21. This can be tied directly to the $\overline{CS}$ pin of the A/D, provided that no other devices are addressed at HX ADDR: 4XXX or 5XXX.

The following subroutine performs essentially the same function as in the case of the 8080A interface and it can be called from anywhere in the user's program.

In *Figure 15* the ADC0801 series is interfaced to the M6800 microprocessor through (the arbitrarily chosen) Port B of the MC6820 or MC6821 Peripheral Interface Adapter, (PIA). Here the $\overline{CS}$ pin of the A/D is grounded since the PIA is already memory mapped in the M6800 system and no $\overline{CS}$ decoding is necessary. Also notice that the A/D output data lines are connected to the microprocessor bus under program control through the PIA and therefore the A/D $\overline{RD}$ pin can be grounded.

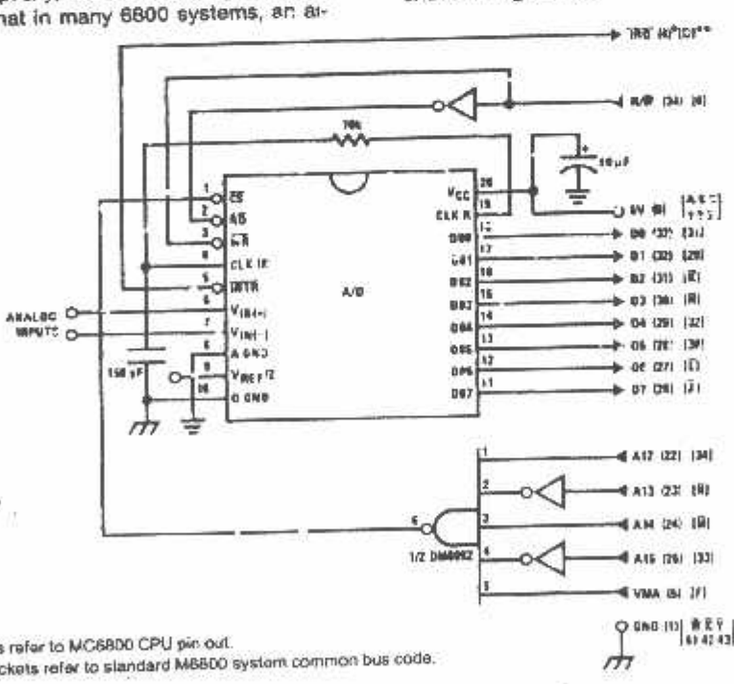
A sample interface program equivalent to the previous one is shown below *Figure 15*. The PIA Data and Control Registers of Port B are located at HEX addresses 8006 and 8007, respectively.

5.0 GENERAL APPLICATIONS

The following applications show some interesting uses for the A/D. The fact that one particular microprocessor is used is not meant to be restrictive. Each of these application circuits would have its counterpart using any microprocessor that is desired.

5.1 Multiple ADC0801 Series to MC6800 CPU Interface

To transfer analog data from several channels to a single microprocessor system, a multiple converter scheme presents several advantages over the conventional multiplexer single-converter approach. With the ADC0801 series, the differential inputs allow individual span adjustment for each channel. Furthermore, all analog input channels are sensed simultaneously, which essentially divides the microprocessor's total system servicing time by the number of channels, since all conversions occur simultaneously. This scheme is shown in *Figure 16*.



Note 1: Numbers in parentheses refer to MC6800 CPU pin out.
Note 2: Number or letters in brackets refer to standard M6800 system common bus code.

FIGURE 14. ADC0801-MC6800 CPU Interface

Functional Description (Continued)

SAMPLE PROGRAM FOR *FIGURE 14* ADC0801-MC6800 CPU INTERFACE

```
0010  DF 36     DATAIN  STX   TEMP2   ; Save contents of X
0012  CE 00 2C        LDX   #$002C  ; Upon IRQ low CPU
0015  FF FF F8        STX   $FFF8   ; Jumps to 002C
0018  B7 50 00        STAA  $5000   ; Start ADC0801
001B  0E              CLI
001C  3E        CONVRT  WAI         ; Wait for interrupt
001D  DE 34           LDX   TEMP1
001F  8C 02 0F        CPX   #$020F  ; Is final data stored?
0022  27 14           BEQ   ENDP
0024  B7 50 00        STAA  $5000   ; Restarts ADC0801
0027  08              INX
0028  DF 34           STX   TEMP1
002A  20 F0           BRA   CONVRT
002C  DE 34     INTRPT  LDX   TEMP1
002E  B6 50 00        LDAA  $5000   ; Read data
0031  A7 00           STAA  X       ; Store it at X
0033  3B              RTI
0034  02 00     TEMP1   FDB   $0200   ; Starting address for
                                      ; data storage
0036  00 00     TEMP2   FDB   $0000
0038  CE 02 00  ENDP    LDX   #$0200  ; Reinitialize TEMP1
003B  DF 34           STX   TEMP1
003D  DE 36           LDX   TEMP2
003F  39              RTS
                                      ; Return from subroutine
                                      ; To user's program
```

Note 1: In order for the microprocessor to service subroutines and interrupts, the stack pointer must be dimensioned in the user's program

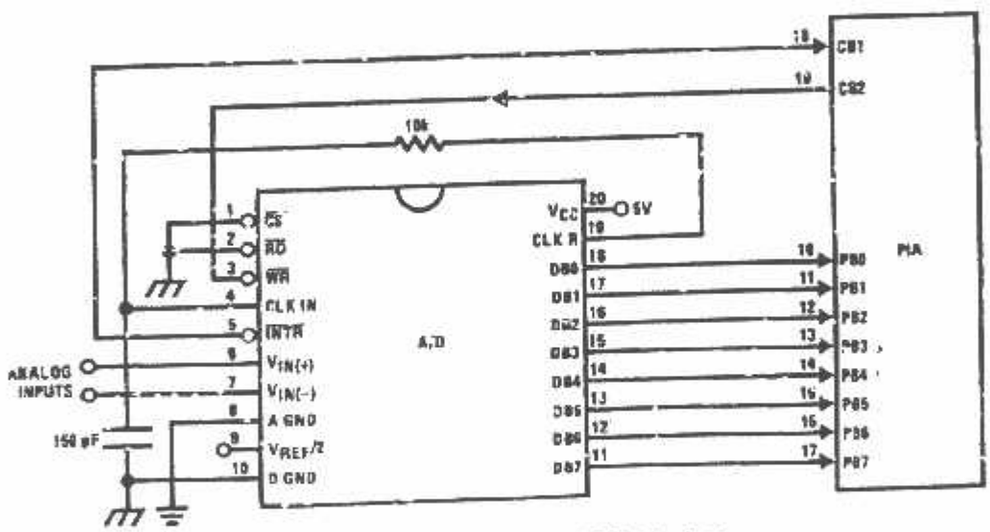


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FIGURE 15. ADC0801–MC6820 PIA Interface

Functional Description (Continued)

SAMPLE PROGRAM FOR *FIGURE 15* ADC0801–MC6820 PIA INTERFACE

```
0010  CE 00 38   DATAIN   LDX   #$0038    ; Upon IRQ low CPU
0013  FF FF F8           STX   $FFF8     ; jumps to 0038
0016  B6 80 06           LDAA  PIAORB    ; Clear possible IRQ flags
0019  4F                 CLRA
001A  B7 80 07           STAA  PIACRB
001D  B7 80 06           STAA  PIAORB    ; Set Port B as input
0020  0E                 CLI
0021  C6 34              LDAB  #$34
0023  86 3D              LDAA  #$3D
0025  F7 80 07   CONVRT  STAB  PIACRB    ; Starts ADC0801
0028  B7 80 07           STAA  PIACRB
002B  3E                 WAI             ; Wait for interrupt
002C  DE CC              LDX   TEMP1
002E  8C 02 0F           CPX   #$020F    ; Is final data stored?
0031  27 CF              BEQ   ENDP
0033  08                 INX
0034  DF 40              STX   TEMP1
0036  20 ED              BRA   CONVRT
0038  DE 40      INTRPT LDX   TEMP1
003A  B6 80 06           LDAA  PIACRB    ; Read data in
003D  A7 00              STAA  X         ; Store it at X
003F  3B                 RTI
0040  02 00      TEMP1  FDB   $0200      ; Starting address for
                                         ; data storage
0042  CE 02 00   ENDP   LDX   #$0200     ; Reinitialize TEMP1
0045  DF 40              STX   TEMP1
0047  39                 RTS             ; Return from subroutine
                 PIAORB EQU   $8006      ; To user's program
                 PIACRB EQU   $8007
```

The following schematic and sample subroutine (DATA IN) may be used to interface (up to) 8 ADC0801's directly to the MC6800 CPU. This scheme can easily be extended to allow the interface of more converters. In this configuration the converters are (arbitrarily) located at HEX address 5000 in the MC6800 memory space. To save components, the clock signal is derived from just one RC pair on the first converter. This output drives the other A/Ds.

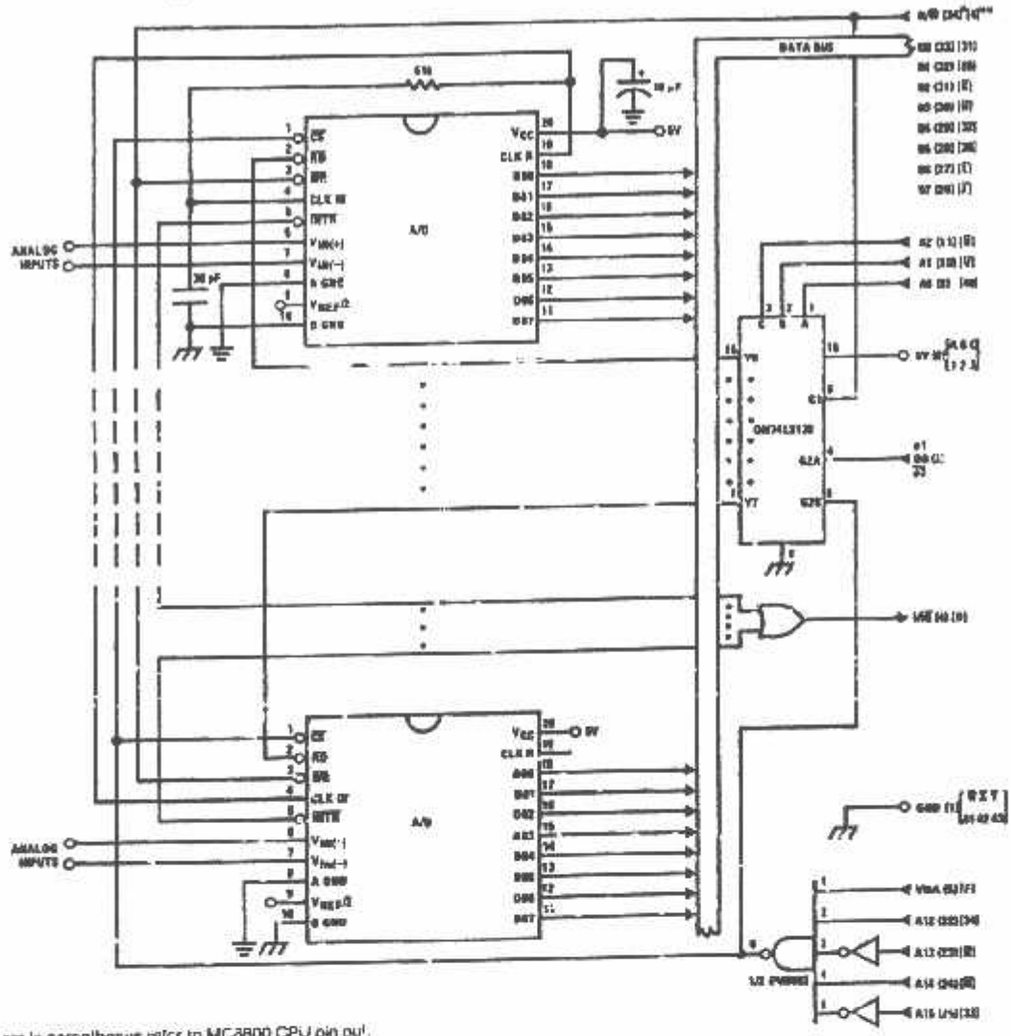
All the converters are started simultaneously with a STORE instruction at HEX address 5000. Note that any other HEX address of the form 5XXX will be decoded by the circuit, pulling all the $\overline{CS}$ inputs low. This can easily be avoided by using a more definitive address decoding scheme. All the interrupts are ORed together to insure that all A/Ds have completed their conversion before the microprocessor is interrupted.

The subroutine, DATA IN, may be called from anywhere in the user's program. Once called, this routine initalizes the CPU, starts all the converters simultaneously and waits for the interrupt signal. Upon receiving the interrupt, it reads the converters (from HEX addresses 5000 through 5007) and stores the data successively at (arbitrarily chosen) HEX addresses 0200 to 0207, before returning to the user's program. All CPU registers then recover the original data they had before servicing DATA IN.

5.2 Auto-Zeroed Differential Transducer Amplifier and A/D Converter

The differential inputs of the ADC0801 series eliminate the need to perform a differential to single ended conversion for a differential transducer. Thus, one op amp can be eliminated since the differential to single ended conversion is provided by the differential input of the ADC0801 series. In general, a transducer preamp is required to take advantage of the full A/D converter input dynamic range.

Functional Description (Continued)



Note 1: Numbers in parentheses refer to MC6800 CPU pin out.

Note 2: Numbers or letters in brackets refer to standard M6800 system common bus code.

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FIGURE 16. Interfacing Multiple A/Ds in an MC6800 System

SAMPLE PROGRAM FOR *FIGURE 16* INTERFACING MULTIPLE A/Ds IN AN MC6800 SYSTEM

ADDRESS	HEX CODE	MNEMONICS			COMMENTS
0010	DF 44	DATAIN	STX	TEMP	; Save Contents of X
0012	CE 00 2A		LDX	#$002A	; Upon $\overline{IRQ}$ LOW CPU
0015	FF FF F8		STX	$FFF8	; Jumps to 002A
0018	B7 50 00		STAA	$5C00	; Starts all A/D's
001B	0E		CLI		
001C	3E		WAI		; Wait for interrupt
001D	CE 50 00		LDX	#$5000	
0020	DF 40		STX	INDEX1	; Reset both INDEX
0022	CE 02 00		LDX	#$0200	; 1 and 2 to starting
0025	DF 42		STX	INDEX2	; addresses
0027	DE 44		LDX	TEMP	
0029	39		RTS		; Return from subroutine
002A	DE 40	INTRPT	LDX	INDEX1	; INDEX1 → X
002C	A6 00		LDAA	X	; Read data in from A/D at X
002E	08		INX		; Increment X by one
002F	DF 40		STX	INDEX1	; X → INDEX1
0031	DE 42		LDX	INDEX2	; INDEX2 → X

Functional Description (Continued)

SAMPLE PROGRAM FOR *FIGURE 16* INTERFACING MULTIPLE A/Ds IN AN MC6800 SYSTEM

ADDRESS	HEX CODE		MNEMONICS		COMMENTS
0033	A7 00		STAA	X	;Store data at X
0035	8C 02 07		CPX	#$0207	;Have all A/D's been read?
0038	27 05		BEQ	RETURN	;Yes: branch to RETURN
003A	08		INX		;No: increment X by one
003B	DF 42		STX	INDEX2	;X → INDEX2
003D	20 EB		BRA	INTRPT	;Branch to 002A
003F	3B	RETURN	RTI		
0040	50 00	INDEX1	FDB	$5000	;Starting address for A/D
0042	02 00	INDEX2	FDB	$0200	;Starting address for data storage
0044	00 00	TEMP	FDB	$0000	

Note 1: In order for the microprocessor to service subroutines and interrupts, the stack pointer must be dimensioned in the user's program.

For amplification of DC input signals, a major system error is the input offset voltage of the amplifiers used for the preamp. *Figure 17* is a gain of 100 differential preamp whose offset voltage errors will be cancelled by a zeroing subroutine which is performed by the INS8080A microprocessor system. The total allowable input offset voltage error for this preamp is only 50 μV for ¼ LSB error. This would obviously require very precise amplifiers. The expression for the differential output voltage of the preamp is:

$$V_O = \underbrace{[V_{IN}(+) - V_{IN}(-)]}_{\text{SIGNAL}} \underbrace{\left[1 + \frac{2R2}{R1}\right]}_{\text{GAIN}} +$$

$$\underbrace{(V_{OS_2} - V_{OS_1} - V_{OS_3} \pm I_X R_X)}_{\text{DC ERROR TERM}} \underbrace{\left(1 + \frac{2R2}{R1}\right)}_{\text{GAIN}}$$

where I_X is the current through resistor R_X. All of the offset error terms can be cancelled by making $\pm I_X R_X = V_{OS1} + V_{OS3} - V_{OS2}$. This is the principle of this auto-zeroing scheme.

The INS8080A uses the 3 I/O ports of an INS8255 Programable Peripheral Interface (PPI) to control the auto zeroing and input data from the ADC0801 as shown in *Figure 18*. The PPI is programmed for basic I/O operation (mode 0) with Port A being an input port and Ports B and C being output ports. Two bits of Port C are used to alternately open or close the 2 switches at the input of the preamp. Switch SW1 is closed to force the preamp's differential input to be zero during the zeroing subroutine and then opened and SW2 is then closed for conversion of the actual differential input signal. Using 2 switches in this manner eliminates concern for the ON resistance of the switches as they must conduct only the input bias current of the input amplifiers.

Output Port B is used as a successive approximation register by the 8080 and the binary scaled resistors in series with each output bit create a D/A converter. During the zeroing subroutine, the voltage at V_X increases or decreases as required to make the differential output voltage equal to zero. This is accomplished by ensuring that the voltage at the output of A1 is approximately 2.5V so that a logic "1" (5V) on any output of Port B will source current into node V_X thus raising the voltage at V_X and making the output differential more negative. Conversely, a logic "0" (0V) will pull current out of node V_X and decrease the voltage, causing the differential output to become more positive. For the resistor values shown, V_X can move ±12 mV with a resolution of 50 μV, which will null the offset error term to ¼ LSB of full-scale for the ADC0801. It is important that the voltage levels that drive the auto-zero resistors be constant. Also, for symmetry, a logic swing of 0V to 5V is convenient. To achieve this, a CMOS buffer is used for the logic output signals of Port B and this CMOS package is powered with a stable 5V source. Buffer amplifier A1 is necessary so that it can source or sink the D/A output current.

A flow chart for the zeroing subroutine is shown in *Figure 19*. It must be noted that the ADC0801 series will output an all zero code when it converts a negative input [$V_{IN}(-) \geq V_{IN}(+)$]. Also, a logic inversion exists as all of the I/O ports are buffered with inverting gates.

Basically, if the data read is zero, the differential output voltage is negative, so a bit in Port B is cleared to pull V_X more negative which will make the output more positive for the next conversion. If the data read is not zero, the output voltage is positive so a bit in Port B is set to make V_X more positive and the output more negative. This continues for 8 approximations and the differential output eventually converges to within 5 mV of zero.

The actual program is given in *Figure 20*. All addresses used are compatible with the BLC 80/10 microcomputer system. In particular:

Port A and the ADC0801 are at port address E4

Port B is at port address E5

Port C is at port address E6

PPI control word port is at port address E7

Program Counter automatically goes to ADDR:3C3D upon acknowledgement of an interrupt from the ADC0801

5.3 Multiple A/D Converters in a Z-80 Interrupt Driven Mode

In data acquisition systems where more than one A/D converter (or other peripheral device) will be interrupting program execution of a microprocessor, there is obviously a need for the CPU to determine which device requires servicing. *Figure 21* and the accompanying software is a method of determining which of 7 ADC0801 converters has completed a conversion ($\overline{INTR}$ asserted) and is requesting an interrupt. This circuit allows starting the A/D converters in any sequence, but will input and store valid data from the converters with a priority sequence of A/D 1 being read first, A/D 2 second, etc., through A/D 7 which would have the lowest priority for data being read. Only the converters whose $\overline{INT}$ is asserted will be read.

The key to decoding circuitry is the DM74LS373, 8-bit D type flip-flop. When the Z-80 acknowledges the interrupt, the program is vectored to a data input Z-80 subroutine. This subroutine will read a peripheral status word from the DM74LS373 which contains the logic state of the $\overline{INTR}$ outputs of all the converters. Each converter which initiates an interrupt will place a logic "0" in a unique bit position in the status word and the subroutine will determine the identity of the converter and execute a data read. An identifier word (which indicates which A/D the data came from) is stored in the next sequential memory location above the location of the data so the program can keep track of the identity of the data entered.

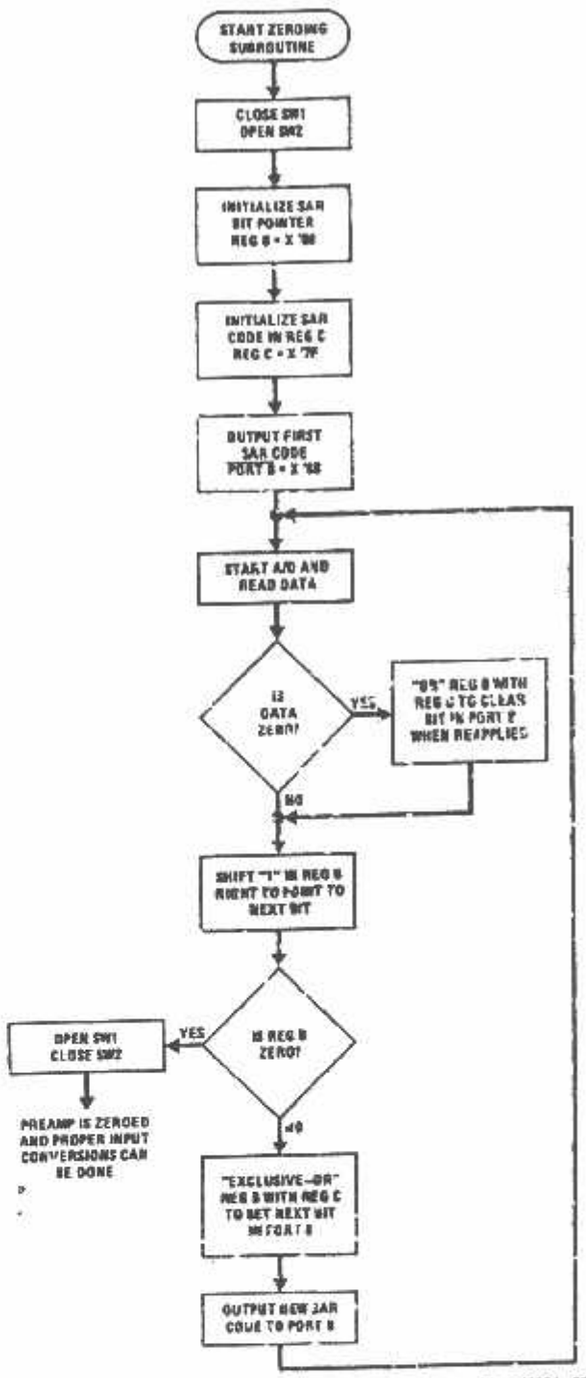

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FIGURE 19. Flow Chart for Auto-Zero Routine

```
3D00  3E90    MVI 90                          ;Program PPI
3D02  D3E7    Out Control Port
3D04  2601    MVI H 01        Auto-Zero Subroutine
3D06  7C      MOV A,H                         ;Close SW1 open SW2
3D07  D3E6    OUT C                           ;Initialize SAR bit pointer
3D09  0680    MVI B 80                        ;Initialize SAR code
3D0B  3E7F    MVI A 7F
3D0D  4F      MOV C,A         Return          ;Port B = SAR code
3D0E  D3E5    OUT B
3D10  31AA3D  LXI SP 3DAA     Start           ;Dimension stack pointer
3D13  D3E4    OUT A                           ;Start A/D
3D15  FB      IE
3D16  00      NOP             Loop            ;Loop until INT asserted
3D17  C3163D  JMP Loop
3D1A  7A      MOV A,D         Auto-Zero
3D1B  C600    ADI 00                          ;Test A/D output data for zero
3D1D  CA2D3D  JZ Set C
3D20  78      MOV A,B         Shift B         ;Clear carry
3D21  F600    ORI 00                          ;Shift "1" in B right one place
3D23  1F      RAR                             ;Is F zero? If yes last
3D24  FE0C    CPI 00                          ;approximation has been made
3D26  CA373D  JZ Done
3D29  47      MOV b,A
3D2A  C3333D  JMP New C
3D2D  79      MOV A,C         Set C           ;Set bit in C that is in same
3D2E  B0      ORA B                           ;position as "1" in B
3D27  4F      MOV C,A
3D30  C3203D  JMP Shift B
3D33  A9      XRA C           New C           ;Clear bit in C that is in
3D34  C30D3D  JMP Return                      ;same position as "1" in B
3D37  47      MOV B,A         Done            ;then output new SAR code.
3D38  7C      MOV A,H                         ;Open SW1, close SW2 then
3D39  EE03    XRI 03                          ;proceed with program. Preamp
3D3B  D3E6    OUT C                           ;is now zeroed.
3D3D          •               Normal
              •
              •
              Program for processing
              proper data values
3C3D  DBE4    IN A            Read A/D Subroutine  ;Read A/D data
3C3F  EEFF    XRI FF                               ;Invert data
3C41  57      MOV D,A
3C42  78      MOV A,B                              ;Is B Reg = 0? If not stay
3C43  E6FF    ANI FF                               ;in auto zero subroutine
3C45  C21A3D  JNZ Auto-Zero
3C48  C33D3D  JMP Normal
```

Note: All numerical values are hexadecimal representations.

FIGURE 20. Software for Auto-Zeroed Differential A/D

5.3 Multiple A/D Converters in a Z-80® Interrupt Driven Mode (Continued)

The following notes apply:

1) It is assumed that the CPU automatically performs a RST 7 instruction when a valid interrupt is acknowledged (CPU is in interrupt mode 1). Hence, the subroutine starting address of X0038.

2) The address bus from the Z-80 and the data bus to the Z-80 are assumed to be inverted by bus drivers.

3) A/D data and identifying words will be stored in sequential memory locations starting at the arbitrarily chosen address X 3E00.

4) The stack pointer must be dimensioned in the main program as the RST 7 instruction automatically pushes the PC onto the stack and the subroutine uses an additional 6 stack addresses.

5) The peripherals of concern are mapped into I/O space with the following port assignments:

HEX PORT ADDRESS	PERIPHERAL
00	MM74C374 8-bit flip-flop
01	A/D 1
02	A/D 2
03	A/D 3
04	A/D 4
05	A/D 5
06	A/D 6
07	A/D 7

This port address also serves as the A/D identifying word in the program.

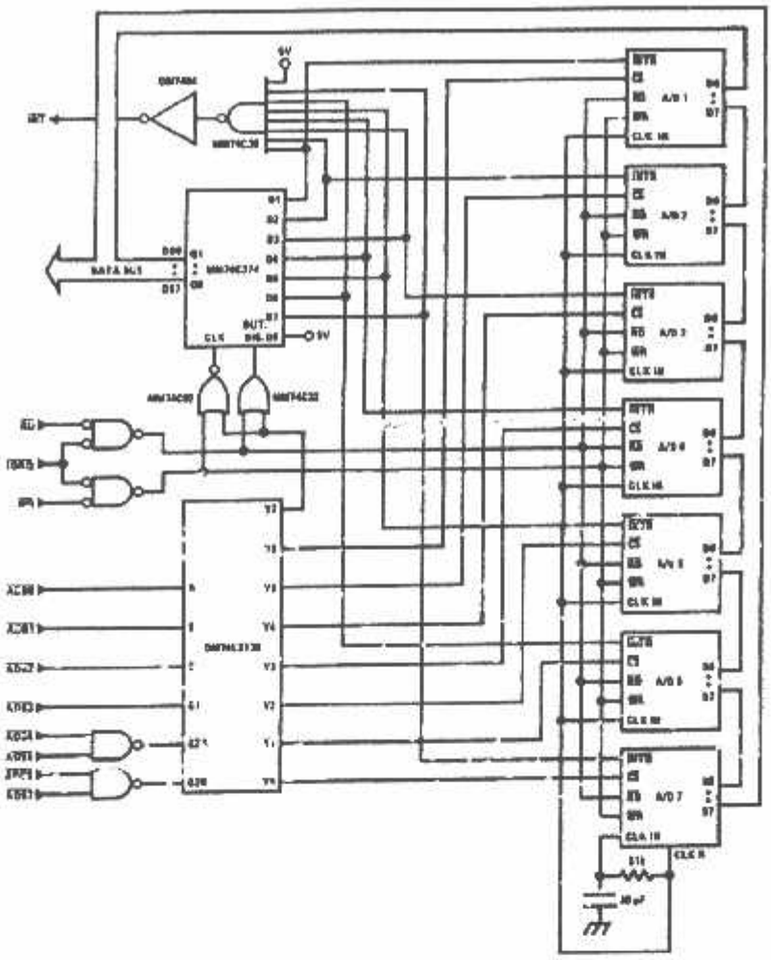

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FIGURE 21. Multiple A/Ds with Z-80 Type Microprocessor

INTERRUPT SERVICING SUBROUTINE

LOC	OBJ CODE	SOURCE STATEMENT		COMMENT
0038	E5		PUSH HL	; Save contents of all registers affected by
0039	C5		PUSH BC	; this subroutine.
003A	F5		PUSH AF	; Assumed INT mode 1 earlier set.
003B	21 00 3E		LD (HL), X3E00	; Initialize memory pointer where data will be stored.
003E	0E 01		LD C, X01	; C register will be port ADDR of A/D converters.
0040	D300		OUT X00, A	; Load peripheral status word into 8-bit latch,
0042	DB00		IN A, X00	; Load status word into accumulator.
0044	47		LD B, A	; Save the status word.
0045	79	TEST	LD A, C	; Test to see if the status of all A/D's have
0046	FE 08		CP, X03	; been checked. If so, exit subroutine
0048	CA 60 00		JPZ, DONE	
004B	78		LD A, B	; Test a single bit in status word by looking for
004C	1F		RRA	; a "1" to be rotated into the CARRY (an INT
004D	47		LD B, A	; is loaded as a "1"). If CARRY is set then load
004E	DA 550C		JFC, LOAD	; contents of A/D at port ADDR in C register.
0051	0C	NEXT	INC C	; If CARRY is not set, increment C register to point
0052	C3 4500		JP, TEST	; to next A/D, then test next bit in status word.
0055	ED 78	LOAD	IN A, (C)	; Read data from interrupting A/D and invert
0057	EE FF		XOR FF	; the data.
0059	77		LD (HL), A	; Store the data
005A	2C		INC L	
005B	71		LD (HL), C	; Store A/D identifier (A/D port ADDR).
005C	2C		INC L	
005D	C3 51 00		JP, NEXT	; Test next bit in status word.
0060	F1	DONE	POP AF	; Re-establish all registers as they were
0061	C1		POP BC	; before the interrupt.
0062	E1		POP HL	
0063	C9		RET	; Return to original program

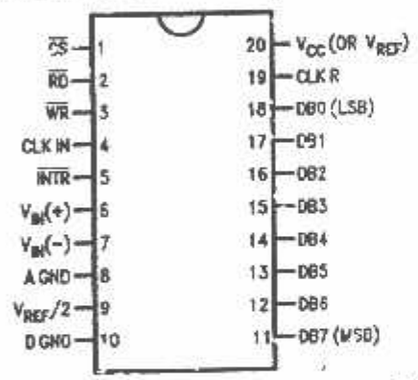
Ordering Information

TEMP RANGE		0°C TO 70°C	0°C TO 70°C	0°C TO 70°C	−40°C TO +85°C
ERROR	± ¼ Bit Adjusted				ADC0801LCN
	± ½ Bit Unadjusted	ADC0802LCWM	ADC0802LCV		ADC0802LCN
	± ½ Bit Adjusted	ADC0803LCWM	ADC0803LCV		ADC0803LCN
	± 1Bit Unadjusted	ADC0804LCWM	ADC0804LCV	ADC0804LCN	ADC0805LCN
PACKAGE OUTLINE		M20B—Small Outline	V20A—Chip Carrier	N20A—Molded DIP	

TEMP RANGE		−40°C TO +85°C	−55°C TO +125°C
ERROR	± ¼ Bit Adjusted	ADC0801LCJ	ADC0801LJ
	± ½ Bit Unadjusted	ADC0802LCJ	ADC0802LJ, ADC0802LJ/883
	± ½ Bit Adjusted	ADC0803LCJ	
	± 1Bit Unadjusted	ADC0804LCJ	
PACKAGE OUTLINE		J20A—Cavity DIP	J20A—Cavity DIP

Connection Diagrams

ADC080X
Dual-In-Line and Small Outline (SO) Packages



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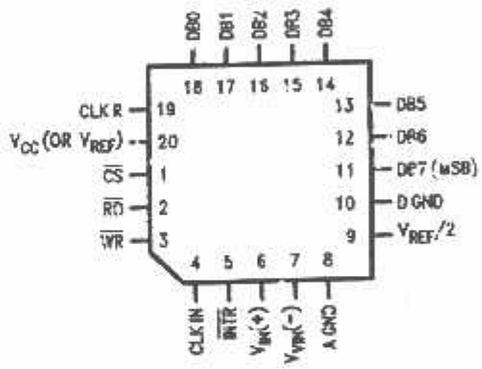
ADC080X
Molded Chip Carrier (PCC) Package



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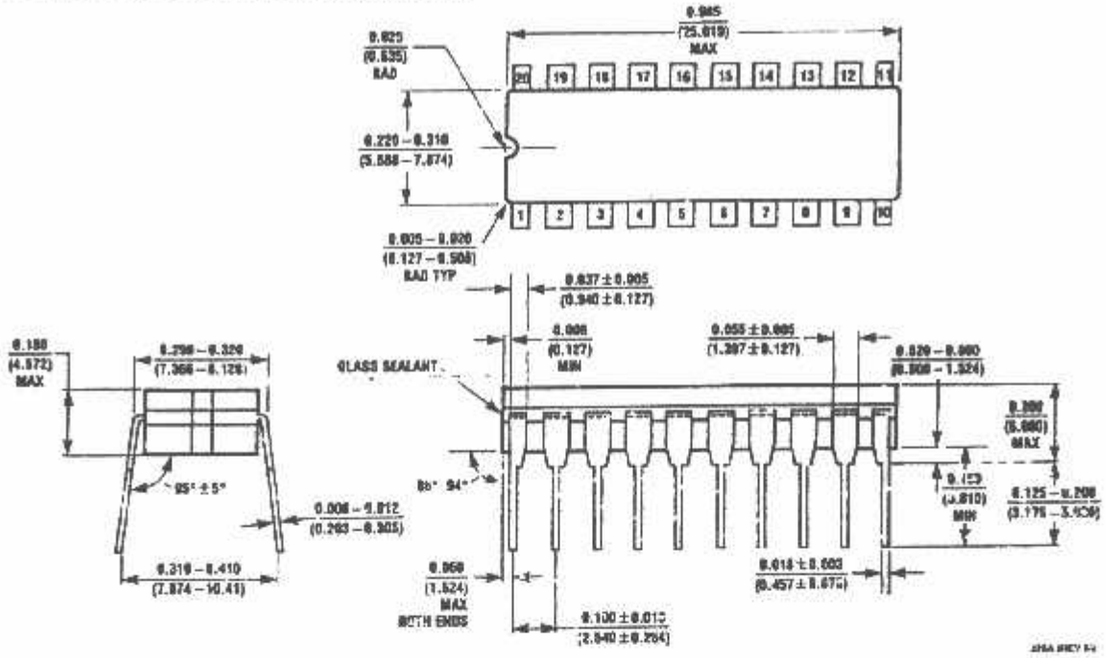
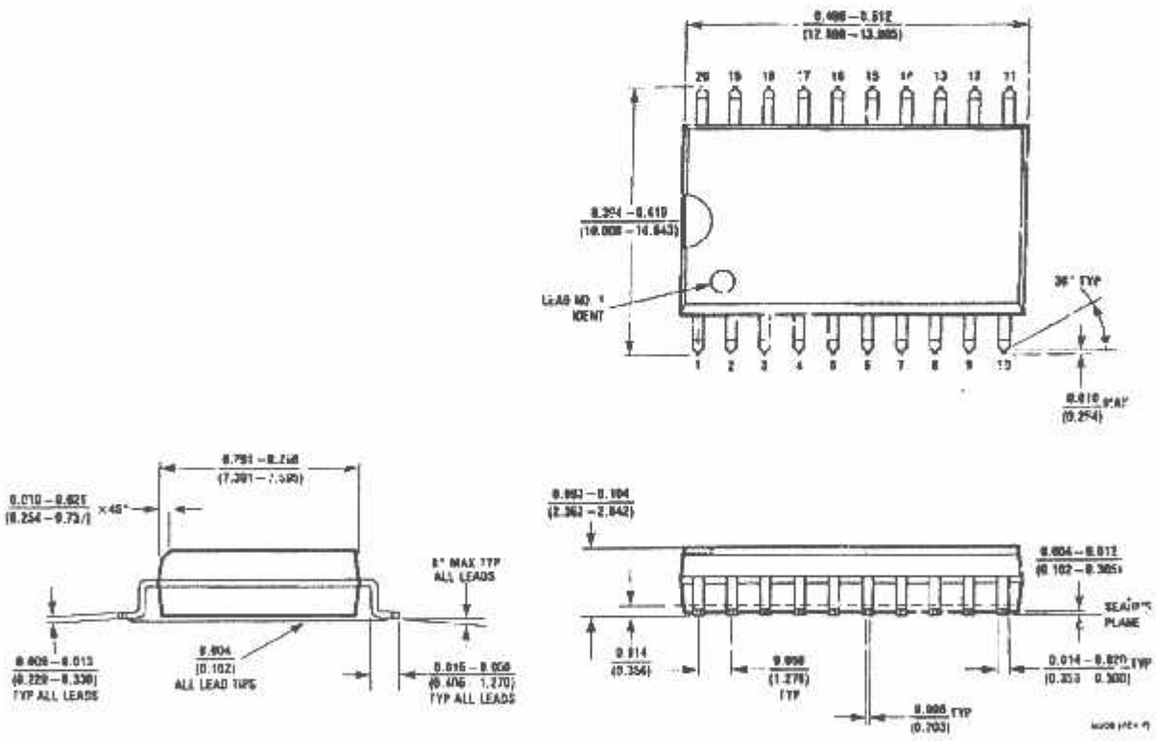
See Ordering Information

Physical Dimensions inches (millimeters)

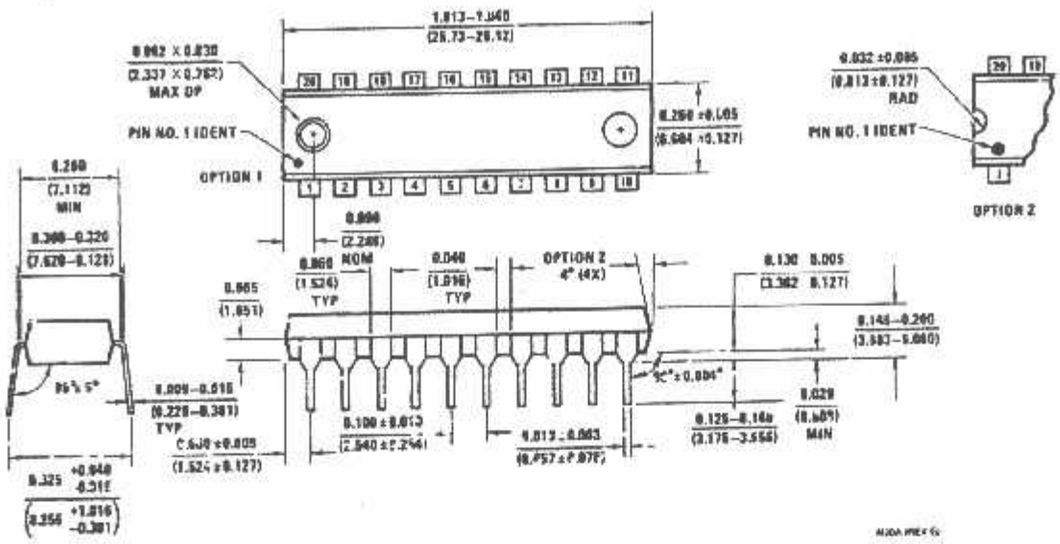


Dual-In-Line Package (J)
Order Number ADC0801LJ, ADC0802LJ, ADC0801LCJ,
ADC0802LCJ, ADC0803LCJ or ADC0804LCJ
ADC0802LJ/883 or 5962-9096601MRA
NS Package Number J20A



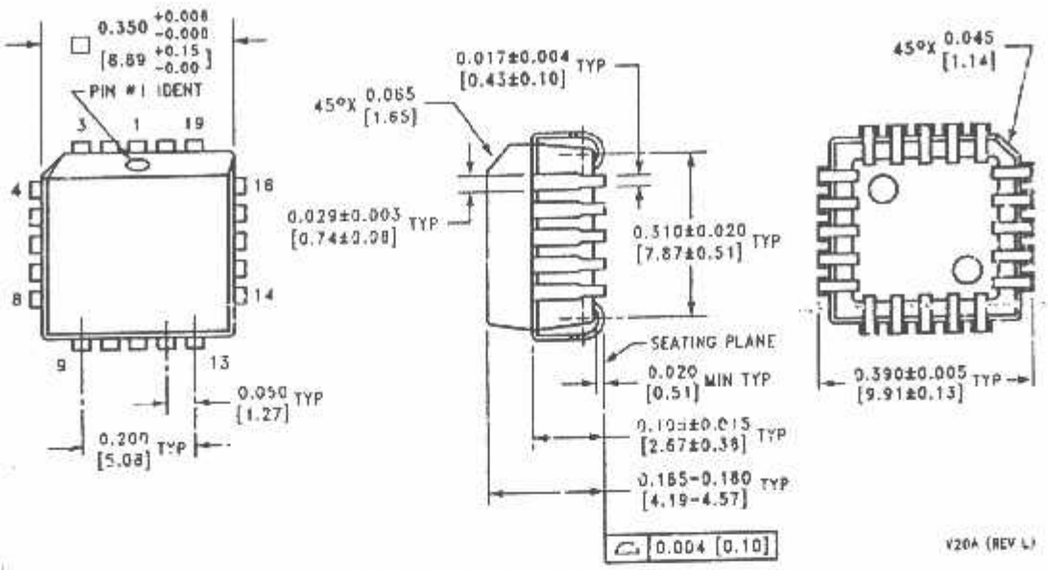
SO Package (M)
Order Number ADC0802LCWM, ADC0803LCWM or ADC0804LCWM
NS Package Number M20B

Physical Dimensions inches (millimeters) (Continued)



Molded Dual-In-Line Package (N)
Order Number ADC0801LCN, ADC0802LCN,
ADC0803LCN, ADC0804LCN or ADC0805LCN
NS Package Number N20A

Physical Dimensions inches (millimeters) (Continued)



Molded Chip Carrier Package (V)
Order Number ADC0802LCV, ADC0803LCV or ADC0804LCV
NS Package Number V20A

LIFE SUPPORT POLICY

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1. Life support devices or systems are devices or systems which, (a) are intended for surgical implant into the body, or (b) support or sustain life, and whose failure to perform, when properly used in accordance with instructions for use provided in the labeling, can be reasonably expected to result in a significant injury to the user.
2. A critical component is any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

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PROGRAM STUDI TEKNIK ELEKTRONIKA
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Tanggal	: 22 Maret 2007
Dengan nilai	: 75,50 (B+)

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