PERENCANAAN DAN PEMBUATAN ALAT PENGENDALI LAMPU DAN PINTU JARAK JAUH BERBASIS MIKROKONTROLER AT89S52

TUGAS AKHIR

Disusun Oleh :

Agustinus Ruddy Catur Utomo

NIM : 03.57.015

KONSENTRASI ELEKTRONIKA

JURUSAN TEKNIK ELEKTRO D - III

FAKULTAS TEKNOLOGI INDUSTRI

INSTITUT TEKNOLOGI NASIONAL MALANG

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LEMBAR PERSETUJUAN

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Diajukan Guna Memenuhi Salah Satu Syarat Untuk Memperoleh Gelar Pada

Jurusan Teknik Elektro D-III Konsentrasi Elektronika.

Disusun Oleh :

Agustinus Ruddy Catur Utomo

NIM : 03. 57. 015

Mengetahui:

Ketua Jurusan	Diperiksa dan disetujui
Teknik Elektro D-III	Dosen Pembimbing
(Ir. Choirul Saleh, MT)	(Ir. Kartiko Adi Widodo, MT)

KONSENTRASI ELEKTRONIKA
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ABSTRAK

Perencanaan dan Pembuatan Alat Pengendali Lampu dan Pintu Jarak Jauh Berbasis Mikrokontroller AT89S52, Agustinus Ruddy Catur Utomo, 0357015, Konsentrasi Elektronika, Jurusan Teknik Elektro DIII, Fakultas Teknologi Industri, Ir. Kartiko Adi Widodo, MT, Institut Teknologi Nasional Malang, 2007.

Dalam Tugas Akhir ini direalisasikan sebuah alat yang dapat melakukan pengontrolan on-off dengan menggunakan SMS (short message service). Pengontrolan ini tidak bergantung jarak antara pengontrol dan alat yang di kontrol, sehingga sangat menguntungkan bila terdapat jarak yang cukup jauh antara pengontrol dengan alat yang di kontrol. Pengontrolan ini bersifat mobile karena pengontrol cukup membawa sebuah handphone, dan biaya yang di gunakan untuk pengontrolan cukup murah. Alat ini dibuat dengan menggunakan pengendali mikro AT89S52 sebagai modul utama.

Untuk sistem pewaktuan alat, digunakan IC RTC (real time clock). Pada alat yang di kontrol terdapat suatu sistem untuk mengirim dan menerima SMS, dalam Tugas Akhir ini digunakan handphone C35. Sedangkan untuk pengontrolan dapat digunakan sembarang handphone dengan fasilitas SMS. Alat ini memiliki delapan jalur keluaran yang berarti alat ini dapat mengendalikan delapan piranti. Di dalam alat ini terdapat fasilitas untuk menghidupkan atau mematikan keluaran dengan interval waktu tertentu. Alat ini sudah diuji dengan menggunakan enam port keluaran untuk lampu dan dua port keluaran untuk motor DC, dimana setiap keluaran diberikan rangkaian driver untuk menyalakan lampu dan menggerakan motor. Bentuk pengujiannya adalah dengan mencoba mematikan atau menghidupkan kedelapan rangkaian yang dikendalikan dalam interval waktu tertentu.

Kata Kunci : *Short Message Service*, Real Time Clock, Handphone C35, Mikrikontroler AT89S52.

KATA PENGANTAR

Puji dan syukur kepada Tuhan Yang Maha Esa karena atas segala berkat dan rahmad – Nya penyusun dapat menyelesaikan Tugas Akhir ini dengan judul **Perencanaan dan Pembuatan Alat Pengendali Lampu dan Pintu Jarak Jauh Berbasis Mikrokontroller AT89S52** dengan baik dan lancar sampai akhirnya penyusun dapat menyelesaikan laporan ini. Pada kesempatan ini penyusun ingin menyampaikan rasa terimakasih atas segala bekal ilmu dan bimbingan yang telah diperoleh selama melaksanakan studi di INSTITUT TEKNOLOGI NASIONAL MALANG. Dengan ini saya menyampaikan terimakasih kepada :

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Penyusunan Laporan Tugas Akhir ini diharapkan dapat bermanfaat bagi penyusun pada khususnya dan pembaca pada umumnya. Penyusun menyadari bahwa laporan ini masih banyak kekurangannya, Oleh karena itu, kritik dan saran yang sifatnya membangun sangat diharapkan demi kesempurnaan laporan ini, Terima kasih.

Malang, Maret 2007

Penyusun

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DAFTAR FLOWCHART

BAB I

PENDAHULUAN

1.1. Latar Belakang

Kemajuan teknologi saat ini sangat pesat, dan tidak dapat dipungkiri bahwa semua kemajuan teknologi ini semakin mempermudah kita untuk melakukan pekerjaan sehari-hari. Misal saja pengontrolan – pengontrolan secara jarak jauh, kapanpun dan dimanapun kita berada, kita dapat melakukan pekerjaan kita. Pengontrolan secara jarak jauh melalui internet merupakan teknologi yang sangat menguntungkan karena pengontrolan ini tidak tergantung jarak dan waktu tetapi pengontrolan melalui internet ini memiliki beberapa kelemahan antara lain :

1. Pengontrolan harus selalu membawa komputer yang juga harus selalu *online* atau tersambung ke internet.
2. Untuk bagian yang di kontrol juga harus menyediakan PC yang harus *standbay* dan *online*

Adapun pengontrolan secara jarak jauh melalui telepon rumah, pengontrolan ini memiliki kelebihan karena sistem pengontrolan ini tidak membutuhkan sebuah PC, tetapi apabila pihak pengontrol berada di luar kota, maka pulsa telepon untuk melakukan pengontrolan cukup mahal apalagi alat yang dikontrol lebih dari satu dan itu membutuhkan waktu yang mungkin tidak sebentar.

Berangkat dari masalah-masalah di atas maka penulis berusaha merancang dan merealisasikan alat pengontrolan jarak jauh dengan menggunakan SMS (*short*

message service). Pengontrolan dengan menggunakan SMS memiliki beberapa keuntungan sekaligus, antara lain :

1. Pengontrolan dengan SMS tidak tergantung waktu dan jarak.
2. Tidak membutuhkan PC yang harus *online*.
3. Biaya pengiriman SMS relatif murah.
4. Pengontrolan ini bersifat *mobile*, karena pengontrolan cukup membawa sebuah *handphone*.

Pengontrolan dengan SMS ini cukup menguntungkan mengingat pengontrolan dengan sistem ini hanya membutuhkan *handphone* dan jaringan GSM pada daerah yang dikontrol dan pengontrol.

1.2. Rumusan Masalahan

Berdasarkan hal tersebut diatas timbul permasalahan

1. Bagaimana cara kerja sebuah SMS untuk bisa digunakan sebagai pengendali alat.
2. Bagaimana merancang dan membuat rangkaian interface antara HP, Mikro, dan RTC untuk mengendalikan lampu dan pintu.
3. Bagaimana membuat perangkat lunak di HP maupun Mikro untuk mengedalikan alat tersebut.

1.3. Batasan Masalah

Tugas akhir ini merancang dan merealisasikan alat yang dapat melakukan pengontrolan jarak jauh dengan menggunakan fasilitas SMS (*short message service*)

pada *handphone* (telepon genggam). Adapun spesifikasi alat yang dirancang adalah sebagai berikut :

1. Informasi yang di kirim dan di terima berupa SMS (*short message service*) di *handphone*.
2. Dapat mengendalikan alat dalam interval waktu tertentu.
3. Menggunakan *handphone SIEMEN C35*.
4. Menggunakan sistem minimum berbasis mikrokontroller AT89S52.
5. Hanya digunakan untuk mengendalikan 8 piranti yaitu berupa 6 lampu dan 1 pintu.

1.4. Tujuan

Tujuan dari pembuatan alat ini adalah untuk mengendalikan dan mengontrol lampu maupun pintu secara jarak jauh.

1.5. Metodologi Pembahasan

Metodologi pembahasan alat dilakukan dengan beberapa tahap antara lain:

1. Metoda kepustakaan, yaitu penulis melakukan studi literatur tentang permasalahan yang ada melalui perpustakaan dan internet.
2. Metoda percobaan, yaitu penulis melakukan berbagai percobaan di dalam menyelesaikan alat.
3. Metoda perencanaan alat, yaitu penulis membuat alat dengan menggabungkan berbagai data dan rangkian yang penulis dapatkan.

1.5.1. Sistematika Penulisan

Adapun sistematika penulisan yang di gunakan pada tugas akhir ini adalah sebagai berikut:

BAB I : PENDAHULUAN

Berisi tentang latar belakang, maksud dan tujuan, batasan masalah, sitematika penulisan dan relevansi penulisan tugas akhir ini.

BAB II : LANDASAN TEORI

Membahas mengenai teori dasar yang menunjang perencanaan dan pembuatan alat serta teori dasar alat-alat pendukung lainnya.

BAB III : REALISASI RANGKAIAN

Pada bab ini berisi penjelasan mengenai cara kerja dan analisa dari masing-masing blok diagram secara garis besar serta skema rangkaian secara keseluruhan.

BAB IV : PENGUJIAN ALAT

Membahas tentang cara pengujian dan hasil pengujian sistem yang telah di realisasikan.

BAB V : PENUTUP

Berisi kesimpulan dan saran-saran pengembangannya.

BAB II

LANDASAN TEORI

Landasan teori sangat membantu untuk dapat memahami suatu sistem. Selain dari pada itu dapat juga dijadikan sebagai bahan acuan didalam merencanakan suatu sistem. Dengan pertimbangan hal-hal tersebut, maka landasan teori merupakan bagian yang harus dipahami untuk pembahasan selanjutnya.

2.1. Mikrokontroller AT89S52

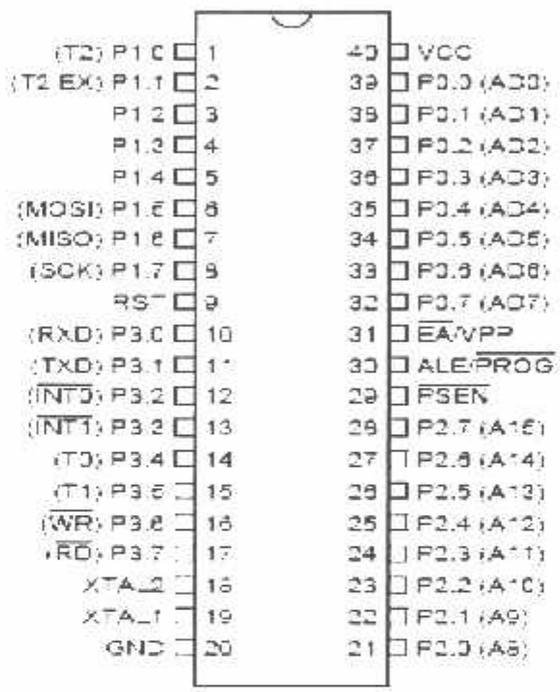
Pada tugas akhir ini digunakan IC pengendali mikro AT89S52 keluaran Atmel merupakan sebuah mikro komputer 8 bit berbasis CMOS. IC ini masih merupakan keluarga MCS-51. IC ini memiliki 8 Kbyte *Flash* PEROM (*Programmabel and Erasable Read Only Memory*). Adapun spesifikasi teknis yang di miliki oleh Pengendalian mikro AT89S52 adalah :

1. 8 Kbytes *Reprogrammable ROM*
2. Dapat di program sebanyak 1000 kali
3. Memiliki 256 x 8 internal RAM
4. 32 *Programmable I/O Lines*
5. 3 buah 16 bit *Timer/Counters*
6. 8 buah sumber *interrupt*

Susunan pin-pin dari AT89S52 diperlihatkan pada Gambar 2.1 sedangkan penjelasan dari masing-masing pin tersebut adalah sebagai berikut :

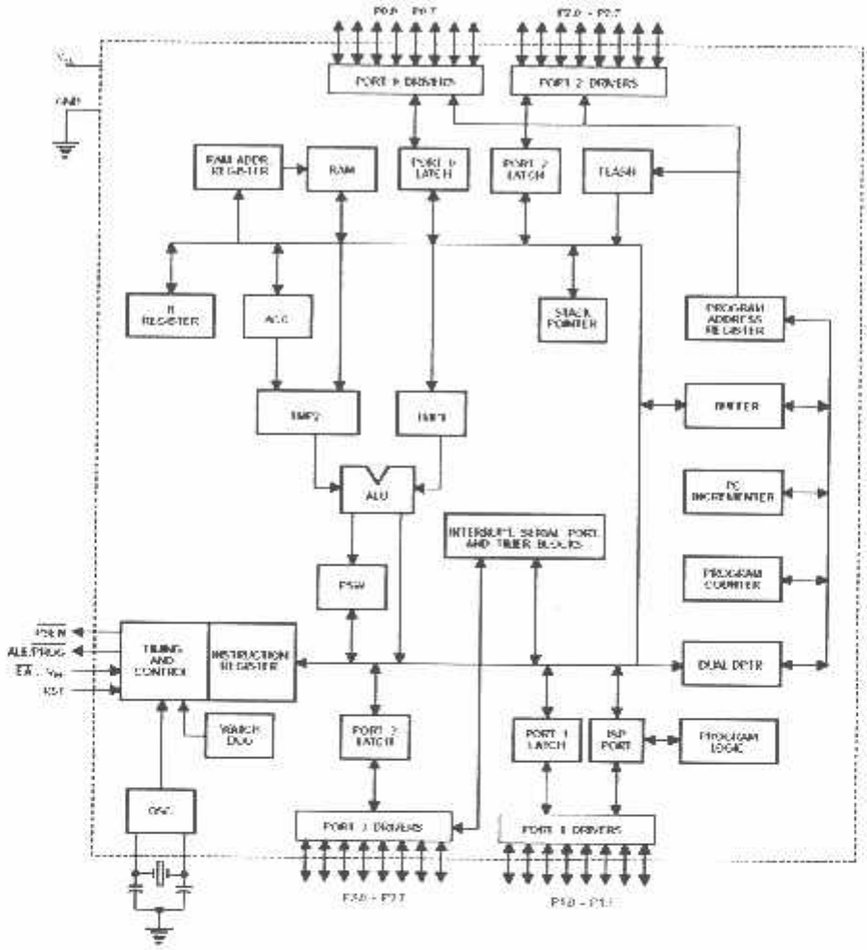
1. Pin 1 sampai 8 (*Port* 1) merupakan port paralel 8 bit dua arah (*bidirectional*) yang dapat digunakan untuk berbagai keperluan (*general purpose*).
2. Pin 9 (*Reset*) adalah masukan reset (aktif *Hi*). Pulsa dari transisi rendah ke tinggi akan me-*reset* AT89S52.
3. Pin 10 sampai 17 (*Port* 3) adalah *port* paralel 8 bit dua arah yang memiliki fungsi pengganti. Fungsi pengganti meliputi TxD (*Transmit Data*), RxD (*Receive Data*), *INT*0 (*Interrupt* 0), *INT*1 (*Interrupt* 1), T0 (*Timer* 0), T1 (*Timer* 1), *WR* (*Write*), *RD* (*Read*). Bila fungsi penggati tidak di pakai, pin-pin ini dapat digunakan sebagai *port* paralel serbaguna.
4. Pin 18 (XTAL 1) adalah pin masukan ke rangkaian osilator internal. Sebuah osilator kristal atau sumber osilator luar dapat digunakan.
5. Pin 19 (XTAL 2) adalah pin keluaran ke rangkaian osilator internal. Pin ini dipakai bila menggunakan osilator kristal.
6. Pin 20 (*Ground*) dihubungkan ke *ground*.
7. Pin 21 sampai 28 (*Port* 2) adalah *port* parelel 8 bit dua arah (*bidirectional*). *Port* 2 ini mengirim *byte* alamat bila di lakukan pengaksesan memori eksternal.
8. Pin 29 adalah *PSEN* (*Program Store Enable*) yang merupakan masukan sinyal pengontrol yang mengizinkan program memori eksternal masukan ke dalam bus selama proses pemberian/pengambilan instruksi.
9. Pin 30 adalah ALE (*Addres Latch Enable*) yang digunakan untuk menahan alamat memori eksternal selama pelaksanaan instruksi.

10. Pin 31 (*EA*). Bila pin ini diberi logika tinggi maka AT89S52 akan melaksanakan instruksi dari PEROM internal. Bila diberi logika rendah AT89S52 akan melaksanakan seluruh instruksi dari memori program luar.
11. Pin 32 sampai 39 (*Port* 0) merupakan port parelel 8 bit *open drain* dua arah. Bila digunakan untuk mengakses memori luar, *port* ini akan memultipleks alamat dengan data.



Gambar 2.1. Konfigurasi Pin AT89S52
Sumber: Data Sheet IC AT89S52

Sedangkan untuk blok diagram AT89S52 diperlihatkan dalam Gambar 2.2



Gambar 2.2. Blok Diagram AT89S52
Sumber: Data Sheet IC AT89S52

2.1.1. Organisasi Memori Mikrokontroler AT89S52

Organisasi memori mikrokontroler AT89S52 dapat dibagi menjadi 2 bagian yang berbeda, yaitu memori program dan memori data. Pembagian itu berdasarkan fungsinya dalam penyimpanan data atau program. Memori program digunakan untuk instruksi yang akan dijalankan oleh mikrokontroler. Sedangkan memori data digunakan sebagai tempat penyimpanan data-data yang akan diakses oleh mikrokontroler.

Mikrokontroler AT89S52 memiliki program internal dan dapat menggunakan memori program *eksternal*. Memori program *eksternal* bisa berupa ROM/EPROM. Memori program internal sebesar 8 Kbyte EEPROM. Lebar jalur alamat yang dapat diakses adalah 16 bit mulai alamat 0000H sampai dengan FFFFH.

Byte Address	Alamat Bit Bit Address							
7F 30	GENERAL PURPOSE RAM (RAM UNTUK SEGALA KEPERLUAN)							
2F	7F	7E	7D	7C	7B	7A	79	78
2E	77	76	75	74	73	72	71	70
2D	6F	6E	6D	6C	6B	6A	69	68
2C	67	66	65	64	63	62	61	60
2B	5F	5E	5D	5C	5B	5A	59	58
2A	57	56	55	54	53	52	51	50
29	4F	4E	4D	4C	4B	4A	49	48
28	47	46	45	44	43	42	41	40
27	3F	3E	3D	3C	3B	3A	39	38
26	37	36	35	34	33	32	31	30
25	2F	2E	2D	2C	2B	2A	29	28
24	27	26	25	24	23	22	21	20
23	1F	1E	1D	1C	1B	1A	19	18
22	17	16	15	14	13	12	11	10
21	0F	0E	0D	0C	0B	0A	9	8
20	7	6	5	4	3	2	1	0
1F 18	REGISTER BANK 3							
17 10	REGISTER BANK 2							
0F 8	REGISTER BANK 1							
7 0	Default Register Bank Untuk R0-R7							

Gambar 2.3. RAM MCS-51
Sumber: Pelatihan Mikrokontroller MCS-51, Tim HALINL

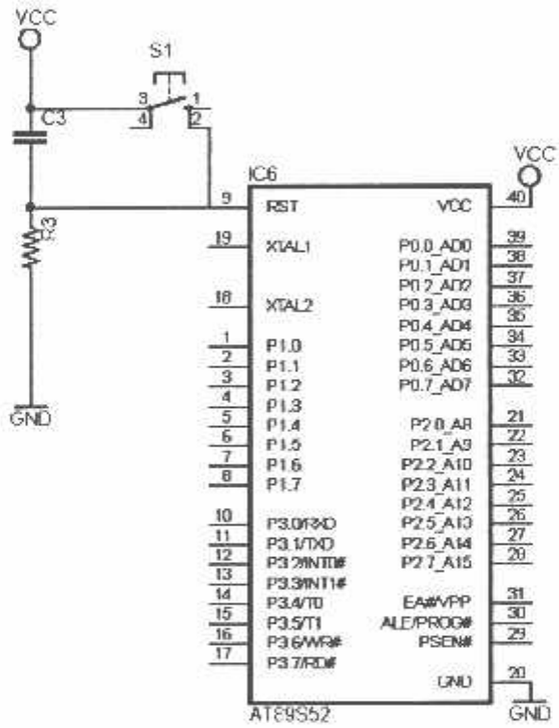
Mikrokontroller AT89S52 memiliki memori data berupa RAM internal sebesar 256 byte. Dari jumlah tersebut, 32 byte terendah dikelompokkan menjadi 4 bank. Tiap-tiap bank terdiri dari 8 register. Pemilihan bank dilakukan melalui register.

Byte Address	Alamat Bit Bit Address								
FF									
F0	F7	F6	F5	F4	F3	F2	F1	F0	B
E0	E7	E6	E5	E4	E3	E2	E1	E0	Acc
D0	D7	D6	D5	D4	D3	D2	-	D0	PSW
B8	-	-	-	BC	BB	BA	B9	B8	IP
B0	B7	B6	B5	B4	B3	B2	B1	B0	P3
A8	AF	-	-	AC	AB	AA	A9	A8	IE
A0	A7	A6	A5	A4	A3	A2	A1	A0	P2
99	not bit adderssable								SBUF
98	9F	9E	9D	9C	9B	9A	99	98	SCON
90	97	96	95	94	93	92	91	90	P1
8D	not bit adderssable								TH1
8C	not bit adderssable								TH0
8B	not bit adderssable								TL1
8A	not bit adderssable								TL0
89	not bit adderssable								TMOD
88	8F	8E	8D	8C	8B	8A	89	88	TCON
87	not bit adderssable								PCON
83	not bit adderssable								DPH
82	not bit adderssable								DPL
81	not bit adderssable								SP
80	87	86	85	84	83	82	81	80	P0

Gambar 2.4. Spesial Function Register
Sumber: Pelatihan Mikrokontroller MCS-51, Tim HALINE

2.1.2. Reset

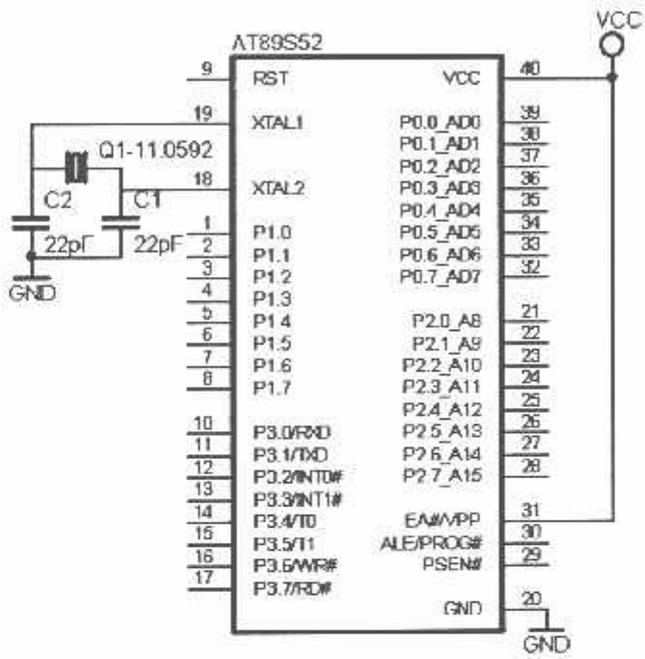
Rangkaian *Power On Reset* diperlukan untuk mereset mikrokontroler secara otomatis setiap catu daya dinyalakan. ketika catu daya diaktifkan, rangkaian reset akan menahan logika tinggi pada penyemat RST dengan jangka waktu yang ditentukan oleh lamanya pengosongan muatan kapasitor. Untuk keabsahan reset, logika tinggi harus bertahan lebih lama dari dua siklus mesin ditambah waktu hidup *(start on)* oscilator. Gambar 2.5 menunjukkan rangkaian *Power On Reset.*



Gambar 2.5. Rangkaian Power On Reset
Sumber: Data Sheet IC AT89S52

2.1.3. Pewaktuan

Mikrokontroler AT89S52 memiliki rangkaian oscilator internal dengan mengacu referensi frekuensi pada penyemat XTAL1 dan XTAL2. Referensi frekuensi berupa kristal dan kapasitor ditunjukkan pada Gambar 2.6



Gambar 2.6. Rangkaian Pewaktuan dengan Osilator Internal
Sumber: Data Sheet IC AT89S52

2.2. Handphone Siemens C35

Siemens merupakan salah satu merek telepon seluler yang dapat berkomunikasi dengan perangkat lain melalui suatu interface tertentu, sehingga suatu pengiriman data dapat terjadi antara perangkat lain dan Handphone Siemens tersebut. Melalui pengiriman data ini pengguna Handphone Siemens dapat mengirim atau menerima suatu pesan singkal *(SMS)*. Untuk dapat berkomunikasi dengan perangkat lain, Handphone Siemens dilengkapi dengan saluran komunikasi khusus yang berupa kabel data. Kabel data merupakan saluran komunikasi pada Handphone Siemens yang dipakai sebagai saluran komunikasi data serial asinkron antara Handphone Siemens dan perangkat lain.

2.2.1. Protokol Komunikasi Data Serial Pada Handphone Siemens C35

Kabel data merupakan saluran komunikasi data serial asinkron pada Siemens yang memakai dua jalur komunikasi. yaitu Rx dan Tx, dengan komunikasi serial 19200 bps 8NI (19,2 kbaud, 8 bit, no parity, 1 stopbit)

2.2.2. Format Data SMS Pada Handphone Siemens C35

Data yang mengalir ke atau dari *SMS-Centre* harus berbentuk *PDU (Protokol Data Unit). PDU* berisi bilangan-bilangan heksadesimal yang mencerminkan bahasa *IO. PDU* terdiri atas beberapa *header. Header* untuk kirim *SMS ke SMS-Centre* berbeda dengan *SMS* yang diterima dari *SMS-Centre.*

Tabel 2.1. Beberapa Nomor *SMS-Centre National Code*

No.	Operator Seluler	SMS-Centre No	Kode PDU
1.	Telkomsel	081100000	068180110000FO
2.	Satelindo	0816124	0581806121 F4
3.	Excelcom	0818445009	06818081440590
4.	Indsat-M3	0855000000	06818055000000

Sumber : Bustam, Aplikasi Berbasis SMS

Tabel 2.2. Beberapa Nomor *SMS-Centre International Code*

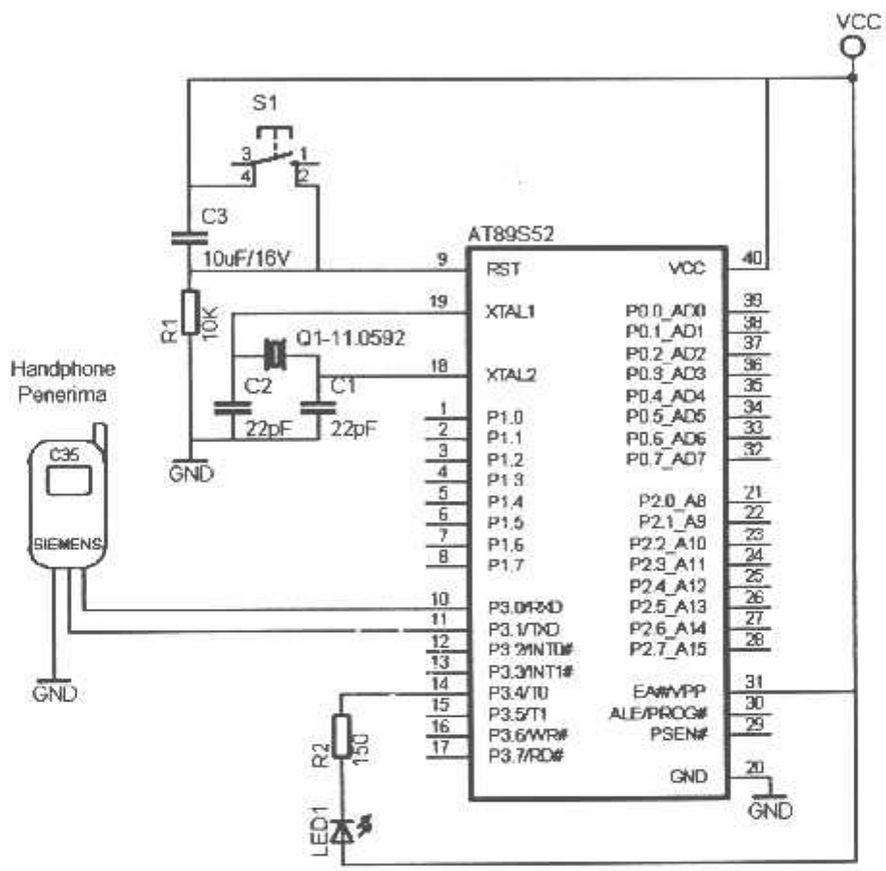
No.	Operator Seluler	SMS-Centre No	Kode PDU
1.	Telkomsel	6281100000	07912618010000F0
2.	Satelindo	62816124	059126181642
3.	Excelcom	62818445009	07912618485400F9
4.	Indsat-M3	62855000000	07912658050000F0

Sumber : Bustam, Aplikasi Berbasis SMS

2.2.3. Interface Handphone Siemens C35 dengan Mikrokontroller

Mikrokontroller AT89S52 dilengkapi dengan port serial. Port serial memungkinkan untuk interface dengan hardware lain dalam format serial. Komunikasi serial antara Mikrokontroller AT89S52 dengan Handphone hanya tinggal menghubungkan pin-pin serial dari masing-masing hardware. Pin *Tx* dari Mikrokontroller akan dihubungkan dengan pin *Rx* yang ada di Handphone. Sedangkan pin *Rx* yang ada di Mikrokontroller dihubungkan pin *Tx* yang ada di

Handphone. Pin ground dari Mikrokontroller dihubungkan dengan pin ground dari Handphone. Gambar 2.7. menunjukan hubungan serial antara Handphone dengan Mikrokontroller.



Gambar 2.7. Hubungan Antara Pengendali Mikro Dengan Handphone

Gambar 2.8. Susunan Pin Pada Handphone Siemens C35
Sumber: Komunitas Siemens Indonesia ; www.siemensxp.com

Tabel 2.3. Data Pin Pada Handphone Siemens C35

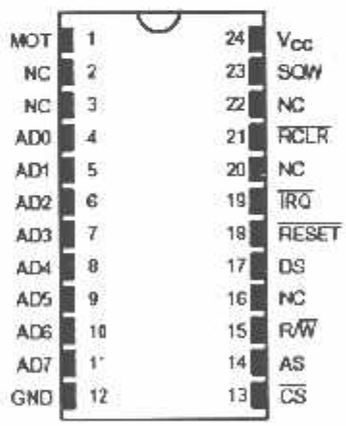
Pin	Name	Dir	Description
1	GND	-	Ground
2	SELF-SERVICE	in/out	Recognition/control battery charger
3	LOAD	in	Charging voltage
4	BATTERY	out	Battery
5	DATA OUT(TX)	out	Data sent
6	DATA IN (RX)	in	Data received
7	Z_CLK	-	Clock line for accessory bus. Use as DCD In data operation
8	Z_DATA	-	Data line for accessory bus. Use as CTS in data operation
9	MICG	-	Ground for microphone
10	MIC	in	Microphone input
11	AUD	out	Loudspeaker
12	AUDG	-	Ground for external speaker

Sumber: Komunitas Siemens Indonesia ; www.siemensxp.com

2.3. RTC (Real Time Clock)

Pencatatan waktu merupakan tugas yang senantiasa harus dikerjakan, meskipun *power-supply* pada suatu peralatan terhenti atau *processor* sedang sibuk mengerjakan tugas lain. Pada tugas akhir ini digunakan IC *real time clock* buatan Dallas Semiconductor yaitu DS12C887. IC ini dibuat lebih tebal dari pada IC-IC lainnya dengan tujuan agar dapat menampung baterai litium. IC ini dapat melakukan pencatatan detik, menit, jam, hari, bulan, tahun bahkan abad. Spesifikasi yang dimiliki IC ini adalah :

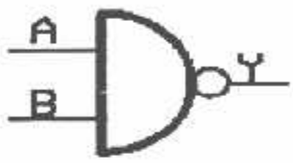
1. Memiliki baterai litium.
2. Dapat menampilkan waktu secara biner, maupun dalam bentuk BCD.
3. Memiliki RAM sebanyak 128 byte :
   - 15 byte untuk *clock* dan kontrol register
   - 113 byte untuk RAM yang dapat digunakan untuk hal-hal yang lain.
4. Data yang di catat tidak akan hilang selama waktu 10 tahun dengan ketidak beradaan *power-supply*.



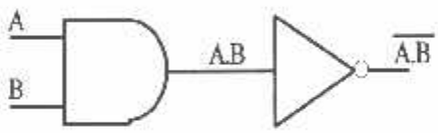
Gambar 2.9. Susunan Pin DS12C887 (RTC)
Sumber: Data Sheet RTC DS12C887

2.4. Gerbang NAND

Gerbang AND, OR dan NOT merupkan tiga rangkaian dasar yang dapat menghasilkan semua rangkaian digital. Gerbang NAND ialah suatu NOT AND, atau suatu fungsi AND yang dibalik. Simbol logika standar untuk gerbang NAND digambarkan pada gambar 2.10. Gelembung Pembalik Kecil (lingkaran kecil) pada ujung kanan dari simbol berarti sebagai pembalik AND.



(a)



(b)

Gambar 2.10. *(a)* Simbol Logika Gerbang NAND
(b) Ekspresi Boolean Keluaran NAND
Sumber : Elektronika Digital ; Roger L. Tokheim

Pada gambar diatas memperlihatkan suatu gerbang AND dan pembalik yang terpisah dan digunakan untuk menghasilakan fungsi logika NAND. Kita perhatikan pula ekspresi boolean untuk gerbang AND (A.B) dan NAND ($\overline{A.B}$) yang diperlihatkan pada diagram logika pada gambar 2.10 *(b)*.

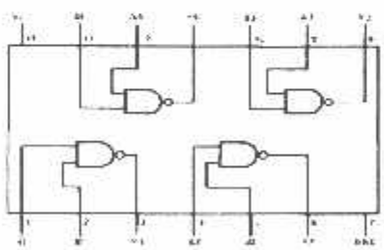
Berikut ini adalah tabel kebenaran untuk gerbang NAND

Tabel 2.4. Tabel kebenaran untuk gerbang AND dan NAND

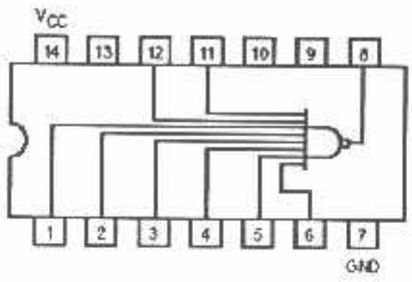
MASUKAN		KELUARAN	
B	A	AND	NAND
0	0	0	1
0	1	0	1
1	0	0	1
1	1	1	0

Sumber : Dasar-dasar Elektronika : Owen Bishop

Perhatikan bahwa tabel kebenaran untuk gerbang NAND dibuat untuk membalikan keluaran gerbang AND. Keluaran gerbang AND juga diberikan pada tabel sebagai acuan. Gerbang NAND keluaran RENDAH bila semua masukan TINGGI. Kolom keluaran pada table 2.4 memperlihatkan bahwa hanya baris 4 dalam tabel kebenaran NAND menghasilkan suatu keluaran 0 sedang semua baris lain menghasilkan keluaran 1.



(a)

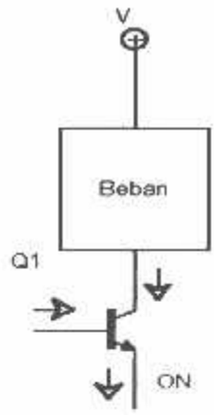


(b)

Gambar 2.11. IC Gerbang NAND *(a)*. 2-Input NAND GATE 74LS00
(b). 8-Input NAND GATE 74LS30
Sumber : Data Sheet IC NAND GATE

2.5. Dioda Pelindung

Dioda pelindung sangat penting untuk digunakan ketika kita mensaklarkan arus listrik ke beban-beban yang memiliki induktansi tinggi. Beban-beban induktif antara lain adalah kumparan relay, bell listrik dan magnet-magnet listrik. Ketika transistor (BJT atau FET) dalam keadaan aktif, arus mengalir melewati kumparan. Arus dapat sedikit berubah-ubah dan, apabila demikian, medan magnet yang ditimbulkan juga akan sedikit berubah-ubah. Tetapi, tidak terdapat perubahan-perubahan yang dramatis.

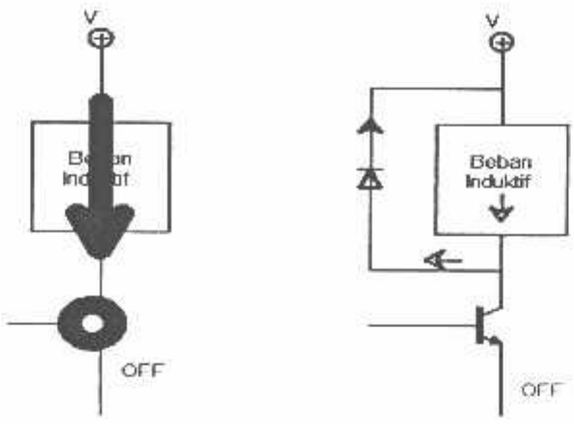


Gambar 2.12. Arus Mengalir Melewati Kumparan
Sumber : Dasar-dasar Elektronika : Owen Bishop

Gambar 2.13 *(a)*. Ketika transistor terputus dari pasokan arus (tidak aktif), arus pada kumparan akan jatuh secara seketika dan medan magnet meluruh dengan sangat cepat pengaruh induksi ditentukan oleh kecepatan perubahan medan magnet. Semakin cepat laju perubahan tersebut, semakin besar pengaruh yang timbul.

Terputusnya arus ke transistor adalah perubahan yang sangat cepat. Sebuaah gaya gerak listrik yang sangat besar di induksikan pada kumparan, untuk mempertahankan agar tidak menghilang. Gaya gerak listrik ini dapat mencapai beberapa ratus volt, bahkan walaupun tegangan awal pada beban hanyalah sebesar, misalnya 10 v. Arus sebesar bebrapa amper akan " membanjiri " transistor dan menghaguskannya.

Gambar 2.13 *(b)*. solusi untuk permasalahan ini adalah menyambungkan sebuah dioda.. Sebagaimana diperlihatkan dalam gambar, untuk mengalirkan dan membuang arus berlebih ini secara aman.



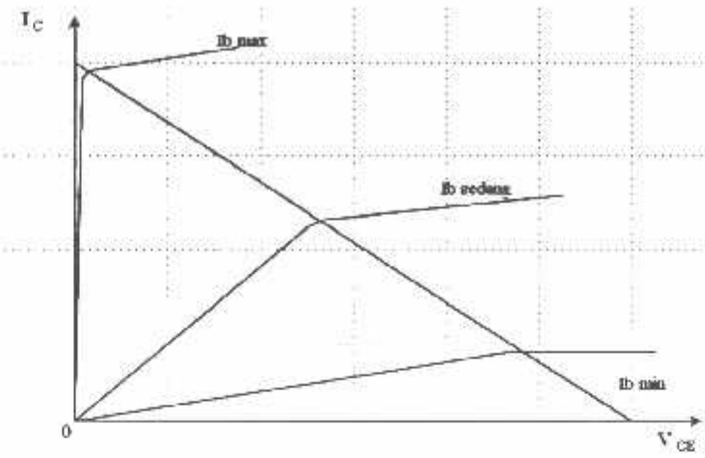
(a) *(b)*

Gambar 2.13. *(a)* Arus Beban Ketika Transistor Tidak Aktif
(b) Dioda Sebagai Pelindung Arus Beban
Sumber : Dasar-dasar Elektronika ; Owen Bishop

2.6. Transistor

Transistor adalah komponen yang paling banyak digunakan sebagi penguat, saklar, dan lain-lain, Transistor akan bekerja / mengalirkan arus antara *colector* ke *emitor* (Ic) jika ada arus yang mengalir pada *basis*nya (Ib). Besar arus *Basis* ini yang mempengaruhi besarnya arus *colector* yang mangalir. Sehingga penguatan didapat dengan mengubah besarnya arus *basis* yang masuk.

Titik kerja transisitor dapat dilihat pada garis karakteristik dari masing masing transistor yang tersusun seperti pada gambar di bawah ini:



Grafik 2.1. Karakteristik kerja transistor *Bipolar*
Sumber : Dasar-dasar Elektronika ; Owen Bishop

Dari gambar grafik di atas dapat diketahui bahwa untuk membuat Ic mengalir akan mengakibatkan perubahan dengan perbandingan terbalik atar V_{CE} dengan I_C. Inilah yang mengakibatkan titik kerja transistor berbeda-beda. Yaitu dengan pemberian I_B yang berbeda sesuai dengan keinginan perancangan. Keadaan dimana I_B maksimum maka akan menghasilkan transistor pada titik jenuh (*saturation*) yaitu arus I_C mengalir dangan maksimum yang seakan-akan *Colector* hubung singkat (*short*) dengan *emitor*, ini digunakan sebagai saklar dalam keadaan on, dan saat dimana I_B minimum atau tidak ada maka V_{CE} sangat tinggi yang mengakibatkan I_C seakan tidak menaglir sehingga terjadi aliran yang terputus antara *colector* dengan *emitor*, keadaan ini disebut *cut off* dan dipakai sebagai saklar dalam keadaan open.

Keadaan dimana arus basis berubah-ubah sesuai dengan frekuensi atau *signal input* akan pula bekerja seperti *cut-off* dan *saturation* yang cepat sesuai dengan *signal* masukan maka akan menjadi rangkaian penguat, rangkaian penguatan memiliki kategori sesuai dengan titik setimbangnya, yaitu saat dimana nilai rata-rata tanpa *signal* masuk ke *basis* (I_B dalam keadaan diam).

Untuk penguat kelas A titik kerja terdapat di tengah yaitu pada I_B sedang, untuk penguat kelas B maka titik kerja pada *cut off* sedang pada penguat kelas C titik kerja ada di bawah *cuf off* (I_B *minus*).

2.6.1. Tipe Transistor

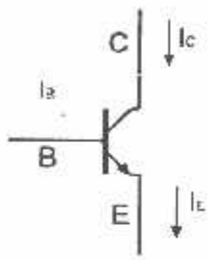
Transistor merupakan salah satu komponen aktif yang mempunyai tiga kaki yang disebut dengan kolektor, basis dan emitter. Pada umumnya untuk memudahkan dalam menentukan kaki-kaki tersebut pada badan transistor diberi tanda tertentu. Berdasarkan pada tipenya, transistor terdiri dari dua macam type yaitu type NPN dan PNP.

(a)

(b)

Gambar 2.14. *(a)* Penggabungan Semikonduktor NPN dan PNP
(b) Simbol Transistor Type NPN dan PNP
Sumber: Prinsip-prinsip Elektronika jilid 1, Malvino.

2.6.2. Arus Transistor



Gambar 2.15. Tiga Arus Transistor
Sumber: Prinsip-prinsip Elektronika jilid I. Malvino

Pada gambar 2.15 menunjukkan arah arus transistor NPN, dimana terdapat tiga arus yang berbeda pada sebuah transistor : arus emitor I_E , arus basis I_B dan arus kolektor I_C. Ingatlah hukum arus Kirchhoff. Hukum itu mengatakan bahwa jumlah semua arus yang masuk ke suatu titik atau sambungan sama dengan jumlah semua arus yang keluar dari titik atau sambungan itu. Jika diterapkan pada transistor, maka didapat persamaan :

$$I_E = I_C + I_B \qquad (a)$$

Persamaan *(a)* tersebut mengatakan bahwa arus emitor adalah jumlah dari arus kolektor dan arus basis. Karena arus basis sangat kecil, arus kolektor kira-kira sama dengan arus emitor :

$$I_C \approx I_E \qquad (b)$$

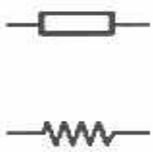
Dan besar arus basis jauh lebih kecil daripada arus kolektor :

$$I_B << I_C \qquad (c)$$

2.7. Resistor

Di dalam kebanyakan rangkaian listrik, kita menyambung nyambungkan berbagai komponen rangkaian dengan menggunakan kawat-kawat tembaga. Hal ini disebabkan karena tembaga adalah sebuah bahan konduktor listrik yang sangat baik. Tembaga memiliki tahanan listrik yang sangat rendah. Akan tetapi, sejumlah sambungan pada rangkaian membutuhkan tahanan listrik yang lebih besar daripada yang dapat diberikan oleh kawat tembaga. Inilah alasan mengapa kita menggunakan resistor.

Gambar 2.16 memperlihatkan dua simbol yang berbeda, yang digunakan untuk merepresentasikan resistor-resistor di dalam sebuah diagram rangkaian listrik

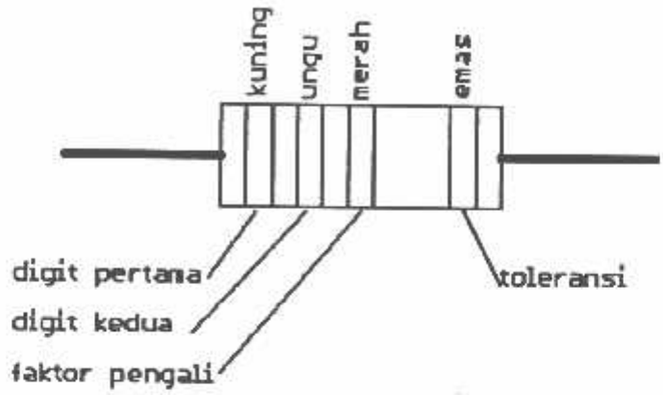


Gambar 2.16. Simbol Resistor Yang Berbeda
Sumber : Dasar-dasar Elektronika ; Owen Bishop

2.7.1. Kode Warna Resistor

Tiga buah cincin berwarna dipergunakan untuk mengindikasikan nilai tahanan sebuah resistor tetap. Cincin-cincin ini ditempatkan saling berdekatan

di salah satu ujung badan resisitor. Warna tiap-tiap cincin merepresentasikan sebuah bilangan.



Gambar 2.17. Kode Warna Pada Badan Resistor
Sumber : Dasar-dasar Elektronika ; Owen Bishop

Membaca kode warna ini dari ujung resistor terdekat, kita dapat mengetahui bahwa warna-warna tersebut memiliki arti:

Cincin prtama	Digit pertama dari nilai tahanan
Cincin kedua	Digit kedua dari nilai tahanan
Cincin ketiga	Faktor pengali – sebuah nilai pemangkatan bilangan 10, atau banyaknya angka nol di belakang kedua digit pertama.

Tabel dibawah memperlihatkan arti dari warna-warna pada badan resisitor

Tabel 2.5. Nilai Dari Warna-Warna Pada Badan Resistor

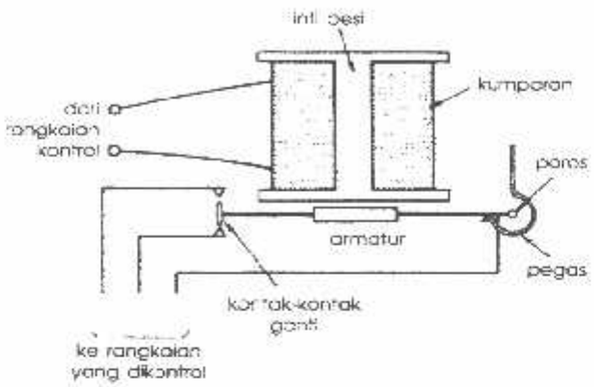
Warna	Bilangan
Hitam	0
Coklat	1
Merah	2
Jingga	3
Kuning	4
Hijau	5
Biru	6
Ungu	7
Abu-abu	8
Putih	9

Sumber : Dasar-dasar Elektronika ; Owen Bishop

2.8. Relay

relay adalah sebuah saklar yang dikendalikan oleh arus. Relay memiliki sebuah kumparan tegangan-rendah yang dililitkan pada sebuah inti. Terdapat sebuah armatur besi yang akan tertarik menuju inti apabila arus mengalir melewati kumparan. Armatur ini terpasang pada sebuah tuas berpagas. Ketika armatur tertarik

menuju ini, kontak jalur bersama akan berubah posisinya dari kontak normal tertutup ke kontak normal terbuka.



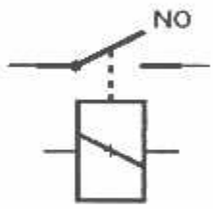
Gambar 2.18. *Bagian Dalam Sebuah Relay*
Sumber : Dasar-dasar Elektronika : Owen Bishop

Sebuah relay yang tipikal dari jenis ini dapat diaktifkan dalam waktu sekitar 10 ms. Sebagian besar relay modern ditempatkan di dalam sebuah kemasan yang sepenuhnya tertutup rapat. Kebanyakan diantaranya memiliki kontak-kontak jenis SPDT, namun terdapat juga beberapa versi DPDT. Relay-relay yang berukuran besar dapat menyambungkan arus hingga 10 A pada tegangan 250 V AC. Tegangan maksimum untuk pensaklaran DC selalu jauh lebih rendah, seringkali bahkan hanya setengah, dari tegangan maksimum untuk AC. Gambar di bawah memperlihatkan simbol-simbol yang digunakan di dalam diagram-diagram rangkaian untuk merepresentasikan kumparan relay (kiri) dan kontak-kontak ganti (kanan). NC mengindikasikan kontak normal-tertutup.

Gambar 2.19. *Simbol Relay*
Sumber : Dasar-dasar Elektronika : Owen Bishop

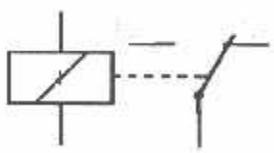
Dalam memutuskan atau menghubungkan kontak digerakkan oleh fluksi yang ditimbulkan dari adanya medan magnet listrik yang dihasilkan oleh kumparan yang melilit pada besi lunak. Ada beberapa macam relay, antara lain :

1. **SPST (Single Pin Single Terminal)**
   Simbol *Relay SPST*



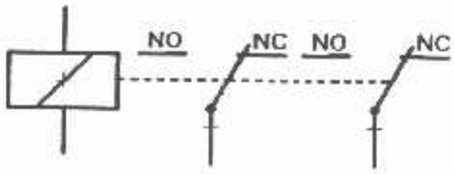
Gambar 2.20. Relay SPST
Sumber:Sistem Relay. www.stts.ac.id

2. **SPDT (Single Pin Dual Terminal)**
   Simbol *Relay SPDT*



Gambar 2.21. Relay SPDT
Sumber:Sistem Relay. www.stts.ac.id

3. **DPDT (Dual Pin Dual Terminal)**
Simbol *Relay DPDT*



Gambar 2.22. Relay DPDT
Sumber:Sistem Relay, www.stts.ac.id

Relay berdasarkan arusnya di golongkan menjadi dua :

- Relay arus searah (DC Relay)
- Relay arus bolak- balik (AC Relay)

Sebuah penahan dipasang pada inti belitan kumparan, jika ada arus yang mengalir, inti akan menjadi magnet dan jangkar tertarik. Pada jangkar terpasang pegas spiral sehingga jangkar akan kembali jika arus diputuskan. Jadi pada dasarnya relay punya dua kontak, normal terbuka (*Normally Open*) dan normal tertutup (*Normally Close*). Dalam praktek kontak-kontak relay tidak hanya dua atau empat, tetapi sampai 24 kontak yang merupakan kombinasi dari kontak NO dan NC.

2.9. Saklar Tekan

Saklar tekan dioperasikan dengan cara menekan sebuah tombol. Terdapat dua jenis saklar semacam ini. Kebanyakan diantaranya termasuk ke dalam jenis ***push-to-make*** **(tekan-untuk-meyambungkan)** atau **(*PTM*)**. Dengan menekan tombol, kontak-kontak akan tertekan hingga saling bersentuhan dan saklar menutup. Jenis

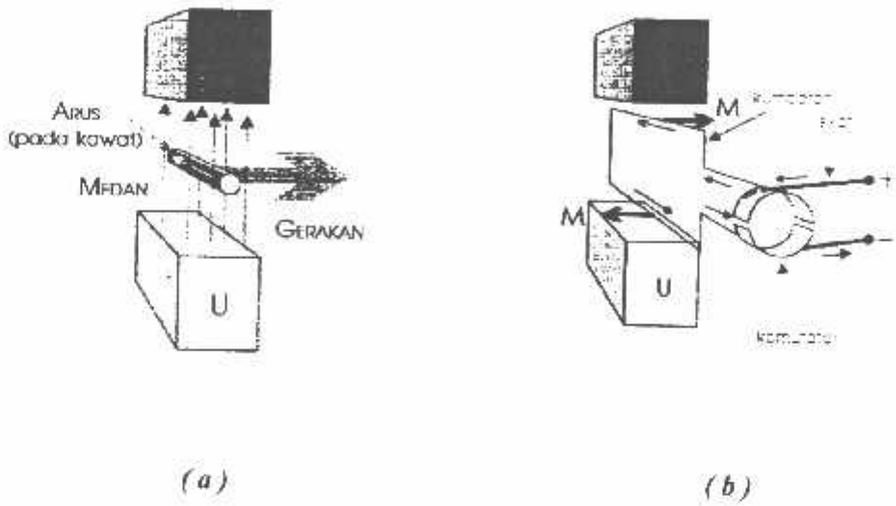
lainnya adalah ***push-to-break*** **(tekan-untuk-memutuskan)** atau ***(PTB)***. Kontak-kontaknya adalah kontak-kontak normal tertutup, namun akan dipaksa membukaketika tombol ditekan.

Masing –masing jenis saklar yang disebutkan diatas dapat bekerja untuk membentuk (atau memutuskan) sambungan selama sekejap atau **menguncinya** ***(laching)*** sebuah saklar yang membentuk (atau memutuskan) sambungan selama **sekejap** hanya akan menutup (atau membuka) selama tombol masih ditekan. Ketika tombol dilepaskan saklar akan kembali keposisi semula. Pada saklar yang **mengunci** ***(latching)*** pnyambungan atau pemutusan daya, tombol akan tetap berada pada posisi tertekan setelah pertama kali ditekan. Kontak-kontak saklar akan tetap menutup atau membuka bergantung pada jenis saklar yang bersangkutan. Anda harus menekan tombol itu sekali lagi untuk membukakunci dan mengembalikan tombol keposisi normalnya.

Gambar 2.23. Simbol dari Saklar Push Button Switch
Sumber : Dasar-dasar Elektronika ; Owen Bishop

2.10. Motor Listrik

Ketika sepotong kawat dialiri oleh arus, dan kawat tersebut berada di dalam sebuah medan magnet, sebuah gaya akan bekcja dan menggerakan kawat.



(a) *(b)*

Gambar 2.24. *(a)* Arah Arus dan Arah Medan Magnet
(b) Cara Kerja Motor DC Sederhana
Sumber : Dasar-dasar Elektronika ; Owen Bishop

Arah gerakan ini dapat ditentukan dengan menggunakan tangan kiri sehingga ibu jari, jari telunjuk dan jari tengah berada pada posisi tegak lurus antara satu sama lainnya. Selanjutnya:

- Tunjuklah dengan jari telunjuk (First finger) kearah yang sama dengan arah medan (Field) (yaitu dari Utara ke Selatan).
- Tunjuklah dengan jari tengah (seCond finger) kearah yang sama dengan arah arus (Current).

- Ibu jari (thuMb) saat ini menunjuk ke arah gerakan (Motion).

Ingatlah ketiga arah ini – F, C, dan M! Aturan ini dikenal sebagai **Aturan Tangan-Kiri Fleming.**

2.10.1. Bagaimana Sebuah Motor DC Sederhana Bekerja

gambar 2.24. *(b)* menggambarkan sebuah motor DC sederhana. Terdapat sebuah magnet permanen yang berfungsi sebagai sumber medan magnet. Sebuah kumparan yang dipasangkan pada sebuah poros akan berputar pada kutub-kutub magnet. Kumparan ini diperlihatkan hanya memiliki satu lilitan. Pada motor yang sebenarnya, kumparan dapat memiliki beberapa ratus lilitan. Ujung kumparan disambungkan ke sebuah komutator, yang terdiri dari sepasang lempengan logam berbentuk setengah cincin. Terdapat dua buah sikat lentur yang membentuk kontak-kontak listrik dengan kedua lempengan setengah cincin.

Ketika tegangan DC diberikan keterminal-terminal rangkaian motor, arus mengalir melewati sikat bagian atas ke komutator, melewati kumparan menuju ke lempeng setengah cincin komutator lainnya dan akhirnya kembali ke sikat bagian bawah. Arus mengalir menjauhi komutator pada bagian atas kumparan. Medan magnet dan arus memiliki arah sebagaimana terlihat pada gambar 2.24. *(a)*. Menunjuk ke Aturan Tangan-Kiri Fleming, bagian atas kumparan akan terdorong oleh gaya yang kemudian menggerakannya kearah kanan. Menerapkan aturan yang sama tehadap bagian bawah kumparan, dimana arus mengalir menuju komutator, bagian bawah kumparan terdorong kearah kiri. Kedua gaya ini mengakibatkan kumparan berputar pada arah yang sama dengan jarum jam.


INSTITUT TEKNOLOGI NASIONAL
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BAB III

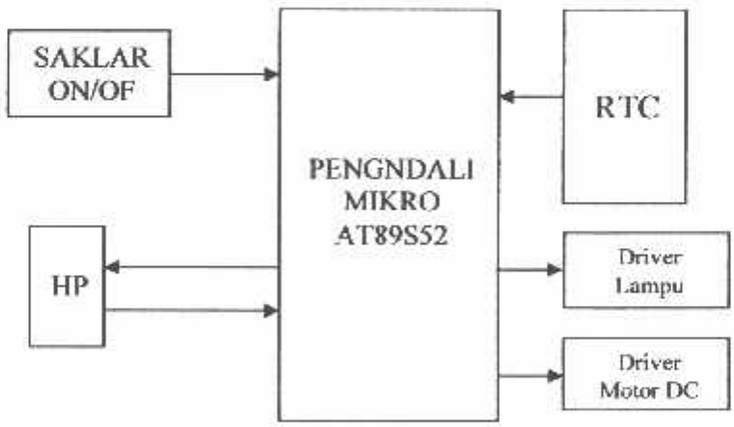
REALISASI RANGKAIAN

Perancangan dan perealisasian alat di dalam tugas akhir ini meliputi dua bagian, yaitu perancangan perangkat keras dan perangkat lunak. Perancangan perangkat keras meliputi:

- Perancangan Rangkaian pengendali mikro.
- Perancangan komunikasi serial dari *handphone* ke alat.
- Perancangan pewaktuan alat dengan menggunakan IC RTC.
- Perancangan tombol saklar *on-off*
- Perancangan keluaran berupa driver untuk lampu dan driver motor DC untuk membuka dan menutup pintu.

Perancangan perangkat lunak mencakup semua program penunjang yang digunakan untuk mengoprasikan pengendali mikro. Perangkat lunak ini akan mengatur keseluruhan kerja alat.

3.1. Perancangan Perangkat Keras



Gambar 3.1. Rangkaian Perancangan Perangkat Keras (Diagram Blok)

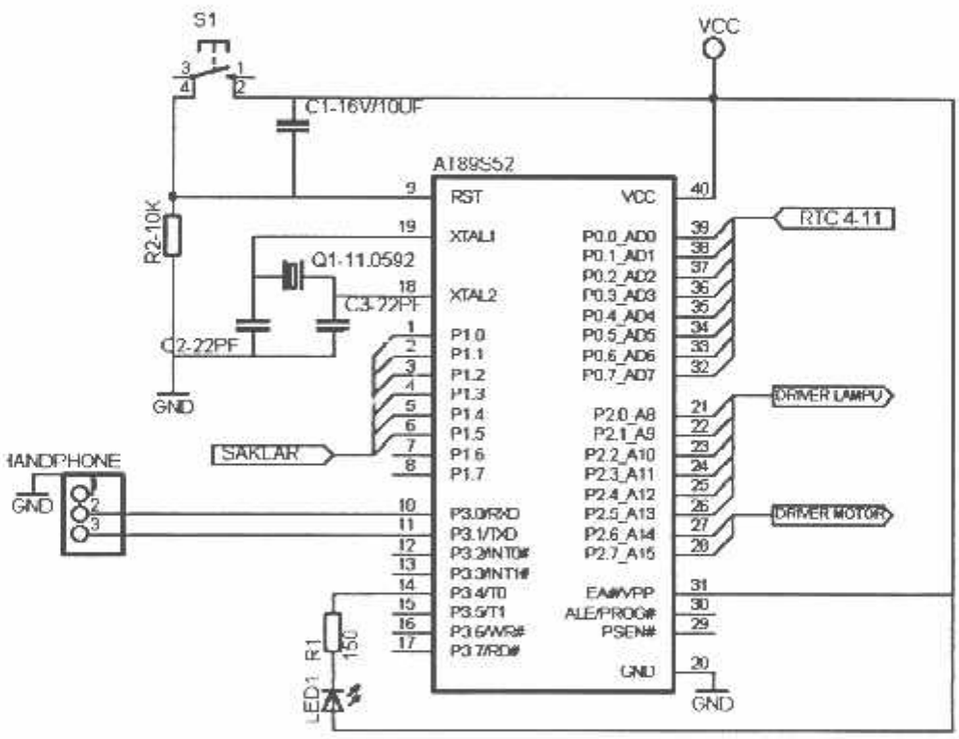
3.1.1. Rangkaian Pengendali Mikro

Pengendali mikro merupakan modul utama di dalam tugas akhir ini. Rangkaian pengendali mikro ini terdiri dari IC pengendali mikro AT89S52, Rangkaian osilator pengendali mikro AT89S52, Rangkaian *reset* pengendali mikro AT89S52.

Rangkaian osilator terdiri dari sebuah kristal dan dua buah kapasitor. Rangkaian ini dihubungkan dengan pin XTAL1 dan XTAL2. Nilai kapasitor yang di pakai sebesar 22 pF dan kristal yang di gunakan mempunyai nilai 11,0592 MHz. Rangkaian *reset* yang di realisasikan memiliki kemampuan *power-on reset*, yang juga disertai dengan tombol *reset*. Rangkaian ini terdiri dari sebuah kapasitor, sebuah resistor dan sebuah *push button*. Nilai kapasitor yang di pakai 10μF, nilai resistor yang di pakai 10 k. *Port* 0 dari pengendali mikro digunakan sebagai jalur komunikasi antara pengendali mikro dengan RTC (DS12C887). Karena *port* 0 ini tidak memiliki *internal pull-up resistor*, maka *port* 0 ini harus di *pull-up* terlebih dahulu dengan menggunakan *resistor array* sebesar 10 k.

1. *Port* 1 dari pengendalian mikro digunakan sebagai masukan data dari penekanan tombol saklar *on-off*.
2. *Port* 2 dari pengendali mikro digunakan sebagai keluaran dari alat. Keluaran ini akan di hubungkan ke rangkaian driver lampu dan rangkaian driver motor untuk membuka pintu.
3. *Port* 3 dari pengendali mikro digunakan untuk bermacam-macam kebutuhan sesuai dengan kegunaan dari *port* 3. penggunaan *port* 3 adalah sebagai berikut:
    - P3.0 (RXD) digunakan sebagai masukan dari komunikasi serial antara *handphone* dengan pengendali mikro.
    - P3.1 (TXD) digunakan sebagai pengirim data serial dari pengendali mikro ke *handphone*.

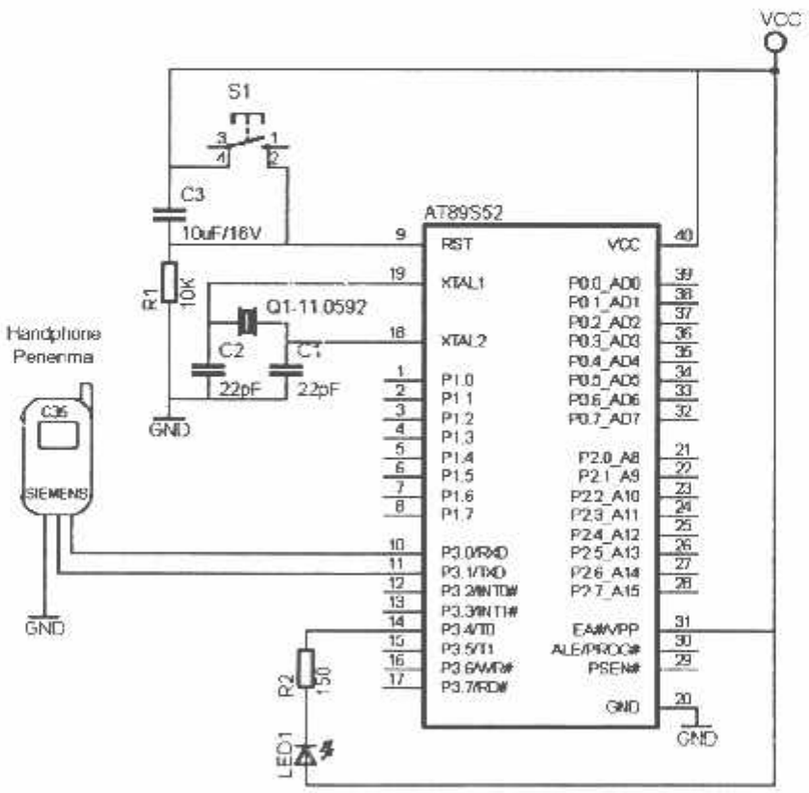
- P3.2 (INT0) digunakan sebagai interupsi eksternal bila terjadi penekanan saklar *on-off*.
- P3.3 (INT1) digunakan sebagai masukan interupsi eksternal dari RTC.
- P3.4 (T0) digunakan sebagai penyala LED bila *handphone* telah terkoneksi ke alat.
- P3.6 (WR) digunakan untuk berkomunikasi dengan RTC.
- P3.7 (R D) digunakan untuk berkomunikasi dengan RTC.



Gambar 3.2. Rangkaian Pengendali Mikro

3.1.2. Komunikasi Serial Handphone Ke Mikrokontroller

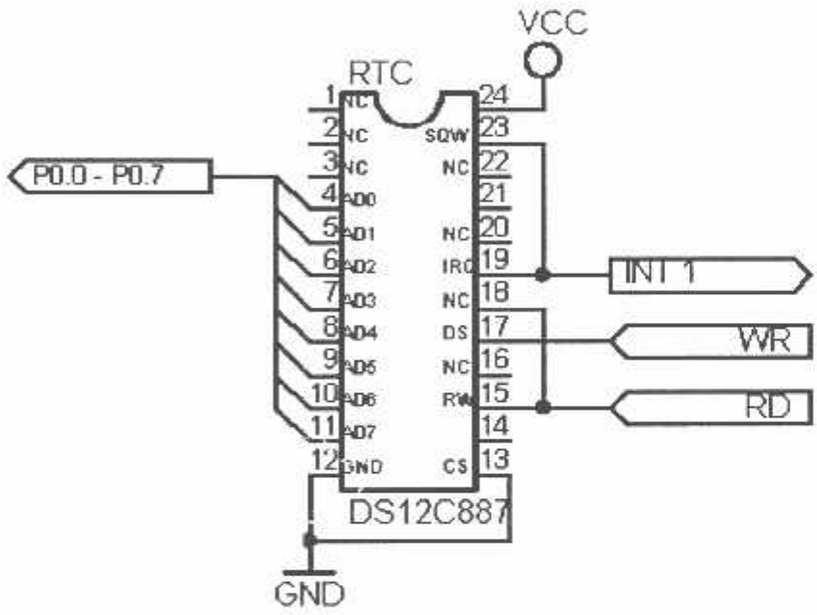
Mikrokontroller AT89S52 dilengkapi dengan port serial. Port serial memungkinkan untuk interface dengan hardware lain dalam format serial. Komunikasi serial antara Mikrokontroller AT89S52 dengan Handphone Siemens C35 hanya tinggal menghubungkan pin-pin serial dari masing-masing hardware. Pin *Tx* dari Mikrokontroller akan dihubungkan dengan pin *Rx* yang ada di Handphone Siemens C35. Sedangkan pin *Rx* yang ada di Mikrokontroller dihubungkan pin *Tx* yang ada di Handphone Siemens C35. Pin ground dari Mikrokontroller dihubungkan dengan pin ground dari Handphone Siemens C35. Gambar 3.3 menunjukan hubungan serial antara Handphone dengan Mikrokontroller.



Gambar 3.3. Hubungan Antara Pengendali Mikro Dengan Hanphone

3.1.3. Rangkaian RTC

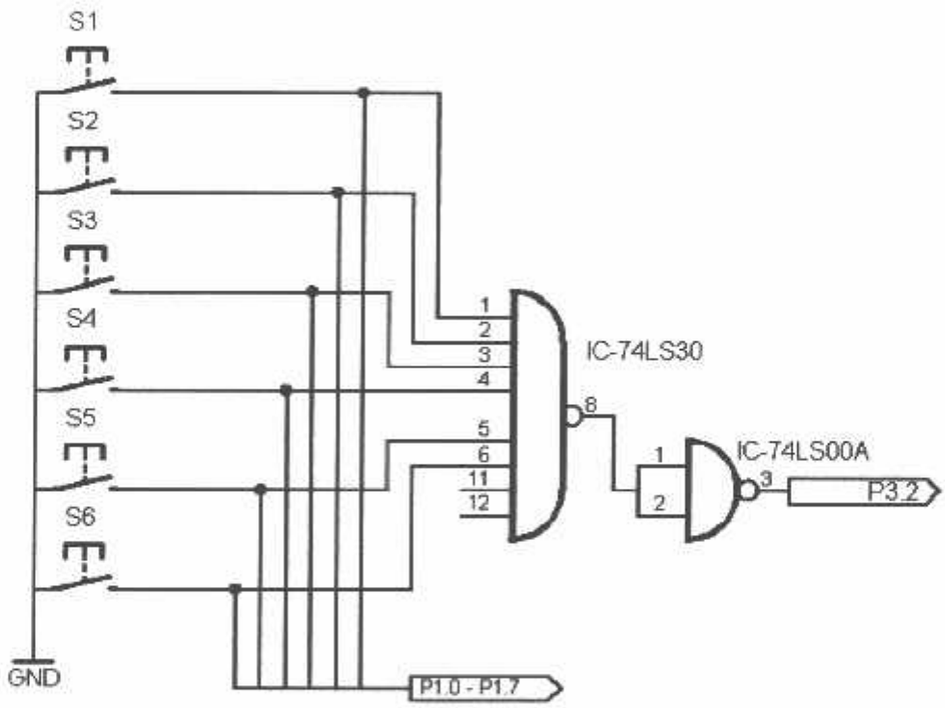
Real Time Clock merupakan suatu IC yang di gunakan sebagai pencatat waktu dari keseluruhan alat. Dalam IC ini sudah dilengkapi dengan baterai sendiri, maka bila terjadi pemutusan *power supply*, data dari waktu yang telah di catat tidak akan hilang, dan IC akan tetap mencatat pertambahan waktu.



Gambar 3.4. Rangkaian Real Time Clock

3.1.4. Rangkaian Saklar On-Off

Saklar *on-off* ini digunakan sebagai pengatur keluaran secara manual. Saklar *on-off* ini dihubungkan ke masukan dari *port* 1. Yang di paralel ke gerbang NAND, yang memiliki masukan sebanyak 8 buah dan memiliki 1 buah keluaran (74LS30). Kemudian keluaran ini dihubungkan ke masukan sebuah inverter (74LS00). Keluaran dari inverter ini disambungkan ke interupsi eksternal 0 pada pengendalian mikro.



Gambar 3.5. Rangkaian Saklar On-Off Manual

3.1.5. Rangkaian Keluaran

Terdapat 8 jalur keluaran dari alat, 6 jalur keluaran dihubungkan ke rangkaian driver lampu dan 2 jalur keluaran dihubungkan ke rangkaian driver motor untuk membuka dan menutup pintu, dimana lampu dan motor ini akan bekerja apabila ada sinyal yang di kirimkan.

3.1.5.1. Rangkaian Driver Lampu

Pada rangkaian ini menggunakan sebuah transistor dengan tipe BD 139 dan sebuah relay 12 Volt. Transistor mempunyai Hfe sebesar 75, hambatan relay sebesar 350 Ohm dan tegangan input (Vin) sebesar 5 volt, maka :

$$\text{I relay} = \frac{Vcc}{Rrelay} = \frac{12V}{350\Omega} = 0{,}034 \text{ Ampere}$$

Setelah diketahui harga dari I relay (Ic) maka dapat kita cari harga Ib sekaligus harga Rb yaitu :

$$\text{Ib} = \frac{Ic}{Hfe} = \frac{0.034A}{75} = 4{,}5 \times 10^{-4} \text{ Ampere}$$

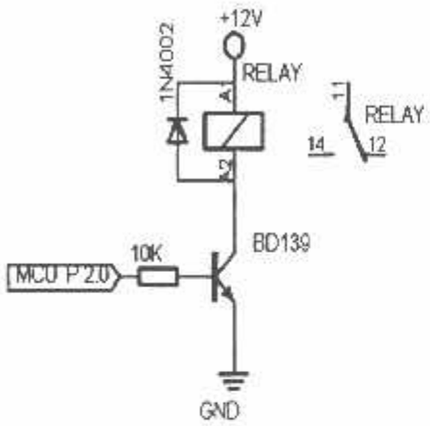
Sedangkan untuk mencari nilai Rb digunakan rumus sebagai berikut :

$$\text{Rb} = \frac{Vin - Vbe}{Ib} = \frac{5V - 0{,}7V}{4{,}5x10^{-4}} = 9555 \text{ Ohm} = 10 \text{ K}$$

Relay yang digunakan mempunyai spesifikasi tegangan dan arus yang bisa dilewati 240 VAC / 10 A untuk mengetahui daya lampu yang bisa dilewatkan oleh relay :

$$P = V \times I = 240 \times 10 = 2400 \text{ Watt}$$

Rangkaian driver relay dapat dilihat pada gambar dibawah ini :

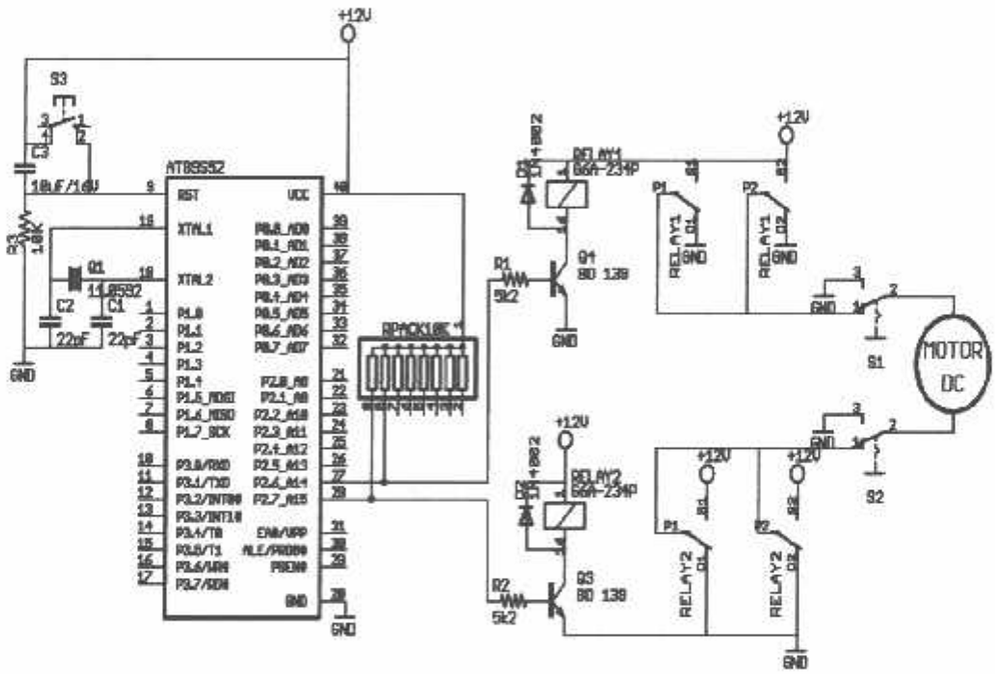


Gambar 3.6. Rangkaian Driver Lampu

Pada penggerak relay dipasang dioda (jenis 1N4002) berfungsi untuk menghubung singkat tegangan induksi yang timbul pada saat transistor sebagai saklar terbuka (off) sehingga tidak terjadi tegangan lebih pada transistor.

3.1.5.2. Rangkaian Driver Motor

Driver ini digunakan untuk menggerakkan motor, sehingga pintu dapat digerakkan membuka dan menutup secara otomatis. Rangkaian driver ini dirancang sesuai program mikrokontroller, dimana terdapat dua output kontrol dari mikrokontroller. Gambar rangkaian driver relay diperlihatkan dalam Gambar 3.6. Pensaklaran supply motor dilakukan oleh relay yang dikendalikan oleh transistor. Transistor-transistor yang digunakan dari jenis BD 139, dengan β sebesar 100. Dari hasil pengukuran diperoleh resistansi belitan relay sebesar R_{relay} = 600 Ω.



Gambar 3.7. Rangkaian Driver Motor DC

Arus kolektor transistor $IC = \frac{V_{CC}}{R_{relay}} - \frac{5}{600} - 83$ mA, kemudian dari rumus $Ib = \frac{Ic}{\beta} = \frac{83}{100} = 0.83\ mA$ diperoleh I_B = 0.83 mA. Vin adalah tegangan logika tinggi dari Mikrokontroller sebesar 5 volt. Dengan memasukkan nilai-nilai yang bersesuaian cari rumus berikut $Rb = \frac{Vbb - Vbe}{Ib} = \frac{5 - 0.7}{0.83} = 5180\ \Omega$ diperoleh R_B = 5180 Ω, disesuaikan dengan nilai resistor di pasaran menjadi 5K2 Ω. Pada kaki-kaki belitan relay yang dialiri arus kolektor dipasang dioda. Bila arus dari kolektor diputus maka arus balik dari belitan relay akan dihubung singkat dan tidak merusak transistor. Digunakan dioda 1N4002 yang mampu melewatkan arus maksimum 1 A.

Spesifikasi motor yang digunakan adalah :

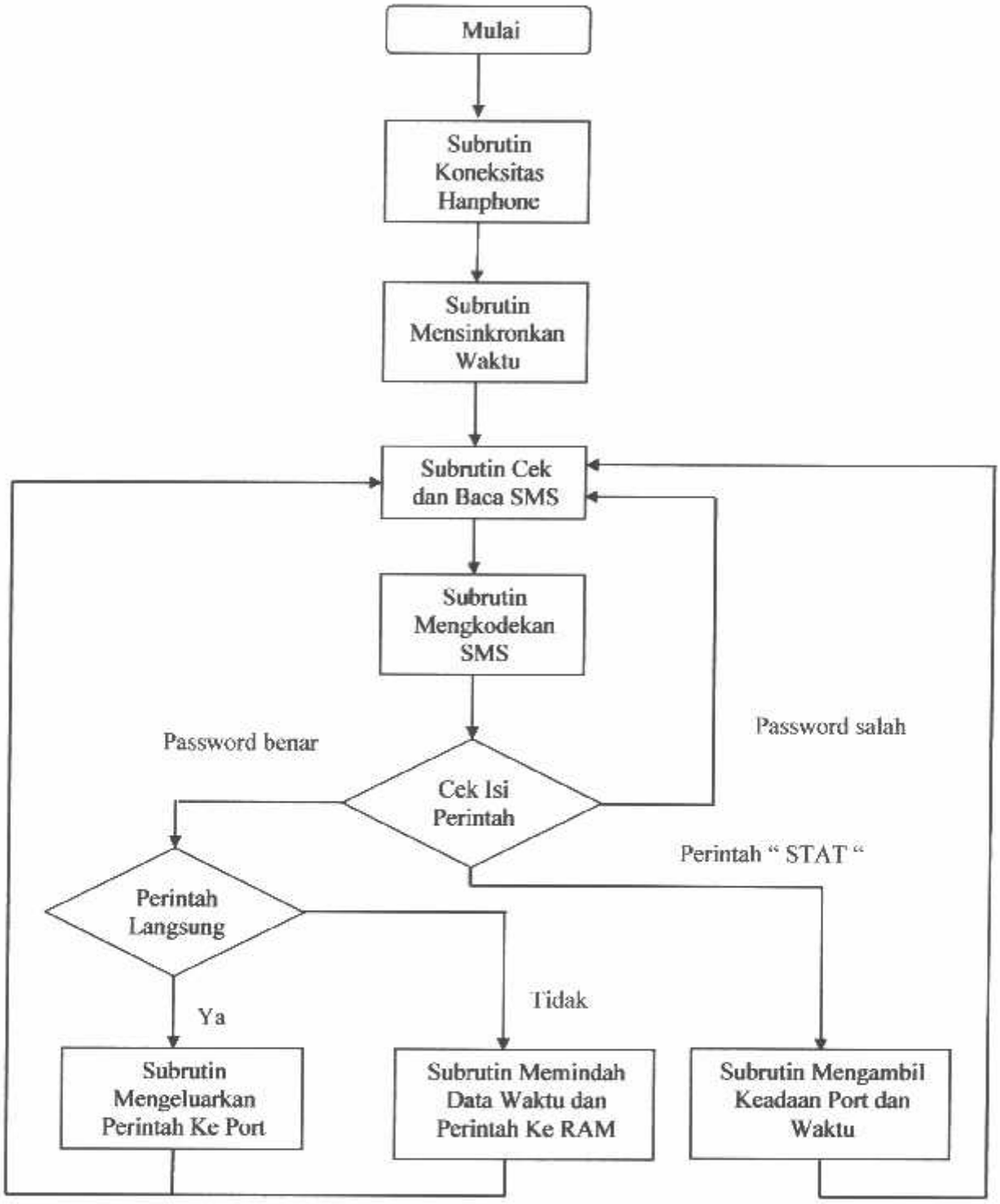
Tegangan input 12 V, Hambatan Motor 15 ohm Arus Untuk Motor :

$$I\ motor = \frac{Vin}{R\ motor} = \frac{12}{15} = 0.8A$$

3.2. Perancangan Perangkat Lunak

3.2.1. Program Utama

Alat dilengkapi dengan sistem *power-on reset*, sehingga ketika pertama kali *power* di nyalakan, alat akan me-*reset* keseluruhan program. Pada awal program dilakukan penginisialisasian komunikasi serial, kemudian interupsi-interupsi yang digunakan. Ketika alat petama kali dinyalakan, alat akan mendeteksi keberadaan *handphone*, apakah *handphone* sudah dalam terkoneksi ke alat atau belum. Sesudah itu alat akan menyamakan pewaktuan *handphone*, dengan mengambil data dari RTC. Kemudian alat akan menunggu SMS yang masuk. Bila ada SMS masuk, alat akan mengadakan proteksi panjang SMS. SMS yang memenuhi syarat akan didekodekan. Setelah di dekodekan, alat akan melakukan pengecekan *password* apakah *password* itu salah atau benar. Bila *password* benar, maka data waktu akan dikirim ke RTC, dan perintah yang akan di keluarkan dari port 2 di simpan di RAM. Data waktu adalah data yang di dapat dari hasil pendekodean SMS. Data ini berisi jam dan menit dari perintah yang akan di keluarkan. Jadi pelaksanaan perintah ini menunggu bila data waktu sudah sama dengan RTC. Selama menunggu, alat juga menunggu SMS baru yang masuk. Data waktu akan selalu mengambil data dari SMS yang terbaru. Jadi data waktu yang lama akan tertumpuk oleh data waktu yang lebih baru. Untuk berkomunikasi dengan handphone digunakan perintah *AT command*.



Flowchart 3.1. Parogram Utama

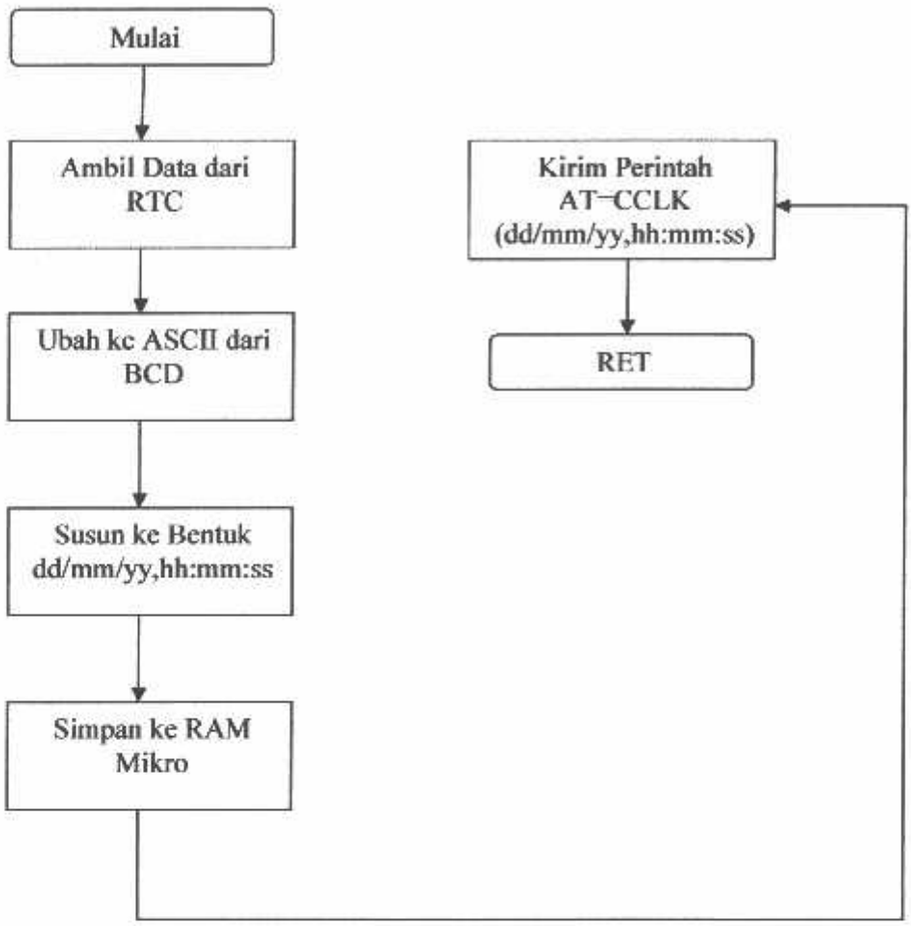
3.2.2. Subrutin Mengecek Koneksitas Handphone

Subrutin ini digunakan untuk mengecek keberadaan *handphone*, ketika alat pertama kali dinyalakan. Pengendali mikro akan mengirim data secara serial ke *handphone*, perintah yang di gunakan adalah "**ATE1**". Alat akan menunggu masukan dari *handphone* selama waktu tertentu. Bila belum ada masukan maka alat akan mengirim perintah itu lagi ke *handphone* dan LED *identifier* belum dinyalakan. Bila sudah ada balasan, maka LED *identifier* akan dinyalakan oleh alat dan subrutin ini selesai.

Flowchart 3.2. Subrutin Mengecek Koneksitas Handphone

3.2.3 Subrutin Mensinkronkan Waktu

Pada subrutin ini akan dilakukan penyamaan waktu antara *handphone* dengan alat. Jadi pertama-tama alat akan mengambil data dari RTC, yaitu data tanggal, bulan, tahun, jam, menit, detik. Lalu data yang semula berformat BCD, terlebih dahulu harus di ubah ke bentuk ASCII. Data ini kemudian di simpan terlebih dahulu di RAM pengendali mikro. Lalu perintah " **AT+CCLK=dd/mm/yy,hh:mm:ss** " di kirim ke *handphone* secara serial. Tentunya data waktu (dd/mm/yy,hh:mm:ss) diisi dengan data hasil olahan yang tadi telah disimpan di dalam RAM pengendali mikro. Setelah itu subrutin ini akan selesai dijalankan, dan program kembali ke program utama.



Flowchart 3.3. Subrutin Mesinkronkan Waktu

3.2.4. Subrutin Cek dan Baca SMS

Subrutin ini dimulai dengan mengirimkan perintah untuk mendeteksi keberadaan SMS di memory *handphone*. Perintah yang di gunakan adalah " **AT+CMGL=4** ". Jika tidak ada SMS, maka alat akan terus menerus mengirimkan perintah ini. Jika terdapat SMS di *memory handphone*, maka *handphone* akan membalas perintah tadi, yang dapat digambarkan sebagai berikut:

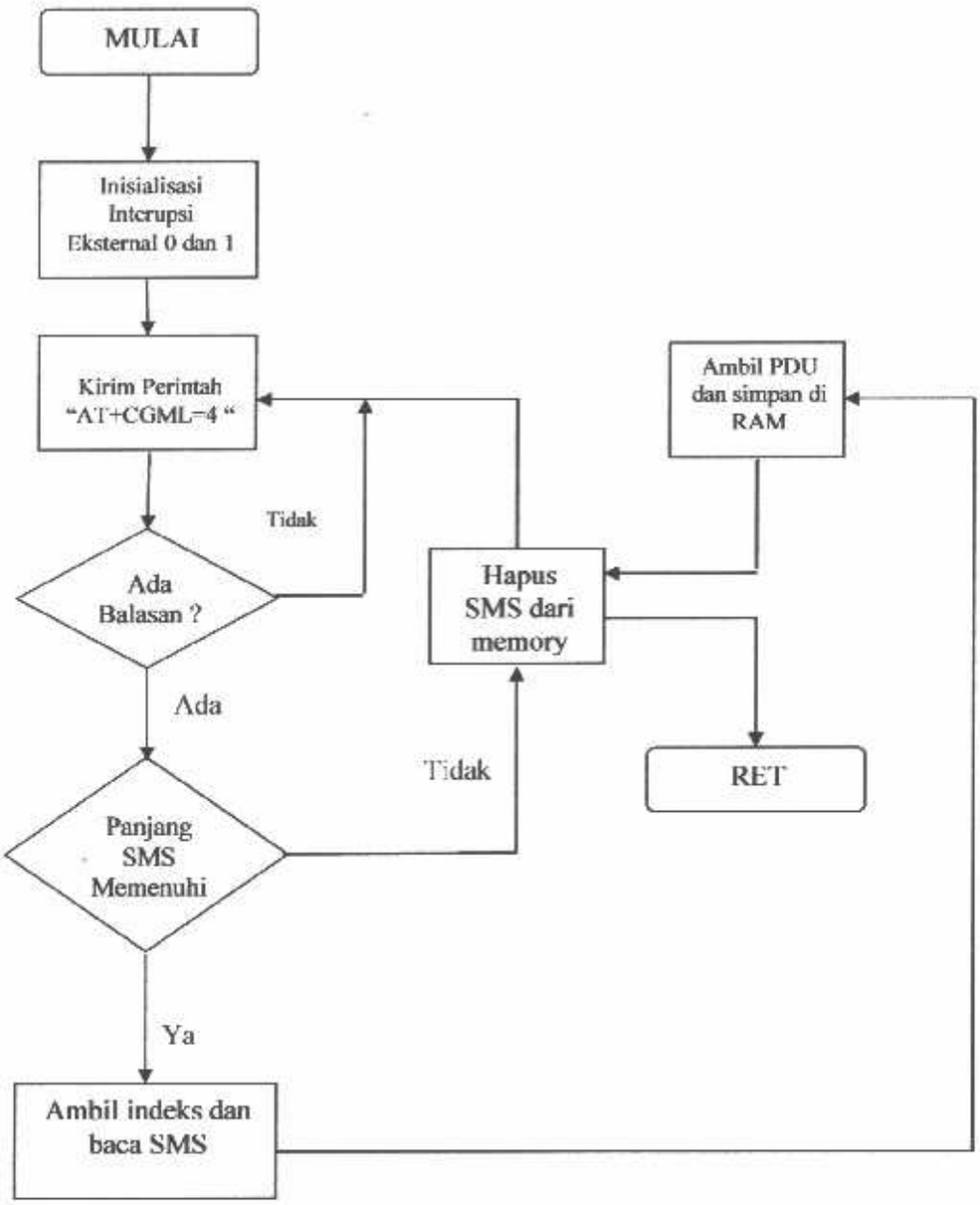
" +CMGL=<index><stat><length><CR><LF><PDU><CR><LF> "

penjelasan :

- Index : Index memory penyimpanan SMS di handphone.
- Stat : Merupakan status dari SMS (Read,Unread,Sto Sent,Sto Unsent,All).
- Length : Merupakan panjang SMS.
- CR : Carriage Return.
- LF : Line Feed.
- PDU : Protocol Data Unit, ini merupakan protokol dari pengiriman dan penerimaan SMS di handphone.

Setelah mendapatkan balasan dari *handphone*, alat akan mengambil data *length* dari SMS tadi. Lalu data itu akan dibandingkan dengan nilai tertentu yang bila data itu melebihi nilai tersebut maka SMS tersebut bukan sebuah perintah dan SMS akan dihapus dari memory *handphone*. Bila data itu lebih kecil dari nilai yang telah di tentukan tadi, maka SMS tersebut akan dianggap sebagai perintah. Setelah itu data indeks akan diambil. Alat akan mengirimkan perintah " **AT+CMGR=<index>** " yang digunakan untuk

membaca satu SMS secara khusus. Balasan dari *handphone* adalah " **+CMGR:<index>„<length><CR><LF><PDU>** ", data **<PDU>** saja yang akan disimpan di RAM. Lalu program akan kembali ke program utama. Di subrutin ini diaktifkan interupsi eksternal 0 yang digunakan untuk mendeteksi bila terjadi penekanan tombol. Juga diaktifkan interupsi eksternal 1 yang digunakan bila ada interupsi dari RTC.



Flowchart 3.4. Subrutin Cek dan Baca SMS

3.2.5. Subrutin Mendekode SMS

3.2.5.1.PDU *(Protocol Data Unit)*

Data yang mengalir dari atau ke *SMS-Center* harus berupa PDU. PDU ini berisi bilangan-bilangan heksa desimal yang mencerminkan bahasa I/O. PDU ini terdiri dari beberapa *header*. *Header* dari SMS terima berbeda dengan *header* dari SMS yang akan di kirimkan. Berikut ini dijelaskan ke delapan *header* untuk melakukan pengiriman SMS :

1. Nomor SMS-*center*

   Header pertama ini terbagi atas tiga *subheader*, yaitu :

   - Jumlah pasangan heksa desimal *SMS-Center* dalam bilangan heksa.
   - Kode nasional/internasional. Untuk kode nasional *subheader*-nya adalah 81, dan untuk kode internasionalnya adalah 91.
   - Nomor SMS-*centernya* sendiri, dalam pasangan heksa yang dibalik balik. Jika tertinggal satu angka heksa yang tidak memiliki pasangan, angka tersebut akan dipasangkan dengan huruf " F " di depannya. Contoh : *SMS-center* dalam kode PDU : 07912658050000F0 (IM-3), 07912618010000F0 (Telkomsel).

2. Tipe SMS

   Untuk *Send* Tipe SMS=1, jadi bilangan heksanya adalah 01.

3. Nomor referensi SMS

   Nomor referensi ini dibiarkan dulu 0, jadi bilangan heksanya adalah 00. Nanti akan diberikan sebuah nomor referensi otomatis oleh *handphone*.

4. Nomor *handphone* penerima

   Sama seperti cara menulis PDU *header* untuk *SMS-center*, *header* ini juga terbagi atas tiga bagian sebagai berikut :

- Jumlah bilangan desimal nomor yang dituju dalam bentuk bilangan heksa.
- Kode nasional/internasional.
- Nomor *handphone* yang di tuju, dalam pasangan heksa dibalik-balik. Jika tertinggal satu angka heksa yang tidak memiliki pasangan, angka tersebut dipasangkan dengan huruf " F " didepannya. Contoh : Misal untuk nomor *handphone* yang dituju : 62818452283.

  62818452283 diubah menjadi :

  - 0B karena ada 11 angka
  - 91
  - 26-18-48-25-82-F3
  - dan bila digabung menjadi : 0B912618482582F3

5. Bentuk SMS, antara lain :

- 0 00 dikirim sebagai SMS
- 1 01 dikirim sebagai telex
- 2 02 dikirim sebagai fax

6. Skema enkoding data I/O

Ada dua skema yaitu :

- Skema 7 bit ditandai dengan angka 0, dan dituliskan sebagai 00
- Skema 8 bit ditandai dengan angka lebih besar dari 0 diubah ke heksa. Pada sekarang ini semua *handphone* menggunakan skema 7 bit sehingga digunakan kode 00.

7. Jangka waktu sebelum *expired*

Bagian ini diberi angka 00 untuk tidak membatasi waktu berlakunya SMS.

8. Isi SMS

Header ini terdiri dari 2 *sub-header*, yaitu :

- Panjang isi, misal untuk kata "hello" berarti ada 5 huruf
- Isi SMS berupa pasangan bilangan heksa.

Adapun langkah yang harus dilakukan untuk mengkonversikan SMS ini yaitu:

1. Langkah pertama : mengubahnya ke kode 7 bit
2. Langkah kedua : mengubah 7 bit menjadi 8 bit yang diwakili oleh pasangan heksa.

Contoh : untuk kata "hello"

Langkah pertama :

h = 110 1000

e = 110 0101

l = 110 1100

l = 110 1100

o = 110 1111

Langkah kedua :

h = 1 110 1000 : 1110 1000 = E8

e = 00 110 010 1 : 0011 0010 = 32

l = 100 110 11 00 : 1001 1101 = 9B

l = 1111 110 1 100 : 1111 1101 = FD

o = 0000 0110 1111 : 0000 1111 = 06

Jadi kata "hello" bila dikonversikan akan menjadi E8329BFD06. Bila kata "hello" dikirimkan ke *handphone* 62818452283 lewat SMS-*center* exelcom, tanpa batas waktu expired, maka PDU lengkapnya adalah **07912618485400F901000B910B912618482582F3000005E8329BFD06**

Untuk PDU dari SMS terima kebanyakan *header* nya telah dibahas di atas. Namun ada beberapa hal yang berbeda, yaitu :

- Nomor SMS-*center*
- Tipe SMS untuk SMS terima bertipe 4 jadi penulisnya 04
- Nomor *handphone* pengirim
- Bentuk SMS
- Skema encoding
- Tanggal dan waktu SMS di SMS-*center*
- Batas waktu validitas
- Isi SMS

Di bawah ini akan diberikan contoh PDU yang diterima **07912658050000F0,04,0B912618482582F3,00,00207022512380,00,05E8329BF** D06 dapat diartikan sebagai berikut :

1. SMS itu dikirim dari SMS-*center* : 62855000000
2. SMS itu merupakan SMS terima.
3. SMS tersebut dikirim dari handphone no.628561013789
4. SMS diterima dalam bentuk teks.
5. SMS memiliki skema enkoding 7 bit.

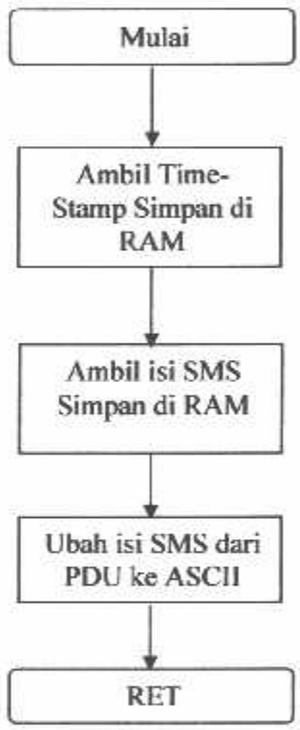
6.SMS sampai di SMS-*center* pada tanggal 22-06-06, pukul 15:32:08.

7. SMS tidak memiliki batas waktu validitas.

8. SMS tersebut berisi kata "hello".

3.2.5.2. Subrutin Pendekodean SMS

Subrutin pendekodean ini digunakan untuk mengambil *Time-Stamp* dari SMS, juga digunakan untuk menerjemahkan isi SMS dari bentuk data PDU menjadi ASCII. Lalu hasil pendekodean ini akan disimpan di RAM.



Flowchart 3.5. Subrutin Pendekodean SMS

3.2.6. Subrutin Mengeluarkan Perintah ke Port

Subrutin ini digunakan untuk mengeluarkan isi perintah ke *port* 2. Isi SMS yang sudah di ubah ke bentuk ASCII yang tersimpan di dalam RAM, akan dirubah ke bentuk heksa. Lalu data heksa inilah yang akan dikeluarkan ke *port* 2.

Flowchart 3.6. Subrutin Mengeluarkan Perintah ke Port

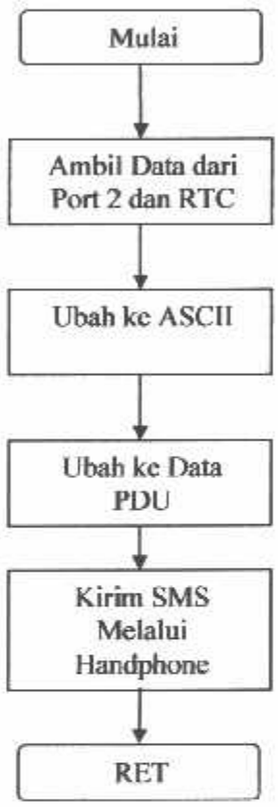
3.2.7. Subrutin Mengambil Data Waktu

Subrutin ini digunakan untuk menginisialisasi data waktu dari RAM kemudian waktu hasil dari pendekodean SMS akan diberikan ke RTC dan perintah akan di simpan di RAM.

Flowchart 3.7. Subrutin Mengambil Data Waktu

3.2.8. Subrutin Mengambil Data dari *Port* Keluaran

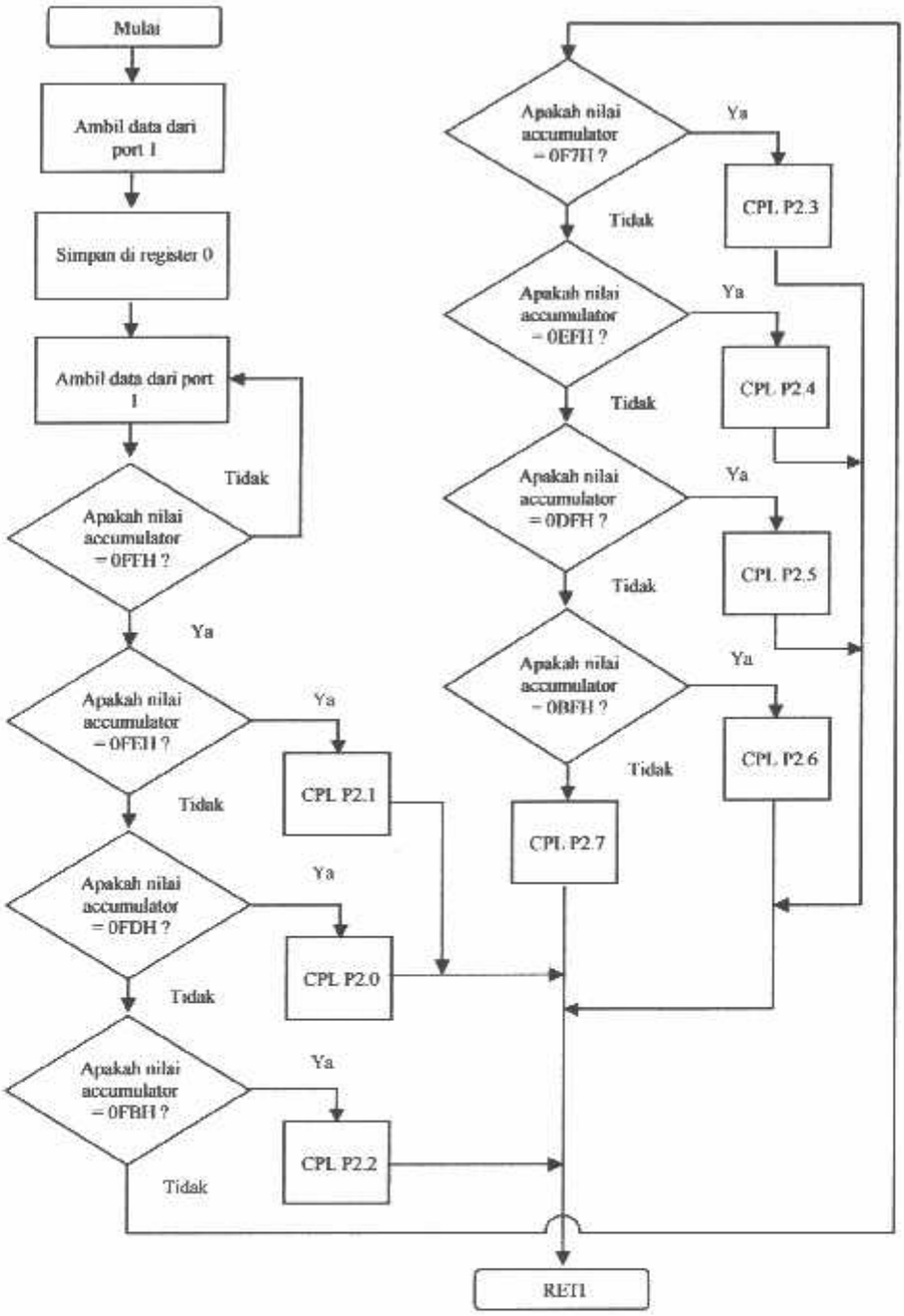
Subrutin ini digunakan untuk mengambil data dari *port* 2 keluaran dan RTC. Lalu diubah ke bilangan ASCII. Setelah itu data dalam bilangan ASCII diubah menjadi bentuk PDU. Data hasil olahan ini kemudian dikirimkan ke *handphone* penerima, dengan perintah " **AT+CMGS=<length><CR><PDU><Ctrl-Z>** "



Flowchart 3.8. Subrutin Pengambilan Data Dari Port 2 dan RTC

3.2.9. Interupsi Eksternal 0

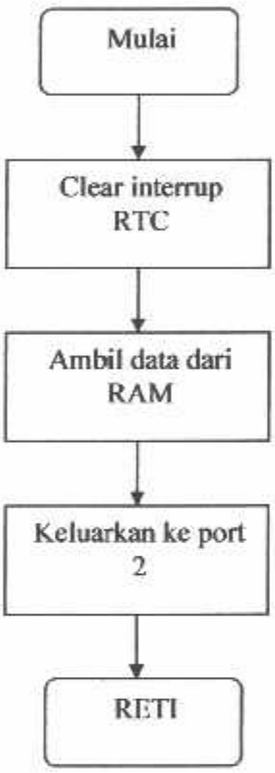
Interupsi ini digunakan bila ada penekanan tombol pada *port* 1. Bila terjadi penekanan, maka alat akan mengambil data dari *port* 1. akan di tunggu sampai *port* 1 memiliki keadaan 0FFh (tombol sudah di lepas), lalu akan di bandingkan hasil dari *port* 1, bila data berupa 0FEh maka *port* 2.0 akan di komplemen, bila data berupa 0FDh maka *port* 2.1 yang akan dikomplemenkan, dst.



Flowchart 3.9. Interupsi Eksternal 0

3.2.10. Interupsi Eksternal 1

Interupsi ini digunakan untuk menandai interupsi yang berasal dari RTC. Yang menandakan bahwa perintah dari SMS sudah dapat ditampilkan pada *port* 2 sebagai keluaran. Jadi data perintah ini akan diambil dari RAM.



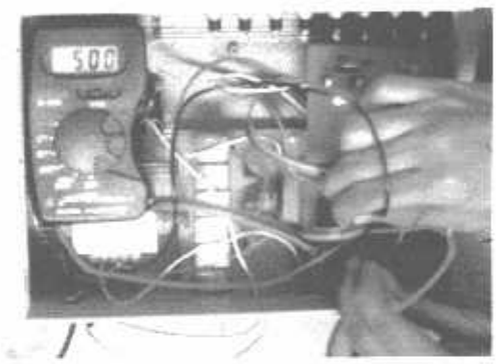
Flowchart 3.10. Interupsi Eksternal 1

BAB IV

PENGUJIAN ALAT

4.1. Pengujian Minimum Sistem AT89S52

Untuk pengujian pengendali mikrokontroller dilakukan dengan cara memberikan sebuah program singkat untuk mengeluarkan data sebesar 0AAh (10101010b) untuk tiap port.



Gambar 4.1. Pengukuran Keluaran Mikrokontroller

Dari hasil pengukuran dengan menggunakan volt meter ternyata pada setiap port pada mikrokontroller mengeluarkan data sebesar 0AAh (10101010b) maka dengan demikian pengendali mikrokontroller bekerja dengan baik.

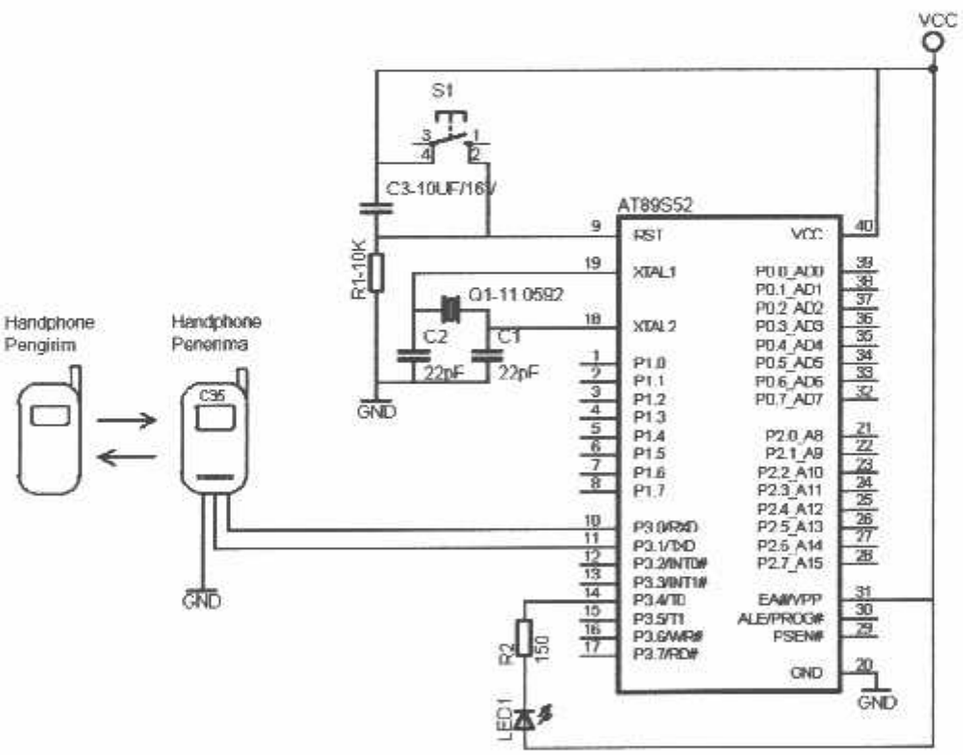
4. 2. Pengujian Konektivitas Handphone Dengan Pengendali Mikro AT89S52

Pengujian ini dilakukan dengan cara melakukan komunikasi data secara langung antara pengendali mikro AT89S52 dengan Handphone.

1. Pada waktu pertama kali pengendali mikro diaktifkan maka mikro akan mendeteksi ada atau tidaknya Handphone, apabila ada koneksi Handphone maka LED identifier akan menyala.

2. Mengirimkan SMS yang berisi " RUDI 00001111 " kepada pengendali mikro melalui Handphone Siemens C35, SMS tersebut adalah sebuah perintah untuk mengeluarkan data " 00001111 " di port 2.

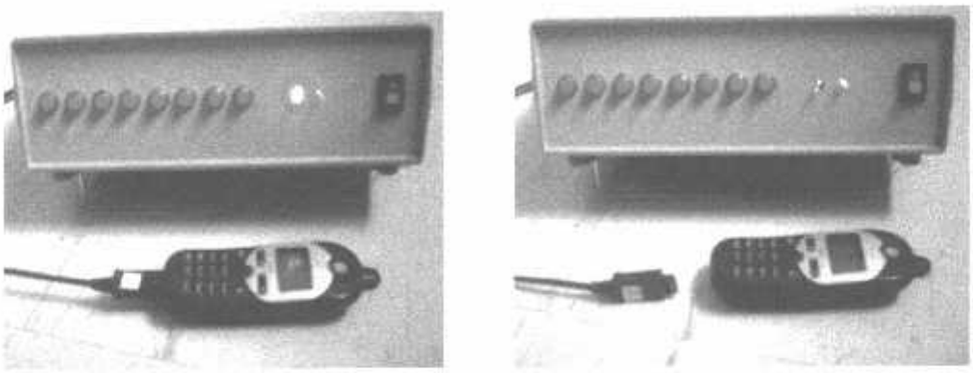
3. Mengirimkan SMS yang berisi " STAT " kepada pengendali mikro melalui Handphone Siemens C35, SMS tersebut adalah sebuah perintah untuk memberikan SMS balasan yang berisikan status data output pada port 2.



Gambar 4.1. Komunikasi Serial Antara Pengendali Mikro Dengan Handphone

Dari pengujian diatas diperoleh hasil

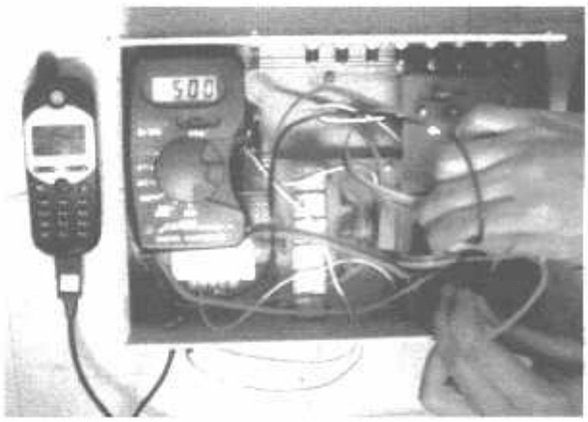
1. LED identifier pada pengendali mikro menyala apabila ada koneksi serial antara Handphone dengan pengendali mikro, dan mati apabila koneksi tersbut terputus.



(a) *(b)*

Gambar 4.2. *(a)* Handphone Terhubung Dengan Mikro
(b) Handphone Terputus Dengan Mikro

2. SMS berisi perintah " RUDI 00001111 " yang dikirimkan ke pengendali mikro melalui Handphone Siemens C35, dibaca oleh pengendali mikro dan dikeluarkan di port 2. Dilakukan pengukuran dengan menggunakan volt meter.



Gambar 4.3. Pengukuran Keluaran Pada Port 2

3. SMS berisi perintah " STAT " yang dikirim ke pengendali mikro melalui Handphone Siemens C35 memberikan balasan SMS yang berisi " 00001111 " yang berarti pada port 2 sedang mengeluarkan data tersebut.

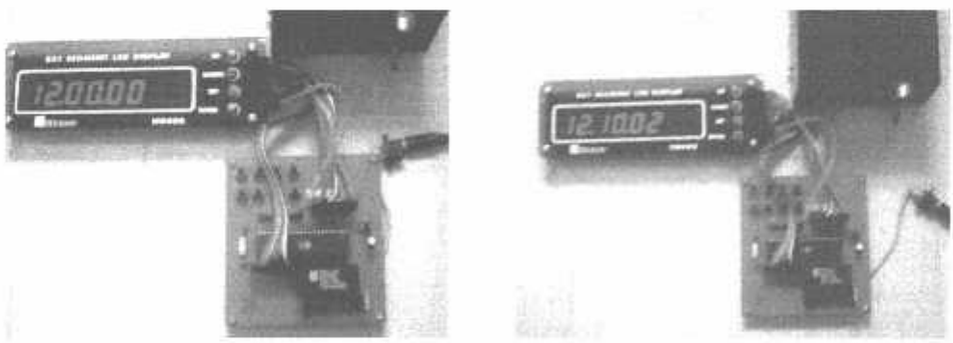
Dengan demikian maka komunikasi serial antara Handphone dengan pengendali mikro AT89S52 dapat berfungsi baik sesuai dengan perencanaan.

4.3. Pengujian RTC

Pengujian RTC dilakukan dengan cara, membuat program untuk memasukan data waktu tertentu ke RTC pada pengendali mikro. Data yang di masukkan adalah 06-10-06, 12:00:00. Kemudian dilakukan pemutusan supply selama beberapa lama. Lalu dibuat program lagi yang di gunakan untuk membaca waktu dari RTC. Ternyata waktu yang tercatat 06-10-06, 12:10:00. Berdasarkan hal itu, maka dapat disimpulkan bahwa RTC telah berfungsi dengan baik.

Tabel 4.1. Hasil Pengujian IC RTC

No	Input waktu	Lama Waktu RTC Terputus Dari Power Supply (Menit)	Output
1	12.00.00	5	12.05.00
2	12.10.00	10	12.20.00
3	12.30.00	30	13.00.00

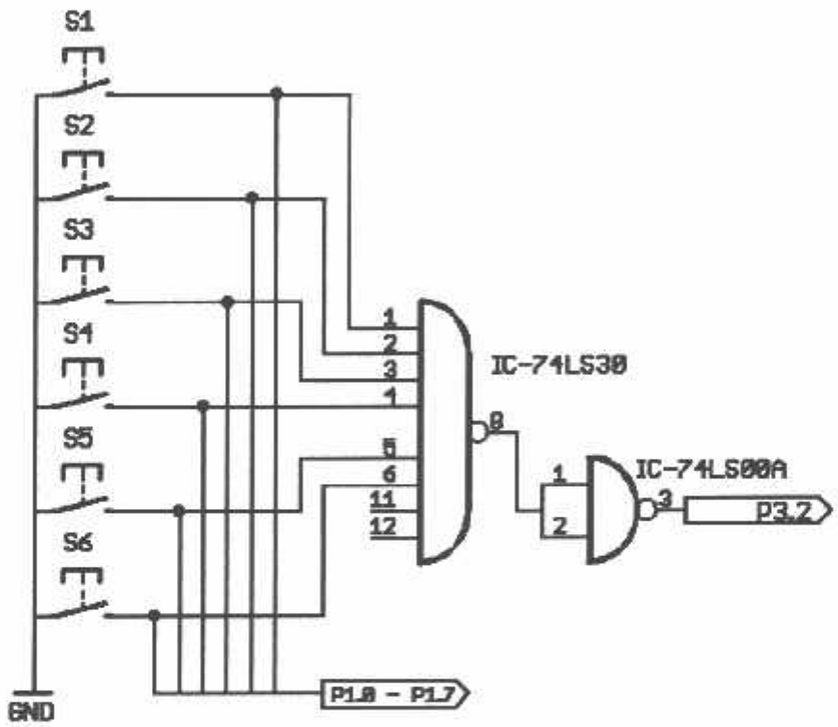


(*a*) (*b*)

Gambar 4.4. Pengujian IC RTC (*a*) Pemberian Progam Awal Pada RTC
(*b*) Pemutusan Power Supply Selama 10 Menit

4.4. Pengujian Saklar On-Off Manual

Pengujian saklar on-off manual dilakukan dengan cara membuat program pengendali mikro, untuk mendeteksi dan mengidentifikasikan penekanan tombol. Jadi penekanan tombol akan menyebabkan penyalaan lampu, sesuai dengan tombol yang di tekan.



Gambar 4.5. Rangkaian Saklar Input

Tabel 4.2. Hasil Pengujian Rangkaian Saklar Input

No	Input						Output (Y)	
	S1	S2	S3	S4	S5	S6	IC74LS30 (pin 8)	74LS00 (pin 3)
1	0	1	1	1	1	1	1	0
2	1	0	1	1	1	1	1	0
3	1	1	0	1	1	1	1	0
4	1	1	1	0	1	1	1	0
5	1	1	1	1	0	1	1	0
6	1	1	1	1	1	0	1	0
7	1	1	1	1	1	1	0	1

Setelah program dijalankan, ternyata pengendali mikro dapat mengenali semua saklar dan dapat menyalakan lampu sesuai dengan tombol yang di tekan. Jadi saklar on-off manual ini telah berfungsi dengan baik.

4.5. Pengujian Keluaran

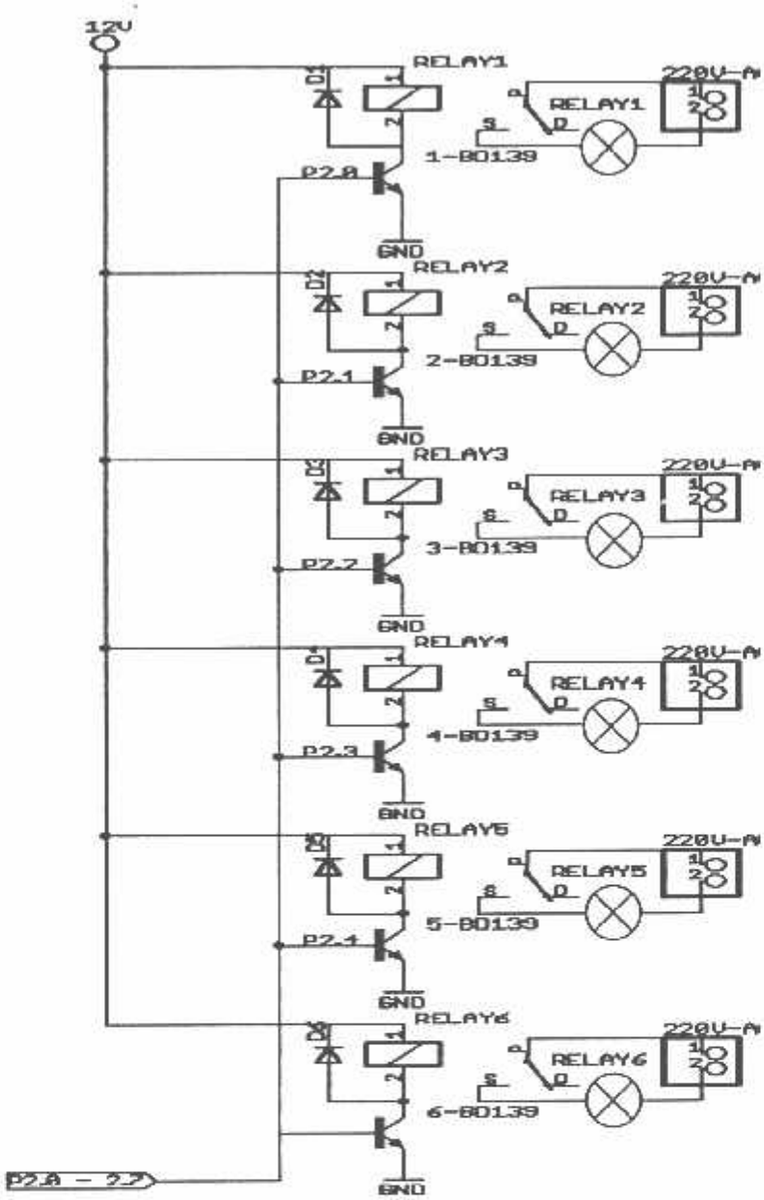
4.5.1. Pengujian Driver Lampu

Pengujian ini dilakukan dengan memberikan lampu, pada keluaran pengendali mikro P2.0 – P2.5. Jadi terdapat 6 lampu yang akan menampilkan keadaan dari keluaran alat..

Tabel 4.3. Hasil Pengujian Rangkaian Driver Lampu

No	Input						Output (LAMPU)
	P2.0	P2.1	P2.2	P2.3	P2.4	P2.5	RELAY " ON "
1	1	0	0	0	0	0	1
2	0	1	0	0	0	0	2
3	0	0	1	0	0	0	3
4	0	0	0	1	0	0	4
5	0	0	0	0	1	0	5
6	0	0	0	0	0	1	6

Alat diperintahkan untuk mematikan keluaran, ternyata lampu yang terpasang tidak menyala. Tetapi bila alat diperintahkan untuk menyalakan keluaran, maka lampu yang terpasang akan menyala. Berdasarkan hal ini dapat disimpulkan bahwa keluaran dari pengendali mikro sudah dapat berfungsi dengan baik pada rangkaian driver lampu.



Gambar 4.6. Rangkaian Driver Lampu

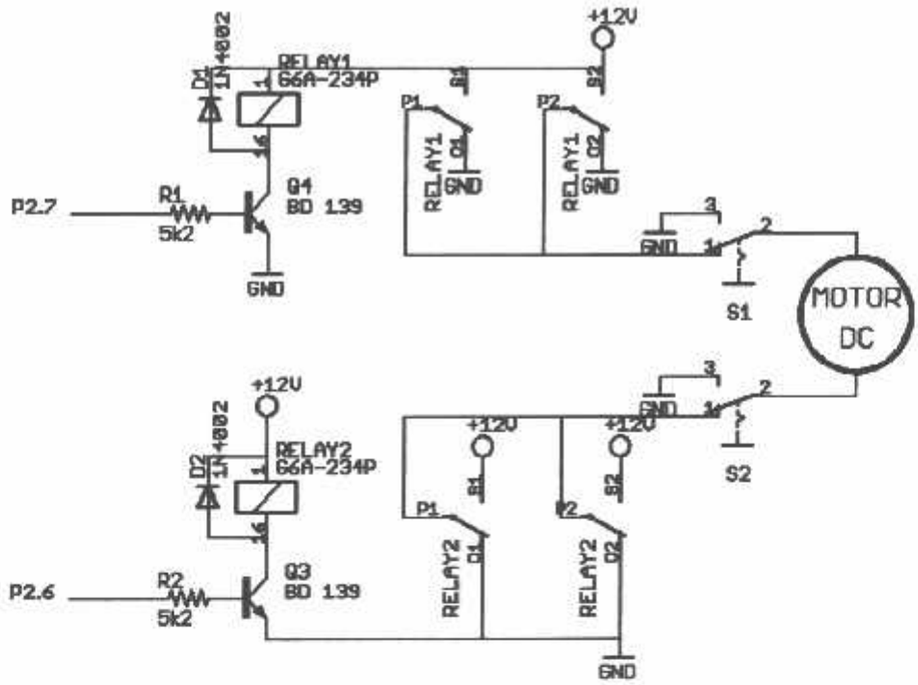
4.5.2. Pengujian Driver Motor DC

Pengujian ini dilakukan dengan cara memberikan sebuah pintu yang terangkai pada sebuah motor DC yang dihubungkan pada keluaran mikro yaitu P2.6 dan P2.7. Pintu akan membuka dan menutup apabila ada perintah untuk motor.

Tabel 4.4. Hasil Pengujian Rangkaian Driver Motor DC

No	PORT		OUTPUT
	P2.6	P2.7	
1	0	0	-
2	0	1	BUKA
3	1	0	TUTUP
4	1	1	-

Perintah yang di berikan untuk motor DC adalah port 2.6 dan port 2.7 di beri logika " 0 1 " motor bergerak, pintu terbuka dan port 2.6 dan port 2.7 di beri logika " 1 0 " motor bergerak, pintu menutup. Berdasarkan hal itu, maka dapat disimpulkan bahwa keluaran dari pengendali mikro untuk rangkaian driver motor DC telah berfungsi dengan baik.



Gambar 4.7. Rangkaian Driver Motor DC

4.6. Pengujian Keseluruhan Alat

Pertama kali power supply disambungkan, maka lampu power di alat akan menyala, yang menandakan bahwa power supply sudah terkoneksi dengan alat. lampu indentifier masih dalam keadaan mati. Kemudian Handphone dihubungkan ke alat, maka lampu ini akan menyala. Bila Handphone di lepas dari alat, maka lampu ini akan mati lagi. Kemudian Handphone dibiarkan dalam keadaan standbay. Lalau di coba mengirim SMS yang berisi " RUDI 00001111 ". Setelah SMS diterima oleh Handphone, maka keluaran dari alat akan menjadi 00001111. Kemudian dilakukan penekanan saklar yang menyebabkan keluaran bernilai " 11110000 ". Lalu dikirim

SMS ke Handphone penerima dengan perintah " STAT ". Maka di Handphone pengirim akan mendapat SMS balasan dari alat yang berisi " 11110000 ".

Dari pengujian kesceluruhan alat ini maka dapat disimpulkan bahwa seluruh perangkat komponen pada alat ini dapat berfungsi dengan baik.

BAB V

PENUTUP

5.1. Kesimpulan

Secara keseluruhan mulai dari perancangan, realisasi dan pengujian sistem, dapat ditarik beberapa kesimpulan, antara lain :

1. Komunikasi serial antara Handphone dengan mikrokontroller AT89S52 yang dihubungkan secara langsung dapat berfungsi dengan baik dari koneksi *RX/TX* handphone ke *RX/TX* pengendali mikrokontroller AT89S52.
2. IC RTC DS12C887 digunakan sebagai pencatat waktu yang kemudian dibaca oleh mikrokontroller AT89S52 dimana RTC akan tetap bekerja meskipun tidak terhubung dengan power supply karena memiliki beterai internal.
3. Agar dapat mengaktifkan lampu dan menggerakan motor untuk membuka dan menutup pintu output mikrokontroller AT89S52 memerlukan rangkaian driver. Alat dapat menyalakan lampu dengan daya maksimum 2400 W, sedangkan untuk membuka dan menutup pintu menggunakan motor. Relay yang dipakai disesuaikan dengan daya yang dibutuhkan motor.
4. Secara keseluruhan alat pengendali lampu dan pintu jarak jauh ini dapat bekerja dan berfungsi dengan baik serta dapat digunakan untuk mengetahui kondisi terakhir dari peralatan yang dikendalikan.

5.2. Saran Pengembangan

Dari perancangan sistem yang telah direalisasikan pada tugas akhir ini, diharapkan dapat menjadi dasar penelitian lebih lanjut. Alat pengontrolan ini dapat di kembangkan dengan tahapan sebagai berikut:

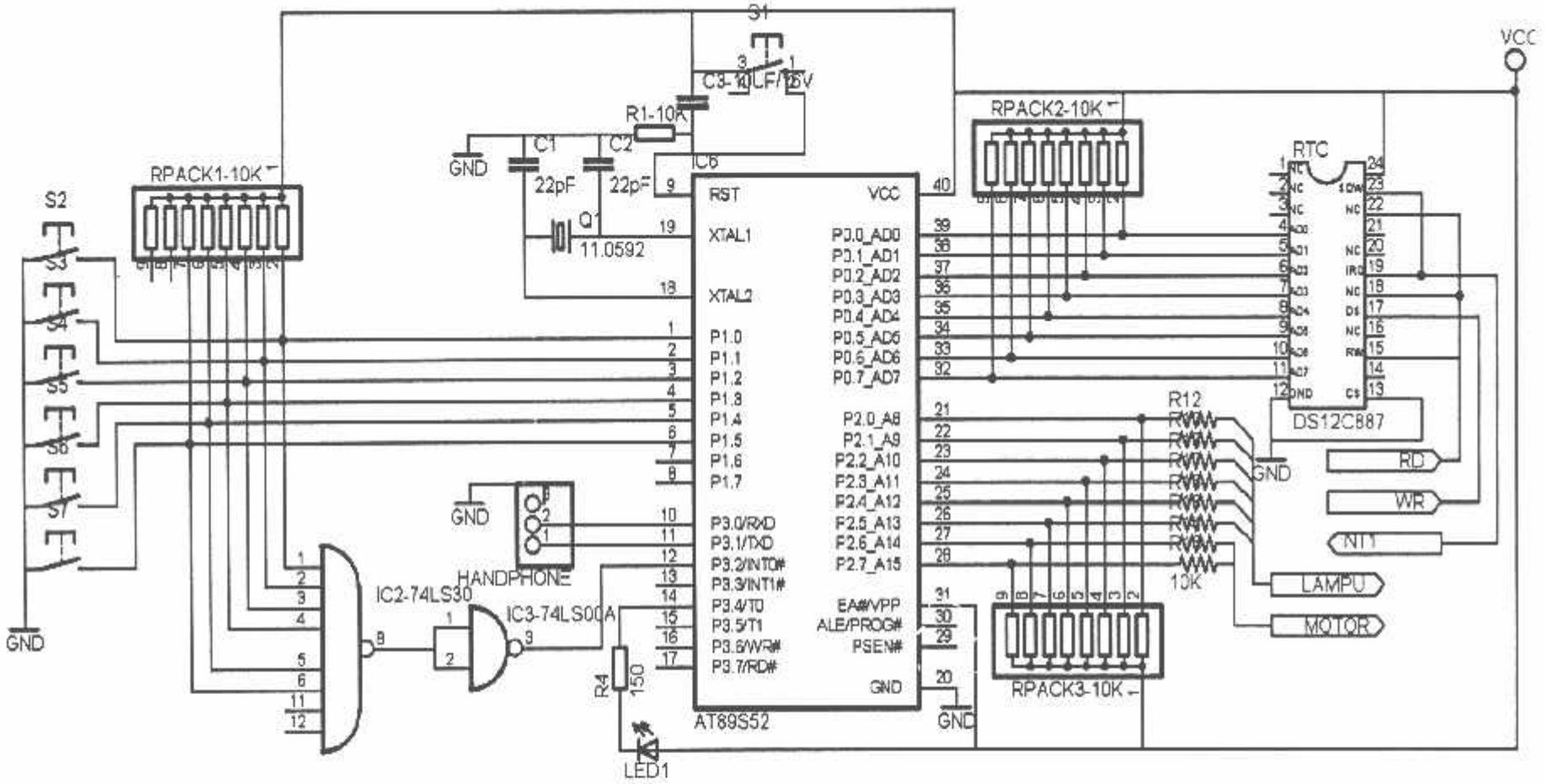
1. SMS perintah yang di kirimkan tidak hanya memuat satu perintah saja, tetapi juga memuat beberapa perintah, sehingga seakan-akan alat dapat dijadwalkan.

2. *Password* dapat diperbaharui dengan menggunakan perintah SMS itu sendiri. Sehingga untuk penggantian *password* tidak perlu memprogram ulang pengendali mikrokontroller.

3. Alat dapat diperintahkan untuk mengirim SMS sebagai pengaman rumah.

4. Keluaran alat dapat mengendalikan lebih dari 8 piranti.

5. Alat dapat digunakan untuk menyalakan dan mematikan kendaraan sepeda motor untuk menghindari pencurian.



Rangkaian Lengkap

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INSTITUT TEKNOLOGI NASIONAL MALANG
FAKULTAS TEKNOLOGI INDUSTRI
JURUSAN TEKNIK ELEKTRO D-III

LEMBAR ASISTENSI BIMBINGAN TUGAS AKHIR

Nama : Agustinus Ruddy

Nim : 03.57.015

Waktu Bimbingan :

Judul : Perencanaan Dan Pembuatan Alat Pengendali Lampu Dan Pintu Secara Jarak Jauh Berbasis Mk AT89S52

No	Tanggal	Materi	Paraf
1	10-1-2007	BAB I - Latar belakang yg menarik - Batasan masalah - Rumusan —"— - tujuan.	
2.	15-2-2007	BAB II - Dasar teori masukkan hal2 yg terkait dgn komponen yg digunakan	
3	25/2'07	BAB III - Blok diagram sistem - rangk. mikrokontroller - diagram alir	
4.	2/3'07	BAB IV. - Pengujian, metode, hasil, analisa. - kesimpulan prinsip kerja hasil percobaan	
5	9/3'07	BAB V Kesimpulan & saran	

Malang, 10 - 3 - 2007

Mengetahui Dosen Pembimbing

(Ir. Kartiko Adi Widodo, MT)

INSTITUT TEKNOLOGI NASIONAL
FAKULTAS TEKNOLOGI INDUSTRI
JURUSAN TEKNIK ELEKTRO D-III
PROGRAM STUDI TEKNIK ELEKTRONIKA
MALANG

BERITA ACARA UJIAN TUGAS AKHIR
FAKULTAS TEKNOLOGI INDUSTRI

Nama	: Agustinus Ruddy Catur Utomo.
NIM	: 03.57.015.
Jurusan	: Teknik Elektro D-III.
Program Studi	: Teknik Elektronika.
Judul Tugas Ahkir	: Perencanaan dan Pembuatan Alat Pengendali Lampu dan Pintu Jarak Jauh Berbasis Mikrokontroller AT89S52.

Dipertahankan di hadapan Team penguji Tugas Akhir Jenjang Diploma (D-III) :

Pada Hari : Kamis

Tanggal : 22 Maret 2007

Dengan nilai : 80,85 (A)

Panitia Ujian Tugas Akhir

(Ir. Mochtar Asroni, MSME)
Ketua Majelis Penguji

(Ir. H Choirul Saleh, MT)
Sekretaris Majelis Penguji

Anggota Penguji

(Ir. M. Abdul Hamid, MT)
Pertama

(Ir. Yunior Siahaan)
Kedua

INSTITUT TEKNOLOGI NASIONAL
FAKULTAS TEKNOLOGI INDUSTRI
JURUSAN TEKNIK ELEKTRO D-III
PROGRAM STUDI TEKNIK ELEKTRONIKA
MALANG

LEMBAR PERBAIKAN TUGAS AKHIR

Telah dilakukan perbaikan oleh:

Nama	: Agustinus Ruddy Catur Utomo.
NIM	: 03.57.015.
Jurusan	: Teknik Elektro D-III.
Program Studi	: Teknik Elektronika.
Hari/Tanggal	: Kamis / 22 Maret 2007

No.	Materi Perbaikan	Paraf
1.	Tujuan disesuaikan dengan pembahasan.	
2.	Tambahkan mengenai spesifikasi (kemampuan) alat yang dibuat, baik pada bab pembahasan maupun di bab kesimpulan.	

Telah Diperiksa/Disetujui:

Anggota Penguji I

(Ir. M. Abdul Hamid, MT)

Anggota Penguji II

(Ir. Yunior Siahaan)

Mengetahui :
Dosen Pembimbing

(Ir. Kartiko Adi Widodo, MT)

INSTITUT TEKNOLOGI NASIONAL
FAKULTAS TEKNOLOGI INDUSTRI
JURUSAN TEKNIK ELEKTRO D-III
PROGRAM STUDI TEKNIK ELEKTRONIKA
MALANG

LEMBAR BIMBINGAN TUGAS AKHIR

Nama	: Agustinus Ruddy Catur Utomo.
NIM	: 03.57. 015.
Jurusan	: Teknik Elektro D-III.
Program Studi	: Teknik Elektronika.
Judul Tugas Ahkir	: Perencanaan dan Pembuatan Alat Pengendali Lampu dan Pintu Jarak Jauh Berbasis Mikrokontroller AT89S52.
Dosen Pembimbing	: Ir. Kartiko Adi Widodo, MT
Telah Dievaluasi Dengan Nilai	: 87 (Delapan Puluh Tujuh)

Mengetahui:
Ketua Jurusan Elektro D-III

(Ir. H Choirul Saleh, MT)

Diperiksa dan Disetujui:
Dosen Pembimbing

(Ir. Kartiko Adi Widodo, MT)

LAMPIRAN

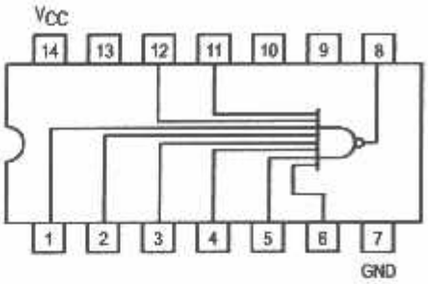
MOTOROLA

8-INPUT NAND GATE

SN54/74LS30

8-INPUT NAND GATE

LOW POWER SCHOTTKY



J SUFFIX
CERAMIC
CASE 632-08

N SUFFIX
PLASTIC
CASE 646-06

D SUFFIX
SOIC
CASE 751A-02

ORDERING INFORMATION

SN54LSXXJ	Ceramic
SN74LSXXN	Plastic
SN74LSXXD	SOIC

GUARANTEED OPERATING RANGES

Symbol	Parameter		Min	Typ	Max	Unit
V_{CC}	Supply Voltage	54 74	4.5 4.75	5.0 5.0	5.5 5.25	V
T_A	Operating Ambient Temperature Range	54 74	−55 0	25 25	125 70	°C
I_{OH}	Output Current — High	54, 74			−0.4	mA
I_{OL}	Output Current — Low	54 74			4.0 8.0	mA

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

Symbol	Parameter		Limits Min	Limits Typ	Limits Max	Unit	Test Conditions	
V_{IH}	Input HIGH Voltage		2.0			V	Guaranteed Input HIGH Voltage for All Inputs	
V_{IL}	Input LOW Voltage	54			0.7	V	Guaranteed Input LOW Voltage for All Inputs	
		74			0.8			
V_{IK}	Input Clamp Diode Voltage			−0.65	−1.5	V	V_{CC} = MIN, I_{IN} = −18 mA	
V_{OH}	Output HIGH Voltage	54	2.5	3.5		V	V_{CC} = MIN, I_{OH} = MAX, V_{IN} = V_{IH} or V_{IL} per Truth Table	
		74	2.7	3.5		V		
V_{OL}	Output LOW Voltage	54, 74		0.25	0.4	V	I_{OL} = 4.0 mA	V_{CC} = V_{CC} MIN, V_{IN} = V_{IL} or V_{IH} per Truth Table
		74		0.35	0.5	V	I_{OL} = 8.0 mA	
I_{IH}	Input HIGH Current				20	μA	V_{CC} = MAX, V_{IN} = 2.7 V	
					0.1	mA	V_{CC} = MAX, V_{IN} = 7.0 V	
I_{IL}	Input LOW Current				−0.4	mA	V_{CC} = MAX, V_{IN} = 0.4 V	
I_{OS}	Short Circuit Current (Note 1)		−20		−100	mA	V_{CC} = MAX	
I_{CC}	Power Supply Current Total, Output HIGH				0.5	mA	V_{CC} = MAX	
	Total, Output LOW				1.1			

Note 1: Not more than one output should be shorted at a time, nor for more than 1 second.

AC CHARACTERISTICS (T_A = 25°C)

Symbol	Parameter	Limits Min	Limits Typ	Limits Max	Unit	Test Conditions
t_{PLH}	Turn-Off Delay, Input to Output		8.0	15	ns	V_{CC} = 5.0 V, C_L = 15 pF
t_{PHL}	Turn-On Delay, Input to Output		13	20	ns	

FAIRCHILD
SEMICONDUCTOR™

August 1986
Revised March 2000

DM74LS00
Quad 2-Input NAND Gate

General Description

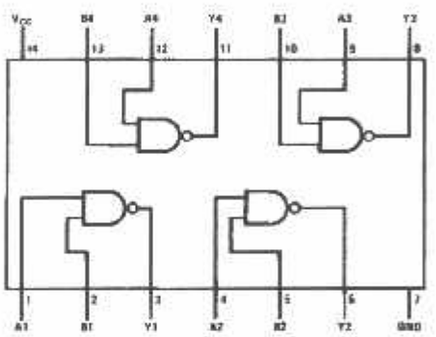
This device contains four independent gates each of which performs the logic NAND function.

Ordering Code:

Order Number	Package Number	Package Description
DM74LS00M	M14A	14-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-120, 0.150 Narrow
DM74LS00SJ	M14D	14-Lead Small Outline Package (SOP), EIAJ TYPE II, 5.3mm Wide
DM74LS00N	N14A	14-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300 Wide

Devices also available in Tape and Reel. Specify by appending the suffix letter "X" to the ordering code.

Connection Diagram



Function Table

$Y = \overline{AB}$

Inputs		Output
A	B	Y
L	L	H
L	H	H
H	L	H
H	H	L

H = HIGH Logic Level
L = LOW Logic Level

Absolute Maximum Ratings(Note 1)

Supply Voltage	7V
Input Voltage	7V
Operating Free Air Temperature Range	0°C to +70°C
Storage Temperature Range	−65°C to +150°C

Note 1: The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the Electrical Characteristics tables are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

Recommended Operating Conditions

Symbol	Parameter	Min	Nom	Max	Units
V_{CC}	Supply Voltage	4.75	5	5.25	V
V_{IH}	HIGH Level Input Voltage	2			V
V_{IL}	LOW Level Input Voltage			0.8	V
I_{OH}	HIGH Level Output Current			−0.4	mA
I_{OL}	LOW Level Output Current			8	mA
T_A	Free Air Operating Temperature	0		70	°C

Electrical Characteristics

over recommended operating free air temperature range (unless otherwise noted)

Symbol	Parameter	Conditions	Min	Typ (Note 2)	Max	Units
V_I	Input Clamp Voltage	V_{CC} = Min, I_I = −18 mA			1.5	V
V_{OH}	HIGH Level Output Voltage	V_{CC} = Min, I_{OH} = Max, V_{IL} = Max	2.7	3.4		V
V_{OL}	LOW Level Output Voltage	V_{CC} = Min, I_{OL} = Max, V_{IH} = Min		0.35	0.5	V
		I_{OL} = 4 mA, V_{CC} = Min		0.25	0.4	
I_I	Input Current @ Max Input Voltage	V_{CC} = Max, V_I = 7V			0.1	mA
I_{IH}	HIGH Level Input Current	V_{CC} = Max, V_I = 2.7V			20	µA
I_{IL}	LOW Level Input Current	V_{CC} = Max, V_I = 0.4V			−0.36	mA
I_{OS}	Short Circuit Output Current	V_{CC} = Max (Note 3)	−20		−100	mA
I_{CCH}	Supply Current with Outputs HIGH	V_{CC} = Max		0.8	1.6	mA
I_{CCL}	Supply Current with Outputs LOW	V_{CC} = Max		2.4	4.4	mA

Note 2: All typicals are at V_{CC} = 5V, T_A = 25°C.

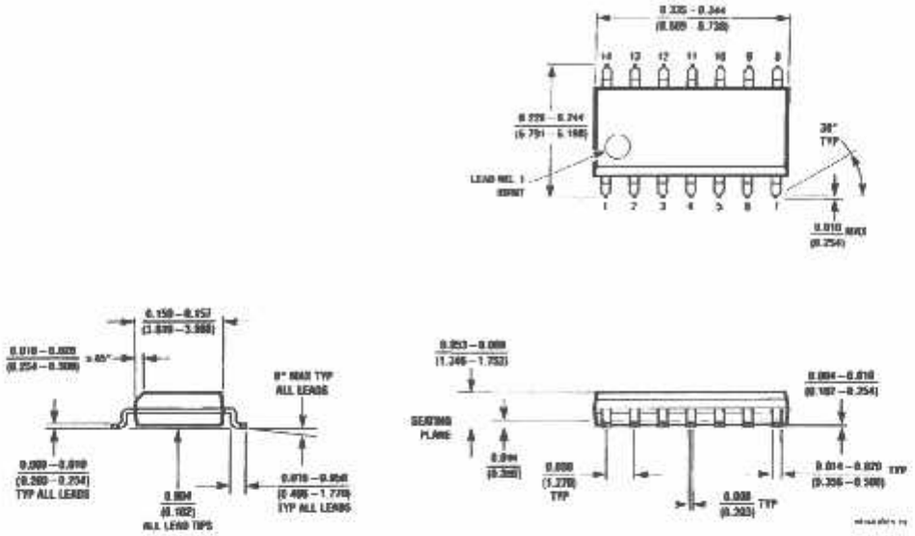
Note 3: Not more than one output should be shorted at a time, and the duration should not exceed one second.

Switching Characteristics

at V_{CC} = 5V and T_A = 25°C

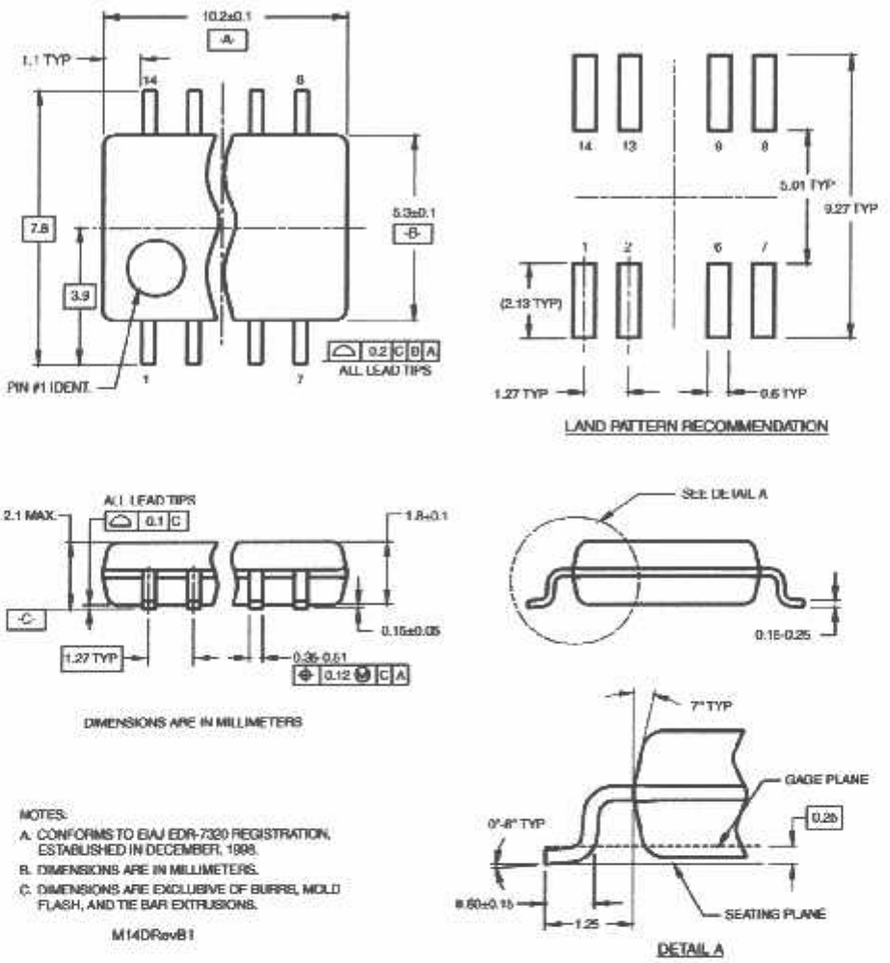
Symbol	Parameter	R_L = 2 kΩ				Units
		C_L = 15 pF		C_L = 50 pF		
		Min	Max	Min	Max	
t_{PLH}	Propagation Delay Time LOW to HIGH Level Output	3	10	4	15	ns
t_{PHL}	Propagation Delay Time HIGH to LOW Level Output	3	10	4	15	ns

Physical Dimensions inches (millimeters) unless otherwise noted



14-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-120, 0.150 Narrow
Package Number M14A

Physical Dimensions inches (millimeters) unless otherwise noted (Continued)



NOTES:

A. CONFORMS TO EIAJ EDR-7320 REGISTRATION, ESTABLISHED IN DECEMBER, 1998.

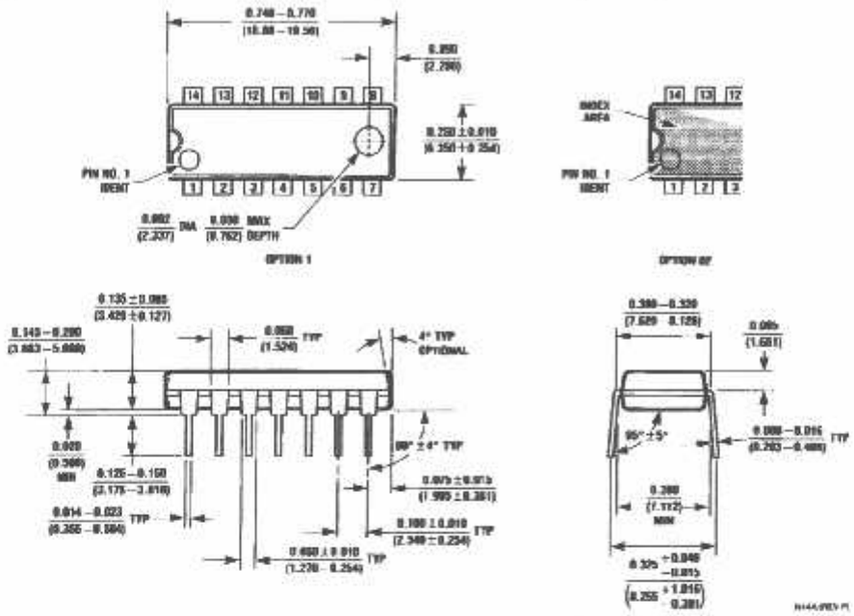
B. DIMENSIONS ARE IN MILLIMETERS.

C. DIMENSIONS ARE EXCLUSIVE OF BURRS, MOLD FLASH, AND TIE BAR EXTRUSIONS.

M14DRevB1

14-Lead Small Outline Package (SOP), EIAJ TYPE II, 5.3mm Wide
Package Number M14D

Physical Dimensions inches (millimeters) unless otherwise noted (Continued)



14-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300 Wide
Package Number N14A

ures

patible with MCS-51® Products
ytes of In-System Programmable (ISP) Flash Memory
Endurance: 1000 Write/Erase Cycles
to 5.5V Operating Range
Static Operation: 0 Hz to 33 MHz
a-level Program Memory Lock
: 8-bit Internal RAM
ogrammable I/O Lines
e 16-bit Timer/Counters
: Interrupt Sources
Duplex UART Serial Channel
power Idle and Power-down Modes
upt Recovery from Power-down Mode
hdog Timer
Data Pointer
r-off Flag
Programming Time
ole ISP Programming (Byte and Page Mode)

:ription

'89S52 is a low-power, high-performance CMOS 8-bit microcontroller with 8K
if in-system programmable Flash memory. The device is manufactured using
high-density nonvolatile memory technology and is compatible with the indus-
ndard 80C51 instruction set and pinout. The on-chip Flash allows the program
y to be reprogrammed in-system or by a conventional nonvolatile memory pro-
er. By combining a versatile 8-bit CPU with in-system programmable Flash on
lithic chip, the Atmel AT89S52 is a powerful microcontroller which provides a
lexible and cost-effective solution to many embedded control applications.

39S52 provides the following standard features: 8K bytes of Flash, 256 bytes
, 32 I/O lines, Watchdog timer, two data pointers, three 16-bit timer/counters, a
or two-level interrupt architecture, a full duplex serial port, on-chip oscillator,
ck circuitry. In addition, the AT89S52 is designed with static logic for operation
zero frequency and supports two software selectable power saving modes.
Mode stops the CPU while allowing the RAM, timer/counters, serial port, and
t system to continue functioning. The Power-down mode saves the RAM con-
t freezes the oscillator, disabling all other chip functions until the next interrupt
vare reset.

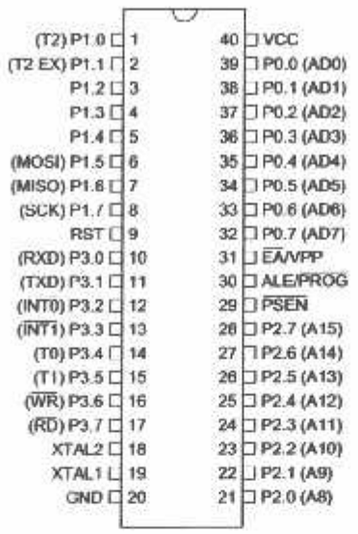
8-bit Microcontroller with 8K Bytes In-System Programmable Flash

AT89S52

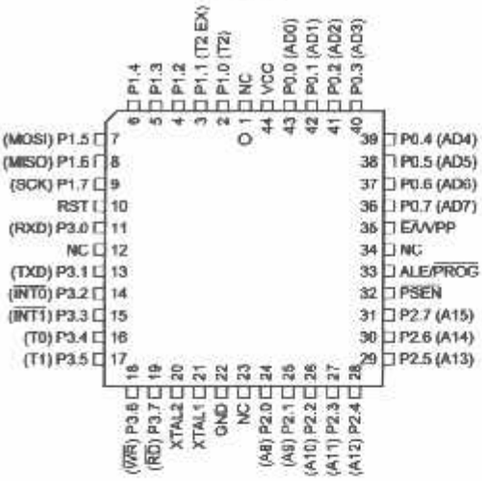
1919B–MICRO–11/03

Configurations

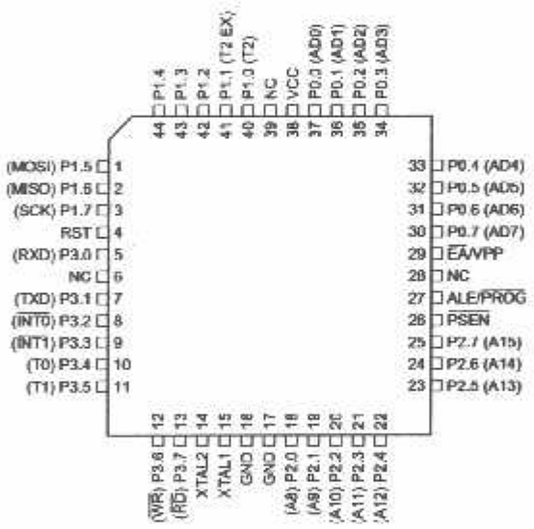
PDIP



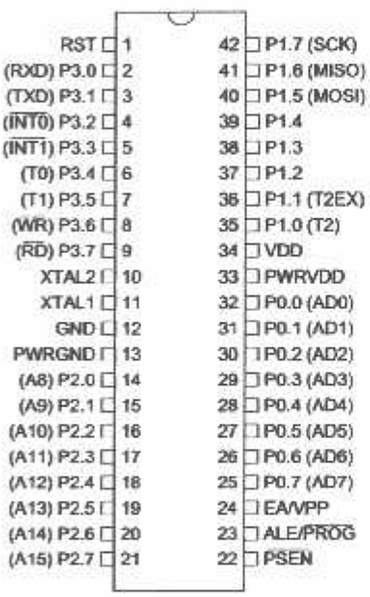
PLCC



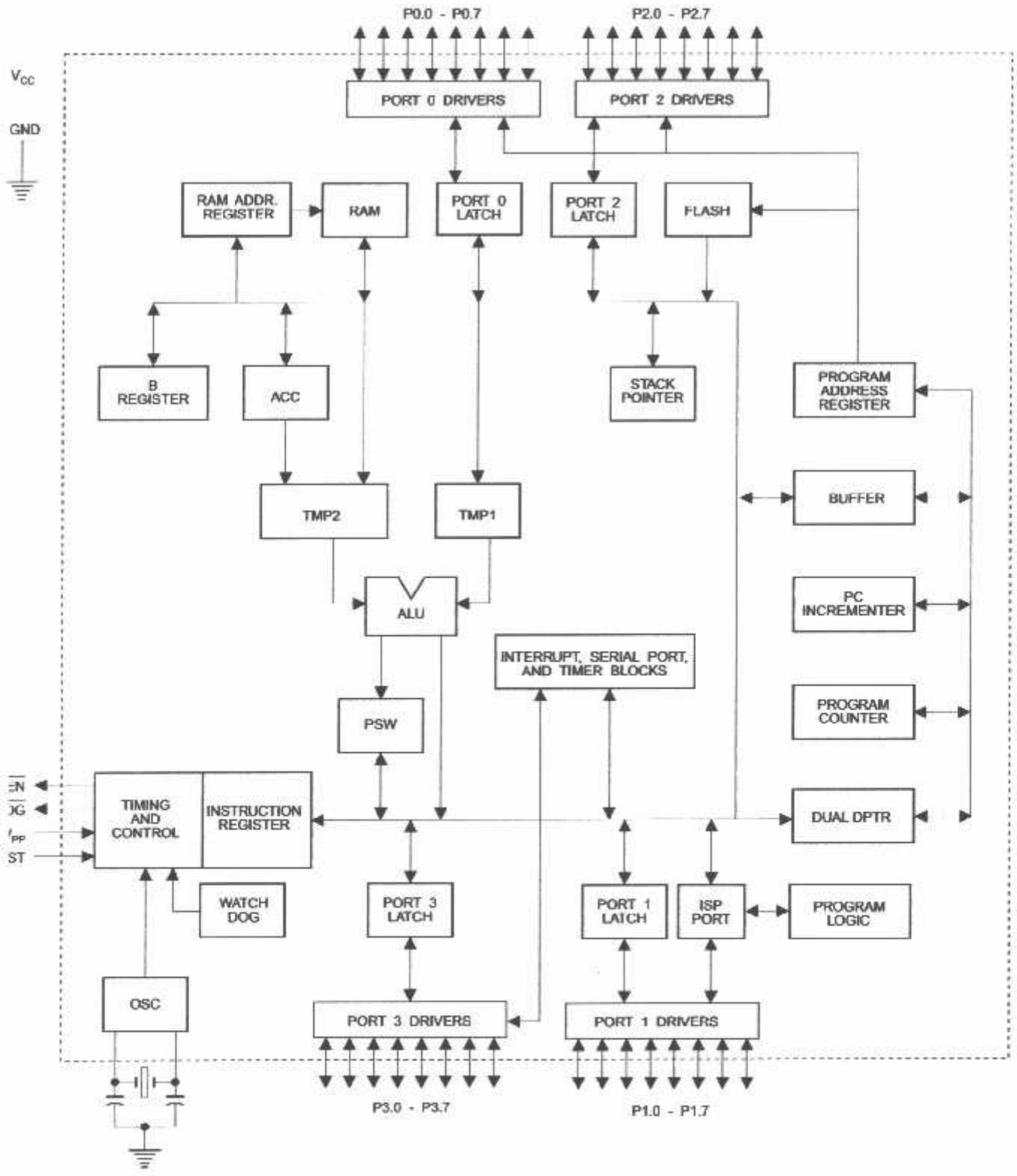
TQFP



PDIP



k Diagram


P0.0 - P0.7
P2.0 - P2.7
V_{CC}
GND
PORT 0 DRIVERS
PORT 2 DRIVERS
RAM ADDR. REGISTER
RAM
PORT 0 LATCH
PORT 2 LATCH
FLASH
B REGISTER
ACC
STACK POINTER
PROGRAM ADDRESS REGISTER
BUFFER
TMP2
TMP1
ALU
PC INCREMENTER
INTERRUPT, SERIAL PORT, AND TIMER BLOCKS
PSW
PROGRAM COUNTER
TIMING AND CONTROL
INSTRUCTION REGISTER
DUAL DPTR
WATCH DOG
PORT 3 LATCH
PORT 1 LATCH
ISP PORT
PROGRAM LOGIC
OSC
PORT 3 DRIVERS
PORT 1 DRIVERS
P3.0 - P3.7
P1.0 - P1.7

Description

Supply voltage.

Ground.

Port 0 is an 8-bit open drain bidirectional I/O port. As an output port, each pin can sink eight TTL inputs. When 1s are written to port 0 pins, the pins can be used as high-impedance inputs.

Port 0 can also be configured to be the multiplexed low-order address/data bus during accesses to external program and data memory. In this mode, P0 has internal pull-ups.

Port 0 also receives the code bytes during Flash programming and outputs the code bytes during program verification. **External pull-ups are required during program verification.**

Port 1 is an 8-bit bidirectional I/O port with internal pull-ups. The Port 1 output buffers can sink/source four TTL inputs. When 1s are written to Port 1 pins, they are pulled high by the internal pull-ups and can be used as inputs. As inputs, Port 1 pins that are externally being pulled low will source current (I_{IL}) because of the internal pull-ups.

In addition, P1.0 and P1.1 can be configured to be the timer/counter 2 external count input (P1.0/T2) and the timer/counter 2 trigger input (P1.1/T2EX), respectively, as shown in the following table.

Port 1 also receives the low-order address bytes during Flash programming and verification.

Port Pin	Alternate Functions
P1.0	T2 (external count input to Timer/Counter 2), clock-out
P1.1	T2EX (Timer/Counter 2 capture/reload trigger and direction control)
P1.5	MOSI (used for In-System Programming)
P1.6	MISO (used for In-System Programming)
P1.7	SCK (used for In-System Programming)

Port 2 is an 8-bit bidirectional I/O port with internal pull-ups. The Port 2 output buffers can sink/source four TTL inputs. When 1s are written to Port 2 pins, they are pulled high by the internal pull-ups and can be used as inputs. As inputs, Port 2 pins that are externally being pulled low will source current (I_{IL}) because of the internal pull-ups.

Port 2 emits the high-order address byte during fetches from external program memory and during accesses to external data memory that use 16-bit addresses (MOVX @ DPTR). In this application, Port 2 uses strong internal pull-ups when emitting 1s. During accesses to external data memory that use 8-bit addresses (MOVX @ RI), Port 2 emits the contents of the P2 Special Function Register.

Port 2 also receives the high-order address bits and some control signals during Flash programming and verification.

Port 3 is an 8-bit bidirectional I/O port with internal pull-ups. The Port 3 output buffers can sink/source four TTL inputs. When 1s are written to Port 3 pins, they are pulled high by the internal pull-ups and can be used as inputs. As inputs, Port 3 pins that are externally being pulled low will source current (I_{IL}) because of the pull-ups.

Port 3 receives some control signals for Flash programming and verification.

Port 3 also serves the functions of various special features of the AT89S52, as shown in the following table.

Port Pin	Alternate Functions
P3.0	RXD (serial input port)
P3.1	TXD (serial output port)
P3.2	$\overline{INT0}$ (external interrupt 0)
P3.3	$\overline{INT1}$ (external interrupt 1)
P3.4	T0 (timer 0 external input)
P3.5	T1 (timer 1 external input)
P3.6	$\overline{WR}$ (external data memory write strobe)
P3.7	$\overline{RD}$ (external data memory read strobe)

Reset input. A high on this pin for two machine cycles while the oscillator is running resets the device. This pin drives high for 98 oscillator periods after the Watchdog times out. The DISRTO bit in SFR AUXR (address 8EH) can be used to disable this feature. In the default state of bit DISRTO, the RESET HIGH out feature is enabled.

ROG

Address Latch Enable (ALE) is an output pulse for latching the low byte of the address during accesses to external memory. This pin is also the program pulse input ($\overline{PROG}$) during Flash programming.

In normal operation, ALE is emitted at a constant rate of 1/6 the oscillator frequency and may be used for external timing or clocking purposes. Note, however, that one ALE pulse is skipped during each access to external data memory.

If desired, ALE operation can be disabled by setting bit 0 of SFR location 8EH. With the bit set, ALE is active only during a MOVX or MOVC instruction. Otherwise, the pin is weakly pulled high. Setting the ALE-disable bit has no effect if the microcontroller is in external execution mode.

Program Store Enable ($\overline{PSEN}$) is the read strobe to external program memory.

When the AT89S52 is executing code from external program memory, $\overline{PSEN}$ is activated twice each machine cycle, except that two $\overline{PSEN}$ activations are skipped during each access to external data memory.

External Access Enable. $\overline{EA}$ must be strapped to GND in order to enable the device to fetch code from external program memory locations starting at 0000H up to FFFFH. Note, however, that if lock bit 1 is programmed, $\overline{EA}$ will be internally latched on reset.

$\overline{EA}$ should be strapped to V_{CC} for internal program executions.

This pin also receives the 12-volt programming enable voltage (V_{PP}) during Flash programming.

Input to the inverting oscillator amplifier and input to the internal clock operating circuit.

Output from the inverting oscillator amplifier.

cial Function sters

A map of the on-chip memory area called the Special Function Register (SFR) space is shown in Table 1.

Note that not all of the addresses are occupied, and unoccupied addresses may not be implemented on the chip. Read accesses to these addresses will in general return random data, and write accesses will have an indeterminate effect.

User software should not write 1s to these unlisted locations, since they may be used in future products to invoke new features. In that case, the reset or inactive values of the new bits will always be 0.

Timer 2 Registers: Control and status bits are contained in registers T2CON (shown in Table 2) and T2MOD (shown in Table 6) for Timer 2. The register pair (RCAP2H, RCAP2L) are the Capture/Reload registers for Timer 2 in 16-bit capture mode or 16-bit auto-reload mode.

Interrupt Registers: The individual interrupt enable bits are in the IE register. Two priorities can be set for each of the six interrupt sources in the IP register.

l. AT89S52 SFR Map and Reset Values

								0FFH
B 00000000								0F7H
								0EFH
ACC 00000000								0E7H
								0DFH
PSW 00000000								0D7H
T2CON 00000000	T2MOD XXXXXX00	RCAP2L 00000000	RCAP2H 00000000	TL2 00000000	TH2 00000000			0CFH
								0C7H
IP XX000000								0BFH
P3 11111111								0B7H
IE 0X000000								0AFH
P2 11111111		AUXR1 XXXXXXX0				WDTRST XXXXXXXX		0A7H
SCON 00000000	SBUF XXXXXXXX							9FH
P1 11111111								97H
TCON 00000000	TMOD 00000000	TL0 00000000	TL1 00000000	TH0 00000000	TH1 00000000	AUXR XXX00XX0		8FH
P0 11111111	SP 00000111	DP0L 00000000	DP0H 00000000	DP1L 00000000	DP1H 00000000		PCON 0XXX0000	87H

2. T2CON – Timer/Counter 2 Control Register

2CON Address = 0C8H — Reset Value = 0000 0000B

it Addressable

it	TF2	EXF2	RCLK	TCLK	EXEN2	TR2	C/$\overline{T2}$	CP/$\overline{RL2}$
	7	6	5	4	3	2	1	0

ol	Function
	Timer 2 overflow flag set by a Timer 2 overflow and must be cleared by software. TF2 will not be set when either RCLK = 1 or TCLK = 1.
	Timer 2 external flag set when either a capture or reload is caused by a negative transition on T2EX and EXEN2 = 1. When Timer 2 interrupt is enabled, EXF2 = 1 will cause the CPU to vector to the Timer 2 interrupt routine. EXF2 must be cleared by software. EXF2 does not cause an interrupt in up/down counter mode (DCEN = 1).
	Receive clock enable. When set, causes the serial port to use Timer 2 overflow pulses for its receive clock in serial port Modes 1 and 3. RCLK = 0 causes Timer 1 overflow to be used for the receive clock.
	Transmit clock enable. When set, causes the serial port to use Timer 2 overflow pulses for its transmit clock in serial port Modes 1 and 3. TCLK = 0 causes Timer 1 overflows to be used for the transmit clock.
2	Timer 2 external enable. When set, allows a capture or reload to occur as a result of a negative transition on T2EX if Timer 2 is not being used to clock the serial port. EXEN2 = 0 causes Timer 2 to ignore events at T2EX.
	Start/Stop control for Timer 2. TR2 = 1 starts the timer.
	Timer or counter select for Timer 2. C/$\overline{T2}$ = 0 for timer function. C/$\overline{T2}$ = 1 for external event counter (falling edge triggered).
$\overline{2}$	Capture/Reload select. CP/$\overline{RL2}$ = 1 causes captures to occur on negative transitions at T2EX if EXEN2 = 1. CP/$\overline{RL2}$ = 0 causes automatic reloads to occur when Timer 2 overflows or negative transitions occur at T2EX when EXEN2 = 1. When either RCLK or TCLK = 1, this bit is ignored and the timer is forced to auto-reload on Timer 2 overflow.

3. AUXR: Auxiliary Register

Address = 8EH — Reset Value = XXX00XX0B

Not Bit Addressable

	–	–	–	WDIDLE	DISRTO	–	–	DISALE
Bit	7	6	5	4	3	2	1	0

Reserved for future expansion

E Disable/Enable ALE

DISALE	Operating Mode
0	ALE is emitted at a constant rate of 1/6 the oscillator frequency
1	ALE is active only during a MOVX or MOVC instruction

O Disable/Enable Reset out

DISRTO	
0	Reset pin is driven High after WDT times out
1	Reset pin is input only

E Disable/Enable WDT in IDLE mode

WDIDLE	
0	WDT continues to count in IDLE mode
1	WDT halts counting in IDLE mode

ata Pointer Registers: To facilitate accessing both internal and external data memory, two banks of 16-bit Data Registers are provided: DP0 at SFR address locations 82H-83H and DP1 at 84H-85H. Bit DPS = 0 in SFR AUXR1 DP0 and DPS = 1 selects DP1. The user should **ALWAYS** initialize the DPS bit to the appropriate value before ng the respective Data Pointer Register.

Off Flag: The Power Off Flag (POF) is located at bit 4 (PCON.4) in the PCON SFR. POF is set to "1" during power n be set and rest under software control and is not affected by reset.

. AUXR1: Auxiliary Register 1

Address = A2H — Reset Value = XXXXXXX0B

Not Bit Addressable

	–	–	–	–	–	–	–	DPS
Bit	7	6	5	4	3	2	1	0

Reserved for future expansion

Data Pointer Register Select

DPS	
0	Selects DPTR Registers DP0L, DP0H
1	Selects DPTR Registers DP1L, DP1H

ıory Organization

MCS-51 devices have a separate address space for Program and Data Memory. Up to 64K bytes each of external Program and Data Memory can be addressed.

·am Memory

If the $\overline{EA}$ pin is connected to GND, all program fetches are directed to external memory.

On the AT89S52, if $\overline{EA}$ is connected to V_{CC}, program fetches to addresses 0000H through 1FFFH are directed to internal memory and fetches to addresses 2000H through FFFFH are to external memory.

Memory

The AT89S52 implements 256 bytes of on-chip RAM. The upper 128 bytes occupy a parallel address space to the Special Function Registers. This means that the upper 128 bytes have the same addresses as the SFR space but are physically separate from SFR space.

When an instruction accesses an internal location above address 7FH, the address mode used in the instruction specifies whether the CPU accesses the upper 128 bytes of RAM or the SFR space. Instructions which use direct addressing access the SFR space.

For example, the following direct addressing instruction accesses the SFR at location 0A0H (which is P2).

```
MOV 0A0H, #data
```

Instructions that use indirect addressing access the upper 128 bytes of RAM. For example, the following indirect addressing instruction, where R0 contains 0A0H, accesses the data byte at address 0A0H, rather than P2 (whose address is 0A0H).

```
MOV @R0, #data
```

Note that stack operations are examples of indirect addressing, so the upper 128 bytes of data RAM are available as stack space.

hdog Timer ·time Enabled Reset-out)

The WDT is intended as a recovery method in situations where the CPU may be subjected to software upsets. The WDT consists of a 14-bit counter and the Watchdog Timer Reset (WDTRST) SFR. The WDT is defaulted to disable from exiting reset. To enable the WDT, a user must write 01EH and 0E1H in sequence to the WDTRST register (SFR location 0A6H). When the WDT is enabled, it will increment every machine cycle while the oscillator is running. The WDT timeout period is dependent on the external clock frequency. There is no way to disable the WDT except through reset (either hardware reset or WDT overflow reset). When WDT overflows, it will drive an output RESET HIGH pulse at the RST pin.

ı the WDT

To enable the WDT, a user must write 01EH and 0E1H in sequence to the WDTRST register (SFR location 0A6H). When the WDT is enabled, the user needs to service it by writing 01EH and 0E1H to WDTRST to avoid a WDT overflow. The 14-bit counter overflows when it reaches 16383 (3FFFH), and this will reset the device. When the WDT is enabled, it will increment every machine cycle while the oscillator is running. This means the user must reset the WDT at least every 16383 machine cycles. To reset the WDT the user must write 01EH and 0E1H to WDTRST. WDTRST is a write-only register. The WDT counter cannot be read or written. When WDT overflows, it will generate an output RESET pulse at the RST pin. The RESET pulse duration is 98xTOSC, where TOSC = 1/FOSC. To make the best use of the WDT, it should be serviced in those sections of code that will periodically be executed within the time required to prevent a WDT reset.

· During Power-n and Idle

In Power-down mode the oscillator stops, which means the WDT also stops. While in Power-down mode, the user does not need to service the WDT. There are two methods of exiting Power-down mode: by a hardware reset or via a level-activated external interrupt which is enabled prior to entering Power-down mode. When Power-down is exited with hardware reset, servicing the WDT should occur as it normally does whenever the AT89S52 is reset. Exiting Power-down with an interrupt is significantly different. The interrupt is held low long enough for the oscillator to stabilize. When the interrupt is brought high, the interrupt is serviced. To prevent the WDT from resetting the device while the interrupt pin is held low, the WDT is not started until the interrupt is pulled high. It is suggested that the WDT be reset during the interrupt service for the interrupt used to exit Power-down mode.

To ensure that the WDT does not overflow within a few states of exiting Power-down, it is best to reset the WDT just before entering Power-down mode.

Before going into the IDLE mode, the WDIDLE bit in SFR AUXR is used to determine whether the WDT continues to count if enabled. The WDT keeps counting during IDLE (WDIDLE bit = 0) as the default state. To prevent the WDT from resetting the AT89S52 while in IDLE mode, the user should always set up a timer that will periodically exit IDLE, service the WDT, and reenter IDLE mode.

With WDIDLE bit enabled, the WDT will stop to count in IDLE mode and resumes the count upon exit from IDLE.

r

The UART in the AT89S52 operates the same way as the UART in the AT89C51 and AT89C52. For further information on the UART operation, refer to the ATMEL Web site (http://www.atmel.com). From the home page, select "Products", then "8051-Architecture Flash Microcontroller", then "Product Overview".

r 0 and 1

Timer 0 and Timer 1 in the AT89S52 operate the same way as Timer 0 and Timer 1 in the AT89C51 and AT89C52. For further information on the timers' operation, refer to the ATMEL Web site (http://www.atmel.com). From the home page, select "Products", then "8051-Architecture Flash Microcontroller", then "Product Overview".

· 2

Timer 2 is a 16-bit Timer/Counter that can operate as either a timer or an event counter. The type of operation is selected by bit C/$\overline{T2}$ in the SFR T2CON (shown in Table 2). Timer 2 has three operating modes: capture, auto-reload (up or down counting), and baud rate generator. The modes are selected by bits in T2CON, as shown in Table 5. Timer 2 consists of two 8-bit registers, TH2 and TL2. In the Timer function, the TL2 register is incremented every machine cycle. Since a machine cycle consists of 12 oscillator periods, the count rate is 1/12 of the oscillator frequency.

Table 5. Timer 2 Operating Modes

RCLK +TCLK	CP/$\overline{RL2}$	TR2	MODE
0	0	1	16-bit Auto-reload
0	1	1	16-bit Capture
1	X	1	Baud Rate Generator
X	X	0	(Off)

In the Counter function, the register is incremented in response to a 1-to-0 transition at its corresponding external input pin, T2. In this function, the external input is sampled during S5P2 of every machine cycle. When the samples show a high in one cycle and a low in the next cycle, the count is incremented. The new count value appears in the register during S3P1 of the cycle following the one in which the transition was detected. Since two machine cycles (24 oscillator periods) are required to recognize a 1-to-0 transition, the maximum count rate s 1/24 of the oscillator frequency. To ensure that a given level is sampled at least once before it changes, the level should be held for at least one full machine cycle.

pture Mode

In the capture mode, two options are selected by bit EXEN2 in T2CON. If EXEN2 = 0, Timer 2 is a 16-bit timer or counter which upon overflow sets bit TF2 in T2CON. This bit can then be used to generate an interrupt. If EXEN2 = 1, Timer 2 performs the same operation, but a 1-to-0 transition at external input T2EX also causes the current value in TH2 and TL2 to be captured into RCAP2H and RCAP2L, respectively. In addition, the transition at T2EX causes bit EXF2 in T2CON to be set. The EXF2 bit, like TF2, can generate an interrupt. The capture mode is illustrated in Figure 1.

to-reload (Up or Down unter)

Timer 2 can be programmed to count up or down when configured in its 16-bit auto-reload mode. This feature is invoked by the DCEN (Down Counter Enable) bit located in the SFR T2MOD (see Table 6). Upon reset, the DCEN bit is set to 0 so that timer 2 will default to count up. When DCEN is set, Timer 2 can count up or down, depending on the value of the T2EX pin.

ıre 1. Timer in Capture Mode

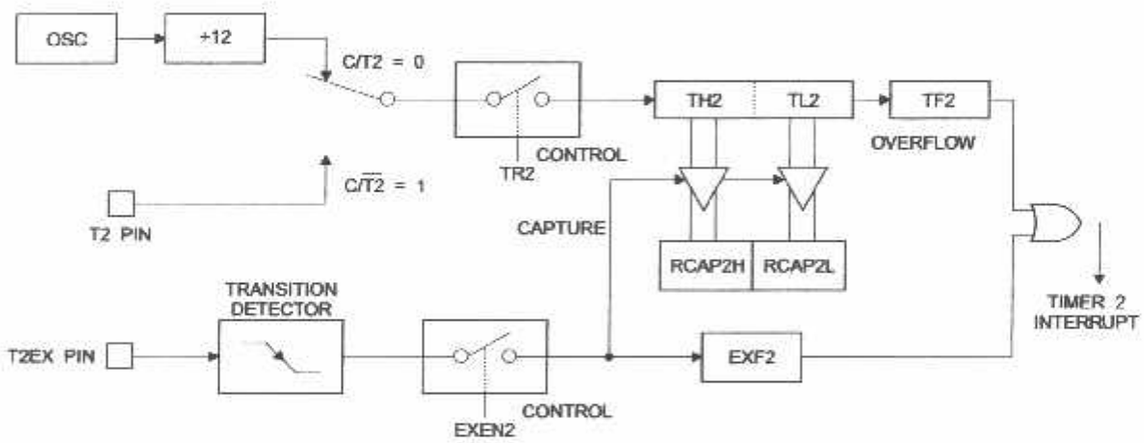


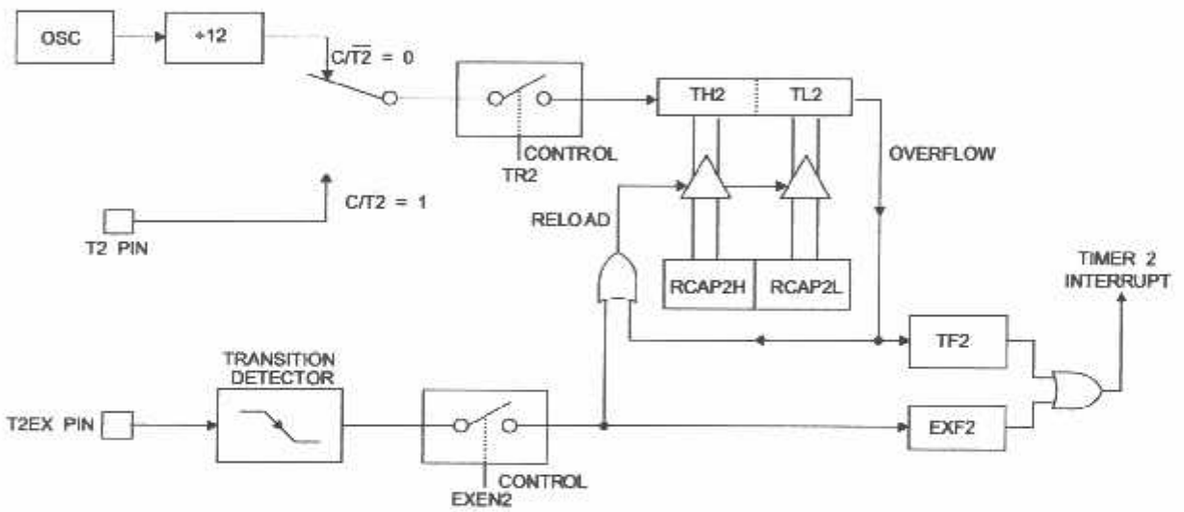
Figure 2 shows Timer 2 automatically counting up when DCEN = 0. In this mode, two options are selected by bit EXEN2 in T2CON. If EXEN2 = 0, Timer 2 counts up to 0FFFFH and then sets the TF2 bit upon overflow. The overflow also causes the timer registers to be reloaded with the 16-bit value in RCAP2H and RCAP2L. The values in Timer in Capture ModeRCAP2H and RCAP2L are preset by software. If EXEN2 = 1, a 16-bit reload can be triggered either by an overflow or by a 1-to-0 transition at external input T2EX. This transition also sets the EXF2 bit. Both the TF2 and EXF2 bits can generate an interrupt if enabled.

Setting the DCEN bit enables T mer 2 to count up or down, as shown in Figure 2. In this mode, the T2EX pin controls the direction of the count. A logic 1 at T2EX makes Timer 2 count up. The timer will overflow at 0FFFFH and set the TF2 bit. This overflow also causes the 16-bit value in RCAP2H and RCAP2L to be reloaded into the timer registers, TH2 and TL2, respectively.

A logic 0 at T2EX makes Timer 2 count down. The timer underflows when TH2 and TL2 equal the values stored in RCAP2H and RCAP2L. The underflow sets the TF2 bit and causes 0FFFFH to be reloaded into the timer registers.

The EXF2 bit toggles whenever Timer 2 overflows or underflows and can be used as a 17th bit of resolution. In this operating mode, EXF2 does not flag an interrupt.

ıre 2. Timer 2 Auto Reload Mode (DCEN = 0)



ıle 6. T2MOD – Timer 2 Mode Control Register

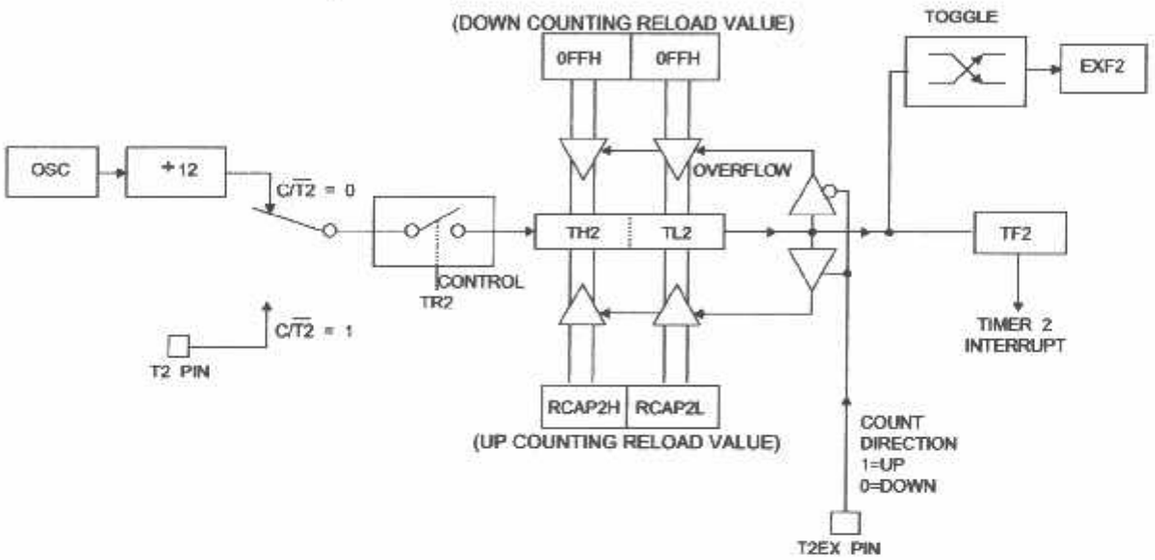
T2MOD Address = 0C9H — Reset Value = XXXX XX00B

Not Bit Addressable

	–	–	–	–	–	–	T2OE	DCEN
Bit	7	6	5	4	3	2	1	0

mbol	Function
	Not implemented, reserved for future
OE	Timer 2 Output Enable bit
:EN	When set, this bit allows Timer 2 to be configured as an up/down counter

ıre 3. Timer 2 Auto Reload Mode (DCEN = 1)



ıud Rate Generator

Timer 2 is selected as the baud rate generator by setting TCLK and/or RCLK in T2CON (Table 2). Note that the baud rates for transmit and receive can be different if Timer 2 is used for the receiver or transmitter and Timer 1 is used for the other function. Setting RCLK and/or TCLK puts Timer 2 into its baud rate generator mode, as shown in Figure 4.

The baud rate generator mode is similar to the auto-reload mode, in that a rollover in TH2 causes the Timer 2 registers to be reloaded with the 16-bit value in registers RCAP2H and RCAP2L, which are preset by software.

The baud rates in Modes 1 and 3 are determined by Timer 2's overflow rate according to the following equation.

$$\text{Modes 1 and 3 Baud Rates} = \frac{\text{Timer 2 Overflow Rate}}{16}$$

The Timer can be configured for either timer or counter operation. In most applications, it is configured for timer operation ($CP/\overline{T2} = 0$). The timer operation is different for Timer 2 when it is used as a baud rate generator. Normally, as a timer, it increments every machine cycle (at 1/12 the oscillator frequency). As a baud rate generator, however, it increments every state time (at 1/2 the oscillator frequency). The baud rate formula is given below.

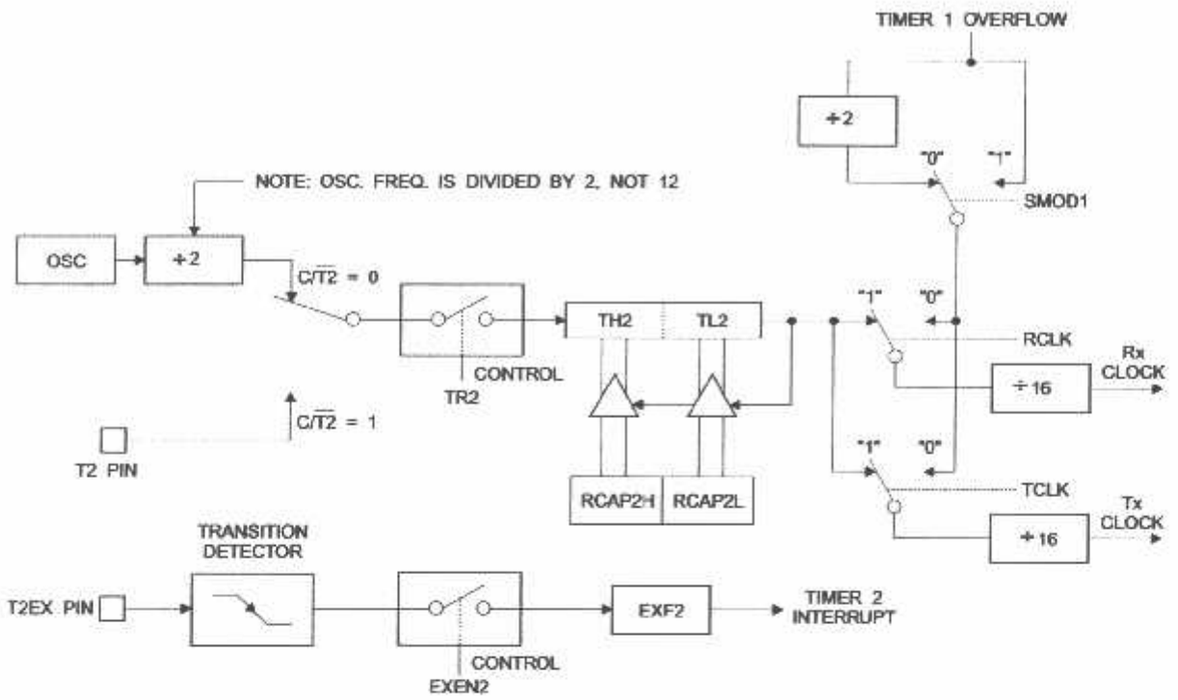
$$\frac{\text{Modes 1 and 3}}{\text{Baud Rate}} = \frac{\text{Oscillator Frequency}}{32 \times [65536\text{-RCAP2H,RCAP2L})]}$$

where (RCAP2H, RCAP2L) is the content of RCAP2H and RCAP2L taken as a 16-bit unsigned integer.

Timer 2 as a baud rate generator is shown in Figure 4. This figure is valid only if RCLK or TCLK = 1 in T2CON. Note that a rollover in TH2 does not set TF2 and will not generate an interrupt. Note too, that if EXEN2 is set, a 1-to-0 transition in T2EX will set EXF2 but will not cause a reload from (RCAP2H, RCAP2L) to (TH2, TL2). Thus, when Timer 2 is in use as a baud rate generator, T2EX can be used as an extra external interrupt.

Note that when Timer 2 is running (TR2 = 1) as a timer in the baud rate generator mode, TH2 or TL2 should not be read from or written to. Under these conditions, the Timer is incremented every state time, and the results of a read or write may not be accurate. The RCAP2 registers may be read but should not be written to, because a write might overlap a reload and cause write and/or reload errors. The timer should be turned off (clear TR2) before accessing the Timer 2 or RCAP2 registers.

ure 4. Timer 2 in Baud Rate Generator Mode



ıgrammable ıck Out

A 50% duty cycle clock can be programmed to come out on P1.0, as shown in Figure 5. This pin, besides being a regular I/O pin, has two alternate functions. It can be programmed to input the external clock for Timer/Counter 2 or to output a 50% duty cycle clock ranging from 61 Hz to 4 MHz (for a 16-MHz operating frequency).

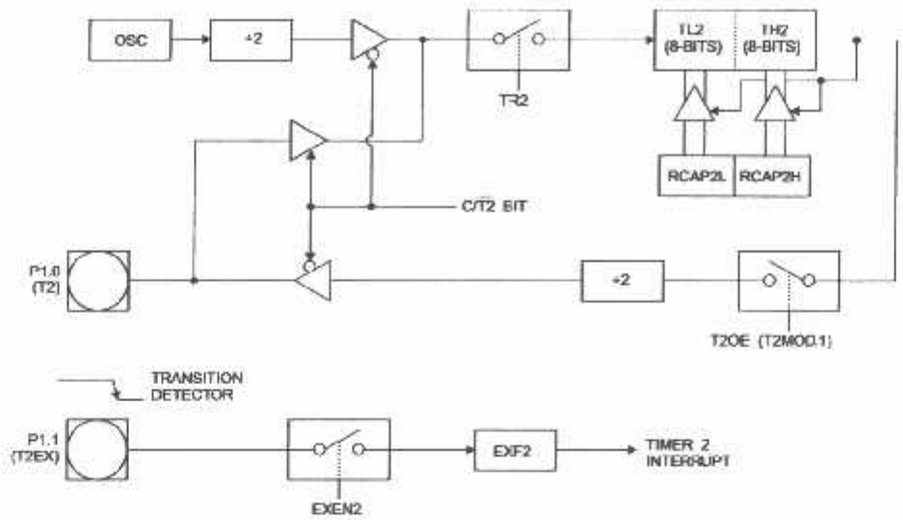
To configure the Timer/Counter 2 as a clock generator, bit C/$\overline{T2}$ (T2CON.1) must be cleared and bit T2OE (T2MOD.1) must be set. Bit TR2 (T2CON.2) starts and stops the timer.

The clock-out frequency depends on the oscillator frequency and the reload value of Timer 2 capture registers (RCAP2H, RCAP2L), as shown in the following equation.

$$\text{Clock-Out Frequency} = \frac{\text{Oscillator Frequency}}{4 \times [65536-(\text{RCAP2H,RCAP2L})]}$$

In the clock-out mode, Timer 2 roll-overs will not generate an interrupt. This behavior is similar to when Timer 2 is used as a baud-rate generator. It is possible to use Timer 2 as a baud-rate generator and a clock generator simultaneously. Note, however, that the baud-rate and clock-out frequencies cannot be determined independently from one another since they both use RCAP2H and RCAP2L.

ure 5. Timer 2 in Clock-Out Mode



errupts

The AT89S52 has a total of six interrupt vectors: two external interrupts ($\overline{INT0}$ and $\overline{INT1}$), three timer interrupts (Timers 0, 1, and 2), and the serial port interrupt. These interrupts are all shown in Figure 6.

Each of these interrupt sources can be individually enabled or disabled by setting or clearing a bit in Special Function Register IE. IE also contains a global disable bit, EA, which disables all interrupts at once.

Note that Table 5 shows that bit position IE.6 is unimplemented. User software should not write a 1 to this bit position, since it may be used in future AT89 products.

Timer 2 interrupt is generated by the logical OR of bits TF2 and EXF2 in register T2CON. Neither of these flags is cleared by hardware when the service routine is vectored to. In fact, the service routine may have to determine whether it was TF2 or EXF2 that generated the interrupt, and that bit will have to be cleared in software.

The Timer 0 and Timer 1 flags, TF0 and TF1, are set at S5P2 of the cycle in which the timers overflow. The values are then polled by the circuitry in the next cycle. However, the Timer 2 flag, TF2, is set at S2P2 and is polled in the same cycle in which the timer overflows.

ıle 7. Interrupt Enable (IE) Register

(MSB) (LSB)

EA	–	ET2	ES	ET1	EX1	ET0	EX0

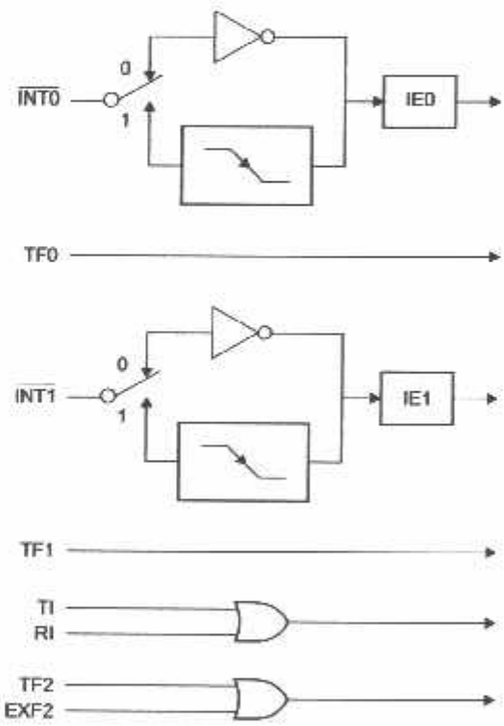
Enable Bit = 1 enables the interrupt.

Enable Bit = 0 disables the interrupt.

mbol	Position	Function
	IE.7	Disables all interrupts. If EA = 0, no interrupt is acknowledged. If EA = 1, each interrupt source is individually enabled or disabled by setting or clearing its enable bit.
	IE.6	Reserved.
2	IE.5	Timer 2 interrupt enable bit.
	IE.4	Serial Port interrupt enable bit.
1	IE.3	Timer 1 interrupt enable bit.
1	IE.2	External interrupt 1 enable bit.
0	IE.1	Timer 0 interrupt enable bit.
0	IE.0	External interrupt 0 enable bit.

er software should never write 1s to reserved bits, because they may be used in future AT89 products.

ıre 6. Interrupt Sources



ıcillator ıaracteristics

XTAL1 and XTAL2 are the input and output, respectively, of an inverting amplifier that can be configured for use as an on-chip oscillator, as shown in Figure 7. Either a quartz crystal or ceramic resonator may be used. To drive the device from an external clock source, XTAL2 should be left unconnected while XTAL1 is driven, as shown in Figure 8. There are no requirements on the duty cycle of the external clock signal, since the input to the internal clocking circuitry is through a divide-by-two flip-flop, but minimum and maximum voltage high and low time specifications must be observed.

e Mode

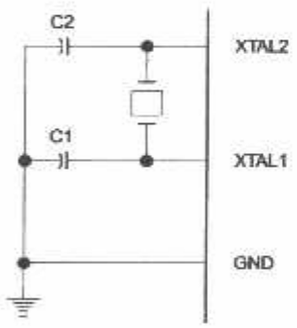
In idle mode, the CPU puts itself to sleep while all the on-chip peripherals remain active. The mode is invoked by software. The content of the on-chip RAM and all the special functions registers remain unchanged during this mode. The idle mode can be terminated by any enabled interrupt or by a hardware reset.

Note that when idle mode is terminated by a hardware reset, the device normally resumes program execution from where it left off, up to two machine cycles before the internal reset algorithm takes control. On-chip hardware inhibits access to internal RAM in this event, but access to the port pins is not inhibited. To eliminate the possibility of an unexpected write to a port pin when idle mode is terminated by a reset, the instruction following the one that invokes idle mode should not write to a port pin or to external memory.

wer-down Mode

In the Power-down mode, the oscillator is stopped, and the instruction that invokes Power-down is the last instruction executed. The on-chip RAM and Special Function Registers retain their values until the Power-down mode is terminated. Exit from Power-down mode can be initiated either by a hardware reset or by an enabled external interrupt. Reset redefines the SFRs but does not change the on-chip RAM. The reset should not be activated before V_{CC} is restored to its normal operating level and must be held active long enough to allow the oscillator to restart and stabilize.

Figure 7. Oscillator Connections



Note: 1. C1, C2 = 30 pF ± 10 pF for Crystals
= 40 pF ± 10 pF for Ceramic Resonators

Figure 8. External Clock Drive Configuration

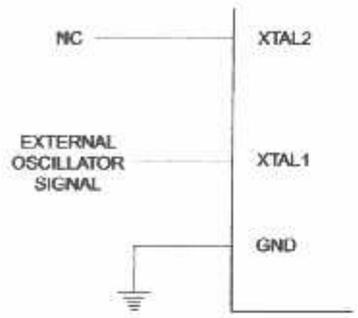


Table 8. Status of External Pins During Idle and Power-down Modes

Mode	Program Memory	ALE	$\overline{PSEN}$	PORT0	PORT1	PORT2	PORT3
Idle	Internal	1	1	Data	Data	Data	Data
Idle	External	1	1	Float	Data	Address	Data
Power-down	Internal	0	0	Data	Data	Data	Data
Power-down	External	0	0	Float	Data	Data	Data

ıgram Memory :k Bits

The AT89S52 has three lock bits that can be left unprogrammed (U) or can be programmed (P) to obtain the additional features listed in the following table.

Table 9. Lock Bit Protection Modes

Program Lock Bits				
	LB1	LB2	LB3	Protection Type
1	U	U	U	No program lock features
2	P	U	U	MOVC instructions executed from external program memory are disabled from fetching code bytes from internal memory, $\overline{EA}$ is sampled and latched on reset, and further programming of the Flash memory is disabled
3	P	P	U	Same as mode 2, but verify is also disabled
4	P	P	P	Same as mode 3, but external execution is also disabled

When lock bit 1 is programmed, the logic level at the $\overline{EA}$ pin is sampled and latched during reset. If the device is powered up without a reset, the latch initializes to a random value and holds that value until reset is activated. The latched value of $\overline{EA}$ must agree with the current logic level at that pin in order for the device to function properly.

ogramming the ash – Parallel Mode

The AT89S52 is shipped with the on-chip Flash memory array ready to be programmed. The programming interface needs a high-voltage (12-volt) program enable signal and is compatible with conventional third-party Flash or EPROM programmers.

The AT89S52 code memory array is programmed byte-by-byte.

Programming Algorithm: Before programming the AT89S52, the address, data, and control signals should be set up according to the Flash programming mode table and Figures 13 and 14. To program the AT89S52, take the following steps:

1. Input the desired memory location on the address lines.
2. Input the appropriate data byte on the data lines.
3. Activate the correct combination of control signals.
4. Raise $\overline{EA}/V_{PP}$ to 12V.
5. Pulse ALE/$\overline{PROG}$ once to program a byte in the Flash array or the lock bits. The byte-write cycle is self-timed and typically takes no more than 50 µs. Repeat steps 1 through 5, changing the address and data for the entire array or until the end of the object file is reached.

$\overline{Data}$ Polling: The AT89S52 features $\overline{Data}$ Polling to indicate the end of a byte write cycle. During a write cycle, an attempted read of the last byte written will result in the complement of the written data on P0.7. Once the write cycle has been completed, true data is valid on all outputs, and the next cycle may begin. $\overline{Data}$ Polling may begin any time after a write cycle has been initiated.

Ready/$\overline{Busy}$: The progress of byte programming can also be monitored by the RDY/$\overline{BSY}$ output signal. P3.0 is pulled low after ALE goes high during programming to indicate $\overline{BUSY}$. P3.0 is pulled high again when programming is done to indicate READY.

Program Verify: If lock bits LB1 and LB2 have not been programmed, the programmed code data can be read back via the address and data lines for verification. The status of the individual lock bits can be verified directly by reading them back.

Reading the Signature Bytes: The signature bytes are read by the same procedure as a normal verification of locations 000H, 100H, and 200H, except that P3.6 and P3.7 must be pulled to a logic low. The values returned are as follows.

(000H) = 1EH indicates manufactured by Atmel
(100H) = 52H indicates AT89S52
(200H) = 06H

Chip Erase: In the parallel programming mode, a chip erase operation is initiated by using the proper combination of control signals and by pulsing ALE/$\overline{PROG}$ low for a duration of 200 ns - 500 ns.

In the serial programming mode, a chip erase operation is initiated by issuing the Chip Erase instruction. In this mode, chip erase is self-timed and takes about 500 ms.

During chip erase, a serial read from any address location will return 00H at the data output.

ogramming the ash – Serial Mode

The Code memory array can be programmed using the serial ISP interface while RST is pulled to V_{CC}. The serial interface consists of pins SCK, MOSI (input) and MISO (output). After RST is set high, the Programming Enable instruction needs to be executed first before other operations can be executed. Before a reprogramming sequence can occur, a Chip Erase operation is required.

The Chip Erase operation turns the content of every memory location in the Code array into FFH.

Either an external system clock can be supplied at pin XTAL1 or a crystal needs to be connected across pins XTAL1 and XTAL2. The maximum serial clock (SCK) frequency should be less than 1/16 of the crystal frequency. With a 33 MHz oscillator clock, the maximum SCK frequency is 2 MHz.

·ial Programming ıorithm

To program and verify the AT89S52 in the serial programming mode, the following sequence is recommended:

1. Power-up sequence:
   Apply power between VCC and GND pins.
   Set RST pin to "H".
   If a crystal is not connected across pins XTAL1 and XTAL2, apply a 3 MHz to 33 MHz clock to XTAL1 pin and wait for at least 10 milliseconds.
2. Enable serial programming by sending the Programming Enable serial instruction to pin MOSI/P1.5. The frequency of the shift clock supplied at pin SCK/P1.7 needs to be less than the CPU clock at XTAL1 divided by 16.
3. The Code array is programmed one byte at a time in either the Byte or Page mode. The write cycle is self-timed and typically takes less than 0.5 ms at 5V.
4. Any memory location can be verified by using the Read instruction which returns the content at the selected address at serial output MISO/P1.6.
5. At the end of a programming session, RST can be set low to commence normal device operation.

Power-off sequence (if needed):
Set XTAL1 to "L" (if a crystal is not used).
Set RST to "L".
Turn V_{CC} power off.

Data Polling: The Data Polling feature is also available in the serial mode. In this mode, during a write cycle an attempted read of the last byte written will result in the complement of the MSB of the serial output byte on MISO.

ırial Programming ıstruction Set

The Instruction Set for Serial Programming follows a 4-byte protocol and is shown in Table 11.

ɔgramming erface – Parallel ɔde

Every code byte in the Flash array can be programmed by using the appropriate combination of control signals. The write operation cycle is self-timed and once initiated, will automatically time itself to completion.

Most worldwide major programming vendors offer support for the Atmel AT89 microcontroller series. Please contact your local programming vendor for the appropriate software revision.

le 10. Flash Programming Modes

de	V_{CC}	RST	$\overline{PSEN}$	ALE/ $\overline{PROG}$	$\overline{EA}$/ V_{PP}	P2.6	P2.7	P3.3	P3.6	P3.7	P0.7-0 Data	P2.4-0 Address	P1.7-0 Address
te Code Data	5V	H	L	(2)	12V	L	H	H	H	H	D_{IN}	A12-8	A7-0
ıd Code Data	5V	H	L	H	H	L	L	L	H	H	D_{OUT}	A12-8	A7-0
te Lock Bit 1	5V	H	L	(3)	12V	H	H	H	H	H	X	X	X
te Lock Bit 2	5V	H	L	(3)	12V	H	H	H	L	L	X	X	X
le Lock Bit 3	5V	H	L	(3)	12V	H	L	H	H	L	X	X	X
ıd Lock Bits .3	5V	H	L	H	H	H	H	L	H	L	P0.2, P0.3, P0.4	X	X
ı Erase	5V	H	L	(1)	12V	H	L	H	L	L	X	X	X
d Atmel ID	5V	H	L	H	H	L	L	L	L	L	1EH	X 0000	00H
ı Device ID	5V	H	L	H	H	L	L	L	L	L	52H	X 0001	00H
ı Device ID	5V	H	L	H	H	L	L	L	L	L	06H	X 0010	00H

1. Each $\overline{PROG}$ pulse is 200 ns - 500 ns for Chip Erase.
2. Each $\overline{PROG}$ pulse is 200 ns - 500 ns for Write Code Data.
3. Each $\overline{PROG}$ pulse is 200 ns - 500 ns for Write Lock Bits.
4. RDY/$\overline{BSY}$ signal is output on P3.0 during programming.
5. X = don't care.

Figure 9. Programming the Flash Memory (Parallel Mode)

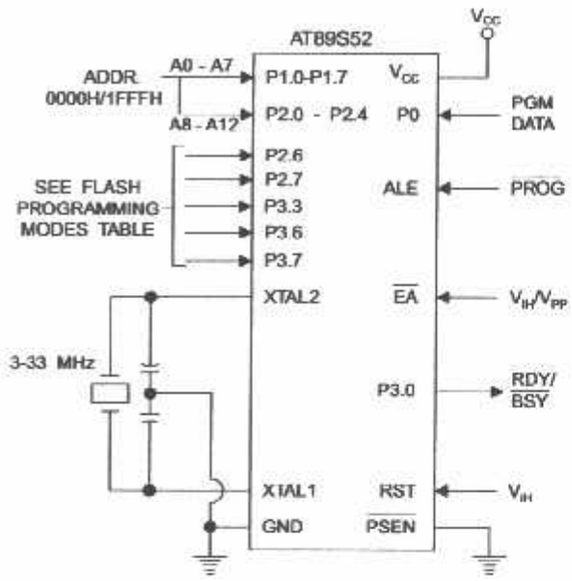
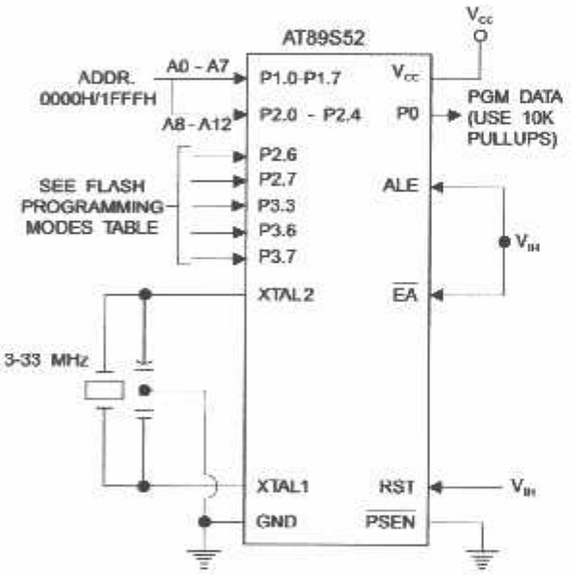


Figure 10. Verifying the Flash Memory (Parallel Mode)



ash Programming and Verification Characteristics (Parallel Mode)

= 20°C to 30°C, V_{CC} = 4.5 to 5.5V

mbol	Parameter	Min	Max	Units
P	Programming Supply Voltage	11.5	12.5	V
	Programming Supply Current		10	mA
	V_{CC} Supply Current		30	mA
CLCL	Oscillator Frequency	3	33	MHz
SL	Address Setup to $\overline{PROG}$ Low	$48t_{CLCL}$		
AX	Address Hold After $\overline{PROG}$	$48t_{CLCL}$		
SL	Data Setup to $\overline{PROG}$ Low	$48t_{CLCL}$		
DX	Data Hold After $\overline{PROG}$	$48t_{CLCL}$		
SH	P2.7 ($\overline{ENABLE}$) High to V_{PP}	$48t_{CLCL}$		
SL	V_{PP} Setup to $\overline{PROG}$ Low	10		µs
SL	V_{PP} Hold After $\overline{PROG}$	10		µs
GH	$\overline{PROG}$ Width	0.2	1	µs
AV	Address to Data Valid		$48t_{CLCL}$	
LV	$\overline{ENABLE}$ Low to Data Valid		$48t_{CLCL}$	
AZ	Data Float After $\overline{ENABLE}$	0	$48t_{CLCL}$	
SL	PROG High to BUSY Low		1.0	µs
	Byte Write Cycle Time		50	µs

re 11. Flash Programming and Verification Waveforms – Parallel Mode

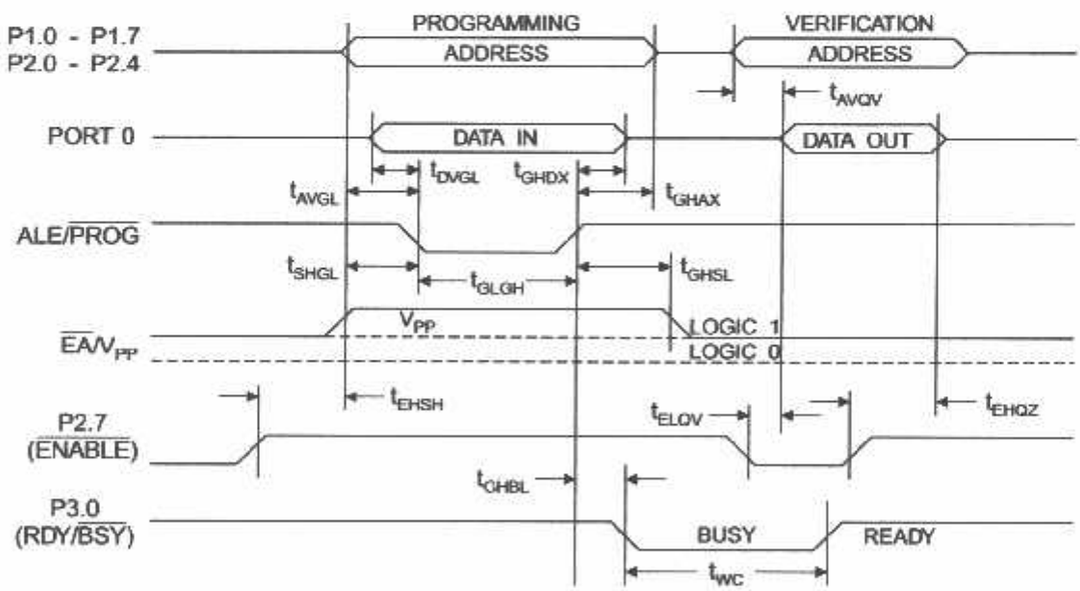
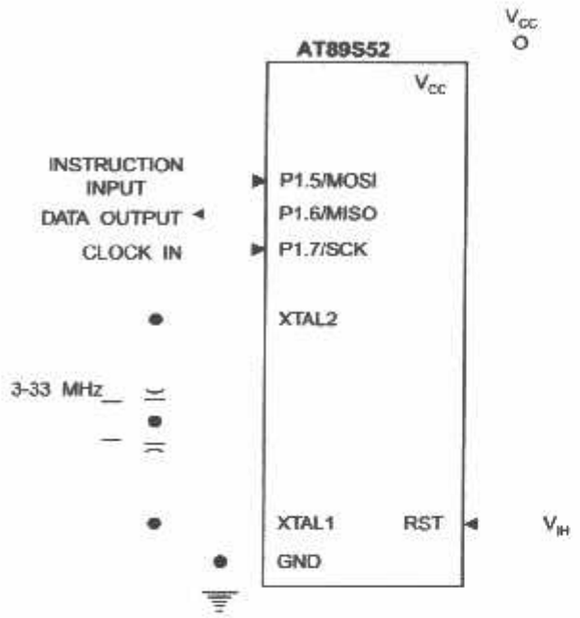


Figure 12. Flash Memory Serial Downloading



sh Programming
i Verification
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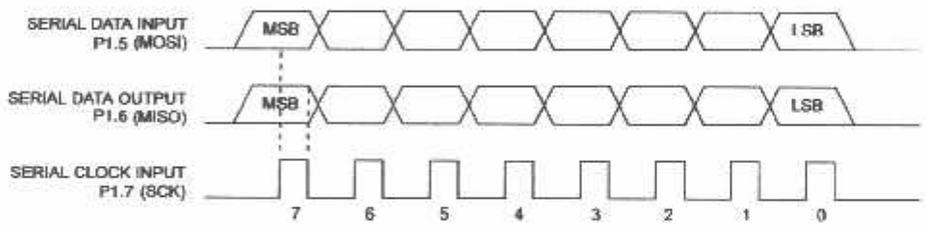
Figure 13. Serial Programming Waveforms



le 11. Serial Programming Instruction Set

ıtruction	Instruction Format Byte 1	Byte 2	Byte 3	Byte 4	Operation
›gramming Enable	1010 1100	0101 0011	xxxx xxxx	xxxx xxxx 0110 1001 (Output on MISO)	Enable Serial Programming while RST is high
ip Erase	1010 1100	100x xxxx	xxxx xxxx	xxxx xxxx	Chip Erase Flash memory array
ad Program Memory te Mode)	0010 0000	xxx A12 A11 A10 A9 A8	A7 A6 A5 A4 A3 A2 A1 A0	D7 D6 D5 D4 D3 D2 D1 D0	Read data from Program memory in the byte mode
te Program Memory te Mode)	0100 0000	xxx A12 A11 A10 A9 A8	A7 A6 A5 A4 A3 A2 A1 A0	D7 D6 D5 D4 D3 D2 D1 D0	Write data to Program memory in the byte mode
te Lock Bits[1]	1010 1100	1110 00 B1 B2	xxxx xxxx	xxxx xxxx	Write Lock bits. See Note (1).
ad Lock Bits	0010 0100	xxxx xxxx	xxxx xxxx	xxx LB3 LB2 LB1 xx	Read back current status of the lock bits (a programmed lock bit reads back as a "1")
ad Signature Bytes	0010 1000	xxx A12 A11 A10 A9 A8	A7 xxx xxx0	Signature Byte	Read Signature Byte
ad Program Memory ge Mode)	0011 0000	xxx A12 A11 A10 A9 A8	Byte 0	Byte 1... Byte 255	Read data from Program memory in the Page Mode (256 bytes)
te Program Memory ge Mode)	0101 0000	xxx A12 A11 A10 A9 A8	Byte 0	Byte 1... Byte 255	Write data to Program memory in the Page Mode (256 bytes)

1. B1 = 0, B2 = 0 —> Mode 1, no lock protection
   B1 = 0, B2 = 1 —> Mode 2, lock bit 1 activated
   B1 = 1, B2 = 0 —> Mode 3, lock bit 2 activated
   B1 = 1, B2 = 1 —> Mode 4, lock bit 3 activated

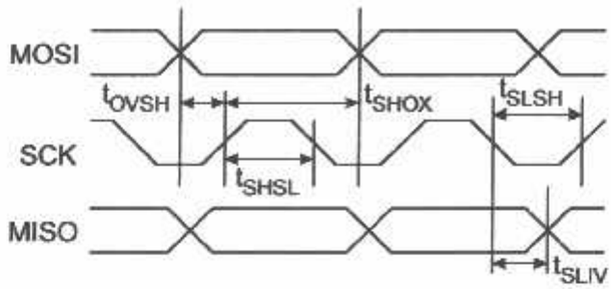
   } **Each of the lock bit modes needs to be activated sequentially** before Mode 4 can be executed.

After Reset signal is high, SCK should be low for at least 64 system clocks before it goes high to clock in the enable data bytes. No pulsing of Reset signal is necessary. SCK should be no faster than 1/16 of the system clock at XTAL1.

For Page Read/Write, the data always starts from byte 0 to 255. After the command byte and upper address byte are latched, each byte thereafter is treated as data until all 256 bytes are shifted in/out. Then the next instruction will be ready to be decoded.

rial Programming Characteristics

ure 14. Serial Programming Timing



e 12. Serial Programming Characteristics, T_A = -40° C to 85° C, V_{CC} = 4.0 - 5.5V (Unless Otherwise Noted)

nbol	Parameter	Min	Typ	Max	Units
:LCL	Oscillator Frequency	3		33	MHz
:L	Oscillator Period	30			ns
SL	SCK Pulse Width High	8 t_{CLCL}			ns
IH	SCK Pulse Width Low	8 t_{CLCL}			ns
SH	MOSI Setup to SCK High	t_{CLCL}			ns
OX	MOSI Hold after SCK High	2 t_{CLCL}			ns
/	SCK Low to MISO Valid	10	16	32	ns
SE	Chip Erase Instruction Cycle Time			500	ms
>	Serial Byte Write Cycle Time			64 t_{CLCL} + 400	µs

ɔsolute Maximum Ratings*

ɛrating Temperature	-55°C to +125°C
ɔrage Temperature	-65°C to +150°C
tage on Any Pin h Respect to Ground	-1.0V to +7.0V
ximum Operating Voltage	6.6V
Output Current	15.0 mA

*NOTICE: Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Characteristics

values shown in this table are valid for T_A = -40°C to 85°C and V_{CC} = 4.0V to 5.5V, unless otherwise noted.

ɔbol	Parameter	Condition	Min	Max	Units
	Input Low Voltage	(Except $\overline{EA}$)	-0.5	0.2 V_{CC}-0.1	V
	Input Low Voltage ($\overline{EA}$)		-0.5	0.2 V_{CC}-0.3	V
	Input High Voltage	(Except XTAL1, RST)	0.2 V_{CC}+0.9	V_{CC}+0.5	V
	Input High Voltage	(XTAL1, RST)	0.7 V_{CC}	V_{CC}+0.5	V
	Output Low Voltage[1] (Ports 1,2,3)	I_{OL} = 1.6 mA		0.45	V
	Output Low Voltage[1] (Port 0, ALE, $\overline{PSEN}$)	I_{OL} = 3.2 mA		0.45	V
	Output High Voltage (Ports 1,2,3, ALE, $\overline{PSEN}$)	I_{OH} = -60 µA, V_{CC} = 5V ± 10%	2.4		V
		I_{OH} = -25 µA	0.75 V_{CC}		V
		I_{OH} = -10 µA	0.9 V_{CC}		V
	Output High Voltage (Port 0 in External Bus Mode)	I_{OH} = -800 µA, V_{CC} = 5V ± 10%	2.4		V
		I_{OH} = -300 µA	0.75 V_{CC}		V
		I_{OH} = -80 µA	0.9 V_{CC}		V
	Logical 0 Input Current (Ports 1,2,3)	V_{IN} = 0.45V		-50	µA
	Logical 1 to 0 Transition Current (Ports 1,2,3)	V_{IN} = 2V, V_{CC} = 5V ±10%		-650	µA
	Input Leakage Current (Port 0, $\overline{EA}$)	0.45 < V_{IN} < V_{CC}		±10	µA
T	Reset Pulldown Resistor		50	300	KΩ
	Pin Capacitance	Test Freq. = 1 MHz, T_A = 25°C		10	pF
	Power Supply Current	Active Mode, 12 MHz		25	mA
		Idle Mode, 12 MHz		6.5	mA
	Power-down Mode[2]	V_{CC} = 5.5V		50	µA

1. Under steady state (non-transient) conditions, I_{OL} must be externally limited as follows:
   Maximum I_{OL} per port pin: 10 mA
   Maximum I_{OL} per 8-bit port:
   Port 0: 26 mA Ports 1, 2, 3: 15 mA
   Maximum total I_{OL} for all output pins: 71 mA
   If I_{OL} exceeds the test condition, V_{OL} may exceed the related specification. Pins are not guaranteed to sink current greater than the listed test conditions.
2. Minimum V_{CC} for Power-down is 2V.

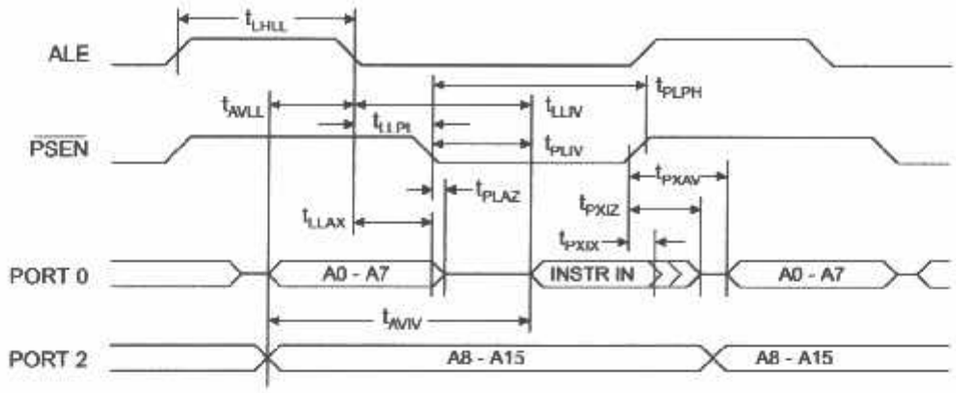
; Characteristics

ler operating conditions, load capacitance for Port 0, ALE/PROG, and PSEN = 100 pF; load capacitance for all other)uts = 80 pF.

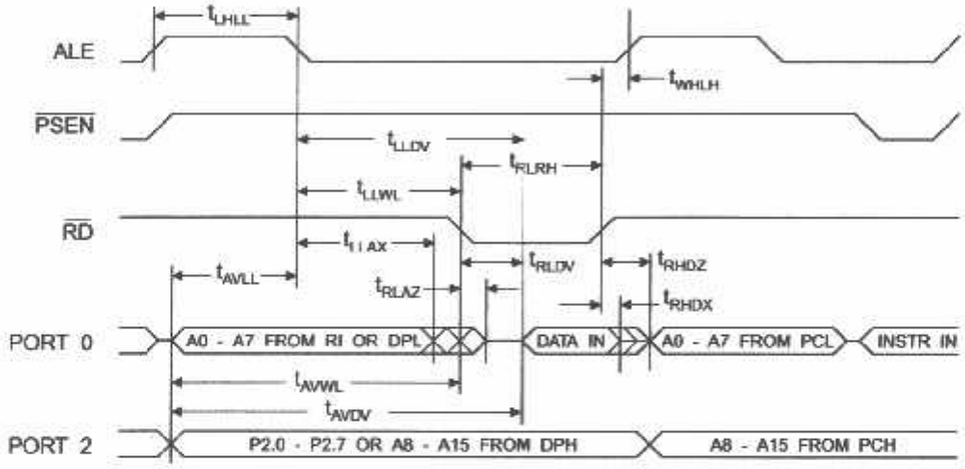
ternal Program and Data Memory Characteristics

mbol	Parameter	12 MHz Oscillator		Variable Oscillator		Units
		Min	Max	Min	Max	
CLCL	Oscillator Frequency			0	33	MHz
L	ALE Pulse Width	127		$2t_{CLCL}$-40		ns
L	Address Valid to ALE Low	43		t_{CLCL}-25		ns
X	Address Hold After ALE Low	48		t_{CLCL}-25		ns
/	ALE Low to Valid Instruction In		233		$4t_{CLCL}$-65	ns
L	ALE Low to $\overline{PSEN}$ Low	43		t_{CLCL}-25		ns
H	$\overline{PSEN}$ Pulse Width	205		$3t_{CLCL}$-45		ns
V	$\overline{PSEN}$ Low to Valid Instruction In		145		$3t_{CLCL}$-60	ns
X	Input Instruction Hold After $\overline{PSEN}$	0		0		ns
Z	Input Instruction Float After $\overline{PSEN}$		59		t_{CLCL}-25	ns
W	$\overline{PSEN}$ to Address Valid	75		t_{CLCL}-8		ns
/	Address to Valid Instruction In		312		$5t_{CLCL}$-80	ns
Z	$\overline{PSEN}$ Low to Address Float		10		10	ns
H	$\overline{RD}$ Pulse Width	400		$6t_{CLCL}$-100		ns
WH	$\overline{WR}$ Pulse Width	400		$6t_{CLCL}$-100		ns
V	$\overline{RD}$ Low to Valid Data In		252		$5t_{CLCL}$-90	ns
X	Data Hold After $\overline{RD}$	0		0		ns
Z	Data Float After $\overline{RD}$		97		$2t_{CLCL}$-28	ns
	ALE Low to Valid Data In		517		$8t_{CLCL}$-150	ns
/	Address to Valid Data In		585		$9t_{CLCL}$-165	ns
	ALE Low to $\overline{RD}$ or $\overline{WR}$ Low	200	300	$3t_{CLCL}$-50	$3t_{CLCL}$+50	ns
	Address to $\overline{RD}$ or $\overline{WR}$ Low	203		$4t_{CLCL}$-75		ns
X	Data Valid to $\overline{WR}$ Transition	23		t_{CLCL}-30		ns
H	Data Valid to $\overline{WR}$ High	433		$7t_{CLCL}$-130		ns
X	Data Hold After $\overline{WR}$	33		t_{CLCL}-25		ns
	$\overline{RD}$ Low to Address Float		0		0	ns
H	$\overline{RD}$ or $\overline{WR}$ High to ALE High	43	123	t_{CLCL}-25	t_{CLCL}+25	ns

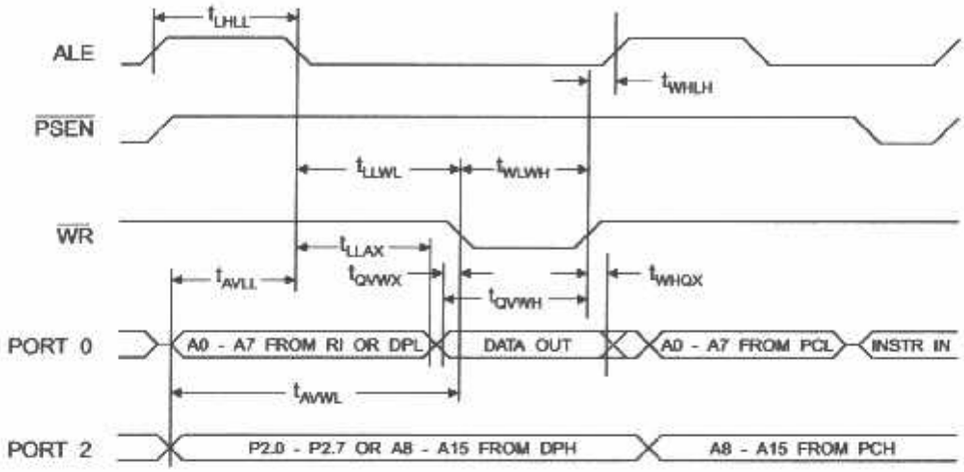
ternal Program Memory Read Cycle



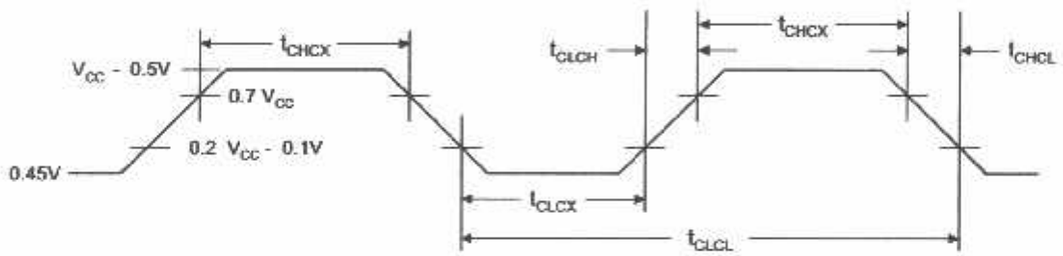
ternal Data Memory Read Cycle



ternal Data Memory Write Cycle



:ernal Clock Drive Waveforms



ernal Clock Drive

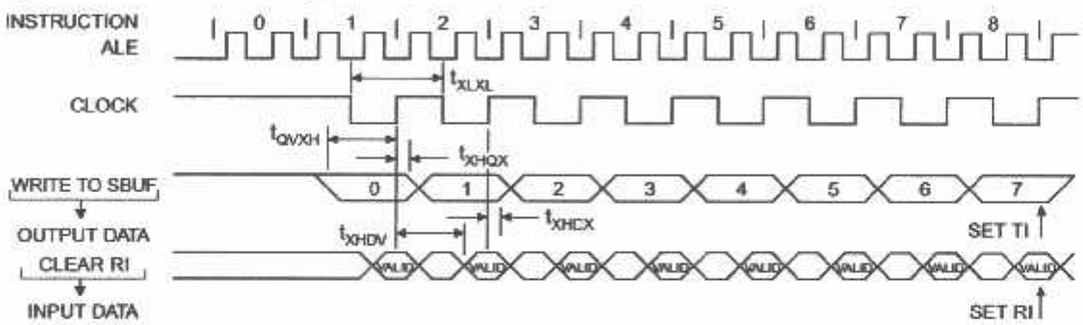
ıbol	Parameter	Min	Max	Units
CL	Oscillator Frequency	0	33	MHz
	Clock Period	30		ns
(	High Time	12		ns
:	Low Time	12		ns
ı	Rise Time		5	ns
	Fall Time		5	ns

rial Port Timing: Shift Register Mode Test Conditions

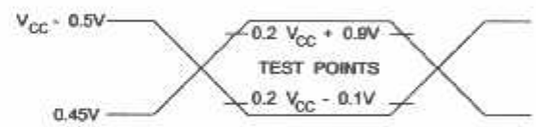
values in this table are valid for V_{CC} = 4.0V to 5.5V and Load Capacitance = 80 pF.

mbol	Parameter	12 MHz Osc		Variable Oscillator		Units
		Min	Max	Min	Max	
:L	Serial Port Clock Cycle Time	1.0		$12t_{CLCL}$		µs
QH	Output Data Setup to Clock Rising Edge	700		$10t_{CLCL}$-133		ns
QX	Output Data Hold After Clock Rising Edge	50		$2t_{CLCL}$-80		ns
DX	Input Data Hold After Clock Rising Edge	0		0		ns
QV	Clock Rising Edge to Input Data Valid		700		$10t_{CLCL}$-133	ns

ift Register Mode Timing Waveforms

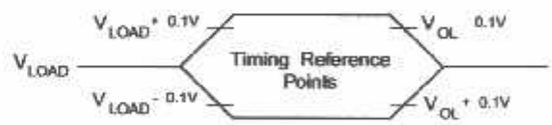


Testing Input/Output Waveforms[1]



1. AC Inputs during testing are driven at V_{CC} - 0.5V for a logic 1 and 0.45V for a logic 0. Timing measurements are made at V_{IH} min. for a logic 1 and V_{IL} max. for a logic 0.

ıt Waveforms[1]



1. For timing purposes, a port pin is no longer floating when a 100 mV change from load voltage occurs. A port pin begins to float when a 100 mV change from the loaded V_{OH}/V_{OL} level occurs.

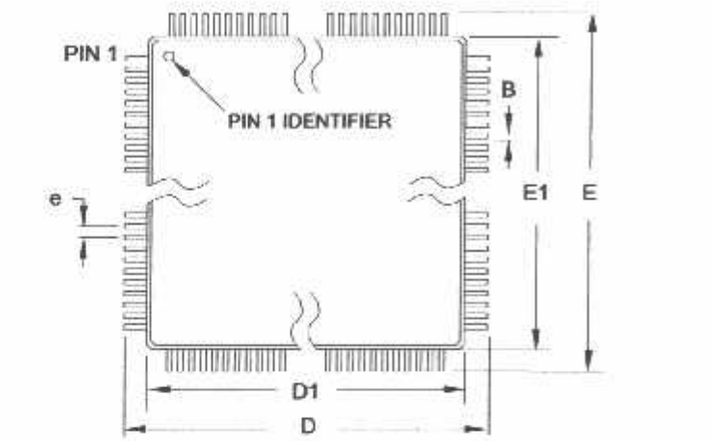
dering Information

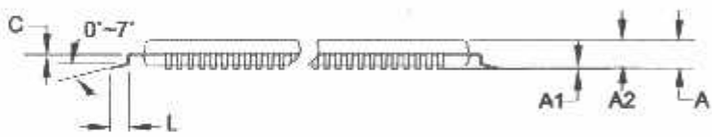
Speed MHz)	Power Supply	Ordering Code	Package	Operation Range
24	4.0V to 5.5V	AT89S52-24AC AT89S52-24JC AT89S52-24PC AT89S52-24SC	44A 44J 40P6 42PS6	Commercial (0° C to 70° C)
		AT89S52-24AI AT89S52-24JI AT89S52-24PI AT89S52-24SI	44A 44J 40P6 42PS6	Industrial (-40° C to 85° C)
33	4.5V to 5.5V	AT89S52-33AC AT89S52-33JC AT89S52-33PC AT89S52-33SC	44A 44J 40P6 42PS6	Commercial (0° C to 70° C)

	Package Type
	44-lead, Thin Plastic Gull Wing Quad Flatpack (TQFP)
	44-lead, Plastic J-leaded Chip Carrier (PLCC)
	40-pin, 0.600" Wide, Plastic Dual Inline Package (PDIP)
6	42-pin, 0.600" Wide, Plastic Dual Inline Package (PDIP)

ckaging Information

A – TQFP





COMMON DIMENSIONS
(Unit of Measure = mm)

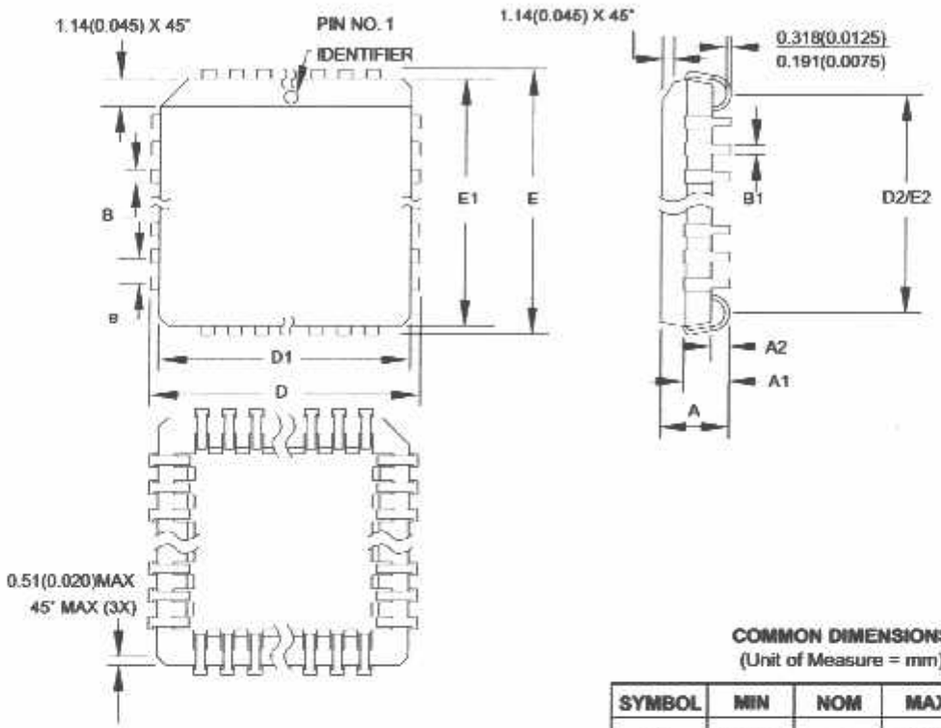
SYMBOL	MIN	NOM	MAX	NOTE
A	–	–	1.20	
A1	0.05	–	0.15	
A2	0.95	1.00	1.05	
D	11.75	12.00	12.25	
D1	9.90	10.00	10.10	Note 2
E	11.75	12.00	12.25	
E1	9.90	10.00	10.10	Note 2
B	0.30	–	0.45	
C	0.09	–	0.20	
L	0.45	–	0.75	
e	0.80 TYP			

Notes:
1. This package conforms to JEDEC reference MS-026, Variation ACB.
2. Dimensions D1 and E1 do not include mold protrusion. Allowable protrusion is 0.25 mm per side. Dimensions D1 and E1 are maximum plastic body size dimensions including mold mismatch.
3. Lead coplanarity is 0.10 mm maximum.

10/5/2001

	TITLE	DRAWING NO.	REV.
2325 Orchard Parkway San Jose, CA 95131	**44A**, 44-lead, 10 x 10 mm Body Size, 1.0 mm Body Thickness, 0.8 mm Lead Pitch, Thin Profile Plastic Quad Flat Package (TQFP)	44A	B

I – PLCC



COMMON DIMENSIONS
(Unit of Measure = mm)

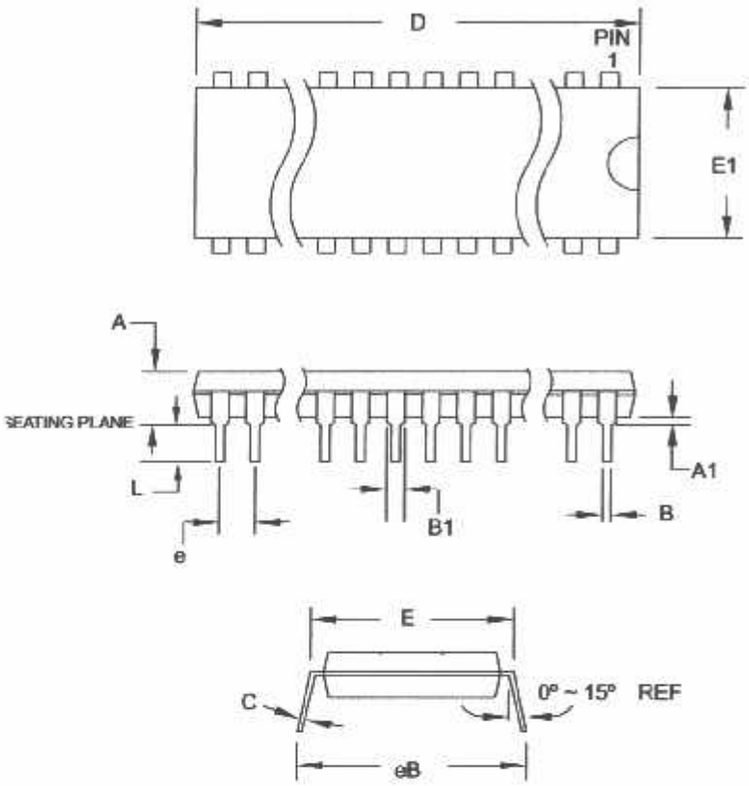
SYMBOL	MIN	NOM	MAX	NOTE
A	4.191	–	4.572	
A1	2.286	–	3.048	
A2	0.508	–	–	
D	17.399	–	17.653	
D1	16.510	–	16.662	Note 2
E	17.399	–	17.653	
E1	16.510	–	16.662	Note 2
D2/E2	14.986	–	16.002	
B	0.660	–	0.813	
B1	0.330	–	0.533	
e	1.270 TYP			

Notes:
1. This package conforms to JEDEC reference MS-018, Variation AC.
2. Dimensions D1 and E1 do not include mold protrusion. Allowable protrusion is .010"(0.254 mm) per side. Dimension D1 and E1 include mold mismatch and are measured at the extreme material condition at the upper or lower parting line.
3. Lead coplanarity is 0.004" (0.102 mm) maximum.

10/04/01

	TITLE	DRAWING NO.	REV.
2325 Orchard Parkway San Jose, CA 95131	**44J**, 44-lead, Plastic J-leaded Chip Carrier (PLCC)	44J	B

40P6 – PDIP



COMMON DIMENSIONS
(Unit of Measure = mm)

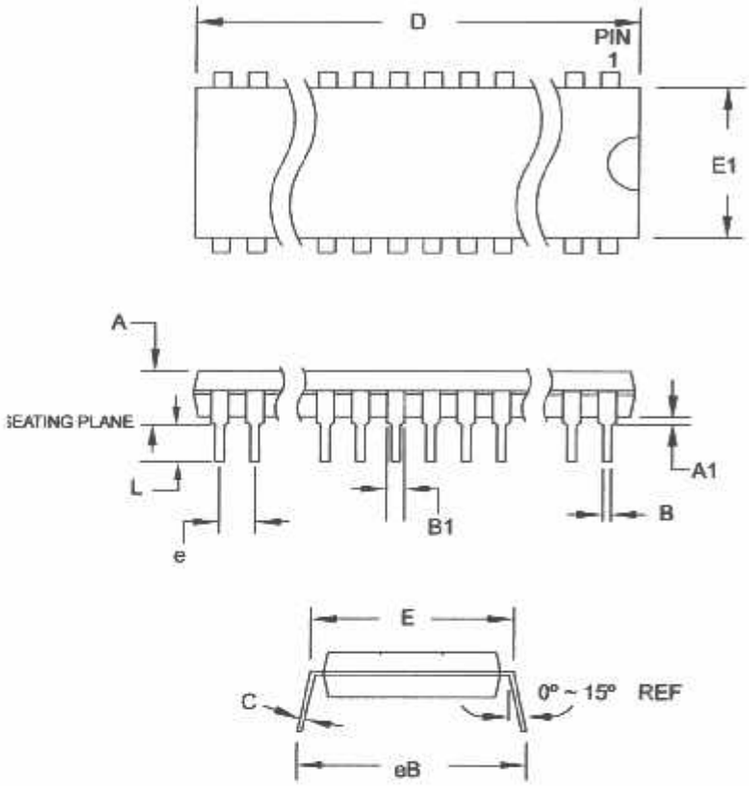
SYMBOL	MIN	NOM	MAX	NOTE
A	–	–	4.826	
A1	0.381	–	–	
D	52.070	–	52.578	Note 2
E	15.240	–	15.875	
E1	13.462	–	13.970	Note 2
B	0.356	–	0.559	
B1	1.041	–	1.651	
L	3.048	–	3.556	
C	0.203	–	0.381	
eB	15.494	–	17.526	
e	2.540 TYP			

Notes:
1. This package conforms to JEDEC reference MS-011, Variation AC.
2. Dimensions D and E1 do not include mold Flash or Protrusion. Mold Flash or Protrusion shall not exceed 0.25 mm (0.010").

09/28/01

	TITLE	DRAWING NO.	REV.
2325 Orchard Parkway San Jose, CA 95131	**40P6**, 40-lead (0.600"/15.24 mm Wide) Plastic Dual Inline Package (PDIP)	40P6	B

'S6 – PDIP



COMMON DIMENSIONS
(Unit of Measure = mm)

SYMBOL	MIN	NOM	MAX	NOTE
A	–	–	4.83	
A1	0.51	–	–	
D	36.70	–	36.96	Note 2
E	15.24	–	15.88	
E1	13.46	–	13.97	Note 2
B	0.38	–	0.56	
B1	0.76	–	1.27	
L	3.05	–	3.43	
C	0.20	–	0.30	
eB	–	–	18.55	
e	1.78 TYP			

Notes:
1. This package conforms to JEDEC reference MS-011, Variation AC.
2. Dimensions D and E1 do not include mold Flash or Protrusion. Mold Flash or Protrusion shall not exceed 0.25 mm (0.010").

11/6/03

	TITLE	DRAWING NO.	REV.
2325 Orchard Parkway San Jose, CA 95131	**42PS6**, 42-lead (0.600"/15.24 mm Wide) Plastic Dual Inline Package (PDIP)	42PS6	A

mel Corporation

:325 Orchard Parkway
San Jose, CA 95131, USA
'el: 1(408) 441-0311
'ax: 1(408) 487-2600

gional Headquarters

rope
.tmel Sarl
:oute des Arsenaux 41
:ase Postale 80
H-1705 Fribourg
witzerland
el: (41) 26-426-5555
ax: (41) 26-426-5500

a
:oom 1219
:hinachem Golden Plaza
7 Mody Road Tsimshatsui
ast Kowloon
ong Kong
el: (852) 2721-9778
ax: (852) 2722-1369

an
:, Tonetsu Shinkawa Bldg.
24-8 Shinkawa
huo-ku, Tokyo 104-0033
pan
l: (81) 3-3523-3551
ix: (81) 3-3523-7581

Atmel Operations

Memory
2325 Orchard Parkway
San Jose, CA 95131, USA
Tel: 1(408) 441-0311
Fax: 1(408) 436-4314

Microcontrollers
2325 Orchard Parkway
San Jose, CA 95131, USA
Tel: 1(408) 441-0311
Fax: 1(408) 436-4314

La Chantrerie
BP 70602
44306 Nantes Cedex 3, France
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Fax: (44) 1355-242-743

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Tel: (49) 71-31-67-0
Fax: (49) 71-31-67-2340

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Colorado Springs, CO 80906, USA
Tel: 1(719) 576-3300
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Fax: (33) 4-76-58-34-80

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1919B–MICRO–11/03

DALLAS SEMICONDUCTOR

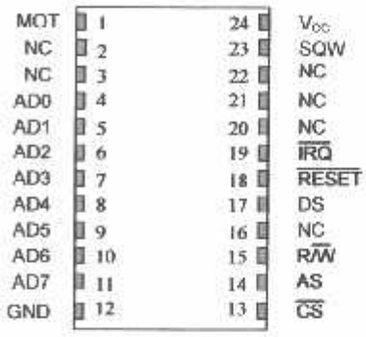
DS12C887
Real Time Clock

www.dalsemi.com

EATURES

Drop-in replacement for IBM AT computer clock/calendar
Pin compatible with the MC146818B and DS1287
Totally nonvolatile with over 10 years of operation in the absence of power
Self-contained subsystem includes lithium, quartz, and support circuitry.
Counts seconds, minutes, hours, days, day of the week, date, month, and year with leap year compensation valid up to 2100
Binary or BCD representation of time, calendar, and alarm
12– or 24–hour clock with AM and PM in 12–hour mode
Daylight Savings Time option
Selectable between Motorola and Intel bus timing
Multiplex bus for pin efficiency
Interfaced with software as 128 RAM locations
  15 bytes of clock and control registers
– 113 bytes of general purpose RAM
Programmable square wave output signal
Bus–compatible interrupt signals (IRQ)
Three interrupts are separately software maskable and testable
– Time–of–day alarm once/second to once/day
– Periodic rates from 122 ms to 500 ms
– End of clock update cycle
Century register

PIN ASSIGNMENT



DS12C887 24-Pin
ENCAPSULATED PACKAGE

PIN DESCRIPTION

AD0-AD7	-	Multiplexed Address/Data Bus
NC	-	No Connect
MOT	-	Bus Type Selection
$\overline{CS}$	-	RTC Chip Select Input
AS	-	Address Strobe
R/$\overline{W}$	-	Read/Write Input
DS	-	Data Strobe
$\overline{RESET}$	-	Reset Input
$\overline{IRQ}$	-	Interrupt Request Output
SQW	-	Square Wave Output
V_{CC}	-	+5 Volt Main Supply
GND	-	Ground

:SCRIPTION

: DS12C887 Real Time Clock plus RAM is designed as a direct upgrade replacement for the DS12887 :xisting IBM compatible personal computers to add hardware year 2000 compliance. A century byte : added to memory location 50, 32h, as called out by the PC AT specification. A lithium energy rce, quartz crystal, and write-protection circuitry are contained within a 24–pin dual in-line package. such, the DS12C887 is a complete subsystem replacing 16 components in a typical application. The :tions include a nonvolatile time-of-day clock, an alarm, a one-hundred-year calendar, programmable rrupt, square wave generator, and 113 bytes of nonvolatile static RAM. The real time clock is inctive in that time-of-day and memory are maintained even in the absence of power.

PERATION

ıe block diagram in Figure 1 shows the pin connections with the major internal functions of the 512C887. The following paragraphs describe the function of each pin.

IGNAL DESCRIPTIONS

ND, V_{CC} - DC power is provided to the device on these pins. V_{CC} is the +5 volt input. When 5 volts are plied within normal limits, the device is fully accessible and data can be written and read. When V_{CC} is low 4.25 volts typical, reads and writes are inhibited. However, the timekeeping function continues affected by the lower input voltage. As V_{CC} falls below 3 volts typical, the RAM and timekeeper are itched over to an internal lithium energy source. The timekeeping function maintains an accuracy of ±1 nute per month at 25°C regardless of the voltage input on the V_{CC} pin.

OT (Mode Select) – The MOT pin offers the flexibility to choose between two bus types. When nected to V_{CC}, Motorola bus timing is selected. When connected to GND or left disconnected, Intel s timing is selected. The pin has an internal pull-down resistance of approximately 20KΩ.

W (Square Wave Output) – The SQW pin can output a signal from one of 13 taps provided by the internal divider stages of the Real Time Clock. The frequency of the SQW pin can be changed by gramming Register A as shown in Table 1. The SQW signal can be turned on and off using the SQWE in Register B. The SQW signal is not available when V_{CC} is less than 4.25 volts typical.

0-AD7 (Multiplexed Bidirectional Address/Data Bus) – Multiplexed buses save pins because dress information and data information time share the same signal paths. The addresses are present ing the first portion of the bus cycle and the same pins and signal paths are used for data in the second tion of the cycle. Address/data multiplexing does not slow the access time of the DS12C887 since the change from address to data occurs during the internal RAM access time. Addresses must be valid or to the falling edge of AS/ALE, at which time the DS12C887 latches the address from AD0 to AD6. lid write data must be present and held stable during the latter portion of the DS or WR pulses. In a d cycle the DS12C887 outputs 8 bits of data during the latter portion of the DS or RD pulses. The read le is terminated and the bus returns to a high impedance state as DS transitions low in the case of torola timing or as RD transitions high in the case of Intel timing.

(Address Strobe Input) – A positive going address strobe pulse serves to demultiplex the bus. The ing edge of AS/ALE causes the address to be latched within the DS12C887. The next rising edge that urs on the AS bus will clear the address regardless of whether $\overline{CS}$ is asserted. Access commands uld be sent in pairs.

(Data Strobe or Read Input) – The DS/RD pin has two modes of operation depending on the level he MOT pin. When the MOT pin is connected to V_{CC}, Motorola bus timing is selected. In this mode is a positive pulse during the latter portion of the bus cycle and is called Data Strobe. During read les, DS signifies the time that the DS12C887 is to drive the bidirectional bus. In write cycles the ling edge of DS causes the DS12C887 to latch the written data. When the MOT pin is connected to D, Intel bus timing is selected. In this mode the DS pin is called Read(RD). RD identifies the time od when the DS12C887 drives the bus with read data. The RD signal is the same definition as the put Enable (OE) signal on a typical memory.

'W (Read/Write Input) – The R/$\overline{W}$ pin also has two modes of operation. When the MOT pin is nnected to V_{CC} for Motorola timing, R/W is at a level which indicates whether the current cycle is a ad or write. A read cycle is indicated with a high level on R/W while DS is high. A write cycle is dicated when R/$\overline{W}$ is low during DS. When the MOT pin is connected to GND for Intel timing, the W signal is an active low signal called WR. In this mode the R/$\overline{W}$ pin has the same meaning as the rite Enable signal (WE) on generic RAMs.

; (Chip Select Input) – The Chip Select signal must be asserted low for a bus cycle in the DS12C887 be accessed. $\overline{CS}$ must be kept in the active state during DS and AS for Motorola timing and during RD d WR for Intel timing. Bus cycles which take place without asserting $\overline{CS}$ will latch addresses but no cess will occur. When V_{CC} is below 4.25 volts, the DS12C887 internally inhibits access cycles by ernally disabling the $\overline{CS}$ input. This action protects both the real time clock data and RAM data during wer outages.

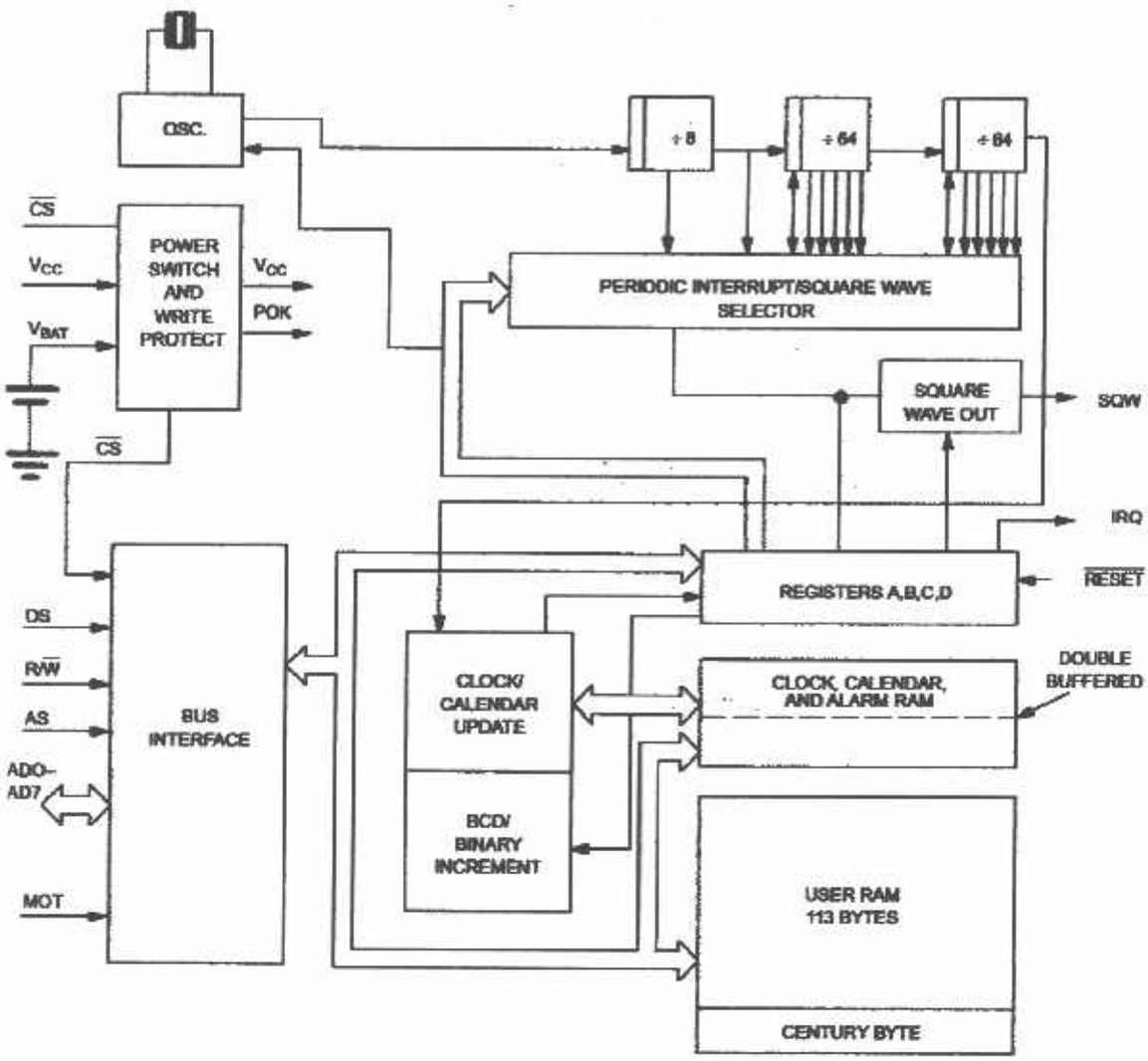
Q (Interrupt Request Output) - The $\overline{IRQ}$ pin is an active low output of the DS12C887 that can be d as an interrupt input to a processor. The $\overline{IRQ}$ output remains low as long as the status bit causing the errupt is present and the corresponding interrupt-enable bit is set. To clear the $\overline{IRQ}$ pin the processor gram normally reads the C register. The RESET pin also clears pending interrupts. When no interrupt ditions are present, the $\overline{IRQ}$ level is in the high impedance state. Multiple interrupting devices can be nected to an $\overline{IRQ}$ bus. The IRQ bus is an open drain output and requires an external pull-up resistor.

$\overline{SET}$ (Reset Input) – The $\overline{RESET}$ pin has no effect on the clock, calendar, or RAM. On power-up the $\overline{SET}$ pin can be held low for a time in order to allow the power supply to stabilize. The amount of e that $\overline{RESET}$ is held low is dependent on the application. However, if $\overline{RESET}$ is used on power–up, time $\overline{RESET}$ is low should exceed 200 ms to make sure that the internal timer that controls the 12C887 on power-up has timed out. When $\overline{RESET}$ is low and V_{CC} is above 4.25 volts, the following urs:

A. Periodic Interrupt Enable (PEI) bit is cleared to zero.
B. Alarm Interrupt Enable (AIE) bit is cleared to zero.
C. Update Ended Interrupt Flag (UF) bit is cleared to zero.
D. Interrupt Request Status Flag (IRQF) bit is cleared to zero.
E. Periodic Interrupt Flag (PF) bit is cleared to zero.
F. The device is not accessible until $\overline{RESET}$ is returned high.
G. Alarm Interrupt Flag (AF) bit is cleared to zero.
H. $\overline{IRQ}$ pin is in the high impedance state.
I. Square Wave Output Enable (SQWE) bit is cleared to zero.
J. Update Ended Interrupt Enable (UIE) is cleared to zero.

typical application $\overline{RESET}$ can be connected to V_{CC} . This connection will allow the DS12C887 to n and out of power fail without affecting any of the control registers.

S12C887 BLOCK DIAGRAM Figure 1



OWER-DOWN/POWER-UP CONSIDERATIONS

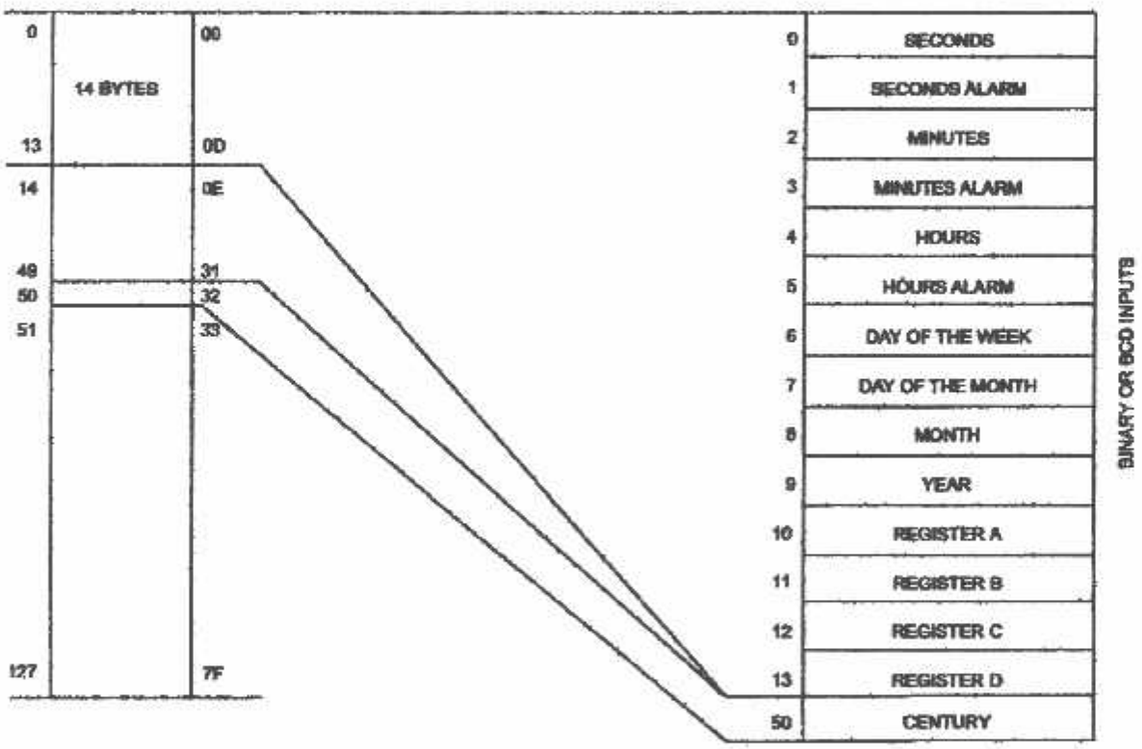
ıe Real Time Clock function will continue to operate and all of the RAM, time, calendar, and alarm emory locations remain nonvolatile regardless of the level of the V_{CC} input. When V_{CC} is applied to the S12C887 and reaches a level of greater than 4.25 volts, the device becomes accessible after 200 ms, ovided that the oscillator is running and the oscillator countdown chain is not in reset (see Register A). iis time period allows the system to stabilize after power is applied. When V_{CC} falls below 4.25 volts, ɔ chip select input is internally forced to an inactive level regardless of the value of $\overline{CS}$ at the input pin. ıe DS12C887 is, therefore, write-protected. When the DS12C887 is in a write-protected state, all inputs ɔ ignored and all outputs are in a high impedance state. When V_{CC} falls below a level of approximately volts, the external V_{CC} supply is switched off and an internal lithium energy source supplies power to ɔ Real Time Clock and the RAM memory.

TC ADDRESS MAP

e address map for the DS12C885 is shown in Figure 2. The address map consists of 113 bytes of user \M, 11 bytes of RAM that contain the RTC time, calendar, and alarm data, and 4 bytes which are used ' control and status. All 128 bytes can be directly written or read except for the following:

1. Registers C and D are read-only.
2. Bit-7 of Register A is read-only.
3. The high order bit of the seconds byte is read-only.

S12C887 REAL TIME CLOCK ADDRESS MAP Figure 2



IME, CALENDAR AND ALARM LOCATIONS

ıe time and calendar information is obtained by reading the appropriate memory bytes. The time, lendar, and alarm are set or initialized by writing the appropriate RAM bytes. The contents of the ten ne, calendar, and alarm bytes can be either Binary or Binary-Coded Decimal (BCD) format. Before riting the internal time, calendar, and alarm registers, the SET bit in Register B should be written to a gic one to prevent updates from occurring while access is being attempted. In addition to writing the ten nc, calendar, and alarm registers in a selected format (binary or BCD), the data mode bit (DM) of egister B must be set to the appropriate logic level. All ten time, calendar, and alarm bytes must use the me data mode. The set bit in Register B should be cleared after the data mode bit has been written to ow the real time clock to update the time and calendar bytes. Once initialized, the real time clock ıkes all updates in the selected mode. The data mode cannot be changed without reinitializing the ten ta bytes. Table 2 shows the binary and BCD formats of the ten time, calendar, and alarm locations. The –12 bit cannot be changed without reinitializing the hour locations. When the 12–hour format is ected, the high order bit of the hours byte represents PM when it is a logic one. The time, calendar, d alarm bytes are always accessible because they are double buffered. Once per second the eleven bytes : advanced by one second and checked for an alarm condition. If a read of the time and calendar data :urs during an update, a problem exists where seconds, minutes, hours, etc. may not correlate. The)bability of reading incorrect time and calendar data is low. Several methods of avoiding any possible :orrect time and calendar reads are covered later in this text. The three alarm bytes can be used in two ys. First, when the alarm time is written in the appropriate hours, minutes, and seconds alarm :ations, the alarm interrupt is initiated at the specified time each day if the alarm enable bit is high . The :ond use condition is to insert a "don't care" state in one or more of the three alarm bytes. The "don't e" code is any hexadecimal value from C0 to FF. The two most significant bits of each byte set the)n't care" condition when at logic 1. An alarm will be generated each hour when the "don't care" bits : set in the hours byte. Similarly, an alarm is generated every minute with "don't care" codes in the ırs and minute alarm bytes. The "don't care" codes in all three alarm bytes create an interrupt every ond.

ME, CALENDAR AND ALARM DATA MODES Table 1

ADDRESS LOCATION	FUNCTION	DECIMAL RANGE	RANGE	
			BINARY DATA MODE	BCD DATA MODE
0	Seconds	0-59	00-3B	00-59
1	Seconds Alarm	0-59	00-3B	00-59
2	Minutes	0-59	00-3B	00-59
3	Minutes Alarm	0-59	00-3B	00-59
4	Hours 12-hr, Mode	1-12	01-0C AM, 81-8C PM	01-12 AM, 81-92 PM
	Hours 24-hr, Mode	0-23	00-17	00-23
5	Hours Alarm 12-hr, Mode	1-12	01-0C AM, 81-8C PM	01-12 AM, 81-92 PM
	Hours Alarm 24-hr, Mode	0-23	00-17	00-23
6	Day of the week Sunday=1	1-7	01-07	01-07
7	Date of Month	1-31	01-1F	01-31
8	Month	1-12	01-0C	01-12
9	Year	0-99	00-63	00-99
50	Century	0-99	NA	19,20

ONTROL REGISTERS

ıe DS12C887 has four control registers which are accessible at all times, even during the update cycle.

EGISTER A

SB **LSB**

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
UIP	DV2	DV1	DV0	RS3	RS2	RS1	RS0

IP - The Update In Progress (UIP) bit is a status flag that can be monitored. When the UIP bit is a 1, the date transfer will soon occur. When UIP is a 0, the update transfer will not occur for at least 244µs. e time, calendar, and alarm information in RAM is fully available for access when the UIP bit is 0. The P bit is read-only and is not affected by $\overline{\text{RESET}}$. Writing the SET bit in Register B to a 1 inhibits any date transfer and clears the UIP status bit.

/2, DV1, DV0 - These three bits are used to turn the oscillator on or off and to reset the countdown ain. A pattern of 010 is the only combination of bits that will turn the oscillator on and allow the RTC keep time. A pattern of 11X will enable the oscillator but holds the countdown chain in reset. The next date will occur at 500 ms after a pattern of 010 is written to DV0, DV1, and DV2.

3, RS2, RS1, RS0 - These four rate-selection bits select one of the 13 taps on the 15-stage divider or able the divider output. The tap selected can be used to generate an output square wave (SQW pin) l/or a periodic interrupt. The user can do one of the following:

1. Enable the interrupt with the PIE bit;
2. Enable the SQW output pin with the SQWE bit;
3. Enable both at the same time and the same rate; or
4. Enable neither

ole 1 lists the periodic interrupt rates and the square wave frequencies that can be chosen with the RS :. These four read/write bits are not affected by $\overline{\text{RESET}}$.

EGISTER B

SB **LSB**

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
SET	PIE	AIE	UIE	SQWE	DM	24/12	DSE

ET - When the SET bit is a 0, the update transfer functions normally by advancing the counts once per cond. When the SET bit is written to a 1, any update transfer is inhibited and the program can initialize e time and calendar bytes without an update occurring in the midst of initializing. Read cycles can be ecuted in a similar manner. SET is a read/write bit and is not affected by $\overline{\text{RESET}}$ or internal functions the DS12C887.

E - The Periodic Interrupt Enable bit is a read/write bit which allows the Periodic Interrupt Flag (PF) in Register C to drive the $\overline{\text{IRQ}}$ pin low. When the PIE bit is set to 1, periodic interrupts are generated driving the $\overline{\text{IRQ}}$ pin low at a rate specified by the RS3-RS0 bits of Register A. A 0 in the PIE bit ocks the $\overline{\text{IRQ}}$ output from being driven by a periodic interrupt, but the Periodic Flag (PF) bit is still set the periodic rate. PIE is not modified by any internal DS12C887 functions but is cleared to 0 on $\overline{\text{ESET}}$.

E - The Alarm Interrupt Enable (AIE) bit is a read/write bit which, when set to a 1, permits the Alarm ag (AF) bit in register C to assert $\overline{\text{IRQ}}$. An alarm interrupt occurs for each second that the 3 time bytes ual the 3 alarm bytes including a "don't care" alarm code of binary 11XXXXXX. When the AIE bit is to 0, the AF bit does not initiate the $\overline{\text{IRQ}}$ signal. The internal functions of the DS12C887 not affect AIE bit.

E - The Update Ended Interrupt Enable (UIE) bit is a read/write bit that enables the Update End Flag F) bit in Register C to assert $\overline{\text{IRQ}}$. The $\overline{\text{RESET}}$ pin going low or the SET bit going high clears the E bit.

WE - When the Square Wave Enable (SQWE) bit is set to a 1, a square wave signal at the frequency by the rate-selection bits RS3 through RS0 is driven out on the SQW pin. When the SQWE bit is set), the SQW pin is held low. SQWE is a read/write bit and is cleared by $\overline{\text{RESET}}$. SQWE is set to a 1 en V_{CC} is powered up.

I - The Data Mode (DM) bit indicates whether time and calendar information is in binary or BCD nat. The DM bit is set by the program to the appropriate format and can be read as required. This bit ot modified by internal functions or $\overline{\text{RESET}}$. A 1 in DM signifies binary data while a 0 in DM cifies Binary Coded Decimal (BCD) data.

12 - The 24/12 control bit establishes the format of the hours byte. A 1 indicates the 24-hour mode and indicates the 12-hour mode. This bit is read/write and is not affected by internal functions or $\overline{\text{RESET}}$.

E - The Daylight Savings Enable (DSE) bit is a read/write bit which enables two special updates when E is set to 1. On the first Sunday in April the time increments from 1:59:59 AM to 3:00:00 AM. On last Sunday in October when the time first reaches 1:59:59 AM it changes to 1:00:00 AM. These cial updates do not occur when the DSE bit is a zero. This bit is not affected by internal functions or $\overline{\text{SET}}$.

EGISTER C

SB **LSB**

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
IRQF	PF	AF	UF	0	0	0	0

:QF - The Interrupt Request Flag (IRQF) bit is set to a 1 when one or more of the following are true:
: = PIE = 1
= AIE = 1
= UIE = 1

., IRQF = (PF • PIE) + (AF • AIE) + (UF • UIE)

ıy time the IRQF bit is a 1, the $\overline{\text{IRQ}}$ pin is driven low. Flag bits PF, AF, and UF are cleared after gister C is read by the program or when the $\overline{\text{RESET}}$ pin is low.

' - The Periodic Interrupt Flag (PF) is a read-only bit which is set to a 1 when an edge is detected on the ected tap of the divider chain. The RS3 through RS0 bits establish the periodic rate. PF is set to a 1 lependent of the state of the PIE bit. When both PF and PIE are 1's, the $\overline{\text{IRQ}}$ signal is active and will the IRQF bit. The PF bit is cleared by a software read of Register C or a $\overline{\text{RESET}}$.

' - A 1 in the Alarm Interrupt Flag (AF) bit indicates that the current time has matched the alarm time. he AIE bit is also a 1, the $\overline{\text{IRQ}}$ pin will go low and a 1 will appear in the IRQF bit. A $\overline{\text{RESET}}$ or a read Register C will clear AF.

' - The Update Ended Interrupt Flag (UF) bit is set after each update cycle. When the UIE bit is set to he 1 in UF causes the IRQF bit to be a 1, which will assert the $\overline{\text{IRQ}}$ pin. UF is cleared by reading gister C or a $\overline{\text{RESET}}$.

T 3 THROUGH BIT 0 - These are unused bits of the status Register C. These bits always read 0 and not be written.

:GISTER D

B **LSB**

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
VRT	0	0	0	0	0	0	0

T - The Valid RAM and Time (VRT) bit indicates the condition of the battery connected to the V_{BAT} . This bit is not writeable and should always be a 1 when read. If a 0 is ever present, an exhausted rnal lithium energy source is indicated and both the contents of the RTC data and RAM data are stionable. This bit is unaffected by $\overline{\text{RESET}}$.

' 6 THROUGH BIT 0 - The remaining bits of Register D are not usable. They cannot be written and, n read, they will always read 0.

:ENTURY REGISTER

he century register at location 32h, is a BCD register designed to automatically load the BCD value 20 ; the year register changes from 99 to 00. The MSB of this register will not be affected when the load of) occurs and will remain at the value written by the user.

ONVOLATILE RAM

ıe 113 general purpose nonvolatile RAM bytes are not dedicated to any special function within the S12C887. They can be used by the processor program as nonvolatile memory and are fully available ıring the update cycle.

ITERRUPTS

ıe RTC plus RAM includes three separate, fully automatic sources of interrupt for a processor. The ırm interrupt can be programmed to occur at rates from once per second to once per day. The periodic :errupt can be selected for rates from 500ms to 122µs. The update-ended interrupt can be used to dicate to the program that an update cycle is complete. Each of these independent interrupt conditions is scribed in greater detail in other sections of this text.

ıe processor program can select which interrupts, if any, are going to be used. Three bits in Register B able the interrupts. Writing a logic 1 to an interrupt-enable bit permits that interrupt to be initiated ıen the event occurs. A zero in an interrupt-enable bit prohibits the $\overline{IRQ}$ pin from being asserted from ıt interrupt condition. If an interrupt flag is already set when an interrupt is enabled, $\overline{IRQ}$ is mediately set at an active level, although the interrupt initiating the event may have occurred much rlier. As a result, there are cases where the program should clear such earlier initiated interrupts before st enabling new interrupts.

ıen an interrupt event occurs, the relating flag bit is set to logic 1 in Register C. These flag bits are set lependent of the state of the corresponding enable bit in Register B. The flag bit can be used in a ling mode without enabling the corresponding enable bits. The interrupt flag bit is a status bit which tware can interrogate as necessary. When a flag is set, an indication is given to software that an errupt event has occurred since the flag bit was last read; however, care should be taken when using the g bits as they are cleared each time Register C is read. Double latching is included with Register C so t bits which are set remain stable throughout the read cycle. All bits which are set (high) are cleared en read and new interrupts which are pending during the read cycle are held until after the cycle is npleted. One, two, or three bits can be set when reading Register C. Each utilized flag bit should be ımined when read to ensure that no interrupts are lost.

: second flag bit usage method is with fully enabled interrupts. When an interrupt flag bit is set and the responding interrupt enable bit is also set, the $\overline{IRQ}$ pin is asserted low. $\overline{IRQ}$ is asserted as long as at st one of the three interrupt sources has its flag and enable bits both set. The IRQF bit in Register C is ne whenever the $\overline{IRQ}$ pin is being driven low. Determination that the RTC initiated an interrupt is omplished by reading Register C. A logic one in bit 7 (IRQF bit) indicates that one or more interrupts e been initiated by the DS12C887. The act of reading Register C clears all active flag bits and the)F bit.

)SCILLATOR CONTROL BITS

Vhen the DS12C887 is shipped from the factory, the internal oscillator is turned off. This feature revents the lithium energy cell from being used until it is installed in a system. A pattern of 010 in bits 4 irough 6 of Register A will turn the oscillator on and enable the countdown chain. A pattern of 11X will irn the oscillator on, but holds the countdown chain of the oscillator in reset. All other combinations of its 4 through 6 keep the oscillator off.

:QUARE WAVE OUTPUT SELECTION

hirteen of the 15 divider taps are made available to a 1-of-15 selector, as shown in the block diagram of igure 1. The first purpose of selecting a divider tap is to generate a square wave output signal on the QW pin. The RS0–RS3 bits in Register A establish the square wave output frequency. These equencies are listed in Table 1. The SQW frequency selection shares its 1-of-15 selector with the :riodic interrupt generator. Once the frequency is selected, the output of the SQW pin can be turned on id off under program control with the square wave enable bit (SQWE).

ERIODIC INTERRUPT SELECTION

ie periodic interrupt will cause the $\overline{IRQ}$ pin to go to an active state from once every 500ms to once 'ery 122µs. This function is separate from the alarm interrupt which can be output from once per second once per day. The periodic interrupt rate is selected using the same Register A bits which select the uare wave frequency (see Table 1). Changing the Register A bits affects both the square wave equency and the periodic interrupt output. However, each function has a separate enable bit in Register . The SQWE bit controls the square wave output. Similarly, the periodic interrupt is enabled by the PIE t in Register B. The periodic interrupt can be used with software counters to measure inputs, create itput intervals, or await the next needed software function.

ERIODIC INTERRUPT RATE AND SQUARE WAVE OUTPUT FREQUENCY

able 2

EXT. REG. B	SELECT BITS REGISTER A				t_{PI} PERIODIC INTERRUPT RATE	SQW OUTPUT FREQUENCY
E32K	RS3	RS2	RS1	RS0		
0	0	0	0	0	None	None
0	0	0	0	1	3.90625 ms	256 Hz
0	0	0	1	0	7.8125 ms	128 Hz
0	0	0	1	1	122.070 µs	8.192 kHz
0	0	1	0	0	244.141 µs	4.096 kHz
0	0	1	0	1	488.281 µs	2.048 kHz
0	0	1	1	0	976.5625 µs	1.024 kHz
0	0	1	1	1	1.953125 ms	512 Hz
0	1	0	0	0	3.90625 ms	256 Hz
0	1	0	0	1	7.8125 ms	128 Hz
0	1	0	1	0	15.625 ms	64 Hz
0	1	0	1	1	31.25 ms	32 Hz
0	1	1	0	0	62.5 ms	16 Hz
0	1	1	0	1	125 ms	8 Hz
0	1	1	1	0	250 ms	4 Hz
0	1	1	1	1	500 ms	2 Hz

IPDATE CYCLE

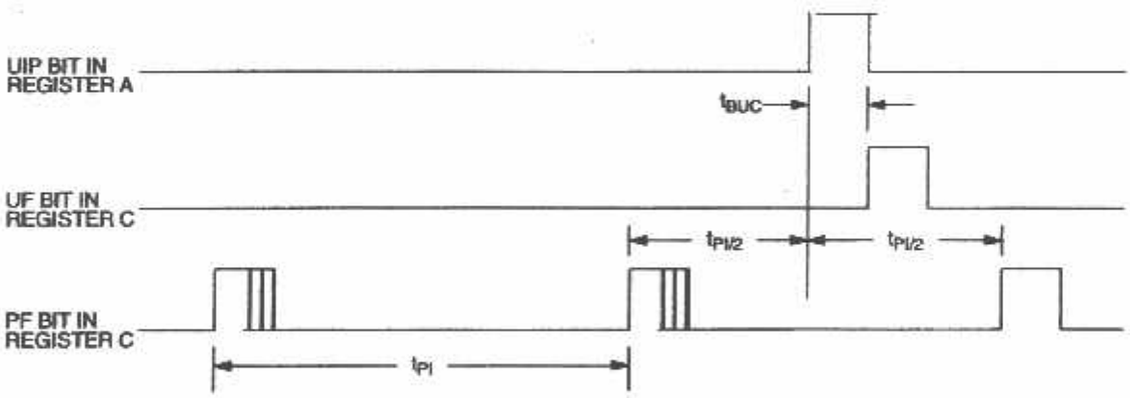
he DS12C887 executes an update cycle once per second regardless of the SET bit in Register B. When ıe SET bit in Register B is set to one, the user copy of the double buffered time, calendar, and alarm ytes is frozen and will not update as the time increments. However, the time countdown chain continues) update the internal copy of the buffer. This feature allows time to maintain accuracy independent of :ading or writing the time, calendar, and alarm buffers and also guarantees that time and calendar ıformation is consistent. The update cycle also compares each alarm byte with the corresponding time yte and issues an alarm if a match or if a "don't care" code is present in all three positions.

here are three methods that can handle access of the real time clock that avoid any possibility of :cessing inconsistent time and calendar data. The first method uses the update-ended interrupt. If ıabled, an interrupt occurs after every up date cycle that indicates that over 999 ms are available to read ılid time and date information. If this interrupt is used, the IRQF bit in Register C should be cleared :fore leaving the interrupt routine.

second method uses the update-in-progress bit (UIP) in Register A to determine if the update cycle is in ogress. The UIP bit will pulse once per second. After the UIP bit goes high, the update transfer occurs 44µs later. If a low is read on the UIP bit, the user has at least 244µs before the time/calendar data will : changed. Therefore, the user should avoid interrupt service routines that would cause the time needed read valid time/calendar data to exceed 244µs.

ıe third method uses a periodic interrupt to determine if an update cycle is in progress. The UIP bit in egister A is set high between the setting of the PF bit in Register C (see Figure 3). Periodic interrupts at occur at a rate of greater than t_{BUC} allow valid time and date information to be reached at each currence of the periodic interrupt. The reads should be complete within 1 ($t_{PI/2} + t_{BUC}$) to ensure that ta is not read during the update cycle.

PDATE-ENDED AND PERIODIC INTERRUPT RELATIONSHIP Figure 3



t_{PI} = PERIODIC INTERRUPT TIME INTERNAL PER TABLE 1
t_{BUC} = DELAY TIME BEFORE UPDATE CYCLE = 244 µs

ABSOLUTE MAXIMUM RATINGS*

Voltage on Any Pin Relative to Ground	-0.3V to +7.0V
Operating Temperature	0° to 70°C
Storage Temperature	-40°C to +70°C
Soldering Temperature	260°C for 10 seconds (See Note 7)

This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operation sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect reliability.

RECOMMENDED DC OPERATING CONDITIONS (0°C to 70°C)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Power Supply Voltage	V_{CC}	4.5	5.0	5.5	V	1
Input Logic 1	V_{IH}	2.3		V_{CC}+0.3	V	1
Input Logic 0	V_{IL}	-0.3		0.8	V	1

DC ELECTRICAL CHARACTERISTICS (0°C to 70°C; VCC = 5.0V ± 10%)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Average V_{CC} Power Supply Current	I_{CC1}		7	15	mA	2
Input Leakage	I_{IL}	-1.0		+1.0	µA	3
I/O Leakage	I_{OL}	-1.0		+1.0	µA	4
Input Current	I_{MOT}	-1.0		+500	µA	3
Output @ 2.4V	I_{OH}	-1.0			mA	1,5
Output @ 0.4V	I_{OL}			4.0	mA	1
Write Protect Voltage	V_{TP}	4.0	4.25	4.5	V	

CAPACITANCE (tA = 25°C)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Input Capacitance	C_{IN}			5	pF	
Output Capacitance	C_{OUT}			7	pF	

\C ELECTRICAL CHARACTERISTICS (0°C to 70°C; VCC = 5.0V ± 10%)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Cycle Time	t_{CYC}	385		DC	ns	
Pulse Width, DS/E Low or RD/$\overline{WR}$ High	PW_{EL}	150			ns	
Pulse Width, DS/E High or RD/$\overline{WR}$ Low	PW_{RH}	125			ns	
Input Rise and Fall	t_R, t_F			30	ns	
R/$\overline{W}$ Hold Time	t_{RWH}	10			ns	
R/$\overline{W}$ Setup Time Before DS/E	t_{RWS}	50			ns	
Chip Select Setup Time Before DS, $\overline{WR}$, or $\overline{RD}$	t_{CS}	20			ns	
Chip Select Hold Time	t_{CH}	0			ns	
Read Data Hold Time	t_{DHR}	10		80	ns	
Write Data Hold Time	t_{DHW}	0			ns	
Mux'ed Address Valid Time to ALE Fall	t_{ASL}	30			ns	
Muxed Address Hold Time to ALE Fall	t_{AHL}	10			ns	
Delay Time DS/E to AS/ALE Rise	t_{ASD}	20			ns	
Pulse Width AS/ALE High	PW_{ASH}	60			ns	
Delay Time, AS/ALE to DS/E Rise	t_{ASED}	40			ns	
Output Data Delay Time from DS/E or $\overline{RD}$	t_{DDR}	20		120	ns	6
Data Setup Time	t_{DSW}	100			ns	
Reset Pulse Width	t_{RWL}	5			µs	
$\overline{IRQ}$ Release from DS	t_{IRDS}			2	µs	
$\overline{IRQ}$ Release from $\overline{RESET}$	t_{IRR}			2	µs	

NOTES:

All voltages are referenced to ground.

All Outputs are open.

The MOT pin has an internal pull-down of 20KΩ.

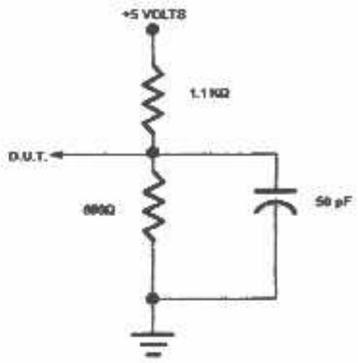
Applies to the AD0-AD7 pins, the $\overline{IRQ}$ pin, and the SQW pin when each is in a high impedance state.

The $\overline{IRQ}$ pin is open drain.

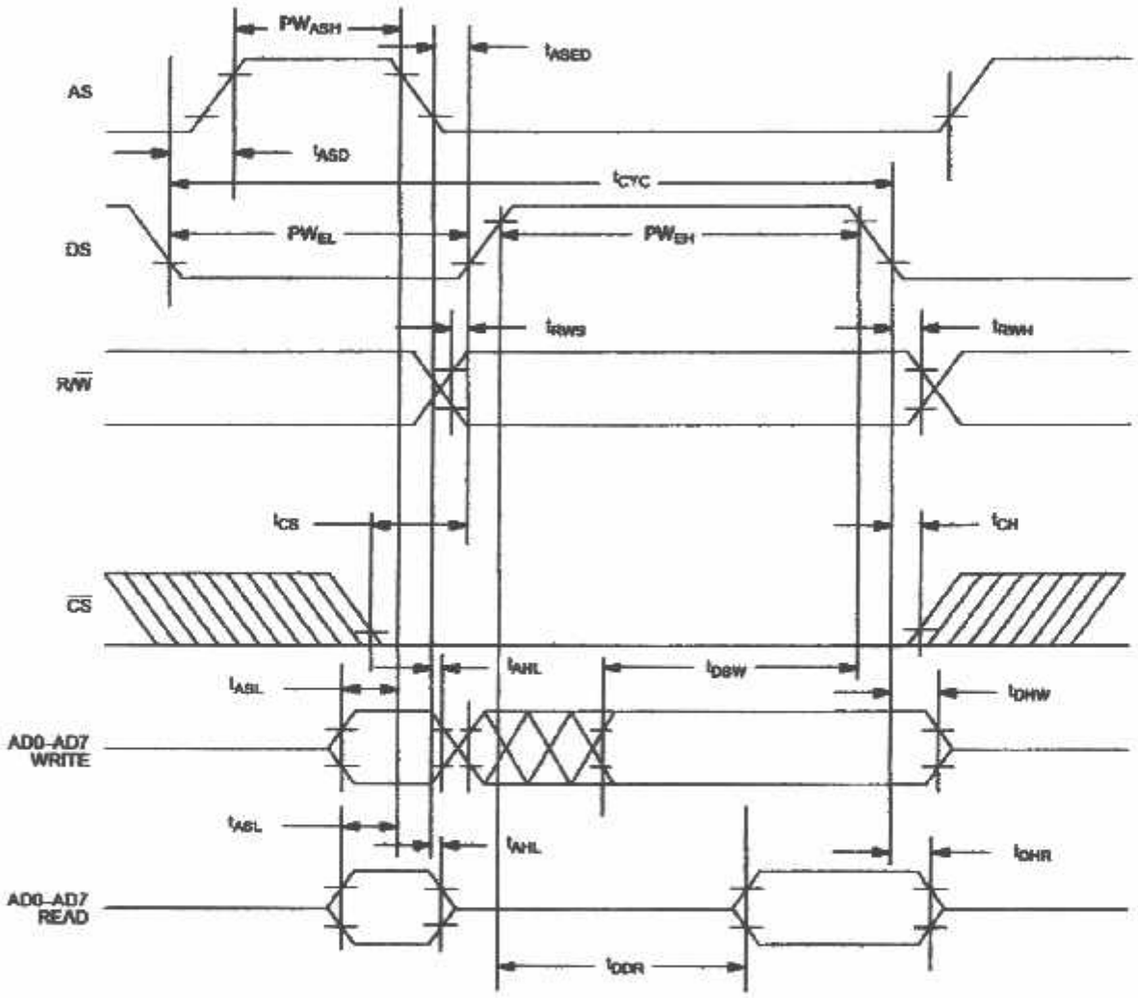
Measured with a load as shown in Figure 4.

Real-Time Clock Modules can be successfully processed through conventional wave-soldering techniques as long as temperature exposure to the lithium energy source contained within does not exceed +85°C. Post solder cleaning with water washing techniques is acceptable, provided that ultrasonic vibration is not used. Such cleaning can damage the crystal.

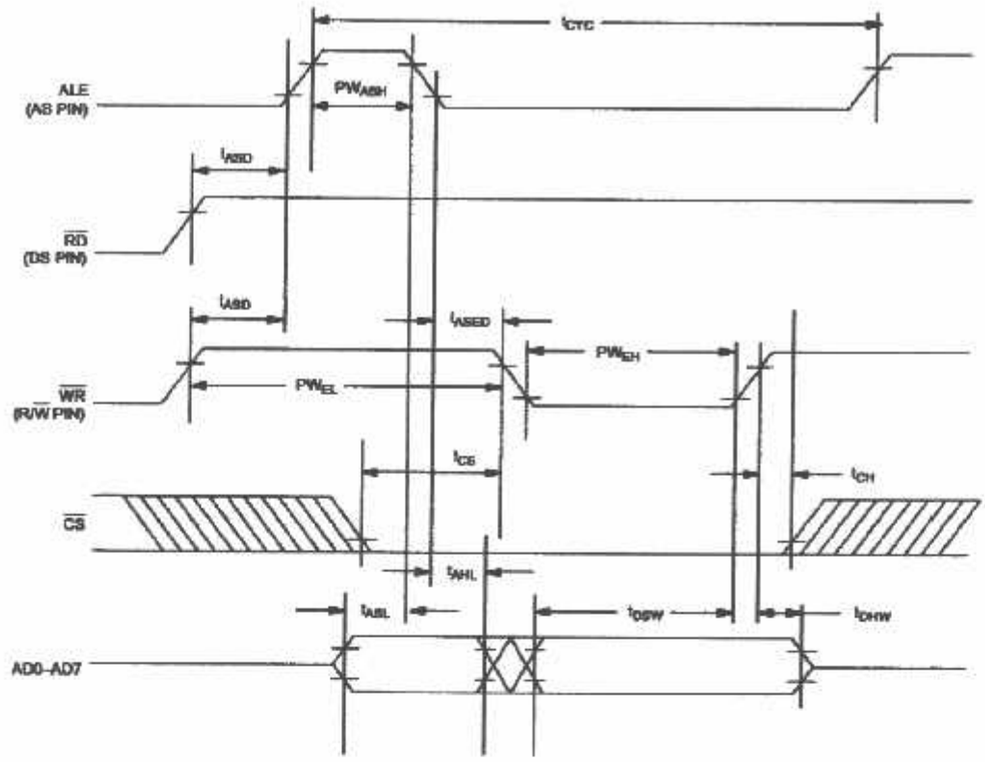
)UTPUT LOAD Figure 4



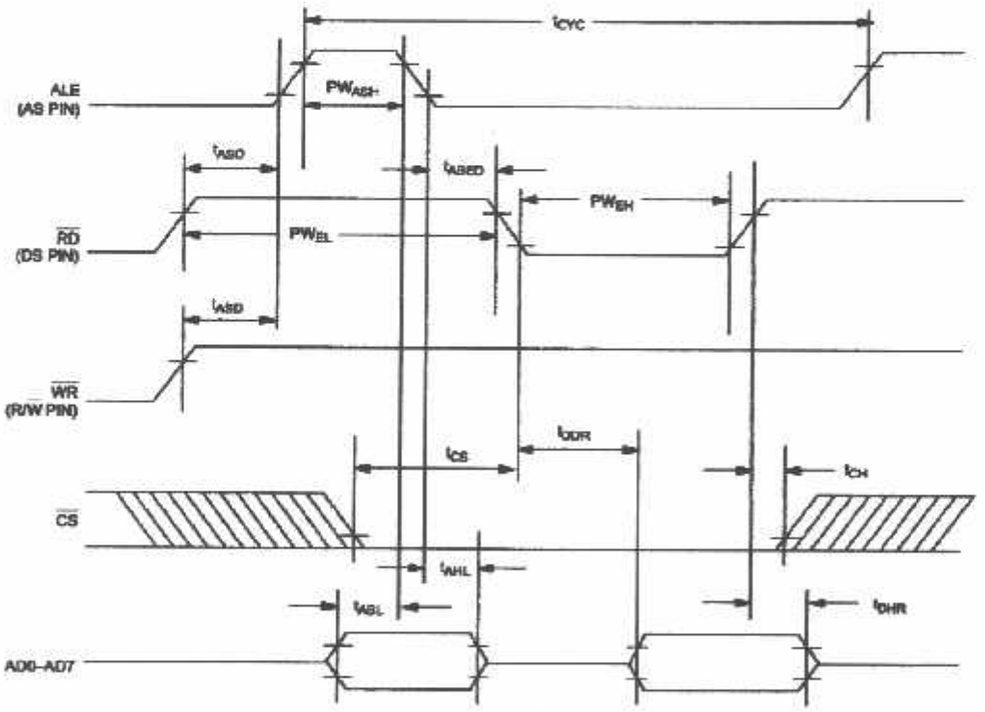
S12C887 BUS TIMING FOR MOTOROLA INTERFACE



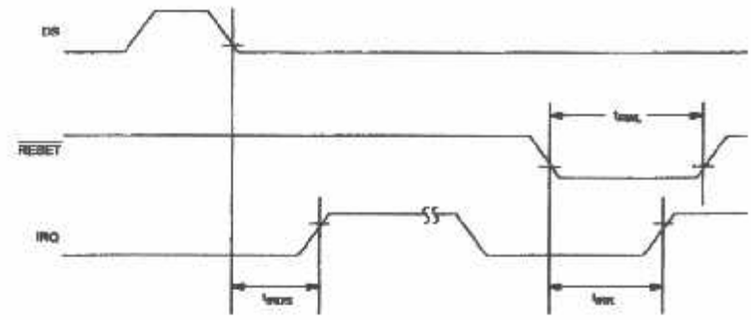
)S12C887 BUS TIMING FOR INTEL INTERFACE WRITE CYCLE



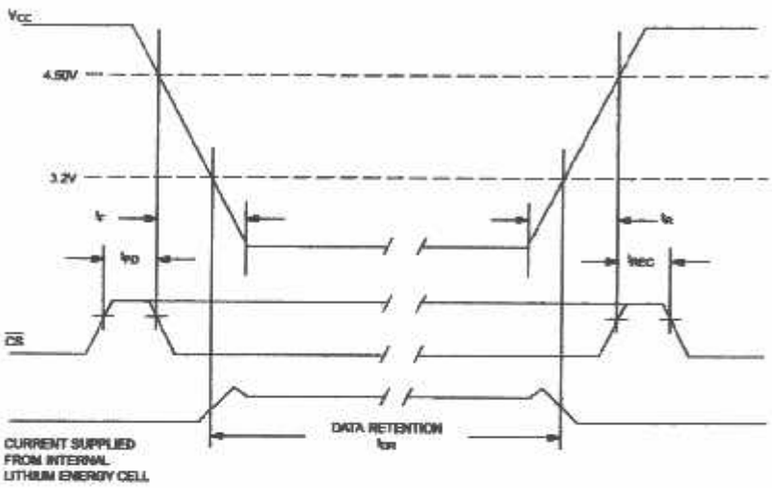
S12C887 BUS TIMING FOR INTEL INTERFACE READ CYCLE



)S12C887 IRQ RELEASE DELAY TIMING



'OWER DOWN / POWER UP TIMING



OWER DOWN / POWER UP TIMING

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
$\overline{CS}$ at V_{IH} before Power-Down	t_{PD}			0	µs	
V_{CC} slew from 4.5V to 0V ($\overline{CS}$ at V_{IH})	t_F $4.0 \le V_{CC} \le 4.5V$	300			µs	
V_{CC} slew from 0V to 4.5V ($\overline{CS}$ at V_{IH})	t_R	100			µs	
$\overline{CS}$ at V_{IH} after Power-Up	t_{REC}	20		200	ms	
Expected Data Retention	t_{DR}	10			years	10,11

(tA=25°C)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Expected Data Retention	t_{DR}	10			years	10,11

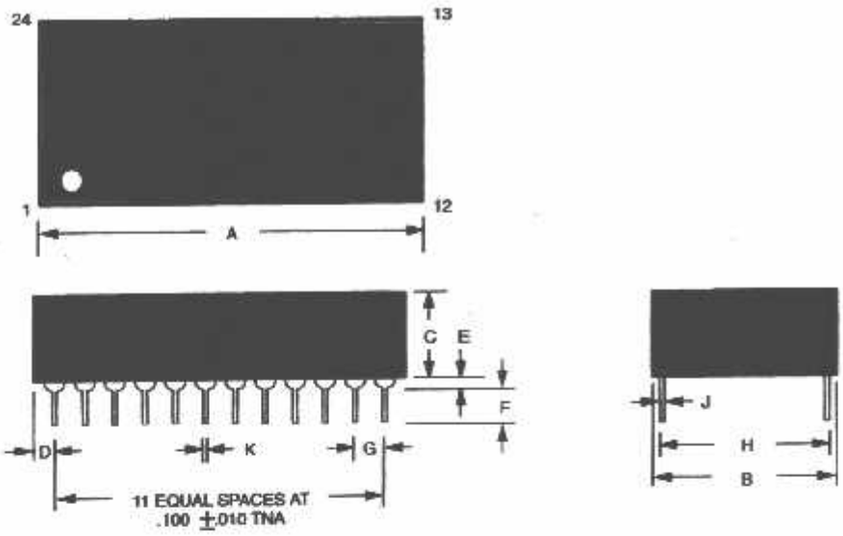
ote:

e real time clock will keep time to an accuracy of ±1 minute per month during data retention time for
: period of t_{DR}.

arning:

ıder no circumstances are negative undershoots, of any amplitude, allowed when device is in battery
:k-up mode.

S12C887 REAL TIME CLOCK PLUS RAM



OTE:

ns 2, 3, 16, 20, 21 and 22 are missing by design

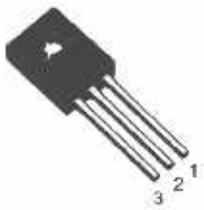
KG	24-PIN	
IM	MIN	MAX
IN	1.320	1.335
IM	33.53	33.91
IN	0.675	0.700
IM	17.15	17.78
IN	0.345	0.370
M	8.76	9.40
IN	0.100	0.130
M	2.54	3.30
IN	0.015	0.030
M	0.38	0.76
IN	0.110	0.140
M	2.79	3.56
IN	0.090	0.110
M	2.29	2.79
IN	0.590	0.630
M	14.99	16.00
IN	0.008	0.012
M	0.20	0.30
IN	0.015	0.021
M	0.38	0.53

BD135
BD139

NPN SILICON TRANSISTORS

Type	Marking
BD135	BD135
BD135-10	BD135-10
BD135-16	BD135-16
BD139	BD139
BD139-10	BD139-10
BD139-16	BD139-16

- STMicroelectronics PREFERRED SALESTYPES



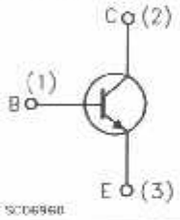
SOT-32

DESCRIPTION

The BD135 and BD139 are silicon Epitaxial Planar NPN transistors mounted in Jedec SOT-32 plastic package, designed for audio amplifiers and drivers utilizing complementary or quasi-complementary circuits.

The complementary PNP types are BD136 and BD140 respectively.

INTERNAL SCHEMATIC DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value		Unit
		BD135	BD139	
V_{CBO}	Collector-Base Voltage (I_E = 0)	45	80	V
V_{CEO}	Collector-Emitter Voltage (I_B = 0)	45	80	V
V_{EBO}	Emitter-Base Voltage (I_C = 0)	5		V
I_C	Collector Current	1.5		A
I_{CM}	Collector Peak Current	3		A
I_B	Base Current	0.5		A
P_{tot}	Total Dissipation at $T_c \leq 25$ °C	12.5		W
P_{tot}	Total Dissipation at $T_{amb} \leq 25$ °C	1.25		W
T_{stg}	Storage Temperature	-65 to 150		°C
T_j	Max. Operating Junction Temperature	150		°C

THERMAL DATA

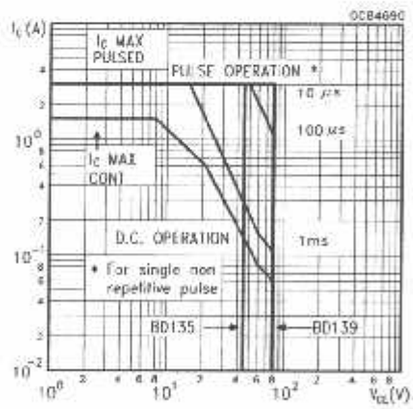
$R_{thj\text{-}case}$	Thermal Resistance Junction-case	Max	10	°C/W

ELECTRICAL CHARACTERISTICS (T_{case} = 25 °C unless otherwise specified)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
I_{CBO}	Collector Cut off Current (I_E = 0)	V_{CB} = 30 V V_{CB} = 30 V T_C = 125 °C			0.1 10	µA µA
I_{EBO}	Emitter Cut-off Current (I_C = 0)	V_{EB} = 5 V			10	µA
$V_{CEO(sus)}$*	Collector-Emitter Sustaining Voltage (I_B = 0)	I_C = 30 mA for **BD135** for **BD139**	 45 80			 V V
$V_{CE(sat)}$*	Collector-Emitter Saturation Voltage	I_C = 0.5 A I_B = 0.05 A			0.5	V
V_{BE}*	Base-Emitter Voltage	I_C = 0.5 A V_{CE} = 2 V			1	V
h_{FE}*	DC Current Gain	I_C = 5 mA V_{CE} = 2 V I_C = 150 mA V_{CE} = 2 V I_C = 0.5 A V_{CE} = 2 V	25 40 25		 250	
h_{FE}	h_{FE} Groups	I_C = 150 mA V_{CE} = 2 V for **BD135/BD139** group-10 for **BD135/BD139** group 16	 63 100		 160 250	

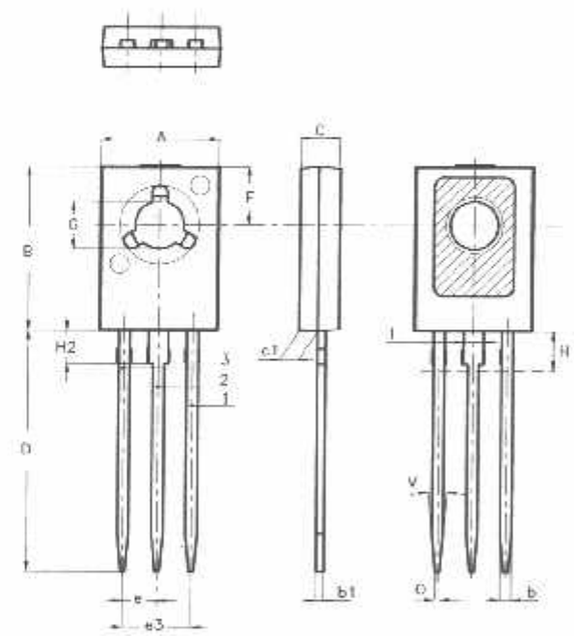
* Pulsed: Pulse duration = 300 µs, duty cycle 1.5 %

Safe Operating Area



SOT-32 (TO-126) MECHANICAL DATA

DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A	7.4		7.8	0.291		0.307
B	10.5		10.8	0.413		0.425
b	0.7		0.9	0.028		0.035
b1	0.40		0.65	0.015		0.025
C	2.4		2.7	0.094		0.106
c1	1.0		1.3	0.039		0.051
D	15.4		16.0	0.606		0.630
e		2.2			0.087	
e3		4.4			0.173	
F		3.8			0.150	
G	3		3.2	0.118		0.126
H			2.54			0.100
H2		2.15			0.084	
I		1.27			0.05	
O		0.3			0.011	
V		10°			10°	



1: Base
2: Collector
3: Emitter

0016114/B