SKRIPSI

PERANCANGAN DAN PEMBUATAN ALAT PENDETEKSI KADAR AMONIAK PADA KAMAR MANDI DENGAN MENGGUNAKAN MIKROKONTROLLER AT89S8252

Disusun Oleh :

YOSSY INDRA KUSUMA

NIM : 03.17.119

JURUSAN TEKNIK ELEKTRO S-1

KOSENTRASI TEKNIK ELEKTRONIKA

FAKULTAS TEKNOLOGI INDUSTRI

INSTITUT TEKNOLOGI NASIONAL MALANG

NOVEMBER 2008

LEMBAR PERSETUJUAN

PERANCANGAN DAN PEMBUATAN ALAT PENDETEKSI KADAR AMONIAK PADA KAMAR MANDI DENGAN MENGGUNAKAN MIKROKONTROLLER AT89S8252

SKRIPSI

Disusun dan diajukan sebagai salah satu syarat untuk memperoleh gelar Sarjana Teknik Elektronika Strata Satu (S-1)

Disusun Oleh :

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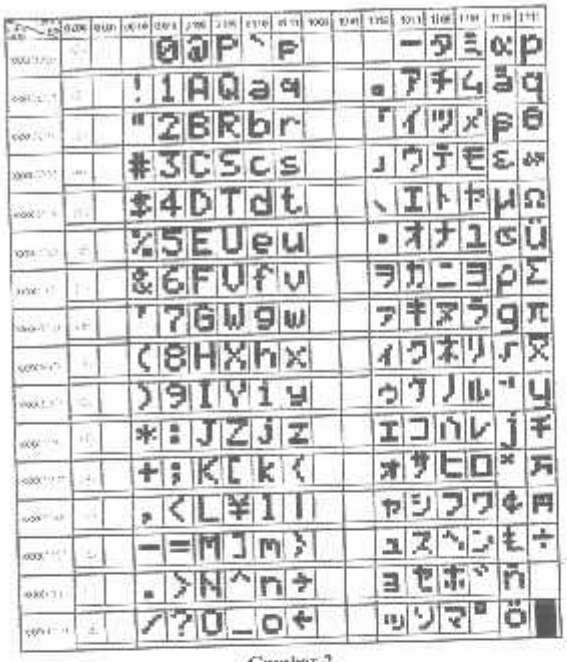
2008



Gambar 2
Hubungan antara CGROM dan DDRAM (diambil dari data sheet HD44780)

Pin Out

No	Nama Pin	Deskripsi
1	VCC	+5V
2	GND	0V
3	VEE	Tegangan Kontras LCD
4	RS	Register Select, 0 = Register Perintah, 1 = Register I
5	R/W	1 = Read, 0 = Write
6	E	Enable Clock LCD, logika 1 setiap kali pengiriman pembacaan data
7	D0	Data Bus 0
8	D1	Data Bus 1
9	D2	Data Bus 2
10	D3	Data Bus 3
11	D4	Data Bus 4
12	D5	Data Bus 5
13	D6	Data Bus 6
14	D7	Data Bus 7
15	Anoda (Kabel coklat untuk LCD Hitachi)	Tegangan positif backlight
16	Katoda (Kabel merah untuk LCD Hitachi)	Tegangan negatif backlight

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JURUSAN TEKNIK ELEKTRO S-1
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Konsentrasi	: Teknik Elektronika
Masa Bimbingan	: 05 Juni 2008 s/d 05 Desember 2008
Judul Skripsi	: Perancangan Dan Pembuatan Alat Pendetaksi Kadar Amoniak Pada Kamar Mandi Dengan Mengunakan Mikrokontroller AT89S8252

Dipertahankan di hadapan Tim Penguji Skripsi Jenjang Strata Satu (S-1) pada :

Hari	: Rabu
Tanggal	: 24 September 2008
Dengan Nilai	: 82,5 (A)

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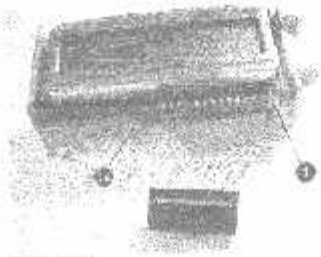
Gambar 3
Pin Out M1632 LCD Hitachi



Gambar 4
Pin Out LCD M1632 Standard

Register

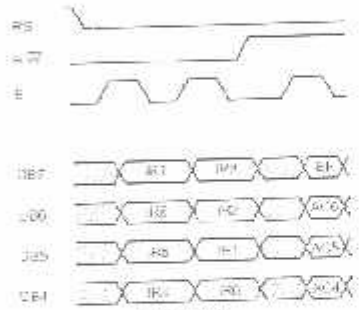
HD44780, mempunyai dua buah Register yang aksesnya diatur dengan menggunakan kaki Pada saat RS berlogika 0, maka register yang diakses adalah Register Perintah dan pada saat RS berlog 1, maka register yang diakses adalah Register Data

Register Perintah

Register ini adalah register di mana perintah-perintah dari mikrokontroler ke HD44780 pada proses penulisan data atau tempat status dari HD44780 dapat dibaca pada saat pembacaan data.

Penulisan Data ke Register Perintah

Penulisan data ke Register Perintah dilakukan dengan tujuan mengatur tampilan LCD, misalk dan mengatur Address Counter maupun Address Data. Gambar 5 menunjukkan proses penulisan data register perintah dengan menggunakan mode 4 bit interface. Kondisi RS berlogika 0 menunjukkan al data ke Register Perintah. RW berlogika 0 yang menunjukkan proses penulisan data akan dilakukan. Nib tinggi (bit 7 sampai bit 4) terlebih dahulu dikirimkan dengan diawali pulsa logika 1 pada E Clo Kemudian Nibble rendah (bit 3 sampai bit 0) dikirimkan dengan diawali pulsa logika 1 pada E Clock L Untuk mode 8 bit interface, proses penulisan dapat langsung dilakukan secara 8 bit (bit 7 ... bit 0) diawali sebuah pulse logika 1 pada E Clock.



Gambar 5
Timing diagram Penulisan Data ke Register Perintah Mode 4 bit Interface

Tabel 1
Perintah-perintah M1632

Perintah	D7	D6	D5	D4	D3	D2	D1	D0	Deskripsi
Hapus Display	0	0	0	0	0	0	0	1	Hapus Display dan DD RAM
Posisi Awal	0	0	0	0	0	0	1	X	Set Alamat DDRAM ke 0
Set Mode	0	0	0	0	0	1	I/D	S	Atur arah pergeseran cursor dan displ

ABSTRAKSI

PERANCANGAN DAN PEMBUATAN ALAT PENDETEKSI KADAR AMONIAK PADA KAMAR MANDI DENGAN MENGGUNAKAN MIKROKONTROLLER AT89S8252

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Jln. Raya Karanglo Km 2 Malang

Dosen Pembimbing : **Ir. Teguh Herbasuki, MT**
M. Ashar, ST, MT

Kata Kunci : Amoniak, TGS 826.

Banyak dijumpai kamar mandi pada pusat-pusat perbelanjaan dewasa ini yang masih terkesan kotor terutama pada masalah bau yang disebabkan oleh urine, sehingga konsumen mengeluhkan keadaan tersebut.

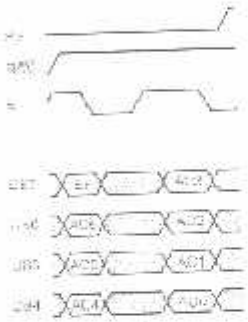
Oleh karena itu diperlukan suatu alat yang bisa mendeteksi kadar amoniak sekaligus sebagai pembersih pada kamar mandi secara otomatis menggunakan mikrokontroller AT89S8252 untuk mengatasi bau amoniak yang mengganggu pada kamar mandi. Desain cara kerja sistem adalah sebagai berikut: Sensor TGS 826 mendeteksi kadar amoniak, output dari sensor diubah dalam bentuk digital oleh ADC 0804 kemudian mikro mengolah data serta memprosesnya yang kemudian memberikan instruksi pada fan, pengharum, kran pembilas. Hasil pengujian alat diperoleh error rata-rata sebesar 0.37%.

Display On/OFF	0	0	0	0	1	D	C	B	Atur display (D) On/OFF, cursor ON/OFF, (C) blinking (B)
Geser Cursor/Display	0	0	0	1	S/C	R/L	X	X	Geser Cursor atau display tanpa merubah alamat DDRAM
Set Fungsi	0	0	1	DL	N	F	X	X	Atur panjang data, jumlah baris yang tampil, dan font karakter
Set Alamat CGRAM	0	1	ACG	ACG	ACG	ACG	ACG	ACG	Data dapat dibaca atau ditulis setelah alamat diatur
Set Alamat DDRAM	0	1	ADD	ADD	ADD	ADD	ADD	ADD	Data dapat dibaca atau ditulis setelah alamat diatur

X = diabaikan
I/D 1=Increment, 0=Decrement
S 0=Display tidak geser
S/C 1=Display Shift, 0=Geser Cursor
R/L 1=Geser Kiri, 0=Geser Kanan
DL 1=8 bit, 0=4bit
N 1=2 baris, 0=1 baris
F 1=5x10, 0=5x8
D 0=Display OFF, 1=Display ON
C 0=Cursor OFF, 1=Cursor ON
B 0=Blinking OFF, 1=Blinking ON

Pembacaan Data dari Register Perintah

Proses pembacaan data pada register perintah biasa digunakan untuk melihat status busy dari L atau membaca Address Counter. RS diatur pada logika 0 untuk akses ke Register Perintah, R/W diatur p logika 1 yang menunjukkan proses pembacaan data. 4 bit nibble tinggi dibaca dengan diawali pulsa log 1 pada E Clock dan kemudian 4 bit nibble rendah dibaca dengan diawali pulsa logika 1 pada E Clo Untuk Mode 8 bit interface, pembacaan 8 bit (nibble tinggi dan rendah) dilakukan sekaligus dengan dias sebuah pulsa logika 1 pada E Clock.



Gambar 6
Timing Diagram Pembacaan Register Perintah Mode 4 bit Interface

Register Data

Register ini adalah register di mana mikrokontroler dapat menuliskan atau membaca data ke dari DDRAM. Penulisan data pada register ini akan menempatkan data tersebut ke DDRAM sesuai den alamat yang telah diatur sebelumnya

Penulisan Data ke Register Data

Penulisan data pada Register Data dilakukan untuk mengirimkan data yang akan ditampilkan pa LCD. Proses diawali dengan adanya logika 1 pada RS yang menunjukkan akses ke Register Data, kondisi R/W diatur pada logika 0 yang menunjukkan proses penulisan data. Data 4 bit nibble tinggi (bit 7 hingga

KATA PENGANTAR

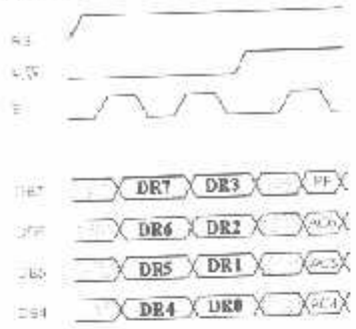
Alhamdulillah, puji syukur kehadirat-Mu Ya Allah yang telah memberikan rahmat dan hidayah-Mu, sehingga saya dapat menyelesaikan skripsi yang berjudul **"Perancangan Dan Pembuatan Alat Pendeteksi Kadar Amoniak Pada Kamar Mandi Dengan Menggunakan Mikrokontroller AT89S8252"** ini dengan lancar. Skripsi ini merupakan persyaratan kelulusan Studi di Jurusan Teknik Elektro S-1 Konsentrasi Teknik Elektronika ITN Malang dan untuk mencapai gelar Sarjana Teknik.

Keberhasilan peyelesaian laporan skripsi ini tidak lepas dari dukungan dan bantuan berbagai pihak. Untuk itu penulis menyampaikan terima kasih kepada :

1. Bapak Prof. Dr. Eng. Ir. Abraham Lomi, MSEE selaku Rektor ITN Malang.
2. Bapak Ir. Mochtar Asroni, MSME selaku selaku Dekan Fakultas Teknologi Industri.
3. Bapak Ir. F. Yudi Limpraptono, MT selaku Ketua Jurusan Teknik Elektro S-1.
4. Bapak Ir.Teguh Herbasuki, MT selaku Dosen Pembimbing I.
5. Bapak M. Ashar, ST, MT selaku Dosen Pembimbing II.
6. Kedua orang tuaku dan saudaraku yang telah memberikan dukungan.
7. Semua temen – temen dan someone yang aku sayang yang telah membantu dalam penyelesaian penyusunan skripsi ini.

Penulis telah berusaha semaksimal mungkin dan menyadari sepenuhnya akan keterbatasan pengetahuan dalam menyelesaikan laporan ini. Untuk itu

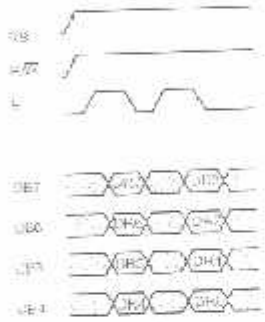
bit 4) dikirim dengan diawali pulsa logika 1 pada sinyal E Clock dan kemudian diikuti 4 bit nibble rendah (bit 3 hingga bit 0) yang juga diawali pulsa logika 1 pada sinyal E Clock.



Gambar 7
Timing Diagram Penulisan Data ke Register Data Mode 4 bit Interface

Pembacaan Data dari Register Data

Pembacaan data dari Register Data dilakukan untuk membaca kembali data yang tampil p LCD. Proses dilakukan dengan mengatur RS pada logika 1 yang menunjukkan adanya akses ke Regi Data. Kondisi R/W diatur pada logika tinggi yang menunjukkan adanya proses pembacaan data. Data 4 nibble tinggi (bit 7 hingga bit 4) dibaca dengan diawali adanya pulsa logika 1 pada E Clock dan diikuti dengan data 4 bit nibble rendah (bit 3 hingga bit 0) yang juga diawali dengan pulsa logika 1 pada h Clock



Gambar 8
Timing Diagram Pembacaan Data dari Register Data Mode 4 bit Interface

Antar muka LCD dengan mikrokontroler

Penulis mengharapkan saran dan kritik yang membangun dari pembaca demi kesempurnaan laporan ini.

Harapan penulis semoga laporan skripsi ini memberikan manfaat bagi perkembangan ilmu pengetahuan dan pembaca.

Malang, September 2008

Penulis

Gambar 9
Antar muka dengan Modul DST-51

Gambar 10
Antar Muka dengan Modul SC-51 atau AT8951

Program
Rutin-rutin Program untuk DST-51 yang diassembly dengan ALIDS atau ASM51
Rutin-rutin Program untuk SC-51/AT8951 yang diassembly dengan ALIDS atau ASM51
Rutin delay yang diassembly dengan ALIDS atau ASM51
Datasheet HD44780

DAFTAR ISI

INSTITUT TEKNOLOGI NASIONAL MALANG
FAKULTAS TEKNOLOGI INDUSTRI
JURUSAN TEKNIK ELEKTRO

Nilai Ujian Skripsi

Nama Mahasiswa : Yussy Indra K / Nim : 0317 119
Fakultas / Jurusan : Teknologi Industri / Teknik Elektro
Konsentrasi : T. Energi Listrik / T. Elektronika / T. Infokom S-I

No	Indikator Penilaian	Nilai
1.	**Penguasaan materi skripsi :** • Ketajaman perumusan masalah dan tujuan penelitian • Ketepatan metode yang digunakan • Ketepatan penarikan kesimpulan dengan tujuan dan hasil penelitian	
2.	**Penguasaan materi penunjang Skripsi / tinjauan pustaka :** • Relevansi, kemuktakhiran dan penyusunan daftar pustaka	
3.	**Konstribusi hasil penelitian** • Manfaat hasil penelitian bagi pengembangan IPTEKS, pembangunan dan atau pengembangan kelembagaan	
	Nilai rata-rata	

Catatan :
1. Nilai diberikan dalam bentuk angka dengan kisaran : 0 sampai dengan 100
2. Nilai komulatip dari penguji kurang dari 56 peserta ujian dinyatakan tidak lulus

Malang, _____ 200

Moderator / Dosen Pembimbing

(_____)

Dosen Penguji

(_____)

*) Coret yang tidak perlu

BAB IV: PENGUJIAN ALAT

DAFTAR GAMBAR

DAFTAR TABEL

BAB I

PENDAHULUAN

1.1. Latar Belakang

Perkembangan teknologi pada dewasa ini sudah sedemikian pesatnya dengan dukungan ilmu teknik elektronika. Teknologi menjadi suatu media penerapan yang membantu manusia dalam hampir seluruh aspek kehidupan. Salah satunya dalam bidang kebersihan. Belakangan ini banyak dibangun tempat-tempat perbelanjaan.yang saling berlomba dalam memberikan pelayanan yang memuaskan bagi konsumen. Pelayanan tersebut tidak hanya berupa transaksi jual beli tetapi juga pelayanan dalam hal kebersihan khususnya kebersihan pada kamar mandi. Banyak dijumpai kamar mandi pada pusat-pusat perbelanjaan dewasa ini yang masih terkesan kotor terutama pada masalah bau yang disebabkan oleh urine, sehingga banyak konsumen mengeluhkan keadaan tersebut. Selain itu dalam penanganan kebersihan masih sering terjadi ketidak-tanggapan petugas kebersihan khususnya pada kebersihan kamar mandi..

Oleh karena itu diperlukan suatu alat yang bisa mendeteksi kadar amoniak sekaligus sebagai pembersih pada kamar mandi secara otomatis. Hal itu menggunakan mikrokontroller sebagai pengendali utama dari sistem, pengolah data, dan pemberi instruksi sesuai dengan keadaan.

Alat yang digunakan menggunakan sensor sebagai cara kerja alat tersebut. Sensor yaitu suatu alat yang mengubah besaran non elektris menjadi besaran elektris, sehingga dapat dilakukan pengukuran secara analog. Dari besaran analog

dapat diubah menjadi besaran digital dengan menggunakan converter analog ke digital (ADC) yang selanjutnya di hubungkan pada mikrokontroller sebagai pengolah data.

Dengan pemikiran tersebut dibuat suatu alat yang mudah, terjangkau, serta dapat memudahkan dalam proses pendeteksian dan pembersih pada kamar mandi.

1.2. Rumusan masalah

Mengacu pada permasalahan yang telah diuraikan pada latar belakang, maka rumusan masalah dapat disusun sebagai berikut :

1. Bagaimana merancang dan membuat alat pendeteksi kadar amoniak dan pembersih pada kamar mandi menggunakan mikrokontroller AT89S8252.
2. Bagaimana cara sensor mendeteksi kadar amoniak pada kamar mandi secara otomatis.

1.3. Tujuan

Tujuan dari pembahasan skripsi ini adalah Perancangan dan pembuatan alat pendeteksi kadar amoniak pada kamar mandi dengan menggunakan mikrokontroller AT89S8252.

1.4. Batasan Masalah

Dengan mengacu pada permasalahan yang telah dirumuskan, maka hal-hal yang berkaitan dengan alat yang dibuat, diberi batasan berikut :

1. Sensor amoniak mendeteksi kadar amoniak antara 30 ppm- 300 ppm.
2. Sistem ini digunakan untuk satu buah kamar mandi.
3. Mikrokontroller yang digunakan adalah AT89S8252.
4. Tidak membahas perancangan dan pembuatan catu daya.

1.5. Metodologi

Metodologi penulisan yang dipakai dalam pembuatan skripsi ini adalah :

- Studi Literatur.
- Perancangan dan pembuatan alat.
- Pelaksanaan uji coba alat.
- Penyusunan Laporan Skripsi.

1.6. Sistematika Penulisan

Penulisan skripsi ini terbagi dalam lima bab dengan sistematika sebagai berikut:

BAB I PENDAHULUAN

Membahas tentang latar belakang permasalahan,rumusan masalah,tujuan, batasan masalah,metodologi penulisan serta sistematika susunan penulisan dari buku skripsi ini

BAB II TEORI

Bab ini berisikan tentang teori-teori penunjang yang digunakan dalam perencanaan dan pembuatan skripsi.

BABIII PERANCANGAN DAN PEMBUATAN ALAT

Membahas tentang perancangan alat baik perangkat keras maupun perangkat lunak, serta cara kerja blok diagram.

BAB IV PENGUJIAN ALAT

Mencakup pembahasan tentang proses pengujian alat yang terdiri dari peralatan yang digunakan, langkah kerja dan analisa hasil pengujian.

BAB V PENUTUP

Berisi kesimpulan dan saran

BAB II

TINJAUAN PUSTAKA

2.1. Sensor Amoniak (TGS826)

Sensor yang digunakan dalam pendeteksi kadar Amoniak ini adalah Sensor *TGS826*. Sensor ini sangat sensitif dengan amoniak, dan sensor ini dapat mendeteksi kadar amoniak dari *30ppm-300ppm* dalam udara dan secara ideal merupakan batas keselamatan yang berhubungan dengan aplikasi seperti deteksi kadar amoniak pada sistem pendingin dan deteksi amoniak pada lahan pertanian.

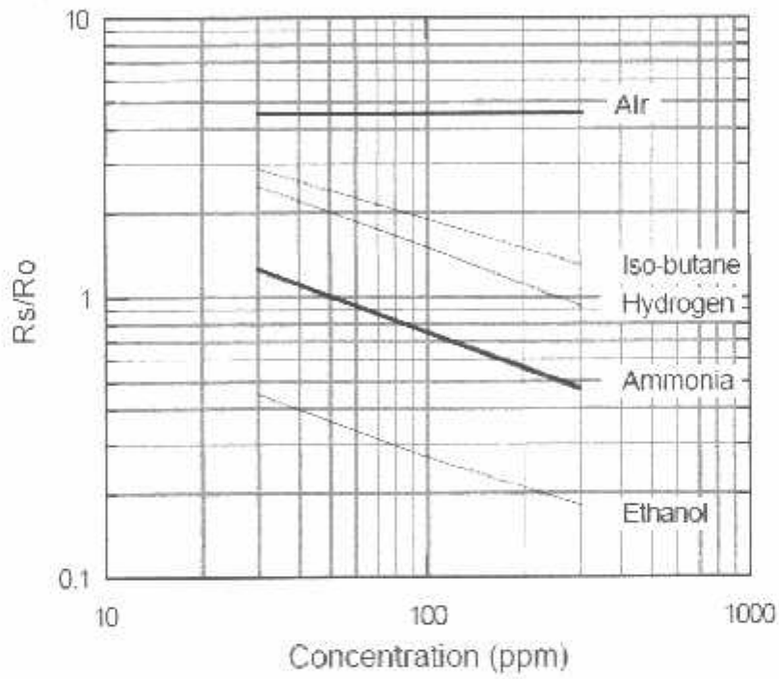
Elemen sensor TGS 826 adalah *metal oxide semiconductor* yang mempunyai konduktivitas yang rendah di udara bersih. Dalam kemampuan pendeteksian gas konduktifitas sensor bertambah tergantung konsentrasi gas pada udara. Sebuah rangkaian listrik sederhana dapat mengkonversikan perubahan konduktivitas kedalam sebuah signal *output* yang sesuai dengan konsentrasi gas.

Gambar 2.1 *Sensor TGS826* / Sensor Amoniak

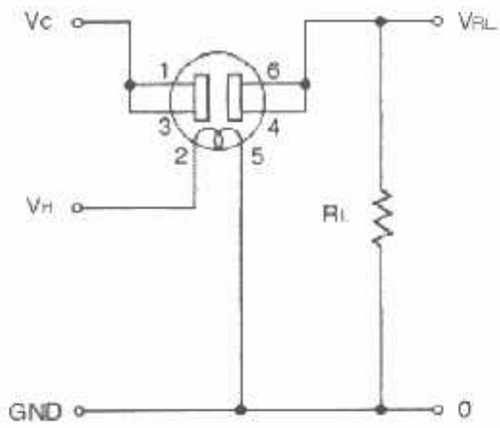
Gambar dibawah ini menjelaskan karakteristik dari sensitivitas sensor, semua data diambil pada kondisi Standard. Garis (Y) diindikasikan sebagai sensor *resistance ratio* (Rs/Ro) yang didefinisikan sebagai berikut:

- Rs = Resistansi sensor dari gas-gas yang ditampilkan dalam berbagai macam konsentrasi.
- Ro = Resistansi sensor dalam 50 ppm amoniak.

Sensitivity Characteristics:



Gambar 2.2 ***Sensitivity characteristics TGS826***



Gambar 2.3 ***Basic measuring circuit***

Apabila sensor memiliki polaritas tegangan DC selalu diperlukan untuk tegangan rangkaian. Apabila sensor dihubungkan seperti yang ditunjukkan pada gambar diatas maka *output* yang melewati *load resistor* (VRL) bertambah sedangkan resistansi sensor (Rs) berkurang tergantung pada konsentrasi gas.

- Resistansi sensor dihitung dengan rumus seperti berikut:

$$Rs = \left(\frac{Vc}{Vrl} - 1\right) \times RL$$

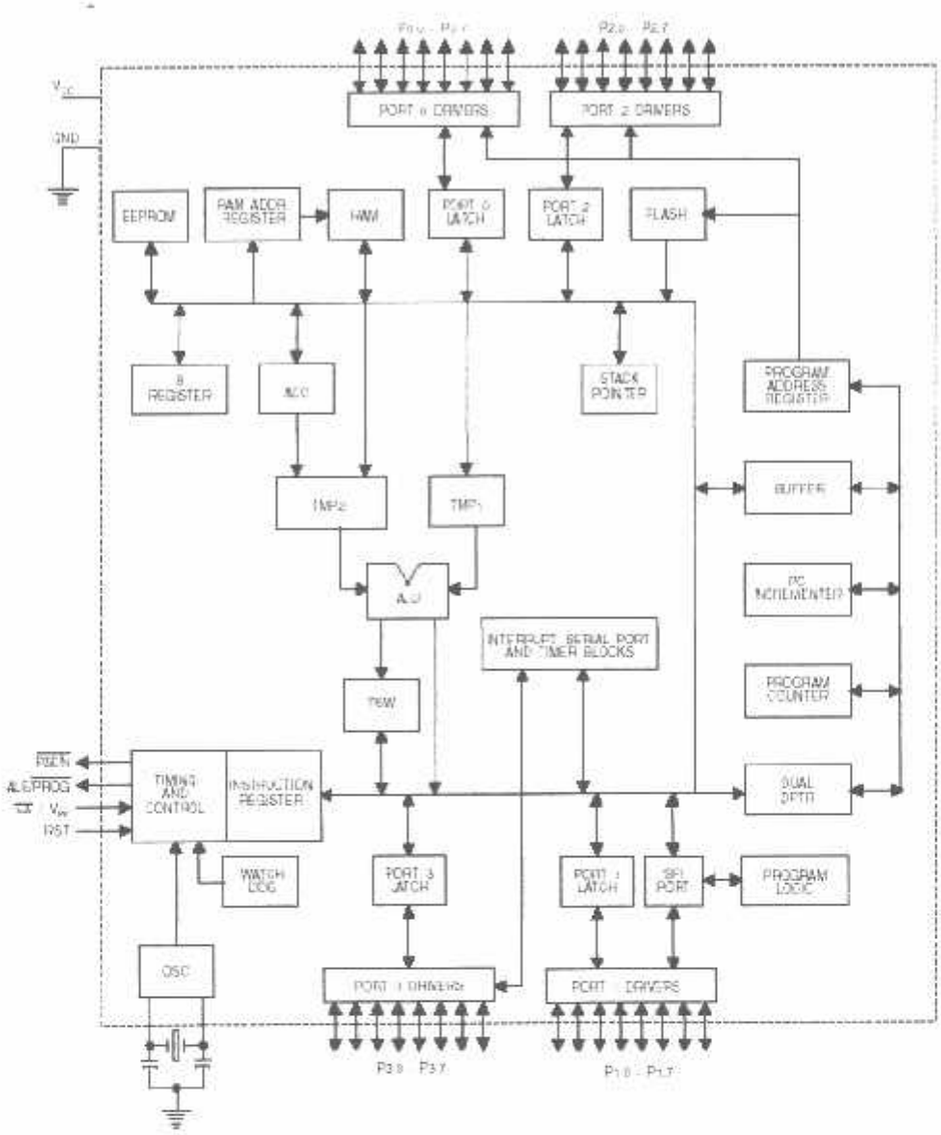
2.2. *Mikrokontroller* AT89S8252

Perbedaan mendasar antara mikrokontroller dan mikroprosesor adalah jika mikrokontroller selain memiliki CPU *(Central Processing Unit)* juga dilengkapi dengan memori dan I/O *(Input/Output)*. Maka mikrokontroller dapat dikatakan sebagai *microcomputer* dalam keping tunggal *(single chip microcomputer) yang* dapat berdiri sendiri.

Mikrokontroller AT89S8252 adalah mikrokontroller keluarga MCS-51 yang membutuhkan daya rendah, memiliki kemampuan yang tinggi, dan merupakan mikrokomputer 8 bit yang dilengkapi 8K *byte Flash* PEROM *(Programmable and Erasable Read Only Memory)* yaitu ROM yang dapat ditulis ulang atau dihapus menggunakan sebuah perangkat *programmer*. Serta terdapat EEPROM *internal* sebesar 2k *Byte*.

Flash PEROM dalam AT89S8252 menggunakan *Atmel 's High-Density Non Volatile Technology* yang mempunyai kemampuan untuk ditulis ulang hingga 1000 kali dan berisikan perintah *standard* MCS-51. Selain itu juga dilengkapi RAM *internal* sebesar 256 *byte*. Dalam sistem Mikrokontroller terdapat dua hal yang mendasar, yaitu perangkat keras dan perangkat lunak yang keduanya saling terkait dan mendukung.

2.2.1. Perangkat Keras *Mikrokontroller* AT89S8252



Gambar 2.4
Blok Diagram *Mikrokontroller* AT89S8252
Sumber : Belajar *Mikrokontroller* ATMEL AT89S8252

Mikrokontroller AT89S8252 secara umum memiliki:

- CPU 8 bit
- 8 Kbyte FLASH PEROM
- 2 Kbyte EEPROM
- *Memory* 256 x 8 bit *Internal* RAM
- 32 Port I/O *Lines*
- 3 *Timer* dan *Counter* 16 bit
- 9 Sumber Interupsi
- SPI serial interface
- Oscillator dan clock maksimal 24 MHz
- *Programmable Watchdog Timer*
- *Programmable UART Serial Chanel*
- *Dual Data Pointer*
- *Power-Off Flag*

2.2.2. Arsitektur AT89S8252

Arsitektur Mikrokontroller AT89S8252 adalah sebagai berikut :

1. CPU *(Central Processing Unit)* 8 bit dengan *register A (Accumulator)* & B.
2. 16-bit *Program Counter* (PC) dan *(Data Pointer)* DTPR.
3. 8-bit *Program Status Word (PSW)*.
4. 8-bit *Stack Pointer (SP)*.
5. 8 *Kbyte* Flash PEROM *internal*.
6. 256 *byte internal* RAM.

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4. 8-bit *Stack Pointer (SP)*.
5. 8 *Kbyte* Flash PEROM *internal*.
6. 256 *byte internal* RAM.

- 4 bank *register*, masing-masing berisi *8 register*.
- 16 *byte* yang dapat dialamati pada *bit-level*.
- 208 byte *general purpose memory data*.

7. 32 pin *input-output* tersusun atas P0-P3, masing-masing 8-bit.
8. 3 buah *timer (T0 & T1)* dengan masing-masing 16-bit *timer/counter*.
9. *Receiver/transmiter data* secara *serial full duplex: Serial buffer* (SBUF).
10. *Control register* : TCON, TMOD, SCON, PCON, IP & IE.
11. 9 buah *sumber* interupsi (4 buah sumber interupsi *external* dan *5* buah sumber interupsi *internal*).
12. *Oscillator* dan *clock internal*.

2.2.3. Organisasi Memori

Dalam mikrokontroller AT89S8252 ruang alamat telah dibedakan untuk program memori dan data memori.

2.2.3.1. *Internal Program Memory*

Mikrokontroller AT89S8252 memiliki program memori *internal* sebesar 8 Kbyte dengan ruang alamat 0000H-0FA0H. Jika alamat-alamat program lebih tinggi dari pada 0FA0H dimana melebihi kapasitas ROM *internal*, menyebabkan AT89S8252 secara otomatis mengambil kode byte dari program memori *external*. Kode *byte* juga dapat diambil hanya dari memori *external* dengan alamat 0000H-FFFFH dengan cara menghubungkan pin EA ke *ground*.

2.2.3.2. *Random Access Memory* (RAM)

Ruangan alamat memory data *internal* (RAM) dengan kapasitas 256 *byte* yaitu : 00H-FFH yang terbagi atas 3 daerah, yaitu :

1. Empat *bank register*

   Setiap *bank* terdiri dari *8 register* (R0-R7) sehingga jumlah *register* untuk ke-empat *bank register* menjadi 32 buah *register* yang menempati ruang alamat 00H-1FH. Mengaktifkan salah satu *bank register* dapat dilakukan dengan mengatur RS0-RS1 pada *Program Status Word (PSW)*.

2. Bit Addressable

   Terdiri dari *16 byte* yang berada pada alamat 20H-2FH. Masing-masing bit dalam 208 bit yang lokasinya dapat dialamati secara langsung.

3. RAM Keperluan Umum

   Terdiri atas 208 *byte* yang menempati alamat 30H-FFH, dan dapat dialamati secara langsung maupun tak langsung dalam penggunaan untuk keperluan umum *(general purpose)*.

Table 2.1
Pengaturan RS0-RS1 *Bank Register*

RS1	RS0	Register Bank Select Bits
0	0	Bank 0
0	1	Bank 1
1	0	Bank 2
1	1	Bank 3

Sumber : Belajar Mikrokontroller ATMEL AT89S8252

2.2.3.3. SFR *(Special Function Register)*

Untuk operasi AT89S8252 yang menggunakan alamat internal RAM (00H-FFH). Beberapa dari *register-register* ini juga mampu dengan pengalamatan bit sehingga dapat dioperasikan seperti *yang* ada pada RAM.

2.2.3.3.1. PSW *(Program Status Word)*

Cara mendefenisikannya *register* ini ditunjukkan dalam tabel 2.4 :

Tabel 2.2
Pengaturan Register PSW

Data	Simbol	Posisi	Fungsi /Art-1
D0	P	PSW.0	*Parity flag*
D1	-	PSW.1	*Flag* didefinisikan oleh pemakai.
D2	OV	PSW.2	*Overflow Flag*
D3	RS0	PSW.3	Bit pemilih *bank register*.
D4	RS1	PSW.4	Bit pemilih *bank register*.
D5	F0	PSW.5	*Flag 0*
D6	AC	PSW.6	*Auxiliary CarryFlag*
D7	CY	PSW.7	*Carry Flag*

Sumber : Belajar Mikrokontroller ATMEL AT89S8252

2.2.3.3.2. PCON *(Power Control)*

Untuk *register* cara mendefenisikannya ditunjukkan dalam tabel 2.3 :

Tabel 2.3
Skema Medefinisikan PCON

Data	Simbol	Fungsi /Arti
D0	IDL	*Idle* mode bit
D1	PD	*Power Down* bit
D2	GF0	*Bit flag* serbaguna.
D3	GF1	Bit *flag* serbaguna.
D4	-	Tidak dipakai.

D5	-	Tidak dipakai.
D6	-	Tidak dipakai.
D7	SMOD	Digunakan untuk menghasilkan *baudrate* dan SMOD_1, maka *baudrate* akan *double* baik mode 0,1,2 atau 3.

Sumber : Belajar Mikrokontroller ATMEL AT89S8252

2.2.3.3.3. Sistem Interupsi

Mikrokontroller AT89S8252 mempunyai 9 buah sumber interupsi yang dapat mengakibatkan permintaan interupsi, yaitu INT0, INT1, T0, T1 port serial dan beberapa port lainnya. Saat terjadi interupsi mikrokontroller secara otomatis akan menuju ke *subrutin* pada alamat tersebut. Setelah interupsi *service* selesai dikerjakan, Mikrokontroller akan mengerjakan program semula. Sumber interupsi *external* adalah INT0, INT1, dimana kedua interupsi *external* ini akan aktif pada transisi rendah selain itu juga ada *Timer/Counter 0, Timer/Counter 0* dan interupsi dari port serial *(receiver)*. Interupsi serial dibangkitkan dengan melakukan operasi OR pada R1 dan T1. Tiap-tiap sumber interupsi dapat *di-enable* atau *di-disable* secara *software*. Tingkat prioritas semua sumber interupsi dapat diprogram sendiri-sendiri dengan *set* atau *clear* bit pada SFRS IP *(Interrupt Priority)*.

Tabel 2.4
Alamat Sumber Interupsi

Sumber Interupsi	Alamat Awal
Power On Reset	0000h
Interrupt luar 0 (INT 0)	0003h
Pewaktu/ pencacah 0 (T0)	000Bh
Interrupt luar 1 (INT 1)	0013h
Pewaktu/ pencacah 1 (T1)	001Bh
Port 110 *Serial*	0023h

Sumber : Belajar Mikrokontroller ATMEL AT89S8252

Register yang berperan dalam mengatur aktif tidaknya interupsi adalah *interrupt enable register*, susunan dari bit-bit beserta kegunaannya adalah :

Tabel 2.5
Kegunaan *Interrupt Enable Register*

Data	Simbol	Posisi	Fungsi /Arti
D0	EX0	IE.0	Diatur secara *software* untuk interupsi dari INT1.
D1	ET0	IE.1	Diatur secara *software* untuk interupsi dari *timer/counter* 1.
D2	EX 1	IE.2	Diatur secara *software* untuk interupsi dari INT 1.
D3	ET1	IE.3	Diatur secara *software* untuk interupsi dari *timer/counter*1.
D4	ES	IE.4	Untuk mengatur *enable* atau *disables* atau interupsi R1/T1.
D5	-	IE.5	Kosong
D6	-	IE.6	Kosong
D7	EA	IE.7	Jika diatur 0 maka semua interupsi *di-disable*, jika diatur 1 maka interupsi diatur *di-disable* atau *di-enable* menurut masing-masing bit.

Sumber : Belajar Mikrokontroller ATMEL AT89S8252

2.2.3.3.4. *Timer/Counter*

Pengendalian kerja dari *timer/counter* dilakukan dengan pengaturan register yang berhubungan dengan kerja dari *timer/counter* yaitu melalui sebuah *timer/counter mode control*. Untuk mengaktifkan *timer/counter* yang meliputi penentuan fungsi sebagai *timer* atau sebagai *counter* serta pemilihan *mode* operasi dapat diatur melalui TMOD. Konfigurasi dari *register* TMOD seperti yang ditunjukkan dalam tabel 2.6 berikut ini :

Tabel 2.6
Register TMOD

Data	Simbol	Posisi	Fungsi /Arti
D0	IT0	TCON.0	*Interrupt 0 type control bit.*
DI	IE0	TCON.1	*External interrupt 0 edge flag.*
D2	IT1	TCON.2	*Interrupt type 1 control bit.* Diatur oleh *software* untuk menentukan aktif *low* atau *high trigger* dari *external*.
D3	IE1	TCON.3	*External interrupt 1 edge flag.* Diatur oleh *hardware* ketika *external interrupt* terdeteksi dan nol-kan melalui *software* ketika *interrupt* diproses.
D4	TR0	TCON.4	*Timer 0 control bit.* Diatur oleh *software* ketika *timer counter 0.*
D5	TF0	TCON.5	*Timer 0 overflow flag control bit.* Diatur oleh *software* ketika *timer/counter 0 overlow.*
D6	TR1	TCON.6	*Timer 1 control bit.* Diatur oleh *software* ketika *timer counter 0.*
D7	TF1	TCON.7	*Timer 1 overflow flag control bit.* Diatur oleh *software* ketika *timer/counter 0 overflow.*

Sumber : Belajar Mikrokontroller ATMEL AT89S8252

Tabel 2.7
Timer/Counter Mode Control Register

Data	Simbol	Fungsi/Arti
D0	*Timer* 0; M0 (0)	Untuk memilih mode *timer.*
D1	*Timer* 0; M1 (0)	Untuk memilih mode *timer.*
D2	*Timer* 0; C/T (0)	1 = *Counter* & *0* = *Timer*
D3	*Timer* 0; GATE (0)	*Timer* akan berjalan jika bit di *set* dan INT0 (untuk *Timer 0)* atau INT1 (untuk *Timer 1).*
D4	*Timer* 1; M0 (1)	Untuk memilih mode *timer.*
D5	*Timer* 1; MI (1)	Untuk memilih mode *timer.*
D6	*Timer* 1; C/T (0)	1 = *Counter* & *0* = *Timer*
D7	*Timer* 1; GATE (1)	*Timer* akan berjalan jika bit di set dan INT0 (untuk *Timer 0)* atau INT1 (untuk *Timer 1).*

Sumber : Belajar Mikrokontroller ATMEL AT89S8252

Tabel 2.8
Mode Operasi *Timer/Counter*

M1	M0	Operating Mode
0	0	*Timer* 13 bit
0	1	*Timer/Counter* 16 bit
1	0	8 bit *Auto reload Timer/Counter*
1	1	TL0 dari *Timer* adalah 8 Bit *Timer/Counter* dikendalikan oleh kontrol bit *Timer* 0. TH0 adalah 8 bit yang dikendalikan oleh *Timer* 1 *control* bit.

Sumber : Belajar Mikrokontroller ATMEL AT89S8252

2.2.3.3.5. Metode Pengalamatan

1. Pengalamatan bit *(Direct Bit Addressing)* :

   Pengalamatan langsung tiap bit ini hanya dilakukan pada lokasi RAM *internal* yaitu 20H-2FH, dan sebagian SFR yaitu port 0, port 1, port 2, port 3, TCON *register,* SCON *register, IE register, PSW register, ACC* dan *B register.*

2. Pengalamatan tak langsung *(Indirect Bit Addressing)* :

   Pada pengalamatan tak langsung, instruksi menunjukkan suatu *register* yang isinya adalah alamat dari *operand, eksternal* dan *internal* RAM dapat dialamati secara tidak langsung. *Register* alamat untuk data dengan lebar 8 bit dapat berupa R0 dan R1 yang digunakan untuk memilih angka *register* atau *stack pointer. Register* alamat untuk data, dengan lebar 16 bit digunakan *Data Pointer* (DPTR).

3. Pengalamatan ber-indeks :

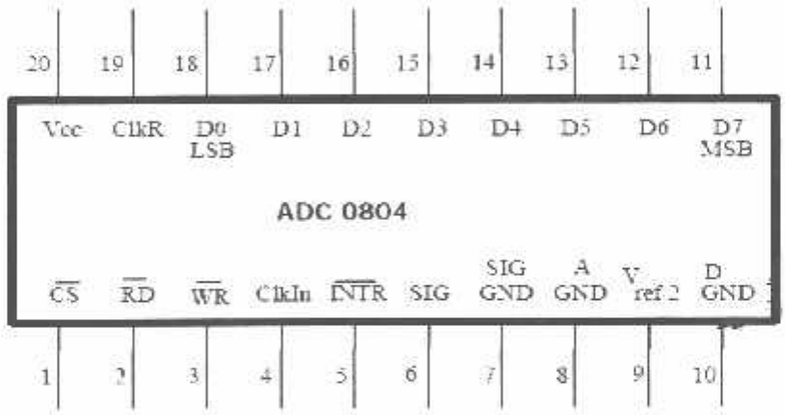
   Yang dapat diakses dengan pengalamatan berindeks hanya *memory program.* Mode ini dimaksudkan untuk membaca *look-up table program.*

4. Konstanta *immediet* :

   Pengalamatan langsung dilakukan dengan memberikan nilai ke *register* secara langsung, dilakukan dengan menggunakan tanda #, (Contoh : Mov A, #100).

2.3. *Analog To Digital Converter* (ADC)

ADC ini berfungsi untuk mengubah sinyal analog menjadi sinyal digital yang akan diumpankan pada mikrokontroller. ADC yang digunakan pada alat pengukur kadar gula dalam darah ini adalah ADC 0804 yang mempunyai fasilitas *internal clock* yang dapat digunakan dengan hanya menambah resistor dan kapasitor eksternal. Tegangan input maksimal ADC adalah 5 Vdc, resolusi 8 bit.Gambar 2.6 di bawah ini adalah gambar pin ADC .



Gambar 2.5. Pin ADC
Sumber : Data Sheet ADC

IC ADC 0804 mempunyai dua masukan analog, Vin(-) dan Vin(+). Masukan analog sesungguhnya (Vin) sama dengan selisih antara tegangan yang dihubungkan dengan kedua pin masukan ini. Untuk operasi normal, ADC 0804

$$fclk = \frac{1}{1{,}1RC}$$

$$fclk = \frac{1}{1{,}1.10K.150pF}$$

$$fclk = 606{,}06Hz$$

Frekuensi ini masih berada dalam batas range ADC 0804 yaitu 100 KHz sampai 1 MHz.

Dengan :

f = Frekuensi *clock* ADC 0804 (Hz)

R = Nilai tahanan pada rangkaian clock ADC 0804 (Ohm)

C = Nilai kapasitansi pada rangkaian clock ADC 0804 (Farad)

Pengubah analog ke digital berfungsi untuk mengkonversikan data dari bentuk analog ke bentuk digital. Diantara berbagai jenis ADC yang biasa digunakan adalah ADC jenis pencacah pendekatan berturut-turut *(successive Aproximate)* dan jenis ADC *dual slope*.

Dalam sebuah pengukuran suatu variabel fisik yang pada umumnya bersifat analog dengan menggunakan piranti digital, diperlukan adanya pengubahan variabel digital yang nilainya proporsional dengan nilai variabel yang diukur. Resolusi ADC adalah perubahan terkecil yang dapat terjadi pada *output* analog sebagai hasil dari perubahan peta *input* digital dimana presentasi resolusi memiliki perhitungan sebagai berikut:

$$\%resolusi = \frac{stepsize}{FS} x100\%$$

Spesifikasi lain untuk ADC adalah waktu konversi *(convertion time)*. Waktu konversi suatu ADC untuk menghasilkan kode biner valid untuk tegangan masukan yang diberikan. Sebuah *converter* disebut berkecepatan tinggi jika memiliki waktu konversi pendek. Pada alat ini menggunakan ADC parallel 8-bit 0804 seperti pada gambar 2.6. diatas. ADC paralel akan mengeluarkan data serial melalui satu buah pin bila diberikan *clock* dari luar.

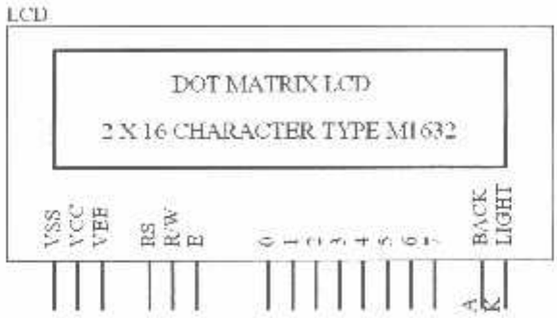
2.4. LCD (*Liquid Crystal Display*).

Liquid Crystal Display adalah modul tampilan yang mempunyai konsumsi daya yang relatif rendah dan terdapat sebuah controller CMOS didalamnya. Controller tersebut sebagai pembangkit ROM/RAM dan display data RAM. Semua fungsi tampilan di kontrol oleh suatu instruksi,sehingga modul LCD dapat dengan mudah diinterfacekan dengan MPU. Ciri-ciri dari LCD M1632:

- Terdiri dari 32 karakter yang dibagi menjadi 2 baris dengan display dot matrik 5 X 7 ditambah cursor.
- Karakter generator ROM dengan 192 karakter.
- Karakter generator RAM dengan 8 tipe karakter.
- 80 X 8 bit display data RAM.
- Dapat diinterfacekan dengan MPU 8 atau 4 bit
- Dilengkapi fungsi tambahan : Display clear, cursor home, display ON/OFF, cursor ON/ OFF, display character blink, cursor shift dan display shift
- Internal data

- Internal otomatis dan reset pada power ON
- +5 V power supply tunggal

Berikut ini merupakan pin-pin LCD berserta konfigurasinya:



Gambar 2-6. LCD M1632

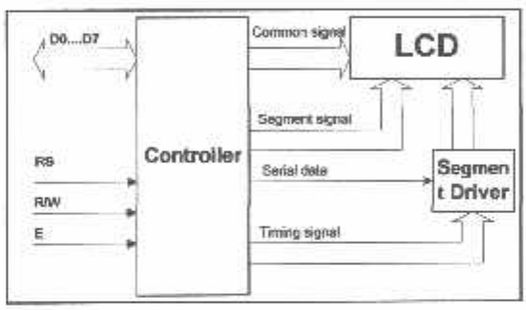
LCD ini mempunyai 16 pin yang dihubungkan dengan perangkat keras prosessor penunjang. Adapun fungsi dari masing-masing pin, ditunjukkan dalam tabel berikut ini:

Tabel 2.9. Fungsi Pin LCD M1632

No	Nama Penyemat	Fungsi
1	Vss	Terminal ground
2	Vcc	Tegangan catu +5 volt
3	Vee	Drive LCD
4	RS	Sinyal pemilih register 0: Instruksi register (tulis) 1: Data Register (tulis dan baca)
5	R/W	Sinyal seleksi tulis atau baca 0: Tulis 1: Baca
6	E	Sinyal operasi awal, sinyal ini mengaktifkan data tulis dan baca

7 – 14	DB0-DB7	Merupakan saluran data, berisi perintah dan data.
15	V+ BL	Pengendali kecerahan latar belakang LCD 4 - 4,42 V dan 50 – 500 mA
16	V-BL	Pengendali kecerahan latar belakang LCD 0 V

Masukan yang diperlukan untuk mengendalikan modul berupa bus data yang masih termutiplek dengan bus alamat serta 3 bit sinyal kontrol. Sementara pengendalian LCD dilakukan secara internal oleh kontroler yang sudah terpasang dalam modul LCD. Diagram blok untuk LCD dapat dilihat dalam Gambar 2.28.



Gambar 2.7 Diagram Blok LCD M1632.

2.5. Keypad 4x4.

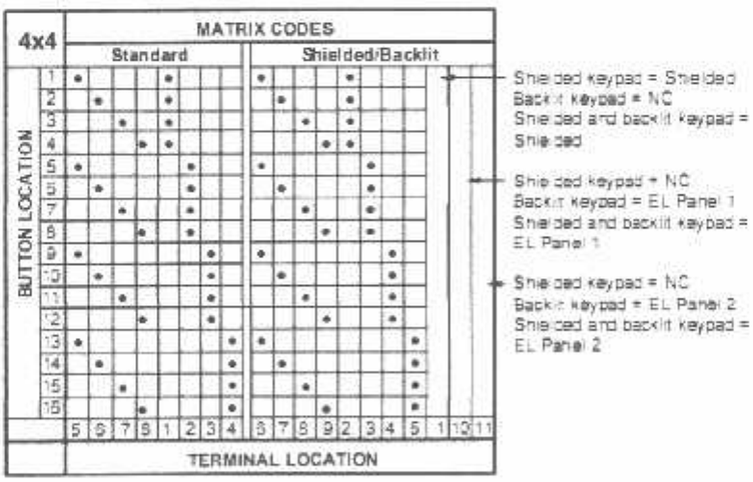
Untuk mempermudah penggunaan mikrokontroler sebagai alat pemroses, maka diperlukan sarana yang dapat menjadi penghubung antara pengguna dan alat kontrol, yaitu sebagai sarana input data yang nantinya akan diolah oleh mikrokontroler.

Peralatan input data yang dapat menunjang mikrokontroler adalah beberapa saklar tekan yang menyatakan angka dan karakter yang disusun

berbentuk matrik 4 kolom dan 4 baris. Keypad ini berfungsi untuk memberikan masukan setting waktu yang diinginkan. Rangkaian keypad menggunakan keypad 4 kolom dan 4 baris yaitu 16 saklar tekan (*push button*) yang dirangkai dalam bentuk matrik. Rangkaian keypad ini dihubungkan langsung ke mikrokontroler. Dalam skripsi ini diperlukan sebuah keypad 4x4 yang memuat angka 0 sampai 9, karakter cancel dan enter. Berikut gambar keypad 4x4 ditunjukkan pada gambar di bawah ini :

Gambar 2.8. Keypad 4 x4

Tabel 2.10 Tabel Kebenaran Key Pad 4x4

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BAB III

PERANCANGAN DAN PEMBUATAN ALAT

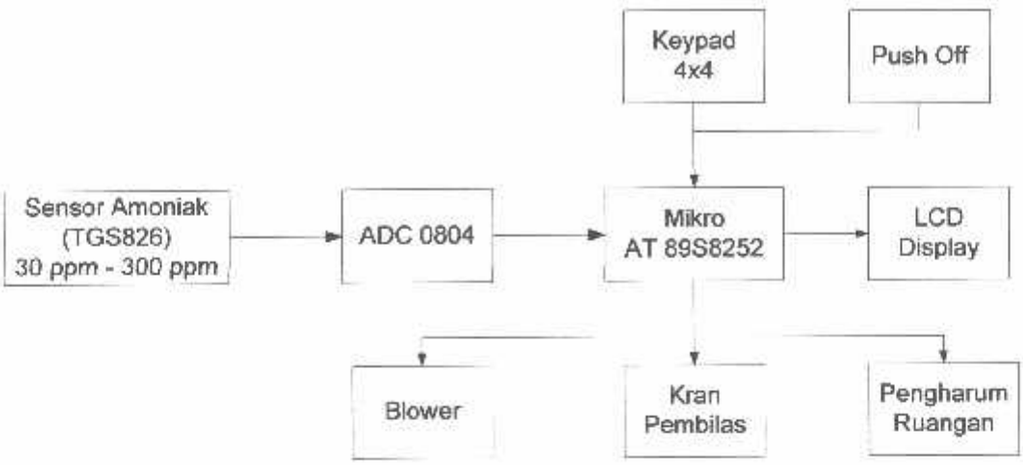
Perencanaan alat yang dibuat dalam tugas akhir ini meliputi perencanaan perangkat keras dan perencanaan perangkat lunak. Komponen yang dipakai dalam perencanaan ini antara lain mikrokontroler AT89S8252 sebagai kontrol utama, dengan komponen pendukung meliputi sensor amoniak TGS826,dan ADC 0804 serta LCD sebagai tampilan kadar amoniak.

Cara kerja dari alat ini secara garis besar dapat dijelaskan sebagai berikut: Sensor *TGS826* digunakan untuk mendeteksi kadar amoniak yang dihasilkan oleh urine. Keluaran dari sensor tersebut berbentuk analog dimana sinyal yang dihasilkan selanjutnya menjadi inputan untuk ADC 0804 untuk diubah menjadi data digital (biner). Kemudian diolah oleh mikrokontroller AT89S8252 melalui program software sehingga data olahan tersebut dapat ditampilkan pada LCD.Selain itu *mikrokontroller* akan memberikan instruksi pada motor untuk menjalankan baik itu membuka kran air, menyalakan kipas, maupun memberi pengharum ruangan.

3.1. Perancangan System

Perancangan alat pendeteksi kadar amoniak pada kamar mandi dimana dikendalikan mikrokontroler AT89S8252 sebagai kendali utama dan menggunakan komponen lain sebagai komponen pendukung. Sebelum membuat perangkat keras terlebih dahulu direncanakan blok diagram yang akan dibuat, dan

membahasnya sesuai dengan blok diagram. Adapun blok diagram yang direncanakan adalah sebagai berikut :



Gambar 3.1 Blok Diagram Perencanaan

Dari blok diagram diatas dapat dijelaskan sebagai berikut :

Fungsi dari tiap-tiap diagram dijelaskan sebagai berikut :

1. Sensor Amoniak

   Mengubah besaran non elektris menjadi besaran elektris dalam hal ini adalah kadar Amoniak dalam urine.

2. ADC 0804

   Merubah atau mengkonversikan sinyal analog menjadi sinyal digital.

3. Mikrokontoller AT 89S8252

   Digunakan sebagai penghitung dan pengolah data serta memprosesnya yang kemudian memberikan instruksi pada blower, pengharum ruangan, dan kran pembilas untuk melakukan proses pembersihan.

4. LCD

   Digunakan untuk menampilkan kadar amoniak pada kamar mandi.

5. Keypad 4x4

   Digunakan untuk memasukkan *Range* kadar amoniak yang dideteksi oleh sensor.

6. Push Off

   Digunakan sebagai pengaman, apabila saklar tertekan maka system akan berhenti.

7. Kran Pembilas

   Berfungsi untuk membilas lantai kamar mandi.

8. Pengharum Ruangan

   Memberikan aroma harum pada ruangan kamar mandi.

9. Blower / Penyedot udara

   Berfungsi untuk mengeluarkan gas amoniak yang terdapat dalam ruangan.

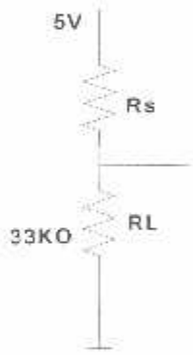
3.1.1.Perencanaan Perangkat Keras Meliputi :

- **Sensor TGS826**
- **ADC 0804**
- **Mikrokontroller AT89S8252**
- **LCD M1632**
- **Keypad 4x4**
- **Rangkaian Driver Relay**

3.1.1.1. Sensor

Sensor yang digunakan pada perencanaan alat ini adalah sensor amoniak TGS826, Dalam kemampuan pendeteksian gas konduktifitas sensor bertambah tergantung konsentrasi gas pada udara. Sebuah rangkaian listrik sederhana dapat mengkonversikan perubahan konduktivitas kedalam sebuah signal *output* yang sesuai dengan konsentrasi gas.

Gambar 3.2 *Sensor TGS826* / Sensor Amoniak



Gambar 3.3 Rangkaian Dasar *TGS826* / Sensor Amoniak

Pada rangakaian sensor, penulis merancang menggunakan RL = 33 KΩ sesuai dengan *data sheet* sensor TGS 826. Sedangkan dalam kondisi tersebut tanpa inputan amoniak pada ADC sudah terdapat nilai desimal sebesar 50. Sehingga diperoleh perhitungan sebagai berikut:

- Vperstep $= \frac{V\max}{2^n - 1}$

$= \frac{5}{255}$

$= 0{,}0196V$

- Vout = Vperstep x ΔDC

dengan diketahui ADC = 50

maka,

Vout $= \frac{RL}{RS + RL} \times V$

Sehingga,

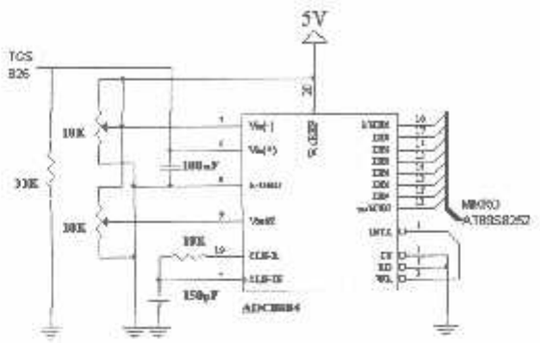
Rs $= \frac{RL \times V}{Vout} - RL$

$= \frac{33 \times 5}{0.98} - 33$

$-135.36\ \text{K}\Omega$

3.1.1.2. Perancangan ADC

Pada perancangan ADC menggunakan IC type 0804. Lihat Gambar 3.4.



Gambar 3.4. Rangkaian ADC 0804

Untuk frekuensi clock dari ADC ini adalah :

Untuk R = 10 KΩ dan C = 150 pF

$$fclk = \frac{1}{1{,}1RC}$$

$$fclk = \frac{1}{1{,}1.10K.150pF}$$

$$fclk = 606{,}06Hz$$

Frekuensi ini masih berada dalam batas range ADC 0804 yaitu 100 KHz sampai 800 Mhz.

Untuk Vin ADC dapat diketahui yaitu :

$$Vin = V\max - 1{,}5\left[\frac{(V\max - V\min)}{256}\right]$$

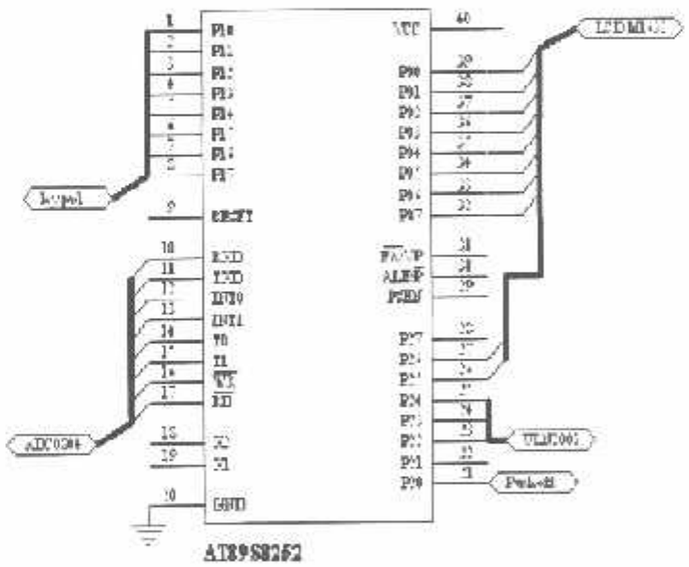
$$Vin - 5 - 1{,}5\left[\frac{(5-2{,}5)}{256}\right]$$

$$Vin = 4{,}98Volt$$

Keterangan Gambar :

1. Untuk Pin 1,2,8 disambungkan ke *ground*.
2. Untuk pin 4 dan 19 di*pull up* resistor 10 K dan *decoupling* kapasitor sebesar 150 pF.
3. Pin 6 merupakan input analog yang dihubungkan ke sensor TGS 826.
4. Tegangan referensi diambilkan dari pin 9 dengan memberi tambahan resistor 10k
5. Pin 11 sampai pin 18 adalah *output* yang akan diumpankan ke Mikrokontroller AT89S8252.

3.1.1.3. Perancangan Mikrokontroller



Gambar 3.5. Rangkaian Mikrokontroller

Keterangan Gambar :

1. Pin 20 dihubungkan ke *ground*
2. Untuk Pin 40 dihubungkan ke Vcc
3. Untuk Pin 1 – 8 atau Port 1.0 – 1.7 digunakan sebagai *input* yang diterima dari *keypad.*
4. Untuk Pin 32 – 39 atau Port 0.0 - 2.7 digunakan sebagai *output data* yang dihubungkan ke pin no 7 – 14 pada *display.*
5. Untuk Pin 23 – 25 dihubungkan pada pin 1 – 3 pada *relay.*
6. Untuk Pin 10 – 17 dihubungkan pada *output* ADC.

Digunakannya MCU AT89S8252 dalam perencanaan ini karena MCU ini telah menyediakan *internal* memori, jadi tidak diperlukan memori tambahan dari luar. Sehingga bentuk fisik alat lebih kecil, dan juga MCU ini mudah didapat di pasaran dengan harga yang relatif terjangkau.

3.1.1.3.1. Oscilator

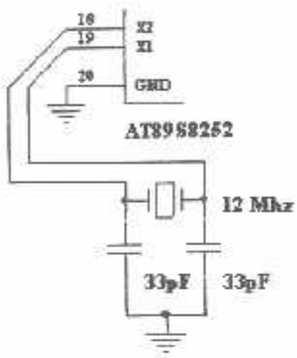
Semua keluarga MCS-51 mempunyai *clock* (rangakaian oscilator) di dalam *chip*nya sendiri yang disebut *on-chip* osilator. Cara mengakses *clock* internal yang terdapat pada *chip* mikrokontroller yaitu sebuah kristal pada pin-pin XTAL 1 dan pin XTAL 2 dengan dua buah kapasitor yang masing-masing dihubungkan ke *ground.* Pemindahan frekuensi kristal berdasarkan akses mikrokontroller untuk sebuah *interface,* kristal yang dipakai sebesar 12 Mhz

dengan ketentuan pada *data sheet* adalah sebesar 30 pF. Rangkaian ini terdiri dari dua buah kapasitor dan sebuah kristal, dengan data sebagai berikut :

C1 dan C2 = 30 – 10 pF untuk kristal

C1 dan C2 = 40 -10 pF untuk keramik resonator

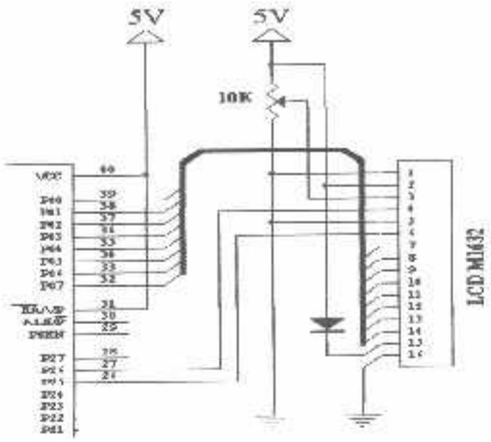
Kristal = 3 – 24 Mhz



Gambar 3.6. Rangkaian Oscillator

3.1.1.4. Rangkaian LCD M1632 (*Liquid Crystal Display*)

Dalam aplikasi ini menggunakan sebuah layar LCD (*Liquid Crystal Display*) yaitu jenis *Seiko Instrument* M1632 yang merupakan LCD dua baris dengan setiap barisnya terdiri 16 karakter dan menggunakan IC 74LS164 yang merupakan register geser 8 bit yang memiliki jalan masuk deret tergerbang. Gambar hubungan antara LCD, IC74LS164 dan mikrokontroler dapat dilihat dalam Gambar 3.7



Gambar 3.7 Rangkaian LCD

LCD dot matrik ini membutuhkan sepuluh buah pin masukan/keluaran dari mikrokontroler dan IC 74164 Adapun dua buah pin yaitu port 1.0 pada penyemat RS yang digunakan sebagai sinyal pemilih register dan port 1.1 pada penyemat Enable digunakan sebagai sinyal operasi awal, sinyal enable ini mengaktifkan data tulis atau baca oleh mikrokontroler, penyemat DB0-DB7 yang dihubungakan ke pin data IC74164 digunakan untuk menampilkan karakter yang dikehendaki oleh mikrokontroler. Ketika terdapat data pada jalur data, data tersebut akan ditahan dengan memberikan *clock* pin E pada LCD. Pin RS menentukan apakah data yang ditahan akan digunakan sebagai instruksi untuk mengatur *setting* tampilan pada LCD atau sebagai kode karakter yang diperlukan LCD untuk menampilkan suatu karakter. Sedangkan untuk pin R/W pada LCD dihubungkan ke *ground* karena dalam hal ini LCD hanya melakukan operasi write atau operasi menampilkan karakter.

Untuk pin Vcc pada LCD dihubungkan ke supply +Vcc dan Vss dihubungkan ke *ground*. Pin V_{EE} beserta pin Vcc dan Vss dihubungkan ke

trimer potensio atau kadang disebut dengan *trimpot*. *Trimpot* ini digunakan untuk mengatur kontras dari tampilan LCD dengan cara mengubah tegangan pada pin V_{EE}.

Pada lembaran datasheet modul LCD M1632 Seiko Instrument Inc. disebutkan bahwa :

Power supply LCD meliputi :

Vss = 0 V

Vcc = 5 V ± 5% (2mA)

Power supply back light :

V + BL = 4 - 4,2 V (50 sampai 200 mA)

V BL = 0 V (GND)

Pada input V + BL dipasang sebuah dioda 1N4001 (bahan silicon dengan Vd = 0,65 V sampai 0,7 V). tujuannya adalah didapatkan tegangan V + BL sebesar 4 - 4,2 V dengan perhitungan sebagai berikut :

Vcc = Vd + (V + BL)

5 = 0,7 + (V + BL)

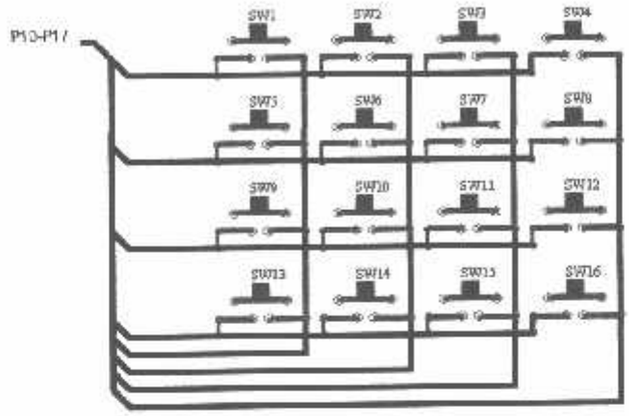
(V + BL) = 5 - 0,7 = 4,3 Volt

Dipilih dioda 1N4001 karena arus maksimum yang biasa dilewatkan oleh dioda ini sebesar 1 A

3.1.1.5. Rangkaian Keypad

Keypad yang digunakan adalah keypad matriks 4x4. Port yang digunakan untuk sinyal port 2.0 – port 2.3 dari mikrokontroller masuk ke

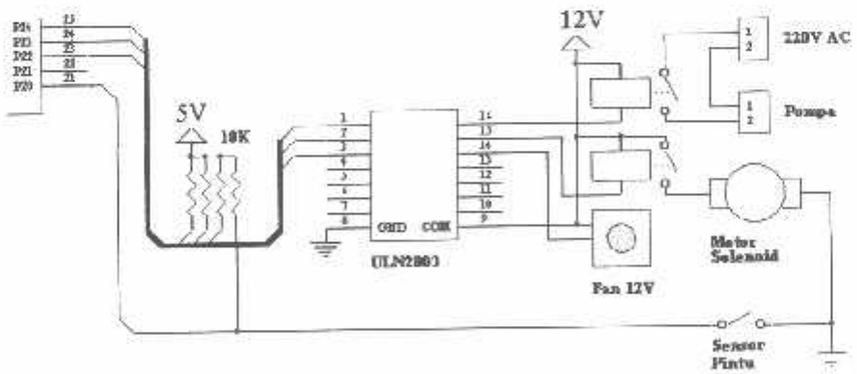
kelompok baris keypad, sedangkan kelompok kolom keypad dihubungkan ke port 2.4 – port 2.7 mikrokontroller. Untuk fungsi dari tombol-tombol keypad tergantung pada pemrogram. Berikut blok diagram dari penyambungan keypad ke mikrokontroller.



Gambar 3.8 Blok Diagram Hubungan Keypad Dengan Mikrokontroller

3.1.1.6. Rangkaian Driver Relay

Rangkaian driver yang digunakan untuk menggerakkan relai yang terhubung dengan motor DC terdiri dari IC ULN2003 yang difungsikan sebagai penguat arus dan pembalik logika driver swithcing.



Gambar 3.9 Rangkaian Driver Motor

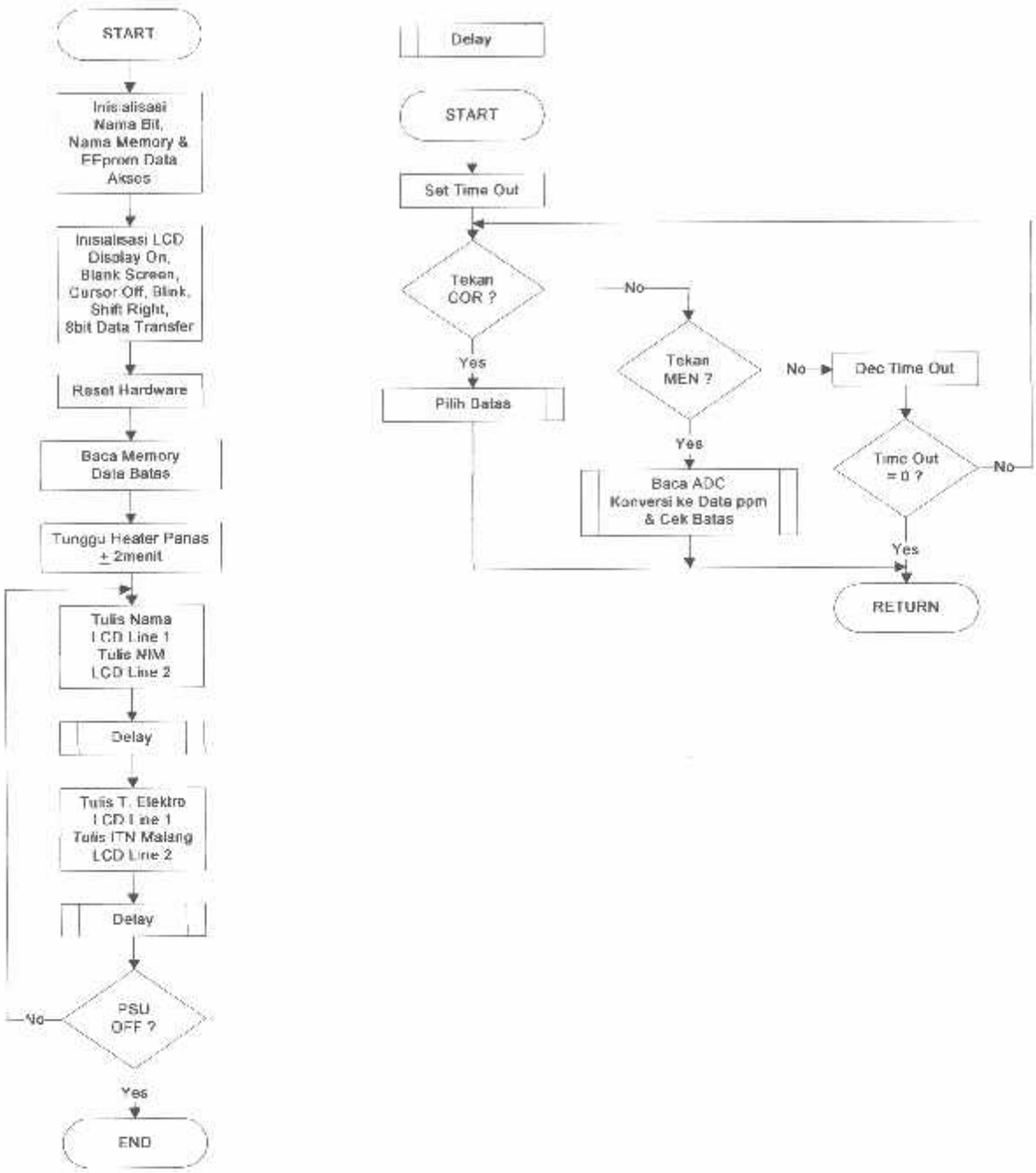
3.1.2. Perancangan Perangkat Lunak

Perancangan perangkat lunak diperlukan untuk menjalankan sistem sesuai yang kita harapkan. Untuk pemakaian mikrokontroller, perlu direncanakan perangkat lunak yang dapat mengatur sistem tersebut. Perangkat lunak disini adalah susunan perintah-perintah (program) didalam memori yang harus dilaksanakan oleh mikrokontroller.

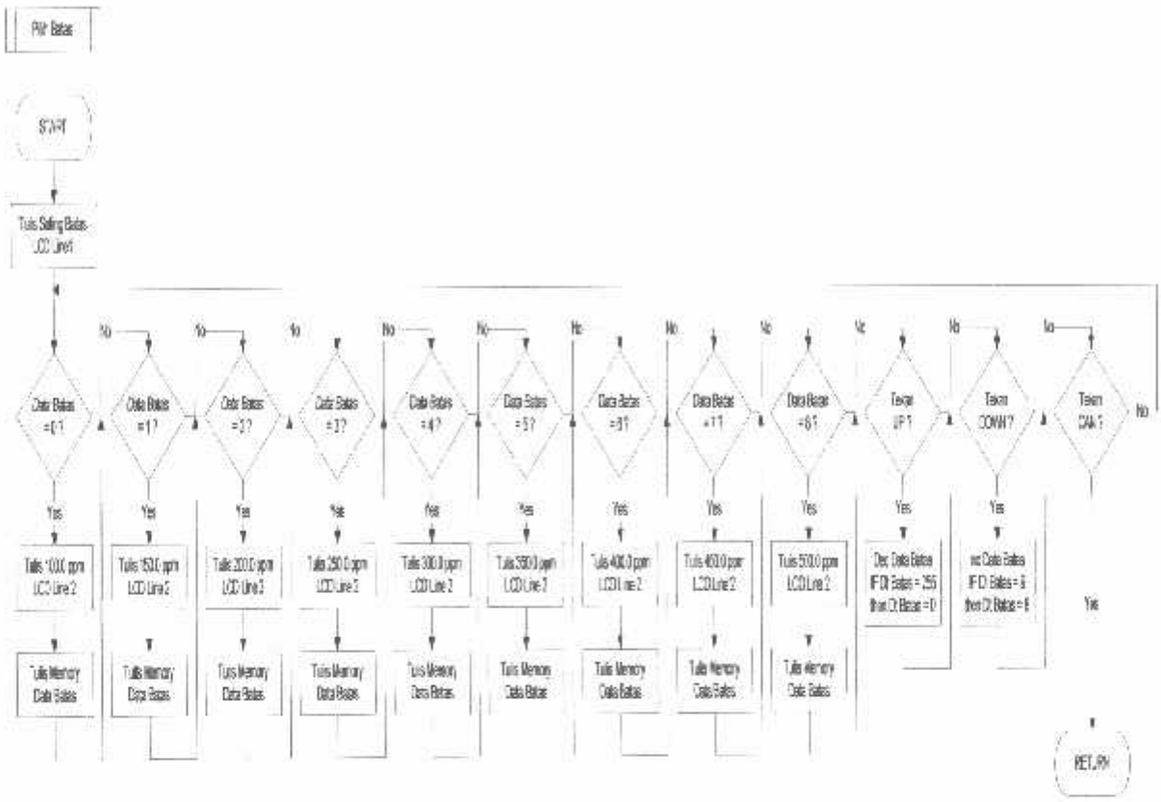
Memori merupakan fasilitas utama karena disinilah disimpan perintah-perintah yang harus dikerjakan. Memori disini dapat dibedakan menurut fungsinya menjadi program dan memori data. Menurut letaknya memori dapat dibedakan menjadi memori program dan memori luar. Memori luar diberikan bila memori didalam mikrokontroller tidak mencukupi untuk menampung semua program dan data. Perancangan perangkat lunak (*software*) didasarkan perencanaan perangkat keras yang telah dibuat sebelumnya, untuk mendapatkan sistem kerja yang diharapkan *software* dari alat tersebut terdapat di bagian lampiran dan diagarm alir (*flowchart*) dari tersebut adalah sebagai berikut :

.Pada perangkat lunak inilah kita dapat menentukan bagaimana sistem rangkaian ini akan bekarja, pada bagian inilah semua tata kerja rangkaian ditentukan .dalam merancang perangkat lunak ini ,mengunakan sofware yaitu sofware pada mikrokontroler.

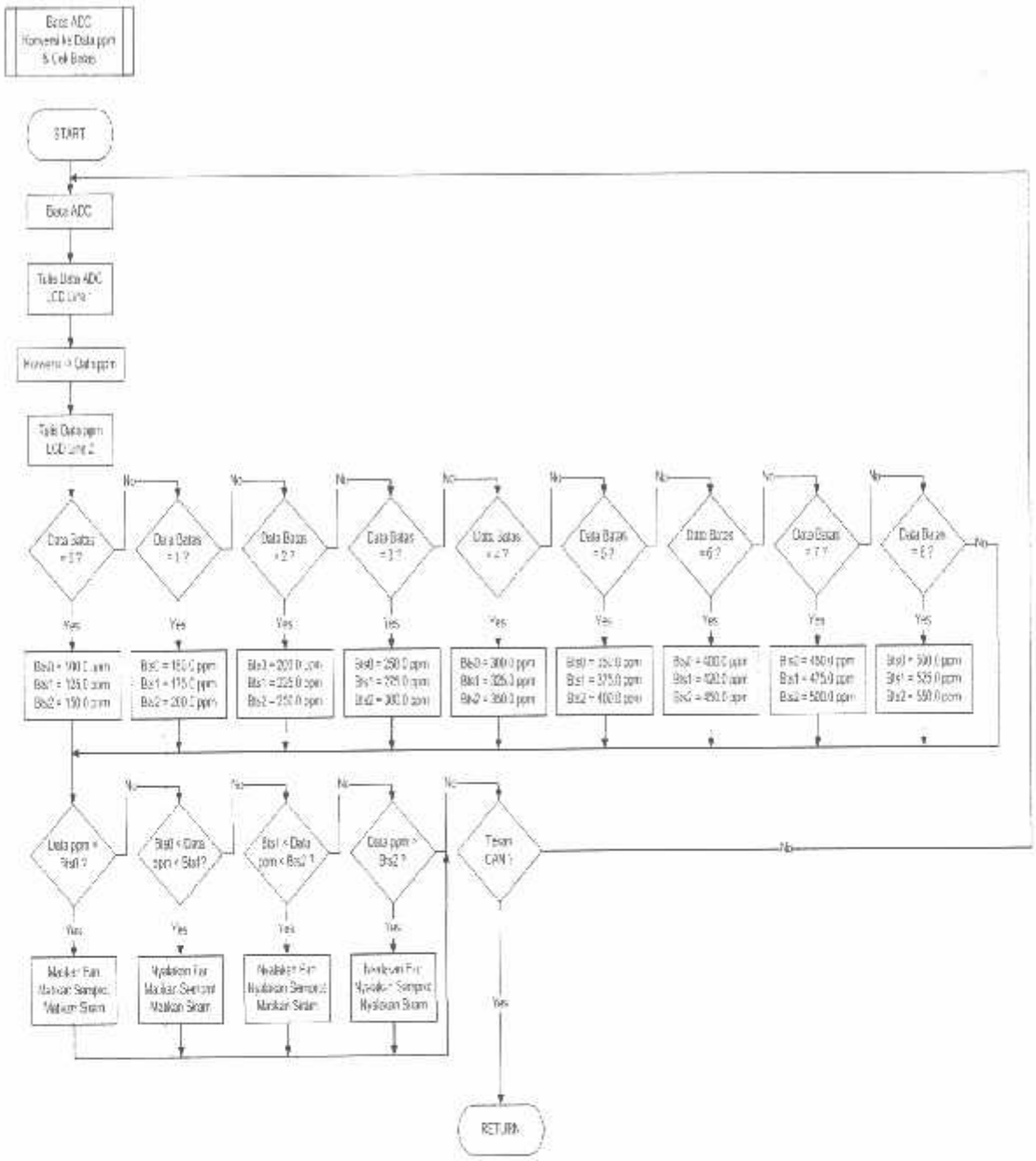
3.1.2.1. FlowChart *Software*



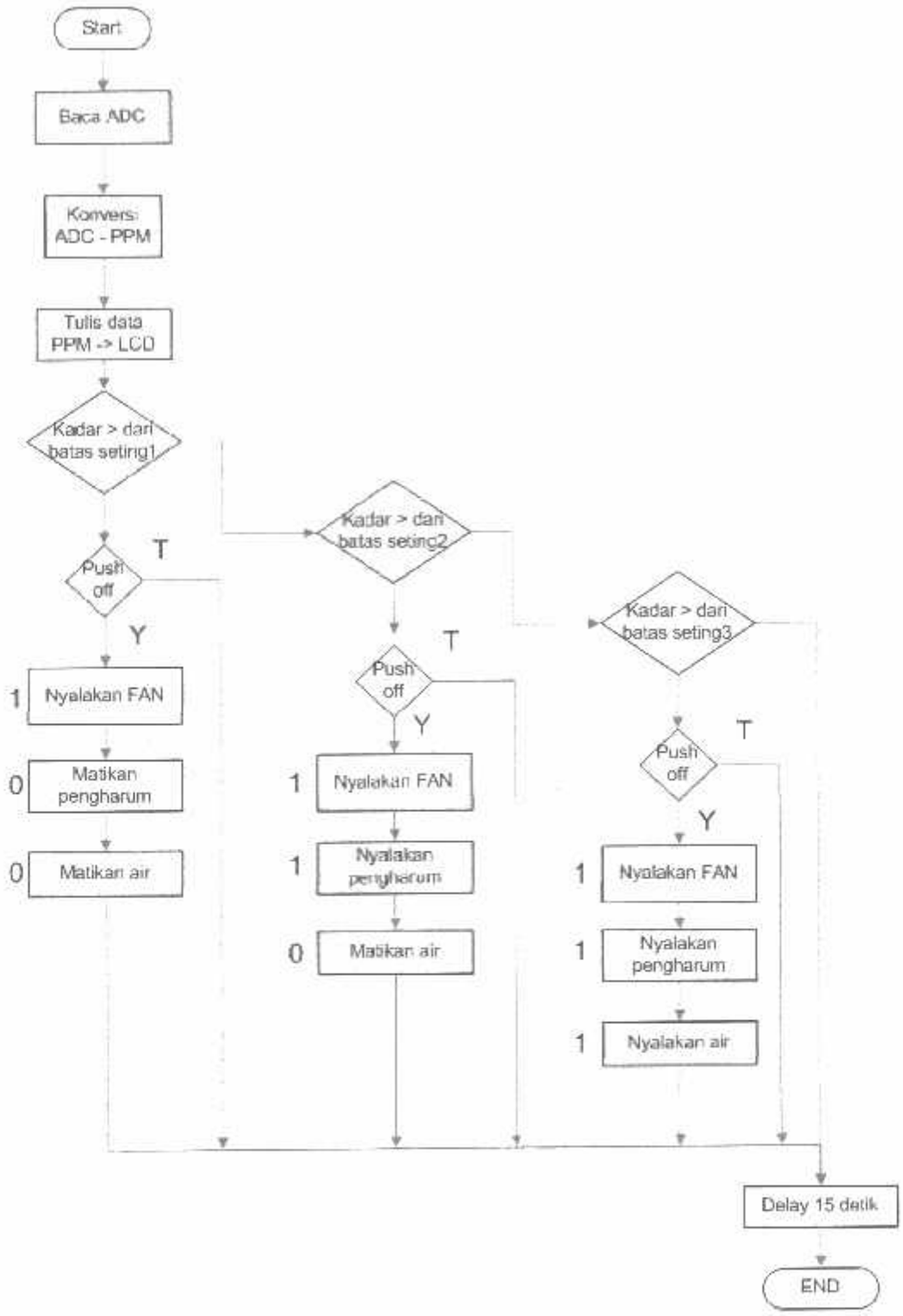
Gambar 3.10 Flowchart Software



Gambar 3.11 Flowchart Software



Gambar 3.12 Flowchart Software



Gambar 3.13 ***FlowChart*** **Sistem**

BAB IV

PENGUJIAN ALAT

4.1. Tujuan

Bab ini akan membahas tentang pengujian alat yang telah dirancang. Adapun tujuan dari pengujian ini adalah untuk mengetahui apakah *hardware* dan *software* dapat bekerja sesuai dengan kondisi yang diinginkan,maka dilakukan pengujian pada alat dan sistem kerja alat, yang mana prosedur pengujian meliputi:

1. Pengujian *Hardware*.
2. Pengujian sistem secara keseluruhan.

4.2. Pengujian Perangkat Keras(*Hardware*).

Dalam pengujian alat dibagi dalam beberapa sub sistem dari instrumen dan peralatan, diantaranya adalah :

1. Pengujian Sensor
2. Pengujian ADC
3. Pengujian LCD
4. Pengujian Keypad
5. Pengujian Keseluruhan Alat

Pengujian perangkat keras ini mencakup pengujian rangkaian elektronika pada masing-masing blok maupun blok secara kesceluruhan.

4.2.1. Pengujian Sensor

4.2.1.1. Tujuan

Untuk mengetahui berapa kadar amoniak yang didcteksi dengan menterjemahkan grafik sensitivitas sensor TGS 826.

4.2.1.2. Prosedur Pengujian

Pada rangakaian sensor, menggunakan RL = 33 KΩ, Vc = 5 Volt sesuai dengan *data sheet* sensor TGS 826.

ADC 0804 bekerja dari 0-5 volt = 0-255 data.

Jadi resolusi ADC linier / Vperstep :

- Vperstep $= \frac{V\,\max}{2^n - 1}$

  $= \frac{5}{255}$

  $= 0{,}0196V$ /data

Pada saat sensor tanpa beban / tanpa kadar amoniak sensor menunjukkan nilai ADC = 50 yang artinya:

- ADC $= \frac{Vout}{Vperstep}$

  50 $= \frac{Vout}{0.0196}$

  Maka

- Vout (sensor) = Vperstep x ADC

  = 0.0196 x 50

  = 0.98 V

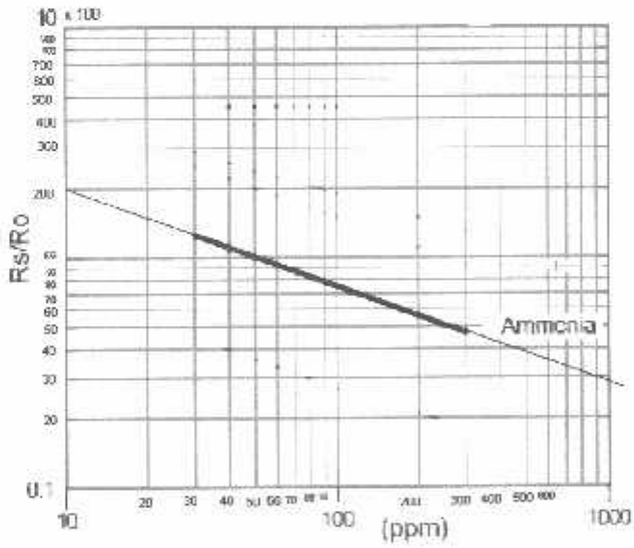
Output dari sensor TGS 826 berbentuk tegangan (Vout sensor), dengan mendapatkan nilai Voutput dari sensor maka dapat diketahui nilai Rs dengan rumus seperti dibawah ini:

- $Rs = \frac{RL \times V}{Vout} - RL$

  $= \frac{33 \times 5}{0.98} - 33$

  $= 135.37\,\Omega$

Kemudian dengan didapat nilai Rs maka kadar amoniak dapat dikonversikan dengan menggunakan grafik sensitifitas sensor TGS 826 seperti gambar 4.1 dibawah ini



Gambar 4.1 Grafik Sensitivitas Sensor TGS 826

Nilai ADC dapat dihitung dengan rumus dibawah ini:

- ADC = $\frac{RL \times V}{Rs \times Vperstep} - RL$

Dari rumus diatas didapat sensitifitas sensor seperti dibawah ini

Tabel 4.1 Sensitifitas Sensor TGS 826

NO	ADC	RS (Ω)	PPM
1	63	100	50
2	74	80	90

4.2.1.3. Perhitungan Rs

Vout (sensor) = Vperstep x ADC

$Rs = \frac{RL \times V}{Vout} - RL$

- Pada ADC = 50

Vout (sensor) = Vperstep x ADC

= 0.0196 x 50

= 0.98 V

$Rs = \frac{33 \times 5}{0.98} - 33 = 135.37\ \Omega$

- Pada ADC = 51

$$\text{Vout (sensor)} = \text{Vperstep x ADC}$$

$$= 0.0196 \times 51 = 0.9996 \text{ V}$$

$$\text{Rs} = \frac{33 \times 5}{0.9996} - 33 = 132.07\ \Omega$$

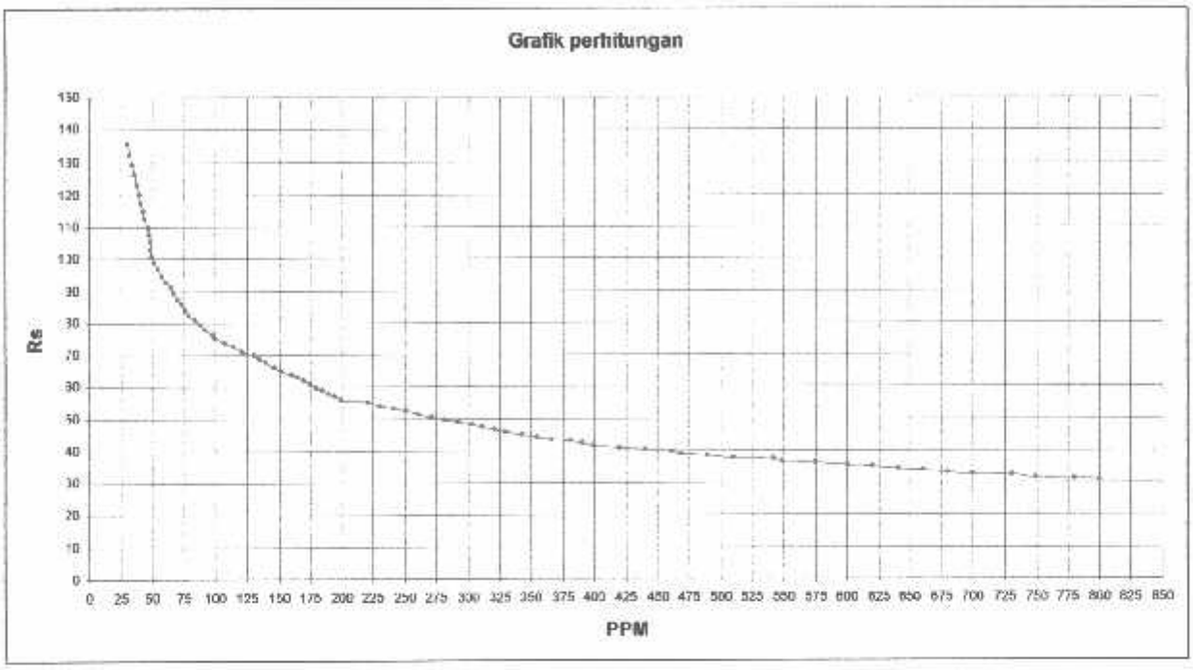
Dari perhitungan Rs diatas didapat tabel seperti dibawah ini

Tabel 4.2 Hasil Perhitungan Sensor TGS 826

ADC (data)	RS Ω	PPM
50	135.37	30.07
51	132.07	32.01
52	128.89	33.98
53	125.84	35.96
54	122.90	37.97
55	120.06	40.02
56	117.33	41.36
57	114.69	43.09
58	112.14	44.04
59	109.68	46.55
60	107.31	47.46
61	105.01	48.39
62	102.78	49.28
63	100.62	50.00
64	98.54	51.98
65	96.51	55.01
66	94.55	58.07
67	92.65	61.12
68	90.80	64.10
69	89.01	67.11
70	87.26	70.15
71	85.57	73.04
72	83.92	75.95
73	82.32	78.88
74	80.76	90.00
75	79.24	93.04
76	77.77	95.97
77	76.33	97.25

ADC (data)	RS Ω	PPM
78	74.93	99.93
79	73.56	107.57
80	72.23	114.45
81	70.93	120.77
82	69.66	130.46
83	68.43	135.10
84	67.22	139.75
85	66.04	146.59
86	64.89	152.74
87	63.76	160.27
88	62.66	165.03
89	61.59	169.80
90	60.54	174.62
91	59.51	179.44
92	58.50	184.32
93	57.52	189.21
94	56.56	194.17
95	55.61	199.13
96	54.69	221.09
97	53.79	231.06
98	52.90	241.07
99	52.03	251.16
100	51.18	261.25
101	50.35	271.43
102	49.53	281.68
103	48.73	292.01
104	47.95	302.41
105	47.17	311.77

ADC (data)	RS Ω	PPM
106	46.42	321.13
107	45.68	330.49
108	44.95	343.09
109	44.23	354.93
110	43.53	366.20
111	42.84	380.91
112	42.16	390.44
113	41.50	399.99
114	40.85	420.26
115	40.20	440.62
116	39.57	461.09
117	38.95	469.36
118	38.34	489.95
119	37.74	510.09
120	37.15	541.80
121	36.57	549.39
122	36.00	575.32
123	35.44	601.25
124	34.89	620.82
125	34.35	640.45
126	33.81	660.12
127	33.29	679.86
128	32.77	699.66
129	32.26	730.66
130	31.76	749.50
131	31.26	780.76
132	30.78	799.69



Gambar 4.3 Grafik Hasil Perhitungan Sensor TGS 826

Untuk menghitung kesalahan pada percobaan yaitu :

$$Error = \frac{HasilPerhitungan - hasilpengukuran}{HasilPerhitungan} \times 100\%$$

$$Error = \frac{100.62 - 100}{100.62} \times 100\%$$

$$Error = 0.61\%$$

Dengan melakukan perhitungan yang sama maka akan didapatkan hasil yang ditunjukkan pada tabel 4.3. di bawah ini.

Tabel 4.3.Perbandingan Rs Sensor dan Rs Perhitungan

ADC	Rs (sensor) Ω	Rs (perhitungan) Ω	% Error	PPM
63	100	100.62	0.61	50
74	80	80.76	0.94	90

Error rata-rata sebesar :

$$\sum errorrata-rata = \frac{\sum error}{n}$$

$$\sum errorrata-rata = \frac{1.55\%}{2} = 0.77\%$$

4.2.2. Pengujian ADC 0804

4.2.2.1. Tujuan

Untuk mengetahui hasil konversi tegangan analog ke digital setiap kenaikan 1digit hasil konversi.

4.2.2.2. Peralatan yang digunakan

- Variabel resistor 10 kΩ
- Digital multimeter
- Catu daya 5 Volt
- Rangkaian ADC 0804
- Delapan bit rangkaian indikator LED

4.2.2.3. Prosedur pengujian

1. Memasang 8 buah LED dengan resistor 220 pada keluaran ADC 0804.
2. Memberikan catu daya 5 Volt pada rangkaian ADC 0804.
3. Memberikan Masukan analog pada tegangan 0 sd 5 Volt pada pin masukan ADC 0804.
4. Mengatur Variabel resistor untuk mendapatkan tegangan yang diinginkan.
5. Mencatat data biner 8 bit pada keluaran ADC 0804.

Gambar 4.4 Diagram Blok Pengujian ADC 0804

4.2.2.4. Hasil Pengujian

Untuk mengetahui perubahan tegangan tiap bit ADC adalah dengan menggunakan perhitungan sebagai berikut

Diketahui V = 5 Volt Step ADC = 2^8 (255), maka

$$1 \text{ bit} = \frac{V}{StepADC}$$

$$= \frac{5}{255} = 19.6 \text{ mV} = 20 \text{ mV}$$

Tabel 4.4 Hasil Pembacaan Dan Perhitungan ADC 0804

Input ADC (Volt)	Output ADC (pembacaan)	Output ADC Perhitungan		
	Biner	Biner	Desimal	Heksa Desimal
0	00000000	00000000	0	00h
0.25	00001101	00001101	13	0Dh
0.5	00011010	00011010	26	1Ah
0.75	00100110	00100110	38	26h
1.01	00110100	00110100	52	34h
1.26	01000000	01000000	64	40h
1.5	01001101	01001101	77	4Dh
1.75	01011001	01011001	89	59h
2.02	01100111	01100111	103	67h
2.25	01110011	01110011	115	73h
2.5	10000000	10000000	128	80h
2.75	10001100	10001100	140	8Ch
3	10011001	10011001	153	99h
3.25	10100110	10100110	166	A6h
3.5	10110011	10110011	179	B3h
3.75	10111111	10111111	191	BFh
4	11001100	11001100	204	CCh
4.25	11011001	11011001	217	D9h
4.5	11100110	11100110	230	E6h
4.75	11110010	11110010	242	F2h
4.99	11111111	11111111	255255	FFh

Sedangkan untuk mengetahui data ADC ditentukan dengan perhitungan sebagai berikut:

Diket V analog = 0.25 Volt, maka

$$\text{Data ADC} = \frac{Vanalog}{resolusi}$$

$$= \frac{0.25}{0.0196} = 12.75 \approx 13_{(10)}$$

$$= 00001101_{(2)}$$

$$= 0\ D_{(16)}$$

4.2.3. Pengujian LCD

4.2.3.1. Tujuan

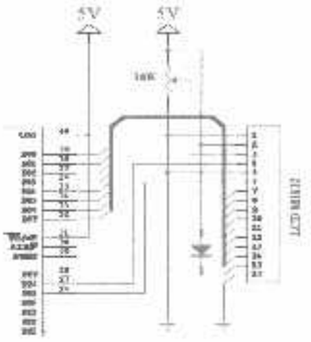
Adapun tujuan dari pengujian rangkaian ini untuk mengetahui kondisi keluaran LCD yaitu sebagai tampilan,juga mencatat nilai tegangan yang masuk pada LCD sebelum dan sesudah melewati diode.

4.2.3.2. Alat-alat yang digunakan

- LCD
- Rangkaian mikrokontroler AT 89S52.
- Catu daya.
- Voltmeter digital

4.2.3.3. Prosedur pengujian

1. Menyusun rangkaian pengujian seperti pada gambar 4.5.

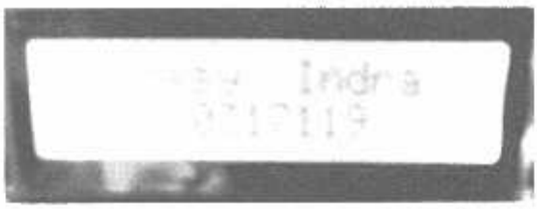


Gambar 4.5 Rangkaian Pengujian LCD

2. Membuat software pengujian rangkaian LCD, program ini berisi inisialisasi *mikrokontroler* dan LCD.
3. Mengaktifkan catu daya.
4. Mengoperasikan program dan hasil keluaran akan ditunjukkan pada layar penampil kristal cair.
5. Mengukur besarnya tegangan awal yang masuk pada LCD dan tegangan setelah lewat pada dioda

4.2.3.4. Hasil pengujian

Dari hasil pengujian maka didapatkan tampilan seperti yang terlihat pada gambar berikut ini :



Gambar 4.6 Hasil Pengujian LCD

Tabel 4.5. Hasil Pengukuran Pengujian Rangkaian LCD

No	Tegangan Awal LCD (Volt)	Tegangan Setelah Melewati Dioda (Volt)
1	4,87	4,25

Gambar 4.7 Pengukuran Tegangan Awal LCD

Gambar 4.8 Pengukuran Tegangan Setelah Melewati Dioda.

4.2.4. Pengujian Keypad 4 x 4

4.2.4.1. Tujuan

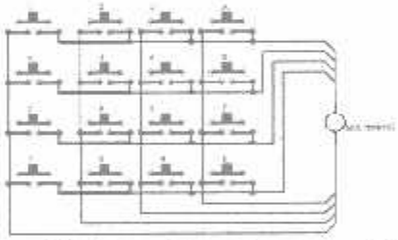
Untuk menguji apakah tombol keypad dapat bekerja sebagai inputan,dan mensimulasikan tombol yang ditekan melalui suara buzzer pada multimeter digital.

4.2.4.2. Alat yang digunakan

- Multimeter digital
- Keypad

4.2.4.3. Prosedur Pengujian

1. Menyusun rangkaian pengujian keypad seperti pada gambar 4.9.



Gambar 4.9 Pengujian Rangkaian Keypad.

2. Memberikan kombinasi masukan dengan menekan tombol-tombol keypad.
3. Mengamati hasil penekanan keypad. Kemudian mencatat hasil pengamatan pada tabel 4.6.

4.2.4.4. Hasil Pengujian

Tabel 4.6 Hasil Pengujian Keypad.

TOMBOL	BARIS				KOLOM			
	1	2	3	4	1	2	3	4
1	1	0	0	0	1	0	0	0
2	1	0	0	0	0	1	0	0
3	1	0	0	0	0	0	1	0
A	1	0	0	0	0	0	0	1
4	0	1	0	0	1	0	0	0
5	0	1	0	0	0	1	0	0
6	0	1	0	0	0	0	1	0
B	0	1	0	0	0	0	0	1
7	0	0	1	0	1	0	0	0
8	0	0	1	0	0	1	0	0
9	0	0	1	0	0	0	1	0
C	0	0	1	0	0	0	0	1
#	0	0	0	1	1	0	0	0
0	0	0	0	1	0	1	0	0
*	0	0	0	1	0	0	1	0
D	0	0	0	1	0	0	0	1

*Keterangan : cara membaca tabel diatas adalah jika antara baris dan kolom terhubung (1) maka akan membentuk matrik baris dan kolom sesuai penekanan tombol keypad.

Gambar 4.10 Pengecekan Jalur Keypad Dengan Multimeter.

- Analisa Hasil Pengujian

Dari rangkaian pengujian didapatkan bahwa untuk membentuk satu karakter penekanan keypad maka baris dan kolom harus terhubung. Sebagai contoh : jika angka 1 ditekan kemudian mengececknya menggunakan multimeter pada baris 1 dan kolom 1 maka akan terdengar suara buzzer pada multimeter,begitu seterusnya pada penekanan keypad yang lain sesuai tabel 4.6.

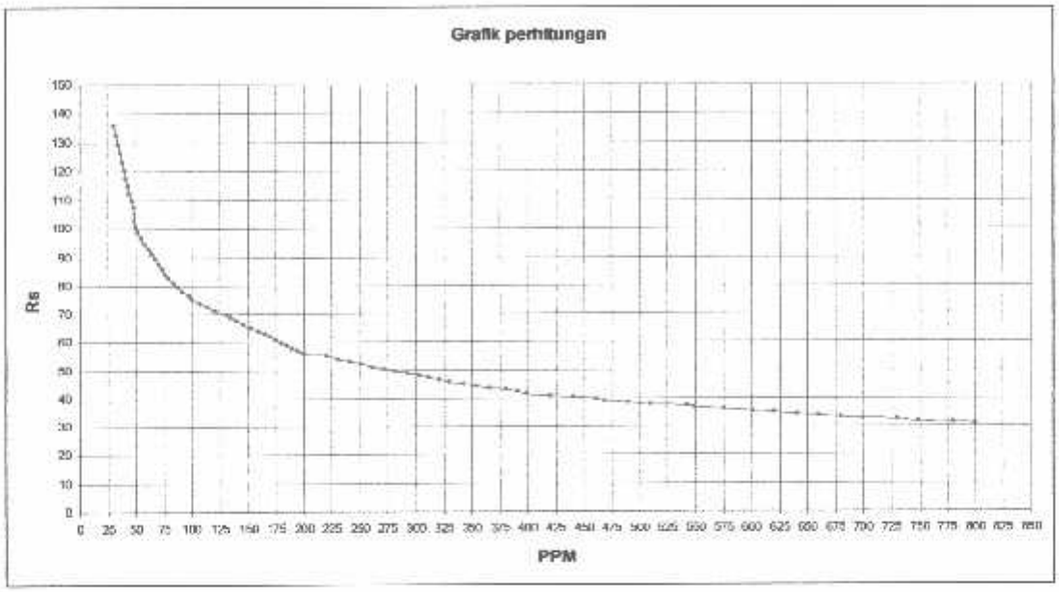
4.2.5. Pengujian Kesceluruhan Alat

Dari pengujian secara kesceluruhan didapatkan hasil tabel dan grafik seperti dibawah ini:

Tabel 4.7 Hasil Pengujian Alat

ADC	RS Ω Sensor	PPM
50	135.30	30.07
51	132.05	32.01
52	128.91	33.98
53	125.87	35.96
54	122.92	37.97
55	120.05	40.02
56	117.40	41.36
57	114.70	43.09
58	112.11	44.04
59	109.29	46.55
60	107.06	47.46
61	104.86	48.39
62	102.59	49.28
63	100.47	50.23
64	98.55	51.98
65	96.51	55.01
66	94.51	58.07
67	92.58	61.12
68	90.75	64.10
69	88.95	67.11
70	87.19	70.15
71	85.55	73.04
72	83.94	75.95
73	82.37	78.88
74	80.71	84.12
75	79.23	88.04
76	77.78	91.97
77	76.24	97.25

ADC	RS Ω Hitung	PPM
50	135.37	30.07
51	132.07	32.01
52	128.89	33.98
53	125.84	35.96
54	122.90	37.97
55	120.06	40.02
56	117.33	41.36
57	114.69	43.09
58	112.14	44.04
59	109.68	46.55
60	107.31	47.46
61	105.01	48.39
62	102.78	49.28
63	100.62	50.23
64	98.54	51.98
65	96.51	55.01
66	94.55	58.07
67	92.65	61.12
68	90.80	64.10
69	89.01	67.11
70	87.26	70.15
71	85.57	73.04
72	83.92	75.95
73	82.32	78.88
74	80.76	84.12
75	79.24	88.04
76	77.77	91.97
77	76.33	97.25



Gambar 4.12 Grafik Hasil Perhitungan Sensor TGS 826

BAB V

PENUTUP

5.1. Kesimpulan

Dari pembahasan Perancangan dan pembuatan alat pendeteksi kadar amoniak pada kamar mandi, dapat diambil kesimpulan, yaitu :

- Nilai Rs sangat berpengaruh pada kadar amoniak, Semakin besar nilai Rs maka nilai PPM juga akan semakin rendah begitu pula sebaliknya.
- Pada pengujian untuk 6 sampel yang memiliki nilai Rs yang sangat besar perbedaannya maka didapatkan error rata-rata sebesar 0.37%.
- Sensor TGS 826 mampu digunakan untuk mendeteksi kadar amoniak secara baik pada kamar mandi, tingkat keakuratan sensor adalah sebesar 99.63%

5.2. Saran

- Bagi peneliti selanjutnya diharapkan bisa mengaplikasikan TGS 826 (pendeteksi kadar amoniak) ini bukan hanya pada kamar mandi saja, melainkan untuk bidang yang lain.
- Diharapkan kedepannya bisa menentukan berapa kadar/sensitifitas dari zat-zat yang dapat dideteksi oleh TGS 826 diantaranya Air, Iso-butane, Hydrogen, Ethanol.

DAFTAR PUSTAKA

1. Innovative_electronics.
2. www.Figarosensor.com
3. Data Sheet AT89S8252
4. Data Sheet LCD M1632
5. Putra.E.A,2002,"*Belajar Mikrokontroller T89C51/52/53*",Yogyakarta,Gava Media
6. www.atmel.com

FIGARO

PRODUCT INFORMATION

TGS 826 - for the Detection of Ammonia

Features:

* High sensitivity to ammonia
* Quick response to low concentrations of ammonia
* Uses simple electrical circuit
* Ceramic base resistant to severe environment

Applications:

* Ammonia leak detection in refrigerators
* Ventilation control for the agricultural and poultry industries

The sensing element of TGS826 is a metal oxide semiconductor which has low conductivity in clean air. In the presence of a detectable gas, the sensor's conductivity increases depending on the gas concentration in the air. A simple electrical circuit can convert the change in conductivity to an output signal which corresponds to the gas concentration.

The TGS826 has high sensitivity to ammonia gas. The sensor can detect concentrations as low as 30ppm in the air and is ideally suited to critical safety-related applications such as the detection of ammonia leaks in refrigeration systems and ammonia detection in the agricultural field.

The figure below represents typical sensitivity characteristics, all data having been gathered at standard test conditions (see reverse side of this sheet). The Y-axis is indicated as *sensor resistance ratio* (Rs/Ro) which is defined as follows:

Rs = Sensor resistance of displayed gases at various concentrations

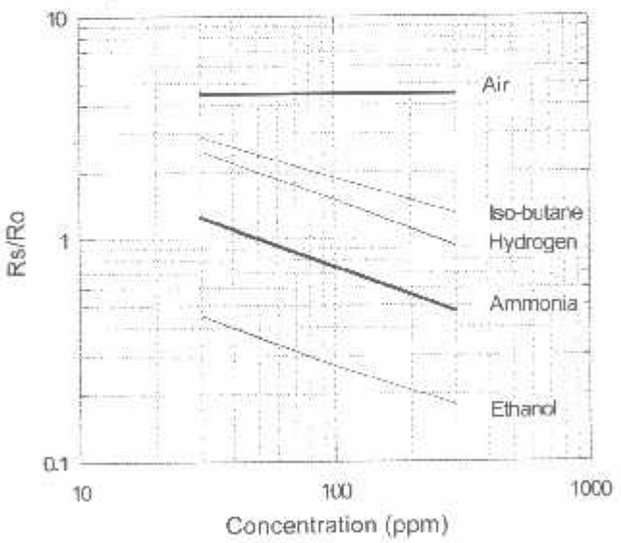
Ro = Sensor resistance at 50ppm of ammonia

The figure below represents typical temperature and humicity dependency characteristics. Again, the Y-axis is indicated as *sensor resistance ratio* (Rs/Ro), defined as follows:

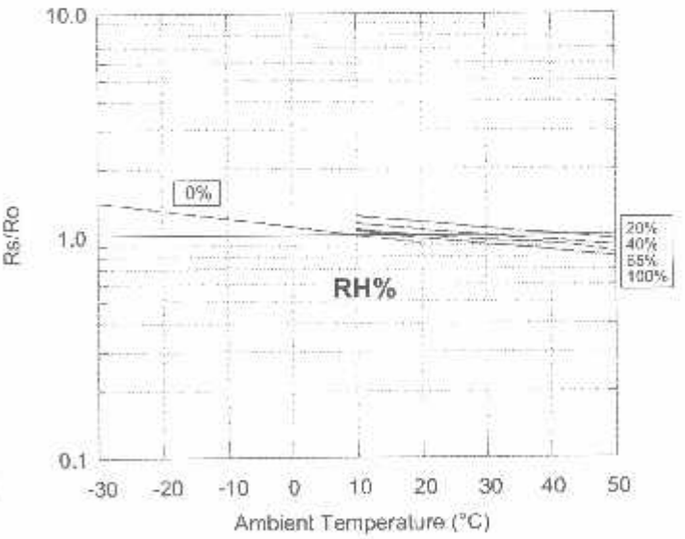
Rs = Sensor resistance at 50ppm of ammonia at various temperatures/humidities

Ro = Sensor resistance at 50ppm of ammonia at 20°C and 65% R.H.

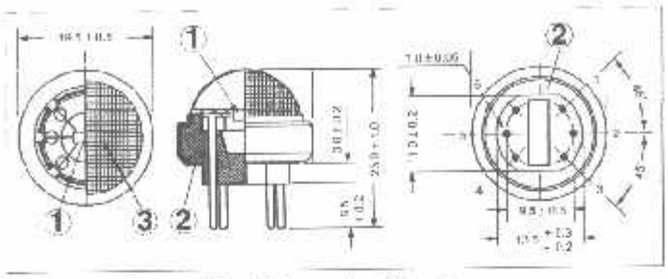
Sensitivity Characteristics:



Temperature/Humidity Dependency:



Structure and Dimensions:



(1) Sensing Element:
Metal oxide is sintered to form a thick film on the surface of an alumina ceramic tube which contains an internal heater.

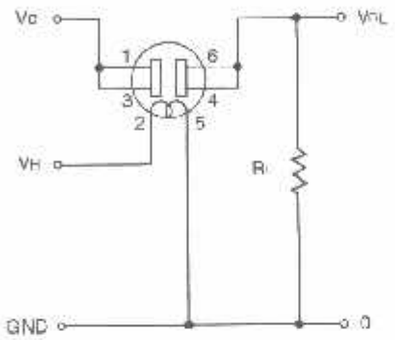
(2) Sensor Base:
Alumina ceramic

(3) Flame Arrestor:
100 mesh SUS 316 double gauze

Pin Connection and Basic Measuring Circuit:

The numbers shown around the sensor symbol in the circuit diagram at the right correspond with the pin numbers shown in the sensor's structure drawing (*above*). Since the sensor has a polarity, DC voltage is always required for circuit voltage (*a white dot indicates pin 2*). When the sensor is connected as shown in the basic circuit, output across the Load Resistor (V_{RL}) increases as the sensor's resistance (Rs) decreases, depending on gas concentration.

Basic Measuring Circuit:



Pin #2 is indicated by a white dot on the sensor's base.

Specifications:

Model number			TGS 826	
Target gases			Ammonia	
Typical detection range			30 – 300 ppm	
Standard circuit conditions	Heater Voltage	V_H	5.0±0.2V DC/AC	
	Circuit voltage	V_C	Max. 24V DC	Ps ≤ 15mW
	Load resistance	R_L	Variable	Ps ≤ 15mW
Electrical characteristics under standard test conditions	Heater resistance	R_H	33Ω at room temp.	
	Heater current	I_H	167mA	
	Heater power consumption	P_H	832mW	V_H = 5.0V DC
	Sensor resistance	Rs	20 – 100kΩ in clean air	
	Sensitivity (change rate of Rs)		0.55 – 0.75	Rs (150ppm) / Rs (50ppm)
Standard test conditions	Test gas conditions		Ammonia in air at 20° C, 65±5%RH	
	Circuit conditions		V_C = 5.0±0.2V DC V_H = 5.0±0.05V DC R_L = 33kΩ 1%	
	Conditioning period before test		7 days	

Sensor Resistance (Rs) is calculated by the following formula:

$$Rs = \left(\frac{Vc}{V_{RL}} - 1\right) \times R_L$$

Power dissipation across sensor electrodes (Ps) is calculated by the following formula:

$$Ps = \frac{Vc^2 \times Rs}{(Rs + RL)^2}$$

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Glenview, Illinois 60025
Phone: (847)-832-1701
Fax: (847)-832-1705
email: figarousa@figarosensor.com

Special Note: A more narrowly defined range of Rs or Rs/Ro will be indicated on each production lot (see Appendix). Preselected ranges of Rs or Rs/Ro are not available.

For information on warranty, please refer to Standard Terms and Conditions of Sale of Figaro USA Inc.

REV: 05/04

Appendix

TGS 826 Pre-Sorted Groupings

The TGS 826 sensor has a wide specification range in terms of its rated value in 50ppm of NH_3 and sensor resistance ratic (Rs in 150ppm of NH_3 / Rs in 50ppm of NH_3). To facilitate usage of this sensor, TGS 826 is shipped in pre-sorted groupings of 20 pieces per bag, with each bag marked with one of the following group numbers which indicate a more narrow range within the specification.

Please be advised that the sensor is produced to meet the overall specification range—production of specific groupings within the spec cannot be done. As a result, if a user requests a specific group(s), the sensor can be made available at an additional charge, but no guarantee can be offered as to availability for shipment. The minimum delivery time for special group selection should be considered at 8 weeks minimum.

Group #	Rs in 50ppm of NH_3 (kΩ)			Rs (in 150ppm of NH_3) / Rs (in 50ppm of NH_3)		
1-A	20 ~ 30			0.4 ~ 0.5		
1-B	20 ~ 30				0.5 ~ 0.6	
1-C	20 ~ 30					0.6 ~ 0.7
2-A		30 ~ 40		0.4 ~ 0.5		
2-B		30 ~ 40			0.5 ~ 0.6	
2-C		30 ~ 40				0.6 ~ 0.7
3-A			40 ~ 53	0.4 ~ 0.5		
3-B			40 ~ 53		0.5 ~ 0.6	
3-C			40 ~ 53			0.6 ~ 0.7
4-A	53 ~ 70			0.4 ~ 0.5		
4-B	53 ~ 70				0.5 ~ 0.6	
4-C	53 ~ 70					0.6 ~ 0.7
5-A		70 ~ 85		0.4 ~ 0.5		
5-B		70 ~ 85			0.5 ~ 0.6	
5-C		70 ~ 85				0.6 ~ 0.7
6-A			85 ~ 100	0.4 ~ 0.5		
6-B			85 ~ 100		0.5 ~ 0.6	
6-C			85 ~ 100			0.6 ~ 0.7

```
        org     00h
;
        Pint    Bit P2.0                ; pintu
        Sirm    Bit P2.1                ; siram
        Smpr    Bit P2.2                ; semprot
        Fan0    Bit P2.3                ; fan 0
        Fan1    Bit P2.4                ; fan 1
        Rest    Bit P2.5
        Enbl    Bit P2.6
        Eecn    Data 96h                ; data eeprom control
        Eeen    Equ 00001000b           ; bit eeprom enable (read)
        Eewr    Equ 00010000b           ; bit eeprom write
        Wtdg    Equ 00000010b           ; bit watchdog
        Stts    Bit 20h.0
        Dbts    Equ 30h
        Dadc    Equ 31h
;        Ppm0    Equ 32h
;        Ppm1    Equ 33h
;        Ppm2    Equ 34h
;        Ppm3    Equ 35h
;        Ppm4    Equ 36h
;        Ppm5    Equ 37h
        Cnt0    Equ 38h
        Cnt1    Equ 39h
        Cnt2    Equ 3Ah
        Cnt3    Equ 3Bh
        Char    Equ 3Ch
        Dly0    Equ 3Dh
        Dly1    Equ 3Eh
        Dly2    Equ 4Fh
;
init:   acall   lcd_in
        acall   rsthrd
        acall   bcmmbt
;
tunggu: mov     DPTR,#wrmght
        acall   line1
        mov     Char,#16
        acall   tulis
        mov     DPTR,#plwait
        acall   line2
        mov     Char,#16
        acall   tulis
        mov     Cnt0,#1;25
tnggu:  acall   delay3
        djnz    Cnt0,tnggu
;
mulai:  mov     DPTR,#nama
        acall   line1
        mov     Char,#16
        acall   tulis
        mov     DPTR,#nim
        acall   line2
        mov     Char,#16
        acall   tulis
        acall   delay2
        mov     DPTR,#jur
        acall   line1
        mov     Char,#16
        acall   tulis
        mov     DPTR,#univ
        acall   line2
        mov     Char,#16
```

```
        acall   tulis
        acall   delay2
        sjmp    mulai
;
setbts: mov     DPTR,#stgbts
        acall   line1
        mov     Char,#16
        acall   tulis
stbts0: mov     A,Dbts
        cjne    A,#0,stbts1
        mov     DPTR,#pilih0
stbts1: cjne    A,#1,stbts2
        mov     DPTR,#pilih1
stbts2: cjne    A,#2,stbts3
        mov     DPTR,#pilih2
stbts3: cjne    A,#3,stbts4
        mov     DPTR,#pilih3
stbts4: cjne    A,#4,stbts5
        mov     DPTR,#pilih4
stbts5: cjne    A,#5,stbts6
        mov     DPTR,#pilih5
stbts6: cjne    A,#6,stbts7
        mov     DPTR,#pilih6
stbts7: cjne    A,#7,stbts8
        mov     DPTR,#pilih7
stbts8: cjne    A,#8,stbts9
        mov     DPTR,#pilih8
stbts9: acall   line2
        mov     Char,#16
        acall   tulis
        acall   tg_lps
stbtsA: acall   scnkpd
        cjne    R0,#11,stbtsB
        mov     SP,#07h
        ljmp    mulai
stbtsB: cjne    R0,#15,stbtsD
        dec     Dbts
        mov     A,Dbts
        cjne    A,#255,stbtsC
        mov     Dbts,#0
stbtsC: acall   tlmmbt
        ljmp    stbts0
stbtsD: cjne    R0,#16,stbtsA
        inc     Dbts
        mov     A,Dbts
        cjne    A,#9,stbtsE
        mov     Dbts,#8
stbtsE: acall   tlmmbt
        ljmp    stbts0
;
bdgdta: jb      Pint,bdgdt8
        mov     A,Dbts
        cjne    A,#0,bdgdt0
        acall   prses0
        sjmp    bdgdt9
bdgdt0: cjne    A,#1,bdgdt1
        acall   prses1
        sjmp    bdgdt9
bdgdt1: cjne    A,#2,bdgdt2
        acall   prses2
        sjmp    bdgdt9
bdgdt2: cjne    A,#3,bdgdt3
        acall   prses3
```

```
        sjmp    bdgdt9
bdgdt3: cjne    A,#4,bdgdt4
        acall   prses4
        sjmp    bdgdt9
bdgdt4: cjne    A,#5,bdgdt5
        acall   prses5
        sjmp    bdgdt9
bdgdt5: cjne    A,#6,bdgdt6
        acall   prses6
        sjmp    bdgdt9
bdgdt6: cjne    A,#7,bdgdt7
        acall   prses7
        sjmp    bdgdt9
bdgdt7: cjne    A,#8,bdgdt9
        acall   prses8
        sjmp    bdgdt9
bdgdt8: clr     Fan0                    ; matikan fan 0
        clr     Fan1                    ; matikan fan 1
        clr     Smpr                    ; matikan semprot
        clr     Sirm                    ; matikan siram
bdgdt9: ret
;
prses0: mov     A,Dadc
        mov     B,#79                   ; batas 1
        div     AB
        jnz     prss00
        clr     Fan0                    ; matikan fan 0
        clr     Fan1                    ; matikan fan 1
        clr     Smpr                    ; matikan semprot
        clr     Sirm                    ; matikan siram
        sjmp    prss03
prss00: mov     A,Dadc
        mov     B,#82                   ; batas 2
        div     AB
        jnz     prss01
        setb    Fan0                    ; nyalakan fan 0
        setb    Fan1                    ; nyalakan fan 1
        clr     Smpr                    ; matikan semprot
        clr     Sirm                    ; matikan siram
        clr     Stts
        sjmp    prss03
prss01: mov     A,Dadc
        mov     B,#86                   ; batas 3
        div     AB
        jnz     prss02
        setb    Fan0                    ; nyalakan fan 0
        setb    Fan1                    ; nyalakan fan 1
        clr     Sirm                    ; matikan siram
        jb      Stts,prss03
        setb    Stts
        setb    Smpr                    ; nyalakan semprot
        acall   delay1
        acall   delay1
        clr     Smpr
        sjmp    prss03
prss02: setb    Fan0                    ; nyalakan fan 0
        setb    Fan1                    ; nyalakan fan 1
;        setb    Smpr                   ; nyakakan semprot
        setb    Sirm                    ; nyalakan siram
prss03: ret
;
prses1: mov     A,Dadc
        mov     B,#86                    ; batas 1
```

```
        div     AB
        jnz     prss10
        clr     Fan0                    ; matikan fan 0
        clr     Fan1                    ; matikan fan 1
        clr     Smpr                    ; matikan semprot
        clr     Sirm                    ; matikan siram
        sjmp    prss13
prss10: mov     A,Dadc
        mov     B,#91                   ; batas 2
        div     AB
        jnz     prss11
        setb    Fan0                    ; nyalakan fan 0
        setb    Fan1                    ; nyalakan fan 1
        clr     Smpr                    ; matikan semprot
        clr     Sirm                    ; matikan siram
        clr     Stts
        sjmp    prss13
prss11: mov     A,Dadc
        mov     B,#96                   ; batas 3
        div     AB
        jnz     prss12
        setb    Fan0                    ; nyalakan fan 0
        setb    Fan1                    ; nyalakan fan 1
        clr     Sirm                    ; matikan siram
        jb      Stts,prss13
        setb    Stts
        setb    Smpr                    ; nyalakan semprot
        acall   delay1
        acall   delay1
        clr     Smpr
        sjmp    prss13
prss12: setb    Fan0                    ; nyalakan fan 0
        setb    Fan1                    ; nyalakan fan 1
;        setb    Smpr                   ; nyalakan semprot
        setb    Sirm                    ; nyalakan siram
prss13: ret
;
prses2: mov     A,Dadc
        mov     B,#96                   ; batas 1
        div     AB
        jnz     prss20
        clr     Fan0                    ; matikan fan 0
        clr     Fan1                    ; matikan fan 1
        clr     Smpr                    ; matikan semprot
        clr     Sirm                    ; matikan siram
        sjmp    prss23
prss20: mov     A,Dadc
        mov     B,#97                   ; batas 2
        div     AB
        jnz     prss21
        setb    Fan0                    ; nyalakan fan 0
        setb    Fan1                    ; nyalakan fan 1
        clr     Smpr                    ; matikan semprot
        clr     Sirm                    ; matikan siram
        clr     Stts
        sjmp    prss23
prss21: mov     A,Dadc
        mov     B,#99                   ; batas 3
        div     AB
        jnz     prss22
        setb    Fan0                    ; nyalakan fan 0
        setb    Fan1                    ; nyalakan fan 1
        clr     Sirm                    ; matikan siram
```

```
        jb      Stts,prss23
        setb    Stts
        setb    Smpr                    ; nyalakan semprot
        acall   delay1
        acall   delay1
        clr     Smpr
        sjmp    prss23
prss22: setb    Fan0                    ; nyalakan fan 0
        setb    Fan1                    ; nyalakan fan 1
;        setb    Smpr                   ; nyalakan semprot
        setb    Sirm                    ; nyalakan siram
prss23: ret
;
prses3: mov     A,Dadc
        mov     B,#99                   ; batas 1
        div     AB
        jnz     prss30
        clr     Fan0                    ; matikan fan 0
        clr     Fan1                    ; matikan fan 1
        clr     Smpr                    ; matikan semprot
        clr     Sirm                    ; matikan siram
        sjmp    prss33
prss30: mov     A,Dadc
        mov     B,#102                  ; batas 2
        div     AB
        jnz     prss31
        setb    Fan0                    ; nyalakan fan 0
        setb    Fan1                    ; nyalakan fan 1
        clr     Smpr                    ; matikan semprot
        clr     Sirm                    ; matikan siram
        clr     Stts
        sjmp    prss33
prss31: mov     A,Dadc
        mov     B,#104                  ; batas 3
        div     AB
        jnz     prss32
        setb    Fan0                    ; nyalakan fan 0
        setb    Fan1                    ; nyalakan fan 1
        clr     Sirm                    ; matikan siram
        jb      Stts,prss33
        setb    Stts
        setb    Smpr                    ; nyalakan semprot
        acall   delay1
        acall   delay1
        clr     Smpr
        sjmp    prss33
prss32: setb    Fan0                    ; nyalakan fan 0
        setb    Fan1                    ; nyalakan fan 1
;        setb    Smpr                   ; nyalakan semprot
        setb    Sirm                    ; nyalakan siram
prss33: ret
;
prses4: mov     A,Dadc
        mov     B,#104                  ; batas 1
        div     AB
        jnz     prss40
        clr     Fan0                    ; matikan fan 0
        clr     Fan1                    ; matikan fan 1
        clr     Smpr                    ; matikan semprot
        clr     Sirm                    ; matikan siram
        sjmp    prss43
prss40: mov     A,Dadc
        mov     B,#107                  ; batas 2
```

```
        div     AB
        jnz     prss41
        setb    Fan0                    ; nyalakan fan 0
        setb    Fan1                    ; nyalakan fan 1
        clr     Smpr                    ; matikan semprot
        clr     Sirm                    ; matikan siram
        clr     Stts
        sjmp    prss43
prss41: mov     A,Dadc
        mov     B,#109                  ; batas 3
        div     AB
        jnz     prss42
        setb    Fan0                    ; nyalakan fan 0
        setb    Fan1                    ; nyalakan fan 1
        clr     Sirm                    ; matikan siram
        jb      Stts,prss43
        setb    Stts
        setb    Smpr                    ; nyalakan semprot
        acall   delay1
        acall   delay1
        clr     Smpr
        sjmp    prss43
prss42: setb    Fan0                    ; nyalakan fan 0
        setb    Fan1                    ; nyalakan fan 1
;        setb    Smpr                   ; nyalakan semprot
        setb    Sirm                    ; nyalakan siram
prss43: ret
;
prses5: mov     A,Dadc
        mov     B,#109                  ; batas 1
        div     AB
        jnz     prss50
        clr     Fan0                    ; matikan fan 0
        clr     Fan1                    ; matikan fan 1
        clr     Smpr                    ; matikan semprot
        clr     Sirm                    ; matikan siram
        sjmp    prss53
prss50: mov     A,Dadc
        mov     B,#111                  ; batas 2
        div     AB
        jnz     prss51
        setb    Fan0                    ; nyalakan fan 0
        setb    Fan1                    ; nyalakan fan 1
        clr     Smpr                    ; matikan semprot
        clr     Sirm                    ; matikan siram
        clr     Stts
        sjmp    prss53
prss51: mov     A,Dadc
        mov     B,#114                  ; batas 3
        div     AB
        jnz     prss52
        setb    Fan0                    ; nyalakan fan 0
        setb    Fan1                    ; nyalakan fan 1
        clr     Sirm                    ; matikan siram
        jb      Stts,prss53
        setb    Stts
        setb    Smpr                    ; nyalakan semprot
        acall   delay1
        acall   delay1
        clr     Smpr
        sjmp    prss53
prss52: setb    Fan0                    ; nyalakan fan 0
        setb    Fan1                    ; nyalakan fan 1
```

```
                                        Yossy
                                         ; nyalakan semprot
                                         ; nyalakan siram
;         setb    Smpr
;        setb    Sirm
prss53: ret
;
prses6: mov     A,Dadc                   ; batas 1
        mov     B,#114
        div     AB
        jnz     prss60                   ; matikan fan 0
        clr     Fan0                     ; matikan fan 1
        clr     Fan1                     ; matikan semprot
        clr     Smpr                     ; matikan siram
        clr     Sirm
        sjmp    prss63                   ; batas 2
 prss60: mov    A,Dadc
        mov     B,#115
        div     AB
        jnz     prss61                   ; nyalakan fan 0
        setb    Fan0                     ; nyalakan fan 1
        setb    Fan1                     ; matikan semprot
        clr     Smpr                     ; matikan siram
        clr     Sirm
        clr     Stts
        sjmp    prss63                   ; batas 3
  prss61: mov   A,Dadc
        mov     B,#116
        div     AB
        jnz     prss62                   ; nyalakan fan 0
        setb    Fan0                     ; nyalakan fan 1
        setb    Fan1                     ; matikan siram
        clr     Sirm
        jb      Stts,prss63              ; nyalakan semprot
        setb    Stts
        setb    Smpr
        acall   delay1
        acall   delay1
        clr     Smpr
        sjmp    prss63                   ; nyalakan fan 0
   prss62: setb Fan0                     ; nyalakan fan 1
        setb    Fan1                     ; nyalakan semprot
;        setb    Smpr                    ; nyalakan siram
        setb    Sirm
   prss63: ret
   ;
   prses7: mov  A,Dadc                   ; batas 1
        mov     B,#116
        div     AB
        jnz     prss70                   ; matikan fan 0
        clr     Fan0                     ; matikan fan 1
        clr     Fan1                     ; matikan semprot
        clr     Smpr                     ; matikan siram
        clr     Sirm
        sjmp    prss73                   ; batas 2
    prss70: mov A,Dadc
        mov     B,#118
        div     AB
        jnz     prss71                   ; nyalakan fan 0
        setb    Fan0                     ; nyalakan fan 1
        setb    Fan1                     ; matikan semprot
        clr     Smpr                     ; matikan siram
        clr     Sirm
        clr     Stts
        sjmp    prss73
     prss71: mov A,Dadc                  Page 7
```

```
                                    Yossy
                                     ; batas 3
        mov     B,#119
        div     AB
        jnz     prss72              ; nyalakan fan 0
        setb    Fan0                ; nyalakan fan 1
        setb    Fan1                ; matikan siram
        clr     Sirm
        jb      Stts,prss73         ; nyalakan semprot
        setb    Stts
        setb    Smpr
        acall   delay1
        acall   delay1
        clr     Smpr
        sjmp    prss73              ; nyalakan fan 0
prss72: setb    Fan0                ; nyalakan fan 1
        setb    Fan1                ; nyalakan semprot
;        setb    Smpr               ; nyalakan siram
        setb    Sirm
prss73: ret
;
prses8: mov     A,Dadc              ; batas 1
        mov     B,#119
        div     AB
        jnz     prss80              ; matikan fan 0
        clr     Fan0                ; matikan fan 1
        clr     Fan1                ; matikan semprot
        clr     Smpr                ; matikan siram
        clr     Sirm
        sjmp    prss83
prss80: mov     A,Dadc              ; batas 2
        mov     B,#120
        div     AB
        jnz     prss81              ; nyalakan fan 0
        setb    Fan0                ; nyalakan fan 1
        setb    Fan1                ; matikan semprot
        clr     Smpr                ; matikan siram
        clr     Sirm
        clr     Stts
        sjmp    prss83
prss81: mov     A,Dadc              ; batas 3
        mov     B,#122
        div     AB
        jnz     prss82              ; nyalakan fan 0
        setb    Fan0                ; nyalakan fan 1
        setb    Fan1                ; matikan siram
        clr     Sirm
        jb      Stts,prss82         ; nyalakan semprot
        setb    Stts
        setb    Smpr
        acall   delay1
        acall   delay1
        clr     Smpr
        sjmp    prss83              ; nyalakan fan 0
prss82: setb    Fan0                ; nyalakan fan 1
        setb    Fan1                ; nyalakan semprot
;        setb    Smpr               ; nyalakan siram
        setb    Sirm
prss83: ret
;
kalbrs: acall   lcdclr
        mov     DPTR,#adcppm
        acall   line1
        mov     Char,#16
        acall   tulis


```

```
          acall   tg_lps
klbrs0:   mov     A,P3
          mov     Dadc,A
          mov     B,#50
          div     AB
          cjne    A,#0,klbrs1
          mov     Dadc,#50
          sjmp    klbrs3
klbrs1:   mov     A,Dadc
          mov     B,#133
          div     AB
          cjne    A,#0,klbrs2
          sjmp    klbrs3
klbrs2:   mov     Dadc,#132
klbrs3:   mov     DPTR,#angka
          mov     P0,#0C2h
          acall   w_ins
          mov     A,Dadc
          acall   nilai
          mov     P0,#0CAh
          acall   w_ins
          mov     A,Dadc
          mov     DPTR,#lokup0
          movc    A,@A+DPTR
          mov     B,#10
          div     AB
          mov     DPTR,#angka
          acall   wr_chr
          mov     A,B
          acall   wr_chr
          mov     A,Dadc
          mov     DPTR,#lokup1
          movc    A,@A+DPTR
          mov     B,#10
          div     AB
          mov     DPTR,#angka
          acall   wr_chr
          mov     P0,#'.'
          acall   w_chr
          mov     A,B
          acall   wr_chr
          mov     P0,#0D0h
          acall   w_ins
          acall   bdgdta
          acall   delay1
          acall   scnkpd
          cjne    R0,#11,klbrs0
          mov     SP,#07h
          ljmp    mulai

;
nilai:    mov     B,#100
          div     AB
          acall   wr_chr
          mov     A,B
          mov     B,#10
          div     AB
          acall   wr_chr
          mov     A,B
          acall   wr_chr
          ret

;
rsthrd:   clr     Fan0
          clr     Fan1
```

```
        clr     Sirm
        clr     Smpr
        clr     Stts
        ret

;
stwrmm: orl     Eecn,#Eeen
        orl     Eecn,#Eewr
        ret

;
enwrmm: xrl     Eecn,#Eewr
        xrl     Eecn,#Eeen
        ret

;
strdmm: orl     Eecn,#Eeen
        ret

;
enrdmm: xrl     Eecn,#Eeen
        ret

;
wt_wr:  mov     A,Eecn
        anl     A,#Wtdg
        jz      wt_wr
        ret

;
cknull: cjne    A,#0FFh,cknul
        mov     A,#00h
cknul:  ret
;
bcmmbt: acall   strdmm
        mov     DPTR,#00
        movx    A,@DPTR
        lcall   cknull
        mov     Dbts,A
        acall   enrdmm
        ret

;
tlmmbt: acall   stwrmm
        mov     DPTR,#00h
        mov     A,Dbts
        movx    @DPTR,A
        lcall   wt_wr
        lcall   enwrmm
        ret

;
line1:  mov     P0,#080h
        acall   w_ins
        ret

;
line2:  mov     P0,#0C0h
        acall   w_ins
        ret

;
tulis:  clr     A
        movc    A,@A+DPTR
        mov     P0,A
        inc     DPTR
        acall   w_chr
        djnz    Char,tulis
        ret

;
wr_chr: movc    A,@A+DPTR
        mov     P0,A
        acall   w_chr
```

```
        ret
;
w_ins:  clr     Enbl
        clr     Rest
        setb    Enbl
        clr     Enbl
        acall   delay0
        ret
;
w_chr:  clr     Enbl
        setb    Rest
        setb    Enbl
        clr     Enbl
        acall   delay0
        ret
;
lcd_in: acall   delay1                  ; Display Clear
        mov     P0,#01h
        acall   w_ins
        mov     P0,#38h                 ; Function Set
        acall   w_ins
        mov     P0,#0Dh                 ; Display On, Cursor, Blink
        acall   w_ins
        mov     P0,#06h                 ; Entry Mode
        acall   w_ins
        mov     P0,#02h                 ; Cursor Home
        acall   w_ins
        ret
;
lcdclr: mov     P0,#01h                 ; Display Clear
        acall   w_ins
        acall   delay0
        acall   delay0
        ret
;
scnkpd: mov     R0,#10
        lcall   delay0
col1:   mov     P1,#11111110b
        mov     A,P1
c1b1:   cjne    A,#11101110b,c1b2
        mov     R0,#1
c1b2:   cjne    A,#11011110b,c1b3
        mov     R0,#2
c1b3:   cjne    A,#10111110b,c1b4
        mov     R0,#3
c1b4:   cjne    A,#01111110b,col2
        mov     R0,#13
;
col2:   mov     P1,#11111101b
        mov     A,P1
c2b1:   cjne    A,#11101101b,c2b2
        mov     R0,#4
c2b2:   cjne    A,#11011101b,c2b3
        mov     R0,#5
c2b3:   cjne    A,#10111101b,c2b4
        mov     R0,#6
c2b4:   cjne    A,#01111101b,col3
        mov     R0,#14
;
col3:   mov     P1,#11111011b
        mov     A,P1
c3b1:   cjne    A,#11101011b,c3b2
        mov     R0,#7
```

```
c3b2:   cjne    A,#11011011b,c3b3
        mov     R0,#8
c3b3:   cjne    A,#10111011b,c3b4
        mov     R0,#9
c3b4:   cjne    A,#01111011b,col4
        mov     R0,#15
;
col4:   mov     P1,#11110111b
        mov     A,P1
c4b1:   cjne    A,#11100111b,c4b2
        mov     R0,#11
c4b2:   cjne    A,#11010111b,c4b3
        mov     R0,#0
c4b3:   cjne    A,#10110111b,c4b4
        mov     R0,#12
c4b4:   cjne    A,#01110111b,back
        mov     R0,#16
back:   ret
;
tg_tkn: lcall   scnkpd
tg_tk0: cjne    R0,#16,tg_tk1
        ljmp    tg_tkn
tg_tk1: cjne    R0,#15,tg_tk2
        ljmp    tg_tkn
tg_tk2: cjne    R0,#14,tg_tk3
        ljmp    tg_tkn
tg_tk3: cjne    R0,#13,tg_tk4
        ljmp    tg_tkn
tg_tk4: cjne    R0,#12,tg_tk5
        ljmp    tg_tkn
tg_tk5: cjne    R0,#11,tg_tk6
        ljmp    tg_tkn
tg_tk6: cjne    R0,#10,tg_tk7
        ljmp    tg_tkn
tg_tk7: ret
;
tg_lps: lcall   scnkpd
        cjne    R0,#10,tg_lps
        ret
;
delay0: djnz    Dly0,delay0
        ret
;
delay1: acall   scnkpd
        cjne    R0,#13,dely10
        ljmp    setbts
dely10: cjne    R0,#14,dely11
        ljmp    kalbrs
dely11: djnz    Dly1,delay1
        ret
;
delay2: mov     Dly2,#20
dely2:  acall   delay1
        djnz    Dly2,dely2
        ret
;
delay3: mov     Dly2,#36
dely3:  djnz    Dly0,dely3
        djnz    Dly1,dely3
        djnz    Dly2,dely3
        ret
```

```
nim:     DB      '     0317119    '
jur:     DB      ' Teknik Elektro '
univ:    DB      '   ITN Malang   '
stgbts:  DB      '  Seting Batas  '
pilih0:  DB      '    100.0ppm    '
pilih1:  DB      '    150.0ppm    '
pilih2:  DB      '    200.0ppm    '
pilih3:  DB      '    250.0ppm    '
pilih4:  DB      '    300.0ppm    '
pilih5:  DB      '    350.0ppm    '
pilih6:  DB      '    400.0ppm    '
pilih7:  DB      '    450.0ppm    '
pilih8:  DB      '    500.0ppm    '
adcppm:  DB      '  ADC  ->  ppm  '
wrmght:  DB      ' Warming Heater '
plwait:  DB      ' Please Wait... '
angka:   DB      '0123456789      '
;
lokup0:  DB      00,00,00,00,00,00,00,00,00,00      ; 000-009
         DB      00,00,00,00,00,00,00,00,00,00      ; 010-019
         DB      00,00,00,00,00,00,00,00,00,00      ; 020-029
         DB      00,00,00,00,00,00,00,00,00,00      ; 030-039
         DB      00,00,00,00,00,00,00,00,00,00      ; 040-049
         DB      03,03,03,03,03,04,04,04,04,04      ; 050-059
         DB      04,04,04,05,05,05,05,06,06,06      ; 060-069
         DB      07,07,07,07,08,08,09,09,09,10      ; 070-079
         DB      11,12,13,13,13,14,15,16,16,16      ; 080-089
         DB      17,17,18,18,19,19,22,23,24,25      ; 090-099
         DB      26,27,28,29,30,31,32,33,34,35      ; 100-109
         DB      36,38,39,39,42,44,46,46,48,51      ; 110-119
         DB      54,54,57,60,62,64,66,67,69,73      ; 120-129
         DB      74,78,79,00,00,00,00,00,00,00      ; 130-139
         DB      00,00,00,00,00,00,00,00,00,00      ; 140-149
         DB      00,00,00,00,00,00,00,00,00,00      ; 150-159
         DB      00,00,00,00,00,00,00,00,00,00      ; 160-169
         DB      00,00,00,00,00,00,00,00,00,00      ; 170-179
         DB      00,00,00,00,00,00,00,00,00,00      ; 180-189
         DB      00,00,00,00,00,00,00,00,00,00      ; 190-199
         DB      00,00,00,00,00,00,00,00,00,00      ; 200-209
         DB      00,00,00,00,00,00,00,00,00,00      ; 210-219
         DB      00,00,00,00,00,00,00,00,00,00      ; 220-229
         DB      00,00,00,00,00,00,00,00,00,00      ; 230-239
         DB      00,00,00,00,00,00,00,00,00,00      ; 240-249
         DB      00,00,00,00,00,00                  ; 250-255
;
lokup1:  DB      00,00,00,00,00,00,00,00,00,00      ; 000-009
         DB      00,00,00,00,00,00,00,00,00,00      ; 010-019
         DB      00,00,00,00,00,00,00,00,00,00      ; 020-029
         DB      00,00,00,00,00,00,00,00,00,00      ; 030-039
         DB      00,00,00,00,00,00,00,00,00,00      ; 040-049
         DB      00,20,39,59,79,00,13,30,40,65      ; 050-059
         DB      74,83,92,02,19,50,80,11,41,71      ; 060-069
         DB      01,30,59,88,41,80,19,72,99,75      ; 070-079
         DB      44,07,04,51,97,65,27,02,50,98      ; 080-089
         DB      46,94,43,92,41,91,10,10,10,11      ; 090-099
         DB      12,14,16,20,24,17,11,04,30,49      ; 100-109
         DB      62,09,04,99,02,06,10,93,99,00      ; 110-119
         DB      18,93,53,12,08,04,01,98,96,06      ; 120-129
         DB      95,07,96,00,00,00,00,00,00,00      ; 130-139
         DB      00,00,00,00,00,00,00,00,00,00      ; 140-149
         DB      00,00,00,00,00,00,00,00,00,00      ; 150-159
         DB      00,00,00,00,00,00,00,00,00,00      ; 160-169
         DB      00,00,00,00,00,00,00,00,00,00      ; 170-179
```

```
                                        Untitled
DB      00,00,00,00,00,00,00,00,00,00   ; 180-189
DB      00,00,00,00,00,00,00,00,00,00   ; 190-199
DB      00,00,00,00,00,00,00,00,00,00   ; 200-209
DB      00,00,00,00,00,00,00,00,00,00   ; 210-219
DB      00,00,00,00,00,00,00,00,00,00   ; 220-229
DB      00,00,00,00,00,00,00,00,00,00   ; 230-239
DB      00,00,00,00,00,00,00,00,00,00   ; 240-249
DB      00,00,00,00,00,00               ; 250-255
DB      00,00,00,00,00,00

;
        end
```

eatures

- Compatible with MCS-51™ Products
- 8K Bytes of In-System Reprogrammable Downloadable Flash Memory
  - SPI Serial Interface for Program Downloading
  - Endurance: 1,000 Write/Erase Cycles
- 2K Bytes EEPROM
  - Endurance: 100,000 Write/Erase Cycles
- 4V to 6V Operating Range
- Fully Static Operation: 0 Hz to 24 MHz
- Three-level Program Memory Lock
- 256 x 8-bit Internal RAM
- 32 Programmable I/O Lines
- Three 16-bit Timer/Counters
- Nine Interrupt Sources
- Programmable UART Serial Channel
- SPI Serial Interface
- Low-power Idle and Power-down Modes
- Interrupt Recovery From Power-down
- Programmable Watchdog Timer
- Dual Data Pointer
- Power-off Flag

escription

ıe AT89S8252 is a low-power, high-performance CMOS 8-bit microcomputer with
: bytes of downloadable Flash programmable and erasable read only memory and
: bytes of EEPROM. The device is manufactured using Atmel's high-density nonvol-
'le memory technology and is compatible with the industry-standard 80C51
ıstruction set and pinout. The on-chip downloadable Flash allows the program mem-
y to be reprogrammed in-system through an SPI serial interface or by a
nventional nonvolatile memory programmer. By combining a versatile 8-bit CPU
ıh downloadable Flash on a monolithic chip, the Atmel AT89S8252 is a powerful
'crocomputer which provides a highly-flexible and cost-effective solution to many
ıbedded control applications.

e AT89S8252 provides the following standard features: 8K bytes of downloadable
ısh, 2K bytes of EEPROM, 256 bytes of RAM, 32 I/O lines, programmable watch-
g timer, two data pointers, three 16-bit timer/counters, a six-vector two-level
errupt architecture, a full duplex serial port, on-chip oscillator, and clock circuitry. In
dition, the AT89S8252 is designed with static logic for operation down to zero fre-
ency and supports two software selectable power saving modes. The Idle Mode
)ps the CPU while allowing the RAM, timer/counters, serial port, and interrupt sys-
n to continue functioning. The Power-down mode saves the RAM contents but
ezes the oscillator, disabling all other chip functions until the next interrupt or hard-
.re reset.

e downloadable Flash can be changed a single byte at a time and is accessible
ough the SPI serial interface. Holding RESET active forces the SPI bus into a serial
)gramming interface and allows the program memory to be written to or read from
less Lock Bit 2 has been activated.

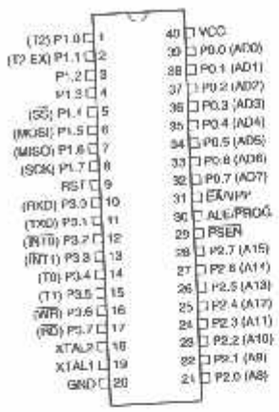
8-bit Microcontroller with 8K Bytes Flash

AT89S8252

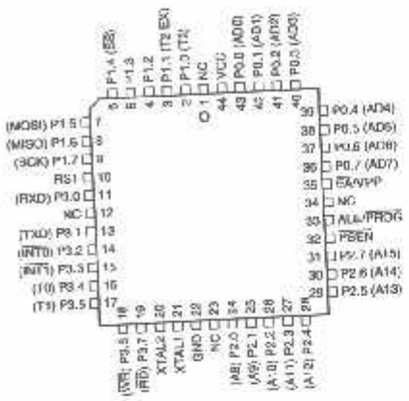
Rev. 0401E–02/00

in Configurations

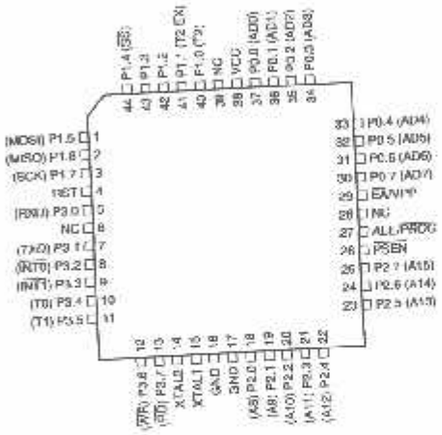
PDIP



PLCC



PQFP/TQFP



in Description

:C

pply voltage.

ND

ound.

rt 0

rt 0 is an 8-bit open drain bbl-didirectional I/O port. As an tput port, each pin can sink eight TTL inputs. When 1s e written to port 0 pins, the pins can be used as high-pedance inputs.

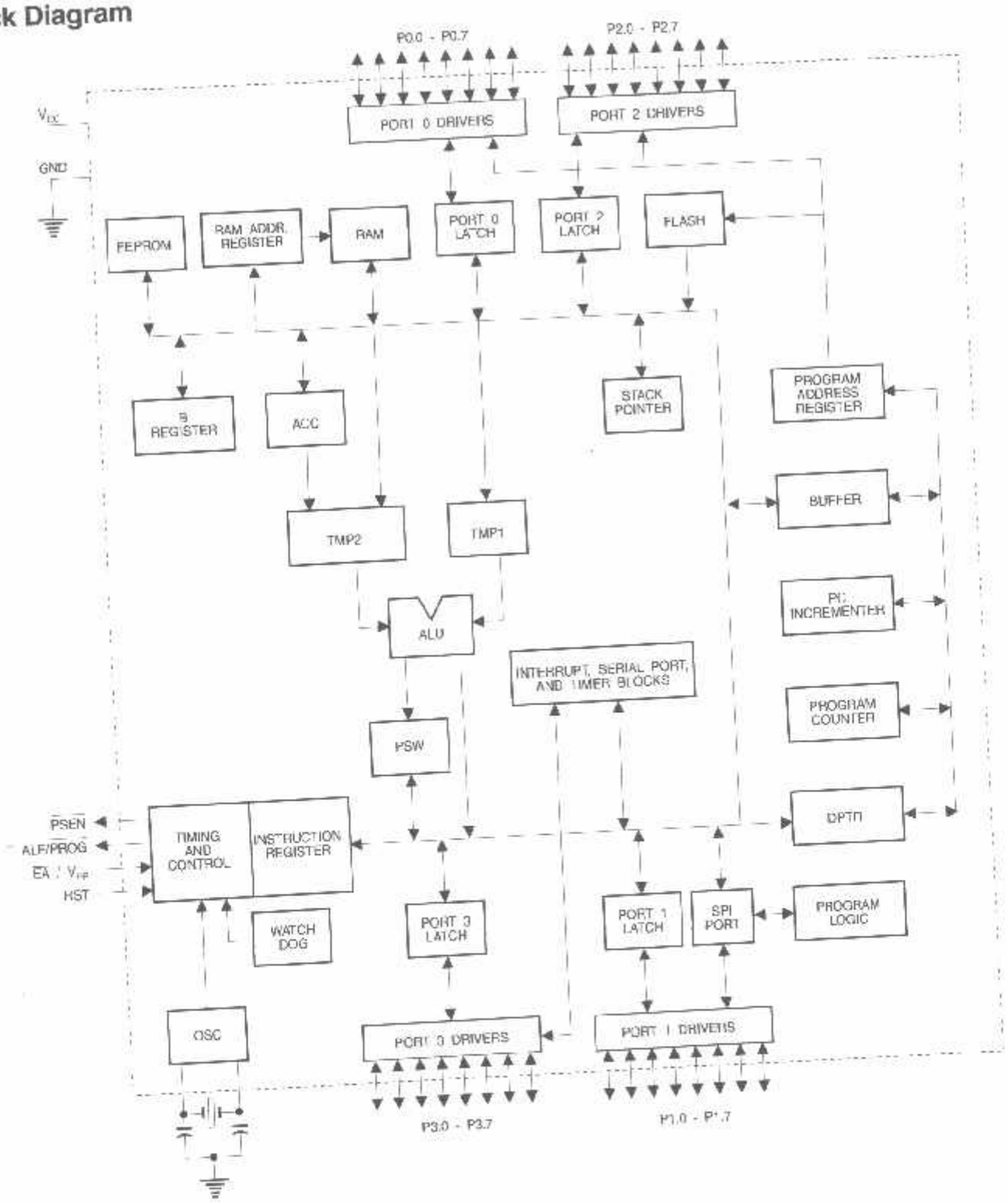
rt 0 can also be configured to be the multiplexed low-der address/data bus during accesses to external program and data memory. In this mode, P0 has internal pullups.

Port 0 also receives the code bytes during Flash programming and outputs the code bytes during program verification. External pullups are required during program verification.

Port 1

Port 1 is an 8-bit bi-directional I/O port with internal pullups. The Port 1 output buffers can sink/source four TTL inputs. When 1s are written to Port 1 pins, they are pulled high by the internal pullups and can be used as inputs. As inputs, Port 1 pins that are externally being pulled low will source current (I_{IL}) because of the internal pullups.

lock Diagram



ome Port 1 pins provide additional functions. P1.0 and 1.1 can be configured to be the timer/counter 2 external unt input (P1.0/T2) and the timer/counter 2 trigger input 1.1/T2EX), respectively.

in Description

rthermore, P1.4, P1.5, P1.6, and P1.7 can be configured the SPI slave port select, data input/output and shift ck input/output pins as shown in the following table.

ort Pin	Alternate Functions
1.0	T2 (external count input to Timer/Counter 2), clock-out
1.1	T2EX (Timer/Counter 2 capture/reload trigger and direction control)
1.4	$\overline{SS}$ (Slave port select input)
1.5	MOSI (Master data output, slave data input pin for SPI channel)
1.6	MISO (Master data input, slave data output pin for SPI channel)
1.7	SCK (Master clock output, slave clock input pin for SPI channel)

rt 1 also receives the low-order address bytes during sh programming and verification.

rt 2

t 2 is an 8-bit bi-directional I/O port with internal pullups. e Port 2 output buffers can sink/source four TTL inputs. en 1s are written to Port 2 pins, they are pulled high by internal pullups and can be used as inputs. As inputs, rt 2 pins that are externally being pulled low will source rent (I_{IL}) because of the internal pullups.

t 2 emits the high-order address byte during fetches n external program memory and during accesses to ernal data memory that use 16-bit addresses (MOVX @ TR). In this application, Port 2 uses strong internal pul- s when emitting 1s. During accesses to external data mory that use 8-bit addresses (MOVX @ RI), Port 2 its the contents of the P2 Special Function Register.

t 2 also receives the high-order address bits and some trol signals during Flash programming and verification.

t 3

t 3 is an 8 bit bi-directional I/O port with internal pullups. Port 3 output buffers can sink/source four TTL inputs. en 1s are written to Port 3 pins, they are pulled high by internal pullups and can be used as inputs. As inputs, Port 3 pins that are externally being pulled low will source current (I_{IL}) because of the pullups.

Port 3 also serves the functions of various special features of the AT89S8252, as shown in the following table.

Port 3 also receives some control signals for Flash programming and verification.

Port Pin	Alternate Functions
P3.0	RXD (serial input port)
P3.1	TXD (serial output port)
P3.2	$\overline{INT0}$ (external interrupt 0)
P3.3	$\overline{INT1}$ (external interrupt 1)
P3.4	T0 (timer 0 external input)
P3.5	T1 (timer 1 external input)
P3.6	$\overline{WR}$ (external data memory write strobe)
P3.7	$\overline{RD}$ (external data memory read strobe)

RST

Reset input. A high on this pin for two machine cycles while the oscillator is running resets the device.

ALE/$\overline{PROG}$

Address Latch Enable is an output pulse for latching the low byte of the address during accesses to external memory. This pin is also the program pulse input ($\overline{PROG}$) during Flash programming.

In normal operation, ALE is emitted at a constant rate of 1/6 the oscillator frequency and may be used for external timing or clocking purposes. Note, however, that one ALE pulse is skipped during each access to external data memory.

If desired, ALE operation can be disabled by setting bit 0 of SFR location 8EH. With the bit set, ALE is active only during a MOVX or MOVC instruction. Otherwise, the pin is weakly pulled high. Setting the ALE-disable bit has no effect if the microcontroller is in external execution mode.

$\overline{PSEN}$

Program Store Enable is the read strobe to external program memory.

When the AT89S8252 is executing code from external program memory, $\overline{PSEN}$ is activated twice each machine cycle, except that two $\overline{PSEN}$ activations are skipped during each access to external data memory.

$\overline{EA}$/VPP

External Access Enable. $\overline{EA}$ must be strapped to GND in order to enable the device to fetch code from external pro-

am memory locations starting at 0000H up to FFFFH. ote, however, that if lock bit 1 is programmed, $\overline{EA}$ will be ernally latched on reset.

$\overline{EA}$ should be strapped to V_{CC} for internal program execu- ons. This pin also receives the 12-volt programming iable voltage (V_{PP}) during Flash programming when 12- lt programming is selected.

XTAL1

Input to the inverting oscillator amplifier and input to the internal clock operating circuit.

XTAL2

Output from the inverting oscillator amplifier.

ble 1. AT89S8252 SFR Map and Reset Values

0F8H								0FFH
								0F7H
0F0H	B 00000000							0EFH
0E8H								0E7H
0E0H	ACC 00000000							0DFH
0D8H						SPCR 000001XX		0D7H
0D0H	PSW 00000000							0CFH
0C8H	T2CON 00000000	T2MOD XXXXXX00	RCAP2L 00000000	RCAP2H 00000000	TL2 00000000	TH2 00000000		0C7H
0C0H								0BFH
0B8H	IP XX000000							0B7H
0B0H	P3 11111111							0AFH
0A8H	IE 0X000000		SPSR 00XXXXXX					0A7H
0A0H	P2 11111111							9FH
98H	SCON 00000000	SBUF XXXXXXXX					WMCON 00000010	97H
90H	P1 11111111							8FH
88H	TCON 00000000	TMOD 00000000	TL0 00000000	TL1 00000000	TH0 00000000	TH1 00000000		87H
80H	P0 11111111	SP 00000111	DP0L 00000000	DP0H 00000000	DP1L 00000000	DP1H 00000000	SPDR XXXXXXXX	PCON 0XXX0000

pecial Function Registers

map of the on-chip memory area called the Special Func- in Register (SFR) space is shown in Table 1.

ote that not all of the addresses are occupied, and unoc- pied addresses may not be implemented on the chip. ead accesses to these addresses will in general return ndom data, and write accesses will have an indeterminate ect.

ser software should not write 1s to these unlisted locations, since they may be used in future products to invoke new features. In that case, the reset or inactive values of the new bits will always be 0.

Timer 2 Registers Control and status bits are contained in registers T2CON (shown in Table 2) and T2MOD (shown in Table 9) for Timer 2. The register pair (RCAP2H, RCAP2L) are the Capture/Reload registers for Timer 2 in 16 bit capture mode or 16-bit auto-reload mode.

ble 2. T2CON—Timer/Counter 2 Control Register

Reset Value = 0000 0000B

2CON Address = 0C8H

it Addressable

it	7	6	5	4	3	2	1	0
	TF2	EXF2	RCLK	TCLK	EXEN2	TR2	C/$\overline{T2}$	CP/$\overline{RL2}$

ymbol	Function
F2	Timer 2 overflow flag set by a Timer 2 overflow and must be cleared by software. TF2 will not be set when either RCLK = 1 or TCLK = 1.
XF2	Timer 2 external flag set when either a capture or reload is caused by a negative transition on T2EX and EXEN2 = 1. When Timer 2 interrupt is enabled, EXF2 = 1 will cause the CPU to vector to the Timer 2 interrupt routine. EXF2 must be cleared by software. EXF2 does not cause an interrupt in up/down counter mode (DCEN = 1).
CLK	Receive clock enable. When set, causes the serial port to use Timer 2 overflow pulses for its receive clock in serial port Modes 1 and 3. RCLK = 0 causes Timer 1 overflows to be used for the receive clock.
CLK	Transmit clock enable. When set, causes the serial port to use Timer 2 overflow pulses for its transmit clock in serial port Modes 1 and 3. TCLK = 0 causes Timer 1 overflows to be used for the transmit clock.
XEN2	Timer 2 external enable. When set, allows a capture or reload to occur as a result of a negative transition on T2EX if Timer 2 is not being used to clock the serial port. EXEN2 = 0 causes Timer 2 to ignore events at T2EX.
R2	Start/Stop control for Timer 2. TR2 = 1 starts the timer.
/T2	Timer or counter select for Timer 2. C/$\overline{T2}$ = 0 for timer function. C/$\overline{T2}$ = 1 for external event counter (falling edge triggered).
P/RL2	Capture/Reload select. CP/$\overline{RL2}$ = 1 causes captures to occur on negative transitions at T2EX if EXEN2 = 1. CP/$\overline{RL2}$ = 0 causes automatic reloads to occur when Timer 2 overflows or negative transitions occur at T2EX when EXEN2 = 1. When either RCLK or TCLK = 1, this bit is ignored and the timer is forced to auto-reload on Timer 2 overflow.

atchdog and Memory Control Register The WMCON gister contains control bits for the Watchdog Timer nown in Table 3). The EEMEN and EEMWE bits are used to select the 2K bytes on-chip EEPROM, and to enable byte-write. The DPS bit selects one of two DPTR registers available.

ble 3. WMCON—Watchdog and Memory Control Register

VMCON Address = 96H — Reset Value = 0000 0010B

	PS2	PS1	PS0	EEMWE	EEMEN	DPS	WDTRST	WDTEN
Bit	7	6	5	4	3	2	1	0

Symbol	Function
S2 S1 S0	Prescaler Bits for the Watchdog Timer. When all three bits are set to "0", the watchdog timer has a nominal period of 16 ms. When all three bits are set to "1", the nominal period is 2048 ms.
EMWE	EEPROM Data Memory Write Enable Bit. Set this bit to "1" before initiating byte write to on-chip EEPROM with the MOVX instruction. User software should set this bit to "0" after EEPROM write is completed.
EMEN	Internal EEPROM Access Enable. When EEMEN = 1, the MOVX instruction with DPTR will access on-chip EEPROM instead of external data memory. When EEMEN = 0, MOVX with DPTR accesses external data memory.
PS	Data Pointer Register Select. DPS = 0 selects the first bank of Data Pointer Register, DP0, and DPS = 1 selects the second bank, DP1
DTRST DY/$\overline{BSY}$	Watchdog Timer Reset and EEPROM Ready/Busy Flag. Each time this bit is set to "1" by user software, a pulse is generated to reset the watchdog timer. The WDTRST bit is then automatically reset to "0" in the next instruction cycle. The WDTRST bit is Write-Only. This bit also serves as the RDY/$\overline{BSY}$ flag in a Read-Only mode during EEPROM write. RDY/$\overline{BSY}$ = 1 means that the EEPROM is ready to be programmed. While programming operations are being executed, the RDY/$\overline{BSY}$ bit equals "0" and is automatically reset to "1" when programming is completed.
DTEN	Watchdog Timer Enable Bit. WDTEN = 1 enables the watchdog timer and WDTEN = 0 disables the watchdog timer.

Registers Control and status bits for the Serial Periph- l Interface are contained in registers SPCR (shown in ble 4) and SPSR (shown in Table 5). The SPI data bits contained in the SPDR register. Writing the SPI data ister during serial data transfer sets the Write Collision WCOL, in the SPSR register. The SPDR is double buff- d for writing and the values in SPDR are not changed by set.

errupt Registers The global interrupt enable bit and the ividual interrupt enable bits are in the IE register. In lition, the individual interrupt enable bit for the SPI is in SPCR register. Two priorities can be set for each of the nterrupt sources in the IP register.

Dual Data Pointer Registers To facilitate accessing both internal EEPROM and external data memory, two banks of 16 bit Data Pointer Registers are provided: DP0 at SFR address locations 82H-83H and DP1 at 84H-85H. Bit DPS = 0 in SFR WMCON selects DP0 and DPS = 1 selects DP1. The user should always initialize the DPS bit to the appropriate value before accessing the respective Data Pointer Register.

Power Off Flag The Power Off Flag (POF) is located at bit_4 (PCON.4) in the PCON SFR. POF is set to "1" during power up. It can be set and reset under software control and is not affected by RESET.

ble 4. SPCR—SPI Control Register

PCR Address = D5H — Reset Value = 0000 01XXB

Bit	SPIE	SPE	DORD	MSTR	CPOL	CPHA	SPR1	SPR0
	7	6	5	4	3	2	1	0

ymbol	Function
PIE	SPI Interrupt Enable. This bit, in conjunction with the ES bit in the IE register, enables SPI interrupts: SPIE = 1 and ES = 1 enable SPI interrupts. SPIE = 0 disables SPI interrupts.
PE	SPI Enable. SPI = 1 enables the SPI channel and connects $\overline{SS}$, MOSI, MISO and SCK to pins P1.4, P1.5, P1.6, and P1.7. SPI = 0 disables the SPI channel.
ORD	Data Order. DORD = 1 selects LSB first data transmission. DORD = 0 selects MSB first data transmission.
STR	Master/Slave Select. MSTR = 1 selects Master SPI mode. MSTR = 0 selects Slave SPI mode.
POL	Clock Polarity. When CPOL = 1, SCK is high when idle. When CPOL = 0, SCK of the master device is low when not transmitting. Please refer to figure on SPI Clock Phase and Polarity Control.
PHA	Clock Phase. The CPHA bit together with the CPOL bit controls the clock and data relationship between master and slave. Please refer to figure on SPI Clock Phase and Polarity Control.
PR0 PR1	SPI Clock Rate Select. These two bits control the SCK rate of the device configured as master. SPR1 and SPR0 have no effect on the slave. The relationship between SCK and the oscillator frequency, F_{osc}, is as follows: SPR1 SPR0 SCK = F_{osc} divided by 0 0 4 0 1 16 1 0 64 1 1 128

ble 5. SPSR – SPI Status Register

PSR Address = AAH — Reset Value = 00XX XXXXB

Bit	SPIF	WCOL	–	–	–	–	–	–
	7	6	5	4	3	2	1	0

ymbol	Function
PIF	SPI Interrupt Flag. When a serial transfer is complete, the SPIF bit is set and an interrupt is generated if SPIE = 1 and ES = 1. The SPIF bit is cleared by reading the SPI status register with SPIF and WCOL bits set, and then accessing the SPI data register.
COL	Write Collision Flag. The WCOL bit is set if the SPI data register is written during a data transfer. During data transfer, the result of reading the SPDR register may be incorrect, and writing to it has no effect. The WCOL bit (and the SPIF bit) are cleared by reading the SPI status register with SPIF and WCOL set, and then accessing the SPI data register.

le 6. SPDR – SPI Data Register

DR Address = 86H — Reset Value = unchanged

it	SPD7	SPD6	SPD5	SPD4	SPD3	SPD2	SPD1	SPD0
	7	6	5	4	3	2	1	0

ata Memory – EEPROM and RAM

ie AT89S8252 implements 2K bytes of on-chip EEPROM r data storage and 256 bytes of RAM. The upper 128 tes of RAM occupy a parallel space to the Special Func- in Registers. That means the upper 128 bytes have the me addresses as the SFR space but are physically sepa- le from SFR space.

hen an instruction accesses an internal location above ldress 7FH, the address mode used in the instruction ecifies whether the CPU accesses the upper 128 bytes RAM or the SFR space. Instructions that use direct dressing access SFR space.

r example, the following direct addressing instruction cesses the SFR at location 0A0H (which is P2).

```
MOV 0A0H, #data
```

tructions that use indirect addressing access the upper 8 bytes of RAM. For example, the following indirect dressing instruction, where R0 contains 0A0H, accesses data byte at address 0A0H, rather than P2 (whose dress is 0A0H).

```
MOV @R0, #data
```

te that stack operations are examples of indirect dressing, so the upper 128 bytes of data RAM are avail- e as stack space.

e on-chip EEPROM data memory is selected by setting EEMEN bit in the WMCON register at SFR address ation 96H. The EEPROM address range is from 000H to FH. The MOVX instructions are used to access the PROM. To access off-chip data memory with the MOVX ructions, the EEMEN bit needs to be set to "0".

e EEMWE bit in the WMCON register needs to be set to before any byte location in the EEPROM can be written. er software should reset EEMWE bit to "0" if no further PROM write is required. EEPROM write cycles in the ial programming mode are self-timed and typically take ms. The progress of EEPROM write can be monitored reading the RDY/$\overline{BSY}$ bit (read-only) in SFR WMCON. Y/$\overline{BSY}$ = 0 means programming is still in progress and Y/$\overline{BSY}$ = 1 means EEPROM write cycle is completed another write cycle can be initiated.

ddition, during EEPROM programming, an attempted d from the EEPROM will fetch the byte being written the MSB complemented. Once the write cycle is com- ed, true data are valid at all bit locations.

ogrammable Watchdog Timer

programmable Watchdog Timer (WDT) operates from ndependent oscillator. The prescaler bits, PS0, PS1 PS2 in SFR WMCON are used to set the period of the chdog Timer from 16 ms to 2048 ms. The available r periods are shown in the following table and the actual timer periods (at V_{CC} = 5V) are within ±30% of the nominal.

The WDT is disabled by Power-on Reset and during Power-down. It is enabled by setting the WDTEN bit in SFR WMCON (address = 96H). The WDT is reset by setting the WDTRST bit in WMCON. When the WDT times out without being reset or disabled, an internal RST pulse is generated to reset the CPU.

Table 7. Watchdog Timer Period Selection

WDT Prescaler Bits			Period (nominal)
PS2	PS1	PS0	
0	0	0	16 ms
0	0	1	32 ms
0	1	0	64 ms
0	1	1	128 ms
1	0	0	256 ms
1	0	1	512 ms
1	1	0	1024 ms
1	1	1	2048 ms

Timer 0 and 1

Timer 0 and Timer 1 in the AT89S8252 operate the same way as Timer 0 and Timer 1 in the AT89C51, AT89C52 and AT89C55. For further information, see the October 1995 Microcontroller Data Book, page 2-45, section titled, "Timer/Counters."

Timer 2

Timer 2 is a 16 bit Timer/Counter that can operate as either a timer or an event counter. The type of operation is selected by bit C/$\overline{T2}$ in the SFR T2CON (shown in Table 2). Timer 2 has three operating modes: capture, auto-reload (up or down counting), and baud rate generator. The modes are selected by bits in T2CON, as shown in Table 8.

Timer 2 consists of two 8-bit registers, TH2 and TL2. In the Timer function, the TL2 register is incremented every machine cycle. Since a machine cycle consists of 12 oscillator periods, the count rate is 1/12 of the oscillator frequency.

In the Counter function, the register is incremented in response to a 1-to-0 transition at its corresponding external input pin, T2. In this function, the external input is sampled during S5P2 of every machine cycle. When the samples show a high in one cycle and a low in the next cycle, the count is incremented. The new count value appears in the register during S3P1 of the cycle following the one in which

e transition was detected. Since two machine cycles (24 cillator periods) are required to recognize a 1-to-0 transi-n, the maximum count rate is 1/24 of the oscillator equency. To ensure that a given level is sampled at least ice before it changes, the level should be held for at least e full machine cycle.

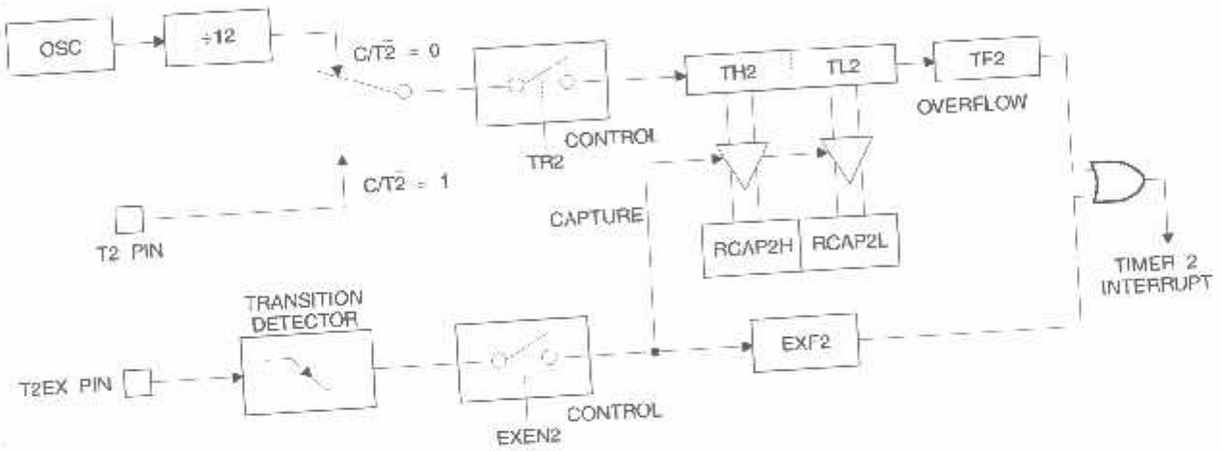
ble 8. Timer 2 Operating Modes

RCLK + TCLK	CP/$\overline{RL2}$	TR2	MODE
0	0	1	16-bit Auto-reload
0	1	1	16-bit Capture
1	X	1	Baud Rate Generator
X	X	0	(Off)

Capture Mode

In the capture mode, two options are selected by bit EXEN2 in T2CON. If EXEN2 = 0, Timer 2 is a 16 bit timer or counter which upon overflow sets bit TF2 in T2CON. This bit can then be used to generate an interrupt. If EXEN2 = 1, Timer 2 performs the same operation, but a l-to-0 transition at external input T2EX also causes the current value in TH2 and TL2 to be captured into RCAP2H and RCAP2L, respectively. In addition, the transition at T2EX causes bit EXF2 in T2CON to be set. The EXF2 bit, like TF2, can generate an interrupt. The capture mode is illustrated in Figure 1.

ıure 1. Timer 2 in Capture Mode



uto-reload (Up or Down Counter)

ner 2 can be programmed to count up or down when nfigured in its 16 bit auto-reload mode. This feature is voked by the DCEN (Down Counter Enable) bit located in e SFR T2MOD (see Table 9). Upon reset, the DCEN bit set to 0 so that timer 2 will default to count up. When CEN is set, Timer 2 can count up or down, depending on e value of the T2EX pin.

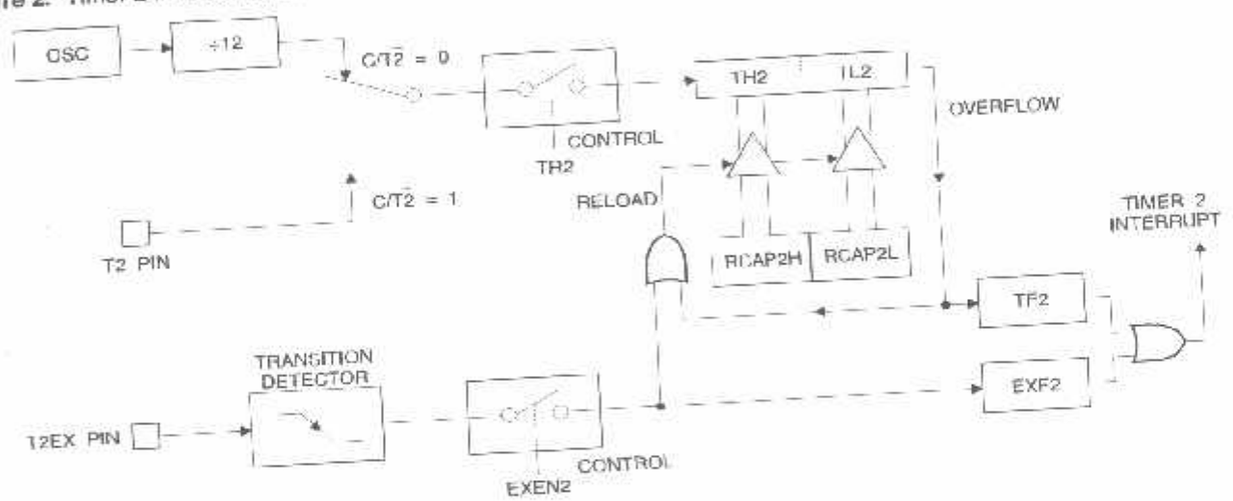
gure 2 shows Timer 2 automatically counting up when CEN = 0. In this mode, two options are selected by bit EN2 in T2CON. If EXEN2 = 0, Timer 2 counts up to FFFH and then sets the TF2 bit upon overflow. The erflow also causes the timer registers to be reloaded with e 16 bit value in RCAP2H and RCAP2L. The values in CAP2H and RCAP2L are preset by software. If EXEN2 = a 16 bit reload can be triggered either by an overflow or by a 1-to-0 transition at external input T2EX. This transition also sets the EXF2 bit. Both the TF2 and EXF2 bits can generate an interrupt if enabled.

Setting the DCEN bit enables Timer 2 to count up or down, as shown in Figure 3. In this mode, the T2EX pin controls the direction of the count. A logic 1 at T2EX makes Timer 2 count up. The timer will overflow at 0FFFFH and set the TF2 bit. This overflow also causes the 16 bit value in RCAP2H and RCAP2L to be reloaded into the timer registers, TH2 and TL2, respectively.

A logic 0 at T2EX makes Timer 2 count down. The timer underflows when TH2 and TL2 equal the values stored in RCAP2H and RCAP2L. The underflow sets the TF2 bit and causes 0FFFFH to be reloaded into the timer registers.

The EXF2 bit toggles whenever Timer 2 overflows or underflows and can be used as a 17th bit of resolution. In this operating mode, EXF2 does not flag an interrupt.

ure 2. Timer 2 in Auto Reload Mode (DCEN = 0)



le 9. T2MOD – Timer 2 Mode Control Register

Reset Value = XXXX XX00B

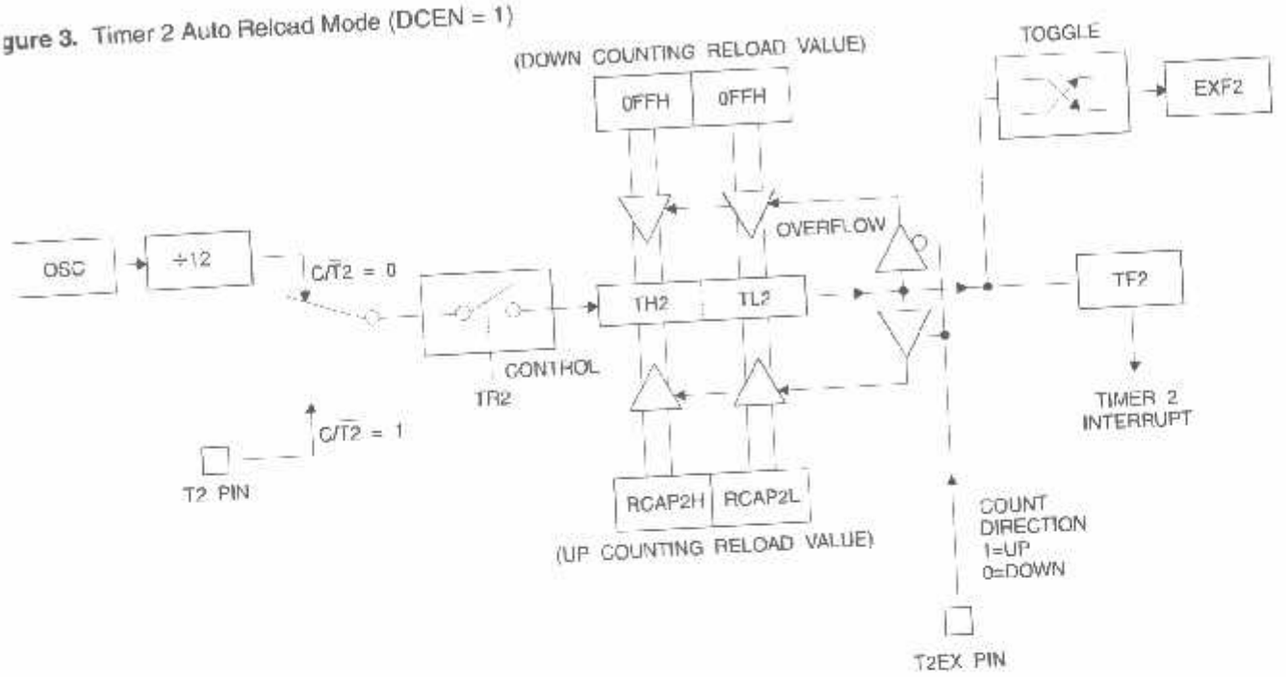
MOD Address = 0C9H

t Bit Addressable

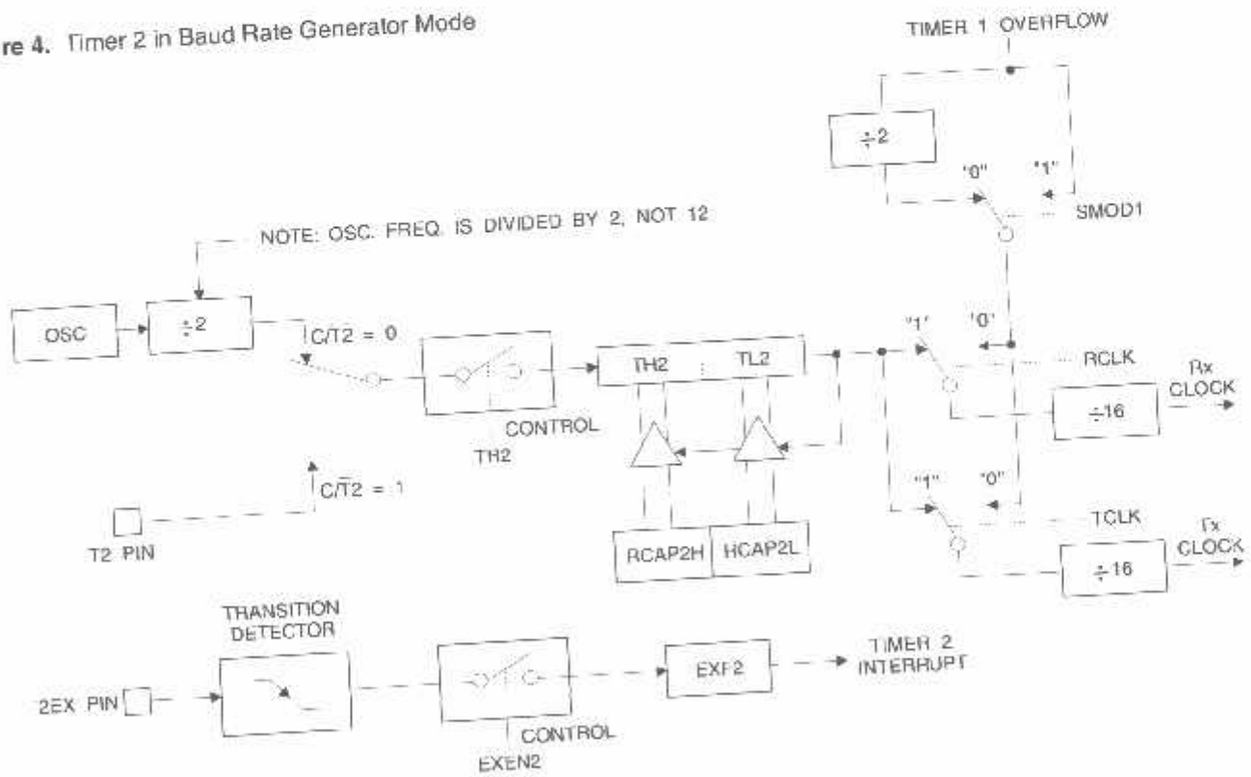
–	–	–	–	–	–	T2OE	DCEN
it 7	6	5	4	3	2	1	0

nbol	Function
	Not implemented, reserved for future use.
)E	Timer 2 Output Enable bit.
EN	When set, this bit allows Timer 2 to be configured as an up/down counter.

gure 3. Timer 2 Auto Reload Mode (DCEN = 1)



ure 4. Timer 2 in Baud Rate Generator Mode



aud Rate Generator

mer 2 is selected as the baud rate generator by setting CLK and/or RCLK in T2CON (Table 2). Note that the aud rates for transmit and receive can be different if Timer is used for the receiver or transmitter and Timer 1 is used r the other function. Setting RCLK and/or TCLK puts mer 2 into its baud rate generator mode, as shown in Fig- e 4.

ie baud rate generator mode is similar to the auto-reload ode, in that a rollover in TH2 causes the Timer 2 registers be reloaded with the 16 bit value in registers RCAP2H d RCAP2L, which are preset by software.

ie baud rates in Modes 1 and 3 are determined by Timer ; overflow rate according to the following equation.

$$\text{Modes 1 and 3 Baud Rates} = \frac{\text{Timer 2 Overflow Rate}}{16}$$

e Timer can be configured for either timer or counter eration. In most applications, it is configured for timer eration ($C/\overline{T2} = 0$). The timer operation is different for ner 2 when it is used as a baud rate generator. Normally, a timer, it increments every machine cycle (at 1/12 the illator frequency). As a baud rate generator, however, it rements every state time (at 1/2 the oscillator fre- ency). The baud rate formula is given below.

$$\frac{\text{Modes 1 and 3}}{\text{Baud Rate}} = \frac{\text{Oscillator Frequency}}{32 \times [65536 - (\overline{\text{RCAP2H,RCAP2L}})]}$$

ere (RCAP2H, RCAP2L) is the content of RCAP2H and AP2L taken as a 16 bit unsigned integer.

ner 2 as a baud rate generator is shown in Figure 4. This ire is valid only if RCLK or TCLK = 1 in T2CON. Note t a rollover in TH2 does not set TF2 and will not gener- an interrupt. Note too, that if EXEN2 is set, a 1-to-0 nsition in T2EX will set EXF2 but will not cause a reload n (RCAP2H, RCAP2L) to (TH2, TL2). Thus when Timer 2 is in use as a baud rate generator, T2EX can be used as an extra external interrupt.

Note that when Timer 2 is running (TR2 = 1) as a timer in the baud rate generator mode, TH2 or TL2 should not be read from or written to. Under these conditions, the Timer is incremented every state time, and the results of a read or write may not be accurate. The RCAP2 registers may be read but should not be written to, because a write might overlap a reload and cause write and/or reload errors. The timer should be turned off (clear TR2) before accessing the Timer 2 or RCAP2 registers.

Programmable Clock Out

A 50% duty cycle clock can be programmed to come out on P1.0, as shown in Figure 5. This pin, besides being a regular I/O pin, has two alternate functions. It can be programmed to input the external clock for Timer/Counter 2 or to output a 50% duty cycle clock ranging from 61 Hz to 4 MHz at a 16 MHz operating frequency.

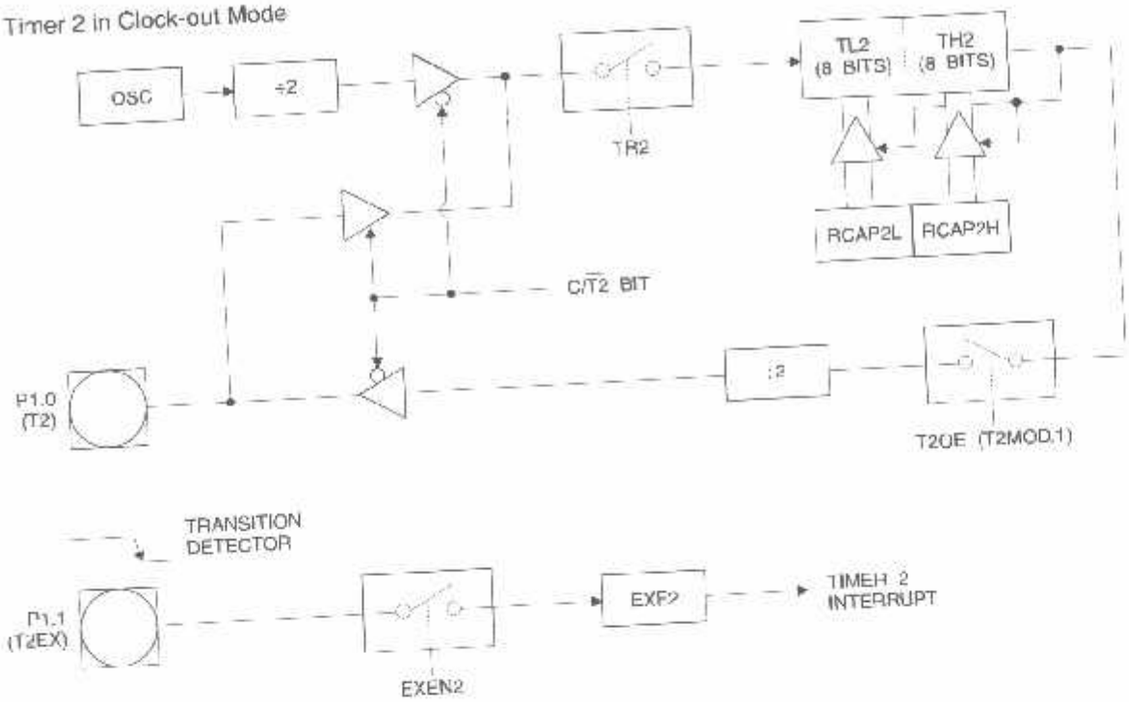
To configure the Timer/Counter 2 as a clock generator, bit $C/\overline{T2}$ (T2CON.1) must be cleared and bit T2OE (T2MOD.1) must be set. Bit TR2 (T2CON.2) starts and stops the timer.

The clock-out frequency depends on the oscillator frequency and the reload value of Timer 2 capture registers (RCAP2H, RCAP2L), as shown in the following equation.

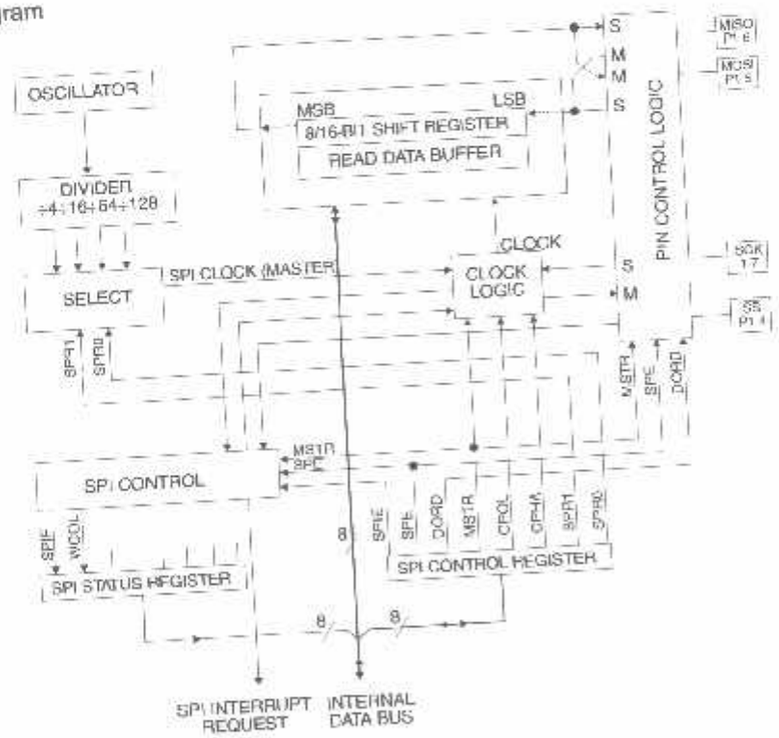
$$\text{Clock Out Frequency} = \frac{\text{Oscillator Frequency}}{4 \times [65536 - (\overline{\text{RCAP2H,RCAP2L}})]}$$

In the clock-out mode, Timer 2 rollovers will not generate an interrupt. This behavior is similar to when Timer 2 is used as a baud-rate generator. It is possible to use Timer 2 as a baud-rate generator and a clock generator simultaneously. Note, however, that the baud-rate and clock-out frequencies cannot be determined independently from one another since they both use RCAP2H and RCAP2L.

gure 5. Timer 2 in Clock-out Mode



ure 6. SPI Block Diagram



ART

e UART in the AT89S8252 operates the same way as
e UART in the AT89C51, AT89C52 and AT89C55. For
ther information, see the October 1995 Microcontroller
ata Book, page 2-49, section titled, "Serial Interface."

erial Peripheral Interface

e serial peripheral interface (SPI) allows high-speed syn-
ronous data transfer between the AT89S8252 and
ripheral devices or between several AT89S8252
vices. The AT89S8252 SPI features include the
lowing:

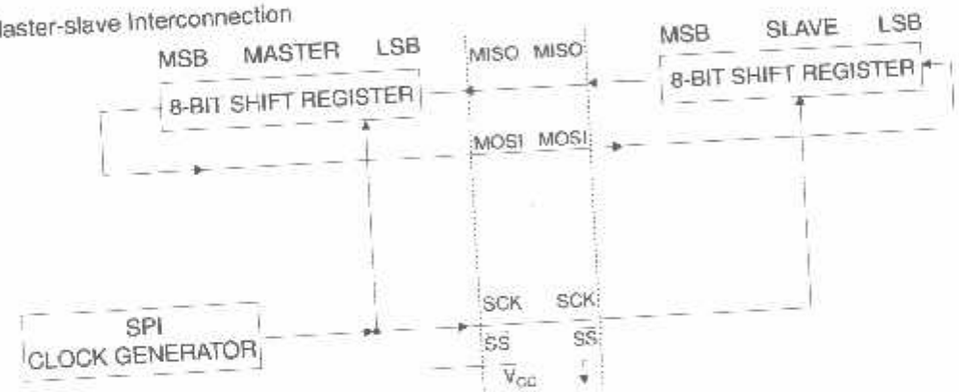
Full-Duplex, 3-Wire Synchronous Data Transfer
Master or Slave Operation
1.5 MHz Bit Frequency (max.)
LSB First or MSB First Data Transfer
Four Programmable Bit Rates
End of Transmission Interrupt Flag
- Write Collision Flag Protection
- Wakeup from Idle Mode (Slave Mode Only)

The interconnection between master and slave CPUs with SPI is shown in the following figure. The SCK pin is the clock output in the master mode but is the clock input in the slave mode. Writing to the SPI data register of the master CPU starts the SPI clock generator, and the data written shifts out of the MOSI pin and into the MOSI pin of the slave CPU. After shifting one byte, the SPI clock generator stops, setting the end of transmission flag (SPIF). If both the SPI interrupt enable bit (SPIE) and the serial port interrupt enable bit (ES) are set, an interrupt is requested.

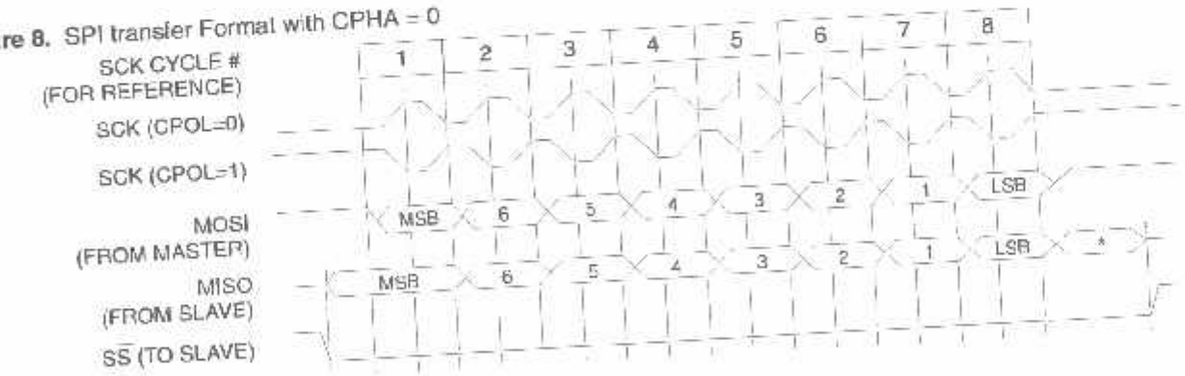
The Slave Select input, $\overline{SS}$/P1.4, is set low to select an individual SPI device as a slave. When $\overline{SS}$/P1.4 is set high, the SPI port is deactivated and the MOSI/P1.5 pin can be used as an input.

There are four combinations of SCK phase and polarity with respect to serial data, which are determined by control bits CPHA and CPOL. The SPI data transfer formats are shown in Figure 8 and Figure 9.

ure 7. SPI Master-slave Interconnection

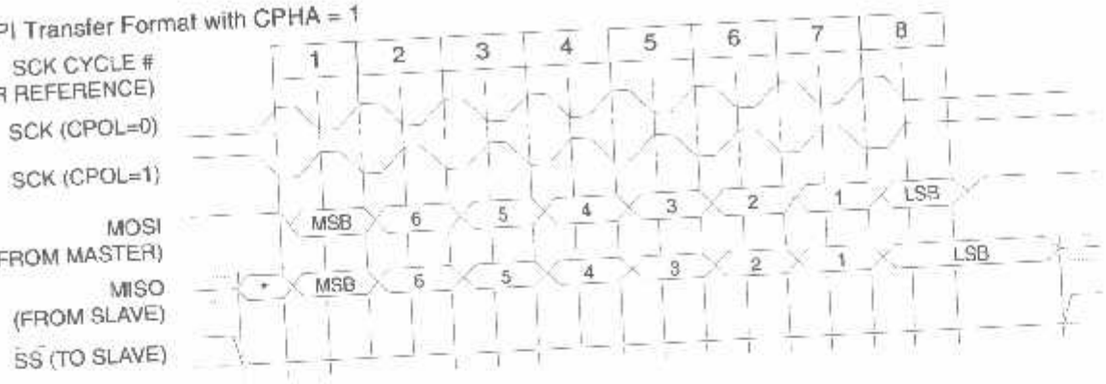


ure 8. SPI transfer Format with CPHA = 0



defined but normally MSB of character just received

igure 9. SPI Transfer Format with CPHA = 1



ot defined but normally LSB of previously transmitted character

terrupts

e AT89S8252 has a total of six interrupt vectors: two ternal nterrupts ($\overline{INT0}$ and $\overline{INT1}$), three timer interrupts imers 0, 1, and 2), and the serial port interrupt. These errupts are all shown in Figure 10.

ch of these interrupt sources can be individually enabled disabled by setting or clearing a bit in Special Function gister IE. IE also contains a global disable bit, EA, which ables all interrupts at once.

te that Table 10 shows that bit position IE.6 is unimple- nted. In the AT89C51, bit position IE.5 is also implemented. User software should not write 1s to these positions, since they may be used in future AT89 oducts.

ner 2 interrupt is generated by the logical OR of bits TF2 d EXF2 in register T2CON. Neither of these flags is ared by hardware when the service routine is vectored In fact, the service routine may have to determine ether it was TF2 or EXF2 that generated the interrupt, d that bit will have to be cleared in software.

e Timer 0 and Timer 1 flags, TF0 and TF1, are set at P2 of the cycle in which the timers overflow. The values then polled by the circuitry in the next cycle. However, Timer 2 flag, TF2, is set at S2P2 and is polled in the ne cycle in which the timer overflows.

Table 10. Interrupt Enable (IE) Register

(MSB)(LSB)

EA	–	ET2	ES	ET1	EX1	ET0	EX0

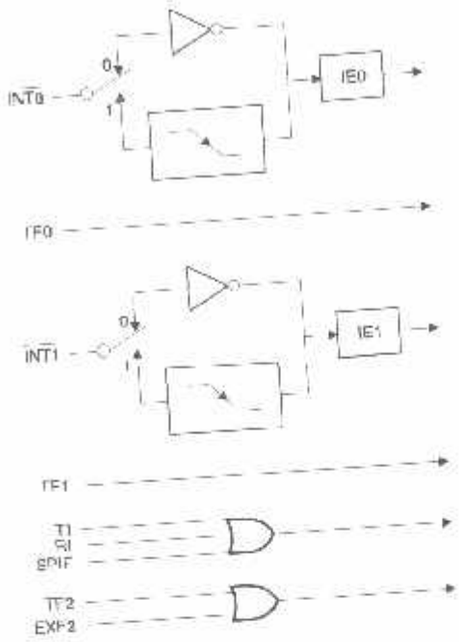
Enable Bit = 1 enables the interrupt.

Enable Bit = 0 disables the interrupt.

Symbol	Position	Function
EA	IE.7	Disables all interrupts. If EA = 0, no interrupt is acknowledged. If EA = 1, each interrupt source is individually enabled or disabled by setting or clearing its enable bit.
–	IE.6	Reserved.
ET2	IE.5	Timer 2 interrupt enable bit.
ES	IE.4	SPI and UART interrupt enable bit.
ET1	IE.3	Timer 1 interrupt enable bit.
EX1	IE.2	External interrupt 1 enable bit.
ET0	IE.1	Timer 0 interrupt enable bit.
EX0	IE.0	External interrupt 0 enable bit.

User software should never write 1s to unimplemented bits, because they may be used in future AT89 products.

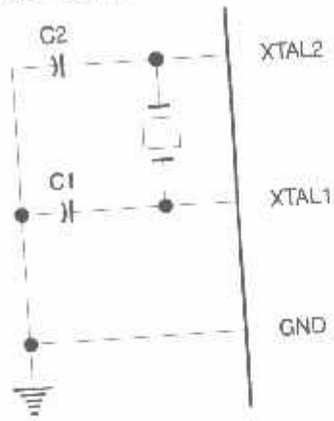
gure 10. Interrupt Sources



scillator Characteristics

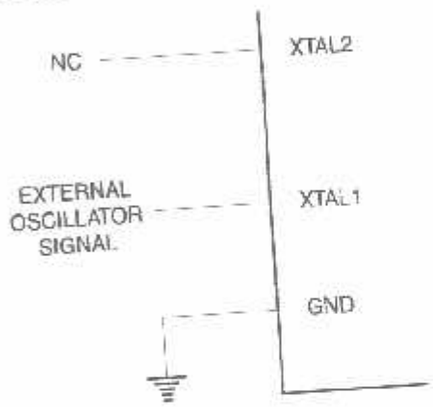
AL1 and XTAL2 are the input and output, respectively, an inverting amplifier that can be configured for use as on-chip oscillator, as shown in Figure 11. Either a quartz stal or ceramic resonator may be used. To drive the rice from an external clock source, XTAL2 should be left connected while XTAL1 is driven, as shown in Figure 12. ere are no requirements on the duty cycle of the external ck signal, since the input to the internal clocking circuitry hrough a divide-by-two flip-flop, but minimum and maxi- m voltage high and low time specifications must be served.

Figure 11. Oscillator Connections



Note: Note: C1, C2 = 30 pF ± 10 pF for Crystals
= 40 pF ± 10 pF for Ceramic Resonators

Figure 12. External Clock Drive Configuration



Idle Mode

In idle mode, the CPU puts itself to sleep while all the on-chip peripherals remain active. The mode is invoked by software. The content of the on-chip RAM and all the special functions registers remain unchanged during this mode. The idle mode can be terminated by any enabled interrupt or by a hardware reset.

It should be noted that when idle mode is terminated by a hardware reset, the device normally resumes program execution from where it left off, up to two machine cycles before the internal reset algorithm takes control. On-chip hardware inhibits access to internal RAM in this event, but access to the port pins is not inhibited. To eliminate the possibility of an unexpected write to a port pin when idle mode is terminated by a reset, the instruction following the one that invokes idle mode should not write to a port pin or to external memory.

Status of External Pins During Idle and Power-down Modes

Mode	Program Memory	ALE	$\overline{PSEN}$	PORT0	PORT1	PORT2	PORT3
Idle	Internal	1	1	Data	Data	Data	Data
Idle	External	1	1	Float	Data	Address	Data
Power-down	Internal	0	0	Data	Data	Data	Data
Power-down	External	0	0	Float	Data	Data	Data

Power-down Mode

In the power-down mode, the oscillator is stopped and the instruction that invokes power-down is the last instruction executed. The on-chip RAM and Special Function Registers retain their values until the power-down mode is terminated. Exit from power-down can be initiated either by hardware reset or by an enabled external interrupt. Reset redefines the SFRs but does not change the on-chip RAM. The reset should not be activated before V_{CC} is restored to its normal operating level and must be held active long enough to allow the oscillator to restart and stabilize.

To exit power-down via an interrupt, the external interrupt must be enabled as level sensitive before entering power-down. The interrupt service routine starts at 16 ms (nominal) after the enabled interrupt pin is activated.

Program Memory Lock Bits

The AT89S8252 has three lock bits that can be left unprogrammed (U) or can be programmed (P) to obtain the additional features listed in the following table.

When lock bit 1 is programmed, the logic level at the $\overline{EA}$ pin is sampled and latched during reset. If the device is powered up without a reset, the latch initializes to a random value and holds that value until reset is activated. The latched value of $\overline{EA}$ must agree with the current logic level at that pin in order for the device to function properly.

Once programmed, the lock bits can only be unprogrammed with the Chip Erase operations in either the parallel or serial modes.

Lock Bit Protection Modes[1][2]

Program Lock Bits				
	LB1	LB2	LB3	Protection Type
1	U	U	U	No internal memory lock feature.
2	P	U	U	MOVC instructions executed from external program memory are disabled from fetching code bytes from internal memory. $\overline{EA}$ is sampled and latched on reset and further programming of the Flash memory (parallel or serial mode) is disabled.
3	P	P	U	Same as Mode 2, but parallel or serial verify are also disabled.
4	P	P	P	Same as Mode 3, but external execution is also disabled.

Notes: 1. U = Unprogrammed
2. P = Programmed

rogramming the Flash and EEPROM

mel's AT89S8252 Flash Microcontroller offers 8K bytes in-system reprogrammable Flash Code memory and 2K tes of EEPROM Data memory.

ıe AT89S8252 is normally shipped with the on-chip Flash ode and EEPROM Data memory arrays in the erased ate (i.e. contents = FFH) and ready to be programmed. his device supports a High-voltage (12V) Parallel pro-ramming mode and a Low-voltage (5V) Serial ogramming mode. The serial programming mode pro-ides a convenient way to download the AT89S8252 inside e user's system. The parallel programming mode is com-ıtible with conventional third party Flash or EPROM ogrammers.

ıe Code and Data memory arrays are mapped via sepa-te address spaces in the serial programming mode. In e parallel programming mode, the two arrays occupy one ntiguous address space: 0000H to 1FFFH for the Code ray and 2000H to 27FFH for the Data array.

ıe Code and Data memory arrays on the AT89S8252 are ogrammed byte-by-byte in either programming mode. An to-erase cycle is provided with the self-timed program-ng operation in the serial programming mode. There is need to perform the Chip Erase operation to reprogram y memory location in the serial programming mode less any of the lock bits have been programmed.

the parallel programming mode, there is no auto-erase cle. To reprogram any non-blank byte, the user needs to e the Chip Erase operation first to erase both arrays.

rallel Programming Algorithm: To program and verify e AT89S8252 in the parallel programming mode, the fol-ving sequence is recommended:

Power-up sequence:

Apply power between V_{CC} and GND pins.

Set RST pin to "H".

Apply a 3 MHz to 24 MHz clock to XTAL1 pin and wait for at least 10 milliseconds.

Set $\overline{PSEN}$ pin to "L"

ALE pin to "H"

$\overline{EA}$ pin to "H" and all other pins to "H".

Apply the appropriate combination of "H" or "L" logic levels to pins P2.6, P2.7, P3.6, P3.7 to select one of the programming operations shown in the Flash Programming Modes table.

Apply the desired byte address to pins P1.0 to P1.7 and P2.0 to P2.5.

Apply data to pins P0.0 to P0.7 for Write Code operation.

5. Raise $\overline{EA}/V_{pp}$ to 12V to enable Flash programming, erase or verification.
6. Pulse ALE/$\overline{PROG}$ once to program a byte in the Code memory array, the Data memory array or the lock bits. The byte-write cycle is self-timed and typically takes 1.5 ms.
7. To verify the byte just programmed, bring pin P2.7 to "L" and read the programmed data at pins P0.0 to P0.7.
8. Repeat steps 3 through 7 changing the address and data for the entire 2K or 8K bytes array or until the end of the object file is reached.
9. Power-off sequence:

   Set XTAL1 to "L".

   Set RST and $\overline{EA}$ pins to "L".

   Turn V_{CC} power off.

In the parallel programming mode, there is no auto-erase cycle and to reprogram any non-blank byte, the user needs to use the Chip Erase operation first to erase both arrays.

Data Polling: The AT89S8252 features $\overline{DATA}$ Polling to indicate the end of a write cycle. During a write cycle in the parallel or serial programming mode, an attempted read of the last byte written will result in the complement of the written datum on P0.7 (parallel mode), and on the MSB of the serial output byte on MISO (serial mode). Once the write cycle has been completed, true data are valid on all outputs, and the next cycle may begin. $\overline{DATA}$ Polling may begin any time after a write cycle has been initiated.

Ready/$\overline{Busy}$: The progress of byte programming in the parallel programming mode can also be monitored by the RDY/$\overline{BSY}$ output signal. Pin P3.4 is pulled Low after ALE goes High during programming to indicate $\overline{BUSY}$. P3.4 is pulled High again when programming is done to indicate READY.

Program Verify: If lock bits LB1 and LB2 have not been programmed, the programmed Code or Data byte can be read back via the address and data lines for verification. The state of the lock bits can also be verified directly in the parallel programming mode. In the serial programming mode, the state of the lock bits can only be verified indirectly by observing that the lock bit features are enabled.

Chip Erase: Both Flash and EEPROM arrays are erased electrically at the same time. In the parallel programming mode, chip erase is initiated by using the proper combination of control signals and by holding ALE/$\overline{PROG}$ low for 10 ms. The Code and Data arrays are written with all "1"s in the Chip Erase operation.

the serial programming mode, a chip erase operation is iated by issuing the Chip Erase instruction. In this mode, ip erase is self-timed and takes about 16 ms.

ring chip erase, a serial read from any address location l return 00H at the data outputs.

rial Programming Fuse: A programmable fuse is avail-le to disable Serial Programming if the user needs ximum system security. The Serial Programming Fuse n only be programmed or erased in the Parallel Program-ng Mode.

e AT89S8252 is shipped with the Serial Programming de enabled.

ading the Signature Bytes: The signature bytes are d by the same procedure as a normal verification of ations 030H and 031H, except that P3.6 and P3.7 must pulled to a logic low. The values returned are as follows:

(030H) = 1EH indicates manufactured by Atmel
(031H) = 72H indicates 89S8252

ogramming Interface

ry code byte in the Flash and EEPROM arrays can be ten, and the entire array can be erased, by using the ropriate combination of control signals. The write oper-on cycle is self-timed and once initiated, will omatically time itself to completion.

najor programming vendors offer worldwide support for Atmel microcontroller series. Please contact your local gramming vendor for the appropriate software revision.

rial Downloading

h the Code and Data memory arrays can be pro-mmed using the serial SPI bus while RST is pulled to The serial interface consists of pins SCK, MOSI (input) MISO (output). After RST is set high, the Programming ble instruction needs to be executed first before pro-n/erase operations can be executed.

uto-erase cycle is built into the self-timed programming ation (in the serial mode ONLY) and there is no need st execute the Chip Erase instruction unless any of the bits have been programmed. The Chip Erase opera-turns the content of every memory location in both the e and Data arrays into FFH.

Code and Data memory arrays have separate address es:

0000H to 1FFFH for Code memory and 000H to 7FFH for Data memory.

Either an external system clock is supplied at pin XTAL1 or a crystal needs to be connected across pins XTAL1 and XTAL2. The maximum serial clock (SCK) frequency should be less than 1/40 of the crystal frequency. With a 24 MHz oscillator clock, the maximum SCK frequency is 600 kHz.

Serial Programming Algorithm

To program and verify the AT89S8252 in the serial programming mode, the following sequence is recommended:

1. Power-up sequence:
   Apply power between VCC and GND pins.
   Set RST pin to "H".
   If a crystal is not connected across pins XTAL1 and XTAL2, apply a 3 MHz to 24 MHz clock to XTAL1 pin and wait for at least 10 milliseconds.
2. Enable serial programming by sending the Programming Enable serial instruction to pin MOSI/P1.5. The frequency of the shift clock supplied at pin SCK/P1.7 needs to be less than the CPU clock at XTAL1 divided by 40.
3. The Code or Data array is programmed one byte at a time by supplying the address and data together with the appropriate Write instruction. The selected memory location is first automatically erased before new data is written. The write cycle is self-timed and typically takes less than 2.5 ms at 5V.
4. Any memory location can be verified by using the Read instruction which returns the content at the selected address at serial output MISO/P1.6.
5. At the end of a programming session, RST can be set low to commence normal operation.

Power-off sequence (if needed):

Set XTAL1 to "L" (if a crystal is not used).

Set RST to "L".

Turn V_{CC} power off.

Serial Programming Instruction

The Instruction Set for Serial Programming follows a 3-byte protocol and is shown in the following table:

ıstruction Set

ıstruction	Input Format			Operation
	Byte 1	Byte 2	Byte 3	
rogramming Enable	1010 1100	0101 0011	xxxx xxxx	Enable serial programming interface after RST goes high.
hip Erase	1010 1100	xxxx x100	xxxx xxxx	Chip erase both 8K & 2K memory arrays.
lead Code Memory	aaaa a001	low addr	xxxx xxxx	Read data from Code memory array at the selected address. The 5 MSBs of the first byte are the high order address bits. The low order address bits are in the second byte. Data are available at pin MISO during the third byte.
Vrite Code Memory	aaaa a010	low addr	data in	Write data to Code memory location at selected address. The address bits are the 5 MSBs of the first byte together with the second byte.
ead Data Memory	00aa a101	low addr	xxxx xxxx	Read data from Data memory array at selected address. Data are available at pin MISO during the third byte.
rite Data Memory	00aa a110	low addr	data in	Write data to Data memory location at selected address.
rite Lock Bits	1010 1100	x x111	xxxx xxxx	Write lock bits. Set LB1, LB2 or LB3 = "0" to program lock bits.

e: 1. DATA polling is used to indicate the end of a write cycle which typically takes less than 2.5 ms at 5V.
2. "aaaaa" = high order address.
3. "x" = don't care.

lash and EEPROM Parallel Programming Modes

lode	RST	PSEN	ALE/PROG	EA/V_{PP}	P2.6	P2.7	P3.5	P3.7	Data I/O P0.7:0	Address P2.5:0 P1.7:0
erial Prog. Modes	H	h[1]	h[1]	X						
hip Erase	H	L	(2)	12V	H	L	L	L	X	X
/rite (10K bytes) Memory	H	L		12V	L	H	H	H	DIN	ADDR
ead (10K bytes) Memory	H	L	H	12V	L	L	H	H	DOUT	ADDR
/rite Lock Bits:	H	L		12V	H	L	H	L	DIN	X
Bit - 1									P0.7 = 0	X
Bit - 2									P0.6 = 0	X
Bit - 3									P0.5 = 0	X
ead Lock Bits:	H	L	H	12V	H	H	L	L	DOUT	X
Bit - 1									@P0.2	X
Bit - 2									@P0.1	X
Bit - 3									@P0.0	X
ead Atmel Code	H	L	H	12V	L	L	L	L	DOUT	30H
ead Device Code	H	L	H	12V	L	L	L	L	DOUT	31H
erial Prog. Enable	H	L	(2)	12V	L	H	L	H	P0.0 = 0	X
erial Prog. Disable	H	L	(2)	12V	L	H	L	H	P0.0 = 1	X
ead Serial Prog. Fuse	H	L	H	12V	H	H	L	H	@P0.0	X

es:
1. "h" = weakly pulled "High" internally.
2. Chip Erase and Serial Programming Fuse require a 10 ms $\overline{PROG}$ pulse. Chip Erase needs to be performed first before reprogramming any byte with a content other than FFH.
3. P3.4 is pulled Low during programming to indicate RDY/$\overline{BSY}$.
4. "X" = don't care

gure 13. Programming the Flash/EEPROM Memory

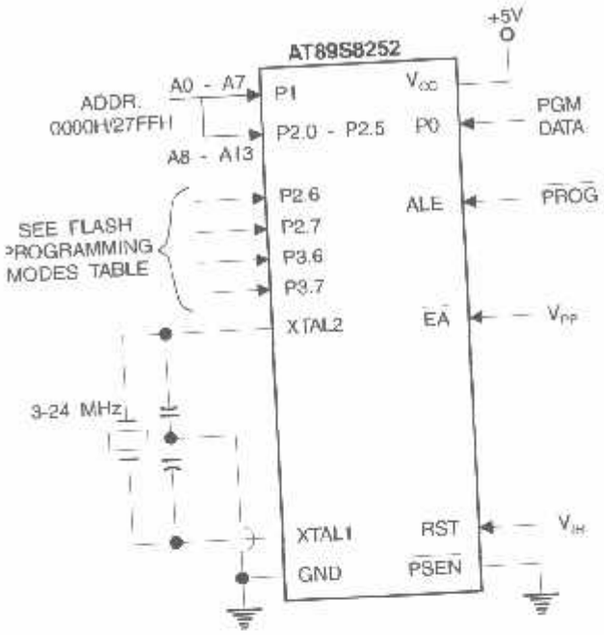
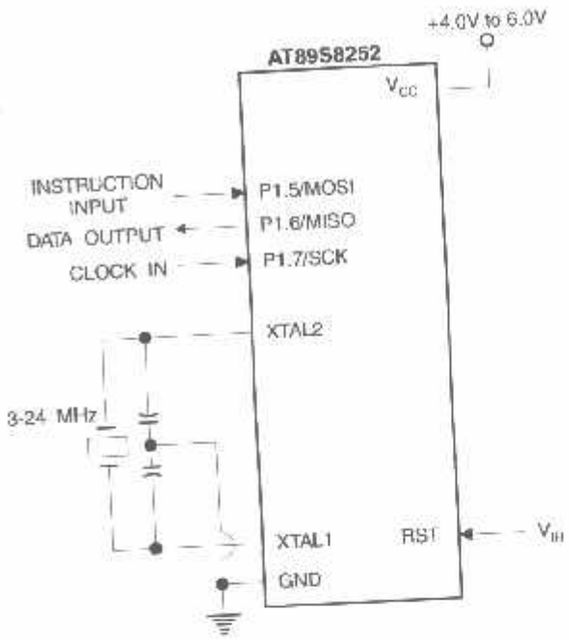
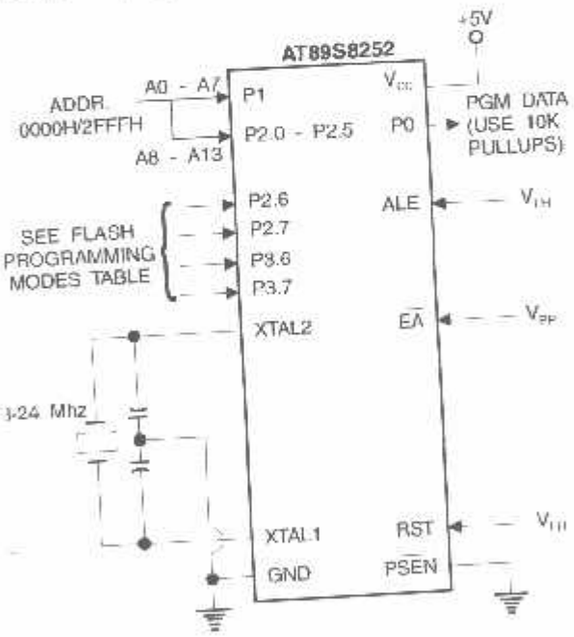


Figure 15. Flash/EEPROM Serial Downloading



ure 14. Verifying the Flash/EEPROM Memory

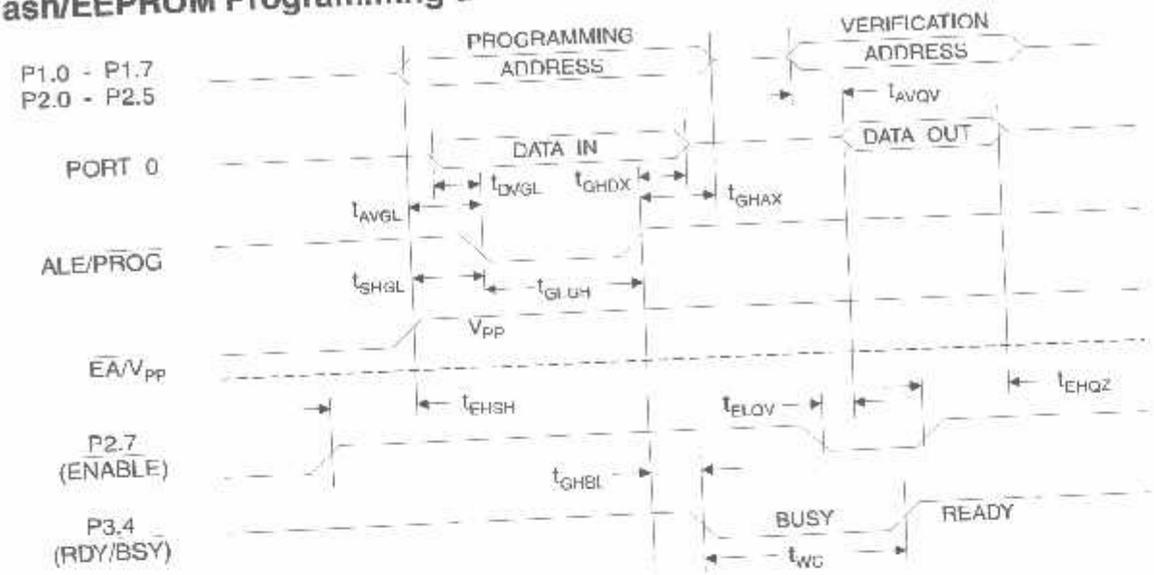


lash Programming and Verification Characteristics – Parallel Mode

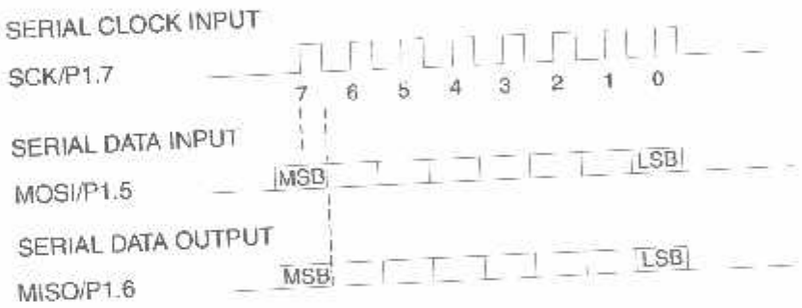
= 0°C to 70°C, V_{CC} = 5.0V ± 10%

ymbol	Parameter	Min	Max	Units
PP	Programming Enable Voltage	11.5	12.5	V
D	Programming Enable Current		1.0	mA
/CLCL	Oscillator Frequency	3	24	MHz
AVGL	Address Setup to $\overline{PROG}$ Low	$48t_{CLCL}$		
GHAX	Address Hold after $\overline{PROG}$	$48t_{CLCL}$		
DVGL	Data Setup to $\overline{PROG}$ Low	$48t_{CLCL}$		
GHDX	Data Hold after $\overline{PROG}$	$48t_{CLCL}$		
EHSH	P2.7 ($\overline{ENABLE}$) High to V_{PP}	10		µs
SHGL	V_{PP} Setup to $\overline{PROG}$ Low	1	110	µs
GLGH	$\overline{PROG}$ Width		$48t_{CLCL}$	
AVQV	Address to Data Valid		$48t_{CLCL}$	
ELQV	$\overline{ENABLE}$ Low to Data Valid	0	$48t_{CLCL}$	
EHQZ	Data Float after $\overline{ENABLE}$		1.0	µs
GHBL	$\overline{PROG}$ High to $\overline{BUSY}$ Low		2.0	ms
WC	Byte Write Cycle Time			

ash/EEPROM Programming and Verification Waveforms – Parallel Mode



rial Downloading Waveforms



bsolute Maximum Ratings*

)perating Temperature	-55°C to +125°C
itorage Temperature	-65°C to +150°C
/oltage on Any Pin ith Respect to Ground	-1.0V to +7.0V
Maximum Operating Voltage	6.6V
)C Output Current	15.0 mA

*NOTICE: Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

C Characteristics

e values shown in this table are valid for T_A = -40°C to 85°C and V_{CC} = 5.0V ± 20%, unless otherwise noted.

ymbol	Parameter	Condition	Min	Max	Units
IL	Input Low-voltage	(Except EA)	-0.5	0.2 V_{CC} - 0.1	V
IL1	Input Low-voltage (EA)		-0.5	0.2 V_{CC} - 0.3	V
IH	Input Hith-voltage	(Except XTAL1, RST)	0.2 V_{CC} + 0.9	V_{CC} + 0.5	V
IH1	Input Hith-voltage	(XTAL1, RST)	0.7 V_{CC}	V_{CC} + 0.5	V
OL	Output Low-voltage (1) (Ports 1,2,3)	I_{OL} = 1.6 mA		0.5	V
OL1	Output Low-voltage (1) (Port 0, ALE, PSEN)	I_{OL} = 3.2 mA		0.5	V
OH	Output Hith-voltage (Ports 1,2,3, ALE, PSEN)	I_{OH} = -60 µA, V_{CC} = 5V ± 10%	2.4		V
		I_{OH} = -25 µA	0.75 V_{CC}		V
		I_{OH} = -10 µA	0.9 V_{CC}		V
OH1	Output Hith-voltage (Port 0 in External Bus Mode)	I_{OH} = -800 µA, V_{CC} = 5V ± 10%	2.4		V
		I_{OH} = -300 µA	0.75 V_{CC}		V
		I_{OH} = -80 µA	0.9 V_{CC}		V
	Logical 0 Input Current (Ports 1,2,3)	V_{IN} = 0.45V		-50	µA
	Logical 1 to 0 Transition Current (Ports 1,2,3)	V_{IN} = 2V, V_{CC} = 5V ± 10%		-650	µA
	Input Leakage Current (Port 0, EA)	0.45 < V_{IN} < V_{CC}		±10	µA
RST	Reset Pull-down Resistor		50	300	KΩ
O	Pin Capacitance	Test Freq. = 1 MHz, T_A = 25°C		10	pF
	Power Supply Current	Active Mode, 12 MHz		25	mA
		Idle Mode, 12 MHz		6.5	mA
	Power-down Mode (2)	V_{CC} = 6V		100	µA
		V_{CC} = 3V		40	µA

s: 1. Under steady state (non-transient) conditions, I_{OL} must be externally limited as follows:
Maximum I_{OL} per port pin: 10 mA
Maximum I_{OL} per 8-bit port:
Port 0: 26 mA
Ports 1, 2, 3: 15 mA
Maximum total I_{OL} for all output pins: 71 mA
If I_{OL} exceeds the test condition, V_{OL} may exceed the related specification. Pins are not guaranteed to sink current greater than the listed test conditions.
2. Minimum V_{CC} for Power-down is 2V

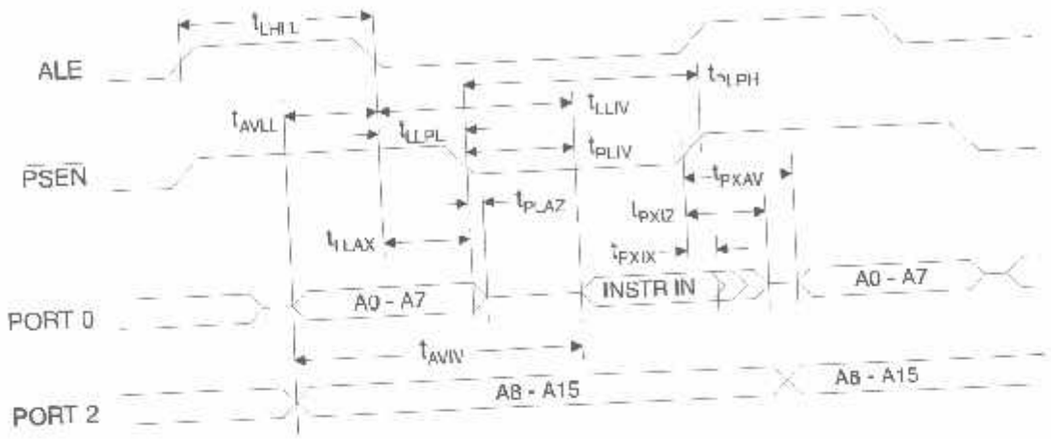
C Characteristics

ıder operating conditions, load capacitance for Port 0, ALE/$\overline{PROG}$, and $\overline{PSEN}$ = 100 pF; load capacitance for all other tputs = 80 pF.

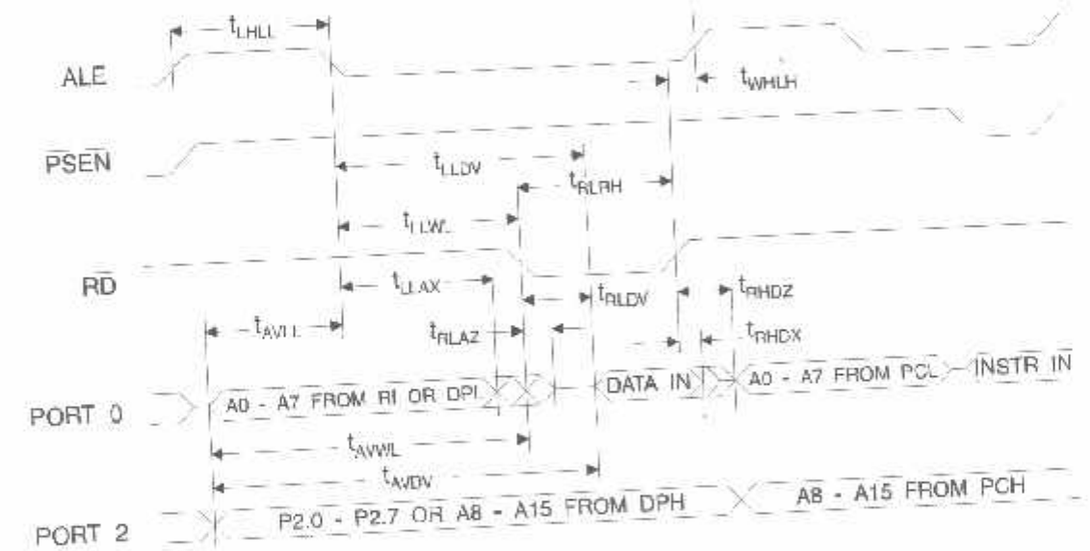
xternal Program and Data Memory Characteristics

ymbol	Parameter	Variable Oscillator		Units
		Min	Max	
/t_{CLCL}	Oscillator Frequency	0	24	MHz
t_{LHLL}	ALE Pulse Width	$2t_{CLCL}$ - 40		ns
t_{AVLL}	Address Valid to ALE Low	t_{CLCL} - 13		ns
t_{LLAX}	Address Hold after ALE Low	t_{CLCL} - 20		ns
t_{LLIV}	ALE Low to Valid Instruction In		$4t_{CLCL}$ - 65	ns
t_{LLPL}	ALE Low to $\overline{PSEN}$ Low	t_{CLCL} - 13		ns
t_{PLPH}	$\overline{PSEN}$ Pulse Width	$3t_{CLCL}$ - 20		ns
t_{PLIV}	$\overline{PSEN}$ Low to Valid Instruction In		$3t_{CLCL}$ - 45	ns
t_{PXIX}	Input Instruction Hold after $\overline{PSEN}$	0		ns
t_{PXIZ}	Input Instruction Float after $\overline{PSEN}$		t_{CLCL} - 10	ns
t_{AVIV}	$\overline{PSEN}$ to Address Valid	t_{CLCL} - 8		ns
t_{PLAZ}	Address to Valid Instruction In		$5t_{CLCL}$ - 55	ns
t_{RLRH}	$\overline{PSEN}$ Low to Address Float		10	ns
t_{WLWH}	$\overline{RD}$ Pulse Width	$6t_{CLCL}$ - 100		ns
t_{RLDV}	$\overline{WR}$ Pulse Width	$6t_{CLCL}$ - 100		ns
t_{RHDX}	$\overline{RD}$ Low to Valid Data In		$5t_{CLCL}$ - 90	ns
t_{RHDZ}	Data Hold after $\overline{RD}$	0		ns
t_{LLDV}	Data Float after $\overline{RD}$		$2t_{CLCL}$ - 28	ns
t_{AVDV}	ALE Low to Valid Data In		$8t_{CLCL}$ - 150	ns
t_{AVLL}	Address to Valid Data In		$9t_{CLCL}$ - 165	ns
t_{AVWL}	ALE Low to $\overline{RD}$ or $\overline{WR}$ Low	$3t_{CLCL}$ - 50	$3t_{CLCL}$ + 50	ns
t_{QVWX}	Address to $\overline{RD}$ or $\overline{WR}$ Low	$4t_{CLCL}$ - 75		ns
t_{WHQX}	Data Valid to $\overline{WR}$ Transition	t_{CLCL} - 20		ns
t_{RLAZ}	Data Valid to $\overline{WR}$ High	$7t_{CLCL}$ - 120		ns
t_{WHLH}	Data Hold after $\overline{WR}$	t_{CLCL} - 20		ns
	$\overline{RD}$ Low to Address Float		0	ns
	$\overline{RD}$ or $\overline{WR}$ High to ALE High	t_{CLCL} - 20	t_{CLCL} + 25	ns

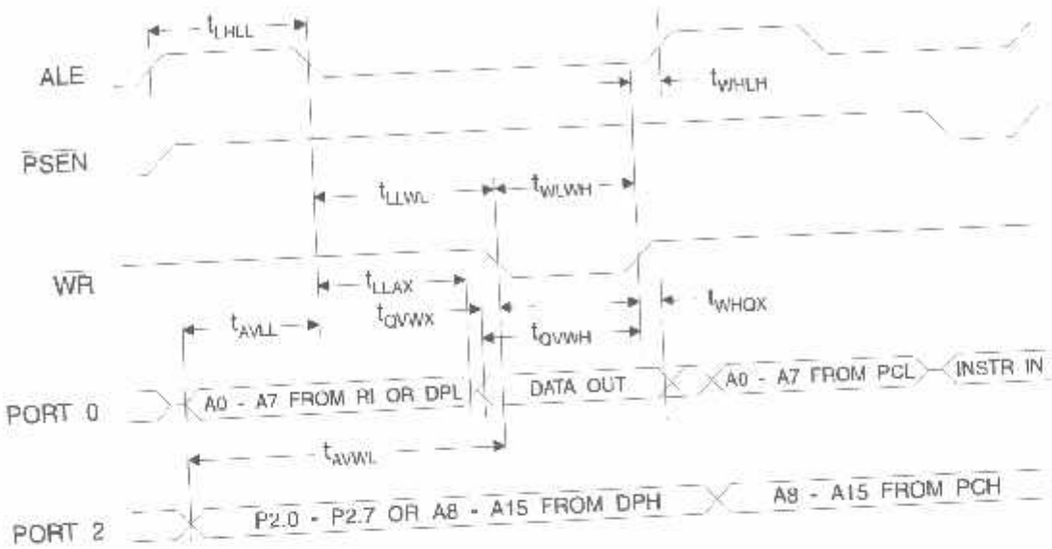
xternal Program Memory Read Cycle



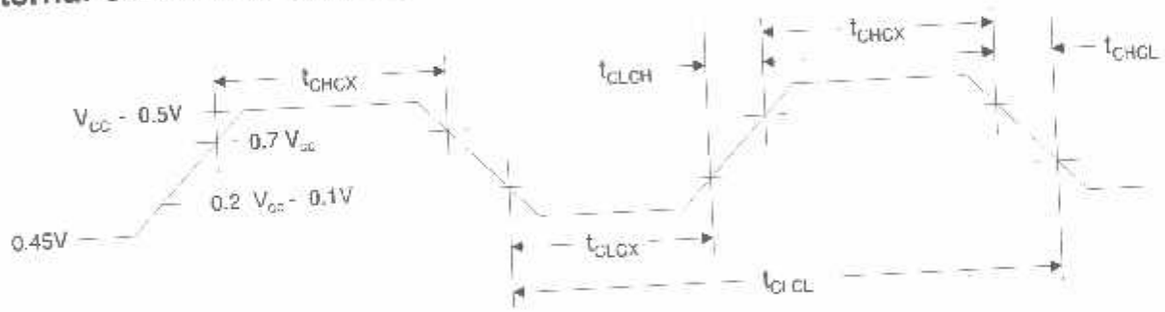
xternal Data Memory Read Cycle



External Data Memory Write Cycle



External Clock Drive Waveforms



External Clock Drive

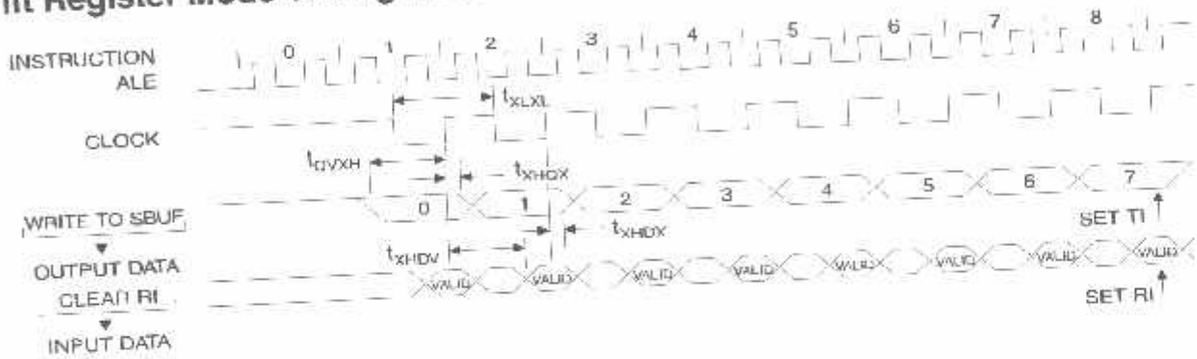
Symbol	Parameter	V_{CC} = 4.0V to 6.0V		Units
		Min	Max	
t_{CLCL}	Oscillator Frequency	0	24	MHz
t_{CLCL}	Clock Period	41.6		ns
t_{CHCX}	High Time	15		ns
t_{CLCX}	Low Time	15		ns
t_{CLCH}	Rise Time		20	ns
t_{CHCL}	Fall Time		20	ns

erial Port Timing: Shift Register Mode Test Conditions

e values in this table are valid for V_{CC} = 4.0V to 6V and Load Capacitance = 80 pF.

ymbol	Parameter	Variable Oscillator		Units
		Min	Max	
	Serial Port Clock Cycle Time	$12t_{CLCL}$		µs
CLXL	Output Data Setup to Clock Rising Edge	$10t_{CLCL}$ - 133		ns
QVXH	Output Data Hold after Clock Rising Edge	$2t_{CLCL}$ - 117		ns
XHQX	Input Data Hold after Clock Rising Edge	0		ns
XLDX	Clock Rising Edge to Input Data Valid		$10t_{CLCL}$ - 133	ns
XHDV				

ıift Register Mode Timing Waveforms



: Testing Input/Output Waveforms[1]

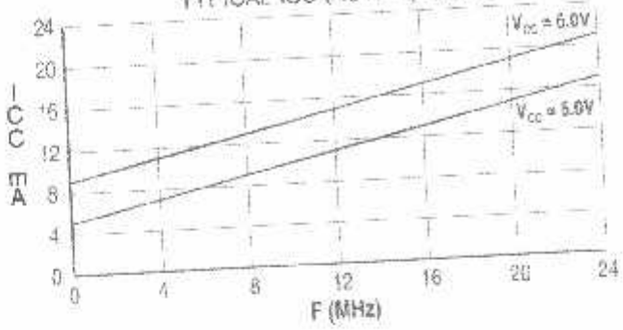
as: 1. AC Inputs during testing are driven at V_{CC} - 0.5V for a logic 1 and 0.45V for a logic 0. Timing measurements are made at V_{IH} min. for a logic 1 and V_{IL} max. for a logic 0.

Float Waveforms[1]

Notes: 1. For timing purposes, a port pin is no longer floating when a 100 mV change from load voltage occurs. A port pin begins to float when a 100 mV change from the loaded V_{OH}/V_{OL} level occurs.

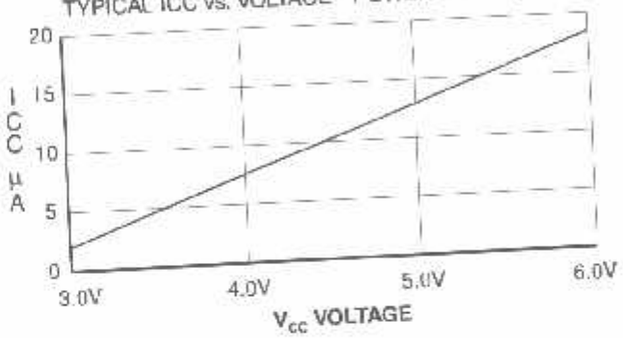
AT89S8252

TYPICAL ICC (ACTIVE) at 25°C



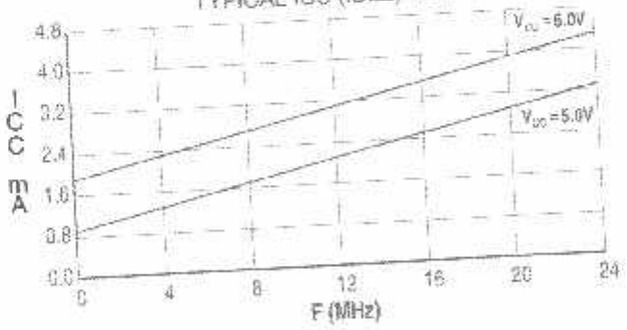
AT89S8252

TYPICAL ICC vs. VOLTAGE - POWER DOWN (85°C)



AT89S8252

TYPICAL ICC (IDLE) at 25°C



Notes: 1. XTAL1 tied to GND for Icc (power-down)
2. Lock bits programmed

rdering Information

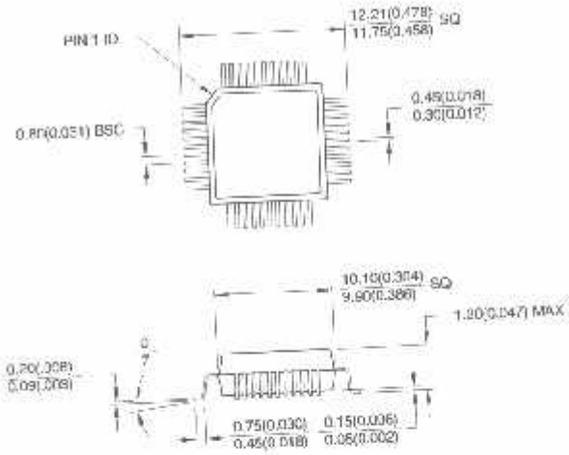
Speed (MHz)	Power Supply	Ordering Code	Package	Operation Range
24	4.0V to 6.0V	AT89S8252-24AC AT89S8252-24JC AT89S8252-24PC AT89S8252-24QC	44A 44J 40P6 44Q	Commercial (0°C to 70°C)
	4.0V to 6.0V	AT89S8252-24AI AT89S8252-24JI AT89S8252-24PI AT89S8252-24QI	44A 44J 40P6 44Q	Industrial (-40°C to 85°C)
33	4.5V to 5.5V	AT89S8252-33AC AT89S8252-33JC AT89S8252-33PC AT89S8252-33QC	44A 44J 40P6 44Q	Commercial (0°C to 70°C)

[ ] = Preliminary Information

	Package Type
1A	44-lead, Thin Plastic Gull Wing Quad Flatpack (TQFP)
1J	44-lead, Plastic J-leaded Chip Carrier (PLCC)
)P6	40-lead, 0.600" Wide, Plastic Dual Inline Package (PDIP)
1Q	44-lead, Plastic Gull Wing Quad Flatpack (PQFP)

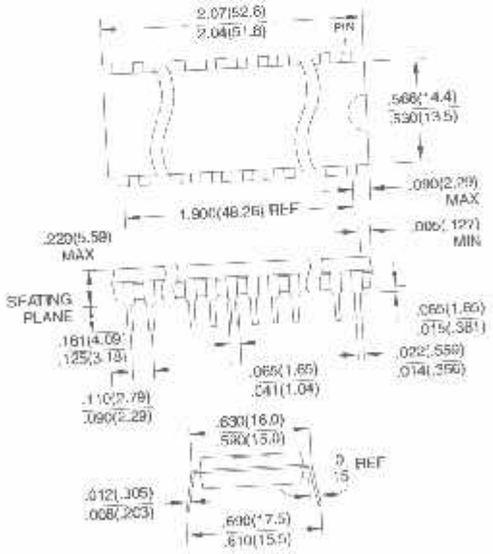
ackaging Information

44A, 44-lead, Thin (1.0 mm) Plastic Gull Wing Quad Flatpack (TQFP)
Dimensions in Millimeters and (Inches)*
JEDEC STANDARD MS-026 ACB

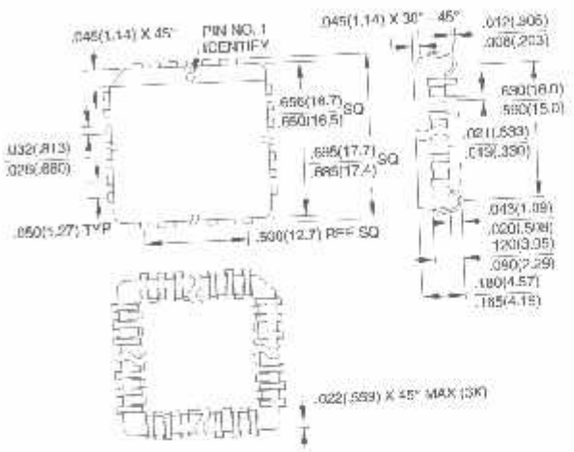


Controlling dimension: millimeters

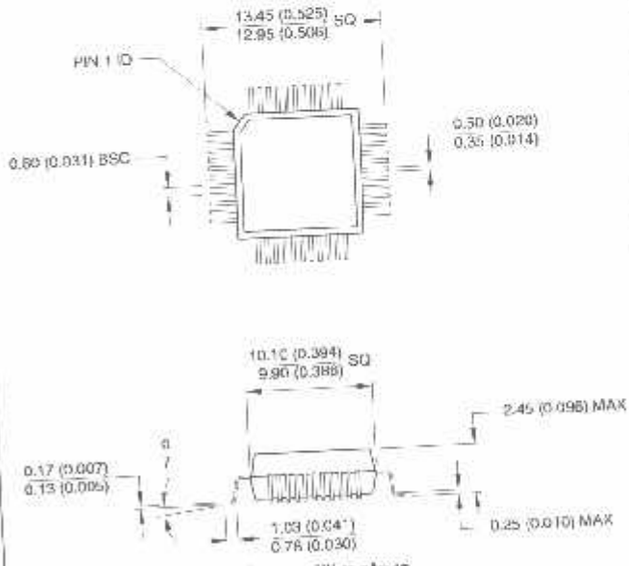
40P6, 40-lead, 0.600" Wide, Plastic Dual Inline Package (PDIP)
Dimensions in Inches and (Millimeters)



44J, 44-lead, Plastic J-leaded Chip Carrier (PLCC)
Dimensions in Inches and (Millimeters)
JEDEC STANDARD MS-018 AC



44Q, 44-lead, Plastic Quad Flat Package (PQFP)
Dimensions in Millimeters and (Inches)*
JEDEC STANDARD MS-022 AB



Controlling dimension: millimeters

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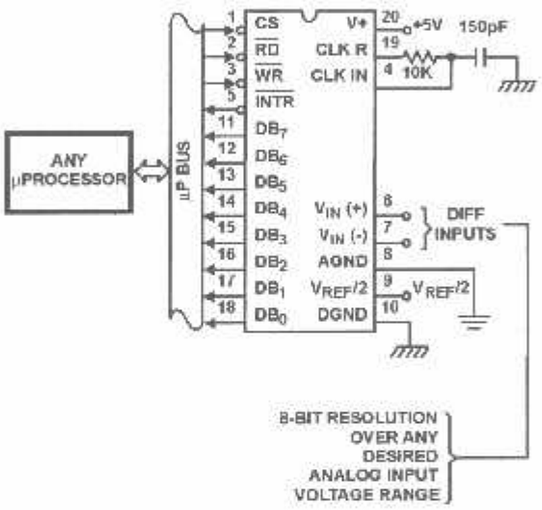
0401E-02/00/xM

8-Bit, Microprocessor-Compatible, A/D Converters

The ADC080X family are CMOS 8-Bit, successive-approximation A/D converters which use a modified potentiometric ladder and are designed to operate with the 8080A control bus via three-state outputs. These converters appear to the processor as memory locations or I/O ports, and hence no interfacing logic is required.

The differential analog voltage input has good common-mode-rejection and permits offsetting the analog zero-input-voltage value. In addition, the voltage reference input can be adjusted to allow encoding any smaller analog voltage span to the full 8 bits of resolution.

Typical Application Schematic

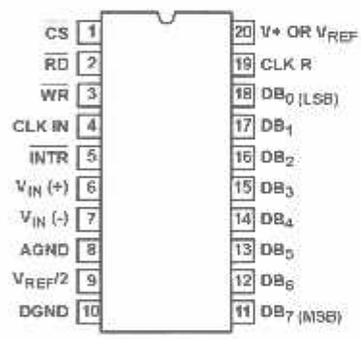


Features

- 80C48 and 80C80/85 Bus Compatible - No Interfacing Logic Required
- Conversion Time ..... <100µs
- Easy Interface to Most Microprocessors
- Will Operate in a "Stand Alone" Mode
- Differential Analog Voltage Inputs
- Works with Bandgap Voltage References
- TTL Compatible Inputs and Outputs
- On-Chip Clock Generator
- Analog Voltage Input Range (Single + 5V Supply) ..... 0V to 5V
- No Zero-Adjust Required
- 80C48 and 80C80/85 Bus Compatible - No Interfacing Logic Required

Pinout

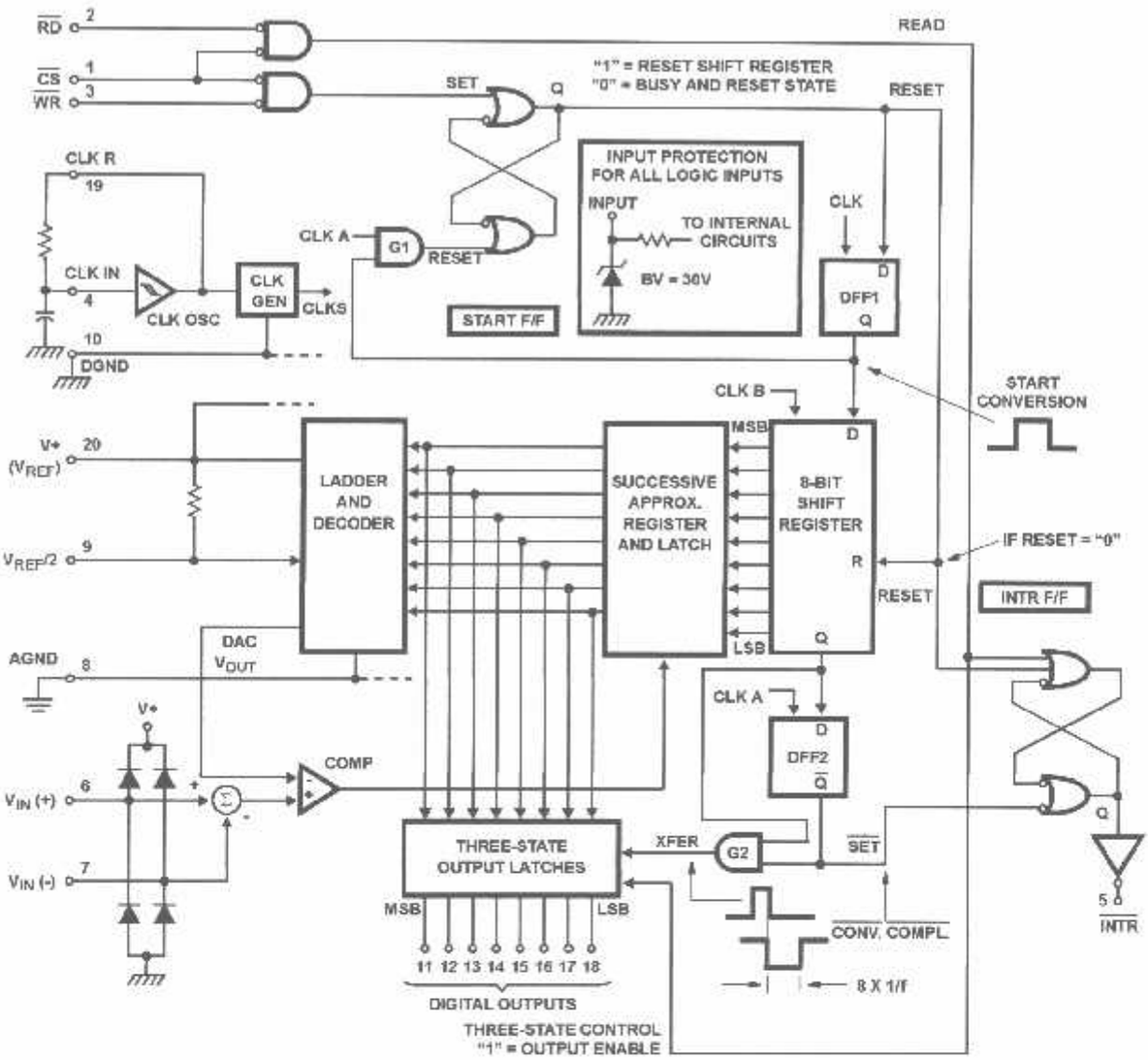
ADC0803, ADC0804
(PDIP)
TOP VIEW



Ordering Information

PART NUMBER	ERROR	EXTERNAL CONDITIONS	TEMP. RANGE (°C)	PACKAGE	PKG. NO
ADC0803LCN	$\pm^1/_2$ LSB	$V_{REF}/2$ Adjusted for Correct Full Scale Reading	0 to 70	20 Ld PDIP	E20.3
ADC0804LCN	1 LSB	$V_{REF}/2 = 2.500V_{DC}$ (No Adjustments)	0 to 70	20 Ld PDIP	E20.3

Functional Diagram



Absolute Maximum Ratings

Supply Voltage 6.5V
Voltage at Any Input . . . . . -0.3V to (V^+ +0.3V)

Operating Conditions

Temperature Range . . . . . 0^oC to 70^oC

Thermal Information

	θ_{JA} ($^oC/W$)
Thermal Resistance (Typical, Note 1)	
PDIP Package	80
Maximum Junction Temperature	
Plastic Package	150^oC
Maximum Storage Temperature Range	-65^oC to 150^oC
Maximum Lead Temperature (Soldering, 10s)	300^oC

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

NOTE:

1. θ_{JA} is measured with the component mounted on a low effective thermal conductivity test board in free air. See Tech Brief TB379 for details.

Electrical Specifications (Notes 2, 8)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
CONVERTER SPECIFICATIONS V+ = 5V, $T_A = 25^oC$ and f_{CLK} = 640kHz, Unless Otherwise Specified					
Total Unadjusted Error					
ADC0803	$V_{REF}/2$ Adjusted for Correct Full Scale Reading	-	-	$\pm 1/2$	LSB
ADC0804	$V_{REF}/2$ = 2.500V	-	-	+1	LSB
$V_{REF}/2$ Input Resistance	Input Resistance at Pin 9	1.0	1.3	-	kΩ
Analog Input Voltage Range	(Note 3)	GND-0.05	-	(V+) + 0.05	V
DC Common-Mode Rejection	Over Analog Input Voltage Range	-	$\pm 1/16$	$\pm 1/8$	LSB
Power Supply Sensitivity	V+ = 5V ±10% Over Allowed Input Voltage Range	-	$\pm 1/16$	$\pm 1/8$	LSB
CONVERTER SPECIFICATIONS V+ = 5V, 0^oC to 70^oC and f_{CLK} = 640kHz, Unless Otherwise Specified					
Total Unadjusted Error					
ADC0803	$V_{REF}/2$ Adjusted for Correct Full Scale Reading	-	-	$\pm 1/2$	LSB
ADC0804	$V_{REF}/2$ = 2.500V	-	-	+1	LSB
$V_{REF}/2$ Input Resistance	Input Resistance at Pin 9	1.0	1.3	-	kΩ
Analog Input Voltage Range	(Note 3)	GND-0.05	-	(V+) + 0.05	V
DC Common-Mode Rejection	Over Analog Input Voltage Range	-	$\pm 1/8$	$\pm 1/4$	LSB
Power Supply Sensitivity	V+ = 5V ±10% Over Allowed Input Voltage Range	-	$\pm 1/16$	$\pm 1/8$	LSB
AC TIMING SPECIFICATIONS V+ = 5V, and $T_A = 25^oC$, Unless Otherwise Specified					
Clock Frequency, f_{CLK}	V+ = 6V (Note 4)	100	640	1280	kHz
	V+ = 5V	100	640	800	kHz
Clock Periods per Conversion (Note 5), t_{CONV}		62	-	73	Clocks/Conv
Conversion Rate In Free-Running Mode, CR	$\overline{INTR}$ tied to $\overline{WR}$ with $\overline{CS}$ = 0V, f_{CLK} = 640kHz	-	-	8888	Conv/s
Width of $\overline{WR}$ Input (Start Pulse Width), $t_{W(WR)l}$	$\overline{CS}$ = 0V (Note 6)	100	-	-	ns
Access Time (Delay from Falling Edge of $\overline{RD}$ to Output Data Valid), t_{ACC}	C_L = 100pF (Use Bus Driver IC for Larger C_L)	-	135	200	ns
Three-State Control (Delay from Rising Edge of $\overline{RD}$ to HI-Z State), t_{1H}, t_{0H}	C_L = 10pF, R_L = 10K (See Three-State Test Circuits)	-	125	250	ns
Delay from Falling Edge of $\overline{WR}$ to Reset of $\overline{INTR}$, t_{WI}, t_{RI}		-	300	450	ns
Input Capacitance of Logic Control Inputs, C_{IN}		-	5	-	pF
Three-State Output Capacitance (Data Buffers), C_{OUT}		-	5	-	pF

Electrical Specifications (Notes 2, 8) (Continued)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
DC DIGITAL LEVELS AND DC SPECIFICATIONS V+ = 5V, and T_{MIN} to T_{MAX}, Unless Otherwise Specified					
CONTROL INPUTS (Note 7)					
Logic "1" Input Voltage (Except Pin 4 CLK IN), V_{INH}	V+ = 5.25V	2.0	-	V+	V
Logic "0" Input Voltage (Except Pin 4 CLK IN), V_{INL}	V+ = 4.75V	-	-	0.8	V
CLK IN (Pin 4) Positive Going Threshold Voltage, $V+_{CLK}$		2.7	3.1	3.5	V
CLK IN (Pin 4) Negative Going Threshold Voltage, $V-_{CLK}$		1.5	1.8	2.1	V
CLK IN (Pin 4) Hysteresis, V_H		0.6	1.3	2.0	V
Logic "1" Input Current (All Inputs), I_{INHI}	V_{IN} = 5V	-	0.005	1	µA
Logic "0" Input Current (All Inputs), I_{INLC}	V_{IN} = 0V	-1	-0.005	-	µA
Supply Current (Includes Ladder Current), I+	f_{CLK} = 640kHz, T_A = 25°C and $\overline{CS}$ = HI	-	1.3	2.5	mA
DATA OUTPUTS AND $\overline{INTR}$					
Logic "0" Output Voltage, V_{OL}	I_O = 1.6mA, V+ = 4.75V	-	-	0.4	V
Logic "1" Output Voltage, V_{OH}	I_O = -360µA, V+ = 4.75V	2.4	-	-	V
Three-State Disabled Output Leakage (All Data Buffers), I_{LO}	V_{OUT} = 0V	-3	-	-	µA
	V_{OUT} = 5V	-	-	3	µA
Output Short Circuit Current, I_{SOURCE}	V_{OUT} Short to GND, T_A = 25°C	4.5	6	-	mA
Output Short Circuit Current, I_{SINK}	V_{OUT} Short to V+, T_A = 25°C	9.0	16	-	mA

NOTES:

2. All voltages are measured with respect to GND, unless otherwise specified. The separate AGND point should always be wired to the DGND, being careful to avoid ground loops.
3. For $V_{IN(-)} \geq V_{IN(+)}$ the digital output code will be 0000 0000. Two on-chip diodes are tied to each analog input (see Block Diagram) which will forward conduct for analog input voltages one diode drop below ground or one diode drop greater than the V+ supply. Be careful, during testing at low V+ levels (4.5V), as high level analog inputs (5V) can cause this input diode to conduct - especially at elevated temperatures, and cause errors for analog inputs near full scale. As long as the analog V_{IN} does not exceed the supply voltage by more than 50mV, the output code will be correct. To achieve an absolute 0V to 5V input voltage range will therefore require a minimum supply voltage of 4.950V over temperature variations, initial tolerance and loading.
4. With V+ = 6V, the digital logic interfaces are no longer TTL compatible.
5. With an asynchronous start pulse, up to 8 clock periods may be required before the internal clock phases are proper to start the conversion process.
6. The $\overline{CS}$ input is assumed to bracket the $\overline{WR}$ strobe input so that timing is dependent on the $\overline{WR}$ pulse width. An arbitrarily wide pulse width will hold the converter in a reset mode and the start of conversion is initiated by the low to high transition of the $\overline{WR}$ pulse (see Timing Diagrams).
7. CLK IN (pin 4) is the input of a Schmitt trigger circuit and is therefore specified separately.
8. None of these A/Ds requires a zero-adjust. However, if an all zero code is desired for an analog input other than 0V, or if a narrow full scale span exists (for example: 0.5V to 4V full scale) the $V_{IN(-)}$ input can be adjusted to achieve this. See the Zero Error description in this data sheet.

Timing Waveforms

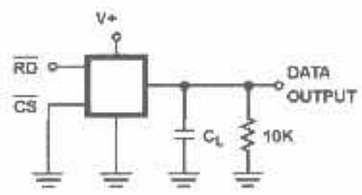


FIGURE 1A. t_{1H}

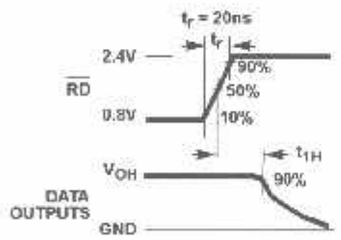


FIGURE 1B. t_{1H}, C_L = 10pF

Timing Waveforms (Continued)

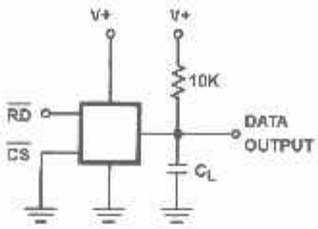


FIGURE 1C. t_{0H}

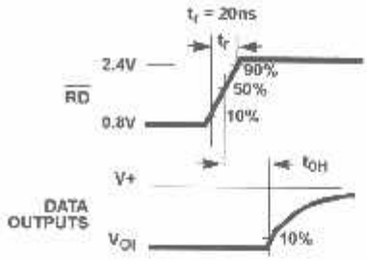


FIGURE 1D. t_{0H}, C_L = 10pF

FIGURE 1. THREE-STATE CIRCUITS AND WAVEFORMS

Typical Performance Curves

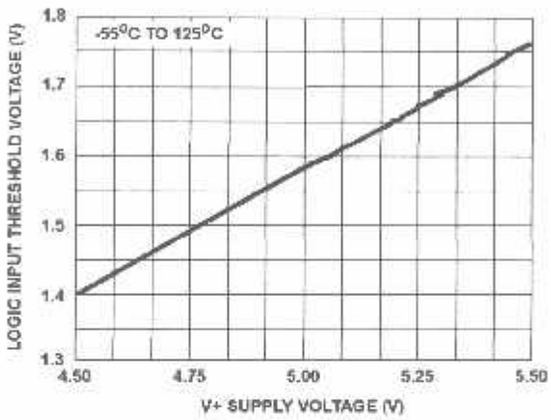


FIGURE 2. LOGIC INPUT THRESHOLD VOLTAGE vs SUPPLY VOLTAGE

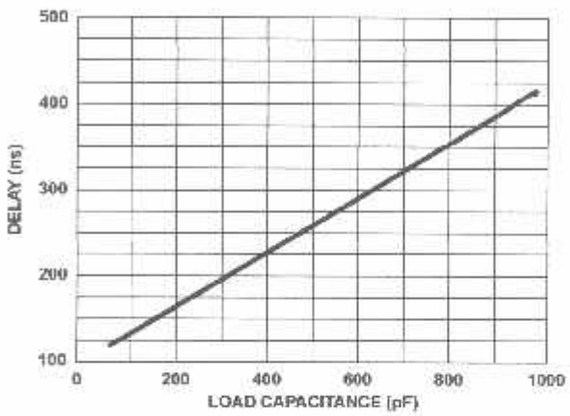


FIGURE 3. DELAY FROM FALLING EDGE OF $\overline{RD}$ TO OUTPUT DATA VALID vs LOAD CAPACITANCE

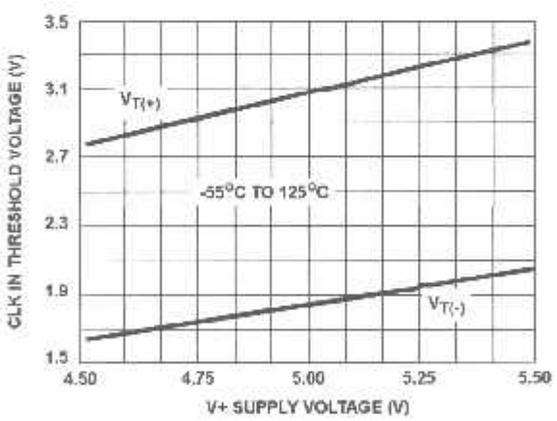


FIGURE 4. CLK IN SCHMITT TRIP LEVELS vs SUPPLY VOLTAGE

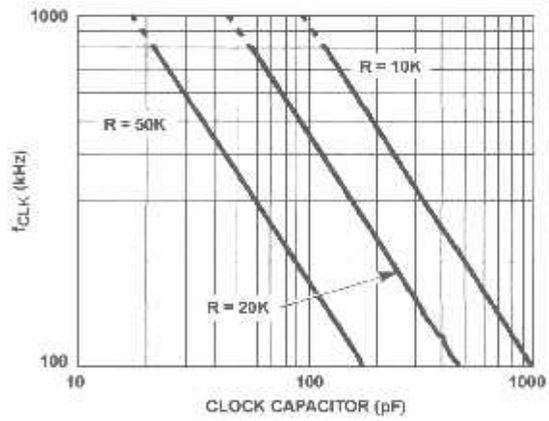


FIGURE 5. f_{CLK} vs CLOCK CAPACITOR

Typical Performance Curves (Continued)

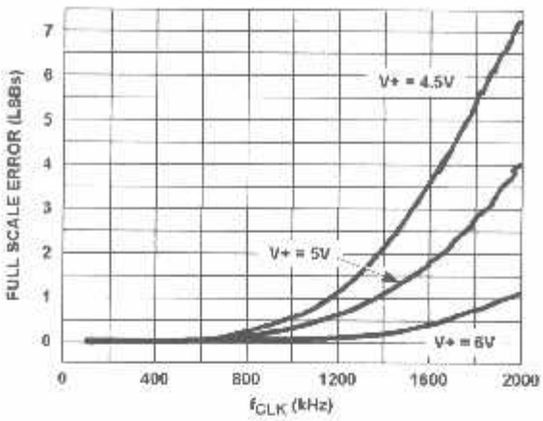


FIGURE 6. FULL SCALE ERROR vs f_{CLK}

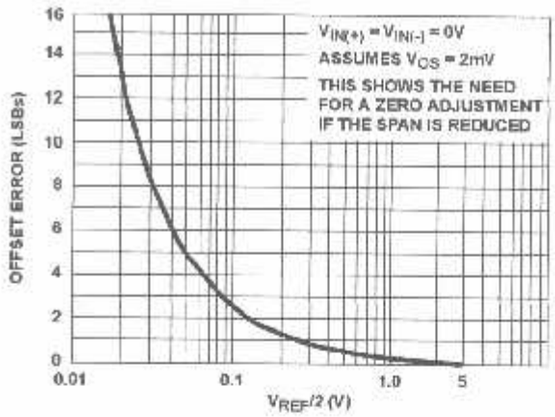


FIGURE 7. EFFECT OF UNADJUSTED OFFSET ERROR

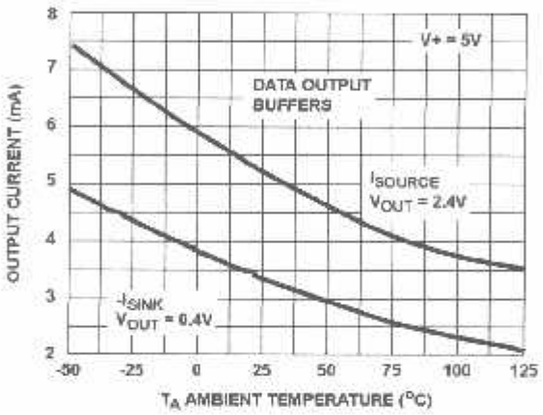


FIGURE 8. OUTPUT CURRENT vs TEMPERATURE

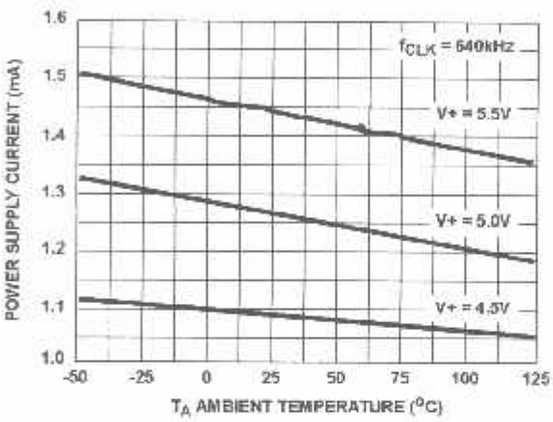


FIGURE 9. POWER SUPPLY CURRENT vs TEMPERATURE

Timing Diagrams

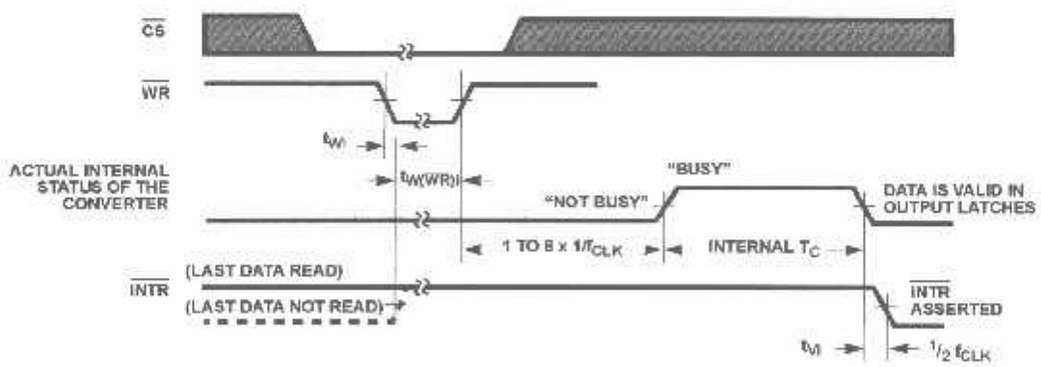


FIGURE 10A. START CONVERSION

Timing Diagrams (Continued)

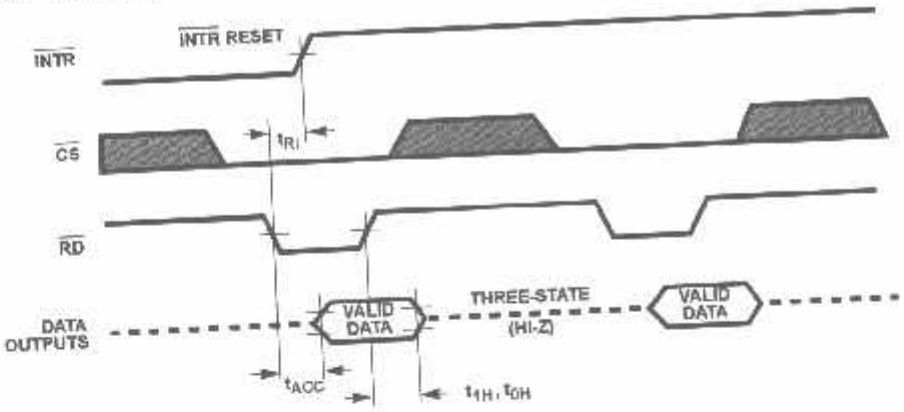


FIGURE 10B. OUTPUT ENABLE AND RESET INTR

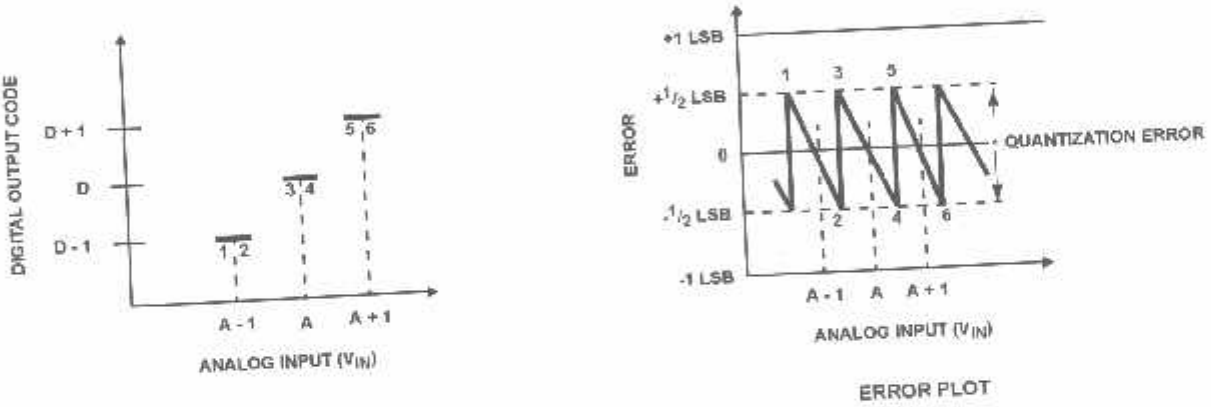


FIGURE 11A. ACCURACY = ±0 LSB: PERFECT A/D

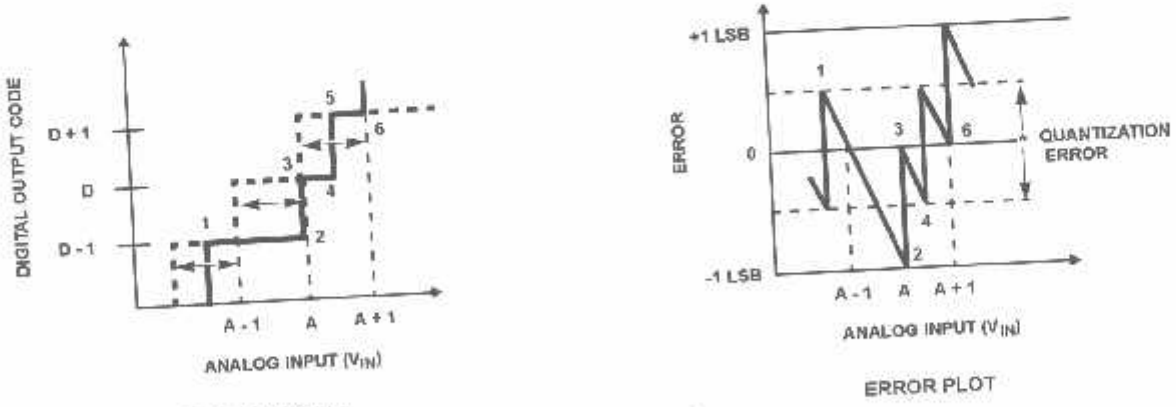


FIGURE 11B. ACCURACY = ±1/2 LSB

FIGURE 11. CLARIFYING THE ERROR SPECS OF AN A/D CONVERTER

Understanding A/D Error Specs

A perfect A/D transfer characteristic (staircase wave-form) is shown in Figure 11A. The horizontal scale is analog input voltage and the particular points labeled are in steps of 1 LSB (19.53mV with 2.5V tied to the $V_{REF}/2$ pin). The digital output codes which correspond to these inputs are shown as D-*, D, and D+1. For the perfect A/D, not only will center-value (A - 1, A, A + 1, . . .) analog inputs produce the correct output digital codes, but also each riser (the transitions between adjacent output codes) will be located $\pm 1/2$ LSB away from each center-value. As shown, the risers are ideal and have no width. Correct digital output codes will be provided for a range of analog input voltages which extend $\pm 1/2$ LSB from the ideal center-values. Each tread (the range of analog input voltage which provides the same digital output code) is therefore 1 LSB wide.

The error curve of Figure 11B shows the worst case transfer function for the ADC080X. Here the specification guarantees that if we apply an analog input equal to the LSB analog voltage center-value, the A/D will produce the correct digital code.

Next to each transfer function is shown the corresponding error plot. Notice that the error includes the quantization uncertainty of the A/D. For example, the error at point 1 of Figure 11A is $+1/2$ LSB because the digital code appeared $1/2$ LSB in advance of the center-value of the tread. The error plots always have a constant negative slope and the abrupt upside steps are always 1 LSB in magnitude, unless the device has missing codes.

Detailed Description

The functional diagram of the ADC080X series of A/D converters operates on the successive approximation principle (see Application Notes AN016 and AN020 for a more detailed description of this principle). Analog switches are closed sequentially by successive-approximation logic until the analog differential input voltage $[V_{IN(+)} - V_{IN(-)}]$ matches a voltage derived from a tapped resistor string across the reference voltage. The most significant bit is tested first and after 8 comparisons (64 clock cycles), an 8-bit binary code (1111 1111 = full scale) is transferred to an output latch.

The normal operation proceeds as follows. On the high-to low transition of the WR input, the internal SAR latches and the shift-register stages are reset, and the INTR output will be set high. As long as the CS input and WR input remain low, the A/D will remain in a reset state. Conversion will start from 1 to 8 clock periods after at least one of these inputs makes a low-to-high transition. After the requisite number of clock pulses to complete the conversion, the INTR pin will make a high-to-low transition. This can be used to interrupt a processor, or otherwise signal the availability of a new conversion. A RD operation (with CS low) will clear the INTR line high again. The device may be operated in the free-running mode by connecting INTR to the WR input with CS = 0. To ensure start-up under all possible conditions, an external WR pulse is required during the first power-up cycle. A conversion-in-process can be interrupted by issuing a second start command.

Digital Operation

The converter is started by having CS and WR simultaneously low. This sets the start flip-flop (F/F) and the resulting "1" level resets the 8-bit shift register, resets the interrupt (INTR) F/F and inputs a "1" to the D flip-flop, DFF1, which is at the input end of the 8-bit shift register. Internal clock signals then transfer this "1" to the Q output of DFF1. The AND gate, G1, combines this "1" output with a clock signal to provide a reset signal to the start F/F. If the set signal is no longer present (either WR or CS is a "1"), the start F/F is reset and the 8-bit shift register then can have the "1" clocked in, which starts the conversion process. If the set signal were to still be present, this reset pulse would have no effect (both outputs of the start F/F would be at a "1" level) and the 8-bit shift register would continue to be held in the reset mode. This allows for asynchronous or wide CS and WR signals.

After the "1" is clocked through the 8-bit shift register (which completes the SAR operation) it appears as the input to DFF2. As soon as this "1" is output from the shift register, the AND gate, G2, causes the new digital word to transfer to the Three-State output latches. When DFF2 is subsequently clocked, the $\overline{Q}$ output makes a high-to-low transition which causes the INTR F/F to set. An inverting buffer then supplies the $\overline{INTR}$ output signal.

When data is to be read, the combination of both $\overline{CS}$ and $\overline{RD}$ being low will cause the INTR F/F to be reset and the three-state output latches will be enabled to provide the 8-bit digital outputs.

Digital Control Inputs

The digital control inputs (CS, RD, and WR) meet standard TTL logic voltage levels. These signals are essentially equivalent to the standard A/D Start and Output Enable control signals, and are active low to allow an easy interface to microprocessor control busses. For non-microprocessor based applications, the CS input (pin 1) can be grounded and the standard A/D Start function obtained by an active low pulse at the WR input (pin 3). The Output Enable function is achieved by an active low pulse at the RD input (pin 2).

Analog Operation

The analog comparisons are performed by a capacitive charge summing circuit. Three capacitors (with precise ratioed values) share a common node with the input to an auto-zeroed comparator. The input capacitor is switched between $V_{IN(+)}$ and $V_{IN(-)}$, while two ratioed reference capacitors are switched between taps on the reference voltage divider string. The net charge corresponds to the weighted difference between the input and the current total value set by the

successive approximation register. A correction is made to offset the comparison by $^1/_2$ LSB (see Figure 11A).

Analog Differential Voltage Inputs and Common-Mode Rejection

This A/D gains considerable applications flexibility from the analog differential voltage input. The $V_{IN(-)}$ input (pin 7) can be used to automatically subtract a fixed voltage value from the input reading (tare correction). This is also useful in 4mA - 20mA current loop conversion. In addition, common-mode noise can be reduced by use of the differential input.

The time interval between sampling $V_{IN(+)}$ and $V_{IN(-)}$ is $4^1/_2$ clock periods. The maximum error voltage due to this slight time difference between the input voltage samples is given by:

$$\Delta V_E(MAX) = (V_{PEAK})(2\pi f_{CM})\left[\frac{4.5}{f_{CLK}}\right]$$

where:

ΔV_E is the error voltage due to sampling delay,

V_{PEAK} is the peak value of the common-mode voltage,

f_{CM} is the common-mode frequency.

For example, with a 60Hz common-mode frequency, f_{CM}, and a 640kHz A/D clock, f_{CLK}, keeping this error to $^1/_4$ LSB (~5mV) would allow a common-mode voltage, V_{PEAK}, given by:

$$V_{PEAK} = \frac{\left[\frac{\Delta V_{E(MAX)}(f_{CLK})}{(2\pi f_{CM})(4.5)}\right]}{}$$

or

$$V_{PEAK} = \frac{(5\times10^{-3})(640\times10^{3})}{(6.28)(60)(4.5)} \cong 1.9V.$$

The allowed range of analog input voltage usually places more severe restrictions on input common-mode voltage levels than this.

An analog input voltage with a reduced span and a relatively large zero offset can be easily handled by making use of the differential input (see Reference Voltage Span Adjust).

Analog Input Current

The internal switching action causes displacement currents to flow at the analog inputs. The voltage on the on-chip capacitance to ground is switched through the analog differential input voltage, resulting in proportional currents entering the $V_{IN(+)}$ input and leaving the $V_{IN(-)}$ input. These current transients occur at the leading edge of the internal clocks. They rapidly decay and do not inherently cause errors as the on-chip comparator is strobed at the end of the clock period.

Input Bypass Capacitors

Bypass capacitors at the inputs will average these charges and cause a DC current to flow through the output resistances of the analog signal sources. This charge pumping action is worse for continuous conversions with the $V_{IN(+)}$ input voltage at full scale. For a 640kHz clock frequency with the $V_{IN(+)}$ input at 5V, this DC current is at a maximum of approximately 5µA. Therefore, **bypass capacitors should not be used at the analog inputs or the $V_{REF}/2$** pin for high resistance sources (>1kΩ). If input bypass capacitors are necessary for noise filtering and high source resistance is desirable to minimize capacitor size, the effects of the voltage drop across this input resistance, due to the average value of the input current, can be compensated by a full scale adjustment while the given source resistor and input bypass capacitor are both in place. This is possible because the average value of the input current is a precise linear function of the differential input voltage at a constant conversion rate.

Input Source Resistance

Large values of source resistance where an input bypass capacitor is not used will not cause errors since the input currents settle out prior to the comparison time. If a low-pass filter is required in the system, use a low-value series resistor (≤1kΩ) for a passive RC section or add an op amp RC active low-pass filter. For low-source-resistance applications (<1kΩ), a 0.1µF bypass capacitor at the inputs will minimize EMI due to the series lead inductance of a long wire. A 100Ω series resistor can be used to isolate this capacitor (both the R and C are placed outside the feedback loop) from the output of an op amp, if used.

Stray Pickup

The leads to the analog inputs (pins 6 and 7) should be kept as short as possible to minimize stray signal pickup (EMI). Both EMI and undesired digital-clock coupling to these inputs can cause system errors. The source resistance for these inputs should, in general, be kept below 5kΩ. Larger values of source resistance can cause undesired signal pickup. Input bypass capacitors, placed from the analog inputs to ground, will eliminate this pickup but can create analog scale errors as these capacitors will average the transient input switching currents of the A/D (see Analog Input Current). This scale error depends on both a large source resistance and the use of an input bypass capacitor. This error can be compensated by a full scale adjustment of the A/D (see Full Scale Adjustment) with the source resistance and input bypass capacitor in place, and the desired conversion rate.

Reference Voltage Span Adjust

For maximum application flexibility, these A/Ds have been designed to accommodate a 5V, 2.5V or an adjusted voltage reference. This has been achieved in the design of the IC as shown in Figure 12.

Notice that the reference voltage for the IC is either $^1/_2$ of the voltage which is applied to the V+ supply pin, or is equal to the voltage which is externally forced at the $V_{REF}/2$ pin. This allows for a pseudo-ratiometric voltage reference using, for the V+ supply, a 5V reference voltage. Alternatively, a voltage less than 2.5V can be applied to the $V_{REF}/2$ input. The internal gain to the $V_{REF}/2$ input is 2 to allow this factor of 2 reduction in the reference voltage.

Such an adjusted reference voltage can accommodate a reduced span or dynamic voltage range of the analog input voltage. If the analog input voltage were to range from 0.5V to 3.5V, instead of 0V to 5V, the span would be 3V. With 0.5V applied to the $V_{IN(-)}$ pin to absorb the offset, the reference voltage can be made equal to $^1/_2$ of the 3V span or 1.5V. The A/D now will encode the $V_{IN(+)}$ signal from 0.5V to 3.5V with the 0.5V input corresponding to zero and the 3.5V input corresponding to full scale. The full 8 bits of resolution are therefore applied over this reduced analog input voltage range. The requisite connections are shown in Figure 13. For expanded scale inputs, the circuits of Figures 14 and 15 can be used.

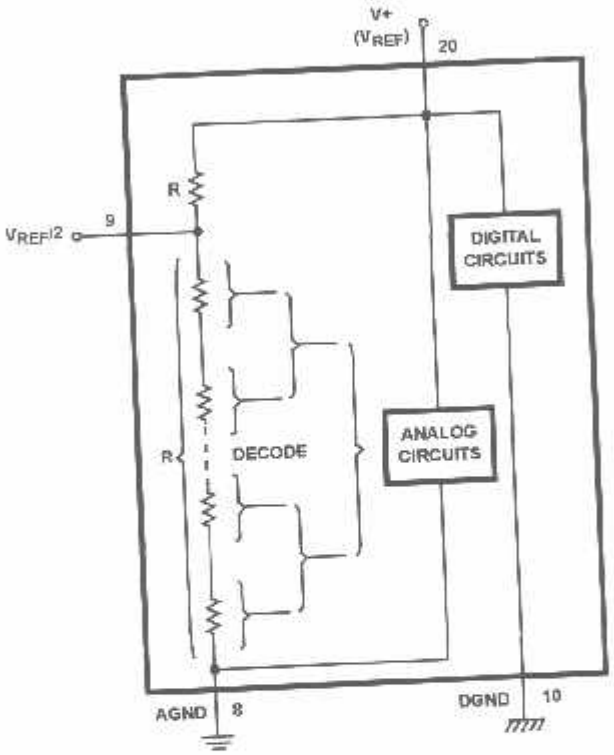


FIGURE 12. THE $V_{REFERENCE}$ DESIGN ON THE IC

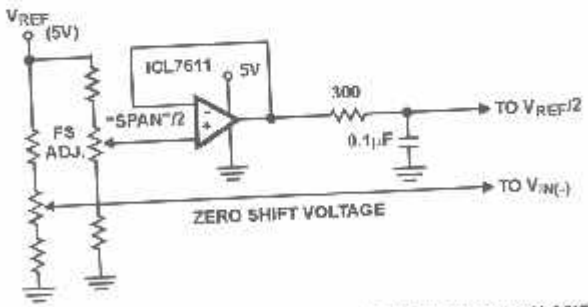


FIGURE 13. OFFSETTING THE ZERO OF THE ADC080X AND PERFORMING AN INPUT RANGE (SPAN) ADJUSTMENT

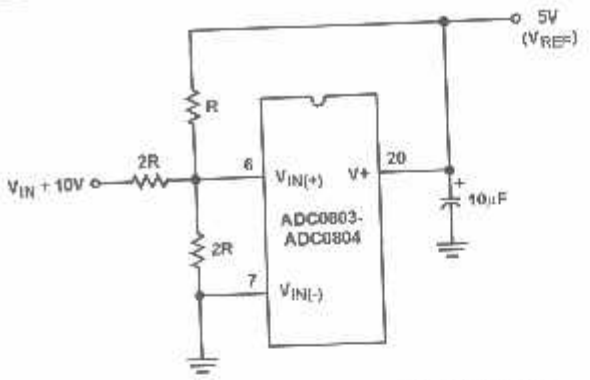


FIGURE 14. HANDLING ±10V ANALOG INPUT RANGE

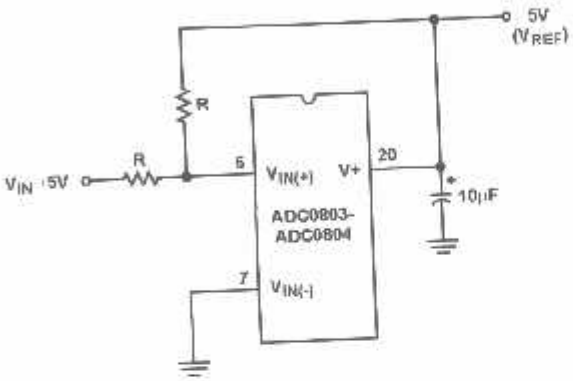


FIGURE 15. HANDLING ±5V ANALOG INPUT RANGE

Reference Accuracy Requirements

The converter can be operated in a pseudo-ratiometric mode or an absolute mode. In ratiometric converter applications, the magnitude of the reference voltage is a factor in both the output of the source transducer and the output of the A/D converter and therefore cancels out in the final digital output code. In absolute conversion applications, both the initial value and the temperature stability of the reference voltage are important accuracy factors in the operation of the A/D converter. For $V_{REF}/2$ voltages of 2.5V nominal value, initial errors of ±10mV will cause conversion errors of ±1 LSB due to the gain of 2 of the $V_{REF}/2$ input. In reduced span applications, the initial value and the stability of the $V_{REF}/2$ input voltage become even more important. For example, if the span is reduced to 2.5V, the analog input LSB voltage value is correspondingly reduced from 20mV (5V span) to 10mV and 1 LSB at the $V_{REF}/2$ input becomes 5mV. As can be seen, this reduces the allowed initial tolerance of the reference voltage and requires correspondingly less absolute change with temperature variations. Note that spans smaller than 2.5V place even tighter requirements on the initial accuracy and stability of the reference source.

In general, the reference voltage will require an initial adjustment. Errors due to an improper value of reference voltage appear as full scale errors in the A/D transfer

function. IC voltage regulators may be used for references if the ambient temperature changes are not excessive.

Zero Error

The zero of the A/D does not require adjustment. If the minimum analog input voltage value, $V_{IN(MIN)}$, is not ground, a zero offset can be done. The converter can be made to output 0000 0000 digital code for this minimum input voltage by biasing the A/D $V_{IN(-)}$ input at this $V_{IN(MIN)}$ value (see Applications section). This utilizes the differential mode operation of the A/D.

The zero error of the A/D converter relates to the location of the first riser of the transfer function and can be measured by grounding the $V_{IN(-)}$ input and applying a small magnitude positive voltage to the $V_{IN(+)}$ input. Zero error is the difference between the actual DC input voltage which is necessary to just cause an output digital code transition from 0000 0000 to 0000 0001 and the ideal $^1/_2$ LSB value ($^1/_2$ LSB = 9.8mV for $V_{REF}/2$ = 2.500V).

Full Scale Adjust

The full scale adjustment can be made by applying a differential input voltage which is $1^1/_2$ LSB down from the desired analog full scale voltage range and then adjusting the magnitude of the $V_{REF}/2$ input (pin 9) for a digital output code which is just changing from 1111 1110 to 1111 1111. When offsetting the zero and using a span-adjusted $V_{REF}/2$ voltage, the full scale adjustment is made by inputting V_{MIN} to the $V_{IN(-)}$ input of the A/D and applying a voltage to the $V_{IN(+)}$ input which is given by:

$$V_{IN(+)}{}_{fSADJ} = V_{MAX} - 1.5\left[\frac{(V_{MAX} - V_{MIN})}{256}\right],$$

where:

V_{MAX} = the high end of the analog input range, and

V_{MIN} = the low end (the offset zero) of the analog range. (Both are ground referenced.)

Clocking Option

The clock for the A/D can be derived from an external source such as the CPU clock or an external RC network can be added to provide self-clocking. The CLK IN (pin 4) makes use of a Schmitt trigger as shown in Figure 16.

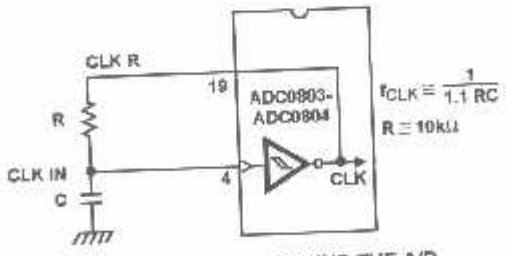


FIGURE 16. SELF-CLOCKING THE A/D

Heavy capacitive or DC loading of the CLK R pin should be avoided as this will disturb normal converter operation. Loads less than 50pF, such as driving up to 7 A/D converter clock inputs from a single CLK R pin of 1 converter, are allowed. For larger clock line loading, a CMOS or low power TTL buffer or PNP input logic should be used to minimize the loading on the CLK R pin (do not use a standard TTL buffer).

Restart During a Conversion

If the A/D is restarted ($\overline{CS}$ and $\overline{WR}$ go low and return high) during a conversion, the converter is reset and a new conversion is started. The output data latch is not updated if the conversion in progress is not completed. The data from the previous conversion remain in this latch.

Continuous Conversions

In this application, the $\overline{CS}$ input is grounded and the $\overline{WR}$ input is tied to the $\overline{INTR}$ output. This $\overline{WR}$ and $\overline{INTR}$ node should be momentarily forced to logic low following a power-up cycle to insure circuit operation. See Figure 17 for details.

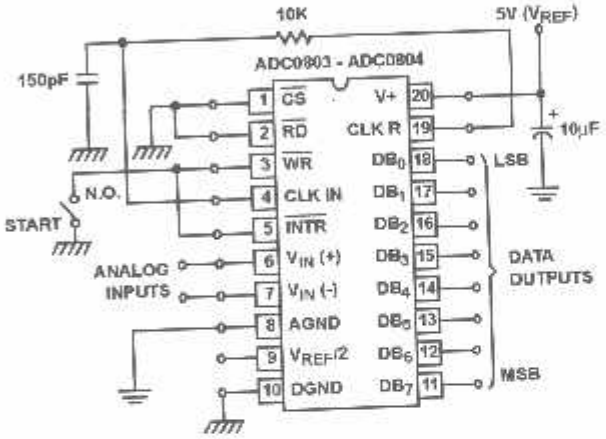


FIGURE 17. FREE-RUNNING CONNECTION

Driving the Data Bus

This CMOS A/D, like MOS microprocessors and memories, will require a bus driver when the total capacitance of the data bus gets large. Other circuitry, which is tied to the data bus, will add to the total capacitive loading, even in three-state (high-impedance mode). Back plane busing also greatly adds to the stray capacitance of the data bus.

There are some alternatives available to the designer to handle this problem. Basically, the capacitive loading of the data bus slows down the response time, even though DC specifications are still met. For systems operating with a relatively slow CPU clock frequency, more time is available in which to establish proper logic levels on the bus and therefore higher capacitive loads can be driven (see Typical Performance Curves).

At higher CPU clock frequencies time can be extended for I/O reads (and/or writes) by inserting wait states (8080) or using clock-extending circuits (6800).

Finally, if time is short and capacitive loading is high, external bus drivers must be used. These can be three-state buffers (low power Schottky is recommended, such as the 74LS240 series) or special higher-drive-current products which are designed as bus drivers. High-current bipolar bus drivers with PNP inputs are recommended.

Power Supplies

Noise spikes on the V+ supply line can cause conversion errors as the comparator will respond to this noise. A low-inductance tantalum filter capacitor should be used close to the converter V+ pin, and values of 1µF or greater are recommended. If an unregulated voltage is available in the system, a separate 5V voltage regulator for the converter (and other analog circuitry) will greatly reduce digital noise on the V+ supply. An ICL7663 can be used to regulate such a supply from an input as low as 5.2V.

Wiring and Hook-Up Precautions

Standard digital wire-wrap sockets are not satisfactory for breadboarding with this A/D converter. Sockets on PC boards can be used. All logic signal wires and leads should be grouped and kept as far away as possible from the analog signal leads. Exposed leads to the analog inputs can cause undesired digital noise and hum pickup; therefore, shielded leads may be necessary in many applications.

A single-point analog ground should be used which is separate from the logic ground points. The power supply bypass capacitor and the self clocking capacitor (if used) should both be returned to digital ground. Any $V_{REF}/2$ bypass capacitors, analog input filter capacitors, or input signal shielding should be returned to the analog ground point. A test for proper grounding is to measure the zero error of the A/D converter. Zero errors in excess of $^1/_4$ LSB can usually be traced to improper board layout and wiring (see Zero Error for measurement). Further information can be found in Application Note AN018.

Testing the A/D Converter

There are many degrees of complexity associated with testing an A/D converter. One of the simplest tests is to apply a known analog input voltage to the converter and use LEDs to display the resulting digital output code as shown in Figure 18.

For ease of testing, the $V_{REF}/2$ (pin 9) should be supplied with 2.560V and a V+ supply voltage of 5.12V should be used. This provides an LSB value of 20mV.

If a full scale adjustment is to be made, an analog input voltage of 5.090V (5.120 - $1^1/_2$ LSB) should be applied to the $V_{IN(+)}$ pin with the $V_{IN(-)}$ pin grounded. The value of the $V_{REF}/2$ input voltage should be adjusted until the digital output code is just changing from 1111 1110 to 1111 1111. This value of $V_{REF}/2$ should then be used for all the tests.

The digital-output LED display can be decoded by dividing the 8 bits into 2 hex characters, one with the 4 most-significant bits (MS) and one with the 4 least-significant bits (LS). The output is then interpreted as a sum of fractions times the full scale voltage:

$$V_{OUT} = \left(\frac{MS}{16} + \frac{LS}{256}\right)(5.12)V.$$

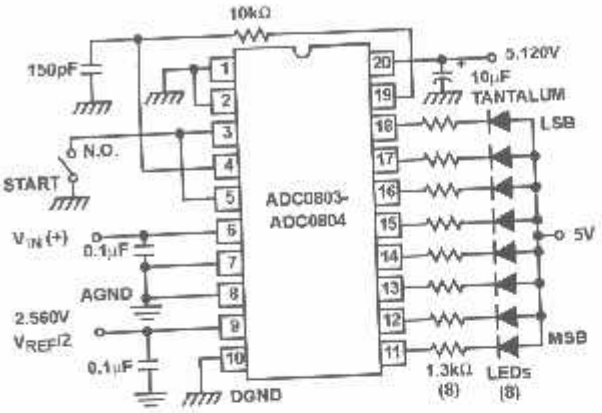


FIGURE 18. BASIC TESTER FOR THE A/D

For example, for an output LED display of 1011 0110, the MS character is hex B (decimal 11) and the LS character is hex (and decimal) 6, so

$$V_{OUT} = \left(\frac{11}{16} + \frac{6}{256}\right)(5.12) = 3.84V.$$

Figures 19 and 20 show more sophisticated test circuits.

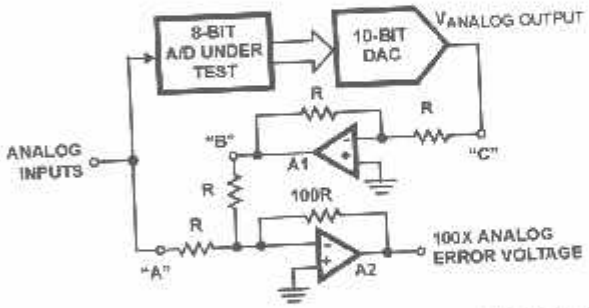


FIGURE 19. A/D TESTER WITH ANALOG ERROR OUTPUT. THIS CIRCUIT CAN BE USED TO GENERATE "ERROR PLOTS" OF FIGURE 11.

FIGURE 20. BASIC "DIGITAL" A/D TESTER

Typical Applications

Interfacing 8080/85 or Z-80 Microprocessors

This converter has been designed to directly interface with 8080/85 or Z-80 Microprocessors. The three-state output capability of the A/D eliminates the need for a peripheral interface device, although address decoding is still required to generate the appropriate $\overline{CS}$ for the converter. The A/D can be mapped into memory space (using standard memory-address decoding for $\overline{CS}$ and the $\overline{MEMR}$ and $\overline{MEMW}$ strobes) or it can be controlled as an I/O device by using the $\overline{I/OR}$ and $\overline{I/OW}$ strobes and decoding the address bits A0 → A7 (or address bits A8 → A15, since they will contain the same 8-bit address information) to obtain the $\overline{CS}$ input. Using the I/O space provides 256 additional addresses and may allow a simpler 8-bit address decoder, but the data can only be input to the accumulator. To make use of the additional memory reference instructions, the A/D should be mapped into memory space. See AN020 for more discussion of memory-mapped vs I/O-mapped interfaces. An example of an A/D in I/O space is shown in Figure 21.

The standard control-bus signals of the 8080 ($\overline{CS}$, $\overline{RD}$ and $\overline{WR}$) can be directly wired to the digital control inputs of the A/D, since the bus timing requirements, to allow both starting the converter, and outputting the data onto the data bus, are met. A bus driver should be used for larger microprocessor systems where the data bus leaves the PC board and/or must drive capacitive loads larger than 100pF.

It is useful to note that in systems where the A/D converter is 1 of 8 or fewer I/O-mapped devices, no address-decoding circuitry is necessary. Each of the 8 address bits (A0 to A7) can be directly used as $\overline{CS}$ inputs, one for each I/O device.

Interfacing the Z-80 and 8085

The Z-80 and 8085 control buses are slightly different from that of the 8080. General $\overline{RD}$ and $\overline{WR}$ strobes are provided and separate memory request, $\overline{MREQ}$, and I/O request, $\overline{IORQ}$, signals have to be combined with the generalized strobes to provide the appropriate signals. An advantage of operating the A/D in I/O space with the Z-80 is that the CPU will automatically insert one wait state (the $\overline{RD}$ and $\overline{WR}$ strobes are extended one clock period) to allow more time for the I/O devices to respond. Logic to map the A/D in I/O space is shown in Figure 22. By using $\overline{MREQ}$ in place of $\overline{IORQ}$, a memory-mapped configuration results.

Additional I/O advantages exist as software DMA routines are available and use can be made of the output data transfer which exists on the upper 8 address lines (A8 to A15) during I/O input instructions. For example, MUX channel selection for the A/D can be accomplished with this operating mode.

The 8085 also provides a generalized $\overline{RD}$ and $\overline{WR}$ strobe, with an IO/$\overline{M}$ line to distinguish I/O and memory requests. The circuit of Figure 22 can again be used, with IO/$\overline{M}$ in place of $\overline{IORQ}$ for a memory-mapped interface, and an extra inverter (or the logic equivalent) to provide $\overline{IO/M}$ for an I/O-mapped connection.

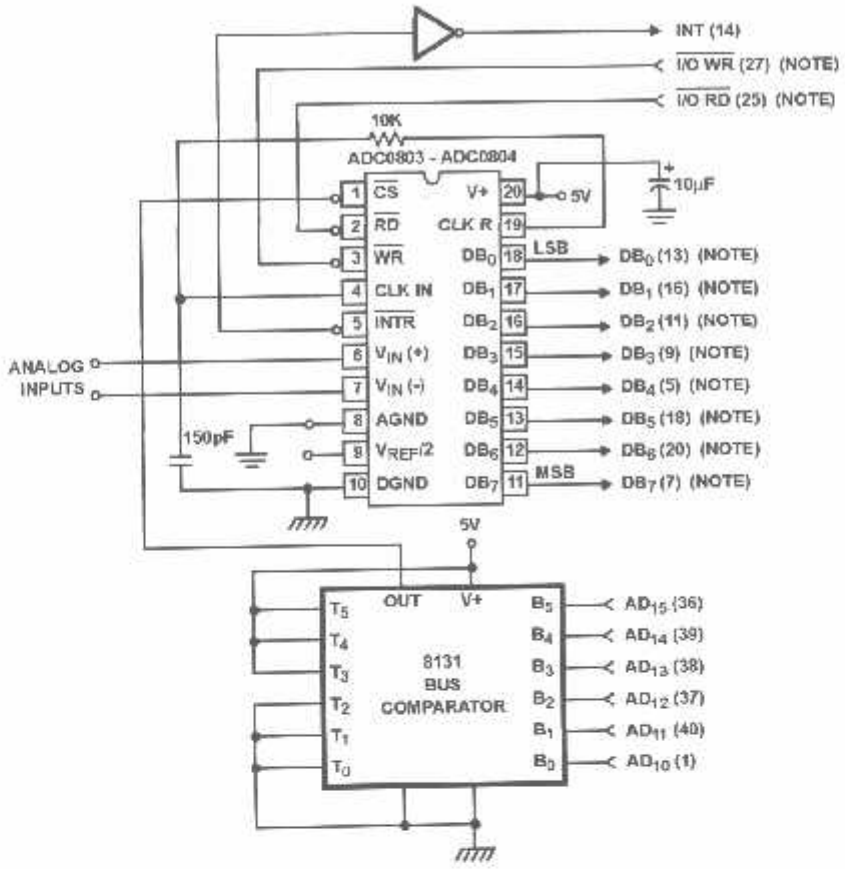
Interfacing 6800 Microprocessor Derivatives (6502, etc.)

The control bus for the 6800 microprocessor derivatives does not use the RD and WR strobe signals. Instead it employs a single R/W line and additional timing, if needed, can be derived from the $\phi 2$ clock. All I/O devices are memory-mapped in the 6800 system, and a special signal, VMA, indicates that the current address is valid. Figure 23 shows an interface schematic where the A/D is memory-mapped in the 6800 system. For simplicity, the CS decoding is shown using $^1/_2$ DM8092. Note that in many 6800 systems, an already decoded $\overline{4/5}$ line is brought out to the common bus at pin 21. This can be tied directly to the CS pin of the A/D, provided that no other devices are addressed at HEX ADDR: 4XXX or 5XXX.

In Figure 24 the ADC080X series is interfaced to the MC6800 microprocessor through (the arbitrarily chosen) Port B of the MC6820 or MC6821 Peripheral Interface Adapter (PIA). Here the CS pin of the A/D is grounded since the PIA is already memory-mapped in the MC6800 system and no CS decoding is necessary. Also notice that the A/D output data lines are connected to the microprocessor bus under program control through the PIA and therefore the A/D RD pin can be grounded.

Application Notes

NOTE #	DESCRIPTION
AN016	"Selecting A/D Converters"
AN018	"Do's and Don'ts of Applying A/D Converters"
AN020	"A Cookbook Approach to High Speed Data Acquisition and Microprocessor Interfacing"
AN030	"The ICL7104 - A Binary Output A/D Converter for Microprocessors"



NOTE. Pin numbers for 8228 System Controller. Others are 8080A.

FIGURE 21. ADC080X TO 8080A CPU INTERFACE

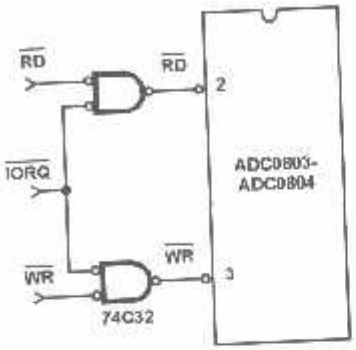
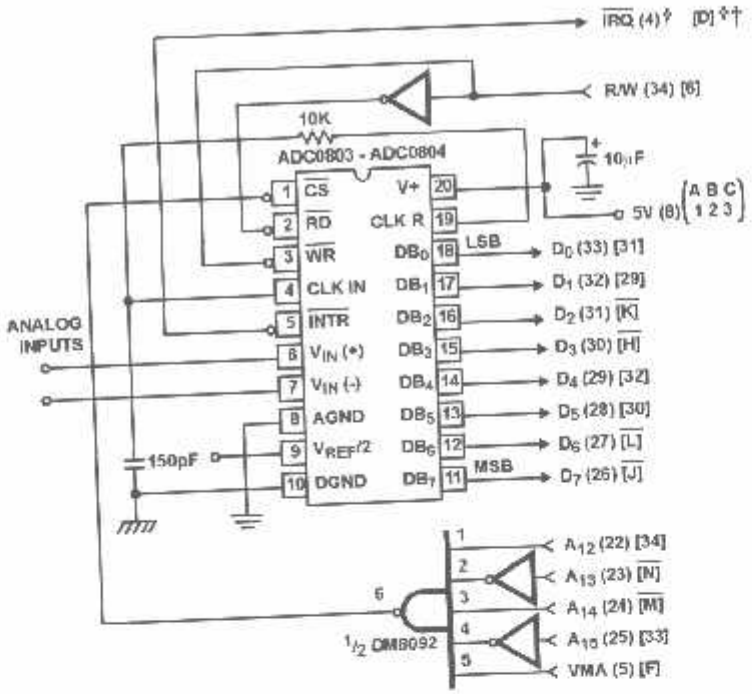


FIGURE 22. MAPPING THE A/D AS AN I/O DEVICE FOR USE WITH THE Z-80 CPU



† Numbers in parentheses refer to MC6800 CPU Pinout.
†† Numbers or letters in brackets refer to standard MC6800 System Common Bus Code.

FIGURE 23. ADC080X TO MC6800 CPU INTERFACE

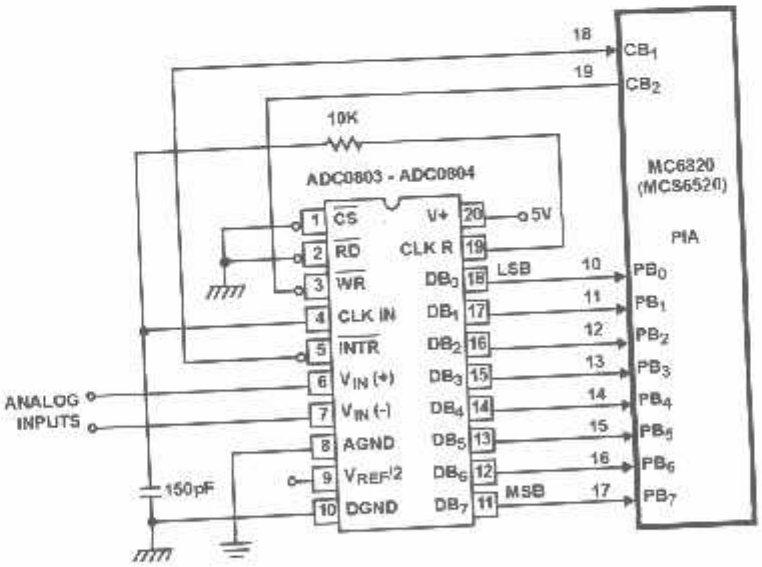


FIGURE 24. ADC080X TO MC6820 PIA INTERFACE

Die Characteristics

DIE DIMENSIONS

101 mils x 93 mils

METALLIZATION

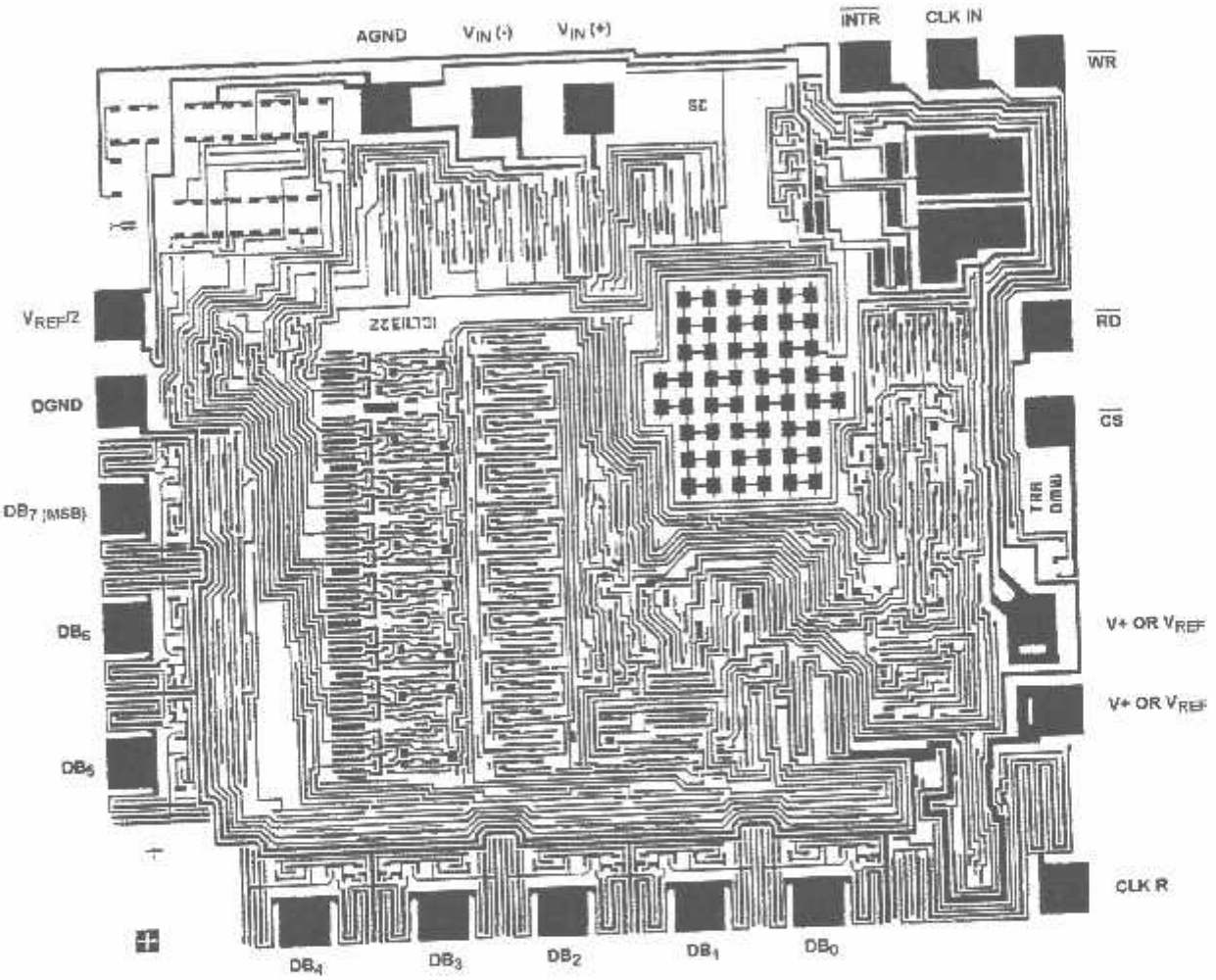
Type: Al
Thickness: 10kÅ ±1kÅ

PASSIVATION

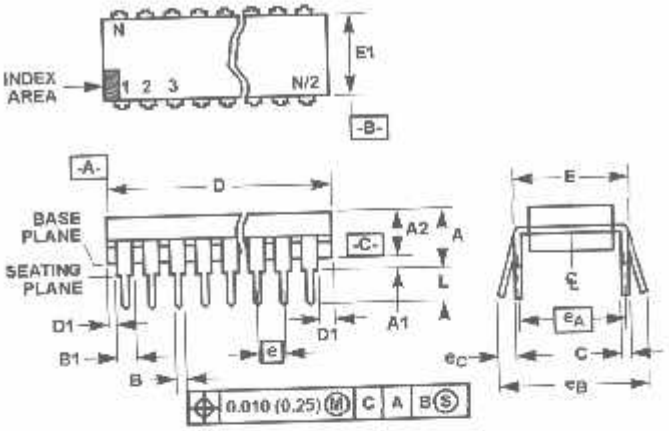
Type: Nitride over Silox
Nitride Thickness: 8kÅ
Silox Thickness: 7kÅ

Metallization Mask Layout

ADC0803, ADC0804



Dual-In-Line Plastic Packages (PDIP)



NOTES:

1. Controlling Dimensions: INCH. In case of conflict between English and Metric dimensions, the inch dimensions control.
2. Dimensioning and tolerancing per ANSI Y14.5M-1982.
3. Symbols are defined in the "MO Series Symbol List" in Section 2.2 of Publication No. 95.
4. Dimensions A, A1 and L are measured with the package seated in JEDEC seating plane gauge GS-3.
5. D, D1, and E1 dimensions do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.010 inch (0.25mm).
6. E and e_A are measured with the leads constrained to be perpendicular to datum -C-.
7. e_B and e_C are measured at the lead tips with the leads unconstrained. e_C must be zero or greater.
8. B1 maximum dimensions do not include dambar protrusions. Dambar protrusions shall not exceed 0.010 inch (0.25mm).
9. N is the maximum number of terminal positions.
10. Corner leads (1, N, N/2 and N/2 + 1) for E8.3, E16.3, E18.3, E28.3, E42.6 will have a B1 dimension of 0.030 - 0.045 inch (0.76 - 1.14mm).

E20.3 (JEDEC MS-001-AD ISSUE D)
20 LEAD DUAL-IN-LINE PLASTIC PACKAGE

SYMBOL	INCHES MIN	INCHES MAX	MILLIMETERS MIN	MILLIMETERS MAX	NOTES
A	-	0.210	-	5.33	4
A1	0.015	-	0.39	-	4
A2	0.115	0.195	2.93	4.95	-
B	0.014	0.022	0.358	0.558	-
B1	0.045	0.070	1.55	1.77	8
C	0.008	0.014	0.204	0.355	-
D	0.980	1.060	24.89	26.9	5
D1	0.005	-	0.13	-	5
E	0.300	0.325	7.62	8.25	6
E1	0.240	0.280	6.10	7.11	5
e	0.100 BSC		2.54 BSC		-
e_A	0.300 BSC		7.62 BSC		6
e_B	-	0.430	-	10.92	7
L	0.115	0.150	2.93	3.81	4
N	20		20		9

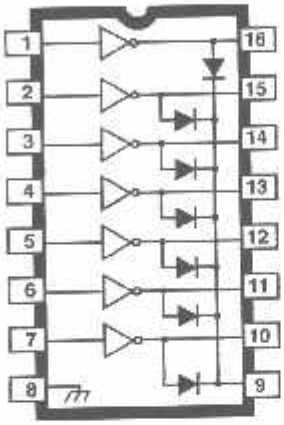
Rev. 0 12/93

TRANSFORMER
12V
Diode Bridge
4700uF
100uF
LM7805
GND
+5V
100uF
DC +5V
DC GND
TGS820
33K
10K
10K
150pF
10K
100nF
ADC0804
5V
10K
10uF
5V
KEYPAD
AT89S52
33pF
33pF
12 Mhz
5V
10K
5V
10K
LCD M1632
ULN2003
12V
Fan 12V
Sensor
Motor
Solenoid
Pompa
220V AC

2003 THRU 2024

Data Sheet 29304F

HIGH-VOLTAGE, HIGH-CURRENT DARLINGTON ARRAYS



Dwg. No. A-9554

Note that the ULN20xxA series (dual in-line package) and ULN20xxL series (small-outline IC package) are electrically identical and share a common terminal number assignment.

ABSOLUTE MAXIMUM RATINGS

Output Voltage, V_{CE}
(ULN200xA and ULN200xL) ..... **50 V**
(ULN202xA and ULN202xL) ..... **95 V**
Input Voltage, V_{IN} ..... **30 V**
Continuous Output Current,
I_C ..... **500 mA**
Continuous Input Current, I_{IN} ..... **25 mA**
Power Dissipation, P_D
(one Darlington pair) ..... **1.0 W**
(total package) ..... **See Graph**
Operating Temperature Range,
T_A ..... **-20°C to +85°C**
Storage Temperature Range,
T_S ..... **-55°C to +150°C**

Ideally suited for interfacing between low-level logic circuitry and multiple peripheral power loads, the Series ULN20xxA/L high-voltage, high-current Darlington arrays feature continuous load current ratings to 500 mA for each of the seven drivers. At an appropriate duty cycle depending on ambient temperature and number of drivers turned ON simultaneously, typical power loads totaling over 230 W (350 mA x 7, 95 V) can be controlled. Typical loads include relays, solenoids, stepping motors, magnetic print hammers, multiplexed LED and incandescent displays, and heaters. All devices feature open-collector outputs with integral clamp diodes.

The ULN2003A/L and ULN2023A/L have series input resistors selected for operation directly with 5 V TTL or CMOS. These devices will handle numerous interface needs — particularly those beyond the capabilities of standard logic buffers.

The ULN2004A/L and ULN2024A/L have series input resistors for operation directly from 6 to 15 V CMOS or PMOS logic outputs.

The ULN2003A/L and ULN2004A/L are the standard Darlington arrays. The outputs are capable of sinking 500 mA and will withstand at least 50 V in the OFF state. Outputs may be paralleled for higher load current capability. The ULN2023A/L and ULN2024A/L will withstand 95 V in the OFF state.

These Darlington arrays are furnished in 16-pin dual in-line plastic packages (suffix "A") and 16-lead surface-mountable SOICs (suffix "L"). All devices are pinned with outputs opposite inputs to facilitate ease of circuit board layout. All devices are rated for operation over the temperature range of -20°C to +85°C. Most (see matrix, next page) are also available for operation to -40°C; to order, change the prefix from "ULN" to "ULQ".

FEATURES

- TTL, DTL, PMOS, or CMOS-Compatible Inputs
- Output Current to 500 mA
- Output Voltage to 95 V
- Transient-Protected Outputs
- Dual In-Line Plastic Package or Small-Outline IC Package

x = digit to identify specific device. Characteristic shown applies to family of devices with remaining digits as shown. See matrix on next page.

2003 THRU 2024
HIGH-VOLTAGE, HIGH-CURRENT DARLINGTON ARRAYS

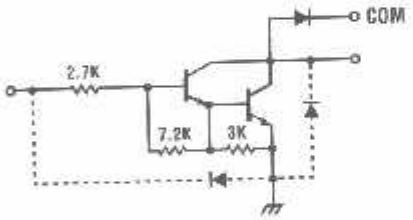
DEVICE PART NUMBER DESIGNATION

$V_{CE(MAX)}$	50 V	95 V
$I_{C(MAX)}$	500 mA	500 mA
Logic	**Part Number**	
5V TTL, CMOS	ULN2003A* ULN2003L*	ULN2023A* ULN2023L
6-15 V CMOS, PMOS	ULN2004A* ULN2004L*	ULN2024A ULN2024L

*Also available for operation between -40°C and +85°C. To order, change prefix from "ULN" to "ULQ".

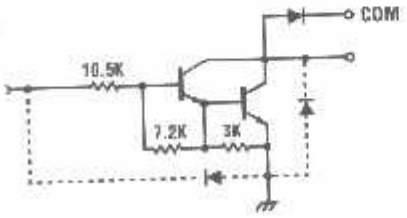
PARTIAL SCHEMATICS

ULN20x3A/L (Each Driver)

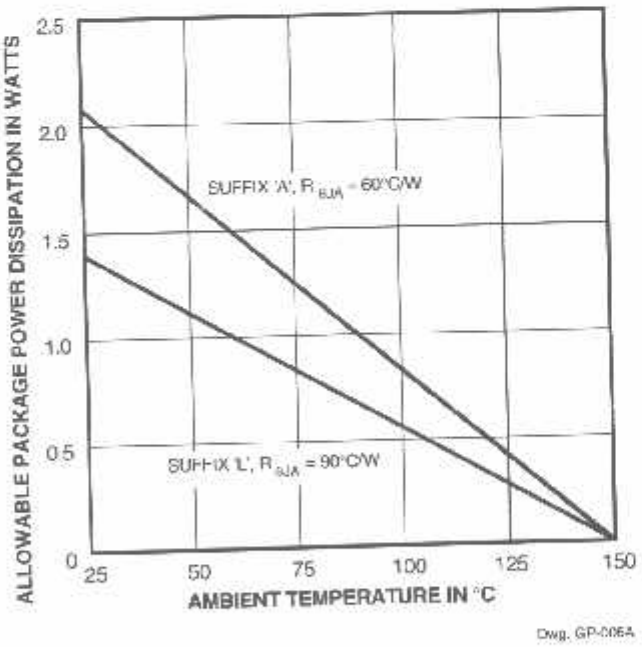


Dwg. No. A-9851

ULN20x4A/L (Each Driver)



Dwg. No. A-9898A



Dwg. GP-006A

X = Digit to identify specific device. Specification shown applies to family of devices with remaining digits as shown. See matrix above.

Allegro MicroSystems, Inc.
115 Northeast Cutoff, Box 15036
Worcester, Massachusetts 01615-0036 (508) 853-5000

Types ULN2003A, ULN2003L, ULN2004A, and ULN2004L
ELECTRICAL CHARACTERISTICS at +25°C (unless otherwise noted).

Characteristic	Symbol	Test Fig.	Applicable Devices	Test Conditions	Limits			
					Min.	Typ.	Max.	Units
Output Leakage Current	I_{CEX}	1A	All	V_{CE} = 50 V, T_A = 25°C	—	< 1	50	µA
				V_{CE} = 50 V, T_A = 70°C	—	< 1	100	µA
		1B	ULN2004A/L	V_{CE} = 50 V, T_A = 70°C, V_{IN} = 1.0 V	—	< 5	500	µA
Collector-Emitter Saturation Voltage	$V_{CE(SAT)}$	2	All	I_C = 100 mA, I_B = 250 µA	—	0.9	1.1	V
				I_C = 200 mA, I_B = 350 µA	—	1.1	1.3	V
				I_C = 350 mA, I_B = 500 µA	—	1.3	1.6	V
Input Current	$I_{IN(ON)}$	3	ULN2003A/L	V_{IN} = 3.85 V	—	0.93	1.35	mA
			ULN2004A/L	V_{IN} = 5.0 V	—	0.35	0.5	mA
				V_{IN} = 12 V	—	1.0	1.45	mA
	$I_{IN(OFF)}$	4	All	I_C = 500 µA, T_A = 70°C	50	65	—	µA
Input Voltage	$V_{IN(ON)}$	5	ULN2003A/L	V_{CE} = 2.0 V, I_C = 200 mA	—	—	2.4	V
				V_{CE} = 2.0 V, I_C = 250 mA	—	—	2.7	V
				V_{CE} = 2.0 V, I_C = 300 mA	—	—	3.0	V
			ULN2004A/L	V_{CE} = 2.0 V, I_C = 125 mA	—	—	5.0	V
				V_{CE} = 2.0 V, I_C = 200 mA	—	—	6.0	V
				V_{CE} = 2.0 V, I_C = 275 mA	—	—	7.0	V
				V_{CE} = 2.0 V, I_C = 350 mA	—	—	8.0	V
Input Capacitance	C_{IN}	—	All		—	15	25	pF
Turn-On Delay	t_{PLH}	8	All	0.5 E_{IN} to 0.5 E_{OUT}	—	0.25	1.0	µs
Turn-Off Delay	t_{PHL}	8	All	0.5 E_{IN} to 0.5 E_{OUT}	—	0.25	1.0	µs
Clamp Diode Leakage Current	I_R	6	All	V_R = 50 V, T_A = 25°C	—	—	50	µA
				V_R = 50 V, T_A = 70°C	—	—	100	µA
Clamp Diode Forward Voltage	V_F	7	All	I_F = 350 mA	—	1.7	2.0	V

Complete part number includes suffix to identify package style: A = DIP, L = SOIC.

003 THRU 2024
HIGH-VOLTAGE, HIGH-CURRENT DARLINGTON ARRAYS

pes ULN2023A, ULN2023L, ULN2024A, and ULN2024L
ECTRICAL CHARACTERISTICS at +25°C (unless otherwise noted).

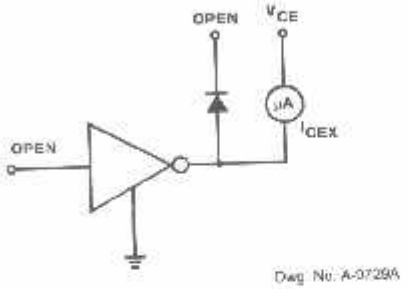
haracteristic	Symbol	Test Fig.	Applicable Devices	Test Conditions	Limits Min.	Typ.	Max.	Units
tput Leakage Current	I_{CEX}	1A	All	V_{CE} = 95 V, T_A = 25°C	—	< 1	50	µA
				V_{CE} = 95 V, T_A = 70°C	—	< 1	100	µA
		1B	ULN2024A/L	V_{CE} = 95 V, T_A = 70°C, V_{IN} = 1.0 V	—	< 5	500	µA
llector-Emitter turation Voltage	$V_{CE(SAT)}$	2	All	I_C = 100 mA, I_B = 250 µA	—	0.9	1.1	V
				I_C = 200 mA, I_B = 350 µA	—	1.1	1.3	V
				I_C = 350 mA, I_B = 500 µA	—	1.3	1.6	V
ut Current	$I_{IN(ON)}$	3	ULN2023A/L	V_{IN} = 3.85 V	—	0.93	1.35	mA
			ULN2024A/L	V_{IN} = 5.0 V	—	0.35	0.5	mA
				V_{IN} = 12 V	—	1.0	1.45	mA
	$I_{IN(OFF)}$	4	All	I_C = 500 µA, T_A = 70°C	50	65	—	µA
ut Voltage	$V_{IN(ON)}$	5	ULN2023A/L	V_{CE} = 2.0 V, I_C = 200 mA	—	—	2.4	V
				V_{CE} = 2.0 V, I_C = 250 mA	—	—	2.7	V
				V_{CE} = 2.0 V, I_C = 300 mA	—	—	3.0	V
			ULN2024A/L	V_{CE} = 2.0 V, I_C = 125 mA	—	—	5.0	V
				V_{CE} = 2.0 V, I_C = 200 mA	—	—	6.0	V
				V_{CE} = 2.0 V, I_C = 275 mA	—	—	7.0	V
				V_{CE} = 2.0 V, I_C = 350 mA	—	—	8.0	V
t Capacitance	C_{IN}	—	All		—	15	25	pF
n-On Delay	t_{PLH}	8	All	0.5 E_{IN} to 0.5 E_{OUT}	—	0.25	1.0	µs
n-Off Delay	t_{PHL}	8	All	0.5 E_{IN} to 0.5 E_{OUT}	—	0.25	1.0	µs
mp Diode kage Current	I_R	6	All	V_R = 95 V, T_A = 25°C	—	—	50	µA
				V_R = 95 V, T_A = 70°C	—	—	100	µA
mp Diode ard Voltage	V_F	7	All	I_F = 350 mA	—	1.7	2.0	V

plete part number includes suffix to identify package style: A = DIP, L = SOIC.

Allegro MicroSystems, Inc.
115 Northeast Cutoff, Box 15036
Worcester, Massachusetts 01615-0036 (508) 853-5000

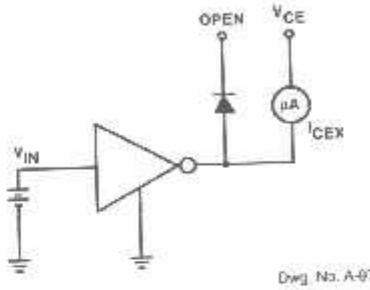
TEST FIGURES

FIGURE 1A



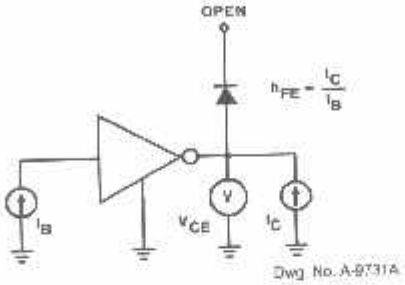
Dwg. No. A-9729A

FIGURE 1B



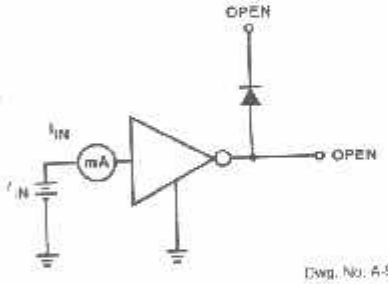
Dwg. No. A-9730A

FIGURE 2



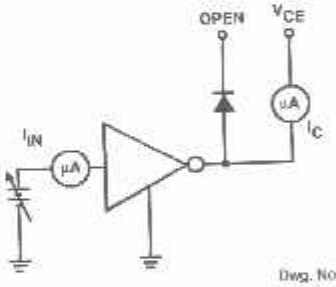
Dwg. No. A-9731A

FIGURE 3



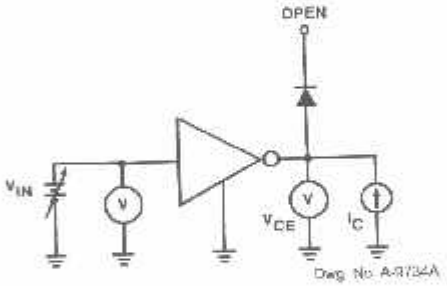
Dwg. No. A-9732A

FIGURE 4



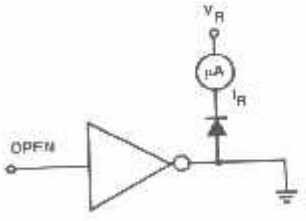
Dwg. No. A-9733A

FIGURE 5



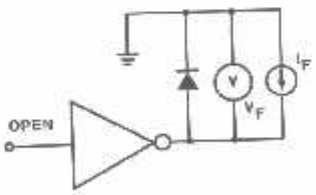
Dwg. No. A-9734A

FIGURE 6



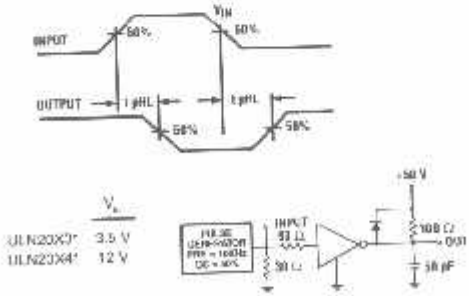
Dwg. No. A-9735A

FIGURE 7



Dwg. No. A-9736A

FIGURE 8



*Complete part number includes a final letter to indicate package.

*Digit to identify specific device. Specification shown applies to family of devices with remaining digits as shown.

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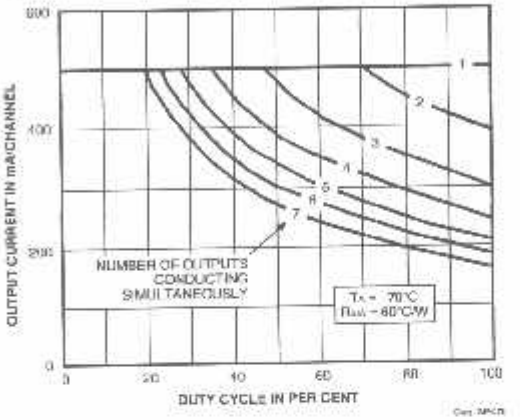
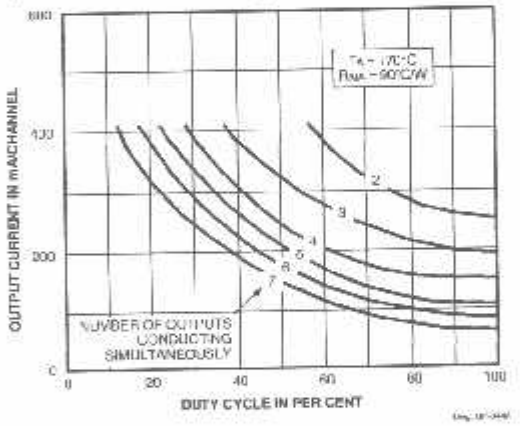
HIGH-VOLTAGE, HIGH-CURRENT DARLINGTON ARRAYS

ALLOWABLE COLLECTOR CURRENT AS A FUNCTION OF DUTY CYCLE

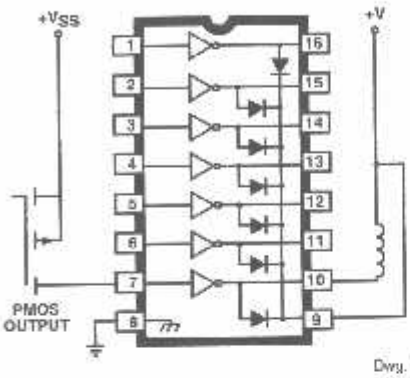
(Dual In-line-Packaged Devices, Suffix 'A')



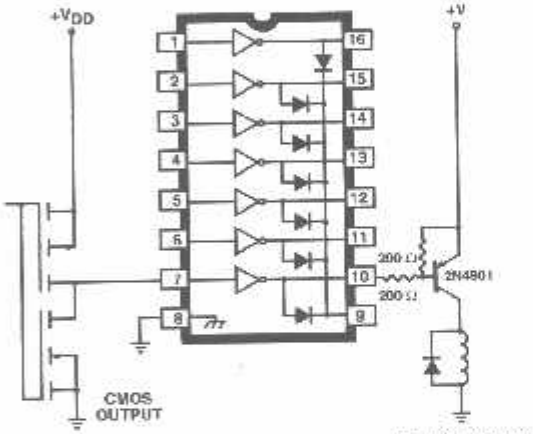
(Small-Outline-Packaged Devices, Suffix 'L')



TYPICAL APPLICATIONS

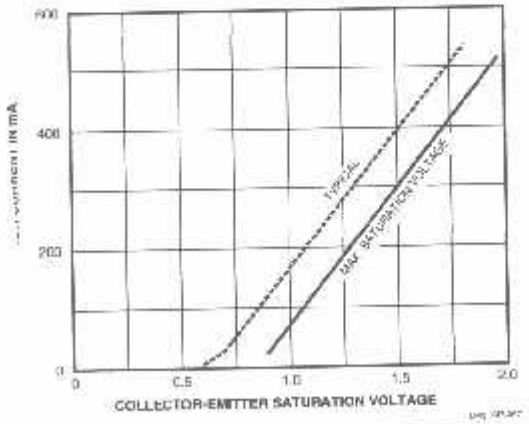


Dwg. No. A-9652

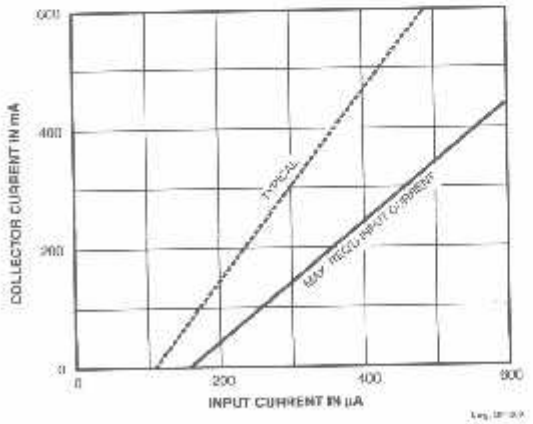


Dwg. No. A-9654A

SATURATION VOLTAGE A FUNCTION OF COLLECTOR CURRENT



COLLECTOR CURRENT AS A FUNCTION OF INPUT CURRENT



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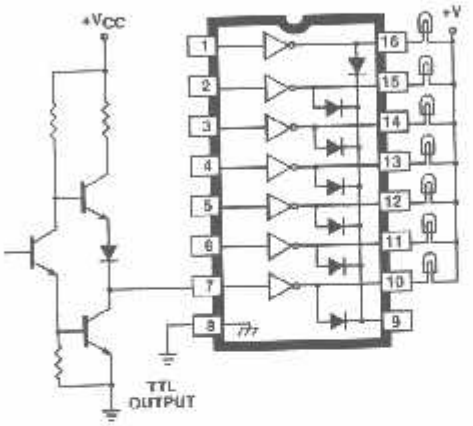
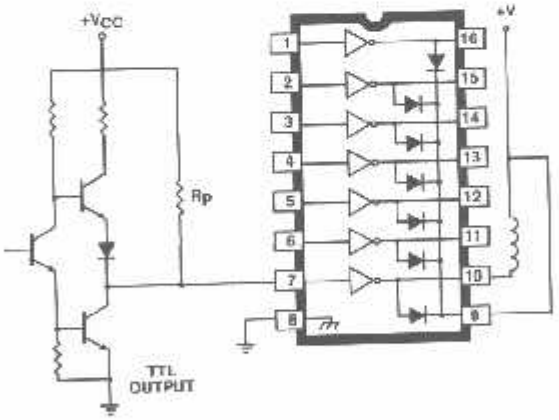
Worcester, Massachusetts 01615-0036 (508) 853-5000

TYPICAL APPLICATIONS



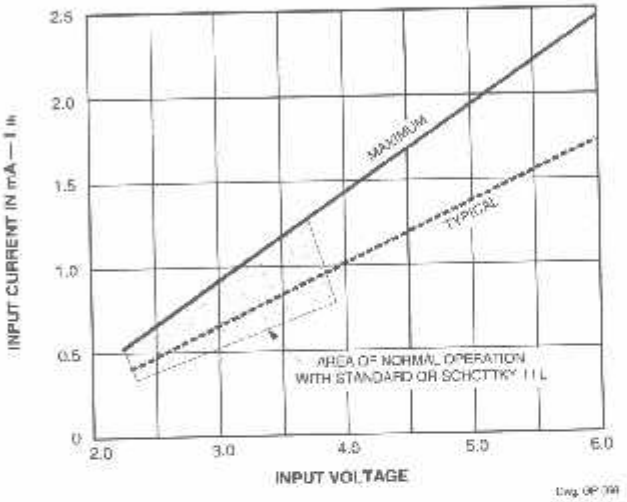
Dwg. No. A-9853A



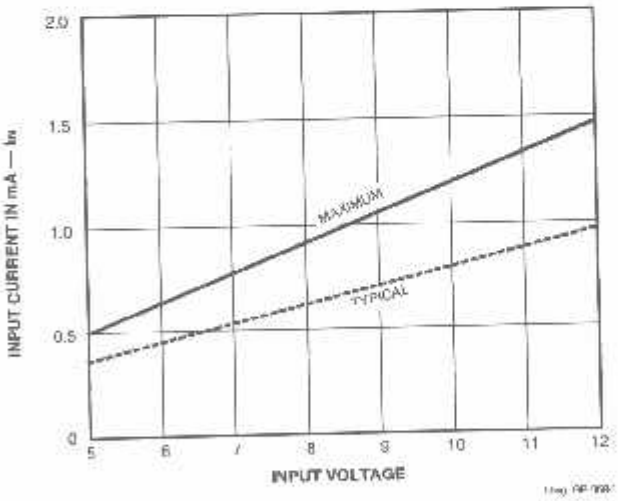
Dwg. No. A-10,175

INPUT CURRENT AS A FUNCTION OF INPUT VOLTAGE

Types ULN2003A, ULN2003L, ULN2023A, and ULN2023L

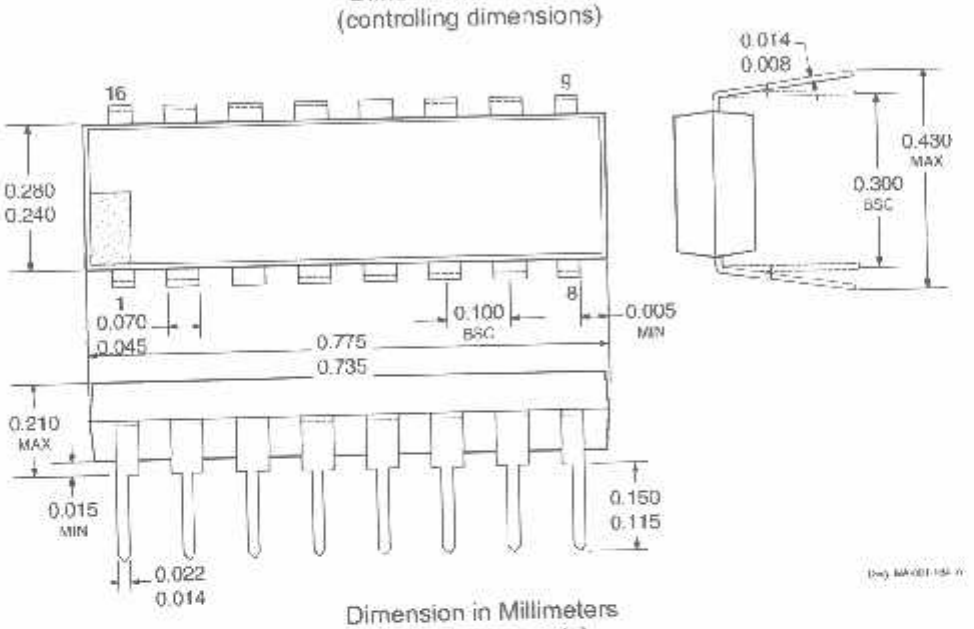


Types ULN2004A, ULN2004L, ULN2024A, and ULN2024L

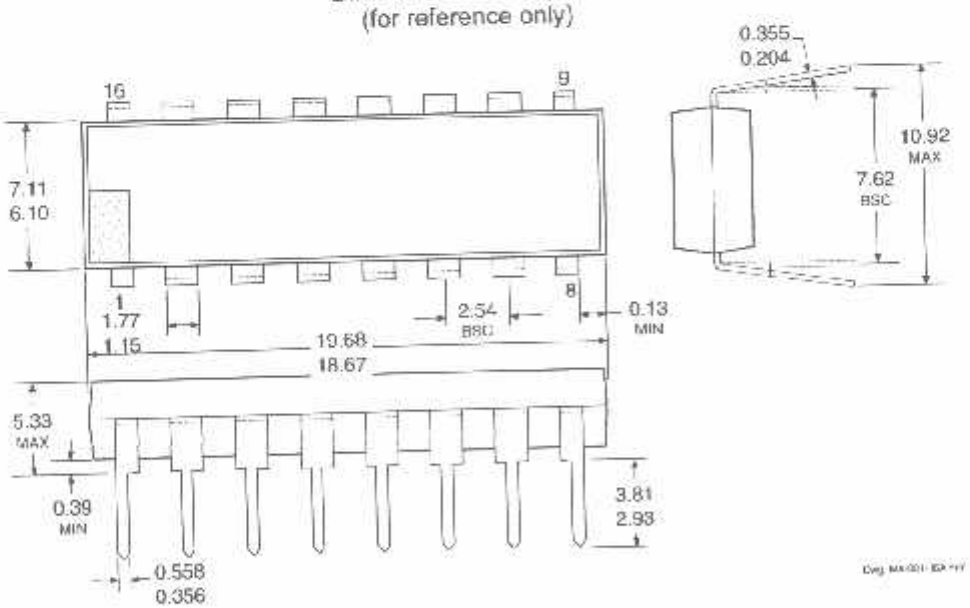


PACKAGE DESIGNATOR "A"

Dimensions in Inches
(controlling dimensions)



Dimension in Millimeters
(for reference only)



Notes: 1. Leads 1, 8, 9, and 16 may be half leads at vendor's option.
2. Lead thickness is measured at seating plane or below.
3. Lead spacing tolerance is non-cumulative.
4. Exact body and lead configuration at vendor's option within limits shown.

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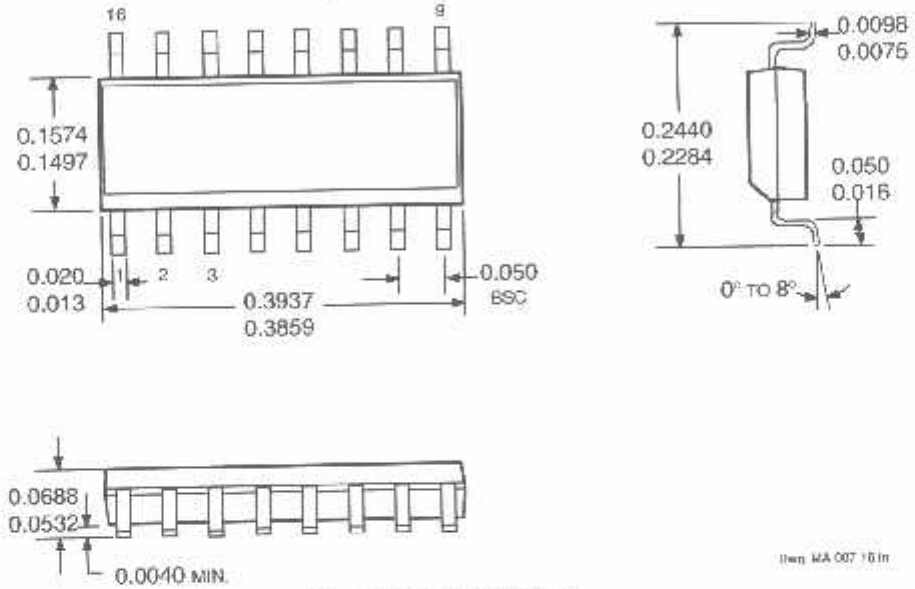
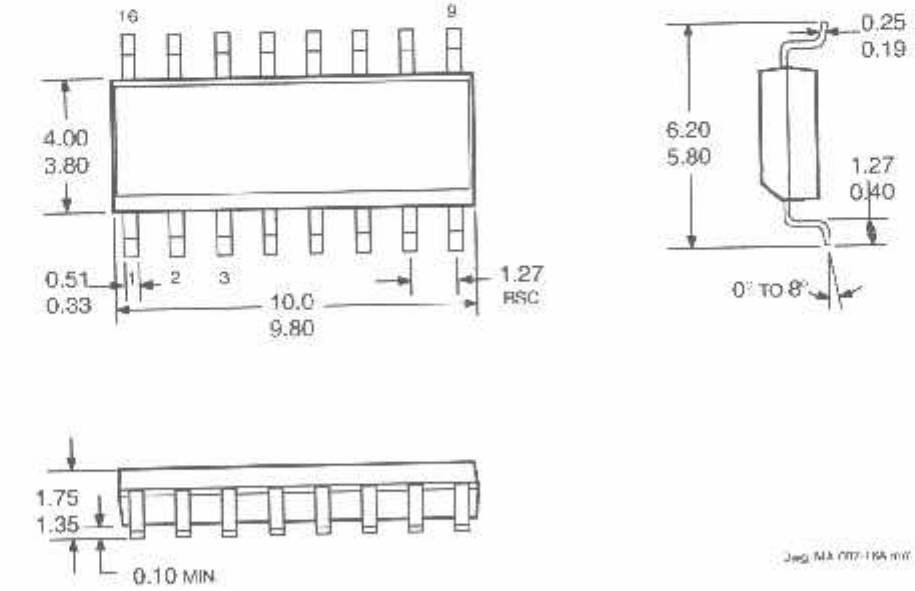
PACKAGE DESIGNATOR "L"

Dimensions in Inches
(for reference only)



Dimension in Millimeters
(controlling dimensions)



NOTES: 1. Lead spacing tolerance is non-cumulative.
2. Exact body and lead configuration at vendor's option within limits shown.

2003 THRU 2024
HIGH-VOLTAGE, HIGH-CURRENT DARLINGTON ARRAYS

The products described here are manufactured under one or more U.S. patents or U.S. patents pending.

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Allegro products are not authorized for use as critical components in life support devices or systems without express written approval.

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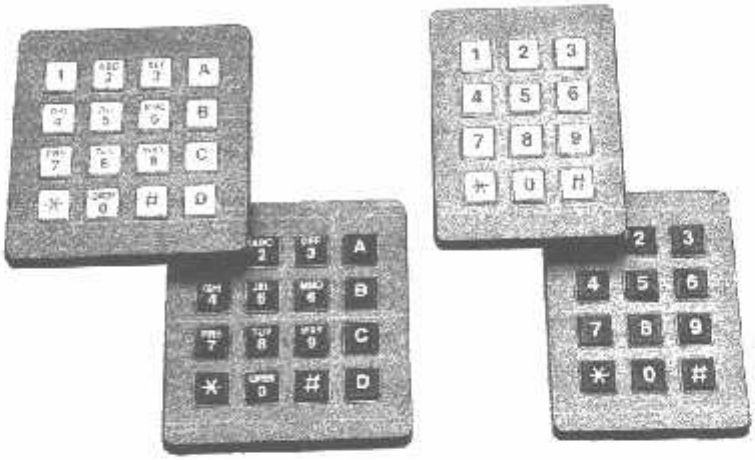
SERIES 96
Conductive Rubber

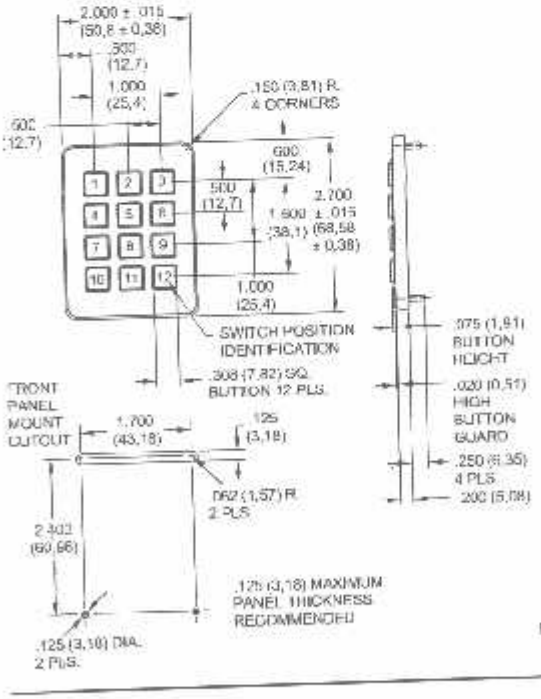
FEATURES
- Quality, Economical Keyboards
- Easily Customized Legends
- Matrix Circuitry
- Backlit and Shielded Options Available
- Termination Mates With Standard Connectors
- Tactile Feedback to Operator
- 1,000,000 Operations per Button
- Compatible With High Resistance Logic Inputs



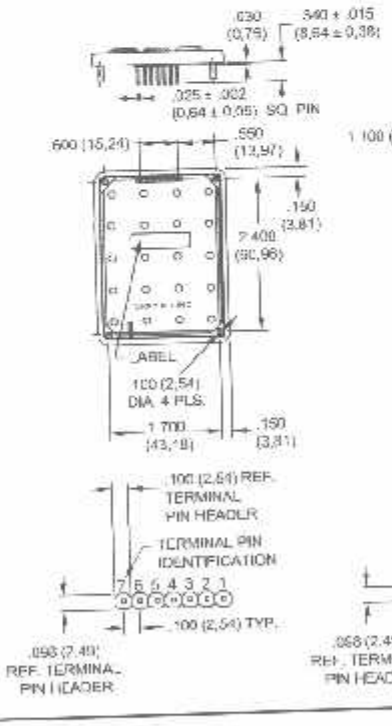
The Series 96 is Grayhill's most economical 3x4 and 4x4 keypad family. The contact system utilizes conductive rubber to mate the appropriate PC board traces. Offered in matrix circuitry, with shielded and backlit options. Built with quality component parts, the Series 96 is subjected to our rigid statistical process control to insure that it meets our reliability standards.

DIMENSIONS In inches (and millimeters)

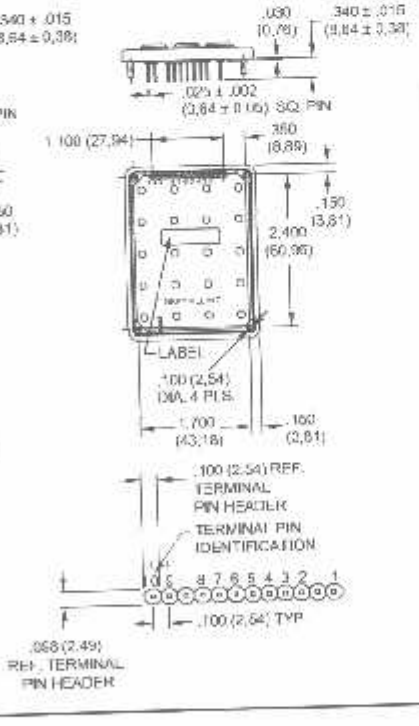
3x4 Front Mount Keyboard



Standard Versions

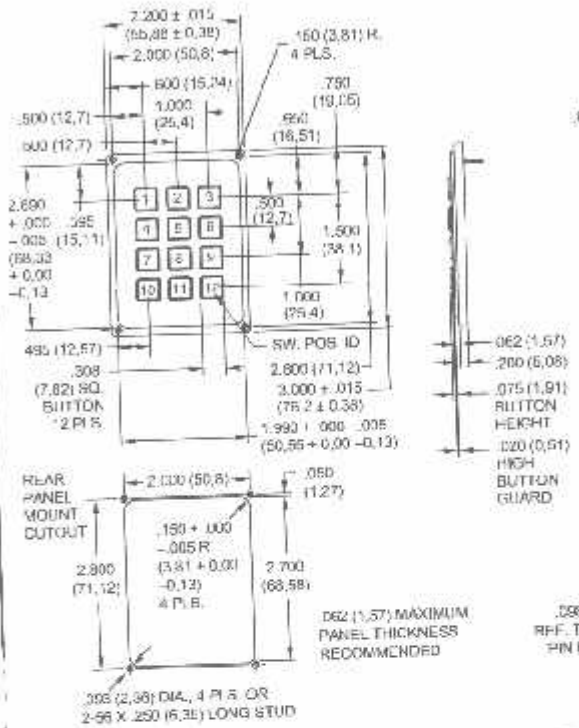


Shielded/Backlit Versions

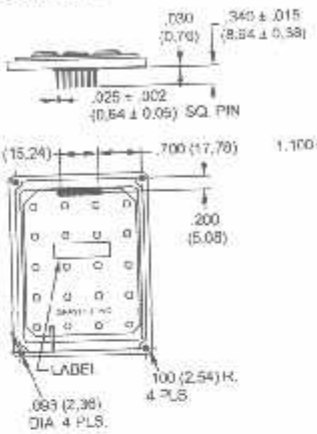


DIMENSIONS In inches (and millimeters)

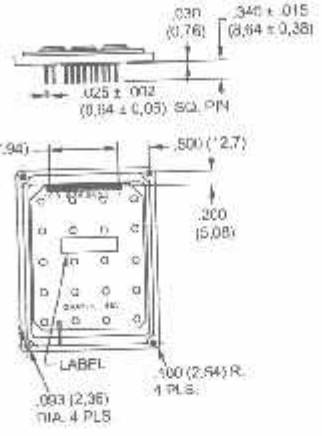
3x4 Rear Mount Keyboard



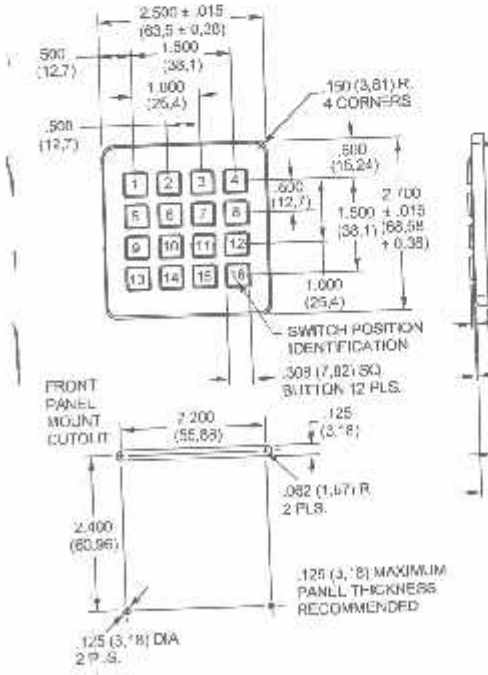
Standard Versions



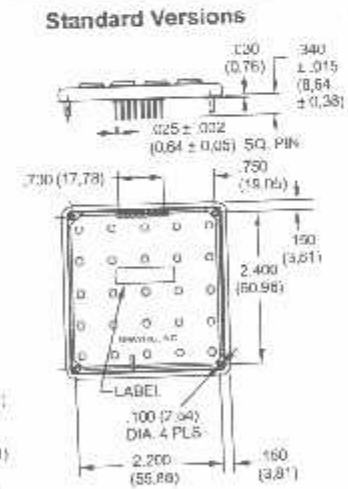
Shielded/Backlit Versions



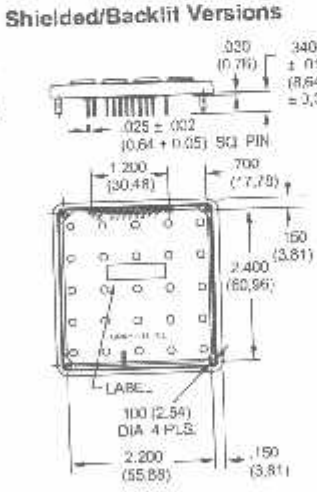
4x4 Front Mount Keyboard



Standard Versions

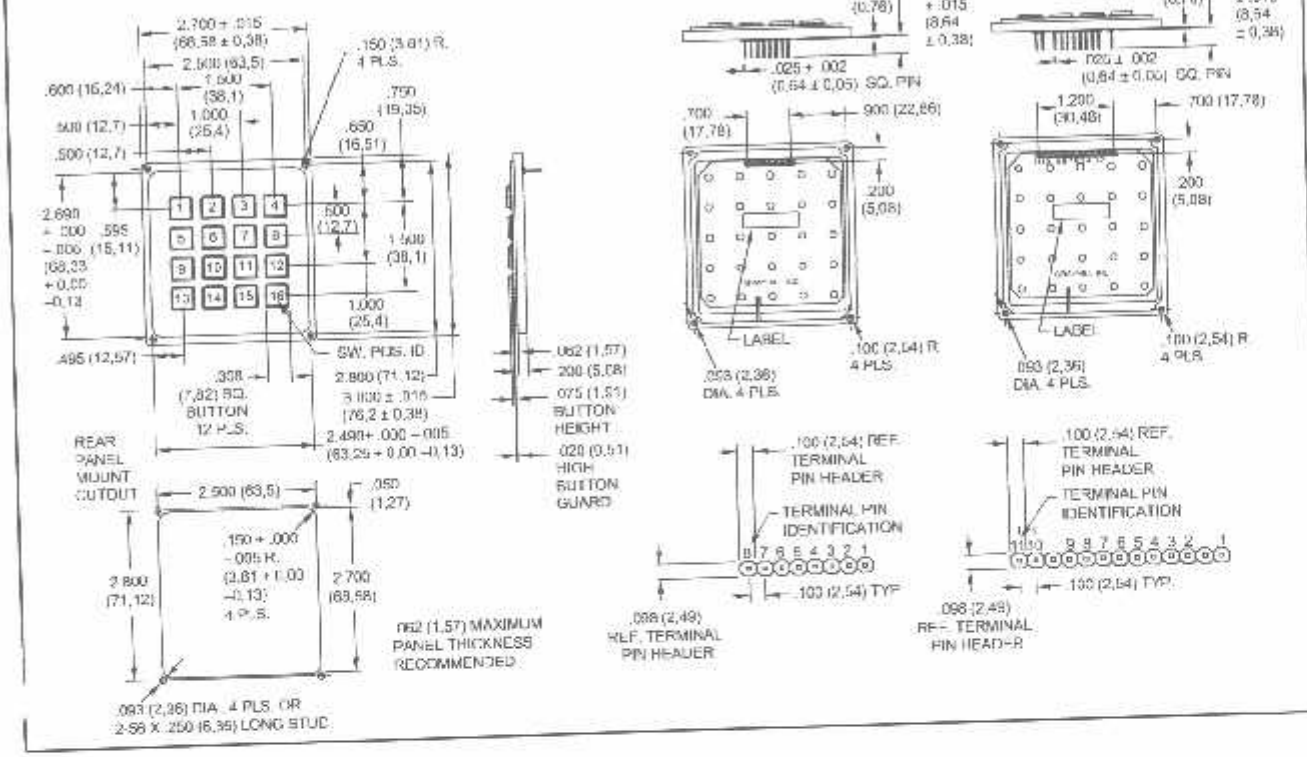


Shielded/Backlit Versions



DIMENSIONS In inches (and millimeters)

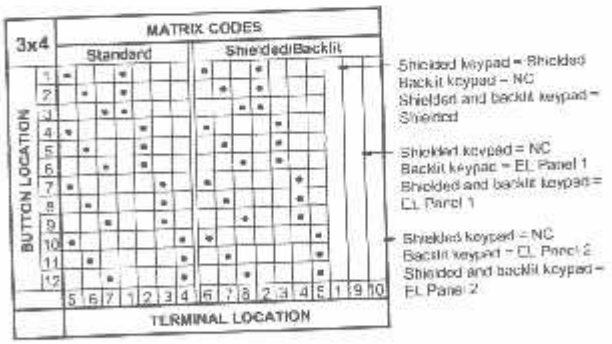
4x4 Rear Mount Keyboard



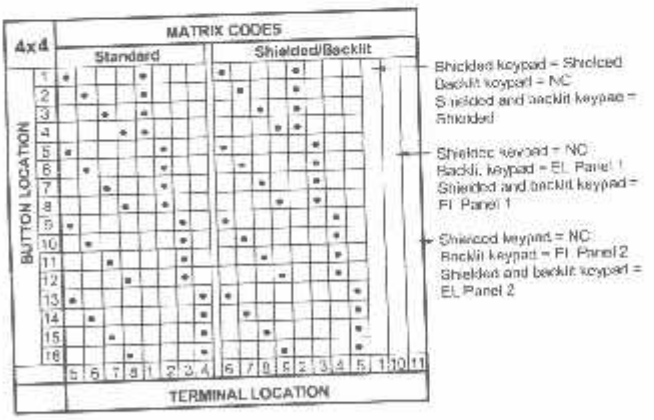
CODE AND TRUTH TABLES

Dots in the chart indicate connected terminals when switch is closed.
Terminals are identified on the keyboard.

12 Button Keypads



16 Button Keypads



SPECIFICATIONS

Rating Criteria

Rating at 12 Vdc: 5 milliamps for .5 seconds
Contact Bounce: < 12 milliseconds
Contact Resistance: < 100 ohms (at stated operating force)
Voltage Breakdown: 250 Vac between components
Mechanical Operation Life: 1,000,000 operations per key
Insulation Resistance: > 10^{12} ohms @ 500 Vdc
Push Out Force Per Pin: 5 lbs.

Operating Features

Travel: .040 minimum
Operating Force: 175 ± 40 grams
Operating Temperature: -30°C to +80°C

Material and Finishes

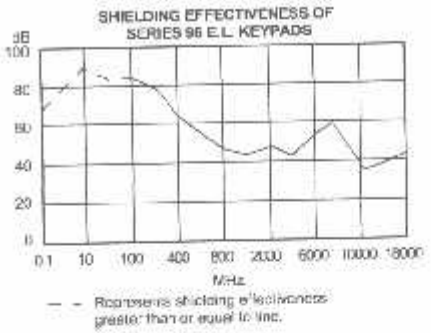
Terminal Pin: Phosphor bronze, solder-plated
PC Board: FR-4 glass cloth epoxy
Keypad: Silicone rubber, durometer 50 ± 5
Housing: ABS, cycolac "KJW"
Housing Color: Black

Shielding Effectiveness

Results shown are typical for a standard Grayhill Series 84S keyboard. A conductive gasket will generally increase the shielding, depending on the size and shape of the gasket and its material. Data derived for E-Field Radiation.

Test Method:
Measurements were made with the keyboard mounted to a brass plate, which in turn was mounted to a shielded enclosure containing the receiving equipment. A signal generator provided the frequency source that was radiated from the transmitting antenna to the enclosed receiving antenna. The spacing between antennas was maintained constant throughout the frequency range. The effectiveness rating is determined by establishing a reference reading without obstruction between the two antennas and determining the difference between that reading and the test setup reading.

Note:
When measured in actual equipment, shielding effectiveness is determined by many factors. This method accurately represents the shielding effectiveness of the Grayhill Series 84S under ideal test conditions.

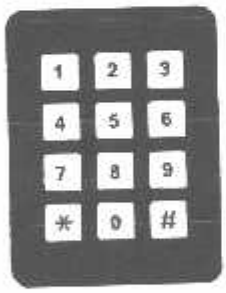


Frequency M Hz	Rating in dB
0.1	≥ 66.2
10	≥ 94.8
100	90.5
400	64.2
800	42.3
2,000	40.5
6,000	33.1
10,000	34.4
18,000	37.0

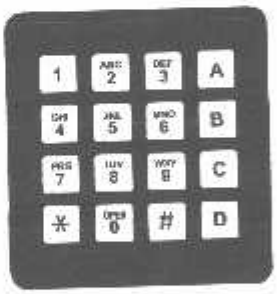
STANDARD LEGENDS

Available through Grayhill Distributors

To order one of the configurations below, use the dash number shown here; select the keypad size and code, and order the part number with the appropriate legend dash number.



-102



-006

-152

-056

ORDERING INFORMATION

96AB2-102-FS-EL

Grayhill Series Number
Keyboard Size: A = 3x4, B = 4x4
Circuitry: B2 = Matrix (terminal pin header)

E.L. Panel Backlighting Option
EL = Backlit, Blank = Non-backlit
EMI/RFI Shielding Option
S = Shielded, Blank = Non-shielded
Mounting Option: F = Front panel mount, R = Rear panel mount
Standard Legend Choices
12 Position legends
102 = Black legends on a white button
152 = White legends on a black button
16 Position legends
006 = Black legends on a white button
056 = White legends on a black button

Available from your local Grayhill Distributor.
For prices and discounts, contact a local Sales Office, an authorized local Distributor or Grayhill.

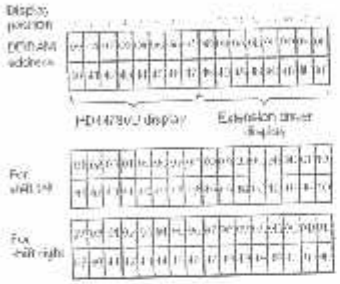
M1632 MODULE LCD 16 X 2 BARIS (M1632)

Deskripsi:

M1632 adalah merupakan modul LCD dengan tampilan 16 x 2 baris dengan konsumsi daya y rendah. Modul ini dilengkapi dengan mikrokontroler yang didisain khusus untuk mengendalikan LC Mikrokontroler HD44780 buatan Hitachi yang berfungsi sebagai pengendali LCD ini mempunyai CGR (Character Generator Read Only Memory), CGRAM (Character Generator Random Access Memory) DDRAM (Display Data Random Access Memory).

DDRAM

DDRAM adalah merupakan memori tempat karakter yang ditampilkan berada. Contoh, ur karakter 'A' atau 41H yang ditulis pada alamat 00, maka karakter tersebut akan tampil pada baris pert dan kolom pertama dari LCD. Apabila karakter tersebut ditulis di alamat 40, maka karakter tersebut a tampil pada baris kedua kolom pertama dari LCD.



Gambar 1
DDRAM M1632 (diambil dari data sheet HD44780)

CGRAM

CGRAM adalah merupakan memori untuk menggambarkan pola sebuah karakter di m bentuk dari karakter dapat diubah-ubah sesuai keinginan. Namun memori ini akan hilang saat power sup tidak aktif, sehingga pola karakter akan hilang.

CGROM

CGROM adalah merupakan memori untuk menggambarkan pola sebuah karakter di mana p tersebut sudah ditentukan secara permanen dari HD44780 sehingga pengguna tidak dapat mengubah l Namun karena ROM bersifat permanen, maka pola karakter tersebut tidak akan hilang walaupun pr supply tidak aktif.

Pada gambar 2, tampak terlihat pola-pola karakter yang tersimpan dalam lokasi lokasi tert dalam CGROM. Pada saat HD44780 akan menampilkan data 41H yang tersimpan pada DDRAM, m HD44780 akan mengambil data di alamat 41H (0100 0001) yang ada pada CGROM yaitu pola karakter '