INSTITUT TEKNOLOGI NASIONAL MALANG
FAKULTAS TEKNOLOGI INDUSTRI
JURUSAN TEKNIK ELEKTRO S-1
KONSENTRASI ELEKTRONIKA

PERENCANAAN DAN PEMBUATAN ALAT PENGONTROL LAMPU OTOMATIS BERDASARKAN KONDISI CAHAYA BERBASIS MIKROKONTROLER AT89S51

SKRIPSI

Disusun Oleh :
R. YUNRI PUTRA ALYADI
98.17.035

OKTOBER 2005

LEMBAR PENGESAHAN

PERENCANAAN DAN PEMBUATAN ALAT PENGONTROL LAMPU OTOMATIS BERDASARKAN KONDISI CAHAYA BERBASIS MIKROKONTROLER AT89S51

SKRIPSI

Disusun dan Diajukan untuk Melengkapi dan Memenuhi Syarat Guna Mencapai Gelar Strata 1 (S-1) Sarjana Teknik

Disusun oleh :

R. YUNRI PUTRA ALYADI
98.17.035

Mengetahui,
Ketua Jurusan Teknik Elektro

(Ir. F. Yudi Limpraptono, MT)
NIP. 103 950 0274

Diperiksa dan Disetujui,
Dosen Pembimbing

(Ir. Widodo Pudji M, MT)
NIP.P 102 870 0171

KONSENTRASI TEKNIK ELEKTRONIKA S-1
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BERITA ACARA UJIAN SKRIPSI
FAKULTAS TEKNOLOGI INDUSTRI

1. Nama Mahasiswa : R. Yunri Putra Alyadi
2. NIM : 98.17.035
3. Jurusan : Teknik Elektro S-1
4. Konsentrasi : Teknik Elektronika
5. Judul Skripsi : Perencanaan dan Pembuatan Alat Pengontrol Lampu Otomatis Berdasarkan Kondisi Cahaya Berbasis Mikrokontroler AT89S51

Dipertahankan dihadapan Tim Penguji Skripsi Jenjang Strata Satu (S-1) pada :

Hari : Jumat
Tanggal : 7 Oktober 2005
Dengan Nilai : B+
76,25 (tujuh puluh enam koma dua puluh lima)

Panitia Ujian Skripsi

Ketua Majelis Penguji	Sekretaris Majelis Penguji
(Ir. Mochtar Asroni, MSME.)	(Ir. F. Yudi Limpraptono, MT.)
NIP. Y.101 8100 036	NIP. Y.103 9500 247

Anggota Penguji

Penguji I	Penguji II
(Ir. F. Yudi Limpraptono, MT.)	(Irmalia Suryani F, ST.)
NIP. Y.103 9500 247	NIP. 103 0100 365

KATA PENGANTAR

T Maha Besar Θ Allah s.w.t., Dzat Yang Kekal dan Penguasa segala sesuatu yang ada dilangit dan dibumi, hanya kepada-Nyalah penulis serahkan seluruh jiwa-raga, hidup dan mati. Hanya Θ Allah s.w.t.-lah yang telah berandil besar dalam proses penyelesaian skripsi ini. Betapapun usaha dan kerja keras yang telah dilakukan hanyalah faktor pendukung yang memang seharusnya dilakukan sebagai realisasi ikhtiar. Sholawat dan salam selalu penulis haturkan kepada junjungan kita, nabi besar B Muhammad 'Rasulullah' ρ s.a.w. yang telah memberikan *'uswatun hasanah'*, suri tauladan yang baik kepada seluruh umat manusia.

Alhamdulillah, puji syukur hanya kepada Θ Allah s.w.t. yang telah membuka hati pihak-pihak berikut, sehingga ikhlas memberikan bantuan dalam proses penyelesaian skripsi ini sebagai salah satu syarat untuk menyelesaikan program strata satu (S-1) pada Jurusan Teknik Elektro, Konsentrasi Elektronika, Fakultas Teknologi Industri, Institut Teknologi Nasional Malang.

Atas selesainya tugas akhir ini, penyusun menyampaikan ucapan terimakasih kepada :

1. Bapak Dr. Ir. Abraham Lomi, MSEE, selaku Rektor Institut Teknologi Nasional Malang.
2. Bapak Ir. Mochtar Asroni, MSME, selaku Dekan Fakultas Teknologi Industri, Institut Teknologi Nasional Malang.
3. Bapak Ir. F.Yudi Limpraptono, MT, selaku Ketua Jurusan Teknik Elektro, Institut Teknologi Nasional Malang.
4. Bapak Ir. Widodo Pudji M,MT, selaku dosen pembimbing.

5. Kedua orang tua dan keluarga penulis yang telah banyak membantu dan memberikan do'a restu dalam penyelesaian skripsi ini.
6. Semua pihak yang telah membantu terselesaikannya skripsi ini, yang tidak dapat penulis sebutkan satu per satu.

Penyusun mengharapkan agar yang penyusun lakukan melalui karya ini dapat membantu dan dimanfaatkan oleh siapa saja yang memerlukan dan yang membutuhkannya. Namun adanya kritik dan saran yang membangun lebih diharapkan lagi sehingga karya ini lebih bermanfaat.

Malang, Oktober 2005

Penulis

Lembar Persembahan

Θ

Bismillaahir Rohmaanir Rahiim

Hanya Engkaulah (Allah) yang kami sembah dan hanya kepada Engkaulah (Allah) kami memohon pertolongan.

[*QS. Al – Faatihah, 1 : 5*]

Bacalah (ya Muhammad) dengan (menyebut) nama Tuhanmu (Allah) Yang telah Menciptakan alam semesta. Dialah yang telah Menciptakan manusia dari segumpal darah yang beku. Bacalah!, dan Tuhanmulah Yang Maha Pemurah, Yang Mengajarkan kepada manusia apa yang tidak diketahuinya.

[*QS. Al – 'Alaq, 96 : 1 - 5*]

Adakah orang yang ta'at (patuh kepada Allah) pada waktu malam, seraya sujud dan berdiri, lagi takut akan siksa akhirat, serta mengharap akan rahmat Tuhan (Allah), samakah dengan orang yang durhaka ?. Katakanlah! Apakah sama orang – orang yang berilmu pengetahuan dengan orang – orang yang tiada berilmu pengetahuan ?. (Tentu tidak) . Hanya yang menerima pengajaran yaitu orang – orang yang berakal.

[*QS. Az – Zumar, 39 : 9*]

Segala puji bagi Allah, Dzat yang telah mengkarunia akal dan kecerdasan kepada segenap hamba-Nya. Yang membimbing mereka dengan fitrah dan pengetahuan yang cukup untuk bisa hidup layak dan nyaman.

Maha Suci Allah, Dzat yang telah menciptakan otak manusia mengajarkan ilmu pengetahuan dan teknologi.

Kupersembahkan skripsi ini kepada hamba-hamba Mu, wahai Dzat *Al Malikul Manan* (Maha Berkuasa dan Maha Memberi Karunia) semata-mata karena ketundukanku kepada Mu wahai Tuhanku.

Kupersembahkan skripsi ini kepada orang tuaku sebagai tanda jasa, tanda bakti dan tanda rasa hormat yang mendalam.

Kupersembahkan skripsi ini kepada istri dan anak-anakku, saudara-saudaraku, sahabat-sahabatku dan rekan-rekanku yang telah banyak membantu dalam hal apapun dan dalam bentuk apapun, sebagai ungkapan rasa terima kasih yang sebanyak-banyaknya.

Kupersembahkan skripsiku ini kepadamu saudara-saudaraku kaum muslim agar engkau tau bahwa Allah telah mengaruniakan akal, kecerdasan, kepandaian dan ilmu pengetahuan untuk menguak rahasia alam dan teknologi yang bermanfaat didalam kehidupan manusia yang telah "diciptakan-Nya" dengan kekuasaan, kebijaksanaan dan kasih sayang-Nya.

Semoga ini semua dinilai sebagai salah satu ibadah oleh Allah Ta'alla...

Alhamdulillah, segala puji hanya milik Allah s.w.t. ...

Abstraksi

R.Yunri Putra Alyadi, 2005. **Perencanaan dan Pembuatan Alat Pengontrol Lampu Otomatis Berdasarkan Kondisi Cahaya Berbasis Mikrokontroler AT89S51.** Skripsi. Jurusan Teknik Elektro, Konsentrasi Elektronika, Fakultas Teknologi Industri, Institut Teknologi Nasional Malang.

- Pembimbing : *Ir. Widodo Pudji M, MT.*

Kata kunci : Sensor Cahaya, Keypad, Mikrokontroler, ADC, Driver, RS485, LCD, Buzzer.

Skripsi ini bertujuan untuk merancang dan membuat suatu sistem pengontrol lampu yang terdiri dari pusat kontrol dan unit kontrol yang saling berkomunikasi dengan menggunakan RS485.

Perubahan intensitas cahaya merupakan kondisi yang dideteksi oleh sensor cahaya, data analog yang diperoleh diubah menjadi data digital agar bisa dikenali mikrokontroler yang akan menetapkan keadan lampu pada ruangan. Lampu yang rusak akan mengaktifkan buzzer dan LCD menampilkan posisi lampu yang rusak pada gedung.

Alat pengontrol lampu ini diharapkan dapat mempermudah kerja pihak pengelola gedung dan menjadi fasilitas yang dapat menambah kenyamanan para pengguna ruangan gedung tersebut.

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BAB I
PENDAHULUAN

1. 1. Latar Belakang

Teknologi digunakan untuk membantu pekerjaan manusia, menjadikan suatu pekerjaan lebih mudah dan efisien. Dalam kehidupan sehari-hari, kita secara langsung sudah menikmati hasil dari perkembangan teknologi tersebut. Sebenarnya masih banyak peralatan baik diindustri maupun pada kehidupan sehari-hari yang masih memerlukan sentuhan teknologi agar alat tersebut menjadi lebih praktis dan efisien.

Kalau kita perhatikan dalam kehiduan sehari-hari, kita akan menjumpai suatu hal yang oleh sebagian pihak mungkin dianggap sepele. Tetapi alangkah baiknya dan tidak ada salahnya bila suatu permasalahan tersebut kita berikan sentuhan ataupun polesan yang bersifat elektronik otomatis, sehingga kita akan mendapat kemudahan dan manfaat yang lebih dibanding keadaaan semula yang masih bersifat manual.

Pada kesempatan ini penyusun akan mengangkat suatu ide yaitu system pengontrol lampu otomatis berdasarkan kondisi cahaya yang berfungsi menghidupkan dan mematikan lampu gedung, serta untuk mengetahui lampu yang rusak dengan menerapkan teknologi microcontroller.

1. 2. Rumusan Masalah

Dengan latar belakang tersebut diatas, maka permasalahan dalam perencanaan dan pembuatan alat pengontrol lampu otomatis berdasarkan kondisi cahaya berbasis mikrokontroler ini dapat dirumuskan sebagai berikut :

1. Merancang dan membuat alat pengontrol lampu otomatis berdasarkan kondisi cahaya, menghidupkan dan mematikan lampu serta mengetahui lampu yang rusak berbasis mikrokontroler AT89S51 yang dijadikan sebagai pengontrol utamanya.
2. Merancang dan membuat alat pengontrol lampu otomatis berdasarkan kondisi cahaya, yang dapat menampilkan (men-*display*kan) keadan lampu pada ruangan.
3. Merancang dan membuat pengontrol lampu otomatis berdasarkan kondisi cahaya, yang dijalankan menggunakan perangkat lunak *(software) assembler* sebagai perangkat lunak dalam mikrokontroler.
4. Merancang dan membuat alat pengontrol lampu otomatis berdasarkan kondisi cahaya yang dapat dikontrol dari pusat control dengan memanfaatkan RS485 sebagai jalur komunikasi.

1. 3. Batasan Masalah

Untuk memberikan pembahasan yang jelas maka diberikan ruang lingkup pembatasan masalah sebagai berikut :

1. Perencanaan perangkat keras (hardware) yang meliputi LDR, ADC, RTC, Keypad, LCD, RS485 dan Microcontroller AT89S51.
2. Perencanaan dan pembuatan perangkat lunak (software) untuk Microcontroller AT89S51.
3. Jangkauan jarak antara Pusat control dengan Unit control maksimal sejauh 1200 meter.
4. Dalam pengerjaan skripsi ini menggunakan dibuat model *(prototype)* miniatur untuk dapat menggambarkan keadaan sebenarnya
5. Dalam rangkaian dianggap catu daya konstan dan tidak akan dibahas.

1. 4. Tujuan

Tujuan dari perencanaan dan pembuatan alat pengontrol lampu otomatis berdasarkan kondisi cahaya yaitu untuk mengaplikasikan teknologi microcontroller AT89S51 sebagai suatu system alat menghidupkan, mematikan dan untuk mengetahui lampu yang sudah rusak pada system penerangan gedung.

1. 5. Metodologi

Untuk mencapai tujuan dari skripsi ini, maka metodologi dalam skripsi ini adalah sebagai berikut :

a. Studi literatur *(library research)*

Yaitu memperoleh data dengan cara membaca dan mempelajari buku literatur/referensi yang ada hubungannya dengan penyusunan skripsi ini yang mencakup prinsip kerja dan kajian teori antara lain mempelajari hal-hal yang berhubungan dengan teori dan rangkaian pendukung dalam perancangan dan pembuatan alat ini.

b. Studi lapangan

Yaitu memperoleh data dengan cara mengamati, meneliti dan menganalisa kondisi sebenarnya yang ada di lapangan.

c. Perencanaan dan pembuatan perangkat keras *(hardware)* dan perangkat lunak *(software)*.

Proses perancangan alat meliputi pembuatan blok diagram lengkap alat yang dirancang, penentuan komponen-komponen yang digunakan kemudian membuat diagram skematik dari rangkaiannya dan merancang diagram alir *(flow chart)* dari perangkat lunaknya.

Proses pembuatan alat meliputi pembuatan papan sirkuit cetak/PCB *(Printed Circuit Board)* dari diagram skematik rangkaian yang telah dirancang, perakitan komponen-komponen pada PCB serta penyolderan beserta instalasi pengkabelannya dan pengisian *(download)* perangkat lunak kedalam keping tunggal.

d. Pengujian dan analisa alat yang dibuat

Untuk mengetahui rangkaian dapat bekerja sesuai dengan yang diharapkan perlu dilakukan pengujian alat. Pengujian yang dilakukan meliputi: pengujian rangkaian per bagian dan pengujian rangkaian secara keseluruhan.

e. Penyusunan laporan skripsi

Yaitu melakukan penulisan dari seluruh langkah-langkah penyusunan skripsi ini mulai dari perencanaan, penelitian, pembuatan, pengujian, analisa sampai penarikan kesimpulan dari seluruh langkah-langkah yang telah dilakukan.

1. 6. Sistematika Pembahasan

Dalam penyusunan skripsi ini, sistematika pembahasan yang digunakan adalah sebagai beriut :

BAB I PENDAHULUAN

Bab ini membahas mengenai latar belakang, rumusan masalah, batasan masalah, tujuan, metodologi dan sistematika pembahasan.

BAB II LANDASAN TEORI

Bab ini membahas mengenai dasar-dasar teori sebagai teori penunjang pada alat yang akan dirancang. Disamping itu juga sebagai pelengkap pemahaman mengenai bagian-bagian atau keseluruhan sistem.

BAB III PERENCANAAN DAN PEMBUATAN ALAT

Bab ini membahas mengani perencanaan dan pembuatan alat yang terdiri dari perangkat keras *(hardware)* dan perangkat lunak *(software)*

BAB IV PENGUJIAN DAN ANALISA ALAT

Bab ini mengulas tentang hasil pengujian dan analisa alat yang telah dibuat.

BAB V PENUTUP

Bab ini berisikan kesimpulan akhir dari keseluruhan alat yang telah dibuat dan saran dari penyusun demi perkembangan selanjutnya dari alat yang telah dibuat.

BAB II

LANDASAN TEORI

2. 1. Mikrokontroller AT89S51

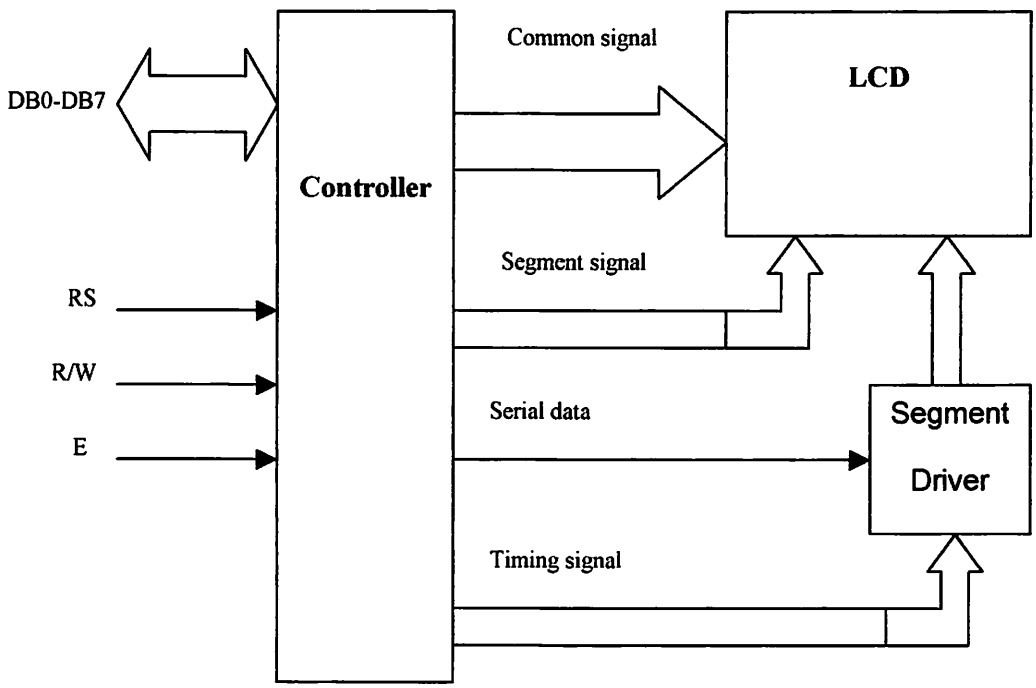
Perbedaaan yang mendasar antara mikrokontroler dan mikroprosesor adalah mikrokontroler selain memiliki CPU *(Central Processing Unit)* juga dilengkapi dengan memori dan port I/O *(Input/Output)* yang merupakan kelengkapan sebagai sistem minimum mikrokomputer sehingga sebuah mikrokontroler dapat dikatakan sebagai mikro komputer dalam keping tunggal *(Single Chip Microcomputer).* Mikroprosesor adalah bagian dari CPU dari sebuah komputer, tanpa memori, tanpa perangkat I/O dan tanpa periferal yang dibutuhkan oleh suatu sistem lengkap. Untuk dapat bekerja, mikroprosesor membutuhkan perangkat pendukung yang dapat berupa RAM *(Random Access Memory),* ROM *(Read Only Memory)* dan perangkat I/O.

Mikrokontroller AT89S51 adalah mikrokontroller keluaran Atmel yang kompatibel penuh dengan mikrokontroler keluarga MCS-51 lainnya. Mikrokontroler AT89S51 merupakan hasil pengembangan dan penyempurnaan dari mikrokontroler AT89C51. Mikrokontroler AT89S51 merupakan CMOS yang mengkonsumsi daya relatif rendah, performa tinggi dan dilengkapi dengan *4K byte Flash PEROM (Programmable and Erasable Read Only Memory)* menggunakan *Atmel's High Density Non Volatile Technology* (memori dengan teknologi *non-volatile*), isi memori tersebut dapat diisi ulang ataupun dihapus sampai dengan 1000 kali proses hapus/tulis.

LCD mempunyai 16 kaki. Fungsi tiap-tiap kaki ditunjukkan dalam tabel berikut:

Tabel 2-7. Fungsi Kaki-Kaki M1632

No	Nama Penyemat	Fungsi
1	Vss	0 V (GND)
2	Vcc	5V ±10%
3	Vee	Drive LCD
4	RS	Pemilih Register 0 = Instruksi register (tulis) Bussy flag dan address counter (baca) 1 = Register data (baca dan tulis)
5	R/W	Sinyal pemilih baca dan tulis 0 = tulis 1 = baca
6	Enable	Sinyal untuk mengawali operasi
7-14	Data Bus	Saluran data
15	V + BL	Pengendali kecerahan latar belakang LCD, 4-4,42 V dan 50-200 mA
16	V – BL	Pengendali kecerahan latar belakang LCD, 0 V



Gambar 2-20. Blok diagram LCD M1632

BAB III

PERANCANGAN DAN PEMBUATAN ALAT

3. 1. Pendahuluan

Dalam bab ini penulis akan mencoba untuk bisa memberikan penjelasan/gambaran tentang fungsi dan cara kerja dari blok-blok atau bagian-bagian yang terdapat pada alat atau *prototype* karya ilmiah ini. Pertama-tama penulis akan memberikan gambaran secara garis besar mengenai sistem dan cara kerja bagian-bagian yang ada pada alat ini.

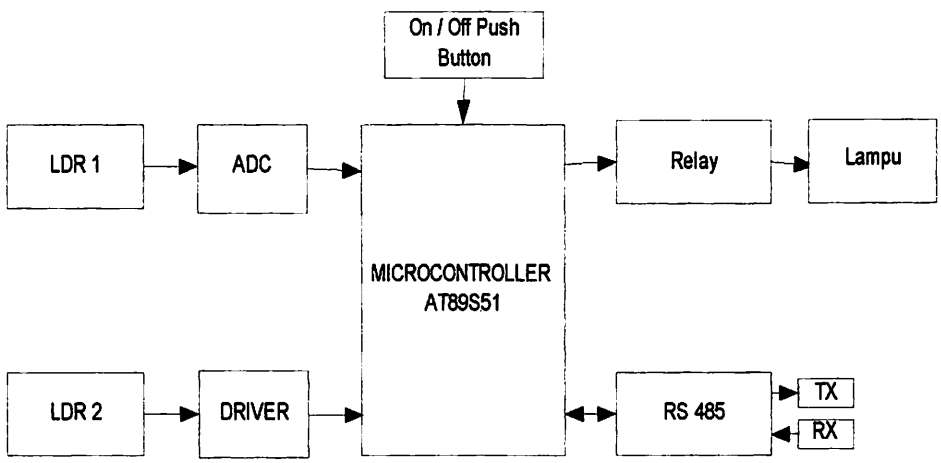
Perancangan secara keseluruhan dapat dibagi menjadi dua bagian, yaitu:

1. Perancangan *hardware.*
2. Perancangan *Software.*

3. 2. Perancangan Hardware

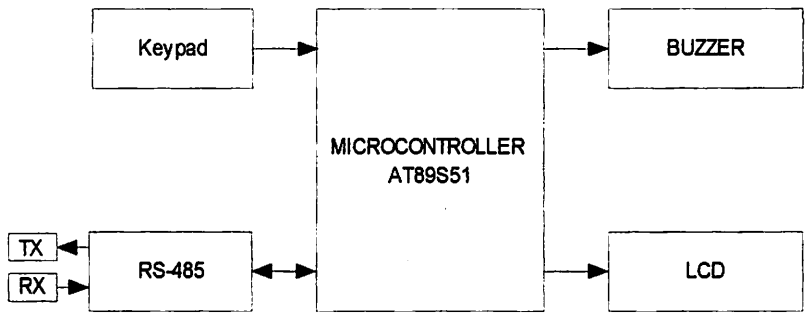
Berikut ini adalah diagram blok dari system rancangan yang dimaksud:

1. Unit Kontrol



Gambar 3-1. Diagram Blok Unit Kontrol

2. Pusat Kontrol



Gambar 3-2. Diagram Blok Pusat Kontrol

Dari blok diagram dapat dijelaskan fungsi masing-masing blok yaitu:

1. Unit Kontrol.

- LDR 1 untuk mendeteksi perubahan cahaya.
- LDR 2 berfungsi mendeteksi lampu yang telah rusak.
- ADC mengubah sinyal analog dari LDR menjadi sinyal digital.
- On/Off Push Button adalah saklar yang terletak pada ruangan untuk menghidupkan dan mematikan lampu.
- Microcontroler AT89S51 sebagai pengolah data masukan dari sensor, saklar dan mengontrol relay serta akan berkomunikasi dengan pusat control.
- Relay berfungsi sebagai pemutus atau penyambung hubungan listrik dengan lampu.
- RS-485 sebagai saluran komunikasi data antara unit control dengan pusat kontrol.

2. Pusat Kontrol.

- Keypad berfungsi untuk memasukan data.
- RS-485 sebagai saluran komuikasi ke unit control untuk mengirim dan menerima data.
- Microcontroler AT89S51 sebagai pengolah data pusat kontrol.
- Buzzer sebagai indicator ada lampu yang rusak.
- LCD berfungsi untuk menampilkan keadaan lampu dan data inputan dari keypad.

Prinsip kerja:

Sensor cahaya yaitu *LDR1* akan mendeteksi kondisi cahaya, gelap atau terang pada ruangan. Kondisi gelap sebagai pemicu *microcontroller unit kontrol* untuk menghidupkan lampu, sebaliknya akan mematikan lampu apabila keadaan ruangan terang.

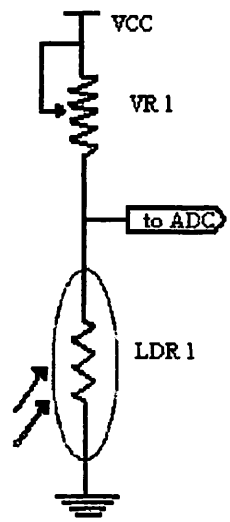
Lampu yang dinyalakan tapi tidak menghasilkan cahaya menyebabkan *LDR2* mendeteksi keadaan ini sebagai putusnya lampu, informasi putusnya lampu akan dikirimkan melalui *RS845* oleh *microcontroller unit* untuk dieksekusi oleh *microcontroller pusat* dengan mengaktifkan *buzzer* dan menampilkan nomor lampu atau ruangan lampu yang putus pada *LCD*, serta mengirim perintah kembali ke *microcontroller unit* agar *relay* memutuskan hubungan lampu ke sumber tegangan.

On/off push button diletakkan pada setiap ruangan, digunakan untuk menyalakan lampu pada saat lampu yang bersangkutan seharusnya padam

keadaan ruangan terang, atau mematikan lampu pada lampu yang seharusnya menyala pada kondisi ruangan gelap.

Keypad berfungsi untuk mengecek keadaan lampu menyala atau padam pada ruangan yang diinginkan dengan menampilkannya pada *LCD*, selain itu *keypad* juga berfungsi sebagai *on/off push button.*

3. 2. 1. Rangkaian Sensor Cahaya



Gambar 3-3. Rangkaian Sensor Cahaya

Untuk sensor cahaya digunakan LDR1 yang dipasang seri dengan VR1, berfungsi sebagai pembagi tegangan. Perubahan intensitas cahaya akan mempengaruhi tingkat resistansi LDR. Semakin tinggi intensitas cahaya yang diterima LDR maka resistansinya akan turun, demikian sebaliknya semakin rendah intensitas cahaya yang diterima LDR maka resistansinya akan naik. Perubahan resitansi LDR pada rangkaian ini akan menghasilkan perubahan level tegangan yang merupakan inputan ADC 0804.

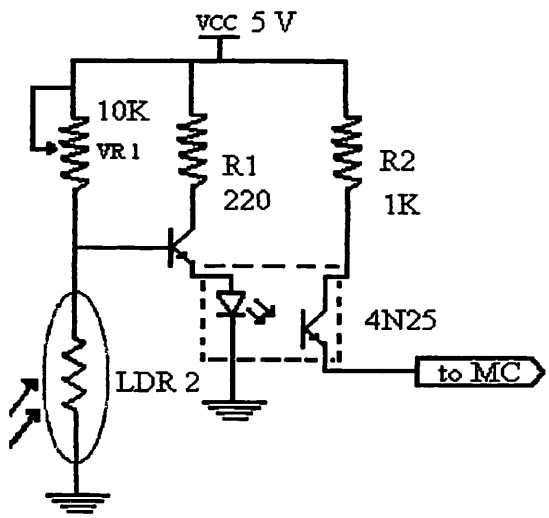
Untuk intensitas cahaya gelap diperoleh resistansi pada LDR sebesar 300 KΩ. Tegangan Output maksimum pada rangkaian sebesar:

$$V_{out} = \frac{R_{LDR}}{R_{LDR} + R_{VR1}} \times Vcc$$

$$V_{out} = \frac{300\ K}{300\ K + 10\ K} \times 5 = 4{,}83\ Volt$$

3. 2. 2. Rangkaian Sensor Lampu

Rangkaian sensor lampu berfungsi untuk mendeteksi keadaan lampu yang telah rusak. Rangkaian ini juga digunakan untuk mengecek keadaan lampu pada tiap ruangan yamg ditampilkan pada LCD pusat control.



Gambar 3-4. Rangkaian Sensor Lampu Rusak

3. 2. 3. Rangkaian ADC

Untuk mengubah level tegangan analog yang keluar dari rangkaian sensor cahaya menjadi level tegangan digital, maka dibutuhkan sebuah pengubah (converter) dari besaran analog menjadi besaran digital berupa ADC. ADC yang digunakan adalah ADC 0804, yang terdiri dari 1 buah input analog dan 8 buah output digital. Input ADC ini kaki pin no.6 berupa tegangan masukan antara 0 sampai 5 Volt yang selanjutnya akan dikonversi menjadi data biner 8-bit ($2^n - 1$) melalui DB0-DB7.

Rangkaian ADC ini dilengkapi dengan tegangan referensi yang berfungsi untuk mendapatkan besarnya nilai resolusi yang diinginkan untuk perubahan tiap bitnya. Untuk menghitung besarnya resolusi tersebut, dapat dihitung dengan menggunakan rumus berikut :

$$\text{Resolusi (R)} = \frac{\text{Vref}}{2^n - 1}, \qquad \text{dimana } n = \text{jumlah bit}$$

Dalam perancangan ini kita menggunakan tegangan referensi (Vref) sebesar 5 Volt, sehingga besarnya resolusi dari A/D Converter adalah :

$$R = \frac{5}{255} = 19{,}6\ \text{mV} \approx 0{,}02\ \text{Volt}$$

Sedangkan untuk menghitung perubahan dari analog ke digital adalah sebagai berikut :

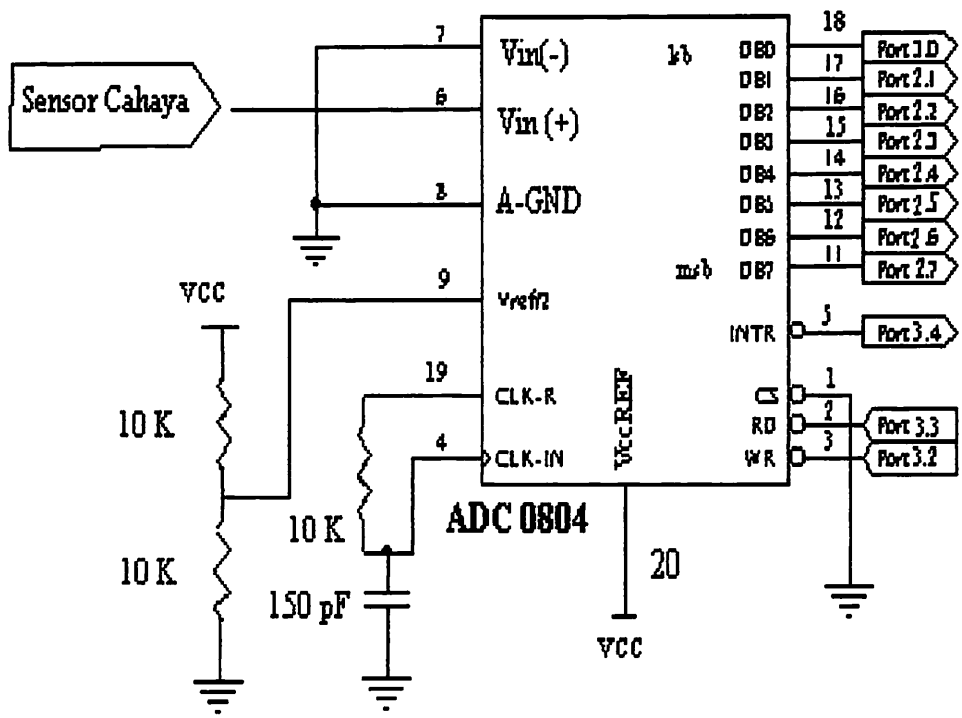
$$\text{Output ADC} = \frac{\text{Vin}}{\text{Resolusi}}$$

Misalkan, jika tegangan masukan yang diperoleh dari rangkaian sensor cahaya sebesar 3 Volt maka output ADC yang akan diperoleh sebesar :

$$\text{Output ADC} = \frac{3}{0{,}02} = 150 \text{ step desimal}$$

$$150\ \text{d} = (10010110)_{\text{b}} \rightarrow 96\ \text{h}$$

Untuk lebih jelasnya, gambar dari rangkaian ADC 0804 seperti yang terlihat pada Gambar berikut:

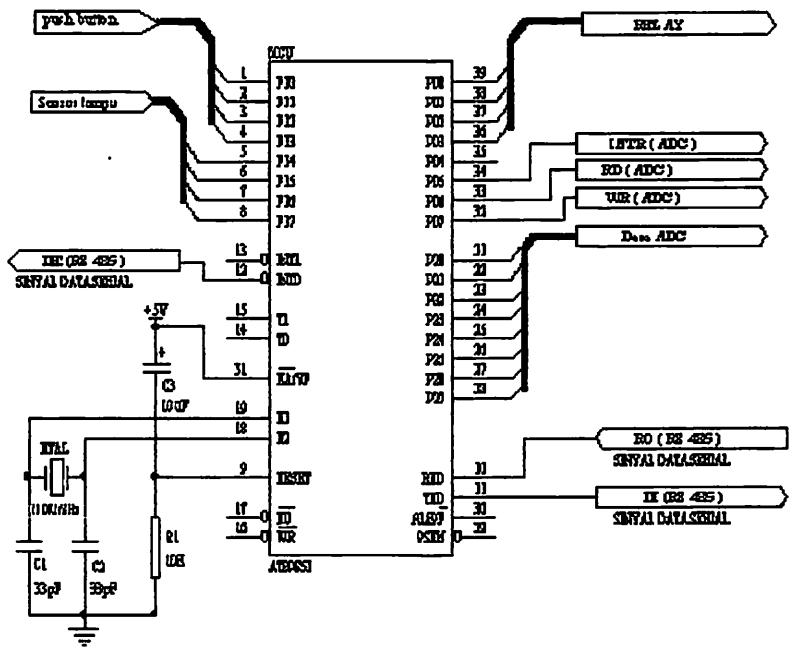


Gambar 3-5 Rangkaian ADC

3. 2. 4. Mikrokontroler AT89S51

Pada bagian ini mikrokontroler merupakan komponen yang paling berperan dalam pengontrolan lampu otomatis berdasarkan kondisi cahaya, disini digunakan mikrokontroler produksi *Atmel Semiconductor Technology* AT89S51 dikarenakan mikrokontroler tersebut banyak tersedia dipasaran sehingga sangat mudah mendapatkannya, disamping harganya yang relatif murah.

3. 2. 4. 1. Unit Kontrol.



Gambar 3-6. Rangkaian Mikrokontroler Unit Kontrol

Dalam perancangan ini mikrokontroler difungsikan sebagai unit kontrol dengan fungsi port sebagai berikut:

a. Port 0

Pin P0.0 sampai pin P0.3 berfungsi sebagai sinyal kontrol relay.

Pin P0.5 sampai pin P0.7 untuk data ADC (INTR, RD, WR)

b. Port 1

Pin P1.0 sampai pin P1.3 berfungsi sebagai inputan dari output push button.

Pin P1.4 sampai pin P1.7 berfungsi sebagai inputan dari ouput rangkaian sensor lampu.

c. Port 2

Pin P2.0 sampai pin P2.7 berfungsi sebagai inputan data ADC.

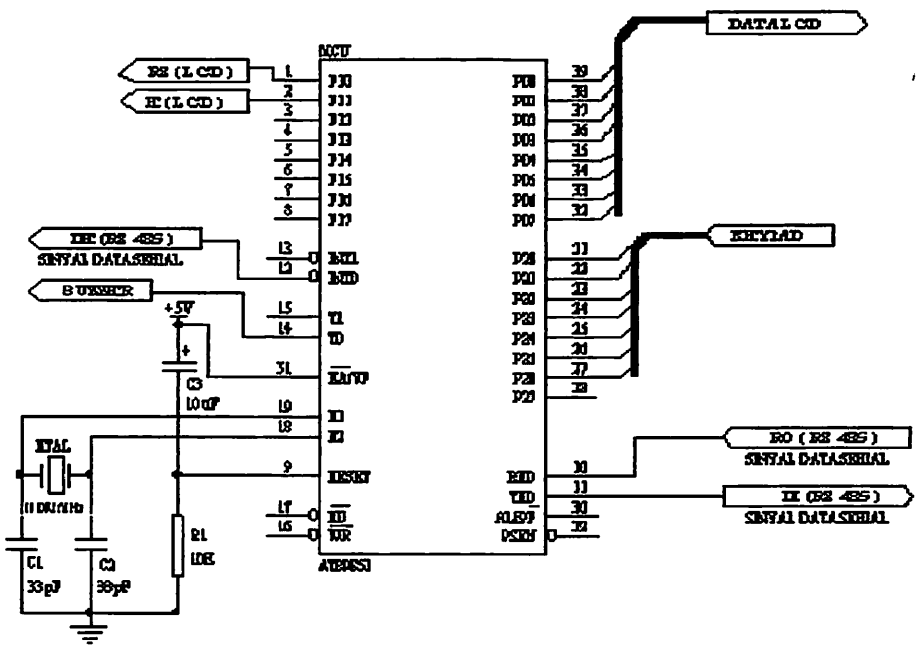
d. Port 3

Pin P3.0 berfungsi sebagai RxD yaitu pin penerima data serial yang dikirimkan dari pusat control.

Pin P3.1 berfungsi sebagai TxD yaitu pin pengirim data serial yang akan dikirimkan menuju pusat kontrol.

Pin P3.2 untuk sinyal control RS 485 (DE).

3. 2. 4. 2. Pusat Kontrol



Gambar 3-7. Rangkaian Mikrokontroler Pusat Kontrol

Fungsi masing–masing port mikrokontroller pusat control adalah sebagai berikut:

a. Port 0

Pin P0.0 sampai pin P0.7 berfungsi sebagai data LCD.

b. Port 1

Pin P1.0 berfungsi sebagai data RS (LCD).

PinP1.2 berfungsi sebagai data E (LCD).

c. Port 2

Pin P2.1 sampai pin P2.7 berfungsi sebagai inputan data dari keypad.

d. Port 3

Pin P3.0 berfungsi sebagai RxD yaitu pin penerima data serial yang dikirimkan dari unit control.

Pin P3.1 berfungsi sebagai TxD yaitu pin pengirim data serial yang akan dikirimkan menuju unit kontrol.

Pin P3.2 untuk sinyal control RS 485 (DE).

3. 2. 5. Rangkaian Clock

Mikrokontroler AT89S51 memiliki rangkaian osilator internal didalam *chip*nya yang difungsikan sebagai sumber clock. Agar rangkaian osilator ini dapat difungsikan, maka dihubungkan dengan sebuah kristal pada pin X1 dan X2 dari mikrokontroler, serta dua buah kapasitor yang dihubungkan ke *ground.* Kapasitor tersebut mempunyai ketentuan sebagai berikut:

- C1 dan C2 = 20 pF – 40 pF untuk kristal.
- C1 dan C2 = 30pF – 50 pF untuk keramik resonator.

Dalam minimum sistem ini kapasitor yang digunakan adalah adalah kapasitor keramik dengan nilai 30 pF, sedangkan dalam rangkaian ini osilator kristal yang dipakai mempunyai harga 11,059 MHz, sehingga siklus mesin *(duty cycle)* program akan dijalankan setiap langkahnya selama 1,085 µs (mikro detik). Siklus tersebut diambil berdasarkan ketentuan MCU AT89S51 yaitu 12 clock = 1 siklus mesin, sedangkan frekuensi yang dipakai adalah 12 MHz.

Untuk menghitung waktu yang dibutuhkan guna menyelesaikan sebuah instruksi adalah dengan cara mencari jumlah siklus mesin (C) dari instruksi, maka dapat diketahui:

Uraiannya adalah sebagai berikut:

$$T_{instruksi} = \frac{C \times 12}{frekuensi}$$

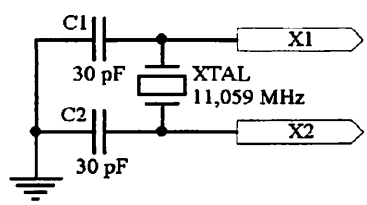
Sehingga untuk frekuensi kristal 11,059 MHz dari satu siklus instruksi adalah:

$$T_{instruksi} = \frac{1 \times 12}{11.059.000}$$

$$= 1.085\ \mu s$$

$$\approx 1\ \mu s \text{ per satu siklus}$$

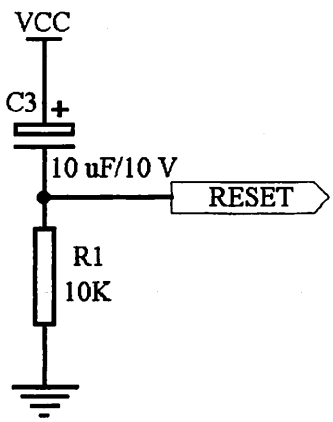
Dan rangkaiannya dapat dilihat pada gambar 3. 3. berikut ini :



Gambar 3-8 Rangkaian Clock

3. 2. 6. Rangkaian Reset

Rangkaian reset bertujuan agar mikrokontroler dapat dapat menjalankan proses dari awal. Rangkaian reset untuk mikrokontroler dirancang agar mempunyai kemampuan *power on reset* yaitu *reset* yang terjadi pada saat sistem pertama kali dinyalakan karena kondisi reset dapat terjadi apabila adanya pulsa transisi dari kondisi '0' *(low)* menuju '1' *(high).* Pulsa transisi *low to high* ini akan me-*reset* mikrokontroler menuju alamat awal 0000H. Rangkaian ini terdiri dari satu buah resistor dan satu buah kapasitor, seperti yang terlihat pada gambar 3-9. berikut ini:



Gambar 3-9 Rangkaian Reset

Kondisi reset terjadi dengan adanya logika '1' *(high)* selama minimal 2 *cycle* pada kaki RST. Setelah kondisi pin RST kembali pada kondisi '0' *(low),* mikrokontroler alan mulai menjalankan program dari alamat 0000H. Kondisi pada RAM internal tidak terjadi perubahan selama terjadi *reset.*

Gambar 3-4 merupakan gambar rangkaian *reset* yang bekerja secara otomatis pada saat sumber daya diaktifkan *(power on reset).* Pada saat sumber daya diaktifkan, maka kapasitor (C), sesuai dengan sifat kapasitor akan terhubung-singkat pada saat itu sehingga arus mengalir dari V_{CC} langsung ke RST sehingga kaki tersebut berlogika '1' *(high).* Kemudian kapasitor terisi hingga tegangan pada kapasitor (V_C) yaitu tegangan antara V_{CC} dan titik antara kapasitor (C), dan resistor (R), mencapai V_{CC}, secara otomatis tegangan pada R atau tegangan RST akan turun menjadi 0 V sehingga kaki RST akan berlogika '0' *(low)* dan proses reset selesai.

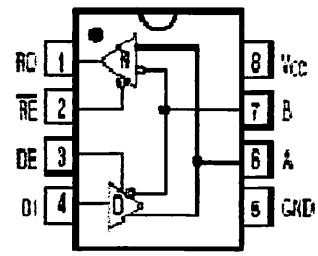
Begitu catu daya dinyalakan maka aliran arus akan mengalir dari V_{CC} menuju kaki RST. Tegangan pada kaki RST atau V_R akan berubah menjadi :

$$V_R = \frac{R \times Vcc}{R}$$

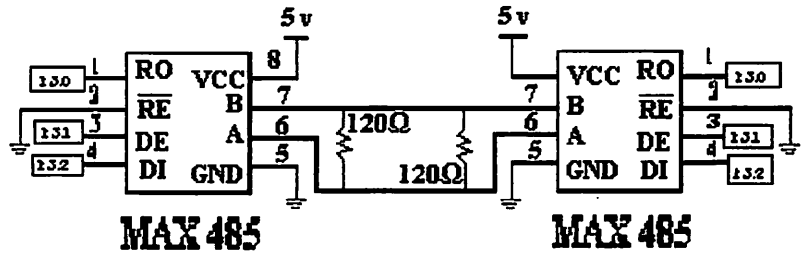
Yaitu 5 V dengan nilai V_{CC} = 5 V. Tegangan 5 V pada kaki RST menyebabkan kaki ini berlogika '1' (high) setelah itu aliran arus dari V_{CC} melalui R akan terhenti dan tegangan pada kaki RST akan turun menuju nol sehingga logika pada kaki ini berubah menjadi '0' (low) dan proses reset selesai.

3. 2. 7. Rangkaian Komunikasi Data Serial.

Komunikasi data ditransmisikan melalui level RS 485, karena output dari TxD dan RxD pada mikrokontroller AT89S51 merupakan level TTL, maka diperlukan rangkaian untuk mengubah ke level RS 485. Dalam perencanaan ini digunakan dua buah IC MAX 485 seperti gambar berikut:



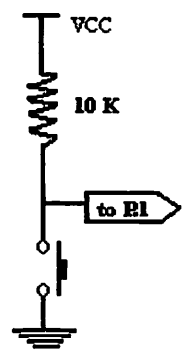
Gambar 3-10. Kontruksi RS 485



Gambar 3-11. Rangkaian RS 485

3. 2. 8. Rangkaian Push Button Switch.

Push button switch adalah saklar lampu pada tiap ruangan yang berfungsi untuk menyalakan dan mematikan lampu pada ruangan. Ouput rangkaian ini merupakan inputan port 1 mikrokontroller unit control AT89S51 yang dikendalikan oleh perangkat lunak (software).

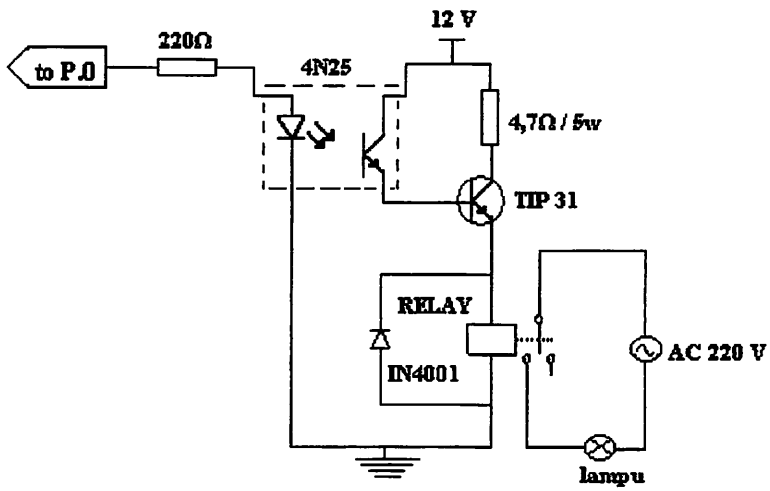


Gambar 3-12. Rangkaian Push Button Switch

3. 2. 9. Rangkaian Driver Relay

Seperti yang telah dijelaskan sebelumnya mengenai fungsi *relay* untuk perancangan ini yang dikontrol oleh mikrokontroler tersebut maka dalam bekerjanya *relay* tersebut membutuhkan suatu rangkaian pengendali relay yang lazim disebut *driver relay.*

Di dalam 4N25 terdapat transistor jenis NPN yang dapat dipicu oleh cahaya LED, transistor ini peka terhadap cahaya sehingga bisa disebut juga fototransistor. Bila LED menyala maka pada basis transistor akan terjadi loncatan electron yang bisa menimbulkan arus basis dan membuat Ic (arus collector) mengalir atau transistor menjadi saturasi. Akibatnya TIP 31 memperoleh arus basis yang akan mengaktifkan relay.

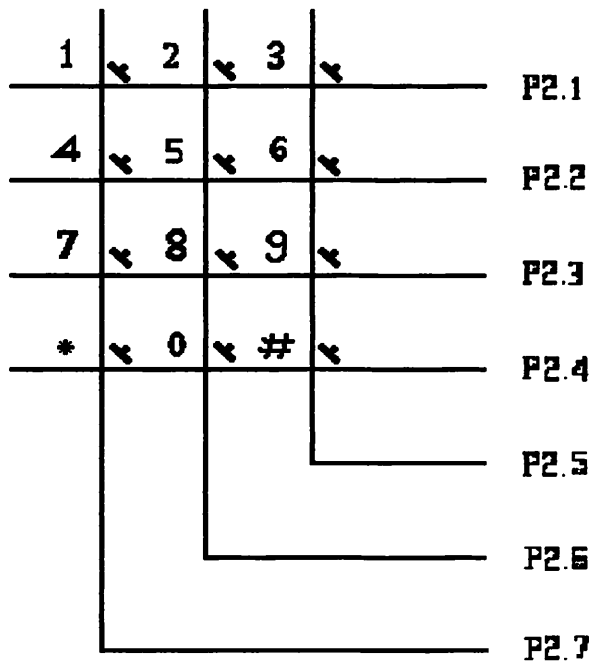


Gambar 3-13. Rangkaian Driver Relay pada Unit Kontrol

Relay yang diparalel dengan dioda bertujuan apabila ada terjadi perubahan kondisi dari kondisi *on* ke kondisi *off* atau sebaliknya, pada transistor tidak terjadi arus balik yang besar.

3. 2. 10. Keypad

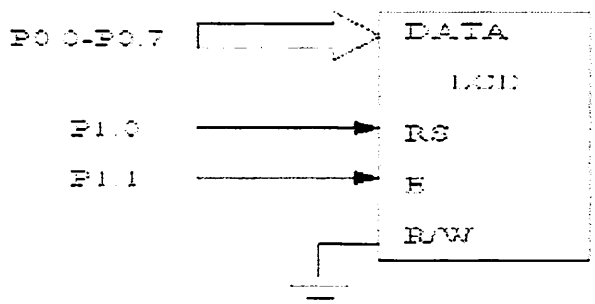
Keypad berfungsi untuk menyalakan dan mematikan lampu pada ruangan yang dilakukan dari pusat control berhubung keadaan lampu pada ruangan yang telah dikondisikan oleh sensor cahaya tidak tepat dengan kebutuhan saat itu, misalnya pada malam hari sensor cahaya mengharuskan lampu hidup, tetapi ruangan tidak dipakai maka lampu pada ruangan itu bisa dimatikan melalui keypad. Keypad yang digunakan adalah keypad matriks 3X4 dengan dua belas saklar tekan (push button switch). Sinyal dari port 2.1 sampai port 2.4 mikrokontroller masuk ke kelompok baris keypad, sedangkan kelompok kolom keypad dihubungkan ke port 2.5 – port 2.7 mikrokontroller. Untuk fungsi dari tombol-tombol keypad tergantung pada pemrograman. Berikut blok diagram dari penyambungan keypad ke mikrokontroller.



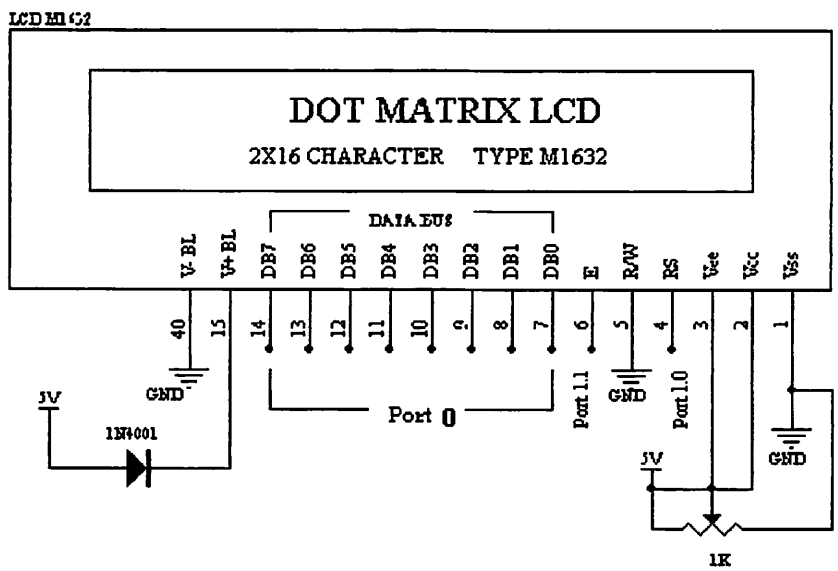
Gambar 3-14.Blok Diagram Hubungan Keypad dengan Mikrokontroller

3. 2. 11. Module LCD

Module LCD ini dalam pengoperasiannya memerlukan 8 bit data dan 3 bit kontrol. 8 bit data LCD dihubungkan ke Port 0 mikrokontroller. Sinyal kontrol berasal dari mikrokontroller port 1.0 untuk RS (*Register Selection*), port 1.1 untuk E (*Enable/Operation start*). Kaki R/W dihubungkan ke ground karena hanya akan dilakukan operasi penulisan ke LCD. Blok diagram dan rancangan rangkaian untuk penanganan tampilan LCD ditunjukkan dalam gambar berikut :



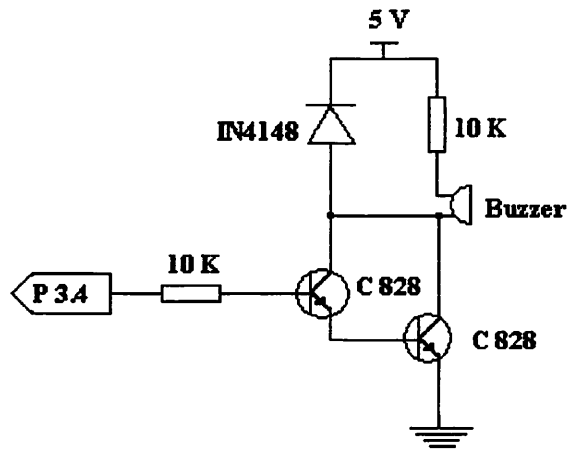
Gambar 3.15 Blok Diagram Hubungan LCD dengan Mikrokontroller



Gambar 3.16 Rancangan Rangkaian LCD

3. 2. 12. Rangkaian Driver Buzzer

Rangkaian driver buzzer diperlukan untuk mengaktifkan buzzer karena output dari mikrokontroller tidak mampu untuk langsung mengaktifkan buzzer. Jika ada arus bias pada basis transistor TR1 maka akan ada arus yang mengalir dari kolektor ke emitor yang merupakan arus bias kaki basis TR2 maka arus kolektor TR2 akan mengalir ke emitor yang akan mengaktifkan buzzer.



Gambar 3.17. Rangkaian Driver Buzzer

Memory ini biasa digunakan untuk menyimpan instruksi (perintah) berstandar *MCS-51 code* sehingga memungkinkan mikrokontroller ini untuk bekerja dalam mode *single chip operation* (mode operasi keping tunggal) yang tidak memerlukan *external memory* (memori luar) untuk menyimpan *source code* tersebut.

Dalam sistem mikrokontroller terdapat dua hal yang mendasar, yaitu perangkat keras dan perangkat lunak yang mana keduanya saling terkait dan saling mendukung.

2. 1. 1. Perangkat Keras Mikrokontroller AT89S51

Mikrokontroller AT89S51 secara umum memiliki spesifikasi data teknis dan fasilitas sebagai berikut :

a. CPU 8-bit berstandart MCS-51.

b. RAM internal 128 byte (128 X 8 bit), *on chip*

c. 4 buah port I/O yang dapat diprogram.

d. Dua *timer* dan *counter* 16 bit.

e. Enam *Interupt Sources*.

f. Port *serial interface* yang dapat diprogram.

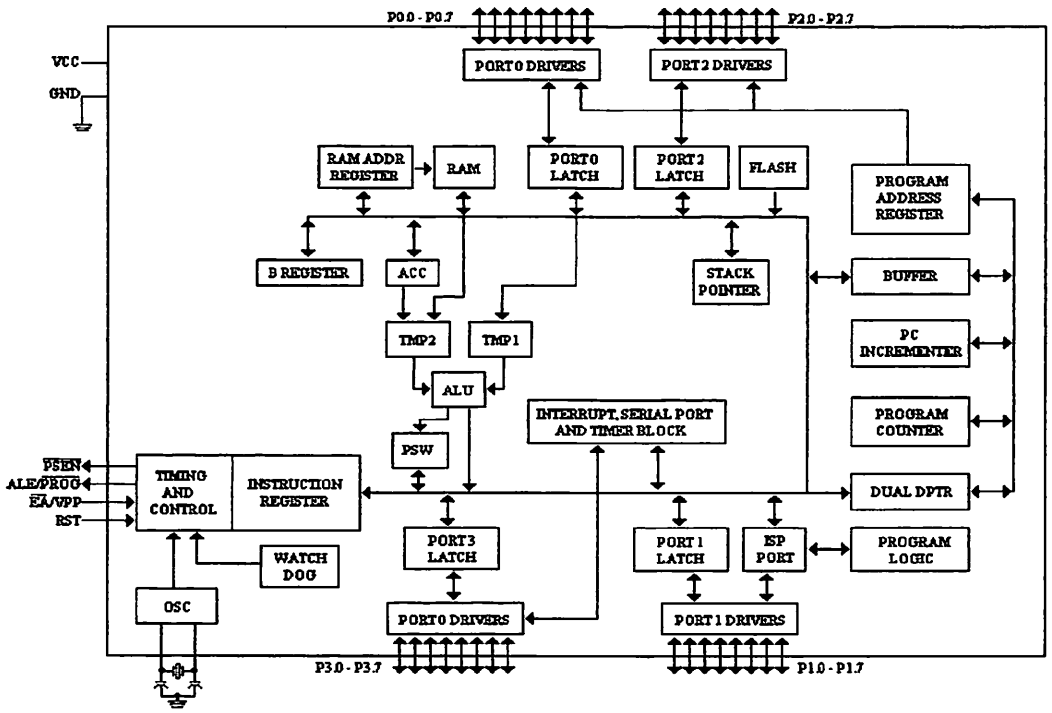
g. Terdapat *Low Power Idle* dan *Power Down Modes*.

h. *Boolean Processor* (dapat melakukan operasi bit).

i. 210 bit *addressable locations*.

j. Clock dan Osilator internal 0 – 24 Hz.

k. Memori 4 Kbyte *(In-system Reprogramable Flash Memory).* Memungkinkan untuk 1000 kali proses hapus / tulis.



Gambar 2-1. Blok Diagram Mikrokontroller AT89S51

2. 1. 2. Arsitektur Mikrokontroller AT89S51

Arsitektur mikrokontroller AT89S51 adalah sebagai berikut :

a. CPU 8-bit dengan register A *(Accumulator)* dan register B, yang optimal untuk aplikasi kontrol.

b. 16 bit PC *(Program Counter)* dan DPTR *(Data Pointer).*

c. 8 bit PSW *(Program Status Word).*

d. 8 bit SP *(Stack Pointer).*

e. 4 Kbyte EPROM internal.

f. 128 byte RAM internal.

- 4 *bank register*, masing-masing berisi 8 register.

- 16 byte yang dapat dialamati pada *bit level.*
- 80 byte *general purpose memory* data.

g. 32 pin input – output tersusun atas Port 0 – Port 3, masing-masing 8 bit.

h. 2 buah *Timer / Counter* 16 bit.

i. *Receiver / Transmitter* data serial *Full Duplex* : SBUF.

j. *Control Register*, yaitu TCON, TMOD, SCON, PCON, IP dan IE.

k. 5 buah sumber interupt (2 buah sumber interupt external dan 3 buah interupt internal).

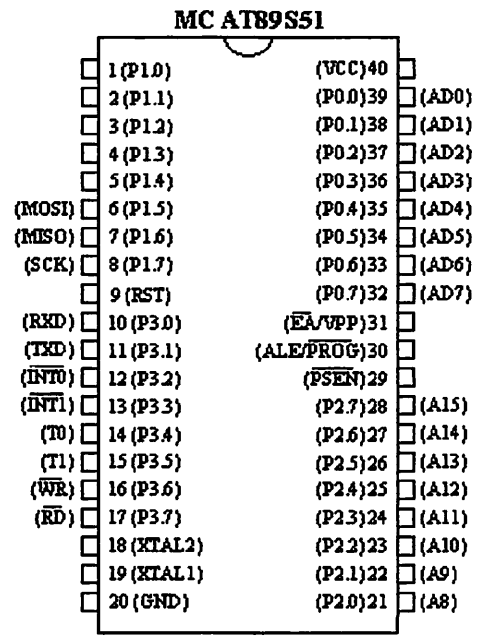
l. Osilator dan Clock Internal.

m. Watchdog Timer.

n. ISP (In System Programming).

2. 1. 3. Konfigurasi Pena-pena Mikrokontroller AT89S51

Mikrokontroller AT89S51 terdiri atas 40 pin, dengan konfigurasi sebagai berikut :



Gambar 2-2. Konfigurasi Pena-pena Mikrokontroller AT89S51

Fungsi tiap-tiap pena adalah sebagai berikut :

1. VCC *(Supply Tegangan)*

   Terhubung pada catu daya + 5 Volt .

2. GND *(Ground)*

   Dihubungkan dengan *ground* rangkaian.

3. Port 0 (P0.0 – P0.7)

   Port 0 merupakan port I/O serbaguna 8 bit dua arah fungsi ganda yang berada pada pin 32-39 dari mikrokontroler AT89S51. Port ini dapat digunakan sebagai *Low Order Multiplex Address* (A0 – A7) / Data (multipleks bus alamat rendah dan bus data selama

pengaksesan ke memori eksternal) ataupun menerima kode byte pada saat *Flash Programming* berlangsung.

Pada fungsi segagai I/O biasa port ini dapat memberikan output *sink* ke delapan buah TTL input atau dapat diubah sebagai input dengan memberikan logika '1' pada port tersebut.

Pada fungsi *low order multiplex address/data port* ini akan mempunyai *internal pull-up* dan pada saat *Flash Programming* berlangsung diperlukan *external pull-up* terutama pada saat verifikasi program.

4. Port 1 (P1.0 – P1.7)

   Merupakan port I/O dua arah biasa atau menerima *low order address byte* selama pada saat *Flash Programming* berlangsung.

   Port ini dilengkapi dengan *internal pull-up* dan berfungsi sebagai input dengan memberikan logika '1'.

   Sebagai output port ini dapat memberikan *output sink* keempat buah input TTL. Port ini berfungsi sebagai input atau output dan bekerja baik untuk operasi bit maupun byte, tergantung dari pengaturan *software* dan berada pada pin 1-8.

5. Port 2 (P2.0 – P2.7)

   Merupakan port I/O dua arah biasa atau sebagai *high order address* (A8-A15) selama pengambilan *(fecthing)*, pada saat mengakses memori secara 16 bit (MOVX @DPTR) dari memori eksternal dan

menerima beberapa sinyal kontrol selama pemrograman dan verifikasi.

Pada saat mengakses memori secara 8 bit, (MOVX @RN) port ini akan mengeluarkan isi dari P2 *Special Function Register*.

Port ini mempunyai *internal pull-up* dan berfungsi sebagai input dengan memberikan logika '1'. Sebagai output port ini dapat memberikan output *sink* keempat buah input TTL. dengan *internal pull-up*. Port 2 mengeluarkan *high order* selama pengambilan *(fetching)* program memori eksternal dan selama mengakses data memori eksternal. Port 2 juga menerima *high order address bit.*

6. Port 3 (P3.0 – P3.7)

Port 3 selain memiliki fungsi dan sifat yang sama sebagai I/O dengan *internal pull-up* sama dengan port 1 maupun port 2, juga mempunyai fungsi khusus port 3 ini adalah sebagai berikut :

- RD (P3.7) : *Strobe* baca data memori eksternal
- WR (P3.6) : *Strobe* tulis data memori eksternal
- T1 (P3.5) : Input eksternal timer 1
- T0 (P3.4) : Input eksternal timer 0
- INT1 (P3.3) : Interupt 1 eksternal
- INT0 (P3.2) : Interupt 0 eksternal
- TxD (P3.1) : Port output serial
- RxD (P3.0) : Port input serial

7. RST

Input reset pada pin 9 adalah *reset master* untuk AT89S51, reset akan aktif dengan memberikan input high selama 2 *cycle.*

8. ALE *(Address Latch Enable)* / PROG

Pulsa output ALE digunakan untuk proses *latching byte* adalah *address* rendah (A0 – A7) selama pengaksesan ke memori eksternal. Pin ini juga merupakan input pulsa program yang aktif rendah (PROG) selama *Flash Programming.*

Sinyal output ALE yang berada pada pin 30 fungsinya dipergunakan untuk demultiplex bus alamat dan bus data. Pada kondisi normal ALE membangkitkan sinyal pulsa sebesar 1/16 frekuensi osilator kecuali pada saat mengakses memori eksternal sinyal clock pada pin ini dapat pula di-*disable* dengan men-set bit 0 dari *Special Function Register* di alamat 8EH.

ALE akan aktif pada saat mengakses memori eksternal (MOVX & MOVC). Juga dapat digunakan sebagai clock dalam aplikasi secara umum. Jika clock pada mikrokontroler menggunakan x'tal 12 Mhz maka frekuensi sinyal osilator ALE sebesar 1/6 frekuensi sinyal x'tal (2 Mhz).

9. PSEN *(Program Strobe Enable)*

PSEN adalah sebuah sinyal keluaran yang terdapat pada pin 29. Fungsinya adalah sebagai sinyal kontrol untuk memungkinkan mikrokontroler membaca program *(code)* dari memori eksternal.

Biasanya pin ini dihubungkan ke pin OE EPROM. Jika eksekusi program dari ROM internal atau *flash memory*, maka PSEN akan berada pada kondisi tidak aktif *(high)*. PSEN akan aktif dua kali pada setiap detiknya.

10. X'TAL 1 *(Input Oscilator)*

Pin XTAL1 merupakan pin input *inverting oscillator amplifier* dan input rangkaian *internal clock operating.*

11. X'TAL 2 *(Output Oscilator).*

Sedangkan pin XTAL2 merupakan pin output dari *inverting oscillator amplifier.*

12. EA / Vpp *(External Access / Programming Supply Voltage)*

Pada kondisi *low* (di-*hold* rendah secara eksternal atau dihubungkan ke *ground*), pin ini akan berfungsi sebagai EA yaitu mikrokontroler akan menjalankan program yang ada pada memori eksternal (0000H – FFFFH) setelah sistem di-*reset.*

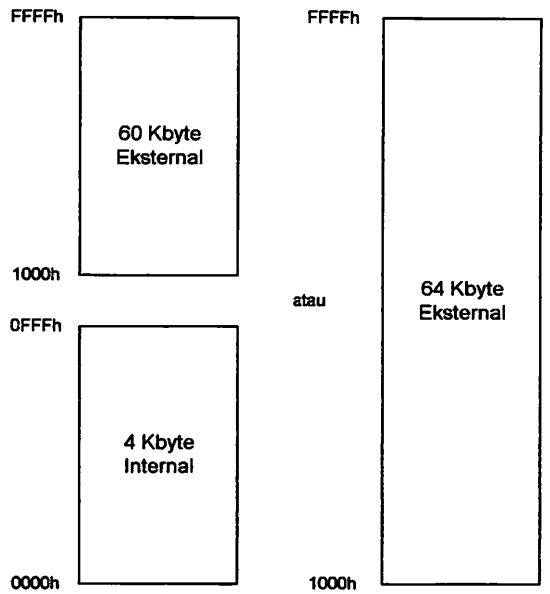
Jika berkondisi *high* (pin ini dihubungkan ke VCC), pin ini akan berfungsi untuk menjalankan program yang ada pada memori internal. Pada saat *Flash Programming* berlangsung pin ini akan mendapatkan tegangan 12 volt (VP).

2. 1. 4. Organisasi Memori

Produk mikrokontroler AT89S51 dari Atmel ini memiliki ruang alamat *(address space)* memori data dan memori program yang terpisah. Pemisahan memori data dan memori program tersebut membolehkan memori data diakses dengan alamat 8-bit sehingga dapat dengan cepat dan mudah disimpan dan dimanipulasi oleh CPU 8-bit. Namun demikian, alamat memori data 16-bit bisa juga dihasilkan melalui register DPTR *(Data Pointer Register).*

Memori program hanya dapat dibaca saja tidak bisa ditulisi (karena disimpan dalam EPROM). Terdapat memori program yang bisa diakses langsung hingga 64 Kbyte. Sedangkan *strobe* (tanda) untuk akses program memori eksternal melalui sinyal PSEN *(Program Store Enable).*

Memori data menempati suatu ruang alamat yang terpisah dari memori program. Memori eksternal dapat diakses secara langsung hingga 64 Kbyte dalam ruang memori data eksternal. CPU akan memberikan sinyal baca dan tulis, (RD dan WR), selama pengaksesan memori data eksternal. Memori data eksternal dan memori program eksternal dapat dikombinasi dengan cara menggabung sinyal RD dan PSEN melalui gerbang AND dan keluarannya sebagai tanda baca ke memori data / program eksternal. Mikrokontroller AT89S51 memiliki internal program memori 4 Kbyte dan dapat diperluas *(expant)* dengan memori luar menjadi 64 Kbyte memori program dan 64 Kbyte memori data. Secara otomatis jika alamat program lebih besar dari 0FFFh akan mengeksekusi *address byte* dari program memori.



Gambar 2-3. Oganisasi Program Memory

Memori internal terdiri dari ROM/*Flash Memory* dan RAM data di dalam *chip*. RAM berisi susunan *general purpose storage, bit addressable storage, register bank* dan *special function register*. Gambar 2-5 menampilkan secara detil memori data didalam *chip* mikrokontroller AT89S51 (MCS-51). Ruang memori internal dibagi menjadi:

- *Register Bank* (00H-1FH)
- *Bit Addressable RAM* (20H-2FH)
- *General Purpose RAM* (30H-7FH)
- *Special Function Register* (80H-FFH)

Untuk data memori dibagi menjadi dua bagian yaitu register khusus yang dipergunakan oleh mikrokontroller adalah SFR *(Special Function Register)* dan 4

bank atau 8 register (R0-R7) yang dapat dipakai oleh pengguna. Untuk alamat bawah yang pertama yaitu 00H sampai 7FH sebanyak 128 byte terbagi dalam tiga bagian besar berdasarkan kegunaannya sebagai berikut :

a. ***Register Banks.***

Mikrokontroler AT89S51 mempunyai delapan buah regiter yang terdiri atas R0 hingga R7.

- Lokasi *register bank* dimulai dari alamat 00H – 1FH terdiri dari 32 *byte*
- *Register bank* ini terdiri dari 4 buah 8 *byte* yang dapat dipilih melalui pengaturan RS0 dan RS1 yang merupakan bit ke-3 dari *Program Status Word Register.*

b. ***Bit Addressable RAM.***

Mikrokontroller AT89S51 memiliki 210 lokasi bit *addressable*, dimana 128 lokasi mempunyai alamat *byte* mulai Terdiri dari 16 byte yang dimulai dari 20h – 2Fh. Masing-masing dari 128 *byte* lokasi ini dapat dialamati secara langsung.

c. ***General Purpose RAM.***

Lokasi memori pada *General Purpose RAM* dapat diakses secara langsung dengan mode *direct* maupun *indirect addressing.* Sebagai contoh, untuk membaca dan meng-*copy* isi RAM internal dengan alamat 5FH kedalam *Accumulator* dapat menggunakan instruksi:

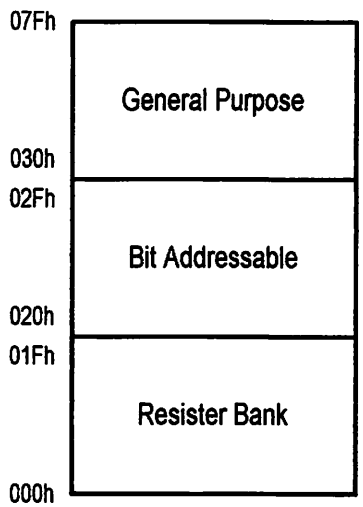
MOV A, 5FH

Instruksi ini memindahkan *byte* data secara *direct addressing* dengan sumber yang beralamat 5FH.

RAM internal dapat juga diakses menggunakan *indirect addressable* melalui R0 atau R1. Sebagai contoh, dua instruksi berikut ini:

```
MOV R0,#5FH
MOV A,@R0
```

Instruksi pertama dipakai sebagai *immediate addressable* yang memindahkan nilai 5FH kedalam register R0 dan instruksi kedua dipakai sebagai *indirect addressing* untuk memindahkan data yang ditunjuk oleh R0 kedalam *Accumulator.*



Gambar 2-4. Data Memory

Tabel 2 - 1. Register Bank

RS1	RS0	Register Bank	Address
0	0	0	00h – 07h
0	1	1	08h – 09h
1	0	2	10h – 17h
1	1	3	18h – 1Fh

2. 1. 5. Special Function Register (SFR)

SFR teletak pada alamat memori internal 80h – FFh. Tetapi tidak semua alamat tersebut digunakan sebagai SFR, melainkan alamat tertentu seperti tabel berikut :

Tabel 2 - 2. Special Function Register

Simbol	Nama	Address
ACC	ACCUMULATOR	0E0h
B	BV REGISTER	0F0h
PSW	PROGRAM STATUS WORD	0D0h
SP	STACK POINTER	81h
DPTR	DATA POINTER	
DPL	LOW BYTE	82h
DPH	HIGH BYTE	83h
P0	PORT 0	80h
P1	PORT 1	90h
P2	PORT 2	0A0h
P3	PORT 3	0B0h
IP	INTERRUPT PRIORITY CONTROL	0B8h
IE	INTERRUPT ENABLE CONTROL	0A8h
TMOD	TIMER/COUNTER MODE CONTROL	89h
TCON	TIMER/COUNTER CONTROL	88h
TH0	TIMER/COUNTER 0 HIGH CONTROL	8Ch
TL0	TIMER/COUNTER 0 LOW CONTROL	8Ah
TH1	TIMER/COUNTER 1 HIGH CONTROL	8Dh
TL1	TIMER/COUNTER 1 LOW CONTROL	8Bh
SCON	SERIAL CONTROL	98h
SBUF	SERIAL DATA BUFFER	99h
PCON	POWER CONTROL	87h

Berikut ini penjelasan dari register-register fungsi khusus tersebut :

- Accumulator (ACC) atau Register A dan Register B.

  Kedua register tersebut digunakan untuk operasi perkalian dan pembagian.

- Program Status Word (PSW).

  Register ini meliputi bit-bit : CY (Carry), AC (*Auxciliary Carry*), OV (*Over Flow*), FO (sebagai Flag), RS0 dan RS1 (untuk pemilihan register bank), dan Parity (*Parity Flag*).

- *Stack Pointer* (SP).

  SP merupakan suatu register yang digunakan untuk petunjuk alamat. Register ini berguna apabila di gunakan suatu *routile* pada program utama.

- *Data Pointer High* (DPTRHigh) dan *Data Pointer Low* (DPTRLow).

  DPTR adalah suatu register yang digunakan untuk pengalamatan tidak langsung. Register ini digunakan untuk mengakses memory program baik internal ataupun eksternal, juga digunakan untuk alamat eksternal data. Data DPTR dikontrol oleh dua buah register 8 bit yaitu DPH dan DPL.

- Port 0, Port 1, Port 2, Port3.

  Pada mikrokontroller AT89S51 masing-masing pada port dapat dialamati baik secara byte maupun secara bit. Masing-masing port merupakan *port bidirectional* yang artinya dapat berjalan dua arah (*input* dan *output*). Port 0 dan port 2 digunakan sebagai port-port pengalamatan memory dari luar, port 1 digunakan sebagai port I/O dari mikrokontroller sedangkan port 3 berisi sinyal-sinyal kontrol seperti Interupt, Serial, WR dan RD.

- Register Prioritas Interrupt (*Interrupt Priority Register /IP*)

  Merupakan suatu register yang berisi bit-bit untuk mengaktifkan prioritas dari suatu interrupt yang ada pada mikrokontroller pada taraf yang dinginkan.

- Interrupt Enable Register

  IE merupakan register yang berisi bit-bit untuk menghidupkan atau mematikan sumber interrupt.

- Timer / Counter Control Register

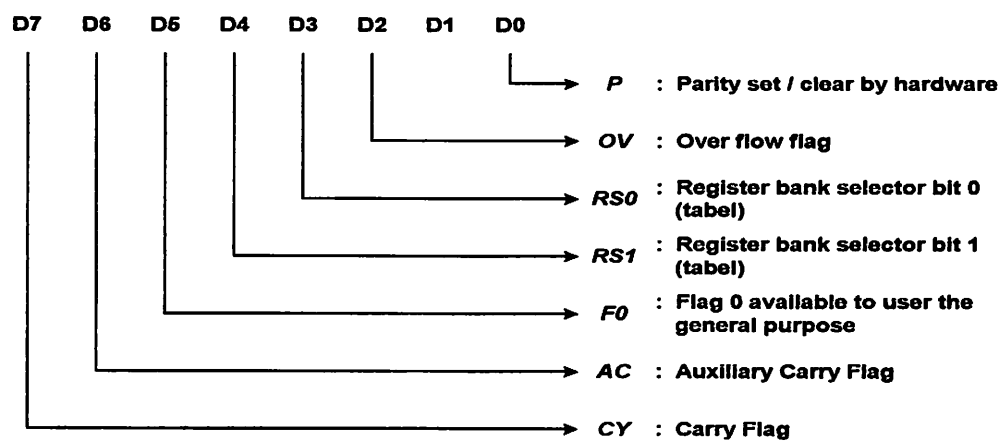
  TCON merupakan register yang berisi bit-bit untuk memulai / menghentikan pewaktu / pencacah.

- Serial Control Buffer (SBUF)

  Register ini digunakan untuk menampung data dari masukan (SBUF IN) ataupun keluaran (SBUF OUT) dari serial port.

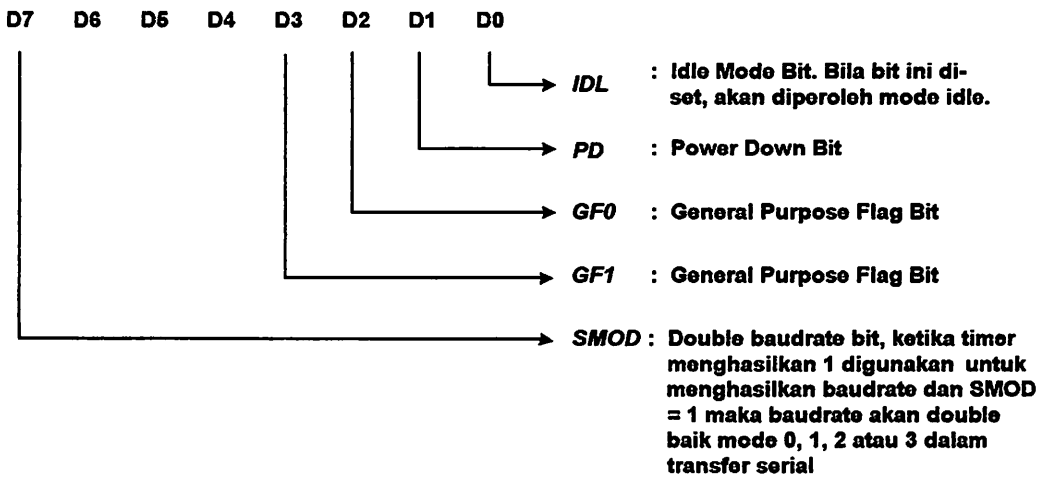
2. 1. 6. *Program Status Word*

Untuk pedefinisian *Program Status Word* ini dapat dilakukan per bit maupun secara keseluruhan dari register ini. Register ini terletak pada alamat D0H. Cara mendefinikannya adalah sebagai berikut :



2. 1. 7. *Power Control Register*

Register ini terletak pada alamat 87H. Cara mendefinisikannya adalah sebagai berikut:



2. 1. 8. Sistem Interrupt

Mikrokontroller AT89S51 mempunyai 5 buah sumber interrupt yang dapat membangkitkan permintaan interrupt, yaitu INT0, INT1, T1, T2 dan port serial.

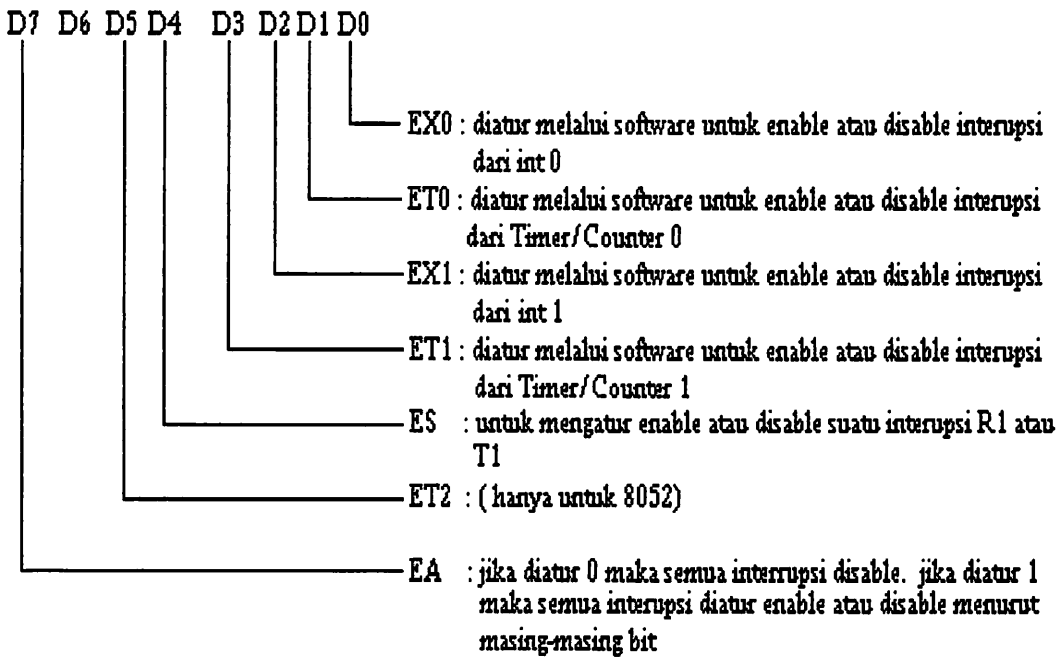
Saat terjadinya interrupt, mikrokontroller secara otomatis akan menuju ke *sub rutin* pada alamat tersebut. Setelah interrupt service selesai di kerjakan, mikrokontroller akan mengerjakan program semula. Dua sumber interrupt eksternal adalah INT0 dan INT1, dimana kedua interupsi eksternal akan aktif atau aktif transisi tergantung isi dari IT0 dan IT 1 pada register TCON. Interupsi T0 dan T1 aktif pada saat timer yang sesuai mengalami *roll over*, interupsi serial dibangkitkan dengan melakukan operasi OR pada R1 dan T1. Tiap-tiap sumber interupsi dapat *enable* atau *disable* secara otomatis.

Tingkat prioritas semua sumber interupsi dapat di program sendiri-sendiri dengan set atau *clear bit* pada SFRS IP (*Interrupt Priority*).

Tabel 2 - 3. Alamat Sumber Interupsi

Sumber Interupt	Alamat Awal
Interrupt Luar 0 (INT0)	0003H
Pewaktu / Pencacah 0 (T0)	000BH
Interrupt Luar 1 (INT1)	0013H
Pewaktu /Pencacah 1 (T1)	001BH
Port Serial	**0023H**

Register yang berperan dalam mengatur aktif tidaknya interupsi adalah *Interupt Enable Register*, berikut ini adalah susunan bit-bit beserta kegunaannya :

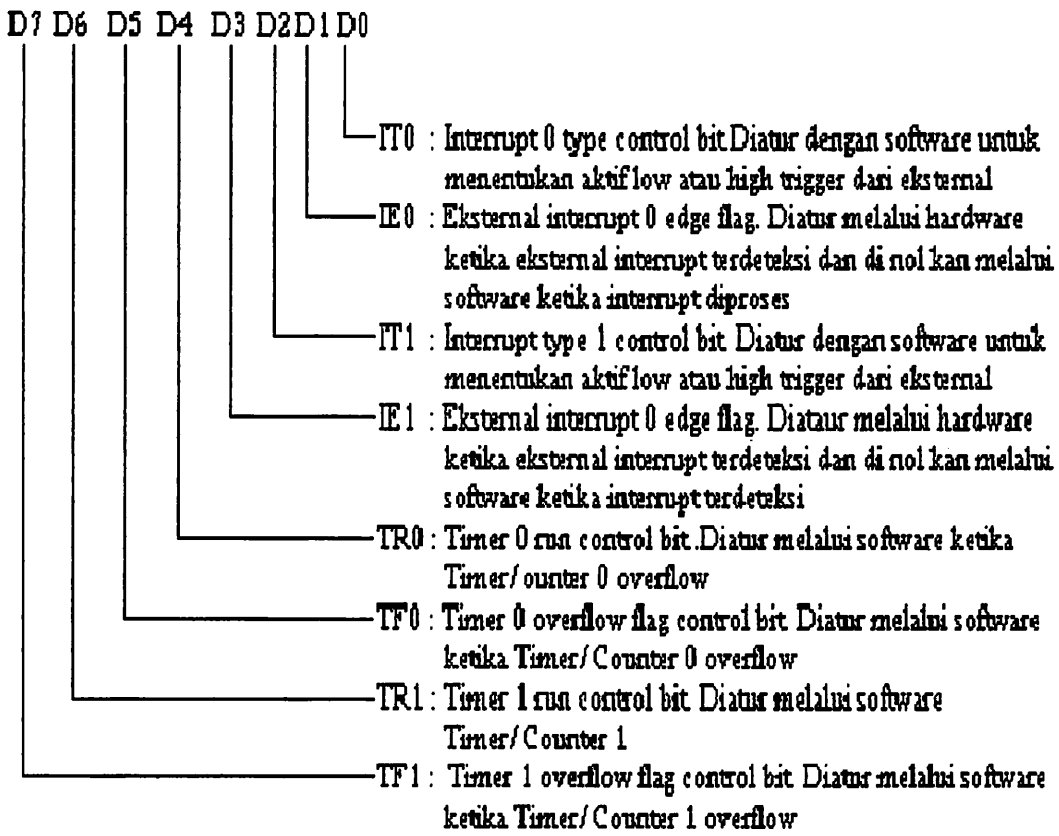


2. 1. 9. Timer /Counter

Pengendalian kerja dari timer / counter dilakukan dengan pengaturan register yang berhubungan dengan kerja dari timer / counter yaitu melalui sebuah TMOD (*Timer / Counter Mode Control*).

Untuk mengaktifkan timer / counter yang meliputi penentuan fungsi sebagai timer atau sebagai counter serta pemilihan mode operasi dapat di atur melalui TMOD yang beralamat pada 89H.

Konfigurasi yang dimaksud adalah sebagai berikut :



2. 1. 10. Metode Pengalamatan

Metode pengalamatan pada AT89S51 adalah sebagai berikut :

a. Pengalamatan Tak Langsung

Operand pengalamatan tak langsung menunjuk ke arah sebuah register yang berisi lokasi alamat memori yang akan digunakan di dalam operasi. Lokasi yang nyata tergantung pada isi register saat instruksi dijalankan. Untuk melaksanakan pengalamatan tak langsung digunakan simbol @.

```
ADD A,@R0        ; Tambahkan isi RAM yang lokasinya
                   ditunjukkan oleh register R0 ke akumulator.
DEC @R1          ; Kurangi satu isi RAM yang
                   alamatnya ditunjukkan oleh register R1.
MOVX @DPTR,A ; Pindahlan isi akumulator ke memori
                   luar yang lokasinya ditunjukkan oleh data
                   pointer (DPTR).
```

b. Pengalamatan Langsung

Pengalamatan langsung dilakukan dengan memberi nilai suatu register secara langsung. Untuk melaksanakan hal tersebut digunakan tanda #.

```
MOV A,#01H       ;  Isi akumulator dengan bilangan 01H.
MOV DPTR,#19ABH  ;  Isi register DPTR dengan bilangan
                    19ABH.
```

Pengalamatan data langsung dari 0 sampai 127 akan mengkases RAM internal, sedang pengalamatan dari 128 sampai 25 akan mengakses register perangkat keras.

```
MOV P3,A        ; Pindahkan isi akumulator ke alamat data
                  B0H (B0H adalah alamat Port 3).
INC 50          ; Naikkan lokasi 50 (desimal) dalam memori.
```

c. Pengalamatan Bit

Pengalamatan bit adalah penunjukkan alamat lokasi bit baik dalam RAM internal (byte 32 sampai 47) atau perangkat keras. Untuk melakukan pengalamatan bit digunakan simbol titik (.), misalnya :

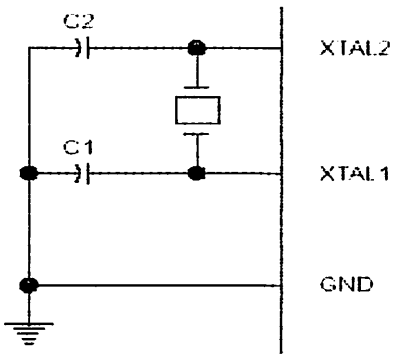
```
SETB P1.1       ; Ubah bit ke 1 pada Port 1 menjadi high.
```

d. Pengalamatan Kode

Ada tiga macam instruksi yang dibutuhkan dalam pengalamatan kode, yaitu *relative jump*, *in-block jump* atau *call* dan *long jump*.

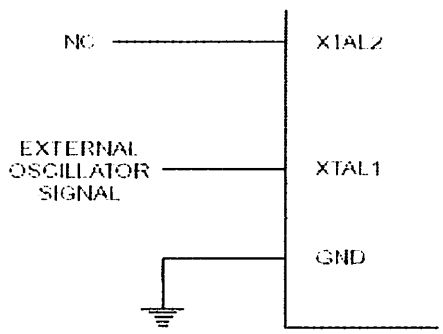
2. 1. 11. Pewaktuan CPU

Mikrokontroler AT89S51 memiliki osilator internal (*on chip oscilator*) yang dapat digunakan yang dapat digunakan sebagai sumber clock bagi CPU. Untuk menggunakan isolator internal diperlukan sebuah kristal atau resonator keramik antara pena XTAL1 dan XTAL2 dan sebuah kapasitor ke *ground* seperti yang terlihat pada gambar 2-9. berikut ini:



Gambar 2-5. Menggunakan Osilator Internal

Untuk kristalnya dapat digunakan frekuensi dari 6 sampai 12 MHz. Sedangkan untuk kapasitor dapat bernilai antara 27 pF sampai 33 pF. Bila menggunakan clock eksternal, maka rangkaiannya dihubungkan seperti pada gambar 2-10. berikut ini:



Gambar 2-6. Menggunakan Sumber Clock Eksternal

2. 1. 12. Watchdog Timer (WDT)

Fungsi dari WDT sebenarnya adalah untuk melakukan peresetan secara otomatis. Dimana dia akan mereset mikrokontroller jika mikrokontroller hang. Oleh sebab itu user harus selalu mereset WDT sebelum WDT mereset mikrokontroller. Jika WDT tidak direset oleh mikrokontroller dalam jangka waktu yang telah ditentukan maka secara otomatis WDTlah yang akan mereset mikrikontroller. WDT terdiri dari 14 bit counter dan Watchdog Timer Reset (WDTRST) SFR. WDT diset default untuk menonaktifkan reset yang ada. Tidak ada jalan lain untuk menonaktifkan WDT kecuali melalui reset (baik hardware reset atau WDT overflow reset). Jika WDT overflow, itu akan membuat suatu keluaran reset high di pin RST.

Untuk mengaktifkannya, user harus menulis 01EH dan 0E1H didalam daftar urutan WDTRST (alamat SFRnya 0A6H). Ketika WDT aktif, user harus mengisinya dengan menuliskan 01EH dan 0E1H ke WDTRST untuk menghindari suatu WDT overflow. 14 bit counter akan overflow jika mencapai angka 16383 (3FFFH), dan ini akan mereset mikrokontroller. Disaat WDT aktif, dia akan menaikkan tiap-tiap siklus mesin ketika osilator sedang menjalankannya. Dan ini artinya user harus mereset WDT sedikitnya tiap-tiap 16383 (3FFFH) siklus mesin. Ketika WDT overflow itu akan menghasilkan suatu keluaran RESET di pin RST. Jangka waktu reset adalah 98 x TOSC, dimana TOSC = 1/FOSC.

2. 1. 13. In System Program (ISP)

ISP port digunakan untuk melakukan pemograman secara langsung tanpa harus melepaskan IC dari tempatnya. Cara ini digunakan agar lebih efisien pada waktu melakukan pemograman. Jika terjadi kesalahan maka kita tidak perlu melepaskan IC tersebut untuk kembali memprogramnya di Downloader AT89S51. Tapi kita hanya perlu memberikan akses pada pin-pin port 1. Tepatnya pada pin P1.5 untuk MOSI dan pin P1.6 untuk MISO serta pin P1.7 untuk SCK.

2. 2. Komunikasi Serial

Melakukan komunikasi serial menggunakan mikrokontroler AT89S51 dapat dilakukan dengan memanfaatkan fasilitas port serial yang sudah ada didalamnya. Port serial memungkinkan kita untuk bisa mengirimkan data dalam format serial. Berdasarkan arahnya, komunikasi data serial dibagi menjadi:

a. **Simplex**

   Pada sistem ini, komunikasi terjadi satu arah saja, dari pengirim (A) ke penerima (B). Penerima B tidak dapat mengirim ke A.

b. **Half Duplex**

   Merupakan komunikasi dua arah, misalnya antara A dan B. Pada saat A mengirim data, B hanya dapat menerima saja. Demikian juga sebaliknya pada saat B mengirim data, A juga hanya dapat menerima saja.

c. Full Duplex

Merupakan komunikasi dua arah yang dapat melakukan pengiriman maupun penerimaan data kepada dua belah pihak yang ber-komunikasi dalam waktu yang bersamaan.

Register penerima dan pengirim pada port serial diakses pada SBUF *(serial buffer)*. Register pengontrol kerja port serial ini adalah *SCON (serial control)*. Bit-bit SCON ini didefinisikan sebagai berikut:

MSB							LSB
SM0	SM1	SM2	REN	TB8	RB8	T1	R1

Tabel 2 - 4. Posisi dan Fungsi Bit

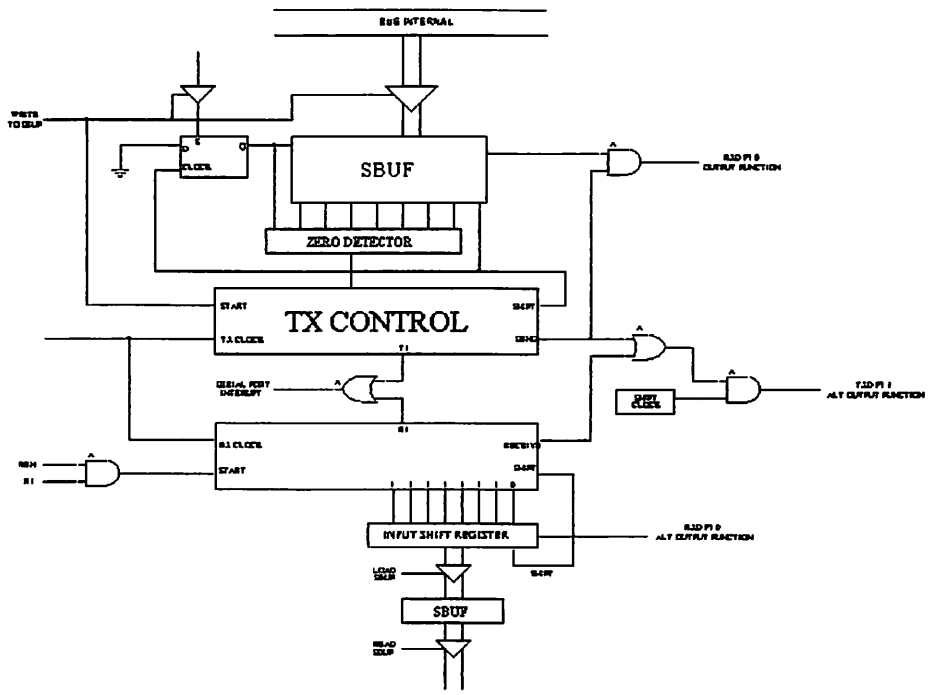
SIMBOL	POSISI	FUNGSI
SM0	SCON.7	Pemilih mode port serial.
SM1	SCON.6	Pemilih mode port serial.
SM2	SCON.5	Membuat *enable* komunikasi multiprosesor dalam mode 2 dan 3.
REN	SCON.4	*Set / clear* oleh perangkat lunak untuk menjalankan / melumpuhkan penerimaan.
TB8	SCON.3	Bit ke-9 yang akan dikirim dalam mode 2 dan 3. *Set / clear* secara *software.*
RB8	SCON.2	Dalam mode 2 dan 3 adalah bit ke-9 yang diterima. Dalam mode 1 jika SM2 = 0, RB8 merupakan *bit stop* yang diterima. Dalam mode 0 RB8 tidak digunakan.
T1	SCON.1	*Transmite interrupt flag.* Di-*set* oleh perangkat keras pada akhir waktu bit ke-8 dalam mode 0, atau pada permulaan dari *bit stop* dalam mode lainnya. Di-*clear* secara *software.*
R1	SCON.0	*Receive interrupt flag.* Di-*set* oleh perangkat keras pada akhir bit ke-8 dalam mode 0

Tabel 2-5. Pemilihan Mode Port Serial.

SM0	SM1	Mode	Keterangan	Baud Rate
0	0	0	*Shift Register*	Frek. osc / 12
0	1	1	8-bit UART	Variabel
1	0	2	9-bit UART	Frek. osc / 32 atau osc / 64

2. 2. 1. Mode 0

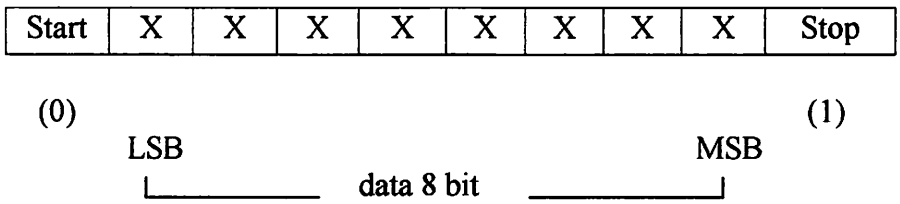
Data serial masuk dan keluar melalui RxD. TxD mengeluarkan clock pergeseran *(shift clock).* Data 8 bit dikirim dan diterima dengan bagian yang pertama masuk sebagai LSB. *Baud rate* tetap pada 1/12 frekuensi osilator.



Gambar 2-7. Port Serial dalam Mode 0

2. 2. 2. Mode 1

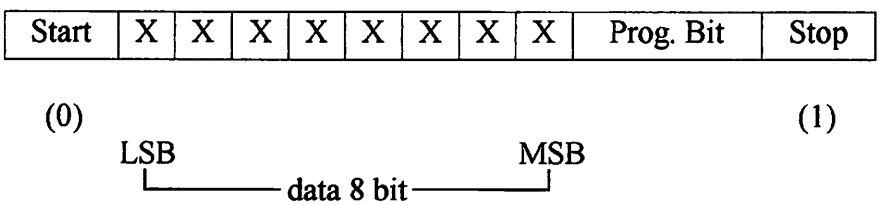
Sepuluh bit dikirim melalui TxD atau diterima melalui RxD. Format ke-10 bit tersebut adalah sebagai berikut:



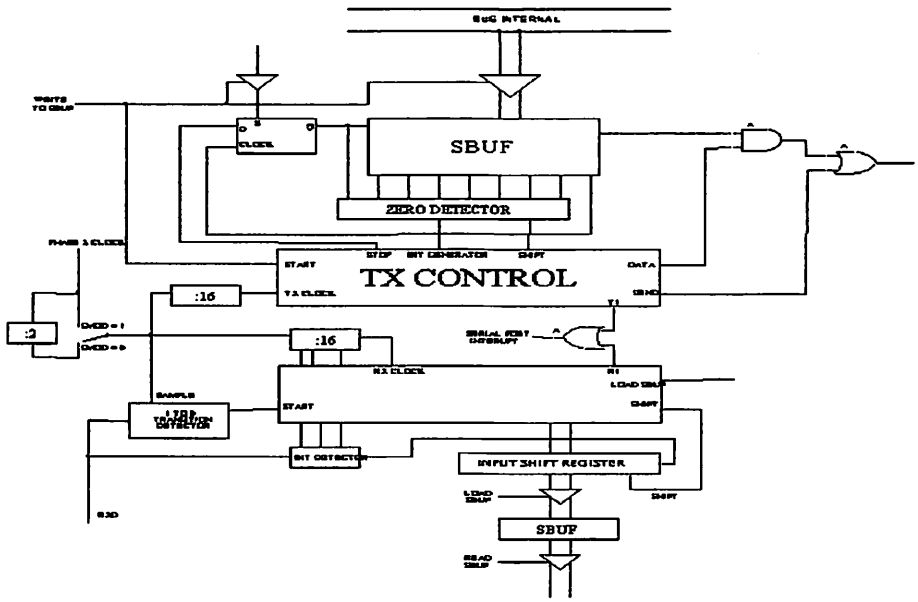
Pada saat duterima stop bit, bit ini akan masuk ke RB8 pada kontrol serial (SCON). *Baud rate* dapat diubah-ubah

2. 2. 3. Mode 2

Sebelas bit dikirim melalui TxD atau diterima melalui RxD. Format datanya adalah sebagai berikut :



Bit data ke-9 (TB8 dalam SCON) dapat menunjukkan nilai 0 atau 1. Sebagai contoh, bit paritas (P dalam PSW) dapat dimasukkan dalam TB8. *Baud rate* dapat diprogram menjadi 1/32 atau 1/64 dari frekuensi osilator.



Gambar. 2-8. Port Serial dalam Mode 2

2. 2. 4. Mode 3

Sebelas bit data dikirim melalui TxD dan diterima melalui RxD. Format datanya adalah sebagai berikut:

Start	X	X	X	X	X	X	X	X	Prog. Bit	Stop

(0) (1)

LSB MSB

data 8 bit

Pada kenyataannya mode 2 sama dengan mode 3 kecuali dalam masalah *baud rate*. Dalam mode 3, *baud rate* adalah variabel.

Keempat mode pengiriman ditandai denga instruksi yang menggunakan SBUF sebagai register tujuan. Penerimaan dalam mode 0 dibuat dengan R1 = 0

dan REN = 1 .Tabel 2-5 berikut ini memperlihatkan nilai yang harus diisikan pada SCON untuk masing-masing mode.

Tabel 2-6. Nilai untuk SCON untuk setiap mode.

Mode	SCON	Variabel SM2
0	10H	
1	50H	Single Processor
2	90H	(SM2 = 0)
3	D0H	
0	--	
1	70H	Multi Processor
2	B0H	(SM2 = 1)
3	F0H	

2. 2. 5. *Baud Rate*

Port serial pada mode 0 mempunyai baud rate yang tetap , yaitu 1/12 dari frekuensi osilator. Untuk menjalankan pada mode ini tidak ada timer/counter yaang dibutuhkan dalam penyetelan. Hanya register SCON yang diperlukan.

Port serial pada mode 1 memiliki *baud rate* yang dapat diubah. Baud rate dapat dihaslikan oleh Timer 1. Untuk melakukan hal ini *Timer* 1 digunakan dalam mode 2 *(auto reload).*

$$BaudRate = \frac{(K \times frek.osc)}{32 \times 12 \times [256 - TH1]}$$

Nilai K ditentukan oleh bit SMOD dalam *power control register* (PCON). Bila SMOD = 0 maka K = 1, bila SMOD = 1 maka K = 2. Bila diketahui baud rate, nilai TH1 dapat dicari melalui persamaan berikut ini:

$$TH1 = \frac{256 - (K \times frek.osc)}{(386 \times baud\_rate)}$$

Nilai TH1 harus dalam bentuk interger. Pembulatan nilai TH1 pada nilai interger terdekat tidak akan menghasilkan *baud rate* yang dikehendaki dalam hal ini pemakai dapat mengganti frekuensi kristal. Karena PCON tidak dapat dialamati per bit, untuk men- *set* PCON dilakukan dengan mengirimkan perintah

ORL PCON, #80H

Pada port serial mode 2, *baud rate* memiliki nilai tetap yaitu 1/32 atau 1/64 dari frekuesi osilator, tergantung pada nilai SMOD dalam register PCON. Pada mode ini tidak ada *timer* yang digunakan. Bila SMOD = 1 *baud rate*-nya 1/32 frekuensi osilator. Bila SMOD = 0, *baud rate*-nya 1/64 frekuensi osilator. Pada port serial mode 3, *baud rate* dapat diatur seperti dalam mode 1.

2. 3. Standart Interface RS-485

RS-485 biasa digunakan untuk menyediakan sinyal serial yang kuat sehingga sanggup mentransmisikan data hingga jarak 4000 ft (1200 m). Mampu melalui kabel transmisi yang cukup panjang pada *baud rate* yang tinggi dalam lingkungan listik yang potensial menimbulkan *noise* atau interferensi elektromagnetik yang tinggi.

RS-485 dapat menangani128 titik cabang ada satu saluran bersama dan bekerja dengan metode *half duplex*. Dalam setiap *chip* terdapat satu unit pengirim (D) dan satu unit pengaktif penerima RE *(Receive Enable),* RO *(Receive Output)* merupakan data output, DE *(Driver Enable)* merupakan pengaktif unit pengirim data, DI *(Data Input)* merupakan inputan data yang akan dikirimkan, A adalah pin

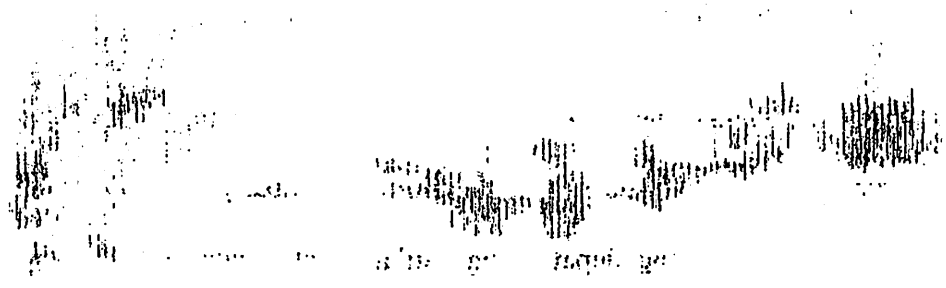
pengirim data menuju pin B RS-485 lawan komunikasi dan B adalah pin penerima data dari pin A RS-485 lawan komunikasi.

2. 4. Transducer

Sistem instrumentasi elektronika terdiri dari sejumlah komponen yang secara bersama-sama digunakan untuk melakukan suatu pengukuran dan mencatat hasilnya. Sebuah sistem instrumentasi umumnya terdiri dari tiga elemen utama, yaitu: peralatan masukan, pengkondisi sinyal (sinyal conditioning) atau peralatan pengolah, dan peralatan keluaran (output).

Besaran masukan pada kebanyakan sistem instrumentasi bukan besaran listrik.Untuk menggunakan metoda dan teknik listrik pada pengukuran, manipulasi atau pengontrolan, besaran yang bukan listrik ini diubah menjadi suatu sinyal listrik oleh sebuah alat yang disebut dengan transducer. Suatu definisi menyatakan bahwa transducer adalah sebuah alat yang dapat digerakkan oleh energi di dalam sebuah sistem transmisi, menyalurkan energi dalam bentuk yang sama atau dalam bentuk yang berlainan ke sistem transmisi kedua. Transmisi energi ini dapat berupa listrik, mekanik, kimia, optik (radiasi) atau thermal (panas).

Transducer dapat dikelompokkan berdasarkan pemakaiannya. Metode pengubahan energi, sifat dasar dari sinyal keluaran, dan lain-lain. Semua pengelompokkan ini biasanya memperlihatkan daerah yang saling melengkapi sedangkan pengelompokkan transducer berdasarkan prinsip listrik adalah sebagai berikut:



a. Transducer Pasif

Merupakan transducer yang memerlukan daya luar pada saat menghasilkan perubahan dalam sebuah parameter listrik seperti halnya tahanan, kapasitansi, dan sebagainya yang dapat diukur sebagai suatu perubahan tegangan atau arus.

b.Transducer Aktif

Merupakan jenis transducer yang memiliki pembangkit sendiri (self generation type), yang dapat menghasilkan suatu tegangan atau arus analog bila dirangsang dengan suatu bentuk fisis energi. Transducer ini tidak memerlukan daya luar pada saat bekerja.

Dengan demikian pemilihan transducer yang sesuai merupakan langkah pertama dan mungkin yang paling penting untuk memperoleh hasil-hasil yang teliti. Persyaratan ketelitian bagi sistem keseluruhan menentukan derajat terhadap masing-masing faktor yang berkontribusi terhadap ketelitian harus diperhitungkan. Sebagian faktor-faktor tersebut adalah:

- Parameter dasar transducer

  Merupakan jenis dan rangkuman pengukuran, sensitivitas, dan eksitasi.

- Kondisi fisik

  Memperlihatkan sambungan-sambungan mekanis dan elektrik, perlengkapan-perlengkapan pemasaran, tahanan korosi.

- Kondisi sekeliling

  Memperhatikan efek ketidak linieran, efek linieritas, respon frekuensi, resolusi.

- Kondisi lingkungan

  Merupakan pengaruh atau efek temperatur, percepatan, guncangan, dan getaran.

- Kesesuaian peralatan yang disertakan

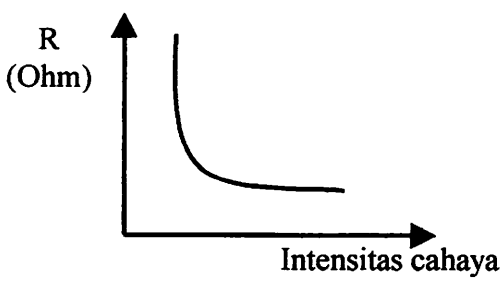
  Merupakan perlengkapan kesetimbangan nol, toleransi sensitivitas, penyesuaian impedansi.

2. 4. 1. Tranduser Cahaya

Tranduser Cahaya yang digunakan adalah LDR (Ligh Dependent Resistor).

Gambar. 2-9. Simbol LDR

Nilai resistansi LDR berbanding terbalik dengan besar cahaya yang diterima yaitu semakin besar intensitas cahaya yang diterima LDR semakin kecil nilai resistansinya, begitu sebaliknya apabila intensitas cahaya yang diterima LDR kecil maka nilai resistansinya besar. Seperti gambar karakteristik dibawah ini:



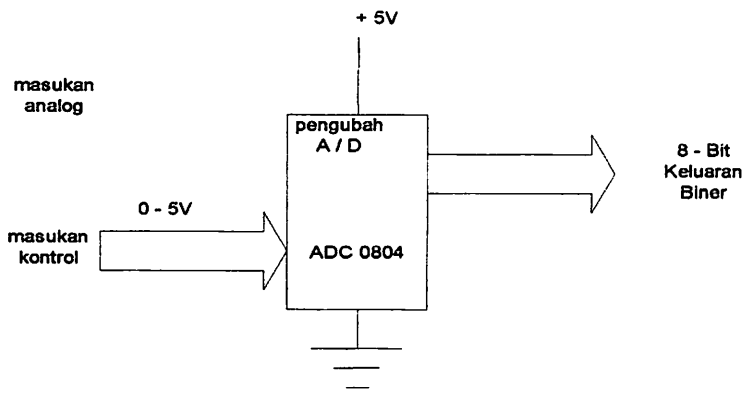
Gambar. 2-10. Karakteristik LDR

2. 5. ADC 0804

Analog To Digital Converter (ADC) berfungsi untuk mengubah level tegangan analog menjadi level tegangan digital yang akan digunakan pada pemrosesan informasi dan transmisi data.

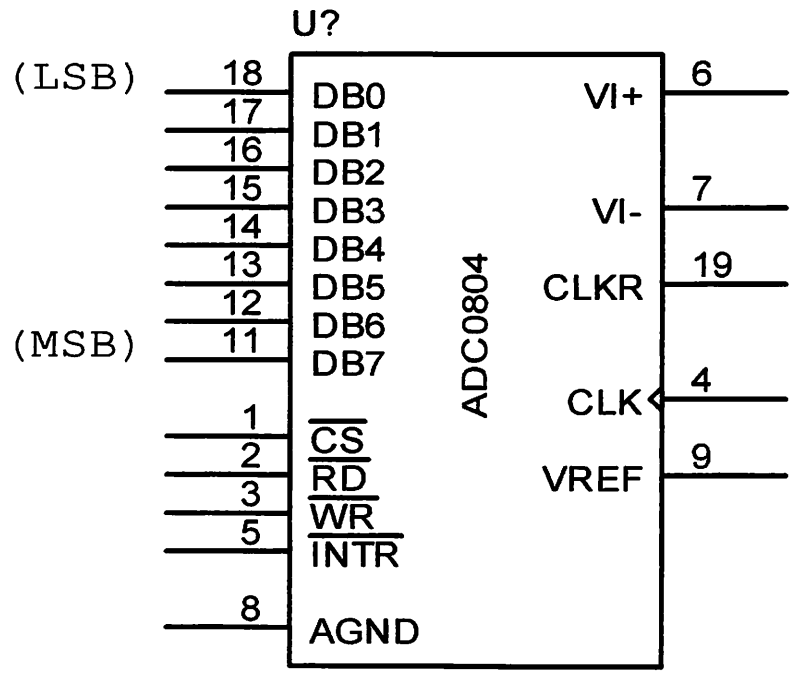
ADC yang digunakan dalam Tugas Akhir ini adalah ADC 0804 yang terdiri dari 20 pin IC DIP, yang dihasilkan oleh pabrik seperti National Semikonduktor. ADC 0804 ini beroperasi dari sebuah supply tunggal +5 Volt dan menerima sebuah input analog dengan range 0 Volt sampai 5 Volt.

Sebuah blok sederhana dari pengubah A/D Converter ditunjukkan pada gambar dibawah ini:



Gambar 2-11. Blok Diagram ADC 0804

ADC 0804 dirancang untuk berhubungan langsung dengan semua jenis mikrokontroler. Letak dan fungsi dari tiap pin ADC 0804 ditunjukkan pada gambar berikut.



Gambar 2-12. Konfigurasi Pin-Pin IC ADC 0804

Adapun fungsi sinyal pada pin-pin ADC 0804 adalah sebagai berikut :

- $\overline{\text{WR}}$ merupakan sinyal control yang digunakan sebagai sinyal Start Convertion yaitu jika pin ini diberi logika '0' maka ADC akan melakukan konversi tegangan analog pada pin VIN (+) dan VIN (-).
- $\overline{\text{INTR}}$ adalah sinyal output interrupt ADC yang memberikan logika '1' apabila ADC telah selesai melakukan pengkonversian. Sebaliknya selama waktu konversi (busy) sinyal ini akan berlogika '0'.
- $\overline{\text{RD}}$ adalah sinyal input control yang digunakan untuk meng-enable- kan keluaran data DB0-DB7 setelah terjadi pengkonversian.
- $\overline{\text{CS}}$ sebagai sinyal input control Chip Select. Sinyal ini harus diberi logika '0' agar IC ADC 0804 dapat berfungsi.

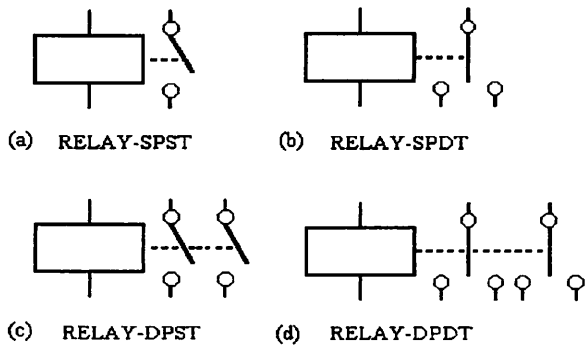
- **DB0-DB7** merupakan keluaran data digital 8-bit dari ADC yang juga sebagai besaran biner yang terkonversi dari tegangan analog.
- **VCC**, pin ini dihubungkan dengan catu daya 5 Volt sekaligus berfungsi sebagai masukan tegangan referensi untuk ADC.
- **CLK-R** dan **CLK-IN** adalah masukan dari rangkaian R-C sebagai sumber pembangkit clock. Clock sendiri digunakan sebagai pengatur irama kerja (timing) dari proses konversi ADC. Besarnya frekuensi clock yang memungkinkan ADC ini bekerja adalah berkisar antara 100 sampai 1460 KHz.
- **A-GND** dan **D-GND** masing-masing sebagai Analog Ground dan Digital Ground. Kedua pin ini harus dihubungkan dengan 0 Volt dari catu daya.

2.6. Relay

Relay adalah suatu perangkat saklar *(switch)* yang dioperasikan oleh gaya elektromagnetik yang dihasilkan oleh kumparan yang berada didalamnya.

Relay ini pada umumnya digunakan untuk menyambung dan memutuskan hubungan antara suatu bagian dengan bagian lainnya dalam suatu rangkaian elektronik, selain itu juga dimaksudkan untuk mengisolasi *switching* antara tegangan catu tinggi dengan catu rendah. Kerugian yang ditemui pada relay yaitu adanya waktu tanggapan *(respons time)* saat on maupun saat *off.* yang relatif lambat dan serta adanya efek induksi balik sesaat setelah relay *off.* Oleh sebab itu maka antara rangkaian pengendali dan relay perlu di-isolasi dengan rangkaian peng-isolasi. Relay terdiri dari 4 jenis relay, yaitu:

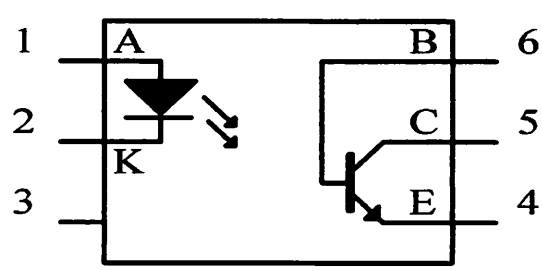
- DPDT *(Double Pole, Double Throw)*
- SPDT *(Single Pole, Double Throw)*
- DPST *(Double Pole, Single Throw)*
- SPST *(Single Pole, Single Throw)*



Gambar 2-13. Jenis-jenis Relay

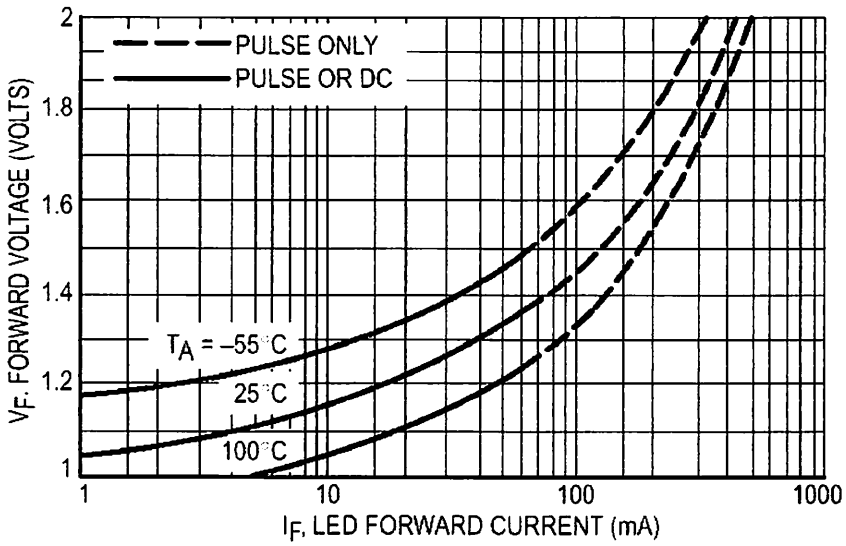
2.7. Optoisolator

Optoisolator berfungsi untuk mengisolasi antara suatu bagian atau rangkaian dengan bagian yang lain. Tujuan pengisolasian ini adalah untuk mencegah agar tidak terjadi kerusakan komponen pada suatu bagian sebagai akibat dari munculnya tegangan tinggi yang tidak diinginkan pada bagian lainnya. Dalam tugas akhir ini digunakan optoisolator 4N25 yang dapat mengisolasi tegangan sampai dengan 5300 volt pada sisi *photodioda.*



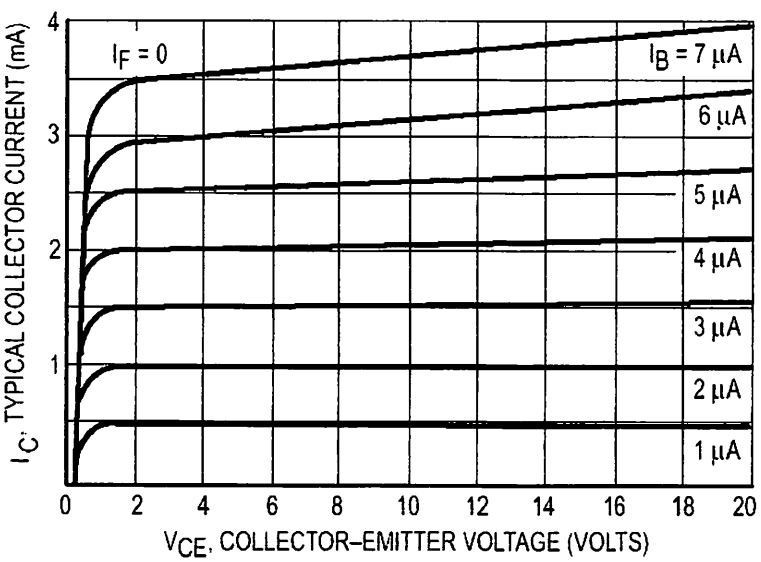
Gambar 2-14. Konfigurasi Pin *Optoisolator* 4N25

Grafik karakteristik dari LED *Optoisolator* diperlihatkan gambar berikut :



Gambar 2-15. Perbandingan Tegangan Maju LED dengan Arus Maju

Sedangkan grafik karakteristik dari transistor *optoisolator* adalah sebagai berikut :



Gambar 2-16. Grafik karakteristik transistor *optoisolator*

2.8. Transistor Sebagai Saklar Elektronik

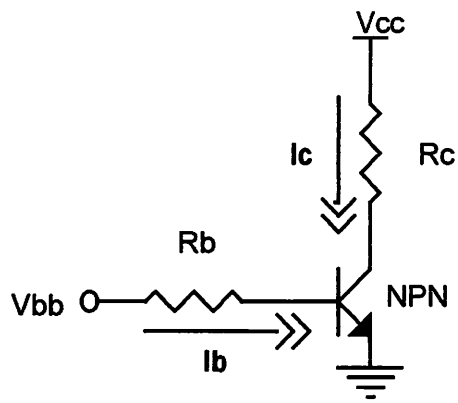
Suatu transistor bila ingin digunakan sebagai saklar elektronik *(connect)* maka harus dioperasikan dalam keadaan saturasi. Pada keadaan ini tegangan antara kaki kolektor dan emitor dianggan 0 Volt (ideal).

$$Vbb = (Ib \bullet Rb) + Vbe$$

$$\beta dc = \frac{Ic}{Ib}$$

$$Vcc = Ic \times Rc$$

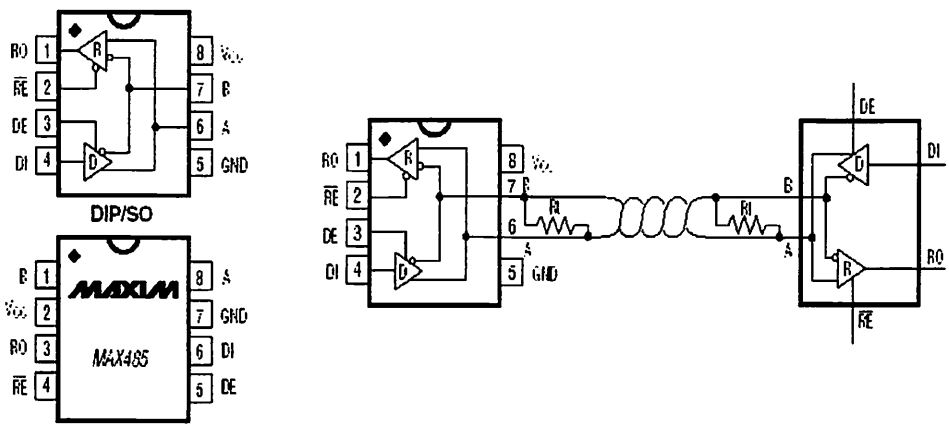
Persamaan-persamaan tersebut akan berlaku untuk rangkaian berikut :



Gambar 2-17. Transistor Sebagai Penguat Arus

2.9. IC MAX 485

IC MAX485 ini merupakan IC penguatan sinyal *(buffer)* yang berfungsi sebagai penguat sinyal data format serial yang diterima dari P3.1 (TxD) pada mikrokontroler. IC ini mampu mentransmisikan data serial sejauh 4000 *feet* atau 1200 meter.

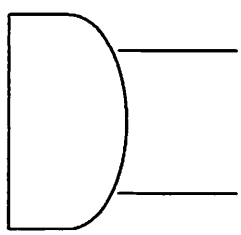


Gambar 2-18. Konfigurasi Pin pada IC MAX485

2.10. BUZZER

Buzzer mempunyai fungsi sebagai tanda / isarat dalam bentuk suara sehingga akan dengan cepat mengetahui akan adanya kerusakan.

Buzzer yang dulu dipakai adalah buzzer yang berupa koil yang bila dialiri arus akan menarik pemukul kelogam dan menghasilkan bunyi, tetapi saat ini buzer sudah berupa komponen kecil yang hanya menngunakan speaker kecil yang berupa dua buah lapisan elektroda yang biasa disebut dengan piezoelektrik yang banyak dipakai untuk tweter salon.



Gambar 2-19. BUZZER

2.11. LCD M1632

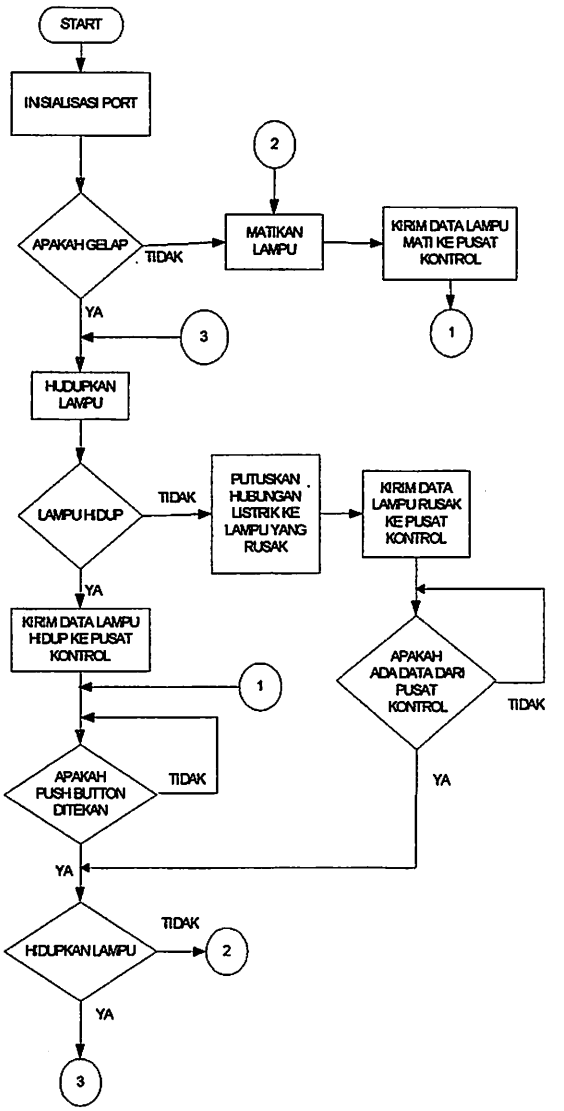
LCD M1632 adalah sebuah modul LCD dot matrix dengan kebutuhan daya kecil, dilengkapi dengan panel LCD bertingkat kontras cukup tinggi dan pengontrol LCD internal. Pengontrol mempunyai pembangkit karakter ROM/RAM dan penampil data RAM. Semua fungsi display diatur oleh instruksi dan modul dapat dengan mudah diantar-mukakan dengan unit mikrokontroller. Karakteristik daripada LCD dot-matrik adalah sebagai berikut :

- 16x2 karakter dengan 5x7 dot-matrik + kursor
- ROM generator karakter dengan 192 type karakter
- RAM generator karakter dengan 8 type karakter (untuk program write)
- 80x8 bit RAM data display
- Dapat diinterfacekan dengan kemungkinan mikrokontroller 4 bit atau 8 bit
- RAM data dan RAM generator karaktor yang dapat dibaca dari mikrokontroller.
- +5 Volt single power supply
- Range temperatur operasi 0°C sampai 50°C
- Memiliki beberapa fungsi instruksi :

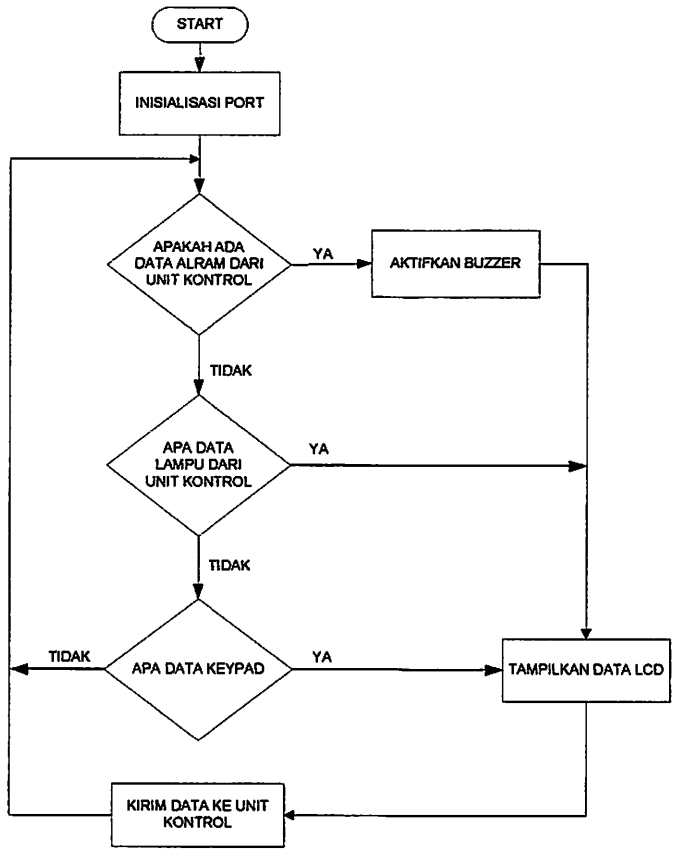
  Display Clear, Cursor Home, Display ON/OFF, Cursor ON/OFF, Display Character Blink, Cursor Shift, dan Display Shift.
- Osilator internal.
- Secara otomatis akan reset saat catu daya dinyalakan.

3. 3. Perancangan Perangkat Lunak *(Software)*

3. 3. 1. Sistem Unit Kontrol



3. 3. 2. Sistem Pusat Kontrol



BAB IV

PENGUJIAN ALAT

4. 1. Pendahuluan

Untuk mengetahui apakah alat yang telah dirancang dapat bekerja sesuai dengan fungsi yang diharapkan, maka perlu melakukan pengujian sistem alat. Dalam rangka pengujian tersebut, pada bab ini diuraikan percobaan yang dilakukan untuk mengetahui respon dan kerja dari keseluruhan alat yang telah dirancang tersebut.

4. 2. Pengujian Pada Bagian-bagian Sub-sistem Alat.

Pengujian bagian sub-sistem dimaksudkan untuk melihat cara kerja dari blok bagian yang diuji sehingga dapat mengurangi resiko kesalahan pada saat peng-integrasian rangkaian.

4. 2. 1. Rangkaian Sensor Cahaya

a. Tujuan

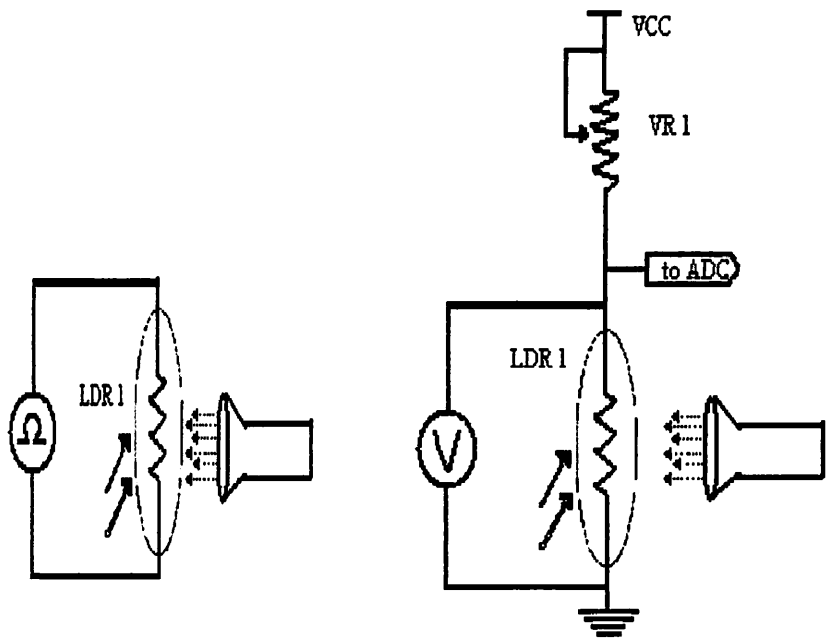
Untuk menguji kepekaan LDR sebagai sensor cahaya terhadap perubahan intensitas cahaya.

b. Peralatan yang Digunakan

- Multitester
- Catu daya
- Rangkaian sensor cahya

c. Langkah-langkah Pengujian

- Menghubungkan rangkaian dengan catu daya.
- Memberi konfigurasi input intensitas cahaya yang beragam.
- Mengukur resistansi LDR dan tegangan output rangkaian.



Gambar 4-1. Pengujian dan Pengukuran pada Rangkaian Sensor Cahaya.

Pada rangkaian sensor cahaya digunakan sebuah LDR1 yang diseri dengan VR1 yang diseting pada nilai 10 KΩ. Tegangan sumber sebesar 5 vol. Dari hasil pengujian diperoleh nilai resistansi LDR1 berkisar antara 4 MΩ hingga 1,5 KΩ dan tegangan output sensor antara 4,9 volt sampai 0,6 volt. Data selengkapnya pada table berikut.

d. Hasil Pengujian

Dari pengujian diperoleh output rangkaian sensor cahaya adalah :

Tabel 4-1. Hasil Pengukuran Pada Rangkaian Sensor Cahaya

Intensitas Cahaya	Resistansi LDR1 (KΩ)	Tegangan Output (volt)
GELAP	4000	4,92
TERANG	1,54	0,66

4. 2. 2. Pengujian Pada Rangkaian ADC

a. Tujuan

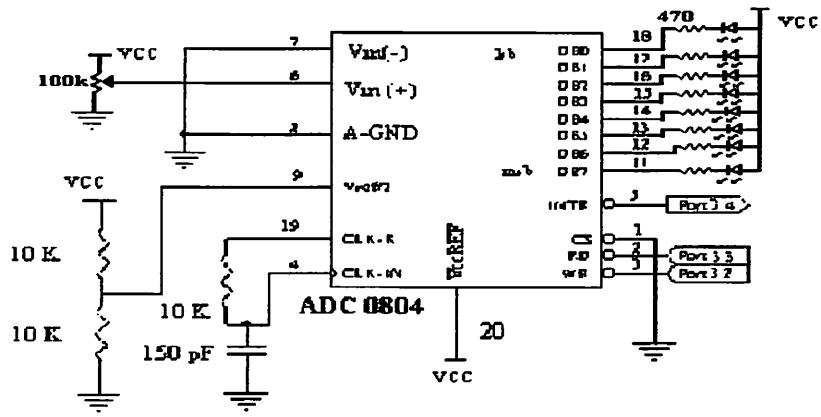
Untuk mengetahui kombinasi logika keluaran dari ADC terhadap input tegangan yang diberikan.

b. Peralatan yang digunakan

- Multitester
- LED indikator
- Rangkaian ADC 0804
- Catu daya

c. Langkah-langkah Pengujian

- Menghubungkan rangkaian dengan catu daya.
- Menghubungkan tiap-tiap output ADC dengan LED indikator
- Memberi konfigurasi inputan tegangan yang bervariasi antara 0 -5 volt.
- Mengamati perubahan nyala LED indikator untuk tiap-tiap nilai tegangan yang diberikan.



Gambar 4-2. Pengujian Pada Rangkaian ADC

d. Hasil Pengujian

Tabel 4-2. Hasil Pengukuran Pada Rangkaian ADC

NO	V in (volt)	Output ADC							
		0	1	2	3	4	5	6	7
1	0,00	0	0	0	0	0	0	0	0
2	0,54	0	0	0	1	1	1	0	0
3	1,00	0	0	1	1	0	1	0	0
4	1,53	0	1	0	0	1	1	1	0
5	2,02	1	1	1	0	0	1	1	1
6	2,50	1	0	0	0	0	0	0	0
7	3,02	1	0	0	1	1	0	1	0
8	3,55	1	0	1	1	0	1	0	1
9	4,07	1	1	0	1	0	0	0	0
10	5,00	1	1	1	1	1	1	1	1

Pada saat tegangan sebesar 0 volt semua led menyala dan pada saat tegangan 5 volt semua led tidak menyala.

4. 2. 3. Pengujian Pada Rangkaian Sensor Lampu.

a. Tujuan

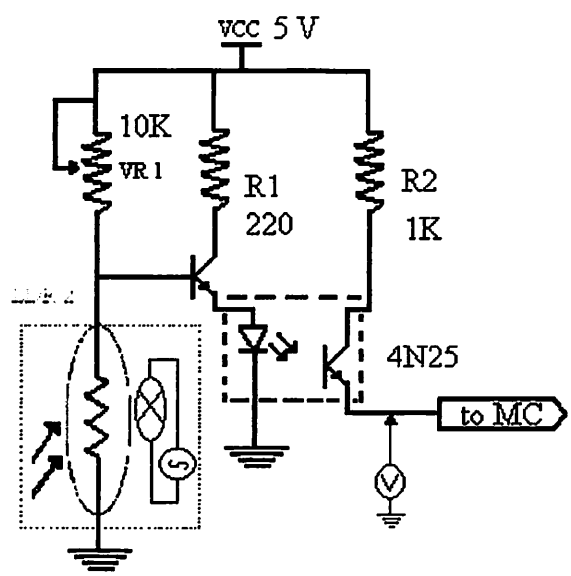
Tujuannya untuk mengetahui tanggapan LDR2 terhadap keadan lampu.

b. Peralatan yang Digunakan

- Rangkaian Sensor Lampu
- Lampu AC 220 V
- Catu daya
- Multitester

c. Langkah-langkah Pengujian

- Menempelkan LDR2 ke lampu, diusahakan LDR2 tidak terpengaruh cahaya luar.
- Menghubungkan Rangkaian dengan catu daya.
- Mengukur tegangan keluaran untuk keadaan lampu hidup dan lampu mati.



Gambar 4-3. Pengujian Pada Rangkaian Sensor Lampu

d. Hasil Pengujian

Tabel 4-3. Hasil Pengukuran Pada Rangkaian Sensor Lampu

KONDISI LAMPU	TEGANGAN OUTPUT (volt)
Lampu Hidup	**0,2**
Lampu Rusak / Mati	**4,9**

Setelah langkah-langkah pengujian diatas maka didapat hasil pengujian sebagai berikut:

- Pada lampu hidup diperoleh tegangan 0,2 volt yang merupakan nilai kondisi 'low'.
- Pada lampu mati diperoleh tegangan 4,9 volt yang merupakan kondisi 'high'.
- Untuk lampu rusak (putus) juga akan diperoleh tegangan 4,9 volt mewakili kondisi 'high'. Letak perbedaan lampu mati dan lampu rusak diketahui dengan kondisi relay yang berbeda yaitu untuk lampu mati relay dalam keadaan tidak terhubung, sedangkan lampu rusak (putus) relay pada kondisi terhubung tetapi lampu tidak menyala.

4. 2. 4. Pengujian Pada Rangkaian Driver Relay

a. Tujuan

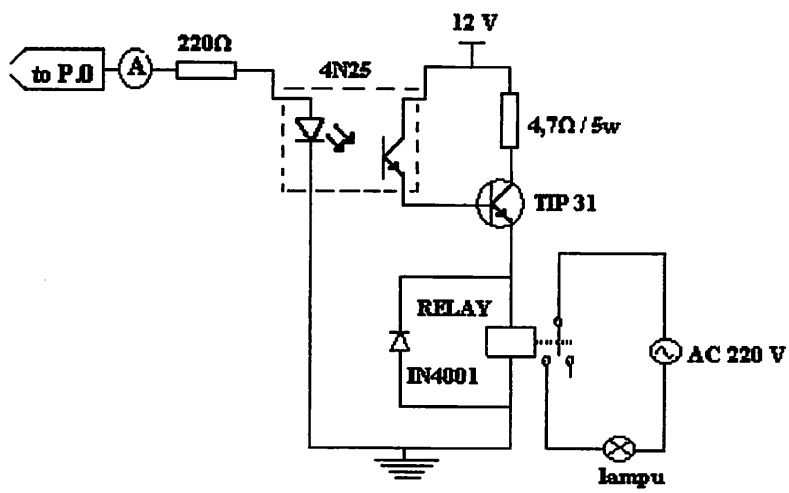
Untuk mengetahui apakah bagian driver relay ini sudah sesuai dengan apa yang direncanakan.

b. Peralatan yang Digunakan

- Power Supply 12 V
- Multimeter
- Rangkaian driver relay

c. Langkah-langkah Pengujian

- Menghubungkan bagian driver relay dengan catu daya 12 V
- Mengukur arus basis pada transistor pada kondisi ada beban (relay aktif) dan pada kondisi tidak ada beban (relay tidak aktif).
- Mengamati dan mencatat hasil pengujian.



Gambar 4-4.Pengujian pada Bagian Driver Relay

d. Hasil Pengujian

Tabel 4-4. Hasil Pengukuran pada Bagian Driver Relay

Kondisi	V_{CC} (V)	I_f (mA)
Relay tidak aktif	12	0 - 0,6
Relay aktif		0,7 – 3,8

4. 3. Pengujian pada Keseluruhan Sistem Alat

a. Tujuan

Untuk mengetahui cara kerja keseluruhan alat yang sudah di-integrasikan bagian-bagiannya

b. Peralatan yang Digunakan

- Bagian Pusat Kontrol
- Bagian Unit Kontrol
- Lampu AC 220 Volt

c. Langkah-langkah Pengujian

- Merangkai seluruh bagian-bagian blok sesuai dengan urutan sehingga menjadi sebuah sistem yang terintegrasi.
- Menghubungkan seluruh sistem dengan catu daya.
- Mengkondisikan LDR1 pada kondisi terang dan gelap.
- Mengkondisikan LDR2 untuk keadan lampu rusak.
- Mengamati tanggapan dan cara kerja alat pada tiap-tiap kondisi seperti diatas.

d. Hasil Pengujian

- Pada kondisi Terang.

  Output tegangan yang dihasilkan Rangkaian sensor intensitas cahaya sangat kecil sekitar 0,5 volt yang akan mengisaratkan untuk tidak mengaktifkan relay, lampu mati.

- Pada kondisi Gelap.

  Rangkaian sensor cahaya akan menghasilkan tegangan yang mendekati 5 volt yaitu sekitar 4,9 volt, relay diaktifkan dan lampu hidup.

- Pada kondisi antara gelap dan terang.

  Untuk kondisi lampu hidup " high " (keadaan gelap) output ADC ditetapkan berkisar antara 1 volt sampai 4,9 volt (mendekati 5 volt). Sedangkan untuk kondisi Lampu Mati " Low " (keadaan Terang) output ADC ditetapkan antara 0 volt – 0,99 volt.

- Pada kondisi lampu rusak.

  Lampu akan dikenali dalam keadaan rusak apabila keadaan gelap kondisi "high" tegangan yang dihasilkan rangkaian sensor lampu sebesar 4,9 volt. Keadaan ini akan mengaktifkan buzzer dan ditampilkan di LCD.

Dari data yang didapat pada pengujian diatas maka dapat diketahui bahwa sistem dan semua bagian sub–sistem telah berjalan lancar sesuai dengan perancangan dan sesuai dengan apa yang telah direncanakan.

BAB V

PENUTUP

5. 1. Kesimpulan

Berdasarkan perencanaan, pembuatan dan pengujian pada tiap-tiap sub-sistem, maka dapat diambil kesimpulan sebagai berikut:

1. Ldr dapat difungsikan sebagai pengindra yang serba guna, pada alat ini ldr di fungsikan sebagai pengindra intensitas cahaya dan untuk mengenali keadaan lampu.
2. Mikrokontroler AT89S51 dapat diaplikasikan sebagai pengontrol lampu otomatis yang merupakan pusat pengontrol yang menetapkan dan menentukan keadaan lampu sesuai kondisi yang telah diprogram.
3. RS 485 memungkinkan alat pengontrol lampu ini untuk berkomunikasi jarak jauh. Keistimewaannya mampu melakukan multi point jaringan komunikasi, standarnya menetapkan 32 pengirim dan 32 penarima pada dua saluran kawat.
4. ADC 0804 diaplikasikan untuk menterjemahkan keluaran sensor cahaya dari analog menjadi digital sehingga bisa dikenali oleh AT89S51. Data digital yang dihasilkan adalah data biner 8 bit.
5. Sensor cahaya pada alat ini dirancang untuk mengenali keadaan gelap 4,9 volt dan keadaan terang 0,6 volt.
6. Kehandalan system ini yaitu mempermudah pekerjaan pihak pengelola gedung dalam menangani permasalahan penerangan.

5. 2. Saran-saran

Mengingat masih adanya kelemahan dan kekurangan dari perancangan alat ini, maka dapat disarankan agar :

1. Jumlah lampu yang dikontrol dapat diperbanyak dengan menggunakan PPI *(Programmable Peripheral Interface)* 8255 menjadi 24 output.
2. Untuk penggunaan alat ini pada gedung luas yang mempunyai banyak lampu dan bisa diindra kondisi lampunya, memerlukan LDR yang banyak pula, sehingga kurang efisien tetapi sangat akurat.
3. Alat ini pada nantinya dapat dikembangkan lagi dengan menambahkan kamera, sehingga memungkinkan untuk mengetahui kondisi ruangan pada gedung.
4. Untuk tampilan display yang semulanya terbatas dapat dikembangkan dengan menggunakan perangkat computer.

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INSTITUT TEKNOLOGI NASIONAL MALANG
FAKULTAS TEKNOLOGI INDUSTRI
JURUSAN TEKNIK ELEKTRO S – 1
KONSENTRASI TEKNIK ELEKTRONIKA

LEMBAR BIMBINGAN SKRIPSI

1.	Nama Mahasiswa	: R. Yunri Putra Alyadi
2.	NIM	: 98.17.035
3.	Jurusan	: Teknik Elektro S-1
4.	Konsentrasi	: Teknik Elektronika
5.	Judul Skripsi	: Perencanaan dan Pembuatan Alat Pengontrol Lampu Otomatis Berdasarkan Kondisi Cahaya Berbasis Mikrokontroler AT89S51
6.	Tanggal Pengajuan Skripsi	: 14 Februari 2005
7.	Selesai Penulisan Skripsi	: 5 April 2006
8.	Pembimbing I	: Ir. Widodo Pudji M, MT
9.	Dievaluasi dengan Nilai	: A 80 (delapan puluh)

Mengetahui,
Ketua Jurusan Teknik Elektro

(Ir. F. Yudi Limpraptono, MT.)
NIP. 131 991 182

Diperiksa dan disetujui
Dosen Pembimbing

(Ir. Widodo Pudji M, MT.)
NIP. P 102 870 0171

INSTITUT TEKNOLOGI NASIONAL MALANG
FAKULTAS TEKNOLOGI INDUSTRI
JURUSAN TEKNIK ELEKTRO S – 1
KONSENTRASI TEKNIK ELEKTRONIKA

FORMULIR PERBAIKAN SKRIPSI

Nama : R. Yunri Putra Alyadi
NIM : 98.17.035
Masa Bimbingan : 27 Juli 2005 s/d 27 Januari 2006
Judul : Perencanaan dan Pembuatan Alat Pengontrol Lampu Otomatis Berdasarkan Kondisi Cahaya Berbasis Mikrokontroler AT89S51.

No.	Tanggal	Uraian	Paraf
1.	7 Oktober 2005	1. Daftar Isi 2. Abtraksi 3. Kesimpulan 4. Pengujian Data	

Disetujui,

Penguji I

(Ir. F. Yudi Limpraptono, MT.)
NIP. Y.103 9500 247

Penguji II

(Irmalia Suryani F, ST.)
NIP. 103 0100 365

Mengetahui,
Dosen Pembimbing

(Ir. Widodo Pudji M, MT.)
NIP. P 102 870 0171

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JURUSAN TEKNIK ELEKTRO

Formulir Perbaikan Ujian Skripsi

Dalam pelaksanaan Ujian Skripsi Jenjang Strata 1 Jurusan Teknik Elektro Konsentrasi T. Energi Listrik / T. Elektronika, maka perlu adanya perbaikan skripsi untuk mahasiswa :

NAMA : R. Yunri P. A
N I M : 9817034
Perbaikan meliputi :

① Tambahkan daftar isi
② Abstrak.
③ Kesimpulan, harus dari hasil penyajian.
→ Uji prosentase data melalui RS 485 dengan proses berkesinambungan.
→ Uji sensor cahaya.
→ Uji kehandalan LDR.

Malang, 200

(_____)

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FAKULTAS TEKNOLOGI INDUSTRI
JURUSAN TEKNIK ELEKTRO

Formulir Perbaikan Ujian Skripsi

Dalam pelaksanaan Ujian Skripsi Janjang Strata 1 Jurusan Teknik Elektro Konsentrasi T. Energi Listrik / T. Elektronika, maka perlu adanya perbaikan skripsi untuk mahasiswa :

NAMA : R. Yunri Putra A
N I M : 98.17.038
Perbaikan meliputi :

- Pengujian data diubah +
- kesimpulan diubah

Malang, 200

(Irmalia ST)

INSTITUT TEKNOLOGI NASIONAL
JL. BENDUNGAN SIGURA-GURA 2
MALANG

FORMULIR BIMBINGAN SKRIPSI

Nama : R. Yundri Putra A.
Nim : 9817035
Masa Bimbingan : 27-Jul-2005 s/d 27-Jan-2006
Judul Skripsi : Perencanaan dan pembuatan alat pengontrol lamp . otomatis berdasarkan kondisi cahaya berbasis Mikrokontroller AT89S51

NO	Tanggal	Uraian	Paraf Pembimbing
1.		Konsultasi Bab I, II	
2.		Revisi Bab I, II	
3.		Acc Bab I, II	
4.		Konsultasi Bab III	
5.		Konsultasi Bab IV	
6.		Acc Bab III & IV	
7.		Acc Seminar Hasil	
8.		Acc Ujian Skripsi	
9.			
10.			

Malang, 2005
Dosen Pembimbing

Ir. Widodo Pudji M., MT

Form. S-4a

Transcription: Bob I, II

Revis: Bob I, II

Acc Bob I, II

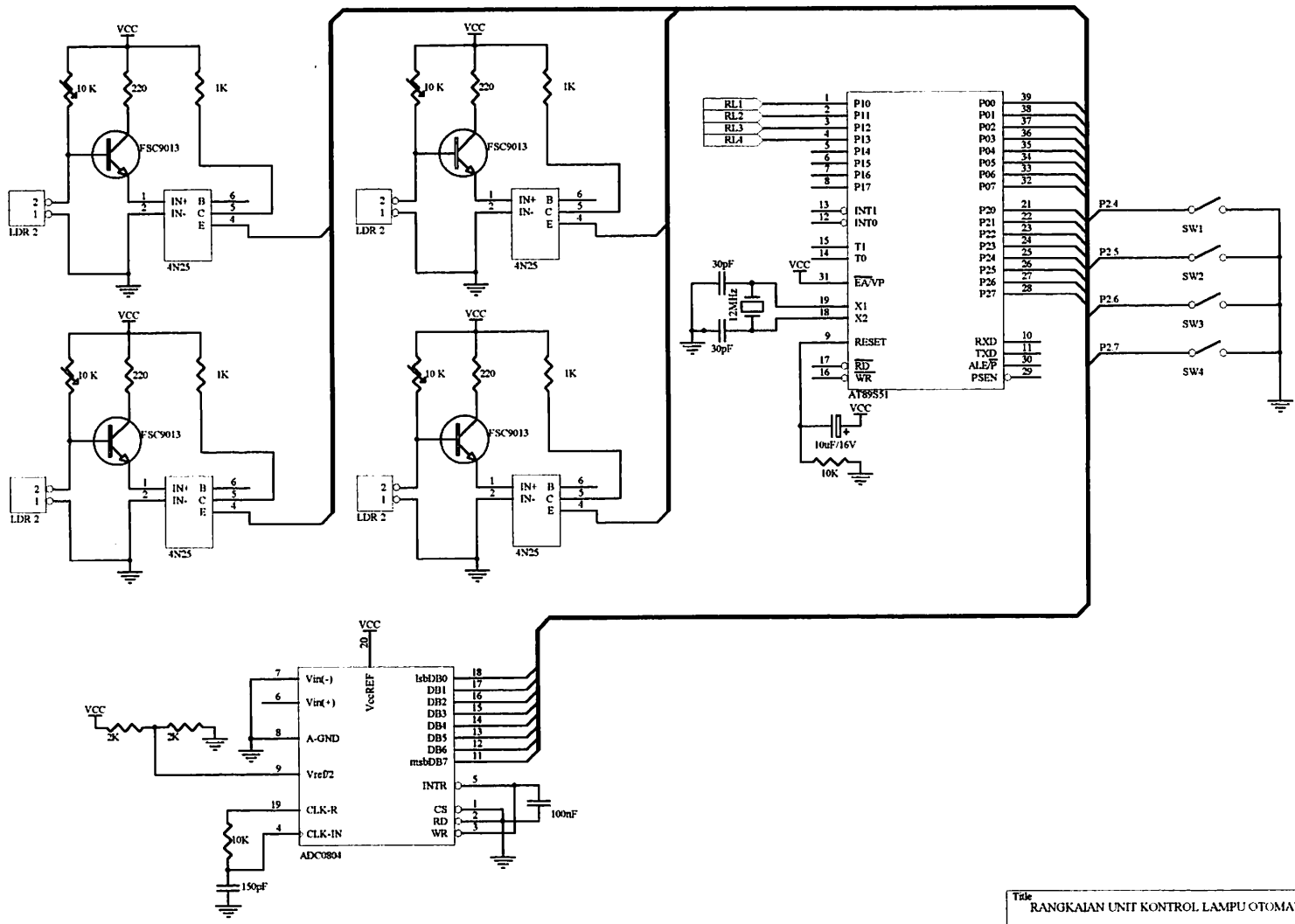
Transmittal Bob III

Transmittal Book IV

Acc Bob III & IV

Acc Supervisor Trans

Acc Ulysses Skrips



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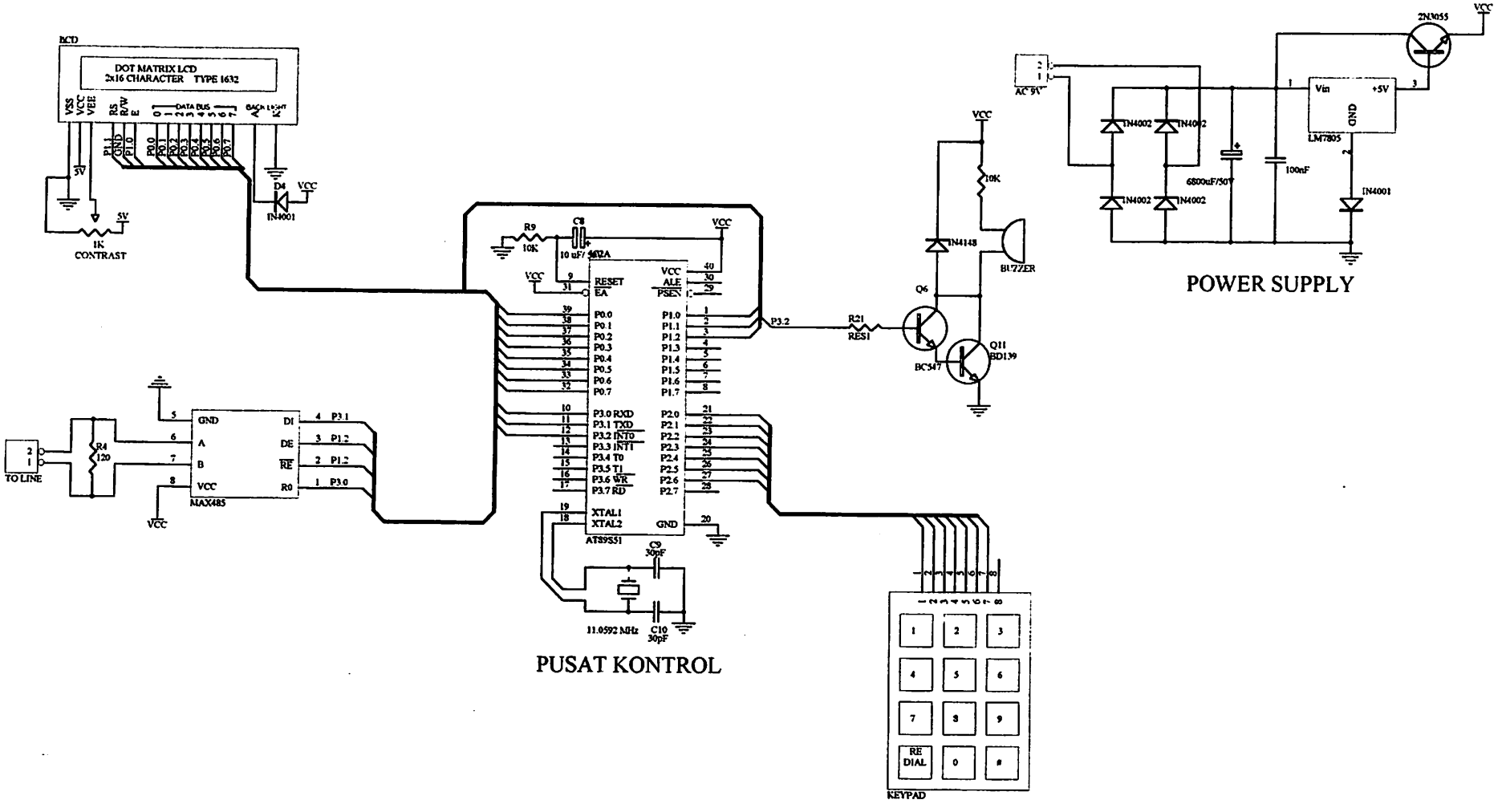

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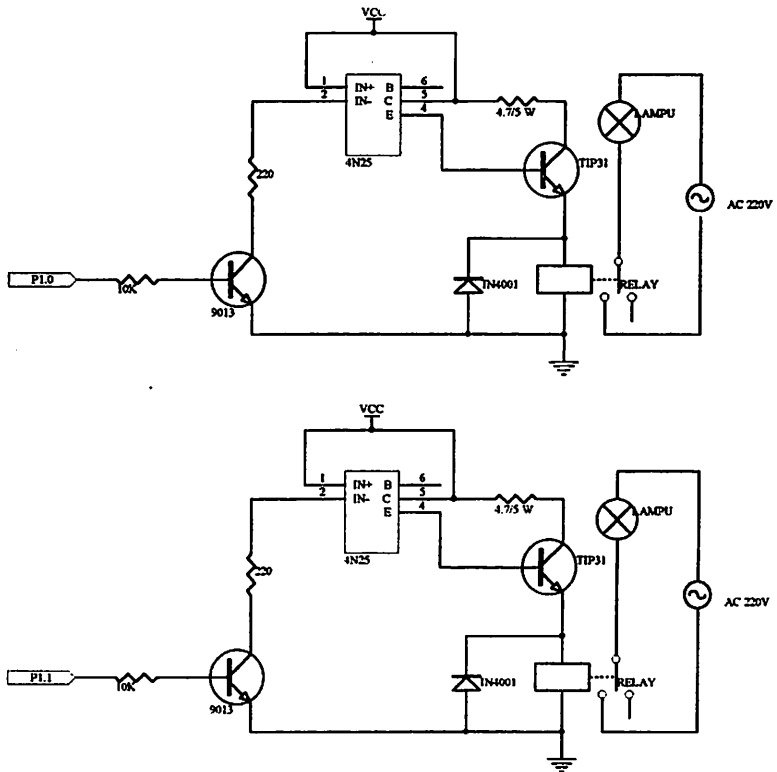

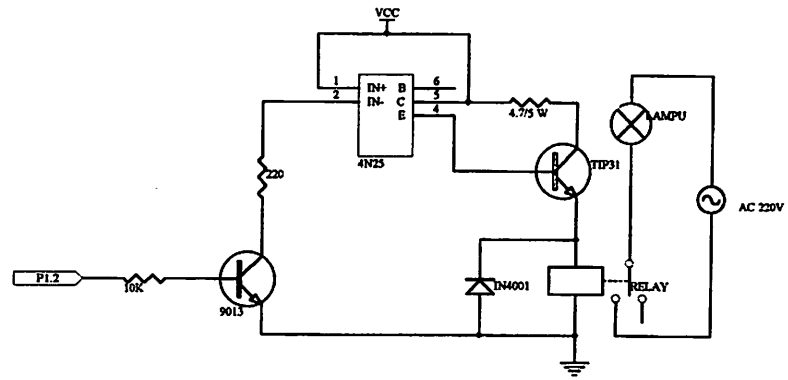

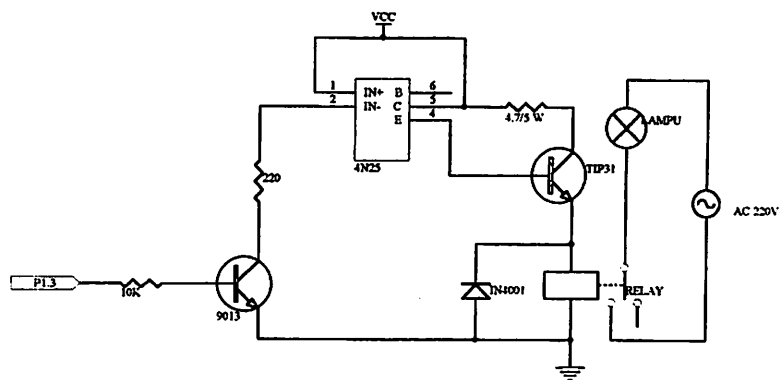

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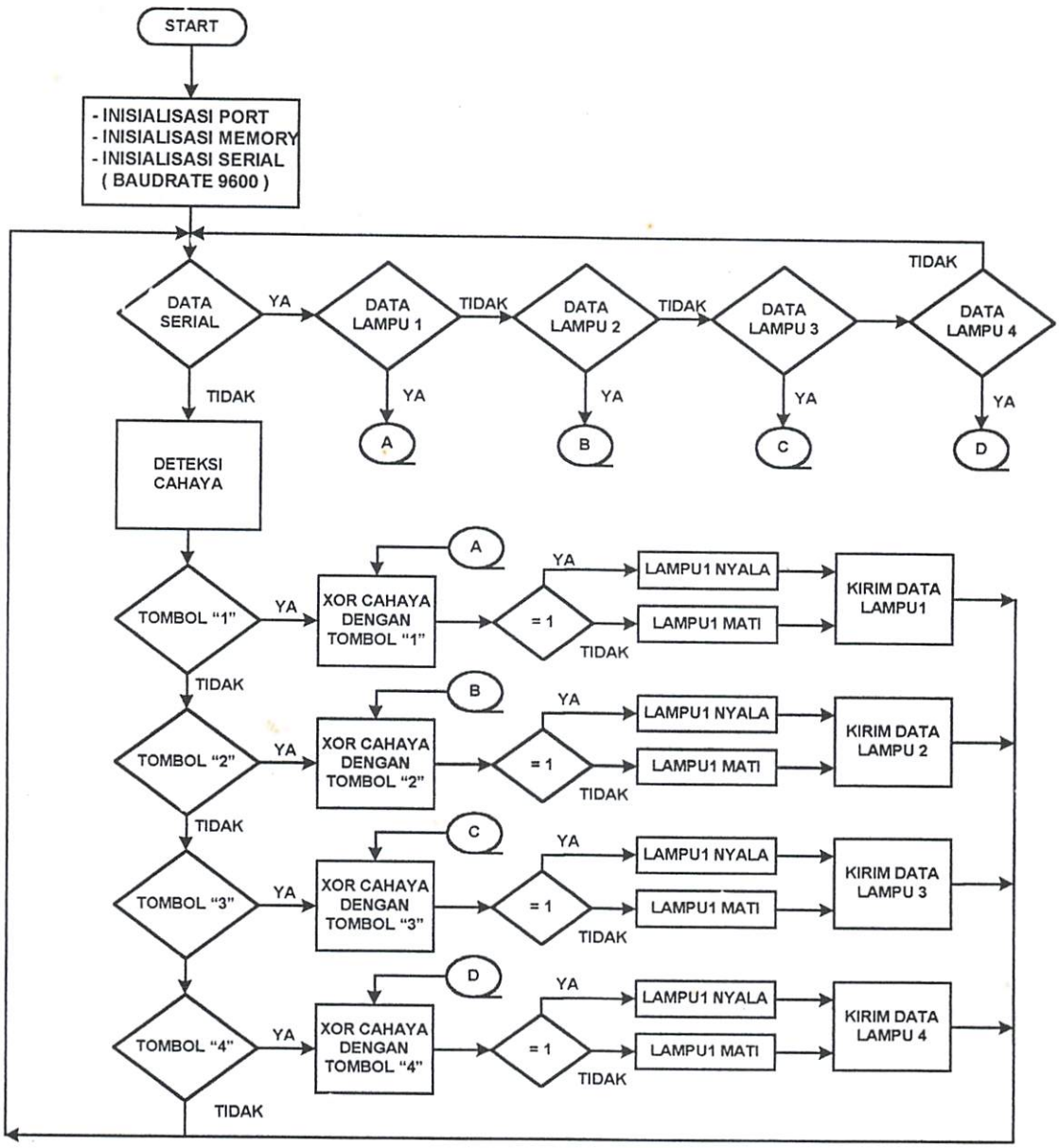
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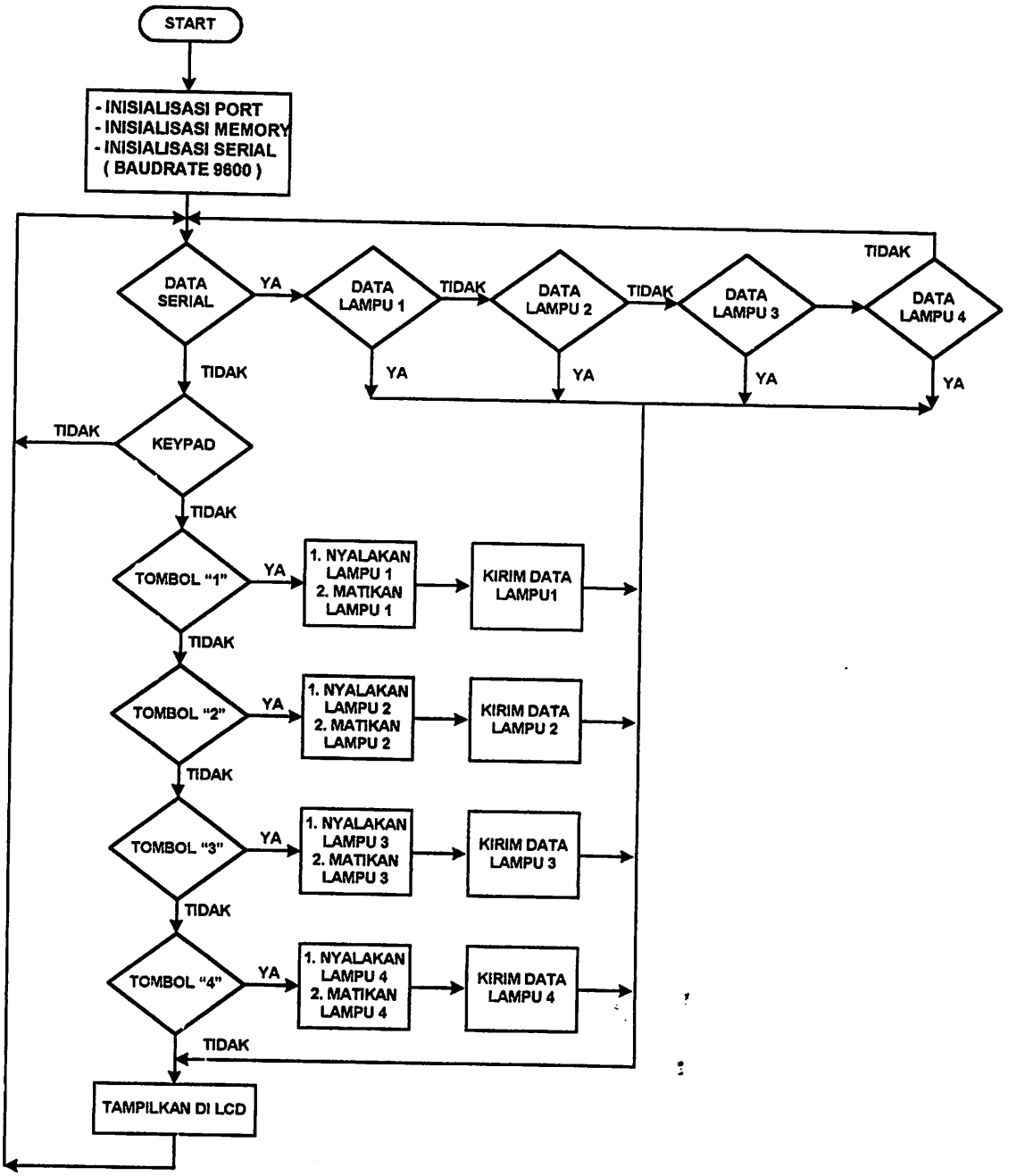
- INISIALISASI PORT
- INISIALISASI MEMORY
- INISIALISASI SERIAL
(BAUDRATE 9600)
DATA SERIAL
YA
DATA LAMPU 1
TIDAK
DATA LAMPU 2
TIDAK
DATA LAMPU 3
TIDAK
DATA LAMPU 4
TIDAK
TIDAK
YA
A
B
C
D
DETEKSI CAHAYA
TOMBOL "1"
TOMBOL "2"
TOMBOL "3"
TOMBOL "4"
XOR CAHAYA DENGAN TOMBOL "1"
XOR CAHAYA DENGAN TOMBOL "2"
XOR CAHAYA DENGAN TOMBOL "3"
XOR CAHAYA DENGAN TOMBOL "4"
= 1
LAMPU1 NYALA
LAMPU1 MATI
KIRIM DATA LAMPU1
KIRIM DATA LAMPU 2
KIRIM DATA LAMPU 3
KIRIM DATA LAMPU 4


START
- INISIALISASI PORT
- INISIALISASI MEMORY
- INISIALISASI SERIAL
(BAUDRATE 9600)
DATA SERIAL
YA
DATA LAMPU 1
TIDAK
DATA LAMPU 2
TIDAK
DATA LAMPU 3
TIDAK
DATA LAMPU 4
TIDAK
YA
YA
YA
YA
TIDAK
KEYPAD
TIDAK
TIDAK
TOMBOL "1"
YA
1. NYALAKAN LAMPU 1
2. MATIKAN LAMPU 1
KIRIM DATA LAMPU1
TIDAK
TOMBOL "2"
YA
1. NYALAKAN LAMPU 2
2. MATIKAN LAMPU 2
KIRIM DATA LAMPU 2
TIDAK
TOMBOL "3"
YA
1. NYALAKAN LAMPU 3
2. MATIKAN LAMPU 3
KIRIM DATA LAMPU 3
TIDAK
TOMBOL "4"
YA
1. NYALAKAN LAMPU 4
2. MATIKAN LAMPU 4
KIRIM DATA LAMPU 4
TIDAK
TAMPILKAN DI LCD

```
;=============================================================
;               Program Unit Kontrol Lampu Gedung
;                    R.Yunri Putra A
;
;=============================================================
Lampu1          bit     00h
Lampu2          bit     01h
Lampu3          bit     02h
Lampu4          bit     03h
;
Relay_1         bit     P1.0
Relay_2         bit     P1.1
Relay_3         bit     P1.2
Relay_4         bit     P1.3
;
Key_1           bit     P2.7
Key_2           bit     P2.6
Key_3           bit     P2.5
Key_4           bit     P2.4
;
Sen_1           bit     P2.0
Sen_2           bit     P2.1
Sen_3           bit     P2.2
Sen_4           bit     P2.3
;
Kirim_485       bit     P3.3
;
Data_ADC        equ     P0
Alamat          equ     50H
Lampu_ID        equ     51H
;
        Org     0H
        Jmp     Start           ; lompat ke label MULAI
;
        Org     23H             ; alamat untuk serial comm. interupt
        Clr     ES              ; matikan interupt serial
        Jnb     RI,$            ; tunggu sampai selesai menerima
        Clr     RI              ; clear receive interupt flag
        Mov     A,SBUF          ; masukkan isi data serial ke accumulator
        Lcall   Terima_data_Serial
        Setb    ES              ; enable serial interupt
        Reti                    ; kembali
;
Start:
        Clr     Relay_1
        Clr     Relay_2
        Clr     Relay_3
        Clr     Relay_4
        Clr     Kirim_485       ; matikan transmit hidupkan receive
        Mov     TMOD,#20H       ; mode timer 1 = 8 bit auto reload
        Mov     TH1,#0FDH       ; isi timer 1 dengan FD h ( baud rate 9600 bps )
        Setb    TR1             ; start timer 1
        Mov     SCON,#50H       ; mode 1
        Setb    EA              ; enable interupt
        Setb    ES              ; enable serial interupt
Ulang:
        Mov     P2,#0FFH
        Acall   Cek_Cahaya
        Acall   Cek_tombol_ditekan
        Acall   Ldelay
        Sjmp    Ulang
;
```

```
;=======================================
; Routine Untuk Mendeteksi Cahaya
;=======================================
Cek_Cahaya:
       Mov    A,Data_Adc
       Subb   A,#0C0H
       Jnc    Terang
       Clr    Lampu1
       Clr    Lampu2
       Clr    C
       Ret
;
Terang:
       Setb   Lampu1
       Setb   Lampu2
       Ret
;
;=======================================
; Routine Untuk Mendeteksi Tombol
;=======================================
Cek_tombol_ditekan:
       Jb     Key_1,Tidak_Ditekan_1
       Cpl    Relay_1
       Jnb    Relay_1,Mati_L1
       Mov    Alamat,#10H
       Mov    Lampu_ID,#70H
       Acall  Kirim_baris_data
       Acall  Keluarkan_hasil_Cahaya_1
       Acall  Cek_Lampu_Rusak_1
       Jnb    Key_1,$
       Acall  Ldelay
       Jnb    Key_1,$
       Ret
Mati_L1:
       Mov    Alamat,#10H
       Mov    Lampu_ID,#71H
       Acall  Kirim_baris_data
       Clr    Relay_3
       Jnb    Key_1,$
       Acall  Ldelay
       Jnb    Key_1,$
       Ret
;
Tidak_Ditekan_1:
       Jb     Key_2,Tidak_Ditekan_2
       Cpl    Relay_2
       Jnb    Relay_2,Mati_L2
       Mov    Alamat,#10H
       Mov    Lampu_ID,#72H
       Acall  Kirim_baris_data
       Acall  Keluarkan_hasil_Cahaya_2
       Acall  Cek_Lampu_Rusak_1
       Jnb    Key_2,$
       Acall  Ldelay
       Jnb    Key_2,$
       Ret
Mati_L2:
       Mov    Alamat,#10H
       Mov    Lampu_ID,#73H
       Acall  Kirim_baris_data
       Clr    Relay_4
       Jnb    Key_2,$
       Acall  Ldelay
       Jnb    Key_2,$
       Ret
```

```
Tidak_Ditekan_2:
        Jb      Key_3,Tidak_Ditekan_3
        Cpl     Relay_3
        Jnb     Relay_3,Mati_L3
        Mov     Alamat,#10H
        Mov     Lampu_ID,#74H
        Acall   Kirim_baris_data
        Jnb     Key_3,$
        Acall   Ldelay
        Jnb     Key_3,$
        Ret
Mati_L3:
        Mov     Alamat,#10H
        Mov     Lampu_ID,#75H
        Acall   Kirim_baris_data
        Jnb     Key_3,$
        Acall   Ldelay
        Jnb     Key_3,$
        Ret
;
Tidak_Ditekan_3:
        Jb      Key_4,Tidak_Ditekan_4
        Cpl     Relay_4
        Jnb     Relay_4,Mati_L4
        Mov     Alamat,#10H
        Mov     Lampu_ID,#76H
        Acall   Kirim_baris_data
        Jnb     Key_4,$
        Acall   Ldelay
        Jnb     Key_4,$
        Ret
Mati_L4:
        Mov     Alamat,#10H
        Mov     Lampu_ID,#77H
        Acall   Kirim_baris_data
        Jnb     Key_4,$
        Acall   Ldelay
        Jnb     Key_4,$
Tidak_Ditekan_4:
        Ret
;
;================================================
; Routine Untuk Menyalakan Lampu Kedua
; Sebagai Pengaruh dari Cahaya
;================================================
Keluarkan_hasil_Cahaya_1:
        Setb    C
        Anl     C,Relay_1
        Anl     C,Lampu1
        Mov     Relay_3,C
        Ret
;
Keluarkan_hasil_Cahaya_2:
        Setb    C
        Anl     C,Relay_2
        Anl     C,Lampu2
        Mov     Relay_4,C
        Ret
;
;================================================
; Routine Untuk Mendeteksi Lampu Rusak
; Menggunakan Sensor Cahaya
;================================================
Cek_Lampu_Rusak_1:
        Mov     C,Sen_1
        Cpl     C
        Anl     C,Relay_1
        Jnc     Tidak_Rusak_1
```

```
        Mov     Alamat,#10H
        Mov     Lampu_ID,#80H
        Acall   Kirim_baris_data
        Ret
Tidak_Rusak_1:
        Mov     C,Sen_2
        Cpl     C
        Anl     C,Relay_2
        Jnc     Tidak_Rusak_2
        Mov     Alamat,#10H
        Mov     Lampu_ID,#80H
        Acall   Kirim_baris_data
Tidak_Rusak_2:
        Mov     C,Sen_3
        Cpl     C
        Anl     C,Relay_3
        Jnc     Tidak_Rusak_3
        Mov     Alamat,#10H
        Mov     Lampu_ID,#81H
        Acall   Kirim_baris_data
        Ret
Tidak_Rusak_3:
        Mov     C,Sen_4
        Cpl     C
        Anl     C,Relay_4
        Jnc     Tidak_Rusak_4
        Mov     Alamat,#10H
        Mov     Lampu_ID,#80H
        Acall   Kirim_baris_data
        Ret
Tidak_Rusak_4:
        Ret
;=============================================
; Routine Untuk Mengirimkan Data Ke Pusat
;
;=============================================
Kirim_baris_data:
        Mov     A,Alamat
        Acall   Kirim
        Mov     A,Lampu_ID
        Acall   Kirim
        Ret
;
;=============================================
; Routine penghasil delay
;=============================================
delay:  Mov     R0,#50
delay1:  Mov     R5,#0
        Djnz    R5,$
        Djnz    R0,delay1
        Ret
;
Ldelay:  Mov     R2,#10H
Ld1:     Acall   delay
        Djnz    R2,Ld1
        Ret
;
;=============================================
; Routine Untuk Mengirim Data Serial
;=============================================
Kirim:
        Setb    Kirim_485
        Nop
        Nop
        Clr     ES              ; matikan serial interupt saat mengirim
        Mov     SBUF,A          ; isi serial buffer dengan data yg dikirim
        Jnb     TI,$            ; tunggu pengiriman selesai
        Clr     TI              ; clear transmit interupt flag
```

```
        Setb   ES
        Nop
        Nop
        Clr    Kirim_485
        Ret
;
;=========================================
; Routine Untuk Menerima Data Serial
;=========================================
Terima_data_Serial:
        Acall  Periksa_Data_Serial
        Acall  Cek_Cahaya
        Acall  Cek_Lampu_Rusak_1
        Ret
;
Periksa_Data_Serial:
        Cjne   A,#10H,Gagal
        Jnb    RI,$            ; tunggu sampai selesai menerima
        Clr    RI              ; clear receive interupt flag
        Mov    A,SBUF          ; masukkan isi data serial ke accumulator
        Cjne   A,#70H,Cek_11
        Setb   Relay_1
        Acall  Keluarkan_hasil_Cahaya_1

Gagal:
        Ret
Cek_11:
        Cjne   A,#71H,Cek_12
        Clr    Relay_1
        Clr    Relay_3
        Ret
Cek_12:
        Cjne   A,#72H,Cek_13
        Setb   Relay_2
        Acall  Keluarkan_hasil_Cahaya_2
        Ret
Cek_13:
        Cjne   A,#73H,Cek_14
        Clr    Relay_2
        Clr    Relay_4
        Ret
Cek_14:
        Ret
;
        Cjne   A,#74H,Cek_15
        Setb   Relay_3
        Ret
Cek_15:
        Cjne   A,#75H,Cek_16
        Clr    Relay_3
        Ret
Cek_16:
        Cjne   A,#76H,Cek_17
        Setb   Relay_4
        Ret
Cek_17:
        Cjne   A,#77H,Cek_18
        Clr    Relay_4
        Ret
Cek_18:
        Ret
;
        END
```

```
;=================================================================
;              Program Pusat Kontrol Lampu Gedung
;                   R.Yunri Putra A
;
;=================================================================
Lampu1        bit     00h
Lampu2        bit     01h
Lampu3        bit     02h
Lampu4        bit     03h
Lampu5        bit     04h
Lampu6        bit     05h
Lampu7        bit     06h
Lampu8        bit     07h
;
kolom1        bit    p2.0   ; kiri (1,4,7,redial)
kolom2        bit    p2.1
kolom3        bit    p2.2
baris1        bit    p2.3   ; atas (1,2,3)
baris2        bit    p2.4
baris3        bit    p2.5
baris4        bit    p2.6
;
Lcd_CS        bit    P1.0
Lcd_RS        bit    P1.1
;
Buzzer        bit    P3.2
;
Kirim_485     bit    P1.2
;
keyport               equ    P2
keydata               equ    50H
keybounc      equ     51H
Old_data      equ     52H
Alamat        equ     53H
Lampu_ID      equ     54H
;
       Org    0H
       Jmp    Start          ; lompat ke label MULAI
;
       Org    23H            ; alamat untuk serial comm. interupt
       Clr    ES             ; matikan interupt serial
       Jnb    RI,$           ; tunggu sampai selesai menerima
       Clr    RI             ; clear receive interupt flag
       Mov    A,SBUF         ; masukkan isi data serial ke accumulator
       Lcall  Terima
       Setb   ES             ; enable serial interupt
       Reti                  ; kembali
;
Start:
       Mov    20H,#00
       Clr    Buzzer         ; matikan buzzer
       Clr    Kirim_485      ; matikan transmit hidupkan receive
       Acall  Init_lcd       ; inisialisasi lcd
       Acall  Judul
       Mov    TMOD,#20H      ; mode timer 1 = 8 bit auto reload
       Mov    TH1,#0FDH      ; isi timer 1 dengan FD h ( baud rate 9600 bps )
       Setb   TR1            ; start timer 1
       Mov    SCON,#50H      ; mode 1
       Setb   EA             ; enable interupt
       Setb   ES             ; enable serial interupt
Ulang:
       Acall  Keypad3x4
       Mov    A,keydata
       Cjne   A,#0FFH,ditekan
       Ajmp   ulang
Ditekan:
       Acall  Cek_Tombol_Yang_Ditekan
       Acall  Kirim_baris_data
```

```
        Acall  Tampilan_Lampu_Keluar_LCD
        Acall  tunggu_tombol_dilepas
        Sjmp   Ulang
;
;=========================================
; Inisialisasi LCD
;=========================================
Init_Lcd:
        Acall  Ldelay
        Mov     A,#03Fh
        Acall   write_inst
        Acall   write_inst
        Mov     A,#0Dh
        Acall   write_inst
        Mov     A,#06h
        Acall   write_inst
        Mov     A,#01h
        Acall   write_inst
        Mov     A,#0Ch
        Acall   write_inst
        Ret
;
;=========================================
; Routine untuk menulis instruksi ke LCD
;=========================================
write_inst:
        Clr     LCD_RS
        Setb    LCD_CS
        Mov     P0,A      ;intruksi ke LCD
        Clr     LCD_CS    ;module
        Setb    LCD_CS
        Acall   delay
        Ret
;
;=========================================
; Routine untuk menulis data ke LCD
;=========================================
write_data:
        Setb    LCD_RS
        Setb    LCD_CS
        Mov     P0,A      ;data ke LCD
        Clr     LCD_CS    ;module
        Setb    LCD_CS
        Acall   delay
        Ret
;
;=========================================
; Routine penghasil delay
;=========================================
delay: Mov      R0,#50
delay1: Mov      R5,#0
       Djnz     R5,$
       Djnz     R0,delay1
       Ret
;
Ldelay: Mov      R2,#020H
Ld1:    Acall    delay
       Djnz     R2,Ld1
       Ret
;
;=========================================
; Routine Untuk Mengirim Data Serial
;=========================================
Kirim:
       Setb   Kirim_485
       Nop
       Nop
       Clr    ES              ; matikan serial interupt saat mengirim
```

```
        Mov     SBUF,A          ; isi serial buffer dengan data yg dikirim
        Jnb     TI,$            ; tunggu pengiriman selesai
        Clr     TI              ; clear transmit interupt flag
        Setb    ES
        Nop
        Nop
        Clr     Kirim_485
        Ret
;
;=======================================
; Routine Untuk Menampilkan Lcd
;=======================================
Judul:
        Mov     R4,#3
        Mov     DPTR,#Tampilan1
Baris_atas:
        Mov     R3,#16
        Mov     A,#80h
        Acall   write_inst
Tulis_1char_1:
        Clr     A
        Movc    A,@A+DPTR
        Inc     DPTR
        Acall   write_data
        Djnz    R3,Tulis_1char_1
;
Baris_bawah:
        Mov     R3,#16
        Mov     A,#0C0h
        Acall   write_inst
Tulis_1char_2:
        Clr     A
        Movc    A,@A+DPTR
        Inc     DPTR
        Acall   write_data
        Djnz    R3,Tulis_1char_2
        Acall   Ldelay
        Djnz    R4,Baris_atas
        Ret
;
;=======================================
; routine untuk baca keypad 3x4
; output pd keydata(0-9,E=redial,F=#)
;=======================================
Keypad3x4:
        mov     keybounc,#200
        mov     keyport,#0FFh
        clr     kolom1
ul1:    jb      baris1,key1
        djnz    keybounc,ul1
        mov     keydata,#1
        ret
key1:   jb      baris2,key2
        djnz    keybounc,key1
        mov     keydata,#4
        ret
key2:   jb      baris3,key3
        djnz    keybounc,key2
        mov     keydata,#7
        ret
key3:   jb      baris4,key4
        djnz    keybounc,key3
        mov     keydata,#0Eh
        ret
key4:   setb    kolom1
        clr     kolom2
        jb      baris1,key5
        djnz    keybounc,key4
```

```
        mov     keydata,#2
        ret
key5:   jb      baris2,key6
        djnz    keybounc,key5
        mov     keydata,#5
        ret
key6:   jb      baris3,key7
        djnz    keybounc,key6
        mov     keydata,#8
        ret
key7:   jb      baris4,key8
        djnz    keybounc,key7
        mov     keydata,#0
        ret
key8:   setb    kolom2
        clr     kolom3
        jb      baris1,key9
        djnz    keybounc,key8
        mov     keydata,#3
        ret
key9:   jb      baris2,key10
        djnz    keybounc,key9
        mov     keydata,#6
        ret
key10:  jb      baris3,key11
        djnz    keybounc,key10
        mov     keydata,#9
        ret
key11:  jb      baris4,key12
        djnz    keybounc,key11
        mov     keydata,#0Fh
        ret
key12:  mov     keydata,#0FFh
        Ret
;
tunggu_tombol_dilepas:
        Jnb     baris1,$
        Jnb     baris2,$
        Jnb     baris3,$
        Jnb     baris4,$
        Ret
;
;=========================================
; Routine Untuk Mengecek Tombol Yang
; Ditekan
;=========================================
Cek_Tombol_Yang_Ditekan:
        Cjne    A,#1,Cek_11
        Mov     Alamat,#10H
        Cpl     Lampu1
        Jnb     Lampu1,Mati_L1
        Mov     Lampu_ID,#70H
        Ret
Mati_L1:
        Mov     Lampu_ID,#71H
        Ret
Cek_11:
        Cjne    A,#2,Cek_12
        Mov     Alamat,#10H
        Cpl     Lampu2
        Jnb     Lampu2,Mati_L2
        Mov     Lampu_ID,#72H
        Ret
Mati_L2:
        Mov     Lampu_ID,#73H
        Ret
```

```
Cek_12:
       Cjne   A,#3,Cek_13
       Mov    Alamat,#10H
       Cpl    Lampu3
       Jnb    Lampu3,Mati_L3
       Mov    Lampu_ID,#74H
       Ret
Mati_L3:
       Mov    Lampu_ID,#75H
       Ret
Cek_13:
       Cjne   A,#4,Cek_14
       Mov    Alamat,#10H
       Cpl    Lampu4
       Jnb    Lampu4,Mati_L4
       Mov    Lampu_ID,#76H
       Ret
Mati_L4:
       Mov    Lampu_ID,#77H
       Ret
Cek_14:
       Cjne   A,#5,Cek_15
       Mov    Alamat,#20H
       Cpl    Lampu5
       Jnb    Lampu5,Mati_L5
       Mov    Lampu_ID,#70H
       Ret
Mati_L5:
       Mov    Lampu_ID,#71H
       Ret
Cek_15:
       Cjne   A,#6,Cek_16
       Mov    Alamat,#20H
       Cpl    Lampu6
       Jnb    Lampu6,Mati_L6
       Mov    Lampu_ID,#72H
       Ret
Mati_L6:
       Mov    Lampu_ID,#73H
       Ret
Cek_16:
       Cjne   A,#7,Cek_17
       Mov    Alamat,#20H
       Cpl    Lampu7
       Jnb    Lampu7,Mati_L7
       Mov    Lampu_ID,#74H
       Ret
Mati_L7:
       Mov    Lampu_ID,#75H
       Ret
Cek_17:
       Cjne   A,#8,Cek_18
       Mov    Alamat,#20H
       Cpl    Lampu8
       Jnb    Lampu8,Mati_L8
       Mov    Lampu_ID,#76H
       Ret
Mati_L8:
       Mov    Lampu_ID,#77H
       Ret
Cek_18:
       Ret
;
```

```
;=============================================
; Routine Untuk Mengirimkan Data Ke Unit
;
;=============================================
Kirim_baris_data:
       Mov    A,Alamat
       Acall  Kirim
       Mov    A,Lampu_ID
       Acall  Kirim
       Ret
;
;=============================================
; Routine Untuk Menampilkan LCD sesuai
; Kondisi Lampu
;=============================================
Tampilan_Lampu_Keluar_LCD:
       Mov    A,Alamat
       Cjne   A,#10H,Ganti_baris_lcd_1
       Acall  Cek_Data_Unit_1
       Mov    A,Alamat
       Acall  write_inst
       Mov    A,Lampu_ID
       Acall  write_data
       Ret
Ganti_baris_lcd_1:
       Cjne   A,#20H,Ganti_baris_lcd_2
       Acall  Cek_Data_Unit_2
       Mov    A,Alamat
       Acall  write_inst
       Mov    A,Lampu_ID
       Acall  write_data
Ganti_baris_lcd_2:
       Ret
;
;=============================================
; Routine Untuk Menampilkan LCD Baris bawah
;=============================================
Cek_Data_Unit_1:
       Mov    A,Lampu_ID
       Cjne   A,#70H,Cek_31
       Mov    Alamat,#82H
       Mov    Lampu_ID,#31H
       Ret
Cek_31:
       Cjne   A,#71H,Cek_32
       Mov    Alamat,#82H
       Mov    Lampu_ID,#30H
       Ret
Cek_32:
       Cjne   A,#72H,Cek_33
       Mov    Alamat,#86H
       Mov    Lampu_ID,#31H
       Ret
Cek_33:
       Cjne   A,#73H,Cek_34
       Mov    Alamat,#86H
       Mov    Lampu_ID,#30H
       Ret
Cek_34:
       Cjne   A,#74H,Cek_35
       Mov    Alamat,#8AH
       Mov    Lampu_ID,#31H
       Ret
Cek_35:
       Cjne   A,#75H,Cek_36
       Mov    Alamat,#8AH
       Mov    Lampu_ID,#30H
       Ret
```

```
Cek_36:
       Cjne   A,#76H,Cek_37
       Mov    Alamat,#8EH
       Mov    Lampu_ID,#31H
       Ret
Cek_37:
       Cjne   A,#77H,Cek_38
       Mov    Alamat,#8EH
       Mov    Lampu_ID,#30H
       Ret
Cek_38:
       Ret
;
;=========================================
; Routine Untuk Menampilkan LCD Baris Atas
;=========================================
Cek_Data_Unit_2:
       Mov    A,Lampu_ID
       Cjne   A,#70H,Cek_51
       Mov    Alamat,#0C2H
       Mov    Lampu_ID,#31H
       Ret
Cek_51:
       Cjne   A,#71H,Cek_52
       Mov    Alamat,#0C2H
       Mov    Lampu_ID,#30H
       Ret
Cek_52:
       Cjne   A,#72H,Cek_53
       Mov    Alamat,#0C6H
       Mov    Lampu_ID,#31H
       Ret
Cek_53:
       Cjne   A,#73H,Cek_54
       Mov    Alamat,#0C6H
       Mov    Lampu_ID,#30H
       Ret
Cek_54:
       Cjne   A,#74H,Cek_55
       Mov    Alamat,#0CAH
       Mov    Lampu_ID,#31H
       Ret
Cek_55:
       Cjne   A,#75H,Cek_56
       Mov    Alamat,#0CAH
       Mov    Lampu_ID,#30H
       Ret
Cek_56:
       Cjne   A,#76H,Cek_57
       Mov    Alamat,#0CEH
       Mov    Lampu_ID,#31H
       Ret
Cek_57:
       Cjne   A,#77H,Cek_58
       Mov    Alamat,#0CEH
       Mov    Lampu_ID,#30H
       Ret
Cek_58:
       Ret
;
;=========================================
; Routine Untuk Menampilkan LCD Sesuai
; Kondisi Lampu Dari Data Yang Dikirim
;=========================================
Terima:
       Mov    Alamat,A
       Jnb    RI,$          ; tunggu sampai selesai menerima
       Clr    RI            ; clear receive interupt flag
```

```
        Mov     A,SBUF          ; masukkan isi data serial ke accumulator
        Mov     Lampu_ID,A
        Mov     A,Alamat
        Cjne    A,#10H,Ganti_baris_lcd_11
        Acall   Cek_Data_Unit_11
        Mov     A,Alamat
        Acall   write_inst
        Mov     A,Lampu_ID
        Acall   write_data
        Ret
Ganti_baris_lcd_11:
        Cjne    A,#20H,Ganti_baris_lcd_12
        Acall   Cek_Data_Unit_12
        Mov     A,Alamat
        Acall   write_inst
        Mov     A,Lampu_ID
        Acall   write_data
Ganti_baris_lcd_12:
        Ret
;
;===========================================
; Routine Untuk Menampilkan LCD Baris bawah
;===========================================
Cek_Data_Unit_11:
        Mov     A,Lampu_ID
        Cjne    A,#70H,Cek_131
        Mov     Alamat,#82H
        Mov     Lampu_ID,#31H
        Setb    Lampu1
        Ret
Cek_131:
        Cjne    A,#71H,Cek_132
        Mov     Alamat,#82H
        Mov     Lampu_ID,#30H
        Clr     Lampu1
        Ret
Cek_132:
        Cjne    A,#72H,Cek_133
        Mov     Alamat,#86H
        Mov     Lampu_ID,#31H
        Setb    Lampu2
        Ret
Cek_133:
        Cjne    A,#73H,Cek_134
        Mov     Alamat,#86H
        Mov     Lampu_ID,#30H
        Clr     Lampu2
        Ret
Cek_134:
        Cjne    A,#74H,Cek_135
        Mov     Alamat,#8AH
        Mov     Lampu_ID,#31H
        Setb    Lampu3
        Ret
Cek_135:
        Cjne    A,#75H,Cek_136
        Mov     Alamat,#8AH
        Mov     Lampu_ID,#30H
        Clr     Lampu3
        Ret
Cek_136:
        Cjne    A,#76H,Cek_137
        Mov     Alamat,#8EH
        Mov     Lampu_ID,#31H
        Setb    Lampu4
        Ret
```

```
Cek_137:
       Cjne   A,#77H,Cek_138
       Mov    Alamat,#8EH
       Mov    Lampu_ID,#30H
       Clr    Lampu4
       Ret
Cek_138:
       Cjne   A,#80H,Cek_139
       Mov    Alamat,#82H
       Mov    Lampu_ID,'E'
       Acall  Alarm
       Ret
Cek_139:
       Cjne   A,#81H,Cek_13A
       Mov    Alamat,#86H
       Mov    Lampu_ID,'E'
       Acall  Alarm
       Ret
Cek_13A:
       Cjne   A,#82H,Cek_13B
       Mov    Alamat,#8AH
       Mov    Lampu_ID,'E'
       Acall  Alarm
       Ret
Cek_13B:
       Cjne   A,#83H,Cek_13C
       Mov    Alamat,#8EH
       Mov    Lampu_ID,'E'
       Acall  Alarm
Cek_13C:
       Ret
;
;=============================================
; Routine Untuk Menampilkan LCD Baris Atas
;=============================================
Cek_Data_Unit_12:
       Mov    A,Lampu_ID
       Cjne   A,#70H,Cek_151
       Mov    Alamat,#0C2H
       Mov    Lampu_ID,#31H
       Setb   Lampu5
       Ret
Cek_151:
       Cjne   A,#71H,Cek_152
       Mov    Alamat,#0C2H
       Mov    Lampu_ID,#30H
       Clr    Lampu5
       Ret
Cek_152:
       Cjne   A,#72H,Cek_153
       Mov    Alamat,#0C6H
       Mov    Lampu_ID,#31H
       Setb   Lampu6
       Ret
Cek_153:
       Cjne   A,#73H,Cek_154
       Mov    Alamat,#0C6H
       Mov    Lampu_ID,#30H
       Clr    Lampu6
       Ret
Cek_154:
       Cjne   A,#74H,Cek_155
       Mov    Alamat,#0CAH
       Mov    Lampu_ID,#31H
       Setb   Lampu7
       Ret
```

```
Cek_155:
        Cjne    A,#75H,Cek_156
        Mov     Alamat,#0CAH
        Mov     Lampu_ID,#30H
        Clr     Lampu7
        Ret
Cek_156:
        Cjne    A,#76H,Cek_157
        Mov     Alamat,#0CEH
        Mov     Lampu_ID,#31H
        Setb    Lampu8
        Ret
Cek_157:
        Cjne    A,#77H,Cek_158
        Mov     Alamat,#0CEH
        Mov     Lampu_ID,#30H
        Clr     Lampu8
        Ret
Cek_158:
        Cjne    A,#80H,Cek_159
        Mov     Alamat,#0C2H
        Mov     Lampu_ID,'E'
        Acall   Alarm
        Ret
Cek_159:
        Cjne    A,#81H,Cek_15A
        Mov     Alamat,#0C6H
        Mov     Lampu_ID,'E'
        Acall   Alarm
        Ret
Cek_15A:
        Cjne    A,#82H,Cek_15B
        Mov     Alamat,#0CAH
        Mov     Lampu_ID,'E'
        Acall   Alarm
        Ret
Cek_15B:
        Cjne    A,#83H,Cek_15C
        Mov     Alamat,#0CEH
        Mov     Lampu_ID,'E'
        Acall   Alarm
Cek_15C:
        Ret
;
;=============================================
; Routine Untuk Menjalankan Buzzer Apabila
; Lampu Ada Yang Rusak
;=============================================
Alarm:
        Setb    Buzzer
Lama:
        Acall   Ldelay
        Djnz    R7,Lama
        Clr     Buzzer
        Ret
;
Tampilan1:
        DB      'ALAT  PENGENDALI'
        DB      ' LAMPU OTOMATIS '
        DB      'R.Yunri Putra A '
        DB      'Nim : 98.17.035 '
        DB      '1.0 2.0 3.0 4.0 '
        DB      '5.0 6.0 7.0 8.0 '
;
        END
```

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- xible ISP Programming (Byte and Page Mode)

scription

AT89S51 is a low-power, high-performance CMOS 8-bit microcontroller with 4K of in-system programmable Flash memory. The device is manufactured using l's high-density nonvolatile memory technology and is compatible with the indus-andard 80C51 instruction set and pinout. The on-chip Flash allows the program ory to be reprogrammed in-system or by a conventional nonvolatile memory pro-mer. By combining a versatile 8-bit CPU with in-system programmable Flash on a olithic chip, the Atmel AT89S51 is a powerful microcontroller which provides a y-flexible and cost-effective solution to many embedded control applications.

AT89S51 provides the following standard features: 4K bytes of Flash, 128 bytes of , 32 I/O lines, Watchdog timer, two data pointers, two 16-bit timer/counters, a five-r two-level interrupt architecture, a full duplex serial port, on-chip oscillator, and circuitry. In addition, the AT89S51 is designed with static logic for operation to zero frequency and supports two software selectable power saving modes. dle Mode stops the CPU while allowing the RAM, timer/counters, serial port, and upt system to continue functioning. The Power-down mode saves the RAM con-but freezes the oscillator, disabling all other chip functions until the next external upt or hardware reset.

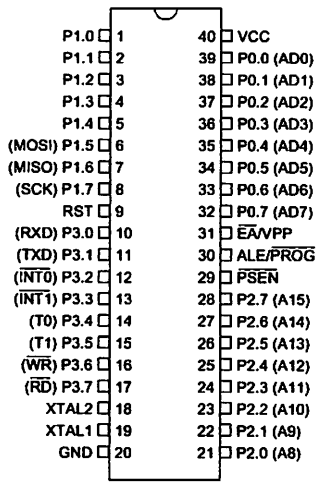
8-bit Microcontroller with 4K Bytes In-System Programmable Flash

AT89S51

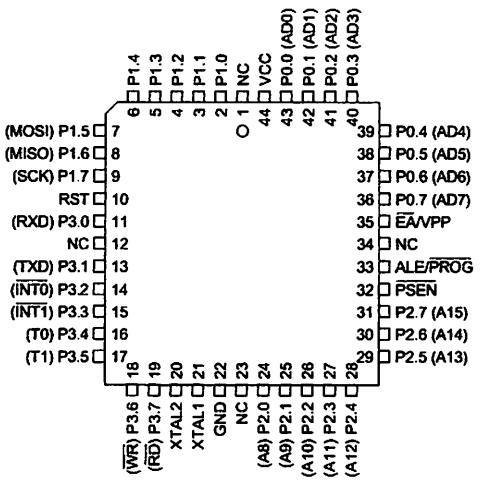
Rev. 2487A–10/01

Configurations

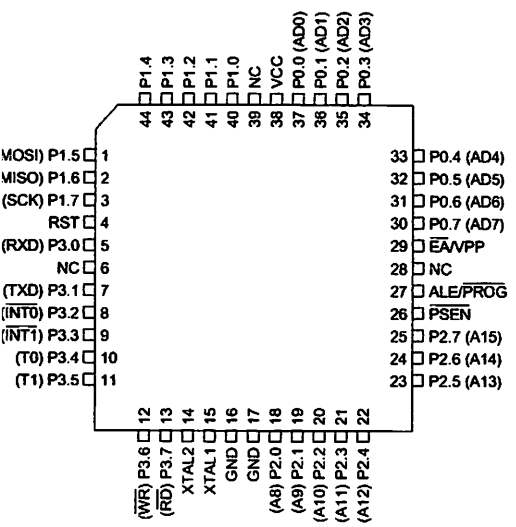
PDIP



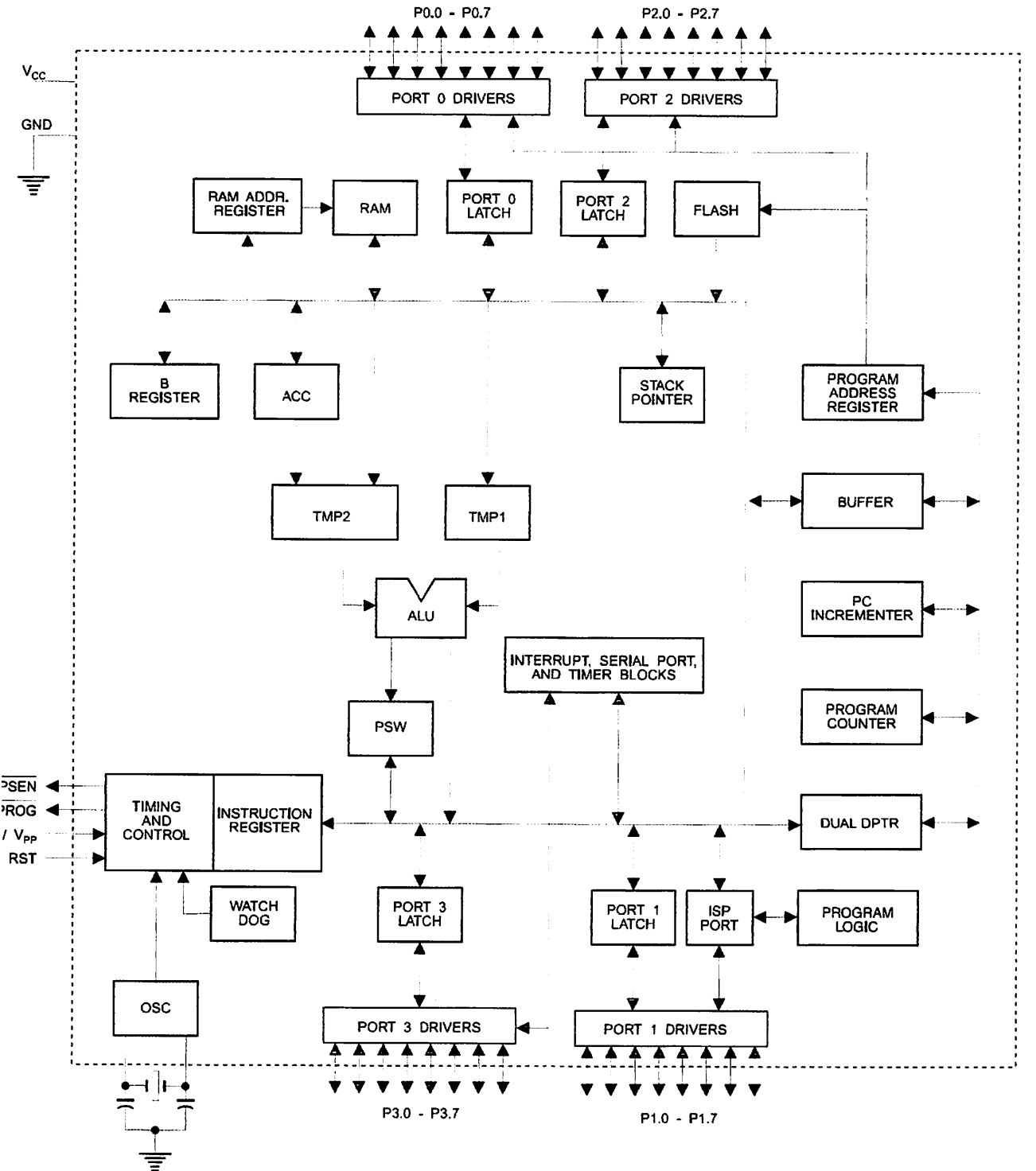
PLCC



TQFP



ck Diagram


P0.0 - P0.7
P2.0 - P2.7
V_{CC}
GND
PORT 0 DRIVERS
PORT 2 DRIVERS
RAM ADDR. REGISTER
RAM
PORT 0 LATCH
PORT 2 LATCH
FLASH
B REGISTER
ACC
STACK POINTER
PROGRAM ADDRESS REGISTER
TMP2
TMP1
BUFFER
ALU
PC INCREMENTER
INTERRUPT, SERIAL PORT, AND TIMER BLOCKS
PSW
PROGRAM COUNTER
PSEN
PROG
/ V_{PP}
RST
TIMING AND CONTROL
INSTRUCTION REGISTER
DUAL DPTR
WATCH DOG
PORT 3 LATCH
PORT 1 LATCH
ISP PORT
PROGRAM LOGIC
OSC
PORT 3 DRIVERS
PORT 1 DRIVERS
P3.0 - P3.7
P1.0 - P1.7

Description

Supply voltage.

Ground.

0

Port 0 is an 8-bit open drain bidirectional I/O port. As an output port, each pin can sink eight TTL inputs. When 1s are written to port 0 pins, the pins can be used as high-impedance inputs.

Port 0 can also be configured to be the multiplexed low-order address/data bus during accesses to external program and data memory. In this mode, P0 has internal pull-ups.

Port 0 also receives the code bytes during Flash programming and outputs the code bytes during program verification. **External pull-ups are required during program verification.**

1

Port 1 is an 8-bit bidirectional I/O port with internal pull-ups. The Port 1 output buffers can sink/source four TTL inputs. When 1s are written to Port 1 pins, they are pulled high by the internal pull-ups and can be used as inputs. As inputs, Port 1 pins that are externally being pulled low will source current (I_{IL}) because of the internal pull-ups.

Port 1 also receives the low-order address bytes during Flash programming and verification.

Port Pin	Alternate Functions
P1.5	MOSI (used for In-System Programming)
P1.6	MISO (used for In-System Programming)
P1.7	SCK (used for In-System Programming)

2

Port 2 is an 8-bit bidirectional I/O port with internal pull-ups. The Port 2 output buffers can sink/source four TTL inputs. When 1s are written to Port 2 pins, they are pulled high by the internal pull-ups and can be used as inputs. As inputs, Port 2 pins that are externally being pulled low will source current (I_{IL}) because of the internal pull-ups.

Port 2 emits the high-order address byte during fetches from external program memory and during accesses to external data memory that use 16-bit addresses (MOVX @ DPTR). In this application, Port 2 uses strong internal pull-ups when emitting 1s. During accesses to external data memory that use 8-bit addresses (MOVX @ RI), Port 2 emits the contents of the P2 Special Function Register.

Port 2 also receives the high-order address bits and some control signals during Flash programming and verification.

3

Port 3 is an 8-bit bidirectional I/O port with internal pull-ups. The Port 3 output buffers can sink/source four TTL inputs. When 1s are written to Port 3 pins, they are pulled high by the internal pull-ups and can be used as inputs. As inputs, Port 3 pins that are externally being pulled low will source current (I_{IL}) because of the pull-ups.

Port 3 receives some control signals for Flash programming and verification.

Port 3 also serves the functions of various special features of the AT89S51, as shown in the following table.

Port Pin	Alternate Functions
P3.0	RXD (serial input port)
P3.1	TXD (serial output port)
P3.2	$\overline{INT0}$ (external interrupt 0)
P3.3	$\overline{INT1}$ (external interrupt 1)
P3.4	T0 (timer 0 external input)
P3.5	T1 (timer 1 external input)
P3.6	$\overline{WR}$ (external data memory write strobe)
P3.7	$\overline{RD}$ (external data memory read strobe)

Reset input. A high on this pin for two machine cycles while the oscillator is running resets the device. This pin drives High for 98 oscillator periods after the Watchdog times out. The DISRTO bit in SFR AUXR (address 8EH) can be used to disable this feature. In the default state of bit DISRTO, the RESET HIGH out feature is enabled.

/PROG Address Latch Enable (ALE) is an output pulse for latching the low byte of the address during accesses to external memory. This pin is also the program pulse input ($\overline{PROG}$) during Flash programming.

In normal operation, ALE is emitted at a constant rate of 1/6 the oscillator frequency and may be used for external timing or clocking purposes. Note, however, that one ALE pulse is skipped during each access to external data memory.

If desired, ALE operation can be disabled by setting bit 0 of SFR location 8EH. With the bit set, ALE is active only during a MOVX or MOVC instruction. Otherwise, the pin is weakly pulled high. Setting the ALE-disable bit has no effect if the microcontroller is in external execution mode.

N Program Store Enable ($\overline{PSEN}$) is the read strobe to external program memory.

When the AT89S51 is executing code from external program memory, $\overline{PSEN}$ is activated twice each machine cycle, except that two $\overline{PSEN}$ activations are skipped during each access to external data memory.

'PP External Access Enable. $\overline{EA}$ must be strapped to GND in order to enable the device to fetch code from external program memory locations starting at 0000H up to FFFFH. Note, however, that if lock bit 1 is programmed, $\overline{EA}$ will be internally latched on reset.

$\overline{EA}$ should be strapped to V_{CC} for internal program executions.

This pin also receives the 12-volt programming enable voltage (V_{PP}) during Flash programming.

-1 Input to the inverting oscillator amplifier and input to the internal clock operating circuit.

-2 Output from the inverting oscillator amplifier

cial ction isters

A map of the on-chip memory area called the Special Function Register (SFR) space is shown in Table 1.

Note that not all of the addresses are occupied, and unoccupied addresses may not be implemented on the chip. Read accesses to these addresses will in general return random data, and write accesses will have an indeterminate effect.

1. AT89S51 SFR Map and Reset Values

H								0FFH
H	B 00000000							0F7H
H								0EFH
H	ACC 00000000							0E7H
H								0DFH
H	PSW 00000000							0D7H
H								0CFH
H								0C7H
H	IP XX000000							0BFH
H	P3 11111111							0B7H
H	IE 0X000000							0AFH
H	P2 11111111		AUXR1 XXXXXXX0				WDTRST XXXXXXXX	0A7H
H	SCON 00000000	SBUF XXXXXXXX						9FH
H	P1 11111111							97H
H	TCON 00000000	TMOD 00000000	TL0 00000000	TL1 00000000	TH0 00000000	TH1 00000000	AUXR XXX00XX0	8FH
H	P0 11111111	SP 00000111	DP0L 00000000	DP0H 00000000	DP1L 00000000	DP1H 00000000	PCON 0XXX0000	87H

User software should not write 1s to these unlisted locations, since they may be used in future products to invoke new features. In that case, the reset or inactive values of the new bits will always be 0.

Interrupt Registers: The individual interrupt enable bits are in the IE register. Two priorities can be set for each of the five interrupt sources in the IP register.

Table 2. AUXR: Auxiliary Register

AUXR Address = 8EH Reset Value = XXX00XX0B

Not Bit Addressable

Bit	7	6	5	4	3	2	1	0
	–	–	–	WDIDLE	DISRTO	–	–	DISALE

– Reserved for future expansion

DISALE Disable/Enable ALE

DISALE Operating Mode

0 ALE is emitted at a constant rate of 1/6 the oscillator frequency

1 ALE is active only during a MOVX or MOVC instruction

DISRTO Disable/Enable Reset out

DISRTO

0 Reset pin is driven High after WDT times out

1 Reset pin is input only

WDIDLE Disable/Enable WDT in IDLE mode

WDIDLE

0 WDT continues to count in IDLE mode

1 WDT halts counting in IDLE mode

Dual Data Pointer Registers: To facilitate accessing both internal and external data memory, two banks of 16-bit Data Pointer Registers are provided: DP0 at SFR address locations 82H-83H and DP1 at 84H-85H. Bit DPS = 0 in SFR AUXR1 selects DP0 and DPS = 1 selects DP1. The user should always initialize the DPS bit to the appropriate value before accessing the respective Data Pointer Register.

Power Off Flag: The Power Off Flag (POF) is located at bit 4 (PCON.4) in the PCON SFR. POF is set to "1" during power up. It can be set and rest under software control and is not affected by reset.

Table 3. AUXR1: Auxiliary Register 1

AUXR1

Address = A2H

Reset Value = XXXXXXX0B

Not Bit Addressable

Bit	7	6	5	4	3	2	1	0
	–	–	–	–	–	–	–	DPS

– Reserved for future expansion

DPS Data Pointer Register Select

DPS	
0	Selects DPTR Registers DP0L, DP0H
1	Selects DPTR Registers DP1L, DP1H

ıory ınization

MCS-51 devices have a separate address space for Program and Data Memory. Up to 64K bytes each of external Program and Data Memory can be addressed.

ram Memory

If the $\overline{EA}$ pin is connected to GND, all program fetches are directed to external memory.

On the AT89S51, if $\overline{EA}$ is connected to V_{CC}, program fetches to addresses 0000H through FFFH are directed to internal memory and fetches to addresses 1000H through FFFFH are directed to external memory.

Memory

The AT89S51 implements 128 bytes of on-chip RAM. The 128 bytes are accessible via direct and indirect addressing modes. Stack operations are examples of indirect addressing, so the 128 bytes of data RAM are available as stack space.

ːhdog ːr ːe-time ɔled with ɛt-out)

The WDT is intended as a recovery method in situations where the CPU may be subjected to software upsets. The WDT consists of a 14-bit counter and the Watchdog Timer Reset (WDTRST) SFR. The WDT is defaulted to disable from exiting reset. To enable the WDT, a user must write 01EH and 0E1H in sequence to the WDTRST register (SFR location 0A6H). When the WDT is enabled, it will increment every machine cycle while the oscillator is running. The WDT timeout period is dependent on the external clock frequency. There is no way to disable the WDT except through reset (either hardware reset or WDT overflow reset). When WDT overflows, it will drive an output RESET HIGH pulse at the RST pin.

ıg the WDT

To enable the WDT, a user must write 01EH and 0E1H in sequence to the WDTRST register (SFR location 0A6H). When the WDT is enabled, the user needs to service it by writing 01EH and 0E1H to WDTRST to avoid a WDT overflow. The 14-bit counter overflows when it reaches 16383 (3FFFH), and this will reset the device. When the WDT is enabled, it will increment every machine cycle while the oscillator is running. This means the user must reset the WDT at least every 16383 machine cycles. To reset the WDT the user must write 01EH and 0E1H to WDTRST. WDTRST is a write-only register. The WDT counter cannot be read or written. When WDT overflows, it will generate an output RESET pulse at the RST pin. The RESET pulse duration is 98xTOSC, where TOSC=1/FOSC. To make the best use of the WDT, it

should be serviced in those sections of code that will periodically be executed within the time required to prevent a WDT reset.

)T During ver-down l Idle

In Power-down mode the oscillator stops, which means the WDT also stops. While in Power-down mode, the user does not need to service the WDT. There are two methods of exiting Power-down mode: by a hardware reset or via a level-activated external interrupt, which is enabled prior to entering Power-down mode. When Power-down is exited with hardware reset, servicing the WDT should occur as it normally does whenever the AT89S51 is reset. Exiting Power-down with an interrupt is significantly different. The interrupt is held low long enough for the oscillator to stabilize. When the interrupt is brought high, the interrupt is serviced. To prevent the WDT from resetting the device while the interrupt pin is held low, the WDT is not started until the interrupt is pulled high. It is suggested that the WDT be reset during the interrupt service for the interrupt used to exit Power-down mode.

To ensure that the WDT does not overflow within a few states of exiting Power-down, it is best to reset the WDT just before entering Power-down mode.

Before going into the IDLE mode, the WDIDLE bit in SFR AUXR is used to determine whether the WDT continues to count if enabled. The WDT keeps counting during IDLE (WDIDLE bit = 0) as the default state. To prevent the WDT from resetting the AT89S51 while in IDLE mode, the user should always set up a timer that will periodically exit IDLE, service the WDT, and reenter IDLE mode.

With WDIDLE bit enabled, the WDT will stop to count in IDLE mode and resumes the count upon exit from IDLE.

RT

The UART in the AT89S51 operates the same way as the UART in the AT89C51. For further information on the UART operation, refer to the ATMEL Web site (http://www.atmel.com). From the home page, select 'Products', then '8051-Architecture Flash Microcontroller', then 'Product Overview'.

er 0 and 1

Timer 0 and Timer 1 in the AT89S51 operate the same way as Timer 0 and Timer 1 in the AT89C51. For further information on the timers' operation, refer to the ATMEL Web site (http://www.atmel.com). From the home page, select 'Products', then '8051-Architecture Flash Microcontroller', then 'Product Overview'.

rrupts

The AT89S51 has a total of five interrupt vectors: two external interrupts ($\overline{INT0}$ and $\overline{INT1}$), two timer interrupts (Timers 0 and 1), and the serial port interrupt. These interrupts are all shown in Figure 1.

Each of these interrupt sources can be individually enabled or disabled by setting or clearing a bit in Special Function Register IE. IE also contains a global disable bit, EA, which disables all interrupts at once.

Note that Table 4 shows that bit position IE.6 is unimplemented. In the AT89S51, bit position IE.5 is also unimplemented. User software should not write 1s to these bit positions, since they may be used in future AT89 products.

The Timer 0 and Timer 1 flags, TF0 and TF1, are set at S5P2 of the cycle in which the timers overflow. The values are then polled by the circuitry in the next cycle

Table 4. Interrupt Enable (IE) Register

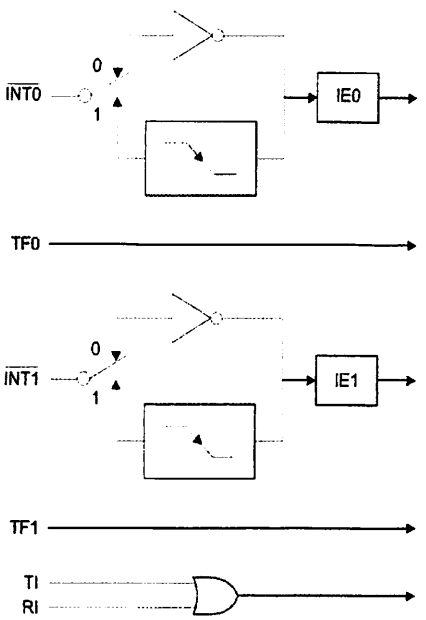
(MSB)							(LSB)
EA	–	–	ES	ET1	EX1	ET0	EX0

Enable Bit = 1 enables the interrupt.

Enable Bit = 0 disables the interrupt.

Symbol	Position	Function
EA	IE.7	Disables all interrupts. If EA = 0, no interrupt is acknowledged. If EA = 1, each interrupt source is individually enabled or disabled by setting or clearing its enable bit.
–	IE.6	Reserved
–	IE.5	Reserved
ES	IE.4	Serial Port interrupt enable bit
ET1	IE.3	Timer 1 interrupt enable bit
EX1	IE.2	External interrupt 1 enable bit
ET0	IE.1	Timer 0 interrupt enable bit
EX0	IE.0	External interrupt 0 enable bit
User software should never write 1s to reserved bits, because they may be used in future AT89 products.		

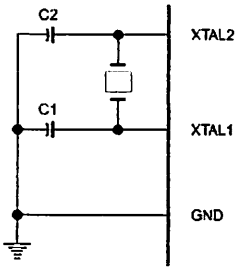
Figure 1. Interrupt Sources



illator racteristics

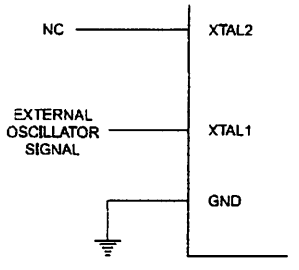
XTAL1 and XTAL2 are the input and output, respectively, of an inverting amplifier that can be configured for use as an on-chip oscillator, as shown in Figure 2. Either a quartz crystal or ceramic resonator may be used. To drive the device from an external clock source, XTAL2 should be left unconnected while XTAL1 is driven, as shown in Figure 3. There are no requirements on the duty cycle of the external clock signal, since the input to the internal clocking circuitry is through a divide-by-two flip-flop, but minimum and maximum voltage high and low time specifications must be observed.

Figure 2. Oscillator Connections



Note: C1, C2 = 30 pF ±10 pF for Crystals = 40 pF ±10 pF for Ceramic Resonators

Figure 3. External Clock Drive Configuration



Mode

In idle mode, the CPU puts itself to sleep while all the on-chip peripherals remain active. The mode is invoked by software. The content of the on-chip RAM and all the special function registers remain unchanged during this mode. The idle mode can be terminated by any enabled interrupt or by a hardware reset.

Note that when idle mode is terminated by a hardware reset, the device normally resumes program execution from where it left off, up to two machine cycles before the internal reset algorithm takes control. On-chip hardware inhibits access to internal RAM in this event, but access to the port pins is not inhibited. To eliminate the possibility of an unexpected write to a port pin when idle mode is terminated by a reset, the instruction following the one that invokes idle mode should not write to a port pin or to external memory.

er-down e

In the Power-down mode, the oscillator is stopped, and the instruction that invokes Power-down is the last instruction executed. The on-chip RAM and Special Function Registers retain their values until the Power-down mode is terminated. Exit from Power-down mode can be initiated either by a hardware reset or by activation of an enabled external interrupt into $\overline{INT0}$ or $\overline{INT1}$. Reset redefines the SFRs but does not change the on-chip RAM. The reset should not be activated before V_{CC} is restored to its normal operating level and must be held active long enough to allow the oscillator to restart and stabilize.

Table 5. Status of External Pins During Idle and Power-down Modes

Mode	Program Memory	ALE	$\overline{PSEN}$	PORT0	PORT1	PORT2	PORT3
Idle	Internal	1	1	Data	Data	Data	Data
Idle	External	1	1	Float	Data	Address	Data
Power-down	Internal	0	0	Data	Data	Data	Data
Power-down	External	0	0	Float	Data	Data	Data

gram nory Lock s

The AT89S51 has three lock bits that can be left unprogrammed (U) or can be programmed (P) to obtain the additional features listed in the following table.

Table 6. Lock Bit Protection Modes

Program Lock Bits				
	LB1	LB2	LB3	Protection Type
1	U	U	U	No program lock features
2	P	U	U	MOVC instructions executed from external program memory are disabled from fetching code bytes from internal memory, $\overline{EA}$ is sampled and latched on reset, and further programming of the Flash memory is disabled
3	P	P	U	Same as mode 2, but verify is also disabled
4	P	P	P	Same as mode 3, but external execution is also disabled

When lock bit 1 is programmed, the logic level at the $\overline{EA}$ pin is sampled and latched during reset. If the device is powered up without a reset, the latch initializes to a random value and holds that value until reset is activated. The latched value of $\overline{EA}$ must agree with the current logic level at that pin in order for the device to function properly.

gramming Flash – allel Mode

The AT89S51 is shipped with the on-chip Flash memory array ready to be programmed. The programming interface needs a high-voltage (12-volt) program enable signal and is compatible with conventional third-party Flash or EPROM programmers.

The AT89S51 code memory array is programmed byte-by-byte.

Programming Algorithm: Before programming the AT89S51, the address, data, and control signals should be set up according to the Flash programming mode table and Figures 13 and 14. To program the AT89S51, take the following steps:

1. Input the desired memory location on the address lines.
2. Input the appropriate data byte on the data lines.
3. Activate the correct combination of control signals.
4. Raise $\overline{EA}/V_{pp}$ to 12V.
5. Pulse ALE/$\overline{PROG}$ once to program a byte in the Flash array or the lock bits. The byte-write cycle is self-timed and typically takes no more than 50 µs. Repeat steps 1 through 5, changing the address and data for the entire array or until the end of the object file is reached.

$\overline{Data}$ Polling: The AT89S51 features $\overline{Data}$ Polling to indicate the end of a byte write cycle. During a write cycle, an attempted read of the last byte written will result in the complement of the written data on P0.7. Once the write cycle has been completed, true data is valid on all outputs, and the next cycle may begin. $\overline{Data}$ Polling may begin any time after a write cycle has been initiated.

Ready/$\overline{\text{Busy}}$: The progress of byte programming can also be monitored by the RDY/$\overline{\text{BSY}}$ output signal. P3.0 is pulled low after ALE goes high during programming to indicate $\overline{\text{BUSY}}$. P3.0 is pulled high again when programming is done to indicate READY.

Program Verify: If lock bits LB1 and LB2 have not been programmed, the programmed code data can be read back via the address and data lines for verification. The status of the individual lock bits can be verified directly by reading them back.

Reading the Signature Bytes: The signature bytes are read by the same procedure as a normal verification of locations 000H, 100H, and 200H, except that P3.6 and P3.7 must be pulled to a logic low. The values returned are as follows.

(000H) = 1EH indicates manufactured by Atmel
(100H) = 51H indicates 89S51
(200H) = 06H

Chip Erase: In the parallel programming mode, a chip erase operation is initiated by using the proper combination of control signals and by pulsing ALE/$\overline{\text{PROG}}$ low for a duration of 200 ns - 500 ns.

In the serial programming mode, a chip erase operation is initiated by issuing the Chip Erase instruction. In this mode, chip erase is self-timed and takes about 500 ms.

During chip erase, a serial read from any address location will return 00H at the data output.

gramming Flash – ial Mode

The Code memory array can be programmed using the serial ISP interface while RST is pulled to V_{CC}. The serial interface consists of pins SCK, MOSI (input) and MISO (output). After RST is set high, the Programming Enable instruction needs to be executed first before other operations can be executed. Before a reprogramming sequence can occur, a Chip Erase operation is required.

The Chip Erase operation turns the content of every memory location in the Code array into FFH.

Either an external system clock can be supplied at pin XTAL1 or a crystal needs to be connected across pins XTAL1 and XTAL2. The maximum serial clock (SCK) frequency should be less than 1/16 of the crystal frequency. With a 33 MHz oscillator clock, the maximum SCK frequency is 2 MHz.

al ıramming ›rithm

To program and verify the AT89S51 in the serial programming mode, the following sequence is recommended:

1. Power-up sequence:
   Apply power between VCC and GND pins.
   Set RST pin to "H".
   If a crystal is not connected across pins XTAL1 and XTAL2, apply a 3 MHz to 33 MHz clock to XTAL1 pin and wait for at least 10 milliseconds.
2. Enable serial programming by sending the Programming Enable serial instruction to pin MOSI/P1.5. The frequency of the shift clock supplied at pin SCK/P1.7 needs to be less than the CPU clock at XTAL1 divided by 16.
3. The Code array is programmed one byte at a time in either the Byte or Page mode. The write cycle is self-timed and typically takes less than 0.5 ms at 5V.
4. Any memory location can be verified by using the Read instruction that returns the content at the selected address at serial output MISO/P1.6.
5. At the end of a programming session, RST can be set low to commence normal device operation.

Power-off sequence (if needed):

Set XTAL1 to "L" (if a crystal is not used).

Set RST to "L".

Turn V_{CC} power off.

$\overline{\text{Data}}$ Polling: The $\overline{\text{Data}}$ Polling feature is also available in the serial mode. In this mode, during a write cycle an attempted read of the last byte written will result in the complement of the MSB of the serial output byte on MISO.

al gramming ruction Set

The Instruction Set for Serial Programming follows a 4-byte protocol and is shown in Table 8 on page 18.

gramming rface – allel Mode

Every code byte in the Flash array can be programmed by using the appropriate combination of control signals. The write operation cycle is self-timed and once initiated, will automatically time itself to completion.

All major programming vendors offer worldwide support for the Atmel microcontroller series. Please contact your local programming vendor for the appropriate software revision.

7. Flash Programming Modes

	V_{CC}	RST	$\overline{\text{PSEN}}$	ALE/ $\overline{\text{PROG}}$	$\overline{\text{EA}}$/ V_{PP}	P2.6	P2.7	P3.3	P3.6	P3.7	P0.7-0 Data	P2.3-0 Address	P1.7-0 Address
Code Data	5V	H	L	(2)	12V	L	H	H	H	H	D_{IN}	A11-8	A7-0
Code Data	5V	H	L	H	H	L	L	L	H	H	D_{OUT}	A11-8	A7-0
Lock Bit 1	5V	H	L	(3)	12V	H	H	H	H	H	X	X	X
Lock Bit 2	5V	H	L	(3)	12V	H	H	H	L	L	X	X	X
Lock Bit 3	5V	H	L	(3)	12V	H	L	H	H	L	X	X	X
Lock Bits 3	5V	H	L	H	H	H	H	L	H	L	P0.2, P0.3, P0.4	X	X
Erase	5V	H	L	(1)	12V	H	L	H	L	L	X	X	X
Atmel ID	5V	H	L	H	H	L	L	L	L	L	1EH	0000	00H
Device ID	5V	H	L	H	H	L	L	L	L	L	51H	0001	00H
Device ID	5V	H	L	H	H	L	L	L	L	L	06H	0010	00H

1. Each $\overline{\text{PROG}}$ pulse is 200 ns - 500 ns for Chip Erase.
2. Each $\overline{\text{PROG}}$ pulse is 200 ns - 500 ns for Write Code Data.
3. Each $\overline{\text{PROG}}$ pulse is 200 ns - 500 ns for Write Lock Bits.
4. RDY/$\overline{\text{BSY}}$ signal is output on P3.0 during programming.
5. X = don't care.

Figure 4. Programming the Flash Memory (Parallel Mode)

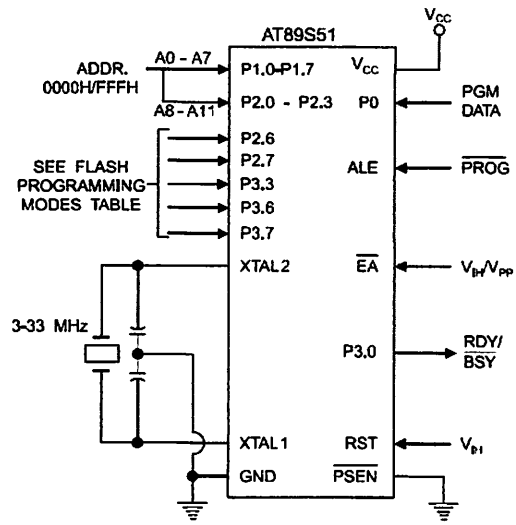
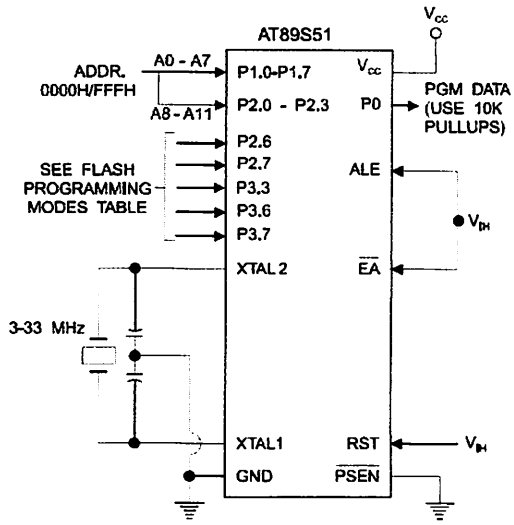


Figure 5. Verifying the Flash Memory (Parallel Mode)

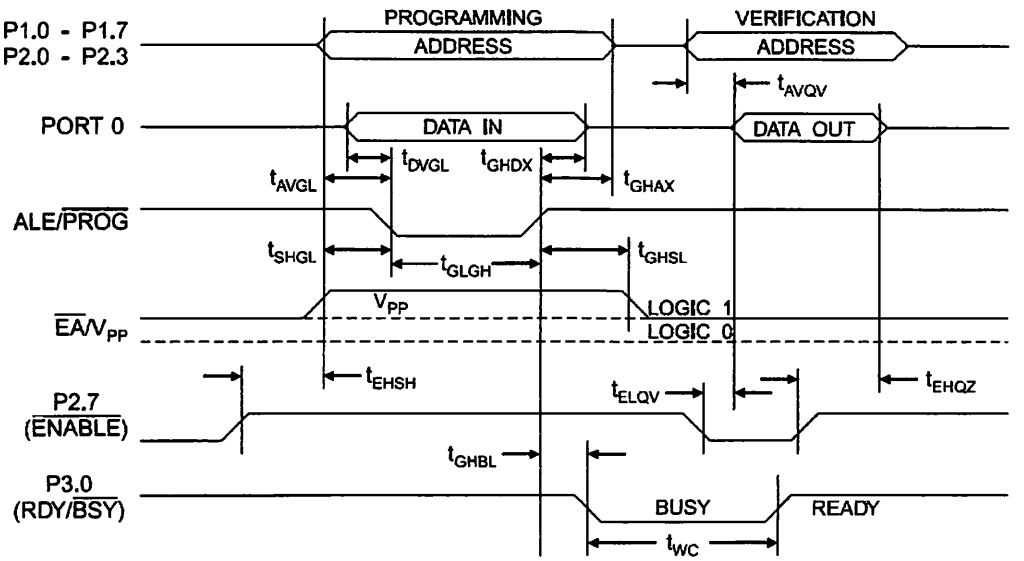


h Programming and Verification Characteristics (Parallel Mode)

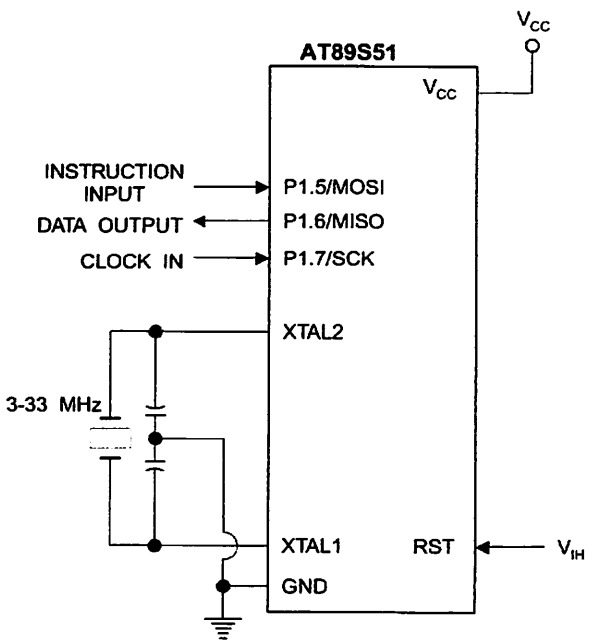
0°C to 30°C, V_{CC} = 4.5 to 5.5V

ol	Parameter	Min	Max	Units
	Programming Supply Voltage	11.5	12.5	V
	Programming Supply Current		10	mA
	V_{CC} Supply Current		30	mA
L	Oscillator Frequency	3	33	MHz
	Address Setup to $\overline{PROG}$ Low	$48t_{CLCL}$		
	Address Hold After $\overline{PROG}$	$48t_{CLCL}$		
	Data Setup to $\overline{PROG}$ Low	$48t_{CLCL}$		
	Data Hold After $\overline{PROG}$	$48t_{CLCL}$		
	P2.7 ($\overline{ENABLE}$) High to V_{PP}	$48t_{CLCL}$		
	V_{PP} Setup to $\overline{PROG}$ Low	10		µs
	V_{PP} Hold After $\overline{PROG}$	10		µs
	$\overline{PROG}$ Width	0.2	1	µs
	Address to Data Valid		$48t_{CLCL}$	
	$\overline{ENABLE}$ Low to Data Valid		$48t_{CLCL}$	
	Data Float After $\overline{ENABLE}$	0	$48t_{CLCL}$	
	$\overline{PROG}$ High to $\overline{BUSY}$ Low		1.0	µs
	Byte Write Cycle Time		50	µs

6. Flash Programming and Verification Waveforms – Parallel Mode

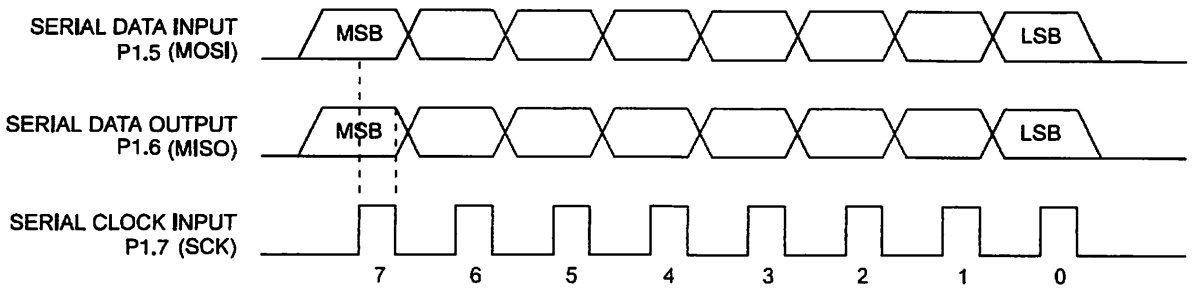


e 7. Flash Memory Serial Downloading



h Programming and Verification Waveforms – Serial Mode

i 8. Serial Programming Waveforms



e 8. Serial Programming Instruction Set

ruction	Instruction Format Byte 1	Byte 2	Byte 3	Byte 4	Operation
gramming Enable	1010 1100	0101 0011	xxxx xxxx	xxxx xxxx 0110 1001 (Output)	Enable Serial Programming while RST is high
) Erase	1010 1100	100x xxxx	xxxx xxxx	xxxx xxxx	Chip Erase Flash memory array
d Program Memory e Mode)	0010 0000	xxxx A11 A10 A9 A8	A7 A6 A5 A4 A3 A2 A1 A0	D7 D6 D5 D4 D3 D2 D1 D0	Read data from Program memory in the byte mode
e Program Memory e Mode)	0100 0000	xxxx A11 A10 A9 A8	A7 A6 A5 A4 A3 A2 A1 A0	D7 D6 D5 D4 D3 D2 D1 D0	Write data to Program memory in the byte mode
e Lock Bits(2)	1010 1100	1110 00 B1 B2	xxxx xxxx	xxxx xxxx	Write Lock bits. See Note (2).
d Lock Bits	0010 0100	xxxx xxxx	xxxx xxxx	xx LB3 LB2 LB1 xx	Read back current status of the lock bits (a programmed lock bit reads back as a "1")
d Signature Bytes(1)	0010 1000	xxx A5 A4 A3 A2 A1	A0 xxx xxxx	Signature Byte	Read Signature Byte
d Program Memory e Mode)	0011 0000	xxxx A11 A10 A9 A8	Byte 0	Byte 1... Byte 255	Read data from Program memory in the Page Mode (256 bytes)
e Program Memory e Mode)	0101 0000	xxxx A11 A10 A9 A8	Byte 0	Byte 1... Byte 255	Write data to Program memory in the Page Mode (256 bytes)

1. The signature bytes are not readable in Lock Bit Modes 3 and 4.
2. B1 = 0, B2 = 0 →Mode 1, no lock protection
   B1 = 0, B2 = 1 →Mode 2, lock bit 1 activated
   B1 = 1, B2 = 0 →Mode 3, lock bit 2 activated
   B1 = 1, B1 = 1 →Mode 4, lock bit 3 activated

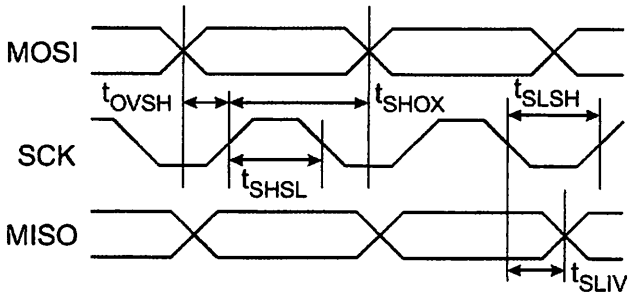
   } Each of the lock bits needs to be activated sequentially before Mode 4 can be executed.

After Reset signal is high, SCK should be low for at least 64 system clocks before it goes high to clock in the enable data bytes. No pulsing of Reset signal is necessary. SCK should be no faster than 1/16 of the system clock at XTAL1.

For Page Read/Write, the data always starts from byte 0 to 255. After the command byte and upper address byte are latched, each byte thereafter is treated as data until all 256 bytes are shifted in/out. Then the next instruction will be ready to be decoded.

rial Programming Characteristics

ure 9. Serial Programming Timing



le 9. Serial Programming Characteristics, T_A = -40° C to 85° C, V_{CC} = 4.0 - 5.5V (Unless Otherwise Noted)

mbol	Parameter	Min	Typ	Max	Units
CLCL	Oscillator Frequency	0		33	MHz
CL	Oscillator Period	30			ns
SL	SCK Pulse Width High	8 t_{CLCL}			ns
SH	SCK Pulse Width Low	8 t_{CLCL}			ns
SH	MOSI Setup to SCK High	t_{CLCL}			ns
OX	MOSI Hold after SCK High	2 t_{CLCL}			ns
V	SCK Low to MISO Valid	10	16	32	ns
ASE	Chip Erase Instruction Cycle Time			500	ms
C	Serial Byte Write Cycle Time			64 t_{CLCL} + 400	µs

olute Maximum Ratings*

ating Temperature	-55°C to +125°C
ge Temperature	-65°C to +150°C
ge on Any Pin Respect to Ground	-1.0V to +7.0V
num Operating Voltage	6.6V
utput Current	15.0 mA

*NOTICE: Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Characteristics

alues shown in this table are valid for T_A = -40°C to 85°C and V_{CC} = 4.0V to 5.5V, unless otherwise noted.

ol	Parameter	Condition	Min	Max	Units
	Input Low Voltage	(Except $\overline{EA}$)	-0.5	0.2 V_{CC}-0.1	V
	Input Low Voltage ($\overline{EA}$)		-0.5	0.2 V_{CC}-0.3	V
	Input High Voltage	(Except XTAL1, RST)	0.2 V_{CC}+0.9	V_{CC}+0.5	V
	Input High Voltage	(XTAL1, RST)	0.7 V_{CC}	V_{CC}+0.5	V
	Output Low Voltage[1] (Ports 1,2,3)	I_{OL} = 1.6 mA		0.45	V
	Output Low Voltage[1] (Port 0, ALE, $\overline{PSEN}$)	I_{OL} = 3.2 mA		0.45	V
	Output High Voltage (Ports 1,2,3, ALE, $\overline{PSEN}$)	I_{OH} = -60 µA, V_{CC} = 5V ± 10%	2.4		V
		I_{OH} = -25 µA	0.75 V_{CC}		V
		I_{OH} = -10 µA	0.9 V_{CC}		V
	Output High Voltage (Port 0 in External Bus Mode)	I_{OH} = -800 µA, V_{CC} = 5V ± 10%	2.4		V
		I_{OH} = -300 µA	0.75 V_{CC}		V
		I_{OH} = -80 µA	0.9 V_{CC}		V
	Logical 0 Input Current (Ports 1,2,3)	V_{IN} = 0.45V		-50	µA
	Logical 1 to 0 Transition Current (Ports 1,2,3)	V_{IN} = 2V, V_{CC} = 5V ± 10%		-650	µA
	Input Leakage Current (Port 0, $\overline{EA}$)	0.45 < V_{IN} < V_{CC}		±10	µA
-	Reset Pulldown Resistor		50	300	KΩ
	Pin Capacitance	Test Freq. = 1 MHz, T_A = 25°C		10	pF
	Power Supply Current	Active Mode, 12 MHz		25	mA
		Idle Mode, 12 MHz		6.5	mA
	Power-down Mode[2]	V_{CC} = 5.5V		50	µA

1. Under steady state (non-transient) conditions, I_{OL} must be externally limited as follows:
   Maximum I_{OL} per port pin: 10 mA
   Maximum I_{OL} per 8-bit port:
   Port 0: 26 mA Ports 1, 2, 3: 15 mA
   Maximum total I_{OL} for all output pins: 71 mA
   If I_{OL} exceeds the test condition, V_{OL} may exceed the related specification. Pins are not guaranteed to sink current greater than the listed test conditions.
2. Minimum V_{CC} for Power-down is 2V.

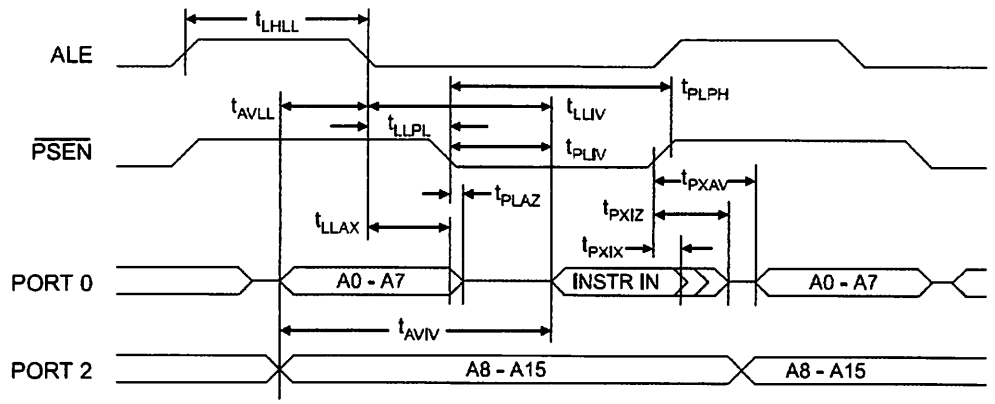
Characteristics

operating conditions, load capacitance for Port 0, ALE/$\overline{PROG}$, and $\overline{PSEN}$ = 100 pF; load capacitance for all other s = 80 pF.

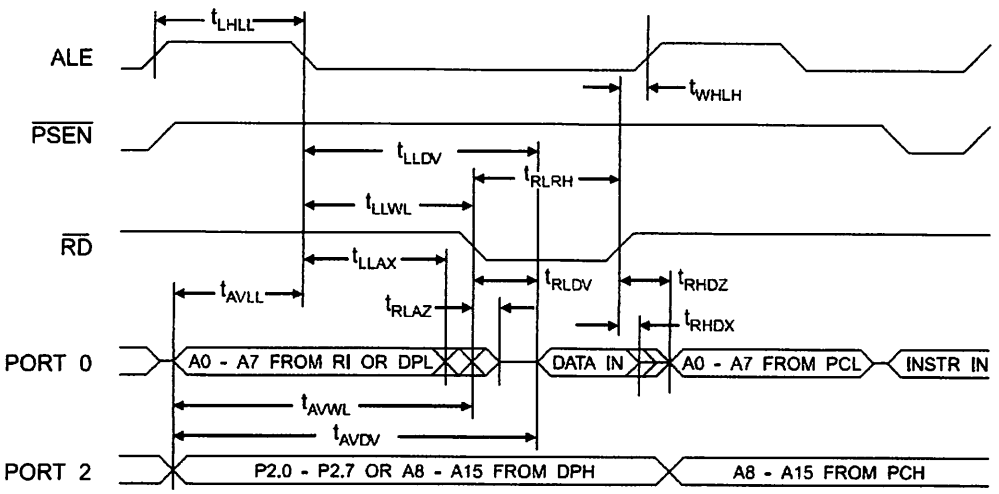
rnal Program and Data Memory Characteristics

ol	Parameter	12 MHz Oscillator		Variable Oscillator		Units
		Min	Max	Min	Max	
L	Oscillator Frequency			0	33	MHz
	ALE Pulse Width	127		$2t_{CLCL}$-40		ns
	Address Valid to ALE Low	43		t_{CLCL}-25		ns
	Address Hold After ALE Low	48		t_{CLCL}-25		ns
	ALE Low to Valid Instruction In		233		$4t_{CLCL}$-65	ns
	ALE Low to $\overline{PSEN}$ Low	43		t_{CLCL}-25		ns
	$\overline{PSEN}$ Pulse Width	205		$3t_{CLCL}$-45		ns
	$\overline{PSEN}$ Low to Valid Instruction In		145		$3t_{CLCL}$-60	ns
	Input Instruction Hold After $\overline{PSEN}$	0		0		ns
	Input Instruction Float After $\overline{PSEN}$		59		t_{CLCL}-25	ns
	$\overline{PSEN}$ to Address Valid	75		t_{CLCL}-8		ns
	Address to Valid Instruction In		312		$5t_{CLCL}$-80	ns
	$\overline{PSEN}$ Low to Address Float		10		10	ns
	$\overline{RD}$ Pulse Width	400		$6t_{CLCL}$-100		ns
	$\overline{WR}$ Pulse Width	400		$6t_{CLCL}$-100		ns
	$\overline{RD}$ Low to Valid Data In		252		$5t_{CLCL}$-90	ns
	Data Hold After $\overline{RD}$	0		0		ns
	Data Float After $\overline{RD}$		97		$2t_{CLCL}$-28	ns
	ALE Low to Valid Data In		517		$8t_{CLCL}$-150	ns
	Address to Valid Data In		585		$9t_{CLCL}$-165	ns
	ALE Low to $\overline{RD}$ or $\overline{WR}$ Low	200	300	$3t_{CLCL}$-50	$3t_{CLCL}$+50	ns
	Address to $\overline{RD}$ or $\overline{WR}$ Low	203		$4t_{CLCL}$-75		ns
	Data Valid to $\overline{WR}$ Transition	23		t_{CLCL}-30		ns
	Data Valid to $\overline{WR}$ High	433		$7t_{CLCL}$-130		ns
	Data Hold After $\overline{WR}$	33		t_{CLCL}-25		ns
	$\overline{RD}$ Low to Address Float		0		0	ns
	$\overline{RD}$ or $\overline{WR}$ High to ALE High	43	123	t_{CLCL}-25	t_{CLCL}+25	ns

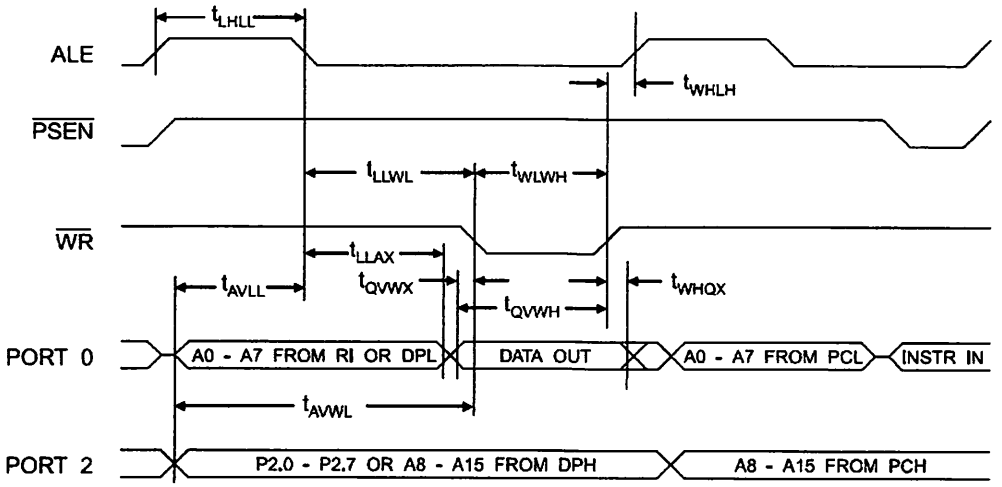
rnal Program Memory Read Cycle



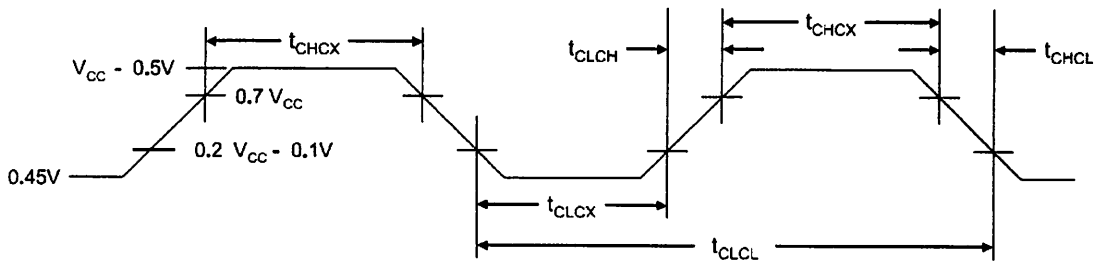
rnal Data Memory Read Cycle



rnal Data Memory Write Cycle



rnal Clock Drive Waveforms



rnal Clock Drive

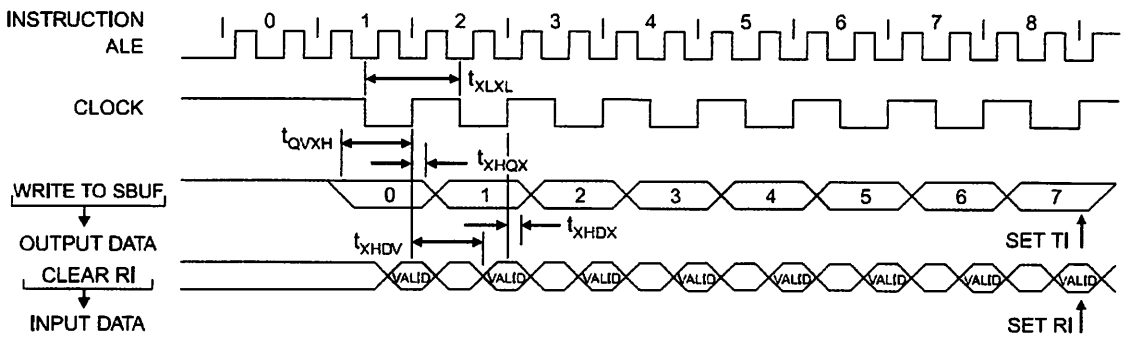
ol	Parameter	Min	Max	Units
L	Oscillator Frequency	0	33	MHz
	Clock Period	30		ns
	High Time	12		ns
	Low Time	12		ns
	Rise Time		5	ns
	Fall Time		5	ns

al Port Timing: Shift Register Mode Test Conditions

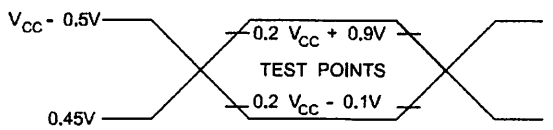
ılues in this table are valid for V_{CC} = 4.0V to 5.5V and Load Capacitance = 80 pF.

›ol	Parameter	12 MHz Osc		Variable Oscillator		Units
		Min	Max	Min	Max	
	Serial Port Clock Cycle Time	1.0		$12t_{CLCL}$		µs
	Output Data Setup to Clock Rising Edge	700		$10t_{CLCL}$-133		ns
	Output Data Hold After Clock Rising Edge	50		$2t_{CLCL}$-80		ns
	Input Data Hold After Clock Rising Edge	0		0		ns
	Clock Rising Edge to Input Data Valid		700		$10t_{CLCL}$-133	ns

t Register Mode Timing Waveforms

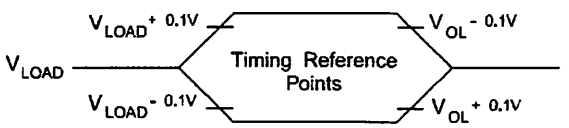


˙esting Input/Output Waveforms(1)



1. AC Inputs during testing are driven at V_{CC} - 0.5V for a logic 1 and 0.45V for a logic 0. Timing measurements are made at V_{IH} min. for a logic 1 and V_{IL} max. for a logic 0.

t Waveforms(1)



1. For timing purposes, a port pin is no longer floating when a 100 mV change from load voltage occurs. A port pin begins to float when a 100 mV change from the loaded V_{OH}/V_{OL} level occurs.

lering Information

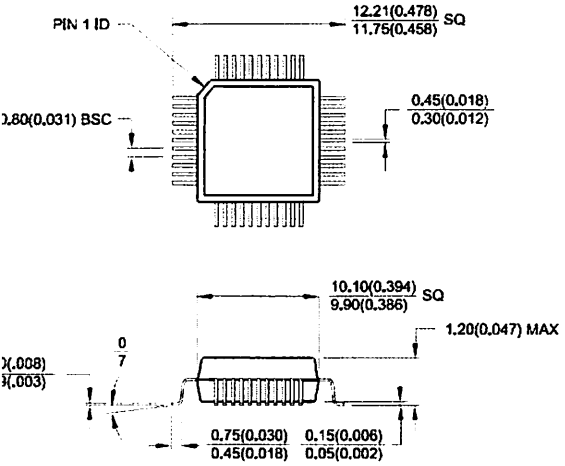
peed MHz)	Power Supply	Ordering Code	Package	Operation Range
24	4.0V to 5.5V	AT89S51-24AC AT89S51-24JC AT89S51-24PC	44A 44J 40P6	Commercial (0° C to 70° C)
		AT89S51-24AI AT89S51-24JI AT89S51-24PI	44A 44J 40P6	Industrial (-40° C to 85° C)
33	4.5V to 5.5V	AT89S51-33AC AT89S51-33JC AT89S51-33PC	44A 44J 40P6	Commercial (0° C to 70° C)

= Preliminary Availability

Package Type	
	44-lead, Thin Plastic Gull Wing Quad Flatpack (TQFP)
	44-lead, Plastic J-leaded Chip Carrier (PLCC)
	40-pin, 0.600" Wide, Plastic Dual Inline Package (PDIP)

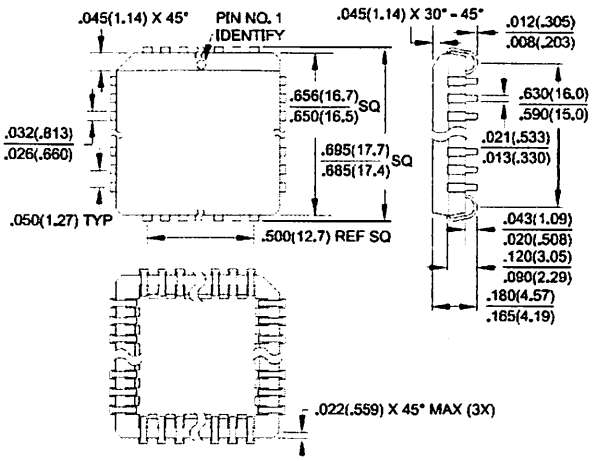
kaging Information

A, 44-lead, Thin (1.0 mm) Plastic Gull Wing Quad
at Package (TQFP)
nensions in Millimeters and (Inches)*

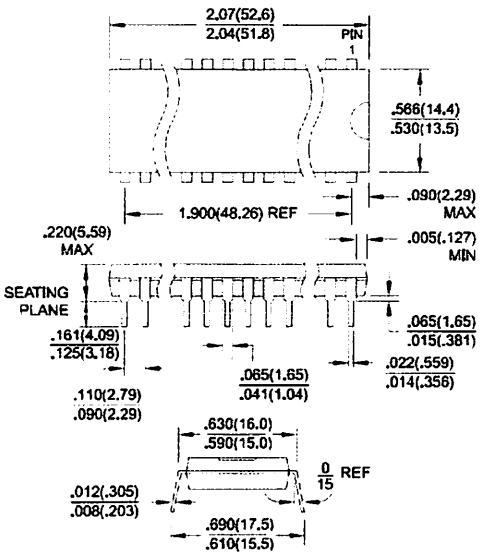


ontrolling dimension: millimeters

44J, 44-lead, Plastic J-leaded Chip Carrier (PLCC)
Dimensions in Inches and (Millimeters)



P6, 40-pin, 0.600" Wide, Plastic Dual Inline
ckage (PDIP)
nensions in Inches and (Millimeters)
)EC STANDARD MS-011 AC



nel Headquarters

porate Headquarters
525 Orchard Parkway
an Jose, CA 95131
EL (408) 441-0311
AX (408) 487-2600

ope
mel SarL
oute des Arsenaux 41
asa Postale 80
-1705 Fribourg
vitzerland
EL (41) 26-426-5555
AX (41) 26-426-5500

mel Asia, Ltd.
om 1219
inachem Golden Plaza
Mody Road Tsimhatsui
st Kowloon
ng Kong
EL (852) 2721-9778
AX (852) 2722-1369

n
nel Japan K.K.
, Tonetsu Shinkawa Bldg.
24-8 Shinkawa
uo-ku, Tokyo 104-0033
pan
L (81) 3-3523-3551
X (81) 3-3523-7581

Atmel Product Operations

Atmel Colorado Springs
1150 E. Cheyenne Mtn. Blvd.
Colorado Springs, CO 80906
TEL (719) 576-3300
FAX (719) 540-1759

Atmel Grenoble
Avenue de Rochepleine
BP 123
38521 Saint-Egreve Cedex, France
TEL (33) 4-7658-3000
FAX (33) 4-7658-3480

Atmel Heilbronn
Theresienstrasse 2
POB 3535
D-74025 Heilbronn, Germany
TEL (49) 71 31 67 25 94
FAX (49) 71 31 67 24 23

Atmel Nantes
La Chantrerie
BP 70602
44306 Nantes Cedex 3, France
TEL (33) 0 2 40 18 18 18
FAX (33) 0 2 40 18 19 60

Atmel Rousset
Zone Industrielle
13106 Rousset Cedex, France
TEL (33) 4-4253-6000
FAX (33) 4-4253-6001

Atmel Smart Card ICs
Scottish Enterprise Technology Park
East Kilbride, Scotland G75 0QR
TEL (44) 1355-357-000
FAX (44) 1355-242-743

e-mail
literature@atmel.com

Web Site
http://www.atmel.com

2487A–10/01/xM

HARRIS Semiconductor

ADC0802, ADC0803 ADC0804

8-Bit, Microprocessor-Compatible, A/D Converters

igust 1997

Features

- **80C48 and 80C80/85 Bus Compatible - No Interfacing Logic Required**
- **Conversion Time < 100μs**
- **Easy Interface to Most Microprocessors**
- **Will Operate in a "Stand Alone" Mode**
- **Differential Analog Voltage Inputs**
- **Works with Bandgap Voltage References**
- **TTL Compatible Inputs and Outputs**
- **On-Chip Clock Generator**
- **0V to 5V Analog Voltage Input Range (Single + 5V Supply)**
- **No Zero-Adjust Required**

Description

The ADC0802 family are CMOS 8-Bit, successive-approximation A/D converters which use a modified potentiometric ladder and are designed to operate with the 8080A control bus via three-state outputs. These converters appear to the processor as memory locations or I/O ports, and hence no interfacing logic is required.

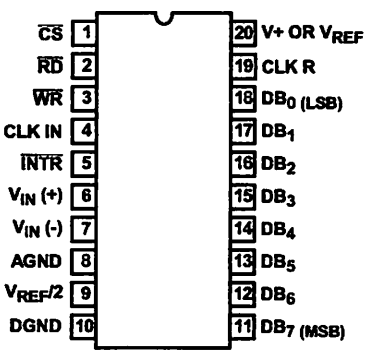
The differential analog voltage input has good common-mode-rejection and permits offsetting the analog zero-input-voltage value. In addition, the voltage reference input can be adjusted to allow encoding any smaller analog voltage span to the full 8 bits of resolution.

Ordering Information

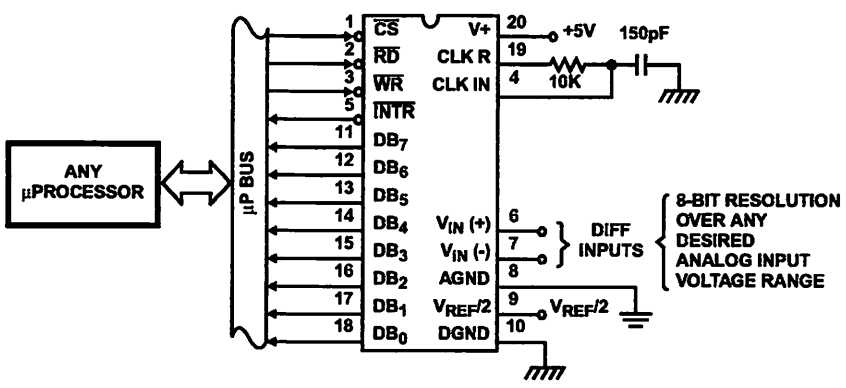
PART NUMBER	ERROR	EXTERNAL CONDITIONS	TEMP. RANGE (°C)	PACKAGE	PKG. NO
ADC0802LCN	$\pm^1/_2$ LSB	$V_{REF}/2 = 2.500V_{DC}$ (No Adjustments)	0 to 70	20 Ld PDIP	E20.3
ADC0802LCD	$\pm^3/_4$ LSB		-40 to 85	20 Ld CERDIP	F20.3
ADC0802LD	±1 LSB		-55 to 125	20 Ld CERDIP	F20.3
ADC0803LCN	$\pm^1/_2$ LSB	$V_{REF}/2$ Adjusted for Correct Full Scale Reading	0 to 70	20 Ld PDIP	E20.3
ADC0803LCD	$\pm^3/_4$ LSB		-40 to 85	20 Ld CERDIP	F20.3
ADC0803LCWM	±1 LSB		-40 to 85	20 Ld SOIC	M20.3
ADC0803LD	±1 LSB		-55 to 125	20 Ld CERDIP	F20.3
ADC0804LCN	±1 LSB	$V_{REF}/2 = 2.500V_{DC}$ (No Adjustments)	0 to 70	20 Ld PDIP	E20.3
ADC0804LCD	±1 LSB		-40 to 85	20 Ld CERDIP	F20.3
ADC0804LCWM	±1 LSB		-40 to 85	20 Ld SOIC	M20.3

Pinout

ADC0802, ADC0803, ADC0804
(PDIP, CERDIP)
TOP VIEW

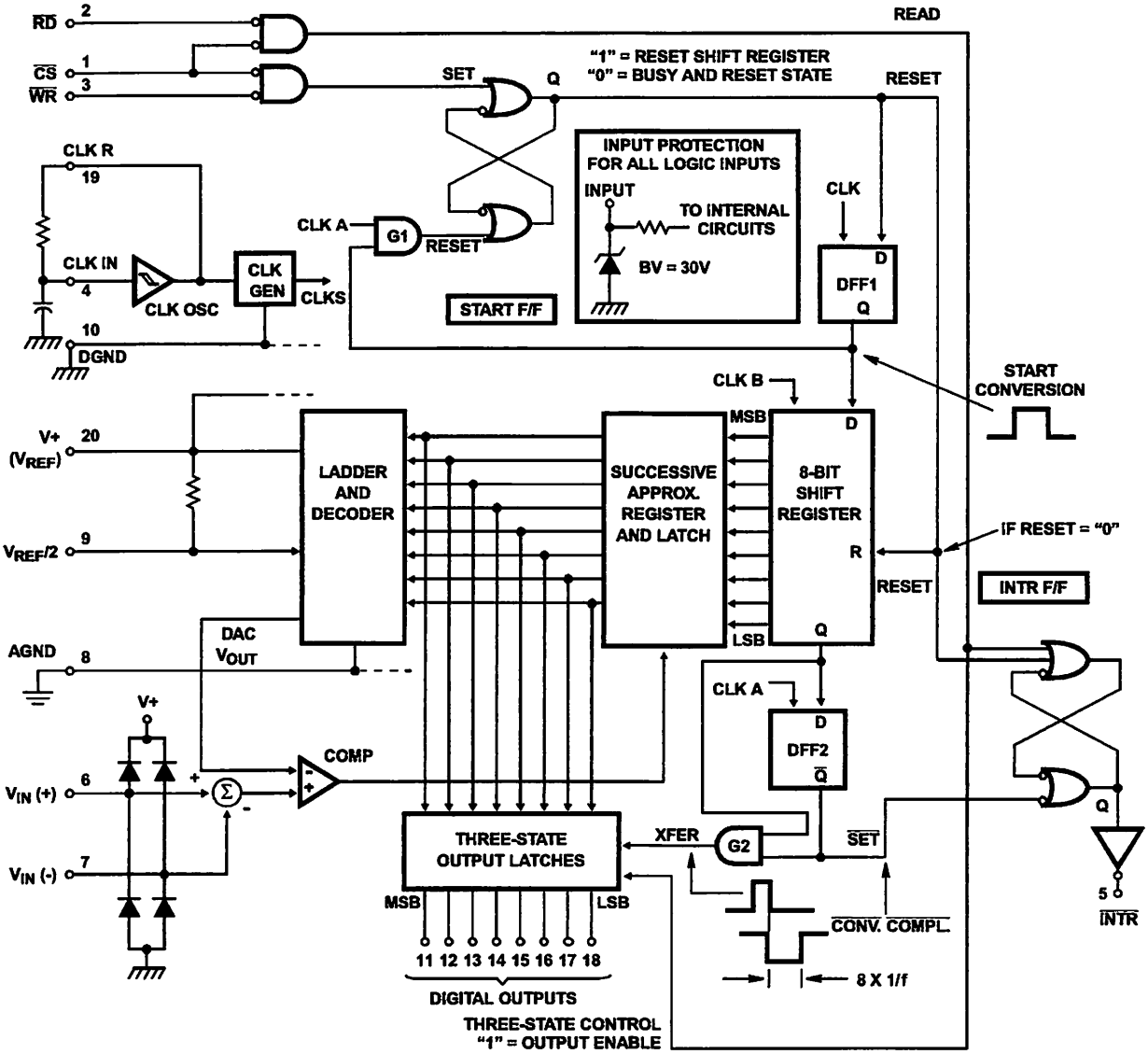


Typical Application Schematic



File Number **3094.1**

Functional Diagram



Absolute Maximum Ratings

Supply Voltage 6.5V
Voltage at Any Input . . . . . -0.3V to (V^+ +0.3V)

Operating Conditions

Temperature Range
ADC0802/03LD . . . . . -55°C to 125°C
ADC0802/03/04LCD . . . . . -40°C to 85°C
ADC0802/03/04LCN . . . . . 0°C to 70°C
ADC0803/04LCWM . . . . . -40°C to 85°C

Thermal Information

Thermal Resistance (Typical, Note 1)	θ_{JA} (°C/W)	θ_{JC} (°C/W)
PDIP Package	125	N/A
CERDIP Package	80	20
SOIC Package	120	N/A

Maximum Junction Temperature
Hermetic Package . . . . . 175°C
Plastic Package . . . . . 150°C
Maximum Storage Temperature Range . . . . . -65°C to 150°C
Maximum Lead Temperature (Soldering, 10s) . . . . . 300°C
(SOIC - Lead Tips Only)

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

NOTE:

1. θ_{JA} is measured with the component mounted on an evaluation PC board in free air.

Electrical Specifications (Notes 1, 7)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
CONVERTER SPECIFICATIONS	V+ = 5V, T_A = 25°C and f_{CLK} = 640kHz, Unless Otherwise Specified				
Total Unadjusted Error					
ADC0802	$V_{REF}/2$ = 2.500V	-	-	$\pm 1/2$	LSB
ADC0803	$V_{REF}/2$ Adjusted for Correct Full Scale Reading	-	-	$\pm 1/2$	LSB
ADC0804	$V_{REF}/2$ = 2.500V	-	-	±1	LSB
$V_{REF}/2$ Input Resistance	Input Resistance at Pin 9	1.0	1.3	-	kΩ
Analog Input Voltage Range	(Note 2)	GND-0.05	-	(V+) + 0.05	V
DC Common-Mode Rejection	Over Analog Input Voltage Range	-	$\pm 1/16$	$\pm 1/8$	LSB
Power Supply Sensitivity	V+ = 5V ±10% Over Allowed Input Voltage Range	-	$\pm 1/16$	$\pm 1/8$	LSB
CONVERTER SPECIFICATIONS	V+ = 5V, 0°C to 70°C and f_{CLK} = 640kHz, Unless Otherwise Specified				
Total Unadjusted Error					
ADC0802	$V_{REF}/2$ = 2.500V	-	-	$\pm 1/2$	LSB
ADC0803	$V_{REF}/2$ Adjusted for Correct Full Scale Reading	-	-	$\pm 1/2$	LSB
ADC0804	$V_{REF}/2$ = 2.500V	-	-	±1	LSB
$V_{REF}/2$ Input Resistance	Input Resistance at Pin 9	1.0	1.3	-	kΩ
Analog Input Voltage Range	(Note 2)	GND-0.05	-	(V+) + 0.05	V
DC Common-Mode Rejection	Over Analog Input Voltage Range	-	$\pm 1/8$	$\pm 1/4$	LSB
Power Supply Sensitivity	V+ = 5V ±10% Over Allowed Input Voltage Range	-	$\pm 1/16$	$\pm 1/8$	LSB
CONVERTER SPECIFICATIONS	V+ = 5V, -25°C to 85°C and f_{CLK} = 640kHz, Unless Otherwise Specified				
Total Unadjusted Error					
ADC0802	$V_{REF}/2$ = 2.500V	-	-	$\pm 3/4$	LSB
ADC0803	$V_{REF}/2$ Adjusted for Correct Full Scale Reading	-	-	$\pm 3/4$	LSB
ADC0804	$V_{REF}/2$ = 2.500V	-	-	±1	LSB
$V_{REF}/2$ Input Resistance	Input Resistance at Pin 9	1.0	1.3	-	kΩ
Analog Input Voltage Range	(Note 2)	GND-0.05	-	(V+) + 0.05	V
DC Common-Mode Rejection	Over Analog Input Voltage Range	-	$\pm 1/8$	$\pm 1/4$	LSB
Power Supply Sensitivity	V+ = 5V ±10% Over Allowed Input Voltage Range	-	$\pm 1/16$	$\pm 1/8$	LSB

Electrical Specifications (Notes 1, 7) **(Continued)**

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
CONVERTER SPECIFICATIONS V+ = 5V, -55°C to 125°C and f_{CLK} = 640kHz, Unless Otherwise Specified					
Total Unadjusted Error					
ADC0802	$V_{REF}/2$ = 2.500V	-	-	±1	LSB
ADC0803	$V_{REF}/2$ Adjusted for Correct Full Scale Reading	-	-	±1	LSB
$V_{REF}/2$ Input Resistance	Input Resistance at Pin 9	1.0	1.3	-	kΩ
Analog Input Voltage Range	(Note 2)	GND-0.05	-	(V+) + 0.05	V
DC Common-Mode Rejection	Over Analog Input Voltage Range	-	$\pm 1/8$	$\pm 1/4$	LSB
Power Supply Sensitivity	V+ = 5V ±10% Over Allowed Input Voltage Range	-	$\pm 1/8$	$\pm 1/4$	LSB
AC TIMING SPECIFICATIONS V+ = 5V, and T_A = 25°C, Unless Otherwise Specified					
Clock Frequency, f_{CLK}	V+ = 6V (Note 3)	100	640	1280	kHz
	V+ = 5V	100	640	800	kHz
Clock Periods per Conversion (Note 4), t_{CONV}		62	-	73	Clocks/Conv
Conversion Rate In Free-Running Mode, CR	$\overline{INTR}$ tied to $\overline{WR}$ with $\overline{CS}$ = 0V, f_{CLK} = 640kHz	-	-	8888	Conv/s
Width of $\overline{WR}$ Input (Start Pulse Width), $t_{W(WR)l}$	$\overline{CS}$ = 0V (Note 5)	100	-	-	ns
Access Time (Delay from Falling Edge of $\overline{RD}$ to Output Data Valid), t_{ACC}	C_L = 100pF (Use Bus Driver IC for Larger C_L)	-	135	200	ns
Three-State Control (Delay from Rising Edge of $\overline{RD}$ to HI-Z State), t_{1H}, t_{0H}	C_L = 10pF, R_L = 10K (See Three-State Test Circuits)	-	125	250	ns
Delay from Falling Edge of $\overline{WR}$ to Reset of $\overline{INTR}$, t_{WI}, t_{RI}		-	300	450	ns
Input Capacitance of Logic Control Inputs, C_{IN}		-	5	-	pF
Three-State Output Capacitance (Data Buffers), C_{OUT}		-	5	-	pF
DC DIGITAL LEVELS AND DC SPECIFICATIONS V+ = 5V, and T_{MIN} to T_{MAX}, Unless Otherwise Specified					
CONTROL INPUTS (Note 6)					
Logic "1" Input Voltage (Except Pin 4 CLK IN), V_{INH}	V+ = 5.25V	2.0	-	V+	V
Logic "0" Input Voltage (Except Pin 4 CLK IN), V_{INL}	V+ = 4.75V	-	-	0.8	V
CLK IN (Pin 4) Positive Going Threshold Voltage, $V+_{CLK}$		2.7	3.1	3.5	V
CLK IN (Pin 4) Negative Going Threshold Voltage, $V-_{CLK}$		1.5	1.8	2.1	V
CLK IN (Pin 4) Hysteresis, V_H		0.6	1.3	2.0	V
Logic "1" Input Current (All Inputs), I_{INHI}	V_{IN} = 5V	-	0.005	1	µA
Logic "0" Input Current (All Inputs), I_{INLO}	V_{IN} = 0V	-1	-0.005	-	µA
Supply Current (Includes Ladder Current), I+	f_{CLK} = 640kHz, T_A = 25°C and $\overline{CS}$ = HI	-	1.3	2.5	mA
DATA OUTPUTS AND $\overline{INTR}$					
Logic "0" Output Voltage, V_{OL}	I_O = 1.6mA, V+ = 4.75V	-	-	0.4	V

lectrical Specifications (Notes 1, 7) (Continued)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
ogic "1" Output Voltage, V_{OH}	I_O = -360µA, V+ = 4.75V	2.4	-	-	V
hree-State Disabled Output eakage (All Data Buffers), I_{LO}	V_{OUT} = 0V	-3	-	-	µA
	V_{OUT} = 5V	-	-	3	µA
)utput Short Circuit Current, SOURCE	V_{OUT} Short to Gnd T_A = 25°C	4.5	6	-	mA
)utput Short Circuit Current, SINK	V_{OUT} Short to V+ T_A = 25°C	9.0	16	-	mA

OTES:

1. All voltages are measured with respect to GND, unless otherwise specified. The separate AGND point should always be wired to the DGND, being careful to avoid ground loops.
2. For $V_{IN(-)} \geq V_{IN(+)}$ the digital output code will be 0000 0000. Two on-chip diodes are tied to each analog input (see Block Diagram) which will forward conduct for analog input voltages one diode drop below ground or one diode drop greater than the V+ supply. Be careful, during testing at low V+ levels (4.5V), as high level analog inputs (5V) can cause this input diode to conduct - especially at elevated temperatures, and cause errors for analog inputs near full scale. As long as the analog V_{IN} does not exceed the supply voltage by more than 50mV, the output code will be correct. To achieve an absolute 0V to 5V input voltage range will therefore require a minimum supply voltage of 4.950V over temperature variations, initial tolerance and loading.
3. With V+ = 6V, the digital logic interfaces are no longer TTL compatible.
4. With an asynchronous start pulse, up to 8 clock periods may be required before the internal clock phases are proper to start the conversion process.
5. The $\overline{CS}$ input is assumed to bracket the $\overline{WR}$ strobe input so that timing is dependent on the $\overline{WR}$ pulse width. An arbitrarily wide pulse width will hold the converter in a reset mode and the start of conversion is initiated by the low to high transition of the $\overline{WR}$ pulse (see Timing Diagrams).
6. CLK IN (pin 4) is the input of a Schmitt trigger circuit and is therefore specified separately.
7. None of these A/Ds requires a zero-adjust. However, if an all zero code is desired for an analog input other than 0V, or if a narrow full scale span exists (for example: 0.5V to 4V full scale) the $V_{IN(-)}$ input can be adjusted to achieve this. See the Zero Error description in this data sheet.

iming Waveforms

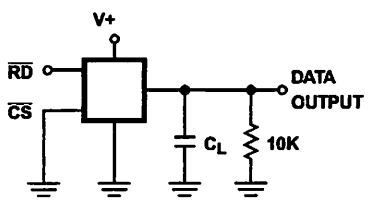


FIGURE 1A. t_{1H}

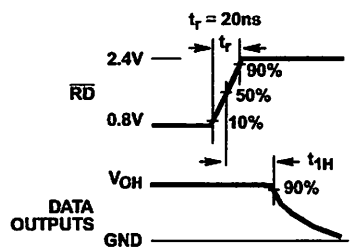


FIGURE 1B. t_{1H}, C_L = 10pF

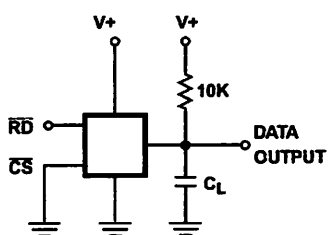


FIGURE 1C. t_{0H}

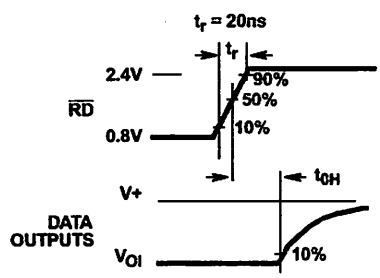


FIGURE 1D. t_{0H}, C_L = 10pF

FIGURE 1. THREE-STATE CIRCUITS AND WAVEFORMS

ypical Performance Curves

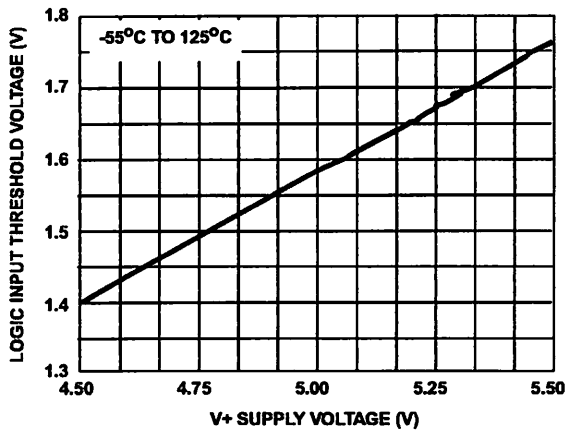


FIGURE 2. LOGIC INPUT THRESHOLD VOLTAGE vs SUPPLY VOLTAGE

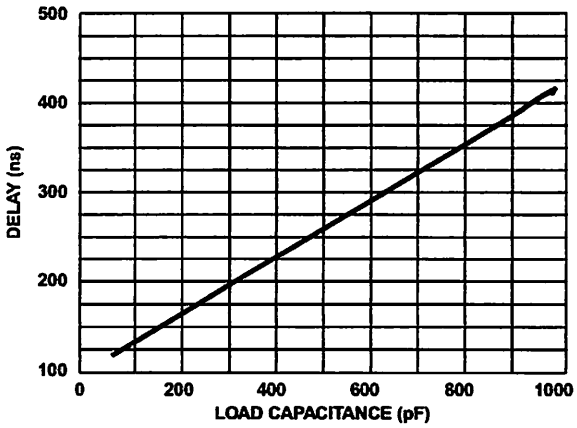
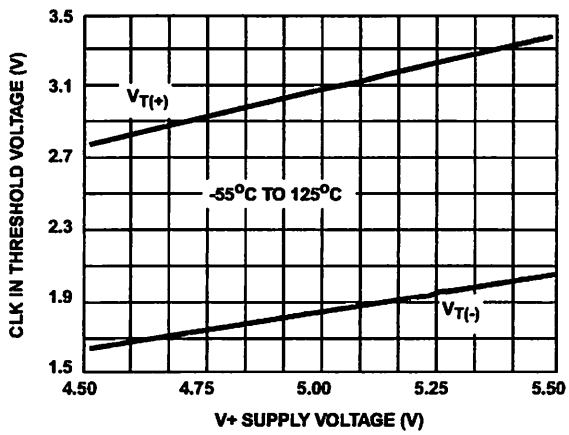


FIGURE 3. DELAY FROM FALLING EDGE OF $\overline{RD}$ TO OUTPUT DATA VALID vs LOAD CAPACITANCE



IGURE 4. CLK IN SCHMITT TRIP LEVELS vs SUPPLY VOLTAGE

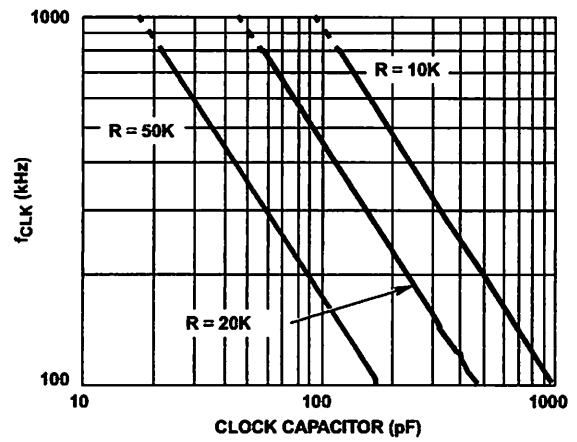


FIGURE 5. f_{CLK} vs CLOCK CAPACITOR

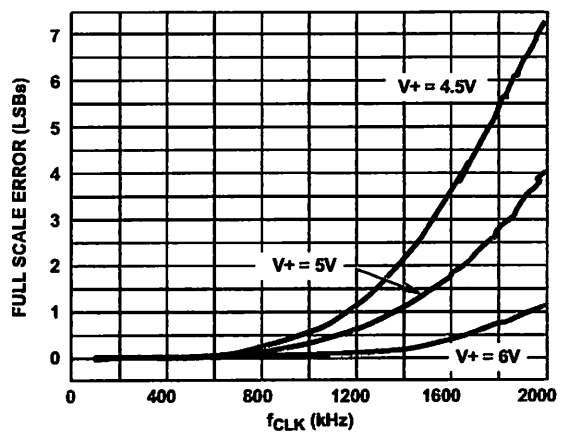


FIGURE 6. FULL SCALE ERROR vs f_{CLK}

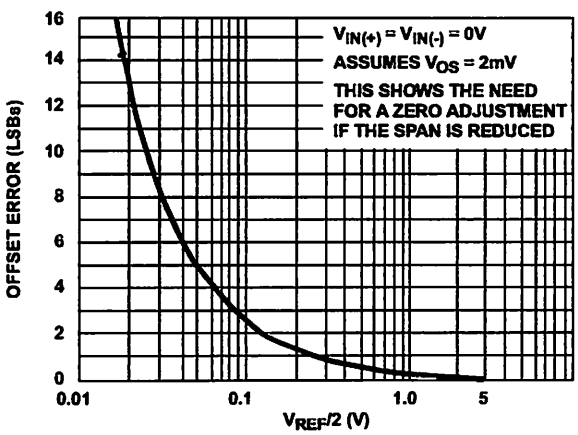


FIGURE 7. EFFECT OF UNADJUSTED OFFSET ERROR

Typical Performance Curves (Continued)

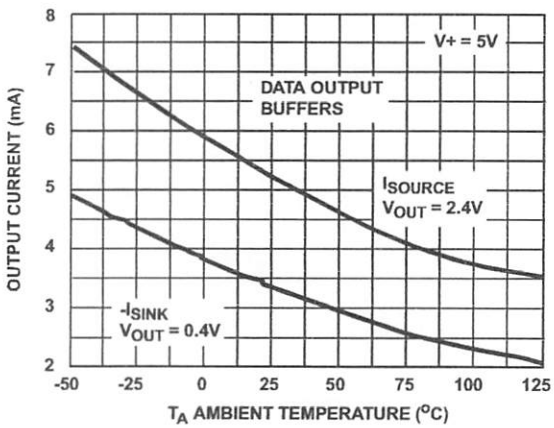


FIGURE 8. OUTPUT CURRENT vs TEMPERATURE

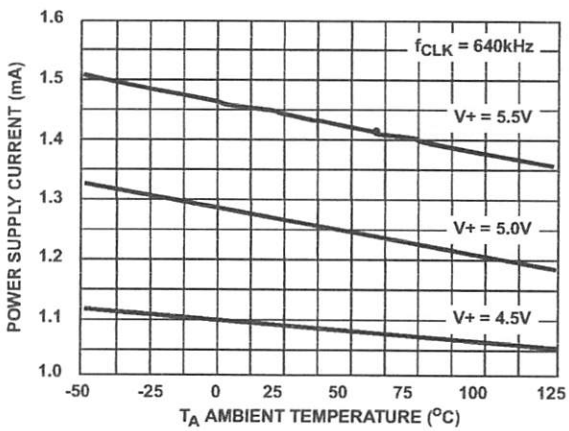


FIGURE 9. POWER SUPPLY CURRENT vs TEMPERATURE

Timing Diagrams

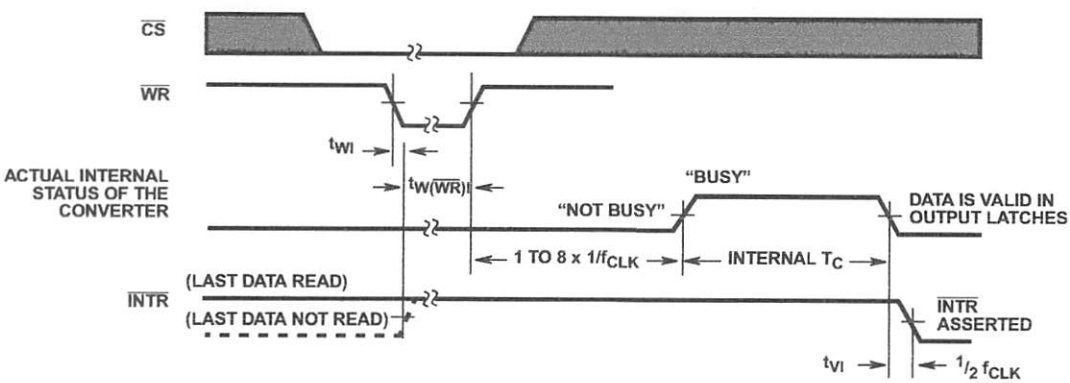


FIGURE 10A. START CONVERSION

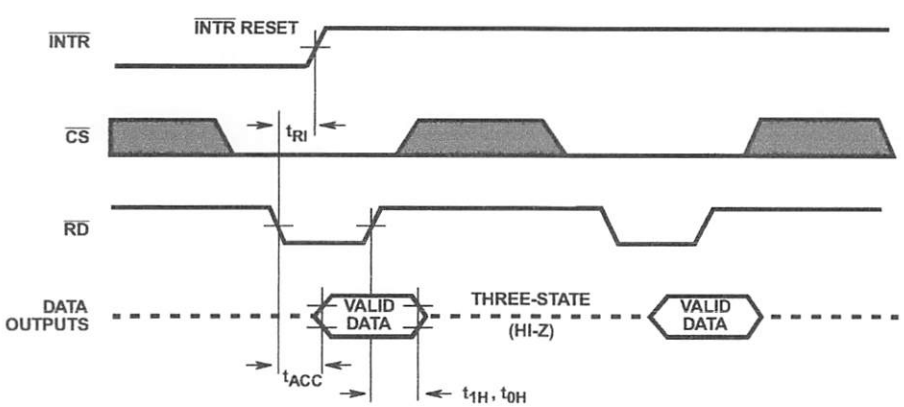


FIGURE 10B. OUTPUT ENABLE AND RESET INTR

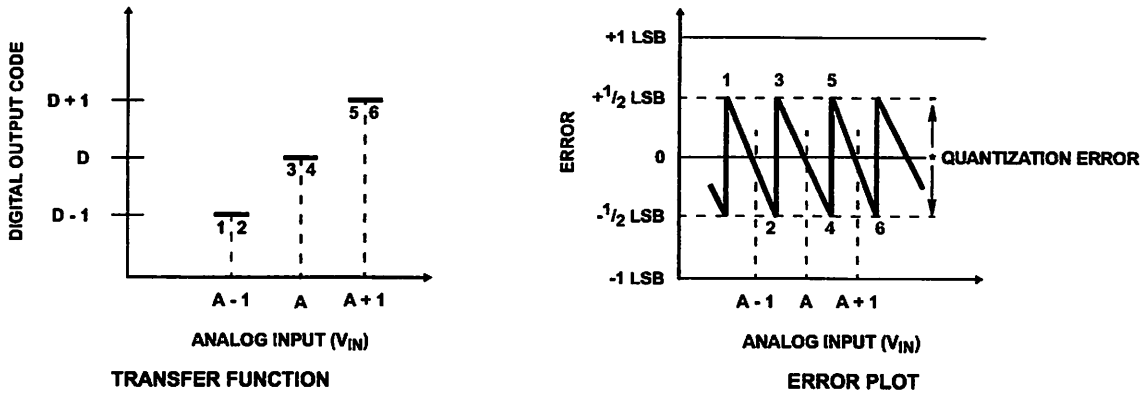


FIGURE 11A. ACCURACY = ±0 LSB; PERFECT A/D

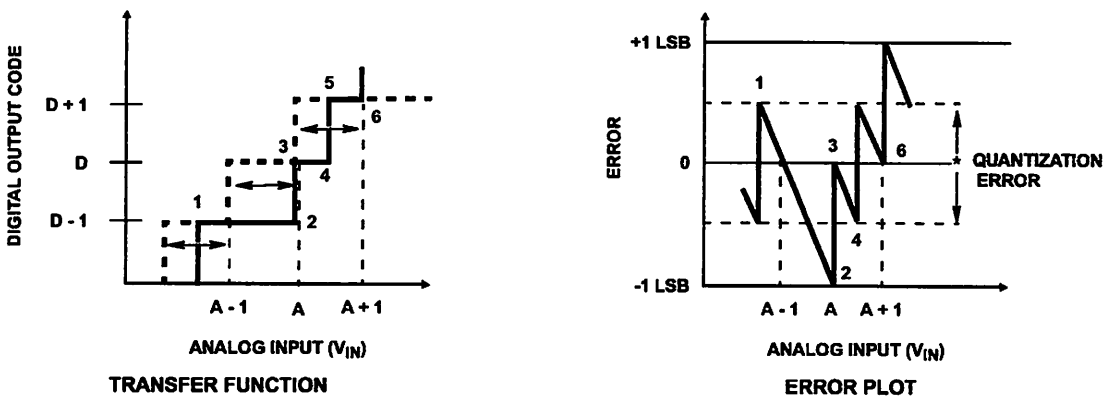


FIGURE 11B. ACCURACY = ±1/2 LSB

FIGURE 11. CLARIFYING THE ERROR SPECS OF AN A/D CONVERTER

Understanding A/D Error Specs

A perfect A/D transfer characteristic (staircase wave-form) is shown in Figure 11A. The horizontal scale is analog input voltage and the particular points labeled are in steps of 1 LSB (9.53mV with 2.5V tied to the $V_{REF}/2$ pin). The digital output codes which correspond to these inputs are shown as D-1, D, and D+1. For the perfect A/D, not only will center-value (A - 1, A, A + 1, . . .) analog inputs produce the correct output digital codes, but also each riser (the transitions between adjacent output codes) will be located ±1/2 LSB away from each center-value. As shown, the risers are ideal and have no width. Correct digital output codes will be provided for a range of analog input voltages which extend ±1/2 LSB from the ideal center-values. Each tread (the range of analog input voltage which provides the same digital output code) is therefore 1 LSB wide.

The error curve of Figure 11B shows the worst case transfer function for the ADC0802. Here the specification guarantees that if we apply an analog input equal to the LSB analog voltage center-value, the A/D will produce the correct digital code. Next to each transfer function is shown the corresponding error plot. Notice that the error includes the quantization uncertainty of the A/D. For example, the error at point 1 of Figure 11A is 1/2 LSB because the digital code appeared 1/2 LSB in advance of the center-value of the tread. The error plots always have a constant negative slope and the abrupt upside steps are always 1 LSB in magnitude, unless the device has missing codes.

Detailed Description

The functional diagram of the ADC0802 series of A/D converters operates on the successive approximation principle (see Application Notes AN016 and AN020 for a more detailed description of this principle). Analog switches are closed sequentially by successive-approximation logic until the analog differential input voltage [$V_{IN(+)} - V_{IN(-)}$] matches a voltage derived from a tapped resistor string across the reference voltage. The most significant bit is tested first and after 8 comparisons (64 clock cycles), an 8-bit binary code (1111 1111 = full scale) is transferred to an output latch.

The normal operation proceeds as follows. On the high-to-low transition of the WR input, the internal SAR latches and the shift-register stages are reset, and the INTR output will be set high. As long as the CS input and WR input remain low, the A/D will remain in a reset state. Conversion will start from 1 to 8 clock periods after at least one of these inputs makes a low-to-high transition. After the requisite number of clock pulses to complete the conversion, the INTR pin will make a high-to-low transition. This can be used to interrupt a processor, or otherwise signal the availability of a new conversion. A RD operation (with CS low) will clear the INTR line high again.

he device may be operated in the free-running mode by connecting INTR to the WR input with CS = 0. To ensure start-up nder all possible conditions, an external WR pulse is required uring the first power-up cycle. A conversion-in-process can e interrupted by issuing a second start command.

igital Operation

he converter is started by having CS and WR simultaneously w. This sets the start flip-flop (F/F) and the resulting "1" level sets the 8-bit shift register, resets the Interrupt (INTR) F/F nd inputs a "1" to the D flip-flop, DFF1, which is at the input nd of the 8-bit shift register. Internal clock signals then transr this "1" to the Q output of DFF1. The AND gate, G1, comines this "1" output with a clock signal to provide a reset gnal to the start F/F. If the set signal is no longer present ither WR or CS is a "1"), the start F/F is reset and the 8-bit ift register then can have the "1" clocked in, which starts the nversion process. If the set signal were to still be present, is reset pulse would have no effect (both outputs of the start /F would be at a "1" level) and the 8-bit shift register would ntinue to be held in the reset mode. This allows for asynronous or wide CS and WR signals.

fter the "1" is clocked through the 8-bit shift register (which mpletes the SAR operation) it appears as the input to FF2. As soon as this "1" is output from the shift register, the ND gate, G2, causes the new digital word to transfer to the hree-State output latches. When DFF2 is subsequently ocked, the $\overline{Q}$ output makes a high-to-low transition which auses the INTR F/F to set. An inverting buffer then supplies ie $\overline{INTR}$ output signal.

/hen data is to be read, the combination of both $\overline{CS}$ and $\overline{RD}$ eing low will cause the INTR F/F to be reset and the threeate output latches will be enabled to provide the 8-bit digital utputs.

igital Control Inputs

he digital control inputs (CS, RD, and WR) meet standard TL logic voltage levels. These signals are essentially equivant to the standard A/D Start and Output Enable control sigals, and are active low to allow an easy interface to icroprocessor control busses. For non-microprocessor ased applications, the CS input (pin 1) can be grounded and e standard A/D Start function obtained by an active low ulse at the WR input (pin 3). The Output Enable function is hieved by an active low pulse at the RD input (pin 2).

nalog Operation

he analog comparisons are performed by a capacitive harge summing circuit. Three capacitors (with precise ratioed alues) share a common node with the input to an autoeroed comparator. The input capacitor is switched between $V_{IN(+)}$ and $V_{IN(-)}$, while two ratioed reference capacitors are witched between taps on the reference voltage divider string. he net charge corresponds to the weighted difference etween the input and the current total value set by the sucessive approximation register. A correction is made to offset e comparison by $^1/_2$ LSB (see Figure 11A).

nalog Differential Voltage Inputs and Common-Mode ejection

his A/D gains considerable applications flexibility from the anag differential voltage input. The $V_{IN(-)}$ input (pin 7) can be used to automatically subtract a fixed voltage value from the input reading (tare correction). This is also useful in 4mA - 20mA current loop conversion. In addition, common-mode noise can be reduced by use of the differential input.

The time interval between sampling $V_{IN(+)}$ and $V_{IN(-)}$ is $4^1/_2$ clock periods. The maximum error voltage due to this slight time difference between the input voltage samples is given by:

$$\Delta V_E(MAX) = (V_{PEAK})(2\pi f_{CM})\left[\frac{4.5}{f_{CLK}}\right]$$

where:

ΔV_E is the error voltage due to sampling delay,

V_{PEAK} is the peak value of the common-mode voltage,

f_{CM} is the common-mode frequency.

For example, with a 60Hz common-mode frequency, f_{CM}, and a 640kHz A/D clock, f_{CLK}, keeping this error to $^1/_4$ LSB (~5mV) would allow a common-mode voltage, V_{PEAK}, given by:

$$V_{PEAK} = \frac{\left[\Delta V_{E(MAX)}(f_{CLK})\right]}{(2\pi f_{CM})(4.5)},$$

or

$$V_{PEAK} = \frac{(5\times10^{-3})(640\times10^{3})}{(6.28)(60)(4.5)} \cong 1.9V.$$

The allowed range of analog input voltage usually places more severe restrictions on input common-mode voltage levels than this.

An analog input voltage with a reduced span and a relatively large zero offset can be easily handled by making use of the differential input (see Reference Voltage Span Adjust).

Analog Input Current

The internal switching action causes displacement currents to flow at the analog inputs. The voltage on the on-chip capacitance to ground is switched through the analog differential input voltage, resulting in proportional currents entering the $V_{IN(+)}$ input and leaving the $V_{IN(-)}$ input. These current transients occur at the leading edge of the internal clocks. They rapidly decay and do not inherently cause errors as the on-chip comparator is strobed at the end of the clock period.

Input Bypass Capacitors

Bypass capacitors at the inputs will average these charges and cause a DC current to flow through the output resistances of the analog signal sources. This charge pumping action is worse for continuous conversions with the $V_{IN(+)}$ input voltage at full scale. For a 640kHz clock frequency with the $V_{IN(+)}$ input at 5V, this DC current is at a maximum of approximately 5μA. Therefore, **bypass capacitors should not be used at the analog inputs or the $V_{REF}/2$** pin for high resistance sources (>1kΩ). If input bypass capacitors are necessary for noise filtering and high source resistance is desirable to minimize capacitor size, the effects of the voltage drop across this input resistance, due to the average value of the input current, can be compensated by a full scale adjustment while the given source resistor and input bypass capacitor are both in place. This is possible because the average value of the input current is a precise linear function of the differential input voltage at a constant conversion rate.

Input Source Resistance

Large values of source resistance where an input bypass capacitor is not used will not cause errors since the input currents settle out prior to the comparison time. If a low-pass filter is required in the system, use a low-value series resistor (≤1kΩ) for a passive RC section or add an op amp RC active low-pass filter. For low-source-resistance applications (≤1kΩ), a 0.1µF bypass capacitor at the inputs will minimize EMI due to the series lead inductance of a long wire. A 100Ω series resistor can be used to isolate this capacitor (both the R and C are placed outside the feedback loop) from the output of an op amp, if used.

Stray Pickup

The leads to the analog inputs (pins 6 and 7) should be kept as short as possible to minimize stray signal pickup (EMI). Both EMI and undesired digital-clock coupling to these inputs can cause system errors. The source resistance for these inputs should, in general, be kept below 5kΩ. Larger values of source resistance can cause undesired signal pickup. Input bypass capacitors, placed from the analog inputs to ground, will eliminate this pickup but can create analog scale errors as these capacitors will average the transient input switching currents of the A/D (see Analog Input Current). This scale error depends on both a large source resistance and the use of an input bypass capacitor. This error can be compensated by a full scale adjustment of the A/D (see Full Scale Adjustment) with the source resistance and input bypass capacitor in place, and the desired conversion rate.

Reference Voltage Span Adjust

For maximum application flexibility, these A/Ds have been designed to accommodate a 5V, 2.5V or an adjusted voltage reference. This has been achieved in the design of the IC as shown in Figure 12.

Notice that the reference voltage for the IC is either $^1/_2$ of the voltage which is applied to the V+ supply pin, or is equal to the voltage which is externally forced at the $V_{REF}/2$ pin. This allows for a pseudo-ratiometric voltage reference using, for the V+ supply, a 5V reference voltage. Alternatively, a voltage less than 2.5V can be applied to the $V_{REF}/2$ input. The internal gain to the $V_{REF}/2$ input is 2 to allow this factor of 2 reduction in the reference voltage.

Such an adjusted reference voltage can accommodate a reduced span or dynamic voltage range of the analog input voltage. If the analog input voltage were to range from 0.5V to 4.5V, instead of 0V to 5V, the span would be 3V. With 0.5V applied to the $V_{IN(-)}$ pin to absorb the offset, the reference voltage can be made equal to $^1/_2$ of the 3V span or 1.5V. The A/D now will encode the $V_{IN(+)}$ signal from 0.5V to 3.5V with the 0.5V input corresponding to zero and the 3.5V input corresponding to full scale. The full 8 bits of resolution are therefore applied over this reduced analog input voltage range. The requisite connections are shown in Figure 13. For expanded scale inputs, the circuits of Figures 14 and 15 can be used.

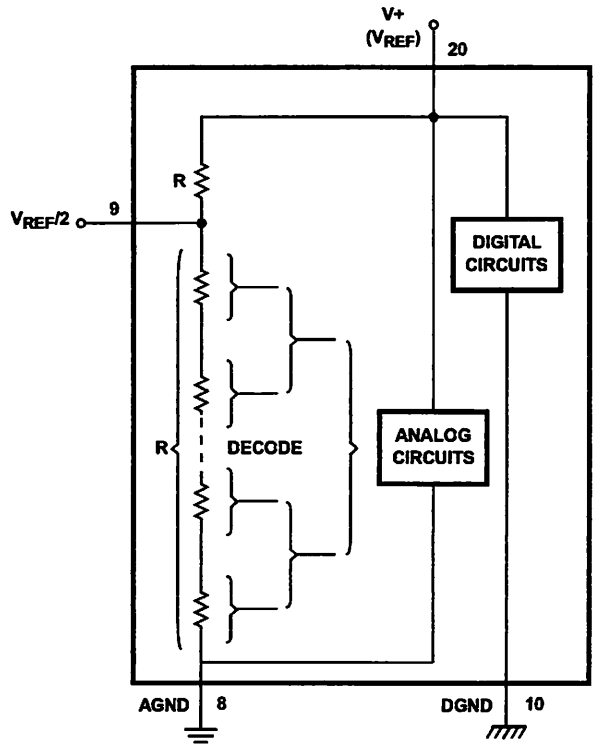


FIGURE 12. THE $V_{REFERENCE}$ DESIGN ON THE IC

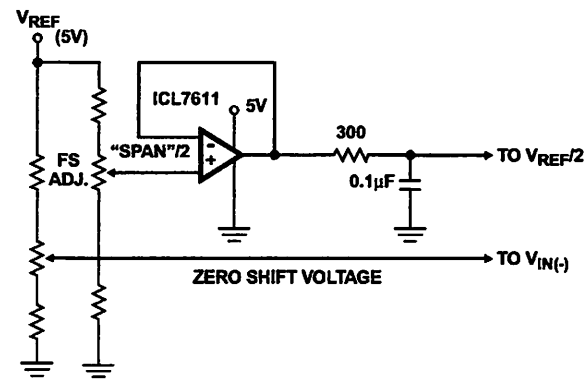


FIGURE 13. OFFSETTING THE ZERO OF THE ADC0802 AND PERFORMING AN INPUT RANGE (SPAN) ADJUSTMENT

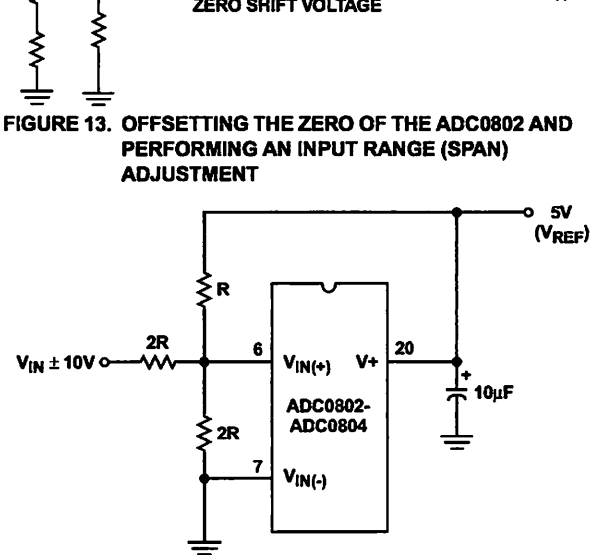


FIGURE 14. HANDLING ±10V ANALOG INPUT RANGE

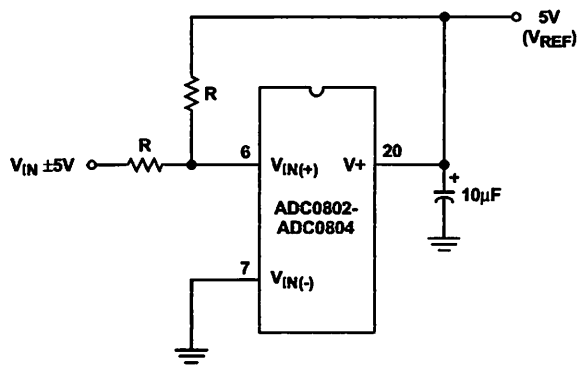


FIGURE 15. HANDLING ±5V ANALOG INPUT RANGE

eference Accuracy Requirements

he converter can be operated in a pseudo-ratiometric mode an absolute mode. In ratiometric converter applications, e magnitude of the reference voltage is a factor in both the itput of the source transducer and the output of the A/D nverter and therefore cancels out in the final digital output de. In absolute conversion applications, both the initial lue and the temperature stability of the reference voltage e important accuracy factors in the operation of the A/D nverter. For $V_{REF}/2$ voltages of 2.5V nominal value, initial rors of ±10mV will cause conversion errors of ±1 LSB due the gain of 2 of the $V_{REF}/2$ input. In reduced span applica-ns, the initial value and the stability of the $V_{REF}/2$ input ltage become even more important. For example, if the an is reduced to 2.5V, the analog input LSB voltage value correspondingly reduced from 20mV (5V span) to 10mV d 1 LSB at the $V_{REF}/2$ input becomes 5mV. As can be en, this reduces the allowed initial tolerance of the refer-ce voltage and requires correspondingly less absolute ange with temperature variations. Note that spans smaller an 2.5V place even tighter requirements on the initial accu-cy and stability of the reference source.

general, the reference voltage will require an initial justment. Errors due to an improper value of reference ltage appear as full scale errors in the A/D transfer func-n. IC voltage regulators may be used for references if the nbient temperature changes are not excessive.

ro Error

e zero of the A/D does not require adjustment. If the inimum analog input voltage value, $V_{IN(MIN)}$, is not ground, a ro offset can be done. The converter can be made to output 00 0000 digital code for this minimum input voltage by bias-g the A/D $V_{IN(-)}$ input at this $V_{IN(MIN)}$ value (see Applications ction). This utilizes the differential mode operation of the A/D.

e zero error of the A/D converter relates to the location of e first riser of the transfer function and can be measured by ounding the $V_{IN(-)}$ input and applying a small magnitude sitive voltage to the $V_{IN(+)}$ input. Zero error is the difference tween the actual DC input voltage which is necessary to st cause an output digital code transition from 0000 0000 to 00 0001 and the ideal $^1/_2$ LSB value ($^1/_2$ LSB = 9.8mV for $_{REF}/2$ = 2.500V).

Full Scale Adjust

The full scale adjustment can be made by applying a differential input voltage which is $1^1/_2$ LSB down from the desired analog full scale voltage range and then adjusting the magnitude of the $V_{REF}/2$ input (pin 9) for a digital output code which is just changing from 1111 1110 to 1111 1111. When offsetting the zero and using a span-adjusted $V_{REF}/2$ voltage, the full scale adjustment is made by inputting V_{MIN} to the $V_{IN(-)}$ input of the A/D and applying a voltage to the $V_{IN(+)}$ input which is given by:

$$V_{IN(+)}f_{SADJ} = V_{MAX} - 1.5\left[\frac{(V_{MAX} - V_{MIN})}{256}\right],$$

where:

V_{MAX} = the high end of the analog input range,

and

V_{MIN} = the low end (the offset zero) of the analog range. (Both are ground referenced.)

Clocking Option

The clock for the A/D can be derived from an external source such as the CPU clock or an external RC network can be added to provide self-clocking. The CLK IN (pin 4) makes use of a Schmitt trigger as shown in Figure 16.

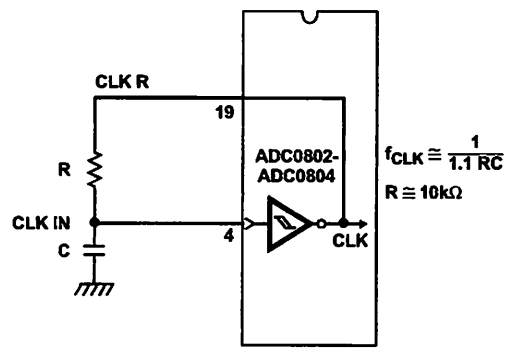


FIGURE 16. SELF-CLOCKING THE A/D

Heavy capacitive or DC loading of the CLK R pin should be avoided as this will disturb normal converter operation. Loads less than 50pF, such as driving up to 7 A/D converter clock inputs from a single CLK R pin of 1 converter, are allowed. For larger clock line loading, a CMOS or low power TTL buffer or PNP input logic should be used to minimize the loading on the CLK R pin (do not use a standard TTL buffer).

Restart During a Conversion

If the A/D is restarted ($\overline{CS}$ and $\overline{WR}$ go low and return high) during a conversion, the converter is reset and a new conversion is started. The output data latch is not updated if the conversion in progress is not completed. The data from the previous conversion remain in this latch.

Continuous Conversions

In this application, the $\overline{CS}$ input is grounded and the $\overline{WR}$ input is tied to the $\overline{INTR}$ output. This $\overline{WR}$ and $\overline{INTR}$ node should be momentarily forced to logic low following a power-up cycle to insure circuit operation. See Figure 17 for details.

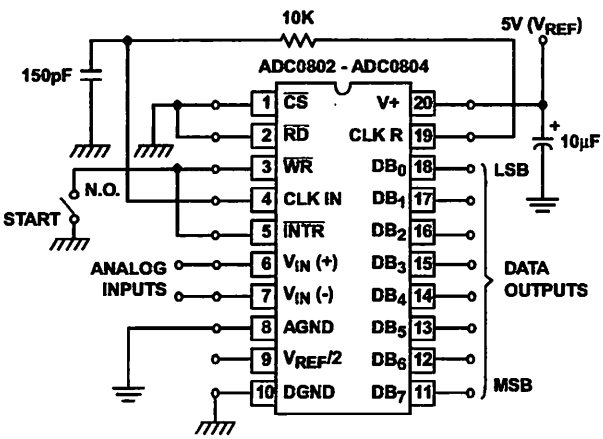


FIGURE 17. FREE-RUNNING CONNECTION

Driving the Data Bus

This CMOS A/D, like MOS microprocessors and memories, will require a bus driver when the total capacitance of the data bus gets large. Other circuitry, which is tied to the data bus, will add to the total capacitive loading, even in three-state (high-impedance mode). Back plane busing also greatly adds to the stray capacitance of the data bus.

There are some alternatives available to the designer to handle this problem. Basically, the capacitive loading of the data bus slows down the response time, even though DC specifications are still met. For systems operating with a relatively slow CPU clock frequency, more time is available in which to establish proper logic levels on the bus and therefore higher capacitive loads can be driven (see Typical Performance Curves).

At higher CPU clock frequencies time can be extended for I/O reads (and/or writes) by inserting wait states (8080) or using clock-extending circuits (6800).

Finally, if time is short and capacitive loading is high, external bus drivers must be used. These can be three-state buffers (low power Schottky is recommended, such as the 74LS240 series) or special higher-drive-current products which are designed as bus drivers. High-current bipolar bus drivers with PNP inputs are recommended.

Power Supplies

Noise spikes on the V+ supply line can cause conversion errors as the comparator will respond to this noise. A low-inductance tantalum filter capacitor should be used close to the converter V+ pin, and values of 1µF or greater are recommended. If an unregulated voltage is available in the system, a separate 5V voltage regulator for the converter and other analog circuitry) will greatly reduce digital noise on the V+ supply. An ICL7663 can be used to regulate such a supply from an input as low as 5.2V.

Wiring and Hook-Up Precautions

Standard digital wire-wrap sockets are not satisfactory for breadboarding with this A/D converter. Sockets on PC boards can be used. All logic signal wires and leads should be grouped and kept as far away as possible from the analog signal leads. Exposed leads to the analog inputs can cause undesired digital noise and hum pickup; therefore, shielded leads may be necessary in many applications.

A single-point analog ground should be used which is separate from the logic ground points. The power supply bypass capacitor and the self-clocking capacitor (if used) should both be returned to digital ground. Any $V_{REF}/2$ bypass capacitors, analog input filter capacitors, or input signal shielding should be returned to the analog ground point. A test for proper grounding is to measure the zero error of the A/D converter. Zero errors in excess of $^1/_4$ LSB can usually be traced to improper board layout and wiring (see Zero Error for measurement). Further information can be found in Application Note AN018.

Testing the A/D Converter

There are many degrees of complexity associated with testing an A/D converter. One of the simplest tests is to apply a known analog input voltage to the converter and use LEDs to display the resulting digital output code as shown in Figure 18.

For ease of testing, the $V_{REF}/2$ (pin 9) should be supplied with 2.560V and a V+ supply voltage of 5.12V should be used. This provides an LSB value of 20mV.

If a full scale adjustment is to be made, an analog input voltage of 5.090V (5.120 - $1^1/_2$ LSB) should be applied to the $V_{IN(+)}$ pin with the $V_{IN(-)}$ pin grounded. The value of the $V_{REF}/2$ input voltage should be adjusted until the digital output code is just changing from 1111 1110 to 1111 1111. This value of $V_{REF}/2$ should then be used for all the tests.

The digital-output LED display can be decoded by dividing the 8 bits into 2 hex characters, one with the 4 most-significant bits (MS) and one with the 4 least-significant bits (LS). The output is then interpreted as a sum of fractions times the full scale voltage:

$$V_{OUT} = \left(\frac{MS}{16} + \frac{LS}{256}\right)(5.12)V\ .$$

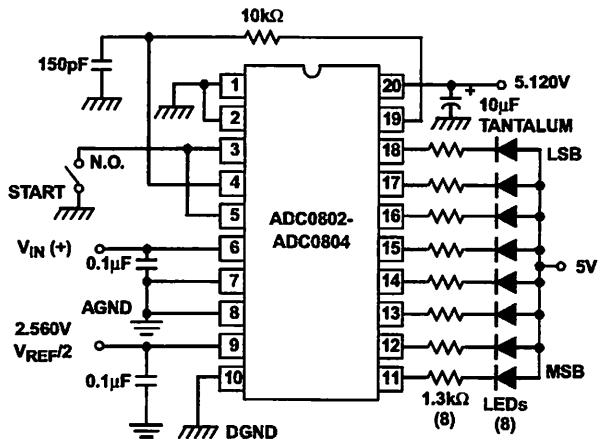
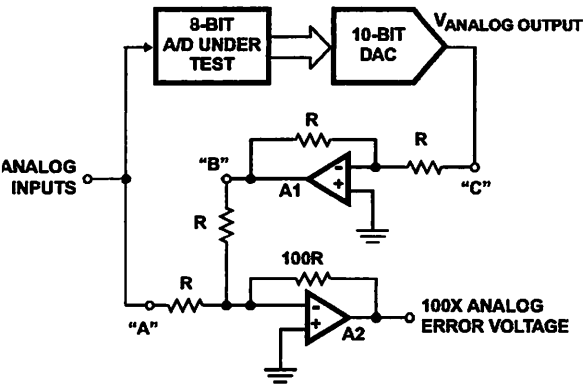


FIGURE 18. BASIC TESTER FOR THE A/D

For example, for an output LED display of 1011 0110, the MS character is hex B (decimal 11) and the LS character is hex (and decimal) 6, so:

$$V_{OUT} = \left(\frac{11}{16} + \frac{6}{256}\right)(5.12) = 3.64V.$$

igures 19 and 20 show more sophisticated test circuits.



IGURE 19. A/D TESTER WITH ANALOG ERROR OUTPUT. THIS CIRCUIT CAN BE USED TO GENERATE "ERROR PLOTS" OF FIGURE 11.

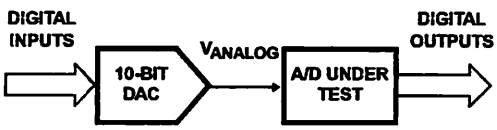


FIGURE 20. BASIC "DIGITAL" A/D TESTER

ypical Applications

terfacing 8080/85 or Z-80 Microprocessors

his converter has been designed to directly interface with 080/85 or Z-80 Microprocessors. The three-state output apability of the A/D eliminates the need for a peripheral terface device, although address decoding is still required generate the appropriate $\overline{CS}$ for the converter. The A/D an be mapped into memory space (using standard mem-y-address decoding for $\overline{CS}$ and the $\overline{MEMR}$ and $\overline{MEMW}$ robes) or it can be controlled as an I/O device by using the $\overline{OR}$ and $\overline{I/OW}$ strobes and decoding the address bits A0 → 7 (or address bits A8 → A15, since they will contain the ime 8-bit address information) to obtain the $\overline{CS}$ input. sing the I/O space provides 256 additional addresses and ay allow a simpler 8-bit address decoder, but the data can ly be input to the accumulator. To make use of the addi-onal memory reference instructions, the A/D should be apped into memory space. See AN020 for more discus-on of memory-mapped vs I/O-mapped interfaces. An ample of an A/D in I/O space is shown in Figure 21.

e standard control-bus signals of the 8080 ($\overline{CS}$, $\overline{RD}$ and $\overline{R}$) can be directly wired to the digital control inputs of the D, since the bus timing requirements, to allow both starting e converter, and outputting the data onto the data bus, are et. A bus driver should be used for larger microprocessor stems where the data bus leaves the PC board and/or ust drive capacitive loads larger than 100pF.

is useful to note that in systems where the A/D converter is of 8 or fewer I/O-mapped devices, no address-decoding rcuitry is necessary. Each of the 8 address bits (A0 to A7) n be directly used as $\overline{CS}$ inputs, one for each I/O device.

Interfacing the Z-80 and 8085

The Z-80 and 8085 control buses are slightly different from that of the 8080. General $\overline{RD}$ and $\overline{WR}$ strobes are provided and separate memory request, $\overline{MREQ}$, and I/O request, $\overline{IORQ}$, signals have to be combined with the generalized strobes to provide the appropriate signals. An advantage of operating the A/D in I/O space with the Z-80 is that the CPU will automatically insert one wait state (the $\overline{RD}$ and $\overline{WR}$ strobes are extended one clock period) to allow more time for the I/O devices to respond. Logic to map the A/D in I/O space is shown in Figure 22. By using $\overline{MREQ}$ in place of $\overline{IORQ}$, a memory-mapped configuration results.

Additional I/O advantages exist as software DMA routines are available and use can be made of the output data transfer which exists on the upper 8 address lines (A8 to A15) during I/O input instructions. For example, MUX channel selection for the A/D can be accomplished with this operating mode.

The 8085 also provides a generalized $\overline{RD}$ and $\overline{WR}$ strobe, with an IO/$\overline{M}$ line to distinguish I/O and memory requests. The circuit of Figure 22 can again be used, with IO/$\overline{M}$ in place of $\overline{IORQ}$ for a memory-mapped interface, and an extra inverter (or the logic equivalent) to provide $\overline{IO}$/M for an I/O-mapped connection.

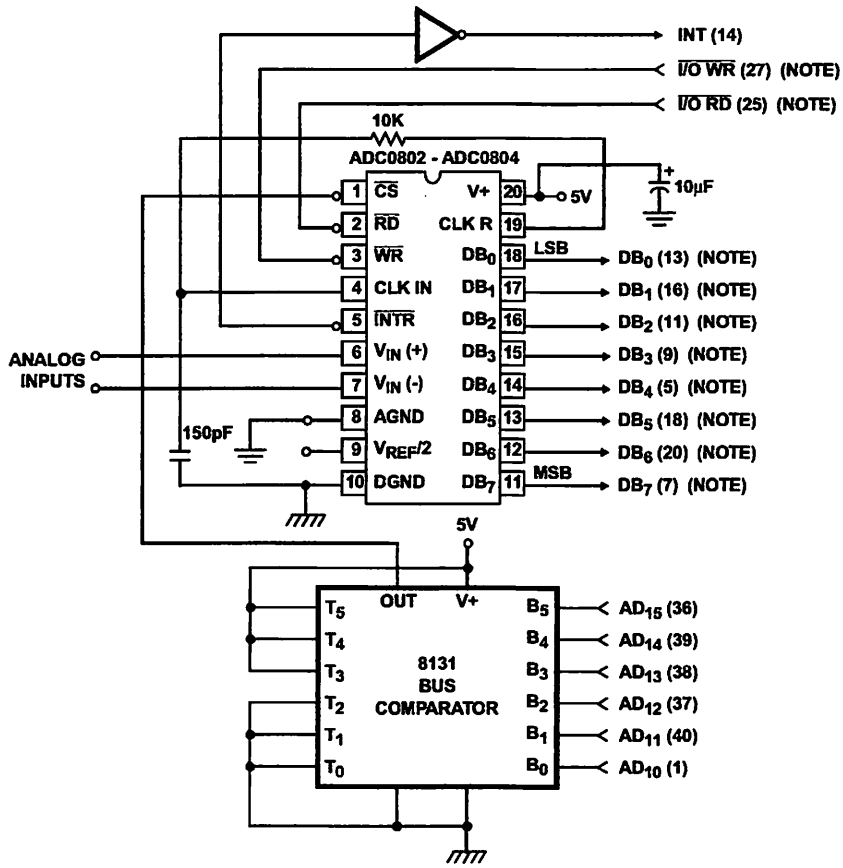
Interfacing 6800 Microprocessor Derivatives (6502, etc.)

The control bus for the 6800 microprocessor derivatives does not use the RD and WR strobe signals. Instead it employs a single R/W line and additional timing, if needed, can be derived from the $\phi 2$ clock. All I/O devices are memory-mapped in the 6800 system, and a special signal, VMA, indicates that the current address is valid. Figure 23 shows an interface schematic where the A/D is memory-mapped in the 6800 system. For simplicity, the CS decoding is shown using $^1/_2$ DM8092. Note that in many 6800 systems, an already decoded $\overline{4/5}$ line is brought out to the common bus at pin 21. This can be tied directly to the CS pin of the A/D, provided that no other devices are addressed at HEX ADDR: 4XXX or 5XXX.

In Figure 24 the ADC0802 series is interfaced to the MC6800 microprocessor through (the arbitrarily chosen) Port B of the MC6820 or MC6821 Peripheral Interface Adapter (PIA). Here the CS pin of the A/D is grounded since the PIA is already memory-mapped in the MC6800 system and no CS decoding is necessary. Also notice that the A/D output data lines are connected to the microprocessor bus under program control through the PIA and therefore the A/D RD pin can be grounded.

Application Notes

NOTE #	DESCRIPTION	AnswerFAX DOC. #
AN016	"Selecting A/D Converters"	9016
AN018	"Do's and Don'ts of Applying A/D Converters"	9018
AN020	"A Cookbook Approach to High Speed Data Acquisition and Microprocessor Interfacing"	9020
AN030	"The ICL7104 - A Binary Output A/D Converter for Microprocessors"	9030



)TE: Pin numbers for 8228 System Controller: Others are 8080A.

FIGURE 21. ADC0802 TO 8080A CPU INTERFACE

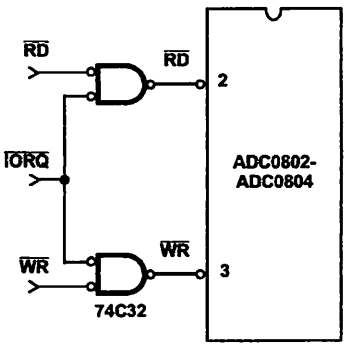
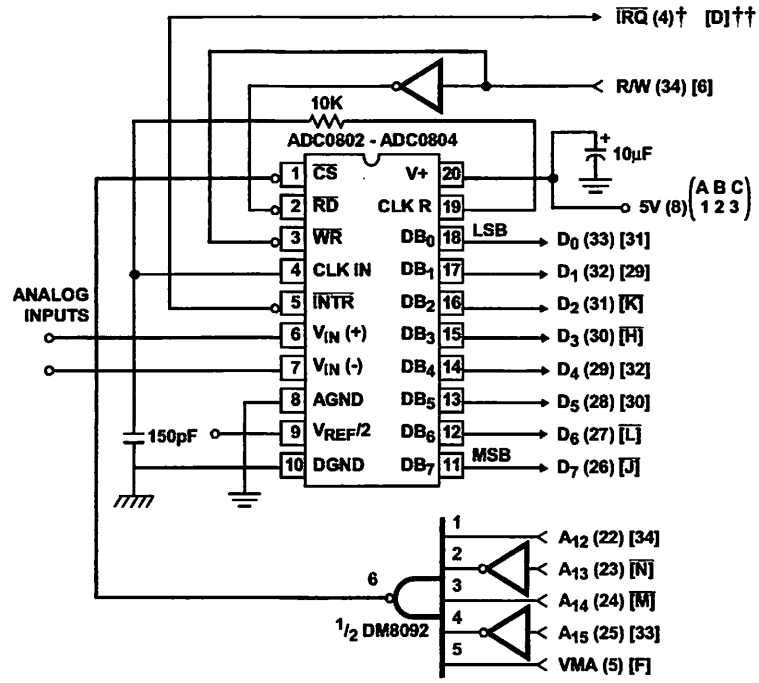


FIGURE 22. MAPPING THE A/D AS AN I/O DEVICE FOR USE WITH THE Z-80 CPU



† Numbers in parentheses refer to MC6800 CPU Pinout.
†† Numbers or letters in brackets refer to standard MC6800 System Common Bus Code.

FIGURE 23. ADC0802 TO MC6800 CPU INTERFACE

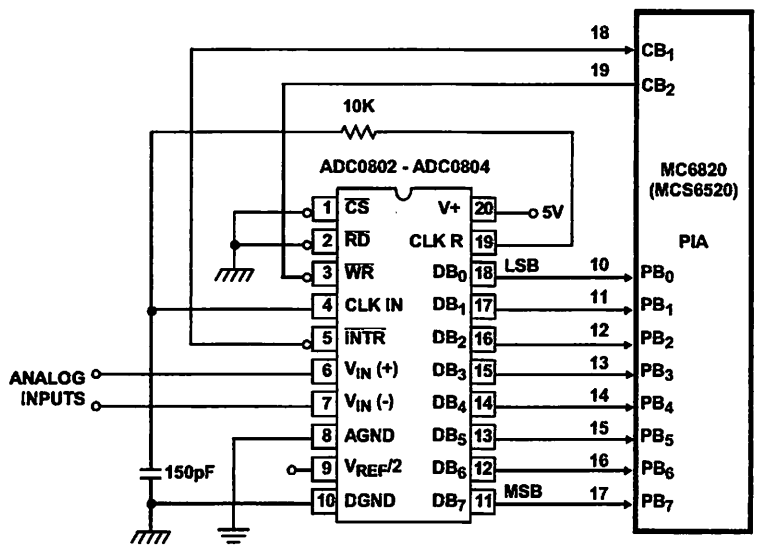


FIGURE 24. ADC0802 TO MC6820 PIA INTERFACE

Die Characteristics

DIE DIMENSIONS:

(101 mils x 93 mils) x 525µm x 25µm

METALLIZATION:

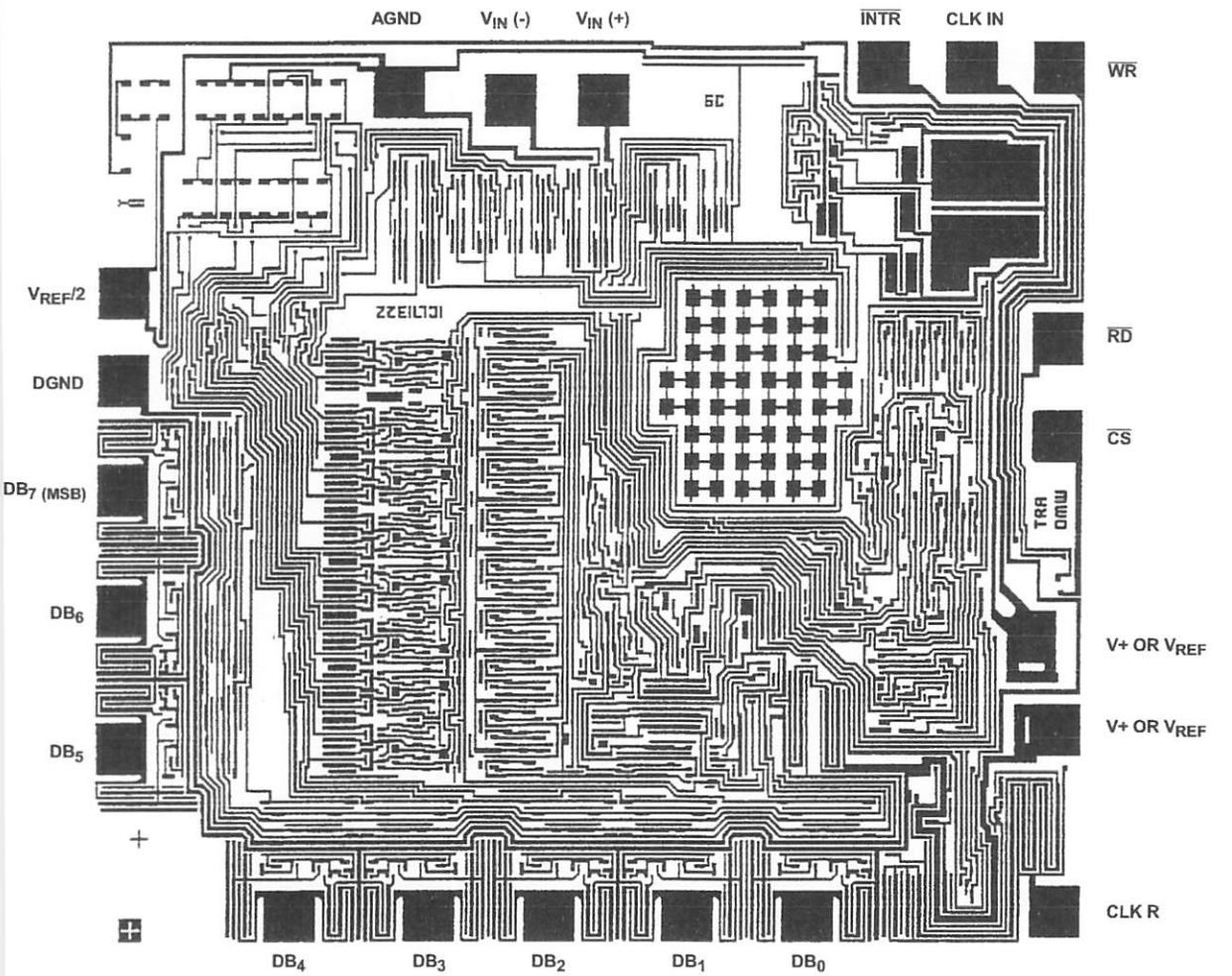
Type: Al
Thickness: 10kÅ ±1kÅ

PASSIVATION:

Type: Nitride over Silox
Nitride Thickness: 8kÅ
Silox Thickness: 7kÅ

Metallization Mask Layout

ADC0802, ADC0803, ADC0804



)-0122; Rev 8; 10/03

MAXIM

Low-Power, Slew-Rate-Limited RS-485/RS-422 Transceivers

General Description

e MAX481, MAX483, MAX485, MAX487–MAX491, and
AX1487 are low-power transceivers for RS-485 and RS-
2 communication. Each part contains one driver and one
ceiver. The MAX483, MAX487, MAX488, and MAX489
ature reduced slew-rate drivers that minimize EMI and
duce reflections caused by improperly terminated cables,
is allowing error-free data transmission up to 250kbps.
e driver slew rates of the MAX481, MAX485, MAX490,
AX491, and MAX1487 are not limited, allowing them to
nsmit up to 2.5Mbps.

ese transceivers draw between 120µA and 500µA of
pply current when unloaded or fully loaded with disabled
vers. Additionally, the MAX481, MAX483, and MAX487
ve a low-current shutdown mode in which they consume
y 0.1µA. All parts operate from a single 5V supply.

vers are short-circuit current limited and are protected
ainst excessive power dissipation by thermal shutdown
cuitry that places the driver outputs into a high-imped-
ce state. The receiver input has a fail-safe feature that
arantees a logic-high output if the input is open circuit.

e MAX487 and MAX1487 feature quarter-unit-load
eiver input impedance, allowing up to 128 MAX487/
AX1487 transceivers on the bus. Full-duplex communi-
ions are obtained using the MAX488–MAX491, while
MAX481, MAX483, MAX485, MAX487, and MAX1487
designed for half-duplex applications.

Applications

Low-Power RS-485 Transceivers

Low-Power RS-422 Transceivers

Level Translators

Transceivers for EMI-Sensitive Applications

Industrial-Control Local Area Networks

Next Generation Device Features

- **For Fault-Tolerant Applications**
  MAX3430: ±80V Fault-Protected, Fail-Safe, 1/4 Unit Load, +3.3V, RS-485 Transceiver
  MAX3440E–MAX3444E: ±15kV ESD-Protected, ±60V Fault-Protected, 10Mbps, Fail-Safe, RS-485/J1708 Transceivers
- **For Space-Constrained Applications**
  MAX3460–MAX3464: +5V, Fail-Safe, 20Mbps, Profibus RS-485/RS-422 Transceivers
  MAX3362: +3.3V, High-Speed, RS-485/RS-422 Transceiver in a SOT23 Package
  MAX3280E–MAX3284E: ±15kV ESD-Protected, 52Mbps, +3V to +5.5V, SOT23, RS-485/RS-422, True Fail-Safe Receivers
  MAX3293/MAX3294/MAX3295: 20Mbps, +3.3V, SOT23, RS-855/RS-422 Transmitters
- **For Multiple Transceiver Applications**
  MAX3030E–MAX3033E: ±15kV ESD-Protected, +3.3V, Quad RS-422 Transmitters
- **For Fail-Safe Applications**
  MAX3080–MAX3089: Fail-Safe, High-Speed (10Mbps), Slew-Rate-Limited RS-485/RS-422 Transceivers
- **For Low-Voltage Applications**
  MAX3483E/MAX3485E/MAX3486E/MAX3488E/MAX3490E/MAX3491E: +3.3V Powered, ±15kV ESD-Protected, 12Mbps, Slew-Rate-Limited, True RS-485/RS-422 Transceivers

Ordering Information appears at end of data sheet.

Selection Table

PART NUMBER	HALF/FULL DUPLEX	DATA RATE (Mbps)	SLEW-RATE LIMITED	LOW-POWER SHUTDOWN	RECEIVER/ DRIVER ENABLE	QUIESCENT CURRENT (µA)	NUMBER OF TRANSMITTERS ON BUS	PIN COUNT
MAX481	Half	2.5	No	Yes	Yes	300	32	8
MAX483	Half	0.25	Yes	Yes	Yes	120	32	8
MAX485	Half	2.5	No	No	Yes	300	32	8
MAX487	Half	0.25	Yes	Yes	Yes	120	128	8
MAX488	Full	0.25	Yes	No	No	120	32	8
MAX489	Full	0.25	Yes	No	Yes	120	32	14
MAX490	Full	2.5	No	No	No	300	32	8
MAX491	Full	2.5	No	No	Yes	300	32	14
MAX1487	Half	2.5	No	No	Yes	230	128	8

ow-Power, Slew-Rate-Limited
S-485/RS-422 Transceivers

SOLUTE MAXIMUM RATINGS

ply Voltage (V_{CC}) 12V
trol Input Voltage ($\overline{RE}$, DE) ..... -0.5V to (V_{CC} + 0.5V)
er Input Voltage (DI) ..... -0.5V to (V_{CC} + 0.5V)
er Output Voltage (A, B) ..... -8V to +12.5V
eiver Input Voltage (A, B) ..... -8V to +12.5V
eiver Output Voltage (RO) ..... -0.5V to (V_{CC} +0.5V)
tinuous Power Dissipation (T_A = +70°C)
Pin Plastic DIP (derate 9.09mW/°C above +70°C) 727mW
-Pin Plastic DIP (derate 10.00mW/°C above +70°C) ..800mW
Pin SO (derate 5.88mW/°C above +70°C) 471mW
14-Pin SO (derate 8.33mW/°C above +70°C) 667mW
8-Pin µMAX (derate 4.1mW/°C above +70°C) 830mW
8-Pin CERDIP (derate 8.00mW/°C above +70°C) 640mW
14-Pin CERDIP (derate 9.09mW/°C above +70°C) 727mW
Operating Temperature Ranges
MAX4_ _C_ _/MAX1487C_ A ..... 0°C to +70°C
MAX4_ _E_ _/MAX1487E_ A ..... -40°C to +85°C
MAX4_ _MJ_/MAX1487MJA ..... -55°C to +125°C
Storage Temperature Range ..... -65°C to +160°C
Lead Temperature (soldering, 10sec) ..... +300°C

sses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional ration of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to olute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

C = 5V ±5%, T_A = T_{MIN} to T_{MAX}, unless otherwise noted.) (Notes 1, 2)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
ferential Driver Output (no load)	V_{OD1}					5	V
ferential Driver Output th load)	V_{OD2}	R = 50Ω (RS-422)		2			V
		R = 27Ω (RS-485), Figure 4		1.5		5	
ange in Magnitude of Driver ferential Output Voltage for mplementary Output States	ΔV_{OD}	R = 27Ω or 50Ω, Figure 4				0.2	V
iver Common-Mode Output ltage	V_{OC}	R = 27Ω or 50Ω, Figure 4				3	V
ange in Magnitude of Driver mmon-Mode Output Voltage Complementary Output States	ΔV_{OD}	R = 27Ω or 50Ω, Figure 4				0.2	V
ut High Voltage	V_{IH}	DE, DI, $\overline{RE}$		2.0			V
ut Low Voltage	V_{IL}	DE, DI, $\overline{RE}$				0.8	V
ut Current	I_{IN1}	DE, DI, $\overline{RE}$				±2	µA
ut Current B)	I_{IN2}	DE = 0V; V_{CC} = 0V or 5.25V, all devices except MAX487/MAX1487	V_{IN} = 12V			1.0	mA
			V_{IN} = -7V			-0.8	
		MAX487/MAX1487, DE = 0V, V_{CC} = 0V or 5.25V	V_{IN} = 12V			0.25	mA
			V_{IN} = -7V			-0.2	
ceiver Differential Threshold ltage	V_{TH}	-7V ≤ V_{CM} ≤ 12V		-0.2		0.2	V
ceiver Input Hysteresis	ΔV_{TH}	V_{CM} = 0V			70		mV
ceiver Output High Voltage	V_{OH}	I_O = -4mA, V_{ID} = 200mV		3.5			V
ceiver Output Low Voltage	V_{OL}	I_O = 4mA, V_{ID} = -200mV				0.4	V
ee-State (high impedance) tput Current at Receiver	I_{OZR}	0.4V ≤ V_O ≤ 2.4V				±1	µA
ceiver Input Resistance	R_{IN}	-7V ≤ V_{CM} ≤ 12V, all devices except MAX487/MAX1487		12			kΩ
		-7V ≤ V_{CM} ≤ 12V, MAX487/MAX1487		48			kΩ

; ELECTRICAL CHARACTERISTICS (continued)

; = 5V ±5%, T_A = T_{MIN} to T_{MAX}, unless otherwise noted.) (Notes 1, 2)

PARAMETER	SYMBOL	CONDITIONS			MIN	TYP	MAX	UNITS
-Load Supply Current ote 3)	I_{CC}	MAX488/MAX489, DE, DI, $\overline{RE}$ = 0V or V_{CC}				120	250	µA
		MAX490/MAX491, DE, DI, $\overline{RE}$ = 0V or V_{CC}				300	500	
		MAX481/MAX485, $\overline{RE}$ = 0V or V_{CC}	DE = V_{CC}			500	900	
			DE = 0V			300	500	
		MAX1487, $\overline{RE}$ = 0V or V_{CC}	DE = V_{CC}			300	500	
			DE = 0V			230	400	
		MAX483/MAX487, $\overline{RE}$ = 0V or V_{CC}	DE = 5V	MAX483		350	650	
				MAX487		250	400	
			DE = 0V			120	250	
pply Current in Shutdown	I_{SHDN}	MAX481/483/487, DE = 0V, $\overline{RE}$ = V_{CC}				0.1	10	µA
ver Short-Circuit Current, = High	I_{OSD1}	-7V ≤ V_O ≤12V (Note 4)			35		250	mA
ver Short-Circuit Current, = Low	I_{OSD2}	-7V ≤ V_O ≤12V (Note 4)			35		250	mA
ceiver Short-Circuit Current	I_{OSR}	0V ≤ V_O ≤ V_{CC}			7		95	mA

/ITCHING CHARACTERISTICS—MAX481/MAX485, MAX490/MAX491, MAX1487

; = 5V ±5%, T_A = T_{MIN} to T_{MAX}, unless otherwise noted.) (Notes 1, 2)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
ver Input to Output	t_{PLH}	Figures 6 and 8, R_{DIFF} = 54Ω, C_{L1} = C_{L2} = 100pF		10	30	60	ns
	t_{PHL}			10	30	60	
ver Output Skew to Output	t_{SKEW}	Figures 6 and 8, R_{DIFF} = 54Ω, C_{L1} = C_{L2} = 100pF			5	10	ns
ver Rise or Fall Time	t_R, t_F	Figures 6 and 8, R_{DIFF} = 54Ω, C_{L1} = C_{L2} = 100pF	MAX481, MAX485, MAX1487	3	15	40	ns
			MAX490C/E, MAX491C/E	5	15	25	
			MAX490M, MAX491M	3	15	40	
ver Enable to Output High	t_{ZH}	Figures 7 and 9, C_L = 100pF, S2 closed			40	70	ns
ver Enable to Output Low	t_{ZL}	Figures 7 and 9, C_L = 100pF, S1 closed			40	70	ns
ver Disable Time from Low	t_{LZ}	Figures 7 and 9, C_L = 15pF, S1 closed			40	70	ns
ver Disable Time from High	t_{HZ}	Figures 7 and 9, C_L = 15pF, S2 closed			40	70	ns
ceiver Input to Output	t_{PLH}, t_{PHL}	Figures 6 and 10, R_{DIFF} = 54Ω, C_{L1} = C_{L2} = 100pF	MAX481, MAX485, MAX1487	20	90	200	ns
			MAX490C/E, MAX491C/E	20	90	150	
			MAX490M, MAX491M	20	90	200	
LH - t_{PHL} | Differential ceiver Skew	t_{SKD}	Figures 6 and 10, R_{DIFF} = 54Ω, C_{L1} = C_{L2} = 100pF			13		ns
ceiver Enable to Output Low	t_{ZL}	Figures 5 and 11, C_{RL} = 15pF, S1 closed			20	50	ns
ceiver Enable to Output High	t_{ZH}	Figures 5 and 11, C_{RL} = 15pF, S2 closed			20	50	ns
ceiver Disable Time from Low	t_{LZ}	Figures 5 and 11, C_{RL} = 15pF, S1 closed			20	50	ns
ceiver Disable Time from High	t_{HZ}	Figures 5 and 11, C_{RL} = 15pF, S2 closed			20	50	ns
ximum Data Rate	f_{MAX}			2.5			Mbps
ie to Shutdown	t_{SHDN}	MAX481 (Note 5)		50	200	600	ns

WITCHING CHARACTERISTICS—MAX481/MAX485, MAX490/MAX491, MAX1487 (continued)

CC = 5V ±5%, T_A = T_{MIN} to T_{MAX}, unless otherwise noted.) (Notes 1, 2)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
river Enable from Shutdown to utput High (MAX481)	$t_{ZH(SHDN)}$	Figures 7 and 9, C_L = 100pF, S2 closed		40	100	ns
river Enable from Shutdown to utput Low (MAX481)	$t_{ZL(SHDN)}$	Figures 7 and 9, C_L = 100pF, S1 closed		40	100	ns
eceiver Enable from Shutdown Output High (MAX481)	$t_{ZH(SHDN)}$	Figures 5 and 11, C_L = 15pF, S2 closed, A - B = 2V		300	1000	ns
eceiver Enable from Shutdown Output Low (MAX481)	$t_{ZL(SHDN)}$	Figures 5 and 11, C_L = 15pF, S1 closed, B - A = 2V		300	1000	ns

NITCHING CHARACTERISTICS—MAX483, MAX487/MAX488/MAX489

C = 5V ±5%, T_A = T_{MIN} to T_{MAX}, unless otherwise noted.) (Notes 1, 2)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
river Input to Output	t_{PLH}	Figures 6 and 8, R_{DIFF} = 54Ω, C_{L1} = C_{L2} = 100pF	250	800	2000	ns
	t_{PHL}		250	800	2000	
river Output Skew to Output	t_{SKEW}	Figures 6 and 8, R_{DIFF} = 54Ω, C_{L1} = C_{L2} = 100pF		100	800	ns
river Rise or Fall Time	t_R, t_F	Figures 6 and 8, R_{DIFF} = 54Ω, C_{L1} = C_{L2} = 100pF	250		2000	ns
river Enable to Output High	t_{ZH}	Figures 7 and 9, C_L = 100pF, S2 closed	250		2000	ns
river Enable to Output Low	t_{ZL}	Figures 7 and 9, C_L = 100pF, S1 closed	250		2000	ns
river Disable Time from Low	t_{LZ}	Figures 7 and 9, C_L = 15pF, S1 closed	300		3000	ns
river Disable Time from High	t_{HZ}	Figures 7 and 9, C_L = 15pF, S2 closed	300		3000	ns
eceiver Input to Output	t_{PLH}	Figures 6 and 10, R_{DIFF} = 54Ω, C_{L1} = C_{L2} = 100pF	250		2000	ns
	t_{PHL}		250		2000	
t_{PLH} - t_{PHL} | Differential eceiver Skew	t_{SKD}	Figures 6 and 10, R_{DIFF} = 54Ω, C_{L1} = C_{L2} = 100pF		100		ns
eceiver Enable to Output Low	t_{ZL}	Figures 5 and 11, C_{RL} = 15pF, S1 closed		20	50	ns
eceiver Enable to Output High	t_{ZH}	Figures 5 and 11, C_{RL} = 15pF, S2 closed		20	50	ns
eceiver Disable Time from Low	t_{LZ}	Figures 5 and 11, C_{RL} = 15pF, S1 closed		20	50	ns
eceiver Disable Time from High	t_{HZ}	Figures 5 and 11, C_{RL} = 15pF, S2 closed		20	50	ns
aximum Data Rate	f_{MAX}	t_{PLH}, t_{PHL} < 50% of data period	250			kbps
ne to Shutdown	t_{SHDN}	MAX483/MAX487 (Note 5)	50	200	600	ns
iver Enable from Shutdown to utput High	$t_{ZH(SHDN)}$	MAX483/MAX487, Figures 7 and 9, C_L = 100pF, S2 closed			2000	ns
iver Enable from Shutdown to utput Low	$t_{ZL(SHDN)}$	MAX483/MAX487, Figures 7 and 9, C_L = 100pF, S1 closed			2000	ns
eceiver Enable from Shutdown Output High	$t_{ZH(SHDN)}$	MAX483/MAX487, Figures 5 and 11, C_L = 15pF, S2 closed			2500	ns
eceiver Enable from Shutdown Output Low	$t_{ZL(SHDN)}$	MAX483/MAX487, Figures 5 and 11, C_L = 15pF, S1 closed			2500	ns

)TES FOR ELECTRICAL/SWITCHING CHARACTERISTICS

e 1: All currents into device pins are positive; all currents out of device pins are negative. All voltages are referenced to device ground unless otherwise specified.

e 2: All typical specifications are given for V_{CC} = 5V and T_A = +25°C.

e 3: Supply current specification is valid for loaded transmitters when DE = 0V.

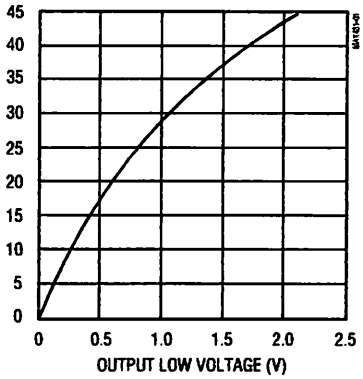
e 4: Applies to peak current. See *Typical Operating Characteristics.*

e 5: The MAX481/MAX483/MAX487 are put into shutdown by bringing $\overline{RE}$ high and DE low. If the inputs are in this state for less than 50ns, the parts are guaranteed not to enter shutdown. If the inputs are in this state for at least 600ns, the parts are guaranteed to have entered shutdown. See *Low-Power Shutdown Mode* section.

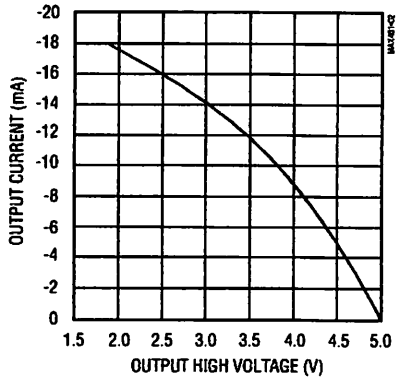
Typical Operating Characteristics

(: = 5V, T_A = +25°C, unless otherwise noted.)

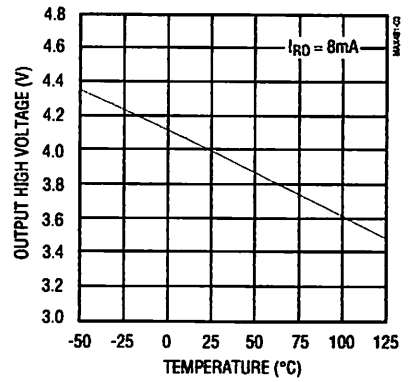
OUTPUT CURRENT vs. RECEIVER OUTPUT LOW VOLTAGE



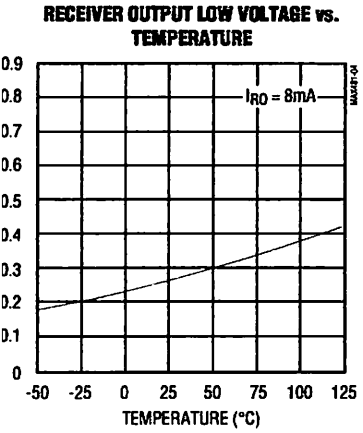
OUTPUT CURRENT vs. RECEIVER OUTPUT HIGH VOLTAGE



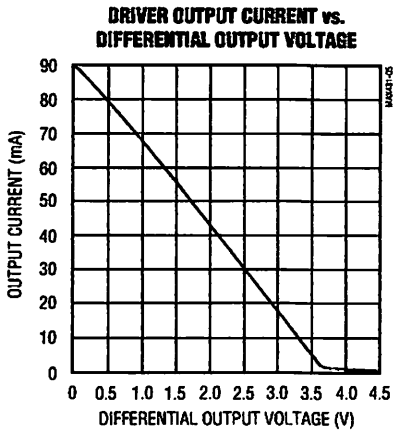
RECEIVER OUTPUT HIGH VOLTAGE vs. TEMPERATURE



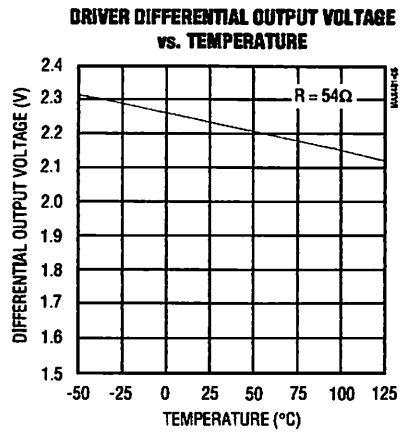
RECEIVER OUTPUT LOW VOLTAGE vs. TEMPERATURE



DRIVER OUTPUT CURRENT vs. DIFFERENTIAL OUTPUT VOLTAGE



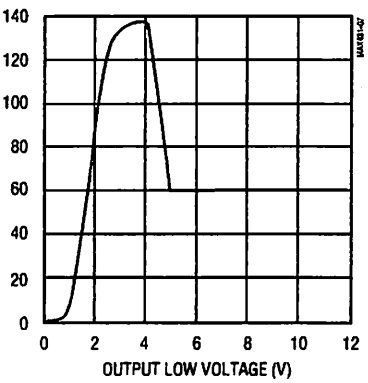
DRIVER DIFFERENTIAL OUTPUT VOLTAGE vs. TEMPERATURE



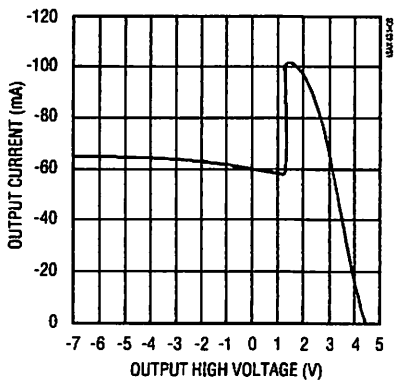
Typical Operating Characteristics (continued)

(= 5V, T_A = +25°C, unless otherwise noted.)

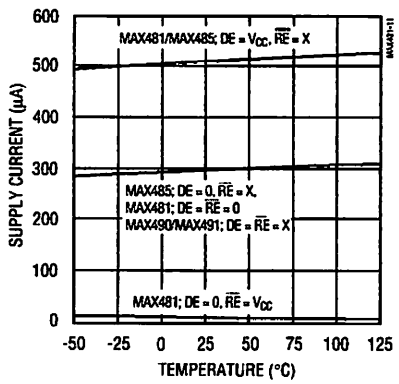
OUTPUT CURRENT vs. DRIVER OUTPUT LOW VOLTAGE



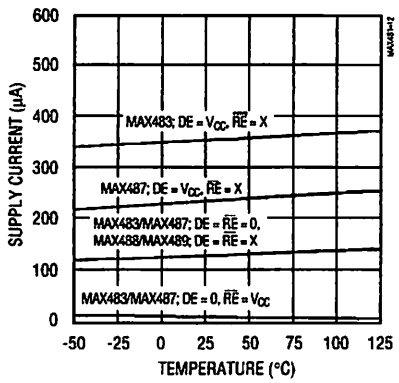
OUTPUT CURRENT vs. DRIVER OUTPUT HIGH VOLTAGE



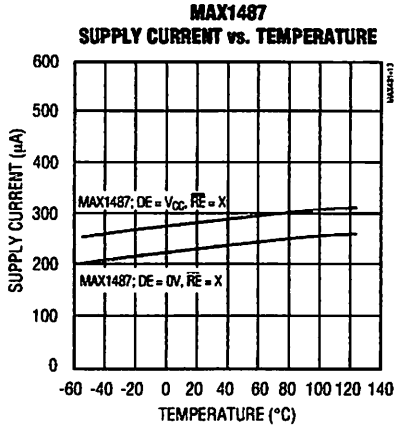
MAX481/MAX485/MAX490/MAX491 SUPPLY CURRENT vs. TEMPERATURE



MAX483/MAX487–MAX489 SUPPLY CURRENT vs. TEMPERATURE



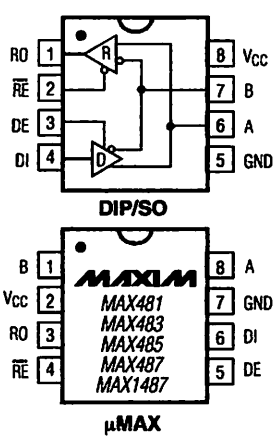
MAX1487 SUPPLY CURRENT vs. TEMPERATURE

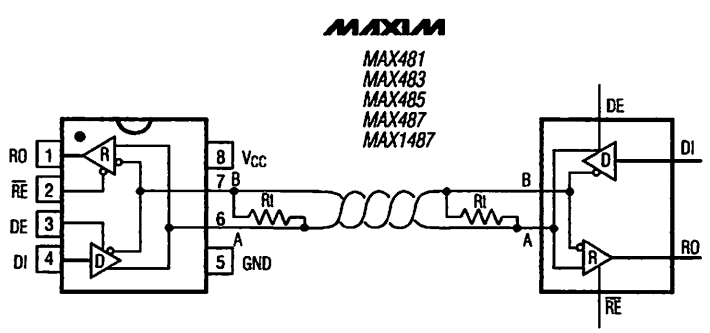


Pin Description

PIN					NAME	FUNCTION
AX481/MAX483/ AX485/MAX487/ MAX1487		MAX488/ MAX490		MAX489/ MAX491		
P/SO	µMAX	DIP/SO	µMAX	DIP/SO		
1	3	2	4	2	RO	Receiver Output: If A > B by 200mV, RO will be high; If A < B by 200mV, RO will be low.
2	4	—	—	3	$\overline{RE}$	Receiver Output Enable. RO is enabled when $\overline{RE}$ is low; RO is high impedance when $\overline{RE}$ is high.
3	5	—	—	4	DE	Driver Output Enable. The driver outputs, Y and Z, are enabled by bringing DE high. They are high impedance when DE is low. If the driver outputs are enabled, the parts function as line drivers. While they are high impedance, they function as line receivers if $\overline{RE}$ is low.
4	6	3	5	5	DI	Driver Input. A low on DI forces output Y low and output Z high. Similarly, a high on DI forces output Y high and output Z low.
5	7	4	6	6, 7	GND	Ground
—	—	5	7	9	Y	Noninverting Driver Output
—	—	6	8	10	Z	Inverting Driver Output
6	8	—	—	—	A	Noninverting Receiver Input and Noninverting Driver Output
—	—	8	2	12	A	Noninverting Receiver Input
7	1	—	—	—	B	Inverting Receiver Input and Inverting Driver Output
—	—	7	1	11	B	Inverting Receiver Input
8	2	1	3	14	VCC	Positive Supply: 4.75V ≤ VCC ≤ 5.25V
—	—	—	—	1, 8, 13	N.C.	No Connect—not internally connected

)P VIEW

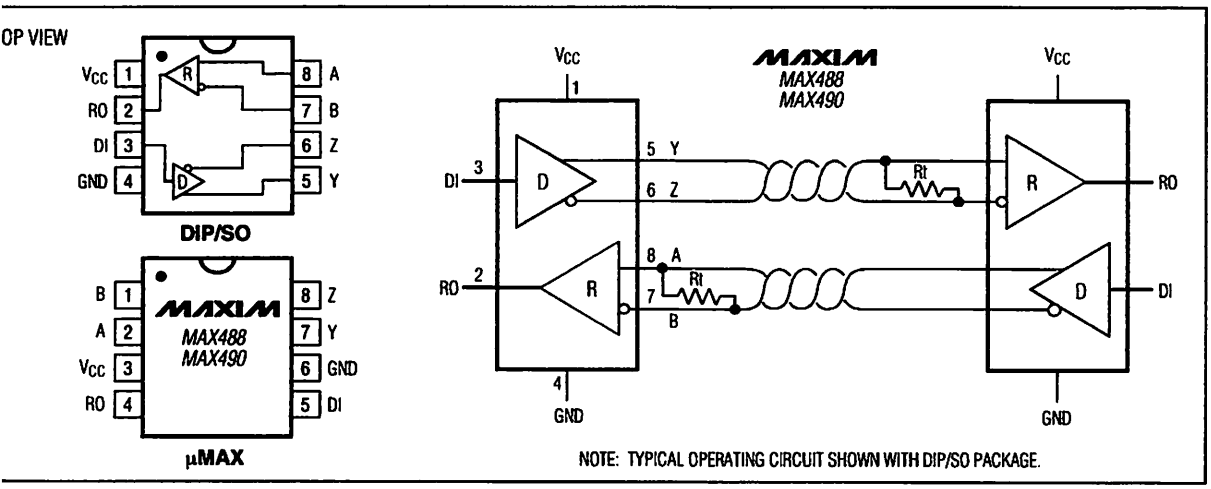




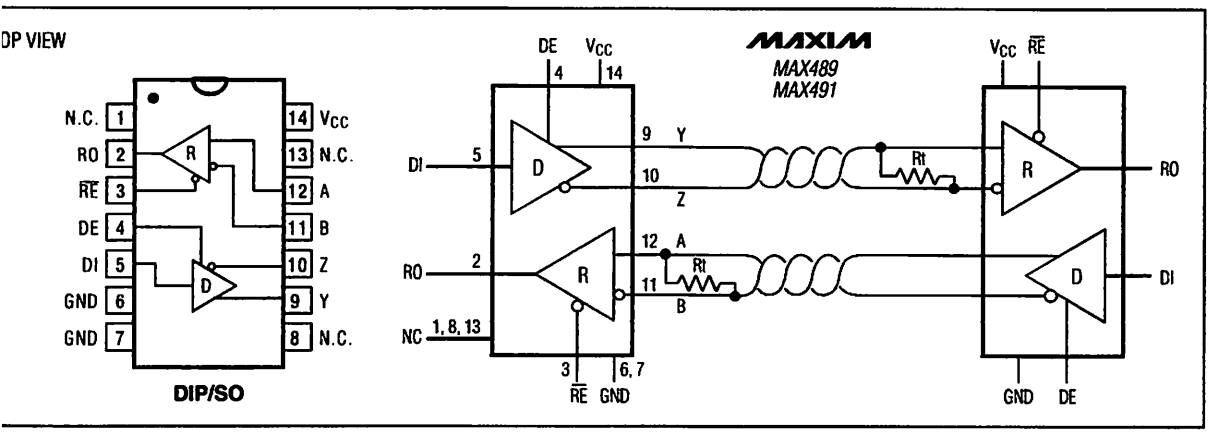
NOTE: PIN LABELS Y AND Z ON TIMING, TEST, AND WAVEFORM DIAGRAMS REFER TO PINS A AND B WHEN DE IS HIGH. TYPICAL OPERATING CIRCUIT SHOWN WITH DIP/SO PACKAGE.

ire 1. MAX481/MAX483/MAX485/MAX487/MAX1487 Pin Configuration and Typical Operating Circuit

ow-Power, Slew-Rate-Limited
S-485/RS-422 Transceivers



re 2. MAX488/MAX490 Pin Configuration and Typical Operating Circuit



re 3. MAX489/MAX491 Pin Configuration and Typical Operating Circuit

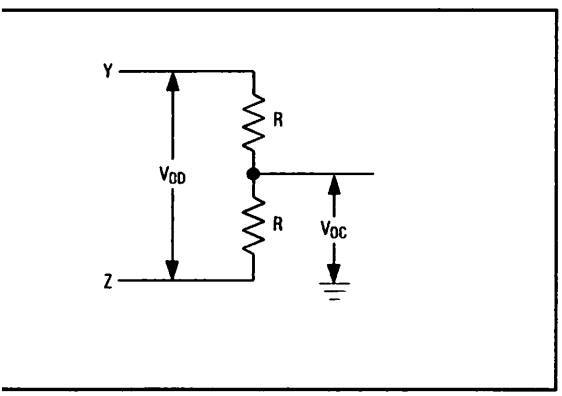
Applications Information

MAX481/MAX483/MAX485/MAX487–MAX491 and
:1487 are low-power transceivers for RS-485 and RS-
communications. The MAX481, MAX485, MAX490,
:491, and MAX1487 can transmit and receive at data
s up to 2.5Mbps, while the MAX483, MAX487,
:488, and MAX489 are specified for data rates up to
‹bps. The MAX488–MAX491 are full-duplex trans-
ers while the MAX481, MAX483, MAX485, MAX487,
MAX1487 are half-duplex. In addition, Driver Enable
and Receiver Enable ($\overline{RE}$) pins are included on the
‹481, MAX483, MAX485, MAX487, MAX489,
:491, and MAX1487. When disabled, the driver and
iver outputs are high impedance.

MAX487/MAX1487: 128 Transceivers on the Bus

The 48kΩ, 1/4-unit-load receiver input impedance of the MAX487 and MAX1487 allows up to 128 transceivers on a bus, compared to the 1-unit load (12kΩ input impedance) of standard RS-485 drivers (32 transceivers maximum). Any combination of MAX487/MAX1487 and other RS-485 transceivers with a total of 32 unit loads or less can be put on the bus. The MAX481/MAX483/MAX485 and MAX488–MAX491 have standard 12kΩ Receiver Input impedance.

Test Circuits



re 4. Driver DC Test Load

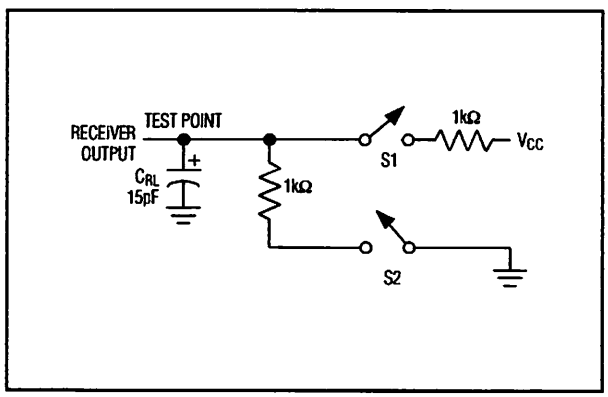
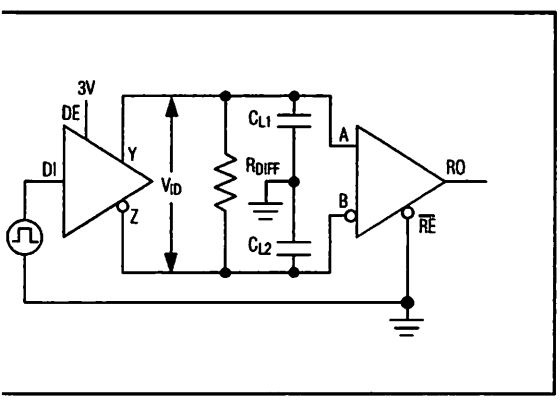


Figure 5. Receiver Timing Test Load



re 6. Driver/Receiver Timing Test Circuit

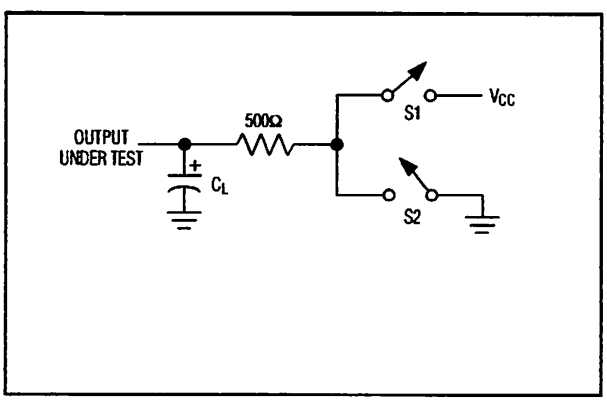


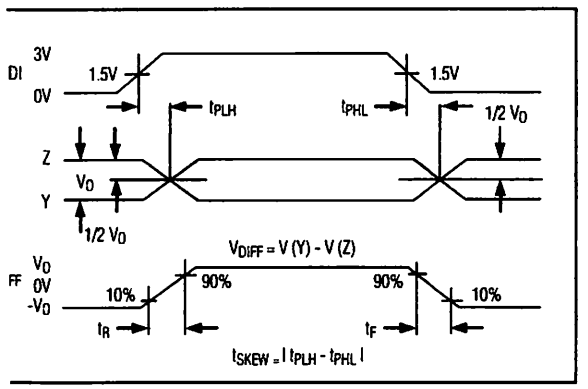
Figure 7. Driver Timing Test Load

MAX483/MAX487/MAX488/MAX489: Reduced EMI and Reflections

MAX483 and MAX487–MAX489 are slew-rate limit- minimizing EMI and reducing reflections caused by roperly terminated cables. Figure 12 shows the dri- output waveform and its Fourier analysis of a kHz signal transmitted by a MAX481, MAX485, (490, MAX491, or MAX1487. High-frequency harmonics with large amplitudes are evident. Figure 13 shows the same information displayed for a MAX483, MAX487, MAX488, or MAX489 transmitting under the same conditions. Figure 13's high-frequency harmonics have much lower amplitudes, and the potential for EMI is significantly reduced.

.ow-Power, Slew-Rate-Limited
?S-485/RS-422 Transceivers

Switching Waveforms



'ure 8. Driver Propagation Delays

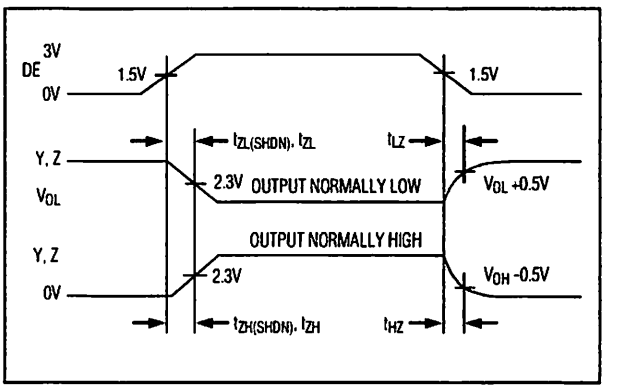
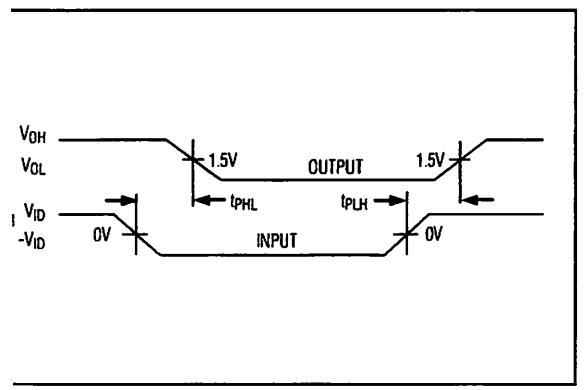


Figure 9. Driver Enable and Disable Times (except MAX488 and MAX490)



'ure 10. Receiver Propagation Delays

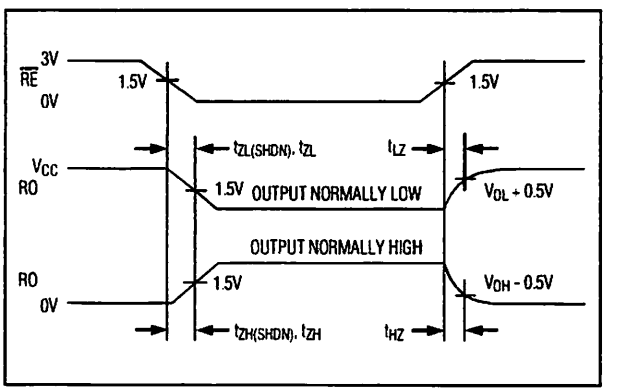


Figure 11. Receiver Enable and Disable Times (except MAX488 and MAX490)

Function Tables (MAX481/MAX483/MAX485/MAX487/MAX1487)

ble 1. Transmitting

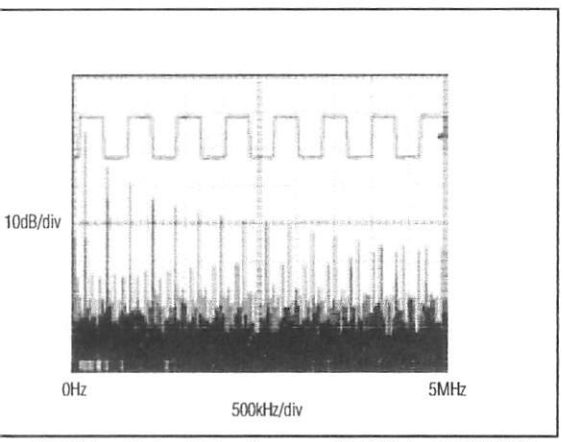
INPUTS			OUTPUTS	
$\overline{RE}$	DE	DI	Z	Y
X	1	1	0	1
X	1	0	1	0
0	0	X	High-Z	High-Z
1	0	X	High-Z*	High-Z*

Don't care
h-Z = High impedance
Shutdown mode for MAX481/MAX483/MAX487

Table 2. Receiving

INPUTS			OUTPUT
$\overline{RE}$	DE	A-B	RO
0	0	≥ +0.2V	1
0	0	≤ -0.2V	0
0	0	Inputs open	1
1	0	X	High-Z*

X = Don't care
High-Z = High impedance
* Shutdown mode for MAX481/MAX483/MAX487



ıre 12. Driver Output Waveform and FFT Plot of MAX481/ X485/MAX490/MAX491/MAX1487 Transmitting a 150kHz nal

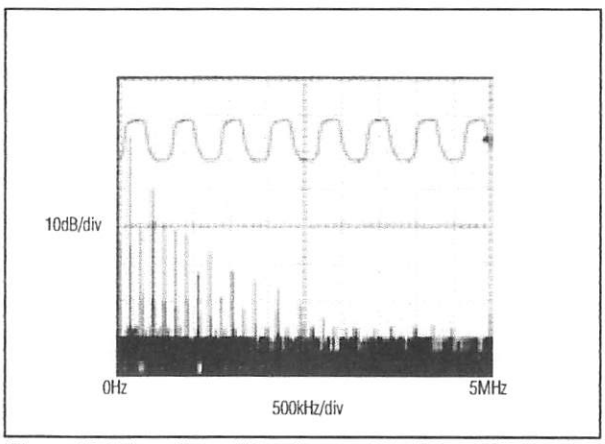


Figure 13. Driver Output Waveform and FFT Plot of MAX483/ MAX487–MAX489 Transmitting a 150kHz Signal

Low-Power Shutdown Mode (MAX481/MAX483/MAX487)

ow-power shutdown mode is initiated by bringing h $\overline{RE}$ high and DE low. The devices will not shut vn unless both the driver and receiver are disabled. shutdown, the devices typically draw only 0.1µA of pply current.

and DE may be driven simultaneously; the parts are aranteed not to enter shutdown if $\overline{RE}$ is high and DE ow for less than 50ns. If the inputs are in this state at least 600ns, the parts are guaranteed to enter tdown.

the MAX481, MAX483, and MAX487, the t_{ZH} and enable times assume the part was not in the low- ver shutdown state (the MAX485/MAX488–MAX491 MAX1487 can not be shut down). The $t_{ZH(SHDN)}$ $t_{ZL(SHDN)}$ enable times assume the parts were shut vn (see *Electrical Characteristics*).

akes the drivers and receivers longer to become abled from the low-power shutdown state H(SHDN), $t_{ZL(SHDN)}$) than from the operating mode , t_{ZL}). (The parts are in operating mode if the $\overline{RE}$, inputs equal a logical 0,1 or 1,1 or 0, 0.)

Driver Output Protection

Excessive output current and power dissipation caused by faults or by bus contention are prevented by two mechanisms. A foldback current limit on the output stage provides immediate protection against short circuits over the whole common-mode voltage range (see *Typical Operating Characteristics*). In addition, a thermal shutdown circuit forces the driver outputs into a high-impedance state if the die temperature rises excessively.

Propagation Delay

Many digital encoding schemes depend on the difference between the driver and receiver propagation delay times. Typical propagation delays are shown in Figures 15–18 using Figure 14's test circuit.

The difference in receiver delay times, $|t_{PLH} - t_{PHL}|$, is typically under 13ns for the MAX481, MAX485, MAX490, MAX491, and MAX1487 and is typically less than 100ns for the MAX483 and MAX487–MAX489.

The driver skew times are typically 5ns (10ns max) for the MAX481, MAX485, MAX490, MAX491, and MAX1487, and are typically 100ns (800ns max) for the MAX483 and MAX487–MAX489.

ow-Power, Slew-Rate-Limited
S-485/RS-422 Transceivers

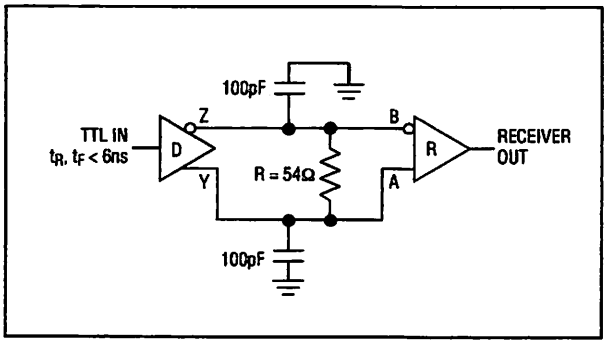
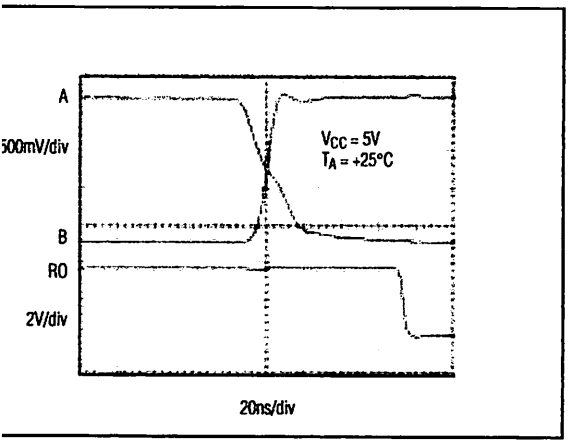


Figure 14. Receiver Propagation Delay Test Circuit



ure 15. MAX481/MAX485/MAX490/MAX491/MAX1487 eiver t_{PHL}

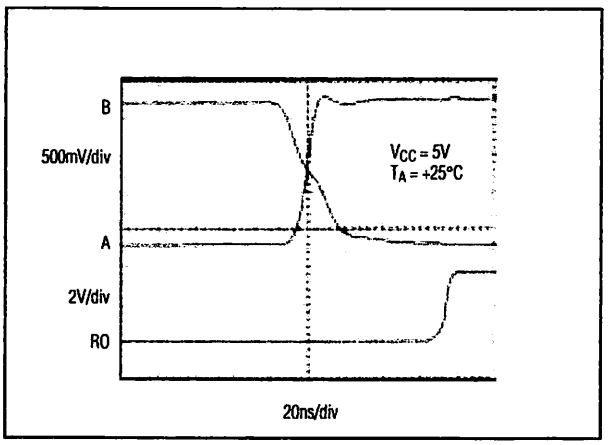
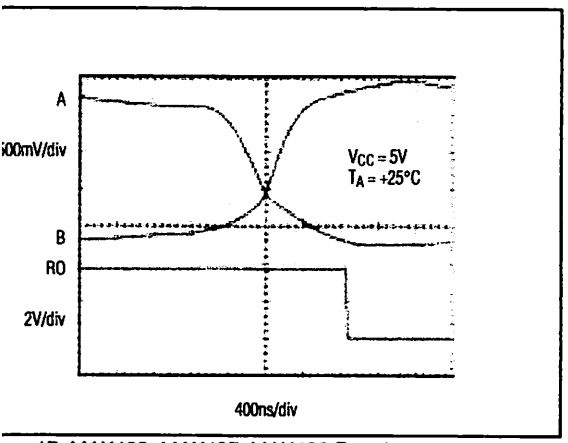


Figure 16. MAX481/MAX485/MAX490/MAX491/MAX1487 Receiver t_{PLH}



ure 17. MAX483, MAX487–MAX489 Receiver t_{PHL}

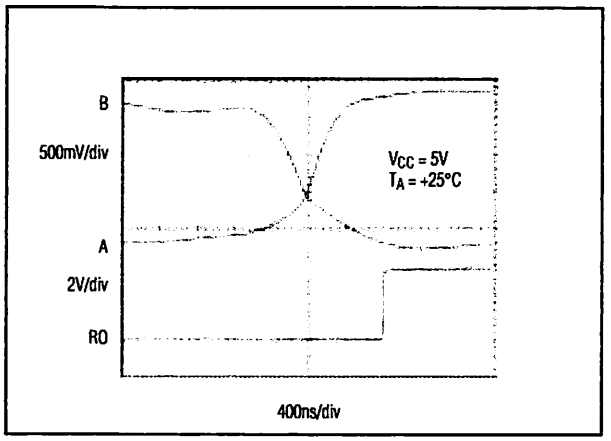


Figure 18. MAX483, MAX487–MAX489 Receiver t_{PLH}

Line Length vs. Data Rate

RS-485/RS-422 standard covers line lengths up to 0 feet. For line lengths greater than 4000 feet, see ure 23.

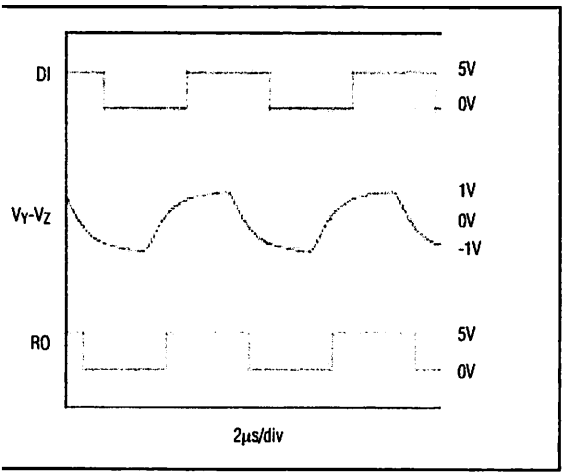
ures 19 and 20 show the system differential voltage the parts driving 4000 feet of 26AWG twisted-pair at 110kHz into 120Ω loads.

Typical Applications

MAX481, MAX483, MAX485, MAX487–MAX491, and X1487 transceivers are designed for bidirectional data nmunications on multipoint bus transmission lines.

Figures 21 and 22 show typical network applications circuits. These parts can also be used as line repeaters, with cable lengths longer than 4000 feet, as shown in Figure 23.

To minimize reflections, the line should be terminated at both ends in its characteristic impedance, and stub lengths off the main line should be kept as short as possible. The slew-rate-limited MAX483 and MAX487–MAX489 are more tolerant of imperfect termination.



ire 19. MAX481/MAX485/MAX490/MAX491/MAX1487 System erential Voltage at 110kHz Driving 4000ft of Cable

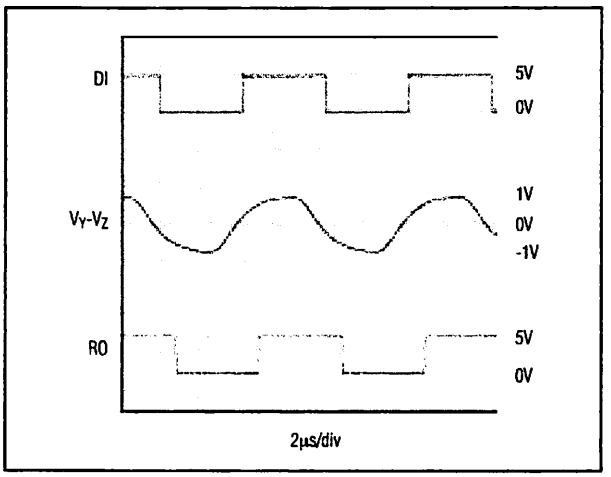
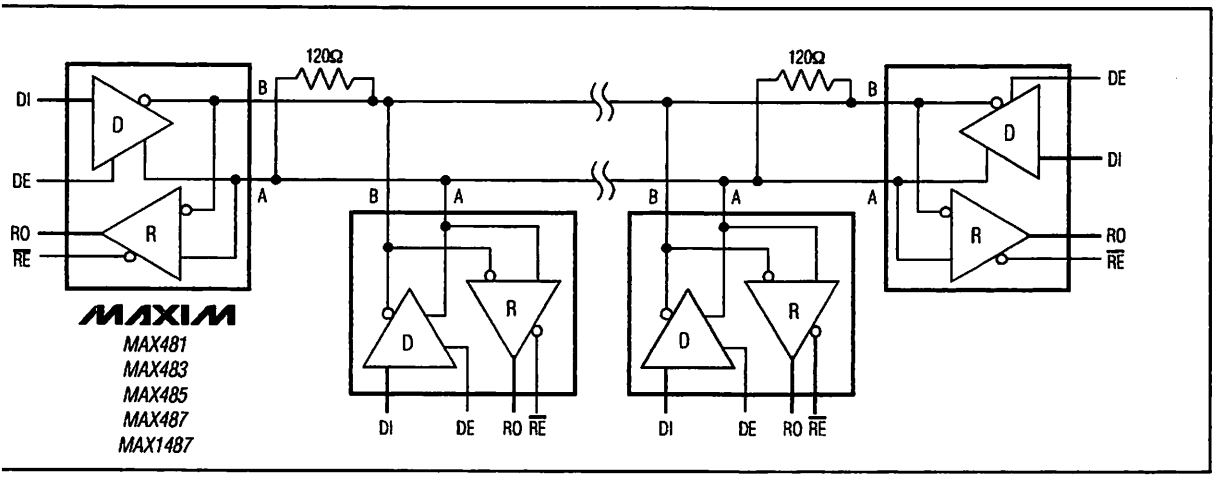
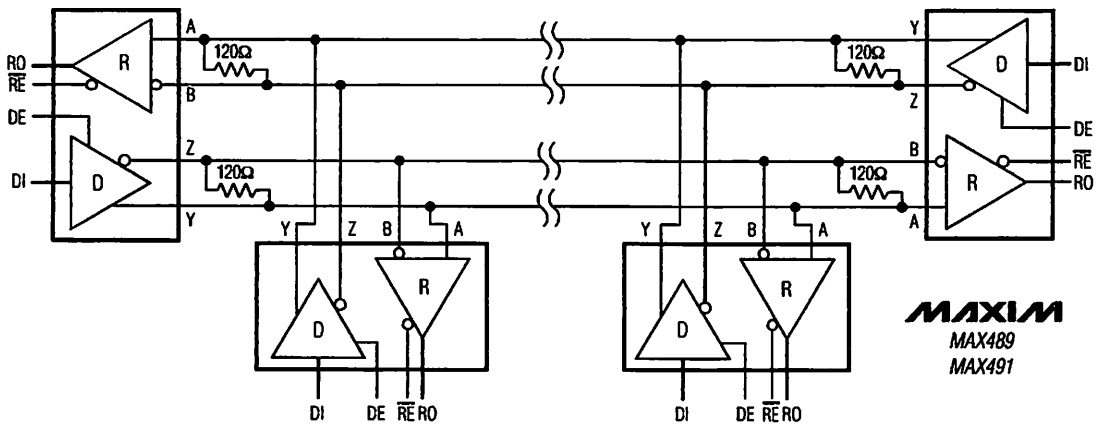


Figure 20. MAX483, MAX487–MAX489 System Differential Voltage at 110kHz Driving 4000ft of Cable

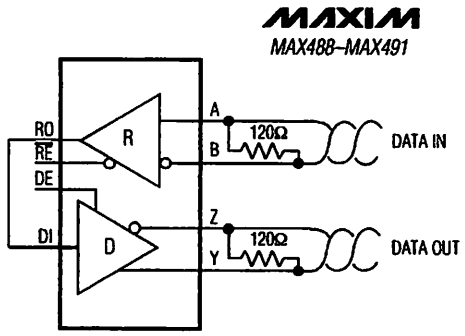


ire 21. MAX481/MAX483/MAX485/MAX487/MAX1487 Typical Half-Duplex RS-485 Network



NOTE: $\overline{RE}$ AND DE ON MAX489/MAX491 ONLY.

ure 22. MAX488–MAX491 Full-Duplex RS-485 Network



NOTE: $\overline{RE}$ AND DE ON MAX489/MAX491 ONLY.

ure 23. Line Repeater for MAX488–MAX491

Isolated RS-485

For isolated RS-485 applications, see the MAX253 and MAX1480 data sheets.

Low-Power, Slew-Rate-Limited RS-485/RS-422 Transceivers

Ordering Information

PART	TEMP. RANGE	PIN-PACKAGE
AX481CPA	0°C to +70°C	8 Plastic DIP
AX481CSA	0°C to +70°C	8 SO
AX481CUA	0°C to +70°C	8 µMAX
AX481C/D	0°C to +70°C	Dice*
AX481EPA	-40°C to +85°C	8 Plastic DIP
AX481ESA	-40°C to +85°C	8 SO
AX481MJA	-55°C to +125°C	8 CERDIP
AX483CPA	0°C to +70°C	8 Plastic DIP
AX483CSA	0°C to +70°C	8 SO
AX483CUA	0°C to +70°C	8 µMAX
AX483C/D	0°C to +70°C	Dice*
AX483EPA	-40°C to +85°C	8 Plastic DIP
AX483ESA	-40°C to +85°C	8 SO
AX483MJA	-55°C to +125°C	8 CERDIP
AX485CPA	0°C to +70°C	8 Plastic DIP
AX485CSA	0°C to +70°C	8 SO
AX485CUA	0°C to +70°C	8 µMAX
AX485C/D	0°C to +70°C	Dice*
AX485EPA	-40°C to +85°C	8 Plastic DIP
AX485ESA	-40°C to +85°C	8 SO
AX485MJA	-55°C to +125°C	8 CERDIP
AX487CPA	0°C to +70°C	8 Plastic DIP
AX487CSA	0°C to +70°C	8 SO
AX487CUA	0°C to +70°C	8 µMAX
AX487C/D	0°C to +70°C	Dice*
AX487EPA	-40°C to +85°C	8 Plastic DIP
AX487ESA	-40°C to +85°C	8 SO
AX487MJA	-55°C to +125°C	8 CERDIP
AX488CPA	0°C to +70°C	8 Plastic DIP
AX488CSA	0°C to +70°C	8 SO
AX488CUA	0°C to +70°C	8 µMAX
AX488C/D	0°C to +70°C	Dice*
AX488EPA	-40°C to +85°C	8 Plastic DIP
AX488ESA	-40°C to +85°C	8 SO
AX488MJA	-55°C to +125°C	8 CERDIP
AX489CPD	0°C to +70°C	14 Plastic DIP
AX489CSD	0°C to +70°C	14 SO
AX489C/D	0°C to +70°C	Dice*
AX489EPD	-40°C to +85°C	14 Plastic DIP
AX489ESD	-40°C to +85°C	14 SO
AX489MJD	-55°C to +125°C	14 CERDIP

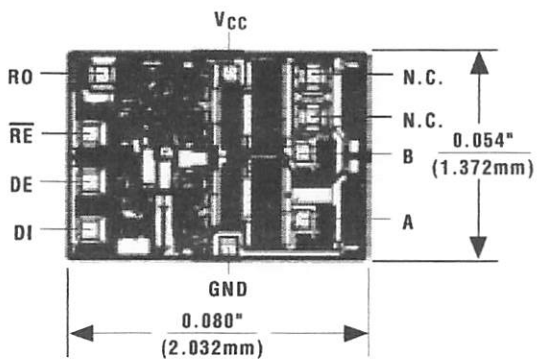
Ordering Information (continued)

PART	TEMP. RANGE	PIN-PACKAGE
MAX490CPA	0°C to +70°C	8 Plastic DIP
MAX490CSA	0°C to +70°C	8 SO
MAX490CUA	0°C to +70°C	8 µMAX
MAX490C/D	0°C to +70°C	Dice*
MAX490EPA	-40°C to +85°C	8 Plastic DIP
MAX490ESA	-40°C to +85°C	8 SO
MAX490MJA	-55°C to +125°C	8 CERDIP
MAX491CPD	0°C to +70°C	14 Plastic DIP
MAX491CSD	0°C to +70°C	14 SO
MAX491C/D	0°C to +70°C	Dice*
MAX491EPD	-40°C to +85°C	14 Plastic DIP
MAX491ESD	-40°C to +85°C	14 SO
MAX491MJD	-55°C to +125°C	14 CERDIP
MAX1487CPA	0°C to +70°C	8 Plastic DIP
MAX1487CSA	0°C to +70°C	8 SO
MAX1487CUA	0°C to +70°C	8 µMAX
MAX1487C/D	0°C to +70°C	Dice*
MAX1487EPA	-40°C to +85°C	8 Plastic DIP
MAX1487ESA	-40°C to +85°C	8 SO
MAX1487MJA	-55°C to +125°C	8 CERDIP

* *Contact factory for dice specifications.*

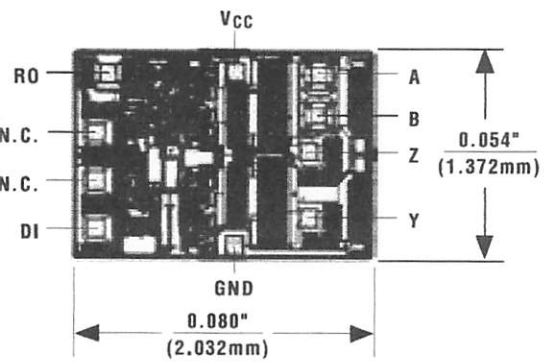
Chip Topographies

MAX481/MAX483/MAX485/MAX487/MAX1487

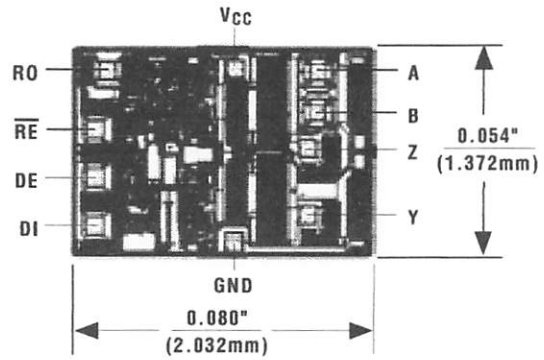


Chip Topographies (continued)

MAX488/MAX490



MAX489/MAX491



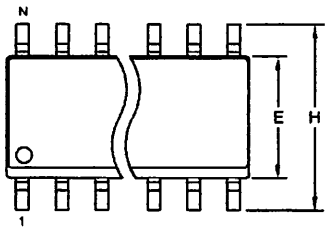
TRANSISTOR COUNT: 248
SUBSTRATE CONNECTED TO GND

Package Information

package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information
) www.maxim-ic.com/packages.)

SOICN .EPS

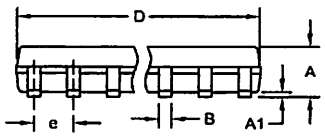
	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	0.053	0.069	1.35	1.75
A1	0.004	0.010	0.10	0.25
B	0.014	0.019	0.35	0.49
C	0.007	0.010	0.19	0.25
e	0.050 BSC		1.27 BSC	
E	0.150	0.157	3.80	4.00
H	0.228	0.244	5.80	6.20
L	0.016	0.050	0.40	1.27



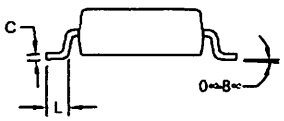
TOP VIEW

VARIATIONS:

	INCHES		MILLIMETERS			
DIM	MIN	MAX	MIN	MAX	N	MS012
D	0.189	0.197	4.80	5.00	8	AA
D	0.337	0.344	8.55	8.75	14	AB
D	0.386	0.394	9.80	10.00	16	AC



FRONT VIEW



SIDE VIEW

NOTES:
1. D&E DO NOT INCLUDE MOLD FLASH.
2. MOLD FLASH OR PROTRUSIONS NOT TO EXCEED 0.15mm (.006").
3. LEADS TO BE COPLANAR WITHIN 0.10mm (.004").
4. CONTROLLING DIMENSION: MILLIMETERS.
5. MEETS JEDEC MS012.
6. N = NUMBER OF PINS.

DALLAS SEMICONDUCTOR MAXIM

PROPRIETARY INFORMATION

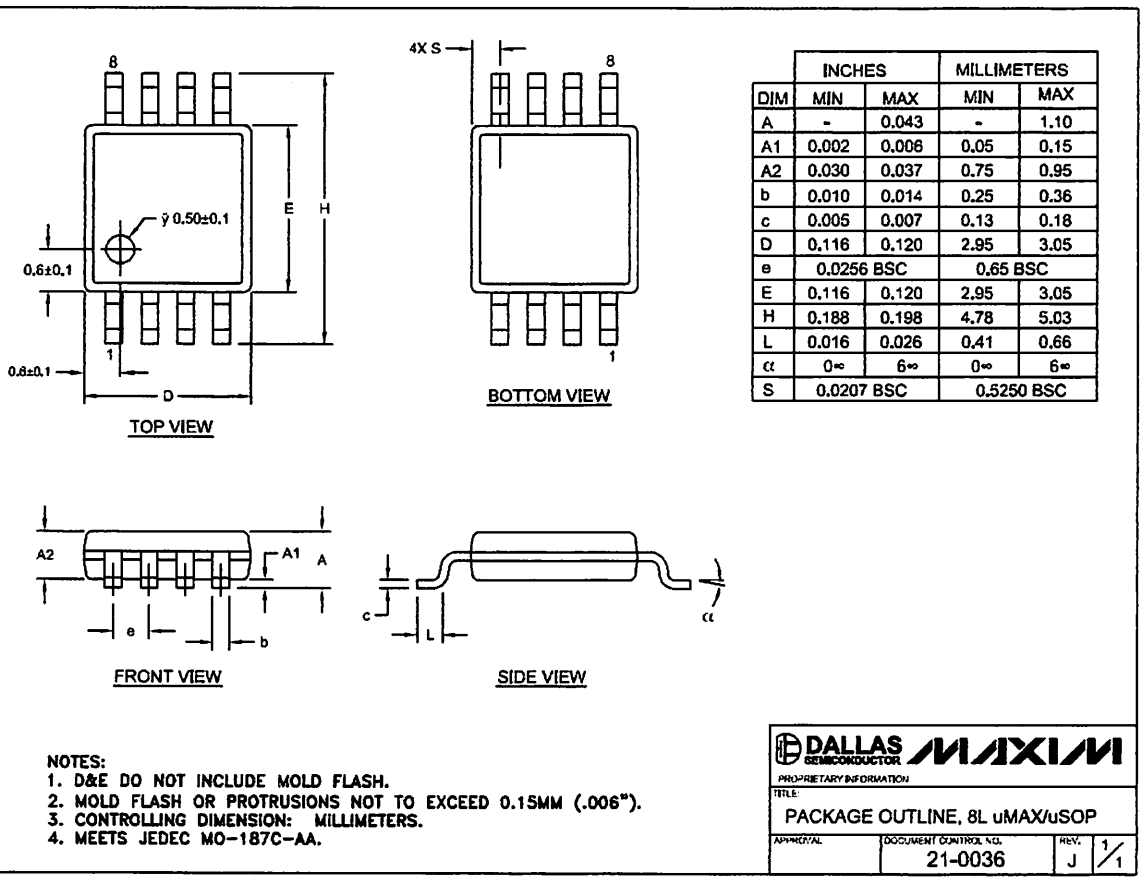
TITLE:

PACKAGE OUTLINE, .150" SOIC

APPROVAL	DOCUMENT CONTROL NO.	REV.	
	21-0041	B	1/1

Package Information (continued)

e package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information to **www.maxim-ic.com/packages**.)



DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	-	0.043	-	1.10
A1	0.002	0.006	0.05	0.15
A2	0.030	0.037	0.75	0.95
b	0.010	0.014	0.25	0.36
c	0.005	0.007	0.13	0.18
D	0.116	0.120	2.95	3.05
e	0.0256 BSC		0.65 BSC	
E	0.116	0.120	2.95	3.05
H	0.188	0.198	4.78	5.03
L	0.016	0.026	0.41	0.66
α	0∞	6∞	0∞	6∞
S	0.0207 BSC		0.5250 BSC	

6LUMAXD.EPS

NOTES:
1. D&E DO NOT INCLUDE MOLD FLASH.
2. MOLD FLASH OR PROTRUSIONS NOT TO EXCEED 0.15MM (.006").
3. CONTROLLING DIMENSION: MILLIMETERS.
4. MEETS JEDEC MO-187C-AA.

DALLAS SEMICONDUCTOR MAXIM

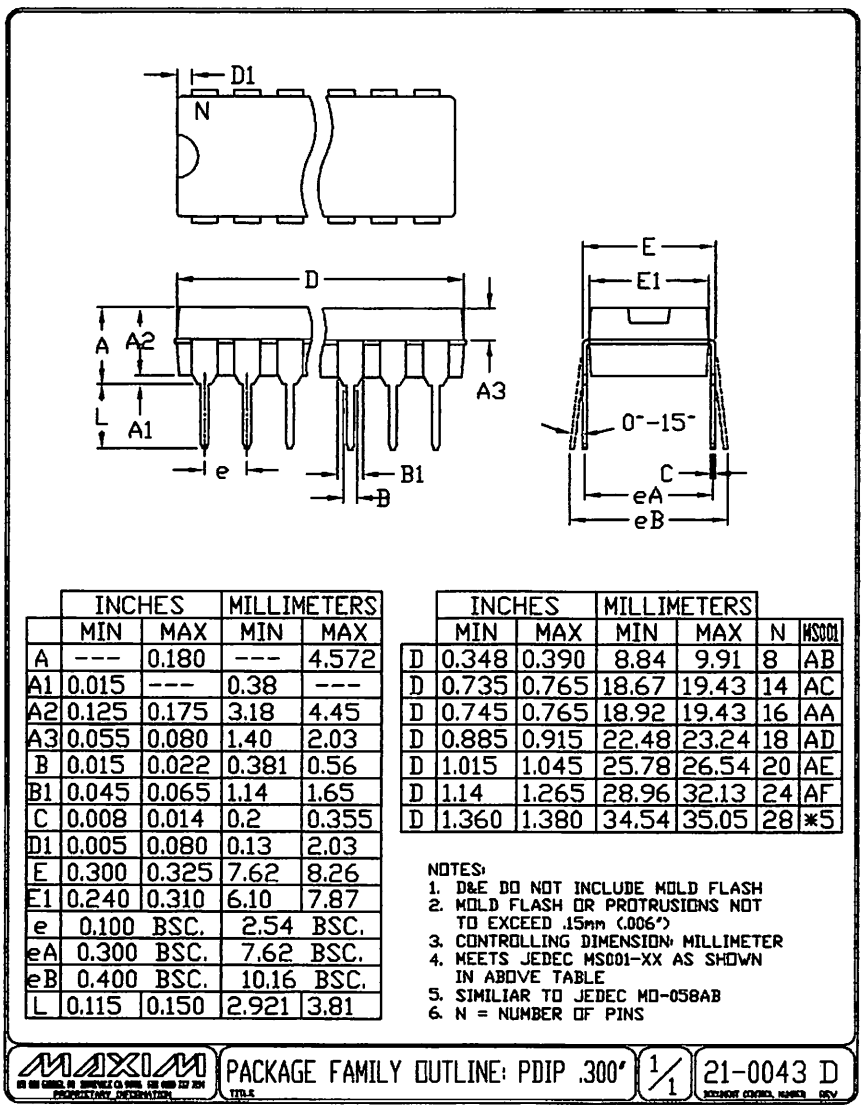
PROPRIETARY INFORMATION

TITLE: PACKAGE OUTLINE, 8L uMAX/uSOP

APPROVAL	DOCUMENT CONTROL NO.	REV.	
	21-0036	J	1/1

Package Information (continued)

package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information) www.maxim-ic.com/packages.)



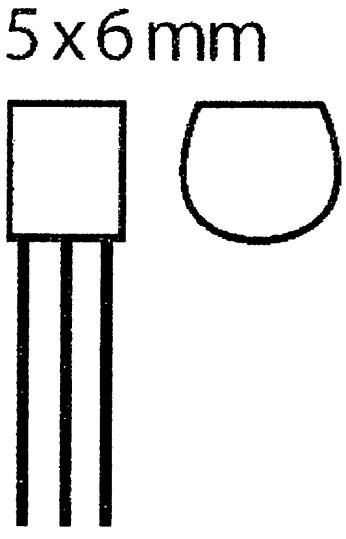
	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	---	0.180	---	4.572
A1	0.015	---	0.38	---
A2	0.125	0.175	3.18	4.45
A3	0.055	0.080	1.40	2.03
B	0.015	0.022	0.381	0.56
B1	0.045	0.065	1.14	1.65
C	0.008	0.014	0.2	0.355
D1	0.005	0.080	0.13	2.03
E	0.300	0.325	7.62	8.26
E1	0.240	0.310	6.10	7.87
e	0.100 BSC.		2.54 BSC.	
eA	0.300 BSC.		7.62 BSC.	
eB	0.400 BSC.		10.16 BSC.	
L	0.115	0.150	2.921	3.81

	INCHES		MILLIMETERS			
	MIN	MAX	MIN	MAX	N	MS001
D	0.348	0.390	8.84	9.91	8	AB
D	0.735	0.765	18.67	19.43	14	AC
D	0.745	0.765	18.92	19.43	16	AA
D	0.885	0.915	22.48	23.24	18	AD
D	1.015	1.045	25.78	26.54	20	AE
D	1.14	1.265	28.96	32.13	24	AF
D	1.360	1.380	34.54	35.05	28	*5

NOTES:
1. D&E DO NOT INCLUDE MOLD FLASH
2. MOLD FLASH OR PROTRUSIONS NOT TO EXCEED .15mm (.006")
3. CONTROLLING DIMENSION: MILLIMETER
4. MEETS JEDEC MS001-XX AS SHOWN IN ABOVE TABLE
5. SIMILIAR TO JEDEC MO-058AB
6. N = NUMBER OF PINS

MAXIM	PACKAGE FAMILY OUTLINE: PDIP .300"	1/1	21-0043 D
PROPRIETARY INFORMATION	TITLE		DOCUMENT CONTROL NUMBER REV

2SC828 Information Datasheet



2SC828 Specifications

Category : Transistors
Class : Transistors; Bipolar; Si NPN Low-Power
Type : Bipolar, Si NPN Low-Power
Military/High-Rel : N
V(BR)CEO (V) : 30
V(BR)CBO (V) : 30
I(C) Max. (A) : 50m
Absolute Max. Power Diss. (W) : 250m
Maximum Operating Temp (uC) : 125x
h(FE) Min. Current gain. : 65
@I(C) (A) (Test Condition) : 2.0мд
@V(CE) (V) (Test Condition) : 5.0X
Package Style : TO-92
Mounting Style : T

Description:

2SC 828
Transistor Silicon NPN / 30V / 0.05A / 0.25W / 220MH

Packing unit: 1

Order Code: 2SC 828

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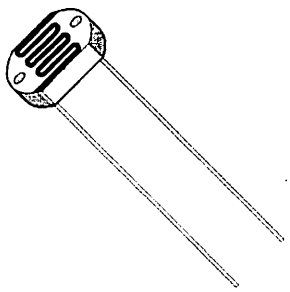
133 Kings Road, Madison, NJ 07940 USA
Telephone: (973)377-9566
Fax: (973)377-3078
Email: info@americanmicrosemi.com

VAC54

MINIATURE CADMIUM SULPHIDE PHOTOCONDUCTIVE CELL

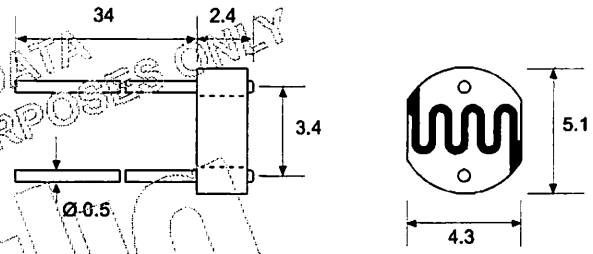
nvac

LIGHT DEPENDENT RESISTOR



FEATURES

- *Miniature open frame package.*
- *Epoxy coated.*
- *Moisture resistant.*
- *Spectral response similar to the human eye.*
- *Applications include dusk - dawn lighting control.*



Dimensions in millimetres

SPECIFICATION AND PERFORMANCE

Model	Vmax (VDC)	Pmax (mW)	Ambient Temp (°C)	Spectral Peak (nm)	Light Resistance at 10 lux (kΩ)	Dark Resistance (MΩ)	Gamma Char. T_{10}^{100}	Response Time (ms)	
								Rise Time	Decay Time
VAC54	150	100	-30 ~ +80	590	50 ~ 140	20	0.7	20	30

Measuring Conditions

Light Resistance:
measured at 10 lux with standard light A (2854k color temperature) and 2h pre-illumination at 400-600 lux prior to testing.

Dark Resistance:
measured 10 seconds after pulsed 10 lux.

Gamma Characteristic:
between 10 lux and 100 lux and given by

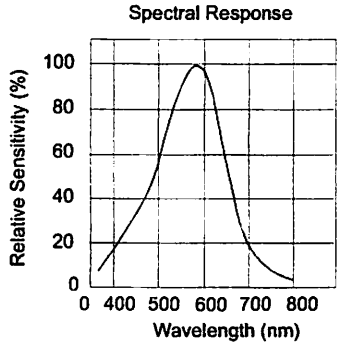
$$T = \frac{\log (R10/R100)}{\log (100/10)} - \log (R10/R100)$$

R10, R100 cell resistance at 10 lux and 100 lux.
The error of T is +0.1.

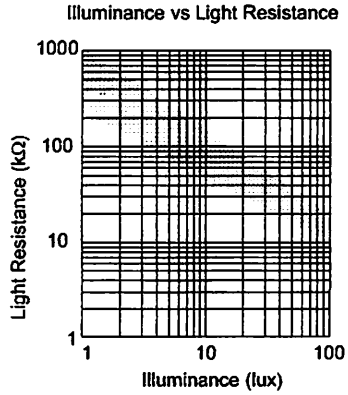
Pmax:
Max. power dissipation at ambient temperature of 25°C.

Vmax:
Max. voltage in darkness that may be applied to the cell continuously.

Spectral Response



Illuminance vs Light Resistance



Issue 0219

National Semiconductor

February 1995

LM78XX Series Voltage Regulators

General Description

The LM78XX series of three terminal regulators is available with several fixed output voltages making them useful in a wide range of applications. One of these is local on card regulation, eliminating the distribution problems associated with single point regulation. The voltages available allow these regulators to be used in logic systems, instrumentation, HiFi, and other solid state electronic equipment. Although designed primarily as fixed voltage regulators these devices can be used with external components to obtain adjustable voltages and currents.

The LM78XX series is available in an aluminum TO-3 package which will allow over 1.0A load current if adequate heat sinking is provided. Current limiting is included to limit the peak output current to a safe value. Safe area protection for the output transistor is provided to limit internal power dissipation. If internal power dissipation becomes too high for the heat sinking provided, the thermal shutdown circuit takes over preventing the IC from overheating.

Considerable effort was expanded to make the LM78XX series of regulators easy to use and mininize the number of external components. It is not necessary to bypass the output, although this does improve transient response. Input bypassing is needed only if the regulator is located far from the filter capacitor of the power supply.

For output voltage other than 5V, 12V and 15V the LM117 series provides an output voltage range from 1.2V to 57V.

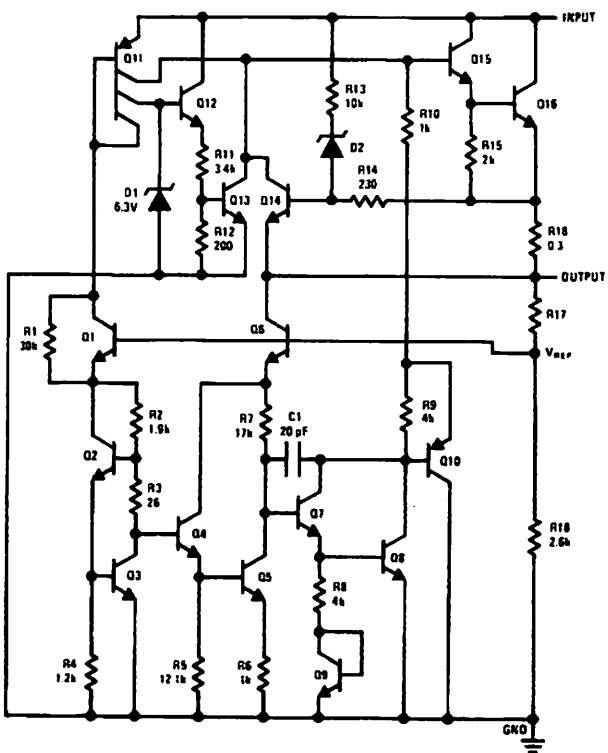
Features

- Output current in excess of 1A
- Internal thermal overload protection
- No external components required
- Output transistor safe area protection
- Internal short circuit current limit
- Available in the aluminum TO-3 package

Voltage Range

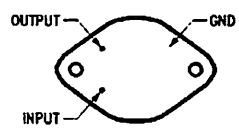
LM7805C	5V
LM7812C	12V
LM7815C	15V

Schematic and Connection Diagrams



TL/H/7746–1

Metal Can Package
TO-3 (K)
Aluminum

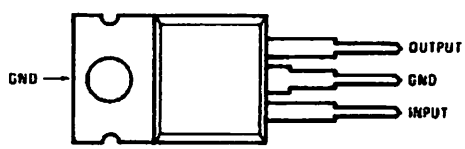


TL/H/7746–2

Bottom View

Order Number LM7805CK, LM7812CK or LM7815CK
See NS Package Number KC02A

Plastic Package
TO-220 (T)



TL/H/7746–3

Top View

Order Number LM7805CT, LM7812CT or LM7815CT
See NS Package Number T03B

RRD-B30M115/Printed in U. S. A.

olute Maximum Ratings

ary/Aerospace specified devices are required, contact the National Semiconductor Sales 'Distributors for availability and specifications.

oltage (V_O = 5V, 12V and 15V)	35V
l Power Dissipation (Note 1)	Internally Limited
ing Temperature Range (T_A)	0°C to +70°C
Maximum Junction Temperature	
(K Package)	150°C
(T Package)	150°C
Storage Temperature Range	−65°C to +150°C
Lead Temperature (Soldering, 10 sec.)	
TO-3 Package K	300°C
TO-220 Package T	230°C

trical Characteristics LM78XXC (Note 2) 0°C ≤ Tj ≤ 125°C unless otherwise noted.

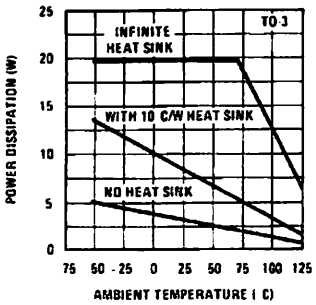
Output Voltage			5V			12V			15V			Units
Input Voltage (unless otherwise noted)			10V			19V			23V			
Parameter	Conditions		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
)utput Voltage	Tj = 25°C, 5 mA ≤ I_O ≤ 1A		4.8	5	5.2	11.5	12	12.5	14.4	15	15.6	V
	P_D ≤ 15W, 5 mA ≤ I_O ≤ 1A		4.75		5.25	11.4		12.6	14.25		15.75	V
	V_{MIN} ≤ V_{IN} ≤ V_{MAX}		(7.5 ≤ V_{IN} ≤ 20)			(14.5 ≤ V_{IN} ≤ 27)			(17.5 ≤ V_{IN} ≤ 30)			V
ine Regulation	I_O = 500 mA	Tj = 25°C		3	50		4	120		4	150	mV
		ΔV_{IN}	(7 ≤ V_{IN} ≤ 25)			14.5 ≤ V_{IN} ≤ 30)			(17.5 ≤ V_{IN} ≤ 30)			V
		0°C ≤ Tj ≤ +125°C			50			120			150	mV
		ΔV_{IN}	(8 ≤ V_{IN} ≤ 20)			(15 ≤ V_{IN} ≤ 27)			(18.5 ≤ V_{IN} ≤ 30)			V
	I_O ≤ 1A	Tj = 25°C			50			120			150	mV
		ΔV_{IN}	(7.5 ≤ V_{IN} ≤ 20)			(14.6 ≤ V_{IN} ≤ 27)			(17.7 ≤ V_{IN} ≤ 30)			V
		0°C ≤ Tj ≤ +125°C			25			60			75	mV
		ΔV_{IN}	(8 ≤ V_{IN} ≤ 12)			(16 ≤ V_{IN} ≤ 22)			(20 ≤ V_{IN} ≤ 26)			V
oad Regulation	Tj = 25°C	5 mA ≤ I_O ≤ 1.5A		10	50		12	120		12	150	mV
		250 mA ≤ I_O ≤ 750 mA			25			60			75	mV
	5 mA ≤ I_O ≤ 1A, 0°C ≤ Tj ≤ +125°C				50			120			150	mV
luiescent Current	I_O ≤ 1A	Tj = 25°C			8			8			8	mA
		0°C ≤ Tj ≤ +125°C			8.5			8.5			8.5	mA
luiescent Current	5 mA ≤ I_O ≤ 1A				0.5			0.5			0.5	mA
hange	Tj = 25°C, I_O ≤ 1A				1.0			1.0			1.0	mA
	V_{MIN} ≤ V_{IN} ≤ V_{MAX}		(7.5 ≤ V_{IN} ≤ 20)			(14.8 ≤ V_{IN} ≤ 27)			(17.9 ≤ V_{IN} ≤ 30)			V
	I_O ≤ 500 mA, 0°C ≤ Tj ≤ +125°C				1.0			1.0			1.0	mA
	V_{MIN} ≤ V_{IN} ≤ V_{MAX}		(7 ≤ V_{IN} ≤ 25)			(14.5 ≤ V_{IN} ≤ 30)			(17.5 ≤ V_{IN} ≤ 30)			V
)utput Noise Voltage	T_A = 25°C, 10 Hz ≤ f ≤ 100 kHz			40			75			90		μV
ipple Rejection	f = 120 Hz	I_O ≤ 1A, Tj = 25°C or	62	80		55	72		54	70		dB
		I_O ≤ 500 mA	62			55			54			dB
		0°C ≤ Tj ≤ +125°C										
	V_{MIN} ≤ V_{IN} ≤ V_{MAX}		(8 ≤ V_{IN} ≤ 18)			(15 ≤ V_{IN} ≤ 25)			(18.5 ≤ V_{IN} ≤ 28.5)			V
ropout Voltage	Tj = 25°C, I_{OUT} = 1A			2.0			2.0			2.0		V
)utput Resistance	f = 1 kHz			8			18			19		mΩ
hort-Circuit Current	Tj = 25°C			2.1			1.5			1.2		A
eak Output Current	Tj = 25°C			2.4			2.4			2.4		A
verage TC of V_{OUT}	0°C ≤ Tj ≤ +125°C, I_O = 5 mA			0.6			1.5			1.8		mV/°C
)ut Voltage equired to Maintain ine Regulation	Tj = 25°C, I_O ≤ 1A			7.5		14.6			17.7			V

Thermal resistance of the TO-3 package (K, KC) is typically 4°C/W junction to case and 35°C/W case to ambient. Thermal resistance of the TO-220 (T) is typically 4°C/W junction to case and 50°C/W case to ambient.

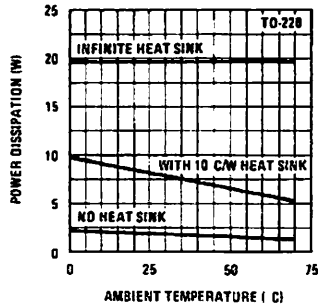
All characteristics are measured with capacitor across the input of 0.22 μF, and a capacitor across the output of 0.1μF. All characteristics except noise and ripple rejection ratio are measured using pulse techniques (t_w ≤ 10 ms, duty cycle ≤ 5%). Output voltage changes due to changes in internal are must be taken into account separately.

Typical Performance Characteristics

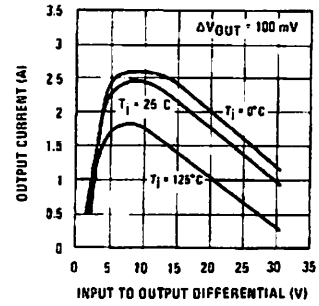
Maximum Average Power Dissipation



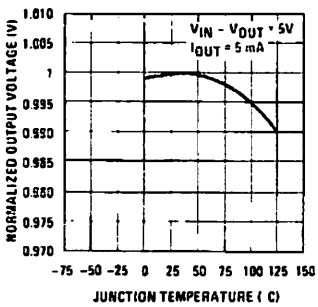
Maximum Average Power Dissipation



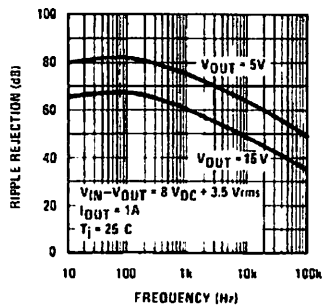
Peak Output Current



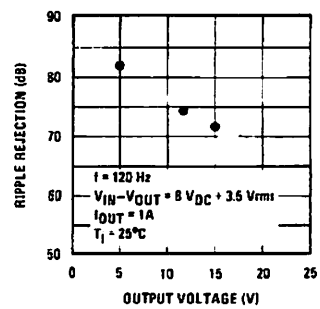
Output Voltage (Normalized to 1V at TJ = 25°C)



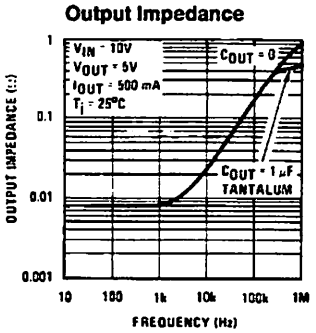
Ripple Rejection



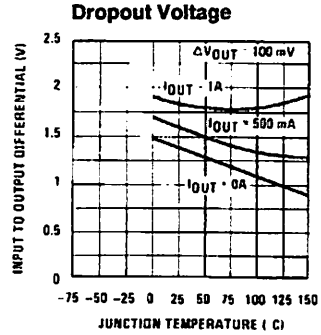
Ripple Rejection



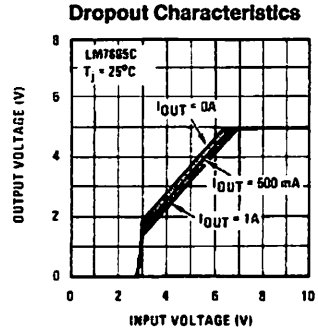
Output Impedance



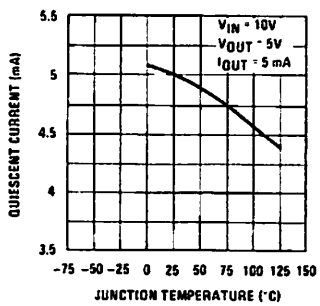
Dropout Voltage



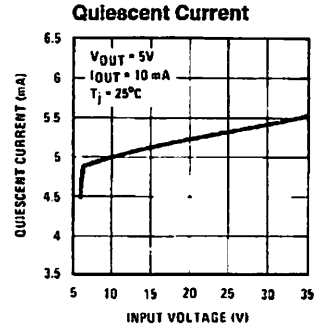
Dropout Characteristics



Quiescent Current

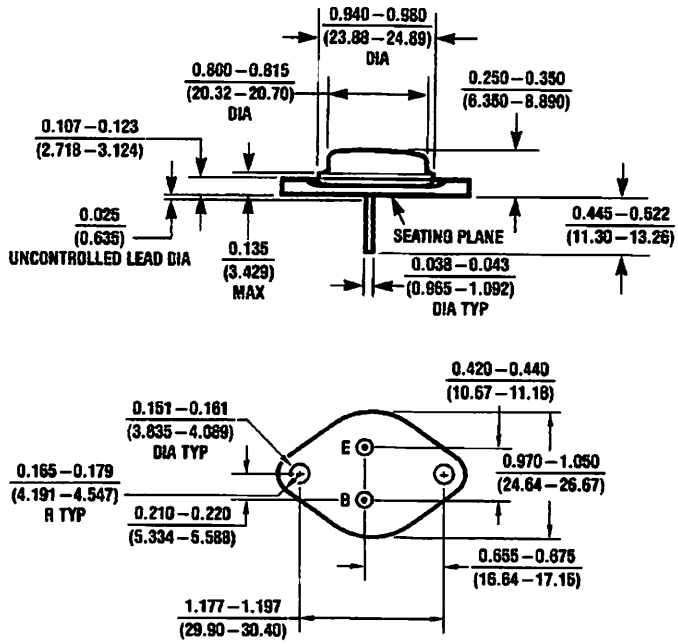


Quiescent Current



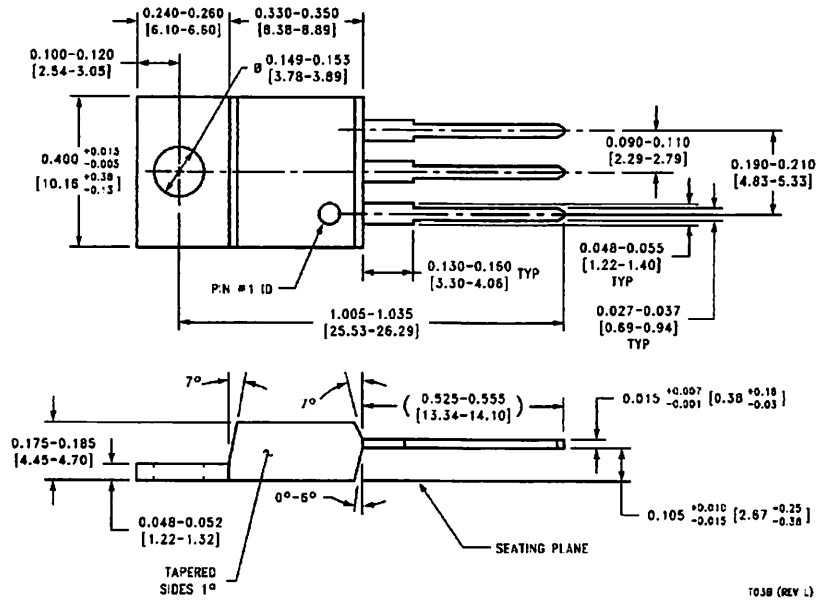
TL/H/7746–4

Physical Dimensions inches (millimeters)



Aluminum Metal Can Package (KC)
Order Number LM7805CK, LM7812CK or LM7815CK
NS Package Number KC02A

Physical Dimensions inches (millimeters) (Continued)



TO-220 Package (T)
Order Number LM7805CT, LM7812CT or LM7815CT
NS Package Number T03B

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2. A critical component is any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

National Semiconductor Corporation
1111 West Bardin Road
Arlington, TX 76017
Tel: 1(600) 272-9959
Fax: 1(800) 737-7018

National Semiconductor Europe
Fax: (+49) 0-180-530 85 86
Email: cnjwge@tevm2.nsc.com
Deutsch Tel: (+49) 0-180-530 85 85
English Tel: (+49) 0-180-532 78 32
Français Tel: (+49) 0-180-532 93 58
Italiano Tel: (+49) 0-180-534 16 80

National Semiconductor Hong Kong Ltd.
13th Floor, Straight Block,
Ocean Centre, 5 Canton Rd.
Tsimshatsui, Kowloon
Hong Kong
Tel: (852) 2737-1600
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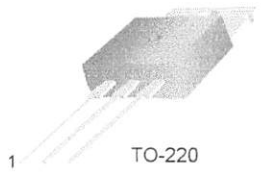
TIP31 Series(TIP31/31A/31B/31C)

Medium Power Linear Switching Applications

- Complementary to TIP32/32A/32B/32C



1 TO-220

1.Base 2.Collector 3.Emitter

NPN Epitaxial Silicon Transistor

Absolute Maximum Ratings T_C=25°C unless otherwise noted

Symbol	Parameter		Value	Units
V_{CBO}	Collector-Base Voltage	: TIP31	40	V
		: TIP31A	60	V
		: TIP31B	80	V
		: TIP31C	100	V
V_{CEO}	Collector-Emitter Voltage	: TIP31	40	V
		: TIP31A	60	V
		: TIP31B	80	V
		: TIP31C	100	V
V_{EBO}	Emitter-Base Voltage		5	V
I_C	Collector Current (DC)		3	A
I_{CP}	Collector Current (Pulse)		5	A
I_B	Base Current		1	A
P_C	Collector Dissipation (T_C=25°C)		40	W
P_C	Collector Dissipation (T_a=25°C)		2	W
T_J	Junction Temperature		150	°C
T_{STG}	Storage Temperature		- 65 ~ 150	°C

Electrical Characteristics T_C=25°C unless otherwise noted

Symbol	Parameter	Test Condition	Min.	Max.	Units
V_{CEO}(sus)	* Collector-Emitter Sustaining Voltage				
	: TIP31	I_C = 30mA, I_B = 0	40		V
	: TIP31A		60		V
	: TIP31B		80		V
	: TIP31C		100		V
I_{CEO}	Collector Cut-off Current				
	: TIP31/31A	V_{CE} = 30V, I_B = 0		0.3	mA
	: TIP31B/31C	V_{CE} = 60V, I_B = 0		0.3	mA
I_{CES}	Collector Cut-off Current				
	: TIP31	V_{CE} = 40V, V_{EB} = 0		200	μA
	: TIP31A	V_{CE} = 60V, V_{EB} = 0		200	μA
	: TIP31B	V_{CE} = 80V, V_{EB} = 0		200	μA
	: TIP31C	V_{CE} = 100V, V_{EB} = 0		200	μA
I_{EBO}	Emitter Cut-off Current	V_{EB} = 5V, I_C = 0		1	mA
h_{FE}	* DC Current Gain	V_{CE} = 4V, I_C = 1A	25		
		V_{CE} = 4V, I_C = 3A	10	50	
V_{CE}(sat)	* Collector-Emitter Saturation Voltage	I_C = 3A, I_B = 375mA		1.2	V
V_{BE}(sat)	* Base-Emitter Saturation Voltage	V_{CE} = 4V, I_C = 3A		1.8	V
f_T	Current Gain Bandwidth Product	V_{CE} = 10V, I_C = 500mA	3.0		MHz

* Pulse Test: PW≤300μs, Duty Cycle≤2%

Typical Characteristics

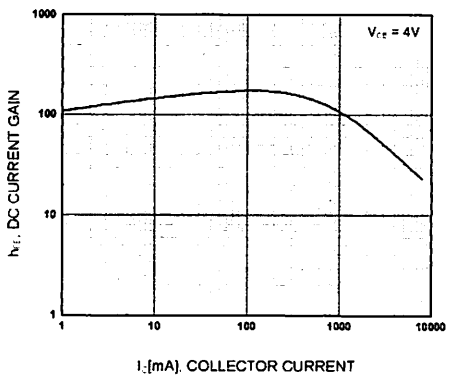


Figure 1. DC current Gain

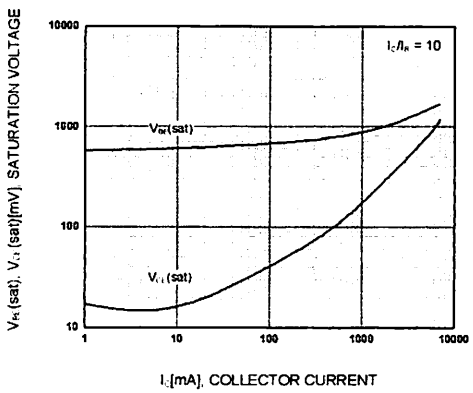


Figure 2. Base-Emitter Saturation Voltage Collector-Emitter Saturation Voltage

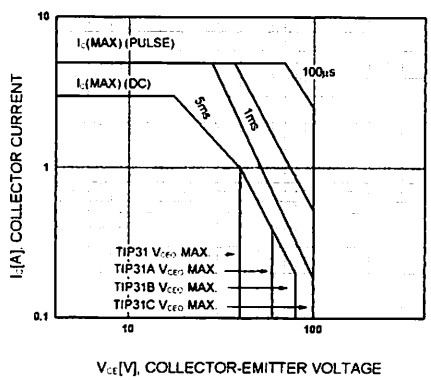


Figure 3. Safe Operating Area

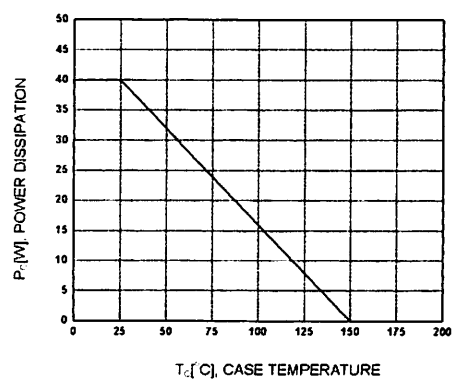
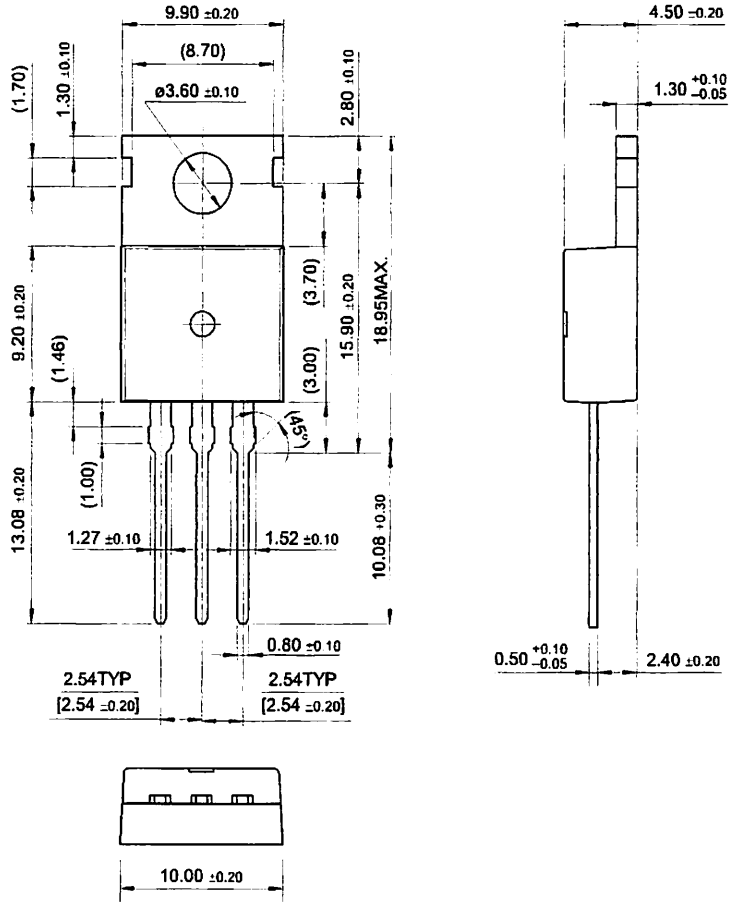


Figure 4. Power Derating

Package Demensions

TO-220



Dimensions in Millimeters

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GTO™
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POP™
PowerTrench®
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QS™
Quiet Series™
SuperSOT™-3
SuperSOT™-6
SuperSOT™-8
SyncFET™
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2. A critical component is any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

PRODUCT STATUS DEFINITIONS

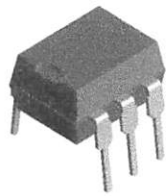
Definition of Terms

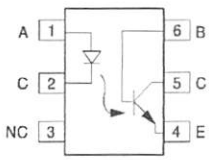
Datasheet Identification	Product Status	Definition
Advance Information	Formative or In Design	This datasheet contains the design specifications for product development. Specifications may change in any manner without notice.
Preliminary	First Production	This datasheet contains preliminary data, and supplementary data will be published at a later date. Fairchild Semiconductor reserves the right to make changes at any time without notice in order to improve design.
No Identification Needed	Full Production	This datasheet contains final specifications. Fairchild Semiconductor reserves the right to make changes at any time without notice in order to improve design.
Obsolete	Not In Production	This datasheet contains specifications on a product that has been discontinued by Fairchild semiconductor. The datasheet is printed for reference information only.

Optocoupler, Phototransistor Output, With Base Connection

Features

- Isolation Test Voltage 5300 V_{RMS}
- Interfaces with Common Logic Families
- Input-output Coupling Capacitance < 0.5 pF
- Industry Standard Dual-in-line 6-pin Package





i173004

Agency Approvals

- UL File #E52744 System Code H or J
- DIN EN 60747-5-2(VDE0884)
  DIN EN 60747-5-5 pending
  Available with Option 1

Applications

AC Mains Detection

Reed relay driving

Switch Mode Power Supply Feedback

Telephone Ring Detection

Logic Ground Isolation

Logic Coupling with High Frequency Noise Rejection

Description

The 4N25 family is an Industry Standard Single Channel Phototransistor Coupler.This family includes the 4N25/ 4N26/ 4N27/ 4N28. Each optocoupler consists of gallium arsenide infrared LED and a silicon NPN phototransistor.

These couplers are Underwriters Laboratories (UL) listed to comply with a 5300 V_{RMS} isolation test voltage. This isolation performance is accomplished through special Vishay manufacturing process.

Compliance to DIN EN 60747-5-2(VDE0884)/ DIN EN 60747-5-5 pending partial discharge isolation specification is available by ordering option1.

These isolation processes and the Vishay ISO9001 quality program results in the highest isolation performance available for a commercial plastic phototransistor optocoupler.

The devices are also available in lead formed configuration suitable for surface mounting and are available either on tape and reel, or in standard tube shipping containers.

Note:

For additional design information see Application Note 45 Normalized Curves

Order Information

Part	Remarks
4N25	CTR > 20 %, DIP-6
4N26	CTR > 20 %, DIP-6
4N27	CTR > 10 %, DIP-6
4N28	CTR > 10 %, DIP-6
4N25-X006	CTR > 20 %, DIP-6 400 mil (option 6)
4N25-X007	CTR > 20 %, SMD-6 (option 7)
4N25-X009	CTR > 20 %, SMD-6 (option 9)
4N26-X006	CTR > 20 %, DIP-6 400 mil (option 6)
4N26-X007	CTR > 20 %, SMD-6 (option 7)
4N26-X009	CTR > 20 %, SMD-6 (option 9)
4N27-X007	CTR > 10 %, SMD-6 (option 7)
4N27-X009	CTR > 10 %, SMD-6 (option 9)
4N28-X009	CTR > 10 %, SMD-6 (option 9)

For additional information on the available options refer to Option Information.

olute Maximum Ratings

25 °C, unless otherwise specified

es in excess of the absolute Maximum Ratings can cause permanent damage to the device. Functional operation of the device is plied at these or any other conditions in excess of those given in the operational sections of this document. Exposure to absolute um Rating for extended periods of the time can adversely affect reliability.

it

Parameter	Test condition	Symbol	Value	Unit
se voltage		V_R	6.0	V
rd current		I_F	60	mA
current	t < 10 µs	I_{FSM}	2.5	A
dissipation		P_{diss}	100	mW

out

Parameter	Test condition	Symbol	Value	Unit
tor-emitter breakdown voltage		V_{CEO}	70	V
r-base breakdown voltage		V_{EBO}	7.0	V
tor current		I_C	50	mA
tor currrent	t < 1.0 ms	I_C	100	mA
dissipation		P_{diss}	150	mW

pler

Parameter	Test condition	Symbol	Value	Unit
on test voltage		V_{ISO}	5300	V_{RMS}
age			≥ 7.0	mm
ance			≥ 7.0	mm
on thickness between r and detector			≥ 0.4	mm
arative tracking index	DIN IEC 112/VDE0303, part 1		175	
on resistance	V_{IO} = 500 V, T_{amb} = 25 °C	R_{IO}	10^{12}	Ω
	V_{IO} = 500 V, T_{amb} = 100 °C	R_{IO}	10^{11}	Ω
ge temperature		T_{stg}	- 55 to + 150	°C
ting temperature		T_{amb}	- 55 to + 100	°C
on temperature		T_j	100	°C
ring temperature	max.10 s, dip soldering: distance to seating plane ≥ 1.5 mm	T_{sld}	260	°C

Electrical Characteristics

T_{amb} = 25 °C, unless otherwise specified
Minimum and maximum values are testing requirements. Typical values are characteristics of the device and are the result of engineering evaluation. Typical values are for information only and are not part of the testing requirements.

Input

Parameter	Test condition	Symbol	Min	Typ.	Max	Unit
Forward voltage[1)]	I_F = 50 mA	V_F		1.3	1.5	V
Reverse current[1)]	V_R = 3.0 V	I_R		0.1	100	µA
Capacitance	V_R = 0 V	C_O		25		pF

[1)] Indicates JEDEC registered values

Output

Parameter	Test condition	Part	Symbol	Min	Typ.	Max	Unit
Collector-base breakdown voltage[1)]	I_C = 100 µA		BV_{CBO}	70			V
Collector-emitter breakdown voltage[1)]	I_C = 1.0 mA		BV_{CEO}	30			V
Emitter-collector breakdown voltage[1)]	I_E = 100 µA		BV_{ECO}	7.0			V
I_{CEO}(dark)[1)]	V_{CE} = 10 V, (base open)	4N25			5.0	50	nA
		4N26			5.0	50	nA
		4N27			5.0	50	nA
		4N28			10	100	nA
I_{CBO}(dark)[1)]	V_{CB} = 10 V, (emitter open)				2.0	20	nA
Collector-emitter capacitance	V_{CE} = 0		C_{CE}		6.0		pF

[1)] Indicates JEDEC registered values

Coupler

Parameter	Test condition	Part	Symbol	Min	Typ.	Max	Unit
Isolation voltage[1)]	Peak, 60 Hz	4N25	V_{IO}	2500			V
		4N26	V_{IO}	1500			V
		4N27	V_{IO}	1500			V
		4N28	V_{IO}	500			V
Saturation voltage, collector-emitter	I_{CE} = 2.0 mA, I_F = 50 mA		$V_{CE(sat)}$			0.5	V
Resistance, input output[1)]	V_{IO} = 500 V		R_{IO}	100			GΩ
Capacitance (input-output)	f = 1.0 MHz		C_{IO}		0.5		pF

[1)] Indicates JEDEC registered values

Current Transfer Ratio

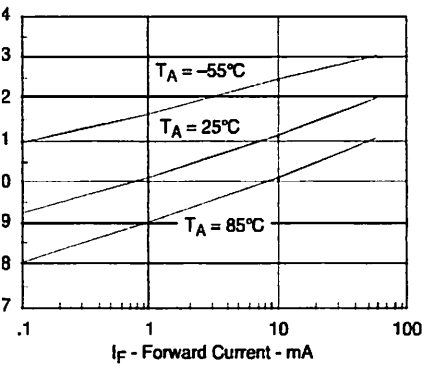
Parameter	Test condition	Part	Symbol	Min	Typ.	Max	Unit
DC Current Transfer Ratio[1)]	V_{CE} = 10 V, I_F = 10 mA	4N25	CTR_{DC}	20	50		%
		4N26	CTR_{DC}	20	50		%
		4N27	CTR_{DC}	10	30		%
		4N28	CTR_{DC}	10	30		%

[1)] Indicates JEDEC registered value

ching Characteristics

Parameter	Test condition	Symbol	Min	Typ.	Max	Unit
and fall times	V_{CE} = 10 V, I_F = 10 mA, R_L = 100 Ω	t_r, t_f		2.0		µs

ical Characteristics (T_{amb} = 25 °C unless otherwise specified)



Forward Voltage vs. Forward Current

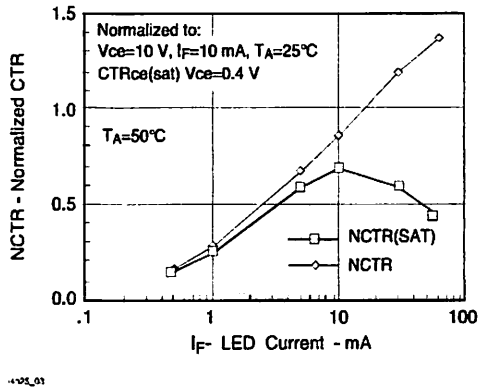
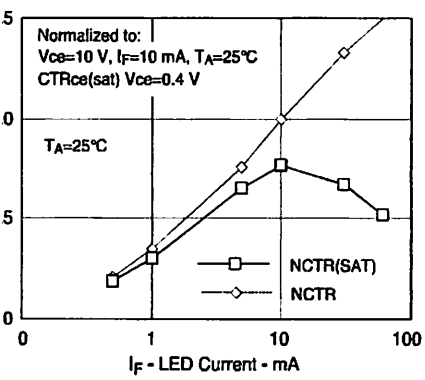


Fig. 3 Normalized Non-saturated and Saturated CTR vs. LED Current



Normalized Non-Saturated and Saturated CTR vs. LED Current

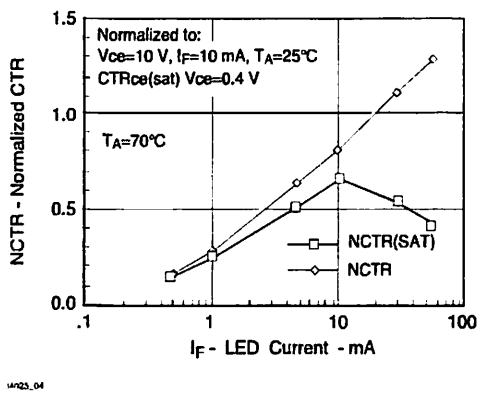


Fig. 4 Normalized Non-saturated and saturated CTR vs. LED Current

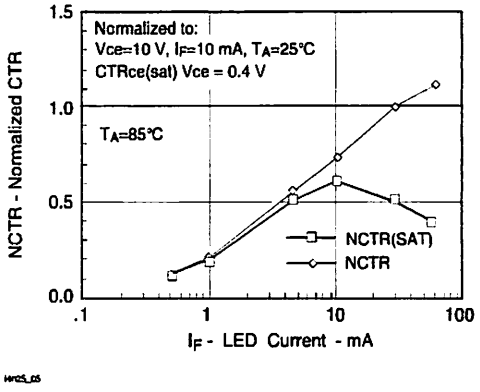


Fig. 5 Normalized Non-saturated and saturated CTR vs. LED Current

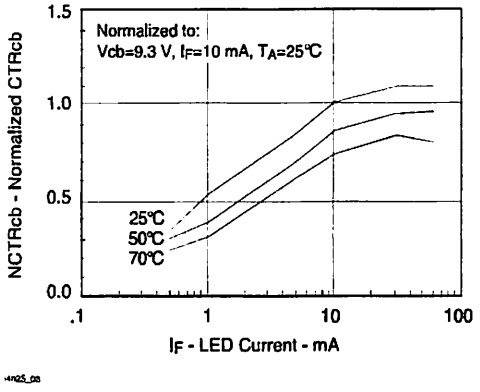


Fig. 8 Normalized CTRcb vs. LED Current and Temp.

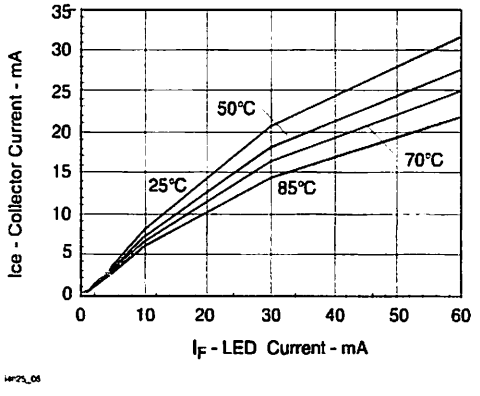


Fig. 6 Collector-Emitter Current vs. Temperature and LED Current

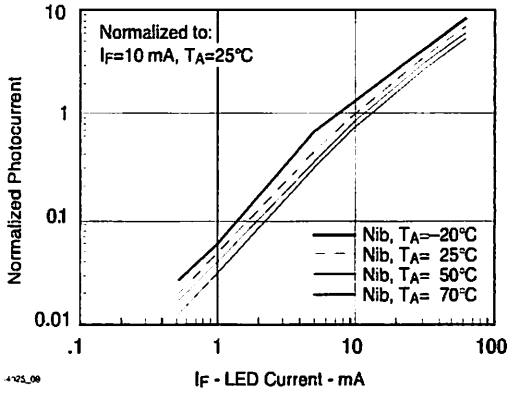


Fig. 9 Normalized Photocurrent vs. I_F and Temp.

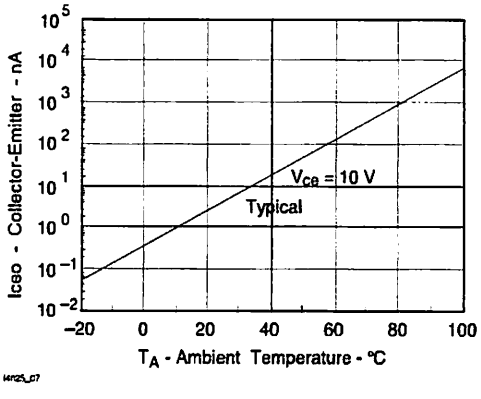


Fig. 7 Collector-Emitter Leakage Current vs.Temp.

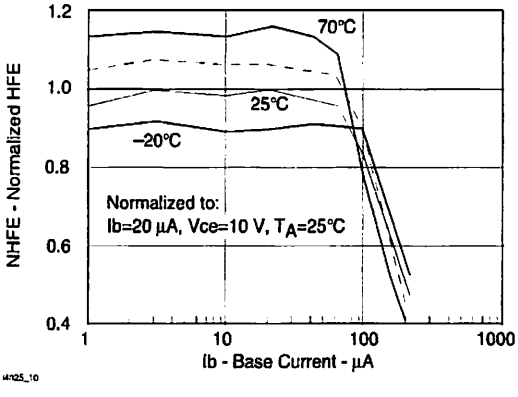
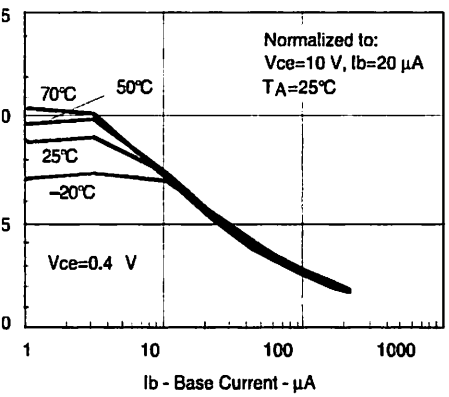


Fig. 10 Normalized Non-saturated HFE vs. Base Current and Temperature



Normalized HFE vs. Base Current and Temp.

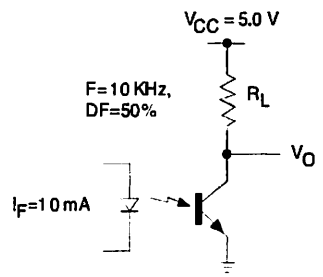
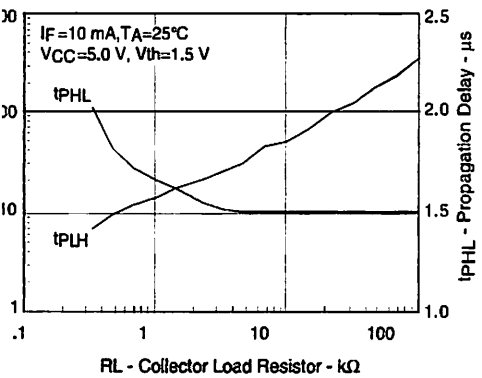
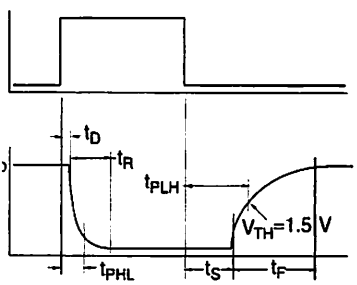


Fig. 14 Switching Schematic

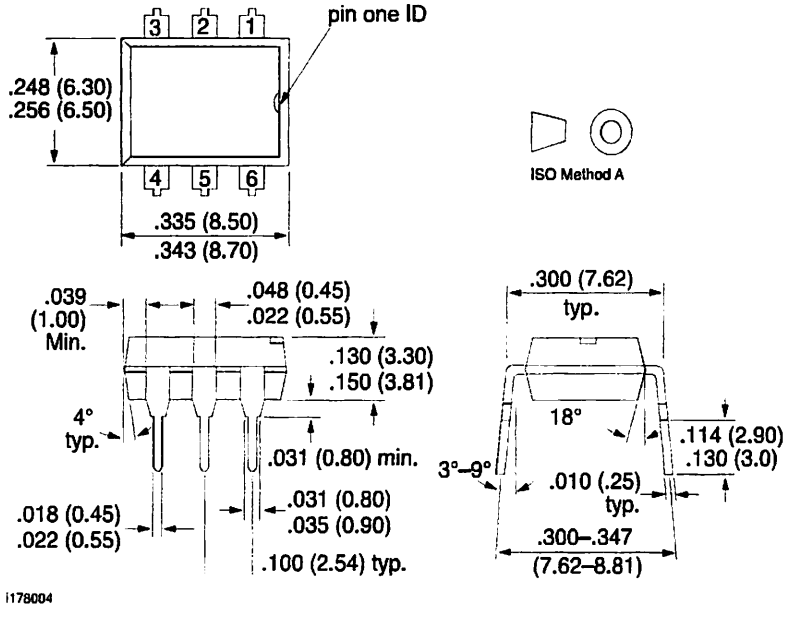


Propagation Delay vs. Collector Load Resistor

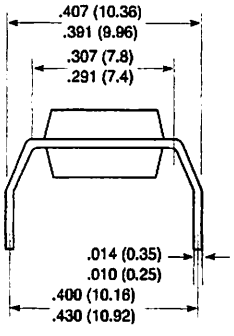


Switching Timing

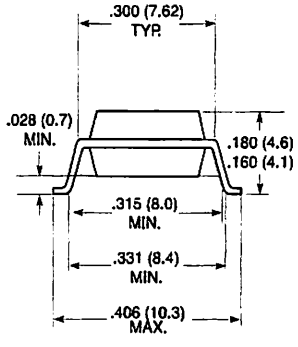
Package Dimensions in Inches (mm)



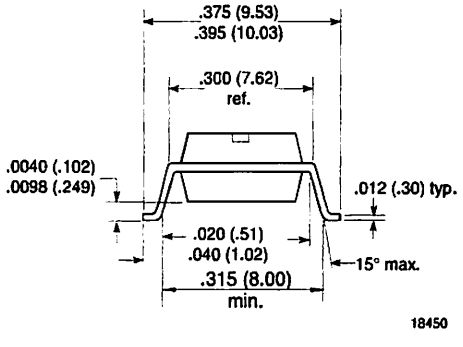
Option 6



Option 7



Option 9



ne Depleting Substances Policy Statement

ne policy of **Vishay Semiconductor GmbH** to

eet all present and future national and international statutory requirements.

egularly and continuously improve the performance of our products, processes, distribution and peratingsystems with respect to their impact on the health and safety of our employees and the public, as ell as their impact on the environment.

articular concern to control or eliminate releases of those substances into the atmosphere which are n as ozone depleting substances (ODSs).

Montreal Protocol (1987) and its London Amendments (1990) intend to severely restrict the use of ODSs orbid their use within the next ten years. Various national and international initiatives are pressing for an r ban on these substances.

ay Semiconductor GmbH has been able to use its policy of continuous improvements to eliminate the f ODSs listed in the following documents.

nnex A, B and list of transitional substances of the Montreal Protocol and the London Amendments spectively

ass I and II ozone depleting substances in the Clean Air Act Amendments of 1990 by the Environmental rotection Agency (EPA) in the USA

ouncil Decision 88/540/EEC and 91/690/EEC Annex A, B and C (transitional substances) respectively.

ay Semiconductor GmbH can certify that our semiconductors are not manufactured with ozone depleting tances and do not contain such substances.

Vishay Semiconductor GmbH, P.O.B. 3535, D-74025 Heilbronn, Germany
Telephone: 49 (0)7131 67 2831, Fax number: 49 (0)7131 67 2423