INSTITUT TEKNOLOGI NASIONAL MALANG
FAKULTAS TEKNOLOGI INDUSTRI
JURUSAN TEKNIK ELEKTRO S-1
KONSENTRASI TEKNIK ELEKTRONIKA

SKRIPSI

PEMANFAATAN TEKNOLOGI MIKROKONTROLLER AT89S51 UNTUK PERANCANGAN DAN PEMBUATAN SIMULASI ALAT PEMINDAH POSISI RANTAI SEPEDA PADA SEPEDA BALAP

Disusun oleh:

KADEK ARTHA MAHARDHIKA
NIM: 99.17.194

SEPTEMBER 2005

[illegible]

LEMBAR PERSETUJUAN

PEMANFAATAN TEKNOLOGI MIKROKONTROLLER AT89S51 UNTUK PERENCANAAN DAN PEMBUATAN SIMULASI ALAT PEMINDAH POSISI RANTAI SEPEDA PADA SEPEDA BALAP

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(Ir. F. Yudi Limpraptono, MT)	**(Ir. Kartiko Ardi Widodo, MT)**

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Judul Skripsi : Pemanfaatan Teknologi Mikrokontroller AT89S51 Untuk Perencanaan dan Pembuatan Simulasi Alat Pemindah Posisi Rantai Sepeda Pada Sepeda Balap.

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Penguji Pertama	**Penguji Kedua**

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"Om Çantih Çantih Çantih Om"

JEMBAR PERSEMBAHAN

ABSTRAKSI

Pemanfaatan Teknologi Mikrokontroller AT89S51 Untuk Perencanaan dan Pembuatan Similasi Alat Pemindah Posisi Rantai Sepeda Pada Sepeda Balap

(Kadek Artha Mahardhika, 9917194, T. Elektro S-1/T. Elektronika)

(Pembimbing: Ir. Kartiko Ardi Widodo, MT)

Skripsi ini bertujuan merancang dan membuat alat pemindah posisi rantai sepeda pada sepeda balap, sehingga memudahkan para pembalap sepeda pemula dalam memindahkan posisi rantai sepeda. Sistem ini menggunakan sebuah sensor kemiringan, Penguat Operasional, *Analog to Digital Converter*, AT89S51, motor DC dan display seven segment.

Pembuatan alat ini pertama-tama adalah dengan melakukan perancangan blok diagram system. Selanjutnya masing-masing blok diagram diimplementasikan dengan rangkaian yang sesuai. Setelah itu pembuatan program mikrokontroller AT89S51 yang nantinya akan berfungsi untuk memproses data yang telah diambil oleh sensor.

Kata kunci: Sensor kemiringan, Penguat Operasional, Mikrokontroller, Perpindahan.

KATA PENGANTAR

Puji syukur penulis panjatkan kepada Tuhan Yang Maha Esa, karena dengan rahmat-Nya penulis dapat menyelasikan laporan skripsi ini.

Adapun maksud dari penyusunan laporan skripsi ini adalah untuk melengkapi persyaratan kurikulum dari Fakultas Teknik Industri Institut Teknologi Nasional Malang dalam menyelesaikan studi untuk meraih gelar kesarjanaan di bidang Teknik Elektronika.

Dalam pembuatan laporan skripsi ini punulis mengambil judul **"PEMANFAATAN TEKNOLOGI MIKROKONTROLLER AT89S51 UNTUK PERENCANAAN DAN PEMBUATAN SIMULASI ALAT PEMINDAH POSISI RANTAI SEPEDA PADA SEPEDA BALAP"**. Penulis menyadari bahwa dalam penulisan laporan skripsi ini masih terdapat kekurangan, sehingga masih jauh dari kesempurnaan. Oleh sebab itu penulis sangat mengharapkan kritik dan saran yang bersifat membangun sehingga dapat berguna di masa mendatang.

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Malang, September 2005

Penulis

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BAB I

PENDAHULUAN

1.1. Latar Belakang

Perkembangan ilmu pengetahuan dan teknologi telah sedemikian majunya, hampir sebagian besar pekerjaan manusia dapat dikerjakan oleh mesin. Hal ini bisa terjadi karena hampir semua aspek kegiatan di dunia ini mempunyai hubungan dengan dunia elektronika. Semua kegiatan itu agaknya sekarang ini akan susah bila dipisahkan dari dunia elektronik. Sehingga dunia elektronika selalu dituntut melakukan riset-riset untuk melakukan inovasi-inovasi baru. Salah satu teknologi yang sangat membantu pekerjaan manusia adalah teknologi yang. memanfaatkan mikrokontroller.

Sekarang ini sepeda gunung sistem pemindahan rantainya masih menggunakan sistem konvensional, dengan memanfaatkan teknologi mikrokontroller kita dapat membuat alat untuk memindahkan posisi rantai sepeda secara otomatis. Untuk mewujudkan salah satu keinginan itulah skripsi ini disusun, dengan judul sebagai berikut: **"PEMANFAATAN TEKNOLOGI MIKROKONTROLLER AT89S51 UNTUK PERENCANAAN DAN PEMBUATAN SIMULASI ALAT PEMINDAH POSISI RANTAI SEPEDA PADA SEPEDA BALAP"**

Dengan memanfaatkan teknologi mikrokontroller, nantinya diharapkan dapat membuat suatu alat pemindahkan posisi rantai sepeda pada sepeda secara otomatis, tanpa menggunakan sistem konvensional lagi.

1.2. Tujuan Penulisan

Adapun tujuan dari pembuatan tugas akhir yang dilaksanakan ini adalah memanfaatkan teknologi mikrokontroller sebagai pengendali alat pemindah posisi rantai sepeda pada sepeda balap secara otomatis.

1.3. Rumusan Masalah

Melihat latar belakang yang telah disampaikan sebelumnya, maka rumusan masalah ditekankan pada :

1. Bagaimana membuat hardware maupun software untuk system yang dapat mengendalikan pemindah posisi rantai sepeda pada sepeda balap.
2. Bagaimana membuat mekanik model simulasi sebuah pemindah posisi rantai sepeda sesuai dengan yang diharapkan.

1.4. Batasan Masalah

Dalam perencanaan dan pembuatan alat ini agar dicapai sasaran yang tepat dan sesuai dengan judul serta mencegah meluasnya pembahasan serta masalah yang timbul, maka dibuat batasan-batasan masalah yakni sebagai berikut :

1. Sistem pengolahan data untuk mengontrol kerja dari hardware berbasis Mikrokontroler AT89S51.
2. Tingkat kecepatan dari sepeda adalah 12 tingkat kecepatan.
3. Hanya diperhitungkan pada jalan menanjak, menurun dan datar (jalan raya yang biasanya digunakan untuk balap sepeda), tidak pada jalan yang bergelombang.
4. Tidak membahas power supply.
5. Sebagai sensor kemiringan digunakan potensiometer yang bukan jenis wirewound.

1.5. Metodologi Penulisan

1. Studi literatur.

   Melakukan kajian dari buku, data sheet, serta bahan yang diperoleh dari internet.

2. Perancangan tiap-tiap blok rangkaian.

   Perancangan alat yang dibuat dengan jalan membuat tiap-tiap blok dari rangkaian kemudian menggabungkannya menjadi satu rangkaian alat yang dirancang.

3. Pengujian alat.

   Pengujian alat dilakukan per blok rangkaian dan keseluruhan rangkaian dari blok-blok yang telah digabungkan sehingga dapat diketahui kerja dari alat yang dibuat.

4. Analisa.

   Setelah dilakukan kalibrasi alat maka dapat dilakukan analisa dan kemudian menarik kesimpulan dari alat yang telah dibuat.

1.6. Sistematika Penulisan

Sistematika penulisan tugas akhir meliputi beberapa bab yaitu sebagai berikut:

- BAB 1 : PENDAHULUAN

  Berisi tentang latar belakang, rumusan masalah, batasan masalah, tujuan, metodologi, dan sistematika penulisan.

- BAB 2 : TEORI PENUNJANG

  Berisi tentang teori-teori yang menunjang perancangan alat serta membahas tentang Mikrokontroler AT89S51.

- BAB 3 : PERANCANGAN ALAT

  Bab ini membahas tentang blok diagram dan komponen-komponen elektronik yang digunakan dalam perancangan alat.

❖ BAB 4 : PENGUJIAN ALAT

Pada bab ini berisi tentang pengujian alat yang dibuat serta data-data hasil pengujian alat per blok dan keseluruhan sistem.

❖ BAB 5 : PENUTUP

Berisi tentang kesimpulan dan saran yang didapat oleh penulis setelah membuat dan melakukan pengujian terhadap alat yang dibuat.

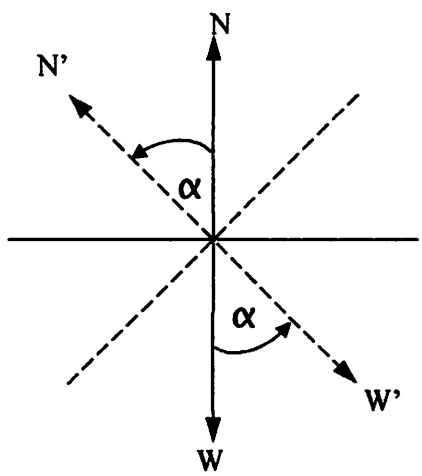
BAB II

LANDASAN TEORI

Landasan teori sangat membantu untuk dapat memahami suaatu sistem. Selain dari pada itu dapat juga dijadikan sebagai bahan acuan didalam merencanakan suatu sistem. Dengan pertimbangan hal-hal tersebut, maka landasan teori merupakan bagian yang harus dipahami untuk pembahasan selanjutnya.

2.1. Potensiometer

Pada pembuatan alat ini, digunakan potensiometer sebagai sensor kemiringan jalan yang dilalui oleh sepeda. Potensiometer berfungsi untuk mengubah perubahan nilai besaran sudut menjadi perubahan nilai besaran resistansi. Prinsip kerja dari sensor kemiringan jalan dapat dilihat pada gambar berikut:



Gambar 2-1

Prinsip Kerja Sensor Kemiringan

Bila W dimiringkan sebesar α, maka W' akan membentuk sudut yang besarnya sama dengan α terhadap bidang normalnya. Besarnya α akan terdeteksi sebagai perubahan sudut. Pergeseran ini juga akan memutar tuas potensio sebesar α. Perubahan nilai yang ditunjukkan oleh potensio merupakan perubahan dari besarnya α dalam satuan Ohm.

Potensiometer atau variable resistor adalah tranducer yang mengubah posisi mekanik menjadi elektrikal signal. Pada pembuatan skripsi ini, potensio berfungsi untuk mengubah perubahan besaran sudut yang terdeteksi menjadi besaran resistansi.

Dengan cara memutar tuas potensio ke kanan atau ke kiri akan mengubah nilai resistansi dari potensio. Posisi putaran biasanya sampai 360^{o} atau bahkan sampai beberapa kali putaran 2, 5, ataupun 10 kali putaran.

Output dari potensio akan berubah-ubah sesuai dengan perubahan dari sudut yang terjadi dan ini berarti adalah konversi dari posisi menjadi suatu besaran resistansi. Pada dasarnya suatu presisi dari potensio terdiri dari elemen resitif dengan angker yang dapat bergerak atau silinder yang dihubungkan dengan elemen. Sebagai angker yang berputar, variasi-variasi tahanan diantara dua yaitu akhir dari elemen tahanan dan silinder menunjukkan posisi sumbuh.

Kelebihan dari tranducer ini adalah memiliki efisiensi listrik yang sangat baik dan dapat memberikan suatu keluaran yang cukup untuk memperbolehkan suatu operasi pengontrolan. Disamping itu jenis tranducer ini bisa mendapatkan input tegangan dari AC maupun DC, sehingga dapat melayani cakupan pemakaian yang cukup luas. Sedangkan kelemahan dari tranducer ini memiliki umur pemakaian yang terbatas dan cepat menjadi derau sebagai akibat dari gesekan mekanis.

2.2. Operasional Amplifier (Op-Amp)

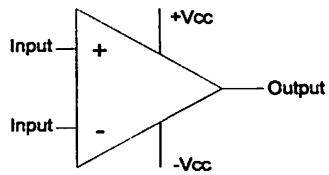
2.2.1. Sekilas tentang Op-Amp

Operasional amplifier adalah penguat gain tinggi yang dirancang untuk melaksanakan tugas-tugas matematis seperti penjumlahan, pengurangan, perkalian dan pembagian. Pada saat ini Op-Amp rangkaian terpadu linier dapat bekerja dengan tegangan yang rendah dan dengan hasil yang tidak kalah baiknya dengan para pendahulunya. Dengan harga yang relatif murah da mudah di ganti-ganti serta sifatnya yang dapat diandalkan, maka tidak heran kalau setiap tahunnya berjuta-juta Op-Amp dipergunakan. Dari kelebihan yang dimiliki oleh Op-Amp telah memperluas penggunaan Op-Amp sampai jauh melampaui kegunaannya saat pertama dirancang. Beberapa penggunaan Op-Amp adalah dibidang pengendalian proses, komunikasi, computer, sumber daya dan isyarat, system peraga dan system pengukuran atau sistem pengujian.

Pemakaian penguat operasional adalah untuk memperkuat sinyal dari tranduser (sensor) tanpa mempengaruhi ketelitian sensor, sebab impedansi inputnya sangat tinggi sehingga dapat dianggap tidak menyerap arus pada masukannya.

Penguat operasioanal dapat dibuat dengan menggunakan Op-Amp. Mutu penguat ini tergantung dari mutu Op-Amp yang dipergunakan. Selain itu ketepatan penguatan Op-Amp dipengaruhi ketepatan dan mutu komponen pendukung yang digunakan.

Penguat Operasional (Op-Amp) adalah penguat DC dengan penguatan tinggi yang dapat dipakai dari 0 sampai 1 MHz. Apabila Op-Amp ini ditambah dengan rangkaian umpan balik (*feedback*) yang sesuai, maka dapat digunakan untuk bermacam-macam aplikasi seperti penguat sinyal AC maupun DC, filter aktif, osilator, dan lain-lain.



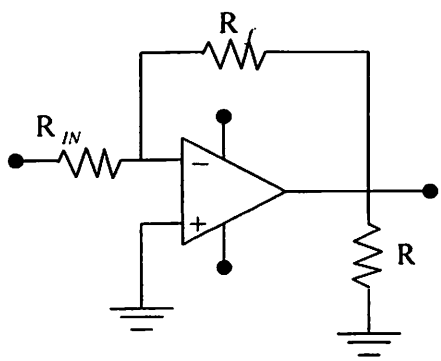
Gambar 2-2

Bentuk Umum Operasional Amplifier (Op-Amp)

Pada gambar Op-Amp menunjukkan bahwa Op-Amp mempunyai dua input yang berfungsi sebagai masukan pembalik dan masukan tak membalik.

2.2.2. Penguat Pembalik (Inverting)

Sebuah penguat menerima arus atau tegangan kecil pada masukannya dan membangkitkan arus atau tegangan yang lebih besar pada ukurannya. Penguat amplifier memiliki gain yang relatif linier, keluaran dikendalikan sebagai fungsi dari pada masukan penguat pembalik Op-Amp memperlihatkan pada gambar dibawah ini:



Gambar 2-3

Penguat Pembalik (Inverting)

Penguatan tegangan rangkaian ditentukan menurut :

$$Av = \frac{Vout}{Vin}$$

Sementara factor penguatan dalam modus tertutup untuk penguat pembalik dinyatakan dalam :

$$Av = \frac{Rf}{R_{IN}}$$

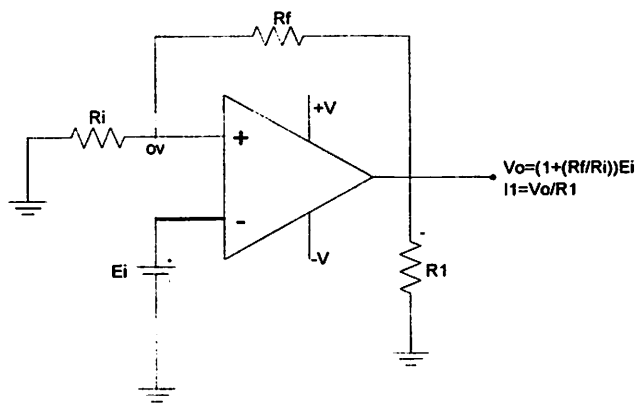
Sedangkan untuk tegangan keluaran diperoleh dengan jalan mengalikan tegangan yang diketahui dengan factor tegangan.

2.2.3. Penguat Tak Membalik (*Non inverting*)

Pada dasarnya semua Op-Amp yang dipakai dalam rangkaian penguat mempunyai prinsip kerja yang sama yaitu menguatkan sinyal masukkan. Tetapi untuk rangkaian penguat *non inverting* adalah kebalikan dari penguat inverting. Yaitu tegangan keluaran Vo mempunyai polaritas yang sama dengan tegangan masukan Ei. Untuk mencari tegangan outputnya kita dapat gunakan rumus:

$$Vo = \left(1 + \frac{Rf}{Rl}\right). Ei$$

Berdasarkan rumus diatas, maka pada pemakaian rangkaian penguat non inverting polaritas dari masukan dan keluaran adalah sama. Jadi apabila masukan kita beri tegangan positif maka keluaran akan berupa tegangan positif begitu juga sebaliknya.



Gambar 2-4

Op-Amp *Non Inverting* dengan Tegangan Input Positif

2.3. ADC (*Analog To Digital Converter*) 0804

Untuk dapat mengukur atau mengolah suatu besaran fisis yang umumnya bersifat analog dengan perangkat digital, maka besaran analog tersebut harus diubah dahulu menjadi besaran digital yang nilainya proposional dengan besaran analognya. Suatu perangkat yang bertugas melakukan hal tersebut dinamakan ADC (*Analog to Digital Converter*). ADC mempunyai kelebihan diantaranya adalah:

a. Mudah menginterfacekannya dengan mikroprosesor atau bekerja sendiri.

b. Bekerja dengan 2,5V tegangan referensi.

c. Tegangan input analog 0-5V dengan single tegangan.

d. Dikemas dalam bentuk single Chip DIP 20 pin, sehingga bentuknya kecil.

ADC dalam interfacing berfungsi sebagai pengubah sinyal listrik analog (kontinyu) menjadi sinyal digital, yang mewakili oleh susunan bit-bit dengan kombinasi tertentu.

Spesifikasi penting lain selain ketelitian (akurasi) dan linieritas adalah waktu konversi (*convertion time*). Waktu konversi ADC adalah waktu yang diperlukan ADC untuk menghasilkan kode biner yang valid untuk tegangan masukan yang diberikan. Semakin pendek waktu konversi berarti kecepatan konversi semakin tinggi.

Pada pembuatan skripsi ini, digunakan ADC 0804. ADC 0804 merupakan ADC buatan National Semiconductor yang mempunyai resolusi 8 bit, berarti ADC ini memiliki 2^N kombinasi atau $2^8 = 256$. Kombinasi untuk mencari tegangan yang diwakili tiap bitnya adalah:

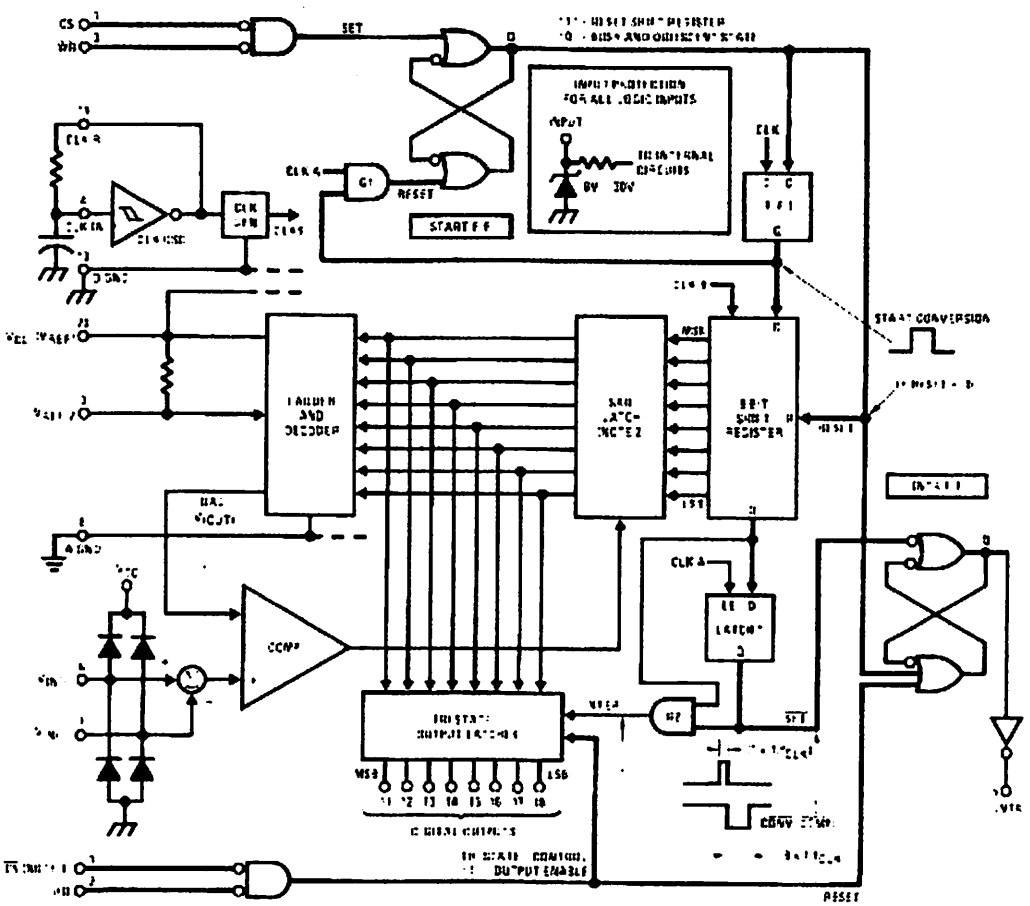
$$V_{bit} = \frac{V_{INMAX} - V_{INMIN}}{2^N} = \frac{5-0}{2^8} = \frac{5}{256} = 0{,}01953125 = 0{,}02V \text{ atau } 20mV$$

Dalam proses konversi ADC, perlu diperhatikan beberapa parameter yang akan menentukan mutu sebuah ADC, yaitu:

- Kesalahan kuantitatis
- Ketidaklinieran
- Kode tidak lengkap (hilang)
- Waktu konversi

Karakteristik yang linier didekati dengan karakteristik dalam bentuk anak tangga sehingga timbul kesalahan kuantitas sebesar setengah dari anak tangga. Karena tinggi anak tangga adalah sama dengan bit paling rendah *(least significant, LSB)* dalam bilangan biner, maka kesalahan tersebut sama dengan ½ LSB. Kadang-kadang kombinasi bit-bit tertentu tidak tersedia dengan perkataan lain buah tangga dilompati. Kombinasi semacam itu disebut kode yang hilang *(missing code)*. Kode hilang tidak akan terjadi bila kesalahan linieritas kurang dari ±½ LSB. Waktu yang dibutuhkan ADC untuk mengubah tegangan menjadi bit kombinasi disebut waktu konversi *(convertion time)*.

Gambar blok diagram dari ADC 0804 ini dapat dilihat pada gambar berikut 2-6. Untuk dapat menggunakan ADC 0804 tidak perlu mempelajari secara detail tentang fungsi dari masing-masing blok.



Gambar 2-5

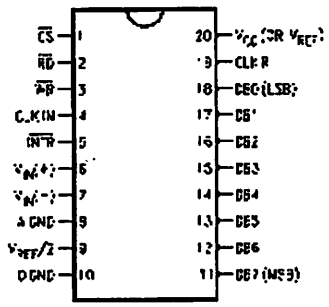
Diagram blok ADC 0804[1]

[1] *Sumber : www.national.com*

Tabel 2-1.

Label dan Fungsi Pin ADC 0804

Pin	Label	Status	Fungsi
1	CS	Masukan	Baris pilihan chip dari kendali PPI
2	RD	Masukan	Baris baca dari kendali PPI
3	WR	Masukan	Baris tulis dari kendali PPI
4	CLK IN	Masukan	Detak/pulsa
5	INTR	Keluaran	Baris inetrupsi menjadi masukan interupsi PPI
6	Vin(+)	Masukan	Tegangan analog (masukan +)
7	Vin(-)	Masukan	Tegangan analog (masukan -)
8	AGND	Daya	Pembulatan analog
9	Vref/2	Masukan	Referensi tegangan yang lain
10	DGND	Daya	Pembulatan digital
11	DB7	Keluaran	Keluaran dari LSB
12	DB6	Keluaran	Keluaran data
13	DB5	Keluaran	Keluaran data
14	DB4	Keluaran	Keluaran data
15	DB3	Keluaran	Keluaran data
16	DB2	Keluaran	Keluaran data
17	DB1	Keluaran	Keluaran data
18	DB0	Keluaran	Keluaran dari MSB
19	CLK R	Keluaran	Tahanan eksternal yang dihubungkan untuk detak
20	Vcc	Daya	Catu daya 5 volt



Gambar 2-6

Konfigurasi pin-pin ADC 0804

2.4. Limit Switch

Merupakan peralatan mekanis yang dapat dipergunakan untuk menentukan posisi fisik dari peralatan. Jenis saklar ini akan aktif bila suatu level melebihi batasan yang telah ditetapkan atau keluar dari jangkauan yang ditentukan.

Gambar 2-7

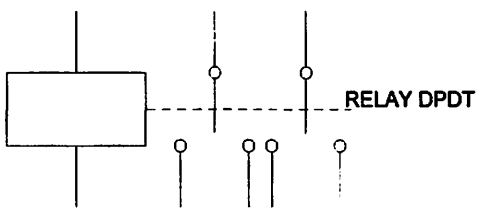
Simbol Limit Switch

2.5. Relay

Relay adalah komponen elektronika yang umumnya digunakan untuk menghidupkan rangkaian kontrol dan peralatan listrik lainnya yang menarik arus relatif kecil. Namun demikian relay dapat mengontrol tegangan dan arus yang lebih besar dengan menggunakan efek pengaturan. Efek pengaturan didapat dengan cara memanfaatkan tegangan kecil (5-24 V) untuk mengaktifkam koil dan relay. Kemudian koil tersebut diguanakan untuk mengubah-ubah posisi kontak. Kontak pada relay dapat digunakan untuk mensaklar

(*switching*) tegangan yang lebih besar sampai 400 Watt. Aliran arus yang digunakan untuk mengatur koil relay terpisah dari arus listrik yang dikontrrol oleh kontak-kontak pada relay tersebut.

Berikut ini merupakan gambar dari relay:



Gambar 2-8
Simbol Relay DPDT

Pada dasarnya relay dapat dikatakan sebagai kontak beban elektrik yang mengontrol suatu rangkaian elektrik dengan cara membuka dan menutup kontak pada rangkaian lain. Apabila kontak relay adalah *Normaly Open* (NO), maka akan terbuka bila relay tidak dialiri energi listrik. Sebaliknya, pada titik kontak relay yang tergolong *Normaly Close* (NC), akan tertutup bila relay tidak dialiri arus listrik. Pada kedua kondisi tersebut kontak-kontak pada relay akan berubah keadaannya apabila relay sialiri arus listrik.

Ada beberapa jenis susunan kontak relay dimana semuanya terisolasi terhadap arus listrik yang ada didalam kumparan. Jenis susunan kontak sebagai berikut:

- *Normaly Open* (normal terbuka)

  Yaitu kontak-kontak tertutup pada saat kumparan relay dialiri listrik.

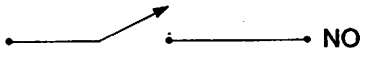
- *Normaly Close* (normal tertutup)

  Yaitu kontak-kontak terbuka pada saat kumparan relay dialiri listrik.

Macam-macam relay:

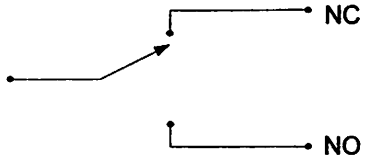
1. SPST (*Single Pin Single Terminal*)

   Simbol Relay SPST



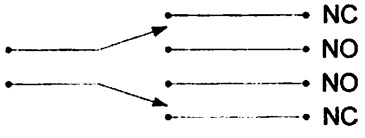
2. SPDT (*Single Pin Dual Terminal*)

   Simbol Relay SPDT



3. DPDT (*Dual Pin Dual Terminal*)

   Simbol Relay DPDT



Sedangkan jenis relay yang dipakai dalam perencanaan dan pembuatan alat pada tugas akhir ini adalah relay jenis DPDT.

2.6. Motor Arus Searah (Motor DC)

Motor adalah komponen yang terdiri dari lilitan/spoel dan magnet permanen, yang mana dia akan bergerak bila dialiri arus padanya. Jadi motor merupakan perangkat elektronik yang berfungsi untuk mengubah energi listrik menjadi energi mekanik/gerak.

Prinsip kerja motor didasarkan pada induksi elektromagnetik dan momen kopel. Adapun bagian dari motor listrik adalah sebagai berikut :

1) Bagian yang tetap atau disebut *stator.*

   Stator terdiri dari bahan magnet permanen artinya memiliki gaya magnet tetap.

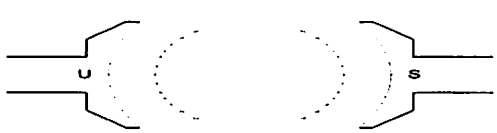
2) Bagian yang berputar atau disebut *rotor.*

Bagian ini merupakan coil/lilitan dimana arus listrik mengalir. Dengan mengalirkan arus listrik, maka menimbulkan medan listrik di sekitar lilitan.

Pada motor DC ini, jika bagian penghantar yang membawa arus searah ditempatkan dalam suatu medan magnet, maka penghantar tersebut akan menghasilkan medan magnet. Bila medan magnet yang dihasilkan sama dengan medan magnet permanennya, maka akan terjadi gaya tolak-menolak diantaranya dan rotor akan berputar. Kejadian ini akan terus berulang selama ada arus yang mengalir sehingga menghasilkan kecepatan putaran motor.

Prinsip kerja dari motor DC ditunjukkan berikut ini :

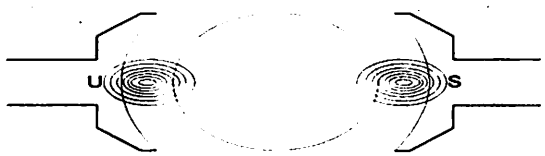
1) Pada gambar 2-9 ditunjukkan garis-garis gaya medan magnet (fluks) yang dihasilkan oleh kutub-kutub magnet permanen dan bagian ini disebut stator.



Gambar 2-9

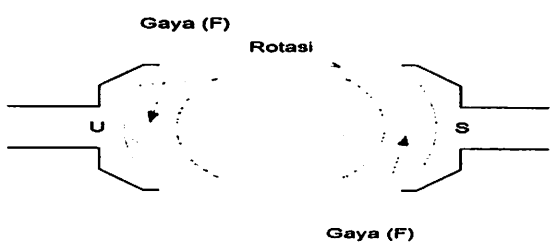
Medan Yang Dihasilkan Oleh Medan Magnet Permanen

2) Gambar 2-10 menunjukkan penghantar yang dialiri arus, maka pada bagian ini timbul medan magnet (garis-garis gaya/fluks) yang kemudian disebut rotor.



Gambar 2-10
Medan Yang Dihasilkan Oleh Arus Listrik Yang Mengalir Pada Penghantar

3) Interaksi kedua medan dari gambar 2-9 dan 2-10 akan menimbulkan medan yang tidak seragam seperti terlihat pada gambar 2-11 sehingga timbul gaya dan gaya tersebut akan menghasilkan torsi yang akan memutar jangkar.



Gambar 2-11
Interaksi Kedua Medan Magnet Menghasilkan Gaya

Arah dan garis-garis gaya (fluks) medan magnet yang dihasilkan oleh kutub ialah sebanding dengan arah arus yang dihasilkan pada penghantar dan arah dari gaya, saling tegak lurus serta menurut Hukum Tangan Kiri Fleming.

2.7. Mikrokontroller AT89S51

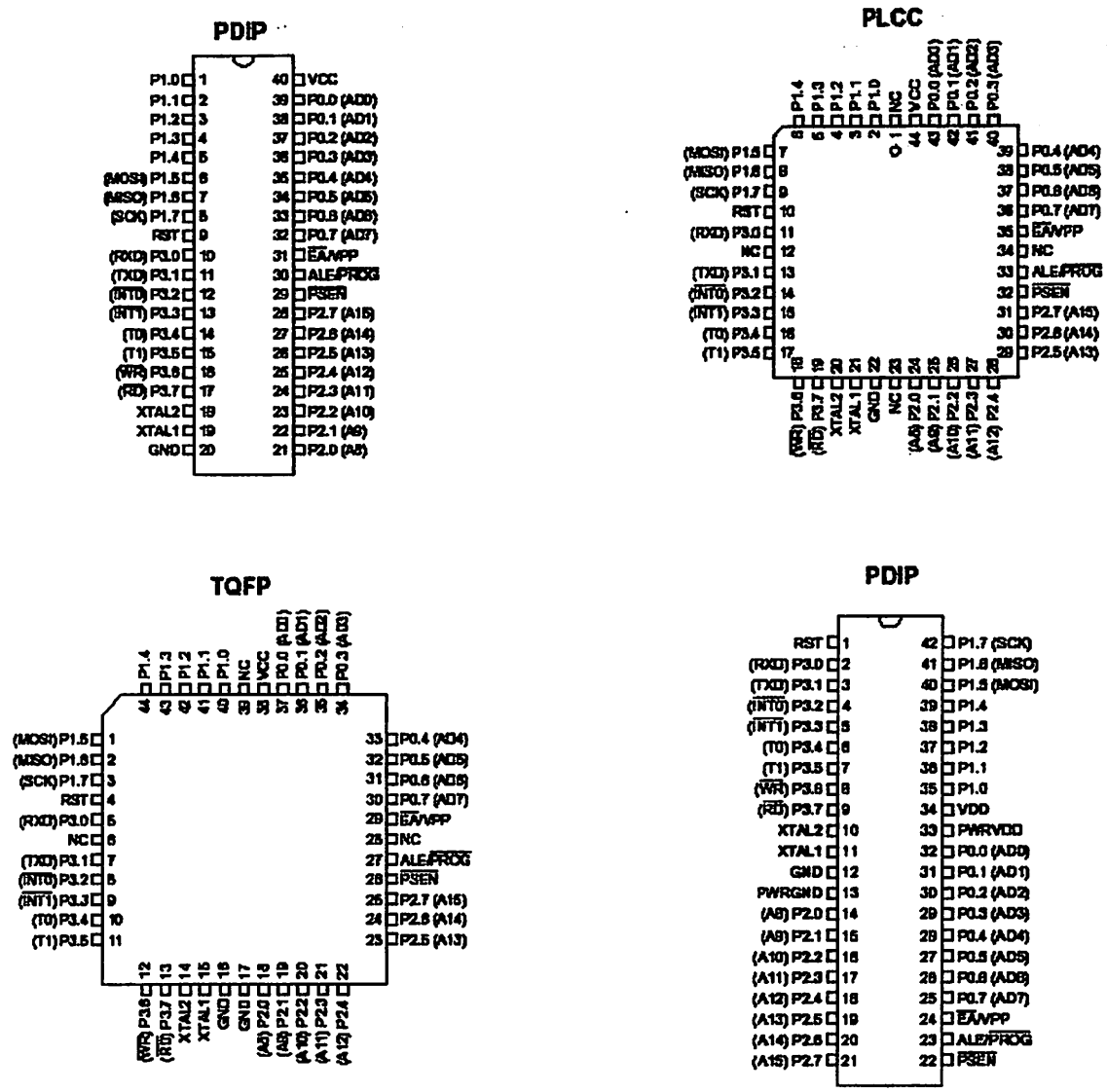
Mikrokontroller AT89S51 merupakan pengembangan dari mikrokontroller standart MCS-51. Karena merupakan pengembangan maka terdapat beberapa fitur tambahan yang tidak terdapat pada mikrokontroller MCS-51, maka mikrokontroller dapat menggantikan mikrokontroller MCS-51, tetapi tidak berlaku sebaliknya.

2.7.1. Struktur Mikrokontroller MCS-51

Fitur – fitur yang dimiliki oleh mikrokontroller AT89S51 adalah sebagai berikut:

a. kompatibel dengan mikrokontroller MCS-51.
b. 4K byte Downloable Flash Memory.
c. 2K byte EEPROM.
d. 3 level program memory lock
e. 128 byte RAM internal
f. 32 I/O yang dapat dipakai semua
g. 2 buah Timer/Counter 16 bit
h. Tegangan operasi 4.0 Volt sampai 5.0 Volt
i. Frekuensi kerja 0 Hz sampai 33 Mhz
j. Dual Data Pointer
k. Programmable Watchdog Timer

Konfigurasi kaki-kaki pin Mikrokontroller AT89S51

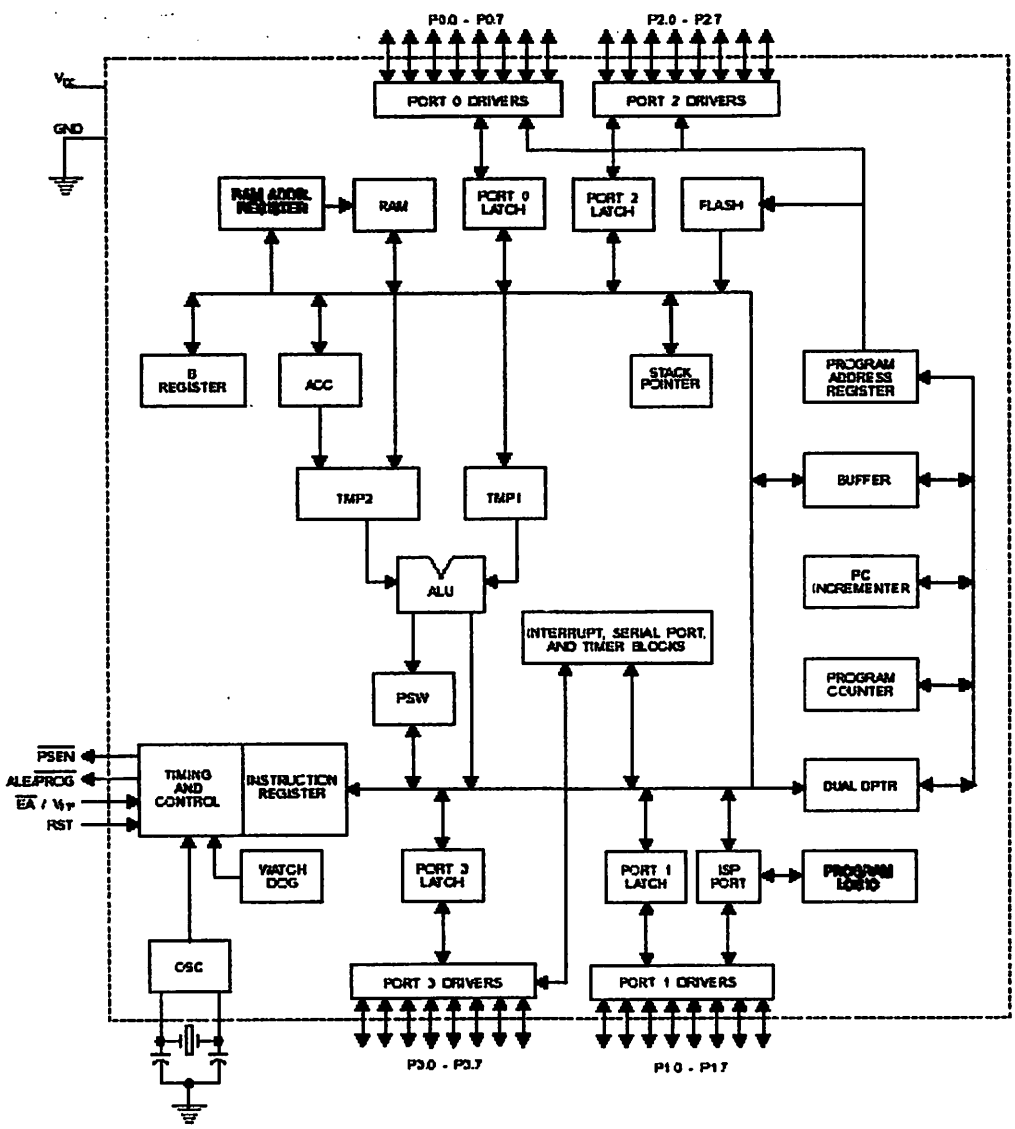


Gambar 2-12

Konfigurasi Kaki – kaki Pin Mikrokontroller AT89S51[2]

[2]*Sumber : www.atmel.com*

Blok Diagram Mikrokontroller AT89S51

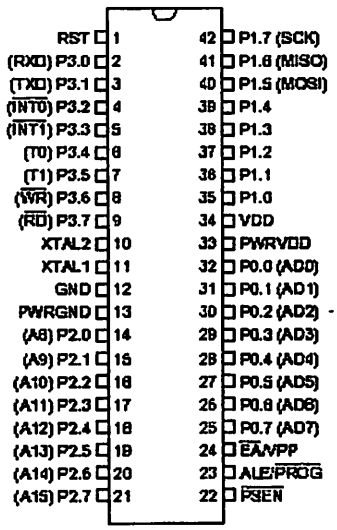


Gambar 2-13

Blok Diagram Mikrokontroller AT89S51[3]

[3]*Sumber : www.atmel.com*

PDIP



Gambar 2-14

Mikrokontroller AT89S51

Semua pin pada Mikrokontroller AT89S51 adalah sama dengan Mikrokontroller MCS-51, namun pada port 1 Mikrokontroller AT89S51 terdapat fungsi khusus yang tidak terdapat pada Mikrokontroller MCS-51.

Adapun fungsi khusus tersebut adalah :

Port Pin	**Fungsi Khusus**
P1.5	MOSI (Master data output, Slave data input untuk kanal SPI)
P1.6	MISO (Master clock input, Slave data input untuk kanal SPI)
P1.7	SCK (Master clock output, Slave clock input untuk kanal SPI)

Selain fungsi khusus diatas, juga mempunyai tambahan yang lain yaitu SFR (Special Function Register) yaitu fungsi register yang mengontrol alat tambahan pada Mikrokontroller AT89S51.

Tambahan SFR ini meliputi:

- TCON : Timer Register dengan alamat 88H
- TMOD : Timer Mode dengan alamat 89H

2.7.2. Register Utama

Mikrokontroller keluarga 8031 mempunyai banyak register yang meliputi Akumulator, register R, register B, Data Pointer (DPTR), Program Counter (PC), dan Stack Pointer (SP).

2.7.2.1. Akumulator

Digunakan sebagai register umum untuk mengakumulasi atau mengumpulkan hasil dari instruksi – instruksi. Daya atau kapasitas tampung sebesar 8 bit (1 *Byte*) data serta merupakan register yang paling sering dipakai. Keluarga 8031 hampir setengahnya menggunakan akumulator sebagai penyimpan instruksi baik dalam hal perhitungan ataupun instruksi yang lainnya.

2.7.2.2. Register R

Register R merupakan delapan set register yang dinamakan R0, R1, R2, R3, R4, R5, R6 dan R7. Adapun fungsi dari register – register ini adalah sebagai register yang membantu penyimpanan data yang menggunakan banyak operasi. Register – register ini membantu akumulator dalam melakukan operasi antara dua operan.

2.7.2.3. Register B

Fungsi dari register B adalah sama dengan akumulator yaitu menyimpan sebuah harga 1 Byte, dan hanya digunakan dalam dua interuksi keluarga 8031, yaitu MUL AB dan DIV AB. Karenanya apabila diperlukan untuk mengalikan atau membagi akumulator A dengan suatu harga yang lain maka dapat dilakukan dengan menyimpan harga tersebut kedalam register B kemudian menjalankan instruksinya.

2.7.2.4. DPTR (Data Pointer)

Merupakan satu – satunya register yang dapat diakses sebanyak 2 Byte di dalam keluarga Mikrokontroller 8031, digunakan untuk merujuk pada lokasi suatu data. DPTR digunakan oleh beberapa perintah untuk mengakses memori *eksternal.* Apabila AT89S51 mengakses memori ekternal dengan merujuk alamat yang ditunjukkan DPTR.

2.7.2.5. PC (*Program Counter*)

PC merupakan alamat 2 Byte yang menginstruksikan 89S51 alamat instruksi yang selanjutnya akan dilaksanakan. Saat inisialisasi 89S51, PC tersisi dengan `00000h` dan akan bertambah satu setiap kali instruksi telah dilaksanakan. Harga PC tidak dapat langsung dirubah dengan menggunakan perintah `MOV PC, 2430h`, namun dengan perintah `LJMP 2340h` akan mengisi PC dengan `2340h`.

2.7.2.6. SP (*Stack Pointer*)

Digunakan untuk menunjukkan dimana harga berikutnya yang akan diambil dari *stack.* Daya tampung dari SP sebesar 1 Byte data. Apabila suatu harga dimasukkan ke dalam *stack*, 89S51 akan pertama – pertama menambah harga SP kemudian akan menyimpan kedalam memori yang bersesuaian. Demikian juga apabila harga diambil dari *stack*, maka 89S51 akam mengambil data dari stack kemudian akan mengurang harga *stack.*

2.7.3. Mode Pengalamatan

Mode Pengalamatan menunjuk pada bagaimana pemrogram yang akan mengalamatkan suatu alamat suatu lokasi memori. Mode Pengalamatan memberikan akan

suatu kemudahan khusus yang sangat penting. Mode Pengalamatan ini meliputi *immediate addressing, direct addressing* dan *indirect addressing.*

2.7.3.1. *Immediate Addressing*

Immediate addressing adalah mode pengalamatan yang sangat umun digunakan mengingat harga yang akan disimpan dalam memori langsung mengikuti kode operasi dalam memori, sehingga tidak memerlukan pengambilan harga dari alamat lain untuk disimpan.

Misalnya: `MOV A#20h`

Pada instruksi diatas, akumulator akan diisi dengan harga yang langsung mengikutinya, dalam hal ini `20h`. mode ini sangat cepat mengingat harga yang dipakai langsung tersedia.

2.7.3.2. *Direct Addressing*

Pada mode ini harga yang akan dipakai diambil langsung dalam alamat memori lain. Mode pengalamatan ini sangat cepat, meskipun harga yang didapat tidak langsung seperti *immediate,* namun cukup cepat karena disimpan dalam RAM internal. Demikian pula akan mudah menggunakan mode ini daripada mode *i*mmediate karena harga yang didapat bisa dari lokasi memori yang mungkin variabel.

Misalnya: `MOV A,30h`

Instruksi diatas akan dibaca data dari RAM internal dengan alamat `30h`, yang selanjutnya disimpan dalam akumulator.

2.7.3.3. *Indirect Addressing*

Mode pengalamatan *indirect addressing* sangat berguna karena dapat memberikan fleksibelitas tinggi dalam mengalamati suatu harga. Mode ini merupakan satu – satunya cara untuk mengakses 128 Byte lebih dari RAM internal pada keluarga 8052.

Misalnya: `MOV A@R0`

Pada instruksi ini 89S51 akan mengambil harga yang berada pada alamat memori yang ditunjukkan oleh isi dari `R0` dan kemudian mengisikannya pada akumulator.

Mode pengalamatan ini selalu merujuk pada RAM internal dan tidak pernah merujuk pada SFR, oleh karena itu menggunakan mode ini untuk mengalamati alamat lebih dari 7Fh hanya digunakan untuk keluarga 8052 yang memiliki 256 Byte spasi RAM internal.

Mode pengalamatan memori eksternal menggunakan mode ini dan terdiri atas dua bagian. Bagian yang pertama digunakan untuk mengakses memori eksternal, dimana alamatnya terdapat di dalam DPTR16 bit.

Misalnya: `MOVX A,@DPTR` atau `MOVX @DPTR,A`

Kedua bagian mengakses almat memori eksternal secara 8 bit, dimana alamat dari harga yang akan diambil terdapat didalam register R.

Misalnya: `MOVX @R0,A.`

Didalam instruksi tersebut, alamat yang terdapat didalam register `R0` dibaca terlebih dahulu dan kemudian harga akumulator ditulis dengan harga yang terdapat pada alamat memori eksternal yang didapat. Karena register `R0` hanya dapat menampung alamat dari `00h` hingga `FFh`, maka penggunaan mode pengalamatan eksternal 8 bit ini hanya terbatas pada 256 *Byte* dari memori eksternal.

2.7.4. Interupsi

Interupsi merupakan suatu kejadian yang akan menghentikan sementara jalan program saat itu. Dengan interupsi, suatu alur program dapat dihentikan sementara untuk menjalankan suatu subrutin, dan kemudian melanjutkan aliran program secara normal seperti tidak pernah ada interupsi. Subrutin ini yang disebut dengan interrupt handler, dan hanya dijalankan jika terjadi suatu kejadian (*event*) khusus. Kejadian ini bisa berupa timer yang mengalami *overflow*, penerimaan karakter melalui port serial, mengirimkan karakter melalui port serial, atau salah satu dari dua kejadian eksternal. Mikrokontroller 89S51 bisa dikonfigurasi untuk menangani interupsi yang disebabkan oleh salah satu dari kejadian.

Dengan interupsi ini, dapat dengan mudah dimonitor kejadian – kejadian yang diinginkan. Tanpa adanya interupsi maka proses monitor ini dilakukan dengan manual melalui pengecekan berulang. Proses pengecekan manual ini akan membuar program menjadi lebih panjang dan lebih rumit.

Tabel 2-2

Daftar Alamat Rutin Interupsi

Interupsi	Flag	Alamat Rutin
Ekternal 0	IF 0	0003h
Timer 0	TF 0	000Bh
Eksternal 1	IF 1	0013h
Timer 1	RF 1	001Bh
Serial	R1/T1	0023h

Dengan demikian, maka perlu dibedakan interupsi yang terjadi karena kejadian-kejadian yang berbeda. Hal ini bisa diwujudkan dengan adanya alamat yang pasti bagi

sebuah rutin interupsi untuk masing-masing interupsi. Dari data diatas dapat dikatakan jika TIMER0 mengalami *overflow* (bit TF0 logika 1), maka program utama akan ditunda sementara dan kontrol program akan melompat ke alamat 0003h.

2.7.4.1. Setting Interupsi

Pada saat pertama dihidupkan (*power on*), maka semua interupsi akan dimatikan. Meskipun bit TF0 diset (interupsi timer 0 diaktifkan), mikrokontroller 89S51 tidak akan menjalankan interupsi. Sebuah program harus dibuat dan dijalankan untuk mengaktifkan dan mengkhususkan untuk interupsi yang diinginkan. Hal ini dapar dilakukan dengan konfigurasi SFR IE (*Interrupt Enable*) yang berda di alamat A8h. Adapun konfigurasi bit–bit yang mengatur enable dari konfigurasi interupsi tercantum pada tabel dibawah ini:

Table 2-3

Konfigurasi Bit – bit SFR IE

Bit	Nama	Alamat	Fungsi
7	EA	Afh	Global enable/disable interupsi
6	-	Aeh	Tidak didefinisikan
5	-	ADh	Tidak didefinisikan
4	ES	Ach	Enable interupsi serial
3	ET1	Abh	Enable interupsi timer 1
2	EX1	Aah	Enable interupsi eksternal 1
1	ET0	A9h	Enable interupsi timer 0
0	EX0	A8h	Enable interupsi eksternal 0

Sebelum semua interupsi dijalankan, bit 7 dari SFR harus diset terlebih dahulu. Global *enable/disable* interupsi ini menyebabkan semua interupsi enable ataupun disable. Jika bit 7 IE ini dinolkan, tidak akan ada satu interupsi pun yang terjadi. Prosedur yang benar adalah dengan mengeset jenis interupsi yang diinginkan dan kemudian mengeset bit 7 IE, barulah interupsi akan berjalan dengan baik.

2.7.4.2. Prioritas Interupsi

Prioritas interupsi yang dimiliki mikrokontroller AT89S51 ada dua macam, yaitu prioritas tinggi dan prioritas rendah. Maka dapat ditentukan priotidas interupsi yang akan dikerjakan terlebih dahulu daripada interupsi – interupsi yang lainnya yang bekerja bersamaan pada saat itu. Sebagai contoh, interupsi timer 1 diaktifkan untuk secara otomatis memanggil sebuah rutin saat timer 1 mengalami kondisi *overflow*. Disamping itu, interupsi serial juga diaktifkan untuk memanggil suatu rutin saat ada sebuah karakter diterima dalam port serial. Dalam hal ini diinginkan penerimaan karakter dari port seria lebih penting dripada interusi timer. Jadi seandainya interupsi timer 1 sedang bekerja dan terjadi penerimaan karakter, maka rutin interupsi timer 1 tersebut akan diinterupsikan oleh interupsi port serial dan akan ditunda sementara untuk mengerjakan rutin interupsi port serial ini. Setelah pengerjaan rutin interupsi serial selesai, maka control program akan kembali ke rutin interupsi timer 1. Yang dikerjakan disini adalah mengeset prioritas interupsi serial lebih tinggi dahulu daripada prioritas interupsi timer. Propritas interupsi ini dikontrol oleh SFR IO dengan alamat B8h yang memiliki konfigurasi bit – bit sebagaimana tercantum dalam tabel dibawah ini:

Tabel 2-3

Konfigurasi Bit – bit SFR IP

Bit	Nama	Alamat	Fungsi
7	-	-	Tidak terdefinisi
6	-	-	Tidak terdefinisi
5	-	-	Tidak terdefinisi
4	PS	BC	Prioritas interupsi serial
3	PT 1	BB	Prioritas interupsi timer 1
2	PX 1	BA	Prioritas interupsi eksternal 1
1	PT 0	B9	Prioritas interupsi timer 0
0	PX 0	B8	Prioritas interupsi eksternal 0

Pemakaian perioritas interupsi di atas mempunyai beberapa peraturan yang tercantum di bawah ini:

1. Interupsi yang lebih tinggi boleh menginterupsi interupsi yang lebih rendah.
2. Interupsi prioritas rendah boleh terjadi jika tidak ada interupsi yang sedang dijalankan.
3. Tidak ada interupsi yang menginterupsi interupsi yang lebih tinggi.

Jika dua interupsi terjadi pada waktu yang bersamaan, maka prioritas instruksi yang lebih tinggi akan dikerjakan terlebih dahulu. Apabila keduanya mempunyai prioritas yang sama, maka interupsi yang mempunyai polling akan dikerjakan terlebih dahulu.

Mikrokontroller AT89S51 secara otomatis akan menguji apakah sebuah interupsi visa terjadi setelah setiap instruksi dikerjakan. Pengecekan ini mengikuti suatu alur yang disebut dengan *Polling Sequence* dengan urutan:

1. Interupsi Eksternal 0
2. Interupsi Timer 0
3. Interupsi eksternal 1
4. Interupsi Timer 1
5. Interupsi Seris

Hal ini berarti jika sebuah interupsi serial terjadi pada waktu yang bersamaan dengan interupsi eksternal 0, maka intrupsi eksternal 0 akan dikerjakan terlebih dahulu, dan interupsi serial akan dikerjakan setelah interupsi external 0 selesai dilakukan.

2.7.5. Timer

Mikrokontroller AT89S51 mempunyai dua timer, keduanya bisa dikontrol, set baca dan konfigurasisecara sendiri-sendiri. Timer 89S51 mempunyai tiga fungsi umum, yaitu:

1. Dapat menghitung waktu antara dua kejadin (*event*).
2. Dapat menghitung sendiri jumlah kejadian.
3. Dapat membangkitkan *baud rate* untuk port serial

Sebuah *timer* akan bekerja dengan mecacah (*trigger*), tidak tergantung fungsinya sebagai timer, *counter* ataupun generator baud rate, yang oleh mikrokontroller akan ditambahkan satu pada timer tersebut.

2.7.5.1. Timer sebagai Setting Waktu

Fungsi utama sebuah timer adalah untuk mengukur waktu, dimana saat timer digunakan akan bertambah satu untuk satu siklus mesin. Setiap siklus mesin membutuhkan 12 pulsa kristal. Maka, apabila mikrokontroller AT89S51 dengan kristal 11,059 MHz, setiap detiknya akan berharga:

$$\frac{11.059000}{12} = 921.583 \ \ pencacahan\ per\ \text{sec}$$

Artinya : terdapat 921.583 kali pencacahan dalam setiap detiknya (second).

Dengan cara yang sama apabila diinginkan mendapatkan pewaktu 0,05 detik, maka dibutuhkan timer yang mencacah sampai:

$$921.583 x 0{,}05 = 46.079{,}05$$

Artinya: kita perlu memonitor cacahan dari timer hingga mencapai harga 46.079. hal ini sekalipun tidak presisi karena menghilangkan hitungan 0,15 dibelakang koma, namun cukup mendekati dan masih bisa ditolelir.

2.7.5.2. Timer SFR

Mikrokontroller 89S51 mempunyai dua buah timer yaitu TIMER 0 dan TIMER 1. yang kedua timer berbagi dua macam SFR, yaitu TMOD dan TCON,yang mengontrol timer, masing – masing timer mempunyai dua macam SFR yaitu TH0/TL0 untuk TIMER 0 dan TH1/TL1 untuk TIMER 1. Berikut ini adalah tabel SFR untuk TIMER.

Tabel 2-5

Daftar SFR untuk Timer

Nama SFR	Keterangan	Alamat
TH0	Timer 0 High Byte	8Ch
TL0	Timer 0 LowByte	8Ah
TH1	Timer 1 High Byte	8Dh
TL1	Timer 1 Low Byte	8Bh
TCON	Timer Kontrol	88h
TMOD	Timer Mode	89h

Timer 0 memiliki dua mcam SFR yang eksklusif bagi dirinya, yaitu TH0 dan TL0 yang membentuk harga actual dari timer.

Timer 1 memiliki persamaan yang identik dengan Timer 0, yang membedakan adalah SFR eksklusif yang dimilikinya yaituTH 1 dan TL1. dan karena kedua timer ini mempunyai kapasitas 2 Byte, maka harga maksimum yang bisa ditampung adalah 65.535. Apabila timer telah melampui harga 65.535 akan mereset atau *overflow* dan kemudian akan kembali ke harga awal yaitu 0.

2.7.5.3. SFR TMOD

SFR TMOD digunakan untuk mengontrol mode operasi dari kedua timer. Setiap bit dari SFR ini menyediakan informasi bagi mikrokontroller untuk menjalankan timer. Empat bit orde tinggi (bit 4 hingga bit 7) berhubungan dengan TIMER 1, sedangkan empat bit orde bawah (bit 0 hingga bit 3) mempunyai fungsi sama yang diperuntukkan untuk TIMER 0.

Tabel 2-6

Daftar Bit SFR TMOD

Bit	Nama	Fungsi	Timer
7	GATE	Jika bit ini diset, timer akan bekerja jika INT1 (P3.3) berlogika 1. Jika bit ini dinolkan, timer akan bekerja tanpa dipengaruhi kondisi INT1.	1
6	C/T1	Jika bit ini diset, timer akan menghitung kondisi pada T1 (P3.5). Jika bit ini dinolkan, timer akan bertambah satu setiap siklus mesin.	1
5	T1M1	Bit mode timer	1
4	T1M0	Bit mode timer	1
3	GATE0	Jika bit in diset, timer hanya akan bekerja jika INT0 (P3.2) berlogika 1. jika bir ini dinolkan, timer akan bekerja, tanpa dipengaruhi kondisi INT0	0
2	C/T0	Jika bit ini diset, timer akan menghitung kondisi pada T0 (P3.4). Jika bit ini dinolkan, timer akan bertambah satu setiap siklus mesin.	0
1	T0M1	Bit mode timer	0
0	T0M0	Bit mode timer	0

2.7.5.4. Mode Timer 16 Bit (Mode 1)

Mode ini adalah timer 16 bit yang paling banyak digunakan, dimana fungsinya sama dengan timer 13 bit. Karena kemampuannya 16 bit, maka mode ini memiliki batas maksimum harga 65.535. Jadi jika timer diset dalam mode ini, akan menjadi nol setelah 65.535 siklus mesin.

2.7.5.5. Mode Timer 8-bit Auto Reload (Mode 2)

Mode ini adalah timer 8 bit dengan kemampuan pengisian ulang (*auto reload*), dimana THx akan menyimpan harga awal counter dan TLx berfungsi sebagai timer 8-bit. TLx akan mulai mencacah dengan harga yang tersimpan pada THx, dan jika telah melampaui harga 255, akan reset dan kembali ke harga awal yang tersimpan di THx.

Jika dimisalkan TH0 menyimpan harga FDh dan TL0 harga aktualnya FEh, maka untuk beberapa siklus mesin akan didapatkan urutan perubahan harga sebagai mana tercantum dalam tabel dibawah ini:

Tabel 2-7

Perubahan Harga TL0

Siklus Mesin	Harga TH0	Harga TL0
1	FDh	FEh
2	FDh	FFh
3	FDh	FDh
4	FDh	FEh
5	FDh	FFh
6	FDh	FDh
7	FDh	FEh

Seperti yang tercantum dalam tabel untuk harga dari TH0 tidak mengalami perubahan, sehingga dalam mode 2, THx sebagai variabel yang menentukan waktu sedangkan RTLx adalah timer yang selalu mencacah secara konstan setiap siklus mesin. TLx akan mengalami *overflow* dan reset ke harga yang tersipan dlam TH0. keuntungan yang didapatkan karena fleksibilitas penentuan tenggang waktu dengan mengatur harga pada THx.

2.7.5.6. Mode Timer Split / Pemecah (Mode 3)

Mode ini merupakan mode yang memecah / split. Apabila TIMER0 diset dalam mode 3, akan menjadi dua timer 8-bit yang berbeda. TIMER0 adalah TL0 dan TIMER1 adalah TH0. kedua-duanya akan mencacah dari dari 0 hingga 255 dan jika menemui kondisi *overflow* akan mereset ke nol. Saat TIMER0 dalam mode split, TIMER1 bisa diset pada mode 0,1 atau bahkan 2 secara normal. Mode ini hanya dipakai jika diperlukan dua timer 8 bit yang terpisah.

2.7.5.7. SFR TCON

Bagian ini mengontrol kedua timer dan menyediakan informasi yang sangat berguna berkaitan dengan timer-timer tersebut. Adapun struktur SFR TCON dapat dilihat pada tabel dibawah ini:

Tabel 2-8

Bit-bit SFR TCON

Bit	Nama	Alamat	Fungsi	Timer
7	TF1	8Fh	Timer 1 overflow.maka diset oleh mikrokontroller.	1
6	TR1	8Eh	Timer 1 RUN, jika diset akan bekerja. Dan jika direset timer 1 akan mati	1
5	TF0	8Dh	Timer 0 overflow.maka diset oleh mikrokontroller.	0
4	TR0	8Ch	Timer 0 RUN, jika diset akan bekerja. Dan jika direset timer 0 akan mati	0

Pada tabel diatas hanya dicantumkan 4-bit dari 8-bit yang ada pada SFR TCON. Hal ini karena hanya 4-bit (bit 4 hingga bit 7) yang berkaitan dengan timer dan bit sisanya

berkaitan dengan interupsi. Untuk mengeset atau mereset bit-bit SFR tidak perlu dengan memberikan nilai 8-bit, dimana bisa dialamati perbit yang tidak akan mengganggu status bit yang lainnnya.

2.7.5.8. Pembacaan Status Timer

Pembacaan status timer dapat dilakukan dengan dua cara yaitu dengan membaca harga aktual 16-bit dari timer, dan yang kedua dengan mendeteksi keadaan jika timer mengalami *overflow*. Jika timer yang digunakan adalah time 8-bit, maka pembacaan akan lebih mudah.

Apabila timer yang digunakan adalah mode 13-bit atau 16-bit, maka akan menjadi lebih rumit.

Sebagai contoh:

Harga aktual *low byte* adalah 255 dan pembacaan high byte adalah 15. seharusnya harga sebenarnya adalah high byte 14 dan *low byte* 255, karena saat membaca *low byte* sebesar 255, beberapa saat kemudian *high byte* akan bertambah satu, saat pembacaan menjadi meleset menjadi 256 hitungan, karena terletak pada *high byte*.

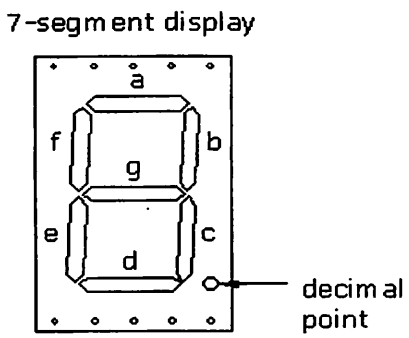
Solusinya adalah dengan membaca *high byte* terlebih dahulu dan kemudian membaca *low byte*, setelah itu *high byte* dibaca lagi dan kemudian dibandingkan dengan pembacaan semula, apabila ada perbedaan maka nilai yang dipakai adalah pembacaan *high byte* yang pertama.

Yang perlu diketahui adalah kapan saat timer reset menjadi nol, tidak perduli berapa harga aktual dari timer, melainkan kapan saat timer *overflow* dan kembali menjadi nol. Pada saat timer menjadi *overflow* maka secara otomatis mikrokontroller mengeset bit TFx dalam

register TCON. Dengan cara ini maka dapat dibuat program untuk menentukan jeda waktu yang jelas.

2.8. Display Seven Segment

Untuk tampilan posisi rantai dari Mikrpkontroller digunakan display *seven segment.* Seven segment terdiri dari tujuh buah LED utama yang dikemas dalam satu kemasan. Antara dua kaki yang oleh LED tersebut salah satu dari ketujuh kaki LED tersebut daling dihubungkan antara yang satu dengan yang lainnya atau lebih dikenal dengan *common.* Common pada seven segment ada dua macam, yaitu: common anoda dan common katoda, tergantung dari kaki yang mana yang saling dihubungkan ke ground.



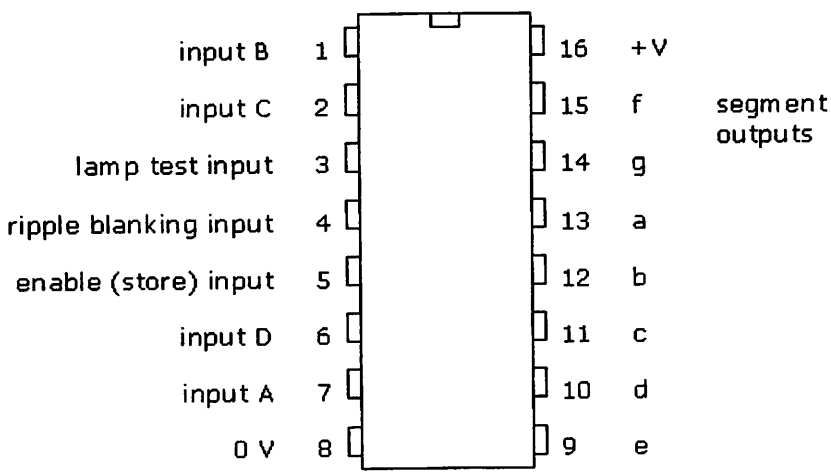
Gambar 2-15
Display seven segment

Seven segment dapat juga tersusun dari masing-masing segment berupa bilangan tipis yang dapat menyala. Jenis ini disebut peragaan pijar dan sama dengan lampu LED biasa. Penayang jenis lain adalah tabung gas, yang dapat beroperasi pada tegangan tinggi. Tabung ini memancarkan cahaya berwarna merah jingga bila beroperasi pada tegangan tinggi dan suatu peraga yang memancarkan warna hijau bila beroperasi pada tegangan rendah. Seven segment dapat menampilkan digit decimal, yaitu dari 0-9.

Jika seven segment digunakan untuk indicator multi digit, metode pergerakan yang paling efektif adalah system *multyflexing.* Walaupun LED-LED tersebut di drive oleh arus tinggi, tapi dilaksanakan secara bersamaan, sehingga mengurangi disipasi daya rata-rata. Clock display yang bekerja pada frekwensi 1 KHz atau lebih, menyebabkan display setiap seven segment dipilih secara bergantian dan disambungkan dengan data masukan yang tepat. Semua segmen yang sama dari setiap display dihubungkan dengan saluran bus bersama yang dihubungkan dengan IC decoder atau drive BCD to sevent segment.

2.9. Decoder 4511

Untuk mendukung sevent segment atau merubah kekurangan dari IC AT89S51 menjadi tampilan bilangan decimal diperlukan IC decoder. Disini IC secoder yang digunakan adalah IC decoder type 4511. IC 4511 ini mempunyai fungsi untuk mengubah data masukan biner menjadi data keluaran decimal. Pin-pin yang terdapat pada IC decoder type 4511 dapat dilihat pada gambar 2-16 dibawah ini.



Gambar 2-16

Pin Decoder 4511

Tabel 2-8 di bawah ini menunjukkan hasil konversi dari inputan bilangan biner pada IC decoder type 4511 dengan output pada seven segment berupa tampilan bilangan decimal.

Tabel 2-9

Decoder to 7 Segment

BCD inputs				*segment outputs*							*display*
D	*C*	*B*	*A*	*a*	*b*	*c*	*d*	*e*	*f*	*g*	
0	0	0	0	1	1	1	1	1	1	0	0
0	0	0	1	0	1	1	0	0	0	0	1
0	0	1	0	1	1	0	1	1	0	1	2
0	0	1	1	1	1	1	1	0	0	1	3
0	1	0	0	0	1	1	0	0	1	1	4
0	1	0	1	1	0	1	1	0	1	1	5
0	1	1	0	0	0	1	1	1	1	1	6
0	1	1	1	1	1	1	0	0	0	0	7
1	0	0	0	1	1	1	1	1	1	1	8
1	0	0	1	1	1	1	0	0	1	1	9

BAB III

PERANCANGAN SISTEM

3.1. Pendahuluan

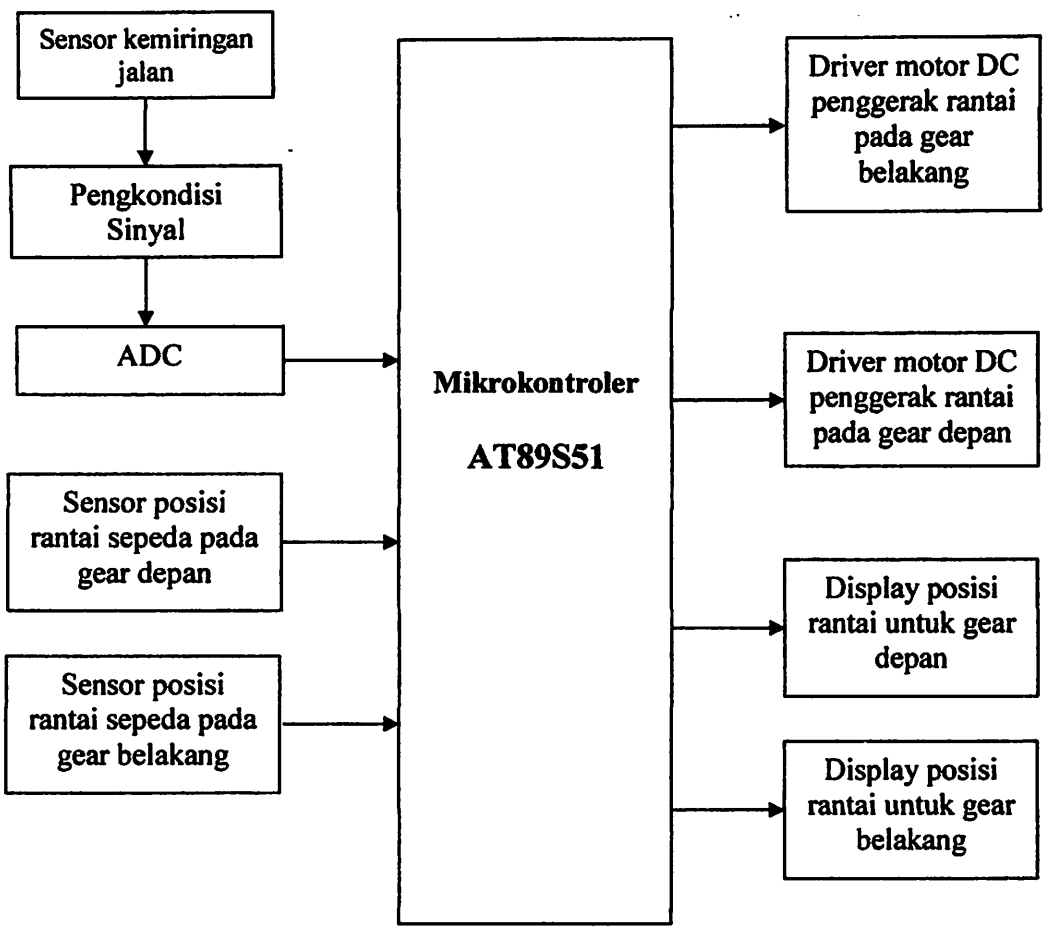
Pada dasarnya perencanaan alat yang dibuat dalam tugas akhir ini meliputi perencanaan perangkat keras dan perencanaan perangkat lunak. Komponen yang dipakai dalam peraencanaan ini antara lain : Mikrokontroller AT89S51 sebagai kontrol utama, dengan komponen pendukung meliputi: sensor kemiringan (potensiometer), ADC (Analog to Digital Converter), Op-amp, seven segment, limit switch dan driver motor dc.

3.2. Perancangan Perangkat Keras *(Hardware)*

3.2.1. Blok diagram

Adapun blok diagram dari model alat pemindah rantai pada sepeda balap ini adalah sebagai berikut :

Blok diagram



Gambar 3-1

. Blok Diagram

Dari blok diagram di atas dapat dijelaskan fungsinya adalah sebagai berikut

1. Sensor posisi kemiringan jalan berfungsi untuk mendeteksi kemiringan jalan yang dilalui.
2. Pengkondisi sinyal berfungsi untuk mengkondisikan dan memperkuat sinyal yang dihasilkan oleh sensor kemiringan agar dapat diubah oleh ADC.

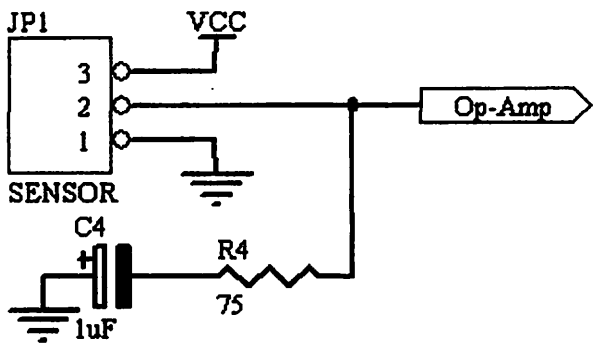
3. ADC berfungsi mengubah sinyal analog yang dihasilkan oleh sensor menjadi sinyal digital.
4. Sensor posisi rantai sepeda berfungsi untuk mendeteksi posisi rantai.
5. Driver motor DC berfungsi untuk menarik kawat seling pada waktu terjadi perpindahan posisi rantai sepeda.
6. Display seven segment berfungsi untuk menampilkan posisi rantai.
7. Mikrokontroller berfungsi untuk sebagai kontrol utama untuk menggerakkan keseluruhan system dengan bantuan software atau untuk memproses data masukan dan selanjutnya akan mengaktifkan driver motor dc dan tampilan pada display seven segment.

Cara kerja:

Pada model sistem pergeseran posisi rantai sepeda pada sepeda balap, saat terjadi perubahan kondisi jalan yang dilalui oleh sepeda, sensor kemiringan akan mendeteksi terjadinya perubahan sudut kemiringan jalan. Perubahan sinyal yang dihasilkan oleh potensiometer kemudian dikuatkan oleh Op-Amp untuk kemudian di-input-kan pada ADC yang berfungsi untuk mengubah sinyal analog yang dihasilkan oleh sensor kemiringan menjadi sinyal digital. Setelah menjadi sinyal digital, maka sinyal digital tersebut kemudian dii-input-kan pada mikrokontroller untuk kemudian diproses. Apabila sensor mendeteksi terjadi perubahan kondisi jalan, maka mikrokontroller akan memerintahkan driver motor dc untuk menggerakkan rantai agar berada pada posisi gear yang telah ditentukan. Sensor posisi rantai akan mendeteksi apakah rantai sudah berada pada posisi yang telah ditentukan yang kemudian akan ditampilkan pada display seven segment.

3.2.2. Perancangan Sensor Kemiringan

Perancangan sensor dibagi menjadi tiga blok yang dapat dilihat pada gambar berikut:



Gambar 3-2

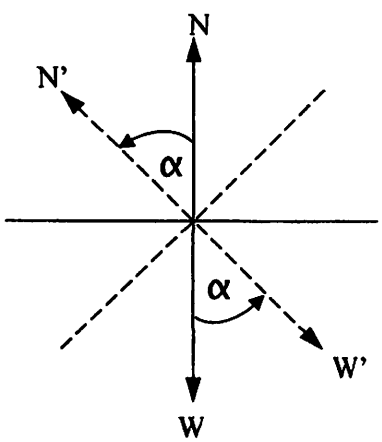
Sensor Kemiringan

Dimana: Pin 1 sebagai ground.

Pin 2 merupakan keluaran dari sensor kemiringan.

Pin 3 sebagai Vcc dengan tegangan sebesar +5 Volt.

Pada pembuatan sensor kemiringan ini digunakan potensiometer. Potensiometer berfungsi untuk mengubah perubahan nilai besaran sudut yang terjadi menjadi perubahan nilai besaran resistansi. Prinsip kerja dari sensor sudut dapat dilihat pada gambar berikut:



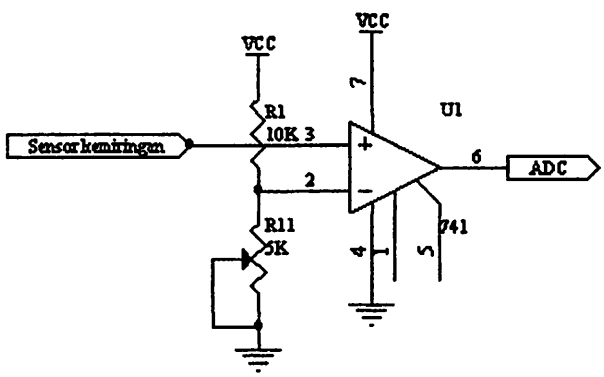
Gambar 3-3

Prinsip Kerja Sensor Kemiringan

Bila W dimiringkan sebesar α, maka W' akan membentuk sudut yang besarnya sama dengan α terhadap bidang normalnya. Besarnya α akan terdeteksi sebagai perubahan sudut. Pergeseran ini juga akan memutar tuas potensio sebesar α. Perubahan nilai yang ditunjukkan oleh potensio merupakan perubahan dari besarnya α dalam satuan Ohm.

3.2.3 Pengkondisi Sinyal

Rangkaian ini dibuat untuk mengubah nilai resistansi dari sensor menjadi nilai tegangan sekaligus berfungsi sebagai penguat. Penguat operasional dipergunakan untuk menguatkan tegangan yang kecil dari Potensiometer, sehingga menjadi tegangan yang berkisar antara 0 volt sampai 5 volt. Sebuah penguat tak membalik, yaitu dengan tegangan keluaran (Vo) mempunyai polaritas yang sama seperti tegangan masukan (Ei), atau tegangan output sefasa dengan tegangan inputnya.



Gambar 3-4
Rangkaian Penguat (Om-Amp)

Apabila tegangan antara terminal masukan (+) dan terminal masukan (-) menunjukkan 0 (nol) volt, hal ini menyebabkan besar tegangan input (-) dan sama dengan

besar tegangan input (+) terhadap ground yaitu berada pada potensial Ei yang sama. Karena Ei tampak melintas Ri, Ei menyebabkan arus I mengalir sebasar :

$$I = \frac{Ei}{Ri} \text{ (Ampere).}$$

Arah arus (I) tergantung pada polaritasEi, karena arus akan mengalir melalui Rf , penurunan tegangan melalui Rf dinyatakan oleh V_{rf}, ditunjukkan dengan persamaan sebagai berikut :

$$Vol = Ei + V_{Rf}$$

$$Vol = Ei + \left(\frac{Rf}{Ri} xEi\right) \text{ (Volt)}$$

$$Vol = \left(1 + \frac{Rf}{Ri}\right) x\ Ei \text{ (Volt).}$$

Besar penguatan (gain) diperoleh dari tegangan output berbanding dengan tegangan input, dimana diperoleh dengan persamaan sebagai berikut :

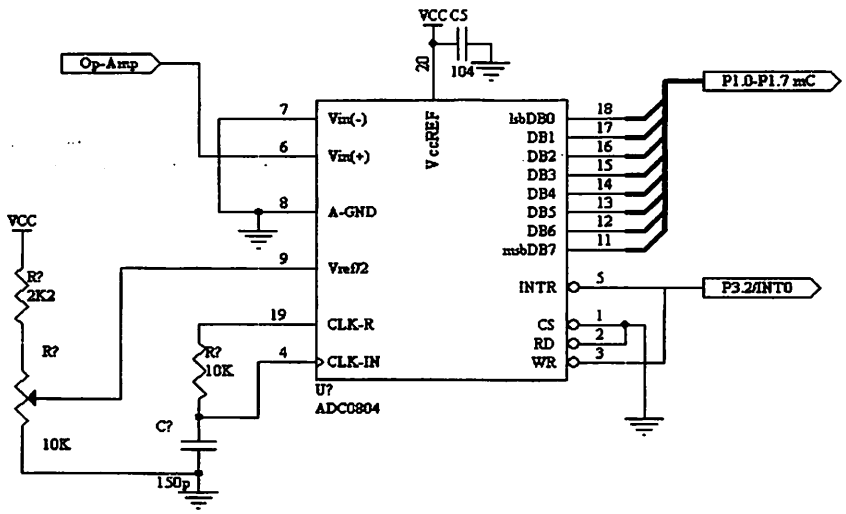
$$Aol = \frac{Vo}{Ei}$$

$$Aol = \left(1 + \frac{Rf}{Ri}\right) = \left(1 + \frac{5K}{10K}\right) = (1+0,5) = 1,5 \textit{ kali.}$$

Arus beban I_L diberikan oleh $\frac{Vo}{RL}$ karena hanya tergantung pada Vo dan RL saja sedangkan Io adalah arus yang mengalir dari keluaran Op-Amp.

3.2.4. Perancangan Rangkaian ADC (*Analog Digital Converter*)

Perancangan rangkaian ADC (*Analog Digital Converter*) dapat dilihat pada gambar 3-5 di bawah ini:



Gambar 3-5

Rangkaian ADC 0804

Rangkaian ADC ini berfungsi mengkonversikan besaran analog menjadi besaran digital agar nantinya dapat diolah oleh mikrokontroller sebagai data masukannya. Jadi sinyal keluaran dari sensor adalah sinyal analog yang harus diubah menjadi sinyal digital agar dapat diinterfacekan sehingga dapat dibaca oleh program komputer.

Untuk rangkaian pengkonversian data analog ke digital (ADC) digunakan *IC 0804* buatan national semikonduktor. Dengan sebuah masukan yaitu Vin + (pin6) dan delapan buah keluaran yaitu DB0-DB7 (pin11-pin18) pada port 1. Bekerja dengan tegangan referensi sebesar 2,5 Volt pada Vref/2 atau pin 9 yang didapat dari resistor pembagi tegangan (sesuai data sheet). Fungsi dari rangkaian referensi ini adalah untuk mendapatkan resolusi 1 bit yang diinginkan. Sebagai Vcc adalah tegangan 5V stabil yang dihubungkan dengan pin 20 pada chip. Pemasangan kapasitor pada pin 20 terhadap ground berfungsi untuk sebagai filter. Untuk mendapat clock, maka pin 19 dan pin 4 dihubungkan dengan resistor R ditentukan

sebesar 10 KΩ dan nilai kapasitor C sebesar 150 pF, sehingga frekuensi clock dapat dihitung dengan rumus:

$$f = \frac{1}{1{,}1 \times RC}$$

$$f = \frac{1}{1{,}1 \times 10K \times 150p}$$

$$f = 606{,}06 \text{ KHz}$$

Dari perhitungan diatas dapat dilihat bahwa harga frekuensi yang didapatkan sudah dapat memenuhi harga yang diminta ADC 0804 berdasarkan data sheetnya. ADC ini dirancang dapat menerima masukan 0 sampai 5 Volt sehingga bit berbobot $\frac{5}{255}$ = 19,6 mV. Tegangan referensi Vref /2 diset 2,00 Volt sehingga Vref yang dihasikan sebesar 4,00 Volt maka untuk perhitungan resolusi setiap 1 bit berbobot :

$$\text{Resolusi 1 bit} = \frac{vref}{255} \text{ (banyaknya data per bit } 2^8 = 255)$$

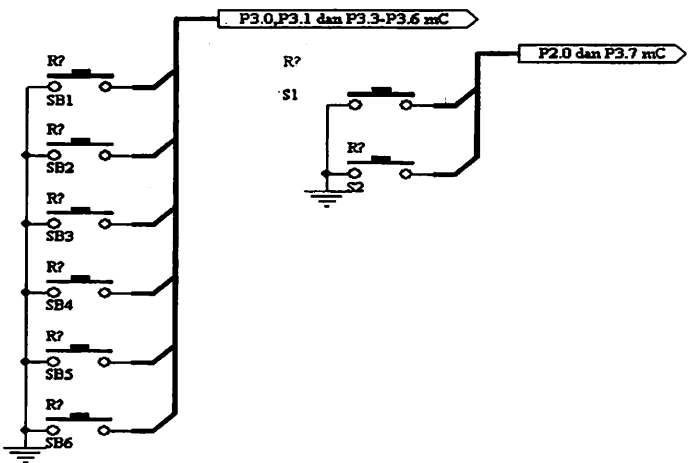
$$= \frac{4}{255} = 15{,}6 \text{ mV.}$$

Sedangkan $V_{IN\,(-)}$ dihubungkan ke ground $V_{IN\,(+)}$ sebagai input analog. Untuk mendapatkan konversi yang terus menerus sesuai perubahan input maka pin 3 WR dan pin 5 INTR pada chip dihubungkan, pin 1 CS dan pin 2 RD dihubungkan ke ground.

3.2.5. Sensor posisi rantai

Perancangan sensor posisi rantai bertujuan untuk mendeteksi posisi rantai, baik pada gear depan maupun pada gear belakang. Pada perancangan sensor posisi rantai digunakan limit switch. Limit switch akan tertekan apabila terjadi perubahan posisi rantai. Misalnya pada gear depan, bila terjadi perubahan posisi rantai dari gear 1 ke gear 2, yang tadinya limit

switch S1 yang tertekan, maka mikrokontrller akan memerintahkan untuk menekan limit switch S2. Demikian pula bila terjadi perubahan posisi rantai pada gear belakang. Perancangan sensor posisi rantai dapat dilihat pada gambar 3-6 berikut.

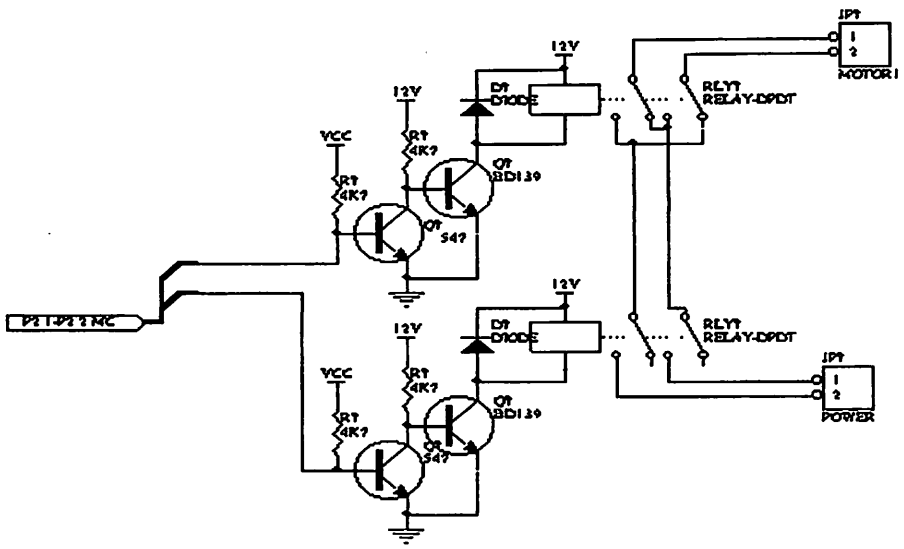


Gambar 3-6

Rangkaian Sensor Posisi Rantai

3.2.6. Rangkaian Driver Motor DC

Pada perancangan rangkaian driver motor dc digunakan rangkaian driver relay yang dapat menggerakkan motor dc bergerak dua arah. Rangkaian relay DPDT yang terhubung dengan AT89S51 dapat dilihat pada gambar 3-7 berikut ini.



Gambar 3-7

Rangkaian Driver Motor Pemindah Posisi Rantai

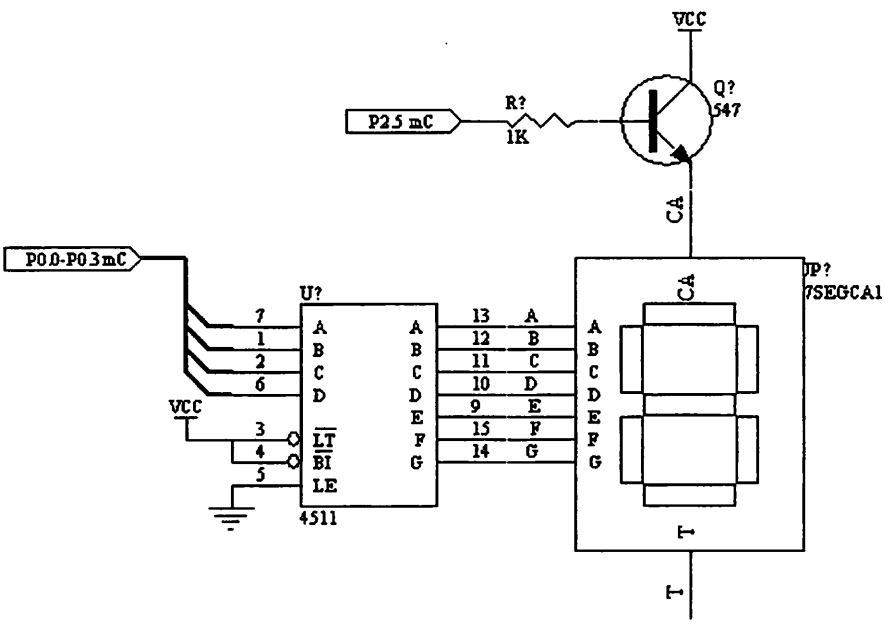
Cara kerja rangkaian driver relay dari gambar diatas menggunakan dua buah transistor yaitu BC 547 dan BD 139 sebagai penguat arus. Penguat arus untuk menggerakkan relay yang selanjutnya relay akan mengaktifkan motor. Relay akan menyambung jika ada arus yang melewati kumparan, arus ini yang akan diatur oleh transistor, sedang transistor akan aktif apabila mendapat arus bias dari basis. Jika ada arus bias dari basis, maka arus akan mengalir dari kolektor dan keluaran arus dari kolektor BC 547 akan masuk ke basis BD 139 dan arus bias dari basis akan mengalir ke kolektor sehingga kumparan relay akan terhubung dengan emitor. Pada saat arus kolektor mengalir, maka arus dari sumber akan mengalir sehingga relay aktif dan jika tidak ada arus bias dari basis, maka tidak ada arus yang mengalir dari kolektor ke emitor sehingga relay tidak aktif. Relay yang digunakan adalah relay mekanik DPDT dengan tegangan 12 V. Sinyal penggerak relay ini adalah keluaran dari transistor. Karena relay adalah beban induktif, maka pada saat saklar berguling

ke off , akan masih terdapat tegangan induksi, sehingga pada rangakainan driver relay ini ditambahkan diode yang berfungsi untuk menghubung-singkat tegangan induksi tersebut.

3.2.7. Rangkaian Display Seven Segment

Seven segment terdiri dari tujuh buah LED yang dikemas di dalam satu kemasan. Diantara dua kaki yang dimiliki oleh LED terdebut, salah satu kaki dari ketujuh LED tersebut saling dihubungkan yang satu dengan yang lainnya atau lebih dikenal dengan common. Common pada seven segment yang digunakan pada perancangan ini adalah jenis common anoda.

Pada perancangan alat ini, seven segment digunakan untuk menampilkan angka 1 sampai 6 untuk posisi rantai pada gear belakang dan angka 1 sampai 2 untuk posisi rantai pada gear depan. Gambar dari rangkaian seven segment terlihat pada gambar 3-8 dibawah ini.



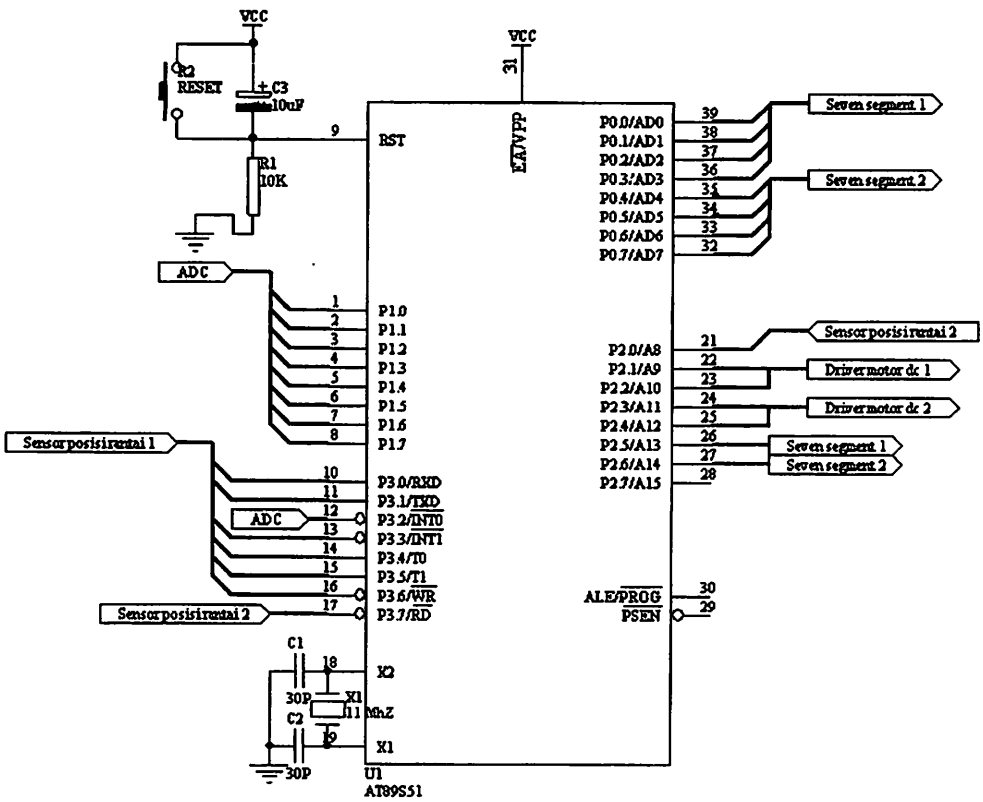
Gambar 3-8

Rangkaian display 7segment

3.2.8. Mikrokontroller AT89S51

Mikrokontroller pada system berfungsi untuk mengolah data masukan dan selanjutnya akan mengaktifkan driver motor dc dan tampilan pada display seven segment.

Mikrokontroller yang digunakan pada system adalah mikrokontroller jenis AT89S51 yang merupakan IC CMOS 8 bit internal RAM, 40 pin dan 3 port I/O. Untuk dapat melakukan fungsinya sebagai pengolah data, mikrokontroler AT89S51 harus didukung oleh beberapa komponen tambahan, yaitu berupa rangkaian clock dan reset. Penggunaan port-port dan sinyal-sinyal yang digunakan juga harus ditentukan.



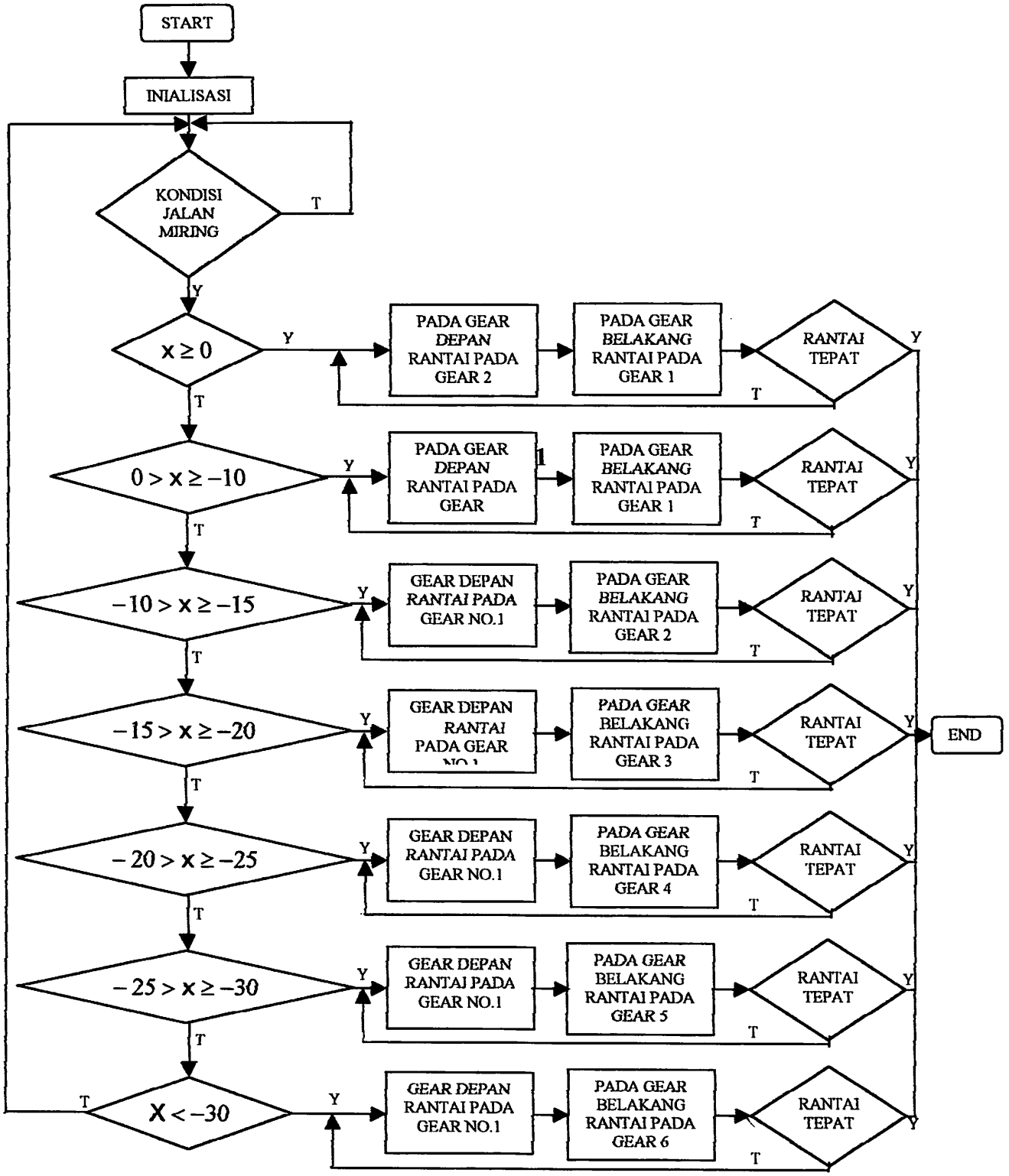
Gambar 3-9

Rangkaian Mikrokontroller AT89S51

Adapun fungsi masing-masing pin dalam mikrokontroller AT89S51 adalah:

1. Pin 1-8 (P1.0-P1.7) dan Pin 12 (P3.2) $\overline{INT0}$ digunakan sebagai input mikrokontroller dari rangkaian ADC (Analog Digital Converter).
2. Pin 9 reset aktif tinggi yang terhubung dengan Power On Reset dan jika diaktifkan akan mereset mikrokontroller.
3. Pin 10,11 dan 13-16 (P3.0, P3.1 dan P3.3-P3.6) befungsi untuk input mikrokontroller dari sensor posisi rantai sepeda pada gear belakang.
4. Pin 17 dan 21 (P3.7 dan P2.0) befungsi untuk input mikrokontroller dari sensor posisi rantai sepeda pada gear depan.
5. Pin 18 (XTAL 1) sebagai pembangkit oscillator (clock) XTAL 1.
6. Pin 19 (XTAL 2) sebagai pembangkit oscillator (clock) XTAL 2.
7. Pin 20 dihubungkan ke ground.
8. Pin 31 (EA/VPP) berfungsi sebagai Vcc +5 volt.
9. Pin 22 dan 23 (P2.1 dan P2.2) merupakan output dari mikrokontroller berfungsi untuk mengaktifkan driver relay motor dc pemindah posisi rantai pada gear depan.
10. Pin 24 dan 25 (P2.3 dan P2.4) merupakan output dari mikrokontroller berfungsi untuk mengaktifkan driver relay motor dc pemindah posisi rantai pada gear belakang.
11. Pin 36-39 (P0.0-P0.3) dan Pin 26 (P2.5) berfungsi sebagai outputan untuk rangkaian display untuk posisi rantai pada gear depan.
12. Pin 32-35 (P0.4-P0.7) dan Pin 27 (P2.6) berfungsi sebagai outputan untuk rangkaian display untuk posisi rantai pada gear belakang.

3.2.9. Diagram Alir Perpindahan Posisi Rantai



Gambar 3-10
Diagram Alir Perpindahan Posisi Rantai Sepeda

Pada saat start perubahan kemiringan jalan akan terdeteksi oleh sensor kemiringan jalan. Apabila terjadi perubahan kondisi kemiringan jalan, maka mikrokontroller akan memerintahkan motor dc untuk menarik atau mengendurkan kawat seling. Jika perubahan sudut yang terjadi lebih besar atau sama dengan $0°$ (jalan mendatar atau menurun), maka rantai sepeda akan digerakkan pada posisi gear depan ke gear nomor 2 dan pada gear belakang ke gear nomor 1. Jika posisi rantai belum tepat berada pada posisi gear yang telah ditentukan maka proses akan terus dilakukan sampai rantai benar-benar berada pada posisi gear yang telah ditentukan. Apabila terjadi perubahan kondisi kemiringan jalan antara $0^0 > x \geq -10^0$ (kondisi jalan menanjak), maka rantai sepeda akan digerakkan pada posisi gear depan ke posisi gear nomor 1 dan posisi gear belakang nomor 1. Proses tersebut akan terus dilakukan sampai posisi rantai tepat berada pada gear yang telah ditentukan. Perubahan-perubahan sudut dengan perubahan posisi rantainya yang telah ditentukan dapat dilihat pada gambar 3-10 diatas.

BAB IV

PENGUJIAN ALAT

4.1. Pendahuluan

Setelah dilakukan perancangan diperlukan pengujian untuk mengetahui apakah peralatan yang telah dirancang bekerja sesuai dengan yang diharapkan. Pada bab ini pengujian alat dilakukan dengan mengamati masukan dan keluaran dari masing-masing sub system dari rangkaian secara keseluruhan. Sub system yang diuji meliputi:

- Sensor kemiringan jalan
- Rangkaian penguat
- Rangkaian ADC
- Rangkaian driver motor DC
- Rangkaian seven segment

4.2. Pengujian Perangkat Keras

Peralatan utama yang dibutuhkan untuk menunjang dalam pengujian alat yang telah dirancang adalah sebagai berikut:

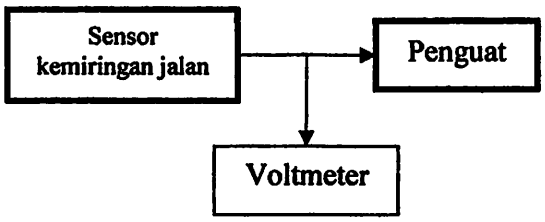
- Multimeter digital
- Power suplay 5 Volt DC dan 12 Volt DC
- Modul downloader AT89S51
- Mistar busur derajat
- Komputer

4.2.1. Pengujian Rangkaian Sensor Kemiringan

Sensor kemiringan yang digunakan adalah potensiometer. Bagian yang diukur pada potensiometer adalah tegangan output (V_{out}) yang dihasilkan. Tegangan output selalu berubah-ubah sesuai dengan nilai yang dihasilkan dari perubahan pada nilai tahanan potensiometer.

1. Tujuan

   Pengujian sensor kemiringan (potensiometer) berfungsi untuk mengetahui keluaran tegangan (V_{out}) dengan sudut yang dibentuk oleh kemiringan jalan dan linieritas dari potensio tersebut.



Gambar 4-1

Pengujian Rangkaian Sensor Kemiringan Jalan

Tabel 4-1

Data Hasil Pengujian Rangkaian Sensor Kemiringan Jalan

Sudut (°)	V_{out} max (Volt)
$X \geq 0$	**0,95**
$0 > X \geq -10$	**1,143**
$-10 > X \geq -15$	**1,264**
$-15 > X \geq -20$	**1,353**
$-20 > X \geq -25$	**1,457**
$-25 > X \geq -30$	**1,575**
$X < -30$	**1,893**

2. Analisa pengujian dan kesimpulan

   - Dari hasil pengujian pada tabel di atas dapat disimpulkan bahwa setiap perubahan sudut yang terjadi, nilai tahanan pada potensiometer tidak berubah secara linier, mengingat potensiometer yang digunakan bukan jenis linier. Hal ini mengakibatkan perubahan nilai tegangan output (V_{out}) tidak linier pula.
   - Dari hasil pengujian pada tabel diatas dapat disimpulkan bahwa semakin kecil perubahan sudut yang terjadi pada potensiometer, semakin besar nilai tegangan output (V_{out}) yang dihasilkan.

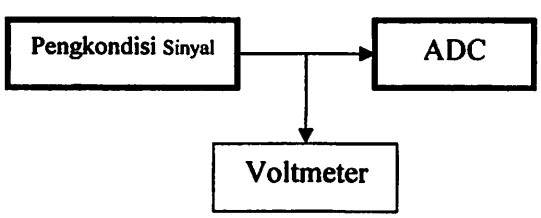
4.2.2. Pengujian Rangkaian Pengkondisi Sinyal

Bagian yang diukur pada penguat non-inferting adalah tegangan output (V_{out}) yang dihasilkan oleh Op-Amp.

1. Tujuan

   Pengujian rangkaian penguat berfungsi untuk mengetahui keluaran tegangan (V_{out}) penguat Op-Amp pada setiap perubahan sudut yang terjadi dan membandingkannya dengan hasil perhitungan. Untuk mengetahui tegangan output yang dihasilkan maka kita dapat mengukurnya pada pin 6 dari Op-Amp.

   Pengujian dan pengukuran rangkaian penguat (Op-Amp) dilakukan berdasarkan blok diagram dibawah.



Gambar 4-2

Pengujian Rangkaian Pengkondisi Sinyal

Pada dasarnya semua Op-Amp yang dipakai dalam rangkaian penguat mempunyai prinsip kerja yang sama yaitu menguatkan sinyal masukkan

Untuk mencari tegangan outputnya kita dapat gunakan rumus:

$$Vo = \left(1 + \frac{Rf}{R1}\right). Ei$$

Dimana Ei adalah tegangan output dari sensor kemiringan. Berdasarkan rumus diatas, penguatan pada masing-masing sudut dapt dicari. Misal Ei = 0,95 Volt maka besarnya penguatan adalah sebagai berikut:

$$Vo = \left(1 + \frac{5}{10}\right) .0{,}95 \text{ Volt}$$

$$= 1{,}425 \text{ Volt}$$

Dengan menggunakan cara yang sama, hasil selengkapnya dapat dilihat pada tabel 4-2 dibawah ini.

Tabel 4-2

Data Hasil Perhitungan dan Pengukuran Output Rangkaian Op-Amp

Sudut Kemiringan (°)	V_{out} max (Volt)	
	Perhitungan	Pengukuran
$X \geq 0$	1,425	1,633
$0 > X \geq -10$	1,715	1,891
$-10 > X \geq -15$	1,896	2,102
$-15 > X \geq -20$	2,030	2,234
$-20 > X \geq -25$	2,186	2,393
$-25 > X \geq -30$	2,363	2,574
$X < -30$	2,840	3,054

Untuk mencari kemungkinan kesalahan relatif dapat dicari dengan rumus sebagai berikut:

$$\text{Kesalahan relatif} = \left|\frac{\text{perhitungan} - \text{pengukuran}}{\text{perhitungan}}\right| \times 100\%$$

$$= \left|\frac{1{,}425 - 1{,}633}{1{,}425}\right| \times 100\%$$

$$= 0{,}208\%$$

Dengan menggunakan cara yang sama, hasil selengkapnya dapat dilihat pada table 4-3 dibawah ini.

Tabel 4-3

Data Kesalahan Relatif

Sudut Kemiringan (°)	V_{out} max (Volt)	V_{out} max (Volt)	Error
	Perhitungan	Pengukuran	(%)
$X \geq 0$	1,425	1,633	0,208
$0 > X \geq -10$	1,715	1,891	0,176
$-10 > X \geq -15$	1,896	2,102	0,206
$-15 > X \geq -20$	2,030	2,234	0,204
$-20 > X \geq -25$	2,186	2,393	0,207
$-25 > X \geq -30$	2,363	2,574	0,211
$X < -30$	2,840	3,054	0,214

Kesalahan relatif rata-rata dapat dicari dengan rumus:

$$\text{Kesalahan relatif rata-rata} = \frac{\Sigma \text{error}}{x}$$

Dimana: $\sum$ error = jumlah error

X = banyaknya sampel

Jadi apabila $\sum$ error = 1,426%

X = 7

Maka kesalahan relatif rata-rata = $\frac{1,426}{7}$ = 0,204%

2. Analisa dan Kesimpulan

Dari hasil perhitungan dan pengukuran pada tabel 4-3 diatas, maka dapat disimpulkan terjadi selisih dari hasil perhitungan dan pengukuran, sehingga terdapat nilai kesalahan relatif rata-ratanya yang dapat dicari dengan rumus:

Kesalahan relatif rata-rata = $\frac{\sum error}{x}$

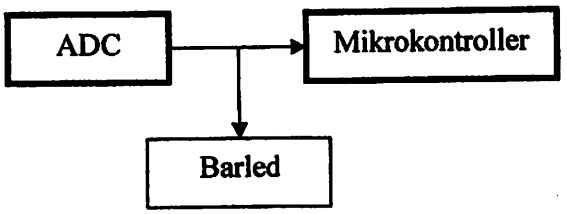
Dimana: $\sum$ error = jumlah error

X = banyaknya sampel

4.2.3. Pengujian Rangkaian ADC

1. Tujuan

Tujuan pengujian rangkian ADC 0804 adalah untuk mengetahui nilai hasil converter tegangan analog ke digital karena mikrokontroller hanya bisa menerima sinyal yang berupa sinyal digital. Pengujian dan pengukuran rangkaian ADC dilakukan berdasarkan blok diagram dibawah.



Gambar 4-3

Pengujian Rangkaian ADC

Data hasil converter dari tegangan analog ke digital dapat dilihat pada table 4-4 berikut ini:

Tabel 4-4

Data Hasil Pengujian Rangkaian ADC

Sudut Kemiringan (°)	V_{out} max (Volt) Perhitungan	V_{out} max (Volt) Pengukuran	Error (%)	ADC output							
				D7	D6	D5	D4	D3	D2	D1	D0
$X \geq 0$	1,425	1,633	0,208	0	1	1	1	1	1	1	0
$0 > X \geq -10$	1,715	1,891	0,176	1	0	0	1	1	0	0	0
$-10 > X \geq -15$	1,896	2,102	0,206	1	0	1	0	0	1	1	1
$-15 > X \geq -20$	2,030	2,234	0,204	1	0	1	1	0	1	0	0
$-20 > X \geq -25$	2,186	2,393	0,207	1	1	0	0	0	0	1	0
$-25 > X \geq -30$	2,363	2,574	0,211	1	1	0	1	0	0	0	1
$X < -30$	2,840	3,054	0,214	1	1	1	1	1	0	0	0

2. Analisa dan kesimpulan

ADC 0804 sebagai pengkonversi sinyal analog menjadi sinyal digital sangatlah membantu, dalam pengkonversian dengan ketentuan masukannya harus disesuaikan dahulu dengan karakteristik ADC itu sendiri.

Dari tabel 4-4 di atas dapat diketahui nilai biner hasil converter tegangan analog ke digital dari ADC. Dari nilai biner tersebut dapat dicari nilai decimal dan hexadecimal dari output ADC. Nilai decimal dan hexadesimalnya dapat dilihat pada table 4-5 dibawah ini:

Tabel 4-5

Data Hasil Converter dari Output Rangkaian ADC

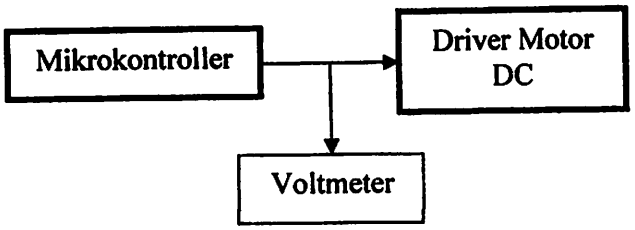
Dari Biner ke Decimal dan Hexadecimal

ADC output									
D7	D6	D5	D4	D3	D2	D1	D0	DECIMAL	HEXADECIMAL
0	1	1	1	1	1	1	0	126	7Eh
1	0	0	1	1	0	0	0	152	98h
1	0	1	0	0	1	1	1	167	A7h
1	0	1	1	0	1	0	0	180	B4h
1	1	0	0	0	0	1	0	194	C2h
1	1	0	1	0	0	0	1	209	D1h
1	1	1	1	1	0	0	0	248	F8h

4.2.4. Pengujian Rangkaian Driver Motor DC

1. Tujuan

Pengujian rangkaian driver motor DC ini bertujuan untuk mengetahui nilai tegangan dan membuktikan cara kerja driver motor DC. Pengujian dan pengukuran rangkaian driver motor DC dilakukan berdasarkan blok diagram dibawah.



Gambar 4-4

Pengujian Rangkaian Driver Motor DC

Dari pengujian diatas didapat hasil pada table 4-6 dibawah ini:

Tabel 4-6

Data Hasil Pengujian Rangkaian Driver Motor DC

Input		V_{output} Driver motor DC (Volt)	Kondisi Motor DC
P2.1	P2.2		
1	1	0	Mati
0	1	4,30	Putar Kanan
0	0	-4,30	Putar Kiri

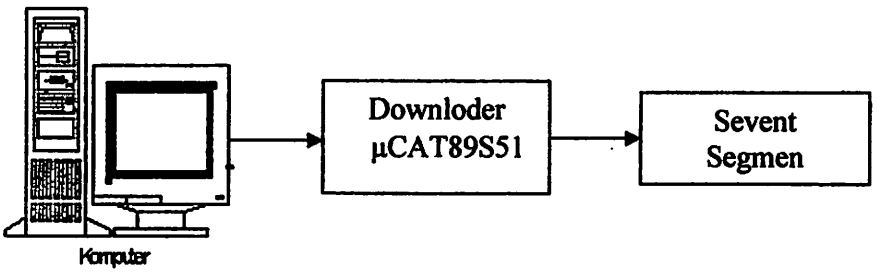
2 Analisa dan kesimpulan

Dari hasil pengujian diatas, driver berfungsi sebagai saklar pembalik polaritas dan driver motor DC ini akan aktif jika diberi logika '0', begitu juga sebaliknya jika diberi logika '1', driver motor DC akan mati. Pada saat motor DC berputar kekiri, tegangan yang dikeluarkan oleh Driver motor DC adalah positif (+), sedangkan pada saat motor DC berputar kekiri tegangan yang dikeluarkan oleh driver motor DC adalah negatif (-).

4.2.5. Pengujian Display (sevent segment)

1. Tujuan pengujian

Untuk mengetahui apakah seven segment yang telah dibuat tersebut dapat menampilkan angka.



Gambar 4-5

Pengujian Sevent Segmen

Hasil pengujian seven segment ditunjukkan dalam Tabel 4-5 berikut ini :

Tabel 4-7

Hasil Pengujian Seven Segment

Data	Tampilan Seven Segment
00111111b	0
00000110b	1
01011011b	2
01001111b	3
01100110b	4
01101101b	5
01111101b	6
00000111b	7
01111111b	8
01101111b	9

2. Analisa pengujian

Berdasarkan tabel hasil pengujian di atas, terlihat bahwa seven segment tersebut mampu menampilkan data angka sesuai dengan data biner yang diinputkan.

- Pada saat di inputkan 00111111b maka LED pada display seven segment menyala menampilkan angka 0 desimal.
- Pada saat di inputkan 00000110b maka LED pada display seven segment menyala menampilkan angka 1 desimal.
- Pada saat di inputkan 01011011b maka LED pada display seven segment menyala menampilkan angka 2 desimal.
- Pada saat di inputkan 01001111b maka LED pada display seven segment menyala menampilkan angka 3 desimal.
- Pada saat di inputkan 01100110b maka LED pada display seven segment menyala menampilkan angka 4 desimal.
- Pada saat di inputkan 01101101b maka LED pada display seven segment menyala menampilkan angka 5 desimal.
- Pada saat di inputkan 01111101b maka LED pada display seven segment menyala menampilkan angka 6 desimal.
- Pada saat di inputkan 00000111b maka LED pada display seven segment menyala menampilkan angka 7 desimal.
- Pada saat di inputkan 01111111b maka LED pada display seven segment menyala menampilkan angka 8 desimal.
- Pada saat di inputkan 01101111b maka LED pada display seven segment menyala menampilkan angka 9 desimal.

BAB V

PENUTUP

5.1. Kesimpulan

Dari keseluruhan pengujian dan perencanaan yang dilakukan dapat ditarik beberapa kesimpulan dibawah ini:

1. Potensiometer dapat dimanfaatkan sebagai sensor kemiringan dimana dalam aplikasi perlu dihubungkan dengan pendulum atau bandul.
2. Dengan posisi sensor kemiringan pada simulasi alat mengakibatkan semakin kecil perubahan sudut yang terjadi pada potensiometer, semakin besar nilai tegangan output (V_{out}) yang dihasilkan.
3. ADC 0804 sebagai pengkonversi sinyal analog menjadi sinyal digital sangatlah membantu dalam pengkonversian dengan ketentuan masukannya harus disesuaikan dahulu dengan karakteristik ADC itu sendiri.
4. Driver pada rangkaian motor DC berfungsi sebagai saklar pembalik polaritas dan driver motor DC ini akan aktif jika diberi logika '0' (aktif low), begitu juga sebaliknya jika diberi logika '1', driver motor DC akan mati.
5. Teknologi mikrokontroller AT89S51 dapat digunakan sebagai pengendali simulasi alat pemindah posisi rantai sepeda pada sepda balap secara otomatis, dimana dari perubahan nilai sensor kemiringan yang terbaca dapat menggerakkan posisi rantai sepada pada gear-gear sesuai tingkat kecepatannya.

5.2. Saran

1. Agar kinerja rangkaian dapat maksimal, disarankan untuk menggunakan komponen yang baik pula, serta jangan lupa untuk merencanakan *PCB* yang baik agar tidak terjadi kesalahan yang mengakibatkan kerusakan komponen yang mengkibatkan rangkaian tidak bekerja.
2. Untuk pengembangan alat ini selanjutnya diharapkan mampu dibuat pada kondisi jalan yang bergelombang atau pada kondisi jalan yang perubahan kondisi kemiringan jalannya cepat.
3. Untuk lebih sempurna lagi disarankan alat ini dapat dikembangkan agar bisa digunakan oleh semua orang, bukan hanya dari kalangan pembalap sepeda saja.

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LAMPIRAN

INSTITUT TEKNOLOGI NASIONAL MALANG
JL. BENDUNGAN SIGURA – GURA NO.2
MALANG

LEMBAR BIMBINGAN SKRIPSI
FAKULTAS TEKNOLOGI INDUSTRI

Nama Mahasiswa	: Kadek Artha Mahardhika
Nim	: 99.17.194
Jurusan	: Teknik Elektronika (S-1)
Konsentrasi	: Teknik Elektronika
Judul Skripsi	: Pemanfaatan Teknologi Mikrokontroller AT89S51 Untuk Perencanaan dan Pembuatan Simulasi Alat Pemindah Posisi Rantai Sepeda Pada Sepeda Balap
Tanggal Pengajuan Skripsi	: 26 Februari 2005
Selesai Menulis Skripsi	: 29 Agustus 2005
Pembimbing	: Ir. Kartiko Ardi Widodo, MT
Telah Dievaluasi Dengan	
Nilai (Dengan Angka)	:

Malang, September 2005
Mengetahui

Ketua Jurusan Teknik Elektro S-1	**Dosen Pembimbing**
(Ir. F. Yudi Limpraptono, MT)	**(Ir. Kartiko Ardi Widodo, MT)**

INSTITUT TEKNOLOGI NASIONAL
JL. BENDUNGAN SIGURA-GURA 2
MALANG

FORMULIR BIMBINGAN SKRIPSI

Nama : Kadek Artha Mahardika
Nim : 9917194
Masa Bimbingan : 26-Feb-2005 s/d 29-Aug-2005
Judul Skripsi : Pemanfaatan teknologi Mikrokontroller AT89S51 untuk Perencanaan dan pembuatan simulasi alat pemindah posisi rantai pada sepeda balap

NO	Tanggal	Uraian	Paraf Pembimbing
1.	4-3-2005	Bab I - tujuan - rumusan - batasan	
2.			
3.	10-4-2005	BAB II. untuk tiap reff perbaikan penulisan	
4.			
5.	25-4-2005	BAB II - blok diagram flow	
6.	12-5-2005	penyelesaian	
7.	20-6-2005	- diagram alir - buat narasi..	
8.	27-7-2005	BAB IV buat analisa utk masing bagian	
9.			
10.	18-8-2005	BAB V. kesimpulan. dan saran BAB IV	

Malang, 2005
Dosen Pembimbing

Ir. Kartiko Ardi Widodo, MT

Form. S-4a

INSTITUT TEKNOLOGI NASIONAL MALANG
FAKULTAS TEKNOLOGI INDUSTRI
JURUSAN TEKNIK ELEKTRO

Formulir Perbaikan Ujian Skripsi

Dalam pelaksanaan Ujian Skripsi Janjang Strata 1 Jurusan Teknik Elektro Konsentrasi T. Energi Listrik / T. Elektronika, maka perlu adanya perbaikan skripsi untuk mahasiswa :

NAMA : Kudela Atha M
N I M : 99.17.194
Perbaikan meliputi :

Malang, 3 Oct 2005

(Lakyo Cyadian)

INSTITUT TEKNOLOGI NASIONAL MALANG
FAKULTAS TEKNOLOGI INDUSTRI
JURUSAN TEKNIK ELEKTRO

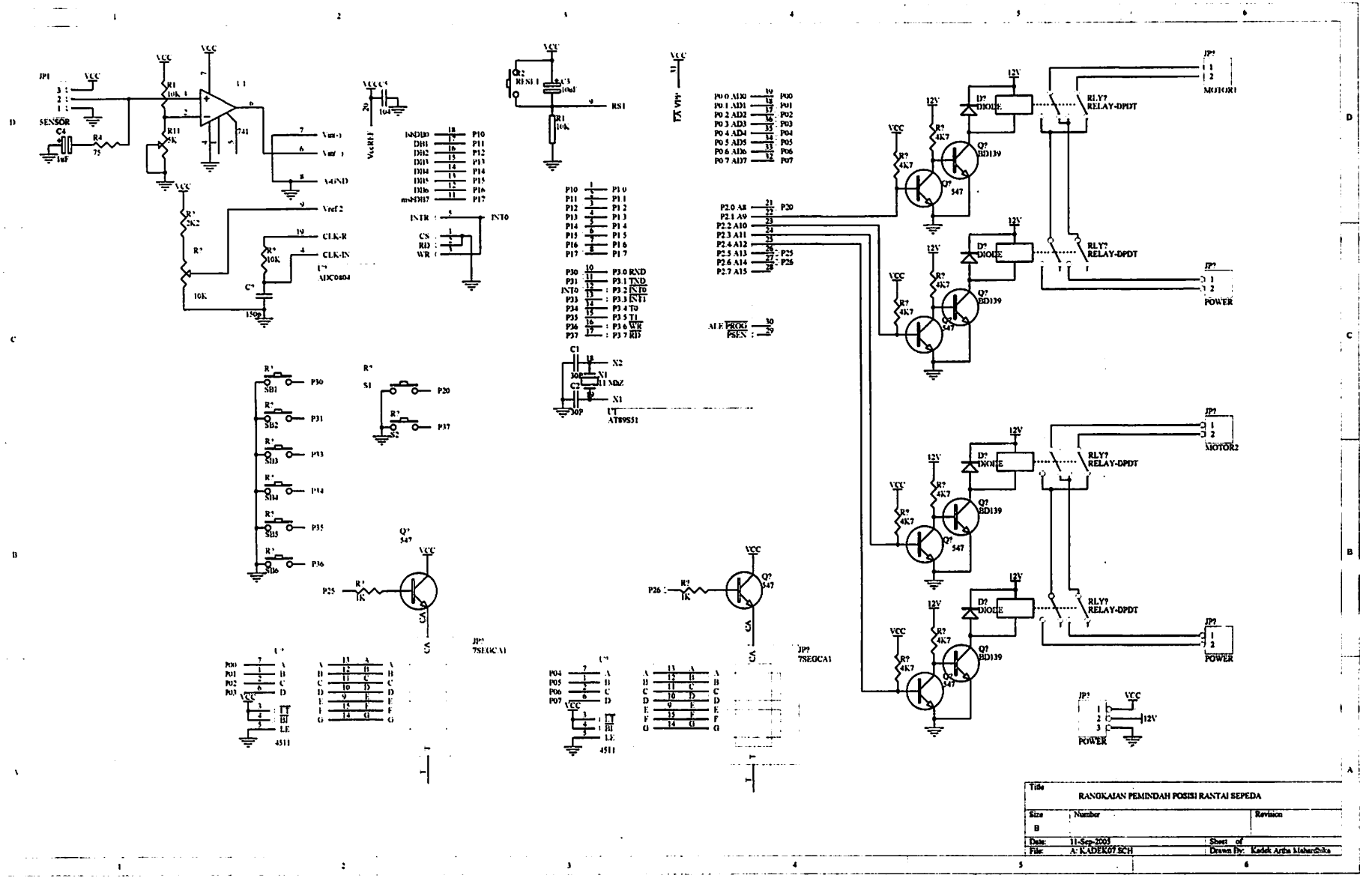
Formulir Perbaikan Ujian Skripsi

Dalam pelaksanaan Ujian Skripsi Janjang Strata 1 Jurusan Teknik Elektro Konsentrasi T. Energi Listrik / T. Elektronika, maka perlu adanya perbaikan skripsi untuk mahasiswa :

NAMA :
N I M :
Perbaikan meliputi :

Malang, 200

(_____)


SENSOR
741
AD0804
AT89S51
7SEGCA1
4511
MOTOR1
MOTOR2
POWER
RELAY-DPDT
DIODE
BD139
547
Title
RANGKAIAN PEMINDAH POSISI RANTAI SEPEDA
Size
B
Number
Revision
Date: 11-Sep-2005
Sheet of
File: A:\KADEK07.SCH
Drawn By: Kadek Artha Mahardhika

```
#include <c:\Gaza04X\FileH\reg51.h>
#include <c:\Gaza04X\FileH\DelayW.h>

sbit d1 = P1^0;
sbit d2 = P1^1;

sbit b1 = P1^2;
sbit b2 = P1^3;
sbit b3 = P1^4;
sbit b4 = P1^5;
sbit b5 = P1^6;
sbit b6 = P1^7;

sbit on1  = P3^2;
sbit blk1 = P3^3;
sbit on2  = P3^4;
sbit blk2 = P3^5;

sbit ss1 = P3^0;
sbit ss2 = P3^1;
sfr  dd  = 0xA0;

sfr sdt = 0x80;

unsigned char gd,gb;



void display11(){
unsigned char ii;
  for(ii=0;ii != 2;ii++){
      dd = 0xf9;
      ss1 = 1;
      delayMSEC(5);
      ss1 = 0;
   }
}

void display12(){
unsigned char ii;
  for(ii=0;ii != 2;ii++){

      dd = 0x24;
      ss1 = 1;
      delayMSEC(5);
      ss1 = 0;
  }
```

```
}

void display21(){
unsigned char ii;
  for(ii=0;ii != 2;ii++){
      dd = 0xf9;
      ss2 = 1;
      delayMSEC(5);
      ss2 = 0;
   }
}

void display22(){
unsigned char ii;
  for(ii=0;ii != 2;ii++){
      dd = 0x24;
      ss2 = 1;
      delayMSEC(5);
      ss2 = 0;
   }
}

void display23(){
unsigned char ii;
  for(ii=0;ii != 2;ii++){
      dd = 0x30;
      ss2 = 1;
      delayMSEC(5);
      ss2 = 0;
   }
}

void display24(){
unsigned char ii;
  for(ii=0;ii != 2;ii++){
      dd = 0x19;
      ss2 = 1;
      delayMSEC(5);
      ss2 = 0;
   }
}

void display25(){
unsigned char ii;
  for(ii=0;ii != 2;ii++){
      dd = 0x12;
      ss2 = 1;
```

```
      delayMSEC(5);
      ss2 = 0;
   }
}

void display26(){
unsigned char ii;
  for(ii=0;ii != 2;ii++){
      dd = 0x02;
      ss2 = 1;
      delayMSEC(5);
      ss2 = 0;
   }
}

void sudut0(){
   if(gd == 1){
      on1  = 0;
      blk1 = 0;

      while(d2){
         on1  = 1;
         blk1 = 1;
         gd   = 2;
      }
   }

   if(gd == 2){
      on1  = 1;
      blk1 = 1;
   }



   if (gb >= 2){
      on2  = 0;
      blk2 = 0;
      while(b1){
         on2 = 1;
         blk2 = 1;
         gb = 1;
      }
   }
   if (gb == 1){
      on2 = 1;
      blk2 = 1;
```

```
  }
}

void sudut10(){
  if(gd == 2){
    on1  = 0;
    blk1 = 0;

    while(d1){
      on1  = 1;
      blk1 = 1;
      gd   = 2;
    }
  }

  if(gd == 1){
    on1  = 1;
    blk1 = 1;
  }



  if (gb >= 2){
    on2  = 0;
    blk2 = 0;
    while(b1){
      on2 = 1;
      blk2 = 1;
      gb = 1;
    }
  }
  if (gb == 1){
    on2  = 1;
    blk2 = 1;
  }
}

void sudut15(){
  if(gd == 2){
    on1  = 0;
    blk1 = 0;

    while(d1){
      on1  = 1;
      blk1 = 1;
      gd   = 2;
    }
```

```
    }

    if(gd == 1){
      on1  = 1;
      blk1 = 1;
    }



    if (gb >= 3){
      on2  = 0;
      blk2 = 0;
      while(b2){
        on2 = 1;
        blk2 = 1;
        gb = 1;
      }
    }

    if (gb <= 1){
      on2  = 0;
      blk2 = 1;
      while(b2){
        on2 = 1;
        blk2 = 1;
        gb = 1;
      }
    }

    if (gb == 2){
      on2 = 1;
      blk2 = 1;

    }
}

void sudut20(){
    if(gd == 2){
      on1  = 0;
      blk1 = 0;

      while(d1){
        on1  = 1;
        blk1 = 1;
        gd   = 2;
      }
    }
```

```
  if(gd == 1){
    on1  = 1;
    blk1 = 1;
  }


  if (gb >= 4){
    on2  = 0;
    blk2 = 0;
    while(b3){
      on2 = 1;
      blk2 = 1;
      gb = 1;
    }
  }

  if (gb <= 2){
    on2  = 0;
    blk2 = 1;
    while(b3){
      on2 = 1;
      blk2 = 1;
      gb = 1;
    }
  }

  if (gb == 3){
    on2 = 1;
    blk2 = 1;

  }
}

void sudut25(){
  if(gd == 2){
    on1  = 0;
    blk1 = 0;

    while(d1){
      on1  = 1;
      blk1 = 1;
      gd   = 2;
    }
  }
```

```
    if(gd == 1){
      on1  = 1;
      blk1 = 1;
    }



    if (gb >= 5){
      on2  = 0;
      blk2 = 0;
      while(b2){
        on2 = 1;
        blk2 = 1;
        gb = 1;
      }
    }

    if (gb <= 3){
      on2  = 0;
      blk2 = 1;
      while(b2){
        on2 = 1;
        blk2 = 1;
        gb = 1;
      }
    }

    if (gb == 4){
      on2 = 1;
      blk2 = 1;

    }
}

Main(){

    P1 = 0xff;
    P3 = 0xff;

    while(1){

      if(d1 == 0){
        gd = 1;
        display11();
      }

      if(d2 == 0){
```

```
        gd = 2;
        display12();
    }

    if(b1 == 0){
        gb = 1;
        display21();
    }

    if(b2 == 0){
        gb = 2;
        display22();
    }

    if(b3 == 0){
        gb = 3;
        display23();
    }

    if(b4 == 0){
        gb = 4;
        display24();
    }

    if(b5 == 0){
        gb = 5;
        display25();
    }

    if(b6 == 0){
        gb = 6;
        display26();
    }

    if(sdt == 0xee) sudut0();
    if(sdt == 0x76) sudut10();
    if(sdt == 0xe6) sudut15();
    if(sdt == 0x86) sudut20();
    if(sdt == 0x86) sudut25();
  }
}
```

eatures

- Compatible with MCS-51® Products
- 4K Bytes of In-System Programmable (ISP) Flash Memory
  - Endurance: 1000 Write/Erase Cycles
- 4.0V to 5.5V Operating Range
- Fully Static Operation: 0 Hz to 33 MHz
- Three-level Program Memory Lock
- 128 x 8-bit Internal RAM
- 32 Programmable I/O Lines
- Two 16-bit Timer/Counters
- Six Interrupt Sources
- Full Duplex UART Serial Channel
- Low-power Idle and Power-down Modes
- Interrupt Recovery from Power-down Mode
- Watchdog Timer
- Dual Data Pointer
- Power-off Flag
- Fast Programming Time
- Flexible ISP Programming (Byte and Page Mode)

)escription

ıe AT89S51 is a low-power, high-performance CMOS 8-bit microcontroller with 4K /tes of in-system programmable Flash memory. The device is manufactured using tmel's high-density nonvolatile memory technology and is compatible with the indus-y-standard 80C51 instruction set and pinout. The on-chip Flash allows the program ıemory to be reprogrammed in-system or by a conventional nonvolatile memory pro-'ammer. By combining a versatile 8-bit CPU with in-system programmable Flash on a ıonolithic chip, the Atmel AT89S51 is a powerful microcontroller which provides a ghly-flexible and cost-effective solution to many embedded control applications.

he AT89S51 provides the following standard features: 4K bytes of Flash, 128 bytes of AM, 32 I/O lines, Watchdog timer, two data pointers, two 16-bit timer/counters, a five-ɛctor two-level interrupt architecture, a full duplex serial port, on-chip oscillator, and ock circuitry. In addition, the AT89S51 is designed with static logic for operation ɔwn to zero frequency and supports two software selectable power saving modes. he Idle Mode stops the CPU while allowing the RAM, timer/counters, serial port, and ıterrupt system to continue functioning. The Power-down mode saves the RAM con-ıts but freezes the oscillator, disabling all other chip functions until the next external ıterrupt or hardware reset.

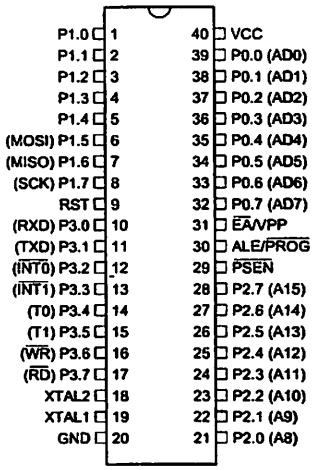
8-bit Microcontroller with 4K Bytes In-System Programmable Flash

AT89S51

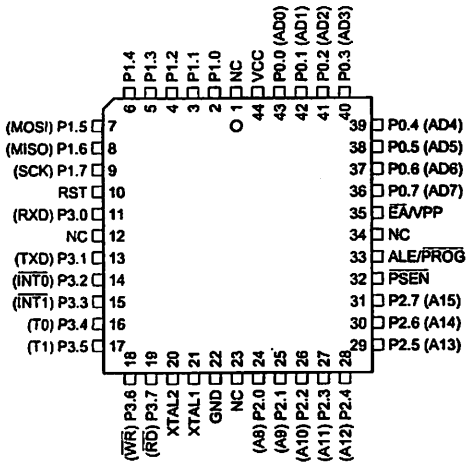
Rev. 2487A–10/01

Pin Configurations

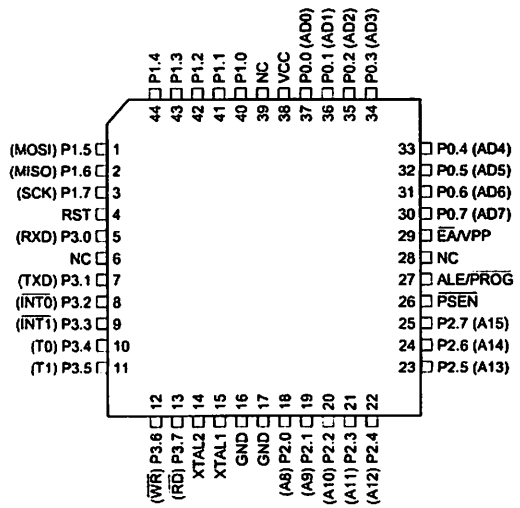
PDIP



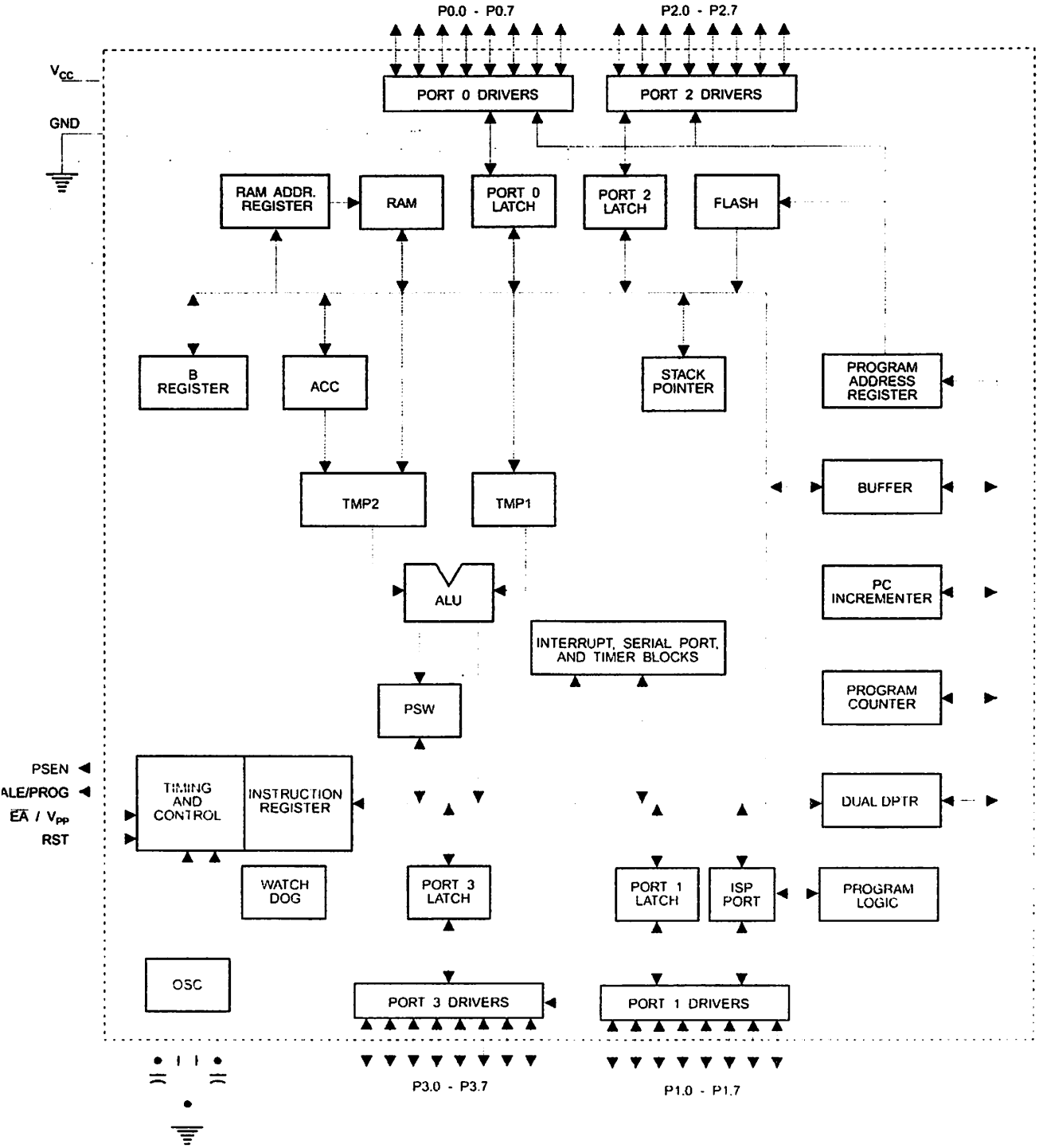
PLCC



TQFP



lock Diagram



in Description

CC Supply voltage.

iND Ground.

ort 0 Port 0 is an 8-bit open drain bidirectional I/O port. As an output port, each pin can sink eight TTL inputs. When 1s are written to port 0 pins, the pins can be used as high-impedance inputs.

Port 0 can also be configured to be the multiplexed low-order address/data bus during accesses to external program and data memory. In this mode, P0 has internal pull-ups.

Port 0 also receives the code bytes during Flash programming and outputs the code bytes during program verification. **External pull-ups are required during program verification.**

ort 1 Port 1 is an 8-bit bidirectional I/O port with internal pull-ups. The Port 1 output buffers can sink/source four TTL inputs. When 1s are written to Port 1 pins, they are pulled high by the internal pull-ups and can be used as inputs. As inputs, Port 1 pins that are externally being pulled low will source current (I_{IL}) because of the internal pull-ups.

Port 1 also receives the low-order address bytes during Flash programming and verification.

Port Pin	Alternate Functions
P1.5	MOSI (used for In-System Programming)
P1.6	MISO (used for In-System Programming)
P1.7	SCK (used for In-System Programming)

'ort 2 Port 2 is an 8-bit bidirectional I/O port with internal pull-ups. The Port 2 output buffers can sink/source four TTL inputs. When 1s are written to Port 2 pins, they are pulled high by the internal pull-ups and can be used as inputs. As inputs, Port 2 pins that are externally being pulled low will source current (I_{IL}) because of the internal pull-ups.

Port 2 emits the high-order address byte during fetches from external program memory and during accesses to external data memory that use 16-bit addresses (MOVX @ DPTR). In this application, Port 2 uses strong internal pull-ups when emitting 1s. During accesses to external data memory that use 8-bit addresses (MOVX @ RI), Port 2 emits the contents of the P2 Special Function Register.

Port 2 also receives the high-order address bits and some control signals during Flash programming and verification.

'ort 3 Port 3 is an 8-bit bidirectional I/O port with internal pull-ups. The Port 3 output buffers can sink/source four TTL inputs. When 1s are written to Port 3 pins, they are pulled high by the internal pull-ups and can be used as inputs. As inputs, Port 3 pins that are externally being pulled low will source current (I_{IL}) because of the pull-ups.

Port 3 receives some control signals for Flash programming and verification.

Port 3 also serves the functions of various special features of the AT89S51, as shown in the following table.

Port Pin	Alternate Functions
P3.0	RXD (serial input port)
P3.1	TXD (serial output port)
P3.2	$\overline{INT0}$ (external interrupt 0)
P3.3	$\overline{INT1}$ (external interrupt 1)
P3.4	T0 (timer 0 external input)
P3.5	T1 (timer 1 external input)
P3.6	$\overline{WR}$ (external data memory write strobe)
P3.7	$\overline{RD}$ (external data memory read strobe)

ST

Reset input. A high on this pin for two machine cycles while the oscillator is running resets the device. This pin drives High for 98 oscillator periods after the Watchdog times out. The DISRTO bit in SFR AUXR (address 8EH) can be used to disable this feature. In the default state of bit DISRTO, the RESET HIGH out feature is enabled.

LE/$\overline{PROG}$

Address Latch Enable (ALE) is an output pulse for latching the low byte of the address during accesses to external memory. This pin is also the program pulse input ($\overline{PROG}$) during Flash programming.

In normal operation, ALE is emitted at a constant rate of 1/6 the oscillator frequency and may be used for external timing or clocking purposes. Note, however, that one ALE pulse is skipped during each access to external data memory.

If desired, ALE operation can be disabled by setting bit 0 of SFR location 8EH. With the bit set, ALE is active only during a MOVX or MOVC instruction. Otherwise, the pin is weakly pulled high. Setting the ALE-disable bit has no effect if the microcontroller is in external execution mode.

$\overline{SEN}$

Program Store Enable ($\overline{PSEN}$) is the read strobe to external program memory.

When the AT89S51 is executing code from external program memory, $\overline{PSEN}$ is activated twice each machine cycle, except that two $\overline{PSEN}$ activations are skipped during each access to external data memory.

$\overline{A}$/VPP

External Access Enable. $\overline{EA}$ must be strapped to GND in order to enable the device to fetch code from external program memory locations starting at 0000H up to FFFFH. Note, however, that if lock bit 1 is programmed, $\overline{EA}$ will be internally latched on reset.

$\overline{EA}$ should be strapped to V_{CC} for internal program executions.

This pin also receives the 12-volt programming enable voltage (V_{PP}) during Flash programming.

TAL1

Input to the inverting oscillator amplifier and input to the internal clock operating circuit.

TAL2

Output from the inverting oscillator amplifier

pecial unction egisters

A map of the on-chip memory area called the Special Function Register (SFR) space is shown in Table 1.

Note that not all of the addresses are occupied, and unoccupied addresses may not be implemented on the chip. Read accesses to these addresses will in general return random data, and write accesses will have an indeterminate effect.

ıble 1. AT89S51 SFR Map and Reset Values

0F8H									0FFH
0F0H	B 00000000								0F7H
0E8H									0EFH
0E0H	ACC 00000000								0E7H
0D8H									0DFH
0D0H	PSW 00000000								0D7H
0C8H									0CFH
0C0H									0C7H
0B8H	IP XX000000								0BFH
0B0H	P3 11111111								0B7H
0A8H	IE 0X000000								0AFH
0A0H	P2 11111111		AUXR1 XXXXXXX0				WDTRST XXXXXXXX		0A7H
98H	SCON 00000000	SBUF XXXXXXXX							9FH
90H	P1 11111111								97H
88H	TCON 00000000	TMOD 00000000	TL0 00000000	TL1 00000000	TH0 00000000	TH1 00000000	AUXR XXX00XX0		8FH
80H	P0 11111111	SP 00000111	DP0L 00000000	DP0H 00000000	DP1L 00000000	DP1H 00000000		PCON 0XXX0000	87H

User software should not write 1s to these unlisted locations, since they may be used in future products to invoke new features. In that case, the reset or inactive values of the new bits will always be 0.

Interrupt Registers: The individual interrupt enable bits are in the IE register. Two priorities can be set for each of the five interrupt sources in the IP register.

Table 2. AUXR: Auxiliary Register

AUXR Address = 8EH Reset Value = XXX00XX0B

Not Bit Addressable

	–	–	–	WDIDLE	DISRTO	–	–	DISALE
Bit	7	6	5	4	3	2	1	0

–	Reserved for future expansion
DISALE	Disable/Enable ALE
	DISALE Operating Mode
	0 ALE is emitted at a constant rate of 1/6 the oscillator frequency
	1 ALE is active only during a MOVX or MOVC instruction
DISRTO	Disable/Enable Reset out
	DISRTO
	0 Reset pin is driven High after WDT times out
	1 Reset pin is input only
WDIDLE	Disable/Enable WDT in IDLE mode
WDIDLE	
0	WDT continues to count in IDLE mode
1	WDT halts counting in IDLE mode

Dual Data Pointer Registers: To facilitate accessing both internal and external data memory, two banks of 16-bit Data Pointer Registers are provided: DP0 at SFR address locations 82H-83H and DP1 at 84H-85H. Bit DPS = 0 in SFR AUXR1 selects DP0 and DPS = 1 selects DP1. The user should always initialize the DPS bit to the appropriate value before accessing the respective Data Pointer Register.

Power Off Flag: The Power Off Flag (POF) is located at bit 4 (PCON.4) in the PCON SFR. POF is set to "1" during power up. It can be set and rest under software control and is not affected by reset.

Table 3. AUXR1: Auxiliary Register 1

AUXR1

Address = A2H

Reset Value = XXXXXXX0B

Not Bit Addressable

	–	–	–	–	–	–	–	DPS
Bit	7	6	5	4	3	2	1	0

– Reserved for future expansion

DPS Data Pointer Register Select

DPS

0 Selects DPTR Registers DP0L, DP0H

1 Selects DPTR Registers DP1L, DP1H

lemory)rganization

MCS-51 devices have a separate address space for Program and Data Memory. Up to 64K bytes each of external Program and Data Memory can be addressed.

rogram Memory

If the $\overline{EA}$ pin is connected to GND, all program fetches are directed to external memory.

On the AT89S51, if $\overline{EA}$ is connected to V_{CC}, program fetches to addresses 0000H through FFFH are directed to internal memory and fetches to addresses 1000H through FFFFH are directed to external memory.

)ata Memory

The AT89S51 implements 128 bytes of on-chip RAM. The 128 bytes are accessible via direct and indirect addressing modes. Stack operations are examples of indirect addressing, so the 128 bytes of data RAM are available as stack space.

Vatchdog 'imer One-time :nabled with ?eset-out)

The WDT is intended as a recovery method in situations where the CPU may be subjected to software upsets. The WDT consists of a 14-bit counter and the Watchdog Timer Reset (WDTRST) SFR. The WDT is defaulted to disable from exiting reset. To enable the WDT, a user must write 01EH and 0E1H in sequence to the WDTRST register (SFR location 0A6H). When the WDT is enabled, it will increment every machine cycle while the oscillator is running. The WDT timeout period is dependent on the external clock frequency. There is no way to disable the WDT except through reset (either hardware reset or WDT overflow reset). When WDT overflows, it will drive an output RESET HIGH pulse at the RST pin.

Jsing the WDT

To enable the WDT, a user must write 01EH and 0E1H in sequence to the WDTRST register (SFR location 0A6H). When the WDT is enabled, the user needs to service it by writing 01EH and 0E1H to WDTRST to avoid a WDT overflow. The 14-bit counter overflows when it reaches 16383 (3FFFH), and this will reset the device. When the WDT is enabled, it will increment every machine cycle while the oscillator is running. This means the user must reset the WDT at least every 16383 machine cycles. To reset the WDT the user must write 01EH and 0E1H to WDTRST. WDTRST is a write-only register. The WDT counter cannot be read or written. When WDT overflows, it will generate an output RESET pulse at the RST pin. The RESET pulse duration is 98xTOSC, where TOSC=1/FOSC. To make the best use of the WDT, it

should be serviced in those sections of code that will periodically be executed within the time required to prevent a WDT reset.

/DT During ower-down nd Idle

In Power-down mode the oscillator stops, which means the WDT also stops. While in Power-down mode, the user does not need to service the WDT. There are two methods of exiting Power-down mode: by a hardware reset or via a level-activated external interrupt, which is enabled prior to entering Power-down mode. When Power-down is exited with hardware reset, servicing the WDT should occur as it normally does whenever the AT89S51 is reset. Exiting Power-down with an interrupt is significantly different. The interrupt is held low long enough for the oscillator to stabilize. When the interrupt is brought high, the interrupt is serviced. To prevent the WDT from resetting the device while the interrupt pin is held low, the WDT is not started until the interrupt is pulled high. It is suggested that the WDT be reset during the interrupt service for the interrupt used to exit Power-down mode.

To ensure that the WDT does not overflow within a few states of exiting Power-down, it is best to reset the WDT just before entering Power-down mode.

Before going into the IDLE mode, the WDIDLE bit in SFR AUXR is used to determine whether the WDT continues to count if enabled. The WDT keeps counting during IDLE (WDIDLE bit = 0) as the default state. To prevent the WDT from resetting the AT89S51 while in IDLE mode, the user should always set up a timer that will periodically exit IDLE, service the WDT, and reenter IDLE mode.

With WDIDLE bit enabled, the WDT will stop to count in IDLE mode and resumes the count upon exit from IDLE.

ART

The UART in the AT89S51 operates the same way as the UART in the AT89C51. For further information on the UART operation, refer to the ATMEL Web site (http://www.atmel.com). From the home page, select 'Products', then '8051-Architecture Flash Microcontroller', then 'Product Overview'.

imer 0 and 1

Timer 0 and Timer 1 in the AT89S51 operate the same way as Timer 0 and Timer 1 in the AT89C51. For further information on the timers' operation, refer to the ATMEL Web site (http://www.atmel.com). From the home page, select 'Products', then '8051-Architecture Flash Microcontroller', then 'Product Overview'.

ıterrupts

The AT89S51 has a total of five interrupt vectors: two external interrupts ($\overline{INT0}$ and $\overline{INT1}$), two timer interrupts (Timers 0 and 1), and the serial port interrupt. These interrupts are all shown in Figure 1.

Each of these interrupt sources can be individually enabled or disabled by setting or clearing a bit in Special Function Register IE. IE also contains a global disable bit, EA, which disables all interrupts at once.

Note that Table 4 shows that bit position IE.6 is unimplemented. In the AT89S51, bit position IE.5 is also unimplemented. User software should not write 1s to these bit positions, since they may be used in future AT89 products.

The Timer 0 and Timer 1 flags, TF0 and TF1, are set at S5P2 of the cycle in which the timers overflow. The values are then polled by the circuitry in the next cycle

Table 4. Interrupt Enable (IE) Register

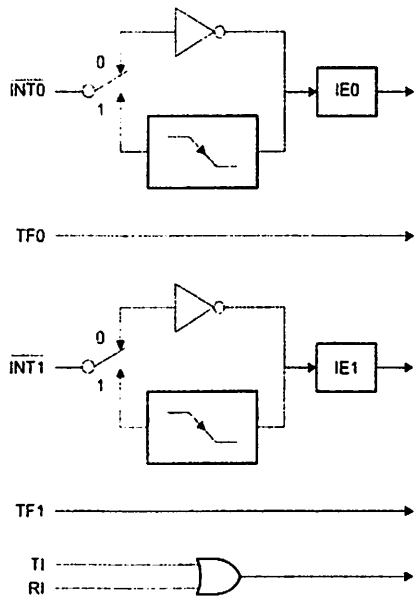
(MSB)							(LSB)
EA	–	–	ES	ET1	EX1	ET0	EX0

Enable Bit = 1 enables the interrupt.

Enable Bit = 0 disables the interrupt.

Symbol	Position	Function
EA	IE.7	Disables all interrupts. If EA = 0, no interrupt is acknowledged. If EA = 1, each interrupt source is individually enabled or disabled by setting or clearing its enable bit.
–	IE.6	Reserved
–	IE.5	Reserved
ES	IE.4	Serial Port interrupt enable bit
ET1	IE.3	Timer 1 interrupt enable bit
EX1	IE.2	External interrupt 1 enable bit
ET0	IE.1	Timer 0 interrupt enable bit
EX0	IE.0	External interrupt 0 enable bit
User software should never write 1s to reserved bits, because they may be used in future AT89 products.		

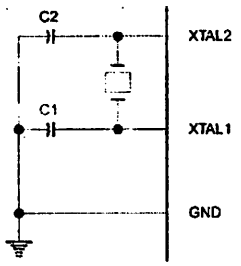
Figure 1. Interrupt Sources



scillator haracteristics

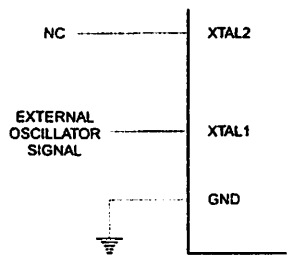
XTAL1 and XTAL2 are the input and output, respectively, of an inverting amplifier that can be configured for use as an on-chip oscillator, as shown in Figure 2. Either a quartz crystal or ceramic resonator may be used. To drive the device from an external clock source, XTAL2 should be left unconnected while XTAL1 is driven, as shown in Figure 3. There are no requirements on the duty cycle of the external clock signal, since the input to the internal clocking circuitry is through a divide-by-two flip-flop, but minimum and maximum voltage high and low time specifications must be observed.

Figure 2. Oscillator Connections



Note: C1, C2 = 30 pF ± 10 pF for Crystals = 40 pF ± 10 pF for Ceramic Resonators

Figure 3. External Clock Drive Configuration



le Mode

In idle mode, the CPU puts itself to sleep while all the on-chip peripherals remain active. The mode is invoked by software. The content of the on-chip RAM and all the special function registers remain unchanged during this mode. The idle mode can be terminated by any enabled interrupt or by a hardware reset.

Note that when idle mode is terminated by a hardware reset, the device normally resumes program execution from where it left off, up to two machine cycles before the internal reset algorithm takes control. On-chip hardware inhibits access to internal RAM in this event, but access to the port pins is not inhibited. To eliminate the possibility of an unexpected write to a port pin when idle mode is terminated by a reset, the instruction following the one that invokes idle mode should not write to a port pin or to external memory.

ower-down ode

In the Power-down mode, the oscillator is stopped, and the instruction that invokes Power-down is the last instruction executed. The on-chip RAM and Special Function Registers retain their values until the Power-down mode is terminated. Exit from Power-down mode can be initiated either by a hardware reset or by activation of an enabled external interrupt into $\overline{INT0}$ or $\overline{INT1}$. Reset redefines the SFRs but does not change the on-chip RAM. The reset should not be activated before V_{CC} is restored to its normal operating level and must be held active long enough to allow the oscillator to restart and stabilize.

Table 5. Status of External Pins During Idle and Power-down Modes

Mode	Program Memory	ALE	$\overline{PSEN}$	PORT0	PORT1	PORT2	PORT3
Idle	Internal	1	1	Data	Data	Data	Data
Idle	External	1	1	Float	Data	Address	Data
Power-down	Internal	0	0	Data	Data	Data	Data
Power-down	External	0	0	Float	Data	Data	Data

rogram lemory Lock its

The AT89S51 has three lock bits that can be left unprogrammed (U) or can be programmed (P) to obtain the additional features listed in the following table.

Table 6. Lock Bit Protection Modes

Program Lock Bits				
	LB1	LB2	LB3	Protection Type
1	U	U	U	No program lock features
2	P	U	U	MOVC instructions executed from external program memory are disabled from fetching code bytes from internal memory, $\overline{EA}$ is sampled and latched on reset, and further programming of the Flash memory is disabled
3	P	P	U	Same as mode 2, but verify is also disabled
4	P	P	P	Same as mode 3, but external execution is also disabled

When lock bit 1 is programmed, the logic level at the $\overline{EA}$ pin is sampled and latched during reset. If the device is powered up without a reset, the latch initializes to a random value and holds that value until reset is activated. The latched value of $\overline{EA}$ must agree with the current logic level at that pin in order for the device to function properly.

rogramming he Flash – arallel Mode

The AT89S51 is shipped with the on-chip Flash memory array ready to be programmed. The programming interface needs a high-voltage (12-volt) program enable signal and is compatible with conventional third-party Flash or EPROM programmers.

The AT89S51 code memory array is programmed byte-by-byte.

Programming Algorithm: Before programming the AT89S51, the address, data, and control signals should be set up according to the Flash programming mode table and Figures 13 and 14. To program the AT89S51, take the following steps:

1. Input the desired memory location on the address lines.
2. Input the appropriate data byte on the data lines.
3. Activate the correct combination of control signals.
4. Raise $\overline{EA}/V_{PP}$ to 12V.
5. Pulse ALE/$\overline{PROG}$ once to program a byte in the Flash array or the lock bits. The byte-write cycle is self-timed and typically takes no more than 50 µs. Repeat steps 1 through 5, changing the address and data for the entire array or until the end of the object file is reached.

$\overline{Data}$ Polling: The AT89S51 features $\overline{Data}$ Polling to indicate the end of a byte write cycle. During a write cycle, an attempted read of the last byte written will result in the complement of the written data on P0.7. Once the write cycle has been completed, true data is valid on all outputs, and the next cycle may begin. $\overline{Data}$ Polling may begin any time after a write cycle has been initiated.

Ready/Busy: The progress of byte programming can also be monitored by the RDY/$\overline{BSY}$ output signal. P3.0 is pulled low after ALE goes high during programming to indicate $\overline{BUSY}$. P3.0 is pulled high again when programming is done to indicate READY.

Program Verify: If lock bits LB1 and LB2 have not been programmed, the programmed code data can be read back via the address and data lines for verification. The status of the individual lock bits can be verified directly by reading them back.

Reading the Signature Bytes: The signature bytes are read by the same procedure as a normal verification of locations 000H, 100H, and 200H, except that P3.6 and P3.7 must be pulled to a logic low. The values returned are as follows.

(000H) = 1EH indicates manufactured by Atmel
(100H) = 51H indicates 89S51
(200H) = 06H

Chip Erase: In the parallel programming mode, a chip erase operation is initiated by using the proper combination of control signals and by pulsing ALE/$\overline{PROG}$ low for a duration of 200 ns - 500 ns.

In the serial programming mode, a chip erase operation is initiated by issuing the Chip Erase instruction. In this mode, chip erase is self-timed and takes about 500 ms.

During chip erase, a serial read from any address location will return 00H at the data output.

rogramming ıe Flash – erial Mode

The Code memory array can be programmed using the serial ISP interface while RST is pulled to V_{CC}. The serial interface consists of pins SCK, MOSI (input) and MISO (output). After RST is set high, the Programming Enable instruction needs to be executed first before other operations can be executed. Before a reprogramming sequence can occur, a Chip Erase operation is required.

The Chip Erase operation turns the content of every memory location in the Code array into FFH.

Either an external system clock can be supplied at pin XTAL1 or a crystal needs to be connected across pins XTAL1 and XTAL2. The maximum serial clock (SCK) frequency should be less than 1/16 of the crystal frequency. With a 33 MHz oscillator clock, the maximum SCK frequency is 2 MHz.

erial rogramming lgorithm

To program and verify the AT89S51 in the serial programming mode, the following sequence is recommended:

1. Power-up sequence:
   Apply power between VCC and GND pins.
   Set RST pin to "H".
   If a crystal is not connected across pins XTAL1 and XTAL2, apply a 3 MHz to 33 MHz clock to XTAL1 pin and wait for at least 10 milliseconds.
2. Enable serial programming by sending the Programming Enable serial instruction to pin MOSI/P1.5. The frequency of the shift clock supplied at pin SCK/P1.7 needs to be less than the CPU clock at XTAL1 divided by 16.
3. The Code array is programmed one byte at a time in either the Byte or Page mode. The write cycle is self-timed and typically takes less than 0.5 ms at 5V.
4. Any memory location can be verified by using the Read instruction that returns the content at the selected address at serial output MISO/P1.6.
5. At the end of a programming session, RST can be set low to commence normal device operation.

Power-off sequence (if needed):

Set XTAL1 to "L" (if a crystal is not used).

Set RST to "L".

Turn V_{CC} power off.

Data Polling: The Data Polling feature is also available in the serial mode. In this mode, during a write cycle an attempted read of the last byte written will result in the complement of the MSB of the serial output byte on MISO.

erial ogramming struction Set

The Instruction Set for Serial Programming follows a 4-byte protocol and is shown in Table 8 on page 18.

rogramming terface – arallel Mode

Every code byte in the Flash array can be programmed by using the appropriate combination of control signals. The write operation cycle is self-timed and once initiated, will automatically time itself to completion.

All major programming vendors offer worldwide support for the Atmel microcontroller series. Please contact your local programming vendor for the appropriate software revision.

ble 7. Flash Programming Modes

lode	V_{CC}	RST	PSEN	ALE/ PROG	EA/ V_{PP}	P2.6	P2.7	P3.3	P3.6	P3.7	P0.7-0 Data	P2.3-0 Address	P1.7-0 Address
/rite Code Data	5V	H	L	(2)	12V	L	H	H	H	H	D_{IN}	A11-8	A7-0
ead Code Data	5V	H	L	H	H	L	L	L	H	H	D_{OUT}	A11-8	A7-0
/rite Lock Bit 1	5V	H	L	(3)	12V	H	H	H	H	H	X	X	X
/rite Lock Bit 2	5V	H	L	(3)	12V	H	H	H	L	L	X	X	X
/rite Lock Bit 3	5V	H	L	(3)	12V	H	L	H	H	L	X	X	X
ead Lock Bits , 2, 3	5V	H	L	H	H	H	H	L	H	L	P0.2, P0.3, P0.4	X	X
hip Erase	5V	H	L	(1)	12V	H	L	H	L	L	X	X	X
ead Atmel ID	5V	H	L	H	H	L	L	L	L	L	1EH	0000	00H
ead Device ID	5V	H	L	H	H	L	L	L	L	L	51H	0001	00H
ead Device ID	5V	H	L	H	H	L	L	L	L	L	06H	0010	00H

tes:
1. Each PROG pulse is 200 ns - 500 ns for Chip Erase.
2. Each PROG pulse is 200 ns - 500 ns for Write Code Data.
3. Each PROG pulse is 200 ns - 500 ns for Write Lock Bits.
4. RDY/BSY signal is output on P3.0 during programming.
5. X = don't care.

Figure 4. Programming the Flash Memory (Parallel Mode)

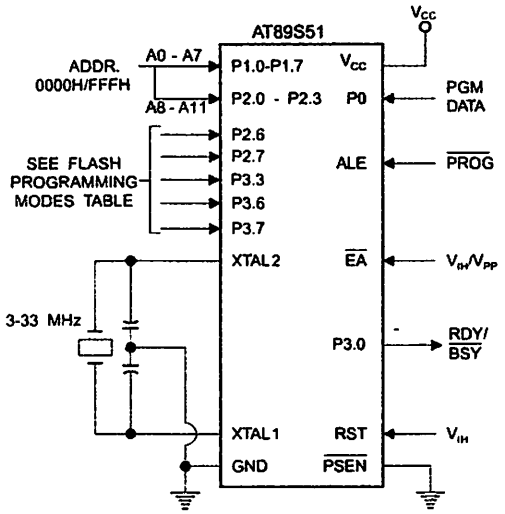
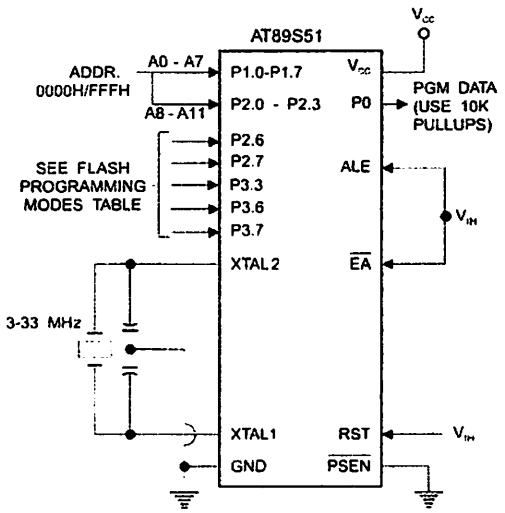


Figure 5. Verifying the Flash Memory (Parallel Mode)

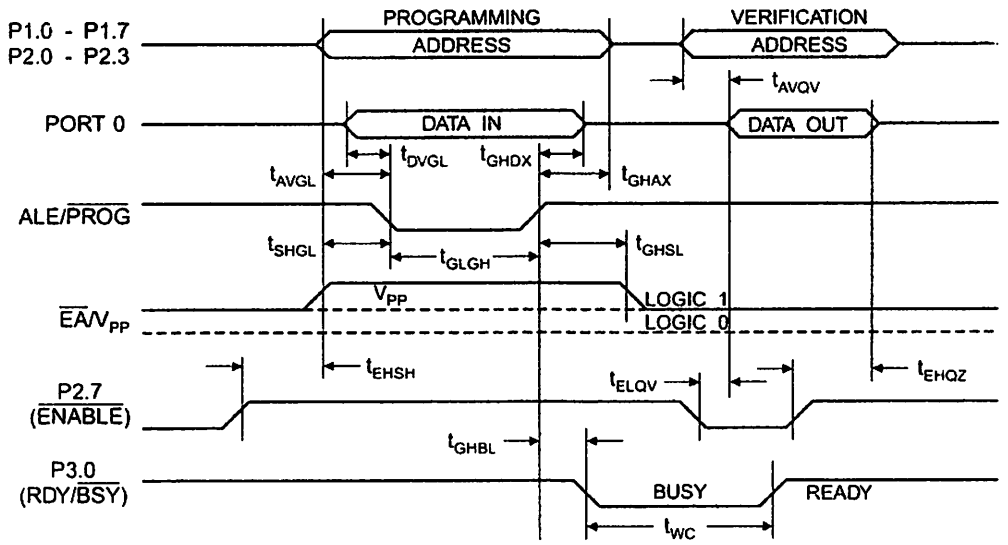


ash Programming and Verification Characteristics (Parallel Mode)

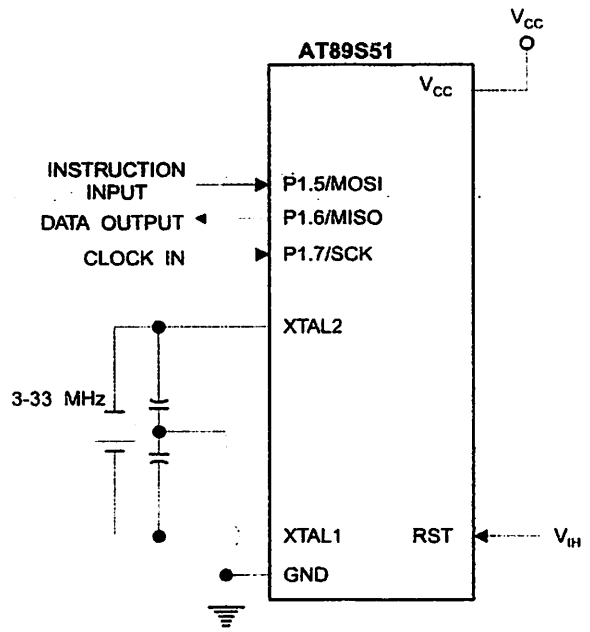
= 20°C to 30°C, V_{CC} = 4.5 to 5.5V

mbol	Parameter	Min	Max	Units
PP	Programming Supply Voltage	11.5	12.5	V
P	Programming Supply Current		10	mA
C	V_{CC} Supply Current		30	mA
t_{CLCL}	Oscillator Frequency	3	33	MHz
AVGL	Address Setup to $\overline{PROG}$ Low	$48t_{CLCL}$		
GHAX	Address Hold After $\overline{PROG}$	$48t_{CLCL}$		
DVGL	Data Setup to $\overline{PROG}$ Low	$48t_{CLCL}$		
GHDX	Data Hold After $\overline{PROG}$	$48t_{CLCL}$		
EHSH	P2.7 ($\overline{ENABLE}$) High to V_{PP}	$48t_{CLCL}$		
SHGL	V_{PP} Setup to $\overline{PROG}$ Low	10		µs
GHSL	V_{PP} Hold After $\overline{PROG}$	10		µs
GLGH	$\overline{PROG}$ Width	0.2	1	µs
AVQV	Address to Data Valid		$48t_{CLCL}$	
ELQV	$\overline{ENABLE}$ Low to Data Valid		$48t_{CLCL}$	
EHQZ	Data Float After $\overline{ENABLE}$	0	$48t_{CLCL}$	
GHBL	$\overline{PROG}$ High to $\overline{BUSY}$ Low		1.0	µs
WC	Byte Write Cycle Time		50	µs

ure 6. Flash Programming and Verification Waveforms – Parallel Mode

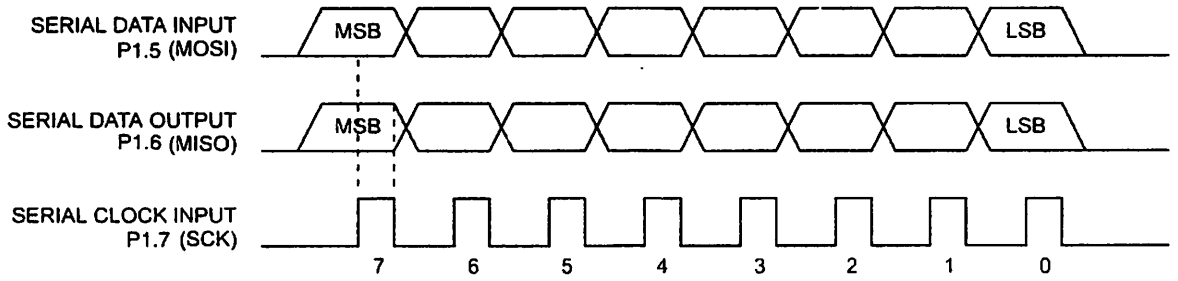


ıre 7. Flash Memory Serial Downloading



ısh Programming and Verification Waveforms – Serial Mode

ıre 8. Serial Programming Waveforms



ble 8. Serial Programming Instruction Set

ıstruction	Instruction Format Byte 1	Byte 2	Byte 3	Byte 4	Operation
'rogramming Enable	1010 1100	0101 0011	xxxx xxxx	xxxx xxxx 0110 1001 (Output)	Enable Serial Programming while RST is high
:hip Erase	1010 1100	100x xxxx	xxxx xxxx	xxxx xxxx	Chip Erase Flash memory array
:ead Program Memory 3yte Mode)	0010 0000	xxxx A11 A10 A9 A8	A7 A6 A5 A4 A3 A2 A1 A0	D7 D6 D5 D4 D3 D2 D1 D0	Read data from Program memory in the byte mode
Vrite Program Memory 3yte Mode)	0100 0000	xxxx A11 A10 A9 A8	A7 A6 A5 A4 A3 A2 A1 A0	D7 D6 D5 D4 D3 D2 D1 D0	Write data to Program memory in the byte mode
Vrite Lock Bits[2]	1010 1100	1110 00 B1 B2	xxxx xxxx	xxxx xxxx	Write Lock bits. See Note (2).
:ead Lock Bits	0010 0100	xxxx xxxx	xxxx xxxx	xx LB3 LB2 LB1 xx	Read back current status of the lock bits (a programmed lock bit reads back as a "1")
:ead Signature Bytes[1]	0010 1000	xxx A5 A4 A3 A2 A1	A0 xxx xxxx	Signature Byte	Read Signature Byte
:ead Program Memory 'age Mode)	0011 0000	xxxx A11 A10 A9 A8	Byte 0	Byte 1... Byte 255	Read data from Program memory in the Page Mode (256 bytes)
Vrite Program Memory 'age Mode)	0101 0000	xxxx A11 A10 A9 A8	Byte 0	Byte 1... Byte 255	Write data to Program memory in the Page Mode (256 bytes)

tes: 1. The signature bytes are not readable in Lock Bit Modes 3 and 4.

2. B1 = 0, B2 = 0 →Mode 1, no lock protection
   B1 = 0, B2 = 1 →Mode 2, lock bit 1 activated
   B1 = 1, B2 = 0 →Mode 3, lock bit 2 activated
   B1 = 1, B1 = 1 →Mode 4, lock bit 3 activated

   } Each of the lock bits needs to be activated sequentially before Mode 4 can be executed.

After Reset signal is high, SCK should be low for at least 64 system clocks before it goes high to clock in the enable data bytes. No pulsing of Reset signal is necessary. SCK should be no faster than 1/16 of the system clock at XTAL1.

For Page Read/Write, the data always starts from byte 0 to 255. After the command byte and upper address byte are latched, each byte thereafter is treated as data until all 256 bytes are shifted in/out. Then the next instruction will be ready to be decoded.

bsolute Maximum Ratings*

perating Temperature	-55°C to +125°C
torage Temperature	-65°C to +150°C
oltage on Any Pin ith Respect to Ground	-1.0V to +7.0V
laximum Operating Voltage	6.6V
C Output Current	15.0 mA

*NOTICE: Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

C Characteristics

e values shown in this table are valid for T_A = -40°C to 85°C and V_{CC} = 4.0V to 5.5V, unless otherwise noted.

ymbol	Parameter	Condition	Min	Max	Units
IL	Input Low Voltage	(Except $\overline{EA}$)	-0.5	0.2 V_{CC}-0.1	V
IL1	Input Low Voltage ($\overline{EA}$)		-0.5	0.2 V_{CC}-0.3	V
IH	Input High Voltage	(Except XTAL1, RST)	0.2 V_{CC}+0.9	V_{CC}+0.5	V
IH1	Input High Voltage	(XTAL1, RST)	0.7 V_{CC}	V_{CC}+0.5	V
OL	Output Low Voltage[1] (Ports 1,2,3)	I_{OL} = 1.6 mA		0.45	V
OL1	Output Low Voltage[1] (Port 0, ALE, $\overline{PSEN}$)	I_{OL} = 3.2 mA		0.45	V
OH	Output High Voltage (Ports 1,2,3, ALE, $\overline{PSEN}$)	I_{OH} = -60 µA, V_{CC} = 5V ± 10%	2.4		V
		I_{OH} = -25 µA	0.75 V_{CC}		V
		I_{OH} = -10 µA	0.9 V_{CC}		V
OH1	Output High Voltage (Port 0 in External Bus Mode)	I_{OH} = -800 µA, V_{CC} = 5V ± 10%	2.4		V
		I_{OH} = -300 µA	0.75 V_{CC}		V
		I_{OH} = -80 µA	0.9 V_{CC}		V
L	Logical 0 Input Current (Ports 1,2,3)	V_{IN} = 0.45V		-50	µA
TL	Logical 1 to 0 Transition Current (Ports 1,2,3)	V_{IN} = 2V, V_{CC} = 5V ± 10%		-650	µA
LI	Input Leakage Current (Port 0, $\overline{EA}$)	0.45 < V_{IN} < V_{CC}		±10	µA
RST	Reset Pulldown Resistor		50	300	KΩ
IO	Pin Capacitance	Test Freq. = 1 MHz, T_A = 25°C		10	pF
CC	Power Supply Current	Active Mode, 12 MHz		25	mA
		Idle Mode, 12 MHz		6.5	mA
	Power-down Mode[2]	V_{CC} = 5.5V		50	µA

tes:
1. Under steady state (non-transient) conditions, I_{OL} must be externally limited as follows:
   Maximum I_{OL} per port pin: 10 mA
   Maximum I_{OL} per 8-bit port:
   Port 0: 26 mA Ports 1, 2, 3: 15 mA
   Maximum total I_{OL} for all output pins: 71 mA
   If I_{OL} exceeds the test condition, V_{OL} may exceed the related specification. Pins are not guaranteed to sink current greater than the listed test conditions.
2. Minimum V_{CC} for Power-down is 2V.

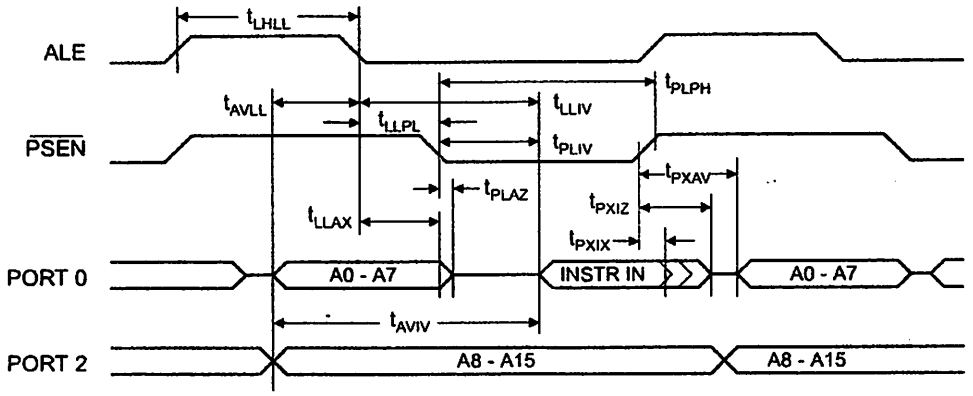
\C Characteristics

nder operating conditions, load capacitance for Port 0, ALE/$\overline{PROG}$, and $\overline{PSEN}$ = 100 pF; load capacitance for all other utputs = 80 pF.

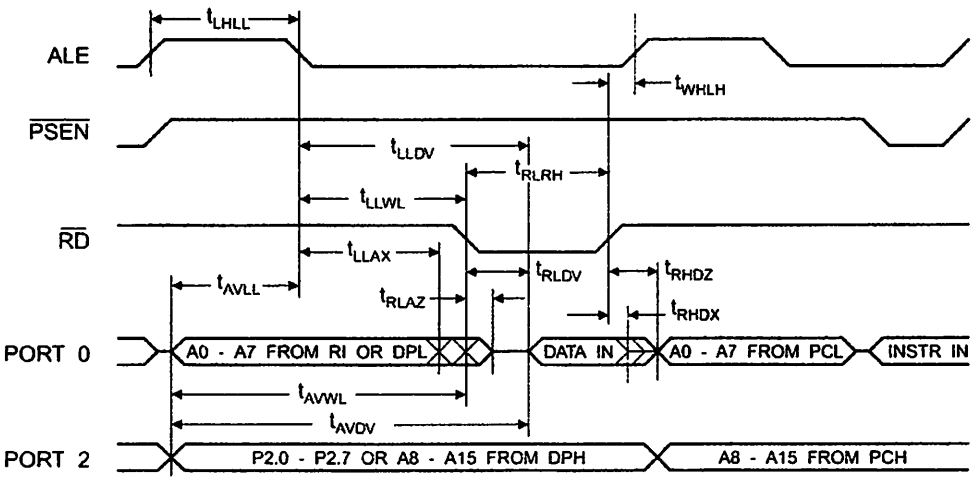
:xternal Program and Data Memory Characteristics

Symbol	Parameter	12 MHz Oscillator		Variable Oscillator		Units
		Min	Max	Min	Max	
$1/t_{CLCL}$	Oscillator Frequency			0	33	MHz
t_{LHLL}	ALE Pulse Width	127		$2t_{CLCL}$-40		ns
t_{AVLL}	Address Valid to ALE Low	43		t_{CLCL}-25		ns
t_{LLAX}	Address Hold After ALE Low	48		t_{CLCL}-25		ns
t_{LLIV}	ALE Low to Valid Instruction In		233		$4t_{CLCL}$-65	ns
t_{LLPL}	ALE Low to $\overline{PSEN}$ Low	43		t_{CLCL}-25		ns
t_{PLPH}	$\overline{PSEN}$ Pulse Width	205		$3t_{CLCL}$-45		ns
t_{PLIV}	$\overline{PSEN}$ Low to Valid Instruction In		145		$3t_{CLCL}$-60	ns
t_{PXIX}	Input Instruction Hold After $\overline{PSEN}$	0		0		ns
t_{PXIZ}	Input Instruction Float After $\overline{PSEN}$		59		t_{CLCL}-25	ns
t_{PXAV}	$\overline{PSEN}$ to Address Valid	75		t_{CLCL}-8		ns
t_{AVIV}	Address to Valid Instruction In		312		$5t_{CLCL}$-80	ns
t_{PLAZ}	$\overline{PSEN}$ Low to Address Float		10		10	ns
t_{RLRH}	$\overline{RD}$ Pulse Width	400		$6t_{CLCL}$-100		ns
t_{WLWH}	$\overline{WR}$ Pulse Width	400		$6t_{CLCL}$-100		ns
t_{RLDV}	$\overline{RD}$ Low to Valid Data In		252		$5t_{CLCL}$-90	ns
t_{RHDX}	Data Hold After $\overline{RD}$	0		0		ns
t_{RHDZ}	Data Float After $\overline{RD}$		97		$2t_{CLCL}$-28	ns
t_{LLDV}	ALE Low to Valid Data In		517		$8t_{CLCL}$-150	ns
t_{AVDV}	Address to Valid Data In		585		$9t_{CLCL}$-165	ns
t_{LLWL}	ALE Low to $\overline{RD}$ or $\overline{WR}$ Low	200	300	$3t_{CLCL}$-50	$3t_{CLCL}$+50	ns
t_{AVWL}	Address to $\overline{RD}$ or $\overline{WR}$ Low	203		$4t_{CLCL}$-75		ns
t_{QVWX}	Data Valid to $\overline{WR}$ Transition	23		t_{CLCL}-30		ns
t_{QVWH}	Data Valid to $\overline{WR}$ High	433		$7t_{CLCL}$-130		ns
t_{WHQX}	Data Hold After $\overline{WR}$	33		t_{CLCL}-25		ns
t_{RLAZ}	$\overline{RD}$ Low to Address Float		0		0	ns
t_{WHLH}	$\overline{RD}$ or $\overline{WR}$ High to ALE High	43	123	t_{CLCL}-25	t_{CLCL}+25	ns

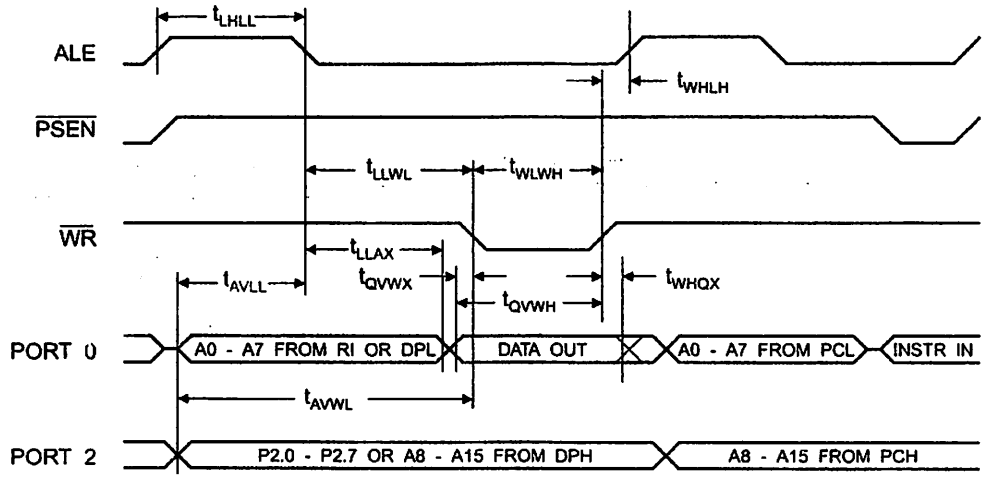
xternal Program Memory Read Cycle



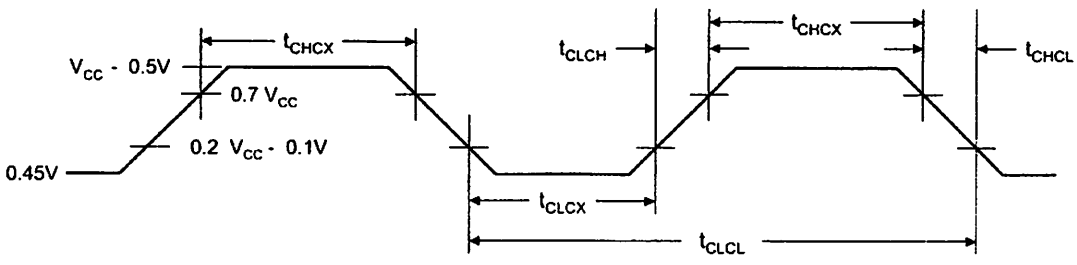
xternal Data Memory Read Cycle



ternal Data Memory Write Cycle



ternal Clock Drive Waveforms



ternal Clock Drive

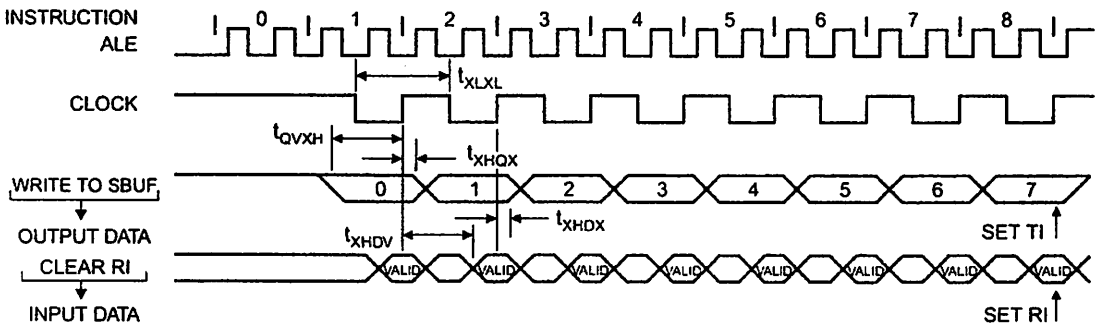
ymbol	Parameter	Min	Max	Units
t_{CLCL}	Oscillator Frequency	0	33	MHz
.CL	Clock Period	30		ns
HCX	High Time	12		ns
.CX	Low Time	12		ns
.CH	Rise Time		5	ns
HCL	Fall Time		5	ns

;erial Port Timing: Shift Register Mode Test Conditions

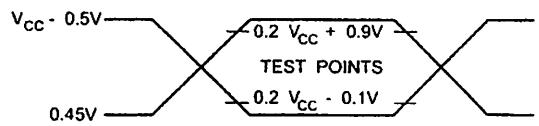
he values in this table are valid for V_{CC} = 4.0V to 5.5V and Load Capacitance = 80 pF.

Symbol	Parameter	12 MHz Osc		Variable Oscillator		Units
		Min	Max	Min	Max	
t_{XLXL}	Serial Port Clock Cycle Time	1.0		$12t_{CLCL}$		µs
t_{QVXH}	Output Data Setup to Clock Rising Edge	700		$10t_{CLCL}$-133		ns
t_{XHQX}	Output Data Hold After Clock Rising Edge	50		$2t_{CLCL}$-80		ns
t_{XHDX}	Input Data Hold After Clock Rising Edge	0		0		ns
t_{XHDV}	Clock Rising Edge to Input Data Valid		700		$10t_{CLCL}$-133	ns

;hift Register Mode Timing Waveforms

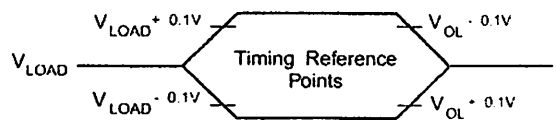


\C Testing Input/Output Waveforms[1]



ote: 1. AC Inputs during testing are driven at V_{CC} - 0.5V for a logic 1 and 0.45V for a logic 0. Timing measurements are made at V_{IH} min. for a logic 1 and V_{IL} max. for a logic 0.

:loat Waveforms[1]



ote: 1. For timing purposes, a port pin is no longer floating when a 100 mV change from load voltage occurs. A port pin begins to float when a 100 mV change from the loaded V_{OH}/V_{OL} level occurs.

rdering Information

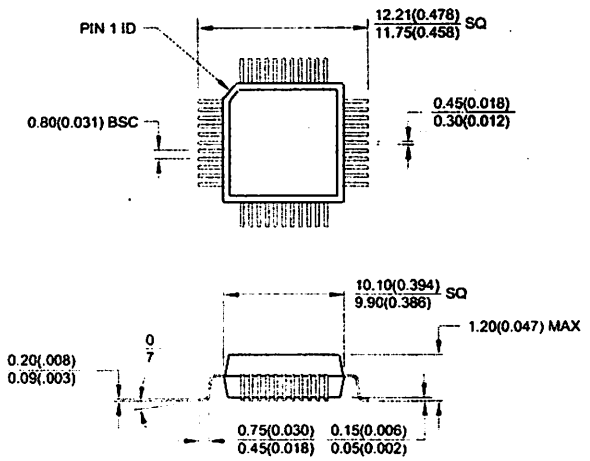
Speed (MHz)	Power Supply	Ordering Code	Package	Operation Range
24	4.0V to 5.5V	AT89S51-24AC AT89S51-24JC AT89S51-24PC	44A 44J 40P6	Commercial (0° C to 70° C)
		AT89S51-24AI AT89S51-24JI AT89S51-24PI	44A 44J 40P6	Industrial (-40° C to 85° C)
33	4.5V to 5.5V	AT89S51-33AC AT89S51-33JC AT89S51-33PC	44A 44J 40P6	Commercial (0° C to 70° C)

= Preliminary Availability

	Package Type
4A	44-lead, Thin Plastic Gull Wing Quad Flatpack (TQFP)
4J	44-lead, Plastic J-leaded Chip Carrier (PLCC)
0P6	40-pin, 0.600" Wide, Plastic Dual Inline Package (PDIP)

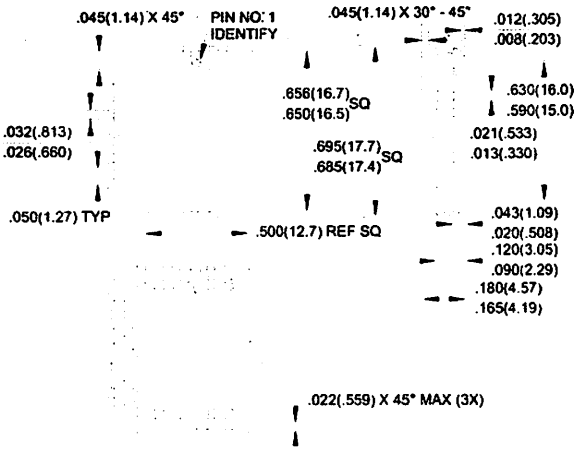
ackaging Information

44A, 44-lead, Thin (1.0 mm) Plastic Gull Wing Quad Flat Package (TQFP)
Dimensions in Millimeters and (Inches)*

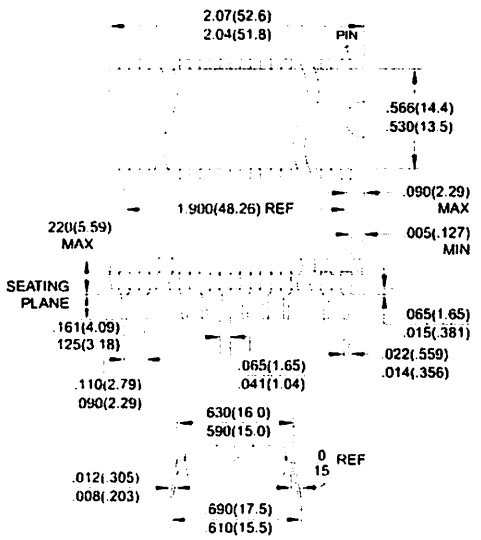


*Controlling dimension: millimeters

44J, 44-lead, Plastic J-leaded Chip Carrier (PLCC)
Dimensions in Inches and (Millimeters)



40P6, 40-pin, 0.600" Wide, Plastic Dual Inline Package (PDIP)
Dimensions in Inches and (Millimeters)
JEDEC STANDARD MS-011 AC



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2487A–10/01/xM

National Semiconductor

August 2000

LM741
Operational Amplifier

General Description

The LM741 series are general purpose operational amplifiers which feature improved performance over industry standards like the LM709. They are direct, plug-in replacements for the 709C, LM201, MC1439 and 748 in most applications.

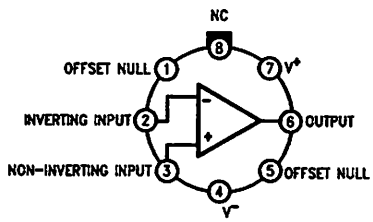
The amplifiers offer many features which make their application nearly foolproof: overload protection on the input and output, no latch-up when the common mode range is exceeded, as well as freedom from oscillations.

The LM741C is identical to the LM741/LM741A except that the LM741C has their performance guaranteed over a 0°C to +70°C temperature range, instead of −55°C to +125°C.

Features

Connection Diagrams

Metal Can Package

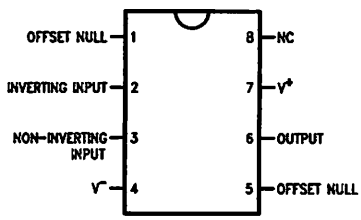


00934102

Note 1: LM741H is available per JM38510/10101

Order Number LM741H, LM741H/883 (Note 1), **LM741AH/883 or LM741CH**
See NS Package Number H08C

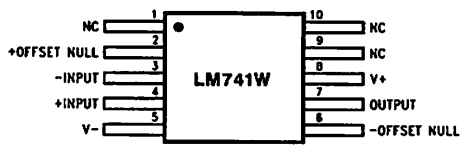
Dual-In-Line or S.O. Package



00934103

Order Number LM741J, LM741J/883, LM741CN
See NS Package Number J08A, M08A or N08E

Ceramic Flatpak

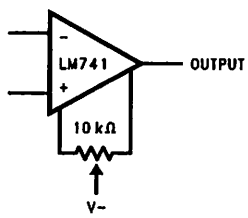


00934106

Order Number LM741W/883
See NS Package Number W10A

Typical Application

Offset Nulling Circuit



00934107

Absolute Maximum Ratings (Note 2)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

(Note 7)

	LM741A	LM741	LM741C
Supply Voltage	±22V	±22V	±18V
Power Dissipation (Note 3)	500 mW	500 mW	500 mW
Differential Input Voltage	±30V	±30V	±30V
Input Voltage (Note 4)	±15V	±15V	±15V
Output Short Circuit Duration	Continuous	Continuous	Continuous
Operating Temperature Range	−55°C to +125°C	−55°C to +125°C	0°C to +70°C
Storage Temperature Range	−65°C to +150°C	−65°C to +150°C	−65°C to +150°C
Junction Temperature	150°C	150°C	100°C
Soldering Information			
N-Package (10 seconds)	260°C	260°C	260°C
J- or H-Package (10 seconds)	300°C	300°C	300°C
M-Package			
Vapor Phase (60 seconds)	215°C	215°C	215°C
Infrared (15 seconds)	215°C	215°C	215°C
See AN-450 "Surface Mounting Methods and Their Effect on Product Reliability" for other methods of soldering surface mount devices.			
ESD Tolerance (Note 8)	400V	400V	400V

Electrical Characteristics (Note 5)

Parameter	Conditions	LM741A			LM741			LM741C			Units
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
Input Offset Voltage	T_A = 25°C										
	$R_S \le 10\ k\Omega$					1.0	5.0		2.0	6.0	mV
	$R_S \le 50\Omega$		0.8	3.0							mV
	$T_{AMIN} \le T_A \le T_{AMAX}$										
	$R_S \le 50\Omega$			4.0							mV
	$R_S \le 10\ k\Omega$						6.0			7.5	mV
Average Input Offset Voltage Drift				15							µV/°C
Input Offset Voltage Adjustment Range	T_A = 25°C, V_S = ±20V	±10				±15			±15		mV
Input Offset Current	T_A = 25°C		3.0	30		20	200		20	200	nA
	$T_{AMIN} \le T_A \le T_{AMAX}$			70		85	500			300	nA
Average Input Offset Current Drift				0.5							nA/°C
Input Bias Current	T_A = 25°C		30	80		80	500		80	500	nA
	$T_{AMIN} \le T_A \le T_{AMAX}$			0.210			1.5			0.8	µA
Input Resistance	T_A = 25°C, V_S = ±20V	1.0	6.0		0.3	2.0		0.3	2.0		MΩ
	$T_{AMIN} \le T_A \le T_{AMAX}$, V_S = ±20V	0.5									MΩ
Input Voltage Range	T_A = 25°C							±12	±13		V
	$T_{AMIN} \le T_A \le T_{AMAX}$				±12	±13					V

Electrical Characteristics (Note 5) (Continued)

Parameter	Conditions	LM741A			LM741			LM741C			Units
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
arge Signal Voltage Gain	T_A = 25°C, $R_L \geq 2$ kΩ										
	V_S = ±20V, V_O = ±15V	50									V/mV
	V_S = ±15V, V_O = ±10V				50	200		20	200		V/mV
	$T_{AMIN} \leq T_A \leq T_{AMAX}$, $R_L \geq 2$ kΩ,										
	V_S = ±20V, V_O = ±15V	32									V/mV
	V_S = ±15V, V_O = ±10V				25			15			V/mV
	V_S = ±5V, V_O = ±2V	10									V/mV
utput Voltage Swing	V_S = ±20V										
	$R_L \geq 10$ kΩ	±16									V
	$R_L \geq 2$ kΩ	±15									V
	V_S = ±15V										
	$R_L \geq 10$ kΩ				±12	±14		±12	±14		V
	$R_L \geq 2$ kΩ				±10	±13		±10	±13		V
utput Short Circuit	T_A = 25°C	10	25	35		25			25		mA
urrent	$T_{AMIN} \leq T_A \leq T_{AMAX}$	10		40							mA
ommon-Mode	$T_{AMIN} \leq T_A \leq T_{AMAX}$										
ejection Ratio	$R_S \leq 10$ kΩ, V_{CM} = ±12V				70	90		70	90		dB
	$R_S \leq 50$Ω, V_{CM} = ±12V	80	95								dB
upply Voltage Rejection	$T_{AMIN} \leq T_A \leq T_{AMAX}$,										
atio	V_S = ±20V to V_S = ±5V										
	$R_S \leq 50$Ω	86	96								dB
	$R_S \leq 10$ kΩ				77	96		77	96		dB
ransient Response	T_A = 25°C, Unity Gain										
Rise Time			0.25	0.8		0.3			0.3		µs
Overshoot			6.0	20		5			5		%
andwidth (Note 6)	T_A = 25°C	0.437	1.5								MHz
lew Rate	T_A = 25°C, Unity Gain	0.3	0.7			0.5			0.5		V/µs
upply Current	T_A = 25°C					1.7	2.8		1.7	2.8	mA
ower Consumption	T_A = 25°C										
	V_S = ±20V		80	150							mW
	V_S = ±15V					50	85		50	85	mW
LM741A	V_S = ±20V										
	$T_A = T_{AMIN}$			165							mW
	$T_A = T_{AMAX}$			135							mW
LM741	V_S = ±15V										
	$T_A = T_{AMIN}$					60	100				mW
	$T_A = T_{AMAX}$					45	75				mW

Note 2: "Absolute Maximum Ratings" indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is functional, but do not guarantee specific performance limits.

Electrical Characteristics (Note 5) (Continued)

Note 3: For operation at elevated temperatures, these devices must be derated based on thermal resistance, and T_j max. (listed under "Absolute Maximum Ratings"). $T_j = T_A + (\theta_{jA} P_D)$.

Thermal Resistance	Cerdip (J)	DIP (N)	HO8 (H)	SO-8 (M)
θ_{jA} (Junction to Ambient)	100°C/W	100°C/W	170°C/W	195°C/W
θ_{jC} (Junction to Case)	N/A	N/A	25°C/W	N/A

Note 4: For supply voltages less than ±15V, the absolute maximum input voltage is equal to the supply voltage.

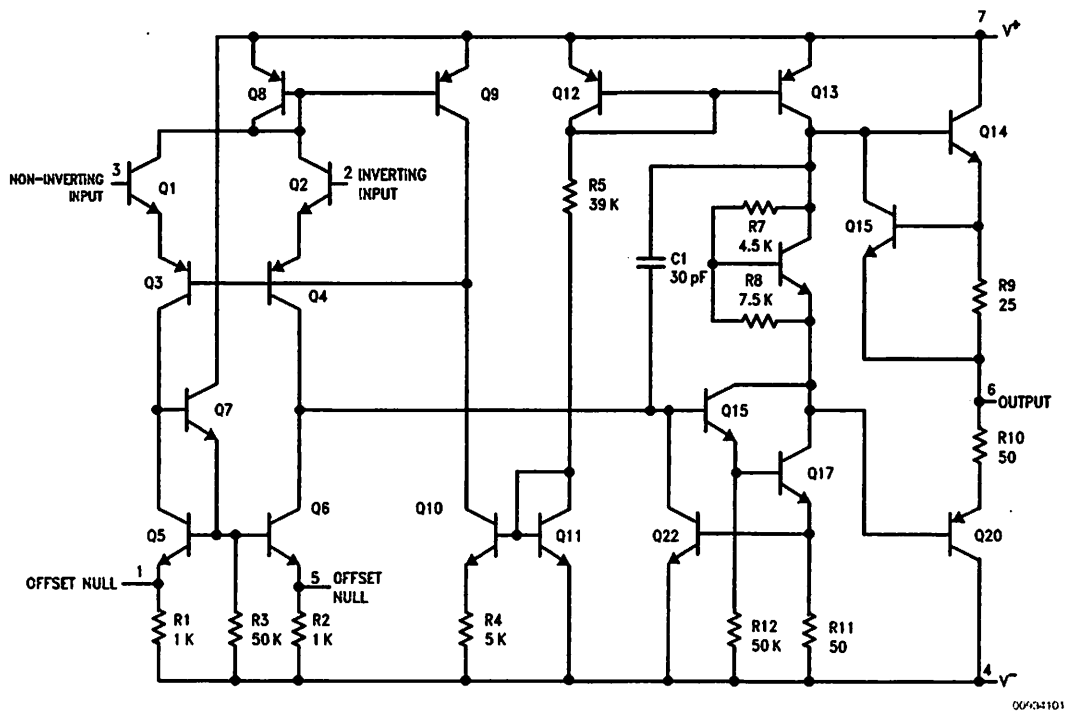
Note 5: Unless otherwise specified, these specifications apply for V_S = ±15V, −55°C ≤ T_A ≤ +125°C (LM741/LM741A). For the LM741C/LM741E, these specifications are limited to 0°C ≤ T_A ≤ +70°C.

Note 6: Calculated value from: BW (MHz) = 0.35/Rise Time(μs).

Note 7: For military specifications see RETS741X for LM741 and RETS741AX for LM741A.

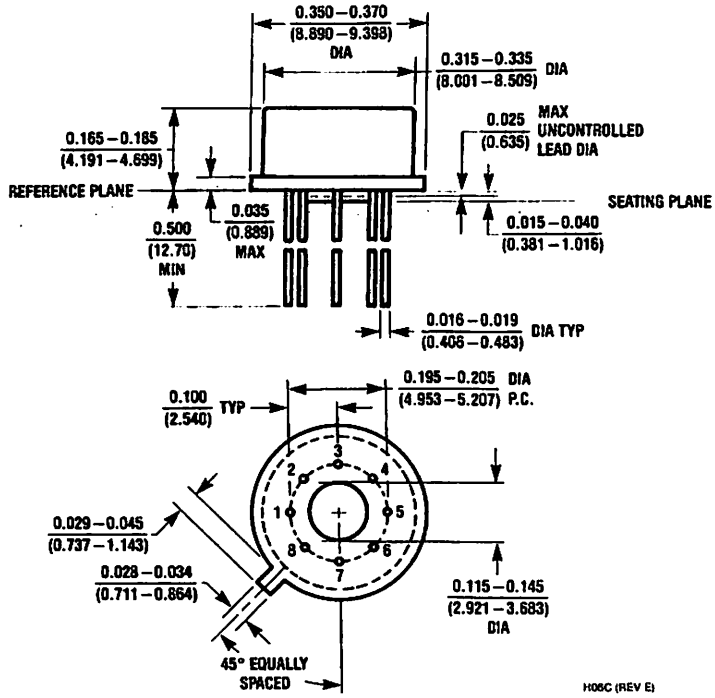
Note 8: Human body model, 1.5 kΩ in series with 100 pF.

Schematic Diagram



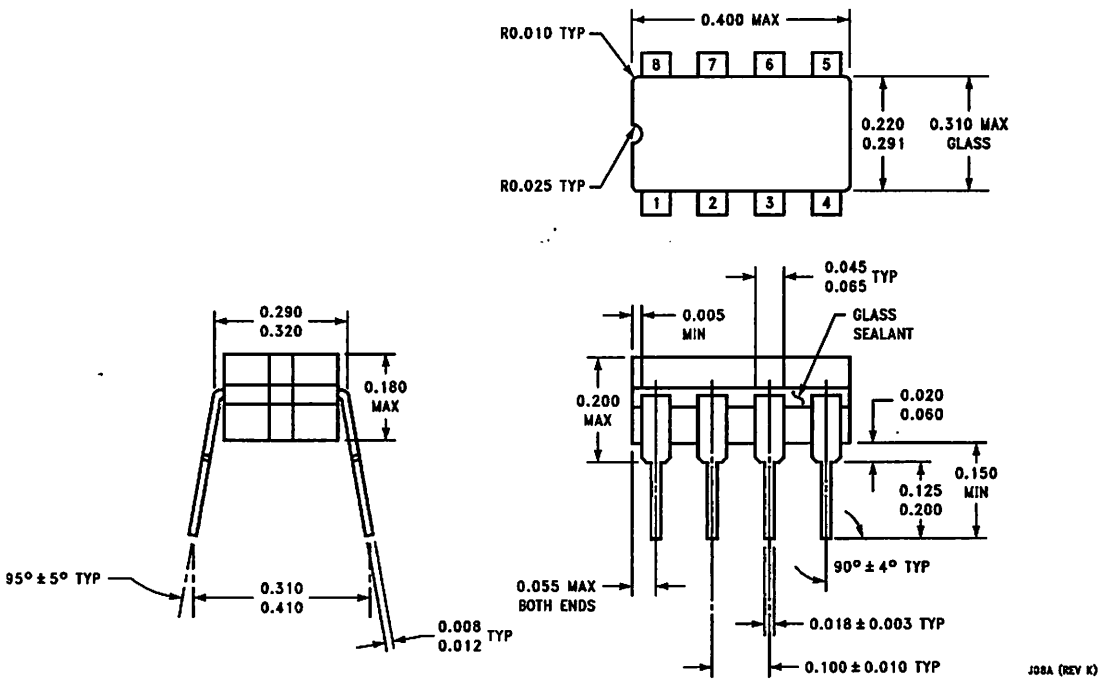
Physical Dimensions inches (millimeters)

unless otherwise noted

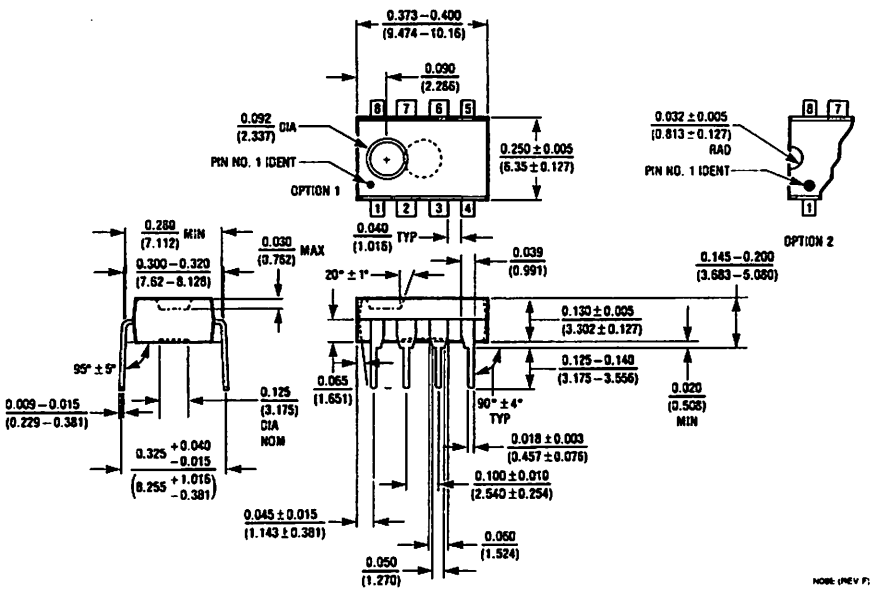


Metal Can Package (H)
Order Number LM741H, LM741H/883, LM741AH/883, LM741AH-MIL or LM741CH
NS Package Number H08C

Physical Dimensions inches (millimeters) unless otherwise noted (Continued)

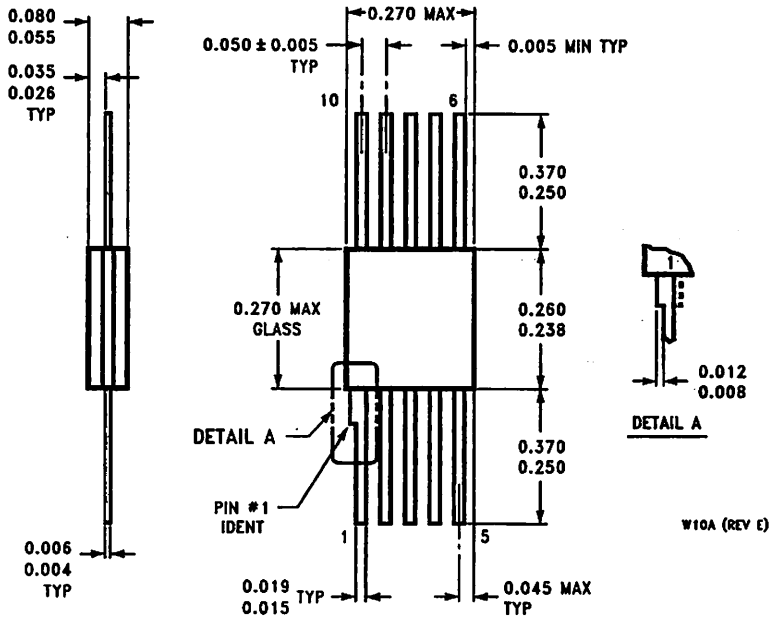


Ceramic Dual-In-Line Package (J)
Order Number LM741J/883
NS Package Number J08A



Dual-In-Line Package (N)
Order Number LM741CN
NS Package Number N08E

Physical Dimensions inches (millimeters) unless otherwise noted (Continued)



10-Lead Ceramic Flatpak (W)
Order Number LM741W/883, LM741WG-MPR or LM741WG/883
NS Package Number W10A

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National Semiconductor

November 1999

ADC0801/ADC0802/ADC0803/ADC0804/ADC0805
8-Bit µP Compatible A/D Converters

General Description

The ADC0801, ADC0802, ADC0803, ADC0804 and ADC0805 are CMOS 8-bit successive approximation A/D converters that use a differential potentiometric ladder—similar to the 256R products. These converters are designed to allow operation with the NSC800 and INS8080A derivative control bus with TRI-STATE output latches directly driving the data bus. These A/Ds appear like memory locations or I/O ports to the microprocessor and no interfacing logic is needed.

Differential analog voltage inputs allow increasing the common-mode rejection and offsetting the analog zero input voltage value. In addition, the voltage reference input can be adjusted to allow encoding any smaller analog voltage span to the full 8 bits of resolution.

Features

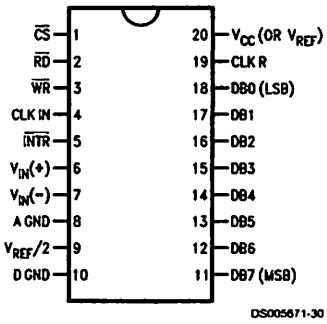
- Compatible with 8080 µP derivatives—no interfacing logic needed - access time - 135 ns
- Easy interface to all microprocessors, or operates "stand alone"
- Differential analog voltage inputs
- Logic inputs and outputs meet both MOS and TTL voltage level specifications
- Works with 2.5V (LM336) voltage reference
- On-chip clock generator
- 0V to 5V analog input voltage range with single 5V supply
- No zero adjust required
- 0.3" standard width 20-pin DIP package
- 20-pin molded chip carrier or small outline package
- Operates ratiometrically or with 5 V_{DC}, 2.5 V_{DC}, or analog span adjusted voltage reference

Key Specifications

- Resolution 8 bits
- Total error ±¼ LSB, ±½ LSB and ±1 LSB
- Conversion time 100 µs

Connection Diagram

ADC080X
Dual-In-Line and Small Outline (SO) Packages



DS005671-30

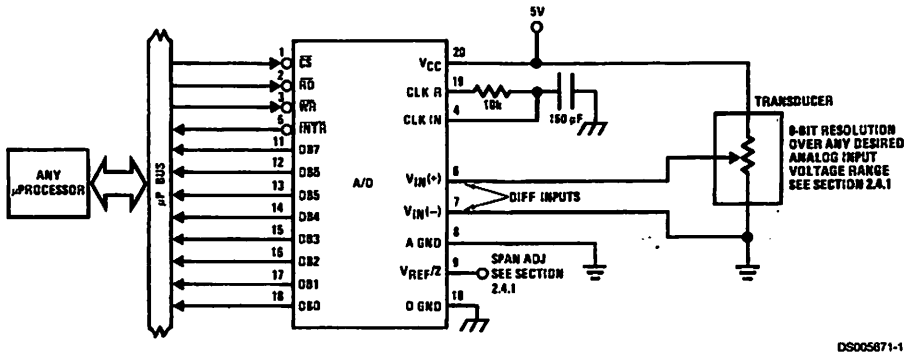
See Ordering Information

Ordering Information

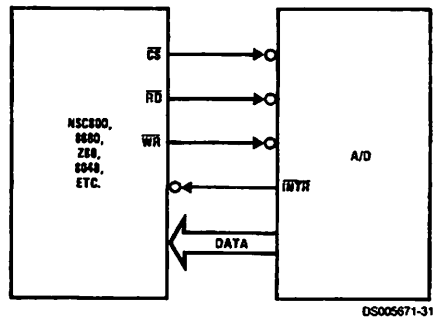
TEMP RANGE		0°C TO 70°C	0°C TO 70°C	−40°C TO +85°C
ERROR	±¼ Bit Adjusted			ADC0801LCN
	±½ Bit Unadjusted	ADC0802LCWM		ADC0802LCN
	±½ Bit Adjusted			ADC0803LCN
	±1Bit Unadjusted	ADC0804LCWM	ADC0804LCN	ADC0805LCN/ADC0804LCJ
PACKAGE OUTLINE		M20B—Small Outline	N20A—Molded DIP	

Z-80® is a registered trademark of Zilog Corp.

Typical Applications



8080 Interface



Error Specification (Includes Full-Scale, Zero Error, and Non-Linearity)			
Part Number	Full-Scale Adjusted	$V_{REF}/2$=2.500 V_{DC} (No Adjustments)	$V_{REF}/2$=No Connection (No Adjustments)
ADC0801	±¼ LSB		
ADC0802		±½ LSB	
ADC0803	±½ LSB		
ADC0804		±1 LSB	
ADC0805			±1 LSB

Absolute Maximum Ratings (Notes 1, 2)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Supply Voltage (V_{CC}) (Note 3)	6.5V
Voltage	
Logic Control Inputs	−0.3V to +18V
At Other Input and Outputs	−0.3V to (V_{CC}+0.3V)
Lead Temp. (Soldering, 10 seconds)	
Dual-In-Line Package (plastic)	260°C
Dual-In-Line Package (ceramic)	300°C
Surface Mount Package	
Vapor Phase (60 seconds)	215°C
Infrared (15 seconds)	220°C
Storage Temperature Range	−65°C to +150°C
Package Dissipation at T_A=25°C	875 mW
ESD Susceptibility (Note 10)	800V

Operating Ratings (Notes 1, 2)

Temperature Range	$T_{MIN} \le T_A \le T_{MAX}$
ADC0804LCJ	−40°C≤T_A≤+85°C
ADC0801/02/03/05LCN	−40°C≤T_A≤+85°C
ADC0804LCN	0°C≤T_A≤+70°C
ADC0802/04LCWM	0°C≤T_A≤+70°C
Range of V_{CC}	4.5 V_{DC} to 6.3 V_{DC}

Electrical Characteristics

The following specifications apply for V_{CC}=5 V_{DC}, $T_{MIN} \le T_A \le T_{MAX}$ and f_{CLK}=640 kHz unless otherwise specified.

Parameter	Conditions	Min	Typ	Max	Units
ADC0801: Total Adjusted Error (Note 8)	With Full-Scale Adj. (See Section 2.5.2)			±¼	LSB
ADC0802: Total Unadjusted Error (Note 8)	V_{REF}/2=2.500 V_{DC}			±½	LSB
ADC0803: Total Adjusted Error (Note 8)	With Full-Scale Adj. (See Section 2.5.2)			±½	LSB
ADC0804: Total Unadjusted Error (Note 8)	V_{REF}/2=2.500 V_{DC}			±1	LSB
ADC0805: Total Unadjusted Error (Note 8)	V_{REF}/2-No Connection			±1	LSB
V_{REF}/2 Input Resistance (Pin 9)	ADC0801/02/03/05	2.5	8.0		kΩ
	ADC0804 (Note 9)	0.75	1.1		kΩ
Analog Input Voltage Range	(Note 4) V(+) or V(−)	Gnd−0.05		V_{CC}+0.05	V_{DC}
DC Common-Mode Error	Over Analog Input Voltage Range		±1/16	±⅛	LSB
Power Supply Sensitivity	V_{CC}=5 V_{DC} ±10% Over Allowed V_{IN}(+) and V_{IN}(−) Voltage Range (Note 4)		±1/16	±⅛	LSB

AC Electrical Characteristics

The following specifications apply for V_{CC}=5 V_{DC} and $T_{MIN} \le T_A \le T_{MAX}$ unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Units
T_C	Conversion Time	f_{CLK}=640 kHz (Note 6)	103		114	μs
T_C	Conversion Time	(Notes 5, 6)	66		73	$1/f_{CLK}$
f_{CLK}	Clock Frequency	V_{CC}=5V, (Note 5)	100	640	1460	kHz
	Clock Duty Cycle		40		60	%
CR	Conversion Rate in Free-Running Mode	$\overline{INTR}$ tied to $\overline{WR}$ with $\overline{CS}$ =0 V_{DC}, f_{CLK}=640 kHz	8770		9708	conv/s
$t_{W(\overline{WR})L}$	Width of $\overline{WR}$ Input (Start Pulse Width)	$\overline{CS}$ =0 V_{DC} (Note 7)	100			ns
t_{ACC}	Access Time (Delay from Falling Edge of $\overline{RD}$ to Output Data Valid)	C_L=100 pF		135	200	ns
t_{1H}, t_{0H}	TRI-STATE Control (Delay from Rising Edge of $\overline{RD}$ to Hi-Z State)	C_L=10 pF, R_L=10k (See TRI-STATE Test Circuits)		125	200	ns
t_{WI}, t_{RI}	Delay from Falling Edge of $\overline{WR}$ or $\overline{RD}$ to Reset of $\overline{INTR}$			300	450	ns
C_{IN}	Input Capacitance of Logic Control Inputs			5	7.5	pF

AC Electrical Characteristics (Continued)

The following specifications apply for V_{CC}=5 V_{DC} and $T_{MIN} \leq T_A \leq T_{MAX}$ unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Units
C_{OUT}	TRI-STATE Output Capacitance (Data Buffers)			5	7.5	pF
CONTROL INPUTS [Note: CLK IN (Pin 4) is the input of a Schmitt trigger circuit and is therefore specified separately]						
V_{IN} (1)	Logical "1" Input Voltage (Except Pin 4 CLK IN)	V_{CC}=5.25 V_{DC}	2.0		15	V_{DC}
V_{IN} (0)	Logical "0" Input Voltage (Except Pin 4 CLK IN)	V_{CC}=4.75 V_{DC}			0.8	V_{DC}
I_{IN} (1)	Logical "1" Input Current (All Inputs)	V_{IN}=5 V_{DC}		0.005	1	μA_{DC}
I_{IN} (0)	Logical "0" Input Current (All Inputs)	V_{IN}=0 V_{DC}	-1	-0.005		μA_{DC}
CLOCK IN AND CLOCK R						
V_T+	CLK IN (Pin 4) Positive Going Threshold Voltage		2.7	3.1	3.5	V_{DC}
V_T-	CLK IN (Pin 4) Negative Going Threshold Voltage		1.5	1.8	2.1	V_{DC}
V_H	CLK IN (Pin 4) Hysteresis (V_T+)-(V_T-)		0.6	1.3	2.0	V_{DC}
V_{OUT} (0)	Logical "0" CLK R Output Voltage	I_O=360 µA V_{CC}=4.75 V_{DC}			0.4	V_{DC}
V_{OUT} (1)	Logical "1" CLK R Output Voltage	I_O=-360 µA V_{CC}=4.75 V_{DC}	2.4			V_{DC}
DATA OUTPUTS AND $\overline{INTR}$						
V_{OUT} (0)	Logical "0" Output Voltage Data Outputs $\overline{INTR}$ Output	 I_{OUT}=1.6 mA, V_{CC}=4.75 V_{DC} I_{OUT}=1.0 mA, V_{CC}=4.75 V_{DC}			 0.4 0.4	 V_{DC} V_{DC}
V_{OUT} (1)	Logical "1" Output Voltage	I_O=-360 µA, V_{CC}=4.75 V_{DC}	2.4			V_{DC}
V_{OUT} (1)	Logical "1" Output Voltage	I_O=-10 µA, V_{CC}=4.75 V_{DC}	4.5			V_{DC}
I_{OUT}	TRI-STATE Disabled Output Leakage (All Data Buffers)	V_{OUT}=0 V_{DC} V_{OUT}=5 V_{DC}	-3		 3	μA_{DC} μA_{DC}
I_{SOURCE}		V_{OUT} Short to Gnd, T_A=25°C	4.5	6		mA_{DC}
I_{SINK}		V_{OUT} Short to V_{CC}, T_A=25°C	9.0	16		mA_{DC}
POWER SUPPLY						
I_{CC}	Supply Current (Includes Ladder Current) ADC0801/02/03/04LCJ/05 ADC0804LCN/LCWM	f_{CLK}=640 kHz, $V_{REF}/2$=NC, T_A=25°C and $\overline{CS}$ =5V		 1.1 1.9	 1.8 2.5	 mA mA

Note 1: Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. DC and AC electrical specifications do not apply when operating the device beyond its specified operating conditions.

Note 2: All voltages are measured with respect to Gnd, unless otherwise specified. The separate A Gnd point should always be wired to the D Gnd.

Note 3: A zener diode exists, internally, from V_{CC} to Gnd and has a typical breakdown voltage of 7 V_{DC}.

Note 4: For $V_{IN}(-) \geq V_{IN}(+)$ the digital output code will be 0000 0000. Two on-chip diodes are tied to each analog input (see block diagram) which will forward conduct for analog input voltages one diode drop below ground or one diode drop greater than the V_{CC} supply. Be careful, during testing at low V_{CC} levels (4.5V), as high level analog inputs (5V) can cause this input diode to conduct–especially at elevated temperatures, and cause errors for analog inputs near full-scale. The spec allows 50 mV forward bias of either diode. This means that as long as the analog V_{IN} does not exceed the supply voltage by more than 50 mV, the output code will be correct. To achieve an absolute 0 V_{DC} to 5 V_{DC} input voltage range will therefore require a minimum supply voltage of 4.950 V_{DC} over temperature variations, initial tolerance and loading.

Note 5: Accuracy is guaranteed at f_{CLK} = 640 kHz. At higher clock frequencies accuracy can degrade. For lower clock frequencies, the duty cycle limits can be extended so long as the minimum clock high time interval or minimum clock low time interval is no less than 275 ns.

Note 6: With an asynchronous start pulse, up to 8 clock periods may be required before the internal clock phases are proper to start the conversion process. The start request is internally latched, see *Figure 4* and section 2.0.

AC Electrical Characteristics (Continued)

Note 7: The $\overline{CS}$ input is assumed to bracket the $\overline{WR}$ strobe input and therefore timing is dependent on the $\overline{WR}$ pulse width. An arbitrarily wide pulse width will hold the converter in a reset mode and the start of conversion is initiated by the low to high transition of the $\overline{WR}$ pulse (see timing diagrams).

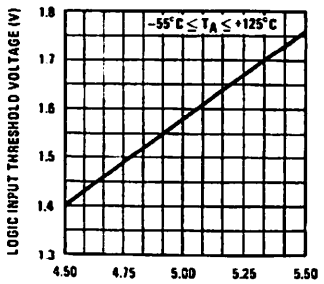
Note 8: None of these A/Ds requires a zero adjust (see section 2.5.1). To obtain zero code at other analog input voltages see section 2.5 and *Figure 7.*

Note 9: The $V_{REF}/2$ pin is the center point of a two-resistor divider connected from V_{CC} to ground. In all versions of the ADC0801, ADC0802, ADC0803, and ADC0805, and in the ADC0804LCJ, each resistor is typically 16 kΩ. In all versions of the ADC0804 except the ADC0804LCJ, each resistor is typically 2.2 kΩ.

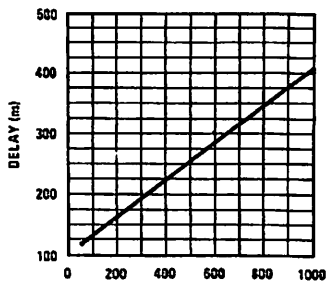
Note 10: Human body model, 100 pF discharged through a 1.5 kΩ resistor.

Typical Performance Characteristics

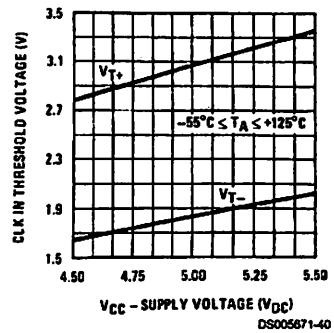
Logic Input Threshold Voltage vs. Supply Voltage



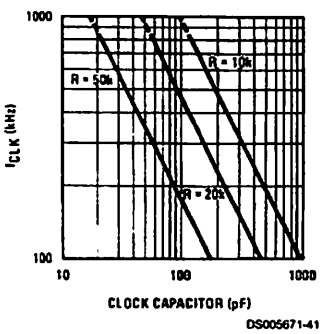
Delay From Falling Edge of RD to Output Data Valid vs. Load Capacitance



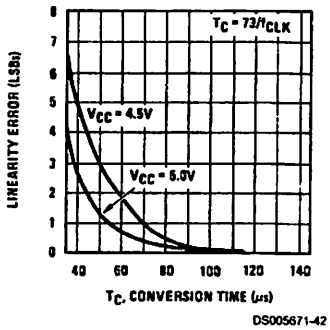
CLK IN Schmitt Trip Levels vs. Supply Voltage



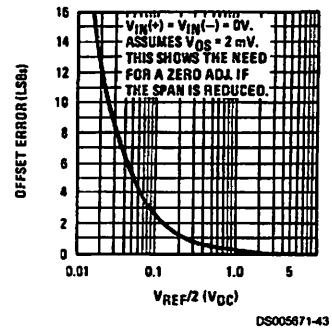
f_{CLK} vs. Clock Capacitor



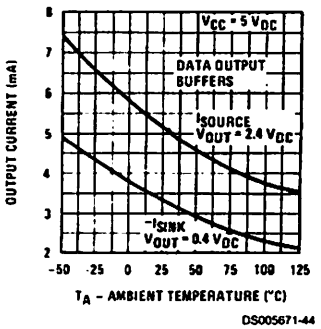
Full-Scale Error vs Conversion Time



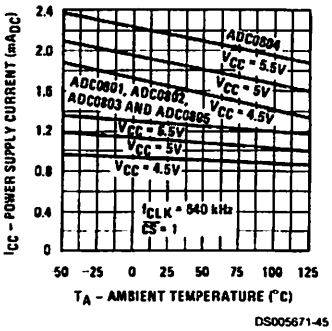
Effect of Unadjusted Offset Error vs. $V_{REF}/2$ Voltage



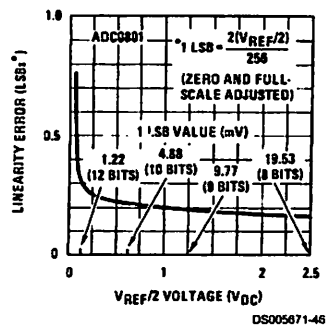
Output Current vs Temperature



Power Supply Current vs Temperature (Note 9)

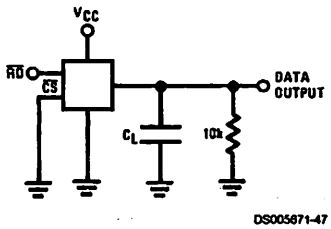


Linearity Error at Low $V_{REF}/2$ Voltages



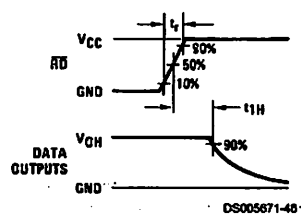
TRI-STATE Test Circuits and Waveforms

t_{1H}



DS005671-47

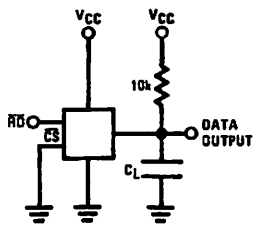
t_{1H}, C_L=10 pF



DS005671-48

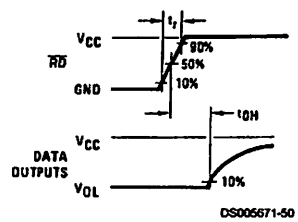
t_r=20 ns

t_{0H}



DS005671-49

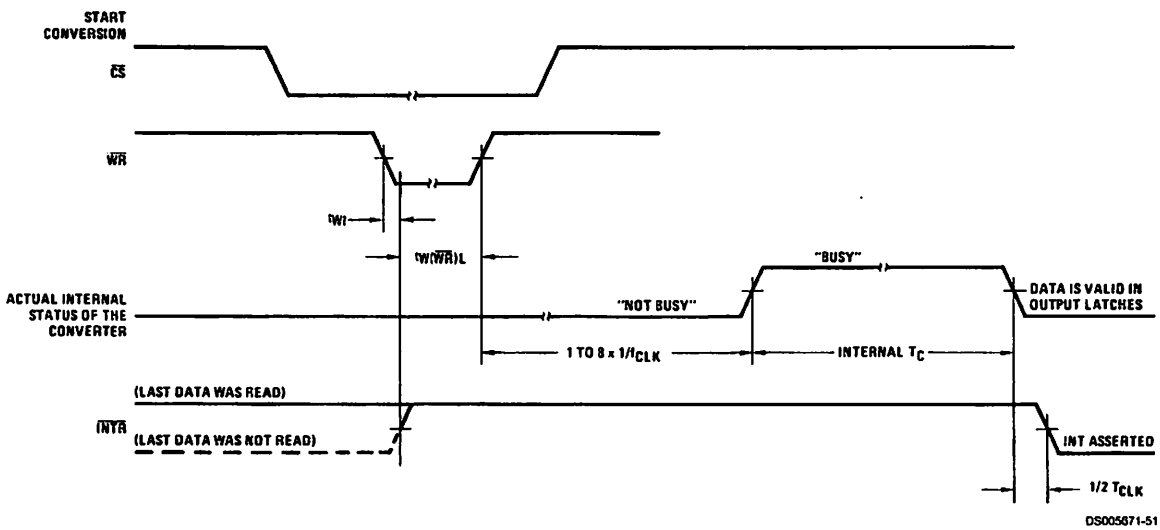
t_{0H}, C_L=10 pF



DS005671-50

t_r=20 ns

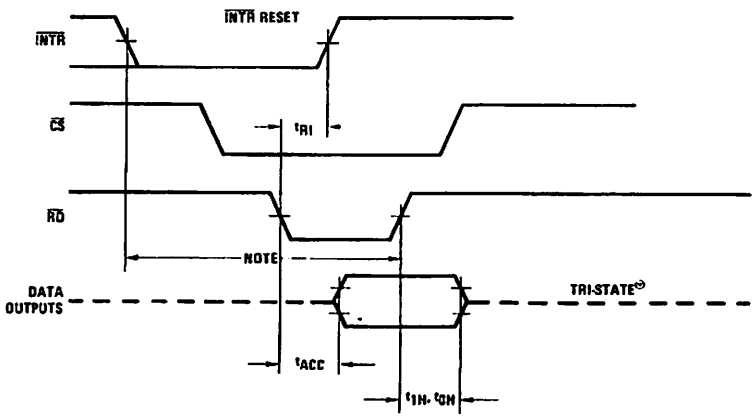
Timing Diagrams (All timing is measured from the 50% voltage points)



DS005671-51

Timing Diagrams (All timing is measured from the 50% voltage points) (Continued)

Output Enable and Reset with $\overline{INTR}$

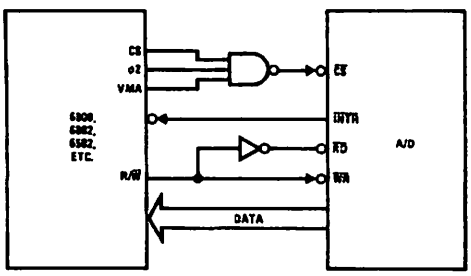


DS005671-52

Note: Read strobe must occur 8 clock periods ($8/f_{CLK}$) after assertion of interrupt to guarantee reset of $\overline{INTR}$.

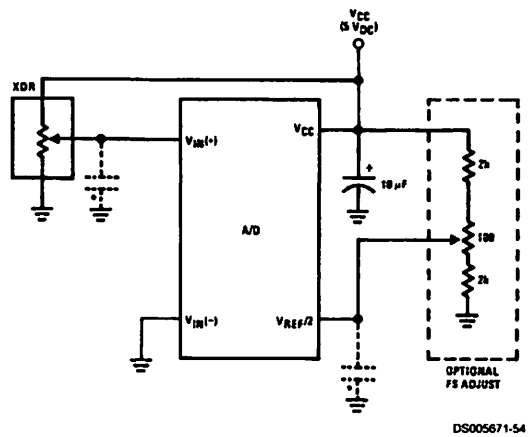
Typical Applications

6800 Interface



DS005671-53

Ratiometeric with Full-Scale Adjust

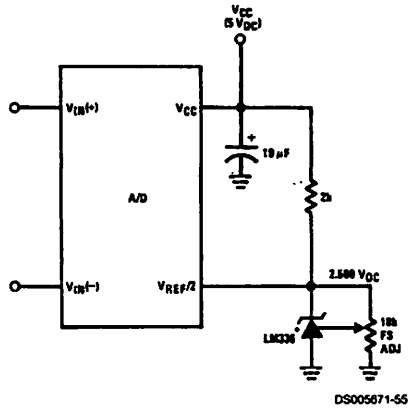


DS005671-54

Note: before using caps at V_{IN} or $V_{REF}/2$, see section 2.3.2 Input Bypass Capacitors.

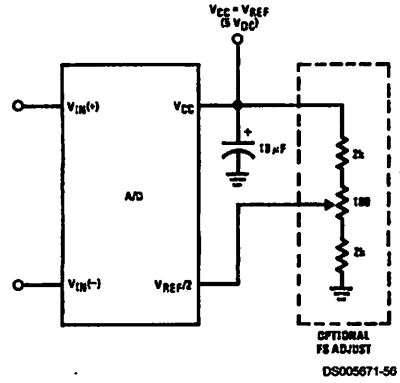
Typical Applications (Continued)

Absolute with a 2.500V Reference

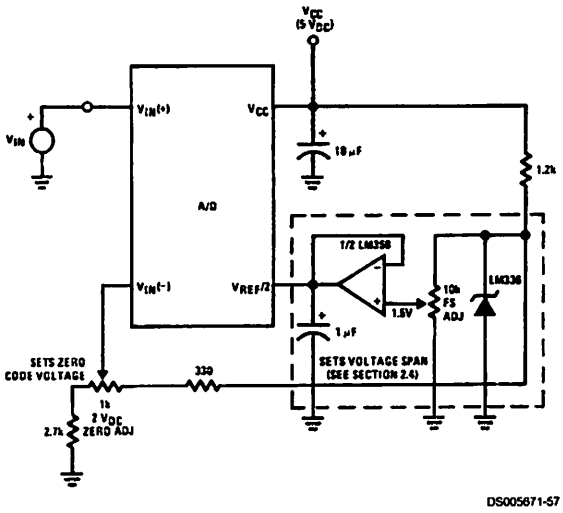


*For low power, see also LM385–2.5

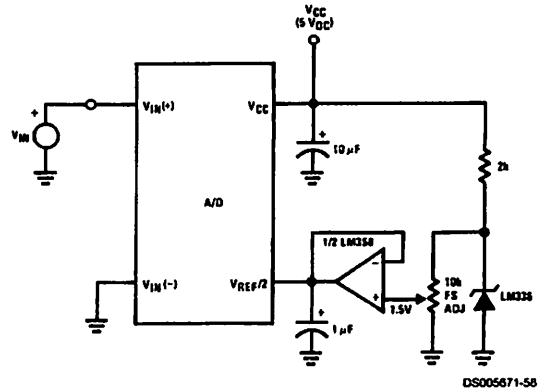
Absolute with a 5V Reference



Zero-Shift and Span Adjust: 2V ≤ V_{IN} ≤ 5V

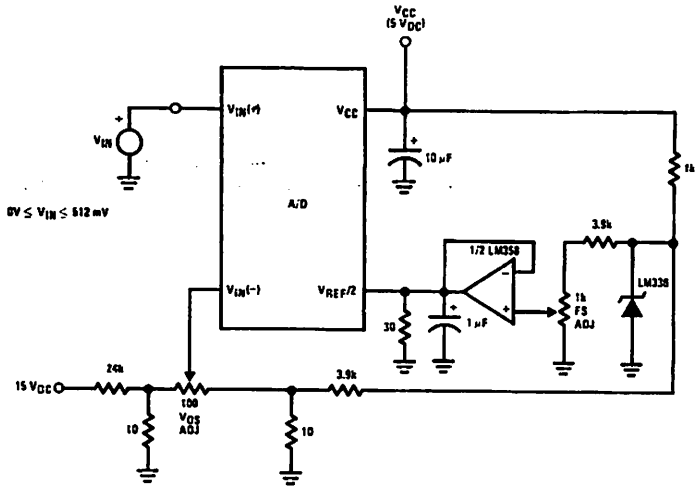


Span Adjust: 0V ≤ V_{IN} ≤ 3V



Typical Applications (Continued)

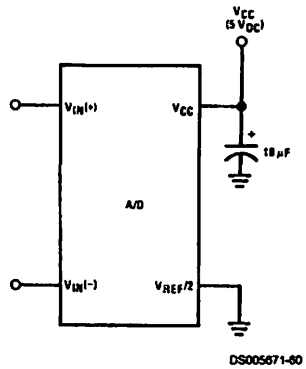
Directly Converting a Low-Level Signal



DS005671-59

$V_{REF}/2$=256 mV

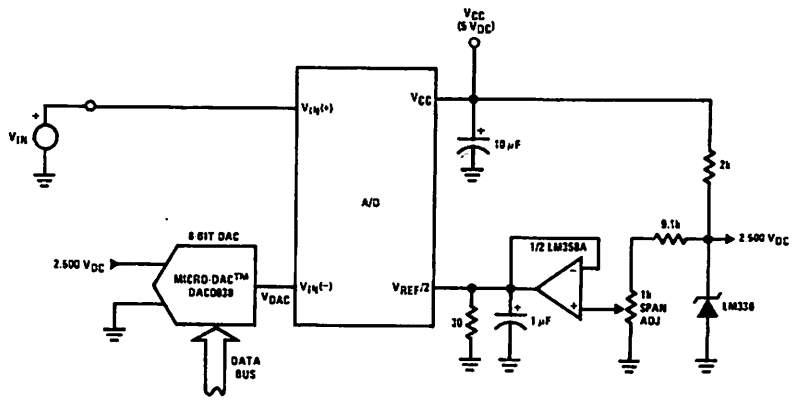
A µP Interfaced Comparator



DS005671-60

For:
$V_{IN}(+) > V_{IN}(-)$
Output=FF_{HEX}
For:
$V_{IN}(+) < V_{IN}(-)$
Output=00_{HEX}

1 mV Resolution with µP Controlled Range

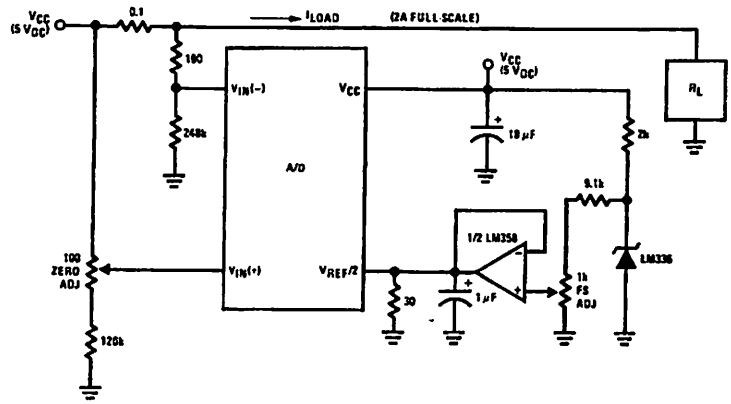


DS005671-61

$V_{REF}/2$=128 mV
1 LSB=1 mV
$V_{DAC} \leq V_{IN} \leq (V_{DAC}+256\ mV)$
$0 \leq V_{DAC} < 2.5V$

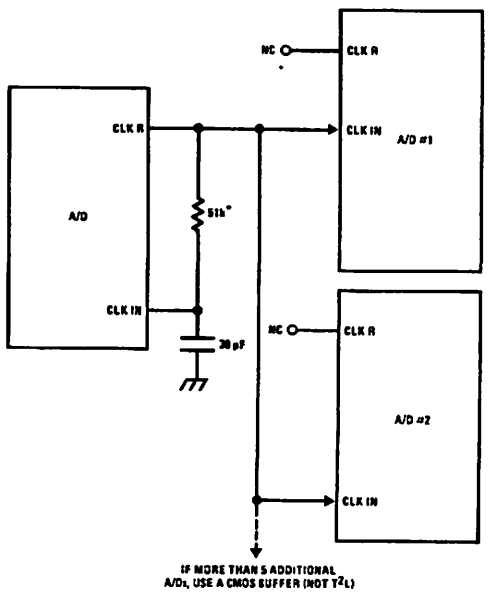
Typical Applications (Continued)

Digitizing a Current Flow



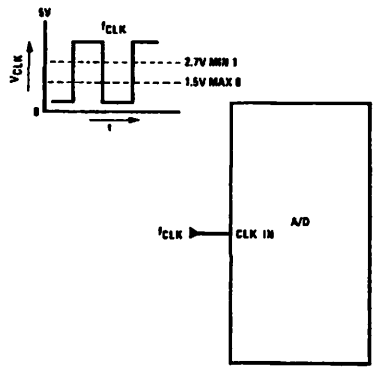
DS005671-62

Self-Clocking Multiple A/Ds



DS005671-63

External Clocking



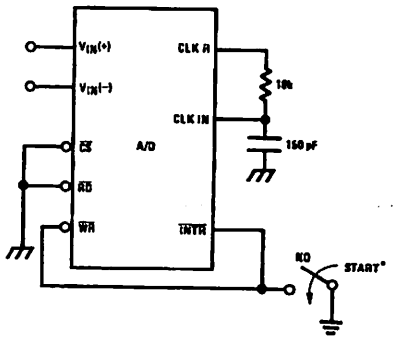
DS005671-64

100 kHz≤f_{CLK}≤1460 kHz

* Use a large R value to reduce loading at CLK R output.

Typical Applications (Continued)

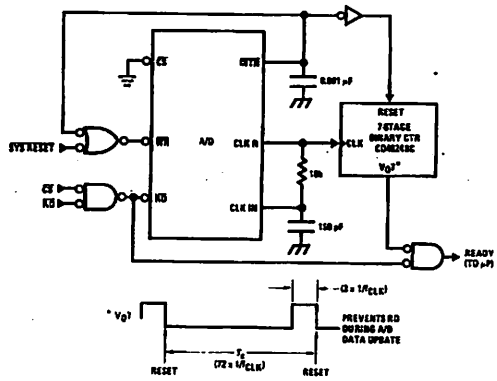
Self-Clocking in Free-Running Mode



DS005671-65

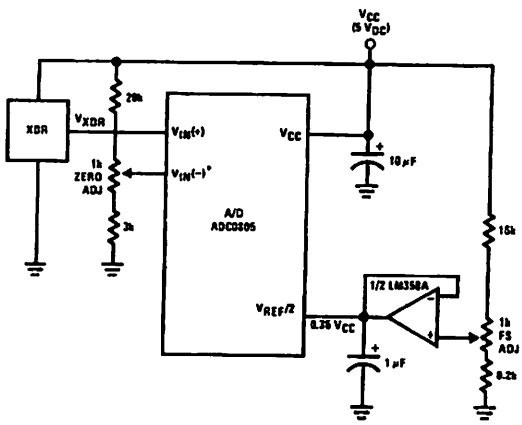
*After power-up, a momentary grounding of the $\overline{WR}$ input is needed to guarantee operation.

µP Interface for Free-Running A/D



DS005671-66

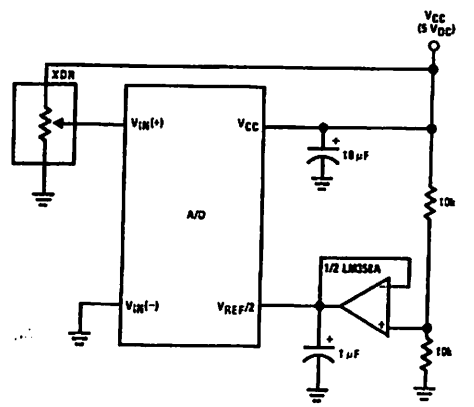
Operating with "Automotive" Ratiometric Transducers



DS005671-67

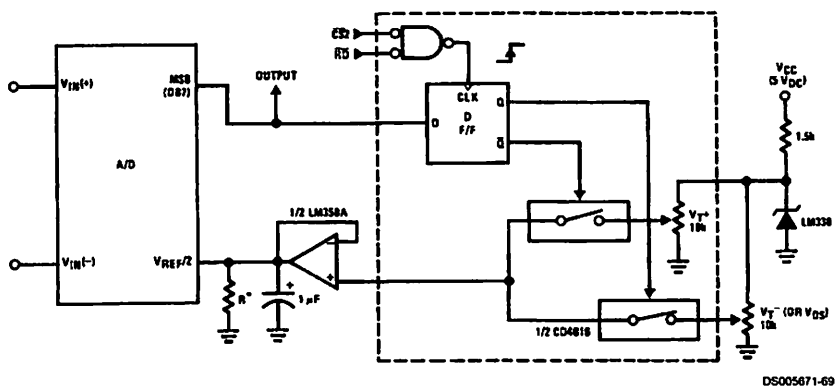
*$V_{IN}(-)$=0.15 V_{CC}
15% of $V_{CC} \leq V_{XDR} \leq 85\%$ of V_{CC}

Ratiometric with $V_{REF}/2$ Forced



DS005671-68

µP Compatible Differential-Input Comparator with Pre-Set V_{OS} (with or without Hysteresis)

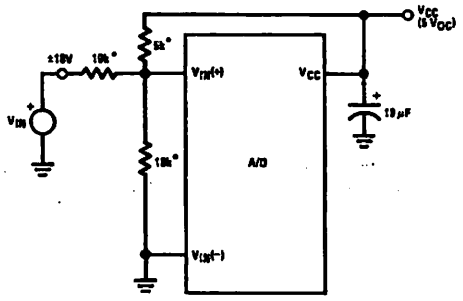


DS005671-69

*See *Figure 5* to select R value
DB7="1" for $V_{IN}(+) > V_{IN}(-)+(V_{REF}/2)$
Omit circuitry within the dotted area if hysteresis is not needed

Typical Applications (Continued)

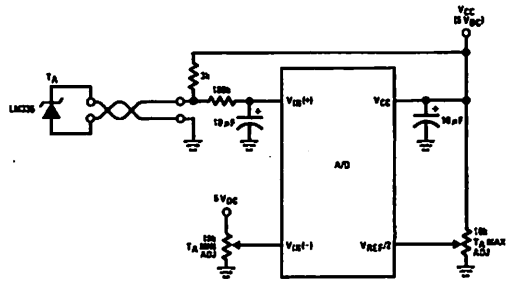
Handling ±10V Analog Inputs



DS005671-70

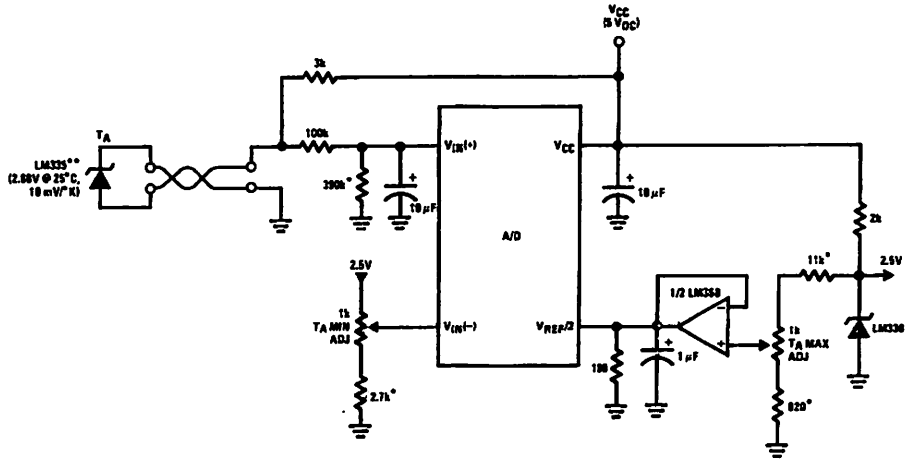
*Beckman Instruments #694-3-R10K resistor array

Low-Cost, µP Interfaced, Temperature-to-Digital Converter



DS005671-71

µP Interfaced Temperature-to-Digital Converter



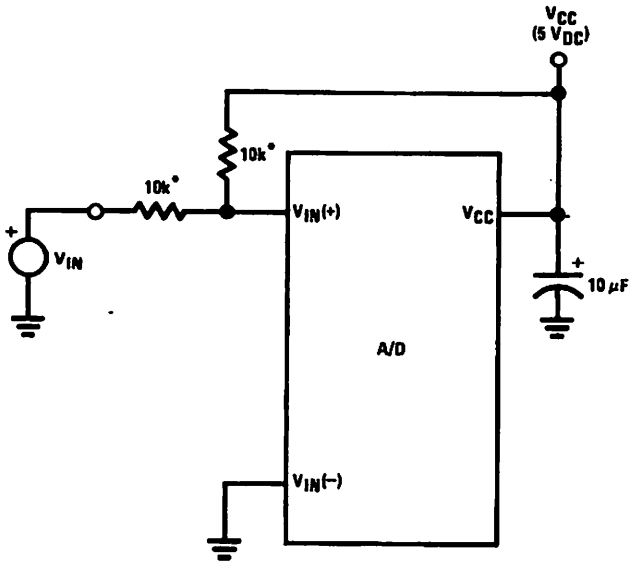
DS005671-72

*Circuit values shown are for 0°C≤T_A≤+128°C

***Can calibrate each sensor to allow easy replacement, then A/D can be calibrated with a pre-set input voltage.

Typical Applications (Continued)

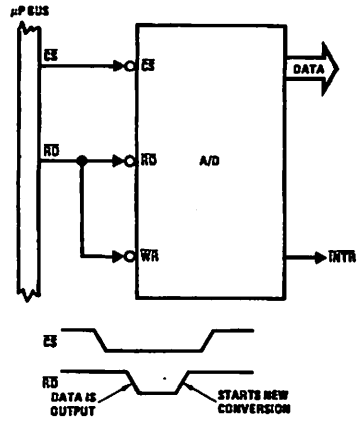
Handling ±5V Analog Inputs



DS005671-33

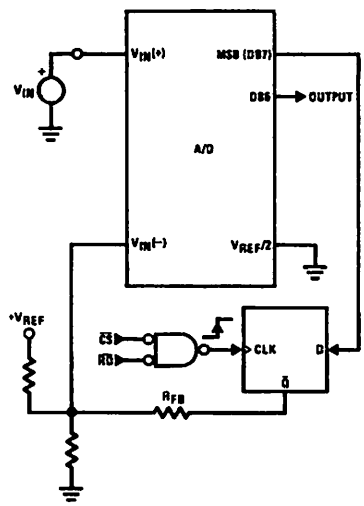
*Beckman Instruments #694-3-R10K resistor array

Read-Only Interface



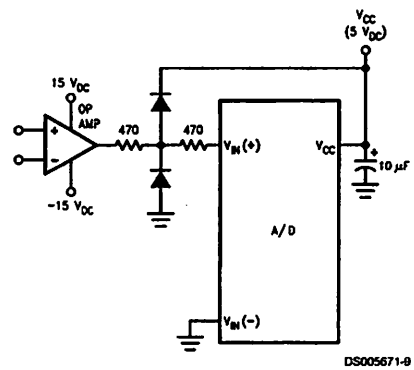
DS005671-34

µP Interfaced Comparator with Hysteresis



DS005671-35

Protecting the Input

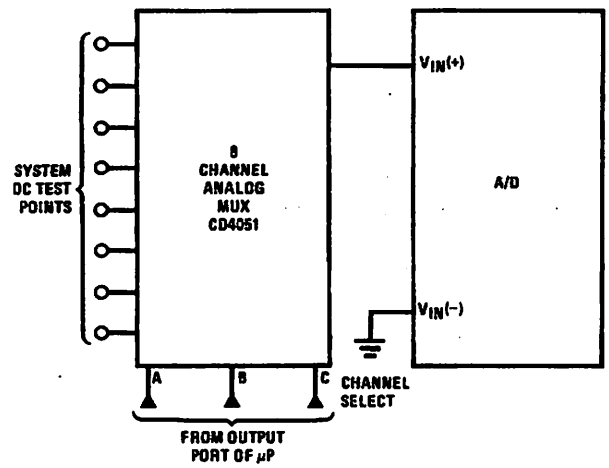


DS005671-9

Diodes are 1N914

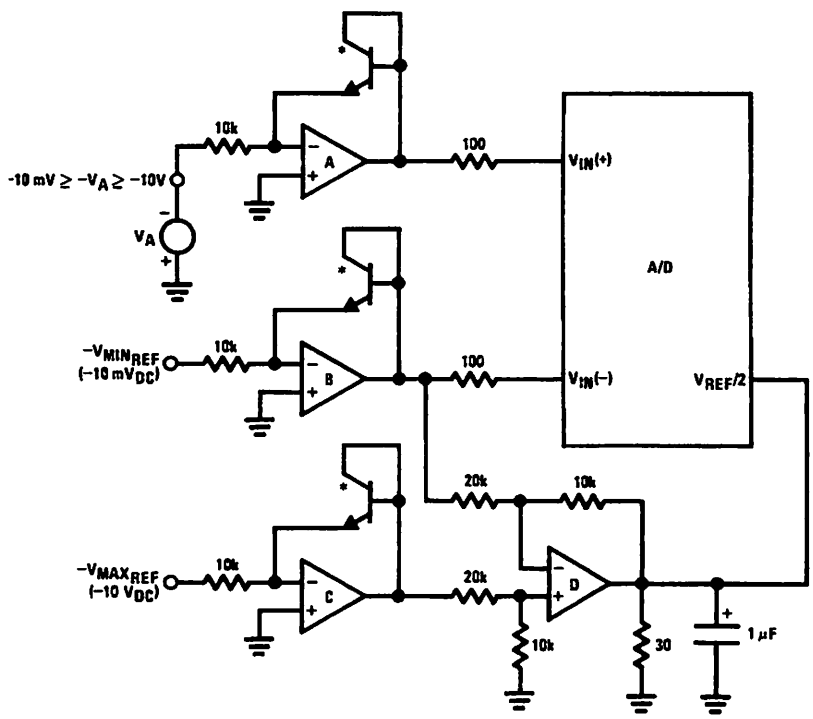
Typical Applications (Continued)

Analog Self-Test for a System



DS005671-36

A Low-Cost, 3-Decade Logarithmic Converter

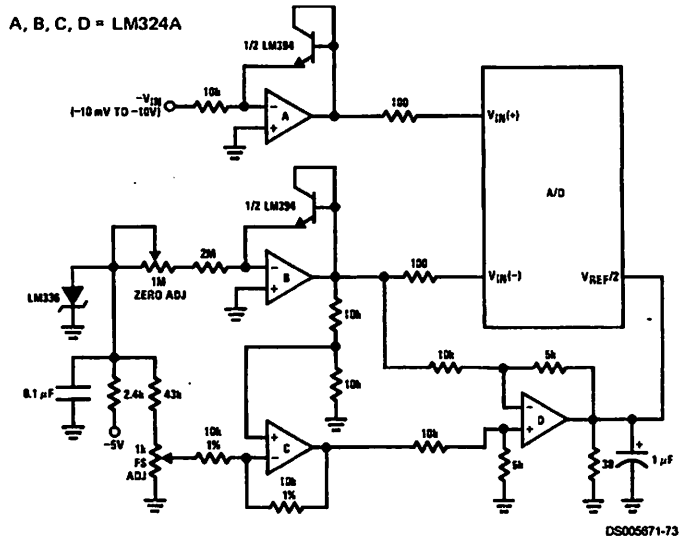


DS005671-37

*LM389 transistors
A, B, C, D = LM324A quad op amp

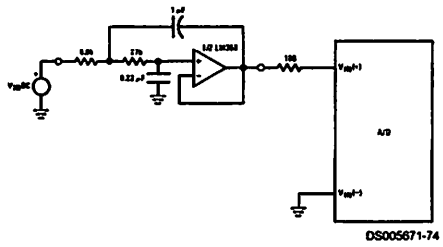
Typical Applications (Continued)

3-Decade Logarithmic A/D Converter



DS005671-73

Noise Filtering the Analog Input



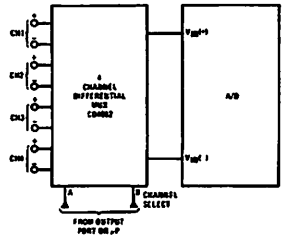
DS005671-74

f_C=20 Hz

Uses Chebyshev implementation for steeper roll-off unity-gain, 2nd order, low-pass filter

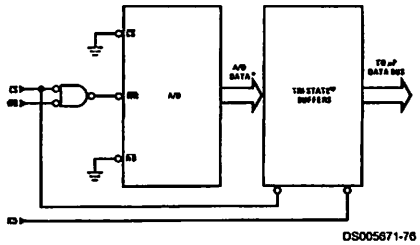
Adding a separate filter for each channel increases system response time if an analog multiplexer is used

Multiplexing Differential Inputs



DS005671-75

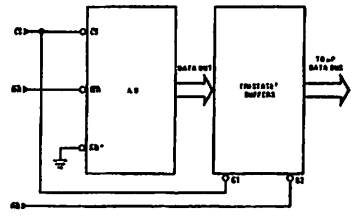
Output Buffers with A/D Data Enabled



DS005671-76

*A/D output data is updated 1 CLK period prior to assertion of $\overline{INTR}$

Increasing Bus Drive and/or Reducing Time on Bus

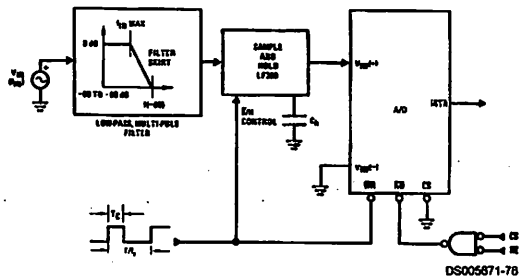


DS005671-77

*Allows output data to set-up at falling edge of $\overline{CS}$

Typical Applications (Continued)

Sampling an AC Input Signal

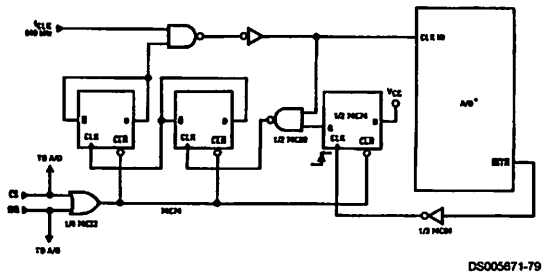


DS005671-78

Note 11: Oversample whenever possible [keep fs > 2f(−60)] to eliminate input frequency folding (aliasing) and to allow for the skirt response of the filter.

Note 12: Consider the amplitude errors which are introduced within the passband of the filter.

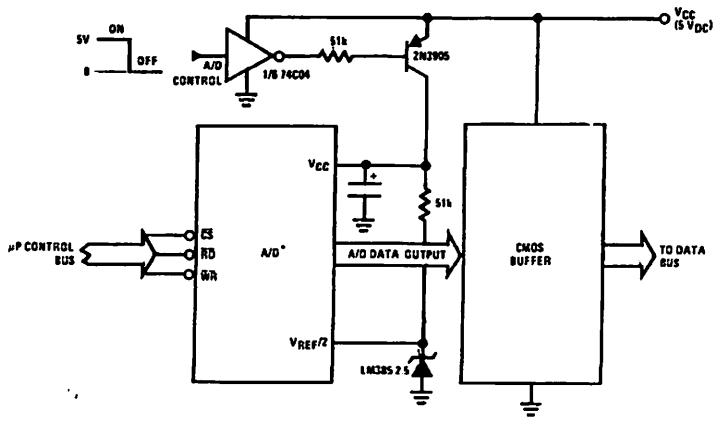
70% Power Savings by Clock Gating



DS005671-79

(Complete shutdown takes ≈ 30 seconds.)

Power Savings by A/D and V_{REF} Shutdown



DS005671-80

*Use ADC0801, 02, 03 or 05 for lowest power consumption.

Note: Logic inputs can be driven to V_{CC} with A/D supply at zero volts.

Buffer prevents data bus from overdriving output of A/D when in shutdown mode.

Functional Description

1.0 UNDERSTANDING A/D ERROR SPECS

A perfect A/D transfer characteristic (staircase waveform) is shown in *Figure 1*. The horizontal scale is analog input voltage and the particular points labeled are in steps of 1 LSB (19.53 mV with 2.5V tied to the $V_{REF}/2$ pin). The digital output codes that correspond to these inputs are shown as D−1, D, and D+1. For the perfect A/D, not only will center-value (A−1, A, A+1, ...) analog inputs produce the correct output digital codes, but also each riser (the transitions between adjacent output codes) will be located ±½ LSB away from each center-value. As shown, the risers are ideal and have no width. Correct digital output codes will be provided for a range of analog input voltages that extend

Functional Description (Continued)

±½ LSB from the ideal center-values. Each tread (the range of analog input voltage that provides the same digital output code) is therefore 1 LSB wide.

Figure 2 shows a worst case error plot for the ADC0801. All center-valued inputs are guaranteed to produce the correct output codes and the adjacent risers are guaranteed to be no closer to the center-value points than ±¼ LSB. In other words, if we apply an analog input equal to the center-value ±¼ LSB, *we guarantee* that the A/D will produce the correct digital code. The maximum range of the position of the code transition is indicated by the horizontal arrow and it is guaranteed to be no more than ½ LSB.

The error curve of *Figure 3* shows a worst case error plot for the ADC0802. Here we guarantee that if we apply an analog input equal to the LSB analog voltage center-value the A/D will produce the correct digital code.

Next to each transfer function is shown the corresponding error plot. Many people may be more familiar with error plots than transfer functions. The analog input voltage to the A/D is provided by either a linear ramp or by the discrete output steps of a high resolution DAC. Notice that the error is continuously displayed and includes the quantization uncertainty of the A/D. For example the error at point 1 of *Figure 1* is +½ LSB because the digital code appeared ½ LSB in advance of the center-value of the tread. The error plots always have a constant negative slope and the abrupt upside steps are always 1 LSB in magnitude.

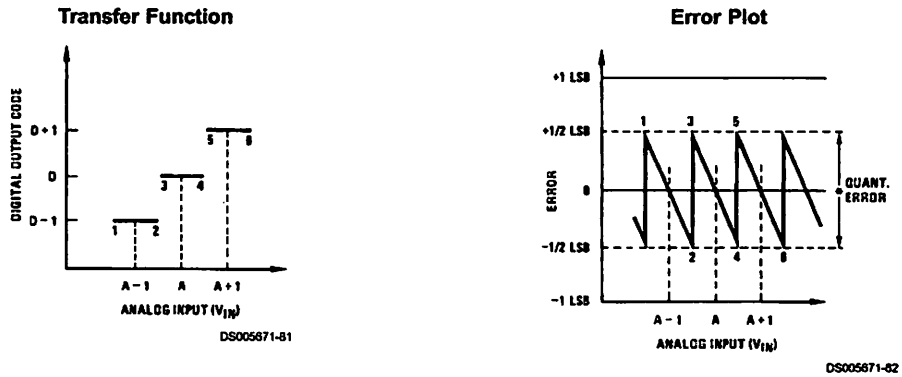


FIGURE 1. Clarifying the Error Specs of an A/D Converter Accuracy=±0 LSB: A Perfect A/D

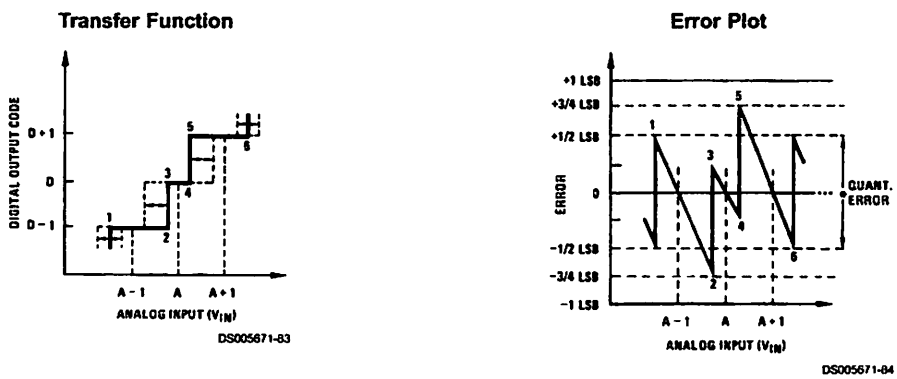


FIGURE 2. Clarifying the Error Specs of an A/D Converter Accuracy=±¼ LSB

Functional Description (Continued)

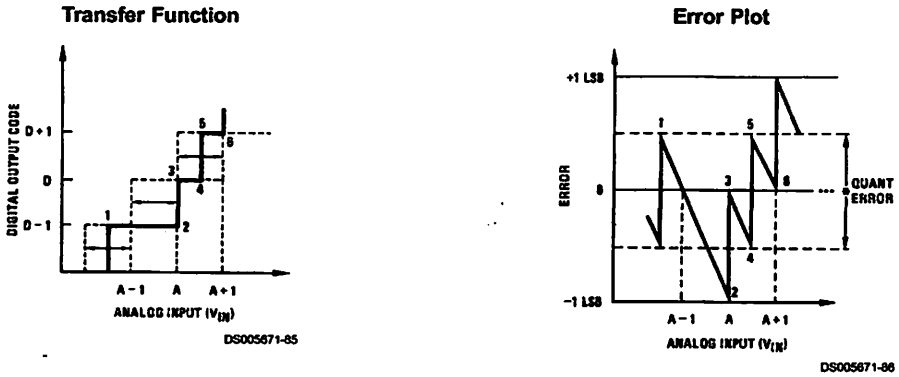


FIGURE 3. Clarifying the Error Specs of an A/D Converter
Accuracy=±½ LSB

2.0 FUNCTIONAL DESCRIPTION

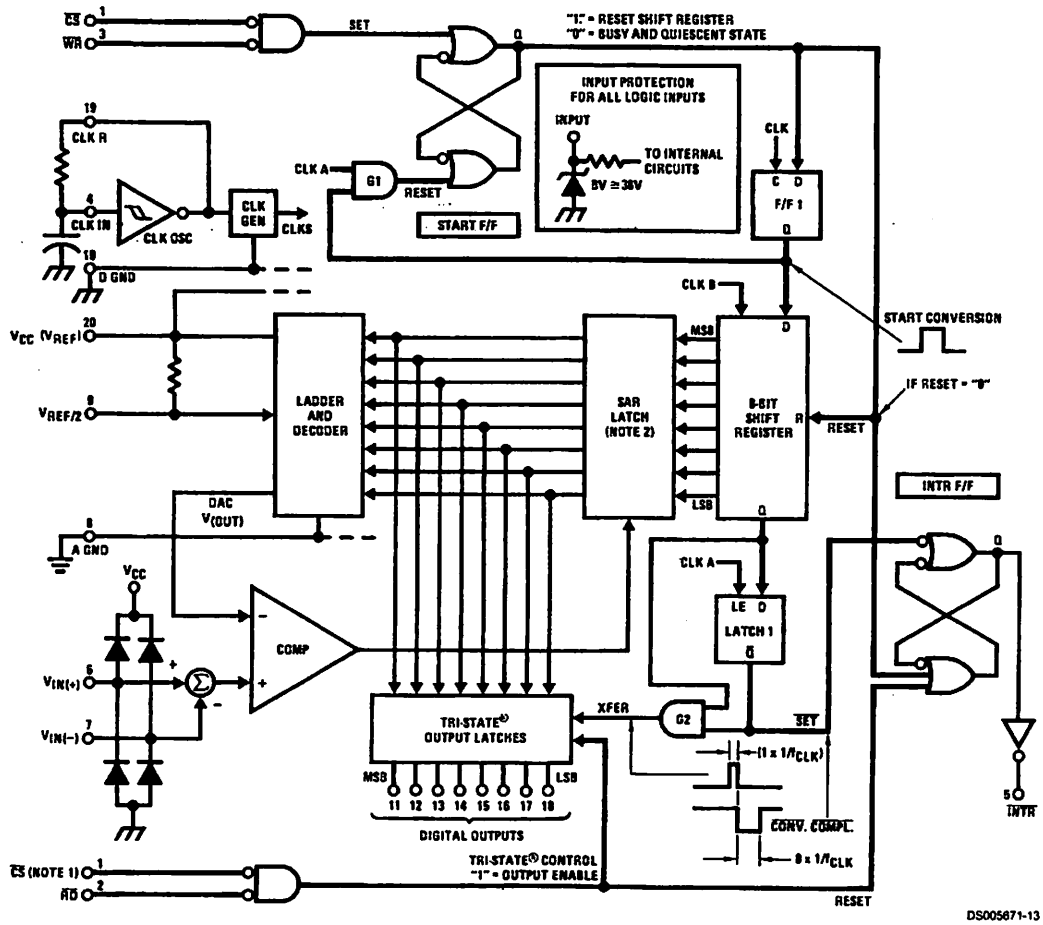
The ADC0801 series contains a circuit equivalent of the 256R network. Analog switches are sequenced by successive approximation logic to match the analog difference input voltage $[V_{IN}(+) - V_{IN}(-)]$ to a corresponding tap on the R network. The most significant bit is tested first and after 8 comparisons (64 clock cycles) a digital 8-bit binary code (1111 1111 = full-scale) is transferred to an output latch and then an interrupt is asserted ($\overline{INTR}$ makes a high-to-low transition). A conversion in process can be interrupted by issuing a second start command. The device may be operated in the free-running mode by connecting $\overline{INTR}$ to the $\overline{WR}$ input with $\overline{CS}$ =0. To ensure start-up under all possible conditions, an external $\overline{WR}$ pulse is required during the first power-up cycle.

On the high-to-low transition of the $\overline{WR}$ input the internal SAR latches and the shift register stages are reset. As long as the $\overline{CS}$ input and $\overline{WR}$ input remain low, the A/D will remain in a reset state. *Conversion will start from 1 to 8 clock periods after at least one of these inputs makes a low-to-high transition.*

A functional diagram of the A/D converter is shown in *Figure 4*. All of the package pinouts are shown and the major logic control paths are drawn in heavier weight lines.

The converter is started by having $\overline{CS}$ and $\overline{WR}$ simultaneously low. This sets the start flip-flop (F/F) and the resulting "1" level resets the 8-bit shift register, resets the Interrupt ($\overline{INTR}$) F/F and inputs a "1" to the D flop, F/F1, which is at the input end of the 8-bit shift register. Internal clock signals then transfer this "1" to the Q output of F/F1. The AND gate, G1, combines this "1" output with a clock signal to provide a reset signal to the start F/F. If the set signal is no longer present (either $\overline{WR}$ or $\overline{CS}$ is a "1") the start F/F is reset and the 8-bit shift register then can have the "1" clocked in, which starts the conversion process. If the set signal were to still be present, this reset pulse would have no effect (both outputs of the start F/F would momentarily be at a "1" level) and the 8-bit shift register would continue to be held in the reset mode. This logic therefore allows for wide $\overline{CS}$ and $\overline{WR}$ signals and the converter will start after at least one of these signals returns high and the internal clocks again provide a reset signal for the start F/F.

Functional Description (Continued)



Note 13: $\overline{CS}$ shown twice for clarity.

Note 14: SAR = Successive Approximation Register.

FIGURE 4. Block Diagram

After the "1" is clocked through the 8-bit shift register (which completes the SAR search) it appears as the input to the D-type latch, LATCH 1. As soon as this "1" is output from the shift register, the AND gate, G2, causes the new digital word to transfer to the TRI-STATE output latches. When LATCH 1 is subsequently enabled, the Q output makes a high-to-low transition which causes the INTR F/F to set. An inverting buffer then supplies the $\overline{INTR}$ input signal.

Note that this $\overline{SET}$ control of the INTR F/F remains low for 8 of the external clock periods (as the internal clocks run at 1/8 of the frequency of the external clock). If the data output is continuously enabled ($\overline{CS}$ and $\overline{RD}$ both held low), the $\overline{INTR}$ output will still signal the end of conversion (by a high-to-low transition), because the $\overline{SET}$ input can control the Q output of the INTR F/F even though the RESET input is constantly at a "1" level in this operating mode. This $\overline{INTR}$ output will therefore stay low for the duration of the $\overline{SET}$ signal, which is 8 periods of the external clock frequency (assuming the A/D is not started during this interval).

When operating in the free-running or continuous conversion mode ($\overline{INTR}$ pin tied to $\overline{WR}$ and $\overline{CS}$ wired low—see also section 2.8), the START F/F is SET by the high-to-low transition of the $\overline{INTR}$ signal. This resets the SHIFT REGISTER which causes the input to the D-type latch, LATCH 1, to go low. As the latch enable input is still present, the $\overline{Q}$ output will go high, which then allows the INTR F/F to be RESET. This reduces the width of the resulting $\overline{INTR}$ output pulse to only a few propagation delays (approximately 300 ns).

When data is to be read, the combination of both $\overline{CS}$ and $\overline{RD}$ being low will cause the INTR F/F to be reset and the TRI-STATE output latches will be enabled to provide the 8-bit digital outputs.

2.1 Digital Control Inputs

The digital control inputs ($\overline{CS}$, $\overline{RD}$, and $\overline{WR}$) meet standard T^2L logic voltage levels. These signals have been renamed when compared to the standard A/D Start and Output Enable labels. In addition, these inputs are active low to allow an easy interface to microprocessor control busses. For non-microprocessor based applications, the $\overline{CS}$ input (pin 1) can be grounded and the standard A/D Start function is obtained by an active low pulse applied at the $\overline{WR}$ input (pin 3) and the Output Enable function is caused by an active low pulse at the $\overline{RD}$ input (pin 2).

Functional Description (Continued)

2.2 Analog Differential Voltage Inputs and Common-Mode Rejection

This A/D has additional applications flexibility due to the analog differential voltage input. The $V_{IN}(-)$ input (pin 7) can be used to automatically subtract a fixed voltage value from the input reading (tare correction). This is also useful in 4 mA–20 mA current loop conversion. In addition, common-mode noise can be reduced by use of the differential input.

The time interval between sampling $V_{IN}(+)$ and $V_{IN}(-)$ is 4-½ clock periods. The maximum error voltage due to this slight time difference between the input voltage samples is given by:

$$\Delta V_e(MAX) = (V_P)(2\pi f_{cm})\left(\frac{4.5}{f_{CLK}}\right)$$

where:

ΔV_e is the error voltage due to sampling delay

V_P is the peak value of the common-mode voltage

f_{cm} is the common-mode frequency

As an example, to keep this error to ¼ LSB (~5 mV) when operating with a 60 Hz common-mode frequency, f_{cm}, and using a 640 kHz A/D clock, f_{CLK}, would allow a peak value of the common-mode voltage, V_P, which is given by:

$$V_P = \frac{[\Delta V_{e(MAX)}(f_{CLK})]}{(2\pi f_{cm})(4.5)}$$

or

$$V_P = \frac{(5 \times 10^{-3})(640 \times 10^3)}{(6.28)(60)(4.5)}$$

which gives

$V_P \simeq 1.9V$.

The allowed range of analog input voltages usually places more severe restrictions on input common-mode noise levels.

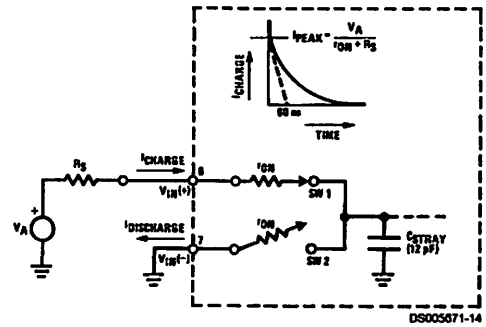
An analog input voltage with a reduced span and a relatively large zero offset can be handled easily by making use of the differential input (see section 2.4 Reference Voltage).

2.3 Analog Inputs

2.3 1 Input Current

Normal Mode

Due to the internal switching action, displacement currents will flow at the analog inputs. This is due to on-chip stray capacitance to ground as shown in *Figure 5.*



r_{ON} of SW 1 and SW 2 ≈ 5 kΩ

$\tau = r_{ON} C_{STRAY} \approx 5\ k\Omega \times 12\ pF = 60\ ns$

FIGURE 5. Analog Input Impedance

The voltage on this capacitance is switched and will result in currents entering the $V_{IN}(+)$ input pin and leaving the $V_{IN}(-)$ input which will depend on the analog differential input voltage levels. These current transients occur at the leading edge of the internal clocks. They rapidly decay and *do not cause errors* as the on-chip comparator is strobed at the end of the clock period.

Fault Mode

If the voltage source applied to the $V_{IN}(+)$ or $V_{IN}(-)$ pin exceeds the allowed operating range of V_{CC}+50 mV, large input currents can flow through a parasitic diode to the V_{CC} pin. If these currents can exceed the 1 mA max allowed spec, an external diode (1N914) should be added to bypass this current to the V_{CC} pin (with the current bypassed with this diode, the voltage at the $V_{IN}(+)$ pin can exceed the V_{CC} voltage by the forward voltage of this diode).

2.3.2 Input Bypass Capacitors

Bypass capacitors at the inputs will average these charges and cause a DC current to flow through the output resistances of the analog signal sources. This charge pumping action is worse for continuous conversions with the $V_{IN}(+)$ input voltage at full-scale. For continuous conversions with a 640 kHz clock frequency with the $V_{IN}(+)$ input at 5V, this DC current is at a maximum of approximately 5 µA. Therefore, *bypass capacitors should not be used at the analog inputs or the $V_{REF}/2$ pin* for high resistance sources (> 1 kΩ). If input bypass capacitors are necessary for noise filtering and high source resistance is desirable to minimize capacitor size, the detrimental effects of the voltage drop across this input resistance, which is due to the average value of the input current, can be eliminated with a full-scale adjustment while the given source resistor and input bypass capacitor are both in place. This is possible because the average value of the input current is a precise linear function of the differential input voltage.

2.3.3 Input Source Resistance

Large values of source resistance where an input bypass capacitor is not used, *will not cause errors* as the input currents settle out prior to the comparison time. If a low pass filter is required in the system, use a low valued series resistor (≤ 1 kΩ) for a passive RC section or add an op amp RC active low pass filter. For low source resistance applications, (≤ 1 kΩ), a 0.1 µF bypass capacitor at the inputs will prevent noise pickup due to series lead inductance of a long

Functional Description (Continued)

wire. A 100Ω series resistor can be used to isolate this capacitor—both the R and C are placed outside the feedback loop—from the output of an op amp, if used.

2.3.4 Noise

The leads to the analog inputs (pins 6 and 7) should be kept as short as possible to minimize input noise coupling. Both noise and undesired digital clock coupling to these inputs can cause system errors. The source resistance for these inputs should, in general, be kept below 5 kΩ. Larger values of source resistance can cause undesired system noise pickup. Input bypass capacitors, placed from the analog inputs to ground, will eliminate system noise pickup but can create analog scale errors as these capacitors will average the transient input switching currents of the A/D (see section 2.3.1.). This scale error depends on both a large source resistance and the use of an input bypass capacitor. This error can be eliminated by doing a full-scale adjustment of the A/D (adjust $V_{REF}/2$ for a proper full-scale reading—see section 2.5.2 on Full-Scale Adjustment) with the source resistance and input bypass capacitor in place.

2.4 Reference Voltage

2.4.1 Span Adjust

For maximum applications flexibility, these A/Ds have been designed to accommodate a 5 V_{DC}, 2.5 V_{DC} or an adjusted voltage reference. This has been achieved in the design of the IC as shown in *Figure 6.*

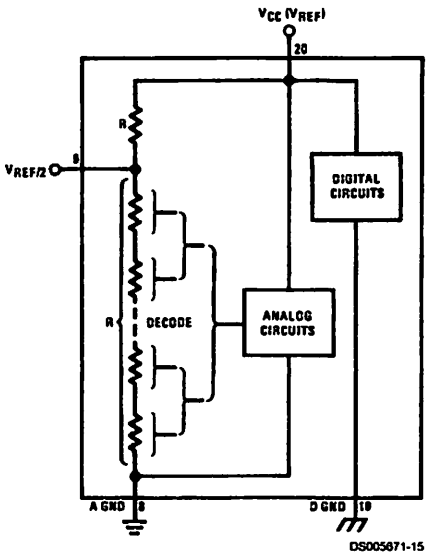


FIGURE 6. The $V_{REFERENCE}$ Design on the IC

Notice that the reference voltage for the IC is either ½ of the voltage applied to the V_{CC} supply pin, or is equal to the voltage that is externally forced at the $V_{REF}/2$ pin. This allows for a ratiometric voltage reference using the V_{CC} supply, a 5 V_{DC} reference voltage can be used for the V_{CC} supply or a voltage less than 2.5 V_{DC} can be applied to the $V_{REF}/2$ input for increased application flexibility. The internal gain to the $V_{REF}/2$ input is 2, making the full-scale differential input voltage twice the voltage at pin 9.

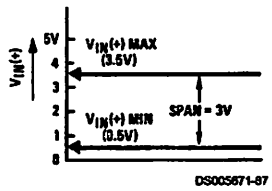
An example of the use of an adjusted reference voltage is to accommodate a reduced span—or dynamic voltage range of the analog input voltage. If the analog input voltage were to range from 0.5 V_{DC} to 3.5 V_{DC}, instead of 0V to 5 V_{DC}, the span would be 3V as shown in *Figure 7.* With 0.5 V_{DC} applied to the $V_{IN}(-)$ pin to absorb the offset, the reference voltage can be made equal to ½ of the 3V span or 1.5 V_{DC}. The A/D now will encode the $V_{IN}(+)$ signal from 0.5V to 3.5 V with the 0.5V input corresponding to zero and the 3.5 V_{DC} input corresponding to full-scale. The full 8 bits of resolution are therefore applied over this reduced analog input voltage range.

2.4.2 Reference Accuracy Requirements

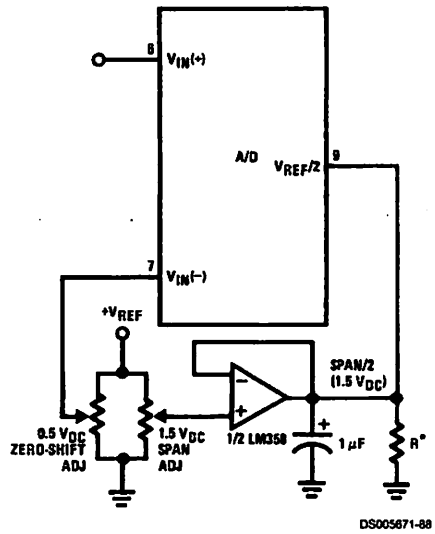
The converter can be operated in a ratiometric mode or an absolute mode. In ratiometric converter applications, the magnitude of the reference voltage is a factor in both the output of the source transducer and the output of the A/D converter and therefore cancels out in the final digital output code. The ADC0805 is specified particularly for use in ratiometric applications with no adjustments required. In absolute conversion applications, both the initial value and the temperature stability of the reference voltage are important factors in the accuracy of the A/D converter. For $V_{REF}/2$ voltages of 2.4 V_{DC} nominal value, initial errors of ±10 mV_{DC} will cause conversion errors of ±1 LSB due to the gain of 2 of the $V_{REF}/2$ input. In reduced span applications, the initial value and the stability of the $V_{REF}/2$ input voltage become even more important. For example, if the span is reduced to 2.5V, the analog input LSB voltage value is correspondingly reduced from 20 mV (5V span) to 10 mV and 1 LSB at the $V_{REF}/2$ input becomes 5 mV. As can be seen, this reduces the allowed initial tolerance of the reference voltage and requires correspondingly less absolute change with temperature variations. Note that spans smaller than 2.5V place even tighter requirements on the initial accuracy and stability of the reference source.

In general, the magnitude of the reference voltage will require an initial adjustment. Errors due to an improper value of reference voltage appear as full-scale errors in the A/D transfer function. IC voltage regulators may be used for references if the ambient temperature changes are not excessive. The LM336B 2.5V IC reference diode (from National Semiconductor) has a temperature stability of 1.8 mV typ (6 mV max) over $0°C \leq T_A \leq +70°C$. Other temperature range parts are also available.

Functional Description (Continued)



a) Analog Input Signal Example



*Add if $V_{REF}/2 \leq 1\ V_{DC}$ with LM358 to draw 3 mA to ground.

b) Accommodating an Analog Input from 0.5V (Digital Out = 00_{HEX}) to 3.5V (Digital Out=FF_{HEX})

FIGURE 7. Adapting the A/D Analog Input Voltages to Match an Arbitrary Input Signal Range

2.5 Errors and Reference Voltage Adjustments

2.5.1 Zero Error

The zero of the A/D does not require adjustment. If the minimum analog input voltage value, $V_{IN(MIN)}$, is not ground, a zero offset can be done. The converter can be made to output 0000 0000 digital code for this minimum input voltage by biasing the A/D $V_{IN}(-)$ input at this $V_{IN(MIN)}$ value (see Applications section). This utilizes the differential mode operation of the A/D.

The zero error of the A/D converter relates to the location of the first riser of the transfer function and can be measured by grounding the V_{IN} (−) input and applying a small magnitude positive voltage to the V_{IN} (+) input. Zero error is the difference between the actual DC input voltage that is necessary to just cause an output digital code transition from 0000 0000 to 0000 0001 and the ideal ½ LSB value (½ LSB = 9.8 mV for $V_{REF}/2$=2.500 V_{DC}).

2.5.2 Full-Scale

The full-scale adjustment can be made by applying a differential input voltage that is 1½ LSB less than the desired analog full-scale voltage range and then adjusting the magnitude of the $V_{REF}/2$ input (pin 9 or the V_{CC} supply if pin 9 is not used) for a digital output code that is just changing from 1111 1110 to 1111 1111.

2.5.3 Adjusting for an Arbitrary Analog Input Voltage Range

If the analog zero voltage of the A/D is shifted away from ground (for example, to accommodate an analog input signal that does not go to ground) this new zero reference should be properly adjusted first. A $V_{IN}(+)$ voltage that equals this desired zero reference plus ½ LSB (where the LSB is calculated for the desired analog span, 1 LSB=analog span/256) is applied to pin 6 and the zero reference voltage at pin 7 should then be adjusted to just obtain the 00_{HEX} to 01_{HEX} code transition.

The full-scale adjustment should then be made (with the proper $V_{IN}(-)$ voltage applied) by forcing a voltage to the $V_{IN}(+)$ input which is given by:

$$V_{IN}(+)\,fs\,adj = V_{MAX} - 1.5\left[\frac{(V_{MAX} - V_{MIN})}{256}\right]$$

where:

V_{MAX}=The high end of the analog input range

and

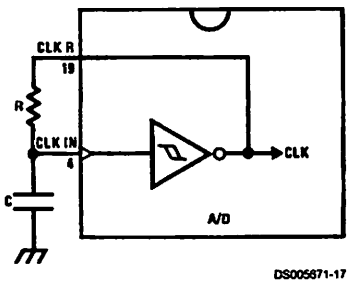
V_{MIN}=the low end (the offset zero) of the analog range. (Both are ground referenced.)

The $V_{REF}/2$ (or V_{CC}) voltage is then adjusted to provide a code change from FE_{HEX} to FF_{HEX}. This completes the adjustment procedure.

2.6 Clocking Option

The clock for the A/D can be derived from the CPU clock or an external RC can be added to provide self-clocking. The CLK IN (pin 4) makes use of a Schmitt trigger as shown in *Figure 8.*

Functional Description (Continued)



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$$CLK \cong \frac{1}{1.1\,RC}$$

$R \cong 10\ k\Omega$

FIGURE 8. Self-Clocking the A/D

leavy capacitive or DC loading of the clock R pin should be voided as this will disturb normal converter operation. oads less than 50 pF, such as driving up to 7 A/D converter lock inputs from a single clock R pin of 1 converter, are llowed. For larger clock line loading, a CMOS or low power TL buffer or PNP input logic should be used to minimize the ɔading on the clock R pin (do not use a standard TTL uffer).

.7 Restart During a Conversion

f the A/D is restarted ($\overline{CS}$ and $\overline{WR}$ go low and return high) luring a conversion, the converter is reset and a new con- ersion is started. The output data latch is not updated if the onversion in process is not allowed to be completed, there- ɔre the data of the previous conversion remains in this latch. he $\overline{INTR}$ output simply remains at the "1" level.

.8 Continuous Conversions

or operation in the free-running mode an initializing pulse hould be used, following power-up, to ensure circuit opera- ion. In this application, the $\overline{CS}$ input is grounded and the $\overline{WR}$ nput is tied to the $\overline{INTR}$ output. This $\overline{WR}$ and $\overline{INTR}$ node hould be momentarily forced to logic low following a ɔower-up cycle to guarantee operation.

.9 Driving the Data Bus

his MOS A/D, like MOS microprocessors and memories, vill require a bus driver when the total capacitance of the lata bus gets large. Other circuitry, which is tied to the data ɔus, will add to the total capacitive loading, even in RI-STATE (high impedance mode). Backplane bussing lso greatly adds to the stray capacitance of the data bus.

here are some alternatives available to the designer to ıandle this problem. Basically, the capacitive loading of the lata bus slows down the response time, even though DC specifications are still met. For systems operating with a elatively slow CPU clock frequency, more time is available n which to establish proper logic levels on the bus and herefore higher capacitive loads can be driven (see typical haracteristics curves).

At higher CPU clock frequencies time can be extended for /O reads (and/or writes) by inserting wait states (8080) or sing clock extending circuits (6800).

Finally, if time is short and capacitive loading is high, external ɔus drivers must be used. These can be TRI-STATE buffers (low power Schottky such as the DM74LS240 series is recommended) or special higher drive current products which are designed as bus drivers. High current bipolar bus drivers with PNP inputs are recommended.

2.10 Power Supplies

Noise spikes on the V_{CC} supply line can cause conversion errors as the comparator will respond to this noise. A low inductance tantalum filter capacitor should be used close to the converter V_{CC} pin and values of 1 µF or greater are recommended. If an unregulated voltage is available in the system, a separate LM340LAZ-5.0, TO-92, 5V voltage regulator for the converter (and other analog circuitry) will greatly reduce digital noise on the V_{CC} supply.

2.11 Wiring and Hook-Up Precautions

Standard digital wire wrap sockets are not satisfactory for breadboarding this A/D converter. Sockets on PC boards can be used and all logic signal wires and leads should be grouped and kept as far away as possible from the analog signal leads. Exposed leads to the analog inputs can cause undesired digital noise and hum pickup, therefore shielded leads may be necessary in many applications.

A single point analog ground that is separate from the logic ground points should be used. The power supply bypass capacitor and the self-clocking capacitor (if used) should both be returned to digital ground. Any $V_{REF}/2$ bypass capacitors, analog input filter capacitors, or input signal shielding should be returned to the analog ground point. A test for proper grounding is to measure the zero error of the A/D converter. Zero errors in excess of ¼ LSB can usually be traced to improper board layout and wiring (see section 2.5.1 for measuring the zero error).

3.0 TESTING THE A/D CONVERTER

There are many degrees of complexity associated with testing an A/D converter. One of the simplest tests is to apply a known analog input voltage to the converter and use LEDs to display the resulting digital output code as shown in *Figure 9.*

For ease of testing, the $V_{REF}/2$ (pin 9) should be supplied with 2.560 V_{DC} and a V_{CC} supply voltage of 5.12 V_{DC} should be used. This provides an LSB value of 20 mV.

If a full-scale adjustment is to be made, an analog input voltage of 5.090 V_{DC} (5.120–1½ LSB) should be applied to the $V_{IN}(+)$ pin with the $V_{IN}(-)$ pin grounded. The value of the $V_{REF}/2$ input voltage should then be adjusted until the digital output code is just changing from 1111 1110 to 1111 1111. This value of $V_{REF}/2$ should then be used for all the tests.

The digital output LED display can be decoded by dividing the 8 bits into 2 hex characters, the 4 most significant (MS) and the 4 least significant (LS). *Table 1* shows the fractional binary equivalent of these two 4-bit groups. By adding the voltages obtained from the "VMS" and "VLS" columns in *Table 1*, the nominal value of the digital display (when $V_{REF}/2$ = 2.560V) can be determined. For example, for an output LED display of 1011 0110 or B6 (in hex), the voltage values from the table are 3.520 + 0.120 or 3.640 V_{DC}. These voltage values represent the center-values of a perfect A/D converter. The effects of quantization error have to be accounted for in the interpretation of the test results.

Functional Description (Continued)

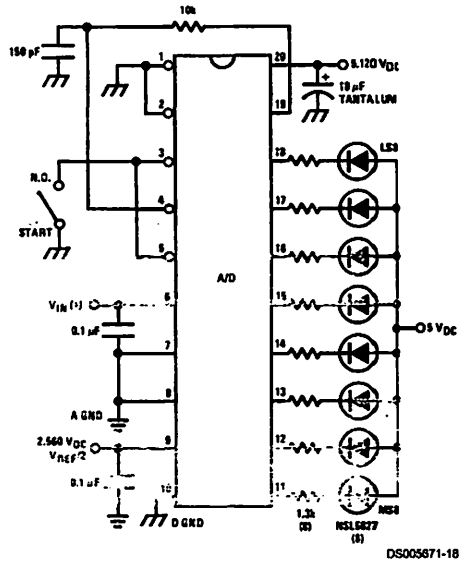


FIGURE 9. Basic A/D Tester

For a higher speed test system, or to obtain plotted data, a digital-to-analog converter is needed for the test set-up. An accurate 10-bit DAC can serve as the precision voltage source for the A/D. Errors of the A/D under test can be expressed as either analog voltages or differences in 2 digital words.

A basic A/D tester that uses a DAC and provides the error as an analog output voltage is shown in *Figure 8*. The 2 op amps can be eliminated if a lab DVM with a numerical subtraction feature is available to read the difference voltage, "A–C", directly. The analog input voltage can be supplied by a low frequency ramp generator and an X-Y plotter can be used to provide analog error (Y axis) versus analog input (X axis).

For operation with a microprocessor or a computer-based test system, it is more convenient to present the errors digitally. This can be done with the circuit of *Figure 11*, where the output code transitions can be detected as the 10-bit DAC is incremented. This provides 1/4 LSB steps for the 8-bit A/D under test. If the results of this test are automatically plotted with the analog input on the X axis and the error (in LSB's) as the Y axis, a useful transfer function of the A/D under test results. For acceptance testing, the plot is not necessary and the testing speed can be increased by establishing internal limits on the allowed error for each code.

4.0 MICROPROCESSOR INTERFACING

To dicuss the interface with 8080A and 6800 microprocessors, a common sample subroutine structure is used. The microprocessor starts the A/D, reads and stores the results of 16 successive conversions, then returns to the user's program. The 16 data bytes are stored in 16 successive memory locations. All Data and Addresses will be given in hexadecimal form. Software and hardware details are provided separately for each type of microprocessor.

4.1 Interfacing 8080 Microprocessor Derivatives (8048, 8085)

This converter has been designed to directly interface with derivatives of the 8080 microprocessor. The A/D can be mapped into memory space (using standard memory address decoding for $\overline{CS}$ and the $\overline{MEMR}$ and $\overline{MEMW}$ strobes) or it can be controlled as an I/O device by using the $\overline{I/O}$ R and $\overline{I/O}$ W strobes and decoding the address bits A0 → A7 (or address bits A8 → A15 as they will contain the same 8-bit address information) to obtain the $\overline{CS}$ input. Using the I/O space provides 256 additional addresses and may allow a simpler 8-bit address decoder but the data can only be input to the accumulator. To make use of the additional memory reference instructions, the A/D should be mapped into memory space. An example of an A/D in I/O space is shown in *Figure 12*.

Functional Description (Continued)

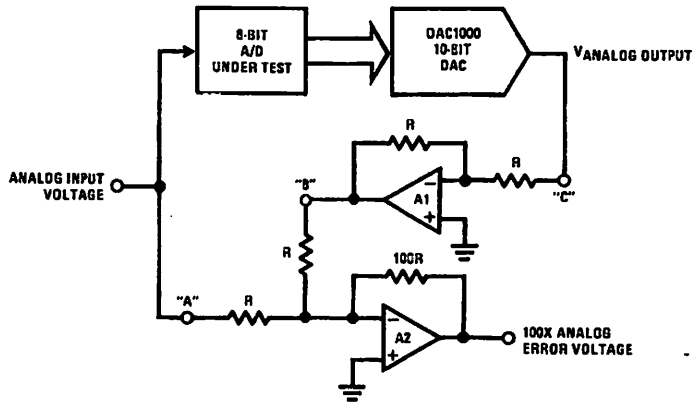


FIGURE 10. A/D Tester with Analog Error Output

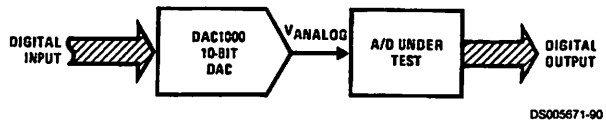


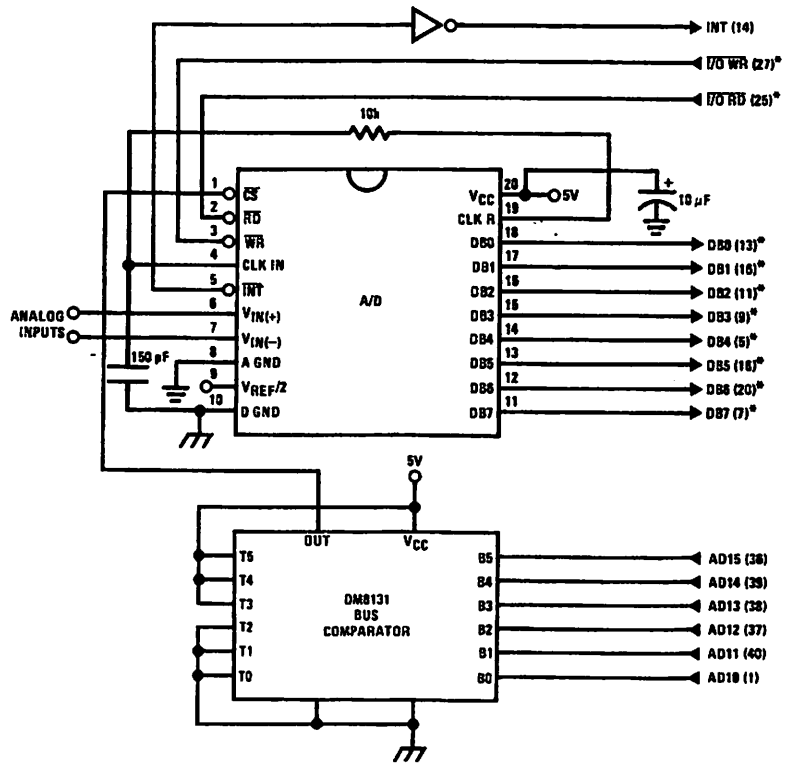
FIGURE 11. Basic "Digital" A/D Tester

TABLE 1. DECODING THE DIGITAL OUTPUT LEDs

HEX	BINARY				FRACTIONAL BINARY VALUE FOR		OUTPUT VOLTAGE CENTER VALUES WITH $V_{REF}/2=2.560\ V_{DC}$	
					MS GROUP	LS GROUP	VMS GROUP (Note 15)	VLS GROUP (Note 15)
F	1	1	1	1	15/16	15/256	4.800	0.300
E	1	1	1	0	7/8	7/128	4.480	0.280
D	1	1	0	1	13/16	13/256	4.160	0.260
C	1	1	0	0	3/4	3/64	3.840	0.240
B	1	0	1	1	11/16	11/256	3.520	0.220
A	1	0	1	0	5/8	5/128	3.200	0.200
9	1	0	0	1	9/16	9/256	2.880	0.180
8	1	0	0	0	1/2	1/32	2.560	0.160
7	0	1	1	1	7/16	7/256	2.240	0.140
6	0	1	1	0	3/8	3/128	1.920	0.120
5	0	1	0	1	5/16	2/256	1.600	0.100
4	0	1	0	0	1/4	1/64	1.280	0.080
3	0	0	1	1	3/16	3/256	0.960	0.060
2	0	0	1	0	1/8	1/128	0.640	0.040
1	0	0	0	1	1/16	1/256	0.320	0.020
0	0	0	0	0			0	0

Note 15: Display Output=VMS Group + VLS Group

Functional Description (Continued)



Note 16: *Pin numbers for the DP8228 system controller, others are INS8080A.

Note 17: Pin 23 of the INS8228 must be tied to +12V through a 1 kΩ resistor to generate the RST 7 instruction when an interrupt is acknowledged as required by the accompanying sample program.

FIGURE 12. ADC0801_INS8080A CPU Interface

Functional Description (Continued)

SAMPLE PROGRAM FOR *Figure 12* ADC0801–INS8080A CPU INTERFACE

```
0038    C3 00 03    RST 7:          JMP     LD DATA
  •       •           •
  •       •           •
0100    21 00 02    START:          LXI H 0200H         ;HL pair will point to
                                                        ;data storage locations
0103    31 00 04    RETURN:         LXI SP 0400H        ;Initialize stack pointer (Note 1)
0106    7D                          MOV A, L            ;Test # of bytes entered
0107    FE 0F                       CPI 0F H            ;If # = 16. JMP to
0109    CA 13 01                    JZ CONT             ;user program
010C    D3 E0                       OUT E0 H            ;Start A/D
010E    FB                          EI                  ;Enable interrupt
010F    00          LOOP:           NOP                 ;Loop until end of
0110    C3 0F 01                    JMP LOOP            ;conversion
0113      •         CONT:             •
  •       •           •               •
  •       •         (User program to  •
  •       •         process data)     •
  •       •           •               •
  •       •           •               •
0300    DB E0       LD DATA:        IN E0 H             ;Load data into accumulator
0302    77                          MOV M, A            ;Store data
0303    23                          INX H               ;Increment storage pointer
0304    C3 03 01                    JMP RETURN
```

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Note 18: The stack pointer must be dimensioned because a RST 7 instruction pushes the PC onto the stack.

Note 19: All address used were arbitrarily chosen.

The standard control bus signals of the 8080 $\overline{CS}$, $\overline{RD}$ and $\overline{WR}$) can be directly wired to the digital control inputs of the A/D and the bus timing requirements are met to allow both starting the converter and outputting the data onto the data bus. A bus driver should be used for larger microprocessor systems where the data bus leaves the PC board and/or must drive capacitive loads larger than 100 pF.

4.1.1 Sample 8080A CPU Interfacing Circuitry and Program

The following sample program and associated hardware shown in *Figure 12* may be used to input data from the converter to the INS8080A CPU chip set (comprised of the INS8080A microprocessor, the INS8228 system controller and the INS8224 clock generator). For simplicity, the A/D is controlled as an I/O device, specifically an 8-bit bi-directional port located at an arbitrarily chosen port address, E0. The TRI-STATE output capability of the A/D eliminates the need for a peripheral interface device, however address decoding is still required to generate the appropriate $\overline{CS}$ for the converter.

It is important to note that in systems where the A/D converter is 1-of-8 or less I/O mapped devices, no address decoding circuitry is necessary. Each of the 8 address bits (A0 to A7) can be directly used as $\overline{CS}$ inputs—one for each I/O device.

4.1.2 INS8048 Interface

The INS8048 interface technique with the ADC0801 series (see *Figure 13*) is simpler than the 8080A CPU interface. There are 24 I/O lines and three test input lines in the 8048. With these extra I/O lines available, one of the I/O lines (bit 0 of port 1) is used as the chip select signal to the A/D, thus eliminating the use of an external address decoder. Bus control signals $\overline{RD}$, $\overline{WR}$ and $\overline{INT}$ of the 8048 are tied directly to the A/D. The 16 converted data words are stored at on-chip RAM locations from 20 to 2F (Hex). The $\overline{RD}$ and $\overline{WR}$ signals are generated by reading from and writing into a dummy address, respectively. A sample interface program is shown below.

Functional Description (Continued)

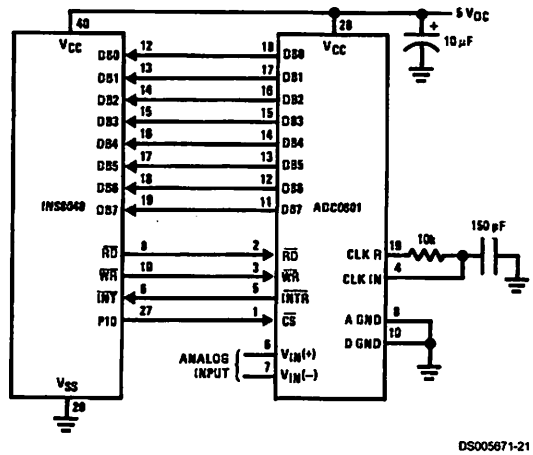

FIGURE 13. INS8048 Interface

SAMPLE PROGRAM FOR *Figure 13* INS8048 INTERFACE

```
04 10                   JMP     10H             ;Program starts at addr 10
                        ORG     3H
04 50                   JMP     50H             ;Interrupt jump vector
                        ORG     10H             ;Main program
99 FE                   ANL     P1, #0FEH       ;Chip select
81                      MOVX    A, @R1          ;Read in the 1st data
                                                ;to reset the intr
89 01           START:  ORL     P1, #1          ;Set port pin high
B8 20                   MOV     R0, #20H        ;Data address
B9 FF                   MOV     R1, #0FFH       ;Dummy address
BA 10                   MOV     R2, #10H        ;Counter for 16 bytes
23 FF           AGAIN:  MOV     A, #0FFH        ;Set ACC for intr loop
99 FE                   ANL     P1, #0FEH       ;Send CS (bit 0 of P1)
91                      MOVX    @R1, A          ;Send WR out
05                      EN      I               ;Enable interrupt
96 21           LOOP:   JNZ     LOOP            ;Wait for interrupt
EA 1B                   DJNZ    R2, AGAIN       ;If 16 bytes are read
00                      NOP                     ;go to user's program
00                      NOP
                        ORG     50H
81              INDATA: MOVX    A, @R1          ;Input data, CS still low
A0                      MOV     @R0, A          ;Store in memory
18                      INC     R0              ;Increment storage counter
89 01                   ORL     P1, #1          ;Reset CS signal
27                      CLR     A               ;Clear ACC to get out of
93                      RETR                    ;the interrupt loop
```

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4.2 Interfacing the Z-80

The Z-80 control bus is slightly different from that of the 8080. General $\overline{RD}$ and $\overline{WR}$ strobes are provided and separate memory request, $\overline{MREQ}$, and I/O request, $\overline{IORQ}$, signals are used which have to be combined with the generalized strobes to provide the equivalent 8080 signals. An advantage of operating the A/D in I/O space with the Z-80 is that the CPU will automatically insert one wait state (the $\overline{RD}$ and $\overline{WR}$ strobes are extended one clock period) to allow more time for the I/O devices to respond. Logic to map the A/D in I/O space is shown in *Figure 14*.

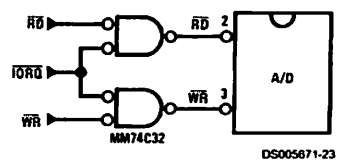


FIGURE 14. Mapping the A/D as an I/O Device for Use with the Z-80 CPU

Additional I/O advantages exist as software DMA routines are available and use can be made of the output data transfer which exists on the upper 8 address lines (A8 to

Functional Description (Continued)

A15) during I/O input instructions. For example, MUX channel selection for the A/D can be accomplished with this operating mode.

4.3 Interfacing 6800 Microprocessor Derivatives (6502, etc.)

The control bus for the 6800 microprocessor derivatives does not use the $\overline{RD}$ and $\overline{WR}$ strobe signals. Instead it employs a single R/$\overline{W}$ line and additional timing, if needed, can be derived fom the $\phi 2$ clock. All I/O devices are memory mapped in the 6800 system, and a special signal, VMA, indicates that the current address is valid. *Figure 15* shows an interface schematic where the A/D is memory mapped in the 6800 system. For simplicity, the $\overline{CS}$ decoding is shown using ½ DM8092. Note that in many 6800 systems, an already decoded $\overline{4/5}$ line is brought out to the common bus at pin 21. This can be tied directly to the $\overline{CS}$ pin of the A/D, provided that no other devices are addressed at HX ADDR: 4XXX or 5XXX.

The following subroutine performs essentially the same function as in the case of the 8080A interface and it can be called from anywhere in the user's program.

In *Figure 16* the ADC0801 series is interfaced to the M6800 microprocessor through (the arbitrarily chosen) Port B of the MC6820 or MC6821 Peripheral Interface Adapter, (PIA). Here the $\overline{CS}$ pin of the A/D is grounded since the PIA is already memory mapped in the M6800 system and no $\overline{CS}$ decoding is necessary. Also notice that the A/D output data lines are connected to the microprocessor bus under program control through the PIA and therefore the A/D $\overline{RD}$ pin can be grounded.

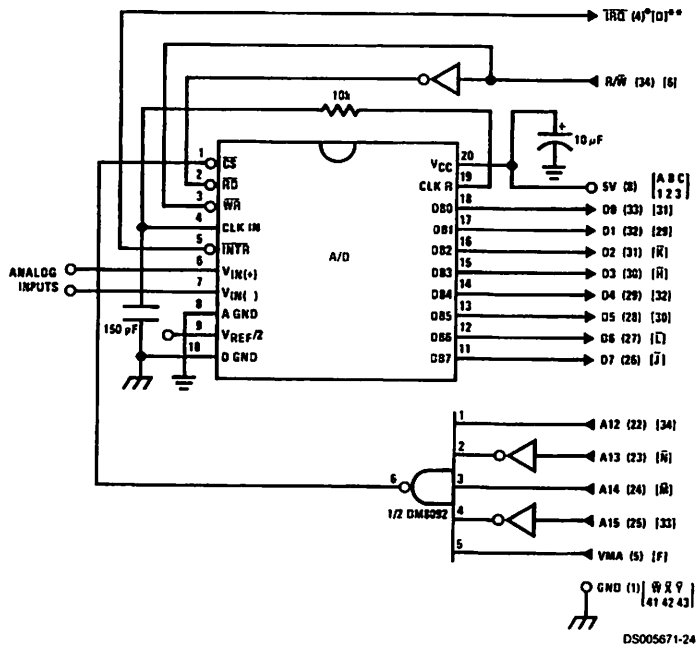
A sample interface program equivalent to the previous one is shown below *Figure 16*. The PIA Data and Control Registers of Port B are located at HEX addresses 8006 and 8007, respectively.

5.0 GENERAL APPLICATIONS

The following applications show some interesting uses for the A/D. The fact that one particular microprocessor is used is not meant to be restrictive. Each of these application circuits would have its counterpart using any microprocessor that is desired.

5.1 Multiple ADC0801 Series to MC6800 CPU Interface

To transfer analog data from several channels to a single microprocessor system, a multiple converter scheme presents several advantages over the conventional multiplexer single-converter approach. With the ADC0801 series, the differential inputs allow individual span adjustment for each channel. Furthermore, all analog input channels are sensed simultaneously, which essentially divides the microprocessor's total system servicing time by the number of channels, since all conversions occur simultaneously. This scheme is shown in *Figure 17*.



Note 20: Numbers in parentheses refer to MC6800 CPU pin out.

Note 21: Number or letters in brackets refer to standard M6800 system common bus code.

FIGURE 15. ADC0801-MC6800 CPU Interface

Functional Description (Continued)

SAMPLE PROGRAM FOR *Figure 15* ADC0801-MC6800 CPU INTERFACE

```
0010   DF 36      DATAIN   STX    TEMP2    ; Save contents of X
0012   CE 00 2C            LDX    #$002C   ; Upon IRQ low CPU
0015   FF FF F8            STX    $FFF8    ; jumps to 002C
0018   B7 50 00            STAA   $5000    ; Start ADC0801
001B   0E                  CLI
001C   3E          CONVRT  WAI              ; Wait for interrupt
001D   DE 34               LDX    TEMP1
001F   8C 02 0F            CPX    #$020F   ; Is final data stored?
0022   27 14               BEQ    ENDP
0024   B7 50 00            STAA   $5000    ; Restarts ADC0801
0027   08                  INX
0028   DF 34               STX    TEMP1
002A   20 F0               BRA    CONVRT
002C   DE 34      INTRPT   LDX    TEMP1
002E   B6 50 00            LDAA   $5000    ; Read data
0031   A7 00               STAA   X        ; Store it at X
0033   3B                  RTI
0034   02 00      TEMP1    FDB    $0200    ; Starting address for
                                            ; data storage
0036   00 00      TEMP2    FDB    $0000
0038   CE 02 00   ENDP     LDX    #$0200   ; Reinitialize TEMP1
003B   DF 34               STX    TEMP1
003D   DE 36               LDX    TEMP2
003F   39                  RTS              ; Return from subroutine
                                            ; To user's program
```

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Note 22: In order for the microprocessor to service subroutines and interrupts, the stack pointer must be dimensioned in the user's program.

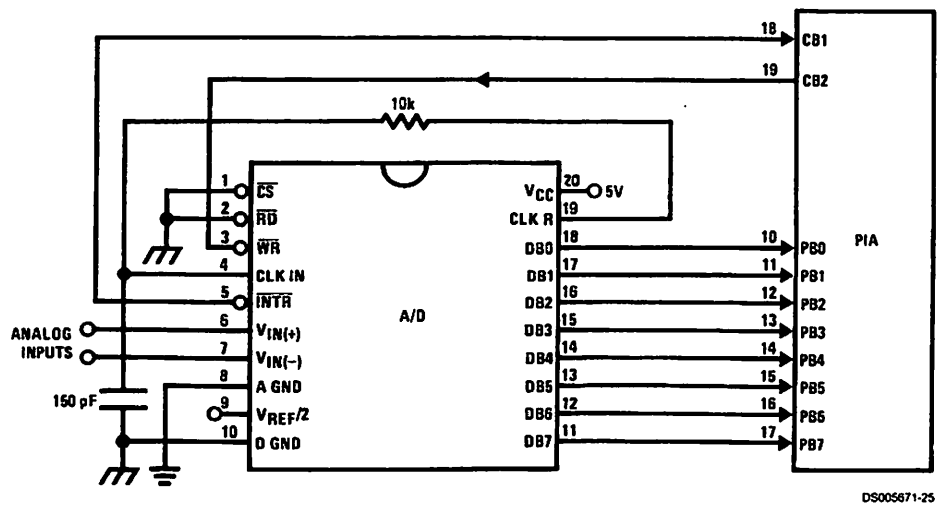

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FIGURE 16. ADC0801–MC6820 PIA Interface

Functional Description (Continued)

SAMPLE PROGRAM FOR *Figure 16* ADC0801–MC6820 PIA INTERFACE

```
0010    CE 00 38    DATAIN    LDX     #$0038    ; Upon IRQ low CPU
0013    FF FF F8              STX     $FFF8     ; jumps to 0038
0016    B6 80 06              LDAA    PIAORB    ; Clear possible IRQ flags
0019    4F                    CLRA
001A    B7 80 07              STAA    PIACRB
001D    B7 80 06              STAA    PIAORB    ; Set Port B as input
0020    0E                    CLI
0021    C6 34                 LDAB    #$34
0023    86 3D                 LDAA    #$3D
0025    F7 80 07    CONVRT    STAB    PIACRB    ; Starts ADC0801
0028    B7 80 07              STAA    PIACRB
002B    3E                    WAI               ; Wait for interrupt
002C    DE 40                 LDX     TEMP1
002E    8C 02 0F              CPX     #$020F    ; Is final data stored?
0031    27 0F                 BEQ     ENDP
0033    08                    INX
0034    DF 40                 STX     TEMP1
0036    20 ED                 BRA     CONVRT
0038    DE 40       INTRPT    LDX     TEMP1
003A    B6 80 06              LDAA    PIAORB    ; Read data in
003D    A7 00                 STAA    X         ; Store it at X
003F    3B                    RTI
0040    02 00       TEMP1     FDB     $0200     ; Starting address for
                                                ; data storage
0042    CE 02 00    ENDP      LDX     #$0200    ; Reinitialize TEMP1
0045    DF 40                 STX     TEMP1
0047    39                    RTS               ; Return from subroutine
                    PIAORB    EQU     $8006     ; To user's program
                    PIACRB    EQU     $8007
```

DS005671-A2

The following schematic and sample subroutine (DATA IN) may be used to interface (up to) 8 ADC0801's directly to the MC6800 CPU. This scheme can easily be extended to allow the interface of more converters. In this configuration the converters are (arbitrarily) located at HEX address 5000 in the MC6800 memory space. To save components, the clock signal is derived from just one RC pair on the first converter. This output drives the other A/Ds.

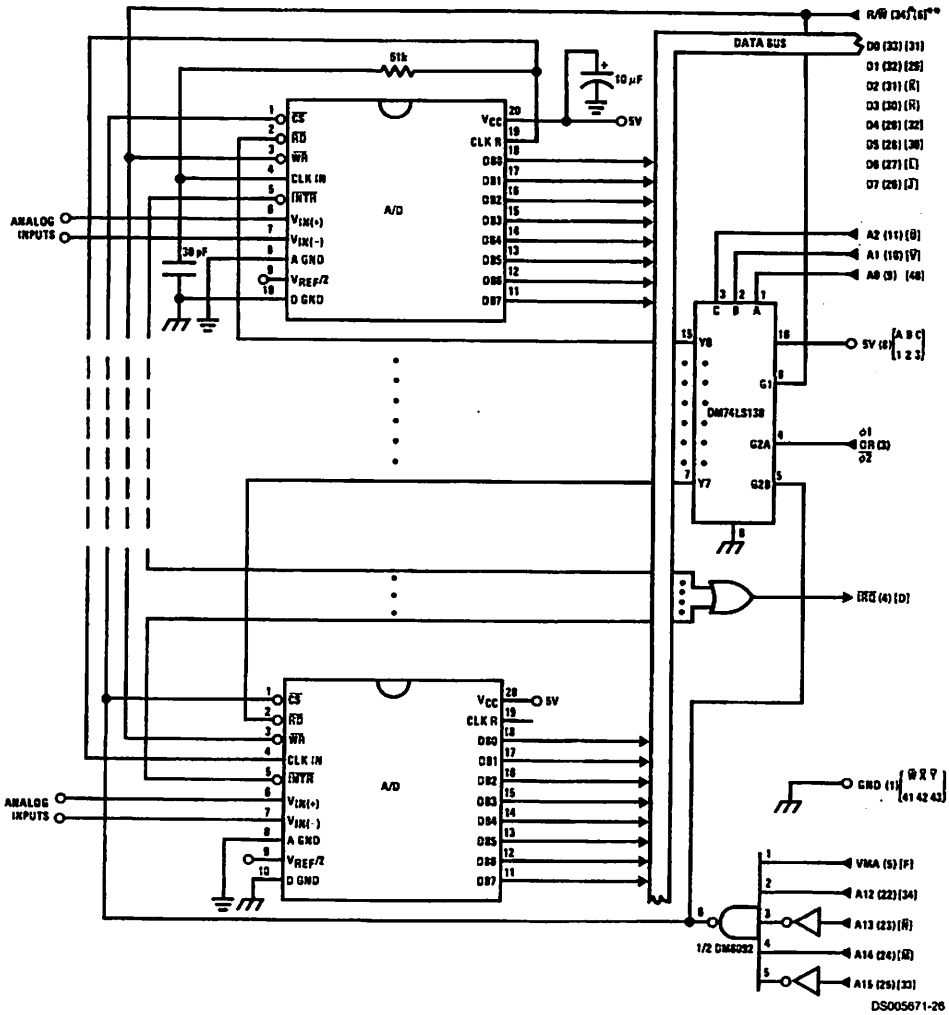
All the converters are started simultaneously with a STORE instruction at HEX address 5000. Note that any other HEX address of the form 5XXX will be decoded by the circuit, pulling all the $\overline{CS}$ inputs low. This can easily be avoided by using a more definitive address decoding scheme. All the interrupts are ORed together to insure that all A/Ds have completed their conversion before the microprocessor is interrupted.

The subroutine, DATA IN, may be called from anywhere in the user's program. Once called, this routine initializes the CPU, starts all the converters simultaneously and waits for the interrupt signal. Upon receiving the interrupt, it reads the converters (from HEX addresses 5000 through 5007) and stores the data successively at (arbitrarily chosen) HEX addresses 0200 to 0207, before returning to the user's program. All CPU registers then recover the original data they had before servicing DATA IN.

5.2 Auto-Zeroed Differential Transducer Amplifier and A/D Converter

The differential inputs of the ADC0801 series eliminate the need to perform a differential to single ended conversion for a differential transducer. Thus, one op amp can be eliminated since the differential to single ended conversion is provided by the differential input of the ADC0801 series. In general, a transducer preamp is required to take advantage of the full A/D converter input dynamic range.

Functional Description (Continued)



Note 23: Numbers in parentheses refer to MC6800 CPU pin out.

Note 24: Numbers of letters in brackets refer to standard M6800 system common bus code.

FIGURE 17. Interfacing Multiple A/Ds in an MC6800 System

Functional Description (Continued)

SAMPLE PROGRAM FOR *Figure 17* INTERFACING MULTIPLE A/D's IN AN MC6800 SYSTEM

ADDRESS	HEX CODE		MNEMONICS		COMMENTS
0010	DF 44	DATAIN	STX	TEMP	; Save Contents of X
0012	CE 00 2A		LDX	#$002A	; Upon $\overline{IRQ}$ LOW CPU
0015	FF FF F8		STX	$FFF8	; Jumps to 002A
0018	B7 50 00		STAA	$5000	; Starts all A/D's
001B	0E		CLI		
001C	3E		WAI		; Wait for interrupt
001D	CE 50 00		LDX	#$5000	
0020	DF 40		STX	INDEX1	; Reset both INDEX
0022	CE 02 00		LDX	#$0200	; 1 and 2 to starting
0025	DF 42		STX	INDEX2	; addresses
0027	DE 44		LDX	TEMP	
0029	39		RTS		; Return from subroutine
002A	DE 40	INTRPT	LDX	INDEX1	; INDEX1 → X
002C	A6 00		LDAA	X	; Read data in from A/D at X
002E	08		INX		; Increment X by one
002F	DF 40		STX	INDEX1	; X → INDEX1
0031	DE 42		LDX	INDEX2	; INDEX2 → X

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SAMPLE PROGRAM FOR *Figure 17* INTERFACING MULTIPLE A/D's IN AN MC6800 SYSTEM

ADDRESS	HEX CODE		MNEMONICS		COMMENTS
0033	A7 00		STAA	X	; Store data at X
0035	8C 02 07		CPX	#$0207	; Have all A/D's been read?
0038	27 05		BEQ	RETURN	; Yes: branch to RETURN
003A	08		INX		; No: increment X by one
003B	DF 42		STX	INDEX2	; X → INDEX2
003D	20 EB		BRA	INTRPT	; Branch to 002A
003F	3B	RETURN	RTI		
0040	50 00	INDEX1	FDB	$5000	; Starting address for A/D
0042	02 00	INDEX2	FDB	$0200	; Starting address for data storage
0044	00 00	TEMP	FDB	$0000	

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Note 25: In order for the microprocessor to service subroutines and interrupts, the stack pointer must be dimensioned in the user's program.

For amplification of DC input signals, a major system error is the input offset voltage of the amplifiers used for the preamp. *Figure 18* is a gain of 100 differential preamp whose offset voltage errors will be cancelled by a zeroing subroutine which is performed by the INS8080A microprocessor system. The total allowable input offset voltage error for this preamp is only 50 µV for ¼ LSB error. This would obviously require very precise amplifiers. The expression for the differential output voltage of the preamp is:

$$V_O = \underbrace{[V_{IN}(+) - V_{IN}(-)]}_{\text{SIGNAL}} \underbrace{\left[1 + \frac{2R2}{R1}\right]}_{\text{GAIN}} +$$

$$\underbrace{(V_{OS_2} - V_{OS_1} - V_{OS_3} \pm I_X R_X)}_{\text{DC ERROR TERM}} \underbrace{\left(1 + \frac{2R2}{R1}\right)}_{\text{GAIN}}$$

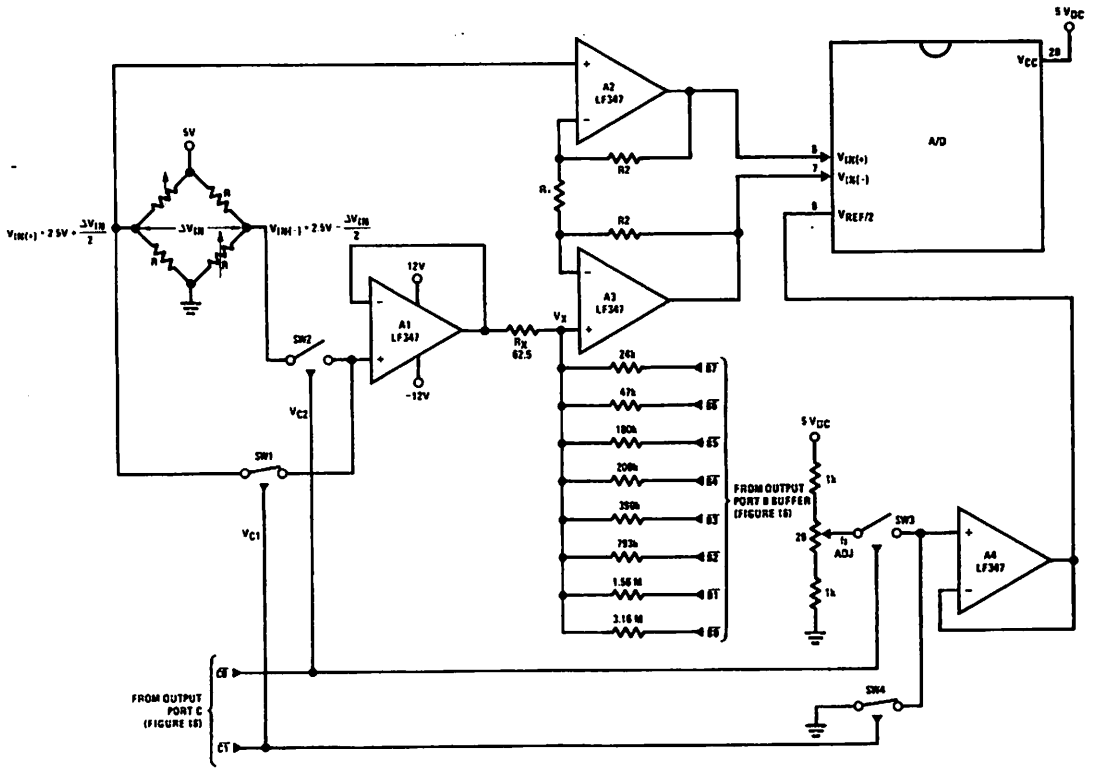
where I_X is the current through resistor R_X. All of the offset error terms can be cancelled by making $\pm I_X R_X = V_{OS1} + V_{OS3} - V_{OS2}$. This is the principle of this auto-zeroing scheme.

The INS8080A uses the 3 I/O ports of an INS8255 Programable Peripheral Interface (PPI) to control the auto zeroing and input data from the ADC0801 as shown in *Figure 19*. The PPI is programmed for basic I/O operation (mode 0) with Port A being an input port and Ports B and C being output ports. Two bits of Port C are used to alternately open or close the 2 switches at the input of the preamp. Switch SW1 is closed to force the preamp's differential input to be zero during the zeroing subroutine and then opened and SW2 is then closed for conversion of the actual differential input signal. Using 2 switches in this manner eliminates concern for the ON resistance of the switches as they must conduct only the input bias current of the input amplifiers.

Output Port B is used as a successive approximation register by the 8080 and the binary scaled resistors in series with each output bit create a D/A converter. During the zeroing subroutine, the voltage at V_x increases or decreases as required to make the differential output voltage equal to zero. This is accomplished by ensuring that the voltage at the output of A1 is approximately 2.5V so that a logic "1" (5V) on

Functional Description (Continued)

any output of Port B will source current into node V_X thus raising the voltage at V_X and making the output differential more negative. Conversely, a logic "0" (0V) will pull current out of node V_X and decrease the voltage, causing the differential output to become more positive. For the resistor values shown, V_X can move ±12 mV with a resolution of 50 µV, which will null the offset error term to ¼ LSB of full-scale for the ADC0801. It is important that the voltage levels that drive the auto-zero resistors be constant. Also, for symmetry, a logic swing of 0V to 5V is convenient. To achieve this, a CMOS buffer is used for the logic output signals of Port B and this CMOS package is powered with a stable 5V source. Buffer amplifier A1 is necessary so that it can source or sink the D/A output current.



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Note 26: R2 = 49.5 R1

Note 27: Switches are LMC13334 CMOS analog switches.

Note 28: The 9 resistors used in the auto-zero section can be ±5% tolerance.

FIGURE 18. Gain of 100 Differential Transducer Preamp

Functional Description (Continued)

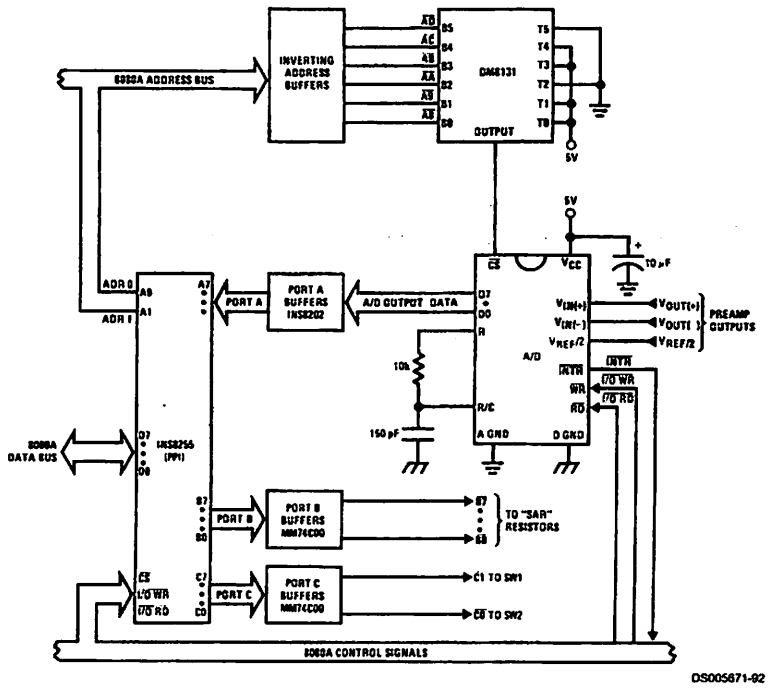


FIGURE 19. Microprocessor Interface Circuitry for Differential Preamp

A flow chart for the zeroing subroutine is shown in *Figure 20.* It must be noted that the ADC0801 series will output an all zero code when it converts a negative input [$V_{IN}(-) \geq V_{IN}(+)$]. Also, a logic inversion exists as all of the I/O ports are buffered with inverting gates.

Basically, if the data read is zero, the differential output voltage is negative, so a bit in Port B is cleared to pull V_X more negative which will make the output more positive for the next conversion. If the data read is not zero, the output voltage is positive so a bit in Port B is set to make V_X more positive and the output more negative. This continues for 8 approximations and the differential output eventually converges to within 5 mV of zero.

The actual program is given in *Figure 21.* All addresses used are compatible with the BLC 80/10 microcomputer system. In particular:

Port A and the ADC0801 are at port address E4

Port B is at port address E5

Port C is at port address E6

PPI control word port is at port address E7

Program Counter automatically goes to ADDR:3C3D upon acknowledgement of an interrupt from the ADC0801

8.3 Multiple A/D Converters in a Z-80 Interrupt Driven Mode

In data acquisition systems where more than one A/D converter (or other peripheral device) will be interrupting program execution of a microprocessor, there is obviously a need for the CPU to determine which device requires servicing. *Figure 22* and the accompanying software is a method of determining which of 7 ADC0801 converters has completed a conversion ($\overline{INTR}$ asserted) and is requesting an interrupt. This circuit allows starting the A/D converters in any sequence, but will input and store valid data from the converters with a priority sequence of A/D 1 being read first, A/D 2 second, etc., through A/D 7 which would have the lowest priority for data being read. Only the converters whose INT is asserted will be read.

The key to decoding circuitry is the DM74LS373, 8-bit D type flip-flop. When the Z-80 acknowledges the interrupt, the program is vectored to a data input Z-80 subroutine. This subroutine will read a peripheral status word from the DM74LS373 which contains the logic state of the $\overline{INTR}$ outputs of all the converters. Each converter which initiates an interrupt will place a logic "0" in a unique bit position in the status word and the subroutine will determine the identity of the converter and execute a data read. An identifier word (which indicates which A/D the data came from) is stored in the next sequential memory location above the location of the data so the program can keep track of the identity of the data entered.

Functional Description (Continued)

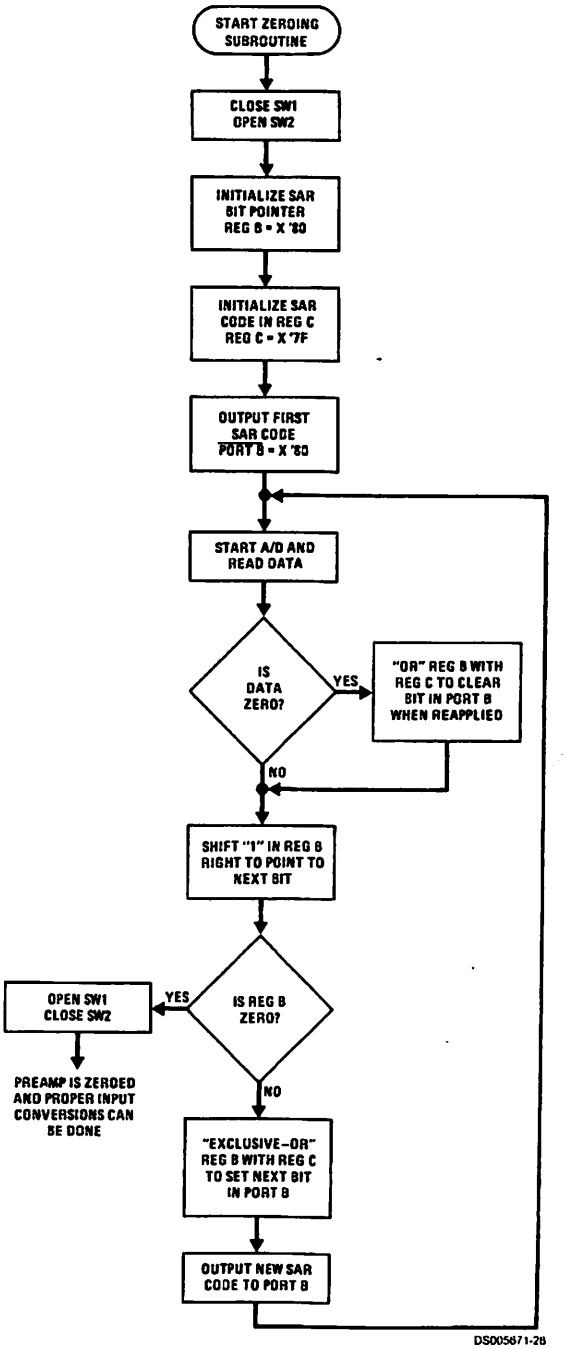


FIGURE 20. Flow Chart for Auto-Zero Routine

Functional Description (Continued)

```
3D00   3E90     MVI 90
3D02   D3E7     Out Control Port                    ;Program PPI
3D04   2601     MVI H 01          Auto-Zero Subroutine
3D06   7C       MOV A,H
3D07   D3E6     OUT C                              ;Close SW1 open SW2
3D09   0680     MVI B 80                           ;Initialize SAR bit pointer
3D0B   3E7F     MVI A 7F                           ;Initialize SAR code
3D0D   4F       MOV C,A           Return
3D0E   D3E5     OUT B                              ;Port B = SAR code
3D10   31AA3D   LXI SP 3DAA       Start            ;Dimension stack pointer
3D13   D3E4     OUT A                              ;Start A/D
3D15   FB       IE
3D16   00       NOP               Loop             ;Loop until INT asserted
3D17   C3163D   JMP Loop
3D1A   7A       MOV A,D           Auto-Zero
3D1B   C600     ADI 00
3D1D   CA2D3D   JZ Set C                           ;Test A/D output data for zero
3D20   78       MOV A,B           Shift B
3D21   F600     ORI 00                             ;Clear carry
3D23   1F       RAR                                ;Shift "1" in B right one place
3D24   FE00     CPI 00                             ;Is B zero? If yes last
3D26   CA373D   JZ Done                            ;approximation has been made
3D29   47       MOV B,A
3D2A   C3333D   JMP New C
3D2D   79       MOV A,C           Set C
3D2E   B0       ORA B                              ;Set bit in C that is in same
3D2F   4F       MOV C,A                            ;position as "1" in B
3D30   C3203D   JMP Shift B
3D33   A9       XRA C             New C            ;Clear bit in C that is in
3D34   C30D3D   JMP Return                         ;same position as "1" in B
3D37   47       MOV B,A           Done             ;then output new SAR code.
3D38   7C       MOV A,H                            ;Open SW1, close SW2 then
3D39   EE03     XRI 03                             ;proceed with program. Preamp
3D3B   D3E6     OUT C                              ;is now zeroed.
3D3D            •                 Normal
                •
                •
                Program for processing
                proper data values
3C3D   DBE4     IN A              Read A/D Subroutine  ;Read A/D data
3C3F   EEFF     XRI FF                             ;Invert data
3C41   57       MOV D,A
3C42   78       MOV A,B                            ;Is B Reg = 0? If not stay
3C43   E6FF     ANI FF                             ;in auto zero subroutine
3C45   C21A3D   JNZ Auto-Zero
3C48   C33D3D   JMP Normal
```

DS005671-A5

Note 29: All numerical values are hexadecimal representations.

FIGURE 21. Software for Auto-Zeroed Differential A/D

5.3 Multiple A/D Converters in a Z-80 Interrupt Driven Mode (Continued)

The following notes apply:

- It is assumed that the CPU automatically performs a RST 7 instruction when a valid interrupt is acknowledged (CPU is in interrupt mode 1). Hence, the subroutine starting address of X0038.
- The address bus from the Z-80 and the data bus to the Z-80 are assumed to be inverted by bus drivers.
- A/D data and identifying words will be stored in sequential memory locations starting at the arbitrarily chosen address X 3E00.
- The stack pointer must be dimensioned in the main program as the RST 7 instruction automatically pushes the PC onto the stack and the subroutine uses an additional 6 stack addresses.
- The peripherals of concern are mapped into I/O space with the following port assignments:

Functional Description (Continued)

HEX PORT ADDRESS	PERIPHERAL
00	MM74C374 8-bit flip-flop
01	A/D 1
02	A/D 2
03	A/D 3
04	A/D 4
05	A/D 5
06	A/D 6
07	A/D 7

This port address also serves as the A/D identifying word in the program.

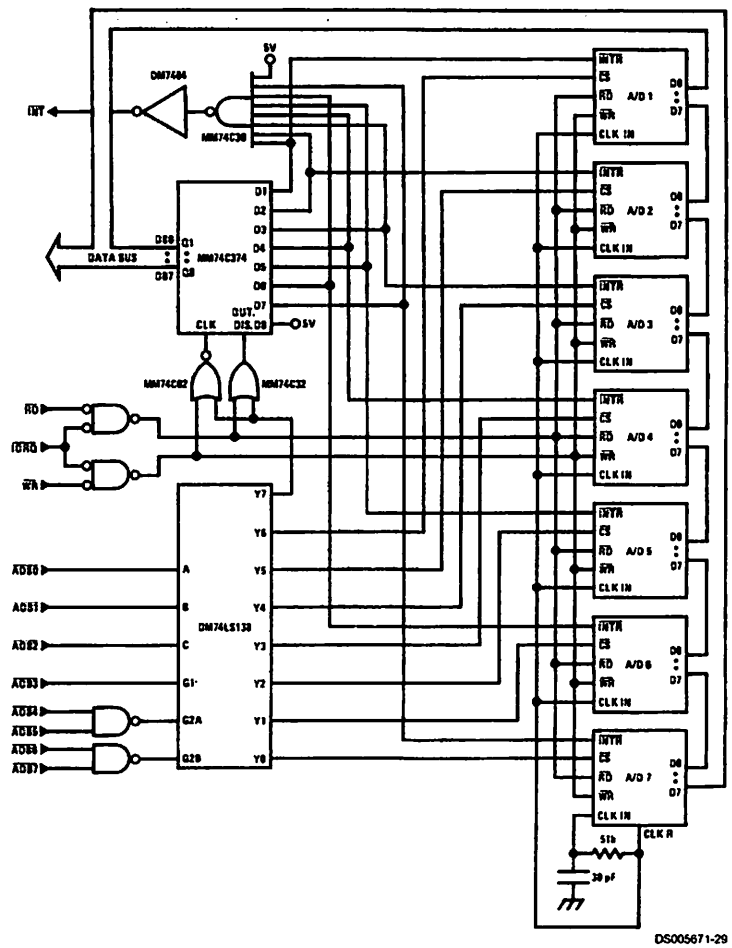


FIGURE 22. Multiple A/Ds with Z-80 Type Microprocessor

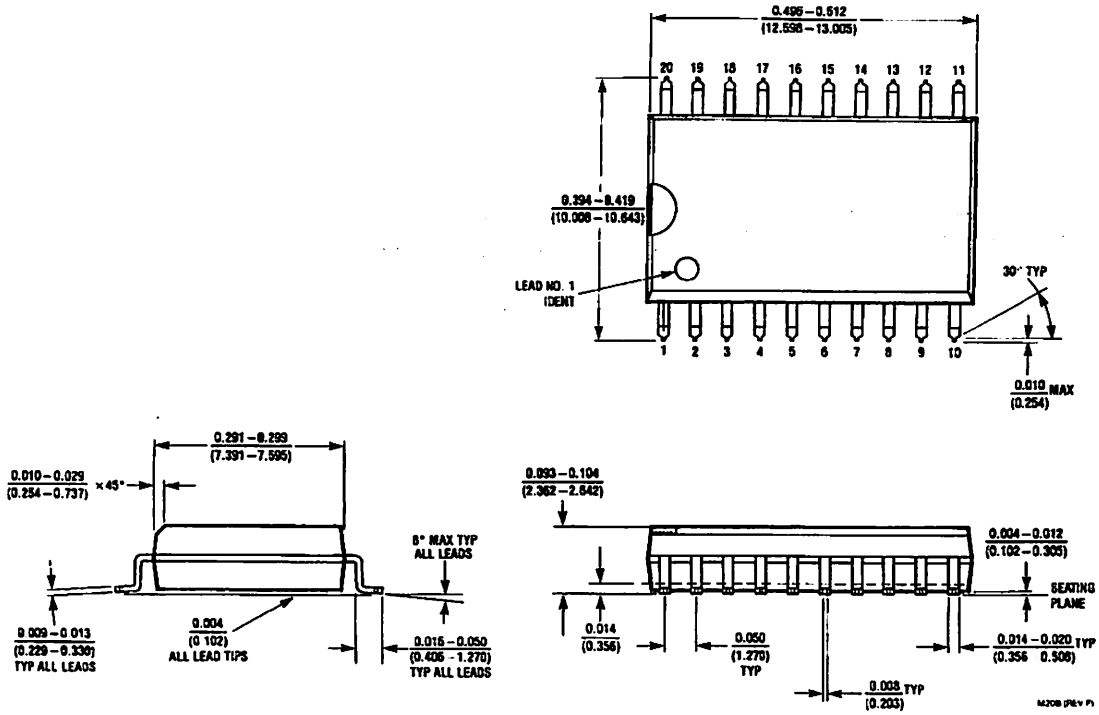
Functional Description (Continued)

INTERRUPT SERVICING SUBROUTINE

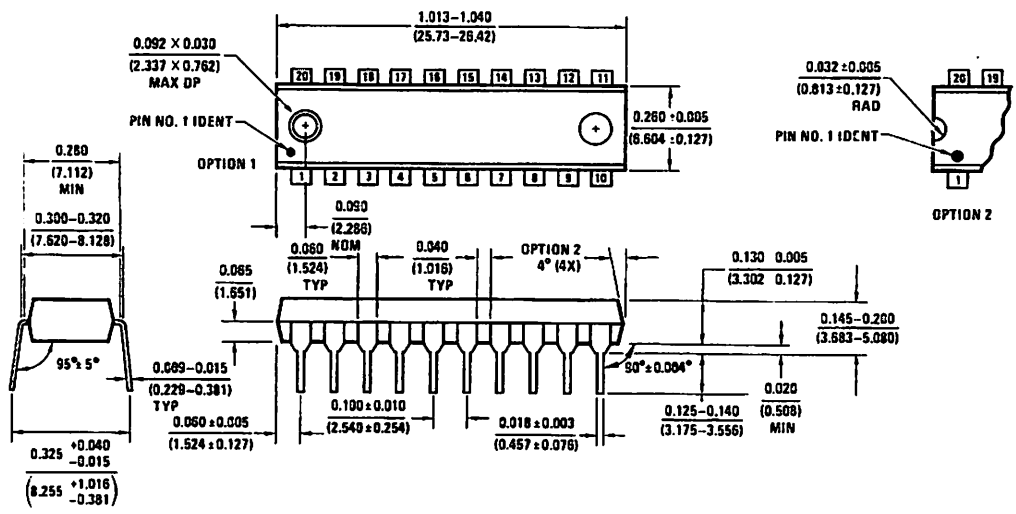
```
LOC   OBJ CODE      SOURCE STATEMENT      COMMENT
0038  E5            PUSH HL               ; Save contents of all registers affected by
0039  C5            PUSH BC               ; this subroutine.
003A  F5            PUSH AF               ; Assumed INT mode 1 earlier set.
003B  21 00 3E      LD (HL),X3E00         ; Initialize memory pointer where data will be stored.
003E  0E 01         LD C, X01             ; C register will be port ADDR of A/D converters.
0040  D300          OUT X00, A            ; Load peripheral status word into 8-bit latch.
0042  DB00          IN A, X00             ; Load status word into accumulator.
0044  47            LD B,A                ; Save the status word.
0045  79      TEST  LD A,C                ; Test to see if the status of all A/D's have
0046  FE 08         CP, X08               ; been checked. If so, exit subroutine
0048  CA 60 00       JPZ, DONE
004B  78            LD A,B                ; Test a single bit in status word by looking for
004C  1F            RRA                   ; a "1" to be rotated into the CARRY (an INT
004D  47            LD B,A                ; is loaded as a "1"). If CARRY is set then load
004E  DA 5500       JPC, LOAD             ; contents of A/D at port ADDR in C register.
0051  0C      NEXT  INC C                 ; If CARRY is not set, increment C register to point
0052  C3 4500       JP,TEST               ; to next A/D, then test next bit in status word.
0055  ED 78   LOAD  IN A, (C)             ; Read data from interrupting A/D and invert
0057  EE FF         XOR FF                ; the data.
0059  77            LD (HL),A             ; Store the data
005A  2C            INC L
005B  71            LD (HL),C             ; Store A/D identifier (A/D port ADDR).
005C  2C            INC L
005D  C3 51 00      JP,NEXT               ; Test next bit in status word.
0060  F1      DONE  POP AF                ; Re-establish all registers as they were
0061  C1           POP BC                 ; before the interrupt.
0062  E1           POP HL
0063  C9           RET                    ; Return to original program
```

DS005671-A5

Physical Dimensions inches (millimeters) unless otherwise noted



SO Package (M)
Order Number ADC0802LCWM or ADC0804LCWM
NS Package Number M20B



Molded Dual-In-Line Package (N)
Order Number ADC0801LCN, ADC0802LCN,
ADC0803LCN, ADC0804LCN or ADC0805LCN
NS Package Number N20A

Notes

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DATA SHEET

HEF4511B
MSI
BCD to 7-segment latch/decoder/driver

Product specification
File under Integrated Circuits, IC04

January 1995

Philips
Semiconductors

PHILIPS

BCD to 7-segment latch/decoder/driver

HEF4511B
MSI

DESCRIPTION

The HEF4511B is a BCD to 7-segment latch/decoder/driver with four address inputs (D_A to D_D), an active LOW latch enable input ($\overline{EL}$), an active LOW ripple blanking input ($\overline{BI}$), an active LOW lamp test input ($\overline{LT}$), and seven active HIGH n-p-n bipolar transistor segment outputs (O_a to O_g).

When $\overline{EL}$ is LOW, the state of the segment outputs (O_a to O_g) is determined by the data on D_A to D_D.
When $\overline{EL}$ goes HIGH, the last data present on D_A to D_D are stored in the latches and the segment outputs remain stable. When $\overline{LT}$ is LOW, all the segment outputs are HIGH independent of all other input conditions. With $\overline{LT}$ HIGH, a LOW on $\overline{BI}$ forces all segment outputs LOW. The inputs $\overline{LT}$ and $\overline{BI}$ do not affect the latch circuit.

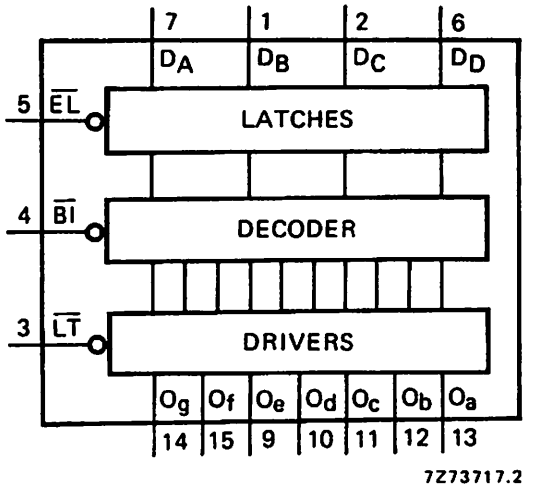


Fig.1 Functional diagram.

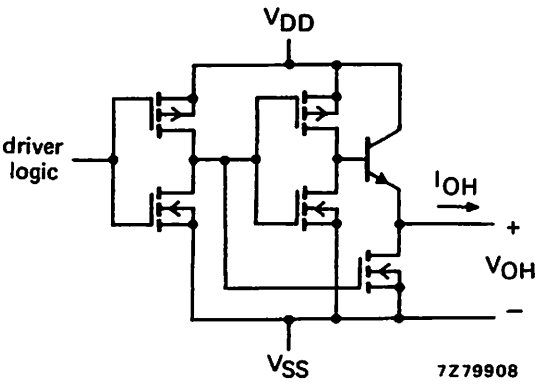


Fig.2 Pinning diagram.

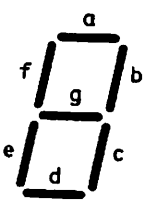
Fig.3 Schematic diagram of output stage.

HEF4511BP(N): 16-lead DIL; plastic (SOT38-1)
HEF4511BD(F): 16-lead DIL; ceramic (cerdip) (SOT74)
HEF4511BT(D): 16-lead SO; plastic (SOT109-1)
( ): Package Designator North America

PINNING

D_A to D_D	address (data) inputs
$\overline{EL}$	latch enable input (active LOW)
$\overline{BI}$	ripple blanking input (active LOW)
$\overline{LT}$	lamp test input (active LOW)
O_a to O_g	segment outputs

Fig.4 Segment designation.



FAMILY DATA, I_{DD} LIMITS category MSI

See Family Specifications

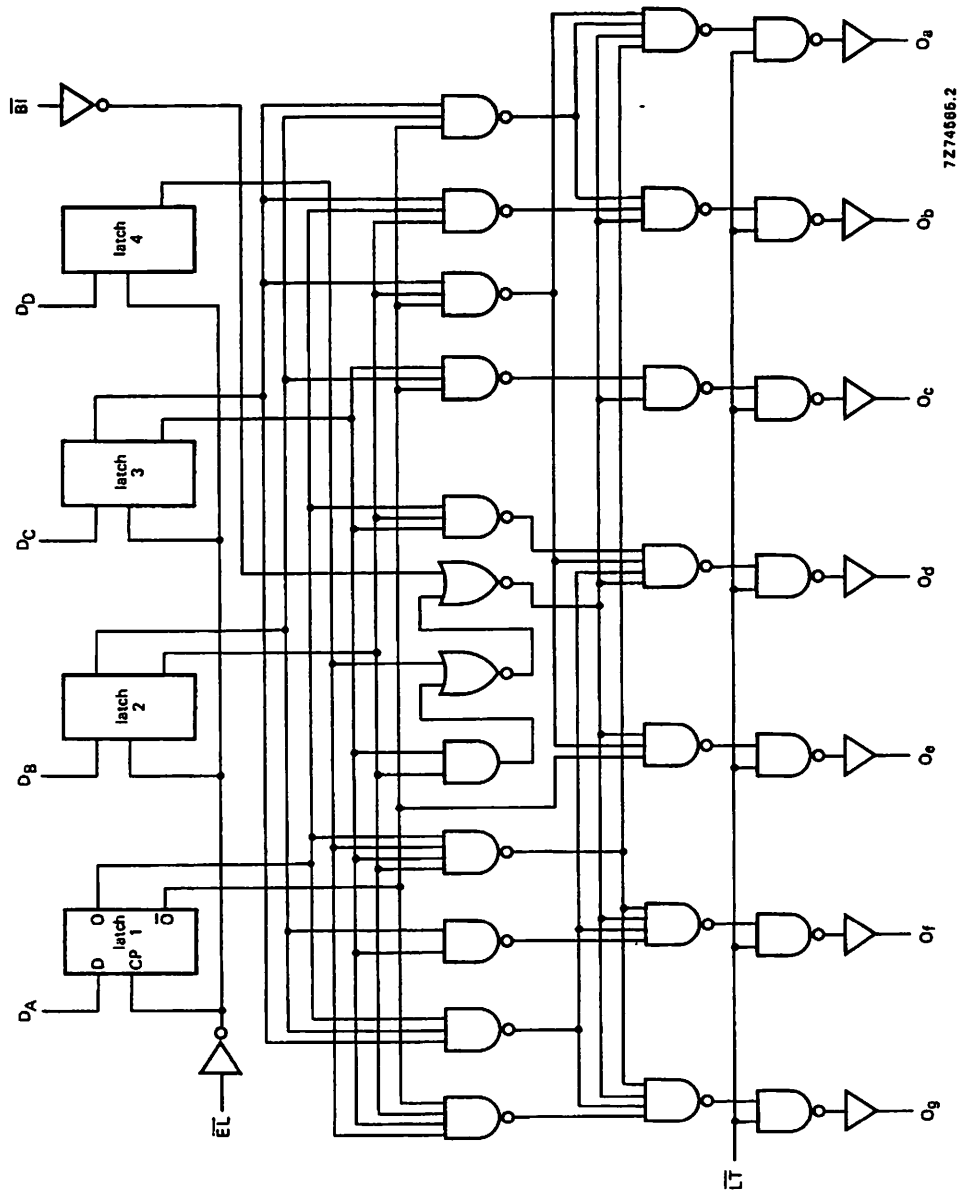


Fig.5 Logic diagram; for one latch see Fig.6.

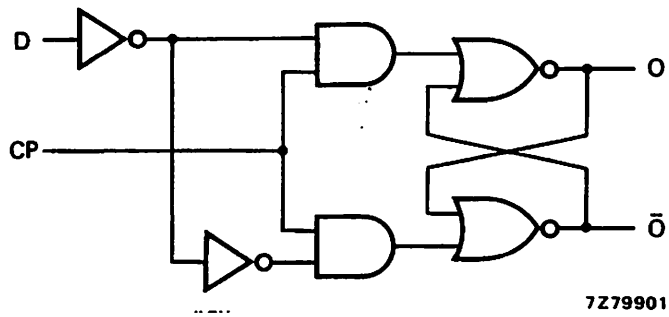


Fig.6 Logic diagram (one latch); see also Fig.5.

FUNCTION TABLE

INPUTS							OUTPUTS							
$\overline{EL}$	$\overline{BI}$	$\overline{LT}$	D_D	D_C	D_B	D_A	O_a	O_b	O_c	O_d	O_e	O_f	O_g	DISPLAY
X	X	L	X	X	X	X	H	H	H	H	H	H	H	8
X	L	H	X	X	X	X	L	L	L	L	L	L	L	blank
L	H	H	L	L	L	L	H	H	H	H	H	H	L	0
L	H	H	L	L	L	H	L	H	H	L	L	L	L	1
L	H	H	L	L	H	L	H	H	L	H	H	L	H	2
L	H	H	L	L	H	H	H	H	H	H	L	L	H	3
L	H	H	L	H	L	L	L	H	H	L	L	H	H	4
L	H	H	L	H	L	H	H	L	H	H	L	H	H	5
L	H	H	L	H	H	L	L	L	H	H	H	H	H	6
L	H	H	L	H	H	H	H	H	H	L	L	L	L	7
L	H	H	H	L	L	L	H	H	H	H	H	H	H	8
L	H	H	H	L	L	H	H	H	H	L	L	H	H	9
L	H	H	H	L	H	L	L	L	L	L	L	L	L	blank
L	H	H	H	L	H	H	L	L	L	L	L	L	L	blank
L	H	H	H	H	L	L	L	L	L	L	L	L	L	blank
L	H	H	H	H	L	H	L	L	L	L	L	L	L	blank
L	H	H	H	H	H	L	L	L	L	L	L	L	L	blank
L	H	H	H	H	H	H	L	L	L	L	L	L	L	blank
H	H	H	X	X	X	X				*				*

Note

1. H = HIGH state (the more positive voltage)
   L = LOW state (the less positive voltage)
   X = state is immaterial
   * Depends upon the BCD code applied during the LOW to HIGH transition of $\overline{EL}$.

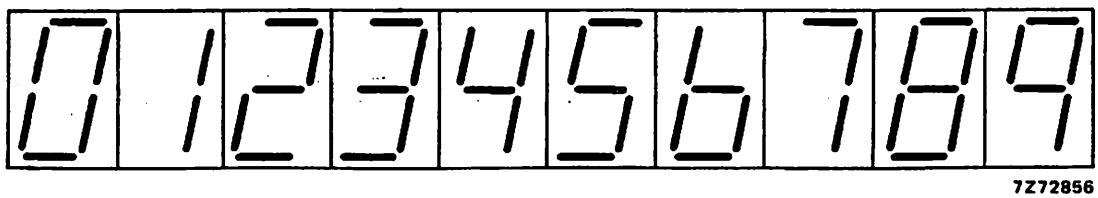


Fig.7 Display.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134).

Output (source) current HIGH	$-I_{OH}$	max.	25	mA

For other RATINGS see Family Specifications.

Note

1. A destructive high current mode may occur if V_I and V_O are not constrained to the range $V_{SS} \leq V_I$ or $V_O \leq V_{DD}$.

DC CHARACTERISTICS

V_{SS} = 0 V

HEF	V_{DD} V	I_{OH} mA	SYMBOL	T_{amb} (°C)						
				−40		+25		+85		
				MIN.	MAX.	MIN.	TYP.	MIN.	MAX.	
Output voltage	5	0		4,10		4,10	4,40	4,10		V
HIGH	10	0	V_{OH}	9,10		9,10	9,40	9,10		V
	15	0		14,10		14,10	14,40	14,10		V
Output voltage	5	5					4,20			V
HIGH	10	5	V_{OH}				9,20			V
	15	5					14,20			V
Output voltage	5	10		3,60		3,60	4,05	3,30		V
HIGH	10	10	V_{OH}	8,75		8,75	9,10	8,45		V
	15	10		13,75		13,75	14,10	13,45		V
Output voltage	5	15					4,00			V
HIGH	10	15	V_{OH}				9,00			V
	15	15					14,00			V
Output voltage	5	20		2,80		2,80	3,80	2,50		V
HIGH	10	20	V_{OH}	8,10		8,10	9,00	7,80		V
	15	20		13,10		13,10	14,00	12,80		V
Output voltage	5	25					3,70			V
HIGH	10	25	V_{OH}				8,90			V
	15	25					14,00			V

HEC	V_{DD} V	I_{OH} mA	SYMBOL	T_{amb} (°C)					
				−55		+ 25		+ 125	
				MIN.	MAX.	MIN.	TYP.	MIN.	MAX.
Output voltage	5	0		4,10		4,10	4,40	4,10	V
HIGH	10	0	V_{OH}	9,10		9,10	9,90	9,10	V
	15	0		14,10		14,10	14,40	14,40	V
Output voltage	5	5					4,30		V
HIGH	10	5	V_{OH}				9,30		V
	15	5					14,30		V
Output voltage	5	10		3,60		3,60	4,25	3,20	V
HIGH	10	10	V_{OH}	8,75		8,75	9,25	8,35	V
	15	10		13,75		13,75	14,25	13,35	V
Output voltage	5	15					4,20		V
HIGH	10	15	V_{OH}				9,20		V
	15	15					14,20		V
Output voltage	5	20		2,80		2,80	4,20	2,30	V
HIGH	10	20	V_{OH}	8,10		8,10	9,20	7,60	V
	15	20		13,10		13,10	14,20	12,60	V
Output voltage	5	25					4,15		V
HIGH	10	25	V_{OH}				9,20		V
	15	25					14,20		V

AC CHARACTERISTICS

V_{SS} = 0 V; T_{amb} = 25 °C; input transition times ≤ 20 ns

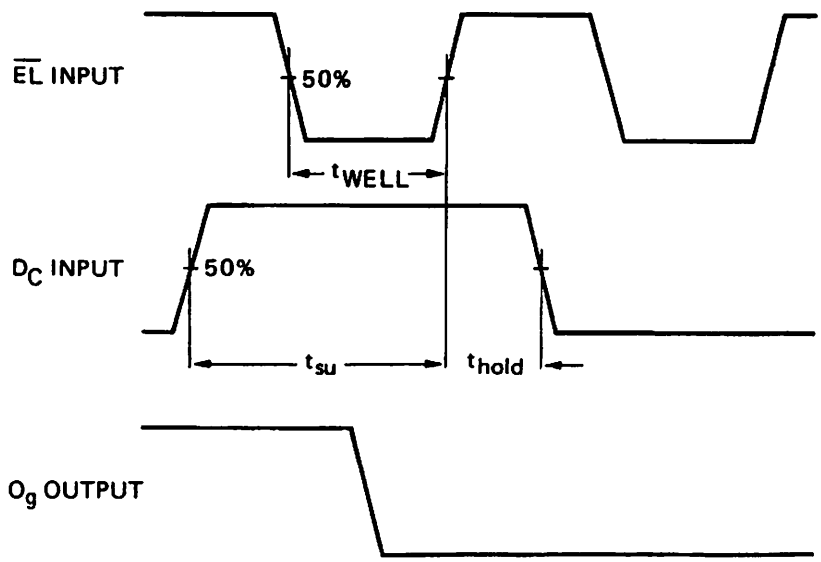
	V_{DD} V	TYPICAL FORMULA FOR P (μW)	
Dynamic power dissipation per package (P)	5	$1\,000\ f_i + \Sigma\ (f_o C_L) \times V_{DD}^2$	where
	10	$4\,000\ f_i + \Sigma\ (f_o C_L) \times V_{DD}^2$	f_i = input freq. (MHz)
	15	$10\,000\ f_i + \Sigma\ (f_o C_L) \times V_{DD}^2$	f_o = output freq. (MHz)
			C_L = load capacitance (pF)
			$\Sigma\ (f_o C_L)$ = sum of outputs
			V_{DD} = supply voltage (V)

AC CHARACTERISTICS

V_{SS} = 0 V; T_{amb} = 25 °C; C_L = 50 pF; input transition times ≤ 20 ns

	V_{DD} V	SYMBOL	MIN.	TYP.	MAX.		TYPICAL EXTRAPOLATION FORMULA
Propagation delays							
$D_n \rightarrow O_n$	5			155	310	ns	128 ns + (0,55 ns/pF) C_L
HIGH to LOW	10	t_{PHL}		60	120	ns	49 ns + (0,23 ns/pF) C_L
	15			40	80	ns	32 ns + (0,16 ns/pF) C_L
	5			135	270	ns	108 ns + (0,55 ns/pF) C_L
LOW to HIGH	10	t_{PLH}		55	110	ns	44 ns + (0,23 ns/pF) C_L
	15			40	80	ns	32 ns + (0,16 ns/pF) C_L
$\overline{EL} \rightarrow O_n$	5			160	320	ns	133 ns + (0,55 ns/pF) C_L
HIGH to LOW	10	t_{PHL}		60	120	ns	49 ns + (0,23 ns/pF) C_L
	15			45	90	ns	37 ns + (0,16 ns/pF) C_L
	5			160	320	ns	133 ns + (0,55 ns/pF) C_L
LOW to HIGH	10	t_{PLH}		70	140	ns	59 ns + (0,23 ns/pF) C_L
	15			50	100	ns	42 ns + (0,16 ns/pF) C_L
$\overline{BI} \rightarrow O_n$	5			120	240	ns	93 ns + (0,55 ns/pF) C_L
HIGH to LOW	10	t_{PHL}		50	100	ns	39 ns + (0,23 ns/pF) C_L
	15			35	70	ns	27 ns + (0,16 ns/pF) C_L
$\overline{BI} \rightarrow O_n$	5			105	210	ns	78 ns + (0,55 ns/pF) C_L
LOW to HIGH	10	t_{PLH}		40	80	ns	29 ns + (0,23 ns/pF) C_L
	15			30	60	ns	22 ns + (0,16 ns/pF) C_L
$\overline{LT} \rightarrow O_n$	5			80	160	ns	52 ns + (0,55 ns/pF) C_L
HIGH to LOW	10	t_{PHL}		30	60	ns	19 ns + (0,23 ns/pF) C_L
	15			20	40	ns	12 ns + (0,16 ns/pF) C_L
	5			60	120	ns	33 ns + (0,55 ns/pF) C_L
LOW to HIGH	10	t_{PLH}		30	60	ns	19 ns + (0,23 ns/pF) C_L
	15			25	50	ns	17 ns + (0,16 ns/pF) C_L
Output transition times	5			60	120	ns	10 ns + (1,0 ns/pF) C_L
HIGH to LOW	10	t_{THL}		30	60	ns	9 ns + (0,42 ns/pF) C_L
	15			20	40	ns	6 ns + (0,28 ns/pF) C_L
	5			25	50	ns	20 ns + (1,0 na/pF) C_L
LOW to HIGH	10	t_{TLH}		16	32	ns	13 ns + (0,06 ns/pF) C_L
	15			13	26	ns	10 ns + (0,06 ns/pF) C_L

	V_{DD} V	SYMBOL	MIN.	TYP.	MAX.		TYPICAL EXTRAPOLATION FORMULA
Minimum $\overline{EL}$	5		80	40		ns	
pulse width; LOW	10	t_{WELL}	40	20		ns	
	15		35	17		ns	
Set-up time	5		50	25		ns	see also waveforms Fig.8
$D_n \rightarrow \overline{EL}$	10	t_{su}	25	12		ns	
	15		20	9		ns	
Hold-time	5		60	30		ns	
$D_n \rightarrow \overline{EL}$	10	t_{hold}	30	15		ns	
	15		25	12		ns	



Conditions:
D_D = LOW
$D_A = D_B = \overline{B_I} = \overline{LT}$ = HIGH

Fig.8 Waveforms showing minimum $\overline{EL}$ pulse width, set-up and hold time for DC to $\overline{EL}$.

APPLICATION INFORMATION

Some examples of applications for the HEF4511B are:

- Driving LED displays.
- Driving incandescent displays.
- Driving fluorescent displays.
- Driving LCD displays.
- Driving gas discharge displays.

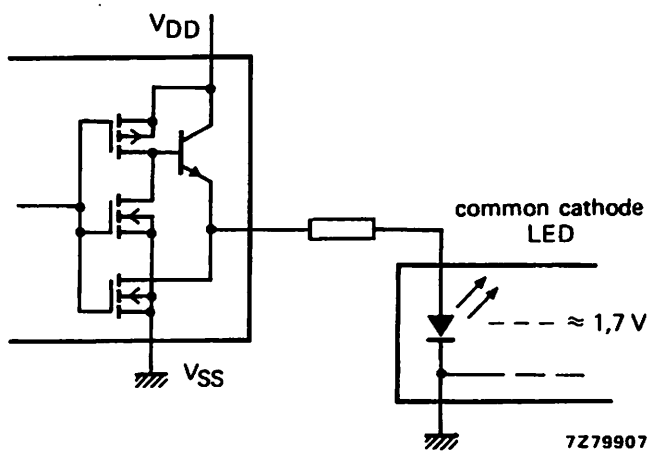


Fig.9 Connection to common cathode LED display readout.

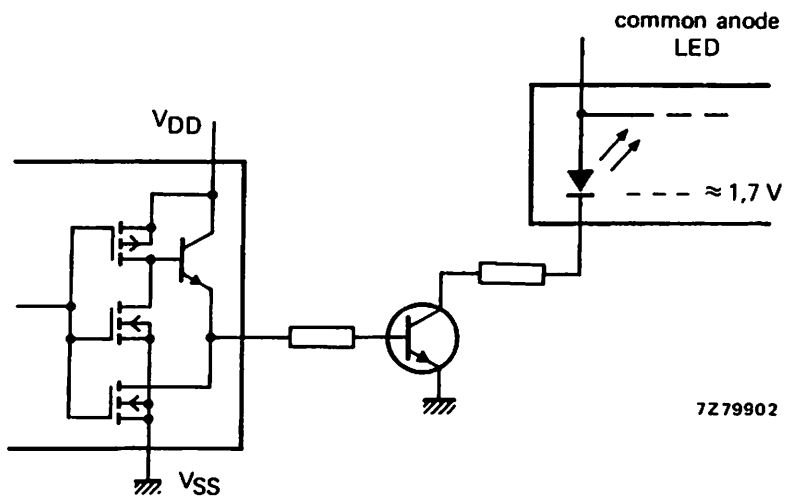
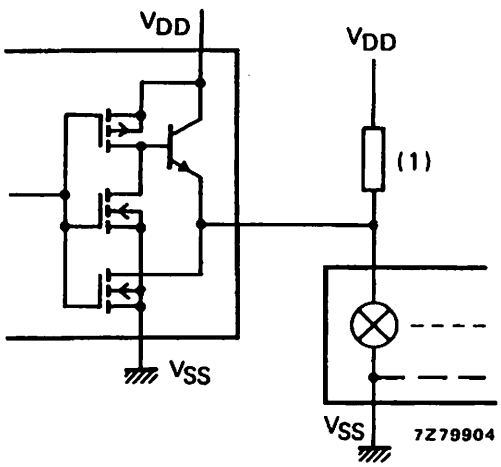


Fig.10 Connection to common anode LED display readout.



(1) A filament pre-warm resistor is recommended to reduce filament thermal shock and increase the effective cold resistance of the filament.

Fig.11 Connection to incandescent display readout.

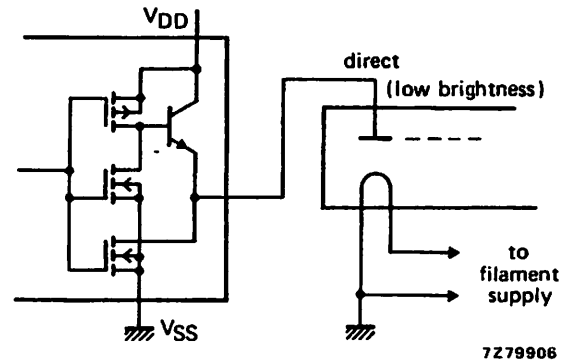


Fig.12 Connection to fluorescent display readout.

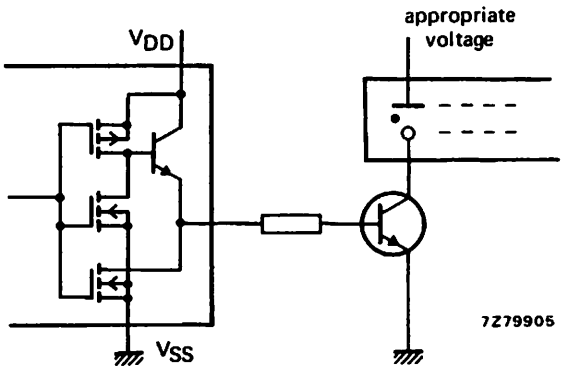


Fig.13 Connection to gas discharge display readout.

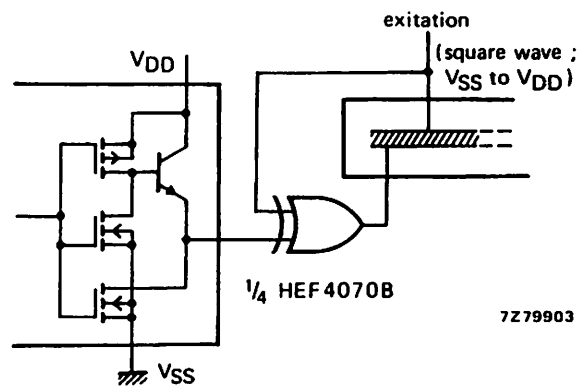


Fig.14 Connection to liquid crystal (LCD) display readout. Direct d.c. drive of LCDs not recommended for life of LCD readouts.

HEWLETT® PACKARD

Low Current Seven Segment Displays

Technical Data

HDSP-335X Series
HDSP-555X Series
HDSP-751X Series
HDSP-A10X Series
HDSP-A80X Series
HDSP-A90X Series
HDSP-E10X Series
HDSP-F10X Series
HDSP-G10X Series
HDSP-H10X Series
HDSP-K12X, K70X Series
HDSP-N10X Series

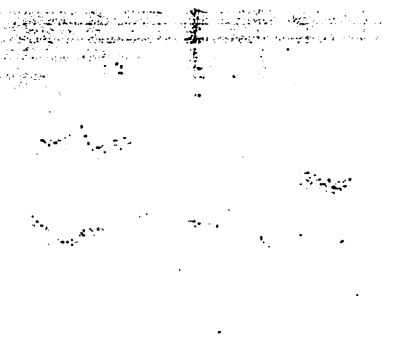
Features

- **Low Power Consumption**
- **Industry Standard Size**
- **Industry Standard Pinout**
- **Choice of Character Size**
  7.6 mm (0.30 in), 10 mm (0.40 in), 10.9 mm (0.43 in), 14.2 mm (0.56 in), 20 mm (0.80 in)
- **Choice of Colors**
  AlGaAs Red, High Efficiency Red (HER), Yellow, Green
- **Excellent Appearance**
  Evenly Lighted Segments
  ± 50° Viewing Angle
- **Design Flexibility**
  Common Anode or Common Cathode
  Single and Dual Digit
  Left and Right Hand Decimal Points
  ± 1. Overflow Character
- **Categorized for Luminous Intensity**
  Yellow and Green Categorized for Color
  Use of Like Categories Yields a Uniform Display
- **Excellent for Long Digit String Multiplexing**

Description

These low current seven segment displays are designed for applications requiring low power consumption. They are tested and selected for their excellent low current characteristics to ensure that the segments are matched at low currents. Drive currents as low as 1 mA per segment are available.

Pin for pin equivalent displays are also available in a standard current or high light ambient design. The standard current displays are available in all colors and are ideal for most applications. The high light ambient displays are ideal for sunlight ambients or long string lengths. For additional information see the 7.6 mm Micro Bright Seven Segment Displays, 10 mm Seven Segment Displays, 7.6 mm/10.9 mm Seven Segment Displays, 14.2 mm Seven Segment Displays, 20 mm Seven Segment Displays, or High Light Ambient Seven Segment Displays data sheets.

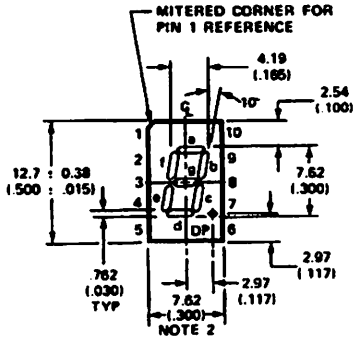


Devices

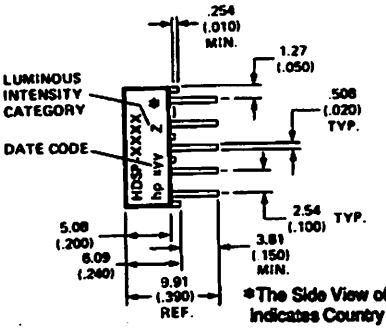
AlGaAs HDSP-	HER HDSP-	Yellow HDSP-	Green HDSP-	Description	Package Drawing
A101	7511	A801	A901	7.6 mm Common Anode Right Hand Decimal	A
A103	7513	A803	A903	7.6 mm Common Cathode Right Hand Decimal	B
A107	7517	A807	A907	7.6 mm Common Anode ± 1. Overflow	C
A108	7518	A808	A908	7.6 mm Common Cathode ± 1. Overflow	D
F101				10 mm Common Anode Right Hand Decimal	E
F103				10 mm Common Cathode Right Hand Decimal	F
F107				10 mm Common Anode ± 1. Overflow	G
F108				10 mm Common Cathode ± 1. Overflow	H
G101				10 mm Two Digit Common Anode Right Hand Decimal	X
G103				10 mm Two Digit Common Cathode Right Hand Decimal	Y
E100	3350			10.9 mm Common Anode Left Hand Decimal	I
E101	3351			10.9 mm Common Anode Right Hand Decimal	J
E103	3353			10.9 mm Common Cathode Right Hand Decimal	K
E106	3356			10.9 mm Universal ± 1. Overflow[1]	L
H101	5551			14.2 mm Common Anode Right Hand Decimal	M
H103	5553			14.2 mm Common Cathode Right Hand Decimal	N
H107	5557			14.2 mm Common Anode ± 1. Overflow	O
H108	5558			14.2 mm Common Cathode ± 1. Overflow	P
K121	K701			14.2 mm Two Digit Common Anode Right Hand Decimal	R
K123	K703			14.2 mm Two Digit Common Cathode Right Hand Decimal	S
N100				20 mm Common Anode Left Hand Decimal	Q
N101				20 mm Common Anode Right Hand Decimal	T
N103				20 mm Common Cathode Right Hand Decimal	U
N105				20 mm Common Cathode Left Hand Decimal	V
N106				20 mm Universal ± 1. Overflow[1]	W

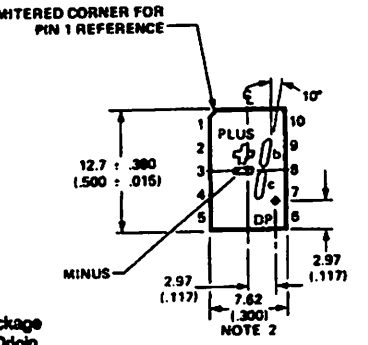
Note:
1. Universal pinout brings the anode and cathode of each segment's LED out to separate pins. See internal diagrams L or W.

Package Dimensions

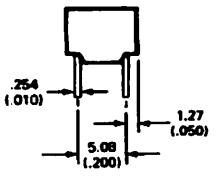


A, B





C, D

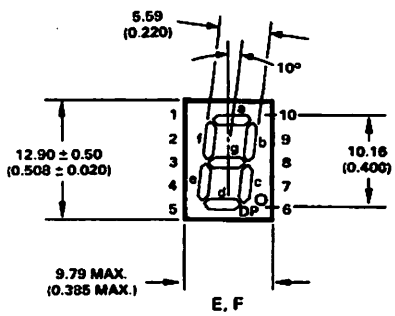


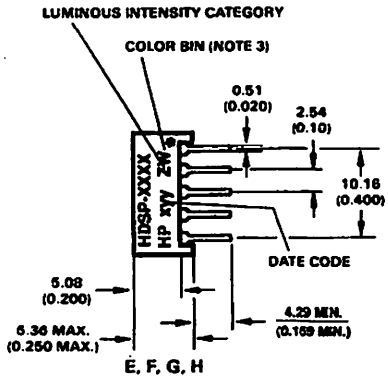
A, B, C, D

PIN	FUNCTION			
	A	B	C	D
1	ANODE[4]	CATHODE[5]	ANODE[4]	CATHODE[5]
2	CATHODE f	ANODE f	CATHODE PLUS	ANODE PLUS
3	CATHODE g	ANODE g	CATHODE MINUS	ANODE MINUS
4	CATHODE e	ANODE e	NC	NC
5	CATHODE d	ANODE d	NC	NC
6	ANODE[4]	CATHODE[5]	ANODE[4]	CATHODE[5]
7	CATHODE DP	ANODE DP	CATHODE DP	ANODE DP
8	CATHODE c	ANODE c	CATHODE c	ANODE c
9	CATHODE b	ANODE b	CATHODE b	ANODE b
10	CATHODE a	ANODE a	NC	NC

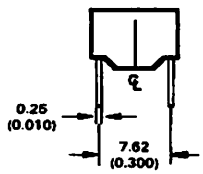
NOTES:
1. ALL DIMENSIONS IN MILLIMETRES (INCHES).
2. MAXIMUM.
3. ALL UNTOLERANCED DIMENSIONS ARE FOR REFERENCE ONLY.
4. REDUNDANT ANODES.
5. REDUNDANT CATHODES.

Package Dimensions (cont.)

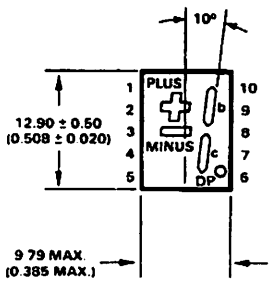




* The Side View of package indicates Country of Origin.

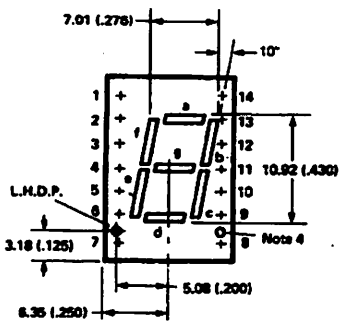


	FUNCTION			
PIN	E	F	G	H
1	ANODE[4]	CATHODE[5]	ANODE[4]	CATHODE[5]
2	CATHODE f	ANODE f	CATHODE PLUS	ANODE PLUS
3	CATHODE g	ANODE g	CATHODE MINUS	ANODE MINUS
4	CATHODE e	ANODE e	NC	NC
5	CATHODE d	ANODE d	NC	NC
6	ANODE[4]	CATHODE[5]	ANODE[4]	CATHODE[5]
7	CATHODE DP	ANODE DP	CATHODE DP	ANODE DP
8	CATHODE c	ANODE c	CATHODE c	ANODE c
9	CATHODE b	ANODE b	CATHODE b	ANODE b
10	CATHODE a	ANODE a	NC	NC



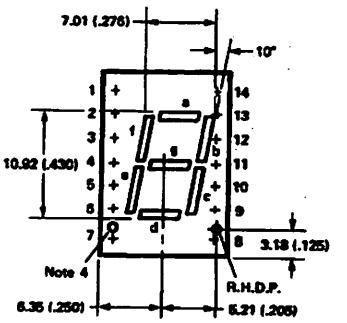
NOTES:
1. ALL DIMENSIONS IN MILLIMETRES (INCHES).
2. ALL UNTOLERANCED DIMENSIONS ARE FOR REFERENCE ONLY.
3. FOR YELLOW AND GREEN SERIES PRODUCT ONLY.
4. REDUNDANT ANODES.
5. REDUNDANT CATHODES.

Package Dimensions (cont.)



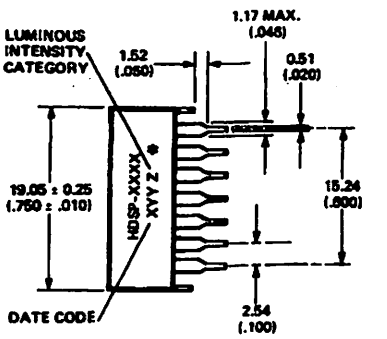
I

FRONT VIEW



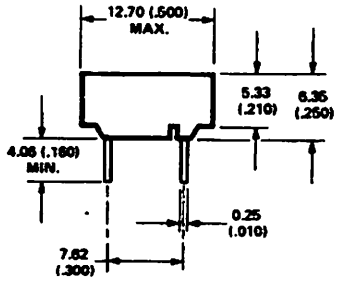
J, K

FRONT VIEW



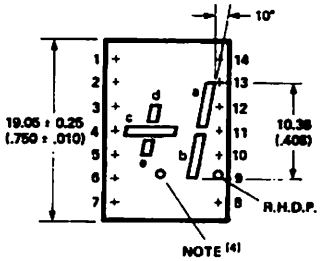
SIDE VIEW

*The Side View of package indicates Country of Origin.



END VIEW

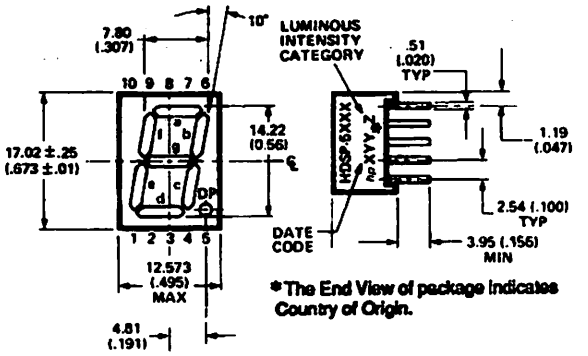
PIN	FUNCTION			
	I	J	K	L
1	CATHODE-e	CATHODE-e	ANODE e	CATHODE-d
2	CATHODE-f	CATHODE-f	ANODE-f	ANODE-d
3	ANODE[3]	ANODE[3]	CATHODE[6]	NO PIN
4	NO PIN	NO PIN	NO PIN	CATHODE-c
5	NO PIN	NO PIN	NO PIN	CATHODE-e
6	CATHODE-dp	NO CONN.[5]	NO CONN.[5]	ANODE-e
7	CATHODE-e	CATHODE-e	ANODE-e	ANODE-c
8	CATHODE-d	CATHODE-d	ANODE-d	ANODE-dp
9	NO CONN.[5]	CATHODE-dp	ANODE-dp	CATHODE-dp
10	CATHODE-c	CATHODE-c	ANODE-c	CATHODE-b
11	CATHODE-g	CATHODE-g	ANODE-g	CATHODE a
12	NO PIN	NO PIN	NO PIN	NO PIN
13	CATHODE-b	CATHODE-b	ANODE-b	ANODE-a
14	ANODE[3]	ANODE[3]	CATHODE[6]	ANODE-b



L

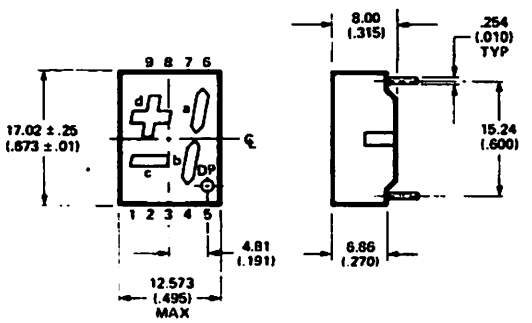
NOTES:
1. ALL DIMENSIONS IN MILLIMETRES (INCHES).
2. ALL UNTOLERANCED DIMENSIONS ARE FOR REFERENCE ONLY.
3. REDUNDANT ANODES.
4. UNUSED dp POSITION.
5. SEE INTERNAL CIRCUIT DIAGRAM.
6. REDUNDANT CATHODES.
7. SEE PART NUMBER TABLE FOR L.H.D.P. AND R.H.D.P. DESIGNATION.

Package Dimensions (cont.)



M, N
FRONT VIEW

M, N, O, P
TOP END VIEW



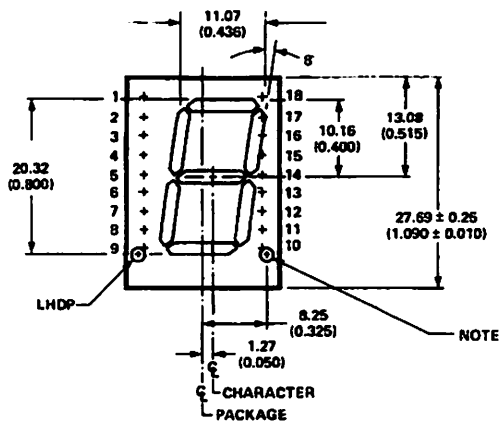
FRONT VIEW O, P

SIDE VIEW M, N, O, P

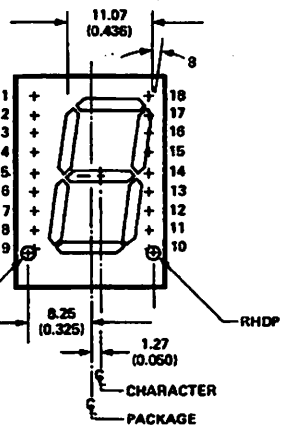
PIN	FUNCTION			
	M	N	O	P
1	CATHODE e	ANODE e	CATHODE c	ANODE c
2	CATHODE d	ANODE d	ANODE c, d	CATHODE c, d
3	ANODE[4]	CATHODE[5]	CATHODE b	ANODE b
4	CATHODE c	ANODE c	ANODE a, b, DP	CATHODE a, b, DP
5	CATHODE DP	ANODE DP	CATHODE DP	ANODE DP
6	CATHODE b	ANODE b	CATHODE a	ANODE a
7	CATHODE a	ANODE a	ANODE a, b, DP	CATHODE a, b, DP
8	ANODE[4]	CATHODE[5]	ANODE c, d	CATHODE c, d
9	CATHODE f	ANODE f	CATHODE d	ANODE d
10	CATHODE g	ANODE g	NO PIN	NO PIN

NOTES:
1. ALL DIMENSIONS IN MILLIMETRES (INCHES).
2. MAXIMUM.
3. ALL UNTOLERANCED DIMENSIONS ARE FOR REFERENCE ONLY.
4. REDUNDANT ANODES.
5. REDUNDANT CATHODES.

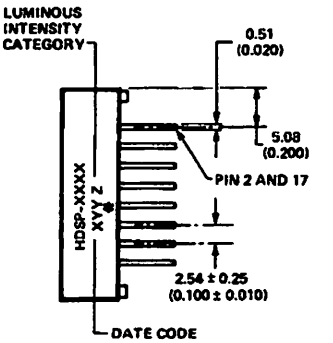
Package Dimensions (cont.)



FRONT VIEW Q, V

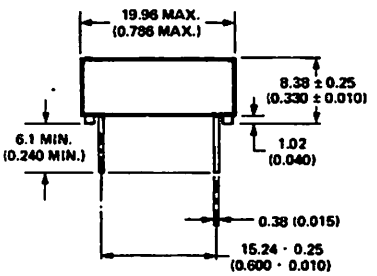


FRONT VIEW T, U



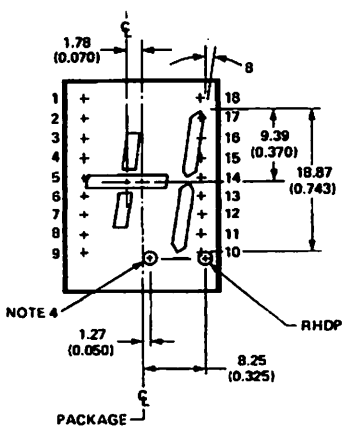
SIDE VIEW Q, T, U, V, W

*The Side View of package indicates Country of Origin.



END VIEW Q, T, U, V, W

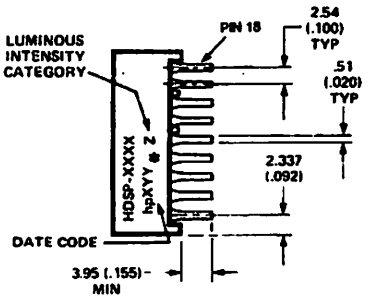
Pin	Function				
	Q	T	U	V	W
1	NO PIN	NO PIN	NO PIN	NO PIN	NO PIN
2	CATHODE a	CATHODE a	ANODE a	ANODE a	CATHODE a
3	CATHODE f	CATHODE f	ANODE f	ANODE f	ANODE d
4	ANODE[3]	ANODE[3]	CATHODE[6]	CATHODE[6]	CATHODE d
5	CATHODE e	CATHODE e	ANODE e	ANODE e	CATHODE c
6	ANODE[3]	ANODE[3]	CATHODE[6]	CATHODE[6]	CATHODE e
7	CATHODE dp	NO CONNEC	NO CONNEC	ANODE dp	ANODE e
8	NO PIN	NO PIN	NO PIN	NO PIN	CATHODE dp
9	NO PIN	NO PIN	NO PIN	NO PIN	NO PIN
10	NO PIN	CATHODE dp	ANODE dp	NO PIN	ANODE dp
11	CATHODE d	CATHODE d	ANODE d	ANODE d	CATHODE dp
12	ANODE[3]	ANODE[3]	CATHODE[6]	CATHODE[6]	CATHODE b
13	CATHODE c	CATHODE c	ANODE c	ANODE c	ANODE b
14	CATHODE g	CATHODE g	ANODE g	ANODE g	ANODE c
15	CATHODE b	CATHODE b	ANODE b	ANODE b	ANODE a
16	NO PIN	NO PIN	NO PIN	NO PIN	NO PIN
17	ANODE[3]	ANODE[3]	CATHODE[6]	CATHODE[6]	CATHODE a
18	NO PIN	NO PIN	NO PIN	NO PIN	NO PIN



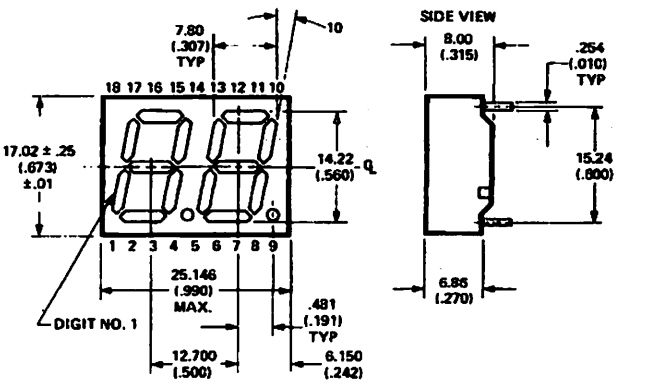
FRONT VIEW W

NOTES:
1. ALL DIMENSIONS IN MILLIMETRES (INCHES).
2. ALL UNTOLERANCED DIMENSIONS ARE FOR REFERENCE ONLY.
3. REDUNDANT ANODES.
4. UNUSED dp POSITION.
5. SEE INTERNAL CIRCUIT DIAGRAM.
6. REDUNDANT CATHODES.
7. SEE PART NUMBER TABLE FOR L.H.D.P. AND R.H.D.P. DESIGNATION.

Package Dimensions (cont.)

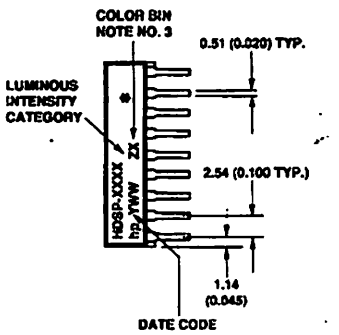


TOP END VIEW R, S

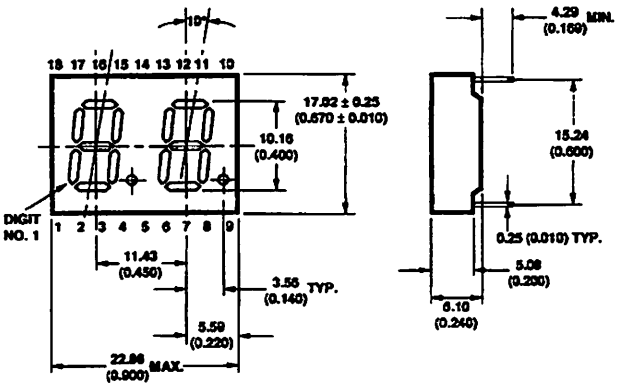


FRONT VIEW R, S

*The Side View of package indicates Country of Origin.



TOP END VIEW X, Y



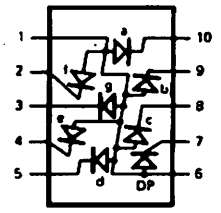
FRONT VIEW X, Y

*The Side View of package indicates Country of Origin.

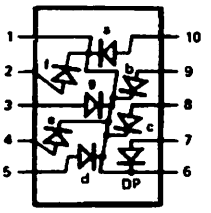
Pin	Function	
	R,X	S,Y
1	E CATHODE NO. 1	E ANODE NO. 1
2	D CATHODE NO. 1	D ANODE NO. 1
3	C CATHODE NO. 1	C ANODE NO. 1
4	DP CATHODE NO. 1	DP ANODE NO. 1
5	E CATHODE NO. 2	E ANODE NO. 2
6	D CATHODE NO. 2	D ANODE NO. 2
7	G CATHODE NO. 2	G ANODE NO. 2
8	C CATHODE NO. 2	C ANODE NO. 2
9	DP CATHODE NO. 2	DP ANODE NO. 2
10	B CATHODE NO. 2	B ANODE NO. 2
11	A CATHODE NO. 2	A ANODE NO. 2
12	F CATHODE NO. 2	F ANODE NO. 2
13	DIGIT NO. 2 ANODE	DIGIT NO. 2 CATHODE
14	DIGIT NO. 1 ANODE	DIGIT NO. 1 CATHODE
15	B CATHODE NO. 1	B ANODE NO. 1
16	A CATHODE NO. 1	A ANODE NO. 1
17	G CATHODE NO. 1	G ANODE NO. 1
18	F CATHODE NO. 1	F ANODE NO. 1

NOTES:
1. DIMENSIONS ARE IN MILLIMETRES (INCHES).
2. ALL UNTOLERANCED DIMENSIONS ARE FOR REFERENCE ONLY.
3. WHERE APPLICABLE.

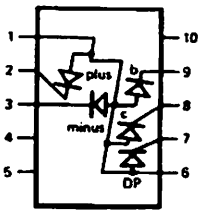
Internal Circuit Diagram



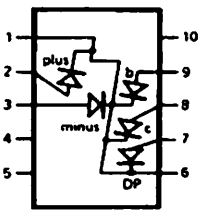
A, E



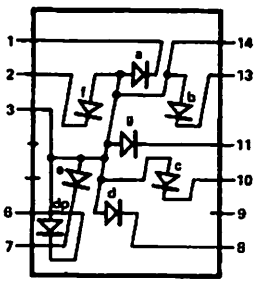
B, F



C, G



D, H



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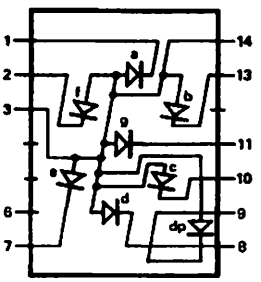

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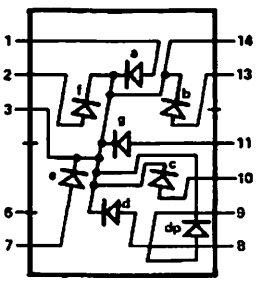
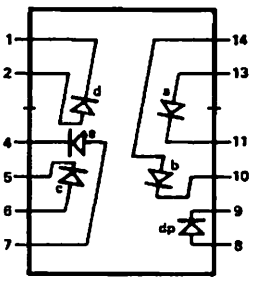


K



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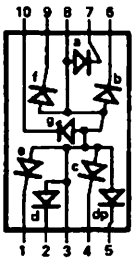

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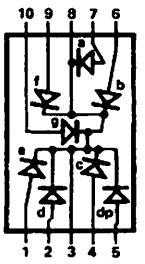

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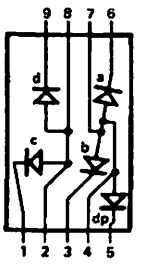
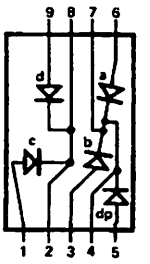
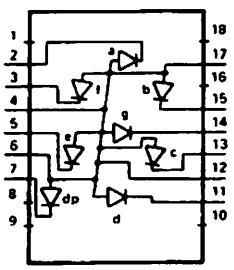


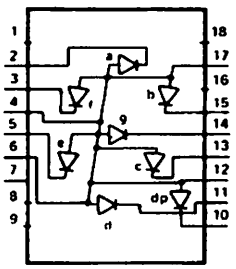
O



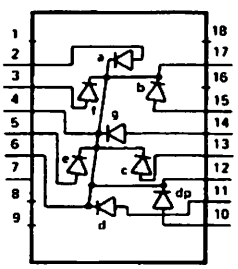
P



Q



T



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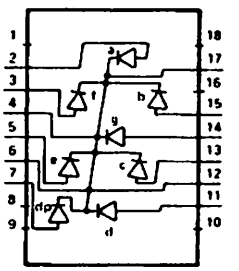
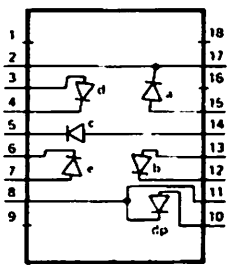
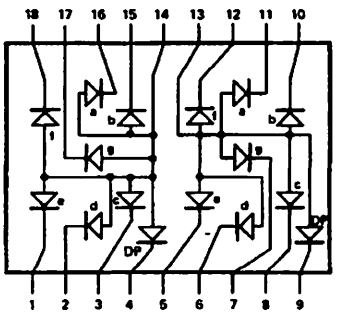


V

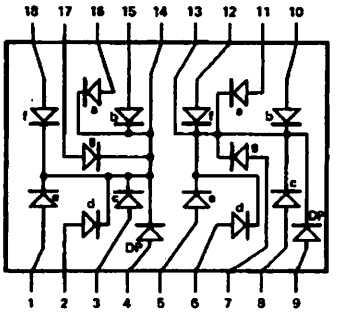


W

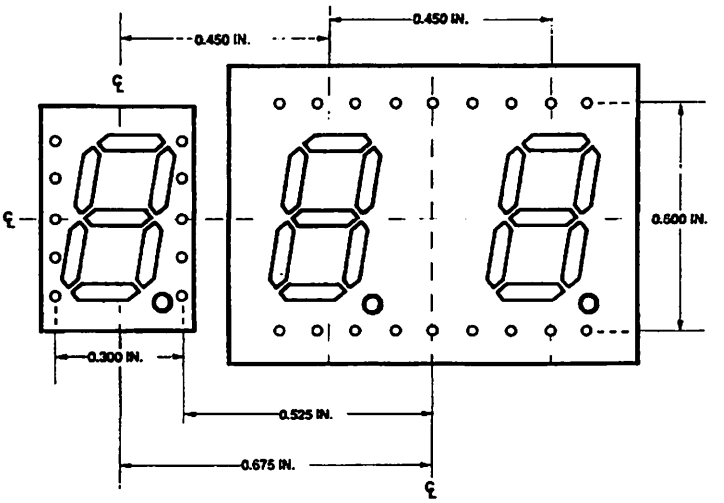
Internal Circuit Diagram (cont.)



R, X



S, Y



HOLE PATTERN FOR PCB LAYOUT TO ACHIEVE UNIFORM 0.450 in. DIGIT TO DIGIT PITCH. FOR HDSP-FXXX TO HDSP-GXXX.

Absolute Maximum Ratings

Description	AlGaAs Red HDSP-A10X/E10X/ H10X/K12X/N10X/ F10X, G10X Series	HER HDSP-751X/ 335X/555X/ K70X Series	Yellow HDSP-A80X Series	Green HDSP-A90X Series	Units
Average Power per Segment or DP	37	52		64	mW
Peak Forward Current per Segment or DP	45				mA
DC Forward Current per Segment or DP	15[1]	15[2]			mA
Operating Temperature Range	-20 to +100	-40 to +100			°C
Storage Temperature Range	-55 to +100				°C
Reverse Voltage per Segment or DP	3.0				V
Lead Solder Temperature for 3 Seconds (1.60 mm [0.063 in.] below seating plane)	260				°C

Notes:
1. Derate above 91°C at 0.53 mA/°C.
2. Derate HER/Yellow above 80°C at 0.38 mA/°C and Green above 71°C at 0.31 mA/°C.

Electrical/Optical Characteristics at T_A = 25°C

AlGaAs Red

Device Series HDSP-	Parameter	Symbol	Min.	Typ.	Max.	Units	Test Conditions
A10X	Luminous Intensity/Segment[1,2] (Digit Average)	I_V	315	600		µcd	I_F = 1 mA
				3600			I_F = 5 mA
F10X, G10X			330	650			I_F = 1 mA
				3900			I_F = 5 mA
E10X			390	650			I_F = 1 mA
				3900			I_F = 5 mA
H10X, K12X			400	700			I_F = 1 mA
				4200			I_F = 5 mA
N10X			270	590			I_F = 1 mA
				3500			I_F = 5 mA
All Devices	Forward Voltage/Segment or DP	V_F		1.6		V	I_F = 1 mA
				1.7			I_F = 5 mA
				1.8	2.2		I_F = 20 mA Pk
	Peak Wavelength	λ_{PEAK}		645		nm	
	Dominant Wavelength[3]	λ_d		637		nm	
	Reverse Voltage/Segment or DP[4]	V_R	3.0	15		V	I_R = 100 mA
	Temperature Coefficient of V_F/Segment or DP	ΔV_F/°C		-2 mV		mV/°C	
A10X	Thermal Resistance LED Junction-to-Pin	$R\theta_{J\text{-}PIN}$		255		°C/W/Seg	
F10X, G10X				320			
E10X				340			
H10X, K12X				400			
N10X				430			

High Efficiency Red

Device Series HDSP-	Parameter	Symbol	Min.	Typ.	Max.	Units	Test Conditions
751X	Luminous Intensity/Segment[1,2] (Digit Average)	I_V	160	270		mcd	I_F = 2 mA
				1050			I_F = 5 mA
335X, 555X, K70X			200	300			I_F = 2 mA
				1200			I_F = 5 mA
			270	370			I_F = 2 mA
				1480			I_F = 5 mA
All Devices	Forward Voltage/Segment or DP	V_F		1.6		V	I_F = 2 mA
				1.7			I_F = 5 mA
				2.1	2.5		I_F = 20 mA Pk
	Peak Wavelength	λ_{PEAK}		635		nm	
	Dominant Wavelength[3]	λ_d		626		nm	
	Reverse Voltage/Segment or DP[4]	V_R	3.0	30		V	I_R = 100 mA
	Temperature Coefficient of V_F/Segment or DP	$\Delta V_F/°C$		-2		mV/°C	
751X	Thermal Resistance LED Junction-to-Pin	$R\theta_{J\text{-}PIN}$		200		°C/W	
335X				280			
555X, K70X				345			

Yellow

Device Series HDSP-	Parameter	Symbol	Min.	Typ.	Max.	Units	Test Conditions
A80X	Luminous Intensity/Segment[1,2] (Digit Average)	I_V	250	420		mcd	I_F = 4 mA
				1300			I_F = 10 mA
	Forward Voltage/Segment or DP	V_F		1.7		V	I_F = 4 mA
				1.8			I_F = 5 mA
				2.1	2.5		I_F = 20 mA Pk
	Peak Wavelength	λ_{PEAK}		583		nm	
	Dominant Wavelength[3,5]	λ_d	581.5	585	592.5	nm	
	Reverse Voltage/Segment or DP[4]	V_R	3.0	30		V	I_R = 100 mA
	Temperature Coefficient of V_F/Segment or DP	ΔV_F/°C		-2		mV/°C	
	Thermal Resistance LED Junction-to-Pin	$R\theta_{J\text{-}PIN}$		200		°C/W	

Green

Device Series HDSP-	Parameter	Symbol	Min.	Typ.	Max.	Units	Test Conditions
A90X	Luminous Intensity/Segment[1,2] (Digit Average)	I_V	250	475		mcd	I_F = 4 mA
				1500			I_F = 10 mA
	Forward Voltage/Segment or DP	V_F		1.9		V	I_F = 4 mA
				2.0			I_F = 10 mA
				2.1	2.5		I_F = 20 mA Pk
	Peak Wavelength	λ_{PEAK}		566		nm	
	Dominant Wavelength[3,5]	λ_d		571	577	nm	
	Reverse Voltage/Segment or DP[4]	V_R	3.0	30		V	I_R = 100 mA
	Temperature Coefficient of V_F/Segment or DP	ΔV_F/°C		-2		mV/°C	
	Thermal Resistance LED Junction-to-Pin	$R\theta_{J\text{-}PIN}$		200		°C/W	

Notes:
1. Device case temperature is 25°C prior to the intensity measurement.
2. The digits are categorized for luminous intensity. The intensity category is designated by a letter on the side of the package.
3. The dominant wavelength, λ_d, is derived from the CIE chromaticity diagram and is the single wavelength which defines the color of the device.
4. Typical specification for reference only. Do not exceed absolute maximum ratings.
5. The yellow (HDSP-A800) and Green (HDSP-A900) displays are categorized for dominant wavelength. The category is designated by a number adjacent to the luminous intensity category letter.

AlGaAs Red

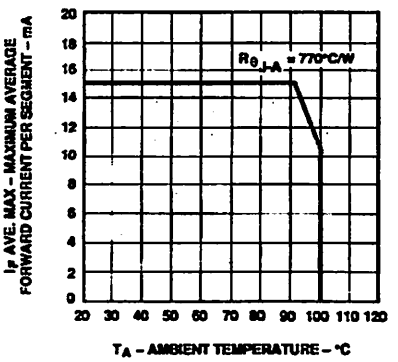


Figure 1. Maximum Allowable Average or DC Current vs. Ambient Temperature.

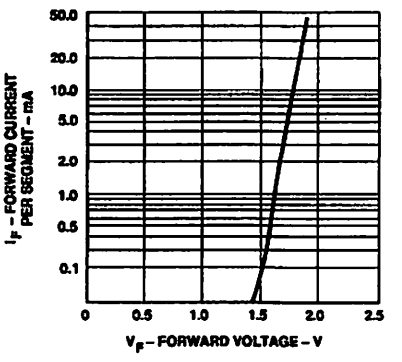


Figure 2. Forward Current vs. Forward Voltage.

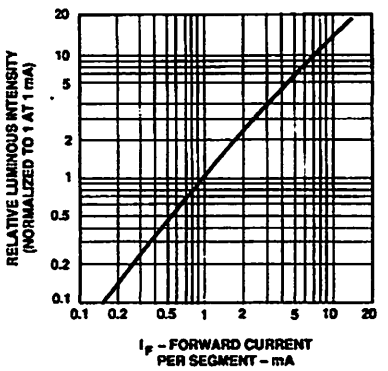


Figure 3. Relative Luminous Intensity vs. DC Forward Current.

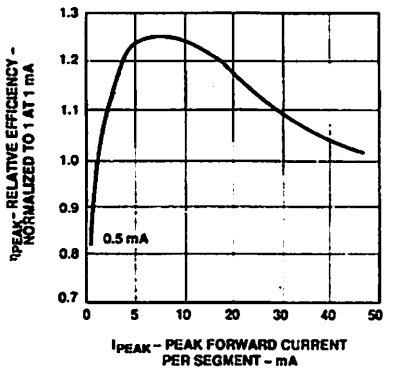


Figure 4. Relative Efficiency (Luminous Intensity per Unit Current) vs. Peak Current.

HEWLETT® PACKARD

HER, Yellow, Green

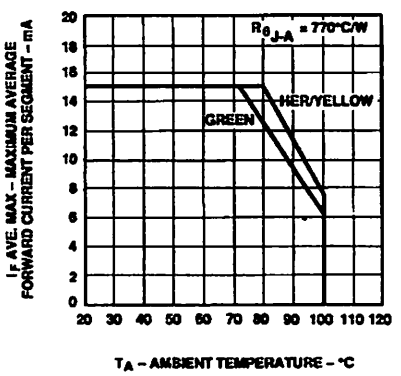


Figure 5. Maximum Allowable Average or DC Current vs. Ambient Temperature.

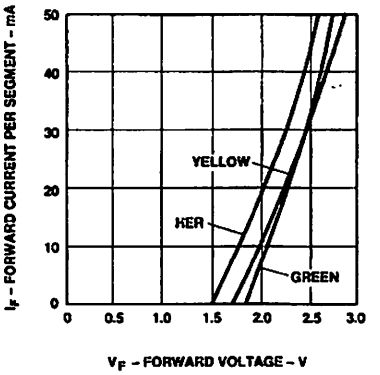


Figure 6. Forward Current vs. Forward Voltage.

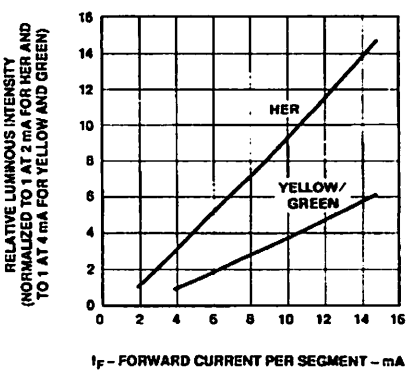


Figure 7. Relative Luminous Intensity vs. DC Forward Current.

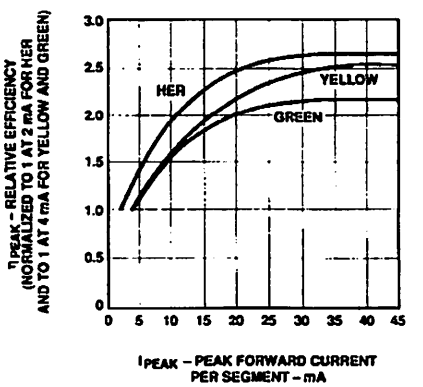


Figure 8. Relative Efficiency (Luminous Intensity per Unit Current) vs. Peak Current.

Electrical/Optical

For more information on electrical/optical characteristics, please see Application Note 1005.

Contrast Enhancement

For information on contrast enhancement please see Application Note 1015.

Soldering/Cleaning

Cleaning agents from the ketone family (acetone, methyl ethyl ketone, etc.) and from the chorinated hydrocarbon family (methylene chloride, trichloroethylene, carbon tetrachloride, etc.) are not recommended for cleaning LED parts. All of these various solvents attack or dissolve the encapsulating epoxies used to form the package of plastic LED parts.

For information on soldering LEDs please refer to Application Note 1027.

www.hp.com/go/led_displays

For technical assistance or the location of your nearest Hewlett-Packard sales office, distributor or representative call:

Americas/Canada: 1-800-235-0312 or 408-654-8675

Far East/Australasia: Call your local HP sales office.

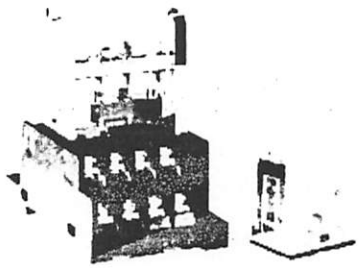
Japan: (81 3) 3335-8152

Europe: Call your local HP sales office.

Data subject to change.

Printed in U.S.A. 5091-8365E (1/98)

rc barrier equipped.
igh dielectric strength (2,000 VAC).
ong dependable service life assured by AgCdO contacts.
hoose models with single or bifurcated contacts, ED indicator, diode surge suppression, ush-to-test button, or RC circuit.
ll models meet UL and CSA pprovals; VDE, LR, and SEV pproved versions are available.



rdering Information

Order: Select the part number and add the desired coil voltage rating (e.g., LY1-*DC6*).

Type	Terminal	Contact form	Model					
			Single contact			Bifurcated contact		
			Standard bracket mounting	Upper mounting bracket	Lower mounting bracket	Standard bracket mounting	Upper mounting bracket	Lower mounting bracket
ındard	Plug-in/solder	SPDT	**LY1**	**LY1F**	**LY1S**	—	—	—
		DPDT	**LY2**	**LY2F**	**LY2S**	**LY2Z**	**LY2ZF**	**LY2ZS**
		3PDT	**LY3**	**LY3F**	**LY3S**	—	—	—
		4PDT	**LY4**	**LY4F**	**LY4S**	—	—	—
	PCB	SPDT	**LY1-0**	—	—	—	—	—
		DPDT	**LY2-0**	—	—	**LY2Z-0**	—	—
		3PDT	**LY3-0**	—	—	—	—	—
		4PDT	**LY4-0**	—	—	—	—	—
D indicator	Plug-in/solder	SPDT	**LY1N**	—	—	—	—	—
		DPDT	**LY2N**	—	—	**LY2ZN**	—	—
		3PDT	**LY3N**	—	—	—	—	—
		4PDT	**LY4N**	—	—	—	—	—
ode surge ppression		SPDT	**LY1-D**	—	—	—	—	—
		DPDT	**LY2-D**	—	—	**LY2Z-D**	—	—
		3PDT	**LY3-D**	—	—	—	—	—
		4PDT	**LY4-D**	—	—	—	—	—
D indicator d diode surge ppression		SPDT	**LY1N-D2**	—	—	—	—	—
		DPDT	**LY2N-D2**	—	—	**LY2ZN-D2**	—	—
		4PDT	**LY4N-D2**	—	—	—	—	—
C circuit		SPDT	**LY1-CR**	—	—	—	—	—
		DPDT	**LY2-CR**	—	—	**LY2Z-CR**	—	—
D indicator d RC circuit		SPDT	**LY1N-CR**	—	—	—	—	—
		DPDT	**LY2N-CR**	—	—	**LY2ZN-CR**	—	—

te: 1. Types with specifications other than those listed are available. Contact your Omron Sales representative.
2. To order connecting sockets and mounting tracks, see "Accessories" section.

Type	Terminal	Contact form	Model					
			Single contact			Bifurcated contact		
			Standard bracket mounting	Upper mounting bracket	Lower mounting bracket	Standard bracket mounting	Upper mounting bracket	Lower mounting bracket
Push-to-test button	Plug-in/solder	SPDT	LY1I4	—	—	—	—	—
		DPDT	LY2I4	—	—	LY2ZI2	—	—
		3PDT	LY3I4	—	—	—	—	—
		4PDT	LY4I4	—	—	—	—	—
LED indicator and push-to-test button	Plug-in/solder	DPDT	LY2I4N	—	—	LY2ZI2N	—	—
		4PDT	LY4I4N	—	—	—	—	—

Note: 1. Types with specifications other than those listed are available. Contact your Omron Sales representative.
2. To order connecting sockets and mounting tracks, see "Accessories" section.

■ Accessories

Connecting Sockets

To Order: Select the appropriate part numbers for sockets, clips, and mounting tracks (if required) from the following charts.

Track Mounted Sockets

Relay	Socket*	Relay hold-down clip		Mounting track
		Standard	RC circuit	
SPDT DPDT	PTF08A-E	PYC-A1	Y92H-3	PFP-100N/PFP-50N & PFP-M or PFP-100N2 PFP-S (Option spacer)
3PDT	PTF11A			
4PDT	PTF14A-E			

* Track mounted socket can be used as a front connecting socket.

Back Connecting Sockets

Relay	Solder terminal socket	Wire wrap terminal socket	Relay hold-down clip				Socket Mounting Plate			
			Standard	Push-to-test	RC circuit	Mtg. plate	1	10	12	18
SPDT DPDT	PT08	PT08QN	PYC-P	PYC-P2	PYC-1	PYC-S	PYP-1	–	–	PYP-18
3PDT	PT11	PT11QN					PTP-1-3	–	PTP-12	–
4PDT	PT14	PT14QN					PTP-1	PTP-10	–	–

Note: Types PYP-18, PTP-12 and PTP-10 may be cut to any desired length.

Relay	PC terminal socket	Relay hold-down clip		
		Standard	Push-to-test	RC circuit
SPDT DPDT	PT08-0	PYC-P	PYC-P2	PYC-1
3PDT	PT11-0			
4PDT	PT14-0			

Specifications

Contact Data

Load	Single contact				Bifurcated contact	
	SPDT		DPDT, 3PDT, 4PDT		DPDT	
	Resistive load (p.f. = 1)	Inductive load (p.f. = 0.4) (L/R = 7 ms)	Resistive load (p.f. = 1)	Inductive load (p.f. = 0.4) (L/R = 7 ms)	Resistive load (p.f. = 1)	Inductive load (p.f. = 0.4) (L/R = 7 ms)
ated load	15 A at 110 VAC 15 A at 24 VDC	10 A at 110 VAC 7 A at 24 VDC	10 A at 110 VAC 10 A at 24 VDC	7.5 A at 110 VAC 5 A at 24 VDC	5 A at 110 VAC 5 A at 24 VDC	4 A at 110 VAC 4 A at 24 VDC
ontact material	AgCdO					
arry current	15 A		10 A		7 A	
lax. operating oltage	250 VAC 125 VDC					
lax. operating urrent	15 A		10 A		7 A	
lax. switching apacity	1,700 VA 360 W	1,100 VA 170 W	1,100 VA 240 W	830 VA 120 W	550 VA 120 W	440 VA 100 W
lin. permissible oad	100 mA, 5 VDC				10 mA, 5 VDC	

Coil Data

- and 2-pole Types – AC

Rated voltage (V)	Rated current (mA)		Coil resistance (Ω)	Coil inductance (ref. value) (H)		Pick-up voltage	Dropout voltage	Maximum voltage	Power consumption (VA, W)
	50 Hz	60 Hz		Armature OFF	Armature ON	(% of rated voltage)			
	214.10	183	12.20	0.04	0.08	80% max.	30% min.	110%	Approx. 1.00 to 1.20 (60 Hz)
2	106.50	91	46	0.17	0.33				
4	53.80	46	180	0.69	1.30				
0	25.70	22	788	3.22	5.66				
00/110	11.70/12.90	10/11	3,750	14.54	24.60				Approx. 0.90 to 1.10 (60 Hz)
10/120	9.90/10.80	8.40/9.20	4,430	19.20	32.10				
00/220	6.20/6.80	5.30/5.80	12,950	54.75	94.07				
20/240	4.80/5.30	4.20/4.60	18,790	83.50	136.40				

- and 2-pole Types – DC

Rated voltage (V)	Rated current (mA)	Coil resistance (Ω)	Coil inductance (ref. value) (H)		Pick-up voltage	Dropout voltage	Maximum voltage	Power consumption (VA, W)
			Armature OFF	Armature ON	(% of rated voltage)			
	150	40	0.16	0.33	80% max.	10% min.	110%	Approx. 0.90
2	75	160	0.73	1.37				
4	36.90	650	3.20	5.72				
8	18.50	2,600	10.60	21				
00/110	9.10/10	11,000	45.60	86.20				

ote: 1. The rated current and coil resistance are measured at a coil temperature of 23°C (73°F) with tolerances of +15%, -20% for AC rated current, and ±15% for DC rated coil resistance.
2. The AC coil resistance and inductance are reference values at 60 Hz.
3. The performance characteristics are measured at a coil temperature of 23°C (73°F).
4. Class B coil insulation is available.

3-pole Type – AC

Rated voltage (V)	Rated current (mA)		Coil resistance (Ω)	Coil inductance (ref. value) (H)		Pick-up voltage	Dropout voltage	Maximum voltage	Power consumption (VA, W)
	50 Hz	60 Hz		Armature OFF	Armature ON	(% of rated voltage)			
6	310	270	6.70	0.03	0.05	80% max.	30% min.	110%	Approx. 1.60 to 2.00 (60 Hz)
12	159	134	24	0.12	0.21				
24	80	67	100	0.44	0.79				
50	38	33	410	2.24	3.87				
100/110	15.90/18.30	13.60/15.60	2,300	10.50	18.50				
120	17.30	14.8	2,450	11.50	20.60				
200/220	10.50/11.60	9.00/9.90	8,650	34.80	59.50				
240	9.40	8	10,400	38.60	74.60				

3-pole Type – DC

Rated voltage (V)	Rated current (mA)	Coil resistance (Ω)	Coil inductance (ref. value) (H)		Pick-up voltage	Dropout voltage	Maximum voltage	Power consumption (VA, W)
			Armature OFF	Armature ON	(% of rated voltage)			
6	234	25.70	0.11	0.21	80% max.	10% min.	110%	Approx. 1.40
12	112	107	0.45	0.98				
24	58.60	410	1.89	3.87				
48	28.20	1,700	8.53	13.90				
100/110	12.70/13	8,500	29.60	54.30				

4-pole Type – AC

Rated voltage (V)	Rated current (mA)		Coil resistance (Ω)	Coil inductance (ref. value) (H)		Pick-up voltage	Dropout voltage	Maximum voltage	Power consumption (VA, W)
	50 Hz	60 Hz		Armature OFF	Armature ON	(% of rated voltage)			
6	386	330	5	0.02	0.04	80% max.	30% min.	110%	Approx. 1.95 to 2.50 (60 Hz)
12	199	170	20	0.10	0.17				
24	93.60	80	78	0.38	0.67				
50	46.80	40	350	1.74	2.88				
100/110	22.50/25.50	19/21.80	1,800	10.50	17.30				
120	19.00	16.40	2,200	9.30	19				
200/220	11.50/13.10	9.80/11.20	6,700	33.10	57.90				
240	11.00	9.50	9,000	33.20	63.40				

4-pole Type – DC

Rated voltage (V)	Rated current (mA)	Coil resistance (Ω)	Coil inductance (ref. value) (H)		Pick-up voltage	Dropout voltage	Maximum voltage	Power consumption (VA, W)
			Armature OFF	Armature ON	(% of rated voltage)			
6	240	25	0.09	0.21	80% max.	10% min.	110%	Approx. 1.50
12	120	100	0.39	0.84				
24	69	350	1.41	2.91				
48	30	1,600	6.39	13.60				
100/110	15/15.90	6,900	32	63.70				

Note: 1. The rated current and coil resistance are measured at a coil temperature of 23°C (73°F) with tolerances of +15%, -20% for AC rated current, and ±15% for DC rated coil resistance.

2. The AC coil resistance and inductance are reference values at 60 Hz.
3. The performance characteristics are measured at a coil temperature of 23°C (73°F).
4. Class B coil insulation is available.

Characteristics

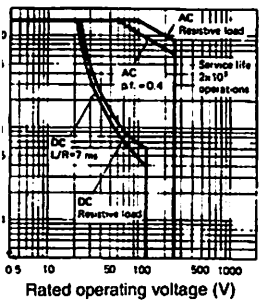
tact resistance		50 mΩ max.
rate time		25 ms max.
ase time		25 ms max.
rating frequency	Mechanically	18,000 operations/hour
	Under rated load	1,800 operations/hour
ulation resistance		100 MΩ min. (at 500 VDC)
ectric strength		2,000 VAC, 50/60 Hz for 1 minute 1,000 VAC, 50/60 Hz for 1 minute between contacts of same polarity
ation	Mechanical durability	10 to 55 Hz, 1.00 mm (0.04 in) double amplitude
	Malfunction durability	10 to 55 Hz, 1.00 mm (0.04 in) double amplitude
ck	Mechanical durability	1,000 m/s² (approx. 100 G)
	Malfunction durability	200 m/s² (approx. 20 G)
bient temperature	Operating	-40° to 70°C (-40° to 158°F)
midity		35 to 85% RH
vice Life	Mechanically	AC: 50 million operations min. (at operating frequency of 18,000 operations/hour) DC: 100 million operations min. (at operating frequency of 18,000 operations/hour)
	Electrically	See "Characteristic Data"
ght		SPDT, DPDT: Approx. 40 g (1.41 oz), 3PDT: Approx. 50 g (1.76 oz) 4PDT: Approx. 70 g (2.47 oz)

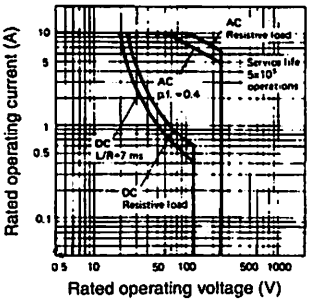
e: Data shown are of initial value.

Characteristic Data

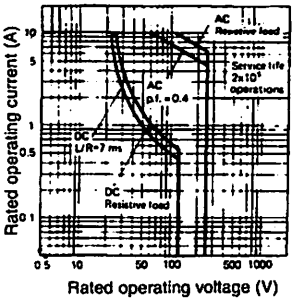
timum switching capacity

LY2

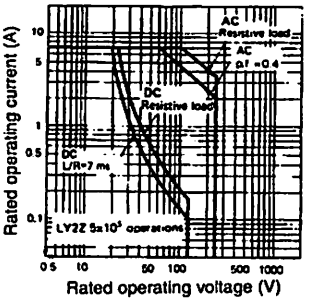




LY3, LY4

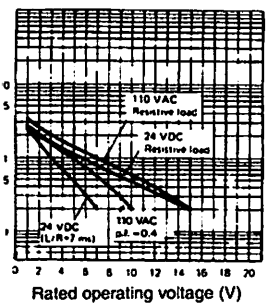


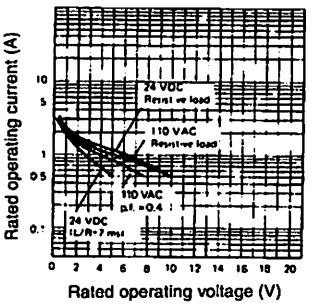
LY2Z



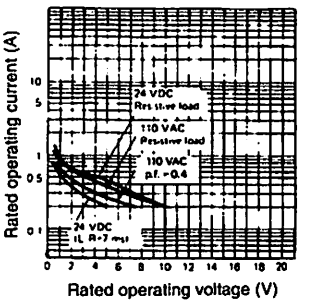
ctrical service life

LY2





LY3, LY4



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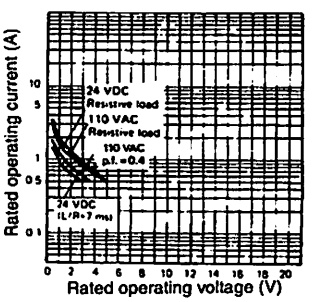
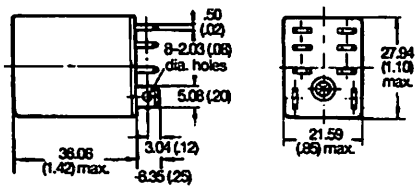


Dimensions

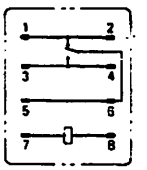
Unit: mm (inch)

■ Relays

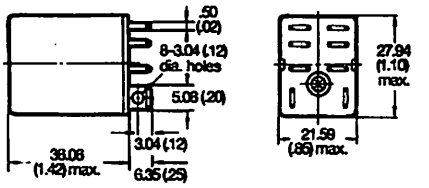
LY1



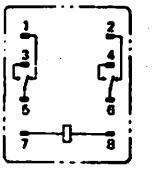
Terminal arrangement (Bottom view)



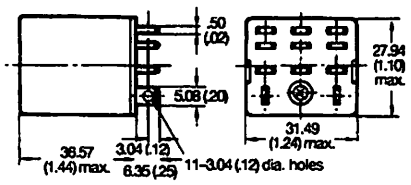
LY2



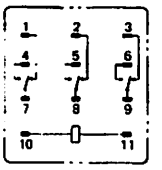
Terminal arrangement (Bottom view)



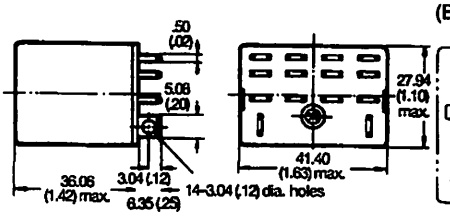
LY3



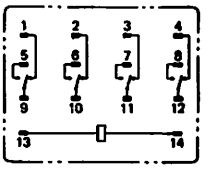
Terminal arrangement (Bottom view)



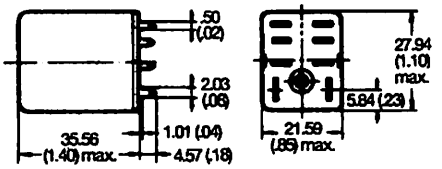
LY4



Terminal arrangement (Bottom view)

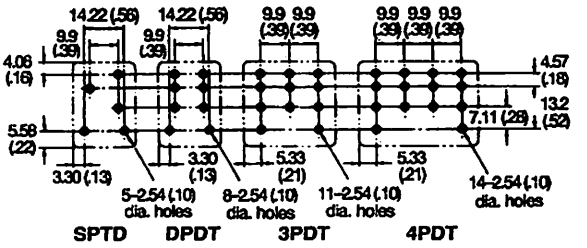


LY1-0, LY2-0, LY3-0, LY4-0

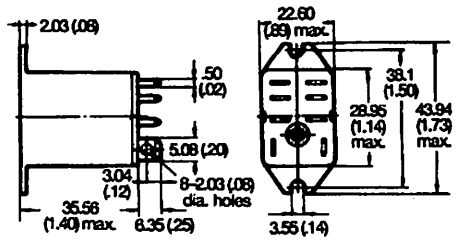


Note: The above drawing shows LY2-0. With LY1-0, dimension "" should read as eight 6.35 (.25).

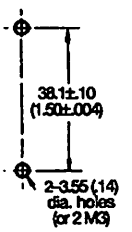
Mounting holes for LY1-0, LY2-0, LY3-0, LY4-0
(Bottom view)



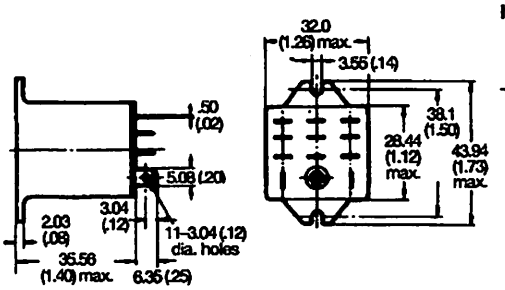
LY1F, LY2F



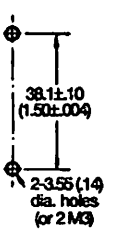
Mounting holes



LY3F

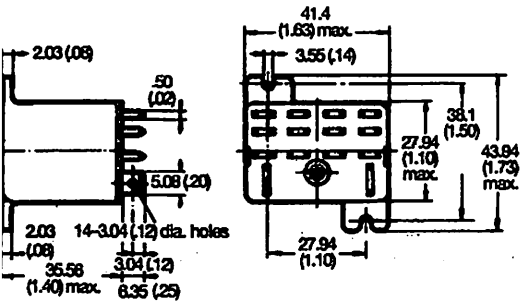


Mounting holes

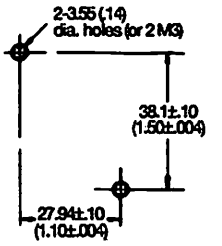


Note: The above drawing shows LY1F. With LY2F, dimension "" should read as eight 3.05 mm (0.12 in) dia. holes.

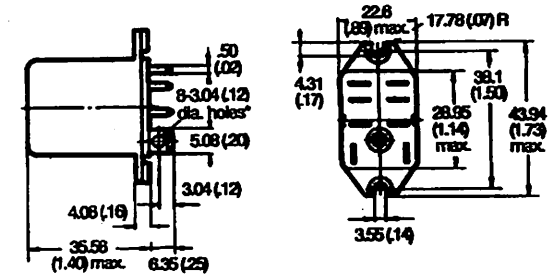
'4F



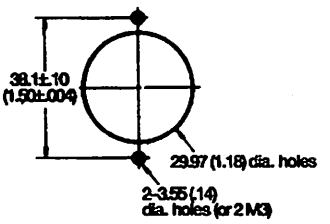
Mounting holes



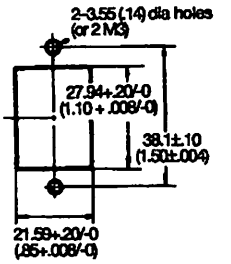
'1S, LY2S



Round hole

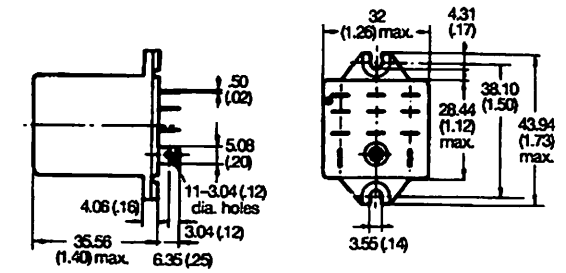


Rectangular hole

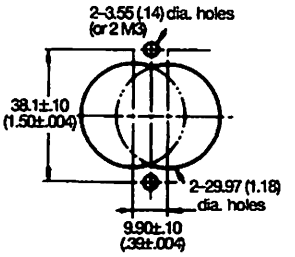


ote: The above drawing shows LY2S-US. With LY1S-US, dimension "*" should read as eight 2.03 mm (0.08 in) dia. holes.

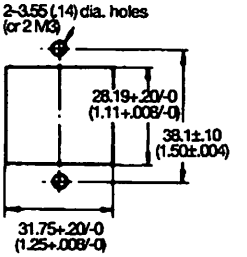
'3S



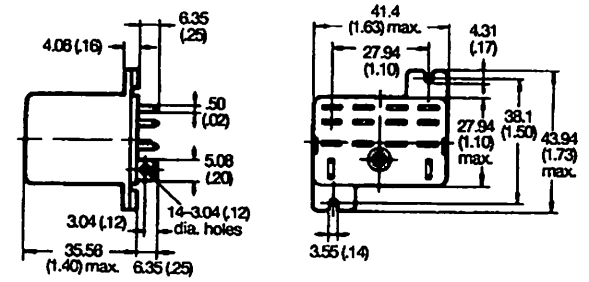
Round hole



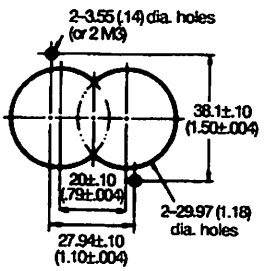
Rectangular hole



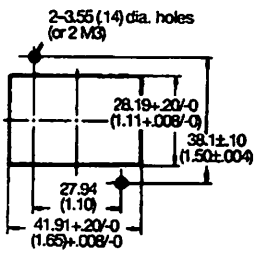
'4S



Round hole



Rectangular hole



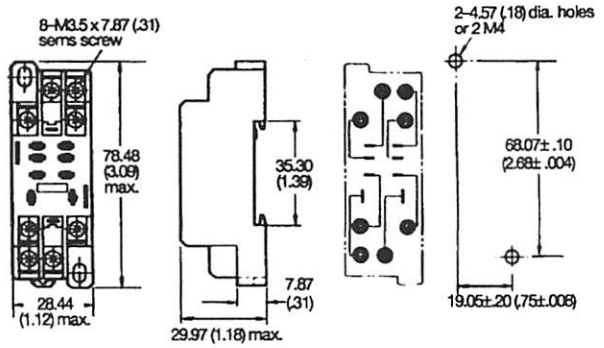
■ Accessories

Unit: mm (inch)

Track mounted sockets (UL File No. E87929) (CSA Report No. LR31928)

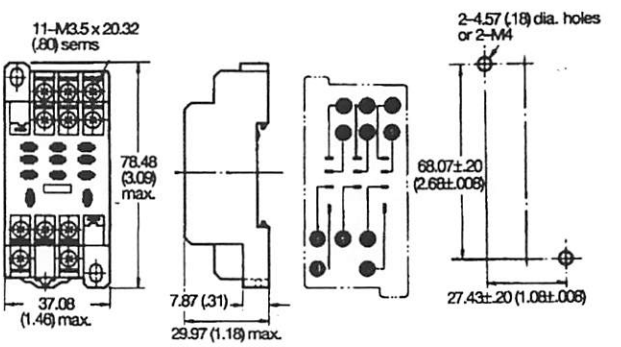
PTF08A-E

Terminal arrangement/ mounting holes
(Top view)



PTF11A

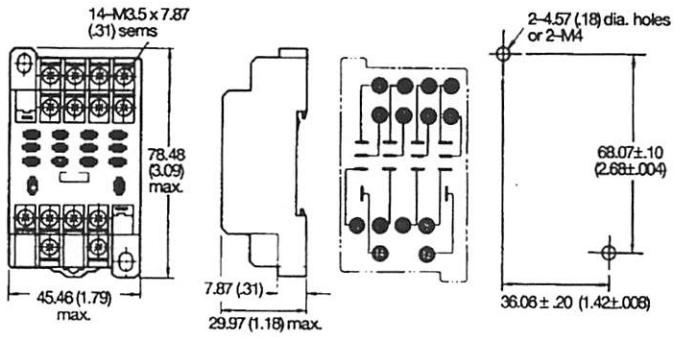
Terminal arrangement/ mounting holes
(Top view)



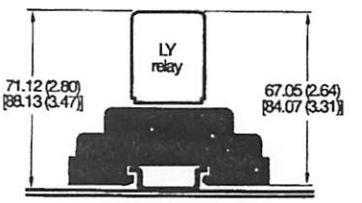
Track mounting sockets (UL File No. E87929) (CSA Report No. LR31928)

PTF14A-E

Terminal arrangement/ mounting holes
(Top view)



Mounting height of relay with socket
(Applies to all PTF□A sockets)

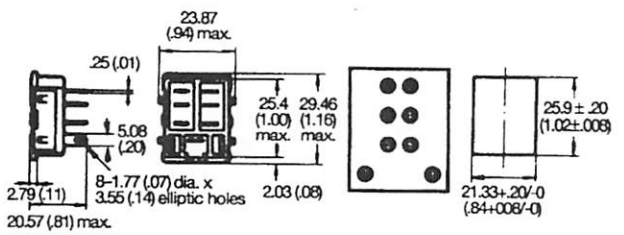


Note: 1. UL/CSA does not apply to wire wrap (Q) type sockets.
2. Values in brackets for LY□CR.

Back connecting socket (UL File No. E87929) (CSA Report No. LR31928)

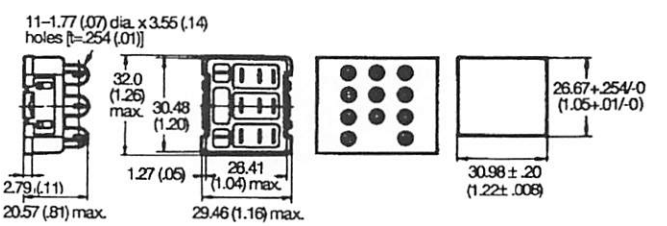
PT08

Terminal arrangement/
(Bottom view)



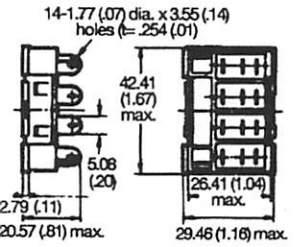
PT11

Terminal arrangement/
(Bottom view)

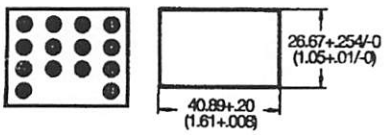


ck connecting socket (UL File No. E87929) (CSA Report No. LR31928)

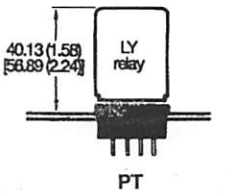
14



Terminal arrangement
(Bottom view)



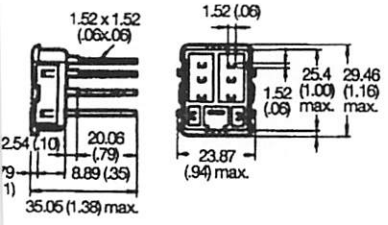
Mounting height of relay with socket
(Applies to all PT sockets)



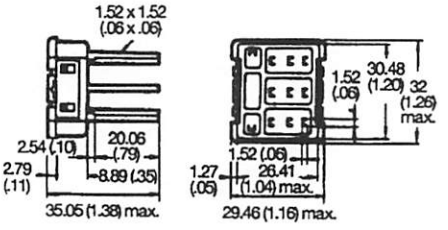
te: Values in brackets for LY□CR.

ck connecting socket (UL File No. E87929) (CSA Report No. LR31928)

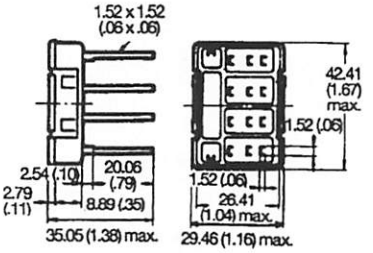
08QN
nel cut-out and terminal
angement are the same
Type PT08.



PT11QN
Panel cut-out and terminal arrangement are the same as Type PT11.

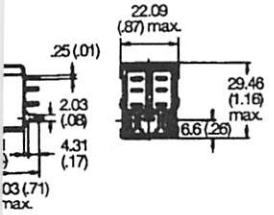


PT14QN
Panel cut-out and terminal arrangement are the same as Type PT14.

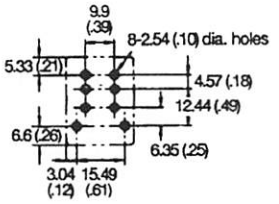


ck connecting socket (UL File No. E87929) (CSA Report No. LR31928)

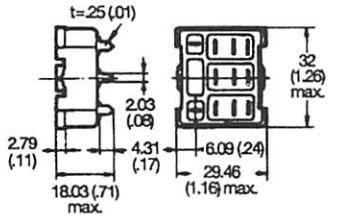
8-0
ninal arrangement is
same as Type PT08.



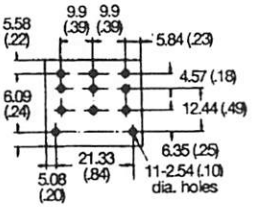
Mounting holes
(Bottom view)



PT11A
Terminal arrangement is the same as Type PT11.

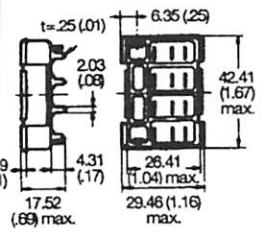


Mounting holes
(Bottom view)

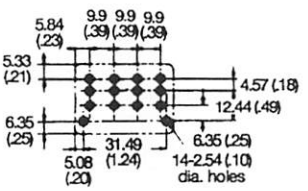


ck connecting socket (UL File No. E87929) (CSA Report No. LR31928)

14-0
minal arrangement is
same as Type PT14.



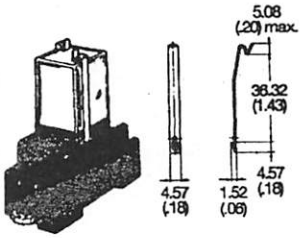
Mounting holes
(Bottom view)



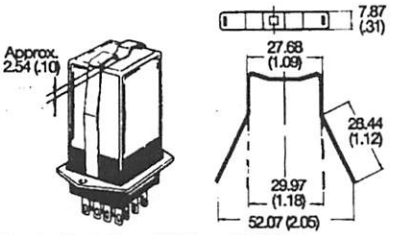
Unit: mm (inch)

Relay hold-down clips

PYC-A1
For PTF□A socket

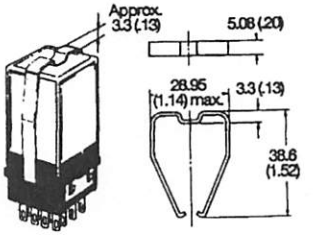


PYC-S
For relay mounting plates
(Applicable to Type PYP-1 and PYP-18 socket mounting plates only.)



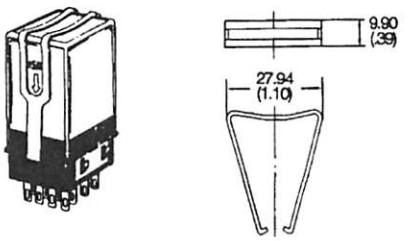
(Applicable to Type PYP-1 and PYP-18 socket mounting plates only.)

PYC-P
For PT□ socket

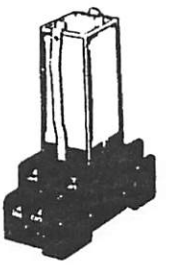


Relay hold-down clips

PYC-P2
For push-to-test button type with PT□ socket



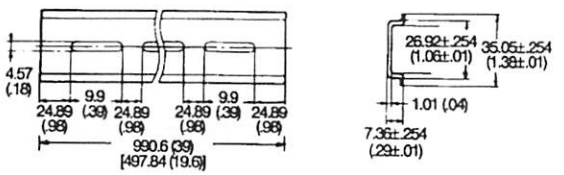
Y92H-3
For RC circuit type



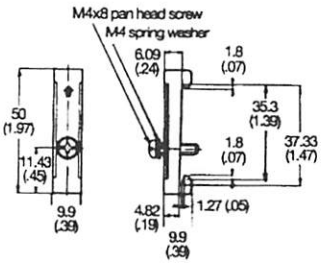
PYC-1
For RC circuit type

Mounting track/end plate/spacer

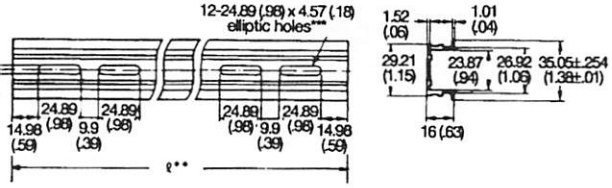
PFP-100N/PFP-50N mounting track



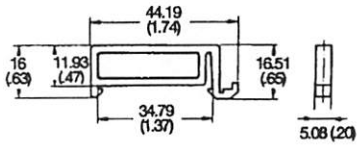
PFP-M end plate



-100N2 mounting track



PFP-S spacer

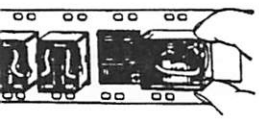


* This dimension is 14.99 mm (0.59 in) on both ends in the case of PFP-100N, but on one end in the case of PFP-50N.

** L = Length
PFP-50N ..... L = 497.84 mm (19.60 in)
PFP-100N ..... L = 990.60 mm (39.00 in)
PFP-100N2 ..... L = 990.60 mm (39.00 in)

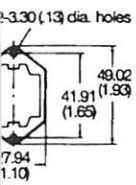
*** A total of twelve 24.89 x 4.57 mm (0.98 x 0.18 in) elliptic holes are provided, with six holes cut from each end of the track at a pitch of 9.91 (0.39) between holes.

ket mounting plates [t=1.52 (.06)]

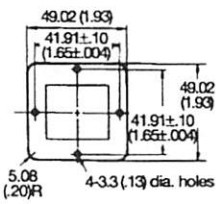


	Number of socket specs.			
Socket needed	1	10	12	18
PT08, PT08QN	PYP-1	–	–	PYP-18
PT11, PT11QN	PTP-1-3	–	PTP-1-2	–
PT14, PT14QN	PTP-1	PTP-10	–	–
PTP-10	PTP-12			

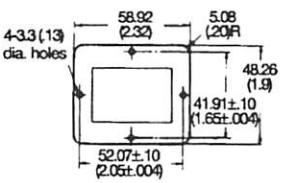
P-1



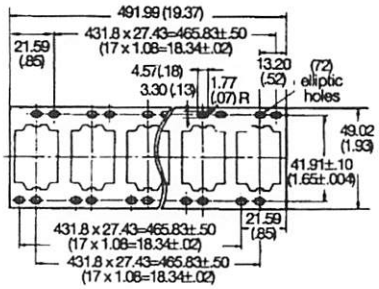
PTP-1-3



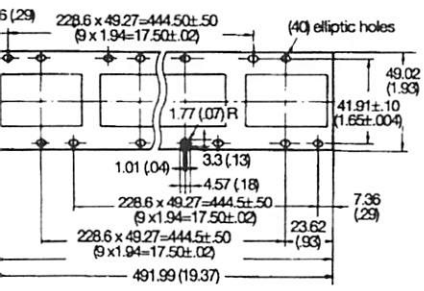
PTP-1



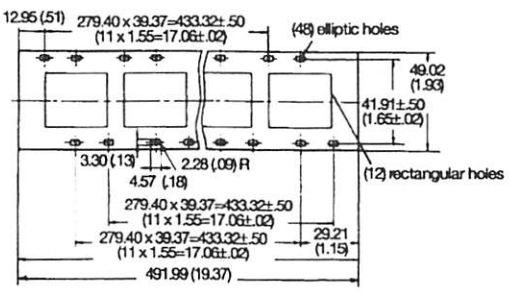
PYP-18



P-10



PTP-12



■ Relay Options

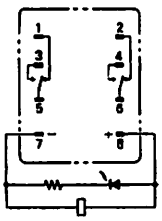
LED Indicator

Specifications and dimensions same as the Standard Type with the following exception. With the LED indicator type, the rated current is approximately 0 to 5.0 mA higher than the Standard Type.

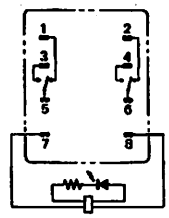
Terminal arrangement/Internal connections (Bottom view)

LY2N

DC coil rating type



AC coil rating type

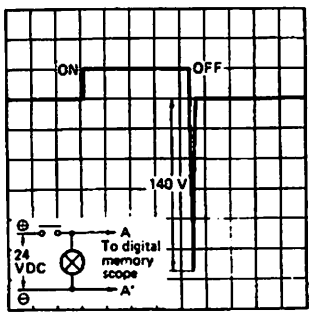


Note: 1. The coil terminals 10 and 11 of Type LY3N become (-) and (+) and terminals 13 and 14 of Type LY4N become (-) and (+), respectively.
2. Pay special attention to the polarities when using the DC type.

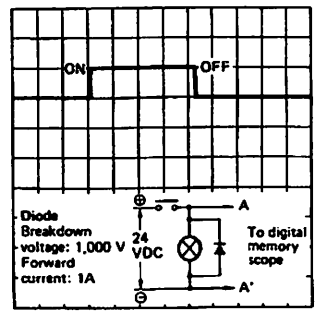
Diode Surge Suppression

Specifications and dimensions same as the Standard Type with the following exception. Ambient operating temperature: -25° to 40°C (-13° to 104°F)

Without Diode



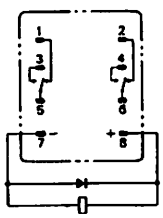
With Diode



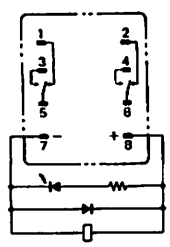
Terminal arrangement/Internal connections (Bottom view)

LY2(N)-D(2)

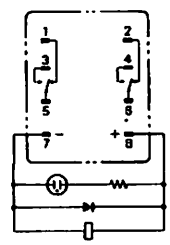
LY2-D
6, 12, 24, 48
100/110 VDC



LY2N-D2
6, 12, 24, 48 VDC



LY2N-D2
100/110 VDC



Note: 1. Pay special attention to the polarities when using the DC type.
2. The release time is somewhat longer, but satisfies the standard specifications of 25 ms.
3. The reverse-breakdown voltage of the diode is 1,000 VDC.
4. Available on DC versions only.

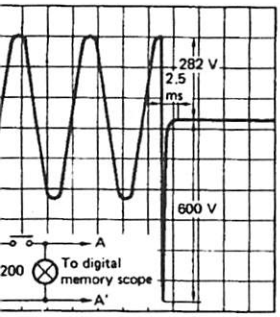
Relay Options

Circuit

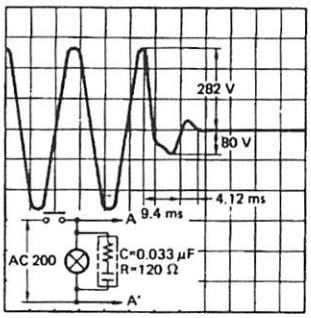
ifications and dimensions same as the Standard Type with the following exceptions.

racteristic Data

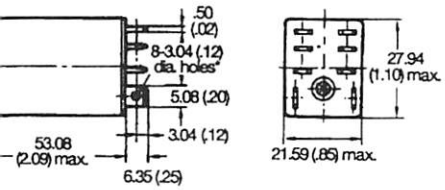
out RC circuit



With RC circuit

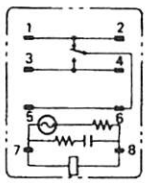


-CR, LY2(Z)-CR

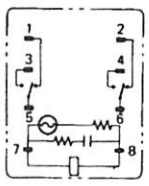


Terminal arrangement/Internal connections (Bottom view)

LY1-CR



LY2(Z)-CR



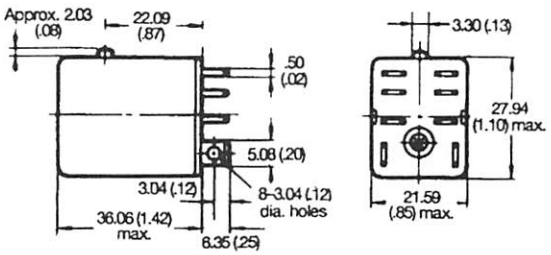
e: 1. The above drawing shows LY2(Z)-CR. With LY1-CR, "*" should read eight 2.03 mm (0.08 in) dia. holes.
2. Available on AC versions only.

sh-to-test Button

cifications and dimensions same as the Standard Type with the following exceptions.

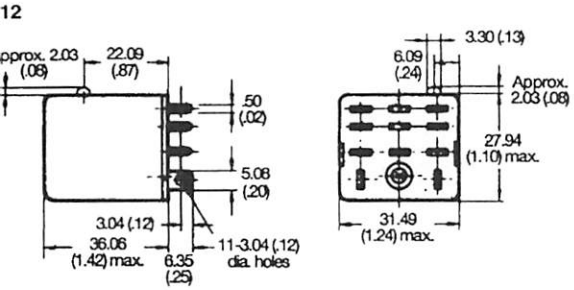
112

LY112, LY212

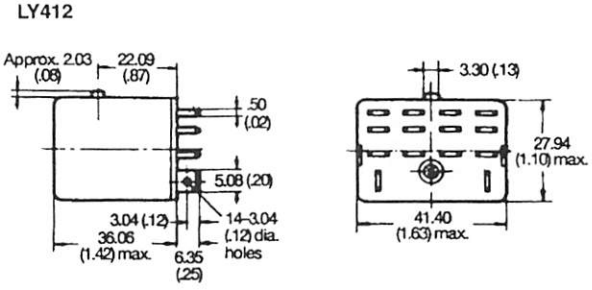


e: Type LY112 has the same dimensions and appearances as Type LY212 shown except that dimensions "*" is 2.03 mm (0.08 in) dia. holes.

112



LY412



■ Approvals

UL Recognized Type (File No. E41643)

Type	Contact form	Coil ratings	Contact ratings
LY□	SPDT	6 to 240 VAC 6 to 120 VDC	15 A, 240 VAC (Inductive)
			15 A, 28 VDC (Resistive)
			TV-5 (ACTV)
			1/2 HP, 120 VAC (Motor)
LY□	DPDT		13 A, 120 VAC (Resistive)
			12 A, 240 VAC (Inductive)
			10 A, 28 VDC (Resistive)
			TV-3 (ACTV)
			1/2 HP, 120 VAC (Motor)
LY□	3PDT 4PDT		10 A, 240 VAC (Inductive)
			10 A, 28 VDC (Resistive)
			1/2 HP, 240 VAC (Motor)

CSA Certified Type (File No. LR31928)

Type	Contact form	Coil ratings	Contact ratings
LY□	SPDT	6 to 240 VAC 6 to 120 VDC	15 A, 120 VAC (Inductive)
			10 A, 240 VAC (Inductive)
			15 A, 28 VDC (Resistive)
			TV-5 (ACTV)
LY□	DPDT		13 A, 28 VDC (Resistive)
			12 A, 120 VAC (Inductive)
			10 A, 240 VAC (Inductive)
			1/3 HP, 120 VAC (Motor)
			TV-3 (ACTV)
LY□	3PDT 4PDT		10 A, 240 VAC (Inductive)
			10 A, 28 VDC (Resistive)

VDE Approved Type (File No. 9903 [SPDT, DPDT & 3PDT], File No. 9947 [4PDT])

Type	Contact form	Coil ratings	Contact ratings
LY□-VD	SPDT	6, 12, 24, 50, 110, 220 VAC and 6, 12, 24, 48, 110 VDC	10 A, 220 VAC (Resistive)
			10 A, 28 VDC (Resistive)
			7 A, 220 VAC (Inductive)
			7 A, 28 VDC (Inductive)
LY□-VD	DPDT 3PDT 4PDT		7 A, 220 VAC (Resistive)
			7 A, 28 VDC (Resistive)
			4 A, 220 VAC (Inductive)
			4 A, 28 VDC (Inductive)

LR (Lloyd's Register) Approved Type (File No. 562KOB-204523)

Type	Contact form	Coil ratings	Contact ratings
LY□	DPDT	6 to 240 VAC	7.5 A, 230 VAC (Inductive)
	4PDT	6 to 110 VDC	5 A, 24 VDC (Inductive)

SEV Listed Type (File No. D7 91/82 [2- & 4-pole], D 91/204a [1- & 3-pole])

Type	Contact form	Coil ratings	Contact ratings
LY□-SV	SPDT	6 to 240 VAC 6 to 110 VDC	15 A, 220 VAC (Resistive)
			15 A, 24 VDC (Resistive)
LY□-SV	DPDT 3PDT 4PDT		10 A, 220 VAC (Resistive)
			10 A, 24 VDC (Resistive)

Note: 1. The rated values approved by each of the safety standards (e.g., UL, CSA, VDE, and SEV) may be different from the performance characteristics individually defined in this catalog.

2. In the interest of product improvement, specifications are subject to change.

OMRON

ALL DIMENSIONS SHOWN ARE IN MILLIMETERS. To convert millimeters into inches, divide by 25.4

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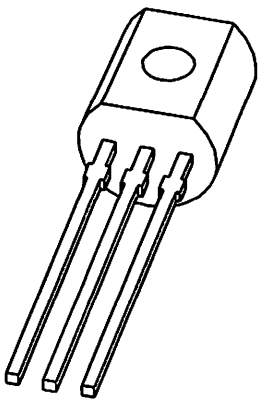
Cat. No. GC RLY8 5/03 Specifications subject to change without notice Printed in USA

DATA SHEET



BC546; BC547; BC548
NPN general purpose transistors

Product specification
Supersedes data of September 1994
File under Discrete Semiconductors, SC04

1997 Mar 04

Philips
Semiconductors

PHILIPS

NPN general purpose transistors — BC546; BC547; BC548

FEATURES

- Low current (max. 100 mA)
- Low voltage (max. 65 V).

APPLICATIONS

- General purpose switching and amplification.

DESCRIPTION

NPN transistor in a TO-92; SOT54 plastic package.
PNP complements: BC556, BC557 and BC558.

PINNING

PIN	DESCRIPTION
1	emitter
2	base
3	collector

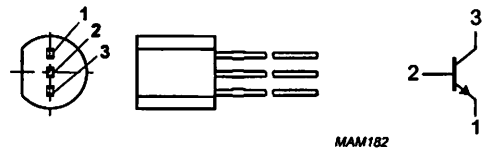


Fig.1 Simplified outline (TO-92; SOT54) and symbol.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{CBO}	collector-base voltage	open emitter			
	BC546		–	80	V
	BC547		–	50	V
	BC548		–	30	V
V_{CEO}	collector-emitter voltage	open base			
	BC546		–	65	V
	BC547		–	45	V
	BC548		–	30	V
I_{CM}	peak collector current		–	200	mA
P_{tot}	total power dissipation	$T_{amb} \leq 25$ °C	–	500	mW
h_{FE}	DC current gain	$I_C = 2$ mA; $V_{CE} = 5$ V			
	BC546		110	450	
	BC547		110	800	
	BC548		110	800	
f_T	transition frequency	$I_C = 10$ mA; $V_{CE} = 5$ V; f = 100 MHz	100	–	MHz

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{CBO}	collector-base voltage	open emitter			
	BC546		–	80	V
	BC547		–	50	V
	BC548		–	30	V
V_{CEO}	collector-emitter voltage	open base			
	BC546		–	65	V
	BC547		–	45	V
	BC548		–	30	V
V_{EBO}	emitter-base voltage	open collector			
	BC546		–	6	V
	BC547		–	6	V
	BC548		–	5	V
I_C	collector current (DC)		–	100	mA
I_{CM}	peak collector current		–	200	mA
I_{BM}	peak base current		–	200	mA
P_{tot}	total power dissipation	$T_{amb} \leq 25$ °C; note 1	–	500	mW
T_{stg}	storage temperature		–65	+150	°C
T_j	junction temperature		–	150	°C
T_{amb}	operating ambient temperature		–65	+150	°C

Note

1. Transistor mounted on an FR4 printed-circuit board.

THERMAL CHARACTERISTICS

SYMBOL	PARAMETER	CONDITIONS	VALUE	UNIT
$R_{th\ j\text{-}a}$	thermal resistance from junction to ambient	note 1	0.25	K/mW

Note

1. Transistor mounted on an FR4 printed-circuit board.

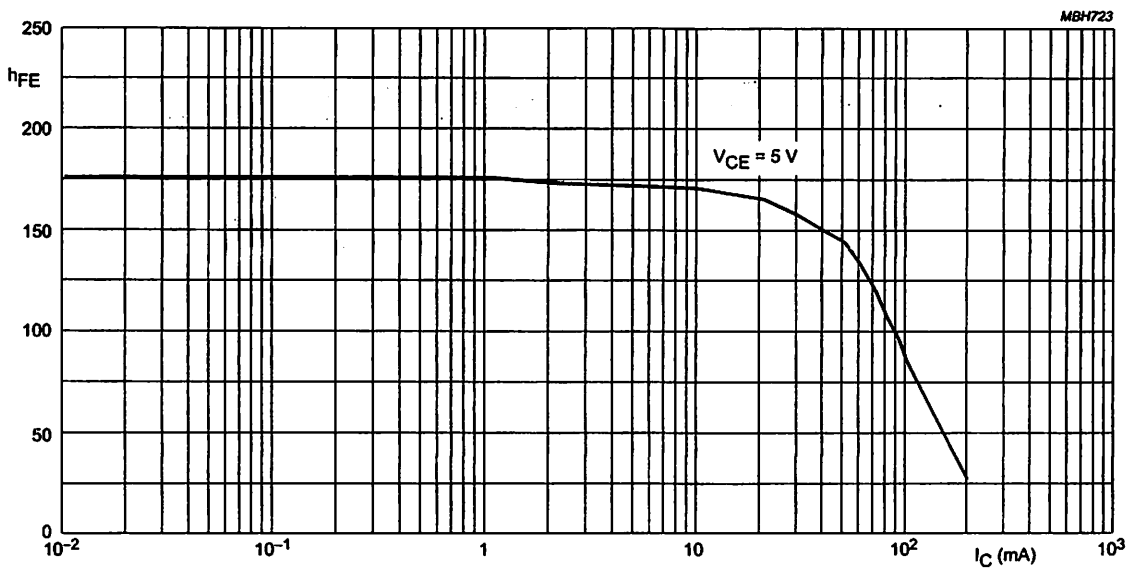
CHARACTERISTICS

T_j = 25 °C unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
I_{CBO}	collector cut-off current	I_E = 0; V_{CB} = 30 V	–	–	15	nA
		I_E = 0; V_{CB} = 30 V; T_j = 150 °C	–	–	5	µA
I_{EBO}	emitter cut-off current	I_C = 0; V_{EB} = 5 V	–	–	100	nA
h_{FE}	DC current gain	I_C = 10 µA; V_{CE} = 5 V; see Figs 2, 3 and 4				
	BC546A; BC547A; BC548A		–	90	–	
	BC546B; BC547B; BC548B		–	150	–	
	BC547C; BC548C		–	270	–	
h_{FE}	DC current gain	I_C = 2 mA; V_{CE} = 5 V; see Figs 2, 3 and 4				
	BC546A; BC547A; BC548A		110	180	220	
	BC546B; BC547B; BC548B		200	290	450	
	BC547C; BC548C		420	520	800	
	BC547; BC548		110	–	800	
	BC546		110	–	450	
V_{CEsat}	collector-emitter saturation voltage	I_C = 10 mA; I_B = 0.5 mA	–	90	250	mV
		I_C = 100 mA; I_B = 5 mA	–	200	600	mV
V_{BEsat}	base-emitter saturation voltage	I_C = 10 mA; I_B = 0.5 mA; note 1	–	700	–	mV
		I_C = 100 mA; I_B = 5 mA; note 1	–	900	–	mV
V_{BE}	base-emitter voltage	I_C = 2 mA; V_{CE} = 5 V; note 2	580	660	700	mV
		I_C = 10 mA; V_{CE} = 5 V	–	–	770	mV
C_c	collector capacitance	$I_E = i_e$ = 0; V_{CB} = 10 V; f = 1 MHz	–	1.5	–	pF
C_e	emitter capacitance	$I_C = i_c$ = 0; V_{EB} = 0.5 V; f = 1 MHz	–	11	–	pF
f_T	transition frequency	I_C = 10mA; V_{CE} = 5 V; f = 100 MHz	100	–	–	MHz
F	noise figure	I_C = 200 µA; V_{CE} = 5 V; R_S = 2 kΩ; f = 1 kHz; B = 200 Hz	–	2	10	dB

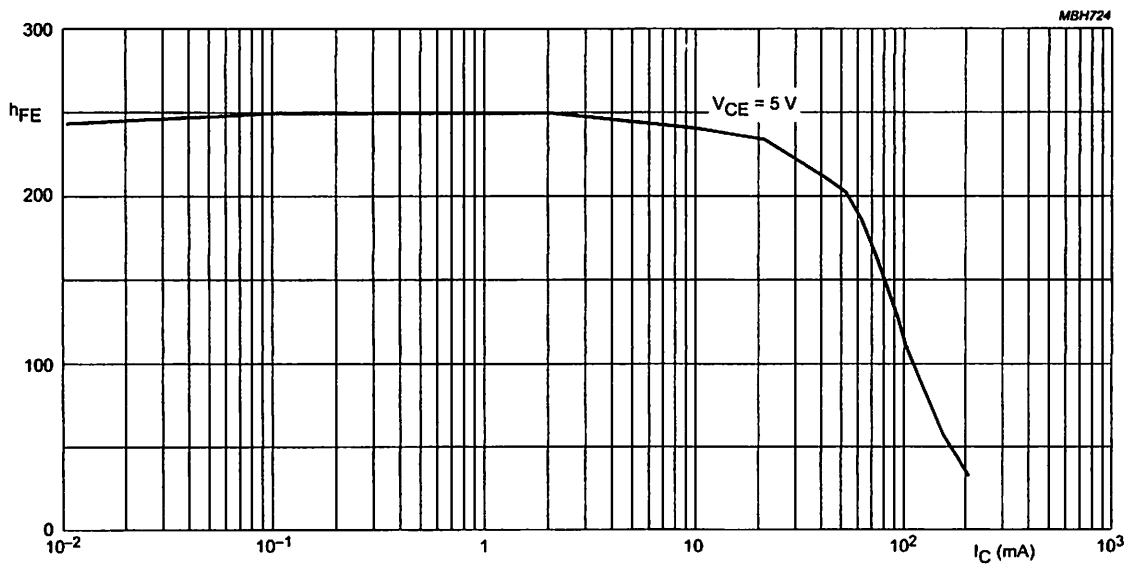
Notes

1. V_{BEsat} decreases by about 1.7 mV/K with increasing temperature.
2. V_{BE} decreases by about 2 mV/K with increasing temperature.



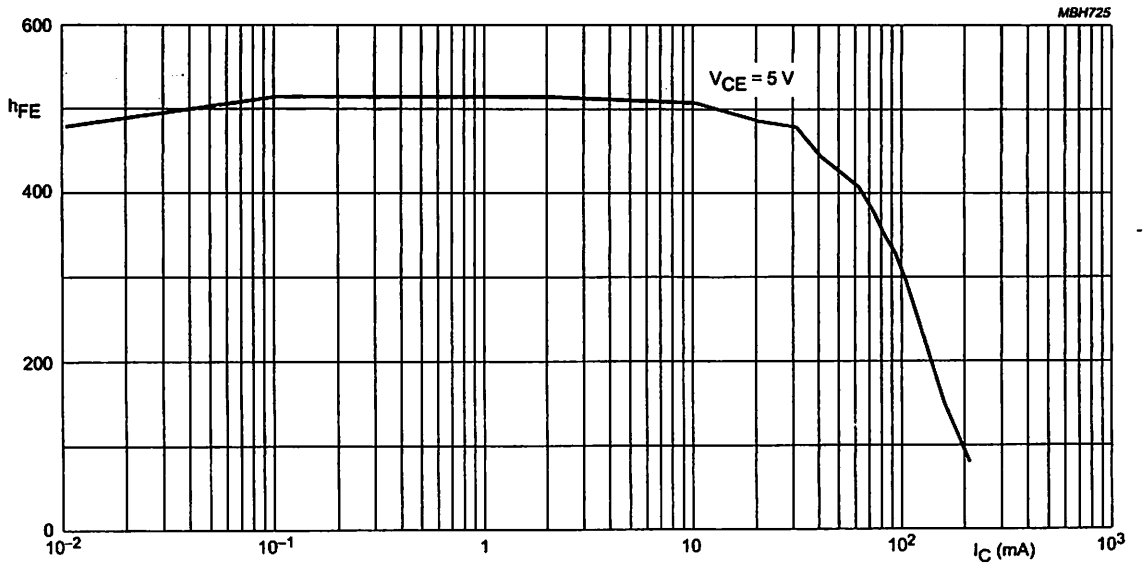
BC546A; BC547A; BC548A.

Fig.2 DC current gain; typical values.



BC546B; BC547B; BC548B.

Fig.3 DC current gain; typical values.

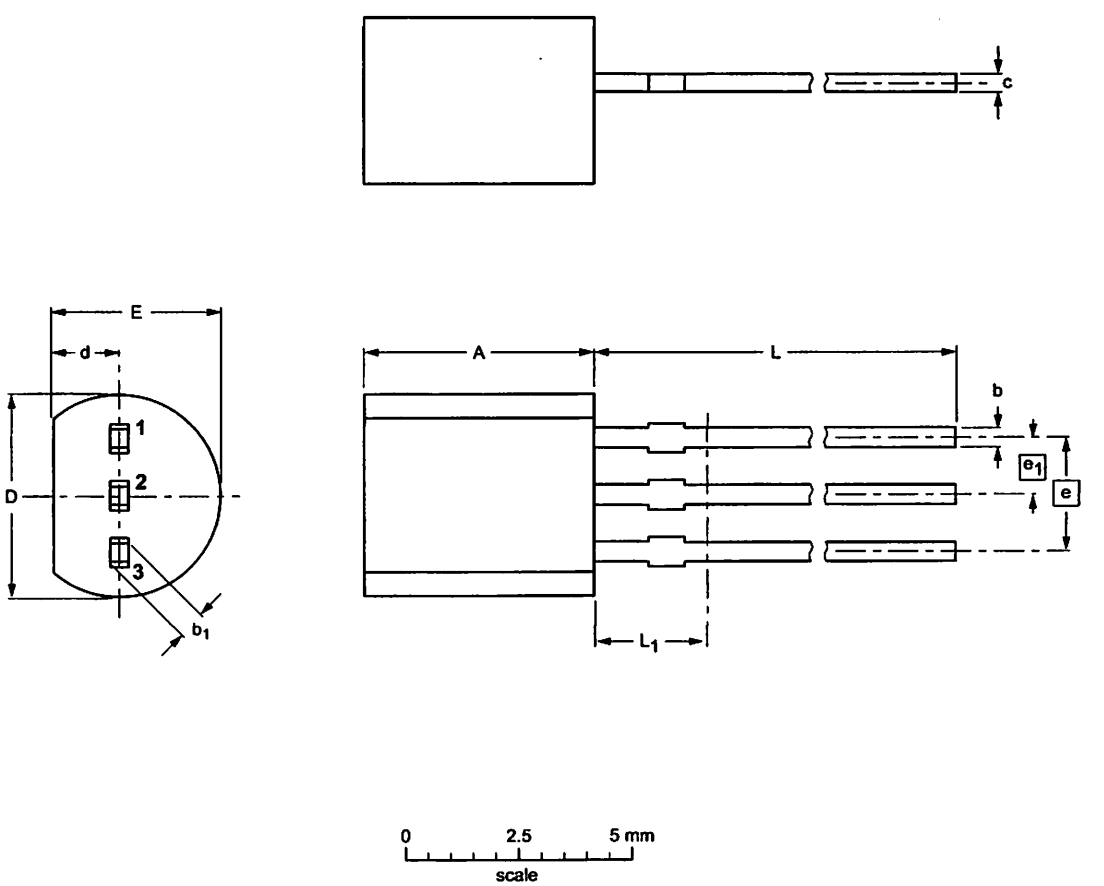


BC547C; BC548C.

Fig.4 DC current gain; typical values.

PACKAGE OUTLINE

Plastic single-ended leaded (through hole) package; 3 leads **SOT54**



DIMENSIONS (mm are the original dimensions)

UNIT	A	b	b_1	c	D	d	E	e	e_1	L	L_1(1)
mm	5.2 5.0	0.48 0.40	0.66 0.56	0.45 0.40	4.8 4.4	1.7 1.4	4.2 3.6	2.54	1.27	14.5 12.7	2.5

Note

1. Terminal dimensions within this zone are uncontrolled to allow for flow of plastic and terminal irregularities.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT54		TO-92	SC-43			97-02-28

)EFINITIONS

Data Sheet Status	
Objective specification	This data sheet contains target or goal specifications for product development.
Preliminary specification	This data sheet contains preliminary data; supplementary data may be published later.
Product specification	This data sheet contains final product specifications.
Limiting values	
Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.	
Application information	
Where application information is given, it is advisory and does not form part of the specification.	

.IFE SUPPORT APPLICATIONS

These products are not designed for use in life support appliances, devices, or systems where malfunction of these products can reasonably be expected to result in personal injury. Philips customers using or selling these products for use in such applications do so at their own risk and agree to fully indemnify Philips for any damages resulting from such improper use or sale.

NOTES

NOTES

NOTES

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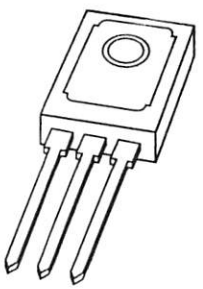
DATA SHEET



BD135; BD137; BD139
NPN power transistors

Product specification
Supersedes data of September 1994
File under Discrete Semiconductors, SC04

1997 Mar 04

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NPN power transistors BD135; BD137; BD139

EATURES

High current (max. 1.5 A)
Low voltage (max. 80 V).

PPLICATIONS

Driver stages in hi-fi amplifiers and television circuits.

ESCRIPTION

PN power transistor in a TO-126; SOT32 plastic ackage. PNP complements: BD136, BD138 and BD140.

PINNING

PIN	DESCRIPTION
1	emitter
2	collector, connected to metal part of mounting surface
3	base

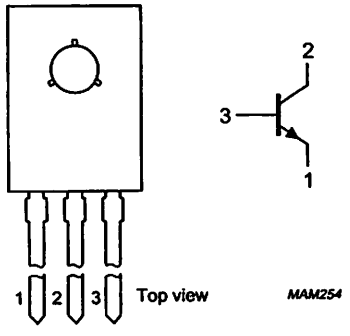


Fig.1 Simplified outline (TO-126; SOT32) and symbol.

UICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{CBO}	collector-base voltage	open emitter				
	BD135		–	–	45	V
	BD137		–	–	60	V
	BD139		–	–	100	V
V_{CEO}	collector-emitter voltage	open base				
	BD135		–	–	45	V
	BD137		–	–	60	V
	BD139		–	–	80	V
I_{CM}	peak collector current		–	–	2	A
P_{tot}	total power dissipation	$T_{mb} \leq 70$ °C	–	–	8	W
h_{FE}	DC current gain	I_C = 150 mA; V_{CE} = 2 V	40	–	250	
f_T	transition frequency	I_C = 50 mA; V_{CE} = 5 V; f = 100 MHz	–	190	–	MHz

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{CBO}	collector-base voltage	open emitter			
	BD135		–	45	V
	BD137		–	60	V
	BD139		–	100	V
V_{CEO}	collector-emitter voltage	open base			
	BD135		–	45	V
	BD137		–	60	V
	BD139		–	80	V
V_{EBO}	emitter-base voltage	open collector	–	5	V
I_C	collector current (DC)		–	1.5	A
I_{CM}	peak collector current		–	2	A
I_{BM}	peak base current		–	1	A
P_{tot}	total power dissipation	$T_{mb} \leq 70$ °C	–	8	W
T_{stg}	storage temperature		–65	+150	°C
T_j	junction temperature		–	150	°C
T_{amb}	operating ambient temperature		–65	+150	°C

THERMAL CHARACTERISTICS

SYMBOL	PARAMETER	CONDITIONS	VALUE	UNIT
$R_{th\ j\text{-}a}$	thermal resistance from junction to ambient	note 1	100	K/W
$R_{th\ j\text{-}mb}$	thermal resistance from junction to mounting base		10	K/W

Note

1. Refer to TO-126; SOT32 standard mounting conditions.

CHARACTERISTICS

T_j = 25 °C unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
I_{CBO}	collector cut-off current	I_E = 0; V_{CB} = 30 V	–	–	100	nA
		I_E = 0; V_{CB} = 30 V; T_j = 125 °C	–	–	10	µA
I_{EBO}	emitter cut-off current	I_C = 0; V_{EB} = 5 V	–	–	100	nA
h_{FE}	DC current gain	V_{CE} = 2 V; see Fig.2				
		I_C = 5 mA	40	–	–	
		I_C = 150 mA	40	–	250	
		I_C = 500 mA	25	–	–	
h_{FE}	DC current gain	I_C = 150 mA; V_{CE} = 2 V; see Fig.2				
	BD135-10; BD137-10; BD139-10		63	–	160	
	BD135-16; BD137-16; BD139-16		100	–	250	
V_{CEsat}	collector-emitter saturation voltage	I_C = 500 mA; I_B = 50 mA	–	–	0.5	V
V_{BE}	base-emitter voltage	I_C = 500 mA; V_{CE} = 2 V	–	–	1	V
f_T	transition frequency	I_C = 50 mA; V_{CE} = 5 V; f = 100 MHz	–	190	–	MHz
$\frac{h_{FE1}}{h_{FE2}}$	DC current gain ratio of the complementary pairs	$\lvert I_C \rvert$ = 150 mA; $\lvert V_{CE} \rvert$ = 2 V	–	1.3	1.6	

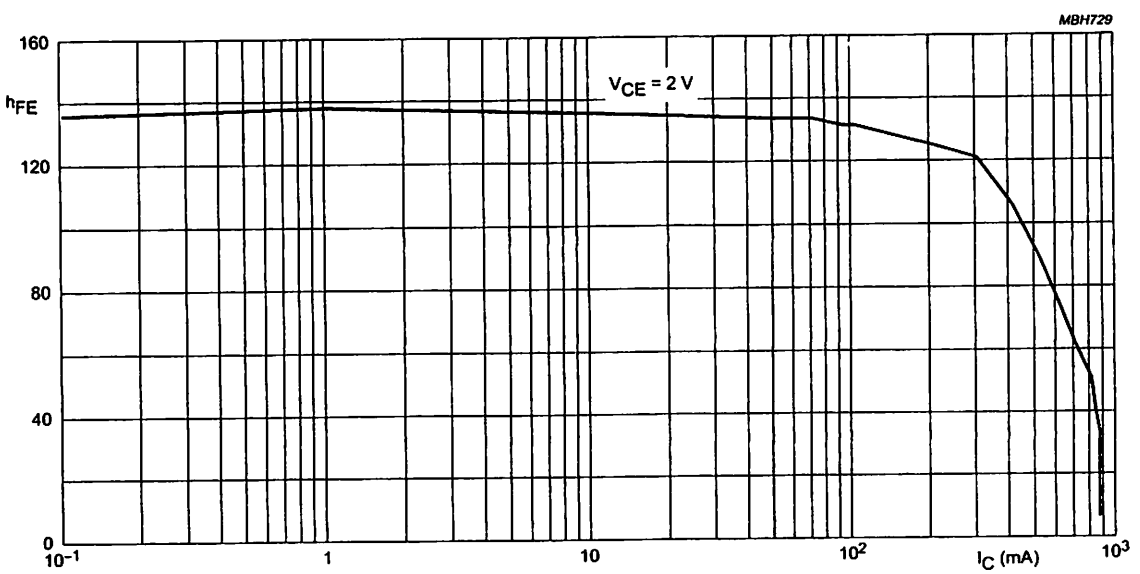
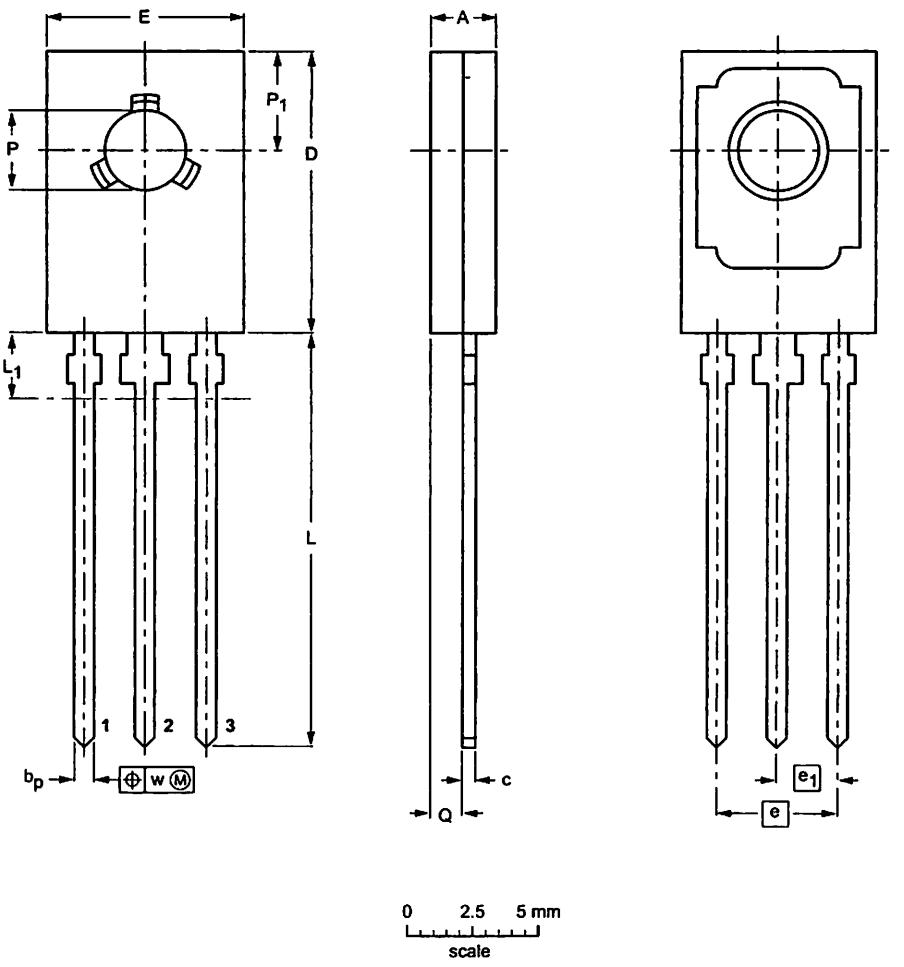


Fig.2 DC current gain; typical values.

PACKAGE OUTLINE

Plastic single-ended leaded (through hole) package; mountable to heatsink, 1 mounting hole; 3 leads SOT32



DIMENSIONS (mm are the original dimensions)

UNIT	A	b_p	c	D	E	e	e_1	L	L_1(1) max	Q	P	P_1	w
mm	2.7 2.3	0.88 0.65	0.60 0.45	11.1 10.5	7.8 7.2	4.58	2.29	16.5 15.3	2.54	1.5 0.9	3.2 3.0	3.9 3.6	0.254

Note

1. Terminal dimensions within this zone are uncontrolled to allow for flow of plastic and terminal irregularities.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT32		TO-126				97-03-04

DEFINITIONS

Data Sheet Status	
Objective specification	This data sheet contains target or goal specifications for product development.
Preliminary specification	This data sheet contains preliminary data; supplementary data may be published later.
Product specification	This data sheet contains final product specifications.
Limiting values	
Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.	
Application information	
Where application information is given, it is advisory and does not form part of the specification.	

LIFE SUPPORT APPLICATIONS

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