SKRIPSI

PERENCANAAN DAN PEMBUATAN JAM MATAHARI DIGITAL UNTUK MENENTUKAN WAKTU SHOLAT BERDASARKAN BAYANGAN MATAHARI DAN ORDINAT DAERAH BERBASIS AT89S8252

Disusun Oleh :

YULI ROHMAD RIADI

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KONSENTRASI TEKNIK ELEKTRONIKA

JURUSAN TEKNIK ELEKTRO S-1

FAKULTAS TEKNOLOGI INDUSTRI

INSTITUT TEKNOLOGI NASIONAL MALANG

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PERENCANAAN DAN PEMBUATAN JAM MATAHARI DIGITAL UNTUK MENENTUKAN WAKTU SHOLAT MENGGUNAKAN BAYANGAN MATAHARI DAN KOORDINAT DENGAN BERBASIS AT89C52

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LEMBAR PERSETUJUAN

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SKRIPSI

Disusun dan Diajukan Sebagai Salah Satu Syarat Untuk Memperoleh
Gelar Sarjana Teknik Elektro Strata Satu (S-1)

Disusun Oleh :

Yuli Rohmad Riadi
NIM : 0017055

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KONSENTRASI TEKNIK ELEKTRONIKA
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FAKULTAS TEKNOLOGI INDUSTRI
JURUSAN TEKNIK ELEKTRO S-1
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Tanggal : 24 September 2008
Dengan Nilai : 84 (A)

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ABSTRAK

PERENCANAAN DAN PEMBUATAN JAM MATAHARI DIGITAL UNTUK MENENTUKAN WAKTU SHOLAT BERDASARKAN BAYANGAN MATAHARI DAN ORDINAT DAERAH BERBASIS AT89S8252

(Yuli Rohmad Riadi, 0017055, Jurusan Teknik Elektro S-1/Elektronika)
(Dosen Pembimbing : Ir. Eko Nurcahyo.)

Kata Kunci : photo dioda, mikrokontroler, waktu sholat,matahari.

Pada skripsi ini telah direalisasikan sebuah jam waktu setempat (LMT = Local Mean Time) yaitu jam yang didasarkan atas perputaran semu matahari terhadap bumi dan pengingat waktu sholat. Untuk merealisasikan alat ini digunakan dua buah sensor photodioda yang diletakkan tepat dibawah benda yang akan membentuk bayangan pada saat kulminasi matahari. Arus dari kedua sensor photodioda dirubah menjadi digital oleh ADC PCF8951 dan selanjutnya dihubungkan dengan mikrokontroller AT89S8252 sebagai pusat kontrol untuk dibandingkan. Sebagai pengingat masuknya waktu sholat digunakan ISD 2560 sedangkan untuk penentu waktu digunakan RTC DS12887. Kelebihan alat ini dengan alat pengingat waktu sholat yang sudah ada adalah alat ini memanfaatkan fenomena alam berupa peredaran matahari. Alat ini juga akan memberikan peringatan ketika masuk waktu sholat berupa suara yang mejelaskan waktu sholat bukan suara adzan sehingga tuna netra juga bisa mengggunakannya. Selain itu alat ini bisa digunakan untuk mengoreksi jam biasa kita gunakan seperti WIB,WITA dan WIT. Dari hasil pengujian dapat disimpulkan bahwa sistem dapat bekerja dengan baik

KATA PENGANTAR

Atas Berkat Rahmat Allah Yang Maha Kuasa, penulis dapat menyelesaikan laporan Skripsi dengan judul:

" PERENCANAAN DAN PEMBUATAN JAM MATAHARI DIGITAL UNTUK MENENTUKAN WAKTU SHOLAT BERDASARKAN BAYANGAN MATAHARI DAN ORDINAT DAERAH BERBASIS AT89S8252"

Pembuatan Skripsi ini disusun guna memenuhi syarat akhir kelulusan pendidikan jenjang Strata-1 di Institut Teknologi Nasional Malang. Laporan Skripsi ini merupakan tanggung jawab tertulis atas ilmu pengetahuan yang didapat selama penyusun mengikuti kuliah.

Atas terselesaikannya Skripsi ini, penulis mengucapkan terima kasih kepada :

- Bapak Dr. Ir. Abraham Lomi, MSEE selaku Rektor Institut Teknologi Nasional Malang.
- Bapak Ir. Mochtar Asroni, MSME selaku Dekan Fakultas Teknologi Industri Institut Teknologi Nasional Malang
- Bapak Ir. Yudi Limpraptono, MT selaku Ketua Jurusan Teknik Elektro S1 / Elektronika.
- Bapak Ir. Eko Nurcahyo selaku Dosen Pembimbing yang telah memberikan bimbingan, pengarahan, serta ilmu-ilmu yang sangat berharga sehingga Skripsi ini dapat terselesaikan.

Penulis menyadari bahwa laporan ini masih banyak yang perlu disempurnakan. Oleh sebab itu kritik dan saran yang membangun sangat diharapkan.

Akhir kata, penulis mohan maaf kepada semua pihak bilamana selama penyusunan skripsi ini penyusun membuat kesalahan secara tidak sengaja dan semoga skripsi ini dapat bermanfaat bagi kita semua.

Malang, September 2008

Penulis

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BAB I

PENDAHULUAN

1.1. LATAR BELAKANG

Waktu sholat merupakan salah satu syarat untuk melaksanakan sholat. Waktu-waktu sholat telah diisyaratkan oleh Alloh swt dalam ayat-ayat al-Qur'an, yang kemudian dijelaskan oleh nabi Muhammad saw dengan amal perbuatannya berupa fenomena alam. Akan tetapi petunjuk tersebut tersebut sulit untuk kita laksanakan , misalkan untuk menentukan awal waktu dzuhur kita harus keluar rumah melihat matahari berkulminasi. Demikian pula untuk menetukan awal waktu sholat ashar kita harus keluar rumah dengan membawa tongkat kemudian mengukur dan membandingkan dengan panjang bayangan tongkat itu dan seterusnya. Oleh karena itu untuk lebih memudahkan kita dalam menetukan awal waktu sholat digunakanlah ilmu falak. Dengan menggunakan rumus-rumus perhitungan yang ada didalam ilmu falak kita dapat mengetahui awal waktu sholat dengan mudah

Seiring dengan perkembangan teknologi saat ini, waktu sholat tidak hanya berbentuk table diatas kertas akan tetapi sudah dikembangkan dalam bentuk alat peringatan waktu sholat yang dikontrol secara otomatis oleh mikrokontroller. Akan tetapi alat yang sudah ada saat ini hanya berpedoman pada waktu daerah tertentu saja seperti WIB saja, WIT saja atau WITA saja sehingga penggunaannya tidak bisa fleksibel. Apabila kita bisa memadukan antara perhitungan ilmu falak

yang sudah ada dengan fenomena alam yang berupa peredaran matahari maka hasilnya akan bisa maksimal.

Selama ini cara yang digunakan untuk mengetahui waktu peredaran matahari yaitu dengan melihat langsung pada alat bantu yang disebut jam matahari (*sundial*) atau biasa disebut jam istiwak. Akan tetapi alat itu bersifat permanen dan tidak dapat digunakan pada malam hari, selain itu alat tersebut tidak bisa digunakan didaerah lain apalagi yang ordinatnya jauh berbeda. Selain itu diperlukan ketelitian seorang dalam melihat jam tersebut.

Sundial yang sudah ada saat ini berupa lempengan bebentuk cekung dan diberi garis-garis busur serta diletakkan dengan kemiringan yang sesuai dengan ordinat daerah tersebut

1.2. RUMUSAN MASALAH

Dari uraian latar belakang di atas, maka didapatkan suatu rumusan masalah sebagai berikut

1. Bagaimana membuat jam matahari yang dapat digunakan di berbagai tempat di dunia ini yang memiliki perbedaan lintang yang tidak terlalu jauh yaitu 2 – 3 derajad
2. Bagaimana supaya alat tersebut dapat merubah jam setiap hari secara otomatis sesuai peredaran matahari
3. Bagaimana merealisasikan alat tersebut dengan sistem otomatis dan digital dengan menggunakan mikrokontroller AT89S8252

1.3. BATASAN MASALAH

Dalam perancangan dan pembuatan alat ini perlu dibatasi agar pembahasan tidak meluas yaitu antara lain:

1. Alat ini hanya bisa digunakan pada semua daerah didunia ini yang berada pada garis lintang 06° LS - 08° LS
2. Hanya berkisar penentuan jam istiwak dan pengingat waktu sholat
3. Teknologi kontrol menggunakan mikrokontroler AT89S8252 beserta perangkat lunak yang mendukung pembuatan alat tersebut
4. Tidak membahas *power supply.*
5. Tidak membahas ilmu falak secara mendetail.

1.4. TUJUAN

Tujuan dari pembuatan alat ini adalah membuat suatu alat yang dapat mengetahui waktu peredaran matahari dan pengingat waktu sholat secara otomatis yang dapat digunakan diseluruh daerah yang terletak pada 06° LS - 08° LS dengan menggunakan mikrokontroller AT89S8252 dan memanfaatkan fenomena alam berupa kulminasi matahari

1.5. METODELOGI

Metodologi dalam sistem kontrol frekwensi ultrasonic yang dihasilkan oleh receiver menggunakan teknologi mikrokontroler adalah sebagai berikut:

1. Kajian pustaka

   Bertujuan untuk mengumpulkan literatur yang berhubungan dengan perencanaan alat, dipadukan dengan teori yang didapat dibangku kuliah.

2. Perencanaan dan pembuatan alat

   Bertujuan untuk membuat diagram blok rangkaian yang sesuai dengan rencana kerja, yang kemudian direalisasikan dengan melaksanakan perencanaan dan pembuatan alat berdasarkan diagram blok rangkaian yang disusun.

3. Studi analisa alat

   Dimaksudkan untuk melakukan analisa dan pengujian alat yang telah dirancang, apakah sesuai dengan fungsi kerja yang diharapkan atau tidak.

4. Penyusunan buku laporan

   Bertujuan untuk menyusun data laporan berpedoman pada alat yang selesai dibuat berserta ksimpulan cara kerja dari alat tersebut

1.5. SISTEMATIKA PENULISAN

Penulisan Skripsi ini terdiri atas 5 bab dengan susunan pembahasan sebagai berikut :

BAB I. PENDAHULUAN

Berisi latar belakang, tujuan, permasalahan, batasan masalah, metodelogi, dan sistematika penulisan.

BAB II. LANDASAN TEORI

Membahas teori–teori dasar penunjang, perancangan dan pembuatan alat.

BAB III. PERANCANGAN DAN PEMBUATAN ALAT

Membahas tentang perancangan alat baik perangkat keras maupun perangkat lunak, serta cara kerja blok diagram.

BAB IV. PENGUJIAN ALAT

Mencakup pembahasan tentang proses pengujian alat yang terdiri dari peralatan yang digunakan, langkah kerja dan analisa hasil pengujian.

BAB V. PENUTUP

Berisi kesimpulan dan saran.

BAB II

LANDASAN TEORI

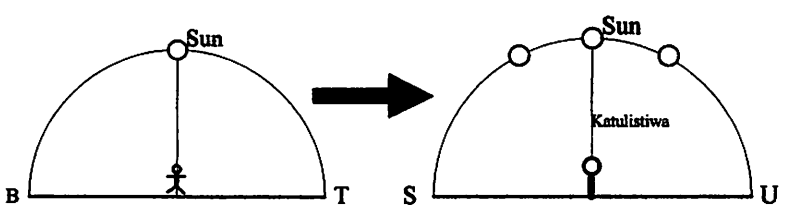
2.1. Perhitungan Awal Waktu Sholat

Penentuan awal waktu sholat pada zaman Rosulullah saw menggunakan fenomena alam baik berupa perubahan bayangan benda yang disebabkan oleh peredaran matahari ataupun warna langit. Akan tetapi seiring dengan perkembangan ilmu pengetahuan penentuan awal waktu sholat menggunakan perhitungan ilmu Falak.

2.1.1. Istilah Ilmu Falak dalam Penentuan Waktu Sholat

Adapun istilah ilmu falak yang digunakan dalam menentukan awal waktu sholat adalah sebagai berikut ;

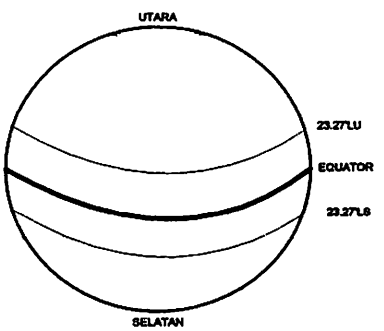
1. **Kulminasi Matahari**, yaitu kondisi dimana matahari berada pada titik puncak peredaran hariannya. Waktu kulminasi matahari / Waktu hakiki matahari selalu menunjukkan pukul 12



Gambar 2.1. Kulminasi Matahari

2. **Deklinasi Matahari,** yaitu jarak posisi matahari dengan equator / katulistiwa langit diukur sepanjang lingkaran deklinasi atau lingkaran waktu. Deklinasi sebelah Utara ekuator diberi tanda positif (+), dan sebelah Selatan ekuator diberi tanda negatif (-).

   Harga atau nilai deklinasi matahari, baik positif maupun negatif adalah 0° sampai sekitar 23° 27'. Harga deklinasi 0° terjadi pada setiap tanggal 21 Maret dan 23 September. Selama waktu (21 Maret sampai 23 September) deklinasi matahari positif, dan selama waktu (23 September sampai 21 Maret) deklinasi matahari negatif. Nilai deklinasi matahari yang mengalami perubahan dari waktu ke waktu dalam satu tahun dapat diketahui pada tabel-tabel astronomi, misalnya; Almanak Nautika, Ephemeris, dan lain-lain.



Gambar 2.2. Garis Batas Deklinasi Matahari

3. **Lintang Daerah Setempat,** yaitu jarak dari daerah / tempat yang dimaksud sampai Khatulistiwa diukur sepanjang garis bujur. Khatulistiwa adalah lintang 0°. Disebelah Selatan Khatulistiwa disebut

Lintang Selatan , diberi tanda negatif (-). Diesebelah Utara Khatulistiwa disebut Lintang Utara, diberi tanda positif (+).

4. **Sudut Waktu Matahari,** yaitu busur sepanjang lingkaran harian matahari dihitung dari titik kulminasi atas sampai matahari berada. Harga sudut matahari dapat dihitung dengan rumus ;

   $\cos t = -\tan \phi \cdot \tan \delta_0 + \sin h : \cos \phi : \cos \delta_0$

   ϕ = Lintang Tempat

   δ_0 = Deklinasi Matahari

   h = Tinggi Matahari

   t = Sudut Waktu Matahari

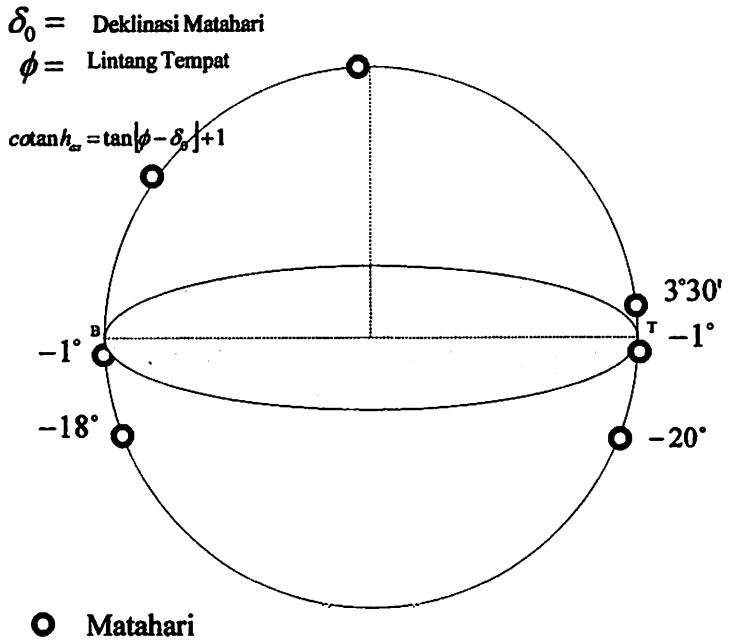
5. **Meridian Pass (MP),** yaitu hasil pengurangan Waktu Hakiki dengan Perata Waktu (*Equation of Time*, yang disimbulkan dengan e)

   Rumus : MP = 12 - e

6. **Perata Waktu,** yaitu selisih antara waktu hakiki dengan waktu pertengahan (jam arloji). Perata Waktu juga disebut dengan *Equation of Time* (e). Secara detail data *Equation of Time* dapat diperoleh pada almanak astronomi, seperti Almanak Nautika atau pada Almanak Ephemeris Hisap Rukyat

7. **Waktu Setempat,** yaitu waktu pertengahan menurut bujur tempat di suatu tempat, sehingga sebanyak bujur tempat di permukaan bumi sebanyak itu pula waktu pertengahan didapati. Waktu demikian ini disebut juga dengan *Local Mean Time* (LMT)

8. **Tinggi Matahari,** yaitu kedudukan matahari pada awal-awal waktu shalat tersebut menurut ilmu falak



Gambar 2.3. Tinggi Matahari

Keterangan ;

1. Cotan h asar $= \tan [\ \phi - \delta_0\ ] + 1]$
2. h magrib $= -1^0$
3. h isya' $= -18^0$
4. h subuh $= -20^0$
5. h imsak $= -22^0$
6. h terbit $= -01^0$
7. h dluha $= 03^0\ 30'$

2.1.2. Perhitungan Waktu Sholat

Untuk menghitung awal waktu sholat terlebih dahulu harus mengumpulkan data yang diperlukan seperti lintang tempat, deklinasi matahari, *equation of time* dan tinggi matahari. Setelah data terkumpul kemudian diproses sesuai dengan langkah-langkah berikut :

1. Menghitung Sudut Waktu Matahari (t)
2. Mengkonversi nilai sudut waktu (t) menjadi satuan waktu, dengan cara t:15.
3. a. Untuk awal waktu Ashar, Maghrib dan Isya' digunakan rumus

   LMT = MP + t:15

   b. Untuk awal waktu Subuh digunakan rumus

   LMT = MP - t:15

2.1.3. Menentukan Arah Mata Angin

Untuk menentukan arah mata angin dapat dilakukan dengan kompas ataupun dengan tongkat istiwak

1. Kompas Magnetic

   Kompas Magnetic adalah alat penunjuk arah mata angin. Alat ini paling mudah digunakan, tetapi perlu diketahui bahwa kompas magnetik mempunyai kelemahan, diantaranya :

   a. Kompas magnetic peka terhadap benda-benda logamyang berada disekitarnya.

b. Kutub utara magnet yang merupakan alat utama dalam kompas tidak selalu berimpit dengan kutub utara bumi, sehingga penunjukan kompas tidak selalu tepat arah utara-selatan yang sesungguhnya, yang disebut variasi magnet atau deklinasi kompas.

2. Tongkat Istiwa'

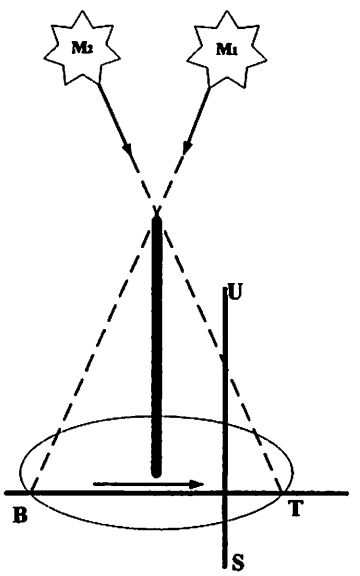
Menentukan arah mata angin dengan menggunakan tongkat istiwa' atau dengan bantuan sinar matahari merupakan cara yang lebih akurat hasilnya daripada menggunakan kompas.

Adapun langkah-langkah yang harus ditempuh adalah sebagai berikut :

a. Pilih tempat yang rata, datar dan terbuka
b. Buatlah sebuah lingkaran ditempat itu dengan jari-jari sekitar 0,5 meter
c. Tancapkan sebuah tongkat lurus setinggi sekitar 1,5 meter tegak lurus tepat ditengah lingkaran itu.
d. Berilah tanda titik B pada titik perpotongan antara bayangan tongkat itu dengan garis lingkaran sebelah barat (ketika bayangan sinar matahari mulai masuk lingkaran). Titik B ini terjadi sebelum waktu dhuhur.
e. Berilah tanda titik T pada titik perpotongan antara bayangan tongkat itu dengan garis lingkaran sebelah Timur (ketika bayangan sinar matahari mulai keluar lingkaran). Titik T ini terjadi sesudah waktu dhuhur.

f. Hubungkan titik B dan titik T tersebut dengan garis lurus / tali. Titik B merupakan titik barat sejati dan T merupakan titik timur sejati

g. Buatlah garis tegak lurus dengan garis barat-timur tadi, maka garis ini menunjukkan titik Utara-Selatan sejati



Gambar 2.4. Tongkat Istiwa'
(Sumber : Moh. Murtadho, 2008:158)

M_1 = Posisi matahari sebelum Dhuhur

M_2 = Posisi Matahari setelah Dhuhur

⟶ = Arah gerak bayangan ujung tongkat

B = Titik perpotongan bayangan ujung tongkat (Barat)

T = Titik perpotongan bayangan ujung tongkat (Timur)

U = Utara

S = Selatan

2.2. Mikrokontroller AT89S8252

2.2.1. Teori Dasar Mikrokontroller AT89S8252

Mikrokontroller AT89S8252 merupakan mikrokontroller 8 bit kompatibel dengan standart industri MCS-51 baik atas segi pemrograman maupun atas kaki tiap pin. Mikrokontroller AT89S8252 mempunyai 8 Kbyte PEROM (*Flash Programmable and Eraseble read Only Memory*). Pada dasarnya adalah terdiri atas mikroprosesor, *timer, counter*, perangkat I/O dan internal memori. Mikrokontroller termasuk perangkat yang sudah didesain dalam bentuk cip tunggal.

Pada dasarnya mikrokontroller mempunyai fungsi yang sama dengan mikroprosesor yaitu mengontrol suatu kerja sistem. Selain itu juga mikrokontroller juga dikemas dalam satu *chip* (*single chip*). Didalam mikrokontroller juga terdapat CPU, ALU, PC, SP dan register seperti dalam mikroprosesor, tetapi juga ditambah dengan perangkat – perangkat lain seperti POM, PAM, SIO, *counter* dan juga ditambah rangkaian *clock*. Mikrokontroller didesain instruksi – instruksi lebih luas dan 8 bit instruksi yang digunakan membaca data instruksi

2.2.2. Fitur Mikrokontroler Atmel AT89S8252

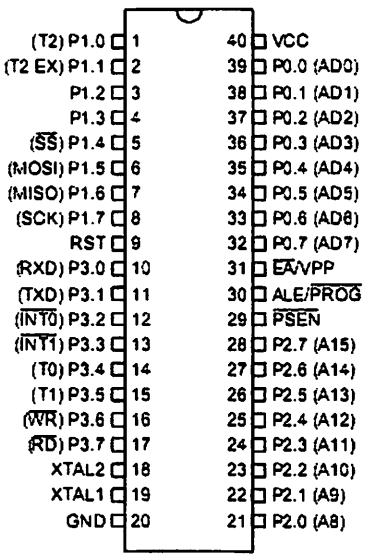
Mikrokontroler AT89S8252 merupakan pengembangan dari mikrokontroler standard MCS – 51, dengan banyak kelebihan yang ditawarkan antara lain :

- Kompatibel dengan Mikrokontroler MCS – 51
- 8K byte Downloadable Flash memori
- 2K byte EEPROM
- 3 level program memori lock
- 256 byte RAM internal
- 32 I/O yang dapat dipakai semua
- 3 buah timer / counter 16 bit
- Programmable watchdog timer
- Dual data pointer
- Frekuensi kerja 0 sampai 24 MHZ
- Tegangan operasi 2,7 – 6 volt

Dipakainya downloadable flash memori memungkinkan mikrokontroler ini bekerja sendiri tanpa diperlukan tambahan chip lainnya. Dan flash memori dapat diprogram hingga seribu kali. Hal lain yang menguntungkan adalah sistem pemrograman jauh lebih sederhana dan tidak memerlukan rangkaian yang rumit seperti rangkaian untuk memprogram AT89C51.

Timer / counter juga bertambah satu dari standar 2 buah pada MCS – 51. Selain itu frekuensi kerja yang lebar dan rancangan statik sangat membantu untuk proses *debugging*. Dengan adanya beberapa fitur tambahan itu, maka akan mengakibatkan bertambahnya SFR (*Special Function Register*). Gambar berikut adalah gambar mikrokontroler AT 89S8252. Tata letak pin – pin ini masih

mengacu pada mikrokontroler MCS – 51 sehingga AT 89S8252 dapat menggantikan mikrokontoler MCS – 51.



Gambar 2.5. Mikrokontroler AT89S8252
(Sumber: Data Sheet ATMEL AT89S8252)

Keterangan pin :

1. Pin 40 (VCC)

   Merupakan pin catu daya dengan tegangan sebesar +5 V (DC)

2. Pin 20 (GND)

   Merupakan pin GROUND yang nanti terhubung dengan grounding rangkaian.

3. Pin 32 – 39 (Port 0)

   PORT 0 mempunyai fungsi sebagai port alamat dan data , maka jika mikrokontroler sedang mengakses alamat, P0 akan aktif sebagai

pembawa alamat 8 bit yang bawah (A0 – A8). Ketika mengakses data (bisa input atau output) port ini sebagai jalur data (D7 – D0).

4. Pin 21 – 28 (Port 2)

   Port 2 berfungsi sebagai pembawa alamat 8 bit atas (A8 – A15). Berbeda dengan port 0, port ini tidak bersifat sebagai jalur data hanya sebagai pembawa alamat. Dengan demikian jelas bahwa untuk alamat AT89S8252 menyediakan 16 bit sedangkan untuk jalur data hanya 8 bit.

5. Pin 10 – 17 (port 3)

   Port 3 ini mempunyai fungsi yang berlainan dari setiap pin-pinnya, seperti yang di tunjukkan di bawah ini:

   A. P 3.7: Kaki *read* yang aktif manakala sedang melakukan eksekusi yang sifatnya membaca data.

   B. P 3.6 : Kaki *write* yang aktif saat melakukan eksekusi yang sifatnya menulis data ke suatu alamat.

   C. P 3.5 : Merupakan pin yang berhubungan dengan timer register timer 1 (T1).

   D. P 3.4 : Merupakan pin yang berhubungan dengan timer register timer 0 (T0).

   E. P 3.3 : Berhubungan dengan control interupt (INT1).

   F. P 3.2 : Berhubungan dengan control interupt (INT0).

   G. P 3.1 : Berhubungan dengan port serial (TXD).

   H. P 3.0 : Berhubungan dengan port serial (RXD).

Untuk lebih jelasnya lihat daftar tabel dibawah ini :

Tabel 2.1. Konfigurasi Port 3 Atmel 89S8252

Port Pin	Alternate Functions
P3.0	RXD (serial input port)
P3.1	TXD (serial output port)
P3.2	$\overline{\text{INT0}}$ (external interrupt 0)
P3.3	$\overline{\text{INT1}}$ (external interrupt 1)
P3.4	T0 (timer 0 external input)
P3.5	T1 (timer 1 external input)
P3.6	$\overline{\text{WR}}$ (external data memory write strobe)
P3.7	$\overline{\text{RD}}$ (external data memory read strobe)

(Sumber: Data Sheet ATMEL AT89S8252)

6. Pin 9 (RST (*Reset*))

   Pin reset ini aktif tinggi (1), jika pin ini aktif tinggi minimal dua kali siklus mesin bekerja maka akan mereset peralatan.

7. Pin 30 (ALE/PROG (*Address Latch Enable/Program*))

   Pin ALE ini aktif tinggi dengan mengeluarkan pulsa output untuk melatch (mengunci/menahan) 1 byte alamat rendah selama mengakses ke alamat memori eksternal. ALE dapat mengendalikan 8 beban TTL dan juga merupakan input program yang aktif rendah selama pemrograman *Flash Eprom*. Pada operasi normal, ALE dikeluarkan pada suatu kecepatan yang konstan yaitu 1/6 dari frekuensi osilator, dan juga dapat dipergunakan untuk pewaktu atau timing eksternal atau untuk pemberian clock.

8. Pin 29 (PSEN (*Program Strobe Enable*))

   Pin ini aktif rendah, yang merupakan pulsa pengaktif untuk pembacaan ke program memori eksternal.

9. Pin 19 (XTAL - !)

   Sebagai pin input ke penguat osilator pembalik dan input rangkaian clock internal untuk operasi sistem.

10. Pin 18 ((XTAL – 2)

    Pin output dari penguat osilator.

11. Pin 31 (EA/VPP (*Externall Access/Program Supplay Voltage*))

    Pin ini harus di tahan dalam kondisi rendah secara eksternal atau dihubungkan ke-*ground* agar AT 89S8252 dapat mengakses kode mesin dari memori eksternal. Jika menggunakan internal program memori maka pin ini harus diberi logika tinggi (1).

Semua pin pada mikrokontroler AT 89S8252 adalah sama dengan mikrokontroler MCS – 51. Namun pada port 1 mikrokontroler AT 89S8252 terdapat beberapa fungsi khusus yang tidak terdapat pada mikrokontoler MCS – 51. Fungsi khusus tersebut dijelaskan pada tabel berikut :

Tabel 2.2. Fungsi khusus pada Port 1 Atmel 89S8252

Port PIN	Fungsi Khusus
P 1.0	T2 (masukan luar untuk timer / counter 2)
P 1.1	T2 EX (timer / counter capture / reload trigger dan control arah)

P 1.2	-
P 1.3	-
P 1.4	SS (*slave port select input*)
P 1.5	MOSI (master data ouput, slave dan input untuk kanal SPI)
P 1.6	MISO (master data input, slave data output untuk kanal SPI)
P 1.7	SCK (master clock output, slave clock input untuk kanal SPI)

(Sumber: Data Sheet ATMEL AT89S8252)

2.2.3. SFR tambahan pada Atmel AT89S8252

Selain memiliki SFR(*Special Function Register*) seperti halnya pada MCS-51, mikrokontroler Atmel AT89S8252 memiliki tambahan SFR. Hal ini tak lain adalah karena adanya fitur tambahan pada mikrokontroler Atmel AT89S8252.

SFR tambahan ini meliputi: T2CON(Timer 2 Register dangan alamat 0C8H), T2MOD(*Timer 2 Mode* dengan alamat 0C9H), WMCON(*Watchdog and Memory Control Register* dengan alamat 96H), SPCR(*SPI Control Register* dengan alamat D5H), SPSR(*SPI Status Refister* dengan alamat AAH), SPDR (SPI Data Register dengan alamat 86H).

Tabel 2.3. AT89S8252 SFR Map dan Reset Value

F8H								FFH
F0H	B 00000000							F7H
E8H								EFH
E0H	ACC 00000000							E7H
D8H								DFH
D0H	PSW 00000000					SPCR 00000XX		D7H
C8H	T2CON 00000000	T2MOD XXXXXX00	RCAP2L 00000000	RCAP2H 00000000	TL2 00000000	TH2 00000000		CFH
C0H								C7H
B8H	IP XX000000							BFH
B0H	P3 11111111							B7H
A8H	IE 0X000000		SPSR 00XXXXXX					AFH
A0H	P2 11111111							A7H
98H	SCON 00000000	SBUF XXXXXXXX						9FH
90H	P1 11111111						WMCON 00000010	97H
88H	TCON 00000000	TMOD 00000000	TL0 00000000	TL1 00000000	TH0 00000000	TH1 00000000		8FH
80H	P0 11111111	SP 00000111	DPOL 00000000	DPOH 00000000	DP1L 00000000	DP1H 00000000	SPDR XXXXXXXX	PCON 0XXX0000	87H

(Sumber: Data Sheet ATMEL AT89S8252)

2.2.4. Data Memory (EEPROM) dan RAM

Berbeda dengan mokrokontroler standart MCS-51, mikrokontroler Atmel AT89S8252 juga dilengkapi dengan data memori yang berupa EEPROM (*Electrically Erasable Programmable Read Only Memory*). EEPROM yang ditanamkan ini besarnya 2 kilo byte (2K) dan dipakai untuk penyimpanan data.

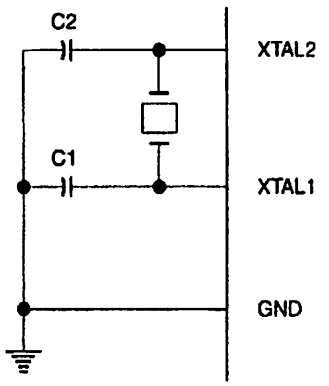
EEPROM ini diakses dengan mengeset bit EEMEN pada register WMCON pada alamat 96H. Alamat EEPROM ini adalah 000H sampai 7FFH. Instruksi movx digunakan untuk mengakses EEPROM internal ini. Namun jika

ingin mengakses data memori luar (diluar mikrokontroler Atmel AT89S8252) dengan menggunakan instruksi movx ini maka bit EEMEN harus dibuat"0".

Bit EEMWE pada register WMCON harus diset ke 1 sebelum sembarang lokasi padaEEPROM dapat ditulisi. Program pengguna harus mereset bit EEMWE ke "0" jika proses penulisan ke EEPROM tidak diperlukan lagi. Proses penulisan pada EEPROM dapat dilihat dengan membaca bt RDY/BSY pada SFR WMCON. Jika bit ini berlogika rendah maka penulisan EEPROM sedang berlangsung, jika bit ini berlogika tinggi maka penulisan sudah selesai dan penulisan lain dapat dimulai lagi. Sedangkan RAM yang ada pada mikrokontroler Atmel AT89S8252 adalah berkapasitas 256 byte. Penjelasan mengenai RAM ini adalah sama dengan RAM yang ada pada mikrokontroler standart MCS-51.

2.2.5. Oscillator

Mikrokontroler Atmel AT89S8252 memiliki osilator internal (*on chip oscillator*) yang dapoat digunakan sebagai sumber pewaktu (*clock*) bagi CPU. Untuk menggunakan internal diperlukan sebuah kristal atau resonator keramik antara pin $XTAL_1$ dan pin $XTAL_2$ dan sebuah kapasitor ke *ground*. Untuk kristal digunakan dengan frekuensi dari 6 – 24 MHz, sedangkan kapasitor dapat bernilai 27 – 33 pF.



Gambar 2.6. Osilator External AT89S8252
(Sumber: Data Sheet ATMEL AT89S8252)

2.2.6. Sistem Interrupt

Mikrokontroler Atmel AT89S8252 mempunyai 5 buah sumber interupsi, 2 eksternal interupsi (INT0 dan INT1), 2 timer interupsi (Timer0 dan Timer1), dan serial port interupsi.

- **INT0** : Interrupt pada P 3.2 (pin 12)
- **INT1** : Interrupt pada P 3.3 (pin 13)
- **Timer0** : Timer pada P 3.4 (pin 14)
- **Timer1** : Timer pada P 3.5 (pin 15)

Saat terjadinya interrupt mikrokontroller secara otomatis akan menuju ke subrutin pada alamat tersebut. Setelah interrupt servise selesai dikerjakan mikrokontroller akan mengerjakan program semula. Dua sumber external adalah INT0 dan INT1 pada register TCON. Interrupt T0 dan T1 aktif pada saat timer yang sesuai mengalami roll over. Interrupt serial dibangkitkan dengan melakukan operasi OR pada R1 dan T1. Setiap sumber interupsi dapaat enable atau disable

secara software. Tingkat prioritas semua sumber interupsi dapat diprogram sendiri - sendiri dengan set atau clear bit pada SFRS IP (*interrupt priority*). Register yang berperan mengatur aktif tidaknya adalah interrupt enable register.

2.2.7. Programable Watchdog Timer (WDT)

Pada mikrokontroler Atmel AT89S8252 juga dilengkapi oleh *watchdog Timer* ini menggunakan detak tersendiri. Untuk mengatur rentang waktu (perioda) pada WDT ini maka terdapat bit prescaler yang dapat mengatur rentang waktru yang dibutuhkan.

Bit prascaler ini adalah bit PS0, PS1dan PS2 pada register WMCON. Perioda waktu pada WDT ini berkisar dari 16 mili detik sampai 2048 mili detik. Karena bit prescalernya ada 3, maka akan ada 8 buah kemungkinan yaitu:

Tabel 2.4. Pemilihan Perioda Waktu WDT

WDT Prescaler Bits			Period (nominal)
PS2	PS1	PS0	
0	0	0	16 ms
0	0	1	32 ms
0	1	0	64 ms
0	1	1	128 ms
1	0	0	256 ms
1	0	1	512 ms
1	1	0	1024 ms
1	1	1	2048 ms

(Sumber: Data Sheet ATMEL AT89S8252)

WDT dilumpuhkan oleh Power on Reset (POR) dan selama Power Down. WDT diaktifkan dengan menseting bit WDTEN pada SFR WMCON

(alamat 96H). Jika perhitungan waktu WDT telah selesai tanpa ada reset atau dilumpuhkan, maka suatu pulsa reset internal akan dihasilkan untuk mereset CPU.

2.2.8. Timer 2

Pada mikrokontroler Atmel AT89S8252 terdapat tambahan *Timer* 2. *Timer* yang lain adalah *timer* 0 dan *timer* 1. Hal yang perlu diperhatikan adalah *Timer/Counter* dapat digunakan sebagai generator *baudrate* untuk serial *port.* Pada standart MS-51 biasanya yang digunakan adalah *timer* 1 sebagai penghasil *baudrate*. Pada mikrokontroler Atmel AT89S8252 selain menggunakan *timer* 1 sebagai *baudrate* (untuk menjaga kompabilitas dengan MCS-51) juga dapat menggunakan *Timer* 2 sebagai penghasil *baudrate* untuk serial *port. Timer* 2 ini merupakan Timer/Counter yang berukuran 16 bit yang dapat beroperasi sebagai timer atau dapat beroperasi sebagai penghitung kejadian dengan detak dari luar. Untuk mengatur fungsi ini dilakukan dengan mengatur bit C/T2 pada SFR T2CON. Terlihat bahwa jika bit ini tinggi maka akan terpilih fungsi *counter*, tapi jika bit ini rendah maka akan terpilih fungsi *Timer* 2.

Timer 2 ini memiliki 3 mode operasi yaitu: *capture, auto reload (up dan down counting)* dan *baud rate* generator. Untuk memilih mode ini dilakukan dengan mengatur bit pada SFR T2CON.

Timer 2 ini terdiri dari 2 buah *timer* 8 bit *register* yaitu TH2 dan TL2 dinaikkan tiap siklus mesin. Karena siklus mesin terdiri dari 1 *periode* osilasi, maka *count rate* menjadi 1/12 dari frekuensi osilator.

Pada fungsi *counter, register* dinaikkan berdasarkan tanggapan adanya transisi tinggi ke rendah pada pena yang bersesuaian (dalam hal ini pin T2 atau Pi.0). pada fungsi ini, masukan luar akan disampling selama S5P2 dari tiap siklus mesin. Jika hasil sampling menunjukkan logika tinggi pada selama satu siklus dan logika rendah pada siklus selanjutnya maka akan terdeteksi transisi tinggi ke rendah dan akibatnya perhitungan akan dinaikkan. Nilai perhitungan yang baru akan muncul pada register selama S3P1 dari siklus setelah transisi tinggi ke rendah terdeteksi.

Tabel 2.5. Mode Operasi Timer 2

RCLK + TCLK	CP/$\overline{RL2}$	TR2	MODE
0	0	1	16-bit Auto-Reload
0	1	1	16-bit Capture
1	X	1	Baud Rate Generator
X	X	0	(Off)

(Sumber: Data Sheet ATMEL AT89S8252)

2.3. Inter Intergrated Circuit Bus (I^2C)

2.3.1. Konsep I^2C

Pada saat ini desain elektronik dituntut untuk semakin ringkas dan fleksibel, dimana ukuran fisik IC semakin diperkecil dan jumlah pin diminimalkan dengan tetap menjaga fleksibilitas dan kompabilitas IC sehingga mudah untuk digunakan dalam berbagai keperluan desain yang berbeda, oleh karenanya banyak perusahaan semikonduktor yang berusaha mengembangkan cara baru komunikasi atas IC yang lebih akomodatif terhadap tuntutan diatas

sebagai alternatif dari hubungan antar IC secara parallel (parallel bus) yang sudah kita kenal luas. Salah satu medote yang sudah matang dan dipakai secara luas adalah IIC (sering ditulis I^2C) singkatan dari *Inter Integrated bus* yang dikembangkan oleh Philips Semiconductor sejak tahun 1992, dengan konsep dasar komunikasi 2 arah antar IC dan atau antar sistem secara serial menggunakan 2 kabel.

2.3.2. Fitur Utama I^2C

Fitur utama dari I^2C bus adalah sebagai berikut :

- Hanya melibatkan 2 kabel yaitu *serial data line* (SDA) dan *serial clock line* (SCL)
- Setiap IC yang terhubung dalam I^2C memiliki alamat yang unik yang diakses secara software dengan *master/slave* protokol yang sederhana
- I^2C merupakan serial bus dengan orientasi data 8 bit (byte), komunikasi 2 arah

2.3.3. Keuntungan I^2C

Keuntungan yang didapat dengan menggunakan I^2C antara lain :

1. Meminimalkan jalur hubungan antar IC (dibandingkan dengan parallel bus)
2. Menghemat luasan PCB yang dibutuhkan

3. Membuat sistem yang didesain beorientasi software (mudah diekspan dan diupgade).
4. Membuat sistem yang didesain menjadi standart, sehingga dapat dihubungkan dengan sistem lain yang juga menggunakan I^2C bus.

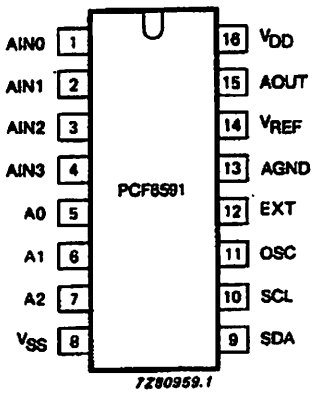
2.3.4. I^2C PCF8591 8-bit ADC

ADC PCF8591 adalah suatu chip tunggal buatan Philips Semikonduktor, dengan empat masukan analog dan suatu serial penghubung I^2C bus. Tiga alamat pin A0, A1, dan A2 digunakan untuk memprogram perangkat keras dan biasa digunakan sebagai I^2C bus.

Spesifikasi yang dimiliki oleh ADC PCF8591 adalah :

1. Kompaibel penuh dengan *mikrokontroller*
2. Hanya perlu dua jalur kabel untuk *interface* dengn *mikrokontroller*
3. *Analog input* 4 chanel 8 bit
4. *Analog output* 1 chanel 8 bit
5. *Input range* tegangan 0 V – 2,5 V
6. Operasi supply tegangan 2,5 Volt sampai 6 Volt
7. *Auto – incremented chanel selection*
8. *Multiplying DAC with one analog output*

Adapun konfigurasi pin dari ADC PCF8591 adalah sebagai berikut :



Gambar 2.7. Pin ADC PCF8951
(Sumber : Datasheet PCF8951)

Tabel 2.6. Fungsi Pin ADC PCF8951

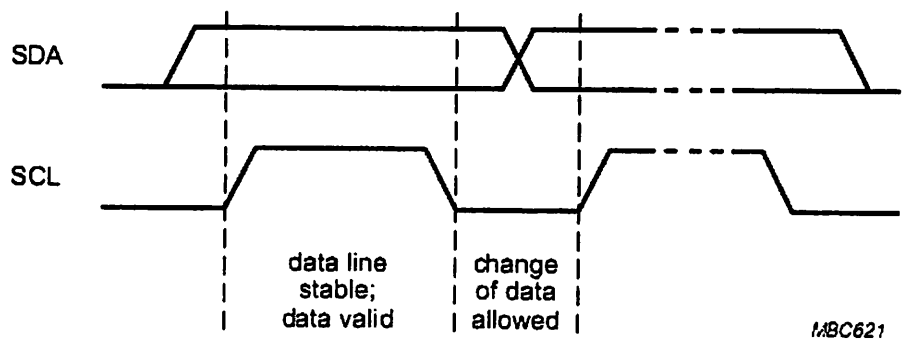
SYMBOL	PIN	DESCRIPTION
AINO	1	analog inputs (A/D converter)
AIN1	2	
AIN2	3	
AIN3	4	
A0	5	hardware address
A1	6	
A2	7	
V_{SS}	8	negative supply voltage
SDA	9	I^2C-bus data input/output
SCL	10	I^2C-bus clock input
OSC	11	oscillator input/output
EXT	12	external/internal switch for oscillator input
AGND	13	analog ground
V_{REF}	14	voltage reference input
AOUT	15	analog output (D/A converter)
V_{DD}	16	positive supply voltage

(Sumber : Datasheet PCF8951)

2.3.5. Cara Kerja I^2C Bus

2.3.5.1. Karakter Transfer Data Bit

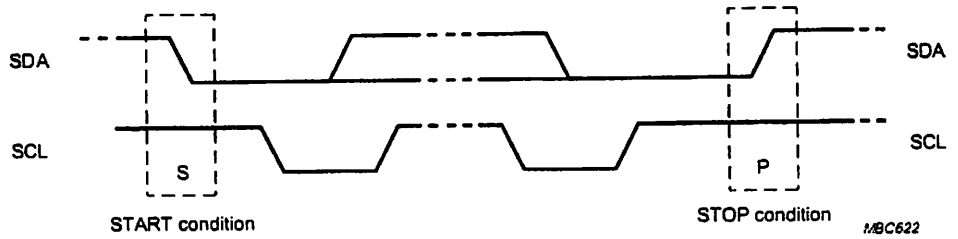
Data bit dikirim atau diterima melalui SDA, sedangkan sinyal clock dikirim/diterima SCL, dimana dalam setiap trasfer data bit satu sinyal clock dihasilkan. Transfer data bit dianggap valid jika data bit pada SDA tetap stabil selama data clock high. Data bit hanya boleh berubah jika sinyal clock dalam kondisi low.



Gambar 2.8. Transfer Data Bit Pada I^2C Bus
(Sumber : Datasheet PCF8951)

2.3.5.2. Kondisi START dan STOP

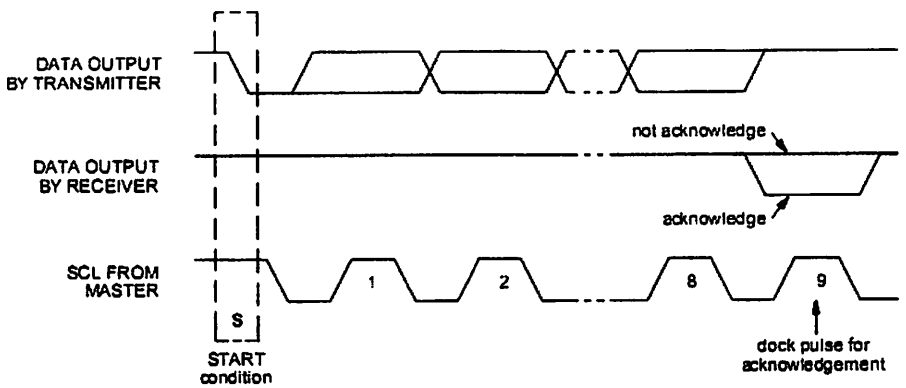
Apabila pada SDA terjadi transisi dari kondisi high ke kondisi low pada saat SCL berkondisi high, maka terjadilah kondisi START. Apabila pada SDA terjadi transisi dari kondisi low ke kondisi high pada saat SCL berkondisi high, naka terjadi kondisi STOP. Kondisi START dan STOP selalu dibangkitkan oleh Master, dan bus dikatak'an sibuk setelah START dan dikatakan bebas setelah STOP



Gambar 2.9. Kondisi Start dan Stop
(Sumber : Datasheet PCF8951)

2.3.5.3. ACK dan NACK

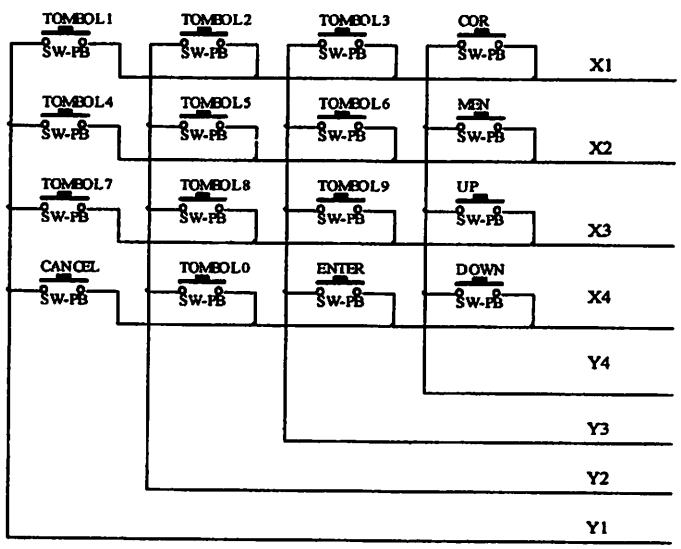
Kondisi ACK terjadi apabila receiver " menarik " SDA pada kondisi low selama satu sinyal clock. Kondisi NACK terjadi apabila receiver " membebaskan " SDA pada kondisi high selama 1 sinyal clock



Gambar 2.10. Kondisi ACK dan NACK
(Sumber : Datasheet PCF8951)

2.4. Keypad

Keypad merupakan komponen yang digunakan sebagai sarana untuk memasukkan data ke komputer atau minimum sistem. Untuk rangkaian *keypad* menggunakan keypad 3 x 4 yaitu 12 buah saklar tekan (*push button*) yang dirangkai dalam bentuk matrik. Gambar rangkaian keypad ditunjukkan pada gambar berikut :



Gambar 2.11. Keypad Matrik 4 x 4

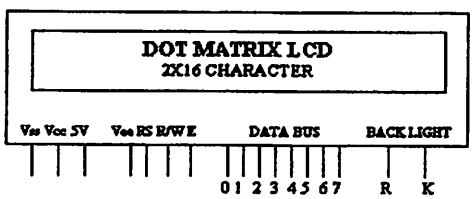
2.5. LCD (Liquid Cristal Display)

Liquid Cristal Display adalah modul tampilan yang mempunyi konsumsi daya yang relatif rendah dan terdapat sebuah kontroler CMOS didalamnya. Kontroler tersebut berfungsi sebagai pembangkit ROM / RAM dan display data RAM. Semua fungsi tampilan dikontrol oleh suatu instruksi, modul LCD dapat dengan mudah diinterfacekan dengan MPU.

LCD yang digunakan dalam Tugas Akhir ini adalah LCD yang memiliki kemampuan sebagai berikut :

1. Meliputi 32 karakter yang dibagi menjadi 2 baris dengan *display dot matric* 5 x 7 ditambah *cursor.*
2. Karakter generator ROM dengan 192 karakter.
3. Karakter generator RAM dengan 8 tipe karakter.
4. Dilengkapi fungsi tambahan yaitu *display clear, cursor home, display ON/OFF, cursor ON / OFF, displat character blink, cursor shift* dan *display shift.*
5. Internal data.
6. 80 x 8 bit display data RAM.
7. Dapat diinterfacekan dengan MPU 8 atau 4 bit.
8. Internal otomatis dan *reset* pada *power ON.*
9. + 5 Volt *power supply* tunggal.

Gambar dibawah ini menunjukkan LCD beserta pin – pinnya :



Gambar 2.12. Bentuk Fisik dari LCD
(Sumber : Seiko Instruments Inc.,LCD Module M1632 User Manual)

2.5.1. Instruksi Operasi

2.5.1.1. Operasi Dasar

A. *Register*

Kontroller dari LCD mempunyai dua buah register 8 bit yaitu register intruksi (IR) dan register data (DR). kedua register tersebut dipilih malalui register select (SR). IR menyimpan intruksi seperti *display clear, cursor shift,* dan *sdplay data* (DD RAM) serta *character generator* (CG RAM). DR menyimpan data untuk dituliskan ke DD RAM atau CG RAM ataupun membaca data dari DD RAM atau CG RAM.

B. Busy Flag

Busy flag menunjukkan bahwa modul siap untuk menerima intruksi selanjutnya.sebagai mana terlihat pada table register seleksi sinyal akan melalui DB.7, jika RS=0 dan R/W=1 maka modul siap melakukan kerja internal dan intruksi tidak dapat diterima. Oleh karena itu status dari *flag* harus diperiksa sebelum melakukan intruksi selanjutnya.

C. Addres Counter

AC melalui lokasi dalam modul LCD. Pemilihan lokasi alamat itu diberikan lewat *register intruksi* (IR). Ketika data pada A, maka data secara otomatis menaikkan atau menurunkan alamat tergantung dari Entry Mode Set.

D. *Display Data RAM (DD RAM)*

Pada LCD masing-masing line memiliki range alamat tersendiri. Alamt tersebutdiekspresikan dengan bilangan Hexadesimal. Untuk line 1 range alamat berkisar antara 00H-0FH sedangkan untuk line 2 range alamat berkisar antara 40H-4FH.

E. *Character Generator ROM (CGROM)*

CG ROM mempunyai tipe dot matrik 5 x 7, dimana pada LCD telah tersedia ROM sebagai pembangkit karakter dalam kode ASCII. CG ROM dipakai untuk pembutan karakter tersendiri melalui program.

2.5.1.2. Fungsi-Fungsi Terminal

Pada tabel dibawah ini ditunjukkan fungsi dari terminal pada LCD:

Tabel 2.7. Fungsi – Fungsi Terminal Pada LCD

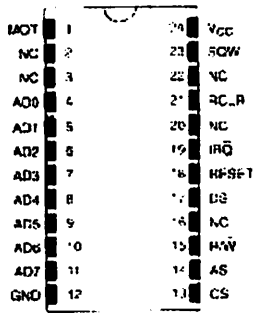
Nama pin	Jumlah	I/O	Tujuan	Fungsi
DB0 – DB3	4	I/O	MPU	Tristate bidirectional lower 4 data bus : data dibaca dari modul ke MPU ditulis ke modul melalui bus.
DB4 – DB7	4	I/O	MPU	Tristate bidirectional upper 4 data bus : data dibaca dari modul ke MPU atau dari MPU ditulis ke modul melaui bus.
E	1	Input	MPU	Sinyal operasi dimulai : sinyal aktif baca/tulis.
R/W	1	Input	MPU	Sinyal pilih data dan tulis (0 : tulis; 1 : baca).

RS	1	-	Power Supply	Sinyal pilih register : 0 : Instruction register (write) busy flag dan address counter (read) 1 : Data register (write dan read)
V_{LC}	1	-	Power Supply	Penyetelan kontras pada tampilan LCD
V_{DD}	1	-	Power Supply	+ 5 Volt
V_{SS}	1	-	Power Supply	Ground 0 Volt
V_{BL} -	1	-	-	Ground untuk lampu (back light)
V_{BL} +	1	-	-	+ 5 Volt untuk lampu (back light)

(Sumber : Seiko Instruments Inc.,LCD Module M1632 User Manual)

2.6. Real Time Click DS 12C887

RTC DC 12C887 adalah IC yang berfungsi sebagai sebuah rangkaian jam digital yang tetap bekerja selama 10 tahun walaupun power supply tidak diaktifkan. Terdiri atas 14 buah register yang terdiri dari 4 buah Register Kontrol dan 10 buah Register Data. Register Data sendiri terpisah menjadi register waktu dan Register Alarm. Setelah Register-register Kontrol diinisial, maka data waktu ataupun alarm dapat dilihat atau diatur dengan cara mengakses register-register data tersebut.



Gambar 2.13. Konfigurasi IC RTC DS 12C887
(Sumber : Datasheet IC RTC DS 12C887)

Keistimewaan IC DS 12C887 antara lain adalah ;

1. Osilator internal dan *time base* internal
2. Menghitung detik, menit, jam, dalam sehari-hari.
3. Menghitung hari dalam setiap minggu, tanggal, bulan, tahun.
4. Seratus tahun kalender.
5. Menpunyai catu daya *back up*
6. Dapat beroperasi selama lebih dari 10 tahun tanpa kehadiran catu daya eksternal.
7. RAM internal sebesar 64 byte, terdiri atas 14 byte untuk *clock* dan register control, sedangkan 50 byte lainnya dapat digunakan oleh pemakai.

Secara keseluruhan fungsi pin-pin RTC DS 12C887 adalah sebagai berikut

1. GND dan Vcc

   Merupakan pin catu daya dimana Vcc dihubungkan pada catu daya 5 Volt dan GND pada ground.

2. MOT (*Motel*)

   Digunakan sebagai saklar pemilih mode diagram pewaktu. Apabila dihubungkan pada Vcc berarti system diagram pewaktu Motorola yang dipakai, jika dihubungkan dengan GND berarti system diagram pewaktu Intel yang dipakai.

3. SQW (*Square Wave Output*)

   Merupakan pin yang dipilih untuk mengeluarkan satu dari 13 frequensi keluaran yang tersedia. Besar frequensi keluaran SQW dapat diubah dengan diprogram pada register A. Untuk mengaktifkan atau menonaktifkan sinyal SQW dipilih lewat bit SQWE pada register B.

4. AD0-AD7 (*Multiplexed Strobe Address / Data Bus*)

   Merupkan bus alamat / data dua arah yang termutiplekS. Pengiriman data maupun alamat dari maupun ke RTC dilakukan melalui bus ini.

5. AS (*Address StrobeInput*)

   Merupakan basukan bagi sinyal yang digunakan untuk memisahkan bus data dan bus alamat (ALE). Pada saat sinyal turun yang terjadi pada AS / ALE akan menyebabkan alamat ditahan dalam DS12887. Akan tetapi sinyal naik berikutnya yang terjadi pada AS akan meniadakan alamat tersebut tanpa memperhatikan apakah penyemat CS aktif atau tidak.

6. DS (*Data Strobe*)

   Pin DS dapat diartikan sama seperti sinyal *Output Enable* (OE) pada komponen memori. Dihubungkan sinyal RD yang berasal dari

mikrokontroller untuk melakukan proses membaca edan pada RAM internal RTC.

7. R/W (*Read / Write Input*)

   Pin R/W dapat diartikan sama seperti sinyal *Write Enable* (WE) yang biasa dipakai pada komponen memori jenis RAM digunakan untuk proses penulisan data pada RAM internal RTC.

8. CS (*Chip Select Input*)

   Merupakan masukan untuk mengaktifkan peripheral RTC. Sinyal CS ini didapat dari decoder alamat dengan alamat tertentu.

9. IRQ (*Interrupt Request Output*)

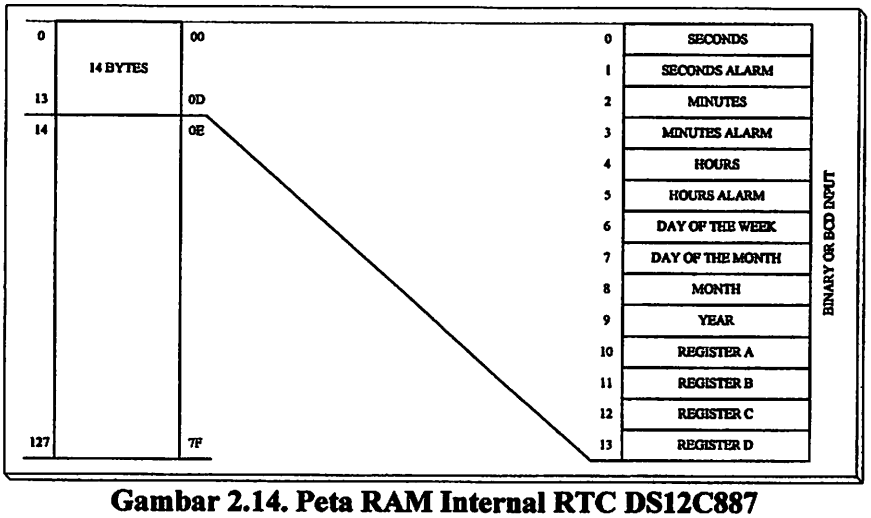
   Sinyal IRQ merupakan sinyal aktif rendah yang dapat digunakan untuk menginterupsi mikrokontroller. Keluaran IRQ tetap rendah selama status bit yang menyebabkan interupsi ada. Untuk me-*reset* IRQ, mikrokontroller memberikan program pada register C RTC. Saat tidak terdapat interupsi, penyemat ini akan dalam kondisi impedansi tinggi (*high impedance*).

10. RESET (*Reset Interupt*)

    Sinyal Reset diberikan logika rendah selama waktu yang dispesifikasikan dan tidak berpengaruh pada unjuk kerja *clock*, kalender dan fungsi RAM. Namun sinyal Reset dapat mengakibatkan beberapa *flag* direset menjadi nol.

Untuk menginisialisai RTC, yaitu men-*set* waktu yang ada di RAM RTC saat kali pertama RTC diaktifkan, digunakan sinyal WR (*write*) yang dihubungkan pada penyamat R/W, data yang diinginkan pada alamat yang bersesuaian. Sedangkan untukl membaca data dari RAM internal RTC digunakan sinyal RD (*read*) yang dihubungkan pada penyemat DS (*data strobe*). Operasi pembacaan dan penulisan pada RAM internal RTC sama seperti operasi baca dan tulis pada komponen memori jenis RAM.

RTC mempunyai RAM internal sebesar 64 byte, yang berisi data-data mengenai waktu yang sedang berjalan, seperti ; detik, menit, jam, hari, tanggal, bulan , tahun, serta beberapa register. Secara otomatis RTC akan mengganti data dalam RAM internal sesuai dengan perhitungannya. Jika diinginkan mengambil data waktu, maka dibaca pada RAM internal sesuai dengan alamat yang dimaksud. Peta alamat RAM internal RTC DS 12C887 ditunjukkan dalam gambar 2.14



Gambar 2.14. Peta RAM Internal RTC DS12C887
(Sumber :Datasheet IC RTC DS 12887)

2.7. ISD (Information Storage Deviee) 2500

Winbond ISD2500 ChipCorder menyediakan kemampuan penyimpanan pesan 60 sampai dengan 120 detik. Didalam piranti CMOS ini tersedia *oscillator, microphone amplifier, automatic gain control, antialiasing filter, smoothing filter, speaaker amplifier* dan *high density multi level storage array.*

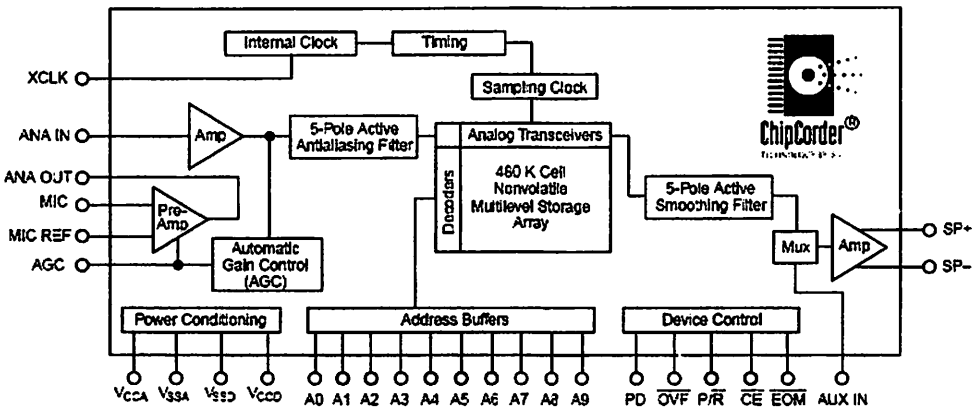
Winbond ISD2500 menyediakan frekuensi sampling pada 4.0, 5.3, 6.4, dan 8.0 KHz, yang memungkinkan pengguna untuk memilih kualitas suara. Semakin bertambah durasi penyimpanan semakin berkurang frekuensi sampling dan *bandwidth* yang akan mengakibatkan perubahan kualitas suara. Sampel suara disimpan secara langsung ke dalam sebuah chip memori non volatil tanpa digitalisasi dan kompresi seperti solusi lainnya. Sinyal suara dan audio disimpan secara langsung ke memori pada tempat naturalnya dengan kualitas suara yang bagus.

Untuk karasteristik ISD adalah sebagai berikut :

1. Chip tunggal yang mudah digunakan untuk merekam atu memainkan suara
2. Suara yang diprodukasi mempunyai kualitas yang bagus dan alami
3. Bisa dioperasikan secara manual atau menggunakan mikrokontroller
4. Memiliki durasi penyimpanan dari 60, 75, 90, 120 detik
5. Arus pada saat stanby = 1 μA
6. Tidak perlu power untuk tetap menyimpan data dalam IC, sehingga tidak perlu baterai ncadangan

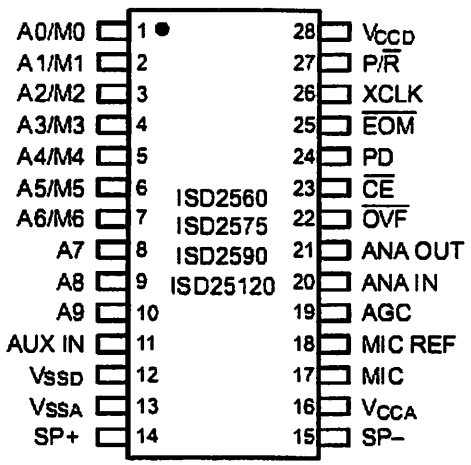
7. Data dapat bertahan hingga 100 tahun
8. 100.000 kali rekam

Adapun blok diagram seri ISD2500 dapat dilihat dalam gambar 2.15



Gambar 2.15. Blok Diagram ISD2500
(Sumber : Datasheet IC ISD2500)

Susunan pin dari ISD2500 ditunjukkkan pada gambar 2.16 dan penjelasan dari masing-masing pin adalah sebagai berikut :



Gambar 2.16. Konfigurasi Pin ISD2500
(Sumber : Datasheet IC ISD2500)

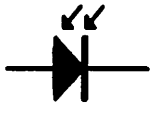
1. *Voltage input* (V_{CCA}, V_{CCD}), untuk mengurangi noise
2. *Ground Input* (V_{SSA}, V_{SSD}), pin ini harus dihubugkan dengan power supply ground dengna impedansi rendah
3. *Power Down Input* (PD), ketika sedang tidak digunakan untuk melakukan operasi *record* atau *plyback*, pin PD harus diberi logika tinggi. Ketika pulsa *overflow* rendah, PD harus berlogika tinggi untuk mereset *addresspointer* kenbali ke awal *record* atau *plyback.*
4. *Chip Enable Input* ($\overline{CE}$), berfungsi untuk mengaktifkan semua operasi *record* dan *playback.*
5. *Playback/Record Input* ($\overline{P}$ / R), $\overline{P}$ / R input ditahan dengan adanya transisi turun dari pin $\overline{CE}$. Logika tinggi akan memilih *playback cycle* dan logika rendah untuk memilih *record cycle.*
6. *End-Of-Message Run Output* ($\overline{EOM}$), sebuah alamat akan dimasukkan secara otomatis diakhir masing-masing perekaman. Pulsa output $\overline{EOM}$ akan rendah untuk setiap periode di akhir masing-masing perekaman.
7. *Microphone Input* (MIC), digunakan untuk mentransfer sinyal suara ke *onchip preamplifier.*
8. *Microphone Reference Input* (MIC REF),merupakan input pembalik ke *microphone preamplifier* yang memberikan *noise-concelling*, atau *common-mode rejection* input ke IC ketika dihubungkan ke sebuah microphone diferensial.

9. *Overflow Output* ($\overline{\text{OVF}}$), sinyal pulsa rendah pada akhir tempat memori,mengindikasikan bahwa IC ini telah terpenuhi dan pesan telah melebihi kapasitas. Keluaran ($\overline{\text{OVF}}$) kemudian diikuti masukan $\overline{\text{CE}}$ sampai pulsa PD telah mereset. Pinini juga berfungsi untuk menambah beberapa IC ISD2500 untuk menambah durasi *record/playback.*
10. *Automatic Gain Control Input* (AGC), secara dinamik mengubah penguatan dari preamplifier untuk mengimbangi dari lebar jarak dari level microphone input. AGC memberikan jarak secara penuh dari suara rendah ke tinggi untuk direkam dengan distorsi minimal.
11. *Analog Output* (ANA OUT), pin ini memberikan preamplifier output ke pengguna.
12. *Analog Input* (ANA IN), pin ini akan mentansfer sinyal kedalam chip untuk perekaman.
13. *External Clock Input* (XCLK), untuk ISD2500 mempunyai sebuah internal pulldown, frekuensi clock sampling internal kurang lebi 1% dari spesifikasi. Frekuensi ini bervariasi dari ± 2,25 % berada pada suhu kamar dan dalam *range* tegangan operasi. *Internal clock* mempunyai toleransi ± 5% pada temperatur dan tegangan kerja. Jika pin XCLK tidak digunakan, pin ini harus dihubungkan ke ground.
14. *Speaker Output* (SP+ / SP-), telah mempunyai sebuah *driver on chip differensial* speaker yang sanggup memikul beban 50mW dalam 16Ω dari AUX IN

15. *Auxiliary Input* (AUX IN), dihubungkan langsung ke kaki keluaran amplifier dan keluaran speaker ketika $\overline{CE}$, $\overline{P}$ / R berada pada logika tinggi dan *playback* tidak aktif.

2.8. Photodioda

Photodioda sejenis dengan dioda pada umumnya. Perbedaan pokok pada photodioda ini adalah dipasangnya sebuah lensa pemfokus sinar. Lensa ini berfungsi untuk memfokuskan sinar jatuh pada pertemuan pn. Konduktivitas dioda ditentukan langsung oleh cahaya yang jatuh padanya. Energi pancaran cahaya yang jatuh paha pertemuan pn menyebabkan sebuah electron berpindah ketingkat energi yang lebih tinggi. Electron berpindah ke luar dari *valensi band* meninggalkan :"*hole*" sehingga membangkitkan pasangan electron bebas dan *hole*. Arus balik akan bertambah besar bila sebuah cahaya jatuh pada pertemuan pn photodioda, dan arus balik akan menjadi sangat kecil bila pada pertemuan pn photodioda tidak terdapat cahaya yang jatuh padanya



Gambar 2.17. Lambang Photodioda

BAB III

PERENCANAAN ALAT

3.1. Pendahuluan

Dalam bab ini akan dibahas pembuatan seluruh perangkat yang ada pada alat ini. Secara umum pembahasan ini terdiri atas 2 bagian perangkat yaitu ;

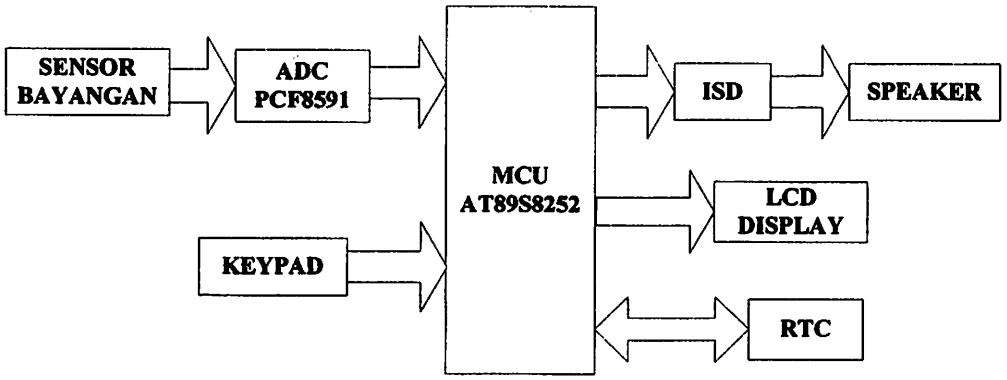
1. Perencanaan Perangkat Keras
2. Perencanaan Perangkat Lunak

Pada perencanaan perangkat keras akan meliputi penjelasan dari perancangan diagram blok system dan juga perencanaan minimum system mikrokontroller AT89S8252 beserta peripheral yang digunakan. Pada perencanaan perangkat lunak akan meliputi penjelasan dari perangkat lunak yang dugunakan pada minimum system AT89S8252. untuk selanjutnya perangkat-perangkat tersebut dalam kerjanya akan saling menunjang antara satu dengan yang lainnya.

3.2. Diagram Blok Rangkaian

Dalam tugas akhir ini, perencanaan dan pembuatan jam matahari untuk menentukan waktu sholat berbasis mikrokontroller AT89S8252 sebagai control utama dan menggunakan komponen lain sebagai komponen pendukung, diantaranya papan tombol (keypad), unit penampil (LCD), Real Time Clock (RTC DS 12887), ISD 2560, ADC PCF 8591 dan unit sensor cahaya (PHOTO

DIODA). Sebelum membuat perangkat keras terlebih dahulu direncanakan blok diagram untuk mempermudah dalam pembuatan alat. Diagram blok rangkaian dari alat ini adalah sebagai berikut;



Gambar 3.1. Blok Diagram Alat

Dari diagram blok diatas, dapat diketahui fungsi dan prinsip kerja dari masing-masing blok diantaranya ;

1. *Sensor bayangan* digunakan untuk menangkap bayangan dari subjek pembentuk bayangan ketika matahari berada tepat diatas alat
2. *ADC* digunakan untuk merubah output analog dari sensor bayangan menjadi digital.
3. *Keypad* digunakan untuk memasukkan nama daerah, jam dan tanggal
4. *LCD display* digunakan untuk menampilkan jam matahari (*istiwak*) dan awal waktu sholat.
5. *RTC* digunakan sebagai *timer.*
6. *ISD* digunakan untuk merekam suara peringatan

7. *Speaker* digunakan untuk membunyikan suara peringatan
8. Unit kontrol yang digunakan adalah IC mikrokontroller AT89S8252, dalam IC ini terdapat 8Kbytes PEROM, 256bytes RAM internal, 32 *Programmable I/O lines*, 2Kbytes EEPROM dan 3 buah *timer / counter* 16 bit.

3.3. Prinsip Kerja Alat

Pada dasarnya ada dua fungsi yang dijalankan oleh alat ini, yaitu mengatur jam sesuai dengan peredaran matahari dan pengingat masuknya waktu sholat. Untuk pengaturan jam digunakan dua buah sensor cahaya berupa dua buah photo dioda yang diletakkan di bawah benda tepatnya disisi bagian barat dan timur. Kedua sensor akan diaktifkan ketika jam menunjukkan pukul 11 siang sampai pukul 13. Ketika kedua sensor mendeteksi besar cahaya yang sama maka akan menghasilkan arus yang sama,dengan besar yang sama maka alat akan mengatur jam menjadi pukul 12. untuk selanjutnya jam akan dijalankan dengan RTC sesuai dengan hasil dari pengaturan tersebut.

Sedangkan untuk fungsi pengingat masuknya waktu sholat digunakan ISD yang akan memberikan peringatan ketika masuk waktu sholat. Adapun suara peringatan yang digunakan berupa suara manusia yang memberikan keterangan mengenai waktu sholat dan bukan suara adzan, untuk memudahkan bagi tuna netra dalam membedakan antara waktu sholat yang satu dengan yang lainnya

3.4. Perancangan Perangkat Keras (Hardware)

Dalam Skripsi ini, perancangan dan pembuatan jam matahari untuk menentukan waktu sholat berbasis mikrokontroller AT89S8252 sebagai pengontrol utama, dan menggunakan komponen-komponen lain sebagai komponen pendukungnya.

3.4.1. Perencanaan Rangkaian Mikrokontroller AT89S8252

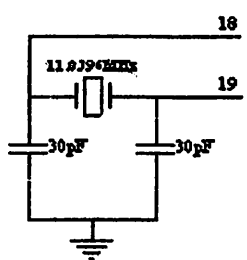
3.4.1.1. Perencanaan Rangkaian Clock

Mikrokontroller AT89S8252 ini memiliki rangkaian *internal clock* generator yang berfungsi sebagai sumber *clock*, tetapi masih diperlukan rangkaian tambahan untuk membangkitkan *clock* yang diperlukan.

Rangkaian ini terdiri dari dua buah kapasitor dan sebuah kristal, dengan ketentuan sebagai berikut:

- 6 – 14 MHz untuk besarnya nilai kristal.
- 27 – 33 pf untuk besarnya nilai kapasitor.

Gambar dari rangkaian clock adalah sebagai berikut:

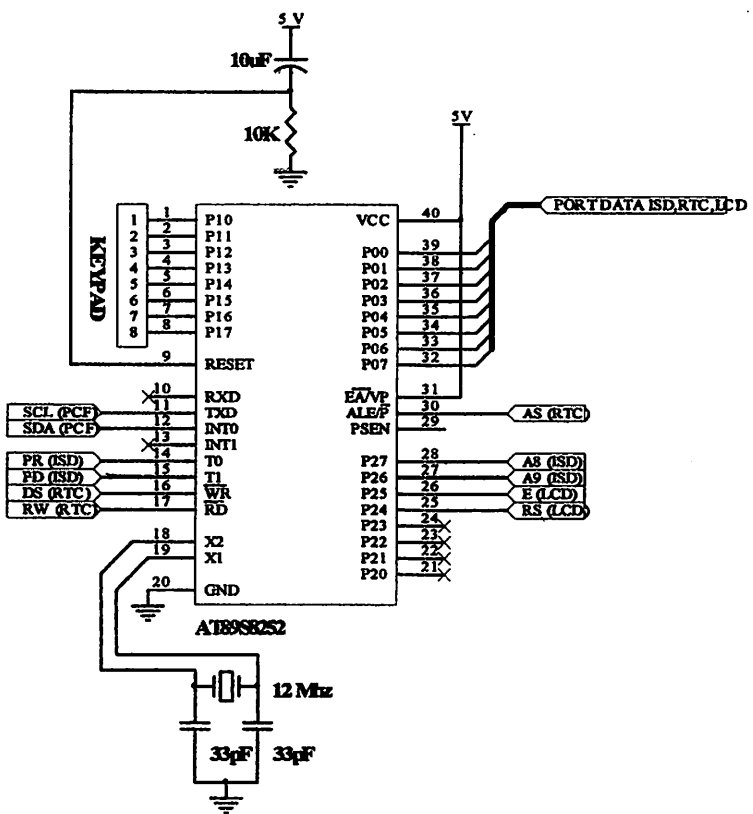


Gambar 3.2. Rangkaian Clock AT89S8252

3.4.1.2. Perencanaan Penggunaan Port Pada Mikrokontroller AT89S8252

Mikrokontroller AT89S8252 merupakan pengembangan dari mikrokontroller standart MCS-51, yang mana mikrokontroller AT89S8252 memiliki beberapa kelebihan dibandingkan dari mikrokontroller MCS-51.

Terlihat bahwa mikrokontroller AT89S8252 memiliki banyak fitur yang menguntungkan. Dipakainya *downloadable flash* memori memungkinkan mikrokontroller ini bekerja sendiri tanpa diperlukan tambahan chip lainya. Sementara *flash* memorinya mampu diprogram hingga seribu kali. Hal ini yang menguntungkan adalah sistem pemrograman jadi lebih sederhana dan tidak memerlukan rangkaian yang rumit.



Gambar 3.3. Rancangan Penggunaan Port-Port AT89S8252

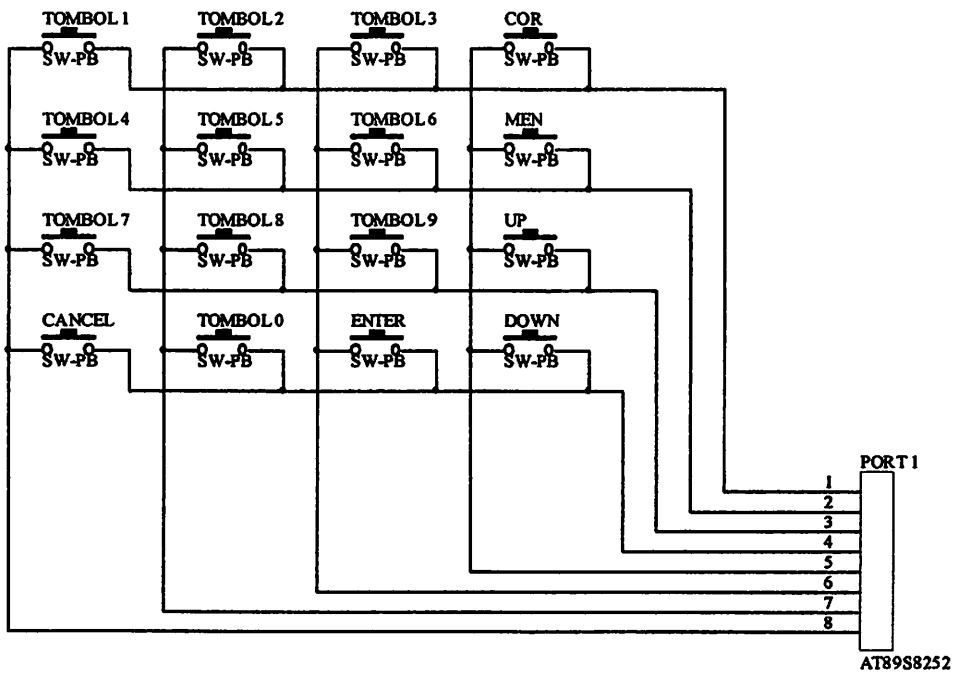
Penjelasan dari pin-pin yang dipergunakan:

1. Pin 1 sampai 8 dihubungkan dengan keypad 4x4.
2. Pin 9 sebagai reset.
3. Pin 11 dihubungkan dengan SCL pada PCF8591
4. Pin 12 dihubungkan dengan SDA pada PCF8591
5. Pin 14 dihubungkan dengan PR pada ISD2560.
6. Pin 15 dihubungkan dengan PD pada ISD2560.
7. Pin 16 dihubungkan dengan DS pada RTC DS12C887.
8. Pin 17 dihubungkan dengan RW pada RTC DS12C887
9. Pin 18 dan 19 dihubungka dengan Kristal 12 MHz.
10. Pin 24 dihubungkan dengan RS pada LCD.
11. Pin 25 dihubungkan dengan E pada LCD.
12. Pin 26 dihubungkan dengan A9 pada ISD2560
13. Pin 27 dihubungkan dengan A8 pada ISD2560
14. Pin 30 dihubungkan dengan AS pada RTC DS12C887
15. Pin 31 dihubungkan dengan sumber tegangan 5 Volt.
16. Pin 32 sampai 39 dihubungkan ke 8 bit data untuk ISD, RTC, dan LCD.
17. Pin 40 dihubungkan dengan Vcc.

3.4.2. Perencanaan Rangkaian Keypad

Keypad digunakan sebagai masukan data referensi dan mengubah data yang diinginkan. Data tersebut dirubah dalam bentuk kode biner oleh rangkaian keypad. Keypad yang dipakai yaitu berukuran 4x4 (4 bagian kolom dan 4 bagian

baris) yang terdiri dari saklar angka 0 sampai 9 sebagai masukan data dan karakter Enter,Cancel, Up, Down, Cord an Men

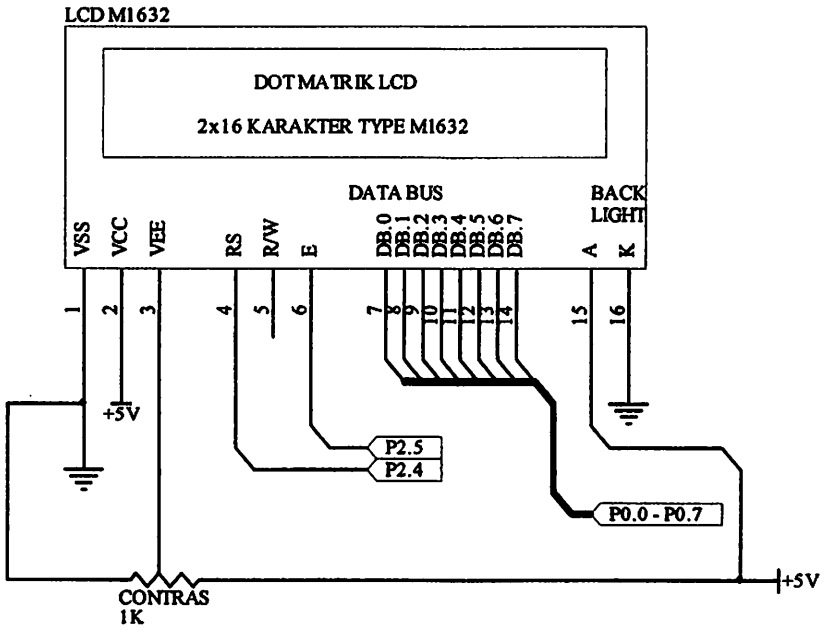


Gambar 3.4. Rangkaian Keypad

3.4.3. Perencanaan Rangkaian LCD

Untuk tampilan dipergunakan LCD Dot Matrik 2 x 16 karakter. Sinyal-sinyal yang diperlukan oleh LCD adalah *RS dan Enable, sinyal RS dan Enable* dipergunakan sebagai *input* yang outputnya dipakai untuk mengaktifkan LCD. LCD akan aktif apabila mikrokontroller memberikan instruksi tulis pada alamat LCD. Saat kondisi *RS don't care dan Enable "0"*, maka LCD tetap pada kondisi semula, pengiriman data ke LCD dilakukan saat RS berlogika "0" dan Enable

berlogika "1". Instruksi dikirim pada LCD bila keadaan RS "1" dan Enable "1". Gambar rangkaian LCD ditunjukkan pada gambar sebagai berikut :



Gambar 3.5. Rangkaian LCD

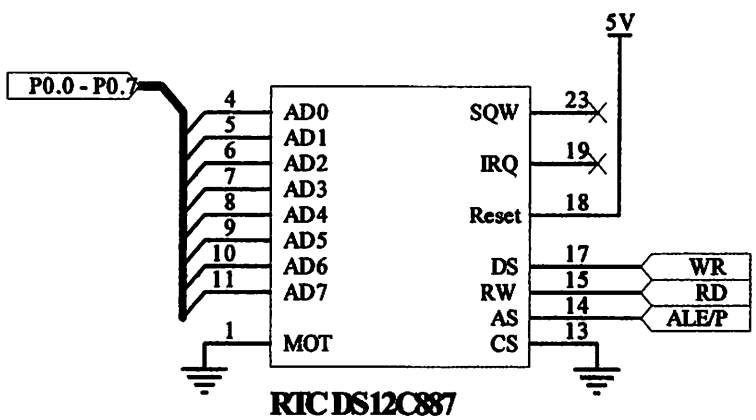
3.4.4. Perencanaan Rangkaian RTC (*Real Time Clock*)

RTC DS 12CF887A ini mempunyai RAM internal sebesar 128 byte yang terdiri atas 14 byte untuk pewktuan dan 114 bytes untuk data yang bisa diprogram oleh pemakai. Hubungan penyamat untuk RTC DS 12C887A, antara lain :

1. Port AD.0-AD.7 merupakan port data dan dihubungkan dengan port 0.0-0.7 mikrokontrol AT89S8252
2. AS dihubungkan dengan ALE mikrokontroller yang berfungsi untuk memisahkan saluran data dan saluran alamat yang termultipleks pada saluran AD.0-AD.7

3. R/W dihubungkan dengan port 3.7 (RD) mikrokontroller yang berfungsi sebagai control untuk penulisan data pada EEPROM
4. DS dihubungkan dengan port 3.6 (WR) mikrokontroller yang berfungsi sebagai control untuk pembacaan data pada EEPROM
5. MOT dihubungkan ke ground untuk mendapatkan sitem pewaktuan bus intel.
6. RESET dihubungkan dengan sumber tegangan 5 V

Operasi pembacaan dan penulisan pada RTC DS 12C887A ini sama dengan operasi baca tulis pada EEPROM. Alamat rangkaian RTC pada system ini adalah 8000h – 803Fh. Rangakaian RTC ditunjukkan dalam gambar



Gambar 3.6. Rangkaian RTC DS 12C887

3.4.5. Perencanaan Rangkaian ADC PCF8591

Dalam pembuatan alat ini juga dibutuhkan pengubah sinyal analog menjadi sinyal digital atau disebut *Analog to Digital Converter* (ADC), hal ini

disebabkan karena sinyal-sinyal yang didapat dari sensor bayangan adalah berupa sinyal analog sedangkan rangkaian kontrolnya menggunakan sistem digital sehingga membutuhkan input berupa sinyal digital. Jenis ADC yang digunakan adalah PCF8591 yang merubah analog ke digital dengan mengambil masukan analog melalui AIN0 dan AIN1 yang mencupliknya, kemudian mengubah ampitudo dari setiap cuplikan menjadi sandi digital. Keluarannya melalui kaki 9 (SDA) dan kaki 10 (SCL) adalah sejumlah bit-bit digital serial yang status logikanya menunjukkan amplitudo dari setiap cuplikan. Tegangan yang keluar dari sensor bayangan merupakan tegangan analog sehingga akan di konversikan oleh ADC menjadi data digital yang dibaca oleh *mikrokontroller* dan tergantung juga terhadap jumlah bit dari ADC yang digunakan. Resolusi ADC mengacu pada jumlah bit keluarannya, semakin banyak biy keluaran maka semakin kecil nilai resolusi yang dihasilkan. Factor yang terpenting dalam konversi adalah resolusi, kecepatan konversi dan pewaktuan. Resolusi yang tinggi di dapat dari tegangan output maksimal (tegangan referensi) di bagi dua pangkat n dikurangi 1, dimana n sama dengan jumlah bit, dengan rumus sebagai berikut:

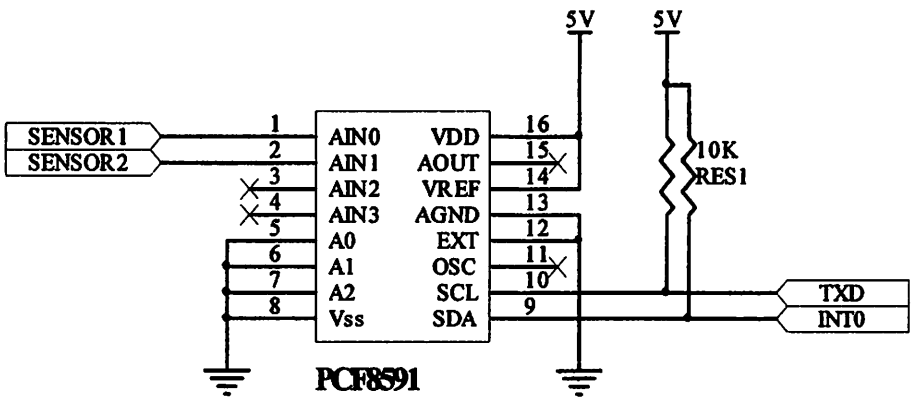
$$Resolusi = \frac{V\ max}{Step\ \max ADC}$$

$$Resolusi = \frac{2,5}{2^8 - 1}$$

$$Resolusi = \frac{2,5}{256 - 1} = \frac{2,5}{255}$$

$$Resolusi = 0.0980392 = 9.8\ mV/Step$$

Jadi bila ada kenaikan tegangan masuk sebesar 9,8 mV, maka terjadi perubahan nilai biner 1. Berikut adalah gambar rangkaian ADC PCF8591



Gambar 3.7. Rangkaian ADC PCF8591

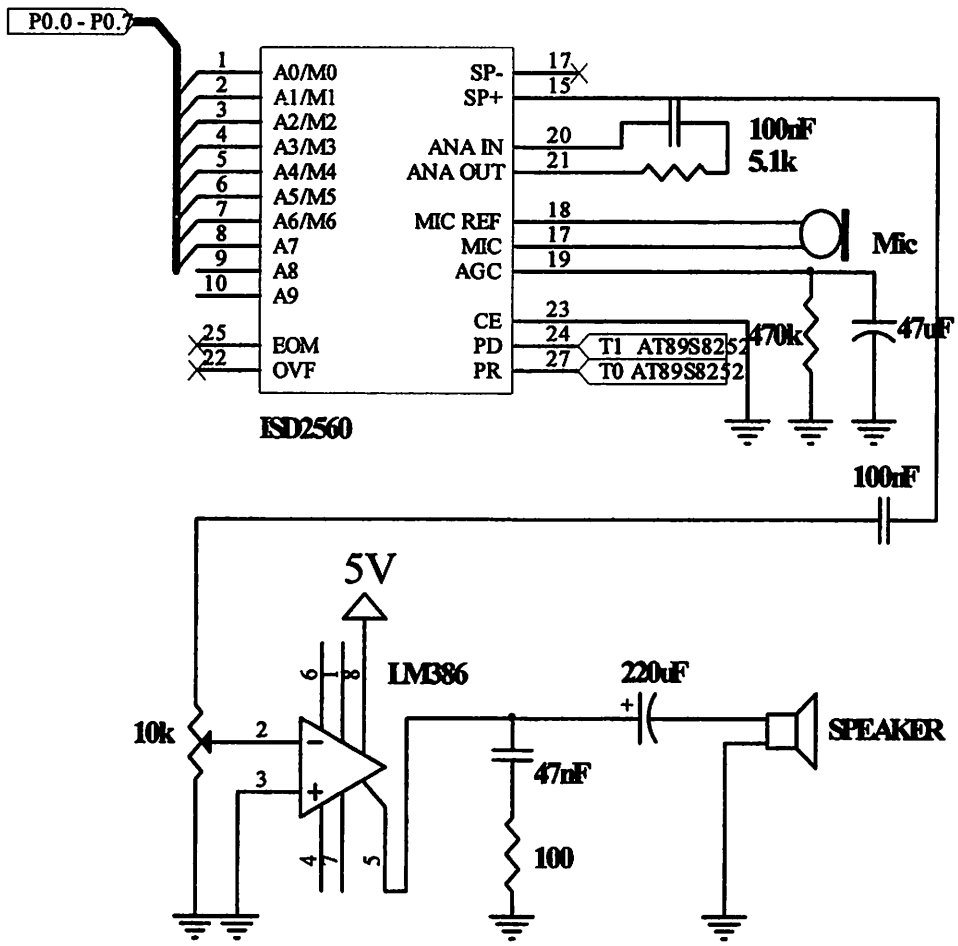
Penjelasan dari gambar diatas :

- AIN 0 (pin1) merupakan inputan yang berupa sinyal analog dari sensor bayangan 1 dan AIN 1 (pin2) merupakan inputan yang berupa sinyal analog yang berasal dari sensor bayangan 2.
- SDA (Serial Data Line) merupakan jalur pengiriman dan penerimaan data bit dihubungkan dengan port 3.2 yang merupakan INT0 AT89S8252
- SCL (Serial Clock Line) merupakan jalur pengiriman dan penerimaan sinyal clock dihubungkan dengan port 3.1 yang mnerupakan port serial AT89S8252
- VDD dan VREF dihubungkan dengan sumber tegangan

3.4.6. Perencanaan Rangkaian ISD 2560

Pada perencanaan dan pembuatan alat ini, suara yang direkam menggunakan *voice processor* ISD 2560. Berdasarkan datasheet ISD 2560

mampu merekam suara dengan lama perekaman 60 detik denan sample rate 8.0 KHz. Demikian pula waktu putar ulangnya juga selama 60 detik. Suara yang direkam dan diputar kembali diantaranya adalah suara peringatan waktu sholat. Perancangan rangkaian dari ISD 2560 dapat dilihat pada gambar berikut :



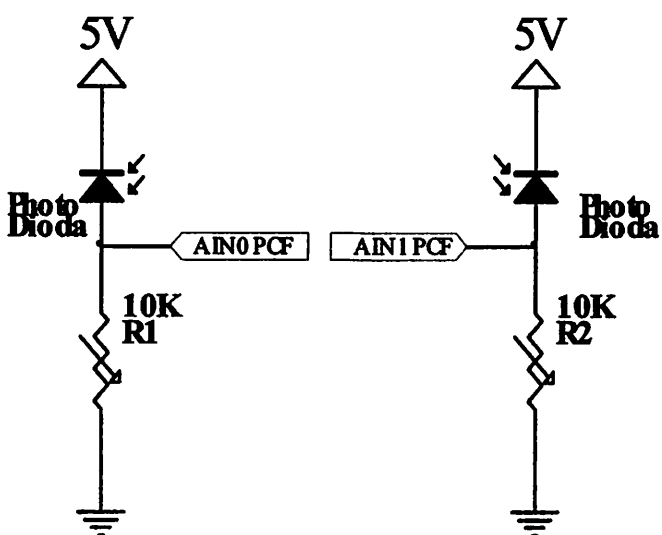
Gambar 3.8. Rangkaian ISD 2560

Penjelasan dari gambar diatas :

- Port A0 – A6 merupakan port data dan dihubungkan dengan port 0.0 – 0.7 mikrokontroller AT89S8252
- Port SP+ merupakan output suara dan dihubungkan dengan speaker
- Port MIC dan MIC REF dihubungkan dengan mikrofon sebagai inputan suara
- Port PD dihubungkan dengan T1 dan PR dihubungkan dengan T0 yang berfongsi sebagai kontol dari ISD 2560

3.4.7. Perencanaan Rangkaian Sensor

Disini digunakan dua buah sensor PHOTO DIODA untuk mengetahui bahwa matahari berada pada titik kulminasi. Dua buah sensor PHOTO DIODA tersebut diletakkan dibawah objek benda



Gambar 3.9. Rangkaian Sensor

Semakin kuat cahaya yang jatuh pada sensor maka resistansi pada sensor photodioda akan semakin kecil dan semakin lemah cahaya yang jatuh pada sensor photodioda maka resistansi akan semakin besar. Kita dapat mengetahui besar besarnya tegangan yang keluar dari rangkaian ini dengan rumus sebagai berikut:

$$Vout = \frac{R}{R\ sensor + R} \times V_{in}$$

Perencanaan sensor ini digunakan untuk dua kondisi yang berbeda yaitu ketika alat diuji dengan sinar matahari dan dengan cahaya lampu supaya alat bisa berjalan dengan baik. Untuk cahaya lampu digunakan R sama dengan 10 KΩ sedangkan untuk cahaya matahari digunakan R sama dengan 1 KΩ. Hal tersebut dilakukan untuk merubah kepekaan dari sensor.

Untuk mencapai hasil yang maksimal, perlu perhitungan rangkaian sensor dalam berbagai kondisi diantaranya:

1. Ketika kondisi gelap, Rsensor = 140 KΩ

$$Vo = \frac{10 \cdot 10^3}{140 \cdot 10^3 + 10 \cdot 10^3} \times 5$$
$$Vo = 0{,}33\ Volt$$

2. Ketika sensor terkena bayangan dari lampu 40 watt, R sensor = 8,2 KΩ

$$Vo = \frac{10 \cdot 10^3}{8{,}2 \cdot 10^3 + 10 \cdot 10^3} \times 5$$
$$Vo = 2{,}75\ Volt$$

3. Ketika terkena cahaya lampu 40 watt, R sensor = 2,6 KΩ

$$Vo = \frac{10 \cdot 10^3}{2{,}6 \cdot 10^3 + 10 \cdot 10^3} \times 5$$
$$Vo = 3{,}97\ Volt$$

4. Ketika sensor terkena bayangan dari matahari, R sensor = 344 Ω

$$Vo = \frac{10^3}{344 + 10^3} \times 5$$
$$Vo = 3{,}72\ Volt$$

5. Ketika terkena cahaya matahari, R sensor = 56 Ω

$$Vo = \frac{10^3}{56 + 10^3} \times 5$$
$$Vo = 4{,}74\ Volt$$

Dari data diatas diperoleh hasil perhitungan sebagai berikut

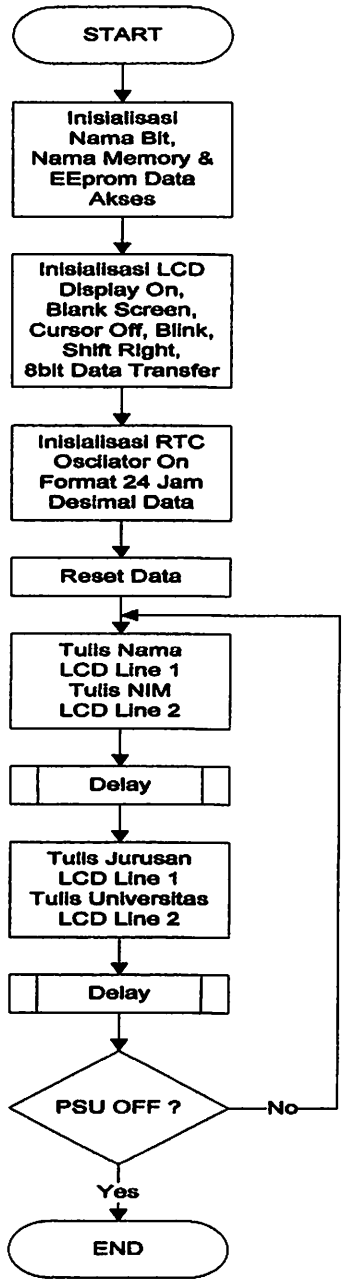
Tabel 3.1. Hasil Perhitungan Rangkaian Sensor Photodioda

NO	DATA			Vo
	R (KΩ)	R sensor (Ω)	Vi (Volt)	(Volt)
1	10	140 K	5	0,33
2	10	8,2 K	5	2,75
3	10	2,6 K	5	3,97
4	1	334	5	3,72
5	1	56	5	4,74

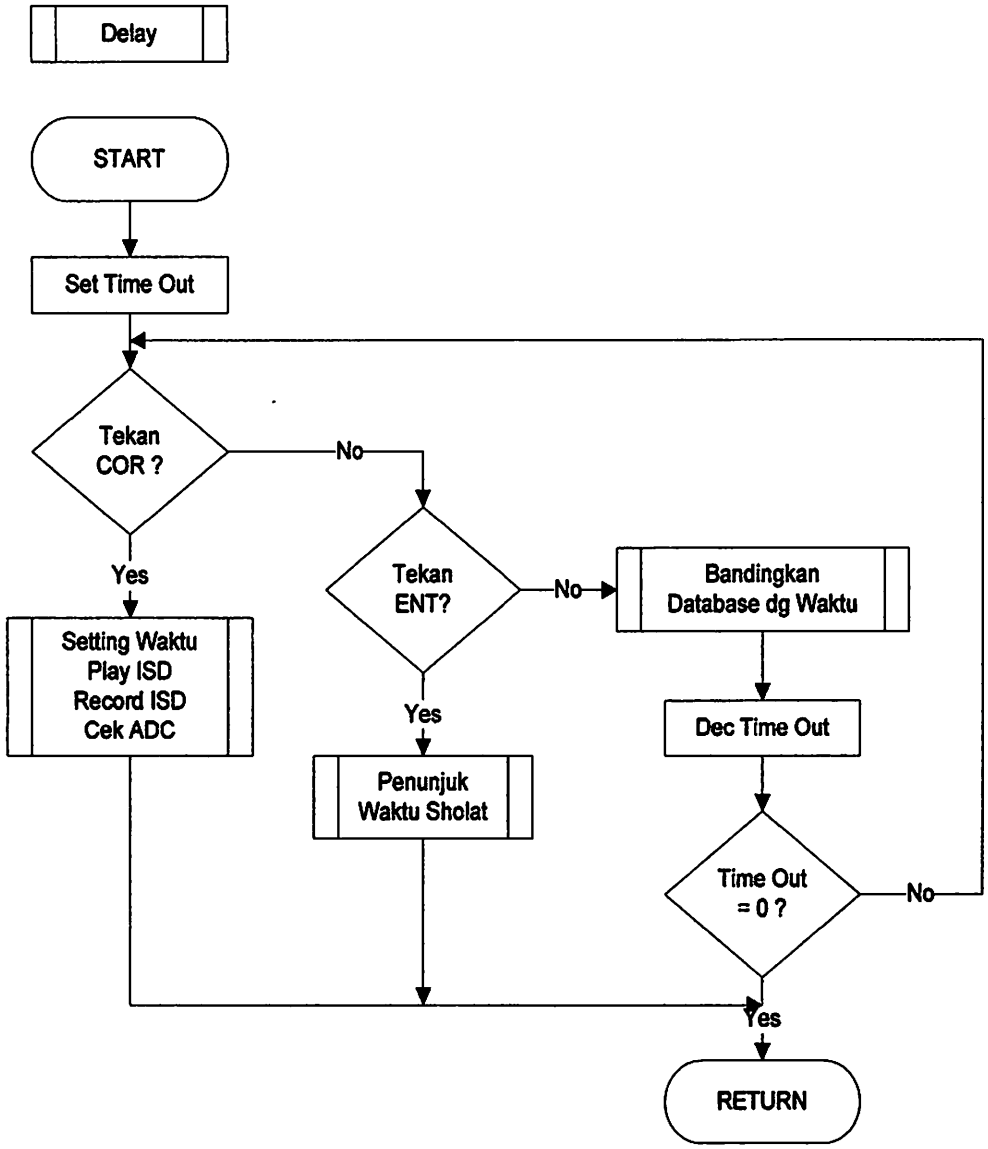
3.5. Perancangan Perangkat Lunak (*Software*)

Untuk pemakaian mikrokontroler didalam suatu sistem, perlu direncanakan perangkat lunak mikrokontroller yang dapat mengatur sistem tersebut. Perangkat lunak disini adalah perintah-perintah (program) didalam memori yang harus dilaksanakan oleh mikrokontroler.

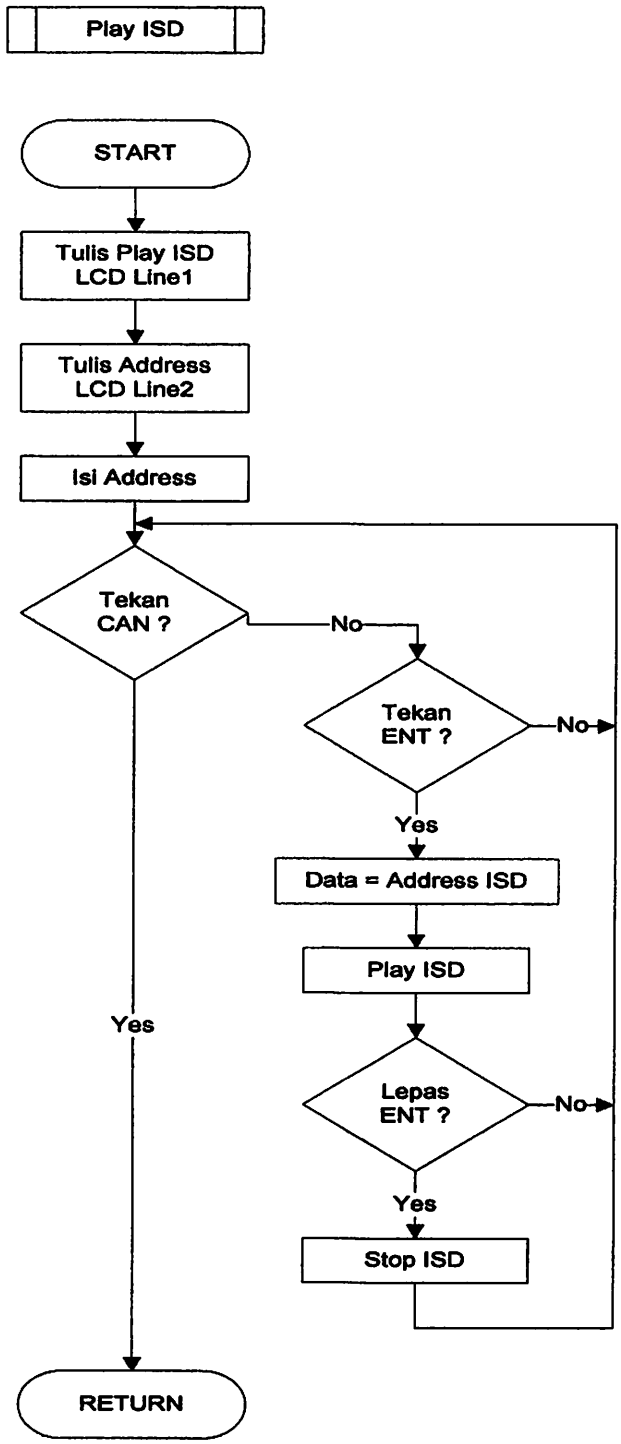
Perencanaan perangkat keras didasarkan perencanaan perangkat lunak *(software)* yang telah dibuat sebelumnya. Cara kerja dari perangkat lunak *(software)* secara umum adalah sebagai berikut



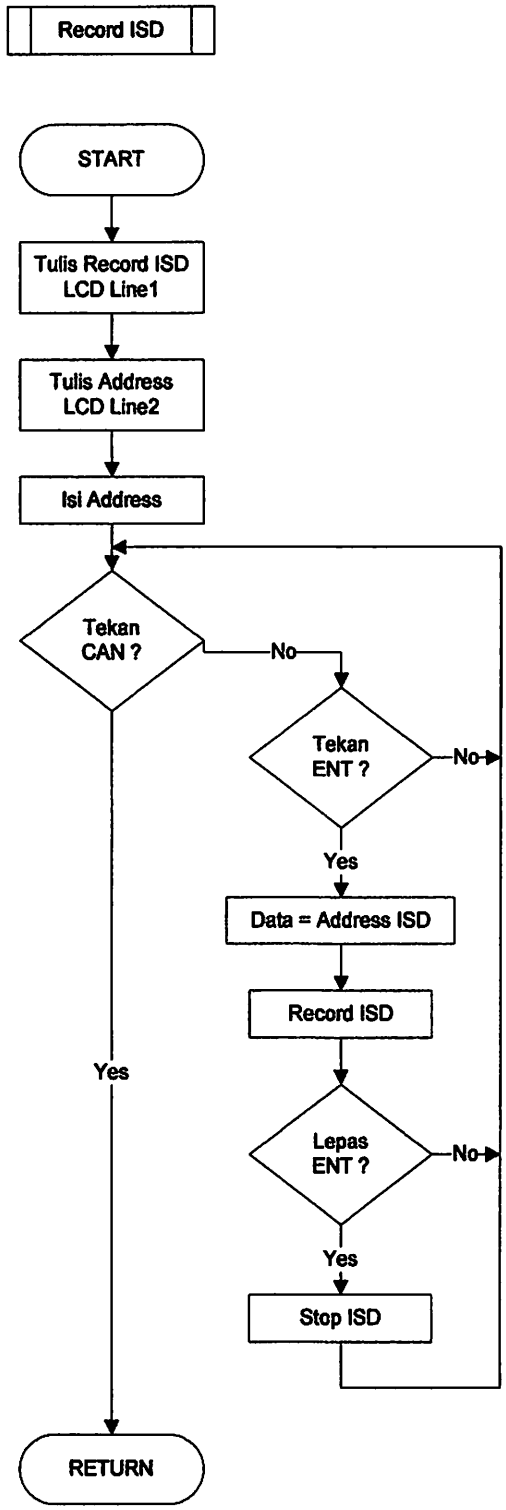
Gambar 3.10. Flowchart Program Utama



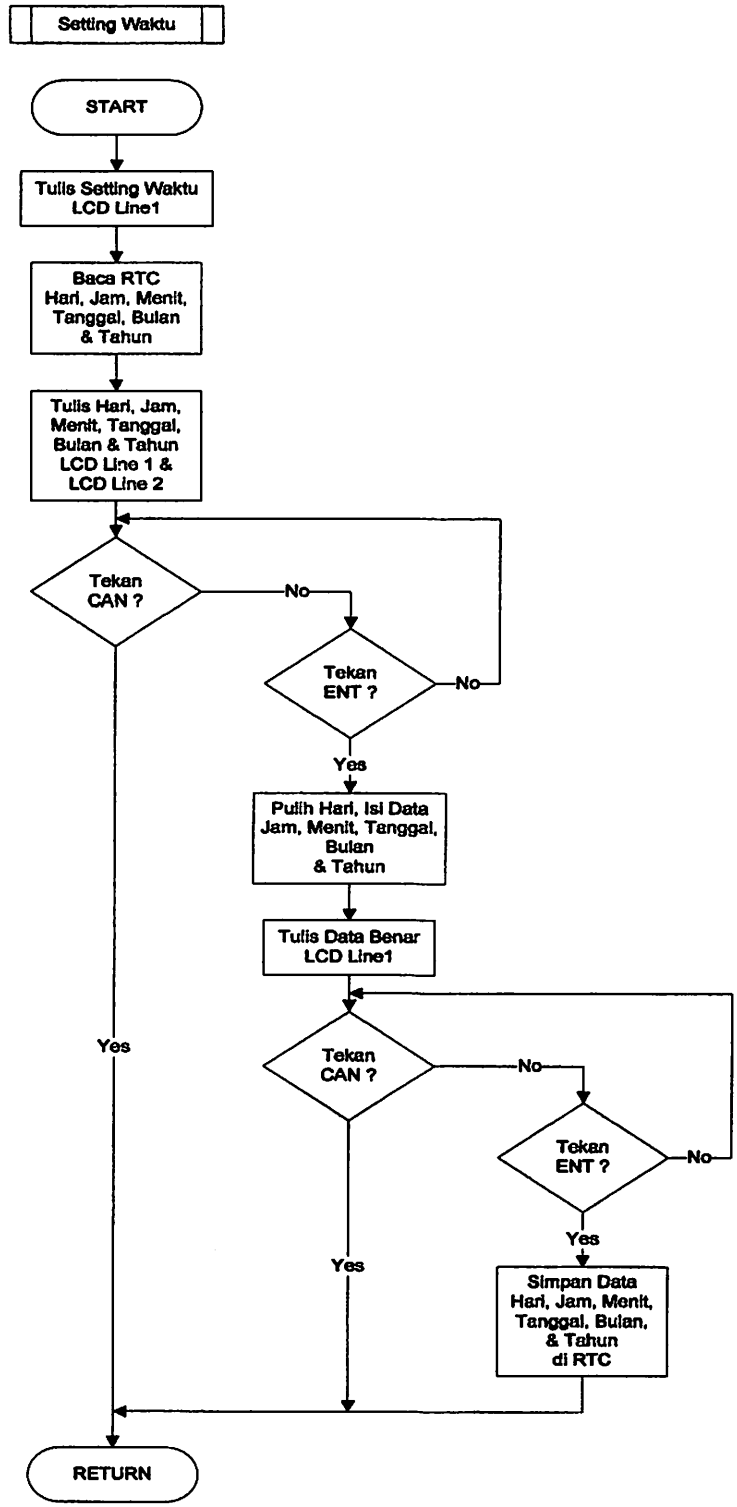
Gambar 3.11. Flowchart Delay



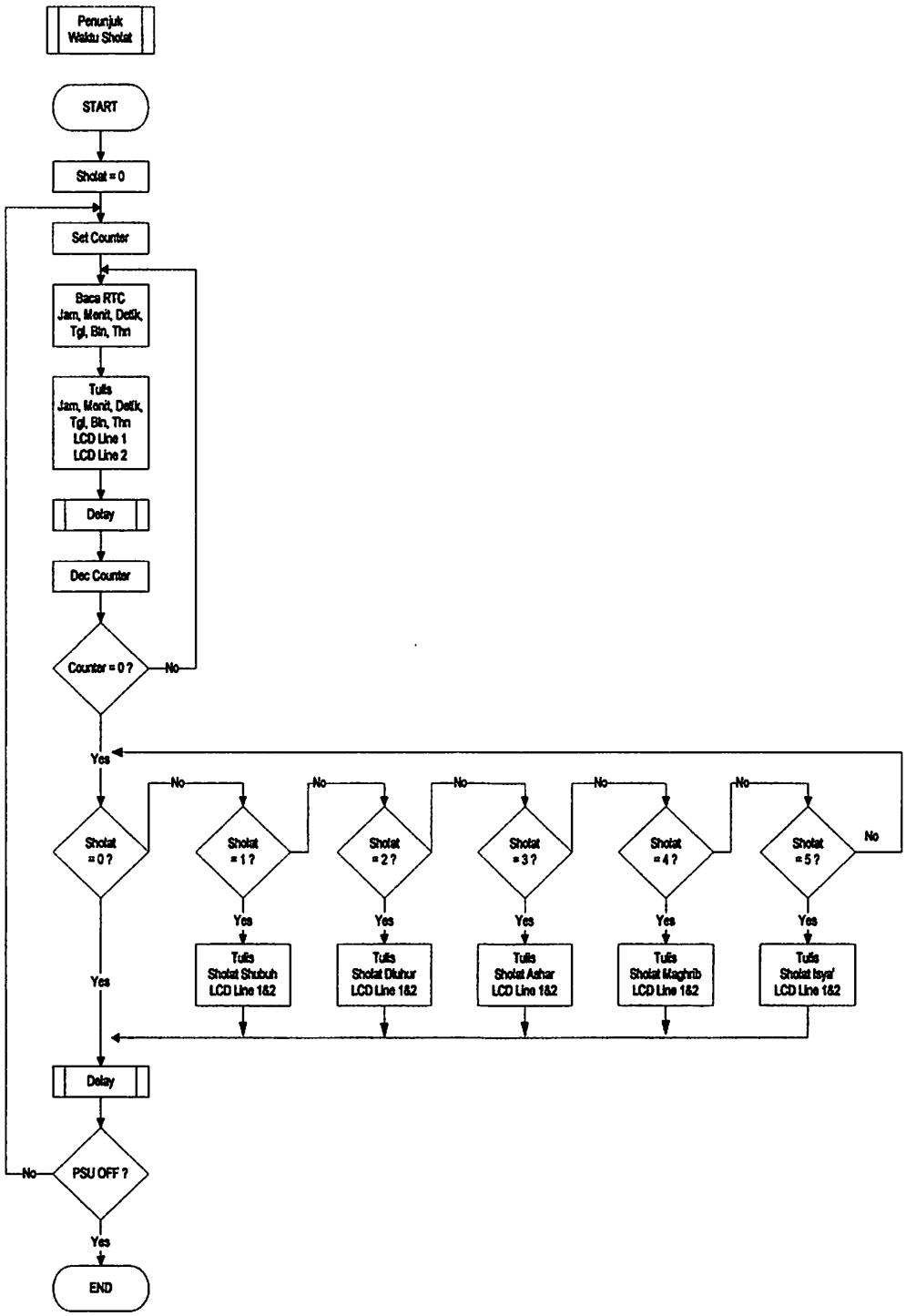
Gambar 3.12. Flowchart Mendengarkan ISD



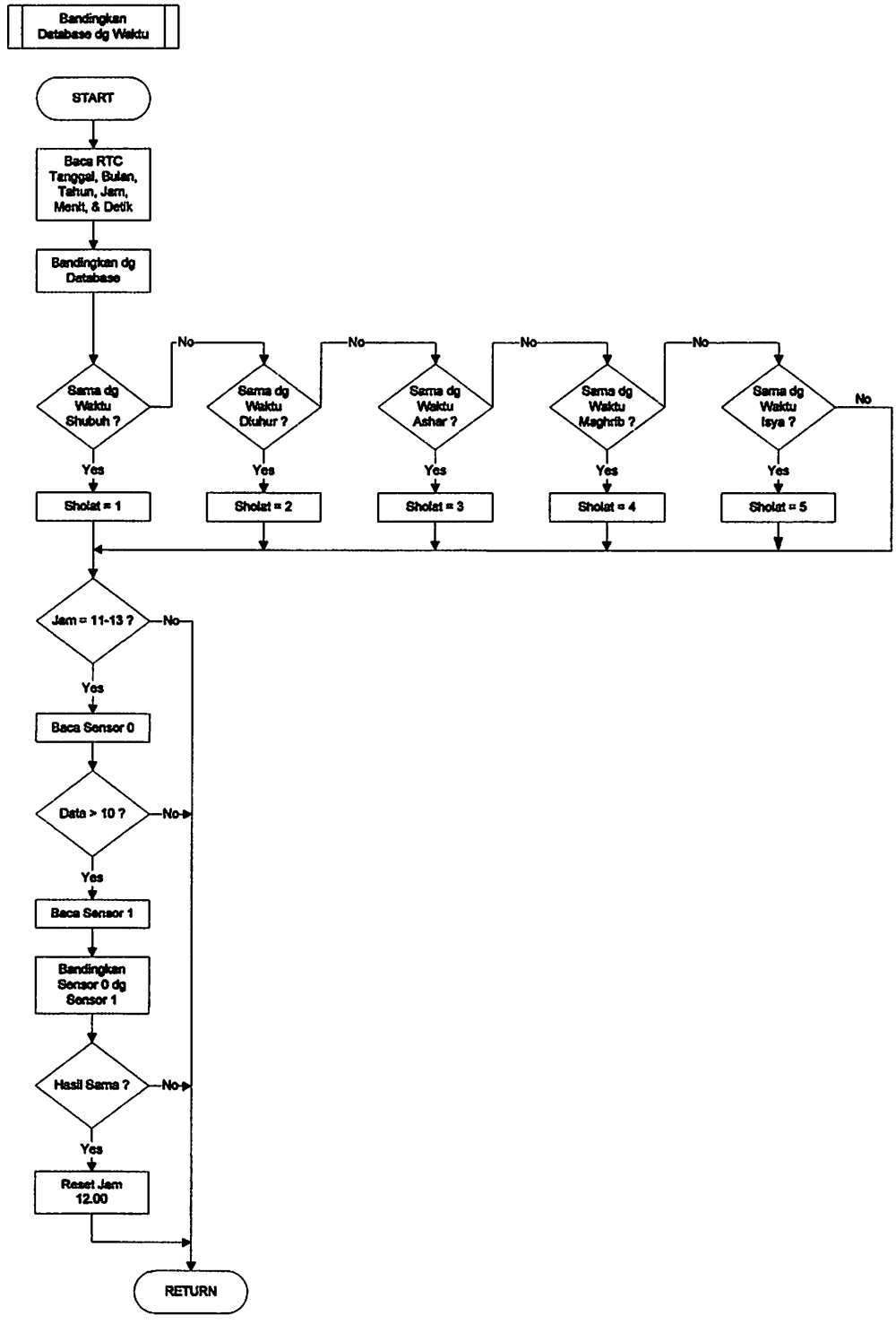
Gambar 3.13. Flowchart Merekam ISD



Gambar 3.14. Flowchart Setting Waktu



Gambar 3.15. Flowchart Penunjuk Waktu Sholat



Gambar 3.16. Flowchart Perbandingan Database dengan Waktu

BAB IV

PENGUJIAN ALAT

Untuk mendapatkann hasil yang maksimal setelah melaksanakan perencanaan dan pembuatab alat, maka perlu dilakukan suatu pengujian terhadap alat yang telah kita buat. Pengujian ini bertujuan untuk mengetahui apakah alat yang telah dibuat dapat bekerja sesuai dengan perencanaan.

Bagian yang akan di uji dari peralatan ini adalah :

1. Pengujian ADC
2. Pengujian RTC
3. Pengujian ISD
4. Pengujian Keseluruhan Sistem

4.1. Pengujian Perangkat Keras

4.1.1. Pengujian RTC

1. Tujuan.

Untuk mengetahui apakah RTC dapat bekerja dengan baik sesuai dengan fungsinya dan dapat dibaca serta direset oleh mikrokontroller sesuai dengan apa yang telah direncanakan.

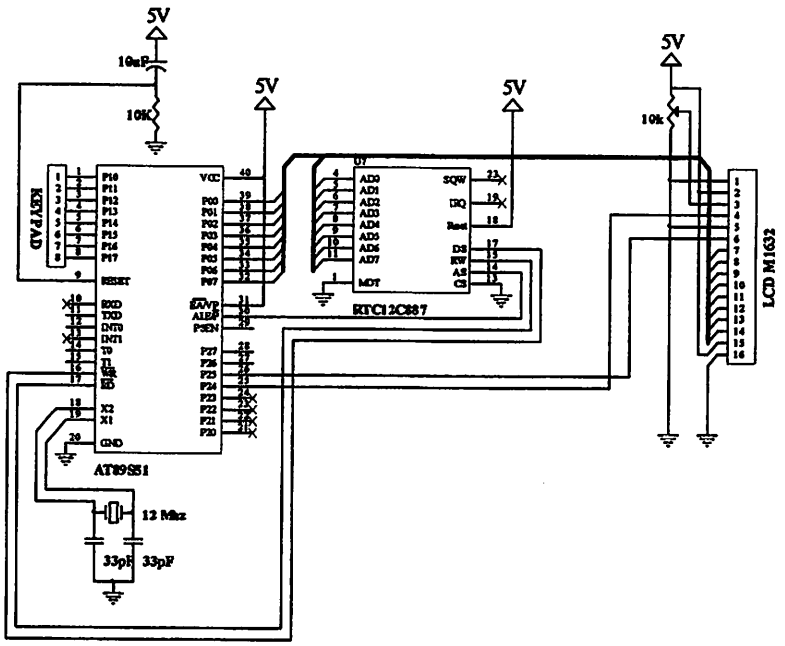
2. Peralatan Yang Dibutuhkan.

1. Minimum sistem mikrok1troller AT89S8252
2. Rangkaian RTC

3. Rangkaian Keypad
4. *Stopwatch*

3. Prosedur Pengujian.

1. Menyusun rangkaian pengujian seeperti pada gambar
2. Memprogram mikrok1troller AT89S8252 sesuai dengan program pengujian untuk mengeluarkan informasi menit, jam, tanggal dan bulan ke port P0
3. Mengatur jam dan tanggal melalui keypad
4. Mengamati perubahan tiap waktu melalui tampilan LCD
5. Mematikan dan menghidupkan sistem
6. Mengamati perubahan setelah dimatikan dan dihidupkan melalui tampilan LCD



Gambar 4.1. Rangkaian Pengujian RTC DS12C887

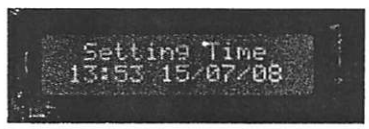
4. Hasil Pengujian

Dari beberapa langkah yang telah dilakukan dapat diketahui hasilnya sebagai berikut

1. RTC dapat bekerja dan dibaca dengan baik oleh mikrokontroller AT89S8252 serta dapat ditampilkan di LCD

Gambar 4.2. Tampilan Pembacaan RTC

2. RTC dapat dirubah dengan menggunakan keypad



Gambar 4.3. Tampilan Setting RTC

3. Perubahan jam pada RTC sesuai dengan perubahan pada stopwatch

4.2.2. Pengujian ISD

1. Tujuan

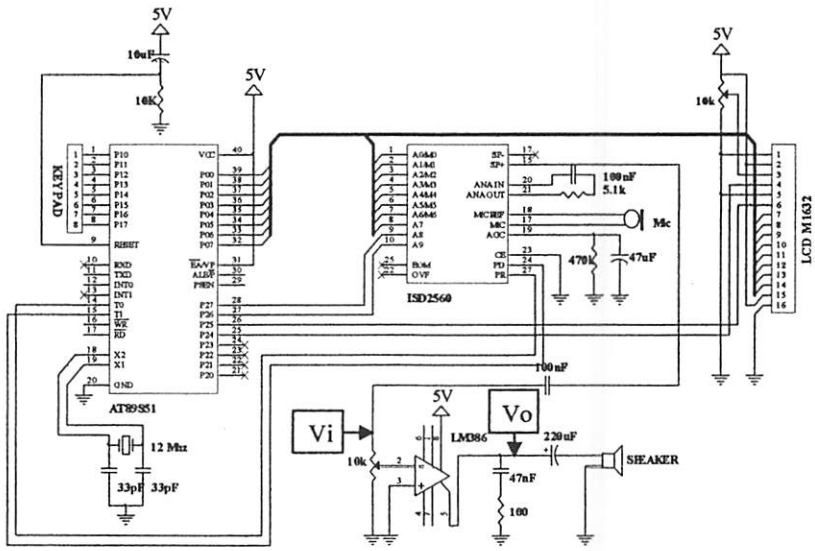
Untuk mengetahui apakah ISD dapat menyimpan suara dan membunyikan suara yang telah direkam serta untuk mengetahui apakah ISD dapat dikontrol oleh mikrokontroller AT89S8252.

2. Peralatan Yang Dibutuhkan

1. Minimum sistem mikrokontroller AT89S8252
2. Rangkaian ISD
3. Rangkaian LCD
4. Rangkaian Keypad

3. Prosedur Pengujian

1. Menyusun rangkaian pengujian sesuai dengan gambar
2. Memprogram mikrokontroller AT89S8252 sesuai dengan program pengujian untuk merekam dan membuyikan suara dari ISD
3. Merekam suara pada alamat mulai 000 – 250
4. Membunyikan suara pada ISD sesuai dengan alamat yang digunakan untuk merekam muai 000 – 250
5. Mengukur penguatan dari LM386



Gambar 4.4. Rangkaian Pengujian ISD

4. Hasil Pengujian

Dari pengujian ISD yang telah dilakukan, dapat diketahui hasilnya sebagai berikut

1. ISD dapat merekam suara yang kita bunyikan pada alamat yang kita tuju dengan menggunakan keypad dan tampilan LCD

Gambar 4.5. Tampilan Merekam Suara

2. ISD dapat membunyikan suara yang kita rekam sesuai dengan alamat yang kita gunakan untuk merekam

Gambar 4.6. Tampilan Mendengarkan Suara

3. Dari hasil pengukuran diketahui

   Vi = 2,6 Vo = 15,6

$$A = \frac{Vo}{Vi} = \frac{15,6}{2,6} = 6\ kali$$

4.2.3. Pengujian ADC dan Sensor

1. Tujuan

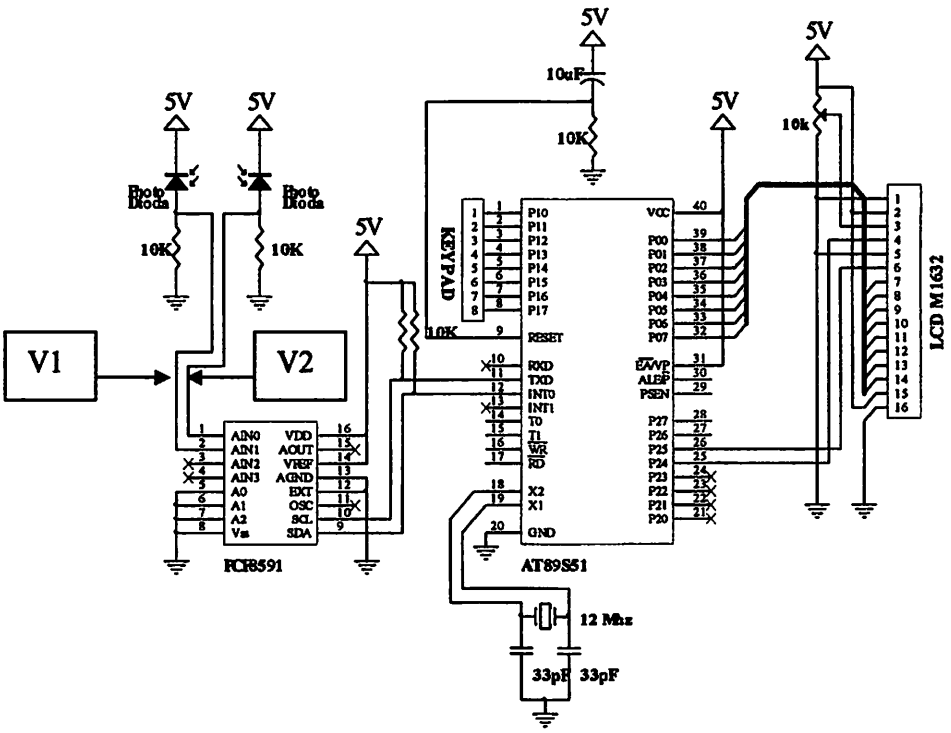
Untuk mengetahui apakah ADC dapat berfungsi dengan baik dalam merubah analog menjadi digital dan untuk mengetahui apakah rangkaian sensor dapat menghasilkan tegangan yang sesuai dengan kondisi yang berbeda-beda

2. Peralatan Yang Dibutuhkan

1. Minimum sistem mikrok1troller AT89S8252
2. Rangakaian ADC
3. Rangkaian Sensor
4. Multimeter Digital
5. Lampu Pijar

3. Prosedur Pengujian

1. Menyusun rangkaian pengujian sesuai dengan gambar
2. Memprogram mikrok1troller AT89S8252 sesuai dengan program pengujian ADC dengan data 1 bit = 0,1 Volt
3. Mengatur cahaya lampu yang mengenai sensor untuk menghasilkan data bit yang dibutuhkan
4. Mengukur tegangan output rangkaian sensor dengan multimeter



Gambar 4.7. Rangkaian Pengujian ADC dan Sensor

4. Hasil Pengujian

Dari hasil pengujian ADC dan sensor dapat diketahui besar *error* dengan rumus :

$$\%error = \frac{selisih\ V\ perhitungan\ \&\ V\ pengukuran}{V\ perhitungan} \times 100\%$$

Tabel 4.1. Hasil Pengujian ADC

OUTPUT ADC (bit)	HASIL PERHITUNGAN	HASIL PENGUKURAN		ERROR	
	Vin = OUTPUT ADC x 0,1 Volt (Volt)	V1 (Volt)	V2 (Volt)	V1 (%)	V2 (%)
10	1	1,03	1,04	3	4
14	1,4	1,43	1,43	2,1	2,1
18	1,8	1,8	1,84	0	2,2
22	2,2	2,24	2,23	0,9	0,5
26	2,6	2,62	2,58	0,8	0,8
30	3	2,96	3	1,3	0
34	3,4	3,36	3,4	1,2	0
38	3,8	3,76	3,76	1,1	1,1
42	4,2	4,17	4,14	0,7	1,4
46	4,6	4,53	4,55	1,5	1,1
% Kesalahan (Error) rata-rata				**1,26**	**1,32**

Besarnya data digital dari ADC dapat dilihat pada LCD

Gambar 4.8. Tampilan ADC

Tabel 4.2. Hasil Pengujian Sensor Photodioda

KONDISI CAHAYA	HASIL PERHITUNGAN				HASIL PENGUKURAN	ERROR (%)
	R (Ohm)	R sensor (Ohm)	Vin (Volt)	Vout (Volt)	Vout (Volt)	
Gelap	10	140 K	5	0,33	0,32	3
Bayangan Lampu	10	8,2 K	5	2,75	2,69	2,2
Cahaya Lampu	10	2,6 K	5	3,97	3.89	2
Bayangan Matahari	1	334	5	3,72	3,65	1,9
Cahaya Matahari	1	56	5	4,74	4,64	2,1
% Kesalahan (Error) rata-rata						**1,8**

4.2.4. Pengujian Keseluruhan Sistem

1. Tujuan

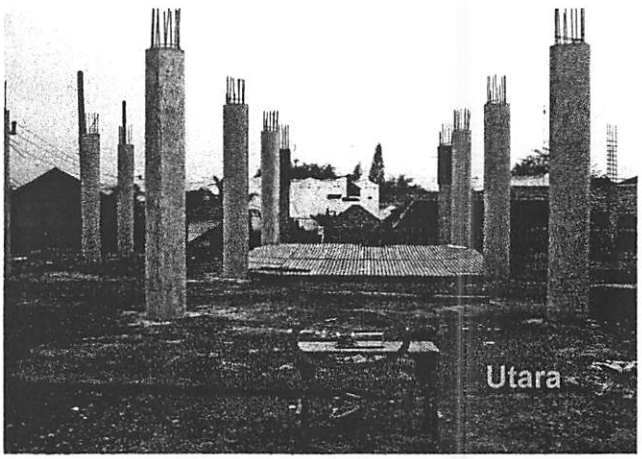
Untuk mengetahui kinerja sistem seecara keseluruhan berdasarkan perancangan yang telah dibuat, maka dilakukan pengujian sistem secara keseluruhan

2. Peralatan Yang Dibutuhkan

1. Rangkaian keseluruhan Mikrokontroller AT89S8252
2. Rangkaian RTC DS 12C887
3. Rangkaian ISD 2560
4. Rangkaian ADC
5. Rangkaian Sensor
6. Speaker
7. Catu Daya
8. Kompas Manual
9. Water Pass

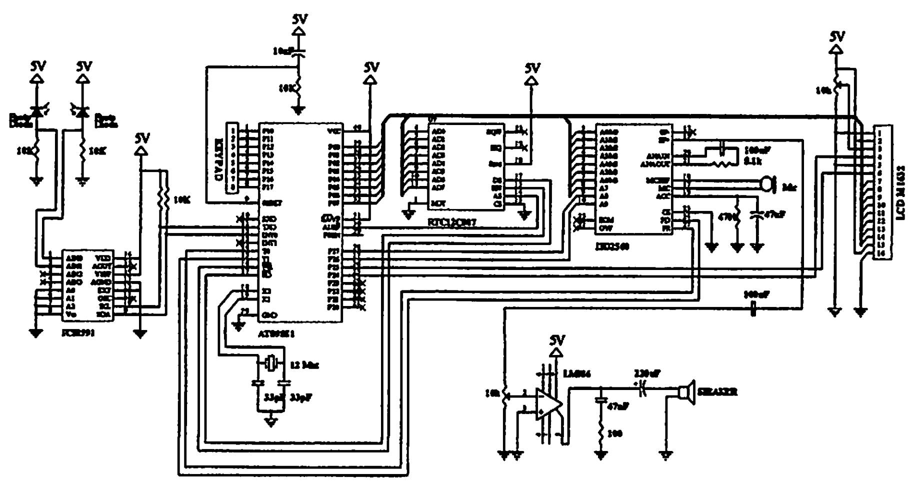
3. Proses Pengujian

1. Menggabungkan seluruh rangkaian seperti pada gambar
2. Meletakkan alat pada tempat terbuka
3. Mengatur posisi alat sesuai dengan arah mata angin yang ditunjukkan oleh kompas manual



Gambar 4.9. Pengujian Alat

4. Menghidupkan catu daya
5. Mengatur jam sesuai dengan daerah seperti WIB, WIT dan WITA
6. Mengamati perubahan jam ketika bayangan tepat berada dibawah benda
7. Membandingkan keakuratan waktu antara jam istiwak pada alat dengan jam dari telkom
8. Mengamati peringatan ketika masuk waktu sholat baik berupa suara maupun tampilan LCD



Gambar 4.10. Rangkaian Pengujian Keseluruhan Sistem

4. Hasil Pengujian

Dari hasil pengujian sistem keseluruhan yang dilakukan di kota Malang didapatkan hasil sebagai berikut :

1. Ketika bayangan tepat berada dibawah benda, jam pada alat di reset menjadi jam 12 istiwak. Setelah direset, jam dijalankan oleh RTC. Kemudian hasil reset tersebut dibandingkan dengan jam dari telkom dan selisih waktu matahari dan WIB .

Sedangkan untuk menentukan selisih antara waktu istiwak dan waktu daerah khususnya WIB (105°) untuk kota Malang menggunakan perhitungan sebagai berikut :

Bujur kota Malang = 112° 36'

Interpolasi = (Bujur – 105°) : 15

= (112° 36' – 105°) : 15

= 7°36' : 15 ➡ 1° = 60' (menit)

= (420' + 36'):15

= 30,4' ➡ 0,4' × 60 = 24" (detik)

= 30 menit 24 detik

a. Tanggal 10 September *equation of time* = 03^m02^d

Selisih = Interpolasi + *equation of time*

= $30^m24^d + 03^m02^d$

= 33^m26^d

b. Tanggal 11 September *equation of time* = 03^m23^d

Selisih = Interpolasi + *equation of time*

= $30^m24^d + 03^m23^d$

= 33^m47^d

c. Tanggal 12 September *equation of time* = 03^m44^d

Selisih = Interpolasi + *equation of time*

= $30^m24^d + 03^m44^d$

= 34^m08^d

d. Tanggal 13 September *equation of time* = 04^m05^d

Selisih = Interpolasi + *equation of time*

= $30^m24^d + 04^m05^d$

= 34^m29^d

e. Tanggal 14 September *equation of time* = 04^m26^d

Selisih = Interpolasi + *equation of time*

= $30^m24^d + 04^m26^d$

= 34^m50^d

f. Tanggal 15 September *equation of time* = 04^m48^d

Selisih = Interpolasi + *equation of time*

= $30^m24^d + 04^m48^d$

= 35^m12^d

g. Tanggal 16 September *equation of time* = 05^m09^d

Selisih = Interpolasi + *equation of time*

= $30^m24^d + 05^m09^d$

= 35^m33^d

h. Tanggal 17 September *equation of time* = 05^m30^d

Selisih = Interpolasi + *equation of time*

= $30^m24^d + 05^m30^d$

= 36^m04^d

Untuk menentukan besar nilai *error* menggunakan rumus perhitungan sebagai berikut:

$$\%\ error = \frac{selisih\ percobaan\ \&\ perhitungan\ (\det ik)}{perhitungan(\det ik)} \times 100\%$$

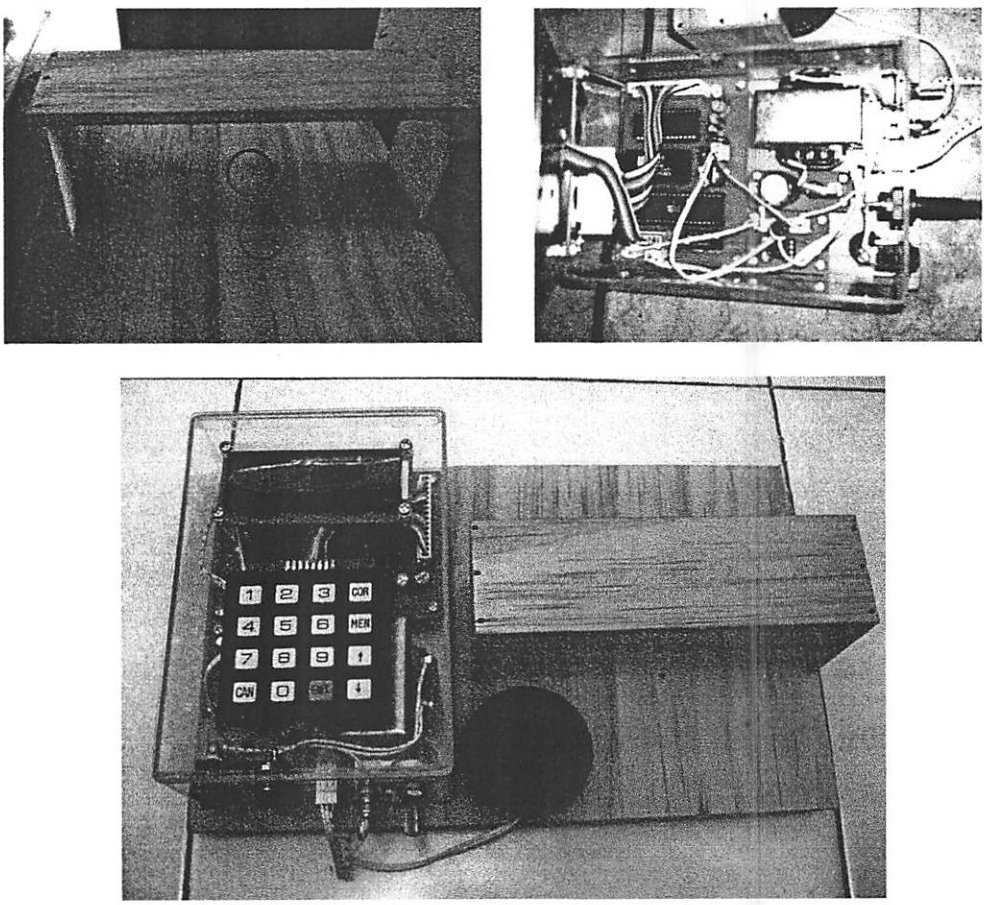
Tabel 4.3. Hasil Pengujian Setting Jam Matahari

TANGGAL	JAM		SELISIH		ERROR (%)
	ALAT	TELKOM	PERCOBAAN	PERHITUNGAN	
10-09-2008	12:00:00	11:25:33	00:34:27	00:33:26	3
11-09-2008	12:00:00	11:25:15	00:34:45	00:33:47	2,9
12-09-2008	12:00:00	11:24:56	00:35:04	00:34:08	3,1
13-09-2008	12:00:00	11:24:32	00:35:18	00:34:29	2,4
14-09-2008	12:00:00	11:24:14	00:35:46	00:34:50	2,7
15-09-2008	12:00:00	11:24:02	00:35:58	00:35:12	2,2
16-09-2008	12:00:00	11:23:39	00:36:21	00:35:33	2,3
17-09-2008	12:00:00	11:23:27	00:36:33	00:36:04	1,3
% Kesalahan (Error) rata-rata					**2,5**

2. Ketika masuk waktu sholat, peringatan suara berbunyi dan diulang selama satu menit, sedangkan keterangan di LCD terus ditampilkan sampai pada pergantian waktu sholat berikutnya.

4.3. Spesifikasi Alat Secara Umum

1. Mikrokontroller AT89S8252
2. ISD 2560
3. RTC DS12C887
4. ADC PCF8951
5. KEYPAD 4x4
6. LCD 16x2
7. Sensor Photodioda
8. Low Voltage Audio Power Am
9. plifier LM386



Gambar 4.11. Foto Alat Secara Keseluruhan

BAB V

PENUTUP

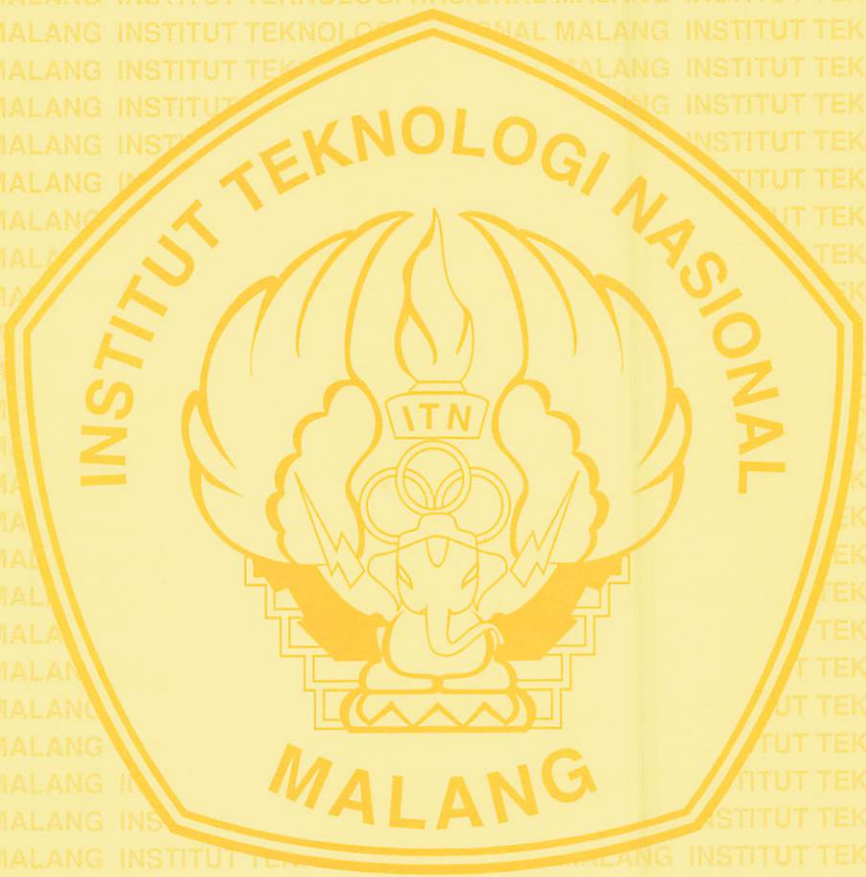
5.1. Kesimpulan

Dari perencanaan, pembuatan, dan pengujian yang telah dilakukan dapat ditarik kesimpulan sebagai berikut:

1. Dari pengujian ADC diketahui bahwa terjadi *error* pada pembacaan data output ADC oleh sensor sebesar 1,26 % dan 1,32 %.
2. Setelah dibandingkan antara perhitungan dengan hasil pengukuran, diketahui bahwa rangkaian sensor memiliki *error* rata-rata sebesar 1,8 % .
3. Ketika dilakukan percobaan langsung pada kondisi sebenarnya, dan hasilnya dibandingkan dengan data hasil perhitungan serta jam dari telkom ternyata pada setting jam matahari terdapat *error* rata-rata sebesar 2,5 %.
4. Peringatan masuknya waktu sholat baik berupa suara maupun tampilan LCD berfungsi dengan baik sesuai dengan jadwal waktu sholat yang telah disimpan di memori
5. Kecilnya *error* yang terjadi pada beberapa bagian alat menunjukkan bahwa alat ini dapat bekerja dengan baik dan memiliki tingkat akurasi yang cukup tinggi.

5.2. Saran

1. Karena sensor diletakkan diruang terbuka yang banyak terdapat debu maupun kotoran, maka perlu dipikirkan lagi bagaimana caranya supaya sensor tidak terganggu oleh kotoran tersebut.
2. Perlu dipertimbangkan lagi bagaimana jika kondisi langit sedang mendung agar alat bisa tetap berjalan dengan baik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MALANG

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LAMPIRAN

INSTITUT TEKNOLOGI NASIONAL MALANG
FAKULTAS TEKNOLOGI INDUSTRI
JURUSAN TEKNIK ELEKTRO

FORMULIR BIMBINGAN SKRIPSI

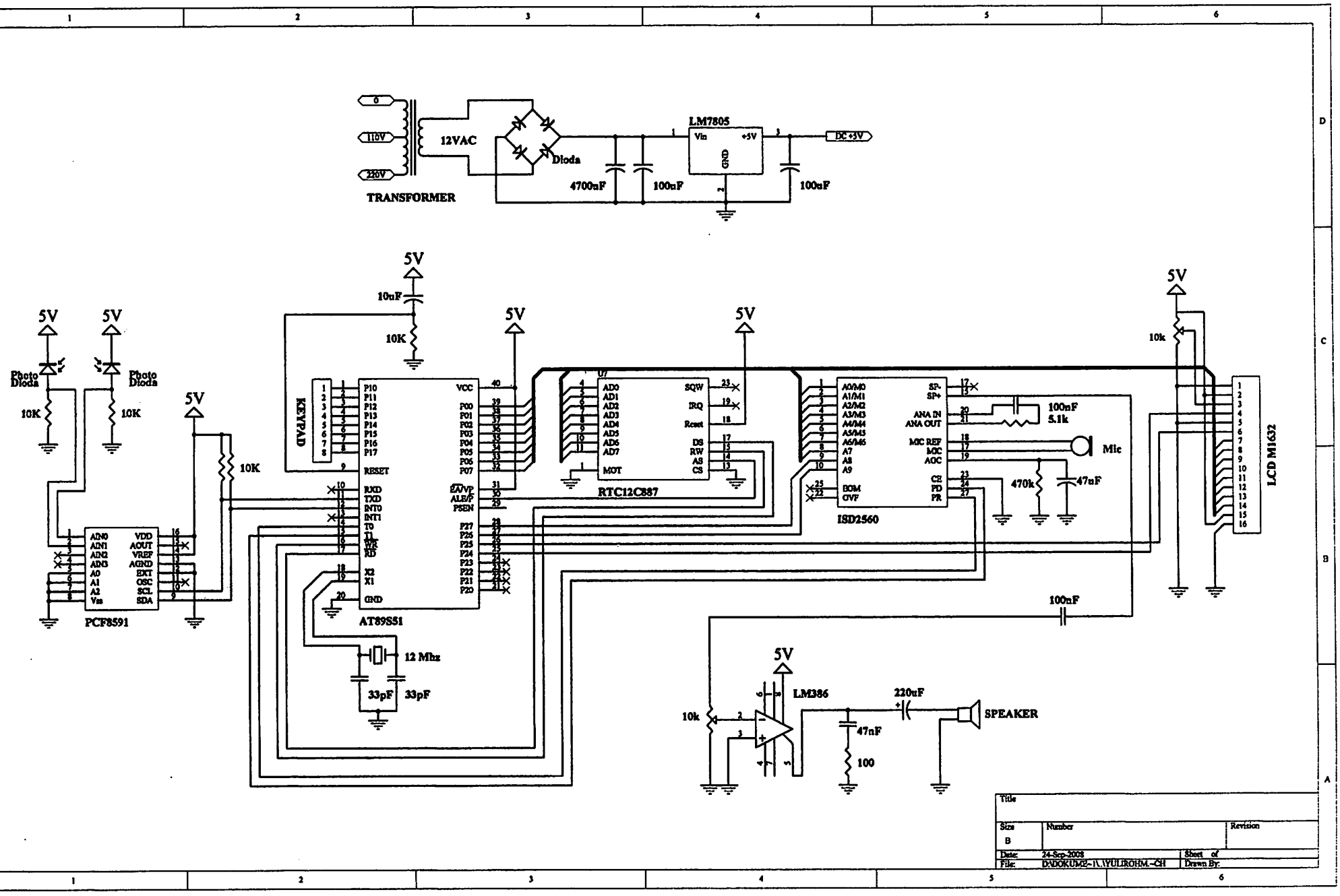
Nama : YULI ROHMAD RIADI
NIM : 00.17055
Masa Bimbingan : 03 April 2008 s/d 03 Oktober 2008
Judul Skripsi : PERENCANAAN DAN PEMBUATAN JAM MATAHARI DIGITAL UNTUK MENENTUKAN WAKTU SHOLAT BERDASARKAN BAYANGAN MATAHARI DAN ORDINAT DAERAH BERRBASIS AT89S8252

No	Tanggal	Uraian	Paraf Pembimbing
1	07-09-2008	Bab III : Lakukan perhitungan pada rangkaian	
2	09-09-2008	Bab III : Periksa dan perbaiki kembali flowchart software Bab V : Kesimpulan harus sesuai dengan percobaan	
3	13-09-2008	Bab IV : Cari besar error yang terjadi pada alat dengan menggunakan jam telkom sebagai pembanding	
4	18-09-2008	Bab III : Tampilkan perhitungan rangkaian sensor untuk setiap data	
5	18-09-2008	Bab IV : Berikan contoh perhitungan pada rumus yang menunjukkan selisih waktu	
6	18-09-2008	Bab V : Nilai error pada kesimpulan tidak sesuai dengan nilai error pada pengujian	
7	18-09-2008	Bab II : Lengkapi gambar dan tabel dengan sumbernya	
8	18-09-2008	Lampiran : Masukkan data-data pendukung kedalam lampiran	
9	20-09-2008	ACC maju ujian skripsi	
10			

Malang, 2008
Dosen Pembimbing

Ir. Eko Nurcahyo
NIP.Y.1028700172

Form S-4a


0
110V
220V
TRANSFORMER
12VAC
Dioda
LM7805
Vin
+5V
GND
DC +5V
4700uF
100uF
100uF
5V
10uF
10K
Photo Dioda
Photo Dioda
10K
10K
10K
PCF8591
AIN0
AIN1
AIN2
AIN3
A0
A1
A2
Vss
VDD
AOUT
VREF
AGND
EXT
OSC
SCL
SDA
AT89S51
P10
P11
P12
P13
P14
P15
P16
P17
RESET
RXD
TXD
INT0
INT1
T0
T1
WR
RD
X2
X1
GND
VCC
P00
P01
P02
P03
P04
P05
P06
P07
EA/VP
ALE/P
PSEN
P27
P26
P25
P24
P23
P22
P21
P20
KEYPAD
U7
AD0
AD1
AD2
AD3
AD4
AD5
AD6
AD7
MOT
SQW
IRQ
Rest
DS
RW
AS
CS
RTC12C887
12 Mhz
33pF
33pF
ISD2560
A0/M0
A1/M1
A2/M2
A3/M3
A4/M4
A5/M5
A6/M6
A7
A8
A9
BOM
OVF
SP-
SP+
ANA IN
ANA OUT
MIC REF
MIC
AOC
CE
PD
FR
100nF
5.1k
Mic
470k
47nF
10k
LCD M1632
100nF
LM386
220uF
SPEAKER
10k
47nF
100
Title
Size
B
Number
Revision
Date:
24-Sep-2008
Sheet of
File:
D:\DOKUM~1\..\VULIROHM.~CH
Drawn By:

DAFTAR DEKLINASI MATAHARI DAN EQUATION OF TIME

TG	JANUARI		PEBRUARI		MARET	
	DEK	EQ.T	DEK	EQ.T	DEK	EQ.T
1	-22° 58' 12"	-03^{m} 38^{d}	-17° 00' 37"	-13^{m} 38^{d}	-07° 28' 10"	-12^{m} 21^{d}
2	-22° 53' 10"	-04^{m} 06^{d}	-16° 43' 18"	-13^{m} 46^{d}	-07° 05' 17"	-12^{m} 08^{d}
3	-22° 47' 24"	-04^{m} 34^{d}	-16° 25' 42"	-13^{m} 52^{d}	-06° 42' 18"	-11^{m} 56^{d}
4	-22° 41' 10"	-05^{m} 01^{d}	-16° 07' 49"	-13^{m} 58^{d}	-06° 19' 13"	-11^{m} 43^{d}
5	-22° 34' 30"	-05^{m} 28^{d}	-15° 49' 39"	-14^{m} 03^{d}	-05° 56' 03"	-11^{m} 29^{d}
6	-22° 27' 23"	-05^{m} 54^{d}	-15° 31' 13"	-14^{m} 07^{d}	-05° 32' 49"	-11^{m} 15^{d}
7	-22° 19' 49"	-06^{m} 20^{d}	-15° 12' 31"	-14^{m} 11^{d}	-05° 09' 30"	-11^{m} 01^{d}
8	-22° 11' 38"	-06^{m} 46^{d}	-14° 53' 34"	-14^{m} 13^{d}	-04° 46' 07"	-10^{m} 46^{d}
9	-22° 03' 23"	-07^{m} 11^{d}	-14° 34' 22"	-14^{m} 15^{d}	-04° 22' 41"	-10^{m} 31^{d}
10	-21° 54' 31"	-07^{m} 35^{d}	-14° 14' 55"	-14^{m} 16^{d}	-03° 59' 11"	-10^{m} 16^{d}
11	-21° 45' 14"	-07^{m} 59^{d}	-13° 55' 14"	-14^{m} 16^{d}	-03° 35' 39"	-10^{m} 00^{d}
12	-21° 35' 31"	-08^{m} 22^{d}	-13° 35' 20"	-14^{m} 16^{d}	-03° 12' 03"	-09^{m} 44^{d}
13	-21° 25' 23"	-08^{m} 45^{d}	-13° 15' 11"	-14^{m} 15^{d}	-02° 48' 26"	-09^{m} 27^{d}
14	-21° 14' 50"	-09^{m} 07^{d}	-12° 54' 50"	-14^{m} 13^{d}	-02° 24' 46"	-09^{m} 11^{d}
15	-21° 03' 53"	-09^{m} 28^{d}	-12° 34' 16"	-14^{m} 10^{d}	-02° 01' 05"	-08^{m} 54^{d}
16	-20° 52' 31"	-09^{m} 49^{d}	-12° 13' 30"	-14^{m} 06^{d}	-01° 37' 23"	-08^{m} 37^{d}
17	-20° 40' 46"	-10^{m} 09^{d}	-11° 52' 32"	-14^{m} 02^{d}	-01° 13' 40"	-08^{m} 20^{d}
18	-20° 28' 53"	-10^{m} 28^{d}	-11° 31' 23"	-13^{m} 57^{d}	-00° 49' 57"	-08^{m} 02^{d}
19	-20° 16' 05"	-10^{m} 47^{d}	-11° 10' 03"	-13^{m} 51^{d}	-00° 26' 14"	-07^{m} 45^{d}
20	-20° 03' 10"	-11^{m} 05^{d}	-10° 48' 32"	-13^{m} 45^{d}	-00° 02' 31"	-07^{m} 27^{d}
21	-19° 49' 52"	-11^{m} 22^{d}	-10° 26' 51"	-13^{m} 38^{d}	+00° 21'12"	-07^{m} 09^{d}
22	-19° 36' 12"	-11^{m} 38^{d}	-10° 05' 00"	-13^{m} 30^{d}	+00° 44'53"	-06^{m} 51^{d}
23	-19° 22' 11"	-11^{m} 54^{d}	-09° 43' 01"	-13^{m} 22^{d}	+01° 08'33"	-06^{m} 33^{d}
24	-19° 07' 48"	-12^{m} 09^{d}	-09° 20' 52"	-13^{m} 13^{d}	+01° 32'11"	-06^{m} 15^{d}
25	-18° 53' 04"	-12^{m} 23^{d}	-08° 58' 35"	-13^{m} 04^{d}	+01° 55'47"	-05^{m} 57^{d}
26	-18° 37' 59"	-12^{m} 36^{d}	-08° 36' 10"	-12^{m} 54^{d}	+02° 19'21"	-05^{m} 38^{d}
27	-18° 22' 33"	-12^{m} 48^{d}	-08° 13' 12"	-12^{m} 43^{d}	+02° 42'51"	-05^{m} 20^{d}
28	-18° 06' 48"	-13^{m} 00^{d}	-07° 50' 57"	-12^{m} 32^{d}	+03° 06'18"	-05^{m} 02^{d}
29	-17° 50' 44"	-13^{m} 11^{d}	—	—	+03° 29'42"	-04^{m} 44^{d}
30	-17° 34' 20"	-13^{m} 21^{d}	—	—	+03° 53'02"	-04^{m} 26^{d}
31	-17° 17' 38"	-13^{m} 30^{d}	—	—	+04° 16'17"	-04^{m} 08^{d}

(Sumber : Muhyidin Khazin, 2004:265)

DAFTAR DEKLINASI MATAHARI DAN EQUATION OF TIME

TG	APRIL		MEI		JUNI	
	DEK	EQ.T	DEK	EQ.T	DEK	EQ.T
1	+04° 39' 27"	-03^{m} 50^{d}	+15° 10' 05"	+02^{m} 55^{d}	+22° 05' 39"	+02^{m} 11^{d}
2	+05° 02' 32"	-03^{m} 33^{d}	+15° 28' 02"	+03^{m} 02^{d}	+22° 13' 29"	+02^{m} 01^{d}
3	+05° 25' 32"	-03^{m} 15^{d}	+15° 45' 43"	+03^{m} 08^{d}	+22° 20' 56"	+01^{m} 52^{d}
4	+05° 48' 26"	-02^{m} 57^{d}	+16° 03' 09"	+03^{m} 14^{d}	+22° 27' 59"	+01^{m} 41^{d}
5	+06° 11' 14"	-02^{m} 40^{d}	+16° 20' 19"	+03^{m} 19^{d}	+22° 34' 39"	+01^{m} 31^{d}
6	+06° 33' 39"	-02^{m} 23^{d}	+16° 37' 12"	+03^{m} 24^{d}	+22° 40' 55"	+01^{m} 20^{d}
7	+06° 56' 29"	-02^{m} 06^{d}	+16° 53' 49"	+03^{m} 28^{d}	+22° 46' 47"	+01^{m} 09^{d}
8	+07° 18' 56"	-01^{m} 50^{d}	+17° 10' 08"	+03^{m} 31^{d}	+22° 52' 15"	+00^{m} 58^{d}
9	+07° 41' 16"	-01^{m} 33^{d}	+17° 26' 11"	+03^{m} 34^{d}	+22° 57' 19"	+00^{m} 46^{d}
10	+08° 03' 28"	-01^{m} 17^{d}	+17° 41' 56"	+03^{m} 37^{d}	+23° 01' 59"	+00^{m} 34^{d}
11	+08° 25' 32"	-01^{m} 01^{d}	+17° 57' 23"	+03^{m} 39^{d}	+23° 06' 14"	+00^{m} 22^{d}
12	+08° 47' 28"	-00^{m} 46^{d}	+18° 12' 33"	+03^{m} 40^{d}	+23° 10' 06"	+00^{m} 10^{d}
13	+09° 09' 15"	-00^{m} 30^{d}	+18° 27' 24"	+03^{m} 40^{d}	+23° 13' 32"	-00^{m} 03^{d}
14	+09° 30' 52"	-00^{m} 15^{d}	+18° 41' 56"	+03^{m} 40^{d}	+23° 16' 35"	-00^{m} 15^{d}
15	+09° 52' 02"	-00^{m} 01^{d}	+18° 56' 10"	+03^{m} 40^{d}	+23° 19' 12"	-00^{m} 29^{d}
16	+10° 13' 40"	+00^{m} 13^{d}	+19° 10' 04"	+03^{m} 39^{d}	+23° 21' 25"	-00^{m} 41^{d}
17	+10° 34' 48"	+00^{m} 27^{d}	+19° 23' 40"	+03^{m} 37^{d}	+23° 23' 13"	-00^{m} 54^{d}
18	+10° 55' 47"	+00^{m} 41^{d}	+19° 36' 55"	+03^{m} 35^{d}	+23° 24' 37"	-01^{m} 07^{d}
19	+11° 16' 34"	+00^{m} 54^{d}	+19° 49' 50"	+03^{m} 32^{d}	+23° 25' 36"	-01^{m} 20^{d}
20	+11° 37' 11"	+01^{m} 07^{d}	+20° 02' 26"	+03^{m} 29^{d}	+23° 26' 09"	-01^{m} 33^{d}
21	+11° 57' 36"	+01^{m} 19^{d}	+20° 14' 40"	+03^{m} 25^{d}	+23° 26' 18"	-01^{m} 46^{d}
22	+12° 17' 50"	+01^{m} 31^{d}	+20° 26' 34"	+03^{m} 21^{d}	+23° 26' 03"	-01^{m} 59^{d}
23	+12° 37' 51"	+01^{m} 42^{d}	+20° 36' 07"	+03^{m} 16^{d}	+23° 25' 22"	-02^{m} 12^{d}
24	+12° 57' 40"	+01^{m} 53^{d}	+20° 49' 19"	+03^{m} 11^{d}	+23° 24' 17"	-02^{m} 25^{d}
25	+13° 17' 16"	+02^{m} 03^{d}	+21° 00' 09"	+03^{m} 05^{d}	+23° 22' 47"	-02^{m} 38^{d}
26	+13° 36' 39"	+02^{m} 13^{d}	+21° 10' 37"	+02^{m} 58^{d}	+23° 20' 52"	-02^{m} 50^{d}
27	+13° 55' 48"	+02^{m} 23^{d}	+21° 20' 44"	+02^{m} 52^{d}	+23° 18' 33"	-03^{m} 03^{d}
28	+14° 14' 44"	+02^{m} 32^{d}	+21° 30' 28"	+02^{m} 44^{d}	+23° 15' 49"	-03^{m} 15^{d}
29	+14° 33' 48"	+02^{m} 40^{d}	+21° 39' 50"	+02^{m} 37^{d}	+23° 12' 40"	-03^{m} 27^{d}
30	+14° 51' 53"	+02^{m} 48^{d}	+21° 48' 49"	+02^{m} 28^{d}	+23° 09' 07"	-03^{m} 39^{d}
31	—	—	+21° 57' 25"	+02^{m} 20^{d}	—	—

(Sumber : Muhyidin Khazin, 2004:266)

DAFTAR DEKLINASI MATAHARI DAN EQUATION OF TIME

TG	JULI		AGUSTUS		SEPTEMBER	
	DEK	EQ.T	DEK	EQ.T	DEK	EQ.T
1	+23° 05' 10"	-03^{m} 51^{d}	+17° 56' 16"	-06^{m} 19^{d}	+08° 10' 03"	+00^{m} 01^{d}
2	+23° 00' 48"	-04^{m} 02^{d}	+17° 40' 56"	-06^{m} 14^{d}	+07° 48' 12"	+00^{m} 20^{d}
3	+22° 56' 03"	-04^{m} 13^{d}	+17° 25' 19"	-06^{m} 10^{d}	+07° 26' 13"	+00^{m} 40^{d}
4	+22° 50' 53"	-04^{m} 24^{d}	+17° 09' 25"	-06^{m} 04^{d}	+07° 04' 07"	+00^{m} 59^{d}
5	+22° 45' 20"	-04^{m} 35^{d}	+16° 53' 14"	-05^{m} 58^{d}	+06° 41' 55"	+01^{m} 19^{d}
6	+22° 39' 23"	-04^{m} 45^{d}	+16° 36' 47"	-05^{m} 52^{d}	+06° 19' 35"	+01^{m} 39^{d}
7	+22° 33' 02"	-04^{m} 55^{d}	+16° 20' 04"	-05^{m} 45^{d}	+05° 57' 10"	+02^{m} 00^{d}
8	+22° 26' 18"	-05^{m} 04^{d}	+16° 03' 05"	-05^{m} 37^{d}	+05° 34' 38"	+02^{m} 20^{d}
9	+22° 19' 11"	-05^{m} 13^{d}	+15° 45' 51"	-05^{m} 29^{d}	+05° 12' 01"	+02^{m} 41^{d}
10	+22° 11' 41"	-05^{m} 21^{d}	+15° 28' 21"	-05^{m} 20^{d}	+04° 49' 18"	+03^{m} 02^{d}
11	+22° 03' 47"	-05^{m} 30^{d}	+15° 10' 37"	-05^{m} 11^{d}	+04° 26' 30"	+03^{m} 23^{d}
12	+21° 55' 31"	-05^{m} 37^{d}	+14° 52' 38"	-05^{m} 01^{d}	+04° 03' 37"	+03^{m} 44^{d}
13	+21° 46' 53"	-05^{m} 45^{d}	+14° 34' 25"	-04^{m} 50^{d}	+03° 40' 40"	+04^{m} 05^{d}
14	+21° 37' 52"	-05^{m} 51^{d}	+14° 15' 57"	-04^{m} 39^{d}	+03° 17' 39"	+04^{m} 26^{d}
15	+21° 28' 29"	-05^{m} 58^{d}	+13° 57' 16"	-04^{m} 27^{d}	+02° 54' 35"	+04^{m} 48^{d}
16	+21° 18' 44"	-06^{m} 03^{d}	+13° 38' 22"	-04^{m} 15^{d}	+02° 31' 27"	+05^{m} 09^{d}
17	+21° 08' 37"	-06^{m} 08^{d}	+13° 19' 49"	-04^{m} 02^{d}	+02° 08' 15"	+05^{m} 30^{d}
18	+20° 58' 09"	-06^{m} 13^{d}	+12° 59' 54"	-03^{m} 49^{d}	+01° 45' 02"	+05^{m} 52^{d}
19	+20° 47' 19"	-06^{m} 17^{d}	+12° 40' 22"	-03^{m} 36^{d}	+01° 21' 45"	+06^{m} 13^{d}
20	+20° 36' 09"	-06^{m} 21^{d}	+12° 20' 37"	-03^{m} 21^{d}	+00° 58' 27"	+06^{m} 34^{d}
21	+20° 24' 38"	-06^{m} 24^{d}	+12° 00' 21"	-03^{m} 07^{d}	+00° 35' 08"	+06^{m} 56^{d}
22	+20° 12' 46"	-06^{m} 26^{d}	+11° 40' 33"	-02^{m} 52^{d}	+00° 11' 47"	+07^{m} 17^{d}
23	+20° 00' 33"	-06^{m} 28^{d}	+11° 20' 14"	-02^{m} 36^{d}	-00° 11' 35"	+07^{m} 38^{d}
24	+19° 48' 01"	-06^{m} 29^{d}	+10° 59' 45"	-02^{m} 20^{d}	-00° 34' 57"	+07^{m} 59^{d}
25	+19° 35' 09"	-06^{m} 30^{d}	+10° 39' 05"	-02^{m} 04^{d}	-00° 58' 20"	+08^{m} 20^{d}
26	+19° 21' 58"	-06^{m} 30^{d}	+10° 18' 15"	-01^{m} 47^{d}	-01° 21' 42"	+08^{m} 40^{d}
27	+19° 08' 27"	-06^{m} 29^{d}	+09° 57' 16"	-01^{m} 30^{d}	-01° 45' 04"	+09^{m} 01^{d}
28	+18° 54' 38"	-06^{m} 28^{d}	+09° 36' 07"	-01^{m} 13^{d}	-02° 08' 24"	+09^{m} 21^{d}
29	+18° 40' 29"	-06^{m} 27^{d}	+09° 14' 48"	-00^{m} 55^{d}	-02° 31' 44"	+09^{m} 41^{d}
30	+18° 26' 03"	-06^{m} 25^{d}	+08° 53' 22"	-00^{m} 36^{d}	-02° 55' 02"	+10^{m} 01^{d}
31	+18° 11' 18"	-06^{m} 22^{d}	+08° 31' 46"	-00^{m} 18^{d}	—	—

(Sumber : Muhyidin Khazin, 2004:267)

DAFTAR DEKLINASI MATAHARI DAN EQUATION OF TIME

TG	OKTOBER		NOPEMBER		DESEMBER	
	DEK	EQ.T	DEK	EQ.T	DEK	EQ.T
1	-03° 18' 18"	+10^{m} 20^{d}	-14° 31' 30"	+16^{m} 27^{d}	-21° 50' 50"	+10^{m} 55^{d}
2	-03° 41' 32"	+10^{m} 40^{d}	-14° 50' 31"	+16^{m} 28^{d}	-21° 59' 49"	+10^{m} 32^{d}
3	-04° 04' 44"	+10^{m} 59^{d}	-15° 09' 18"	+16^{m} 28^{d}	-22° 08' 23"	+10^{m} 09^{d}
4	-04° 27' 52"	+11^{m} 17^{d}	-15° 27' 50"	+16^{m} 27^{d}	-22° 16' 32"	+09^{m} 45^{d}
5	-04° 50' 57"	+11^{m} 36^{d}	-15° 46' 06"	+16^{m} 25^{d}	-22° 24' 15"	+09^{m} 20^{d}
6	-05° 13' 59"	+11^{m} 53^{d}	-16° 04' 08"	+16^{m} 23^{d}	-22° 31' 31"	+08^{m} 55^{d}
7	-05° 36' 32"	+12^{m} 11^{d}	-16° 21' 53"	+16^{m} 21^{d}	-22° 38' 22"	+08^{m} 29^{d}
8	-06° 00' 48"	+12^{m} 29^{d}	-16° 39' 22"	+16^{m} 17^{d}	-22° 44' 45"	+08^{m} 03^{d}
9	-06° 22' 40"	+12^{m} 45^{d}	-16° 56' 34"	+16^{m} 12^{d}	-22° 50' 42"	+07^{m} 36^{d}
10	-06° 45' 24"	+13^{m} 01^{d}	-17° 13' 29"	+16^{m} 06^{d}	-22° 56' 12"	+07^{m} 09^{d}
11	-07° 08' 03"	+13^{m} 17^{d}	-17° 30' 06"	+16^{m} 00^{d}	-23° 01' 15"	+06^{m} 41^{d}
12	-07° 30' 36"	+13^{m} 32^{d}	-17° 46' 26"	+15^{m} 52^{d}	-23° 05' 51"	+06^{m} 13^{d}
13	-07° 53' 03"	+13^{m} 47^{d}	-18° 02' 27"	+15^{m} 44^{d}	-23° 09' 59"	+05^{m} 45^{d}
14	-08° 15' 25"	+14^{m} 01^{d}	-18° 18' 09"	+15^{m} 35^{d}	-23° 13' 39"	+05^{m} 17^{d}
15	-08° 37' 38"	+14^{m} 15^{d}	-18° 33' 32"	+15^{m} 25^{d}	-23° 16' 52"	+04^{m} 47^{d}
16	-08° 59' 44"	+14^{m} 28^{d}	-18° 48' 35"	+15^{m} 14^{d}	-23° 19' 37"	+04^{m} 19^{d}
17	-09° 21' 43"	+14^{m} 40^{d}	-19° 03' 18"	+15^{m} 02^{d}	-23° 21' 54"	+03^{m} 50^{d}
18	-09° 43' 34"	+14^{m} 52^{d}	-19° 17' 41"	+14^{m} 50^{d}	-23° 23' 42"	+03^{m} 20^{d}
19	-10° 05' 16"	+15^{m} 04^{d}	-19° 31' 43"	+14^{m} 36^{d}	-23° 25' 03"	+02^{m} 51^{d}
20	-10° 26' 50"	+15^{m} 14^{d}	-19° 45' 24"	+14^{m} 22^{d}	-23° 25' 55"	+02^{m} 21^{d}
21	-10° 48' 14"	+15^{m} 24^{d}	-19° 58' 43"	+14^{m} 07^{d}	-23° 26' 19"	+01^{m} 51^{d}
22	-11° 09' 28"	+15^{m} 34^{d}	-20° 11' 40"	+13^{m} 51^{d}	-23° 26' 15"	+01^{m} 22^{d}
23	-11° 30' 33"	+15^{m} 42^{d}	-20° 24' 15"	+13^{m} 35^{d}	-23° 25' 42"	+00^{m} 52^{d}
24	-11° 51' 26"	+15^{m} 50^{d}	-20° 36' 27"	+13^{m} 17^{d}	-23° 24' 42"	+00^{m} 22^{d}
25	-12° 12' 09"	+15^{m} 57^{d}	-20° 48' 16"	+12^{m} 59^{d}	-23° 23' 13"	-00^{m} 08^{d}
26	-12° 32' 41"	+16^{m} 04^{d}	-20° 59' 42"	+12^{m} 40^{d}	-23° 21' 15"	-00^{m} 37^{d}
27	-12° 53' 01"	+16^{m} 10^{d}	-21° 10' 44"	+12^{m} 21^{d}	-23° 18' 50"	-01^{m} 07^{d}
28	-13° 13' 08"	+16^{m} 15^{d}	-21° 21' 22"	+12^{m} 00^{d}	-23° 15' 56"	-01^{m} 36^{d}
29	-13° 33' 03"	+16^{m} 19^{d}	-21° 31' 36"	+11^{m} 39^{d}	-23° 12' 35"	-02^{m} 05^{d}
30	-13° 52' 45"	+16^{m} 22^{d}	-21° 41' 25"	+11^{m} 18^{d}	-23° 08' 46"	-02^{m} 34^{d}
31	-14° 12' 14"	+16^{m} 25^{d}	—	—	-23° 04' 29"	-03^{m} 03^{d}

(Sumber : Muhyidin Khazin, 2004:268)

Jadwal Waktu Sholat WIS Versi Durusul Falakiyah

untuk Daerah :Malang Kota (07°57' LS / 112°36' BT)

(Arah QIBLAT :294° 17' dari titik Utara / 24° 17' dari titik Barat)

Bln	Tgl	Dluhur	Ashar	Maghrib	Isya'	Shubuh	Tgl	Bln
JUNI	17	12:04	15:22	17:51	19:02	4:52	22	JUNI
	12	12:04	15:22	17:51	19:02	4:52	27	
	7	12:04	15:22	17:51	19:02	4:52	3	JULI
	2	12:04	15:22	17:52	19:02	4:52	8	
MEI	27	12:04	15:22	17:52	19:02	4:52	13	
	22	12:04	15:22	17:53	19:02	4:51	18	
	17	12:04	15:22	17:53	19:02	4:51	23	
	12	12:04	15:22	17:54	19:02	4:51	28	
	7	12:04	15:22	17:55	19:03	4:51	3	AGUSTUS
	2	12:04	15:22	17:56	19:03	4:51	8	
APRIL	26	12:04	15:22	17:57	19:04	4:50	13	
	21	12:04	15:22	17:58	19:04	4:50	18	
	16	12:04	15:21	17:59	19:05	4:49	23	
	11	12:04	15:20	18:00	19:06	4:48	29	
	6	12:04	15:19	18:01	19:06	4:47	3	SEPTEMBER
	1	12:04	15:18	18:02	19:07	4:47	8	
MARET	26	12:04	15:16	18:04	19:09	4:45	13	
	21	12:04	15:14	18:05	19:10	4:44	18	
	16	12:04	15:11	18:06	19:11	4:43	24	
	11	12:04	15:09	18:07	19:12	4:41	29	
	6	12:04	15:06	18:08	19:14	4:40	4	OKTOBER
	1	12:04	15:03	18:09	19:15	4:39	9	
PEBRUARI	24	12:04	15:07	18:10	19:17	4:37	14	
	19	12:04	15:11	18:11	19:18	4:35	19	
	14	12:04	15:14	18:12	19:20	4:34	24	
	9	12:04	15:17	18:13	19:21	4:32	29	
	4	12:04	15:19	18:14	19:23	4:30	3	NOPEMBER
JANUARI	31	12:04	15:21	18:15	19:24	4:29	8	
	26	12:04	15:23	18:16	19:25	4:28	13	
	21	12:04	15:24	18:16	19:27	4:26	18	
	16	12:04	15:26	18:17	19:28	4:25	22	
	11	12:04	15:27	18:17	19:29	4:24	28	
	6	12:04	15:27	18:18	19:30	4:23	4	DES
	1	12:04	15:28	18:18	19:30	4:22	9	
DES	29	12:04	15:28	18:18	19:31	4:22	14	
	24	12:04	15:28	18:18	19:31	4:22	19	
Bln	Tgl	Dluhur	Ashar	Maghrib	Isya'	Shubuh	Tgl	Bln

(Sumber : Lajnah Falakiyah NU Kab. Pasuruan)

Features

- Compatible with MCS-51™ Products
- 8K Bytes of In-System Reprogrammable Downloadable Flash Memory
  - SPI Serial Interface for Program Downloading
  - Endurance: 1,000 Write/Erase Cycles
- 2K Bytes EEPROM
  - Endurance: 100,000 Write/Erase Cycles
- 4.0V to 6V Operating Range
- Fully Static Operation: 0 Hz to 24 MHz
- Three-Level Program Memory Lock
- 256 x 8-bit Internal RAM
- 32 Programmable I/O Lines
- Three 16-bit Timer/Counters
- Nine Interrupt Sources
- Programmable UART Serial Channel
- SPI Serial Interface
- Low Power Idle and Power Down Modes
- Interrupt Recovery From Power Down
- Programmable Watchdog Timer
- Dual Data Pointer
- Power Off Flag

Description

The AT89S8252 is a low-power, high-performance CMOS 8-bit microcomputer with 8K bytes of Downloadable Flash programmable and erasable read only memory and 2K bytes of EEPROM. The device is manufactured using Atmel's high density nonvolatile memory technology and is compatible with the industry standard 80C51 instruction set and pinout. The on-chip Downloadable Flash allows the program memory to be reprogrammed in-system through an SPI serial interface or by a conventional nonvolatile memory programmer. By combining a versatile 8-bit CPU with Downloadable Flash on a monolithic chip, the Atmel AT89S8252 is a powerful microcomputer which provides a highly flexible and cost effective solution to many embedded control applications.

The AT89S8252 provides the following standard features: 8K bytes of Downloadable Flash, 2K bytes of EEPROM, 256 bytes of RAM, 32 I/O lines, programmable watchdog timer, two Data Pointers, three 16-bit timer/counters, a six-vector two-level interrupt architecture, a full duplex serial port, on-chip oscillator, and clock circuitry. In addition, the AT89S8252 is designed with static logic for operation down to zero frequency and supports two software selectable power saving modes. The Idle Mode stops the CPU while allowing the RAM, timer/counters, serial port, and interrupt system to continue functioning. The Power Down Mode saves the RAM contents but freezes the oscillator, disabling all other chip functions until the next interrupt or hardware reset.

The Downloadable Flash can be changed a single byte at a time and is accessible through the SPI serial interface. Holding RESET active forces the SPI bus into a serial programming interface and allows the program memory to be written to or read from unless Lock Bit 2 has been activated.

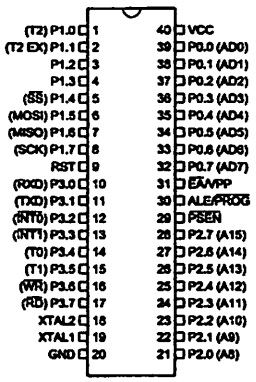
8-Bit Microcontroller with 8K Bytes Flash

AT89S8252

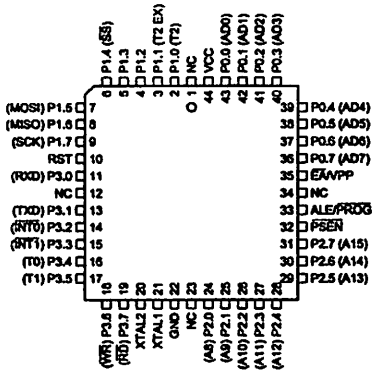
0401D-A-12/97

Pin Configurations

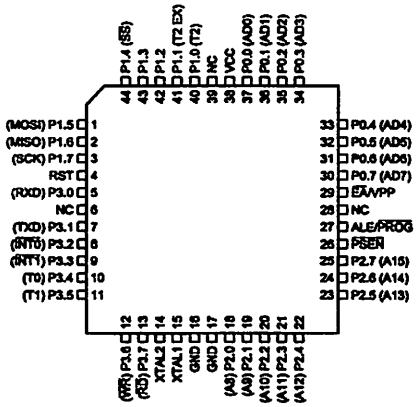
PDIP



PLCC



PQFP/TQFP



Pin Description

V_{CC}
Supply voltage.

GND
Ground.

Port 0
Port 0 is an 8-bit open drain bidirectional I/O port. As an output port, each pin can sink eight TTL inputs. When 1s are written to port 0 pins, the pins can be used as high-impedance inputs.

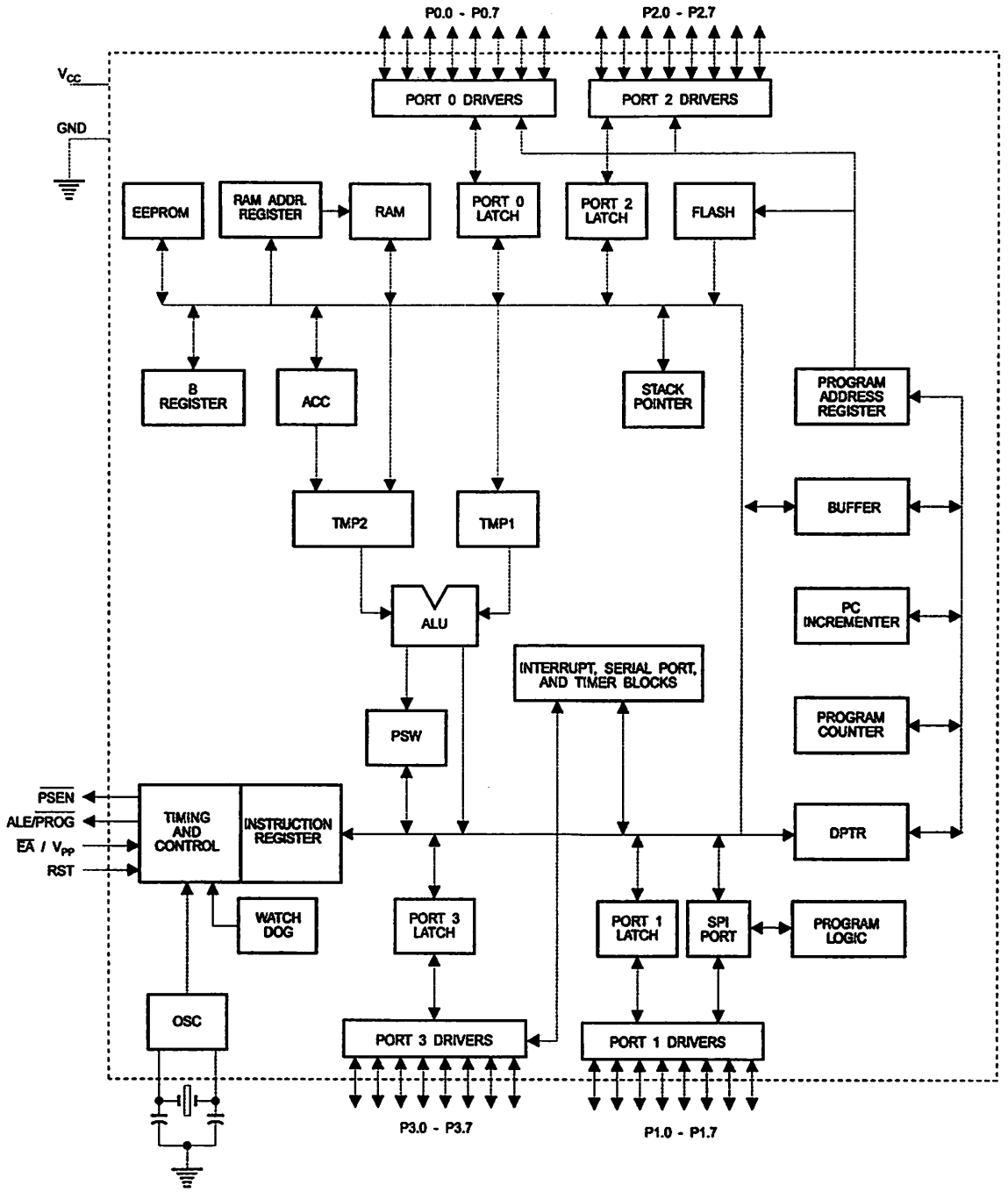
Port 0 can also be configured to be the multiplexed low-order address/data bus during accesses to external program and data memory. In this mode, P0 has internal pullups.

Port 0 also receives the code bytes during Flash programming and outputs the code bytes during program verification. External pullups are required during program verification.

Port 1
Port 1 is an 8-bit bidirectional I/O port with internal pullups. The Port 1 output buffers can sink/source four TTL inputs. When 1s are written to Port 1 pins, they are pulled high by the internal pullups and can be used as inputs. As inputs, Port 1 pins that are externally being pulled low will source current (I_{IL}) because of the internal pullups.

Some Port 1 pins provide additional functions. P1.0 and P1.1 can be configured to be the timer/counter 2 external count input (P1.0/T2) and the timer/counter 2 trigger input (P1.1/T2EX), respectively.

Block Diagram



Furthermore, P1.4, P1.5, P1.6, and P1.7 can be configured as the SPI slave port select, data input/output and shift clock input/output pins as shown in the following table.

Port Pin	Alternate Functions
P1.0	T2 (external count input to Timer/Counter 2), clock-out
P1.1	T2EX (Timer/Counter 2 capture/reload trigger and direction control)
P1.4	$\overline{SS}$ (Slave port select input)
P1.5	MOSI (Master data output, slave data input pin for SPI channel)
P1.6	MISO (Master data input, slave data output pin for SPI channel)
P1.7	SCK (Master clock output, slave clock input pin for SPI channel)

Port 1 also receives the low-order address bytes during Flash programming and verification.

Port 2

Port 2 is an 8-bit bidirectional I/O port with internal pullups. The Port 2 output buffers can sink/source four TTL inputs. When 1s are written to Port 2 pins, they are pulled high by the internal pullups and can be used as inputs. As inputs, Port 2 pins that are externally being pulled low will source current (I_{IL}) because of the internal pullups.

Port 2 emits the high-order address byte during fetches from external program memory and during accesses to external data memory that use 16-bit addresses (MOVX @ DPTR). In this application, Port 2 uses strong internal pullups when emitting 1s. During accesses to external data memory that use 8-bit addresses (MOVX @ RI), Port 2 emits the contents of the P2 Special Function Register.

Port 2 also receives the high-order address bits and some control signals during Flash programming and verification.

Port 3

Port 3 is an 8 bit bidirectional I/O port with internal pullups. The Port 3 output buffers can sink/source four TTL inputs. When 1s are written to Port 3 pins, they are pulled high by the internal pullups and can be used as inputs. As inputs, Port 3 pins that are externally being pulled low will source current (I_{IL}) because of the pullups.

Port 3 also serves the functions of various special features of the AT89S8252, as shown in the following table.

Port 3 also receives some control signals for Flash programming and verification.

Port Pin	Alternate Functions
P3.0	RXD (serial input port)
P3.1	TXD (serial output port)
P3.2	$\overline{INT0}$ (external interrupt 0)
P3.3	$\overline{INT1}$ (external interrupt 1)
P3.4	T0 (timer 0 external input)
P3.5	T1 (timer 1 external input)
P3.6	$\overline{WR}$ (external data memory write strobe)
P3.7	$\overline{RD}$ (external data memory read strobe)

RST

Reset input. A high on this pin for two machine cycles while the oscillator is running resets the device.

ALE/$\overline{PROG}$

Address Latch Enable is an output pulse for latching the low byte of the address during accesses to external memory. This pin is also the program pulse input ($\overline{PROG}$) during Flash programming.

In normal operation, ALE is emitted at a constant rate of 1/6 the oscillator frequency and may be used for external timing or clocking purposes. Note, however, that one ALE pulse is skipped during each access to external data memory.

If desired, ALE operation can be disabled by setting bit 0 of SFR location 8EH. With the bit set, ALE is active only during a MOVX or MOVC instruction. Otherwise, the pin is weakly pulled high. Setting the ALE-disable bit has no effect if the microcontroller is in external execution mode.

$\overline{PSEN}$

Program Store Enable is the read strobe to external program memory.

When the AT89S8252 is executing code from external program memory, $\overline{PSEN}$ is activated twice each machine cycle, except that two $\overline{PSEN}$ activations are skipped during each access to external data memory.

$\overline{EA}$/V_{PP}

External Access Enable. $\overline{EA}$ must be strapped to GND in order to enable the device to fetch code from external program memory locations starting at 0000H up to FFFFH. Note, however, that if lock bit 1 is programmed, $\overline{EA}$ will be internally latched on reset.

$\overline{EA}$ should be strapped to V_{CC} for internal program executions. This pin also receives the 12-volt programming enable voltage (V_{PP}) during Flash programming when 12-volt programming is selected.

XTAL1
Input to the inverting oscillator amplifier and input to the internal clock operating circuit.

XTAL2
Output from the inverting oscillator amplifier.

Special Function Registers

A map of the on-chip memory area called the Special Function Register (SFR) space is shown in Table 1.

Note that not all of the addresses are occupied, and unoccupied addresses may not be implemented on the chip. Read accesses to these addresses will in general return random data, and write accesses will have an indeterminate effect.

Table 1. AT89S8252 SFR Map and Reset Values

0F8H									0FFH
0F0H	B 00000000								0F7H
0E8H									0EFH
0E0H	ACC 00000000								0E7H
0D8H									0DFH
0D0H	PSW 00000000					SPCR 000001XX			0D7H
0C8H	T2CON 00000000	T2MOD XXXXXX00	RCAP2L 00000000	RCAP2H 00000000	TL2 00000000	TH2 00000000			0CFH
0C0H									0C7H
0B8H	IP XX000000								0BFH
0B0H	P3 11111111								0B7H
0A8H	IE 0X000000		SPSR 00XXXXXX						0AFH
0A0H	P2 11111111								0A7H
98H	SCON 00000000	SBUF XXXXXXXX							9FH
90H	P1 11111111						WMCON 00000010		97H
88H	TCON 00000000	TMOD 00000000	TL0 00000000	TL1 00000000	TH0 00000000	TH1 00000000			8FH
80H	P0 11111111	SP 00000111	DP0L 00000000	DP0H 00000000	DP1L 00000000	DP1H 00000000	SPDR XXXXXXXX	PCON 0XXX0000	87H

User software should not write 1s to these unlisted locations, since they may be used in future products to invoke new features. In that case, the reset or inactive values of the new bits will always be 0.

Timer 2 Registers Control and status bits are contained in registers T2CON (shown in Table 2) and T2MOD (shown in Table 9) for Timer 2. The register pair (RCAP2H, RCAP2L) are the Capture/Reload registers for Timer 2 in 16 bit capture mode or 16-bit auto-reload mode.

Watchdog and Memory Control Register The WMCON register contains control bits for the Watchdog Timer (shown in Table 3). The EEMEN and EEMWE bits are used to select the 2K bytes on-chip EEPROM, and to enable byte-write. The DPS bit selects one of two DPTR registers available.

SPI Registers Control and status bits for the Serial Peripheral Interface are contained in registers SPCR (shown in Table 4) and SPSR (shown in Table 5). The SPI data bits are contained in the SPDR register. Writing the SPI data register during serial data transfer sets the Write Collision bit, WCOL, in the SPSR register. The SPDR is double buffered for writing and the values in SPDR are not changed by Reset.

Interrupt Registers The global interrupt enable bit and the individual interrupt enable bits are in the IE register. In addition, the individual interrupt enable bit for the SPI is in the SPCR register. Two priorities can be set for each of the six interrupt sources in the IP register.

Table 2. T2CON—Timer/Counter 2 Control Register

T2CON Address = 0C8H — Reset Value = 0000 0000B

Bit Addressable

Bit	7	6	5	4	3	2	1	0
	TF2	EXF2	RCLK	TCLK	EXEN2	TR2	C/$\overline{T2}$	CP/$\overline{RL2}$

Symbol	Function
TF2	Timer 2 overflow flag set by a Timer 2 overflow and must be cleared by software. TF2 will not be set when either RCLK = 1 or TCLK = 1.
EXF2	Timer 2 external flag set when either a capture or reload is caused by a negative transition on T2EX and EXEN2 = 1. When Timer 2 interrupt is enabled, EXF2 = 1 will cause the CPU to vector to the Timer 2 interrupt routine. EXF2 must be cleared by software. EXF2 does not cause an interrupt in up/down counter mode (DCEN = 1).
RCLK	Receive clock enable. When set, causes the serial port to use Timer 2 overflow pulses for its receive clock in serial port Modes 1 and 3. RCLK = 0 causes Timer 1 overflows to be used for the receive clock.
TCLK	Transmit clock enable. When set, causes the serial port to use Timer 2 overflow pulses for its transmit clock in serial port Modes 1 and 3. TCLK = 0 causes Timer 1 overflows to be used for the transmit clock.
EXEN2	Timer 2 external enable. When set, allows a capture or reload to occur as a result of a negative transition on T2EX if Timer 2 is not being used to clock the serial port. EXEN2 = 0 causes Timer 2 to ignore events at T2EX.
TR2	Start/Stop control for Timer 2. TR2 = 1 starts the timer.
C/$\overline{T2}$	Timer or counter select for Timer 2. C/$\overline{T2}$ = 0 for timer function. C/$\overline{T2}$ = 1 for external event counter (falling edge triggered).
CP/$\overline{RL2}$	Capture/Reload select. CP/$\overline{RL2}$ = 1 causes captures to occur on negative transitions at T2EX if EXEN2 = 1. CP/$\overline{RL2}$ = 0 causes automatic reloads to occur when Timer 2 overflows or negative transitions occur at T2EX when EXEN2 = 1. When either RCLK or TCLK = 1, this bit is ignored and the timer is forced to auto-reload on Timer 2 overflow.

Dual Data Pointer Registers To facilitate accessing both internal EEPROM and external data memory, two banks of 16 bit Data Pointer Registers are provided: DP0 at SFR address locations 82H-83H and DP1 at 84H-85H. Bit DPS = 0 in SFR WMCON selects DP0 and DPS = 1 selects DP1. The user should always initialize the DPS bit to the appropriate value before accessing the respective Data Pointer Register.

Power Off Flag The Power Off Flag (POF) is located at bit_4 (PCON.4) in the PCON SFR. POF is set to "1" during power up. It can be set and reset under software control and is not affected by RESET.

Table 3. WMCON—Watchdog and Memory Control Register

WMCON Address = 96H — Reset Value = 0000 0010B

Bit	7	6	5	4	3	2	1	0
	PS2	PS1	PS0	EEMWE	EEMEN	DPS	WDTRST	WDTEN

Symbol	Function
PS2 PS1 PS0	Prescaler Bits for the Watchdog Timer. When all three bits are set to "0", the watchdog timer has a nominal period of 16 ms. When all three bits are set to "1", the nominal period is 2048 ms.
EEMWE	EEPROM Data Memory Write Enable Bit. Set this bit to "1" before initiating byte write to on-chip EEPROM with the MOVX instruction. User software should set this bit to "0" after EEPROM write is completed.
EEMEN	Internal EEPROM Access Enable. When EEMEN = 1, the MOVX instruction with DPTR will access on-chip EEPROM instead of external data memory. When EEMEN = 0, MOVX with DPTR accesses external data memory.
DPS	Data Pointer Register Select. DPS = 0 selects the first bank of Data Pointer Register, DP0, and DPS = 1 selects the second bank, DP1
WDTRST RDY/$\overline{BSY}$	Watchdog Timer Reset and EEPROM Ready/$\overline{Busy}$ Flag. Each time this bit is set to "1" by user software, a pulse is generated to reset the watchdog timer. The WDTRST bit is then automatically reset to "0" in the next instruction cycle. The WDTRST bit is Write-Only. This bit also serves as the RDY/$\overline{BSY}$ flag in a Read-Only mode during EEPROM write. RDY/$\overline{BSY}$ = 1 means that the EEPROM is ready to be programmed. While programming operations are being executed, the RDY/$\overline{BSY}$ bit equals "0" and is automatically reset to "1" when programming is completed.
WDTEN	Watchdog Timer Enable Bit. WDTEN = 1 enables the watchdog timer and WDTEN = 0 disables the watchdog timer.

Table 4. SPCR—SPI Control Register

SPCR Address = D5H — Reset Value = 0000 01XXB

Bit	7	6	5	4	3	2	1	0
	SPIE	SPE	DORD	MSTR	CPOL	CPHA	SPR1	SPR0

Symbol	Function
SPIE	SPI Interrupt Enable. This bit, in conjunction with the ES bit in the IE register, enables SPI interrupts: SPIE = 1 and ES = 1 enable SPI interrupts. SPIE = 0 disables SPI interrupts.
SPE	SPI Enable. SPI = 1 enables the SPI channel and connects $\overline{SS}$, MOSI, MISO and SCK to pins P1.4, P1.5, P1.6, and P1.7. SPI = 0 disables the SPI channel.
DORD	Data Order. DORD = 1 selects LSB first data transmission. DORD = 0 selects MSB first data transmission.
MSTR	Master/Slave Select. MSTR = 1 selects Master SPI mode. MSTR = 0 selects Slave SPI mode.
CPOL	Clock Polarity. When CPOL = 1, SCK is high when idle. When CPOL = 0, SCK of the master device is low when not transmitting. Please refer to figure on SPI Clock Phase and Polarity Control.
CPHA	Clock Phase. The CPHA bit together with the CPOL bit controls the clock and data relationship between master and slave. Please refer to figure on SPI Clock Phase and Polarity Control.
SPR0 SPR1	SPI Clock Rate Select. These two bits control the SCK rate of the device configured as master. SPR1 and SPR0 have no effect on the slave. The relationship between SCK and the oscillator frequency, $F_{osc.}$, is as follows: SPR1 SPR0 SCK = $F_{osc.}$ divided by 0 0 4 0 1 16 1 0 64 1 1 128

Table 5. SPSR—SPI Status Register

SPSR Address = AAH — Reset Value = 00XX XXXXB

Bit	7	6	5	4	3	2	1	0
	SPIF	WCOL	—	—	—	—	—	—

Symbol	Function
SPIF	SPI Interrupt Flag. When a serial transfer is complete, the SPIF bit is set and an interrupt is generated if SPIE = 1 and ES = 1. The SPIF bit is cleared by reading the SPI status register with SPIF and WCOL bits set, and then accessing the SPI data register.
WCOL	Write Collision Flag. The WCOL bit is set if the SPI data register is written during a data transfer. During data transfer, the result of reading the SPDR register may be incorrect, and writing to it has no effect. The WCOL bit (and the SPIF bit) are cleared by reading the SPI status register with SPIF and WCOL set, and then accessing the SPI data register.

Table 6. SPDR—SPI Data Register

SPDR Address = 86H — Reset Value = unchanged

Bit	SPD7	SPD6	SPD5	SPD4	SPD3	SPD2	SPD1	SPD0
	7	6	5	4	3	2	1	0

Data Memory—EEPROM and RAM

The AT89S8252 implements 2K bytes of on-chip EEPROM for data storage and 256 bytes of RAM. The upper 128 bytes of RAM occupy a parallel space to the Special Function Registers. That means the upper 128 bytes have the same addresses as the SFR space but are physically separate from SFR space.

When an instruction accesses an internal location above address 7FH, the address mode used in the instruction specifies whether the CPU accesses the upper 128 bytes of RAM or the SFR space. Instructions that use direct addressing access SFR space.

For example, the following direct addressing instruction accesses the SFR at location 0A0H (which is P2).

```
MOV 0A0H, #data
```

Instructions that use indirect addressing access the upper 128 bytes of RAM. For example, the following indirect addressing instruction, where R0 contains 0A0H, accesses the data byte at address 0A0H, rather than P2 (whose address is 0A0H).

```
MOV @R0, #data
```

Note that stack operations are examples of indirect addressing, so the upper 128 bytes of data RAM are available as stack space.

The on-chip EEPROM data memory is selected by setting the EEMEN bit in the WMCON register at SFR address location 96H. The EEPROM address range is from 000H to 7FFH. The MOVX instructions are used to access the EEPROM. To access off-chip data memory with the MOVX instructions, the EEMEN bit needs to be set to "0".

The EEMWE bit in the WMCON register needs to be set to "1" before any byte location in the EEPROM can be written. User software should reset EEMWE bit to "0" if no further EEPROM write is required. EEPROM write cycles in the serial programming mode are self-timed and typically take 2.5 ms. The progress of EEPROM write can be monitored by reading the RDY/$\overline{BSY}$ bit (read-only) in SFR WMCON. RDY/$\overline{BSY}$ = 0 means programming is still in progress and RDY/$\overline{BSY}$ = 1 means EEPROM write cycle is completed and another write cycle can be initiated.

In addition, during EEPROM programming, an attempted read from the EEPROM will fetch the byte being written with the MSB complemented. Once the write cycle is completed, true data are valid at all bit locations.

Programmable Watchdog Timer

The programmable Watchdog Timer (WDT) operates from an independent oscillator. The prescaler bits, PS0, PS1 and PS2 in SFR WMCON are used to set the period of the Watchdog Timer from 16 ms to 2048 ms. The available timer periods are shown in the following table and the actual timer periods (at V_{CC} = 5V) are within ±30% of the nominal.

The WDT is disabled by Power-on Reset and during Power Down. It is enabled by setting the WDTEN bit in SFR WMCON (address = 96H). The WDT is reset by setting the WDTRST bit in WMCON. When the WDT times out without being reset or disabled, an internal RST pulse is generated to reset the CPU.

Table 7. Watchdog Timer Period Selection

WDT Prescaler Bits			Period (nominal)
PS2	PS1	PS0	
0	0	0	16 ms
0	0	1	32 ms
0	1	0	64 ms
0	1	1	128 ms
1	0	0	256 ms
1	0	1	512 ms
1	1	0	1024 ms
1	1	1	2048 ms

Timer 0 and 1

Timer 0 and Timer 1 in the AT89S8252 operate the same way as Timer 0 and Timer 1 in the AT89C51, AT89C52 and AT89C55. For further information, see the October 1995 Microcontroller Data Book, page 2-45, section titled, "Timer/Counters."

Timer 2

Timer 2 is a 16 bit Timer/Counter that can operate as either a timer or an event counter. The type of operation is selected by bit C/$\overline{T2}$ in the SFR T2CON (shown in Table 2). Timer 2 has three operating modes: capture, auto-reload (up or down counting), and baud rate generator. The modes are selected by bits in T2CON, as shown in Table 8.

Timer 2 consists of two 8-bit registers, TH2 and TL2. In the Timer function, the TL2 register is incremented every machine cycle. Since a machine cycle consists of 12 oscillator periods, the count rate is 1/12 of the oscillator frequency.

In the Counter function, the register is incremented in response to a 1-to-0 transition at its corresponding external input pin, T2. In this function, the external input is sampled during S5P2 of every machine cycle. When the samples show a high in one cycle and a low in the next cycle, the count is incremented. The new count value appears in the register during S3P1 of the cycle following the one in which the transition was detected. Since two machine cycles (24 oscillator periods) are required to recognize a 1-to-0 transition, the maximum count rate is 1/24 of the oscillator frequency. To ensure that a given level is sampled at least once before it changes, the level should be held for at least one full machine cycle.

Table 8. Timer 2 Operating Modes

RCLK + TCLK	CP/$\overline{RL2}$	TR2	MODE
0	0	1	16-bit Auto-Reload
0	1	1	16-bit Capture
1	X	1	Baud Rate Generator
X	X	0	(Off)

Capture Mode

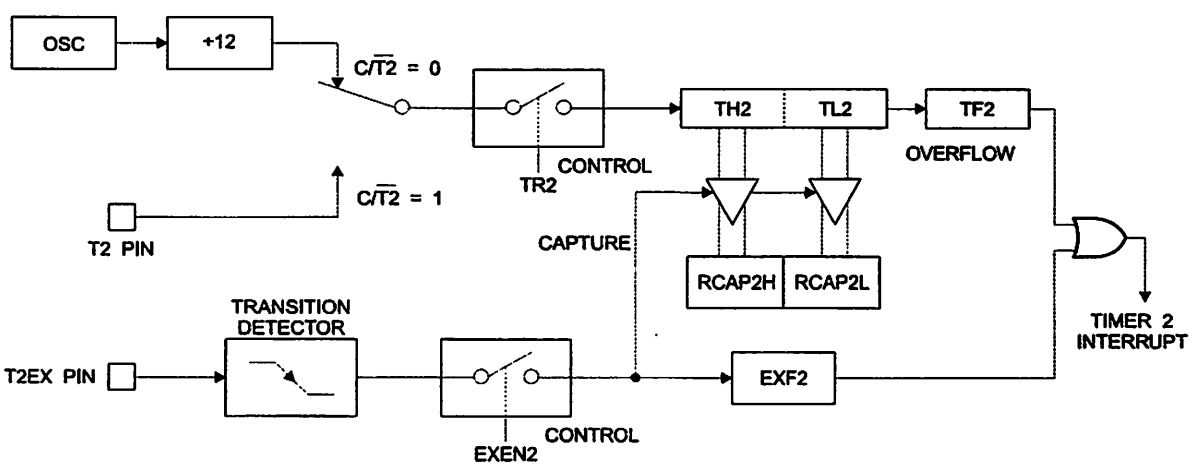
In the capture mode, two options are selected by bit EXEN2 in T2CON. If EXEN2 = 0, Timer 2 is a 16 bit timer or counter which upon overflow sets bit TF2 in T2CON. This bit can then be used to generate an interrupt. If EXEN2 = 1, Timer 2 performs the same operation, but a 1-to-0 transition at external input T2EX also causes the current value in TH2 and TL2 to be captured into RCAP2H and RCAP2L, respectively. In addition, the transition at T2EX causes bit EXF2 in T2CON to be set. The EXF2 bit, like TF2, can generate an interrupt. The capture mode is illustrated in Figure 1.

Auto-Reload (Up or Down Counter)

Timer 2 can be programmed to count up or down when configured in its 16 bit auto-reload mode. This feature is invoked by the DCEN (Down Counter Enable) bit located in the SFR T2MOD (see Table 9). Upon reset, the DCEN bit is set to 0 so that timer 2 will default to count up. When DCEN is set, Timer 2 can count up or down, depending on the value of the T2EX pin.

Figure 2 shows Timer 2 automatically counting up when DCEN = 0. In this mode, two options are selected by bit EXEN2 in T2CON. If EXEN2 = 0, Timer 2 counts up to

Figure 1. Timer 2 in Capture Mode



0FFFFH and then sets the TF2 bit upon overflow. The overflow also causes the timer registers to be reloaded with the 16 bit value in RCAP2H and RCAP2L. The values in RCAP2H and RCAP2L are preset by software. If EXEN2 = 1, a 16 bit reload can be triggered either by an overflow or by a 1-to-0 transition at external input T2EX. This transition also sets the EXF2 bit. Both the TF2 and EXF2 bits can generate an interrupt if enabled.

Setting the DCEN bit enables Timer 2 to count up or down, as shown in Figure 3. In this mode, the T2EX pin controls the direction of the count. A logic 1 at T2EX makes Timer 2 count up. The timer will overflow at 0FFFFH and set the TF2 bit. This overflow also causes the 16 bit value in RCAP2H and RCAP2L to be reloaded into the timer registers, TH2 and TL2, respectively.

A logic 0 at T2EX makes Timer 2 count down. The timer underflows when TH2 and TL2 equal the values stored in RCAP2H and RCAP2L. The underflow sets the TF2 bit and causes 0FFFFH to be reloaded into the timer registers.

The EXF2 bit toggles whenever Timer 2 overflows or underflows and can be used as a 17th bit of resolution. In this operating mode, EXF2 does not flag an interrupt.

Figure 2. Timer 2 in Auto Reload Mode (DCEN = 0)

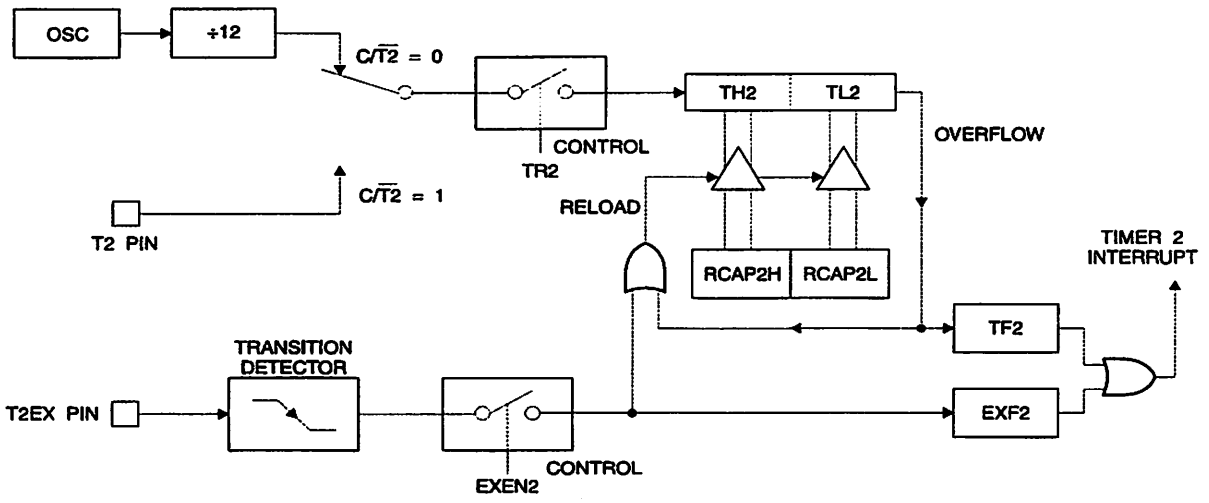


Table 9. T2MOD—Timer 2 Mode Control Register

T2MOD Address = 0C9H — Reset Value = XXXX XX00B

Not Bit Addressable

	—	—	—	—	—	—	T2OE	DCEN
Bit	7	6	5	4	3	2	1	0

Symbol	Function
—	Not implemented, reserved for future use.
T2OE	Timer 2 Output Enable bit.
DCEN	When set, this bit allows Timer 2 to be configured as an up/down counter.

Figure 3. Timer 2 Auto Reload Mode (DCEN = 1)

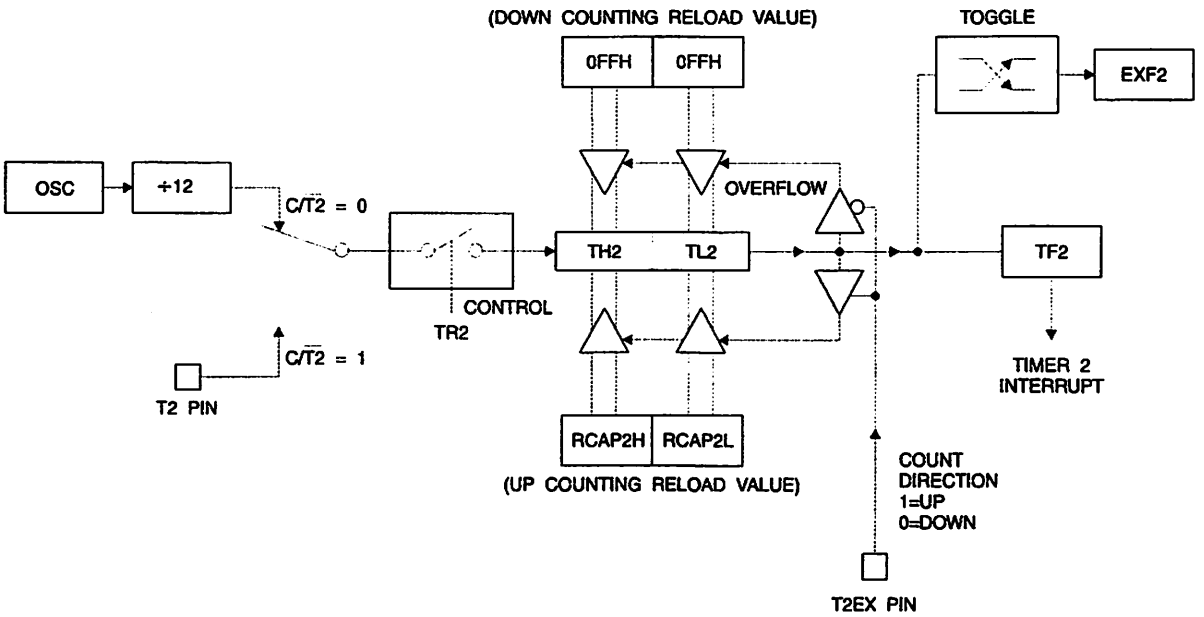
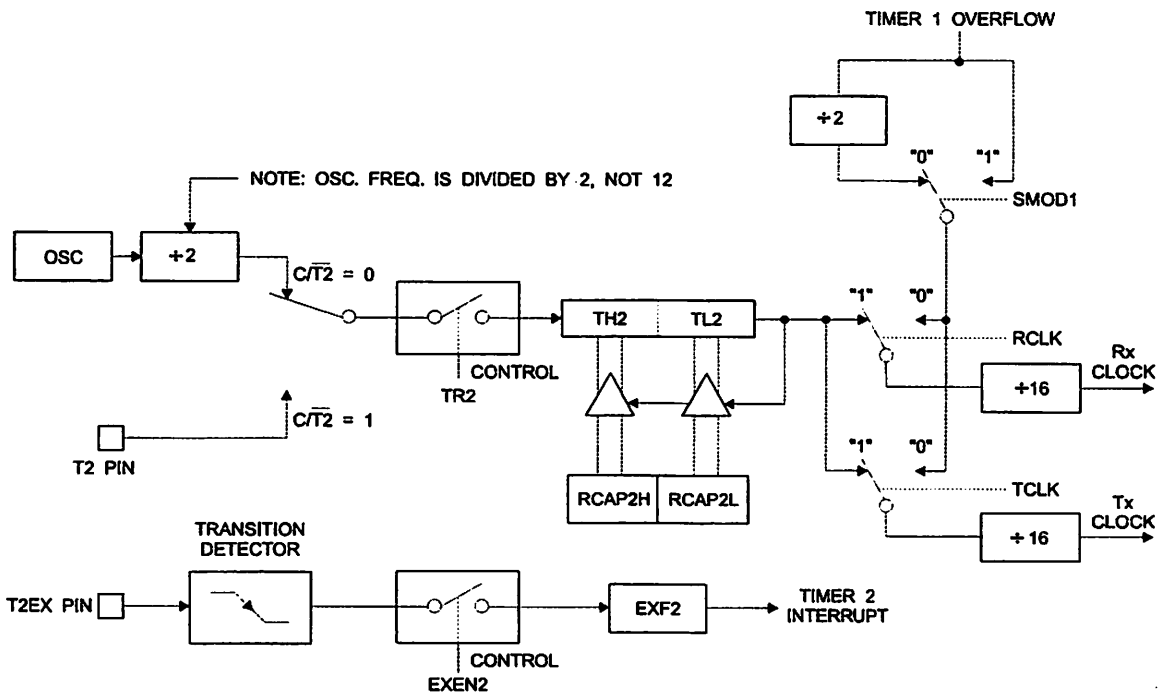


Figure 4. Timer 2 in Baud Rate Generator Mode



Baud Rate Generator

Timer 2 is selected as the baud rate generator by setting TCLK and/or RCLK in T2CON (Table 2). Note that the baud rates for transmit and receive can be different if Timer 2 is used for the receiver or transmitter and Timer 1 is used for the other function. Setting RCLK and/or TCLK puts Timer 2 into its baud rate generator mode, as shown in Figure 4.

The baud rate generator mode is similar to the auto-reload mode, in that a rollover in TH2 causes the Timer 2 registers to be reloaded with the 16 bit value in registers RCAP2H and RCAP2L, which are preset by software.

The baud rates in Modes 1 and 3 are determined by Timer 2's overflow rate according to the following equation.

$$\text{Modes 1 and 3 Baud Rates} = \frac{\text{Timer 2 Overflow Rate}}{16}$$

The Timer can be configured for either timer or counter operation. In most applications, it is configured for timer operation ($C/\overline{T2} = 0$). The timer operation is different for Timer 2 when it is used as a baud rate generator. Normally, as a timer, it increments every machine cycle (at 1/12 the oscillator frequency). As a baud rate generator, however, it increments every state time (at 1/2 the oscillator frequency). The baud rate formula is given below.

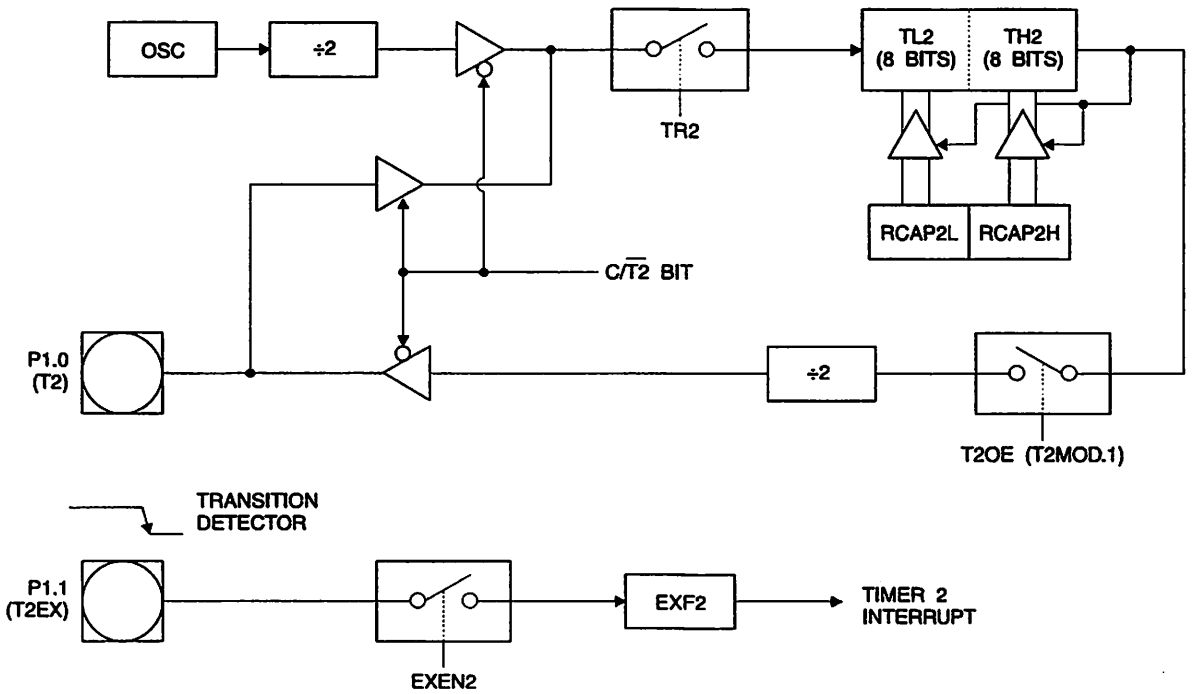
$$\frac{\text{Modes 1 and 3}}{\text{Baud Rate}} = \frac{\text{Oscillator Frequency}}{32 \times [65536 - (\text{RCAP2H,RCAP2L})]}$$

where (RCAP2H, RCAP2L) is the content of RCAP2H and RCAP2L taken as a 16 bit unsigned integer.

Timer 2 as a baud rate generator is shown in Figure 4. This figure is valid only if RCLK or TCLK = 1 in T2CON. Note that a rollover in TH2 does not set TF2 and will not generate an interrupt. Note too, that if EXEN2 is set, a 1-to-0 transition in T2EX will set EXF2 but will not cause a reload from (RCAP2H, RCAP2L) to (TH2, TL2). Thus when Timer 2 is in use as a baud rate generator, T2EX can be used as an extra external interrupt.

Note that when Timer 2 is running (TR2 = 1) as a timer in the baud rate generator mode, TH2 or TL2 should not be read from or written to. Under these conditions, the Timer is incremented every state time, and the results of a read or write may not be accurate. The RCAP2 registers may be read but should not be written to, because a write might overlap a reload and cause write and/or reload errors. The timer should be turned off (clear TR2) before accessing the Timer 2 or RCAP2 registers.

Figure 5. Timer 2 In Clock-Out Mode



Programmable Clock Out

A 50% duty cycle clock can be programmed to come out on P1.0, as shown in Figure 5. This pin, besides being a regular I/0 pin, has two alternate functions. It can be programmed to input the external clock for Timer/Counter 2 or to output a 50% duty cycle clock ranging from 61 Hz to 4 MHz at a 16 MHz operating frequency.

To configure the Timer/Counter 2 as a clock generator, bit C/$\overline{T2}$ (T2CON.1) must be cleared and bit T2OE (T2MOD.1) must be set. Bit TR2 (T2CON.2) starts and stops the timer.

The clock-out frequency depends on the oscillator frequency and the reload value of Timer 2 capture registers (RCAP2H, RCAP2L), as shown in the following equation.

$$\text{Clock Out Frequency} = \frac{\text{Oscillator Frequency}}{4 \times [65536 - (\text{RCAP2H,RCAP2L})]}$$

In the clock-out mode, Timer 2 rollovers will not generate an interrupt. This behavior is similar to when Timer 2 is used as a baud-rate generator. It is possible to use Timer 2 as a baud-rate generator and a clock generator simultaneously. Note, however, that the baud-rate and clock-out frequencies cannot be determined independently from one another since they both use RCAP2H and RCAP2L.

UART

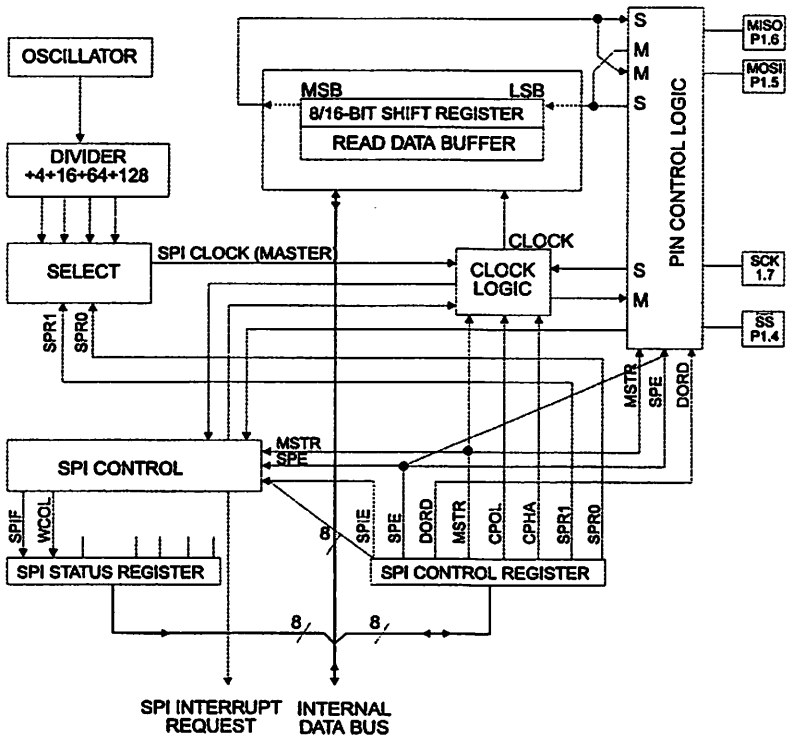
The UART in the AT89S8252 operates the same way as the UART in the AT89C51, AT89C52 and AT89C55. For further information, see the October 1995 Microcontroller Data Book, page 2-49, section titled, "Serial Interface."

Serial Peripheral Interface

The serial peripheral interface (SPI) allows high-speed synchronous data transfer between the AT89S8252 and peripheral devices or between several AT89S8252 devices. The AT89S8252 SPI features include the following:

- Full-Duplex, 3-Wire Synchronous Data Transfer
- Master or Slave Operation
- 1.5-MHz Bit Frequency (max.)
- LSB First or MSB First Data Transfer
- Four Programmable Bit Rates
- End of Transmission Interrupt Flag
- Write Collision Flag Protection
- Wakeup from Idle Mode (Slave Mode Only)

Figure 6. SPI Block Diagram



The interconnection between master and slave CPUs with SPI is shown in the following figure. The SCK pin is the clock output in the master mode but is the clock input in the slave mode. Writing to the SPI data register of the master CPU starts the SPI clock generator, and the data written shifts out of the MOSI pin and into the MOSI pin of the slave CPU. After shifting one byte, the SPI clock generator stops, setting the end of transmission flag (SPIF). If both the SPI interrupt enable bit (SPIE) and the serial port interrupt enable bit (ES) are set, an interrupt is requested.

The Slave Select input, $\overline{SS}$/P1.4, is set low to select an individual SPI device as a slave. When $\overline{SS}$/P1.4 is set high, the SPI port is deactivated and the MOSI/P1.5 pin can be used as an input.

There are four combinations of SCK phase and polarity with respect to serial data, which are determined by control bits CPHA and CPOL. The SPI data transfer formats are shown in Figures 8 and 9.

Figure 7. SPI Master-Slave Interconnection

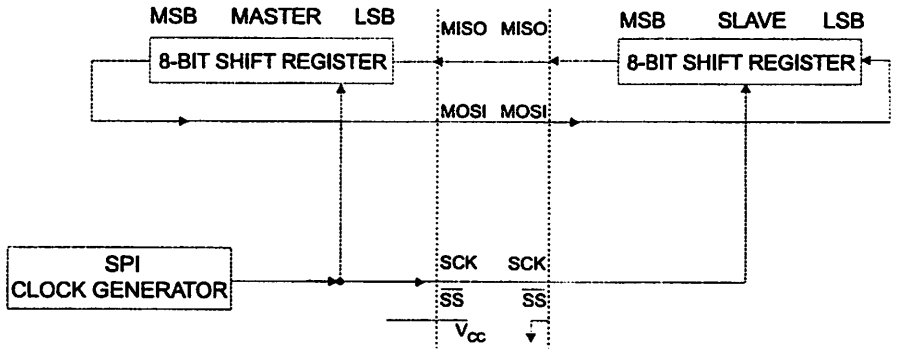
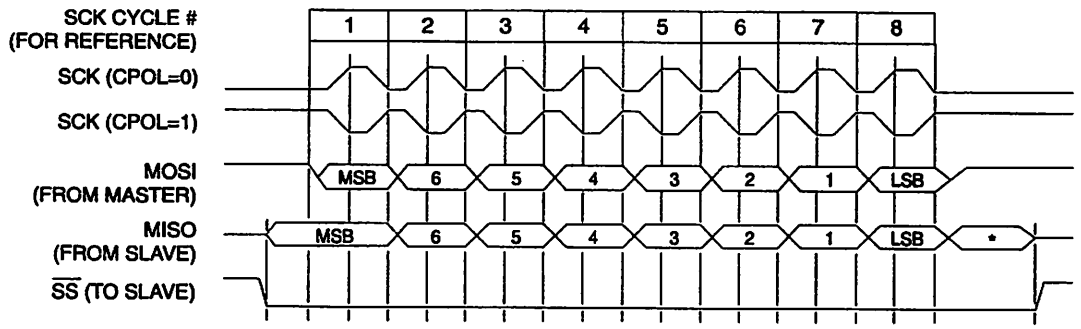
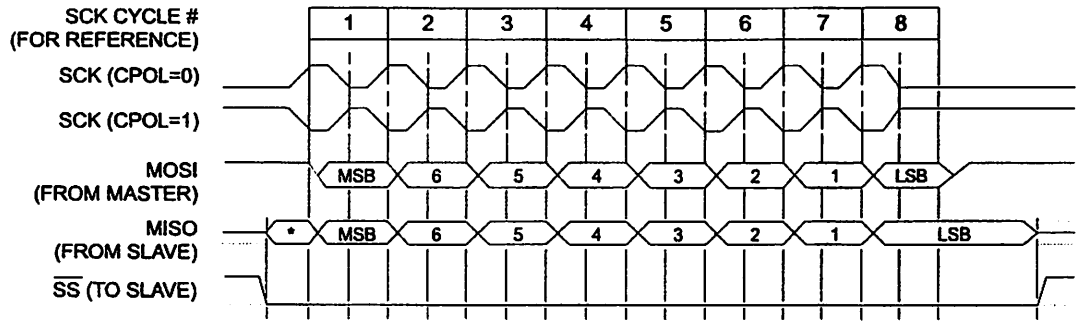


Figure 8. SPI transfer Format with CPHA = 0



*Not defined but normally MSB of character just received

igure 9. SPI Transfer Format with CPHA = 1



Not defined but normally LSB of previously transmitted character

nterrupts

he AT89S8252 has a total of six interrupt vectors: two xternal interrupts ($\overline{INT0}$ and $\overline{INT1}$), three timer interrupts Timers 0, 1, and 2), and the serial port interrupt. These iterrupts are all shown in Figure 10.

ach of these interrupt sources can be individually enabled r disabled by setting or clearing a bit in Special Function egister IE. IE also contains a global disable bit, EA, which isables all interrupts at once.

lote that Table 10 shows that bit position IE.6 is unimplemented. In the AT89C51, bit position IE.5 is also unimplemented. User software should not write 1s to these bit positions, since they may be used in future AT89 products.

Timer 2 interrupt is generated by the logical OR of bits TF2 and EXF2 in register T2CON. Neither of these flags is cleared by hardware when the service routine is vectored to. In fact, the service routine may have to determine whether it was TF2 or EXF2 that generated the interrupt, and that bit will have to be cleared in software.

The Timer 0 and Timer 1 flags, TF0 and TF1, are set at S5P2 of the cycle in which the timers overflow. The values are then polled by the circuitry in the next cycle. However, the Timer 2 flag, TF2, is set at S2P2 and is polled in the same cycle in which the timer overflows.

able 10. Interrupt Enable (IE) Register

(MSB) (LSB)

EA	—	ET2	ES	ET1	EX1	ET0	EX0

Enable Bit = 1 enables the interrupt.

Enable Bit = 0 disables the interrupt.

Symbol	Position	Function
EA	IE.7	Disables all interrupts. If EA = 0, no interrupt is acknowledged. If EA = 1, each interrupt source is individually enabled or disabled by setting or clearing its enable bit.
—	IE.6	Reserved.
ET2	IE.5	Timer 2 interrupt enable bit.
ES	IE.4	SPI and UART interrupt enable bit.
ET1	IE.3	Timer 1 interrupt enable bit.
EX1	IE.2	External interrupt 1 enable bit.
ET0	IE.1	Timer 0 interrupt enable bit.
EX0	IE.0	External interrupt 0 enable bit.

User software should never write 1s to unimplemented bits, because they may be used in future AT89 products.

Figure 10. Interrupt Sources

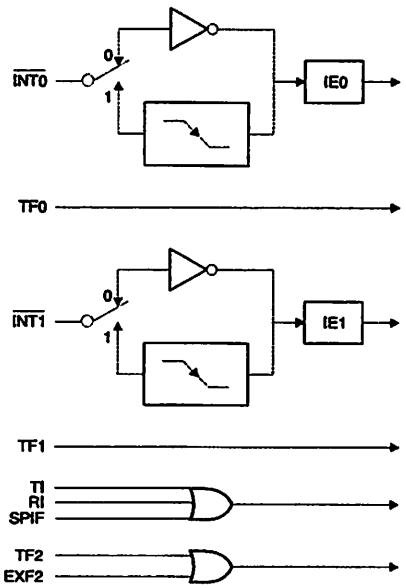


Figure 11. Oscillator Connections

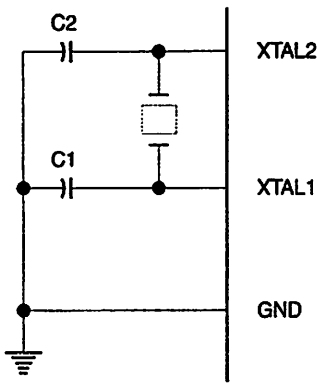
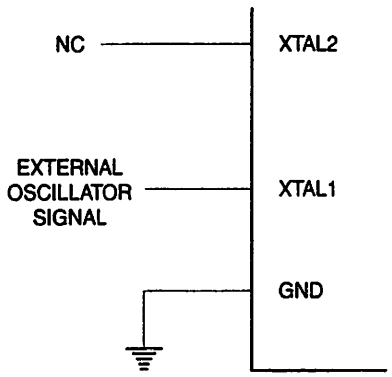


Figure 12. External Clock Drive Configuration



Note: Note: C1, C2 = 30 pF ± 10 pF for Crystals
= 40 pF ± 10 pF for Ceramic Resonators

Oscillator Characteristics

XTAL1 and XTAL2 are the input and output, respectively, of an inverting amplifier that can be configured for use as an on-chip oscillator, as shown in Figure 11. Either a quartz crystal or ceramic resonator may be used. To drive the device from an external clock source, XTAL2 should be left unconnected while XTAL1 is driven, as shown in Figure 12. There are no requirements on the duty cycle of the external clock signal, since the input to the internal clocking circuitry is through a divide-by-two flip-flop, but minimum and maximum voltage high and low time specifications must be observed.

Idle Mode

In idle mode, the CPU puts itself to sleep while all the on-chip peripherals remain active. The mode is invoked by software. The content of the on-chip RAM and all the special functions registers remain unchanged during this mode. The idle mode can be terminated by any enabled interrupt or by a hardware reset.

Note that when idle mode is terminated by a hardware reset, the device normally resumes program execution from where it left off, up to two machine cycles before the internal reset algorithm takes control. On-chip hardware inhibits access to internal RAM in this event, but access to the port pins is not inhibited. To eliminate the possibility of an unexpected write to a port pin when idle mode is terminated by a reset, the instruction following the one that invokes idle mode should not write to a port pin or to external memory.

Power Down Mode

In the power down mode, the oscillator is stopped and the instruction that invokes power down is the last instruction executed. The on-chip RAM and Special Function Registers retain their values until the power down mode is terminated. Exit from power down can be initiated either by a hardware reset or by an enabled external interrupt. Reset redefines the SFRs but does not change the on-chip RAM. The reset should not be activated before V_{CC} is restored to its normal operating level and must be held active long enough to allow the oscillator to restart and stabilize.

To exit power down via an interrupt, the external interrupt must be enabled as level sensitive before entering power down. The interrupt service routine starts at 16 ms (nominal) after the enabled interrupt pin is activated.

Status of External Pins During Idle and Power Down Modes

Mode	Program Memory	ALE	$\overline{PSEN}$	PORT0	PORT1	PORT2	PORT3
Idle	Internal	1	1	Data	Data	Data	Data
Idle	External	1	1	Float	Data	Address	Data
Power Down	Internal	0	0	Data	Data	Data	Data
Power Down	External	0	0	Float	Data	Data	Data

Program Memory Lock Bits

The AT89S8252 has three lock bits that can be left unprogrammed (U) or can be programmed (P) to obtain the additional features listed in the following table.

When lock bit 1 is programmed, the logic level at the $\overline{EA}$ pin is sampled and latched during reset. If the device is powered up without a reset, the latch initializes to a random value and holds that value until reset is activated. The latched value of $\overline{EA}$ must agree with the current logic level at that pin in order for the device to function properly.

Once programmed, the lock bits can only be unprogrammed with the Chip Erase operations in either the parallel or serial modes.

Lock Bit Protection Modes[1][2]

Program Lock Bits				Protection Type
	LB1	LB2	LB3	
1	U	U	U	No internal memory lock feature.
2	P	U	U	MOVC instructions executed from external program memory are disabled from fetching code bytes from internal memory. $\overline{EA}$ is sampled and latched on reset and further programming of the Flash memory (parallel or serial mode) is disabled.
3	P	P	U	Same as Mode 2, but parallel or serial verify are also disabled.
4	P	P	P	Same as Mode 3, but external execution is also disabled.

Notes: 1. U = Unprogrammed
2. P = Programmed

Programming the Flash and EEPROM

Atmel's AT89S8252 Flash Microcontroller offers 8K bytes of in-system reprogrammable Flash Code memory and 2K bytes of EEPROM Data memory.

The AT89S8252 is normally shipped with the on-chip Flash Code and EEPROM Data memory arrays in the erased state (i.e. contents = FFH) and ready to be programmed. This device supports a High-Voltage (12V) Parallel programming mode and a Low-Voltage (5V) Serial programming mode. The serial programming mode provides a convenient way to download the AT89S8252 inside the user's system. The parallel programming mode is compatible with conventional third party Flash or EPROM programmers.

The Code and Data memory arrays are mapped via separate address spaces in the serial programming mode. In the parallel programming mode, the two arrays occupy one contiguous address space: 0000H to 1FFFH for the Code array and 2000H to 27FFH for the Data array.

The Code and Data memory arrays on the AT89S8252 are programmed byte-by-byte in either programming mode. An auto-erase cycle is provided with the self-timed programming operation in the serial programming mode. There is no need to perform the Chip Erase operation to reprogram any memory location in the serial programming mode unless any of the lock bits have been programmed.

In the parallel programming mode, there is no auto-erase cycle. To reprogram any non-blank byte, the user needs to use the Chip Erase operation first to erase both arrays.

Parallel Programming Algorithm

To program and verify the AT89S8252 in the parallel programming mode, the following sequence is recommended:

1. Power-up sequence:
   Apply power between V_{CC} and GND pins.
   Set RST pin to "H".
   Apply a 3 MHz to 24 MHz clock to XTAL1 pin and wait for at least 10 milliseconds.
2. Set $\overline{PSEN}$ pin to "L"
   ALE pin to "H"
   $\overline{EA}$ pin to "H" and all other pins to "H".
3. Apply the appropriate combination of "H" or "L" logic levels to pins P2.6, P2.7, P3.6, P3.7 to select one of the programming operations shown in the Flash Programming Modes table.
4. Apply the desired byte address to pins P1.0 to P1.7 and P2.0 to P2.5.
   Apply data to pins P0.0 to P0.7 for Write Code operation.
5. Raise $\overline{EA}/V_{PP}$ to 12V to enable Flash programming, erase or verification.
6. Pulse ALE/$\overline{PROG}$ once to program a byte in the Code memory array, the Data memory array or the lock bits. The byte-write cycle is self-timed and typically takes 1.5 ms.
7. To verify the byte just programmed, bring pin P2.7 to "L" and read the programmed data at pins P0.0 to P0.7.

8. Repeat steps 3 through 7 changing the address and data for the entire 2K or 8K bytes array or until the end of the object file is reached.
9. Power-off sequence:

   Set XTAL1 to "L".

   Set RST and $\overline{EA}$ pins to "L".

   Turn V_{CC} power off.

In the parallel programming mode, there is no auto-erase cycle and to reprogram any non-blank byte, the user needs to use the Chip Erase operation first to erase both arrays.

$\overline{DATA}$ Polling

The AT89S8252 features $\overline{DATA}$ Polling to indicate the end of a write cycle. During a write cycle in the parallel or serial programming mode, an attempted read of the last byte written will result in the complement of the written datum on P0.7 (parallel mode), and on the MSB of the serial output byte on MISO (serial mode). Once the write cycle has been completed, true data are valid on all outputs, and the next cycle may begin. $\overline{DATA}$ Polling may begin any time after a write cycle has been initiated.

Ready/$\overline{Busy}$

The progress of byte programming in the parallel programming mode can also be monitored by the RDY/$\overline{BSY}$ output signal. Pin P3.4 is pulled Low after ALE goes High during programming to indicate $\overline{BUSY}$. P3.4 is pulled High again when programming is done to indicate READY.

Program Verify

If lock bits LB1 and LB2 have not been programmed, the programmed Code or Data byte can be read back via the address and data lines for verification. The state of the lock bits can also be verified directly in the parallel programming mode. In the serial programming mode, the state of the lock bits can only be verified indirectly by observing that the lock bit features are enabled.

Chip Erase

Both Flash and EEPROM arrays are erased electrically at the same time. In the parallel programming mode, chip erase is initiated by using the proper combination of control signals and by holding ALE/$\overline{PROG}$ low for 10 ms. The Code and Data arrays are written with all "1"s in the Chip Erase operation.

In the serial programming mode, a chip erase operation is initiated by issuing the Chip Erase instruction. In this mode, chip erase is self-timed and takes about 16 ms.

During chip erase, a serial read from any address location will return 00H at the data outputs.

Serial Programming Fuse

A programmable fuse is available to disable Serial Programming if the user needs maximum system security. The Serial Programming Fuse can only be programmed or erased in the Parallel Programming Mode.

The AT89S8252 is shipped with the Serial Programming Mode enabled.

Reading the Signature Bytes: The signature bytes are read by the same procedure as a normal verification of locations 030H and 031H, except that P3.6 and P3.7 must be pulled to a logic low. The values returned are as follows:

(030H) = 1EH indicates manufactured by Atmel
(031H) = 72H indicates 89S8252

Programming Interface

Every code byte in the Flash and EEPROM arrays can be written, and the entire array can be erased, by using the appropriate combination of control signals. The write operation cycle is self-timed and once initiated, will automatically time itself to completion.

All major programming vendors offer worldwide support for the Atmel microcontroller series. Please contact your local programming vendor for the appropriate software revision.

Serial Downloading

Both the Code and Data memory arrays can be programmed using the serial SPI bus while RST is pulled to V_{CC}. The serial interface consists of pins SCK, MOSI (input) and MISO (output). After RST is set high, the Programming Enable instruction needs to be executed first before program/erase operations can be executed.

An auto-erase cycle is built into the self-timed programming operation (in the serial mode ONLY) and there is no need to first execute the Chip Erase instruction unless any of the lock bits have been programmed. The Chip Erase operation turns the content of every memory location in both the Code and Data arrays into FFH.

The Code and Data memory arrays have separate address spaces:

0000H to 1FFFH for Code memory and 000H to 7FFH for Data memory.

Either an external system clock is supplied at pin XTAL1 or a crystal needs to be connected across pins XTAL1 and XTAL2. The maximum serial clock (SCK) frequency should be less than 1/40 of the crystal frequency. With a 24 MHz oscillator clock, the maximum SCK frequency is 600 kHz.

erial Programming Algorithm

o program and verify the AT89S8252 in the serial programming mode, the following sequence is recommended:

. Power-up sequence:

Apply power between V_{CC} and GND pins.

Set RST pin to "H".

If a crystal is not connected across pins XTAL1 and XTAL2, apply a 3 MHz to 24 MHz clock to XTAL1 pin and wait for at least 10 milliseconds.

. Enable serial programming by sending the Programming Enable serial instruction to pin MOSI/P1.5. The frequency of the shift clock supplied at pin SCK/P1.7 needs to be less than the CPU clock at XTAL1 divided by 40.

. The Code or Data array is programmed one byte at a time by supplying the address and data together with the appropriate Write instruction. The selected memory location is first automatically erased before new data is written. The write cycle is self-timed and typically takes less than 2.5 ms at 5V.

4. Any memory location can be verified by using the Read instruction which returns the content at the selected address at serial output MISO/P1.6.

5. At the end of a programming session, RST can be set low to commence normal operation.

Power-off sequence (if needed):

Set XTAL1 to "L" (if a crystal is not used).

Set RST to "L".

Turn V_{CC} power off.

Serial Programming Instruction

The Instruction Set for Serial Programming follows a 3-byte protocol and is shown in the following table:

nstruction Set

Instruction	Input Format			Operation
	Byte 1	Byte 2	Byte 3	
Programming Enable	1010 1100	0101 0011	xxxx xxxx	Enable serial programming interface after RST goes high.
Chip Erase	1010 1100	xxxx x100	xxxx xxxx	Chip erase both 8K & 2K memory arrays.
Read Code Memory	aaaa a001	low addr	xxxx xxxx	Read data from Code memory array at the selected address. The 5 MSBs of the first byte are the high order address bits. The low order address bits are in the second byte. Data are available at pin MISO during the third byte.
Write Code Memory	aaaa a010	low addr	data in	Write data to Code memory location at selected address. The address bits are the 5 MSBs of the first byte together with the second byte.
Read Data Memory	00aa a101	low addr	xxxx xxxx	Read data from Data memory array at selected address. Data are available at pin MISO during the third byte.
Write Data Memory	00aa a110	low addr	data in	Write data to Data memory location at selected address.
Write Lock Bits	1010 1100	LB1 LB2 LB3 x x111	xxxx xxxx	Write lock bits. Set LB1, LB2 or LB3 = "0" to program lock bits.

otes: 1. $\overline{\text{DATA}}$ polling is used to indicate the end of a write cycle which typically takes less than 2.5 ms at 5V.
2. "aaaaa" = high order address.
3. "x" = don't care.

Flash and EEPROM Parallel Programming Modes

Mode	RST	$\overline{PSEN}$	ALE/$\overline{PROG}$	$\overline{EA}$/V_{PP}	P2.6	P2.7	P3.6	P3.7	Data I/O P0.7:0	Address P2.5:0 P1.7:0
Serial Prog. Modes	H	h[1]	h[1]	x						
Chip Erase	H	L	⌐‾_/‾¬ [2]	12V	H	L	L	L	X	X
Write (10K bytes) Memory	H	L	⌐‾_/‾¬	12V	L	H	H	H	DIN	ADDR
Read (10K bytes) Memory	H	L	H	12V	L	L	H	H	DOUT	ADDR
Write Lock Bits:	H	L	⌐‾_/‾¬	12V	H	L	H	L	DIN	X
Bit - 1									P0.7 = 0	X
Bit - 2									P0.6 = 0	X
Bit - 3									P0.5 = 0	X
Read Lock Bits:	H	L	H	12V	H	H	L	L	DOUT	X
Bit - 1									@P0.2	X
Bit - 2									@P0.1	X
Bit - 3									@P0.0	X
Read Atmel Code	H	L	H	12V	L	L	L	L	DOUT	30H
Read Device Code	H	L	H	12V	L	L	L	L	DOUT	31H
Serial Prog. Enable	H	L	⌐‾_/‾¬ [2]	12V	L	H	L	H	P0.0 = 0	X
Serial Prog. Disable	H	L	⌐‾_/‾¬ [2]	12V	L	H	L	H	P0.0 = 1	X
Read Serial Prog. Fuse	H	L	H	12V	H	H	L	H	@P0.0	X

Notes:
1. "h" = weakly pulled "High" internally.
2. Chip Erase and Serial Programming Fuse require a 10-ms $\overline{PROG}$ pulse. Chip Erase needs to be performed first before reprogramming any byte with a content other than FFH.
3. P3.4 is pulled Low during programming to indicate RDY/$\overline{BSY}$.
4. "X" = don't care

Figure 14. Programming the Flash/EEPROM Memory

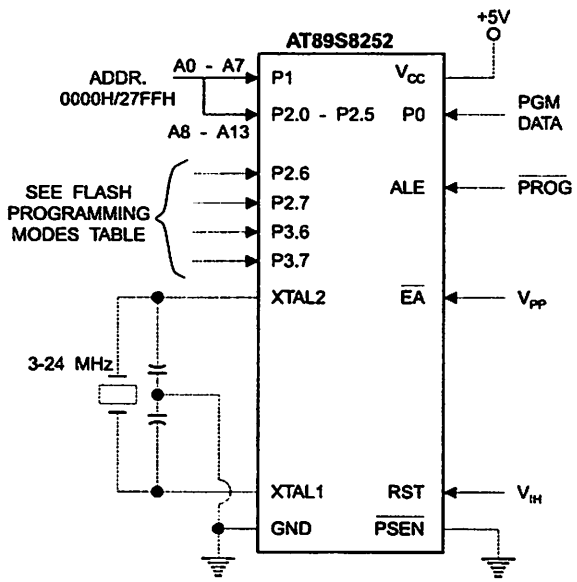


Figure 15. Flash/EEPROM Serial Downloading

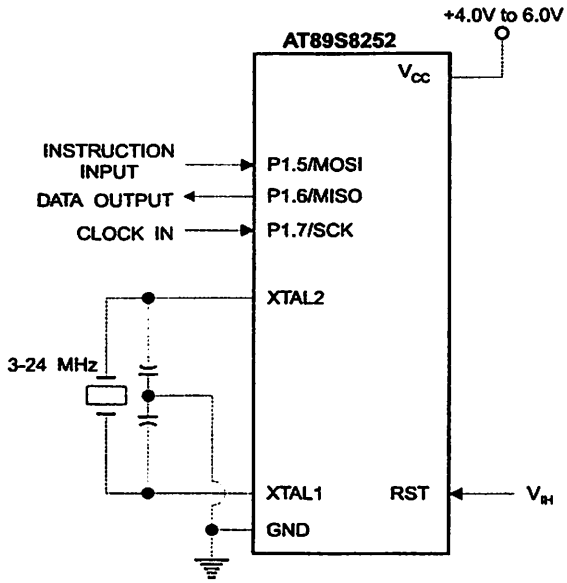
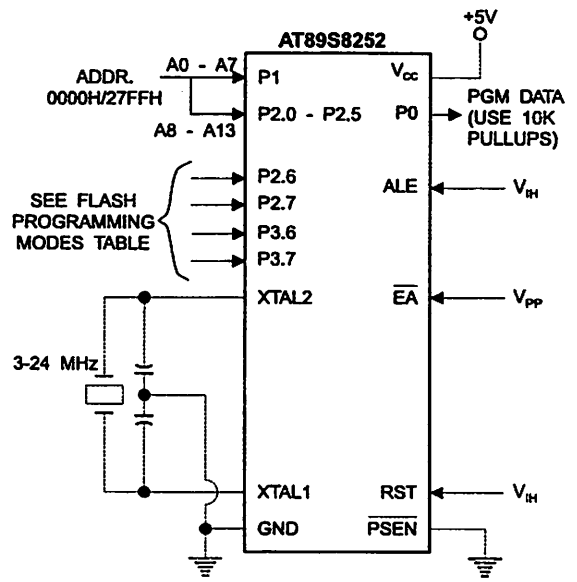


Figure 16. Verifying the Flash/EEPROM Memory

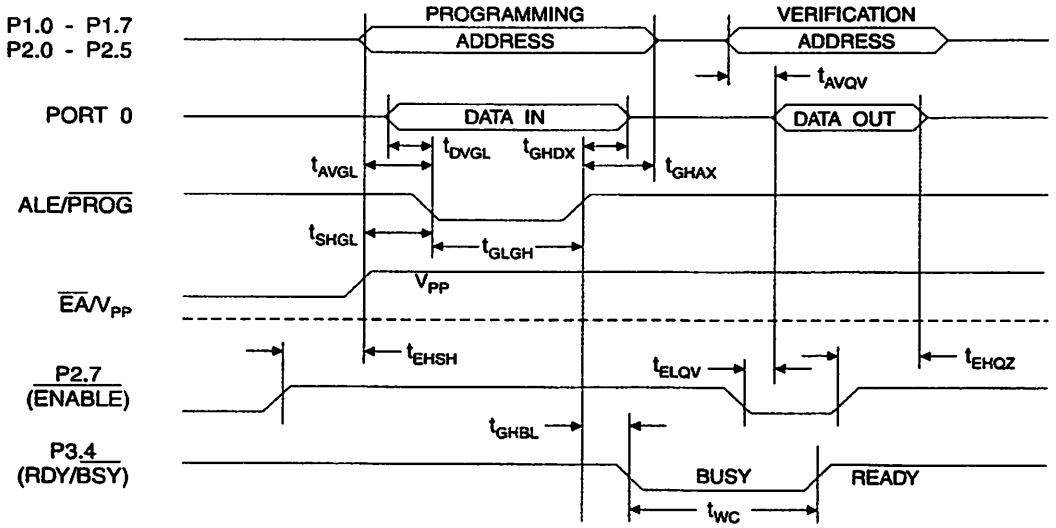


Flash Programming and Verification Characteristics-Parallel Mode

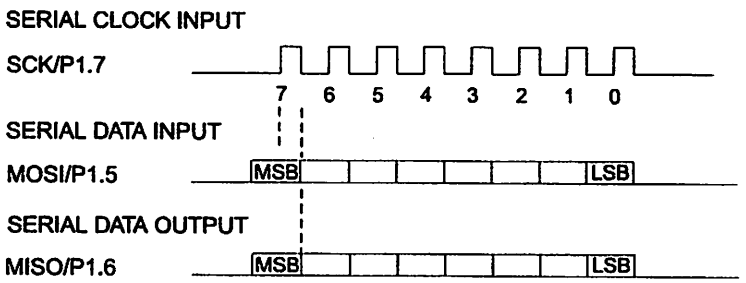
T_A = 0°C to 70°C, V_{CC} = 5.0V ± 10%

Symbol	Parameter	Min	Max	Units
V_{PP}	Programming Enable Voltage	11.5	12.5	V
I_{PP}	Programming Enable Current		1.0	mA
$1/t_{CLCL}$	Oscillator Frequency	3	24	MHz
t_{AVGL}	Address Setup to $\overline{PROG}$ Low	$48t_{CLCL}$		
t_{GHAX}	Address Hold After $\overline{PROG}$	$48t_{CLCL}$		
t_{DVGL}	Data Setup to $\overline{PROG}$ Low	$48t_{CLCL}$		
t_{GHDX}	Data Hold After $\overline{PROG}$	$48t_{CLCL}$		
t_{EHSH}	P2.7 ($\overline{ENABLE}$) High to V_{PP}	$48t_{CLCL}$		
t_{SHGL}	V_{PP} Setup to $\overline{PROG}$ Low	10		µs
t_{GLGH}	$\overline{PROG}$ Width	1	110	µs
t_{AVQV}	Address to Data Valid		$48t_{CLCL}$	
t_{ELQV}	$\overline{ENABLE}$ Low to Data Valid		$48t_{CLCL}$	
t_{EHQZ}	Data Float After $\overline{ENABLE}$	0	$48t_{CLCL}$	
t_{GHBL}	$\overline{PROG}$ High to $\overline{BUSY}$ Low		1.0	µs
t_{WC}	Byte Write Cycle Time		2.0	ms

Flash/EEPROM Programming and Verification Waveforms - Parallel Mode



Serial Downloading Waveforms



Absolute Maximum Ratings*

Operating Temperature	-55°C to +125°C
Storage Temperature	-65°C to +150°C
Voltage on Any Pin with Respect to Ground	-1.0V to +7.0V
Maximum Operating Voltage	6.6V
DC Output Current	15.0 mA

*NOTICE: Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC Characteristics

The values shown in this table are valid for T_A = -40°C to 85°C and V_{CC} = 5.0V ± 20%, unless otherwise noted.

Symbol	Parameter	Condition	Min	Max	Units
V_{IL}	Input Low Voltage	(Except $\overline{EA}$)	-0.5	0.2 V_{CC} - 0.1	V
V_{IL1}	Input Low Voltage ($\overline{EA}$)		-0.5	0.2 V_{CC} - 0.3	V
V_{IH}	Input High Voltage	(Except XTAL1, RST)	0.2 V_{CC} + 0.9	V_{CC} + 0.5	V
V_{IH1}	Input High Voltage	(XTAL1, RST)	0.7 V_{CC}	V_{CC} + 0.5	V
V_{OL}	Output Low Voltage (1) (Ports 1,2,3)	I_{OL} = 1.6 mA		0.5	V
V_{OL1}	Output Low Voltage (1) (Port 0, ALE, $\overline{PSEN}$)	I_{OL} = 3.2 mA		0.5	V
V_{OH}	Output High Voltage (Ports 1,2,3, ALE, $\overline{PSEN}$)	I_{OH} = -60 µA, V_{CC} = 5V ± 10%	2.4		V
		I_{OH} = -25 µA	0.75 V_{CC}		V
		I_{OH} = -10 µA	0.9 V_{CC}		V
V_{OH1}	Output High Voltage (Port 0 in External Bus Mode)	I_{OH} = -800 µA, V_{CC} = 5V ± 10%	2.4		V
		I_{OH} = -300 µA	0.75 V_{CC}		V
		I_{OH} = -80 µA	0.9 V_{CC}		V
I_{IL}	Logical 0 Input Current (Ports 1,2,3)	V_{IN} = 0.45V		-50	µA
I_{TL}	Logical 1 to 0 Transition Current (Ports 1,2,3)	V_{IN} = 2V, V_{CC} = 5V ± 10%		-650	µA
I_{LI}	Input Leakage Current (Port 0, $\overline{EA}$)	0.45 < V_{IN} < V_{CC}		±10	µA
RRST	Reset Pulldown Resistor		50	300	KΩ
C_{IO}	Pin Capacitance	Test Freq. = 1 MHz, T_A = 25°C		10	pF
I_{CC}	Power Supply Current	Active Mode, 12 MHz		25	mA
		Idle Mode, 12 MHz		6.5	mA
	Power Down Mode (2)	V_{CC} = 6V		100	µA
		V_{CC} = 3V		40	µA

Notes:
1. Under steady state (non-transient) conditions, I_{OL} must be externally limited as follows:
   Maximum I_{OL} per port pin: 10 mA
   Maximum I_{OL} per 8-bit port:
   Port 0: 26 mA
   Ports 1, 2, 3: 15 mA
   Maximum total I_{OL} for all output pins: 71 mA
   If I_{OL} exceeds the test condition, V_{OL} may exceed the related specification. Pins are not guaranteed to sink current greater than the listed test conditions.
2. Minimum V_{CC} for Power Down is 2V

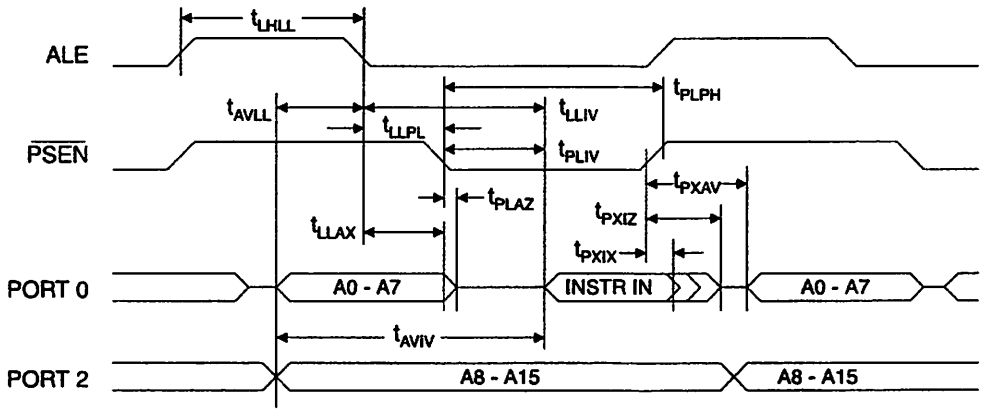
AC Characteristics

Under operating conditions, load capacitance for Port 0, ALE/$\overline{PROG}$, and $\overline{PSEN}$ = 100 pF; load capacitance for all other outputs = 80 pF.

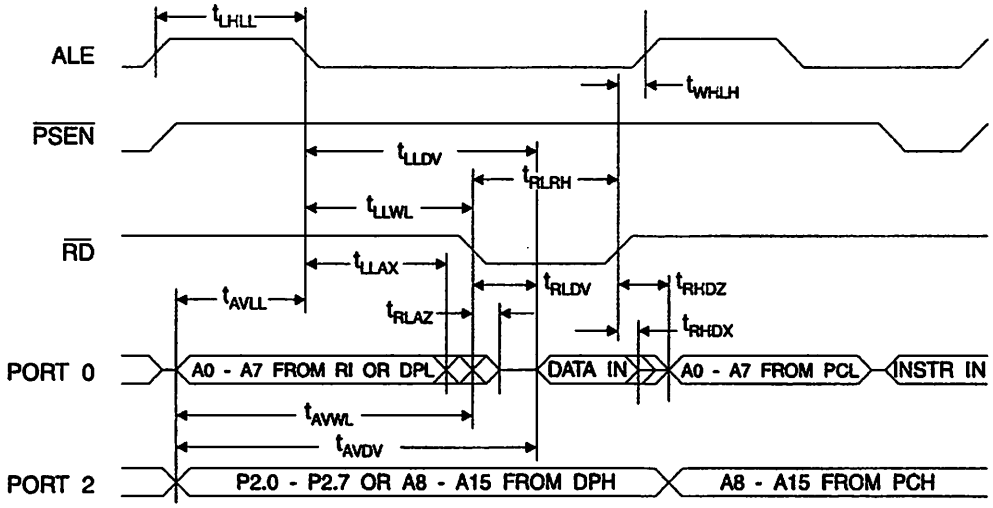
External Program and Data Memory Characteristics

Symbol	Parameter	Variable Oscillator		Units
		Min	Max	
$1/t_{CLCL}$	Oscillator Frequency	0	24	MHz
t_{LHLL}	ALE Pulse Width	$2t_{CLCL}$ - 40		ns
t_{AVLL}	Address Valid to ALE Low	t_{CLCL} - 13		ns
t_{LLAX}	Address Hold After ALE Low	t_{CLCL} - 20		ns
t_{LLIV}	ALE Low to Valid Instruction In		$4t_{CLCL}$ - 65	ns
t_{LLPL}	ALE Low to $\overline{PSEN}$ Low	t_{CLCL} - 13		ns
t_{PLPH}	$\overline{PSEN}$ Pulse Width	$3t_{CLCL}$ - 20		ns
t_{PLIV}	$\overline{PSEN}$ Low to Valid Instruction In		$3t_{CLCL}$ - 45	ns
t_{PXIX}	Input Instruction Hold After $\overline{PSEN}$	0		ns
t_{PXIZ}	Input Instruction Float After $\overline{PSEN}$		t_{CLCL} - 10	ns
t_{PXAV}	$\overline{PSEN}$ to Address Valid	t_{CLCL} - 8		ns
t_{AVIV}	Address to Valid Instruction In		$5t_{CLCL}$ - 55	ns
t_{PLAZ}	$\overline{PSEN}$ Low to Address Float		10	ns
t_{RLRH}	$\overline{RD}$ Pulse Width	$6t_{CLCL}$ - 100		ns
t_{WLWH}	$\overline{WR}$ Pulse Width	$6t_{CLCL}$ - 100		ns
t_{RLDV}	$\overline{RD}$ Low to Valid Data In		$5t_{CLCL}$ - 90	ns
t_{RHDX}	Data Hold After $\overline{RD}$	0		ns
t_{RHDZ}	Data Float After $\overline{RD}$		$2t_{CLCL}$ - 28	ns
t_{LLDV}	ALE Low to Valid Data In		$8t_{CLCL}$ - 150	ns
t_{AVDV}	Address to Valid Data In		$9t_{CLCL}$ - 165	ns
t_{LLWL}	ALE Low to $\overline{RD}$ or $\overline{WR}$ Low	$3t_{CLCL}$ - 50	$3t_{CLCL}$ + 50	ns
t_{AVWL}	Address to $\overline{RD}$ or $\overline{WR}$ Low	$4t_{CLCL}$ - 75		ns
t_{QVWX}	Data Valid to $\overline{WR}$ Transition	t_{CLCL} - 20		ns
t_{QVWH}	Data Valid to $\overline{WR}$ High	$7t_{CLCL}$ - 120		ns
t_{WHQX}	Data Hold After $\overline{WR}$	t_{CLCL} - 20		ns
t_{RLAZ}	$\overline{RD}$ Low to Address Float		0	ns
t_{WHLH}	$\overline{RD}$ or $\overline{WR}$ High to ALE High	t_{CLCL} - 20	t_{CLCL} + 25	ns

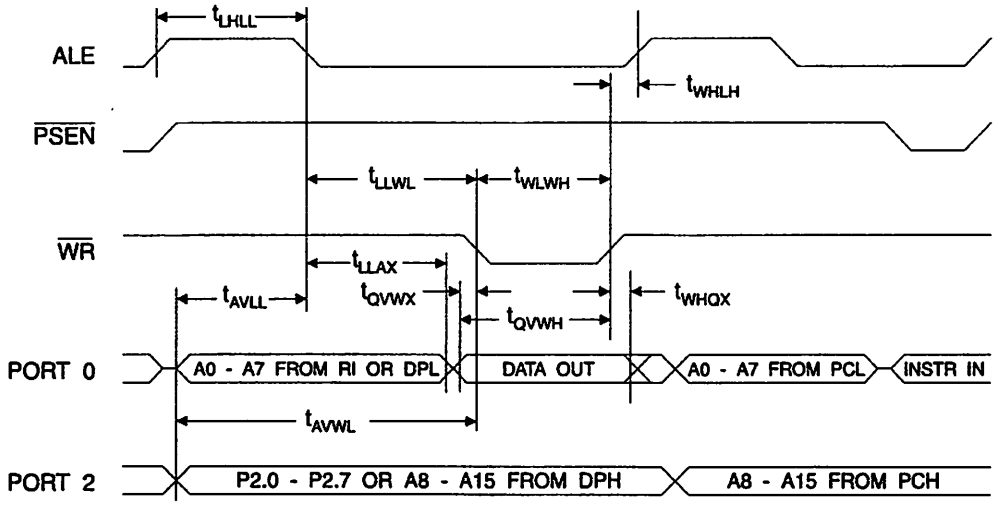
External Program Memory Read Cycle



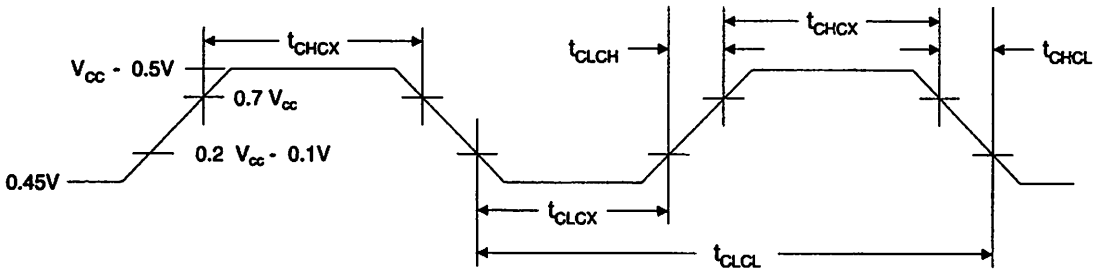
External Data Memory Read Cycle



External Data Memory Write Cycle



External Clock Drive Waveforms



External Clock Drive

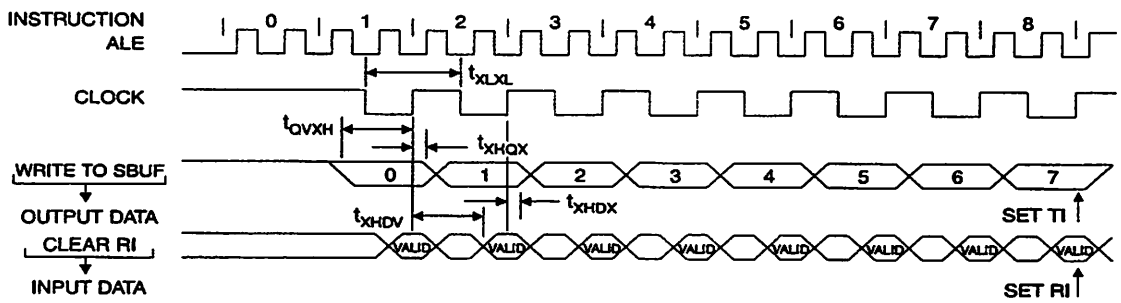
Symbol	Parameter	V_{CC} = 4.0V to 6.0V		Units
		Min	Max	
$1/t_{CLCL}$	Oscillator Frequency	0	24	MHz
t_{CLCL}	Clock Period	41.6		ns
t_{CHCX}	High Time	15		ns
t_{CLCX}	Low Time	15		ns
t_{CLCH}	Rise Time		20	ns
t_{CHCL}	Fall Time		20	ns

Serial Port Timing: Shift Register Mode Test Conditions

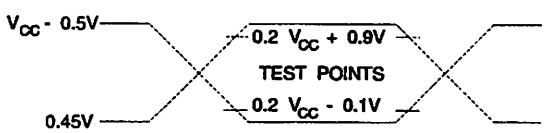
The values in this table are valid for V_{CC} = 4.0V to 6V and Load Capacitance = 80 pF.

Symbol	Parameter	Variable Oscillator		Units
		Min	Max	
t_{XLXL}	Serial Port Clock Cycle Time	$12t_{CLCL}$		µs
t_{QVXH}	Output Data Setup to Clock Rising Edge	$10t_{CLCL}$ - 133		ns
t_{XHQX}	Output Data Hold After Clock Rising Edge	$2t_{CLCL}$ - 117		ns
t_{XHDX}	Input Data Hold After Clock Rising Edge	0		ns
t_{XHDV}	Clock Rising Edge to Input Data Valid		$10t_{CLCL}$ - 133	ns

Shift Register Mode Timing Waveforms

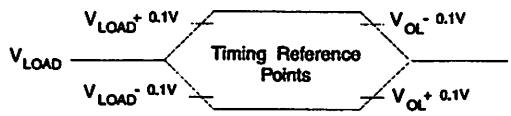


AC Testing Input/Output Waveforms[1]



Notes: 1. AC Inputs during testing are driven at V_{CC} - 0.5V for a logic 1 and 0.45V for a logic 0. Timing measurements are made at V_{IH} min. for a logic 1 and V_{IL} max. for a logic 0.

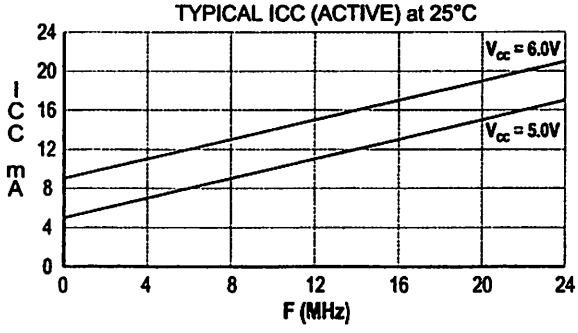
Float Waveforms[1]



Notes: 1. For timing purposes, a port pin is no longer floating when a 100 mV change from load voltage occurs. A port pin begins to float when a 100 mV change from the loaded V_{OH}/V_{OL} level occurs.

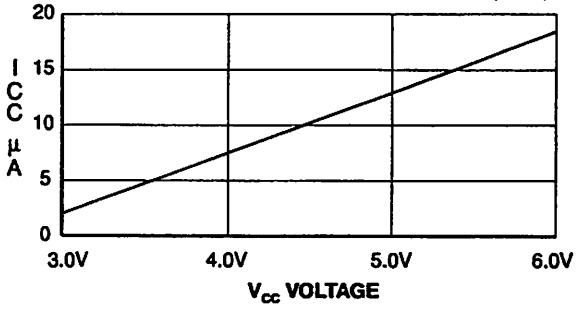
AT89S8252

TYPICAL ICC (ACTIVE) at 25°C



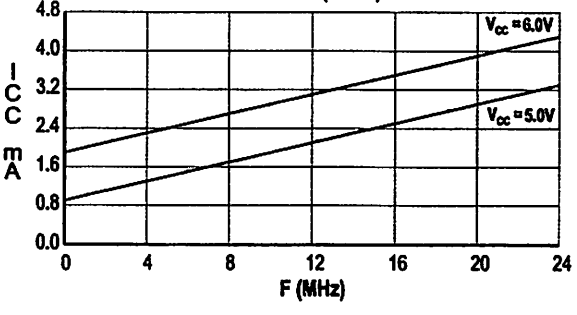
AT89S8252

TYPICAL ICC vs. VOLTAGE - POWER DOWN (85°C)



AT89S8252

TYPICAL ICC (IDLE) at 25°C



Notes: 1. XTAL1 tied to GND for Icc (power down)
2. Lock bits programmed

Ordering Information

Speed (MHz)	Power Supply	Ordering Code	Package	Operation Range
16	4.0V to 6.0V	AT89S8252-16AA AT89S8252-16JA AT89S8252-16PA AT89S8252-16QA	44A 44J 40P6 44Q	Automotive (-40°C to 105°C)
24	4.0V to 6.0V	AT89S8252-24AC AT89S8252-24JC AT89S8252-24PC AT89S8252-24QC	44A 44J 40P6 44Q	Commercial (0°C to 70°C)
	4.0V to 6.0V	AT89S8252-24AI AT89S8252-24JI AT89S8252-24PI AT89S8252-24QI	44A 44J 40P6 44Q	Industrial (-40°C to 85°C)
33	4.5V to 5.5V	AT89S8252-33AC AT89S8252-33JC AT89S8252-33PC AT89S8252-33QC	44A 44J 40P6 44Q	Commercial (0°C to 70°C)

= Preliminary Information

Package Type	
44A	44 Lead, Thin Plastic Gull Wing Quad Flatpack (TQFP)
44J	44 Lead, Plastic J-Leaded Chip Carrier (PLCC)
40P6	40 Lead, 0.600" Wide, Plastic Dual Inline Package (PDIP)
44Q	44 Lead, Plastic Gull Wing Quad Flatpack (PQFP)

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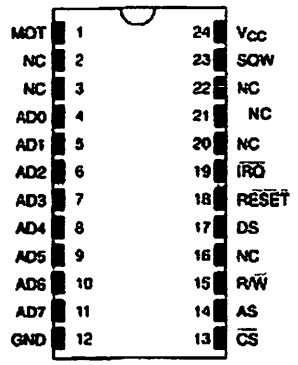
FEATURES

- Drop–in replacement for IBM AT computer clock/calendar
- Pin-compatible with the MC146818B and DS1287
- Totally nonvolatile with over 10 years of operation in the absence of power
- Self–contained subsystem includes lithium, quartz, and support circuitry
- Counts seconds, minutes, hours, days, day of the week, date, month, and year with leap year compensation valid up to 2100
- Binary or BCD representation of time, calendar, and alarm
- 12– or 24–hour clock with AM and PM in 12–hour mode
- Daylight Savings Time option
- Selectable between Motorola and Intel bus timing
- Multiplex bus for pin efficiency
- Interfaced with software as 128 RAM locations
  - 14 bytes of clock and control registers
  - 114 bytes of general purpose RAM
- Programmable square wave output signal
- Bus–compatible interrupt signals ($\overline{IRQ}$)
- Three interrupts are separately software–maskable and testable
  - Time–of–day alarm once/second to once/day
  - Periodic rates from 122 ms to 500 ms
  - End of clock update cycle

PIN ASSIGNMENT



24-PIN ENCAPSULATED PACKAGE

PIN DESCRIPTION

AD0–AD7	– Multiplexed Address/Data Bus
NC	– No Connection
MOT	– Bus Type Selection
$\overline{CS}$	– Chip Select
AS	– Address Strobe
R/$\overline{W}$	– Read/Write Input
DS	– Data Strobe
$\overline{RESET}$	– Reset Input
$\overline{IRQ}$	– Interrupt Request Output
SQW	– Square Wave Output
V_{CC}	– +5 Volt Supply
GND	– Ground

DESCRIPTION

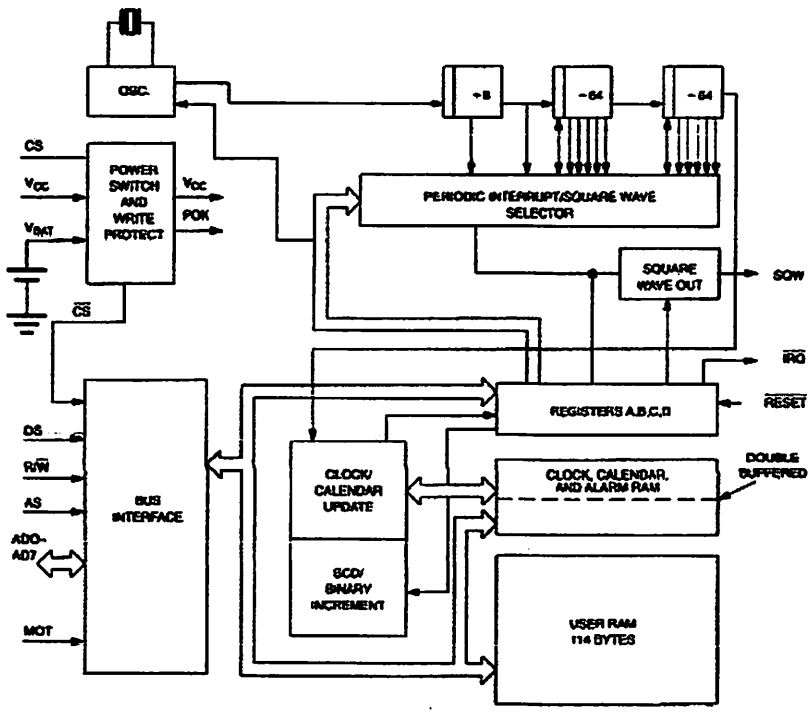
The DS12887 Real Time Clock plus RAM is designed to be a direct replacement for the DS1287. The DS12887 is identical in form, fit, and function to the DS1287, and has an additional 64 bytes of general purpose RAM. Access to this additional RAM space is determined by the logic level presented on AD6 during the address portion of an access cycle. A lithium energy source, quartz crystal, and write–protection circuitry are contained within a 24–pin dual in-line package. As such, the DS12887 is a complete subsystem replacing 16 components in a typical application. The functions include a nonvolatile time–of–day clock, an alarm, a one-hundred–year calendar, programmable interrupt, square wave

generator, and 114 bytes of nonvolatile static RAM. The real time clock is distinctive in that time–of–day and memory are maintained even in the absence of power.

OPERATION

The block diagram in Figure 1 shows the pin connections with the major internal functions of the DS12887. The following paragraphs describe the function of each pin.

BLOCK DIAGRAM DS12887 Figure 1



POWER–DOWN/POWER–UP CONSIDERATIONS

The Real Time Clock function will continue to operate and all of the RAM, time, calendar, and alarm memory locations remain nonvolatile regardless of the level of the V_{CC} input. When V_{CC} is applied to the DS12887 and reaches a level of greater than 4.25 volts, the device becomes accessible after 200 ms, provided that the oscillator is running and the oscillator countdown chain is not in reset (see Register A). This time period allows the system to stabilize after power is applied. When V_{CC} falls below 4.25 volts, the chip select input is internally forced to an inactive level regardless of the value of $\overline{CS}$ at the input pin. The DS12887 is, therefore, write–protected. When the DS12887 is in a write–protected state, all inputs are ignored and all outputs are in a high impedance state. When V_{CC} falls below a level of approximately 3 volts, the external V_{CC} supply is switched off and an internal lithium energy source supplies power to the Real Time Clock and the RAM memory.

SIGNAL DESCRIPTIONS

GND, V_{CC} – DC power is provided to the device on these pins. V_{CC} is the +5 volt input. When 5 volts are applied within normal limits, the device is fully accessible and data can be written and read. When V_{CC} is below 4.25 volts typical, reads and writes are inhibited. However, the timekeeping function continues

unaffected by the lower input voltage. As V_{CC} falls below 3 volts typical, the RAM and timekeeper are switched over to an internal lithium energy source. The timekeeping function maintains an accuracy of ±1 minute per month at 25°C regardless of the voltage input on the V_{CC} pin.

MOT (Mode Select) – The MOT pin offers the flexibility to choose between two bus types. When connected to V_{CC}, Motorola bus timing is selected. When connected to GND or left disconnected, Intel bus timing is selected. The pin has an internal pulldown resistance of approximately 20 kΩ.

SQW (Square Wave Output) – The SQW pin can output a signal from one of 13 taps provided by the 15 internal divider stages of the Real Time Clock. The frequency of the SQW pin can be changed by programming Register A as shown in Table 1. The SQW signal can be turned on and off using the SQWE bit in Register B. The SQW signal is not available when V_{CC} is less than 4.25 volts, typically.

PERIODIC INTERRUPT RATE AND SQUARE WAVE OUTPUT FREQUENCY Table 1

SELECT BITS REGISTER A				t_{PI} PERIODIC INTERRUPT RATE	SQW OUTPUT FREQUENCY
RS3	RS2	RS1	RS0		
0	0	0	0	None	None
0	0	0	1	3.90625 ms	256 Hz
0	0	1	0	7.8125 ms	128 Hz
0	0	1	1	122.070 µs	8.192 kHz
0	1	0	0	244.141 µs	4.096 kHz
0	1	0	1	488.281 µs	2.048 kHz
0	1	1	0	976.5625 µs	1.024 kHz
0	1	1	1	1.953125 ms	512 Hz
1	0	0	0	3.90625 ms	256 Hz
1	0	0	1	7.8125 ms	128 Hz
1	0	1	0	15.625 ms	64 Hz
1	0	1	1	31.25 ms	32 Hz
1	1	0	0	62.5 ms	16 Hz
1	1	0	1	125 ms	8 Hz
1	1	1	0	250 ms	4 Hz
1	1	1	1	500 ms	2 Hz

AD0–AD7 (Multiplexed Bidirectional Address/Data Bus) – Multiplexed buses save pins because address information and data information time-share the same signal paths. The addresses are present during the first portion of the bus cycle and the same pins and signal paths are used for data in the second portion of the cycle. Address/data multiplexing does not slow the access time of the DS12887 since the bus change from address to data occurs during the internal RAM access time. Addresses must be valid prior to the falling edge of AS/ ALE, at which time the DS12887 latches the address from AD0 to AD6. Valid write data must be present and held stable during the latter portion of the DS or $\overline{WR}$ pulses. In a read cycle the DS12887 outputs 8 bits of data during the latter portion of the DS or $\overline{RD}$ pulses. The read cycle is terminated and the bus returns to a high impedance state as DS transitions low in the case of Motorola timing or as $\overline{RD}$ transitions high in the case of Intel timing.

AS (Address Strobe Input) – A positive-going address strobe pulse serves to demultiplex the bus. The falling edge of AS/ALE causes the address to be latched within the DS12887. The next rising edge that

occurs on the AS bus will clear the address regardless of whether $\overline{CS}$ is asserted. Access commands should be sent in pairs.

DS (Data Strobe or Read Input) – The DS/$\overline{RD}$ pin has two modes of operation depending on the level of the MOT pin. When the MOT pin is connected to V_{CC}, Motorola bus timing is selected. In this mode DS is a positive pulse during the latter portion of the bus cycle and is called Data Strobe. During read cycles, DS signifies the time that the DS12887 is to drive the bidirectional bus. In write cycles the trailing edge of DS causes the DS12887 to latch the written data. When the MOT pin is connected to GND, Intel bus timing is selected. In this mode the DS pin is called Read ($\overline{RD}$). $\overline{RD}$ identifies the time period when the DS12887 drives the bus with read data. The $\overline{RD}$ signal is the same definition as the Output Enable ($\overline{OE}$) signal on a typical memory.

R/$\overline{W}$ (Read/Write Input) – The R/$\overline{W}$ pin also has two modes of operation. When the MOT pin is connected to V_{CC} for Motorola timing, R/$\overline{W}$ is at a level which indicates whether the current cycle is a read or write. A read cycle is indicated with a high level on R/$\overline{W}$ while DS is high. A write cycle is indicated when R/$\overline{W}$ is low during DS.

When the MOT pin is connected to GND for Intel timing, the R/$\overline{W}$ signal is an active low signal called WR. In this mode the R/$\overline{W}$ pin has the same meaning as the Write Enable signal ($\overline{WE}$) on generic RAMs.

$\overline{CS}$ (Chip Select Input) – The Chip Select signal must be asserted low for a bus cycle in the DS12887 to be accessed. $\overline{CS}$ must be kept in the active state during DS and AS for Motorola timing and during $\overline{RD}$ and $\overline{WR}$ for Intel timing. Bus cycles which take place without asserting $\overline{CS}$ will latch addresses but no access will occur. When V_{CC} is below 4.25 volts, the DS12887 internally inhibits access cycles by internally disabling the $\overline{CS}$ input. This action protects both the real time clock data and RAM data during power outages.

$\overline{IRQ}$ (Interrupt Request Output) – The $\overline{IRQ}$ pin is an active low output of the DS12887 that can be used as an interrupt input to a processor. The $\overline{IRQ}$ output remains low as long as the status bit causing the interrupt is present and the corresponding interrupt-enable bit is set. To clear the $\overline{IRQ}$ pin the processor program normally reads the C register. The $\overline{RESET}$ pin also clears pending interrupts.

When no interrupt conditions are present, the $\overline{IRQ}$ level is in the high impedance state. Multiple interrupting devices can be connected to an $\overline{IRQ}$ bus. The $\overline{IRQ}$ bus is an open drain output and requires an external pullup resistor.

$\overline{RESET}$ (Reset Input) – The $\overline{RESET}$ pin has no effect on the clock, calendar, or RAM. On power-up the $\overline{RESET}$ pin can be held low for a time in order to allow the power supply to stabilize. The amount of time that $\overline{RESET}$ is held low is dependent on the application. However, if $\overline{RESET}$ is used on power-up, the time $\overline{RESET}$ is low should exceed 200 ms to make sure that the internal timer that controls the DS12887 on power-up has timed out. When $\overline{RESET}$ is low and V_{CC} is above 4.25 volts, the following occurs:

A. Periodic Interrupt Enable (PEI) bit is cleared to 0.
B. Alarm Interrupt Enable (AIE) bit is cleared to 0.
C. Update Ended Interrupt Flag (UF) bit is cleared to 0.
D. Interrupt Request Status Flag (IRQF) bit is cleared to 0.
E. Periodic Interrupt Flag (PF) bit is cleared to 0.
F. The device is not accessible until $\overline{\text{RESET}}$ is returned high.
G. Alarm Interrupt Flag (AF) bit is cleared to 0.
H. $\overline{\text{IRQ}}$ pin is in the high impedance state.
I. Square Wave Output Enable ($\overline{\text{SQWE}}$) bit is cleared to 0.
J. Update Ended Interrupt Enable (UIE) is cleared to 0.

In a typical application $\overline{\text{RESET}}$ can be connected to V_{CC}. This connection will allow the DS12887 to go in and out of power fail without affecting any of the control registers.

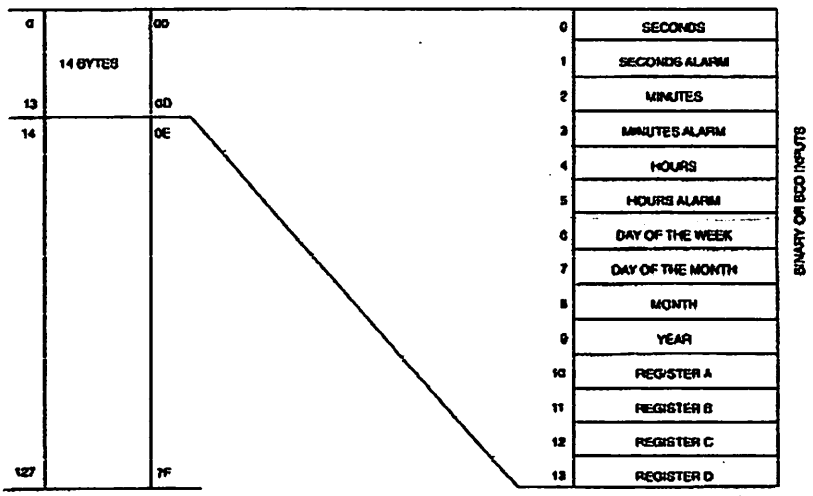
ADDRESS MAP

The address map of the DS12887 is shown in Figure 2. The address map consists of 114 bytes of user RAM, 10 bytes of RAM that contain the RTC time, calendar, and alarm data, and 4 bytes which are used for control and status. All 128 bytes can be directly written or read except for the following:

1. Registers C and D are read–only.
2. Bit 7 of Register A is read–only.
3. The high order bit of the seconds byte is read–only.

The contents of four registers (A,B,C, and D) are described in the "Registers" section.

ADDRESS MAP DS12887 Figure 2



TIME, CALENDAR AND ALARM LOCATIONS

The time and calendar information is obtained by reading the appropriate memory bytes. The time, calendar, and alarm are set or initialized by writing the appropriate RAM bytes. The contents of the 10 time, calendar, and alarm bytes can be either Binary or Binary–Coded Decimal (BCD) format. Before writing the internal time, calendar, and alarm registers, the SET bit in Register B should be written to a logic 1 to prevent updates from occurring while access is being attempted. In addition to writing the 10 time, calendar, and alarm registers in a selected format (binary or BCD), the data mode bit (DM) of Register B must be set to the appropriate logic level. All 10 time, calendar, and alarm bytes must use the same data mode. The set bit in Register B should be cleared after the data mode bit has been written to allow the real time clock to update the time and calendar bytes. Once initialized, the real time clock makes all updates in the selected mode. The data mode cannot be changed without reinitializing the 10 data bytes. Table 2 shows the binary and BCD formats of the 10 time, calendar, and alarm locations. The 24–12 bit cannot be changed without reinitializing the hour locations. When the 12–hour format is selected, the high order bit of the hours byte represents PM when it is a logic 1. The time, calendar, and alarm bytes are always accessible because they are double buffered. Once per second the 10 bytes are advanced by 1 second and checked for an alarm condition. If a read of the time and calendar data occurs during an update, a problem exists where seconds, minutes, hours, etc. may not correlate. The probability of reading incorrect time and calendar data is low. Several methods of avoiding any possible incorrect time and calendar reads are covered later in this text.

The three alarm bytes can be used in two ways. First, when the alarm time is written in the appropriate hours, minutes, and seconds alarm locations, the alarm interrupt is initiated at the specified time each day if the alarm enable bit is high. The second use condition is to insert a "don't care" state in one or more of the three alarm bytes. The "don't care" code is any hexadecimal value from C0 to FF. The two most significant bits of each byte set the "don't care" condition when at logic 1. An alarm will be generated each hour when the "don't care" bits are set in the hours byte. Similarly, an alarm is generated every minute with "don't care" codes in the hours and minute alarm bytes. The "don't care" codes in all three alarm bytes create an interrupt every second.

TIME, CALENDAR AND ALARM DATA MODES Table 2

ADDRESS LOCATION	FUNCTION	DECIMAL RANGE	RANGE	
			BINARY DATA MODE	BCD DATA MODE
0	Seconds	0-59	00-3B	00-59
1	Seconds Alarm	0-59	00-3B	00-59
2	Minutes	0-59	00-3B	00-59
3	Minutes Alarm	0-59	00-3B	00-59
4	Hours-12-hr Mode	1-12	01-0C AM, 81-8C PM	01-12AM, 81-92PM
	Hours-24-hr Mode	0-23	00-17	00-23
5	Hours Alarm-12-hr	1-12	01-0C AM, 81-8C PM	01-12AM, 81-92PM
	Hours Alarm-24-hr	0-23	00-17	00-23
6	Day of the Week Sunday = 1	1-7	01-07	01-07
7	Date of the Month	1-31	01-1F	01-31
8	Month	1-12	01-0C	01-12
9	Year	0-99	00-63	00-99

NONVOLATILE RAM

The 114 general purpose nonvolatile RAM bytes are not dedicated to any special function within the DS12887. They can be used by the processor program as nonvolatile memory and are fully available during the update cycle.

INTERRUPTS

The RTC plus RAM includes three separate, fully automatic sources of interrupt for a processor. The alarm interrupt can be programmed to occur at rates from once per second to once per day. The periodic interrupt can be selected for rates from 500 ms to 122 µs. The update-ended interrupt can be used to indicate to the program that an update cycle is complete. Each of these independent interrupt conditions is described in greater detail in other sections of this text.

The processor program can select which interrupts, if any, are going to be used. Three bits in Register B enable the interrupts. Writing a logic 1 to an interrupt-enable bit permits that interrupt to be initiated when the event occurs. A 0 in an interrupt-enable bit prohibits the $\overline{IRQ}$ pin from being asserted from that interrupt condition. If an interrupt flag is already set when an interrupt is enabled, $\overline{IRQ}$ is immediately set at an active level, although the interrupt initiating the event may have occurred much earlier. As a result, there are cases where the program should clear such earlier initiated interrupts before first enabling new interrupts.

When an interrupt event occurs, the relating flag bit is set to logic 1 in Register C. These flag bits are set independently of the state of the corresponding enable bit in Register B. The flag bit can be used in a polling mode without enabling the corresponding enable bits. The interrupt flag bit is a status bit which software can interrogate as necessary. When a flag is set, an indication is given to software that an interrupt event has occurred since the flag bit was last read; however, care should be taken when using the flag bits as they are cleared each time Register C is read. Double latching is included with Register C so that bits which are set remain stable throughout the read cycle. All bits which are set (high) are cleared when read and new interrupts which are pending during the read cycle are held until after the cycle is completed. One, 2, or 3 bits can be set when reading Register C. Each utilized flag bit should be examined when read to ensure that no interrupts are lost.

The second flag bit usage method is with fully enabled interrupts. When an interrupt flag bit is set and the corresponding interrupt enable bit is also set, the $\overline{IRQ}$ pin is asserted low. $\overline{IRQ}$ is asserted as long as at least one of the three interrupt sources has its flag and enable bits both set. The IRQF bit in Register C is a 1 whenever the $\overline{IRQ}$ pin is being driven low. Determination that the RTC initiated an interrupt is accomplished by reading Register C. A logic 1 in bit 7 (IRQF bit) indicates that one or more interrupts have been initiated by the DS12887. The act of reading Register C clears all active flag bits and the IRQF bit.

OSCILLATOR CONTROL BITS

When the DS12887 is shipped from the factory, the internal oscillator is turned off. This feature prevents the lithium energy cell from being used until it is installed in a system. A pattern of 010 in bits 4 through 6 of Register A will turn the oscillator on and enable the countdown chain. A pattern of 11X will turn the oscillator on, but holds the countdown chain of the oscillator in reset. All other combinations of bits 4 through 6 keep the oscillator off.

SQUARE WAVE OUTPUT SELECTION

Thirteen of the 15 divider taps are made available to a 1-of-15 selector, as shown in the block diagram of Figure 1. The first purpose of selecting a divider tap is to generate a square wave output signal on the SQW pin. The RS0–RS3 bits in Register A establish the square wave output frequency. These frequencies are listed in Table 1. The SQW frequency selection shares its 1–of–15 selector with the periodic interrupt generator. Once the frequency is selected, the output of the SQW pin can be turned on and off under program control with the square wave enable bit (SQWE).

PERIODIC INTERRUPT SELECTION

The periodic interrupt will cause the $\overline{IRQ}$ pin to go to an active state from once every 500 ms to once every 122 µs. This function is separate from the alarm interrupt which can be output from once per second to once per day. The periodic interrupt rate is selected using the same Register A bits which select the square wave frequency (see Table 1). Changing the Register A bits affects both the square wave frequency and the periodic interrupt output. However, each function has a separate enable bit in Register B. The SQWE bit controls the square wave output. Similarly, the periodic interrupt is enabled by the PIE bit in Register B. The periodic interrupt can be used with software counters to measure inputs, create output intervals, or await the next needed software function.

UPDATE CYCLE

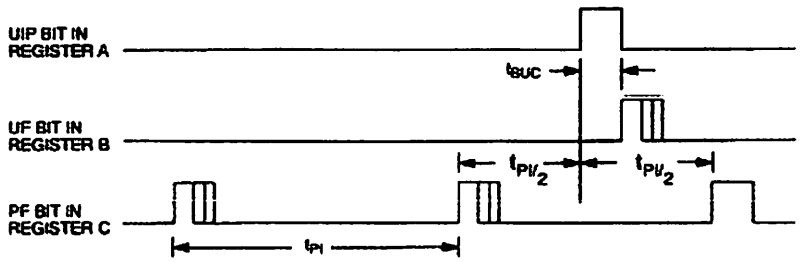
The DS12887 executes an update cycle once per second regardless of the SET bit in Register B. When the SET bit in Register B is set to 1, the user copy of the double buffered time, calendar, and alarm bytes is frozen and will not update as the time increments. However, the time countdown chain continues to update the internal copy of the buffer. This feature allows time to maintain accuracy independent of reading or writing the time, calendar, and alarm buffers and also guarantees that time and calendar information is consistent. The update cycle also compares each alarm byte with the corresponding time byte and issues an alarm if a match or if a "don't care" code is present in all three positions.

There are three methods that can handle access of the real time clock that avoid any possibility of accessing inconsistent time and calendar data. The first method uses the update–ended interrupt. If enabled, an interrupt occurs after every up date cycle that indicates that over 999 ms are available to read valid time and date information. If this interrupt is used, the IRQF bit in Register C should be cleared before leaving the interrupt routine.

A second method uses the update–in–progress bit (UIP) in Register A to determine if the update cycle is in progress. The UIP bit will pulse once per second. After the UIP bit goes high, the update transfer occurs 244 µs later. If a low is read on the UIP bit, the user has at least 244 µs before the time/calendar data will be changed. Therefore, the user should avoid interrupt service routines that would cause the time needed to read valid time/calendar data to exceed 244 µs.

The third method uses a periodic interrupt to determine if an update cycle is in progress. The UIP bit in Register A is set high between the setting of the PF bit in Register C (see Figure 3). Periodic interrupts that occur at a rate of greater than t_{BUC} allow valid time and date information to be reached at each occurrence of the periodic interrupt. The reads should be complete within one ($t_{PI/2} + t_{BUC}$) to ensure that data is not read during the update cycle.

UPDATE–ENDED AND PERIODIC INTERRUPT RELATIONSHIP Figure 3



t_{PI} = Periodic interrupt time interval per Table 1.
t_{BUC} = Delay time before update cycle = 244 µs.

REGISTERS

The DS12887 has four control registers which are accessible at all times, even during the update cycle.

REGISTER A

MSB							LSB
BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
UIP	DV2	DV1	DV0	RS3	RS2	RS1	RS0

UIP

The Update In Progress (UIP) bit is a status flag that can be monitored. When the UIP bit is a 1, the update transfer will soon occur. When UIP is a 0, the update transfer will not occur for at least 244 µs. The time, calendar, and alarm information in RAM is fully available for access when the UIP bit is 0. The UIP bit is read only and is not affected by $\overline{\text{RESET}}$. Writing the SET bit in Register B to a 1 inhibits any update transfer and clears the UIP status bit.

DV0, DV1, DV2

These 3 bits are used to turn the oscillator on or off and to reset the countdown chain. A pattern of 010 is the only combination of bits that will turn the oscillator on and allow the RTC to keep time. A pattern of 11X will enable the oscillator but holds the countdown chain in reset. The next update will occur at 500 ms after a pattern of 010 is written to DV0, DV1, and DV2.

RS3, RS2, RS1, RS0

These four rate–selection bits select one of the 13 taps on the 15–stage divider or disable the divider output. The tap selected can be used to generate an output square wave (SQW pin) and/or a periodic interrupt. The user can do one of the following:

1. Enable the interrupt with the PIE bit;
2. Enable the SQW output pin with the SQWE bit;
3. Enable both at the same time and the same rate; or
4. Enable neither.

Table 1 lists the periodic interrupt rates and the square wave frequencies that can be chosen with the RS bits. These four read/write bits are not affected by $\overline{\text{RESET}}$.

REGISTER B

MSB LSB

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
SET	PIE	AIE	UIE	SQWE	DM	24/12	DSE

SET

When the SET bit is a 0, the update transfer functions normally by advancing the counts once per second. When the SET bit is written to a 1, any update transfer is inhibited and the program can initialize the time and calendar bytes without an update occurring in the midst of initializing. Read cycles can be executed in a similar manner. SET is a read/write bit that is not modified by $\overline{\text{RESET}}$ or internal functions of the DS12887.

PIE

The periodic interrupt enable PIE bit is a read/write bit which allows the Periodic Interrupt Flag (PF) bit in Register C to drive the $\overline{\text{IRQ}}$ pin low. When the PIE bit is set to 1, periodic interrupts are generated by driving the $\overline{\text{IRQ}}$ pin low at a rate specified by the RS3–RS0 bits of Register A. A 0 in the PIE bit blocks the $\overline{\text{IRQ}}$ output from being driven by a periodic interrupt, but the Periodic Flag (PF) bit is still set at the periodic rate. PIE is not modified by any internal DS12887 functions, but is cleared to 0 on $\overline{\text{RESET}}$.

AIE

The Alarm Interrupt Enable (AIE) bit is a read/write bit which, when set to a 1, permits the Alarm Flag (AF) bit in Register C to assert $\overline{\text{IRQ}}$. An alarm interrupt occurs for each second that the three time bytes equal the three alarm bytes including a "don't care" alarm code of binary 11XXXXXX. When the AIE bit is set to 0, the AF bit does not initiate the $\overline{\text{IRQ}}$ signal. The $\overline{\text{RESET}}$ pin clears AIE to 0. The internal functions of the DS12887 do not affect the AIE bit.

UIE

The Update Ended Interrupt Enable (UIE) bit is a read/ write that enables the Update End Flag (UF) bit in Register C to assert $\overline{\text{IRQ}}$. The $\overline{\text{RESET}}$ pin going low or the SET bit going high clears to UIE bit.

SQWE

When the Square Wave Enable (SQWE) bit is set to a 1, a square wave signal at the frequency set by the rate-selection bits RS3 through RS0 is driven out on a SQW pin. When the SQWE bit is set to z0, the SQW pin is held low; the state of SQWE is cleared by the $\overline{\text{RESET}}$ pin. SQWE is a read/write bit.

DM

The Data Mode (DM) bit indicates whether time and calendar information is in binary or BCD format. The DM bit is set by the program to the appropriate format and can be read as required. This bit is not modified by internal functions or $\overline{\text{RESET}}$. A 1 in DM signifies binary data while a 0 in DM specifies Binary Coded Decimal (BCD) data.

24/12

The 24/12 control bit establishes the format of the hours byte. A 1 indicates the 24–hour mode and a 0 indicates the 12–hour mode. This bit is read/write and is not affected by internal functions of $\overline{\text{RESET}}$.

DSE

The Daylight Savings Enable (DSE) bit is a read/write bit which enables two special updates when DSE is set to 1. On the first Sunday in April the time increments from 1:59:59 AM to 3:00:00 AM. On the last Sunday in October when the time first reaches 1:59:59 AM it changes to 1:00:00 AM. These special updates do not occur when the DSE bit is a 0. This bit is not affected by internal functions or $\overline{\text{RESET}}$.

REGISTER C

MSB LSB

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
IRQF	PF	AF	UF	0	0	0	0

IRQF

The Interrupt Request Flag (IRQF) bit is set to a 1 when one or more of the following are true:

PF = PIE = 1
AF = AIE = 1
UF = UIE = 1

That is, IRQF = PF • PIE + AF • AIE + UF • UIE.

Any time the IRQF bit is a 1, the $\overline{\text{IRQ}}$ pin is driven low. All flag bits are cleared after Register C is read by the program or when the $\overline{\text{RESET}}$ pin is low.

PF

The Periodic Interrupt Flag (PF) is a read–only bit which is set to a 1 when an edge is detected on the selected tap of the divider chain. The RS3 through RS0 bits establish the periodic rate. PF is set to a 1 independent of the state of the PIE bit. When both PF and PIE are 1s, the $\overline{\text{IRQ}}$ signal is active and will set the IRQF bit. The PF bit is cleared by a $\overline{\text{RESET}}$ or a software read of Register C.

AF

A 1 in the Alarm Interrupt Flag (AF) bit indicates that the current time has matched the alarm time. If the AIE bit is also a 1, the $\overline{\text{IRQ}}$ pin will go low and a 1 will appear in the IRQF bit. A $\overline{\text{RESET}}$ or a read of Register C will clear AF.

UF

The Update Ended Interrupt Flag (UF) bit is set after each update cycle. When the UIE bit is set to 1, the one in UF causes the IRQF bit to be a 1, which will assert the $\overline{\text{IRQ}}$ pin. UF is cleared by reading Register C or a $\overline{\text{RESET}}$.

BIT 0 THROUGH BIT 3

These are unused bits of the status Register C. These bits always read 0 and cannot be written.

REGISTER D

MSB LSB

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
VRT	0	0	0	0	0	0	0

/RT

The Valid RAM and Time (VRT) bit is set to the 1 state by Dallas Semiconductor prior to shipment. This bit is not writable and should always be a 1 when read. If a 0 is ever present, an exhausted internal lithium energy source is indicated and both the contents of the RTC data and RAM data are questionable. This bit is unaffected by $\overline{\text{RESET}}$.

BIT 6 THROUGH BIT 0

The remaining bits of Register D are not usable. They cannot be written and, when read, they will always read 0.

ABSOLUTE MAXIMUM RATINGS*

Voltage on Any Pin Relative to Ground	–0.3V to +7.0V
Operating Temperature	0°C to 70°C
Storage Temperature	–40°C to +70°C
Soldering Temperature	260°C for 10 seconds (See Note 7)

* This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operation sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect reliability.

RECOMMENDED DC OPERATING CONDITIONS (0°C to 70°C)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Power Supply Voltage	V_{CC}	4.5	5.0	5.5	V	1
Input Logic 1	V_{IH}	2.2		V_{CC}+0.3	V	1
Input Logic 0	V_{IL}	–0.3		0.8	V	1

DC ELECTRICAL CHARACTERISTICS (0°C to 70°C; V_{CC} = 4.5 to 5.5V)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Power Supply Current	I_{CCI}		7	15	mA	2
Input Leakage	I_{IL}	–1.0		+1.0	µA	3
I/O Leakage	I_{LO}	–1.0		+1.0	µA	4
Input Current	I_{MOT}	–1.0		+500	µA	3
Output @ 2.4V	I_{OH}	–1.0			mA	1, 5
Output @ 0.4V	I_{OL}			4.0	mA	1
Write Protect Voltage	V_{TP}	4.0	4.25	4.5	V	

CAPACITANCE (t_A = 25°C)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Input Capacitance	C_{IN}			5	pF	
Output Capacitance	C_{OUT}			7	pF	

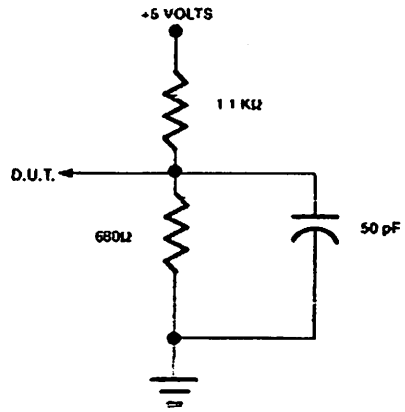
AC ELECTRICAL CHARACTERISTICS (0°C to 70°C; V_{CC} = 4.5V to 5.5V)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Cycle Time	t_{CYC}	385		DC	ns	
Pulse Width, DS/E Low or RD/$\overline{WR}$ High	PW_{EL}	150			ns	
Pulse Width, DS/E High or RD/$\overline{WR}$ Low	PW_{EH}	125			ns	
Input Rise and Fall Time	t_R, t_F			30	ns	
R/$\overline{W}$ Hold Time	t_{RWH}	10			ns	
R/$\overline{W}$ Setup Time Before DS/E	t_{RWS}	50			ns	
Chip Select Setup Time Before DS, $\overline{WR}$, or $\overline{RD}$	t_{CS}	20			ns	
Chip Select Hold Time	t_{CH}	0			ns	
Read Data Hold Time	t_{DHR}	10		80	ns	
Write Data Hold Time	t_{DHW}	0			ns	
Muxed Address Valid Time to AS/ALE Fall	t_{ASL}	30			ns	
Muxed Address Hold Time	t_{AHL}	10			ns	
Delay Time DS/E to AS/ALE Rise	t_{ASD}	20			ns	
Pulse Width AS/ALE High	PW_{ASH}	60			ns	
Delay Time, AS/ALE to DS/E Rise	t_{ASED}	40			ns	
Output Data Delay Time From DS/E or $\overline{RD}$	t_{DDR}	20		120	ns	6
Data Setup Time	t_{DSW}	100			ns	
Reset Pulse Width	t_{RWL}	5			µs	
$\overline{IRQ}$ Release from DS	t_{IRDS}			2	µs	
$\overline{IRQ}$ Release from $\overline{RESET}$	t_{IRR}			2	µs	

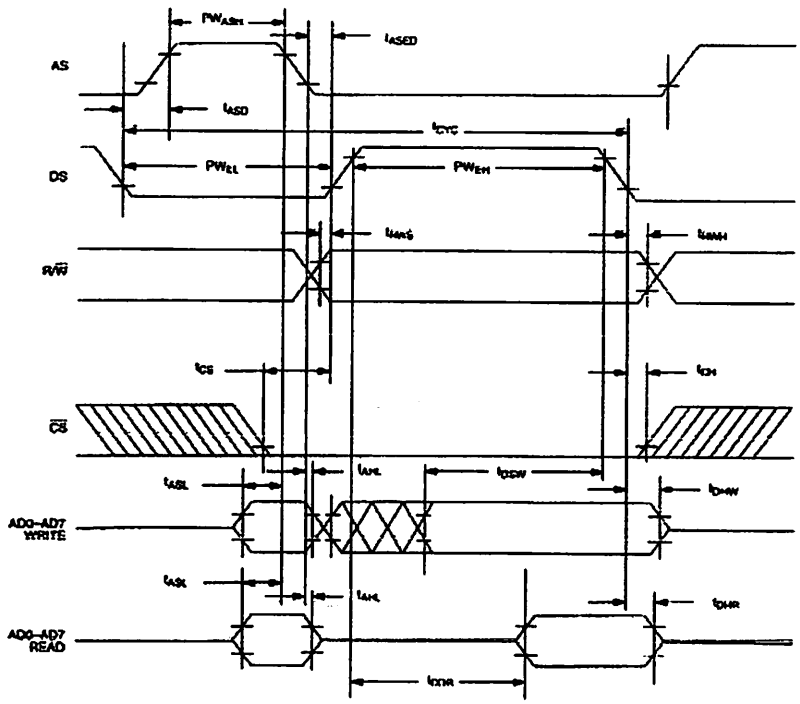
NOTES:

1. All voltages are referenced to ground.
2. All outputs are open.
3. The MOT pin has an internal pulldown of 20 KΩ.
4. Applies to the AD0–AD7 pins, the $\overline{IRQ}$ pin, and the SQW pin when each is in the high impedance state.
5. The $\overline{IRQ}$ pin is open drain.
6. Measured with a load as shown in Figure 4.
7. Real time clock modules can be successfully processed through conventional wave–soldering techniques as long as temperature exposure to the lithium energy source contained within does not exceed +85°C. However, post-solder cleaning with water washing techniques is acceptable, provided that ultrasonic vibration is not used to prevent damage to the crystal.

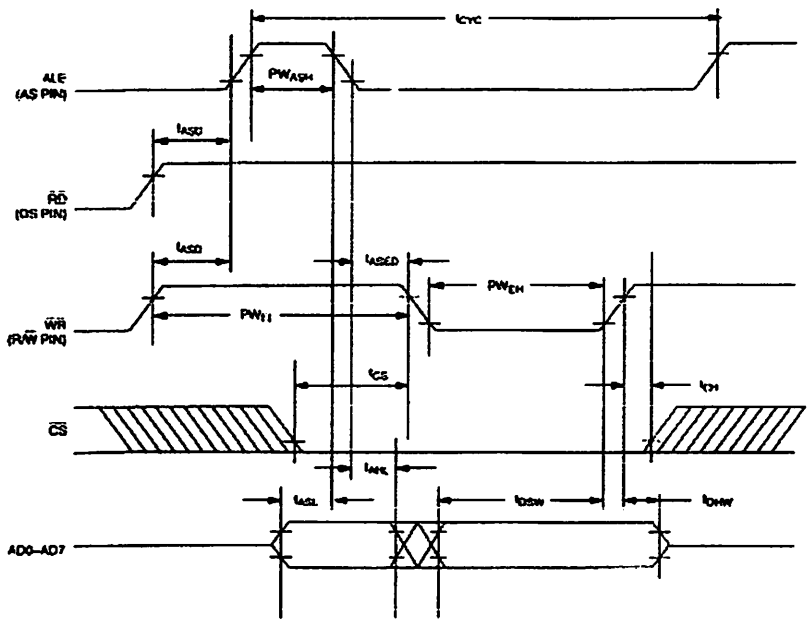
OUTPUT LOAD Figure 4



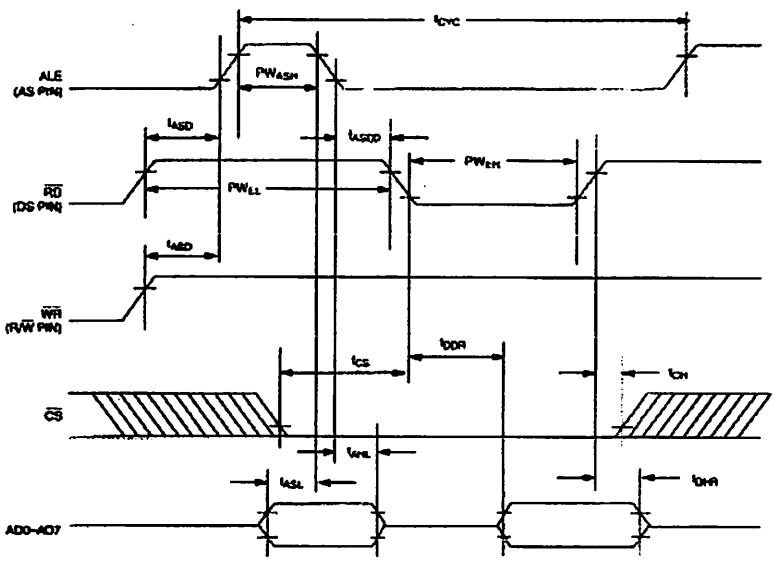
DS12887 BUS TIMING FOR MOTOROLA INTERFACE



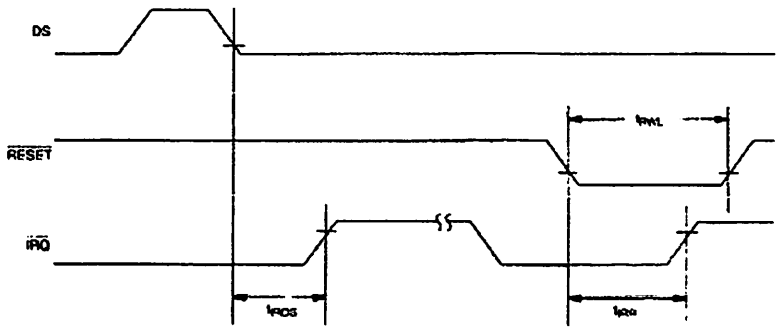
DS12887 BUS TIMING FOR INTEL INTERFACE WRITE CYCLE



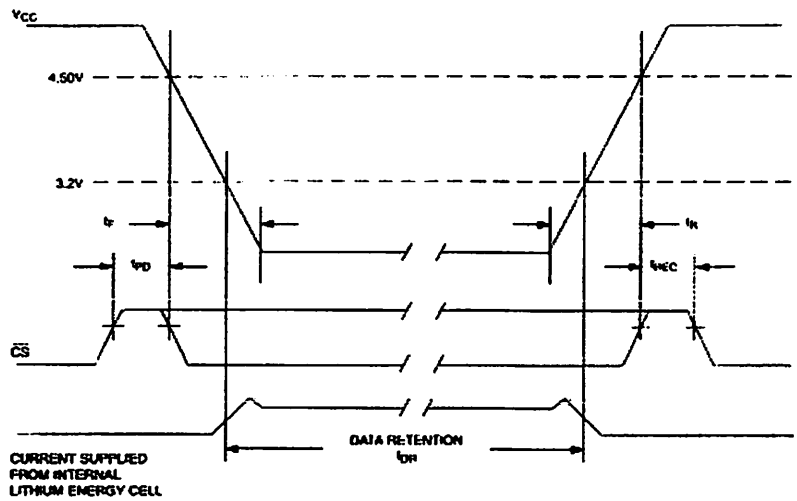
DS12887 BUS TIMING FOR INTEL INTERFACE READ CYCLE



DS12887 IRQ RELEASE DELAY TIMING



POWER-DOWN/POWER-UP TIMING



POWER-DOWN/POWER-UP TIMING

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
$\overline{CS}$ at V_{IH} before Power-Down	t_{PD}	0			µs	
V_{CC} Slew from 4.5V to 0V ($\overline{CS}$ at V_{IH})	t_F	300			µs	
V_{CC} Slew from 0V to 4.5V ($\overline{CS}$ at V_{IH})	t_R	100			µs	
$\overline{CS}$ at V_{IH} after Power-Up	t_{REC}	20		200	ms	

(t_A = 25°C)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Expected Data Retention	t_{DR}	10			years	

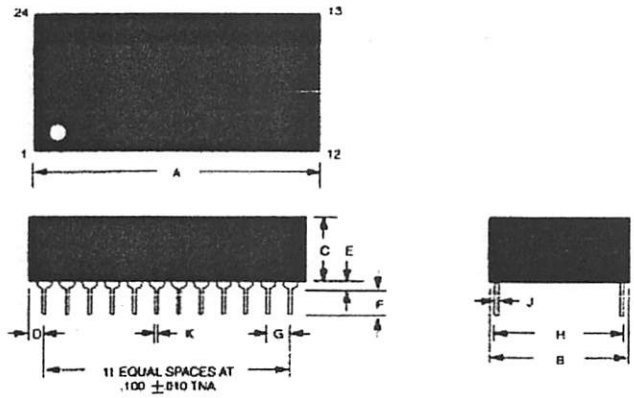
NOTE:

The real time clock will keep time to an accuracy of ±1 minute per month during data retention time for the period of t_{DR}.

WARNING:

Under no circumstances are negative undershoots, of any amplitude, allowed when device is in battery backup mode.

DS12887 REAL TIME CLOCK PLUS RAM



PKG	24-PIN	
DIM	MIN	MAX
A IN.	1.320	1.335
MM	33.53	33.91
B IN.	0.675	0.700
MM	17.15	17.78
C IN.	0.345	0.370
MM	8.76	9.40
D IN.	0.100	0.130
MM	2.54	3.30
E IN.	0.015	0.030
MM	0.38	0.76
F IN.	0.110	0.140
MM	2.79	3.56
G IN.	0.090	0.110
MM	2.29	2.79
H IN.	0.590	0.630
MM	14.99	16.00
J IN.	0.008	0.012
MM	0.20	0.30
K IN.	0.015	0.021
MM	0.38	0.53

NOTE: PINS 2, 3, 16, 20, 21 AND 22 ARE MISSING BY DESIGN.

DATA SHEET

PCF8591
8-bit A/D and D/A converter

Product specification
Supersedes data of 1997 Apr 02
File under Integrated Circuits, IC12

1998 Jul 02

Philips
Semiconductors

PHILIPS

CONTENTS

8-bit A/D and D/A converter PCF8591

1 FEATURES

- Single power supply
- Operating supply voltage 2.5 V to 6 V
- Low standby current
- Serial input/output via I²C-bus
- Address by 3 hardware address pins
- Sampling rate given by I²C-bus speed
- 4 analog inputs programmable as single-ended or differential inputs
- Auto-incremented channel selection
- Analog voltage range from V_{SS} to V_{DD}
- On-chip track and hold circuit
- 8-bit successive approximation A/D conversion
- Multiplying DAC with one analog output.

2 APPLICATIONS

- Closed loop control systems
- Low power converter for remote data acquisition
- Battery operated equipment
- Acquisition of analog values in automotive, audio and TV applications.

3 GENERAL DESCRIPTION

The PCF8591 is a single-chip, single-supply low power 8-bit CMOS data acquisition device with four analog inputs, one analog output and a serial I²C-bus interface. Three address pins A0, A1 and A2 are used for programming the hardware address, allowing the use of up to eight devices connected to the I²C-bus without additional hardware. Address, control and data to and from the device are transferred serially via the two-line bidirectional I²C-bus.

The functions of the device include analog input multiplexing, on-chip track and hold function, 8-bit analog-to-digital conversion and an 8-bit digital-to-analog conversion. The maximum conversion rate is given by the maximum speed of the I²C-bus.

4 ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
PCA8591P	DIP16	plastic dual in-line package; 16 leads (300 mil); long body	SOT38-1
PCA8591T	SO16	plastic small outline package; 16 leads; body width 7.5 mm	SOT162-1

5 BLOCK DIAGRAM

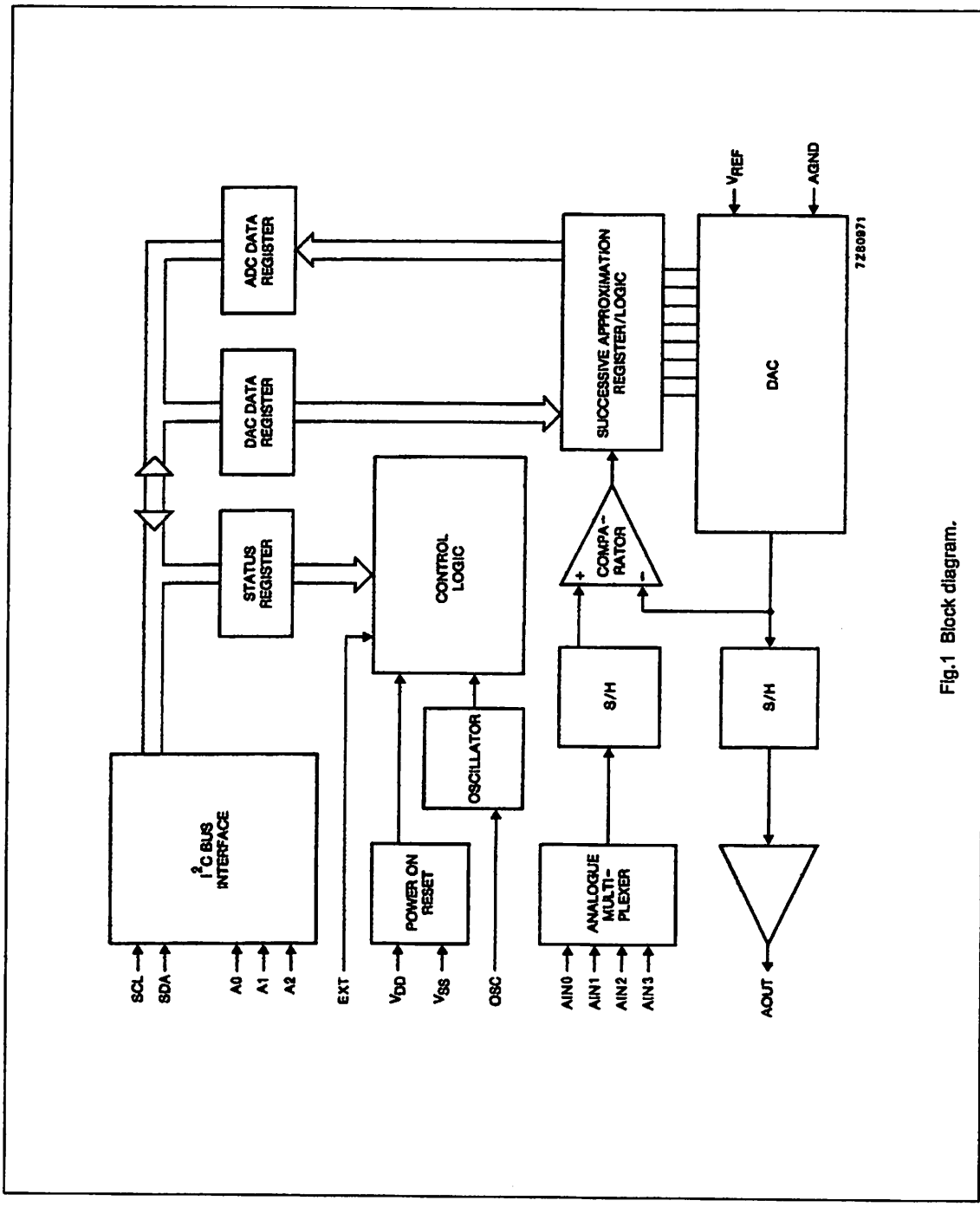


Fig.1 Block diagram.

6 PINNING

SYMBOL	PIN	DESCRIPTION
AINO	1	analog inputs (A/D converter)
AIN1	2	
AIN2	3	
AIN3	4	
A0	5	hardware address
A1	6	
A2	7	
V_{SS}	8	negative supply voltage
SDA	9	I^2C-bus data input/output
SCL	10	I^2C-bus clock input
OSC	11	oscillator input/output
EXT	12	external/internal switch for oscillator input
AGND	13	analog ground
V_{REF}	14	voltage reference input
AOUT	15	analog output (D/A converter)
V_{DD}	16	positive supply voltage

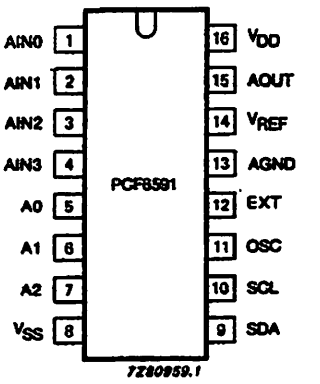


Fig.2 Pinning diagram.

7 FUNCTIONAL DESCRIPTION

7.1 Addressing

Each PCF8591 device in an I²C-bus system is activated by sending a valid address to the device. The address consists of a fixed part and a programmable part. The programmable part must be set according to the address pins A0, A1 and A2. The address always has to be sent as the first byte after the start condition in the I²C-bus protocol. The last bit of the address byte is the read/write-bit which sets the direction of the following data transfer (see Figs 3, 15 and 16).

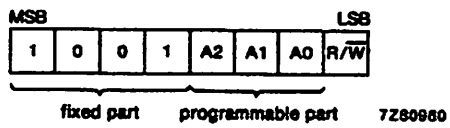


Fig.3 Address byte.

7.2 Control byte

The second byte sent to a PCF8591 device will be stored in its control register and is required to control the device function.

The upper nibble of the control register is used for enabling the analog output, and for programming the analog inputs as single-ended or differential inputs. The lower nibble selects one of the analog input channels defined by the upper nibble (see Fig.4). If the auto-increment flag is set the channel number is incremented automatically after each A/D conversion.

If the auto-increment mode is desired in applications where the internal oscillator is used, the analog output enable flag in the control byte (bit 6) should be set. This allows the internal oscillator to run continuously, thereby preventing conversion errors resulting from oscillator start-up delay. The analog output enable flag may be reset at other times to reduce quiescent power consumption.

The selection of a non-existing input channel results in the highest available channel number being allocated. Therefore, if the auto-increment flag is set, the next selected channel will be always channel 0. The most significant bits of both nibbles are reserved for future functions and have to be set to 0. After a Power-on reset condition all bits of the control register are reset to 0. The D/A converter and the oscillator are disabled for power saving. The analog output is switched to a high-impedance state.

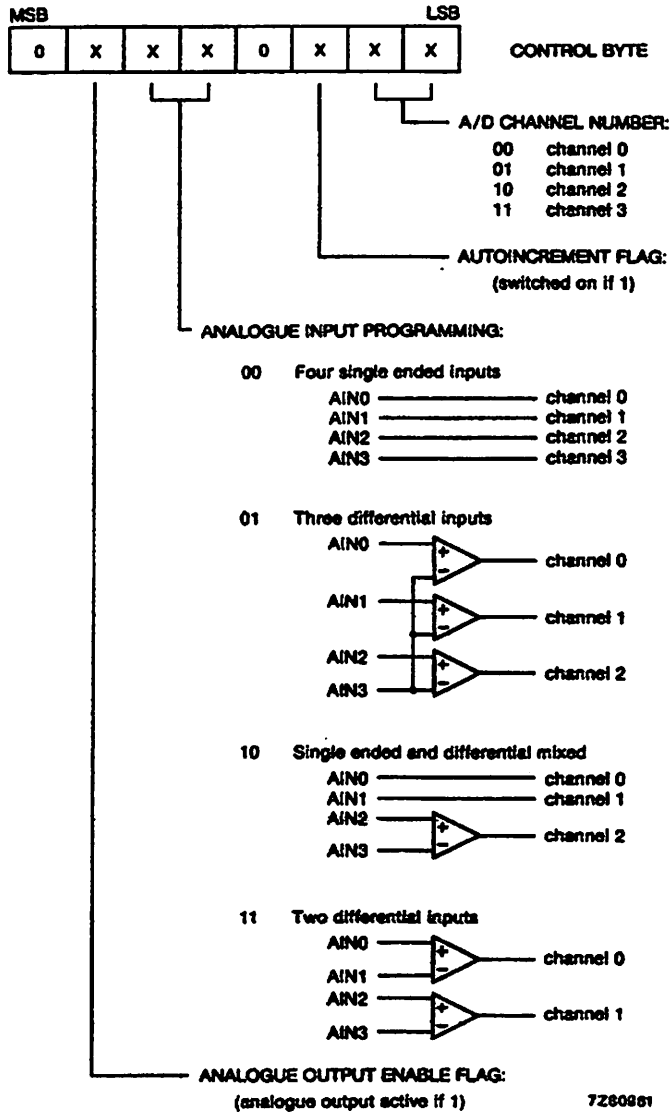


Fig.4 Control byte.

7.3 D/A conversion

The third byte sent to a PCF8591 device is stored in the DAC data register and is converted to the corresponding analog voltage using the on-chip D/A converter. This D/A converter consists of a resistor divider chain connected to the external reference voltage with 256 taps and selection switches. The tap-decoder switches one of these taps to the DAC output line (see Fig.5).

The analog output voltage is buffered by an auto-zeroed unity gain amplifier. This buffer amplifier may be switched on or off by setting the analog output enable flag of the control register. In the active state the output voltage is held until a further data byte is sent.

The on-chip D/A converter is also used for successive approximation A/D conversion. In order to release the DAC for an A/D conversion cycle the unity gain amplifier is equipped with a track and hold circuit. This circuit holds the output voltage while executing the A/D conversion.

The output voltage supplied to the analog output AOUT is given by the formula shown in Fig.6. The waveforms of a D/A conversion sequence are shown in Fig.7.

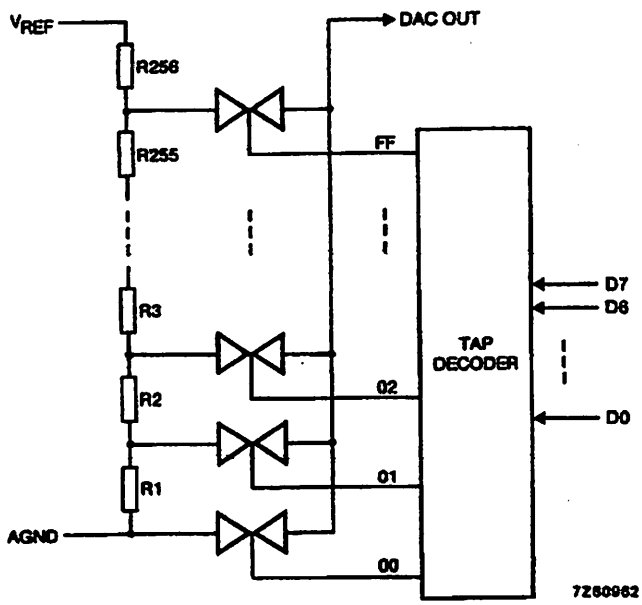


Fig.5 DAC resistor divider chain.

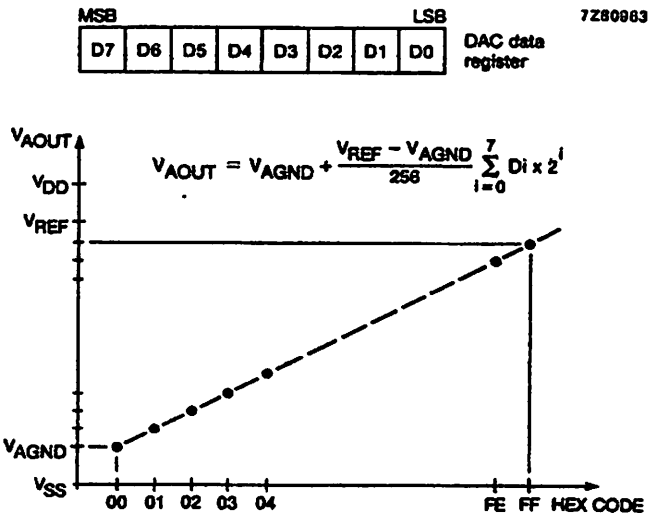


Fig.6 DAC data and DC conversion characteristics.

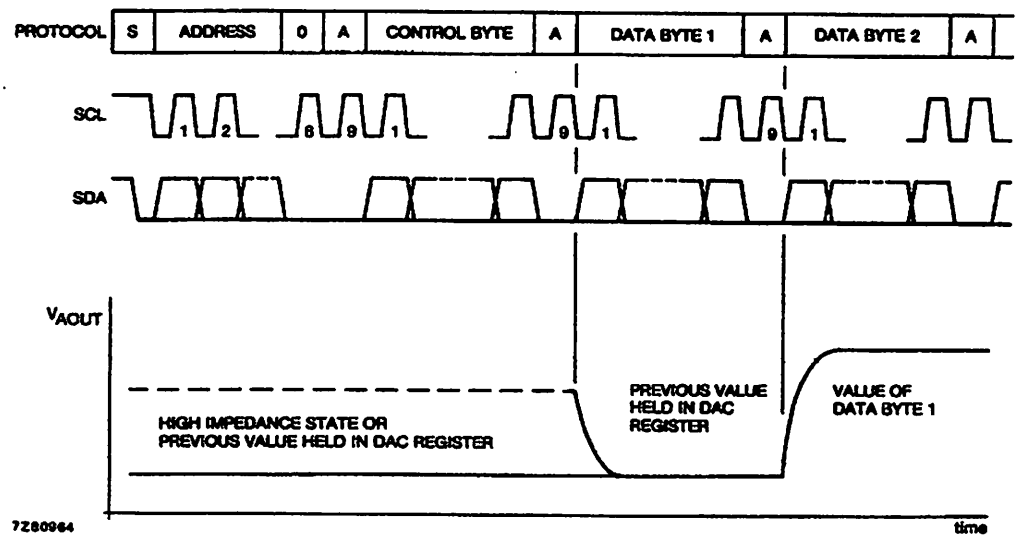


Fig.7 D/A conversion sequence.

7.4 A/D conversion

The A/D converter makes use of the successive approximation conversion technique. The on-chip D/A converter and a high-gain comparator are used temporarily during an A/D conversion cycle.

An A/D conversion cycle is always started after sending a valid read mode address to a PCF8591 device. The A/D conversion cycle is triggered at the trailing edge of the acknowledge clock pulse and is executed while transmitting the result of the previous conversion (see Fig.8).

Once a conversion cycle is triggered an input voltage sample of the selected channel is stored on the chip and is converted to the corresponding 8-bit binary code. Samples picked up from differential inputs are converted to an 8-bit two's complement code (see Figs 9 and 10).

The conversion result is stored in the ADC data register and awaits transmission. If the auto-increment flag is set the next channel is selected.

The first byte transmitted in a read cycle contains the conversion result code of the previous read cycle. After a Power-on reset condition the first byte read is a hexadecimal 80. The protocol of an I²C-bus read cycle is shown in Chapter 8, Figs 15 and 16.

The maximum A/D conversion rate is given by the actual speed of the I²C-bus.

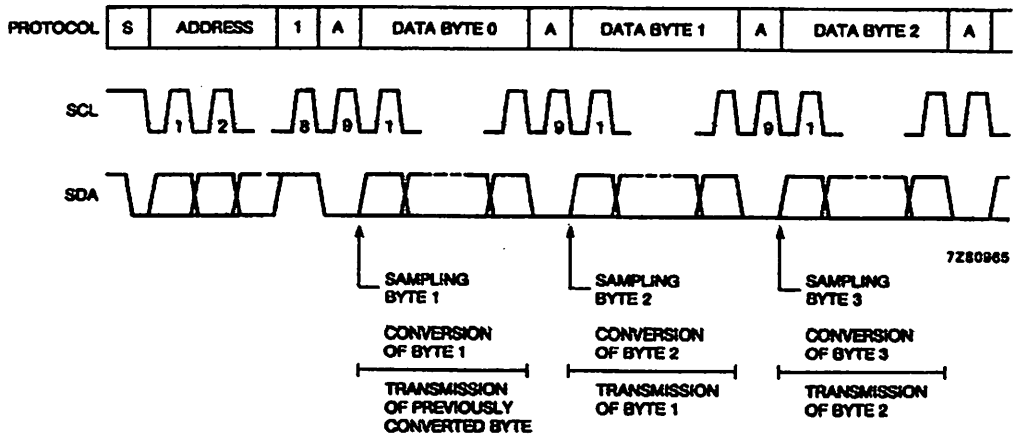


Fig.8 A/D conversion sequence.

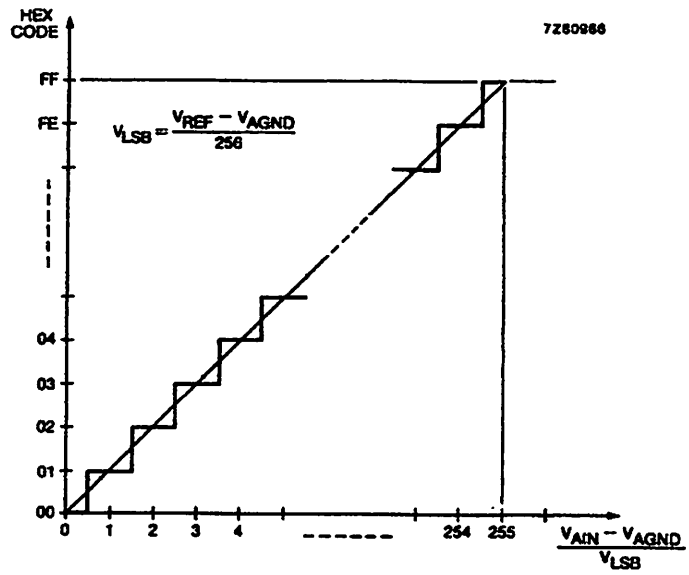


Fig.9 A/D conversion characteristics of single-ended inputs.

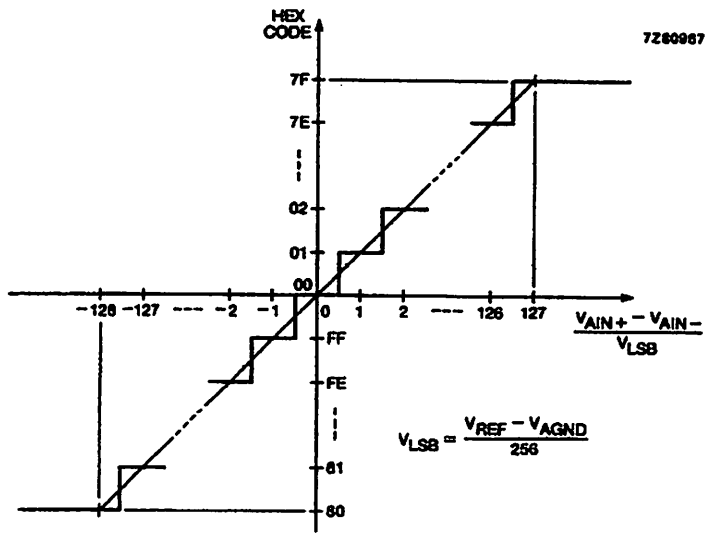


Fig.10 A/D conversion characteristics of differential inputs.

7.5 Reference voltage

For the D/A and A/D conversion either a stable external voltage reference or the supply voltage has to be applied to the resistor divider chain (pins V_{REF} and AGND). The AGND pin has to be connected to the system analog ground and may have a DC off-set with reference to V_{SS}.

A low frequency may be applied to the V_{REF} and AGND pins. This allows the use of the D/A converter as a one-quadrant multiplier; see Chapter 15 and Fig.6.

The A/D converter may also be used as a one or two quadrant analog divider. The analog input voltage is divided by the reference voltage. The result is converted to a binary code. In this application the user has to keep the reference voltage stable during the conversion cycle.

7.6 Oscillator

An on-chip oscillator generates the clock signal required for the A/D conversion cycle and for refreshing the auto-zeroed buffer amplifier. When using this oscillator the EXT pin has to be connected to V_{SS}. At the OSC pin the oscillator frequency is available.

If the EXT pin is connected to V_{DD} the oscillator output OSC is switched to a high-impedance state allowing the user to feed an external clock signal to OSC.

8 CHARACTERISTICS OF THE I²C-BUS

The I²C-bus is for bidirectional, two-line communication between different ICs or modules. The two lines are a serial data line (SDA) and a serial clock line (SCL). Both lines must be connected to a positive supply via a pull-up resistor. Data transfer may be initiated only when the bus is not busy.

8.1 Bit transfer

One data bit is transferred during each clock pulse. The data on the SDA line must remain stable during the HIGH period of the clock pulse as changes in the data line at this time will be interpreted as a control signal.

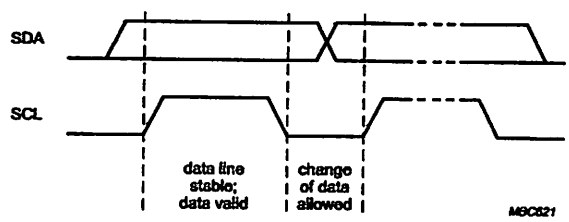


Fig.11 Bit transfer.

8.2 Start and stop conditions

Both data and clock lines remain HIGH when the bus is not busy. A HIGH-to-LOW transition of the data line, while the clock is HIGH, is defined as the start condition (S). A LOW-to-HIGH transition of the data line while the clock is HIGH, is defined as the stop condition (P).

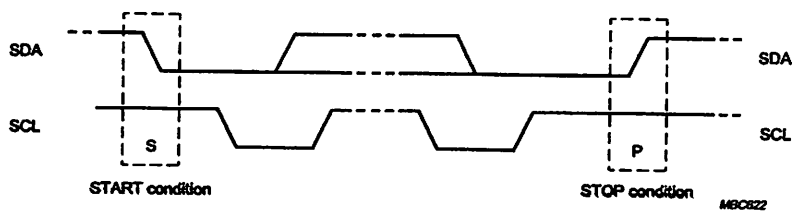


Fig.12 Definition of START and STOP condition.

8.3 System configuration

A device generating a message is a 'transmitter', a device receiving a message is the 'receiver'. The device that controls the message is the 'master' and the devices which are controlled by the master are the 'slaves'.

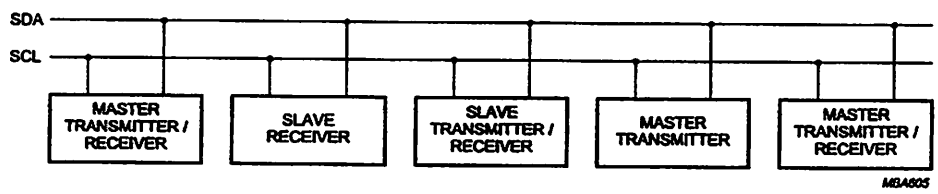


Fig.13 System configuration.

8.4 Acknowledge

The number of data bytes transferred between the start and stop conditions from transmitter to receiver is not limited. Each data byte of eight bits is followed by one acknowledge bit. The acknowledge bit is a HIGH level put on the bus by the transmitter whereas the master also generates an extra acknowledge related clock pulse. A slave receiver which is addressed must generate an acknowledge after the reception of each byte. Also a master must generate an acknowledge after the reception of each byte that has been clocked out of the slave transmitter. The device that acknowledges has to pull down the SDA line during the acknowledge clock pulse, so that the SDA line is stable LOW during the HIGH period of the acknowledge related clock pulse. A master receiver must signal an end of data to the transmitter by not generating an acknowledge on the last byte that has been clocked out of the slave. In this event the transmitter must leave the data line HIGH to enable the master to generate a stop condition.

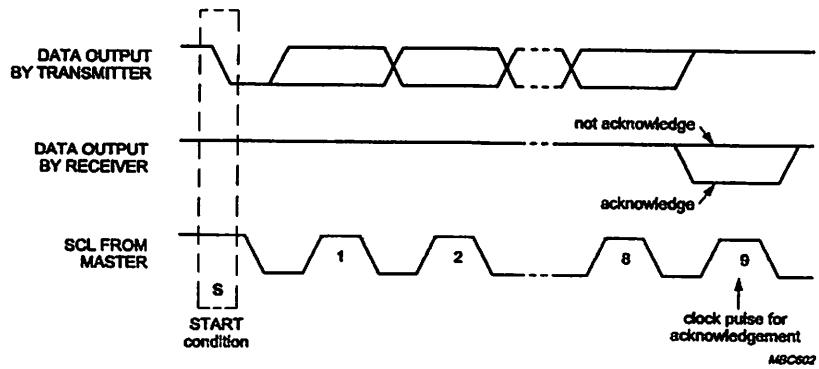


Fig.14 Acknowledgement on the I²C-bus.

8.5 I²C-bus protocol

After a start condition a valid hardware address has to be sent to a PCF8591 device. The read/write bit defines the direction of the following single or multiple byte data transfer. For the format and the timing of the start condition (S), the stop condition (P) and the acknowledge bit (A) refer to the I²C-bus characteristics. In the write mode a data transfer is terminated by sending either a stop condition or the start condition of the next data transfer.

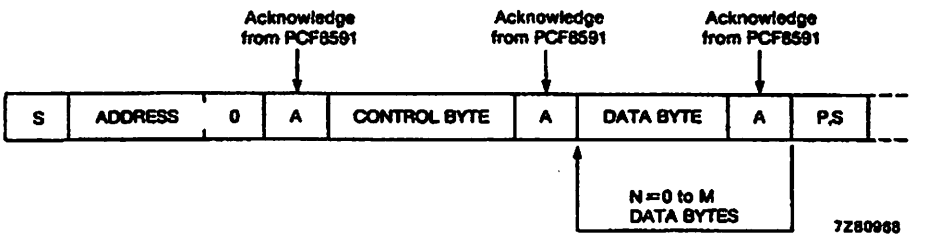


Fig.15 Bus protocol for write mode, D/A conversion.

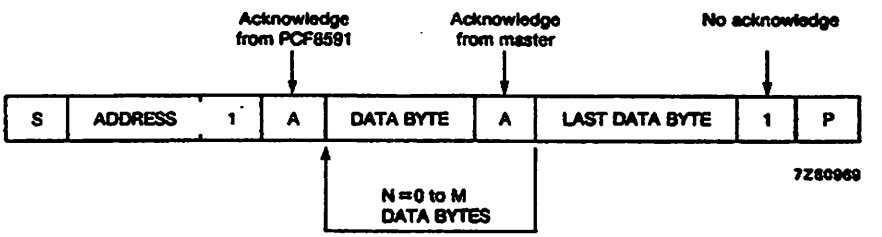


Fig.16 Bus protocol for read mode, A/D conversion.

9 LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134).

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
V_{DD}	supply voltage (pin 16)	−0.5	+8.0	V
V_I	input voltage (any input)	−0.5	V_{DD} + 0.5	V
I_I	DC input current	−	±10	mA
I_O	DC output current	−	±20	mA
I_{DD}, I_{SS}	V_{DD} or V_{SS} current	−	±50	mA
P_{tot}	total power dissipation per package	−	300	mW
P_O	power dissipation per output	−	100	mW
T_{amb}	operating ambient temperature	−40	+85	°C
T_{stg}	storage temperature	−65	+150	°C

10 HANDLING

Inputs and outputs are protected against electrostatic discharge in normal handling. However, to be totally safe, it is desirable to take precautions appropriate to handling MOS devices. Advice can be found in Data Handbook IC12 under *"Handling MOS Devices"*.

11 DC CHARACTERISTICS

V_{DD} = 2.5 V to 6 V; V_{SS} = 0 V; T_{amb} = −40 °C to +85 °C unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Supply						
V_{DD}	supply voltage (operating)		2.5	–	6.0	V
I_{DD}	supply current					
	standby	$V_I = V_{SS}$ or V_{DD}; no load	–	1	15	µA
	operating, AOUT off	f_{SCL} = 100 kHz	–	125	250	µA
	operating, AOUT active	f_{SCL} = 100 kHz	–	0.45	1.0	mA
V_{POR}	Power-on reset level	note 1	0.8	–	2.0	V
Digital inputs/output: SCL, SDA, A0, A1, A2						
V_{IL}	LOW level input voltage		0	–	$0.3 \times V_{DD}$	V
V_{IH}	HIGH level input voltage		$0.7 \times V_{DD}$	–	V_{DD}	V
I_L	leakage current					
	A0, A1, A2	$V_I = V_{SS}$ to V_{DD}	−250	–	+250	nA
	SCL, SDA	$V_I = V_{SS}$ to V_{DD}	−1	–	+1	µA
C_I	input capacitance		–	–	5	pF
I_{OL}	LOW level SDA output current	V_{OL} = 0.4 V	3.0	–	–	mA
Reference voltage inputs						
V_{REF}	reference voltage	$V_{REF} > V_{AGND}$; note 2	V_{SS} + 1.6	–	V_{DD}	V
V_{AGND}	analog ground voltage	$V_{REF} > V_{AGND}$; note 2	V_{SS}	–	V_{DD} − 0.8	V
I_{LI}	input leakage current		−250	–	+250	nA
R_{REF}	input resistance	pins V_{REF} and AGND	–	100	–	kΩ
Oscillator: OSC, EXT						
I_{LI}	input leakage current		–	–	250	nA
f_{OSC}	oscillator frequency		0.75	–	1.25	MHz

Notes

1. The power on reset circuit resets the I²C-bus logic when V_{DD} is less than V_{POR}.
2. A further extension of the range is possible, if the following conditions are fulfilled:

$$\frac{V_{REF} + V_{AGND}}{2} \geq 0.8V, V_{DD} - \frac{V_{REF} + V_{AGND}}{2} \geq 0.4V$$

12 D/A CHARACTERISTICS

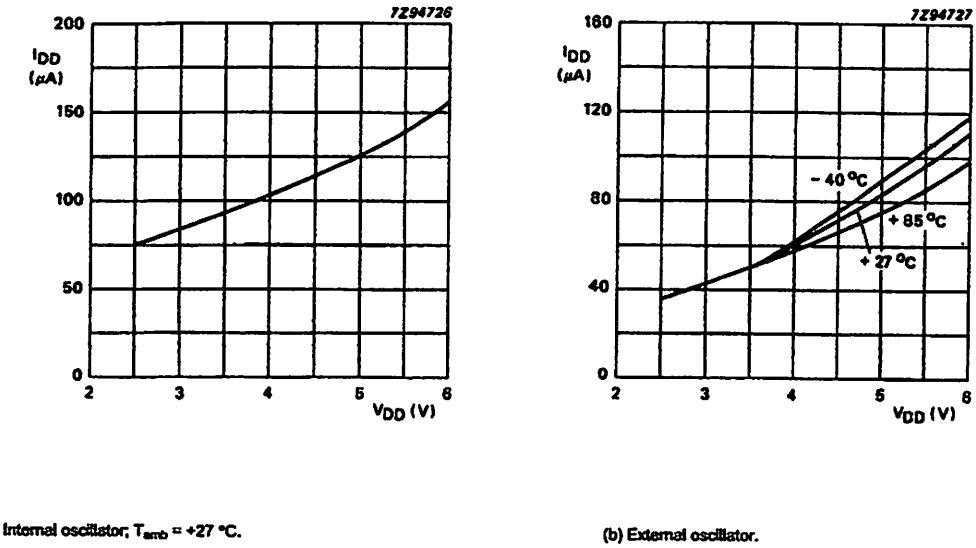
V_{DD} = 5.0 V; V_{SS} = 0 V; V_{REF} = 5.0 V; V_{AGND} = 0 V; R_L = 10 kΩ; C_L = 100 pF; T_{amb} = –40 °C to +85 °C unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Analog output						
V_{OA}	output voltage	no resistive load	V_{SS}	–	V_{DD}	V
		R_L = 10 kΩ	V_{SS}	–	0.9 × V_{DD}	V
I_{LO}	output leakage current	AOUT disabled	–	–	250	nA
Accuracy						
OS_e	offset error	T_{amb} = 25 °C	–	–	50	mV
L_e	linearity error		–	–	±1.5	LSB
G_e	gain error	no resistive load	–	–	1	%
t_{DAC}	settling time	to ½ LSB full scale step	–	–	90	µs
f_{DAC}	conversion rate		–	–	11.1	kHz
SNRR	supply noise rejection ratio	f = 100 Hz; V_{DDN} = 0.1 × V_{PP}	–	40	–	dB

13 A/D CHARACTERISTICS

V_{DD} = 5.0 V; V_{SS} = 0 V; V_{REF} = 5.0 V; V_{AGND} = 0 V; R_S = 10 kΩ; T_{amb} = –40 °C to +85 °C unless otherwise specified.

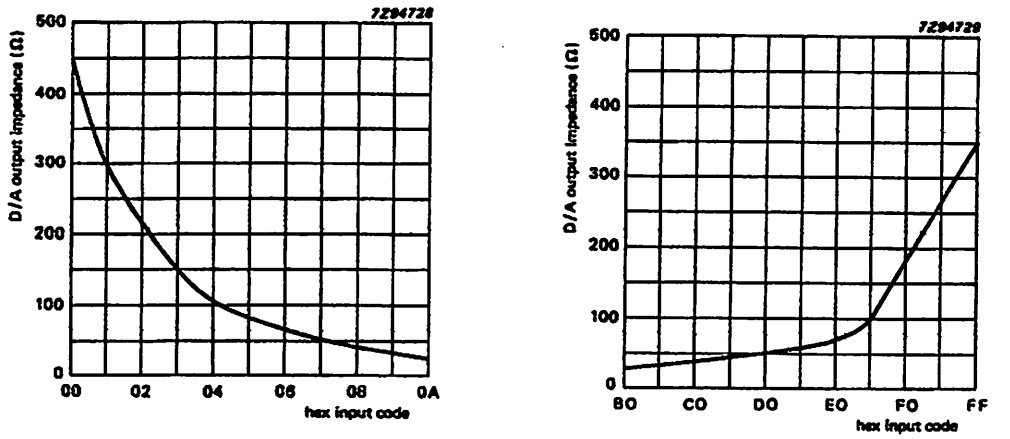
SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Analog inputs						
V_{IA}	analog input voltage		V_{SS}	–	V_{DD}	V
I_{LIA}	analog input leakage current		–	–	100	nA
C_{IA}	analog input capacitance		–	10	–	pF
C_{ID}	differential input capacitance		–	10	–	pF
V_{IS}	single-ended voltage	measuring range	V_{AGND}	–	V_{REF}	V
V_{ID}	differential voltage	measuring range; $V_{FS} = V_{REF} - V_{AGND}$	$\frac{-V_{FS}}{2}$	–	$\frac{+V_{FS}}{2}$	V
Accuracy						
OS_e	offset error	T_{amb} = 25 °C	–	–	20	mV
L_e	linearity error		–	–	±1.5	LSB
G_e	gain error		–	–	1	%
GS_e	small-signal gain error	ΔV_i = 16 LSB	–	–	5	%
CMRR	common-mode rejection ratio		–	60	–	dB
SNRR	supply noise rejection ratio	f = 100 Hz; V_{DDN} = 0.1 × V_{PP}	–	40	–	dB
t_{ADC}	conversion time		–	–	90	µs
f_{ADC}	sampling/conversion rate		–	–	11.1	kHz



(a) Internal oscillator; T_{amb} = +27 °C.

(b) External oscillator.

Fig.17 Operating supply current as a function of supply voltage (analog output disabled).



(a) Output impedance near negative power rail; T_{amb} = +27 °C.

(b) Output impedance near positive power rail; T_{amb} = +27 °C.

The x-axis represents the hex input-code equivalent of the output voltage.

Fig.18 Output impedance of analog output buffer (near power rails).

14 AC CHARACTERISTICS

All timing values are valid within the operating supply voltage and ambient temperature range and reference to V_{IL} and V_{IH} with an input voltage swing of V_{SS} to V_{DD}.

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
I²C-bus timing (see Fig.19; note 1)					
f_{SCL}	SCL clock frequency	–	–	100	kHz
t_{SP}	tolerable spike width on bus	–	–	100	ns
t_{BUF}	bus free time	4.7	–	–	µs
$t_{SU;STA}$	START condition set-up time	4.7	–	–	µs
$t_{HD;STA}$	START condition hold time	4.0	–	–	µs
t_{LOW}	SCL LOW time	4.7	–	–	µs
t_{HIGH}	SCL HIGH time	4.0	–	–	µs
t_r	SCL and SDA rise time	–	–	1.0	µs
t_f	SCL and SDA fall time	–	–	0.3	µs
$t_{SU;DAT}$	data set-up time	250	–	–	ns
$t_{HD;DAT}$	data hold time	0	–	–	ns
$t_{VD;DAT}$	SCL LOW-to-data out valid	–	–	3.4	µs
$t_{SU;STO}$	STOP condition set-up time	4.0	–	–	µs

Note

1. A detailed description of the I²C-bus specification, with applications, is given in brochure *"The I²C-bus and how to use it"*. This brochure may be ordered using the code 9398 393 40011.

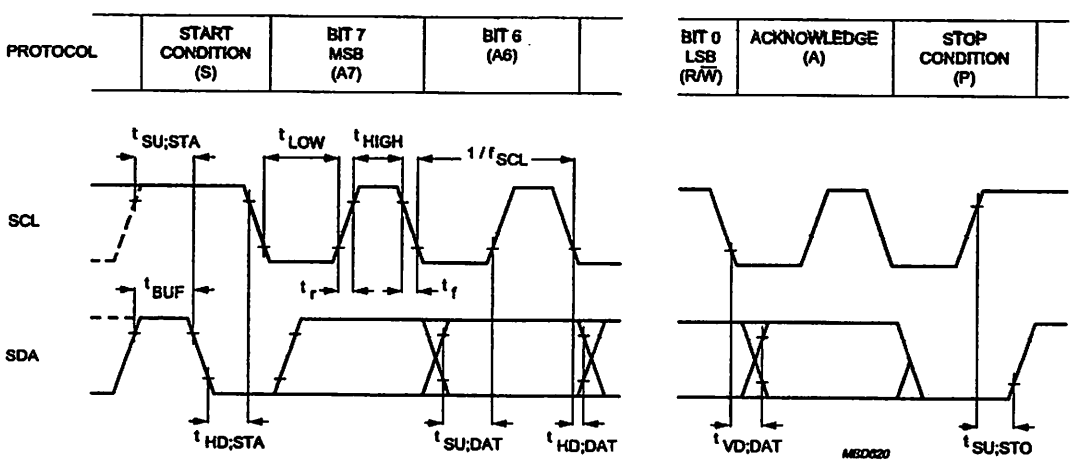


Fig.19 I²C-bus timing diagram; rise and fall times refer to V_{IL} and V_{IH}.

15 APPLICATION INFORMATION

Inputs must be connected to V_{SS} or V_{DD} when not in use. Analog inputs may also be connected to AGND or V_{REF}.

In order to prevent excessive ground and supply noise and to minimize cross-talk of the digital to analog signal paths the user has to design the printed-circuit board layout very carefully. Supply lines common to a PCF8591 device and noisy digital circuits and ground loops should be avoided. Decoupling capacitors (>10 μF) are recommended for power supply and reference voltage inputs.

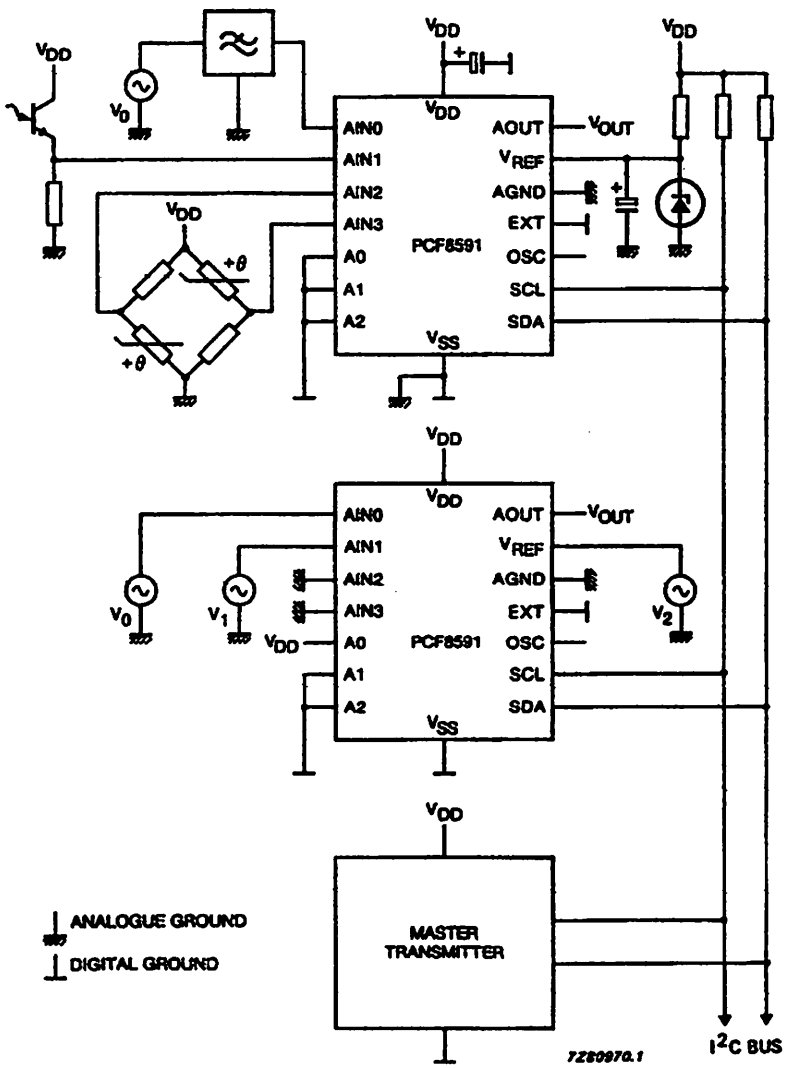
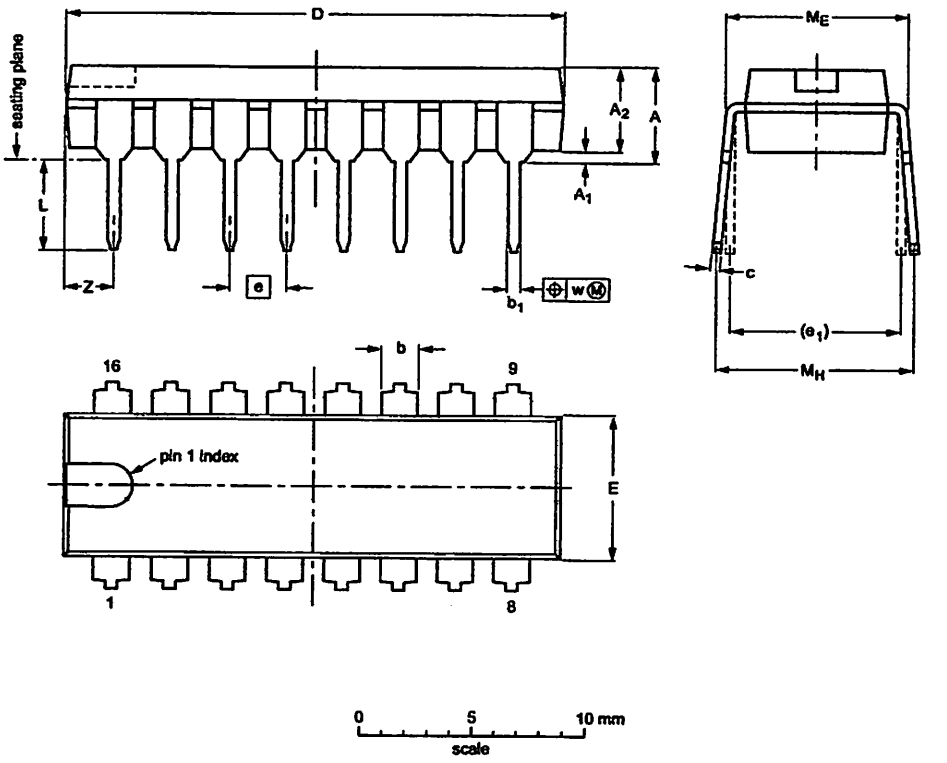


Fig.20 Application diagram.

16 PACKAGE OUTLINES

DIP16: plastic dual in-line package; 16 leads (300 mil); long body **SOT38-1**



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

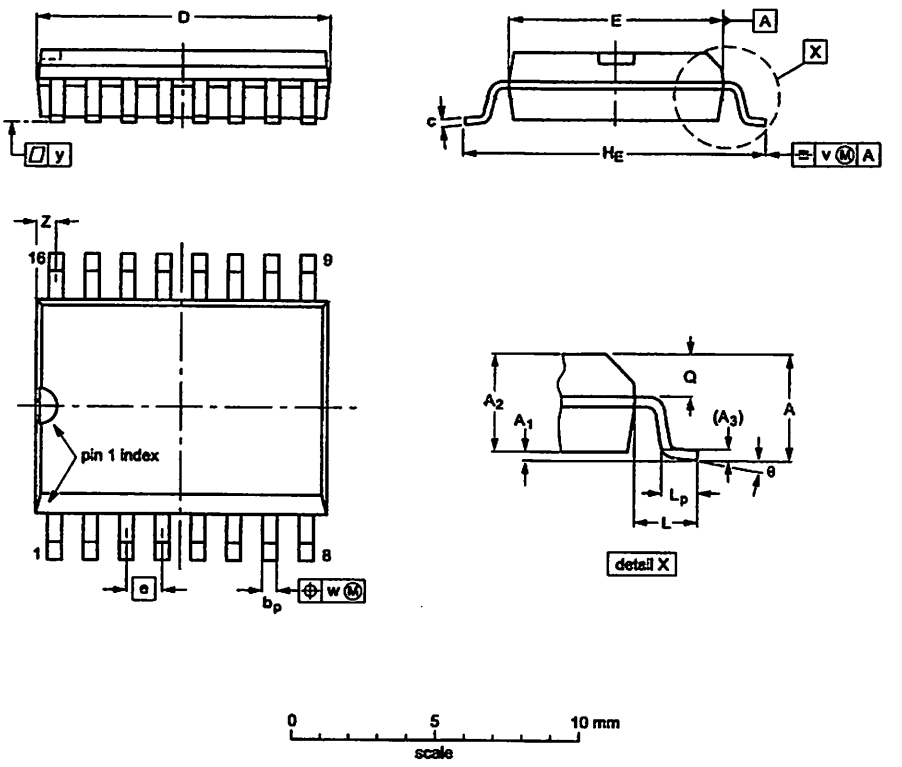
UNIT	A max.	A_1 min.	A_2 max.	b	b_1	c	$D^{(1)}$	$E^{(1)}$	e	e_1	L	M_E	M_H	w	$Z^{(1)}$ max.
mm	4.7	0.51	3.7	1.40 1.14	0.53 0.38	0.32 0.23	21.8 21.4	6.48 6.20	2.54	7.62	3.9 3.4	8.25 7.80	9.5 8.3	0.254	2.2
inches	0.19	0.020	0.15	0.055 0.045	0.021 0.015	0.013 0.009	0.86 0.84	0.26 0.24	0.10	0.30	0.15 0.13	0.32 0.31	0.37 0.33	0.01	0.087

Note

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT38-1	050G09	MO-001AE				~~92-10-02~~ 95-01-19

SO16: plastic small outline package; 16 leads; body width 7.5 mm **SOT162-1**



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(1)}$	e	H_E	L	L_p	Q	v	w	y	$Z^{(1)}$	θ
mm	2.65	0.30 0.10	2.45 2.25	0.25	0.49 0.36	0.32 0.23	10.5 10.1	7.6 7.4	1.27	10.65 10.00	1.4	1.1 0.4	1.1 1.0	0.25	0.25	0.1	0.9 0.4	8° 0°
inches	0.10	0.012 0.004	0.096 0.089	0.01	0.019 0.014	0.013 0.009	0.41 0.40	0.30 0.29	0.050	0.419 0.394	0.055	0.043 0.016	0.043 0.039	0.01	0.01	0.004	0.035 0.016	

Note

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT162-1	075E03	MS-013AA				~~95-01-24~~ 97-05-22

17 SOLDERING

17.1 Introduction

There is no soldering method that is ideal for all IC packages. Wave soldering is often preferred when through-hole and surface mounted components are mixed on one printed-circuit board. However, wave soldering is not always suitable for surface mounted ICs, or for printed-circuits with high population densities. In these situations reflow soldering is often used.

This text gives a very brief insight to a complex technology. A more in-depth account of soldering ICs can be found in our *"Data Handbook IC26; Integrated Circuit Packages"* (order code 9398 652 90011).

17.2 DIP

17.2.1 SOLDERING BY DIPPING OR BY WAVE

The maximum permissible temperature of the solder is 260 °C; solder at this temperature must not be in contact with the joint for more than 5 seconds. The total contact time of successive solder waves must not exceed 5 seconds.

The device may be mounted up to the seating plane, but the temperature of the plastic body must not exceed the specified maximum storage temperature ($T_{stg\ max}$). If the printed-circuit board has been pre-heated, forced cooling may be necessary immediately after soldering to keep the temperature within the permissible limit.

17.2.2 REPAIRING SOLDERED JOINTS

Apply a low voltage soldering iron (less than 24 V) to the lead(s) of the package, below the seating plane or not more than 2 mm above it. If the temperature of the soldering iron bit is less than 300 °C it may remain in contact for up to 10 seconds. If the bit temperature is between 300 and 400 °C, contact may be up to 5 seconds.

17.3 SO

17.3.1 REFLOW SOLDERING

Reflow soldering techniques are suitable for all SO packages.

Reflow soldering requires solder paste (a suspension of fine solder particles, flux and binding agent) to be applied to the printed-circuit board by screen printing, stencilling or pressure-syringe dispensing before package placement.

Several techniques exist for reflowing; for example, thermal conduction by heated belt. Dwell times vary between 50 and 300 seconds depending on heating method. Typical reflow temperatures range from 215 to 250 °C.

Preheating is necessary to dry the paste and evaporate the binding agent. Preheating duration: 45 minutes at 45 °C.

17.3.2 WAVE SOLDERING

Wave soldering techniques can be used for all SO packages if the following conditions are observed:

- A double-wave (a turbulent wave with high upward pressure followed by a smooth laminar wave) soldering technique should be used.
- The longitudinal axis of the package footprint must be parallel to the solder flow.
- The package footprint must incorporate solder thieves at the downstream end.

During placement and before soldering, the package must be fixed with a droplet of adhesive. The adhesive can be applied by screen printing, pin transfer or syringe dispensing. The package can be soldered after the adhesive is cured.

Maximum permissible solder temperature is 260 °C, and maximum duration of package immersion in solder is 10 seconds, if cooled to less than 150 °C within 6 seconds. Typical dwell time is 4 seconds at 250 °C.

A mildly-activated flux will eliminate the need for removal of corrosive residues in most applications.

17.3.3 REPAIRING SOLDERED JOINTS

Fix the component by first soldering two diagonally-opposite end leads. Use only a low voltage soldering iron (less than 24 V) applied to the flat part of the lead. Contact time must be limited to 10 seconds at up to 300 °C. When using a dedicated tool, all other leads can be soldered in one operation within 2 to 5 seconds between 270 and 320 °C.

18 DEFINITIONS

Data sheet status	
Objective specification	This data sheet contains target or goal specifications for product development.
Preliminary specification	This data sheet contains preliminary data; supplementary data may be published later.
Product specification	This data sheet contains final product specifications.
Limiting values	
Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.	
Application information	
Where application information is given, it is advisory and does not form part of the specification.	

19 LIFE SUPPORT APPLICATIONS

These products are not designed for use in life support appliances, devices, or systems where malfunction of these products can reasonably be expected to result in personal injury. Philips customers using or selling these products for use in such applications do so at their own risk and agree to fully indemnify Philips for any damages resulting from such improper use or sale.

20 PURCHASE OF PHILIPS I²C COMPONENTS

Purchase of Philips I²C components conveys a license under the Philips' I²C patent to use the components in the I²C system provided the system conforms to the I²C specification defined by Philips. This specification can be ordered using the code 9398 393 40011.

National Semiconductor

January 2000

LM386
Low Voltage Audio Power Amplifier

General Description

The LM386 is a power amplifier designed for use in low voltage consumer applications. The gain is internally set to 20 to keep external part count low, but the addition of an external resistor and capacitor between pins 1 and 8 will increase the gain to any value up to 200.

The inputs are ground referenced while the output is automatically biased to one half the supply voltage. The quiescent power drain is only 24 milliwatts when operating from a 6 volt supply, making the LM386 ideal for battery operation.

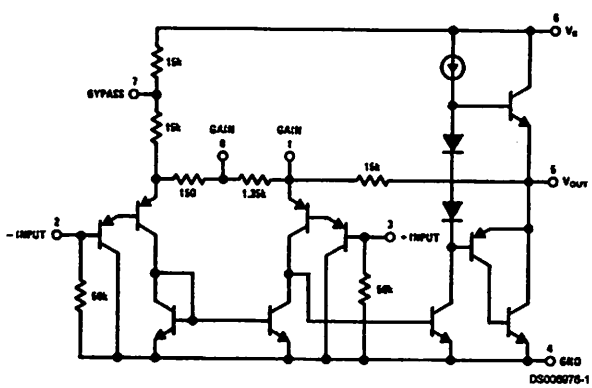
Features

- Battery operation
- Minimum external parts
- Wide supply voltage range: 4V–12V or 5V–18V
- Low quiescent current drain: 4 mA
- Voltage gains from 20 to 200
- Ground referenced input
- Self-centering output quiescent voltage
- Low distortion
- Available in 8 pin MSOP package

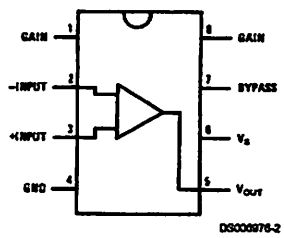
Applications

- AM-FM radio amplifiers
- Portable tape player amplifiers
- Intercoms
- TV sound systems
- Line drivers
- Ultrasonic drivers
- Small servo drivers
- Power converters

Equivalent Schematic and Connection Diagrams



Small Outline, Molded Mini Small Outline, and Dual-In-Line Packages



Top View
Order Number LM386M-1, LM386MM-1, LM386N-1, LM386N-3 or LM386N-4
See NS Package Number M08A, MUA08A or N08E

Absolute Maximum Ratings (Note 2)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Supply Voltage	
(LM386N-1, -3, LM386M-1)	15V
Supply Voltage (LM386N-4)	22V
Package Dissipation (Note 3)	
(LM386N)	1.25W
(LM386M)	0.73W
(LM386MM-1)	0.595W
Input Voltage	±0.4V
Storage Temperature	−65°C to +150°C
Operating Temperature	0°C to +70°C
Junction Temperature	+150°C
Soldering Information	
Dual-In-Line Package	
Soldering (10 sec)	+260°C
Small Outline Package	
(SOIC and MSOP)	
Vapor Phase (60 sec)	+215°C
Infrared (15 sec)	+220°C

See AN-450 "Surface Mounting Methods and Their Effect on Product Reliability" for other methods of soldering surface mount devices.

Thermal Resistance	
θ_{JC} (DIP)	37°C/W
θ_{JA} (DIP)	107°C/W
θ_{JC} (SO Package)	35°C/W
θ_{JA} (SO Package)	172°C/W
θ_{JA} (MSOP)	210°C/W
θ_{JC} (MSOP)	56°C/W

Electrical Characteristics (Notes 1, 2)

T_A = 25°C

Parameter	Conditions	Min	Typ	Max	Units
Operating Supply Voltage (V_S)					
LM386N-1, -3, LM386M-1, LM386MM-1		4		12	V
LM386N-4		5		18	V
Quiescent Current (I_Q)	V_S = 6V, V_{IN} = 0		4	8	mA
Output Power (P_{OUT})					
LM386N-1, LM386M-1, LM386MM-1	V_S = 6V, R_L = 8Ω, THD = 10%	250	325		mW
LM386N-3	V_S = 9V, R_L = 8Ω, THD = 10%	500	700		mW
LM386N-4	V_S = 16V, R_L = 32Ω, THD = 10%	700	1000		mW
Voltage Gain (A_V)	V_S = 6V, f = 1 kHz		26		dB
	10 µF from Pin 1 to 8		46		dB
Bandwidth (BW)	V_S = 6V, Pins 1 and 8 Open		300		kHz
Total Harmonic Distortion (THD)	V_S = 6V, R_L = 8Ω, P_{OUT} = 125 mW		0.2		%
	f = 1 kHz, Pins 1 and 8 Open				
Power Supply Rejection Ratio (PSRR)	V_S = 6V, f = 1 kHz, C_{BYPASS} = 10 µF		50		dB
	Pins 1 and 8 Open, Referred to Output				
Input Resistance (R_{IN})			50		kΩ
Input Bias Current (I_{BIAS})	V_S = 6V, Pins 2 and 3 Open		250		nA

Note 1: All voltages are measured with respect to the ground pin, unless otherwise specified.

Note 2: Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is functional, but do not guarantee specific performance limits. Electrical Characteristics state DC and AC electrical specifications under particular test conditions which guarantee specific performance limits. This assumes that the device is within the Operating Ratings. Specifications are not guaranteed for parameters where no limit is given, however, the typical value is a good indication of device performance.

Note 3: For operation in ambient temperatures above 25°C, the device must be derated based on a 150°C maximum junction temperature and 1) a thermal resistance of 107°C/W junction to ambient for the dual-in-line package and 2) a thermal resistance of 170°C/W for the small outline package.

Application Hints

GAIN CONTROL

To make the LM386 a more versatile amplifier, two pins (1 and 8) are provided for gain control. With pins 1 and 8 open the 1.35 kΩ resistor sets the gain at 20 (26 dB). If a capacitor is put from pin 1 to 8, bypassing the 1.35 kΩ resistor, the gain will go up to 200 (46 dB). If a resistor is placed in series with the capacitor, the gain can be set to any value from 20 to 200. Gain control can also be done by capacitively coupling a resistor (or FET) from pin 1 to ground.

Additional external components can be placed in parallel with the internal feedback resistors to tailor the gain and frequency response for individual applications. For example, we can compensate poor speaker bass response by frequency shaping the feedback path. This is done with a series RC from pin 1 to 5 (paralleling the internal 15 kΩ resistor). For 6 dB effective bass boost: R ≅ 15 kΩ, the lowest value for good stable operation is R = 10 kΩ if pin 8 is open. If pins 1 and 8 are bypassed then R as low as 2 kΩ can be used. This restriction is because the amplifier is only compensated for closed-loop gains greater than 9.

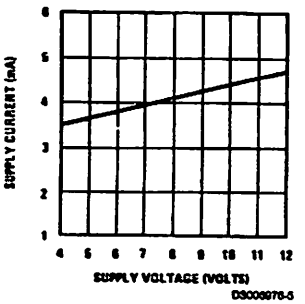
INPUT BIASING

The schematic shows that both inputs are biased to ground with a 50 kΩ resistor. The base current of the input transistors is about 250 nA, so the inputs are at about 12.5 mV when left open. If the dc source resistance driving the LM386 is higher than 250 kΩ it will contribute very little additional offset (about 2.5 mV at the input, 50 mV at the output). If the dc source resistance is less than 10 kΩ, then shorting the unused input to ground will keep the offset low (about 2.5 mV at the input, 50 mV at the output). For dc source resistances between these values we can eliminate excess offset by putting a resistor from the unused input to ground, equal in value to the dc source resistance. Of course all offset problems are eliminated if the input is capacitively coupled.

When using the LM386 with higher gains (bypassing the 1.35 kΩ resistor between pins 1 and 8) it is necessary to bypass the unused input, preventing degradation of gain and possible instabilities. This is done with a 0.1 µF capacitor or a short to ground depending on the dc source resistance on the driven input.

Typical Performance Characteristics

Quiescent Supply Current vs Supply Voltage



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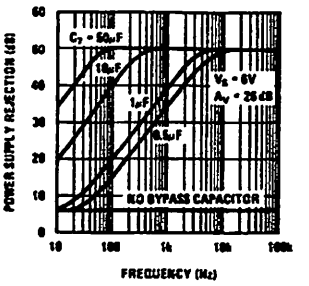
Power Supply Rejection Ratio (Referred to the Output) vs Frequency



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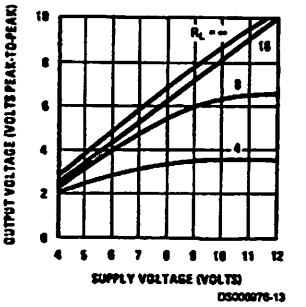
Peak-to-Peak Output Voltage Swing vs Supply Voltage



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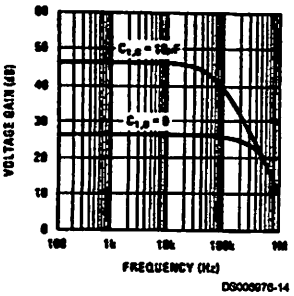
Voltage Gain vs Frequency



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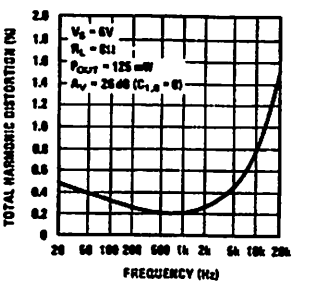
Distortion vs Frequency



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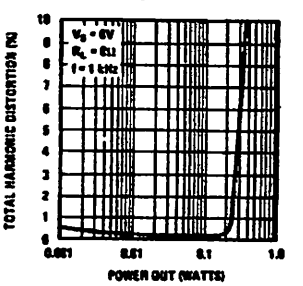
Distortion vs Output Power



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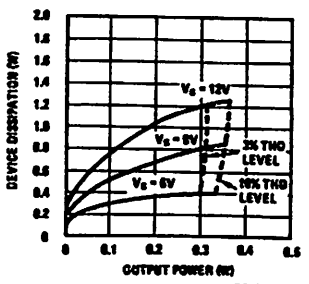
Device Dissipation vs Output Power—4Ω Load



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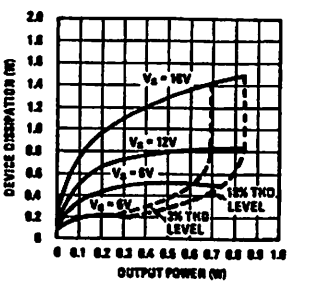
Device Dissipation vs Output Power—8Ω Load



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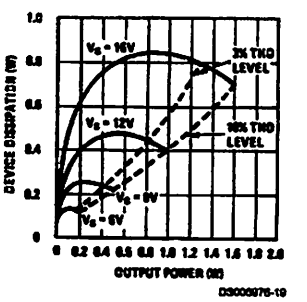
Device Dissipation vs Output Power—16Ω Load



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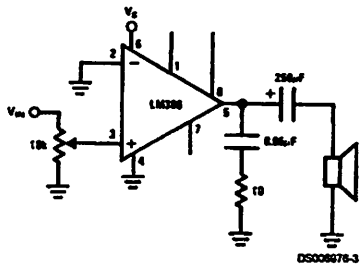
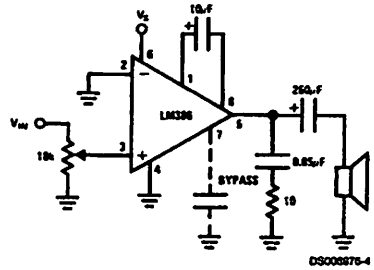
Typical Applications

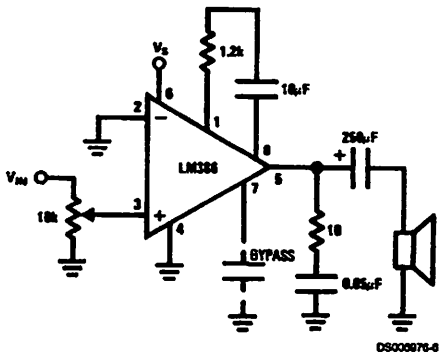
Amplifier with Gain = 20
Minimum Parts



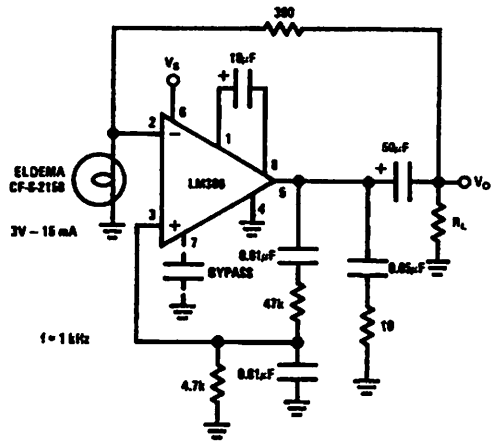
Amplifier with Gain = 200



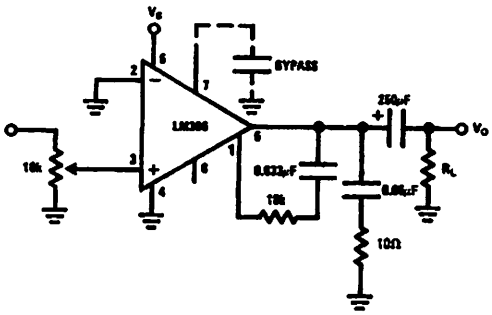
Amplifier with Gain = 50



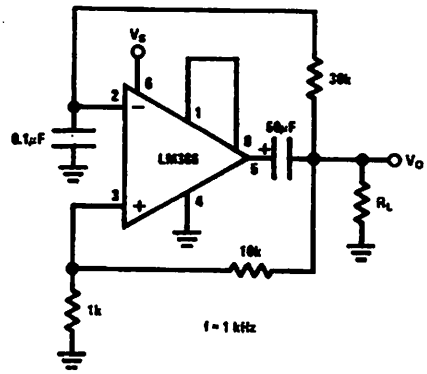
Low Distortion Power Wienbridge Oscillator



Amplifier with Bass Boost

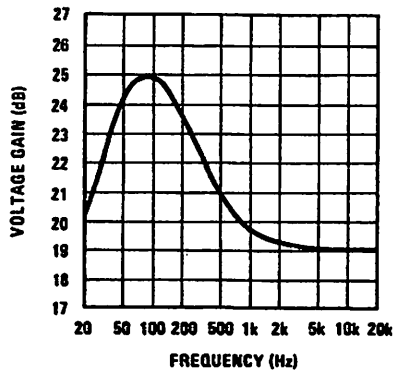


Square Wave Oscillator



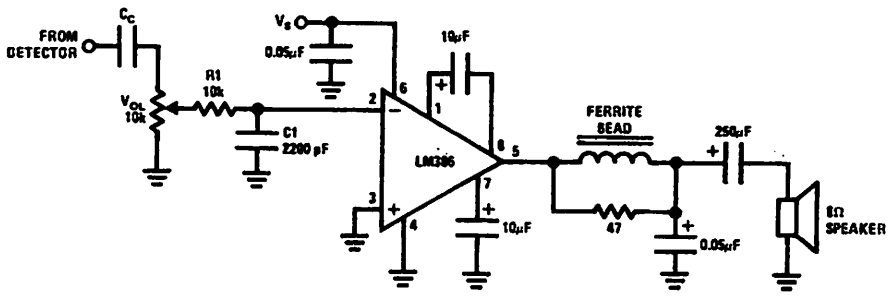
Typical Applications (Continued)

Frequency Response with Bass Boost



DS006976-10

AM Radio Power Amplifier



DS006976-11

Note 4: Twist Supply lead and supply ground very tightly.

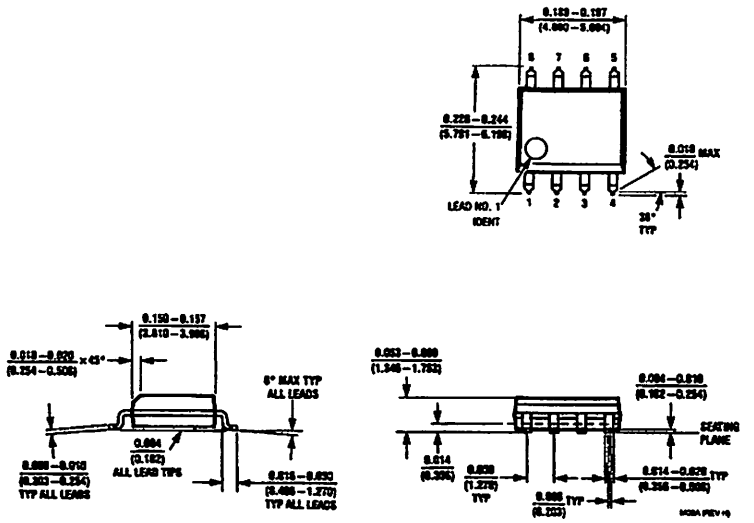
Note 5: Twist speaker lead and ground very tightly.

Note 6: Ferrite bead in Ferroxcube K5-001-001/3B with 3 turns of wire.

Note 7: R1C1 band limits input signals.

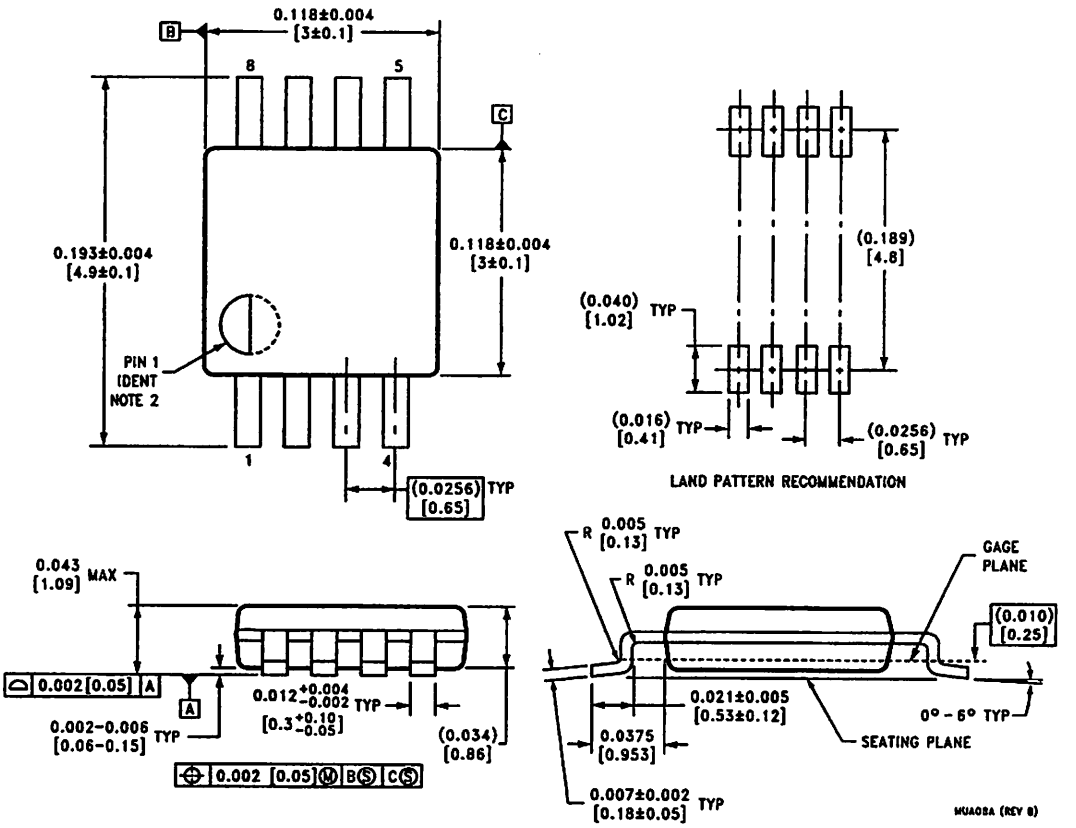
Note 8: All components must be spaced very closely to IC.

Physical Dimensions inches (millimeters) unless otherwise noted



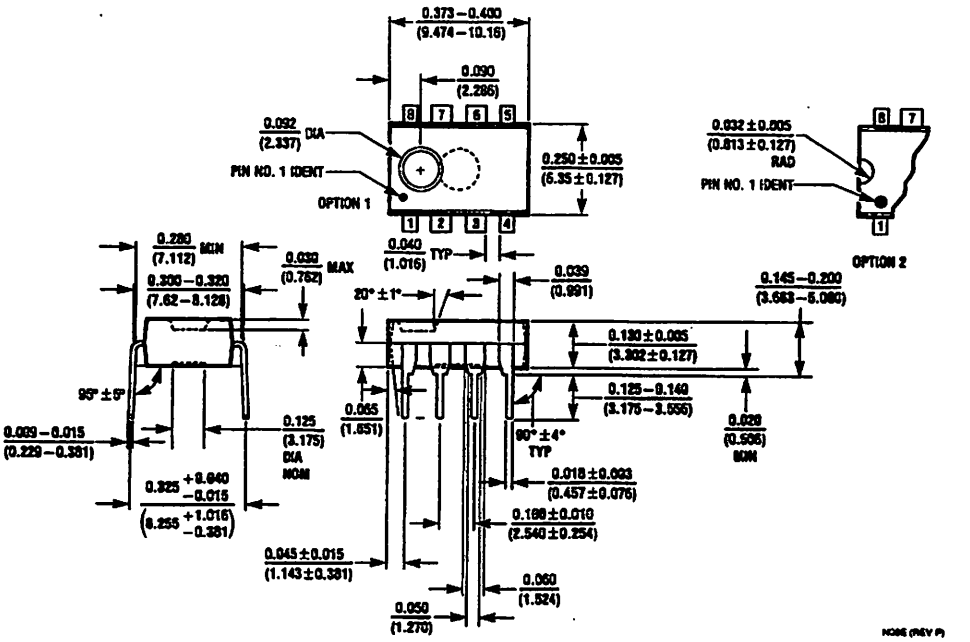
SO Package (M)
Order Number LM386M-1
NS Package Number M08A

Physical Dimensions inches (millimeters) unless otherwise noted (Continued)



8-Lead (0.118" Wide) Molded Mini Small Outline Package
Order Number LM386MM-1
NS Package Number MUA08A

Physical Dimensions inches (millimeters) unless otherwise noted (Continued)



Dual-In-Line Package (N)
Order Number LM386N-1, LM386N-3 or LM386N-4
NS Package Number N08E

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2. A critical component is any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

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Winbond Electronics Corp.

ISD2560/75/90/120

SINGLE-CHIP, MULTIPLE-MESSAGES, VOICE RECORD/PLAYBACK DEVICE 60-, 75-, 90-, AND 120-SECOND DURATION

Publication Release Date: May 2003
Revision 1.0

Winbond Electronics Corp.

1. GENERAL DESCRIPTION

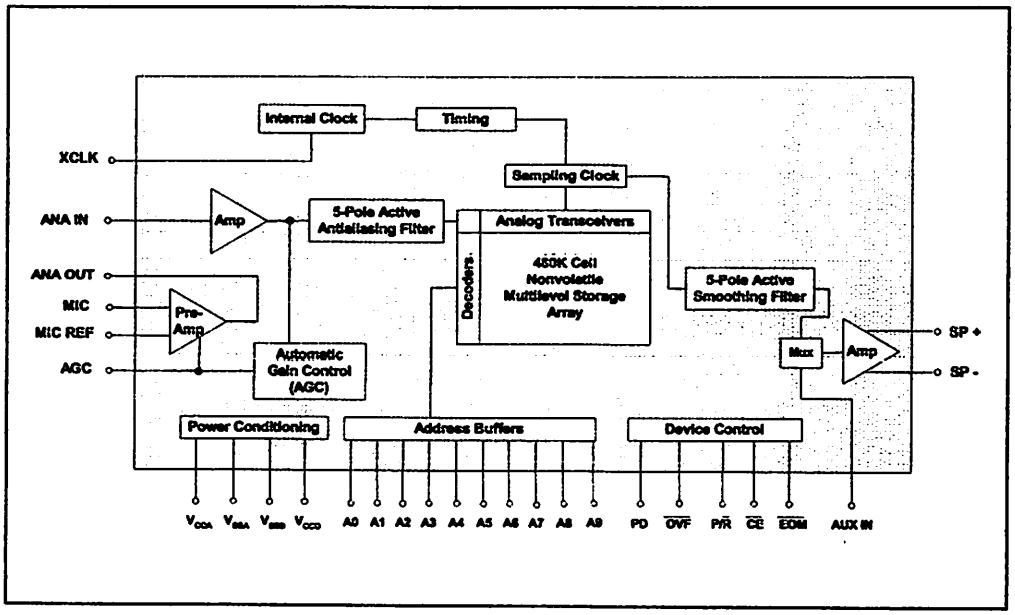
Winbond's ISD2500 ChipCorder® Series provide high-quality, single-chip, Record/Playback solutions for 60- to 120-second messaging applications. The CMOS devices include an on-chip oscillator, microphone preamplifier, automatic gain control, antialiasing filter, smoothing filter, speaker amplifier, and high density multi-level storage array. In addition, the ISD2500 is microcontroller compatible, allowing complex messaging and addressing to be achieved. Recordings are stored into on-chip nonvolatile memory cells, providing zero-power message storage. This unique, single-chip solution is made possible through Winbond's patented multilevel storage technology. Voice and audio signals are stored directly into memory in their natural form, providing high-quality, solid-state voice reproduction.

2. FEATURES

- Easy-to-use single-chip, voice record/playback solution
- High-quality, natural voice/audio reproduction
- Single-chip with duration of 60, 75, 90, or 120 seconds.
- Manual switch or microcontroller compatible
- Playback can be edge- or level-activated
- Directly cascadable for longer durations
- Automatic power-down (push-button mode)
  - Standby current 1 µA (typical)
- Zero-power message storage
  - Eliminates battery backup circuits
- Fully addressable to handle multiple messages
- 100-year message retention (typical)
- 100,000 record cycles (typical)
- On-chip clock source
- Programmer support for play-only applications
- Single +5 volt power supply
- Available in die form, PDIP, SOIC and TSOP packaging
- Temperature = die (0°C to +50°C) and package (0°C to +70°C)

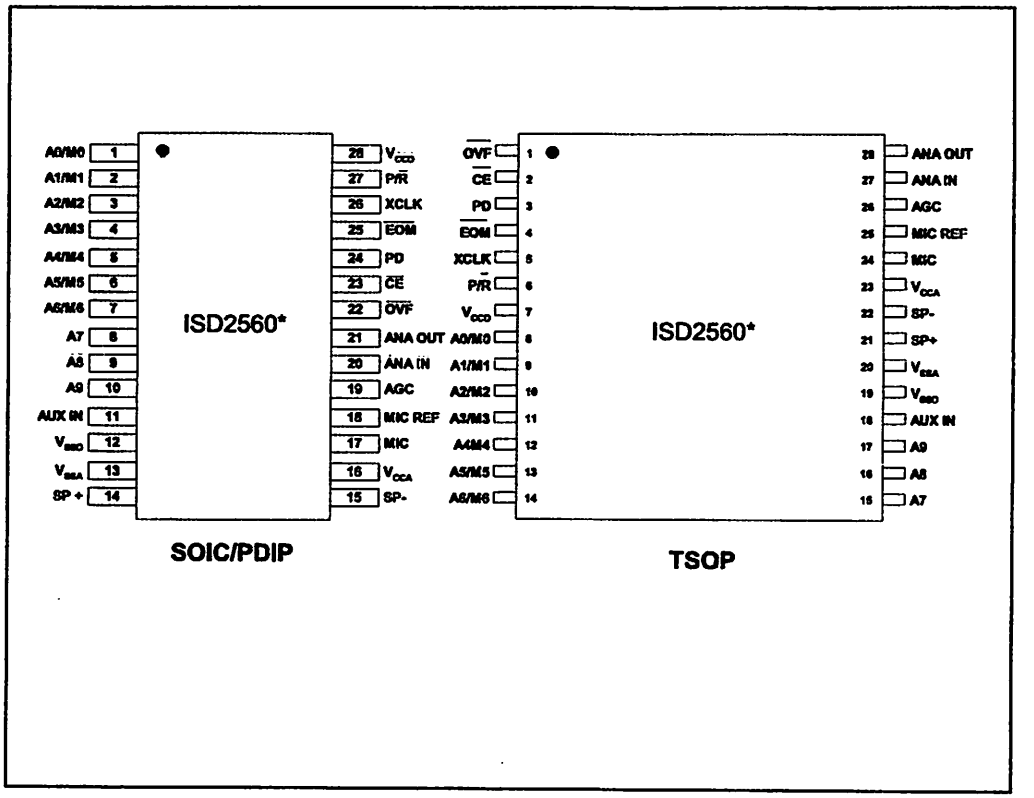
Winbond Electronics Corp.

3. BLOCK DIAGRAM



4. TABLE OF CONTENTS

5. PIN CONFIGURATION



* Same pinouts for ISD2575 / 2590 / 25120 products

6. PIN DESCRIPTION

PIN NAME	PIN NO.		FUNCTION
	SOIC/ PDIP	TSOP	
Ax/Mx	1-10/ 1-7	8-17/ 8-14	**Address/Mode Inputs:** The Address/Mode Inputs have two functions depending on the level of the two Most Significant Bits (MSB) of the address pins (A8 and A9). If either or both of the two MSBs are LOW, the inputs are all interpreted as address bits and are used as the start address for the current record or playback cycle. The address pins are inputs only and do not output any internal address information during the operation. Address inputs are latched by the falling edge of $\overline{CE}$. If both MSBs are HIGH, the Address/Mode inputs are interpreted as Mode bits according to the Operational Mode table on page 12. There are six operational modes (M0...M6) available as indicated in the table. It is possible to use multiple operational modes simultaneously. Operational Modes are sampled on each falling edge of $\overline{CE}$, and thus Operational Modes and direct addressing are mutually exclusive.
AUX IN	11	18	**Auxiliary Input:** The Auxiliary Input is multiplexed through to the output amplifier and speaker output pins when $\overline{CE}$ is HIGH, P/$\overline{R}$ is HIGH, and playback is currently not active or if the device is in playback overflow. When cascading multiple ISD2500 devices, the AUX IN pin is used to connect a playback signal from a following device to the previous output speaker drivers. For noise considerations, it is suggested that the auxiliary input not be driven when the storage array is active.
V_{SSA}, V_{SSD}	13, 12	20, 19	**Ground:** The ISD2500 series of devices utilizes separate analog and digital ground busses. These pins should be connected separately through a low-impedance path to power supply ground.
SP+/SP-	14/15	21/22	**Speaker Outputs:** All devices in the ISD2500 series include an on-chip differential speaker driver, capable of driving 50 mW into 16 Ω from AUX IN (12.2mW from memory). [1] The speaker outputs are held at V_{SSA} levels during record and power down. It is therefore not possible to parallel speaker outputs of multiple ISD2500 devices or the outputs of other speaker drivers. [2] A single-end output may be used (including a coupling capacitor between the SP pin and the speaker). These outputs may be used individually with the output signal taken from either pin. However, the use of single-end output results in a 1 to 4 reduction in its output power.

[1] Connection of speaker outputs in parallel may cause damage to the device.
[2] Never ground or drive an unused speaker output.

PIN NAME	PIN NO. SOIC/ PDIP	PIN NO. TSOP	FUNCTION
V_{CCA}, V_{CCD}	16, 28	23, 7	**Supply Voltage:** To minimize noise, the analog and digital circuits in the ISD2500 series devices use separate power busses. These voltage busses are brought out to separate pins and should be tied together as close to the supply as possible. In addition, these supplies should be decoupled as close to the package as possible.
MIC	17	24	**Microphone:** The microphone pin transfers input signal to the on-chip preamplifier. A built-in Automatic Gain Control (AGC) circuit controls the gain of this preamplifier from –15 to 24dB. An external microphone should be AC coupled to this pin via a series capacitor. The capacitor value, together with the internal 10 KΩ resistance on this pin, determines the low-frequency cutoff for the ISD2500 series passband. See Winbond's Application Information for additional information on low-frequency cutoff calculation.
MIC REF	18	25	**Microphone Reference:** The MIC REF input is the inverting input to the microphone preamplifier. This provides a noise-canceling or common-mode rejection input to the device when connected to a differential microphone.
AGC	19	26	**Automatic Gain Control:** The AGC dynamically adjusts the gain of the preamplifier to compensate for the wide range of microphone input levels. The AGC allows the full range of whispers to loud sounds to be recorded with minimal distortion. The "attack" time is determined by the time constant of a 5 KΩ internal resistance and an external capacitor (C2 on the schematic of Figure 5 in section 11) connected from the AGC pin to V_{SSA} analog ground. The "release" time is determined by the time constant of an external resistor (R2) and an external capacitor (C2) connected in parallel between the AGC pin and V_{SSA} analog ground. Nominal values of 470 KΩ and 4.7 µF give satisfactory results in most cases.
ANA IN	20	27	**Analog Input:** The analog input transfers analog signal to the chip for recording. For microphone inputs, the ANA OUT pin should be connected via an external capacitor to the ANA IN pin. This capacitor value, together with the 3.0 KΩ input impedance of ANA IN, is selected to give additional cutoff at the low-frequency end of the voice passband. If the desired input is derived from a source other than a microphone, the signal can be fed, capacitively coupled, into the ANA IN pin directly.
ANA OUT	21	28	**Analog Output:** This pin provides the preamplifier output to the user. The voltage gain of the preamplifier is determined by the voltage level at the AGC pin.

PIN NAME	PIN NO.		FUNCTION
	SOIC/ PDIP	TSOP	
$\overline{OVF}$	22	1	**Overflow:** This signal pulses LOW at the end of memory array, indicating the device has been filled and the message has overflowed. The $\overline{OVF}$ output then follows the $\overline{CE}$ input until a PD pulse has reset the device. This pin can be used to cascade several ISD2500 devices together to increase record/playback durations.
$\overline{CE}$	23	2	**Chip Enable:** The $\overline{CE}$ input pin is taken LOW to enable all playback and record operations. The address pins and playback/record pin (P/$\overline{R}$) are latched by the falling edge of $\overline{CE}$. $\overline{CE}$ has additional functionality in the M6 (Push-Button) Operational Mode as described in the Operational Mode section.
PD	24	3	**Power Down:** When neither record nor playback operation, the PD pin should be pulled HIGH to place the part in standby mode (see I_{SB} specification). When overflow ($\overline{OVF}$) pulses LOW for an overflow condition, PD should be brought HIGH to reset the address pointer back to the beginning of the memory array. The PD pin has additional functionality in the M6 (Push-Button) Operation Mode as described in the Operational Mode section.
$\overline{EOM}$	25	4	**End-Of-Message:** A nonvolatile marker is automatically inserted at the end of each recorded message. It remains there until the message is recorded over. The $\overline{EOM}$ output pulses LOW for a period of T_{EOM} at the end of each message. In addition, the ISD2500 series has an internal V_{CC} detect circuit to maintain message integrity should V_{CC} fall below 3.5V. In this case, $\overline{EOM}$ goes LOW and the device is fixed in Playback-only mode. When the device is configured in Operational Mode M6 (Push-Button Mode), this pin provides an active-HIGH signal, indicating the device is currently recording or playing. This signal can conveniently drive an LED for visual indicator of a record or playback operation in process.

<table>
<tr><th rowspan="2">PIN NAME</th><th colspan="2">PIN NO.</th><th rowspan="2">FUNCTION</th></tr>
<tr><th>SOIC/ PDIP</th><th>TSOP</th></tr>
<tr><td>XCLK</td><td>26</td><td>5</td><td>External Clock: The external clock input has an internal pull-down device. The device is configured at the factory with an internal sampling clock frequency centered to ±1 percent of specification. The frequency is then maintained to a variation of ±2.25 percent over the entire commercial temperature and operating voltage ranges. If greater precision is required, the device can be clocked through the XCLK pin as follows:
<table>
<tr><th>Part Number</th><th>Sample Rate</th><th>Required Clock</th></tr>
<tr><td>ISD2560</td><td>8.0 kHz</td><td>1024 kHz</td></tr>
<tr><td>ISD2575</td><td>6.4 kHz</td><td>819.2 kHz</td></tr>
<tr><td>ISD2590</td><td>5.3 kHz</td><td>682.7 kHz</td></tr>
<tr><td>ISD25120</td><td>4.0 kHz</td><td>512 kHz</td></tr>
</table>
These recommended clock rates should not be varied because the antialiasing and smoothing filters are fixed, and aliasing problems can occur if the sample rate differs from the one recommended. The duty cycle on the input clock is not critical, as the clock is immediately divided by two. If the XCLK is not used, this input must be connected to ground.</td></tr>
<tr><td>P/$\overline{R}$</td><td>27</td><td>6</td><td>Playback/Record: The P/$\overline{R}$ input pin is latched by the falling edge of the $\overline{CE}$ pin. A HIGH level selects a playback cycle while a LOW level selects a record cycle. For a record cycle, the address pins provide the starting address and recording continues until PD or $\overline{CE}$ is pulled HIGH or an overflow is detected (i.e. the chip is full). When a record cycle is terminated by pulling PD or $\overline{CE}$ HIGH, then End-Of-Message ($\overline{EOM}$) marker is stored at the current address in memory. For a playback cycle, the address inputs provide the starting address and the device will play until an $\overline{EOM}$ marker is encountered. The device can continue to pass an $\overline{EOM}$ marker if $\overline{CE}$ is held LOW in address mode, or in an Operational Mode. (See Operational Modes section)</td></tr>
</table>

7. FUNCTIONAL DESCRIPTION

7.1. DETAILED DESCRIPTION

Speech/Sound Quality

The Winbond's ISD2500 series includes devices offered at 4.0, 5.3, 6.4, and 8.0 kHz sampling frequencies, allowing the user a choice of speech quality options. Increasing the duration within a product series decreases the sampling frequency and bandwidth, which affects the sound quality. Please refer to the ISD2560/75/90/120 Product Summary table below to compare the duration, sampling frequency and filter pass band.

The speech samples are stored directly into the on-chip nonvolatile memory without any digitization and compression associated like other solutions. Direct analog storage provides a very true, natural sounding reproduction of voice, music, tones, and sound effects not available with most solid state digital solutions.

Duration

To meet various system requirements, the ISD2560/75/90/120 products offer single-chip solutions at 60, 75, 90, and 120 seconds. Parts may also be cascaded together for longer durations.

TABLE 1: ISD2560/75/90/120 PRODUCT SUMMARY

Part Number	Duration (Seconds)	Input Sample Rate (kHz)	Typical Filter Pass Band * (kHz)
ISD2560	60	8.0	3.4
ISD2575	75	6.4	2.7
ISD2590	90	5.3	2.3
ISD25120	120	4.0	1.7

* 3db roll-off point

EEPROM Storage

One of the benefits of Winbond's ChipCorder® technology is the use of on-chip nonvolatile memory, providing zero-power message storage. The message is retained for up to 100 years typically without power. In addition, the device can be re-recorded typically over 100,000 times.

Microcontroller Interface

In addition to its simplicity and ease of use, the ISD2500 series includes all the interfaces necessary for microcontroller-driven applications. The address and control lines can be interfaced to a microcontroller and manipulated to perform a variety of tasks, including message assembly, message concatenation, predefined fixed message segmentation, and message management.

Programming

The ISD2500 series is also ideal for playback-only applications, where single or multiple messages are referenced through buttons, switches, or a microcontroller. Once the desired message configuration is created, duplicates can easily be generated via a gang programmer.

7.2. OPERATIONAL MODES

The ISD2500 series is designed with several built-in Operational Modes that provide maximum functionality with minimum external components. These modes are described in details as below. The Operational Modes are accessed via the address pins and mapped beyond the normal message address range. When the two Most Significant Bits (MSB), A8 and A9, are HIGH, the remaining address signals are interpreted as mode bits and not as address bits. Therefore, Operational Modes and direct addressing are not compatible and cannot be used simultaneously.

There are two important considerations for using Operational Modes. First, all operations begin initially at address 0 of its memory. Later operations can begin at other address locations, depending on the Operational Mode(s) chosen. In addition, the address pointer is reset to 0 when the device is changed from record to playback, playback to record (except M6 mode), or when a Power-Down cycle is executed.

Second, Operational Modes are executed when $\overline{CE}$ goes LOW. This Operational Mode remains in effect until the next LOW-going $\overline{CE}$ signal, at which point the current mode(s) are sampled and executed.

TABLE 2: OPERATIONAL MODES

Mode [1]	Function	Typical Use	Jointly Compatible [2]
M0	Message cueing	Fast-forward through messages	M4, M5, M6
M1	Delete $\overline{EOM}$ markers	Position $\overline{EOM}$ marker at the end of the last message	M3, M4, M5, M6
M2	Not applicable	Reserved	N/A
M3	Looping	Continuous playback from Address 0	M1, M5, M6
M4	Consecutive addressing	Record/playback multiple consecutive messages	M0, M1, M5
M5	$\overline{CE}$ level-activated	Allows message pausing	M0, M1, M3, M4
M6	Push-button control	Simplified device interface	M0, M1, M3

[1] Besides mode pin needed to be "1", A8 and A9 pin are also required to be "1" in order to enter into the related operational mode.

[2] Indicates additional Operational Modes which can be used simultaneously with the given mode.

7.2.1. Operational Modes Description

The Operational Modes can be used in conjunction with a microcontroller, or they can be hardwired to provide the desired system operation.

M0 – Message Cueing

Message Cueing allows the user to skip through messages, without knowing the actual physical addresses of each message. Each $\overline{CE}$ LOW pulse causes the internal address pointer to skip to the next message. This mode is used for playback only, and is typically used with the M4 Operational Mode.

M1 – Delete $\overline{EOM}$ Markers

The M1 Operational Mode allows sequentially recorded messages to be combined into a single message with only one $\overline{EOM}$ marker set at the end of the final message. When this Operational Mode is configured, messages recorded sequentially are played back as one continuous message.

M2 – Unused

When Operational Modes are selected, the M2 pin should be LOW.

M3 – Message Looping

The M3 Operational Mode allows for the automatic, continuously repeated playback of the message located at the beginning of the address space. A message can completely fill the ISD2500 device and will loop from beginning to end without $\overline{OVF}$ going LOW.

M4 – Consecutive Addressing

During normal operation, the address pointer will reset when a message is played through an $\overline{EOM}$ marker. The M4 Operational Mode inhibits the address pointer reset on $\overline{EOM}$, allowing messages to be played back consecutively.

M5 - $\overline{CE}$-Level Activated

The default mode for ISD2500 devices is for $\overline{CE}$ to be edge-activated on playback and level-activated on record. The M5 Operational Mode causes the $\overline{CE}$ pin to be interpreted as level-activated as opposed to edge-activated during playback. This is especially useful for terminating playback operations using the $\overline{CE}$ signal. In this mode, $\overline{CE}$ LOW begins a playback cycle, at the beginning of the device memory. The playback cycle continues as long as $\overline{CE}$ is held LOW. When $\overline{CE}$ goes HIGH, playback will immediately end. A new $\overline{CE}$ LOW will restart the message from the beginning unless M4 is also HIGH.

M6 – Push-Button Mode

The ISD2500 series contain a Push-Button Operational Mode. The Push-Button Mode is used primarily in very low-cost applications and is designed to minimize external circuitry and components, thereby reducing system cost. In order to configure the device in Push-Button Operational Mode, the two most significant address bits must be HIGH, and the M6 mode pin must also be HIGH. A device in this mode always powers down at the end of each playback or record cycle after $\overline{CE}$ goes HIGH.

When this operational mode is implemented, three of the pins on the device have alternate functionality as described in the table below.

TABLE 3: ALTERNATE FUNCTIONALITY IN PINS

Pin Name	Alternate Functionality in Push-Button Mode
$\overline{CE}$	Start/Pause Push-Button (LOW pulse-activated)
PD	Stop/Reset Push-Button (HIGH pulse-activated)
$\overline{EOM}$	Active-HIGH Run Indicator

$\overline{CE}$ (START/PAUSE)

In Push-Button Operational Mode, $\overline{CE}$ acts as a LOW-going pulse-activated START/PAUSE signal. If no operation is currently in progress, a LOW-going pulse on this signal will initiate a playback or record cycle according to the level on the P/$\overline{R}$ pin. A subsequent pulse on the $\overline{CE}$ pin, before an $\overline{EOM}$ is reached in playback or an overflow condition occurs, will pause the current operation, and the address counter is not reset. Another $\overline{CE}$ pulse will cause the device to continue the operation from the place where it is paused.

PD (STOP/RESET)

In Push-Button Operational Mode, PD acts as a HIGH-going pulse-activated STOP/RESET signal. When a playback or record cycle is in progress and a HIGH-going pulse is observed on PD, the current cycle is terminated and the address pointer is reset to address 0, the beginning of the message space.

$\overline{EOM}$ (RUN)

In Push-Button Operational Mode, $\overline{EOM}$ becomes an active-HIGH RUN signal which can be used to drive an LED or other external device. It is HIGH whenever a record or playback operation is in progress.

Recording in Push-Button Mode

1. The PD pin should be LOW, usually using a pull-down resistor.

2. The P/$\overline{R}$ pin is taken LOW.
3. The $\overline{CE}$ pin is pulsed LOW. Recording starts, $\overline{EOM}$ goes HIGH to indicate an operation in progress.
4. When the $\overline{CE}$ pin is pulsed LOW. Recording pauses, $\overline{EOM}$ goes back LOW. The internal address pointers are not cleared, but the $\overline{EOM}$ marker is stored in memory to indicate as the message end. The P/$\overline{R}$ pin may be taken HIGH at this time. Any subsequent $\overline{CE}$ would start a playback at address 0.
5. The $\overline{CE}$ pin is pulsed LOW. Recording starts at the next address after the previous set $\overline{EOM}$ marker. $\overline{EOM}$ goes back HIGH.[3]
6. When the recording sequences are finished, the final $\overline{CE}$ pulse LOW will end the last record cycle, leaving a set $\overline{EOM}$ marker at the message end. Recording may also be terminated by a HIGH level on PD, which will leave a set $\overline{EOM}$ marker.

Playback in Push-Button Mode

1. The PD pin should be LOW.
2. The P/$\overline{R}$ pin is taken HIGH.
3. The $\overline{CE}$ pin is pulsed LOW. Playback starts, $\overline{EOM}$ goes HIGH to indicate an operation in progress.
4. If the $\overline{CE}$ pin is pulsed LOW or an $\overline{EOM}$ marker is encountered during an operation, the part will pause. The internal address pointers are not cleared, and $\overline{EOM}$ goes back LOW. The P/$\overline{R}$ pin may be changed at this time. A subsequent record operation would not reset the address pointers and the recording would begin where playback ended.
5. $\overline{CE}$ is again pulsed LOW. Playback starts where it left off, with $\overline{EOM}$ going HIGH to indicate an operation in progress.
6. Playback continues as in steps 4 and 5 until PD is pulsed HIGH or overflow occurs.
7. If in overflow, pulling $\overline{CE}$ LOW will reset the address pointer and start playback from the beginning. After a PD pulse, the part is reset to address 0.

Note: Push-Button Mode can be used in conjunction with modes M0, M1, and M3.

[3] If the M1 Operational Mode pin is also HIGH, the just previously written $\overline{EOM}$ bit is erased, and recording starts at that address.

Good Audio Design Practices

Winbond products are very high-quality single-chip voice recording and playback systems. To ensure the highest quality voice reproduction, it is important that good audio design practices on layout and power supply decoupling be followed. See Application Information or below links for details.

Good Audio Design Practices

http://www.winbond-usa.com/products/isd_products/chipcorder/applicationinfo/apin11.pdf

Single-Chip Board Layout Diagrams

http://www.winbond-usa.com/products/isd_products/chipcorder/applicationinfo/apin12.pdf

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8. TIMING DIAGRAMS

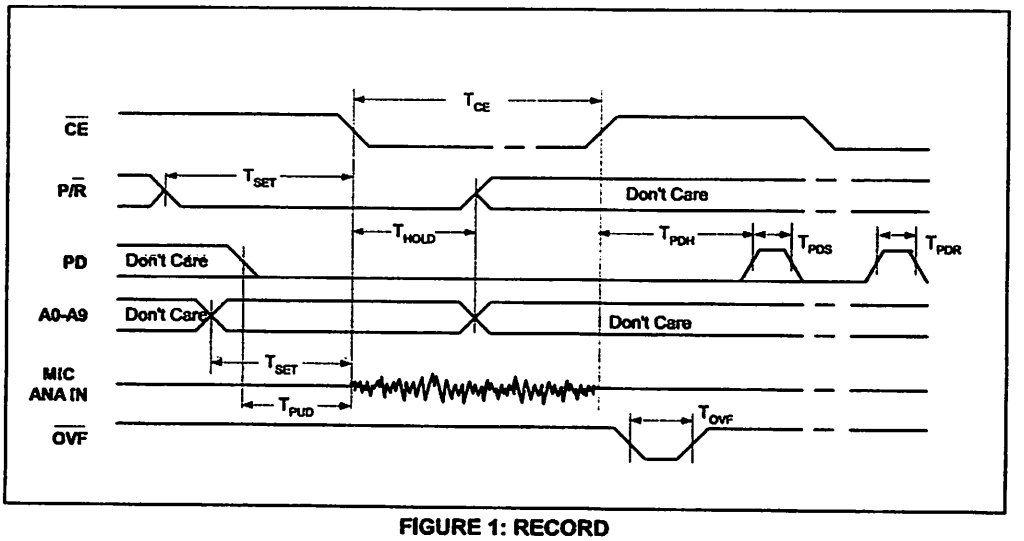


FIGURE 1: RECORD

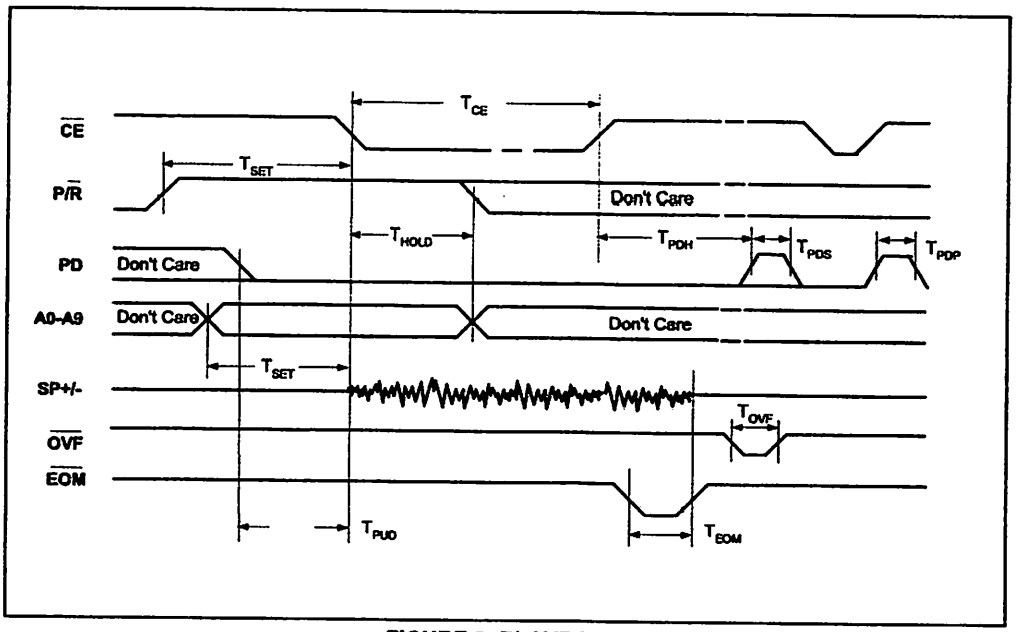


FIGURE 2: PLAYBACK

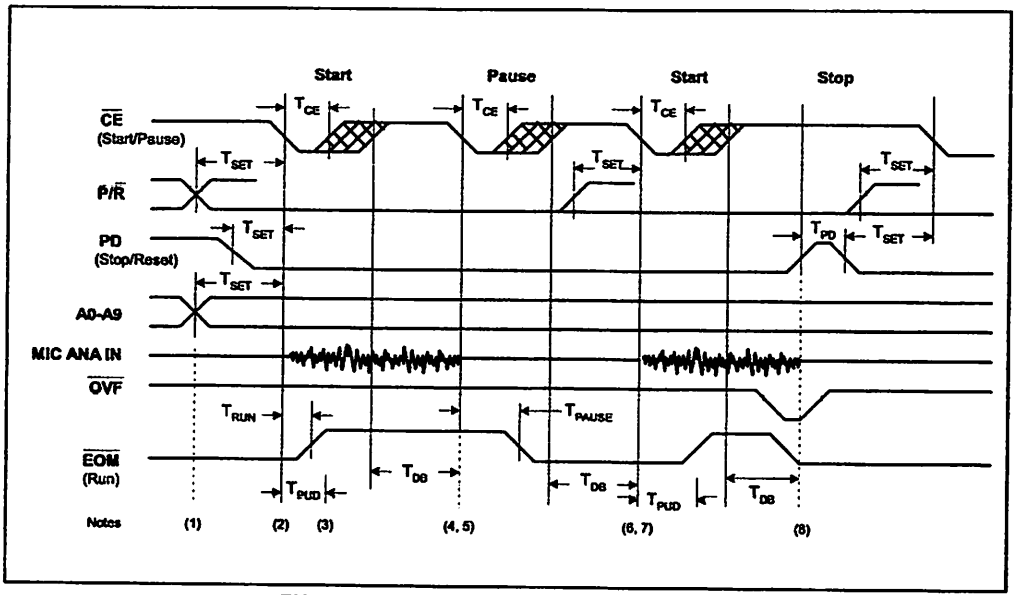


FIGURE 3: PUSH-BUTTON MODE RECORD

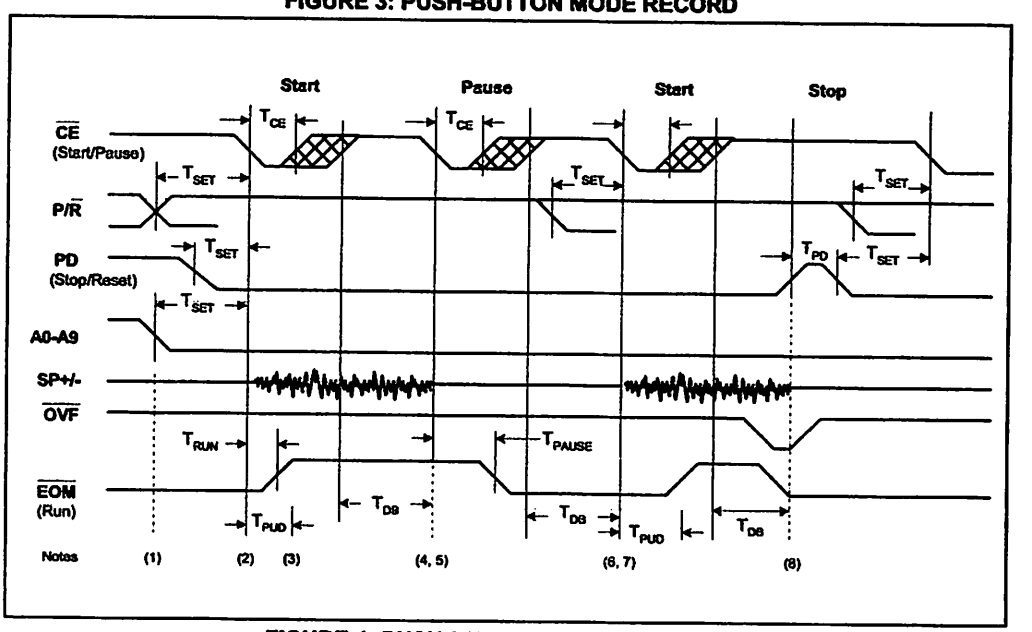


FIGURE 4: PUSH-BUTTON MODE PLAYBACK

Notes for Push-Button modes:

1. A9, A8, and A6 = 1 for push-button operation.
2. The first $\overline{CE}$ LOW pulse performs a start function.
3. The part will begin to play or record after a power-up delay T_{PUD}.
4. The part must have $\overline{CE}$ HIGH for a debounce period T_{DB} before it will recognize another falling edge of $\overline{CE}$ and pause.
5. The second $\overline{CE}$ LOW pulse, and every even pulse thereafter, performs a Pause function.
6. Again, the part must have $\overline{CE}$ HIGH for a debounce period T_{DB} before it will recognize another falling edge of $\overline{CE}$, which would restart an operation. In addition, the part will not do an internal power down until $\overline{CE}$ is HIGH for the T_{DB} time.
7. The third $\overline{CE}$ LOW pulse, and every odd pulse thereafter, performs a Resume function.
8. At any time, a HIGH level on PD will stop the current function, reset the address counter, and power down the device.

9. ABSOLUTE MAXIMUM RATINGS

TABLE 4: ABSOLUTE MAXIMUM RATINGS (DIE)

CONDITION	VALUE
Junction temperature	150°C
Storage temperature range	-65°C to +150°C
Voltage applied to any pad	(V_{SS} –0.3V) to (V_{CC} +0.3V)
Voltage applied to any pad (Input current limited to ±20mA)	(V_{SS} –1.0V) to (V_{CC} +1.0V)
$V_{CC} - V_{SS}$	-0.3V to +7.0V

TABLE 5: ABSOLUTE MAXIMUM RATINGS (PACKAGED PARTS)

CONDITION	VALUE
Junction temperature	150°C
Storage temperature range	-65°C to +150°C
Voltage applied to any pin	(V_{SS} –0.3V) to (V_{CC} +0.3V)
Voltage applied to any pin (Input current limited to ±20 mA)	(V_{SS} –1.0V) to (V_{CC} +1.0V)
Lead temperature (Soldering – 10sec)	300°C
$V_{CC} - V_{SS}$	-0.3V to +7.0V

Note: Stresses above those listed may cause permanent damage to the device. Exposure to the absolute maximum ratings may affect device reliability and performance. Functional operation is not implied at these conditions.

9.1 OPERATING CONDITIONS

TABLE 6: OPERATING CONDITIONS (DIE)

CONDITION	VALUE
Commercial operating temperature range	0°C to +50°C
Supply voltage (V_{CC}) [1]	+4.5V to +6.5V
Ground voltage (V_{SS}) [2]	0V

TABLE 7: OPERATING CONDITIONS (PACKAGED PARTS)

CONDITION	VALUE
Commercial operating temperature range [3]	0°C to +70°C
Supply voltage (V_{CC}) [1]	+4.5V to +5.5V
Ground voltage (V_{SS}) [2]	0V

[1] $V_{CC} = V_{CCA} = V_{CCD}$

[2] $V_{SS} = V_{SSA} = V_{SSD}$

[3] Case Temperature

10. ELECTRICAL CHARACTERISTICS

10.1. PARAMETERS FOR PACKAGED PARTS

TABLE 8: DC PARAMETERS – Packaged Parts

PARAMETER	SYMBOL	MIN[2]	TYP[1]	MAX[2]	UNITS	CONDITIONS
Input Low Voltage	V_{IL}			0.8	V	
Input High Voltage	V_{IH}	2.0			V	
Output Low Voltage	V_{OL}			0.4	V	I_{OL} = 4.0 mA
Output High Voltage	V_{OH}	V_{CC} - 0.4			V	I_{OH} = -10 µA
$\overline{OVF}$ Output High Voltage	V_{OH1}	2.4			V	I_{OH} = -1.6 mA
$\overline{EOM}$ Output High Voltage	V_{OH2}	V_{CC} – 1.0	V_{CC} - 0.8		V	I_{OH} = -3.2 mA
V_{CC} Current (Operating)	I_{CC}		25	30	mA	R_{EXT} = ∞ [3]
V_{CC} Current (Standby)	I_{SB}		1	10	µA	[3]
Input Leakage Current	I_{IL}			±1	µA	
Input Current HIGH w/Pull Down	I_{ILPD}			130	µA	Force V_{CC} [4]
Output Load Impedance	R_{EXT}	16			Ω	Speaker Load
Preamp Input Resistance	R_{MIC}	4	9	15	KΩ	MIC and MIC REF Pins
AUX IN Input Resistance	R_{AUX}	5	11	20	KΩ	
ANA IN Input Resistance	$R_{ANA\ IN}$	2.3	3	5	KΩ	
Preamp Gain 1	A_{PRE1}	21	24	26	dB	AGC = 0.0V
Preamp Gain 2	A_{PRE2}		-15	5	dB	AGC = 2.5V
AUX IN/SP+ Gain	A_{AUX}		0.98	1.0	V/V	
ANA IN to SP+/- Gain	A_{ARP}	21	23	26	dB	
AGC Output Resistance	R_{AGC}	2.5	5	9.5	KΩ	

Notes:

[1] Typical values @ T_A = 25° and V_{CC} = 5.0V.

[2] All Min/Max limits are guaranteed by Winbond via electrical testing or characterization. Not all specifications are 100 percent tested.

[3] V_{CCA} and V_{CCD} connected together.

[4] XCLK pin only.

TABLE 9: AC PARAMETERS – Packaged Parts

CHARACTERISTIC	SYMBOL	MIN[2]	TYP[1]	MAX[2]	UNITS	CONDITIONS
Sampling Frequency	F_S					
ISD2560			8.0		kHz	[7]
ISD2575			6.4		kHz	[7]
ISD2590			5.3		kHz	[7]
ISD25120			4.0		kHz	[7]
Filter Pass Band	F_{CF}					
ISD2560			3.4		kHz	3 dB Roll-Off Point[3][8]
ISD2575			2.7		kHz	3 dB Roll-Off Point[3][8]
ISD2590			2.3		kHz	3 dB Roll-Off Point[3][8]
ISD25120			1.7		kHz	3 dB Roll-Off Point[3][8]
Record Duration	T_{REC}					
ISD2560		58.1	60.0	62.0	sec	Commercial Operation[7]
ISD2575		72.6	75.0	77.5	sec	Commercial Operation[7]
ISD2590		87.1	90.0	93.0	sec	Commercial Operation[7]
ISD25120		116.1	120.0	123.9	sec	Commercial Operation[7]
Playback Duration	T_{PLAY}					
ISD2560		58.1	60.0	62.0	sec	Commercial Operation
ISD2575		72.6	75.0	77.5	sec	Commercial Operation
ISD2590		87.1	90.0	93.0	sec	Commercial Operation
ISD25120		116.1	120.0	123.9	sec	Commercial Operation
$\overline{CE}$ Pulse Width	T_{CE}		100		nsec	
Control/Address Setup Time	T_{SET}		300		nsec	
Control/Address Hold Time	T_{HOLD}		0		nsec	
Power-Up Delay	T_{PUD}					
ISD2560		24.1	25.0	27.8	msec	Commercial Operation
ISD2575		30.2	31.3	34.3	msec	Commercial Operation
ISD2590		36.2	37.5	40.8	msec	Commercial Operation
ISD25120		48.2	50.0	53.6	msec	Commercial Operation
PD Pulse Width (record)	T_{PDR}					
ISD2560			25.0		msec	
ISD2575			31.25		msec	
ISD2590			37.5		msec	
ISD25120			50.0		msec	

TABLE 9: AC PARAMETERS – Packaged Parts (Cont'd)

CHARACTERISTIC	SYMBOL	MIN[2]	TYP[1]	MAX[2]	UNITS	CONDITIONS
PD Pulse Width (Play)	T_{PDP}					
ISD2560			12.5		msec	
ISD2575			15.625		msec	
ISD2590			18.75		msec	
ISD25120			25.0		msec	
PD Pulse Width (Static)	T_{PDS}		100		nsec	[6]
Power Down Hold	T_{PDH}		0		nsec	
$\overline{EOM}$ Pulse Width	T_{EOM}					
ISD2560			12.5		msec	
ISD2575			15.625		msec	
ISD2590			18.75		msec	
ISD25120			25.0		msec	
Overflow Pulse Width	T_{OVF}		6.5		µsec	
Total Harmonic Distortion	THD		1	2	%	@ 1 kHz
Speaker Output Power	P_{OUT}		12.2	50	mW	R_{EXT} = 16 Ω[4]
Voltage Across Speaker Pins	V_{OUT}			2.5	V p-p	R_{EXT} = 600 Ω
MIC Input Voltage	V_{IN1}			20	mV	Peak-to-Peak[5]
ANA IN Input Voltage	V_{IN2}			50	mV	Peak-to-Peak
AUX Input Voltage	V_{IN3}			1.25	V	Peak-to-Peak; R_{EXT} = 16 Ω

Notes:

[1] Typical values @ T_A = 25°C and V_{CC} = 5.0V.

[2] All Min/Max limits are guaranteed by Winbond via electrical testing or characterization. Not all specifications are 100 percent tested.

[3] Low-frequency cutoff depends upon the value of external capacitors (see Pin Descriptions)

[4] From AUX IN; if ANA IN is driven at 50 mV p-p, the P_{OUT} = 12.2 mW, typical.

[5] With 5.1 K Ω series resistor at ANA IN.

[6] T_{PDS} is required during a static condition, typically overflow.

[7] Sampling Frequency and playback Duration can vary as much as ±2.25 percent over the commercial temperature range. For greater stability, an external clock can be utilized (see Pin Descriptions)

[8] Filter specification applies to the antialiasing filter and the smoothing filter. Therefore, from input to output, expect a 6 dB drop by nature of passing through both filters.

10.1.1. Typical Parameter Variation with Voltage and Temperature (Packaged Parts)

Chart 1: Record Mode Operating Current (I_{CC})

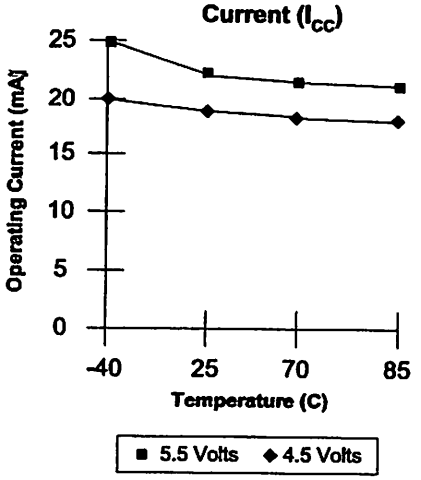


Chart 3: Standby Current (I_{SB})

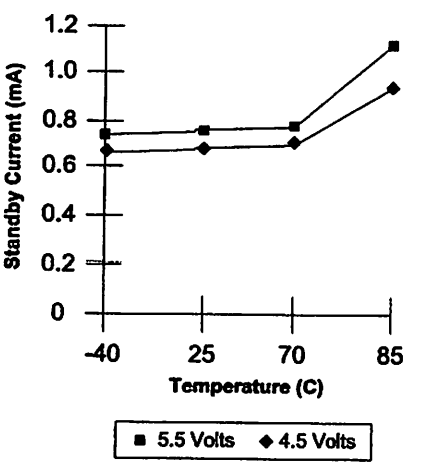


Chart 2: Total Harmonic Distortion

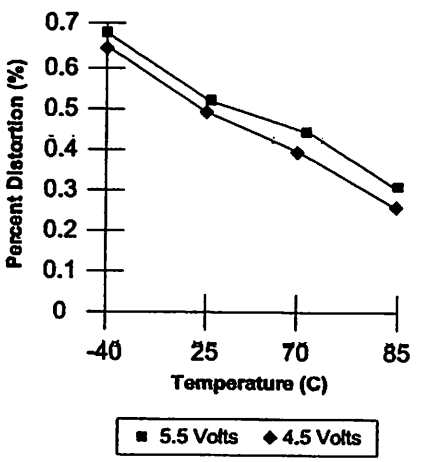
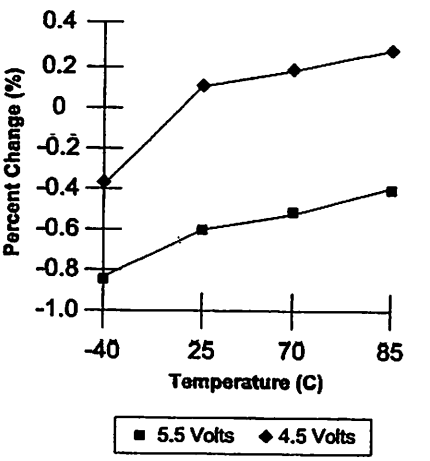


Chart 4: Oscillator Stability



10.2. PARAMETERS FOR DIE

TABLE 10: DC PARAMETERS – Die

PARAMETER	SYMBOL	MIN[2]	TYP[1]	MAX[2]	UNITS	CONDITIONS
Input Low Voltage	V_{IL}			0.8	V	
Input High Voltage	V_{IH}	2.0			V	
Output Low Voltage	V_{OL}			0.4	V	I_{OL} = 4.0 mA
Output High Voltage	V_{OH}	V_{CC} - 0.4			V	I_{OH} = -10 µA
$\overline{OVF}$ Output High Voltage	V_{OH1}	2.4			V	I_{OH} = -1.6 mA
$\overline{EOM}$ Output High Voltage	V_{OH2}	V_{CC} – 1.0	V_{CC} - 0.8		V	I_{OH} = -3.2 mA
V_{CC} Current (Operating)	I_{CC}		25	30	mA	R_{EXT} = ∞ [3]
V_{CC} Current (Standby)	I_{SB}		1	10	µA	[2]
Input Leakage Current	I_{IL}			±1	µA	
Input Current HIGH w/Pull Down	I_{ILPD}			130	µA	Force V_{CC} [4]
Output Load Impedance	R_{EXT}	16			Ω	Speaker Load
Preamp IN Input Resistance	R_{MIC}	4	9	15	KΩ	MIC and MIC REF Pads
AUX IN Input Resistance	R_{AUX}	5	11	20	KΩ	
ANA IN Input Resistance	$R_{ANA\ IN}$	2.3	3	5	KΩ	
Preamp Gain 1	A_{PRE1}	21	24	26	dB	AGC = 0.0V
Preamp Gain 2	A_{PRE2}		-15	5	dB	AGC = 2.5V
AUX IN/SP+ Gain	A_{AUX}		0.98	1.0	V/V	
ANA IN to SP+/- Gain	A_{ARP}	21	23	26	dB	
AGC Output Resistance	R_{AGC}	2.5	5	9.5	KΩ	

Notes:

[1] Typical values @ T_A = 25°C and V_{CC} = 5.0V.

[2] All Min/Max limits are guaranteed by Winbond via electrical testing or characterization. Not all specifications are 100 percent tested.

[3] V_{CCA} and V_{CCD} connected together.

[4] XCLK pad only.

TABLE 11: AC PARAMETERS – Die

CHARACTERISTIC	SYMBOL	MIN[2]	TYP[1]	MAX[2]	UNITS	CONDITIONS
Sampling Frequency	F_S					
ISD2560			8.0		kHz	[7]
ISD2575			6.4		kHz	[7]
ISD2590			5.3		kHz	[7]
ISD25120			4.0		kHz	[7]
Filter Pass Band	F_{CF}					
ISD2560			3.4		kHz	3 dB Roll-Off Point[3][6]
ISD2575			2.7		kHz	3 dB Roll-Off Point[3][6]
ISD2590			2.3		kHz	3 dB Roll-Off Point[3][6]
ISD25120			1.7		kHz	3 dB Roll-Off Point[3][6]
Record Duration	T_{REC}					
ISD2560		58.1	60.0	62.0	sec	Commercial Operation[7]
ISD2575		72.6	75.0	77.5	sec	Commercial Operation[7]
ISD2590		87.1	90.0	93.0	sec	Commercial Operation[7]
ISD25120		116.1	120.0	123.9	sec	Commercial Operation[7]
Playback Duration	T_{PLAY}					
ISD2560		58.1	60.0	62.0	sec	Commercial Operation[7]
ISD2575		72.6	75.0	77.5	sec	Commercial Operation[7]
ISD2590		87.1	90.0	93.0	sec	Commercial Operation[7]
ISD25120		116.1	120.0	123.9	sec	Commercial Operation[7]
$\overline{CE}$ Pulse Width	T_{CE}		100		nsec	
Control/Address Setup Time	T_{SET}		300		nsec	
Control/Address Hold Time	T_{HOLD}		0		nsec	
Power-Up Delay	T_{PUD}					
ISD2560		24.1	25.0	27.8	msec	Commercial Operation
ISD2575		30.2	31.3	34.3	msec	Commercial Operation
ISD2590		36.2	37.5	40.8	msec	Commercial Operation
ISD25120		48.2	50.0	53.6	msec	Commercial Operation
PD Pulse Width (Record)	T_{PDR}					
ISD2560			25.0		msec	
ISD2575			31.25		msec	
ISD2590			37.5		msec	
ISD25120			50.0		msec	

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TABLE 11: AC PARAMETERS – Die (Cont'd)

CHARACTERISTIC	SYMBOL	MIN[2]	TYP[1]	MAX[2]	UNITS	CONDITIONS
PD Pulse Width (Play)	T_{PDP}					
ISD2560			12.5		msec	
ISD2575			15.625		msec	
ISD2590			18.75		msec	
ISD25120			25.0		msec	
PD Pulse Width (Static)	T_{PDS}		100		nsec	[6]
Power Down Hold	T_{PDH}		0		nsec	
$\overline{EOM}$ Pulse Width	T_{EOM}					
ISD2560			12.5		msec	
ISD2575			15.625		msec	
ISD2590			18.75		msec	
ISD25120			25.0		msec	
Overflow Pulse Width	T_{OVF}		6.5		µsec	
Total Harmonic Distortion	THD		1	3	%	@ 1 kHz
Speaker Output Power	P_{OUT}		12.2	50	mW	R_{EXT} = 16 Ω[4]
Voltage Across Speaker Pins	V_{OUT}			2.5	V p-p	R_{EXT} = 600 Ω
MIC Input Voltage	V_{IN1}			20	mV	Peak-to-Peak[5]
ANA IN Input Voltage	V_{IN2}			50	mV	Peak-to-Peak
AUX Input Voltage	V_{IN3}			1.25	V	Peak-to-Peak; R_{EXT} = 16 Ω

Notes:

[1] Typical values @ T_A = 25°C and V_{CC} = 5.0V.

[2] All Min/Max limits are guaranteed by Winbond via electrical testing or characterization. Not all specifications are 100 percent tested.

[3] Low-frequency cutoff depends upon the value of external capacitors (see Pin Descriptions)

[4] From AUX IN; if ANA IN is driven at 50 mV p-p, the P_{OUT} = 12.2 mW, typical.

[5] With 5.1 K Ω series resistor at ANA IN.

[6] T_{PDS} is required during a static condition, typically overflow.

[7] Sampling Frequency and playback Duration can vary as much as ±2.25 percent over the commercial temperature range. For greater stability, an external clock can be utilized (see Pin Descriptions)

[8] Filter specification applies to the antialiasing filter and the smoothing filter. Therefore, from input to output, expect a 6 dB drop by nature of passing through both filters.

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10.2.1. Typical Parameter Variation with Voltage and Temperature (Die)

Chart 5: Record Mode Operating Current (I_{CC})

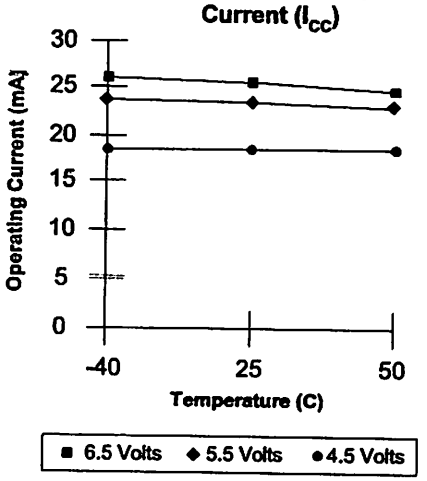


Chart 7: Standby Current (I_{SB})

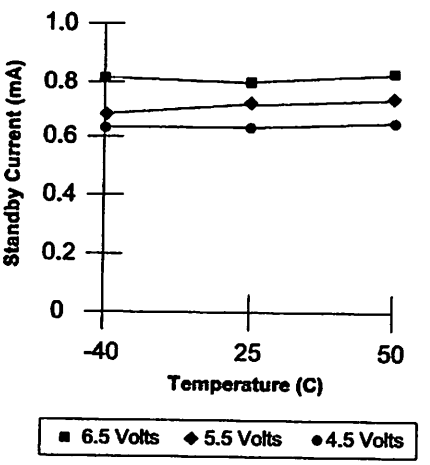


Chart 6: Total Harmonic Distortion

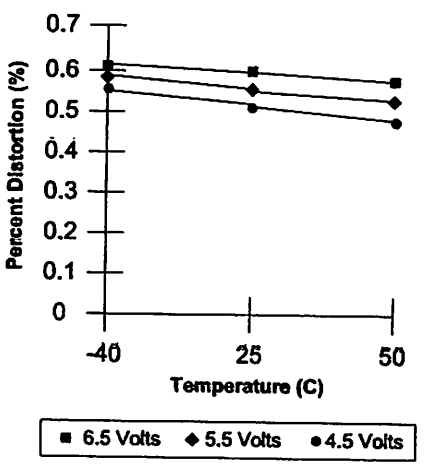
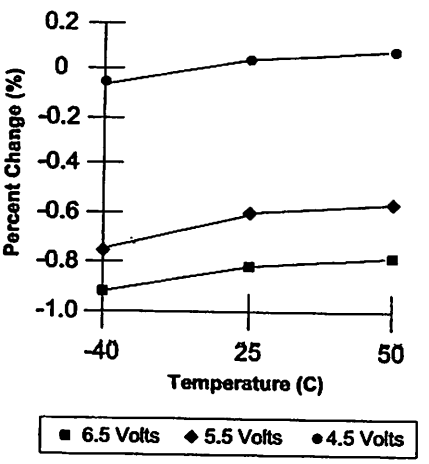


Chart 8: Oscillator Stability



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10.3. PARAMETERS FOR PUSH-BUTTON MODE

TABLE 12: PARAMETERS FOR PUSH-BUTTON MODE

PARAMETER	SYMBOL	MIN[2]	TYP[1]	MAX[2]	UNITS	CONDITIONS
$\overline{CE}$ Pulse Width (Start/Pause)	T_{CE}		300		nsec	
Control/Address Setup Time	T_{SET}		300		nsec	
Power-Up Delay	T_{PUD}					
ISD2560			25.0		msec	
ISD2575			31.25		msec	
ISD2590			37.25		msec	
ISD25120			50.0		msec	
PD Pulse Width (Stop/Restart)	T_{PD}		300		nsec	
$\overline{CE}$ to $\overline{EOM}$ HIGH	T_{RUN}	25		400	nsec	
$\overline{CE}$ to $\overline{EOM}$ LOW	T_{PAUSE}	50		400	nsec	
$\overline{CE}$ HIGH Debounce	T_{DB}					
ISD2560		70		105	msec	
ISD2575		85		135	msec	
ISD2590		105		160	msec	
ISD25120		135		215	msec	

Notes:

[1] Typical values @ T_A = 25°C and V_{CC} = 5.0V.

[2] All Min/Max limits are guaranteed by Winbond via electrical testing or characterization. Not all specifications are 100 percent tested.

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11. TYPICAL APPLICATION CIRCUIT

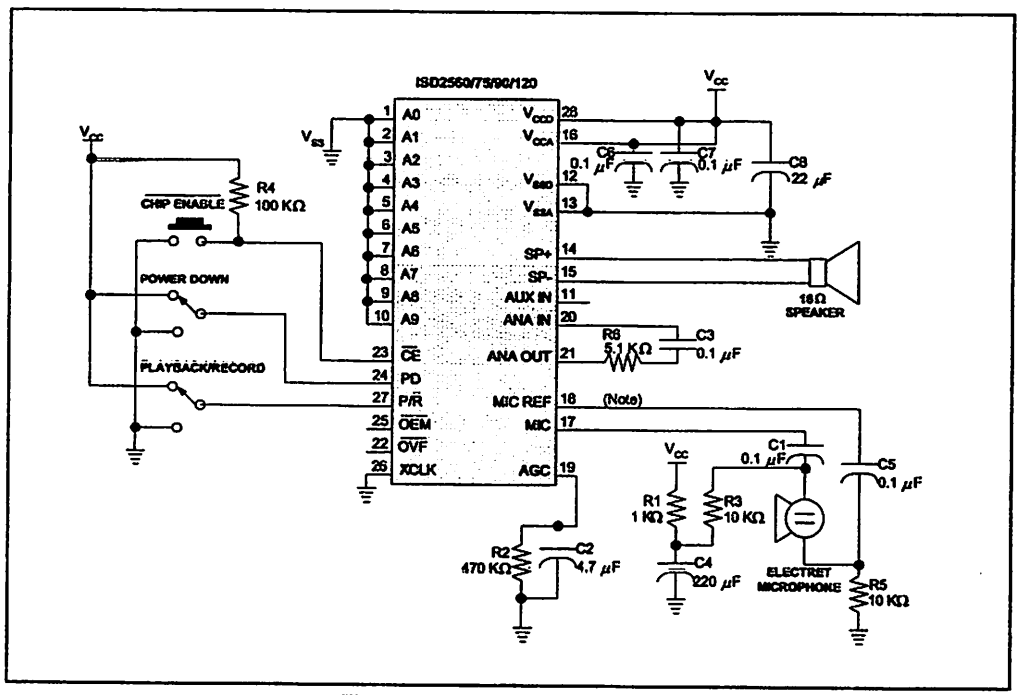

FIGURE 5: DESIGN SCHEMATIC

Note: If desired, pin 18 (PDIP package) may be left unconnected (microphone preamplifier noise will be higher). In this case, pin 18 must not be tied to any other signal or voltage. Additional design example schematics are provided below.

TABLE 13: APPLICATION EXAMPLE – BASIC DEVICE CONTROL

Control Step	Function	Action
1	Power up chip and select Record/Playback Mode	1. PD = LOW, 2. P/$\overline{R}$ = As desired
2	Set message address for record/playback	Set addresses A0-A9
3A	Begin playback	P/$\overline{R}$ = HIGH, $\overline{CE}$ = Pulse LOW
3B	Begin record	P/$\overline{R}$ = LOW, $\overline{CE}$ = LOW
4A	End playback	Automatic
4B	End record	PD or $\overline{CE}$ = HIGH

TABLE 14: APPLICATION EXAMPLE – PASSIVE COMPONENT FUNCTIONS

Part	Function	Comments
R1	Microphone power supply decoupling	Reduces power supply noise
R2	Release time constant	Sets release time for AGC
R3, R5	Microphone biasing resistors	Provides biasing for microphone operation
R4	Series limiting resistor	Reduces level to prevent distortion at higher supply voltages
R6	Series limiting resistor	Reduces level to high supply voltages
C1, C5	Microphone DC-blocking capacitor Low-frequency cutoff	Decouples microphone bias from chip. Provides single-pole low-frequency cutoff and command mode noise rejection.
C2	Attack/Release time constant	Sets attack/release time for AGC
C3	Low-frequency cutoff capacitor	Provides additional pole for low-frequency cutoff
C4	Microphone power supply decoupling	Reduces power supply noise
C6, C7, C8	Power supply capacitors	Filter and bypass of power supply

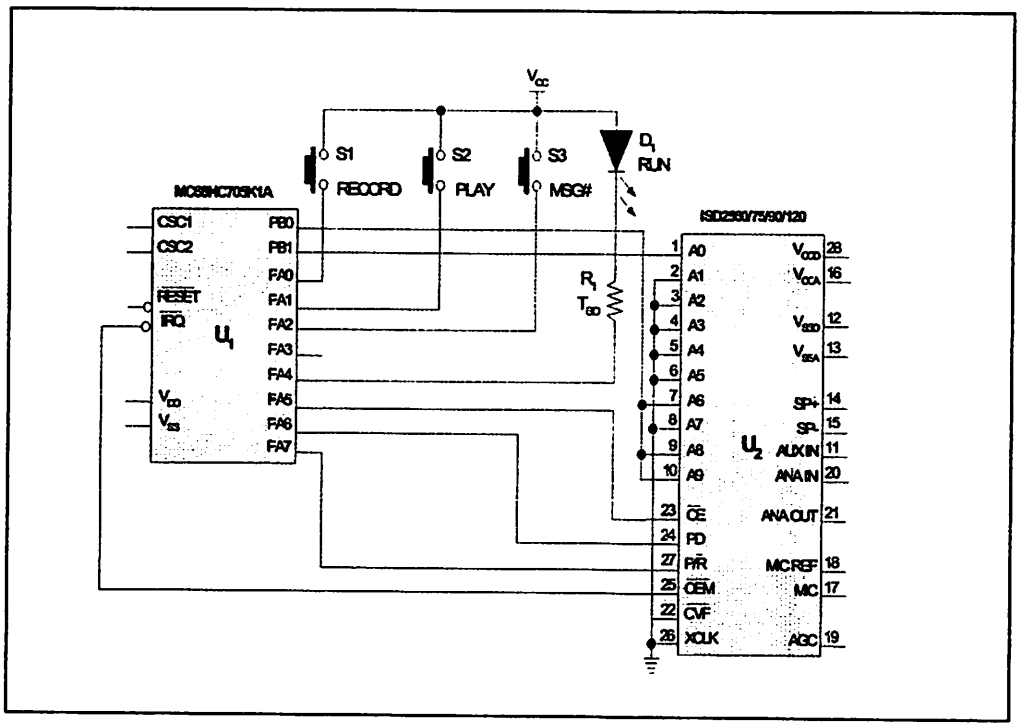

FIGURE 6: ISD2560/75/90/120 APPLICATION EXAMPLE – MICROCONTROLLER/ISD2500 INTERFACE

In this simplified block diagram of a microcontroller application, the Push-Button Mode and message cueing are used. The microcontroller is a 16-pin version with enough port pins for buttons, an LED, and the ISD2500 series device. The software can be written to use three buttons: one each for play and record, and one for message selection. Because the microcontroller is interpreting the buttons and commanding the ISD2500 device, software can be written for any function desired in a particular application.

Note: Winbond does not recommend connecting address lines directly to a microprocessor bus. Address lines should be externally latched.

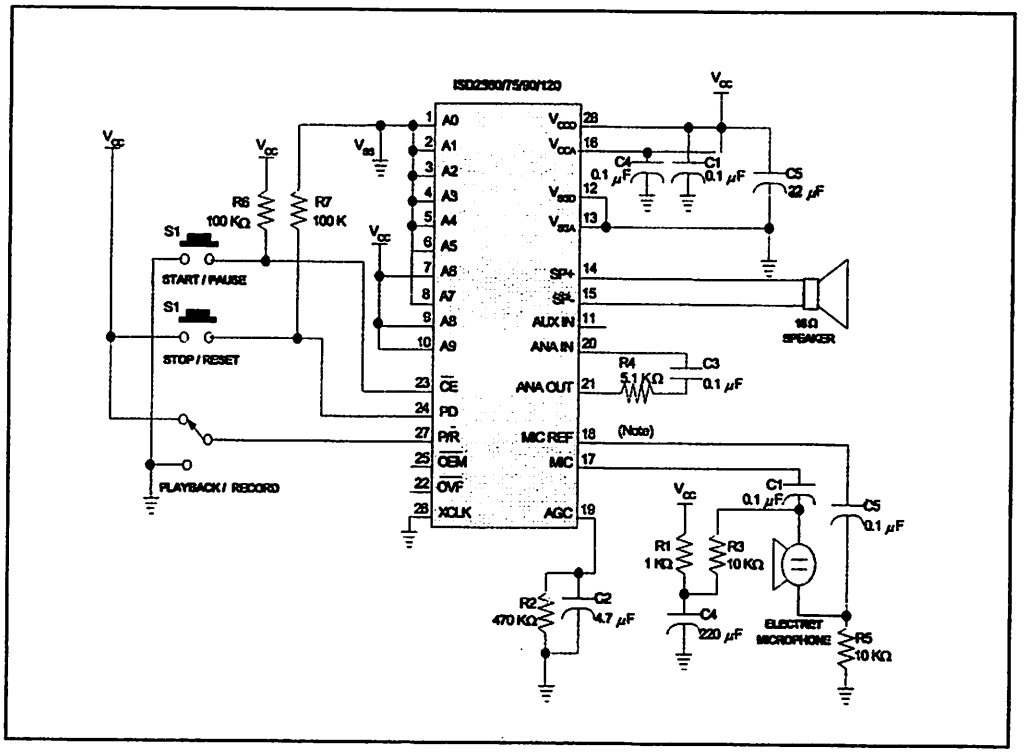

FIGURE 7: ISD2560/75/90/120 APPLICATION EXAMPLE – PUSH-BUTTON

Note: Please refer to page 13 for more details.

TABLE 15: APPLICATION EXAMPLE – PUSH-BUTTON CONTROL

Control Step	Function	Action
1	Select Record/Playback Mode	$P/\overline{R}$ = As desired
2A	Begin playback	$P/\overline{R}$ = HIGH, $\overline{CE}$ = Pulse LOW
2B	Begin record	$P/\overline{R}$ = LOW, $\overline{CE}$ = Pulse LOW
3	Pause record or playback	$\overline{CE}$ = Pulsed LOW
4A	End playback	Automatic at $\overline{EOM}$ marker or PD = Pulsed HIGH
4B	End record	PD = Pulsed HIGH

TABLE 16: APPLICATION EXAMPLE – PASSIVE COMPONENT FUNCTIONS

Part	Function	Comments
R2	Release time constant	Sets release time for AGC
R4	Series limiting resistor	Reduces level to prevent distortion at higher supply voltages
R6, R7	Pull-up and pull-down resistors	Defines static state of inputs
C1, C4, C5	Power supply capacitors	Filters and bypass of power supply
C2	Attack/Release time constant	Sets attack/release time for AGC
C3	Low-frequency cutoff capacitor	Provides additional pole for low-frequency cutoff