INSTITUT TEKNOLOGI NASIONAL MALANG
FAKULTAS TEKNOLOGI INDUSTRI
KONSENTRASI TEKNIK ELEKTRONIKA
JURUSAN TEKNIK ELEKTRO S-1

SKRIPSI

RANCANG BANGUN TIMBANGAN EMAS DAN PENGHITUNG/PENAMPIL HARGA SECARA ELEKTRONIK

Disusun Oleh :
YUSAK AL MUKHLAS
00.17.244

SEPTEMBER 2006

LEMBAR PERSETUJUAN

RANCANG BANGUN TIMBANGAN EMAS DAN PENGHITUNG/PENAMPIL HARGA SECARA ELEKTRONIK

SKRIPSI

Disusun dan diajukan sebagai salah satu syarat untuk memperoleh gelar Sarjana Teknik Elektronika Strata Satu (S-1)

Disusun Oleh :

YUSAK AL MUKHLAS
00.17.244

Diperiksa dan Disetujui Dosen Pembimbing I	Diperiksa dan Disetujui Dosen Pembimbing II
(Ir. Poerwanto,MT)	(Irmalia Suryani F., ST)

Mengetahui :
Ketua Jurusan Elektro S-1

(Ir. F.Yudi Limpraptono, MT.)
NIP.Y.1039500 274

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BERITA ACARA UJIAN SKRIPSI
FAKULTAS TEKNOLOGI INDUSTRI

Nama Mahasiswa	: Yusak Al Mukhlas
NIM	: 0017244
Jurusan	: Teknik Elektro S-1
Konsentrasi	: Teknik Elektronika
Judul Skripsi	: RANCANG BANGUN TIMBANGAN EMAS DAN PENGHITUNG/PENAMPIL HARGA SECARA ELEKTRONIK

Dipertahankan dihadapan Team Penguji Skripsi Jenjang Strata Satu (S-1) pada:

Hari	: Sabtu
Tanggal	: 23 September 2006
Dengan Nilai	: 81,9 (A)

Panitia Ujian Skripsi

Ketua	Sekretaris
(Ir. Mochtar Asroni, MSME)	**(Ir.F.Yudi Limpraptono, MT)**
NIP.Y. 1018100036	**NIP.Y. 1039500274**

Anggota Penguji

Penguji Pertama	Penguji Kedua
(Ir. Usman Djuanda, MM.)	**(Sotyohadi, ST, Msc.)**

YUSAK AL MUKHLAS, 2006. Judul " *Rancang Bangun Timbangan Emas dan Penghitung/Penampil Harga Secara Elektronik*" Skripsi Teknik Elektro Strata 1, Konsentrasi Teknik Elektronika, Fakultas Teknologi Industri, Institut Teknologi Nasional Malang, Dosen Pembimbing I : Ir. Poerwanto, MT, Dosen Pembimbing II : Irmalia Suryani F., ST

ABSTRAKSI

Kata kunci : Sensor Kapasitif, IC LM555, Keypad, AT89S8252, LCD.

Skripsi ini bertujuan untuk merancang dan membuat sistem pengukuran berat emas secara digital yang terdapat display harga dari emas tersebut berdasarkan berat emas yang sebenarnya (kalibrasi).

Karena itu, sehubungan dengan skripsi, saya bermaksud merancang timbangan emas elektronik (digital) yang juga mampu menunjukkan nilai rupiah harga emas yang sedang ditimbang. Alat ini memiliki keunggulan diantaranya tidak perlu lagi menghitung harga emas yang sedang ditimbang beratnya sebab sudah terhitung secara otomatis berdasarkan nilai karat dan berat, dan proses penimbangan bisa berlangsung lebih cepat karena tidak menggunakan anak timbangan atau pengesetan secara manual.

Pembuatan alat ini menggunakan sensor kapasitif sebagai pengukur beban dan IC LM555 sebagai pembangkit frekuensi yang datanya dibaca oleh mikrokontroller AT89S8252 dan outputnya berupa angka ditampilkan pada LCD. Tetapi sebelum kita menmberikan beban pada alat sebaiknya kita memeriksa dan mengatur kadar yang ada pada emas yang biasanya berupa karat beserta harganya untuk masing-masing kadar.

KATA PENGANTAR

Puji dan syukur kami panjatkan kehadirat Tuhan Yang Maha Esa karena atas segala berkah dan rahmat-Nya, kami dapat menyelesaikan Laporan Tugas Akhir ini dengan judul : " Rancang Basngun Timbangan Emas dan Penghitung/Penampil Harga Secara Elektronik"

Pada kesempatan ini kami sebagai penyusun mengucapkan banyak terima kasih kepada semua pihak yang telah membantu dan mendukung dari persiapan hingga selesainya Tugas Akhir ini.

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5. Dosen Penguji Laporan Tugas Akhir.
6. Seluruh staf pengajar dan karyawan Program Studi Teknik Elektronika ITN Malang.
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Penulis menyadari benar segala kekurangan yang ada pada penyusunan Laporan Akhir ini. Oleh sebab itu penulis mengharapkan segala kritik dan saran demi kesempurnaan Laporan Akhir ini. Semoga Laporan akhir ini dapat memberikan manfaat bagi pembaca dan semua pihak yang memerlukan.

Malang , September 2006

Penyusun

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BAB I

PENDAHULUAN

1.1. Latar Belakang

Kita melihat berat suatu benda dari satuan miligram sampai satuan ton menggunakan timbangan biasa dengan sistem pemberat (timbel) yang kini masih banyak digunakan. Kalau untuk satuan kilo gram sampai ton untuk mengkalibrasinya sangat mudah sekali karena tidak terlalu terpengaruh oleh kondisi cuaca (terutama angin). Sedangkan untuk satuan miligram sampai gram amat sangatlah peka terhadap keadaan alam sekitar, oleh sebab untuk menghindari hal tersebut timbangan emas yang manual menggunakan pelindung kaca disekelilingnya dan untuk mengetahui beratnya kita menggunakan pembanding dengan pemberat yang sama dengan berat barang yang akan kita timbang (misalkan emas).

Karena itu, sehubungan dengan skripsi, saya bermaksud merancang timbangan emas elektronik (digital) yang juga mampu menunjukkan nilai rupiah harga emas yang sedang ditimbang. Alat ini memiliki keunggulan diantaranya tidak perlu lagi menghitung harga emas yang sedang ditimbang beratnya sebab sudah terhitung secara otomatis berdasarkan nilai karat dan berat, dan proses penimbangan bisa berlangsung lebih cepat karena tidak menggunakan anak timbangan atau pengesetan secara manual.

1.2. Tujuan

Penelitian ini bertujuan untuk merancang dan membuat sistem pengukuran berat emas secara digital yang terdapat display harga dari emas tersebut berdasarkan berat emas yang sebenarnya (kalibrasi).

1.3. Rumusan Masalah

Masalah yang mungkin timbul dalam perancangan dan membuat alat timbangan emas meliputi :

1. Bagaimana membuat sensor berat emas secara elektronik menggunakan Sensor Capasitif.
2. Menggunakan bahasa pemrograman assembly untuk Mikrokontroller AT89S8252.
3. Bagaimana mengkalibrasi timbangan.
4. Bagaimana menghitung dan menampilkan berat dan harga total untuk emas yang sedang ditimbang..

1.4. Batasan Masalah

Penelitian ini hanya terbatas pada:

1. Range timbangan yang dibuat antara 0 gram sampai 100 gram
2. Sistem pengkalibrasi timbangan menggunakan timbangan yang sudah ada dan pengkalibrasiannya dilakukan secara software.
3. Menggunakan Keypad sebagai masukan database mikrokontroller AT89S8252.

4. Menggunakan LCD sebagai display untuk mempermudah pengamatan.
5. Keakurasian direncanakan sampai dengan 5 %.
6. Tidak membahas tentang kadar emas (karat).

1.5. Metodologi

1.5.1. Studi Literatur

hal pertama yang akan kita kerjakan adalah mencari literature bahasa pemrograman dengan menggunakan bahasa assembler, LCD (Liquid Circuit Display), Capasitif, Keypad, dan sebagai otak dari alat ini adalah Mikrokontroller AT89S8252.

1.5.2. Perencanaan Alat

Setelah memahami teori tersebut diatas kemudian dilanjutkan dengan perencanaan rangkaian dan PCB-nya (Project Circuit Board) yang akan kita buat serta tidak lupa pembuatan program assembly untuk Mikrokontroller AT89S8252. Jika rangkaian dan program sudah berjalan sesuai dengan yang diinginkan.

1.5.3. Pengujian Alat

Kita harus menguji satu persatu rangkaian yang telah kita rakit, pertama kita menguji Sensor Capasitif yang nantinya kita gunakan untuk sensor pembacaan data pada Berat emas, pengujian keypad juga harus kita lakukan untuk menghindari kesalahan setelah keseluruhan rangkaian dirakit, untuk pengujian Mikrokontroller

AT89S8252 dan LCD hendaknya menunggu semua rangkaian telah terpasang sesuai dengan apa yang telah kita rencanakan setelah semua benar maka rangkaian dipindah ke PCB (Project Circuit Board) dan dimasukkan kedalam kotak (BOX). Langkah terakhir adalah penulisan laporan dalam bentuk laporan skripsi.

1.5.4. Kesimpulan

Dari pengujian yang telah kita lakukan maka dapat ditarik kesimpulan dari keunggulan dan kekurangan alat kita.

1.6. Sistematika Penulisan

Sistematika penulisan dalam Skripsi ini terdiri dari 5 bab, yaitu :

BAB I : PENDAHULUAN

Menjelaskan tentang latar belakang, Rumusan masalah, Batasan masalah. Tujuan, Metodologi Penulisan.

BAB II : TEORI DASAR

Menjelaskan tentang teori yang mendukung agar supaya alat kita bisa bekerja yaitu berupa : mikrokontroller AT89S8252, resistor, transistor, capasitor, LCD, dioda, Capasitif, op-amp.

BAB III : PERENCANAAN DAN PEMBUATAN ALAT

Membahas tentang macam-macam alat yang akan kita gunakan beserta rangkaiannya. Baik berupa hardware maupun software sehingga nantinya alat yang telah kita buat bisa bekerja dengan baik dan sesuai dengan apa yang kita inginkan.

BAB IV : PENGUJIAN ALAT

Berisi tentang bagaimana caranya alat agar bisa bekerja dan kita melakukan pengujian terhadap alat kita.

BAB V : PENUTUP

Berisi kesimpulan dan saran tentang alat tersebut dan memuat kesimpulan yang diperoleh dari perancangan alat serta saran-saran untuk pengembangan lebih lanjut.

BAB II
TEORI DASAR

Pada bab ini kita akan membahas tentang teori dasar dari komponen yang kita gunakan dalam pembuatan alat pengkoreksi lembar jawaban komputer. Mulai dari Mikrokontroller AT89S8252 sebagai otak tempatnya proses dari masukan yang berupa data dari infra merah menjadi keluaran dalam bentuk cetakan kertas dari printer.

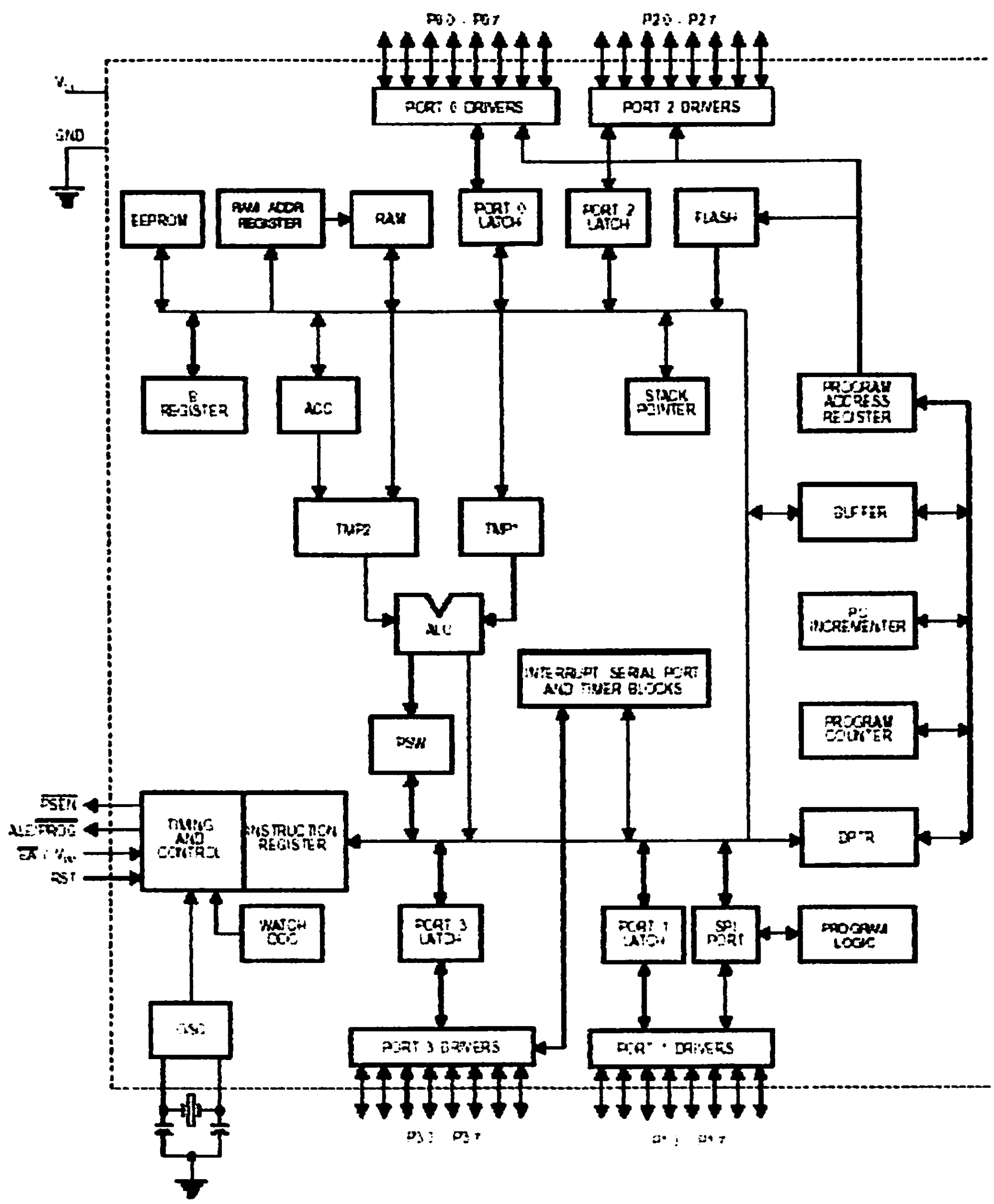
2.1. Mikrokontroler AT89S8252

Mikrokontroler AT89S8252 merupakan versi CHMOS dari AT89S8252 yaitu versi NMOS. NMOS merupakan kependekan dari *N-Channel Metal Oxide Silicon* dan kompatibel dengan MCS-51 mikrokomputer yang merupakan produksi dari ATMEL. Seri AT89S8252 terdiri dari beberapa jenis tingkat kecepatan mulai dari 12 MHz sampai dengan 24 MHz. Digunakan untuk beberapa keperluan mulai dari komersial, industri, otomotif, dan militer.

Arsitektur dari MCU AT89S8252 adalah sebagai berikut :

1. Compatible with MCS-51™ Products
2. 8K Bytes of In-System Reprogrammable Downloadable Flash Memory
   a. SPI Serial Interface for Program Downloading
   b. Endurance: 1,000 Write/Erase Cycles
3. 2K Bytes EEPROM
   a. Endurance: 100,000 Write/Erase Cycles

4. 4.0V to 6V Operating Range
5. Fully Static Operation: 0 Hz to 24 MHz
6. Three-Level Program Memory Lock
7. 256 x 8-bit Internal RAM
8. 32 Programmable I/O Lines
9. Three 16-bit Timer/Counters
10. Nine Interrupt Sources
11. Programmable UART Serial Channel
12. SPI Serial Interface
13. Low Power Idle and Power Down Modes
14. Interrupt Recovery From Power Down
15. Programmable Watchdog Timer
16. Dual Data Pointer
17. Power Off Flag



Gambar 2-1

Blok Diagram AT89S8252

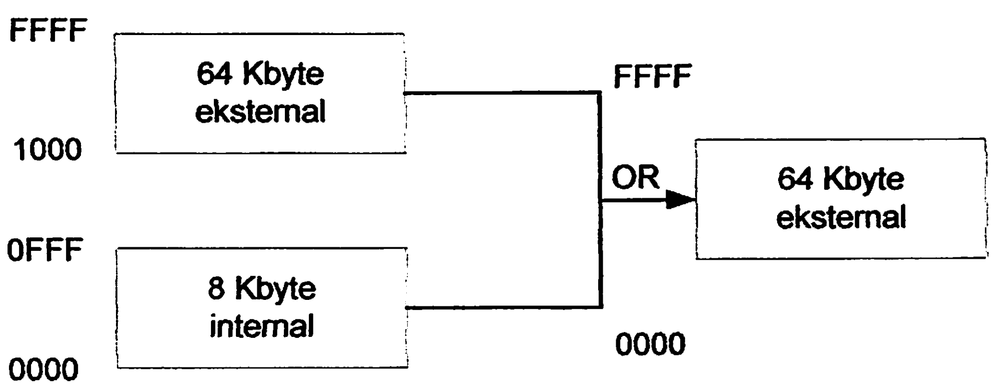
(Sumber : Data Sheet AT89S8252 Hal. 02)

2.1.1. Organisasi Memori MCU AT89S8252

Mikrokontroler keluarga MCS-51 memiliki memori program dan memori data yang terpisah. Pemisahan ini dilakukan secara logika sehingga

CPU dapat mengakses sampai 64 *Kbyte* memori program dan 64 *Kbyte* memori data. Lebar memori data internal adalah 8 bit dan 16 bit (register PC dan register DPTR).

2.1.1.1. Memori Program



Gambar 2-2

Memori program MCS-51

(Sumber : Advanced Microdevice)

Memori program menggunakan alamat sepanjang 64 *Kbyte* dengan 8 *Kybte* (alamat $0000 sampai dengan $0FFF) yang merupakan memori internal sehingga 60 *Kbyte* merupakan memori eksternal. Dapat menggunakan 64 *Kbyte* memori eksternal sebagaimana yang ditunjukkan pada gambar memori data.

Memori program merupakan tempat penyimpanan data permanen. Memori program lebih dikenal dengan nama *Read Only Memory* (ROM). Data dalam ROM tidak akan terhapus meskipun catu daya dimatikan atau dikenal sebagai sifat *non-volatile*. Karena sifatnya yang demikian ROM dapat digunakan untuk menyimpan program.

Ada beberapa tipe ROM, antara lain :

a. ROM (*Read Only Memory*)

   Merupakan memori yang sudah diprogram oleh pabrik (ROM murni).

b. PROM (*Programmable Read Only Memory*)

   Merupakan memori yang dapat diprogram oleh pemakai tetapi tidak dapat diprogram ulang.

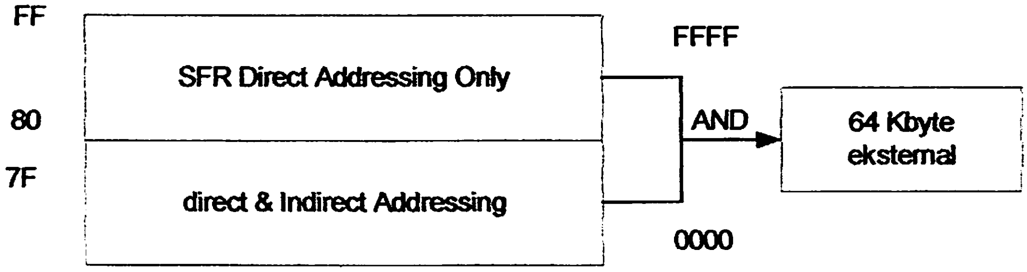
c. EPROM (*Erasable Programmable Read Only Memory*)

   Merupakan PROM yang dapat diulang. ROM ini juga terdapat pada mikrokontroler 8751, hal ini ditandai dengan adanya jendela kaca pada konstruksi IC 8751 yang digunakan untuk menghapus atau memperbaiki program yang sudah ada.

d. EEPROM (*Electrical Erasable Programmable Read Only Memory*)

   Pada prinsipnya hampir sama dengan EPROM, tetapi perbedaaanya terletak pada pengosongan atau penghapusan program. Untuk EPROM dapat dihapus dengan menggunakan sinar *ultra violet*, sedangkan pada EEPROM pengisian program dapat dilakukan langsung atau menumpuk program lama dengan program yang baru. EEPROM lebih fleksibel dibandingkan EPROM.

2.1.1.2. Memori Data



Gambar 2-3

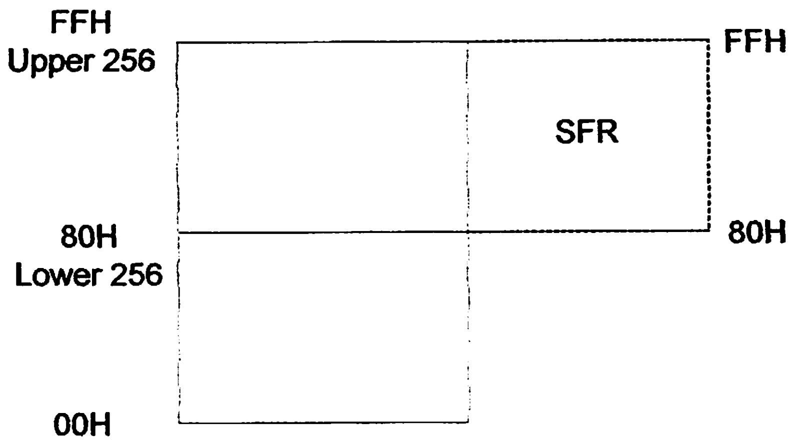
Memori data MCS-51

(Sumber : Advanced Microdevices)

Memori data merupakan tempat penyimpanan data yang bersifat sementara atau *volatile*. Dengan kata lain data akan hilang bila tidak dicatu. Memori data lebih dikenal dengan nama RAM (*Random Access Memory*), yaitu dapat dilakukan pembacaan dan penulisan data alamat yang tersedia.

Memori MCS-51 mempunyai 256 *bytes* RAM internal ditambah sejumlah register fungsi khusus atau *Special Function Register* (SFR). (*Advanced Mikrodevides*, 1988.1.6). Selain mempunyai memori internal, MCU AT89S8252 mempunyai memori eksternal yang memiliki pengalamatan sampai 64 *Kbytes*.

Pada keluarga mikrokontroler MCS-51, ruang memori data eksternal terbagi menjadi 3 blok yang disebut *lower* 256, *upper* 256 dan ruang SFR, sebagaimana ditunjukkan pada gambar di bawah ini.



Gambar 2-4

Memori Data Eksternal

(Sumber : Advanced Microdevices)

Pada *lower* 256 lokasi memori dibagi menjadi 3 bagian :

1. Register bank 0 – 3

   Lokasi bank register dimulai dari alamat 00h – 1h yang terdiri dari 32 *bytes*. Register bank ini terdiri dari 4 buah register 8 bit yang dapat dipilih melalui pengaturan *program status word* register.

2. Bit *Addressing*

   Terdiri dari 16 *bytes* yang dimulai dari 20h – 2fh. Masing-masing dari 128 bit lokasi ini dapat dialamati secara langsung yaitu dari $00h sampai $7fh.

3. *Scratch Pad Area*

Lokasi dari alamat $30h sampai $7fh atau sebanyak 80 *bytes* yang dapat digunakan sebagai alamat bagi RAM.

Pada 256 *bytes* atas (*upper* 256) ditempati oleh register yang mempunyai fungsi khusus yang disebut dengan *Special Fuction Register* (SFR). Ruang dari register fungsi khusus ini adalah dari 80h sampai FFh. Berikut ini adalah contoh isi vector alamat pada *Special Function Register.*

a. Akumulator (Acc) atau register A dan register B.

Kedua register tersebut digunakan untuk operasi perkalian dan pembagian.

b. *Program Status Word*

Register ini meliputi bit-bit : CY (*Carry*), AC (*Auxillary Carry*), FO sebagai flag, RS0 dan RS1 untuk pemilih register bank, OV (*Over Flow*), dan *parity flag.*

c. *Stack Pointer* (SP)

SP merupakan register yang digunakan untuk penunjuk alamat. Register ini berguna apabila digunakan suatu *routine* pada program utama.

d. *Data Pointer High* (DPH) dan *Data Pointer Lower* (DPL)

DPTR adalah register yang digunakan untuk pengalamatan tidak langsung. Register ini digunakan untuk mengakses memori program baik internal maupun eksternal. DPTR dikontrol oleh 2 buah register 8 bit yaitu DPH dan DPL.

e. *Port 0, Port 1, Port 2, Port 3*

Pada keluarga 8051 masing-masing *port* dapat dialamati langsung baik secara *byte* atau bit. Masing-masing *port* merupakan *port bi-directional* (*input/output*) :

1. *Port* 0 digunakan sebagai pengalamatan memori dari luar.
2. *Port* 1 digunakan sebagai I/O dari mikrokontroler.
3. *Port* 2 digunakan sebagai pengalamatan memori dari luar.
4. *Port* 3 berisi sinyal kontrol seperti *interrupt serial*, WR, dan RD.

f. *Register Prioritas Interrupt* (*Interrupt Priority Register* /IP).

Merupakan register yang berisi bit-bit untuk mengaktifkan prioritas dari suatu *interrupt* yang ada pada mikrokontroler pada taraf yang diinginkan.

g. *Interrupt Enable Register*

Merupakan register yang berisi bit-bit untuk menghidupkan atau mematikan sumber-sumber *interrupt*.

h. *Timer/Counter Control Register*

TCON merupakan register yang berisi bit-bit memulai atau menghentikan pencacah atau pewaktu.

i. *Serial Control Buffer*

Register ini digunakan untuk menampung data masukan (SBUF *in*) atau keluaran (SBUF *out*) dari *serial port*.

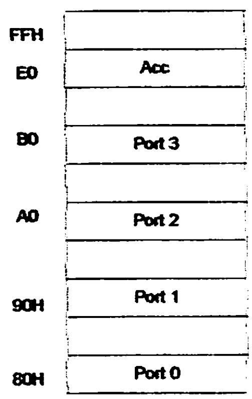
Tabel 2-1
Pembagian alamat pada SFR

Simbol	Nama	Alamat
Acc	Accumulator	0E0H
B	B register	0F0H
PSW	Program Status Word	0D0H
SP	Stack Pointer	81H
DPTR	Data Pointer 2 bytes	
DPL	Low byte	82H
DPH	High byte	83H
P0	Port 0	80H
P1	Port 1	90H
P2	Port 2	0A0H
P3	Port 3	0B0H
IP	Interrupt Priority	0B8H
IE	Control	ABH
TMOD	Interrupt Enable	89H
TCON	Control	88H
TH0	T/C Mode Control	8CH
TL0	T/C Control	8AH
TH1	T/C 0 High Control	8DH
TL1	T/C 0 Low Control	8BH
SCON	T/C 1 High Control	98H

SBUF PCON	T/C 1 Low Control Serial Control Serial Buffer Power Control	99H 87H

(Sumber : Paulus Andi Nalwan, Teknik Antar Muka dan Pemrograman Mikrokontroller AT89C51 Hal. 07)

Adapun diagram blok dari SFR adalah sebagai berikut :



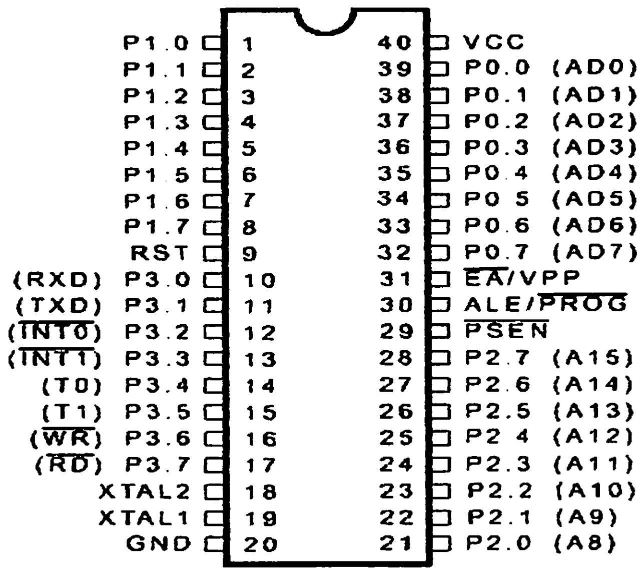
Gambar 2-5

Ruang Special Function Register

(Sumber : Paulus Andi Nalwan, Teknik Antar Muka dan Pemrograman Mikrokontroller AT89C51)

2.1.2. Konfigurasi Kaki-kaki MCU AT89S8252

Berikut ini adalah bentuk fisik dari AT89S8252.



Gambar 2-6

Bentuk Fisik AT89S8252

(Sumber : Data Sheet AT89S8252)

Fungsi-fungsi dari tiap-tiap pin sebagai berikut :

a. Vss

Dihubungkan dengan *ground* rangkaian atau media pentanahan.

b. Vcc

Dihubungkan dengan sumber tegangan + 5 V.

c. *Port* 0 (P0.0 – P0.7)

Port 0 merupakan *port* I/O 8 bit dua arah. *Port* ini digunakan sebagai multipleks bus alamat rendah dan bus data selama pengaksesan ke memori luar.

d. *Port* 1 (P1.0 – P1.7)

Port 1 dapat difungsikan sebagai masukan atau keluaran dan bekerja baik untuk operasi bit maupun *byte*, tergantung dari pengaturan program yang dibuat.

e. *Port* 2 (P2.0 – P2.7)

Port 2 dapat digunakan sebagai alamat bus baik *byte* tinggi selama adanya akses ke memori program atau memori data luar.

f. *Port* 3 (P3.0 – P3.7)

Port 3 mempunyai fungsi sebagai I/O juga mempunyai fungsi khusus sebagai berikut :

g. RD (P3.7), sinyal pembacaan memori data luar.

h. WR (P3.6), sinyal penulisan memori data luar.

i. T1 (P3.5), masukan dari pewaktu/pencacah 1.

j. T0 (P3.4), masukan dari pewaktu/pencacah 0.

k. INT1 (P3.3), masukan interrupt 1.

l. INT0 (P3.2), masukan interrupt 0.

m. TXD (P3.1), keluaran pengiriman data untuk serial *port* (*asynchronous*) atau sebagai keluaran *clock* (*sybchronous*).

n. RXD (P3.0), masukan data serial atau sebagai keluaran data.

o. RST/VPD, merupakan pin input yang aktif jika pin aktif tinggi selama dua siklus mesin maka ketika osilator bekerja akan mereset peralatan.

p. ALE (*Address Latch Enable*), pin ALE (aktif tinggi) mengeluarkan pulsa output untuk menyangga (*latch*) satu byte alamat rendah selama mengakses ke memori eksternal. ALE dapat mengendalikan 8 beban TTL. Pin ini juga merupakan input pulsa program yang aktif rendah selama pemrograman EPROM. Pada operasi normal, ALE dikeluarkan pada suatu kecepatan yang konstan yaitu 1/6 dari frekuensi osilator dan dapat digunakan untuk *timing* eksternal atau untuk tujuan membuat *clock*.

q. PSEN (*Program Strobe Enable*). Pin ini aktof rendah yang merupakan *strobe* pembacaan ke program memori eksternal.

r. XTA1, pin XTAL1 merupakan pin input ke penguat osilator pembalik dan XTAL2 merupakan pin output dari penguat osilator pembalik.

s. EA,VPP (*External Access/Programming Supply Voltage*), pin EA di Vcc agar AT89S8252 dapat mengakses kode mesin dari program memori.

2.1.3. Metode Pengalamatan

Metode pengalamatan yang digunakan pada MCS-51 terbagi menjadi dua jenis, yaitu pengalamatan langsung dan pengalamatan tidak langsung. (Moh. Ibnu Malik, 1997:36)

1. Pengalamatan Tak Langsung

Operasi pengalamatan tak langsung menunjukkan ke sebuah register yang berisi lokasi alamat memori yang akan digunakan dalam suatu operasi. Lokasi yang nyata tergantung dari isi register saat instruksi dijalankan. Untuk melakukan pengalamatan tak langsung digunakan

ADD A, @R0 : tambahkan isi R0 dengan Acc dan hasilnya di Acc

a. DEC @R1 : kurangi isi dari alamat R1

2. Pengalamatan Langsung

Pengalamatan langsung dilakukan dengan memberikan nilai ke suatu register secara langsung. Untuk melakukan hal tersebut digunakan tanda #. Misalnya :

a. MOV A,#01H : isi Acc dengan data 01H

b. MOV DPTR,#19H : isi DPTR dengan data 19H

Pengalamatan data langsung dari 0 sampai 127 akan mengakses RAM internal, sedangkan pengalamatan dari 128 sampai 255 akan mengakses register perangkat keras. Misalnya :

a. MOV P3,A : pindahkan isi Acc ke alamat *Port* 3 (B0H)

b. INC 50 : naikkan lokasi 50 (desimal) dalam memori

2.1.4. Bahasa Assembler MCS-51

Bahasa assembler digunakan dalam setiap operasi CPU dalam bentuk bahasa yang disusun berurutan dalam pernyataannya. Masing-masing pernyataan akan diterjemahkan ke dalam instruksi bahasa mesin atau sering disebut *operation code/opcode*. Dalam penulisan bahasa mesin ini, terdapat berbagai macam kelompok instruksi, diantaranya :

a. Perpindahan Data

Instruksi ini digunakan untuk memindahkan data antar register, memori, register-memori, antar muka register dan antar muka memori.

Contonya : MOV A,R0 : memindahkan isi register R0 ke Acc.

MOV A,@R0 : memindahkan isi alamat R0 ke Acc.

b. Operasi Aritmatika

Instruksi ini melaksanakan operasi aritmatika yang meliputi penjumlahan, pengurangan, perkalian, maupun pembagian.

Contohnya : ADD A,#data : menambah Acc dengan data.

ADC A,#data : menambah Acc dengan data dan carry.

INC R6 : menambah isi R6 dengan 1.

DEC R7 : mengurangi isi R5 dengan 1.

MUL AB : mengalikan isi Acc dengan isi register B.

DIV AB : membagi isi Acc dengan isi register B.

c. Operasi Percabangan

Instruksi ini mengubah urutan normal pelaksanaan suatu program untuk melaksanakan pada lain tempat yang kita perlukan pada saat itu. Contohnya :

1. CJNE (*Compare Jump Not Equal*)

   Instruksi ini membandingkan isi lokasi memori tertentu dengan isi Acc, jika sama instruksi ini selanjutnya akan dieksekusi. Jika tidak sama eksekusi akan kembali ke alamat kode yang telah ditunjuk.

2. JB (*Jump if Bit Set*)

Instruksi ini akan menguji suatu alamat bit isi satu, eksekusi akan menuju ke alamat kode dan jika tidak instruksi akan dilanjutkan.

3. JNB (*Jump if Bit Not Set*)

Instruksi ini menguji suatu alamat bit. Jika berisi 0 maka eksekusi akan menuju ke alamat kode. Jika berisi 1 maka instruksi selanjutnya yang akan dieksekusi.

2.2. Sensor Kapasitif

Pada dasarnya kapasitor merupakan alat penyimpan muatan listrik yang dibentuk dari dua permukaan (piringan) yang berhubungan, tetapi dipisahkan oleh suatu penyekat. Bila sebuah kapasitor dihubungkan dengan tegangan searah terjadilah antara-antara penghantar suatu selisih potensial (tegangan). Selisih suatu potensial ini diringi dengan pergeseran dari muatan listrik. Sehingga penghantar yang lain yang sama besarnya mendapat muatan negatif.

Kapasitas dari kapasitor dinyatakan dengan :

$$\text{Kapasitansi } C = \frac{Q}{V} \quad \text{...(2.5)}$$

Dimana : Q = Muatan (Coloumb)

C = Kapasitansi (Farad)

V = Tegangan (Volt)

Kapasitor banyak digunakan dalam sirkit elektronik dan mengerjakan berbagai fungsi. Pada dasarnya kapasitor merupakan alat penyimpan muatan listrik yang dibentuk dari dua permukaan (piringan) yang berhubungan, tetapi dipisahkan oleh suatu penyekat. Bila elektron berpisah dari satu plat ke plat yang lain, akan terdapat muatan diantara mereka pada medium penyekat tadi. Muatan ini disebabkan oleh muatan positif pada plat yang kehilangan elektron dan muatan negatif pada plat yang memperoleh elektron.

Dari keterangan diatas dapat ditarik kesimpulan bahwa kepasitor dapat dibentuk dimanapun asalkan kondisi diatas terpenuhi. Dengan kata lain, kapasitor dapat dibuat berdasarkan cara ini dan kapasitor "yang tidak diharapkan" juga dapat ditemukan ditempat-tempat tertentu, seperti pada dua jalur kabel terpisah yang bekerja sama atau pada pertemuan alat semi konduktor.

Muatan (bersimbol Q) diukur dengan satuan couloumb dan kapasitor yang memperoleh muatan listrik akan mempunyai tegangan terminal sebesar V volt. Kemampuan kapasitor dalam menyimpan muatan disebut kapasitansi (bersimbol C). kapasitansi ini diukur berdasarkan besar muatan yang dapat disimpan pada suatu kenaikan tegangan.

Permukaan kapasitor yang berhubungan biasanya berbentuk "plat" rata. Ukuran kapasitor tergantung pada luas plat, A, jarak antar plat, d, dan medium penyekat. Kapasitansi dapat dihiting lewat rumus :

$$C = \epsilon \, {}^{A}\!/_{d}$$

Dimana $\epsilon = \epsilon_o \epsilon_r$; ϵ_o = tempat yang tersedia (permitivitas tempat), berupa bilangan konstanta ; ϵ_r = permitivitas relatif, berupa faktor perkalian yang tergantung pada medium penyekat atau bahan *dielektris* yang digunakan diantara kedua plat.

Kapasitansi diukur dalam satuan *farad* (bersimbol F).

Satuan

Sebuah kapasitor dikatakan mempunyai kapasitansi 1F kalau muatan sebesar 1 C membuat tegangan naik sebesar 1 V.

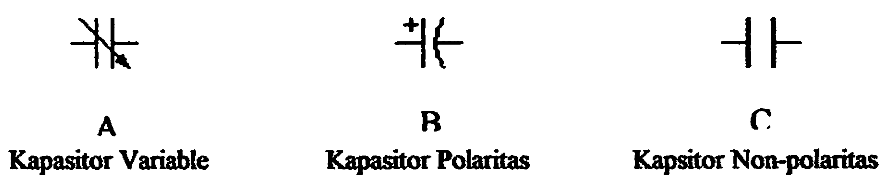
Namun farad ternyata terlampau besar, sehingga digunakan mikrofarad dan satuan yang lebih kecil lainnya :

1 mikrofarad = 1 μF = 1 x 10^{-6} F,

1 nano farad = 1 nF = 1 x 10^{-9} F,

1 pikofarad = 1 pF = 1 x 10^{-12} F.

Kapasitas dari kapasitor dinyatakan dengan Farad (F) $1F = \frac{1C}{1V}$

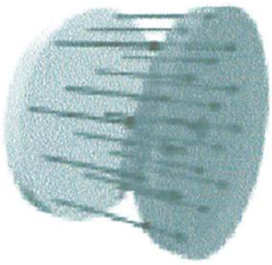


Gambar 2-7

Simbol Kapasitor

(Sumber : Drs. Ridwan Rusli, Teknik Elektronika)

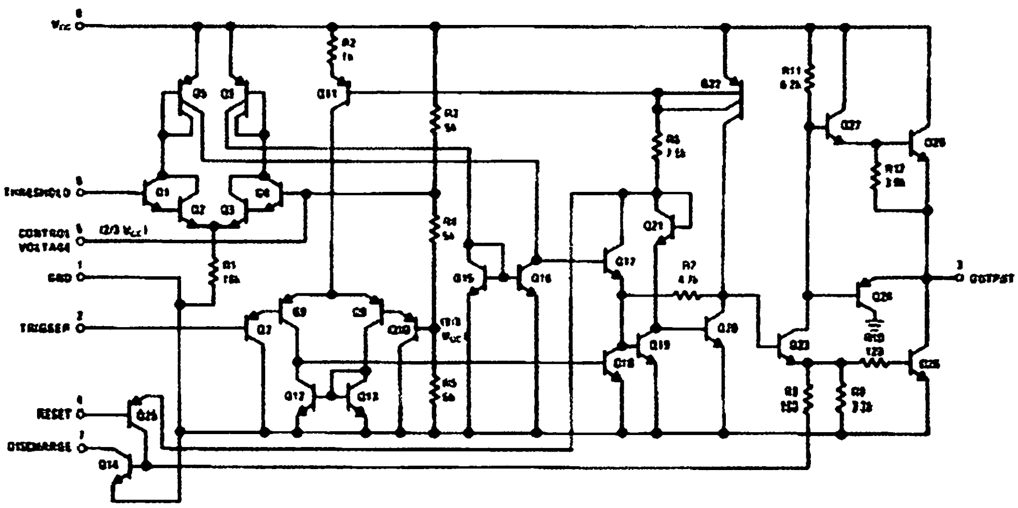
Simbol dari sensor kapasitif sama dengan kapasitor variable pada gambar 2-7, Karena adanya dua lempengan logam yang berhimpitan dan berinti udara serta mempunyai nilai yang berubah-ubah, semakin menekan kebawah atau lempengannya semakin dekat maka nilai kapasitifnya semakin kecil. Untuk lebih jelasnya kita lihat gambar dibawah ini :



Gambar 2-8
Sensor Kapasitif
(Sumber : www.lionprecision.com)

2.3. LM555

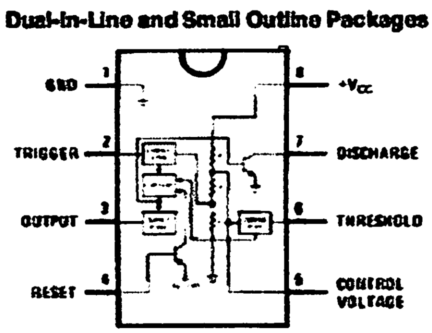
IC ini biasa difunakan untuk mengolah atau membangkitkan frekuensi (Osilator) bisa juga digunakan untuk menentukan waktu (Timers). Mempunyai tegangan sumber 200mA serta kompatibel untuk dipakai bersama mikrokontroller atau IC TTL, mempunyai temperatur untuk kestabilan bekerja 0,005% per ^{0}C. tingkat perhitungannya adalah sampai dengan mikroseconds. IC 555 adalah kumpulan dari transistor logika. Untuk lebih jelasnya kita lihat skematik diagram dari IC LM555



Gambar 2-9

Skematik Diagram ICLM555

(Sumber : Data Sheet LM555)



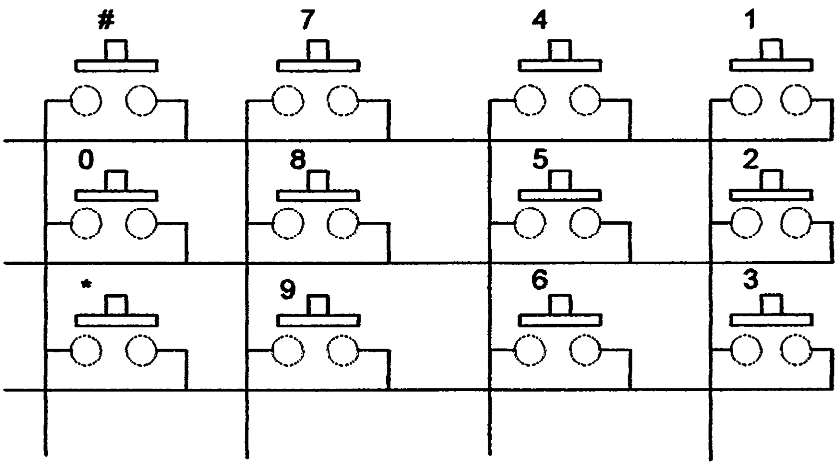
Gambar 2-10

Bentuk kaki dari IC LM555

(Sumber : Data Sheet LM555)

2.4. Keypad

Keypad ini digunakan sebagai salah satu dari inputan untuk operasi password dan membuka serta menutup inti brankas. Untuk Keypad ini digunakan jenis Keypad dengan 4 x 3. seperti yang diperlihatkan pada gambar 2-4



Gambar 2-11

Keypad 4 x 3

(Sumber : elektronika digital)

Tabel 2-2

Kombinasi Output Keypad Matrik 4x4 [4]

Posisi Saklar		0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
		Y1	Y1	Y1	Y1	Y2	Y2	Y2	Y2	Y3	Y3	Y3	Y3	Y4	Y4	Y4	Y4
		X1	X2	X3	X4	X1	X2	X3	X4	X1	X2	X3	X4	X1	X2	X3	X4
DATA OUT	A	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1
	B	0	0	1	1	0	0	1	1	0	0	1	1	0	0	1	1
	C	0	0	0	0	1	1	1	1	0	0	0	0	1	1	1	1
	D	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1

(Sumber : elektronika digital)

Berdasarkan tabel diatas kita dapat dengan mudah menyeleksi tombol mana yang ditekan dari rangkaian keypad yang dibuat. Keluaran tombol yang dipilih dihubungkan langsung dengan P2.0-P2.7 dan selanjutnya display akan menampilkan karakter dengan angka yang dipilih.

2.5. LCD Module M1632

Sebagai tampilan yang telah diproses oleh mikrokontroler maka dibutuhkan suatu perangkat yang brfungsi sebagai alat keluaran. Diharapkan dengan adanya display ini pengguna dapat mengetahui data dan informasi hasil proses yang dikehendaki.

Suatu perangkat display yang siap pakai dan mudah didapatkan serta banyak dipakai adalah LCD Dot matrik 2 x 16 karakter, jenis LCD mudah dalam penggunaannya. Dalam perencanaan dan pembuatan alat ini digunakan LCD type M1632 dari Seico Instrument.

Struktur pin-pin dan cara pengaksesannya pada LCD M1632 dijelaskan pada table berikut ini :

Tabel 2-3

definisi pin LCD Modul M163

Pin No	Simbol	Level	Keterangan
1	Vss	.	Power Supply
2	Vcc		
3	Vee		
4	RS	H/L	H : Data Input L : Intrupsi Input

5	R/W	H/L	H : read L : Disable
6	E	H/L	H: Enable L : Disable
7	DB0	H/L	
8	DB1	H/L	
9	DB2	H/L	
10	DB3	H/L	
11	DB4	H/L	
12	DB5	H/L	
13	DB6	H/L	
14	DB7	H/L	
15	V + BL		Power Suplly
16	V – BL		

(Sumber: Module User Manual)

Intruksi –intruksi untuk dapat mengakses LCD tipe M 1632 dijelaskan pada tabel 2-4 berikut :

Tabel 2-4

Perintah Dalam Pengaksesan LCD

Intruksi	Code										Fungsi
	RS	R/W	DB 7	DB 6	DB 5	DB 4	DB 3	DB 2	DB 1	DB 6	
Display Clear	0	0	0	0	0	0	0	0	0	1	Clear display dan kursor pada Add 0
Cursor home	0	0	0	0	0	0	0	0	1	X	Kursor ke Add 0
Entry mode Set	0	0	0	0	0	0	0		I/D	S	Pemakaian mode pd LCD
Display ON/OFF	0	0	0	0	0	0	1	D	C	B	Menset tampilan display
Cursor/displa y Shift	0	0	0	0	0	1	S/C	R/L	X	X	Gerakan kursor tanpa merubah DD

											RAM
Fuction Set	0	0	0	0	1	DL	1	X	X	X	Untuk menset data lebar yangakan digunakan
CG RAM Address set	0	0	0	ACG							Digunakan untuk pengisian CG RAM
DD RAM Address set	0	0	1	ADD							Untuk pengisian DD Ram
Tlis data ke CG RAM	1	0	DATA								Perintah untuk Menulis data dan CG atau DD RAM
Baca data dari CG atau DD RAM	1	1	DATA								Perintah untuk membaca data dan CG atau DD RAM

(Sumber: Module User Manual)

ACG :CG RAM Address

ADD : DD RAM Addess

I/D = 1 : Increment

I/D = 0 : decrement

S = 1 : Display Shift

S = 0 : NO display Shift :

D = 1 : Display on

D = 1 : Display Off

C = 1 : Cursor On

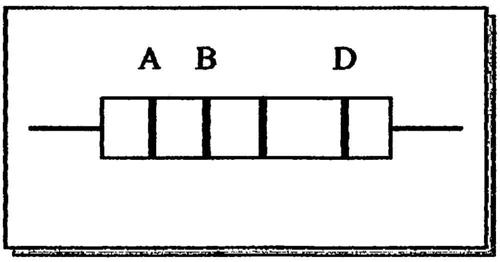
C = 0 : Cursor Off

B = 1 : Blink On

B = 0	: Blink Off
S/C = 1	: Display Shift
S/C = 1	:Cursor Movement
R/L = 1	: Right Shift
R/L = 0	: Left Shift
DL = 1	: 8 Bit data
DL = 0	: 4 Bit data

2.6. Resistor

Resistor merupakan komponen positif yang dibuat untuk mendapatkan suatu hambatan tertentu. Resistor yang paling banyak digunakan terbuat dari karbon yang dilapiskan pada sebatang keramik.resistor semacam ini disebut resistor film karbon. Resistor karbon menggunakan sandi warna yang dicat pada bahan resistor resistor untuk menyatakan nilai hambatan.



Gambar 2-12
Ring Sandi Pada Resistor
(Sumber : Drs. Ridwan Rusli, Teknik Elektronika, Hal.5)

Tabel 2-5
Kode Warna Resistor

Warna	Satuan	Puluhan	Pengali	Toleransi
Hitam	0	-	1	-
Coklat	1	1	10	-
Merah	2	2	100	-
Jingga	3	3	1000	-
Kuning	4	4	10000	-
Hijau	5	5	100000	-
Biru	6	6	1000000	-
Ungu	7	7	10000000	-
Abu-abu	8	8	100000000	-
Putih	9	9	1000000000	-
Perak	-	-	0,01	10%
Emas	-	-	0,1	5%

(Sumber : Drs. Ridwan Rusli, Teknik Elektronika Hal. 7)

Resistor dibuat dengan ukuran badan yang mencerminkan kemampuan bertahan terhadap daya lesap yang diterima jika dialiri arus listrik. Suatu resistor dengan hambatan (R) yang dialiri arus listrik arus (I) akan menerima daya lesap $P = I^2 \times R$. Daya ini akan menaikkan suhu resistor dan jika melebihi kemampuan daya (power rating) yang dihasilkan dapat menyebabkan kerusakan yang permanenberupa perubahan nilai hambatan ataupun membuat resistor menjadi hangus.

Rumus dari resistor adalah sebagai berikut:

Hubungan seri: $R_{total} = R_1 + R_2 + R_3 + \ldots\ldots + R_n$ ....(2.3)

Hubungan parallel: $1/R_{total} = 1/R_1 + 1/R_2 + 1/R_3 + \ldots\ldots + 1/R_n$ ....(2.4)

2.7. Kristal

Dari beberapa jenis kristal yang ditemukan di alam menunjukkan *efek piezoelektrik*, bila dalam penerapannya tegangan AC melintasi bahan-bahan ini maka kristal tersebut bergetar dengan frekuensi yang sama dengan frekuensi tegangan yang diterapkan. Sebaliknya bila dipaksa untuk bergetar, maka akan membangkitkan tegangan AC. Bahan utama yang dapat menimbulkan efek piezoelektrik ini adalah kuarsa, garam Rochelle dan turnalin.

Kuarsa merupakan kompromi diantara perilaku piezoelektrik dari garam Rochelle dan kekuatan dari turmalin. Karena harganya yang murah dan telah tersedia di alam, kuarsa banyak digunakan pada osilator RF dan penapis. Kristal hampir selalu dipotong dan dibuat untuk bergetar paling baik pada salah satu frekuensi resonansinya, yang biasanya merupakan frekuensi dasar atau frekuensi yang terendah. Frekuensi-frekuensi yang lebih tinggi, yang disebut nada-nada tambahan hampir merupakan hasil perbanyakan yang tepat dari frekuensi dasarnya.

Rumus untuk frekuensi dasar dari sebuah kristal adalah:

$$F = \frac{K}{t} \qquad (2.10)$$

Dimana : K = tetapan yang tergantung pada jenis potongan

t = ketebalan kristal.

Gambar 2-13

Simbol Kristal

(Sumber : Teknik Elektronika)

BAB III

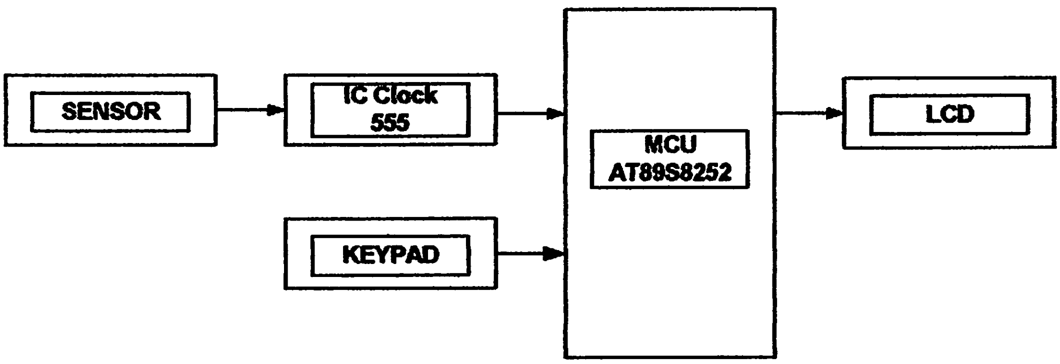
PERENCANAAN DAN PEMBUATAN ALAT

3.1 Umum

Dalam BAB ini kita akan membahas tentang bagaimana cara perancanaan dan pembuatan alat pengukur Berat emas berbasis Mikrokontroller AT89S8252. perencanaan dibagi menjadi 2 bagian pokok yaitu bagian hardware dan software. Dan secara garis besar blok diagram dari keseluruhan rangkaian hardwarenya adalah sebagai berikut.

3.2. Dasar Perencanaan Hardware

Blok Diagram Perangkat Keras adalah sebagai beikut:



Gambar 3-1

Diagram Blok Minimum Sistem

Cara kerja dari masing-masing Blok

1. Keypad

   Berfungsi untuk masukan data base untuk mikrokontroller AT89S8252

2. Sensor

   Sensor yang kita gunakan adalah berjenis capasitif sebagai masukan data dari beban yang akan ditimbang.

3. IC Clock

   Berfungsi sebagai pembangkit frekuensi dari perubahan sensor kapasitif menggunakan ICLM555

4. MCU AT89S8252

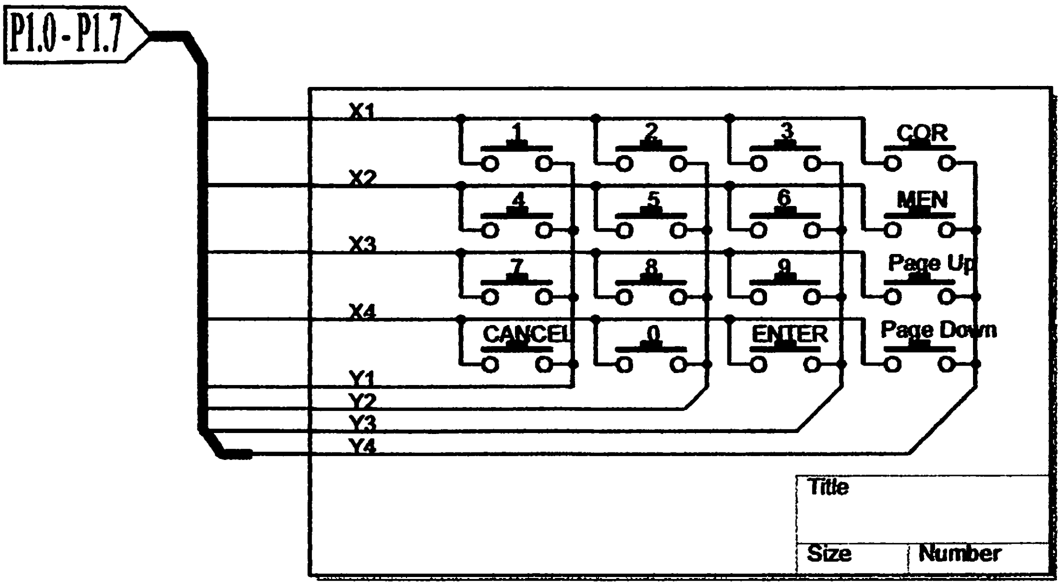
   Mengolah semua masukan (Keypad, Sensor Capasitif), menjadi keluaran (LCD)

5. LCD (Liquid Crystal Display)

   Untuk menampilkan karakter baik angka, huruf atau simbol sesuai dengan yang kita inginkan.

3.2.1. Rangkaian KeyPad

Keypad berfungsi untuk memasukan input data dari mikrokontroler. rangkaian keypad menggunakan keypad 4x4 yaitu 12 buah saklar tekan (push bottom) yang dirangkai dalam bentuk matrik. Rangkaian keypad dihubungkan langsung ke mikrontroler pin 1, 2 dan 3 dipergunakan sebagai scaning sedangkan pin 4, 5, 6 dan 7 dipergunakan sebagai data hasil penekanan keypad proses scaning dari penekanan keypad ditujukan pada table 3-1 gambar rangkaian keypad ditunjukan pada gambar berikut :



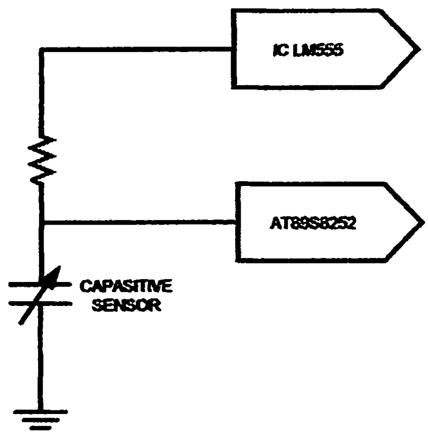
Gambar 3-2

Rangkaian Keypad

Untuk 4 bagian kolom yaitu row / Y dan 4 bagian baris adalah col / X, system kerjanya yaitu salah satu pin misalnya X1 terhubung dengan Y1 maka data outputnya akan "1" sedangkan untuk X1 dan Y2 data outputnya akan "2", dari rangkaian diatas dapat diperoleh 16 kemungkinan output.

3.2.2. Rangkaian Sensor

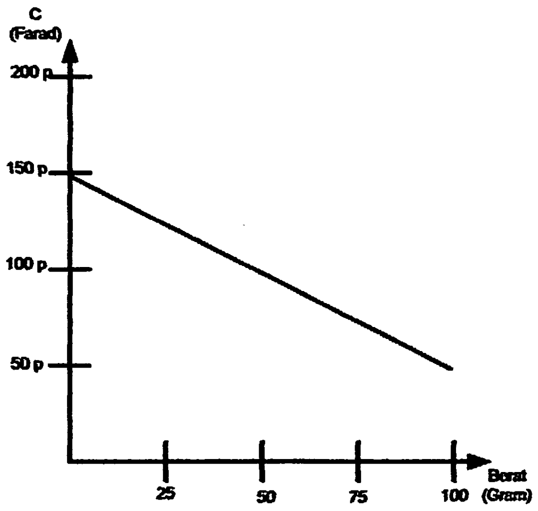
Mikrokontroller mendeteksi beban dengan melihat perbandingan antara resistor dan capasitor yang kita pasangkan untuk lebih jelasnya kita lihat gambar dibawan ini :



Gambar 3-3
Rangkaian Sensor

Mikrokontroller AT89S8252 mendeteksi adanya perbedaan frekwensi yang ditimbulkan oleh nilai kapasitif yang berubah-ubah yang nilainya antara 50 sampai dengan 150 pF. Karena adanya pembanding antara Resistor dengan kapasitif maka IC Cock LM555 bekerja sebagai pembangkit frekuensi. Masukan untuk Mikrokontroller AT89S8252 membaca berapa besarnya frekuensi dalam satu satuan waktu itulah yang akan ditampikan pada LCD.

Gambar grafik dibawah ini menunjukkan Hubungan parameter berat dan sensor.



Grafik 3-1

Hubungan Parameter Berat dan Sensor

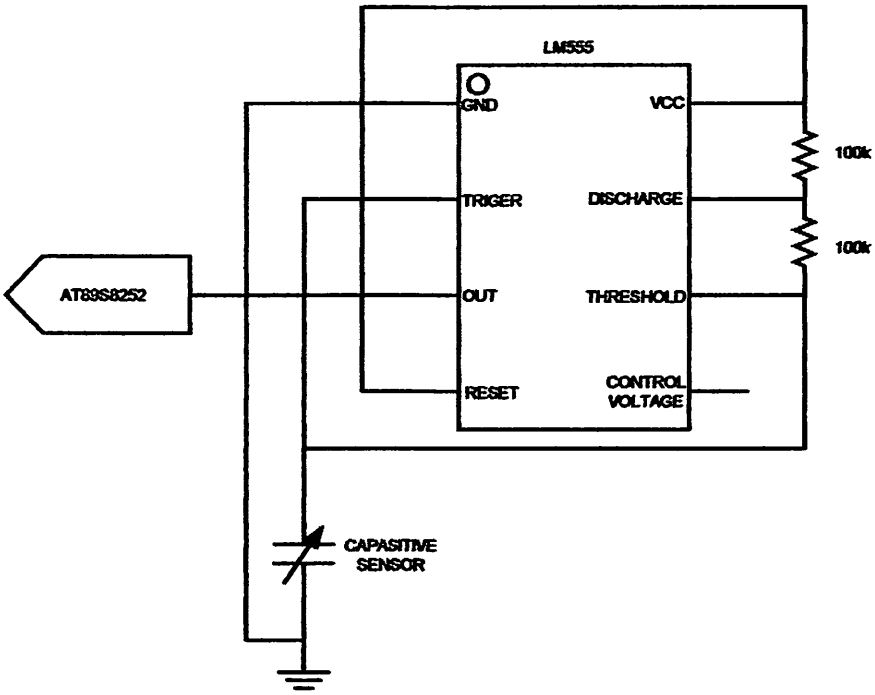
Tabel 3-1

Hubungan Parameter Berat dan Sensor

No	Berat (Gram)	Kapasitif (Farad)
1	0	150 p
2	25	125 p
3	50	100 p
4	75	75 p
5	100	50 p

3.2.3. Rangkaian Pengkondisi Sinyal LM555

IC ini biasa difunakan untuk mengolah atau membangkitkan frekuensi (Osilator) bisa juga digunakan untuk menentukan waktu (Timers). Mempunyai tegangan sumber 200mA serta kompatibel untuk dipakai bersama mikrokontroller atau IC TTL, mempunyai temperatur untuk kestabilan bekerja 0,005% per ^{0}C. tingkat perhitungannya adalah sampai dengan mikroseconds. IC 555 adalah kumpulan dari transistor logika. Untuk lebih jelasnya kita lihat skematik diagram dari IC LM555



Gambar 3-4

Rangkaian pengkondisi sinyal IC LM555

Nilai kapasitor pada rangkaian pembangkit frekuensi dengan IC LM555

Semakin besar nilai kapasitif yang ada maka semakin rendah frekuensinya

Frekuensi $(f) = \dfrac{1{,}44}{R1x2R2xC}$

Apabila diketahui R1 = 100 KΩ

R2 = 100 KΩ

Misal nilai C = 50 pF

Maka

Frekuensi $(f) = \dfrac{1{,}44}{100x2x100x0{,}00000000005}$

$= \dfrac{1{,}44}{0{,}000001}$

$= 1.440.000$ Hz

$= 1,44$ Mhz

Misal nilai C = 100 pF

Maka

$$\text{Frekuensi } (f) = \frac{1,44}{100x2x100x0,0000000001}$$

$$= \frac{1,44}{0,000002}$$

$= 720.000$ Hz

$= 720$ Khz

Misal nilai C = 150 pF

Maka

$$\text{Frekuensi } (f) = \frac{1,44}{100x2x100x0,00000000015}$$

$$= \frac{1,44}{0,000003}$$

$= 480.000$ Hz

$= 480$ Khz

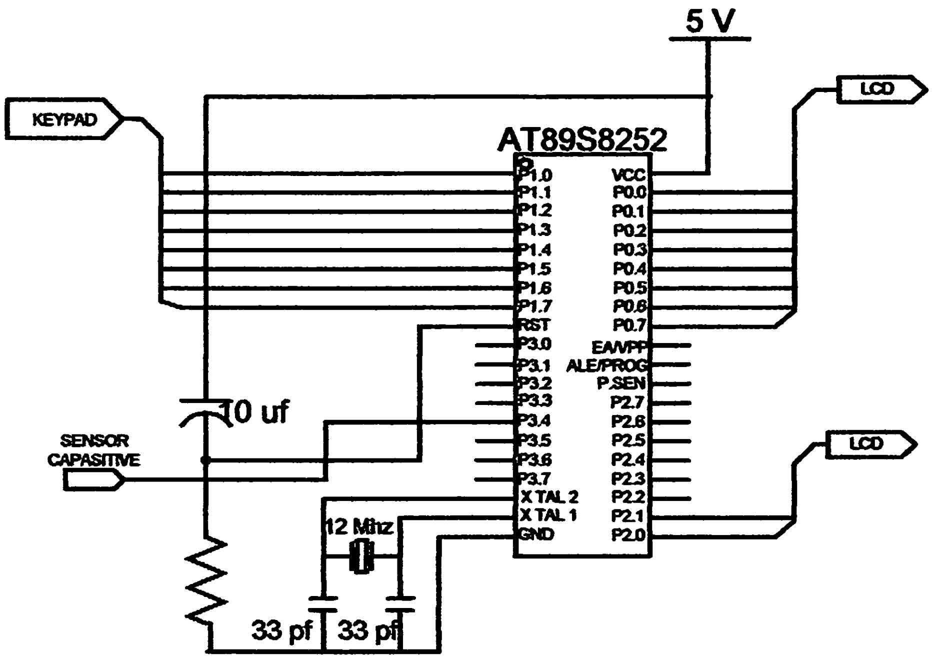
Tabel 3-2

Hubungan Antara Kapasitansi dan Frekuensi

No	Nilai R1 & R2	Nilai C	Hasil Perhitungan
1	100 KΩ & 100 KΩ	50 pF	1,44 Mhz
2	100 KΩ & 100 KΩ	100 pF	720 Khz
3	100 KΩ & 100 KΩ	150 pF	480 Khz

3.2.4. Rangkaian Mikorkontroller AT89S8252

Minimum sistem yang dirancang menggunakan mikrokontroler AT89S8252 sebagai prosesornya. Minimum sistem AT89S8252 disini dirancang untuk menggunakan memori internal yang sudah tersedia dimikrokontroler. Untuk mengaktifkan memori internalnya maka pin EA pada kaki 31 dihubungkan ke Vcc. Mapping dari minimum system tersebut, untuk alamat 0000H sampai dengan 017FH ditempati oleh internal sebagai penyimpan program yang dirancang.

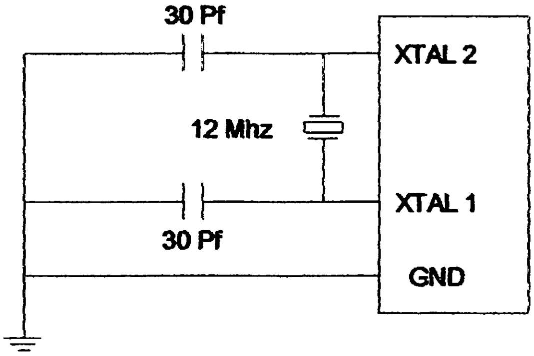


Gambar 3-5
Rangkaian Mikrokontroller

3.2.5. Rangkaian Clock Internal

Semua keluarga MCS-51 mempunyai clock (rangkaian osilator) didalam chip nya sendiri yangdisebut on-chip osilator. Cara mengkases clock internal yang terdapat pada chip mikrokontroler yaitu sebuah kristal pada pin pin XTAL 1 dan pin XTAL 2 dengan dua buah kapasitor yang masing – masing dihubungkan ke kaki kristal dan dihubungkan ke ground.

Pemindahan frekwensi kristal berdasarkan akses mikrokontroler untuk untuk serial interface, kristal yang digunakan adalah kristal 11,0592 MHz dengan ketentuan pada data sheet adalah sebesar 30 pF. Untuk gambar rangkaian clock dari mikrokontroler AT89S8252 ditunjukan pada gambar berikut :



Gambar 3-6
Rangkaian Clock

Untuk nilai kapasitor yang digunakan adalah sebesar 30 pf samapai dengan 10 pF untuk C1 atau C2Dengan demikian perhitungannya dapat dilihat sebagai berikut :

F = 12 Mhz

$$T = \frac{1}{f}$$

Sehingga $\frac{1}{12x10^6} = \frac{1}{12}$ µs

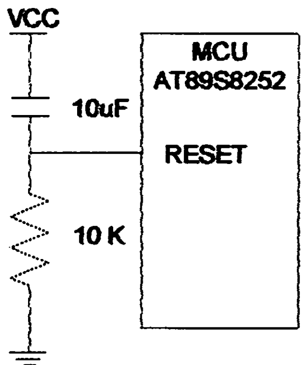
Maka untuk satu siklus mesin dari mikrokontroller adalah sebesar :

Tme – 12 x T

$$Tme = 12 \times \frac{1}{12}\ \mu s \qquad \text{Jadi} \quad Tme = 1\ \mu s$$

3.2.6. Rangkaian Reset

Rangakaian reset digunakan untuk mereset atau mengembalikan keadaan awal dari mikrokontroler AT89S8252. rangkaian ini dipergunakan untuk mereset mikrokontroler pada keadaan pertama kali saat power diaktifkan atau disebut power on reset. Untuk menjalankan reset maka pin reset (pin no 9) pada mikrokontroler diberi snyal high (1). Gambar rangkaian reset dapat ditunjukan pada gambar berikut :



Gambar 3-7
Rangkaian Reset

Besarnya nilai tahanan dan kapasitor pada rangkaian reset akan menentukan waktu lama pulsa reset.

Dengan rumus : $t = R \times C$

Agar reset dapat terjadi secara normal maka nilai t harus lebih besar dari 30 siklus mesin.

T >> 30 x Tme

Karena nilai Tme diatas adalah 1 μs, maka :

T >> 30 x 1μs

T >> 30 μs

Dengan mengambil nilai R dan C sebesar 10 KΩ dan 10 μF maka besarnya t dapat dicari dengan rumus sebagai berikut :

$T = 10\ K\Omega \times 10\ \mu F \quad = (10 \times 10^{3}) \times (10 \times 10^{-6})$

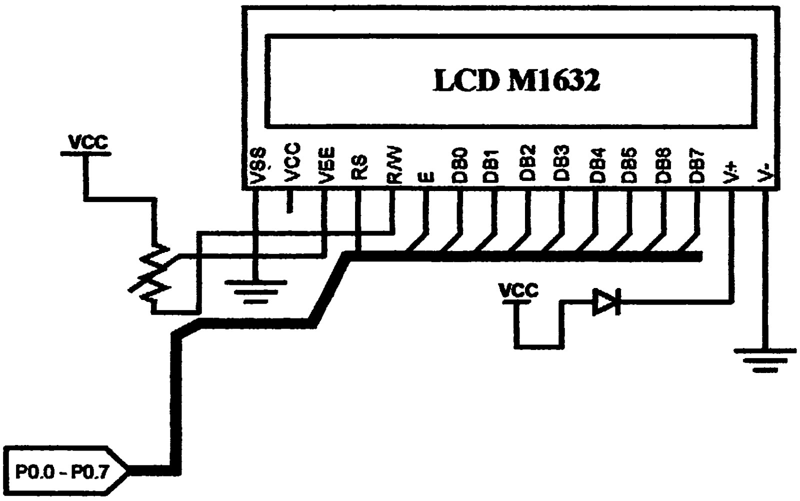
$= 100 \times 10^{-3}$

= 0,1 second

Dengan demikian nilai "t" jauh lebih besar dibanding nilai minimalnya

3.2.7. Rangkaian Display LCD

Sebagai tampilan dari petunjuk penggunaan dari pemasukan pasword dan keadaan pintu digunakan display LCD dot matrik 2 x 16 karakter. Sinyal-sinyal yang dipergunakan oleh LCD adalah data bus, RS, R/W dan E. sinyal E dihubungkan ke port 3.5 untuk mengaktifkan LCD. LCD akan aktif jika mikrokontroler memberikan intruksi tulis pada alamat LCD. Sedangkan P3.4 dipergunakan untuk memberikan sinyal RS yang membedakan data yang diberikan pada LCD. Sinyal RS diberikan ke LCD untuk membedakan sinyal antara intruksi program atau intruksi penulisan data. Untuk pin R/W akan berlogika Low (0) apabila dihubungkan dengan ground maka LCD difungsikan hanya untuk menuliskan program atau data ke display. Untuk mengambil data dari mikrokontroler maka pin –pin data dihubungkan dengan P0.0 samapi P0.7 yang merupakan pin-pin data dari mikrokontroler.



Gambar 3-8

Rangkaian Display LCD

VR1 pada pin 3 (VEE) digunakan untuk mengatur contras dari karakter yang ditampilkan, sedangkan pada pin 15 (V+) diberi sebuah diode (D6) gunanya adalah agar tegangan yang masuk dengan data sheet yaitu sebesar 4,5V maksimal.

Tegangan Dioda = 0,6V

VCC = 5V

Jadi tegangan yang masuk = 5 – 0,6 = 4,4V

3.3 Perancangan Perangkat Lunak

3.3.1. Perangkat Lunak AT89S8252

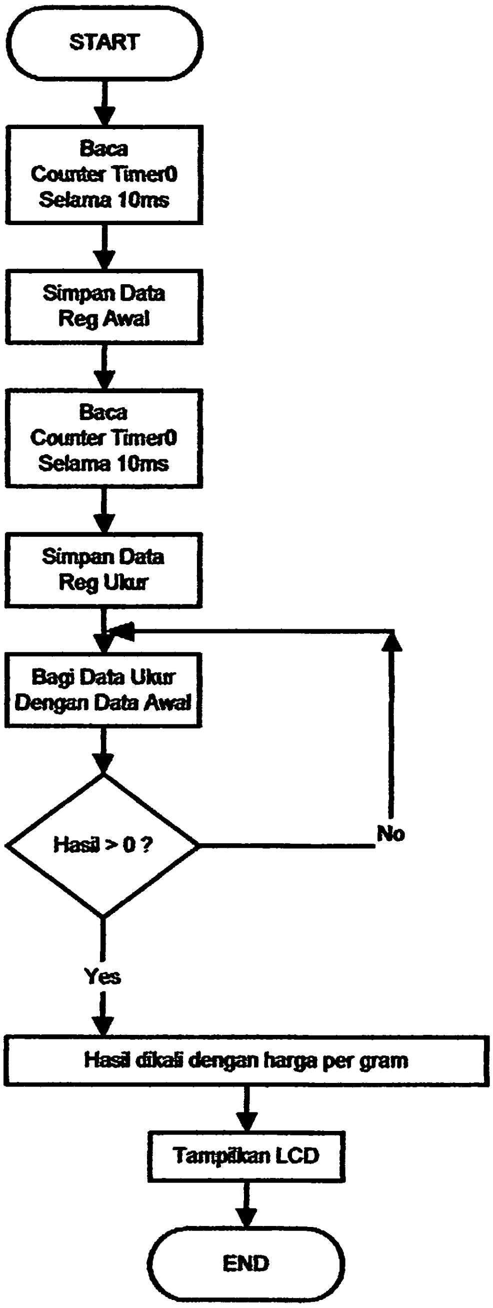
Perangkat lunak yang digunakan unuk AT89S8252 ini adalah menggunakan bahasa assembly keluarga MCC51. program yang ditulis dengan bahasa assembly terdiri dari label kode numeric dan lain sebagianya, pada umumnya dinamakan sebagai program sumber (source Code) yang belum bisa diterima oleh prosesor untuk dijalankan seagi program tapi harus diterjemahkan dulu menjadi bahasa mesin dalam bentuk kode biner.

Program sumber dibuat dengan program editor biasa, misalnya notepad pada windows, selanjutnya program sumber diterjemahkan (Compille) ke bahasa mesin dengan menggunakan compiler MCS51. Hasil kerja dari program tersebut adalah file "asm" dan diubah menjadi file-file dengan extension "hex", "Oj", "Lst", dan "Bin".

File yang berektension "Bin", berisikan kode-kode bahasa mesin, kode-kode bahasa mesin inilah yang diumpankan ke memori program (ROM). Dalam dunia mikrokontroler biasanya file ini diisikan ke UV EPROM, dan khusus untuk mikrokontroler buatan atmel, program ini diisikan ke dalam Flash PEROM yang ada didalam chip AT89S8252.

Assembly Listing merpkan naskah yang berasal dari program sumber, dalam naskah tersebut pada bagian sebelah kanan / kiri setiap baris program sumber diberi tambahan hasil program assembler. Tambahan tersebut berupa nomor memori program berikut dengan kode-kode yang akan diisikan pada memori program bersangkutan. file ini sangat berguna untuk dokumentasi dan sarana untuk menulusuri program yang ditulis apabila terjadi kesalahan.

Perlu diperhatikan adalah setiap prosesor mempunyai kontruksi yang berbeda, intruksi untuk mengendalikan masing-masing prosesor juga berlainan dengan demikian bahasa assembly untuk masing-masing prosesor juga berbeda yang sama hanyalah pola dasar cara penulisan program assembly saja.



Gambar 3-9

Flow Chard dari MCU 89S8252

BAB IV

PENGUJIAN ALAT

4.1. Prinsip Kerja Alat.

Alat ini bekerja jika ada beban yang dibaca oleh sensor, Sebagai sensor untuk menentukan berat beban adalah sensor capasitif dimana sensor ini bekerja dengan cara yang sama dengan cara kerja kapasitor.

Dalam rangka pengujian alat tersebut, Pada bab ini akan di uraikan sejumlah pengukuran dan percobaan yang dilakukan untuk mengetahui unjuk kerja alat tersebut secara keseluruhan . Bagian-bagian yang diuji adalah

1. Pengujian Sensor
2. Pengujian IC Clock LM555
3. Pengujian Keypad
4. Pengujian LCD dan Mikrokontroller AT89S8252 (Minimum Sistem)

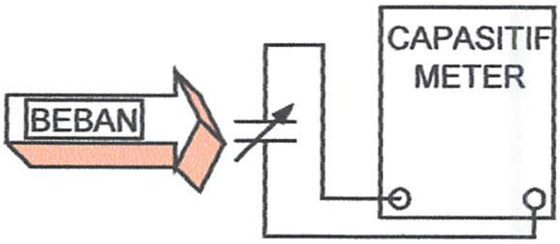
4.2. Pengujian Sensor

Tujuan pengujian sensor ini adalah untuk mengetahui apakah sensor benar-benar bisa bekerja dengan baik dan sesuai dengan yang kita rencanakan, yaitu sebagai sinyal masukan untuk mikrokontroller.

Komponen yang kita butuhkan untuk pengujian sensor adalah sebagai berikut:

1. Sensor kapasitif
2. Kapasitif Meter

Rangkaian untuk menguji sensor dapat kita lihat pada gambar 4-1



Gambar 4-1

Rangkaian Pengujian Sensor kapasitif

Tabel 4-1

Hasil Pengujian Sensor

No	Berat (Gram)	Kapasitif (Farad)
1	0	150 p
2	25	125 p
3	50	100 p
4	75	75 p
5	100	50 p

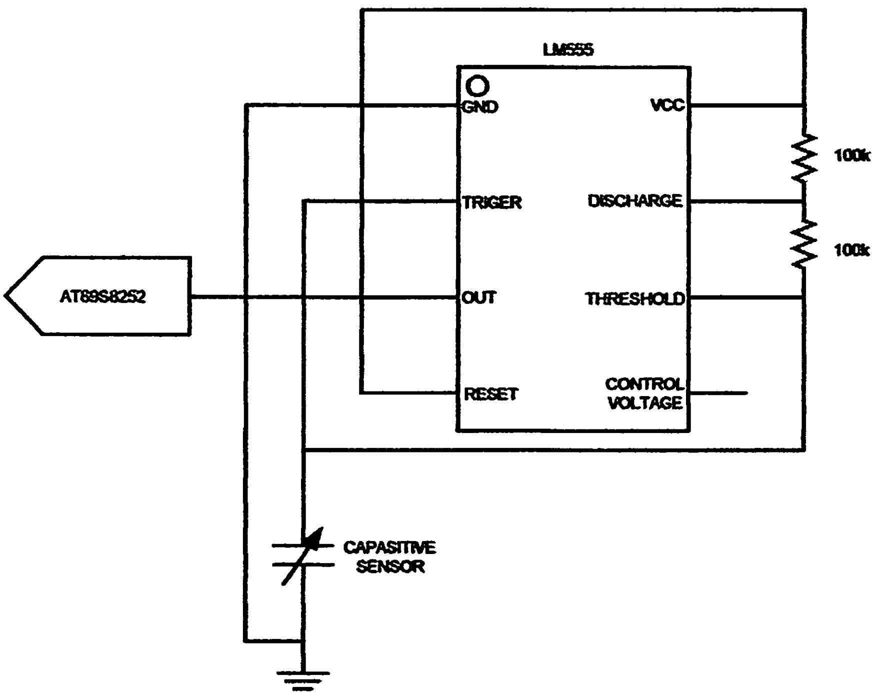
4.3. Pengujian IC Clock LM555

Rangkaian pengujian IC LM555 ini dapat dilihat pada gambar 4-2, dari gambar tersebut dapat kita ketahui bahwa komponen yang kita pakai untuk menguji sensor adalah :

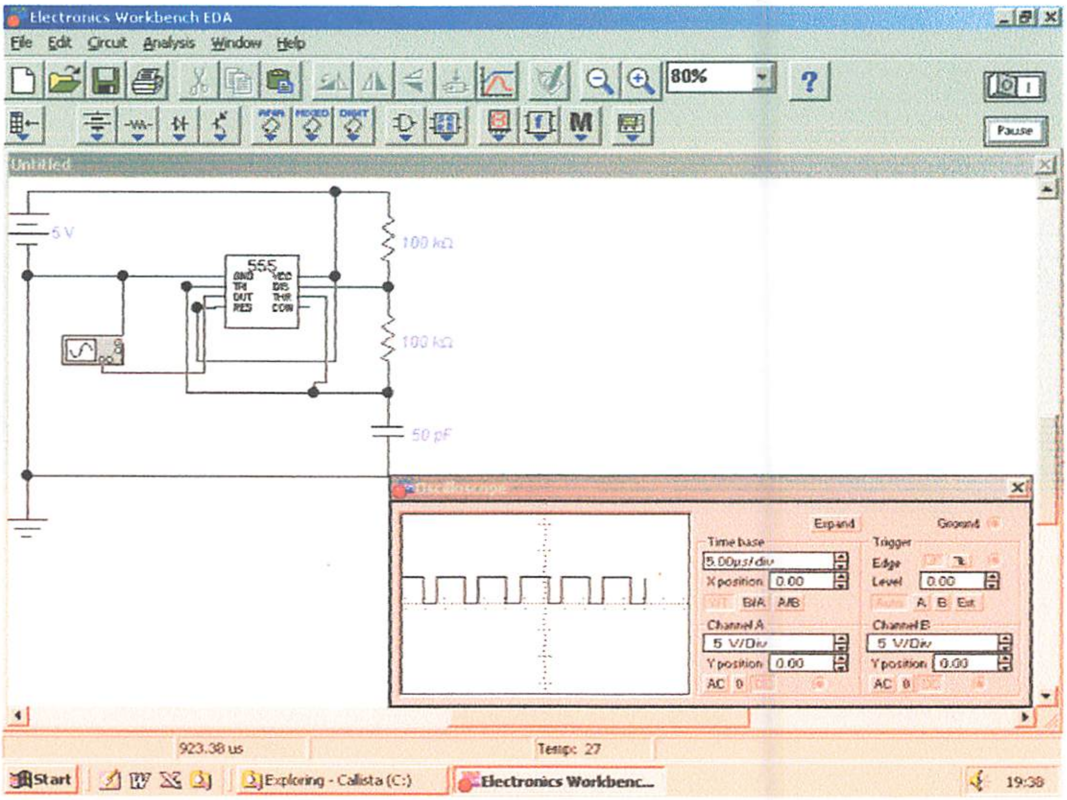
- Osciloscope
- Power Supply
- Sensor capasitif pada IC555

Langkah-Langkah pengujian adalah sebagai berikut:

- Mengatur saklar pada Osciloscope supaya dapat membaca frekwensi.
- Mengamati dan mencatat hasil pengujian, hasil pengujian dapat kita lihat pada tabel 4-2
- Membuat analisa apakah nantinya sensor ini dapat bekerja dengan baik.



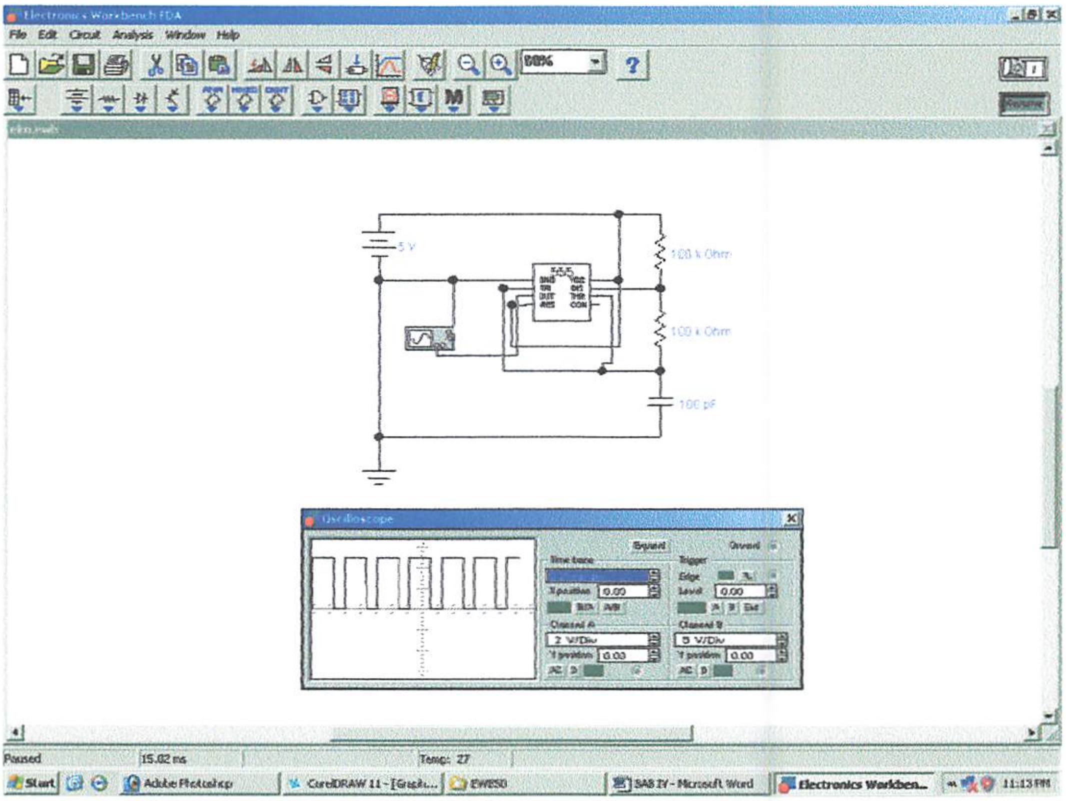
Gambar 4-2
Rangkaian Pengujian IC Clock LM555



Gambar 4-3

Hasil Pengujian IC Clock LM555 berkapasitansi 50pF

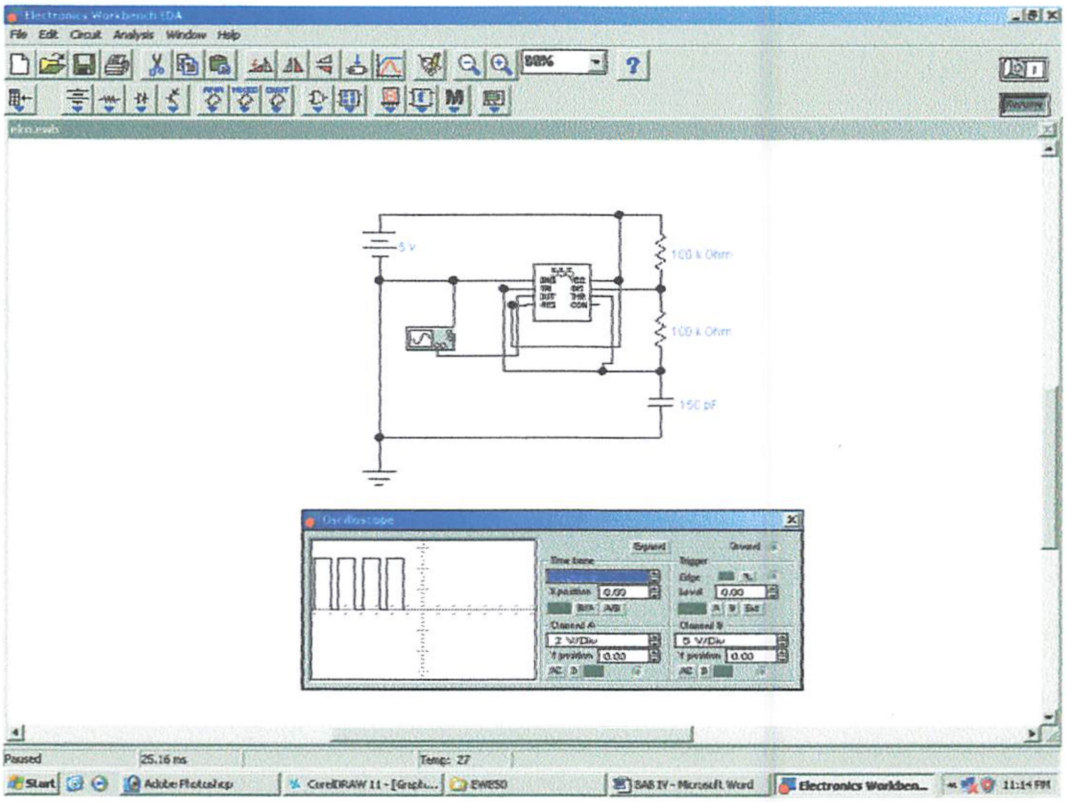
Dengan menggunakan program EWB



Gambar 4-4

Hasil Pengujian IC Clock LM555 berkapasitansi 100pF

Dengan menggunakan program EWB



Gambar 4-5

Hasil Pengujian IC Clock LM555 berkapasitansi 150pF

Dengan menggunakan program EWB

Tabel 4-2

Hasil Pengujian IC LM555

No	IC LM555 Dengan Menggunakan Resistor 100K Ohm dan nilai kapasitansinya adalah	Hasil yang diperoleh (Time/Div)	Hasil yang diperoleh (Volt/Div)
1	50 pF	5.00 μS/div	5 V/div
2	100 pF	0.01 mS/div	2 V/div
3	150 pF	0.02 mS/div	2 V/div

Dari Tabel 4-2 dapat kita peroleh bahwa IC Clock LM555 yang kita rencanakan sudah berjalan, sensor juga bekerja dengan baik.

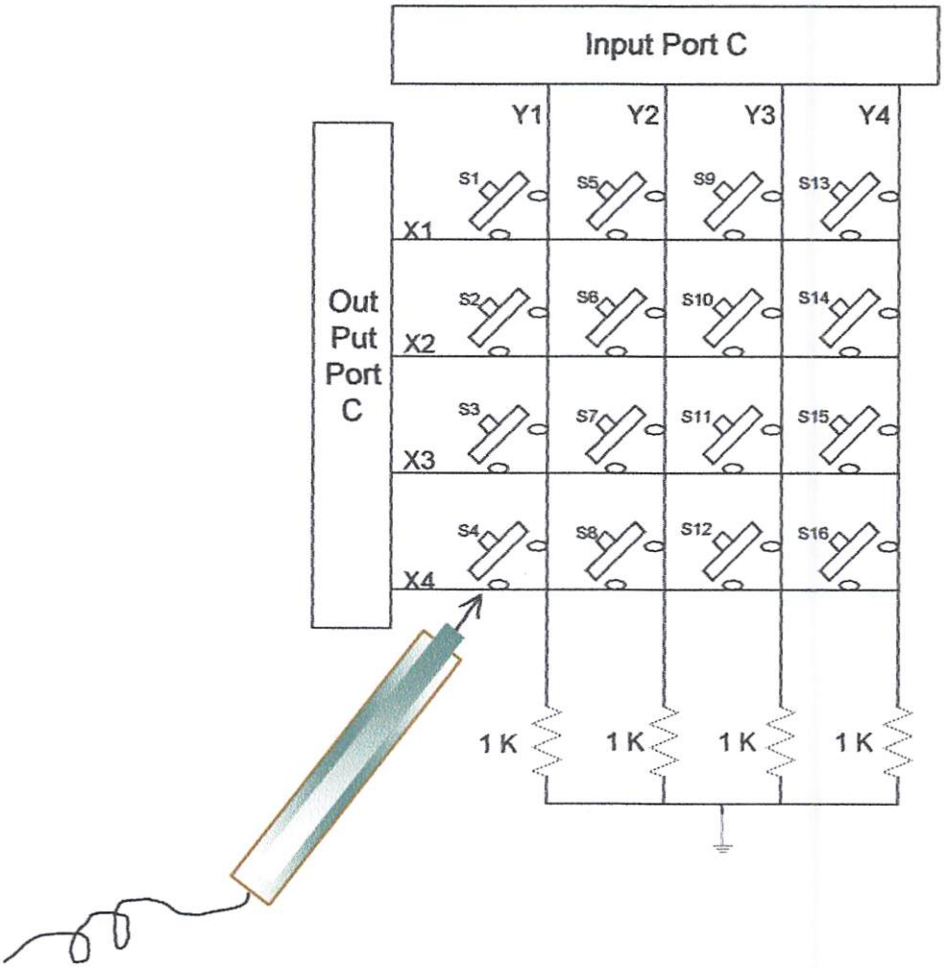
4.4. Pengujian Papan Tombol (*keypad*)

Pengujian ini bertujuan untuk mengetahui konfigurasi logika keluaran dari unit papan tombol saat tombol ditekan. Peralatan yang dipergunakan antara lain catu daya, unit papan tombol, dan *logic probe*. Dalam pengujian ini keluaran yang diamati adalah proses *scanning* yang terjadi pada lajur baris dan kolom. Lajur baris merupakan bagian output sedangkan lajur kolom merupakan bagian input. Untuk mengetahui kebenaran rangkaian keypad yang telah dibuat maka keluaran dari rangkaian keypad ini akan ditampilkan ke port 1 MCU 89C51.

Langkah-langkah pengujian papan tombol adalah sebagai berikut ;

- ♣ Menyiapkan catu daya dengan keluaran 5 V DC, rangkaian papan tombol seperti dalam bab 3 dan *logic probe*.
- ♣ Menyusun rangkaian pengujian papan tombol seperti terlihat dalam Gambar 4-6 serta memastikan bahwa hubungan antar pin pada masing-masing saklar telah benar.
- ♣ Jalankan program pengujian keypad, amati keluaran pin Port C bagian output. Langkah ini dilakukan dalam keadaan tidak ada penekanan tombol sama sekali.
- ♣ Tekan sembarang tombol kemudian amati keluaran pin Port C bagian output.

Hasil dari pengujian rangkaian papan tombol terdapat dalam Tabel 4-3



Gambar 4-6

Pengujian rangkaian Keypad

Tabel 4-3

Hasil Pengujian Papan Tombol.

Input Tombol yang ditekan		Output Port 1			
Nomor tombol	Definisi tombol	D	C	B	A
-	-	X	X	X	X
(S1)	1	0	0	0	1
(S2)	4	0	1	0	0
(S3)	7	0	1	1	1
(S4)	ESC	1	0	1	0
(S5)	2	0	0	1	0
(S6)	5	0	1	0	1
(S7)	8	1	0	0	0
(S8)	0	0	0	0	0
(S9)	3	0	0	1	1
(S10)	6	0	1	1	0
(S11)	9	1	0	0	1
(S12)	OK	1	0	1	1
(S13)	F1	1	1	0	0
(S14)	F2	1	1	0	1
(S15)	F3	1	1	1	0
(S16)	F4	1	1	1	1

Dari hasil pengujian, didapatkan data seperti dalam Tabel 4-3 maka dapat diketahui bahwa saat tombol ditekan maka keluaran port 1 mikrokontroler 89S8252 akan berlogika sesuai dengan tombol yang ditekan. Hasil pengujian dalam Tabel 4-3 terlihat bahwa rangkaian papan tombol yang telah direalisasikan sesuai dengan unjuk kerja perencanaan.

4.5. Pengujian Mikrokontroller AT89S8252 (Minimum Sistem)

Tujuan dari pengujian Mikrokontroler AT89S8252 adalah untuk mengetahui apakah Mikrokontroller AT898252 dapat berfungsi dengan baik, sesuai dengan yang telah kita rencanakan, yaitu :

1. Dapat menerima sinyal masukan dari rangkaian sensor.
2. Dapat Mengolah sinyal dari rangkaian sensor penerima untuk selanjutnya dapat ditapilkan melalui output yang telah kita rencanakan dan yang kita buat yaitu berupa LCD.
3. Dapat menampilkan sinyal keluaran berupa LCD.

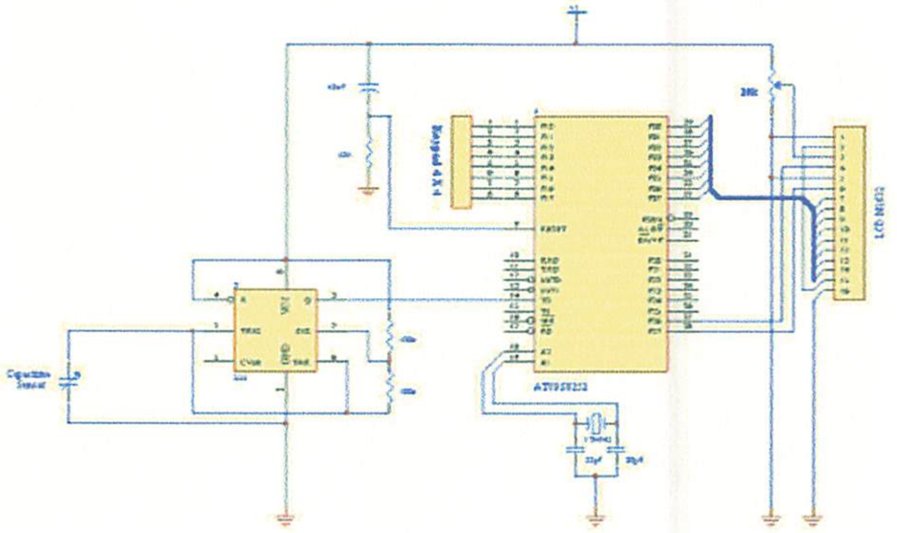
Rangkaian pengujian Mikrokontroller AT89S8252 dapat dilihat pada gambar 4-7 Dari gambar tersebut dapat dilihat bahwa komponen yang digunakan dalam pengujian adalah :

- Rangkaian Sensor
- Mikrokontroller AT89S8252
- LM555
- Keypad

♣ LCD M1632

♣ Kapasitif Sensor

♣ Resistor



Gambar 4-7

Rangkaian Pengujian Mikrokontroller AT89S8252

Langkah-langkah pengujian adalah sebagai berikut

♣ Membuat rangkaian seperti gambar 4-7

♣ Membuat program dan diisikan pada internal flash memory microcontroller AT89S8252. Flow chart dari program pengujian Sistem Minimum dapat dilihat pada gambar 3-9

♣ Menyalakan Power Suply

♣ Mengamati apakah sesuai dengan yang kita rencanakan

♣ Membuat analisa apakah alat ini bekerja dengan baik

Tabel 4 - 4

Pengujian Minimum Sistem (Mikrokontroller AT89S8252)

Yang direncanakan	**Hasil yang diperoleh.**
AT89S8252 apabila dicompille tidak ada pesan error (No Error Found) dan Compillenya berhasil (Compille Success)	tidak ada pesan error dan compille berhasil dengan baik.

Dari Tabel 4-4 dapat kita ketahui bahwa mikrokontroller dapat bekerja dengan baik sesuai dengan yang kita rencanakan yaitu mikrokontroller dapat membaca sensor dan mengeluarkan karakter pada LCD sesuai dengan yang kita rencanakan.

4.6. Spesifikasi Alat

1. Mikrokontroller AT89S8252 sebagai pengolah data masukan menjadi data keluaran IC7805 Sebagai Regulator Rangkaian
2. LCD M1632
3. Keypad 4 x 4
4. IC 555 Sebagai Counter (pembangkit frekuensi)
5. Kapasitif sensor

4.7. Pengujian sistem Keseluruhan

Tujuan dari pengujian sistem secara keseluruhan adalah untuk mengetahui cara kerja piranti setelah perangkat keras dan perangkat lunak diintegrasikan bersama-sama. Pengujian sistem secara keseluruhan diuji atas beberapa tahap berdasarkan tampilan menu dan mengikuti diagram alir atau flowchard dalam perencanaan pada BAB III.

Tahap-tahap pengujian sistem secara keseluruhan adalah sebagai berikut :

- Menyiapkan piranti dan memastikan bahwa catu daya telah terpasang dengan benar.
- Memasang sensor pada tempat yang telah kita siapkan
- Menyalakan Rangkaian yang telah kita pasang sensor.
- Melihat LCD perkembangan penunjukan berat jika Sensor tidak diberi beban, dengan beban. Penunjukan pada LCD Apakah sesuai dengan beban yang telah kita berikan

LCD mengeluarkan karakter sesuai dengan yang kita inginkan dan sensor bekerja dengan baik sesuai dengan beban yang telah kita berikan pada sensor.

Cara Pengkalibrasian alat

Kalibrasi adalah penyesuaian alat kita dengan keadaan yang sebenarnya dan yang akan kita lakukan ada beberapa Langkah yaitu :

1. Dicoba dengan beban 10 gram

a. Jika kurang dari 10 gram maka waktu sampling counter timer diperpanjang.

b. Jika lebih dari 10 gram maka waktu sampling counter timer diperpendek.

2. Dicoba dengan beban 50 gram

a. Jika kurang dari 50 gram maka waktu sampling counter timer diperpanjang.

b. Jika lebih dari 50 gram maka waktu sampling counter timer diperpendek.

3. Apabila dicoba dengan beban yang lain dan ternyata tidak linier maka dibuat rumus tertentu agar hasil menjadi linier.

4. Membandingkan timbangan yang telah kita buat dengan timbangan yang sesungguhnya.

Dan hasil pengujian antara alat yang telah kita buat dengan timbangan yang sebenarnya adalah :

Tabel 4-5

Perbandingan Alat yang kita buat dan Timbangan yang sebenarnya

Berat (Gram)	Data Timbangan yang sebenarnya (Gram)	Data Alat yang kita buat (Gram)
0	0	0
25	25	24
50	50	48

75	75	76
100	100	98

4.8. Kesalahan Relatif Data

Kesalahan relatif rata-rata akan menjadikan tendensi pada setiap hasil pengukuran yang dilakukan. Oleh sebab itu untuk mencari kesalahan relatif tiap data yang diambil maka dipakai rumus :

$$Kr = \frac{|X - \overline{X}|}{\overline{X}} \times 100\,\%$$

Dimana :

Kr = kesalahan relatif

X = nilai yang sebenarnya

$\overline{X}$ = nilai yang diperoleh dari pengukuran

Sebagai contoh hasil pengujian saat pengukuran pada relay, maka didapat:

$$Kr = \frac{X - \overline{X}}{|\ \overline{X}\ |} \times 100\,\%$$

Untuk berat Timbangan 25 Gram

$$= \frac{25 - 24}{24} \times 100\%$$

$= 4{,}16\,\%$

Untuk berat Timbangan 50 Gram

$50 \quad - 48$

$$= \frac{\quad}{48} \times 100\%$$

$$= 4{,}16\ \%$$

Untuk berat Timbangan 75 Gram

$$= \frac{75 \quad - 76}{76} \times 100\%$$

$$= 1{,}31\ \%$$

Untuk berat Timbangan 100 Gram

$$= \frac{100 \quad - 98}{98} \times 100\%$$

$$= 2{,}04\ \%$$

Tabel 4-6

Prosentase Kesalahan Alat dengan Timbangan yang sebenarnya

Berat (Gram)	Data Timbangan yang sebenarnya (Gram)	Data Alat yang kita buat(Gram)	Prosentase Kesalahan
0	0	0	0
25	25	24	4,16 %
50	50	48	4,16 %
75	75	76	1,31 %
100	100	98	2,04 %

Dari Pengujian keseluruhan maka kita dapat mengetahui kesalahan relatif yang ada untuk prosentasi dapat dihitung dengan sistem pengurangan yaitu,

100 % - 4,16 % = 95,84%

BAB V

PENUTUP

5.1. Kesimpulan

Sesuai dengan perencanaan dan pengujian alat yang telah kita lakukan maka dapat ditarik kesimpulan sebagai berikut :

1. Dengan mikrokontroller menjadikan suatu sistem lebih sederhana dan mudah dalam mengontrol sesuatu.
2. Menggunakan Capasitive sensor sebagai penunjuk karena lebih mudah dalam perakitannya.
3. IC LM555 digunakan sebagai pembangkit sinyal yang frekuensinya bergantung pada perbandingan antara nilai resistor dan perubahan nilai kapasitor.
4. Keypad yang digunakan adalah 4 x 4
5. LCD bertype M1632 sebagai media keluaran.
6. Prosentase data yang benar dari alat yang kita buat adalah 95,84%

5.2. Saran

Setelah kita melakukan percobaan diatas maka dapat diketahui kelemahan alat kita yaitu

1. Kestabilan alat masih perlu diperbaiki
2. Sebaiknya bisa menggunakan catu daya baterei biar mudah dan fleksible untuk dibawa kemana-mana.

3. Alat ini dilengkapi dengan printer agar hasil perhitungan lebih mudah dilihat dan dapat dijadikan dokumen.

Daftar Pustaka

1. Data Sheet AT89S8252
2. Advanced Microdevices,1988
3. Eksperimen Dengan Mikrokontroller, 1999
4. Drs. Ridwan Rusli, Teknik Elektronika
5. Paulus Andi Nalwan Teknik Antarmuka dan Pemrograman Mikrokontroller AT89C51
6. www.lionprecision.com
7. Data sheet LM555
8. Malvino Barmawi, Prinsip-prinsip Elektronika
9. Ibnu Malik, M & Anistardi, *Bereksperimen dengan Mikrokontroller 80C31*. Elex Media Komputindo, Jakarta, 1996.
10. Schweber, William L, *Data communication*. Mc Graw Hill Book company, USA, International Edition,1988.
11. Elektuur, *Data Sheet Book 1*, Elex Media Komputindo, Jakarta 1994.
12. Steeman, J.P.M. *Data Sheet Book 2*. Elex Media Komputindo, Jakarta, 1988.
13. Intel. 1994. *MCS®51 Microcontroller Family User Manual*. Intel Corporation.
14. Malvino, Albert Paul. 1996. *Prinsip-prinsip Elektronika*. Jilid Pertama. Edisi Ketiga. 7. 7. Terjemahan Prof. M. Barnawi, Ph.D. Jakarta : Penerbit Erlangga.
15. www.atmel.com
16. www.sci.com.electronic.components
17. http://alds.stts.edu

LAMPIRAN

INSTITUT TEKNOLOGI NASIONAL
Jl. Bendungan Sigura-gura No. 2
Malang

LEMBAR BIMBINGAN SKRIPSI

1. Nama Mahasiswa : Yusak Al Mukhlas
2. NIM : 0017244
3. Jurusan : Teknik Elektro S-1
4. Konsentrasi : Teknik Elektronika
5. Judul Skripsi : RANCANG BANGUN TIMBANGAN EMAS DAN PENGHITUNG/PENAMPIL HARGA SECARA ELEKTRONIK
6. Tanggal Pengajuan Skripsi : 17 Februari 2006
7. Selesai Menulis Skripsi : 19 September 2006
8. Dosen Pembimbing : Pembimbing I : Ir. Poerwanto, MT
   Pembimbing II : Irmalia Suryani F., ST
9. Telah dievaluasi dengan nilai : Pembimbing I : 87 (Delapan Puluh Tujuh)
   Pembimbing II : 87 (Delapan Puluh Tujuh)

Diperiksa dan disetujui,
Dosen Pembimbing I

(Ir.Poerwanto, MT.)

Diperiksa dan disetujui,
Dosen Pembimbing II

(Irmalia Suryani F., ST)

Mengetahui,
Ketua Jurusan Teknik Elektro S-1

(Ir.F.Yudi Limpraptono,MT.)
NIP.P : 1039500274

INSTITUT TEKNOLOGI NASIONAL
Kampus I : Jl. Bendungan Sigura-gura No.2
Kampus II : Jl. Raya Karanglo, Km.2
MALANG

FORMULIR BIMBINGAN SKRIPSI

Nama : Yusak Al Mukhlas
Nim : 00.17.244
Masa Bimbingan : 17 Februari 2006 s/d 17 Juli 2006
Judul : Rancang Bangun Timbangan Emas dan Penghitung/Penampil Harga Secara Elektronik

No.	Tanggal	Uraian	Paraf Pembimbing
1	08-09-06	Bab I .	
2		- latar belakang	
3		- Rumusan masalah.	
4		Bab II	
5		Ref. Ditambahkan	
6	—	Rencana Daftar isi	
7		Bab III / Bab IV.	
8		Bab VI	
9	—	Desain pemrograman	
10		Hardware ..	

— hitungan pembacaan berat dan sensor

Malang, 2006
Dosen Pembimbing

(Ir. Purwanto, MT)

Form.S-4a

INSTITUT TEKNOLOGI NASIONAL
Kampus I : Jl. Bendungan Sigura-gura No.2
Kampus II : Jl. Raya Karanglo, Km.2
MALANG

FORMULIR BIMBINGAN SKRIPSI

Nama : Yusak Al Mukhlas
Nim : 00.17.244
Masa Bimbingan : 17 Februari 2006 s/d 17 Juli 2006
Judul : Rancang Bangun Timbangan Emas dan Penghitung/Penampil Harga Secara Elektronik

No.	Tanggal	Uraian	Paraf Pembimbing
1	12-07-06	- Revisi Ltr blkg. Rms msl, Btk Mslh Metodologi	
2	12-08-06	- Revisi BAB I	
3	04-09-06	- Acc BAB I - BAB II, III Susunan	
4	09-09-06	- BAB II, IC 555 Sensor	
5	15-09-06	Lengkapi BAB III, IV, V	
6			
7			
8			
9			
10			

Malang, 2006
Dosen Pembimbing

(Irmalia Suryani F, ST)

2 sirah

Form.S-4a

INSTITUT TEKNOLOGI NASIONAL
Jl. Bendungan Sigura-gura No. 2
Malang

FORMULIR PERBAIKAN SKRIPSI

1. Nama Mahasiswa : Yusak Al Mukhlas
2. NIM : 0017244
3. Jurusan : Teknik Elektro S-1
4. Konsentrasi : Teknik Elektronika
5. Masa Bimbingan : 17 Februari 2006 s/d 17 Juli 2006
6. Judul Skripsi : RANCANG BANGUN TIMBANGAN EMAS DAN PENGHITUNG/PENAMPIL HARGA SECARA ELEKTRONIK

No	Tanggal	Uraian	Paraf
1	23-09-2006	Analisa Dari Sensor Kapasitif	
2	23-09-2006	Analisa Antara Sensor Kapasitif dengan IC555 Serta Hubungannya	
3	23-09-2006	Cara Pengkalibrasian Alat	

Disetujui

Penguji Pertama

(Ir. Usman Djuanda, MM.)

Penguji Kedua

(Sotyohadi, ST, Msc.)

Mengetahui

Dosen Pembimbing I

(Ir.Poerwanto, MT.)

Dosen Pembimbing II

(Irmalia Suryani F., ST)

INSTITUT TEKNOLOGI NASIONAL
FAKULTAS TEKNOLOGI INDUSTRI
JURUSAN TEKNIK ELEKTRO

Formulir Perbaikan Ujian Skripsi

Dalam pelaksanaan Ujian Skripsi Janjang Strata 1 Jurusan Teknik Elektro Konsentasi T. Energi Listrik / T. Elektronika, maka perlu adanya perbaikan skripsi untuk mahasiswa :

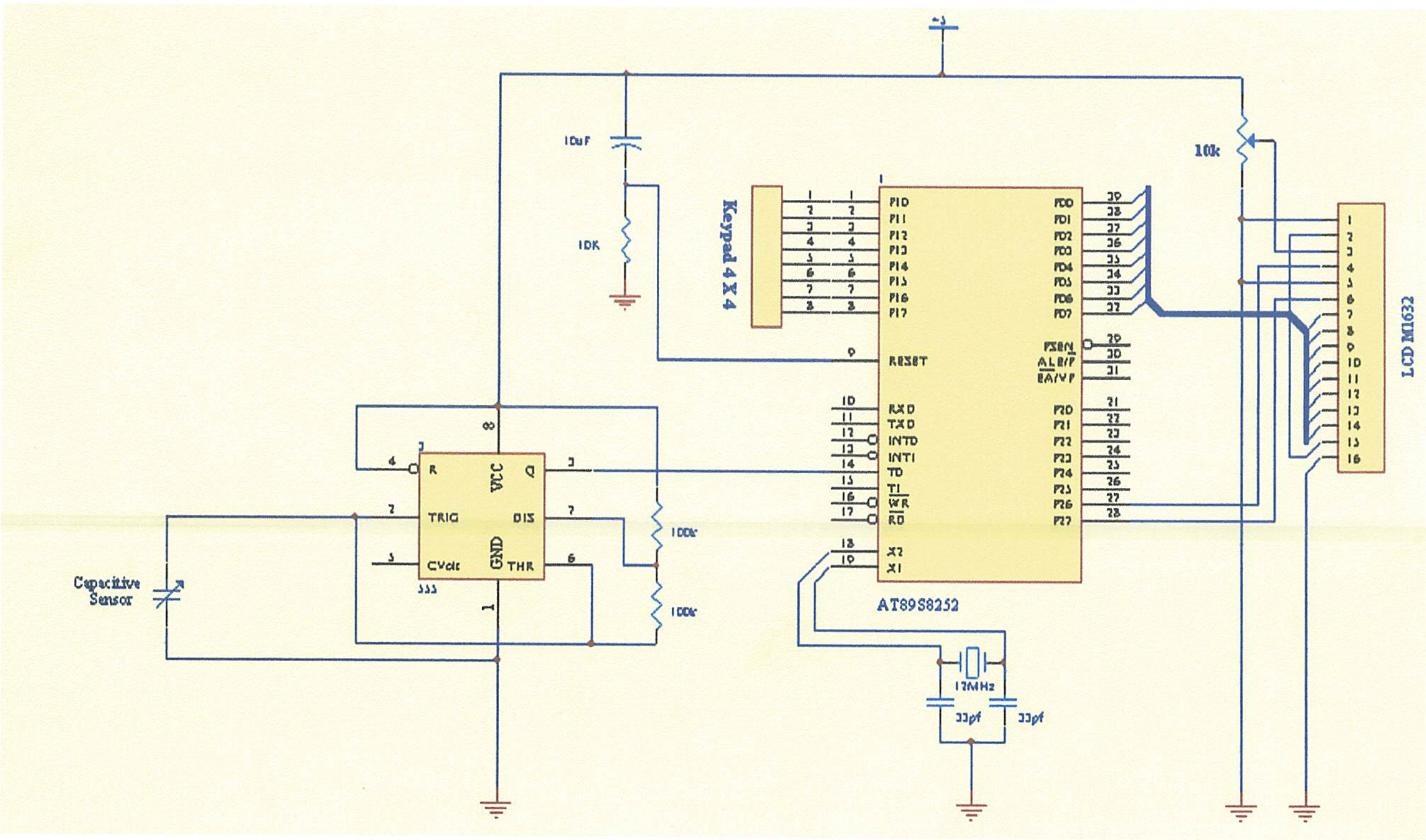
NAMA : Yusak Al Mukhlas
N I M : 0017244
Perbaikan meliputi :

1) Analisa dari sensor kapasitif.
2). Analisa antara sensor kapasitif dengan IC 555 serta hubungannya.
3). Cara pengkalibrasian alat.

Malang, 23 - 9 - 2006

( )

Gambar Rangkaian Kaseluruhan



Listing Programs

```
org   0h

    Wmcn     Data 96h         ; eeprom control
    Eemn     Equ 00001000b         ; eeprom enable
    Eemw     Equ 00010000b         ; eeprom write
    Wtdg     Equ 00000010b         ; watchdog
    Rest     Bit P2.6
    Enbl     Bit P2.7
    Brt0     Equ 30h
    Brt1     Equ 31h
    Brt2     Equ 32h
    Hrg0     Equ 33h
    Hrg1     Equ 34h
    Hrg2     Equ 35h
    Hrg3     Equ 36h
    Hrg4     Equ 37h
    Hrg5     Equ 38h
    Hbfr     Equ 39h
    Hb00     Equ 3Ah
    Hb01     Equ 3Bh
    Hb02     Equ 3Ch
    Hb03     Equ 3Dh
    Hb04     Equ 3Eh
    Hb05     Equ 3Fh
    Hb06     Equ 40h
    Hb10     Equ 41h
    Hb11     Equ 42h
    Hb12     Equ 43h
    Hb13     Equ 44h
```

```
        Hb14    Equ 45h
        Hb15    Equ 46h
        Hb16    Equ 47h
        Hb20    Equ 48h
        Hb21    Equ 49h
        Hb22    Equ 4Ah
        Hb23    Equ 4Bh
        Hb24    Equ 4Ch
        Hb25    Equ 4Dh
        Hb26    Equ 4Eh
        Hrt0    Equ 4Fh
        Hrt1    Equ 50h
        Hrt2    Equ 51h
        Hrt3    Equ 52h
        Hrt4    Equ 53h
        Hrt5    Equ 54h
        Hrt6    Equ 55h
        Hrt7    Equ 56h
        Hrt8    Equ 57h
        Awal    Equ 58h
        Ukur    Equ 59h
        Hurf    Equ 5Ah
        Dly0    Equ 5Bh
        Dly1    Equ 5Ch
        Dly2    Equ 5Dh
;
init:   lcall   lcdins
        mov     TMOD,#15h          ; timer0 mode counter, timer1
mode 16 bit
;
mulai:  mov     SP,#07h            ; reset RAM
        mov     DPTR,#nama
```

```
        lcall   line1
        mov     Hurf,#16
        lcall   tulis
        lcall   line2
        mov     Hurf,#16
        lcall   tulis
        lcall   tg_lps
        lcall   delay1
        lcall   line1
        mov     Hurf,#16
        lcall   tulis
        lcall   line2
        mov     Hurf,#16
        lcall   tulis
        lcall   delay1
        ljmp    mulai
;
seting: mov     SP,#07h             ; reset RAM
plh0:   cjne    R7,#1,plh1
        lcall   rd_mem
        lcall   hpshrg
        mov     DPTR,#gr20k
plh1:   cjne    R7,#2,plh2
        lcall   rd_mem
        lcall   hpshrg
        mov     DPTR,#gr21k
plh2:   cjne    R7,#3,plh3
        lcall   rd_mem
        lcall   hpshrg
        mov     DPTR,#gr22k
plh3:   cjne    R7,#4,plh4
        lcall   rd_mem
```

```
        lcall   hpshrg
        mov     DPTR,#gr23k
plh4:   cjne    R7,#5,plh5
        lcall   rd_mem
        lcall   hpshrg
        mov     DPTR,#gr24k
plh5:   lcall   line1
        mov     Hurf,#16
        lcall   tulis
        mov     DPTR,#angka
        lcall   line2
        mov     A,#10
        lcall   wr_chr
        mov     A,#10
        lcall   wr_chr
        mov     A,#11
        lcall   wr_chr
        mov     A,#12
        lcall   wr_chr
        mov     A,#13
        lcall   wr_chr
        mov     A,Hrg0
        lcall   wr_chr
        mov     A,Hrg1
        lcall   wr_chr
        mov     A,Hrg2
        lcall   wr_chr
        mov     A,#13
        lcall   wr_chr
        mov     A,Hrg3
        lcall   wr_chr
        mov     A,Hrg4
```

```
        lcall   wr_chr
        mov     A,Hrg5
        lcall   wr_chr
        mov     A,#14
        lcall   wr_chr
        mov     A,#15
        lcall   wr_chr
        mov     A,#10
        lcall   wr_chr
        mov     A,#10
        lcall   wr_chr
        lcall   tg_lps
plh6:   lcall   scnkpd
        cjne    R1,#15,plh8
        dec     R7
        cjne    R7,#0,plh7
        mov     R7,#1
plh7:   ljmp    seting
plh8:   cjne    R1,#16,plhA
        inc     R7
        cjne    R7,#6,plh9
        mov     R7,#5
plh9:   ljmp    seting
plhA:   cjne    R1,#11,plhB
        ljmp    mulai
plhB:   cjne    R1,#12,plh6
        ljmp    gnthrg
;
gnthrg: mov     SP,#07h             ; reset RAM
        mov     DPTR,#mshrg
        lcall   line1
        mov     Hurf,#16
```

```
lcall   tulis
mov     DPTR,#angka
lcall   line2
mov     A,#10
lcall   wr_chr
mov     A,#10
lcall   wr_chr
mov     A,#11
lcall   wr_chr
mov     A,#12
lcall   wr_chr
mov     A,#13
lcall   wr_chr
lcall   tg_lps
lcall   tg_tkn
mov     A,R1
mov     Hrg0,A
lcall   wr_chr
lcall   tg_lps
lcall   tg_tkn
mov     A,R1
mov     Hrg1,A
lcall   wr_chr
lcall   tg_lps
lcall   tg_tkn
mov     A,R1
mov     Hrg2,A
lcall   wr_chr
lcall   tg_lps
mov     A,#13
lcall   wr_chr
lcall   tg_tkn
```

```
        mov     A,R1
        mov     Hrg3,A
        lcall   wr_chr
        lcall   tg_lps
        lcall   tg_tkn
        mov     A,R1
        mov     Hrg4,A
        lcall   wr_chr
        lcall   tg_lps
        lcall   tg_tkn
        mov     A,R1
        mov     Hrg5,A
        lcall   wr_chr
        lcall   tg_lps
        mov     A,#14
        lcall   wr_chr
        mov     A,#15
        lcall   wr_chr
        mov     A,#10
        lcall   wr_chr
        mov     A,#10
        lcall   wr_chr
        mov     DPTR,#hrbnr
        lcall   line1
        mov     Hurf,#16
        lcall   tulis
bole0:  lcall   scnkpd
        cjne    R1,#11,bole1
        ljmp    mulai
bole1:  cjne    R1,#12,bole0
        lcall   wr_mem
        lcall   tg_lps
```

```
        ljmp    mulai
;
hpshrg: mov     A,Hrg0
        cjne    A,#0,hpshr1
        mov     Hrg0,#10
hpshr1: mov     A,Hrg1
        cjne    A,#0,hpshr2
        mov     A,Hrg0
        cjne    A,#10,hpshr2
        mov     Hrg1,#10
hpshr2: mov     A,Hrg2
        cjne    A,#0,hpshr3
        mov     A,Hrg1
        cjne    A,#10,hpshr3
        mov     Hrg2,#10
hpshr3: mov     A,Hrg3
        cjne    A,#0,hpshr4
        mov     A,Hrg2
        cjne    A,#10,hpshr4
        mov     Hrg3,#10
hpshr4: mov     A,Hrg4
        cjne    A,#0,hpshr5
        mov     A,Hrg3
        cjne    A,#10,hpshr5
        mov     Hrg4,#10
hpshr5: mov     A,Hrg5
        cjne    A,#0,hpshr6
        mov     A,Hrg4
        cjne    A,#10,hpshr6
        mov     Hrg5,#10
hpshr6: ret
;
```

```
imbng: mov     SP,#07h          ; reset RAM
       lcall   bc_sns
       mov     Awal,Ukur
       lcall   rd_mem

oop0:  cjne    R7,#1,loop1
       mov     DPTR,#hr20k
oop1:  cjne    R7,#2,loop2
       mov     DPTR,#hr21k
oop2:  cjne    R7,#3,loop3
       mov     DPTR,#hr22k
oop3:  cjne    R7,#4,loop4
       mov     DPTR,#hr23k
oop4:  cjne    R7,#5,loop5
       mov     DPTR,#hr24k
oop5:  lcall   line1
       mov     Hurf,#8
       lcall   tulis
       lcall   bc_sns
       lcall   klbrs
       lcall   cacah
       mov     DPTR,#angka
       mov     A,Brt0
       lcall   wr_chr
       mov     A,Brt1
       lcall   wr_chr
       mov     A,Brt2
       lcall   wr_chr
       mov     DPTR,#hr20k
       mov     A,#11
       lcall   wr_chr
       mov     A,#12
```

```
lcall   wr_chr
mov     A,#13
lcall   wr_chr
mov     A,#14
lcall   wr_chr
mov     A,#15
lcall   wr_chr
lcall   brxhrg              ; berat kali harga
mov     DPTR,#angka
lcall   line2
mov     A,#11
lcall   wr_chr
mov     A,#12
lcall   wr_chr
mov     A,#13
lcall   wr_chr
mov     A,Hrt0
lcall   wr_chr
mov     A,Hrt1
lcall   wr_chr
mov     A,Hrt2
lcall   wr_chr
mov     A,#13
lcall   wr_chr
mov     A,Hrt3
lcall   wr_chr
mov     A,Hrt4
lcall   wr_chr
mov     A,Hrt5
lcall   wr_chr
mov     A,#13
lcall   wr_chr
```

```
        mov     A,Hrt6
        lcall   wr_chr
        mov     A,Hrt7
        lcall   wr_chr
        mov     A,Hrt8
        lcall   wr_chr
        mov     A,#14
        lcall   wr_chr
        mov     A,#15
        lcall   wr_chr
        lcall   delay
        lcall   delay
        lcall   delay
        ljmp    loop0
;
bc_sns: mov     TH0,#000h
        mov     TL0,#000h
        setb    TR0
        mov     TH1,#0B8h           ;\ 65535 - 18250 = 47285
        mov     TL1,#0B5h           ;/ FFFF  - 474A  = B8B5
        clr     TF1
        setb    TR1
        jnb     TF1,$
        clr     TR0
        clr     TR1
        mov     Ukur,TL0
        ret
;
klbrs:  mov     A,Ukur
        mov     B,Awal
        div     AB
cek0:   cjne    A,#0,cek1
```

```
        ljmp    hps2
cekl:   mov     A,Ukur
        mov     B,Awal
        subb    A,B
        mov     Ukur,A
        mov     B,#101
        div     AB
cek2:   cjne    A,#0,brtmax
        mov     A,Ukur
        ret
;
brtmax: mov     DPTR,#ovrld
        lcall   line1
        mov     Hurf,#16
        lcall   tulis
        mov     DPTR,#kosong
        lcall   line2
        mov     Hurf,#16
        lcall   tulis
        lcall   bc_sns
        ljmp    klbrs
;
cacah:  mov     B,#100
        div     AB
        mov     R2,A
        mov     A,B
        mov     B,#10
        div     AB
        mov     R3,A
        mov     R4,B
        mov     Brt0,R2
        mov     Brt1,R3
```

```
        mov     Brt2,R4
hps0:   mov     A,Brt0
        cjne    A,#0,hps1
        mov     Brt0,#10
hps1:   mov     A,Brt1
        cjne    A,#0,hps2
        mov     A,Brt0
        cjne    A,#10,hps2
        mov     Brt1,#10
hps2:   ret
;
brxhrg: lcall   rd_mem
        clr     C
        mov     A,Hrg5          ;\
        mov     B,R4            ; | hrg5 x brt3
        mul     AB              ; | hasil : 10
        mov     B,#10           ; | simpan hasil bagi
        div     AB              ; | simpan sisa Hb00
        mov     Hbfr,A          ; |
        mov     Hb00,B          ;/
        mov     A,Hrg4          ;\
        mov     B,R4            ; |
        mul     AB              ; | hrg4 x brt3
        mov     B,Hbfr          ; | hasil + hasil bagi sblmnya
        add     A,B             ; | hasil : 10
        mov     B,#10           ; | simpan hasil bagi
        div     AB              ; | simpan sisa Hb01
        mov     Hbfr,A          ; |
        mov     Hb01,B          ;/
        mov     A,Hrg3          ;\
        mov     B,R4            ; |
        mul     AB              ; | hrg3 x brt3
```

```
mov     B,Hbfr          ; | hasil + hasil bagi sblmnya
add     A,B             ; | hasil : 10
mov     B,#10           ; | simpan hasil bagi
div     AB              ; | simpan sisa Hb02
mov     Hbfr,A          ; |
mov     Hb02,B          ;/
mov     A,Hrg2          ;\
mov     B,R4            ; |
mul     AB              ; | hrg2 x brt3
mov     B,Hbfr          ; | hasil + hasil bagi sblmnya
add     A,B             ; | hasil : 10
mov     B,#10           ; | simpan hasil bagi
div     AB              ; | simpan sisa Hb03
mov     Hbfr,A          ; |
mov     Hb03,B          ;/
mov     A,Hrg1          ;\
mov     B,R4            ; |
mul     AB              ; | hrg1 x brt3
mov     B,Hbfr          ; | hasil + hasil bagi sblmnya
add     A,B             ; | hasil : 10
mov     B,#10           ; | simpan hasil bagi
div     AB              ; | simpan sisa Hb04
mov     Hbfr,A          ; |
mov     Hb04,B          ;/
mov     A,Hrg0          ;\
mov     B,R4            ; |
mul     AB              ; | hrg0 x brt3
mov     B,Hbfr          ; | hasil + hasil bagi sblmnya
add     A,B             ; | hasil : 10
mov     B,#10           ; | hasil bagi simpan Hb06
div     AB              ; | simpan sisa Hb05
mov     Hb06,A          ; |
```

```
        mov     Hb05,B              ;/
;
        clr     C
        mov     A,Hrg5              ;\
        mov     B,R3                ; | hrg5 x brt2
        mul     AB              ; | hasil : 10
        mov     B,#10               ; | simpan hasil bagi
        div     AB              ; | simpan sisa Hb10
        mov     Hbfr,A              ; |
        mov     Hb10,B              ;/
        mov     A,Hrg4              ;\
        mov     B,R3                ; |
        mul     AB              ; | hrg4 x brt2
        mov     B,Hbfr              ; | hasil + hasil bagi sblmnya
        add     A,B             ; | hasil : 10
        mov     B,#10               ; | simpan hasil bagi
        div     AB              ; | simpan sisa Hb11
        mov     Hbfr,A              ; |
        mov     Hb11,B              ;/
        mov     A,Hrg3              ;\
        mov     B,R3                ; |
        mul     AB              ; | hrg3 x brt2
        mov     B,Hbfr              ; | hasil + hasil bagi sblmnya
        add     A,B             ; | hasil : 10
        mov     B,#10               ; | simpan hasil bagi
        div     AB              ; | simpan sisa Hb12
        mov     Hbfr,A              ; |
        mov     Hb12,B              ;/
        mov     A,Hrg2              ;\
        mov     B,R3                ; |
        mul     AB              ; | hrg2 x brt2
        mov     B,Hbfr              ; | hasil + hasil bagi sblmnya
```

```
        add     A,B             ; | hasil : 10
        mov     B,#10               ; | simpan hasil bagi
        div     AB              ; | simpan sisa Hb13
        mov     Hbfr,A              ; |
        mov     Hb13,B              ;/
        mov     A,Hrg1              ;\
        mov     B,R3                ; |
        mul     AB              ; | hrg1 x brt2
        mov     B,Hbfr              ; | hasil + hasil bagi sblmnya
        add     A,B             ; | hasil : 10
        mov     B,#10               ; | simpan hasil bagi
        div     AB              ; | simpan sisa Hb14
        mov     Hbfr,A              ; |
        mov     Hb14,B              ;/
        mov     A,Hrg0              ;\
        mov     B,R3                ; |
        mul     AB              ; | hrg0 x brt2
        mov     B,Hbfr              ; | hasil + hasil bagi sblmnya
        add     A,B             ; | hasil : 10
        mov     B,#10               ; | hasil bagi simpan Hb16
        div     AB              ; | simpan sisa Hb15
        mov     Hb16,A              ; |
        mov     Hb15,B              ;/
;
        clr     C
        mov     A,Hrg5              ;\
        mov     B,R2                ; | hrg5 x brt1
        mul     AB              ; | hasil : 10
        mov     B,#10               ; | simpan hasil bagi
        div     AB              ; | simpan sisa hb20
        mov     Hbfr,A              ; |
        mov     hb20,B              ;/
```

```
mov     A,Hrg4          ;\
mov     B,R2            ; |
mul     AB              ; | hrg4 x brt1
mov     B,Hbfr          ; | hasil + hasil bagi sblmnya
add     A,B             ; | hasil : 10
mov     B,#10           ; | simpan hasil bagi
div     AB              ; | simpan sisa hb21
mov     Hbfr,A          ; |
mov     hb21,B          ;/
mov     A,Hrg3          ;\
mov     B,R2            ; |
mul     AB              ; | hrg3 x brt1
mov     B,Hbfr          ; | hasil + hasil bagi sblmnya
add     A,B             ; | hasil : 10
mov     B,#10           ; | simpan hasil bagi
div     AB              ; | simpan sisa hb22
mov     Hbfr,A          ; |
mov     hb22,B          ;/
mov     A,Hrg2          ;\
mov     B,R2            ; |
mul     AB              ; | hrg2 x brt1
mov     B,Hbfr          ; | hasil + hasil bagi sblmnya
add     A,B             ; | hasil : 10
mov     B,#10           ; | simpan hasil bagi
div     AB              ; | simpan sisa hb23
mov     Hbfr,A          ; |
mov     hb23,B          ;/
mov     A,Hrg1          ;\
mov     B,R2            ; |
mul     AB              ; | hrg1 x brt1
mov     B,Hbfr          ; | hasil + hasil bagi sblmnya
add     A,B             ; | hasil : 10
```

```
        mov     B,#10               ; | simpan hasil bagi
        div     AB              ; | simpan sisa hb24
        mov     Hbfr,A              ; |
        mov     hb24,B              ;/
        mov     A,Hrg0              ;\
        mov     B,R2                ; |
        mul     AB              ; | hrg0 x brt1
        mov     B,Hbfr              ; | hasil + hasil bagi sblmnya
        add     A,B             ; | hasil : 10
        mov     B,#10               ; | hasil bagi simpan hb26
        div     AB              ; | simpan sisa hb25
        mov     hb26,A              ; |
        mov     hb25,B              ;/
;
        clr     C
        mov     Hrt8,Hb00           ; hb00 simpan hrt8
        mov     A,Hb01              ;\
        mov     B,Hb10              ; | hb01 + hb10
        add     A,B             ; | hasil : 10
        mov     B,#10               ; | hasil bagi simpan hbfr
        div     AB              ; | sisa simpan hrt7
        mov     Hbfr,A              ; |
        mov     Hrt7,B              ;/
        mov     A,Hb02              ;\
        mov     B,Hb11              ; |
        add     A,B             ; | hb02 + hb11
        mov     B,Hb20              ; | hasil + hb20
        add     A,B             ; | hasil + hasil bagi sblmnya
        mov     B,Hbfr              ; | hasil : 10
        add     A,B             ; | hasil bagi simpan hbfr
        mov     B,#10               ; | sisa simpan hrt6
        div     AB              ; |
```

```
mov     Hbfr,A              ; |
mov     Hrt6,B              ;/
mov     A,Hb03              ;\
mov     B,Hb12              ; |
add     A,B           ; | hb03 + hb12
mov     B,Hb21              ; | hasil + hb21
add     A,B           ; | hasil + hasil bagi sblmnya
mov     B,Hbfr              ; | hasil : 10
add     A,B           ; | hasil bagi simpan hbfr
mov     B,#10               ; | sisa simpan hrt5
div     AB            ; |
mov     Hbfr,A              ; |
mov     Hrt5,B              ;/
mov     A,Hb04              ;\
mov     B,Hb13              ; |
add     A,B           ; | hb04 + hb13
mov     B,Hb22              ; | hasil + hb22
add     A,B           ; | hasil + hasil bagi sblmnya
mov     B,Hbfr              ; | hasil : 10
add     A,B           ; | hasil bagi simpan hbfr
mov     B,#10               ; | sisa simpan hrt4
div     AB            ; |
mov     Hbfr,A              ; |
mov     Hrt4,B              ;/
mov     A,Hb05              ;\
mov     B,Hb14              ; |
add     A,B           ; | hb05 + hb14
mov     B,Hb23              ; | hasil + hb23
add     A,B           ; | hasil + hasil bagi sblmnya
mov     B,Hbfr              ; | hasil : 10
add     A,B           ; | hasil bagi simpan hbfr
mov     B,#10               ; | sisa simpan hrt3
```

```
        div     AB              ; |
        mov     Hbfr,A              ; |
        mov     Hrt3,B              ;/
        mov     A,Hb06              ;\
        mov     B,Hb15              ; |
        add     A,B             ; | hb06 + hb15
        mov     B,Hb24              ; | hasil + hb24
        add     A,B             ; | hasil + hasil bagi sblmnya
        mov     B,Hbfr              ; | hasil : 10
        add     A,B             ; | hasil bagi simpan hbfr
        mov     B,#10               ; | sisa simpan hrt2
        div     AB              ; |
        mov     Hbfr,A              ; |
        mov     Hrt2,B              ;/
        mov     A,Hb16              ;\
        mov     B,Hb25              ; |
        add     A,B             ; | hb16 + hb25
        mov     B,Hbfr              ; | hasil + hasil bagi sblmnya
        add     A,B             ; | hasil : 10
        mov     B,#10               ; | hasil bagi simpan hbfr
        div     AB              ; | sisa simpan hrt1
        mov     Hbfr,A              ; |
        mov     Hrt1,B              ;/
        mov     A,Hb26              ;\
        mov     B,Hbfr              ; | bh26 + hasil bagi sblmnya
        add     A,B             ; | hasil bagi simpan hrt0
        mov     Hrt0,A              ;/

ıphrt0: mov     A,Hrt0
        cjne    A,#0,hphrt1
        mov     Hrt0,#10
ıphrt1: mov     A,Hrt1
```

```
        cjne    A,#0,hphrt2
        mov     A,Hrt0
        cjne    A,#10,hphrt2
        mov     Hrt1,#10
phrt2:  mov     A,Hrt2
        cjne    A,#0,hphrt3
        mov     A,Hrt1
        cjne    A,#10,hphrt3
        mov     Hrt2,#10
phrt3:  mov     A,Hrt3
        cjne    A,#0,hphrt4
        mov     A,Hrt2
        cjne    A,#10,hphrt4
        mov     Hrt3,#10
phrt4:  mov     A,Hrt4
        cjne    A,#0,hphrt5
        mov     A,Hrt3
        cjne    A,#10,hphrt5
        mov     Hrt4,#10
phrt5:  mov     A,Hrt5
        cjne    A,#0,hphrt6
        mov     A,Hrt4
        cjne    A,#10,hphrt6
        mov     Hrt5,#10
phrt6:  mov     A,Hrt6
        cjne    A,#0,hphrt7
        mov     A,Hrt5
        cjne    A,#10,hphrt7
        mov     Hrt6,#10
phrt7:  mov     A,Hrt7
        cjne    A,#0,hphrt8
        mov     A,Hrt6
```

```
        cjne    A,#10,hphrt8
        mov     Hrt7,#10
ıphrt8: ret
;
.ine1:     mov  R0,#80h
     lcall      inst
        ret
.
.ine2:     mov  R0,#0C0h
     lcall      inst
        ret
,
:ulis:  clr    A
     movc A,@A+DPTR
     mov  R0,A
     inc  DPTR
     lcall      char
     djnz Hurf,tulis
        ret

ır_chr: movc    A,@A+DPTR
        mov     R0,A
        lcall   char
        ret

.nst:   clr     Enbl
        clr     Rest
        mov     P0,R0
        setb    Enbl
        clr     Enbl
        lcall   jeda
        ret
```

```
ıar:   clr     Enbl
       setb    Rest
       mov     P0,R0
       setb    Enbl
       clr     Enbl
       lcall   jeda
       ret

:dins:    mov  R0,#03Fh
    lcall     inst
    lcall     inst
    mov  R0,#0Dh
    lcall     inst
    mov  R0,#06h
    lcall     inst
    mov  R0,#01h
    lcall     inst
    mov  R0,#0Ch
    lcall     inst
       lcall   jeda
       ret

:nkpd: lcall   jeda
       mov     R1,#10
ɔl1:   mov     P1,#11111110b
       mov     A,P1
lb1:   cjne    A,#11101110b,clb2
       mov     R1,#1
lb2:   cjne    A,#11011110b,clb3
       mov     R1,#2
lb3:   cjne    A,#10111110b,clb4
```

```
        mov     R1,#3
c1b4:   cjne    A,#01111110b,col2
        mov     R1,#13
;
col2:   mov     P1,#11111101b
        mov     A,P1
c2b1:   cjne    A,#11101101b,c2b2
        mov     R1,#4
c2b2:   cjne    A,#11011101b,c2b3
        mov     R1,#5
c2b3:   cjne    A,#10111101b,c2b4
        mov     R1,#6
c2b4:   cjne    A,#01111101b,col3
        mov     R1,#14
;
col3:   mov     P1,#11111011b
        mov     A,P1
c3b1:   cjne    A,#11101011b,c3b2
        mov     R1,#7
c3b2:   cjne    A,#11011011b,c3b3
        mov     R1,#8
c3b3:   cjne    A,#10111011b,c3b4
        mov     R1,#9
c3b4:   cjne    A,#01111011b,col4
        mov     R1,#15
;
col4:   mov     P1,#11110111b
        mov     A,P1
c4b1:   cjne    A,#11100111b,c4b2
        mov     R1,#11
c4b2:   cjne    A,#11010111b,c4b3
        mov     R1,#0
```

```
c4b3:   cjne    A,#10110111b,c4b4
        mov     R1,#12
c4b4:   cjne    A,#01110111b,back
        mov     R1,#16
back:   ret
;
tg_tkn: lcall   jeda
        lcall   scnkpd
tg_tk0: cjne    R1,#16,tg_tk1
        ljmp    tg_tkn
tg_tk1: cjne    R1,#15,tg_tk2
        ljmp    tg_tkn
tg_tk2: cjne    R1,#14,tg_tk3
        ljmp    tg_tkn
tg_tk3: cjne    R1,#13,tg_tk4
        ljmp    tg_tkn
tg_tk4: cjne    R1,#12,tg_tk5
        ljmp    tg_tkn
tg_tk5: cjne    R1,#11,tg_tk6
        ljmp    mulai
tg_tk6: cjne    R1,#10,tg_tk7
        ljmp    tg_tkn
tg_tk7: ret
;
tg_lps: lcall   jeda
        lcall   scnkpd
        cjne    R1,#10,tg_lps
        ret
;
jeda:   djnz    Dly0,$
        ret
;
```

```
ilys0:  lcall   scnkpd
        cjne    R1,#13,dlys1
        mov     R7,#1
        ljmp    seting
ilys1:  cjne    R1,#14,dlys2
        mov     R7,#1
        ljmp    timbng
ilys2:  djnz    Dly1,dlys0
        ret

lelay:  lcall   scnkpd
        cjne    R1,#11,dely1
        ljmp    mulai
lely1:  cjne    R1,#15,dely3
        lcall   tg_lps
        dec     R7
        cjne    R7,#0,dely2
        mov     R7,#1
lely2:  lcall   rd_mem
        ljmp    loop0
lely3:  cjne    R1,#16,dely5
        lcall   tg_lps
        inc     R7
        cjne    R7,#6,dely4
        mov     R7,#5
lely4:  lcall   rd_mem
        ljmp    loop0
lely5:  djnz    Dly1,delay
        ret

lelay1: mov     Dly2,#20
llyl:   lcall   dlys0
```

```
        djnz    Dly2,dly1
        ret

d_mem:  cjne    R7,#1,rd_mm1
        lcall   strdmm
        mov     DPTR,#00
        movx    A,@DPTR
        mov     Hrg0,A
        mov     DPTR,#01
        movx    A,@DPTR
        mov     Hrg1,A
        mov     DPTR,#02
        movx    A,@DPTR
        mov     Hrg2,A
        mov     DPTR,#03
        movx    A,@DPTR
        mov     Hrg3,A
        mov     DPTR,#04
        movx    A,@DPTR
        mov     Hrg4,A
        mov     DPTR,#05
        movx    A,@DPTR
        mov     Hrg5,A

d_mm1:  cjne    R7,#2,rd_mm2
        lcall   strdmm
        mov     DPTR,#06
        movx    A,@DPTR
        mov     Hrg0,A
        mov     DPTR,#07
        movx    A,@DPTR
        mov     Hrg1,A
```

```
        mov     DPTR,#08
        movx    A,@DPTR
        mov     Hrg2,A
        mov     DPTR,#09
        movx    A,@DPTR
        mov     Hrg3,A
        mov     DPTR,#10
        movx    A,@DPTR
        mov     Hrg4,A
        mov     DPTR,#11
        movx    A,@DPTR
        mov     Hrg5,A

rd_mm2: cjne    R7,#3,rd_mm3
        lcall   strdmm
        mov     DPTR,#12
        movx    A,@DPTR
        mov     Hrg0,A
        mov     DPTR,#13
        movx    A,@DPTR
        mov     Hrg1,A
        mov     DPTR,#14
        movx    A,@DPTR
        mov     Hrg2,A
        mov     DPTR,#15
        movx    A,@DPTR
        mov     Hrg3,A
        mov     DPTR,#16
        movx    A,@DPTR
        mov     Hrg4,A
        mov     DPTR,#17
        movx    A,@DPTR
```

```
        mov     Hrg5,A
;
rd_mm3: cjne    R7,#4,rd_mm4
        lcall   strdmm
        mov     DPTR,#18
        movx    A,@DPTR
        mov     Hrg0,A
        mov     DPTR,#19
        movx    A,@DPTR
        mov     Hrg1,A
        mov     DPTR,#20
        movx    A,@DPTR
        mov     Hrg2,A
        mov     DPTR,#21
        movx    A,@DPTR
        mov     Hrg3,A
        mov     DPTR,#22
        movx    A,@DPTR
        mov     Hrg4,A
        mov     DPTR,#23
        movx    A,@DPTR
        mov     Hrg5,A
;
rd_mm4: cjne    R7,#5,rd_mm5
        lcall   strdmm
        mov     DPTR,#24
        movx    A,@DPTR
        mov     Hrg0,A
        mov     DPTR,#25
        movx    A,@DPTR
        mov     Hrg1,A
        mov     DPTR,#26
```

```
        movx    A,@DPTR
        mov     Hrg2,A
        mov     DPTR,#27
        movx    A,@DPTR
        mov     Hrg3,A
        mov     DPTR,#28
        movx    A,@DPTR
        mov     Hrg4,A
        mov     DPTR,#29
        movx    A,@DPTR
        mov     Hrg5,A
rd_mm5: ret
;
wr_mem: cjne    R7,#1,wr_mm1
        lcall   stwrmm
        mov     DPTR,#00
        mov     A,Hrg0
        movx    @DPTR,A
        lcall   wt_wr
        mov     DPTR,#01
        mov     A,Hrg1
        movx    @DPTR,A
        lcall   wt_wr
        mov     DPTR,#02
        mov     A,Hrg2
        movx    @DPTR,A
        lcall   wt_wr
        mov     DPTR,#03
        mov     A,Hrg3
        movx    @DPTR,A
        lcall   wt_wr
        mov     DPTR,#04
```

```
        mov     A,Hrg4
        movx    @DPTR,A
        lcall   wt_wr
        mov     DPTR,#05
        mov     A,Hrg5
        movx    @DPTR,A
        lcall   wt_wr
        lcall   enwrmm
;
wr_mm1: cjne    R7,#2,wr_mm2
        lcall   stwrmm
        mov     DPTR,#06
        mov     A,Hrg0
        movx    @DPTR,A
        lcall   wt_wr
        mov     DPTR,#07
        mov     A,Hrg1
        movx    @DPTR,A
        lcall   wt_wr
        mov     DPTR,#08
        mov     A,Hrg2
        movx    @DPTR,A
        lcall   wt_wr
        mov     DPTR,#09
        mov     A,Hrg3
        movx    @DPTR,A
        lcall   wt_wr
        mov     DPTR,#10
        mov     A,Hrg4
        movx    @DPTR,A
        lcall   wt_wr
        mov     DPTR,#11
```

```
        mov     A,Hrg5
        movx    @DPTR,A
        lcall   wt_wr
        lcall   enwrmm
;
wr_mm2: cjne    R7,#3,wr_mm3
        lcall   stwrmm
        mov     DPTR,#12
        mov     A,Hrg0
        movx    @DPTR,A
        lcall   wt_wr
        mov     DPTR,#13
        mov     A,Hrg1
        movx    @DPTR,A
        lcall   wt_wr
        mov     DPTR,#14
        mov     A,Hrg2
        movx    @DPTR,A
        lcall   wt_wr
        mov     DPTR,#15
        mov     A,Hrg3
        movx    @DPTR,A
        lcall   wt_wr
        mov     DPTR,#16
        mov     A,Hrg4
        movx    @DPTR,A
        lcall   wt_wr
        mov     DPTR,#17
        mov     A,Hrg5
        movx    @DPTR,A
        lcall   wt_wr
        lcall   enwrmm
```

```
;
wr_mm3: cjne     R7,#4,wr_mm4
        lcall    stwrmm
        mov      DPTR,#18
        mov      A,Hrg0
        movx     @DPTR,A
        lcall    wt_wr
        mov      DPTR,#19
        mov      A,Hrg1
        movx     @DPTR,A
        lcall    wt_wr
        mov      DPTR,#20
        mov      A,Hrg2
        movx     @DPTR,A
        lcall    wt_wr
        mov      DPTR,#21
        mov      A,Hrg3
        movx     @DPTR,A
        lcall    wt_wr
        mov      DPTR,#22
        mov      A,Hrg4
        movx     @DPTR,A
        lcall    wt_wr
        mov      DPTR,#23
        mov      A,Hrg5
        movx     @DPTR,A
        lcall    wt_wr
        lcall    enwrmm

wr_mm4: cjne     R7,#5,wr_mm5
        lcall    stwrmm
        mov      DPTR,#24
```

```
        mov     A,Hrg0
        movx    @DPTR,A
        lcall   wt_wr
        mov     DPTR,#25
        mov     A,Hrg1
        movx    @DPTR,A
        lcall   wt_wr
        mov     DPTR,#26
        mov     A,Hrg2
        movx    @DPTR,A
        lcall   wt_wr
        mov     DPTR,#27
        mov     A,Hrg3
        movx    @DPTR,A
        lcall   wt_wr
        mov     DPTR,#28
        mov     A,Hrg4
        movx    @DPTR,A
        lcall   wt_wr
        mov     DPTR,#29
        mov     A,Hrg5
        movx    @DPTR,A
        lcall   wt_wr
        lcall   enwrmm
r_mm5:  ret

twrmm:  orl     Wmcn,#Eemn
        orl     Wmcn,#Eemw
        ret

nwrmm:  xrl     Wmcn,#Eemw
        xrl     Wmcn,#Eemn
```

```
        ret

strdmm: orl     Wmcn,#Eemn
        ret

nrdmm:  xrl     Wmcn,#Eemn
        ret

t_wr:   mov     A,Wmcn
        anl     A,#Wtdg
        jz      wt_wr
        ret

ama:    DB      'Yusak Al Mukhlas'
        DB      ' NIM: 00.17.000 '
        DB      'Pengukuran Berat'
        DB      'Metode Kapasitif'
r20k:   DB      ' 20 Karat /gram '
r21k:   DB      ' 21 Karat /gram '
r22k:   DB      ' 22 Karat /gram '
r23k:   DB      ' 23 Karat /gram '
r24k:   DB      ' 24 Karat /gram '
shrg:   DB      ' Masukkan Harga '
rbnr:   DB      '  Harga Benar?  '
r20k:   DB      '20 Karat    gram'
r21k:   DB      '21 Karat    gram'
r22k:   DB      '22 Karat    gram'
r23k:   DB      '23 Karat    gram'
r24k:   DB      '24 Karat    gram'
vrld:   DB      '  OVER LOAD !!  '
ngka:   DB      '0123456789 Rp.,-'
osong:  DB      '                '
```

ures

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ytes of In-System Reprogrammable Downloadable Flash Memory
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ogrammable I/O Lines
16-bit Timer/Counters
Interrupt Sources
rammable UART Serial Channel
ierial Interface
Power Idle and Power Down Modes
upt Recovery From Power Down
rammable Watchdog Timer
Data Pointer
r Off Flag

8-Bit Microcontroller with 8K Bytes Flash

AT89S8252

:ription

T89S8252 is a low-power, high-performance CMOS 8-bit microcomputer with es of Downloadable Flash programmable and erasable read only memory and es of EEPROM. The device is manufactured using Atmel's high density nonvol- emory technology and is compatible with the industry standard 80C51 instruc- t and pinout. The on-chip Downloadable Flash allows the program memory to ogrammed in-system through an SPI serial interface or by a conventional non- memory programmer. By combining a versatile 8-bit CPU with Downloadable n a monolithic chip, the Atmel AT89S8252 is a powerful microcomputer which s a highly flexible and cost effective solution to many embedded control appli-

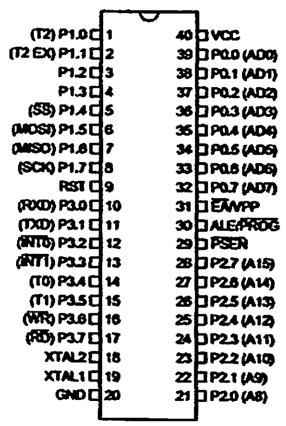
'89S8252 provides the following standard features: 8K bytes of Downloadable 2K bytes of EEPROM, 256 bytes of RAM, 32 I/O lines, programmable watch- ier, two Data Pointers, three 16-bit timer/counters, a six-vector two-level inter- chitecture, a full duplex serial port, on-chip oscillator, and clock circuitry. In 1, the AT89S8252 is designed with static logic for operation down to zero fre- and supports two software selectable power saving modes. The Idle Mode ne CPU while allowing the RAM, timer/counters, serial port, and interrupt sys- continue functioning. The Power Down Mode saves the RAM contents but the oscillator, disabling all other chip functions until the next interrupt or hard- set.

wnloadable Flash can be changed a single byte at a time and is accessible the SPI serial interface. Holding RESET active forces the SPI bus into a serial nming interface and allows the program memory to be written to or read from Lock Bit 2 has been activated.

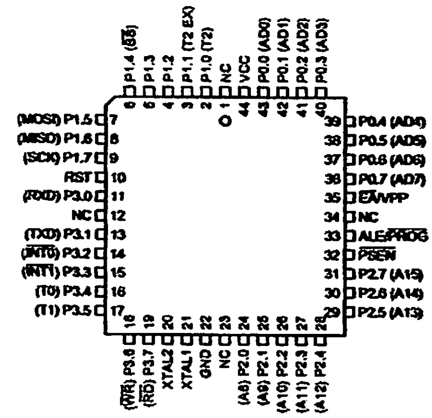
0401D-A-12/97

Configurations

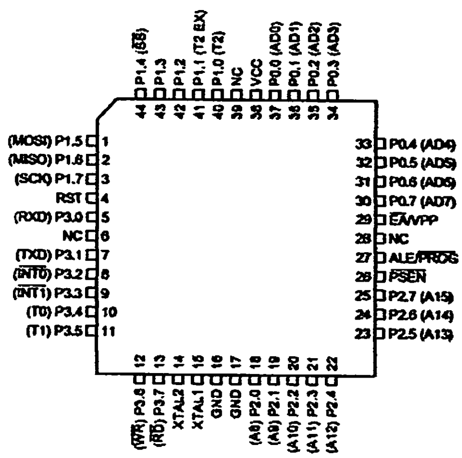
PDIP



PLCC



PQFP/TQFP



Description

voltage.

1.

is an 8-bit open drain bidirectional I/O port. As an port, each pin can sink eight TTL inputs. When 1s itten to port 0 pins, the pins can be used as high-ance inputs.

can also be configured to be the multiplexed low-address/data bus during accesses to external pro-nd data memory. In this mode, P0 has internal pul-

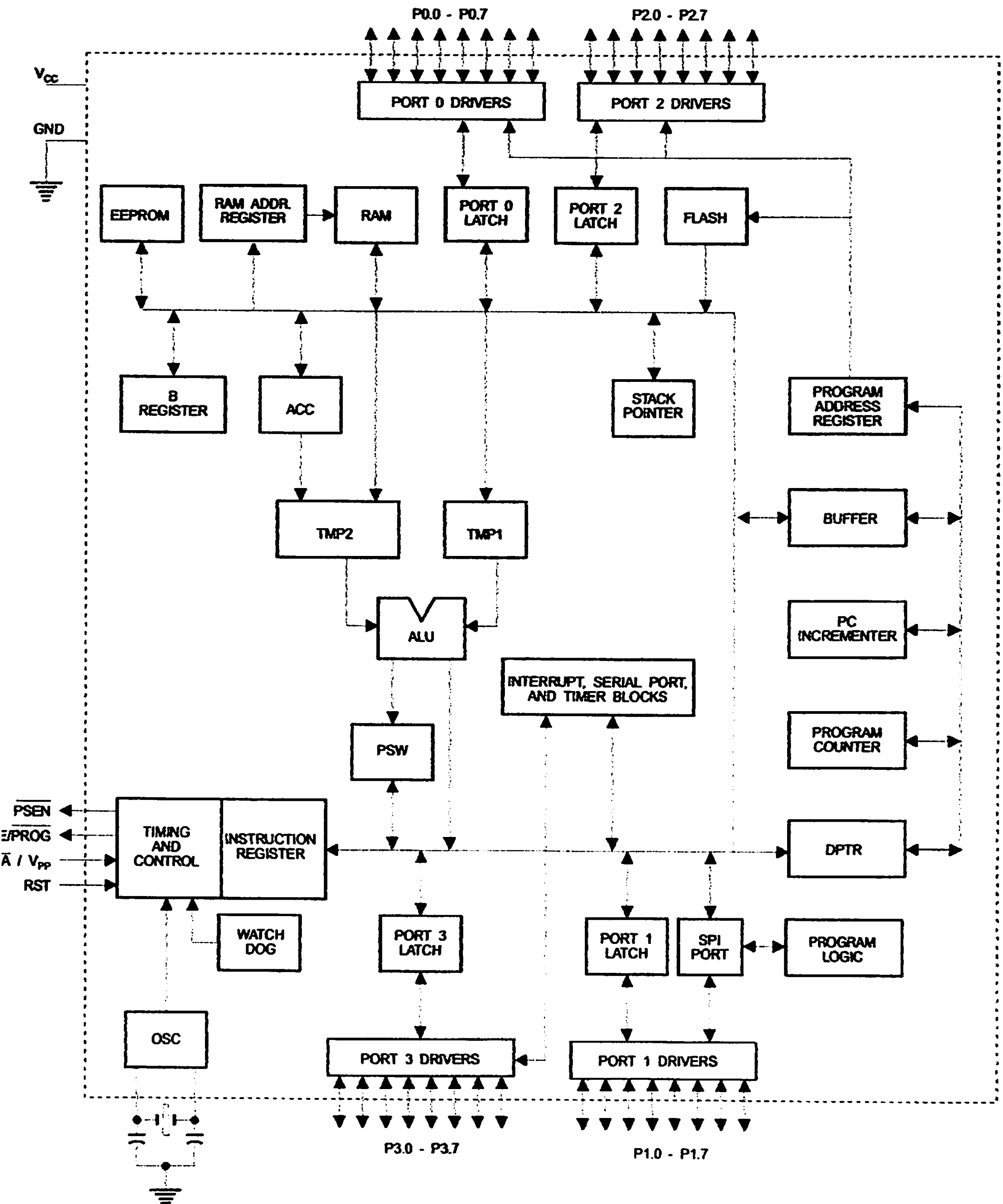
Port 0 also receives the code bytes during Flash programming and outputs the code bytes during program verification. External pullups are required during program verification.

Port 1

Port 1 is an 8-bit bidirectional I/O port with internal pullups. The Port 1 output buffers can sink/source four TTL inputs. When 1s are written to Port 1 pins, they are pulled high by the internal pullups and can be used as inputs. As inputs, Port 1 pins that are externally being pulled low will source current (I_{IL}) because of the internal pullups.

Some Port 1 pins provide additional functions. P1.0 and P1.1 can be configured to be the timer/counter 2 external count input (P1.0/T2) and the timer/counter 2 trigger input (P1.1/T2EX), respectively.

k Diagram


P0.0 - P0.7
P2.0 - P2.7
VCC
GND
PORT 0 DRIVERS
PORT 2 DRIVERS
EEPROM
RAM ADDR. REGISTER
RAM
PORT 0 LATCH
PORT 2 LATCH
FLASH
B REGISTER
ACC
STACK POINTER
PROGRAM ADDRESS REGISTER
BUFFER
TMP2
TMP1
ALU
PC INCREMENTER
INTERRUPT, SERIAL PORT, AND TIMER BLOCKS
PSW
PROGRAM COUNTER
PSEN
E/PROG
A / VPP
RST
TIMING AND CONTROL
INSTRUCTION REGISTER
DPTR
WATCH DOG
PORT 3 LATCH
PORT 1 LATCH
SPI PORT
PROGRAM LOGIC
OSC
PORT 3 DRIVERS
PORT 1 DRIVERS
P3.0 - P3.7
P1.0 - P1.7

nore, P1.4, P1.5, P1.6, and P1.7 can be configured
SPI slave port select, data input/output and shift
put/output pins as shown in the following table.

n	Alternate Functions
	T2 (external count input to Timer/Counter 2), clock-out
	T2EX (Timer/Counter 2 capture/reload trigger and direction control)
	$\overline{SS}$ (Slave port select input)
	MOSI (Master data output, slave data input pin for SPI channel)
	MISO (Master data input, slave data output pin for SPI channel)
	SCK (Master clock output, slave clock input pin for SPI channel)

ılso receives the low-order address bytes during
ogramming and verification.

; an 8-bit bidirectional I/O port with internal pullups.
t 2 output buffers can sink/source four TTL inputs.
s are written to Port 2 pins, they are pulled high by
nal pullups and can be used as inputs. As inputs,
ins that are externally being pulled low will source
I_{IL}) because of the internal pullups.

mits the high-order address byte during fetches
ternal program memory and during accesses to
data memory that use 16-bit addresses (MOVX @
In this application, Port 2 uses strong internal pul-
en emitting 1s. During accesses to external data
that use 8-bit addresses (MOVX @ RI), Port 2
e contents of the P2 Special Function Register.

lso receives the high-order address bits and some
signals during Flash programming and verification.

; an 8 bit bidirectional I/O port with internal pullups.
t 3 output buffers can sink/source four TTL inputs.
s are written to Port 3 pins, they are pulled high by
nal pullups and can be used as inputs. As inputs,
ins that are externally being pulled low will source
I_{IL}) because of the pullups.

lso serves the functions of various special features
T89S8252, as shown in the following table.

ılso receives some control signals for Flash pro-
ıg and verification.

Port Pin	Alternate Functions
P3.0	RXD (serial input port)
P3.1	TXD (serial output port)
P3.2	$\overline{INT0}$ (external interrupt 0)
P3.3	$\overline{INT1}$ (external interrupt 1)
P3.4	T0 (timer 0 external input)
P3.5	T1 (timer 1 external input)
P3.6	$\overline{WR}$ (external data memory write strobe)
P3.7	$\overline{RD}$ (external data memory read strobe)

RST

Reset input. A high on this pin for two machine cycles while the oscillator is running resets the device.

ALE/$\overline{PROG}$

Address Latch Enable is an output pulse for latching the low byte of the address during accesses to external memory. This pin is also the program pulse input ($\overline{PROG}$) during Flash programming.

In normal operation, ALE is emitted at a constant rate of 1/6 the oscillator frequency and may be used for external timing or clocking purposes. Note, however, that one ALE pulse is skipped during each access to external data memory.

If desired, ALE operation can be disabled by setting bit 0 of SFR location 8EH. With the bit set, ALE is active only during a MOVX or MOVC instruction. Otherwise, the pin is weakly pulled high. Setting the ALE-disable bit has no effect if the microcontroller is in external execution mode.

$\overline{PSEN}$

Program Store Enable is the read strobe to external program memory.

When the AT89S8252 is executing code from external program memory, $\overline{PSEN}$ is activated twice each machine cycle, except that two $\overline{PSEN}$ activations are skipped during each access to external data memory.

$\overline{EA}$/V_{PP}

External Access Enable. $\overline{EA}$ must be strapped to GND in order to enable the device to fetch code from external program memory locations starting at 0000H up to FFFFH. Note, however, that if lock bit 1 is programmed, $\overline{EA}$ will be internally latched on reset.

$\overline{EA}$ should be strapped to V_{CC} for internal program executions. This pin also receives the 12-volt programming enable voltage (V_{PP}) during Flash programming when 12-volt programming is selected.

o the inverting oscillator amplifier and input to the
l clock operating circuit.

from the inverting oscillator amplifier.

Special Function Registers

A map of the on-chip memory area called the Special Function Register (SFR) space is shown in Table 1.

Note that not all of the addresses are occupied, and unoccupied addresses may not be implemented on the chip. Read accesses to these addresses will in general return random data, and write accesses will have an indeterminate effect.

l. AT89S8252 SFR Map and Reset Values

								0FFH
B 00000000								0F7H
								0EFH
ACC 00000000								0E7H
								0DFH
PSW 00000000					SPCR 000001XX			0D7H
T2CON 00000000	T2MOD XXXXXX00	RCAP2L 00000000	RCAP2H 00000000	TL2 00000000	TH2 00000000			0CFH
								0C7H
IP XX000000								0BFH
P3 11111111								0B7H
IE 0X000000		SPSR 00XXXXXX						0AFH
P2 11111111								0A7H
SCON 00000000	SBUF XXXXXXXX							9FH
P1 11111111						WMCON 00000010		97H
TCON 00000000	TMOD 00000000	TL0 00000000	TL1 00000000	TH0 00000000	TH1 00000000			8FH
P0 11111111	SP 00000111	DP0L 00000000	DP0H 00000000	DP1L 00000000	DP1H 00000000	SPDR XXXXXXXX	PCON 0XXX0000	87H

software should not write 1s to these unlisted loca- , since they may be used in future products to invoke features. In that case, the reset or inactive values of the bits will always be 0.

ır 2 Registers Control and status bits are contained in ters T2CON (shown in Table 2) and T2MOD (shown in ɜ 9) for Timer 2. The register pair (RCAP2H, RCAP2L) ıe Capture/Reload registers for Timer 2 in 16 bit cap- node or 16-bit auto-reload mode.

:hdog and Memory Control Register The WMCON ıter contains control bits for the Watchdog Timer vn in Table 3). The EEMEN and EEMWE bits are used lect the 2K bytes on-chip EEPROM, and to enable write. The DPS bit selects one of two DPTR registers able.

SPI Registers Control and status bits for the Serial Peripheral Interface are contained in registers SPCR (shown in Table 4) and SPSR (shown in Table 5). The SPI data bits are contained in the SPDR register. Writing the SPI data register during serial data transfer sets the Write Collision bit, WCOL, in the SPSR register. The SPDR is double buffered for writing and the values in SPDR are not changed by Reset.

Interrupt Registers The global interrupt enable bit and the individual interrupt enable bits are in the IE register. In addition, the individual interrupt enable bit for the SPI is in the SPCR register. Two priorities can be set for each of the six interrupt sources in the IP register.

ı 2. T2CON—Timer/Counter 2 Control Register

ON Address = 0C8H Reset Value = 0000 0000B

ıddressable

TF2	EXF2	RCLK	TCLK	EXEN2	TR2	$C/\overline{T2}$	$CP/\overline{RL2}$
7	6	5	4	3	2	1	0

ıbol	Function
	Timer 2 overflow flag set by a Timer 2 overflow and must be cleared by software. TF2 will not be set when either RCLK = 1 or TCLK = 1.
2	Timer 2 external flag set when either a capture or reload is caused by a negative transition on T2EX and EXEN2 = 1. When Timer 2 interrupt is enabled, EXF2 = 1 will cause the CPU to vector to the Timer 2 interrupt routine. EXF2 must be cleared by software. EXF2 does not cause an interrupt in up/down counter mode (DCEN = 1).
K	Receive clock enable. When set, causes the serial port to use Timer 2 overflow pulses for its receive clock in serial port Modes 1 and 3. RCLK = 0 causes Timer 1 overflows to be used for the receive clock.
K	Transmit clock enable. When set, causes the serial port to use Timer 2 overflow pulses for its transmit clock in serial port Modes 1 and 3. TCLK = 0 causes Timer 1 overflows to be used for the transmit clock.
N2	Timer 2 external enable. When set, allows a capture or reload to occur as a result of a negative transition on T2EX if Timer 2 is not being used to clock the serial port. EXEN2 = 0 causes Timer 2 to ignore events at T2EX.
	Start/Stop control for Timer 2. TR2 = 1 starts the timer.
;	Timer or counter select for Timer 2. $C/\overline{T2}$ = 0 for timer function. $C/\overline{T2}$ = 1 for external event counter (falling edge triggered).
$\overline{RL2}$	Capture/Reload select. $CP/\overline{RL2}$ = 1 causes captures to occur on negative transitions at T2EX if EXEN2 = 1. $CP/\overline{RL2}$ = 0 causes automatic reloads to occur when Timer 2 overflows or negative transitions occur at T2EX when EXEN2 = 1. When either RCLK or TCLK = 1, this bit is ignored and the timer is forced to auto-reload on Timer 2 overflow.

Data Pointer Registers To facilitate accessing both al EEPROM and external data memory, two banks of : Data Pointer Registers are provided: DP0 at SFR ss locations 82H-83H and DP1 at 84H-85H. Bit DPS ı SFR WMCON selects DP0 and DPS = 1 selects The user should always initialize the DPS bit to the appropriate value before accessing the respective Data Pointer Register.

Power Off Flag The Power Off Flag (POF) is located at bit_4 (PCON.4) in the PCON SFR. POF is set to "1" during power up. It can be set and reset under software control and is not affected by RESET.

3. WMCON—Watchdog and Memory Control Register

:ON Address = 96H — Reset Value = 0000 0010B

PS2	PS1	PS0	EEMWE	EEMEN	DPS	WDTRST	WDTEN
7	6	5	4	3	2	1	0

bol	Function
	Prescaler Bits for the Watchdog Timer. When all three bits are set to "0", the watchdog timer has a nominal period of 16 ms. When all three bits are set to "1", the nominal period is 2048 ms.
WE	EEPROM Data Memory Write Enable Bit. Set this bit to "1" before initiating byte write to on-chip EEPROM with the MOVX instruction. User software should set this bit to "0" after EEPROM write is completed.
EN	Internal EEPROM Access Enable. When EEMEN = 1, the MOVX instruction with DPTR will access on-chip EEPROM instead of external data memory. When EEMEN = 0, MOVX with DPTR accesses external data memory.
	Data Pointer Register Select. DPS = 0 selects the first bank of Data Pointer Register, DP0, and DPS = 1 selects the second bank, DP1
RST $\overline{\text{BSY}}$	Watchdog Timer Reset and EEPROM Ready/$\overline{\text{Busy}}$ Flag. Each time this bit is set to "1" by user software, a pulse is generated to reset the watchdog timer. The WDTRST bit is then automatically reset to "0" in the next instruction cycle. The WDTRST bit is Write-Only. This bit also serves as the RDY/$\overline{\text{BSY}}$ flag in a Read-Only mode during EEPROM write. RDY/$\overline{\text{BSY}}$ = 1 means that the EEPROM is ready to be programmed. While programming operations are being executed, the RDY/$\overline{\text{BSY}}$ bit equals "0" and is automatically reset to "1" when programming is completed.
EN	Watchdog Timer Enable Bit. WDTEN = 1 enables the watchdog timer and WDTEN = 0 disables the watchdog timer.

4. SPCR—SPI Control Register

R Address = D5H   Reset Value = 0000 01XXB

SPIE	SPE	DORD	MSTR	CPOL	CPHA	SPR1	SPR0
7	6	5	4	3	2	1	0

bol	Function
	SPI Interrupt Enable. This bit, in conjunction with the ES bit in the IE register, enables SPI interrupts: SPIE = 1 and ES = 1 enable SPI interrupts. SPIE = 0 disables SPI interrupts.
	SPI Enable. SPI = 1 enables the SPI channel and connects $\overline{SS}$, MOSI, MISO and SCK to pins P1.4, P1.5, P1.6, and P1.7. SPI = 0 disables the SPI channel.
D	Data Order. DORD = 1 selects LSB first data transmission. DORD = 0 selects MSB first data transmission.
R	Master/Slave Select. MSTR = 1 selects Master SPI mode. MSTR = 0 selects Slave SPI mode.
-	Clock Polarity. When CPOL = 1, SCK is high when idle. When CPOL = 0, SCK of the master device is low when not transmitting. Please refer to figure on SPI Clock Phase and Polarity Control.
A	Clock Phase. The CPHA bit together with the CPOL bit controls the clock and data relationship between master and slave. Please refer to figure on SPI Clock Phase and Polarity Control.
) |	SPI Clock Rate Select. These two bits control the SCK rate of the device configured as master. SPR1 and SPR0 have no effect on the slave. The relationship between SCK and the oscillator frequency, $F_{OSC.}$, is as follows: SPR1 SPR0 SCK = $F_{OSC.}$ divided by 0 0 4 0 1 16 1 0 64 1 1 128

5. SPSR—SPI Status Register

R Address = AAH   Reset Value = 00XX XXXXB

SPIF	WCOL	—	—	—	—	—	—
7	6	5	4	3	2	1	0

ol	Function
	SPI Interrupt Flag. When a serial transfer is complete, the SPIF bit is set and an interrupt is generated if SPIE = 1 and ES = 1. The SPIF bit is cleared by reading the SPI status register with SPIF and WCOL bits set, and then accessing the SPI data register.
L	Write Collision Flag. The WCOL bit is set if the SPI data register is written during a data transfer. During data transfer, the result of reading the SPDR register may be incorrect, and writing to it has no effect. The WCOL bit (and the SPIF bit) are cleared by reading the SPI status register with SPIF and WCOL set, and then accessing the SPI data register.

. SPDR—SPI Data Register

Address = 86H Reset Value = unchanged

SPD7	SPD6	SPD5	SPD4	SPD3	SPD2	SPD1	SPD0
7	6	5	4	3	2	1	0

Memory—EEPROM and RAM

89S8252 implements 2K bytes of on-chip EEPROM a storage and 256 bytes of RAM. The upper 128 f RAM occupy a parallel space to the Special Func- gisters. That means the upper 128 bytes have the ddresses as the SFR space but are physically sepa- n SFR space.

in instruction accesses an internal location above s 7FH, the address mode used in the instruction s whether the CPU accesses the upper 128 bytes l or the SFR space. Instructions that use direct ing access SFR space.

imple, the following direct addressing instruction es the SFR at location 0A0H (which is P2).

```
0A0H, #data
```

ions that use indirect addressing access the upper tes of RAM. For example, the following indirect ing instruction, where R0 contains 0A0H, accesses a byte at address 0A0H, rather than P2 (whose is 0A0H).

```
@R0, #data
```

iat stack operations are examples of indirect ing, so the upper 128 bytes of data RAM are avail- stack space.

chip EEPROM data memory is selected by setting MEN bit in the WMCON register at SFR address 96H. The EEPROM address range is from 000H to The MOVX instructions are used to access the M. To access off-chip data memory with the MOVX ons, the EEMEN bit needs to be set to "0".

MWE bit in the WMCON register needs to be set to re any byte location in the EEPROM can be written. ftware should reset EEMWE bit to "0" if no further M write is required. EEPROM write cycles in the ogramming mode are self-timed and typically take The progress of EEPROM write can be monitored ing the RDY/$\overline{BSY}$ bit (read-only) in SFR WMCON. $\overline{SY}$ = 0 means programming is still in progress and $\overline{SY}$ = 1 means EEPROM write cycle is completed ither write cycle can be initiated.

ion, during EEPROM programming, an attempted m the EEPROM will fetch the byte being written MSB complemented. Once the write cycle is com- rue data are valid at all bit locations.

Programmable Watchdog Timer

The programmable Watchdog Timer (WDT) operates from an independent oscillator. The prescaler bits, PS0, PS1 and PS2 in SFR WMCON are used to set the period of the Watchdog Timer from 16 ms to 2048 ms. The available timer periods are shown in the following table and the actual timer periods (at V_{CC} = 5V) are within ±30% of the nominal.

The WDT is disabled by Power-on Reset and during Power Down. It is enabled by setting the WDTEN bit in SFR WMCON (address = 96H). The WDT is reset by setting the WDTRST bit in WMCON. When the WDT times out without being reset or disabled, an internal RST pulse is generated to reset the CPU.

Table 7. Watchdog Timer Period Selection

WDT Prescaler Bits			Period (nominal)
PS2	PS1	PS0	
0	0	0	16 ms
0	0	1	32 ms
0	1	0	64 ms
0	1	1	128 ms
1	0	0	256 ms
1	0	1	512 ms
1	1	0	1024 ms
1	1	1	2048 ms

er 0 and 1

0 and Timer 1 in the AT89S8252 operate the same s Timer 0 and Timer 1 in the AT89C51, AT89C52 and :55. For further information, see the October 1995 controller Data Book, page 2-45, section titled, r/Counters."

er 2

2 is a 16 bit Timer/Counter that can operate as either er or an event counter. The type of operation is ed by bit C/$\overline{T2}$ in the SFR T2CON (shown in Table 2). 2 has three operating modes: capture, auto-reload down counting), and baud rate generator. The s are selected by bits in T2CON, as shown in Table 8.

2 consists of two 8-bit registers, TH2 and TL2. In the function, the TL2 register is incremented every ne cycle. Since a machine cycle consists of 12 oscil- eriods, the count rate is 1/12 of the oscillator fre- y.

Counter function, the register is incremented in nse to a 1-to-0 transition at its corresponding external pin, T2. In this function, the external input is sampled S5P2 of every machine cycle. When the samples a high in one cycle and a low in the next cycle, the is incremented. The new count value appears in the er during S3P1 of the cycle following the one in which nsition was detected. Since two machine cycles (24 tor periods) are required to recognize a 1-to-0 transi- he maximum count rate is 1/24 of the oscillator fre- y. To ensure that a given level is sampled at least efore it changes, the level should be held for at least ll machine cycle.

Table 8. Timer 2 Operating Modes

RCLK + TCLK	CP/$\overline{RL2}$	TR2	MODE
0	0	1	16-bit Auto-Reload
0	1	1	16-bit Capture
1	X	1	Baud Rate Generator
X	X	0	(Off)

Capture Mode

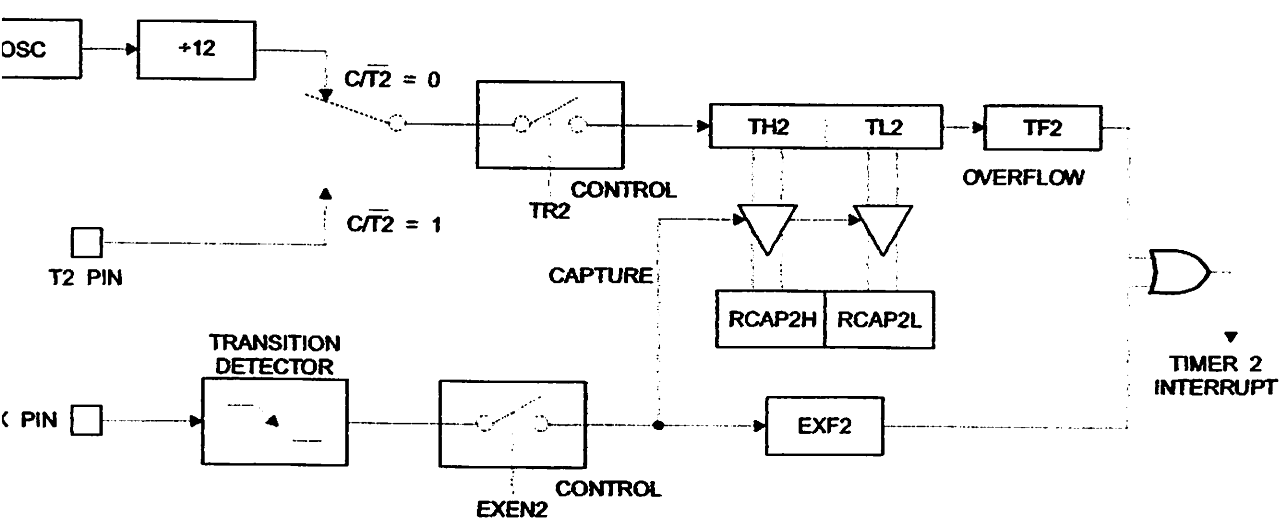
In the capture mode, two options are selected by bit EXEN2 in T2CON. If EXEN2 = 0, Timer 2 is a 16 bit timer or counter which upon overflow sets bit TF2 in T2CON. This bit can then be used to generate an interrupt. If EXEN2 = 1, Timer 2 performs the same operation, but a 1-to-0 transition at external input T2EX also causes the current value in TH2 and TL2 to be captured into RCAP2H and RCAP2L, respectively. In addition, the transition at T2EX causes bit EXF2 in T2CON to be set. The EXF2 bit, like TF2, can generate an interrupt. The capture mode is illustrated in Figure 1.

Auto-Reload (Up or Down Counter)

Timer 2 can be programmed to count up or down when configured in its 16 bit auto-reload mode. This feature is invoked by the DCEN (Down Counter Enable) bit located in the SFR T2MOD (see Table 9). Upon reset, the DCEN bit is set to 0 so that timer 2 will default to count up. When DCEN is set, Timer 2 can count up or down, depending on the value of the T2EX pin.

Figure 2 shows Timer 2 automatically counting up when DCEN = 0. In this mode, two options are selected by bit EXEN2 in T2CON. If EXEN2 = 0, Timer 2 counts up to

1. Timer 2 in Capture Mode



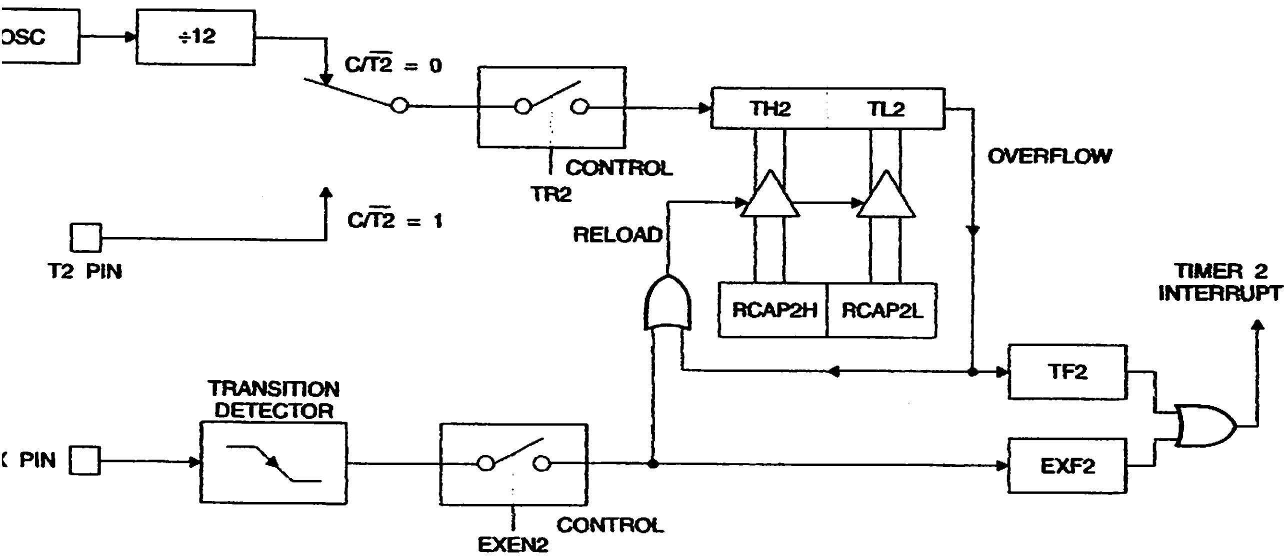
ᐧH and then sets the TF2 bit upon overflow. The over- lso causes the timer registers to be reloaded with the : value in RCAP2H and RCAP2L. The values in 2H and RCAP2L are preset by software. If EXEN2 = 5 bit reload can be triggered either by an overflow or -to-0 transition at external input T2EX. This transition ets the EXF2 bit. Both the TF2 and EXF2 bits can ate an interrupt if enabled.

g the DCEN bit enables Timer 2 to count up or down, own in Figure 3. In this mode, the T2EX pin controls ection of the count. A logic 1 at T2EX makes Timer 2 up. The timer will overflow at 0FFFFH and set the it. This overflow also causes the 16 bit value in RCAP2H and RCAP2L to be reloaded into the timer registers, TH2 and TL2, respectively.

A logic 0 at T2EX makes Timer 2 count down. The timer underflows when TH2 and TL2 equal the values stored in RCAP2H and RCAP2L. The underflow sets the TF2 bit and causes 0FFFFH to be reloaded into the timer registers.

The EXF2 bit toggles whenever Timer 2 overflows or underflows and can be used as a 17th bit of resolution. In this operating mode, EXF2 does not flag an interrupt.

ᐧ 2. Timer 2 in Auto Reload Mode (DCEN = 0)



9. T2MOD—Timer 2 Mode Control Register

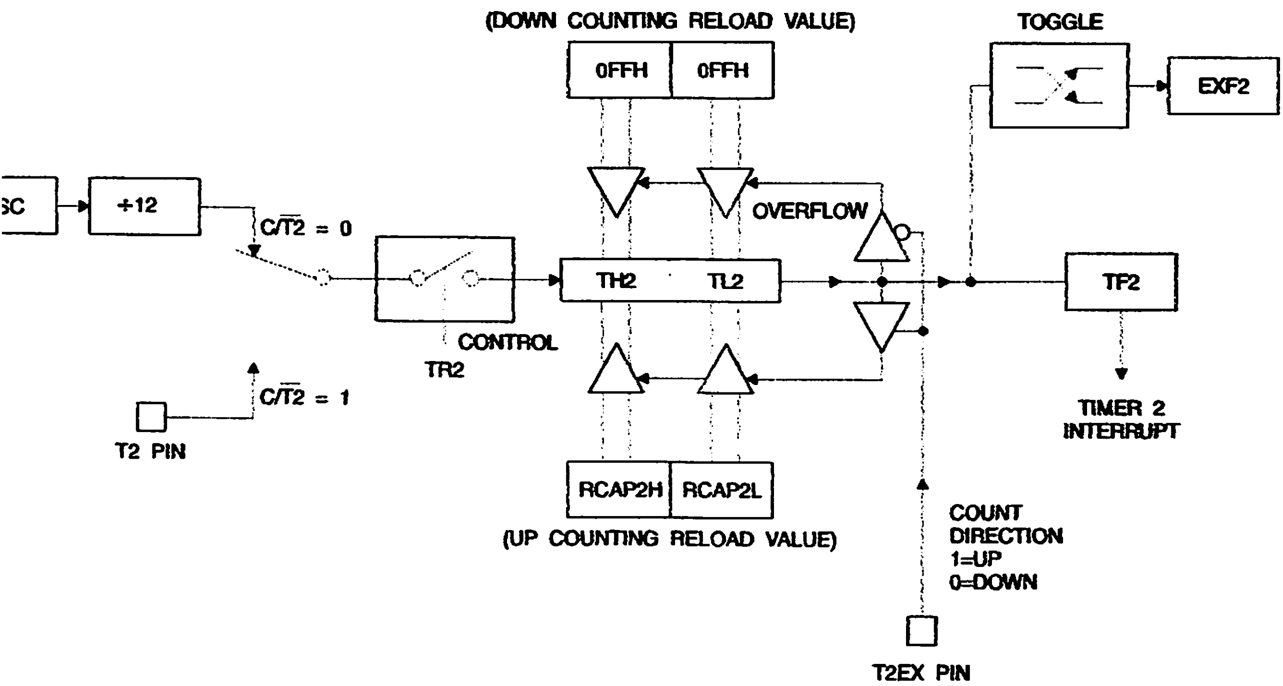
ᐧD Address = 0C9H — Reset Value = XXXX XX00B

it Addressable

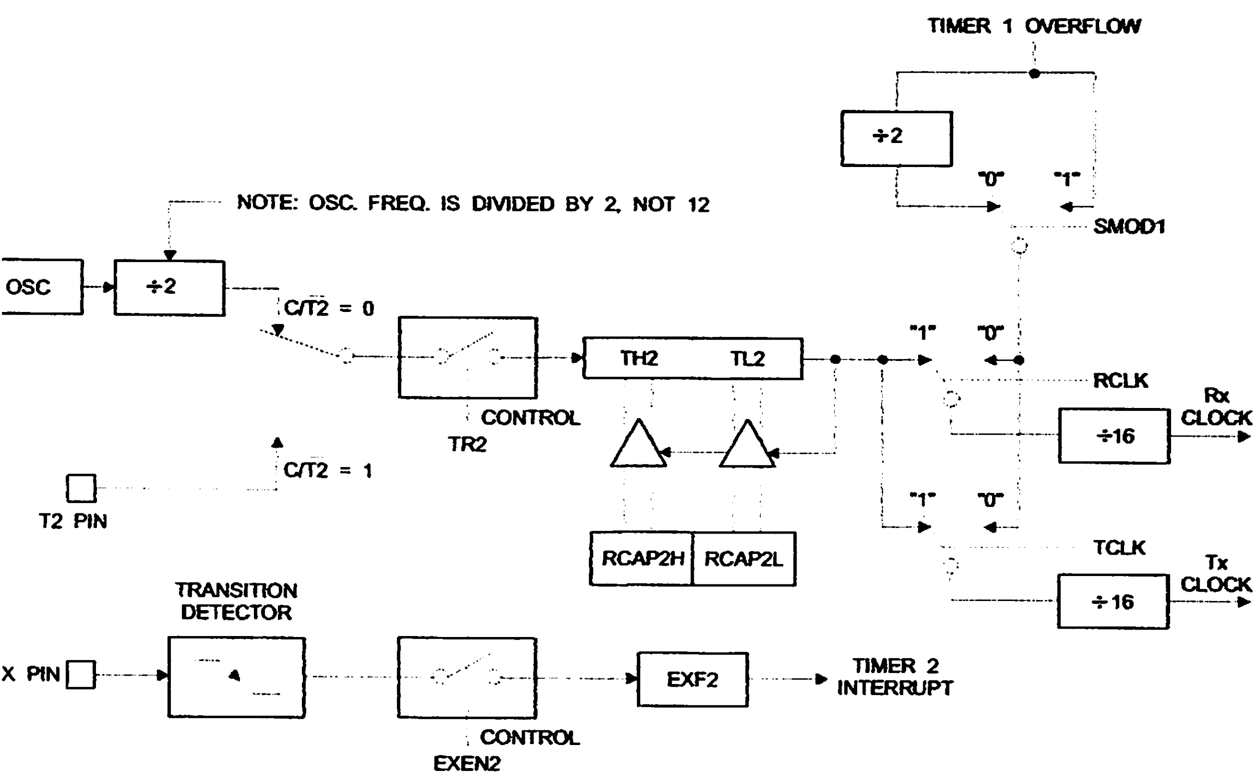
—	—	—	—	—	—	T2OE	DCEN
7	6	5	4	3	2	1	0

ᐧol	Function
	Not implemented, reserved for future use.
:	Timer 2 Output Enable bit.
ᐧ	When set, this bit allows Timer 2 to be configured as an up/down counter.

3. Timer 2 Auto Reload Mode (DCEN = 1)



4. Timer 2 in Baud Rate Generator Mode



Rate Generator

is selected as the baud rate generator by setting nd/or RCLK in T2CON (Table 2). Note that the baud r transmit and receive can be different if Timer 2 is the receiver or transmitter and Timer 1 is used for r function. Setting RCLK and/or TCLK puts Timer 2 aud rate generator mode, as shown in Figure 4.

d rate generator mode is similar to the auto-reload that a rollover in TH2 causes the Timer 2 registers loaded with the 16 bit value in registers RCAP2H AP2L, which are preset by software.

d rates in Modes 1 and 3 are determined by Timer flow rate according to the following equation.

$$\text{s 1 and 3 Baud Rates} = \frac{\text{Timer 2 Overflow Rate}}{16}$$

ner can be configured for either timer or counter on. In most applications, it is configured for timer n (CP/$\overline{\text{T2}}$ = 0). The timer operation is different for when it is used as a baud rate generator. Normally, er, it increments every machine cycle (at 1/12 the r frequency). As a baud rate generator, however, it ents every state time (at 1/2 the oscillator fre-). The baud rate formula is given below.

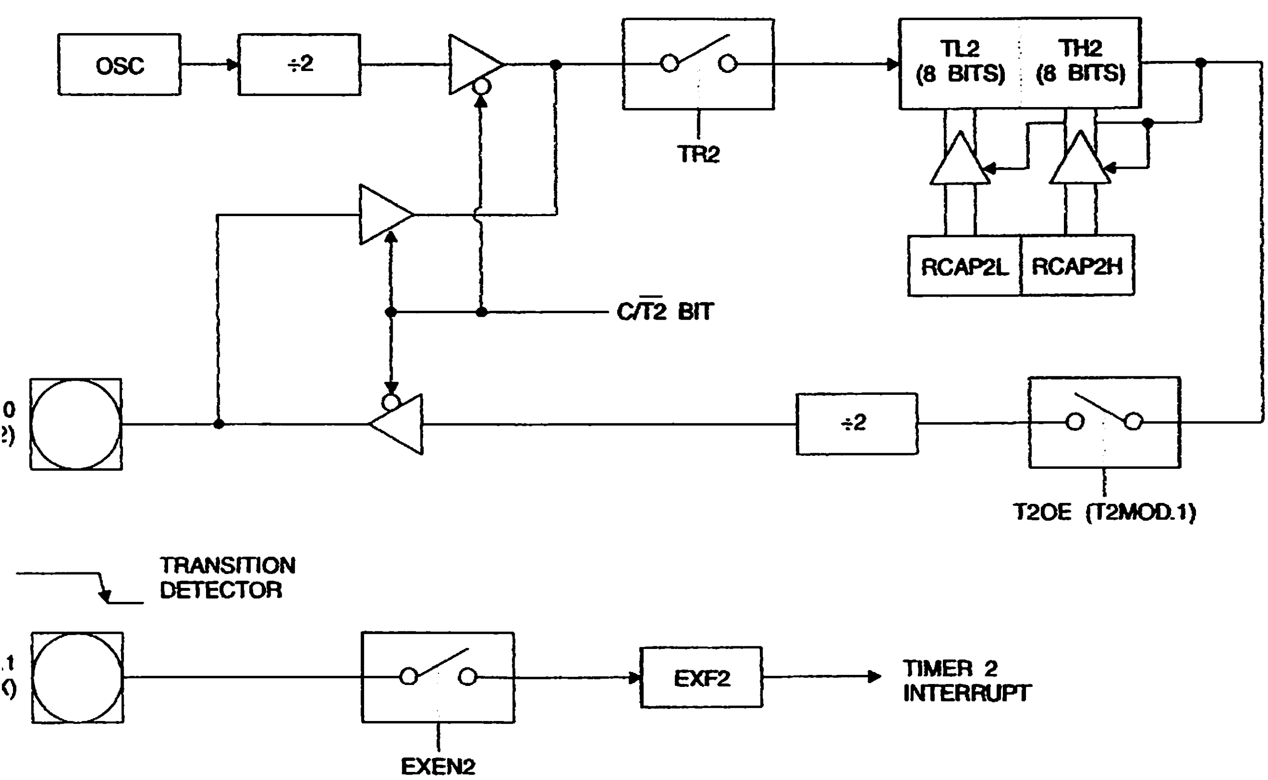
$$\frac{\text{Modes 1 and 3}}{\text{Baud Rate}} = \frac{\text{Oscillator Frequency}}{32 \times [65536 - (\text{RCAP2H,RCAP2L})]}$$

where (RCAP2H, RCAP2L) is the content of RCAP2H and RCAP2L taken as a 16 bit unsigned integer.

Timer 2 as a baud rate generator is shown in Figure 4. This figure is valid only if RCLK or TCLK = 1 in T2CON. Note that a rollover in TH2 does not set TF2 and will not generate an interrupt. Note too, that if EXEN2 is set, a 1-to-0 transition in T2EX will set EXF2 but will not cause a reload from (RCAP2H, RCAP2L) to (TH2, TL2). Thus when Timer 2 is in use as a baud rate generator, T2EX can be used as an extra external interrupt.

Note that when Timer 2 is running (TR2 = 1) as a timer in the baud rate generator mode, TH2 or TL2 should not be read from or written to. Under these conditions, the Timer is incremented every state time, and the results of a read or write may not be accurate. The RCAP2 registers may be read but should not be written to, because a write might overlap a reload and cause write and/or reload errors. The timer should be turned off (clear TR2) before accessing the Timer 2 or RCAP2 registers.

5. Timer 2 in Clock-Out Mode



rammable Clock Out

ı duty cycle clock can be programmed to come out on as shown in Figure 5. This pin, besides being a regu-) pin, has two alternate functions. It can be pro- ned to input the external clock for Timer/Counter 2 or put a 50% duty cycle clock ranging from 61 Hz to 4 ıt a 16 MHz operating frequency.

nfigure the Timer/Counter 2 as a clock generator, bit T2CON.1) must be cleared and bit T2OE (T2MOD.1) ɔe set. Bit TR2 (T2CON.2) starts and stops the timer.

lock-out frequency depends on the oscillator fre- y and the reload value of Timer 2 capture registers ᵓ2H, RCAP2L), as shown in the following equation.

$$\text{ck Out Frequency} = \frac{\text{Oscillator Frequency}}{4 \times [65536 - (\text{RCAP2H,RCAP2L})]}$$

clock-out mode, Timer 2 rollovers will not generate errupt. This behavior is similar to when Timer 2 is ıs a baud-rate generator. It is possible to use Timer 2 ɩaud-rate generator and a clock generator simulta- ly. Note, however, that the baud-rate and clock-out ıncies cannot be determined independently from one ɜr since they both use RCAP2H and RCAP2L.

UART

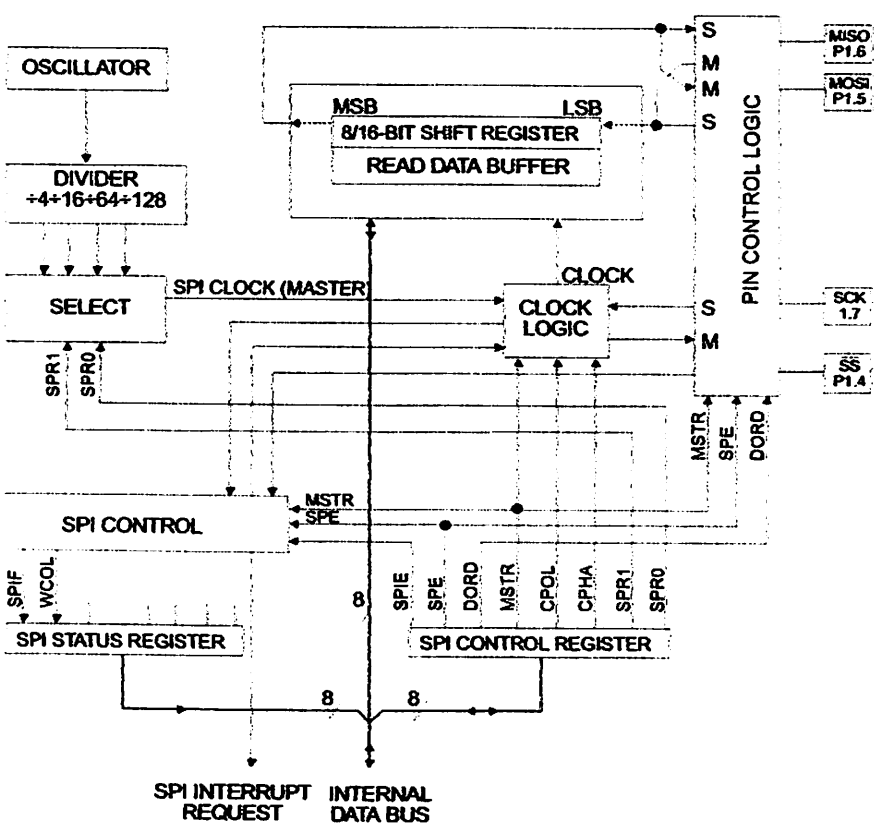
The UART in the AT89S8252 operates the same way as the UART in the AT89C51, AT89C52 and AT89C55. For further information, see the October 1995 Microcontroller Data Book, page 2-49, section titled, "Serial Interface."

Serial Peripheral Interface

The serial peripheral interface (SPI) allows high-speed synchronous data transfer between the AT89S8252 and peripheral devices or between several AT89S8252 devices. The AT89S8252 SPI features include the following:

- Full-Duplex, 3-Wire Synchronous Data Transfer
- Master or Slave Operation
- 1.5-MHz Bit Frequency (max.)
- LSB First or MSB First Data Transfer
- Four Programmable Bit Rates
- End of Transmission Interrupt Flag
- Write Collision Flag Protection
- Wakeup from Idle Mode (Slave Mode Only)

› 6. SPI Block Diagram

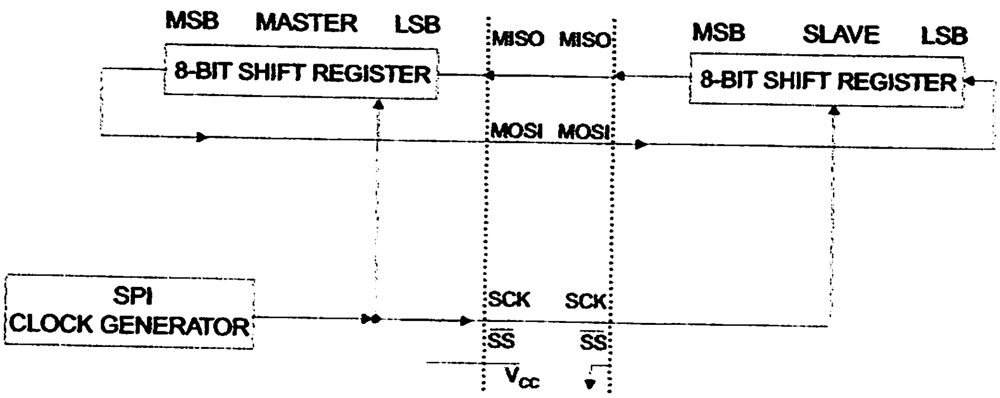


nterconnection between master and slave CPUs with s shown in the following figure. The SCK pin is the output in the master mode but is the clock input in the mode. Writing to the SPI data register of the master starts the SPI clock generator, and the data written ; out of the MOSI pin and into the MOSI pin of the CPU. After shifting one byte, the SPI clock generator ·, setting the end of transmission flag (SPIF). If both PI interrupt enable bit (SPIE) and the serial port inter- nable bit (ES) are set, an interrupt is requested.

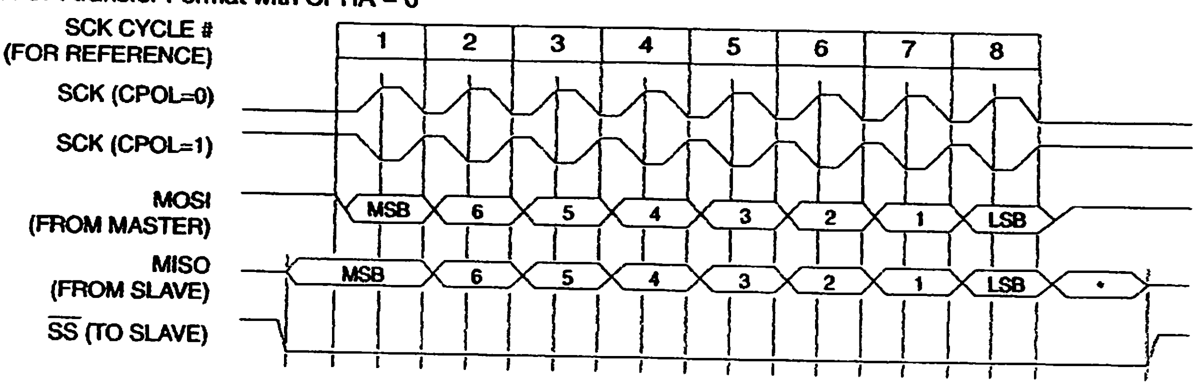
The Slave Select input, $\overline{SS}$/P1.4, is set low to select an individual SPI device as a slave. When $\overline{SS}$/P1.4 is set high, the SPI port is deactivated and the MOSI/P1.5 pin can be used as an input.

There are four combinations of SCK phase and polarity with respect to serial data, which are determined by control bits CPHA and CPOL. The SPI data transfer formats are shown in Figures 8 and 9.

e 7. SPI Master-Slave Interconnection

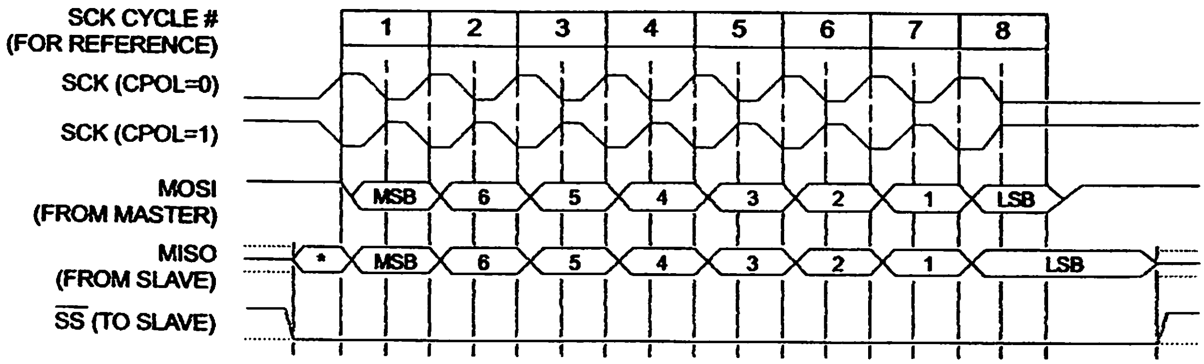


› 8. SPI transfer Format with CPHA = 0



›fined but normally MSB of character just received

ꞏ 9. SPI Transfer Format with CPHA = 1



əfined but normally LSB of previously transmitted character

rupts

T89S8252 has a total of six interrupt vectors: two al interrupts ($\overline{INT0}$ and $\overline{INT1}$), three timer interrupts s 0, 1, and 2), and the serial port interrupt. These pts are all shown in Figure 10.

ıf these interrupt sources can be individually enabled ıbled by setting or clearing a bit in Special Function ər IE. IE also contains a global disable bit, EA, which ıs all interrupts at once.

ıat Table 10 shows that bit position IE.6 is unimple- ɨ. In the AT89C51, bit position IE.5 is also unimple- ɨ. User software should not write 1s to these bit posi- ɪince they may be used in future AT89 products.

Timer 2 interrupt is generated by the logical OR of bits TF2 and EXF2 in register T2CON. Neither of these flags is cleared by hardware when the service routine is vectored to. In fact, the service routine may have to determine whether it was TF2 or EXF2 that generated the interrupt, and that bit will have to be cleared in software.

The Timer 0 and Timer 1 flags, TF0 and TF1, are set at S5P2 of the cycle in which the timers overflow. The values are then polled by the circuitry in the next cycle. However, the Timer 2 flag, TF2, is set at S2P2 and is polled in the same cycle in which the timer overflows.

l0. Interrupt Enable (IE) Register

							(LSB)
A	—	ET2	ES	ET1	EX1	ET0	EX0

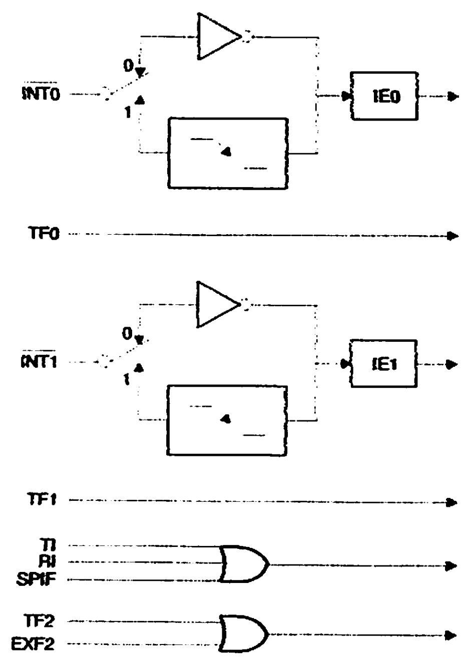
ɪnable Bit = 1 enables the interrupt.

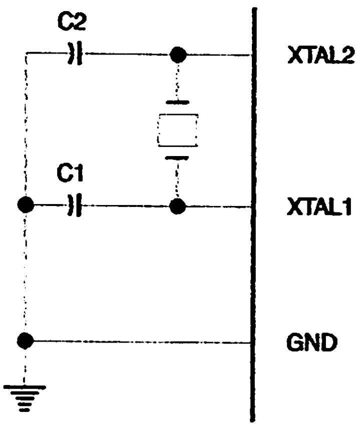
ɪnable Bit = 0 disables the interrupt.

ɔl	Position	Function
	IE.7	Disables all interrupts. If EA = 0, no interrupt is acknowledged. If EA = 1, each interrupt source is individually enabled or disabled by setting or clearing its enable bit.
	IE.6	Reserved.
	IE.5	Timer 2 interrupt enable bit.
	IE.4	SPI and UART interrupt enable bit.
	IE.3	Timer 1 interrupt enable bit.
	IE.2	External interrupt 1 enable bit.
	IE.1	Timer 0 interrupt enable bit.
	IE.0	External interrupt 0 enable bit.

ɔftware should never write 1s to unimplemented bits, because əy be used in future AT89 products.

Figure 10. Interrupt Sources





11. Oscillator Connections

Note: C1, C2 = 30 pF ± 10 pF for Crystals
= 40 pF ± 10 pF for Ceramic Resonators

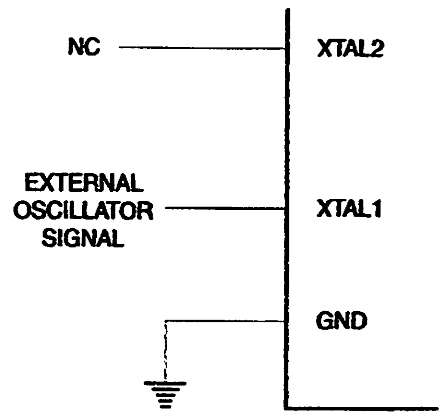


Figure 12. External Clock Drive Configuration

illator Characteristics

and XTAL2 are the input and output, respectively, nverting amplifier that can be configured for use as chip oscillator, as shown in Figure 11. Either a quartz l or ceramic resonator may be used. To drive the from an external clock source, XTAL2 should be left nected while XTAL1 is driven, as shown in Figure 12. are no requirements on the duty cycle of the external ignal, since the input to the internal clocking circuitry ugh a divide-by-two flip-flop, but minimum and maxi- voltage high and low time specifications must be ed.

Mode

mode, the CPU puts itself to sleep while all the on- eripherals remain active. The mode is invoked by re. The content of the on-chip RAM and all the spe- nctions registers remain unchanged during this The idle mode can be terminated by any enabled ot or by a hardware reset.

hat when idle mode is terminated by a hardware the device normally resumes program execution here it left off, up to two machine cycles before the internal reset algorithm takes control. On-chip hardware inhibits access to internal RAM in this event, but access to the port pins is not inhibited. To eliminate the possibility of an unexpected write to a port pin when idle mode is terminated by a reset, the instruction following the one that invokes idle mode should not write to a port pin or to external memory.

Power Down Mode

In the power down mode, the oscillator is stopped and the instruction that invokes power down is the last instruction executed. The on-chip RAM and Special Function Registers retain their values until the power down mode is terminated. Exit from power down can be initiated either by a hardware reset or by an enabled external interrupt. Reset redefines the SFRs but does not change the on-chip RAM. The reset should not be activated before V_{CC} is restored to its normal operating level and must be held active long enough to allow the oscillator to restart and stabilize.

To exit power down via an interrupt, the external interrupt must be enabled as level sensitive before entering power down. The interrupt service routine starts at 16 ms (nominal) after the enabled interrupt pin is activated.

ıs of External Pins During Idle and Power Down Modes

	Program Memory	ALE	PSEN	PORT0	PORT1	PORT2	PORT3
	Internal	1	1	Data	Data	Data	Data
	External	1	1	Float	Data	Address	Data
Down	Internal	0	0	Data	Data	Data	Data
Down	External	0	0	Float	Data	Data	Data

ram Memory Lock Bits

89S8252 has three lock bits that can be left unpro-ed (U) or can be programmed (P) to obtain the addi-eatures listed in the following table.

ock bit 1 is programmed, the logic level at the $\overline{EA}$ pin pled and latched during reset. If the device is pow-p without a reset, the latch initializes to a random value and holds that value until reset is activated. The latched value of $\overline{EA}$ must agree with the current logic level at that pin in order for the device to function properly.

Once programmed, the lock bits can only be unprogrammed with the Chip Erase operations in either the parallel or serial modes.

Bit Protection Modes(1)(2)

ogram Lock Bits			Protection Type
LB1	LB2	LB3	
U	U	U	No internal memory lock feature.
P	U	U	MOVC instructions executed from external program memory are disabled from fetching code bytes from internal memory. $\overline{EA}$ is sampled and latched on reset and further programming of the Flash memory (parallel or serial mode) is disabled.
P	P	U	Same as Mode 2, but parallel or serial verify are also disabled.
P	P	P	Same as Mode 3, but external execution is also disabled.

1. U = Unprogrammed
2. P = Programmed

ramming the Flash and EEPROM

AT89S8252 Flash Microcontroller offers 8K bytes stem reprogrammable Flash Code memory and 2K f EEPROM Data memory.

89S8252 is normally shipped with the on-chip Flash nd EEPROM Data memory arrays in the erased .e. contents = FFH) and ready to be programmed. evice supports a High-Voltage (12V) Parallel pro-ing mode and a Low-Voltage (5V) Serial program-ode. The serial programming mode provides a con-way to download the AT89S8252 inside the user's . The parallel programming mode is compatible with tional third party Flash or EPROM programmers.

de and Data memory arrays are mapped via sepa-dress spaces in the serial programming mode. In allel programming mode, the two arrays occupy one ous address space: 0000H to 1FFFH for the Code nd 2000H to 27FFH for the Data array.

de and Data memory arrays on the AT89S8252 are nmed byte-by-byte in either programming mode. An ase cycle is provided with the self-timed program-peration in the serial programming mode. There is d to perform the Chip Erase operation to reprogram emory location in the serial programming mode any of the lock bits have been programmed.

arallel programming mode, there is no auto-erase o reprogram any non-blank byte, the user needs to Chip Erase operation first to erase both arrays.

Parallel Programming Algorithm

To program and verify the AT89S8252 in the parallel programming mode, the following sequence is recommended:

1. Power-up sequence:

   Apply power between V_{CC} and GND pins.

   Set RST pin to "H".

   Apply a 3 MHz to 24 MHz clock to XTAL1 pin and wait for at least 10 milliseconds.
2. Set $\overline{PSEN}$ pin to "L"

   ALE pin to "H"

   $\overline{EA}$ pin to "H" and all other pins to "H".
3. Apply the appropriate combination of "H" or "L" logic levels to pins P2.6, P2.7, P3.6, P3.7 to select one of the programming operations shown in the Flash Programming Modes table.
4. Apply the desired byte address to pins P1.0 to P1.7 and P2.0 to P2.5.

   Apply data to pins P0.0 to P0.7 for Write Code operation.
5. Raise $\overline{EA}/V_{PP}$ to 12V to enable Flash programming, erase or verification.
6. Pulse ALE/$\overline{PROG}$ once to program a byte in the Code memory array, the Data memory array or the lock bits. The byte-write cycle is self-timed and typically takes 1.5 ms.
7. To verify the byte just programmed, bring pin P2.7 to "L" and read the programmed data at pins P0.0 to P0.7.

ıpeat steps 3 through 7 changing the address and ta for the entire 2K or 8K bytes array or until the end the object file is reached.

wer-off sequence:

t XTAL1 to "L".

t RST and $\overline{EA}$ pins to "L".

rn V_{CC} power off.

parallel programming mode, there is no auto-erase ınd to reprogram any non-blank byte, the user needs the Chip Erase operation first to erase both arrays.

Polling

T89S8252 features $\overline{DATA}$ Polling to indicate the end ite cycle. During a write cycle in the parallel or serial mming mode, an attempted read of the last byte writ- l result in the complement of the written datum on)arallel mode), and on the MSB of the serial output ı MISO (serial mode). Once the write cycle has been ıted, true data are valid on all outputs, and the next nay begin. $\overline{DATA}$ Polling may begin any time after a ycle has been initiated.

y/$\overline{Busy}$

ogress of byte programming in the parallel program- ıode can also be monitored by the RDY/$\overline{BSY}$ output Pin P3.4 is pulled Low after ALE goes High during mming to indicate $\overline{BUSY}$. P3.4 is pulled High again ırogramming is done to indicate READY.

am Verify

bits LB1 and LB2 have not been programmed, the nmed Code or Data byte can be read back via the s and data lines for verification. The state of the lock ı also be verified directly in the parallel programming In the serial programming mode, the state of the lock ı only be verified indirectly by observing that the lock ures are enabled.

Erase

ash and EEPROM arrays are erased electrically at ne time. In the parallel programming mode, chip s initiated by using the proper combination of control ; and by holding ALE/$\overline{PROG}$ low for 10 ms. The ınd Data arrays are written with all "1"s in the Chip operation.

ierial programming mode, a chip erase operation is l by issuing the Chip Erase instruction. In this mode, ase is self-timed and takes about 16 ms.

chip erase, a serial read from any address location ırn 00H at the data outputs.

Serial Programming Fuse

A programmable fuse is available to disable Serial Programming if the user needs maximum system security. The Serial Programming Fuse can only be programmed or erased in the Parallel Programming Mode.

The AT89S8252 is shipped with the Serial Programming Mode enabled.

Reading the Signature Bytes: The signature bytes are read by the same procedure as a normal verification of locations 030H and 031H, except that P3.6 and P3.7 must be pulled to a logic low. The values returned are as follows:

(030H) = 1EH indicates manufactured by Atmel
(031H) = 72H indicates 89S8252

Programming Interface

Every code byte in the Flash and EEPROM arrays can be written, and the entire array can be erased, by using the appropriate combination of control signals. The write operation cycle is self-timed and once initiated, will automatically time itself to completion.

All major programming vendors offer worldwide support for the Atmel microcontroller series. Please contact your local programming vendor for the appropriate software revision.

Serial Downloading

Both the Code and Data memory arrays can be programmed using the serial SPI bus while RST is pulled to V_{CC}. The serial interface consists of pins SCK, MOSI (input) and MISO (output). After RST is set high, the Programming Enable instruction needs to be executed first before program/erase operations can be executed.

An auto-erase cycle is built into the self-timed programming operation (in the serial mode ONLY) and there is no need to first execute the Chip Erase instruction unless any of the lock bits have been programmed. The Chip Erase operation turns the content of every memory location in both the Code and Data arrays into FFH.

The Code and Data memory arrays have separate address spaces:

0000H to 1FFFH for Code memory and 000H to 7FFH for Data memory.

Either an external system clock is supplied at pin XTAL1 or a crystal needs to be connected across pins XTAL1 and XTAL2. The maximum serial clock (SCK) frequency should be less than 1/40 of the crystal frequency. With a 24 MHz oscillator clock, the maximum SCK frequency is 600 kHz.

ıl Programming Algorithm

ɔgram and verify the AT89S8252 in the serial pro-
ning mode, the following sequence is recommended:

ɔwer-up sequence:

ɔply power between V_{CC} and GND pins.

ɜt RST pin to "H".

a crystal is not connected across pins XTAL1 and
TAL2, apply a 3 MHz to 24 MHz clock to XTAL1 pin
ıd wait for at least 10 milliseconds.

ıable serial programming by sending the Program-
ing Enable serial instruction to pin MOSI/P1.5. The
ɜquency of the shift clock supplied at pin SCK/P1.7
ɜeds to be less than the CPU clock at XTAL1 divided
ɪ 40.

ıe Code or Data array is programmed one byte at a
ne by supplying the address and data together with
e appropriate Write instruction. The selected memory
cation is first automatically erased before new data is
written. The write cycle is self-timed and typically takes less than 2.5 ms at 5V.

4. Any memory location can be verified by using the Read instruction which returns the content at the selected address at serial output MISO/P1.6.
5. At the end of a programming session, RST can be set low to commence normal operation.

Power-off sequence (if needed):

Set XTAL1 to "L" (if a crystal is not used).

Set RST to "L".

Turn V_{CC} power off.

Serial Programming Instruction

The Instruction Set for Serial Programming follows a 3-byte protocol and is shown in the following table:

ruction Set

uction	Input Format			Operation
	Byte 1	Byte 2	Byte 3	
ramming Enable	1010 1100	0101 0011	xxxx xxxx	Enable serial programming interface after RST goes high.
Erase	1010 1100	xxxx x100	xxxx xxxx	Chip erase both 8K & 2K memory arrays.
l Code Memory	aaaa a001	low addr	xxxx xxxx	Read data from Code memory array at the selected address. The 5 MSBs of the first byte are the high order address bits. The low order address bits are in the second byte. Data are available at pin MISO during the third byte.
Code Memory	aaaa a010	low addr	data in	Write data to Code memory location at selected address. The address bits are the 5 MSBs of the first byte together with the second byte.
l Data Memory	00aa a101	low addr	xxxx xxxx	Read data from Data memory array at selected address. Data are available at pin MISO during the third byte.
Data Memory	00aa a110	low addr	data in	Write data to Data memory location at selected address.
Lock Bits	1010 1100	LB1 LB2 LB3 x x111	xxxx xxxx	Write lock bits. Set LB1, LB2 or LB3 = "0" to program lock bits.

1. $\overline{\text{DATA}}$ polling is used to indicate the end of a write cycle which typically takes less than 2.5 ms at 5V.
2. "aaaaa" = high order address.
3. "x" = don't care.

sh and EEPROM Parallel Programming Modes

	RST	$\overline{PSEN}$	ALE/$\overline{PROG}$	$\overline{EA}/V_{PP}$	P2.6	P2.7	P3.6	P3.7	Data I/O P0.7:0	Address P2.5:0 P1.7:0
l Prog. Modes	H	h(1)	h(1)	x						
Erase	H	L	¯_/¯ (2)	12V	H	L	L	L	X	X
(10K bytes) Memory	H	L	¯_/¯	12V	L	H	H	H	DIN	ADDR
(10K bytes) Memory	H	L	H	12V	L	L	H	H	DOUT	ADDR
Lock Bits:	H	L	¯_/¯	12V	H	L	H	L	DIN	X
Bit - 1									P0.7 = 0	X
Bit - 2									P0.6 = 0	X
Bit - 3									P0.5 = 0	X
Lock Bits:	H	L	H	12V	H	H	L	L	DOUT	X
Bit - 1									@P0.2	X
Bit - 2									@P0.1	X
Bit - 3									@P0.0	X
Atmel Code	H	L	H	12V	L	L	L	L	DOUT	30H
Device Code	H	L	H	12V	L	L	L	L	DOUT	31H
Prog. Enable	H	L	¯_/¯ (2)	12V	L	H	L	H	P0.0 = 0	X
Prog. Disable	H	L	¯_/¯ (2)	12V	L	H	L	H	P0.0 = 1	X
Serial Prog. Fuse	H	L	H	12V	H	H	L	H	@P0.0	X

1. "h" = weakly pulled "High" internally.
2. Chip Erase and Serial Programming Fuse require a 10-ms $\overline{PROG}$ pulse. Chip Erase needs to be performed first before reprogramming any byte with a content other than FFH.
3. P3.4 is pulled Low during programming to indicate RDY/$\overline{BSY}$.
4. "X" = don't care

14. Programming the Flash/EEPROM Memory

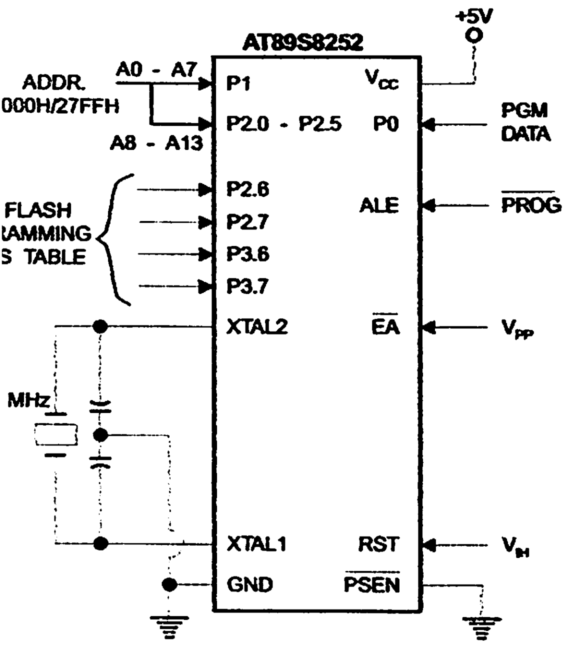
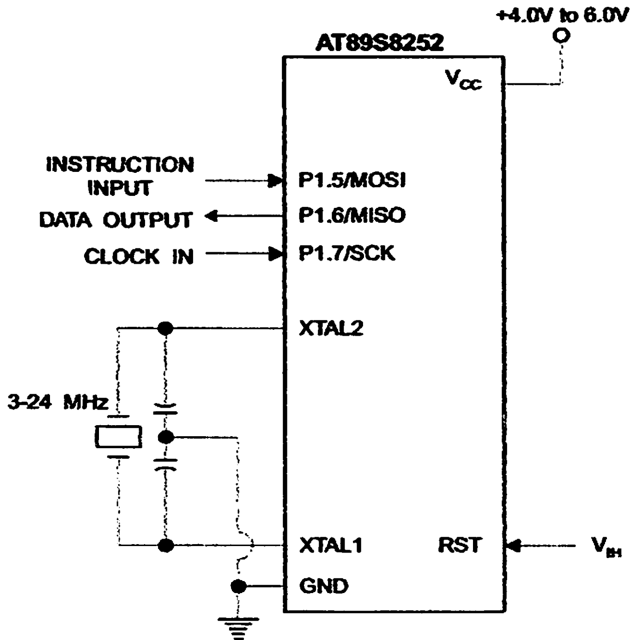
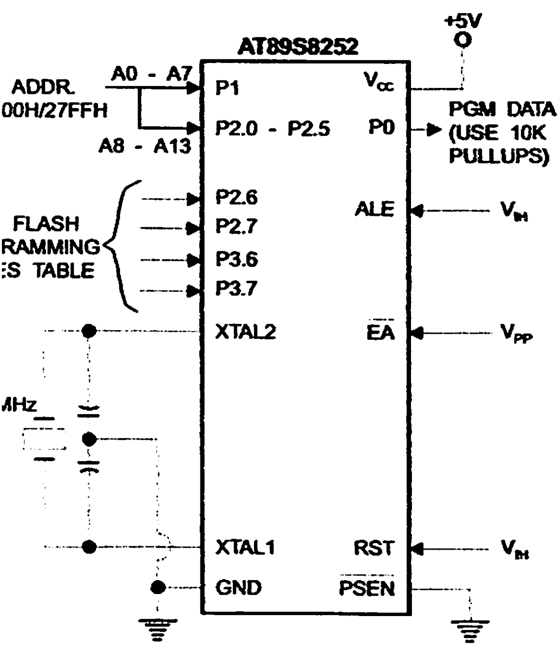


Figure 15. Flash/EEPROM Serial Downloading



16. Verifying the Flash/EEPROM Memory

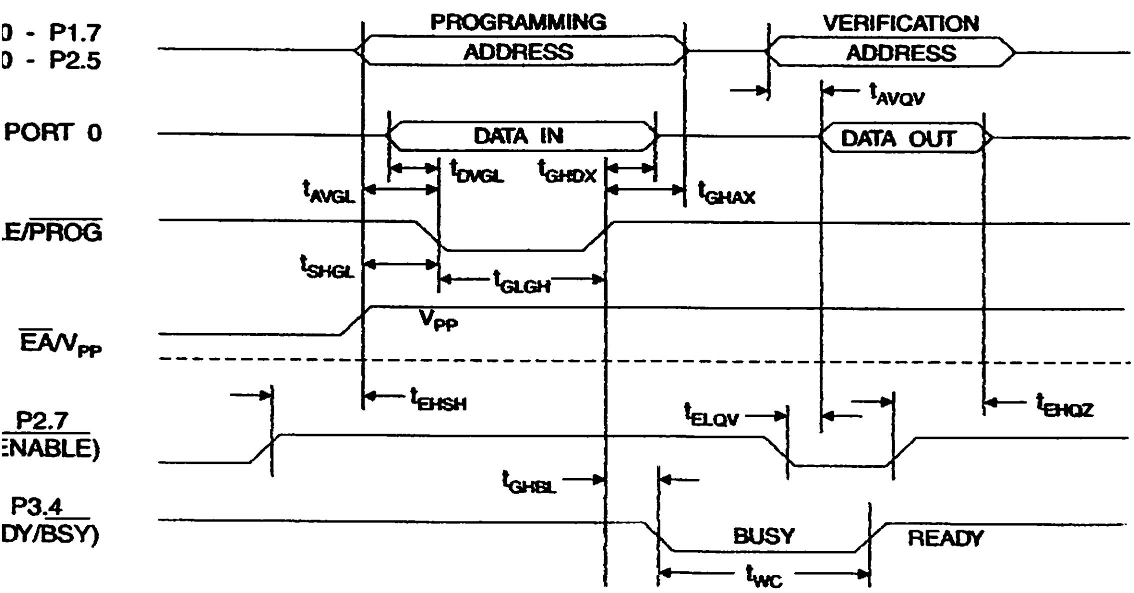


h Programming and Verification Characteristics-Parallel Mode

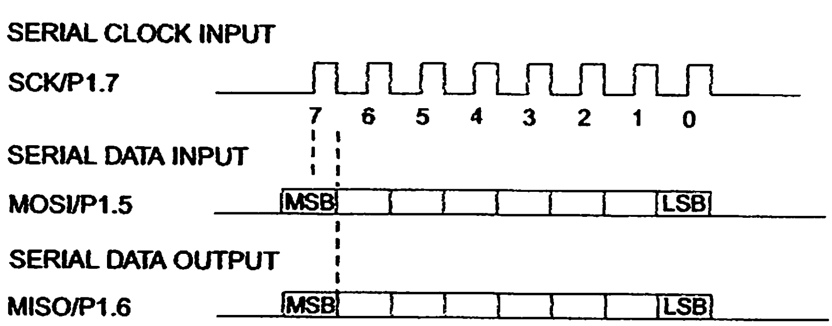
C to 70°C, V_{CC} = 5.0V ± 10%

ol	Parameter	Min	Max	Units
	Programming Enable Voltage	11.5	12.5	V
	Programming Enable Current		1.0	mA
L	Oscillator Frequency	3	24	MHz
	Address Setup to $\overline{PROG}$ Low	$48t_{CLCL}$		
	Address Hold After $\overline{PROG}$	$48t_{CLCL}$		
	Data Setup to $\overline{PROG}$ Low	$48t_{CLCL}$		
	Data Hold After $\overline{PROG}$	$48t_{CLCL}$		
	P2.7 ($\overline{ENABLE}$) High to V_{PP}	$48t_{CLCL}$		
	V_{PP} Setup to $\overline{PROG}$ Low	10		µs
	$\overline{PROG}$ Width	1	110	µs
	Address to Data Valid		$48t_{CLCL}$	
	$\overline{ENABLE}$ Low to Data Valid		$48t_{CLCL}$	
	Data Float After $\overline{ENABLE}$	0	$48t_{CLCL}$	
	$\overline{PROG}$ High to $\overline{BUSY}$ Low		1.0	µs
	Byte Write Cycle Time		2.0	ms

...h/EEPROM Programming and Verification Waveforms - Parallel Mode



al Downloading Waveforms



olute Maximum Ratings*

ting Temperature .... -55°C to +125°C

je Temperature .... -65°C to +150°C

e on Any Pin
espect to Ground ....-1.0V to +7.0V

ıum Operating Voltage... 6.6V

ıtput Current.. 15.0 mA

*NOTICE: Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

haracteristics

lues shown in this table are valid for T_A = -40°C to 85°C and V_{CC} = 5.0V ± 20%, unless otherwise noted.

ol	Parameter	Condition	Min	Max	Units
	Input Low Voltage	(Except $\overline{EA}$)	-0.5	0.2 V_{CC} - 0.1	V
	Input Low Voltage ($\overline{EA}$)		-0.5	0.2 V_{CC} - 0.3	V
	Input High Voltage	(Except XTAL1, RST)	0.2 V_{CC} + 0.9	V_{CC} + 0.5	V
	Input High Voltage	(XTAL1, RST)	0.7 V_{CC}	V_{CC} + 0.5	V
	Output Low Voltage (1) (Ports 1,2,3)	I_{OL} = 1.6 mA		0.5	V
	Output Low Voltage (1) (Port 0, ALE, $\overline{PSEN}$)	I_{OL} = 3.2 mA		0.5	V
	Output High Voltage (Ports 1,2,3, ALE, $\overline{PSEN}$)	I_{OH} = -60 µA, V_{CC} = 5V ± 10%	2.4		V
		I_{OH} = -25 µA	0.75 V_{CC}		V
		I_{OH} = -10 µA	0.9 V_{CC}		V
	Output High Voltage (Port 0 in External Bus Mode)	I_{OH} = -800 µA, V_{CC} = 5V ± 10%	2.4		V
		I_{OH} = -300 µA	0.75 V_{CC}		V
		I_{OH} = -80 µA	0.9 V_{CC}		V
	Logical 0 Input Current (Ports 1,2,3)	V_{IN} = 0.45V		-50	µA
	Logical 1 to 0 Transition Current (Ports 1,2,3)	V_{IN} = 2V, V_{CC} = 5V ± 10%		-650	µA
	Input Leakage Current (Port 0, $\overline{EA}$)	0.45 < V_{IN} < V_{CC}		±10	µA
	Reset Pulldown Resistor		50	300	KΩ
	Pin Capacitance	Test Freq. = 1 MHz, T_A = 25°C		10	pF
	Power Supply Current	Active Mode, 12 MHz		25	mA
		Idle Mode, 12 MHz		6.5	mA
	Power Down Mode (2)	V_{CC} = 6V		100	µA
		V_{CC} = 3V		40	µA

1. Under steady state (non-transient) conditions, I_{OL} must be externally limited as follows:
   Maximum I_{OL} per port pin: 10 mA
   Maximum I_{OL} per 8-bit port:
   Port 0: 26 mA
   Ports 1, 2, 3: 15 mA
   Maximum total I_{OL} for all output pins: 71 mA
   If I_{OL} exceeds the test condition, V_{OL} may exceed the related specification. Pins are not guaranteed to sink current greater than the listed test conditions.
2. Minimum V_{CC} for Power Down is 2V

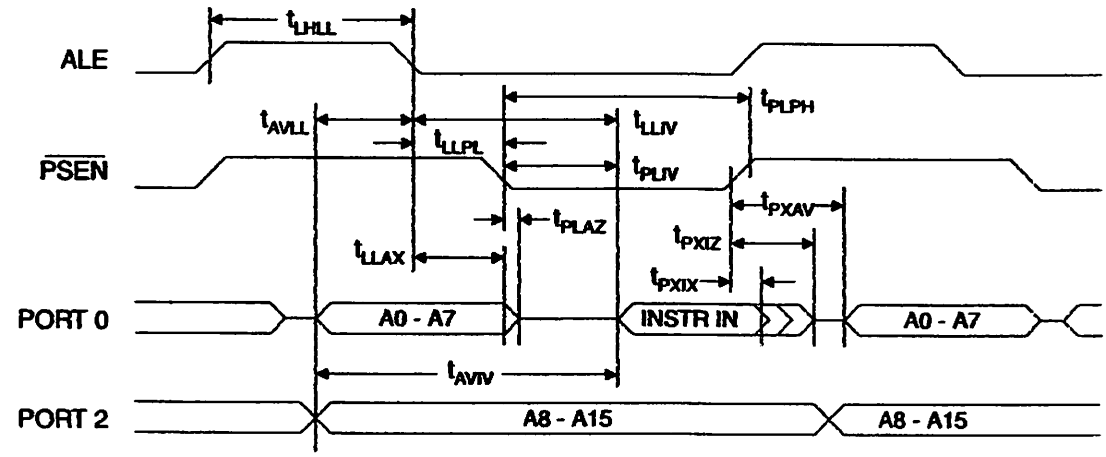
Characteristics

operating conditions, load capacitance for Port 0, ALE/$\overline{PROG}$, and $\overline{PSEN}$ = 100 pF; load capacitance for all other
s = 80 pF.

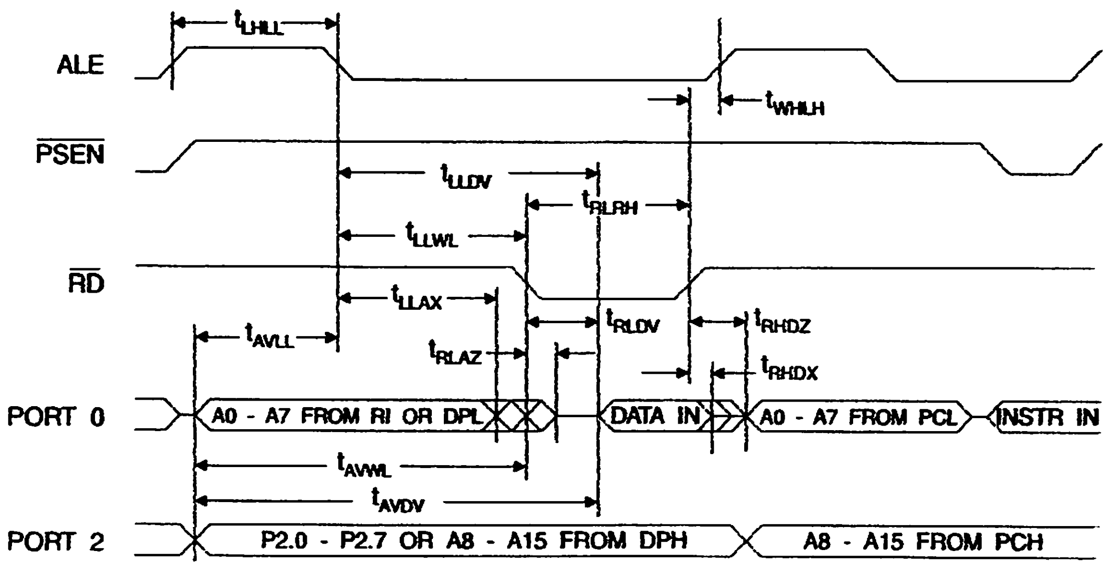
rnal Program and Data Memory Characteristics

ol	Parameter	Variable Oscillator		Units
		Min	Max	
L	Oscillator Frequency	0	24	MHz
	ALE Pulse Width	$2t_{CLCL}$ - 40		ns
	Address Valid to ALE Low	t_{CLCL} - 13		ns
	Address Hold After ALE Low	t_{CLCL} - 20		ns
	ALE Low to Valid Instruction In		$4t_{CLCL}$ - 65	ns
	ALE Low to $\overline{PSEN}$ Low	t_{CLCL} - 13		ns
	$\overline{PSEN}$ Pulse Width	$3t_{CLCL}$ - 20		ns
	$\overline{PSEN}$ Low to Valid Instruction In		$3t_{CLCL}$ - 45	ns
	Input Instruction Hold After $\overline{PSEN}$	0		ns
	Input Instruction Float After $\overline{PSEN}$		t_{CLCL} - 10	ns
	$\overline{PSEN}$ to Address Valid	t_{CLCL} - 8		ns
	Address to Valid Instruction In		$5t_{CLCL}$ - 55	ns
	$\overline{PSEN}$ Low to Address Float		10	ns
	$\overline{RD}$ Pulse Width	$6t_{CLCL}$ - 100		ns
	$\overline{WR}$ Pulse Width	$6t_{CLCL}$ - 100		ns
	$\overline{RD}$ Low to Valid Data In		$5t_{CLCL}$ - 90	ns
	Data Hold After $\overline{RD}$	0		ns
	Data Float After $\overline{RD}$		$2t_{CLCL}$ - 28	ns
	ALE Low to Valid Data In		$8t_{CLCL}$ - 150	ns
	Address to Valid Data In		$9t_{CLCL}$ - 165	ns
	ALE Low to $\overline{RD}$ or $\overline{WR}$ Low	$3t_{CLCL}$ - 50	$3t_{CLCL}$ + 50	ns
	Address to $\overline{RD}$ or $\overline{WR}$ Low	$4t_{CLCL}$ - 75		ns
	Data Valid to $\overline{WR}$ Transition	t_{CLCL} - 20		ns
	Data Valid to $\overline{WR}$ High	$7t_{CLCL}$ - 120		ns
	Data Hold After $\overline{WR}$	t_{CLCL} - 20		ns
	$\overline{RD}$ Low to Address Float		0	ns
	$\overline{RD}$ or $\overline{WR}$ High to ALE High	t_{CLCL} - 20	t_{CLCL} + 25	ns

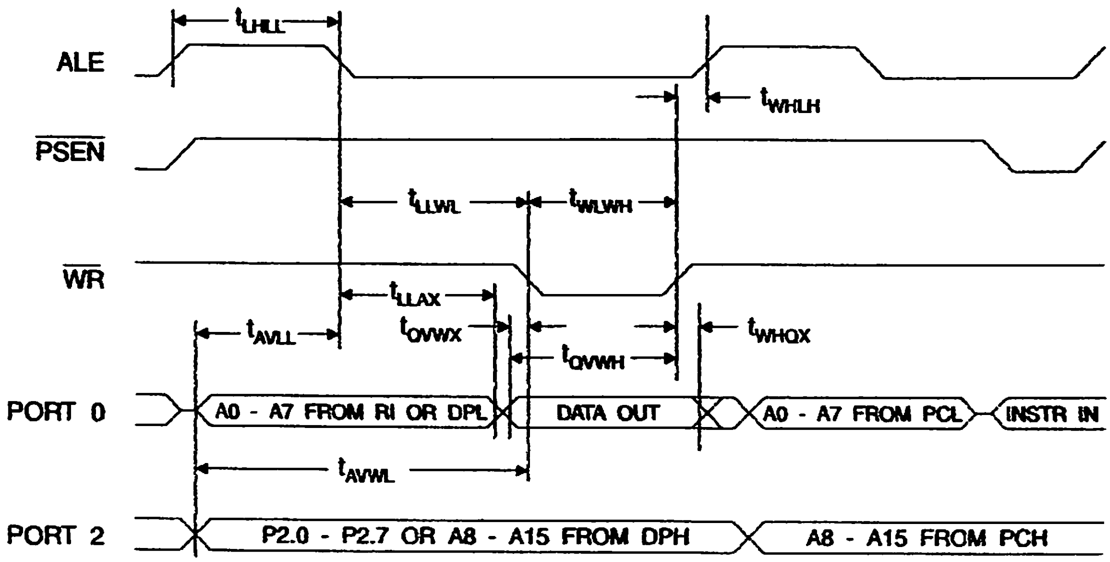
rnal Program Memory Read Cycle



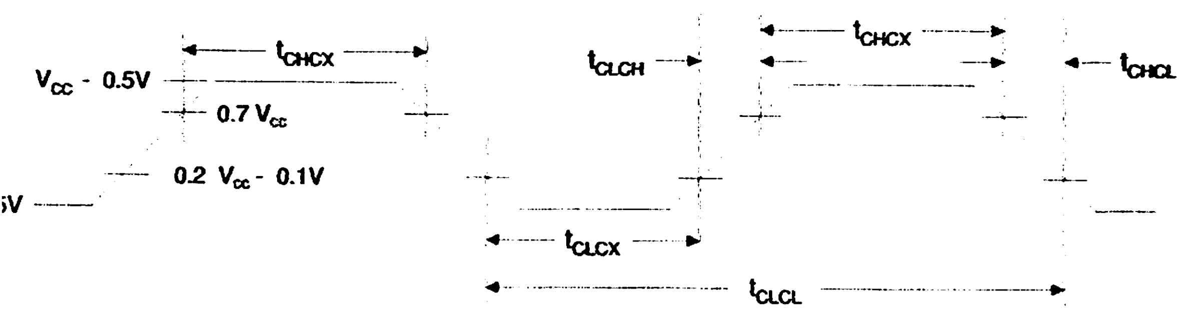
rnal Data Memory Read Cycle



rnal Data Memory Write Cycle



rnal Clock Drive Waveforms



rnal Clock Drive

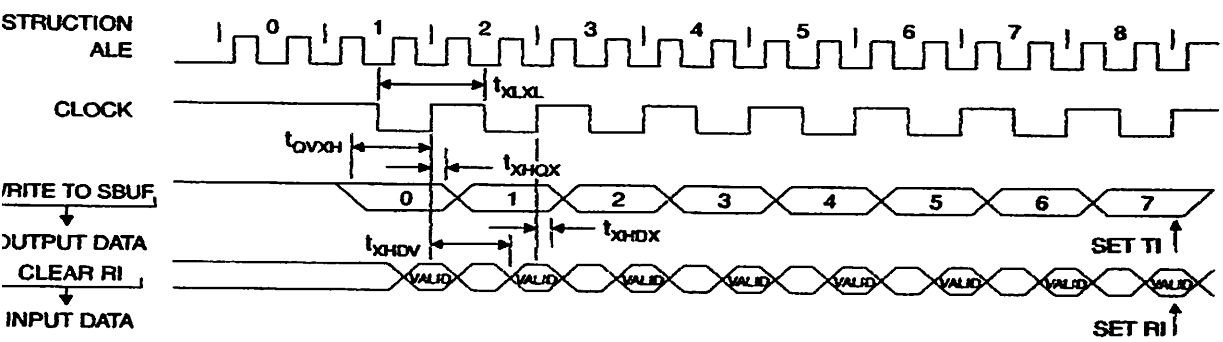
ol	Parameter	VCC = 4.0V to 6.0V		Units
		Min	Max	
.	Oscillator Frequency	0	24	MHz
	Clock Period	41.6		ns
	High Time	15		ns
	Low Time	15		ns
	Rise Time		20	ns
	Fall Time		20	ns

al Port Timing: Shift Register Mode Test Conditions

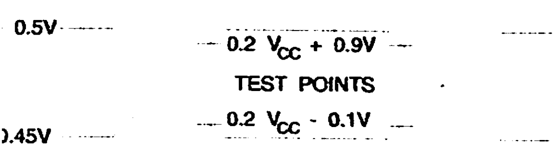
alues in this table are valid for V_{CC} = 4.0V to 6V and Load Capacitance = 80 pF.

ɔol	Parameter	Variable Oscillator		Units
		Min	Max	
	Serial Port Clock Cycle Time	$12t_{CLCL}$		µs
ı	Output Data Setup to Clock Rising Edge	$10t_{CLCL}$ - 133		ns
;	Output Data Hold After Clock Rising Edge	$2t_{CLCL}$ - 117		ns
:	Input Data Hold After Clock Rising Edge	0		ns
	Clock Rising Edge to Input Data Valid		$10t_{CLCL}$ - 133	ns

t Register Mode Timing Waveforms

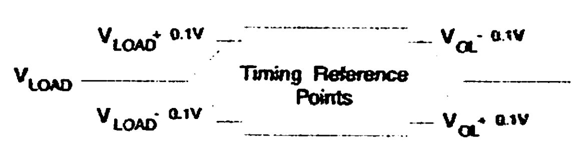


'esting Input/Output Waveforms(1)

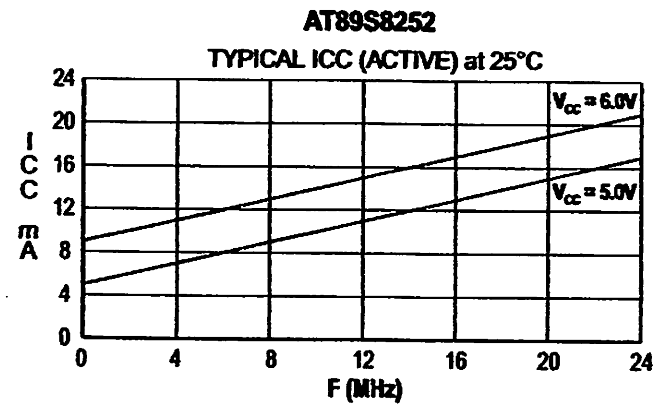


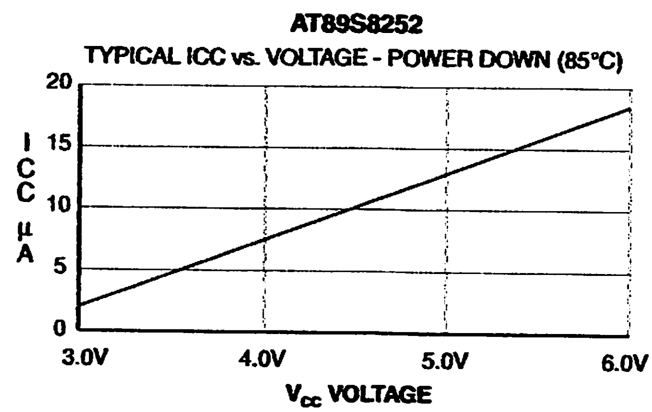
1. AC Inputs during testing are driven at V_{CC} - 0.5V for a logic 1 and 0.45V for a logic 0. Timing measurements are made at V_{IH} min. for a logic 1 and V_{IL} max. for a logic 0.

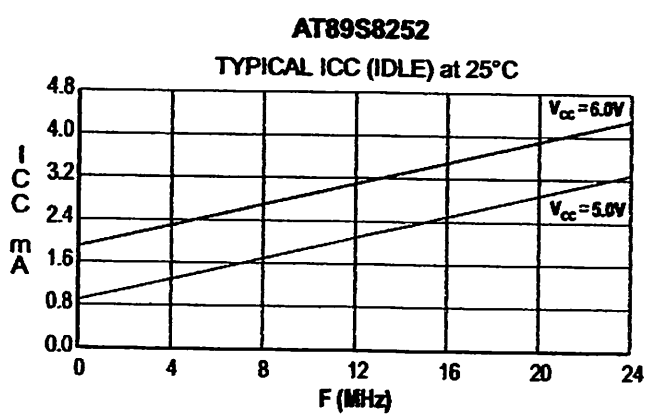
Float Waveforms(1)



Notes: 1. For timing purposes, a port pin is no longer floating when a 100 mV change from load voltage occurs. A port pin begins to float when a 100 mV change from the loaded V_{OH}/V_{OL} level occurs.







1. XTAL1 tied to GND for Icc (power down)
2. Lock bits programmed

NO. SB-6002

EPSON DOT MATRIX LCD MODULE

EA-C20017AR

TENTATIVE SPECIFICATIONS

REVISION VOL. 1

FEBRUALY / 28 / 1985

EPSON CORPORATION

EA-C20017AR TENTATIVE SPECIFICATION

TABLE OF REVISION

Rev. No.	Page	Revision contents: Before Revision	Revision contents: After Revision	Date
1	8	(1) 6.1 No.1/D2 bit is "0" (2) 6.1 [NOTE]	6.1 No. 1/D2 bit is "1" 6.1 "DISP ON/OFF" command is added	Feb/28/85
	18	t comd 16/φ (MHZ)	t comd 16/CLOCK (HZ)	
	20	T WCYC 16/φ (MHZ)	T WCYC 16/CLOCK (HZ)	

CONTENTS

INTRODUCTION

The EA-C20017AR is a dot matrix liquid crystal display (LCD) module capable of generating 20 characters per line. The on-chip driver configuration provides the TCM-A0077-3 with two attractive features -- very compact design and very low cost.

The built-in memories include a 20-word data RAM, a 160-character CG ROM and a 4-character CG RAM. Data from the MPU or others can be programmed in the data RAM for convenient display.

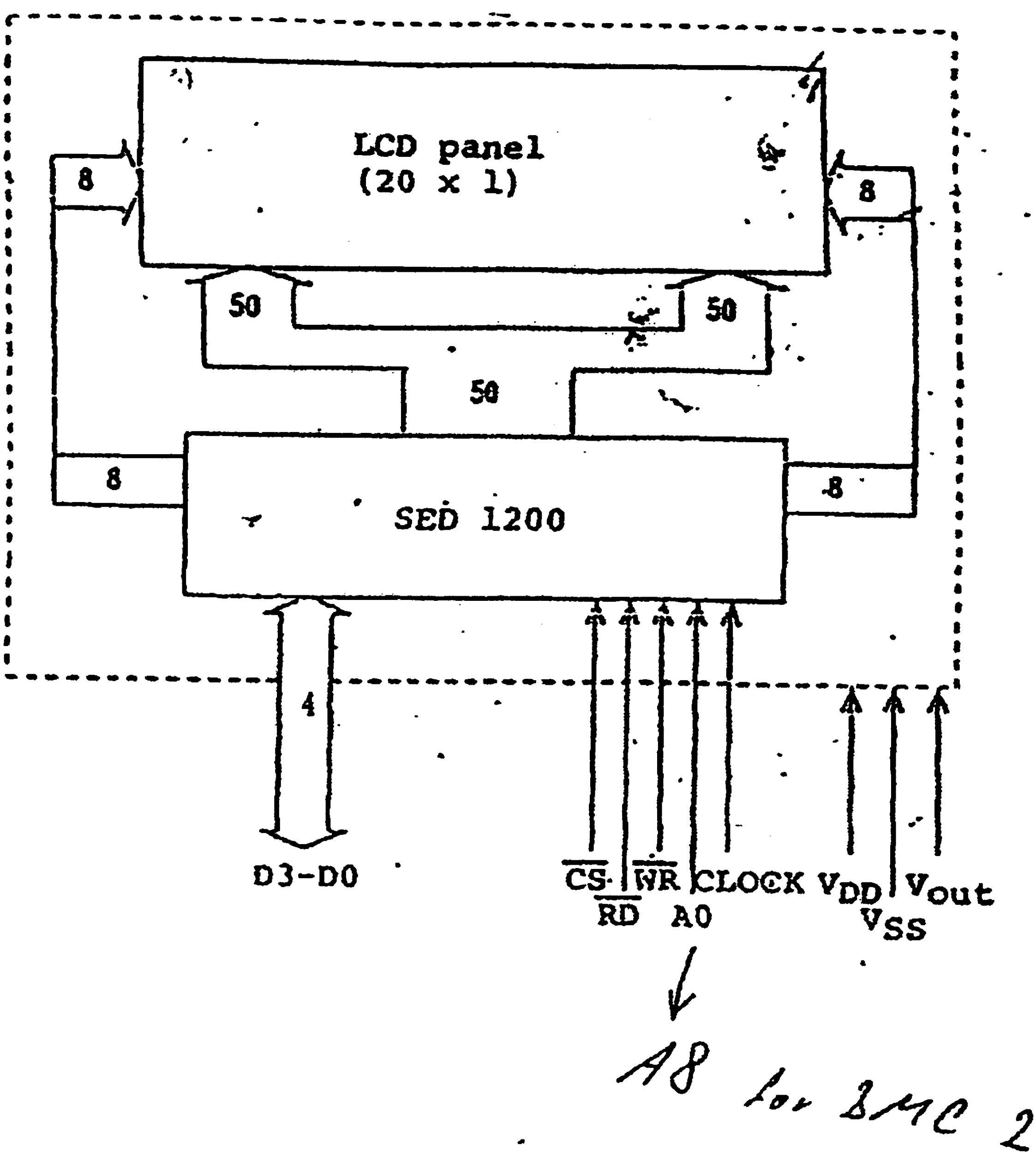
The MPU is responsible for only display data and commands and is not required to control any other display functions This means that, with the EA-C20017AR , the MPU workload is reduced.

Features

1)	On-chip display data RAM	: 20 words (8 bits/word)
2)	On-chip CG ROM	: 96 ASCII character codes + 64 special letters
3)	On-chip CG RAM	: 4 characters (5 x 8 dots, allowing pseudo-graphics display)
4)	Character font	: 5 x 7 dots + cursor line
5)	Cursor font	: Underline or all dot blinking (selectable)
6)	Commands	: 13 different commands (including System Set and Cursor Control)

Interface	:	Possible with 4-bit or 8-bit MPU
Power supply	:	5V DC single power
Display	:	TN-FEM positive display, reflection type, 1/16 duty

BLOCK DIAGRAM



FUNDAMENTAL OPERATIONS

(1) The module consists of an on-chip character displa control driver, a CR oscillator and an LCD panel. The LCD supply voltage dividing resistors are buil into the chip.

(2) The contrast of the LCD panel has temperature and visual angle characteristics. The contrast and visual angle can be adjusted by a variable resisto of specific value connected between VSS and Vout o the I/O connector, so that the module may be used under an optimum condition in the operating enviror ment.

(3) The module operates from a +5V single power supply.

(4) The controller contains a display data RAM and a character generator (CG) which produces 96 ASCII character codes and 64 special letters.. The MPU controls only display data and commands and nothing more. This leads to a reduction in MPU workload.

5) All display functions for display data, address dat and the cursor are controlled by 13 different commands entered via the data bus.

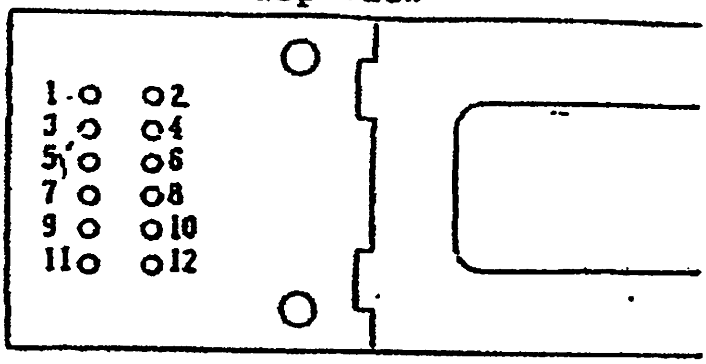
6) Two cursor display formats are available: underlinir and all-dot blinking.

7) Other functions include system reset and display on-off.

5. INPUT/OUTPUT PINS

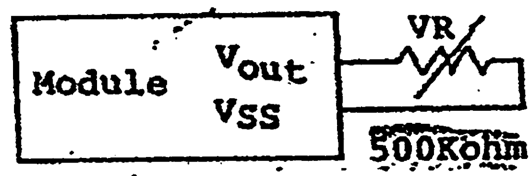
5.1 Pin Configuration

Top View



No.	Symbol name
1	V_{DD}
2	V_{SS}
3	V_{out}
4	CLOCK
5	$\overline{CS}$
6	A0
7	$\overline{WR}$
8	$\overline{RD}$
9	D3
10	D2
11	D1
12	D0

.2 Pin Description

Symbol	I/O	Name	Fucntion
V_{DD}	I	Power input	+5V ±5%
V_{SS}	I	Power input	0V (GND)
V_{out}	I	LCD contrast adjustment	Contrast adjustment 
CLOCK	I	Command clock input	System clock input pin (1 to 3.2 MHz)
$\overline{CS}$	I	Chip select	Active "L"
A0	I	Display data/ command input selection	[redacted]
$\overline{WR}$	I	Write enable input	Active "L"
$\overline{RD}$	I	Read enable input	Active "L"
D3-D0	I/O	Data input (D3 only: input/ output)	8 bits, consisting of upper 4 bits and lower 4 bits

COMMANDS

.1 Command List

Command name	$\overline{CS}$	$\overline{WR}$	$\overline{RD}$	A0	D7	D6	D5	D4	D3	D2	D1	D0	Remarks
SET CURSOR DIRECTION	0	0	1	0	0	0	0	0	0	1	0	D/I	D/I=1 decrement D/I=0 increment
CURSOR ADDRESS -1/+1	0	0	1	0	0	0	0	0	0	1	1	-1/+1	-1/+1=1 cursor address -1 -1/+1=0 cursor address +1
CURSOR FONT SELECT	0	0	1	0	0	0	0	0	1	0	0	A/U	A/U=1 all dots blinking A/U=0 underlining
CURSOR BLINK ON/OFF	0	0	1	0	0	0	0	0	1	0	1	ON/OFF	ON/OFF=1 ON ON/OFF=0 OFF
DISPLAY ON/OFF	0	0	1	0	0	0	0	0	1	1	0	ON/OFF	ON/OFF=1 ON ON/OFF=0 OFF
CURSOR ON/OFF	0	0	1	0	0	0	0	0	1	1	1	ON/OFF	ON/OFF=1 ON ON/OFF=0 OFF
SYSTEM RESET	0	0	1	0	0	0	0	1	0	0	0	0	Data RAM and CG RAM are not affected.
LINE SELECT	0	0	1	0	0	0	0	1	0	0	1	1	Set for 1/16 duty & 20 x 1.line
SET CGRAM ADDRESS	0	0	1	0	0	0	1	0	(lower address)				Upper address fixed to 0H
SET CGRAM DATA	0	0	1	0	0	1	0		(CG RAM data)				
SET CURSOR ADDRESS	0	0	1	0	(character address code)								See character address code, section 7.
SET CHARACTER CODE	0	0	1	1	(character code)								See character code map, section 7.
BUSY FLAG CHECK	0	1	0	0	BF	*	*	*	BF	*	*	*	BF=1 busy BF=0 not busy
					(*:high impedance)								

[NOTE] Entry of any command other than those listed above may cause an instruction or internal flag status to change. [redacted].

[redacted]

Command Description

1) SET CURSOR DIRECTION

A0	$\overline{WR}$	MSB (D7)		LSB (D0)	
0	0	0 0 0 0	0 1 0 0		Increment
		0 0 0 0	0 1 0 1		Decrement

This command specifies the direction in which the cursor moves. Writing 04H brings cursor increment mode. Writing 05H brings cursor decrement mode.
With a cursor direction set, the cursor address register (data RAM address) is set for increment or decrement direction. Each time a SET CHARACTER CODE command is executed, the address changes automatically in the set direction.

2) CURSOR ADDRESS -1/+1

A0	$\overline{WR}$	MSB (D7)		LSB (D0)	
0	0	0 0 0 0	0 1 1 0		+1
		0 0 0 0	0 1 1 1		-1

This command adds 1 to, or subtracts 1 from, the cursor address. Writing 06H causes the cursor address to be incremented by 1. Writing 07H causes the address to be decremented by 1. The command enables only cursor movement, and is useful for editing.

CURSOR FONT SELECT

A0 : 0 $\overline{WR}$: 0

	MSB(D7)	LSB(D0)	
	0 0 0 0	0 1 1 0	Underlining
		1 0 0 0	
	0 0 0 0	0 1 1 1	All dot blinking
		1 0 0 1	

This command selects a cursor format. Writing 08H brings underlining mode. Writing 09H brings all dot blinking mode. (in which case blinking cannot be turned off)

CURSOR BLINK ON/OFF

A0 : 0 $\overline{WR}$: 0

	MSB(D7)	LSB(D0)	
	0 0 0 0	1 0 1 0	Off
	0 0 0 0	1 0 1 1	On

This command turns on or off underline blinking when the cursor is used in underline format. Writing 0AH turns off the blinking of the cursor. Writing 0BH turns on the blinking of the cursor.

DISPLAY ON/OFF

A0 : 0 $\overline{WR}$: 0

	MSB(D7)	LSB(D0)	
	0 0 0 0	1 1 0 0	Off
	0 0 0 0	1 1 0 1	On

This command turns on or off the display. Writing 0CH turns off the display. Writing 0DH turns on the display. With the display off, the contents of the data RAM are not cleared.

URSOR ON/OFF

			MSB(D7)	LSB(D0)	
0 :	0	$\overline{WR}$: 0	0 0 0 0	1 1 1 0	Off
			0 0 0 0	1 1 1 1	On

his command turns on or off the cursor. Writing 0EH urns off the cursor. Writing 0FH turns on the cursor.

YSTEM RESET

			MSB(D7)	LSB(D0)
0 :	0	$\overline{WR}$: 0	0 0 0 1	0 0 0 0

his command initializes the system. (However, it does ot affect the data RAM and CG RAM.) Writing 10H auses the instruction commands to be set as follows:

ET CURSOR DIRECTION ---------------------- Increment
URSOR FONT SELECT ------------------------ Underlining
URSOR BLINK ON/OFF ---------------------- Off
ISPLAY ON/OFF --------------------------- Off
URSOR ON/OFF ---------------------------- Off
INE SELECT ------------------------------ One line display
ET CURSOR ADDRESS ---------------------- Line 1, address (

INE SELECT

			MSB(D7)	LSB(D0)
0 :	0	$\overline{WR}$: 0	0 0 0 1	0 0 1 1

his command specifies the number of lines to be dis- layed (LCD drive duty). 13H is set as this module s of 1/16 duty driving.

SET CURSOR ADDRESS

A0 : 0 WR : 0 MSB(D7) | character address code | LSB(D0)

This command presets the address of the cursor. Use the character address code to preset the cursor address. (See Character Address Code, section 7.)

SET CHARACTER CODE

A0 : 1 WR : 0 MSB(D7) | character code | LSB(D0)

This command writes a character code into the data
(See Character Code Map, section 7.)

BUSY FLAG CHECK

A0 : 0 RD : 0 WR : 1 MSB(D7) | BF * * * | BF * * | LSB

*:high impedance

This command checks the status of the module.
The flag showing whether the internal conditio
busy or not busy appears at pin D3. (In this c
D2, D1 and D0 are at high impedance.)

To check the internal condition of the module
external unit, read the value appearing at pi
If pin [redacted] the [redacted] Then
the BUSY FLAG CHECK command.
If pin D3 is [redacted] the system is [redacted]. I
another command can be written.
Unlike the others, the BUSY FLAG CHECK comm
terminate when read once.

A0 : 0 $\overline{WR}$: 0   0 0 1 0 ...

This command specifies a CG RAM address (character code). Four CG RAM addresses are available: 00H, 01H, 02H and 03H. Only the lower addresses must be used for setting: 0H, 1H, 2H and 3H.

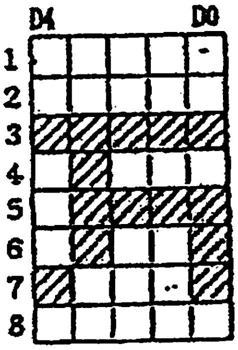
(13) SET CGRAM DATA

A0 : 0 $\overline{WR}$: 0   MSB(D7) [0 1 0 (CGRAM data)] LSB(D0)

This command registers a pattern (5 x 8 dots) at a preset address (set by the SET CGRAM ADDRESS command). Data, in bit image, is to be set at D4 through D0. ('1' -- on, '0' -- off)

[Example]

Register pattern "万" at CG RAM address 01H.

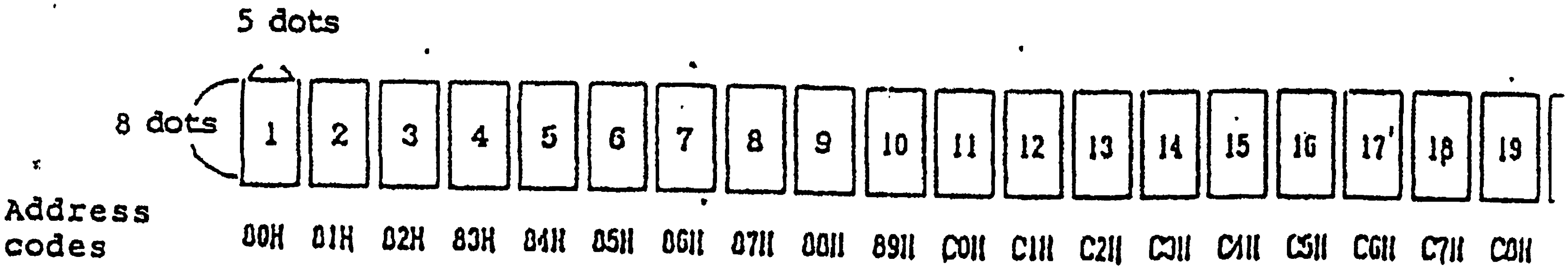


Step	A0	$\overline{WR}$	Data	Contents
1.	0	0	21H	Set CG RAM address.
2.	0	0	40H	Set ROW1 data.
3.	0	0	40H	" 2 "
4.	0	0	5FH	" 3 "
5.	0	0	48H	" 4 "
6.	0	0	4FH	" 5 "
7.	0	0	49H	" 6 "
8.	0	0	51H	" 7 "
9.	0	0	40H	" 8 "

[NOTE] The BUSY FLAG CHECK command is omitted from the step.

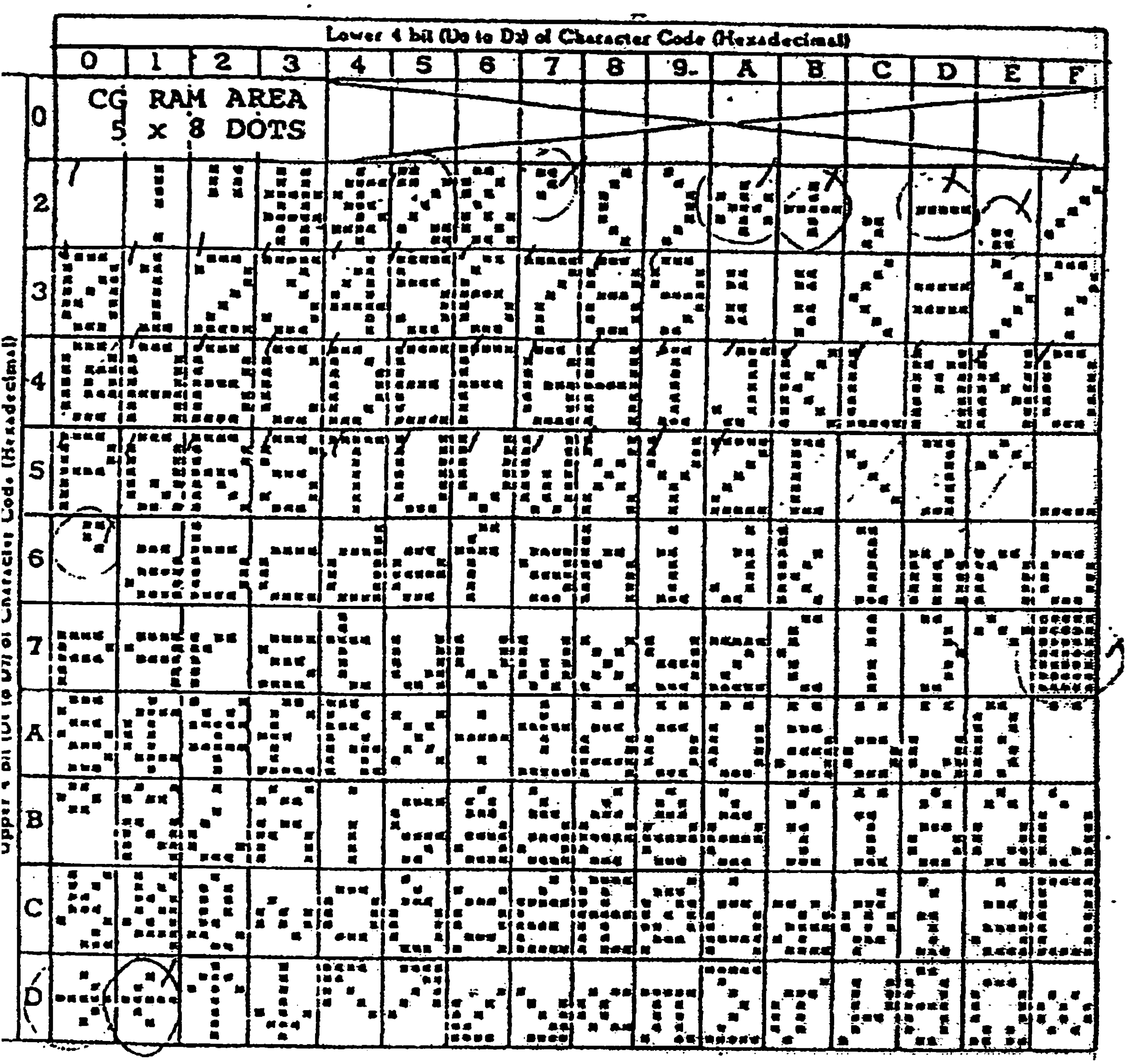
Assignment of the address codes to the characters on the display is shown.

Character positions

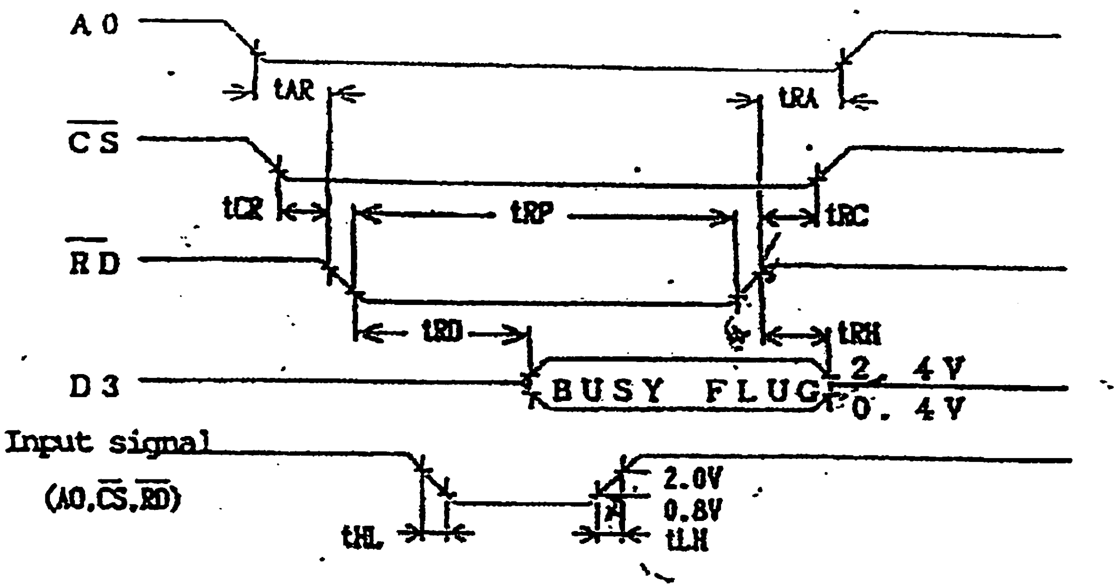


7.2 Character Code and Display Patterns

* Character Code Map



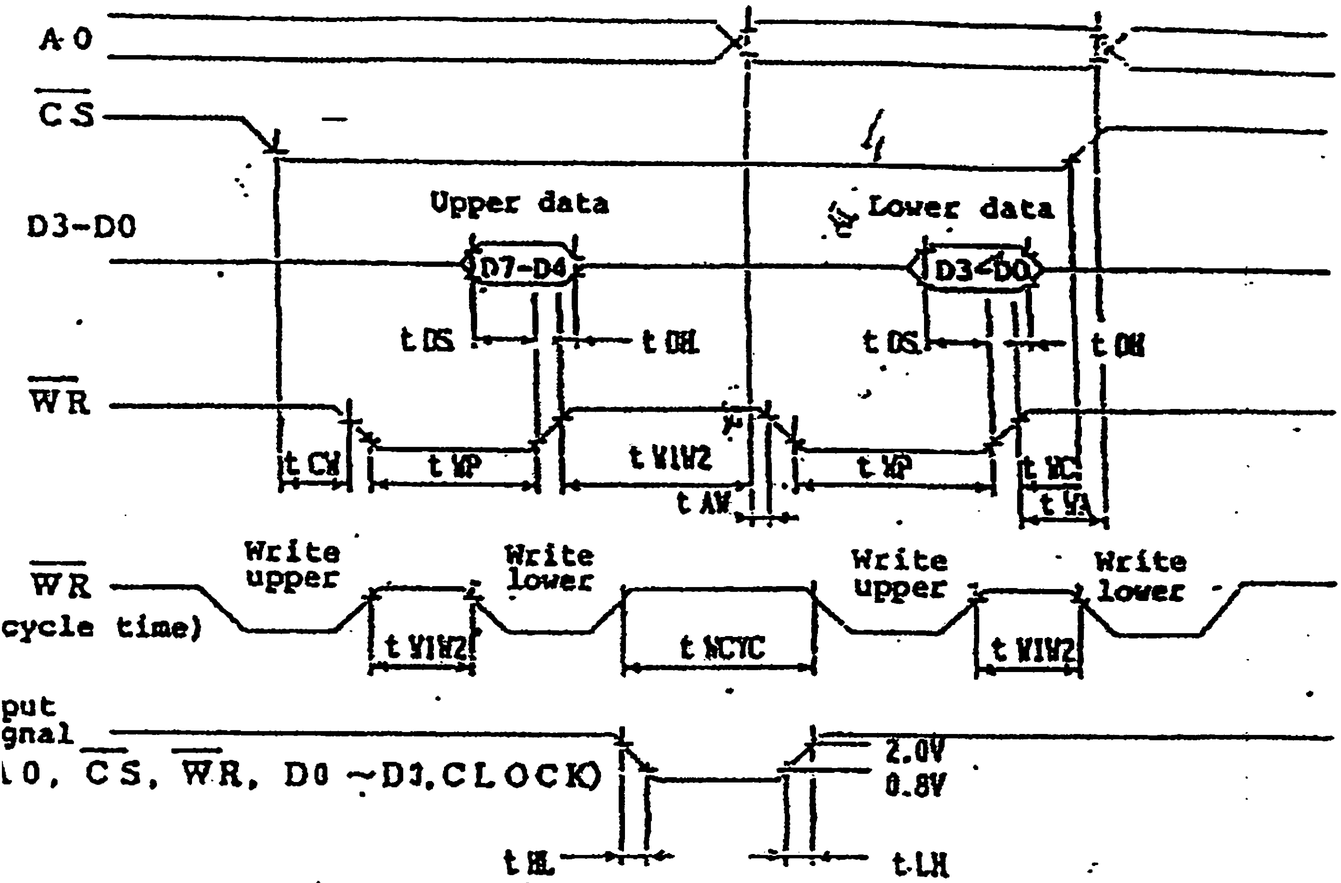
2.1 Read Timing (BUSY Flag)



(Ta = 0 ∿ 50°C V_{DD}=5V±5%)

Parameter	Symbol	Standard			Unit	Remarks
		Min.	Typ.	Max.		
→ RD set time	t_{AR}	0	—	—	nsec	
→ RD set time	t_{CR}	0	—	—	nsec	
put delay time from	t_{RD}	—	—	250	nsec	D3 load CL=100pF
→ A0 hold time	t_{RA}	20	—	—	nsec	
→ CS hold time	t_{RC}	20	—	—	nsec	
a hold time	t_{RH}	10	—	—	nsec	
d pulse width	t_{RP}	350	—	—	nsec	
ut fall time	t_{HL}	—	—	50	nsec	
ut rise time	t_{LH}	—	—	50	nsec	

2.2 Write Timing



Ta = 0 ~ 50°C VDD=5V±5%

Parameter	Symbol	Standard			Unit
		Min.	Typ.	Max.	
→ WR set time	t_{AW}	0	--	--	nsec
→ WR set time	t_{CW}	0	--	--	nsec
ta set-up time	t_{DS}	120	--	--	nsec
→ A0 hold time	t_{WA}	20	--	--	nsec
→ CS hold time	t_{WC}	20	--	--	nsec
ta hold time	t_{DH}	20	--	--	nsec
ite pulse width	t_{WP}	200	--	--	nsec
per write → lower write time	t_{W1W2}	200	--	--	nsec
wer write → upper write time	t_{WCYC}	16/CLOCK (Hz)	--	--	µsec
put fall time	t_{HL}	--	--	50	nsec
	t_{LH}	--	--	50	nsec

Fig. 1 Definition of V_{th}

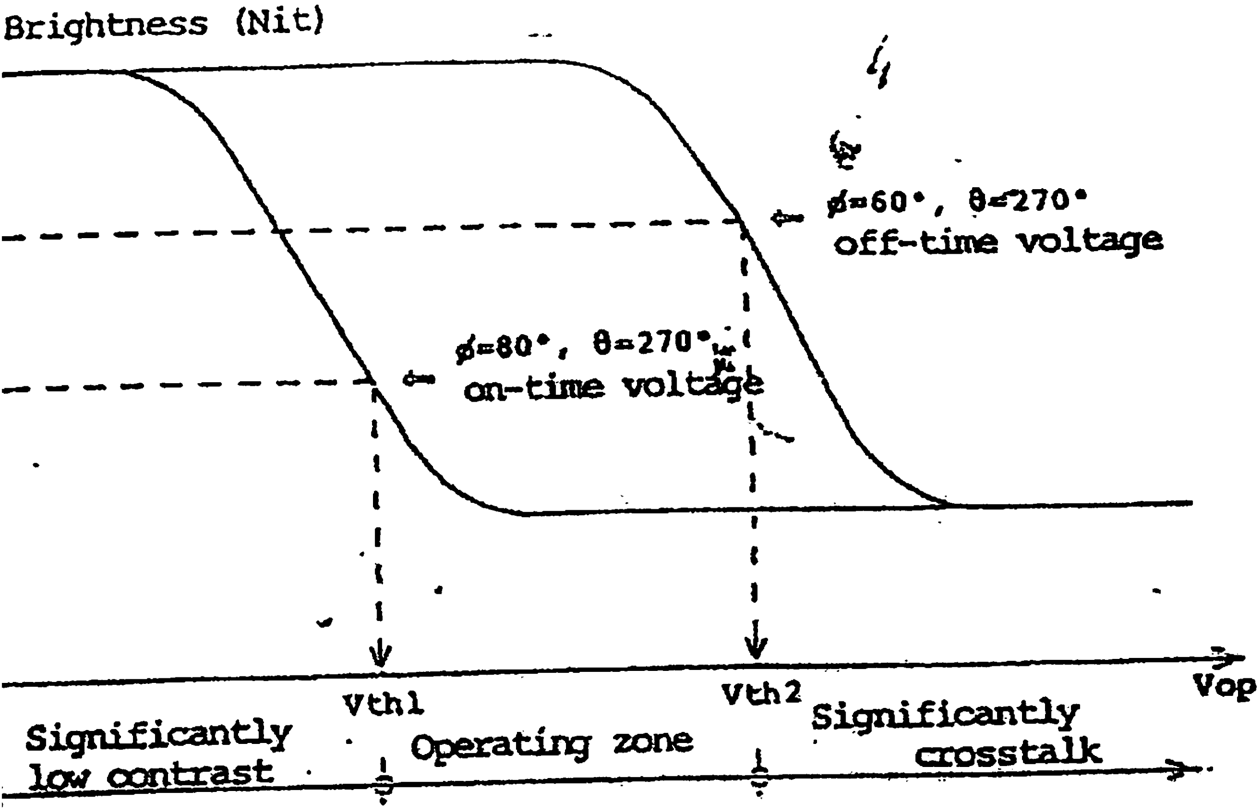
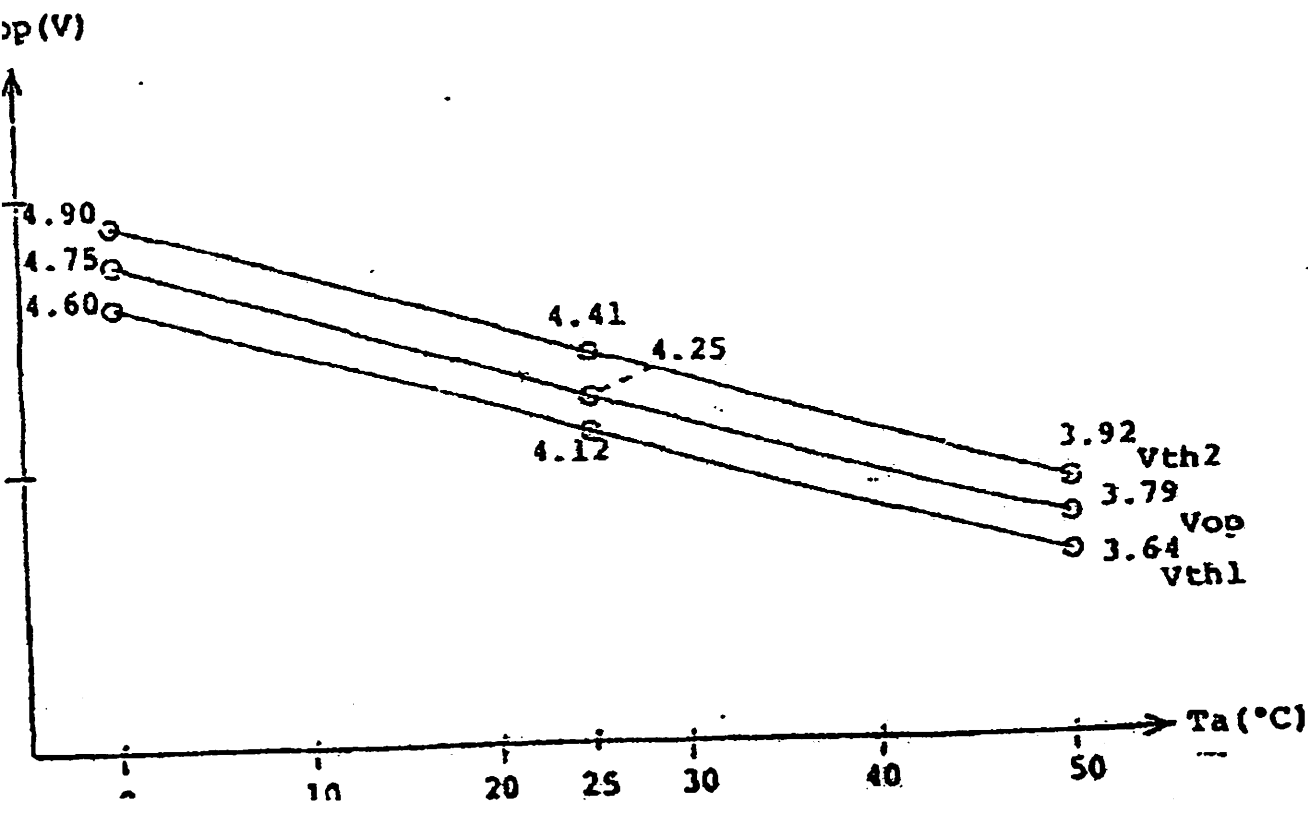


Fig. 2 V_{op}- Temperature Curves



OPTICAL CHARACTERISTICS

1 Drive Conditions

(Ta=25°C)

Parameter	Voltage	Duty	Bias
Specification	4.25V	1/16	1/5

2 Electro-Optical Characteristics

Parameter	Symbol	Temperature °C		Standard Min.	Standard Typ.	Standard Max.	Unit	Remarks
Drive voltage ($V_{DD}-V_{LCD}$)	V_{OP}	0	Vth 2	4.65	4.90	--	V	Fig. 1
			Vth 1	--	4.60	4.83		Fig. 2
		25	Vth 2	4.19	4.41	--		
			Vop	--	4.25	--		
			Vth 1	--	4.12	4.33		
		50	Vth 2	3.60	3.92	--		
			Vth 1	--	3.64	3.80		
Response time	tr	Low temp. (0)		--	500	700	ms	Note 2
				--	--	--		
		25		--	170	250		
	tf	Low temp. (0)		--	350	550		
				--	--	--		
		25		--	150	250		
Range of Viewing angles: Longi-tudinal	ø1			60	--	80	DEG	Note 3
Range of Viewing angles: Lateral	ø2			60	--	120	DEG	
Contrast ratio	K	25		--	3	--		Note 4

NOTE 1] Definition of frame frequency:

1 period = common side supply waveform

Optical Measuring Apparatus

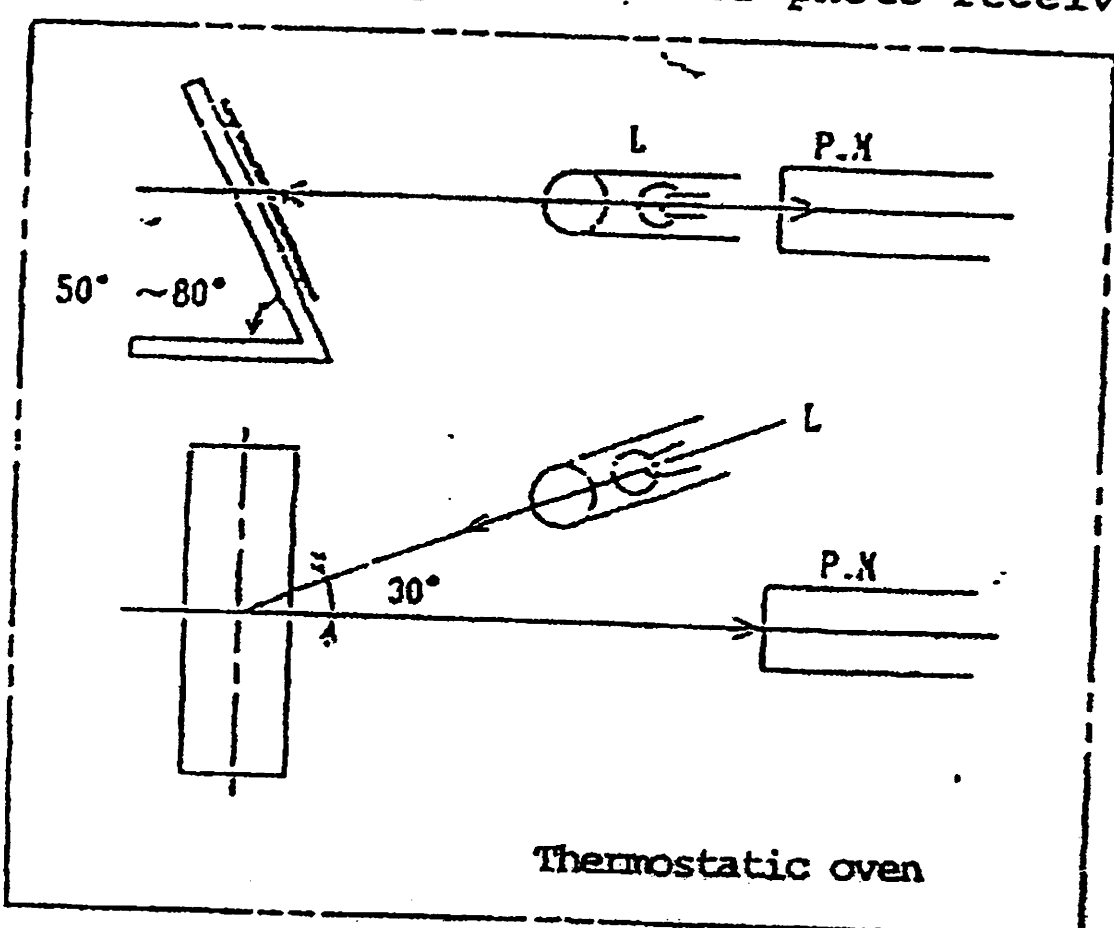
Specifications: Brightness meter   Canon LC-2S
Light source   Halogen lamp

Measuring conditions:

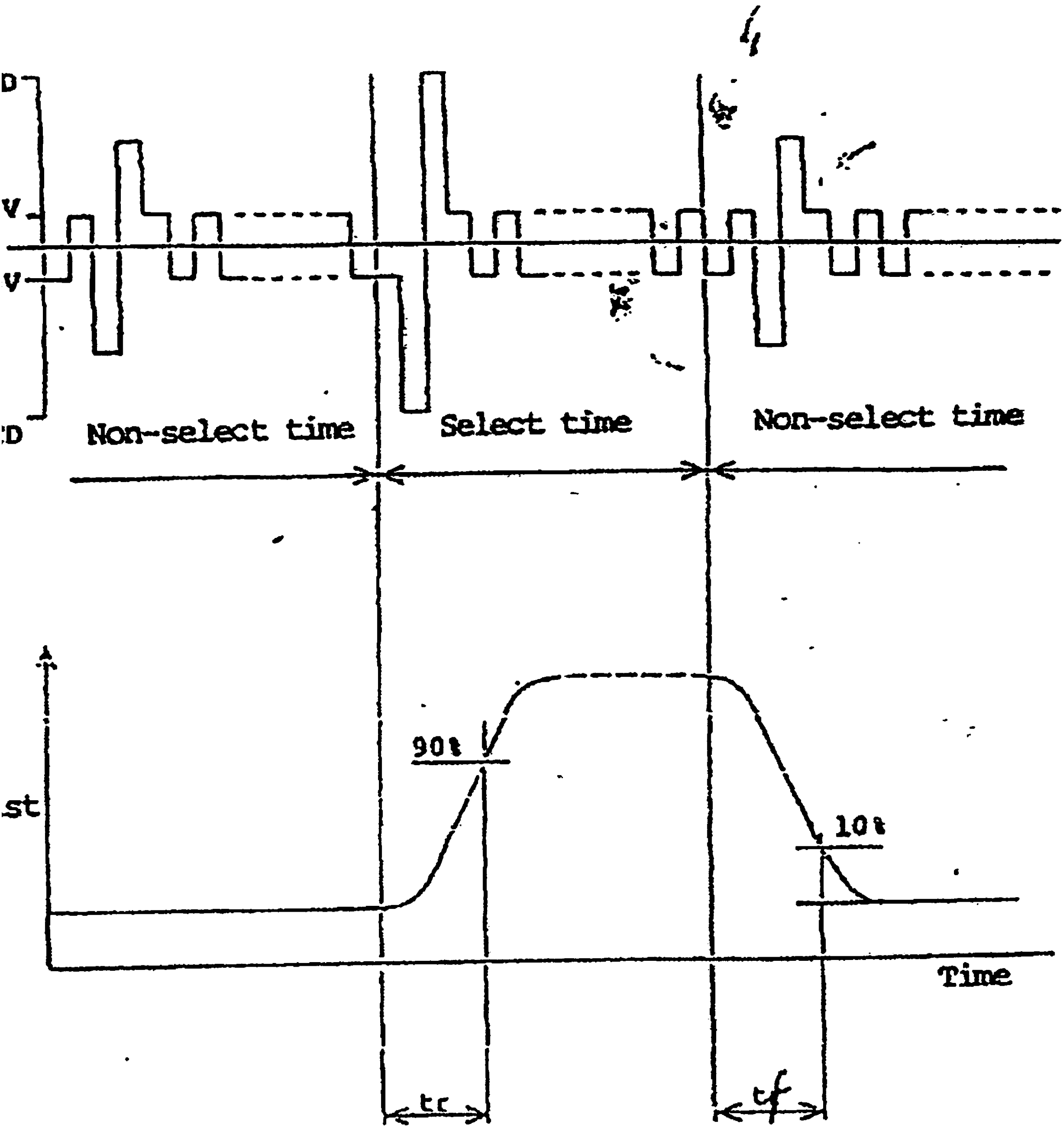
Brightness measuring spot diameter	ø0.3
Light source irradiation spot	ø10mm

L : Light source

P.M.: Brightness meter photo receiver



[NOTE 2] Definition of Response Time, and Measuring Conditions



[tr·tf] The segment whose response is the lowest is to be measured under the following conditions:

a) Ambient temperature : 0°C and 25°C

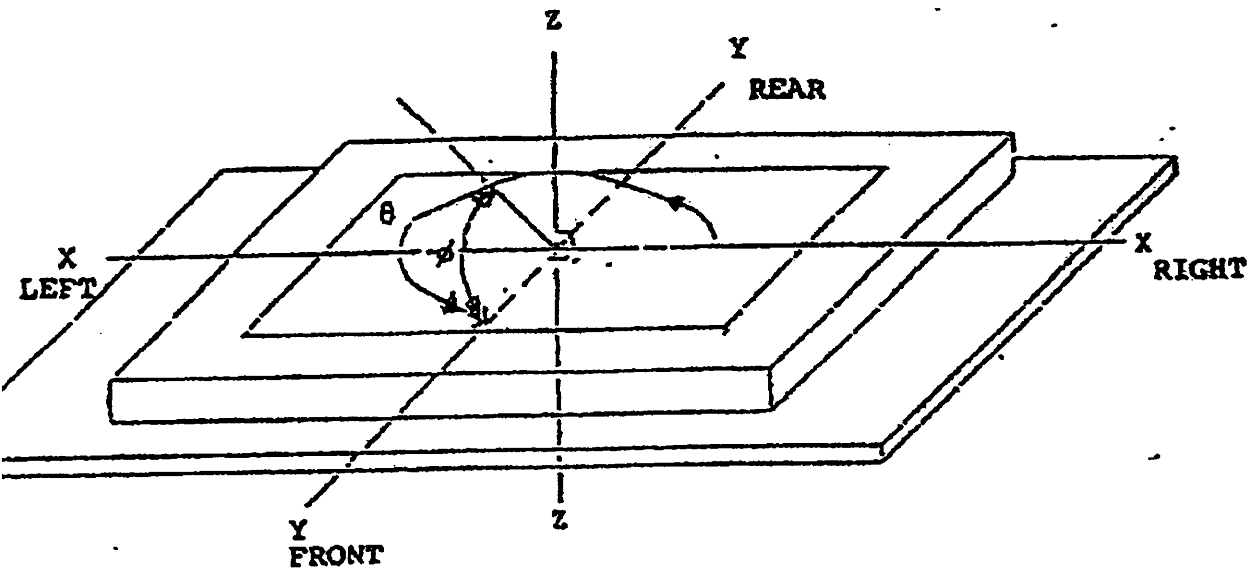
b) Frame frequency (f_F) : 64 Hz

c) Viewing angle : 70°

d) Drive voltage V_{OP} : 4.25V

NOTE 3] Definition of Viewing Angle Range

	Conditions	Min.	Max.	Unit
ont - rear	θ = 270°	60	80	DEG
ght - left	θ = 180°	60	120	DEG



NOTE 4] Definition of Contrast Ratio

- Definition

$$\text{Contrast ratio} = \frac{\text{Brightness with OFF voltage applie}}{\text{Brightness with ON volatge appliec}}$$

- Measuring conditions

a) Drive voltage V_{op} =4.25V

b) Ambient temperature Ta =25°C

c) Viewing angle θ =270°

ø =70°

HANDLING PRECAUTIONS

1) The display panel of the module is covered with a U.V. cut polarizer. Use extreme care when handling the panel because it is very vulnerable.

2) If the display panel gets dirty, clean it lightly with soft cloth (e.g., gauze) impregnated with one of the following solvents:

- isopropyl alcohol
- ethanol
- trichloro-trifluoro-ethane

Avoid using cloth or gauze alone that can damage the surface of the polarizer. Do not use the following solvents:

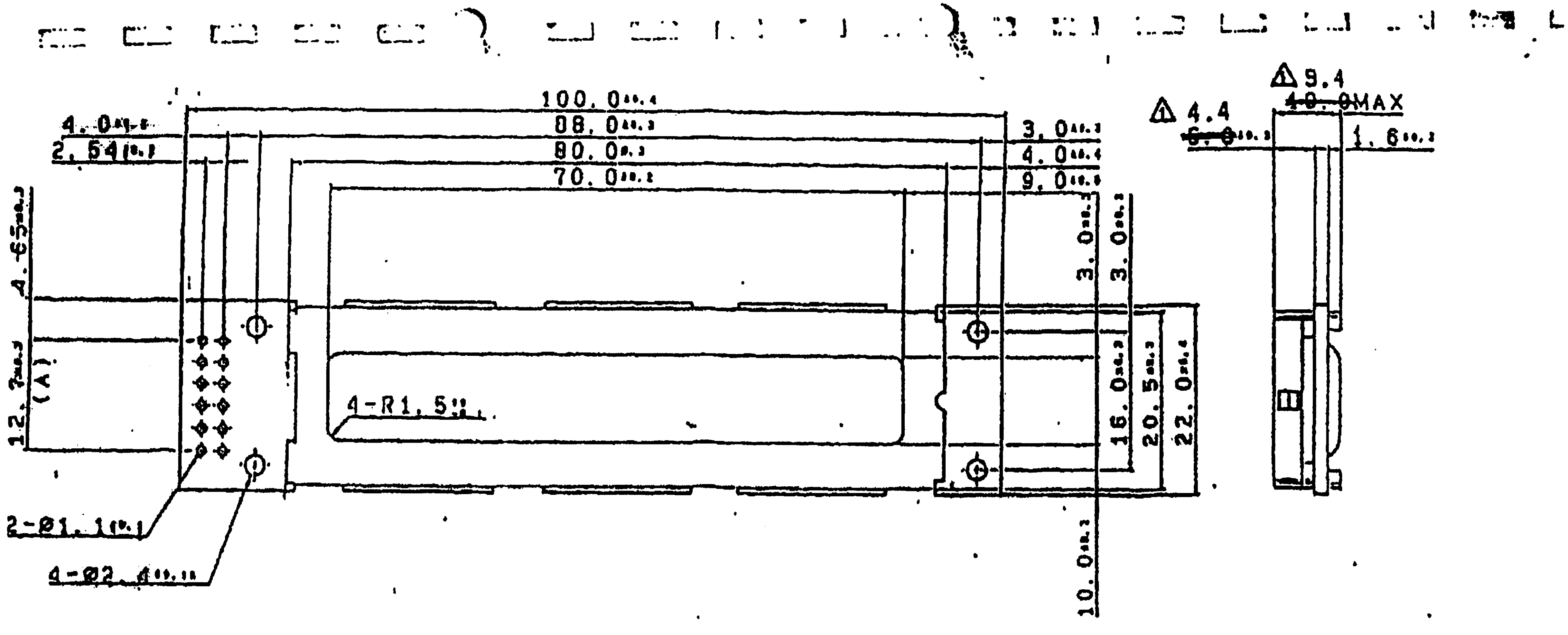
- water
- ketones
- aromatics

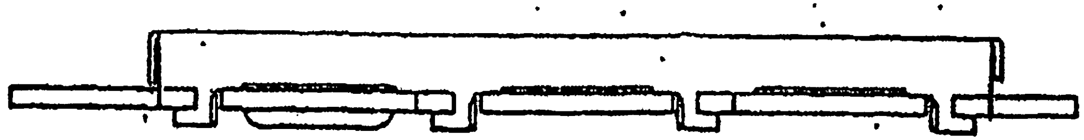
) Observe the following as the module uses CMOS LSI.

(a) Connect any unused input pins to V_{DD} or V_{SS}.
(b) Do not apply input signals to the module with no supply voltage applied.
(c) When doing assembly, use utmost care not to cause damage by electrostatic charge.

) Avoid applying strong shock to the module or letting it fall from a height. It does use liquid crystal display

) Avoid using or storing modules exposed direct to sunshine or high temperature/humidity which otherwise will shorten the life of LCD.





NOTES

(A) PITCH 2.54±0.2X(16-1)

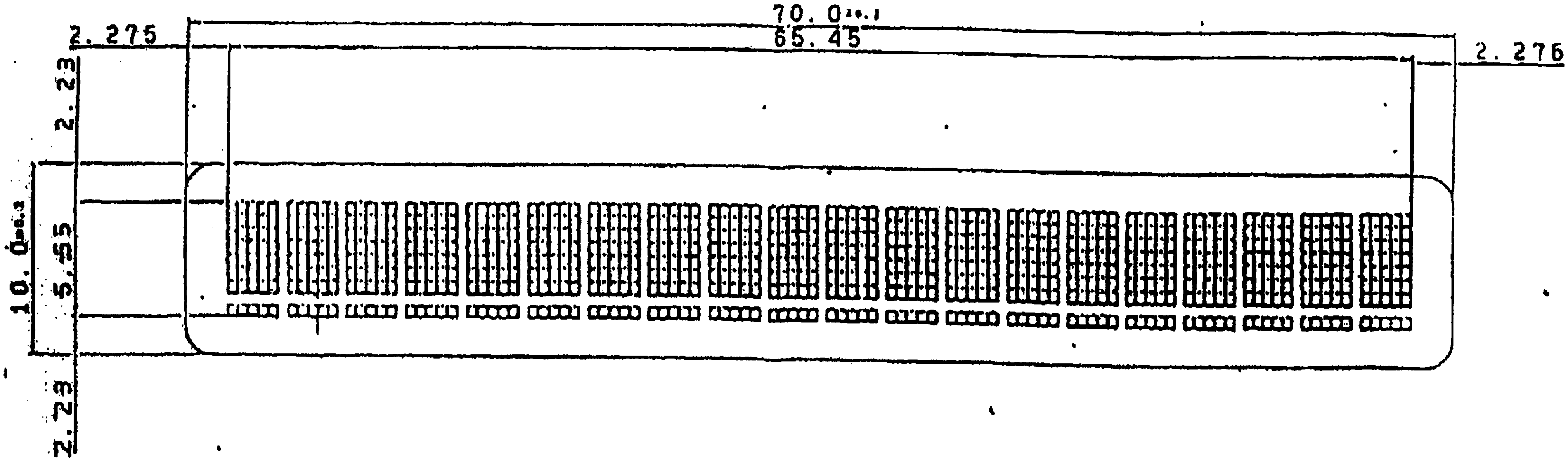
Δ Revision Date : 27th May, 85

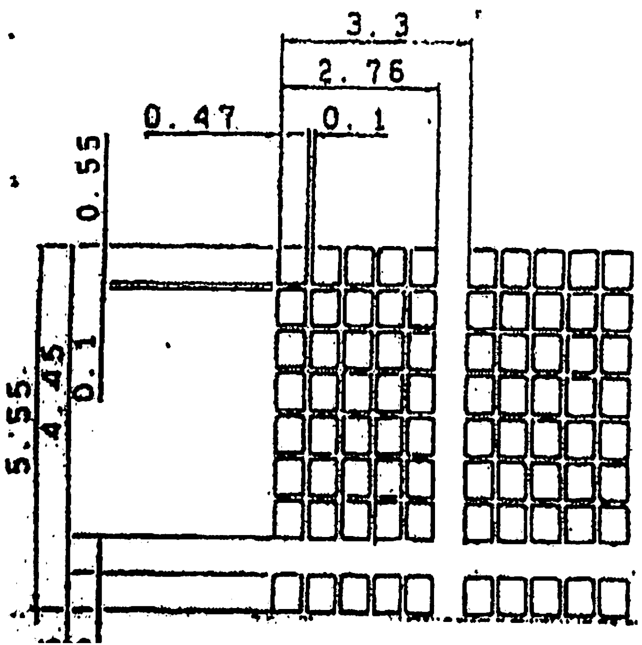
PIN ARRANGEMENT

1 ◆◆ 2
3 ◆◆ 4

Outline Drawing

(DWG. No. TD-270019-A)





NOTE

(1)DO NOT SCALE

Outline Drawing

:A-C20017AR TENTATIVE SPECIFICATIONS No. SB-6002.

pared on October 18, 1984.

ied by EPSON CORPORATION
Display Division, Toyoshina Branch
6925 Tazawa, Toyoshina, minamiazumi-gun
Nagano 399-82 JAPAN Tel.:(0263)72-1324

:ion: Information contained in this TENTATIVE SPECIFICATIONS is subject to changes without notice. Confirm the information before using the final specification.

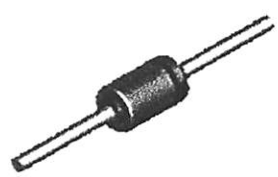
FAIRCHILD
SEMICONDUCTOR™

Discrete POWER & Signal Technologies

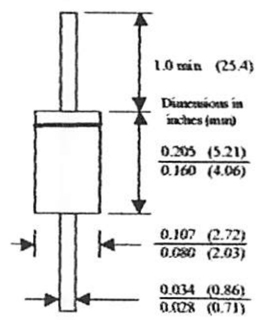
1N4001 - 1N4007

Features

- Low forward voltage drop.
- High surge current capability.



DO-41
COLOR BAND DENOTES CATHODE



1.0 Ampere General Purpose Rectifiers

Absolute Maximum Ratings*

T_A = 25°C unless otherwise noted

Symbol	Parameter	Value	Units
I_O	Average Rectified Current .375 " lead length @ T_A = 75°C	1.0	A
$i_{f(surge)}$	Peak Forward Surge Current 8.3 ms single half-sine-wave Superimposed on rated load (JEDEC method)	30	A
P_D	Total Device Dissipation Derate above 25°C	2.5 20	W mW/°C
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient	50	°C/W
T_{stg}	Storage Temperature Range	-55 to +175	°C
T_J	Operating Junction Temperature	-55 to +150	°C

*These ratings are limiting values above which the serviceability of any semiconductor device may be impaired.

Electrical Characteristics

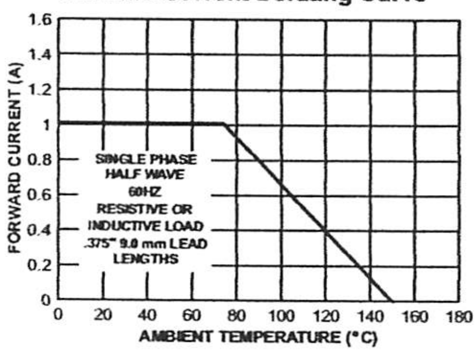
T_A = 25°C unless otherwise noted

Parameter	Device							Units
	4001	4002	4003	4004	4005	4006	4007	
Peak Repetitive Reverse Voltage	50	100	200	400	600	800	1000	V
Maximum RMS Voltage	35	70	140	280	420	560	700	V
DC Reverse Voltage (Rated V_R)	50	100	200	400	600	800	1000	V
Maximum Reverse Current @ rated V_R T_A = 25°C T_A = 100°C	5.0 500							µA µA
Maximum Forward Voltage @ 1.0 A	1.1							V
Maximum Full Load Reverse Current, Full Cycle T_A = 75°C	30							µA
Typical Junction Capacitance V_R = 4.0 V, f = 1.0 MHz	15							pF

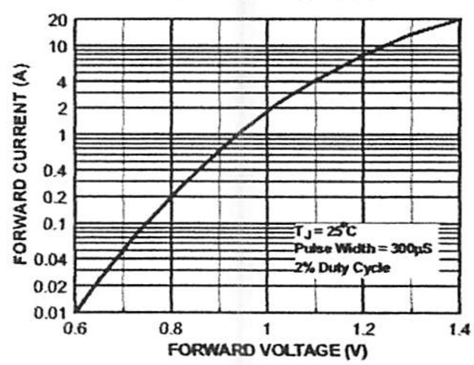
General Purpose Rectifiers
(continued)

Typical Characteristics

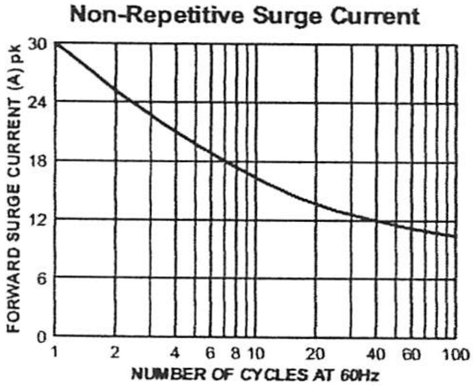
Forward Current Derating Curve



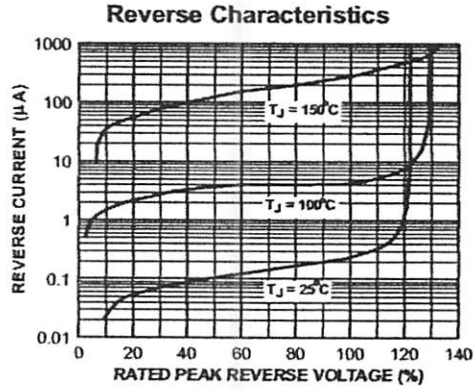
Forward Characteristics



Non-Repetitive Surge Current



Reverse Characteristics



National Semiconductor

February 1995

LM555/LM555C Timer

General Description

The LM555 is a highly stable device for generating accurate time delays or oscillation. Additional terminals are provided for triggering or resetting if desired. In the time delay mode of operation, the time is precisely controlled by one external resistor and capacitor. For astable operation as an oscillator, the free running frequency and duty cycle are accurately controlled with two external resistors and one capacitor. The circuit may be triggered and reset on falling waveforms, and the output circuit can source or sink up to 200 mA or drive TTL circuits.

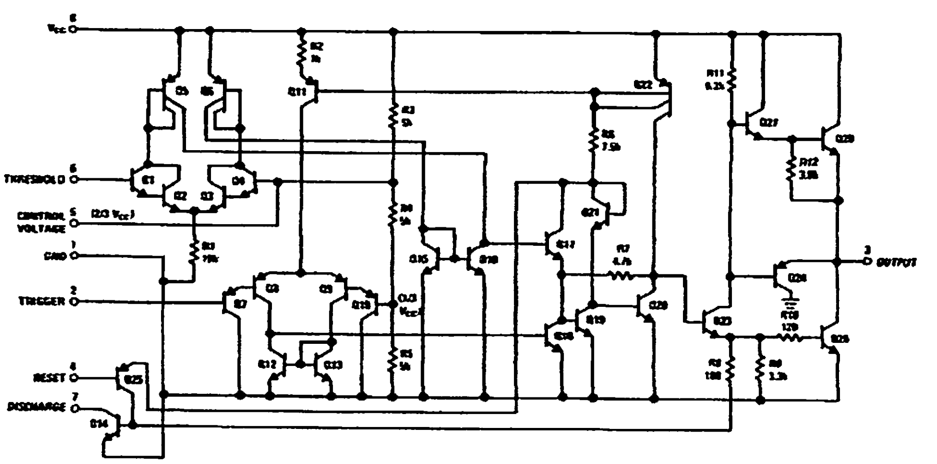
Features

- Direct replacement for SE555/NE555
- Timing from microseconds through hours
- Operates in both astable and monostable modes
- Adjustable duty cycle
- Output can source or sink 200 mA
- Output and supply TTL compatible
- Temperature stability better than 0.005% per °C
- Normally on and normally off output

Applications

- Precision timing
- Pulse generation
- Sequential timing
- Time delay generation
- Pulse width modulation
- Pulse position modulation
- Linear ramp generator

Schematic Diagram



TL/H/7851-1

\bsolute Maximum Ratings

f Military/Aerospace specified devices are required, lease contact the National Semiconductor Sales Office/Distributors for availability and specifications.

iupply Voltage	+18V
'ower Dissipation (Note 1)	
LM555H, LM555CH	760 mW
LM555, LM555CN	1180 mW
)perating Temperature Ranges	
LM555C	0°C to +70°C
LM555	−55°C to +125°C
Storage Temperature Range	−65°C to +150°C
Soldering Information	
Dual-In-Line Package	
Soldering (10 Seconds)	260°C
Small Outline Package	
Vapor Phase (60 Seconds)	215°C
Infrared (15 Seconds)	220°C

See AN-450 "Surface Mounting Methods and Their Effect on Product Reliability" for other methods of soldering surface mount devices.

:lectrical Characteristics (T_A = 25°C, V_{CC} = +5V to +15V, unless othewise specified)

Parameter	Conditions	Limits LM555 Min	LM555 Typ	LM555 Max	LM555C Min	LM555C Typ	LM555C Max	Units
ıpply Voltage		4.5		18	4.5		16	V
ıpply Current	V_{CC} = 5V, R_L = ∞ V_{CC} = 15V, R_L = ∞ (Low State) (Note 2)		3 10	5 12		3 10	6 15	mA mA
ming Error, Monostable Initial Accuracy Drift with Temperature Accuracy over Temperature Drift with Supply	R_A = 1k to 100 kΩ, C = 0.1 μF, (Note 3)		0.5 30 1.5 0.05			1 50 1.5 0.1		% ppm/°C % %/V
ming Error, Astable Initial Accuracy Drift with Temperature Accuracy over Temperature Drift with Supply	R_A, R_B = 1k to 100 kΩ, C = 0.1 μF, (Note 3)		1.5 90 2.5 0.15			2.25 150 3.0 0.30		% ppm/°C % %/V
ıreshold Voltage			0.667			0.667		x V_{CC}
igger Voltage	V_{CC} = 15V V_{CC} = 5V	4.8 1.45	5 1.67	5.2 1.9		5 1.67		V V
igger Current			0.01	0.5		0.5	0.9	μA
eset Voltage		0.4	0.5	1	0.4	0.5	1	V
eset Current			0.1	0.4		0.1	0.4	mA
ıreshold Current	(Note 4)		0.1	0.25		0.1	0.25	μA
ontrol Voltage Level	V_{CC} = 15V V_{CC} = 5V	9.6 2.9	10 3.33	10.4 3.8	9 2.6	10 3.33	11 4	V V
n 7 Leakage Output High			1	100		1	100	nA
n 7 Sat (Note 5) Output Low Output Low	 V_{CC} = 15V, I_7 = 15 mA V_{CC} = 4.5V, I_7 = 4.5 mA		 150 70	 100		 180 80	 200	 mV mV

Electrical Characteristics $T_A = 25°C$, $V_{CC} = +5V$ to $+15V$, (unless othewise specified) (Continued)

Parameter	Conditions	Limits						Units
		LM555			LM555C			
		Min	Typ	Max	Min	Typ	Max	
Output Voltage Drop (Low)	$V_{CC} = 15V$							
	$I_{SINK} = 10$ mA		0.1	0.15		0.1	0.25	V
	$I_{SINK} = 50$ mA		0.4	0.5		0.4	0.75	V
	$I_{SINK} = 100$ mA		2	2.2		2	2.5	V
	$I_{SINK} = 200$ mA		2.5			2.5		V
	$V_{CC} = 5V$							
	$I_{SINK} = 8$ mA		0.1	0.25				V
	$I_{SINK} = 5$ mA					0.25	0.35	V
Output Voltage Drop (High)	$I_{SOURCE} = 200$ mA, $V_{CC} = 15V$		12.5			12.5		V
	$I_{SOURCE} = 100$ mA, $V_{CC} = 15V$	13	13.3		12.75	13.3		V
	$V_{CC} = 5V$	3	3.3		2.75	3.3		V
Rise Time of Output			100			100		ns
Fall Time of Output			100			100		ns

Note 1: For operating at elevated temperatures the device must be derated above 25°C based on a +150°C maximum junction temperature and a thermal resistance of 164°c/w (T0-5), 106°c/w (DIP) and 170°c/w (S0-8) junction to ambient.

Note 2: Supply current when output high typically 1 mA less at $V_{CC} = 5V$.

Note 3: Tested at $V_{CC} = 5V$ and $V_{CC} = 15V$.

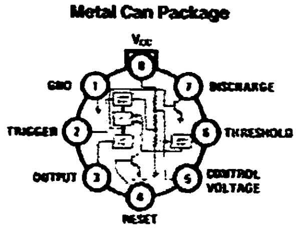
Note 4: This will determine the maximum value of $R_A + R_B$ for 15V operation. The maximum total $(R_A + R_B)$ is 20 MΩ.

Note 5: No protection against excessive pin 7 current is necessary providing the package dissipation rating will not be exceeded.

Note 6: Refer to RETS555X drawing of military LM555H and LM555J versions for specifications.

Connection Diagrams

Metal Can Package

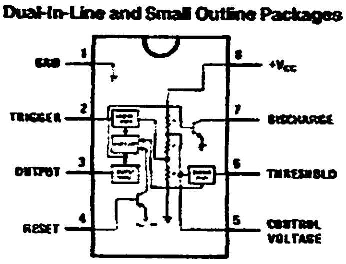


TL/H/7851-2

Top View

Order Number LM555H or LM555CH
See NS Package Number H08C

Dual-In-Line and Small Outline Packages



TL/H/7851-3

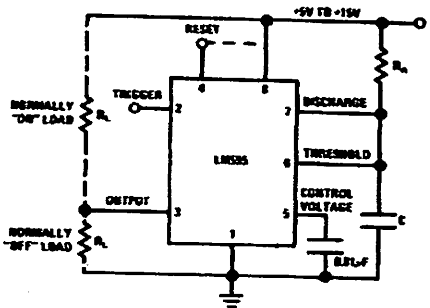
Top View

Order Number LM555J, LM555CJ, LM555CM or LM555CN
See NS Package Number J08A, M08A or N08E

Applications Information

MONOSTABLE OPERATION

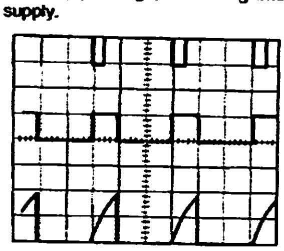
In this mode of operation, the timer functions as a one-shot (*Figure 1*). The external capacitor is initially held discharged by a transistor inside the timer. Upon application of a negative trigger pulse of less than 1/3 V_{CC} to pin 2, the flip-flop is set which both releases the short circuit across the capacitor and drives the output high.



TL/H/7851-5

FIGURE 1. Monostable

The voltage across the capacitor then increases exponentially for a period of $t = 1.1\ R_A\ C$, at the end of which time the voltage equals 2/3 V_{CC}. The comparator then resets the flip-flop which in turn discharges the capacitor and drives the output to its low state. *Figure 2* shows the waveforms generated in this mode of operation. Since the charge and the threshold level of the comparator are both directly proportional to supply voltage, the timing internal is independent of supply.



TL/H/7851-6

V_{CC} = 5V
TIME = 0.1 ms/DIV.
R_A = 9.1 kΩ
C = 0.01 μF

Top Trace: Input 5V/Div.
Middle Trace: Output 5V/Div.
Bottom Trace: Capacitor Voltage 2V/Div.

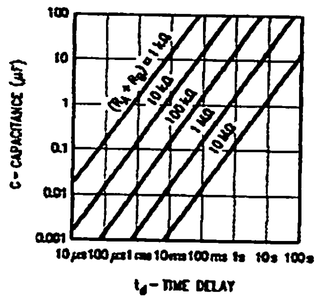
FIGURE 2. Monostable Waveforms

During the timing cycle when the output is high, the further application of a trigger pulse will not effect the circuit so long as the trigger input is returned high at least 10 μs before the end of the timing interval. However the circuit can be reset during this time by the application of a negative pulse to the reset terminal (pin 4). The output will then remain in the low state until a trigger pulse is again applied.

When the reset function is not in use, it is recommended that it be connected to V_{CC} to avoid any possibility of false triggering.

Figure 3 is a nomograph for easy determination of R, C values for various time delays.

NOTE: In monostable operation, the trigger should be driven high before the end of timing cycle.

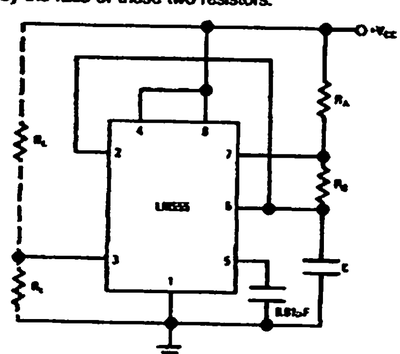


TL/H/7851-7

FIGURE 3. Time Delay

ASTABLE OPERATION

If the circuit is connected as shown in *Figure 4* (pins 2 and 6 connected) it will trigger itself and free run as a multivibrator. The external capacitor charges through $R_A + R_B$ and discharges through R_B. Thus the duty cycle may be precisely set by the ratio of these two resistors.



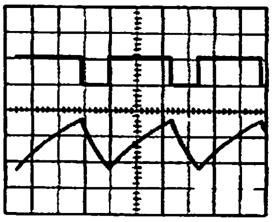
TL/H/7851-8

FIGURE 4. Astable

In this mode of operation, the capacitor charges and discharges between 1/3 V_{CC} and 2/3 V_{CC}. As in the triggered mode, the charge and discharge times, and therefore the frequency are independent of the supply voltage.

\pplications Information (Continued)

igure 5 shows the waveforms generated in this mode of peration.



TL/H/7851-9

V_{CC} = 5V
TIME = 20 µs/DIV.
R_A = 3.9 kΩ
R_B = 3 kΩ
C = 0.01 µF

Top Trace: Output 5V/Div.
Bottom Trace: Capacitor Voltage 1V/Div.

FIGURE 5. Astable Waveforms

The charge time (output high) is given by:

$$t_1 = 0.693\,(R_A + R_B)\,C$$

And the discharge time (output low) by:

$$t_2 = 0.693\,(R_B)\,C$$

Thus the total period is:

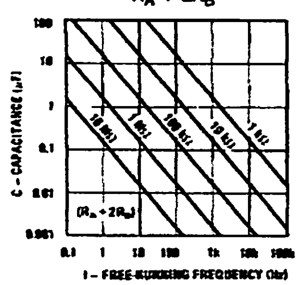
$$T = t_1 + t_2 = 0.693\,(R_A + 2R_B)\,C$$

The frequency of oscillation is:

$$f = \frac{1}{T} = \frac{1.44}{(R_A + 2\,R_B)\,C}$$

igure 6 may be used for quick determination of these RC alues.

The duty cycle is: $D = \dfrac{R_B}{R_A + 2R_B}$

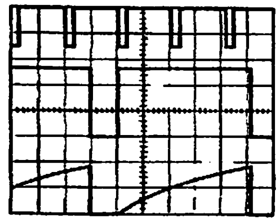


TL/H/7851-10

FIGURE 6. Free Running Frequency

FREQUENCY DIVIDER

The monostable circuit of *Figure 1* can be used as a frequency divider by adjusting the length of the timing cycle. *Figure 7* shows the waveforms generated in a divide by three circuit.



TL/H/7851-11

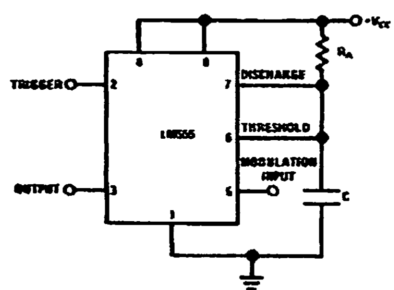
V_{CC} = 5V
TIME = 20 µs/DIV.
R_A = 9.1 kΩ
C = 0.01 µF

Top Trace: Input 4V/Div.
Middle Trace: Output 2V/Div.
Bottom Trace: Capacitor 2V/Div.

FIGURE 7. Frequency Divider

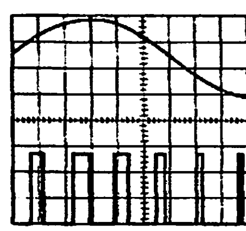
PULSE WIDTH MODULATOR

When the timer is connected in the monostable mode and triggered with a continuous pulse train, the output pulse width can be modulated by a signal applied to pin 5. *Figure 8* shows the circuit, and in *Figure 9* are some waveform examples.



TL/H/7851-12

FIGURE 8. Pulse Width Modulator



TL/H/7851-13

V_{CC} = 5V
TIME = 0.2 ms/DIV.
R_A = 9.1 kΩ
C = 0.01 µF

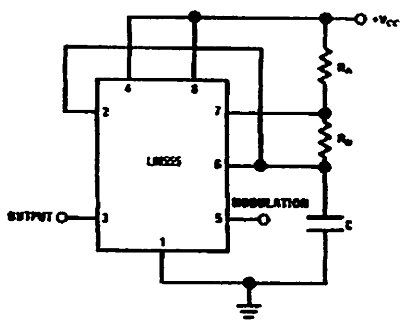
Top Trace: Modulation 1V/Div.
Bottom Trace: Output Voltage 2V/Div.

FIGURE 9. Pulse Width Modulator

PULSE POSITION MODULATOR

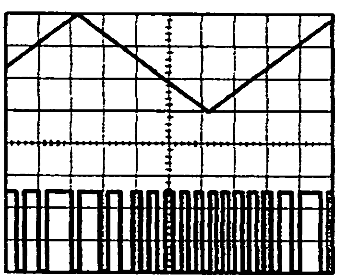
This application uses the timer connected for astable operation, as in *Figure 10*, with a modulating signal again applied to the control voltage terminal. The pulse position varies with the modulating signal, since the threshold voltage and hence the time delay is varied. *Figure 11* shows the waveforms generated for a triangle wave modulation signal.

Applications Information (Continued)



TL/H/7851–14

FIGURE 10. Pulse Position Modulator



TL/H/7851–15

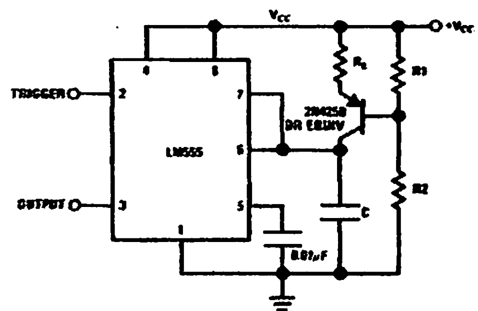
V_{CC} = 5V
TIME = 0.1 ms/DIV.
R_A = 3.9 kΩ
R_B = 3 kΩ
C = 0.01 μF

Top Trace: Modulation Input 1V/Div.
Bottom Trace: Output 2V/Div.

FIGURE 11. Pulse Position Modulator

LINEAR RAMP

When the pullup resistor, R_A, in the monostable circuit is replaced by a constant current source, a linear ramp is generated. *Figure 12* shows a circuit configuration that will perform this function.



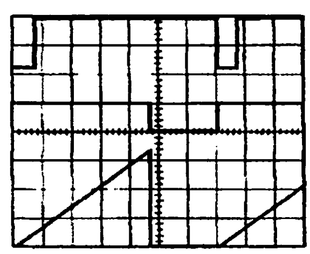
TL/H/7851–16

FIGURE 12

Figure 13 shows waveforms generated by the linear ramp. The time interval is given by:

$$T = \frac{2/3\, V_{CC}\, R_E\, (R_1 + R_2)\, C}{R_1\, V_{CC} - V_{BE}\, (R_1 + R_2)}$$

$$V_{BE} \cong 0.6V$$



TL/H/7851–17

V_{CC} = 5V
TIME = 20 μs/DIV.
R_1 = 47 kΩ
R_2 = 100 kΩ
R_E = 2.7 kΩ
C = 0.01 μF

Top Trace: Input 3V/Div.
Middle Trace: Output 5V/Div.
Bottom Trace: Capacitor Voltage 1V/Div.

FIGURE 13. Linear Ramp

50% DUTY CYCLE OSCILLATOR

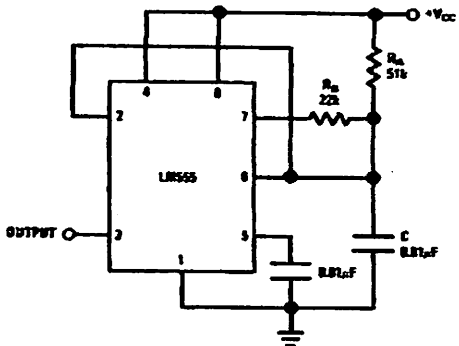
For a 50% duty cycle, the resistors R_A and R_B may be connected as in *Figure 14.* The time period for the out-

Applications Information (Continued)

put high is the same as previous, $t_1 = 0.693\ R_A\ C$. For the output low it is $t_2 =$

$$\left[(R_A R_B)/(R_A + R_B)\right] C\ \ln \left[\frac{R_B - 2R_A}{2R_B - R_A}\right]$$

Thus the frequency of oscillation is $f = \frac{1}{t_1 + t_2}$



TL/H/7851-18

FIGURE 14. 50% Duty Cycle Oscillator

Note that this circuit will not oscillate if R_B is greater than 1/2 R_A because the junction of R_A and R_B cannot bring pin 2 down to 1/3 V_{CC} and trigger the lower comparator.

ADDITIONAL INFORMATION

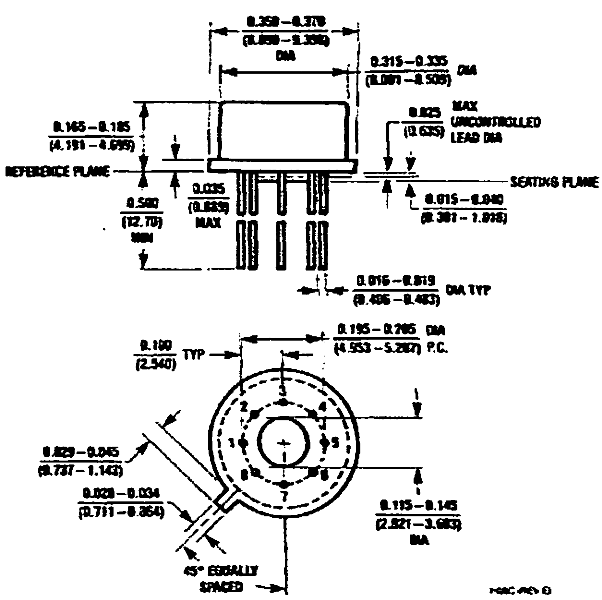
Adequate power supply bypassing is necessary to protect associated circuitry. Minimum recommended is 0.1 µF in parallel with 1 µF electrolytic.

Lower comparator storage time can be as long as 10 µs when pin 2 is driven fully to ground for triggering. This limits the monostable pulse width to 10 µs minimum.

Delay time reset to output is 0.47 µs typical. Minimum reset pulse width must be 0.3 µs, typical.

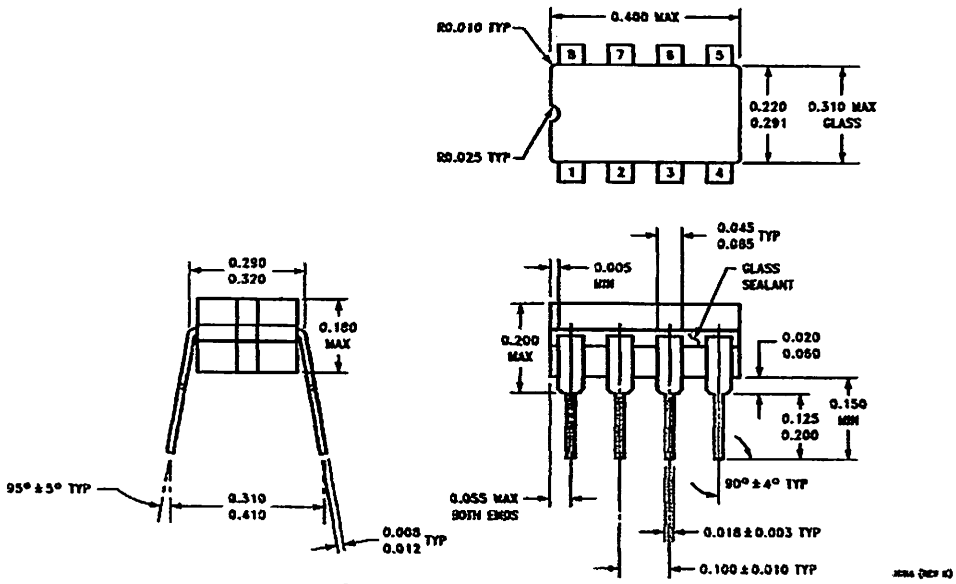
Pin 7 current switches within 30 ns of the output (pin 3) voltage.

Physical Dimensions inches (millimeters)

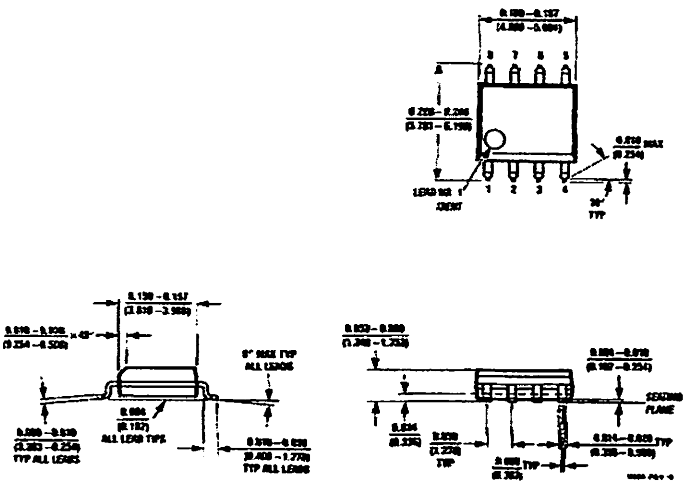


Metal Can Package (H)
Order Number LM555H or LM555CH
NS Package Number H08C

Physical Dimensions inches (millimeters) (Continued)

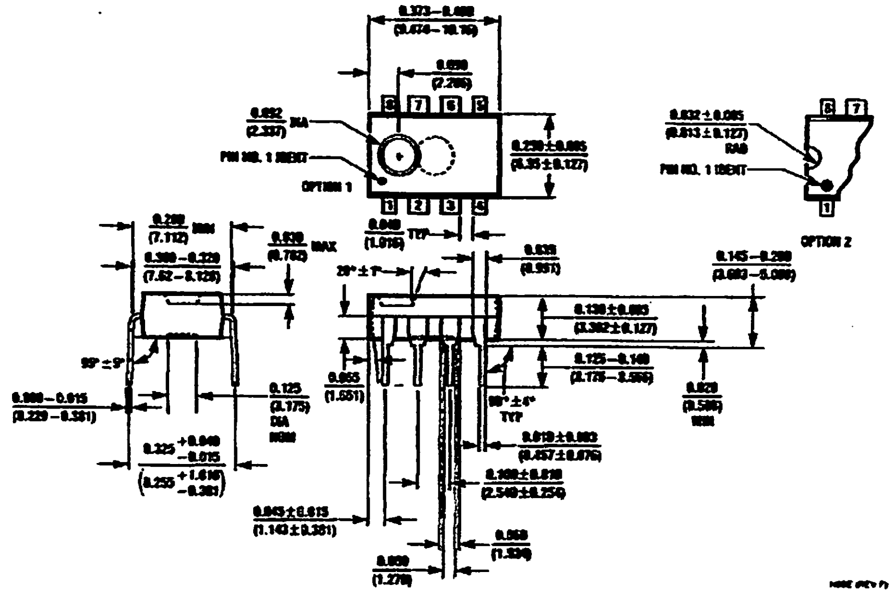


Ceramic Dual-In-Line Package (J)
Order Number LM555J or LM555CJ
NS Package Number J08A



Small Outline Package (M)
Order Number LM555CM
NS Package Number M08A

Physical Dimensions inches (millimeters) (Continued)



Molded Dual-In-Line Package (N)
Order Number LM555CN
NS Package Number N08E

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2. A critical component is any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

National Semiconductor Corporation
1111 West Bardin Road
Arlington, TX 76017
Tel: 1(800) 272-9959
Fax: 1(800) 737-7018

National Semiconductor Europe
Fax: (+49) 0-180-530 85 86
Email: cnjwge@tevm2.nsc.com
Deutsch Tel: (+49) 0-180-530 85 85
English Tel: (+49) 0-180-532 78 32
Français Tel: (+49) 0-180-532 93 58
Italiano Tel: (+49) 0-180-534 16 80

National Semiconductor Hong Kong Ltd.
13th Floor, Straight Block,
Ocean Centre, 5 Canton Rd.
Tsimshatsui, Kowloon
Hong Kong
Tel: (852) 2737-1600
Fax: (852) 2736-9960

National Semiconductor Japan Ltd.
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TechNote

LT03-0020 • July, 2006

Capacitive Sensor Operation and Optimization

Applicable Equipment:

Capacitive displacement measurement systems.

Applications:

All capacitive measurements.

Summary:

This TechNote reviews concepts and theory of capacitive sensing to help in optimizing capacitive sensor performance. It also defines capacitive sensing terms as used throughout Lion Precision literature and manuals.

:ision • 563 Shoreview Park Rd. • St. Paul, MN 55126 • 651-484-6544 • www.lionprecision.com • info@lionprecision.com

A Capacitive Measurement System

Capacitive dimensional measurement requires three basic components:

- a probe that uses changes in capacitance to sense changes in distance to the target,
- driver electronics to convert these changes in capacitance into voltage changes,
- a device to indicate and/or record the resulting voltage change.

Each of these components is a critical part in providing reliable, accurate measurements. The probe geometry, sensing area size, and mechanical construction effect range, accuracy, and stability. A probe requires a driver to provide the changing electric field that is used to sense the capacitance. The driver electronics are a primary factor in determining the resolution of the system and must be well designed. The voltage measuring device is the final link in the system. Oscilloscopes, voltmeters and data acquisition systems must be properly selected for the application.

What is Capacitance?

Capacitance describes how the space between two conductors effects an electric field between them. If two steel plates are placed with a gap between them and a voltage is applied to one of the plates, an electric field will exist between the plates. This electric field is the result of the difference between electric charges that are stored on the surfaces of the plates. Capacitance refers to the "capacity" of the two plates to hold this charge. A large capacitance has the capacity to hold more charge than a small capacitance. The amount of existing charge determines how much current must be used to change the voltage on the plate. It's like trying to change the water level by one inch in a fifty-five gallon drum compared to a coffee cup. It takes a lot of water to move the level one inch in the drum, but in a coffee cup it takes very little water. The difference is their capacity.

When using a capacitance sensor, the sensor surface is the electrified plate and what you're measuring (the target) is the other plate (we'll talk about measuring non-conductive targets later). The sensor electronics continually change the voltage on the sensor surface. This is called the excitation voltage. The amount of current required to make the change is measured by the circuit and indicates the amount of capacitance between the probe and the target.

ce is measured in Farads,
er Michael Faraday who did
experiments in electricity
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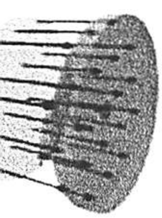

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$$\frac{\text{Area x Dielectric}}{\text{Gap}}$$

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$$C \approx \frac{1}{\text{Gap}}$$

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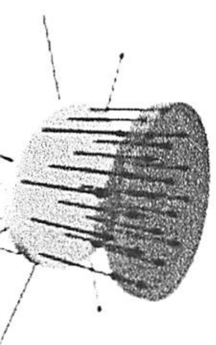

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a guard to focus the electric

How Capacitance Relates to Distance

The capacitance between two plates is determined by three things:

- Size of the plates: capacitance increases as the plate size increases
- Gap Size: capacitance decreases as the gap increases
- Material between the plates (the dielectric): dielectric material will cause the capacitance to increase or decrease depending on the material

In ordinary capacitance sensing the size of the sensor, the size of the target, and the dielectric material (air) remain constant. The only variable is the gap size. Based on this assumption, driver electronics assume that all changes in capacitance are a result of a change in gap size. The electronics are calibrated to output specific voltage changes for corresponding changes in capacitance. These voltages are scaled to represent specific changes in gap size. The amount of voltage change for a given amount of gap change is called the sensitivity. A common sensitivity setting is 1.0V/100µm. That means that for every 100µm change in the gap, the output voltage changes exactly 1.0V. With this calibration, a +2V change in the output means that the target has moved 200µm closer to the probe.

Focusing the Electric Field

When a voltage is applied to a conductor, there is an electric field coming from every surface. For accurate gaging, the electric field from a probe needs to be contained within the space between the probe's sensing area and the target. If the electric field is allowed to spread to other items or other areas on the target then a change in the position of the other item will be measured as a change in the position of the target. To prevent this from happening a technique called guarding is used. To create a guarded probe, the back and sides of the sensing area are surrounded by another conductor that is kept at the same voltage as the sensing area itself. When the excitation voltage is applied to the sensing area, a separate circuit applies the exact same voltage to the guard. Because there is no difference in voltage between the sensing area and the guard, there is no electric field between them. Any other conductors beside or behind the probe form an electric field with the guard instead of the sensing area. Only the unguarded front of the sensing area is allowed to form an electric field to the target.

r's electric field covers an
: 30% larger than the sensing
: probe.

the maximum gap at which a
seful is approximately 40% of
diameter. Standard calibra-
lly keep the gap considerably
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tiple probes on the same tar-
s that the excitation voltages
nized. This is accomplished
ring one driver as a master
: as slaves.

sensors measure all conduc-
, steel, aluminum, or even
with equal accuracy.

Effects of Target Size

The target size is a primary consideration when selecting a probe for a specific application. When the sensor's electric field is focused by guarding, it creates a field that is a projection of the sensor size and shape. The minimum target diameter for standard calibration is 30% of the diameter of the sensing area. The further the probe is from the target, the larger the minimum target size.

Range of Measurement

The range in which a probe is useful is a function of the area of the sensor. The greater the area, the larger the range. The driver electronics are designed for a certain amount of capacitance at the sensor. Therefore, a smaller sensor must be considerably closer to the target to achieve the desired amount of capacitance. The electronics are adjustable during calibration but there is a limit to the range of adjustment.

In general, the maximum gap at which a probe is useful is approximately 40% of the sensor diameter. Standard calibrations usually keep the gap considerably less than that.

Multiple Channel Sensing

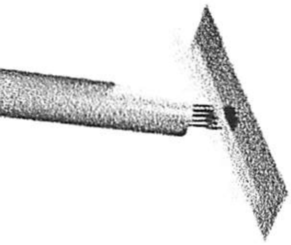
Frequently, a target is measured simultaneously by multiple probes. Because the system measures a changing electric field, the excitation voltage for each probe must be synchronized or the probes would interfere with each other. If they were not synchronized, one probe would be trying to increase the electric field while another was trying to decrease it thereby giving a false reading.

Driver electronics can be configured as masters or slaves. The master sets the synchronization for the slaves in multiple channel systems.

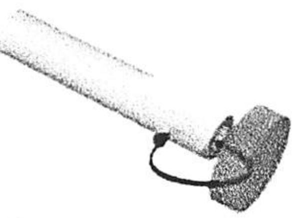
Effects of Target Material

The electric field from the probe sensor is seeking a conductive surface. For this reason, capacitance sensors are not effected by the target material provided that it is a conductor. Because the electric field from the sensor stops at the surface of the conductor, target thickness does not effect the measurement.

Surface finish can effect the measurement. Capacitance probes will measure the average position of the target surface within the spot size of the sensor.



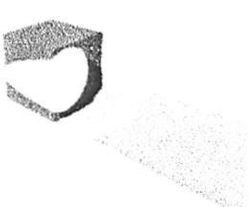
ctors can be measured by electric field through them to a onductive target behind.



be used to measure non-argets without a conductive target.

al	Dielectric Constant Relative (ξ_r)
n	1.0
	1.0006
	2.5-6.0
	2.8-3.1
	3.7-10.0
	80.0

nstants of common materials



ts make measurement ac-sitive to small probe post ion

Measuring Non-Conductors

Capacitance probes are most often used to measure the change in position of a conductive target. But capacitance probes can be very effective in measuring presence, density, thickness, and location of non-conductors as well. Non-conductive materials like plastic have a different dielectric constant than air. The dielectric constant determines how a non-conductive material effects capacitance between two conductors. By inserting a non-conductive material in the gap between the probe and a stationary reference target, the capacitance will change in relationship to the thickness, density, or location of the material.

Sometimes it's not feasible to have a reference target in front of the probe. Often, measurements can still be made by a technique called fringing. If there is no conductive surface directly in front of the probe, the sensor's electric field will wrap back to the shell of the probe itself. This is called a fringe field. If a non-conductive material is brought in proximity to the probe, its dielectric will change the fringe field and this can be used to measure the non-conductive material.

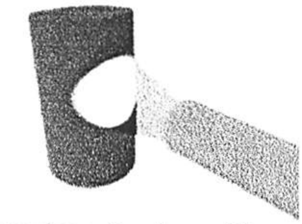
Maximizing Accuracy

Now that we've discussed the basics of how capacitance gaging works, we can form some strategies for maximizing effectiveness and minimizing error when capacitance gaging systems are used. Accuracy requires that the measurements be made under the same conditions in which the system was calibrated. Whether it's a system calibrated at the factory, or one that's calibrated during use, repeatable results come from repeatable conditions. If we only want the gap size to change the reading, then all the other variables must be constant. The following sections discuss sources of these errors and how to minimize them.

Target Size

Unless otherwise specified, factory calibrations are done with a flat conductive target that is considerably larger than the sensor area. A system calibrated in this way will give accurate results when measuring a flat target more than 30% larger than the sensing area. If the target area is too small, the electric field will begin to wrap around the sides of the target. In this case, the electric field extends farther than it did in calibration and will measure the target as farther away. This means that the probe must be closer to the target for the same zero point. Because this distance differs from the original calibration, error will be introduced. Error is also created because the probe is no longer measuring a flat surface.

An additional problem of an undersized target is that the system becomes sensitive to X and Y location of the probe relative to the target. Without changing the gap, the output will change significantly if the probe is moved up, down, left, or right because less of the electric field is going to the center of the target and more is going around to the sides.



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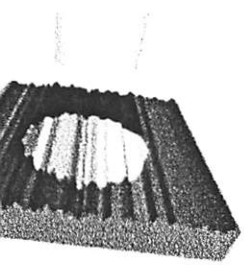

rface finish can cause different
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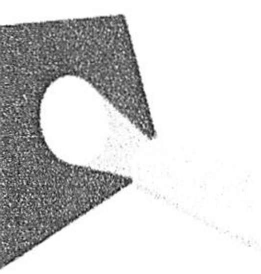

of the target is not parallel to
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drift.

Target Shape

Shape is also a consideration. Since the probes are calibrated to a flat target, measuring a target with a curved surface will cause errors. Because the probe will measure the average distance to the target, the gap at zero volts will be different than when the system was calibrated. Errors will also be introduced because of the different behavior of the electric field with the curved surface. In cases where a non-flat target must be measured, the system can be factory calibrated to the final target shape. Alternatively, when flat calibrations are used with curved surfaces, multipliers can be provided to correct the measurement value.

Surface Finish

When the target surface is not perfectly smooth, the system will average over the area covered by the spot size of the sensor. The measurement value can change as the probe is moved across the surface due to a change in the average location of the surface. The magnitude of this error depends on the nature and symmetry of the surface irregularities.

Parallelism

During calibration the surface of the sensor is parallel to the target surface. If the probe or target is tilted any significant amount, the shape of the spot where the field hits the target elongates and changes the interaction of the field between the probe and target. Because of the different behavior of the electric field, measurement errors will be introduced. Parallelism must be considered when designing a fixture for the measurement.

Environment

Lion Precision capacitance systems are compensated to minimize drift due to temperature from 22°C - 35°C (72°F - 95°F). In this temperature range errors are less than 0.5% of full scale.

A more troublesome problem is that virtually all target and fixture materials exhibit a significant expansion and contraction over this temperature range. When this happens, the changes in the measurement are not gage error. They are real changes in the gap between the target and the probe. Careful fixture design goes a long way toward maximizing accuracy.

The dielectric constant of air is affected by humidity. As humidity increases the dielectric increases. Humidity can also interact with probe construction materials. Experimental data shows that changes from 50%RH to 80%RH can cause errors up to 0.5% of full scale.

While Lion Precision probe materials are selected to minimize these errors, in applications requiring utmost precision, control of temperature and humidity is standard practice. International standards specify that measurements shall be done at 20°C or corrected to "true length" at 20°C.

Factory Calibration

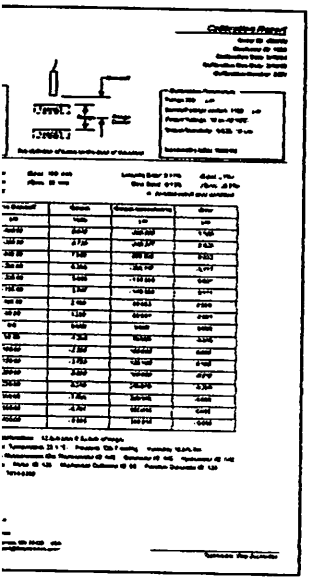
Lion Precision's calibration system was designed in cooperation with Professional Instruments, a world leader in air bearing spindle and slide design. It's state of the art design is driven by precision motion control electronics with positional accuracies of less than 0.012μm uncertainty.

The calibration system is certified on a regular basis with a NIST traceable laser interferometer. The measurement equipment used during calibration (digital meters and signal generators) are also calibrated to NIST traceable standards. The calibration information for each of these pieces of equipment is kept on file for verification of traceability.

Technicians use the calibration system to precisely position a calibration target at known gaps to the probe. The measurements at these points are collected and the sensitivity and linearity are analyzed by the calibration system. The analysis of the data is used to adjust the system being calibrated to meet order specifications.

After sensitivity and linearity are calibrated, the systems are placed in an environmental chamber where the temperature compensation circuitry is calibrated to minimize drift over the temperature range of 22°C to 35°C. Measurements are also taken of bandwidth and output noise which effect resolution.

When calibration is complete, a calibration certificate is generated. This certificate is shipped with the ordered system and archived. Calibration certificates conform to section 4.8 of ISO 10012-1.



:able calibration certificate

Definitions

Sensitivity

Sensitivity indicates how much the output voltage changes as a result of a change in the gap between the target and the probe. A common sensitivity is 1V/0.1mm. This means that for every 0.1mm of change in the gap, the output voltage will change 1V. When the output voltage is plotted against the gap size, the slope of the line is the sensitivity.

Sensitivity Error

A system's sensitivity is set during calibration. When sensitivity deviates from the ideal value this is called sensitivity error, gain error, or scaling error. Since sensitivity is the slope of a line, sensitivity error is usually presented as a percentage of slope; comparing the ideal slope with the actual slope.

Offset Error

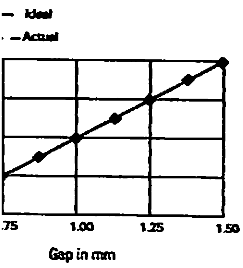
Offset error occurs when a constant value is added to the output voltage of the system. Capacitance gaging systems are usually "zeroed" during setup, eliminating any offset deviations from the original calibration. However, should the offset error change after the system is zeroed, error will be introduced into the measurement. Temperature change is the primary factor in offset error. Lion Precision systems are compensated for temperature related offset errors to keep them less than 0.04%F.S./°C.

Linearity Error

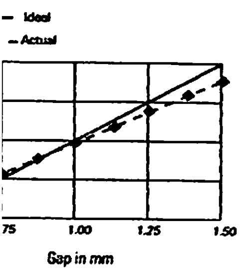
Sensitivity can vary slightly between any two points of data. This variation is called linearity error. The linearity specification is the measurement of how far the output varies from a straight line.

To calculate the linearity error, calibration data is compared to the straight line that would best fit the points. This straight reference line is calculated from the calibration data using a technique called least squares fitting. The amount of error at the point on the calibration line that is furthest away from this ideal line is the linearity error. Linearity error is usually expressed in terms of percent of full scale. If the error at the worst point was 0.001mm and the full scale range of the calibration was 1mm, the linearity error would be 0.1%.

Note that linearity error does not account for errors in sensitivity. It is only a measure of the straightness of the line and not the slope of the line. A system with gross sensitivity errors can be very linear.



The slope of the line is the
ı this case 1V/0.05mm.



ror - The slope of the actual
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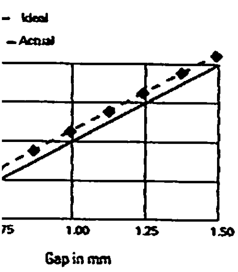

A constant value is added to
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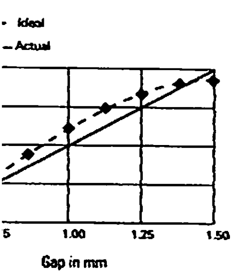


r - Measurement data is not
line.

xpected Value (VDC)	Actual Value (VDC)	Error Band (mm)
10.000	-9.800	-0.010
-5.000	-4.900	-0.005
0.000	0.000	0.000
5.000	5.000	0.000
10.000	10.100	0.005

- the worst case deviation of
d values from the expected
alibration chart. In this case,
r is -0.010mm.

nding outputs maximize
gin when used in servo-
dback systems.

Error Band

Error band accounts for the combination of linearity and sensitivity errors. It is the measurement of the worst case absolute error in the calibrated range. The total error is calculated by comparing the output voltages at specific gaps to their expected value. The worst case error from this comparison is listed as the system's total error.

Bandwidth

Bandwidth is defined as the frequency at which the output falls to -3dB. This frequency is also called the cutoff frequency. A -3dB drop in the signal level equates to approximately 70% drop in actual output voltage. With a 15kHz bandwidth, a change of ±1V at low frequency will only produce a ±0.7V change at 15kHz.

Excitation frequency of the driver electronics is a major factor in determining bandwidth. A meaningful change in output voltage requires several cycles of the changing electric field in the gap. Lion Precision uses an excitation frequency of 1MHz compared to a more typical 10kHz-15kHz. This higher excitation frequency gives Lion Precision a standard bandwidth of 15kHz compared to an industry average of less than 5kHz. Bandwidth is also affected by the geometry of the probe. Bandwidth tends to drop as the probe size decreases.

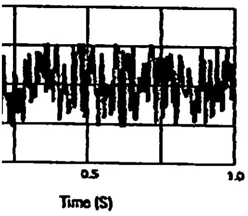
Fast responding outputs maximize phase margin when used in servo-control feedback systems. Some drivers provide selectable bandwidth for maximizing resolution or response time.

Resolution

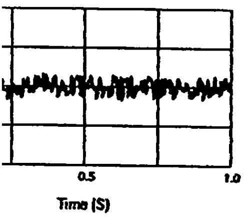
Resolution is defined as the smallest reliable measurement that a system can make. The resolution of a measurement system must be better than the final accuracy the measurement requires. If you need to know a measurement to within 0.02μm, then the resolution of the measurement system must be better than 0.02μm.

The primary determining factor of resolution is electrical noise. Electrical noise appears in the output voltage causing small instantaneous errors in the output. Even when the probe/target gap is perfectly constant, the output voltage of the driver has some small but measurable amount of noise that would seem to indicate that the gap is changing. This noise is inherent in electronic components and can only be minimized, but never eliminated.

If a driver has an output noise of 0.002V with a sensitivity of 10V/1mm, then it has an output noise of 0.000,2mm (0.2μm). This means that at any instant in time, the output could have an error of 0.2μm.



ridth Output Noise - typical
e from a system with 15kHz
The peak to peak noise during
:ond sample period is 0.010V.
tivity of 10V/1mm the peak to
tion is 1.0μm.



red Output Noise - typical
e from a system with 100Hz
The peak to peak noise during
ond sample period is 0.002V.
ivity of 10V/1mm the peak to
tion is 0.2μm; a 500% improve-
he 15kHz resolution.

The amount of noise in the output is directly related to bandwidth. Generally speaking, noise is distributed uniformly over a wide range of frequencies. If the higher frequencies are filtered before the output, the result is less noise and better resolution. When examining resolution specifications it's critical to know at what bandwidth the measurements were taken.

Resolution Calculation

Resolution as indicated in this catalog is calculated by measuring and recording the output noise over a period of one second with a digital oscilloscope sampling at 100kHz. The maximum peak to peak value during this time is defined as the peak to peak resolution. This same sampling of measurements is used to calculate the RMS value for the RMS resolution.

Test methods to determine resolution vary. This makes resolution and noise difficult to compare with numbers only. In applications where these values are critical, we recommend that systems be evaluated in the application. This is the best way to accurately determine whether or not system performance is sufficient.

Super-Compact Composite Right-/Left-Handed Transmission Line with Vertically Stacked Left-Handed Unit Cells

Yasushi Horii
Faculty of Informatics, Kansai University
2-1-1 Ryozenji, Takatsuki, Osaka 569-1095 Japan
E-mail : horii@res.kutc.kansai-u.ac.jp

Christophe Caloz
Ecole Polytechnique de Montreal
Montreal, QB, H3V 1A2, Canada
E-mail : christophe.caloz@polymtl.ca

RACT

r the last decade, left-handed (LH) meta-materials, characterized by anti-parallel phase and group velocities, have considerable interest in the microwave community due to their potential for developing new types of devices and nents. In such a movement of this research, we have proposed a super-compact multi-layered (ML) composite-eft-handed (CRLH) transmission line (TL). This TL consists of U-shaped parallel plate LH unit cells connected to nd enclosure by meander lines. In this architecture, the coupling between stacked U-shapes provides the LH capacitance C_L, and the meander line provides the LH shunt inductance L_L, while the right-handed (RH) series ance L_R and the RH shunt capacitance C_R are generated by the metallic connections in the direction of propagation the voltage gradient from the TL to the ground enclosure, respectively. In contrast to previously reported planar TLs, the multi-layered TL has its direction of propagation along the *vertical* direction, perpendicular to the plane substrates. Therefore, the large electrical length can be achieved over an extremely short TL length and small erse footprint. In addition, it has a specific feature in the transmission parameter S_{21} that the *transmission zero* can ated just above the LH passband, which characteristic is quite useful for the design of narrow passband response. ver, this response could not be explained by the conventional CRLH equivalent circuit model.

his paper, the effect of a capacitive coupling C_P between the meander line and the U-shaped metallizations is introduced to the conventional equivalent circuit, and a new circuit model is developed for the ML CRLH TLs. the C_P is small enough, the behavior of the circuit is almost the same as the conventional CRLH TL. However, by ng the larger C_P, the shunt components of the TL makes a short circuit and consequently the transmission zero is d above the LH passband. In the demonstration with the circuit parameters, C_L=10.0pF, L_{L1}=6.5nH, L_{L2}=3.5nH, 5pF, L_R=1.8nH, and C_P=5.5pF, the LH passband is obtained at the frequency range from 0.25GHz to 0.6GHz and 1 1.05GHz. Also, the transmission zero can be seen around 1.0GHz.

newly estimated result shows good agreement with the experimental demonstration and the full-wave FEM and simulations.

OWLEDGEMENTS

esearch is financially supported by the Kansai University Special Research Fund 2005, "Development of multi-d left-handed meta-materials for microwave and millimeter-wave applications".

NTRODUCTION

composite right/left-handed (CRLH) transmission line (TL) theory, developed by Caloz *et al.* and Eleftheriades *et* -2], has been successfully applied to various kinds of LH structures, and high-performance applications have been uced in the fields of microwave couplers, resonators, antennas and dual-band components. Thus, this TL theory is powerful and useful for planar LH structures based on microstrip lines or coupled mushrooms. However, the entional theory is still insufficient to describe the whole mechanism of newly proposed multi-layered (ML) CRLH [3-5]. A LH unit cell of the ML CRLH TL is composed of U-shaped parallel plates and a meander line sandwiched ose plates. Therefore, a strong coupling between them is occurred just inside the U-shape. In this paper, the effect is coupling is newly introduced to the conventional equivalent circuit, and a new circuit model is developed for the CRLH TLs. The basic behavior of this circuit is studied and the results are compared with the FEM and FDTD full- simulations and experiments.

ULTI-LAYERED CRLH TRANSMISSION LINE

rchitecture and Equivalent circuit

g.1 shows geometry of the ML CRLH TL. The TL is composed of periodically stacked LH unit cells, each of which nstituted by a pair of U-shaped parallel plates (shown by "green" color in the figure) connected to a ground sure by a meander line ("red"). Another two plates ("blue"), placed at the top or the bottom of the stacked U- es, couple to the LH body and give an input and an output ports of this TL.

equivalent circuit model corresponding to this architecture is shown in Fig. 2 (a) and (b). In this architecture, the ling between stacked U-shapes provides the LH series capacitance C_L, and the meander line provides the LH shunt tance L_L. On the other hand, the right-handed (RH) series inductance L_R and the RH shunt capacitance C_R are

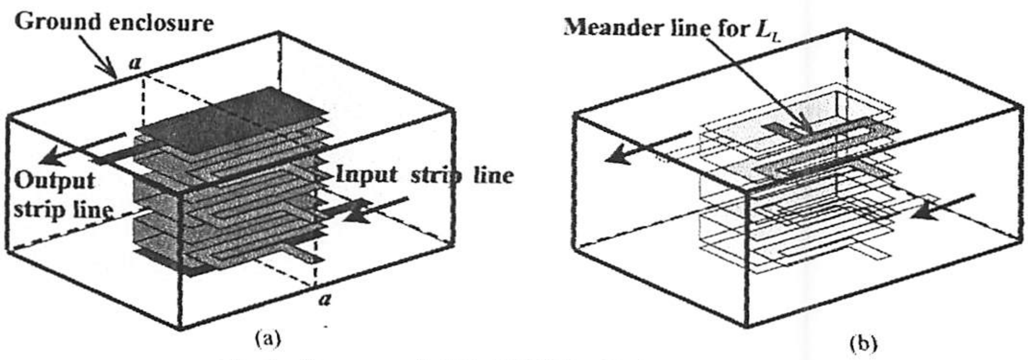


Fig. 1 Geometry of a ML CRLH TL with three LH unit cells.

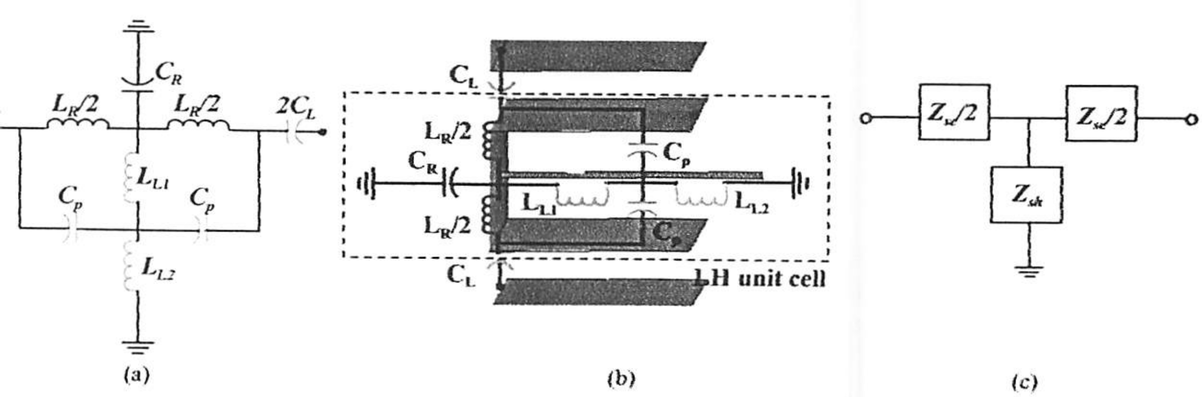


Fig. 2 A new equivalent circuit model for a ML CRLH TL.
(a) Equivalent circuit of a unit cell. (b) Arrangement of circuit elements on a U-shaped geometry, observed at *a-a'* section in Fig.1 (a).
(c) T-type unit cell in a ladder network.

ted by the metallic connections in the direction of ;ation and by the voltage gradient from the TL to the l enclosure, respectively.

:ontrast to previously reported CRLH TLs based on a structure, it should be noted that the ML structure has a coupling between the meander line and the parallel plates :d just inside the U-shape. To express this effect, the LH ınce L_L is divided into two elements, L_{L1} and L_{L2}, and a ıpacitance C_P is introduced as illustrated in Fig.2 (b).

:twork expression shown in Fig.2 (c) is useful to evaluate ıavior of the CRLH TLs in respects of a series and a shunt lances Z_{se} and Z_{sh}. This expression can be derived by ıg $Y-\nabla$ and $\nabla-Y$ transformations several times to ginal equivalent circuit shown in Fig.2 (a).

ıivalent Circuit Analysis

a demonstration of the new equivalent circuit, the ude of the transmission coefficient $|S_{21}|$ and the reflection ient $|S_{11}|$ are calculated for a ML CRLH TL with three LH ells, assuming the circuit parameters as C_L=10.0pF, ;nH, L_{L2}=3.5nH, C_R=0.5pF, L_R=1.8nH, and C_P=5.5pF. Also, ries impedance Z_{se} and the shunt impedance Z_{sh} are ted and these results are shown in Fig.3.

3 (a) clearly indicates that the TL has a passband from łz to 0.6GHz and around 1.05GHz. This response can be ıed in respect of Z_{se} and Z_{sh}, based on the conventional TL theory [1-2]. As the imaginary part of the series ınce $Im(Z_{se})$ is capasitive and the imaginary part of the mpedance $Im(Z_{sh})$ is inductive at these frequency range, can work as a LH TL. While at the frequency range from z to 1.0GHz or above 1.15GHz, since both the $Im(Z_{se})$ and become capacitive or inductive simultaneously, a band yielded and the wave propagation is prohibited.

ther unique feature is that it has a transmissin zero around This is because $Im(Z_{sh})$ becomes zero when it changes apacitive to inductive, leading to make a short circuit n the vertical metallic connections and the ground ıre. This frequency is quite sensitive to the parameters L_{L1} , and it can be shifted to the lower frequency by setting values for them. In the real ML CRLH structure, it can be y placing the U-shaped parallel plates closer to each other iving a higher inductance to L_L using a dense meander line ge-scale spiral coil.

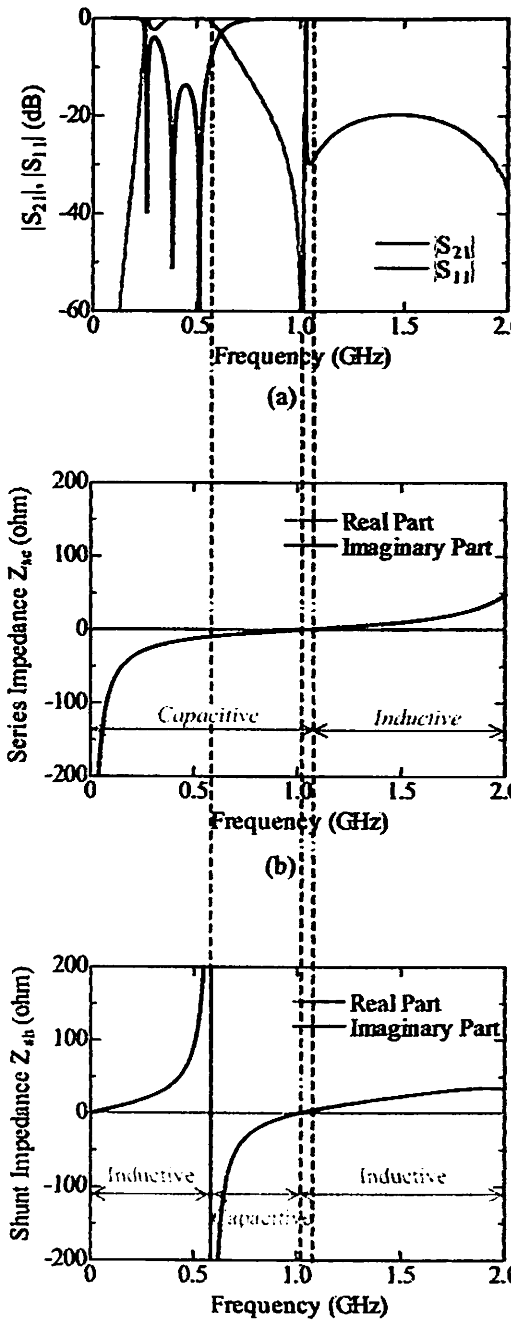


Fig. 3 Frequency response of a ML CRLH TL with three LH unit cells, calculated by an equivalnet circuit model shown in Fig.2. Parameters are C_L=10.0pF, L_{L1}=6.5nH, L_{L2}=3.5nH, C_R=0.5pF, L_R=1.8nH, and C_P=5.5pF.
(a) Scattering characteristics $|S_{21}|$ and $|S_{11}|$.
(b) Reactance of a series impedance Z_{se}.
(c) Reactance of a shunt impedance Z_{se}.

ıeriment

onfirm the theoretical predictions, experiments have been carried out by building a hand-made prototype [5] as in Fig.4. This TL consists of three LH unit cells, and the structure is the same as illustrated in Fig.1. The ired scattering parameters of this TL are presented in Fig.5 in comparison with the FEM (Ansoft HFSS 9) and the) (in-house code) results. Though the experimental result has some errors due to misalignment and air-gaps led in the assembling process of different twelve layers, these results show good agreement with those of FEM DTD as a whole. Fig.6 illustrates the time variation of the 0.4GHz electric field distribution in the TL observed at oss section *a-a'*, calculated by FDTD. A backward wave propagation can be seen clearly in this structure.

'ONCLUSION

ing a strong coupling between the parallel plates and the inductive line of each LH unit cell into consideration, a quivalent circuit specialized for the ML CRLH TL was developed and demonstrated in this paper. This equivalent t has a potential to predict transmission zeros and pulse-like response observed just above the LH passband. The ated result by the circuit analysis showed good agreement with the experimental results and the FEM and FDTD ation results.

ERENCES

Caloz, and T. Itoh, "Application of the transmission line theory of left-handed (LH) materials to the realization of nicrostrip "LH line"," *IEEE-APS Int'l Symp*, vol.2, pp.412-415, San Antonio, TX, June 2002.

V. Eleftheriades, A. K. Iyer, and P. C. Kremer, "Planar negative refractive index media using periodically *L-C* aded transmission lines," *IEEE Trans. Microwave Theory Tech.*, vol.50, No.12, pp.2702-2712, Dec. 2002.

Horii, C. Caloz, and T. Itoh, "Vertical multi-layered implementation of a purely left-handed transmission line for per-compact and dual-band devices," *European Microwave Conference*, pp.471-474, Amsterdam, Oct. 2004.

Horii, C. Caloz, S. M. Han, and T. Itoh, "A Super-Compact Diplexer Composed of Multi-layered Composite ght/Left-handed Transmission Lines," *Asia-Pacific Microwave Conference*, India, Dec. 2004.

Horii, C. Caloz, and T. Itoh, "Super-Compact Multi-Layered Left-Handed Transmission Line and Diplexer oplication," *IEEE Trans. Microwave Theory Tech.*, vol.53, No.4., pp.1527-1534, vol.53, No.4, April 2005.

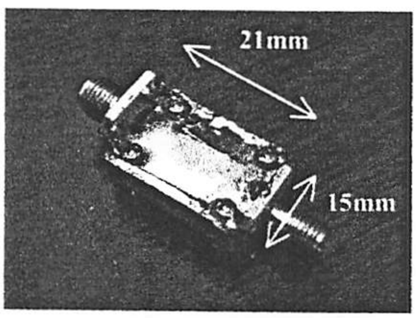
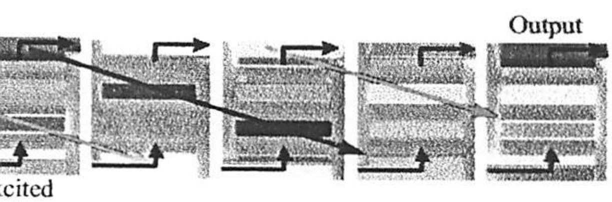


Fig. 4. Prototype of a ML CRLH TL [5].



6. Time variation of the electric field distribution in the ML LH TL, observed at *a-a'* cross section in Fig. 1 (a). Calculation is ied out at 0.4 GHz by FDTD. (a) $t = 0$, (b) $t = 1/4T$, (c) $t = 1/2T$, $= 3/4T$, (e) $t = T$ (period $T = 2.5 \times 10^{-9}$ sec).

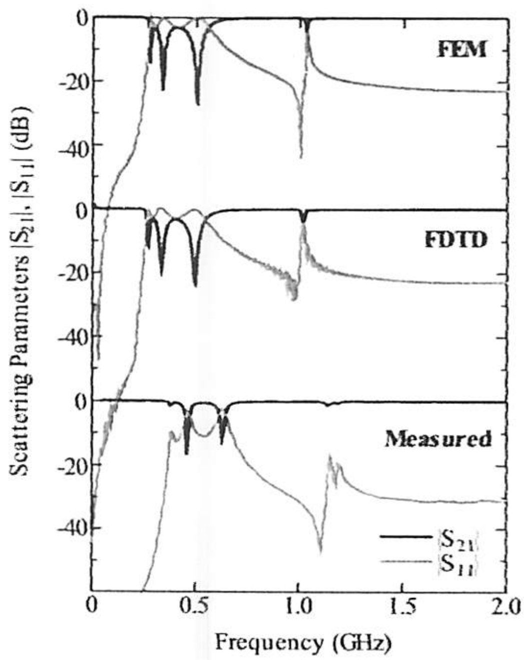
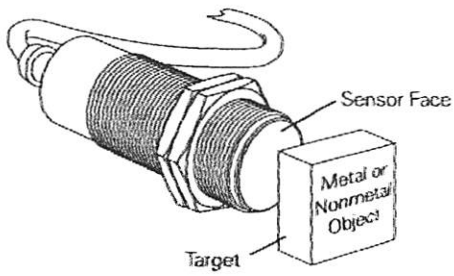


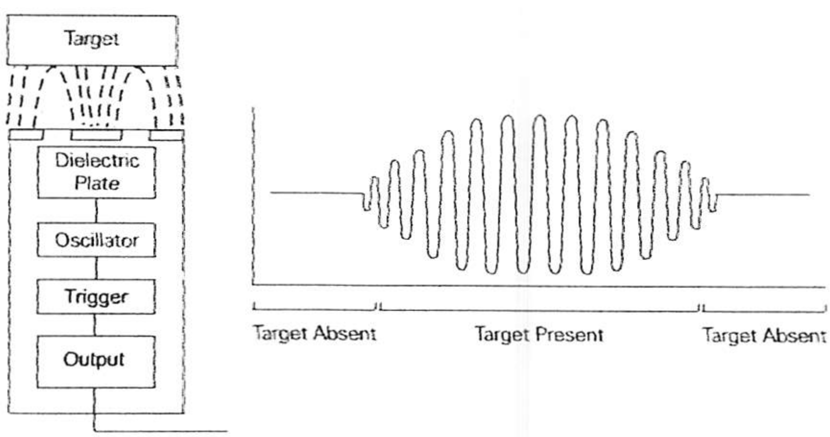
Fig. 5 Scattering characteristics of the ML CRLH TL shown in Fig. 4.

Capacitive Proximity Sensors Theory of Operation

Capacitive proximity sensors are similar to inductive proximity sensors. The main difference between the two types is that capacitive proximity sensors produce an electrostatic field instead of an electromagnetic field. Capacitive proximity switches will sense metal as well as nonmetallic materials such as paper, glass, liquids, and cloth.

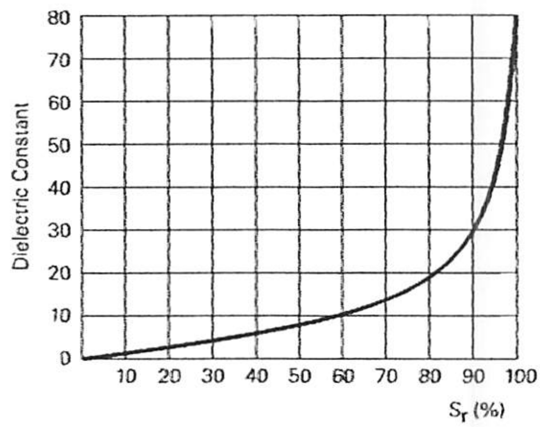


The sensing surface of a capacitive sensor is formed by two concentrically shaped metal electrodes of an unwound capacitor. When an object nears the sensing surface it enters the electrostatic field of the electrodes and changes the capacitance in an oscillator circuit. As a result, the oscillator begins oscillating. The trigger circuit reads the oscillator's amplitude and when it reaches a specific level the output state of the sensor changes. As the target moves away from the sensor the oscillator's amplitude decreases, switching the sensor output back to its original state.



ndard Target and lectric Constant

Standard targets are specified for each capacitive sensor. The standard target is usually defined as metal and/or water. Capacitive sensors depend on the dielectric constant of the target. The larger the dielectric number of a material the easier it is to detect. The following graph shows the relationship of the dielectric constant of a target and the sensor's ability to detect the material based on the rated sensing distance (Sr).

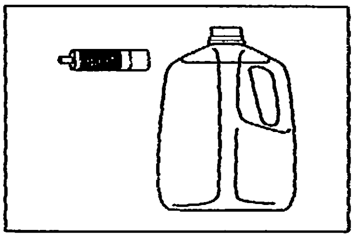


The following table shows the dielectric constants of some materials. If, for example, a capacitive sensor has a rated sensing distance of 10 mm and the target is alcohol, the effective sensing distance (Sr) is approximately 85% of the rated distance, or 8.5 mm.

Material	Dielectric Constant	Material	Dielectric Constant
Alcohol	25.8	Polyamide	5
Araldite	3.6	Polyethylene	2.3
Bakelite	3.6	Polyproplene	2.3
Glass	5	Polystyrene	3
Mica	6	Polyvinyl Chloride	2.9
Hard Rubber	4	Porcelain	4.4
Paper-Based Laminate	4.5	Pressboard	4
Wood	2.7	Silica Glass	3.7
Cable Casting Compound	2.5	Silica Sand	4.5
Air, Vacuum	1	Silicone Rubber	2.8
Marble	8	Teflon	2
Oil-Impregnated Paper	4	Turpentine Oil	2.2
Paper	2.3	Transformer Oil	2.2
Paraffin	2.2	Water	80
Petroleum	2.2	Soft Rubber	2.5
Plexiglas	3.2	Celluloid	3

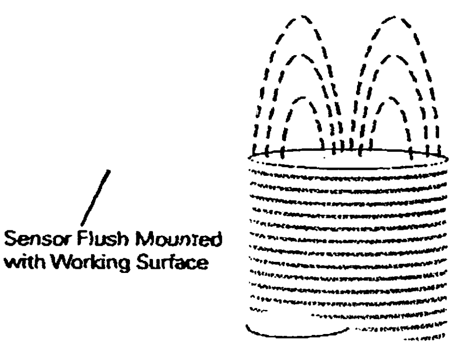
tion Through Barriers

One application for capacitive proximity sensors is level detection through a barrier. For example, water has a much higher dielectric than plastic. This gives the sensor the ability to "see through" the plastic and detect the water.



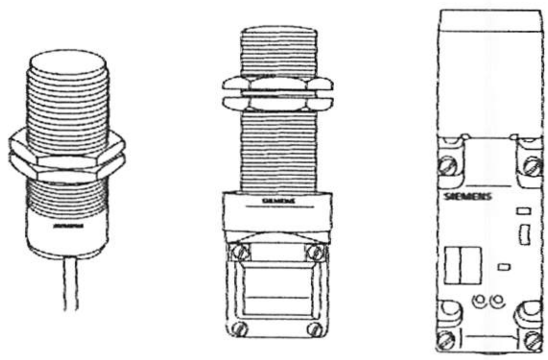
ling

All Siemens capacitive sensors are shielded. These sensors will detect conductive material such as copper, aluminum, or conductive fluids, and nonconductive material such as glass, plastic, cloth, and paper. Shielded sensors can be flush mounted without adversely affecting their sensing characteristics. Care must be taken to ensure that this type of sensor is used in a dry environment. Liquid on the sensing surface could cause the sensor to operate.



Capacitive Proximity Sensor Family

The 3RG16 product family identifies the Siemens capacitive proximity sensor. Units are available in DC or AC versions. Electronic controls such as SIMATIC® PLCs or relays can be controlled directly with the DC voltage version. In the case of the AC voltage version the load (contactor relay, solenoid valve) is connected with the sensor in series directly to the AC voltage. Sensors are available with two-, three-, and four-wire outputs.



acitive Sensor ction Guide

Housing Dimension (mm)	Material	Shielded Unshielded	Sn (mm)	Operating Voltage	Wires
18	Plastic	Shielded	5	10-65 VDC	3
30	Metal	Shielded	10	20-250 VAC	3
	Plastic	Shielded	10	20-250 VAC	2
	Metal	Shielded	10	10-65 VDC	4
	Plastic	Shielded	10	10-65 VDC	4
40	Plastic	Shielded	20	20-250 VAC	2
	Plastic	Shielded	20	10-65 VDC	4
40x40	Plastic	Shielded	20	20-250 VAC	2
(Limit Switch Style)	Plastic	Shielded	20	10-65 VDC	4
20x20 (Flat Pack)	Metal	Shielded	5	10-30 VDC	3

v 4

1) A main difference between an inductive proximity sensor and a capacitive proximity sensor is that a capacitive proximity sensor produces an ___________ field.

2) Capacitive proximity sensors will sense ___________ material.

3) The larger the ___________ constant of a material the easier it is for a capacitive proximity sense to detect.

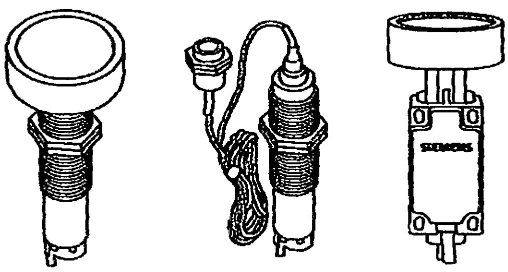
4) It is easier for a capacitive proximity sensor to detect ___________ than porcelain.

a. teflon
b. marble
c. petroleum
d. paper

5) The maximum rated sensing distance of a capacitive proximity sensor is ___________ mm.

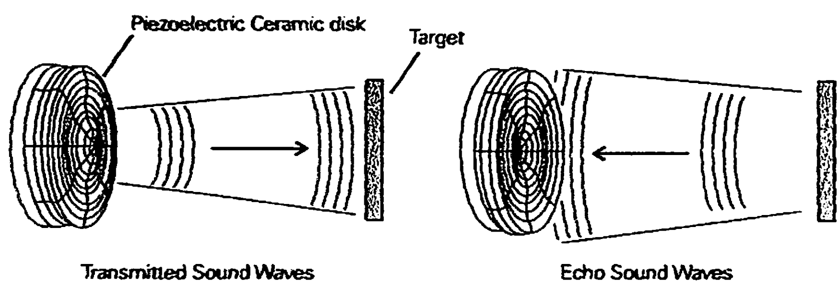
Ultrasonic Proximity Sensors
Theory of Operation

Ultrasonic proximity sensors use a transducer to send and receive high frequency sound signals. When a target enters the beam the sound is reflected back to the switch, causing it to energize or deenergize the output circuit.

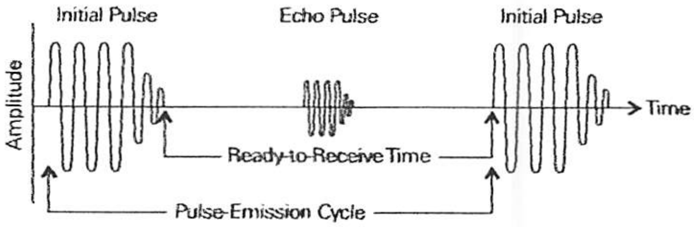


zoelectric Disk

A piezoelectric ceramic disk is mounted in the sensor surface. It can transmit and receive high-frequency pulses. A high-frequency voltage is applied to the disk, causing it to vibrate at the same frequency. The vibrating disk produces high-frequency sound waves. When transmitted pulses strike a sound-reflecting object, echoes are produced. The duration of the reflected pulse is evaluated at the transducer. When the target enters the preset operating range, the output of the switch changes state. When the target leaves the preset operating range, the output returns to its original state.

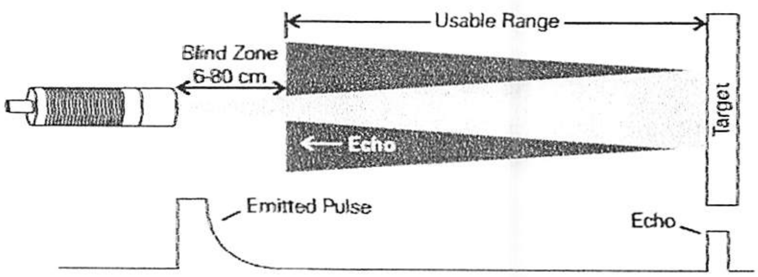


The emitted pulse is actually a set of 30 pulses at an amplitude of 200 Kvolts. The echo can be in microvolts.



Zone

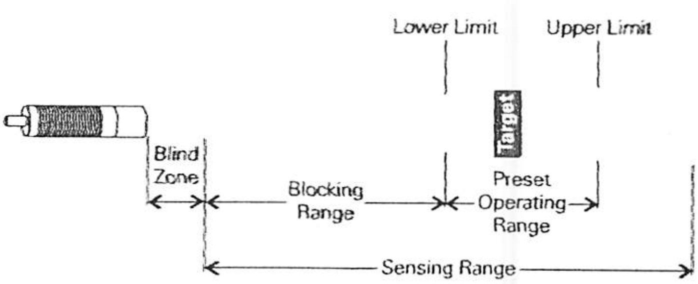
A blind zone exists directly in front of the sensor. Depending on the sensor the blind zone is from 6 to 80 cm. An object placed in the blind zone will produce an unstable output.



Definition

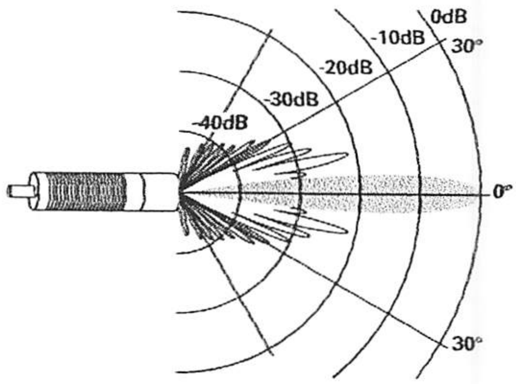
The time interval between the transmitted signal and the echo is directly proportional to the distance between the object and sensor. The operating range can be adjusted in terms of its width and position within the sensing range. The upper limit can be adjusted on all sensors. The lower limit can be adjusted only with certain versions. Objects beyond the upper limit do not produce a change at the output of the sensor. This is known as "blanking out the background".

On some sensors, a blocking range also exists. This is between the lower limit and the blind zone. An object in the blocking range prevents identification of a target in the operating range. There is a signal output assigned to both the operating range and the output range.



liation Pattern

The radiation pattern of an ultrasonic sensor consists of a main cone and several neighboring cones. The approximate angle of the main cone is 5°.

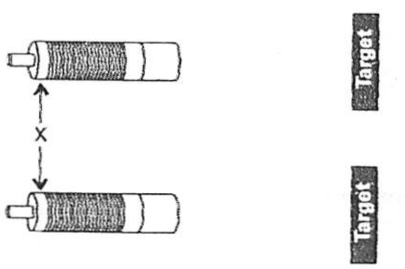


e Zones

Free zones must be maintained around the sensor to allow for neighboring cones. The following examples show the free area required for different situations.

llel Sensors

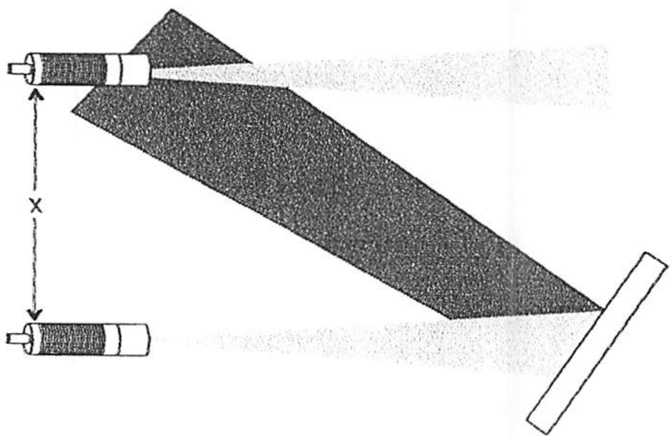
In the first example, two sonar sensors with the same sensing range have been mounted parallel to each other. The targets are vertical to the sound cone. The distance between the sensors is determined by the sensing range. For example, if the sensing range of the sensors is 6 cm, they must be located at least 15 cm apart.



Sensing Range (CM)	X (CM)
6-30	>15
20-130	>60
40-300	>150
60-600	>250
80-1000	>350

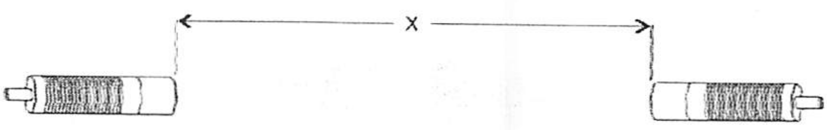
al Interference

Mutual interference occurs when sonar devices are mounted in close proximity to each other and the target is in a position to reflect echoes back to a sensor in the proximity of the transmitting sensor. In this case, the distance between sensors (X) can be determined through experimentation.



sing Sensors

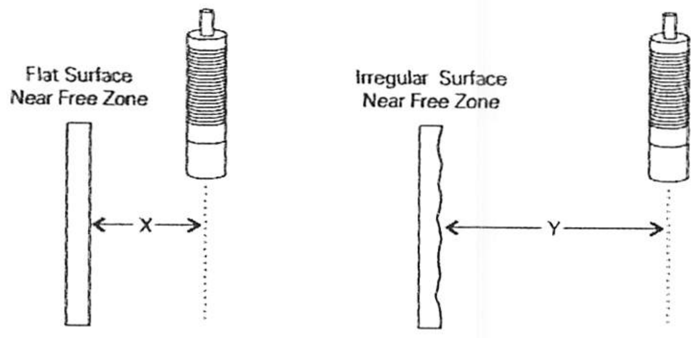
In the following example, two sonar sensors with the same sensing range have been positioned opposite of each other. A minimum distance (X) is required between opposing sensors so that mutual interferance does not occur.



Sensing Range (CM)	X (CM)
6-30	>120
20-130	>400
40-300	>1200
60-600	>2500
80-1000	>4000

t and Irregular ped Surfaces

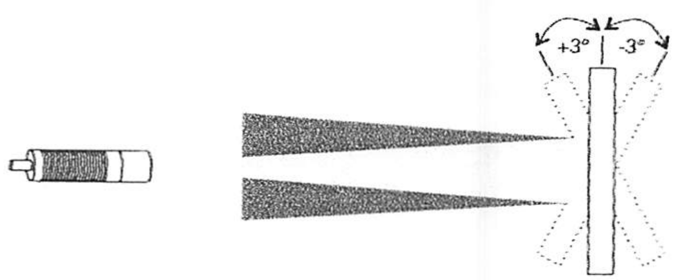
Sonar sensors mounted next to a flat surface, such as a wall or smooth machine face, require less free area than sensors mounted next to an irregular shaped surface.



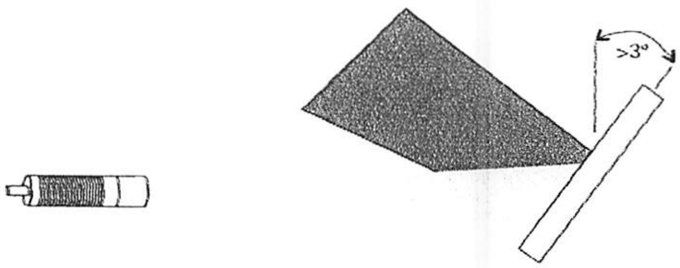
Sensing Range (CM)	X (CM)	Y (CM)
6-130	>3	>6
20-130	>15	>30
40-300	>30	>60
60-600	>40	>80
80-1000	>70	>150

ular Alignment

The angle of the target entering the sound cone must also be considered. The maximum deviation from the send direction to a flat surface is ±3°.

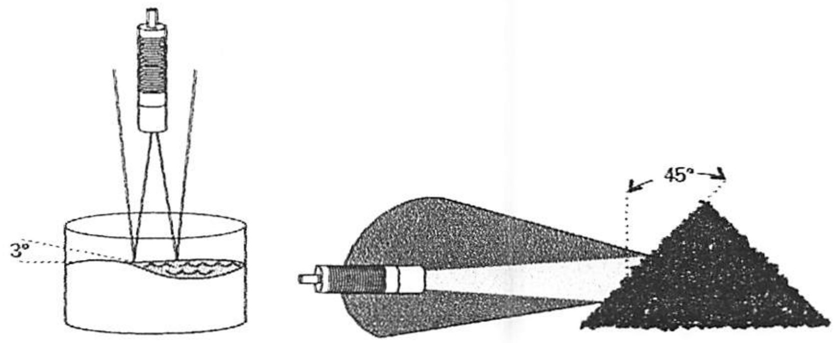


If the angle were greater than 3° the sonic pulses would be reflected away and the sensor would not receive an echo.



ds and e-Grained Materials

Liquids, such as water, are also limited to an angular alignment of 3°. Coarse-grained materials, such as sand, can have an angular deviation as much as 45°. This is because the sound is reflected over a larger angle by coarse-grained materials.

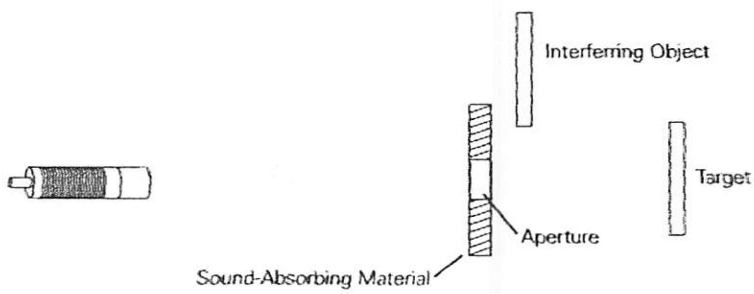


Liquid

Coarse-Grained Material

ing Out Objects

An object may be located in the vicinity of the sound cone that causes improper operating of the sensor. These objects can be blanked out by using an aperture made of a sound absorbing material such as rock wool. This narrows the sound cone and prevents pulses from reaching the interfering object.

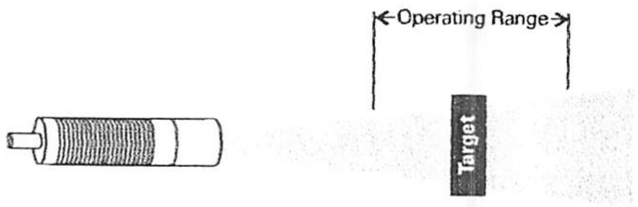


erating Modes

Sonar sensors can be setup to operate in several different modes: diffuse, reflex, and thru-beam.

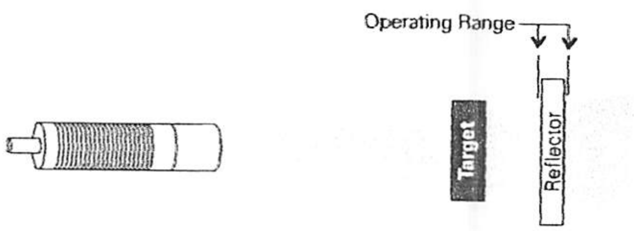
fuse Mode

This is the standard mode of operation. Objects, traveling in any direction into the operating range of the sound cone, will cause the sensor output to switch states. This mode of operation is similar to a proximity sensor.



lex Mode

The reflex mode uses a reflector located in the preset operating range. The operating range is adjusted for the reflector. The pulses are bounced off the reflector and the echo pulses are returned to the sensor. When a target blocks the echo pulses the output is activated. Typically used in applications where the target is not a good sound absorber.



u-Beam Mode

Thru-beam sensors consist of a transmitter, which emits ultrasonic pulses, and a receiver. If the beam between the transmitter and the receiver is interrupted the output of the receiver switches state.

nmental Influences

Sound travel time can be affected by physical properties of the air. This, in turn, can affect the preset operating distance of the sensor.

Condition	Effect
Temperature	Sonic wave speed changes by 0.17%/°K. Most sensors have a compensation adjustment.
Pressure	With normal atmospheric variation of ±5%, sound velocity varies approximately ±0.6%. Sound velocity decreases 3.6% between sea level and 3 km above sea level. Adjust sensor for appropriate operating range.
Vacuum	Sensors will not operate in a vacuum.
Humidity	Sound velocity increases as humidity increases. This leads to the impression of a shorter distance to the target. The increase of velocity from dry to moisture-saturated air is up to 2%.
Air Currents	Wind Speed <50 km/h - No Effect 50 - 100 km/h - Unpredictable Results >100 km/h - No Echo Received by Sensor
Gas	Sensors are designed for operation in normal atmospheric conditions. If sensors are operated in other types of atmospheres, such as carbon dioxide, measuring errors will occur.
Precipitation	Rain or snow of normal density does not impair the operation of a sensor. The transducer surface should be kept dry.
Paint Mist	Paint mist in the air will have no effect, however, paint mist should not be allowed to settle on transducer surface.
Dust	Dusty environments can lower sensing range 25-33%.

1) Ultrasonic proximity sensors use high frequency ____________ signals to detect the presence of a target.

2) The blind zone of an ultrasonic proximity sensor can be from ____________ - ____________ cm, depending on the sensor.

3) The approximate angle of the main sound cone of an ultrasonic proximity sensor is ____________ degrees.

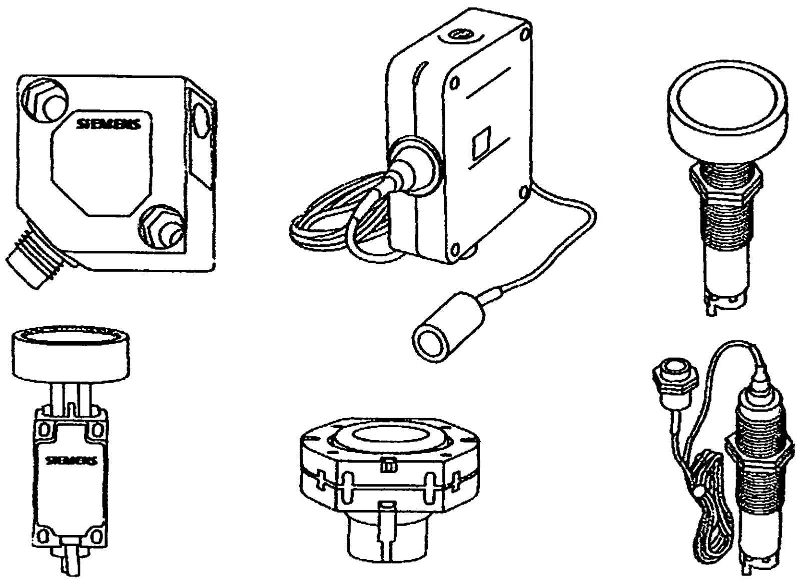
4) The free zone between two parallel ultrasonic sensors with a rated sensing range of 20-130 cm must be greater than ____________ cm.

5) The maximum angle of deviation from the send direction of an ultrasonic sensor to a flat surface is ____________ degrees.

6) ____________ mode is the standard mode of operation for an ultrasonic sensor.

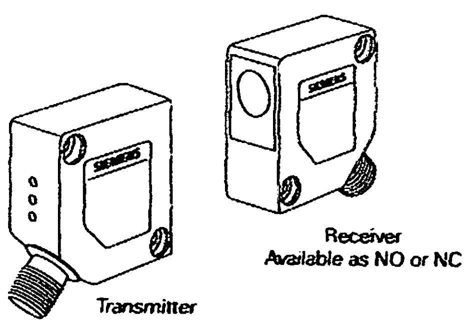
Ultrasonic Proximity Sensor Family

The ultrasonic proximity sensor family consists of a Thru-Beam sensor, compact range (M18, Compact Range 0, I, II, and III), and modular (Modular Range II) sensors.



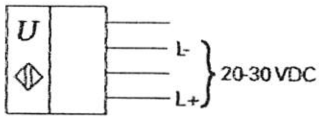
əam

Thru-Beam sensors consist of a transmitter and a receiver. The transmitter sends a narrow continuous tone. When a target is positioned between the transmitter and the receiver the tone is interrupted, which causes the output of the receiver to change state. The operating voltage is 20-30 VDC. The switching frequency is 200 Hz at 40 cm sensing distance.

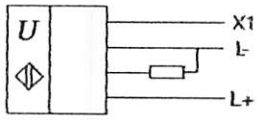


ru-Beam Receivers

There are two receivers available for the Thru-Beam sensors. Both use a PNP transistor. One receiver provides a normally open (NO) contact and the other provides a normally closed (NC) contact.



Transmitter



Receiver
1 NO Contact or 1 NC Contact

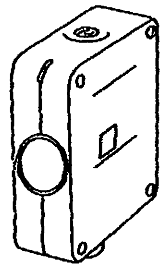
The sensitivity and frequency setting of the Thru-Beam sensors is a function of the X1 connection on the receiver.

Receiver	Distance (cm)	Switching Frequency (Hz)
X1 Open	5-150	100
X1 to L-	5-80	150
X1 to L+	5-40	200

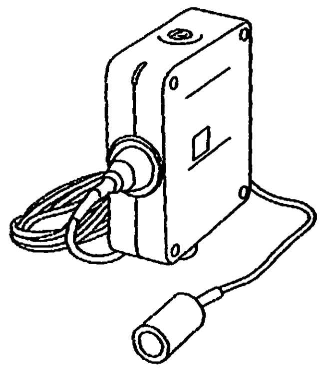
The minimum size of a detectable object is a function of the distance between the transmitter and the receiver. If the distance between the transmitter and the receiver is less than 40 cm and the minimum gap width between two objects is at least 3 cm, objects of 2 cm or larger will be detected. If the distance between the sensors is less, even gaps of less than 1 mm can be detected. At maximum sensing distance, objects greater than 4 cm will be detected, provided the gap between objects is greater than 1 cm.

act Range 0

Compact Range 0 sensors are available with an integrated or an separate transducer. They are configured with a normally open (NO), normally closed (NC) or analog output. These sensors have a cubic shape (88 x 65 x 30 mm). The sensors operate on 18 - 35 VDC and can handle a load up to 100 mA.

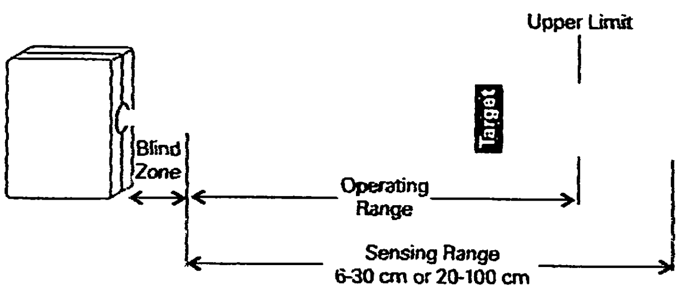


Integrated Transducer



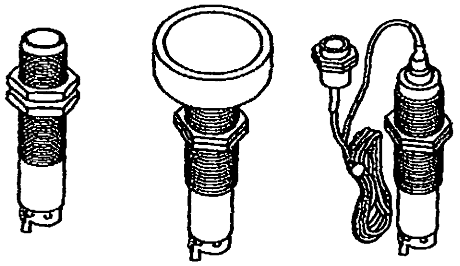
Separate Transducer

Depending on the sensor, the sensing range is either 6 - 30 cm (separate transducer) or 20 - 100 cm (integrated transducer). Switching frequencies vary from 5 Hz to 8 Hz. Compact Range 0 sensors have background suppression. This means the upper limit of the sensing range is adjustable with a potentiometer. Targets within the sensing range but beyond the switching range of the upper limit will not be detected.

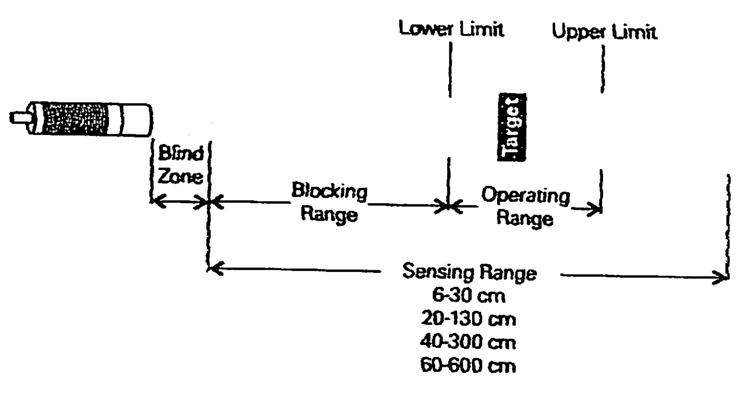


npact Range I

Compact Range I sensors are available with a normally open (NO) or a normally closed (NC) contact. They are also available with two outputs, one normally open (NO) and one normally closed (NC). These sensors have a cylindrical shape (M30 x 150 mm). Several versions are available, including a separate transducer (shown) and a tilting head (not shown). The sensors operate on 20 - 30 VDC and can handle a load up to 200 mA.



Depending on the sensor the sensing range is either 6 - 30 cm, 20 - 130 cm, 40 - 300 cm, or 60 - 600 cm. Switching frequencies vary from 1 Hz to 8 Hz. Compact Range I sensors have background and foreground suppression. This means the upper and lower limits of the sensing range are adjustable with separate potentiometer. Targets within the sensing range but beyond the switching range of the upper and lower limits will not be detected.



PROG

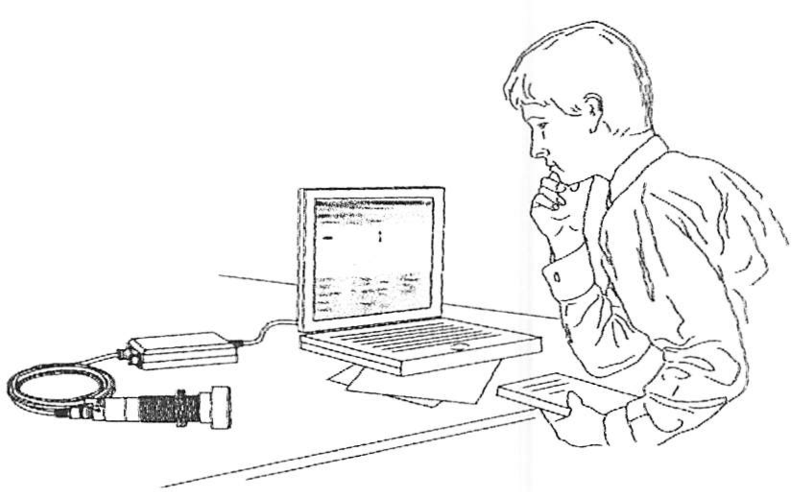
The ultrasonic sensors discussed so far (Thru-Beam, Compact Range 0, and Compact Range I) are either nonadjustable or can be adjusted manually with potentiometers. SONPROG is a computer program, unique to Siemens, that is used to adjust Compact Range II, Compact Range III, and Compact Range M18 sensors.

Sensor	Adjustment
Thru-Beam	None
Compact Range 0	1 Potentiometer
Compact Range I	2 Potentiometers
Compact Range II	SONPROG
Compact Range III	SONPROG
Compact Range M18	SONPROG

With SONPROG sonar sensors can be matched individually to the requirements of a particular application. An interface is connected between the sensor and an RS232 port of a computer. SONPROG can be used to set the following parameters:

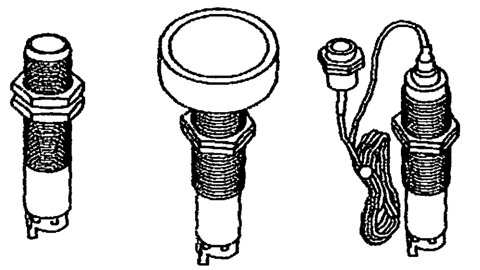
- Beginning and end of switching range
- Switching hysteresis
- Beginning and end of analog characteristic
- End of blind zone
- End of sensing range
- NO/NC contacts
- Potentiometer adjustments on sensors on/off

These values can be printed out and stored in a file. They are immediately available when needed. When replacing a sensor, for example, the stored parameters can be easily applied to the new sensor.

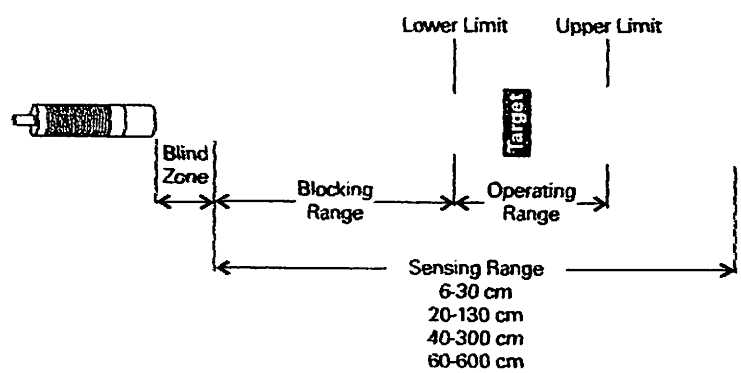


npact Range II

Compact Range II sensors are similar in appearance to Compact Range I sensors. A major difference is that Compact Range II sensors can be adjusted manually or with SONPROG. They are available with a normally open (NO) or a normally closed (NC) contact. They are also available with two outputs, one normally open (NO) and one normally closed (NC). These sensors have a cylindrical shape (M30 x 150 mm). Several versions are available, including a separate transducer. The sensors operate on 20 - 30 VDC and can handle a load up to 300 mA. Compact Range II sensors can be synchronized to prevent mutual interference when using multiple sensors in close proximity to each other.

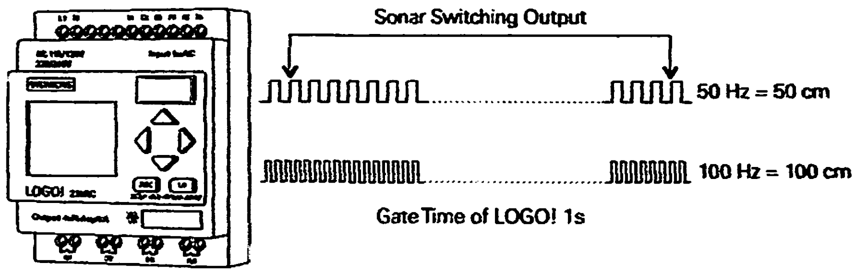


Depending on the sensor the sensing range is either 6 - 30 cm, 20 - 130 cm, 40 - 300 cm, or 60 - 600 cm. Switching frequencies vary from 1 Hz to 8 Hz. Compact Range II sensors have background and foreground suppression.



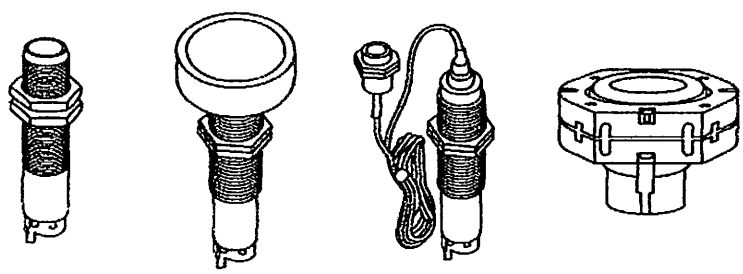
ɔact Range II og Version

An analog version of the Compact Range II sensor is available. The analog measurement is converted by the sensor to digital pulses. A counter in LOGO! or a PLC counts the pulses and makes the measurement conversion. If, for example, the switching output of the sensor were set such that 50 Hz was equivalent to 50 cm and the gate time of LOGO! was set for 1 second, LOGO! would be able to accurately convert any frequency to its corresponding distance.

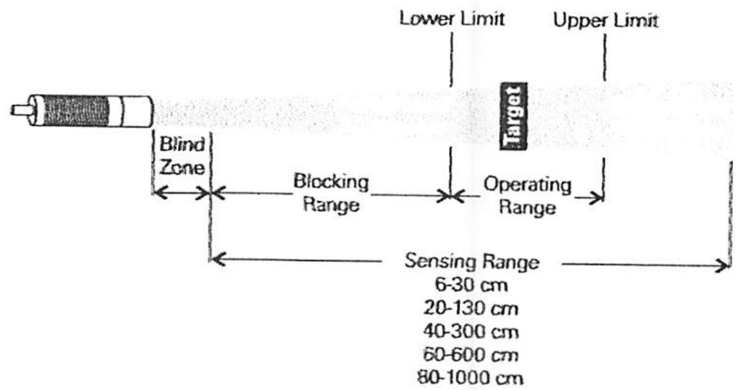


ɔact Range III

Like the Compact Range II sensors, Compact Range III sensors can be adjusted manually or with SONPROG. They are available with a normally open (NO) or a normally closed (NC) contact. They are also available with two analog outputs, 0 - 20 mA or 0 - 10 VDC. The sensors operate on 20 - 30 VDC and can handle a load up to 300 mA. Compact Range III sensors can be synchronized to prevent mutual interference when using multiple sensors in close proximity to each other. In addition, they offer an arithmetic mean feature. This is useful for liquid level sensing or other applications where reflection variations can occur. The arithmetic mean feature helps compensate for these variations.

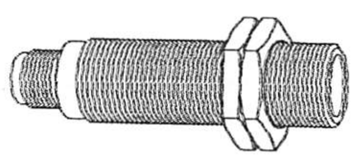


Depending on the sensor, the sensing range is either 6 - 30 cm, 20 - 130 cm, 40 - 300 cm, 60 - 600 cm, or 80 - 1000 cm. Switching frequencies vary from 0.5 Hz to 5 Hz. Compact Range III sensors have background and foreground suppression.

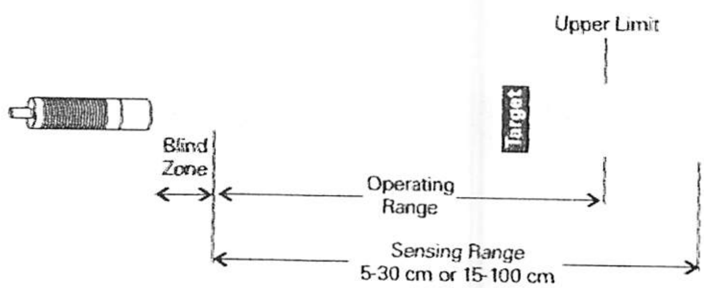


mpact Range M18

The small size (M18 x 101 mm) of the Compact Range M18 sensor makes it suited for applications where space is limited. Compact Range M18 sensors are available with a normally open (NO) or a normally closed (NC) contact. They are also available with an analog output (4 - 20 mA, 0 - 20 mA, or 0 - 10 VDC). The sensors operate on 20 - 30 VDC and can handle a load up to 100 mA.

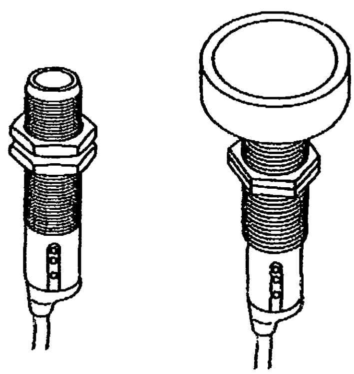


Depending on the sensor the sensing range is either 5 - 30 cm or 15 - 100 cm and the switching frequency is either 4 or 5 Hz. Compact Range M18 sensors have background suppression.



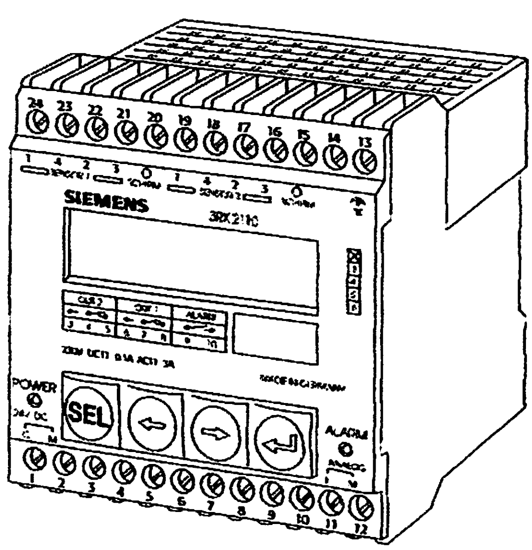
act Range with
e with AS-i

Siemens also manufactures ultrasonic sensors for use with AS-i. Four sensing ranges are available: 6 - 30 cm, 20 - 130 cm, 40 - 300 cm, and 60 - 600 cm. The switching frequency varies from 1 to 8 Hz.

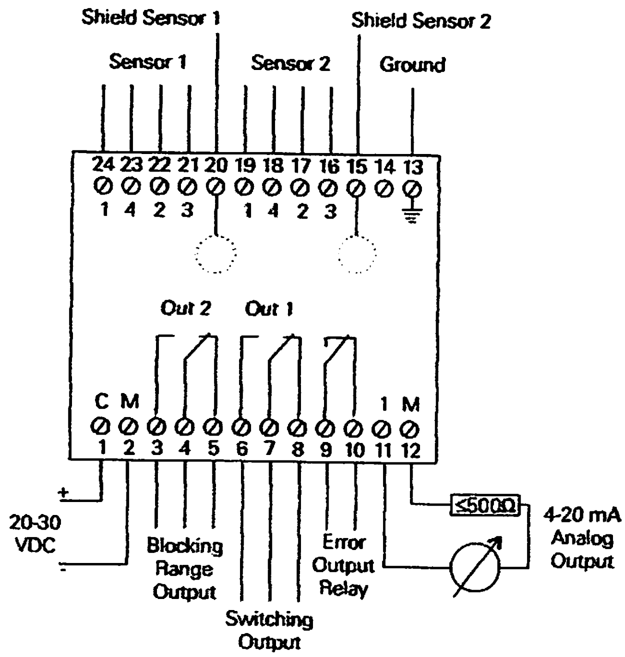


ar Range II
e Signal Evaluator

The next group of ultrasonic sensors is Modular Range II. The Modular Range II consists of sensors and their corresponding signal evaluator. The signal evaluator is required for Modular Range II sensors. Sensor values are set using buttons on the evaluator. A two-line LCD displays the set values.

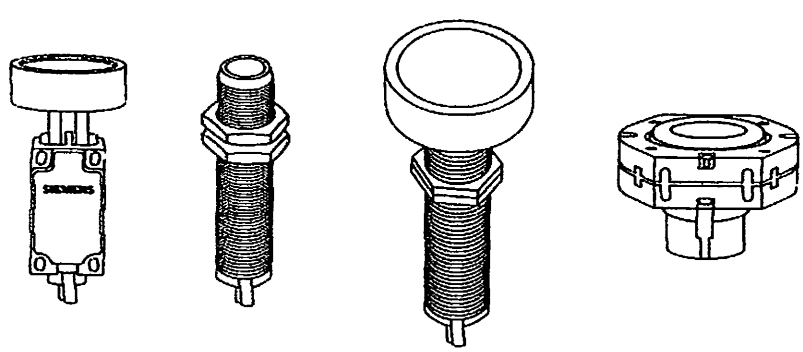


The signal evaluator can operate a maximum of two Modular Range II sensors. It is supplied with a 20 - 30 VDC power supply. It has two switching outputs, one error output, and one analog output.



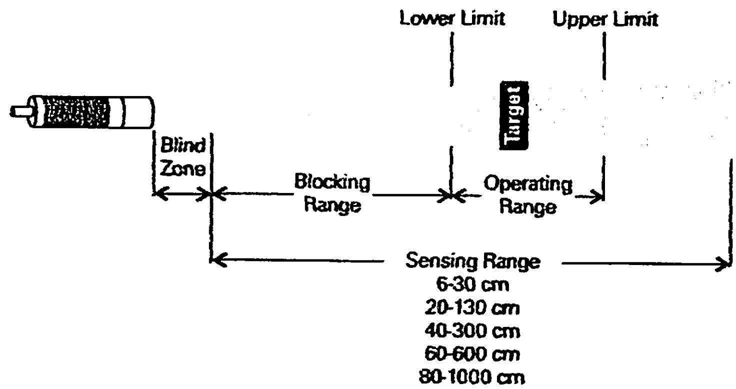
dular Range II Sensors

Module Range II sensors are available in three versions: cubic sensors, cylindrical sensors, and spherical sensors. They have analog and normally open (NO) or normally closed (NC) outputs. As mentioned earlier, all settings and operations are done with a signal evaluator.



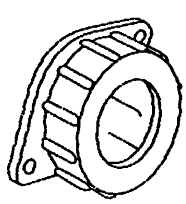
Cubic Sensors   Cylindrical Sensors   Spherical Sensors

Depending on the sensor the sensing range is either 6 - 30 cm, 20 - 130 cm, 40 - 300 cm, 60 - 600 cm, or 80 - 1000 cm. Switching frequencies vary from 1 Hz to 20 Hz. Modular Range II sensors have background and foreground suppression.

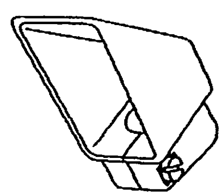


ssories

An adjusting device with a mounting flange (shown) or bracket (not shown) and a 90° diverting reflector are available for M30 spherical sensors. The adjusting device allows the sensor to be positioned in hard-to-mount areas.



Adjusting Device
Flange Model



90° Diverting Reflector

1) Ultrasonic ___________-___________ proximity sensors require a separate transmitter and receiver.

2) If X1 is connected to L+ of a Thru-Beam ultrasonic proximity sensor, the sensing range is ___________ to ___________ cm.

3) The maximum sensing range of a Compact Range 0 ultrasonic sensor with a ___________ transducer is 6 - 30 cm.

4) Compact Range ___________ does not offer foreground suppression.

a. 0
b. I
c. II
d. III

5) ___________ is a computer program used to adjust Compact Range II, Compact Range III, and Compact Range M18 ultrasonic sensors.

6) ___________ Range II require a signal evaluator.

7) A signal evaluator can operate a maximum of ___________ sensors.

a. 1
b. 2
c. 3
d. 4