SKRIPSI

PERANCANGAN DAN PEMBUATAN ALAT PENDETEKSI WARNA BAGI PENDERITA TUNA NETRA DAN BUTA WARNA DENGAN OUTPUT SUARA

Disusun Oleh:

RENDY PRASETIA ONE

NIM : 04.12.255

KONSENTRASI TEKNIK ELEKTRONIKA

JURUSAN TEKNIK ELEKTRO S-1

FAKULTAS TEKNOLOGI INDUSTRI

INSTITUT TEKNOLOGI NASIONAL MALANG

2009

LEMBAR PERSETUJUAN

PERANCANGAN DAN PEMBUATAN ALAT PENDETEKSI WARNA BAGI PENDERITA TUNA NETRA DAN BUTA WARNA DENGAN OUTPUT SUARA

SKRIPSI

Disusun dan Diajukan Sebagai Salah Satu Syarat Untuk Memperoleh Gelar Sarjana Teknik Elektronika Strata Satu (S-1)

Disusun Oleh :

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FAKULTAS TEKNOLOGI INDUSTRI
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INSTITUT TEKNOLOGI NASIONAL
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Judul Skripsi	: Perancangan Dan Pembuatan Alat Pendeteksi Warna Bagi Penderita Tuna Netra dan Buta Warna Dengan Output Suara

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ABSTRAK

PERANCANGAN DAN PEMBUATAN ALAT PENDETEKSI WARNA BAGI PENDERITA TUNA NETRA DAN BUTA WARNA DENGAN OUTPUT SUARA

Rendy Pasetia One, 04.12.255, Teknik Elektro S.1/Elektronika)
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Perkembangan ilmu pengetahuan dan teknologi dewasa ini sangatlah cepat, yang mana melingkupi berbagai sisi kehidupan manusia. Dalam meningkatkan sumber daya manusia (SDM) pada negara berkembang pada umumnya, dan khususnya untuk meningkatkan SDM pada orang tuna netra dan buta warna. Untuk meningkatkan SDM pada penderita tuna netra dan buta warna maka dilakukan pembuatan suatu alat yang bisa mendeteksi warna benda, dengan output suara, agar penderita tuna netra dan buta warna dapat mengenali warna yang ada di sekitarnya.

Untuk membantu dalam pembuatan dan perancangan alat ini, maka dibutuhkan referensi-referensi yang berhubungan dengan perencanaan alat yang akan dibuat. Setelah referensi-referensi terkumpul, maka dilakukan penelitian dan percobaan mengenai objek yang berhubungan dengan perencanaan alat yang akan di buat, dari hasil percobaan dapat diambil suatu kesimpulan dari alat.

Alat bantu identifikasi warna ini dapat bekerja pada warna merah, kuning, hijau, biru, coklat, hitam dan putih. Dari hasil pengujian sensor, dari 20 Jenis benda yang telah di uji, untuk setiap warna, masih terdapat dalam range frekuensi. Dengan terciptanya alat pendeteksi warna ini, diharapkan dapat membantu penderita tuna netra dan buta warna untuk dapat mengenali warna benda secara mandiri.

Kata kunci: sensor warna, IC suara ISD 1420

KATA PENGANTAR

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Keberhasilan penyelesaian laporan skripsi ini tidak lepas dari dukungan dan bantuan berbagai pihak. Untuk itu penyusun menyampaikan terimakasih kepada:

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Penyusun telah berusaha semaksimal mungkin dan menyadari sepenuhnya akan keterbatasan pengetahuan dalam menyelesaikan laporan ini, untuk itu penyusun mengharapkan saran dan kritik yang membangun dari pembaca demi kesempurnaan laporan ini.

Harapan penyusun semoga laporan ini memberikan manfaat bagi perkembangan ilmu pengetahuan bagi pembaca.

Malang, Septembetr 2009

Penulis

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BAB I
PENDAHULUAN

1.1 Latar Belakang

Perkembangan ilmu pengetahuan dan teknologi dewasa ini sangatlah cepat, yang mana melingkupi berbagai sisi kehidpan manusia. Salah satu kemajuannya adalah di bidang teknologi yaitu dengan terciptanya sebuah sensor yang dapat mengenali warna. Kemajuan tersebut tidak terlepas dari tuntutan manusia yang selalu ingin hidup lebih praktis dan efisien dalam kehidupan sehari-harinya.

Dalam meningkatkan sumber daya manusia (SDM) pada negara berkembang pada umumnya, dan khususnya untuk meningkatkan SDM pada orang tuna netra dan buta warna. Untuk meningkatkan SDM pada penderita tuna netra dan buta warna perlu adanya pembuatan suatu alat yang bisa membantu untuk meningkatkan pengetahuan mereka akan warna. Dimana dalam kehidupan sehari-hari sangat di perlukan pengetahuan tentang warna suatu benda agar dapat diterapkan dalam kehidupan bermasyarakat.

Dengan adanya kasus tersebut maka sangat diperlukan adanya pembuatan suatu alat pendeteksi warna yang bisa gunakan untuk penderita tuna netra dan buta warna, agar bisa mengetahui warna suatu benda tanpa harus menunggu bantuan dari orang lain, sehingga, mereka bisa lebih cepat untuk mengetahui warna barang atau benda di sekitar mereka. Untuk memudahkan dalam mengenali tentang warna khususnya pada penderita tuna netra dan buta warna tersebut maka dibuat suatu alat pendeteksi warna, dengan output suara, yang menggunakan sebuah sensor warna TCS230, IC suara ISD 1420, IC 555

sebagai sumber clock eksternal dan MCU AT89S8253 sebagai pengendalinya. Pembuatan alat ini merupakan pengembangan dari skripsi terdahulu, yang mana hanya dapat mendeteksi warna dari kertas. Pengembangan dari alat ini adalah agar dapat digunakan bukan hanya untuk mengenali warna kertas saja melainkan juga benda-benda lain yang ada di sekitar kita. Dengan adanya teknologi tersebut, diharapkan dapat membantu mereka untuk dapat lebih mudah dalam mengenali suatu warna benda.

1.2 Rumusan Masalah

Mengacu pada permasalahan yang di uraikan pada latar belakang, maka rumusan masalah dapat ditekankan pada:

1. Bagaimana membuat alat Identifikasi warna dengan sensor TCS230 menggunakan mikrokontroller dan ISD.
2. Bagaimana cara menampilkan komposisi R G B warna, dari sebuah warna yang di deteksi.
3. Bagaimana agar mikrokontroller dapat dapat mengolah data R G B dari sensor, dan memberikan outputan warna sesuai data dari sensor, yang dikeluarkan melalui ISD.

1.3 Batasan Masalah

Batasan masalah pada penelitian ini adalah sebagai berikut:

1. Suara yang dihasilkan adalah bahasa Indonesia.
2. Pendeteksian warna hanya pada benda bertekstur rata ,tidak transparan,
3. Tidak membahas amplifier yang digunakan.
4. Tidak membahas catu daya.

1.4 Tujuan

Tujuan yang ingin dicapai dalam penyusunan skripsi ini adalah merancang dan membuat alat pendeteksi warna bagi penderita tunanetra dan buta warna, dengan output suara, agar penderita tunanetra dan buta warna dapat mengetahui warna warna benda yang ada di sekitarnya.

1.5 Metodologi

Metodologi yang dipakai dalam pembuatan skripsi ini adalah :

1. Studi literatur

   Mencari referensi – referensi yang berhubungan dengan perencanaan dan pembuatan alat yang akan dibuat.

2. Penulisan

   Melakukan penelitian dan penulisan langsung serta melakukan percobaan secara berulang - ulang mengenai objek yang berhubungan langsung dengan perencanaan alat yang akan dibuat.

3. Pembuatan

   Mengolah dan membuat analisa serta menarik kesimpulan dari hasil pengujian yang ada.

4. Pengujian

   Melakukan pengujian alat setelah pembuatan dan analisa selesai.

1.6 Sistematika penulisan

Sistematika yang digunakan dalam penyusunan skripsi ini adalah sebagai berikut.:

BAB I : Pendahuluan

Menjelaskan latar belakang permasalahan, rumusan masalah, tujuan, pembatasan masalah dan sistematika pembahasan skripsi.

BAB II : Teori Penunjang

Menjelaskan tentang teori-teori dasar penunjang perancangan dan pembuatan alat.

BAB III : Perencanaan Sistem

Pada bab ini dibahas tentang perencanaan dan pembuatan keseluruhan sistem perangkat keras (hardware) dan perangkat lunak (software).

BAB IV : Pengujian Alat

Menjelaskan pengujian alat dan analisis terhadap data hasil pengujian menggunakan teori yang ada.

BAB V : Kesimpulan dan Saran

Menjelaskan kesimpulan dari perancangan dan pembuatan alat serta menjelaskan tentang saran-saran untuk kesempurnaan dalam pembuatan alat ini.

BAB II

TEORI PENUNJANG

Untuk memudahkan dalam memahami sistem ini, maka diperlukan suatu teori-teori yang menunjang dan dapat menjelaskan tentang karakteristik dari komponen- komponen yang digunakan, sehingga dapat memperkirakan cara kerja dari seluruh komponen. Sehingga dapat menambah pengetahuan yang mendukung perencanaan dan pembuatan alat, yang meliputi teori tentang warna, mikrokontroller AT89S8253, Sensor Warna TCS 230, ISD 1420 IC 555, switch danLCD 2x16.

2.1 Teori Warna

Warna adalah speKtrum tertentu yang terdapat dalam suatu cahaya sempurna (cahaya putih). Identitas suatu warna ditentukan oleh panjang gelombang dari warna itu sendiri. Panjang gelombang yang masih bisa di tangkap oleh mata manusia berkisar antara 400-780 nanometer. Mata normal manusia bisa menerima panjang gelombang dari 400-700.

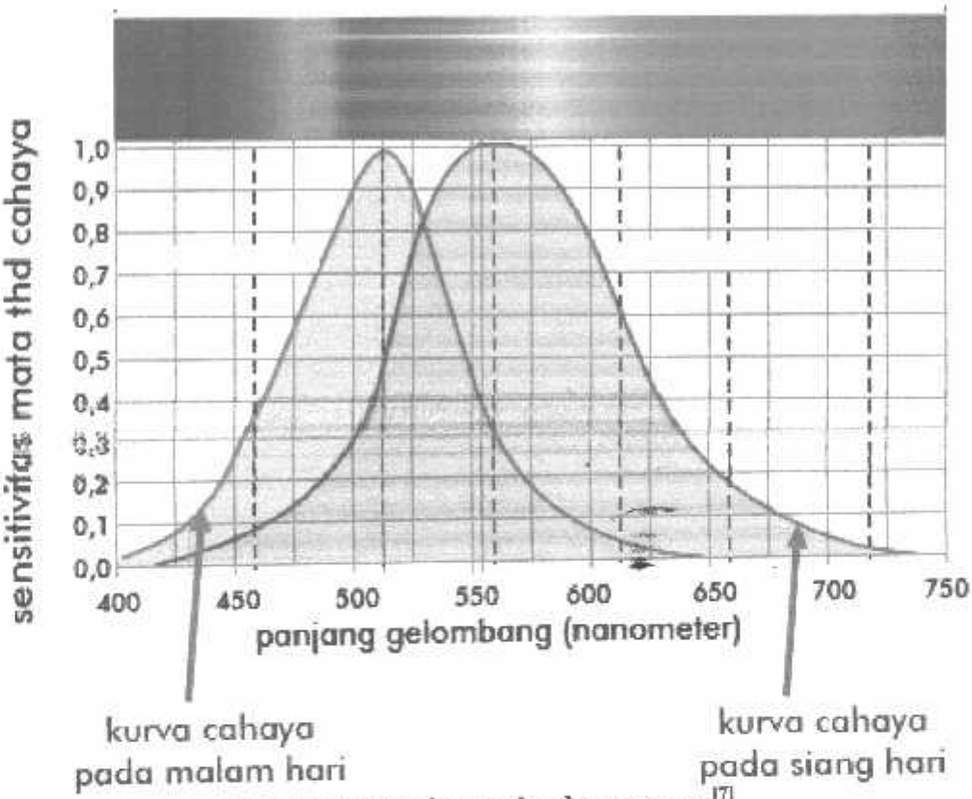
Perkiraan batas spectrum warna:

Tabel 2.1 panjang gelombang warna

NO	WARNA	PANJANG GELOMBANG (nm)
1	MERAH	620-750
2	JINGGA	590-620
3	KUNING	570-590

4	HIJAU	495-570
5	BIRU	430-495
6	UNGU	400-430

Sumber : www.soft7.com



Gambar 2.1 panjang gelombang warna[7]
Sumber : www.soft7.com

2.2 Sensor Warna TCS-230

Setiap warna bisa disusun dari warna dasar. Untuk cahaya, warna dasar penyusunnya adalah warna Merah, Hijau dan Biru, atau lebih dikenal dengan istilah **RGB (Red-Green-Blue).** Photodiode pada IC TCS230 disusun secara array 8x8 dengan konfigurasi: 16 photodiode untuk menfilter warna merah, 16 photodiode untuk memfilter warna hijau, 16 photodiode untuk memfilter warna

biru, dan 16 photodiode tanpa filter. Kelompok photodiode mana yang akan dipakai bisa diatur melalui kaki selektor S2 dan S3. Kombinasi fungsi dari S2 dan S3 bisa dilihat pada Tabel

Tabel 2.2 Pin/Kaki pengatur filter warna

S2	S3	Photodiode yang aktif
0	0	Pemfilter merah
0	1	Pemfilter biru
1	0	Tanpa filter
1	1	Pemfilter hijau

Sumber : www.paralax.com, datasheet TCS 230

TCS-230 mempunyai suatu susunan photodetector yaitu merah, hijau dan biru. Photodiode akan mengeluarkan arus yang besarnya sebanding dengan kadar warna dasar cahaya yang menimpanya. Arus ini kemudian dikonversikan menjadi sinyal kotak dengan frekuensi sebanding dengan besarnya arus. Frekuensi Output ini bisa diskala dengan mengatur kaki selektor S0 dan S1.. Frequensi output sebanding dengan intensitas warna yang dipilih. Frequensi output bisa diskala dengan mengatur logika kaki selektor S0 dan S1. Penskalaan output dapat dilihat pada tabel 2.2:

Tabel 2.3 Skala Pembanding TCS-230

S0	S1	Devide
0	0	Power Down
0	1	1:50
1	0	1: 5
1	1	1: 1

Sumber : www.paralax.com, datasheet TCS 230

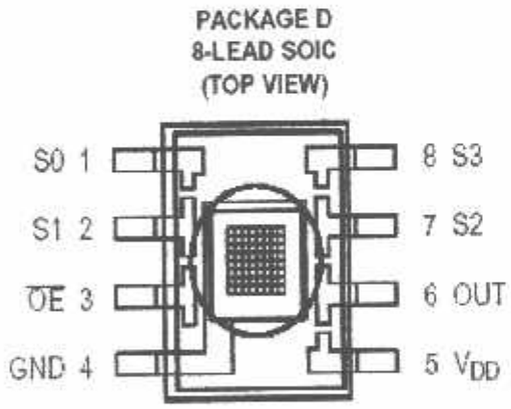
Adapun fungsi masing-masing pin pada tabel 2.4 :

Tabel 2.4 Pin/Kaki Sensor TCS-230

Pin	Sinyal	Deskripsi
1	GND	Ground Power Supply, Semua tegangan
		direfrensikan terhadap Ground
2	VDD	Tegangan Supply (2,7-5 Volt)
3	S1	Input pemilihan skala frekuensi output
4	S0	Input pemilihan skala frekuensi output
5	S2	Input pemilih filter yang diaktifkan
6	OE	Enable low
7	S3	Input pemilih filter yang diaktifkan
8	OUT	Frekuensi Output
9	LED	Control LED (Aktif LOW)
10	NC	No Conect

Sumber : www.paralax.com, datasheet TCS 230

TCS230 adalah IC pengkonversi warna cahaya ke frekuensi. Ada dua komponen utama pembentuk IC ini, yaitu photodioda dan pengkonversi arus ke frekuensi, sebagaimana bisa dilihat pada gambar 2.3.

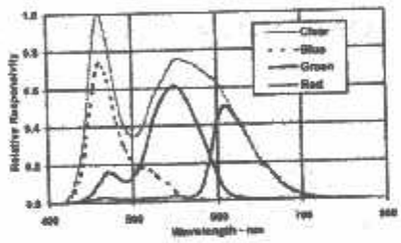


Gambar 2.2 Pin/kaki Sensor TCS-230[5]
Sumber : www.paralax.com, datasheet TCS 230

Keistimewaan TCS-230 adalah sebagai berikut

- Mengkonversi cahaya ke frekuensi dengan resolusi tinggi.
- Skala frekuensi output dapat di tentukan sesuai kebutuhan.
- Dapat berkomunikasi langsung dengan mikrokontroller.
- Tegangan suply (2,7 V sampai 5,5 V)

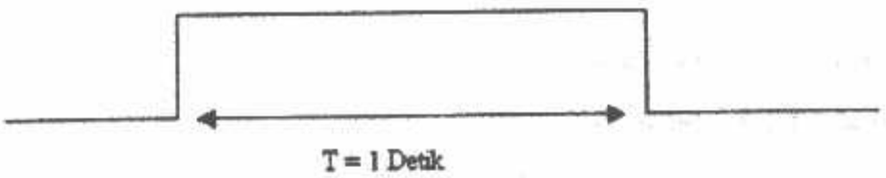
TCS-230 mempunyai ukuran sensor 5,3mm dengan ketebalan 25mm.Untuk pengukuran semua variasi warna baik kasar maupun halus yang terdapat pada area warna merupakan rata-rata frekuensi warna yang diukur. Kombinasi warna yang ditangkap merupakan saringan dan emisi pancaran yang dapat dilihat pada grafik 2.1 :



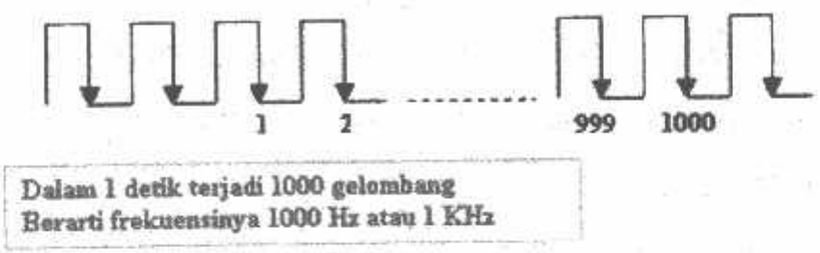
Gambar 2.3 Grafik Sensor Color Response [5]
Sumber : www.paralax.com, datasheet TCS 230

Sinyal yang dikirim dari sensor TCS-230 ke mikrokontroler berupa sinyal kotak atau dalam bentuk pulsa yang dikonversikan kedalam digital.

Untuk menghitung frekuensi output dengan membuat timer 1 detik, dan selama periode kita hitung berapa kali terjadi gelombang kotak. Sebagai contoh dapat dilihat pada gambar 2.4:

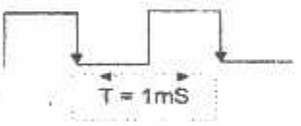


Gambar 2.4 Bentuk gelombang dalam pulsa selama 1 detik [5]
Sumber : www.paralax.com, datasheet TCS 230



Gambar 2.5 Bentuk gelombang dalam bentuk pulsa selama 1 detik.
Sumber : www.paralax.com, datasheet TCS 230 [5]

Dalam satu detik terjadi 1000 gelombang, maka frekuensinya 1000 Hz atau 1KHz, dapat di cari dengan $f=1/T$

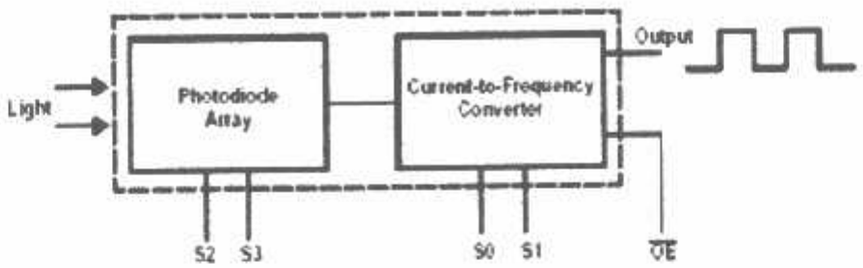


Gambar 2.6 Bentuk gelombang selama 1 periode T = mS [5]
Sumber : www.paralax.com, datasheet TCS 230

Berarti 1 gelombang penuh periodenya 1mS dengan frekuensinya 1/1mS = 1000 Hz atau 1KHz

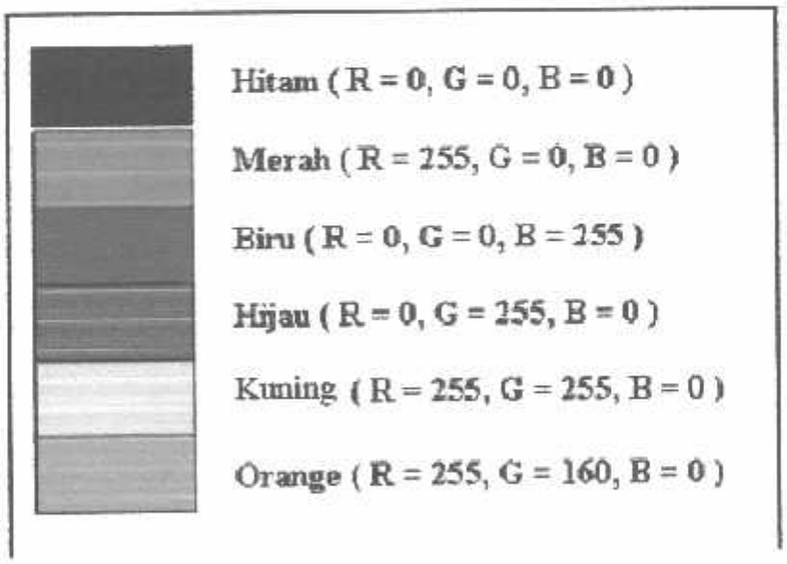
Frekuensi keluaran TCS-230 dapat dibaca dengan COUNT statement yang di tunjukkan sisi area yang diukur. TCS-230 adalah IC pengkonversi warna cahaya ke frekuensi.Ada dua komponen utama

pembentuk IC ini, yaitu photodioda dan pengkonversi arus ke frekuensi,sebagaimana bisa dilihat pada gambar 2.7:



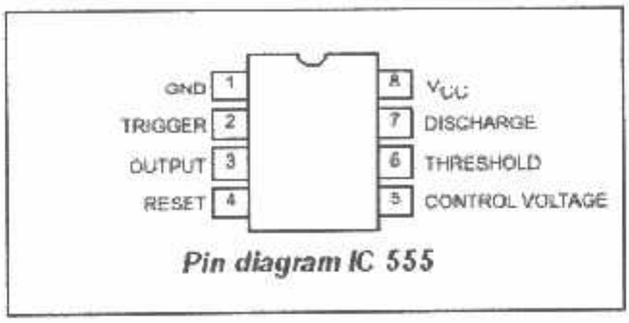
Gambar 2.7 Sketsa fisik dan blok fungsional TCS 230 [5]
Sumber : www.paralax.com, datasheet TCS 230

Setiap warna dapat disusun dari warna dasar .Untuk cahaya ,warna dasarnya adalah warna Merah, Hijau dan Biru, atau lebih dikenal dengan RGB. Gambar di bawah ini memperlihatkan beberapa sampel warna dan komposisi RGB-nya terskala 8 bit.



Gambar 2.8 Contoh Beberapa Sampel warna dan komposisi RGB-nya [5]
Sumber : www.paralax.com, datasheet TCS 230

2.3 IC 555



Gambar 2.9 Pin-Pin IC 555 [9]

Sumber : www.alldatasheet.com, datasheet IC 555

Pin 1 (GROUND) : Merupakan titik 0 V komponen yang dihubungkan dengan ground rangkaian atau *ground supply*. Pin ini ditunjukkan oleh titik (notch) yang terdapat pada badan komponen.

Pin 2 (TRIGGER) : Merupakan salah satu input komparator bagian bawah yang akan dibandingkan dengan input lain pada komparator tersebut yang telah direferensikan nilainya sebesar 1/3 tegangan supply (Vs). Jika input trigger berubah dari HIGH ke LOW dan besarnya kurang dari 1/3 Vs maka komparator bagian bawah ini akan mengaktifkan flip-flop sehingga akan dihasilkan output IC 555 dalam kondisi HIGH. Pin trigger ini mempunyai impedansi yang sangat besar, yaitu > 2MΩ.

Pin 3 (OUTPUT) : Output IC 555 dinyatakan pada pin ini.

Pin 4 (RESET) : Digunakan untuk membuat *output* IC 555 dalam kondisi LOW (reset) untuk semua kondisi input. Reset akan terjadi saat pin ini diberikan tegangan sebesar ≤ 0,7V.

Pin 5 (CONTROL) : Merupakan salah satu input komparator bagian atas dimana input lain dari komparator adalah pin Threshold pada IC 555. Pin ini digunakan untuk mengatur tegangan ambang (threshold) yang telah diatur secara default sebesar 2/3 tegangan supply (Vs). Biasanya pin ini jarang digunakan dan saat tidak digunakan pin ini dihubungkan pada titik ground rangkaian melalui sebuah kapasitor 0,01uF yang berguna untuk mengurangi gangguan noise.

Pin 6 (THRESHOLD) : Saat tegangan input pin ini berubah dari LOW ke HIGH dan besarnya lebih dari 2/3 tegangan supply (Vs) maka komparator bagian atas akan mereset flip-flop sehingga akan dihasilkan output IC 555 dalam kondisi LOW.

Pin 7 (DISCHARGE) : Merupakan jalur pembuangan arus yang berasal dari kaki kolektor transistor NPN yang terdapat pada IC 555. Pin ini biasanya dihubungkan pada sebuah kapasitor yang juga berfungsi untuk mengatur pewaktuan (timing) IC 555.

Pin 8 (VCC) : Sebagai input sumber tegangan DC yang digunakan untuk mengaktifkan IC 555. Sumber tegangan yang digunakan sebesar 5V – 15V Dalam aplikasi rangkaiannya, IC timer 555 mempunyai 3 mode operasi dasar, yaitu :

1. Monostable

   Output rangkaian monostable hanya berupa satu pulsa (HIGH) saja, yaitu saat input sinyal yang diumpankan pada pin trigger berubah dari kondisi HIGH ke LOW. Rangkaian monostable juga biasa disebut dengan rangkaian one-shoot.

2. Astable

   Output rangkaian astable berupa gelombang kotak yang berosilasi pada frekuensi dan periode tertentu, tergantung dari komponen RC yang digunakan.

3. Bistable

   Output rangkaian bistable mempunyai 2 kondisi output yang dipengaruhi oleh input pada pin trigger dan reset. Atau dapat dikatakan, output rangkaian bistable serupa dengan output rangkaian astable yang dioperasikan secara manual tanpa menggunakan komponen RC sebagai pengatur pewaktuan (timing).

2.4 Mikrokontroller AT89S8253

2.4.1 Pendahuluan

Mikrokontroller bisa dipandang sebagai sebuah mini komputer yang terintegrasi dalam sebuah chip. Didalam satu chip mikrokontroller sudah terdapat bagian-bagian seperti dalam sebuah komputer. Bagian-bagian itu antara lain ; ALU (*Arithmetic Logic Unit*), PC (*Program Counter*), SP (*Stack Pointer*), Register, ROM (*Read Only Memory*), RAM (*Random Acces Memory*), Paralel I/O, Serial I/O, *Counter* dan sebuah rangkaian *Clock*.

Seperti sebuah mikroprosessor, mikrokontroller adalah sebuah perangkat serbaguna, yang fungsi kerjanya dapat ditentukan melalui sebuah perangkat lunak yang mendeskripsikan sebuah sistem yang diinginkan.

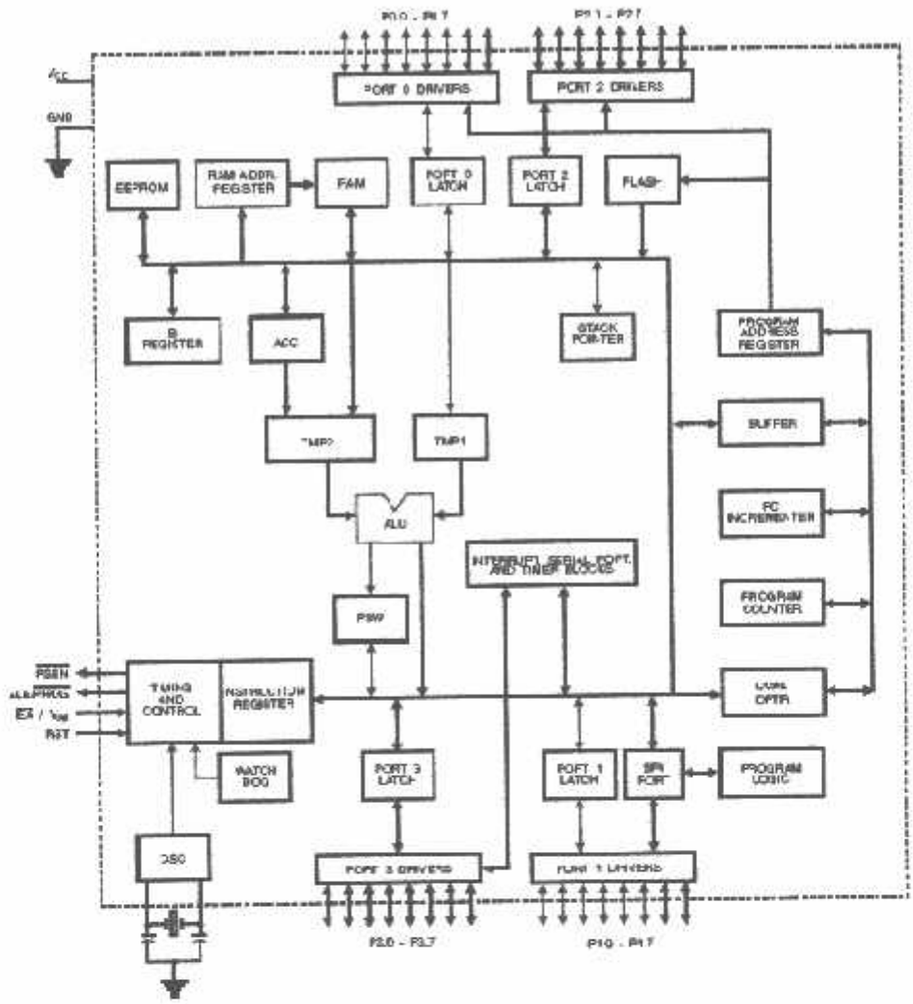
Pada saat ini terdapat banyak keluarga mikrokontroller salah satunya adalah keluarga MCS51. Salah satu tipe mikrokontroller yang termasuk dalam keluarga MCS51 adalah AT89S8253 buatan Atmel.

AT89S8253 adalah mikrokontroler keluaran atmel dengan 12K byte Flash PEROM (*Programmable and Erasable Read Only Memory*). AT89S8253 merupakan memori dengan teknologi nonvolatile memori, artinya isi memori tersebut dapat diisi ulang ataupun dihapus berulang kali.

Memori ini biasa digunakan untuk menyimpan instruksi (Perintah) berstandar MCS – 51 code sehingga memungkinkan mikrokontroler ini untuk bekerja dalam mode *Single Chip Operation* (Mode Operasi Keping Tunggal) yang tidak memerlukan *Eksternal Memori* (Memori luar) untuk menyimpan source code tersebut.

AT89S8253 juga memiliki 2K byte EEPROM (*Electrical Erasable Programmabel Read Only Memory*). Memori ini biasa digunakan untuk menyimpan data sehingga memungkinkan mikrokontroler ini untuk melakukan pengambilan data.

2.4.2 Arsitektur AT89S8253



Gambar 2.10 Blok Diagram AT89S8253[1]
Sumber : www.atmel.com, datasheet AT89S8253

IC ATMEL AT89S8253 menyediakan standart berikut:

⇒ 12K Bytes memori yang dapat diprogram ulang

⇒ 256 Bytes internal RAM

⇒ 2K Byte internal EEPROM

⇒ 32 jalur I/O (Input dan Output) yang dapat diprogram

⇒ Sepasang 16 bit Timer dan Counter

⇒ Dual data Pointer (DPTR)

⇒ Watchdog Timer

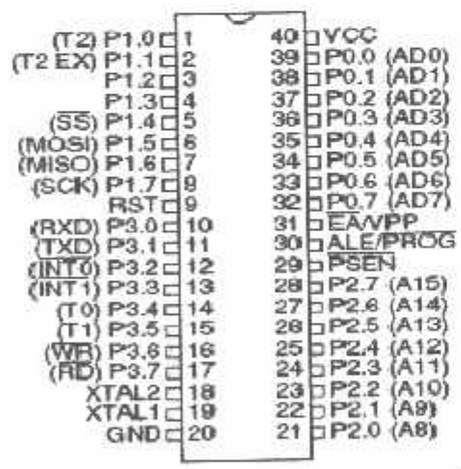
⇒ ISP Port

⇒ Mendukung serial Port secara penuh

⇒ Waktu Pemrograman yang singkat

Sebagai tambahan AT89S8253 dirancang menggunakan logika yang statis untuk 0 mode pengoperasian yang menuju ke frekuensi dasar dan pendukungan terhadap dua *Software*, serta dapat memilih model *Power Savingnya.* Mode idle akan berhenti ketika CPU sedang menjalankan RAM, *Timer/Counter*, Serial Port dan *Interrupt System* untuk terus melanjutkan fungsinya. *Model power down* akan menyimpan isi dari RAM tapi akan memberhentikan *ossilator* dan akan menghentikan semua chip lain yang sedang berfungsi sampai terdapat adanya gangguan dari luar atau *hardware* di reset.

2.4.3 Pin Deskripsi



Gambar 2 .11 Pin – Pin AT89S8253 [1]
Sumber : www.atmel.com, datasheet AT89S8253

VCC : Power Supply

GND : Ground

Port 0 : Port 0 berfungsi sebagai 8 bit I/O bertipe *open drain bi-directional.* Sebagai port keluaran masing – masing pin dapat menyerap arus sebesar 8 masukan TTL (sekitar 3,8 mA). Ketika diberikan logika '1' pada pin port 0 ini maka pin – pin port 0 ini akan dapat digunakan sebagai inputan berimpedansi tinggi.

Port 0 juga dapat dikonfigurasikan pada sebagai bus alamat/data selama proses pengaksesan data memori dan program eksternal. Jika digunakan dalam mode ini port 0 memiliki internal Pull Up.

Port 0 juga menerima kode – kode data yang diberkan padanya selama proses pemrograman dan memberikan kode – kode selama proses verifikasi program yang telah tersimpan didalam memori. Dalam hal ini dibutuhkan eksternal Pull Up selama proses verifikasi program.

Port 1 : Port 1 berfungsi sebagai 8 bit I/O Bi-directional yang dilengkapi dengan internal Pull Up. Ketika diberikan logika '1' pin ini akan di Pull Up secara internal sehingga dapat digunakan sebagai input. Sebagai inputan jika pin – pin ini dihubungkan ke ground maka masing – masing pin ini dapat menghantarkan arus karena di Pull High secara internal. Port 1 juga menerima *Low Order Address Bytes* selama melakukan verifikasi program.

Pada port 1 di AT89S8253 pin ini mempunyai alternatif seperti pada tabel berikut ini:

Tabel 2.5 Fungsi – Fungsi Alternative Port 1

Port Pin	Alternate Funtions
P1.5	MOSI (Master Output Slave Input)*
P1.6	MISO (Master Input Slave Output)*
P1.7	SCK (Serial Clock)*

Sumber : www.atmel.com, datasheet AT89S8253

Port 2 : Port 2 berfungsi sebagai 8 bit I/O Bi-directional yang dilengkapi dengan internal Pull Up Penyangga keluaran port 2 dapat memberikan atau menyerap arus empat masukan TTL (sekitar 1,6 mA). Jika diberikan logika '1' pada pin – pin port 2, maka masing – masing pin akan di Pull High secara internal sehingga dapat digunakan sebagai inputan. Sebagai inputan jika pin – pin port 2 dihubungkan ke ground (di Pull Low), maka , masing – masing pin dapat menghantarkan arus karena di Pull High secara internal.

Port 2 akan memberikan byte alamat bagian tinggi (High Byte) selama pengambilan instruksi dari memori program eksternal dan selama pengaksesan memori data eksternal yang menggunakan perintah dengan alamat 16 bit (misalkan **MOVX@DPTR**). Dalam aplikasi ini , jika ingin mengirimkan '1', maka digunakan Pull Up internal yang sudah disediakan. Selama pengaksesan memori data eksternal yang menggunaka perintah 8 bit (misalkan **MOVX@RI**),

port 2 akan mengirimkan isi dari SFR P2 (*Special Function 0Register Port 2*). Port 2 juga menerima alamat bagian tinggi (High Order Address) selama pemrograman dan verifikasi memori.

Port 3 : Port 3 sebagai 8 bit I/O Bi-directional yang dilengkapi dengan Pull Up Internal. Penyangga keluaran port 3 dapat memberikan atau menyerap arus empat masukan TTL (sekitar 1,6 mA).

Jika diberikan logika '1' pada pin pin port 3, maka masing – masing pin akan di Pull High oleh Pull Up internal sehingga dapat digunakan sebagai inputan. Sebagai inputan, jika pin – pin port 3 dihubungkan ke ground, maka masing – masing kaki akan memberikan arus karena di Pull High secara internal.

Seperti Port 1, port 3 juga mempunyai fungsi – fungsi alternatif yang diberikan oleh AT89S8253 seperti pada tabel berikut ini:

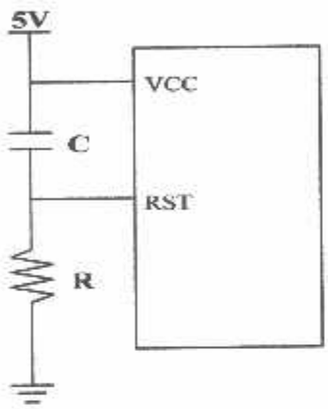
Tabel 2.6 Fungsi – Fungsi Alternatif Port 3

Port Pin	Fungsi Alternatif
P3.0	RXD (Serial Input Port)
P3.1	TXD (Serial Output Port)
P3.2	$\overline{\text{INT0}}$ (Eksternal Interrupt 0)
P3.3	$\overline{\text{INT1}}$ (Eksternal Interrupt 1)
P3.4	T0 (Timer 0 Eksternal Input)
P3.5	T1 (Timer 1 Eksternal Input)
P3.6	WR (Eksternal Data Memory Write Strobe)

P3.7	RD (Eksternal Data Memory Read Strobe)

Sumber : www.atmel.com, datasheet AT89S8253

Reset : Inputan Reset akan memberikan logika High '1' pada pin ini dengan jangka waktu yang ditentukan oleh lamanya pengosongan data muatan kapasitor. Jangka waktu minimal adalah 2 siklus mesin (24 periode frekwensi clock) ditambah waktu start On Osilator.



Gambar 2 .12 Rangkaian Power On Reset [1]
Sumber : www.atmel.com, datasheet AT89S8253

ALE/$\overline{\text{PROG}}$: Keluaran ALE (*Address Latch Enable*) menghasilkan pulsa – pulsa untuk menutup byte rendah (*Low Byte*) alamat selama mengakses memori eksternal. P0in ini juga berfungsi sebagai inputan pulsa program (*The Program Pulse Input*) atau $\overline{\text{PROG}}$ selama melakukan Flash Program. Pada operasi normal, ALE akan berpulsa dengan pewaktuan (*Timing*) atau pendetakan (*Clocking*) rangkaian eksternal. Sebagai catatan ada sebuah pulsa yang dilewati selama

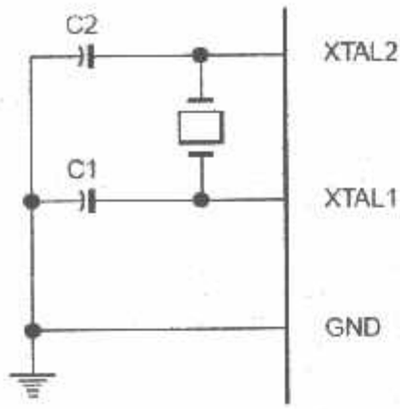
pengaksesan memori data eksternal. Jika dikehendaki operasi ALE dapat di nonaktifkan dengan cara mengatur bit 0 dari SFR (*Special Function Register*) lokasi 8Eh. Jika diberi logika '1' ALE hanya akan aktif selama menemui instruksi **MOVX** atau **MOVC**. Selain itu, pin ini secara perlahan akan di Pull High. Mematikan bit ALE tidak akan ada efeknya jika mikrokontroller mengeksekusi program secara eksternal.

$\overline{\text{EA}}$/VPP : **$\overline{\text{EA}}$/VPP** (*External Access Enable*). **$\overline{\text{EA}}$** harus selalu dihubungkan ke Ground karena digunakan untuk mengakses eksternal memori dengan lokasi 0000H sampai FFFFH. Catatan sekalipun bit '1' sudah terkunci dan terprogram, maka $\overline{\text{EA}}$ akan terkunci pada reset. **$\overline{\text{EA}}$** juga harus dihubungkan ke **Vcc** untuk melakukan menjalankan program secara internal. Pada saat Flash Programming pin ini mendapatkan tegangan sebesar 12 Volt.

XTAL1 : Merupakan input ke penguat pembalik osilator dan ke rangkaian operasi Clock internal.

XTAL2 : Keluaran dari penguat pembalik osilator.

Mikrokontroler AT89S8253 memiliki rangkaian osilator internal dengan mengacu pada frekwensi referensi pada pin XTAL1 dan XTAL2.



Gambar 2 .13 Rangkaian Cristal [1]
Sumber : www.atmel.com, datasheet AT89S8253

2.4.4 Register Fungsi Khusus

AT89S8253 mempunyai 21 ***Special Function Registers*** (Register Fungsi Khusus) yang terletak pada antara alamat 80H hingga FFH. Beberapa dari register – register ini juga bisa dialamati dengan pengalamatan bit sehingga dapat dioperasikan seperti yang ada pada RAM yang lokasinya dapat dialamati dengan pengalamatan bit.

⇒ Accumulator

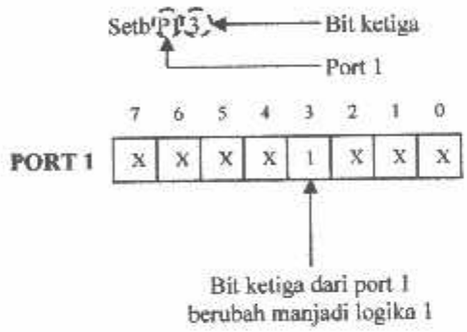
Register ini terletak pada alamat E0H. Hampir semua operasi aritmatik dan operasi logika selalu menggunakan register ini. Untuk proses pengambilan dan pengiriman data ke memori eksternal juga diperlukan register ini.

⇒ Port

89S51 mempunyai empat buah Port, yaitu Port 0, Port 1, Port 2 dan Port 3 yang terletak pada alamat 80H, 90H, A0H dan B0H. Namun,

jika digunakan eksternal memoriataupun fungsi – fungsi special, seperti Eksternal Interrupt, Serial ataupun Eksternal Timer, Port 0, Port 2 dan Port 3 tidak dapat digunakan sebagai Port dengan fungsi umum. Semua Port ini dapat diakses dengan pengalamatan secara bit sehingga dapat dilakukan perubahan output pada tiap – tiap pin dari port ini tanpa mempengaruhi port – port yang lainnya.

Sebagai contoh, jika dilakukan instruksi Setb P1.3, maka bit ketiga dari port 1 akan berkondisi high (5V) tanpa mempengaruhi bit – bit yang lain pada port ini.



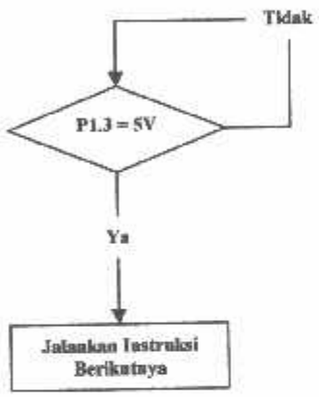
Gambar 2 .14 Bit – Bit Port [1]
Sumber : www.atmel.com, datasheet AT89S8253

Seperti yang tampak pada gambar 2 - 8, bit ketiga dari port 1 terletak pada alamat 93H oleh karena itu instruksi Setb P1.3 dapat diganti dengan instruksi Setb 93H.

Port ini digunakan untuk menunggu sinyal yang dikirim oleh komponen lain yang merupakan sinyal positif (5V) misalnya, dengan

```
Tunggu:
        Jnb     P1.3, tunggu
```

Selama kondisi pada port 1 pin ketiga masih low (0V), program akan terus melompat ke alamat yang ditunjukkan oleh label "tunggu" sehingga dapat diartikan bahwa program berhenti di alamat tersebut hingga terjadi sinyal positif (5V). Setelah sinyal positif (5V) muncul di bit ketiga dari port 1; program akan menuju ke alamat yang berikutnya:



Gambar 2 .15 Diagram Alir Deteksi Bit Ketiga Port 1 [1]
Sumber : www.atmel.com, datasheet AT89S8253

⇒ Register B

Register B digunakan bersama accumulator untuk proses aritmatik selain dapat juga difungsikan sebagai register biasa. Register ini juga bersifat *Bit Addressable*.

⇒ Stack Pointer

Stack Pointer merupakan sebuah register 8 bit yang terletak di alamat 81H. Isi dari Stack Pointer ini merupakan alamat dari data yang disimpan di stack. Stack Pointer dapat diedit atau dibiarkan saja

mengikuti standart sesudah terjadi reset. Jika Stack Pointer diisi data 5FH, area untuk proses penyimpanan dan pengambilan data dari dan ke stack adalah sebesar 32 byte, yaitu antara 60H hingga 7FH karena AT89S8253 mempunyai Internal RAM sebesar 256 byte.

⇒ Data Pointer Two Byte Register (DPTR)

Data Pointer Two Byte Register atau DPTR merupakan register 16 bit dan terletak pada alamat 82H untuk DPL (Data Pointer Low) dan 83H untuk DPH (Data Pointer High). DPTR biasa digunakan untuk mengakses source code ataupun data yang terletak di memori eksternal.

Contoh:

```
MOV   A, #01h
MOV   DPTR, #2000H
MOVX  @Dptr,A
```

2000H. Pertama, data 01H diisikan ke accumulator. Kemudian, DPTR yang berfungsi untuk menunjukan alamat penyimpanan data diisi dengan 2000H. terakhir, isi dari accumulator A disimpan ke lokasi memori yang ditunjukan oleh DPTR (*Indirect Addressing*).

⇒ Register Port Serial

AT89S8253 mempunyai sebuah *on chip serial port* (serial port dalam keping) yang dapat digunakan untuk berkomunikasi dengan peralatan lain yang menggunakan serial port juga seperti modem, shift register dan lain – lain.

Buffer (Penyangga) untuk proses pengiriman maupun pengambilan data terletak pada register SBUF, yaitu pada alamat 99H. Sedangkan

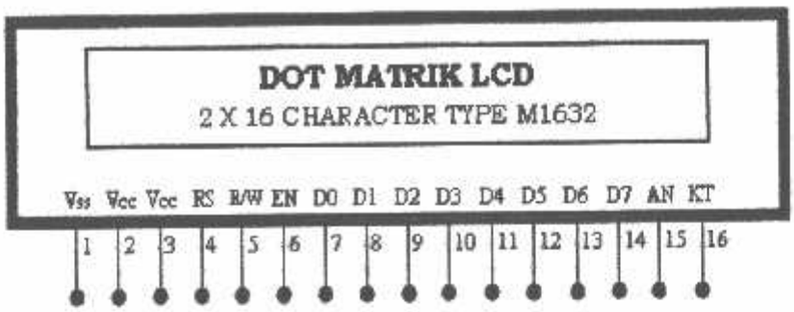
untuk mengatur mode serial dapat dilakukan dengan mengubah isi dari SCON yang terletak pada alamat 98H.

2.5 LCD (Liquid Crystal Display) M1632

Liquid Crystal Display adalah modul tampilan yang mempunyai konsumsi daya yang relatif rendah dan terdapat sebuah kontroller CMOS didalamnya. Kontroller tersebut sebagai pembangkit ROM/RAM dan display data RAM. Semua fungsi tampilan di kontrol oleh suatu instruksi modul LCD dapat dengan mudah diinterfacekan dengan MPU.

Spesifikasi dari LCD M1632:

- Terdiri dari 32 karakter yang dibagi menjadi 2 baris dengan display dot matrik 5 X 7 ditambah cursor
- Karakter generator ROM dengan 192 karakter
- Karakter generator RAM dengan 8 tipe karakter
- 80 X 8 bit display data RAM
- Dapat diinterfacekan dengan MPU 8 atau 4 bit
- Dilengkapi fungsi tambahan : Display clear, cursor home, display ON/OFF, cursor ON/ OFF, display character blink, cursor shift dan display shift
- Internal data
- Internal otomatis dan reset pada power ON
- +5 V power supply tunggal



Gambar 2.16 Pin Out LCD M1632
(Sumber: LCD Module User Manual)

LCD modul M1632 mempunyai 16 pin dengan fungsi sebagai berikut :

Tabel 2.7 Fungsi Pin – Pin LCD

Nama Pin	Jumlah	I/O	Tujuan	Fungsi
DB0-DB3	4	I/O	MPU	Tri state bidirectional lower data bus: data dibaca dari modul ke MPU atau dari MPU ditulis ke modul melalui bus
DB4-DB7	4	I/O	MPU	Tri state bidirectional upper fourdata bus: data dibaca dari modul ke MPU atau dari MPU ditulis ke modul melalui bus
E	1	Input	MPU	Sinyal operasi dimulai: sinyal aktif baca/tulis
R/W	1	Input	MPU	Sinyalpilih data dan tulis (0:tulis,1:baca)
RS	1	-	Power supply	Sinyal pilih register 0: Instruction register (write) Busy flag dan addess counter (read) 1:Data register (write dan read)
VLC	1	-	Power supply	Penyetelan kontras pada tampilan LCD
VDD	1	-	Power supply	+ 5V

VSS	1	-	Power supply	Ground 0V

*(**Sumber** : LCD Module User Manual)*

Pada pin 15 (V_+) diberi diode gunanya adalah agar tegangan yang masuk sesuai dengan *data sheet* yaitu sebesar 4,5 Volt maksimal.

Tegangan diode = 0,7 Volt

V_{cc} = 5 Volt

Jadi tegangan yang masuk = 5 – 0,7 = 4,3 Volt.

2.5.1 Register

Control LCD mempunyai 2 register 8 bit yaitu *Instruction register* (IR) dan *Data Register* (DR). Kedua register tersebut dipilih melalui *Register Select* (RS). IR menyimpan kode instruksi seperti Display clear dan cursor shift, dan alamat informasi dari Display Data RAM (DD RAM) dan character generator RAM (CG RAM)

DR menyimpan data sementara untuk ditulis ke DD RAM atau CG RAM, atau dibaca dari DD RAM atau CG RAM. Ketika data ditulis ke DD RAM atau CG RAM dari MPU, data di DR secara otomatis ditulis ke DD RAM atau CG RAM dengan operasi internal. Tetapi ketika data dibaca dari DD RAM atau CG RAM maka alamat data ditulis pada IR.Data tersebut akan dimasukkan ke DR dan MPU akan membaca data dari DR, Setelah operasi pembacaan, alamat berikutnya diset data dari DD RAM atau CG RAM pada alamat tersebut akan dimasukkan ke DR untuk operasi berikutnya. Display data RAM (DD RAM) mempunyai kapasitas area 80 X 8 bit. Beberapa area dari DDRAM yang tidak digunakan untuk display dapat digunakan sebagai General data RAM.

Pada LCD masing-masing pin mempunyai range alamat tersendiri, alamat itu diekspresikan dengan bilangan heksa. Untuk line 1 range alamat berkisar antara 00h-0Fh sedangkan untuk line 2 alamat berkisar antara 40h-4fh

*(**Sumber** : LCD Module User Manual)*

2.6 ISD (Information Storage Devices) 1420

Information Storage Device adalah sebuah chip IC yang mampu merekam dan menyimpan data suara yang direkam tersebut dalam interval waktu tertentu. Pada setiap jenis IC ISD kode nama pada dua digit terakhir menunjukkan lama duarasi waktu maksimal yang mampu disimpan kedalam device tersebut.

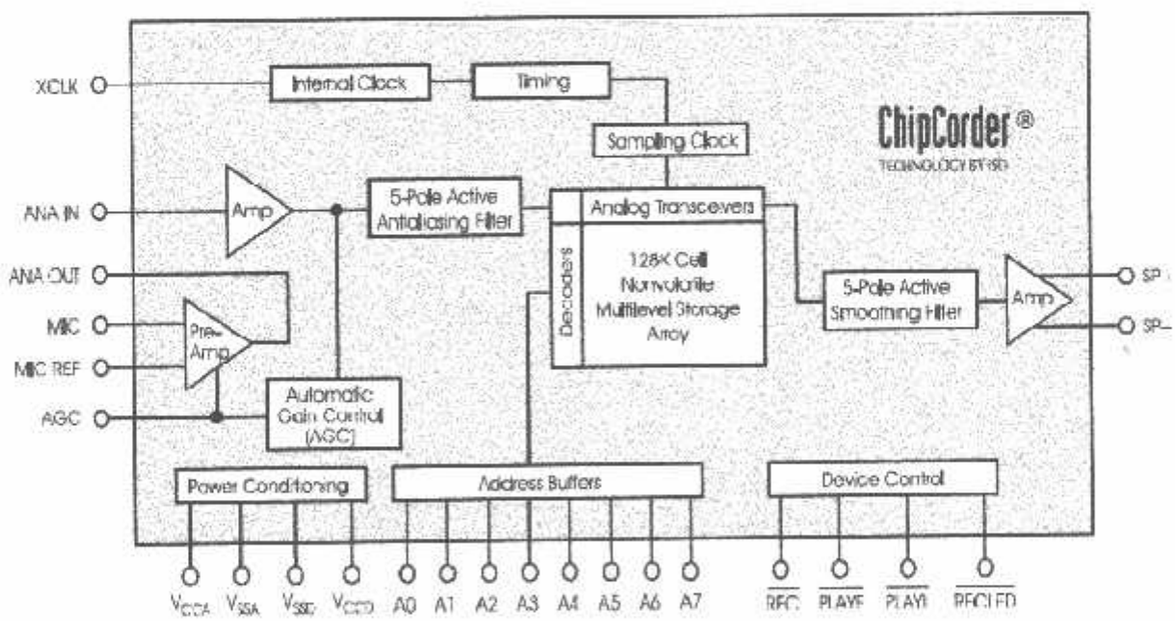
Didalam IC ini telah include beberapa kebutuhan perekaman dan pemanggilan data kembali diantaranya penguat mikrofone, filter suara dan penguat speaker untuk menampilkan suara kembali.

ISD 1420 digunakan sebagai outputan berupa suara yang berkualitas. ISD 1420 terbagi menjadi beberapa segmen alamat, dengan tiap segmen alamat mempunyai durasi penyimpanan suara (audio saving duration) sebesar 120ms. ISD 1420 memunyai 8 buah pin yang digunakan sebagai alamat, yaitu (A0 - A7), sehingga dapat di berikan alamat mulai dari 00H sampai FFH, atau terbagi dalam $2^8 = 256$ alamat. ISD 1420 ini merupakan sebuah IC yang dirancang untuk dapat merekam dan memutar kembali suara yang telah terekam di dalam IC. Sehingga ISD 1420 sangat tepat untuk digunakan menyimpan dan memutar suara untuk aplikasi-aplikasi tertentu.

ISD 1420 mempunyai komponen-komponen yang telah tertanam di dalamnya, antara lain: oscilator internal, mikrophone pre-amplifier, gain kontrol otomatis, filter parata dan speaker amplifier. Secara keseluruhan IC ini dapat digunakan untuk merekam dan memutar dengan komponen sederhana, seperti mikrophone, speaker dan beberapa komponen penunjang, dan dua buah saklar tekan dan sumber tegangan. Rekaman akan disimpang dalam sel memori yang tidak mudah hilang. IC ini merupakan IC (Strorage Direct Analog) yang dapat dengan langsung menyimpan suara yang berupa analog, kedalam memori EPROM.

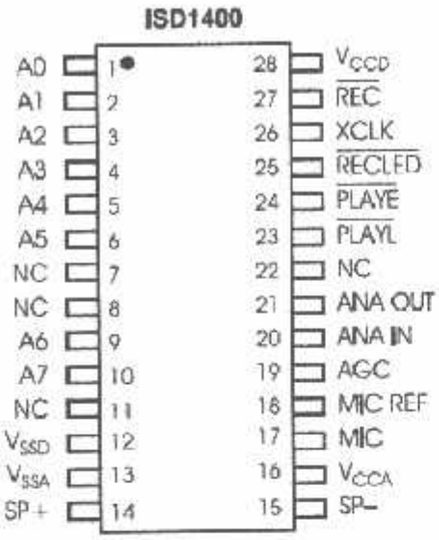
ISD 1420 mempunyai waktu penyimpanan suara selama 20 detik, yang dapat disimpan di alamat yang kita tentukan.

Blok Diagram ISD 1420.



Gambar 2.17 Rangkaian ISD 1420 [2]
Sumber : www.alldatasheet.com, datasheet ISD 1420

Konfigurasi Pin-Pin ISD 1420



Gambar 2.18 Konfigurasi Pin dari ISD 1420 [2]
Sumber : www.alldatasheet.com, datasheet ISD 1420

- Playback, *adge – actifated* (played) pin 24.

  Ketika sinyal akan berpindah ke kondisi low, maka *playe* akan berjalan sampai tanda akhir dari ruang memori yang tercapai. Setelah melakukan *playback*, ISD secara otomatis akan kembali kemode *standby*, dan *playback* akan berhenti jika ruang memori telah habis.

- Playback, level – *activated* (PLAYL) pin 23

  Ketika input berpindah dari high ke low, maka PLAYL akan berjalan. *Playback* akan berjalan sampai *input high*, atau ruang memori telah habis. ISD akan kembali ke mode *standby* jika *playback* telah berhenti.

- Record Led Output (RECLED) Pin 25:

  Output dari RECLED akan *low* selama perekaman, maka *output* ini digunakan untuk mengetahui bahwa sedang terjadi perekaman.

- Record (REC) pin 27:

  Proses perekaman terjadi apabila REC dalam keadaan low, sampai kita selesai melakukan perekaman.

- Automatic Gain Control (AGC) pin 19:

  AGC digunakan untuk menambah atau mengurangi penguatan (gain) dari pre-amplificr. AGC dapat secara dinamis meluaskan batas dari suara yang terekam dari suara bisikan sampai suara yang keras.

- Speaker Output (SP+, SP-) Pin 14 dan 15:

  Ini digunakan untuk mengeluarkan suara yang telah direkam ke speaker. Output ini mempunyai impedansi 16 Ω.

- Optimal Eksternal clock (XCLK) pin 26:

  Digunakn untuk menambah Kristal clock bila dibutuhkan pewaktuan yang lebih besar dan presisi, tetapi bila tidak digunakan harus dihubungkan dengan ground.

- VCCA dan VCCD pin 16 dan 28:

  Analog dan digital sircuit didalam ISD menggunakan bus power yang terpisah, untuk meminimalisasi noise. Pin ini harus dihubungkan sedekat mungkin dengan sumber tegangan.

- VSSA dan VSSD (grond) pin 13 dan 12:

  Sama sepertti VSSA dan VSSD, Analog dan digital sircuit didalam ISD menggunakan bus power yang terpisah, untuk meminimalisasi noise. Pin ini harus dihubungkan sedekat mungkin dengan ground.

- Addres input (A0 - A7) pin 1-6 dan 9-10:

Input ini mempunyai dua fungsi, tergantung dari level dua Most Significant Bits (MSB) dari alamat.

Jika MSB ini keduanya low, maka semua input digunakan sebagai bit pengalamatan, untuk merekam atau memutar ulang

- Microphone – input (MIC) pin 17:

  Kaki microphone ini terhubung dengan VCC melalui beberapa kapasitor tang terhubung seri, bersamaan dengan resistor 10KΩ yang berada dalam chip.

- Microphone Reference (MIC REF) pin 18:

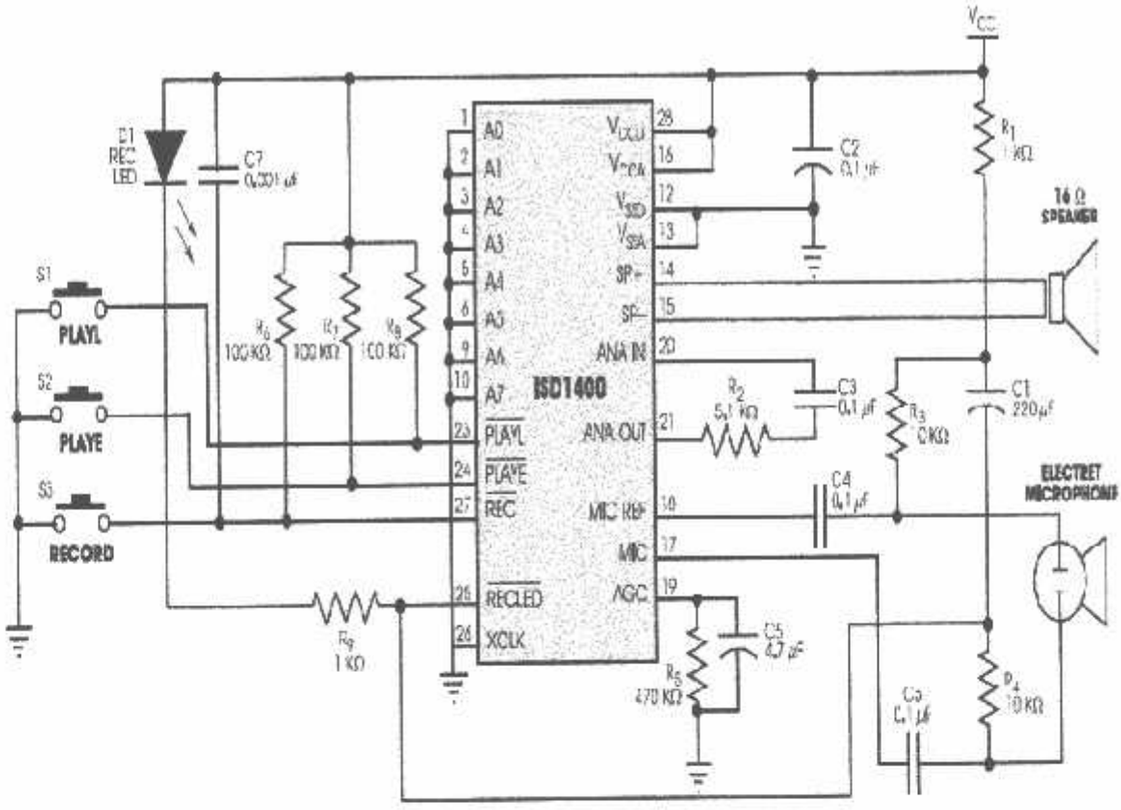
  Ketika MIC REF terhubung ke Vcc dengan microphone ke ground, maka tingkat noise selama perekaman dapat dikurangi. Bila tidak digunakan, maka pin ini tidak boleh terhubung dengan sinyal atau tegangan apapun, harus dalam keadaan terbuka.

- Analog Output (ANA OUT) pin 21:

  Sinyal dari microphone dikuatkan dan dikeluarkan melalui ANA OUT pin. Penguatan dari Pre-amp tergantung dari AGC pin.pre-amp ini mempunyai penguatan maksimum sekitar 24 dB.

- Analog Input (ANA IN) pin 20:

  Kapasitor eksternal menghubungkan antara ANA IN dan ANA UOT pin.



Gambar 2.19 Rangkaian pengisi ISD 1420 [2]
Sumber : www.alldatasheet.com, datasheet ISD 1420

Untuk melakukan perekaman, dilakukan langkah langkah seperti berikut:

1. Set alamat dimana kita akan mulai menyimpan suara, dengan cara memberikan logika 0 atau 1 pada A0 sampai A7.
2. Memasang speaker da microphone.
3. Member logika 0 pada pin REC.
4. Mulai merekam suara yang diinginkan, dengan maksimal durasi penyimpanannya adalah selama 20 detik.
5. Jika sudah selesai, beri logic 1 pada pin REC.

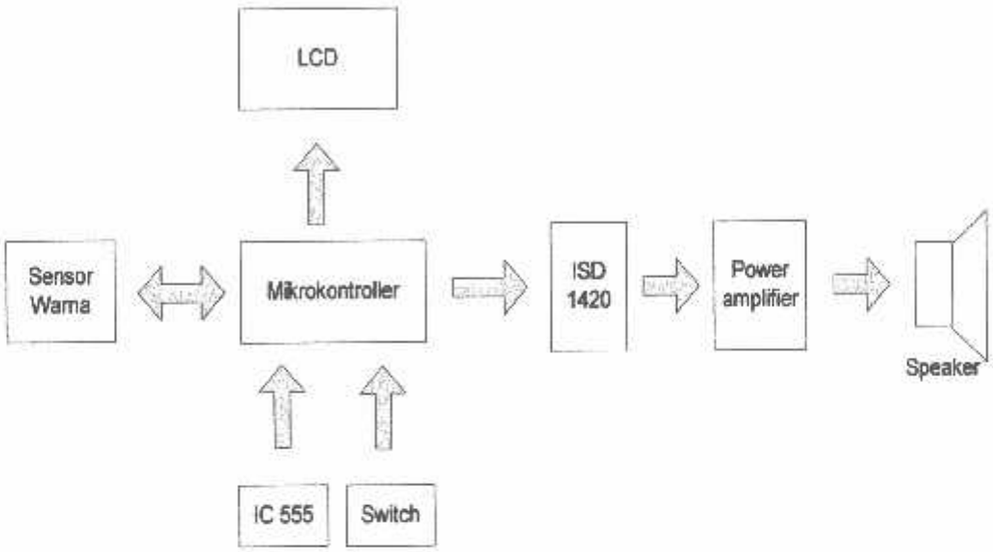
Untuk mengeluarkan suara yang telah direkam, dilakukan hal hal berikut:

1. Set alamat dimana kita telah menyimpan suara yang telah terekam dalam ISD.
2. Ada dua cara yang dapat dilakukan untuk mengeluarkan suara pada ISD
    1. Dengan cara memberikan logika 0 pada PLAYL.
    2. Member logika transisi low pada PLAYE, maka ISD akan secara otomatis akan mengeluarkan suara sampai sinyal EOM dikeluarkan.
    3. Sinyal EOM akan keluar, setiap kali ISD telah habis mengeluarkan suara.

BAB III
PERENCANAAN DAN PEMBUATAN ALAT

3.1. Perancangan Perangkat Keras (*Hardware*)

Blok diagram sistem dapat dilihat pada gambar dibawah ini:



Gambar 3.1. Blok Diagram Sistem

Fungsi dari masing – masing blok diagram adalah sebagai berikut :

-. Sensor warna

Sensor yang digunakan adalah TCS 230, untuk mendeteksi warna.

-. Mikrokontroller AT89S8253

Mikrokontroller merupakan inti atau pusat dari seluruh sistem. Disini mikrokontroller berfungsi sebagai pengolah data.

-. LCD

Berfungsi sebagai penampil R G B dari warna yang telah dibaca oleh sensor.

-. Switch

Berfungsi untuk mengeluarkan suara yang terdeteksi olch sensor.

-. IC 555

Berfungsi sebagai suply timer eksternal untuk mikrokontroller

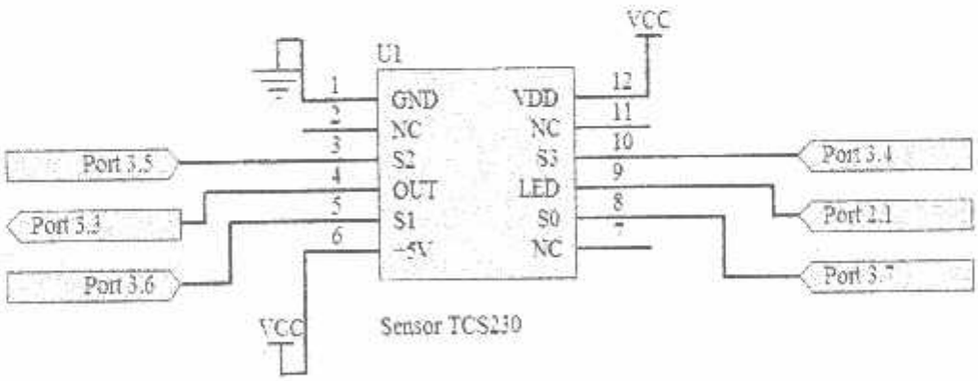
-. ISD 1420

Merupakan IC penyimpan suara, yang mana suara yang di hasilkan akan disesuaikan dengan warna yang diterima oleh sensor.

Berdasarkan diagram blok diatas, maka prinsip kerja dari alat tersebut dapat dijelaskan sebagai berikut :

AT89S8253 sebagai pengontrol utama, kemudian sensor digunakan untuk mendeteksi warna dari benda yang dideteksi, data dari sensor di kirimkan ke mikrokontroller dan diolah untuk disesuaikan dengan data base yang ada. Jika data yang dikirimkan sensor tersedia di data base mikrokontroller, dan button telah aktif, maka mikro akan memerintahkan ISD untuk mengeluarkan suara yang sesuai dengan warna yang terdeteksi oleh sensor. Tetapi apabila data yang di kirimkan sensor ke mikrokontroller tidak ada dalam data base maka suara yang di keluarkan ISD adalah erorr.

3.2 Rangkaian Sensor *TCS 230*



Gambar 3.2 Perencanaan Rangkaian Sensor TCS 230

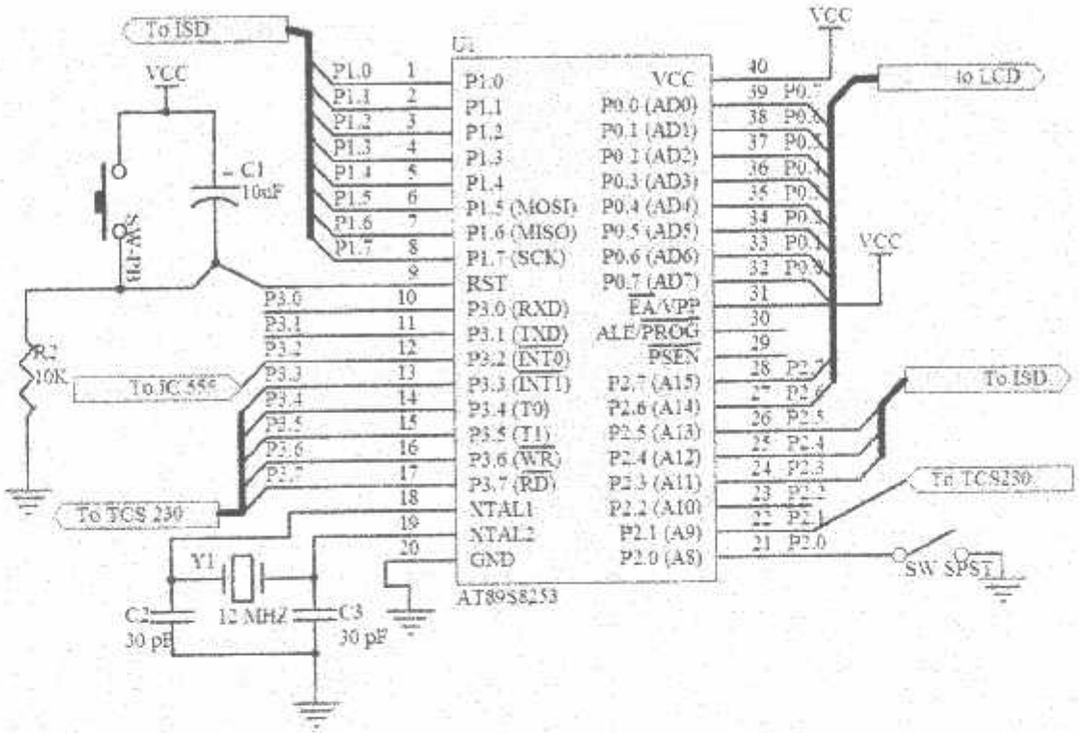
Pada aplikasi ini menggunakan sensor warna TCS 230. Port 3.5 dan port 3.4 yang digunakan untuk mengaktifkan atau memilih filter warna, yang akan di tampilkan pada LCD. Port 3.3 sebagai outputan dari sensor. Port 2.1 berfungsi untuk memerintahkan led agar menyala. Photodiode akan mengeluarkan arus yang besarnya sebanding dengan kadar warna dasar cahaya yang menimpanya. Arus ini kemudian dikonversikan menjadi sinyal kotak dengan frekuensi sebanding dengan besarnya arus. Frekuensi Output ini bisa diskala dengan mengatur kaki selektor S0 dan S1 yang terhubung dengan Port 3.7 dan 3.6 pada mikrokontroller. Pada aplikasi ini digunakan skala 1:5 atau 20% dari frekuensi warna yang di terima oleh sensor. Pengolahan keluaran sensor ke mikrokontroler AT89S8253 dengan cara membaca pulsa yang di keluarkan sensor selama satu periode dengan begitu dapat diketahui bila satu periode pulsa semakin lebar maka keluaran frekuensi semakin besar dan sebaliknya.

3.3 Perancangan Minimum Sistem *AT89S8253*

Mikrokontroller AT89S8253 dirancang untuk dapat berdiri sendiri karena terdapat EEPROM, RAM serta port *input/output* dan perlengkapan lainnya dengan tujuan menambah kemudahan dalam aplikasinya juga dalam *software*.

Mikrokontroller yang digunakan pada sistem adalah mikrokontroller jenis AT89S8253 yang merupakan IC CMOS 8 bit *internal* RAM, 40 pin dan 3 port *I/O*.

Dalam perancangan sistem ini pin-pin yang dipergunakan adalah sebagai berikut :

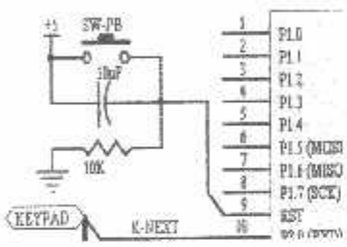


Gambar 3.3 Rangkaian Minimum sistem AT89S8253

1. Pin 1 (P1.0) sampai pin 8 (P1.7) digunakan untuk jalur ISD.
2. Pin 9 (Reset) digunakan untuk reset mikrokontroller.
3. Pin 12 (P3.2) digunakan untuk jalur IC 555.
4. Pin 13 (P3.3) sampai pin 17 (P3.7) dan pin 22 (P2.1) digunakan untuk sensor TCS 230.
5. Pin 18 (XTAL 1) untuk *clock* pada Mikrokontroller AT89S8253.
6. Pin 19 (XTAL 1) untuk *clock* pada Mikrokontroller AT89S8253.
7. Pin 20 (GND) untuk *ground* Mikrokontroller AT89S8253.
8. Pin 21 (P2.0) digunakan untuk button.
9. Pin 24 (P2.3) sampai pin 26 (P2.5) digunakan untuk ISD.

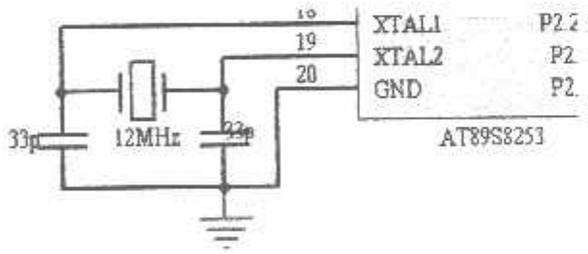
10. Pin 27 (P2.6) sampai pin 28 (P2.7) dan pin 32 (P0.7) sampai pin 39 (P0.0) untuk jalur LCD
11. Pin 40 (Vcc) Berfungsi sebagai tegangan *supply* Vcc = 5 Volt.

Perancangan rangkaian *reset* pada mikrokontroler AT89S8253 adalah dengan memberikan logika *high* pada pin reset mikrokontroler AT89S8253. Rangkaian *reset* ini diperoleh dari *application note mcs-51 Design Consideration* dari ATMEL. Berikut ialah gambar rancangan rangkaian *reset* pada AT89S8253 :



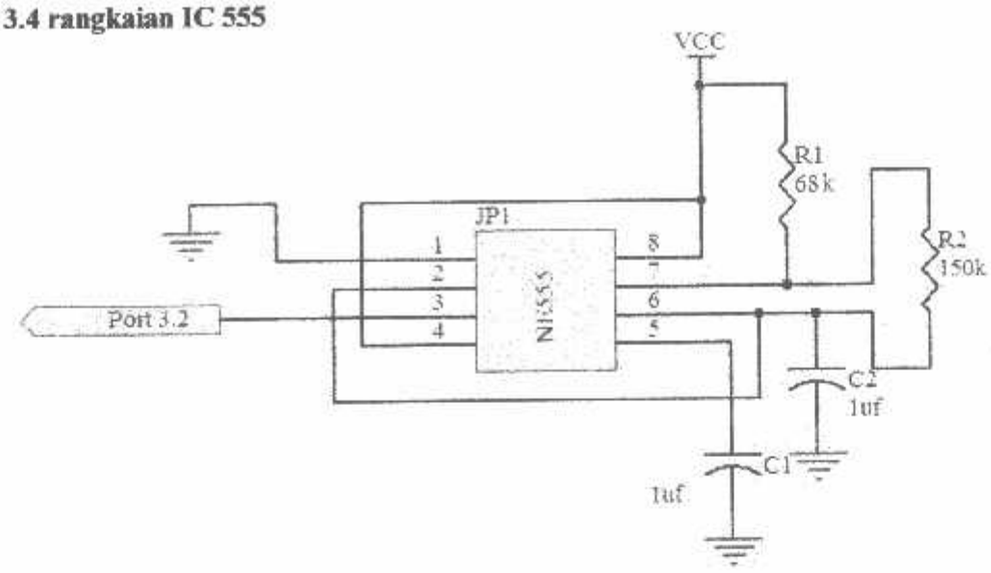
Gambar 3.4 Rangkaian *Reset* pada AT89S8253

***Osilator* pada rangkaian minimum sistem AT89S8253 menggunakan kristal 12 MHz dan kapasitor 33 pF. Nilai kapasitor ini diperoleh dari tabel *datasheet* tentang penggunaan kapasitor untuk rangkaian *osilator* / sistem *clock* pada AT89S8253. Berikut ialah gambar rangkaian *osilator* pada mikrokontroler AT89S8253:**



Gambar 3.5 Rangkaian *osilator* pada mikrokontroler AT89S8253

3.4 rangkaian IC 555



Gambar 3.6 rangkaian IC 555

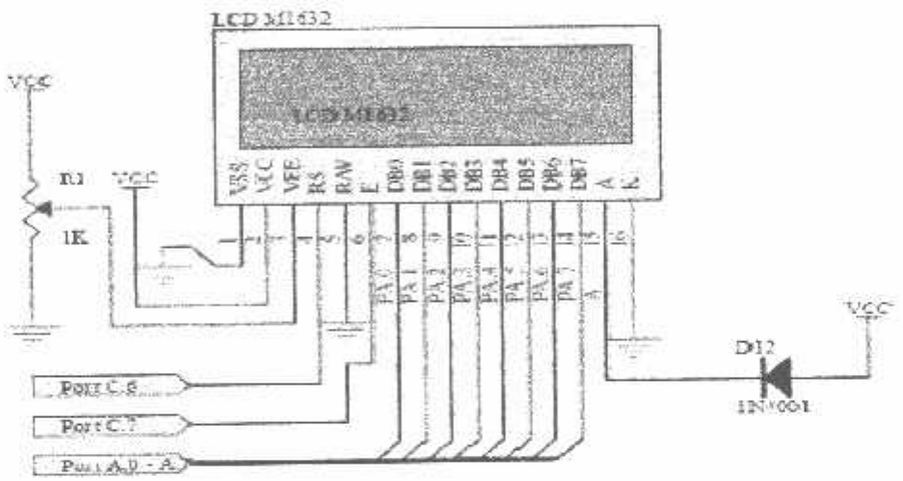
Pada perancangan ini digunakan IC 555 sebagai pembangkit pulsa atau clock. Rangkaian yang dibuat pada perancangan alat ini adalah rangkaian astable, dimana besar pulsa yang dihasilkan dapat di atur, dengan cara menentukan besar resistor dan capasitor yang digunakan.

Output dari IC ini di hubungkan dengan port 3.2 (INT0) mikrokontroller. Clock dari IC 555 ini digunakan mikrokontroller untuk menjalankan atau mematikan timer dan counter internal pada mikrokontroller secara bersamaan.

3.5 Perancangan Rangkaian *LCD*

Sebagai tampilan data pengaturan jam, tanggal dan data dari RTC digunakan *display* LCD dot matrik 2 x 16 karakter. Sinyal – sinyal yang dipergunakan oleh LCD adalah *data bus*, RS, R/W dan E. Sinyal E dihubungkan ke P3.4 untuk mengaktifkan LCD. LCD akan aktif jika

mikrokontroller memberikan instruksi tulis pada alamat LCD. Sedangkan port 3.5 dipergunakan untuk memberikan sinyal RS yang membedakan data yang diberikan pada LCD. Sinyal RS diberikan ke LCD untuk membedakan sinyal antara instruksi program atau instruksi penulisan data. Untuk pin R/W akan berlogika *low* (0) apabila dihubungkan dengan *ground* maka LCD difungsikan hanya untuk menuliskan program atau data ke *display*. Untuk mengambil data dari mikrokontroller maka pin – pin data dihubungkan dengan Port 0.0 sampai Port 0.7 yang merupakan pin – pin data dari mikrokontroller.



Gambar 3.7 Perancangan Rangkaian *Liquid Crystal Display* (LCD)

V_{R1} pada pin 1 (V_{SS}) digunakan untuk mengatur kontras dari karakter yang ditampilkan, sedangkan pada pin 15 (V_+) diberi diode gunanya adalah agar tegangan yang masuk sesuai dengan *data sheet* yaitu sebesar 4,5 Volt maksimal.

Tegangan diode = 0,6 Volt

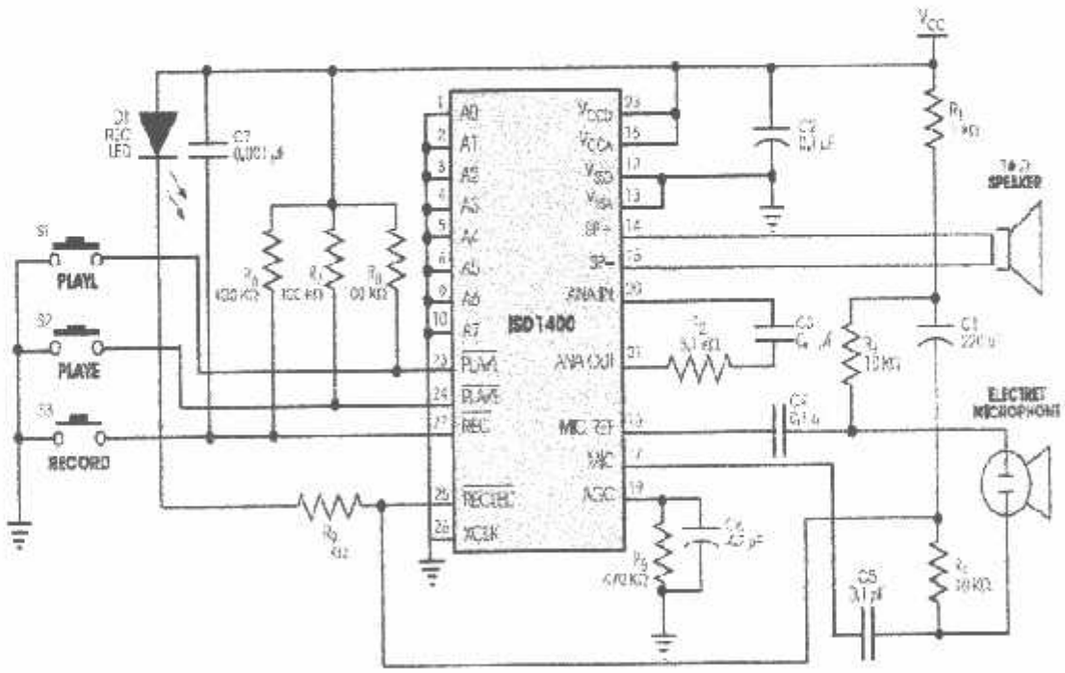
V_{cc} = 5 Volt

Jadi tegangan yang masuk = 5 – 0,6 = 4,4 Volt.

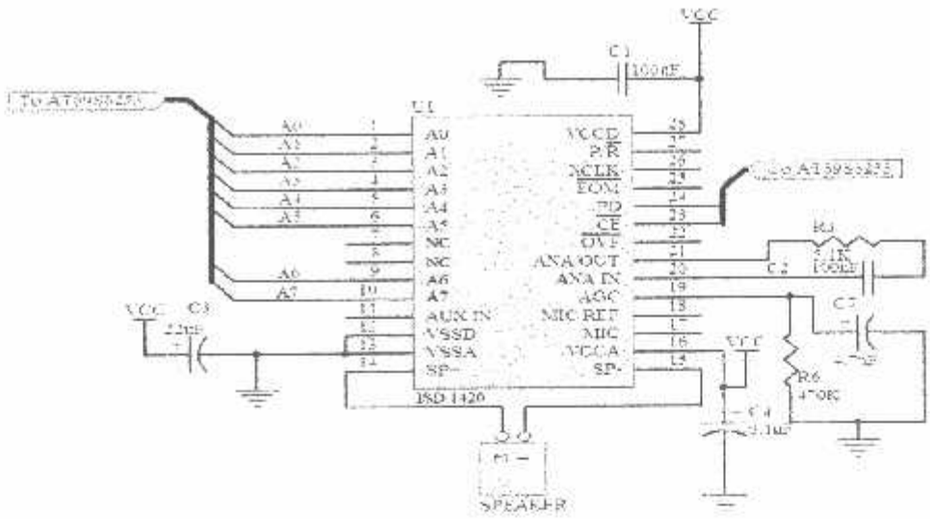
3.6 Perancangan Rangkaian *ISD 1420.*

Perancangan rangkaian ISD digunakan untuk menentukan alamat dimana kita melakukan perekaman suara, sehingga mikrokontroller akan mudah untuk mengakses alamat dari suara suara yang telah kita rekam. Untuk melakukan perekaman langkah pertama yang harus dilakukan adalah mengeset alamat sesuai dengan alamat atau durasi waktu yang dibutuhkan. Schingga untuk memanggil suara yang diinginkan adalah dengan menentukan alamat dari suara tersebut.

ISD yang digunakan untuk perancangan alat ini adalah ISD 1420, seperti pada gambar di bawah ini.



Gambar 3.8 Rangkaian Modul ISD 1420



Gambar 3.9 Rangkaian ISD 1420

Pada rangkaian ini digunakan IC ISD 1420. Alamat yang digunakan untuk komunikasi dengan mikrokontroller adalah A0 sampai A7, yang dihubungkan dengan port 0. Untuk memutar suara yang ada pada ISD, mikrokontroller mengirimkan data alamat, dimana suara yang akan di putar di simpan. Jika alamat sudah di tentukan, maka mikrokontroller memerintahkan ISD untuk memutar suara yang tentukan, melalui pin 24 (PLAYE).

Tabel 3.1 Alamat Suara Pada ISD 1420

NO	JENIS WARNA	DATA ISD								DATA ISD
		A7	A6	A5	A4	A3	A2	A1	A0	
1	HITAM	0	0	0	0	0	0	0	0	00H
2	UNGU	0	0	0	1	0	0	0	0	08H
3	ERROR	0	0	0	0	1	0	0	0	10H
4	MERAH	1	1	0	0	1	0	0	0	13H
5	KUNING	1	0	0	1	0	1	0	0	29H
6	HIJAU	1	1	0	0	1	1	0	0	33H
7	COKLAT	1	1	0	1	0	0	0	0	0AH
8	BIRU	0	1	1	1	1	1	0	0	3EH
9	JINGGA	1	1	1	1	1	0	0	0	1FH
10	PUTIH	1	1	1	1	1	0	1	0	5FH

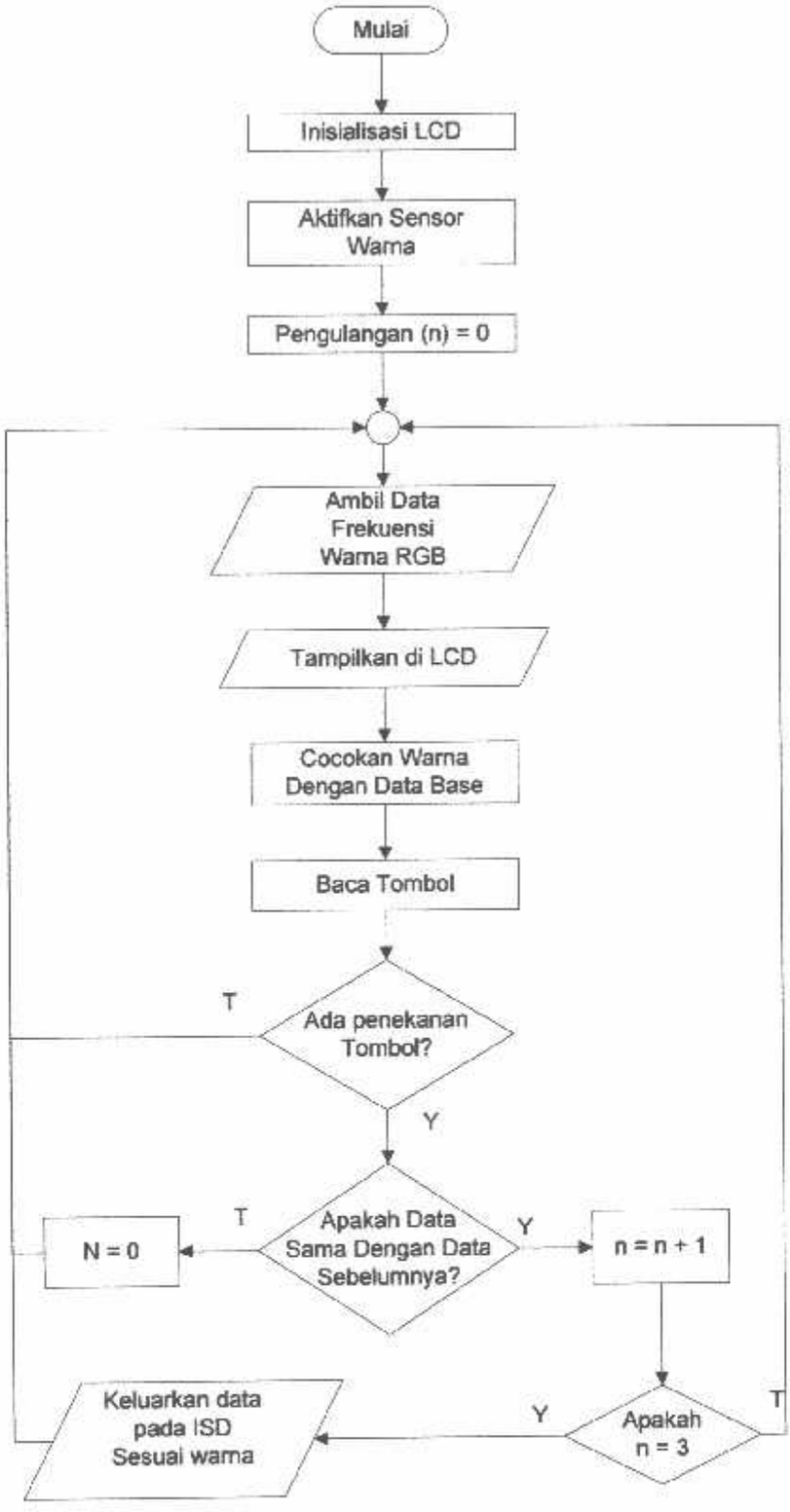
Durasi waktu yang tersedia di ISD 1420 hanya 20 detik, maka suara yang akan disimpan tidak boleh melebihi kapasitas yang telah ada. Tabel 3.1 merupakan alamat dari suara-suara yang telah terekam di dalam ISD.

Tabel 3.2 Range Warna Pada Data Base Mikrokontroller

NO	WARNA	FREKUENSI		
		R	G	B
1	MERAH	174 - 260	15 - 255	14 - 84
2	JINGGA	268 - 752	96-252	23 - 112
3	KUNING	220 - 386	257 - 420	90 - 200
4	HIJAU	42 - 160	146 - 607	70 - 235
5	BIRU	29 - 126	60 - 143	166 - 389
6	UNGU	38 - 79	31 - 221	71 - 161
7	COKLAT	82 - 177	28 - 144	36 - 110
8	HITAM	2 - 28	2 - 34	2 - 33
9	PUTIH	200 - 450	350 - 710	400 - 880

3.7 Perancangan Perangkat Lunak

Perancangan perangkat lunak (*software*) yang digunakan dalam perencanaan dan pembuatan alat akan dipaparkan dalam *flowchart* sistem secara kesceluruhan. Pembuatan *software* hanya dilakukan pada mikrokontroler menggunakan bahasa pemrograman *Basic* dengan bantuan *compiler BASCOM - 8051*. Diagram alir atau *Flowchart* program secara keseluruhan adalah sebagai berikut:



Gambar 3.10. ***Flow chart*** **Program**

BAB IV

PENGUJIAN ALAT

Dalam bab ini akan di bahas mengenai pengujian alat yang telah dibuat. Hal ini dapat dilakukan untuk mengetahui kekurangan dari kinerja sistem yang telah dibuat, sehingga dapat diketahui apakah alat tersebut dapat bekerja sesuai dengan yang telah di rencanakan. Dalam rangka pengujian alat tersebut diuraikan percobaan yang telah di lakukan untuk mengetahui respon dari keseluruhan alat yang telah dirancang.

4.1. Tujuan Pengujian

Tujuan pengujian yang dilakukan terhadap sistem aplikasi ini adalah sebagai berikut :

- Mengetahui unjuk kerja rangkaian Sensor *TCS 230* dan *LCD*.
- Mengetahui unjuk kerja rangkaian *IC 555*.
- Mengetahui unjuk kerja rangkaian *ISD 1420*.

4.2. Alat-alat untuk pengujian

Alat-alat yang digunakan dalam pengujian adalah :

1. Modul sensor warna TCS 230
2. Rangkaian mikrokontroller AT89S8253
3. Rangkaian IC 555
4. Rangkaian ISD 1420
5. Benda-benda yang akan di deteksi.

4.3. Pengujian

4.3.1. Pengujian Sensor Warna *TCS 230.*

Dalam pengujian rangkaian *sensor* ini memiliki tujuan yaitu untuk mengetahui data counter yang masuk ke mikrokontroller, yang ditampilkan frekuensi RGB nya pada LCD. Diagram blok dari pengujian rangkaian Sensor ini terlihat pada gambar di bawah ini :

Gambar 4.1. Diagram Blok Pengujian Rangkaian *Sensor.*

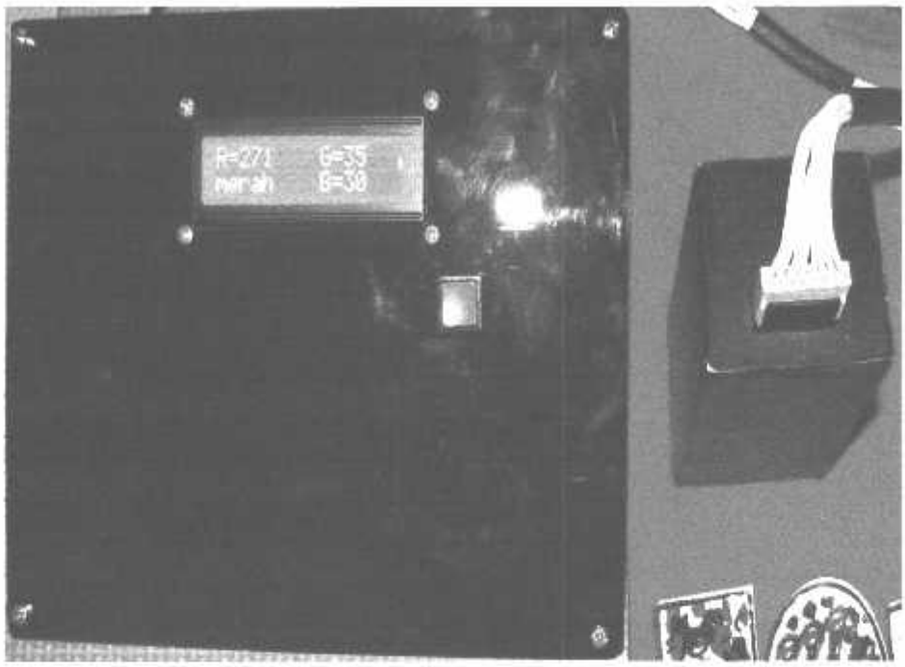
Langkah – langkah pengujian rangkaian ini adalah sebagai berikut :

1. Merangkai peralatan seperti dalam gambar blok diagram di atas.
2. Membuat perangkat lunak pegujian rangkaian sensor. Program ini berisi inisialisasi LCD dan karakter yang akan ditampilkan dari sensor. Yang selanjutnya diisikan pada mikrokontroler AT89S8253.
3. Mengaktifkan catu daya minimum sistem AT89S8253 dan LCD.
4. Meletakkan sensor di atas benda yang di uji.
5. Menuliskan data pengujian kedalam tabel.

1. Pengujian I Warna Merah

Tampilan LCD dari hasil pengujian baju warna merah.

Range Warna: R=(174-260), G=(15-255), B=(14-84).



Gambar 4.2 Sampling hasil pengujian baju warna merah.

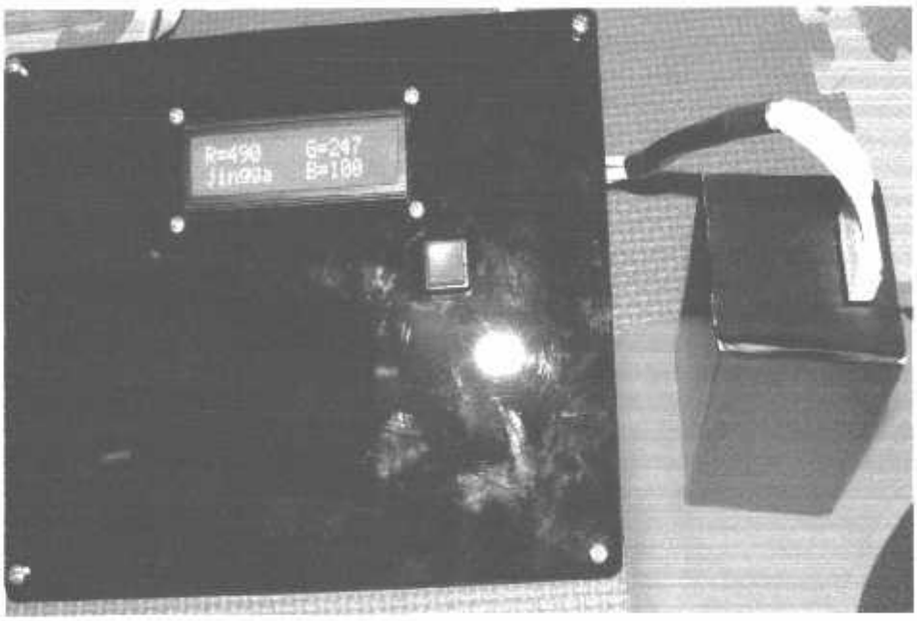
Tabel 4.1 Hasil pengujian sensor untuk warna merah.

NO	BENDA	FREKUENSI		
		R	G	B
1	Baju	271	35	30
2	Binder	238	47	45
3	Tutup Toples	245	41	31
4	Kertas Mengkilap	246	43	37
5	Kertas doff	267	80	62

2. Pengujian II Warna Jingga

Tampilan LCD dari hasil pengujian baju warna jingga.

Range Warna: R=(430-868), G=(243-359), B=(89-150).



Gambar 4.3 Sampling hasil pengujian baju warna jingga.

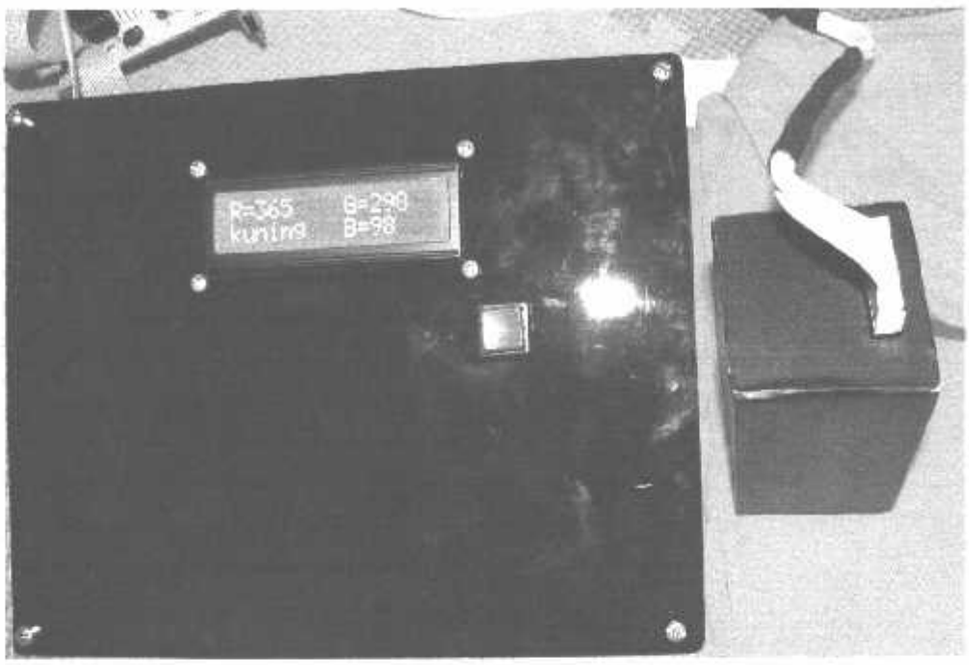
Tabel 4.2 Hasil pengujian sensor untuk warna Jingga.

NO	BENDA	FREKUENSI		
		R	G	B
1	Baju	524	263	109
2	Kertas	448	251	92
3	Jaket	525	263	119
4				
5				

3. Pengujian III Warna Kuning

Tampilan LCD dari hasil pengujian baju warna kuning.

Range Warna: R=(220-386), G=(257-420), B=(90-200).



Gambar 4.4 Sampling hasil pengujian baju warna kuning.

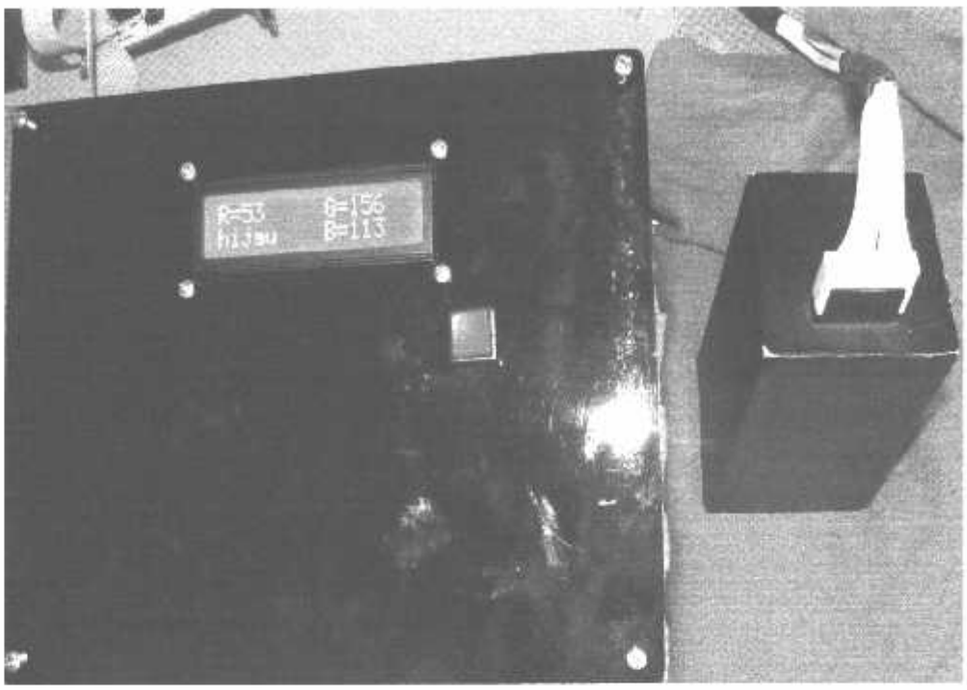
Tabel 4.3 Hasil pengujian sensor untuk warna kuning.

NO	BENDA	FREKUENSI		
		R	G	B
1	Spon	340	358	141
2	Baju	365	298	98
3	Tutup Botol Plastik	366	384	119
4	Kertas Mengkilap	352	382	96
5	Kertas doff	370	397	125

4. Pengujian IV Warna Hijau

Tampilan LCD dari hasil pengujian baju warna Hijau.

Range Warna: R=(42-160), G=(146-607), B=(70-235).



Gambar 4.5 Sampling hasil pengujian baju warna Hijau.

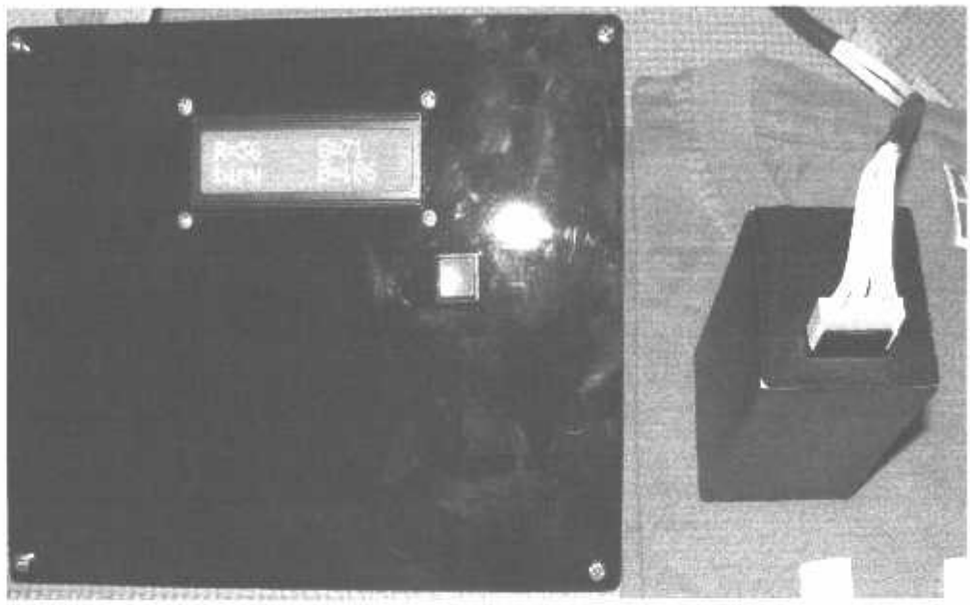
Tabel 4.4 Hasil pengujian sensor untuk warna Hijau.

NO	BENDA	FREKUENSI		
		R	G	B
1	Baju	53	156	113
2	Bantal	96	173	95
3	Botol Frestea	135	254	122
4	Kertas Mengkilap	44	153	78
5	Kertas doff	72	177	105

5. Pengujian V Warna Biru

Tampilan LCD dari hasil pengujian baju warna Biru.

Range Warna: R=(29-126), G=(60-143), B=(166-389).



Gambar 4.6 Sampling hasil pengujian baju warna Biru.

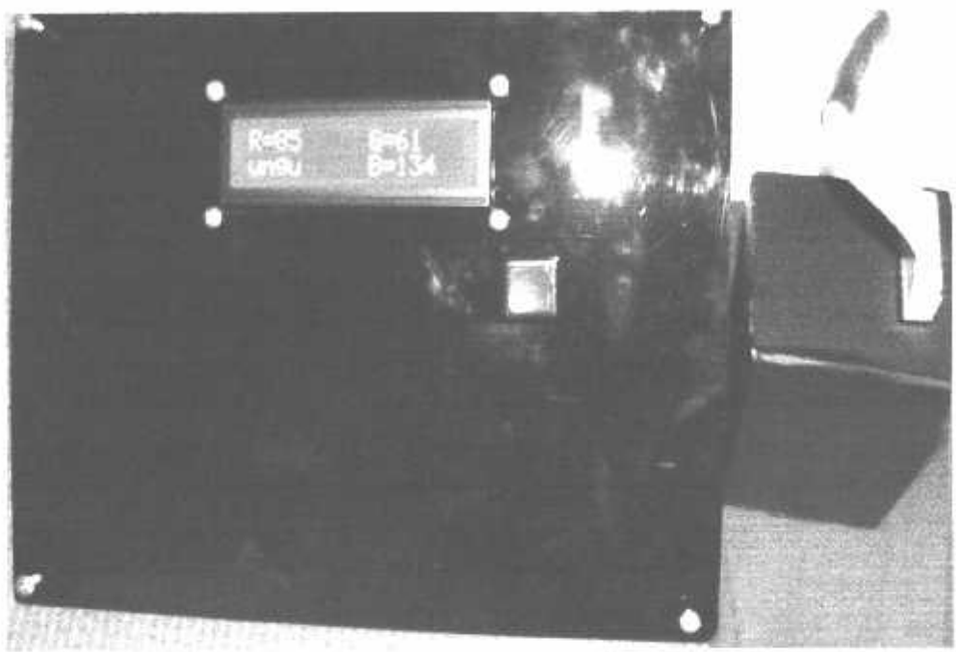
Tabel 4.5 Hasil pengujian sensor untuk warna Biru.

NO	BENDA	FREKUENSI		
		R	G	B
1	Baju	36	71	186
2	Spon	60	121	255
3	Tas Jinjing	44	107	262
4	Tutup Teko	74	142	337
5	Kertas doff	84	188	440

6. Pengujian VI Warna Ungu

Tampilan LCD dari hasil pengujian baju warna ungu.

Range Warna: R=(38-79), G=(31-221), B=(71-161).



Gambar 4.7 Sampling hasil pengujian baju warna Ungu.

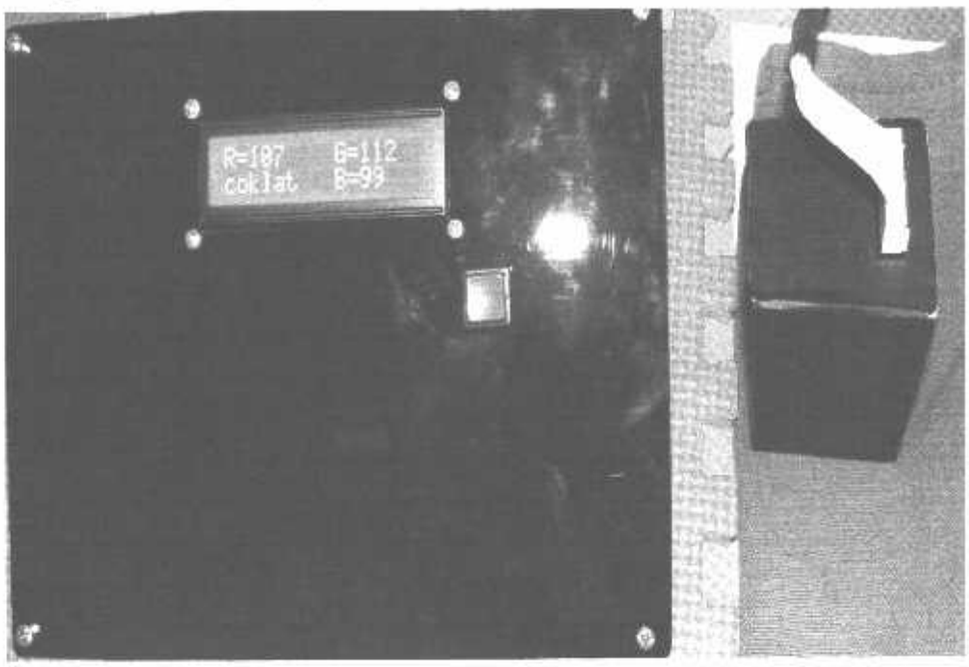
Tabel 4.6 Hasil pengujian sensor untuk warna Ungu.

NO	BENDA	FREKUENSI		
		R	G	B
1	Baju	64	35	74
2	Tutup Toples	73	68	159
3	Buku	78	67	151
4	Kertas	44	41	127
5				

7. Pengujian VII Warna Coklat

Tampilan LCD dari hasil pengujian baju warna Coklat.

Range Warna: R=(82-177), G=(28-144), B=(36-110).



Gambar 4.8 Sampling hasil pengujian baju warna Coklat.

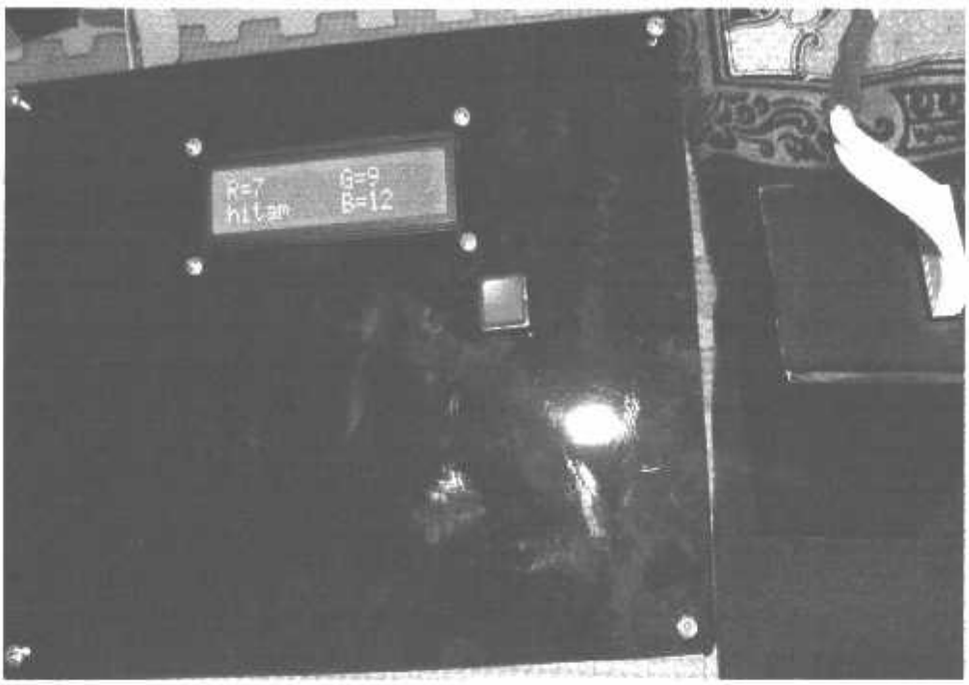
Tabel 4.7 Hasil pengujian sensor untuk warna Coklat.

NO	BENDA	FREKUENSI		
		R	G	B
1	Celana	107	112	99
2	Busur	89	64	43
3	Kardus	127	112	90
4	Kulit	93	61	49
5				

8. Pengujian VIII Warna Hitam

Tampilan LCD dari hasil pengujian baju warna Hitam.

Range Warna: R=(2-28), G=(2-34), B=(2-33).



Gambar 4.9 Sampling hasil pengujian baju warna Hitam.

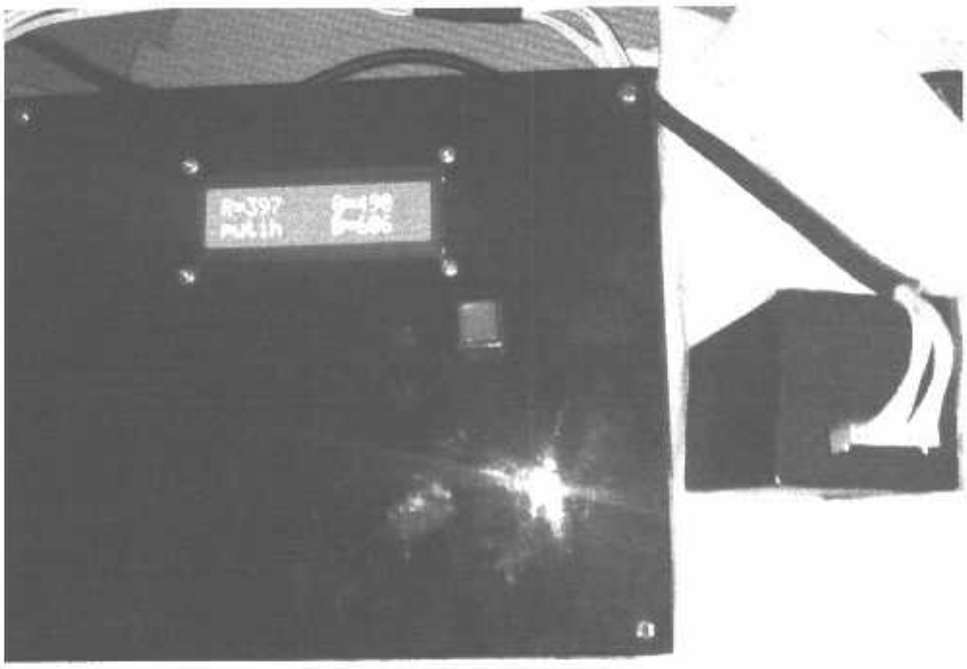
Tabel 4.8 Hasil pengujian sensor untuk warna Hitam.

NO	BENDA	FREKUENSI		
		R	G	B
1	Baju	7	9	12
2	Mika	7	9	11
3	Multimeter	20	25	30
4	Gantungan Kunci	11	16	20
5	Charger	11	15	19

9. Pengujian IX Warna Putih

Tampilan LCD dari hasil pengujian baju warna Putih.

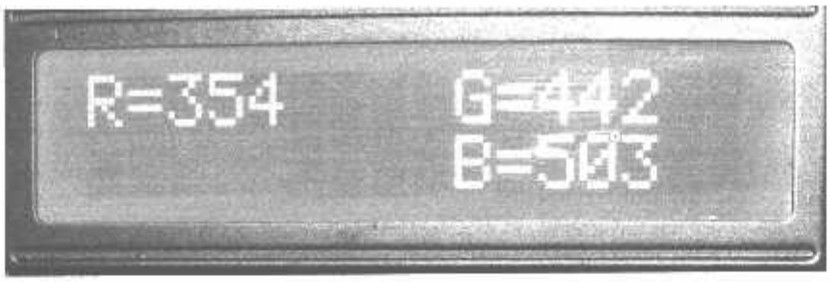
Range Warna: R=(200-450), G=(350-710), B=(400-880).



Gambar 4.10 Sampling hasil pengujian baju warna Putih.

Tabel 4.9 Hasil pengujian sensor untuk warna Putih.

NO	BENDA	FREKUENSI		
		R	G	B
1	Baju	426	514	545
2	Tisu	344	440	505
3	Tas	393	509	560
4	Casing HP	382	497	524
5	Kertas	392	491	560



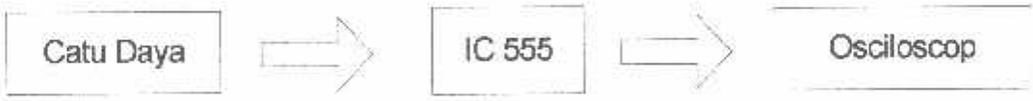
Gambar 4.11 Tampilan LCD dari Hasil Pengujian Rangkaian *sensor*.

Dari pengujian diperoleh hasil bahwa di layar LCD muncul frekuensi dari RGB sensor, dengan demikian dapat disimpulkan bahwa rangkaian sensor dan LCD berfungsi dengan baik.

4.3.2. Pengujian Rangkaian IC 555.

Dalam pengujian rangkaian IC 555 ini memiliki tujuan yaitu untuk mengetahui apakah rangkaian ini dapat bekerja dengan baik dalam menghasilkan clock.

Diagram blok pengujian rangkaian IC 555 terlihat pada gambar dibawah ini :



Gambar 4.12 Diagram Blok Pengujian Rangkaian IC 555

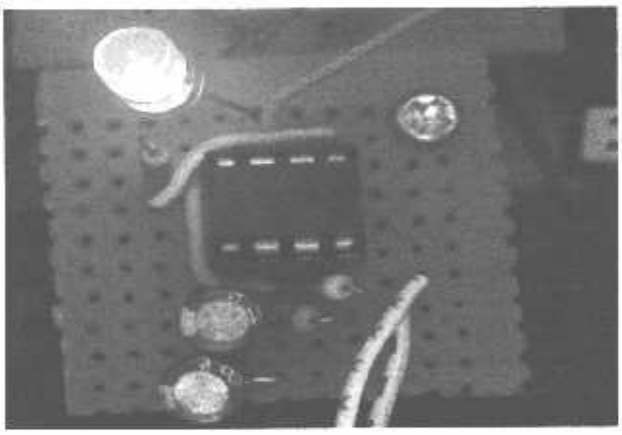
Frekuensi yang di inginkan dari IC 555 ini adalah 4 KHz. Untuk bisa mendapatkan frekuensi yang diinginkan, maka kita menentukan komposisi antara R dan C, pada alat ini besar Ra = 68K, Rb = 150K dan C = 1mF.

Dengan nilai komponen tersebut, maka dihasilkan frekuensi sekitar 3.913Hz, melalui perhitungan sebagai berikut:

$$f = \frac{1,44}{(Ra+2\,Rb)c} + \frac{1,44}{(68000+(2.150000))1x10^{-6}} = 3,913\ \text{Hz}$$

Dari hasil pengukuran didapatkan frekuensi dari IC 555 sebesar 4.049 Hz, dari data tersebut dapat dicari persentase error hasil pengujian terhadap perhitungan adalah:

$$V_1 = Hasil\_perhitungan$$
$$V_2 = Hasil\_pengujian$$
$$\%Error = \frac{|V_1 - V_2|}{V_1} x100\%$$
$$\%Error = \frac{|4,049 - 3,913|}{4,049} x100\% = 3,35\%$$

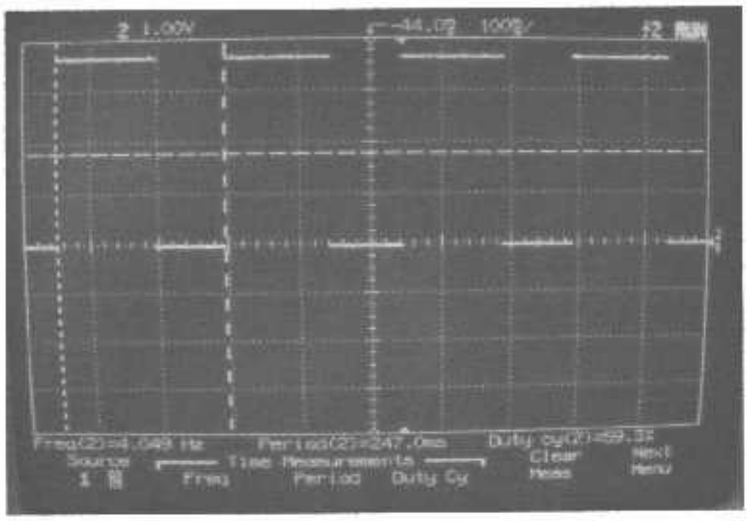


Gambar 4.13 Rangkaian IC 555

Langkah – langkah pengujian IC 555 adalah sebagai berikut :

1. Alat dirangkai seperti pada gambar diagram blok diatas.
2. Menentukan resistor dan capasitor yang digunakan, untuk menentukan output dari IC 555.

3. Mengaktifkan catu daya.
4. Menghitung output dari IC 555 yang tertampil di osciloscop.



Gambar 4.14 Output Signal dari IC 555

Dari hasil pengujian dapat dilihat bahwa rangkaian IC 555 dapat bekerja dengan baik dalam memberikan clock sesuai dengan yang diinginkan.

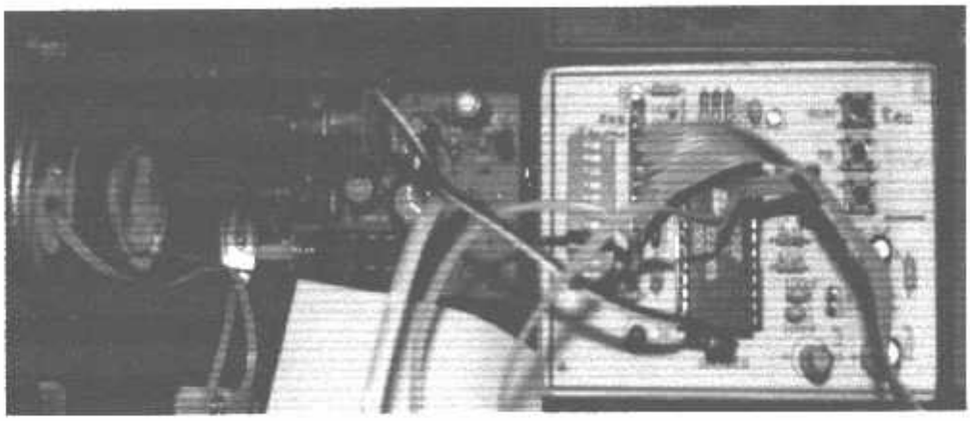
4.3.3. Pengujian Rangkaian ISD 1420

Pengujian rangkaian ini bertujuan untuk mengetahui kesesuaian data biner pada IC ISD 1420 yang digunakan untuk alamat tiap suara yang telah direkam. Dalam pengujian IC ISD ini data biner yang nantinya dari mikro di wakili oleh saklar deep switch.

Langkah langkah pengujian IC ISD 1420 adalah sebagai berikut:

1. Menempatkan pengalamatan 00H pada dipswitch, sebagai alamat awal untuk pengisian suara.
2. Menekan REC selama melakukan perekaman.

3. Untuk perekaman berikutnya, dicari alamat yang kosong terlabih dahulu, baru merekam lagi.
4. Untuk mendengarkan hasil rekaman, IC dihubungkan dengan amplifier, dan ditekan play.



Gambar 4.15 Hasil Pengujian Rangkaian ISD 1420.

4.3.4 Pengujian Alat Keseluruhan

Pengujian I

Pengujian untuk Baju Warna Hitam

Tabel 4.10 Hasil Pengujian Alat Untuk Baju Warna Hitam.

NO	PENGUJIAN	OUTPUT ISD
1	1	HITAM
2	2	HITAM
3	3	HITAM
4	4	HITAM
5	5	HITAM

Pengujian II

Pengujian untuk Baju Warna Coklat

Tabel 4.11 Hasil Pengujian Alat Untuk Celana Warna Coklat.

NO	PENGUJIAN	OUTPUT ISD
1	1	COKLAT
2	2	COKLAT
3	3	COKLAT
4	4	COKLAT
5	5	COKLAT

Pengujian III

Pengujian untuk Baju Warna Merah

Tabel 4.12 Hasil Pengujian Alat Untuk Baju Warna Merah.

NO	PENGUJIAN	OUTPUT ISD
1	1	MERAH
2	2	MERAH
3	3	MERAH
4	4	MERAH
5	5	MERAH

Pengujian IV

Pengujian untuk Baju Warna Jingga

Tabel 4.13 Hasil Pengujian Alat Untuk Baju Warna Jingga.

NO	PENGUJIAN	OUTPUT ISD
1	1	MERAH

2	2	JINGGA
3	3	JINGGA
4	4	ERROR
5	5	JINGGA

Pengujian V

Pengujian untuk Baju Warna Kuning

Tabel 4.14 Hasil Pengujian Alat Untuk Baju Warna Kuning.

NO	PENGUJIAN	OUTPUT ISD
1	1	KUNING
2	2	KUNING
3	3	KUNING
4	4	KUNING
5	5	KUNING

Pengujian VI

Pengujian untuk Baju Warna Hijau

Tabel 4.15 Hasil Pengujian Alat Untuk Baju Warna Hijau.

NO	PENGUJIAN	OUTPUT ISD
1	1	HIJAU
2	2	HIJAU
3	3	HIJAU
4	4	HIJAU
5	5	HIJAU

Pengujian VII

Pengujian untuk Baju Warna Biru

Tabel 4.16 Hasil Pengujian Alat Untuk Baju Warna Biru.

NO	PENGUJIAN	OUTPUT ISD
1	1	BIRU
2	2	BIRU
3	3	BIRU
4	4	BIRU
5	5	BIRU

Pengujian VIII

Pengujian untuk Baju Warna Ungu

Tabel 4.17 Hasil Pengujian Alat Untuk Baju Warna Ungu.

NO	PENGUJIAN	OUTPUT ISD
1	1	UNGU
2	2	BIRU
3	3	UNGU
4	4	UNGU
5	5	UNGU

Pengujian IX

Pengujian untuk Baju Warna Putih

Tabel 4.18 Hasil Pengujian Alat Untuk Baju Warna Putih.

NO	PENGUJIAN	OUTPUT ISD
1	1	PUTIH

2	2	PUTIH
3	3	PUTIH
4	4	PUTIH
5	5	PUTIH

BAB V

PENUTUP

5.1 Kesimpulan

Dari pembuatan alat pendeteksi warna ini, dapat diambil kesimpulan sebagai berikut:

1. Alat bantu identifikasi warna ini dapat bekerja pada warna merah, kuning, hijau, biru, coklat, hitam dan putih.
2. Dari hasil pengujian sensor, dari 20 Jenis benda yang telah di uji, untuk setiap warna, masih terdapat dalam range frekuensi.
3. Dari hasil pengujian alat secara keseluruhan, kesalahan hanya terjadi pada warna jingga dan ungu.
4. Prosentase error dari rangkaian clock adalah sebesar = 3,35%

5.2 Saran

Dari pembuatan alat pendeteksi warna ini, masih ada beberapa kekurangan, untuk itu ada beberapa hal yang perlu dilakukan untuk pengembangan:

1. Sebaiknya alat dibuat sekecil mungkin dengan catu daya baterai, sehingga dapat dibawa kemana-mana dengan lebih praktis dan efisien.
2. Untuk dapat mendeteksi warna dengan lebih teliti sebaiknya range warna dibuat lebih luas, dengan asumsi tidak ada range warna yang sama dengan warna lainya

DAFTAR PUSTAKA

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LAMPIRAN

INSTITUT TEKNOLOGI NASIONAL
FAKULTAS TEKNOLOGI INDUSTRI
JURUSAN TEKNIK ELEKTRO S-1
KONSENTRASI TEKNIK ELEKTRONIKA

FORMULIR PERBAIKAN SKRIPSI

Nama : Rendy Prasetia One

NIM : 04.12.255

Jurusan : Teknik Elektro S-1

Konsentrasi : Teknik Elektronika

Judul : Perancangan Dan Pembuatan Alat Pendeteksi Warna Bagi Penderita Tuna Netra dan Buta Warna Dengan Output Suara

Hari / Tanggal Ujian Skripsi : Selasa / 29 September 2009

Penguji	Revisi	Paraf
Penguji I	- Kesimpulan Diperbaiki - Sesuaikan Data Pengamatan Dengan Warna yang di Uji - Batasan Masalah 1&2 Tidak Usah	
Penguji II	- Abstrak - Sumber - Istilah Asing Dicetak Miring - Teori LCD - Flow Chart (Simbol)	

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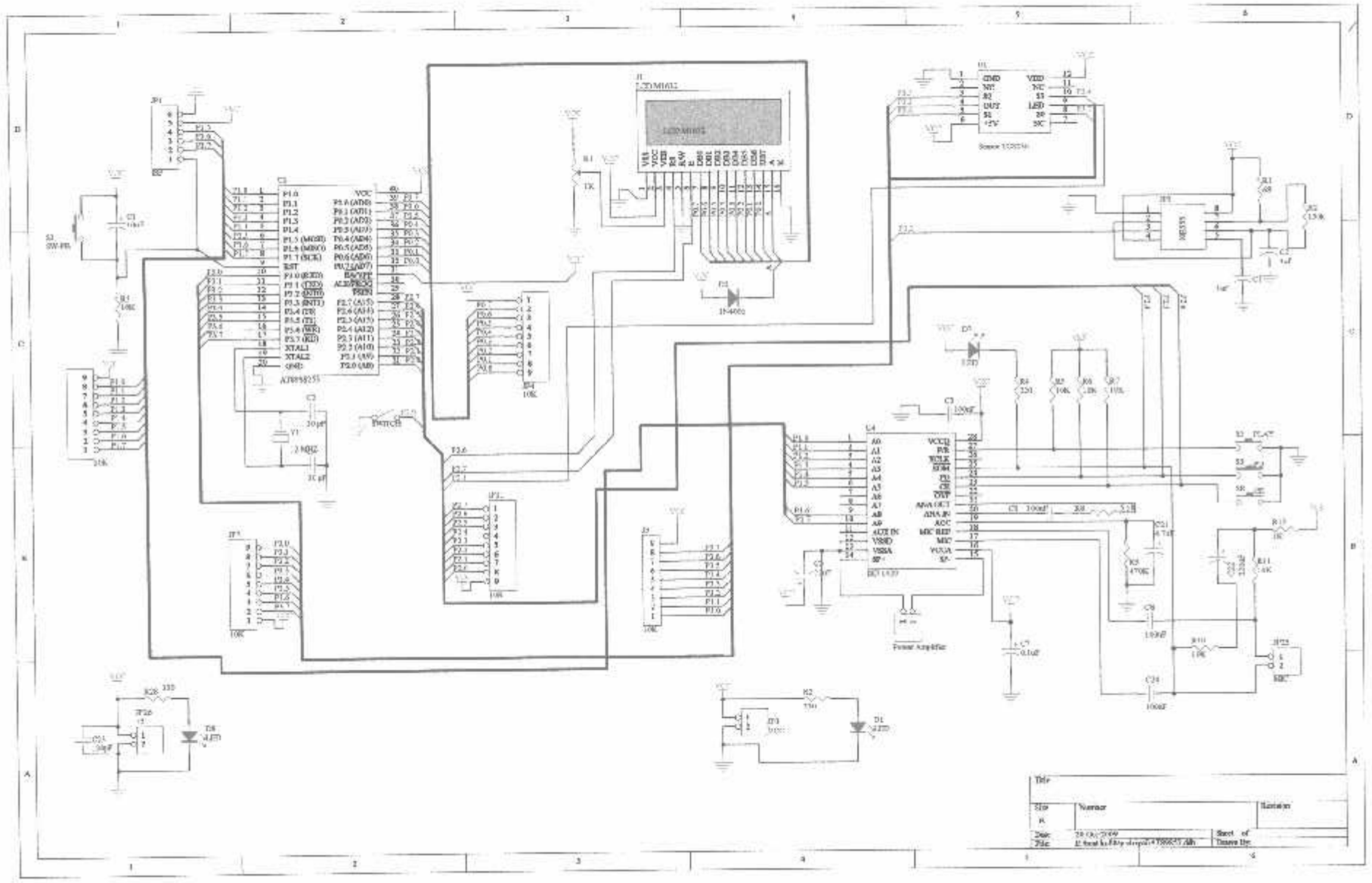
SKEMATIK RANGKAIAN



LISTING PROGRAM

```
Loop

Red:
  Locate 1 , 1
  Lcd "R="
  Lcd R
  Lcd "   "
  Return

Green:
  Locate 1 , 10
  Lcd "G="
  Lcd G
  Lcd "   "
  Return

Blue:
  Locate 2 , 10
  Lcd "B="
  Lcd Bl
  Lcd "   "
  Return

Nt_0:
If C = 0 Then
  Enable Int1
  C = 1
Else
  Disable Int1
  Frek = A
  C = 0
  A = 0
  Incr D
  If D = 1 Then
    R = Frek
    Gosub Red
    S2 = 1
    S3 = 1
  Elseif D = 2 Then
    G = Frek
    Gosub Green
    S2 = 0
    S3 = 1
  Elseif D = 3 Then
    D = 0
    Bl = Frek
    Gosub Blue
    Gosub Warna
```

```
    If P2.0 = 0 Then
      If N2 = N1 Then
        Incr N3
        If N3 = 2 Then
        Locate 2 , 8
        Lcd "s"
        Waitms 500
        Gosub Isd
        Locate 2 , 8
        Lcd " "
        N1 = 0
        N2 = 0
        N3 = 0
        End If
      End If
     End If
    N2 = N1
    S2 = 0
    S3 = 0
  End If

End If
Return

Nt_1:
A = A + 1
Return

Warna:
If R <= 602 And R >= 182 And G >= 15 And G <= 255 And Bl >= 14 And Bl <=
84 Then
  Locate 2 , 1
  Lcd "merah "
  P1 = &H13
  P3.0 = 0
  P3.1 = 0
  N1 = 1
Elseif R <= 868 And R >= 430 And G >= 180 And G <= 359 And Bl >= 86 And
Bl <= 150 Then
  Locate 2 , 1
  Lcd "jingga  "
  P1 = &H1F
  P3.0 = 0
  P3.1 = 0
  N1 = 2
Elseif R <= 386 And R >= 220 And G >= 257 And G <= 420 And Bl >= 90 And
Bl <= 200 Then
  Locate 2 , 1
```

```
  Lcd "kuning  "
  P1 = &H29
  P3.0 = 0
  P3.1 = 0
  N1 = 3
Elseif R <= 126 And R >= 29 And G >= 60 And G <= 305 And Bl >= 166 And Bl
<= 498 Then
  Locate 2 , 1
  Lcd "biru  "
  P1 = &H3E
  P3.0 = 0
  P3.1 = 0
  N1 = 4
Elseif R <= 160 And R >= 42 And G >= 146 And G <= 607 And Bl >= 78 And Bl
<= 235 Then
  Locate 2 , 1
  Lcd "hijau "
  P1 = &H33
  P3.0 = 0
  P3.1 = 0
  N1 = 5
Elseif R <= 200 And R >= 278 And G >= 350 And G <= 710 And Bl >= 500 And
Bl <= 880 Then
  Locate 2 , 1
  Lcd "putih "
  P1 = &H1F
  P3.0 = 1
  P3.1 = 0
  N1 = 6
Elseif R <= 170 And R >= 38 And G >= 35 And G <= 227 And Bl >= 115 And Bl
<= 164 Then
  Locate 2 , 1
  Lcd "ungu "
  P1 = &H08
  P3.0 = 1
  P3.1 = 0
  N1 = 7
Elseif R <= 177 And R >= 80 And G >= 28 And G <= 144 And Bl >= 36 And Bl
<= 110 Then
  Locate 2 , 1
  Lcd "coklat "
  P1 = &H0A
  P3.0 = 0
  P3.1 = 0
  N1 = 8
Elseif R <= 28 And R >= 2 And G >= 2 And G <= 34 And Bl >= 2 And Bl <= 33
Then
  Locate 2 , 1
```

```
  Lcd "hitam  "
  P1 = &H00
  P3.0 = 0
  P3.1 = 0
  N1 = 9
Else
  Locate 2 , 1
  Lcd "erorr  "
  P1 = &H10
  P3.0 = 1
  P3.1 = 0
  N1 = 10
End If
Return

Isd:
Playe = 1
Delay
Playe = 0
Delay
Playe = 1
Bitwait Recled , Set
Wait 2
Return
```

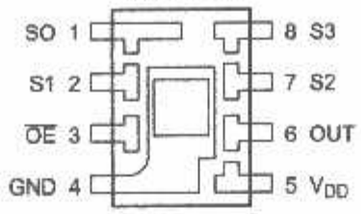
DATA SHEET

TCS230
PROGRAMMABLE
COLOR LIGHT-TO-FREQUENCY CONVERTER

TAOS046 – JANUARY 2003

- High-Resolution Conversion of Light Intensity to Frequency
- Programmable Color and Full-Scale Output Frequency
- Communicates Directly With a Microcontroller
- Single-Supply Operation (2.7 V to 5.5 V)
- Power Down Feature
- Nonlinearity Error Typically 0.2% at 50 kHz
- Stable 200 ppm/°C Temperature Coefficient
- Low-Profile Surface-Mount Package

SOIC PACKAGE
(TOP VIEW)

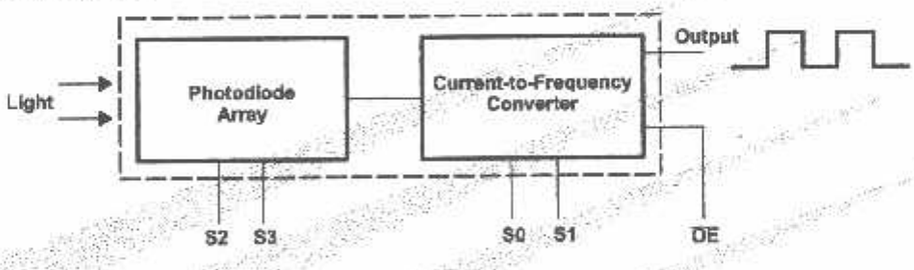


Description

The TCS230 programmable color light-to-frequency converter combines configurable silicon photodiodes and a current-to-frequency converter on single monolithic CMOS integrated circuit. The output is a square wave (50% duty cycle) with frequency directly proportional to light intensity (irradiance). The full-scale output frequency can be scaled by one of three preset values via two control input pins. Digital inputs and digital output allow direct interface to a microcontroller or other logic circuitry. Output enable ($\overline{OE}$) places the output in the high-impedance state for multiple-unit sharing of a microcontroller input line.

The light-to-frequency converter reads an 8 x 8 array of photodiodes. Sixteen photodiodes have blue filters, 16 photodiodes have green filters, 16 photodiodes have red filters, and 16 photodiodes are clear with no filters. The four types (colors) of photodiodes are interdigitated to minimize the effect of non-uniformity of incident irradiance. All 16 photodiodes of the same color are connected in parallel and which type of photodiode the device uses during operation is pin-selectable. Photodiodes are 120 µm x 120 µm in size and are on 144-µm centers.

Functional Block Diagram



Texas Advanced Optoelectronic Solutions Inc.
800 Jupiter Road, Suite 205 • Plano, TX 75074 • (972) 673-0759
www.taosinc.com

Terminal Functions

TERMINAL NAME	TERMINAL NO.	I/O	DESCRIPTION
GND	4		Power supply ground. All voltages are referenced to GND.
$\overline{OE}$	3	I	Enable for f_o (active low).
OUT	6	O	Output frequency (f_o).
S0, S1	1, 2	I	Output frequency scaling selection inputs.
S2, S3	7, 8	I	Photodiode type selection inputs.
V_{DD}	5		Supply voltage

Table 1. Selectable Options

S0	S1	OUTPUT FREQUENCY SCALING (f_o)		S2	S3	PHOTODIODE TYPE
L	L	Power down		L	L	Red
L	H	2%		L	H	Blue
H	L	20%		H	L	Clear (no filter)
H	H	100%		H	H	Green

Available Options

DEVICE	T_A	PACKAGE – LEADS	PACKAGE DESIGNATOR	ORDERING NUMBER
TCS230	–25°C to 85° C	SOIC–8	D	TCS230D

Absolute Maximum Ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage, V_{DD} (see Note 1) . . . . . 6 V
Input voltage range, all inputs, V_I . . . . . –0.3 V to V_{DD} + 0.3 V
Operating free-air temperature range, T_A . . . . . 0°C to 70°C
Storage temperature range . . . . . –25°C to 85°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds . . . . . 260°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: All voltage values are with respect to GND.

Recommended Operating Conditions

		MIN	NOM	MAX	UNIT
Supply voltage, V_{DD}		2.7	5	5.5	V
High-level input voltage, V_{IH}	V_{DD} = 2.7 V to 5.5 V	2		V_{DD}	V
Low-level input voltage, V_{IL}	V_{DD} = 2.7 V to 5.5 V	0		0.8	V
Operating free-air temperature range, T_A		0		70	°C

Electrical Characteristics at T_A = 25°C, V_{DD} = 5 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{OH}	High-level output voltage	I_{OH} = –4 mA	4	4.5		V
V_{OL}	Low-level output voltage	I_{OL} = 4 mA		0.25	0.40	V
I_{IH}	High-level input current				5	µA
I_{IL}	Low-level input current				5	µA
I_{DD}	Supply current	Power-on mode		2	3	mA
		Power-down mode		7	15	µA
	Full-scale frequency (See Note 2)	S0 = H, S1 = H	500	600		kHz
		S0 = H, S1 = L	100	120		kHz
		S0 = L, S1 = H	10	12		kHz
	Temperature coefficient of output frequency	λ < 700 nm, –25°C ≤ T_A ≤ 70°C		+200		ppm/°C
k_{SVS}	Supply voltage sensitivity	V_{DD} = 5 V ±10%		±0.5		%/V

NOTE 2: Full-scale frequency is the maximum operating frequency of the device without saturation.

Operating Characteristics at V_{DD} = 5 V, T_A = 25°C, S0 = H, S1 = H (unless otherwise noted) (See Notes 3, 4, 5, 6, and 7).

PARAMETER		TEST CONDITIONS	CLEAR PHOTODIODE S2 = H, S3 = L			BLUE PHOTODIODE S2 = L, S3 = H			GREEN PHOTODIODE S2 = H, S3 = H			RED PHOTODIODE S2 = L, S3 = L			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
f_O	Output frequency	E_e = 45.6 µW/cm², λ_p = 470 nm	16	20	24	11.2	16.4	21.6							kHz
		E_e = 39.2 µW/cm², λ_p = 524 nm	16	20	24				8	13.6	19.2				kHz
		E_e = 32.8 µW/cm², λ_p = 635 nm	16	20	24							14	19	24	kHz
		E_e = 0		2	12		2	12		2	12		2	12	Hz
R_e	Irradiance responsivity (Note 8)	λ_p = 470 nm		439			360			88			31		Hz/(µW/cm²)
		λ_p = 524 nm		510			189			347			46		
		λ_p = 565 nm		548			49			318			110		
		λ_p = 635 nm		610			30			37			579		
	Saturation Irradiance (Note 9)	λ_p = 470 nm		1370			1670								µW/cm²
		λ_p = 524 nm		1180						1730					
		λ_p = 565 nm		1090						1890					
		λ_p = 635 nm		980									1040		
R_v	Illuminance responsivity (Note 10)	λ_p = 470 nm		585			480			117			41		Hz/lx
		λ_p = 524 nm		98			36			67			9		
		λ_p = 565 nm		92			8			53			18		
		λ_p = 635 nm		407			20			25			386		
	Nonlinearity (Note 11)	f_O = 0 to 5 kHz		±0.1%			±0.1%			±0.1%			±0.1%		% F.S.
		f_O = 0 to 50 kHz		±0.2%			±0.2%			±0.2%			±0.2%		% F.S.
		f_O = 0 to 500 kHz		±0.5%			±0.5%			±0.5%			±0.5%		% F.S.
	Recovery from power down			100			100			100			100		µs
	Response time to output enable (OE)			100			100			100			100		ns

NOTES:
3. Optical measurements are made using small-angle incident radiation from a light-emitting diode (LED) optical source.
4. The 470 nm input irradiance is supplied by an InGaN light-emitting diode with the following characteristics: peak wavelength λ_p = 470 nm, spectral halfwidth $\Delta\lambda_{1/2}$ = 35 nm, and luminous efficacy = 75 lm/W.
5. The 524 nm input irradiance is supplied by an InGaN light-emitting diode with the following characteristics: peak wavelength λ_p = 524 nm, spectral halfwidth $\Delta\lambda_{1/2}$ = 47 nm, and luminous efficacy = 520 lm/W.
6. The 565 nm input irradiance is supplied by a GaP light-emitting diode with the following characteristics: peak wavelength λ_p = 565 nm, spectral halfwidth $\Delta\lambda_{1/2}$ = 28 nm, and luminous efficacy = 595 lm/W.
7. The 635 nm input irradiance is supplied by a AlInGaP light-emitting diode with the following characteristics: peak wavelength λ_p = 635 nm, spectral halfwidth $\Delta\lambda_{1/2}$ = 17 nm, and luminous efficacy = 150 lm/W.
8. Irradiance responsivity R_e is characterized over the range from zero to 5 kHz.
9. Saturation irradiance = (full-scale frequency)/(irradiance responsivity).
10. Illuminance responsivity Rv is calculated from the irradiance responsivity by using the LED luminous efficacy values stated in notes 4, 5, and 6 and using 1 lx = 1 lm/m².
11. Nonlinearity is defined as the deviation of f_O from a straight line between zero and full scale, expressed as a percent of full scale.

TYPICAL CHARACTERISTICS

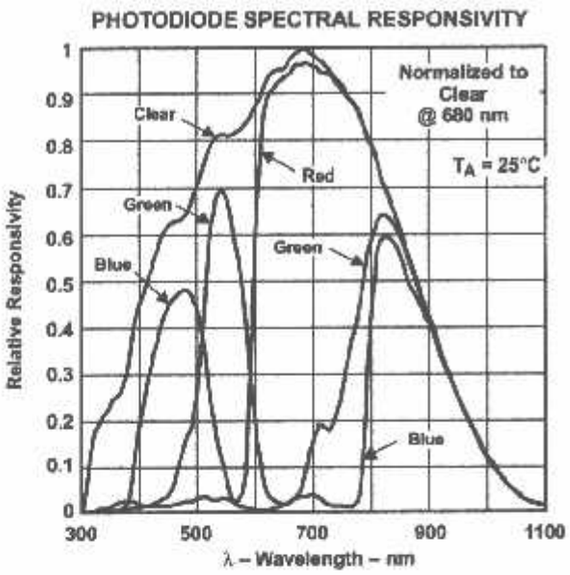


Figure 1

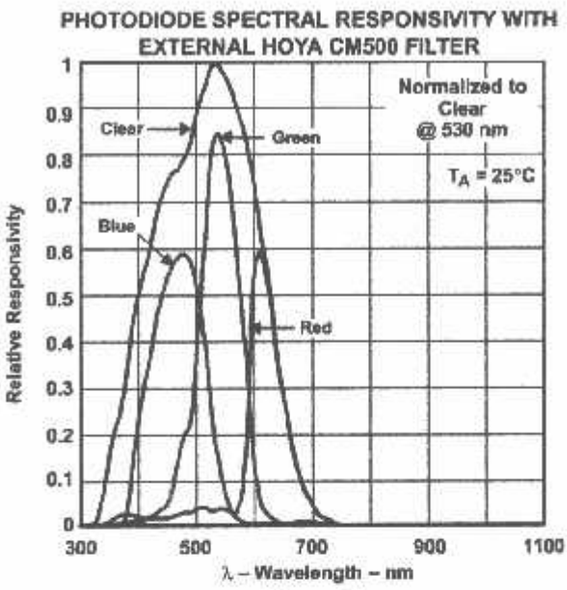


Figure 2

APPLICATION INFORMATION

Power supply considerations

Power-supply lines must be decoupled by a 0.01-µF to 0.1-µF capacitor with short leads mounted close to the device package.

Input interface

A low-impedance electrical connection between the device $\overline{OE}$ pin and the device GND pin is required for improved noise immunity.

Output interface

The output of the device is designed to drive a standard TTL or CMOS logic input over short distances. If lines greater than 12 inches are used on the output, a buffer or line driver is recommended.

Photodiode type (color) selection

The type of photodiode (blue, green, red, or clear) used by the device is controlled by two logic inputs, S2 and S3 (see Table 1).

Output frequency scaling

Output-frequency scaling is controlled by two logic inputs, S0 and S1. The internal light-to-frequency converter generates a fixed-pulsewidth pulse train. Scaling is accomplished by internally connecting the pulse-train output of the converter to a series of frequency dividers. Divided outputs are 50%-duty cycle square waves with relative frequency values of 100%, 20%, and 2%. Because division of the output frequency is accomplished by counting pulses of the principal internal frequency, the final-output period represents an average of the multiple periods of the principle frequency.

The output-scaling counter registers are cleared upon the next pulse of the principal frequency after any transition of the S0, S1, S2, S3, and $\overline{OE}$ lines. The output goes high upon the next subsequent pulse of the principal frequency, beginning a new valid period. This minimizes the time delay between a change on the input lines and the resulting new output period. The response time to an input programming change or to an irradiance step change is one period of new frequency plus 1 µS. The scaled output changes both the full–scale frequency and the dark frequency by the selected scale factor.

The frequency-scaling function allows the output range to be optimized for a variety of measurement techniques. The scaled-down outputs may be used where only a slower frequency counter is available, such as low-cost microcontroller, or where period measurement techniques are used.

Measuring the frequency

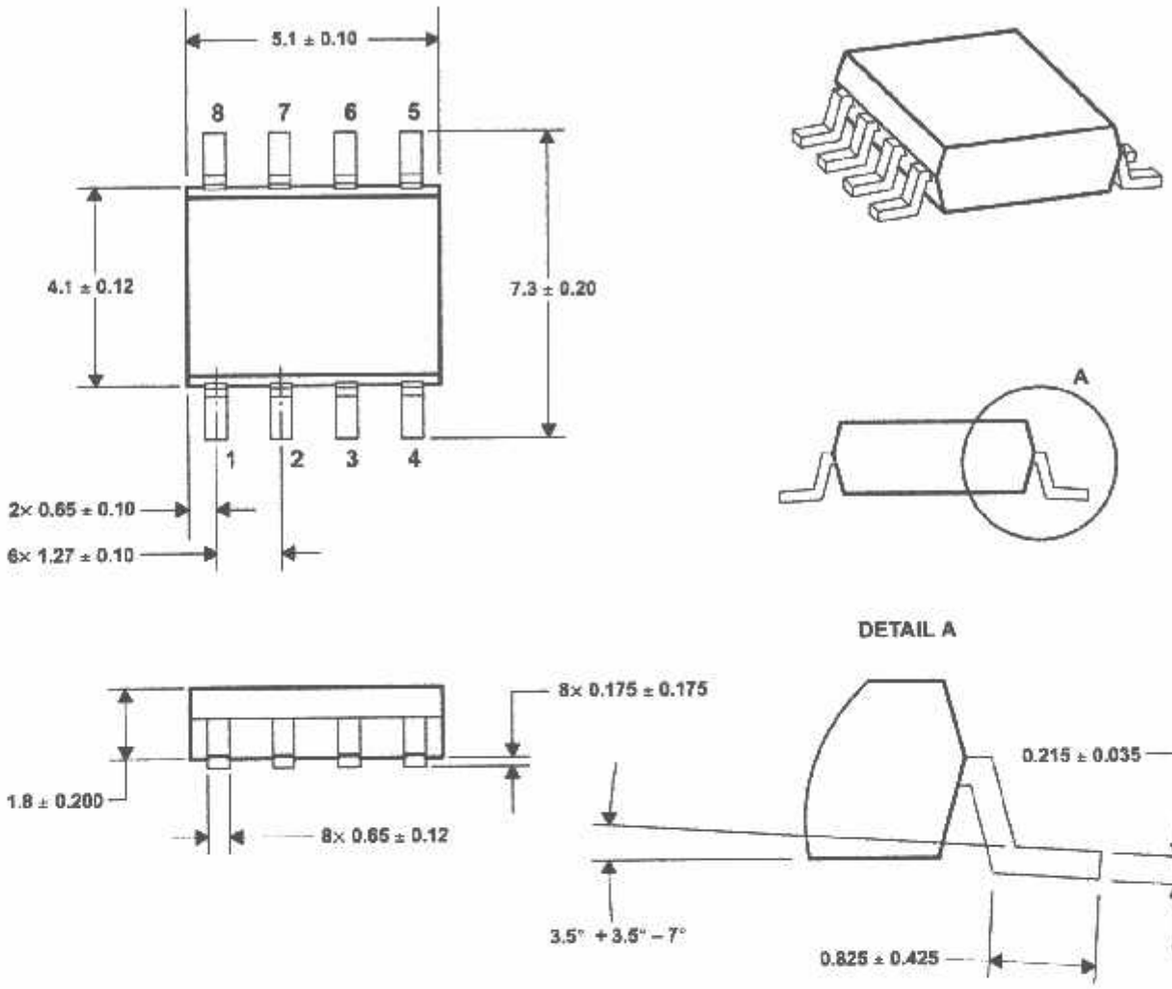
The choice of interface and measurement technique depends on the desired resolution and data acquisition rate. For maximum data-acquisition rate, period-measurement techniques are used.

Output data can be collected at a rate of twice the output frequency or one data point every microsecond for full-scale output. Period measurement requires the use of a fast reference clock with available resolution directly related to reference clock rate. Output scaling can be used to increase the resolution for a given clock rate or to maximize resolution as the light input changes. Period measurement is used to measure rapidly varying light levels or to make a very fast measurement of a constant light source.

Maximum resolution and accuracy may be obtained using frequency-measurement, pulse-accumulation, or integration techniques. Frequency measurements provide the added benefit of averaging out random- or high-frequency variations (jitter) resulting from noise in the light signal. Resolution is limited mainly by available counter registers and allowable measurement time. Frequency measurement is well suited for slowly varying or constant light levels and for reading average light levels over short periods of time. Integration (the accumulation of pulses over a very long period of time) can be used to measure exposure, the amount of light present in an area over a given time period.

MECHANICAL INFORMATION

PACKAGE D **PLASTIC SMALL-OUTLINE PACKAGE**



NOTES: A. All linear dimensions are in millimeters.
B. Package is molded with an electrically nonconductive clear plastic compound having an index of refraction of 1.55.
C. Actual product will vary within the mechanical tolerances shown on this specification. Designs for use of this product MUST allow for the data sheet tolerances.
D. Pin 4 (GND) is mechanically connected to the die mount pad.
E. The 8 × 8 photodiode array area is 1.15 mm × 1.15 mm (1.33 sq. mm).
F. This drawing is subject to change without notice.

Figure 3. TCS230 Mechanical Specifications

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Features

- Compatible with MCS®-51 Products
- 12K Bytes of In-System Programmable (ISP) Flash Program Memory
  - SPI Serial Interface for Program Downloading
  - Endurance: 10,000 Write/Erase Cycles
- 2K Bytes EEPROM Data Memory
  - Endurance: 100,000 Write/Erase Cycles
- 64-byte User Signature Array
- 2.7V to 5.5V Operating Range
- Fully Static Operation: 0 Hz to 24 MHz
- Three-level Program Memory Lock
- 256 x 8-bit Internal RAM
- 32 Programmable I/O Lines
- Three 16-bit Timer/Counters
- Nine Interrupt Sources
- Enhanced UART Serial Port with Framing Error Detection and Automatic Address Recognition
- Enhanced SPI (Double Write/Read Buffered) Serial Interface
- Low-power Idle and Power-down Modes
- Interrupt Recovery from Power-down Mode
- Programmable Watchdog Timer
- Dual Data Pointer
- Power-off Flag
- Flexible ISP Programming (Byte and Page Modes)
  - Page Mode: 64 Bytes/Page for Code Memory, 32 Bytes/Page for Data Memory
- Four-level Enhanced Interrupt Controller
- Programmable and Fuseable x2 Clock Option
- Internal Power-on Reset
- 42-pin PDIP Package Option for Reduced EMC Emission
- Green (Pb/Halide-free) Packaging Option

1. Description

The AT89S8253 is a low-power, high-performance CMOS 8-bit microcontroller with 12K bytes of In-System Programmable (ISP) Flash program memory and 2K bytes of EEPROM data memory. The device is manufactured using Atmel's high-density nonvolatile memory technology and is compatible with the industry-standard MCS-51 instruction set and pinout. The on-chip downloadable Flash allows the program memory to be reprogrammed in-system through an SPI serial interface or by a conventional nonvolatile memory programmer. By combining a versatile 8-bit CPU with downloadable Flash on a monolithic chip, the Atmel AT89S8253 is a powerful microcontroller which provides a highly-flexible and cost-effective solution to many embedded control applications.

8-bit Microcontroller with 12K Bytes Flash and 2K Bytes EEPROM

AT89S8253

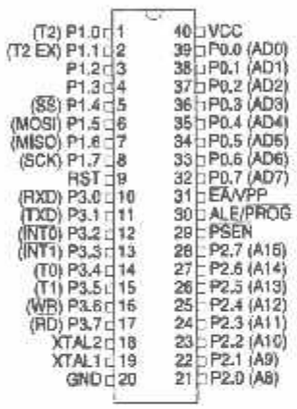
3286J–MICRO–12/05

The AT89S8253 provides the following standard features: 12K bytes of In-System Programmable Flash, 2K bytes of EEPROM, 256 bytes of RAM, 32 I/O lines, programmable watchdog timer, two data pointers, three 16-bit timer/counters, a six-vector, four-level interrupt architecture, a full duplex serial port, on-chip oscillator, and clock circuitry. In addition, the AT89S8253 is designed with static logic for operation down to zero frequency and supports two software selectable power saving modes. The Idle Mode stops the CPU while allowing the RAM, timer/counters, serial port, and interrupt system to continue functioning. The Power-down mode saves the RAM contents but freezes the oscillator, disabling all other chip functions until the next external interrupt or hardware reset.

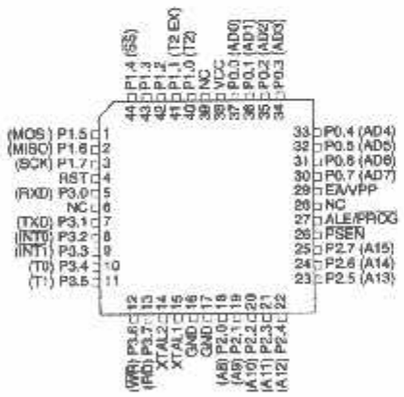
The on-board Flash/EEPROM is accessible through the SPI serial interface. Holding RESET active forces the SPI bus into a serial programming interface and allows the program memory to be written to or read from, unless one or more lock bits have been activated.

2. Pin Configurations

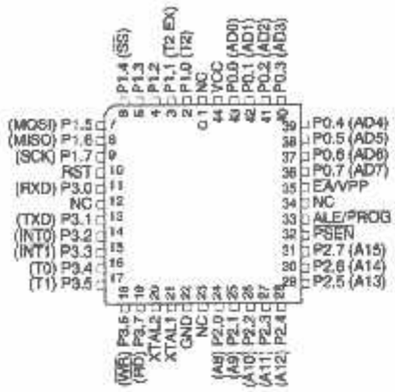
2.1 40P6 – 40-lead PDIP



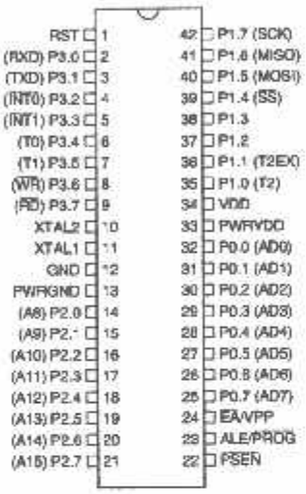
2.2 44A – 44-lead TQFP



2.3 44J – 44-lead PLCC



2.4 42PS6 – PDIP



3. Pin Description

3.1 VCC

Supply voltage (all packages except 42-PDIP).

3.2 GND

Ground (all packages except 42-PDIP; for 42-PDIP GND connects only the logic core and the embedded program/data memories).

3.3 VDD

Supply voltage for the 42-PDIP which connects only the logic core and the embedded program/data memories.

3.4 PWRVDD

Supply voltage for the 42-PDIP which connects only the I/O Pad Drivers.

The application board **must** connect both VDD and PWRVDD to the board supply voltage.

3.5 PWRGND

Ground for the 42-PDIP which connects only the I/O Pad Drivers. PWRGND and GND are weakly connected through the common silicon substrate, but not through any metal links. The application board **must** connect both GND and PWRGND to the board ground.

3.6 Port 0

Port 0 is an 8-bit open drain bi-directional I/O port. As an output port, each pin can sink six TTL inputs. When 1s are written to port 0 pins, the pins can be used as high-impedance inputs.

Port 0 can also be configured to be the multiplexed low-order address/data bus during accesses to external program and data memory. In this mode, P0 has internal pull-ups.

Port 0 also receives the code bytes during Flash programming and outputs the code bytes during program verification. **External pull-ups are required during program verification.**

3.7 Port 1

Port 1 is an 8-bit bi-directional I/O port with internal pull-ups. The Port 1 output buffers can sink/source six TTL inputs. When 1s are written to Port 1 pins, they are pulled high by the weak internal pull-ups and can be used as inputs. As inputs, Port 1 pins that are externally being pulled low will source current (I_{IL}, 150 µA typical) because of the weak internal pull-ups.

Some Port 1 pins provide additional functions. P1.0 and P1.1 can be configured to be the timer/counter 2 external count input (P1.0/T2) and the timer/counter 2 trigger input (P1.1/T2EX), respectively.

Furthermore, P1.4, P1.5, P1.6, and P1.7 can be configured as the SPI slave port select, data input/output and shift clock input/output pins as shown in the following table.

Port Pin	Alternate Functions
P1.0	T2 (external count input to Timer/Counter 2), clock-out
P1.1	T2EX (Timer/Counter 2 capture/reload trigger and direction control)
P1.4	$\overline{SS}$ (Slave port select input)
P1.5	MOSI (Master data output, slave data input pin for SPI channel)
P1.6	MISO (Master data input, slave data output pin for SPI channel)
P1.7	SCK (Master clock output, slave clock input pin for SPI channel)

Port 1 also receives the low-order address bytes during Flash programming and verification.

3.8 Port 2

Port 2 is an 8-bit bi-directional I/O port with internal pull-ups. The Port 2 output buffers can sink/source six TTL inputs. When 1s are written to Port 2 pins, they are pulled high by the weak internal pull-ups and can be used as inputs. As inputs, Port 2 pins that are externally being pulled low will source current (I_{IL}, 150 µA typical) because of the weak internal pull-ups.

Port 2 emits the high-order address byte during fetches from external program memory and during accesses to external data memory that use 16-bit addresses (MOVX @ DPTR). In this application, Port 2 uses strong internal pull-ups when emitting 1s. During accesses to external data memory that use 8-bit addresses (MOVX @ RI), Port 2 emits the contents of the P2 Special Function Register.

Port 2 also receives the high-order address bits and some control signals during Flash programming and verification.

3.9 Port 3

Port 3 is an 8-bit bi-directional I/O port with internal pull-ups. The Port 3 output buffers can sink/source six TTL inputs. When 1s are written to Port 3 pins, they are pulled high by the weak internal pull-ups and can be used as inputs. As inputs, Port 3 pins that are externally being pulled low will source current (I_{IL},150 µA typical) because of the weak internal pull-ups.

Port 3 receives some control signals for Flash programming and verification.

Port 3 also serves the functions of various special features of the AT89S8253, as shown in the following table.

Port Pin	Alternate Functions
P3.0	RXD (serial input port)
P3.1	TXD (serial output port)
P3.2	$\overline{INT0}$ (external interrupt 0)[1]
P3.3	$\overline{INT1}$ (external interrupt 1)[1]
P3.4	T0 (timer 0 external input)
P3.5	T1 (timer 1 external input)
P3.6	$\overline{WR}$ (external data memory write strobe)
P3.7	$\overline{RD}$ (external data memory read strobe)

Note: 1. All pins in ports 1 and 2 and almost all pins in port 3 (the exceptions are P3.2 $\overline{INT0}$ and P3.3 $\overline{INT1}$) have their inputs disabled in the Power-down mode. Port pins P3.2 ($\overline{INT0}$) and P3.3 ($\overline{INT1}$) are active even in Power-down mode (to be able to sense an interrupt request to exit the Power-down mode) and as such still have their weak internal pull-ups turned on.

3.10 RST

Reset input. A high on this pin for at least two machine cycles while the oscillator is running resets the device.

3.11 ALE/$\overline{PROG}$

Address Latch Enable. ALE/$\overline{PROG}$ is an output pulse for latching the low byte of the address (on its falling edge) during accesses to external memory. This pin is also the program pulse input ($\overline{PROG}$) during Flash programming.

In normal operation, ALE is emitted at a constant rate of 1/6 the oscillator frequency and may be used for external timing or clocking purposes. Note, however, that one ALE pulse is skipped during each access to external data memory.

If desired, ALE operation can be disabled by setting bit 0 of the AUXR SFR at location 8EH. With the bit set, ALE is active only during a MOVX or MOVC instruction. Otherwise, the pin is weakly pulled high. Setting the ALE-disable bit has no effect if the microcontroller is in external execution mode.

3.12 $\overline{PSEN}$

Program Store Enable. $\overline{PSEN}$ is the read strobe to external program memory (active low).

When the AT89S8253 is executing code from external program memory, $\overline{PSEN}$ is activated twice each machine cycle, except that two $\overline{PSEN}$ activations are skipped during each access to external data memory.

3.13 $\overline{EA}$/VPP

External Access Enable. $\overline{EA}$ must be strapped to GND in order to enable the device to fetch code from external program memory locations starting at 0000H up to FFFFH. Note, however, that if lock bit 1 is programmed, $\overline{EA}$ will be internally latched on reset.

$\overline{EA}$ should be strapped to V_{CC} for internal program executions. This pin also receives the 12-volt programming enable voltage (V_{PP}) during Flash programming when 12-volt programming is selected.

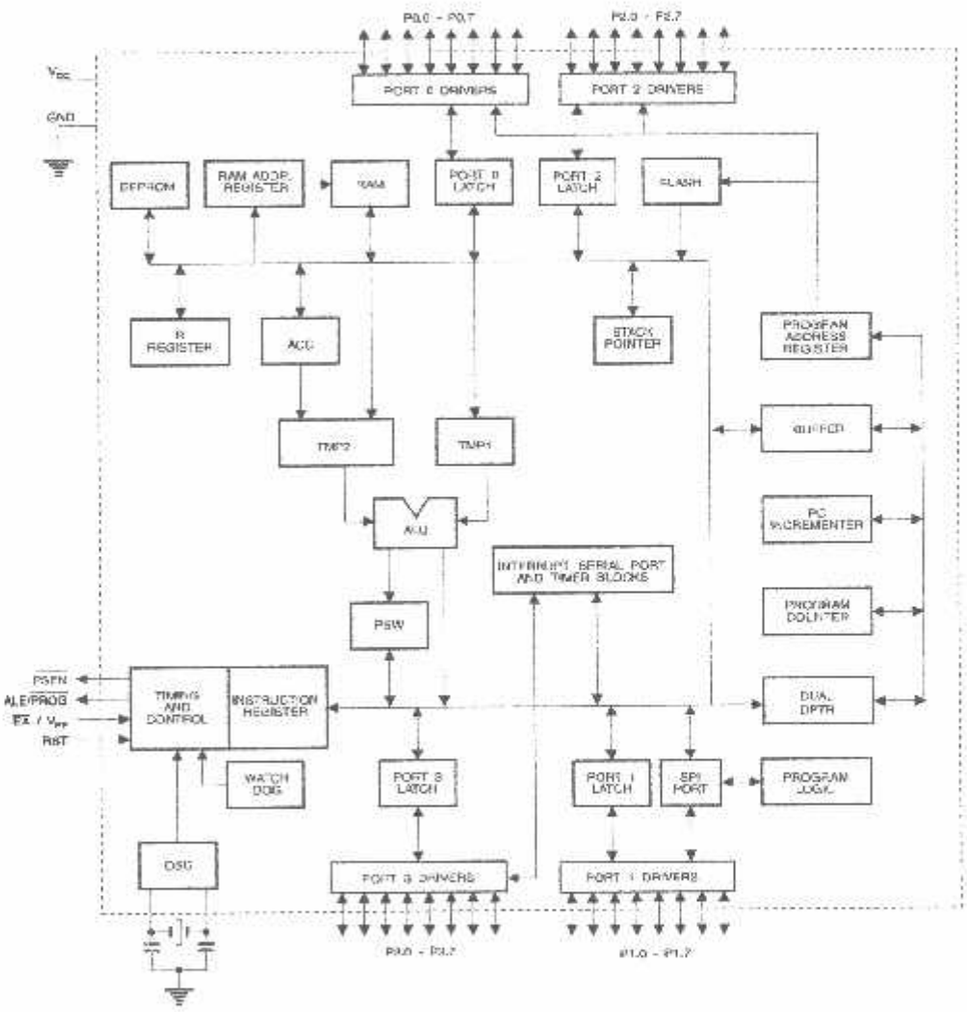
3.14 XTAL1

Input to the inverting oscillator amplifier and input to the internal clock operating circuit.

3.15 XTAL2

Output from the inverting oscillator amplifier.

4. Block Diagram



5. Special Function Registers

A map of the on-chip memory area called the Special Function Register (SFR) space is shown in Table 5-1.

Note that not all of the addresses are occupied, and unoccupied addresses may not be implemented on the chip. Read accesses to these addresses will generally return random data, and write accesses will have an indeterminate effect.

User software should not write 1s to these unlisted locations, since they may be used in future products to invoke new features. In that case, the reset or inactive values of the new bits will always be 0.

Table 5-1. AT89S8253 SFR Map and Reset Values

0F8H									0FFH
0F0H	B 00000000								0F7H
0E8H									0EFH
0E0H	ACC 00000000								0E7H
0D8H									0DFH
0D0H	PSW 00000000					SPCR 00000100			0D7H
0C8H	T2CON 00000000	T2MOD XXXXXX00	RCAP2L 00000000	RCAP2H 00000000	TL2 00000000	TH2 00000000			0CFH
0C0H									0C7H
0B8H	IP XX000000	SADEN 00000000							0BFH
0B0H	P3 11111111							IPH XX000000	0B7H
0A8H	IE 0X000000	SADDR 00000000	SPSR 00XXXX00						0AFH
0A0H	P2 11111111						WDTRST (Write Only)	WDTCON 0000 0000	0A7H
98H	SCON 00000000	SBUF XXXXXXXX							9FH
90H	P1 11111111						EECON XX000011		97H
88H	TCON 00000000	TMOD 00000000	TL0 00000000	TL1 00000000	TH0 00000000	TH1 00000000	AUXR XXXXXXX0	CLKREG XXXXXXX0	8FH
80H	P0 11111111	SP 00000111	DP0L 00000000	DP0H 00000000	DP1L 00000000	DP1H 00000000	SPDR ########	PCON 00XX0000	87H

Note: # means: 0 after cold reset and unchanged after warm reset.

5.1 Auxiliary Register

The AUXR Register contains a single active bit called DISALE.

Table 5-2. AUXR – Auxiliary Register

AUXR Address = 8EH — Reset Value = XXXX XXX0B

Not Bit Addressable

	–	–	–	–	–	–	Intel_Pwd_Exit	DISALE
Bit	7	6	5	4	3	2	1	0

Symbol	Function
DISALE	When DISALE = 0, ALE is emitted at a constant rate of 1/6 the oscillator frequency (except during MOVX when 1 ALE pulse is missing). When DISALE = 1, ALE is active only during a MOVX or MOVC instruction.
Intel_Pwd_Exit	When set, this bit configures the Interrupt driven exit from power-down to resume execution on the rising edge of the interrupt signal. When this bit is cleared, the execution resumes after a self-timed interval (nominal 2 ms) referenced from the falling edge of the interrupt signal.

5.2 Clock Register

The CLKREG register contains a single active bit called X2.

Table 5-3. CLKREG – Clock Register

CLKREG Address = 8FH — Reset Value = XXXX XXX0B

Not Bit Addressable

	–	–	–	–	–	–	–	X2
Bit	7	6	5	4	3	2	1	0

Symbol	Function
X2	When X2 = 0, the oscillator frequency (at XTAL1 pin) is internally divided by 2 before it is used as the device system frequency. When X2 = 1, the divider by 2 is no longer used and the XTAL1 frequency becomes the device system frequency. This enables the user to choose a 6 MHz crystal instead of a 12 MHz crystal, for example, in order to reduce EMI.

5.3 SPI Registers

Control and status bits for the Serial Peripheral Interface are contained in registers SPCR (see Table 14-1 on page 25) and SPSR (see Table 14-2 on page 26). The SPI data bits are contained in the SPDR register. In normal SPI mode, writing the SPI data register during serial data transfer sets the Write Collision bit (WCOL) in the SPSR register. In enhanced SPI mode, the SPDR is also write double-buffered because WCOL works as a Write Buffer Full Flag instead of being a collision flag. The values in SPDR are not changed by Reset.

5.4 Interrupt Registers

The global interrupt enable bit and the individual interrupt enable bits are in the IE register. In addition, the individual interrupt enable bit for the SPI is in the SPCR register. Four priorities can be set for each of the six interrupt sources in the IP and IPH registers.

IPH bits have the same functions as IP bits, except IPH has higher priority than IP. By using IPH in conjunction with IP, a priority level of 0, 1, 2, or 3 may be set for each interrupt.

5.5 Dual Data Pointer Registers

To facilitate accessing both internal EEPROM and external data memory, two banks of 16-bit Data Pointer Registers are provided: DP0 at SFR address locations 82H - 83H and DP1 at 84H - 85H. Bit DPS = 0 in SFR EECON selects DP0 and DPS = 1 selects DP1. The user should ALWAYS initialize the DPS bit to the appropriate value before accessing the respective Data Pointer Register.

5.6 Power Off Flag

The Power Off Flag (POF), located at bit_4 (PCON.4) in the PCON SFR. POF, is set to "1" during power up. It can be set and reset under software control and is not affected by RESET.

6. Data Memory – EEPROM and RAM

The AT89S8253 implements 2K bytes of on-chip EEPROM for data storage and 256 bytes of RAM. The upper 128 bytes of RAM occupy a parallel space to the Special Function Registers. That means the upper 128 bytes have the same addresses as the SFR space but are physically separate from SFR space.

When an instruction accesses an internal location above address 7FH, the address mode used in the instruction specifies whether the CPU accesses the upper 128 bytes of RAM or the SFR space. Instructions that use direct addressing access the SFR space.

For example, the following direct addressing instruction accesses the SFR at location 0A0H (which is P2).

```
MOV 0A0H, #data
```

Instructions that use indirect addressing access the upper 128 bytes of RAM. For example, the following indirect addressing instruction, where R0 contains 0A0H, accesses the data byte at address 0A0H, rather than P2 (whose address is 0A0H).

```
MOV @R0, #data
```

Note that stack operations are examples of indirect addressing, so the upper 128 bytes of data RAM are available as stack space.

The on-chip EEPROM data memory is selected by setting the EEMEN bit in the EECON register at SFR address location 96H. The EEPROM address range is from 000H to 7FFH. MOVX instructions are used to access the EEPROM. To access off-chip data memory with the MOVX instructions, the EEMEN bit needs to be set to "0".

During program execution mode (using the MOVX instruction) there is an auto-erase capability at the byte level. This means that the user can update or modify a single EEPROM byte location in real-time without affecting any other bytes.

The EEMWE bit in the EECON register needs to be set to "1" before any byte location in the EEPROM can be written. User software should reset EEMWE bit to "0" if no further EEPROM write is required. EEPROM write cycles in the serial programming mode are self-timed and typically take 4 ms. The progress of EEPROM write can be monitored by reading the RDY/$\overline{BSY}$ bit (read-only) in SFR EECON. RDY/$\overline{BSY}$ = 0 means programming is still in progress and RDY/$\overline{BSY}$ = 1 means an EEPROM write cycle is completed and another write cycle can be initiated. Bit EELD in EECON controls whether the next MOVX instruction will only load the write buffer of the EEPROM or will actually start the programming cycle. By setting EELD, only load will occur. Before the last MOVX in a given page of 32 bytes, EELD should be cleared so that after the last MOVX the entire page will be programmed at the same time. This way, 32 bytes will only require 4 ms of programming time instead of 128 ms required in single byte programming.

In addition, during EEPROM programming, an attempted read from the EEPROM will fetch the byte being written with the MSB complemented. Once the write cycle is completed, true data are valid at all bit locations.

6.1 Memory Control Register

The EECON register contains control bits for the 2K bytes of on-chip data EEPROM. It also contains the control bit for the dual data pointer.

Table 6-1. EECON – Data EEPROM Control Register

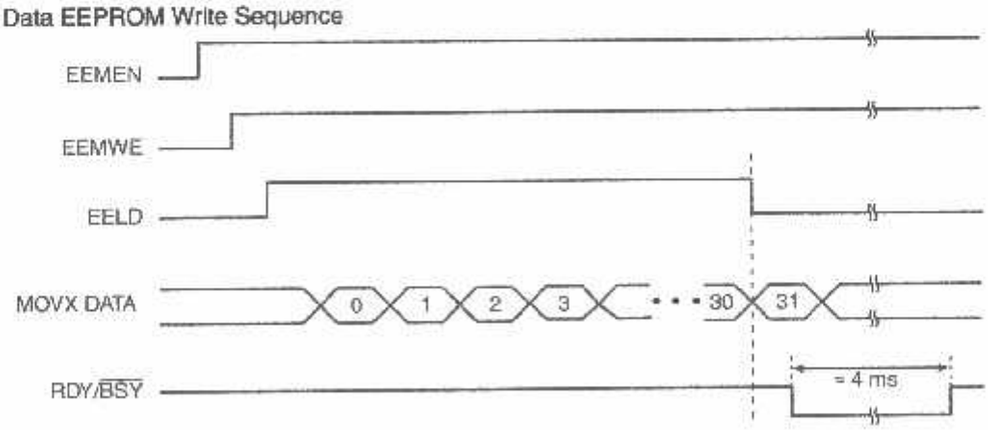
EECON Address = 96H — Reset Value = XX00 0011B

Not Bit Addressable

Bit	–	–	EELD	EEMWE	EEMEN	DPS	RDY/$\overline{BSY}$	$\overline{WRTINH}$
	7	6	5	4	3	2	1	0

Symbol	Function
EELD	EEPROM data memory load enable bit. Used to implement Page Mode Write. A MOVX instruction writing into the data EEPROM will not initiate the programming cycle if this bit is set, rather it will just load data into the volatile data buffer of the data EEPROM memory. Before the last MOVX, reset this bit and the data EEPROM will program all the bytes previously loaded on the same page of the address given by the last MOVX instruction.
EEMWE	EEPROM data memory write enable bit. Set this bit to 1 before initiating byte write to on-chip EEPROM with the MOVX instruction. User software should set this bit to 0 after EEPROM write is completed.
EEMEN	Internal EEPROM access enable. When EEMEN = 1, the MOVX instruction with DPTR will access on-chip EEPROM instead of external data memory if the address used is less than 2K. When EEMEN = 0 or the address used is ≥ 2K, MOVX with DPTR accesses external data memory.
DPS	Data pointer register select. DPS = 0 selects the first bank of data pointer register, DP0, and DPS = 1 selects the second bank, DP1.
RDY/$\overline{BSY}$	RDY/$\overline{BSY}$ (Ready/$\overline{Busy}$) flag for the data EEPROM memory. This is a read-only bit which is cleared by hardware during the programming cycle of the on-chip EEPROM. It is also set by hardware when the programming is completed. Note that RDY/$\overline{BSY}$ will be cleared long after the completion of the MOVX instruction which has initiated the programming cycle.
$\overline{WRTINH}$	$\overline{WRTINH}$ (Write Inhibit) is a READ-ONLY bit which is cleared by hardware when V_{CC} is too low for the programming cycle of the on-chip EEPROM to be executed. When this bit is cleared, an ongoing programming cycle will be aborted or a new programming cycle will not start.

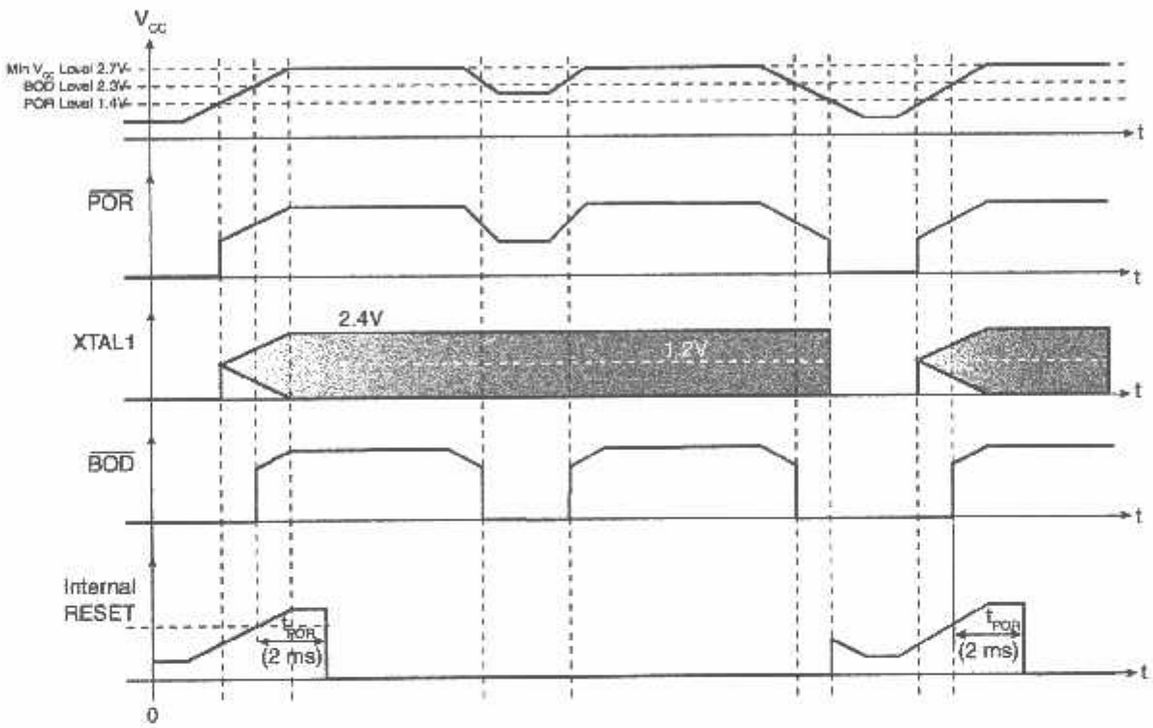
Figure 6-1. Data EEPROM Write Sequence



7. Power-On Reset

A Power-On Reset (POR) is generated by an on-chip detection circuit. The detection level is nominally 1.4V. The POR is activated whenever V_{CC} is below the detection level. The POR circuit can be used to trigger the start-up reset or to detect a supply voltage failure in devices without a brown-out detector. The POR circuit ensures that the device is reset from power-on. When V_{CC} reaches the Power-on Reset threshold voltage, the POR delay counter determines how long the device is kept in POR after V_{CC} rise, nominally 2 ms. The POR signal is activated again, without any delay, when V_{CC} falls below the POR threshold level. A Power-On Reset (i.e. a cold reset) will set the POF flag in PCON.

Figure 7-1. Power-up and Brown-out Detection Sequence



7.1 Brown-out Reset

The AT89S8253 has an on-chip Brown-out Detection (BOD) circuit for monitoring the V_{CC} level during operation by comparing it to a fixed trigger level of 2.4V (max). The trigger level for the BOD is nominally 2.2V. The purpose of the BOD is to ensure that if V_{CC} fails or dips while executing at speed, the system will gracefully enter reset without the possibility of errors induced by incorrect execution. When V_{CC} decreases to a value below the trigger level, the Brown-out Reset is immediately activated. When V_{CC} increases above the trigger level, the BOD delay counter starts the MCU after the timeout period has expired in approximately 2 ms.

8. Programmable Watchdog Timer

The programmable Watchdog Timer (WDT) counts instruction cycles. The prescaler bits, PS0, PS1 and PS2 in SFR WDTCON are used to set the period of the Watchdog Timer from 16K to 2048K instruction cycles. The available timer periods are shown in Table 8-1. The WDT time-out period is dependent upon the external clock frequency.

The WDT is disabled by Power-on Reset and during Power-down mode. When WDT times out without being serviced or disabled, an internal RST pulse is generated to reset the CPU. See Table 8-1 for the WDT period selections.

Table 8-1. Watchdog Timer Time-out Period Selection

WDT Prescaler Bits			Period (Nominal for F_{CLK} = 12 MHz)
PS2	PS1	PS0	
0	0	0	16 ms
0	0	1	32 ms
0	1	0	64 ms
0	1	1	128 ms
1	0	0	256 ms
1	0	1	512 ms
1	1	0	1024 ms
1	1	1	2048 ms

8.1 Watchdog Control Register

The WDTCON register contains control bits for the Watchdog Timer (shown in Table 8-2).

Table 8-2. WDTCON – Watchdog Control Register

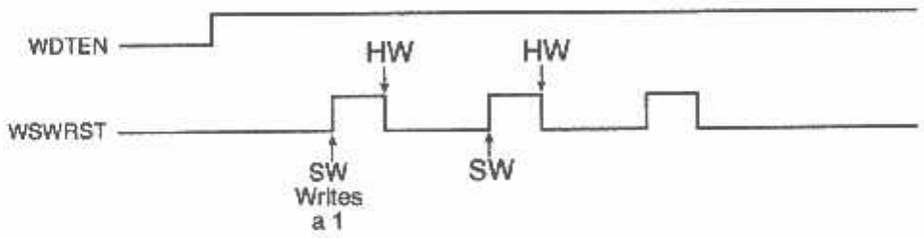
WDTCON Address = A7H — Reset Value = 0000 0000B

Not Bit Addressable

	PS2	PS1	PS0	WDIDLE	DISRTO	HWDT	WSWRST	WDTEN
Bit	7	6	5	4	3	2	1	0

Symbol	Function
PS2 PS1 PS0	Prescaler bits for the watchdog timer (WDT). When all three bits are cleared to 0, the watchdog timer has a nominal period of 16K machine cycles, (i.e. 16 ms at a XTAL frequency of 12 MHz in normal mode or 6 MHz in x2 mode). When all three bits are set to 1, the nominal period is 2048K machine cycles, (i.e. 2048 ms at 12 MHz clock frequency in normal mode or 6 MHz in x2 mode).
WDIDLE	Enable/disable the Watchdog Timer in IDLE mode. When WDIDLE = 0, WDT continues to count in IDLE mode. When WDIDLE = 1, WDT freezes while the device is in IDLE mode.
DISRTO	Enable/disable the WDT-driven Reset Out (WDT drives the RST pin). When DISRTO = 0, the RST pin is driven high after WDT times out and the entire board is reset. When DISRTO = 1, the RST pin remains only as an input and the WDT resets only the microcontroller internally after WDT times out.
HWDT	Hardware mode select for the WDT. When HWDT = 0, the WDT can be turned on/off by simply setting or clearing WDTEN in the same register (this is the software mode for WDT). When HWDT = 1, the WDT has to be set by writing the sequence 1EH/E1H to the WDTRST register (with address 0A6H) and after being set in this way, WDT cannot be turned off except by reset, warm or cold (this is the hardware mode for WDT). To prevent the hardware WDT from resetting the entire device, the same sequence 1EH/E1H must be written to the same WDTRST SFR before the timeout interval.
WSWRST	Watchdog software reset bit. If HWDT = 0 (i.e. WDT is in software controlled mode), when set by software, this bit resets WDT. After being set by software, WSWRST is reset by hardware during the next machine cycle. If HWDT = 1, this bit has no effect, and if set by software, it will not be cleared by hardware.
WDTEN	Watchdog software enable bit. When HWDT = 0 (i.e. WDT is in software-controlled mode), this bit enables WDT when set to 1 and disables WDT when cleared to 0 (it does not reset WDT in this case, but just freezes the existing counter state). If HWDT = 1, this bit is READ-ONLY and reflects the status of the WDT (whether it is running or not).

Figure 8-1. Software Mode – Watchdog Timer Sequence



9. Timer 0 and 1

Timer 0 and Timer 1 in the AT89S8253 operate the same way as Timer 0 and Timer 1 in the AT89S51 and AT89S52. For more detailed information on the Timer/Counter operation, please click on the document link below:

http://www.atmel.com/dyn/resources/prod_documents/DOC4316.PDF

10. Timer 2

Timer 2 is a 16-bit Timer/Counter that can operate as either a timer or an event counter. The type of operation is selected by bit C/$\overline{T2}$ in the SFR T2CON (see Table 10-2 on page 15). Timer 2 has three operating modes: capture, auto-reload (up or down counting), and baud rate generator. The modes are selected by bits in T2CON, as shown in Table 10-2.

Timer 2 consists of two 8-bit registers, TH2 and TL2. In the Timer function, the TL2 register is incremented every machine cycle. Since a machine cycle consists of 12 oscillator periods, the count rate is 1/12 of the oscillator frequency.

In the Counter function, the register is incremented in response to a 1-to-0 transition at its corresponding external input pin, T2. In this function, the external input is sampled during S5P2 of every machine cycle. When the samples show a high in one cycle and a low in the next cycle, the count is incremented. The new count value appears in the register during S3P1 of the cycle following the one in which the transition was detected. Since two machine cycles (24 oscillator periods) are required to recognize a 1-to-0 transition, the maximum count rate is 1/24 of the oscillator frequency. To ensure that a given level is sampled at least once before it changes, the level should be held for at least one full machine cycle.

Table 10-1. Timer 2 Operating Modes

RCLK + TCLK	CP/$\overline{RL2}$	TR2	MODE
0	0	1	16-bit Auto-reload
0	1	1	16-bit Capture
1	X	1	Baud Rate Generator
X	X	0	(Off)

Table 10-2. T2CON – Timer/Counter 2 Control Register

T2CON Address = 0C8H — Reset Value = 0000 0000B

Bit Addressable

Bit	7	6	5	4	3	2	1	0
	TF2	EXF2	RCLK	TCLK	EXEN2	TR2	C/$\overline{T2}$	CP/$\overline{RL2}$

Symbol	Function
TF2	Timer 2 overflow flag set by a Timer 2 overflow and must be cleared by software. TF2 will not be set when either RCLK = 1 or TCLK = 1.
EXF2	Timer 2 external flag set when either a capture or reload is caused by a negative transition on T2EX and EXEN2 = 1. When Timer 2 interrupt is enabled, EXF2 = 1 will cause the CPU to vector to the Timer 2 interrupt routine. EXF2 must be cleared by software. EXF2 does not cause an interrupt in up/down counter mode (DCEN = 1).
RCLK	Receive clock enable. When set, causes the serial port to use Timer 2 overflow pulses for its receive clock in serial port Modes 1 and 3. RCLK = 0 causes Timer 1 overflows to be used for the receive clock.
TCLK	Transmit clock enable. When set, causes the serial port to use Timer 2 overflow pulses for its transmit clock in serial port Modes 1 and 3. TCLK = 0 causes Timer 1 overflows to be used for the transmit clock.
EXEN2	Timer 2 external enable. When set, allows a capture or reload to occur as a result of a negative transition on T2EX if Timer 2 is not being used to clock the serial port. EXEN2 = 0 causes Timer 2 to ignore events at T2EX.
TR2	Start/Stop control for Timer 2. TR2 = 1 starts the timer.
C/$\overline{T2}$	Timer or counter select for Timer 2. C/$\overline{T2}$ = 0 for timer function. C/$\overline{T2}$ = 1 for external event counter (falling edge triggered).
CP/$\overline{RL2}$	Capture/Reload select. CP/$\overline{RL2}$ = 1 causes captures to occur on negative transitions at T2EX if EXEN2 = 1. CP/$\overline{RL2}$ = 0 causes automatic reloads to occur when Timer 2 overflows or negative transitions occur at T2EX when EXEN2 = 1. When either RCLK or TCLK = 1, this bit is ignored and the timer is forced to auto-reload on Timer 2 overflow.

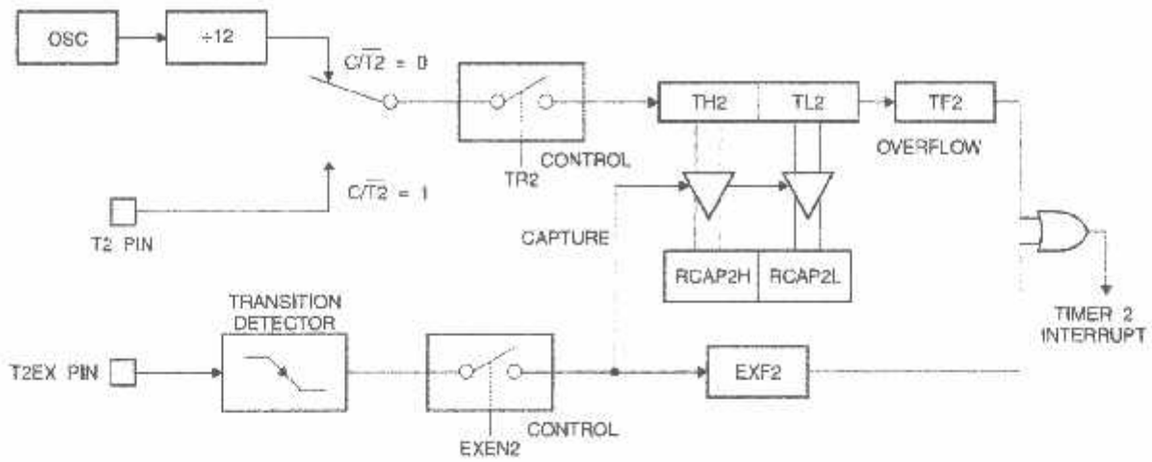
10.1 Timer 2 Registers

Control and status bits are contained in registers T2CON (see Table 10-2) and T2MOD (see Table 10-3) for Timer 2. The register pair (RCAP2H, RCAP2L) are the Capture/Reload registers for Timer 2 in 16-bit capture mode or 16-bit auto-reload mode.

10.2 Capture Mode

In the capture mode, two options are selected by bit EXEN2 in T2CON. If EXEN2 = 0, Timer 2 is a 16-bit timer or counter which upon overflow sets bit TF2 in T2CON. This bit can then be used to generate an interrupt. If EXEN2 = 1, Timer 2 performs the same operation, but a 1-to-0 transition at external input T2EX also causes the current value in TH2 and TL2 to be captured into RCAP2H and RCAP2L, respectively. In addition, the transition at T2EX causes bit EXF2 in T2CON to be set. The EXF2 bit, like TF2, can generate an interrupt. The capture mode is illustrated in Figure 10-1.

Figure 10-1. Timer 2 in Capture Mode



10.3 Auto-reload (Up or Down Counter)

Timer 2 can be programmed to count up or down when configured in its 16-bit auto-reload mode. This feature is invoked by the DCEN (Down Counter Enable) bit located in the SFR T2MOD (see Table 10-3). Upon reset, the DCEN bit is set to 0 so that timer 2 will default to count up. When DCEN is set, Timer 2 can count up or down, depending on the value of the T2EX pin.

Table 10-3. T2MOD – Timer 2 Mode Control Register

T2MOD Address = 0C9H — Reset Value = XXXX XX00B

Not Bit Addressable

	–	–	–	–	–	–	T2OE	DCEN
Bit	7	6	5	4	3	2	1	0

Symbol	Function
–	Not implemented, reserved for future use.
T2OE	Timer 2 Output Enable bit.
DCEN	When set, this bit allows Timer 2 to be configured as an up/down counter.

Figure 10-2 shows Timer 2 automatically counting up when DCEN = 0. In this mode, two options are selected by bit EXEN2 in T2CON. If EXEN2 = 0, Timer 2 counts up to 0FFFFH and then sets the TF2 bit upon overflow. The overflow also causes the timer registers to be reloaded with the 16-bit value in RCAP2H and RCAP2L. The values in RCAP2H and RCAP2L are preset by software. If EXEN2 = 1, a 16-bit reload can be triggered either by an overflow or by a 1-to-0 transition at external input T2EX. This transition also sets the EXF2 bit. Both the TF2 and EXF2 bits can generate an interrupt if enabled.

Setting the DCEN bit enables Timer 2 to count up or down, as shown in Figure 10-3. In this mode, the T2EX pin controls the direction of the count. A logic 1 at T2EX makes Timer 2 count up. The timer will overflow at 0FFFFH and set the TF2 bit. This overflow also causes the 16-bit value in RCAP2H and RCAP2L to be reloaded into the timer registers, TH2 and TL2, respectively.

A logic 0 at T2EX makes Timer 2 count down. The timer underflows when TH2 and TL2 equal the values stored in RCAP2H and RCAP2L. The underflow sets the TF2 bit and causes 0FFFFH to be reloaded into the timer registers.

The EXF2 bit toggles whenever Timer 2 overflows or underflows and can be used as a 17th bit of resolution. In this operating mode, EXF2 does not flag an interrupt.

Figure 10-2. Timer 2 in Auto Reload Mode (DCEN = 0)

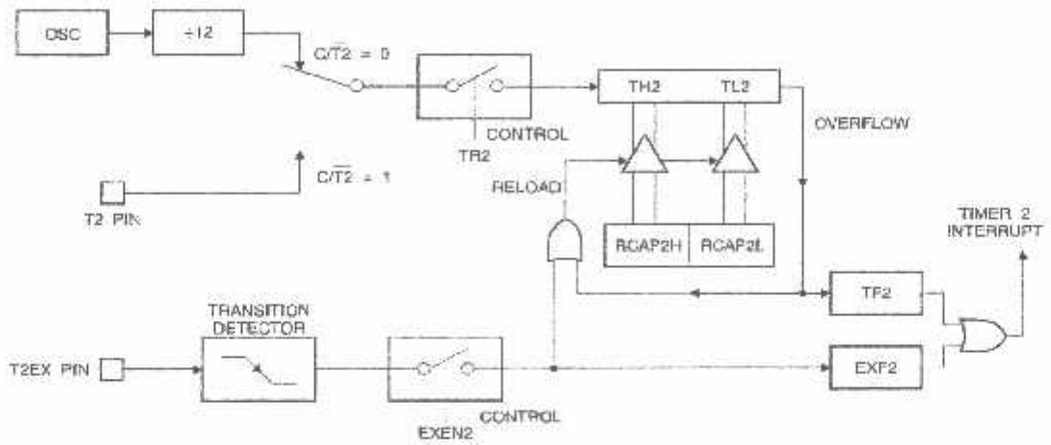


Figure 10-3. Timer 2 Auto Reload Mode (DCEN = 1 Timer 2 Auto Reload Mode (DCEN = 1)

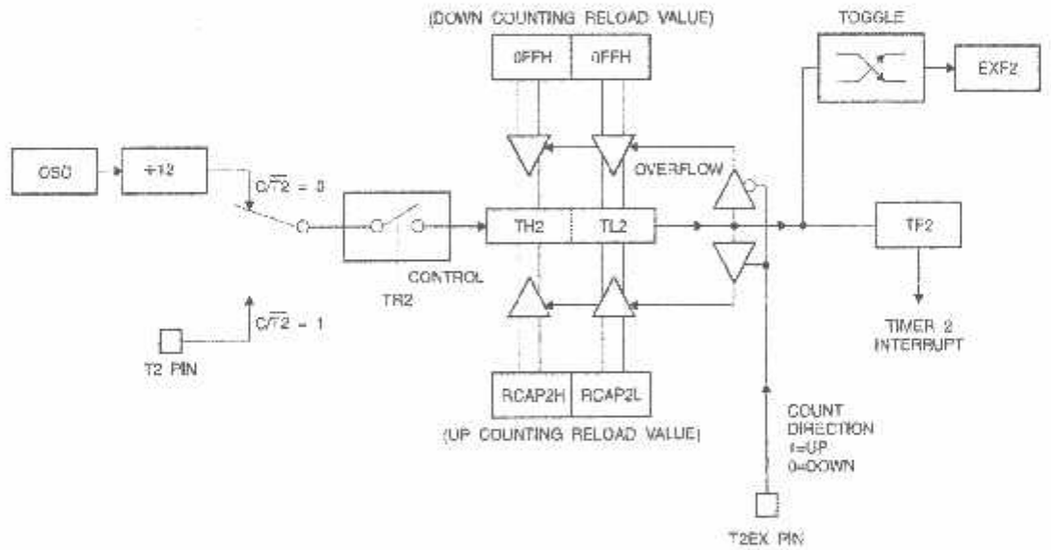
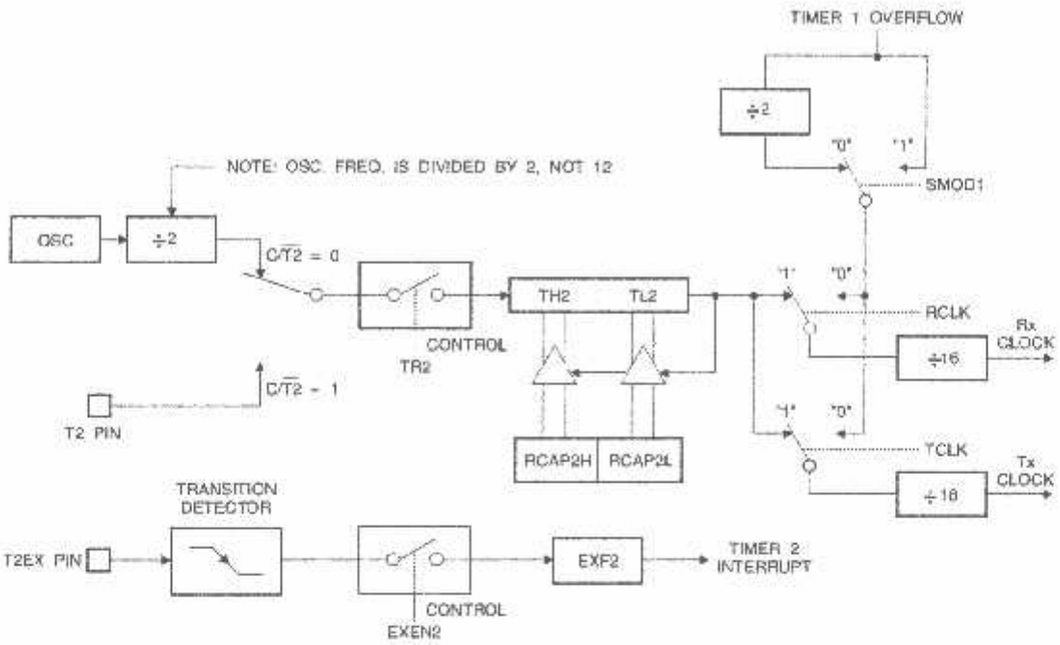


Figure 10-4. Timer 2 in Baud Rate Generator Mode



11. Baud Rate Generator

Timer 2 is selected as the baud rate generator by setting TCLK and/or RCLK in T2CON (Table 10-2). Note that the baud rates for transmit and receive can be different if Timer 2 is used for the receiver or transmitter and Timer 1 is used for the other function. Setting RCLK and/or TCLK puts Timer 2 into its baud rate generator mode, as shown in Figure 10-4.

The baud rate generator mode is similar to the auto-reload mode, in that a rollover in TH2 causes the Timer 2 registers to be reloaded with the 16-bit value in registers RCAP2H and RCAP2L, which are preset by software.

The baud rates in Modes 1 and 3 are determined by Timer 2's overflow rate according to the following equation.

$$\text{Modes 1 and 3 Baud Rates} = \frac{\text{Timer 2 Overflow Rate}}{16}$$

The Timer can be configured for either timer or counter operation. In most applications, it is configured for timer operation ($C/\overline{T2} = 0$). The timer operation is different for Timer 2 when it is used as a baud rate generator. Normally, as a timer, it increments every machine cycle (at 1/12 the oscillator frequency). As a baud rate generator, however, it increments every state time (at 1/2 the oscillator frequency). The baud rate formula is given below.

$$\frac{\text{Modes 1 and 3}}{\text{Baud Rate}} = \frac{\text{Oscillator Frequency}}{32 \times [65536 - (\text{RCAP2H,RCAP2L})]}$$

where (RCAP2H, RCAP2L) is the content of RCAP2H and RCAP2L taken as a 16-bit unsigned integer.

Timer 2 as a baud rate generator is shown in Figure 10-4. This figure is valid only if RCLK or TCLK = 1 in T2CON. Note that a rollover in TH2 does not set TF2 and will not generate an interrupt. Note too, that if EXEN2 is set, a 1-to-0 transition in T2EX will set EXF2 but will not cause a reload from (RCAP2H, RCAP2L) to (TH2, TL2). Thus when Timer 2 is in use as a baud rate generator, T2EX can be used as an extra external interrupt.

Note that when Timer 2 is running (TR2 = 1) as a timer in the baud rate generator mode, TH2 or TL2 should not be read from or written to. Under these conditions, the Timer is incremented every state time, and the results of a read or write may not be accurate. The RCAP2 registers may be read but should not be written to, because a write might overlap a reload and cause write and/or reload errors. The timer should be turned off (clear TR2) before accessing the Timer 2 or RCAP2 registers.

12. Programmable Clock Out

A 50% duty cycle clock can be programmed to come out on P1.0, as shown in Figure 12-1. This pin, besides being a regular I/O pin, has two alternate functions. It can be programmed to input the external clock for Timer/Counter 2 or to output a 50% duty cycle clock ranging from 61 Hz to 4 MHz (for a 16 MHz operating frequency).

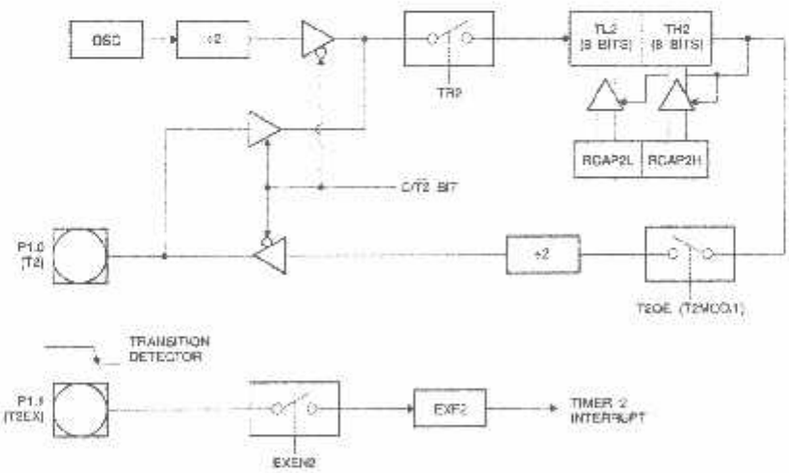
To configure the Timer/Counter 2 as a clock generator, bit C/$\overline{T2}$ (T2CON.1) must be cleared and bit T2OE (T2MOD.1) must be set. Bit TR2 (T2CON.2) starts and stops the timer.

The clock-out frequency depends on the oscillator frequency and the reload value of Timer 2 capture registers (RCAP2H, RCAP2L), as shown in the following equation.

$$\text{Clock Out Frequency} = \frac{\text{Oscillator Frequency}}{4 \times [65536 - (\text{RCAP2H,RCAP2L})]}$$

In the clock-out mode, Timer 2 rollovers will not generate an interrupt. This behavior is similar to when Timer 2 is used as a baud-rate generator. It is possible to use Timer 2 as a baud-rate generator and a clock generator simultaneously. Note, however, that the baud-rate and clock-out frequencies cannot be determined independently from one another since they both use RCAP2H and RCAP2L.

Figure 12-1. Timer 2 in Clock-out Mode



13. UART

The UART in the AT89S8253 operates the same way as the UART in the AT89S51 and AT89S52. For more detailed information on the UART operation, please click on the document link below:

http://www.atmel.com/dyn/resources/prod_documents/DOC4316.PDF

13.1 Enhanced UART

In addition to all of its usual modes, the UART can perform framing error detection by looking for missing stop bits, and automatic address recognition. The UART also fully supports multiprocessor communication as does the standard 80C51 UART.

When used for framing error detect, the UART looks for missing stop bits in the communication. A missing bit will set the FE bit in the SCON register. The FE bit shares the SCON.7 bit with SM0 and the function of SCON.7 is determined by PCON.6 (SMOD0). If SMOD0 is set then SCON.7 functions as FE. SCON.7 functions as SM0 when SMOD0 is cleared. When used as FE, SCON.7 can only be cleared by software.

13.1.1 Automatic Address Recognition

Automatic Address Recognition is a feature which allows the UART to recognize certain addresses in the serial bit stream by using hardware to make the comparisons. This feature saves a great deal of software overhead by eliminating the need for the software to examine every serial address which passes by the serial port. This feature is enabled by setting the SM2 bit in SCON. In the 9-bit UART modes, mode 2 and mode 3, the Receive Interrupt flag (RI) will be automatically set when the received byte contains either the "Given" address or the "Broadcast" address. The 9-bit mode requires that the 9th information bit is a 1 to indicate that the received information is an address and not data.

The 8-bit mode is called mode 1. In this mode the RI flag will be set if SM2 is enabled and the information received has a valid stop bit following the 8 address bits and the information is either a Given or Broadcast address.

Mode 0 is the Shift Register mode and SM2 is ignored.

Using the Automatic Address Recognition feature allows a master to selectively communicate with one or more slaves by invoking the given slave address or addresses. All of the slaves may be contacted by using the Broadcast address. Two special Function Registers are used to define the slave's address, SADDR, and the address mask, SADEN. SADEN is used to define which bits in the SADDR are to be used and which bits are "don't care". The SADEN mask can be logically ANDed with the SADDR to create the "Given" address which the master will use for addressing each of the slaves. Use of the Given address allows multiple slaves to be recognized while excluding others. The following examples will help to show the versatility of this scheme:

Slave 0

SADDR = 1100 0000

SADEN = 1111 1101

Given = 1100 00X0

Slave 1

SADDR = 1100 0000

SADEN = 1111 1110

Given = 1100 000X

In the previous example SADDR is the same and the SADEN data is used to differentiate between the two slaves. Slave 0 requires a 0 in bit 0 and it ignores bit 1. Slave 1 requires a 0 in bit 1 and bit 0 is ignored. A unique address for slave 0 would be 1100 0010 since slave 1 requires a 0 in bit 1. A unique address for slave 1 would be 1100 0001 since a 1 in bit 0 will exclude slave 0. Both slaves can be selected at the same time by an address which has bit 0 = 0 (for slave 0) and bit 1 = 0 (for slave 1). Thus, both could be addressed with 1100 0000.

In a more complex system the following could be used to select slaves 1 and 2 while excluding slave 0:

Slave 0

SADDR = 1100 0000

SADEN = 1111 1001

Given = 1100 0XX0

Slave 1

SADDR = 1110 0000

SADEN = 1111 1010

Given = 1110 0X0X

Slave 2

SADDR = 1110 0000

SADEN = 1111 1100

Given = 1110 00XX

In the previous example the differentiation among the 3 slaves is in the lower 3 address bits. Slave 0 requires that bit 0 = 0 and it can be uniquely addressed by 1110 0110. Slave 1 requires that bit 1 = 0 and it can be uniquely addressed by 1110 and 0101. Slave 2 requires that bit 2 = 0 and its unique address is 1110 0011. To select Slaves 0 and 1 and exclude Slave 2, use address 1110 0100, since it is necessary to make bit 2 = 1 to exclude slave 2.

The Broadcast Address for each slave is created by taking the logical OR of SADDR and SADEN. Zeros in this result are trended as don't-cares. In most cases, interpreting the don't-cares as ones, the broadcast address will be FF hexadecimal.

Upon reset SADDR (SFR address 0A9H) and SADEN (SFR address 0B9H) are loaded with 0s. This produces a given address of all "don't cares" as well as a Broadcast address of all "don't cares". This effectively disables the Automatic Addressing mode and allows the microcontroller to use standard 80C51-type UART drivers which do not make use of this feature.

Table 13-1. PCON – Power Control Register

PCON Address = 87H — Reset Value = 00xx 0000B

Bit Addressable

Bit	7	6	5	4	3	2	1	0
	SMOD1	SMOD0	–	POF	GF1	GF0	PD	IDL

Symbol	Function
SMOD1	Double Baud Rate bit. Doubles the baud rate of the UART in Modes 1, 2, or 3.
SMOD0	Frame Error Select. When SMOD0 = 1, SCON.7 is SM0. When SMOD0 = 1, SCON.7 is FE. Note that FE will be set after a frame error regardless of the state of SMOD0.
POF	Power Off Flag. POF is set to "1" during power up (i.e. cold reset). It can be set or reset under software control and is not affected by RST or BOD (i.e. warm resets).
GF1, GF0	General-purpose Flags
PD	Power-down bit. Setting this bit activates power-down operation.
IDL	Idle Mode bit. Setting this bit activates Idle mode operation

Table 13-2. SCON – Serial Port Control Register

SCON Address = 98H — Reset Value = 0000 0000B

Bit Addressable

Bit	7	6	5	4	3	2	1	0
	SM0/FE	SM1	SM2	REN	TB8	RB8	TI	RI

(SMOD0 = 0/1)[1]

Symbol	Function
FE	Framing error bit. This bit is set by the receiver when an invalid stop bit is detected. The FE bit is not cleared by valid frames but should be cleared by software. The SMOD0 bit must be set to enable access to the FE bit. FE will be set regardless of the state of SMOD0.
SM0	Serial Port Mode Bit 0, (SMOD0 must = 0 to access bit SM0)
SM1	Serial Port Mode Bit 1 SM0 / SM1 / Mode / Description / Baud Rate[2] 0 / 0 / 0 / shift register / $f_{osc}/12$ 0 / 1 / 1 / 8-bit UART / variable 1 / 0 / 2 / 9-bit UART / $f_{osc}/64$ or $f_{osc}/32$ 1 / 1 / 3 / 9-bit UART / variable
SM2	Enables the Automatic Address Recognition feature in modes 2 or 3. If SM2 = 1 then RI will not be set unless the received 9th data bit (RB8) is 1, indicating an address, and the received byte is a Given or Broadcast Address. In mode 1, if SM2 = 1 then RI will not be activated unless a valid stop bit was received, and the received byte is a Given or Broadcast Address. In Mode 0, SM2 should be 0.
REN	Enables serial reception. Set by software to enable reception. Clear by software to disable reception.
TB8	The 9th data bit that will be transmitted in modes 2 and 3. Set or clear by software as desired.
RB8	In modes 2 and 3, the 9th data bit that was received. In mode 1, if SM2 = 0, RB8 is the stop bit that was received. In mode 0, RB8 is not used.
TI	Transmit interrupt flag. Set by hardware at the end of the 8th bit time in mode 0, or at the beginning of the stop bit in the other modes, in any serial transmission. Must be cleared by software.
RI	Receive interrupt flag. Set by hardware at the end of the 8th bit time in mode 0, or halfway through the stop bit time in the other modes, in any serial reception (except see SM2). Must be cleared by software.

Notes: 1. SMOD0 is located at PCON.6.
2. f_{osc} = oscillator frequency.

14. Serial Peripheral Interface

The serial peripheral interface (SPI) allows high-speed synchronous data transfer between the AT89S8253 and peripheral devices or between multiple AT89S8253 devices. The AT89S8253 SPI features include the following:

- Full-Duplex, 3-Wire Synchronous Data Transfer
- Master or Slave Operation
- Maximum Bit Frequency = f/4 (f/2 if in x2 Clock Mode)
- LSB First or MSB First Data Transfer
- Four Programmable Bit Rates in Master Mode
- End of Transmission Interrupt Flag
- Write Collision Flag Protection
- Double-Buffered Receive
- Double-Buffered Transmit (Enhanced Mode only)
- Wakeup from Idle Mode (Slave Mode only)

The interconnection between master and slave CPUs with SPI is shown in Figure 14-1. The four pins in the interface are Master-In/Slave-Out (MISO), Master-Out/Slave-In (MOSI), Shift Clock (SCK), and Slave Select ($\overline{SS}$). The SCK pin is the clock output in master mode, but is the clock input in slave mode. The MSTR bit in SPCR determines the directions of MISO and MOSI. Also notice that MOSI connects to MOSI and MISO to MISO. In master mode, $\overline{SS}$/P1.4 is ignored and may be used as a general-purpose input or output. In slave mode, $\overline{SS}$ must be driven low to select an individual device as a slave. When $\overline{SS}$ is driven high, the slave's SPI port is deactivated and the MOSI/P1.5 pin can be used as a general-purpose input.

Figure 14-1. SPI Master-Slave Interconnection

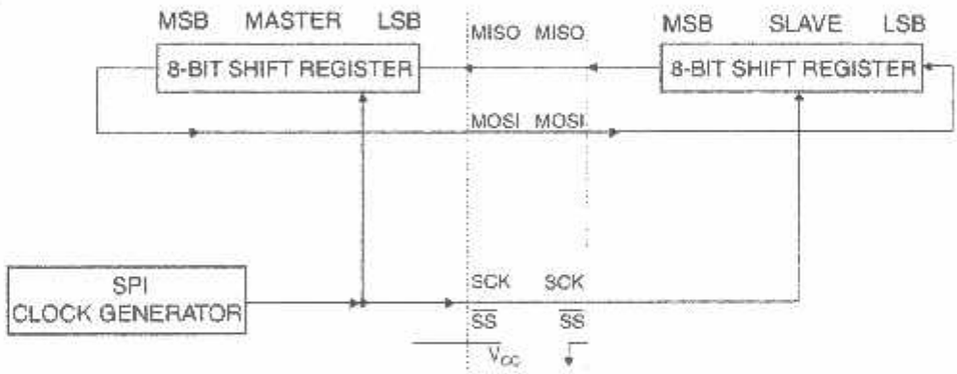
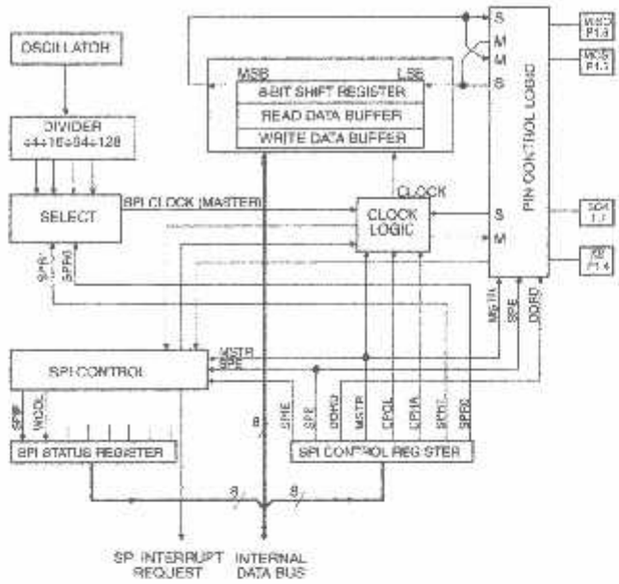


Figure 14-2. SPI Block Diagram



Note: 1. The Write Data Buffer is only used in enhanced SPI mode.

The SPI has two modes of operation: normal (non-buffered write) and enhanced (buffered write). In normal mode, writing to the SPI data register (SPDR) of the master CPU starts the SPI clock generator and the data written shifts out of the MOSI pin and into the MOSI pin of the slave CPU. Transmission may start after an initial delay while the clock generator waits for the next full bit slot of the specified baud rate. After shifting one byte, the SPI clock generator stops, setting the end of transmission flag (SPIF) and transferring the received byte to the read buffer (SPDR). If both the SPI interrupt enable bit (SPIE) and the serial port interrupt enable bit (ES) are set, an interrupt is requested. Note that SPDR refers to either the write data buffer or the read data buffer, depending on whether the access is a write or read. In normal mode, because the write buffer is transparent (and a write access to SPDR will be directed to the shift buffer), any attempt to write to SPDR while a transmission is in progress will result in a write collision with WCOL set. However, the transmission will still complete normally, but the new byte will be ignored and a new write access to SPDR will be necessary.

Enhanced mode is similar to normal mode except that the write buffer holds the next byte to be transmitted. Writing to SPDR loads the write buffer and sets WCOL to signify that the buffer is full and any further writes will overwrite the buffer. WCOL is cleared by hardware when the buffered byte is loaded into the shift register and transmission begins. If the master SPI is currently idle, i.e. if this is the first byte, then after loading SPDR, transmission of the byte starts and WCOL is cleared immediately. While this byte is transmitting, the next byte may be written to SPDR. The Load Enable flag (LDEN) in SPSR can be used to determine when transmission has started. LDEN is asserted during the first four bit slots of a SPI transfer. The master CPU should first check that LDEN is set and that WCOL is cleared before loading the next byte. In enhanced mode, if WCOL is set when a transfer completes, i.e. the next byte is available, then the SPI immediately loads the buffered byte into the shift register, resets WCOL, and continues transmission without stopping and restarting the clock generator. As long as the CPU can keep the write buffer full in this manner, multiple bytes may be transferred with minimal latency between bytes.

Table 14-1. SPCR – SPI Control Register

SPCR Address = D5H — Reset Value = 0000 0100B

Not Bit Addressable

	SPIE	SPE	DORD	MSTR	CPOL	CPHA	SPR1	SPR0
Bit	7	6	5	4	3	2	1	0

Symbol	Function
SPIE	SPI interrupt enable. This bit, in conjunction with the ES bit in the IE register, enables SPI interrupts: SPIE = 1 and ES = 1 enable SPI interrupts. SPIE = 0 disables SPI interrupts.
SPE	SPI enable. SPI = 1 enables the SPI channel and connects $\overline{SS}$, MOSI, MISO and SCK to pins P1.4, P1.5, P1.6, and P1.7. SPI = 0 disables the SPI channel.
DORD	Data order. DORD = 1 selects LSB first data transmission. DORD = 0 selects MSB first data transmission.
MSTR	Master/slave select. MSTR = 1 selects Master SPI mode. MSTR = 0 selects slave SPI mode.
CPOL	Clock polarity. When CPOL = 1, SCK is high when idle. When CPOL = 0, SCK of the master device is low when not transmitting. Please refer to figure on SPI clock phase and polarity control.
CPHA	Clock phase. The CPHA bit together with the CPOL bit controls the clock and data relationship between master and slave. Please refer to figure on SPI clock phase and polarity control.
SPR0 SPR1	SPI clock rate select. These two bits control the SCK rate of the device configured as master. SPR1 and SPR0 have no effect on the slave. The relationship between SCK and the oscillator frequency, $F_{osc.}$, is as follows: **SPR1 SPR0 SCK** 0 0 f/4 (f/2 in x2 mode) 0 1 f/16 (f/8 in x2 mode) 1 0 f/64 (f/32 in x2 mode) 1 1 f/128 (f/64 in x2 mode)

Notes:
1. Set up the clock mode before enabling the SPI: set all bits needed in SPCR except the SPE bit, then set SPE.
2. Enable the master SPI prior to the slave device.
3. Slave echoes master on next Tx if not loaded with new data.

ChipCorder®
TECHNOLOGY BY ISD

ISD1400 Series

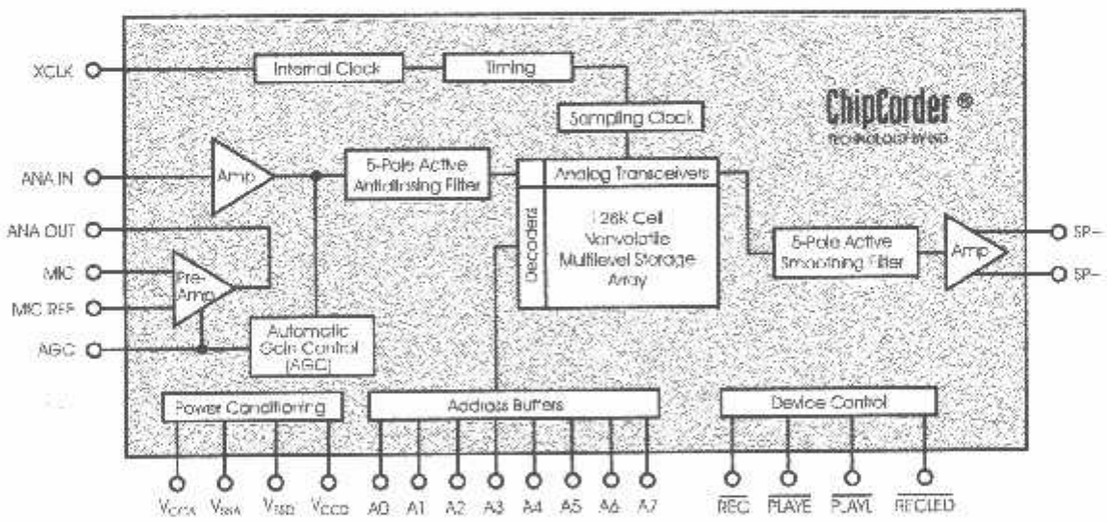
Single-Chip Voice Record/Playback Devices
16- and 20-Second Durations

GENERAL DESCRIPTION

Information Storage Devices' ISD1400 ChipCorder® series provides high-quality, single-chip record/playback solutions to short-duration messaging applications. The CMOS devices include an on-chip oscillator, microphone preamplifier, automatic gain control, antialiasing filter, smoothing filter, and speaker amplifier. A minimum record/playback subsystem can be configured with a microphone, a speaker, several passives, two push-buttons, and a power source.

Recordings are stored in on-chip nonvolatile memory cells, providing zero-power message storage. This unique, single-chip solution is made possible through ISD's patented multilevel storage technology. Voice and audio signals are stored directly into memory in their natural form, providing high-quality, solid-state voice reproduction.

Figure: ISD1400 Series Block Diagram



FEATURES

- Easy-to-use single-chip voice record/playback solution
- High-quality, natural voice/audio reproduction
- Push-button interface
  - Playback can be edge- or level-activated
- Single-chip durations of 16 and 20 seconds
- Automatic power-down mode
  - Enters standby mode immediately following a record or playback cycle
  - Standby current 0.5 μA (typical)
- Zero-power message storage
  - Eliminates battery backup circuits
- Fully addressable to handle multiple messages
- 100-year message retention (typical)
- 100,000 record cycles (typical)
- On-chip clock source
- No programmer or development system needed
- Single +5 volt power supply
- Available in die form, DIP, and SOIC packaging
- Industrial temperature (–40°C to +85°C) versions available

Table: ISD1400 Series Summary

Part Number	Minimum Duration (Seconds)	Input Sample Rate (KHz)	Typical Filter Pass Band (KHz)
ISD1416	16	8.0	3.3
ISD1420	20	6.4	2.6

Table of Contents

ISD1400 Series

Single-Chip Voice Record/Playback Devices
16- and 20-Second Durations

FIGURES, CHARTS, AND TABLES IN THE ISD1400 SERIES DATASHEET

DETAILED DESCRIPTION

SPEECH/SOUND QUALITY

The ISD1400 series includes devices offered at 6.4 and 8.0 KHz sampling frequencies, allowing the user a choice of speech quality options. The speech samples are stored directly into on-chip nonvolatile memory without the digitization and compression associated with other solutions. Direct analog storage provides a very true, natural sounding reproduction of voice, music, tones, and sound effects not available with most solid-state digital solutions.

DURATION

To meet end system requirements, the ISD1400 series offers single-chip solutions at 16 and 20 seconds.

EEPROM STORAGE

One of the benefits of ISD's ChipCorder technology is the use of on-chip nonvolatile memory, providing zero-power message storage. The message is retained for up to 100 years typically without power. In addition, the device can be re-recorded typically over 100,000 times.

BASIC OPERATION

The ISD1400 ChipCorder series devices are controlled by a single record signal, $\overline{REC}$, and either of two push-button control playback signals, $\overline{PLAYE}$ (edge-activated playback), and PLAYL (level-activated playback). The ISD1400 parts are configured for simplicity of design in a single-message application. Using the address lines will allow multiple message applications. Device operation is explained on page 15.

AUTOMATIC POWER-DOWN MODE

At the end of a playback or record cycle, the ISD1400 series devices automatically return to a low-power standby mode, consuming typically 0.5 μA. During a playback cycle, the device powers down automatically at the end of the message. During a record cycle, the device powers down immediately after $\overline{REC}$ is released HIGH.

ADDRESSING (OPTIONAL)

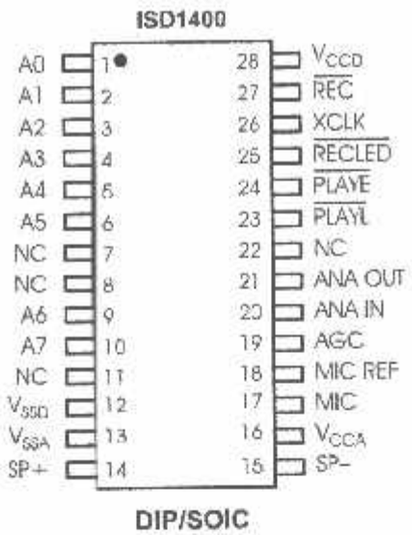
In addition to providing simple message playback, the ISD1400 series provides a full addressing capability.

The ISD1400 series storage array has 160 distinct addressable segments, providing the following resolutions. See Application Information for ISD1400 address tables.

Table 1: Device Playback/Record Durations

Part Number	Minimum Duration (Seconds)
ISD1416	100 ms
ISD1420	125 ms

Figure 1: ISD1400 Series Pinouts



NOTE: *NC means must Not Connect.*

PIN DESCRIPTION

NOTE *The $\overline{REC}$ signal is debounced for 50 ms on the rising edge to prevent a false retriggering from a push-button switch.*

VOLTAGE INPUTS (V_{CCA}, V_{CCD})

Analog and digital circuits internal to the ISD1400 series use separate power buses to minimize noise on the chip. These power buses are brought out to separate pins on the package and should be tied together as close to the supply as possible. It is important that the power supply be decoupled as close as possible to the package.

GROUND INPUTS (V_{SSA}, V_{SSD})

Similar to V_{CCA} and V_{CCD}, the analog and digital circuits internal to the ISD1400 series use separate ground buses to minimize noise. These pins should be tied together as close as possible to the device.

RECORD ($\overline{REC}$)

The $\overline{REC}$ input is an active-LOW record signal. The device records whenever $\overline{REC}$ is LOW. This signal must remain LOW for the duration of the recording. $\overline{REC}$ takes precedence over either playback ($\overline{PLAYE}$ or $\overline{PLAYL}$) signal. If $\overline{REC}$ is pulled LOW during a playback cycle, the playback immediately ceases and recording begins.

A record cycle is completed when $\overline{REC}$ is pulled HIGH or the memory space is filled.

An end-of-message marker (EOM) is internally recorded, enabling a subsequent playback cycle to terminate appropriately. The device automatically powers down to standby mode when $\overline{REC}$ goes HIGH.

PLAYBACK, EDGE-ACTIVATED ($\overline{PLAYE}$)

When a LOW-going transition is detected on this input signal, a playback cycle begins. Playback continues until an EOM is encountered or the end of the memory space is reached. Upon completion of the playback cycle, the device automatically powers down into standby mode. Taking $\overline{PLAYE}$ HIGH during a playback cycle will not terminate the current cycle.

PLAYBACK, LEVEL-ACTIVATED ($\overline{PLAYL}$)

When this input signal transitions from HIGH to LOW, a playback cycle is initiated. Playback continues until $\overline{PLAYL}$ is pulled HIGH, an EOM marker is detected, or the end of the memory space is reached. The device automatically powers down to standby mode upon completion of the playback cycle.

NOTE *In playback, if either $\overline{PLAYE}$ or $\overline{PLAYL}$ is held LOW during EOM or OVF, the device will still enter standby and the internal oscillator and timing generator will stop. However, the rising edge of $\overline{PLAYE}$ and $\overline{PLAYL}$ are not debounced and any subsequent falling edge (particularly switch bounce) present on the input pins will initiate another playback.*

RECORD LED OUTPUT ($\overline{\text{RECLED}}$)

The output $\overline{\text{RECLED}}$ is LOW during a record cycle. It can be used to drive an LED to provide feedback that a record cycle is in progress. In addition, $\overline{\text{RECLED}}$ pulses LOW momentarily when an EOM is encountered in a playback cycle.

MICROPHONE INPUT (MIC)

The microphone input transfers its signal to the on-chip preamplifier. An on-chip Automatic Gain Control (AGC) circuit controls the gain of this preamplifier from –15 to 24 dB. An external microphone should be AC coupled to this pin via a series capacitor. The capacitor value, together with the internal 10 KΩ resistance on this pin, determine the low-frequency cutoff for the ISD1400 series passband. See Application Information for additional information on low-frequency cutoff calculations.

MICROPHONE REFERENCE (MIC REF)

The MIC REF input is the inverting input to the microphone preamplifier. This provides a noise-canceling or common-mode rejection input to the device when connected differentially to a microphone.

AUTOMATIC GAIN CONTROL (AGC)

The AGC dynamically adjusts the gain of the preamplifier to compensate for the wide range of microphone input levels. The AGC allows the full range of sound, from whispers to loud sounds, to be recorded with minimal distortion. The "attack" time is determined by the time constant of a 5 KΩ internal resistance and an external capacitor (C6 on the schematic in Figure 4) connected from the AGC pin to V_{SSA} analog ground. The "release" time is determined by the time constant of an external resistor (R5) and an external capacitor (C6) connected in parallel between the AGC Pin and V_{SSA} analog ground. Nominal values of 470 KΩ and 4.7 µF give satisfactory results in most cases.

ANALOG OUTPUT (ANA OUT)

This pin provides the preamplifier output to the user. The voltage gain of the preamplifier is determined by the voltage level at the AGC pin.

ANALOG INPUT (ANA IN)

The ANA IN pin transfers the input signal to the chip for recording. For microphone inputs, the ANA OUT pin should be connected via an external capacitor to the ANA IN pin. This capacitor value, together with the 3.0 KΩ input impedance of ANA IN, is selected to give additional cutoff at the low-frequency end of the voice passband. If the desired input is derived from a source other than a microphone, the signal can be fed, capacitively coupled, into the ANA IN pin directly.

EXTERNAL CLOCK INPUT (XCLK)

The external clock input for the ISD1400 devices has an internal pull-down device. The ISD1400 is configured at the factory with an internal sampling clock frequency that guarantees its minimum nominal record/playback time. For instance, an ISD1420 operating within specification will be observed to always have a minimum of 20 seconds of recording time. The sampling frequency is then maintained to a variation of ±2.25 percent over the commercial temperature and operating voltage ranges, while still maintaining the minimum specified recording duration. This will result in some devices having a few percent more than nominal recording time.

The internal clock has a ±5 percent tolerance over the industrial temperature and voltage range. A regulated power supply is recommended for industrial temperature parts. If greater precision is required, the device can be clocked through the XCLK pin as follows:

Table 2: External Clock Sample Rates

Part Number	Sample Rate	Required Clock
ISD1416	8.0 KHz	1024 KHz
ISD1420	6.4 KHz	819.2 KHz

These recommended clock rates should not be varied because the antialiasing and smoothing filters are fixed, and aliasing problems can occur if the sample rate differs from the one recommended. The duty cycle on the input clock is not critical, as the clock is immediately divided by two internally. **If the XCLK is not used, this input should be connected to ground.**

SPEAKER OUTPUTS (SP+, SP–)

The SP+ and SP– pins provide direct drive for loudspeakers with impedances as low as 16 Ω. A single output may be used, but, for direct-drive loudspeakers, the two opposite-polarity outputs provide an improvement in output power of up to four times over a single-ended connection. Furthermore, when SP– and SP– are used, a speaker-coupling capacitor is not required. A single-ended connection will require an AC-coupling capacitor between the SP pin and the speaker. The speaker outputs are in a high-impedance state during a record cycle, and held at V_{SSA} during power down.

ADDRESS INPUTS (A0–A7)

The Address Inputs have two functions, depending upon the level of the two Most Significant Bits (MSB) of the address.

If either of the two MSBs is LOW, the inputs are all interpreted as address bits and are used as the start address for the current record or playback cycle. The address pins are inputs only and do not output interna address information as the operation progresses. Address inputs are latched by the falling edge of $\overline{\text{PLAYE}}$, $\overline{\text{PLAYL}}$, or $\overline{\text{REC}}$.

OPERATIONAL MODES

The ISD1400 series is designed with several built-in operational modes provided to allow maximum functionality with a minimum of additional components, described in detail below. The operational modes use the address pins on the ISD1400 devices, but are mapped outside the valid address range. When the two Most Significant Bits (MSBs) are HIGH (A6 and A7), the remaining address signals are interpreted as mode bits and not as address bits. Therefore, operational modes and direct addressing are not compatible and cannot be used simultaneously.

There are two important considerations for using operational modes. First, all operations begin initially at address 0, which is the beginning of the ISD1400 address space. Later operations can begin at other address locations, depending on the operational mode(s) chosen. In addition, the address pointer is reset to 0 when the device is changed from record to playback but not from playback to record when A4 is HIGH in Operational Mode.

Second, an Operational Mode is executed when any of the control inputs, $\overline{\text{PLAYE}}$, $\overline{\text{PLAYL}}$, or $\overline{\text{REC}}$, go LOW and the two MSBs are HIGH. This Operational Mode remains in effect until the next LOW-going control input signal, at which point the current address/mode levels are sampled and executed.

NOTE *The two MSBs are on pins 9 and 10 for each ISD1400 series device.*

OPERATIONAL MODES DESCRIPTION

The Operational Modes can be used in conjunction with a microcontroller, or they can be hardwired to provide the desired system operation.

A0 — MESSAGE CUEING

Message Cueing allows the user to skip through messages, without knowing the actual physical addresses of each message. Each control input LOW pulse causes the internal address pointer to skip to the next message. This mode should be used for playback only, and is typically used with the A4 Operational Mode.

A1 — DELETE $\overline{\text{EOM}}$ MARKERS

The A1 Operational Mode allows sequentially recorded messages to be combined into a single message with only one EOM marker set at the end of the final message. When this operational mode is configured, messages recorded sequentially are played back as one continuous message.

A2 — UNUSED

A3 — MESSAGE LOOPING

The A3 Operational Mode allows for the automatic, continuously repeated playback of the message located at the beginning of the address space.

A message can completely fill the ISD1400 device and will loop from beginning to end. Pulsing $\overline{\text{PLAYE}}$ will start the playback and pulsing $\overline{\text{PLAYL}}$ will end the playback.

A4 — CONSECUTIVE ADDRESSING

During normal operations, the address pointer will reset when a message is played through to an EOM marker. The A4 Operational Mode inhibits the address pointer reset, allowing messages to be recorded or played back consecutively. When the device is in a static state; i.e., not recording or playing back, momentarily taking this pin LOW will reset the address counter to zero.

A5 — UNUSED

Table 3: Operational Modes Table

Address Cntl. (HIGH)	Function	Typical Use	Jointly Compatible[1]
A0	Message cueing	Fast-forward through messages	A4
A1	Delete EOM markers	Position EOM marker at the end of the last message	A3, A4
A2	Unused		
A3	Looping	Continuous playback from Address 0	A1
A4	Consecutive addressing	Record/play multiple consecutive messages	A0, A1
A5	Unused		

1. *Additional operational modes can be used simultaneously with the given mode.*

TIMING DIAGRAMS

Figure 2: Record

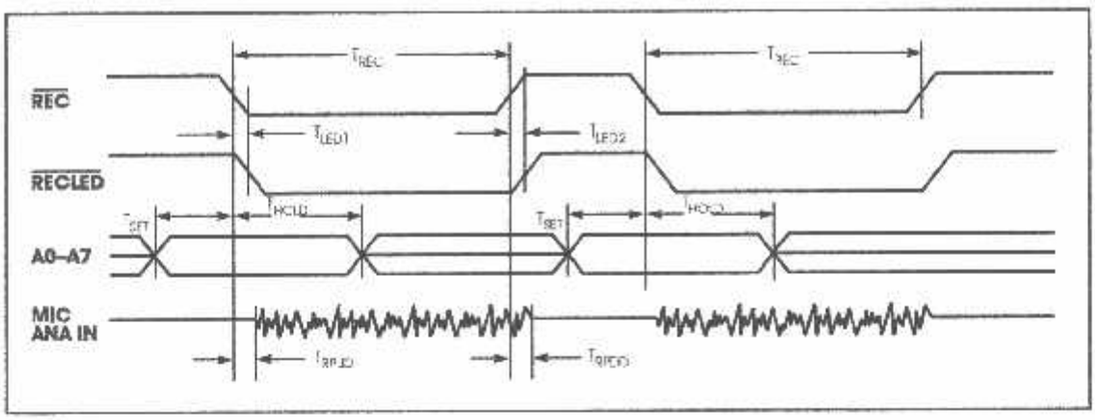
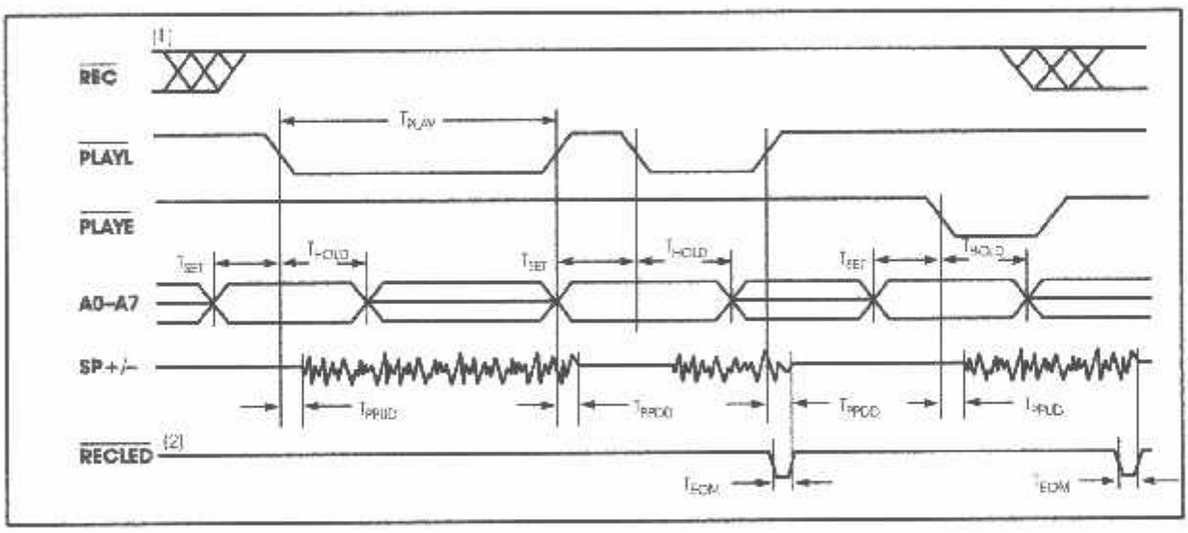


Figure 3: Playback



1. *REC must be HIGH for the entire duration of a playback cycle.*
2. *RECLED functions as an EOM during playback.*

Table 4: Absolute Maximum Ratings (Packaged Parts)[1]

Condition	Value
Junction temperature	150°C
Storage temperature range	–65°C to +150°C
Voltage applied to any pin	(V_{SS} – 0.3 V) to (V_{CC} + 0.3 V)
Voltage applied to any pin (Input current limited to ±20 mA)	(V_{SS} – 1.0 V) to (V_{CC} + 1.0 V)
Lead temperature (soldering – 10 seconds)	300°C
$V_{CC} - V_{SS}$	–0.3 V to +7.0 V

1. *Stresses above those listed may cause permanent damage to the device. Exposure to the absolute maximum ratings may affect device reliability. Functional operation is not implied at these conditions.*

Table 5: Operating Conditions (Packaged Parts)

Condition	Value
Commercial operating temperature range[1]	0°C to +70°C
Industrial operating temperature[1]	–40°C to +85°C
Supply voltage (V_{CC})[2]	+4.5 V to +5.5 V
Ground voltage (V_{SS})[3]	0 V

1. *Case temperature.*
2. $V_{CC} = V_{CCA} = V_{CCD}$.
3. $V_{SS} = V_{SSA} = V_{SSD}$.

Table 6: DC Parameters (Packaged Parts)

Symbol	Parameters	Min[2]	Typ[1]	Max[2]	Units	Conditions
V_{IL}	Input Low Voltage			0.8	V	
V_{IH}	Input High Voltage	2.4			V	
V_{OL}	Output Low Voltage			0.4	V	I_{OL} = 4.0 mA
V_{OH}	Output High Voltage	2.4			V	I_{OH} = –1.6 mA
I_{CC}	V_{CC} Current (Operating)		15	30	mA	V_{CC} = 5.5 V [3], R_{EXT} = ∞
I_{SB}	V_{CC} Current (Standby)		0.5	10	µA	[3] [4]
I_{IL}	Input Leakage Current			±1	µA	
I_{ILPD}	Input Current HIGH w/Pull Down			130	µA	Force V_{CC} [5]
R_{EXT}	Output Load Impedance	16			Ω	Speaker Load
R_{MIC}	Preamp In Input Resistance	4	9	17	KΩ	Pins 17, 18
$R_{ANA\ IN}$	ANA IN Input Resistance	2.5	3	5	KΩ	
A_{PRE1}	Preamp Gain 1	20	23	26	dB	AGC = 0.0 V
A_{PRE2}	Preamp Gain 2		–45	–15	dB	AGC = 2.5 V

Table 6: DC Parameters (Packaged Parts)

Symbol	Parameters	Min[2]	Typ [1]	Max[2]	Units	Conditions
A_{ARP}	ANA IN to SP+/– Gain	20	22	25	dB	
R_{AGC}	AGC Output Resistance	2.5	5	9.5	KΩ	
I_{PREH}	Preamp Out Source		–2		mA	@ V_{OUT} = 1.0 V
I_{PREL}	Preamp In Sink		0.5		mA	@ V_{OUT} = 2.0 V

1. *Typical values @ T_A = 25°C and 5.0 V.*
2. *All Min/Max limits are guaranteed by ISD via electrical testing or characterization. Not all specifications are 100 percent tested.*
3. *V_{CCA} and V_{CCD} connected together.*
4. *$\overline{REC}$, $\overline{PLAYL}$, and $\overline{PLAYE}$ must be at V_{CCD}.*
5. *XCLK pin.*

Table 7: AC Parameters (Packaged Parts)

Symbol	Characteristic		Min[2]	Typ [1]	Max[2]	Units	Conditions
F_S	Sampling Frequency	ISD1416 ISD1420			8 6.4	KHz KHz	[5] [5]
F_{CF}	Filter Pass Band	ISD1416 ISD1420		3.3 2.6		KHz KHz	3 dB Roll-Off Point [3][6] 3 dB Roll-Off Point [3][6]
T_{REC}	Record Duration	ISD1416 ISD1420	16 20			sec sec	
T_{PLAY}	Playback Duration	ISD1416 ISD1420	16 20			sec sec	[5] [5]
T_{LED1}	$\overline{REC}$LED ON Delay			5		msec	
T_{LED2}	$\overline{REC}$LED OFF Delay	ISD1416 ISD1420	30 40	38.9 48.6	95 110	msec msec	
T_{SET}	Address Setup Time		300			nsec	
T_{HOLD}	Address Hold Time		0			nsec	
T_{RPUD}	Record Power-Up Delay	ISD1416 ISD1420		26 32		msec msec	
T_{RPDD}	Record Power-Down Delay	ISD1416 ISD1420		26 32		msec msec	
T_{PPUD}	Play Power-Up Delay	ISD1416 ISD1420		26 32		msec msec	

Table 7: AC Parameters (Packaged Parts)

Symbol	Characteristic		Min[2]	Typ[1]	Max[2]	Units	Conditions
T_{PPDD}	Play Power-Down Delay	ISD1416 ISD1420		6.5 8.1		msec msec	
T_{EOM}	EOM Pulse Width	ISD1416 ISD1420		12.5 15.625		msec msec	
THD	Total Harmonic Distortion			1	3	%	@ 1 KHz
P_{OUT}	Speaker Output Power			12.2		mW	R_{EXT} = 16 Ω
V_{OUT}	Voltage Across Speaker Pins			1.25	2.5	V p-p	R_{EXT} = 600 Ω
V_{IN1}	MIC Input Voltage				20	mV	Peak-to-Peak [4]
V_{IN2}	ANA IN Input Voltage				50	mV	Peak-to-Peak

1. *Typical values @ T_A = 25°C and 5.0 V.*
2. *All Min/Max limits are guaranteed by ISD via electrical testing or characterization. Not all specifications are 100 percent tested.*
3. *Low-frequency cutoff depends upon value of external capacitors (see Pin Descriptions).*
4. *With 5.1 KΩ series resistor at ANA IN.*
5. *Sampling frequency and playback duration will vary as much as ±2.25 percent over the commercial temperature and voltage ranges. It may vary as much as ±5 percent over the industrial temperature and voltage ranges. All devices will meet the maximum sampling frequency and minimum playback duration parameters. For greater stability, an external clock can be utilized (see Pin Descriptions).*
6. *Filter specification applies to the antialiasing filter and to the smoothing filter.*

TYPICAL PARAMETER VARIATION WITH VOLTAGE AND TEMPERATURE (PACKAGED PARTS)

Chart 1: Record Mode Operating Current (I_{CC})

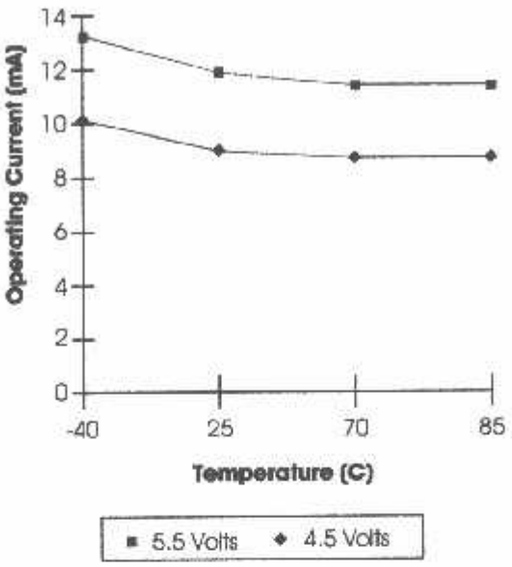


Chart 3: Standby Current (I_{SB})

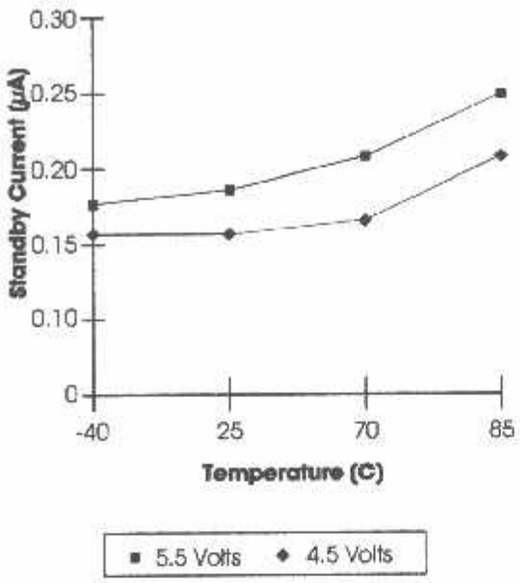


Chart 2: Total Harmonic Distortion

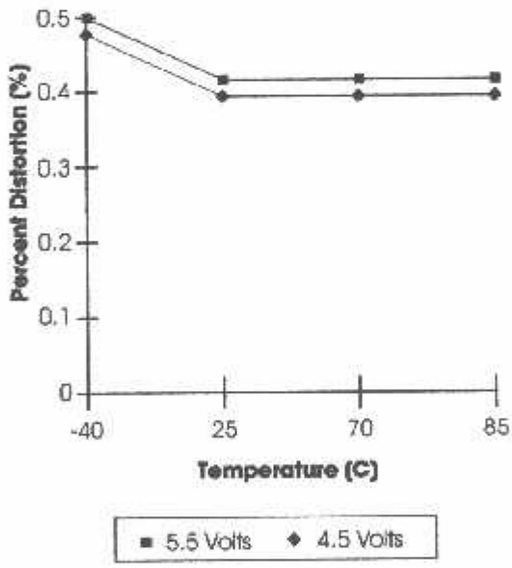


Chart 4: Oscillator Stability

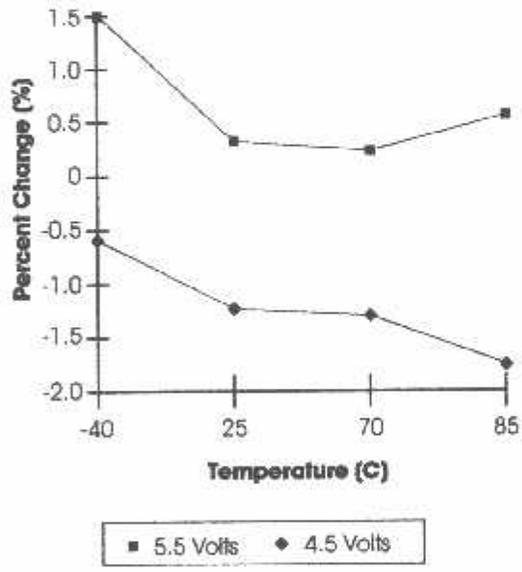


Table 8: Absolute Maximum Ratings (Die)[1]

Condition	Value
Junction temperature	150°C
Storage temperature range	–65°C to +150°C
Voltage applied to any pad	(V_{SS} – 0.3V) to (V_{CC} + 0.3V)
Voltage applied to any pad (Input current limited to ±20 mA)	(V_{SS} – 1.0 V) to (V_{CC} + 1.0 V)
$V_{CC} - V_{SS}$	–0.3 V to +7.0 V

1. *Stresses above those listed may cause permanent damage to the device. Exposure to the absolute maximum ratings may affect device reliability. Functional operation is not implied at these conditions.*

Table 9: Operating Conditions (Die)

Condition	Value
Commercial operating temperature range	0°C to +50°C
Supply voltage (V_{CC})[1]	+4.5 V to +6.5 V
Ground voltage (V_{SS})[2]	0 V

1. $V_{CC} = V_{CCA} = V_{CCD}$.
2. $V_{SS} = V_{SSA} = V_{SSD}$.

Table 10: DC Parameters (Die)

Symbol	Parameters	Min[2]	Typ[1]	Max[2]	Units	Conditions
V_{IL}	Input Low Voltage			0.8	V	
V_{IH}	Input High Voltage	2.4			V	
V_{OL}	Output Low Voltage			0.4	V	I_{OL} = 4.0 mA
V_{OH}	Output High Voltage	2.4			V	I_{OH} = –1.6 mA
I_{CC}	V_{CC} Current (Operating)		15	30	mA	V_{CC} = 5.5 V[3], R_{EXT} = ∞
I_{SB}	V_{CC} Current (Standby)		0.5	10	µA	[3] [4]
I_{IL}	Input Leakage Current			±1	µA	
I_{ILPD}	Input Current HIGH w/Pull Down			130	µA	Force V_{CC}[5]
R_{EXT}	Output Load Impedance	16			Ω	Speaker Load
R_{MIC}	Preamp In Input Resistance	4	9	17	KΩ	Pins 17, 18
$R_{ANA\ IN}$	ANA IN Input Resistance	2.5	3	5	KΩ	
A_{PRE1}	Preamp Gain 1	20	23	26	dB	AGC = 0.0 V
A_{PRE2}	Preamp Gain 2		–45	–15	dB	AGC = 2.5 V
A_{ARP}	ANA IN to SP+/– Gain	20	22	25	dB	

Table 10: DC Parameters (Die)

Symbol	Parameters	Min[2]	Typ [1]	Max[2]	Units	Conditions
R_{AGC}	AGC Output Resistance	2.5	5	9.5	KΩ	
I_{PREH}	Preamp Out Source		-2		mA	@ V_{OUT} = 1.0 V
I_{PREL}	Preamp In Sink		0.5		mA	@ V_{OUT} = 2.0 V

1. *Typical values @ T_A = 25°C and 5.0 V.*
2. *All Min/Max limits are guaranteed by ISD via electrical testing or characterization. Not all specifications are 100 percent tested.*
3. *V_{CCA} and V_{CCD} connected together.*
4. *$\overline{REC}$, $\overline{PLAYL}$, and $\overline{PLAYE}$ must be at V_{CCD}.*
5. *XCLK pin.*

Table 11: AC Parameters (Die)

Symbol	Characteristic		Min[2]	Typ [1]	Max[2]	Units	Conditions
F_S	Sampling Frequency	ISD1416 ISD1420			8 6.4	KHz KHz	(5) (5)
F_{CF}	Filter Pass Band	ISD1416 ISD1420		3.3 2.6		KHz KHz	3 dB Roll-Off Point [3][6] 3 dB Roll-Off Point [3][6]
T_{REC}	Record Duration	ISD1416 ISD1420	16 20			sec sec	
T_{PLAY}	Playback Duration	ISD1416 ISD1420	16 20			sec sec	(5) (5)
T_{LED1}	$\overline{RECLED}$ ON Delay			5		msec	
T_{LED2}	$\overline{RECLED}$ OFF Delay	ISD1416 ISD1420	30 40	38.9 48.6	95 110	msec msec	
T_{SET}	Address Setup Time		300			nsec	
T_{HOLD}	Address Hold Time		0			nsec	
T_{RPUD}	Record Power-Up Delay	ISD1416 ISD1420		26 32		msec msec	
T_{RPDD}	Record Power-Down Delay	ISD1416 ISD1420		26 32		msec msec	
T_{PPUD}	Play Power-Up Delay	ISD1416 ISD1420		26 32		msec msec	

Table 11: AC Parameters (Die)

Symbol	Characteristic		Min[2]	Typ [1]	Max[2]	Units	Conditions
T_{PPDD}	Play Power-Down Delay	ISD1416 ISD1420		6.5 8.1		msec msec	
T_{EOM}	EOM Pulse Width	ISD1416 ISD1420		12.5 15.625		msec msec	
THD	Total Harmonic Distortion			1	3	%	@ 1 KHz
P_{OUT}	Speaker Output Power			12.2		mW	R_{EXT} = 16 Ω
V_{OUT}	Voltage Across Speaker Pins			1.25	2.5	V p-p	R_{EXT} = 600 Ω
V_{IN1}	MIC Input Voltage				20	mV	Peak-to-Peak [4]
V_{IN2}	ANA IN Input Voltage				50	mV	Peak-to-Peak

1. *Typical values @ T_A = 25°C and 5.0 V.*
2. *All Min/Max limits are guaranteed by ISD via electrical testing or characterization. Not all specifications are 100 percent tested.*
3. *Low-frequency cutoff depends upon value of external capacitors (see Pin Descriptions).*
4. *With 5.1 KΩ series resistor at ANA IN.*
5. *Sampling frequency and playback duration will vary as much as ±2.25 percent over the commercial temperature and voltage ranges. All devices will meet the maximum sampling frequency and minimum playback duration parameters. For greater stability, an external clock can be utilized (see Pin Descriptions).*
6. *Filter specification applies to the antialiasing filter and to the smoothing filter.Typical Parameter Variation with Voltage and Temperature (Die).*

TYPICAL PARAMETER VARIATION WITH VOLTAGE AND TEMPERATURE (DIE)

Chart 5: Record Mode Operating Current (I_{CC})

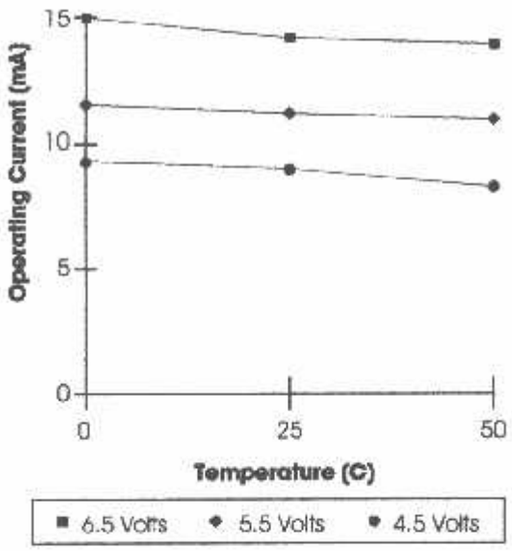


Chart 7: Standby Current (I_{SB})

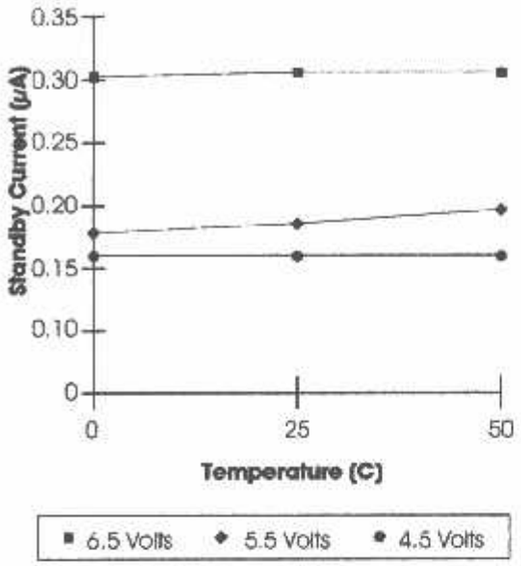


Chart 6: Total Harmonic Distortion

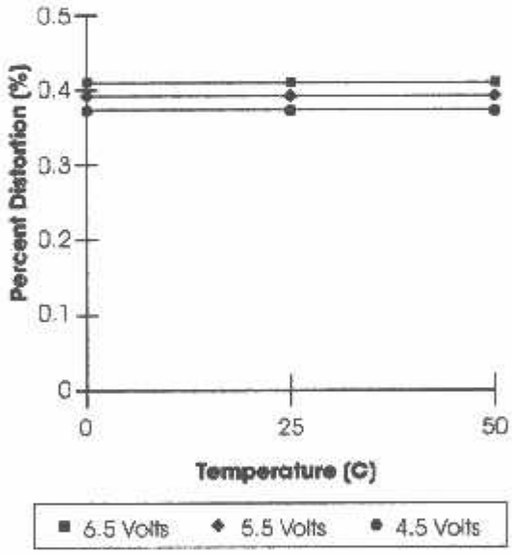


Chart 8: Oscillator Stability

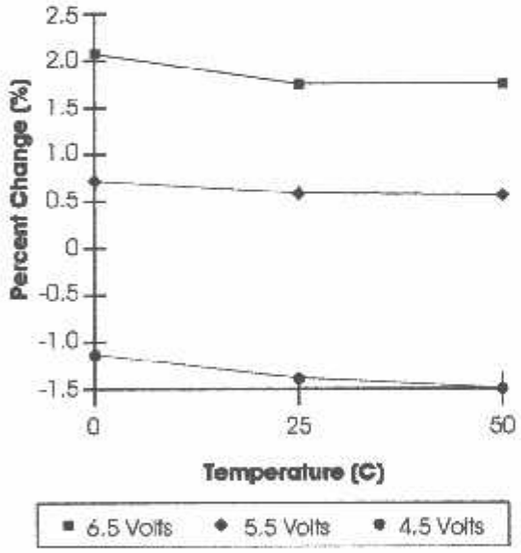
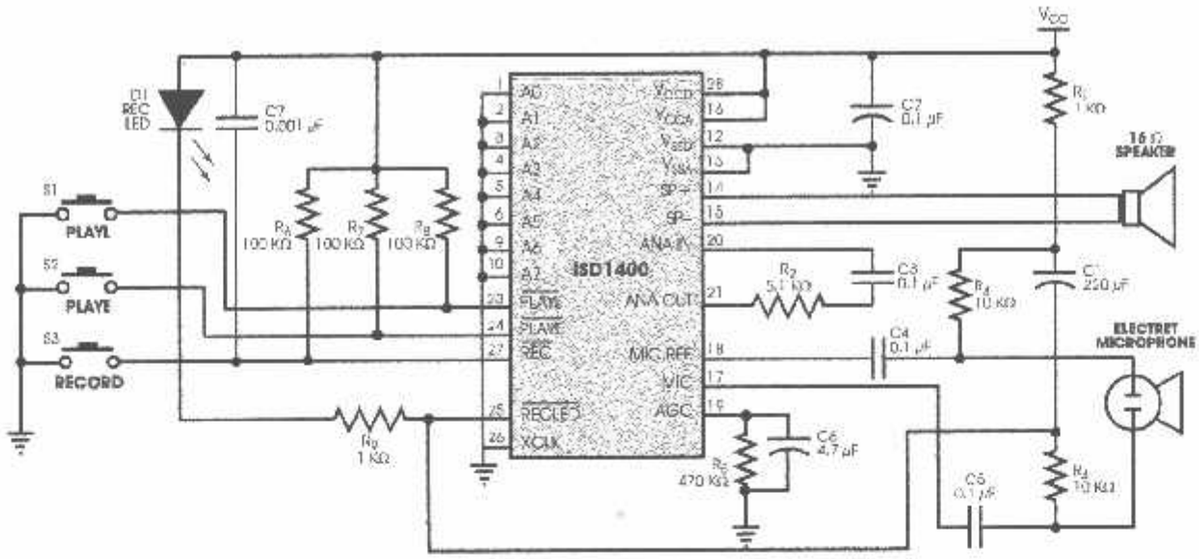


Figure 4: Application Example



FUNCTIONAL DESCRIPTION EXAMPLE

The following example operating sequence demonstrates the functionality of the ISD1400 series devices.

1. Record a message filling the address space.

   Pulling the $\overline{\text{REC}}$ signal LOW initiates a record cycle from the beginning of the message space. If $\overline{\text{REC}}$ is held LOW, the recording continues until the message space has been filled. Once the message space is filled, recording ceases. The device will automatically power down after $\overline{\text{REC}}$ is pulled HIGH.

2. Edge-activated playback.

   Pulling the $\overline{\text{PLAYE}}$ signal LOW initiates a playback cycle from the beginning of the message space or at a selected location. The rising edge of $\overline{\text{PLAYE}}$ has no effect on operation. If a recording has filled the message space, the entire message is played. When the device reaches the EOM marker, it automatically powers down. A subsequent falling edge on $\overline{\text{PLAYE}}$ initiates a new play cycle from the start address.

3. Level-activated playback.

   Pulling the $\overline{\text{PLAYL}}$ signal LOW initiates a playback cycle from the beginning of the message space or a selected location. If recording has filled the message space, the entire message is played. When the device reaches the EOM marker, it automatically powers down. A subsequent falling edge on $\overline{\text{PLAYL}}$ initiates a new play cycle from the starting address.

4. Level-activated playback (truncated).

   If $\overline{\text{PLAYL}}$ is pulled HIGH any time during the playback cycle, the device stops playing and enters the power-down mode. A subsequent falling edge on $\overline{\text{PLAYL}}$ initiates a new play cycle from the start address.

5. Record (interrupting playback).

   The $\overline{\text{REC}}$ signal takes precedence over other operations. Any LOW-going transition

on $\overline{REC}$ initiates a new record operation from the beginning of the start address or at a selected location, regardless of any current operation in progress.

6. Record a message, partially filling the address space.

   A record operation need not fill the entire message space. Releasing the $\overline{REC}$ signal HIGH before filling the message space causes the recording to stop and an EOM to be placed. The device powers down automatically.

7. Play back a message, partially filling the address space.

   Pulling the $\overline{PLAYE}$ or $\overline{PLAYL}$ signal LOW initiates a playback cycle which is then completed when the EOM marker is encountered. Playback ceases and the device powers down.

8. $\overline{RECLED}$ operation.

   The $\overline{RECLED}$ output pin provides an active-LOW signal which can be used to drive an LED as a "record-in-progress" indicator. It returns to a HIGH state when the $\overline{REC}$ pin is released HIGH or when the recording is completed due to the message space being filled. This pin also pulses LOW to indicate an EOM at the end of a message being played.

APPLICATIONS NOTE

Some users may experience an unexpected recording taking place when their circuit is powered up, or the batteries are changed and V_{CC} rises faster than $\overline{REC}$. This undesired recording prevents playback of the previously recorded message. A spurious End Of Message (EOM) marker appears at the very beginning of the memory, preventing access to the original message, and nothing is played.

To prevent this occurrence, place a capacitor (approx. 0.001 μF) between the control pin ($\overline{REC}$) and V_{CC}. This pulls the control pin voltage up with V_{CC} as it rises. Once the voltage is HIGH, the pull-up device will keep the pin HIGH until intentionally pulled LOW, preventing the false EOM marker.

Since this anomaly depends on factors such as the capacitance of the user's printed circuit board, not all circuit designs will exhibit the spurious marker. However, it is recommended that the capacitor is included for design reliability. A more detailed explanation and resolution of this occurrence is described in Application Information.

ISD1400 SERIES PHYSICAL DIMENSIONS

Figure 5: 28-Lead 0.600-Inch Plastic Dual Inline Package (PDIP) (P)

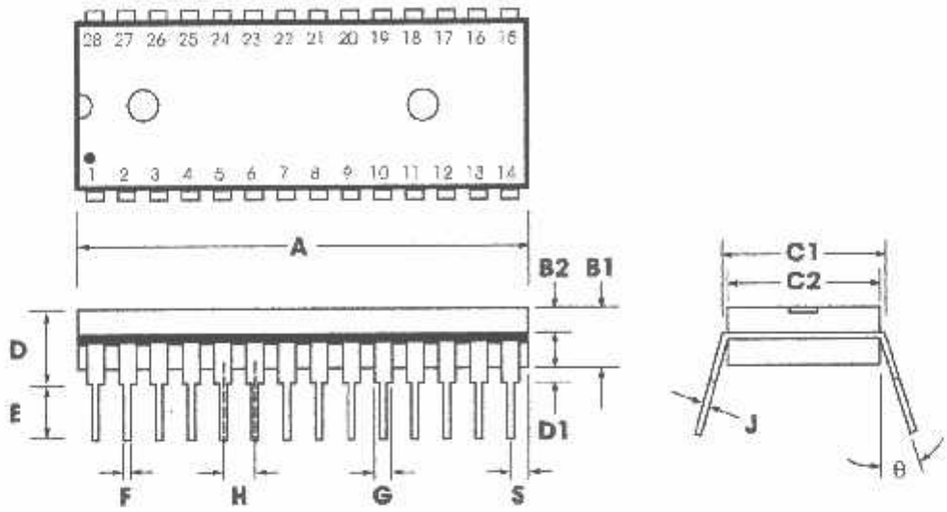


Table 12: Plastic Dual Inline Package (PDIP) (P) Dimensions

	INCHES			MILLIMETERS		
	Min	Nom	Max	Min	Nom	Max
A	1.445	1.450	1.455	36.70	36.83	36.96
B1		0.150			3.81	
B2	0.065	0.070	0.075	1.65	1.78	1.91
C1	0.600		0.625	15.24		15.88
C2	0.530	0.540	0.550	13.46	13.72	13.97
D			0.19			4.83
D1	0.015			0.38		
E	0.125		0.135	3.18		3.43
F	0.015	0.018	0.022	0.38	0.46	0.56
G	0.055	0.060	0.065	1.40	1.52	1.65
H		0.100			2.54	
J	0.008	0.010	0.012	0.20	0.25	0.30
S	0.070	0.075	0.080	1.78	1.91	2.03
q	0°		15°	0°		15°

NOTE: *Lead coplanarity to be within 0.005 inches.*

Figure 6: 28-Lead 0.300-Inch Plastic Small Outline Integrated Circuit (SOIC) (S)

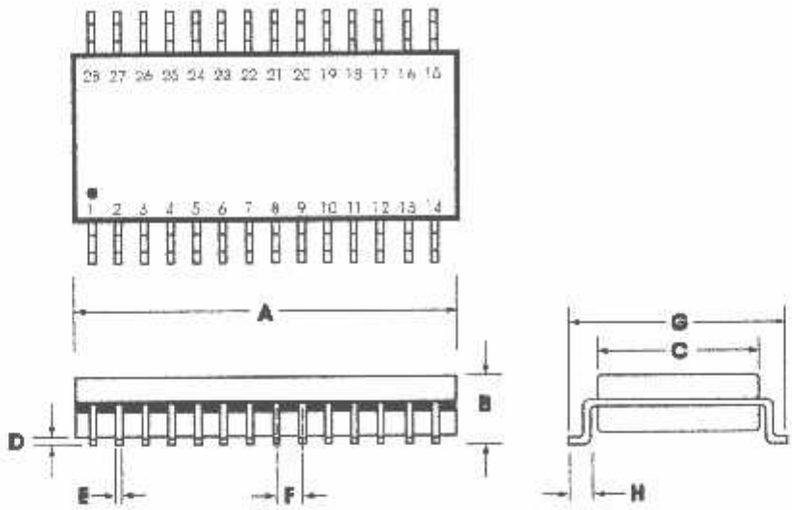


Table 13: Plastic Small Outline Integrated Circuit (SOIC) (S) Dimensions

	INCHES			MILLIMETERS		
	Min	Nom	Max	Min	Nom	Max
A	0.701	0.706	0.711	17.81	17.93	18.06
B	0.097	0.101	0.104	2.46	2.56	2.64
C	0.292	0.296	0.299	7.42	7.52	7.59
D	0.005	0.009	0.0115	0.127	0.22	0.29
E	0.014	0.016	0.019	0.35	0.41	0.48
F		0.050			1.27	
G	0.400	0.406	0.410	10.16	10.31	10.41
H	0.024	0.032	0.040	0.61	0.81	1.02

NOTE: *Lead coplanarity to be within 0.004 inches.*

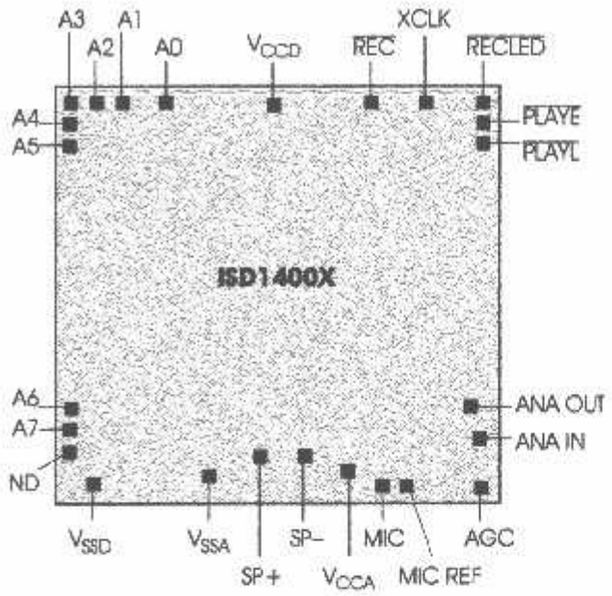
Figure 7: ISD1400 Series Bonding Physical Layout[1]

ISD1400X

I. Die Dimensions
X: 172.2 ±1 mils
Y: 168.5 ±1 mils

II. Die Thickness[2]
17.5 ±1 mils

III. Pad Opening
100 x 112 microns
3.9 x 4.4 mils



1. *The backside of die is internally connected to V_{SS}. It **MUST NOT** be connected to any other potential or damage may occur.*
2. *Die thickness is subject to change, please contact ISD factory for status.*

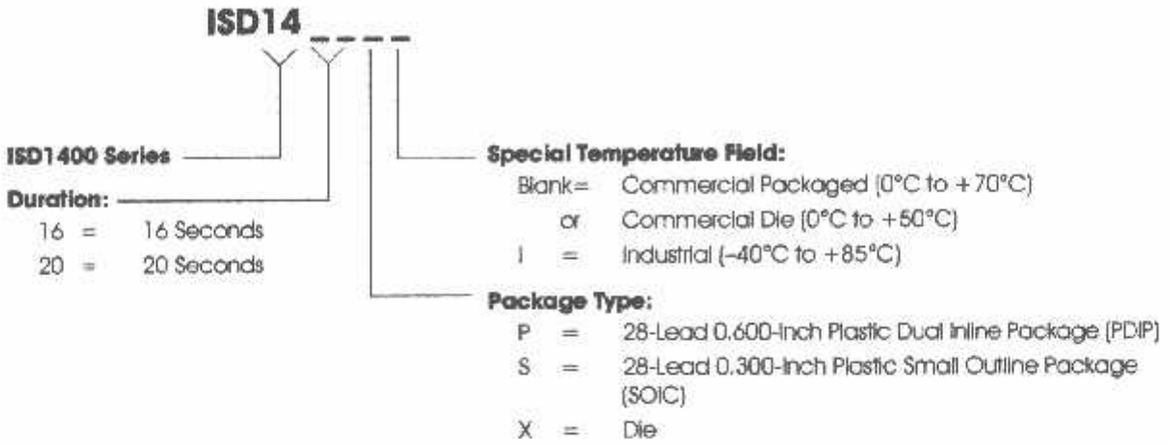
Table 14: ISD1400 Series PIN/PAD Designations, with Respect to Die Center (µm)

Pin	Pin Name	X Axis	Y Axis
A0	Address 0	-1332.5	1973.8
A1	Address 1	-1628.9	1973.8
A2	Address 2	-1808.9	1973.8
A3	Address 3	-2014.1	1910.2
A4	Address 4	-2014.1	1722.6
A5	Address 5	-2014.1	1519.8
A6	Address 6	-2014.1	-1214.6
A7	Address 7	-2014.1	-1399.8
NC	No Connect	-2014.1	-1745.4
V_{SSD}	V_{SS} Digital Power Supply	-1894.1	-1971.8
V_{SSA}	V_{SS} Analog Power Supply	-358.1	-1971.8
SP+	Speaker Output +	-17.7	-1896.6
SP-	Speaker Output -	411.9	-1896.6
V_{CCA}	V_{CC} Analog Power Supply	779.5	-1936.2
MIC	Microphone Input	991.5	-1973.8
MIC REF	Microphone Reference	1168.7	-1973.8
AGC	Automatic Gain Control	1977.9	-1910.6
ANA IN	Analog Input	2005.1	-1580.2
ANA OUT	Analog Output	1990.7	-1379.0
$\overline{PLAYL}$	Level-Activated Playback	2013.9	1608.6
$\overline{PLAYE}$	Edge-Activated Playback	2013.9	1777.0
$\overline{RECLED}$	Record LED Output	2011.9	1971.8
XCLK	No Connect (optional)	1580.7	1973.8
$\overline{REC}$	Record	752.3	1973.8
V_{CCD}	V_{CC} Digital Power Supply	-48.5	1929.4

NOTE: *Die dimensions and pin/pad positions may be subject to change. Please contact ISD Sales Offices or Representatives to verify current or future specifications.*

ORDERING INFORMATION

Product Number Descriptor Key



When ordering ISD1400 Series devices, please refer to the following valid part numbers.

Part Number	Part Number
ISD1416P	ISD1420P
ISD1416PI	ISD1420PI
ISD1416S	ISD1420S
ISD1416SI	ISD1420SI
ISD1416X	ISD1420X

For the latest product information, access ISD's worldwide website at http://www.isd.com.