INSTITUT TEKNOLOGI NASIONAL MALANG
FAKULTAS TEKNOLOGI INDUSTRI
JURUSAN TEKNIK ELEKTRO S-1
KONSENTRASI TEKNIK ELEKTRONIKA

SKRIPSI

PERANCANGAN DAN PEMBUATAN PAPAN SKOR PADA PANAHAN YANG DILENGKAPI DENGAN KELUARAN SUARA BERBASIS MIKROKONTROLLER AT89S8252

Disusun Oleh :
SETYO HADI PRAMONO
01.17.043

Maret 2006

LEMBAR PERSETUJUAN

PERANCANGAN DAN PEMBUATAN PAPAN SKOR PADA PANAHAN YANG DILENGKAPI DENGAN KELUARAN SUARA BERBASIS MIKROKONTROLLER AT89S8252

SKRIPSI

Disusun dan Diajukan Sebagai Salah Satu Syarat Untuk Memperoleh Gelar Sarjana Teknik Elektronika Strata Satu (S-1)

Disusun Oleh :

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JURUSAN TEKNIK ELEKTRO S-1
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FAKULTAS TEKNOLOGI INDUSTRI
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2006

INSTITUT TEKNOLOGI NASIONAL
FAKULTAS TEKNOLOGI INDUSTRI
JURUSAN TEKNIK ELEKTRO S-1
PROGRAM STUDI TEKNIK ELEKTRONIKA
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بسم الله الرحمن الرحيم

"Dengan Menyebut Nama Allah Yang Maha Pengasih Lagi Maha Penyayang"

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"La Qaula Walla Quwwata Illah Billahil Aliyil Adzim "

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"YOO WiSSS!!!!!!"

BY : EYO' 01

ABSTRAKSI

PERANCANGAN DAN PEMBUATAN PAPAN SKOR PADA PANAHAN YANG DILENGKAPI DENGAN KELUARAN SUARA BERBASIS MIKROKONTROLLER AT89S8252

(Setyo Hadi Pramono, 01.17.043, Jurusan Teknik ElektroS-1/Elektronika)

(Dosen Pembimbing : Ir. F.Yudi Limpraptono, MT)

Kata kunci: Mikrokontroler AT 89S8252, Papan Skor, Tampilan, suara.

Papan skor yang dilengkapi dengan keluaran angka dan suara untuk olah raga panahan yang mampu mengeluarkan nilai melalui display seven segmen dan keluaran suara melalui speaker yang dapat dilihat dan didengar langsung oleh pemanah maupun panitia. Dengan dibuatnya alat ini maka diharapkan dapat membantu panitia untuk pencatatan skor yang di peroleh pemanah secara langsung dan tidak mondar mandir dilapangan sehingga menghambat jalannya perlombaan.

Sistem ini menggunakan Mikrokontroller AT89S8252 sebagai basisnya. Alat yang dibuat meliputi perencanaan perangkat keras dan perangkat lunak. Perencanaan perangkat keras meliputi: papan panahan, rangkaian display seven segmen, rangkaian ISD, rangkaian penguat audio, rangkaian serial, minimum sistem Mikrokontroller AT89S8252.

Dari hasil pengujian sampel lemparan anak panah ke papan skor sebanyak 45 kali maka dapat diketahui bahwa jumlah yang sukses 39 kali sehingga didapat kesalahan dalam pengujian ini sebesar 6 kali dengan jarak 3-5 m. Kesalahan ini dapat terjadi karena beberapa hal, antara lain jarak antara pelemparan anak panah pada papan target, kekuatan tekanan, maupun faktor kesalahan manusia yang terjadi dalam penggunaan alat ini. Dari hasil pengujian maka dapat dikatakan sistem bekerja sesuai dengan yang direncanakan. Dalam perancangan ini kami berharap agar alat ini dapat bermanfaat membantu memudahkan pencatatan skor pada olah raga panahan.

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Atas Berkat Rahmat Allah Yang Maha Kuasa, sehingga penulis dapat menyelesaikan laporan Skripsi dengan judul :

" PERANCANGAN DAN PEMBUATAN PAPAN SKOR PADA PANAHAN YANG DILENGKAPI DENGAN KELUARAN SUARA BERBASIS MIKROKONTROLLER AT89S8252 "

Pembuatan Skripsi ini disusun guna memenuhi syarat akhir kelulusan pendidikan jenjang Strata-1 di Institut Teknologi Nasional Malang. Laporan Skripsi ini merupakan tanggung jawab tertulis atas ilmu pengetahuan yang didapat selama penyusun mengikuti kuliah.

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Malang, Maret 2006

Penulis

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BAB I

PENDAHULUAN

1.1 Latar belakang

Dalam era globalisasi dan modern sekarang ini, kemajuan di bidang teknologi telah menjadi alternatif utama. Teknologi berkembang dengan pesat dalam kehidupan bermasyarakat, karena itu kita dituntut untuk mengikuti perkembangan tersebut. Salah satunya ialah dengan cara pembuatan papan skor pada olah raga panahan yang dilengkapi dengan output suara.

Saat ini papan skor pada olah raga panahan bisa dibilang masih bersifat konvensional, hal ini dikarenakan waktu melihat skor pada panahan masih manual yaitu panitia dan pemanah jalan ke tempat papan panahan, Sehingga pemanah lain tidak bisa melihat skor secara langsung dan panitia tidak usah mondar-mandir melihat skor pemanah satu ke satu pemanah yang lain.

Untuk menanggulangi hal tersebut maka direncanakan dan dibuat suatu alat yang dapat menampilkan skor secara langsung sekaligus dengan mengeluarkan suara dari skor yang di dapat pemanah yang tertera pada papan skor.

1.2 Rumusan Masalah

Dalam pembuatan papan skor pada olah raga panahan yang dilengkapi dengan output suara dibutuhkan sarana hardware dan software

Dari Hardware :

- Membuat papan tembakan untuk olah raga panahan yang dilengkapi dengan sensor tekanan untuk data inputan.

- Membuat perangkat keras dari mikrokontroller AT89C8252 yang berfungsi sebagai pengolah data dari inputan sensor tekanan yang akan ditampilkan pada Seven Segment dan pengontrolan suara yang akan dikeluarkan oleh ISD serta untuk mengendalikan rangkaian-rangkaian yang dihubungkan dengan mikrokontroler tersebut.

Dari software:

- Membuat program yang berfungsi sebagai pengolahan data-data yang diterima melalui sensor tekanan untuk ditampilkan pada Seven Segment dan pengendalian dari suara yang akan dikeluarkan oleh ISD.

1.3 Tujuan

Tujuan dari penulisan skripsi ini adalah untuk membuat suatu alat yang dapat menampilkan skor pada olah raga panahan yang dilengkapi dengan suara dari skor yang di peroleh pemanah sehingga informasi tersebut dapat dilihat dan didengar oleh semua pemanah lain dan disampaikan dengan mudah. Dan panitia hanya melihat dan mendengar hasilnya dan menulis pada lembar penilaian/ skor yang di peroleh pemanah.

1.4 Batasan Masalah

Agar permasalahan tidak meluas, maka skripsi ini akan dibatasi hanya pada hal-hal berikut ini:

1. Bahasa pemprograman yang digunakan adalah bahasa C dengan SDCC (Small Device C Compiler) untuk minimum sistem AT 89S8252.
2. Menampilkan hasil penilaian panahan pada display segmen dan output suara dari ISD.
3. Alat ini hanya terbatas pada Prototype saja dan tidak menekankan bagaimana olah raga panahan secara sesungguhnya.
4. Sistem penilaian alat ini hanya menekankan pada ketepatan sasaran tembakan.
5. Pemanah melakukan 6 kali tembakan.
6. Tidak membahas catu daya.

1.5 Metodologi

1. Metodologi Studi Literature, meliputi :
   - Mempelajari bahasa C dengan SDCC (Small Device C Compiler) untuk minimum sistem AT 89S8252.
   - Mempelajari karakteristik dari ISD yang digunakan.
   - Mempelajari penilaian olah raga panahan.
2. Pengumpulan data, meliputi :

   Karakteristik dari sensor tekanan, mikrokontroler, rangkaian penguat, ISD dan seven segment.
3. Analisa Perancangan

   Rancangan dari tugas akhir yang di buat terdiri dari:

- Sensor tekanan sebagai inputan yang akan diolah oleh mikrokontroler dan ditampilkan ke seven segment dan ISD.
- Penggunaan ISD sebagai output suara yang akan dikeluarkan sehingga data yang dimasukkan sama dengan keluaran dari suara yang dihasilkan dari ISD yang telah direkam sebelumnya.

4. Pembuatan Alat

   Dalam hal ini alat yang akan dibuat adalah sebagai berikut :

   - Membuat parangkat keras papan tembakan untuk olah raga panahan.
   - Membuat perangkat keras dan lunak untuk mikrokontroler AT89S8252 sebagai pengolah data inputan untuk tampilkan pada Seven Segment dan pengontrol keluaran suara dari ISD.

5. Pengujian Alat

   Pengujian dan pemrograman alat dilakukan saat mencapai tahap akhir untuk menemukan kesalahan atau kekurangan pada program dan alat tersebut untuk selanjutnya dilakukan perbaikan.

1.6 Sistematika Penulisan

Sistematika penulisan dari tugas akhir ini adalah sebagai berikut :

- BAB I : Pendahuluan

  Membahas tentang latar belakang permasalahan, tujuan dan manfaat, batasan masalah, metodologi, dan sistematika penulisan.

- BAB II : Teori Penunjang

  Merupakan teori penunjang dari alat dan program yang dibuat

- BAB III : Perancangan dan Pembuatan Program dan Alat

  Membahas tentang perancangan alat dan program yang digunakan, mulai dari pembuatan hardware, software, ISD dan cara kerja alat.

- BAB IV : Pengujian Program dan Alat

  Membahas pengujian dari program dan alat yang telah selesai dengan menjalankan program tersebut dan mengamati hasilnya.

- BAB VI : Kesimpulan

  Membahas tentang kesimpulan dari hasil perancangan

BAB II

TEORI PENUNJANG

Landasan teori ini sangat membantu untuk dapat memahami suatu sistem. Disamping itu dapat juga dijadikan sebagai bahan acuan didalam merencanakan suatu sistem. Dengan pertimbangan hal-hal tersebut maka landasan teori merupakan bagian yang harus dipahami untuk pembahasan selanjutnya.

2.1 Mikrokontroler AT89S8252

Mikrokontroler AT89S8252 merupakan mikrokontroler 8 bit kompatibel dengan Standar industri MCS-51™ baik atas segi pemrograman maupun kaki tiap pin. Mikrokontroler AT89S8252 menpunyai 8 *Kby (FlashProgrammable and Read Only Memori*) pada dasarnya mikrokontroler adalah terdiri atas mikroprosesor, *timer*, dan *counter*, perangkat I/O dan internal memori. Mikrokontroler termasuk perangkat yang sudah didesain dalam chip tunggal.

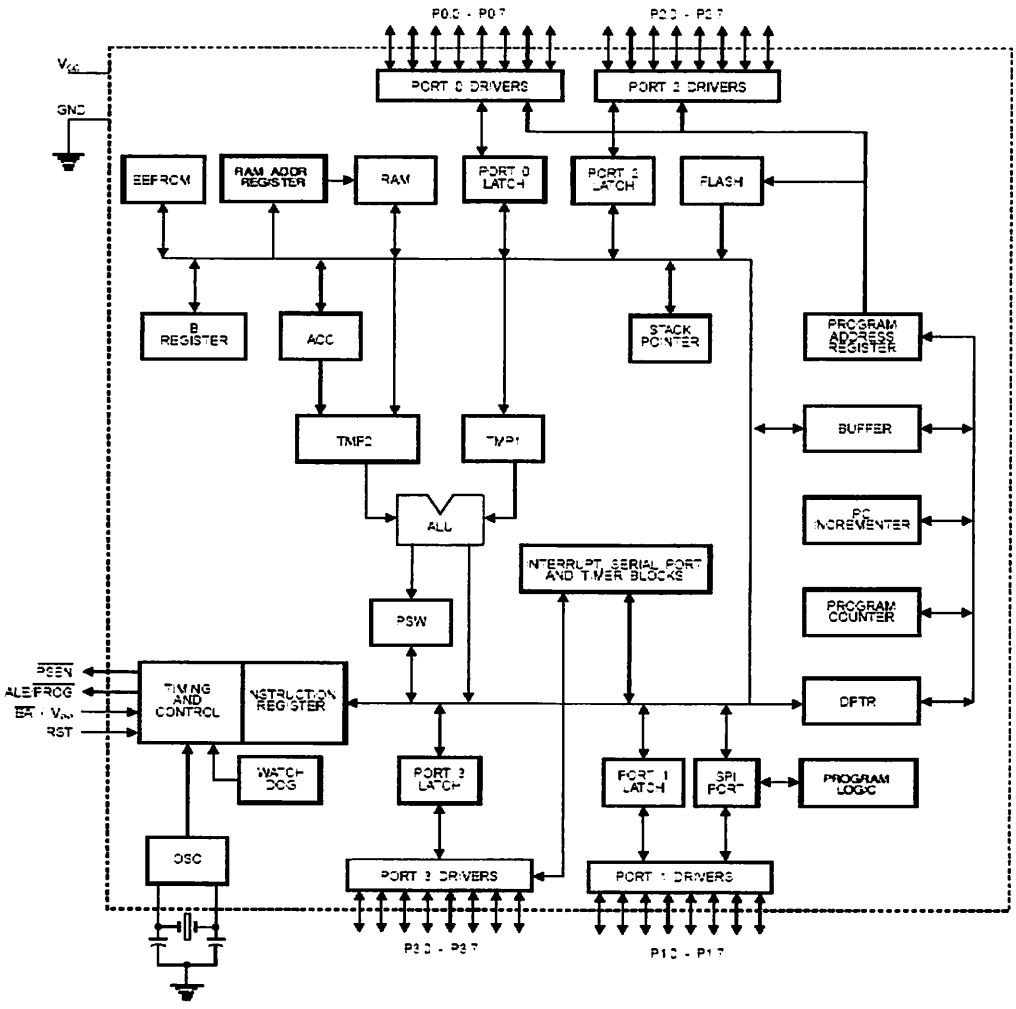
Pada dasarnya mikrokontroler mempunyai fungsi yang sama dengan mikroprosesor yaitu untuk mengontrol suatu kerja system. Selain itu mikrokontroler juga dikemas dalam satu *chip* (*single chip*). Didalam mikrokontroler juga terdapat CPU, ALU, PC, SP, dan register seperti dalam mikroprosesor, tetapi juga ditambah dengan perangkat-perangkat lain seperti ROM, RAM, PIO, SIO, *counter* dan sebuah rangkaian *clock*. Mikroprosesor didesain dengan intruksi-intruksi lebih luas dan 8 bit instruksi yang digunakan membaca data instruksi dari internal memori ke ALU. Sebagai suatu system

control mikrokontroler bila dibandingkan dengan mikroprosesor memiliki kemampuan dan segi ekonomis yang bisa diandalkan karena dalam mikrokontroler sudah terdapat RAM dan ROM. Sedangkan mikroprosesor didalamnya tidak terdapat keduanya. Terlihat bahwa mikrokontroler Atmel AT89S8252 memilki banyak fitur yang menguntungkan. Dipakainya downloadable flash memori memungkinkan mikrokontroler ini bekerja sendiri tanpa diperlukan tambahan chip lainya. Sementara Flash memorinya mampu diprogram hingga seribu kali. Hal lain yang menguntungkan adalah system pemrograman menjadi lebih sederhana dan tidak memerlukan rangkaian yang rumit seperti rangkaian untuk memprogram produk Atmel lainya. Secara umum konfigurasi yang dimiliki mikrokontroler AT89S8252 adalah sebagai berikut : *(Atmel, 1997:4-105)*

- Sebuah CPU 8 bit dengan menggunakan teknologi dari Atmel.
- 8K byte Downloadable Flash Memori.
- 2K byte EEPROM
- Sebuah *port* serial dengan control *full duplex* UART (Universal Asynchronous Receiver Transmiter.
- 256 byte RAM internal.
- 32 I/O yang dapat dipakai semua.
- 3 buah Timer/Counter 16 bit .
- SPI Serial Interface.
- Programmable Watchdog Timer .
- Dual Data Pointer.
- Frekuensi kerja 0 sampai 24 MHz

- Tegangan operasi 2,7 Volt sampai 6Volt.
- Kemampuan melaksanakan operasi perkalian, pembagian, dan operasi *Bolean* (bit)

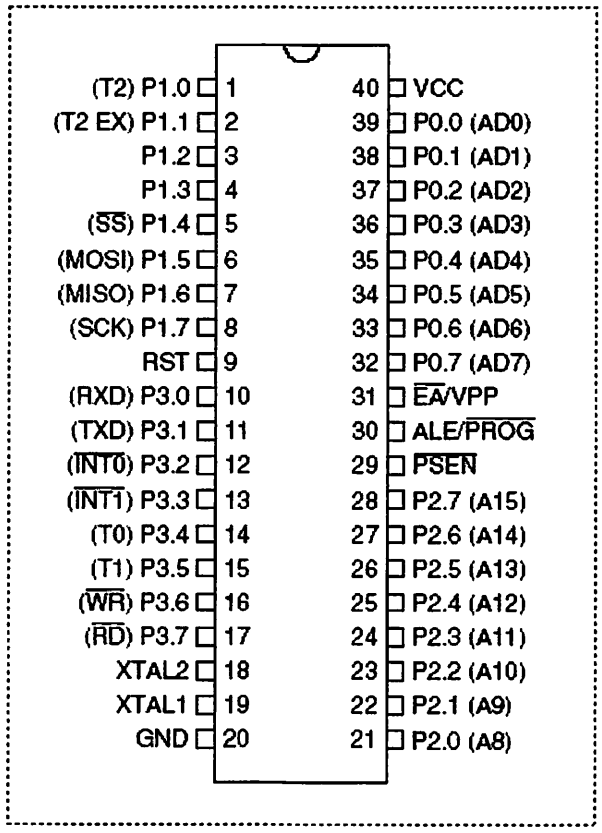
Sedangkan untuk blok diagram AT89S8252 diperlihatkan dalam gambar 2.1



Gambar 2.1 Blok Diagram AT89S8252[1]

2.1.1. Penjelasan Fungsi Pin AT89S8252

Mikrokontroler AT89S8252 mempunyai 40 pin seperti yang ditunjukkan dalam gambar 2-2 Fungsi-fungsi pin dijelaskan sebagai berikut :



Gambar 2.2 Susunan Pin AT89S8252[1]

- Pin 1 sampai 8

  Port 1 yang terdiri atas pin 1 sampai 8 merupakan saluran masukan/keluaran dua arah.

- Pin 9

  RST merupakan saluran dua masukan untuk me*reset* mikrokontroler dengan cara memberi masukan logika tinggi.

- Pin 10 sampai 17

  Port 3 yang terdiri atas pin 10 sampai pin 17 merupakan saluran masukan/keluaran dua arah dan mempunyai fungsi khusus seperti yang terlihat dalam tabel 2.1

- Pin 18 dan 19

  $XTAL_1$ dan $XTAL_2$ merupakan saluran untuk mengatur pewaktuan system. Untuk pewaktuan dapat menggunakan pewaktuan internal maupun eksternal .

- Pin 20

  Vss merupakan hubungan ke *ground* dari rangkaian.

- Pin 21 sampai 28

  Port 2 yang terdiri atas pin 21 sampai 28 merupakan saluran masukan/keluaran dua arah. *Port* ini mengeluarkan 8 bit bagian alamat tinggi (A8-A15) selama pengambilan instruksi dari memori program eksternal dan pengambilan data memori eksternal yang menggunakan mode pengalamatan 16 bit.

- Pin 29

  PSEN (*Program Store Enable*) merupakan sinyal baca untuk mengaktifkan memori program eksternal.

- Pin 30

  ALE/PROG (*Address Latch Enable*) merupakan pulsa yang berfungsi untuk menahan alamat rendah (A0-A7) dalam *port* 0, selama proses baca/tulis memori eksternal. Frekuensi ALE adalah 1/6 kali rekuensi osilator, dan digunakan sebagai pewaktu. Pin ini juga berfungsi sebagai saluran program selama dilakukan pemrograman jika menggunakan memori program eksternal.

- Pin 31

  EA/VPP (External Access Enable) untuk mengatur penggunaan memori program eksternal dan internal. Pin ini harus dihubungkan dengan ground bila menggunakan memori program eksternal dan dihubungkan dengan VPP sebesar 12 Volt jika menggunakan memori program eksternal.

- Pin 32 sampai 39

  Port 0 yang terdiri atas pin 32 sampai 39 merupakan saluran masukan/keluaran. *Port* 0 merupakan saluran alamat rendah (A0-A7) yang dimultipleks dengan saluran *bus* data (D0-D7).

- Pin 40

  Vcc merupakan saluran masukan untuk catu daya positi sebesar 5 Volt DC dengan toleransi kurang lebih 10 %.

2.1.2. Masukan dan Keluaran

Untuk saluran dan keluaran terdapat 4 buah *port* yang masing-masing 8 bit. Saluran ini bersifat dua arah (*bidirectional*) yang berarti dapat difungsikan sebagai masukan atau keluaran, serta dapat dialamati per bit. *Port* 3 selain digunakan sebagai *port* masukan dan keluaran juga dapat digunakan sebagai fungsi pengganti sebagaimana yang terdapat dalam tabel 2-1. Sedangkan AT89S8252 memiliki fitur tambahan yang terdapat pada *port 1* seperti pada tabel 2-2.

Tabel 2.1 Fungsi Pengganti Port 3[1]

Port Pin	Alternate Functions
P3.0	RXD (serial input port)
P3.1	TXD (serial output port)
P3.2	$\overline{\text{INT0}}$ (external interrupt 0)
P3.3	$\overline{\text{INT1}}$ (external interrupt 1)
P3.4	T0 (timer 0 external input)
P3.5	T1 (timer 1 external input)
P3.6	$\overline{\text{WR}}$ (external data memory write strobe)
P3.7	$\overline{\text{RD}}$ (external data memory read strobe)

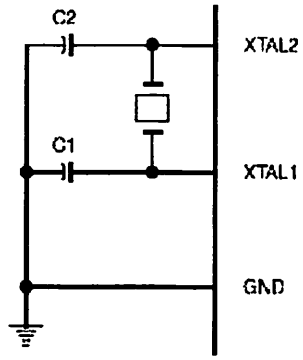
Tabel 2.2 Fungsi khusus pada port AT89S8252[1]

Port Pin	Alternate Functions
P1.0	T2 (external count input to Timer/Counter 2), clock-out
P1.1	T2EX (Timer/Counter 2 capture/reload trigger and direction control)
P1.4	$\overline{\text{SS}}$ (Slave port select input)
P1.5	MOSI (Master data output, slave data input pin for SPI channel)
P1.6	MISO (Master data input, slave data output pin for SPI channel)
P1.7	SCK (Master clock output, slave clock input pin for SPI channel)

2.1.3. Osilator

Jantung dari AT89S8252 adalah rangkaian yang membangkitkan pulsa clock yang mesinkronkan semua operasi internal. Mikrokontroler AT89S8252 memiliki osilator internal (*on chip oscillator*) yang dapat digunakan sebagai sumber pewaktu (*clock*) bagi CPU. Untuk menggunakan internal diperlukan

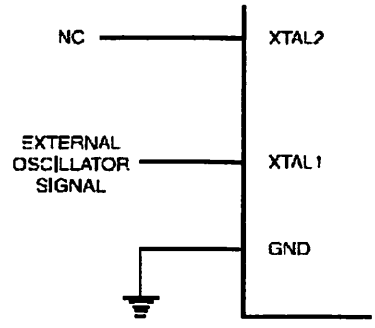
sebuah kristal atau resonator keramik antara pin XTAL1 dan pin XTAL2 dan sebuah kapasitor ke ground. Konfigurasinya dapat dilihat pada gambar berikut.



Gambar 2.3 Konfigurasi Osilator Menggunakan Kristal[1]

Nilai C1 dan C2 adalah 10 pF – 30 pF bila menggunakan kristal, dan bernilai 10 pF – 40 pF bila menggunakan resonator keramik.

Untuk penggunaan dengan external clock, XTAL2 harus dibiarkan dalam kondisi tidak terhubung. Konfigurasinya dapat dilihat pada gambar berikut ini :

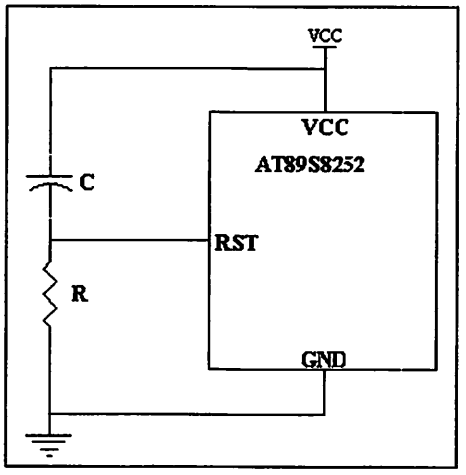


Gambar 2.4

Konfigurasi Osilator Menggunakan External Oscilator Signal[1]

2.1.4. Reset

Rangkaian *power on reset* diperlukan untuk m*ereset* mikrokontroler secara otomatis setiap catu daya *on*. Gambar 2.5 menunjukkan rangkaian *power on reset*. Ketika catu daya diaktifkan, rangkaian *reset* menahan logika tinggi pin RST dengan jangka waktu yang ditentukan oleh besarnya pengisian muatan C.



Gambar 2.5 Rangkaian Power On Reset[1]

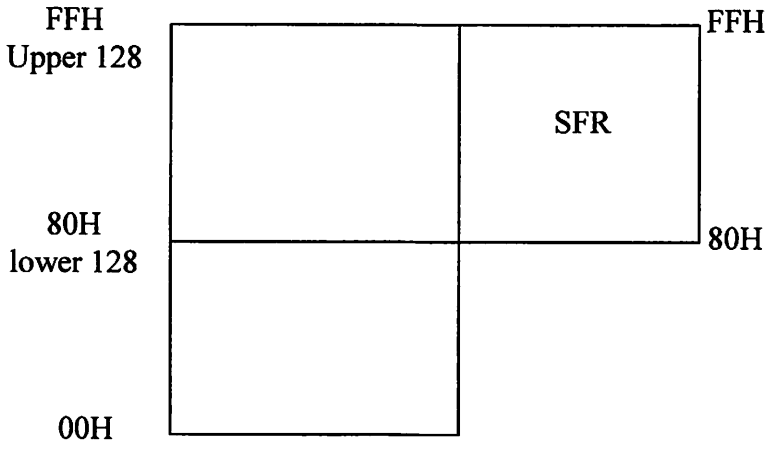
2.1.5. Data Memori (EEPROM) Dan RAM

Berbeda dengan mikrokontroler standard MCS-51, mikrokontroler Atmel AT89S8252 juga dilengkapi dengan data memori yang berupa EEPROM (*Electrically Erasable Programmable Read Only Memory*). EEPROM yang dimaksud ini besarnya 2 *klo byte* (2K) dan dipakai untuk penyimpanan data.

EEPROM *on-chip* ini diakses dengan mengeset bit EEMEN pada register WMCON pada alamat 96H. Alamat EEPROM ini adalah 000H sampai 7FFH. Intruksi move digunakan untuk mengakses EEPROM internal ini. Bit EEMWE pada register WMCON harus diset ke-1 sebelum seberang lokasi pada EEPROM dapat ditulisi. Program pengguna harus *mereset* bit EEMWE ke '0'jika proses

penulisan ke EEPROM tidak diperlukan lagi. Proses penulisan ke EEPROM dapat dilihat dengan membaca bit RDY/BSY pada SFR WMCON. Jika bit ini berlogika rendah maka berarti penulisan EEPROM sedang berlangsung, jika bit ini berlogika tinggi berarti penulisan sudah selesai dan penulisan lain dapat dimulai lagi.

Sedangkan RAM yang ada pada mikrokontroler AT89S8252 adalah berkapasitas 256 *byte* dan kompatibel dengan RAM yang ada pada mikrokontroler standard MCS-51.



Gambar 2.6 Memori Data Eksternal[1]

Pada *lower* 128 lokasi memori dibagi menjadi 3 bagian :

1. Register bank 0 – 3

   Lokasi bank register dimulai dari alamat 00H – 1 H yang terdiri dari 32 *bytes*. Register bank ini terdiri dari 4 buah register 8 bit yang dapat dipilih melalui pengaturan *program status word* register.

2. Bit *Addressing*

   Terdiri dari 16 *bytes* yang dimulai dari 20H – 2FH. Masing-masing dari 128 bit lokasi ini dapat dialamati secara langsung yaitu dari 00H sampai 7FH.

3. *Scratch Pad Area*

   Lokasi dari alamat 30H – 7FH atau sebanyak 80 *bytes* yang dapat digunakan sebagai alamat bagi RAM.

2.1.6. Special Function Register (SFR)

Special Function Register merupakan register dengan tugas khusus. SFR pada mikrokontroler AT89S8252 kompatibel dengan mikrokontroler keluarga MCS-51 dan memiliki alamat 80H - FFH sehingga terdapat 128 lokasi alamat untuk SFR. Namun demikian pada mikrokontroler ini tidak berarti memiliki SFR sebanyak 128 buah. Berikut ini adalah gambar letak dari lokasi alamat SFR.

0F8H									0FFH
0F0H	B 00000000								0F7H
0E8H									0EFH
0E0H	ACC 00000000								0E7H
0D8H									0DFH
0D0H	PSW 00000000					SPCR 000001XX			0D7H
0C8H	T2CON 00000000	T2MOD XXXXXX00	RCAP2L 00000000	RCAP2H 00000000	TL2 00000000	TH2 00000000			0CFH
0C0H									0C7H
0B8H	IP XX000000								0BFH
0B0H	P3 11111111								0B7H
0A8H	IE 0X000000		SPSR 00XXXXXX						0AFH
0A0H	P2 11111111								0A7H
98H	SCON 00000000	SBUF XXXXXXXX							9FH
90H	P1 11111111						WMCON 00000010		97H
88H	TCON 00000000	TMOD 00000000	TL0 00000000	TL1 00000000	TH0 00000000	TH1 00000000			8FH
80H	P0 11111111	SP 00000111	DP0L 00000000	DP0H 00000000	DP1L 00000000	DP1H 00000000	SPDR XXXXXXXX	PCON 0XX00000	87H

Gambar 2.7 AT89S8252 SFR Map dan Reset Value[1]

Selain itu mikrokontroler AT89S8252 memiliki tambahan SFR . Hal ini tak lain adalah karena terdapatnya tambahan fitur pada mikrokontroler ini. SFR tambahan ini meliputi : T2CON (Timer 2 Register dengan alamat 0C8H), T2MOD (Timer 2 Mode dengan alamat 0C9H), WMCON (*Watcdog and Memory Control* Register dengan alamat 96H), SPCR (SPI *Control* Register dengan alamat D5H), SPSR (SPI Status Register dengan alamat AAH), SPDR (SPI Data Register dengan alamat 86H).

- SFR untuk Timer 2

  Mikrokontroler AT89S8252 terdapat tambahan sebuah Timer/Counter yang diberi nama timer 2 (sehingga AT89S8252 memiliki 3 Timer /Counter yaitu Timer/Counter 0, Timer/Counter 1, Timer/Counter 2). Pada Timer/Counter 2 ini dikendalikan oleh *Special Function* Register yang bernama T2CON (Timer 2 Control), T2MOD (Timer @ MODE) dan sepasang register RCAP2H, RCAP2L merupakan register *capture/reload* untuk Timer 2 dalam 16 bit *capture mode/auto reload mode.*

- SFR untuk *Watchdog* Memori.

  Untuk menggunakan *Watchdog* timer atau memori, maka dapat dilakukan dengan mengatur SFR yang bernama WMCON dengan alamat 96H.

- SFR pengontrol SPI

  Berbeda dengan mikrokontroler MCS-51, AT89S8252 memiliki fasilitas SPI (*Serial Perpheral Interface*). Fasilitas ini memungkinkan transfer data kecepatan tinggi secara sinkron antara mikrokontroler dengan peripheral atau antar mikrokontroler AT89S8252. Fitur ini meliputi :

a. Full Duplek, 3 kawat dengan transfer data secara sinkron .

b. Operasi Master atau Slave.

c. Frekuensi maksimum 6 MHz.

d. 4 bit rate terprogram.

2.1.7. Timer dan Counter

Dalam mikrokontroler AT89S8252 terdapat tiga buah pewaktu/pencacah (timer/counter 16) 16 bit yang dapat diatur melalui perangkat lunak, yaitu pewaktu / pencacah 0 dan pewaktu / pencacah 1. Timer/counter ini diatur oleh *special function* register yaitu Timer/Counter *Control* (TCON alamat 88H), dan Timer/Counter Mode *Control* (TMOD alamat 89H). Selain itu nilai byte bawah dan byte atas dari Timer/Counter disimpan dalam register TL dan TH.

Jika difungsikan sebagai Timer, maka akan menggunakan system clock sebagai sumber masukan pulsanya. Jika sebagai Counter (pencacah), maka akan menggunakan pulsa dari luar (eksternal) sebagai masukan pulsanya. Pada Port 3 terdapat fungsi khusus yaitu TO (masukan luar untuk Timer/Counter 0) dan T1 (masukan luar untuk Timer/Counter 1). Pemilihan mode Timer/Counter dikontrol oleh register TMOD. Dengan memberikan nilai tertentu pada register TMOD dapat dipilih mode operasi untuk Timer/Counter 0 dan Timer/Counter 1 seperti terlihat dalam Tabel 2.3.

Tabel 2.3 Mode Operasi Timer/Counter 0 dan 1[1]

Mode	Timer/Counter 0	Timer/Counter 1
0	13 bit Timer	13 bit Timer
1	16 bit Timer	16 bit Timer
2	8 bit auto-reload	8 bit auto-reload
3	28 bit timer	Tidak bekerja

Pada mikrokontroler AT89S8252 terdapat tambahan Timer 2. Timer yang lain adalah Timer 0 dan Timer 1. Timer 2 ini merupakan Timer/Counter 16 bit dan memiliki 3 mode operasi yaitu *capture, auto reload* (*up down counting*) dan baud rate generator. Untuk memilih mode ini dilakukan dengan mengatur bit pada SFR T2CON (Timer 2 Control Register). Timer 2 ini terdiri dari 2 buah timer 8 bit register yaitu TH2 dan TL2. pada fungsi Timer, register TL2 dinaikkan (increment) tiap siklus mesin. Karena siklus mesin terdiri dari 12 periode osilasi, maka count rate menjadi 1/12 dari frekuensi osilator. Sedangkan pada fungsi Counter, register dinaikkan berdasarkan tanggapan adanya transisi tinggi ke rendah pada pena yang bersesuaian (dalam hal ini pin T2 atau P1.0). Tabel berikut menunjukkan mode operasi yang dapat dijalankan pada timer 2.

Tabel 2.4 Mode Operasi Timer 2[1]

RCLK + TCLK	CP/$\overline{RL2}$	TR2	MODE
0	0	1	16-bit Auto-reload
0	1	1	16-bit Capture
1	X	1	Baud Rate Generator
X	X	0	(Off)

RCLK = Receive clock enable. Jika diset menyebabkan serial port menggunakan pulsa overflow Timer 2 sebagai detak penerimaan pada serial port. Jika RCLK = 0 Timer 1 yang digunakan.

TCLK = Transmit clok enable. Jika diset menyebabkan serial port menggunakan pulsa overflow Timer 2 sebagai detak pengiriman. Jika TCLK = 0 pulsa overflow timer 1 yang digunakan.

CP/RL2 = Pemilihan capture/Reload. Jika diset maka proses capture yang terjadi sedangkan jika bit ini diclear maka proses reload.

TR2 = Bit untuk mengatur start/stop untuk timer 2 jika TR2 = 1 Timer akan aktif.

2.1.8. Idle Mode

Saat *Idle Mode* mikrokontroler tidak melakukan apa-apa. Tetapi peralatan lain yang terhubung tetap aktif. Kondisi ini dapat dihentikan dengan sebuah *interrupt* atau dengan me-*reset* system.

2.1.9. Sistem Interupt

Mikrokontroler AT89S8252 mempunyai 6 buah sumber interrupt yang dapat membangkitkan permintaan interrupt, yaitu INTO, INT1, T0, T1, T2 dan port serial.

Saat terjadinya interupt, mikrokontroler secara otomatis akan menuju ke *sub rutin* pada alamat tersebut. Setelah interupt service selesai dikerjakan, mikrokontroler akan mengerjakan program semula. Dua sumber interrupt external adalah INTO dan INT1, dimana kedua interupsi eksternal akan aktif atau aktif transisi tergantung isi dari IT0 dan IT1 pada register TCON. Interupsi T0, T1, T2 aktif pada saat timer yang sesuai mengalami *roll over*, interupsi serial dibangkitkan dengan melakukan operasi OR pada R1 dan T1. Tiap-tiap sumber interupsi dapat *enable* atau *disable* secara otomatis.

Tingkat prioritas semua sumber interupsi dapat diprogram sendiri-sendiri dengan set atau *clear bit* pada SFRS IP (*interrupt Priority*).

Tabel 2.5 Alamat Sumber Interupsi[1]

(MSB)(LSB)

EA	–	ET2	ES	ET1	EX1	ET0	EX0

Enable Bit = 1 enables the interrupt.

Enable Bit = 0 disables the interrupt.

Symbol	Position	Function
EA	IE.7	Disables all interrupts. If EA = 0, no interrupt is acknowledged. If EA = 1, each interrupt source is individually enabled or disabled by setting or clearing its enable bit.
–	IE.6	Reserved.
ET2	IE.5	Timer 2 interrupt enable bit.
ES	IE.4	SPI and UART interrupt enable bit.
ET1	IE.3	Timer 1 interrupt enable bit.
EX1	IE.2	External interrupt 1 enable bit.
ET0	IE.1	Timer 0 interrupt enable bit.
EX0	IE.0	External interrupt 0 enable bit.

2.2. Mikrokontroller AT89C51

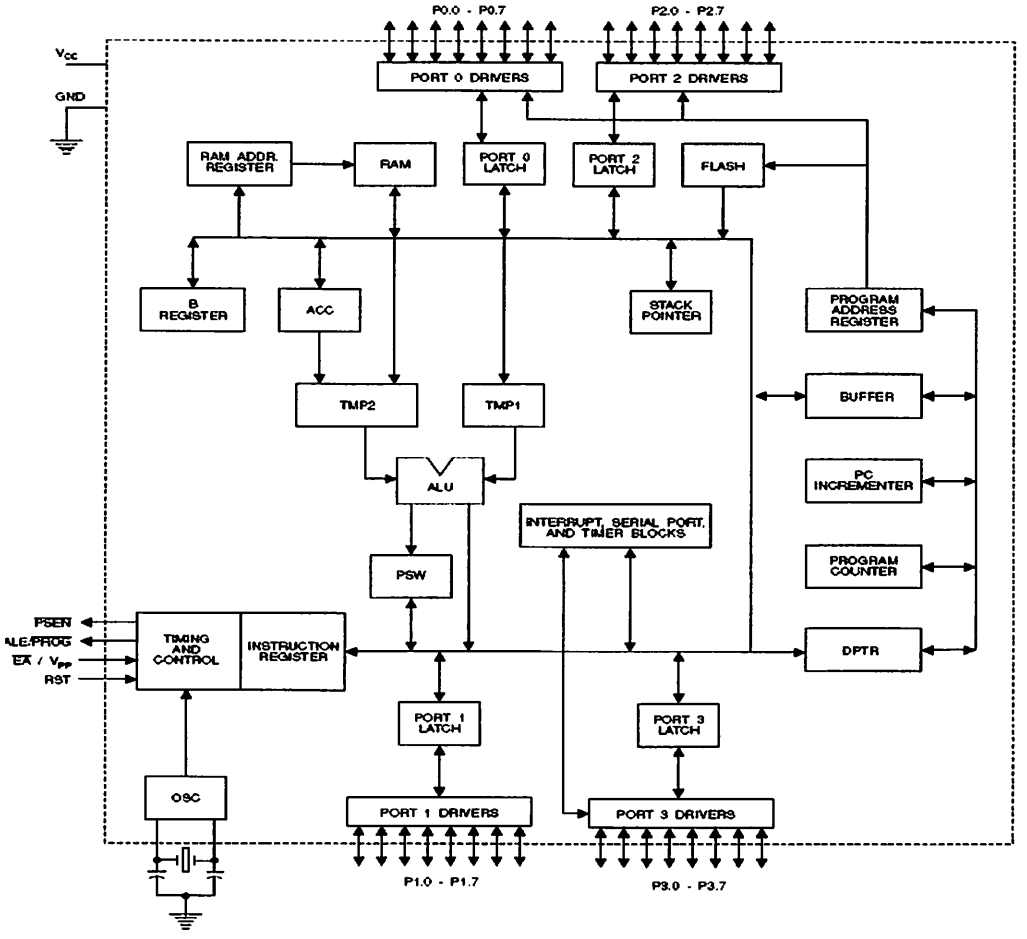
Mikrokontroller AT89C51 adalah mikrokontroller ATMEL *kompatibel* penuh dengan mikrokontroller keluarga MCS-51, dengan *supply* daya rendah, memiliki *performance* yang tinggi, dan merupakan mikrokontroller 8 bit yang dilengkapi 4 Kbyte EPROM (*Enable and programmable read Only Memory*) dan 128 Byte RAM *internal*. Program memori dapat diprogram ulang dalam sistem atau dengan menggunakan *Programmer Nomolately Memory Konvensional*.

Dalam sistem mikrokontroller terdapat dua hal yang mendasar, yaitu: perangkat keras dan perangkat lunak yang keduanya saling terkait dan mendukung.

2.2.1.Perangkat keras Mikrokontroller AT89C51

Mikrokontroller AT89C51 secara umum memiliki:

- CPU 8 bit
- *Memory*
- *Port I/O*
- *Timer* dan *Counter*
- Sumber *Interupt*
- *Program Serial* yang dapat diprogram
- Osilator dan *Clock*



Gambar 2.8 Blok diagram Mikrokontroller AT89C51[2]

2.2.2. Arsitektur AT89C51

Arsitektur mikrokontroller AT89C51 adalah sebagai berikut :

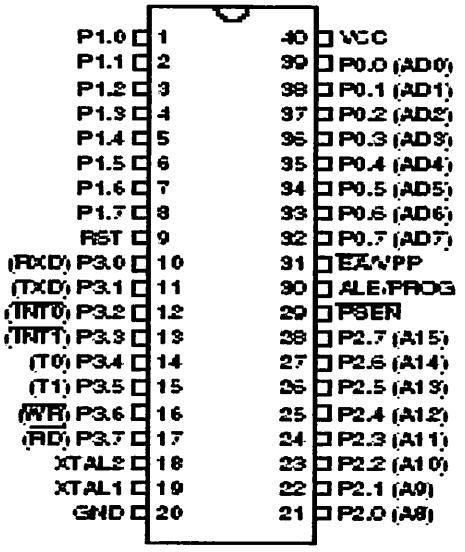
1. CPU (*Central Processing Unit*) 8-bit dengan *register* A (*accumulator*) dan B
2. 16-Bit *Program Counter* (PC) dan *Data Pointer* (DPTR).
3. 8- Bit *Program Status Word* (PSW).
4. 4-Bit *Stack Pointer* (SP).
5. 4 Kbyte *internal* EPROM.
6. 128 byte *internal* RAM.

- 4 *bank register*, masing-masing berisi 8 byte
- 16 byte alamat serbaguna yang dapat diakses sebagai byte atau bit, tergantung *software* yang digunakan.
- 80 byte *general purpose memory* data.

7. 32 pin *input-output* tersusun atas P0-P3, masing-masing 8-bit.
8. 2 buah 16-bit *Timer/Counter*.
9. 2 buah *port serial full duplex*
10. *Control Register*, antara lain : TCON, SCON, PCON, IP, dan IE
11. 5 buah sumber interupsi (2 buah sumber interup eksternal dan 3 buah sumber *internal*).
12. Osilator dan *Clock Internal*.
13. *Watch Dog Programmable Timer*.
14. ISP *Port* .

2.2.3. Konfigurasi Pin-pin Mikrokontroller AT89C51

Konfigurasi kaki-kaki Mikrokontroller AT89C51 terdiri dari 40 pena (pin), seperti pada gambar dibawah ini :



Gambar 2.9 Konfigurasi pin-pin AT89C51[2]

Fungsi dari tiap-tiap pena adalah sebagai berikut :

1. VCC, *Pin 40*

   Merupakan pin positif sumber tegangan 5 volt DC.

2. GND (ground), *Pin 20*

   Merupakan pin grounding sumber tegangan.

3. Port 0, *Pin 32 - 39*

   Merupakan port input dua arah dan dikonfigurasikan sebagai *multipleks* dua bus alamat rendah (A0-A7) dan data selama pengaksesan program memori dan data internal.

   Port 1, *Pin 1 – 8*

   Merupakan port input dua arah dengan pull-up dan juga menerima *Low-order address byte* selama memprogram dan verifikasi dari flash.. Pada mikrokontroller AT89C51 port 1 memikili 3 pin dengan fungsi khusus.

Tabel 2.6. Fungsi Khusus Port 1[2]

Port Pin	Alternative Functions
P1.5	MOSI (*used for In-system Programming*)
P1.6	MOSI (*used for In-system Programming*)
P1.7	SCK (*used for In-Programming*)

4. Port 2, *Pin 21 - 28*

   Merupakan port I/O dengan *internal pull-up*. Mengeluarkan *address* tinggi selama pengambilan (*fetching*) program memori external. Selama pengaksesan ke external data memori, port 2 mengeluarkan isi SFR (*Special Function Register*). Menerima a*ddress* dan beberapa sinyal control selama pemrograman.

5. Port 3, *Pin 10 - 17*

   Merupakan port I/O dengan *internal pull-up*. Port 3 juga memiliki fungsi khusus, yaitu:

Tabel 2.7. Fungsi Khusus Port 3[2]

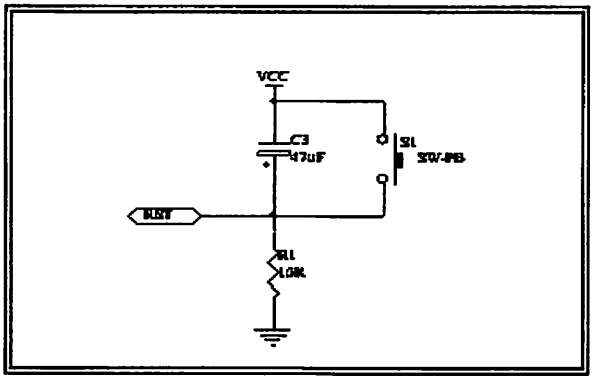
Port Pin	Alternative Funtions
P3.0	RXD (*serial input port*)
P3.1	TXD (*serial output port*)
P3.2	$\overline{INT0}$ (*external interrupt 0*)
P3.3	$\overline{INT1}$ (*external interrupt 1*)

P3.4	T0 (*timer 0 external input*)
P3.5	T1 (*timer 1 external input*)
P3.6	$\overline{WR}$ (*internal data memory write strobe*)
P3.7	$\overline{RD}$ (*external memory read strobe*)

6. Reset, *Pin 9*

   Perubahan taraf tegangan dari rendah ketinggi akan mereset AT 89C51.

   T = R.C Ln 2



Gambar 2.10 Rangkaian Reset[2]

7. ALE/PROG, *Pin 30*

   Pulsa output ALE digunakan untuk proses-proses '*latching*' *byte address* rendah (A0-A7) selama pengaksesan ke external memori. Pin ini juga digunakan untuk memasukkan pulsa program (prog) selama pemrograman.

8. PSEN, *Pin 29*

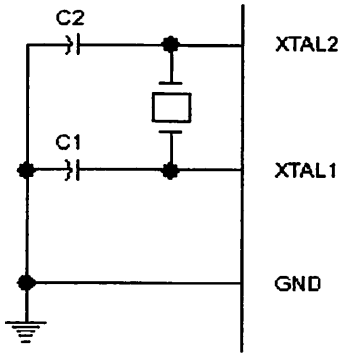
   Merupakan strobe baca ke program memori ekternal.

9. EA/VPP, *Pin 31*

   External Address Enable (EA) digroundkan jika mengakses memori ekternal, akan dihubungkan ke VCC jika digunakan untuk mengakses memori internal.

10. X-TALL 1 dan X-TALL 2, *Pin 19 dan Pin 18*

Kaki ini dihubungkan dengan kristal bila menggunakan osilator internal. XTALL 1 merupakan input inverting osilator amplifier sedangkan X-TALL 2 merupakan output inverting osilator amplifier.



Gambar 2.11 Rangkaian Clock[2]

2.2.4. Organisasi Memori

Organisasi memori pada mikrokontroller AT89C51 dapat dibagi menjadi dua bagian besar yaitu memori program dan memori data. Pembagian tersebut didasarkan atas fungsi dari penyimpangan data maupun program. Memori program digunakan untuk menyimpan instruksi-instruksi yang akan diajarkan oleh mikrokontroller, sedangkan memori data digunakan sebagai tempat menyimpan instruksi-instruksi yang sedang diolah mikrokontroller.

Program mikrokontroller disimpan dalam memori program berupa ROM. Mikrokontrller AT89C51 dilengkapi dengan ROM internal, sehingga untuk menyimpan program tidak digunakan ROM ekstrernal yang terpisah dari mikrokontroller. Agar tidak menggunakan memori program eksternal, EA (*Eksternal Address enable*) dihubungkan dengan Vcc.

Memori program mikrokontroller menggunakan alamat 16 bit mulai 0000_H-$0FFF_H$, sehingga kapasitas penyimpanan program maksimal adalah 4Kbyte. Sinyal / PSEN (*Program Strobe Enable*) tidak digunakan jika menggunakan memori internal.

Selain program mikrokontroller AT 89C51 juga memiliki data internal 128 *byte* dan mampu mengakses memori data eksternal sebesar 64Kb. Semua memori data internal dapat dialamati dengan data langsung atau tidak langsung. Ciri dari pengalamatan langsung adalah *operand* adalah alamat *register* yang berisi alamat data yang akan diolah. Sebagian memori tersebut dapat dialamati dengan memori satu bit. Untuk membaca data digunakan sinyal / RD sedangkan untuk menulis data digunakan sinyal / WR.

2.2.5. SFR (*Special Function Register*)

Register Fungsi Khusus (*Special Function Register*) terletak pada 128 byte bagian atas memori data internal dan berisi *register-register* untuk pelayanan *latch port, timer, program status words, control peripheral* dan sebagainya. Alamat register fungsi khusus ditunjukkan pada tabel 2.8 dibawah ini:

Tabel 2.8. *Special Function Register*[2]

Simbol	Nama Register	Alamat
ACC	*Accumulator*	$E0_H$
B	*Register* B	$F0_H$
PSW	*Program Status Word*	$D0_H$
SP	*Stack Pointer*	81_H
DPTR	*Data Pointer* 2 Byte	

DPL	Bit Rendah	82_H
DPH	Bit Tinggi	83_H
P0	*Port* 0	80_H
P1	*Port* 1	90_H
P2	*Port* 2	$A0_H$
P3	*Port* 3	$B0_H$
IP	*Interupt Priority Control*	$D8_H$
IE	*Interupt Enable Control*	$A8_H$
TMOD	*Timer/Counter Mode Control*	89_H
TCON	*Timer/Counter Control*	88_H
TH0	*Timer/Counter 0 High byte*	$8C_H$
TL0	*Timer/Counter 0 Low byte*	$8A_H$
TH1	*Timer/Counter 1 High byte*	$8D_H$
TL1	*Timer/Counter 1 Low*	$8B_H$
SCON	*Serial Control*	98_H
SBUF	*Serial Data Buffer*	99_H
PCON	*Power Control*	87_H

Beberapa macam *register* fungsi khusus yang sering digunakan adalah sebagai berikut :

- *Accumulator* (ACC) merupakan *register* untuk penambahan dan pengurangan. Perintah *mnemonic* untuk mengakses akumulator disederhanakan sebagai A.
- *Register* B merupakan *register* khusus yang berfungsi melayani operasi perkalian dan pembagian.
- *Register R* merupakan delapan set *register* yang dinamakan R0, R1, R2, R3, R4, R5, R6 dan R7, fungsi dari *register-register* ini adalah sebagai *register* yang membantu penyimpanan data yang menggunakan banyak operasi.

Register-register ini yang membantu akumulator dalam melakukan operasi antara dua operan.

- *Stack Pointer* (SP) merupakan *register* 8 bit yang dapat diletakkan dialamat manapun pada RAM *internal.*
- *Data Pointer* (DPTR) terdiri dari dua *register*, yaitu *register* untuk byte tinggi *(Data Pointer High*, DPH) dan register untuk byte rendah (*Data Pointer Low*, DPL) yang berfungsi untuk mengunci alamat 16 bit. DPTR berfungsi untuk menunjuk suatu lokasi data, namun pada beberapa perintah DPTR digunakan untuk mengakses memori eksternal.
- *PC (Program Counter)* merupakan alamat 16 bit yang menginstruksikan AT89C51 alamat instruksi yang selanjutnya akan dilaksanakan. Saat inisialisasi AT89C51, PC terisi dengan 00000h dan akan bertambah satu setiap kali instruksi telah dilaksanakan. Harga PC tidak dapat langsung dirubah dengan menggunakan perintah MOV PC,2340h, namun dengan perintah LJMP 2340 yang akan mengisi PC dengan 2340h..
- *Program Status Word* (PSW) berisi bit-bit status yamg berkaitan dengan kondisi CPU saat itu. PSW terletak pada alamat D0H.

PSW
D0H

PSW.7	PSW.6	PSW.5	PSW.4	PSW.3	PSW.2	PSW.1	PSW.0
CY	AC	F0	RS1	RS0	OV	-	P

1. CY (*Flag Carry*)

   Flag carry, yang terletak pada alamat D7H, berfungsi sebagai pendeteksi terjadinya kelebihan pada operasi penjumlahan, atau terjadinya peminjaman *(borrow)* pada operasi pengurangan. Misalnya, jika data pada

akumulator adalah FFH dan dijumlahkan dengan bilangan satu atau lebih, maka akan terjadi kelebihan sehingga akan membuat *carry* menjadi *set*. Demikian juga apabila data pada akumulator adalah 00H dan dikurangkan dengan bilangan satu atau lebih, akan terjadi peminjaman sehingga membuat *carry* juga menjadi *set*.

2. AC (*Flag Auxiliary Carry*)

   Flag auxiliary carry akan selalu dalam kondisi *set* apabila pada saat proses penjumlahan terjadi *carry* dari bit ketiga hingga bit keempat.

3. *Flag* 0

   Flag 0 dapat digunakan untuk tujuan umum tergantung pada kebutuhan pemakai.

4. RS *(Register Select)*

   Bit Pemilih *Bank Register (Register Bank Select Bits)* RS0 dan RS1 digunakan untuk menentukan lokasi dari *bank register* (R0-R7) pada memori. RS0 dan RS1 selalu bernilai 0 setiap kali sistem di reset sehingga lokasi dari *register* R0 hingga R7 akan berada pada alamat 00H hingga 07H.

5. OV (*Flag Overflow*)

   Flag overflow akan berada pada kondisi set jika pada operasi aritmatik menghasilkan bilangan yang lebih besar daripada 128 atau lebih kecil dari -128.

6. P (bit paritas)

   Bit paritas akan berada pada kondisi set jika jumlah bit 1 dalam akumulator adalah ganjil dan akan berada pada kondisi *clear* jika jumlah

bit 1 dalam akumulator adalah genap. Misalnya, data yang tersimpan pada akumulator adalah 10101110b atau AEH maka *parity bit* akan berada pada kondisi *set*. Data AEH mempunyai lima bit yang berkondisi 1 atau dapat disebut mempunyai bit 1 dalam jumlah yang ganjil.

- *Port* 0 sampai *Port* 3 merupakan *register* yang berfungsi untuk membaca dan mengeluarkan data pada port 0,1,2 dan 3. Masing-masing *register* ini dapat dialamati per byte maupun per bit.
- *Control Register* terdiri dari register yang mempunyai fungsi kontrol. Untuk mengontrol sistem interupsi, terdapat dua *register* khusus yaitu *register* IP (*Interupt Priority*) dan *register* IE (*Interupt Enable*). Untuk mengontrol *timer/counter* terdapat dua *register* khusus yaitu register TCON (*Timewr Counter Control*) serta *port serial* menggunakan *register* SCON (*Serial Port Control*).

2.3 ISD (Information Storage Device) 2500

Peralatan penyimpanan informasi suara, ISD seri 2500 mempunyai kualitas bagus, dengan durasi penyimpanan dari 60 sampai 120 detik. Peralatan CMOS yang ada didalamnya adalah *chip oscilator, mocrophone preamplifier, automatic gain control, antilisiang filter, smouthing filter, speaker amplifier*. Pada pengembangannya, ISD 2500 adalah kompatibel dengan mikrokontroler, mengijinkan penyimpanan dan pengalamatan yang komplek. Perekaman disimpan dalam suatu chip yang tidak mudah berubah dalam cell memori.

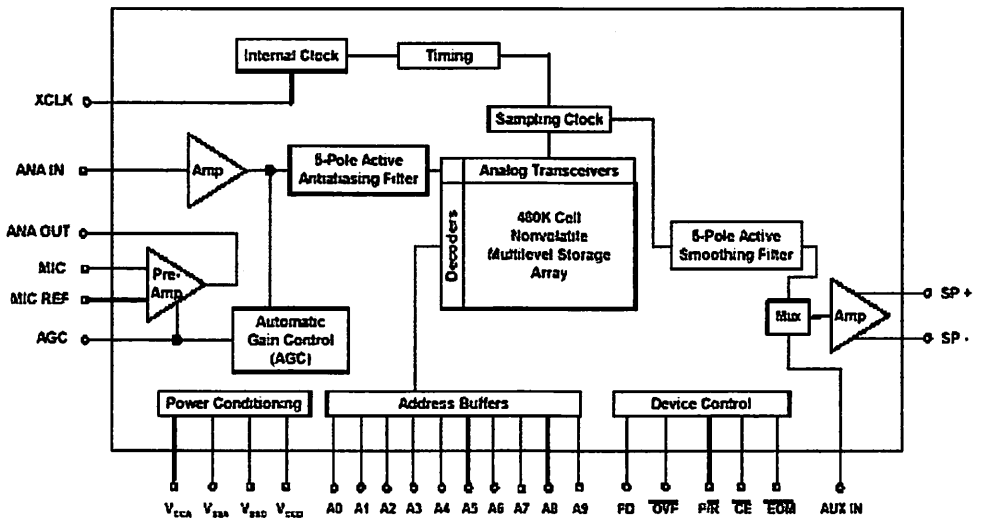
Sinyal suara dan audio disimpan secara langsung ke memori pada tempat naturalnya dengan kualitas suara yang bagus. Untuk karakteristiknya adalah sebagai berikut:

- *Chip* tunggal yang mudah digunakan untuk merekam atau memainkan suara.
- Suara yang direproduksi menpunyai kualitas yang bagus dan alami.
- Bisa dioperasikan secara manual dengan *switch* atau dengan mircokontroler.
- Memiliki durasi penyinpanan dari 60,75,90,120 detik.
- Arus pada saat *standby* = 1 μA.
- Tidak perlu power untuk tetap menyimpan data dalam IC, sehingga tidak perlu baterai cadangan.
- Data dapat tahan hingga 100 tahun.
- 100.000 kali rekam.
- *Power supply* +5 Volt.

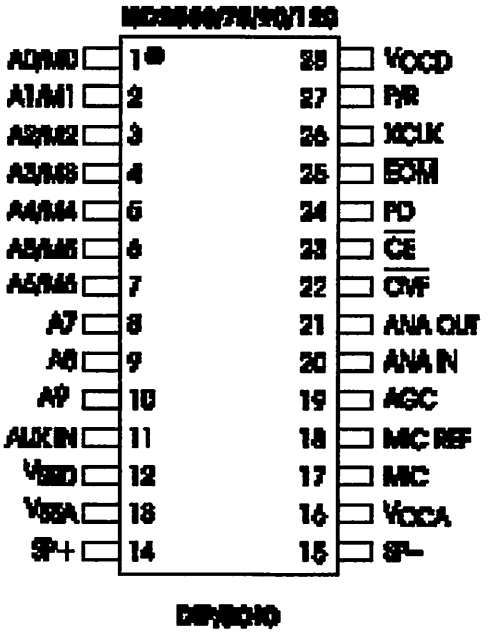
Tabel 2.9 Seri ISD 2500[3]

Part Number	Duration (Seconds)	Input Sample Rate (kHz)	Typical Filter Pass Band * (kHz)
ISD2560	60	8.0	3.4
ISD2575	75	6.4	2.7
ISD2590	90	5.3	2.3
ISD25120	120	4.0	1.7

Dengan melihat tabel diatas, maka dapat diketahui bahwa IC penyimpan suara ISD seri 2500 ini adalah merupakan jenis EEPROM (Electrically Erasable Programable ROM). EEPROM adalah jenis ROM yang dapat diprogram, dihapus dan diprogram ulang secara elektrik. IC ISD 2500 ini dapat melakukan perekaman suara atau pesan dengan jangka waktu durasi maksimum 120 detik. dengan sample rate 4.0 Khz. Dimana untuk cell penyimpanan ini terbagi dalam alamat yaitu dari 00H sampai 257H.



Gambar 2.12 Diagram Blok ISD 2500[3]



Gambar 2.13 Susunan Kaki ISD 2500[3]

Keterangan pin ISD 2500 :

1. Power Down Input (PD)

   Apabila suara tidak di rekam atau diputar ulang PD dapat diaktifkan supaya ISD 2500 mendapat konsumsi daya yang rendah. Jika EOM rendah selama terjadi kondisi overflow, PD harus berlogika '1' untuk mereset address supaya kembali ke awal perekaman / playback.

2. Chip Enable Input (CE)

   Untuk mengakses ISD 2500 maka pin CE harus berlogika '0'. Apabila pin CE berlogika '1' maka ISD tidak dapat diakses dan auxiliry input terhubung langsung ke amplifier speker.

3. Playback Input (P/R)

   Pada mode rekam pin P/R harus berlogika '0' dan pada mode playback maka pin P/R harus berlogika '1'.

4. End of Message Output (EOM)

   Penandaan ini secara otomatis disisipkan pada akhir penyimpanan pesan. EOM output akan rendah selama periode TEOM pada akhir pesan telah melampaui 120 detik (device full).

5. Address Mode Input (A0-A9)

   Address mode Input menyediakan dua fungsi yaitu sebagai address pesan (A6 atau A7 rendah) dan sebagai operasional mode (A6-A7 tinggi). Message address dapat mengalamati maksimum 160 segment. Setiap segment mempunyai durasi 0,125 detik. Arah pembacaan dan perekaman dimulai dari awal setting address (A0-A9).

6. Overflow Output (OVF)

   Pin ini akan Low apabila batas akhir memori terlewati.

7. Microphone Output (Mic)

   Input microphone akan mentransfer sinyal yang akan masuk ke amplifier yang berada di dalam IC rangkaian *AGC* mengontrol penguatan antara -15 sampai 24 dB. Microphone eksternal harus dihubungkan dengan kondensator kopling ke pin ini. Nilai kapasitor kopling bersama dengan impendasi internal (normal 10 KΩ) akan menentukan frekuensi *cut-off* rendah dari *filter* internal.

8. Microphone Reference Input (Mic Ref)

   Microphone Reference input merupakan inverting input yang berhubungan dengan amplifier.

9. Automatic Gain Control (AGC)

   AGC menyesuaikan penguatan dari *pre-amplifier* sesuai dengan input microphone.

10. Analog Input (ANA IN)

    Analog input akan mentransfer sinyal ke chip untuk perekaman. Jika digunakan microphone maka ANA OUT harus dihubungkan ke pin ANA IN melalui kondensator kopling. Nilai kapasitor ini dengan impendasi input ANA IN (normal 3 KΩ) akan menentukan frekuensi *cut-off filter*.

11. Analog Output (ANA OUT)

    Pin ini merupakan output dari pre-amplifier yang akan digunakan oleh pemakai.

12. Auxiliary Input (AUX IN)

    Auxiliary Input dimultipleks melewati output amplifier dan dikeluarkan ke speker jika CE dalam keadaan high. P/R high dan playback tidak aktif.

13. Address input (A0-A9)

    Digunakan mengalamati segment-segment pada chip. Dengan demikian kita dapat menentukan alamat untuk tiap-tiap pesan.

14. Voltage Input (V_{CCA},V_{CCD})

    Merupakan kaki untuk memasukkan tegangan +5 Volt pada IC.

15. Ground Input (V_{SSA},V_{SSD})

    Input untuk kaki *ground* pada IC.

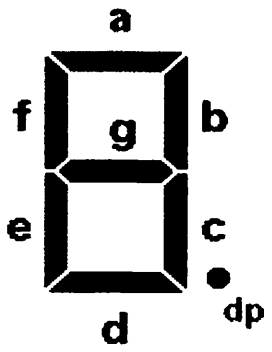
2.3.1 Cara perekaman / pengisian suara

Langkah langkah yang dilakukan untuk memulai perekaman yang mengeset alamat / durasi waktu yang dibutuhkan untuk perekaman. Pada saat memulai perekaman sinyal P/R LOW maka dengan demikian secara otomatis pin ANA – IN bekerja. Pada saat inilah dimasukan suara yang akan direkam melalui microphone. Jika ruang sudah terisi penuh maka sinyal P/D harus dikembalikan keposisi HIGH. Tanda ahkir dari pesan (end – off – message merker) akan otomatis terekam sesudah itu. Tanda ini berguna untuk memutuskan playback secara otomatis bila rekaman sudah habis. ISD 2500 akan langsung ke stanby bila P/D dalam keadaan high.

2.4 Display Seven Segmen

Penampil-penampil biner dari sandi BCD menjadi bilangan desimal selain dalam tabung angka (nixe tube) yang sudah berbentuk angka –angka desimal dari 0 sampai 9 dapat di tampilkan dengan mengatur penyelaan dari 7 ruas tersebut. Perlu di ketahui bahwa LED (light emmiting diode) adalah suatu diode yang bersifat menyala bila mendapat suatu arus maju (forward bias).

Dengan sifatnya yang demikian, led banyak di pakai pada lampu-lampu penunjuk kecil yang serba guna. Misalnya untuk menunjuk keadaan ON dari suatu peratan atau lampu-lampu tes, penggunaannya sebagai seven segmen display adalah susunanya sesuai gambar:



Gambar 2.14 Display seven segmen[4]

pada gambar diatas segmennya adalah a,b,c,d,e,f,g (tujuh buah). Bila semua segmen menyala, maka dapat di baca sebagai angka desimal.

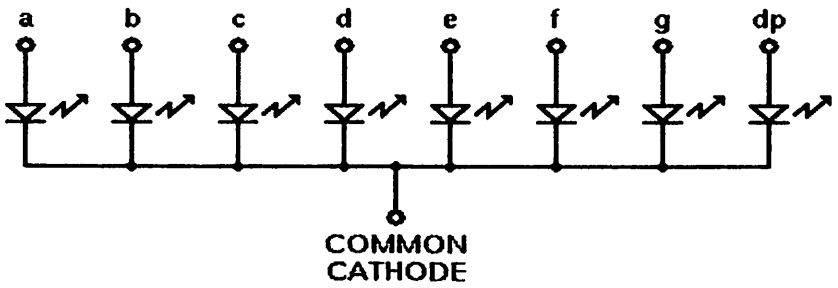
Tabel 2.10

Tabel kebenaran BCD to seven segmen

Desimal	BCD	Seven segmen
	8421	A b c d e f g
0	0000	1 1 1 1 1 1 0
1	0001	0 1 1 0 0 0 0
2	0010	1 1 0 1 1 0 1
3	0011	1 1 1 1 0 0 1
4	0100	0 1 1 0 0 1 1
5	0101	1 0 1 1 0 1 1
6	0110	1 0 1 1 1 1 1
7	0111	1 1 1 0 0 0 0
8	1000	1 1 1 1 1 1 1
9	1001	1 1 1 1 0 1 1

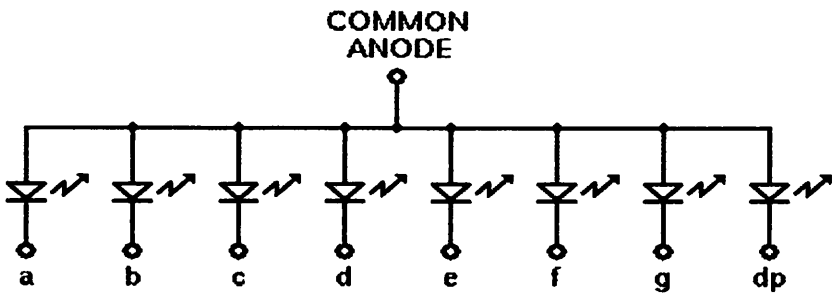
`Ada 2 jenis Seven Segmen:

1. Seven segmen common cathode:



Gambar 2.15 Common Cathoda[4]

2. Seven Segmen Common Anode

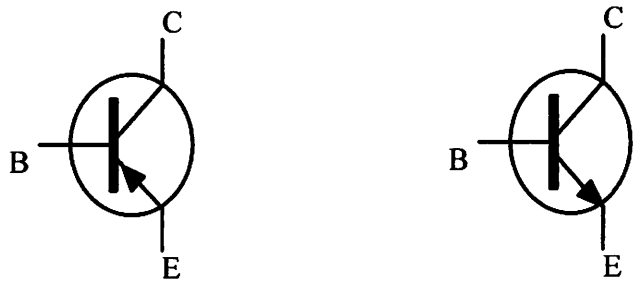


Gambar 2.16 Common Anode[4]

2.5 Transistor

Transistor adalah suatu komponen aktif yang dibuat dari bahan semikonduktor. Apabila kita mendoping semikonduktor untuk mendapatkan kristal NPN atau PNP, maka kristal seperti ini disebut Transistor *Junctio*n. Daerah

tipe N mempunyai banyak sekali elektron pita konduksi dan daerah tipe P mempunyai banyak *hole*. Jadi transistor *junction* mempunyai dua macam pembawa muatan yaitu elektron bebas pada daerah N dan *hole* pada daerah P. Oleh karena itu transistor junction disebut juga transistor dua kutub (*bipolar*). Transistor bipolar ada dua macam yaitu transistor jenis NPN dan PNP. Adapun simbol dari kedua transistor seperti pada gambar 2.13 berikut ini :

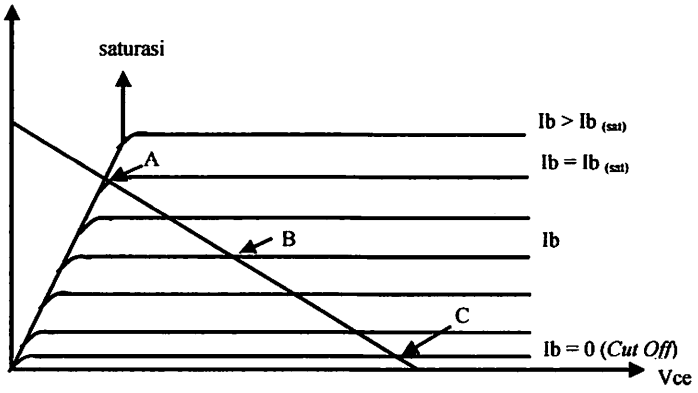


Transistor PNP ***Transistor NPN***

Gambar 2.17 Simbol Transistor Bipolar [12]

Daerah kerja dari transistor terbagi menjadi tiga yaitu : daerah kerja *cut off*, daerah kerja saturasi dan daerah kerja aktif.

Untuk lebih jelasnya mengenai daerah kerja Transistor dapat dilihat pada gambar 2.18 dibawah ini :



Gambar 2.18 Garis Beban Transistor [12]

A = Penjenuhan (saturasi)

B = Titik Kerja

C = Titik Sumbat (*Cut Off*)

Untuk garis beban diperoleh dengan persamaan :

$$V_{CC} = I_C \cdot R_C + V_{CE}$$

Saat *cut off* $I_B = 0$, sehingga :

$$I_C = \beta_{dc} \cdot I_B$$

$$I_B = \frac{Vcc - Vbe}{Rb}$$

$V_{CE\,(\text{cut off})} = V_{CC}$ (pada titik A)

Saat saturasi, maka $I_B = I_{B\,(\text{sat})}$, sehingga :

$$I_{C\,(\text{sat})} = \frac{Vcc}{Rc} \text{ (titik B)}$$

Jika arus basis lebih besar atau sama dengan I_B saturasi, titik kerja Q berada dalam ujung atas dari garis beban, maka transistor seperti sebuah saklar tertutup. Sebaliknya, jika arus basis nol, transistor bekerja dalam ujung bawah dari garis beban, dan transistor seperti sebagai saklar terbuka .

2.5.1. Daerah Kerja Transistor

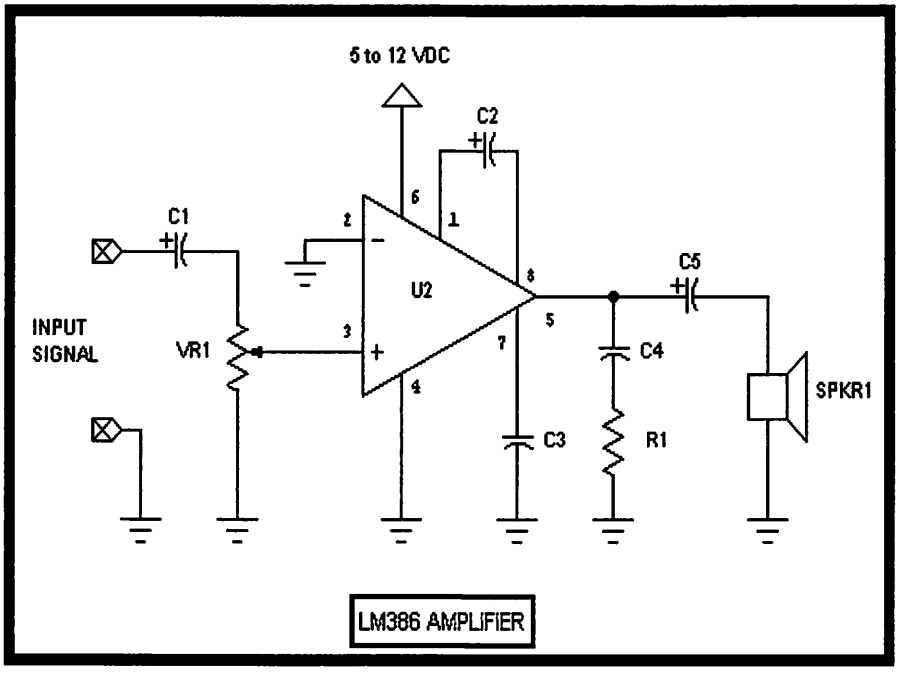
Berdasarkan pada teori di atas maka dapat dilihat bahwa transistor mempunyai 3 daerah yaitu : Basis, Kolektor dan Emitor. Pada transistor NPN mempunyai dua junction , yaitu *junction* antara Emitor dan Basis serta *junction* antara Basis dan Kolektor. Oleh karena itu, transistor bersifat seperti dua buah

dioda. Sedangkan pada transistor PNP adalah kebalikan dari transistor NPN khususnya untuk karakteristik arus dan tegangannya.

2.6 LM 386 (Low Voltage Audio Power Amplifier)

LM 386 pada dasarnya adalah sebuah penguat operasional yang di khususkan penggunaanya untuk arus yang lemah (low voltage audio amplifier), dengan karakteristik khusus diantaranya:

- Interval gain di tetapkan atau di set pada 20.
- Dapat di tingkatkan gainnya sampai 200 dengan menambah tahanan antara pin1 dan pin8.
- Sangat cocok di pakai untuk catu daya bateray karena konsomsi energi yang sangat rendah (sekitar 24 miliwatt ketika di noperasikan dengan catu daya sebear 6V)
- Dapat di pakai dengan range voltase yang lebar (antara 4V-12V atau 5V-18V).
- Rendah distorsi (Low Distorsi) : 0,2% (AV=20, VS=6V, RL=8W, PO=125 mW, f=1Khz).



Gambar 2.19 Rangkaiaan IC LM 386[5]

2.7 Push Button

Push Button merupakan sebuah saklar yang bekerja karena ada suatu sentuhan atau gesekan. Push Button ini di tempatkan sesuai kebutuhan dan keadaan agar dapat menyentuh suatu benda pada tangkai Push Button tersebut.

Push Button mempunyai beberapa bagian antara pengungkit dan roda penjulang yang merupakan bagian mekanik yang jika tersentuh oleh suatu benda atau mekanisasi lain, maka Push Button akan ON dan lalu menggerakkan lengan pengungkit dalam suatu kontak.

Ada beberapa tipe Push Button yaitu Push Button yang merupakan kontak NC (Normally Closed) dan NO (Normally Open). Push Button yang merupakan

kontak NO berfungsi sebagai penghubung sedangkan yang kontak NC berfungsi sebagai pemutus.

Adapun simbol dari push botton dari yang kontak NC dan kontak NO adalah sbb:

Push button make NO
(Normally Open)

Push button break NC
(Normally Closed)

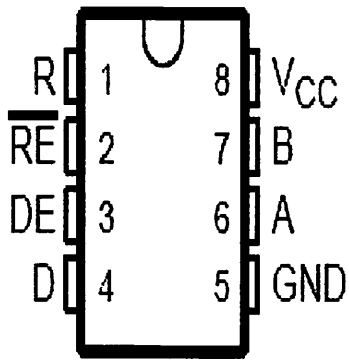
Gambar 2.20 Simbol Push Button

2.8 IC SN75176

IC SN75176 adalah sebuah IC yang dikeluarkan oleh Texas Instruments yang berfungsi sebagai rangkaian penguat dan biasa digunakan untuk menyediakan signal serial yang kuat sehingga sanggup untuk mengirimkan sinyal walaupun dengan jarak kabel yang panjang (sampai dengan 1,2 km). Mampu melalui kabel yang panjang (1,2 km) pada *baudrate* yang tinggi dalam lingkungan listrik yang berpotensi menimbulkan *noise* atau interferensi elektromagnetik yang tinggi.

SN75176 adalah IC monolitik yang di desain untuk data komonikasi 2 arah pada jalur transmisi multipoin bus. SN75176 mengkombinasikan 3 driver deferensial dan jalur penerima input berbeda, yang keduanya beroperasi dari penyedia energi tunggal 5V. Driver dan penerima memiliki enable yang tinggi aktif dan rendah aktif, berturut-turut yang dapat di hubungkan bersama-sama ke dalam fungsi sebagai pengontrol arah.

Driver didesain untuk mengatasi muatan sampai 60mA penampang atau sumber aliran. Driver aliran positif dan negatif membatasi dan menurunkan temperatur untuk perlindungan dari kondisi jalur yang salah. Penurunan temperatur di desain untuk persimpangan suhu sekitar 150°C. Fitur penerima input minimum dengan hambatan 12Ω, kepekaan input 200mV.



Gambar 2.21 IC SN 75176[6]

Tabel 2.11

Tabel fungsi logika IC SN 75176[6]

DS75176B Transmitting

Inputs			Line Condition	Outputs	
$\overline{RE}$	DE	DI		$\overline{DO}$	DO
X	1	1	No Fault	0	1
X	1	0	No Fault	1	0
X	0	X	X	Z	Z
X	1	X	Fault	Z	Z

DS75176B Receiving

Inputs			Outputs
$\overline{RE}$	DE	RI-$\overline{RI}$	RO
0	0	≥ +0.2V	1
0	0	≤ −0.2V	0
0	0	Inputs Open**	1
1	0	X	Z

IC sebagai transmisi:

RE diabaikan, DE sebagai kontrol untuk pengaktifan transmisi. Bila DE berlogika 1,RE berlogika 1 maka output DO berlogika 1.

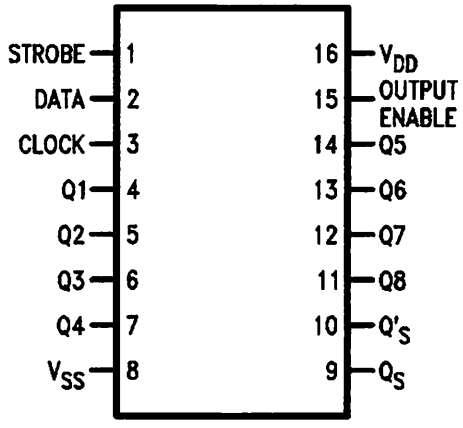
IC sebagai penerima:

RE berlogika 0, DE juga berlogika 0,sedang RI ≥ +0,2V maka RO berlogika 1, untuk RE berlogika 0, DE juga berlogika 0, sedang RI ≤ -0,2V maka RO berlogika 0.

2.9 IC CD4094BC

CD4094BC terdari atas 8 bit shif register dan 3 state 8-bit latch. Data dibagi secara serial melalui shift register pada transmisi positif dari sebuah Clock. Output pada tahap akhir (Qs) dapat digunakan untuk mengalirkan beberapa data. Data pada output Qs disalurkan untuk output kedua, Q's. Pada ujung negatif clock berikutnya.

Output pada setiap tahap shift register, yaitu data latch negatif pada *strobe* input. Ketika strobe tinggi, data memperbanyak melalui latch ke 3-state. Keadaan enable ketika output enable tetap pada posisi high.



Gambar 2.22 IC CD4094BC[7]

Tabel 2.12

Tabel fungsi logika IC CD4094BC[7]

Clock	Output Enable	Strobe	Data	Parallel Outputs		Serial Outputs	
				Q1	Q_N	Q_S (Note 1)	Q'_Σ
↗	0	X	X	Hi-Z	Hi-Z	Q7	No Change
↘	0	X	X	Hi-Z	Hi-Z	No Change	Q7
↗	1	0	X	No Change	No Change	Q7	No Change
↗	1	1	0	0	Q_N–1	Q7	No Change
↗	1	1	1	1	Q_N–1	Q7	No Change
↘	1	1	1	No Change	No Change	No Change	Q7

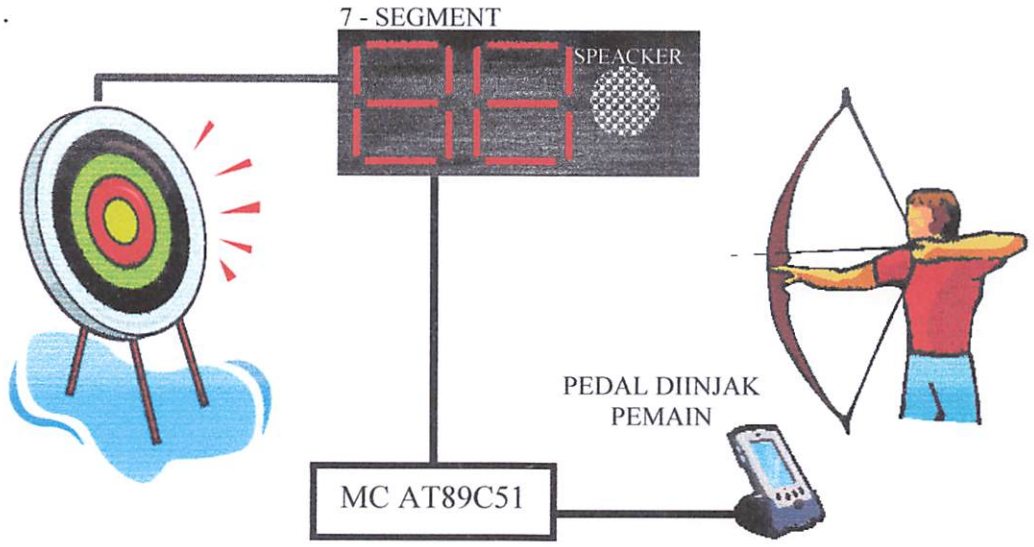
X = Don't Care
↘ = HIGH-to-LOW
↗ = LOW-to-HIGH

BAB III

PERENCANAAN SISTEM

3.1 Pendahuluan

Dalam bab ini akan dijelaskan tentang perencanaan dan pembuatan papan skor pada panahan. Alat ini akan menampilkan skor pada seven segmen dan output suara melalui ISD apabila anak panah yang di tembakkan menyentuh push button dan bernilai sama dengan nol apabila tidak menyentuh push button.



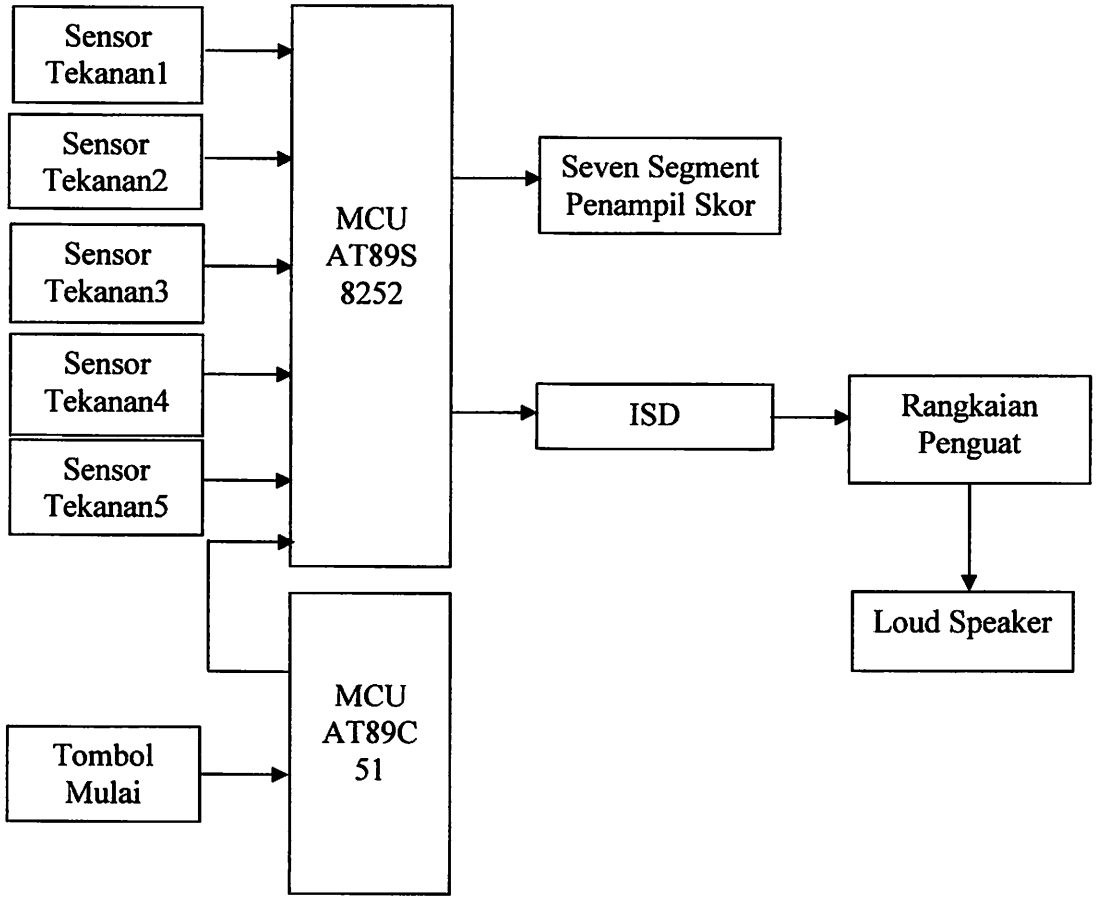
Gambar 3.1 Bentuk Fisik Perencanaan Alat

Pada gambar kanan atas dapat dilihat bahwa apabila pemanah menembakkan anak panah secara tepat pada sasaran maka papan skor atau display seven segmen akan menampilkan hasil penilaian sesuai dengan tembakan yang di peroleh pemanah tersebut. Sedangkan gambar kiri atas (papan skor) menjelaskan tentang penilaiannya.

Perencanaan dan Pembuatan alat ini, tahapan- tahapan yang di lakukan adalah sebagai berikut :

- Perencanaan dan pembuatan alat
- Perencanaan rangkaian kontrol dalam blok diagram sistem secara garis besar.
- Perencanaan perangkat keras (hard-ware) yang berupa rangkaian elektronik.
- Perencanaan perangkat lunak (soft-were) yang meliputi pembuatan flowchar dan pemrograman.

Gambaran secara singkat mengenai alat yang dibuat adalah :



Gambar 3.2 Diagram Blok Perencanaan Alat

Fungsi dari masing – masing blok adalah :

1 Sensor tekanan

Digunakan sebagai inputan data dari papan skor ke mikrokontroler .

2 Mikrokontroler AT89S8252

Digunakan untuk mengolah data yang diterima dari input, mengontrol dan mengendalikan rangkaian-rangkaian yang dihubungkan dengan mikrokontroler tersebut.

3 Tombol mulai

Digunakan untuk memulai bahwa mikro siap menerima data.

4 Mikrokontroler AT89C51

Digunakan untuk mengolah data serial yang akan di tranfer ke mikrokontroler AT 89S8252.

5 Seven Segment Penampil Skor

Untuk menampilkan data yang diterima sebagai skor yang di peroleh dari pemanah.

6 ISD (Information Storage Device)

Digunakan untuk merekam suara dan menampilkan ulang suara tersebut melalui speaker.

7 Rangkaian penguat

Sebagai penguat dari ISD yang akan mengeluarkan suara melalui loud speker.

8 Speaker

Digunakan untuk menampilkan suara yang telah direkam pada ISD.

3.1.1 Prinsip Kerja Sistem :

Pertama-tama pemanah sebelum melakukan tembakan, di haruskan menginjak pedal (mulai) push button sebagai tanda sudah siapnya alat bekerja. Anak panah menancap di papan panah yang terdiri dari nilai-nilai yang telah ditentukan, kemudian papan yang sudah di lengkapi dengan push button, menyentuh sensor tekan Push button dan mengeluarkan data input ke mikrokontroler. Kemudian mikrokontroler akan mendeteksi dan mengolah data dari sensor tekan kemudian akan menampilkannya ke seven segmen penampil skor ,bersamaan dengan seven segmen, ISD yang telah merekam nilai-nilai yang telah ditentukan akan mengeluarkan suara berapa skor yang di peroleh oleh pemanah. Sehingga pemanah dapat mengetahui berapa nilai yang di perolehnya.

3.2 Mikrokontroller AT89S8252

Mikrokontroller AT89S8252 adalah sebuah chip IC yang terdiri dari 40 pin. Dalam perencanaan sistem ini pin – pin yang digunakan adalah sebagai berikut:

Adapun fungsi dari masing – masing pin tersebut adalah:

1 Pin 1 (P1.0) merupakan port output mikro yang digunakan sebagai address mode input A0 yang berasal dari ISD.

2 Pin 2 (P1.1) merupakan port 1 dari mikrokontroller untuk output ke ISD, digunakan sebagai mode rekam pin P/R harus berlogika '0' dan pada mode playback maka pin P/R harus berlogika '1'.

3 Pin 3 (P1.2) merupakan output mikro untuk mengaktifkan PD pada ISD.

4 Pin 4 (P1.3) merupakan port output mikro ke ISD yang digunakan sebagai penandaan pada akhir penyimpanan pesan (EOM).

5 Pin 5 (P1.4) merupakan port output mikro ke ISD yang di gunakan Untuk mengakses ISD 2500 maka pin CE harus berlogika '0'.

6 Pin 6 (P1.5) merupakan port output mikro ke ISD yang di gunakan sebagai Overflow Output.

7 Pin 7 (P1.6) merupakan port yang digunakan sebagai port keluaran dari mikrokontroler ke data serial.

8 Pin 8 (P1.7) merupakan port yang digunakan sebagai port pengirim data ke serial.

9 Pin 10 (P3.0) merupakan input mikro dari data serial.

10 Pin 11 (P3.1) merupakan output mikro untuk pengiriman data ke serial.

11 Pin 15 (P3.5) merupakan output mikro untuk pengiriman data ke display yaitu di pin STB.

12 Pin 16 (P3.6) merupakan outputan dari mikro untuk mengirim data ke display Data.

13 Pin 17 (P3. 7) merupakan data yang akan dikirim ke display CLK.

14 Pin 21-25 (P2.0-P2.4) sebagai inputan sakalar push_button

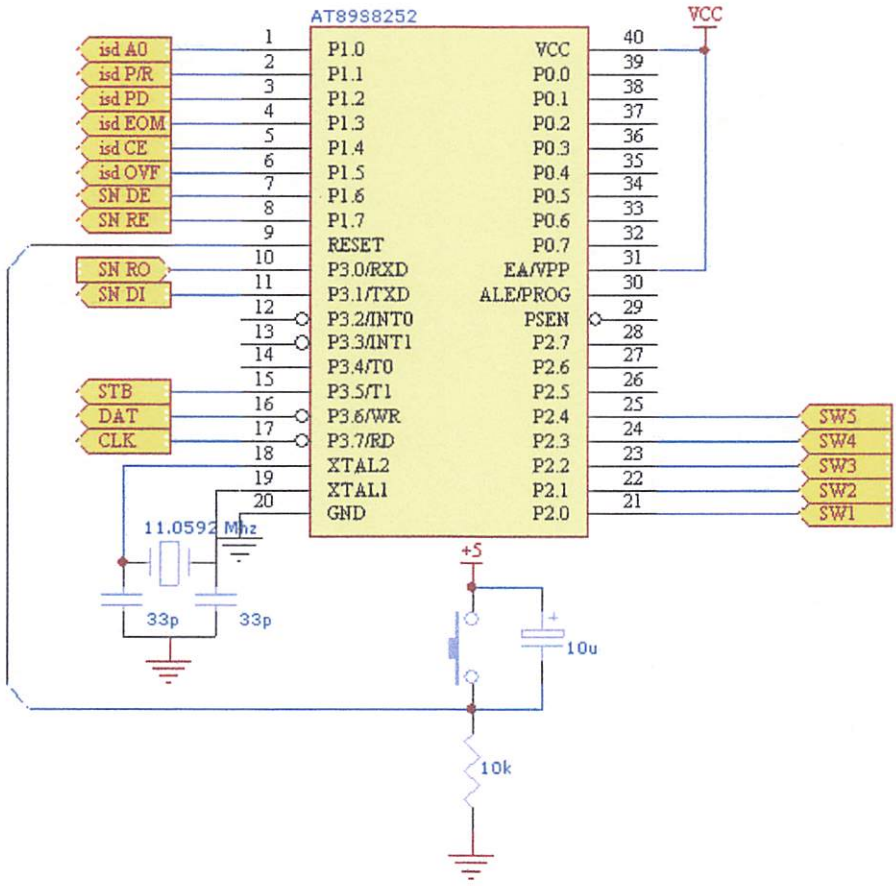
15 Pin 18 (XTAL 2) sebagai pembangkit ossilator (clock) XTAL 2

16 Pin 19 (XTAL 1) sebagai Pembangkit Ossilator (clock) XTAL 1

17 Pin 9 berfungsi sebagai Reset.

18 Pin 31 (EA/VPP) berfungsi sebagai VCC + 5 Volt

Mikrokontroller pada alat ini tidak dapat bekerja sendiri sehingga masih membutuhkan komponen – komponen pendukung lain, komponen – komponen tersebut saling berhubungan secara hardware dan juga sofware. Rangkaian mikrokontroller dapat dilihat pada gambar dibawah ini:



Gambar 3.3 Rangkaian Mikrokontroller AT89S8252

3.2.1. Minimum Sistem AT89S8252

Mikrokontroller AT89S8252 dirancang untuk dapat berdiri sendiri, karena sudah terdapat 2 Kbytes EEPROM, 256 bit RAM internal, 32 *Programmable I/Ollines*, dan terdapat dua 16 bit timer/counters. Dari fasilitas-fasilitas tersebut dapat memfungsikan mikrokontroller AT89S8252 untuk bekerja dalam *single chip*, maksudnya dengan sebuah mikrokontroller saja sudah dapat mengontrol

kerja dari keseluruhan sistem. Dalam perancangan ini digunakan 1 buah mikrokontroller AT89S8252.

- ALE/PROG

  Pulsa ALE (*Address Latch Enable*) hanya digunakan untuk akses ke eksternal memori. Sedangkan PROG digunakan untuk input program selama program *Flash* memori. Karena dalam perancanagn ini menggunakan *single chip* maka untuk pin ALE/PROG tidak digunakan.

- PSEN

  Program Strobe Enable berfungsi membaca *strobe* ke program memori eksternal. Untuk itu PSEN tidak digunakan.

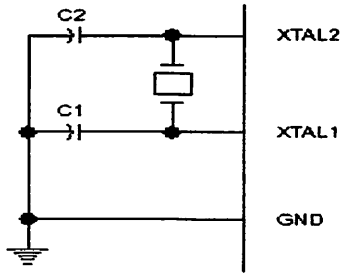
- EA/Vpp

  Logika yang diberikan pada pin ini menunjukkan kerja dari mikrokontroller AT89S51. Pin ini dihubungkan ke Vcc karena pada perancangan ini tidak memanfaatkan memori eksternal.

- XTAL1 dan XTAL2

  Kecepatan proses yang dilakukan oleh mikrokontroller ditentukan oleh sumber *clock* (pewaktu) yang dikendalikan oleh mikrokontroller tersebut. Untuk mendapatkan *clock* pada mikrokontroller, maka digunakan pin XTAL1 dan XTAL2 yang dihubungkan dengan sebuah kristal yang sudah terancang dan tersedia di dalam chip AT89S8252. Besar XTAL yang digunakan adalah 11,059 MHz dan kapasitansinya sebesar 33 pf yang sesuai dengan spesifikasi pada data sheet AT89S8252 dengan frekuensi pewaktu berdasarkan kebutuhan dan kecepatan waktu pelaksaan intruksi.

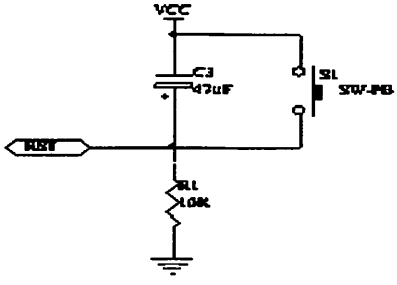
Untuk menjaga kestabilan *clock*, maka ditambah 2 buah kapasitor seperti pada gambar dibawah ini:



Gambar 3.4 Rangkaian Clock

- *Reset*

Untuk melakukan reset sistem pada mikrokontroller yaitu untuk mengawali eksekusi program pada alamat paling rendah yang dapat dimanfaatkan pin reset yang ada pada mikrokontroller. Pin 9 dihubungkan dengan rangkaian *reset* rangkaian ini diharapkan agar dapat mempunyai kemampuan *power ON Reset*, yaitu Reset terjadi saat *power* diaktifkan. Dibawah ini adalah adalah rangkaian reset :



Gambar 3.5. Rangkaian Reset

Sehingga dengan komponen resistor dengan nilai 10 K serta kapasitor dengan nilai 47μF akan dihasilkan :

$$T = R.C \ \text{Ln}\, 2$$

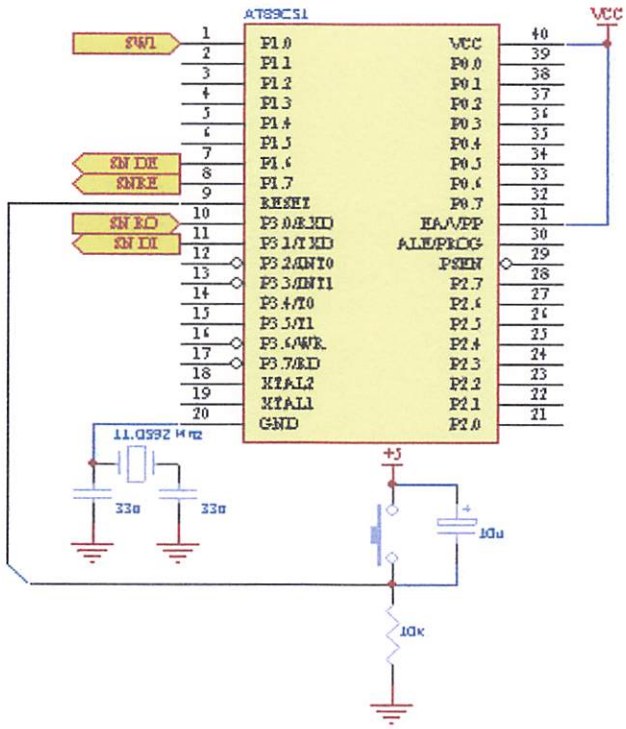
$$= 3{,}2\mu s$$

3.3 Mikrokontroller AT89C51

Mikrokontroller AT89C51 adalah sebuah chip IC yang terdiri dari 40 pin. Dalam perencanaan sistem ini pin – pin yang digunakan adalah sebagai berikut: Adapun fungsi dari masing – masing pin tersebut adalah:

1. Pin 1 (P1.0) merupakan port input mikrokontroler dari sensor tekan.
2. Pin 7 (P1.6) merupakan port output dari mikrokontroller ke serial.
3. Pin 8 (P1.7) merupakan port output dari mikrokontroller ke serial.
4. Pin 10 (P3.0) merupakan port input mikrokontroller dari serial.
5. Pin 11 (P3.1) merupakan port output dari mikrokontroller ke serial.
6. Pin 9 berfungsi sebagai Reset.
7. Pin 31 dan 40 berfungsi sebagai VCC.

Mikrokontroller pada alat ini tidak dapat bekerja sendiri sehingga masih membutuhkan komponen – komponen pendukung lain, komponen – komponen tersebut saling berhubungan secara hardware dan juga sofware. Rangkaian mikrokontroller dapat dilihat pada gambar dibawah ini:



Gambar 3.6 Rangkaian Mikrokontroller AT89C51

3.3.1 Minimum Sistem AT89C51

1. ALE/PROG

   Pulsa output ALE digunakan untuk proses-proses '*latching*' *byte address* rendah (A0-A7) selama pengaksesan ke external memori. Pin ini juga digunakan untuk memasukkan pulsa program (prog) selama pemrograman.

2. PSEN

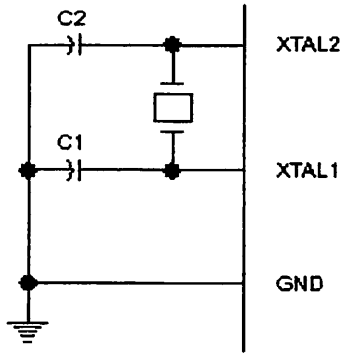
   Merupakan strobe baca ke program memori ekternal.

3. EA/VPP

   External Address Enable (EA) digroundkan jika mengakses memori ekternal, akan dihubungkan ke VCC jika digunakan untuk mengakses memori internal.

4. X-TALL 1 dan X-TALL 2

   Kaki ini dihubungkan dengan kristal bila menggunakan osilator internal. XTALL 1 merupakan input inverting osilator amplifier sedangkan X-TALL 2 merupakan output inverting osilator amplifier.

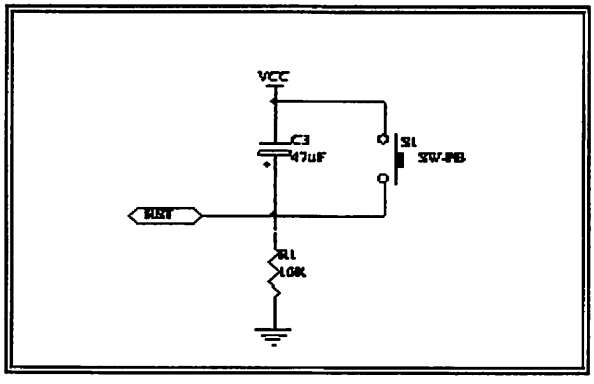


Gambar 3.7 Rangkaian Clock

5. Reset

   Perubahan taraf tegangan dari rendah ketinggi akan mereset AT 89C51.

   T = R.C Ln 2



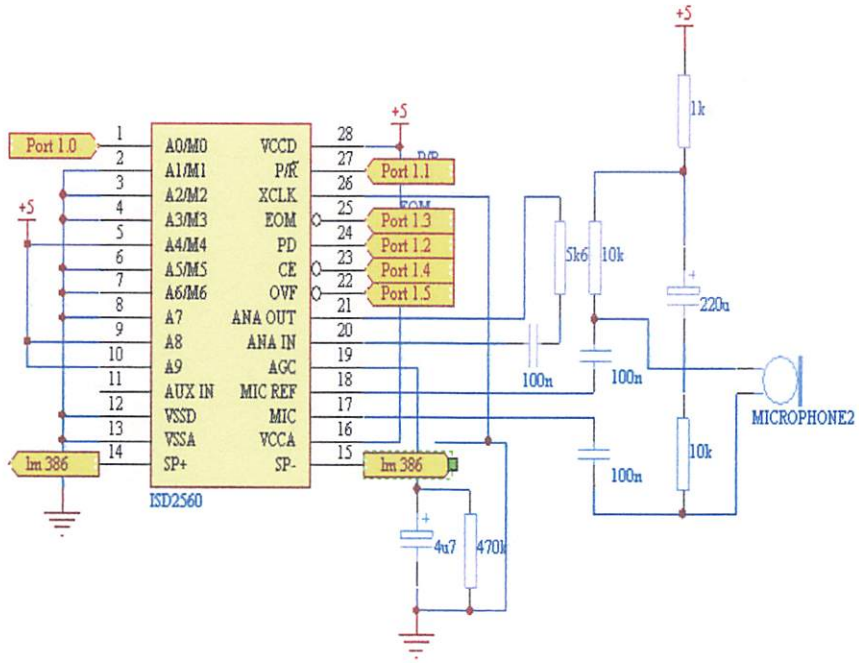
Gambar 3.8 Rangkaian Reset

3.4 Perencanaan ISD 2560

Pada perencanaan dan pembuatan alat ini, suara yang direkam menggunakan voice processor ISD 2560. berdasarkan data sheet ISD 2560 mampu merekam suara dengan lama perekaman 60 detik. Demikian pula untuk waktu putar ulangnya juga selama 60 detik.

ISD dengan tipe 2560 ini mempunyai 256k cell penyimpanan yang didesain untuk menyimpan suara dengan lama 60 detik dengan sample rate 8.0 KHz. ISD 2560 ini melakukan penyimpanan dan pemutar ulang dari perekaman suaranya dapat diatur sedemikian rupa sesuai kehendak dari pemakai dengan melakukan pengendalian atau pengontrolan pada pin-pin alamatnya.

Rangkaian ISD 2560 dengan Mikrokontroller AT89S8252 untuk memutar suara ditunjukkan pada gambar berikut:



Gambar 3.9 Rangkaian ISD 2560

Dalam aplikasinya dengan memberikan input P/R low dan CE low, berarti IC ini berfungsi dalam operasi begin rekam (record) dan siap untuk merekam semua sinyal analog yang masuk melalui mikrofon. Dan dengan memberikan input P/R high, CE pulsed low maka IC ini berfungsi pada operasi begin playback dan PD atau CE high maka IC ini akan end record, sedang untuk end playback adalah otomatis. IC ini akan membaca kembali pesan yang telah tersimpan sebelumnya dan dikeluarkan melalui speaker. Adapun cara kerja dari rangkaian ini adalah:

1. Untuk menyimpan atau merekam suara:
   - Kondisi pin P/R = low (logika "0")
   - Kondisi pin CE = low
   - Kondisi pin PD = high
2. Untuk pemutaran suara:
   - Kondisi pin P/R = high (logika"1")
   - Kondisi pin CE = pulsed low

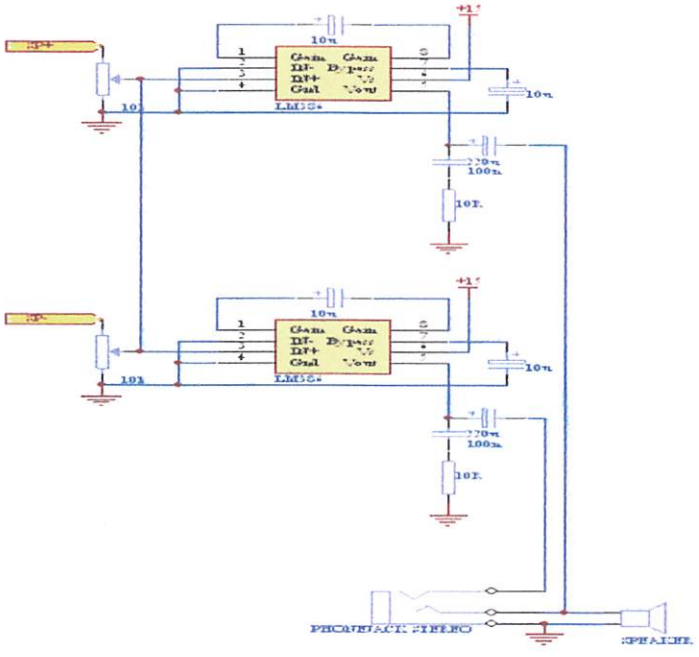
Pemutaran ulang dalam perancangan ISD ini, menggunakan mode operasional yaitu MO (Message Cueing) yang akan memungkinkan untuk melewati pesan, tanpa mengetahui alamat pasti pesan tersebut. Setiap CE Low menyebabkan pointer untuk melewati pesan selanjutnya. Ketika mengoperasikan mode ini, waktu internal dipercepat 800 kali. Mode ini digunakan untuk play back dan secara khusus digunakan dengan mode operasional M4.

Dalam mode M4 (Alamat Berurutan), pointer akan mengeset ulang ketika pesan ditampilkan melalui EOM marker. Mode operasional M4 menghalangi

pointer untuk mereset pada EOM, memungkinkan pesan ditampilkan ulang secara berurutan.

3.5 Rangkaian Penguat Audio

Pada perancangan alat ini yang di gunakan sebagai output dari ISD adalah suara yang sudah di rekam ISD. Pendeteksian suara yang keluar menggunakan rangkaian penguat audio, dan menguatkan suara yang akan di keluarkan melalui speker. Rangkaian ini di gunakan untuk menguatkan audio dari ISD. Rangkaian penguat audio yang di gunakan terdiri dari penguat kerja *LM 386* , beberapa capasitor dan resistor. Tegangan referensi adalah +15V. Untuk komponen tahanannya berupa variabel resistor di gunakan sebesar 10K dan kapasitansinya di gunakan untuk memperkuat rangkaian penguat audio. Rangkaian penguat audio dapat dilihat dalam gambar:

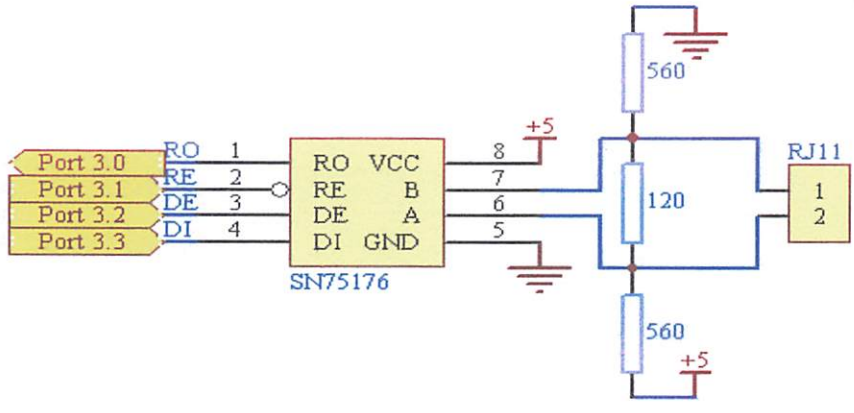


Gambar 3.10 Rangkaian penguat audio

3.6 IC SN75176

Agar Mikrokontroller AT89S8252 Unit dapat berkomunikasi dengan jarak jauh dengan push button untuk nilai "0" maka dibutuhkan penguat transmisi data serial (buffer) yaitu dengan menggunakan penguat SN75176. Penguat SN75176 disini digunakan agar data serial yang dikirimkan dari push button untuk nilai "0" dapat menjangkau mikrokontroler AT 89S8252, tetapi alat ini menggunakan kabel panjang maka pasti ada rugi-rugi yang disebabkan oleh kabel, Dalam alat ini penguat SN75176 hanya mampu mentransmisikan data serial dengan jarak dekat. Jadi penguat SN75176 ini untuk memperpanjangan jarak agar tidak terjadi rugi-rugi dalam pengiriman data.

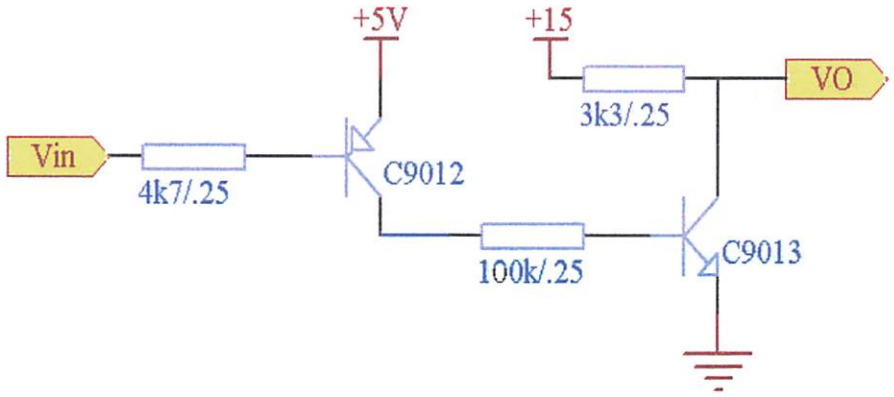
Gambar rangkaian penguat SN75176 yang digunakan pada perancangan alat ini ditunjukkan sebagai berikut :



Gambar 3.11 Rangkaian penguat SN 75176

3.7 Transistor Sebagai Saklar dan Penguat

Pada dasarnya sebuah display mengeluarkan sinyal yang sangat kecil sehingga tidak dapat dideteksi oleh alat ukur biasa. Karena itu di dalam aplikasinya sebuah display memerlukan sebuah rangkaian saklar dan penguat (Amplifier) agar sinyal yang dihasilkan sesuai dengan yang diinginkan dan mampu menggerakkan rangkaian lainnya. Sebuah rangkaian saklar dan penguat transistor bipolar dengan menggunakan konfigurasi CE (Common Emitor) diperlihatkan pada gambar 3.12 dibawah ini:



Gambar 3.12 Rangkaian Transistor sebagai Saklar dan penguat

Asas kerja dari transistor adalah akan ada arus diantara terminal-terminal kolektor-emitor (Ic) hanya apabila ada arus yang mengalir diantara terminal basis-emitor (Ib). jadi transistor harus dioperasikan di daerah linier agar diperoleh sinyal keluaran yang tidak cacat (distorsi) untuk dapat mengoperasikan secara tepat maka pengertian tentang karakteristik, titik kerja, disipasi daya transistor, dan rangkaian bias (ada yang menyebutnya dengan pra tegangan, tegangan kerja awal) amatlah penting.

Agar dapat mengkondisikan transistor sebagai saklar maka kita dapat menghitung nilai Rb sebagai berikut:

$$Ib = \frac{Ic}{\beta dc}$$

$$Ib = \frac{50mA}{64}$$

$$Ib = 0{,}78mA$$

$$Rb = \frac{Vcc - Vbe}{Ib}$$

$$Rb = \frac{5 - 1{,}2}{0{,}78mA}$$

$$Rb = 4871\Omega = 4K8$$

Karena keterbatasan komponen di pasaran maka Rb=4K7

Agar dapat mengkondisikan transistor 9013 sebagai penguat, Dengan menentukan nilai Rc sebesar 3K3 maka kita bisa menghitung nilai Ic:

$$Ic = \frac{15}{3K3}$$

$$Ic = 4{,}5mA$$

Dari data sheet diketahui nilai Bdc dari transistor 9013 =120 maka nilai Ib dapat dicari:

$$Ib = \frac{Ic}{\beta dc}$$

$$Ib = \frac{4{,}5mA}{120}$$

$$Ib = 0{,}0375mA$$

Setalah nilai Ic dan Ib sudah dicari maka kita dapat mencari nilai Rb:

$$Rb = \frac{Vin - Vbe}{Ib}$$

$$Rb = \frac{5 - 1{,}2}{0{,}0375mA}$$

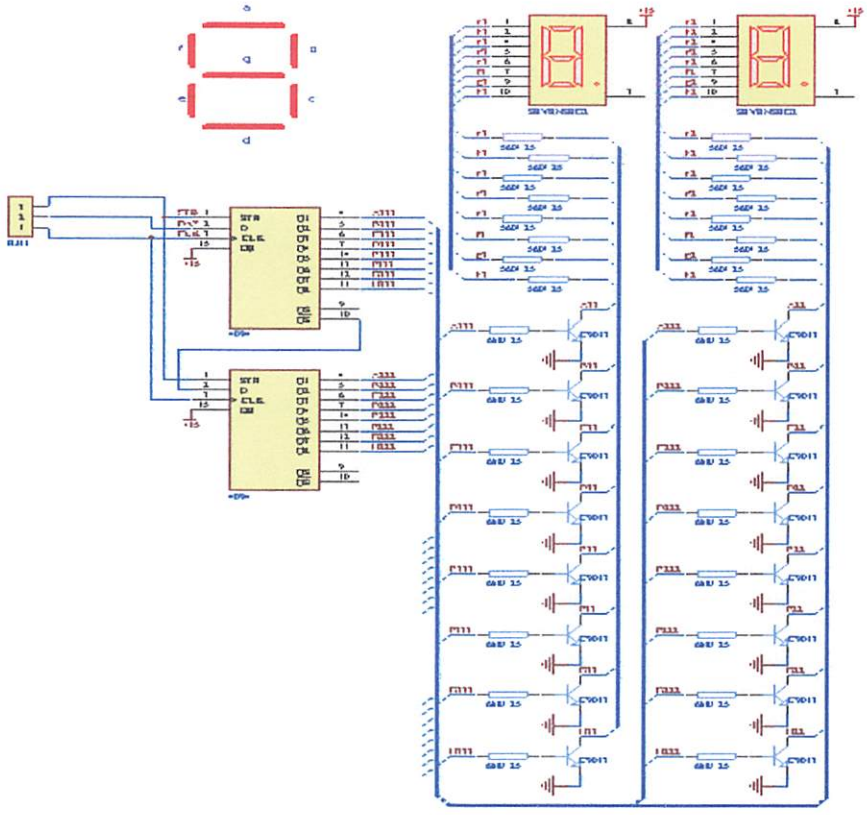
$$Rb = 101K\Omega$$

Karena keterbatasan komponen maka nilai Rb=100KΩ

3.8 Rangkaian Display Seven Segmen

Seven Segmen terdiri dari tujuh buah Led yang dikemas dalam satu kemasan. Antara dua kaki yang oleh Led tersebut salah satu kaki dari tujuh Led tersebut saling dihubungkan satu sama lain atau lebih dikenal dengan common. Common pada seven segmen yang di gunakan dalam perencanaan ini adalah jenis common anoda.

Pada perencangan alat ini seven segmen digunakan sebagai tampilan angka-angka dari 00 sampai 99, tapi pada alat ini angka yang di tampilkan dari 00 sampai 54. seven segmen ini dipasang untuk mengetahui nilai dari hasil dari pemanah yang terdiri dari 2 buah seven segmen. Gambar dari rangkaian seven segmen terlihat seperti gambar 3.13 di bawah ini:



Gambar 3.13 Rangkaian display

Untuk menyalakan satu Led membutuhkan penguatan yaitu sebuah transistor untuk mengatur terang gelapnya cahaya dari seven segmen tersebut. Penguatan ini menggunakan transistor jenis C9013. Dengan perhitungan sebagai berikut:

$$Il = Ic = \frac{Vcc - Vled}{Rc}$$

$$Ic = \frac{15 - 2{,}5}{560}$$

$$Ic = 22mA$$

Nilai Ic = 22 mA, maka nilai Ib dapat dicari:

$$Ib = \frac{Ic(sat)}{Hfe}$$

$$Ib = \frac{22mA}{64}$$

$$Ib = 0{,}34mA$$

Dari perhitungan ini dapat dicari nilai Vin:

$$Vin = IbxRB + Vbe$$

$$Vin = 0{,}34x6800 + 1{,}2$$

$$Vin = 3{,}37V$$

Untuk mencari Rc adalah dengan menggunakan rumus:

$$Rc = \frac{Vcc}{Ic}$$

$$Rc = \frac{15}{22mA}$$

$$Rc = 681\Omega$$

karena keterbatasan nilai resistor yang terdapat dipasaran, maka dipilih nilai resistansi dengan nilai terdekat yaitu 560 Ohm.

Sehingga nilai Rb:

$$Rb = \frac{Vin - Vbe}{Ib}$$

$$Rb = \frac{3{,}37 - 1{,}2}{0{,}34mA}$$

$$Rb = 6{,}38K\Omega$$

Karena tahanan memiliki nilai toleransi maka nilai dari Rb yang digunakan sebesar 6K8

3.9 Sensor Tekan (Push Button)

Rangkaian push button digunakan untuk memberikan masukan pada Mikrokontroler AT89S8252 berupa *high* atau *low,* sinyal tersebut akan di gunakan untuk masukan nilai yang mengenai sasaran.

Rangkaian push button ini berguna untuk membentuk logika *high* pada saat push button ditekan. Demikian sebaliknya, jika push button tidak ditekan maka output rangkaian adalah *low.*

Pada saat push button dalam keadaan tertutup maka tegangan di keluarkan sebesar 5V, tetapi pada saat push button dalam keadaan terbuka, diharapkan tegangan keluaran mendekati 0 volt. Ini dapat dicapai dengan pertimbangan sebagai berikut:

Tegangan supply (Vcc) = 5 Volt

Arus (I) = 0,01mA (Arus yang dibutuhkan oleh masukan mikrokontroler

Tegangan Keluaran (V out) = 5 Volt (atau 4,9 Volt)

Maka R dapat dicari:

Vcc = I x R + Vout

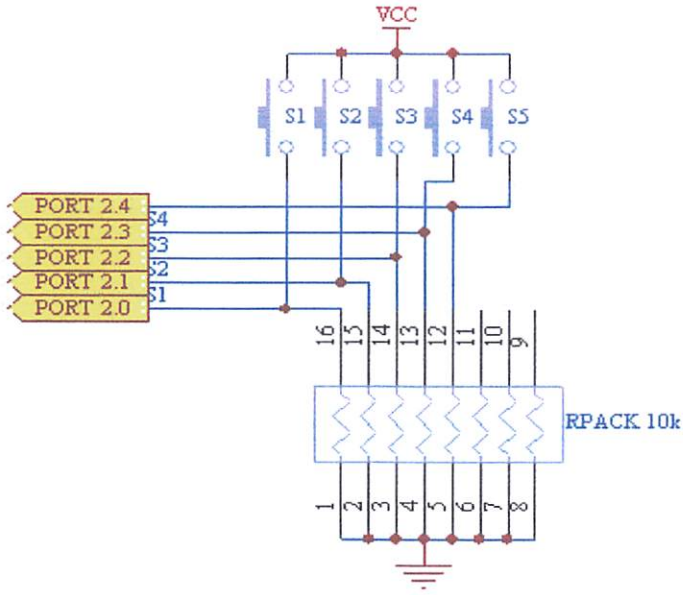
$5 = (0{,}01 \times 10^{-3} \times R) + 4{,}9$

$$R = \frac{0{,}1}{0{,}01 x 10^{-3}}$$

$R = 10000\,\Omega$

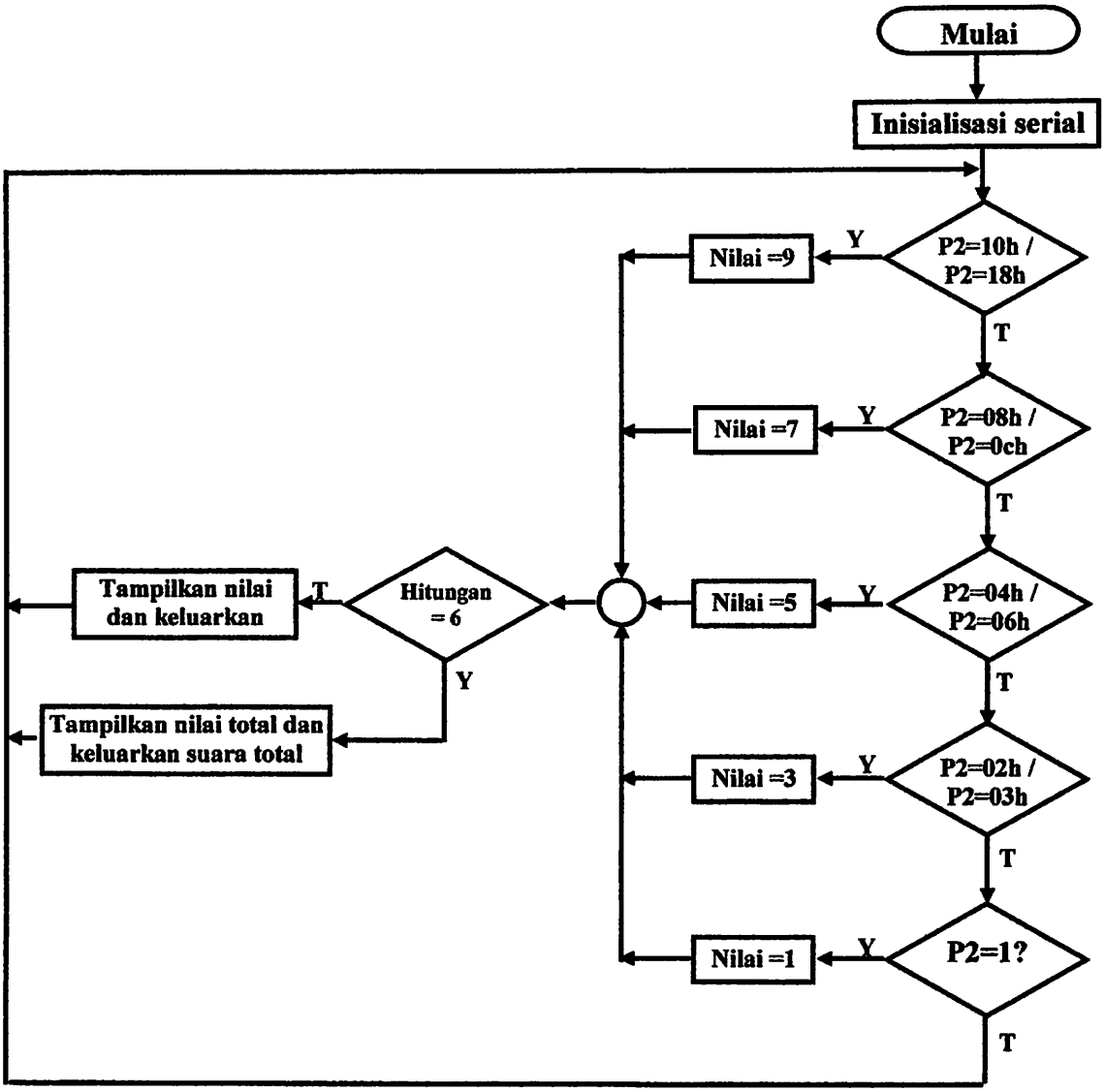
Maka nilai $R = 10K\,\Omega$

Di bawah ini merupakan rangkaian dari push button:

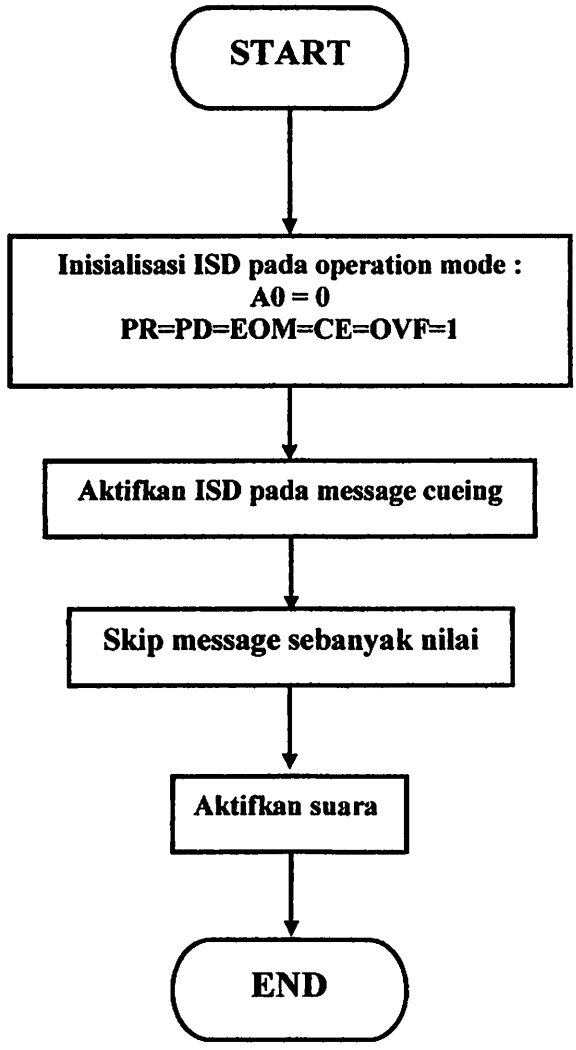


Gambar 3.14 Rangkaian Push Button

Flowchart Program



Flowchart ISD



BAB IV

PENGUJIAN ALAT

4.1 Umum

Pengujian alat ini dilakukan untuk mengetahui kinerja dari keseluruhan sistem rangkaian. Jadi pada tahap ini akan diketahui nilai-nilai serta parameter-parameter dari setiap bagian yang menyusun sistem secara keseluruhan.

4.2 Pengujian Sensor Tekan (Push Button)

1. Tujuan

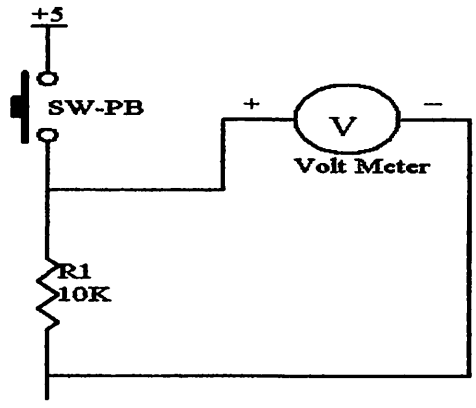
Untuk mengetahui apakah push button dapat bekerja dengan baik dan mampu mengkondisikan keluaran menjadi kondisi *high* atau *low*.

2. Peralatan yang digunakan

- Multimeter Digital
- Power Supply 5 volt
- Rangkaian Push Button yang telah dirancang

3. Prosedur Pengujian

- Membuat rangkaian sensor push button seperti pada gambar 4.1.
- Menghubungkan rangkaian dengan power supply 5 volt.
- Mengukur besarnya arus dan tegangan dengan menggunakan multimeter.
- Pengujian dilakukan dalam dua kondisi yaitu saat tidak ada penekanan dan ada penekanan.
- Memasukkan hasil pengukuran pada tabel 4.1



Gambar 4.1 Pengujian Rangkaian Push button

4. Hasil pengujian

Tabel 4.1 Hasil Pengujian Rangkaian Push button

Perlakuan Tombol	Tegangan (V)				
	Tombol Nilai 9	Tombol Nilai 7	Tombol Nilai 5	Tombol Nilai 3	Tombol Nilai 1
Ada Penekanan	4.6 v	4.6 v	4.6 v	4.6 v	4.6 v
Tidak Ada Penekanan	0 v	0 v	0 v	0 v	0 v

Dari hasil pengujian Push button pada tabel 4.1 diatas, maka dapat diketahui bahwa pada saat ada *penekanan tombol* dan tegangan yang dihasilkan adalah 4,6 volt, maka digolongkan sebagai logika *high* sebagai inputan mikrokontroller, sebaliknya pada saat kondisi *tidak ada penekanan tombol* dan tegangan yang dihasilkan adalah 0 volt, maka digolongkan logika *low* atau tidak sebagai inputan mikrokontroller.

5. Pengukuran dan Pengujian push button

Untuk pengukuran dan pengujian push button yaitu dengan mengukur respon tekanan yang di berikan terhadap push button dengan menguji dan mengukur jarak pelemparan terhadap area peletakan push button. Dapat dilihat pada tabel 4.2

Tabel 4.2 Hasil pengukuran dan Pengujian Push button

Area Push Button	Jarak Pelemparan Maximum	Pelemparan keras	Pelemparan sedang	Pelemparan pelan
0 cm	5 m	√	√	√
1 cm	4,5 m	√	√	√
2 cm	4 m	√	√	–
3 cm	3,5 m	√	√	–
4 cm	3 m	√	√	–
5 cm	2,5 m	√	–	–

4.3 Pengujian Display (Seven Segmen)

1. Tujuan

Untuk mengetahui apakah seven segmen yang bibuat tersebut dapat menampilkan angka.

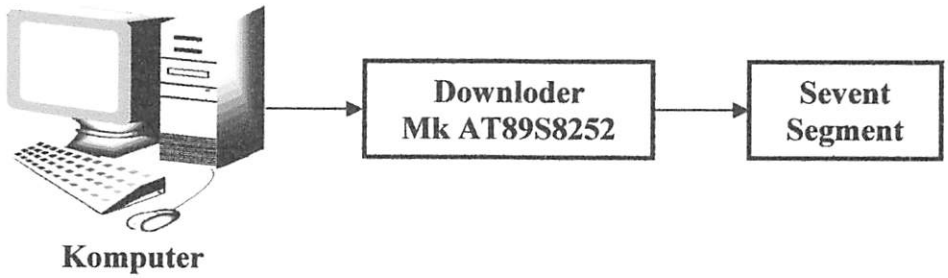
2. Peralatan yang digunakan

- PC (Personal Computer)
- Mikrokontroler dan Downlodernya
- Seven Segmen

- Catu daya 5 volt

3. Prosedur Pengujian

- Merangkai peralatan yang digunakan sesuai gambar 4.2.
- Memberikan catu daya 5volt pada rangkaian mikrokontroler dan seven segmen.
- Memberikan data ke mikrokontroler.
- Memberikan data ke seven segmen.
- Mengamati tampilan seven segmen.



Gambar 4.2 Pengujian Sevent Segment

4. hasil pengujian

Hasil pengujian seven segmen ditunjukkan dalam tabel 4.3 berikut ini:

Tabel 4.3 Hasil pengujian Seven Segmen

Data	Tampilan Seven Segmen
00111111b	0
00000110b	1
01011011b	2

01001111b	3
01100110b	4
01101101b	5
01111101b	6
00000111b	7
01111111b	8
01101111b	9

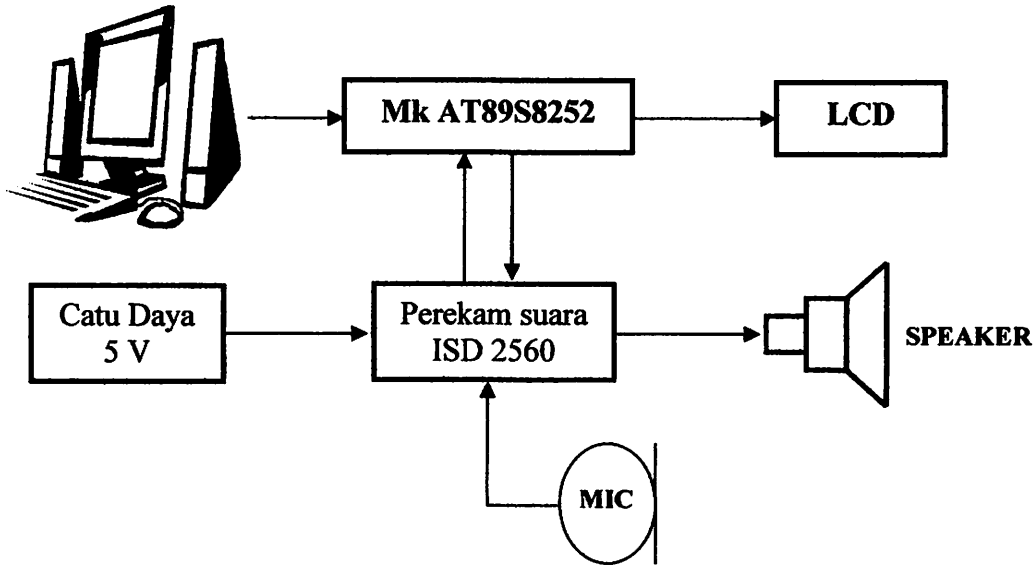
4.4 Pengujian Rangkaian ISD 2560

1. Tujuan

Mengetahui bagaimana kerja ISD 2560 dalam menyimpan suara dan sekaligus dapat mengulang kembali suara dengan menggunakan media mikropon dan speaker.

2. Peralatan yang digunakan

- Mikropon
- Speaker
- Catu daya 5V
- LCD
- PC (Personal Computer)



Gambar 4.3 pengujian Rangkaian ISD 2560

3. Prosedur pengujian

- Merangkai seperti blok diagram dalam gambar 4.3
- Mengaktifkan catu daya 5V
- Proses perekaman
  - kondisi pin P/R = low
  - kondisi pin CE = low
- Proses Playback
  - kondisi pin PD = high
  - kondisi pin CE= low

4. Hasil Pengujian

Hasil pengujian rangkaian ISD 2560, sesuai dengan langkah-langkah diatas maka untuk memplayback pesan "N", dilakukan sebagai berikut:

1. Ubah pin PD ke low dan delay Tpud.
2. Ubah P/R ke High.
3. Jika N=1 (pesan pertama), lalu AO=0 dan pulse CE low. Pesan pertama akan mulai dan kemudian berhenti.
4. Jika N lebih besar dari 1, harus melakukan N-1 AO Message Cueing pada mode operasional, dengan melakukan langkah-langkah sebagai berikut:
    a. Ubah AO =0
    b. Pulse CE low
    c. Tetap pada low EOM
    d. Setiap menemukan EOM, berarti telah mencapai pesan, dan akan bergerak melalui pesan pada 800 kali kecepatan normal.
    e. Kurangi 1 dari N, jika N tidak sama, lakukan kembali ke langkah (a) dan lakukan lagi.
5. Jika N telah dikurangi menjadi 1, lalu ubah AO=0 dan pulse CE low. Pesan N akan berjalan pada kecepatan normal.

Tabel 4.4 Proses Pemetaan suara rekaman

Pesan ke	Isi
1	Nol
2	Satu
3	Dua
4	Tiga

5	Empat
6	Lima
7	Enam
8	Tujuh
9	Delapan
10	Sembilan
11	Sepuluh
12	Sebelas
13	Puluh
14	Belas

4.5. Pengujian Rangkaian Serial

1. Tujuan

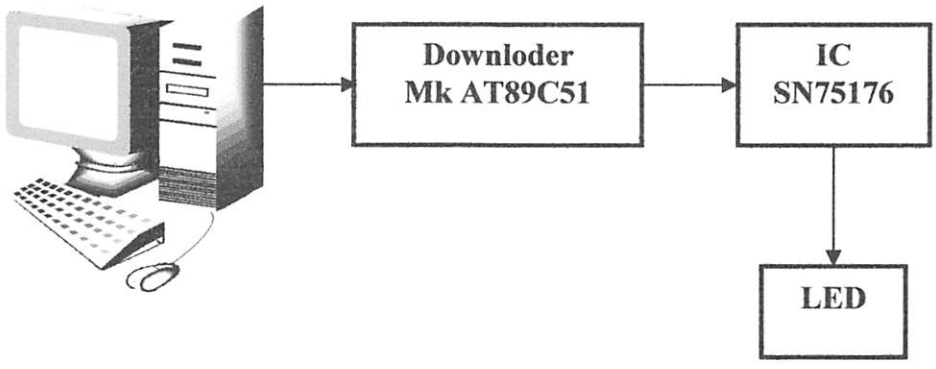
Untuk mengetahui apakah Rangkaian Serial dapat mengirimkan data dengan baik dan mampu mengirim data tanpa menghilangkan data (noise) di tengah jalan karena jarak pengiriman data yang jauh.

2. Peralatan yang digunakan

- PC (Personal komputer)
- Mikrokontroler dan Downlodernya
- Power Supply 5 volt
- Kabel telpon
- Led
- Limit Switch

3. Prosedur Pengujian

- Merangkai peralatan yang digunakan sesuai gambar 4.4.
- Memberikan catu daya 5 volt pada rangkaian mikrokontroler dan IC SN75176.
- Memberikan data ke mikrokontroler.
- Memberikan data ke IC SN75176.
- Mengamati tampilan Led.



Gambar 4.4 Pengujian Rangkaian Serial

4. Hasil pengujian

Tabel 4.5 Hasil Pengujian Rangkaian Serial

Data	Led
00 H	Mati
FE H	Mati
FF H	Nyala

Dari hasil pengujian rangkaian serial pada tabel 4.5 diatas, maka dapat diketahui bahwa pada saat ada *penekanan tombol* dari Rangkaian serial pertama, dimasukkan data 00H-FEH ternyata Led dirangkaian serial kedua tidak menyala, Sedangkan pada waktu dimasukkan data FFH Led menyala.

4.6 Hasil Pengujian Tembakan Anak Panah Pada Papan Target

Tabel 4.6

Pengujian Tingkat Keberhasilan dalam tembakan anak panah pada papan target

Kuning	Nilai	Keterangan
1	9	Berhasil
2	9	Berhasil
3	9	Berhasil
4	9	Berhasil
5	9	Berhasil

Merah	Nilai	Keterangan
1	7	Berhasil
2	7	Berhasil
3	7	Berhasil
4	7	Berhasil
5	7	Berhasil

Biru	Nilai	Keterangan
1	5	Berhasil
2	5	Berhasil
3	5	Berhasil
4	5	Berhasil
5	0	Tidak Berhasil

Hitam	Nilai	Keterangan
1	3	Berhasil
2	3	Berhasil
3	3	Berhasil
4	3	Berhasil
5	3	Berhasil

Putih	Nilai	Keterangan
1	1	Berhasil
2	1	Berhasil
3	1	Berhasil
4	1	Berhasil
5	0	Tidak Berhasil

Garis antara kuning dan merah	Nilai	Keterangan
1	9	Berhasil
2	9	Berhasil
3	7	Tidak Berhasil
4	9	Berhasil
5	9	Berhasil

Garis antara merah dan biru	Nilai	Keterangan
1	7	Berhasil
2	7	Berhasil
3	7	Berhasil
4	7	Berhasil
5	5	Tidak Berhasil

Garis antara biru Dan hitam	Nilai	Keterangan
1	5	Berhasil
2	3	Tidak Berhasil
3	5	Berhasil
4	5	Berhasil
5	5	Berhasil

Garis antara hitam Dan putih	Nilai	Keterangan
1	3	Berhasil
2	3	Berhasil
3	3	Berhasil
4	3	Berhasil
5	1	Tidak Berhasil

- *Berhasil* adalah data yang diterima mikrokontroller pada saat pelemparan anak panah pada papan score.
- *Tidak berhasil* adalah data yang tidak diterima mikrokontroller pada saat pelemparan anak panah pada papan score.

Data diambil dari jarak maximal 5 meter, Untuk warna kuning dengan nilai 9, 5 kali pelemparan berhasil semua. Warna merah dengan nilai 7, 5 kali pelemparan berhasil semua. Warna biru dengan nilai 5, 5 kali pelemparan 1 kali tidak berhasil. Warna hitam dengan nilai 3, 5 kali pelemparan berhasil semua. Warna putih dengan nilai 1, 5 kali pelemparan 1 kali tidak berhasil. Garis antara kuning dan merah dengan nilai 9, 5 kali pelemparan 1 kali tidak berhasil. Garis antara merah dan biru dengan nilai 7, 5 kali pelemparan 1 kali tidak berhasil.

Garis antara biru dan hitam dengan nilai 5, 5 kali pelemparan 1 kali tidak berhasil, garis antara hitam dan putih dengan nilai 3, 5 kali pelemparan 1 kali tidak berhasil. Dari hasil pengujian terlihat bahwa sistem bekerja cukup baik bila dicoba dengan jarak maksimal 5 meter. Terbukti dari besarnya tingkat keberhasilan pelemparan anak panah ke papan target sebanyak 45 pelemparan yang hampir berhasil semua.

Namun dari seluruh hasil pengujian tetap didapatkan kesalahan yang terjadi, yaitu sebanyak 6 tidak berhasil dari 45 pelemparan. Kesalahan ini dapat terjadi karena beberapa hal, antara lain jarak antara pelemparan anak panah pada papan target, kekuatan tekanan, maupun faktor kesalahan manusia yang terjadi dalam penggunaan alat ini.

BAB V
PENUTUP

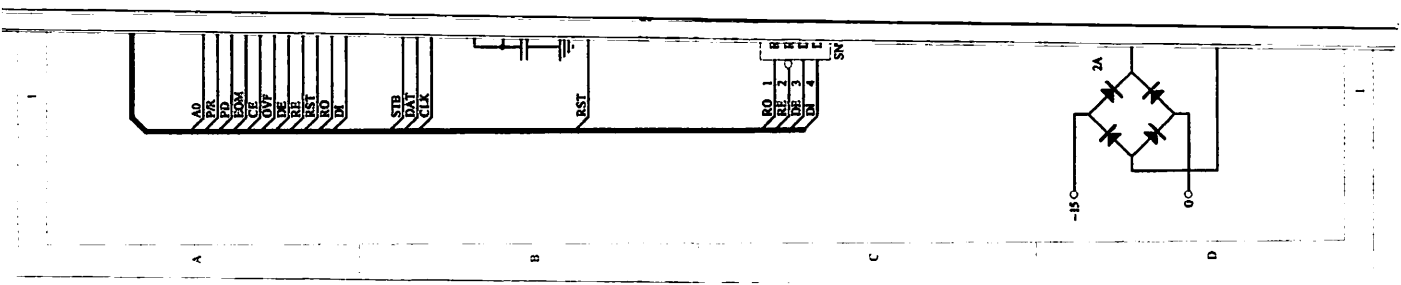
5.1. Kesimpulan

Dari hasil perancangan dan pembuatan serta pengukuran alat yang telah dilakukan dapat disimpulkan bahwa :

1. Sistem kontrol dalam perancangan ini menggunakan Mikrokontroller AT 89S8252 sebagai pengendali utama dan pengolah data dari masukan Sensor tekan (push button).
2. Berdasarkan pengujian jarak antara respon push button terhadap tekanan pelemparan diperoleh kesensitifan push button paling besar pada area titik 0 cm dengan maximal jarak push button sebesar 5m , sehingga pada area titik 5 cm dari push button didapat jarak maximal adalah 2,5 m dengan tekanan yang keras..
3. Dari pengujian sampel lemparan anak panah ke papan skor sebanyak 45 kali, jumlah yang berhasil 39 kali sehingga didapat kesalahan dalam pengujian ini sebesar 6 kali. Kesalahan ini dapat terjadi karena beberapa hal, antara lain jarak antara pelemparan anak panah pada papan target, kekuatan tekanan, maupun faktor kesalahan manusia yang terjadi dalam penggunaan alat ini.

5.2. Saran – saran

1. Untuk pengembangan lebih lanjut, ada baiknya jika papan skor lebih disempurnakan lagi agar anak panah dapat lebih menancap pada papan skor.
2. Peletakan sensor pada alat ditempatkan pada posisi yang tepat agar lebih presisi.
3. Dalam perencanaan alat ini bentuk papan skor dibuat hanya prototype, oleh karena itu lemparan anak panah menuju papan skor mungkin masih jauh dari sempurna dari yang diharapkan, karena keterbatasan dan kurang kemampuan papan skor untuk menahan tekanan dari anak panah.



5.2. Saran – saran

1. Untuk pengembangan lebih lanjut, ada baiknya jika papan skor lebih disempurnakan lagi agar anak panah dapat lebih menancap pada papan skor.
2. Peletakan sensor pada alat ditempatkan pada posisi yang tepat agar lebih presisi.
3. Dalam perencanaan alat ini bentuk papan skor dibuat hanya prototype, oleh karena itu lemparan anak panah menuju papan skor mungkin masih jauh dari sempurna dari yang diharapkan, karena keterbatasan dan kurang kemampuan papan skor untuk menahan tekanan dari anak panah.

DAFTAR PUSTAKA

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INSTITUT TEKNOLOGI NASIONAL
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PROGRAM STUDI TEKNIK ELEKTRONIKA
MALANG

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Program Studi	: Teknik Elektronika
Judul Skripsi	: Perancangan dan pembuatan papan skor pada panahan yang dilengkapi dengan keluaran suara berbasis mikrokontroller AT 89S8252
Tanggal Pengajuan Skripsi	: 7 Desember 2005
Selesai Penulisan Skripsi	: Maret 2006
Dosen Pembimbing	: Ir. F. Yudi Limpraptono,MT
Telah Dievaluasi Dengan Nilai	: 90

Mengetahui
Ketua Jurusan Elektro S-1

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Dosen Pembimbing

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Formulir Bimbingan Skripsi

NAMA : SETYO HADI PRAMONO
NIM : 0117043
Masa Bimbingan : 7 Desember 2005 – 8 Mei 2006
Judul Skripsi : **PERANCANGAN DAN PEMBUATAN PAPAN SKOR PADA PANAHAN YANG DI LENGKAPI DENGAN KELUARAN SUARA BERBASIS MIKROKONTROLER AT89S8252**

No	Tanggal	Uraian	Paraf Pembimbing
1	8/2 2006	Bab I & Bab II Perbaiki cara tulis ulang	
2	4/3 2006	Bab III – Bab V	
3	2/3 2006	Materi Seminar hasil	
4	10/3 2006	Bab I – V (Ulang)	
5	13/3 2006	Persiapan Konsep	
6			
7			
8			
9			
10			

Malang, 13-3-2006

Dosen Pembimbing

Ir. F. YUDI LIMPRAPTONO, MT
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FAKULTAS TEKNOLOGI INDUSTRI
JURUSAN TEKNIK ELEKTRO S-1
PROGRAM STUDI TEKNIK ELEKTRONIKA
MALANG

FORMULIR PERBAIKAN SKRIPSI

Dari hasil ujian Skripsi Jenjang Strata Satu (S-1) Jurusan Teknik Elektro Konsentrasi Elektronika yang diselenggarakan pada :

Hari : Senin

Tanggal : 20 Maret 2006

Telah dilakukan perbaikan Skripsi oleh :

Nama : Setyo Hadi Pramono

NIM : 01.17.043

Jurusan : Teknik Elektrto S-1

Program Studi : Teknik Elektronika

Judul Skripsi :Perancangan dan pembuatan papan skor pada panahan yang dilengkapi dengan keluaran suara berbasis mikrokontroller AT 89S8252

No.	Materi Perbaikan	Paraf
1.	Prinsip Push Button berdasarkan jarak	
2.	Penjelasan Error Pengujian	
3.	Kesimpulan	

Disetujui

Mengetahui
Dosen Pembimbing I

Ir. F. Yudi Limpraptono, MT
NIP.Y. 1039500274

Penguji

M. Ashar, ST,MT

INSTITUT TEKNOLOGI NASIONAL
FAKULTAS TEKNOLOGI INDUSTRI
JURUSAN TEKNIK ELEKTRO

Formulir Perbaikan Ujian Skripsi

Dalam pelaksanaan Ujian Skripsi Janjang Strata 1 Jurusan Teknik Elektro Konsentasi T. Energi Listrik / T. Elektronika, maka perlu adanya perbaikan skripsi untuk mahasiswa :

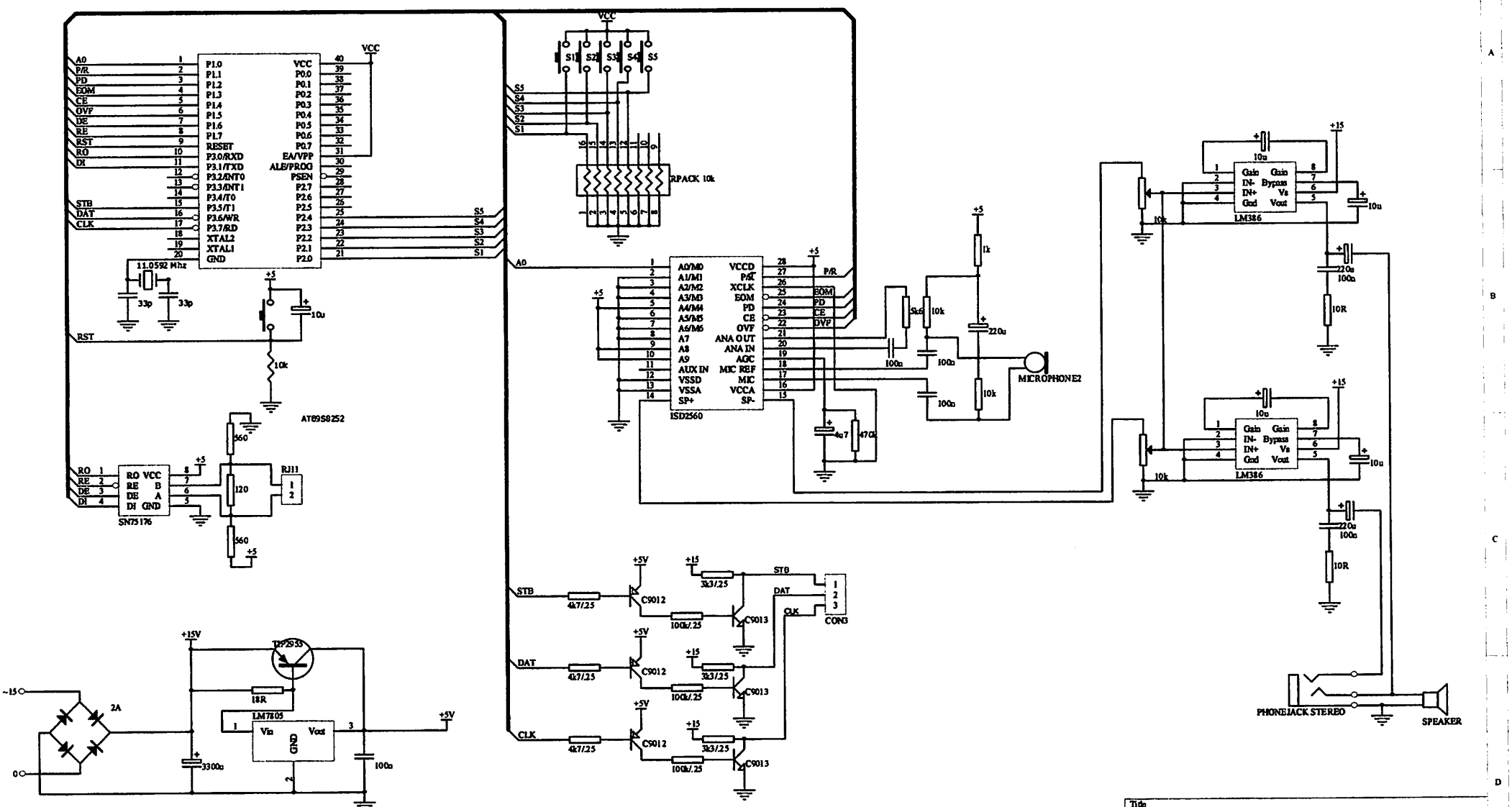
NAMA : Setyohadi P.
NIM : 0117043
Perbaikan meliputi :

- Prinsip push button berdasarkan jarak ?
- Penjelasan Error · pengujian ·
- Kesimpulan

Malang,

(M. ASHAR)

lampiran


AT89S8252
ISD2560
SN75176
LM386
LM386
LM7805
MICROPHONE2
PHONEJACK STEREO
SPEAKER
CON3
RPACK 10k
11.0592 Mhz
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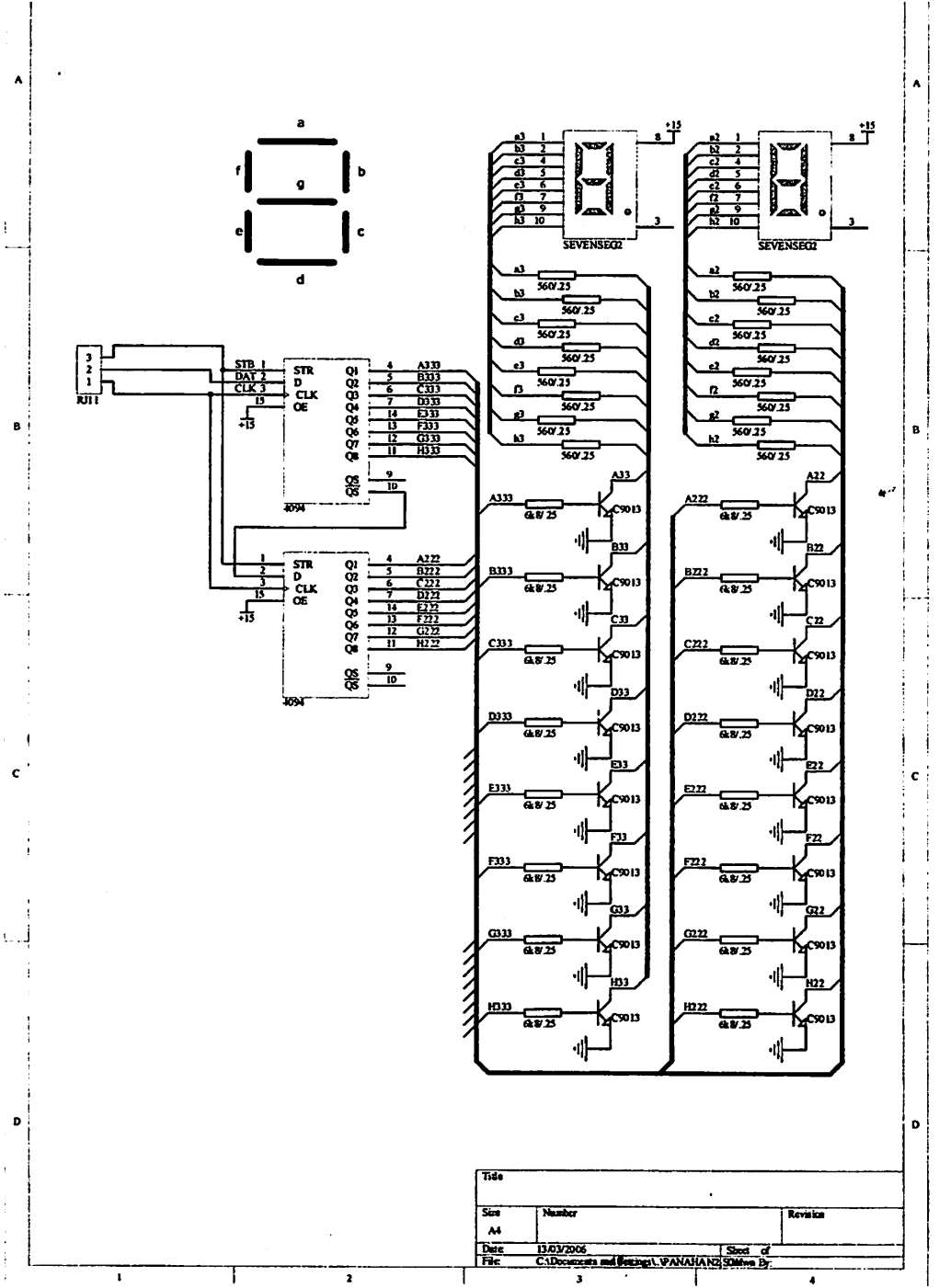
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DAT
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STR
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CLK
OE
4094
4094
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C9013
Title
Size
A4
Number
Revision
Date
13/03/2006
Sheet of
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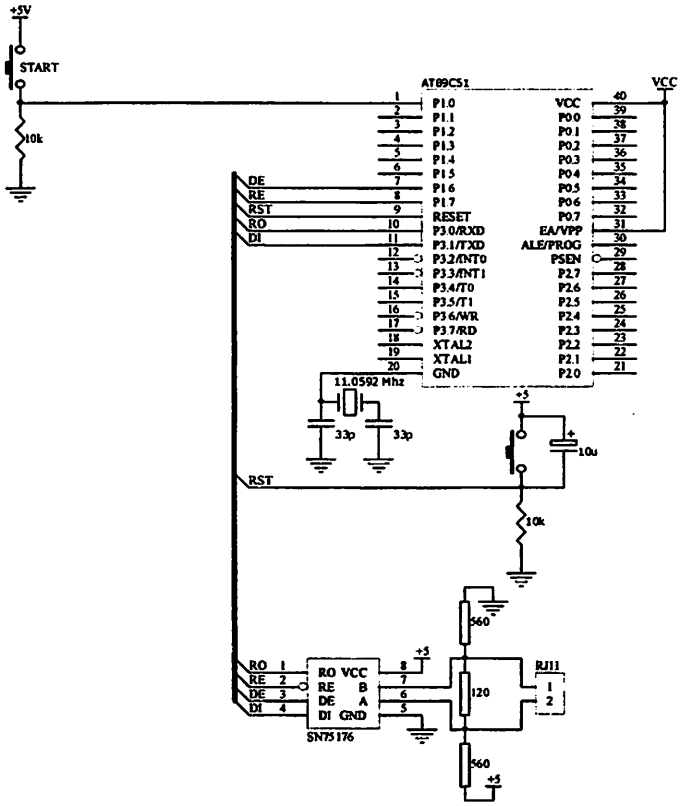


Title		
Size: B	Number	Revision
Date: 13/03/2006	Sheet of	
File: C:\Documents and Settings\...\PANAHAN2.SCH	Drawn By:	

```
#include <at89S8252.h>

// kontrol 4094
#define stb     P3_5
#define dat     P3_6
#define clk     P3_7

//kontrol isd
#define isd_a0      P1_0
#define isd_pr      P1_1
#define isd_pd      P1_2
#define isd_eom     P1_3
#define isd_ce      P1_4
#define isd_ovf     P1_5

#define led         P3_2
#define led_s       P3_3
#define clear       10
#define full        11

volatile unsigned char nilai,hitungan,terima,total,puluhan,satuan;
volatile bit status;
void mainkan();
void tunda1ms();
void tunda(unsigned int n);
void shift_byte( unsigned char byte );
void update_display();
void init_display();
void init_intser();
void Init_Serial(unsigned char baud);
void tampil();
void play();
void go();
void start_skip();

/* fungsi tunda 1 milidetik (kira-kira) */
void tunda1ms()
{
 unsigned char i;
 for(i=0;i<150;i++)
 ;
}

/* fungsi tunda n milidetik */
void tunda(unsigned int n)
{
 unsigned int i;
 for (i=0; i<n;i++)
 tunda1ms();
}

// seven segment
/*
         A           msb                                 lsb
        ####         +---+---+---+---+---+---+---+---+
       #    #        | A | B | C | D | E | F | G | H |
     F #    # B      +---+---+---+---+---+---+---+---+
       # G  #        4094 arah pergeseran >------->>
        ####
       #    #
     E #    # C
       #    #
        ####  #
         D    H
*/

code unsigned char ss_table[12] = {
```

```
    0xfc,   // 0
    0x60,   // 1
    0xda,   // 2
    0xf2,   // 3
    0x66,   // 4
    0xb6,   // 5
    0xbe,   // 6
    0xe0,   // 7
    0xfe,   // 8
    0xf6,   // 9
    0x00,   // clear
    0xff    // full
};

void shift_byte( unsigned char byte ) {
    unsigned char mask = 1;

    while ( mask ) {
        dat = ( byte & mask ) ? 1 : 0;
        mask <<= 1;
        clk = 1;
        tunda(3);
        clk = 0;
        tunda(3);
    }
}

unsigned char ss_buffer[2];

void update_display() {
    unsigned char i;
    for ( i = 0; i < 2; i++ ) {
        shift_byte( ss_table[ ss_buffer[i] ] );
    }

    // STROBE 'em!!
    stb = 1;
    tunda(3);
    stb = 0;
    tunda(3);
}


void init_display() {
    unsigned char i;

    for ( i = 0; i < 2; i++ ) {
        ss_buffer[i] = full;
    }

    update_display();

    tunda(2000);

    for ( i = 0; i < 2; i++ ) {
        ss_buffer[i] = clear;
    }

    update_display();
}

void init_intser()
{
  EA=1;
  ES=1;
  PS=1; //prioritas tinggi
}
```

```
void Init_Serial(unsigned char baud)
  {
     TMOD=0x20;          //timer 1 mode 2 (autoreload)
     PCON=0x0 ;           // SMOD =0
     SM0=0;
     SM1=1;               //mode 1
     REN=1;               //terima dibolehkan
     TH1=baud;            //kecepatan 9600 bps (nilai reload)
     TL1=baud;            //nilai awal timer
     TR1=1;               // timer dijalankan
  }

void IntSerial ()interrupt 4 using 1      //interupsi serial
{
   ES=0;
   RI=0;                  //flag interrupt dinolkan
   terima=SBUF;
   if (terima==0xff)
   {

     led_s=0;
     if (status)
     {
       if (hitungan==0) hitungan+=1;

       else if (hitungan==7)
       {
           ss_buffer[0]=total / 10;
           ss_buffer[1]=total % 10;
           update_display();
           play();
       }

       else if ((hitungan != 0) || (hitungan != 7))
       {
          nilai=0;
          hitungan+=1;
          tampil();
          go();
       }
     }

     else
     {
       status=1;
       if (hitungan==6) hitungan=0;
       else hitungan +=1;
     }

//     total=22;
//     play();
   }
   ES=1;
}
void mainkan()
{
   isd_a0=0;
   isd_ce=0;
   isd_ce=1;
   while (isd_eom==1)
   ;
   tunda(13);
   isd_pd=1;
}

void start_skip()
```

```
{
  isd_pd=0;
  tunda(25);
  isd_a0=1;
}
void play()
{
  unsigned char z;
  puluhan=total / 10;
  satuan=total % 10;
  start_skip();

  if (puluhan==0) go();

  else  if (puluhan==1)
  {
    if (satuan==0)
     {
       for (z=0;z<10;z++)
       {
        isd_ce=0;
        isd_ce=1;
        while (isd_eom) ;
        tunda(13);
        }
        mainkan();
    } //end satuan=0

    else if (satuan==1)
    {
       for (z=0;z<11;z++)
       {
       isd_ce=0;
       isd_ce=1;
       while (isd_eom) ;
       tunda(13);
       }
       mainkan();
    } //end satuan=1

    else
    {
       for (z=0;z<satuan;z++)
       {
       isd_ce=0;
       isd_ce=1;
       while (isd_eom) ;
       tunda(13);
       }
       mainkan();
       tunda(50);
       start_skip();

       for (z=0;z<12;z++)
       {
       isd_ce=0;
       isd_ce=1;
       while (isd_eom) ;
       tunda(13);
       }
       mainkan();
    }
  } //end puluhan=1

  else
  {
     if (satuan==0)
```

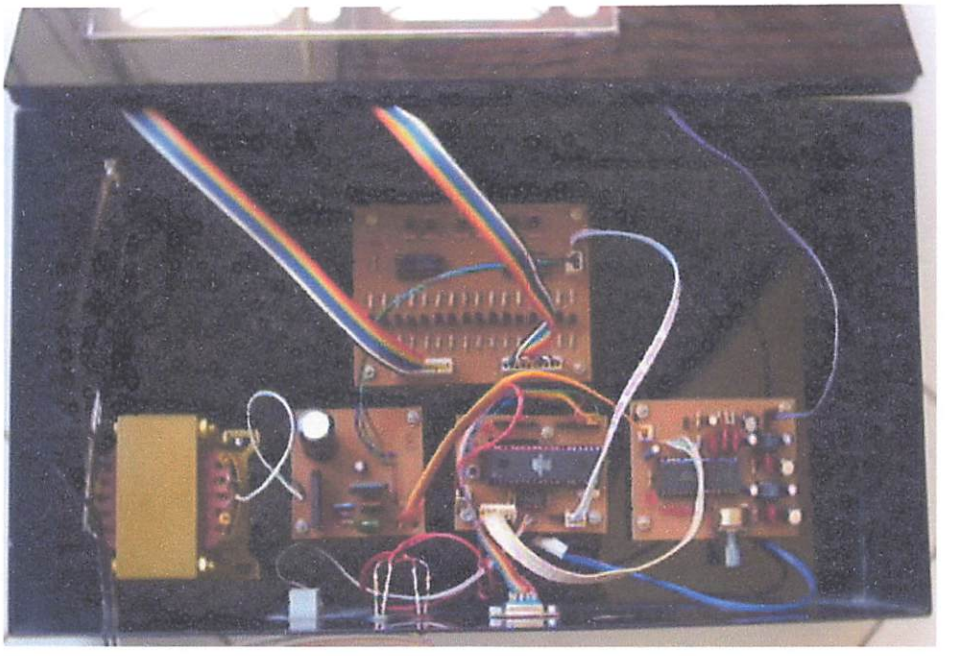
```
    {
       for (z=0;z<puluhan;z++)
       {
       isd_ce=0;
       isd_ce=1;
       while (isd_eom) ;
       tunda(13);
       }
       mainkan();
       tunda(50);
       start_skip();

       for (z=0;z<13;z++)
       {
       isd_ce=0;
       isd_ce=1;
       while (isd_eom) ;
       tunda(13);
       }
       mainkan();
    }
    else
    {
       for (z=0;z<puluhan;z++)
       {
       isd_ce=0;
       isd_ce=1;
       while (isd_eom) ;
       tunda(13);
       }
       mainkan();
       tunda(50);
       start_skip();

       for (z=0;z<13;z++)
       {
       isd_ce=0;
       isd_ce=1;
       while (isd_eom) ;
       tunda(13);
       }
       mainkan();
       tunda(50);
       start_skip();

       for (z=0;z<satuan;z++)
       {
       isd_ce=0;
       isd_ce=1;
       while (isd_eom) ;
       tunda(13);
       }
       mainkan();
    }

  } //end else
  hitungan=nilai=total=0;
}// end fungsi

void tampil()
{
   led=1;
   total+=nilai;
   if (hitungan <= 5)
   {
     ss_buffer[0]=nilai / 10;
     ss_buffer[1]=nilai % 10;
```

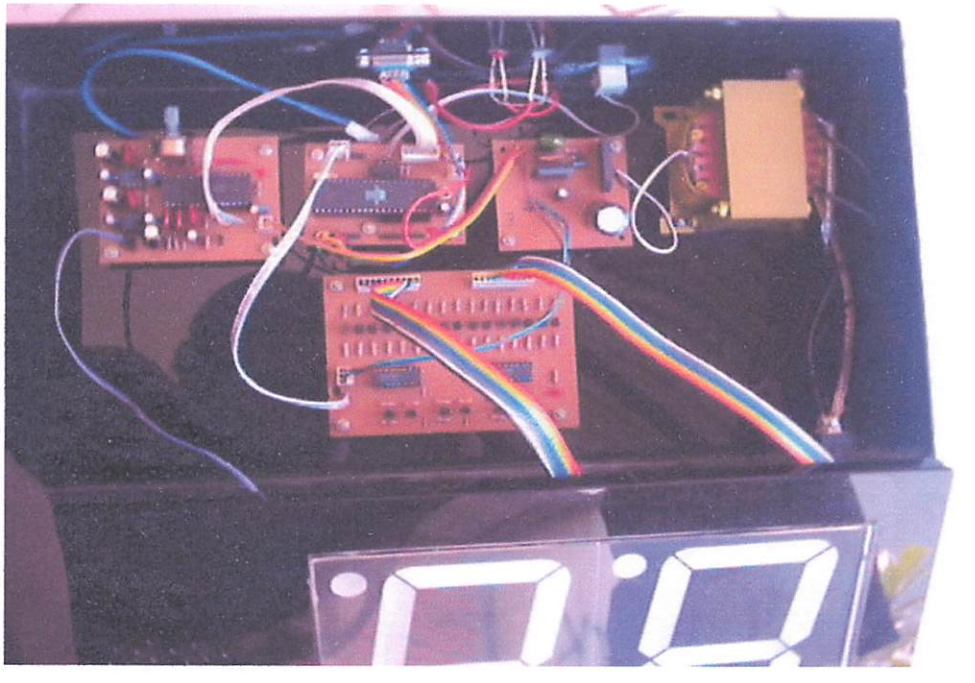
```
      update_display();
    }

    else
    {
      ss_buffer[0]=nilai / 10;
      ss_buffer[1]=nilai % 10;
      update_display();
      tunda(3000);
      ss_buffer[0]=total / 10;
      ss_buffer[1]=total % 10;
      update_display();
      status=0;
    }
}

void go()
{
  unsigned char lup;
  isd_pd=0;
  tunda(25);
  isd_a0=1;
  for (lup=0;lup<nilai;lup++)
  {
     isd_ce=0;
     isd_ce=1;
     while (isd_eom) ;
     tunda(13);
  }
  isd_a0=0;
  isd_ce=0;
  isd_ce=1;
  while (isd_eom) ;
  tunda(13);
  isd_pd=1;
}

void main()
{

     P2=0;
     isd_a0=0;
     isd_pr=isd_pd=isd_eom=isd_ce=isd_ovf=1;

     P1_6=0;             //Disable Transmit
     P1_7=0;             //Enable Receive

     nilai=total=hitungan=0;
     stb=clk=dat=0;
     led=led_s=1;

     init_intser();
     Init_Serial(0xfd);    // inisialisasi port serial

     ss_buffer[0]=0;
     ss_buffer[1]=0;
     update_display();
     tunda(1000);

     while(1)
     {
        while(status)
        {
           if ((P2==0x10) || (P2==0x18))
           {
             tunda(10);
             led=0;
```

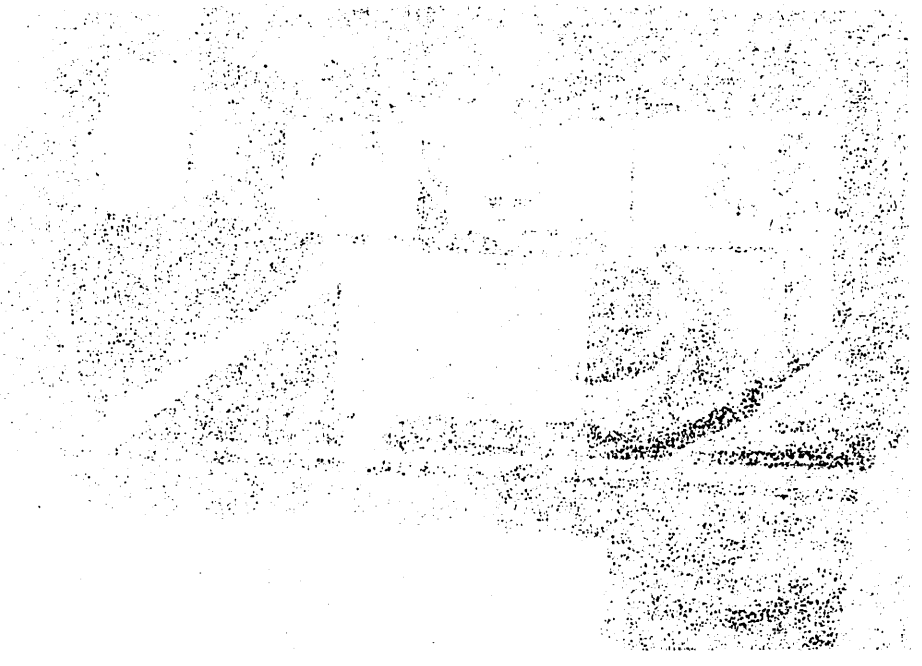
```
  led_s=1;
  while ((P2==0x10) || (P2==0x18));
  tunda(2000);
  nilai=9;
  tampil();
  go();
  status=0;
  if (hitungan == 6)
  {
    tunda(2000);
    play();
  }
}

else if ((P2==0x08) || (P2==0x0c))
{
  tunda(10);
  led=0;
  led_s=1;
  while ((P2==0x08) || (P2==0x0c));
  tunda(2000);
  nilai=7;
  tampil();
  go();
  status=0;
  if (hitungan == 6)
  {
    tunda(2000);
    play();
  }
}

else if ((P2==0x04) || (P2==0x06))
{
  tunda(10);
  led=0;
  led_s=1;
  while ((P2==0x04) || (P2==0x06));
  tunda(2000);
  nilai=5;
  tampil();
  go();
  status=0;
  if (hitungan == 6)
  {
    tunda(2000);
    play();
  }
}

else if ((P2==0x02) || (P2==0x03))
{
  tunda(10);
  led=0;
  led_s=1;
  while ((P2==0x02) || (P2==0x03));
  tunda(2000);
  nilai=3;
  tampil();
  go();
  status=0;
  if (hitungan == 6)
  {
    tunda(2000);
    play();
  }
}
```

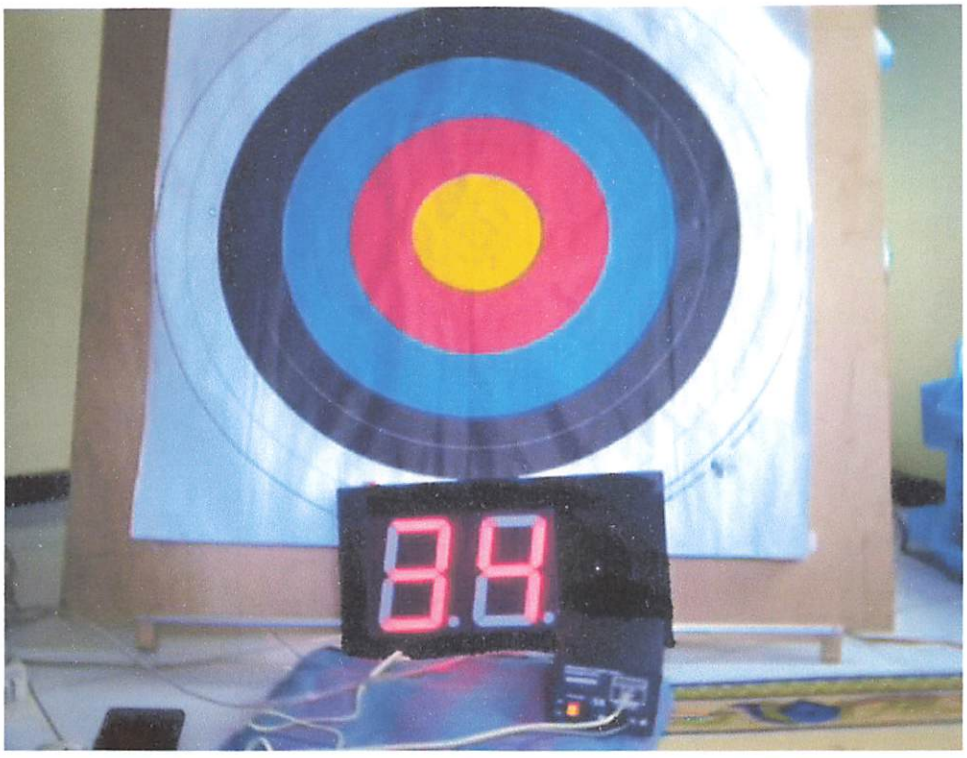
```
            else if (P2==0x01)
            {
              tunda(10);
              led=0;
              led_s=1;
              while (P2==0x01);
              tunda(2000);
              nilai=1;
              tampil();
              go();
              status=0;
              if (hitungan == 6)
              {
                tunda(2000);
                play();
              }
            }
          } // end status
      }
}
```

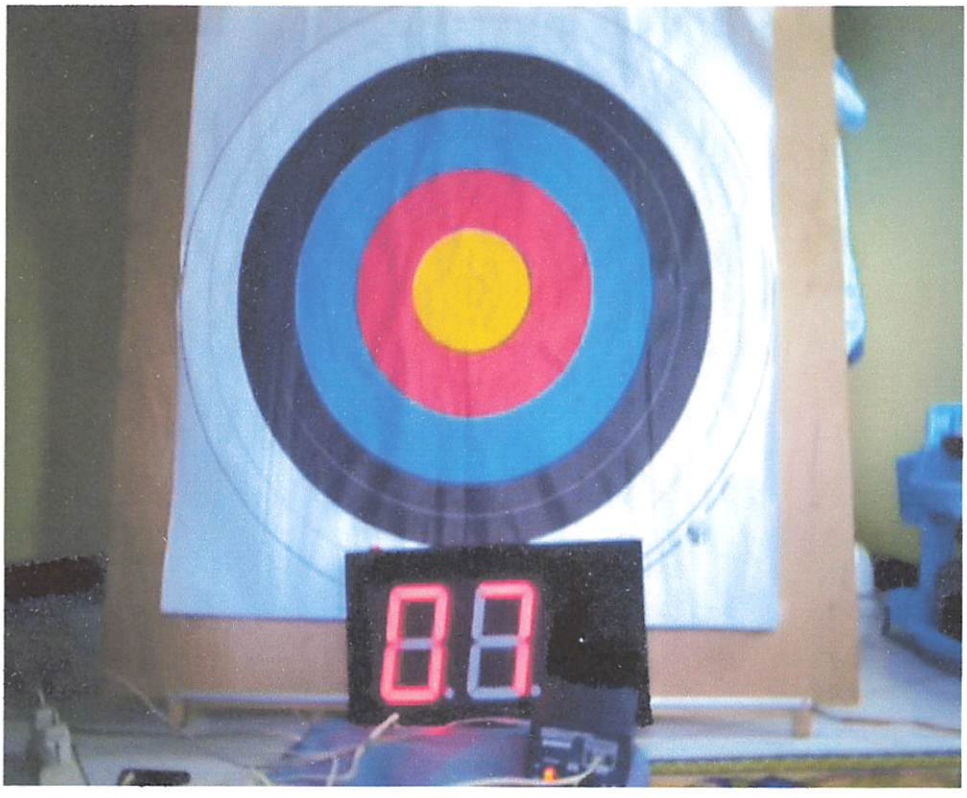
Foto Alat








8.8.


8.8.

Features

- Compatible with MCS-51™ Products
- 8K Bytes of In-System Reprogrammable Downloadable Flash Memory
  - SPI Serial Interface for Program Downloading
  - Endurance: 1,000 Write/Erase Cycles
- 2K Bytes EEPROM
  - Endurance: 100,000 Write/Erase Cycles
- 4.0V to 6V Operating Range
- Fully Static Operation: 0 Hz to 24 MHz
- Three-Level Program Memory Lock
- 256 x 8-bit Internal RAM
- 32 Programmable I/O Lines
- Three 16-bit Timer/Counters
- Nine Interrupt Sources
- Programmable UART Serial Channel
- SPI Serial Interface
- Low Power Idle and Power Down Modes
- Interrupt Recovery From Power Down
- Programmable Watchdog Timer
- Dual Data Pointer
- Power Off Flag

Description

The AT89S8252 is a low-power, high-performance CMOS 8-bit microcomputer with 8K bytes of Downloadable Flash programmable and erasable read only memory and 2K bytes of EEPROM. The device is manufactured using Atmel's high density nonvolatile memory technology and is compatible with the industry standard 80C51 instruction set and pinout. The on-chip Downloadable Flash allows the program memory to be reprogrammed in-system through an SPI serial interface or by a conventional nonvolatile memory programmer. By combining a versatile 8-bit CPU with Downloadable Flash on a monolithic chip, the Atmel AT89S8252 is a powerful microcomputer which provides a highly flexible and cost effective solution to many embedded control applications.

The AT89S8252 provides the following standard features: 8K bytes of Downloadable Flash, 2K bytes of EEPROM, 256 bytes of RAM, 32 I/O lines, programmable watchdog timer, two Data Pointers, three 16-bit timer/counters, a six-vector two-level interrupt architecture, a full duplex serial port, on-chip oscillator, and clock circuitry. In addition, the AT89S8252 is designed with static logic for operation down to zero frequency and supports two software selectable power saving modes. The Idle Mode stops the CPU while allowing the RAM, timer/counters, serial port, and interrupt system to continue functioning. The Power Down Mode saves the RAM contents but freezes the oscillator, disabling all other chip functions until the next interrupt or hardware reset.

The Downloadable Flash can be changed a single byte at a time and is accessible through the SPI serial interface. Holding RESET active forces the SPI bus into a serial programming interface and allows the program memory to be written to or read from unless Lock Bit 2 has been activated.

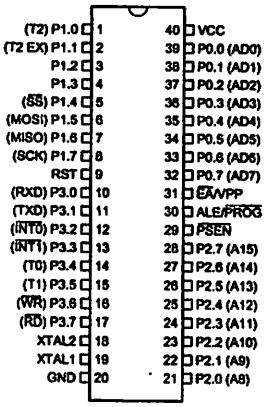
8-Bit Microcontroller with 8K Bytes Flash

AT89S8252

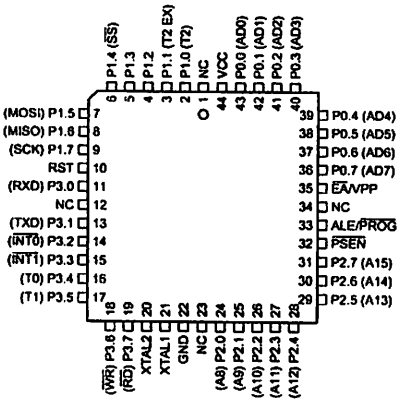
0401D-A-12/97

Pin Configurations

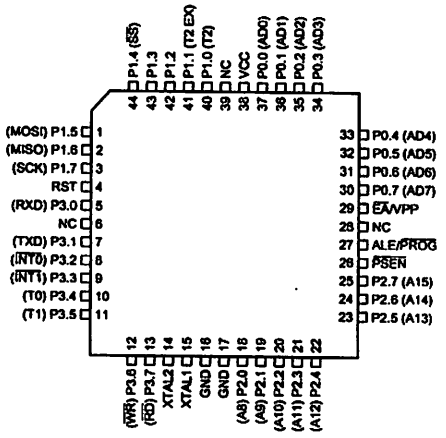
PDIP



PLCC



PQFP/TQFP



Pin Description

V_{CC}
Supply voltage.

GND
Ground.

Port 0
Port 0 is an 8-bit open drain bidirectional I/O port. As an output port, each pin can sink eight TTL inputs. When 1s are written to port 0 pins, the pins can be used as high-impedance inputs.

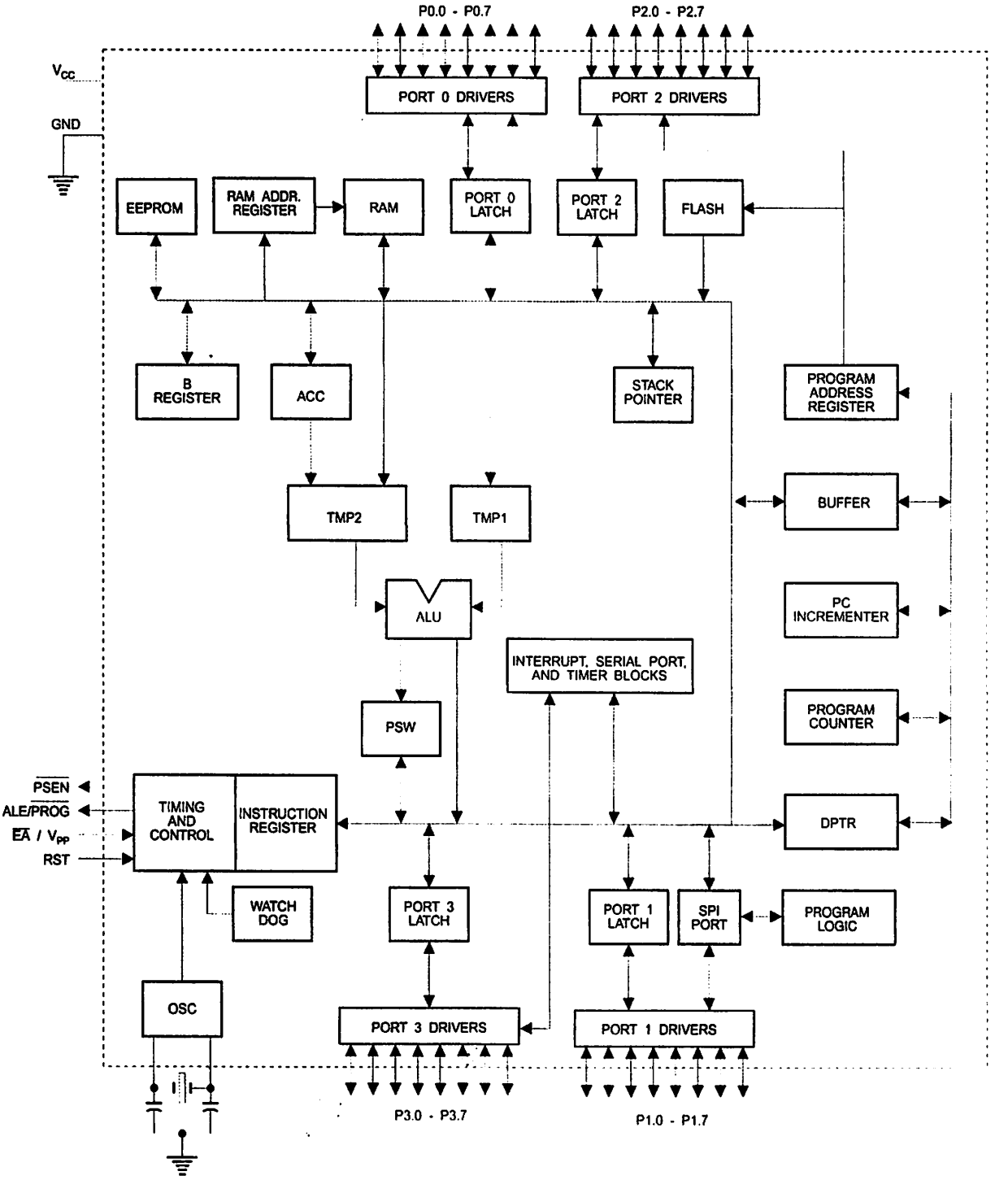
Port 0 can also be configured to be the multiplexed low-order address/data bus during accesses to external program and data memory. In this mode, P0 has internal pullups.

Port 0 also receives the code bytes during Flash programming and outputs the code bytes during program verification. External pullups are required during program verification.

Port 1
Port 1 is an 8-bit bidirectional I/O port with internal pullups. The Port 1 output buffers can sink/source four TTL inputs. When 1s are written to Port 1 pins, they are pulled high by the internal pullups and can be used as inputs. As inputs, Port 1 pins that are externally being pulled low will source current (I_{IL}) because of the internal pullups.

Some Port 1 pins provide additional functions. P1.0 and P1.1 can be configured to be the timer/counter 2 external count input (P1.0/T2) and the timer/counter 2 trigger input (P1.1/T2EX), respectively.

Block Diagram



Furthermore, P1.4, P1.5, P1.6, and P1.7 can be configured as the SPI slave port select, data input/output and shift clock input/output pins as shown in the following table.

Port Pin	Alternate Functions
P1.0	T2 (external count input to Timer/Counter 2), clock-out
P1.1	T2EX (Timer/Counter 2 capture/reload trigger and direction control)
P1.4	$\overline{SS}$ (Slave port select input)
P1.5	MOSI (Master data output, slave data input pin for SPI channel)
P1.6	MISO (Master data input, slave data output pin for SPI channel)
P1.7	SCK (Master clock output, slave clock input pin for SPI channel)

Port 1 also receives the low-order address bytes during Flash programming and verification.

Port 2

Port 2 is an 8-bit bidirectional I/O port with internal pullups. The Port 2 output buffers can sink/source four TTL inputs. When 1s are written to Port 2 pins, they are pulled high by the internal pullups and can be used as inputs. As inputs, Port 2 pins that are externally being pulled low will source current (I_{IL}) because of the internal pullups.

Port 2 emits the high-order address byte during fetches from external program memory and during accesses to external data memory that use 16-bit addresses (MOVX @ DPTR). In this application, Port 2 uses strong internal pullups when emitting 1s. During accesses to external data memory that use 8-bit addresses (MOVX @ RI), Port 2 emits the contents of the P2 Special Function Register.

Port 2 also receives the high-order address bits and some control signals during Flash programming and verification.

Port 3

Port 3 is an 8 bit bidirectional I/O port with internal pullups. The Port 3 output buffers can sink/source four TTL inputs. When 1s are written to Port 3 pins, they are pulled high by the internal pullups and can be used as inputs. As inputs, Port 3 pins that are externally being pulled low will source current (I_{IL}) because of the pullups.

Port 3 also serves the functions of various special features of the AT89S8252, as shown in the following table.

Port 3 also receives some control signals for Flash programming and verification.

Port Pin	Alternate Functions
P3.0	RXD (serial input port)
P3.1	TXD (serial output port)
P3.2	$\overline{INT0}$ (external interrupt 0)
P3.3	$\overline{INT1}$ (external interrupt 1)
P3.4	T0 (timer 0 external input)
P3.5	T1 (timer 1 external input)
P3.6	$\overline{WR}$ (external data memory write strobe)
P3.7	$\overline{RD}$ (external data memory read strobe)

RST

Reset input. A high on this pin for two machine cycles while the oscillator is running resets the device.

ALE/$\overline{PROG}$

Address Latch Enable is an output pulse for latching the low byte of the address during accesses to external memory. This pin is also the program pulse input ($\overline{PROG}$) during Flash programming.

In normal operation, ALE is emitted at a constant rate of 1/6 the oscillator frequency and may be used for external timing or clocking purposes. Note, however, that one ALE pulse is skipped during each access to external data memory.

If desired, ALE operation can be disabled by setting bit 0 of SFR location 8EH. With the bit set, ALE is active only during a MOVX or MOVC instruction. Otherwise, the pin is weakly pulled high. Setting the ALE-disable bit has no effect if the microcontroller is in external execution mode.

$\overline{PSEN}$

Program Store Enable is the read strobe to external program memory.

When the AT89S8252 is executing code from external program memory, $\overline{PSEN}$ is activated twice each machine cycle, except that two $\overline{PSEN}$ activations are skipped during each access to external data memory.

$\overline{EA}$/V_{PP}

External Access Enable. $\overline{EA}$ must be strapped to GND in order to enable the device to fetch code from external program memory locations starting at 0000H up to FFFFH. Note, however, that if lock bit 1 is programmed, $\overline{EA}$ will be internally latched on reset.

$\overline{EA}$ should be strapped to V_{CC} for internal program executions. This pin also receives the 12-volt programming enable voltage (V_{PP}) during Flash programming when 12-volt programming is selected.

XTAL1
Input to the inverting oscillator amplifier and input to the internal clock operating circuit.

XTAL2
Output from the inverting oscillator amplifier.

Special Function Registers

A map of the on-chip memory area called the Special Function Register (SFR) space is shown in Table 1.

Note that not all of the addresses are occupied, and unoccupied addresses may not be implemented on the chip. Read accesses to these addresses will in general return random data, and write accesses will have an indeterminate effect.

Table 1. AT89S8252 SFR Map and Reset Values

0F8H									0FFH
0F0H	B 00000000								0F7H
0E8H									0EFH
0E0H	ACC 00000000								0E7H
0D8H									0DFH
0D0H	PSW 00000000					SPCR 000001XX			0D7H
0C8H	T2CON 00000000	T2MOD XXXXXX00	RCAP2L 00000000	RCAP2H 00000000	TL2 00000000	TH2 00000000			0CFH
0C0H									0C7H
0B8H	IP XX000000								0BFH
0B0H	P3 11111111								0B7H
0A8H	IE 0X000000		SPSR 00XXXXXX						0AFH
0A0H	P2 11111111								0A7H
98H	SCON 00000000	SBUF XXXXXXXX							9FH
90H	P1 11111111						WMCON 00000010		97H
88H	TCON 00000000	TMOD 00000000	TL0 00000000	TL1 00000000	TH0 00000000	TH1 00000000			8FH
80H	P0 11111111	SP 00000111	DP0L 00000000	DP0H 00000000	DP1L 00000000	DP1H 00000000	SPDR XXXXXXXX	PCON 0XXX0000	87H

User software should not write 1s to these unlisted locations, since they may be used in future products to invoke new features. In that case, the reset or inactive values of the new bits will always be 0.

Timer 2 Registers Control and status bits are contained in registers T2CON (shown in Table 2) and T2MOD (shown in Table 9) for Timer 2. The register pair (RCAP2H, RCAP2L) are the Capture/Reload registers for Timer 2 in 16 bit capture mode or 16-bit auto-reload mode.

Watchdog and Memory Control Register The WMCON register contains control bits for the Watchdog Timer (shown in Table 3). The EEMEN and EEMWE bits are used to select the 2K bytes on-chip EEPROM, and to enable byte-write. The DPS bit selects one of two DPTR registers available.

SPI Registers Control and status bits for the Serial Peripheral Interface are contained in registers SPCR (shown in Table 4) and SPSR (shown in Table 5). The SPI data bits are contained in the SPDR register. Writing the SPI data register during serial data transfer sets the Write Collision bit, WCOL, in the SPSR register. The SPDR is double buffered for writing and the values in SPDR are not changed by Reset.

Interrupt Registers The global interrupt enable bit and the individual interrupt enable bits are in the IE register. In addition, the individual interrupt enable bit for the SPI is in the SPCR register. Two priorities can be set for each of the six interrupt sources in the IP register.

Table 2. T2CON—Timer/Counter 2 Control Register

T2CON Address = 0C8H — Reset Value = 0000 0000B

Bit Addressable

	TF2	EXF2	RCLK	TCLK	EXEN2	TR2	C/$\overline{T2}$	CP/$\overline{RL2}$
Bit	7	6	5	4	3	2	1	0

Symbol	Function
TF2	Timer 2 overflow flag set by a Timer 2 overflow and must be cleared by software. TF2 will not be set when either RCLK = 1 or TCLK = 1.
EXF2	Timer 2 external flag set when either a capture or reload is caused by a negative transition on T2EX and EXEN2 = 1. When Timer 2 interrupt is enabled, EXF2 = 1 will cause the CPU to vector to the Timer 2 interrupt routine. EXF2 must be cleared by software. EXF2 does not cause an interrupt in up/down counter mode (DCEN = 1).
RCLK	Receive clock enable. When set, causes the serial port to use Timer 2 overflow pulses for its receive clock in serial port Modes 1 and 3. RCLK = 0 causes Timer 1 overflows to be used for the receive clock.
TCLK	Transmit clock enable. When set, causes the serial port to use Timer 2 overflow pulses for its transmit clock in serial port Modes 1 and 3. TCLK = 0 causes Timer 1 overflows to be used for the transmit clock.
EXEN2	Timer 2 external enable. When set, allows a capture or reload to occur as a result of a negative transition on T2EX if Timer 2 is not being used to clock the serial port. EXEN2 = 0 causes Timer 2 to ignore events at T2EX.
TR2	Start/Stop control for Timer 2. TR2 = 1 starts the timer.
C/$\overline{T2}$	Timer or counter select for Timer 2. C/$\overline{T2}$ = 0 for timer function. C/$\overline{T2}$ = 1 for external event counter (falling edge triggered).
CP/$\overline{RL2}$	Capture/Reload select. CP/$\overline{RL2}$ = 1 causes captures to occur on negative transitions at T2EX if EXEN2 = 1. CP/$\overline{RL2}$ = 0 causes automatic reloads to occur when Timer 2 overflows or negative transitions occur at T2EX when EXEN2 = 1. When either RCLK or TCLK = 1, this bit is ignored and the timer is forced to auto-reload on Timer 2 overflow.

Dual Data Pointer Registers To facilitate accessing both internal EEPROM and external data memory, two banks of 16 bit Data Pointer Registers are provided: DP0 at SFR address locations 82H-83H and DP1 at 84H-85H. Bit DPS = 0 in SFR WMCON selects DP0 and DPS = 1 selects DP1. The user should always initialize the DPS bit to the appropriate value before accessing the respective Data Pointer Register.

Power Off Flag The Power Off Flag (POF) is located at bit_4 (PCON.4) in the PCON SFR. POF is set to "1" during power up. It can be set and reset under software control and is not affected by RESET.

Table 3. WMCON—Watchdog and Memory Control Register

WMCON Address = 96H — Reset Value = 0000 0010B

Bit	PS2	PS1	PS0	EEMWE	EEMEN	DPS	WDTRST	WDTEN
	7	6	5	4	3	2	1	0

Symbol	Function
PS2 PS1 PS0	Prescaler Bits for the Watchdog Timer. When all three bits are set to "0", the watchdog timer has a nominal period of 16 ms. When all three bits are set to "1", the nominal period is 2048 ms.
EEMWE	EEPROM Data Memory Write Enable Bit. Set this bit to "1" before initiating byte write to on-chip EEPROM with the MOVX instruction. User software should set this bit to "0" after EEPROM write is completed.
EEMEN	Internal EEPROM Access Enable. When EEMEN = 1, the MOVX instruction with DPTR will access on-chip EEPROM instead of external data memory. When EEMEN = 0, MOVX with DPTR accesses external data memory.
DPS	Data Pointer Register Select. DPS = 0 selects the first bank of Data Pointer Register, DP0, and DPS = 1 selects the second bank, DP1
WDTRST RDY/$\overline{BSY}$	Watchdog Timer Reset and EEPROM Ready/$\overline{Busy}$ Flag. Each time this bit is set to "1" by user software, a pulse is generated to reset the watchdog timer. The WDTRST bit is then automatically reset to "0" in the next instruction cycle. The WDTRST bit is Write-Only. This bit also serves as the RDY/$\overline{BSY}$ flag in a Read-Only mode during EEPROM write. RDY/$\overline{BSY}$ = 1 means that the EEPROM is ready to be programmed. While programming operations are being executed, the RDY/$\overline{BSY}$ bit equals "0" and is automatically reset to "1" when programming is completed.
WDTEN	Watchdog Timer Enable Bit. WDTEN = 1 enables the watchdog timer and WDTEN = 0 disables the watchdog timer.

Table 4. SPCR—SPI Control Register

SPCR Address = D5H — Reset Value = 0000 01XXB

Bit	SPIE	SPE	DORD	MSTR	CPOL	CPHA	SPR1	SPR0
	7	6	5	4	3	2	1	0

Symbol	Function
SPIE	SPI Interrupt Enable. This bit, in conjunction with the ES bit in the IE register, enables SPI interrupts: SPIE = 1 and ES = 1 enable SPI interrupts. SPIE = 0 disables SPI interrupts.
SPE	SPI Enable. SPI = 1 enables the SPI channel and connects $\overline{SS}$, MOSI, MISO and SCK to pins P1.4, P1.5, P1.6, and P1.7. SPI = 0 disables the SPI channel.
DORD	Data Order. DORD = 1 selects LSB first data transmission. DORD = 0 selects MSB first data transmission.
MSTR	Master/Slave Select. MSTR = 1 selects Master SPI mode. MSTR = 0 selects Slave SPI mode.
CPOL	Clock Polarity. When CPOL = 1, SCK is high when idle. When CPOL = 0, SCK of the master device is low when not transmitting. Please refer to figure on SPI Clock Phase and Polarity Control.
CPHA	Clock Phase. The CPHA bit together with the CPOL bit controls the clock and data relationship between master and slave. Please refer to figure on SPI Clock Phase and Polarity Control.
SPR0 SPR1	SPI Clock Rate Select. These two bits control the SCK rate of the device configured as master. SPR1 and SPR0 have no effect on the slave. The relationship between SCK and the oscillator frequency, $F_{osc.}$, is as follows: SPR1 SPR0 SCK = $F_{osc.}$ divided by 0 0 4 0 1 16 1 0 64 1 1 128

Table 5. SPSR—SPI Status Register

SPSR Address = AAH — Reset Value = 00XX XXXXB

Bit	SPIF	WCOL	—	—	—	—	—	—
	7	6	5	4	3	2	1	0

Symbol	Function
SPIF	SPI Interrupt Flag. When a serial transfer is complete, the SPIF bit is set and an interrupt is generated if SPIE = 1 and ES = 1. The SPIF bit is cleared by reading the SPI status register with SPIF and WCOL bits set, and then accessing the SPI data register.
WCOL	Write Collision Flag. The WCOL bit is set if the SPI data register is written during a data transfer. During data transfer, the result of reading the SPDR register may be incorrect, and writing to it has no effect. The WCOL bit (and the SPIF bit) are cleared by reading the SPI status register with SPIF and WCOL set, and then accessing the SPI data register.

Table 6. SPDR—SPI Data Register

SPDR Address = 86H — Reset Value = unchanged

Bit	SPD7	SPD6	SPD5	SPD4	SPD3	SPD2	SPD1	SPD0
	7	6	5	4	3	2	1	0

Data Memory—EEPROM and RAM

The AT89S8252 implements 2K bytes of on-chip EEPROM for data storage and 256 bytes of RAM. The upper 128 bytes of RAM occupy a parallel space to the Special Function Registers. That means the upper 128 bytes have the same addresses as the SFR space but are physically separate from SFR space.

When an instruction accesses an internal location above address 7FH, the address mode used in the instruction specifies whether the CPU accesses the upper 128 bytes of RAM or the SFR space. Instructions that use direct addressing access SFR space.

For example, the following direct addressing instruction accesses the SFR at location 0A0H (which is P2).

```
MOV 0A0H, #data
```

Instructions that use indirect addressing access the upper 128 bytes of RAM. For example, the following indirect addressing instruction, where R0 contains 0A0H, accesses the data byte at address 0A0H, rather than P2 (whose address is 0A0H).

```
MOV @R0, #data
```

Note that stack operations are examples of indirect addressing, so the upper 128 bytes of data RAM are available as stack space.

The on-chip EEPROM data memory is selected by setting the EEMEN bit in the WMCON register at SFR address location 96H. The EEPROM address range is from 000H to 7FFH. The MOVX instructions are used to access the EEPROM. To access off-chip data memory with the MOVX instructions, the EEMEN bit needs to be set to "0".

The EEMWE bit in the WMCON register needs to be set to "1" before any byte location in the EEPROM can be written. User software should reset EEMWE bit to "0" if no further EEPROM write is required. EEPROM write cycles in the serial programming mode are self-timed and typically take 2.5 ms. The progress of EEPROM write can be monitored by reading the RDY/$\overline{BSY}$ bit (read-only) in SFR WMCON. RDY/$\overline{BSY}$ = 0 means programming is still in progress and RDY/$\overline{BSY}$ = 1 means EEPROM write cycle is completed and another write cycle can be initiated.

In addition, during EEPROM programming, an attempted read from the EEPROM will fetch the byte being written with the MSB complemented. Once the write cycle is completed, true data are valid at all bit locations.

Programmable Watchdog Timer

The programmable Watchdog Timer (WDT) operates from an independent oscillator. The prescaler bits, PS0, PS1 and PS2 in SFR WMCON are used to set the period of the Watchdog Timer from 16 ms to 2048 ms. The available timer periods are shown in the following table and the actual timer periods (at V_{CC} = 5V) are within ±30% of the nominal.

The WDT is disabled by Power-on Reset and during Power Down. It is enabled by setting the WDTEN bit in SFR WMCON (address = 96H). The WDT is reset by setting the WDTRST bit in WMCON. When the WDT times out without being reset or disabled, an internal RST pulse is generated to reset the CPU.

Table 7. Watchdog Timer Period Selection

WDT Prescaler Bits			Period (nominal)
PS2	PS1	PS0	
0	0	0	16 ms
0	0	1	32 ms
0	1	0	64 ms
0	1	1	128 ms
1	0	0	256 ms
1	0	1	512 ms
1	1	0	1024 ms
1	1	1	2048 ms

Timer 0 and 1

Timer 0 and Timer 1 in the AT89S8252 operate the same way as Timer 0 and Timer 1 in the AT89C51, AT89C52 and AT89C55. For further information, see the October 1995 Microcontroller Data Book, page 2-45, section titled, "Timer/Counters."

Timer 2

Timer 2 is a 16 bit Timer/Counter that can operate as either a timer or an event counter. The type of operation is selected by bit C/$\overline{T2}$ in the SFR T2CON (shown in Table 2). Timer 2 has three operating modes: capture, auto-reload (up or down counting), and baud rate generator. The modes are selected by bits in T2CON, as shown in Table 8.

Timer 2 consists of two 8-bit registers, TH2 and TL2. In the Timer function, the TL2 register is incremented every machine cycle. Since a machine cycle consists of 12 oscillator periods, the count rate is 1/12 of the oscillator frequency.

In the Counter function, the register is incremented in response to a 1-to-0 transition at its corresponding external input pin, T2. In this function, the external input is sampled during S5P2 of every machine cycle. When the samples show a high in one cycle and a low in the next cycle, the count is incremented. The new count value appears in the register during S3P1 of the cycle following the one in which the transition was detected. Since two machine cycles (24 oscillator periods) are required to recognize a 1-to-0 transition, the maximum count rate is 1/24 of the oscillator frequency. To ensure that a given level is sampled at least once before it changes, the level should be held for at least one full machine cycle.

Table 8. Timer 2 Operating Modes

RCLK + TCLK	CP/$\overline{RL2}$	TR2	MODE
0	0	1	16-bit Auto-Reload
0	1	1	16-bit Capture
1	X	1	Baud Rate Generator
X	X	0	(Off)

Capture Mode

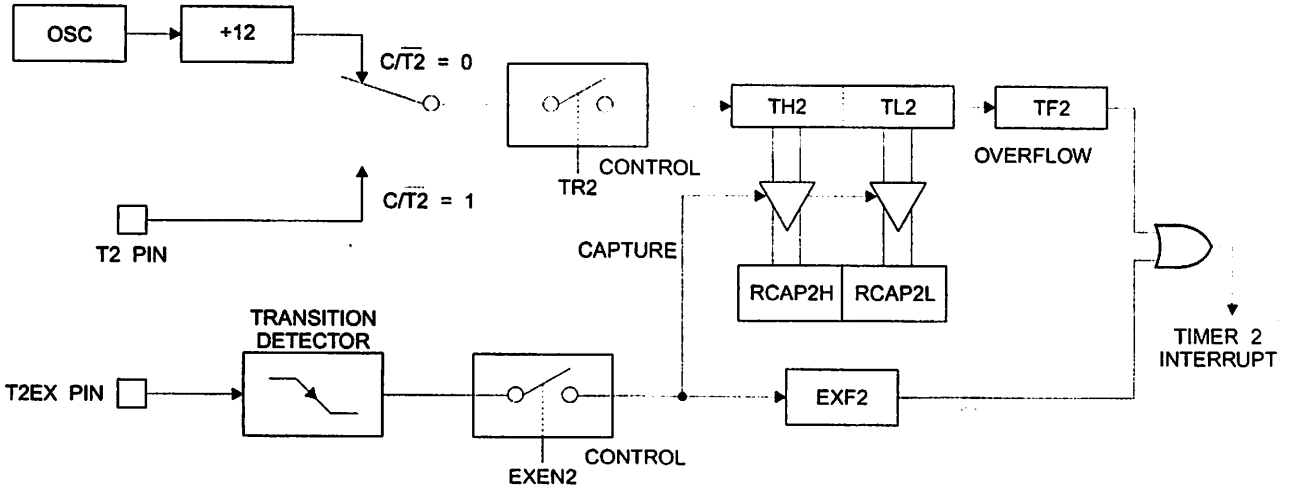
In the capture mode, two options are selected by bit EXEN2 in T2CON. If EXEN2 = 0, Timer 2 is a 16 bit timer or counter which upon overflow sets bit TF2 in T2CON. This bit can then be used to generate an interrupt. If EXEN2 = 1, Timer 2 performs the same operation, but a 1-to-0 transition at external input T2EX also causes the current value in TH2 and TL2 to be captured into RCAP2H and RCAP2L, respectively. In addition, the transition at T2EX causes bit EXF2 in T2CON to be set. The EXF2 bit, like TF2, can generate an interrupt. The capture mode is illustrated in Figure 1.

Auto-Reload (Up or Down Counter)

Timer 2 can be programmed to count up or down when configured in its 16 bit auto-reload mode. This feature is invoked by the DCEN (Down Counter Enable) bit located in the SFR T2MOD (see Table 9). Upon reset, the DCEN bit is set to 0 so that timer 2 will default to count up. When DCEN is set, Timer 2 can count up or down, depending on the value of the T2EX pin.

Figure 2 shows Timer 2 automatically counting up when DCEN = 0. In this mode, two options are selected by bit EXEN2 in T2CON. If EXEN2 = 0, Timer 2 counts up to

Figure 1. Timer 2 in Capture Mode



0FFFFH and then sets the TF2 bit upon overflow. The overflow also causes the timer registers to be reloaded with the 16 bit value in RCAP2H and RCAP2L. The values in RCAP2H and RCAP2L are preset by software. If EXEN2 = 1, a 16 bit reload can be triggered either by an overflow or by a 1-to-0 transition at external input T2EX. This transition also sets the EXF2 bit. Both the TF2 and EXF2 bits can generate an interrupt if enabled.

Setting the DCEN bit enables Timer 2 to count up or down, as shown in Figure 3. In this mode, the T2EX pin controls the direction of the count. A logic 1 at T2EX makes Timer 2 count up. The timer will overflow at 0FFFFH and set the TF2 bit. This overflow also causes the 16 bit value in RCAP2H and RCAP2L to be reloaded into the timer registers, TH2 and TL2, respectively.

A logic 0 at T2EX makes Timer 2 count down. The timer underflows when TH2 and TL2 equal the values stored in RCAP2H and RCAP2L. The underflow sets the TF2 bit and causes 0FFFFH to be reloaded into the timer registers.

The EXF2 bit toggles whenever Timer 2 overflows or underflows and can be used as a 17th bit of resolution. In this operating mode, EXF2 does not flag an interrupt.

Figure 2. Timer 2 in Auto Reload Mode (DCEN = 0)

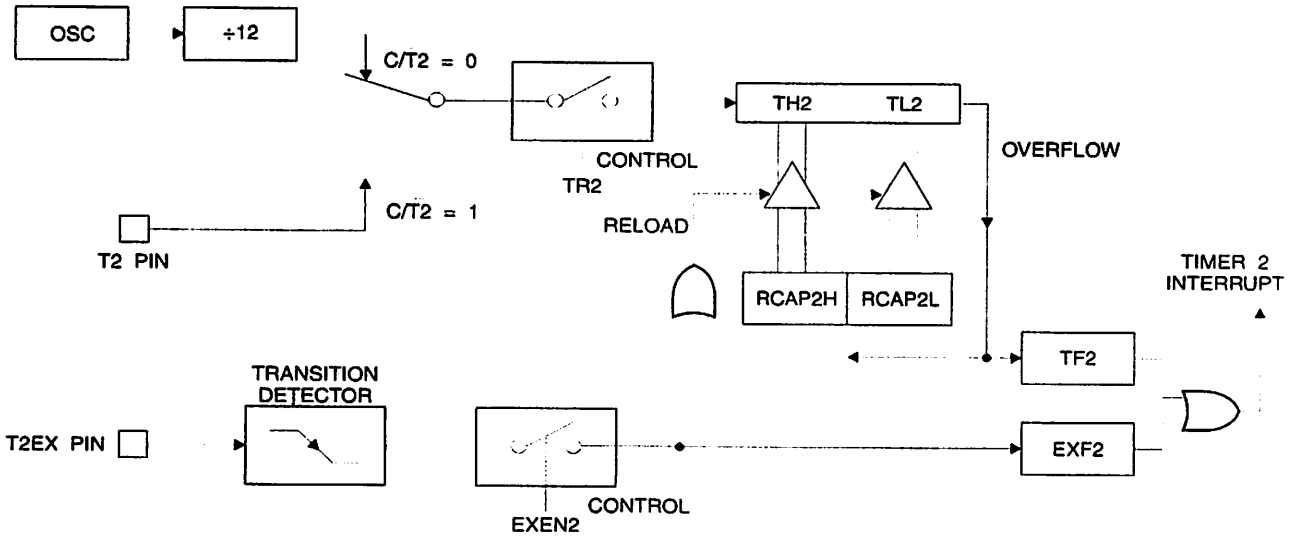


Table 9. T2MOD—Timer 2 Mode Control Register

T2MOD Address = 0C9H — Reset Value = XXXX XX00B

Not Bit Addressable

Bit	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	T2OE	DCEN

Symbol	Function
—	Not implemented, reserved for future use.
T2OE	Timer 2 Output Enable bit.
DCEN	When set, this bit allows Timer 2 to be configured as an up/down counter.

Figure 3. Timer 2 Auto Reload Mode (DCEN = 1)

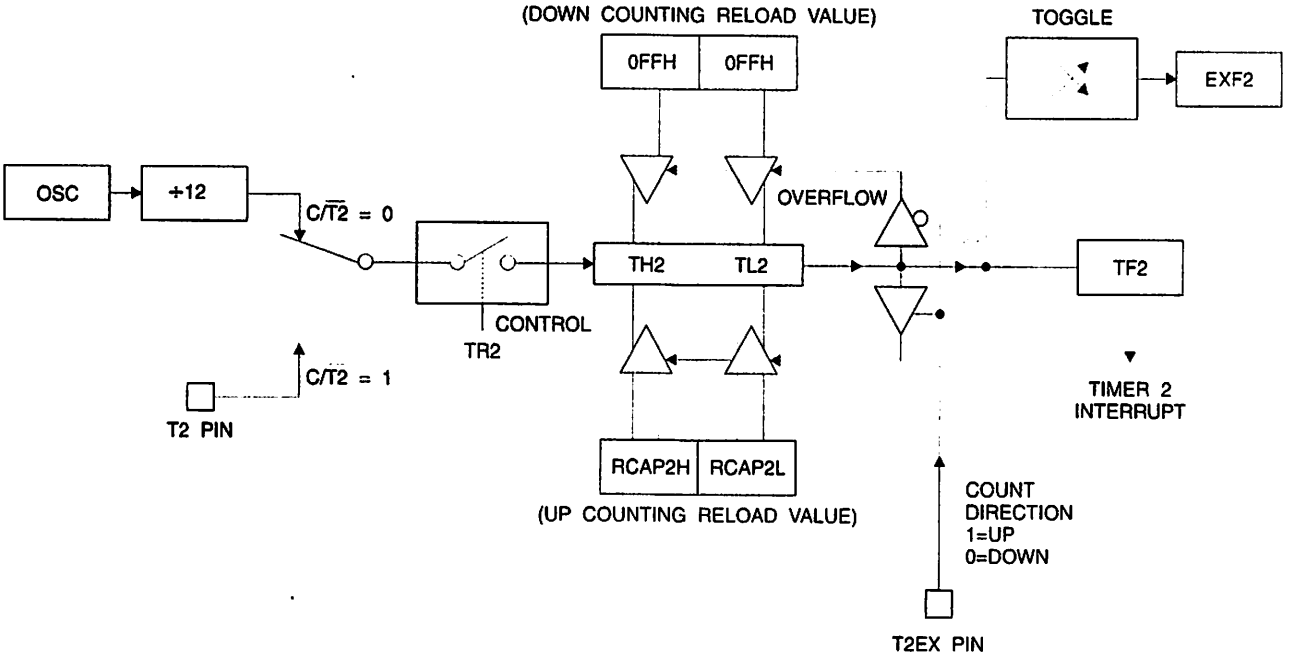
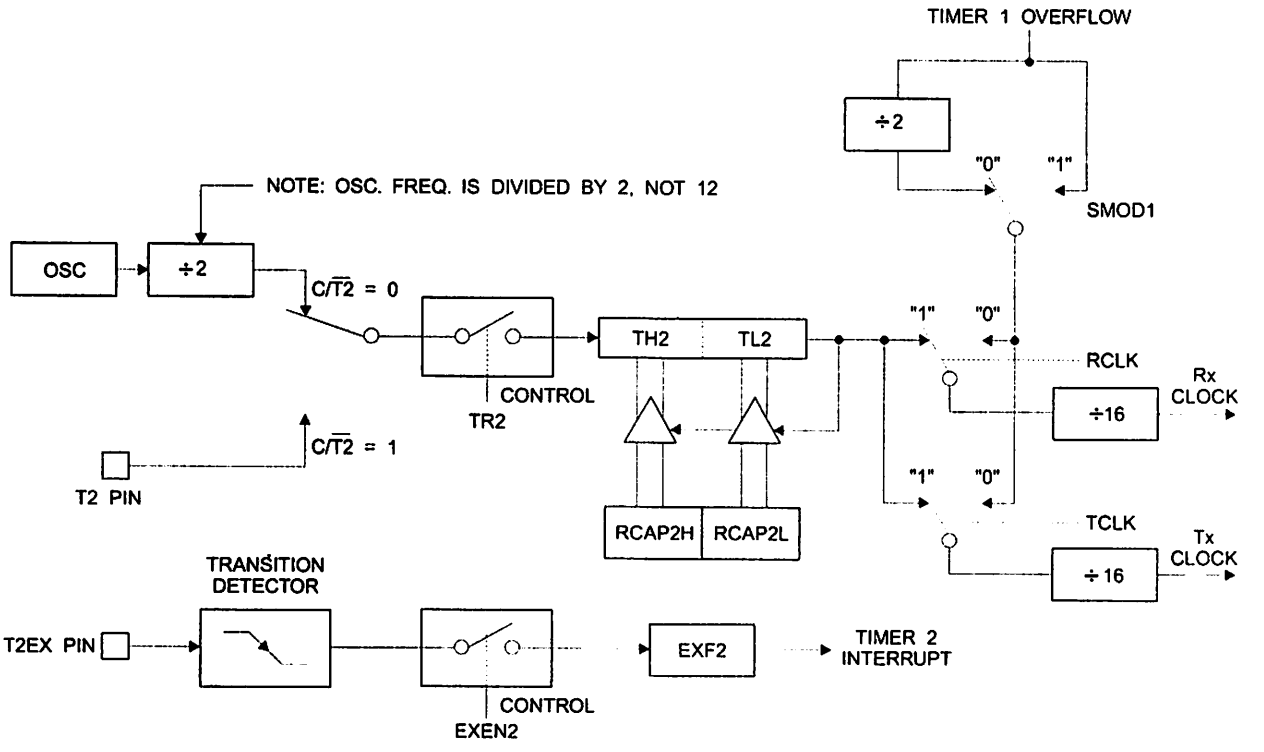


Figure 4. Timer 2 in Baud Rate Generator Mode



Baud Rate Generator

Timer 2 is selected as the baud rate generator by setting TCLK and/or RCLK in T2CON (Table 2). Note that the baud rates for transmit and receive can be different if Timer 2 is used for the receiver or transmitter and Timer 1 is used for the other function. Setting RCLK and/or TCLK puts Timer 2 into its baud rate generator mode, as shown in Figure 4.

The baud rate generator mode is similar to the auto-reload mode, in that a rollover in TH2 causes the Timer 2 registers to be reloaded with the 16 bit value in registers RCAP2H and RCAP2L, which are preset by software.

The baud rates in Modes 1 and 3 are determined by Timer 2's overflow rate according to the following equation.

$$\text{Modes 1 and 3 Baud Rates} = \frac{\text{Timer 2 Overflow Rate}}{16}$$

The Timer can be configured for either timer or counter operation. In most applications, it is configured for timer operation ($C/\overline{T2} = 0$). The timer operation is different for Timer 2 when it is used as a baud rate generator. Normally, as a timer, it increments every machine cycle (at 1/12 the oscillator frequency). As a baud rate generator, however, it increments every state time (at 1/2 the oscillator frequency). The baud rate formula is given below.

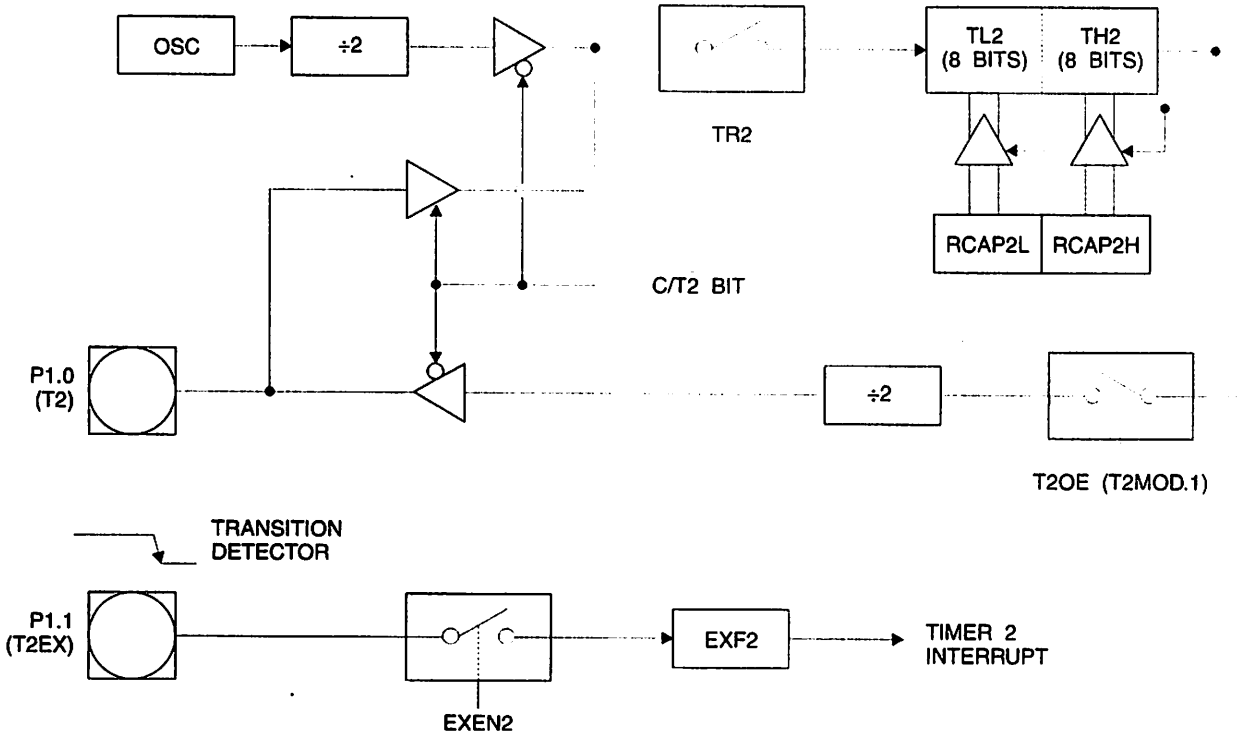
$$\frac{\text{Modes 1 and 3}}{\text{Baud Rate}} = \frac{\text{Oscillator Frequency}}{32 \times [65536 - (\text{RCAP2H,RCAP2L})]}$$

where (RCAP2H, RCAP2L) is the content of RCAP2H and RCAP2L taken as a 16 bit unsigned integer.

Timer 2 as a baud rate generator is shown in Figure 4. This figure is valid only if RCLK or TCLK = 1 in T2CON. Note that a rollover in TH2 does not set TF2 and will not generate an interrupt. Note too, that if EXEN2 is set, a 1-to-0 transition in T2EX will set EXF2 but will not cause a reload from (RCAP2H, RCAP2L) to (TH2, TL2). Thus when Timer 2 is in use as a baud rate generator, T2EX can be used as an extra external interrupt.

Note that when Timer 2 is running (TR2 = 1) as a timer in the baud rate generator mode, TH2 or TL2 should not be read from or written to. Under these conditions, the Timer is incremented every state time, and the results of a read or write may not be accurate. The RCAP2 registers may be read but should not be written to, because a write might overlap a reload and cause write and/or reload errors. The timer should be turned off (clear TR2) before accessing the Timer 2 or RCAP2 registers.

Figure 5. Timer 2 in Clock-Out Mode



Programmable Clock Out

A 50% duty cycle clock can be programmed to come out on P1.0, as shown in Figure 5. This pin, besides being a regular I/O pin, has two alternate functions. It can be programmed to input the external clock for Timer/Counter 2 or to output a 50% duty cycle clock ranging from 61 Hz to 4 MHz at a 16 MHz operating frequency.

To configure the Timer/Counter 2 as a clock generator, bit C/$\overline{T2}$ (T2CON.1) must be cleared and bit T2OE (T2MOD.1) must be set. Bit TR2 (T2CON.2) starts and stops the timer.

The clock-out frequency depends on the oscillator frequency and the reload value of Timer 2 capture registers (RCAP2H, RCAP2L), as shown in the following equation.

$$\text{Clock Out Frequency} = \frac{\text{Oscillator Frequency}}{4 \times (65536 - \text{RCAP2H,RCAP2L})}$$

In the clock-out mode, Timer 2 rollovers will not generate an interrupt. This behavior is similar to when Timer 2 is used as a baud-rate generator. It is possible to use Timer 2 as a baud-rate generator and a clock generator simultaneously. Note, however, that the baud-rate and clock-out frequencies cannot be determined independently from one another since they both use RCAP2H and RCAP2L.

UART

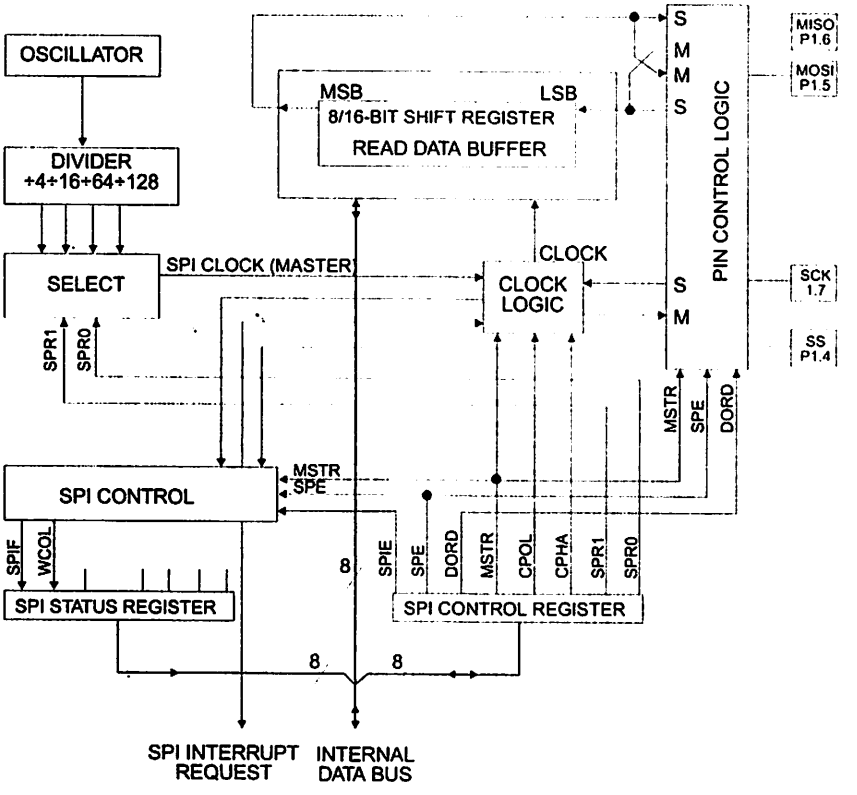
The UART in the AT89S8252 operates the same way as the UART in the AT89C51, AT89C52 and AT89C55. For further information, see the October 1995 Microcontroller Data Book, page 2-49, section titled, "Serial Interface."

Serial Peripheral Interface

The serial peripheral interface (SPI) allows high-speed synchronous data transfer between the AT89S8252 and peripheral devices or between several AT89S8252 devices. The AT89S8252 SPI features include the following:

- Full-Duplex, 3-Wire Synchronous Data Transfer
- Master or Slave Operation
- 1.5-MHz Bit Frequency (max.)
- LSB First or MSB First Data Transfer
- Four Programmable Bit Rates
- End of Transmission Interrupt Flag
- Write Collision Flag Protection
- Wakeup from Idle Mode (Slave Mode Only)

Figure 6. SPI Block Diagram



The interconnection between master and slave CPUs with SPI is shown in the following figure. The SCK pin is the clock output in the master mode but is the clock input in the slave mode. Writing to the SPI data register of the master CPU starts the SPI clock generator, and the data written shifts out of the MOSI pin and into the MOSI pin of the slave CPU. After shifting one byte, the SPI clock generator stops, setting the end of transmission flag (SPIF). If both the SPI interrupt enable bit (SPIE) and the serial port interrupt enable bit (ES) are set, an interrupt is requested.

The Slave Select input, $\overline{SS}$/P1.4, is set low to select an individual SPI device as a slave. When $\overline{SS}$/P1.4 is set high, the SPI port is deactivated and the MOSI/P1.5 pin can be used as an input.

There are four combinations of SCK phase and polarity with respect to serial data, which are determined by control bits CPHA and CPOL. The SPI data transfer formats are shown in Figures 8 and 9.

Figure 7. SPI Master-Slave Interconnection

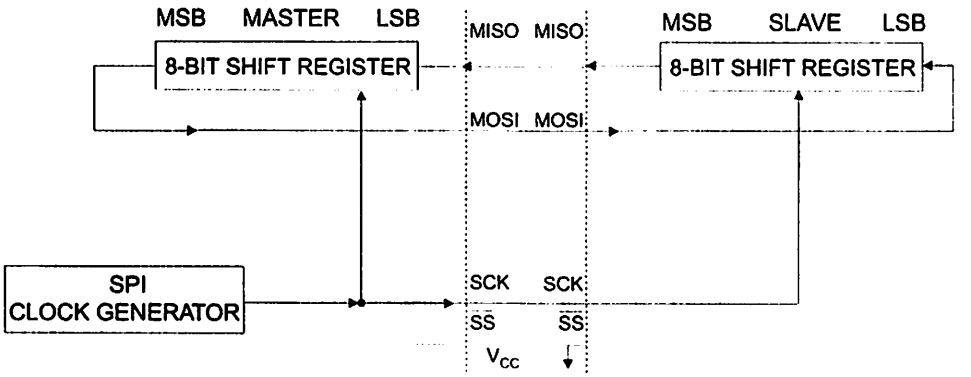
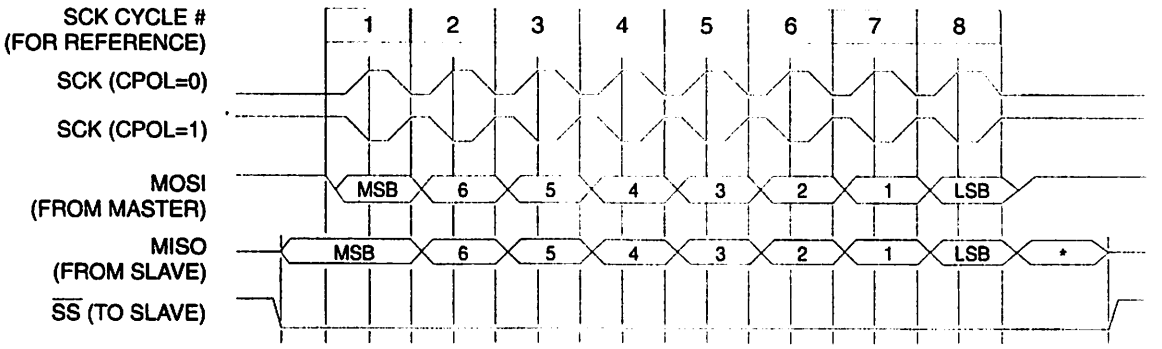
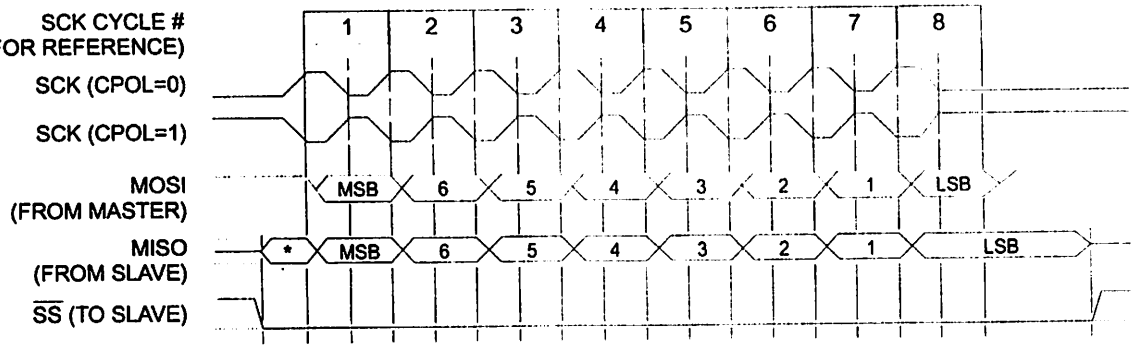


Figure 8. SPI transfer Format with CPHA = 0



*Not defined but normally MSB of character just received

gure 9. SPI Transfer Format with CPHA = 1



Not defined but normally LSB of previously transmitted character

nterrupts

The AT89S8252 has a total of six interrupt vectors: two external interrupts ($\overline{INT0}$ and $\overline{INT1}$), three timer interrupts Timers 0, 1, and 2), and the serial port interrupt. These nterrupts are all shown in Figure 10.

Each of these interrupt sources can be individually enabled r disabled by setting or clearing a bit in Special Function Register IE. IE also contains a global disable bit, EA, which isables all interrupts at once.

Note that Table 10 shows that bit position IE.6 is unimplemented. In the AT89C51, bit position IE.5 is also unimplemented. User software should not write 1s to these bit positions, since they may be used in future AT89 products.

Timer 2 interrupt is generated by the logical OR of bits TF2 and EXF2 in register T2CON. Neither of these flags is cleared by hardware when the service routine is vectored to. In fact, the service routine may have to determine whether it was TF2 or EXF2 that generated the interrupt, and that bit will have to be cleared in software.

The Timer 0 and Timer 1 flags, TF0 and TF1, are set at S5P2 of the cycle in which the timers overflow. The values are then polled by the circuitry in the next cycle. However, the Timer 2 flag, TF2, is set at S2P2 and is polled in the same cycle in which the timer overflows.

Table 10. Interrupt Enable (IE) Register

(MSB) (LSB)

EA	—	ET2	ES	ET1	EX1	ET0	EX0

Enable Bit = 1 enables the interrupt.

Enable Bit = 0 disables the interrupt.

Symbol	Position	Function
EA	IE.7	Disables all interrupts. If EA = 0, no interrupt is acknowledged. If EA = 1, each interrupt source is individually enabled or disabled by setting or clearing its enable bit.
—	IE.6	Reserved.
ET2	IE.5	Timer 2 interrupt enable bit.
ES	IE.4	SPI and UART interrupt enable bit.
ET1	IE.3	Timer 1 interrupt enable bit.
EX1	IE.2	External interrupt 1 enable bit.
ET0	IE.1	Timer 0 interrupt enable bit.
EX0	IE.0	External interrupt 0 enable bit.

User software should never write 1s to unimplemented bits, because they may be used in future AT89 products.

Figure 10. Interrupt Sources

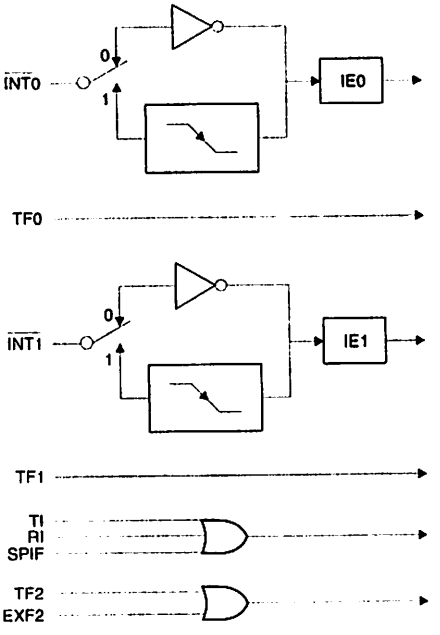


Figure 11. Oscillator Connections

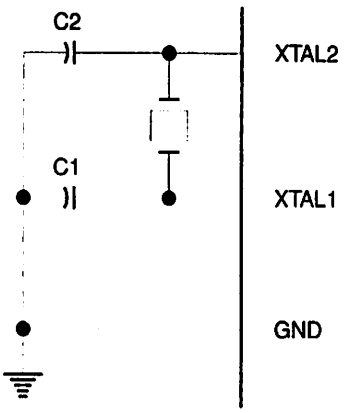
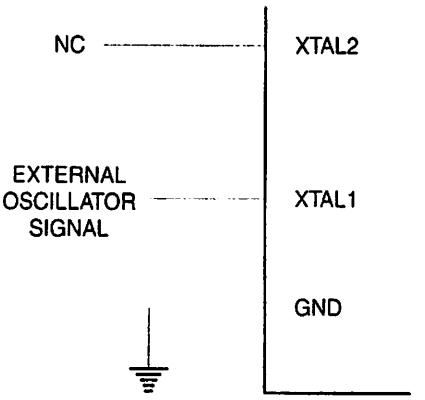


Figure 12. External Clock Drive Configuration



Note: Note: C1, C2 = 30 pF □ 10 pF for Crystals
= 40 pF □ 10 pF for Ceramic Resonators

Oscillator Characteristics

XTAL1 and XTAL2 are the input and output, respectively, of an inverting amplifier that can be configured for use as an on-chip oscillator, as shown in Figure 11. Either a quartz crystal or ceramic resonator may be used. To drive the device from an external clock source, XTAL2 should be left unconnected while XTAL1 is driven, as shown in Figure 12. There are no requirements on the duty cycle of the external clock signal, since the input to the internal clocking circuitry is through a divide-by-two flip-flop, but minimum and maximum voltage high and low time specifications must be observed.

Idle Mode

In idle mode, the CPU puts itself to sleep while all the on-chip peripherals remain active. The mode is invoked by software. The content of the on-chip RAM and all the special functions registers remain unchanged during this mode. The idle mode can be terminated by any enabled interrupt or by a hardware reset.

Note that when idle mode is terminated by a hardware reset, the device normally resumes program execution from where it left off, up to two machine cycles before the internal reset algorithm takes control. On-chip hardware inhibits access to internal RAM in this event, but access to the port pins is not inhibited. To eliminate the possibility of an unexpected write to a port pin when idle mode is terminated by a reset, the instruction following the one that invokes idle mode should not write to a port pin or to external memory.

Power Down Mode

In the power down mode, the oscillator is stopped and the instruction that invokes power down is the last instruction executed. The on-chip RAM and Special Function Registers retain their values until the power down mode is terminated. Exit from power down can be initiated either by a hardware reset or by an enabled external interrupt. Reset redefines the SFRs but does not change the on-chip RAM. The reset should not be activated before V_{CC} is restored to its normal operating level and must be held active long enough to allow the oscillator to restart and stabilize.

To exit power down via an interrupt, the external interrupt must be enabled as level sensitive before entering power down. The interrupt service routine starts at 16 ms (nominal) after the enabled interrupt pin is activated.

Status of External Pins During Idle and Power Down Modes

Mode	Program Memory	ALE	$\overline{PSEN}$	PORT0	PORT1	PORT2	PORT3
Idle	Internal	1	1	Data	Data	Data	Data
Idle	External	1	1	Float	Data	Address	Data
Power Down	Internal	0	0	Data	Data	Data	Data
Power Down	External	0	0	Float	Data	Data	Data

Program Memory Lock Bits

The AT89S8252 has three lock bits that can be left unprogrammed (U) or can be programmed (P) to obtain the additional features listed in the following table.

When lock bit 1 is programmed, the logic level at the $\overline{EA}$ pin is sampled and latched during reset. If the device is powered up without a reset, the latch initializes to a random value and holds that value until reset is activated. The latched value of $\overline{EA}$ must agree with the current logic level at that pin in order for the device to function properly.

Once programmed, the lock bits can only be unprogrammed with the Chip Erase operations in either the parallel or serial modes.

Lock Bit Protection Modes[1][2]

Program Lock Bits				Protection Type
	LB1	LB2	LB3	
1	U	U	U	No internal memory lock feature.
2	P	U	U	MOVC instructions executed from external program memory are disabled from fetching code bytes from internal memory. $\overline{EA}$ is sampled and latched on reset and further programming of the Flash memory (parallel or serial mode) is disabled.
3	P	P	U	Same as Mode 2, but parallel or serial verify are also disabled.
4	P	P	P	Same as Mode 3, but external execution is also disabled.

Notes: 1. U = Unprogrammed
2. P = Programmed

Programming the Flash and EEPROM

Atmel's AT89S8252 Flash Microcontroller offers 8K bytes of in-system reprogrammable Flash Code memory and 2K bytes of EEPROM Data memory.

The AT89S8252 is normally shipped with the on-chip Flash Code and EEPROM Data memory arrays in the erased state (i.e. contents = FFH) and ready to be programmed. This device supports a High-Voltage (12V) Parallel programming mode and a Low-Voltage (5V) Serial programming mode. The serial programming mode provides a convenient way to download the AT89S8252 inside the user's system. The parallel programming mode is compatible with conventional third party Flash or EPROM programmers.

The Code and Data memory arrays are mapped via separate address spaces in the serial programming mode. In the parallel programming mode, the two arrays occupy one contiguous address space: 0000H to 1FFFH for the Code array and 2000H to 27FFH for the Data array.

The Code and Data memory arrays on the AT89S8252 are programmed byte-by-byte in either programming mode. An auto-erase cycle is provided with the self-timed programming operation in the serial programming mode. There is no need to perform the Chip Erase operation to reprogram any memory location in the serial programming mode unless any of the lock bits have been programmed.

In the parallel programming mode, there is no auto-erase cycle. To reprogram any non-blank byte, the user needs to use the Chip Erase operation first to erase both arrays.

Parallel Programming Algorithm

To program and verify the AT89S8252 in the parallel programming mode, the following sequence is recommended:

1. Power-up sequence:
   Apply power between V_{CC} and GND pins.
   Set RST pin to "H".
   Apply a 3 MHz to 24 MHz clock to XTAL1 pin and wait for at least 10 milliseconds.
2. Set $\overline{PSEN}$ pin to "L"
   ALE pin to "H"
   $\overline{EA}$ pin to "H" and all other pins to "H".
3. Apply the appropriate combination of "H" or "L" logic levels to pins P2.6, P2.7, P3.6, P3.7 to select one of the programming operations shown in the Flash Programming Modes table.
4. Apply the desired byte address to pins P1.0 to P1.7 and P2.0 to P2.5.
   Apply data to pins P0.0 to P0.7 for Write Code operation.
5. Raise $\overline{EA}/V_{PP}$ to 12V to enable Flash programming, erase or verification.
6. Pulse ALE/$\overline{PROG}$ once to program a byte in the Code memory array, the Data memory array or the lock bits. The byte-write cycle is self-timed and typically takes 1.5 ms.
7. To verify the byte just programmed, bring pin P2.7 to "L" and read the programmed data at pins P0.0 to P0.7.

8. Repeat steps 3 through 7 changing the address and data for the entire 2K or 8K bytes array or until the end of the object file is reached.
9. Power-off sequence:

   Set XTAL1 to "L".

   Set RST and $\overline{EA}$ pins to "L".

   Turn V_{CC} power off.

In the parallel programming mode, there is no auto-erase cycle and to reprogram any non-blank byte, the user needs to use the Chip Erase operation first to erase both arrays.

$\overline{DATA}$ Polling

The AT89S8252 features $\overline{DATA}$ Polling to indicate the end of a write cycle. During a write cycle in the parallel or serial programming mode, an attempted read of the last byte written will result in the complement of the written datum on P0.7 (parallel mode), and on the MSB of the serial output byte on MISO (serial mode). Once the write cycle has been completed, true data are valid on all outputs, and the next cycle may begin. $\overline{DATA}$ Polling may begin any time after a write cycle has been initiated.

Ready/$\overline{Busy}$

The progress of byte programming in the parallel programming mode can also be monitored by the RDY/$\overline{BSY}$ output signal. Pin P3.4 is pulled Low after ALE goes High during programming to indicate $\overline{BUSY}$. P3.4 is pulled High again when programming is done to indicate READY.

Program Verify

If lock bits LB1 and LB2 have not been programmed, the programmed Code or Data byte can be read back via the address and data lines for verification. The state of the lock bits can also be verified directly in the parallel programming mode. In the serial programming mode, the state of the lock bits can only be verified indirectly by observing that the lock bit features are enabled.

Chip Erase

Both Flash and EEPROM arrays are erased electrically at the same time. In the parallel programming mode, chip erase is initiated by using the proper combination of control signals and by holding ALE/$\overline{PROG}$ low for 10 ms. The Code and Data arrays are written with all "1"s in the Chip Erase operation.

In the serial programming mode, a chip erase operation is initiated by issuing the Chip Erase instruction. In this mode, chip erase is self-timed and takes about 16 ms.

During chip erase, a serial read from any address location will return 00H at the data outputs.

Serial Programming Fuse

A programmable fuse is available to disable Serial Programming if the user needs maximum system security. The Serial Programming Fuse can only be programmed or erased in the Parallel Programming Mode.

The AT89S8252 is shipped with the Serial Programming Mode enabled.

Reading the Signature Bytes: The signature bytes are read by the same procedure as a normal verification of locations 030H and 031H, except that P3.6 and P3.7 must be pulled to a logic low. The values returned are as follows:

(030H) = 1EH indicates manufactured by Atmel
(031H) = 72H indicates 89S8252

Programming Interface

Every code byte in the Flash and EEPROM arrays can be written, and the entire array can be erased, by using the appropriate combination of control signals. The write operation cycle is self-timed and once initiated, will automatically time itself to completion.

All major programming vendors offer worldwide support for the Atmel microcontroller series. Please contact your local programming vendor for the appropriate software revision.

Serial Downloading

Both the Code and Data memory arrays can be programmed using the serial SPI bus while RST is pulled to V_{CC}. The serial interface consists of pins SCK, MOSI (input) and MISO (output). After RST is set high, the Programming Enable instruction needs to be executed first before program/erase operations can be executed.

An auto-erase cycle is built into the self-timed programming operation (in the serial mode ONLY) and there is no need to first execute the Chip Erase instruction unless any of the lock bits have been programmed. The Chip Erase operation turns the content of every memory location in both the Code and Data arrays into FFH.

The Code and Data memory arrays have separate address spaces:

0000H to 1FFFH for Code memory and 000H to 7FFH for Data memory.

Either an external system clock is supplied at pin XTAL1 or a crystal needs to be connected across pins XTAL1 and XTAL2. The maximum serial clock (SCK) frequency should be less than 1/40 of the crystal frequency. With a 24 MHz oscillator clock, the maximum SCK frequency is 600 kHz.

Serial Programming Algorithm

To program and verify the AT89S8252 in the serial programming mode, the following sequence is recommended:

1. Power-up sequence:

   Apply power between V_{CC} and GND pins.

   Set RST pin to "H".

   If a crystal is not connected across pins XTAL1 and XTAL2, apply a 3 MHz to 24 MHz clock to XTAL1 pin and wait for at least 10 milliseconds.
2. Enable serial programming by sending the Programming Enable serial instruction to pin MOSI/P1.5. The frequency of the shift clock supplied at pin SCK/P1.7 needs to be less than the CPU clock at XTAL1 divided by 40.
3. The Code or Data array is programmed one byte at a time by supplying the address and data together with the appropriate Write instruction. The selected memory location is first automatically erased before new data is written. The write cycle is self-timed and typically takes less than 2.5 ms at 5V.
4. Any memory location can be verified by using the Read instruction which returns the content at the selected address at serial output MISO/P1.6.
5. At the end of a programming session, RST can be set low to commence normal operation.

Power-off sequence (if needed):

Set XTAL1 to "L" (if a crystal is not used).

Set RST to "L".

Turn V_{CC} power off.

Serial Programming Instruction

The Instruction Set for Serial Programming follows a 3-byte protocol and is shown in the following table:

Instruction Set

Instruction	Input Format			Operation
	Byte 1	Byte 2	Byte 3	
Programming Enable	1010 1100	0101 0011	xxxx xxxx	Enable serial programming interface after RST goes high.
Chip Erase	1010 1100	xxxx x100	xxxx xxxx	Chip erase both 8K & 2K memory arrays.
Read Code Memory	aaaa a001	low addr	xxxx xxxx	Read data from Code memory array at the selected address. The 5 MSBs of the first byte are the high order address bits. The low order address bits are in the second byte. Data are available at pin MISO during the third byte.
Write Code Memory	aaaa a010	low addr	data in	Write data to Code memory location at selected address. The address bits are the 5 MSBs of the first byte together with the second byte.
Read Data Memory	00aa a101	low addr	xxxx xxxx	Read data from Data memory array at selected address. Data are available at pin MISO during the third byte.
Write Data Memory	00aa a110	low addr	data in	Write data to Data memory location at selected address.
Write Lock Bits	1010 1100	LB1 LB2 LB3 x x111	xxxx xxxx	Write lock bits. Set LB1, LB2 or LB3 = "0" to program lock bits.

Notes: 1. $\overline{\text{DATA}}$ polling is used to indicate the end of a write cycle which typically takes less than 2.5 ms at 5V.
2. "aaaaa" = high order address.
3. "x" = don't care.

Flash and EEPROM Parallel Programming Modes

Mode	RST	$\overline{PSEN}$	ALE/$\overline{PROG}$	$\overline{EA}$/V_{PP}	P2.6	P2.7	P3.6	P3.7	Data I/O P0.7:0	Address P2.5:0 P1.7:0
Serial Prog. Modes	H	h(1)	h(1)	x						
Chip Erase	H	L	 (2)	12V	H	L	L	L	X	X
Write (10K bytes) Memory	H	L		12V	L	H	H	H	DIN	ADDR
Read (10K bytes) Memory	H	L	H	12V	L	L	H	H	DOUT	ADDR
Write Lock Bits:	H	L		12V	H	L	H	L	DIN	X
Bit - 1									P0.7 = 0	X
Bit - 2									P0.6 = 0	X
Bit - 3									P0.5 = 0	X
Read Lock Bits:	H	L	H	12V	H	H	L	L	DOUT	X
Bit - 1									@P0.2	X
Bit - 2									@P0.1	X
Bit - 3									@P0.0	X
Read Atmel Code	H	L	H	12V	L	L	L	L	DOUT	30H
Read Device Code	H	L	H	12V	L	L	L	L	DOUT	31H
Serial Prog. Enable	H	L	 (2)	12V	L	H	L	H	P0.0 = 0	X
Serial Prog. Disable	H	L	 (2)	12V	L	H	L	H	P0.0 = 1	X
Read Serial Prog. Fuse	H	L	H	12V	H	H	L	H	@P0.0	X

Notes:
1. "h" = weakly pulled "High" internally.
2. Chip Erase and Serial Programming Fuse require a 10-ms $\overline{PROG}$ pulse. Chip Erase needs to be performed first before reprogramming any byte with a content other than FFH.
3. P3.4 is pulled Low during programming to indicate RDY/$\overline{BSY}$.
4. "X" = don't care

Figure 14. Programming the Flash/EEPROM Memory

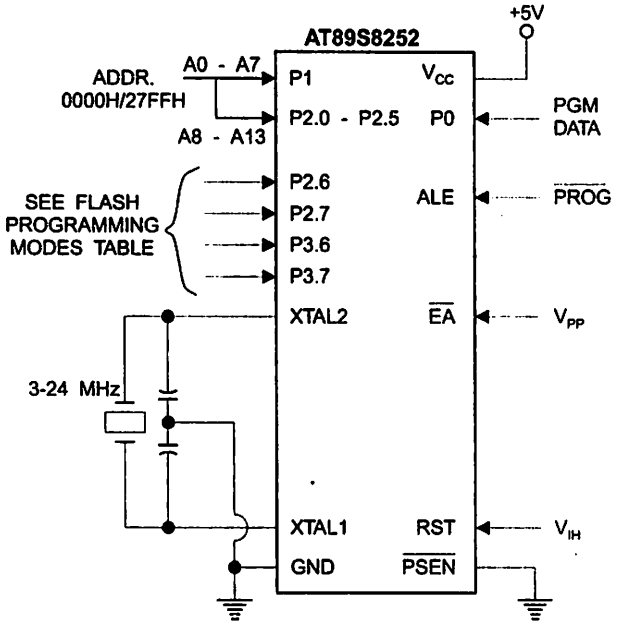


Figure 15. Flash/EEPROM Serial Downloading

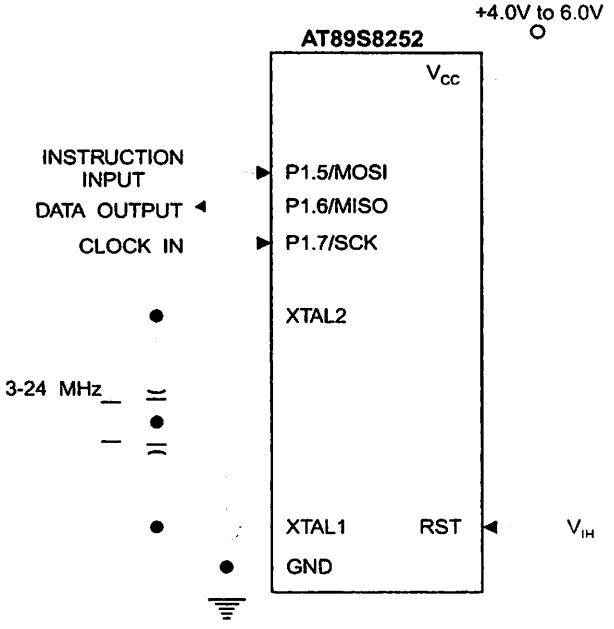
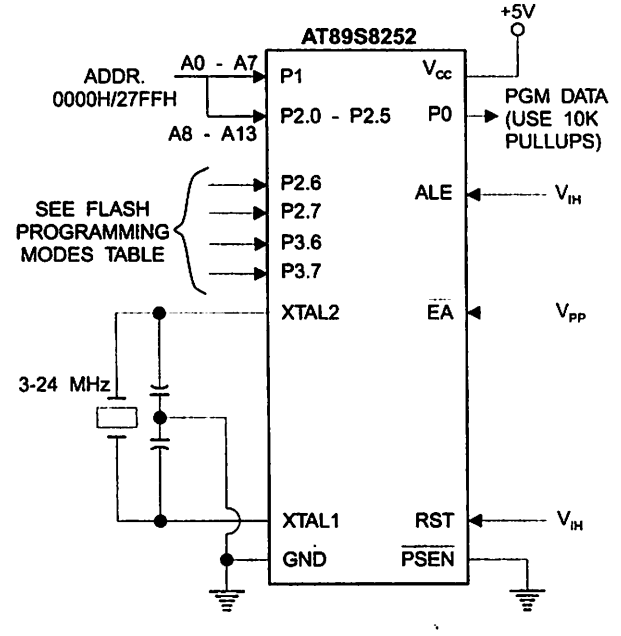


Figure 16. Verifying the Flash/EEPROM Memory

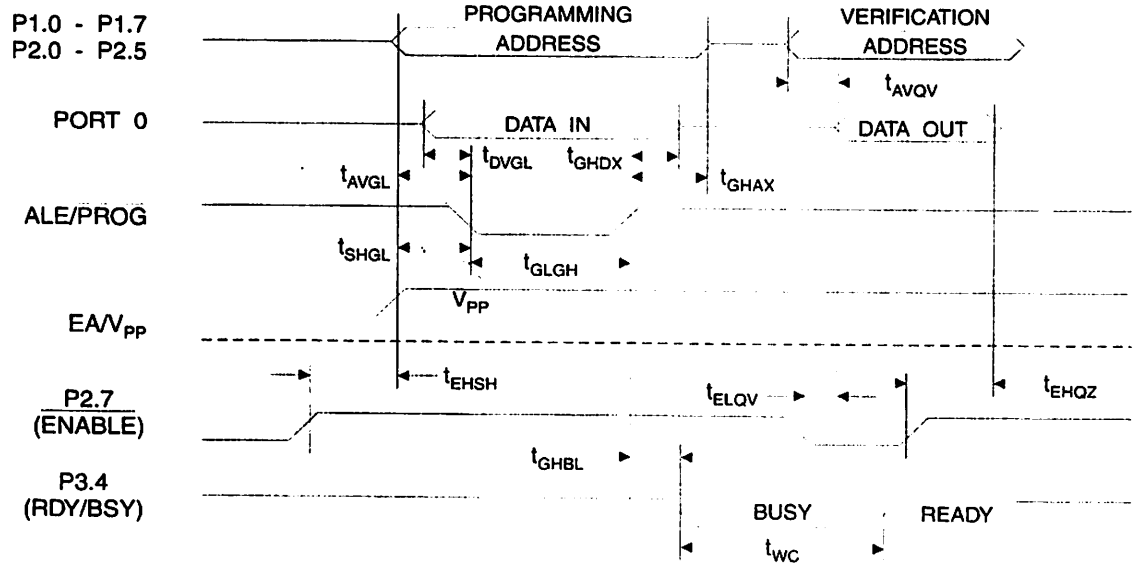


Flash Programming and Verification Characteristics-Parallel Mode

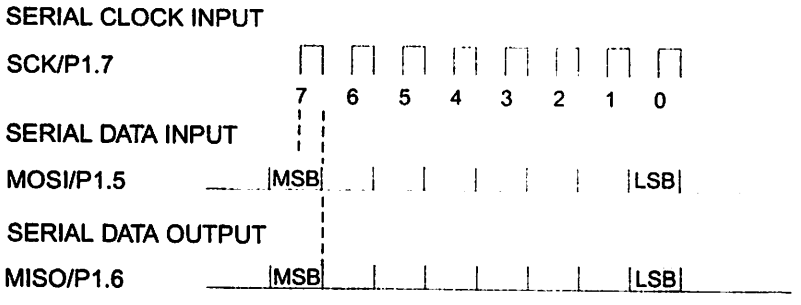
T_A = 0°C to 70°C, V_{CC} = 5.0V □ 10%

Symbol	Parameter	Min	Max	Units
V_{PP}	Programming Enable Voltage	11.5	12.5	V
I_{PP}	Programming Enable Current		1.0	mA
$1/t_{CLCL}$	Oscillator Frequency	3	24	MHz
t_{AVGL}	Address Setup to $\overline{PROG}$ Low	$48t_{CLCL}$		
t_{GHAX}	Address Hold After $\overline{PROG}$	$48t_{CLCL}$		
t_{DVGL}	Data Setup to $\overline{PROG}$ Low	$48t_{CLCL}$		
t_{GHDX}	Data Hold After $\overline{PROG}$	$48t_{CLCL}$		
t_{EHSH}	P2.7 ($\overline{ENABLE}$) High to V_{PP}	$48t_{CLCL}$		
t_{SHGL}	V_{PP} Setup to $\overline{PROG}$ Low	10		□s
t_{GLGH}	$\overline{PROG}$ Width	1	110	□s
t_{AVQV}	Address to Data Valid		$48t_{CLCL}$	
t_{ELQV}	$\overline{ENABLE}$ Low to Data Valid		$48t_{CLCL}$	
t_{EHQZ}	Data Float After $\overline{ENABLE}$	0	$48t_{CLCL}$	
t_{GHBL}	$\overline{PROG}$ High to $\overline{BUSY}$ Low		1.0	□s
t_{WC}	Byte Write Cycle Time		2.0	ms

Flash/EEPROM Programming and Verification Waveforms - Parallel Mode



Serial Downloading Waveforms



Absolute Maximum Ratings*

Operating Temperature	-55°C to +125°C
Storage Temperature	-65°C to +150°C
Voltage on Any Pin with Respect to Ground	-1.0V to +7.0V
Maximum Operating Voltage	6.6V
DC Output Current	15.0 mA

*NOTICE: Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC Characteristics

The values shown in this table are valid for T_A = -40°C to 85°C and V_{CC} = 5.0V □20%, unless otherwise noted.

Symbol	Parameter	Condition	Min	Max	Units
V_{IL}	Input Low Voltage	(Except $\overline{EA}$)	-0.5	0.2 V_{CC} - 0.1	V
V_{IL1}	Input Low Voltage ($\overline{EA}$)		-0.5	0.2 V_{CC} - 0.3	V
V_{IH}	Input High Voltage	(Except XTAL1, RST)	0.2 V_{CC} + 0.9	V_{CC} + 0.5	V
V_{IH1}	Input High Voltage	(XTAL1, RST)	0.7 V_{CC}	V_{CC} + 0.5	V
V_{OL}	Output Low Voltage (1) (Ports 1,2,3)	I_{OL} = 1.6 mA		0.5	V
V_{OL1}	Output Low Voltage (1) (Port 0, ALE, $\overline{PSEN}$)	I_{OL} = 3.2 mA		0.5	V
V_{OH}	Output High Voltage (Ports 1,2,3, ALE, $\overline{PSEN}$)	I_{OH} = -60 □A, V_{CC} = 5V □10%	2.4		V
		I_{OH} = -25 □A	0.75 V_{CC}		V
		I_{OH} = -10 □A	0.9 V_{CC}		V
V_{OH1}	Output High Voltage (Port 0 in External Bus Mode)	I_{OH} = -800 □A, V_{CC} = 5V □10%	2.4		V
		I_{OH} = -300 □A	0.75 V_{CC}		V
		I_{OH} = -80 □A	0.9 V_{CC}		V
I_{IL}	Logical 0 Input Current (Ports 1,2,3)	V_{IN} = 0.45V		-50	□A
I_{TL}	Logical 1 to 0 Transition Current (Ports 1,2,3)	V_{IN} = 2V, V_{CC} = 5V □10%		-650	□A
I_{LI}	Input Leakage Current (Port 0, $\overline{EA}$)	0.45 < V_{IN} < V_{CC}		□10	□A
RRST	Reset Pulldown Resistor		50	300	K□
C_{IO}	Pin Capacitance	Test Freq. = 1 MHz, T_A = 25°C		10	pF
I_{CC}	Power Supply Current	Active Mode, 12 MHz		25	mA
		Idle Mode, 12 MHz		6.5	mA
	Power Down Mode (2)	V_{CC} = 6V		100	□A
		V_{CC} = 3V		40	□A

Notes: 1. Under steady state (non-transient) conditions, I_{OL} must be externally limited as follows:
Maximum I_{OL} per port pin: 10 mA
Maximum I_{OL} per 8-bit port:
Port 0: 26 mA
Ports 1, 2, 3: 15 mA
Maximum total I_{OL} for all output pins: 71 mA
If I_{OL} exceeds the test condition, V_{OL} may exceed the related specification. Pins are not guaranteed to sink current greater than the listed test conditions.

2. Minimum V_{CC} for Power Down is 2V

eatures

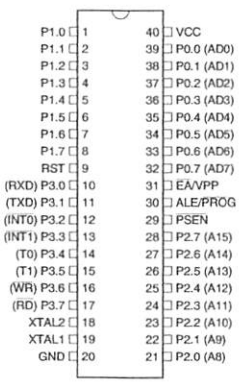
- Compatible with MCS-51™ Products
- 4K Bytes of In-System Reprogrammable Flash Memory
  - Endurance: 1,000 Write/Erase Cycles
- Fully Static Operation: 0 Hz to 24 MHz
- Three-level Program Memory Lock
- 128 x 8-bit Internal RAM
- 32 Programmable I/O Lines
- Two 16-bit Timer/Counters
- Six Interrupt Sources
- Programmable Serial Channel
- Low-power Idle and Power-down Modes

escription

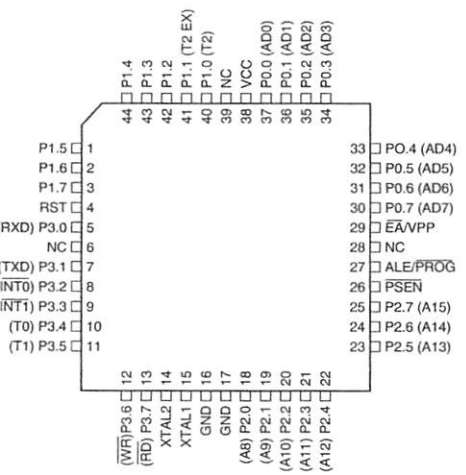
he AT89C51 is a low-power, high-performance CMOS 8-bit microcomputer with 4K ytes of Flash programmable and erasable read only memory (PEROM). The device manufactured using Atmel's high-density nonvolatile memory technology and is mpatible with the industry-standard MCS-51 instruction set and pinout. The on-chip ash allows the program memory to be reprogrammed in-system or by a conven- onal nonvolatile memory programmer. By combining a versatile 8-bit CPU with Flash a monolithic chip, the Atmel AT89C51 is a powerful microcomputer which provides highly-flexible and cost-effective solution to many embedded control applications.

in Configurations

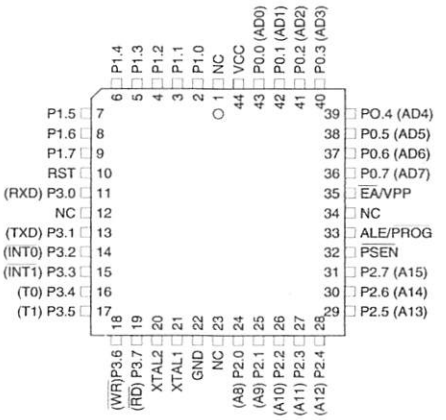
PDIP



PQFP/TQFP



PLCC

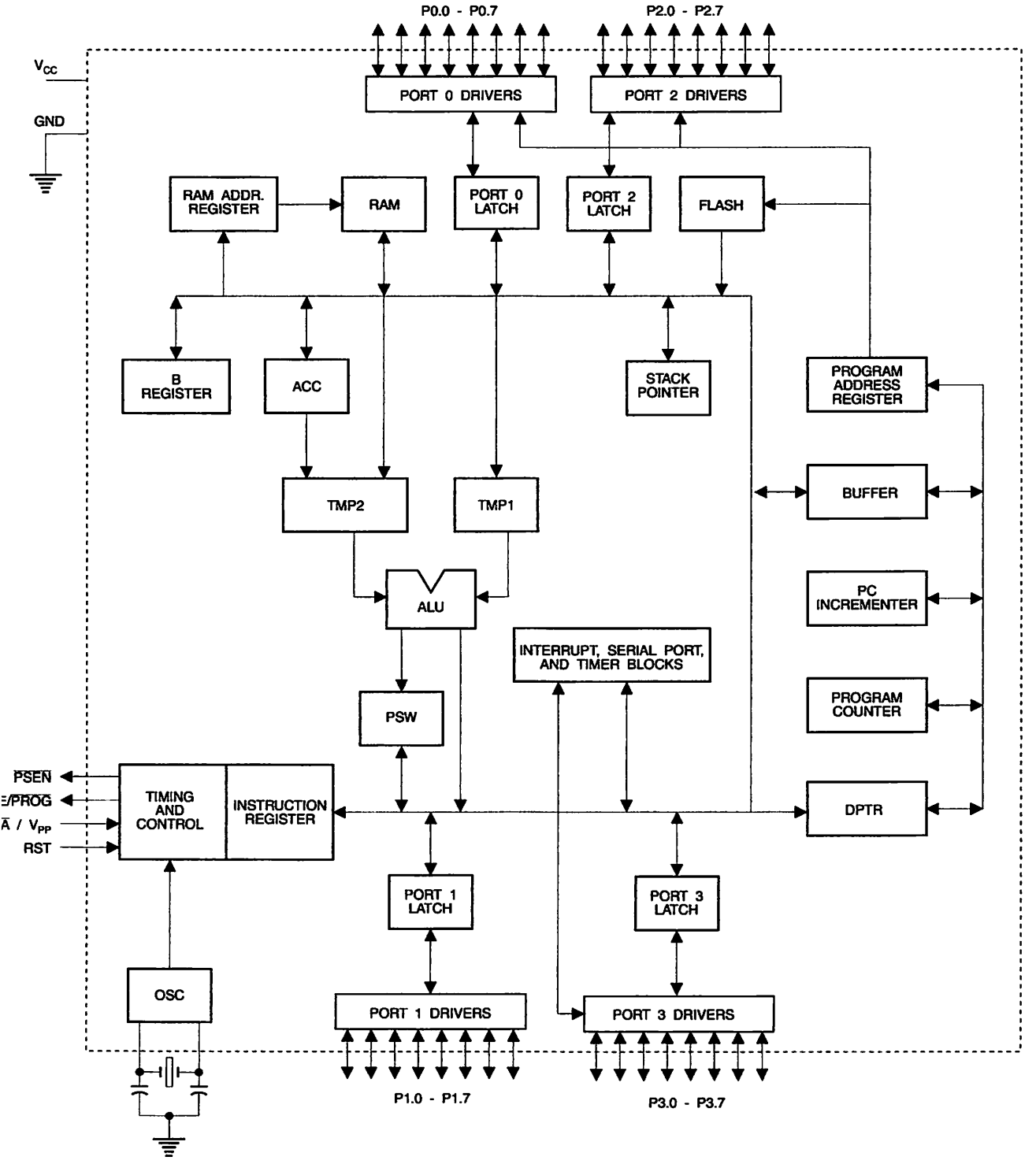


8-bit Microcontroller with 4K Bytes Flash

AT89C51

Rev. 0265G–02/00

lock Diagram



e AT89C51 provides the following standard features: 4K tes of Flash, 128 bytes of RAM, 32 I/O lines, two 16-bit ıer/counters, a five vector two-level interrupt architecture, ull duplex serial port, on-chip oscillator and clock cir- itry. In addition, the AT89C51 is designed with static logic operation down to zero frequency and supports two ftware selectable power saving modes. The Idle Mode ops the CPU while allowing the RAM, timer/counters, rial port and interrupt system to continue functioning. The wer-down Mode saves the RAM contents but freezes oscillator disabling all other chip functions until the next rdware reset.

in Description

:C

ıpply voltage.

ND

ound.

ort 0

ort 0 is an 8-bit open-drain bi-directional I/O port. As an tput port, each pin can sink eight TTL inputs. When 1s e written to port 0 pins, the pins can be used as high- pedance inputs.

ort 0 may also be configured to be the multiplexed low- der address/data bus during accesses to external pro- am and data memory. In this mode P0 has internal llups.

ort 0 also receives the code bytes during Flash program- ng, and outputs the code bytes during program rification. External pullups are required during program rification.

ort 1

ort 1 is an 8-bit bi-directional I/O port with internal pullups. e Port 1 output buffers can sink/source four TTL inputs. hen 1s are written to Port 1 pins they are pulled high by e internal pullups and can be used as inputs. As inputs, ort 1 pins that are externally being pulled low will source rrent (I_{IL}) because of the internal pullups.

ort 1 also receives the low-order address bytes during ash programming and verification.

ort 2

ort 2 is an 8-bit bi-directional I/O port with internal pullups. e Port 2 output buffers can sink/source four TTL inputs. hen 1s are written to Port 2 pins they are pulled high by e internal pullups and can be used as inputs. As inputs, Port 2 pins that are externally being pulled low will source current (I_{IL}) because of the internal pullups.

Port 2 emits the high-order address byte during fetches from external program memory and during accesses to external data memory that use 16-bit addresses (MOVX @ DPTR). In this application, it uses strong internal pullups when emitting 1s. During accesses to external data memory that use 8-bit addresses (MOVX @ RI), Port 2 emits the contents of the P2 Special Function Register.

Port 2 also receives the high-order address bits and some control signals during Flash programming and verification.

Port 3

Port 3 is an 8-bit bi-directional I/O port with internal pullups. The Port 3 output buffers can sink/source four TTL inputs. When 1s are written to Port 3 pins they are pulled high by the internal pullups and can be used as inputs. As inputs, Port 3 pins that are externally being pulled low will source current (I_{IL}) because of the pullups.

Port 3 also serves the functions of various special features of the AT89C51 as listed below:

Port Pin	Alternate Functions
P3.0	RXD (serial input port)
P3.1	TXD (serial output port)
P3.2	$\overline{INT0}$ (external interrupt 0)
P3.3	$\overline{INT1}$ (external interrupt 1)
P3.4	T0 (timer 0 external input)
P3.5	T1 (timer 1 external input)
P3.6	$\overline{WR}$ (external data memory write strobe)
P3.7	$\overline{RD}$ (external data memory read strobe)

Port 3 also receives some control signals for Flash programming and verification.

RST

Reset input. A high on this pin for two machine cycles while the oscillator is running resets the device.

ALE/$\overline{PROG}$

Address Latch Enable output pulse for latching the low byte of the address during accesses to external memory. This pin is also the program pulse input ($\overline{PROG}$) during Flash programming.

In normal operation ALE is emitted at a constant rate of 1/6 the oscillator frequency, and may be used for external timing or clocking purposes. Note, however, that one ALE

lse is skipped during each access to external Data emory.

lesired, ALE operation can be disabled by setting bit 0 of R location 8EH. With the bit set, ALE is active only dur- a MOVX or MOVC instruction. Otherwise, the pin is akly pulled high. Setting the ALE-disable bit has no ect if the microcontroller is in external execution mode.

EN

ogram Store Enable is the read strobe to external pro- am memory.

hen the AT89C51 is executing code from external pro- am memory, PSEN is activated twice each machine cle, except that two PSEN activations are skipped during ch access to external data memory.

VPP

ternal Access Enable. EA must be strapped to GND in der to enable the device to fetch code from external pro- am memory locations starting at 0000H up to FFFFH. te, however, that if lock bit 1 is programmed, EA will be ernally latched on reset.

should be strapped to V_{CC} for internal program ecutions.

is pin also receives the 12-volt programming enable volt- e (V_{PP}) during Flash programming, for parts that require -volt V_{PP}.

AL1

ut to the inverting oscillator amplifier and input to the ernal clock operating circuit.

AL2

tput from the inverting oscillator amplifier.

scillator Characteristics

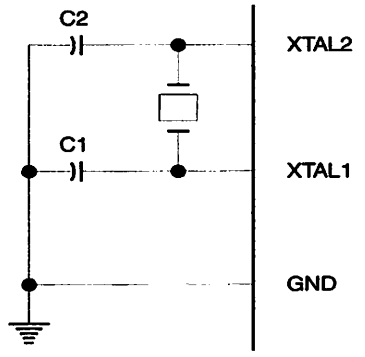
AL1 and XTAL2 are the input and output, respectively, an inverting amplifier which can be configured for use as on-chip oscillator, as shown in Figure 1. Either a quartz ystal or ceramic resonator may be used. To drive the vice from an external clock source, XTAL2 should be left unconnected while XTAL1 is driven as shown in Figure 2. There are no requirements on the duty cycle of the external clock signal, since the input to the internal clocking circuitry is through a divide-by-two flip-flop, but minimum and maximum voltage high and low time specifications must be observed.

Idle Mode

In idle mode, the CPU puts itself to sleep while all the on-chip peripherals remain active. The mode is invoked by software. The content of the on-chip RAM and all the special functions registers remain unchanged during this mode. The idle mode can be terminated by any enabled interrupt or by a hardware reset.

It should be noted that when idle is terminated by a hard ware reset, the device normally resumes program execution, from where it left off, up to two machine cycles before the internal reset algorithm takes control. On-chip hardware inhibits access to internal RAM in this event, but access to the port pins is not inhibited. To eliminate the possibility of an unexpected write to a port pin when Idle is terminated by reset, the instruction following the one that invokes Idle should not be one that writes to a port pin or to external memory.

Figure 1. Oscillator Connections

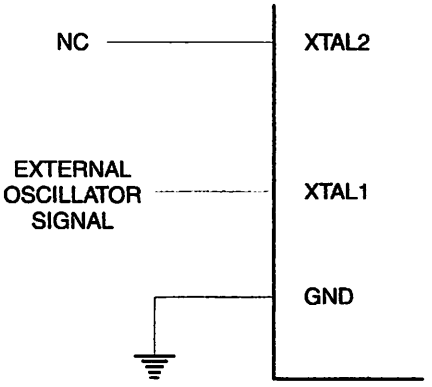


Note: C1, C2 = 30 pF ± 10 pF for Crystals
= 40 pF ± 10 pF for Ceramic Resonators

tatus of External Pins During Idle and Power-down Modes

lode	Program Memory	ALE	PSEN	PORT0	PORT1	PORT2	PORT3
ile	Internal	1	1	Data	Data	Data	Data
ile	External	1	1	Float	Data	Address	Data
ower-down	Internal	0	0	Data	Data	Data	Data
ower-down	External	0	0	Float	Data	Data	Data

ɟure 2. External Clock Drive Configuration



ɔwer-down Mode

the power-down mode, the oscillator is stopped, and the ɨtruction that invokes power-down is the last instruction ecuted. The on-chip RAM and Special Function Registers retain their values until the power-down mode is terminated. The only exit from power-down is a hardware reset. Reset redefines the SFRs but does not change the on-chip RAM. The reset should not be activated before V_{CC} is restored to its normal operating level and must be held active long enough to allow the oscillator to restart and stabilize.

Program Memory Lock Bits

On the chip are three lock bits which can be left unprogrammed (U) or can be programmed (P) to obtain the additional features listed in the table below.

When lock bit 1 is programmed, the logic level at the $\overline{EA}$ pin is sampled and latched during reset. If the device is powered up without a reset, the latch initializes to a random value, and holds that value until reset is activated. It is necessary that the latched value of $\overline{EA}$ be in agreement with the current logic level at that pin in order for the device to function properly.

ɔck Bit Protection Modes

	Program Lock Bits			
	LB1	**LB2**	**LB3**	**Protection Type**
1	U	U	U	No program lock features
2	P	U	U	MOVC instructions executed from external program memory are disabled from fetching code bytes from internal memory, $\overline{EA}$ is sampled and latched on reset, and further programming of the Flash is disabled
3	P	P	U	Same as mode 2, also verify is disabled
4	P	P	P	Same as mode 3, also external execution is disabled

rogramming the Flash

ıe AT89C51 is normally shipped with the on-chip Flash emory array in the erased state (that is, contents = FFH) ıd ready to be programmed. The programming interface :cepts either a high-voltage (12-volt) or a low-voltage $_{CC}$) program enable signal. The low-voltage programing mode provides a convenient way to program the T89C51 inside the user's system, while the high-voltage ogramming mode is compatible with conventional third-ırty Flash or EPROM programmers.

ıe AT89C51 is shipped with either the high-voltage or w-voltage programming mode enabled. The respective p-side marking and device signature codes are listed in e following table.

	V_{PP} = 12V	V_{PP} = 5V
op-Side Mark	AT89C51 xxxx yyww	AT89C51 xxxx-5 yyww
ignature	(030H) = 1EH (031H) = 51H (032H) =F FH	(030H) = 1EH (031H) = 51H (032H) = 05H

ıe AT89C51 code memory array is programmed byte-by-te in either programming mode. *To program any non-ank byte in the on-chip Flash Memory, the entire memory ust be erased using the Chip Erase Mode.*

ogramming Algorithm: Before programming the T89C51, the address, data and control signals should be t up according to the Flash programming mode table and gure 3 and Figure 4. To program the AT89C51, take the lowing steps.

Input the desired memory location on the address lines.

Input the appropriate data byte on the data lines.

Activate the correct combination of control signals.

Raise $\overline{EA}/V_{PP}$ to 12V for the high-voltage programming mode.

Pulse ALE/$\overline{PROG}$ once to program a byte in the Flash array or the lock bits. The byte-write cycle is self-timed and typically takes no more than 1.5 ms. Repeat steps 1 through 5, changing the address and data for the entire array or until the end of the object file is reached.

$\overline{Data}$ Polling: The AT89C51 features $\overline{Data}$ Polling to indicate the end of a write cycle. During a write cycle, an attempted read of the last byte written will result in the complement of the written datum on PO.7. Once the write cycle has been completed, true data are valid on all outputs, and the next cycle may begin. $\overline{Data}$ Polling may begin any time after a write cycle has been initiated.

Ready/$\overline{Busy}$: The progress of byte programming can also be monitored by the RDY/$\overline{BSY}$ output signal. P3.4 is pulled low after ALE goes high during programming to indicate BUSY. P3.4 is pulled high again when programming is done to indicate READY.

Program Verify: If lock bits LB1 and LB2 have not been programmed, the programmed code data can be read back via the address and data lines for verification. The lock bits cannot be verified directly. Verification of the lock bits is achieved by observing that their features are enabled.

Chip Erase: The entire Flash array is erased electrically by using the proper combination of control signals and by holding ALE/$\overline{PROG}$ low for 10 ms. The code array is written with all "1"s. The chip erase operation must be executed before the code memory can be re-programmed.

Reading the Signature Bytes: The signature bytes are read by the same procedure as a normal verification of locations 030H, 031H, and 032H, except that P3.6 and P3.7 must be pulled to a logic low. The values returned are as follows.

(030H) = 1EH indicates manufactured by Atmel
(031H) = 51H indicates 89C51
(032H) = FFH indicates 12V programming
(032H) = 05H indicates 5V programming

Programming Interface

Every code byte in the Flash array can be written and the entire array can be erased by using the appropriate combination of control signals. The write operation cycle is self-timed and once initiated, will automatically time itself to completion.

All major programming vendors offer worldwide support for the Atmel microcontroller series. Please contact your local programming vendor for the appropriate software revision.

lash Programming Modes

lode		RST	PSEN	ALE/PROG	EA/V_{PP}	P2.6	P2.7	P3.6	P3.7
Vrite Code Data		H	L		H/12V	L	H	H	H
ead Code Data		H	L	H	H	L	L	H	H
Vrite Lock	Bit - 1	H	L		H/12V	H	H	H	H
	Bit - 2	H	L		H/12V	H	H	L	L
	Bit - 3	H	L		H/12V	H	L	H	L
hip Erase		H	L	(1)	H/12V	H	L	L	L
ead Signature Byte		H	L	H	H	L	L	L	L

te: 1. Chip Erase requires a 10 ms PROG pulse.

gure 3. Programming the Flash

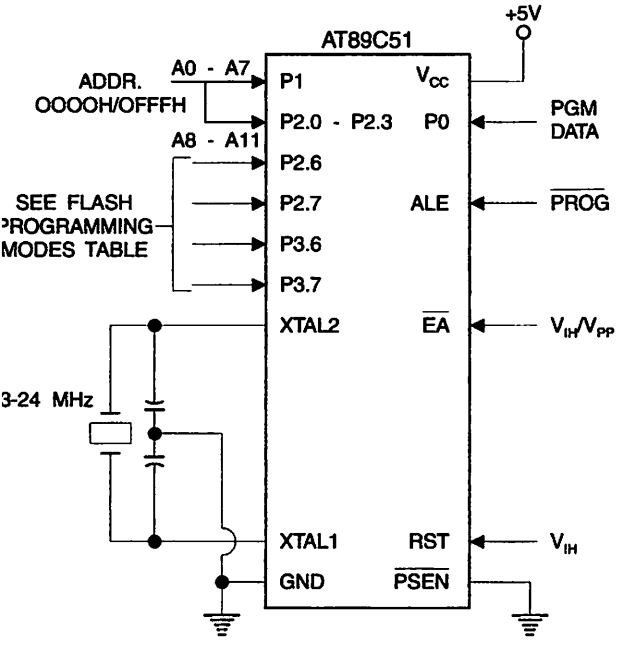
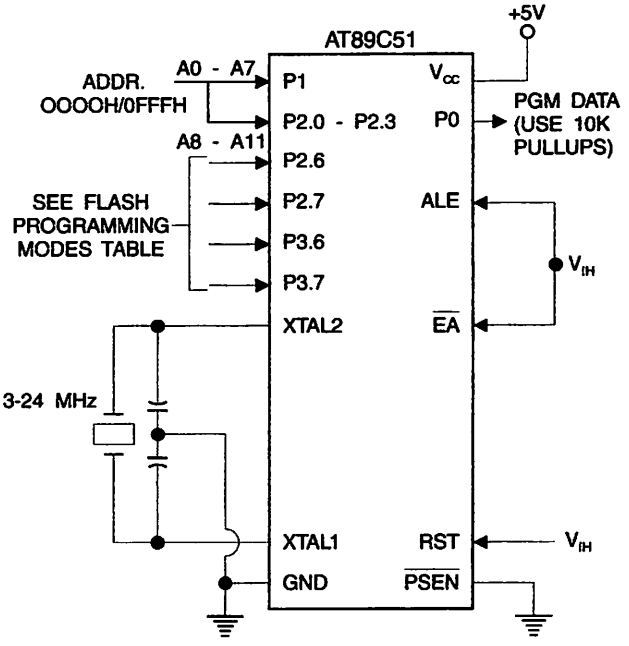
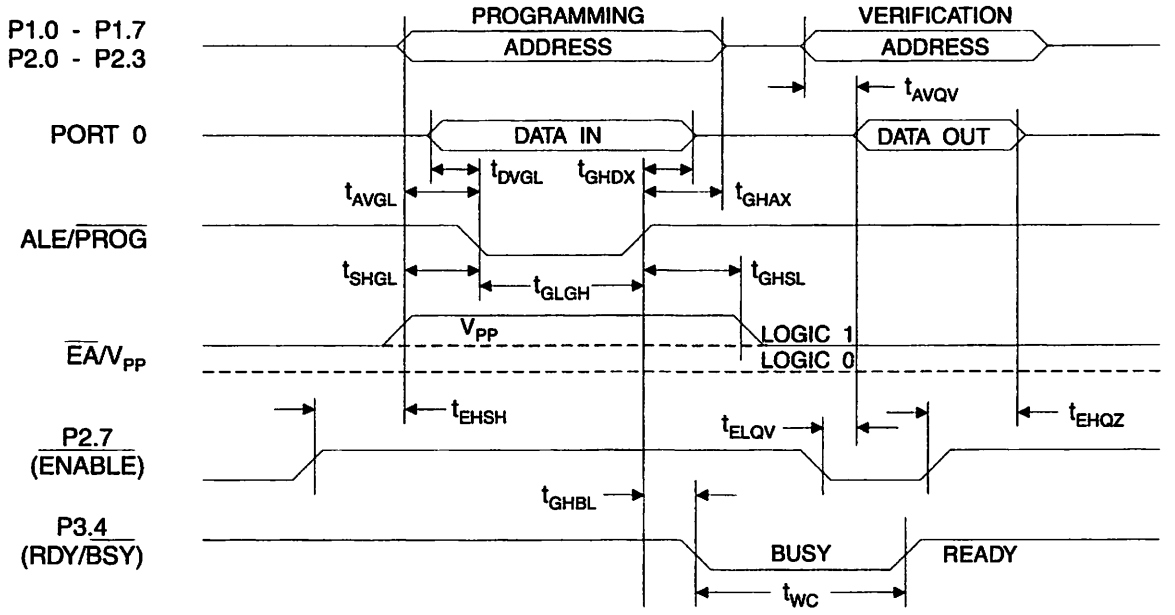


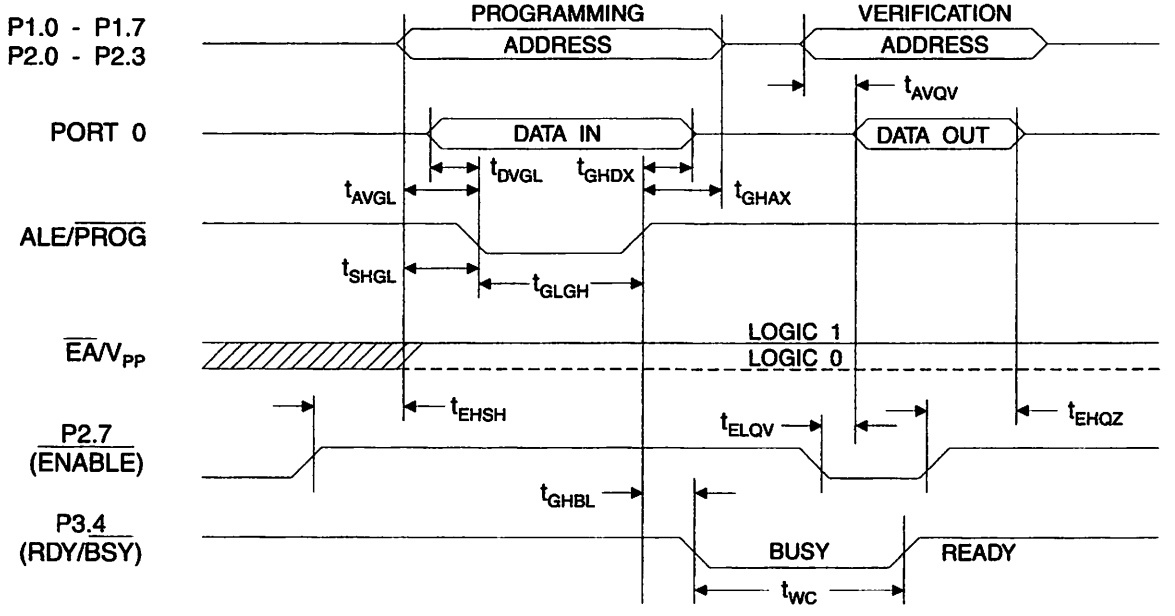
Figure 4. Verifying the Flash



lash Programming and Verification Waveforms - High-voltage Mode (V_{PP} = 12V)



lash Programming and Verification Waveforms - Low-voltage Mode (V_{PP} = 5V)



lash Programming and Verification Characteristics

= 0°C to 70°C, V_{CC} = 5.0 ± 10%

ymbol	Parameter	Min	Max	Units
$/_{PP}$(1)	Programming Enable Voltage	11.5	12.5	V
$_{PP}$(1)	Programming Enable Current		1.0	mA
$/t_{CLCL}$	Oscillator Frequency	3	24	MHz
AVGL	Address Setup to $\overline{PROG}$ Low	$48t_{CLCL}$		
GHAX	Address Hold After $\overline{PROG}$	$48t_{CLCL}$		
DVGL	Data Setup to $\overline{PROG}$ Low	$48t_{CLCL}$		
GHDX	Data Hold After $\overline{PROG}$	$48t_{CLCL}$		
EHSH	P2.7 ($\overline{ENABLE}$) High to V_{PP}	$48t_{CLCL}$		
SHGL	V_{PP} Setup to $\overline{PROG}$ Low	10		µs
$_{GHSL}$(1)	V_{PP} Hold After $\overline{PROG}$	10		µs
$_{GLGH}$	$\overline{PROG}$ Width	1	110	µs
$_{AVQV}$	Address to Data Valid		$48t_{CLCL}$	
$_{ELQV}$	$\overline{ENABLE}$ Low to Data Valid		$48t_{CLCL}$	
$_{EHQZ}$	Data Float After $\overline{ENABLE}$	0	$48t_{CLCL}$	
$_{GHBL}$	$\overline{PROG}$ High to $\overline{BUSY}$ Low		1.0	µs
$_{WC}$	Byte Write Cycle Time		2.0	ms

ote: 1. Only used in 12-volt programming mode.

bsolute Maximum Ratings*

)perating Temperature	-55°C to +125°C
torage Temperature	-65°C to +150°C
'oltage on Any Pin ith Respect to Ground	-1.0V to +7.0V
laximum Operating Voltage	6.6V
C Output Current	15.0 mA

*NOTICE: Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

C Characteristics

= -40°C to 85°C, V_{CC} = 5.0V ± 20% (unless otherwise noted)

ymbol	Parameter	Condition	Min	Max	Units
IL	Input Low-voltage	(Except $\overline{EA}$)	-0.5	0.2 V_{CC} - 0.1	V
IL1	Input Low-voltage ($\overline{EA}$)		-0.5	0.2 V_{CC} - 0.3	V
IH	Input High-voltage	(Except XTAL1, RST)	0.2 V_{CC} + 0.9	V_{CC} + 0.5	V
IH1	Input High-voltage	(XTAL1, RST)	0.7 V_{CC}	V_{CC} + 0.5	V
OL	Output Low-voltage[1] (Ports 1,2,3)	I_{OL} = 1.6 mA		0.45	V
OL1	Output Low-voltage[1] (Port 0, ALE, $\overline{PSEN}$)	I_{OL} = 3.2 mA		0.45	V
OH	Output High-voltage (Ports 1,2,3, ALE, $\overline{PSEN}$)	I_{OH} = -60 µA, V_{CC} = 5V ± 10%	2.4		V
		I_{OH} = -25 µA	0.75 V_{CC}		V
		I_{OH} = -10 µA	0.9 V_{CC}		V
OH1	Output High-voltage (Port 0 in External Bus Mode)	I_{OH} = -800 µA, V_{CC} = 5V ± 10%	2.4		V
		I_{OH} = -300 µA	0.75 V_{CC}		V
		I_{OH} = -80 µA	0.9 V_{CC}		V
-	Logical 0 Input Current (Ports 1,2,3)	V_{IN} = 0.45V		-50	µA
L	Logical 1 to 0 Transition Current (Ports 1,2,3)	V_{IN} = 2V, VCC = 5V ± 10%		-650	µA
I	Input Leakage Current (Port 0, $\overline{EA}$)	0.45 < V_{IN} < V_{CC}		±10	µA
RST	Reset Pull-down Resistor		50	300	KΩ
IO	Pin Capacitance	Test Freq. = 1 MHz, T_A = 25°C		10	pF
	Power Supply Current	Active Mode, 12 MHz		20	mA
		Idle Mode, 12 MHz		5	mA
C	Power-down Mode[2]	V_{CC} = 6V		100	µA
		V_{CC} = 3V		40	µA

tes:
1. Under steady state (non-transient) conditions, I_{OL} must be externally limited as follows:
   Maximum I_{OL} per port pin: 10 mA
   Maximum I_{OL} per 8-bit port: Port 0: 26 mA
   Ports 1, 2, 3: 15 mA
   Maximum total I_{OL} for all output pins: 71 mA
   If I_{OL} exceeds the test condition, V_{OL} may exceed the related specification. Pins are not guaranteed to sink current greater than the listed test conditions.
2. Minimum V_{CC} for Power-down is 2V.

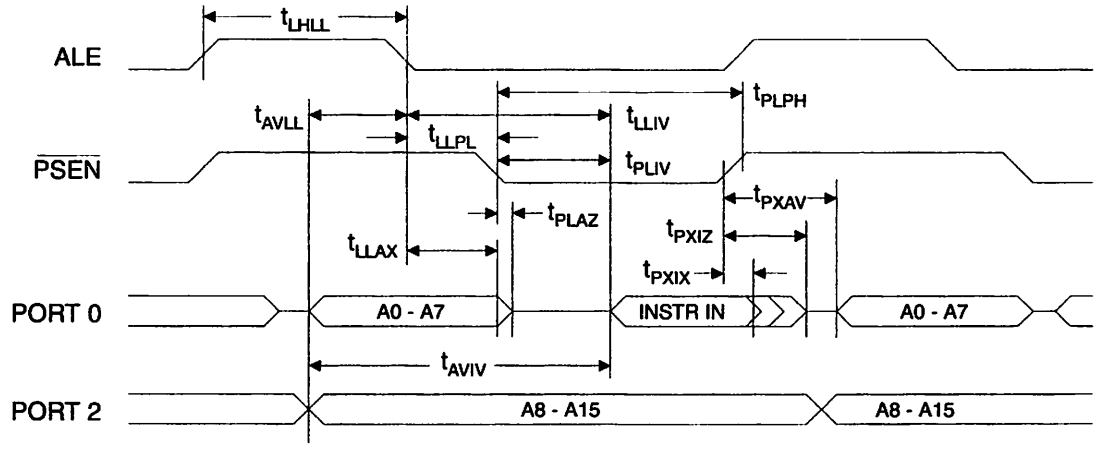
C Characteristics

der operating conditions, load capacitance for Port 0, ALE/$\overline{PROG}$, and $\overline{PSEN}$ = 100 pF; load capacitance for all other tputs = 80 pF.

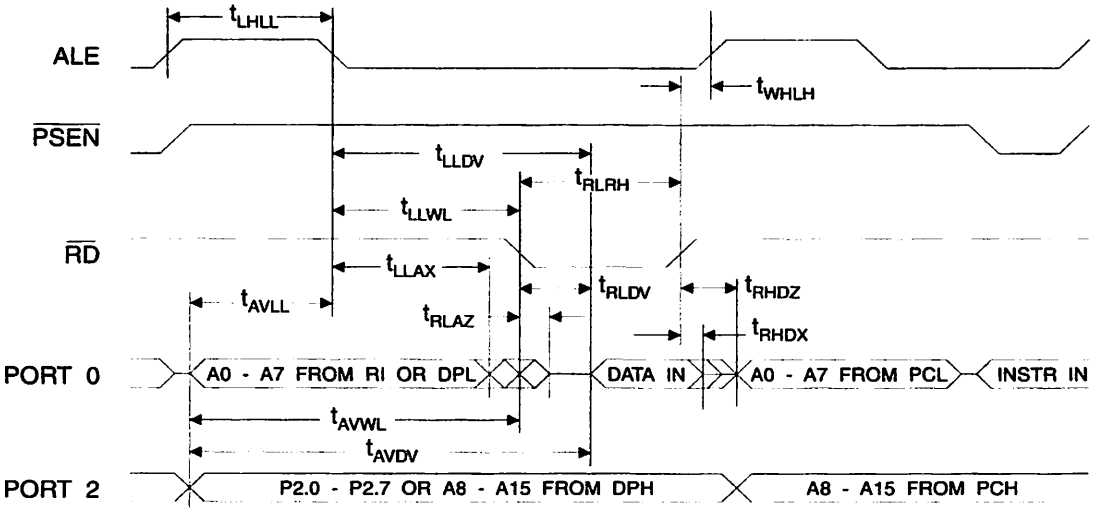
kternal Program and Data Memory Characteristics

ymbol	Parameter	12 MHz Oscillator		16 to 24 MHz Oscillator		Units
		Min	Max	Min	Max	
t_{CLCL}	Oscillator Frequency			0	24	MHz
HLL	ALE Pulse Width	127		$2t_{CLCL}$-40		ns
VLL	Address Valid to ALE Low	43		t_{CLCL}-13		ns
LAX	Address Hold After ALE Low	48		t_{CLCL}-20		ns
LIV	ALE Low to Valid Instruction In		233		$4t_{CLCL}$-65	ns
LPL	ALE Low to $\overline{PSEN}$ Low	43		t_{CLCL}-13		ns
LPH	$\overline{PSEN}$ Pulse Width	205		$3t_{CLCL}$-20		ns
LIV	$\overline{PSEN}$ Low to Valid Instruction In		145		$3t_{CLCL}$-45	ns
XIX	Input Instruction Hold After $\overline{PSEN}$	0		0		ns
XIZ	Input Instruction Float After $\overline{PSEN}$		59		t_{CLCL}-10	ns
XAV	$\overline{PSEN}$ to Address Valid	75		t_{CLCL}-8		ns
AIV	Address to Valid Instruction In		312		$5t_{CLCL}$-55	ns
LAZ	$\overline{PSEN}$ Low to Address Float		10		10	ns
LRH	$\overline{RD}$ Pulse Width	400		$6t_{CLCL}$-100		ns
WLWH	$\overline{WR}$ Pulse Width	400		$6t_{CLCL}$-100		ns
LDV	$\overline{RD}$ Low to Valid Data In		252		$5t_{CLCL}$-90	ns
HDX	Data Hold After $\overline{RD}$	0		0		ns
HDZ	Data Float After $\overline{RD}$		97		$2t_{CLCL}$-28	ns
LDV	ALE Low to Valid Data In		517		$8t_{CLCL}$-150	ns
AVDV	Address to Valid Data In		585		$9t_{CLCL}$-165	ns
LWL	ALE Low to $\overline{RD}$ or $\overline{WR}$ Low	200	300	$3t_{CLCL}$-50	$3t_{CLCL}$+50	ns
AVWL	Address to $\overline{RD}$ or $\overline{WR}$ Low	203		$4t_{CLCL}$-75		ns
QVWX	Data Valid to $\overline{WR}$ Transition	23		t_{CLCL}-20		ns
QVWH	Data Valid to $\overline{WR}$ High	433		$7t_{CLCL}$-120		ns
WHQX	Data Hold After $\overline{WR}$	33		t_{CLCL}-20		ns
RLAZ	$\overline{RD}$ Low to Address Float		0		0	ns
WHLH	$\overline{RD}$ or $\overline{WR}$ High to ALE High	43	123	t_{CLCL}-20	t_{CLCL}+25	ns

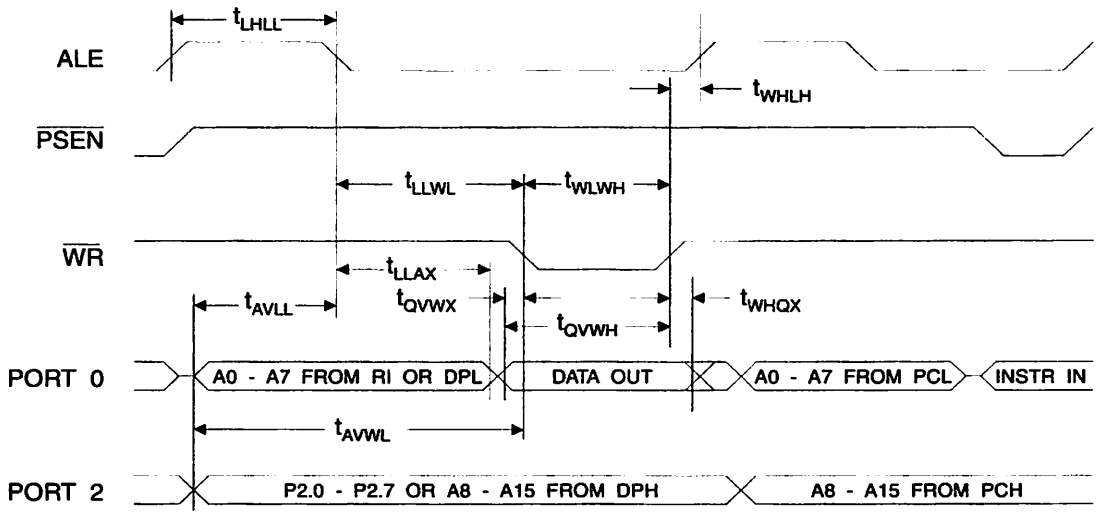
xternal Program Memory Read Cycle



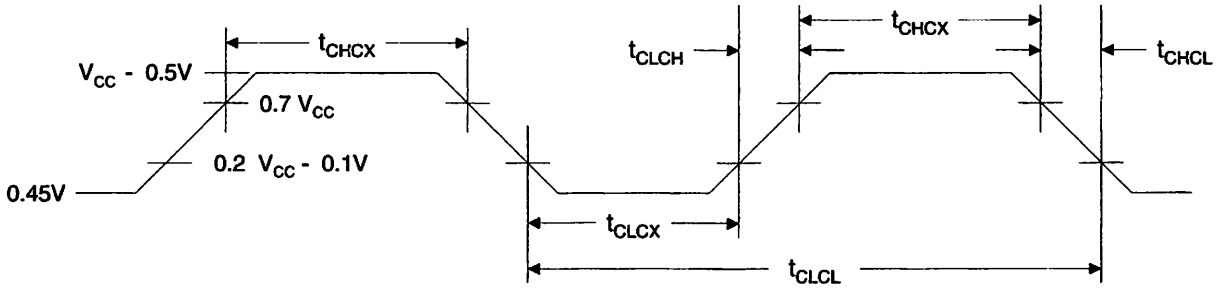
xternal Data Memory Read Cycle



ĸternal Data Memory Write Cycle



ĸternal Clock Drive Waveforms



ĸternal Clock Drive

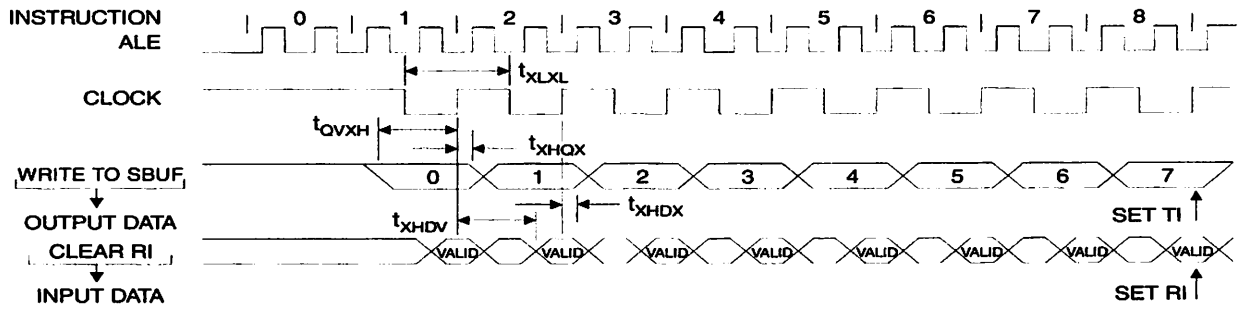
ymbol	Parameter	Min	Max	Units
f_{CLCL}	Oscillator Frequency	0	24	MHz
:LCL	Clock Period	41.6		ns
:HCX	High Time	15		ns
:LCX	Low Time	15		ns
:LCH	Rise Time		20	ns
:HCL	Fall Time		20	ns

erial Port Timing: Shift Register Mode Test Conditions

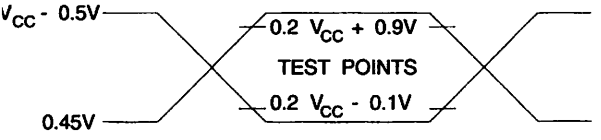
$_{CC}$ = 5.0 V ± 20%; Load Capacitance = 80 pF)

ymbol	Parameter	12 MHz Osc		Variable Oscillator		Units
		Min	Max	Min	Max	
LXL	Serial Port Clock Cycle Time	1.0		$12t_{CLCL}$		µs
IVXH	Output Data Setup to Clock Rising Edge	700		$10t_{CLCL}$-133		ns
HQX	Output Data Hold After Clock Rising Edge	50		$2t_{CLCL}$-117		ns
HDX	Input Data Hold After Clock Rising Edge	0		0		ns
HDV	Clock Rising Edge to Input Data Valid		700		$10t_{CLCL}$-133	ns

ıift Register Mode Timing Waveforms

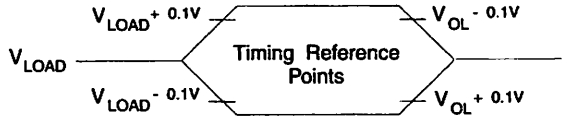


C Testing Input/Output Waveforms[1]



te: 1. AC Inputs during testing are driven at V_{CC} - 0.5V for a logic 1 and 0.45V for a logic 0. Timing measurements are made at V_{IH} min. for a logic 1 and V_{IL} max. for a logic 0.

Float Waveforms[1]



Note: 1. For timing purposes, a port pin is no longer floating when a 100 mV change from load voltage occurs. A port pin begins to float when 100 mV change from the loaded V_{OH}/V_{OL} level occurs.

ChipCorder
TECHNOLOGY BY ISD

ISD2560/75/90/120 Products

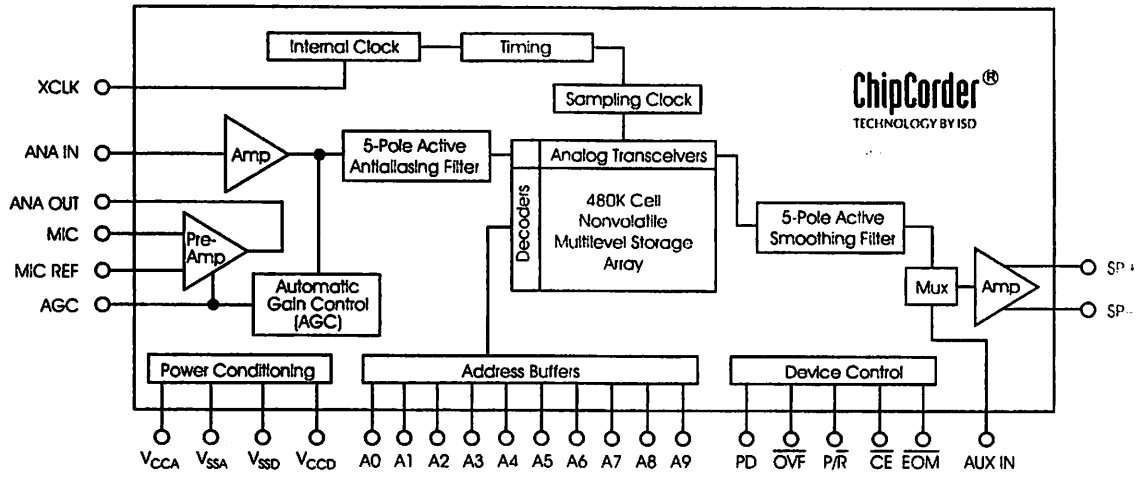
Single-Chip Voice Record/Playback Devices
60-, 75-, 90-, and 120-Second Durations

GENERAL DESCRIPTION

Information Storage Devices' ISD2500 ChipCorder® Series provides high-quality, single-chip record/playback solutions for 60- to 120-second messaging applications. The CMOS devices include an on-chip oscillator, microphone preamplifier, automatic gain control, antialiasing filter, smoothing filter, speaker amplifier, and high density multilevel storage array. In addition, the ISD2500 is microcontroller compatible, allowing complex messaging and addressing to be achieved.

Recordings are stored in on-chip nonvolatile memory cells, providing zero-power message storage. This unique, single-chip solution is made possible through ISD's patented multilevel storage technology. Voice and audio signals are stored directly into memory in their natural form, providing high-quality, solid-state voice reproduction.

Figure i: ISD2560/75/90/120 Device Block Diagram



FEATURES

- Easy-to-use single-chip voice record/playback solution
- High-quality, natural voice/audio reproduction
- Manual switch or microcontroller compatible playback can be edge- or level-activated
- Single-chip durations of 60, 75, 90, and 120 seconds
- Directly cascadable for longer durations
- Automatic Power-Down (Push-Button Mode)
  - Standby current 1 μA (typical)
- Zero-power message storage
  - Eliminates battery backup circuits
- Fully addressable to handle multiple messages
- 100-year message retention (typical)
- 100,000 record cycles (typical)
- On-chip clock source
- Programmer support for play-only applications
- Single +5 volt power supply
- Available in die form, DIP, and TSOP packaging
- Industrial temperature (–40°C to +85°C) versions available

Table i: ISD2560/75/90/120 Product Summary

Part Number	Duration (Seconds)	Input Sample Rate (KHz)	Typical Filter Pass Band (KHz)
ISD2560	60	8.0	3.4
ISD2575	75	6.4	2.7
ISD2590	90	5.3	2.3
ISD25120	120	4.0	1.7

DETAILED DESCRIPTION

SPEECH/SOUND QUALITY

The ISD2500 series includes devices offered at 4.0, 5.3, 6.4, and 8.0 KHz sampling frequencies, allowing the user a choice of speech quality options. Increasing the duration within a product series decreases the sampling frequency and bandwidth, which affects sound quality. Please refer to the ISD2560/75/90/120 Product Summary table on page *ii* to compare filter pass band and product durations.

The speech samples are stored directly into on-chip nonvolatile memory without the digitization and compression associated with other solutions. Direct analog storage provides a very true, natural sounding reproduction of voice, music, tones, and sound effects not available with most solid-state digital solutions.

DURATION

To meet end system requirements, the ISD2500 series offers single-chip solutions at 60, 75, 90, and 120 seconds. Parts may also be cascaded together for longer durations.

EEPROM STORAGE

One of the benefits of ISD's ChipCorder technology is the use of on-chip nonvolatile memory, providing zero-power message storage. The message is retained for up to 100 years typically without power. In addition, the device can be re-recorded typically over 100,000 times.

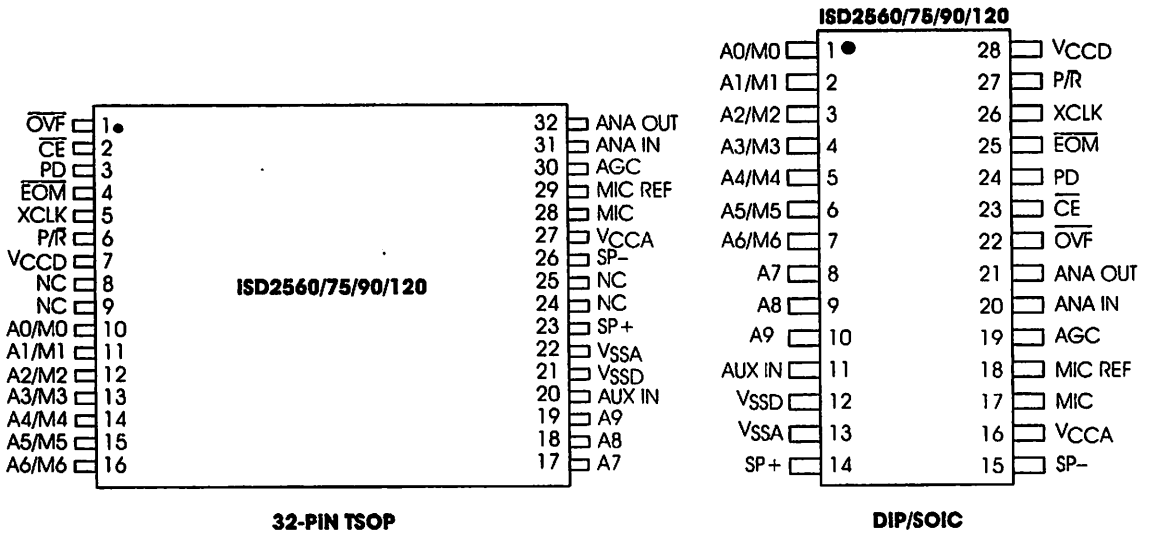
MICROCONTROLLER INTERFACE

In addition to its simplicity and ease of use, the ISD2500 series includes all the interfaces necessary for microcontroller-driven applications. The address and control lines can be interfaced to a microcontroller and manipulated to perform a variety of tasks, including message assembly, message concatenation, predefined fixed message segmentation, and message management.

PROGRAMMING

The ISD2500 series is also ideal for playback-only applications, where single or multiple messages are referenced through buttons, switches, or a microcontroller. Once the desired message configuration is created, duplicates can easily be generated via an ISD programmer.

Figure 1: ISD2560/75/90/120 Device Pinouts



PIN DESCRIPTIONS

VOLTAGE INPUTS (V_{CCA}, V_{CCD})

To minimize noise, the analog and digital circuits in the ISD2500 series devices use separate power busses. These voltage busses are brought out to separate pins and should be tied together as close to the supply as possible. In addition, these supplies should be decoupled as close to the package as possible.

GROUND INPUTS (V_{SSA}, V_{SSD})

The ISD2500 series of devices utilizes separate analog and digital ground busses. These pins should be connected separately through a low-impedance path to power supply ground.

POWER DOWN INPUT (PD)

When not recording or playing back, the PD pin should be pulled HIGH to place the part in a very low power mode (see I_{SB} specification). When overflow ($\overline{OVF}$) pulses LOW for an overflow condition, PD should be brought HIGH to reset the address pointer back to the beginning of the record/playback space. The PD pin has additional functionality in the M6 (Push-Button) Operational Mode described later in the Operational Mode section.

CHIP ENABLE INPUT ($\overline{CE}$)

The $\overline{CE}$ pin is taken LOW to enable all playback and record operations. The address inputs and playback/record input (P/$\overline{R}$) are latched by the falling edge of $\overline{CE}$. $\overline{CE}$ has additional functionality in the M6 (Push-Button) Operational Mode described later in the Operational Mode section.

PLAYBACK/RECORD INPUT (P/$\overline{R}$)

The P/$\overline{R}$ input is latched by the falling edge of the $\overline{CE}$ pin. A HIGH level selects a playback cycle while a LOW level selects a record cycle. For a record cycle, the address inputs provide the starting address and recording continues until PD or $\overline{CE}$ is pulled HIGH or an overflow is detected (i.e. the chip is full). When a record cycle is terminated by pulling PD or $\overline{CE}$ HIGH, an End-Of-Message ($\overline{EOM}$) marker is stored at the current address in memory. For a playback cycle, the address inputs provide the starting address and the device will play until an $\overline{EOM}$ marker is encountered. The device can continue past an $\overline{EOM}$ marker in an Operational Mode, or if $\overline{CE}$ is held LOW in address mode. (See page 5 for more Operational Modes).

END-OF-MESSAGE / RUN OUTPUT ($\overline{EOM}$)

A nonvolatile marker is automatically inserted at the end of each recorded message. It remains there until the message is recorded over. The $\overline{EOM}$ output pulses LOW for a period of T_{EOM} at the end of each message.

In addition, the ISD2500 series has an internal V_{CC} detect circuit to maintain message integrity should V_{CC} fall below 3.5 V. In this case, $\overline{EOM}$ goes LOW and the device is fixed in playback-only mode.

When the device is configured in Operational Mode M6 (Push-Button Mode), this pin provides an active-HIGH RUN signal, indicating the device is currently recording or playing. This signal can conveniently drive an LED for a visual indicator of a record or playback operation in process.

OVERFLOW OUTPUT ($\overline{OVF}$)

This signal pulses LOW at the end of memory space, indicating the device has been filled and the message has overflowed. The $\overline{OVF}$ output then follows the $\overline{CE}$ input until a PD pulse has reset the device. This pin can be used to cascade several ISD2500 devices together to increase record/playback durations.

MICROPHONE INPUT (MIC)

The microphone input transfers its signal to the on-chip preamplifier. An on-chip Automatic Gain Control (AGC) circuit controls the gain of this preamplifier from –15 to 24 dB. An external microphone should be AC coupled to this pin via a series capacitor. The capacitor value, together with the internal 10 KΩ resistance on this pin, determines the low-frequency cutoff for the ISD2500 series passband. See Application Information for additional information on low-frequency cutoff calculation.

MICROPHONE REFERENCE INPUT (MIC REF)

The MIC REF input is the inverting input to the microphone preamplifier. This provides a noise-canceling or common-mode rejection input to the device when connected to a differential microphone.

AUTOMATIC GAIN CONTROL INPUT (AGC)

The AGC dynamically adjusts the gain of the preamplifier to compensate for the wide range of microphone input levels. The AGC allows the full range of whispers to loud sounds to be recorded with minimal distortion. The "attack" time is determined by the time constant of a 5 KΩ internal resistance and an external capacitor (C2 on the schematic on page 18) connected from the AGC pin to V_{SSA} analog ground. The "release" time is determined by the time constant of an external resistor (R2) and an external capacitor (C2) connected in parallel between the AGC Pin and V_{SSA} analog ground. Nominal values of 470 KΩ and 4.7 μF give satisfactory results in most cases.

ANALOG OUTPUT (ANA OUT)

This pin provides the preamplifier output to the user. The voltage gain of the preamplifier is determined by the voltage level at the AGC pin.

ANALOG INPUT (ANA IN)

The analog input pin transfers its signal to the chip for recording. For microphone inputs, the ANA OUT pin should be connected via an external capacitor to the ANA IN pin. This capacitor value, together with the 3.0 KΩ input impedance of ANA IN, is selected to give additional cutoff at the low-frequency end of the voice passband. If the desired input is derived from a source other than a microphone, the signal can be fed, capacitively coupled, into the ANA IN pin directly.

EXTERNAL CLOCK INPUT (XCLK)

The external clock input for the ISD2500 devices has an internal pull-down device. These devices are configured at the factory with an internal sampling clock frequency centered to ±1 percent of specification. The frequency is then maintained to a variation of ±2.25 percent over the entire commercial temperature and operating voltage ranges. The internal clock has a ±5 percent tolerance over the industrial temperature and voltage range. A regulated power supply is recommended for industrial temperature range parts. If greater precision is required, the device can be clocked through the XCLK pin as follows:

Table 1: External Clock Sample Rates

Part Number	Sample Rate	Required Clock
ISD2560	8.0 KHz	1024 KHz
ISD2575	6.4 KHz	819.2 KHz
ISD2590	5.3 KHz	682.7 KHz
ISD25120	4.0 KHz	512 KHz

These recommended clock rates should not be varied because the antialiasing and smoothing filters are fixed, and aliasing problems can occur if the sample rate differs from the one recommended. The duty cycle on the input clock is not critical, as the clock is immediately divided by two. **If the XCLK is not used, this input must be connected to ground.**

SPEAKER OUTPUTS (SP+/SP–)

All devices in the ISD2500 series include an on-chip differential speaker driver, capable of driving 50 mW into 16 Ω from AUX IN (12.2 mW from memory).

The speaker outputs are held at V_{SSA} levels during record and power down. It is therefore not possible to parallel speaker outputs of multiple ISD2500 devices or the outputs of other speaker drivers.

NOTE *Connection of speaker outputs in parallel may cause damage to the device.*

A single output may be used alone (including a coupling capacitor between the SP pin and the speaker). These outputs may be used individually with the output signal taken from either pin. Using the differential outputs results in a 4 to 1 improvement in output power.

NOTE *Never ground or drive an unused speaker output.*

AUXILIARY INPUT (AUX IN)

The Auxiliary input is multiplexed through to the output amplifier and speaker output pins when $\overline{CE}$ is HIGH, P/$\overline{R}$ is HIGH, and playback is currently not active or if the device is in playback overflow. When cascading multiple ISD2500 devices, the AUX IN pin is used to connect a playback signal from a following device to the previous output speaker drivers. For noise considerations, it is suggested that the auxiliary input not be driven when the storage array is active.

ADDRESS/MODE INPUTS (AX/MX)

The Address/Mode inputs have two functions depending on the level of the two Most Significant Bits (MSB) of the address (A8 and A9).

If either or both of the two MSBs are LOW, the inputs are all interpreted as address bits and are used as the start address for the current record or playback cycle. The address pins are inputs only and do not output internal address information as the operation progresses. Address inputs are latched by the falling edge of $\overline{CE}$.

If both MSBs are HIGH, the Address/Mode inputs are interpreted as Mode bits according to the Operational Mode table. There are six Operational Modes (M0..M6) available as indicated in the table. It is possible to use multiple Operational Modes simultaneously. Operational Modes are sampled on each falling edge of $\overline{CE}$, and thus Operational Modes and direct addressing are mutually exclusive.

OPERATIONAL MODES

The ISD2500 series is designed with several built-in Operational Modes that provide maximum functionality with minimum additional components. These are described in detail below. The Operational Modes use the address pins on the ISD2500 devices, but are mapped outside the valid address range. When the two Most Significant Bits (MSBs) are HIGH (A8 and A9), the remaining address signals are interpreted as mode bits and not as address bits. Therefore, Operational Modes and direct addressing are not compatible and cannot be used simultaneously.

There are two important considerations for using Operational Modes. First, all operations begin initially at address 0, which is the beginning of the ISD2500 address space. Later operations can begin at other address locations, depending on the Operational Mode(s) chosen. In addition, the address pointer is reset to 0 when the device is changed from record to playback, playback to record (except M6 mode), or when a Power-Down cycle is executed.

Second, Operational Modes are executed when $\overline{CE}$ goes LOW and the two MSBs are HIGH. This Operational Mode remains in effect until the next LOW-going $\overline{CE}$ signal, at which point the current address/mode levels are sampled and executed.

Table 2: Operational Modes Table

Mode Control	Function	Typical Use	Jointly Compatible[1]
M0	Message cueing	Fast-forward through messages	M4, M5, M6
M1	Delete $\overline{EOM}$ markers	Position $\overline{EOM}$ marker at the end of the last message	M3, M4, M5, M6
M2	Not applicable	Reserved	N/A
M3	Looping	Continuous playback from Address 0	M1, M5, M6
M4	Consecutive addressing	Record/play multiple consecutive messages	M0, M1, M5
M5	$\overline{CE}$ level-activated	Allows message pausing	M0, M1, M3, M4
M6	Push-button control	Simplified device interface	M0, M1, M3

1. Additional Operational Modes can be used simultaneously with the given mode.

OPERATIONAL MODES DESCRIPTION

The Operational Modes can be used in conjunction with a microcontroller, or they can be hardwired to provide the desired system operation.

M0 — MESSAGE CUEING

Message Cueing allows the user to skip through messages, without knowing the actual physical addresses of each message. Each $\overline{CE}$ LOW pulse causes the internal address pointer to skip to the next message. This mode should be used for playback only, and is typically used with the M4 Operational Mode.

M1 — DELETE $\overline{EOM}$ MARKERS

The M1 Operational Mode allows sequentially recorded messages to be combined into a single message with only one $\overline{EOM}$ marker set at the end of the final message. When this Operational Mode is configured, messages recorded sequentially are played back as one continuous message.

M2 — UNUSED

When Operational Modes are selected, the M2 pin should be LOW.

M3 — MESSAGE LOOPING

The M3 Operational Mode allows for the automatic, continuously repeated playback of the message located at the beginning of the address space. A message can completely fill the ISD2500 device and will loop from beginning to end without $\overline{OVF}$ going LOW.

M4 — CONSECUTIVE ADDRESSING

During normal operations, the address pointer will reset when a message is played through to an $\overline{EOM}$ marker. The M4 Operational Mode inhibits the address pointer reset on $\overline{EOM}$, allowing messages to be played back consecutively.

M5 — $\overline{CE}$-LEVEL ACTIVATED

The default mode for ISD2500 devices is for $\overline{CE}$ to be edge-activated on playback and level-activated on record. The M5 Operational Mode causes the $\overline{CE}$ pin to be interpreted as level-activated as opposed to edge-activated during playback. This is specifically useful for terminating playback operations using the $\overline{CE}$ signal.

In this mode, $\overline{CE}$ LOW begins a playback cycle, at the beginning of the device memory. The playback cycle continues as long as $\overline{CE}$ is held LOW. When $\overline{CE}$ goes HIGH, playback will immediately end. A new $\overline{CE}$ LOW will restart the message from the beginning unless M4 is also HIGH.

M6 — PUSH-BUTTON MODE

The ISD2500 series of devices contain a Push-Button Operational Mode. The Push-Button mode is used primarily in very low-cost applications and is designed to minimize external circuitry and components, thereby reducing system cost. In order to configure the device in Push-Button Operational Mode, the two most significant address bits must be HIGH, and the M6 mode pin must also be HIGH. A device in this mode always powers down at the end of each playback or record cycle after $\overline{CE}$ goes HIGH.

When this Operational Mode is implemented, several of the pins on the device have alternate functionality:

Table 3: Alternate Functionality in Pins

Pin Name	Alternate Functionality in Push-Button Mode
$\overline{CE}$	Start/Pause Push-Button (LOW pulse-activated)
PD	Stop/Reset Push-Button (HIGH pulse activated)
$\overline{EOM}$	Active-HIGH Run Indicator

$\overline{CE}$ PIN (START/PAUSE)

In Push-Button Operational Mode, $\overline{CE}$ acts as a LOW-going pulse-activated START/PAUSE signal. If no operation is currently in progress, a LOW-going pulse on this signal will initiate a playback or a record cycle according to the level on the P/$\overline{R}$ pin. A subsequent pulse on the $\overline{CE}$ pin, before an End-Of-Message is reached in playback or an overflow condition occurs, will cause the device to pause. The address counter is not reset, and another $\overline{CE}$ pulse will cause the device to continue the operation from the place where it was paused.

PD PIN (STOP/RESET)

In push-button Operational Mode, PD acts as a HIGH-going pulse-activated STOP/RESET signal. When a playback or record cycle is in progress and a HIGH-going pulse is observed on PD, the current cycle is terminated and the address pointer is reset to address 0, the beginning of the message space.

$\overline{EOM}$ PIN (RUN)

In Push-Button Operational Mode, $\overline{EOM}$ becomes an active-HIGH RUN signal which can be used to drive an LED or other external device. It is HIGH whenever a record or playback operation is in progress.

Recording in Push-Button Mode

1. The PD pin should be LOW, usually using a pull-down resistor.
2. The P/$\overline{R}$ pin is taken LOW.
3. The $\overline{CE}$ pin is pulsed LOW. Recording starts, $\overline{EOM}$ goes HIGH to indicate an operation in progress.
4. The $\overline{CE}$ pin is pulsed LOW. Recording pauses, $\overline{EOM}$ goes back LOW. The internal address pointers are not cleared, but an EOM marker is stored in memory to point to the message end. The P/$\overline{R}$ pin may be taken HIGH at this time. Any subsequent $\overline{CE}$ would start a playback at address 0.
5. The $\overline{CE}$ pin is pulsed LOW. Recording starts at the next address after the previous set EOM marker. $\overline{EOM}$ goes back HIGH.

NOTE *If the M1 Operational Mode pin is also HIGH, the just previously written EOM bit is erased, and recording starts at that address.)*

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6. When the recording sequences are finished, the final $\overline{CE}$ pulse LOW will end the last record cycle, leaving a set $\overline{EOM}$ marker at the message end. Recording may also be terminated by a HIGH level on PD, which will leave a set EOM marker.

Playback in Push-Button Mode

1. The PD pin should be LOW.
2. The P/$\overline{R}$ pin is taken HIGH.
3. The $\overline{CE}$ pin is pulsed LOW. Playback starts, $\overline{EOM}$ goes HIGH to indicate an operation in progress.
4. If the $\overline{CE}$ pin is pulsed LOW or an EOM marker is encountered during an operation, the part will pause. The internal address pointers are not cleared, and $\overline{EOM}$ goes back LOW. The P/$\overline{R}$ pin may be changed at this time. A subsequent record operation would not reset the address pointers and the recording would begin where playback ended.
5. $\overline{CE}$ is again pulsed LOW. Playback starts where it left off, with $\overline{EOM}$ going HIGH to indicate an operation in progress.
6. Playback continues as in steps 4 and 5 until PD is pulsed HIGH or overflow occurs.
7. If in overflow, pulling $\overline{CE}$ LOW will reset the address pointer and start playback from the beginning. After a PD pulse, the part is reset to address 0.

NOTE *Push-button mode can be used in conjunction with modes M0, M1, and M3.*

GOOD AUDIO DESIGN PRACTICES

ISD products are very high-quality single-chip voice recording and playback systems. To ensure the highest quality voice reproduction, it is important that good audio design practices on layout and power supply decoupling be followed. See the ISD Application Notes in this book for details.

ISD1000A COMPATIBILITY

The ISD2500 series of devices is designed to provide upward compatibility with the ISD1000A family. When designing with the ISD2500 series, the following differences should be noted.

ADDRESSING

The ISD2560/75/90/120 devices have 480K storage cells designed to provide 60 seconds of storage at a sampling rate of 8.0 KHz. This is approximately four times the storage of the ISD1000A family. To enable the same addressing resolution, two additional address pins have been added. The address space of each device is divisible into 600 increments with valid addressing from 00 to 257 Hex. Some higher addresses are mapped into the Operational Modes. All other addresses are invalid.

OVERFLOW

The ISD1000A series combined two functions on the $\overline{EOM}$ pin: end-of-message indication and overflow. The ISD2500 separates these two functions. Pin 25 (PDIP package) remains as $\overline{EOM}$, but outputs only the EOM signal indication. Pin 22 (PDIP package) becomes $\overline{OVF}$ and pulses LOW only when the device reaches its end of memory, or is "full." This change allows easy message cueing and addressability across device boundaries. This also means that the M2 Operational Mode found in the ISD1000A family is not implemented in the ISD2500 series.

PUSH-BUTTON MODE

The ISD2500 series includes an additional Operational Mode called Push-Button mode. This provides an alternative interface to the record and playback functions of the part. The $\overline{CE}$ and PD pins become redefined as edge-activated "push-buttons." A pulse on $\overline{CE}$ initiates a cycle, and if triggered again, pauses the current cycle without resetting the address pointer (i.e., a Start or Pause function). PD stops any current cycle and resets the address pointer to the beginning of the message space (i.e., a Stop and Reset function). Additionally, the $\overline{EOM}$ pin functions as an active-HIGH run indicator, and can be used to drive an LED indicating a record or playback operation is in progress. Devices in the Push-Button mode cannot be cascaded.

LOOPING MODE

The ISD2500 series can loop with a message that completely fills the memory space.

NOTE *Additional descriptions of ISD2500 device functionality and application examples are provided in the ISD Application Notes in this book.*

TIMING DIAGRAMS

Figure 2: Record

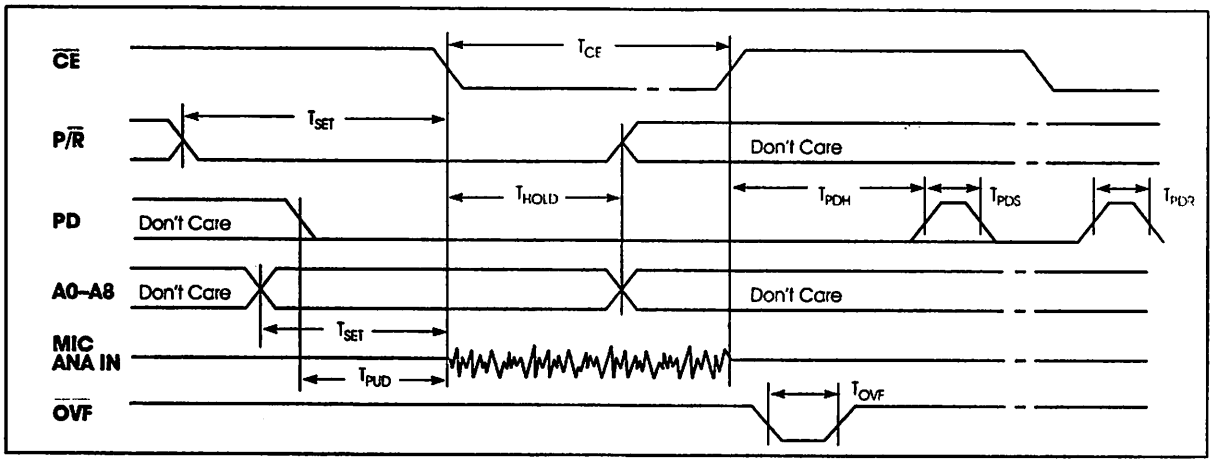


Figure 3: Playback

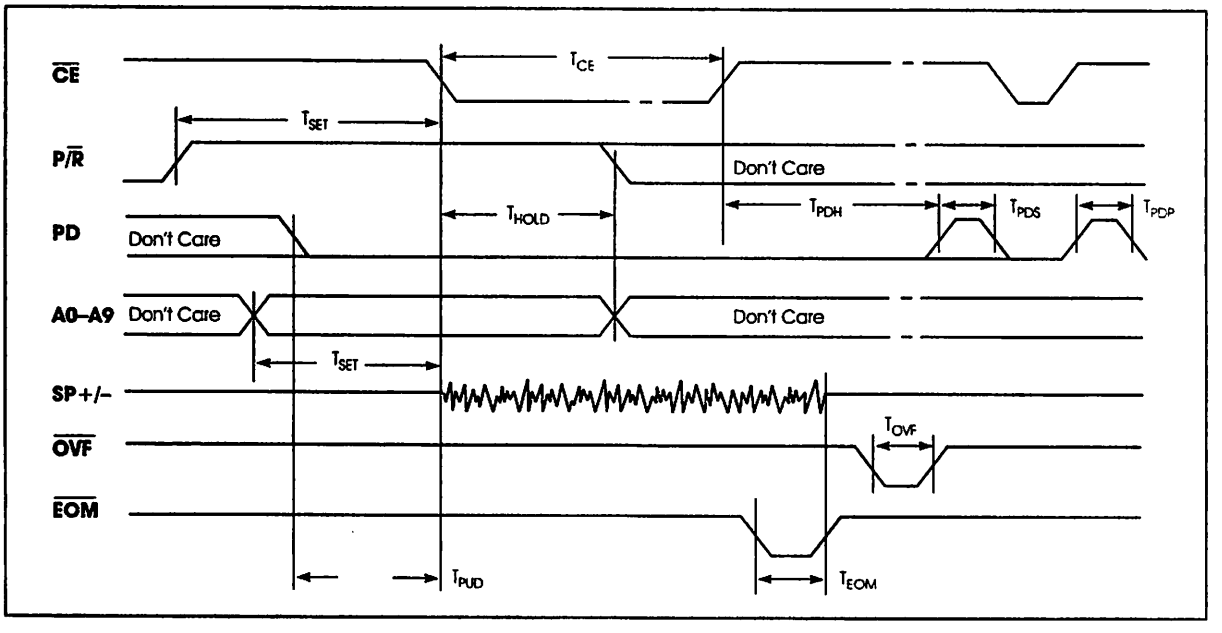


Table 4: Absolute Maximum Ratings (Packaged Parts)[1]

Condition	Value
Junction temperature	150°C
Storage temperature range	–65°C to +150°C
Voltage applied to any pin	(V_{SS} – 0.3 V) to (V_{CC} + 0.3 V)
Voltage applied to any pin (Input current limited to ±20 mA)	(V_{SS} – 1.0 V) to (V_{CC} + 1.0 V)
Lead temperature (soldering – 10 seconds)	300°C
V_{CC} – V_{SS}	–0.3 V to +7.0 V

1. *Stresses above those listed may cause permanent damage to the device. Exposure to the absolute maximum ratings may affect device reliability. Functional operation is not implied at these conditions.*

Table 5: Operating Conditions (Packaged Parts)

Condition	Value
Commercial operating temperature range[1]	0°C to +70°C
Industrial operating temperature range[1]	–40°C to +85°C
Supply voltage (V_{CC})[2]	+4.5 V to +5.5 V
Ground voltage (V_{SS})[3]	0 V

1. *Case temperature.*
2. $V_{CC} = V_{CCA} = V_{CCD}$.
3. $V_{SS} = V_{SSA} = V_{SSD}$.

Table 6: DC Parameters (Packaged Parts)

Symbol	Parameters	Min[2]	Typ [1]	Max[2]	Units	Conditions
V_{IL}	Input Low Voltage			0.8	V	
V_{IH}	Input High Voltage	2.0			V	
V_{OL}	Output Low Voltage			0.4	V	I_{OL} = 4.0 mA
V_{OH}	Output High Voltage	V_{CC} – 0.4			V	I_{OH} = –10 µA
V_{OH1}	$\overline{OVF}$ Output High Voltage	2.4			V	I_{OH} = –1.6 mA
V_{OH2}	$\overline{EOM}$ Output High Voltage	V_{CC} – 1.0	V_{CC} – 0.8		V	I_{OH} = –3.2 mA
I_{CC}	V_{CC} Current (Operating)		25	30	mA	$R_{EXT} = \infty$ [3]
I_{SB}	V_{CC} Current (Standby)		1	10	µA	[3]
I_{IL}	Input Leakage Current			±1	µA	
I_{ILPD}	Input Current HIGH with Pull Down			130	µA	Force V_{CC} [4]
R_{EXT}	Output Load Impedance	16			Ω	Speaker Load
R_{MIC}	Preamp In Input Resistance	4	9	15	KΩ	MIC and MIC REF Pins
R_{AUX}	AUX INPUT Resistance	5	11	20	KΩ	

Table 6: DC Parameters (Packaged Parts)

Symbol	Parameters	Min(2)	Typ (1)	Max(2)	Units	Conditions
$R_{ANA\ IN}$	ANA IN Input Resistance	2.3	3	5	KΩ	
A_{PRE1}	Preamp Gain 1	21	24	26	dB	AGC = 0.0 V
A_{PRE2}	Preamp Gain 2		-15	5	dB	AGC = 2.5 V
A_{AUX}	AUX IN/SP+ Gain		0.98	1.0	V/V	
A_{ARP}	ANA IN to SP+/- Gain	21	23	26	dB	
R_{AGC}	AGC Output Resistance	2.5	5	9.5	KΩ	

1. *Typical values @ T_A = 25°C and 5.0 V.*
2. *All Min/Max limits are guaranteed by ISD via electrical testing or characterization. Not all specifications are 100 percent tested.*
3. *V_{CCA} and V_{CCD} connected together.*
4. *XCLK pin only.*

Table 7: AC Parameters (Packaged Parts)

Symbol	Characteristic		Min(2)	Typ (1)	Max(2)	Units	Conditions
F_S	Sampling Frequency	ISD2560		8.0		KHz	(7)
		ISD2575		6.4		KHz	(7)
		ISD2590		5.3		KHz	(7)
		ISD25120		4.0		KHz	(7)
F_{CF}	Filter Pass Band	ISD2560		3.4		KHz	3 dB Roll-Off Point (3) (8)
		ISD2575		2.7		KHz	3 dB Roll-Off Point (3) (8)
		ISD2590		2.3		KHz	3 dB Roll-Off Point (3) (8)
		ISD25120		1.7		KHz	3 dB Roll-Off Point (3) (8)
T_{REC}	Record Duration	ISD2560	58.1	60.0	62.0	sec	Commercial Operation(7)
		ISD2560	56.5	60.0	63.8	sec	Industrial Operation(7)
		ISD2575	72.6	75.0	77.5	sec	Commercial Operation(7)
		ISD2575	70.7	75.0	79.7	sec	Industrial Operation(7)
		ISD2590	87.1	90.0	93.0	sec	Commercial Operation(7)
		ISD25120	116.1	120.0	123.9	sec	Commercial Operation(7)
T_{PLAY}	Playback Duration	ISD2560	58.1	60.0	62.0	sec	Commercial Operation
		ISD2560	56.5	60.0	63.8	sec	Industrial Operation
		ISD2575	72.6	75.0	77.5	sec	Commercial Operation
		ISD2575	70.7	75.0	79.7	sec	Industrial Operation
		ISD2590	87.1	90.0	93.0	sec	Commercial Operation
		ISD25120	116.1	120.0	123.9	sec	Commercial Operation
T_{CE}	$\overline{CE}$ Pulse Width			100		nsec	
T_{SET}	Control/Address Setup Time			300		nsec	
T_{HOLD}	Control/Address Hold Time			0		nsec	

Table 7: AC Parameters (Packaged Parts)

Symbol	Characteristic		Min[2]	Typ [1]	Max[2]	Units	Conditions
T_{PUD}	Power-Up Delay	ISD2560	24.1	25.0	27.8	msec	Commercial Operation
		ISD2560	23.5		28.5	msec	Industrial Operation
		ISD2575	30.2	31.3	34.3	msec	Commercial Operation
		ISD2575	29.3	31.3	35.2	msec	Industrial Operation
		ISD2590	36.2	37.5	40.8	msec	Commercial Operation
		ISD25120	48.2	50.0	53.6	msec	Commercial Operation
T_{PDR}	PD Pulse Width Record	ISD2560		25		msec	
		ISD2575		31.25		msec	
		ISD2590		37.5		msec	
		ISD25120		50.0		msec	
T_{PDP}	PD Pulse Width Play	ISD2560		12.5		msec	
		ISD2575		15.625		msec	
		ISD2590		18.75		msec	
		ISD25120		25.0		msec	
T_{PDS}	PD Pulse Width Static			100		nsec	[6]
T_{PDH}	Power Down Hold			0		nsec	
T_{EOM}	$\overline{EOM}$ Pulse Width	ISD2560		12.5		msec	
		ISD2575		15.625		msec	
		ISD2590		18.75		msec	
		ISD25120		25.0		msec	
T_{OVF}	Overflow Pulse Width			6.5		µsec	
THD	Total Harmonic Distortion			1	2	%	@ 1 KHz
P_{OUT}	Speaker Output Power			12.2	50	mW	R_{EXT} = 16 Ω [4]
V_{OUT}	Voltage Across Speaker Pins				2.5	V p-p	R_{EXT} = 600 Ω
V_{IN1}	MIC Input Voltage				20	mV	Peak-to-Peak [5]
V_{IN2}	ANA IN Input Voltage				50	mV	Peak-to-Peak
V_{IN3}	Aux Input Voltage				1.25	V	Peak-to-Peak; R_{EXT} = 16 Ω

1. *Typical values @ T_A = 25°C and 5.0 V.*
2. *All Min/Max limits are guaranteed by ISD via electrical testing or characterization. Not all specifications are 100 percent tested.*
3. *Low-frequency cutoff depends upon the value of external capacitors (see Pin Descriptions).*
4. *From AUX IN; if ANA IN is driven at 50 mV p-p, the P_{OUT} = 12.2 mW, typical.*
5. *With 5.1 KΩ series resistor at ANA IN.*
6. *T_{PDS} is required during a static condition, typically overflow.*
7. *Sampling Frequency and playback Duration can vary as much as ±2.25 percent over the commercial temperature range and voltage range and ±5 percent over the industrial temperature and voltage range. For greater stability, an external clock can be utilized (see Pin Descriptions).*
8. *Filter specification applies to both the antialiasing filter and the smoothing filter. Therefore, from input to output, expect a 6 dB drop by nature of passing through both filters.*

TYPICAL PARAMETER VARIATION WITH VOLTAGE AND TEMPERATURE (PACKAGED PARTS)

Chart 1: Record Mode Operating Current (I_{CC})

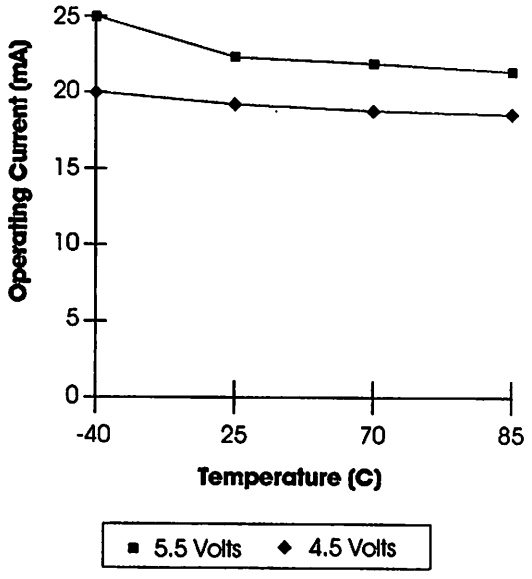


Chart 3: Standby Current (I_{SB})

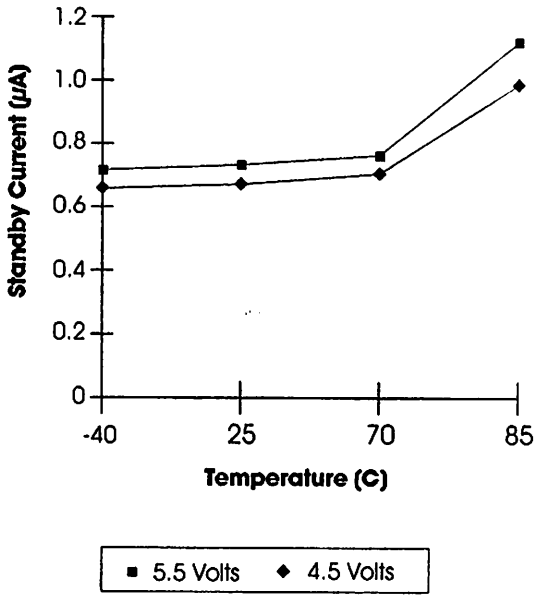


Chart 2: Total Harmonic Distortion

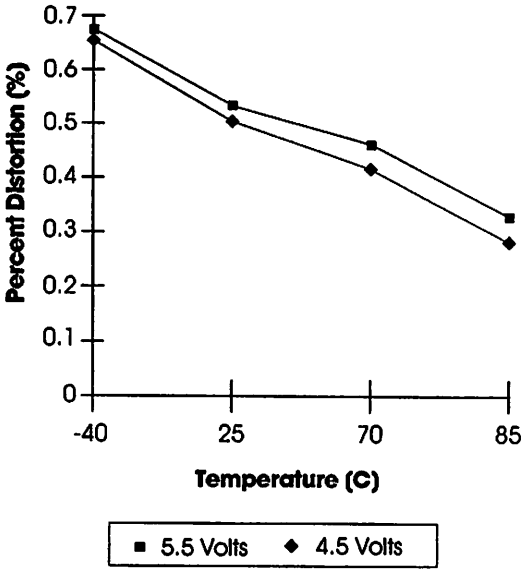


Chart 4: Oscillator Stability

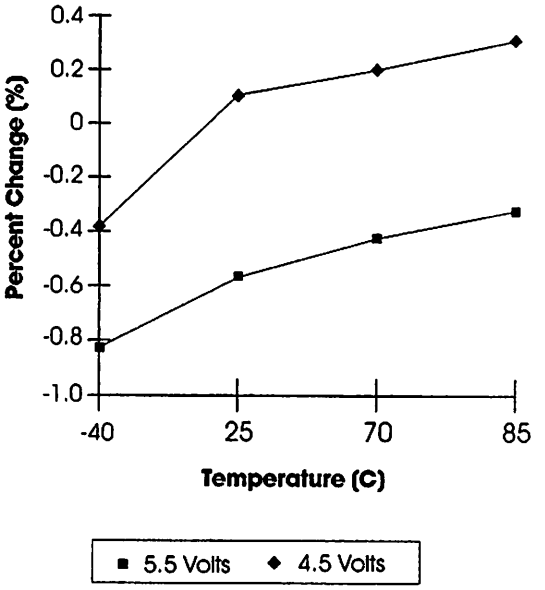


Table 8: Absolute Maximum Ratings (Die)[1]

Condition	Value
Junction temperature	150°C
Storage temperature range	–65°C to +150°C
Voltage applied to any pad	(V_{SS} – 0.3 V) to (V_{CC} + 0.3 V)
Voltage applied to any pad (Input current limited to ±20 mA)	(V_{SS} –1.0 V) to (V_{CC} + 1.0 V)
$V_{CC} - V_{SS}$	–0.3 V to +7.0 V

1. *Stresses above those listed may cause permanent damage to the device. Exposure to the absolute maximum ratings may affect device reliability. Functional operation is not implied at these conditions.*

Table 9: Operating Conditions (Die)

Condition	Value
Commercial operating temperature range	0°C to +50°C
Supply voltage (V_{CC})[1]	+4.5 V to +6.5 V
Ground voltage (V_{SS})[2]	0 V

1. $V_{CC} = V_{CCA} = V_{CCD}$.
2. $V_{SS} = V_{SSA} = V_{SSD}$.

Table 10: DC Parameters (Die)

Symbol	Parameters	Min[2]	Typ [1]	Max[2]	Units	Conditions
V_{IL}	Input Low Voltage			0.8	V	
V_{IH}	Input High Voltage	2.0			V	
V_{OL}	Output Low Voltage			0.4	V	I_{OL} = 4.0 mA
V_{OH}	Output High Voltage	V_{CC} – 0.4			V	I_{OH} = –10 µA
V_{OH1}	$\overline{OVF}$ Output High Voltage	2.4			V	I_{OH} = –1.6 mA
V_{OH2}	$\overline{EOM}$ Output High Voltage	V_{CC} – 1.0	V_{CC} – 0.8		V	I_{OH} = –3.2 mA
I_{CC}	V_{CC} Current (Operating)		25	30	mA	$R_{EXT} = \infty$ [3]
I_{SB}	V_{CC} Current (Standby)		1	10	µA	[2]
I_{IL}	Input Leakage Current			±1	µA	
I_{ILPD}	Input Current HIGH with Pull Down			130	µA	Force V_{CC} [4]
R_{EXT}	Output Load Impedance	16			Ω	Speaker Load
R_{MIC}	Preamp In Input Resistance	4	9	15	KΩ	MIC and MIC REF Pads
R_{AUX}	AUX INput Resistance	5	11	20	KΩ	
$R_{ANA\ IN}$	ANA IN Input Resistance	2.3	3	5	KΩ	
A_{PRE1}	Preamp Gain 1	21	24	26	dB	AGC = 0.0 V

Table 10: DC Parameters (Die)

Symbol	Parameters	Min[2]	Typ [1]	Max[2]	Units	Conditions
A_{PRE2}	Preamp Gain 2		-15	5	dB	AGC = 2.5 V
A_{AUX}	AUX IN/SP+ Gain		0.98	1.0	V/V	
A_{ARP}	ANA IN to SP+/- Gain	21	23	26	dB	
R_{AGC}	AGC Output Resistance	2.5	5	9.5	KΩ	

1. *Typical values @ T_A = 25°C and 5.0 V.*
2. *All Min/Max limits are guaranteed by ISD via electrical testing or characterization. Not all specifications are 100 percent tested.*
3. *V_{CCA} and V_{CCD} connected together.*
4. *XCLK pad only.*

Table 11: AC Parameters (Die)

Symbol	Characteristic		Min[2]	Typ [1]	Max[2]	Units	Conditions
F_S	Sampling Frequency	ISD2560		8.0		KHz	[7]
		ISD2575		6.4		KHz	[7]
		ISD2590		5.3		KHz	[7]
		ISD25120		4.0		KHz	[7]
F_{CF}	Filter Pass Band	ISD2560		3.4		KHz	3 dB Roll-Off Point [3] [8]
		ISD2575		2.7		KHz	3 dB Roll-Off Point [3] [8]
		ISD2590		2.3		KHz	3 dB Roll-Off Point [3] [8]
		ISD25120		1.7		KHz	3 dB Roll-Off Point [3] [8]
T_{REC}	Record Duration	ISD2560	58.1	60.0	62.0	sec	Commercial Operation[7]
		ISD2575	72.6	75.0	77.5	sec	Commercial Operation[7]
		ISD2590	87.1	90.0	93.0	sec	Commercial Operation[7]
		ISD25120	116.1	120.0	123.9	sec	Commercial Operation[7]
T_{PLAY}	Playback Duration	ISD2560	58.1	60.0	62.0	sec	Commercial Operation[7]
		ISD2575	72.6	75.0	77.5	sec	Commercial Operation[7]
		ISD2590	87.1	90.0	93.0	sec	Commercial Operation[7]
		ISD25120	116.1	120.0	123.9	sec	Commercial Operation[7]
T_{CE}	$\overline{CE}$ Pulse Width			100		nsec	
T_{SET}	Control/Address Setup Time			300		nsec	
T_{HOLD}	Control/Address Hold Time			0		nsec	
T_{PUD}	Power-Up Delay	ISD2560	24.1	25.0	27.8	msec	Commercial Operation
		ISD2575	30.2	31.3	34.3	msec	Commercial Operation
		ISD2590	36.2	37.5	40.8	msec	Commercial Operation
		ISD25120	48.2	50.0	53.6	msec	Commercial Operation

Table 11: AC Parameters (Die)

Symbol	Characteristic		Min[2]	Typ [1]	Max[2]	Units	Conditions
T_{PDR}	PD Pulse Width Record	ISD2560		25		msec	
		ISD2575		31.25		msec	
		ISD2590		37.5		msec	
		ISD25120		50.0		msec	
T_{PDP}	PD Pulse Width Play	ISD2560		12.5		msec	
		ISD2575		15.625		msec	
		ISD2590		18.75		msec	
		ISD25120		25.0		msec	
T_{PDS}	PD Pulse Width Static			100		nsec	[6]
T_{PDH}	Power Down Hold			0		nsec	
T_{EOM}	$\overline{EOM}$ Pulse Width	ISD2560		12.5		msec	
		ISD2575		15.625		msec	
		ISD2590		18.75		msec	
		ISD25120		25.0		msec	
T_{OVF}	Overflow Pulse Width			6.5		µsec	
THD	Total Harmonic Distortion			1	3	%	@ 1 KHz
P_{OUT}	Speaker Output Power			12.2	50	mW	R_{EXT} = 16 Ω[4]
V_{OUT}	Voltage Across Speaker Pins				2.5	V p-p	R_{EXT} = 600 Ω
V_{IN1}	MIC Input Voltage				20	mV	Peak-to-Peak [5]
V_{IN2}	ANA IN Input Voltage				50	mV	Peak-to-Peak
V_{IN3}	Aux Input Voltage				1.25	V	Peak-to-Peak; R_{EXT} = 16 Ω

1. *Typical values @ T_A = 25°C and 5.0 V.*
2. *All Min/Max limits are guaranteed by ISD via electrical testing or characterization. Not all specifications are 100 percent tested.*
3. *Low-frequency cutoff depends upon the value of external capacitors (see Pin Descriptions).*
4. *From AUX IN; if ANA IN is driven at 50 mV p-p, the P_{OUT} = 12.2 mW, typical.*
5. *With 5.1 KΩ series resistor at ANA IN.*
6. *T_{PDS} is required during a static condition, typically overflow.*
7. *Sampling Frequency and playback Duration can vary as much as ±2.25 percent over the commercial temperature range and voltage range. For greater stability, an external clock can be utilized (see Pin Descriptions).*
8. *Filter specification applies to the antialiasing filter and the smoothing filter.*

TYPICAL PARAMETER VARIATION WITH VOLTAGE AND TEMPERATURE (DIE)

Chart 5: Record Mode Operating Current (I_{CC})

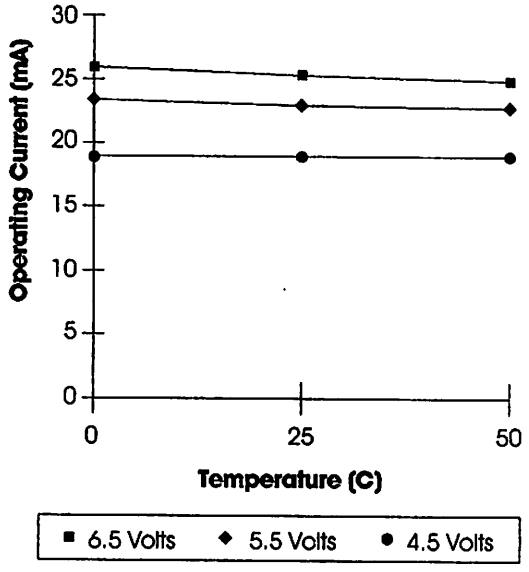


Chart 7: Standby Current (I_{SB})

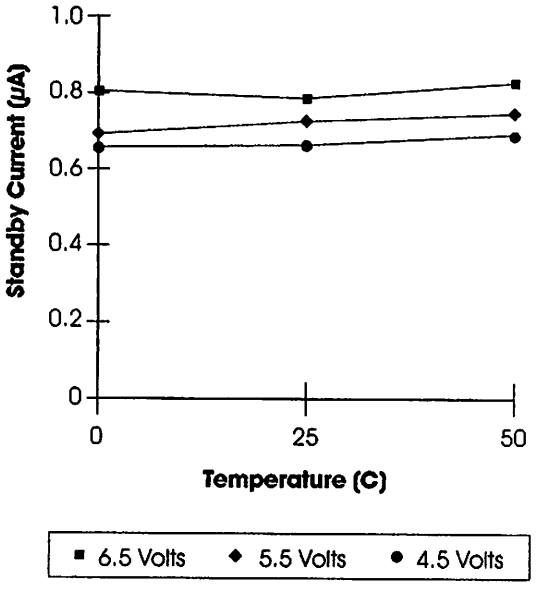


Chart 6: Total Harmonic Distortion

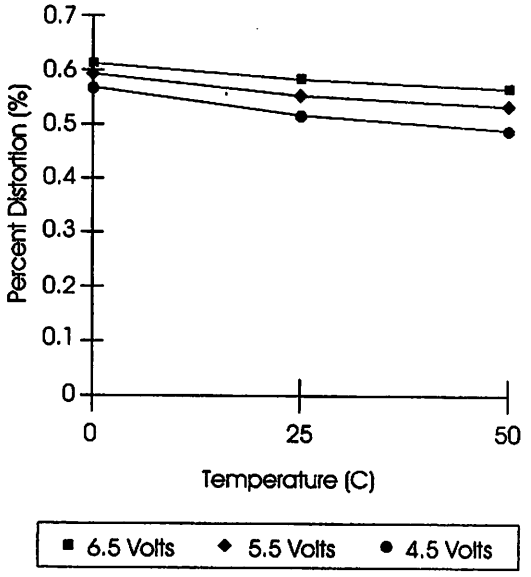


Chart 8: Oscillator Stability

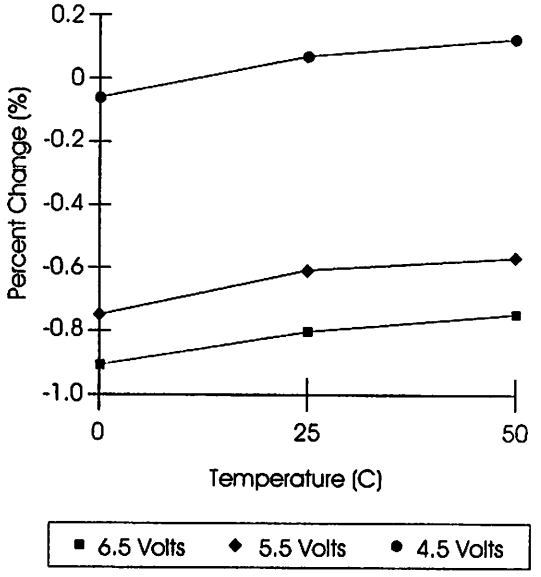
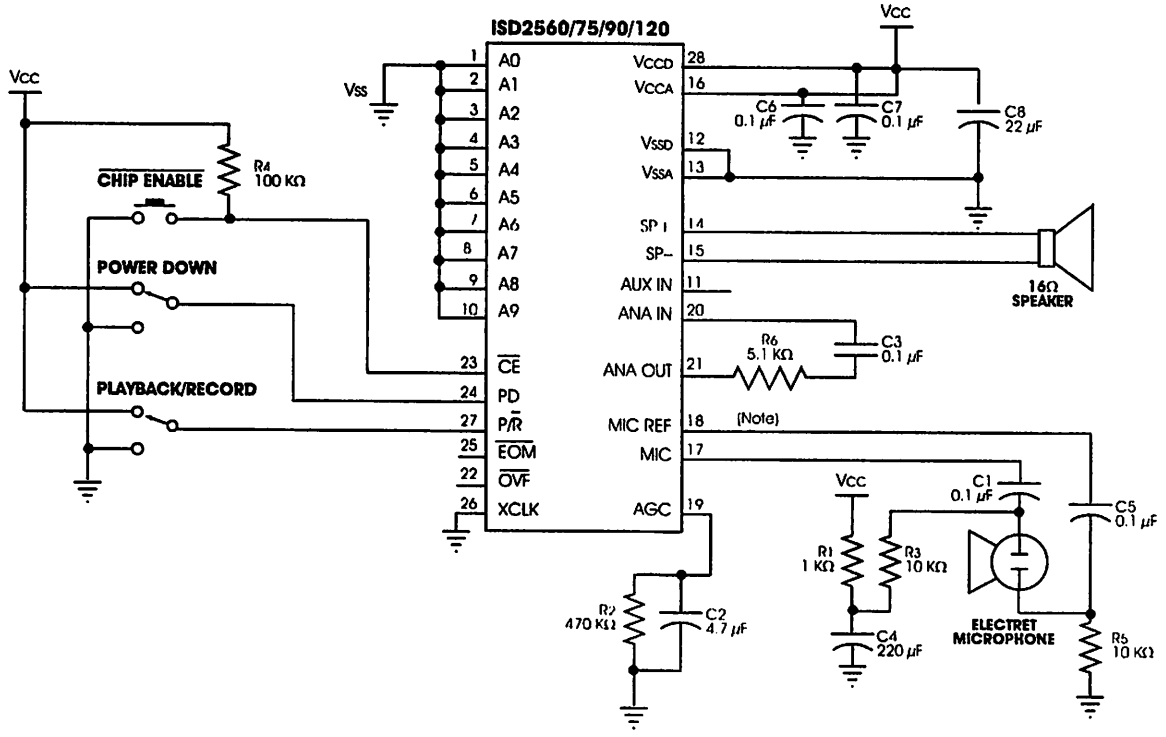


Figure 4: ISD2560/75/90/120 Application Example—Design Schematic



NOTE: *If desired, pin 18 (PDIP package) may be left unconnected (microphone preamplifier noise will be higher). In this case, pin 18 must not be tied to any other signal or voltage. Additional design example schematics are provided in the Application Notes in this book.*

Table 12: Application Example—Basic Device Control

Control Step	Function	Action
1	Power up chip and select record/playback mode	(1.) PD = LOW, (2.) P/$\overline{R}$ = As desired
2	Set message address for record/playback	Set addresses A0–A9
3A	Begin playback	P/$\overline{R}$ = HIGH, $\overline{CE}$ = Pulsed LOW
3B	Begin record	P/$\overline{R}$ = LOW, $\overline{CE}$ = LOW
4A 4B	End playback End record	Automatic PD or $\overline{CE}$ = HIGH

Table 13: Application Example—Passive Component Functions

Part	Function	Comments
R1	Microphone power supply decoupling	Reduces power supply noise
R2	Release time constant	Sets release time for AGC
R3, R5	Microphone biasing resistors	Provides biasing for microphone operation
R4	Series limiting resistor	Reduces level to prevent distortion at higher supply voltages.
R6	Series limiting resistor	Reduces level to high supply voltages
C1, C5	Microphone DC-blocking capacitor Low-frequency cutoff	Decouples microphone bias from chip. Provides single-pole low-frequency cutoff and common mode noise rejection.
C2	Attack/Release time constant	Sets attack/release time for AGC
C3	Low-frequency cutoff capacitor	Provides additional pole for low-frequency cutoff
C4	Microphone power supply decoupling	Reduces power supply noise
C6, C7, C8	Power supply capacitors	Filter and bypass of power supply

EXPLANATION

In this simplified block diagram of a microcontroller application, the Push-Button mode and message cueing are used. The microcontroller is a 16-pin version with enough port pins for buttons, an LED, and the ISD2500 series device. The software can be written to use three buttons: one each for play and record, and one for message selection. Because the microcontroller is interpreting the buttons and commanding the ISD2500 device, software can be written for any functions desired in a particular application.

NOTE *ISD does not recommend connecting address lines directly to a microprocessor bus. Address lines should be externally latched.*

Figure 5: ISD2560/75/90/120 Application Example—Microcontroller/ISD2500 Interface

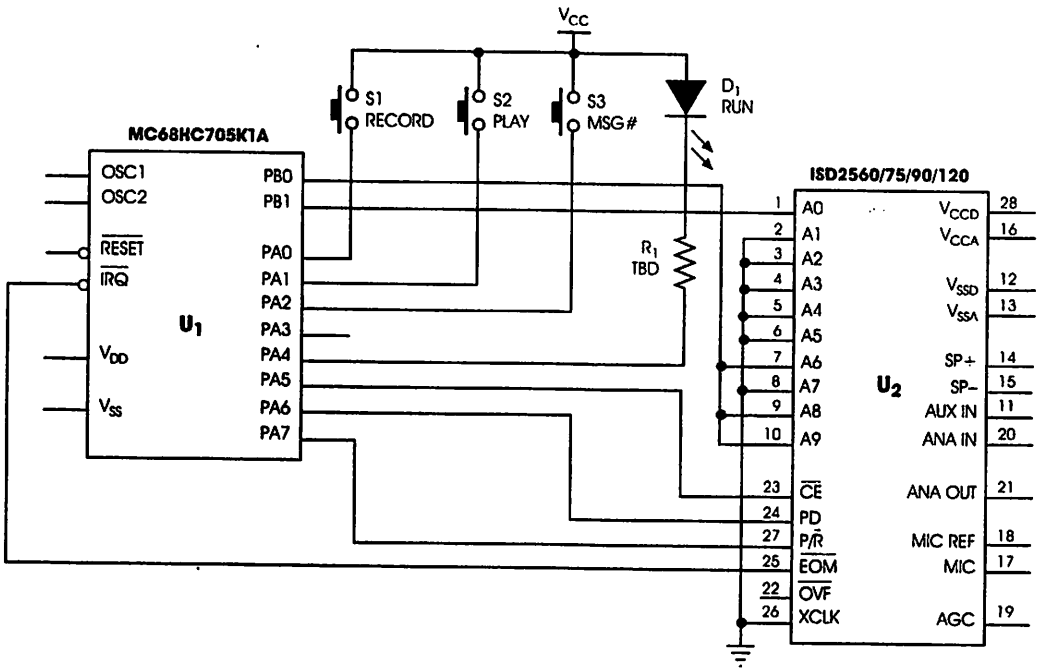
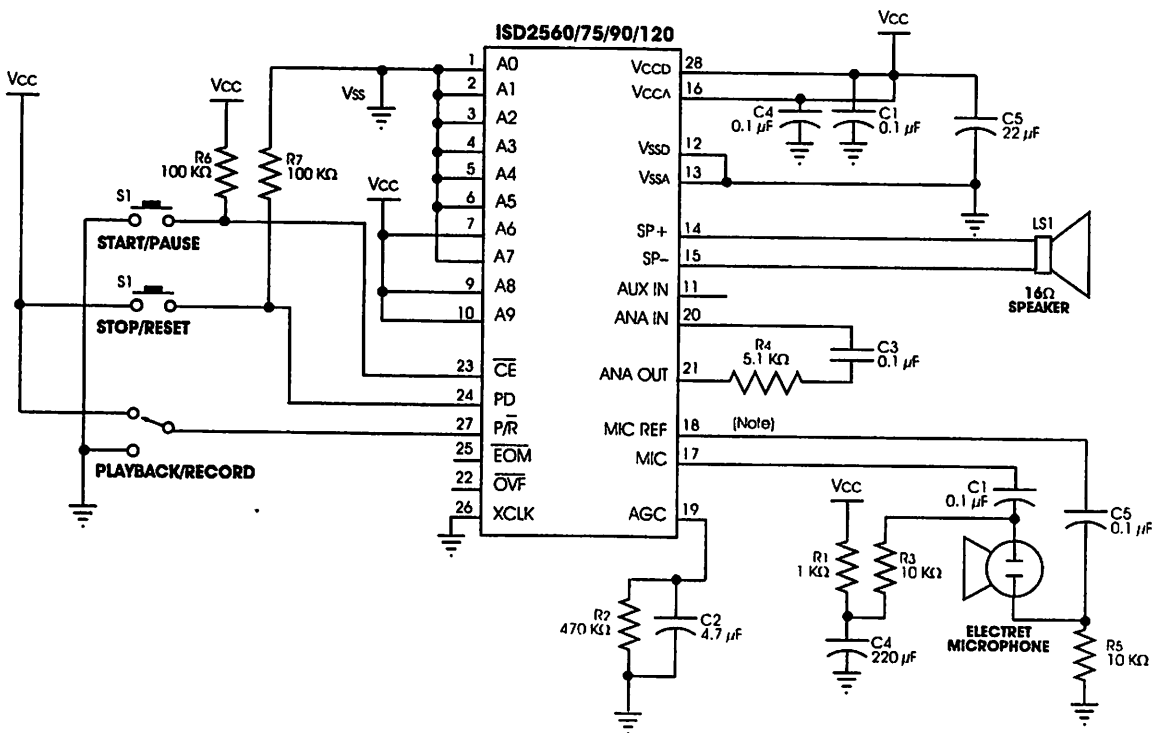


Figure 6: ISD2500 Application Example—Push-Button



NOTE: *Please refer to Application Information.*

Table 14: Application Example—Push-Button Control

Control Step	Function	Action
1	Select record/playback mode	P/$\overline{R}$ = As desired
2A 2B	Begin playback Begin record	P/$\overline{R}$ = HIGH, $\overline{CE}$ = Pulsed LOW P/$\overline{R}$ = LOW, $\overline{CE}$ = Pulsed LOW
3	Pause record or playback	$\overline{CE}$ = Pulsed LOW
4A 4B	End playback End record	Automatic at $\overline{EOM}$ marker or PD = Pulsed HIGH PD = Pulsed HIGH

Table 15: Application Example—Passive Component Functions

Part	Function	Comments
R2	Release time constant	Sets release time for AGC
R4	Series limiting resistor	Reduces level to prevent distortion at higher supply voltages
R6, R7	Pull-up and pull-down resistors	Defines static state of inputs
C1, C4, C5	Power supply capacitors	Filters and bypass of power supply
C2	Attack/Release time constant	Sets attack/release time for AGC
C3	Low-frequency cutoff capacitor	Provides additional pole for low-frequency cutoff

Table 16: Push-Button Parameters

Symbol	Characteristic		Min	Typ (1)	Max	Units	Conditions
T_{CE}	$\overline{CE}$ Pulse Width [Start/Pause]			300		nsec	
T_{SET}	Control/Address Setup Time			300		nsec	
T_{PUD}	Power-Up Delay	ISD2560		25		msec	
		ISD2575		31.25		msec	
		ISD2590		37.25		msec	
		ISD25120		50.0		msec	
T_{PD}	PD Pulse Width [Stop/Reset]			300		nsec	
T_{RUN}	$\overline{CE}$ to $\overline{EOM}$ HIGH		25		400	nsec	
T_{PAUSE}	$\overline{CE}$ to $\overline{EOM}$ LOW		50		400	nsec	
T_{DB}	$\overline{CE}$ HIGH Debounce	ISD2560	70		105	msec	
		ISD2575	85		135	msec	
		ISD2590	105		160	msec	
		ISD25120	135		215	msec	

PUSH-BUTTON TIMING DIAGRAMS

Figure 7: Push-Button Mode Record

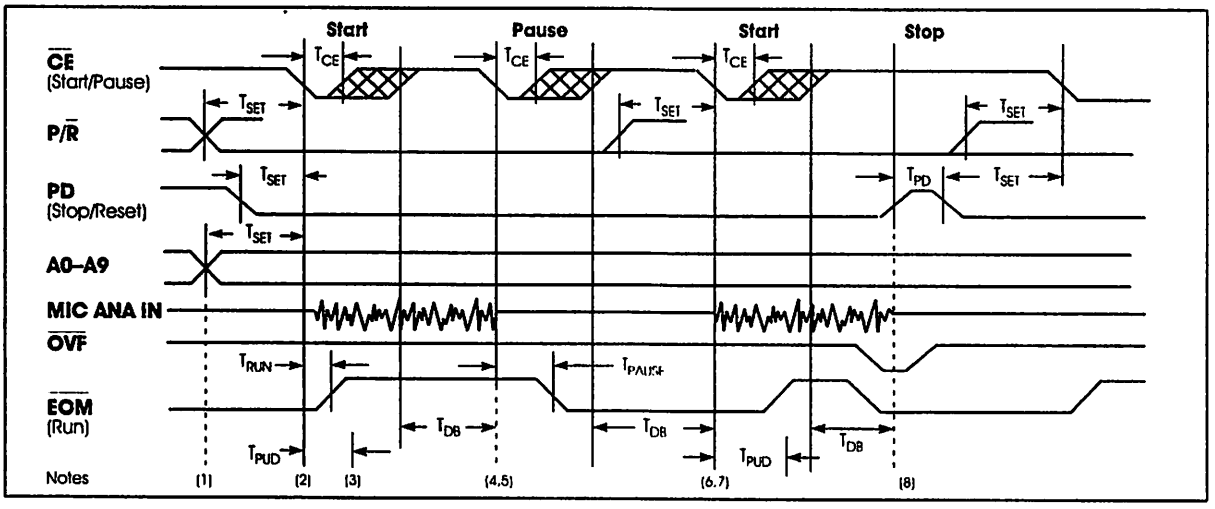
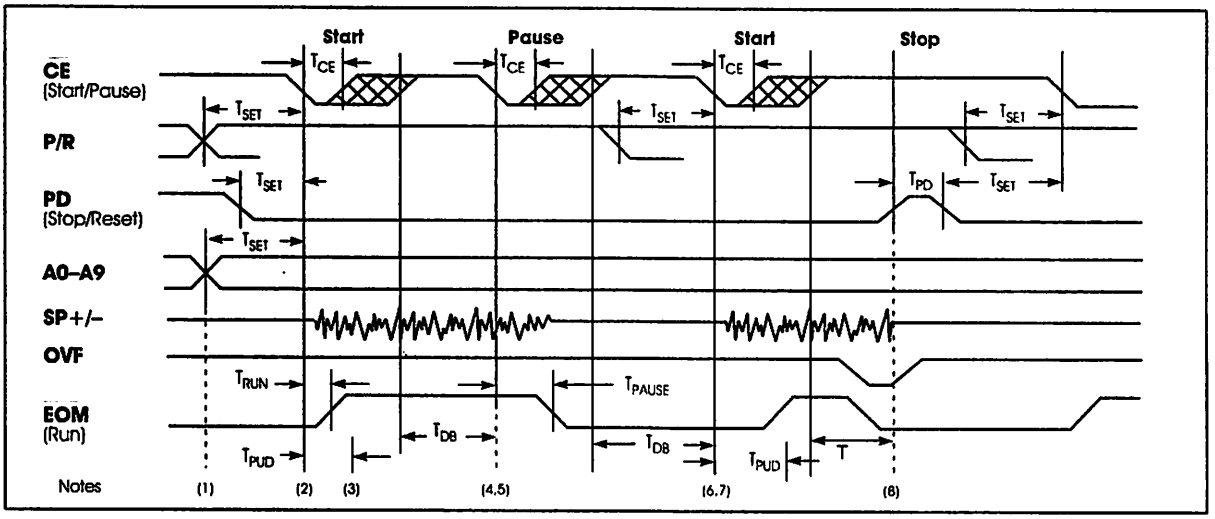


Figure 8: Push-Button Mode Playback



1. *A9, A8, and A6 = 1 for push-button operation.*
2. *The first $\overline{CE}$ LOW pulse performs a Start function.*
3. *The part will begin to play or record after a power-up delay T_{PUD}.*
4. *The part must have $\overline{CE}$ HIGH for a debounce period TDB before it will recognize another falling edge of $\overline{CE}$ and pause.*
5. *The second $\overline{CE}$ LOW pulse, and every even pulse thereafter, performs a Pause function.*
6. *Again, the part must have $\overline{CE}$ HIGH for a debounce period TDB before it will recognize another falling edge of CE, which would restart an operation. In addition, the part will not do an internal power down until $\overline{CE}$ is HIGH for the TDB time.*
7. *The third $\overline{CE}$ LOW pulse, and every odd pulse thereafter, performs a Resume function.*
8. *At any time, a HIGH level on PD will stop the current function, reset the address counter, and power down the device.*

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STAND-ALONE/PARALLEL INTERFACE PRODUCTS

Circuit Examples for ISD1000A and ISD2500 Products

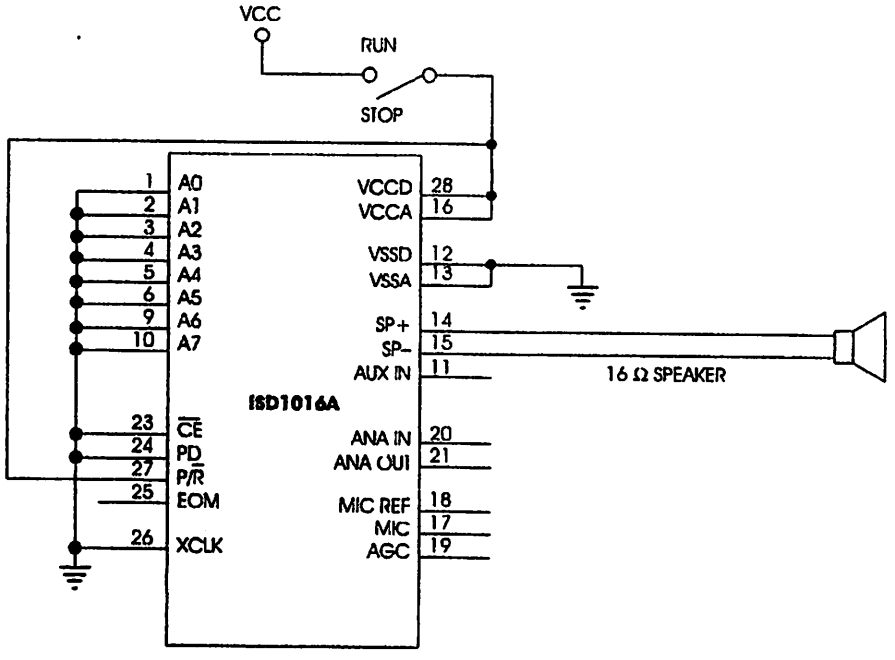
This chapter provides various applications of the ISD series of devices. Most can use the ISD1016A or ISD1020A, as required for the exact application. In many cases, the schematic shows an ISD1016A or the ISD2500 device in the socket.

SIMPLEST PLAYBACK ONLY

The circuit in the figure below represents the simplest playback-only implementation of an ISD1000A series device.

This schematic shows the minimum device count playback-only circuit. Change SW1 to the +5 volt "RUN" position and the contents of the ISD1000A will play one time, then stop. Because $\overline{CE}$ is strapped LOW, set EOM bits will be ignored (though an EOM pulse will be output through the $\overline{EOM}$ pin when a set EOM bit is encountered) and the device will play until it goes into overflow. A momentary change of SW1 to "STOP" then back to "RUN" will cause the contents of the ISD1000A to be played a second time.

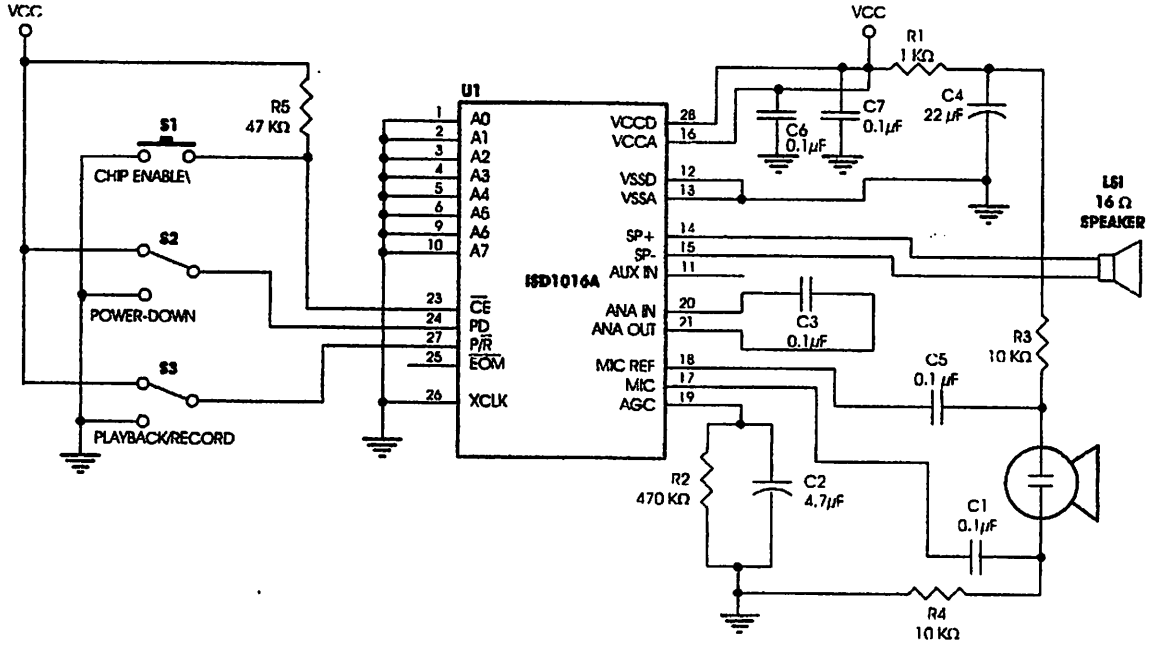
Figure 1: Simplest Playback Only



SIMPLEST PLAYBACK/RECORD

The next circuit represents the simplest implementation of a record and playback non-addressed application. This circuit can use either an ISD1000A or ISD2500 device and is the same schematic found in the data sheets. To operate, start with chip enable HIGH. To record, change the Playback/Record switch to LOW, make sure the power-down switch is LOW, then change the chip enable switch to LOW. Record for the time period of the ISD device used. To playback, momentarily set the power-down switch to HIGH, then back to LOW, change the Playback/Record switch to HIGH, then pulse the chip enable switch LOW, then back HIGH. The previously recorded message will Playback. If the message did not totally fill the device, the power-down cycle is not required. If the chip enable switch is held LOW while in Playback, the entire contents of the device will play regardless of any EOM bits being set.

Figure 2: Simplest Playback/Record Schematic



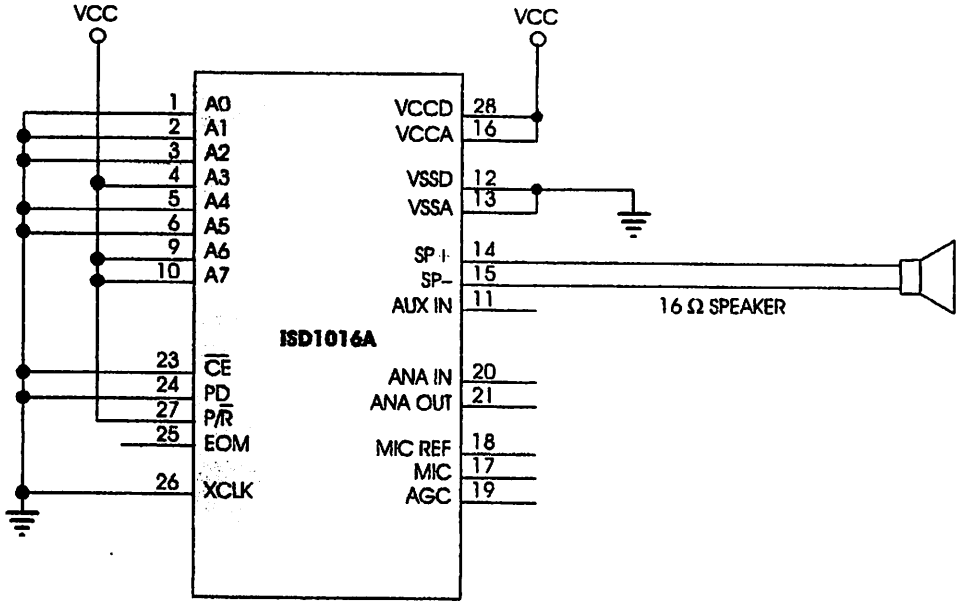
PLAYBACK LOOPING

Many audio applications require repetitive playback or looping on the same message for an extended time. The ISD1000A series of devices may be used to satisfy this requirement using either the built in Operational Mode or using a small amount of external logic. Both applications may be controlled by the Chip Enable pin so looping can be started and stopped or run continuously when power is applied.

PLAYBACK LOOPING USING OPERATIONAL MODE

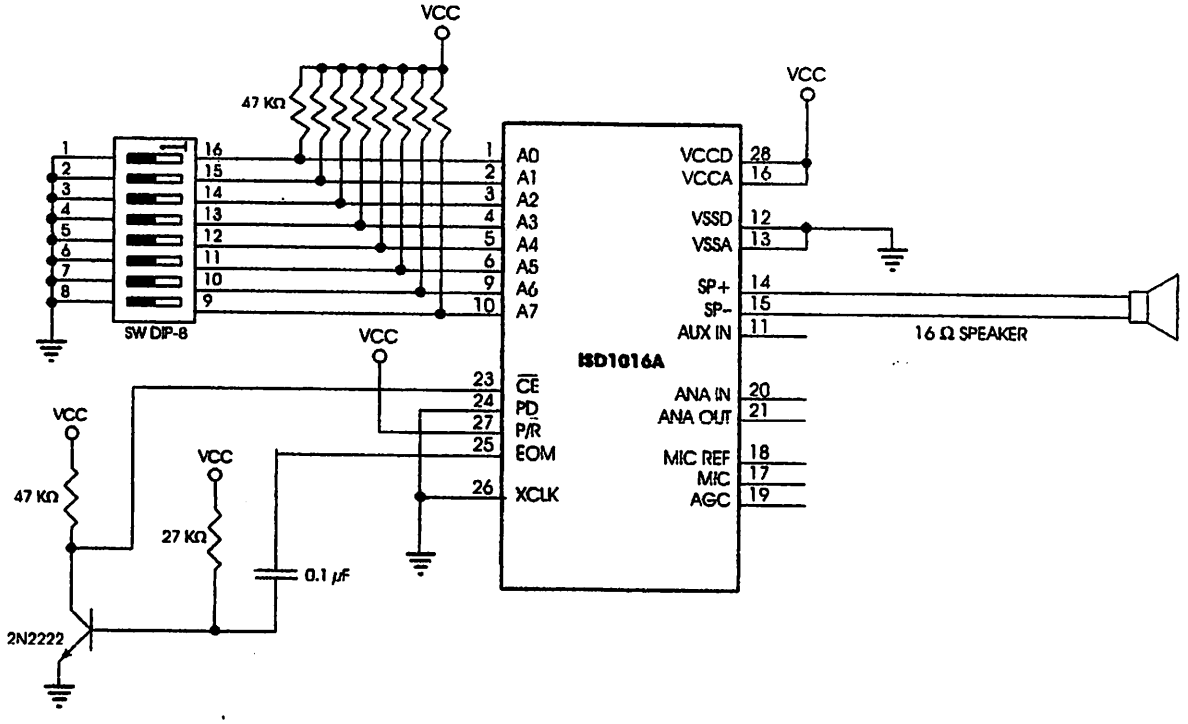
Figure 3 shows that Operational Mode may be used to accomplish playback looping if the message starts at Address 0 (the beginning of the memory) and does not require the full 16 seconds of analog storage. Operational Mode may not be used if the starting address is not zero or the message completely fills the ISD1016A.

Figure 3: Operation Mode Playback Looping



NOTE: *Circuit loops beginning at 000 and the message cannot reach 160 (end).*

Figure 4: Chip Enable Initiated Looping



A message is first recorded into an ISD1016A with all the address bits tied LOW. This positions this message at the beginning of the ISD1016A's address space. Next, the device is put into Operational Mode by connecting Address bits A7 and A6 HIGH (+5 VDC). Bit A3 is also connected HIGH to enable continuous repeat. With PD LOW, P/$\overline{R}$ HIGH, and $\overline{CE}$ held LOW, the beginning message in the ISD1016A will repeat. If $\overline{CE}$ is taken back HIGH after a message has begun, the ISD1016A will complete the message, then stop. If $\overline{CE}$ is strapped LOW, when power is applied, the message will repeat continuously.

CHIP ENABLE INITIATED LOOPING

Figure 4 shows a simple one transistor circuit that may be used to achieve playback looping using chip enable. This circuit may not be used if the ISD1000A series device is completely full.

The $\overline{EOM}$ pulse at the end of a message is differentiated to produce about a 15 ms positive going pulse into the $\overline{CE}$ pin. When this pulse falls, the address is loaded into the device by the DIP switch and a new Playback cycle starts at that address. Since the original message has continued to play during this pulse, the message is smoothly restarted without a break.

THREE MINUTE CASCADE USING THE ISD2560

The circuit illustrated in Figure 5 demonstrates a method of cascading three ISD2560 devices to obtain up to three minutes of storage.

The ISD2560 may be easily cascaded to increase the storage capacity of a system. Two methods are discussed in the following paragraphs. The first method shows three devices cascaded in a mode where a number of messages may be sequentially recorded starting at the beginning of memory. A message may be recorded across the boundary of two devices. The transition between the two devices will be transparent to the user. Message cueing, the A0 Operational Mode (fast forward) may then be used to rapidly access and playback any of the recorded messages. It is not necessary to know the exact address location of each message. Only the sequential message number need be known.

The second method shows how to directly address and record or playback a message at any point in the three devices' memory space. A message may be recorded or played back across the boundary of two devices. The transition between the two devices will again be transparent to the user.

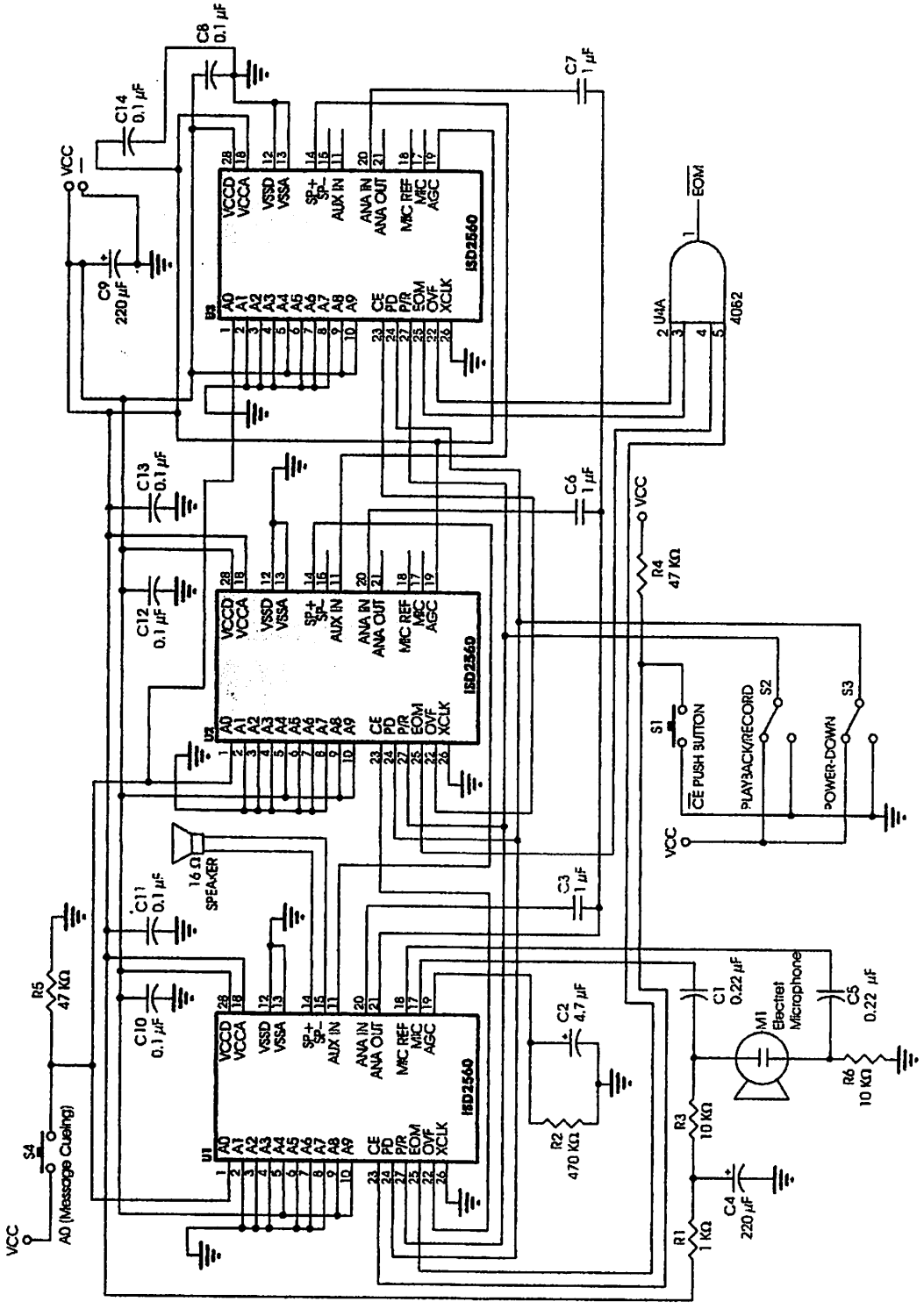
In the two examples shown, three ISD2560s have been cascaded resulting in a total record/playback time of three minutes. Alternatively, ISD2575s or ISD2590s could be used to achieve 3 minutes 45 seconds, or 4 minutes 30 seconds, respectively.

In each example, U1, the first ISD2560 in the series, contains the microphone preamplifier and the speaker output for the entire system. This is in addition to having the first 60 seconds of analog memory. The remainder of the ICs being cascaded serve only as memory elements. The ANA OUT (microphone preamplifier output) pin of U1 is connected through blocking capacitors to the ANA IN of each of the three devices in the cascade. Additionally, the SP+ of U3 is fed back to U2's AUX IN pin and U2's SP+ is connected back to U1's AUX IN pin. Thus, the ANA IN pins are fed in parallel from U1's microphone preamplifier while the speaker outputs "daisy chain" back to U1's speaker amplifier.

SEQUENTIAL RECORD AND MESSAGE CUEING EXAMPLE

Operational Mode is used to set up the ISD2560 for proper cascade operation. The ISD2560 is placed into Operational Mode by connecting address bits A8 and A9 HIGH. The remainder of the Operational Mode bits are tied LOW except as follows:

Figure 5: 3-Minute Cascade Schematic



Bit A4 is HIGH to cause the Message Start Pointer (MSP) to *only* be reset when the system's mode is changed between Record and Playback. (Normally the MSP is initialized anytime the Chip Enable pin goes LOW.)

NOTE The MSP controls where the ISD2500 is going to begin to record or playback on the next operation. It is also initialized when the Power-Down Cycle is initiated.

The result of this configuration is that messages will be stacked sequentially during record across chip boundaries in a manner transparent to the user. Changing from Record to Playback resets the MSP back to the beginning of the first message in the series. The next Playback proceeds under control of chip enable.

Record Operation

To begin recording, place the Record/Playback switch in the record position and hold chip enable LOW for the duration of the recording. To record the second message, repeat the operation; recording will now begin at the end of the first message. Additional recordings may be placed sequentially into the cascaded devices until the memory is full. The $\overline{OVF}$ pulse out of the last memory may be used as a "memory full" indicator.

Playback Operation

To playback the first recorded messages, change the P/$\overline{R}$ pin to a HIGH and pulse the $\overline{CE}$ pin LOW. The first message will playback and stop at the set EOM bit. A second LOW $\overline{CE}$ pulse will start playback of the second message. Each message may start or stop anywhere in the cascade memory. The A0 Message Cueing Operational Mode may also be used to access messages anywhere in the cascade memory. This "fast forward" operation will transparently cross the boundary between two devices. A0 Message Cueing is discussed in detail in the section on Operational Modes.

DIRECT ADDRESSING EXAMPLE

The second cascade circuit shows the added logic necessary for direct address of messages anywhere in the three devices' memories. Only a single 2 input AND gate is required for each chip cascade. For simplicity, the analog circuitry is left off this schematic.

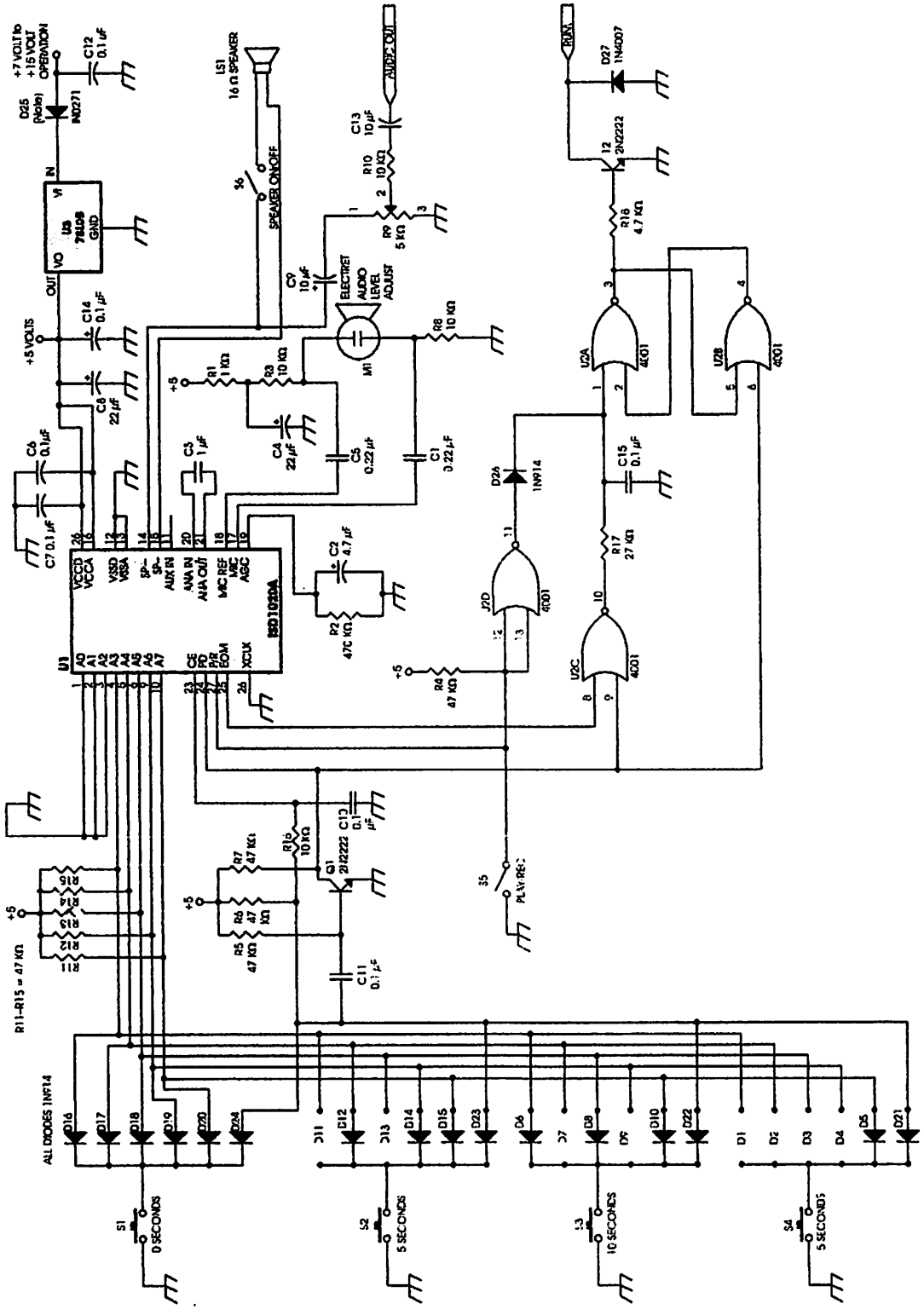
To address any message, the user must know the starting address of the message and in which device it begins. For instance, a message might begin in device U2 at address 400, or 40 seconds into the memory. This message may run over into U3 with no problems. To start playback of this message, PD must be taken LOW and P/$\overline{R}$ taken HIGH. The address 400 (decimal) must be placed on the address bus. This equates to 190 Hex.

Next the $\overline{CE}$2 line is taken LOW and playback begins. Playback will continue until a set EOM bit is found. The pulse will appear at the $\overline{EOM}$ output from U5A. Note that this will be a 12.5 ms pulse unless the message ends at overflow at U3. In this case, the $\overline{EOM}$ pulse will be approximately 6 μs long.

PUSH BUTTON FOUR MEMORY RECORD/PLAYBACK

A version of the circuit shown in Figure 7 first appeared in December 1991 *QST Magazine*. It demonstrates how a single ISD1020A may be used to store up to four 5-second messages that may be individually retrieved using a single push button for each.

Figure 7: Push-Button Four Memory Schematic



NOTE: *D25 is polarity protection.*

HOW THE CIRCUIT WORKS

The ISD1020A can be operated in several different modes. In this project, it operates in an "addressed" mode. The eight address pins of the device determine where the Record and Playback operations begin. The ISD1020A can be looked at as a miniature tape recorder. It has the ability to pre-position the Playback/Record head anywhere on this 20-second tape before we begin an operation. The device has 160 valid addresses, giving an address resolution of 0.125 seconds. This means eight address counts equal 1 second of record time.

To determine what address to give the device, we must first convert seconds into binary counts. A 1-second resolution is adequate for our purposes. Since eight counts equal 1 second and eight is an "even" binary multiple, we can ignore all the counts less than eight. We do this by strapping A0, A1 and A2 to ground and just programming the five remaining bits. Using push buttons and diodes, we can select any interval between 1 and 19 seconds for the start of record or playback.

As shown in Table 1, the four start message locations are 0 seconds (beginning of memory), 5 seconds, 10 seconds and 15 seconds. This defines four 5-second messages.

Table 1: Address Boundaries Example

Chart 1		Chart 2	
Message Start Location	Addr Pins AAAAAAAA 76543210	Message Start Location	Addr Pins AAAAAAAA 76543210
Seconds		Seconds	
0	00000000	0	00000000
5	00101000	4	00100000
10	01010000	8	01000000
15	01111000	14	01110000

Table 1 shows the binary addressing for these intervals. The message start locations could have as easily been defined as 0 seconds, 4 seconds, 8 seconds, and 14 seconds giving two 4-second messages and two 6-second messages. Chart 2 shows this second set of intervals. You can experiment with the diode positions for various addresses but keep in mind that the highest message start address the ISD1020A will recognize is binary 10011111 or 159 decimal. Since A0, A1 and A2 are always at ground, the highest recognizable address is at the 19-second boundary or 10011000.

The Playback/Record function of the ISD1020A is determined by the P/$\overline{R}$ pin (pin 27) of the device. Simply tie it LOW for Record and to +5 V for Playback.

The ISD1020A requires the Chip Enable pin (pin 23) to start HIGH, pulse LOW for Playback and stay at a LOW level during record. All the address and the Playback/Record inputs must be set up before the Chip Enable pin goes LOW. At the end of recording, returning the Chip Enable pin to a HIGH ends the recording and inserts an end of message bit into the ISD1020A's memory. When the Chip Enable pin is pulsed LOW when the Playback/Record pin is HIGH, the device will playback what is recorded until it encounters an end of message bit. It then stops Playback and waits for the next control input.

The one remaining input to the ISD1020A is the power-down or PD pin (pin 24). This pin controls the power requirements of the ISD1020A. When taken to +5 volts, the chip uses less than 10 microamps of current. The device must be powered up (Power-Down pin at ground) to record or playback. This pin also serves as a reset if the ISD1020A is recorded or played "into the stops." That is, all the way to the end of the device's 20-second memory. When that happens, the Power-Down pin must be cycled HIGH then back LOW again for the device to continue operation. This is by design. When two or more ISD1020As are cascaded together to make messages longer than 20 seconds, the device must stop operating when it reaches the end of its memory space so the next chip in the series can take over. This condition is called "memory overflow."

get around the requirement to cycle the Power-wn pin after a memory overflow, the circuit de-n shown here automatically cycles the device ɔugh a power-down cycle each time the chip able is activated. All four push buttons are con-cted to the $\overline{CE}$ pin and to C11 through diodes. ɜ R16, C10 network "debounces" the chip en-le input. When you press a push button, a se-ence of events happens:

1. The $\overline{CE}$ input that is normally held HIGH through R6 is pulled LOW through a diode.
2. The combination of C11 and R5 on the base of Q1 causes a positive pulse to be generated into the PD pin of the ISD1020A.
3. For the duration of this pulse, the ISD1020A is in a power-down state that resets a memory overflow condition if it exists.
4. When the pulse ends and the PD pin returns to ground, the status of the $\overline{CE}$ pin is read.
5. Assuming the $\overline{CE}$ pin is still being pulled LOW (don't be too quick on the push button), the status of the address and P/$\overline{R}$ pins is read and the Record or Playback operation begins.

mponents R2 and C2 control the AGC operation he ISD1020A's internal microphone preamplifi-The AGC pin has an impedance of about 5K ns. This resistance plus C2 determines the at-k time of the AGC which should be very fast. R2 d C2 together determine the release time of AGC which should be fairly slow.

connects the output of the microphone amplifier (ANA OUT, pin 21) to the analog input IA IN, pin 20) of the ISD1020A. These pins are ught out externally so the user can control the frequency response of the recording or direct-ɔccess the analog storage memory of the 1020A. A 1 µF capacitor at this location sets low frequency response to 80 Hz. Users who do want to use the AGC should capacitively cou-to the ANA IN pin with an 50 millivolt peak-to-ɔk signal.

The speaker output of the ISD1020A is designed to drive a 16-ohm speaker. To use an 8-ohm speaker, install R8 to bring the impedance into specification. If you use a 16 Ω speaker, R8 should be replaced with a wire jumper.

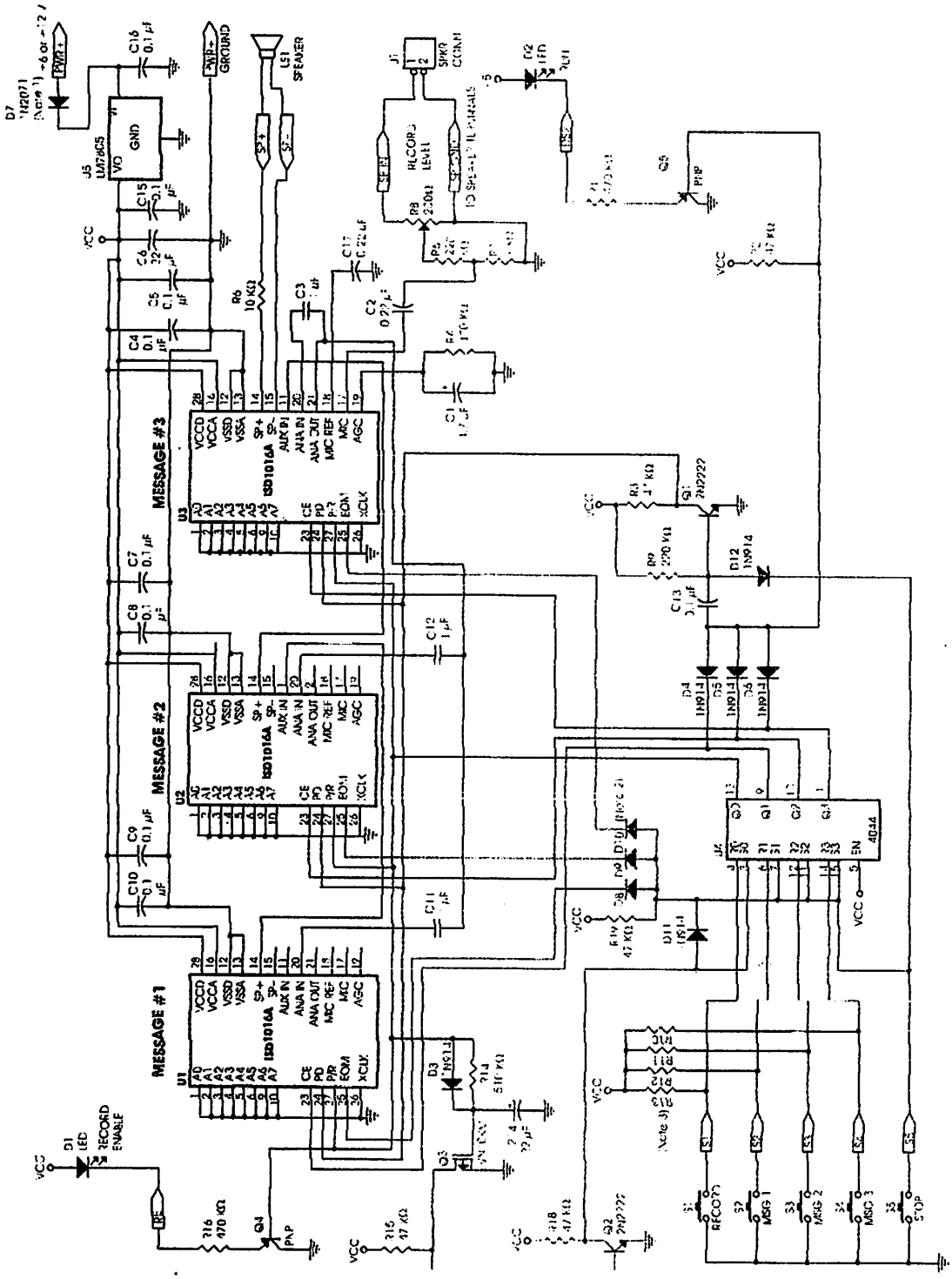
The ISD1000A series does not have a "RUN" output to show when a device is playing back speech. Such a signal is easy to create, however, using a pair of the two input NOR gates contained in a 4001. These gates (U2A and U2B) are connected in a "cross-coupled" configuration and are set by PD signal going LOW at the beginning of Playback and reset by $\overline{EOM}$ going LOW at the end of a message. The resulting signal drives the base of the Q2 2N2222 transistor through R21. U2D keeps the gate from being set during a record operation. U2C and the RC network C15 and R20 correct a possible race condition between the PD signal and $\overline{EOM}$.

OPERATION

Operation of the circuit is simple. To record a message, change the Record/Playback switch to record, then press and hold the desired address button for the duration of the message. To play the message back, change the Record/Playback switch back to Playback and momentarily press the button. The ISD1020A will replay the message.

Keep in mind when recording a new message that if you record a message longer than the address space you have reserved for it, you will begin erasing the next message in the series (unless you go into memory overflow). If you then try to select the message you just erased part of, you will get the end of the new message starting at the message address of the message you just "corrupted." If you want to record a message longer than its allowed message space, just go ahead and do it. Just remember that the next message is not available in this instance.

Figure 8: Radio Notepad Schematic



1. *D7 is a polarity protection diode.*
2. *D8, D9, and D10 are IN914*
3. *R10, R11, R12, and R13 are 47 KΩ.*

IDIO NOTEPAD

e circuit in Figure 8 presents a method of storing ee different 16-second messages using a eaker input. The suggested application is for re-rding messages from a radio receiver.

ere are many applications that require the re-rding of audio directly from a speaker. A short-ve listener-hobbyist may want to record an ent heard on a shortwave or two-way radio annel. There may be a call sign, a radio fre-ency or some other information announced er the air that needs recording for later review. a public safety environment, a police dispatch-may want to record an incoming call for assis-ce to ensure no details are missed.

h the circuit in Figure 8, a simple two button se-ence is all it takes to record the next 16 seconds. A gle push of a button plays each message ck. Three ISD1016As are used to hold indepen-nt messages. An ISD1020A could be used in-ad if desired. This circuit example also monstrates an ISD1000A device run entirely n push buttons.

W IT WORKS

e heart of this application is a 4044 CMOS Quad ND R-S Latch and a VN10 FET timer. The 4044) "remembers" which message button has en pressed when a Record or Playback opera-n is desired. The FET timer enables a record op-tion for its time period. The rest of the circuit is ncipally diode steered logic.

layback operation is initiated by pressing S2, S3 S4 (MSG 1, MSG 2 and MSG 3 respectively) ich resets the appropriate section of U4. The put of the cleared Flip Flop goes LOW, en-ling the correct $\overline{CE}$ for the ISD1016A holding the ssage selected. This output also pulls C13 LOW using Q1 to initiate a PD cycle clearing any pos-e overflow condition. The base of Q1 is pulled W, allowing R3 to pull its collector HIGH, reset-g the PD pins of U1-U3. As R9 charges C13 back the PD line returns LOW. When the PD cycle ds, the selected device plays back its stored ssage. When a set EOM bit is found or an over-flow occurs in the operating ISD1016A, Playback stops and the $\overline{EOM}$ signal goes LOW, setting the U4 flip flops through D8, D9 or D10. Or, a momentary press of the STOP button resets the set R/S flip-flops and initiates a PD cycle. This also ends Playback.

A record operation is started by first pressing the S1 "Record" button. This clears the Record Enable section of U4 (R0/S0/Q0) whose Q output goes to the P/$\overline{R}$ input of all the ISD1016A's. This holds these pins LOW or in the record state. This flip-flop stays cleared until the Q3, R14, C14 network times out. When this happens, the signal from the collector of the Q2 NPN inverter transistor sets the first section of U4, returning all the P/$\overline{R}$ inputs HIGH, back to Playback. If S2 through S4 is pressed while the Q3 timer is running, the appropriate ISD1016A will start recording. A press of the STOP button will end recording by forcing the chip enable lines HIGH out of U4 and setting an EOM bit in the recording device, U1–U3. The values of R14 and C14 are chosen so that the P/$\overline{R}$ pins are held LOW throughout the complete record cycle, or in this example, greater than 16 seconds. If an ISD1020A is used, the value of R14 should be made greater so this time period is greater than 20 seconds.

OPERATION

To operate the radio notepad, connect the input across the speaker terminals and apply power. To record, press the record Enable S1 button then immediately press S2, S3 or S4. Recording will start with the press of the second button. The record Enable LED, D1, along with the RUN LED, D2, will indicate that a record operation is in progress. To stop recording, or to clear a record Enable condition before it times out, press the S5 Stop button. To Playback, press S2, S3 or S4. The message recorded in the appropriate ISD1016A will Playback until the 16 seconds is complete or a set EOM bit is found in the device's EOM memory. The RUN LED, D2, will indicate when a message is being played back. To stop Playback, press Stop.

Some experimentation with the setting of the R8 Record Level pot may be necessary to get good results.

USING THE ISD2500 SERIES WITH A MICROCONTROLLER

The record and playback duration of the ISD2500 series make it possible to perform several functions with a single device. A chip with 32 or more seconds of storage may be used in a number of ways. A library of permanent words, phrases or sounds may be individually played back under external control. Alternatively, this device might be used to record and randomly retrieve arbitrary length messages. A combination of these two approaches is also possible.

Combinational logic may be used to achieve these ends. This approach is complex, however. An inexpensive microcontroller is a simpler and much more flexible solution. The following notes demonstrate several methods of using a single chip microcontroller to control an ISD2500 device.

NOTE ***The address lines of all ISD single-chip record/playback devices are not microprocessor bus compatible.*** *If a device is to be used on a bus oriented system, the address lines must be buffered and latched.*

CONVENTIONAL MODE OPERATION

An obvious method of driving the device is to operate it in the conventional mode. The sequence for such an operation is as follows:

1. Change the PD pin to LOW and delay T_{PUD} (see the ISD2500 series data sheets). This will power up the device.
2. Apply the desired address to the address inputs.
3. Apply the correct level to the P/$\overline{R}$ pin as desired (0 = record, 1 = play).
4. Pulse $\overline{CE}$ LOW to begin Playback, hold $\overline{CE}$ low to begin record, bring $\overline{CE}$ back HIGH to end record.
5. If low power is required, change PD back to HIGH when the operation is complete.

The timing of the above sequence is not critical at microcontroller speeds. For instance, required address setup timing (T_{SET}) is 300 nanoseconds before the falling edge of $\overline{CE}$. Few microcontrollers can execute fast enough to violate this timing.

A microcontroller may be used to detect the end of a normal speed Playback operation in at least two ways.

- Since the $\overline{EOM}$ pulse width in the fastest ISD2500 series parts (ISD2532/60) is over 12.5 milliseconds long, it is possible to poll this input and watch for it to go LOW.
- An alternative method would be to connect the $\overline{EOM}$ pin to the microcontroller's interrupt input. If an edge-triggered interrupt sense is available, it may be more efficient to sense the rising edge of $\overline{EOM}$. This is because a new $\overline{CE}$ initiated operation cannot begin until $\overline{EOM}$ pin returns to the HIGH state.

The ISD2500 series includes the $\overline{OVF}$ pin to indicate the overflow or message full condition. During Playback the $\overline{OVF}$ pin pulses LOW for approximately 6 microseconds when overflow is reached. The $\overline{EOM}$ pin does not go LOW at overflow unless an EOM bit is set in last row of the analog memory. After the initial $\overline{OVF}$ pulse goes LOW, the $\overline{OVF}$ pin will track the $\overline{CE}$ input as long as the device remains in overflow. This pin is normally used to cascade multiple ISD2500 devices together.

The original short $\overline{OVF}$ pulse may be detected using the microcontroller's external interrupt input. An alternative technique would be to hold $\overline{CE}$ LOW, even during Playback. The $\overline{OVF}$ pin will now go LOW and stay LOW at overflow and may be detected by polling. In this example, a falling $\overline{EOM}$ must be detected and used to force $\overline{CE}$ back HIGH. $\overline{CE}$ must go back HIGH before $\overline{EOM}$ goes HIGH. If $\overline{EOM}$ goes HIGH with $\overline{CE}$ still LOW, the set EOM bit will be skipped and the device will continue on playing back the next message.

;SAGE CUEING "FAST FORWARD" OPERATION

ne applications may require the use of the ssage Cueing M0 Operational Mode. This de allows the user to "fast forward" through the ssage space of the device (see the section on erational Mode). When operating in this mode, ISD2500's internal timing is sped up by a factor 00. The $\overline{EOM}$ pulse width now may be as small 1 1 ms. (A general discussion of Message Cue- timing may be found in the section on Opera- al Modes.) This timing is too short to allow for led operation in most microcontrollers. The ex- al interrupt should be used to detect $\overline{EOM}$ in instance.

count is often a factor when using a microcon- er. The designer may not want to tie up 8 pins address plus PD, $\overline{CE}$, P/$\overline{R}$, $\overline{OVF}$ and $\overline{EOM}$. This is otal of 13 pins. An alternative approach is to the Message Cueing M0 Operational Mode the M4 consecutive addressing mode. This olication requires the connection of only 6 pins he microcontroller: PD, $\overline{CE}$, P/$\overline{R}$, $\overline{OVF}$, $\overline{EOM}$ and . M4, A8 and A9 are permanently tied HIGH d all the rest of the address pins are tied LOW. quential recordings of multiple messages of dom length and the playback of those mes- es in any order are possible in the following se- ences.

quential Recording

1. M0 is left LOW throughout record.
2. Change the PD pin to LOW and delay T_{PUD}.
3. Change P/$\overline{R}$ to LOW.
4. Hold $\overline{CE}$ low to begin the first record. Bring $\overline{CE}$ back HIGH to end record.
5. Additional record operations may be done using sequence 4. Each recording will be appended to the end of the previous with an EOM flag bit set at the end of each messages.
6. $\overline{OVF}$ will go LOW if the device overflows during record.
7. At the end of the record sequence, PD is taken HIGH to power down the device and to reset the internal address counter.

Playback of Messages in Any Order

To playback message "N," perform the following sequence:

1. Change the PD pin to LOW and delay T_{PUD}.
2. Change P/$\overline{R}$ to HIGH.
3. If N = 1 (the first message), then A0 = 0, and pulse $\overline{CE}$ LOW. The first message will play then stop.
4. If N is greater than 1, you must first execute N-1 A0 Message Cueing Operational Mode cycles by doing the following:
   a. Change A0 to HIGH.
   b. Pulse $\overline{CE}$ LOW for less than 10 μs.
   c. Either watch for a LOW $\overline{EOM}$ (may be as short as 11 μs) or pause for approximately 100 ms.
   d. Each time you find an EOM, you have reached the end of a message. You will have moved silently through a message at 800 times normal speed.
   e. Subtract 1 from N. If N does not equal 1, proceed to sequence (a) and do it again.
5. If N has been subtracted down to 1, then change A0 to 0 and pulse $\overline{CE}$ LOW. The Nth message will play at normal speed.

NOTE *The timings above are approximate. See the Operational Modes for a general discussion of Message Cueing Timing.*

PUSH-BUTTON MODE OPERATION

The ISD2500 series device includes a new Operational Mode called "Push-Button Mode." This M6 Operational Mode changes the functionality of the $\overline{CE}$, PD and $\overline{EOM}$ pins. The operations of these pins are fully explained in the Operational Mode section. A microcontroller may be used with this mode to gain several important extra features. Push-Button Mode allows the user to sequentially

playback several messages then change to record and add additional messages at the end of those already played. This also allows the designer to power-down the device between sequential record operations, an important feature in battery powered applications.

Sequential Record with Power-Down in Between

In the following sequences, M4, M6, A8 and A9 of an ISD2560 are tied together and to a pin of the microcontroller. The A0 Message Cueing Operational Mode is used as indicated. All the other address pins are tied LOW. It is only necessary to use 6 pins from the microcontroller, PD (Stop/Reset), $\overline{CE}$ (Start/Pause), $\overline{EOM}$ (run), P/$\overline{R}$, A0 and the combined M4, M6, A8 and A9. These combined pins will be called Op Mode Control. $\overline{EOM}$ is tied to the microcontroller's external interrupt pin. The microcontroller should be set up for a negative edge triggered interrupt. $\overline{OVF}$ is not needed as explained below.

To achieve flexible message control, the microcontroller must keep track of the number of messages recorded and played back. This count will be used with the A0 Message Cueing "fast forward" function to record messages sequentially and play them back in any order.

NOTE *A false interrupt is generated each time a control operation causes the $\overline{EOM}$ to fall. These interrupts should be ignored by the microcontroller. The $\overline{EOM}$ pin will go LOW and generate a wanted interrupt under two circumstances: during Playback or Message Cueing when a set EOM bit is encountered and during record when the device goes into overflow. This also allows the designer to determine when overflow is reached without looking at the overflow pin.*

---

1. The sequence begins with PD HIGH, P/$\overline{R}$ HIGH, $\overline{CE}$ HIGH and Op Mode control LOW.
2. Set up to record of the first message by taking PD LOW, P/$\overline{R}$ LOW, and Op Mode control HIGH.
3. When the OP Mode control pin goes HIGH, the $\overline{EOM}$ pin (which becomes the active HIGH run pin in Push-Button Mode) pin will go LOW to indicate the operation has not yet started. This will cause an interrupt in the microcontroller that should be "discarded."
4. To begin record, pulse $\overline{CE}$ LOW (a pulse begins and ends record in Push-Button Mode). The $\overline{EOM}$ pin will go HIGH to indicate an operation in progress. When recording is finished, pulse $\overline{CE}$ LOW to end the record cycle. The $\overline{EOM}$ pin will go LOW and generate another false interrupt.
5. After the completion of the record, change the Op Mode control pin to HIGH, and take PD HIGH. This powers down the ISD2560 device to typically 1 microamp.
6. To record the second message, take PD HIGH (T_{PUD} delay), P/$\overline{R}$ HIGH, and Op Mode control HIGH (false interrupt). We are now positioned at the beginning of the first message. Take A0 HIGH and pulse $\overline{CE}$ LOW. This puts the device into Message Cueing "fast forward" and jumps to the end of the first message. The $\overline{EOM}$ pin will go HIGH and then LOW to indicate the end of the first message has been found. The $\overline{EOM}$ interrupt may be used by the microcontroller to process this.
7. A0 may now be taken LOW, P/$\overline{R}$ changed to LOW, and a new record cycle begun. A unique feature of Push-Button Mode keeps the internal address pointer of the ISD2560 from being reset during the change of P/$\overline{R}$ from HIGH to LOW. Recording of the second message will begin at the end of the first message. The set EOM bit at the end of the first message will remain. The device may again be powered down.
8. Subsequent recordings may be made using additional A0 Message Cueing operations.

ıyback Operations

yback of any message may be achieved us- | the Push-Button and A0 Operational Modes.

1. The sequence begins with PD HIGH, P/$\overline{R}$ HIGH, $\overline{CE}$ HIGH and Op Mode control LOW.
2. Change PD to LOW (T_{PUD}), and Op Mode control HIGH (false interrupt).
3. Take A0 HIGH and execute N-1 Fast Forward operations.
4. Take A0 LOW and pulse $\overline{CE}$ LOW to begin playback of the desired message.
5. A falling $\overline{EOM}$ indicates an end of message has been found.
6. Take Op Mode control LOW and PD HIGH to power-down the device.

OTHER NOTES

A continuous LOW on the interrupt input of some microcontrollers may interfere with other types of interrupts. The reason that the device is taken out of Push-Button Mode after each operation is to make the $\overline{EOM}$ pin go HIGH in the static state. This frees up the microcontroller's interrupt structure.

All Push-Button Mode operations will be slowed by the debounce timer built into this function. A delay of T_{DB} will occur with each Push-Button Mode operation.

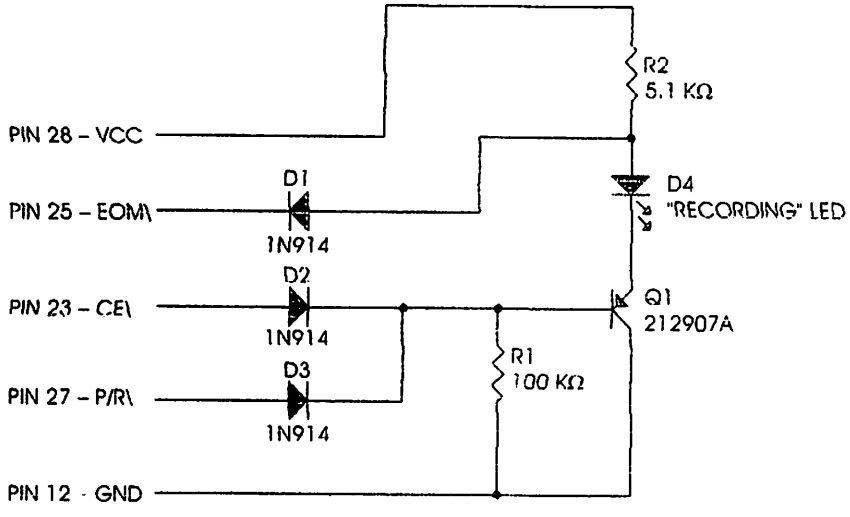
CONCLUSION

The above explanations show one of many possible ways to control the ISD2500 series device with a microcontroller. The designers should review this information and apply their unique perspective to the application they are designing.

RECORDING INDICATOR LIGHT

The circuit shown in Figure 9 is a simple method of using an LED to indicate when a record operation is in progress with an ISD1000A series device.

Figure 9: Recording Indicator Light for ISD1000A



'E: *This circuit will turn on the LED only when actually recording. It requires a valid record selection (P/$\overline{R}$ LOW), and CE LOW to turn on. At the end of the time in the chip, EOM goes LOW and turns off the LED.*

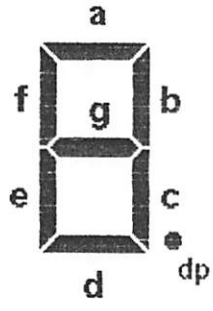
possible number of LEDs in such a way as to represent only numbers in a simple fashion.

This requires just seven LEDs (plus an eighth one for the decimal point, if that is needed). A common technique is to use a shaped piece of translucent plastic to operate as a specialized optical fiber, to distribute the light from the LED evenly over a fixed bar shape. The seven bars are laid out as a squared-off figure "8". The result is known as a seven-segment LED.

We've all seen seven-segment displays in a wide range of applications. Clocks, watches, digital instruments, and many household appliances already have such displays. In this experiment, we'll look at what they are and how they can display any of the ten decimal digits 0-9 on demand.

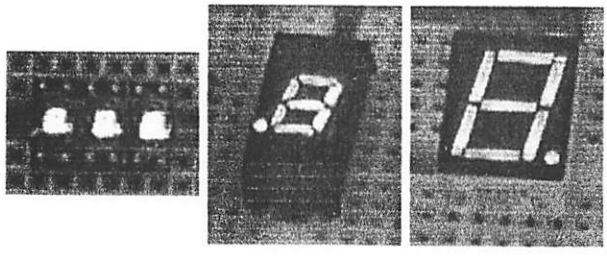
Seven-Segment Display Layout

The illustration to the right shows the basic layout of the segments in a seven-segment display. The segments themselves are identified with lower-case letters "a" through "g," with segment "a" at the top and then counting clockwise. Segment "g" is the center bar.



Most seven-segment digits also include a decimal point ("dp"), and some also include an extra triangle to turn the decimal point into a comma. This improves readability of large numbers on a calculator, for example. The decimal point is shown here on the right, but some display units put it on the left, or have a decimal point on each side.

In addition, most displays are actually slanted a bit, making them look as if they were in italics. This arrangement allows us to turn one digit upside down and place it next to another, so that the two decimal points look like a colon between the two digits. The technique is commonly used in LED clock displays.



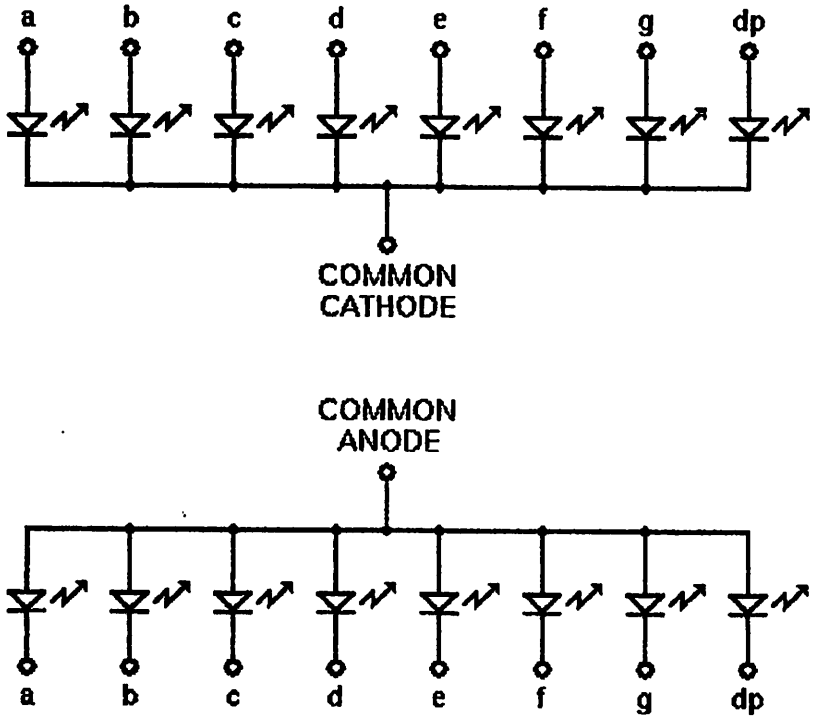
Seven-segment displays can be packaged in a number of ways. Three typical packages are shown above. On the left we see three small digits in a single 12-pin DIP package. The individual digits are very small, so a clear plastic bubble is molded over each digit to act as a magnifying lens. The sides of the end bubbles are flattened so that additional packages of this type can be placed end-to-end to create a display of as many digits as may be needed.

The second package is essentially a 14-pin DIP designed to be installed vertically. Note that for this particular device, the decimal point is on the left. This is not true of all seven-segment displays in this type of package.

One limitation of the DIP package is that it cannot support larger digits. To get larger displays for easy reading at a distance, it is necessary to change the package size and shape. The package on the right above is larger than the other two, and thus can display a digit that is significantly larger than will fit on a standard DIP footprint. Even larger displays are also available; some digital clocks sport digits that are two to five inches tall.

Seven-segment displays can be constructed using any of a number of different technologies. The three most common methods are fluorescent displays (used in many line-powered devices such as microwave ovens and some clocks and clock radios), liquid crystal displays (used in many battery-powered devices such as watches and many digital instruments), and LEDs (used in either line-powered or battery-powered devices). However, fluorescent displays require a fairly high driving voltage to operate, and liquid crystal displays require special treatment that we are not yet ready to discuss. Therefore, we will work with a seven-segment LED display in this experiment.

Schematic Diagram



As shown in the two schematic diagrams above, the LEDs in a seven-segment display are not isolated from each other. Rather, either all of the cathodes, or all of the anodes, are connected together into a common lead, while the other end of each LED is individually available. This means fewer electrical connections to the package, and also allows us to easily enable or disable a particular digit by controlling the common lead. (In some cases, the common connections are made to groups of LEDs, and the external wiring must make the final connections between them. In other cases, the common connection is made available at more than one location for convenience in laying out printed circuit boards. When laying out circuits using such devices, you simply need to take the specific connection details into account.)

of the two segments in this orientation.

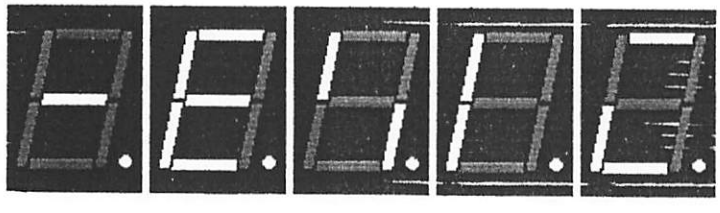
When you turned on every switch except S0, you saw a digit 8, where all seven segments were turned on. However, when you reversed the LED display unit again, you saw a digit 0 with the decimal point turned on. This indicated that the decimal point and segment g are connected to opposite but corresponding pins.

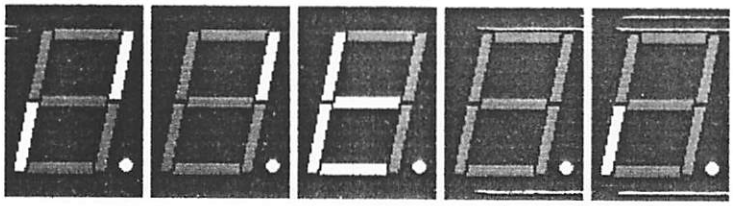
To verify this and all other connections, you reversed the LED display once more and then identified which switch controls which segment in the inverted position. You discovered that S6 through S1 still controlled segments a through f, whether the LED display is right side up or upside down. Only segment g and the decimal point are interchanged.

This arrangement is deliberate. It often simplifies the layout of printed circuit boards. In addition, a common technique used in digital clock displays is to turn the tens of minutes digit upside down and use its decimal point in tandem with the hours digit decimal point to form a colon.

Most single-digit 7 segment displays are set up this way, with the segment connections symmetrical. In some cases, however, the common connection is not shared among all LEDs. Rather, multiple common connections (common cathode for this experiment) must sometimes be linked externally to enable all segments. In the case of the LED display we specified for this experiment, all LED cathodes are connected together, and to the center pins at the top and bottom of the package. The black jumper grounded the cathodes regardless of the orientation of the display. The actual pin connections to the specified display unit are ('K' represents the common cathode):

You should also have found that it's not hard to form all ten digits using the 7-segment display. Digit 2, for example, requires segments a, b, d, e, and g. Digit 3 removes segment e from that list, and adds segment c. The two digits 6 and 9 have two possibilities each. Digit 6 can be made with or without segment a, and digit 9 can be made with or without segment d. You can choose either method, but for consistency you should treat both digits the same way. Except for that possible variation, your ten digits should have looked like this:





When you have completed this experiment, make sure power to your experimental circuit is turned off. Remove all of the orange jumpers from your breadboard socket and put them aside for later use. Leave the 7-segment LED display and its black jumper in place for the next experiment.

Your next experiment is: The Seven-Segment LED Driver

National Semiconductor

August 2000

LM386
Low Voltage Audio Power Amplifier

General Description

The LM386 is a power amplifier designed for use in low voltage consumer applications. The gain is internally set to 20 to keep external part count low, but the addition of an external resistor and capacitor between pins 1 and 8 will increase the gain to any value from 20 to 200.

The inputs are ground referenced while the output automatically biases to one-half the supply voltage. The quiescent power drain is only 24 milliwatts when operating from a 6 volt supply, making the LM386 ideal for battery operation.

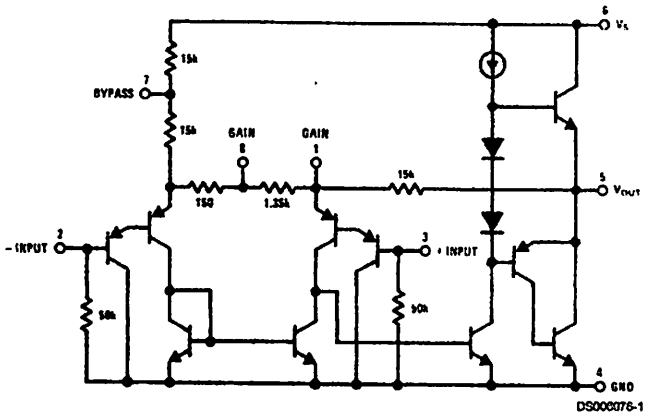
Features

- Battery operation
- Minimum external parts
- Wide supply voltage range: 4V–12V or 5V–18V
- Low quiescent current drain: 4mA
- Voltage gains from 20 to 200
- Ground referenced input
- Self-centering output quiescent voltage
- Low distortion: 0.2% (A_V = 20, V_S = 6V, R_L = 8Ω, P_O = 125mW, f = 1kHz)
- Available in 8 pin MSOP package

Applications

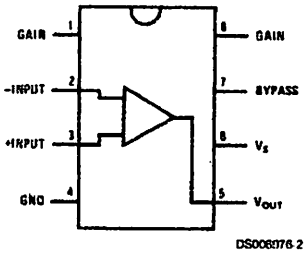
- AM-FM radio amplifiers
- Portable tape player amplifiers
- Intercoms
- TV sound systems
- Line drivers
- Ultrasonic drivers
- Small servo drivers
- Power converters

Equivalent Schematic and Connection Diagrams



DS006976-1

Small Outline, Molded Mini Small Outline, and Dual-In-Line Packages



DS006976-2

Top View
Order Number LM386M-1, LM386MM-1, LM386N-1, LM386N-3 or LM386N-4
See NS Package Number M08A, MUA08A or N08E

Absolute Maximum Ratings (Note 2)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Supply Voltage	
(LM386N-1, -3, LM386M-1)	15V
Supply Voltage (LM386N-4)	22V
Package Dissipation (Note 3)	
(LM386N)	1.25W
(LM386M)	0.73W
(LM386MM-1)	0.595W
Input Voltage	±0.4V
Storage Temperature	−65°C to +150°C
Operating Temperature	0°C to +70°C
Junction Temperature	+150°C
Soldering Information	
Dual-In-Line Package	
Soldering (10 sec)	+260°C
Small Outline Package	
(SOIC and MSOP)	
Vapor Phase (60 sec)	+215°C
Infrared (15 sec)	+220°C

See AN-450 "Surface Mounting Methods and Their Effect on Product Reliability" for other methods of soldering surface mount devices.

Thermal Resistance	
θ_{JC} (DIP)	37°C/W
θ_{JA} (DIP)	107°C/W
θ_{JC} (SO Package)	35°C/W
θ_{JA} (SO Package)	172°C/W
θ_{JA} (MSOP)	210°C/W
θ_{JC} (MSOP)	56°C/W

Electrical Characteristics (Notes 1, 2)

T_A = 25°C

Parameter	Conditions	Min	Typ	Max	Units
Operating Supply Voltage (V_S)					
LM386N-1, -3, LM386M-1, LM386MM-1		4		12	V
LM386N-4		5		18	V
Quiescent Current (I_Q)	V_S = 6V, V_{IN} = 0		4	8	mA
Output Power (P_{OUT})					
LM386N-1, LM386M-1, LM386MM-1	V_S = 6V, R_L = 8Ω, THD = 10%	250	325		mW
LM386N-3	V_S = 9V, R_L = 8Ω, THD = 10%	500	700		mW
LM386N-4	V_S = 16V, R_L = 32Ω, THD = 10%	700	1000		mW
Voltage Gain (A_V)	V_S = 6V, f = 1 kHz		26		dB
	10 µF from Pin 1 to 8		46		dB
Bandwidth (BW)	V_S = 6V, Pins 1 and 8 Open		300		kHz
Total Harmonic Distortion (THD)	V_S = 6V, R_L = 8Ω, P_{OUT} = 125 mW		0.2		%
	f = 1 kHz, Pins 1 and 8 Open				
Power Supply Rejection Ratio (PSRR)	V_S = 6V, f = 1 kHz, C_{BYPASS} = 10 µF		50		dB
	Pins 1 and 8 Open, Referred to Output				
Input Resistance (R_{IN})			50		kΩ
Input Bias Current (I_{BIAS})	V_S = 6V, Pins 2 and 3 Open		250		nA

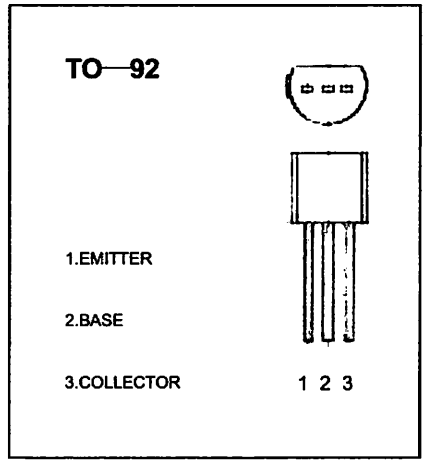
Note 1: All voltages are measured with respect to the ground pin, unless otherwise specified.

Note 2: Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is functional, but do not guarantee specific performance limits. Electrical Characteristics state DC and AC electrical specifications under particular test conditions which guarantee specific performance limits. This assumes that the device is within the Operating Ratings. Specifications are not guaranteed for parameters where no limit is given, however, the typical value is a good indication of device performance.

Note 3: For operation in ambient temperatures above 25°C, the device must be derated based on a 150°C maximum junction temperature and 1) a thermal resistance of 107°C/W junction to ambient for the dual-in-line package and 2) a thermal resistance of 170°C/W for the small outline package.

9012

PNP SILICON TRANSISTOR



EATURES

Power dissipation

P_{CM} : 0.625 W (Tamb=25℃)

Collector current

I_{CM} : -0.5 A

Collector-base voltage

$V_{(BR)CBO}$: -40 V

LECTRICAL CHARACTERISTICS (Tamb=25℃ unless otherwise specified)

Parameter	Symbol	Test conditions	MIN	TYP	MAX	UNIT
ollector-base breakdown voltage	$V(BR)_{CBO}$	Ic= -100 μ A, I_E=0	-40			V
ollector-emitter breakdown voltage	$V(BR)_{CEO}$	Ic= -0. 1 mA, I_B=0	-20			V
mitter-base breakdown voltage	$V(BR)_{EBO}$	I_E= -100 μ A, I_C=0	-5			V
ollector cut-off current	I_{CBO}	V_{CB}=-40 V I_E=0			-0.1	μ A
ollector cut-off current	I_{CEO}	V_{CE}=- 20 V I_B=0			-0.2	μ A
mitter cut-off current	I_{EBO}	V_{EB}= - 5 V, I_C=0			-0.1	μ A
C current gain(note)	$H_{FE\ (1)}$	V_{CE}= -1 V, I_C= -50 mA	64		300	
	$H_{FE\ (2)}$	V_{CE}= -1V, I_C =-500 mA	40			
ollector-emitter saturation voltage	V_{CE}(sat)	I_C=-500 mA, I_B=-50 mA			-0.6	V
ase-emitter saturation voltage	V_{BE}(sat)	I_C=-500mA,I_B=-50 mA			-1.2	V
ase-emitter voltage	V_{EB}	I_E=-100mA			-1.4	V
ransition frequency	f_T	V_{CE}=- 6 V, I_C= -20 mA f =30MHz	150			MHz

LASSIFICATION OF $H_{FE(1)}$

Rank	D	E	F	G	H	I
Range	64-91	78-112	96-135	112-166	144-202	190-300

ıg Shing Computer Components Co., (H.K.)Ltd. Tel:(852)2341 9276 Fax:(852)2797 8153
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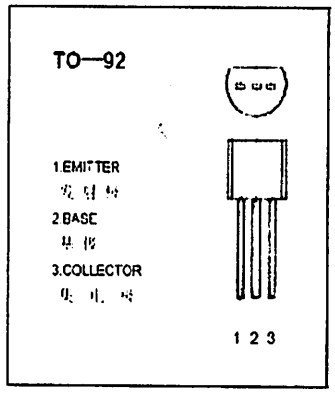
9013 NPN SILICON TRANSISTOR



FEATURES

特　　征

Power dissipation　　（最大耗散功率）

P_{CM} : 0.625 W (Tamb=25℃)

Collector current　　（最大集电极电流）

I_{CM} : 0.5 A

Collector-base voltage　　（集电极-基极击穿电压）

$V_{(BR)CBO}$: 45 V

ELECTRICAL CHARACTERISTICS (Tamb=25℃ unless otherwise specified)

电　　特　　性　　（环境温度　　除　非　另　有　规　定）

Parameter 参　数	Symbol 符　号	Test conditions 测　试　条　件	MIN 最小值	TYP 典型值	MAX 最大值	UNIT 单位
Collector-base breakdown voltage 集电极--基极击穿电压	$V(BR)_{CBO}$	Ic= 100μA, I_E=0	45			V
Collector-emitter breakdown voltage 集电极--发射极击穿电压	$V(BR)_{CEO}$	Ic= 0.1mA, I_B=0	25			V
Emitter-base breakdown voltage 发射极--基极击穿电压	$V(BR)_{EBO}$	I_E= 100μA, I_C=0	5			V
Collector cut-off current 集电极--基极截止电流	I_{CBO}	V_{CB}= 40 V I_E=0			0.1	μA
Collector cut-off current 集电极--发射极截止电流	I_{CEO}	V_{CE}= 20 V I_B=0			0.1	μA
Emitter cut-off current 发射极--基极截止电流	I_{EBO}	V_{EB}= 5 V, I_C=0			0.1	μA
DC current gain(note) 直流电流增益	$H_{FE(1)}$	V_{CE}= 1V, I_C= 50 mA	64		300	
	$H_{FE(2)}$	V_{CE}= 1V, I_C=500 mA	40			
Collector-emitter saturation voltage 集电极--发射极饱和压降	V_{CE}(sat)	I_C= 500 mA, I_B=50 mA			0.6	V
Base-emitter saturation voltage 基极-发射极饱和压降	V_{BE}(sat)	I_C= 500mA, I_B= 50 mA			1.2	V
Base-emitter voltage 基极--发射极正向电压	V_{BE}	I_E=100mA			1.4	V
Transition frequency 特征频率	f-	V_{CE}= 6 V, I_C= 20 mA f =30MHz	150			MHz

CLASSIFICATION OF $H_{FE(1)}$　　（分类）

Rank 档次	D	E	F	G	H	I
Range 范围	64-91	78-112	96-135	112-166	144-220	190-300

Wing Shing Computer Components Co., (H.K.)Ltd. Tel.(852)2341 9276 Fax.(852)2797 8153
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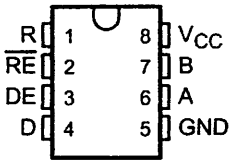
SLLS101B – JULY 1985 – REVISED JUNE 1999

- Bidirectional Transceivers
- Meet or Exceed the Requirements of ANSI Standards TIA/EIA-422-B and TIA/EIA-485-A and ITU Recommendations V.11 and X.27
- Designed for Multipoint Transmission on Long Bus Lines in Noisy Environments
- 3-State Driver and Receiver Outputs
- Individual Driver and Receiver Enables
- Wide Positive and Negative Input/Output Bus Voltage Ranges
- Driver Output Capability . . . ±60 mA Max
- Thermal Shutdown Protection
- Driver Positive and Negative Current Limiting
- Receiver Input Impedance . . . 12 kΩ Min
- Receiver Input Sensitivity . . . ±200 mV
- Receiver Input Hysteresis . . . 50 mV Typ
- Operate From Single 5-V Supply

D OR P PACKAGE
(TOP VIEW)



description

The SN65176B and SN75176B differential bus transceivers are monolithic integrated circuits designed for bidirectional data communication on multipoint bus transmission lines. They are designed for balanced transmission lines and meet ANSI Standards TIA/EIA-422-B and TIA/EIA-485-A and ITU Recommendations V.11 and X.27.

The SN65176B and SN75176B combine a 3-state differential line driver and a differential input line receiver, both of which operate from a single 5-V power supply. The driver and receiver have active-high and active-low enables, respectively, that can be connected together externally to function as a direction control. The driver differential outputs and the receiver differential inputs are connected internally to form differential input/output (I/O) bus ports that are designed to offer minimum loading to the bus when the driver is disabled or V_{CC} = 0. These ports feature wide positive and negative common-mode voltage ranges, making the device suitable for party-line applications.

The driver is designed for up to 60 mA of sink or source current. The driver features positive and negative current limiting and thermal shutdown for protection from line-fault conditions. Thermal shutdown is designed to occur at a junction temperature of approximately 150°C. The receiver features a minimum input impedance of 12 kΩ, an input sensitivity of ±200 mV, and a typical input hysteresis of 50 mV.

The SN65176B and SN75176B can be used in transmission-line applications employing the SN75172 and SN75174 quadruple differential line drivers and SN75173 and SN75175 quadruple differential line receivers.

The SN65176B is characterized for operation from −40°C to 105°C and the SN75176B is characterized for operation from 0°C to 70°C.

Function Tables

DRIVER

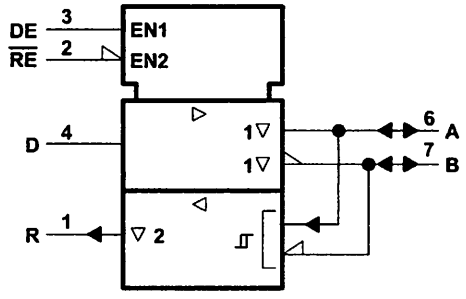
INPUT D	ENABLE DE	OUTPUTS A	OUTPUTS B
H	H	H	L
L	H	L	H
X	L	Z	Z

RECEIVER

DIFFERENTIAL INPUTS A–B	ENABLE $\overline{RE}$	OUTPUT R
$V_{ID} \geq 0.2$ V	L	H
-0.2 V $< V_{ID} < 0.2$ V	L	?
$V_{ID} \leq -0.2$ V	L	L
X	H	Z
Open	L	?

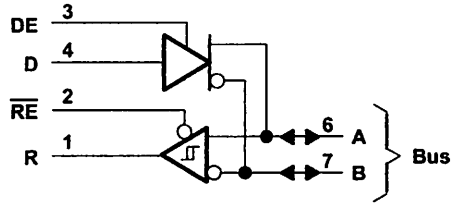
H = high level, L = low level, ? = indeterminate,
X = irrelevant, Z = high impedance (off)

ɟic symbol†

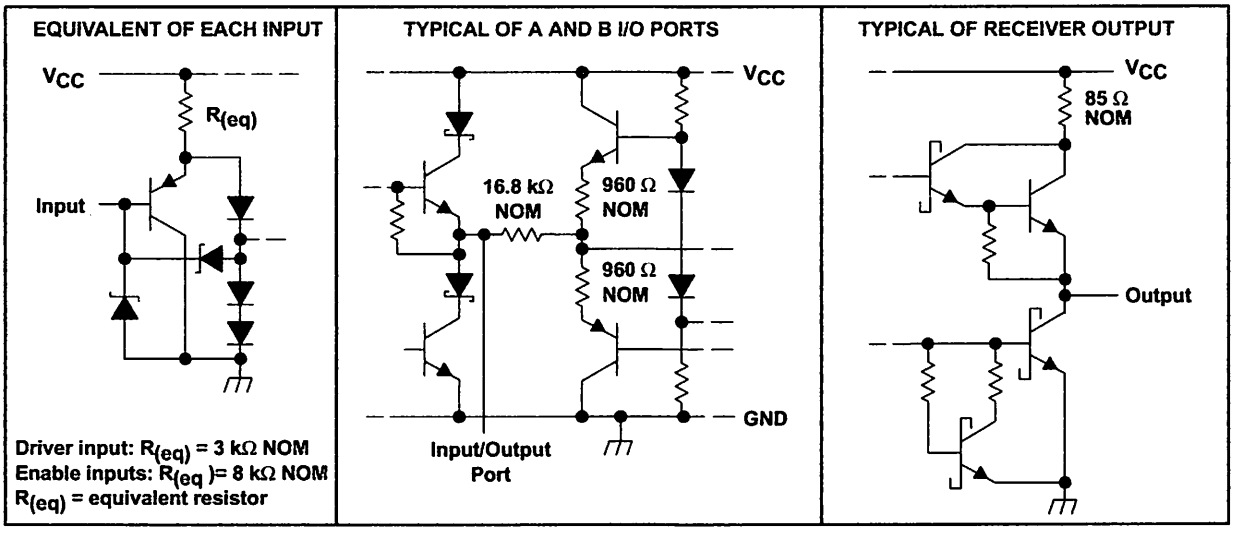


ıis symbol is in accordance with ANSI/IEEE Std 91-1984
ıd IEC Publication 617-12.

logic diagram (positive logic)



schematics of inputs and outputs



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage, V_{CC} (see Note 1) ..... 7 V
Voltage range at any bus terminal ..... −10 V to 15 V
Enable input voltage, V_I ..... 5.5 V
Package thermal impedance, θ_{JA} (see Note 2): D package ..... 197°C/W
P package ..... 104°C/W
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds ..... 260°C
Storage temperature range, T_{stg} ..... −65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. All voltage values, except differential input/output bus voltage, are with respect to network ground terminal.
2. The package thermal impedance is calculated in accordance with JESD 51, except for through-hole packages, which use a trace length of zero.

recommended operating conditions

		MIN	TYP	MAX	UNIT
Supply voltage, V_{CC}		4.75	5	5.25	V
Voltage at any bus terminal (separately or common mode), V_I or V_{IC}				12	V
				−7	
High-level input voltage, V_{IH}	D, DE, and $\overline{RE}$	2			V
Low-level input voltage, V_{IL}	D, DE, and $\overline{RE}$			0.8	V
Differential input voltage, V_{ID} (see Note 3)				±12	V
High-level output current, I_{OH}	Driver			−60	mA
	Receiver			−400	µA
Low-level output current, I_{OL}	Driver			60	mA
	Receiver			8	
Operating free-air temperature, T_A	SN65176B	−40		105	°C
	SN75176B	0		70	

NOTE 3: Differential-input/output bus voltage is measured at the noninverting terminal A with respect to the inverting terminal B.

DRIVER SECTION

ctrical characteristics over recommended ranges of supply voltage and operating free-air nperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS†		MIN	TYP‡	MAX	UNIT
	Input clamp voltage	I_I = –18 mA				–1.5	V
	Output voltage	I_O = 0		0		6	V
$\|V_{OD1}\|$	Differential output voltage	I_O = 0		1.5	3.6	6	V
$\|V_{OD2}\|$	Differential output voltage	R_L = 100 Ω,	See Figure 1	1/2 V_{OD1} or 2¶			V
		R_L = 54 Ω,	See Figure 1	1.5	2.5	5	V
V_{OD3}	Differential output voltage	See Note 4		1.5		5	V
$\Delta\|V_{OD}\|$	Change in magnitude of differential output voltage§	R_L = 54 Ω or 100 Ω,	See Figure 1			±0.2	V
V_{OC}	Common-mode output voltage					+3 –1	V
$\Delta\|V_{OC}\|$	Change in magnitude of common-mode output voltage§					±0.2	V
	Output current	Output disabled, See Note 5	V_O = 12 V			1	mA
			V_O = – 7 V			–0.8	
	High-level input current	V_I = 2.4 V				20	µA
	Low-level input current	V_I = 0.4 V				–400	µA
I_{OS}	Short-circuit output current	V_O = –7 V				–250	mA
		V_O = 0				150	
		V_O = V_{CC}				250	
		V_O = 12 V				250	
I_{CC}	Supply current (total package)	No load	Outputs enabled		42	70	mA
			Outputs disabled		26	35	

e power-off measurement in ANSI Standard TIA/EIA-422-B applies to disabled outputs only and is not applied to combined inputs and outputs.
typical values are at V_{CC} = 5 V and T_A = 25°C.
V_{OD}| and $\Delta|V_{OC}|$ are the changes in magnitude of V_{OD} and V_{OC}, respectively, that occur when the input is changed from a high level to a low el.
e minimum V_{OD2} with a 100-Ω load is either 1/2 V_{OD1} or 2 V, whichever is greater.
ES: 4. See ANSI Standard TIA/EIA-485-A, Figure 3.5, Test Termination Measurement 2.
5. This applies for both power on and off; refer to ANSI Standard TIA/EIA-485-A for exact conditions. The TIA/EIA-422-B limit does not apply for a combined driver and receiver terminal.

itching characteristics, V_{CC} = 5 V, R_L = 110 kΩ, T_A = 25°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
t_{PD})	Differential-output delay time	R_L = 54 Ω,	See Figure 3		15	22	ns
t_D)	Differential-output transition time				20	30	ns
t_{PZH}	Output enable time to high level	See Figure 4			85	120	ns
t_{PZL}	Output enable time to low level	See Figure 5			40	60	ns
t_{PHZ}	Output disable time from high level	See Figure 4			150	250	ns
t_{PLZ}	Output disable time from low level	See Figure 5			20	30	ns

SYMBOL EQUIVALENTS

DATA-SHEET PARAMETER	TIA/EIA-422-B	TIA/EIA-485-A
V_O	V_{oa}, V_{ob}	V_{oa}, V_{ob}
$\|V_{OD1}\|$	V_o	V_o
$\|V_{OD2}\|$	V_t (R_L = 100 Ω)	V_t (R_L = 54 Ω)
$\|V_{OD3}\|$		V_t (Test Termination Measurement 2)
$\Delta\|V_{OD}\|$	$\|\|V_t\| - \|\overline{V}_t\|\|$	$\|\|V_t\| - \|\overline{V}_t\|\|$
V_{OC}	$\|V_{os}\|$	$\|V_{os}\|$
$\Delta\|V_{OC}\|$	$\|V_{os} - \overline{V}_{os}\|$	$\|V_{os} - \overline{V}_{os}\|$
I_{OS}	$\|I_{sa}\|$, $\|I_{sb}\|$	
I_O	$\|I_{xa}\|$, $\|I_{xb}\|$	I_{ia}, I_{ib}

RECEIVER SECTION

electrical characteristics over recommended ranges of common-mode input voltage, supply voltage, and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP†	MAX	UNIT
V_{IT+}	Positive-going input threshold voltage	V_O = 2.7 V,	I_O = −0.4 mA			0.2	V
V_{IT-}	Negative-going input threshold voltage	V_O = 0.5 V,	I_O = 8 mA	−0.2‡			V
V_{hys}	Input hysteresis voltage ($V_{IT+} - V_{IT-}$)				50		mV
V_{IK}	Enable Input clamp voltage	I_I = −18 mA				−1.5	V
V_{OH}	High-level output voltage	V_{ID} = 200 mV, See Figure 2	I_{OH} = −400 µA,	2.7			V
V_{OL}	Low-level output voltage	V_{ID} = −200 mV, See Figure 2	I_{OL} = 8 mA,			0.45	V
I_{OZ}	High-impedance-state output current	V_O = 0.4 V to 2.4 V				±20	µA
I_I	Line input current	Other input = 0 V, See Note 6	V_I = 12 V			1	mA
			V_I = −7 V			−0.8	
I_{IH}	High-level enable input current	V_{IH} = 2.7 V				20	µA
I_{IL}	Low-level enable input current	V_{IL} = 0.4 V				−100	µA
r_I	Input resistance	V_I = 12 V		12			kΩ
I_{OS}	Short-circuit output current			−15		−85	mA
I_{CC}	Supply current (total package)	No load	Outputs enabled		42	55	mA
			Outputs disabled		26	35	

† All typical values are at V_{CC} = 5 V, T_A = 25°C.
‡ The algebraic convention, in which the less positive (more negative) limit is designated minimum, is used in this data sheet for common-mode input voltage and threshold voltage levels only.
NOTE 6: This applies for both power on and power off. Refer to EIA Standard TIA/EIA-485-A for exact conditions.

itching characteristics, V_{CC} = 5 V, C_L = 15 pF, T_A = 25°C

	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
H	Propagation delay time, low- to high-level output	V_{ID} = 0 to 3 V, See Figure 6		21	35	ns
L	Propagation delay time, high- to low-level output			23	35	ns
H	Output enable time to high level	See Figure 7		10	20	ns
L	Output enable time to low level			12	20	ns
Z	Output disable time from high level	See Figure 7		20	35	ns
Z	Output disable time from low level			17	25	ns

PARAMETER MEASUREMENT INFORMATION

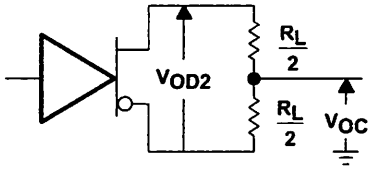


Figure 1. Driver V_{OD} and V_{OC}

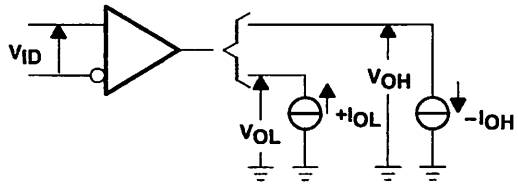
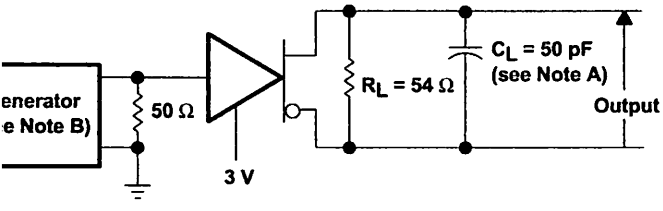
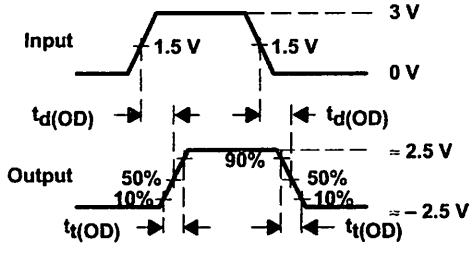


Figure 2. Receiver V_{OH} and V_{OL}



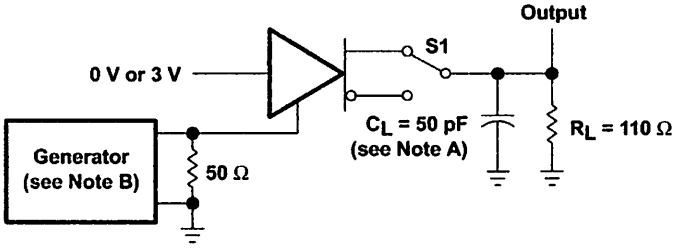
TEST CIRCUIT



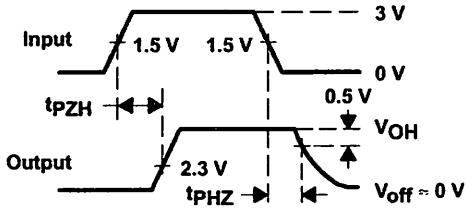
VOLTAGE WAVEFORMS

TES: A. C_L includes probe and jig capacitance.
B. The input pulse is supplied by a generator having the following characteristics: PRR ≤ 1 MHz, 50% duty cycle, t_r ≤ 6 ns, t_f ≤ 6 ns, Z_O = 50 Ω.

Figure 3. Driver Test Circuit and Voltage Waveforms



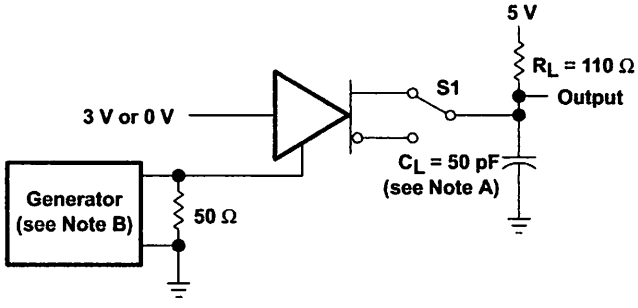
TEST CIRCUIT



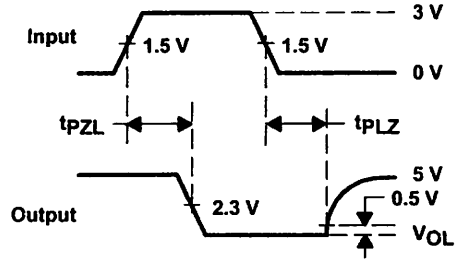
VOLTAGE WAVEFORMS

NOTES: A. C_L includes probe and jig capacitance.
B. The input pulse is supplied by a generator having the following characteristics: PRR ≤ 1 MHz, 50% duty cycle, t_r ≤ 6 ns, t_f ≤ 6 ns, Z_O = 50 Ω.

Figure 4. Driver Test Circuit and Voltage Waveforms



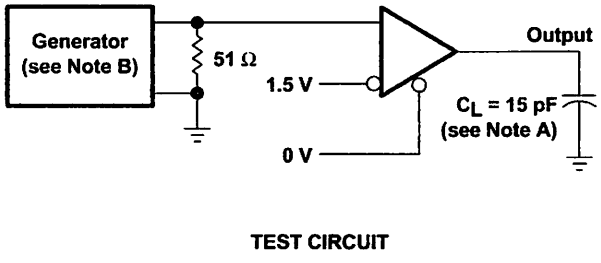
TEST CIRCUIT



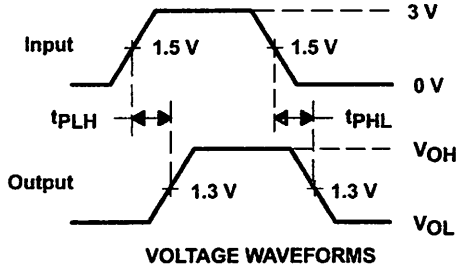
VOLTAGE WAVEFORMS

NOTES: A. C_L includes probe and jig capacitance.
B. The input pulse is supplied by a generator having the following characteristics: PRR ≤ 1 MHz, 50% duty cycle, t_r ≤ 6 ns, t_f ≤ 6 ns, Z_O = 50 Ω.

Figure 5. Driver Test Circuit and Voltage Waveforms



TEST CIRCUIT

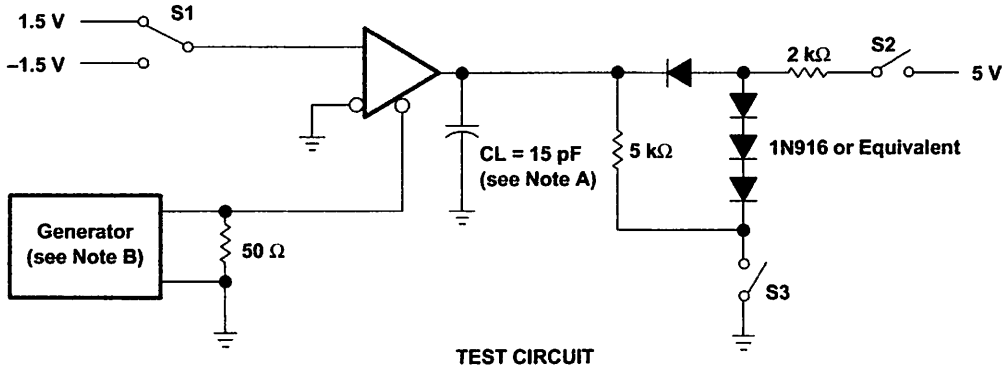


VOLTAGE WAVEFORMS

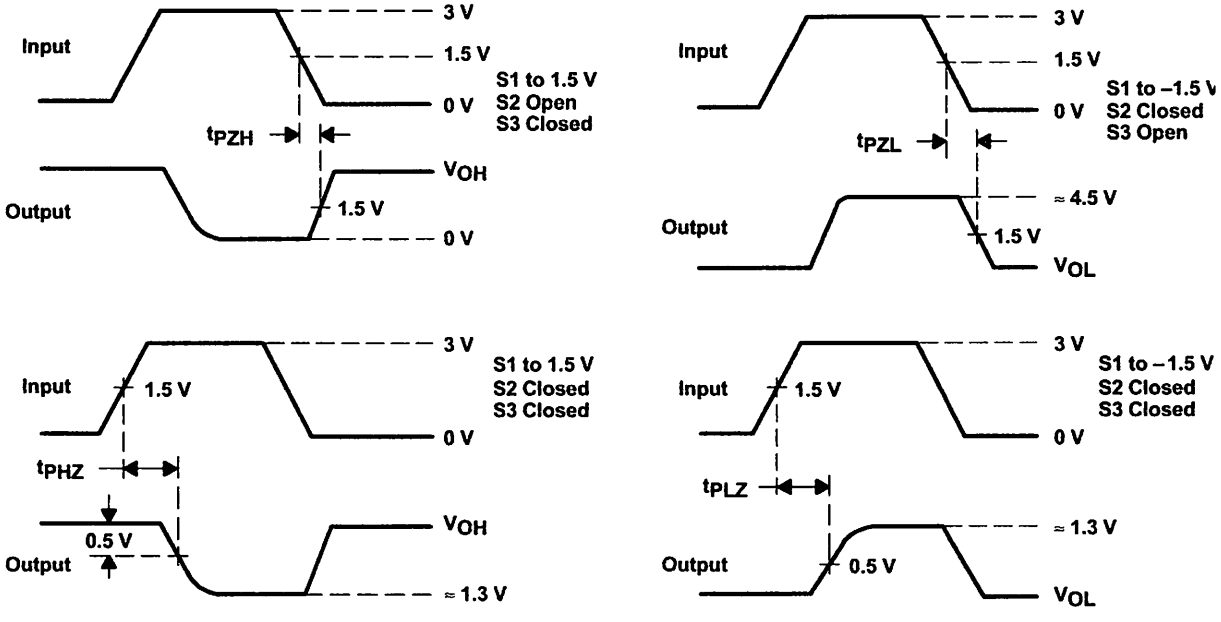
NOTES: A. C_L includes probe and jig capacitance.
B. The input pulse is supplied by a generator having the following characteristics: PRR ≤ 1 MHz, 50% duty cycle, t_r ≤ 6 ns, t_f ≤ 6 ns, Z_O = 50 Ω.

Figure 6. Receiver Test Circuit and Voltage Waveforms

PARAMETER MEASUREMENT INFORMATION



TEST CIRCUIT



VOLTAGE WAVEFORMS

TES: A. C_L includes probe and jig capacitance.
B. The input pulse is supplied by a generator having the following characteristics: PRR ≤ 1 MHz, 50% duty cycle, t_r ≤ 6 ns, t_f ≤ 6 ns, Z_O = 50 Ω.

Figure 7. Receiver Test Circuit and Voltage Waveforms

TYPICAL CHARACTERISTICS

DRIVER
HIGH-LEVEL OUTPUT VOLTAGE
vs
HIGH-LEVEL OUTPUT CURRENT

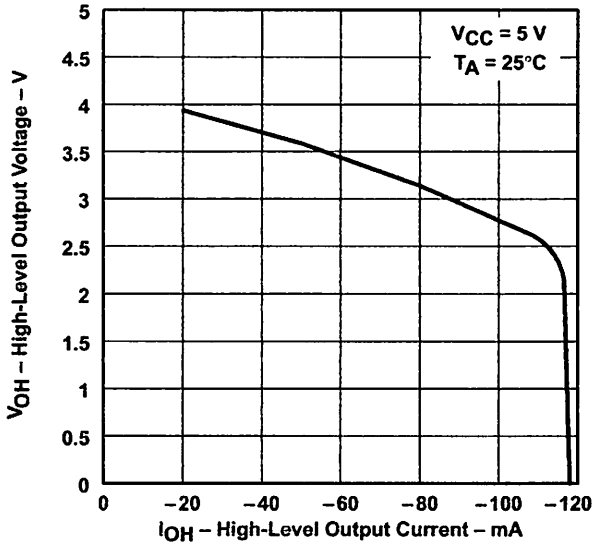


Figure 8

DRIVER
LOW-LEVEL OUTPUT VOLTAGE
vs
LOW-LEVEL OUTPUT CURRENT

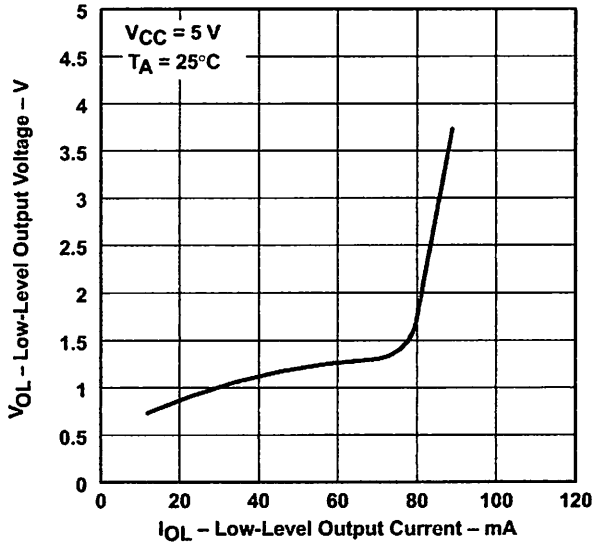


Figure 9

DRIVER
DIFFERENTIAL OUTPUT VOLTAGE
vs
OUTPUT CURRENT

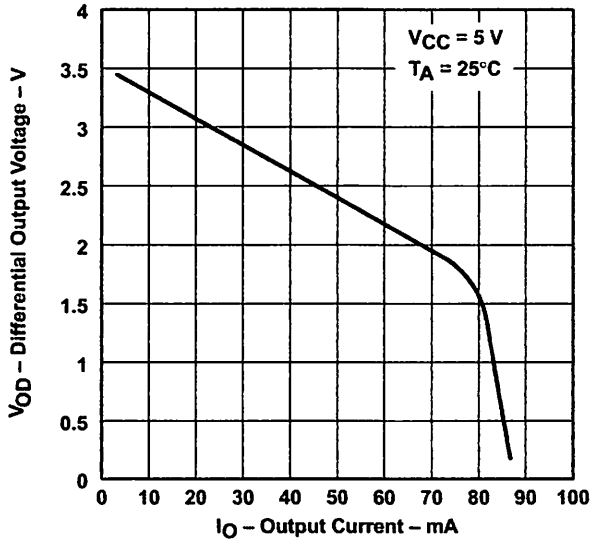


Figure 10

TYPICAL CHARACTERISTICS

RECEIVER
HIGH-LEVEL OUTPUT VOLTAGE
vs
HIGH-LEVEL OUTPUT CURRENT

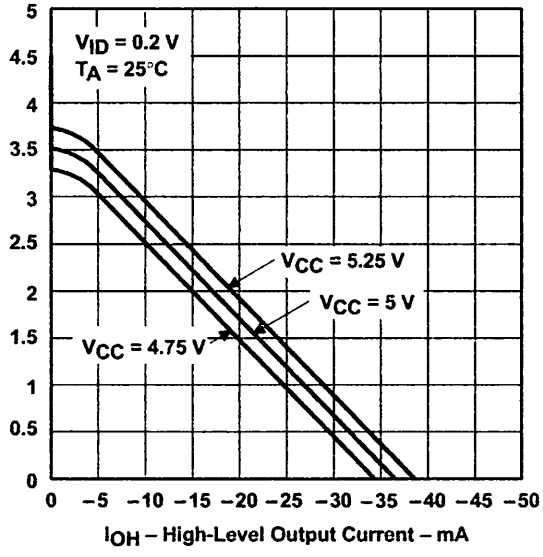
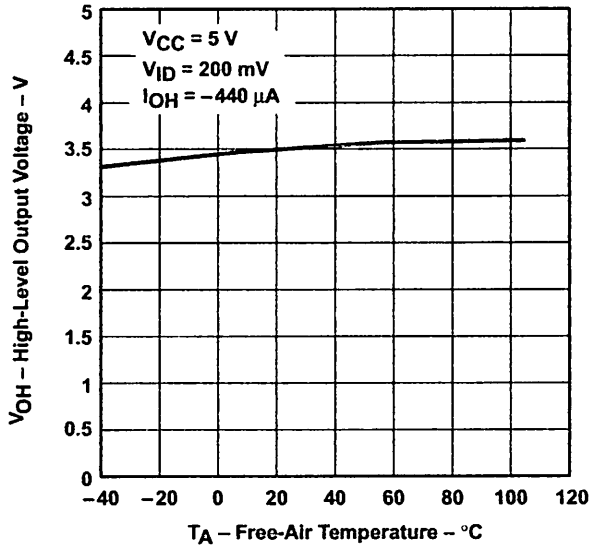


Figure 11

RECEIVER
HIGH-LEVEL OUTPUT VOLTAGE
vs
FREE-AIR TEMPERATURE†



† Only the 0°C to 70°C portion of the curve applies to the SN75176B.

Figure 12

RECEIVER
LOW-LEVEL OUTPUT VOLTAGE
vs
LOW-LEVEL OUTPUT CURRENT

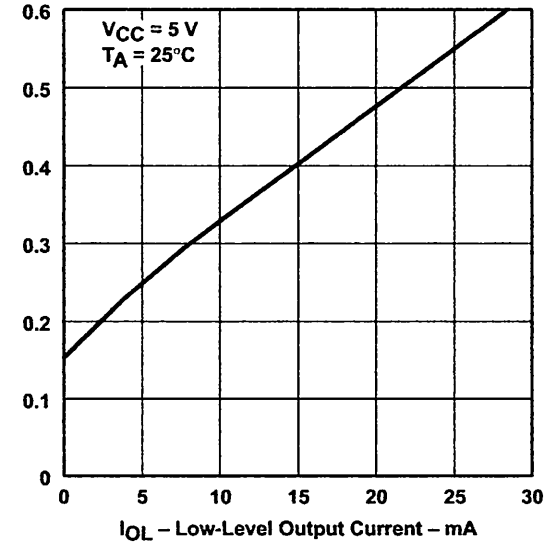


Figure 13

RECEIVER
LOW-LEVEL OUTPUT VOLTAGE
vs
FREE-AIR TEMPERATURE

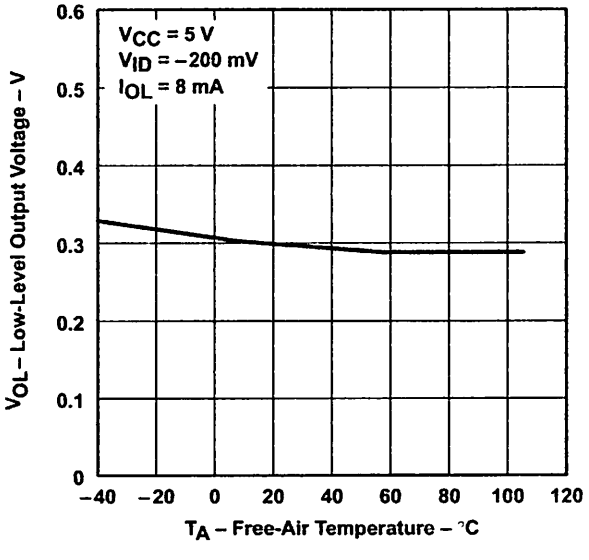


Figure 14

TYPICAL CHARACTERISTICS

RECEIVER
OUTPUT VOLTAGE
vs
ENABLE VOLTAGE

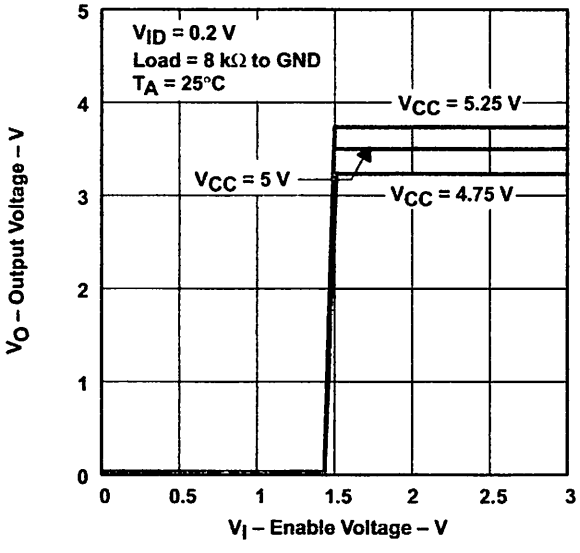


Figure 15

RECEIVER
OUTPUT VOLTAGE
vs
ENABLE VOLTAGE

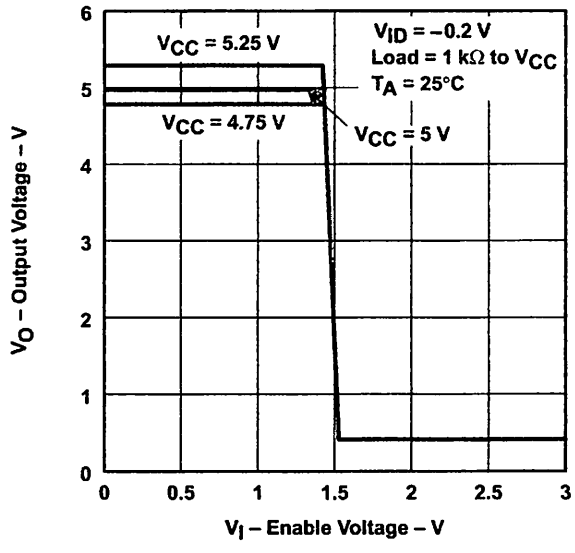
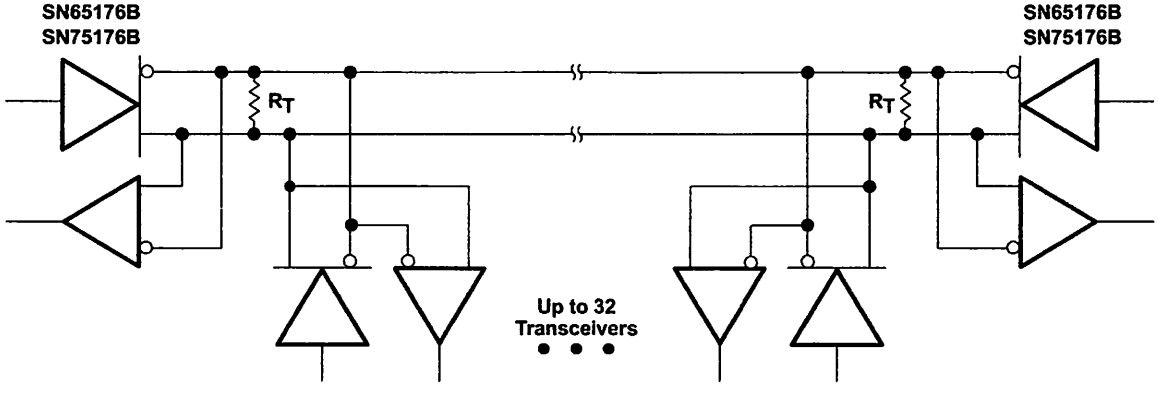


Figure 16

APPLICATION INFORMATION



NOTE A: The line should be terminated at both ends in its characteristic impedance ($R_T = Z_O$). Stub lengths off the main line should be kept as short as possible.

Figure 17. Typical Application Circuit

FAIRCHILD SEMICONDUCTOR™

October 1987
Revised January 1999

CD4094BC
8-Bit Shift Register/Latch with 3-STATE Outputs

General Description

The CD4094BC consists of an 8-bit shift register and a 3-STATE 8-bit latch. Data is shifted serially through the shift register on the positive transition of the clock. The output of the last stage (Q_S) can be used to cascade several devices. Data on the Q_S output is transferred to a second output, Q'_S, on the following negative clock edge.

The output of each stage of the shift register feeds a latch, which latches data on the negative edge of the STROBE input. When STROBE is HIGH, data propagates through the latch to 3-STATE output gates. These gates are enabled when OUTPUT ENABLE is taken HIGH.

Features

- Wide supply voltage range: 3.0V to 18V
- High noise immunity: 0.45 V_{DD} (typ.)
- Low power TTL compatibility:
  Fan out of 2 driving 74L or 1 driving 74LS
- 3-STATE outputs

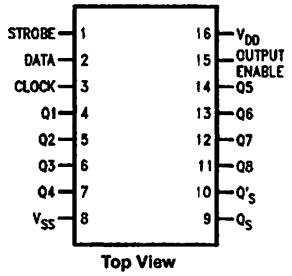
Ordering Code:

Order Number	Package Number	Package Description
CD4094BCWM	M16B	16-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-013, 0.300" Wide
CD4094BCN	N16E	16-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300" Wide

Devices also available in Tape and Reel. Specify by appending the suffix letter "X" to the ordering code.

Connection Diagram

Pin Assignments for DIP and SOIC



Top View

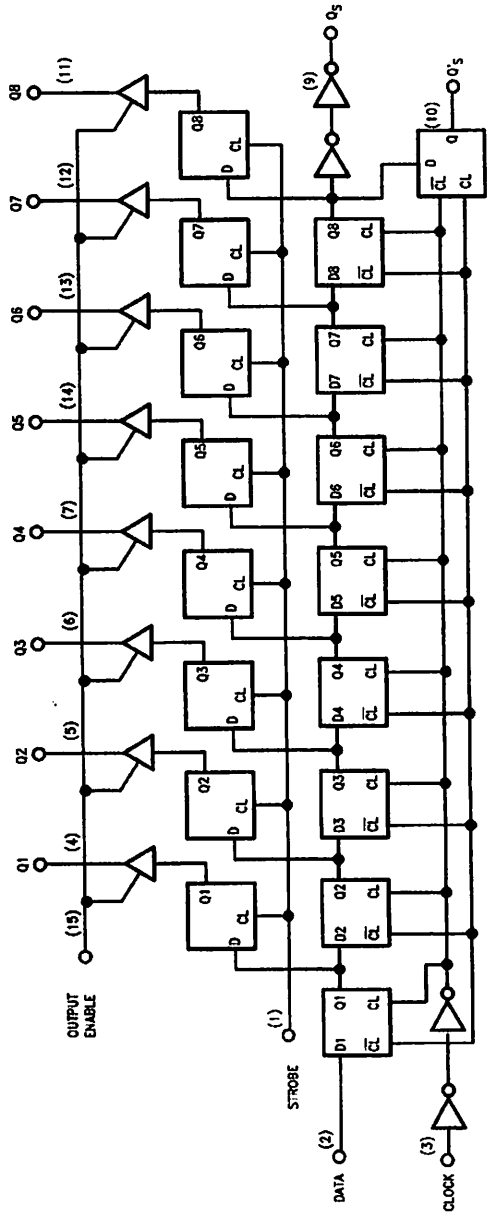
Truth Table

Clock	Output Enable	Strobe	Data	Parallel Outputs		Serial Outputs	
				Q1	Q_N	Q_S (Note 1)	Q'_Σ
↗	0	X	X	Hi-Z	Hi-Z	Q7	No Change
↘	0	X	X	Hi-Z	Hi-Z	No Change	Q7
↗	1	0	X	No Change	No Change	Q7	No Change
↗	1	1	0	0	Q_N-1	Q7	No Change
↗	1	1	1	1	Q_N-1	Q7	No Change
↘	1	1	1	No Change	No Change	No Change	Q7

X = Don't Care
↘ = HIGH-to-LOW
↗ = LOW-to-HIGH

Note 1: At the positive clock edge, information in the 7th shift register stage is transferred to Q8 and Q_S.

Block Diagram



Absolute Maximum Ratings (Note 2)

(Note 3)

Supply Voltage (V_{DD})	−0.5 to +18 V_{DC}
Input Voltage (V_{IN})	−0.5 to V_{DD} +0.5 V_{DC}
Storage Temperature Range (T_S)	−65°C to +150°C
Power Dissipation (P_D)	
Dual-In-Line	700 mW
Small Outline	500 mW
Lead Temperature (T_L)	
(Soldering, 10 seconds)	260°C

Recommended Operating Conditions (Note 3)

DC Supply Voltage (V_{DD})	+3.0 to +15 V_{DC}
Input Voltage (V_{IN})	0 to V_{DD} V_{DC}
Operating Temperature Range (T_A)	−40°C to +85°C

Note 2: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed; they are not meant to imply that the devices should be operated at these limits. The tables of "Recommended Operating Conditions" and "Electrical Characteristics" provide conditions for actual device operation.

Note 3: V_{SS} = 0V unless otherwise specified.

DC Electrical Characteristics (Note 3)

Symbol	Parameter	Conditions	−40°C		+25°C			+85°C		Units
			Min	Max	Min	Typ	Max	Min	Max	
I_{DD}	Quiescent Device Current	V_{DD} = 5.0V		20			20		150	μA
		V_{DD} = 10V		40			40		300	μA
		V_{DD} = 15V		80			80		600	μA
V_{OL}	LOW Level Output Voltage	V_{DD} = 5.0V		0.05		0	0.05		0.05	V
		V_{DD} = 10V $\lvert I_O \rvert \le 1.0$ μA		0.05		0	0.05		0.05	V
		V_{DD} = 15V		0.05		0	0.05		0.05	V
V_{OH}	HIGH Level Output Voltage	V_{DD} = 5.0V	4.95		4.95	5.0		4.95		V
		V_{DD} = 10V $\lvert I_O \rvert \le 1$ μA	9.95		9.95	10.0		9.95		V
		V_{DD} = 15V	14.95		14.95	15.0		14.95		V
V_{IL}	LOW Level Input Voltage	V_{DD} = 5.0V, V_O = 0.5V or 4.5V		1.5			1.5		1.5	V
		V_{DD} = 10V, V_O = 1.0V or 9.0V		3.0			3.0		3.0	V
		V_{DD} = 15V, V_O = 1.5V or 13.5V		4.0			4.0		4.0	V
V_{IH}	HIGH Level Input Voltage	V_{DD} = 5.0V, V_O = 0.5V or 4.5V	3.5		3.5			3.5		V
		V_{DD} = 10V, V_O = 1.0V or 9.0V	7.0		7.0			7.0		V
		V_{DD} = 15V, V_O = 1.5V or 13.5V	11.0		11.0			11.0		V
I_{OL}	LOW Level Output Current (Note 4)	V_{DD} = 5.0V, V_O = 0.4V	0.52		0.44	0.88		0.36		mA
		V_{DD} = 10V, V_O = 0.5V	1.3		1.1	2.25		0.9		mA
		V_{DD} = 15V, V_O = 1.5V	3.6		3.0	8.8		2.4		mA
I_{OH}	HIGH Level Output Current (Note 4)	V_{DD} = 5.0V, V_O = 4.6V	−0.52		−0.44	0.88		−0.36		mA
		V_{DD} = 10V, V_O = 9.5V	−1.3		−1.1	2.25		−0.9		mA
		V_{DD} = 15V, V_O = 13.5V	−3.6		−3.0	8.8		−2.4		mA
I_{IN}	Input Current	V_{DD} = 15V, V_{IN} = 0V		−0.3			−0.3		−1.0	μA
		V_{DD} = 15V, V_{IN} = 15V		0.3			0.3		1.0	μA
I_{OZ}	3-STATE Output Leakage Current	V_{DD} = 15V, V_{IN} = 0V or 15V		1			1		10	μA

Note 4: I_{OH} and I_{OL} are tested one output at a time.