PERENCANAAN DAN PEMBUATAN ALAT PEMANTAU PUTARAN DAN SUHU MESIN SEPEDA MOTOR 4 TAK SILINDER TUNGGAL

TUGAS AKHIR

Disusun Oleh :

Nama : Agung Triono

NIM : 02.57.033

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LEMBAR PERSETUJUAN

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ABSTRAKSI

Perencanaan dan Pembuatan Alat Pemantau Putaran dan Suhu Mesin Sepeda Motor Empat Langkah Silinder Tunggal, AGUNG TRIONO / NIM 02.57.033. 2007., Tugas Akhir Jurusan Teknik Elektro DIII, Program Studi Teknik Elektronika, Fakultas Teknologi Industri, Institut Teknologi Nasional Malang. Dosen Pembimbing Bambang Prio Hartono ST.

Kata kunci : Putaran dan suhu mesin sepeda motor, Sensor suhu LM35, Analog to Digital Converter, Optocoupler, Mikrokontroler

Tachometer atau RPM meter, alat ini sangat membantu para pengendara untuk mengetahui dan mengontrol putaran mesin. Dimana dengan memantau putaran mesin kita akan mengetahui saatnya memindah gigi persnelling pada putaran yang tepat. Selain itu dengan adanya pemantau putaran kita akan lebih mudah dalam menyeting karburator. Penggunaan sepeda motor dengan putaran mesin tinggi dalam waktu yang lama tentu akan menyebabkan suhu mesin meningkat. Penggunaan oli dengan mutu yang buruk selain akan mempercepat ausnya komponen yang bergerak juga akan menyebabkan suhu mesin cepat meningkat pula. Settingan karburator yang tidak pas juga dapat menyebabkan suhu mesin cepat meningkat. Dengan pemasangan sebuah alat pengukur suhu maka pengendara akan mengetahui lebih dini gejala-gejala seperti diatas. Dari latar belakang diatas diperoleh rumusan masalah yaitu bagaimana menggunakan LM35 sebagai sensor panas untuk mendeteksi suhu mesin, bagaimana menggunakan optocoupler untuk mendeteksi putaran pada mesin dengan tujuan membuat alat pengukur putaran dan suhu mesin untuk sepeda motor.

Metodologi penyusunan yang dipakai adalah studi literatur meliputi mencari dan memahami dasar-dasar teori komponen yang dipakai, yaitu LM35, Mikrokontroler, optocoupler, dan ADC. Kemudian perencanaan realisasi alat yang meliputi perencanaan sensor suhu dan penempatanya, ADC dan resolusinya, perencanaan optocoupler sebagai pendeteksi putaran, sistem mikrokontroler, serta penggunaan seven segment sebagai penampil.

Setelah alat direalisasikan maka tahap selanjutnya adalah pengujian dan pembahasan alat, dimana dari hasil pengujian didapat kesimpulan bahwa alat dapat bekerja dengan baik unuk melakukan pengukuran suhu dan putaran mesin dengan tingkat penyimpangan untuk pengukur suhu sebesar 0,66 % dan untuk pengukur putaran sebesar 1,43 %.

KATA PENGANTAR

Alhamdulillah, puji syukur kehadirat Allah yang telah memberikan rahmat, hidayah, dan kekuatan sehingga saya dapat menyelesaikan tugas akhir yang berjudul "Perencanaan Dan Pembuatan Alat Pemantau Putaran dan Suhu Mesin Sepeda Motor 4 Tak Silinder Tunggal" ini dengan lancar. Tugas akhir ini merupakan persyaratan kelulusan Studi di Jurusan Teknik Elektro D-III Konsentrasi Teknik Elektronika ITN Malang dan untuk mencapai gelar ahli madya.

Keberhasilan penyelesaian laporan tugas akhir ini tidak lepas dari dukungan dan bantuan berbagai pihak. Untuk itu penyusun menyampaikan terima kasih kepada :

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Penyusun telah berusaha semaksimal mungkin dan menyadari sepenuhnya akan keterbatasan pengetahuan dalam menyelesaikan laporan ini. Untuk itu penyusun mengharapkan saran dan kritik yang membangun dari pembaca demi kesempurnaan laporan ini.

Harapan penyusun semoga laporan tugas akhir ini memberikan manfaat bagi perkembangan ilmu pengetahuan dan menambah wawasan kita terhadap teknologi khususnya teknologi di bidang elektronika.

Malang, Maret 2007

Penyusun

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Bab I
Pendahuluan

1.1 Latar Belakang

Pada industri otomotif penggunaan perangkat digital berkembang sangat cepat. Salah satunya adalah penggunan speedometer, odometer, dan RPM meter digital. Dibanding dengan peralatan analog jelas perangkat digital ini memberikan keunggulan lebih, terutama pada tingkat keakuratan dan mudahnya dalam pembacaan hasil pengukuran.

Salah satunya adalah penggunaan RPM Meter, alat ini sangat membantu para pengendara untuk mengetahui dan mengontrol putaran mesin. Dimana dengan memantau putaran mesin kita akan mengetahui saatnya memindah gigi persnelling pada putaran yang tepat guna mendapatkan akselerasi yang maksimal. Selain itu dengan adanya pemantau putaran kita akan lebih mudah dalam menyetting karburator.

Penggunaan sepeda motor dengan putaran mesin yang tinggi dalam waktu yang lama tentu akan menyebabkan suhu mesin meningkat. Penggunaan oli dengan mutu yang buruk selain akan mempercepat ausnya komponen yang bergerak juga akan menyebabkan suhu mesin cepat meningkat, terutama penggunaan oli yang sudah melampaui masa pakai. Hal ini dikarenakan komposisi oli menjadi lebih encer dan sedikit berkurang volumenya. Settingan karburator yang tidak pas juga dapat menyebabkan suhu mesin cepat meningkat. Terutama jika komposisi miskin antara bensin dengan udara, hal ini menyebabkan pembakaran yang tidak sempurna dan menimbulkan panas yang berlebihan.

Dari sini kita dapat menyimpulkan bahwa penggunaan RPM meter dan pengukur suhu pada sepeda motor sangat diperlukan. Sayangnya pihak produsen tidak menyertakan peralatan-peralatan tersebut dalam setiap produknya terutama pada sepeda motor tipe bebek, padahal kita tahu bahwa dengan alat tersebut kita akan semakin terbantu untuk mengontrol kinerja dan kondisi dari sepeda motor kita.

Karakteristik mesin dua langkah sangat berbeda dengan mesin empat langkah, ini jelas terlihat pada proses pembakaranya. Pada mesin dua langkah untuk satu kali proses pembakaran mesin hanya membutuhkan dua kali gerakan piston sedangkan pada mesin empat langkah terjadi empat kali gerakan piston. Alat yang direncanakan hanya digunakan pada sepeda motor 4 langkah saja dengan pertimbangan karena sepeda motor dua langkah sudah mulai ditinggalkan oleh konsumen. Sensor putaran mesin dihubungkan dengan kabel busi, dengan pedoman bahwa pada mesin empat langkah silinder tunggal setiap satu letikan busi berarti terjadi putaran sebanyak dua kali pada kruk as-nya (proses hisap, kompresi, pembakaran dan pelepasan). *Mikrokontroler* berfungsi untuk menghitung jumlah pulsa yang terjadi dalam setiap menit, hasil konversinya ditampilkan melalui *Seven Segment.* Sedangkan untuk mendeteksi suhu, sensor panas (LM 35) dipasang pada kalter mesin sebelah kanan (melalui lubang tutup oli). Disini diutamakan untuk mengukur suhu pada ruang *crankcase,* suhu kerja mesin dalam pemakaian normal berkisar antara 70° C - 90° C, sehingga temperatur tersebut masih masuk pada range kerja sensor LM35 (-55° - 150° C).

1.2 Rumusan Masalah

Dalam pembuatan alat ukur ini, rumusan masalah ditekankan pada :

1. Bagaimana merancang dan membuat sensor panas untuk mendeteksi temperatur kerja mesin sepeda motor.
2. Bagaimana menggunakan optocoupler sebagi sensor putaran pada mesin sepeda motor empat langkah silinder tunggal.
3. Bagaimana pengaplikasi alat dilapangan.

1.3 Tujuan

Membuat alat pengukur putaran dan suhu mesin sepeda motor empat langkah silinder tunggal.

1.4 Batasan Masalah

Mengacu pada permasalahan yang ada dan untuk menghindari pembahasan yang melebar maka perencanaan alat pengukur putaran dan suhu mesin ini dibatasi :

1. Alat hanya digunakan pada sepeda motor empat langkah silinder tunggal.
2. Tidak membahas catudaya
3. Catu daya alat diambil dari tegangan aki sepeda motor.
4. Tidak membahas perambatan panas pada logam dan cairan.
5. Pengukuran suhu mesin dilakukan pada ruang *crankcase* (kalter mesin).
6. Tidak membahas konstruksi alat

1.5 Metodologi Penelitian

Metodologi yang digunakan dalam penyusunan tugas akhir ini adalah:

1. Studi literatur

   Memperoleh data dengan cara membaca dan mempelajari buku-buku literatur yang berhubungan dengan penyusunan tugas akhir ini.

2. Perancangan dan pembuatan alat

   Penyusunan tugas akhir ini dilakukan dengan perencanaan dan pembuatan perangkat keras dan perangkat lunak sesuai keperluan mikrokontroler

3. Pengujian alat

   Dilakukan untuk mengetahui apakah alat yang dibuat telah bekerja sesuai dengan perencanaan atau belum.

1.6 Sistematika Penulisan

Tugas akhir ini disusun berdasarkan beberapa faktor teori penunjang serta bagian bagian dari perencanaan piranti system yang dibagi menjadi 6 (enam) bab dan beberapa sub bab. Inti pembahasan penulisan dapat diuraikan sebagai berikut :

BAB I : PENDAHULUAN

Merupakan pendahuluan yang berisikan latar belakang, rumusan masalah, ruang lingkup masalah, tujuan penulisan dan sistematika penulisan .

BAB II : LANDASAN TEORI

Membahas tentang teori teori dasar penunjang perencanaan dan pembuatan alat .

BAB III : METODOLOGI PENELITIAN

Membahas metodologi yang digunakan dalam penulisan beserta perencanaan dan pembuatan alat .

BAB IV : PEMBAHASAN ALAT

Memuat hasil pengujian dan analisa alat yang di buat dan dibandingkan dengan teori yang dibahas sebelumnya.

BAB V : PENUTUP

Memuat kesimpulan dan saran

Bab II
Teori Dasar

Pada bab ini akan dibahas teori-teori dasar yang berkaitan dengan peralatan yang akan dirancang dalam tugas akhir ini, meliputi teori tentang IC AT89C51, sensor suhu LM35, Optocoupler, dan komponen-komponen penunjang lainnya.

2.1. Mesin Empat Langkah Silinder Tunggal

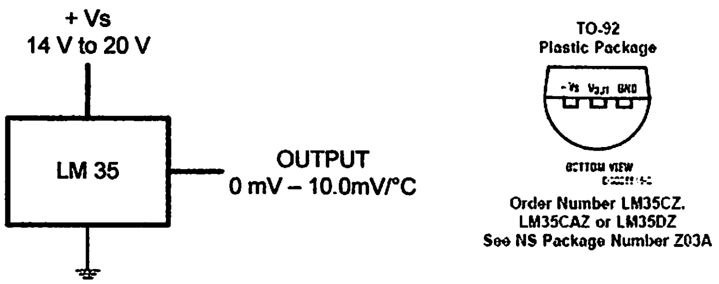
Alat yang direncanakan pada tugas akhir ini akan diaplikasikan pada sepeda motor dengan mesin silinder tunggal tipe empat langkah. Pada mesin 4 tak akan terjadi empat kali gerakan piston dalam melakukan satu kali proses pembakaran, yaitu proses hisap, kompresi, pembakaran, dan pembuangan. Dimana setiap dua kali gerakan piston berarti mesin sudah melakukan putaran sebanyak satu kali pada kruk as nya. Jadi pada mesin empat langkah silinder tunggal setiap satu kali proses pembakaran mesin telah berputar sebanyak dua kali. Hal ini merupakan dasar perhitungan untuk menentukan banyaknya putaran per-menitnya, yaitu :

1 pulsa pada busi / CDI = 2 kali putaran mesin

2.2. Sensor Suhu

Pada pembuatan alat ini digunakan sensor temperatur LM 35 karena linier, murah, dan mudah dalam perencanaannya. Pada dasarnya IC ini merupakan jenis komponen sensor yang output tegangannya sensitif terhadap temperatur.

LM 35 adalah salah satu jenis sensor produksi *National Semiconductor*, yang memiliki jangkauan (*range*) dari -55°C sampai + 150°C. (TL/H/5516 C1995 *National Semiconductor Corporation*)



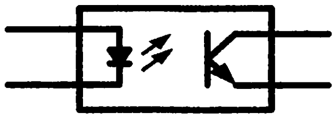
Gambar 2.1. Sensor Suhu LM 35

Sumber National semiconductor corporations, LM35 datasheet

Rangkaian IC sensor ini mampu mengeliminasi kesalahan linier, tetapi kelemahan sensor ini adalah timbulnya kesalahan akibat *self heating*. Untuk mengurangi efek ini adalah dengan cara mengoperasikan IC pada arus minimum namun cukup mendriver sensor dan tahanan (potensiometer) dikalibrasi pada temperatur kerja maksimum. IC ini memiliki output sebesar 10mV/°C. Artinya setiap kenaikan suhu 1°C maka tegangannya bertambah 10mV atau sebaliknya.

2.3. Optocoupler

Optocoupler atau yang juga dikenal sebagai optoisolator yaitu suatu alat yang memancarkan suatu foton yang *flugnya* melalui bahan isolator yang transparan ke jenis detektor. Alat pemancar foton ini dapat berupa lampu pijar neon ataupun LED. Insulator transparan dapat berupa kaca, udara, atau serat optik. Detektornya dapat berupa fotokonduktor, fotodiode, fototransistor, fotoFET, fotoTRIAC, fotoSCR, dan lain sebagainya.



Gambar 2.2. Simbol Optocoupler

Sumber : Fairchild Semiconductor, Phototransistor Optocouplers

Optocoupler dirancang sebagai rangkaian isolasi yang memberikan isolasi tingkat tinggi antara terminal input dan terminal output. Keuntungan dari optocoupler ini adalah sebagai berikut :

a) Kecepatan operasi tinggi.

b) Ukuran kecil,

c) Tahan terhadap getaran dan benturan.

d) Tidak mempunyai bagian bergerak yang dapat saling melekat.

Isolasi merupakan parameter yang penting pada optocoupler. Tiga parameter isolasi kritis adalah resistansi, kapasitas isolasi dan ketahanan dielektrik. Resistansi isolasi adalah resistansi DC dari input ke output dari optocoupler. Resistansi isolasi dengan 10 MΩ adalah umum, nilai ini mungkin lebih tinggi dari pada resistansi antara penempatan dari PCB dimana optocoupler ditempatkan. Oleh sebab itu penanganan PCB harus hati-hati agar tingkat parameter tidak menurun.

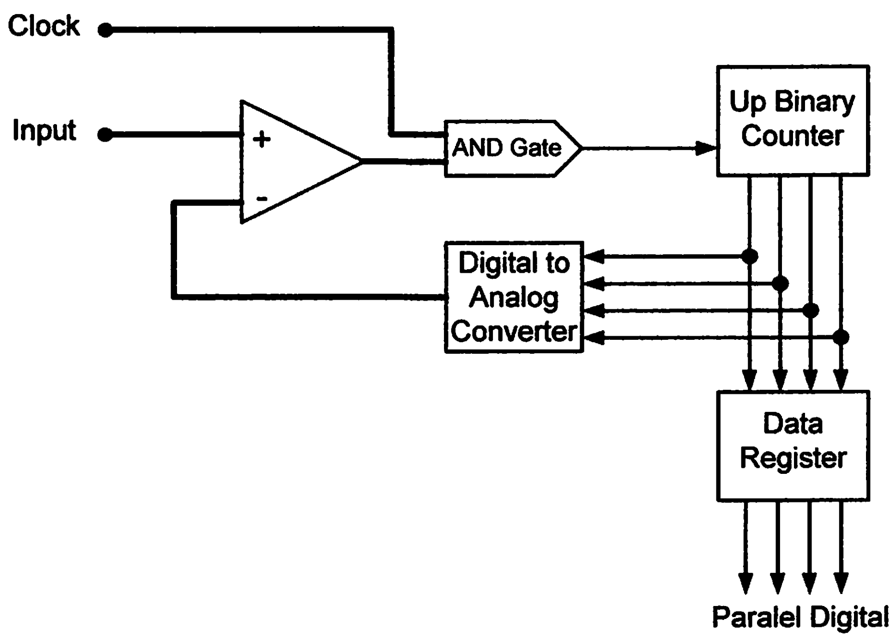
2.4. Analog to Digital Converter (ADC)

2.4.1. Prinsip Dasar ADC

Ada bermacam - macam pengubahan analog ke digital, namun yang paling banyak digunakan adalah ADC jenis pencacah berturut - turut (*Successive Approximation Counter*) sebab memberikan prestasi yang paling baik untuk suatu rangkuman pemakaian yang luas dengan biaya yang pantas.

Rangkaian pembanding (*Comparator*) membentuk dasar dan semua pengubah A/D. Rangkaian ini membandingkan suatu tegangan yang tidak diketahui terhadap sebuah tegangan referensi dan menunjukkan yang mana dari kedua tegangan tersebut lebih besar. Pada dasarnya sebuah rangkaian pembanding adalah penguat selisih tingkat ganda berpenguatan tinggi, dimana keadaan keluaran ditentukan oleh polaritas relalif dan kedua sinyal masukan. Jika misalnya, sinyal masukan A lebih besar dari sinyal masukkan B, tegangan keluaran adalah paling besar dan rangkaian pembanding menghasilkan keluaran (On). Jika sinyal masukan A lebih kecil dan rangkaian pembanding tidak menghasilkan keluaran (Off).

Karena penguat ini mempunyai penguatan yang sangat tinggi, dia saturasi ataupun dihentikan (*cut off*): pada level - level masukkan selisih yang relatif rendah, sehingga dia bertindak sebagai alat biner.



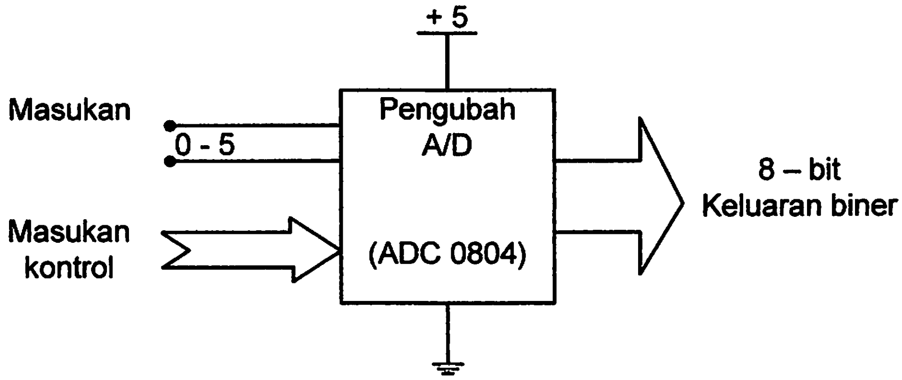
Gambar 2.3. Prinsip Dasar ADC

Sumber : Sumber : www.electroniclab.com, rubrik elka digital

2.4.2. IC ADC 0804

Ada bermacam - macam tipe dari IC ADC. Dengan menggunakan teknologj CMOS modern, banyak gambaran yang dapat ditambahkan terhadap perubahan A/D IC sementara yang penghamburan daya tertahan dan pembayarannya dengan level yang rendah.

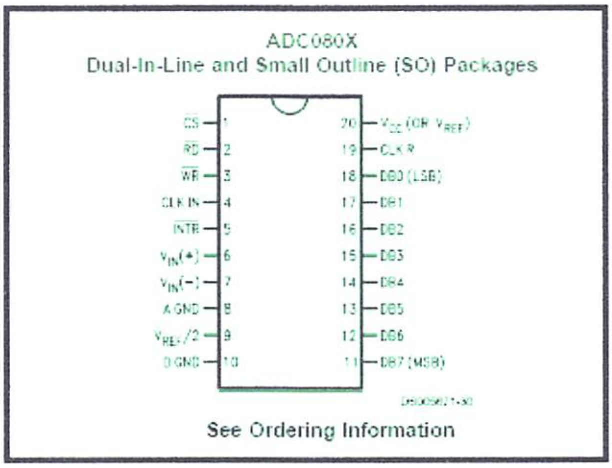
Sebuah Blok sederhana dari ADC 0804 ditunjukkan pada gambar dibawah. Pertama baris pengontrol pengubah A/D secara langsung disample dan didigitalkan dengan tegangan analog pada masukan. Kedua, baris pengontrol pengubah A/D secara langsung membangkitkan 8-bit keluaran biner. Keluaran biner 8-bit adalah langsung disesuaikan terhadap masukan tegangan analog. Jika tegangan masukan 5 Volt maka keluaran biner seharusnya 11111111. Apabila tegangan masukkan 0 Volt, keluaran biner akan 00000000.



Gambar. 2.4. Blok Diagram ADC 0804

Sumber : www.electroniclab.com, rubrik elka digital

Sebuah diagram pin dari A/D IC 0804 Ditunjukkan dalam gambar dibawah. IC ADC 0804 adalah sebuah CMOS 8-bit berurut diperkirakan pengubah A/D dimana perancangannya dioperasikan dengan mikroprosessor 8080A dan microcontroller 89C51 tanpa tambahan Interface. IC pengubah waktu adalah dibawah 100 µs (*micro second*), dan semua masukan dan keluaran adalah TTL yang lengkap.



Gambar 2.5. Diagram Pin ADC 0804

Sumber : National Semiconductor Corporation, ADC 0804 Datasheet

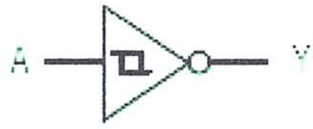
Pengoperasian ADC 0804 dengan catu daya 5 Volt, dan akan dapat menangani secara penuh jarak 0 - 5 Volt masukan analog diantara pin 6 dan 7. IC ADC 0804 mempunyai cip pendetak (clock) dimana hanya memerlukan resistor luar dan kapasitor, dimana untuk clock untuk ADC 0804 antara 600 Hz sampai 1,46 MHz. Resolusi dari ADC 0804 dengan keluaran 8-bit yaitu:

Rcsolusi Vin max: $2^n - 1$ ....(2.1)

2.5. *Schemitt Trigger* 74HC14

Pada dasarnya schemitt trigger adalah suatu rangkaian yang prinsip kerjanya digunakan untuk memperbaiki bentuk dari suatu gelombang tertentu menjadi bentuk gelombang segi empat yang mantap dan stabil. Sedangkan fungsi logika dari *Schmitt trigger* mirip dengan fungsi *inverter* (pembalik), outputnya akan berlogika kebalikanya dari input.

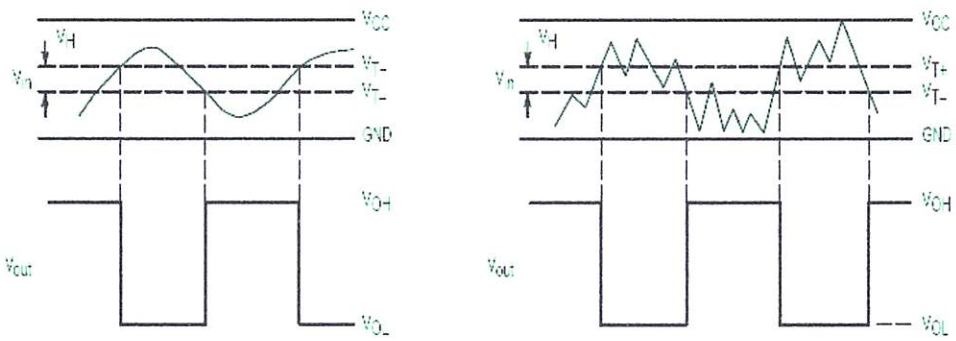
Pada tugas akhir ini digunakan IC 74HC14 dari Motorola yang didalamnya terdapat 6 buah *Scmitt trigger*. IC ini mempunyai tegangan kerja (VCC) antara 2,0 Volt – 6,0 Volt pada pin 14, dan ground pada Pin 7.



Gambar 2.6. Simbol Schemitt Trigger

Sumber : Motorola semiconductor Technical data (74HC14)

Kemampuan *Schemitt Tigger* dalam memperbaiki bentuk gelombang tertentu menjadi gelombang segi empat yang mantap dapat dilihat pada gambar dibawah ini :



Gambar 2.7. Bentuk Gelombang Setelah Melewati Schemitt Trigger

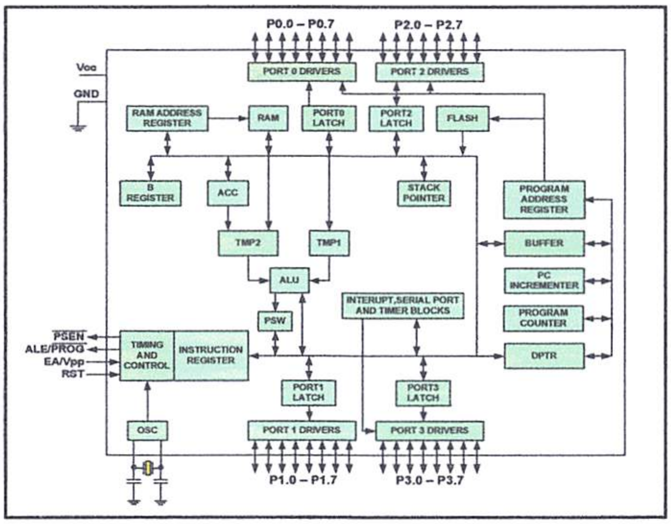
Sumber : Motorola, Shcemitt Trigger Typical Applications (74HC14)

2.6. Keluarga MCS-51

Mikrokontroler Keluarga MCS-51 adalah seperti tabel berikut ini :

Tabel 2.1. Keluarga Mikrokontroler MCS-51

Tipe	Tipe tanpa EPROM	Tipe ber-EPROM	ROM (Byte)	RAM (Byte)	8 bit I/O port	16 bit Timer
8501	8031	-	4K	128	4	2
8501AH	8031AH	8751H 8751BH	4K	128	4	2
80C51	8032AH	8752BH	8K	256	4	3
80C51	80C31BH	87C51	4K	128	4	2
80C52	80C32	-	8K	256	4	3
83C51FA	80C51FA	80C51FA	8K	256	4	3
83C51FB	80C51FB	80C51FB	16K	256	4	3
83C152	80C152	-	8K	256	5	3



Gambar 2.8. Blok Diagram Mikrokontroller AT89C51

Sumber: ATMEL datasheet book, 2

Sebagai suatu sistem kontrol Mikrokontroler 89C51 bila dibandingkan dengan mikroprosesor memiliki kemampuan dan segi ekonomis yang bias diandalkan karena pada mikrokontroler didalamnya sudah terdapat RAM dan ROM sedangkan mikroprosesor didalamnya tidak terdapat kedua-duanya. Secara rinci arsitektur daripada AT89C51 adalah sebagai:

1) 8 bit CPU (Central Processing Unit) dengan register A dan B

2) 16 bit PC (Program Counter) dan DPTR (Data Pointer)

3) 8 bit PSW (Program Status Word)

4) 8 bit SP (Stack Pointer)

5) 4 Kbyte EPROM (Erasable and Programable Read Only Memory)

6) 128 X 8-Bit Internal RAM

7) 32 pin I/O tersusun dari 4 port (masing-masing port 8-bit)

8) 2 buah Timer/Counter 16 Bit

9) Register Control : TCON, TMOD, SCON, PCON, IP dan IE

10) Rangkaian Osilator dan Clock

11) Serial data Transmiterl Receiver (SBUFF)

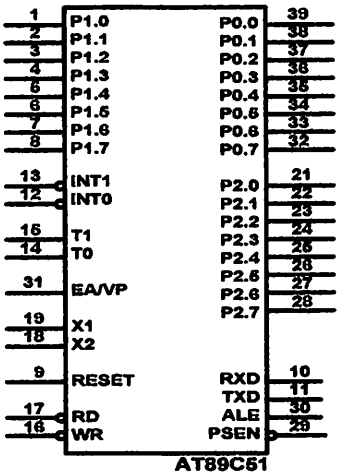
12) 2 buah eksternal interupt dan 3 buah internal interrupt

2.6.1. Mikrokontroler AT89C51

Mikrokontroler AT89C51 merupakan mikrokontroler 8 bit kompatibel dengan standart industri MCS-5FM. baik dari segi pemrograman dan kaki tiap pin, Mikrokontroler 89C51 mempunyai 4 Kbyte PROM (Flash Programmable and Erasable Read Only Memory).

Pada dasarnya Mikrokontroler adalah terdiri dari mikroposesor, timer dan counter, Perangkat I/O dan internal memory. Mikrokontroler Termasuk perangkat yang sudah didesain dalam bentuk chip tunggal. Pada dasamya Mikrokontroler mempunyai fungsi yang sama dengan Mikroprosesor yaitu untuk mengontrol kerja dari suatu system. Selain itu Mikrokontroler juga dikemas dalam satu chip (single chip). Didalam Mikrokontroler juga terdapat CPU, ALU, PC, SP dan register seperti dalam Mikroprosesor, tapi juga ditambah dengan perangkat-perangkat lain seperti ROM, RAM, PIO, SIO, Counter dan sebuah rangkaian clock. Mikrokontroler didesain dengan instruksi-instruksi lebih luas dan 8 bit instruksi yang digunakan membaca data instruksi dari internal memory ke ALU. Banyak instruksi yang digabung dengan pin-pin pada chipnya. Pin tersebut yaitu pin yang dapat diprogram (programable) yang mempunyai fungsi yang berbeda tergantung pada kehendak pembuat program (programer). Sedangkan Mikroprosesor didesain sangat fleksibel dan mempunyai banyak byte instruksi. Semua instruksi bekerja dalam satu konfigurasi perangkat keras yang membutuhkan banyak ruang memory I/O dihubungkan ke alamat dan pin-pin data bus pada chip. Sebagian besar aktifitas pada Mikroprosesor bekerja dengan kode instruksi dan data kepada dan dari memory luar ke CPU.

2.6.2. Fungsi masing-masing Pin AT89C51



Gambar 2.9. Konfigurasi Pin AT89C51

Sumber: ATMEL Datashet book, 1

Fungsi dari masing-masing pin gambar diatas adalah sebagai berikut:

1) VCC

Sumber tegangan positif

2) GND

Ground

3) Port 0

Port 0 merupakan port I/O 8 bit 2 arah. Port ini digunakan sebagai multiplex bus alamat rendah dan bus data selama pengaksesan ke memori luar.

4) Port 1

Port 1 dapat berfungsi sebagai input maupun output dan dapat bekerja baik untuk operasi bit maupun byte, tergantung dari software.

5) Port 2

Port 2 dapat digunakan sebagai bus alamat byte tinggi selama adanya akses ke memory program luar atau memori data luar.

6) Port 3

Pada port 3 ini'mempunyai beberapa fungsi khusus selain sebagai I/O. Beberapa fungsi khusus itu antara lain:

P3.0 : RXD sebagai masukan penerimaan data serial (asynchronous), atau sebagai I/O data (synchronous).

P3.1 :TXD sebagai keluaran pengiriman data untuk serial port asyncronous), atau sebagai clock (synchronous).

P3.2 . INTO sebagai masukan interrupt

P3.3 . INTI sebagai masukan interrupt

P3.4 . TO sebagai masukan dari pewaktu/pencacah 0

P3.5 . T 1 sebagai masukan dari pewaktu/pencacah 1

P3.6 . WR sebagai sinyal penulisan memori data luar

P3.7 . RD sebagai sinyal pembacaan memori data luar

7) RST (Reset)

Mikrokontroler akan reset pada saat pin RST (no.9) diberi logic aktif tinggi.

8) ALE/PROG (Address Latch Enable)/(Pulsa program)

Sinyal digunakan untuk me-latch alamat rendah pada saat pengaksesan memori program luar. Pin ini merupakan pembeda antara data dan program pada lower byte.

9) PSEN (Program Store Enable)

Merupakan sinyal kontrol yang dihubungkan dengan memori program luar selama proses akses. Pada saat mikrokontroler mengeksekusi kode data eksternal program memori, PSEN diaktifkan masing-masing 2 machine cycle.

10) EA/Vpp (Eksternal Akses Enable)

Untuk akses internal program EA- diharuskan terhubung ke Vcc. Sebaliknya untuk akses eksternal EA harus terhubung ke GND.

11) XTAL 1

Sebagai masukan ke penguat osilator dan masukan ke internal clock mikrokontroler.

12) XTAL 2

Keluaran dan penguat osilator. Kaki ini dihubungkan dengan kristal bila menggunakan sumber osilator dari dalam.

2.6.3. Organisasi Memori AT89C51

2.6.3.1. Memori Data Internal

Pada *mikrokontroler* 89C51 terdapat internal memori data. Internal memori data dialamati dengan lebar 1 byte. Lower 128 (00H-7FH) terdapat pada semua anggota keluarga MCS51. Pada lower 128 lokasi memori terbagi atas 3 bagian yaitu:

1) Register Bank 0-3

32 byte terendah terdiri dari 4 kelompok (bank) register, dimana masing-

masing dari kelompok register itu berisi 8 register 8 bit (RO-7) yang masing-masing kelompok register dapat dipilih dengan melalui register PSW. Pada register PSW. RSO dan RSI digunakan untuk memilih kelompok register yang ada.

2) Bit Addressable

16 bit diatas kelompok register tersebut membentuk suatu lokasi blok memori yang dapat dialamati dimulai dari 20H-2FH.

3) Scratch Pad Area

Dimulai dari alamat 30H-7FH yang digunakan untuk inisialisasi alamat bawah dari Stack Pointer. Jika telah diinisialisasi, alamat bawah dari Stack Pointer akan naik ke atas sampai 7FH. Sedangkan pada 128 byte atas (uppwe 128) ditempati oleh suatu register yang mempunyai fungsi khusus yang disebut dengan SFR.

2.6.3.2. Memori Data Eksternal

Untuk mengakses memori program eksternal, pin EA dihubungkan ke ground. 16 jalur I/O (pada port 0 dan port 2) difungsikan sebagai bus alamat port 0 mengeluarkan alamat rendah (Ao - A_7) dari pencacah program (program counter). Pada saat port 0 mengeluarkan alamat rendah, maka sinyal ALE (Address Latch Enable) akan menahan alamat pada pengunci port 2,yang merupakan alamat tinggi (A_8 – A_{15}) yang bersama-sama alamat rendah (A_0 - A_7) membentuk alamat 16 bit. Sinyal PSEN digunakan untuk membaca memori program eksternal:

2.6.4. Register Fungsi Khusus (SFR)

Register dengan fungsi khusus (Spesial Fungsi Register SFR) terletak pada 128 byte bagian atas memori data internal. Wilayah SFR ini terletak pada alamat 80H sampai FFH. Pengalamatan harus khusus diakses secara langsung baik secara bit maupun secara byte. Register-register khusus dalam MC 8031, yaitu:

1) Accumulator (ACC) atau register A dan register B

   Register B: Register im digunakan untuk proses perkalian dan pembagian bersama dengan accumulator.

2) PSW

   Register ini terdiri dari beberapa bit status yang menggambarkan kejadian di accumulator sebelumnya, yaitu carry bit, auxikiary carry, dua buah bit pemilih bank (RSo dan RS1), bendera overflow, parity bit dan 2 buah bendera yang dapat didefinisikan sendiri oleh pemakai. Ada 4 bank yang dapat dipilih untuk digunakan yang semuanya bersifat addressable, yaitu :

Tabel 2.2. Bank Register

RSI	RSO	Register
0	0	BANK 0
0	1	BANK 1
1	0	BANK 2
1	1	BANK 3

Sumber: ATMEL Datashet book

3) SP

Merupakan register 8 bit. Register Sp dapat ditempatkan dalam suatu alamat eksternal maupun internal RAM. Isi register ini ditambah sebelum data disimpan, selama instruksi PUSH dan CALL. Pada saat reset register SP diinisialisasi pada alamat 07H sehingga stack akan dimulai pada alamat 08H.

4) DPTR

Register yang digunakan untuk pengalamatan tidak langsung. Register ini digunakan untuk mengakses memori program baik internal maupun eksternal. RAM juga digunakan untuk alamat eksternal data. DPTR ini dikontrol oleh 2 buah register 8 bit yaitu DPH dan DPL.

5) Register Prioritas Interrupt (Interup Priority /IP)

Merupakan suatu register yang berisi bit-bit untuk mengaktifkan prioritas dari suatu interrupt yang ada pada suatu mikrokontroler pada taraf yang diinginkan.

6) Interrupt Enable Register (ER)

Merupakan register yang berisi bit-bit untuk menghidupkan atau mematikan sumber interrupt.

7) Timer/Counter Control Register (TCON)

Merupakan register yang berisi bit-bit untuk memulai/menghentikan pewaktu/pencacah.

8) Serial Control Buffer (SBUFF)

Register ini digunakan untuk menampung data dari masukan (SBUFF IN) ataupun keluaran (SBUUF OUT) dari serial port.

Berikut ini adalah tabel dari pembagian alamat pada register fungsi-fungsi khusus:

Tabel 2.3. Pembagian Alamat Pada SFR

(Advanced Micro Device, 1998 : 3.6)

SYMBOL	NAME	ADDRESS
*ACC	Accumulator	OEOH
*B	B Register	OFOH
*PSW	Program Status Word	ODOH
SP	Stack Pointer	8IH
DPTR	Data Pointer 2 bytes	
DPL	Low Byte	82H
DPH	High Byte	83H
*PO	Port 0	80H
*Pl	Port 1	90H
*P2	Pon 2	OAOH
*P3	Port 3	080H
*IP	Interupt Priority Control	OB8H
*IE	Interupt Enable Control"	OABH
TMOD	Timer/Counter Mode Control'	89H
"'TCON	Timer/Counter Control	88H
*+ T2CON	Timer/Counter 2 Control	OC8H
THO	Timer/Counter 0 High Control	8CH
TLO	Timer/Counter 0 Low Control	8DH
THI	Timer/Counter 1 High Control	SOH
TLI	Timer/Counter 1 Low Control	8BH
*TH2	Timer/Counter 2 High Control	OCDH
*TL2	Timer/Counter 2 Low Control	OCCH
*RCAP2H	*TIC* Capture Register High Byte	OCBH
+RCAP2L	*TIC* Capture Register Low Byte	OCAH
**SCON*	Serial Control	98H
SBUFF	Serial Data Buffer	99H

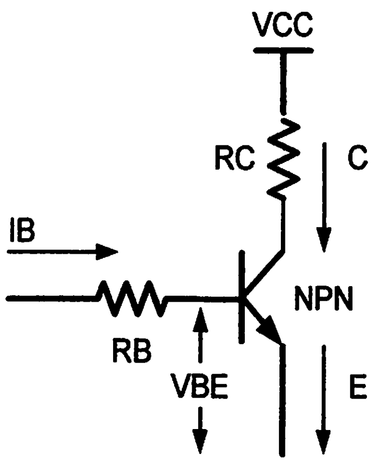
Keterangan tabel :

* = Bit Addresable

+ = 8052 only

2.7. Transistor Sebagai Switching

Rangkaian transistor sebagai switching adalah mengerjakan transistor pada daerah saturasi ketika mendapat sinyal saat melakukan transmitter. Oleh karena itu,diperlukan hfe dari transistor yang cukup besar sehingga arus Ib dapat menyebabkan transistor saturasi. Rangkaian lengkap transistor sebagai switching dapat dilihat pada gambar dibawah ini, Persamaan tentang hal tersebut adalah:



Gambar 2.10. Rangkaian Transistor Sebagai Switching

Sumber : www.electroniclab.com, rubrik elka analog

Persamaan yang dapat diperoleh dari rangkaian diatas adalah:

$$Ib = Vbb - \frac{Vbe}{Rb} \quad (2.2)$$

$$Ic = \frac{Vcc}{Rc} \quad (2.3)$$

Keterangan:

Vcc = tegangan inputan pada kolektor

Vbb = tegangan inputan pada basis

Ic= arus kolektor

Ib= arus basis

Rb= resistansi pada basis

Transistor mempunyai dua keadaan yaitu keadaan kerja jenuh *(saturasi)* dan keadaan tidak bekerja *(cut-off)*. Perubahannya dapat berupa arus atau tegangan. Pada keadaan kerja jenuh *(saturasi)* tegangan kolektor akan menjadi rendah (mendekati nol), dengan demikian arus kolektor akan menjadi sangat besar dan arus yang menuju beban kecil. Pada keadaan tidak bekerja *(cut-off)* tegangan kolektor akan menjadi besar, dengan demikian arus kolektor akan menuju beban. Pada kondisi normal masukannya tidak dibias sehingga titik kerjanya berada pada kondisi *cut-off* dan tidak ada arus yang menuju beban. Apabila transistor masukannya diberikan bias maka arus yang mengalir adalah :.

$$Ib = \frac{Ic}{hfe} \qquad (2.4)$$

Keterangan:

Ib = arus basis

Ie = arus kolektor

Hfe = penguatan transistor

Sedangkan untuk mencari nilai tahanan basis transistor Rb yang berfungsi sebagai pembatas arus maka harga Rb dapat ditentukan dengan rumus :

$$Rb = \frac{(Vbb - Vbe)}{Ib} \qquad (2.5)$$

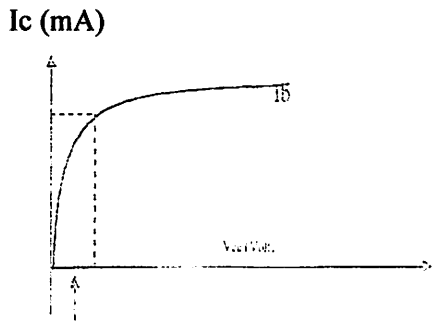
Keterangan :

Rb= tahanan basis

Vhb = tegangan inputan basis

Vbe = tegangan basis emitor

Ib= arus basis



Daerah jenuh saklar
Beroperasi dalam daerah ini

Gambar 2.11. Karakteristik Transistor

Sumber : www.electroniclab.com, rubrik elka analog

Transistor dapat dibuat sebagai saklar elektronik yang memiliki kelebihan-kelebihan dibandingkan dengan saklar mekanik biasa antara lain tidak ada bagian yang bergerak tanpa adanya sobekan *(aus),* tidak ada pengapian kontak bekerja dengan kecepatan tinggi serta biaya yang relatif murah.

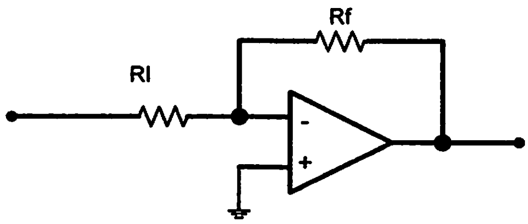
- Penguatannya terkopel langsung (Direct Coupled)
- Impedansi masukan (Zi) = ~ (tak terhingga)
- Impedansi keluaran (Zo) = 0 (nol)
- Penguatan (a) = ~ (tak terhingga)
- Tegangan keluaran 0 (nol), kalau tegangan masukan 0 (nol)
- Tegangan keluaran dapat mengayun ke arah positif maupun ke arah negative

2.8.1. Pemakaian Op-Amp

2.8.1.1. Penguat membalik *(Inverting Amplifier)*

Pada penguat membalik sumber masukan di hubungkan dengan masukan membalik

Gambar rangkaian



Gambar 2.13. Penguat Membalik

Sumber : Texas Instrument, Op Amp for everyone Design Reference, 2002

Penguatan tegangan untuk rangkaian inverting dapat ditentukan dengan :

$$Av = \frac{Voutput}{Vinput} \qquad (2.6)$$

Untuk faktor penguatan dalam modus lup tertutup untuk penguatan membalik dinyatakan dalam :

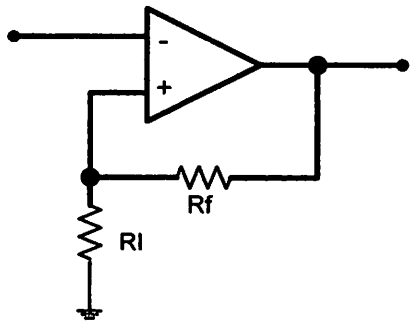
$$Av = \frac{Rf}{Rl} \quad (2.7)$$

Tegangan keluaran diperoleh dengan jalan mengalikan tegangan masukan yang diketahui dengan faktor penguatan:

$$Voutput = -(Av.Vin) \quad (2.8)$$

2.8.1.2. Penguat Tak Membalik *(Non Inverting Amplifier)*

Gambar Rangkaian :



Gambar 2.14. Rangkaian Penguat Tak Membalik

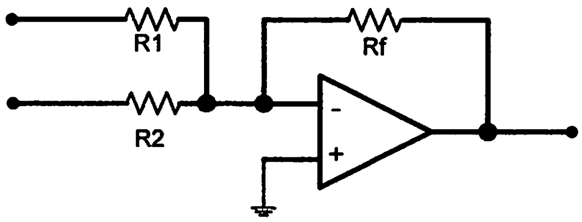
Sumber : Texas Instrument, Op Amp for everyone Design Reference, 2002

Besarnya penguatan tegangan untuk penguat tak membalik yaitu :

$$Av = \frac{Rf}{Rl} + 1 \quad (2.9)$$

2.8.1.3. Op-Amp sebagai penjumlah *(Adder)*

Dengan menggunakan rangkaian penguat membalik dasar dan menambahkan resistor masukan, kita dapat membuat penguat penjumlah membalik, yang ditunjukkan pada rangkaian berikut:



Gambar 2.15. Rangkaian Op-Amp Sebagai Penjumlah

Sumber : Texas Instrument, Op Amp for everyone Design Reference, 2002

$$Voutput = -[\frac{Rf}{R1}V1 + \frac{Rf}{R2}V2] \qquad (2.10)$$

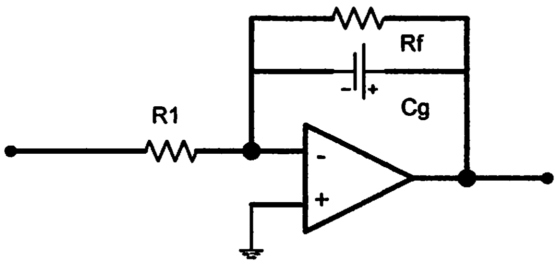
Bila semua resistor luar sama nilainya Rf= Rl = R2 ++Rn keluaran dengan mudah dapat dihitung sebagai penjumlah aljabar dari masing-masing tegangan masukan, atau:

$$Vout = -(V1 + V2 + ... + Vn) \qquad (2.11)$$

2.8.1.4. Op-Amp sebagai Integrator

Rangkaian integrator secara terus menerus mengintegralkan masukan yang akan diukur selama selang waktu yang diberikan.bentuk gelombang keluaran sebanding dengan lamanya waktu sinyal masukan.

Gambar Rangkaian:



Gambar 2.16. Op-Amp Sebagai Integrator

Sumber : Texas Instrument, Op Amp for everyone Design Reference, 2002

Pada rangkaian integrator bekelja pada frekuensi rendah dan mempunyai penguatan sangat tinggi maka dibatasi dengan Rf. Pada rangkaian integrator reaktansi kapasitif berubah terhadap frekuensi. Pada rendah besarnya reaktansi kapasitif bertambah besar, sehingga keluaran tambah besar. Pada frekuensi tinggi besarnya reaktansi kapasitif berkurang, keluaran juga berkurang. Selama tegangan masukan konstan, tegangan keluaran dapat dihitung

menurut rumus:

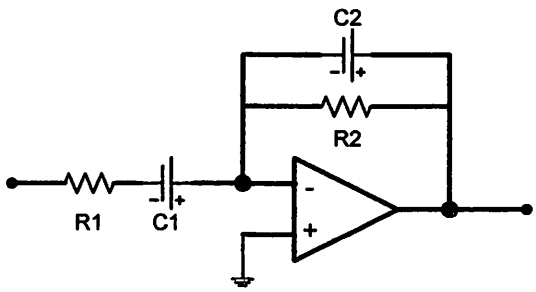
$$Vout = [-\frac{1}{R1.Cf}]\int dVin.dt \qquad (2.12)$$

Tanda-tanda integral menunjukkan batas-batas daerah integrasi yang akan dihitung dengan Vin konstanta dan dt adalah waktu atau periode integrasi. Tanda minus hanya menunjukkan bahwa keluaran berlawanan fasa 1800 terhadap masukannya.

2.8.1.5. Op-Amp Sebagai Differensiator

Kebalikan dari integrator adalah differensiator. Keluaran rangkaian Differensiator sebanding dengan laju perubahan sinyal masukan.

Gambar rangkaian:



Gambar 2.17. Op-Amp Sebagai Differensiator

Sumber : Texas Instrument, Op Amp for everyone Design Reference, 2002

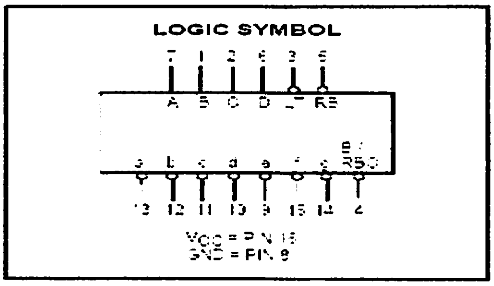
Dengan menggunakan Op-Amp dalam rangkaian Differensiator pada rangkaian diatas, keluaran dapat dibuat sama atau lebih besar dari masukan. Tegangan keluaran dapat dicari menurut rumus:

$$Vout = -Rf.C1\frac{dVin}{dt} \qquad (2.13)$$

Dengan dVin adalah perubahan masukan dan dt adalah perubahan waktu terjadinya. Tanda minus hanya menunjukkan adanya pembalikan fasa.

2.9. Dekoder BCD to Segment IC 74LS47

IC 74LS47 merupakan sebuah dekoder dari BCD ke seven segment yang mempunyai output rendah sehingga 74LS47 kompatibel dengan seven segment common anoda.



Gambar 2.18. Karakteristik IC74LS47

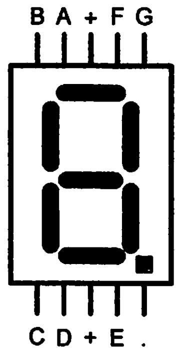
Sumber : Motorola, 74LS47 datasheet

Fasilitas yang ada pada 74LS47 antara lain:

1) LT pad pin 3 berfungsi untuk memeriksa seven segment, saat tidak dioperasikan untuk memeriksa seven segment LT harus dipergunakan tinggi.
2) Ripple Blanking input (RBI) dan Ripple Blanking Output (RBO) yang berfungsi untuk mengontrol penggunaan seven segment.
3) Untuk mengkaskadekan seven segment maka REO dari LSD harus dihubungkan dengan RBI dari MSD.

2.10. Display Seven Segment

Pada dasarnya display seven segment, terdiri dari 7 buah dioda yang disusun membentuk suatu konfigurasi angka. Terdapat 2 macam seven segment, yaitu *common anoda* dan *common katoda.*



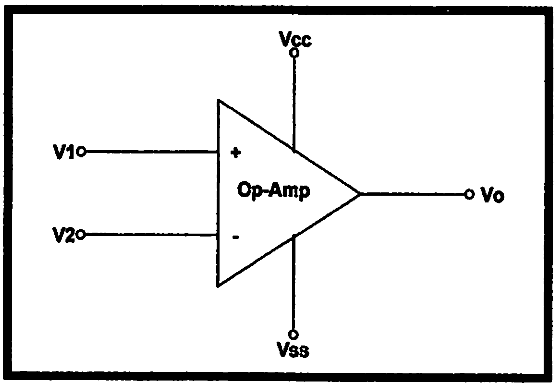
Gambar 2.19. Karakteristik Seven Segment Common Anoda

Sumber : www.electroniclab.com, rubrik elka analog

Pada *common anoda,* berarti bahwa anoda-anoda dari 7 dioda dihubungkan menjadi satu dan diberikan tegangan high sehingga untuk mengaktifkannya pada katodanya diberi inputan tegangan low, Sedangkan pada *common katoda,* katoda-katoda dari dioda dihubungkan menjadi satu dan diberi tegangan low sehingga untuk mengaktifkan seven segment diberikan tegangan input high.

2.8. Operational Amplifier

Penguat Operasional (Op-Amp) merupakan sebuah komponen aktif yang terdiri dari rangkaian penguat gandengan langsung dengan penguatan tinggi yang dalam pengoprasiannya dilengkapi dengan umpan balik untuk memberikan tanggapan secara menyeluruh. Skematis dari Op-Amp diperlihatkan pada gambar 2.12.



Gambar 2.12. Penguat Operasional

Sumber : Texas Instrument, Op Amp for everyone Design Reference, 2002

Penguat ini mempunyai 5 buah terminal dasar, diantaranya 2 buah terminal untuk mensupply daya, 2 buah terminal untuk isyarat masukan, dan 1 buah teminal keluaran. Kedua terminal isyarat masukan masing masing terminal masukan pembalik (inverting input [-]), dan terminal masukan tak membalik (non inverting input [+]).

Jika pada kutub masukan tak membalik V_1 diberi tegangan masukan, maka tegangan keluarannya akan sefasa dengan masukannya. Sebaliknya jika pada kutub masukan membalik V_2 diberi tegangan masukan, maka tegangan keluarannya akan berlawanan fasa dengan masukannya.

Suatu penguat operasional yang ideal memiliki sifat sifat berikut ini :

BAB III
METODOLOGI PENELITIAN

3.1. Studi literatur

Pemasangan alat ukur putaran atau RPM meter *(Tachometer)* pada sepeda motor sangat besar fungsinya. Selain sebagai indikator perpindahan gigi persneling juga akan mempermudah dalam melakukan setting karburator. Pengoperasian mesin dengan putaran tinggi dalam waktu yang lama atau pemakaian gigi persneling yang tidak sesuai dengan putaran mesin, selain dapat menyebabkan peningkatan suhu mesin juga akan memperpendek usia sepeda motor itu sendiri.

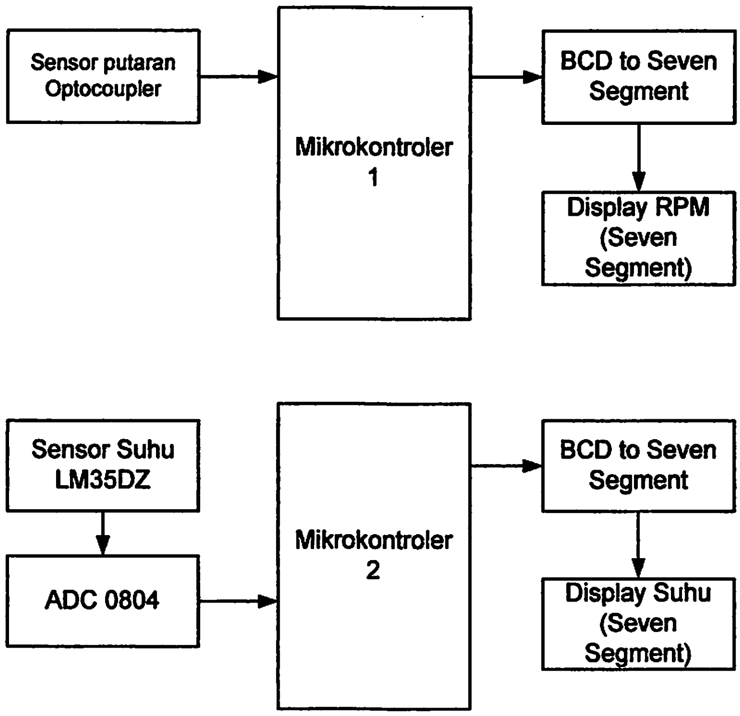
Suhu mesin optimal dari sepeda motor 4 tak berpendingin udara saat digunakan adalah antara 70°C-85°C, dan mesin dikatakan mulai *overheat* jika temperaturnya mencapai 90°C keatas *(RXZ, Tune up sepeda motor dan deteksi piston macet, www.motorplusonline.com).*

Dengan pemasangan alat pemantau putaran dan suhu mesin maka pengendara akan mudah dalam memonitor keadaan sepeda motornya, terutama deteksi dini gejala *overheat* dan seting karburator. Studi literatur juga dilakukan untuk mencari data teknis dari komponen-komponen yang digunakan serta mempelajari teori-teori yang berhubungan dengan prinsip kerja komponen elektronika tersebut, diantaranya: Sensor suhu LM35, ADC 0804, *Optocoupler*, Sistem mikrokontroler, dll.

3.2. Perencanaan dan pembuatan alat

Pada perancangan perangkat keras diperlukan alat atau rangkaian penunjang antara lain rangkaian mikrokontroler AT89C51, sensor temperatur LM35DZ, sensor putaran Optocoupler, rangkaian ADC, dan display seven segment. Sedangkan perangkat lunak, berupa program *software* sebagai pengendali dan pemroses perangkat keras yang telah dirancang.

Adapun blok diagram dari alat yang akan dirancang adalah sebagai berikut



Gambar 3.1. Diagram Blok Sistem

Sumber : Perancangan

Fungsi dari tiap-tiap blok adalah :

- Sensor putaran (*optocoupler*)

  Berfungsi untuk mendeteksi adanya sinyal pada busi sepeda motor.

- Sensor suhu (LM35DZ)

  Berfungsi untuk mendeteksi temperatur ruang *crankcase* mesin sepeda motor.

- ADC *(Analog to Digital Converter)* (ADC0804)

  Berfungsi untuk mengubah data analog dari sensor suhu LM35 menjadi data digital agar dapat diproses oleh mikrokontroler.

- Mikrokontroler 1

  Digunakan untuk memproses data masukan dari optocoupler dan menampilkanya pada seven segment.

- Mikrokontroler 2

  Digunakan untuk memproses data masukan dari ADC dan menampilkanya pada seven segment.

- BCD to Seven segment (7447)

  Berfungsi untuk menterjemahkan 4 bit data biner agar dapat dibaca oleh seven segment

- Display RPM

  Digunakan untuk menampilkan jumlah putaran per menit (RPM) dari mesin.

- Display Suhu

  Digunakan untuk menampilkan besar suhu mesin.

Cara kerja rangkaian :

Untuk mendeteksi temperatur mesin digunakan IC LM35, agar lebih akurat sensor sengaja diletakan didalam kalter mesin sebelah kanan. Selain dapat mendeteksi temperatur oli dan ruang *crankcase*, pada kalter sebelah kanan terdapat lubang tutup oli jadi akan memudahkan untuk memasukan sensor kedalam mesin.

Keluaran IC LM35 merupakan tegangan analog yang besarnya sebanding dengan perubahan temperatur, dengan resolusi sebesar 10mV/°C. Tegangan output yang kecil dan agar setiap perubahanya dapat dideteksi oleh ADC sebesar 1bit maka output sensor dikuatkan dengan menggunakan *op amp*. Oleh ADC tegangan analog tadi diubah dalam bentuk data digital 8bit yang kemudian dihubungkan dengan mikrokontroler untuk diproses dan hasilnya ditampilkan melalui *seven segment*.

Pada mesin 4 tak silinder tunggal setiap satu kali proses pembakaran maka mesin akan berputar sebanyak dua kali pada *crankshaft*-nya. Jadi untuk menghitung jumlah putaran permenitnya digunakan optocoupler. *Optocoupler* disini dihubungkan dengan kabel *pulser* pengapian (*pickup coil*) sehingga setiap terjadi proses pengapian akan terdeteksi dan dapat diproses oleh *software* yang terdapat pada mikrokontroler untuk kemudian hasilnya ditampilkan pada *sevent segment.*

3.3. Pengujian Alat

Dilakukan untuk mengetahui bahwa alat yang telah dibuat sudah sesuai dengan perencanaan atau belum. Tahap ini akan dibahas lebih jauh pada Bab IV.

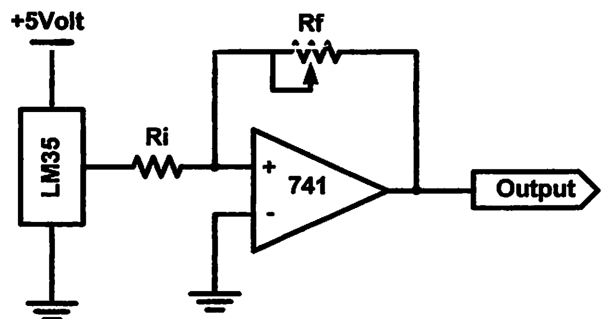
3.4. Perencanaan Dan Pembuatan Perangkat Keras *(Hardware)*

Pada dasarnya alat yang direncanakan terdiri dari dua rangkaian utama yaitu rangkaian pengukur suhu dan rangkaian pengukur putaran. Dimana setiap rangkaian dikontrol oleh satu buah mikrokontroler

3.4.1. Perangkat Keras Rangkaian Pengukur Suhu Mesin

3.4.1.1. Sensor Suhu LM35

Sensor suhu merupakan tranduser yang berfungsi untuk mendeteksi perubahan suhu menjadi sinyal listrik dalam bentuk tegangan. Dalam perencanaan alat ini digunakan IC LM35 keluaran National Semiconduktor sebagai sensor suhu. Sebagai pertimbangan antara lain sederhana rangkaiannya, keluarannya linier terhadap suhu, terkalibrasi secara langsung dalam derajat celcius serta murah dan mudah didapatkan. Rangkaian sensor suhu ditunjukkan dalam Gambar 3.2. Rangkaian ini digunakan untuk mendeteksi temperatur ruang *crankcase.*



Gambar 3.2. Rangkaian Sensor Suhu.

Sumber : Perancangan

Keluaran dari sensor suhu yang berupa sinyal kecil akan dikuatkan oleh *non inverting amplifier* menggunakan op-amp type LM741 yang besar penguatanya dapat diatur dengan tahanan *feedback* nya (Rf).

Besarnya penguat dari penguat *non-inverting* ini akan ditentukan oleh besarnya resolusi pengukuran suhu yang diinginkan. Jika keluaran tegangan dari sensor adalah 10mV/°C *(Datasheet)* maka besar tegangan ini adalah ½ LSB dari resolusi ADC 0804 dengan Vref sama dengan 5Volt, dimana resolusi 1 LSB adalah:

$$\text{Resolusi ADC} = \frac{5volt}{2^8 - 1} = 19{,}6mVolt \approx 20mVolt$$

Agar resolusi suhu menjadi per 1°C dan keluaran dari sensor ditanggapi oleh ADC sebesar 1LSB, maka besar penguatan adalah:

$$A = \frac{Vout}{Vin} = \frac{20mV}{10mV} = 2kali$$

Pada penguat, nilai *Ri* ditentukan sebesar 10 KΩ, maka nilai *Rf* dapat dicari :

$$A_{CL} = \frac{R_F}{R_i}$$

$$2 = \frac{R_F}{10K\Omega}$$

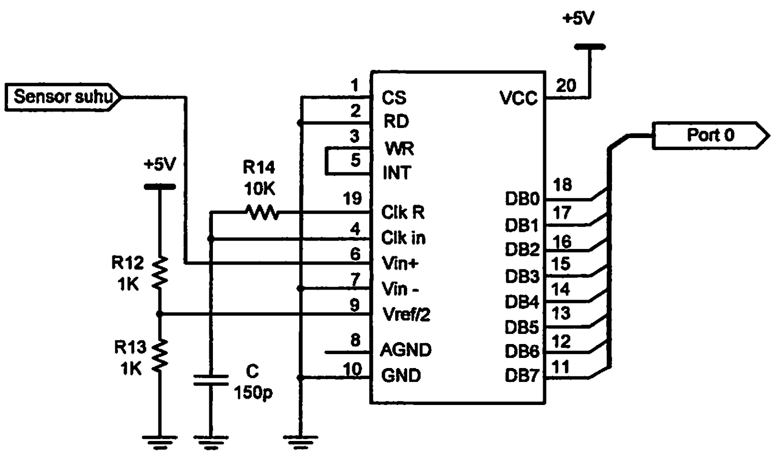
$$Rf = 10K\Omega \text{ x } 2$$

$$Rf = 20K\Omega$$

3.4.1.2. Rangkaian ADC 0804

Agar dapat diproses oleh mikrokontroler maka sinyal yang masuk kedalam mikrokontroler harus merupakan sinyal digital.Untuk itu sinyal dari sensor suhu yang telah diperkuat harus dikonversikan terlebih dahulu menjadi sinyal digital dengan rangkaian ADC. Dalam perancangan ini dipergunakan ADC 0804.

Rangkaian konversi analog ke digital yang mempergunakan ADC 0804 dapat dilihat dalam Gambar 3.3



Gambar 3.3. Rangkaian ADC 0804

Sumber : Perancangan

Rangkaian ADC ini mempunyai 8 bit keluaran (DB0-DB7) yang dihubungkan ke mikrokontroler. Sedangkan masukannya adalah keluaran sensor suhu yang telah diperkuat, yang dihubungkan ke terminal Vin (+). Masukan yang diterima ADC ini dibatasi antara 0 sampai 5 volt *(datasheet)*. Pada pin CS dan RD diberi logika rendah, karena pada pin CS ini akan mengaktifkan ADC 0804 sedangkan untuk pin RD berfungsi agar ADC 0804 secara terus-menerus melakukan pembacaan data dari pendeteksian sensor suhu. Untuk pin INTR dihubungkan juga ke pin WR. Ketika adanya data konversi maka pin INTR akan aktif, dan aktifnya pin ini akan mengaktifkan pin WR yang akan melakukan pemberian atau penulisan data kepada mikrokontroler.

ADC 0804 membutuhkan tegangan referensi per dua (Vref/2) sebesar setengah dari jangkauan masukan analognya. Karena masukan tegangan analog yang direncanakan maksimum sebesar 5Volt maka dibutuhkan tegangan referensi 2,5 Volt. Tegangan ini diperoleh dari pembagi tegangan R12 dan R13. Jika pada R12 dan R13 diberikan resistansi 1 kΩ maka nilai tegangan referensinya.

$$V_{ref} = \frac{R_{13}}{R_{12} + R_{13}} \times V_{masukan\ maksimum} = \frac{1K\Omega}{1K\Omega 0 + 1K\Omega} \times 5\,volt = 2{,}5\,volt$$

ADC 0804 tersebut dapat juga diketahui persen resolusinya. Berdasarkan *data sheet* ADC 0804 mempunyai 8 bit keluaran. Dari bit keluaran yang terdapat pada ADC ini dapat diketahui persen resolusi.

$$\%\,\mathrm{Re}\,solusi = \frac{1}{2^n - 1} \times 100\,\%$$

dimana (n) menyatakan banyaknya jumlah bit keluaran yang terdapat dalam ADC ini.

$$\% \mathrm{Re}\,solusi = \frac{1}{2^8 - 1} \times 100\% = 0{,}392\%$$

Untuk mengetahui kenaikan tegangan setiap *step* (langkah) atau resolusi tegangan yang terdapat pada ADC 0804 ini, dapat dilakukan dengan mengetahui tegangan masukan maksimum yang dapat dideteksi oleh ADC. Berdasarkan *datasheet* tegangan masukan maksimum untuk ADC 0804 adalah sebesar 5volt.

$$\% \mathrm{Re}\,solusi = \frac{Kenaikan\ tegangan\ setiap\ step}{Tegangan\ skala\ penuh} \times 100\%$$

$$0{,}392\% = \frac{Kenaikan\ tegangan\ setiap\ step}{5\,volt} \times 100\%$$

$$Kenaikan\ tegangan\ setiap\ step = \frac{0{,}392\%}{100\%} \times 5\,volt = 19{,}6\,mV \cong 20\,mV$$

Kenaikan tegangan setiap *step* = tegangan resolusi ADC 0804 = 19,6 mV ≅ 20 mV.

Resolusi pembacaan suhu yang dapat dilakukan oleh ADC 0804 dapat diketahui.

$$\Delta T = \frac{\Delta V_T}{\mathrm{Re}\,solusi\ sensor\ suhu}$$

dengan:

ΔT = Resolusi pembacaan sensor suhu (°C)

$$\Delta V_T = \frac{Tegangan\ untuk\ setiap\ perubahan\ 1\ bit\ LSB}{Pengua\tan\,(gain)\ pada\ rangkaian\ penguat} = \frac{20mV}{2} = 10mV$$

Resolusi sensor suhu sebesar 10 mV/°C

Adapun besarnya resolusi pembacaan suhu adalah sebagai berikut :

$$\Delta T = \frac{10mV}{10mV/°C} = 1°C$$

Kerja ADC 0804 akan optimum bila frekuensi clock yang digunakan sebesar kHz (*datasheet*). Dengan menentukan R atau R14 sebesar 10 kΩ dan f sebesar 640kHz maka akan diperoleh nilai C atau C4 sebesar :

$$f = \frac{1}{1{,}1RC}, \text{ nilai } C = \frac{1}{1{,}1 \times 640.10^3 Hz \times 10.10^3 \Omega} = 142.10^{-12} F \cong 150pf$$

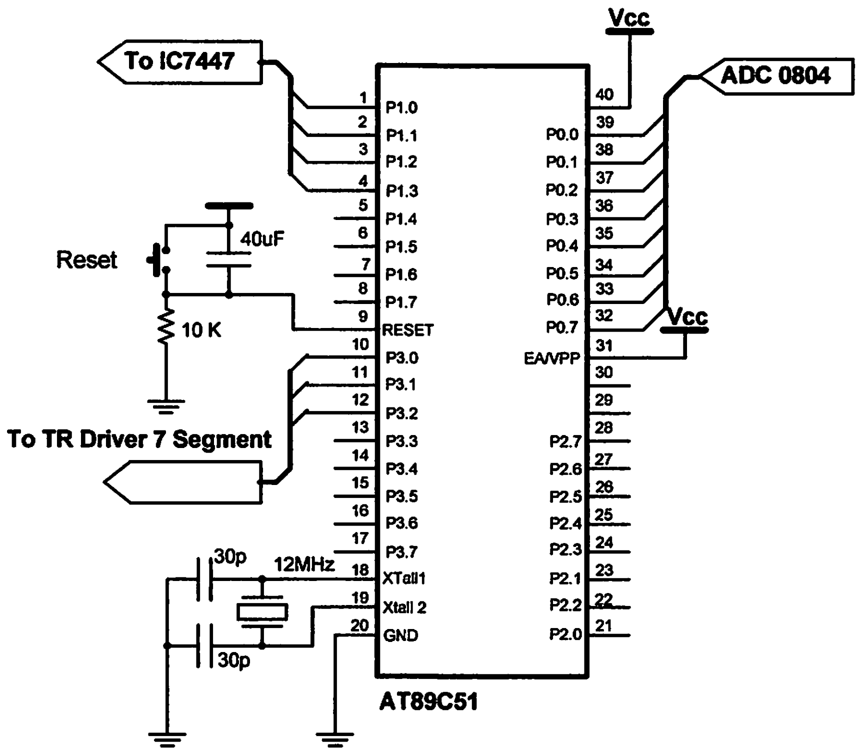
Dari frekuensi clock tersebut maka dapat diketahui pula waktu konversi yang digunakan oleh ADC 0804 dalam melakukan konversi data dari sinyal analog ke sinyal digital. Waktu konversi tersebut didapatkan dari perbandingan terbalik frekuensi yang digunakan dalam ADC 0804 tersebut.

$$Waktu\ konversi = \frac{1}{f_{clock}} \qquad t = \frac{1}{640.10^3} = 1{,}56\,\mu S$$

Dari perhitungan diatas dapat diketahui bahwa waktu konversi yang digunakan ADC ini dalam melakukan konversinya sebesar 1,56μs, dan waktu konversi ini sesuai dengan ketentuan *datasheet* ADC 0804, dimana waktu konversinya tersebut maksimum 100 μs.

3.4.1.3. Sistem mikrokontroler AT89C51

Komponen utama dari rangkaian ini adalah IC AT89C51, dan selanjutnya adalah merencanakan pemakaian tiap-tiap port pada IC tersebut. Perancangan pemakaian port dapat dilihat pada gambar berikut :



Gambar 3.4. Pemakaian Port Mikrokontroler Rangkaian Pengukur Suhu

Sumber : Perancangan

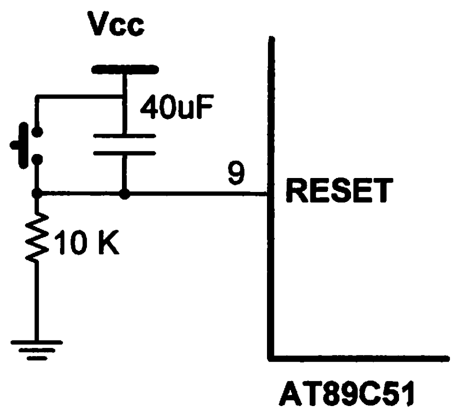
Port-port yang digunakan dalam sistem adalah :

- Pin 32-39 (Port 0.0 – Port 0.7) digunakan sebagai input mikrokontroler dari ADC0804.

- Pin 1-4 (Port 1.0 – Port 1.3) digunakan sebagai output mikrokontroler yang dihubungkan dengan IC7447 *(BCD to Seven Segment).*
- Pin 10-12 (Port 3.0 – Port 3.2) dihubungkan ke transistor *driver seven segment*
- Pin 9 (RESET) ,reset aktif tinggi yang terhubung dengan *power on reset* dan jika diaktifkan maka akan mereset mikrokontroler.
- Pin 18 dan Pin 19 (XTAL1 dan XTAL2) digunakan untuk *clock* sistem mikrokontroler.
- Pin 20 (GND) digunakan sebagai *ground.*
- Pin 40 (VCC) digunakan sebagai tegangan sumber.

3.4.1.3.1. Rangkaian Reset

Untuk mereset mikrokontroler AT89C51, maka Pin 9 (RESET) diberi logika tinggi selama sekurangnya dua siklus mesin (24 periode osilator). Untuk membangkitkan sinyal reset, kapasitor dihubungkan dengan VCC dan sebuah resistor yang dihubungkan dengan *Ground.* Rangkaian reset ditunjukan oleh gambar berikut ini :

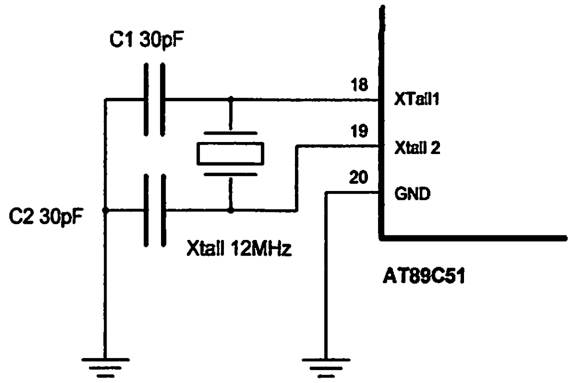


Gambar 3.5. Rangkaian Reset Pada Mikrokonrtroler AT89C51

Sumber : Panduan praktikum mikrokontroler,Rangkaian Reset AT89C51

3.4.1.3.2. Rangkaian *Clock*

Kecepatan proses yang dilakukan mikrokontroler ditentukan oleh sumber *clock* yang mengendalikan mikrokontroler tersebut. Mikrokontroler AT89C51 memiliki *internal clock generator* sebagai sumber *clock* yang diperlukan. Untuk system clocknya dipasang kristal dan dan dua buah kapasitor keramik yang berfungsi sebagai pembangkit clock osilator. Untuk kristal digunakan range antara 2MHz – 26MHz, sedang nilai untuk kapasitor resonator antara 27pF – 33pF. Pada perencanaan dipakai kristal 12MHz dan kapasitor resonator 30pF. Gambar rangkaian reset dapat dilihat pada gambar 3.6



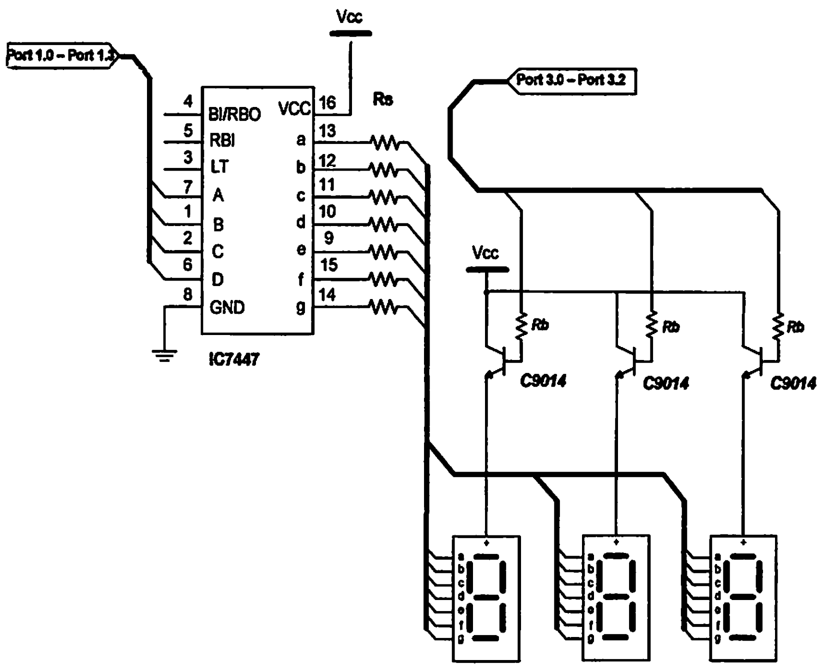
Gambar 3.6. Rangkaian *Clock* Mikrokontroler

Sumber : Panduan praktikum mikrokontroler,Rangkaian Clock AT89C51

3.4.1.4. Rangkaian Driver Seven Segment

Rangkaian ini digunakan untuk mengubah 4 digit data biner dari mikrokontroler agar dapat dibaca kedalam bentuk angka desimal oleh seven segment. Jenis IC yang digunakan adalah tipe SN7447 dari *National Semiconductor.*

Rangkaian *driver seven segment* ditunjukan pada gambar 3.7, dimana output mikrokontroler (Port 0.0 – Port 0.3) digunakan sebagai input IC SN7447. Karena output IC SN7447 Aktif low, maka *seven segment* yang dipakai adalah tipe *Comon Anoda*, sehingga dibutuhkan transistor NPN sebagai driver yang digunakan untuk *switching* dengan tegangan catu dimana tegangan bias basisnya didapat dari output Mikrokontroler (Port 3.0 – Port 3.2).



Gambar 3.7. Rangkaian *Driver Seven Segment*

Sumber : Perancangan

Diketahui tegangan Vcc 5V, dan transistor yang digunakan adalah C9014, *Seven segment* dioperasikan pada tegangan 5V, dan Vbb = 5 volt (logika *high* port mikrokontroler).

Dari *datsheet* transistor (*Data Praktis Elektronika)* diketahui:

Ic maks =500 mA.

β maks = 250

Ib maks = $\frac{Ic}{\beta} = \frac{500}{250} = 2mA$

Ib diset lebih kecil dari Ib maks yaitu sekitar 1,5 mA dengan tujuan menjaga transistor tidak cepat rusak karena bekerja pada keadaan maksimal. Dengan pengesetan nilai-nilai tersebut diharapkan transitor akan bekerja dalam keadaan optimalnya. Sehingga nilai resistansi dan R dapat diketahui yaitu:

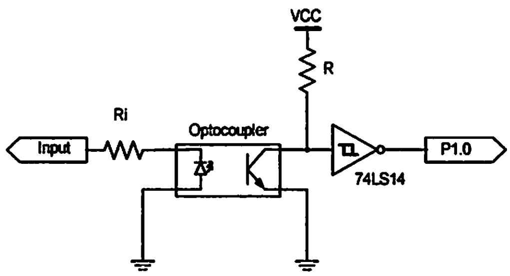
$$Rb=\frac{(Vbb-Vbe)}{Ib}=\frac{5-0.7}{1,5}=2,86.10^3\cong 3K3$$

3.4.2. Perangkat Keras Rangkaian Pengukur Putaran Mesin (*RPM*)

3.4.2.1. Sensor Putaran *Optocoupler* TLP721

Pada sepeda motor empat langkah, setiap satu kali terjadi proses pembakaran maka mesin berputar sebanyak dua kali putaran. Sehingga dengan memasang pendeteksi pengapian pada CDI kita akan mengetahui banyaknya putaran yang terjadi pada saat mesin dinyalakan. Selain sebagai sensor putaran (pendeteksi pengapian) *optocoupler* juga berfungsi sebagai kopling antara jalur tegangan pada pulser CDI dan rangkaian.

Gambar rangkaian sensor putaran dapat dilihat pada gambar dibawah ini :



Gambar 3.8. Rangkaian Sensor Putaran

Sumber : Perancangan

BAB IV
PEMBAHASAN ALAT

4.1. Pengujian Dan Pengamatan Perangkat Keras

Setelah perangkat keras telah selesai dirancang dan dibuat, maka perangkat ini harus diuji terlebih dahulu untuk memastikan alat ini dapat dioperasikan sesuai dengan tujuan perancangan yang diinginkan. Pengujian dan pengamatan dilakukan terhadap sistem pengkabelan, hubungan tiap komponen, tiap blok rangkaian, dan keseluruhan sistem.

Instrumen yang digunakan dalam pengujian ini menggunakan beberapa instrumen diantaranya adalah sebagai berikut:

- Multimeter digital Sunwa DMM CD800.
- Termometer suhu analog.
- LED sebagai indikator kondisi tegangan logika dari diagram blok rangkaian yang dilakukan pengujian dan pengamanan.

Pengujian alat meliputi:

1. Pengujian sensor suhu.
2. Pengujian rangkaian sensor putaran *(optocoupler)*
3. Pengujian rangkaian ADC.
4. Pengujian *driver seven segment*
5. Pengujian sistem secara keseluruhan

4.2. Pengujian Sensor Suhu.

a. Tujuan pengujian.

Pengujian sensor suhu yang menggunakan LM35 bertujuan untuk mengetahui ketepatan sensor dalam merespon perubahan suhu sekitarnya yaitu dengan mengukur tegangan keluarannya. Jika tanggapan sensor suhu baik maka setiap perubahan 1°C keluaran sensor akan berubah ±10 mV.

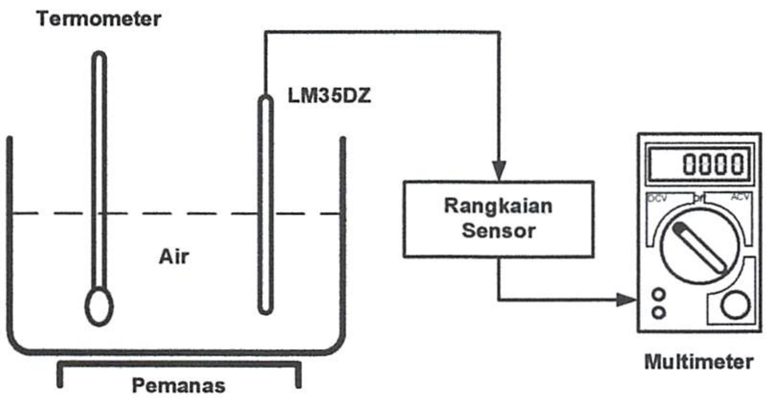
b. Peralatan pengujian.

- Pemanas
- Thermometer
- Catu daya
- Multimeter Digital

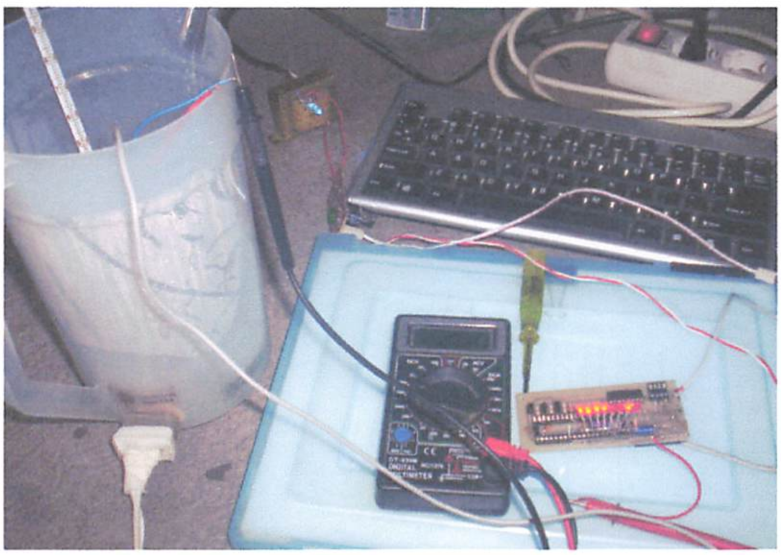
c. Prosedur pengujian

- Menyusun rangkaian pengujian sensor suhu seperti yang ditunjukkan dalam Gambar 4.1.
- Menghubungkan catu daya ke rangkaian pengujian.
- Memasukkan sensor suhu yang sudah diisolasi dengan baik ke dalam bejana berisi air.
- Memasukkan termometer ke dalam bejana untuk mengetahui pembacaan suhu.
- Menaikkan suhu air dengan cara menyalakan pemanas.
- Mengukur tegangan keluaran sensor dengan multimeter digital.

- Pengukuran suhu dimuali dari suhu 25°C -100°C dengan kenaikkan tiap1°C.
- Memasukkan hasil pengujian kedalam Tabel 4.1.



Gambar 4.1 Blok diagram pengujian rangkaian sensor suhu.



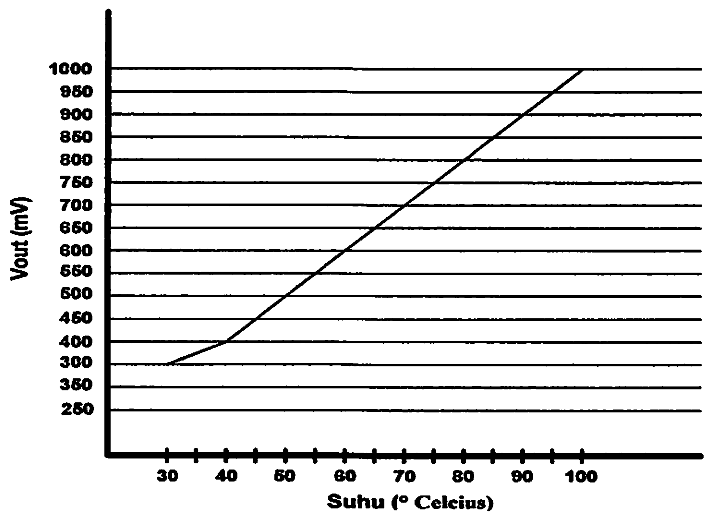
Gambar 4.2. Foto Pengujian Sensor Suhu LM35

d. Hasil pengujian

Tabel 4.1 Hasil Pengujian Sensor Suhu IC LM35

No	Suhu (°C)	Tegangan keluaran pengukuran (mV)	Tegangan keluaran perhitungan (mV)	Penyimpangan (%)
1	25	251	250	0.39
2	26	260	260	0
3	27	272	270	0.73
4	28	283	280	10.6
5	29	285	290	1.72
6	30	299	300	0.33
7	35	346	350	0.86
8	40	398	400	0.50
9	45	452	450	0.44
10	50	501	500	0.20
11	55	556	550	1.07
12	60	601	600	0.16
13	65	658	650	1.21
14	70	701	700	0.14
15	71	711	710	0.14
16	72	724	720	0.55
17	73	728	730	0.27
18	74	735	740	0.67
19	75	750	750	0
20	76	764	760	0.52
21	77	770	770	0
22	78	782	780	0.25
23	79	788	790	0.25
24	80	798	800	0.25
25	81	811	810	0.12
26	82	823	820	0.36
27	83	829	830	0.12
28	84	845	840	0.59

29	85	851	850	0.11
30	86	858	860	0.23
31	87	871	870	0.11
32	88	878	880	0.22
33	89	897	890	0.33
34	90	910	900	1.09
35	91	912	910	0.21
36	92	919	920	0.10
37	93	935	930	0.53
38	94	945	940	0.52
39	95	949	950	0.10
40	96	966	960	0.62
41	97	972	970	2.17
42	98	980	980	0
43	99	988	990	0.20
44	100	996	1000	0.40
Penyimpangan rata-rata				0.66 %



Grafik 4.1. Perubahan Vout Sensor Terhadap Suhu

e. Analisis pengujian

Dari tabel 4.1 bisa dilihat bahwa tegangan keluaran sensor suhu terhadap perubahan suhu adalah linier dan sesuai dengan spesifikasi sensor suhu tersebut. Persentase kesalahan dari hasil pengujian terhadap nilai yang diinginkan dalam perancangan bisa dihitung dengan:

$$Persentase\ penyimpangan = \frac{V_0\ perhitungan - V_0\ pengukuran}{V_0\ perhitungan} \times 100\%$$

Untuk percobaan 1 :

$$PersentasePenyimpangan = \frac{251 - 250}{251} x100\% = 0{,}39\%$$

Dengan cara yang sama dapat dicari nilai persentase kesalahan untuk percobaan-percobaan berikutnya. Sedangkan untuk nilai rata-rata penyimpangan dapat dicari dengan:

$$Penyimpangan\ rata-rata = \frac{\Sigma(\%KesalahanPengukuran)}{BanyaknyaData}$$

$$Penyimpangan\ rata-rata = \frac{29{,}38\%}{44}$$

$$= 0{,}66\%$$

Adanya penyimpangan dikarenakan :

- Sensor suhu LM35 yang digunakan mempunyai nilai akurasi ±0,5°C.
- Pembacaan yang tidak tepat pada termometer karena untuk skala yang lebih kecil dari satu pembacaan akan sulit.

- Tidak presisinya multimeter sehingga menyebabkan kesalahan dalam pembacaan.

4.3. Pengujian Rangkaian ADC 0804.

a. Tujuan pengujian.

Tujuan pengujian rangkaian ADC (*Analog to Digital Converter*) ini adalah untuk menguji kepresisian serta kelinieran ADC dalam mengkonversi tegangan analog ke dalam nilai digital 8 bit.

b. Peralatan yang digunakan

- Sumber tegangan DC variabel
- Multimeter Digital
- Catu daya 5 volt
- LED Display

c. Prosedur pengujian

- Menyusun rangkaian sesuai dengan blok diagram yang ditunjukkan dalam Gambar 4.2.

Diketahui tegangan Vcc 5V, dan transistor yang digunakan adalah C9014, *Seven segment* dioperasikan pada tegangan 5V, dan Vbb = 5 volt (logika *high* port mikrokontroler).

Dari *datsheet* transistor (*Data Praktis Elektronika)* diketahui:

Ic maks =500 mA.

β maks = 250

Ib maks = $\frac{Ic}{\beta} = \frac{500}{250} = 2mA$

Ib diset lebih kecil dari Ib maks yaitu sekitar 1,5 mA dengan tujuan menjaga transistor agar tidak cepat rusak karena bekerja pada keadaan maksimal. Dengan pengesetan nilai-nilai tersebut diharapkan transitor akan bekerja dalam keadaan optimalnya. Sehingga nilai resistansi dan R dapat diketahui yaitu:

$$Rb = \frac{(Vbb - Vbe)}{Ib} = \frac{5-0.7}{1,5} = 2{,}86.10^3 \cong 3K3$$

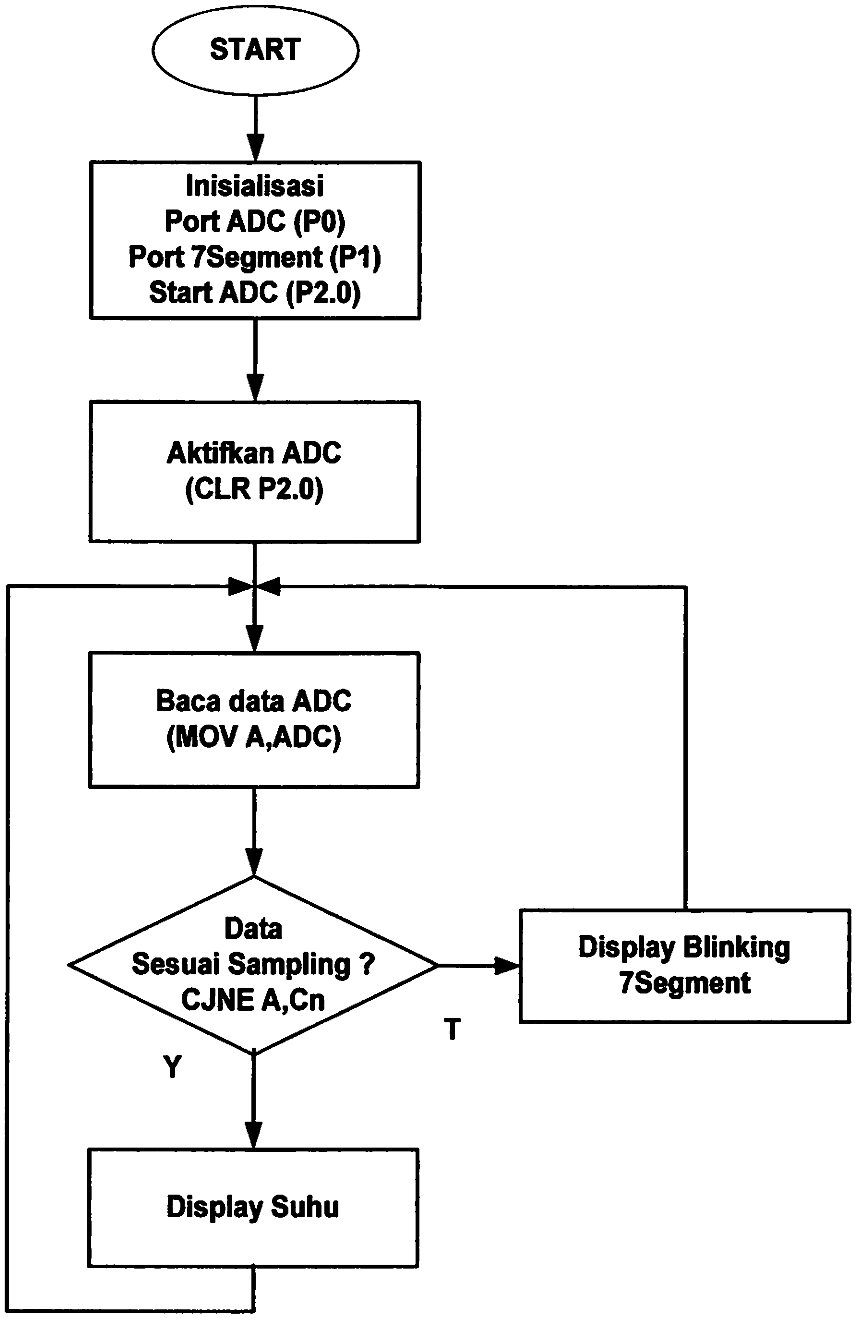
3.5. Perencanaan Dan Pembuatan Perangkat Lunak *(Software)*

Untuk melengkapi dan mendukung perangkat keras (*Hardware*) yang direncanakan, diperlukan perangkat lunak (*Software*) agar perangkat keras yang telah direncanakan dapat berfungsi sesuai dengan yang diinginkan. Pembuatan perangkat lunak terdiri dari dua macam yaitu *software* pengukur suhu dan s*oftware* pengukur putaran mesin

Adapun langkah pembuatan program adalah sebagai berikut :

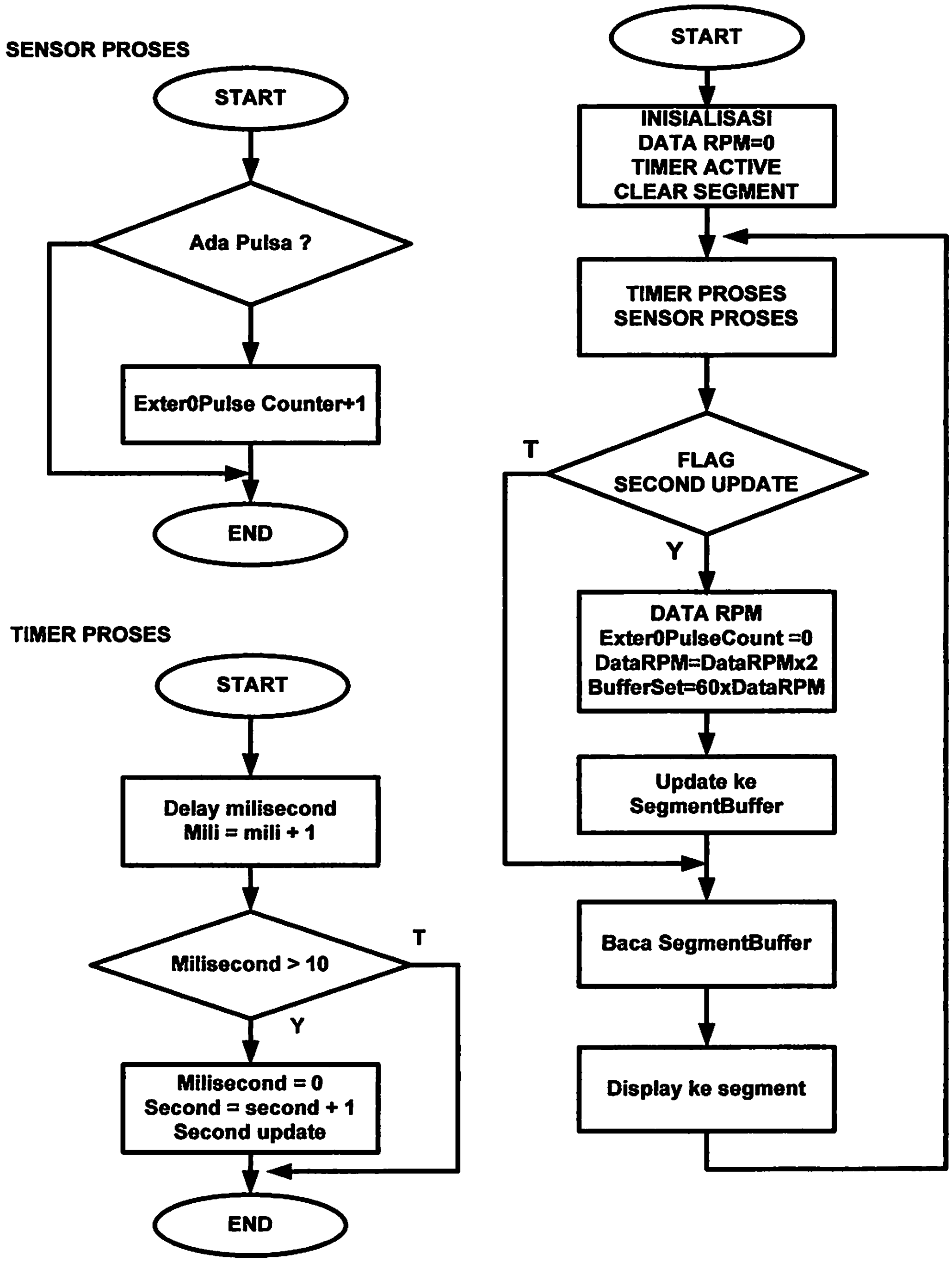
1. Membuat diagram alir (*Flowchart*) dari program yang akan dibuat.
2. Mengubah diagram alir (*Flowchart*) tersebut ke dalam bahasa pemrograman *assembler* sesuai dengan urutan jalannya program.
3. Mengkompilasi program yang dibuat ke memori sampai menghasilkan struktur program yang diharapkan.
4. Memasukkan program yang telah sesuai dengan apa yang diharapkan ke dalam Mikrokontroller AT89C51 dengan menggunakan EEPROM *Programmer.*

Perangkat lunak yang dirancang, dibuat dengan menggunakan bahasa *assembler* Mikrokontroller MCS 51. Seluruh system ini akan bekerja dengan baik apabila perencanaan perangkat lunak (*Software*) sesuai dengan perangkat keras (*Hardware*) yang mendukung



Gambar 3.13. Flowchart Software Pengukur Suhu Mesin

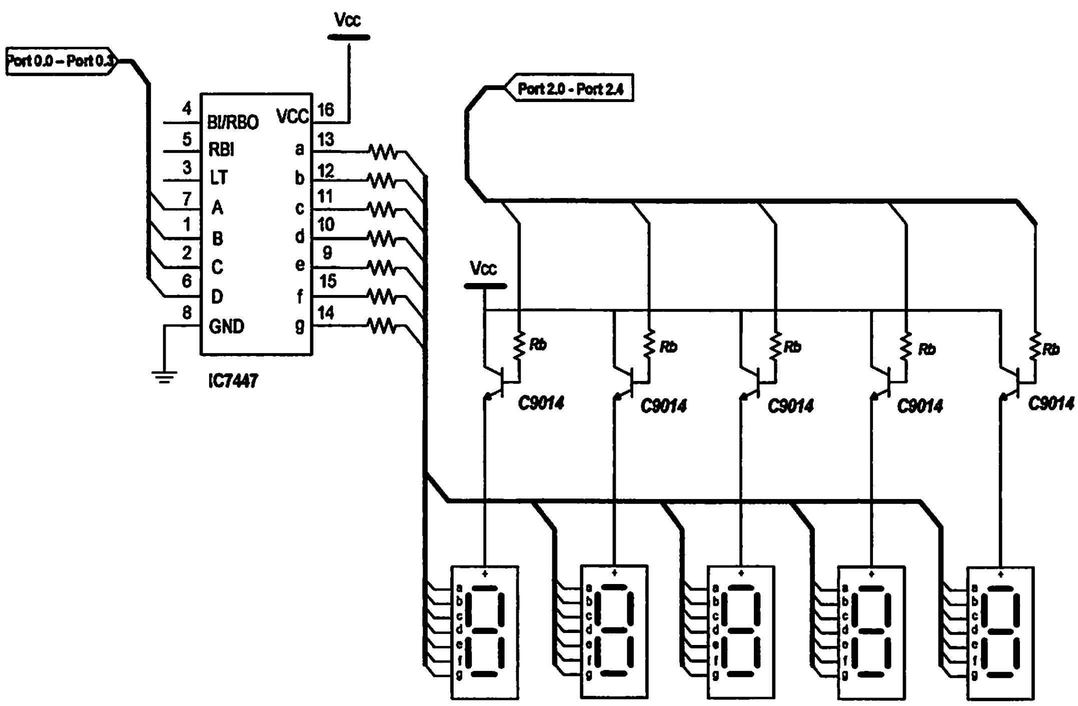
Sumber : Perancangan



Gambar 3.14. Flowchart Software Pengukur Putaran Mesin

Sumber : Perancangan

Rangkaian *driver seven segment* ditunjukan pada gambar 3.7, dimana output mikrokontroler (Port 0.0 – Port 0.3) digunakan sebagai input IC SN7447. Karena output IC SN7447 Aktif low, maka *seven segment* yang dipakai adalah tipe *Comon Anoda*, sehingga dibutuhkan transistor driver yang digunakan untuk *switching* dengan tegangan catu dimana tegangan bias basisnya didapat dari output Mikrokontroler (Port 2.0 – Port 2.4)

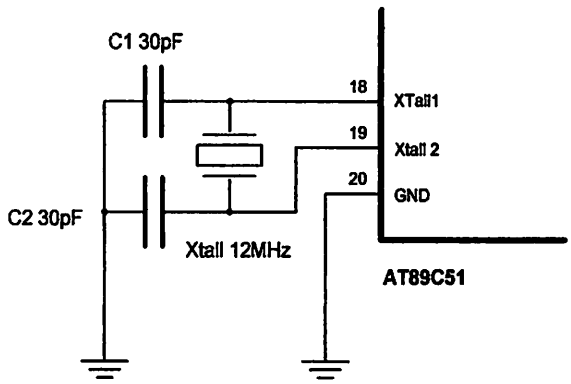


Gambar 3.12. Rangkaian *Driver Seven Segment*

Sumber : Perancangan

3.4.2.2.2. Rangkaian Clock

Kecepatan proses yang dilakukan mikrokontroler ditentukan oleh sumber *clock* yang mengendalikan mikrokontroler tersebut. Mikrokontroler AT89C51 memiliki *internal clock generator* sebagai sumber *clock* yang diperlukan. Untuk system clocknya dipasang kristal dan dan dua buah kapasitor keramik yang berfungsi sebagai pembangkit clock osilator. Untuk kristal digunakan 12 MHz sedang nilai untuk kapasitor resonator adalah 30pF (*Praktikum Mikrokontroler, rangkaian cock)*



Gambar 3.11. Rangkaian *Clock* Mikrokontroler

Sumber : Panduan praktikum mikrokontroler,Rangkaian Clock AT89C51

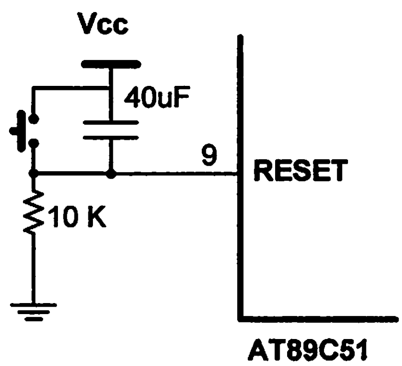
3.4.2.3. Rangkaian Driver Seven Segment

Rangkaian ini digunakan untuk mengubah 4 digit data heksa dari mikrokontroler (Port 0.0 – Port 0.3) agar dapat dibaca kedalam bentuk angka desimal oleh seven segment. Jenis IC yang digunakan adalah tipe SN7447 dari *National Semiconductor.*

- Pin 9 (RESET) ,reset aktif tinggi yang terhubung dengan ***power on reset*** dan jika diaktifkan maka akan mereset mikrokontroler.
- Pin 18 dan Pin 19 (XTAL1 dan XTAL2) digunakan untuk *clock* sistem mikrokontroler.
- Pin 20 (GND) digunakan sebagai *ground*.
- Pin 40 (VCC) digunakan sebagai tegangan sumber.

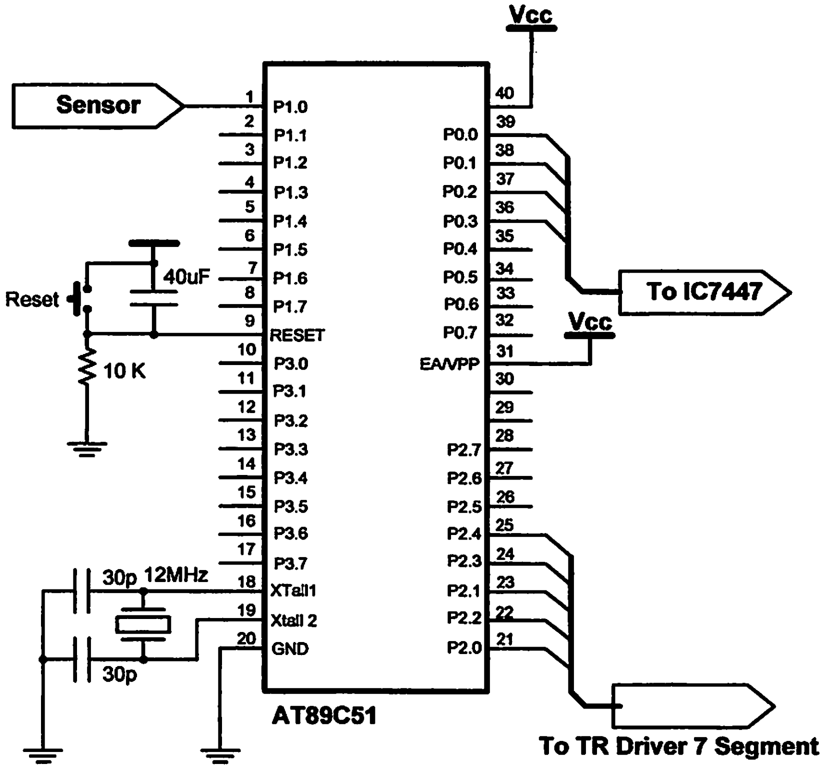
3.4.2.2.1. Rangkaian Reset

Untuk mereset mikrokontroler AT89C51, maka Pin 9 (RESET) diberi logika tinggi selama sekurangnya dua siklus mesin (24 periode osilator). Untuk membangkitkan sinyal reset, kapasitor dihubungkan dengan VCC dan sebuah resistor yang dihubungkan dengan *Ground*. Rangkaian reset ditunjukan oleh gambar berikut ini :



Gambar 3.10. Rangkaian Reset Pada Mikrokonrtroler AT89C51

Sumber : Panduan praktikum mikrokontroler,Rangkaian reset AT89C51



Gambar 3.9. Pemakaian Port Mikrokontroler Pada Rangkaian Pengukur Putaran Mesin

Sumber : Perancangan

Port-port mikrokontroler AT89C51 yang digunakan dalam sistem adalah :

- Pin 1 (Port 1.0) digunakan sebagai input mikrokontroler.
- Pin 36 - 39 (Port 0.0 – Port 0.3) digunakan sebagai output mikrokontroler yang dihubungkan dengan IC7447 *(BCD to Seven Segment).*
- Pin 21 - 25 (Port 2.0 – Port 2.4) dihubungkan ke transistor *driver seven segment*

Rangkaian ini dirancang aktif high, jadi saat tidak ada sinyal input maka output rangkaian akan berlogika low (Gambar 3.8.)

Diketahui tegangan output pulser CDI ±12 Volt, arus *infra led* pada *optocoupler* sebesar 12 mA. Maka besarnya nilai tahanan input (Ri) dapat dicari menggunakan rumus :

$$Iled = \frac{Vin}{Ri}$$

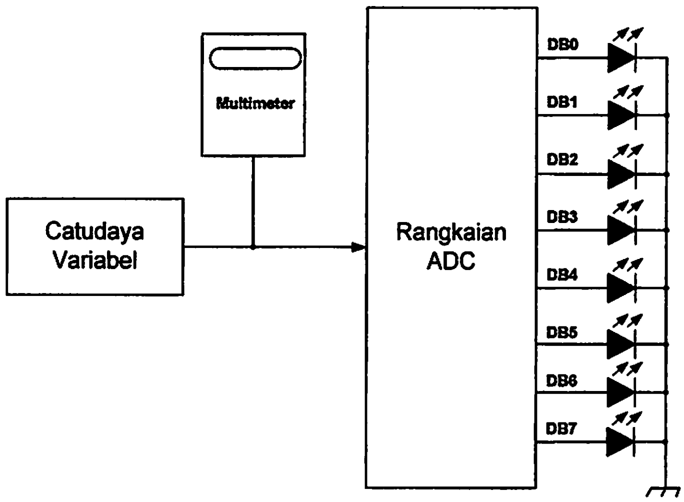
$$Ri = \frac{Vin}{Iled} = \frac{12}{12mA} = 1k\Omega$$

Untuk mendapatkan fungsi aktif low maka diperlukan tahanan R yang menghubungkan input *schemitt trigger* dengan Vcc. Diketahui nilai I max input schemitt trigger sebesar 20mA, maka :

$$R = \frac{Vcc}{I} = \frac{5Volt}{20mA} = 2500\Omega \cong 3{,}3K\Omega$$

3.4.2.2. Sistem Mikrokontroler AT89C51

Komponen utama pada rangkaian ini adalah IC AT89C51 sebagai pengontrol utama pengukuran *RPM* mesin. Untuk selanjutnya adalah merencanakan pemakaian port-portnya, perencanaan pemakaian port dapat dilihat pada gambar 3.9



Gambar 4.3. Pengujian Rangkaian ADC

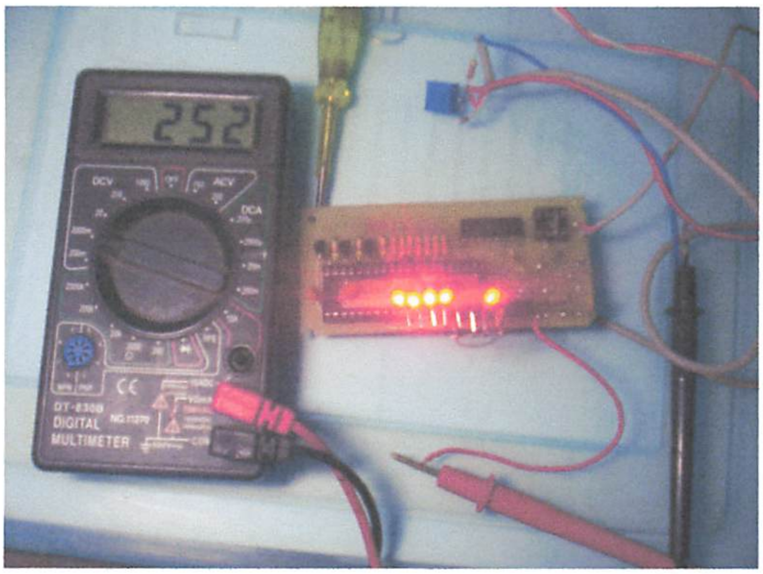
- Menaikan tegangan input ADC dimulai dari tegangan 0Volt sampai dengan 2Volt
- Menghubungkan keluaran 8 bit ADC dengan LED peraga untuk mengetahui keluaran nilai biner dalam mengkonversikan masukan analog ke bentuk keluaran digital.
- Mengamati hasil pengujian dengan memperhatian nyala masing-masing LED peraga untuk tiap-tiap masukan analog yang berbeda.
- Mencatat hasil pengujian pada tabel 4.2.

d. Hasil Pengujian.

Tabel 4.2. Hasil Pengujian Rangkaian ADC

No	Tegangan Input (V)	Output ADC (Biner)								HEX	DEC
		Db0	Db1	Db2	Db3	Db4	Db5	Db6	Db7		
1	0,00	0	0	0	0	0	0	0	0	00h	0
2	0,50	0	0	1	0	0	1	0	1	19h	25
3	1,00	0	1	0	1	0	0	0	0	32h	50
4	1,10	0	1	0	1	0	1	0	1	37h	55
5	1,20	0	1	1	0	0	0	0	0	3ch	60
6	1,22	0	1	1	0	0	0	0	1	3dh	61
7	1,24	0	1	1	0	0	0	1	0	3eh	62
8	1,26	0	1	1	0	0	0	1	1	3fh	63
9	1,28	0	1	1	0	0	1	0	0	40h	64
10	1,30	0	1	1	0	0	1	0	1	41h	65
11	1,32	0	1	1	0	0	1	1	0	42h	66
12	1,34	0	1	1	0	0	1	1	1	43h	67
13	1,36	0	1	1	0	1	0	0	0	44h	68
14	1,38	0	1	1	0	1	0	0	1	45h	69
15	1,40	0	1	1	0	0	0	0	0	46h	70
16	1,42	0	1	1	1	0	0	0	1	47h	71
17	1,44	0	1	1	1	0	0	1	0	48h	72
18	1,46	0	1	1	1	0	0	1	1	49h	73
19	1,48	0	1	1	1	0	1	0	0	4ah	74
20	1,50	0	1	1	1	0	1	0	1	4bh	75
21	1,52	0	1	1	1	0	1	1	0	4ch	76
22	1,54	0	1	1	1	0	1	1	1	4dh	77
23	1,56	0	1	1	1	1	0	0	0	4eh	78
24	1,58	0	1	1	1	1	0	0	1	4fh	79
25	1,60	1	0	0	0	0	0	0	0	50h	80
26	1,62	1	0	0	0	0	0	0	1	51h	81
27	1,64	1	0	0	0	0	0	1	0	52h	82
28	1,66	1	0	0	0	0	0	1	1	53h	83
29	1,68	1	0	0	0	0	1	0	0	54h	84
30	1,70	1	0	0	0	0	1	0	1	55h	85
32	1,72	1	0	0	0	0	1	1	0	56h	86
33	1,74	1	0	0	0	0	1	1	1	57h	87
34	1,76	1	0	0	0	1	0	0	0	58h	88
35	1,78	1	0	0	0	1	0	0	1	59h	89
36	1,80	1	0	0	1	0	0	0	0	5ah	90

37	1,82	1	0	0	1	0	0	0	1	5bh	91
38	1,84	1	0	0	1	0	0	1	0	5ch	92
39	1,86	1	0	0	1	0	0	1	1	5dh	93
40	1,88	1	0	0	1	0	1	0	0	5eh	94
41	1,90	1	0	0	1	0	1	0	1	5fh	95
42	1,92	1	0	0	1	0	1	1	0	60h	96
43	1,94	1	0	0	1	0	1	1	1	61h	97
44	1,96	1	0	0	1	1	0	0	0	62h	98
45	1,98	1	0	0	1	1	0	0	1	63h	99



Gambar 4.4. Foto Pengujian Rangkaian ADC 0804

e. Analisis hasil pengujian.

Dari tabel hasil pengujian dapat diketahui bahwa ADC 0804 mampu mengkonversi masukan analog menjadi keluaran biner. Hasil konversi tersebut linier dengan bobot perbitnya adalah ± 20mV. Dimana setiap terjadi perubahan 20mV maka pada output akan mengalami perubahan pula sebesar 1bit.

Nilai kesalahan menunjukkan nilai penyimpangan data digital keluaran ADC dengan nilai yang sebenarnya. Nilai kesalahan maksimum berdasarkan data yang diberikan ke ADC 0804 adalah sebesar 1 LSB.

Bobot biner 1LSB adalah untuk sistem ini adalah :

$$\text{Re}\,solusi\,1Bit = \frac{V_{ref}}{2^8 - 1} = \frac{5}{255} = 19{,}6\,mV$$

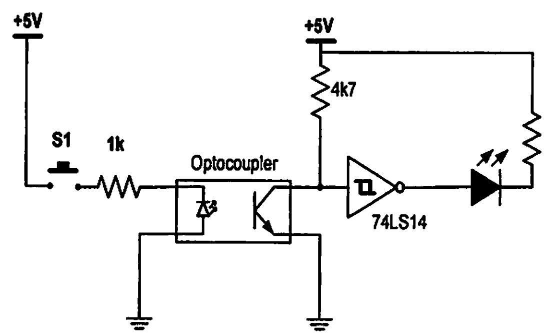
4.4. Pengujian Rangkaian Optocoupler

a. Tujuan

Pengujian bagian rangkaian optocoupler bertujuan untuk mengetahui apakah optocoupler dapat berfungsi dengan baik mendeteksi tegangan dari pulser.

b. Prosedur pengujian

Pengujian rangkaian optocoupler dilakukan dengan menghubungkan input dengan tegangan catu 5V outputnya dihubungkan dengan led sebagai display logika high. Rangkaian pengujian dapat dilihat pada gambar 4.5



Gambar 4.5. Pengujian Optocoupler

c. Hasil pengujian

Tabel 4.3. Pengujian Optocoupler

No	Posisi Saklar	Output (LED)
1	On	High (menyala)
2	Off	Low (Mati)

Dari hasil pengujian dapat diketahui bahwa optocoupler dapat dengan baik mendeteksi tegangan dan menampilkan outputnya dalam bentuk logika logika digital. Dimana sesuai dengan *datasheet* IC 74HC14 bahwa tegangan output pada saat *high* adalah 5V dan tegangan saat *low* adalah 0V.

4.5. Pengujian Rangkaian *Driver Seven Segment*

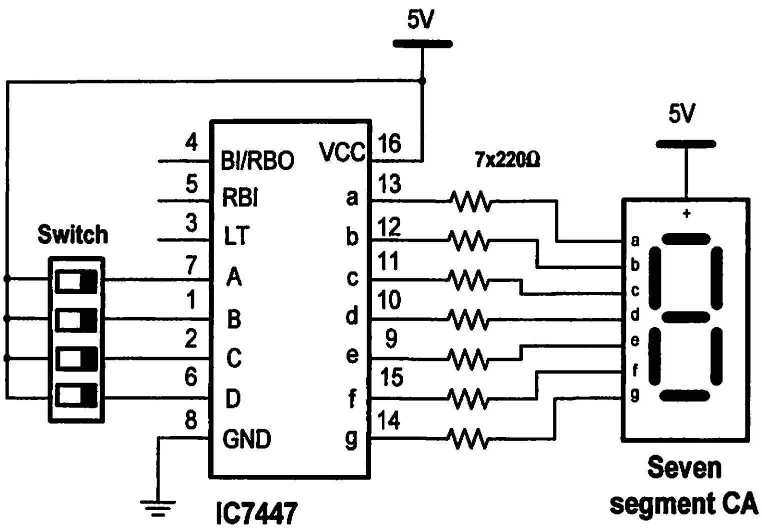
a. Tujuan

Tujuan dari pengujian rangkaian *driver seven segment* adalah untuk mengetahui apakah IC7447 sudah dapat menterjemahkan 4 digit data biner menjadi data decimal dan menampilkanya melalui *seven segment* seperti yang telah direncanakan.

b. Prosedur pengujian

- Menyusun rangkaian seperti pada gambar 4.3
- Memasukan data biner pada masukan IC7447 melalui switch yang terhubung dengan tegangan catu daya

- Mengamati tampilan output pada seven segment dan mencatat perubahan yang terjadi pada tabel 4.3



Gambar 4.6. Pengujian Rangkaian *Driver Seven Segment*

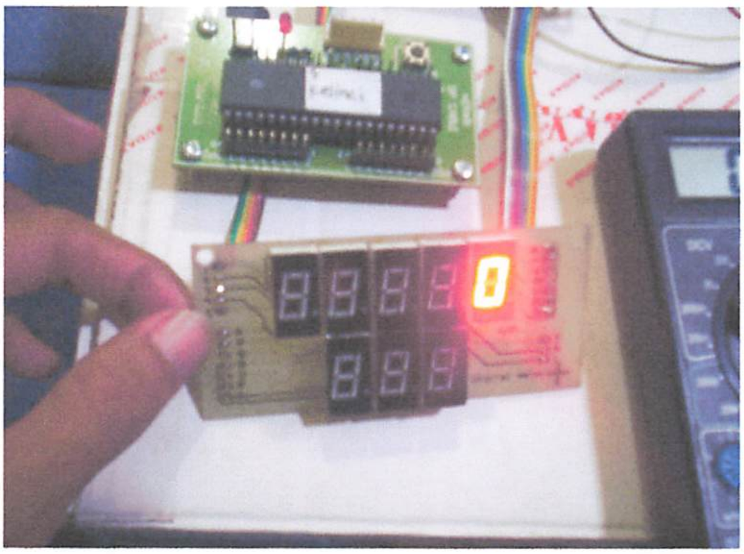
c. Hasil pengujian

Dari pengujian yang telah dilakukan maka didapat hasil yang membuktikan bahwa rangkaian IC7447 dapat menterjemahkan data biner dari input dan menampilkanya pada seven segment sesuai dengan yang telah direncanakan. Berikut ini adalah tabel dari hasil pengujian rangkaian *driver seven segment*

Tabel 4.3. Hasil Pengujian Rangkaian *Driver Seven Segment*

Desimal	Input IC7447				Output IC7447						
	D	C	B	A	a	b	c	d	e	f	g
0	0	0	0	0	0	0	0	0	0	0	1
1	0	0	0	1	1	0	0	1	1	1	1
2	0	0	1	0	0	0	1	0	0	1	0

3	0	0	1	1	0	0	0	0	1	1	0
4	0	1	0	0	1	0	0	1	1	0	0
5	0	1	0	1	0	1	0	0	1	0	0
6	0	1	1	0	1	1	0	0	0	0	0
7	0	1	1	1	0	0	0	1	1	1	1
8	1	0	0	0	0	0	0	0	0	0	0
9	1	0	0	1	0	0	0	1	1	0	0



Gambar 4.7. Foto Pengujian Rangkaian *Driver Seven Segment*

4.6. Pengujian Keseluruhan Sistem

Pengujian sistem secara keseluruhan dilakukan dengan tujuan untuk mengetahui apakah alat yang telah dibuat sudah dapat bekerja sesuai dengan yang direncanakan atau belum. Pengujian dilakukan dengan memasang alat pada sepeda motor secara langsung, yaitu pengukuran RPM mesin dan pengukuran suhu mesin.

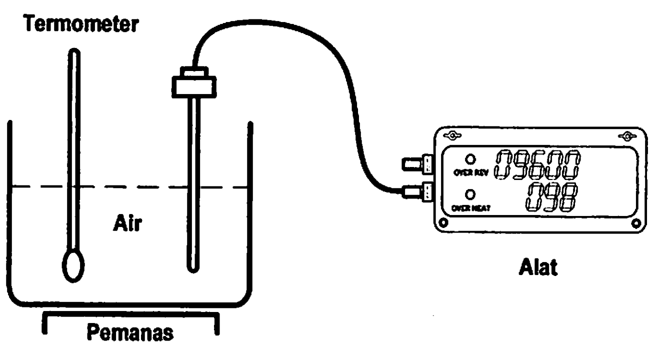
4.6.1. Pengujian Rangkaian Pengukur Suhu

a. Tujuan

Tujuan dari pengujian rangkaian pengukur suhu pada umumnya adalah untuk mengetahui tanggapan alat terhadap perubahan temperature yang didteksi sensor.

b. Pengujian pertama

Pengujian pertama dilakukan dengan cara memasukan sensor pada bak pemanas pengujian dilakukan untuk mengetahui tanggapan alat terhadap perubahan suhu. Sebagai acuan digunakan thermometer analog. Proses pengujian dapat dilihat seperti pada gambar 4.4., kemudian data hasil pengukuran dicatat pada tabel 4.4



Gambar 4.8. Pengujian Pengukur Suhu

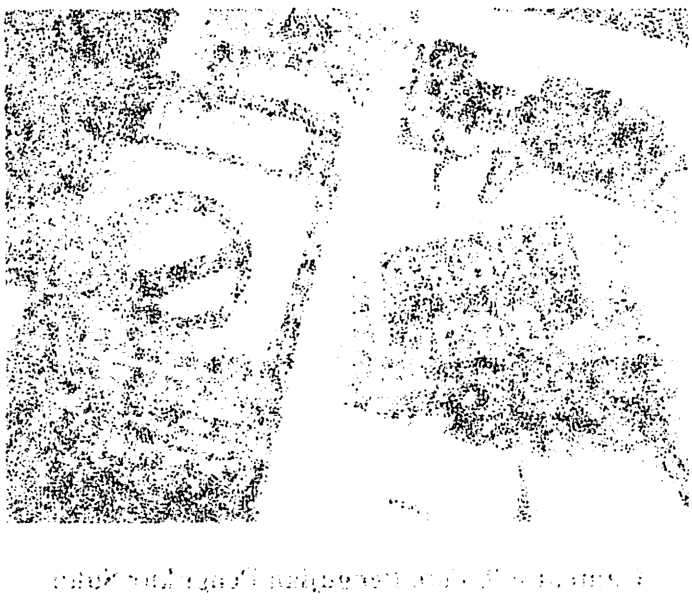
Tabel 4.4. Pengukuran Suhu Air Pada Bak Pemanas

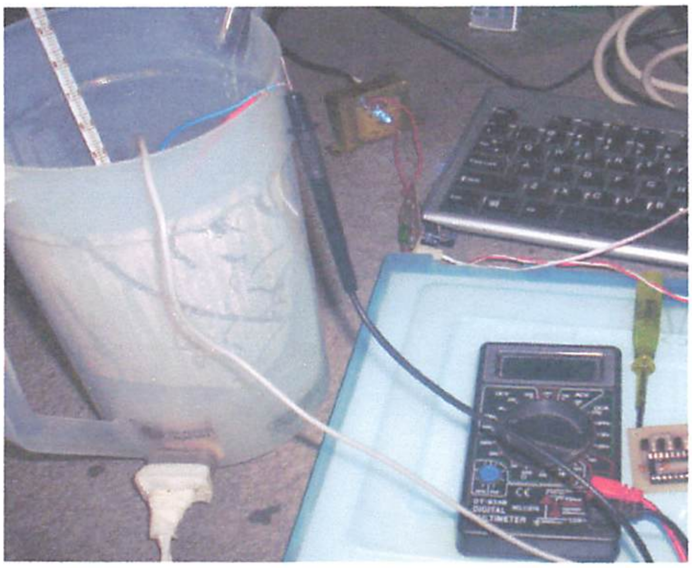
No	Pembacaan Temperatur		Penyimpangan (%)
	Termometer (°C)	Alat (°C)	
1	25	25	0
2	30	31	3,22
3	40	40	0

4	50	50	0
5	55	54	1,81
6	60	61	1,63
7	65	65	0
8	70	70	0
9	71	71	0
10	72	71	1,38
11	73	73	0
12	74	73	1,35
13	75	75	0
14	76	76	0
15	77	76	1,29
16	78	78	0
17	79	79	0
18	80	81	1,23
19	81	81	0
20	82	82	0
21	83	83	0
22	84	84	0
23	85	85	0
24	86	85	1,16
25	87	86	1,14
26	88	88	0
27	89	89	0
28	90	91	
29	91	91	0
30	92	92	0

31	93	93	00
32	94	94	1,09
33	95	94	1,05
34	96	95	1,04
35	97	97	0
36	98	99	1,01
37	99	99	0
38	100	100	0
Kesalahan rata-rata			0.48 %

Gambar 4.9. Foto Pengujian Pengukur Suhu





Gambar 4.10. Penempatan Sensor Pada Pemanas Air

$$Persentase\ penyimpangan = \frac{PembacaanAlat - PembacaanTermometer}{PembacaanAlat} \times 100\%$$

Misalnya untuk pengukuran 2

$$Persentase\ penyimpangan = \frac{31 - 30}{31} \times 100\% = 3{,}22\%$$

Dengan cara yang sama dapat dicari nilai persentase kesalahan untuk percobaan-percobaan berikutnya. Sedangkan untuk nilai rata-rata penyimpangan dapat dicari dengan:

$$Penyimpangan\ rata - rata = \frac{\Sigma(\%KesalahanPengukuran)}{BanyaknyaData}$$

$$Penyimpangan\ rata - rata = \frac{18{,}24\%}{38}$$
$$= 0{,}48\%$$

Tingkat akurasi pembacaan : 100% - 0.48% = 99,52%

c. Pengujian kedua

Pengujian dilakukan dengan cara memasang sensor suhu yang sudah diisolasi dengan baik kedalam *crankcase* mesin melalui lubang tutup oli kemudian membandingkanya hasil pembacaan alat dengan pembacaan pada skala thermometer.

Prosedur pengujian rangkaian pengukur suhu mesin adalah sebagai berikut:

- Pasang sensor suhu pada *crankcase* melalui lubang tutup oli mesin
- Nyalakan mesin selama beberapa menit, atau gunakan sepeda motor untuk menempuh jarak beberapa kilometer dan amati pembacaan suhu pada alat
- Matikan mesin dan masukan thermometer pada *crankcase* melalui lubang yang sama
- Perhatikan pembacaan suhu pada alat dan pembacaan suhu pada termometer
- Mencatat hasil pembacaan keduanya pada tabel 4.5

Tabel 4.5. Pengukuran Suhu Oli Mesin

No	Temperatur	Pembacaan		
		Termometer (°C)	Alat (°C)	Penyimpangan (%)
1	70	70	70	0
2	75	75	75	0
3	77	77	76	1.29
4	78	78	78	0
5	79	79	78	1.26
6	80	80	80	0
7	81	81	80	1.23
8	82	82	81	1.21
9	83	83	83	0

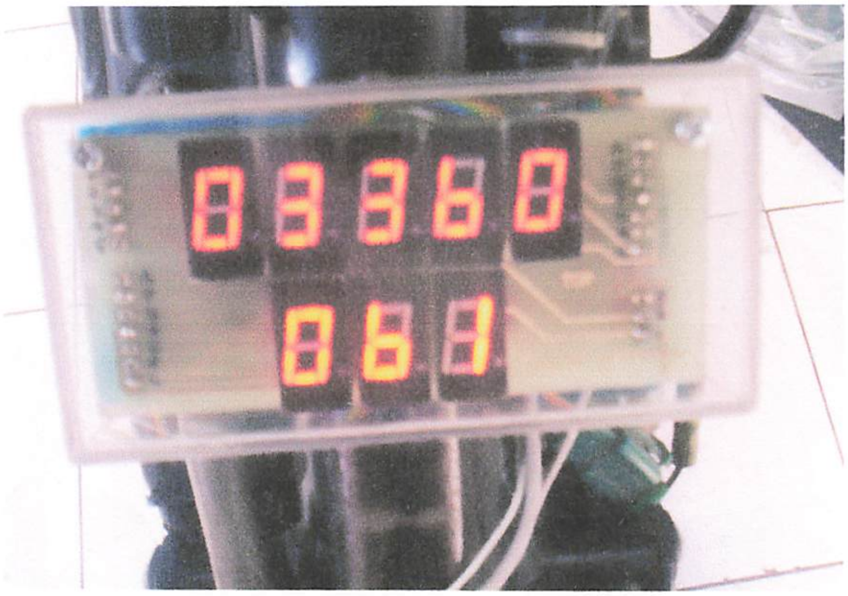
1	84	84	84	0
0	85	85	85	0
11	86	86	85	1.16
12	87	87	87	0
13	88	88	88	0
14	89	89	88	1.12
Kesalahan rata-rata				0.56%

$$Persentase\ penyimpangan = \frac{PembacaanAlat - PembacaanTermometer}{PembacaanAlat} \times 100\%$$

$$Penyimpangan\ rata - rata = \frac{17{,}27\%}{14}$$
$$= 0.52\%$$

Tingkat akurasi pembacaan 100% - 0,52% = 99,48%

Gambar 4.11. Foto Pengukuran Suhu Mesin



Gambar 4.12. Foto Pembacaan Temperatur Mesin

d. Analisa hasil pengujian

Dari hasil kedua proses pengujian rangkaian pengukur suhu diatas dapat diketahui bahwa alat yang telah dibuat mempunyai tanggapan yang baik terhadap perubahan suhu. Dimana dapat diketahui prosentase kesalahan pembacaan adalah sebagai berikut :

$$Persentase\ penyimpangan = \frac{PembacaanAlat - PembacaanTermometer}{PembacaanAlat} \times 100\%$$

$$Penyimpangan\ rata-rata = \frac{\Sigma(\%KesalahanPengukuran)}{BanyaknyaData}$$

Untuk pengujian pertama :

$$Penyimpangan\ rata-rata = \frac{18,24\%}{38}$$
$$= 0,48\%$$

Dengan nilai akurasi pembacaan sebesar : 100% - 0.48% = 95,2%

Untuk pengujian kedua

$$Penyimpangan\ rata-rata = \frac{17,27\%}{14}$$
$$= 0.52\%$$

Dengan nilai akurasi pembacaan sebesar : 100% - 0,52% = 99,48%

Faktor yang mempengaruhi terjadinya penyimpangan atau kesalahan pembacaan adalah tingkat akurasi ADC 0804 yang sebesar 1LSB, kesalahan pada saat proses sampling data ADC sehingga software tidak melakukan konversi sesuai dengan data yang sebenarnya, serta kesalahan pembacaan pada skala thermometer pada saat melakukan pengukuran

.

4.6.2. Pengujian Rangkaian Pengukur Putaran Mesin.

a. Tujuan

Pengujian dilakukan untuk mengetahui apakah alat yang telah dibuat sudah dapat bekerja sesuai dengan yang telah direncanakan yaitu mengukur putaran mesin. Kemudian membandingkan hasil dari pembacaan alat dengan hasil pembacaan alat ukur yang dijadikan acuan.

b. Prosedur pengujian

Sebagai pembanding digunakan *tachometer* analog pada sepeda motor Honda GL Max. Untuk mendeteksi putaran, kabel sensor dihubungkan dengan kabel pulser pada CDI unit, kemudian menghidupkan sepeda motor dan mencatat hasil pembacaan keduanya pada tabel 4.5.

c. Hasil pengujian

Tabel 4.5. Pengukuran Putaran Mesin**

No	Putaran Mesin *(RPM)*	Pembacaan pada alat *(RPM)*	Penyimpangan (%)
1	1200	1200	0
2	1500	1560	3,84
3	2000	2040	2,5
4	2500	2520	0,7
5	3000	3120	3,8
6	3500	3480	0,5
7	4000	3960	1,0
8	4500	4440	1,3
9	5000	5040	0,8
10	5500	5640	2,4
11	6000	6000	0
12	6500	6480	0,3
13	7000	6960	0,5
14	7500	7560	1
15	8000	8160	1,9
16	8500	8520	0,2
17	9000	9000	0
Kesalahan pembacaan rata-rata			1.43%

Keterangan :

** Pengujian dilakukan pada sepeda motor Honda GL MAX 2001 kondisi standart

Gambar 4.13. Foto Pengukuran Putaran Mesin

d. Analisa hasil pengujian

Dari proses pengujian dapat diketahui bahwa rangkaian pengukur putaran mesin *(RPM meter)* yang telah dibuat dapat melakukan pengukuran dengan baik. Dengan tingkat akurasi sebesar 0.14%. nilai tersebut dapt dicari dengan menggunakan rumus sebagai berikut :

$$Persentase\ penyimpangan = \frac{PembacaanAlat - PembacaanAlatAcuan}{PembacaanAlat} \times 100\%$$

$$Penyimpangan\ rata - rata = \frac{\Sigma(\%KesalahanPengukuran)}{BanyaknyaData}$$

$$Penyimpangan\ rata - rata = \frac{24.31\%}{17}$$
$$= 1.43\%$$

Nilai akurasi pembacaan pengukur putaran = 100% - 0,82% = 98,73%

Penyimpangan pembacaan yang terjadi disebabkan oleh kesalahan software dalam melakukan perhitungan pulsa yang keluar dari pulser pengapian, dimana setiap satu pulsa yang terdeteksi diartikan telah terjadi putaran sebanyak dua kali. Dan pengukuran putaran dilakukan dengan menghitung jumlah pulsa dalam satu detik kemudian hasilnya dikalikan 120. jadi angka yang muncul pada display adalah kelipatan 120.

4.7. Spesifikasi Alat

Alat yang telah dibuat ini mempunyai spesifikasi sebagai berikut :

1. Pengolah data utama : Mikrokontroler AT89C51
2. Tegangan kerja alat : 6 -12 VDC
3. Range pengukuran suhu mesin : 25°C - 100°C (akurasi 99,48)
4. Range pengukuran kecepatan putar mesin : 0 RPM – 12000 RPM (akurasi 98,73%)
5. Dimensi alat : P x L x T = 9 x 4,5 x 4,5 CM
6. Aplikasi alat : Sepeda motor 4 tak silinder tunggal dengan sistem pendingin udara

BAB V
PENUTUP

5.1. Kesimpulan

Berdasarkan pada hasil pengujian dan analisis rangkaian pengukur putaran dan temperatur mesin sepeda motor empat langkah silinder tunggal, maka dapat diambil beberapa kesimpulan sebagai berikut:

1. Dari hasi pengujian sensor LM 35 yang dipakai pada rangkaian pengukur suhu adalah linier dengan prosentase penyimpangan sebesar 0,39%
2. Untuk mendeteksi setiap pulsa pengapian yang keluar dari *Pulser* digunakan optocoupler. Dimana setiap pulsa yang terdeteksi pada sepeda motor empat langkah silinder tunggal berarti telah terjadi putaran sebanyak dua kali.
3. Aplikasi sistem untuk pengukuran putaran mesin terjadi penyimpangan pengukuran sebesar 0,45%

5.2. Saran

Ada beberapa hal yang perlu diperhatikan dalam pengembangan alat ukur ini dikemudian hari. Meskipun alat ini sudah dapat bekerja dengan baik dan sesuai dengan perencanaan tetapi masih ada beberapa hal yang perlu ditingkatkan diantaranya :

1. Dalam mendesain PCB sebaiknya diusahakan sekecil mungkin sehingga kemasan alat juga tidak terlalu besar. Serta menghindari pemakaian socket pada komponen yang akan dipasang karena akan mempengaruhi ketebalan kemasan alat.
2. Agar alat lebih awet pada komponen-komponen vital diberikan lem besi untuk menghindari kerusakan akibat getaran.
3. Untuk kedepanya, agar perancangan lebih sempurna bisa mendesain sebuah panel speedometer lengkap dengan aplikasi pokok lainya seperti indikator kecepatan dan indikator volume bahan bakar.
4. Agar kemasan lebih kuat dan tahan benturan sebaiknya boks dibuat dari logam.

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INSTITUT TEKNOLOGI NASIONAL MALANG
JURUSAN TEKNIK ELEKTRO DIPLOMA TIGA (D-III)
MALANG

UT - 2

KESEDIAAN PEMBIMBING
TUGAS AKHIR

Sesuai permohonan dari mahasiswa :

Nama : Agung Triono

No. Mahasiswa : 0257033

Program Studi : Teknik Elektro D-III

Judul Tugas Akhir : Perencanaan dan Pembuatan Alat Pemantau Putaran dan Suhu Mesin Pada Sepeda Motor 4 tak silinder Tunggal

Bahwa kami bersedia membimbing Tugas Akhir dari mahasiswa tersebut.

Jangka waktu penyelesaian Tugas Akhir selama 4 (empat) bulan mulai tanggal 10/01/2006 s/d 10/04/2007 dan apabila dalam jangka waktu tersebut belum selesai maka tugas akhir tersebut dinyatakan **GUGUR**

Malang, 10 Januari 2007

Dosen Pembimbing;

Bambang Prio Hartono,ST,MT

NIP.

Nb :
Setelah disetujui agar formulir ini diserahkan Mahasiswa yang bersangkutan kepada sekretaris jurusan Teknik Elektro D-III

INSTITUT TEKNOLOGI NASIONAL MALANG
FAKULTAS TEKNOLOGI INDUSTRI
JURUSAN TEKNIK ELEKTRO D-III

LEMBAR ASISTENSI TUGAS AKHIR

Nama : Agung Triono

NIM : 02.57.033

Jurusan : T. Elektronika D-III

Judul Tugas Akhir : Perencanaan Dan Pembuatan Alat Pemantau Putaran dan Suhu Mesin Sepeda Motor 4 Tak Silinder Tunggal

Dosen Pembimbing : Bambang Prio H. ST, MT

NO	TANGGAL	REVISI	TTD
1.	7-2-2007	BAB I Perbaikan BAB II Sensor, terdiri ADC, Op-Amp rumus.	[signature]
2.	12-2-2007	BAB II Acc	[signature]
3.	7-3-2007	BAB III Perbaiki	[signature]
4.	12-3-2007	BAB IV Acc BAB V Perbaiki	[signature] [signature]
5	17-3-2007	Acc kesimpulan revisi	[signature]

Acc maju [signature]

PERKUMPULAN PENGELOLA PENDIDIKAN UMUM DAN TEKNOLOGI NASIONAL MALANG
INSTITUT TEKNOLOGI NASIONAL MALANG
FAKULTAS TEKNOLOGI INDUSTRI
FAKULTAS TEKNIK SIPIL DAN PERENCANAAN
PROGRAM PASCA SARJANA MAGISER TEKNIK

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BERITA ACARA UJIAN TUGAS AKHIR
FAKULTAS TEKNOLOGI INDUSTRI

Nama Mahasiswa : AGUNG TRIONO

NIM : 02.57.033

Jurusan : Teknik Elektro D-III

Konsentrasi : Teknik Elektronika

Judul Tugas Akhir : Perencanaan dan Pembuatan Alat Pemantau Putaran dan Suhu Mesin Sepeda Motor 4 Tak Silinder Tunggal

Dipertahankan dihadapan Tim Penguji Tugas Akhir Jenjang Diploma (D-III)

Pada Hari : Kamis

Tanggal : 22 Maret 2007

Dengan Nilai : 82,6 (A) ✓

Panitia Ujian Tugas Akhir

(Ir. Mochtar Asroni, MSME)
Ketua Majelis Penguji

(Ir. Choirul Saleh, MT)
Sekretaris Majelis Penguji

Anggota Penguji

(Ir. M. Abdul Hamid, MT)
Anggota Penguji I

(Ir. Yunior Siahaan)
Anggota Penguji II

LAMPIRAN

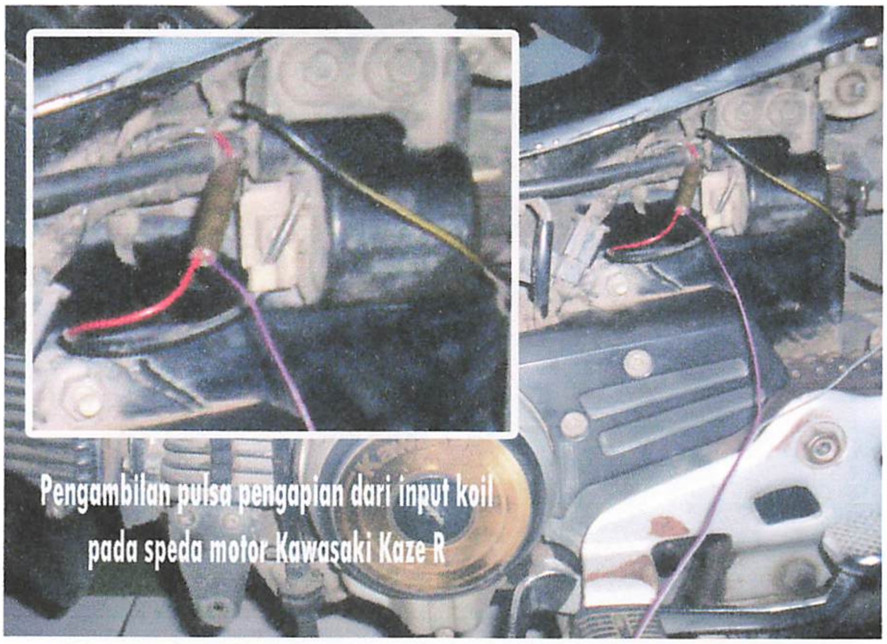
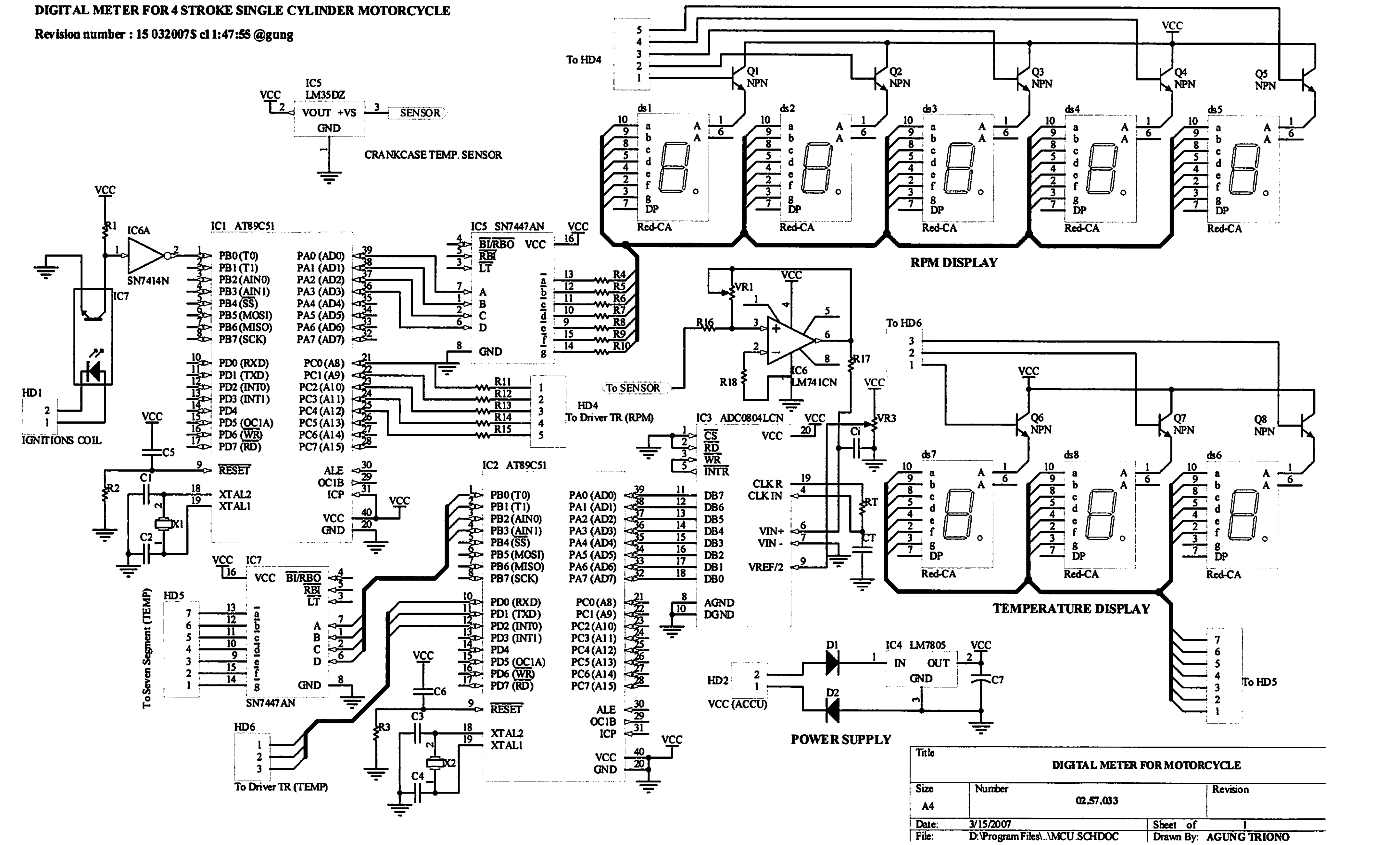


Foto Pemasangan Sensor Pada Pulser Pengapian

Pemasangan Alat Pada Sepeda Motor Kawasaki Kaze R

DIGITAL METER FOR 4 STROKE SINGLE CYLINDER MOTORCYCLE

Revision number : 15 032007S c1 1:47:55 @gung



```
;===========================================================
; MEITAN X Compiler for ATMEL microChips
; Release Vesion 2004
; RPM METER
; User NAME : AGUNG
; FILE NAME : DIGITAL METER.asm
;===========================================================
CSeg   At 00h
    Jmp    main

$Include(D:\protel job\Digital Meter\const.MOL)
$Include(D:\protel job\Digital Meter\Timers.MOL)
$Include(D:\protel job\Digital Meter\BCD.MOL)
$Include(D:\protel job\Digital Meter\Segment.MOL)
CSeg   At    670h
;===========================================================
; user Mapping bit & memory
;===========================================================
DSeg              At     DefineStorage
DataRPS:            Ds     Byte
SegmentBufferset:     Ds     Dword

CSeg

;===========================================================
; For User Listing Program
;===========================================================

Subroutine SegmentBufferUpdate:
    Mov    R0,#SegmentBufferSet
    Mov    R1,#SegmentBuffer
    Mov    R2,#DWord
    Call   BCDMoveBufferToBuffer
EndSub
Subroutine DisplayData:
    Mov    R0,#SegmentBufferSet
    Mov    R6,#BufferSize
    Call   BCDClearBuffer
    Mov    A,DataRps
    Mov    R0,#SegmentBufferSet
    Call   ByteToBCDBuffer
    Call   CopyBuffer
    Mov    R0,#SegmentBufferSet  ; Source and result
    Mov    R1,#BufferCalc  ; adder location
    Call   BCDAddRam

    Mov    A,#60
    Mov    R0,#BCDBuffer
    Call   ByteToBCDBuffer
    Mov    R0,#SegmentBufferSet
    Call   BCDMultiplex
```

```
      Call   SegmentBufferUpdate
      ExitDisplay:

EndSub
Subroutine PulseHandle:
      Jnb    SecondUpdate,ExitPulse
      Clr    SecondUpdate
      Mov    A,Exter0PulseCount
      Cjne   A,DataRPS,NotSame
      Jmp    NextClear
NotSame:
      Cjne   A,#100,Over
OVer:
      Jc     NotOver
      Mov    A,#100
NotOver:
      Mov    DataRPS,A
NextClear:
      Mov    Exter0PulseCount,#00
ExitPulse:
EndSub

MAIN:
      Mov    SP,#57h
      Anl    auxr,#0EFh
      Orl    auxr,#09h
      Anl    auxr1,#0FEh
      Call   TimersInit
      Call   SegmentInit
      Mov    DataRps,#0
      Call   InterruptEnable
      Call   TimerActive
      Call   SensorEnable
Preloop:
      Call   PulseHandle
      Call   DisplayData
      Call   SegmentScan
      Jmp    Preloop
      Ljmp   MAIN

End.
```

```
;==============================
;OIL / ENGINE TEMPERATURE
;programed by Agung Triono
;==============================
adc             data    p0
startadc        bit     p2.7
        org     0h
start:  clr     p2.7    ;aktifkan ADC
        nop
        nop
        nop
        setb    p2.7
        mov     A,adc
c1:     cjne    A,#0dh,c2
        call    s25
c2:     cjne    A,#0eh,c3
        call    s26
c3:     cjne    A,#0fh,c4
        call    s27
c4:     cjne    A,#10h,c5
        call    s28
c5:     cjne    A,#11h,c6
        call    s29
c6:     cjne    A,#12h,c7
        call    s30
c7:     cjne    A,#13h,c8
        call    s31
c8:     cjne    A,#14h,c9
        call    s32
c9:     cjne    A,#15h,c10
        call    s33
c10:    cjne    A,#16h,c11
        call    s34
c11:    cjne    A,#17h,c12
        call    s35
c12:    cjne    A,#18h,c13
        call    s36
c13:    cjne    A,#19h,c14
        call    s37
c14:    cjne    A,#1ah,c15
        call    s38
c15:    cjne    A,#1bh,c16
        call    s39
c16:    cjne    A,#1ch,c17
        call    s40
c17:    cjne    A,#1dh,c18
        call    s41
c18:    cjne    A,#1eh,c19
        call    s42
c19:    cjne    A,#1fh,c20
        call    s43
c20:    cjne    A,#20h,c21
        call    s44
c21:    cjne    A,#21h,c22
        call    s45
c22:    cjne    A,#22h,c23
        call    s46
c23:    cjne    A,#23h,c24
        call    s47
c24:    cjne    A,#24h,c25
        call    s48
c25:    cjne    A,#25h,c26
        call    s49
c26:    cjne    A,#26h,c27
        call    s50
c27:    cjne    A,#27h,c28
        call    s51
c28:    cjne    A,#28h,c29
        call    s52
c29:    cjne    A,#29h,c30
        call    s53
c30:    cjne    A,#2ah,c31
        call    s54
c31:    cjne    A,#2bh,c32
        call    s55
c32:    cjne    A,#2ch,c33
        call    s56
c33:    cjne    A,#2dh,c34
        call    s57
c34:    cjne    A,#2eh,c35
        call    s58
c35:    cjne    A,#2fh,c36
        call    s59
c36:    cjne    A,#30h,c37
        call    s60
c37:    cjne    A,#31h,c38
```

```
        call    s61
c38:    cjne    A,#32h,c39
        call    s62
c39:    cjne    A,#33h,c40
        call    s63
c40:    cjne    A,#34h,c41
        call    s64
c41:    cjne    A,#35h,c42
        call    s65
c42:    cjne    A,#36h,c43
        call    s66
c43:    cjne    A,#37h,c44
        call    s67
c44:    cjne    A,#38h,c45
        call    s68
c45:    cjne    A,#39h,c46
        call    s69
c46:    cjne    A,#3ah,c47
        call    s70
c47:    cjne    A,#3bh,c48
        call    s71
c48:    cjne    A,#3ch,c49
        call    s72
c49:    cjne    A,#3dh,c50
        call    s73
c50:    cjne    A,#3eh,c51
        call    s74
c51:    cjne    A,#3fh,c52
        call    s75
c52:    cjne    A,#40h,c53
        call    s76
c53:    cjne    A,#41h,c54
        call    s77
c54:    cjne    A,#42h,c55
        call    s78
c55:    cjne    A,#43h,c56
        call    s79
c56:    cjne    A,#44h,c57
        call    s80
c57:    cjne    A,#45h,c58
        call    s81
c58:    cjne    A,#46h,c59
        call    s82
c59:    cjne    A,#47h,c60
        call    s83
c60:    cjne    A,#48h,c61
        call    s84
c61:    cjne    A,#49h,c62
        call    s85
c62:    cjne    A,#4ah,c63
        call    s86
c63:    cjne    A,#4bh,c64
        call    s87
c64:    cjne    A,#4ch,c65
        call    s88
c65:    cjne    A,#4dh,c66
        call    s89
c66:    cjne    A,#4eh,c67
        call    s90
c67:    cjne    A,#4fh,c68
        call    s91
c68:    cjne    A,#50h,c69
        call    s92
c69:    cjne    A,#51h,c70
        call    s93
c70:    cjne    A,#52h,c71
        call    s94
c71:    cjne    A,#53h,c72
        call    s95
c72:    cjne    A,#54h,c73
        call    s96
c73:    cjne    A,#55h,c74
        call    s97
c74:    cjne    A,#56h,c75
        call    s98
c75:    cjne    A,#57h,c76
        call    s99
c76:    cjne    A,#58h,c77
        call    s100
c77:    cjne    A,#59h,c78
        call    s101
c78:    cjne    A,#5ah,error
        call    s102
error:  mov     p1,#08h
        mov     p3,#0ffh
        call    delay
```

```
        mov     p3,#00h
        call    delay
        mov     p3,#0ffh
        call    delay
        mov     p3,#00h
        jmp     start
;==============================
;Subroutine angka
;==============================
a0:     mov     p1,#00h
        call    del
        ret
a1:     mov     p1,#01h
        call    del
        ret
a2:     mov     p1,#02h
        call    del
        ret
a3:     mov     p1,#03h
        call    del
        ret
a4:     mov     p1,#04h
        call    del
        ret
a5:     mov     p1,#05h
        call    del
        ret
a6:     mov     p1,#06h
        call    del
        ret
a7:     mov     p1,#07h
        call    del
        ret
a8:     mov     p1,#08h
        call    del
        ret
a9:     mov     p1,#09h
        call    del
        ret
;==============================
;Subroutine suhu yang akan
;ditampilkan
;==============================
s25:    mov     p3,#04h
        call    a0
        mov     p3,#02h
        call    a2
        mov     p3,#01h
        call    a5
        jmp     start
s26:    mov     p3,#04h
        call    a0
        mov     p3.#02h
        call    a2
        mov     p3,#01h
        call    a6
        jmp     start
s27:    mov     p3,#04h
        call    a0
        mov     p3,#02h
        call    a2
        mov     p3,#01h
        call    a7
        jmp     start
s28:    mov     p3,#04h
        call    a0
        mov     p3,#02h
        call    a2
        mov     p3,#01h
        call    a8
        jmp     start
s29:    mov     p3,#04h
        call    a0
        mov     p3,#02h
        call    a2
        mov     p3,#01h
        call    a9
        jmp     start
s30:    mov     p3,#04h
        call    a0
        mov     p3,#02h
        call    a3
        mov     p3,#01h
        call    a0
        jmp     start
```

```
s31:    mov     p3,#04h
        call    a0
        mov     p3,#02h
        call    a3
        mov     p3,#01h
        call    a1
        jmp     start
s32:    mov     p3,#04h
        call    a0
        mov     p3,#02h
        call    a3
        mov     p3,#01h
        call    a2
        jmp     start
s33:    mov     p3,#04h
        call    a0
        mov     p3,#02h
        call    a3
        mov     p3,#01h
        call    a3
        jmp     start
s34:    mov     p3,#04h
        call    a0
        mov     p3,#02h
        call    a3
        mov     p3,#01h
        call    a4
        jmp     start
s35:    mov     p3,#04h
        call    a0
        mov     p3,#02h
        call    a3
        mov     p3,#01h
        call    a5
        jmp     start
s36:    mov     p3,#04h
        call    a0
        mov     p3,#02h
        call    a3
        mov     p3,#01h
        call    a6
        jmp     start
s37:    mov     p3,#04h
        call    a0
        mov     p3,#02h
        call    a3
        mov     p3,#01h
        call    a7
        jmp     start
s38:    mov     p3,#04h
        call    a0
        mov     p3,#02h
        call    a3
        mov     p3,#01h
        call    a8
        jmp     start
s39:    mov     p3,#04h
        call    a0
        mov     p3,#02h
        call    a3
        mov     p3,#01h
        call    a9
        jmp     start
s40:    mov     p3,#04h
        call    a0
        mov     p3,#02h
        call    a4
        mov     p3,#01h
        call    a0
        jmp     start
s41:    mov     p3,#04h
        call    a0
        mov     p3,#02h
        call    a4
        mov     p3,#01h
        call    a1
        jmp     start
s42:    mov     p3,#04h
        call    a0
        mov     p3,#02h
        call    a4
        mov     p3,#01h
        call    a2
        jmp     start
s43:    mov     p3,#04h
        call    a0
```

```
        mov     p3,#02h
        call    a4
        mov     p3,#01h
        call    a3
        jmp     start
s44:    mov     p3,#04h
        call    a0
        mov     p3,#02h
        call    a4
        mov     p3,#01h
        call    a4
        jmp     start
s45:    mov     p3,#04h
        call    a0
        mov     p3,#02h
        call    a4
        mov     p3,#01h
        call    a5
        jmp     start
s46:    mov     p3,#04h
        call    a0
        mov     p3,#02h
        call    a4
        mov     p3,#01h
        call    a6
        jmp     start
s47:    mov     p3,#04h
        call    a0
        mov     p3,#02h
        call    a4
        mov     p3,#01h
        call    a7
        jmp     start
s48:    mov     p3,#04h
        call    a0
        mov     p3,#02h
        call    a4
        mov     p3,#01h
        call    a8
        jmp     start
s49:    mov     p3,#04h
        call    a0
        mov     p3,#02h
        call    a4
        mov     p3,#01h
        call    a9
        jmp     start
s50:    mov     p3,#04h
        call    a0
        mov     p3,#02h
        call    a5
        mov     p3,#01h
        call    a0
        jmp     start
s51:    mov     p3,#04h
        call    a0
        mov     p3,#02h
        call    a5
        mov     p3,#01h
        call    a1
        jmp     start
s52:    mov     p3,#04h
        call    a0
        mov     p3,#02h
        call    a5
        mov     p3,#01h
        call    a2
        jmp     start
s53:    mov     p3,#04h
        call    a0
        mov     p3,#02h
        call    a5
        mov     p3,#01h
        call    a3
        jmp     start
s54:    mov     p3,#04h
        call    a0
        mov     p3,#02h
        call    a5
        mov     p3,#01h
        call    a4
        jmp     start
s55:    mov     p3,#04h
        call    a0
        mov     p3,#02h
        call    a5
```

```
        mov   p3,#01h
        call  a5
        jmp   start
s56:    mov   p3,#04h
        call  a0
        mov   p3,#02h
        call  a5
        mov   p3,#01h
        call  a6
        jmp   start
s57:    mov   p3,#04h
        call  a0
        mov   p3,#02h
        call  a5
        mov   p3,#01h
        call  a7
        jmp   start
s58:    mov   p3,#04h
        call  a0
        mov   p3,#02h
        call  a5
        mov   p3,#01h
        call  a8
        jmp   start
s59:    mov   p3,#04h
        call  a0
        mov   p3,#02h
        call  a5
        mov   p3,#01h
        call  a9
        jmp   start
s60:    mov   p3,#04h
        call  a0
        mov   p3,#02h
        call  a6
        mov   p3,#01h
        call  a0
        jmp   start
s61:    mov   p3,#04h
        call  a0
        mov   p3,#02h
        mov   p1,#06h
        mov   p3,#01h
        call  a1
        jmp   start
s62:    mov   p3,#04h
        call  a0
        mov   p3,#02h
        call  a6
        mov   p3,#01h
        call  a2
        jmp   start
s63:    mov   p3,#04h
        call  a0
        mov   p3,#02h
        call  a6
        mov   p3,#01h
        call  a3
        jmp   start
s64:    mov   p3,#04h
        call  a0
        mov   p3,#02h
        call  a6
        mov   p3,#01h
        call  a4
        jmp   start
s65:    mov   p3,#04h
        call  a0
        mov   p3,#02h
        call  a6
        mov   p3,#01h
        call  a5
        jmp   start
s66:    mov   p3,#04h
        call  a0
        mov   p3,#02h
        call  a6
        mov   p3,#01h
        call  a6
        jmp   start
s67:    mov   p3,#04h
        call  a0
        mov   p3,#02h
        call  a6
        mov   p3,#01h
        call  a7
```

```
        jmp     start
s68:    mov     p3,#04h
        call    a0
        mov     p3,#02h
        call    a6
        mov     p3,#01h
        call    a8
        jmp     start
s69:    mov     p3,#04h
        call    a0
        mov     p3,#02h
        call    a6
        mov     p3,#01h
        call    a9
        jmp     start
s70:    mov     p3,#04h
        call    a0
        mov     p3,#02h
        call    a7
        mov     p3,#01h
        call    a0
        jmp     start
s71:    mov     p3,#04h
        call    a0
        mov     p3,#02h
        call    a7
        mov     p3,#01h
        call    a1
        jmp     start
s72:    mov     p3,#04h
        call    a0
        mov     p3,#02h
        call    a7
        mov     p3,#01h
        call    a2
        jmp     start
s73:    mov     p3,#04h
        call    a0
        mov     p3,#02h
        call    a7
        mov     p3,#01h
        call    a3
        jmp     start
s74:    call    a0
        mov     p3,#02h
        call    a7
        mov     p3,#01h
        call    a4
        jmp     start
s75:    mov     p3,#04h
        call    a0
        mov     p3,#02h
        call    a7
        mov     p3,#01h
        call    a5
        jmp     start
s76:    mov     p3,#04h
        call    a0
        mov     p3,#02h
        call    a7
        mov     p3,#01h
        call    a6
        jmp     start
s77:    mov     p3,#04h
        call    a0
        mov     p3,#02h
        call    a7
        mov     p3,#01h
        call    a7
        jmp     start
s78:    mov     p3,#04h
        call    a0
        mov     p3,#02h
        call    a7
        mov     p3,#01h
        call    a8
        jmp     start
s79:    mov     p3,#04h
        call    a0
        mov     p3,#02h
        call    a7
        mov     p3,#01h
        call    a9
        jmp     start
s80:    mov     p3,#04h
        call    a0
```

```
        mov   p3,#02h
        call  a8
        mov   p3,#01h
        call  a0
        jmp   start
s81:    mov   p3,#04h
        call  a0
        mov   p3,#02h
        call  a8
        mov   p3,#01h
        call  a1
        jmp   start
s82:    mov   p3,#04h
        call  a0
        mov   p3,#02h
        call  a8
        mov   p3,#01h
        call  a2
        jmp   start
s83:    mov   p3,#04h
        call  a0
        mov   p3,#02h
        call  a8
        mov   p3,#01h
        call  a3
        jmp   start
s84:    mov   p3,#04h
        call  a0
        mov   p3,#02h
        call  a8
        mov   p3,#01h
        call  a4
        jmp   start
s85:    mov   p3,#04h
        call  a0
        mov   p3,#02h
        call  a8
        mov   p3,#01h
        call  a5
        jmp   start
s86:    mov   p3,#04h
        call  a0
        mov   p3,#02h
        call  a8
        mov   p3,#01h
        call  a6
        jmp   start
s87:    mov   p3,#04h
        call  a0
        mov   p3,#02h
        call  a8
        mov   p3,#01h
        call  a7
        jmp   start
s88:    mov   p3,#04h
        call  a0
        mov   p3,#02h
        call  a8
        mov   p3,#01h
        call  a8
        jmp   start
s89:    mov   p3,#04h
        call  a0
        mov   p3,#02h
        call  a8
        mov   p3,#01h
        call  a9
        jmp   start
s90:    mov   p3,#04h
        call  a0
        mov   p3,#02h
        call  a9
        mov   p3,#01h
        call  a0
        jmp   start
s91:    mov   p3,#04h
        call  a0
        mov   p3,#02h
        call  a9
        mov   p3,#01h
        call  a1
        jmp   start
s92:    mov   p3,#04h
        call  a0
        mov   p3,#02h
        call  a9
```

```
        mov     p3,#01h
        call    a2
        jmp     start
s93:    mov     p3,#04h
        call    a0
        mov     p3,#02h
        call    a9
        mov     p3,#01h
        call    a3
        jmp     start
s94:    mov     p3,#04h
        call    a0
        mov     p3,#02h
        call    a9
        mov     p3,#01h
        call    a4
        jmp     start
s95:    mov     p3,#04h
        call    a0
        mov     p3,#02h
        call    a9
        mov     p3,#01h
        call    a5
        jmp     start
s96:    mov     p3,#04h
        call    a0
        mov     p3,#02h
        call    a9
        mov     p3,#01h
        call    a6
        jmp     start
s97:    mov     p3,#04h
        call    a0
        mov     p3,#02h
        call    a9
        mov     p3,#01h
        call    a7
        jmp     start
s98:    mov     p3,#04h
        call    a0
        mov     p3,#02h
        call    a9
        mov     p3,#01h
        call    a8
        jmp     start
s99:    mov     p3,#04h
        call    a0
        mov     p3,#02h
        call    a9
        mov     p3,#01h
        call    a9
        jmp     start
s100:   mov     p3,#04h
        call    a1
        mov     p3,#02h
        call    a0
        mov     p3,#01h
        call    a0
        jmp     start
s101:   mov     p3,#04h
        call    a1
        mov     p3,#02h
        call    a0
        mov     p3,#01h
        call    a1
        jmp     start
s102:   mov     p3,#04h
        call    a1
        mov     p3,#02h
        call    a0
        mov     p3,#01h
        call    a2
        jmp     start
;========================
;routine delay
del:    mov     r0,#10
del1:   mov     r1,#10
        djnz    r1,$
        djnz    r0,del1
        ret
delay:  mov     r0,#0ffh
delay1: mov     r1,#0ffh
        djnz    r1,$
        djnz    r0,delay1
        ret
        end
```

National Semiconductor

August 1999

LM35
Precision Centigrade Temperature Sensors

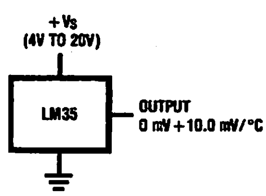
General Description

The LM35 series are precision integrated-circuit temperature sensors, whose output voltage is linearly proportional to the Celsius (Centigrade) temperature. The LM35 thus has an advantage over linear temperature sensors calibrated in ˚ Kelvin, as the user is not required to subtract a large constant voltage from its output to obtain convenient Centigrade scaling. The LM35 does not require any external calibration or trimming to provide typical accuracies of ±¼˚C at room temperature and ±¾˚C over a full −55 to +150˚C temperature range. Low cost is assured by trimming and calibration at the wafer level. The LM35's low output impedance, linear output, and precise inherent calibration make interfacing to readout or control circuitry especially easy. It can be used with single power supplies, or with plus and minus supplies. As it draws only 60 µA from its supply, it has very low self-heating, less than 0.1˚C in still air. The LM35 is rated to operate over a −55˚ to +150˚C temperature range, while the LM35C is rated for a −40˚ to +110˚C range (−10˚ with improved accuracy). The LM35 series is available packaged in hermetic TO-46 transistor packages, while the LM35C, LM35CA, and LM35D are also available in the plastic TO-92 transistor package. The LM35D is also available in an 8-lead surface mount small outline package and a plastic TO-220 package.

Features

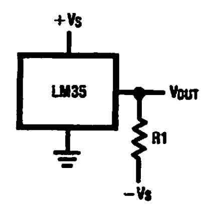
- Calibrated directly in ˚ Celsius (Centigrade)
- Linear + 10.0 mV/˚C scale factor
- 0.5˚C accuracy guaranteeable (at +25˚C)
- Rated for full −55˚ to +150˚C range
- Suitable for remote applications
- Low cost due to wafer-level trimming
- Operates from 4 to 30 volts
- Less than 60 µA current drain
- Low self-heating, 0.08˚C in still air
- Nonlinearity only ±¼˚C typical
- Low impedance output, 0.1 Ω for 1 mA load

Typical Applications



DS005516-3

FIGURE 1. Basic Centigrade Temperature Sensor (+2˚C to +150˚C)



DS005516-4

Choose $R_1 = -V_S/50\ \mu A$

V_{OUT}=+1,500 mV at +150˚C

= +250 mV at +25˚C

= −550 mV at −55˚C

FIGURE 2. Full-Range Centigrade Temperature Sensor

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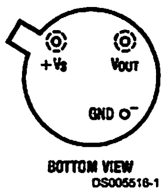
 DS005516

Connection Diagrams

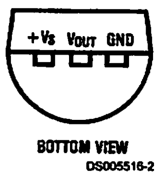
TO-46
Metal Can Package*



*Case is connected to negative pin (GND)

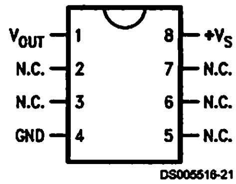
Order Number LM35H, LM35AH, LM35CH, LM35CAH or LM35DH
See NS Package Number H03H

TO-92
Plastic Package



Order Number LM35CZ, LM35CAZ or LM35DZ
See NS Package Number Z03A

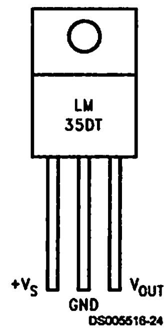
SO-8
Small Outline Molded Package



N.C. = No Connection

Top View
Order Number LM35DM
See NS Package Number M08A

TO-220
Plastic Package*



*Tab is connected to the negative pin (GND).
Note: The LM35DT pinout is different than the discontinued LM35DP.

Order Number LM35DT
See NS Package Number TA03F

Absolute Maximum Ratings (Note 10)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Supply Voltage	+35V to −0.2V
Output Voltage	+6V to −1.0V
Output Current	10 mA
Storage Temp.;	
TO-46 Package,	−60°C to +180°C
TO-92 Package,	−60°C to +150°C
SO-8 Package,	−65°C to +150°C
TO-220 Package,	−65°C to +150°C
Lead Temp.:	
TO-46 Package, (Soldering, 10 seconds)	300°C
TO-92 and TO-220 Package, (Soldering, 10 seconds)	260°C
SO Package (Note 12)	
Vapor Phase (60 seconds)	215°C
Infrared (15 seconds)	220°C
ESD Susceptibility (Note 11)	2500V

Specified Operating Temperature Range: T_{MIN} to T_{MAX} (Note 2)

LM35, LM35A	−55°C to +150°C
LM35C, LM35CA	−40°C to +110°C
LM35D	0°C to +100°C

Electrical Characteristics

Notes 1, 6)

Parameter	Conditions	LM35A			LM35CA			Units
		Typical	Tested Limit (Note 4)	Design Limit (Note 5)	Typical	Tested Limit (Note 4)	Design Limit (Note 5)	(Max.)
curacy ote 7)	T_A=+25°C	±0.2	±0.5		±0.2	±0.5		°C
	T_A=−10°C	±0.3			±0.3		±1.0	°C
	$T_A=T_{MAX}$	±0.4	±1.0		±0.4	±1.0		°C
	$T_A=T_{MIN}$	±0.4	±1.0		±0.4		±1.5	°C
nlinearity ote 8)	$T_{MIN}≤T_A≤T_{MAX}$	**±0.18**		**±0.35**	**±0.15**		**±0.3**	°C
nsor Gain verage Slope)	$T_{MIN}≤T_A≤T_{MAX}$	**+10.0**	**+9.9, +10.1**		**+10.0**		**+9.9, +10.1**	mV/°C
ad Regulation ote 3) $0≤I_L≤1$ mA	T_A=+25°C	±0.4	±1.0		±0.4	±1.0		mV/mA
	$T_{MIN}≤T_A≤T_{MAX}$	**±0.5**		**±3.0**	**±0.5**		**±3.0**	mV/mA
ie Regulation ote 3)	T_A=+25°C	±0.01	±0.05		±0.01	±0.05		mV/V
	$4V≤V_S≤30V$	**±0.02**		**±0.1**	**±0.02**		**±0.1**	mV/V
iiescent Current ote 9)	V_S=+5V, +25°C	56	67		56	67		μA
	V_S=+5V	**105**		**131**	**91**		**114**	μA
	V_S=+30V, +25°C	56.2	68		56.2	68		μA
	V_S=+30V	**105.5**		**133**	**91.5**		**116**	μA
iange of iiescent Current ote 3)	$4V≤V_S≤30V$, +25°C	0.2	1.0		0.2	1.0		μA
	$4V≤V_S≤30V$	**0.5**		**2.0**	**0.5**		**2.0**	μA
mperature iefficient of iiescent Current		**+0.39**		**+0.5**	**+0.39**		**+0.5**	μA/°C
nimum Temperature Rated Accuracy	In circuit of *Figure 1*, I_L=0	+1.5		+2.0	+1.5		+2.0	°C
ng Term Stability	$T_J=T_{MAX}$, for 1000 hours	±0.08			±0.08			°C

Electrical Characteristics

(Notes 1, 6)

Parameter	Conditions	LM35 Typical	LM35 Tested Limit (Note 4)	LM35 Design Limit (Note 5)	LM35C, LM35D Typical	LM35C, LM35D Tested Limit (Note 4)	LM35C, LM35D Design Limit (Note 5)	Units (Max.)
Accuracy, LM35, LM35C (Note 7)	T_A=+25°C	±0.4	±1.0		±0.4	±1.0		°C
	T_A=−10°C	±0.5			±0.5		±1.5	°C
	$T_A=T_{MAX}$	±0.8	±1.5		±0.8		±1.5	°C
	$T_A=T_{MIN}$	±0.8		±1.5	±0.8		±2.0	°C
Accuracy, LM35D (Note 7)	T_A=+25°C				±0.6	±1.5		°C
	$T_A=T_{MAX}$				±0.9		±2.0	°C
	$T_A=T_{MIN}$				±0.9		±2.0	°C
Nonlinearity (Note 8)	$T_{MIN} \le T_A \le T_{MAX}$	**±0.3**		**±0.5**	**±0.2**		**±0.5**	°C
Sensor Gain (Average Slope)	$T_{MIN} \le T_A \le T_{MAX}$	**+10.0**	**+9.8, +10.2**		**+10.0**		**+9.8, +10.2**	mV/°C
Load Regulation (Note 3) $0 \le I_L \le 1$ mA	T_A=+25°C	±0.4	±2.0		±0.4	±2.0		mV/mA
	$T_{MIN} \le T_A \le T_{MAX}$	**±0.5**		**±5.0**	**±0.5**		**±5.0**	mV/mA
Line Regulation (Note 3)	T_A=+25°C	±0.01	±0.1		±0.01	±0.1		mV/V
	$4V \le V_S \le 30V$	**±0.02**		**±0.2**	**±0.02**		**±0.2**	mV/V
Quiescent Current (Note 9)	V_S=+5V, +25°C	56	80		56	80		µA
	V_S=+5V	**105**		**158**	**91**		**138**	µA
	V_S=+30V, +25°C	56.2	82		56.2	82		µA
	V_S=+30V	**105.5**		**161**	**91.5**		**141**	µA
Change of Quiescent Current (Note 3)	$4V \le V_S \le 30V$, +25°C	0.2	2.0		0.2	2.0		µA
	$4V \le V_S \le 30V$	**0.5**		**3.0**	**0.5**		**3.0**	µA
Temperature Coefficient of Quiescent Current		**+0.39**		**+0.7**	**+0.39**		**+0.7**	µA/°C
Minimum Temperature for Rated Accuracy	In circuit of *Figure 1*, I_L=0	+1.5		+2.0	+1.5		+2.0	°C
Long Term Stability	$T_J=T_{MAX}$, for 1000 hours	±0.08			±0.08			°C

Note 1: Unless otherwise noted, these specifications apply: $-55°C \le T_J \le +150°C$ for the LM35 and LM35A; $-40°C \le T_J \le +110°C$ for the LM35C and LM35CA; and $0°C \le T_J \le +100°C$ for the LM35D. V_S=+5Vdc and I_{LOAD}=50 µA, in the circuit of *Figure 2*. These specifications also apply from +2°C to T_{MAX} in the circuit of *Figure 1*. Specifications in **boldface** apply over the full rated temperature range.

Note 2: Thermal resistance of the TO-46 package is 400°C/W, junction to ambient, and 24°C/W junction to case. Thermal resistance of the TO-92 package is 180°C/W junction to ambient. Thermal resistance of the small outline molded package is 220°C/W junction to ambient. Thermal resistance of the TO-220 package is 90°C/W junction to ambient. For additional thermal resistance information see table in the Applications section.

Note 3: Regulation is measured at constant junction temperature, using pulse testing with a low duty cycle. Changes in output due to heating effects can be computed by multiplying the internal dissipation by the thermal resistance.

Note 4: Tested Limits are guaranteed and 100% tested in production.

Note 5: Design Limits are guaranteed (but not 100% production tested) over the indicated temperature and supply voltage ranges. These limits are not used to calculate outgoing quality levels.

Note 6: Specifications in **boldface** apply over the full rated temperature range.

Note 7: Accuracy is defined as the error between the output voltage and 10mv/°C times the device's case temperature, at specified conditions of voltage, current, and temperature (expressed in °C).

Note 8: Nonlinearity is defined as the deviation of the output-voltage-versus-temperature curve from the best-fit straight line, over the device's rated temperature range.

Note 9: Quiescent current is defined in the circuit of *Figure 1*.

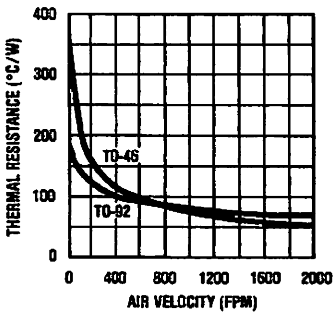
Note 10: Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. DC and AC electrical specifications do not apply when operating the device beyond its rated operating conditions. See Note 1.

Note 11: Human body model, 100 pF discharged through a 1.5 kΩ resistor.

Note 12: See AN-450 "Surface Mounting Methods and Their Effect on Product Reliability" or the section titled "Surface Mount" found in a current National Semiconductor Linear Data Book for other methods of soldering surface mount devices.

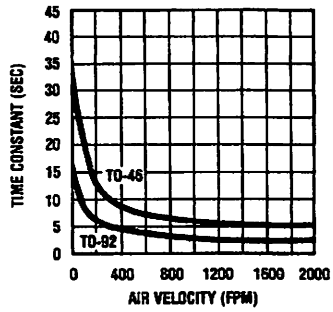
Typical Performance Characteristics

Thermal Resistance Junction to Air



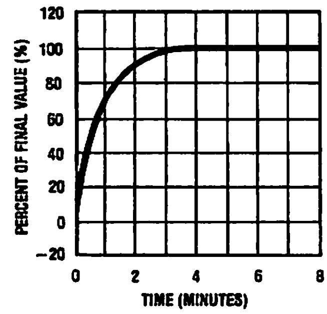
DS005516-25

Thermal Time Constant



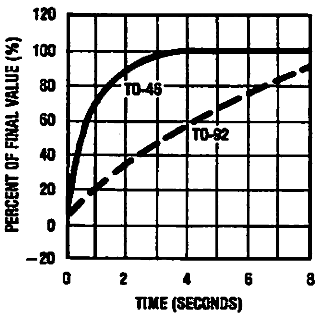
DS005516-26

Thermal Response in Still Air



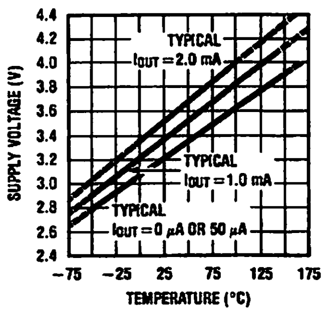
DS005516-27

Thermal Response in Stirred Oil Bath



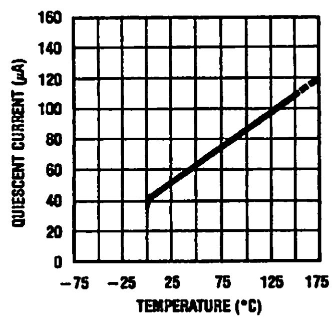
DS005516-28

Minimum Supply Voltage vs. Temperature



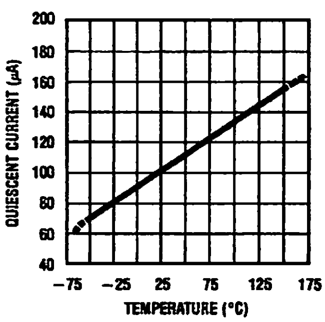
DS005516-29

Quiescent Current vs. Temperature (In Circuit of *Figure 1.*)



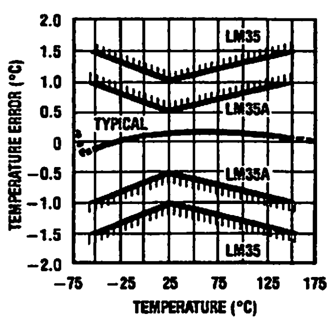
DS005516-30

Quiescent Current vs. Temperature (In Circuit of *Figure 2.*)



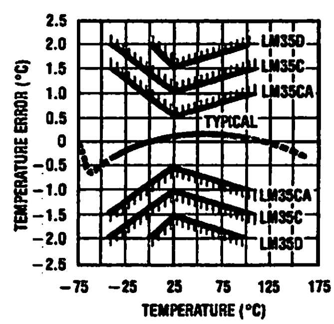
DS005516-31

Accuracy vs. Temperature (Guaranteed)



DS005516-32

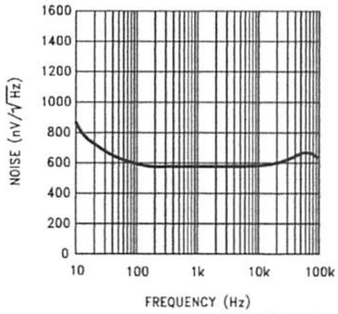
Accuracy vs. Temperature (Guaranteed)



DS005516-33

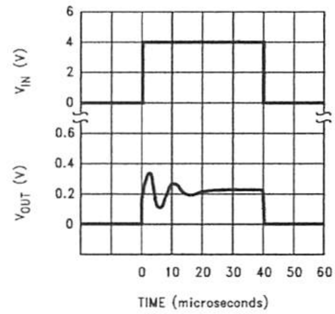
Typical Performance Characteristics (Continued)

Noise Voltage



DS005516-34

Start-Up Response



DS005516-35

Applications

The LM35 can be applied easily in the same way as other integrated-circuit temperature sensors. It can be glued or cemented to a surface and its temperature will be within about 0.01˚C of the surface temperature.

This presumes that the ambient air temperature is almost the same as the surface temperature; if the air temperature were much higher or lower than the surface temperature, the actual temperature of the LM35 die would be at an intermediate temperature between the surface temperature and the air temperature. This is expecially true for the TO-92 plastic package, where the copper leads are the principal thermal path to carry heat into the device, so its temperature might be closer to the air temperature than to the surface temperature.

To minimize this problem, be sure that the wiring to the LM35, as it leaves the device, is held at the same temperature as the surface of interest. The easiest way to do this is to cover up these wires with a bead of epoxy which will insure that the leads and wires are all at the same temperature as the surface, and that the LM35 die's temperature will not be affected by the air temperature.

The TO-46 metal package can also be soldered to a metal surface or pipe without damage. Of course, in that case the V− terminal of the circuit will be grounded to that metal. Alternatively, the LM35 can be mounted inside a sealed-end metal tube, and can then be dipped into a bath or screwed into a threaded hole in a tank. As with any IC, the LM35 and accompanying wiring and circuits must be kept insulated and dry, to avoid leakage and corrosion. This is especially true if the circuit may operate at cold temperatures where condensation can occur. Printed-circuit coatings and varnishes such as Humiseal and epoxy paints or dips are often used to insure that moisture cannot corrode the LM35 or its connections.

These devices are sometimes soldered to a small light-weight heat fin, to decrease the thermal time constant and speed up the response in slowly-moving air. On the other hand, a small thermal mass may be added to the sensor, to give the steadiest reading despite small deviations in the air temperature.

Temperature Rise of LM35 Due To Self-heating (Thermal Resistance, θ_{JA})

	TO-46, no heat sink	TO-46*, small heat fin	TO-92, no heat sink	TO-92**, small heat fin	SO-8 no heat sink	SO-8** small heat fin	TO-220 no heat sink
Still air	400˚C/W	100˚C/W	180˚C/W	140˚C/W	220˚C/W	110˚C/W	90˚C/W
Moving air	100˚C/W	40˚C/W	90˚C/W	70˚C/W	105˚C/W	90˚C/W	26˚C/W
Still oil	100˚C/W	40˚C/W	90˚C/W	70˚C/W			
Stirred oil	50˚C/W	30˚C/W	45˚C/W	40˚C/W			
(Clamped to metal, Infinite heat sink)		(24˚C/W)				(55˚C/W)	

*Wakefield type 201, or 1" disc of 0.020" sheet brass, soldered to case, or similar.

**TO-92 and SO-8 packages glued and leads soldered to 1" square of 1/16" printed circuit board with 2 oz. foil or similar.

Typical Applications

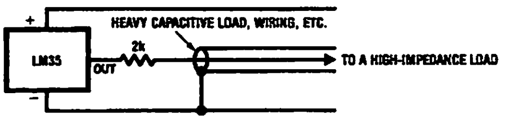


FIGURE 3. LM35 with Decoupling from Capacitive Load

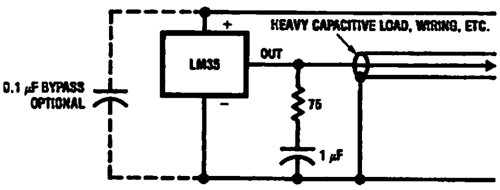


FIGURE 4. LM35 with R-C Damper

CAPACITIVE LOADS

.ike most micropower circuits, the LM35 has a limited ability o drive heavy capacitive loads. The LM35 by itself is able to lrive 50 pf without special precautions. If heavier loads are inticipated, it is easy to isolate or decouple the load with a esistor; see *Figure 3*. Or you can improve the tolerance of :apacitance with a series R-C damper from output to jround; see *Figure 4*.

Vhen the LM35 is applied with a 200Ω load resistor as hown in *Figure 5*, *Figure 6* or *Figure 8* it is relatively immune o wiring capacitance because the capacitance forms a by-)ass from ground to input, not on the output. However, as vith any linear circuit connected to wires in a hostile environ-nent, its performance can be affected adversely by intense lectromagnetic sources such as relays, radio transmitters, notors with arcing brushes, SCR transients, etc, as its wiring :an act as a receiving antenna and its internal junctions can ict as rectifiers. For best results in such cases, a bypass ca-)acitor from V_{IN} to ground and a series R-C damper such as '5Ω in series with 0.2 or 1 μF from output to ground are often iseful. These are shown in *Figure 13*, *Figure 14*, and *Figure 16*.

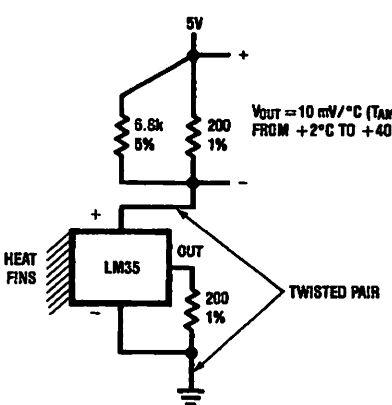


FIGURE 5. Two-Wire Remote Temperature Sensor (Grounded Sensor)

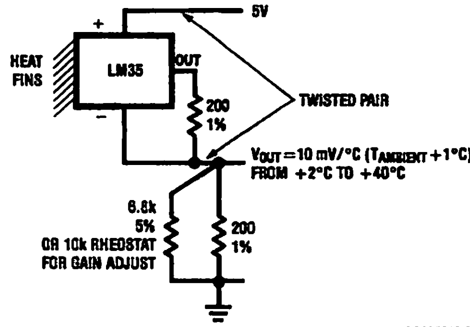


FIGURE 6. Two-Wire Remote Temperature Sensor (Output Referred to Ground)

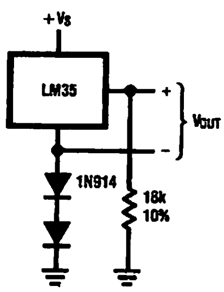


FIGURE 7. Temperature Sensor, Single Supply, −55° to +150°C

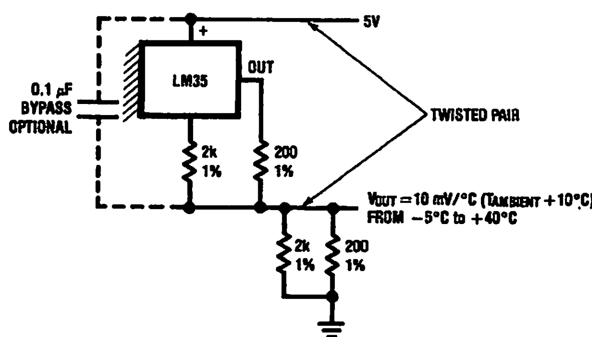


FIGURE 8. Two-Wire Remote Temperature Sensor (Output Referred to Ground)

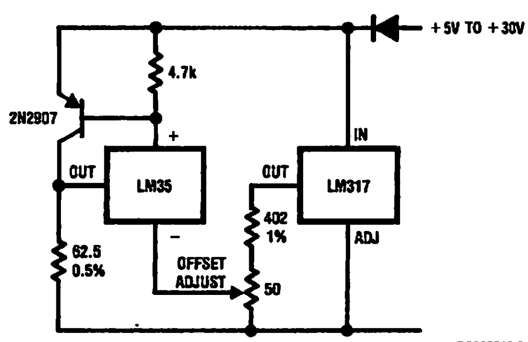


FIGURE 9. 4-To-20 mA Current Source (0°C to +100°C)

Typical Applications (Continued)

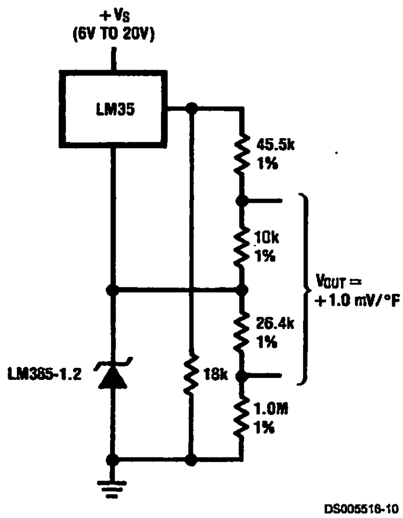


FIGURE 10. Fahrenheit Thermometer

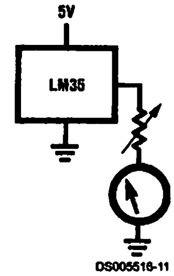


FIGURE 11. Centigrade Thermometer (Analog Meter)

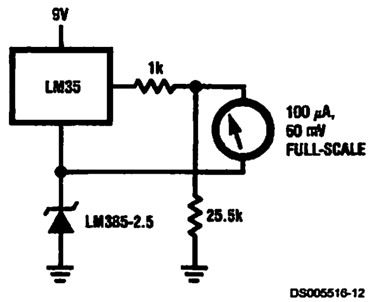


FIGURE 12. Fahrenheit ThermometerExpanded Scale Thermometer
(50° to 80° Fahrenheit, for Example Shown)

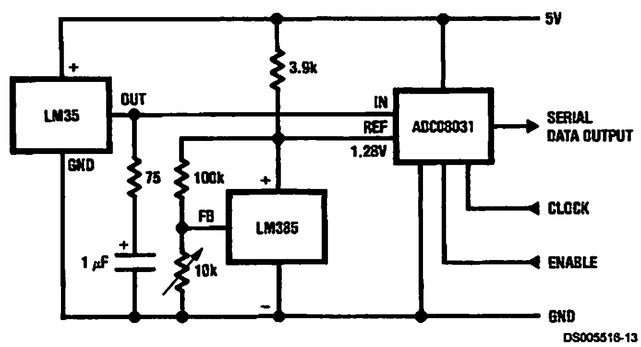


FIGURE 13. Temperature To Digital Converter (Serial Output) (+128°C Full Scale)

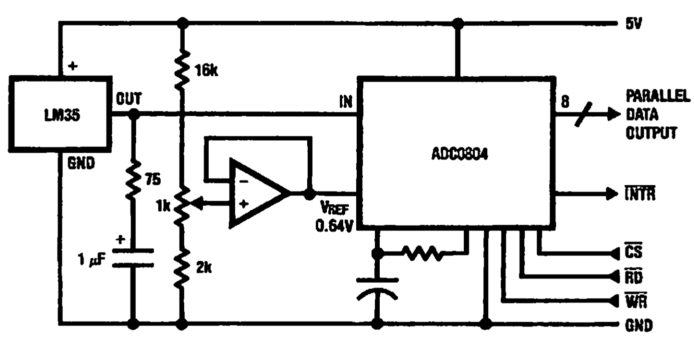
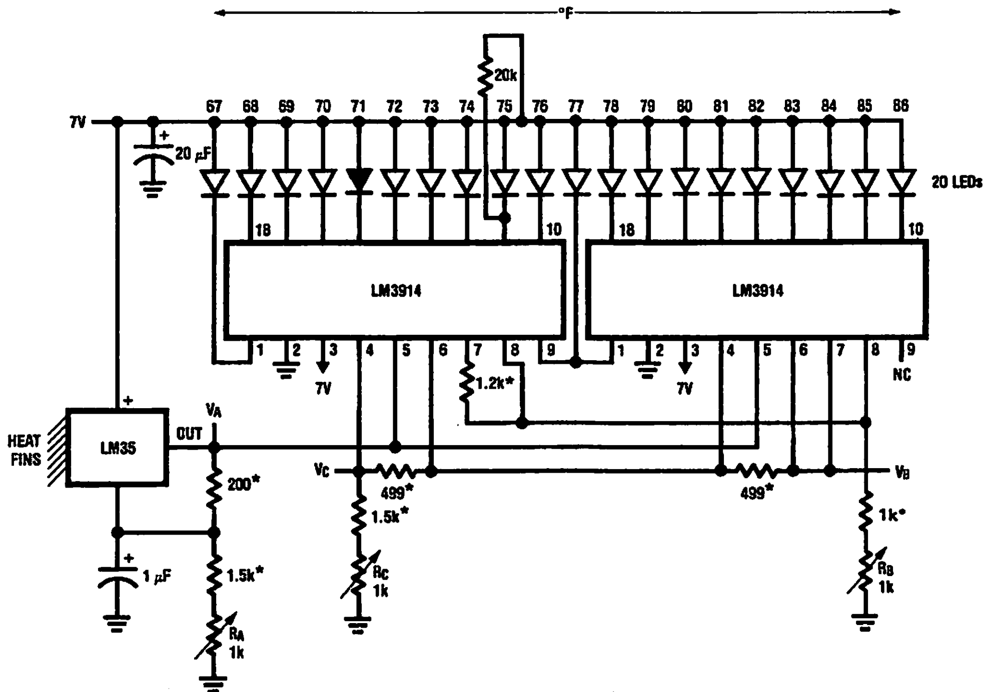


FIGURE 14. Temperature To Digital Converter (Parallel TRI-STATE™ Outputs for Standard Data Bus to µP Interface) (128°C Full Scale)

Typical Applications (Continued)



*=1% or 2% film resistor
Trim R_B for V_B=3.075V
Trim R_C for V_C=1.955V
Trim R_A for V_A=0.075V + 100mV/°C x $T_{ambient}$
Example, V_A=2.275V at 22°C

FIGURE 15. Bar-Graph Temperature Display (Dot Mode)

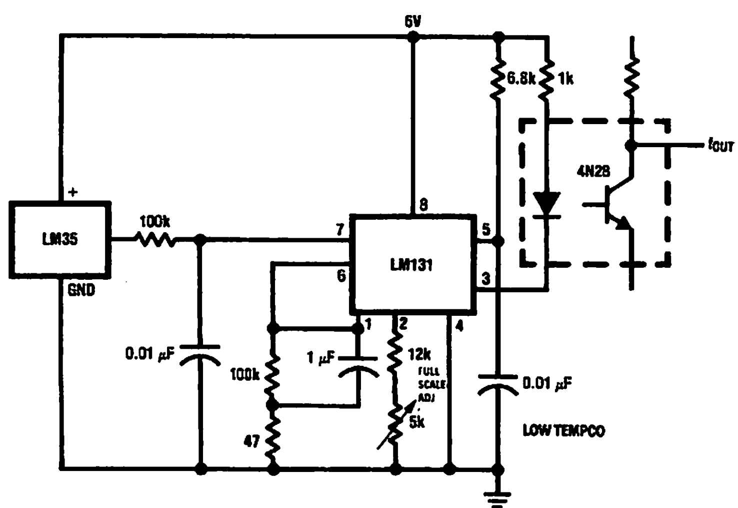
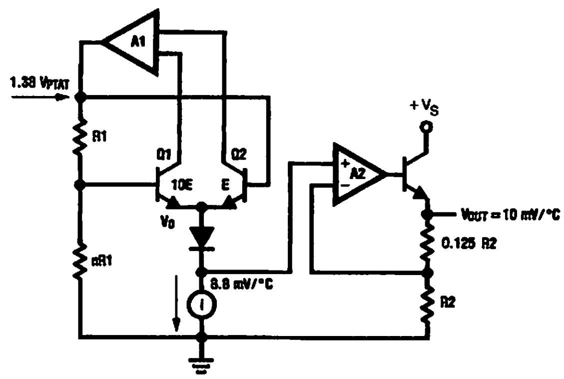


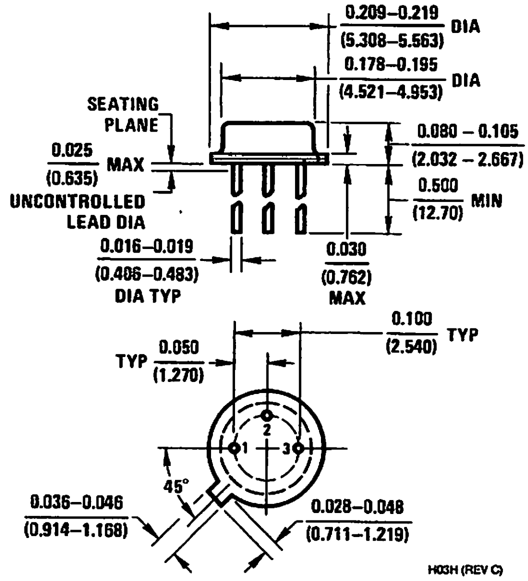
FIGURE 16. LM35 With Voltage-To-Frequency Converter And Isolated Output (2°C to +150°C; 20 Hz to 1500 Hz)

Block Diagram

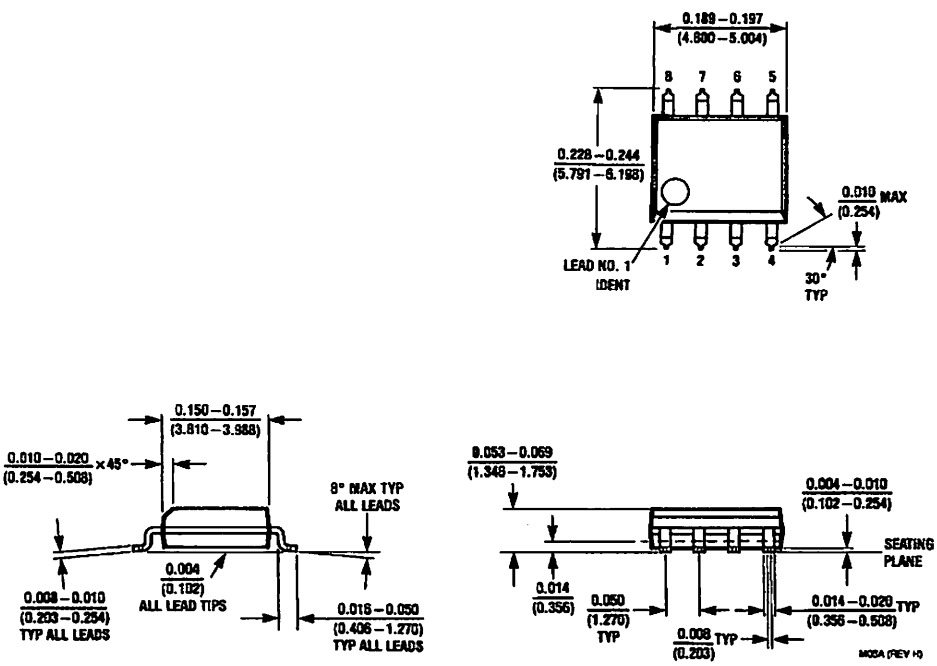


DS005516-23

ᴾhysical Dimensions inches (millimeters) unless otherwise noted

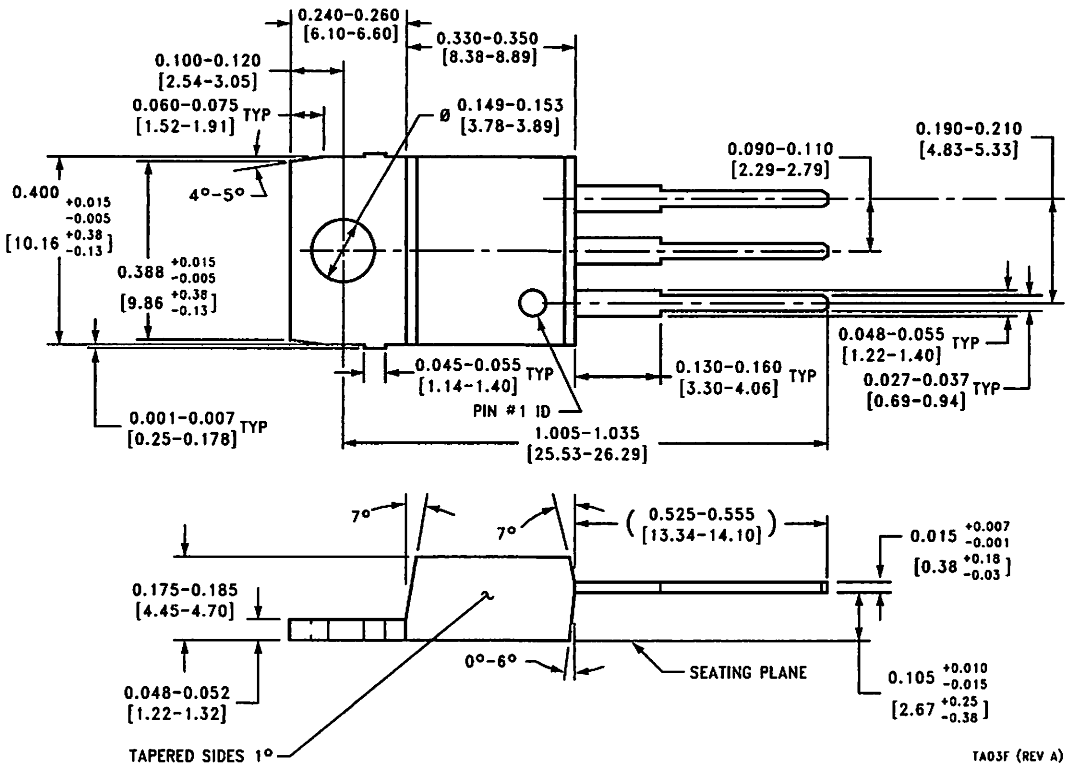


TO-46 Metal Can Package (H)
Order Number LM35H, LM35AH, LM35CH, LM35CAH, or LM35DH
NS Package Number H03H

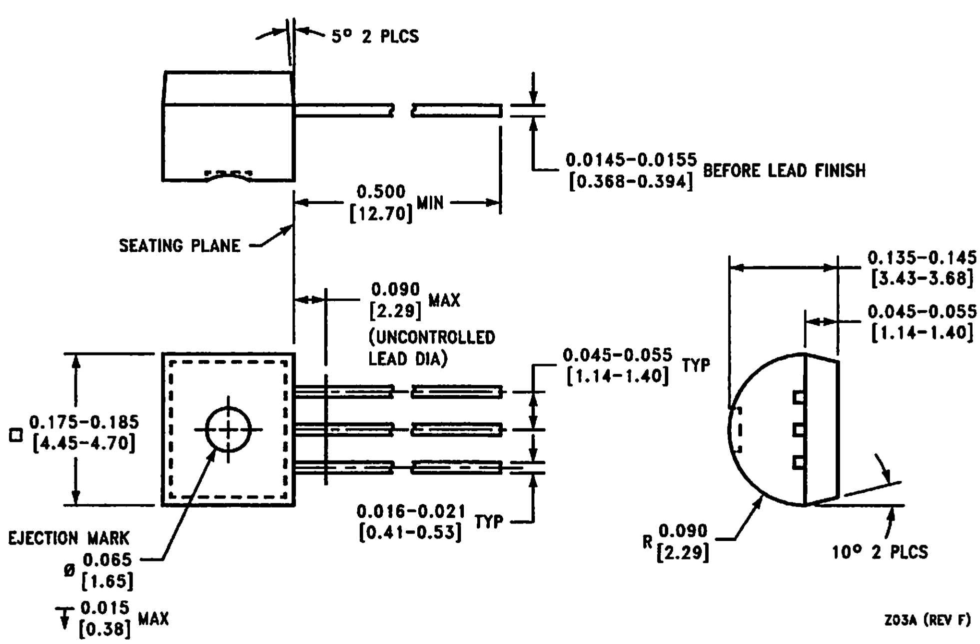


SO-8 Molded Small Outline Package (M)
Order Number LM35DM
NS Package Number M08A

Physical Dimensions inches (millimeters) unless otherwise noted (Continued)



Power Package TO-220 (T)
Order Number LM35DT
NS Package Number TA03F



TO-92 Plastic Package (Z)
Order Number LM35CZ, LM35CAZ or LM35DZ
NS Package Number Z03A

Notes

IFE SUPPORT POLICY

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2. A critical component is any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

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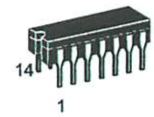
MC54/74HC14A

Hex Schmitt-Trigger Inverter
High–Performance Silicon–Gate CMOS

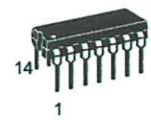
The MC54/74HC14A is identical in pinout to the LS14, LS04 and the HC04. The device inputs are compatible with Standard CMOS outputs; with pullup resistors, they are compatible with LSTTL outputs.

The HC14A is useful to "square up" slow input rise and fall times. Due to hysteresis voltage of the Schmitt trigger, the HC14A finds applications in noisy environments.

- Output Drive Capability: 10 LSTTL Loads
- Outputs Directly Interface to CMOS, NMOS and TTL
- Operating Voltage Range: 2 to 6V
- Low Input Current: 1μA
- High Noise Immunity Characteristic of CMOS Devices
- In Compliance With the JEDEC Standard No. 7A Requirements
- Chip Complexity: 60 FETs or 15 Equivalent Gates

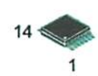


J SUFFIX
CERAMIC PACKAGE
CASE 632–08



N SUFFIX
PLASTIC PACKAGE
CASE 646–06

D SUFFIX
SOIC PACKAGE
CASE 751A–03

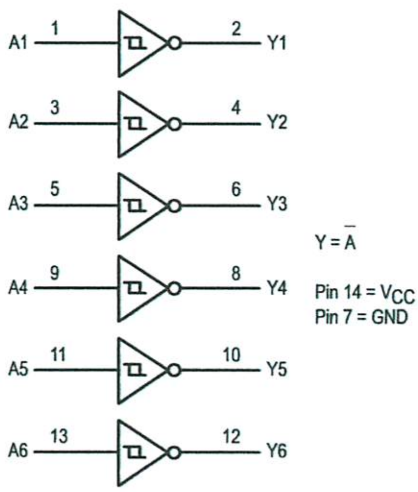


DT SUFFIX
TSSOP PACKAGE
CASE 948G–01

ORDERING INFORMATION

MC54HCXXAJ	Ceramic
MC74HCXXAN	Plastic
MC74HCXXAD	SOIC
MC74HCXXADT	TSSOP

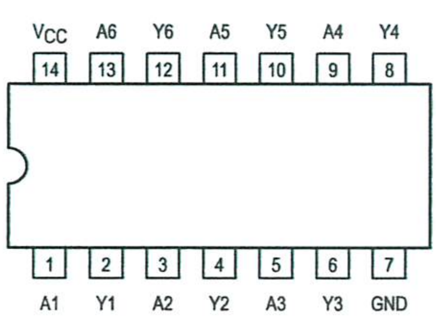
LOGIC DIAGRAM



FUNCTION TABLE

Inputs	Outputs
A	Y
L	H
H	L

Pinout: 14–Lead Packages (Top View)



MAXIMUM RATINGS*

Symbol	Parameter	Value	Unit
V_{CC}	DC Supply Voltage (Referenced to GND)	– 0.5 to + 7.0	V
V_{in}	DC Input Voltage (Referenced to GND)	– 0.5 to V_{CC} + 0.5	V
V_{out}	DC Output Voltage (Referenced to GND)	– 0.5 to V_{CC} + 0.5	V
I_{in}	DC Input Current, per Pin	± 20	mA
I_{out}	DC Output Current, per Pin	± 25	mA
I_{CC}	DC Supply Current, V_{CC} and GND Pins	± 50	mA
P_D	Power Dissipation in Still Air, Plastic or Ceramic DIP† SOIC Package† TSSOP Package†	750 500 450	mW
T_{stg}	Storage Temperature Range	– 65 to + 150	°C
T_L	Lead Temperature, 1 mm from Case for 10 Seconds Plastic DIP, SOIC or TSSOP Package Ceramic DIP	 260 300	°C

* Maximum Ratings are those values beyond which damage to the device may occur.
Functional operation should be restricted to the Recommended Operating Conditions.
†Derating — Plastic DIP: – 10 mW/°C from 65° to 125°C
Ceramic DIP: – 10 mW/°C from 100° to 125°C
SOIC Package: – 7 mW/°C from 65° to 125°C
TSSOP Package: – 6.1 mW/°C from 65° to 125°C

For high frequency or heavy load considerations, see Chapter 2 of the Motorola High–Speed CMOS Data Book (DL129/D).

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high–impedance circuit. For proper operation, V_{in} and V_{out} should be constrained to the range GND ≤ (V_{in} or V_{out}) ≤ V_{CC}.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either GND or V_{CC}). Unused outputs must be left open.

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min	Max	Unit
V_{CC}	DC Supply Voltage (Referenced to GND)	2.0	6.0	V
V_{in}, V_{out}	DC Input Voltage, Output Voltage (Referenced to GND)	0	V_{CC}	V
T_A	Operating Temperature Range, All Package Types	– 55	+ 125	°C
t_r, t_f	Input Rise/Fall Time (Figure 1) V_{CC} = 2.0 V V_{CC} = 4.5 V V_{CC} = 6.0 V	0 0 0	No Limit* No Limit* No Limit*	ns

* When V_{in} = 50% V_{CC}, I_{CC} > 1mA

DC CHARACTERISTICS (Voltages Referenced to GND)

Symbol	Parameter	Condition	V_{CC} V	Guaranteed Limit –55 to 25°C	≤85°C	≤125°C	Unit
V_{T+} max	Maximum Positive–Going Input Threshold Voltage (Figure 3)	V_{out} = 0.1V $\lvert I_{out}\rvert \le 20\mu A$	2.0 3.0 4.5 6.0	1.50 2.15 3.15 4.20	1.50 2.15 3.15 4.20	1.50 2.15 3.15 4.20	V
V_{T+} min	Minimum Positive–Going Input Threshold Voltage (Figure 3)	V_{out} = 0.1V $\lvert I_{out}\rvert \le 20\mu A$	2.0 3.0 4.5 6.0	1.0 1.5 2.3 3.0	0.95 1.45 2.25 2.95	0.95 1.45 2.25 2.95	V
V_{T-} max	Maximum Negative–Going Input Threshold Voltage (Figure 3)	$V_{out} = V_{CC} - 0.1V$ $\lvert I_{out}\rvert \le 20\mu A$	2.0 3.0 4.5 6.0	0.9 1.4 2.0 2.6	0.95 1.45 2.05 2.65	0.95 1.45 2.05 2.65	V
V_{T-} min	Minimum Negative–Going Input Threshold Voltage (Figure 3)	$V_{out} = V_{CC} - 0.1V$ $\lvert I_{out}\rvert \le 20\mu A$	2.0 3.0 4.5 6.0	0.3 0.5 0.9 1.2	0.3 0.5 0.9 1.2	0.3 0.5 0.9 1.2	V
$V_H$max Note 2	Maximum Hysteresis Voltage (Figure 3)	V_{out} = 0.1V or $V_{CC} - 0.1V$ $\lvert I_{out}\rvert \le 20\mu A$	2.0 3.0 4.5 6.0	1.20 1.65 2.25 3.00	1.20 1.65 2.25 3.00	1.20 1.65 2.25 3.00	V
$V_H$min Note 2	Minimum Hysteresis Voltage (Figure 3)	V_{out} = 0.1V or $V_{CC} - 0.1V$ $\lvert I_{out}\rvert \le 20\mu A$	2.0 3.0 4.5 6.0	0.20 0.25 0.40 0.50	0.20 0.25 0.40 0.50	0.20 0.25 0.40 0.50	V
V_{OH}	Minimum High–Level Output Voltage	$V_{in} \le V_{T-}$ min $\lvert I_{out}\rvert \le 20\mu A$	2.0 4.5 6.0	1.9 4.4 5.9	1.9 4.4 5.9	1.9 4.4 5.9	V
		$V_{in} \le V_{T-}$ min $\lvert I_{out}\rvert \le 2.4mA$ $\lvert I_{out}\rvert \le 4.0mA$ $\lvert I_{out}\rvert \le 5.2mA$	3.0 4.5 6.0	2.48 3.98 5.48	2.34 3.84 5.34	2.20 3.70 5.20	
V_{OL}	Maximum Low–Level Output Voltage	$V_{in} \ge V_{T+}$ max $\lvert I_{out}\rvert \le 20\mu A$	2.0 4.5 6.0	0.1 0.1 0.1	0.1 0.1 0.1	0.1 0.1 0.1	V
		$V_{in} \ge V_{T+}$ max $\lvert I_{out}\rvert \le 2.4mA$ $\lvert I_{out}\rvert \le 4.0mA$ $\lvert I_{out}\rvert \le 5.2mA$	3.0 4.5 6.0	0.26 0.26 0.26	0.33 0.33 0.33	0.40 0.40 0.40	
I_{in}	Maximum Input Leakage Current	$V_{in} = V_{CC}$ or GND	6.0	±0.1	±1.0	±1.0	µA
I_{CC}	Maximum Quiescent Supply Current (per Package)	$V_{in} = V_{CC}$ or GND $I_{out} = 0\mu A$	6.0	1.0	10	40	µA

1. Information on typical parametric values along with frequency or heavy load considerations can be found in Chapter 2 of the Motorola High–Speed CMOS Data Book (DL129/D).
2. $V_H$min > (V_{T+} min) – (V_{T-} max); $V_H$max = (V_{T+} max) – (V_{T-} min).

AC CHARACTERISTICS (C_L = 50pF, Input t_r = t_f = 6ns)

Symbol	Parameter	V_{CC} V	Guaranteed Limit			Unit
			–55 to 25°C	≤85°C	≤125°C	
t_{PLH}, t_{PHL}	Maximum Propagation Delay, Input A or B to Output Y (Figures 1 and 2)	2.0 3.0 4.5 6.0	75 30 15 13	95 40 19 16	110 55 22 19	ns
t_{TLH}, t_{THL}	Maximum Output Transition Time, Any Output (Figures 1 and 2)	2.0 3.0 4.5 6.0	75 27 15 13	95 32 19 16	110 36 22 19	ns
C_{in}	Maximum Input Capacitance		10	10	10	pF

NOTE: For propagation delays with loads other than 50 pF, and information on typical parametric values, see Chapter 2 of the Motorola High–Speed CMOS Data Book (DL129/D).

		Typical @ 25°C, V_{CC} = 5.0 V	
C_{PD}	Power Dissipation Capacitance (Per Inverter)*	22	pF

* Used to determine the no–load dynamic power consumption: $P_D = C_{PD} V_{CC}^2 f + I_{CC} V_{CC}$. For load considerations, see Chapter 2 of the Motorola High–Speed CMOS Data Book (DL129/D).

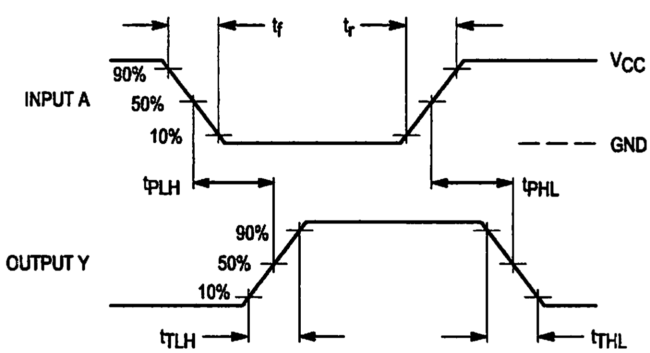
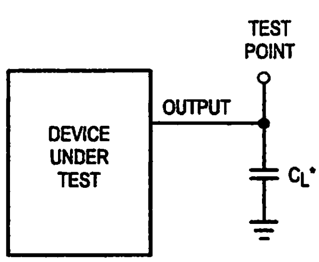


Figure 1. Switching Waveforms



*Includes all probe and jig capacitance

Figure 2. Test Circuit

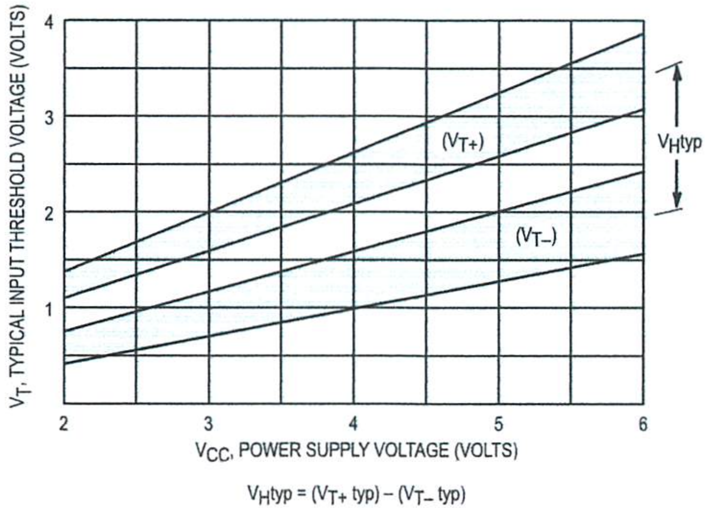


Figure 3. Typical Input Threshold, V_{T+}, V_{T-} versus Power Supply Voltage

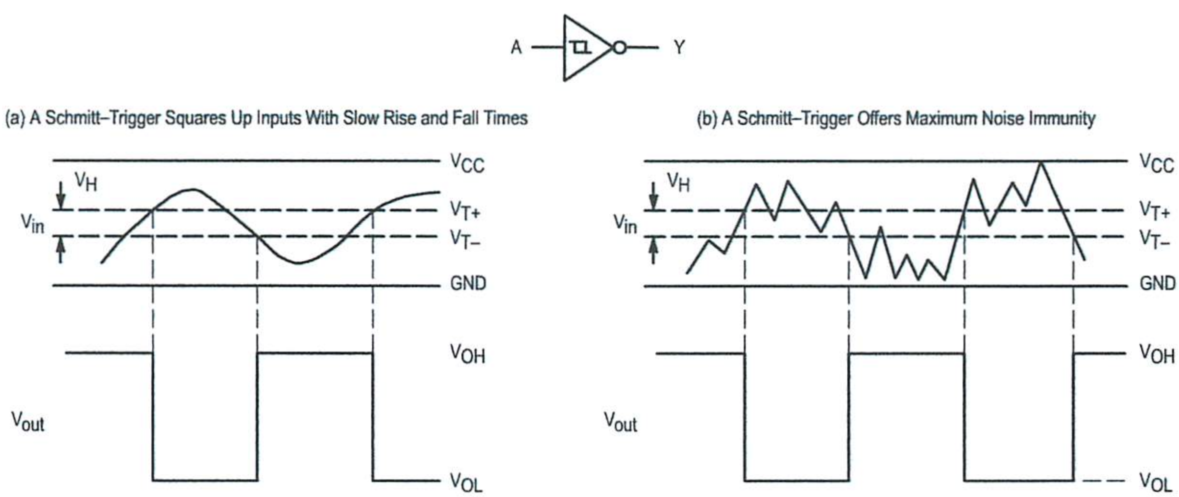
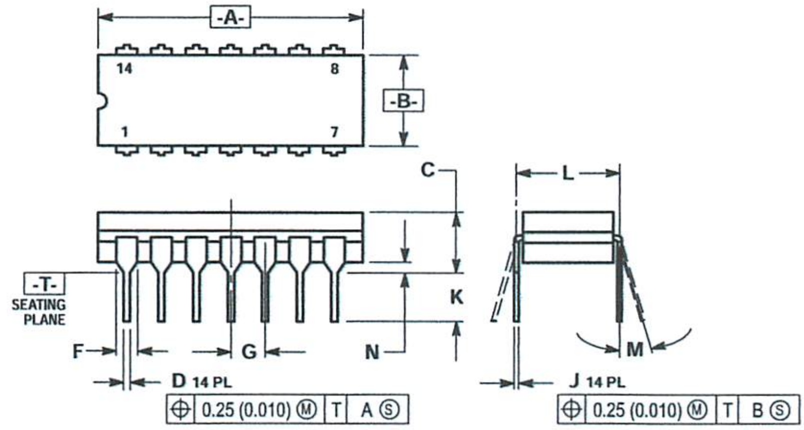


Figure 4. Typical Schmitt–Trigger Applications

OUTLINE DIMENSIONS

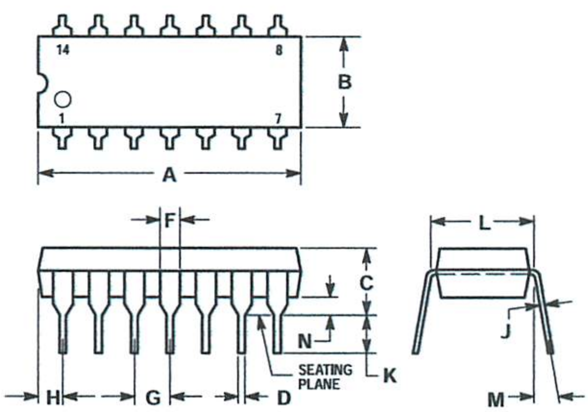
J SUFFIX
CERAMIC DIP PACKAGE
CASE 632–08
ISSUE Y



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. DIMENSION L TO CENTER OF LEAD WHEN FORMED PARALLEL.
4. DIMESNION F MAY NARROW TO 0.76 (0.030) WHERE THE LEAD ENTERS THE CERAMIC BODY.

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.750	0.785	19.05	19.94
B	0.245	0.280	6.23	7.11
C	0.155	0.200	3.94	5.08
D	0.015	0.020	0.39	0.50
F	0.055	0.065	1.40	1.65
G	0.100 BSC		2.54 BSC	
J	0.008	0.015	0.21	0.38
K	0.125	0.170	3.18	4.31
L	0.300 BSC		7.62 BSC	
M	0°	15°	0°	15°
N	0.020	0.040	0.51	1.01

N SUFFIX
PLASTIC DIP PACKAGE
CASE 646–06
ISSUE L

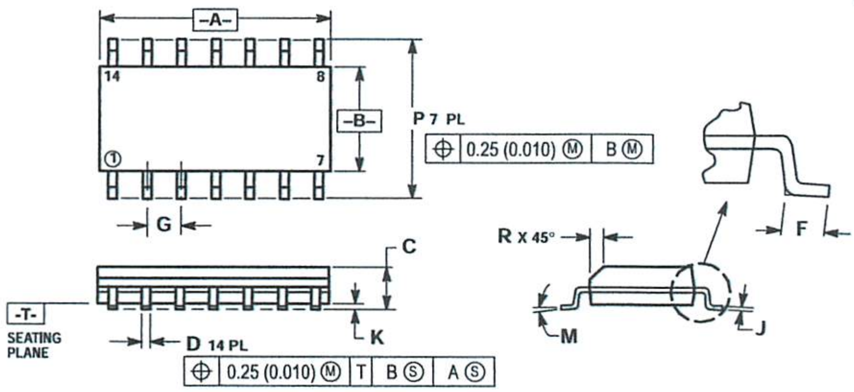


NOTES:
1. LEADS WITHIN 0.13 (0.005) RADIUS OF TRUE POSITION AT SEATING PLANE AT MAXIMUM MATERIAL CONDITION.
2. DIMENSION L TO CENTER OF LEADS WHEN FORMED PARALLEL.
3. DIMENSION B DOES NOT INCLUDE MOLD FLASH.
4. ROUNDED CORNERS OPTIONAL.

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.715	0.770	18.16	19.56
B	0.240	0.260	6.10	6.60
C	0.145	0.185	3.69	4.69
D	0.015	0.021	0.38	0.53
F	0.040	0.070	1.02	1.78
G	0.100 BSC		2.54 BSC	
H	0.052	0.095	1.32	2.41
J	0.008	0.015	0.20	0.38
K	0.115	0.135	2.92	3.43
L	0.300 BSC		7.62 BSC	
M	0°	10°	0°	10°
N	0.015	0.039	0.39	1.01

OUTLINE DIMENSIONS

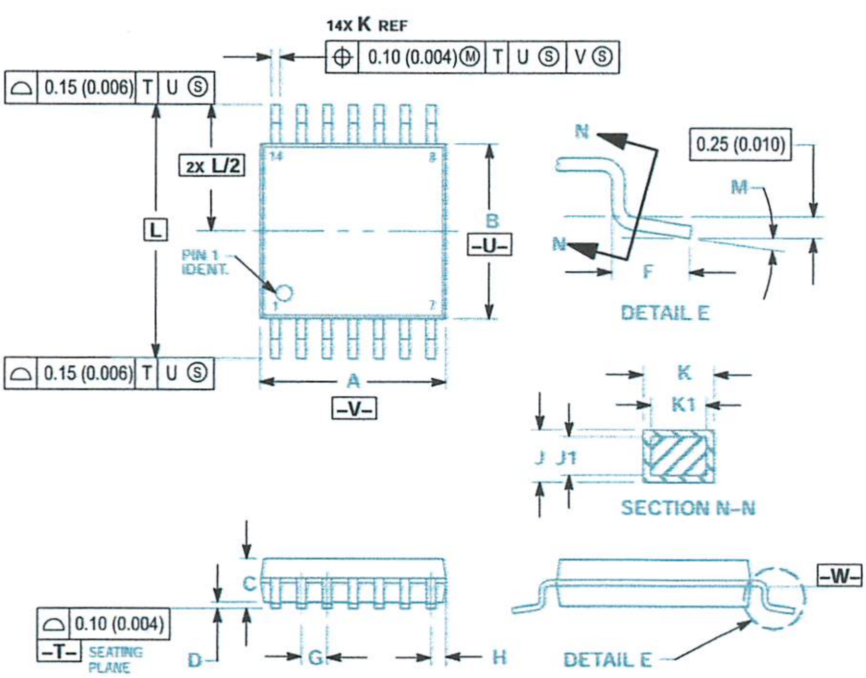
D SUFFIX
PLASTIC SOIC PACKAGE
CASE 751A–03
ISSUE F



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSIONS A AND B DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
5. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127 (0.005) TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	8.55	8.75	0.337	0.344
B	3.80	4.00	0.150	0.157
C	1.35	1.75	0.054	0.068
D	0.35	0.49	0.014	0.019
F	0.40	1.25	0.016	0.049
G	1.27 BSC		0.050 BSC	
J	0.19	0.25	0.008	0.009
K	0.10	0.25	0.004	0.009
M	0°	7°	0°	7°
P	5.80	6.20	0.228	0.244
R	0.25	0.50	0.010	0.019

DT SUFFIX
PLASTIC TSSOP PACKAGE
CASE 948G–01
ISSUE O



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION A DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH OR GATE BURRS SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
4. DIMENSION B DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.25 (0.010) PER SIDE.
5. DIMENSION K DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 (0.003) TOTAL IN EXCESS OF THE K DIMENSION AT MAXIMUM MATERIAL CONDITION.
6. TERMINAL NUMBERS ARE SHOWN FOR REFERENCE ONLY.
7. DIMENSION A AND B ARE TO BE DETERMINED AT DATUM PLANE –W–.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	4.90	5.10	0.193	0.200
B	4.30	4.50	0.169	0.177
C	—	1.20	—	0.047
D	0.05	0.15	0.002	0.006
F	0.50	0.75	0.020	0.030
G	0.65 BSC		0.026 BSC	
H	0.50	0.60	0.020	0.024
J	0.09	0.20	0.004	0.008
J1	0.09	0.16	0.004	0.006
K	0.19	0.30	0.007	0.012
K1	0.19	0.25	0.007	0.010
L	6.40 BSC		0.252 BSC	
M	0°	8°	0°	8°

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6F Seibu–Butsuryu–Center, 3–14–2 Tatsumi Koto–Ku, Tokyo 135, Japan. 03–3521–8315

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51 Ting Kok Road, Tai Po, N.T., Hong Kong. 852–26629298

MOTOROLA

◊ CODELINE

MC54/74HC14A/D

MOTOROLA

SN54/74LS47

BCD TO 7-SEGMENT DECODER/DRIVER

The SN54/74LS47 are Low Power Schottky BCD to 7-Segment Decoder/Drivers consisting of NAND gates, input buffers and seven AND-OR-INVERT gates. They offer active LOW, high sink current outputs for driving indicators directly. Seven NAND gates and one driver are connected in pairs to make BCD data and its complement available to the seven decoding AND-OR-INVERT gates. The remaining NAND gate and three input buffers provide lamp test, blanking input/ripple-blanking output and ripple-blanking input.

The circuits accept 4-bit binary-coded-decimal (BCD) and, depending on the state of the auxiliary inputs, decodes this data to drive a 7-segment display indicator. The relative positive-logic output levels, as well as conditions required at the auxiliary inputs, are shown in the truth tables. Output configurations of the SN54/74LS47 are designed to withstand the relatively high voltages required for 7-segment indicators.

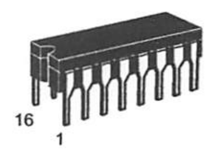
These outputs will withstand 15 V with a maximum reverse current of 250 µA. Indicator segments requiring up to 24 mA of current may be driven directly from the SN74LS47 high performance output transistors. Display patterns for BCD input counts above nine are unique symbols to authenticate input conditions.

The SN54/74LS47 incorporates automatic leading and/or trailing-edge zero-blanking control (RBI and RBO). Lamp test (LT) may be performed at any time which the BI/RBO node is a HIGH level. This device also contains an overriding blanking input (BI) which can be used to control the lamp intensity by varying the frequency and duty cycle of the BI input signal or to inhibit the outputs.

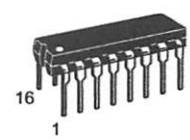
- Lamp Intensity Modulation Capability (BI/RBO)
- Open Collector Outputs
- Lamp Test Provision
- Leading/Trailing Zero Suppression
- Input Clamp Diodes Limit High-Speed Termination Effects

BCD TO 7-SEGMENT DECODER/DRIVER

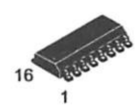
LOW POWER SCHOTTKY



J SUFFIX
CERAMIC
CASE 620-09



N SUFFIX
PLASTIC
CASE 648-08

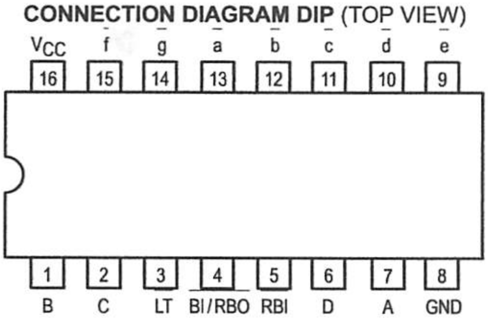


D SUFFIX
SOIC
CASE 751B-03

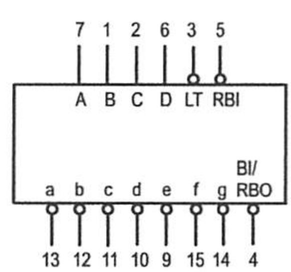
ORDERING INFORMATION

SN54LSXXJ	Ceramic
SN74LSXXN	Plastic
SN74LSXXD	SOIC

CONNECTION DIAGRAM DIP (TOP VIEW)



LOGIC SYMBOL

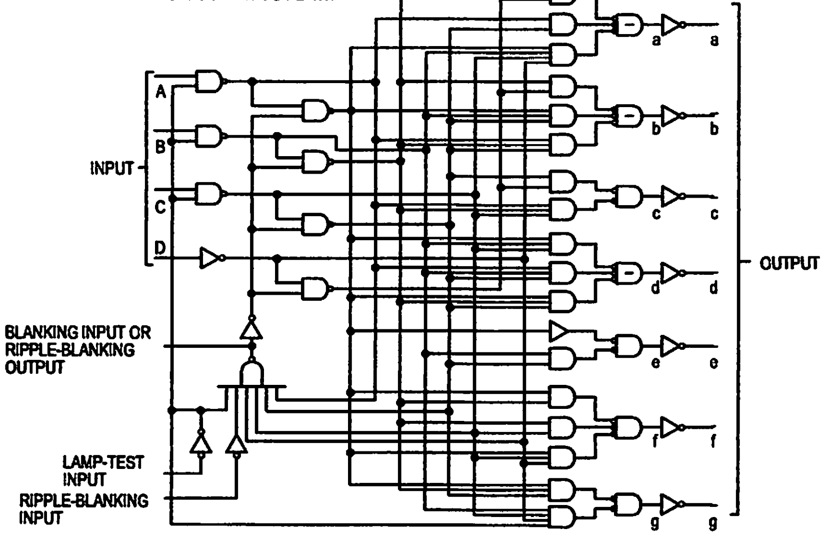


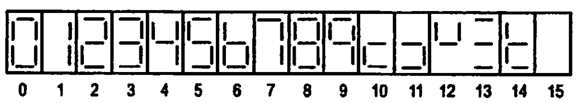
PIN NAMES **LOADING** (Note a)

		HIGH	LOW
A, B, C, D	BCD Inputs	0.5 U.L.	0.25 U.L.
RBI	Ripple-Blanking Input	0.5 U.L.	0.25 U.L.
LT	Lamp-Test Input	0.5 U.L.	0.25 U.L.
BI/RBO	Blanking Input or	0.5 U.L.	0.75 U.L.
	Ripple-Blanking Output	1.2 U.L.	2.0 U.L.
a, to g	Outputs	Open-Collector	15 (7.5) U.L.

NOTES:
a) 1 Unit Load (U.L.) = 40 µA HIGH, 1.6 mA LOW.
b) Output current measured at V_{OUT} = 0.5 V
The Output LOW drive factor is 7.5 U.L. for Military (54) and 15 U.L. for Commercial (74) Temperature Ranges.

LOGIC DIAGRAM





NUMERICAL DESIGNATIONS — RESULTANT DISPLAYS

TRUTH TABLE

DECIMAL OR FUNCTION	INPUTS							OUTPUTS							NOTE
	$\overline{LT}$	$\overline{RBI}$	D	C	B	A	$\overline{BI/RBO}$	$\bar{a}$	$\bar{b}$	$\bar{c}$	$\bar{d}$	$\bar{e}$	$\bar{f}$	$\bar{g}$	
0	H	H	L	L	L	L	H	L	L	L	L	L	L	H	A
1	H	X	L	L	L	H	H	H	L	L	H	H	H	H	A
2	H	X	L	L	H	L	H	L	L	H	L	L	H	L	
3	H	X	L	L	H	H	H	L	L	L	L	H	H	L	
4	H	X	L	H	L	L	H	H	L	L	H	H	L	L	
5	H	X	L	H	L	H	H	L	H	L	L	H	L	L	
6	H	X	L	H	H	L	H	H	H	L	L	L	L	L	
7	H	X	L	H	H	H	H	L	L	L	H	H	H	H	
8	H	X	H	L	L	L	H	L	L	L	L	L	L	L	
9	H	X	H	L	L	H	H	L	L	L	H	H	L	L	
10	H	X	H	L	H	L	H	H	H	H	L	L	H	L	
11	H	X	H	L	H	H	H	H	H	L	L	H	H	L	
12	H	X	H	H	L	L	H	H	L	H	H	H	L	L	
13	H	X	H	H	L	H	H	L	H	H	L	H	L	L	
14	H	X	H	H	H	L	H	H	H	H	L	L	L	L	
15	H	X	H	H	H	H	H	H	H	H	H	H	H	H	
BI	X	X	X	X	X	X	L	H	H	H	H	H	H	H	B
RBI	H	L	L	L	L	L	L	H	H	H	H	H	H	H	C
LT	L	X	X	X	X	X	H	L	L	L	L	L	L	L	D

H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial

NOTES:

(A) $\overline{BI/RBO}$ is wire-AND logic serving as blanking Input ($\overline{BI}$) and/or ripple-blanking output ($\overline{RBO}$). The blanking out ($\overline{BI}$) must be open or held at a HIGH level when output functions 0 through 15 are desired, and ripple-blanking input ($\overline{RBI}$) must be open or at a HIGH level if blanking of a decimal 0 is not desired. X = input may be HIGH or LOW.

(B) When a LOW level is applied to the blanking input (forced condition) all segment outputs go to a LOW level regardless of the state of any other input condition.

(C) When ripple-blanking input ($\overline{RBI}$) and inputs A, B, C, and D are at LOW level, with the lamp test input at HIGH level, all segment outputs go to a HIGH level and the ripple-blanking output ($\overline{RBO}$) goes to a LOW level (response condition).

(D) When the blanking input/ripple-blanking output ($\overline{BI/RBO}$) is open or held at a HIGH level, and a LOW level is applied to lamp test input, all segment outputs go to a LOW level.

GUARANTEED OPERATING RANGES

Symbol	Parameter		Min	Typ	Max	Unit
V_{CC}	Supply Voltage	54 74	4.5 4.75	5.0 5.0	5.5 5.25	V
T_A	Operating Ambient Temperature Range	54 74	−55 0	25 25	125 70	°C
I_{OH}	Output Current — High BI/RBO	54, 74			−50	µA
I_{OL}	Output Current — Low $\overline{BI}/\overline{RBO}$ BI/RBO	54 74			1.6 3.2	mA
$V_{O\ (off)}$	Off-State Output Voltage $\bar{a}$ to $\bar{g}$	54, 74			15	V
$I_{O\ (on)}$	On-State Output Current $\bar{a}$ to $\bar{g}$ $\bar{a}$ to $\bar{g}$	54 74			12 24	mA

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

Symbol	Parameter		Limits Min	Typ	Max	Unit	Test Conditions	
V_{IH}	Input HIGH Voltage		2.0			V	Guaranteed Input HIGH Theshold Voltage for All Inputs	
V_{IL}	Input LOW Voltage	54			0.7	V	Guaranteed Input LOW Threshold Voltage for All Inputs	
		74			0.8			
V_{IK}	Input Clamp Diode Voltage			−0.65	−1.5	V	V_{CC} = MIN, I_{IN} = −18 mA	
V_{OH}	Output HIGH Voltage, $\overline{BI}/\overline{RBO}$		2.4	4.2		V	V_{CC} = MIN, I_{OH} = −50 µA, V_{IN} = V_{IN} or V_{IL} per Truth Table	
V_{OL}	Output LOW Voltage BI/RBO	54, 74		0.25	0.4	V	I_{OL} = 1.6 mA	V_{CC} = MIN, V_{IN} = V_{IN} or V_{IL} per Truth Table
		74		0.35	0.5	V	I_{OL} = 3.2 mA	
$I_{O\ (off)}$	Off-State Output Current a thru g				250	µA	V_{CC} = MAX, V_{IN} = V_{IN} or V_{IL} per Truth Table, $V_{O\ (off)}$ = 15 V	
$V_{O\ (on)}$	On-State Output Voltage a thru g	54, 74		0.25	0.4	V	$I_{O\ (on)}$ = 12 mA	V_{CC} = MAX, V_{IN} = V_{IH} or V_{IL} per Truth Table
		74		0.35	0.5	V	$I_{O\ (on)}$ = 24 mA	
I_{IH}	Input HIGH Current				20	µA	V_{CC} = MAX, V_{IN} = 2.7 V	
					0.1	mA	V_{CC} = MAX, V_{IN} = 7.0 V	
I_{IL}	Input LOW Current $\overline{BI}/\overline{RBO}$ Any Input except BI/RBO				−1.2 −0.4	mA	V_{CC} = MAX, V_{IN} = 0.4 V	
I_{OS} BI/RBO	Output Short Circuit Current (Note 1)		−0.3		−2.0	mA	V_{CC} = MAX, V_{OUT} = 0 V	
I_{CC}	Power Supply Current			7.0	13	mA	V_{CC} = MAX	

Note 1: Not more than one output should be shorted at a time, nor for more than 1 second.

AC CHARACTERISTICS (T_A = 25°C)

Symbol	Parameter	Limits Min	Typ	Max	Unit	Test Conditions
t_{PHL} t_{PLH}	Propagation Delay, Address Input to Segment Output			100 100	ns ns	V_{CC} = 5.0 V C_L = 15 pF
t_{PHL} t_{PLH}	Propagation Delay, RBI Input To Segment Output			100 100	ns ns	

AC WAVEFORMS

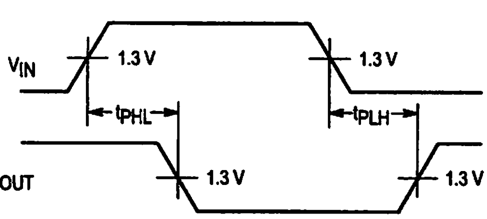


Figure 1

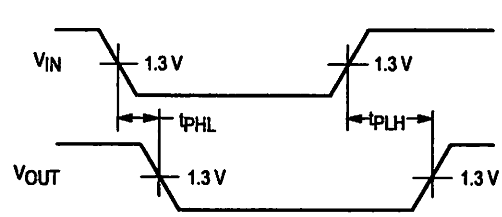


Figure 2

National Semiconductor

December 1994

ADC0801/ADC0802/ADC0803/ADC0804/ADC0805 8-Bit μP Compatible A/D Converters

General Description

The ADC0801, ADC0802, ADC0803, ADC0804 and ADC0805 are CMOS 8-bit successive approximation A/D converters that use a differential potentiometric ladder—similar to the 256R products. These converters are designed to allow operation with the NSC800 and INS8080A derivative control bus with TRI-STATE® output latches directly driving the data bus. These A/Ds appear like memory locations or I/O ports to the microprocessor and no interfacing logic is needed.

Differential analog voltage inputs allow increasing the common-mode rejection and offsetting the analog zero input voltage value. In addition, the voltage reference input can be adjusted to allow encoding any smaller analog voltage span to the full 8 bits of resolution.

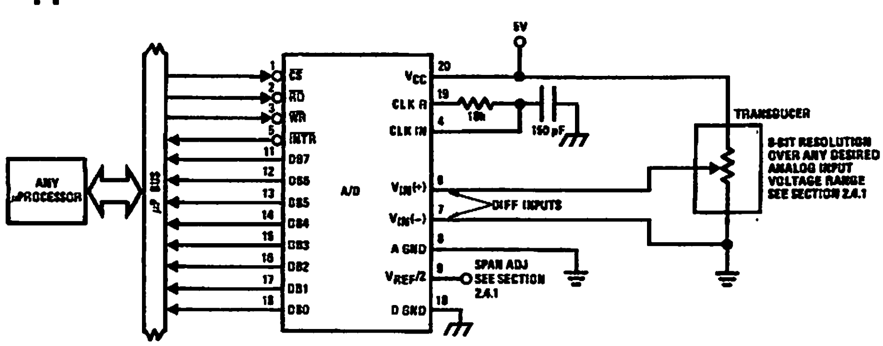
Features

- Compatible with 8080 μP derivatives—no interfacing logic needed - access time - 135 ns
- Easy interface to all microprocessors, or operates "stand alone"
- Differential analog voltage inputs
- Logic inputs and outputs meet both MOS and TTL voltage level specifications
- Works with 2.5V (LM336) voltage reference
- On-chip clock generator
- 0V to 5V analog input voltage range with single 5V supply
- No zero adjust required
- 0.3" standard width 20-pin DIP package
- 20-pin molded chip carrier or small outline package
- Operates ratiometrically or with 5 V_{DC}, 2.5 V_{DC}, or analog span adjusted voltage reference

Key Specifications

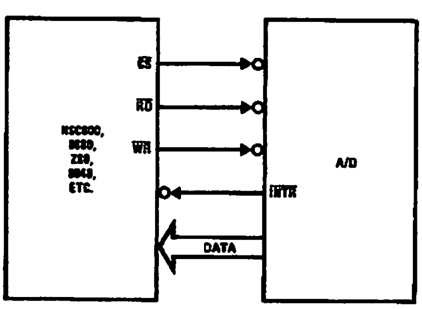
- Resolution: 8 bits
- Total error: ±¼ LSB, ±½ LSB and ±1 LSB
- Conversion time: 100 μs

Typical Applications



TL/H/5671–1

8080 Interface



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Error Specification (Includes Full-Scale, Zero Error, and Non-Linearity)			
Part Number	Full-Scale Adjusted	$V_{REF}/2 = 2.500\ V_{DC}$ (No Adjustments)	$V_{REF}/2$ = No Connection (No Adjustments)
ADC0801	±¼ LSB		
ADC0802		±½ LSB	
ADC0803	±½ LSB		
ADC0804		±1 LSB	
ADC0805			±1 LSB

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Z-80® is a registered trademark of Zilog Corp.

Absolute Maximum Ratings (Notes 1 & 2)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage (V_{CC}) (Note 3)	6.5V
Voltage	
Logic Control Inputs	−0.3V to +18V
At Other Input and Outputs	−0.3V to (V_{CC}+0.3V)
Lead Temp. (Soldering, 10 seconds)	
Dual-In-Line Package (plastic)	260°C
Dual-In-Line Package (ceramic)	300°C
Surface Mount Package	
Vapor Phase (60 seconds)	215°C
Infrared (15 seconds)	220°C
Storage Temperature Range	−65°C to +150°C
Package Dissipation at T_A=25°C	875 mW
ESD Susceptibility (Note 10)	800V

Operating Ratings (Notes 1 & 2)

Temperature Range	$T_{MIN} \le T_A \le T_{MAX}$
ADC0801/02LJ, ADC0802LJ/883	$-55°C \le T_A \le +125°C$
ADC0801/02/03/04LCJ	$-40°C \le T_A \le +85°C$
ADC0801/02/03/05LCN	$-40°C \le T_A \le +85°C$
ADC0804LCN	$0°C \le T_A \le +70°C$
ADC0802/03/04LCV	$0°C \le T_A \le +70°C$
ADC0802/03/04LCWM	$0°C \le T_A \le +70°C$
Range of V_{CC}	4.5 V_{DC} to 6.3 V_{DC}

Electrical Characteristics

The following specifications apply for V_{CC}=5 V_{DC}, $T_{MIN} \le T_A \le T_{MAX}$ and f_{CLK}=640 kHz unless otherwise specified.

Parameter	Conditions	Min	Typ	Max	Units
ADC0801: Total Adjusted Error (Note 8)	With Full-Scale Adj. (See Section 2.5.2)			±¼	LSB
ADC0802: Total Unadjusted Error (Note 8)	V_{REF}/2=2.500 V_{DC}			±½	LSB
ADC0803: Total Adjusted Error (Note 8)	With Full-Scale Adj. (See Section 2.5.2)			±½	LSB
ADC0804: Total Unadjusted Error (Note 8)	V_{REF}/2=2.500 V_{DC}			±1	LSB
ADC0805: Total Unadjusted Error (Note 8)	V_{REF}/2-No Connection			±1	LSB
V_{REF}/2 Input Resistance (Pin 9)	ADC0801/02/03/05 ADC0804 (Note 9)	2.5 0.75	8.0 1.1		kΩ kΩ
Analog Input Voltage Range	(Note 4) V(+) or V(−)	Gnd−0.05		V_{CC}+0.05	V_{DC}
DC Common-Mode Error	Over Analog Input Voltage Range		±1/16	±⅛	LSB
Power Supply Sensitivity	V_{CC}=5 V_{DC} ±10% Over Allowed $V_{IN}(+)$ and $V_{IN}(-)$ Voltage Range (Note 4)		±1/16	±⅛	LSB

AC Electrical Characteristics

The following specifications apply for V_{CC}=5 V_{DC} and T_A=25°C unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Units
T_C	Conversion Time	f_{CLK}=640 kHz (Note 6)	103		114	µs
T_C	Conversion Time	(Note 5, 6)	66		73	1/f_{CLK}
f_{CLK}	Clock Frequency Clock Duty Cycle	V_{CC}=5V, (Note 5) (Note 5)	100 40	640	1460 60	kHz %
CR	Conversion Rate in Free-Running Mode	$\overline{INTR}$ tied to $\overline{WR}$ with $\overline{CS}$=0 V_{DC}, f_{CLK}=640 kHz	8770		9708	conv/s
$t_{W(\overline{WR})L}$	Width of $\overline{WR}$ Input (Start Pulse Width)	$\overline{CS}$=0 V_{DC} (Note 7)	100			ns
t_{ACC}	Access Time (Delay from Falling Edge of $\overline{RD}$ to Output Data Valid)	C_L=100 pF		135	200	ns
t_{1H}, t_{0H}	TRI-STATE Control (Delay from Rising Edge of $\overline{RD}$ to Hi-Z State)	C_L=10 pF, R_L=10k (See TRI-STATE Test Circuits)		125	200	ns
t_{WI}, t_{RI}	Delay from Falling Edge of $\overline{WR}$ or $\overline{RD}$ to Reset of $\overline{INTR}$			300	450	ns
C_{IN}	Input Capacitance of Logic Control Inputs			5	7.5	pF
C_{OUT}	TRI-STATE Output Capacitance (Data Buffers)			5	7.5	pF
CONTROL INPUTS [Note: CLK IN (Pin 4) is the input of a Schmitt trigger circuit and is therefore specified separately]						
V_{IN} (1)	Logical "1" Input Voltage (Except Pin 4 CLK IN)	V_{CC}=5.25 V_{DC}	2.0		15	V_{DC}

AC Electrical Characteristics (Continued)

The following specifications apply for $V_{CC} = 5V_{DC}$ and $T_{MIN} \le T_A \le T_{MAX}$, unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Units
CONTROL INPUTS [Note: CLK IN (Pin 4) is the input of a Schmitt trigger circuit and is therefore specified separately]						
V_{IN} (0)	Logical "0" Input Voltage (Except Pin 4 CLK IN)	V_{CC}=4.75 V_{DC}			0.8	V_{DC}
I_{IN} (1)	Logical "1" Input Current (All Inputs)	V_{IN}=5 V_{DC}		0.005	1	μA_{DC}
I_{IN} (0)	Logical "0" Input Current (All Inputs)	V_{IN}=0 V_{DC}	−1	−0.005		μA_{DC}
CLOCK IN AND CLOCK R						
V_T+	CLK IN (Pin 4) Positive Going Threshold Voltage		2.7	3.1	3.5	V_{DC}
V_T-	CLK IN (Pin 4) Negative Going Threshold Voltage		1.5	1.8	2.1	V_{DC}
V_H	CLK IN (Pin 4) Hysteresis $(V_T+)-(V_T-)$		0.6	1.3	2.0	V_{DC}
V_{OUT} (0)	Logical "0" CLK R Output Voltage	I_O=360 μA V_{CC}=4.75 V_{DC}			0.4	V_{DC}
V_{OUT} (1)	Logical "1" CLK R Output Voltage	I_O=−360 μA V_{CC}=4.75 V_{DC}	2.4			V_{DC}
DATA OUTPUTS AND $\overline{INTR}$						
V_{OUT} (0)	Logical "0" Output Voltage Data Outputs $\overline{INTR}$ Output	 I_{OUT}=1.6 mA, V_{CC}=4.75 V_{DC} I_{OUT}=1.0 mA, V_{CC}=4.75 V_{DC}			 0.4 0.4	 V_{DC} V_{DC}
V_{OUT} (1)	Logical "1" Output Voltage	I_O=−360 μA, V_{CC}=4.75 V_{DC}	2.4			V_{DC}
V_{OUT} (1)	Logical "1" Output Voltage	I_O=−10 μA, V_{CC}=4.75 V_{DC}	4.5			V_{DC}
I_{OUT}	TRI-STATE Disabled Output Leakage (All Data Buffers)	V_{OUT}=0 V_{DC} V_{OUT}=5 V_{DC}	−3		 3	μA_{DC} μA_{DC}
I_{SOURCE}		V_{OUT} Short to Gnd, T_A=25°C	4.5	6		mA_{DC}
I_{SINK}		V_{OUT} Short to V_{CC}, T_A=25°C	9.0	16		mA_{DC}
POWER SUPPLY						
I_{CC}	Supply Current (Includes Ladder Current) ADC0801/02/03/04LCJ/05 ADC0804LCN/LCV/LCWM	f_{CLK}=640 kHz, $V_{REF}/2$=NC, T_A=25°C and $\overline{CS}$=5V		 1.1 1.9	 1.8 2.5	 mA mA

Note 1: Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. DC and AC electrical specifications do not apply when operating the device beyond its specified operating conditions.

Note 2: All voltages are measured with respect to Gnd, unless otherwise specified. The separate A Gnd point should always be wired to the D Gnd.

Note 3: A zener diode exists, internally, from V_{CC} to Gnd and has a typical breakdown voltage of 7 V_{DC}.

Note 4: For $V_{IN}(-) \ge V_{IN}(+)$ the digital output code will be 0000 0000. Two on-chip diodes are tied to each analog input (see block diagram) which will forward conduct for analog input voltages one diode drop below ground or one diode drop greater than the V_{CC} supply. Be careful, during testing at low V_{CC} levels (4.5V), as high level analog inputs (5V) can cause this input diode to conduct–especially at elevated temperatures, and cause errors for analog inputs near full-scale. The spec allows 50 mV forward bias of either diode. This means that as long as the analog V_{IN} does not exceed the supply voltage by more than 50 mV, the output code will be correct. To achieve an absolute 0 V_{DC} to 5 V_{DC} input voltage range will therefore require a minimum supply voltage of 4.950 V_{DC} over temperature variations, initial tolerance and loading.

Note 5: Accuracy is guaranteed at f_{CLK} = 640 kHz. At higher clock frequencies accuracy can degrade. For lower clock frequencies, the duty cycle limits can be extended so long as the minimum clock high time interval or minimum clock low time interval is no less than 275 ns.

Note 6: With an asynchronous start pulse, up to 8 clock periods may be required before the internal clock phases are proper to start the conversion process. The start request is internally latched, see *Figure 2* and section 2.0.

Note 7: The $\overline{CS}$ input is assumed to bracket the $\overline{WR}$ strobe input and therefore timing is dependent on the $\overline{WR}$ pulse width. An arbitrarily wide pulse width will hold the converter in a reset mode and the start of conversion is initiated by the low to high transition of the $\overline{WR}$ pulse (see timing diagrams).

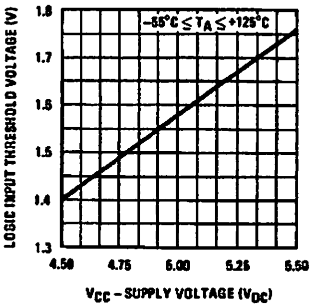
Note 8: None of these A/Ds requires a zero adjust (see section 2.5.1). To obtain zero code at other analog input voltages see section 2.5 and *Figure 5*.

Note 9: The $V_{REF}/2$ pin is the center point of a two-resistor divider connected from V_{CC} to ground. In all versions of the ADC0801, ADC0802, ADC0803, and ADC0805, and in the ADC0804LCJ, each resistor is typically 16 kΩ. In all versions of the ADC0804 except the ADC0804LCJ, each resistor is typically 2.2 kΩ.

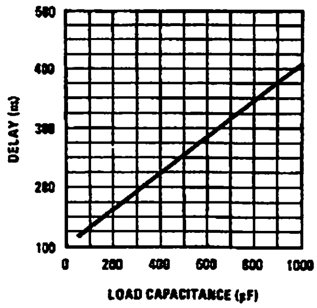
Note 10: Human body model, 100 pF discharged through a 1.5 kΩ resistor.

Typical Performance Characteristics

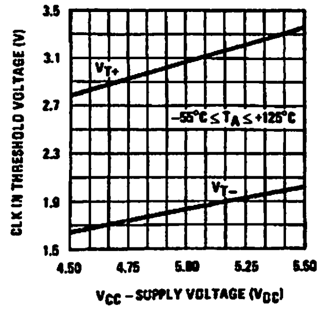
Logic Input Threshold Voltage vs. Supply Voltage



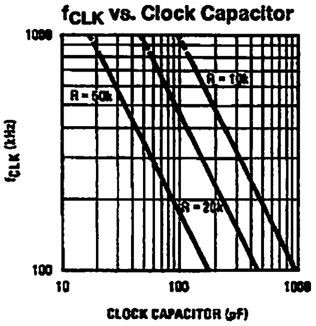
Delay From Falling Edge of $\overline{RD}$ to Output Data Valid vs. Load Capacitance



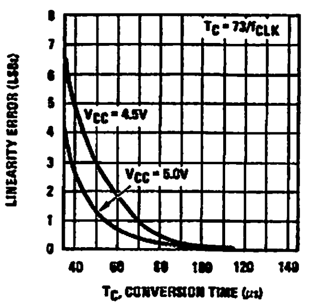
CLK IN Schmitt Trip Levels vs. Supply Voltage



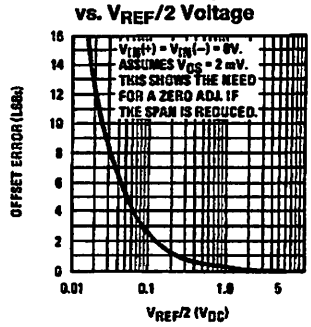
f_{CLK} vs. Clock Capacitor



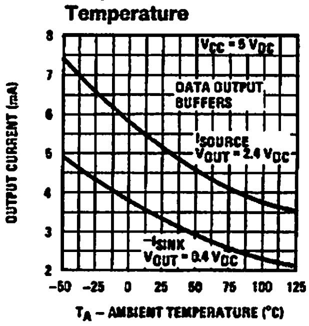
Full-Scale Error vs Conversion Time



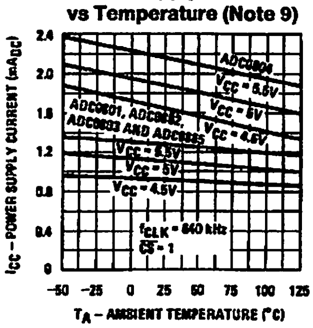
Effect of Unadjusted Offset Error vs. $V_{REF}/2$ Voltage



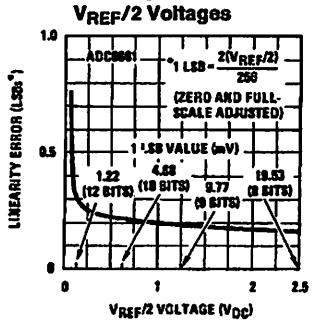
Output Current vs Temperature



Power Supply Current vs Temperature (Note 9)



Linearity Error at Low $V_{REF}/2$ Voltages



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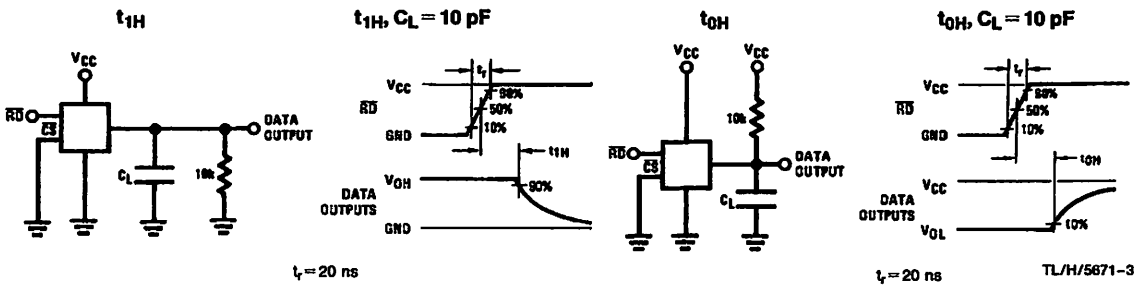
TRI-STATE Test Circuits and Waveforms



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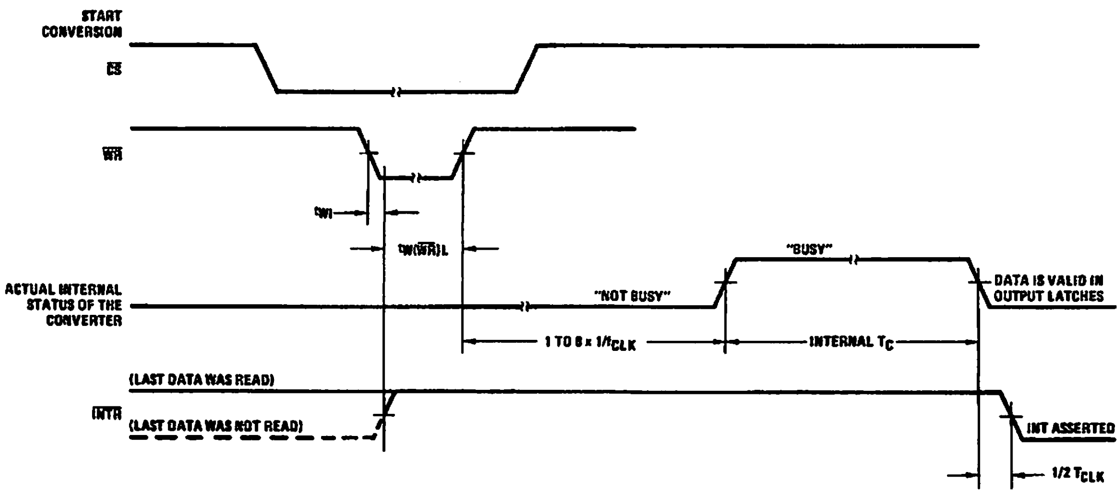
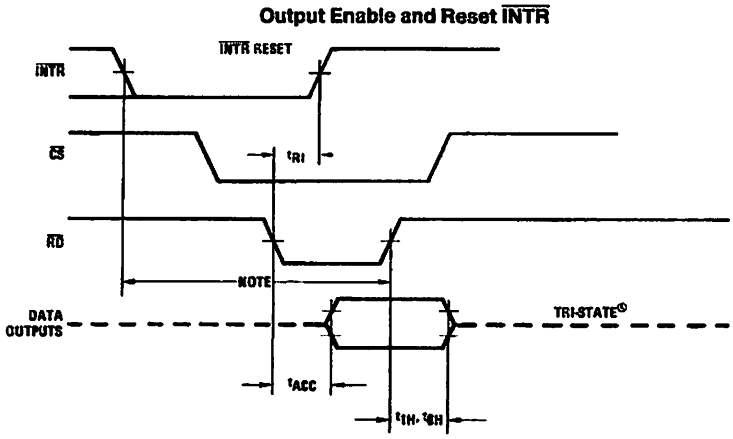
Timing Diagrams (All timing is measured from the 50% voltage points)



Output Enable and Reset $\overline{\text{INTR}}$



Note: Read strobe must occur 8 clock periods ($8/f_{CLK}$) after assertion of interrupt to guarantee reset of $\overline{\text{INTR}}$.

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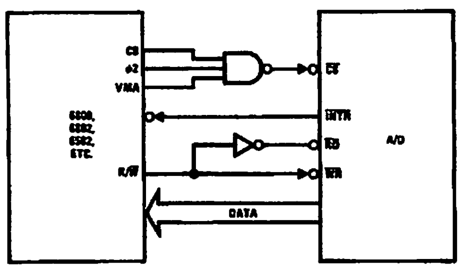
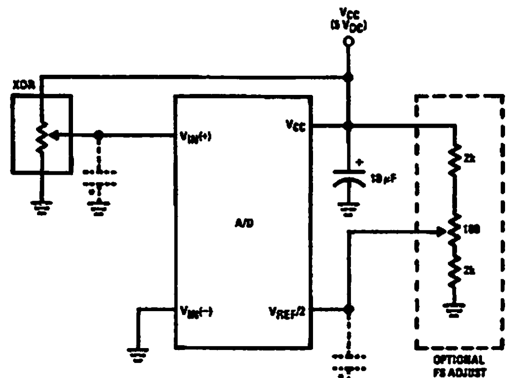
Typical Applications (Continued)

6800 Interface

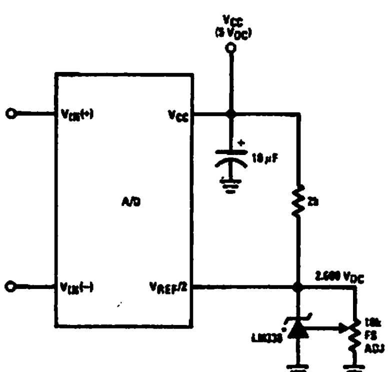


Ratiometric with Full-Scale Adjust



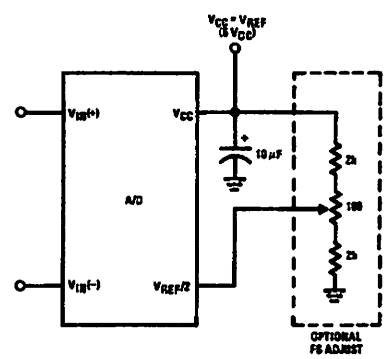
Note: before using caps at V_{IN} or $V_{REF}/2$, see section 2.3.2 Input Bypass Capacitors.

Absolute with a 2.500V Reference

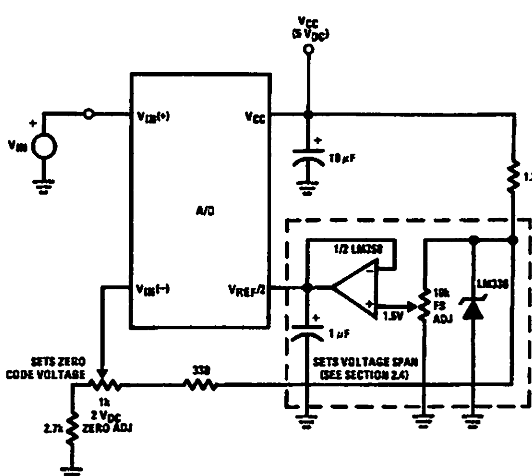


*For low power, see also LM385-2.5

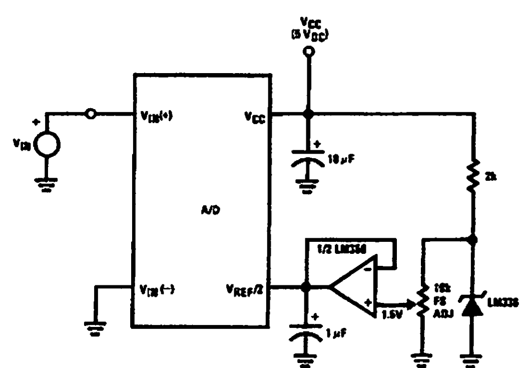
Absolute with a 5V Reference



Zero-Shift and Span Adjust: $2V \le V_{IN} \le 5V$



Span Adjust: $0V \le V_{IN} \le 3V$



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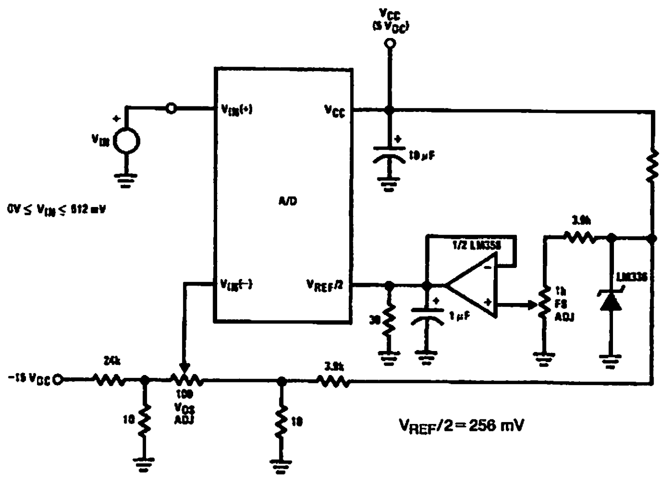
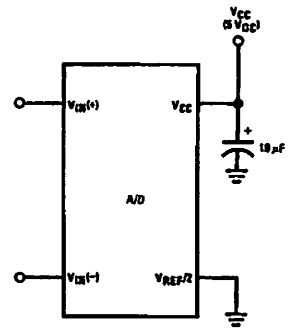
Typical Applications (Continued)

Directly Converting a Low-Level Signal



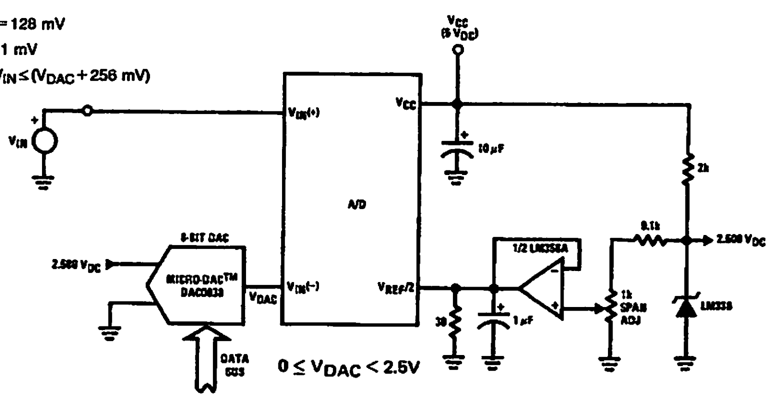
A μP Interfaced Comparator



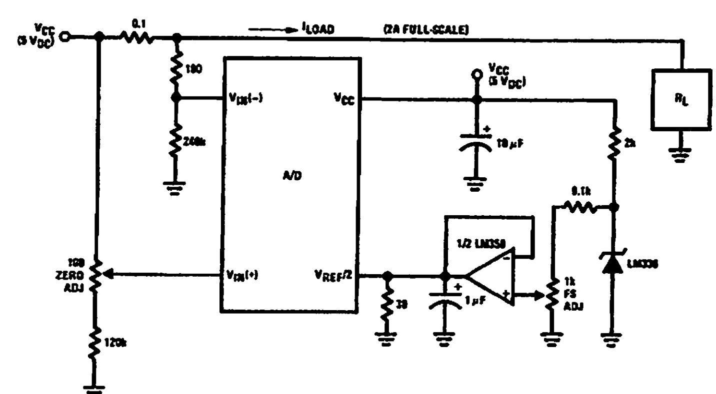
For: $V_{IN}(+) > V_{IN}(-)$
Output = FF_{HEX}
For: $V_{IN}(+) < V_{IN}(-)$
Output = 00_{HEX}

1 mV Resolution with μP Controlled Range

$V_{REF}/2 = 128$ mV
1 LSB = 1 mV
$V_{DAC} \leq V_{IN} \leq (V_{DAC} + 256$ mV)



Digitizing a Current Flow



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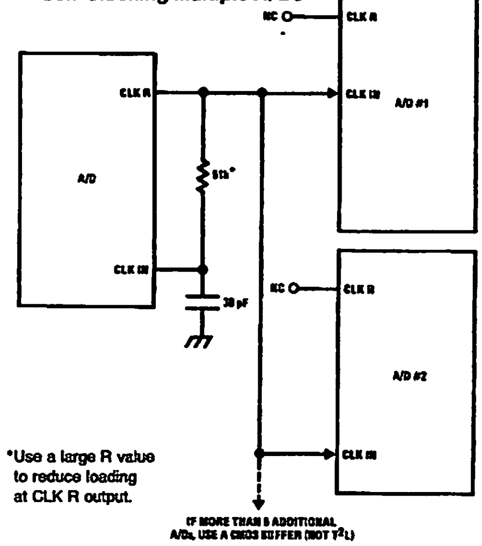
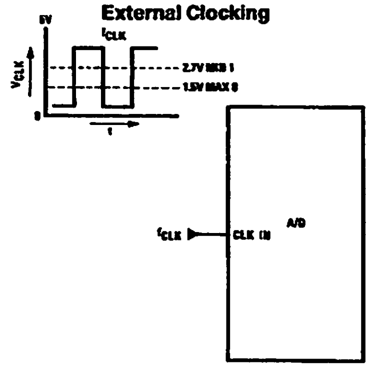
Typical Applications (Continued)

Self-Clocking Multiple A/Ds



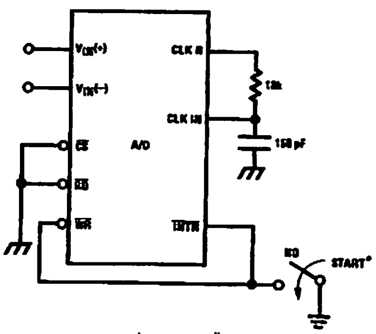
*Use a large R value to reduce loading at CLK R output.

External Clocking



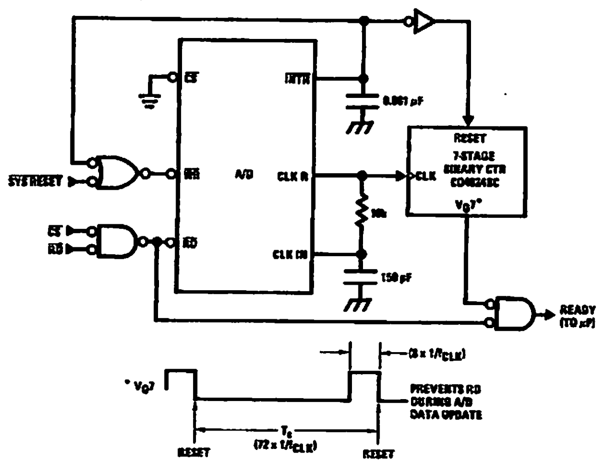
100 kHz $\leq f_{CLK} \leq$ 1460 kHz

Self-Clocking in Free-Running Mode

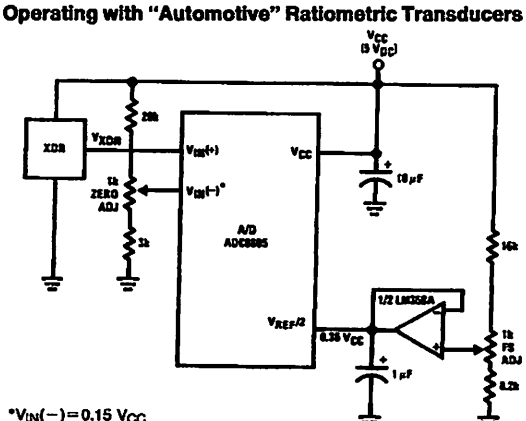


*After power-up, a momentary grounding of the $\overline{WR}$ input is needed to guarantee operation.

μP Interface for Free-Running A/D

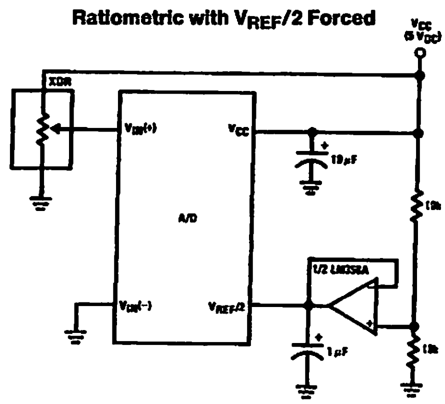


Operating with "Automotive" Ratiometric Transducers



*$V_{IN}(-) = 0.15\ V_{CC}$
15% of $V_{CC} \leq V_{XDR} \leq$ 85% of V_{CC}

Ratiometric with $V_{REF}/2$ Forced



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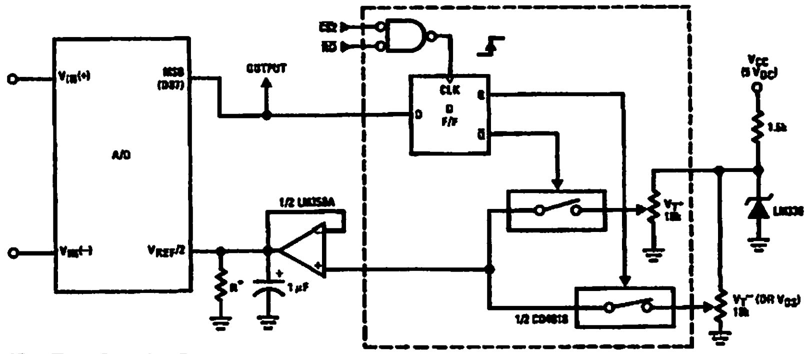
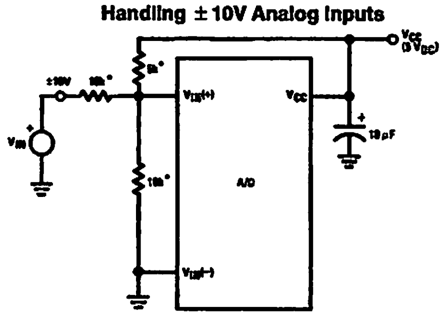
Typical Applications (Continued)

μP Compatible Differential-Input Comparator with Pre-Set V_{OS} (with or without Hysteresis)



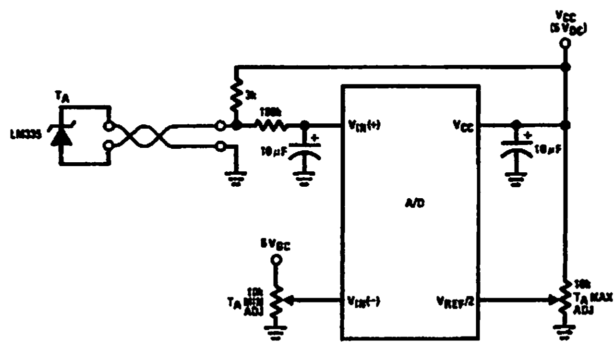
*See *Figure 5* to select R value
DB7 = "1" for $V_{IN}(+) > V_{IN}(-) + (V_{REF}/2)$
Omit circuitry within the dotted area if hysteresis is not needed

Handling ±10V Analog Inputs

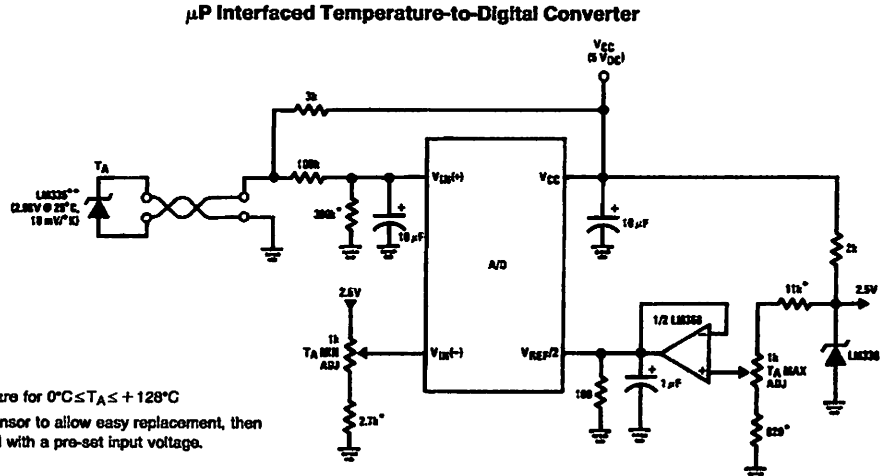


*Beckman Instruments #694-3-R10K resistor array

Low-Cost, μP Interfaced, Temperature-to-Digital Converter



μP Interfaced Temperature-to-Digital Converter



*Circuit values shown are for $0°C \leq T_A \leq +128°C$
**Can calibrate each sensor to allow easy replacement, then A/D can be calibrated with a pre-set input voltage.

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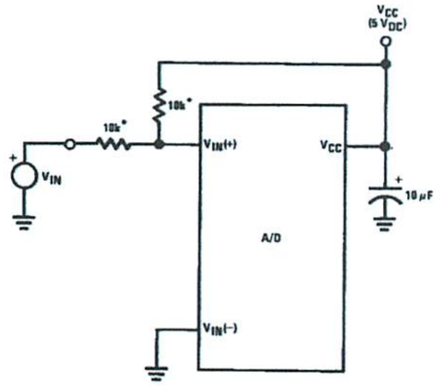
Typical Applications (Continued)

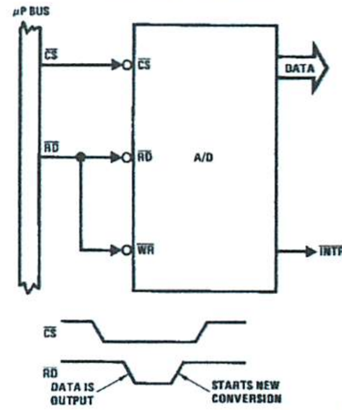
Handling ±5V Analog Inputs



TL/H/5671-33

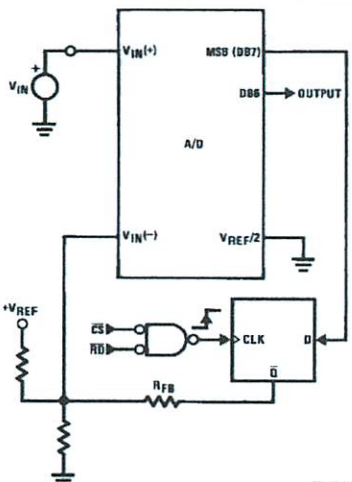
*Beckman Instruments #694-3-R10K resistor array

Read-Only Interface



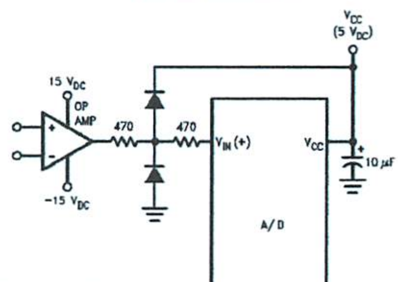
TL/H/5671-34

µP Interfaced Comparator with Hysteresis



TL/H/5671-35

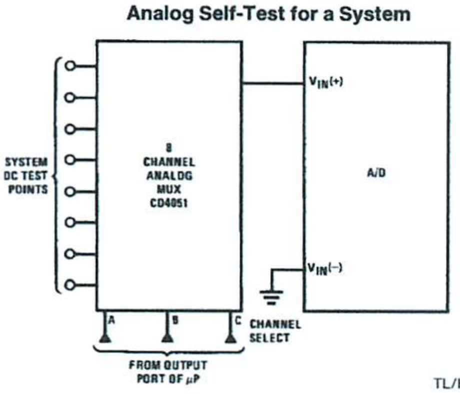
Protecting the Input



Diodes are 1N914

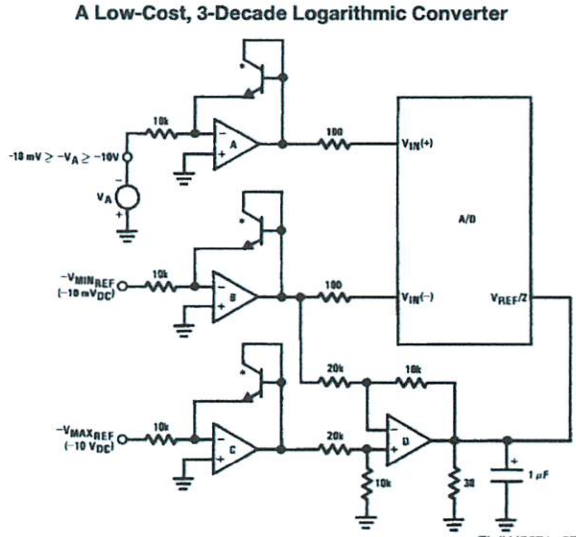
TL/H/5671-9

Analog Self-Test for a System



TL/H/5671-36

A Low-Cost, 3-Decade Logarithmic Converter



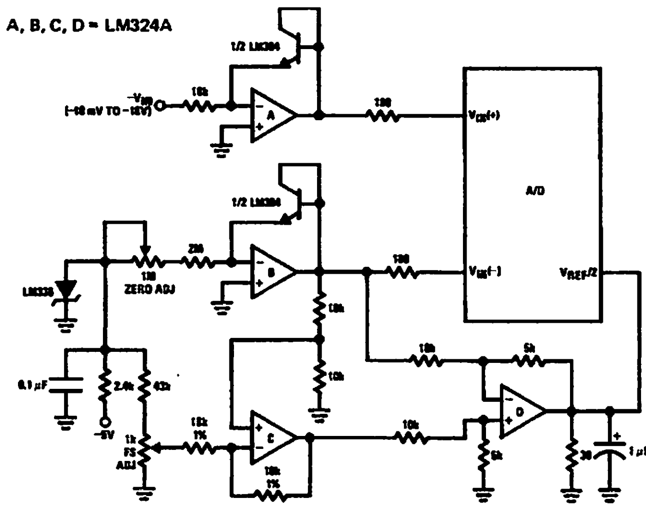
*LM389 transistors

A, B, C, D = LM324A quad op amp

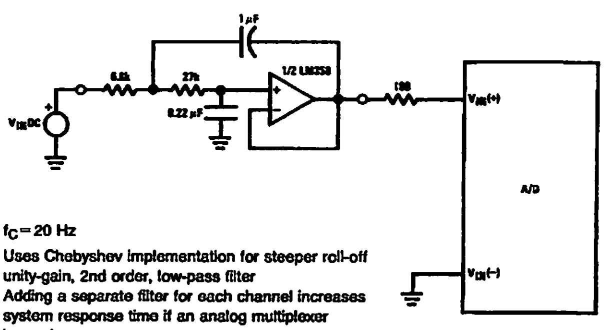
TL/H/5671-37

Typical Applications (Continued)

3-Decade Logarithmic A/D Converter

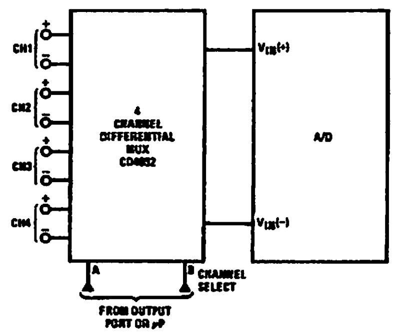


Noise Filtering the Analog Input

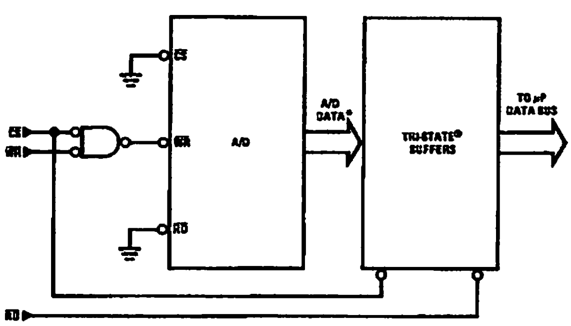


$f_C = 20$ Hz
Uses Chebyshev implementation for steeper roll-off unity-gain, 2nd order, low-pass filter
Adding a separate filter for each channel increases system response time if an analog multiplexer is used

Multiplexing Differential Inputs

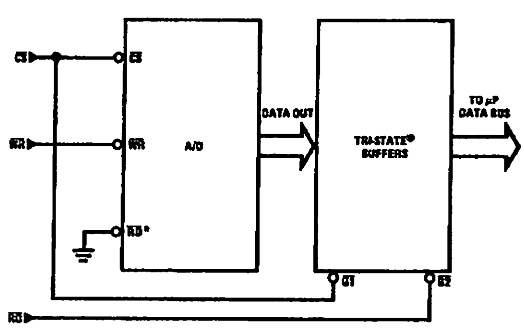


Output Buffers with A/D Data Enabled



*A/D output data is updated 1 CLK period prior to assertion of $\overline{\text{INTR}}$

Increasing Bus Drive and/or Reducing Time on Bus

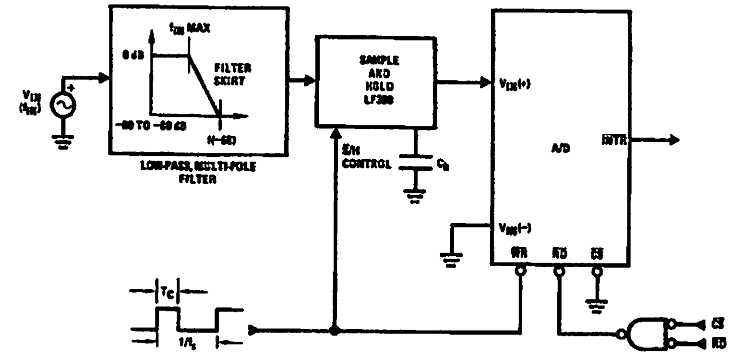


TL/H/5671–10

*Allows output data to set-up at falling edge of $\overline{\text{CS}}$

Typical Applications (Continued)

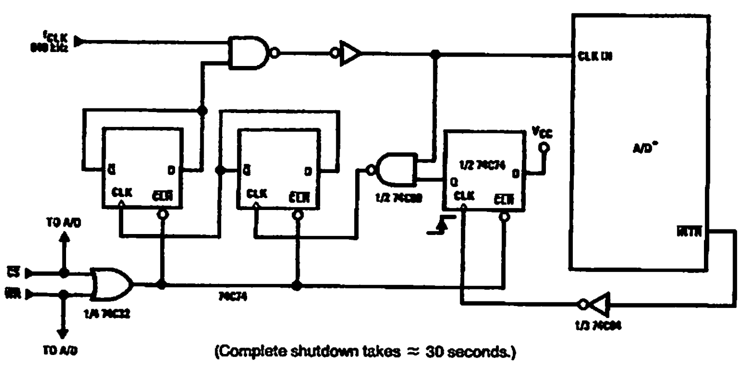
Sampling an AC Input Signal



Note 1: Oversample whenever possible [keep fs > 2f(−60)] to eliminate input frequency folding (aliasing) and to allow for the skirt response of the filter.

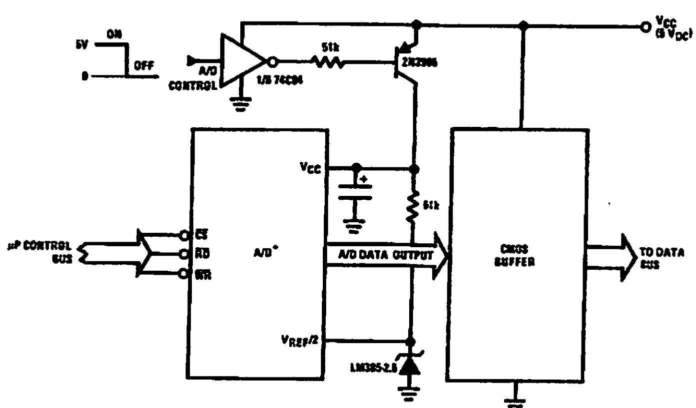
Note 2: Consider the amplitude errors which are introduced within the passband of the filter.

70% Power Savings by Clock Gating



(Complete shutdown takes ≈ 30 seconds.)

Power Savings by A/D and V_{REF} Shutdown



TL/H/5671-11

*Use ADC0801, 02, 03 or 05 for lowest power consumption.

Note: Logic inputs can be driven to V_{CC} with A/D supply at zero volts.

Buffer prevents data bus from overdriving output of A/D when in shutdown mode.

Functional Description

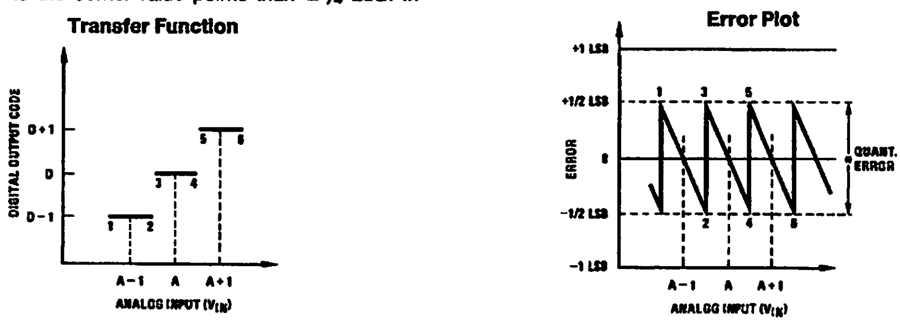
1.0 UNDERSTANDING A/D ERROR SPECS

A perfect A/D transfer characteristic (staircase waveform) is shown in *Figure 1a*. The horizontal scale is analog input voltage and the particular points labeled are in steps of 1 LSB (19.53 mV with 2.5V tied to the $V_{REF}/2$ pin). The digital output codes that correspond to these inputs are shown as D−1, D, and D+1. For the perfect A/D, not only will center-value (A−1, A, A+1, ...) analog inputs produce the correct output ditigal codes, but also each riser (the transitions between adjacent output codes) will be located ±½ LSB away from each center-value. As shown, the risers are ideal and have no width. Correct digital output codes will be provided for a range of analog input voltages that extend ±½ LSB from the ideal center-values. Each tread (the range of analog input voltage that provides the same digital output code) is therefore 1 LSB wide.

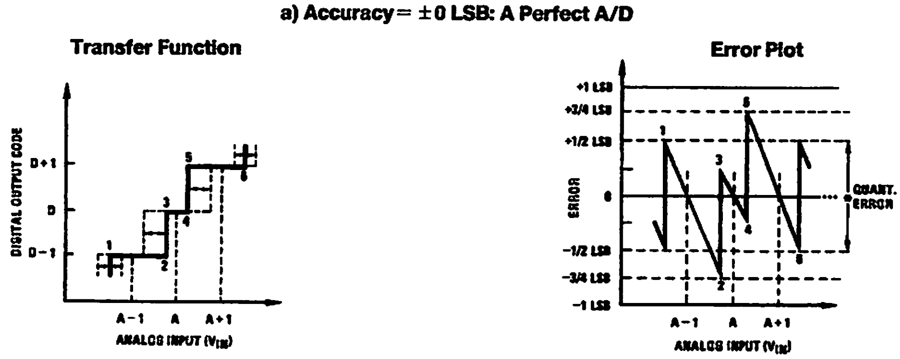
Figure 1b shows a worst case error plot for the ADC0801. All center-valued inputs are guaranteed to produce the correct output codes and the adjacent risers are guaranteed to be no closer to the center-value points than ±¼ LSB. In other words, if we apply an analog input equal to the center-value ±¼ LSB, *we guarantee* that the A/D will produce the correct digital code. The maximum range of the position of the code transition is indicated by the horizontal arrow and it is guaranteed to be no more than ½ LSB.

The error curve of *Figure 1c* shows a worst case error plot for the ADC0802. Here we guarantee that if we apply an analog input equal to the LSB analog voltage center-value the A/D will produce the correct digital code.

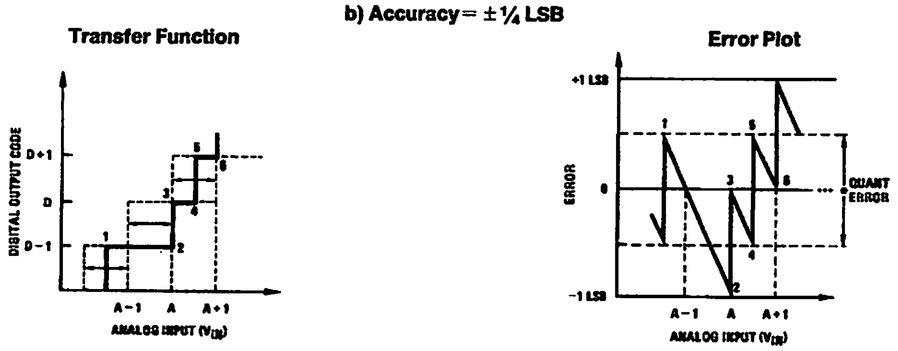
Next to each transfer function is shown the corresponding error plot. Many people may be more familiar with error plots than transfer functions. The analog input voltage to the A/D is provided by either a linear ramp or by the discrete output steps of a high resolution DAC. Notice that the error is continuously displayed and includes the quantization uncertainty of the A/D. For example the error at point 1 of *Figure 1a* is +½ LSB because the digital code appeared ½ LSB in advance of the center-value of the tread. The error plots always have a constant negative slope and the abrupt upside steps are always 1 LSB in magnitude.



a) Accuracy= ±0 LSB: A Perfect A/D



b) Accuracy= ±¼ LSB



c) Accuracy= ±½ LSB

TL/H/5671-12

FIGURE 1. Clarifying the Error Specs of an A/D Converter

Functional Description (Continued)

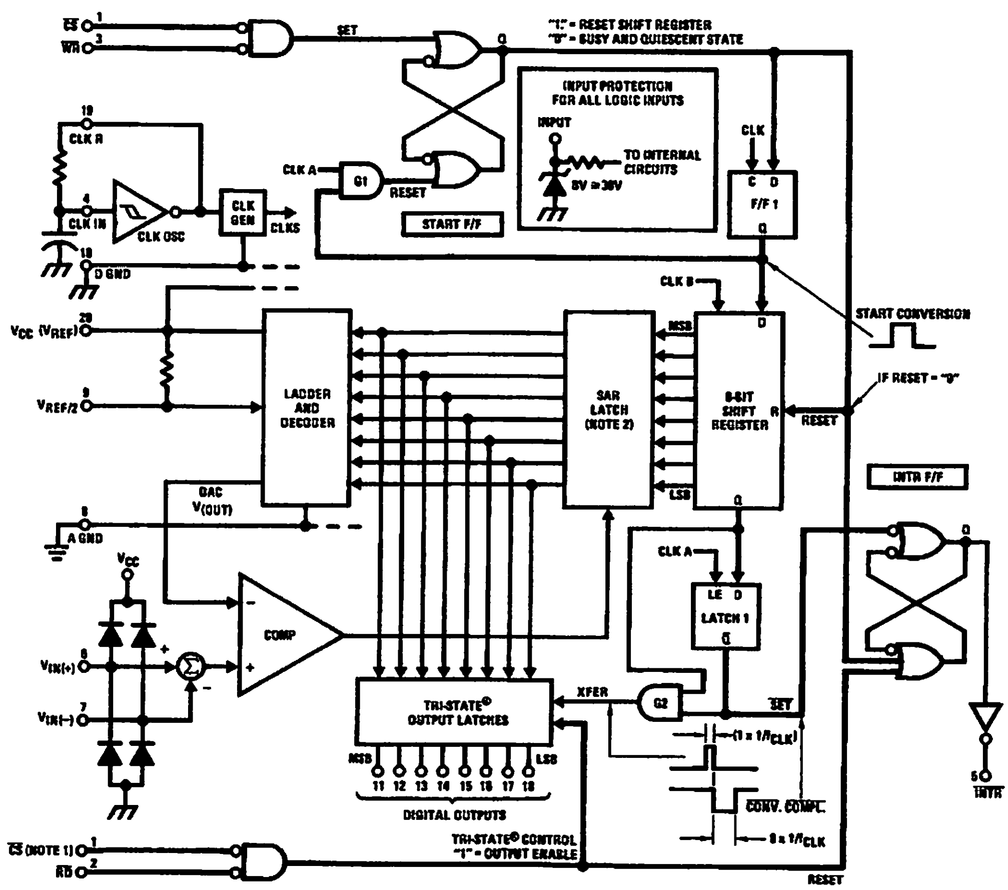
2.0 FUNCTIONAL DESCRIPTION

The ADC0801 series contains a circuit equivalent of the 256R network. Analog switches are sequenced by successive approximation logic to match the analog difference input voltage $[V_{IN}(+) - V_{IN}(-)]$ to a corresponding tap on the R network. The most significant bit is tested first and after 8 comparisons (64 clock cycles) a digital 8-bit binary code (1111 1111 = full-scale) is transferred to an output latch and then an interrupt is asserted ($\overline{INTR}$ makes a high-to-low transition). A conversion in process can be interrupted by issuing a second start command. The device may be operated in the free-running mode by connecting $\overline{INTR}$ to the $\overline{WR}$ input with $\overline{CS}=0$. To ensure start-up under all possible conditions, an external $\overline{WR}$ pulse is required during the first power-up cycle.

On the high-to-low transition of the $\overline{WR}$ input the internal SAR latches and the shift register stages are reset. As long as the $\overline{CS}$ input and $\overline{WR}$ input remain low, the A/D will remain in a reset state. *Conversion will start from 1 to 8 clock periods after at least one of these inputs makes a low-to-high transition.*

A functional diagram of the A/D converter is shown in *Figure 2*. All of the package pinouts are shown and the major logic control paths are drawn in heavier weight lines.

The converter is started by having $\overline{CS}$ and $\overline{WR}$ simultaneously low. This sets the start flip-flop (F/F) and the resulting "1" level resets the 8-bit shift register, resets the Interrupt (INTR) F/F and inputs a "1" to the D flop, F/F1, which is at the input end of the 8-bit shift register. Internal clock signals then transfer this "1" to the Q output of F/F1. The AND gate, G1, combines this "1" output with a clock signal to provide a reset signal to the start F/F. If the set signal is no longer present (either $\overline{WR}$ or $\overline{CS}$ is a "1") the start F/F is reset and the 8-bit shift register then can have the "1" clocked in, which starts the conversion process. If the set signal were to still be present, this reset pulse would have no effect (both outputs of the start F/F would momentarily be at a "1" level) and the 8-bit shift register would continue to be held in the reset mode. This logic therefore allows for wide $\overline{CS}$ and $\overline{WR}$ signals and the converter will start after at least one of these signals returns high and the internal clocks again provide a reset signal for the start F/F.



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Note 1: $\overline{CS}$ shown twice for clarity.

Note 2: SAR = Successive Approximation Register.

FIGURE 2. Block Diagram

Functional Description (Continued)

After the "1" is clocked through the 8-bit shift register (which completes the SAR search) it appears as the input to the D-type latch, LATCH 1. As soon as this "1" is output from the shift register, the AND gate, G2, causes the new digital word to transfer to the TRI-STATE output latches. When LATCH 1 is subsequently enabled, the Q output makes a high-to-low transition which causes the INTR F/F to set. An inverting buffer then supplies the $\overline{INTR}$ input signal.

Note that this $\overline{SET}$ control of the INTR F/F remains low for 8 of the external clock periods (as the internal clocks run at ⅛ of the frequency of the external clock). If the data output is continuously enabled ($\overline{CS}$ and $\overline{RD}$ both held low), the $\overline{INTR}$ output will still signal the end of conversion (by a high-to-low transition), because the $\overline{SET}$ input can control the Q output of the INTR F/F even though the RESET input is constantly at a "1" level in this operating mode. This $\overline{INTR}$ output will therefore stay low for the duration of the $\overline{SET}$ signal, which is 8 periods of the external clock frequency (assuming the A/D is not started during this interval).

When operating in the free-running or continuous conversion mode ($\overline{INTR}$ pin tied to $\overline{WR}$ and $\overline{CS}$ wired low—see also section 2.8), the START F/F is SET by the high-to-low transition of the $\overline{INTR}$ signal. This resets the SHIFT REGISTER which causes the input to the D-type latch, LATCH 1, to go low. As the latch enable input is still present, the $\overline{Q}$ output will go high, which then allows the INTR F/F to be RESET. This reduces the width of the resulting $\overline{INTR}$ output pulse to only a few propagation delays (approximately 300 ns).

When data is to be read, the combination of both $\overline{CS}$ and $\overline{RD}$ being low will cause the INTR F/F to be reset and the TRI-STATE output latches will be enabled to provide the 8-bit digital outputs.

2.1 Digital Control Inputs

The digital control inputs ($\overline{CS}$, $\overline{RD}$, and $\overline{WR}$) meet standard T^2L logic voltage levels. These signals have been renamed when compared to the standard A/D Start and Output Enable labels. In addition, these inputs are active low to allow an easy interface to microprocessor control busses. For non-microprocessor based applications, the $\overline{CS}$ input (pin 1) can be grounded and the standard A/D Start function is obtained by an active low pulse applied at the $\overline{WR}$ input (pin 3) and the Output Enable function is caused by an active low pulse at the $\overline{RD}$ input (pin 2).

2.2 Analog Differential Voltage Inputs and Common-Mode Rejection

This A/D has additional applications flexibility due to the analog differential voltage input. The $V_{IN}(-)$ input (pin 7) can be used to automatically subtract a fixed voltage value from the input reading (tare correction). This is also useful in 4 mA–20 mA current loop conversion. In addition, common-mode noise can be reduced by use of the differential input.

The time interval between sampling $V_{IN}(+)$ and $V_{IN}(-)$ is 4-½ clock periods. The maximum error voltage due to this slight time difference between the input voltage samples is given by:

$$\Delta V_e(MAX) = (V_P)(2\pi f_{cm})\left(\frac{4.5}{f_{CLK}}\right),$$

where:

ΔV_e is the error voltage due to sampling delay

V_P is the peak value of the common-mode voltage

f_{cm} is the common-mode frequency

As an example, to keep this error to ¼ LSB (~5 mV) when operating with a 60 Hz common-mode frequency, f_{cm}, and using a 640 kHz A/D clock, f_{CLK}, would allow a peak value of the common-mode voltage, V_P, which is given by:

$$V_P = \frac{[\Delta V_{e(MAX)}(f_{CLK})]}{(2\pi f_{cm})(4.5)}$$

or

$$V_P = \frac{(5\times10^{-3})(640\times10^3)}{(6.28)(60)(4.5)}$$

which gives

$V_P \cong 1.9V.$

The allowed range of analog input voltages usually places more severe restrictions on input common-mode noise levels.

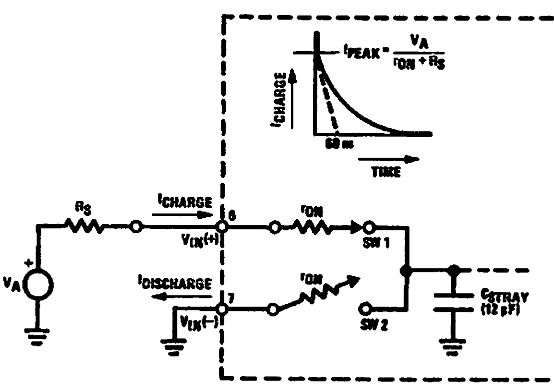
An analog input voltage with a reduced span and a relatively large zero offset can be handled easily by making use of the differential input (see section 2.4 Reference Voltage).

2.3 Analog Inputs

2.3.1 Input Current

Normal Mode

Due to the internal switching action, displacement currents will flow at the analog inputs. This is due to on-chip stray capacitance to ground as shown in *Figure 3*.



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r_{ON} of SW 1 and SW 2 ≅ 5 kΩ

$r = r_{ON}\,C_{STRAY} \cong 5\,k\Omega \times 12\,pF = 60\,ns$

FIGURE 3. Analog Input Impedance

Functional Description (Continued)

The voltage on this capacitance is switched and will result in currents entering the $V_{IN}(+)$ input pin and leaving the $V_{IN}(-)$ input which will depend on the analog differential input voltage levels. These current transients occur at the leading edge of the internal clocks. They rapidly decay and *do not cause errors* as the on-chip comparator is strobed at the end of the clock period.

Fault Mode

If the voltage source applied to the $V_{IN}(+)$ or $V_{IN}(-)$ pin exceeds the allowed operating range of $V_{CC}+50$ mV, large input currents can flow through a parasitic diode to the V_{CC} pin. If these currents can exceed the 1 mA max allowed spec, an external diode (1N914) should be added to bypass this current to the V_{CC} pin (with the current bypassed with this diode, the voltage at the $V_{IN}(+)$ pin can exceed the V_{CC} voltage by the forward voltage of this diode).

2.3.2 Input Bypass Capacitors

Bypass capacitors at the inputs will average these charges and cause a DC current to flow through the output resistances of the analog signal sources. This charge pumping action is worse for continuous conversions with the $V_{IN}(+)$ input voltage at full-scale. For continuous conversions with a 640 kHz clock frequency with the $V_{IN}(+)$ input at 5V, this DC current is at a maximum of approximately 5 μA. Therefore, *bypass capacitors should not be used at the analog inputs or the $V_{REF}/2$ pin* for high resistance sources (> 1 kΩ). If input bypass capacitors are necessary for noise filtering and high source resistance is desirable to minimize capacitor size, the detrimental effects of the voltage drop across this input resistance, which is due to the average value of the input current, can be eliminated with a full-scale adjustment while the given source resistor and input bypass capacitor are both in place. This is possible because the average value of the input current is a precise linear function of the differential input voltage.

2.3.3 Input Source Resistance

Large values of source resistance where an input bypass capacitor is not used, *will not cause errors* as the input currents settle out prior to the comparison time. If a low pass filter is required in the system, use a low valued series resistor ($\leq$ 1 kΩ) for a passive RC section or add an op amp RC active low pass filter. For low source resistance applications, ($\leq$ 1 kΩ), a 0.1 μF bypass capacitor at the inputs will prevent noise pickup due to series lead inductance of a long wire. A 100Ω series resistor can be used to isolate this capacitor—both the R and C are placed outside the feedback loop—from the output of an op amp, if used.

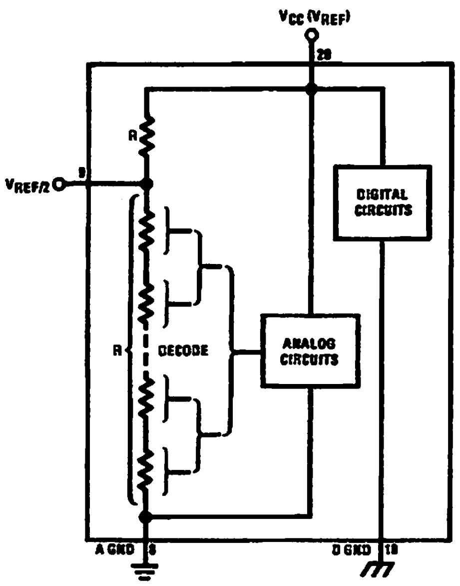
2.3.4 Noise

The leads to the analog inputs (pin 6 and 7) should be kept as short as possible to minimize input noise coupling. Both noise and undesired digital clock coupling to these inputs can cause system errors. The source resistance for these inputs should, in general, be kept below 5 kΩ. Larger values of source resistance can cause undesired system noise pickup. Input bypass capacitors, placed from the analog inputs to ground, will eliminate system noise pickup but can create analog scale errors as these capacitors will average the transient input switching currents of the A/D (see section 2.3.1.). This scale error depends on both a large source resistance and the use of an input bypass capacitor. This error can be eliminated by doing a full-scale adjustment of the A/D (adjust $V_{REF}/2$ for a proper full-scale reading—see section 2.5.2 on Full-Scale Adjustment) with the source resistance and input bypass capacitor in place.

2.4 Reference Voltage

2.4.1 Span Adjust

For maximum applications flexibility, these A/Ds have been designed to accommodate a 5 V_{DC}, 2.5 V_{DC} or an adjusted voltage reference. This has been achieved in the design of the IC as shown in *Figure 4*.

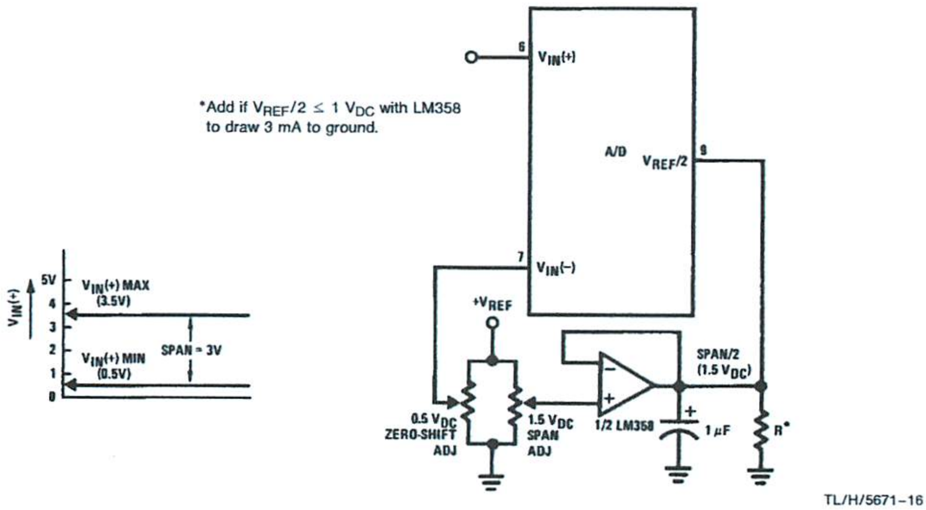


TL/H/5671–15

FIGURE 4. The $V_{REFERENCE}$ Design on the IC

Notice that the reference voltage for the IC is either ½ of the voltage applied to the V_{CC} supply pin, or is equal to the voltage that is externally forced at the $V_{REF}/2$ pin. This allows for a ratiometric voltage reference using the V_{CC} supply, a 5 V_{DC} reference voltage can be used for the V_{CC} supply or a voltage less than 2.5 V_{DC} can be applied to the $V_{REF}/2$ input for increased application flexibility. The internal gain to the $V_{REF}/2$ input is 2, making the full-scale differential input voltage twice the voltage at pin 9.

An example of the use of an adjusted reference voltage is to accommodate a reduced span—or dynamic voltage range of the analog input voltage. If the analog input voltage were to range from 0.5 V_{DC} to 3.5 V_{DC}, instead of 0V to 5 V_{DC}, the span would be 3V as shown in *Figure 5*. With 0.5 V_{DC} applied to the $V_{IN}(-)$ pin to absorb the offset, the reference voltage can be made equal to ½ of the 3V span or 1.5 V_{DC}. The A/D now will encode the $V_{IN}(+)$ signal from 0.5V to 3.5 V with the 0.5V input corresponding to zero and the 3.5 V_{DC} input corresponding to full-scale. The full 8 bits of resolution are therefore applied over this reduced analog input voltage range.



a) Analog Input Signal Example

b) Accommodating an Analog Input from 0.5V (Digital Out = = 00_{HEX}) to 3.5V (Digital Out = FF_{HEX})

FIGURE 5. Adapting the A/D Analog Input Voltages to Match an Arbitrary Input Signal Range

2.4.2 Reference Accuracy Requirements

The converter can be operated in a ratiometric mode or an absolute mode. In ratiometric converter applications, the magnitude of the reference voltage is a factor in both the output of the source transducer and the output of the A/D converter and therefore cancels out in the final digital output code. The ADC0805 is specified particularly for use in ratiometric applications with no adjustments required. In absolute conversion applications, both the initial value and the temperature stability of the reference voltage are important factors in the accuracy of the A/D converter. For $V_{REF}/2$ voltages of 2.4 V_{DC} nominal value, initial errors of ± 10 mV_{DC} will cause conversion errors of ± 1 LSB due to the gain of 2 of the $V_{REF}/2$ input. In reduced span applications, the initial value and the stability of the $V_{REF}/2$ input voltage become even more important. For example, if the span is reduced to 2.5V, the analog input LSB voltage value is correspondingly reduced from 20 mV (5V span) to 10 mV and 1 LSB at the $V_{REF}/2$ input becomes 5 mV. As can be seen, this reduces the allowed initial tolerance of the reference voltage and requires correspondingly less absolute change with temperature variations. Note that spans smaller than 2.5V place even tighter requirements on the initial accuracy and stability of the reference source.

In general, the magnitude of the reference voltage will require an initial adjustment. Errors due to an improper value of reference voltage appear as full-scale errors in the A/D transfer function. IC voltage regulators may be used for references if the ambient temperature changes are not excessive. The LM336B 2.5V IC reference diode (from National Semiconductor) has a temperature stability of 1.8 mV typ (6 mV max) over $0°C \le T_A \le +70°C$. Other temperature range parts are also available.

2.5 Errors and Reference Voltage Adjustments

2.5.1 Zero Error

The zero of the A/D does not require adjustment. If the minimum analog input voltage value, $V_{IN(MIN)}$, is not ground, a zero offset can be done. The converter can be made to output 0000 0000 digital code for this minimum input voltage by biasing the A/D $V_{IN}(-)$ input at this $V_{IN(MIN)}$ value (see Applications section). This utilizes the differential mode operation of the A/D.

The zero error of the A/D converter relates to the location of the first riser of the transfer function and can be measured by grounding the V_{IN} (−) input and applying a small magnitude positive voltage to the V_{IN} (+) input. Zero error is the difference between the actual DC input voltage that is necessary to just cause an output digital code transition from 0000 0000 to 0000 0001 and the ideal ½ LSB value (½ LSB = 9.8 mV for $V_{REF}/2 = 2.500\ V_{DC}$).

2.5.2 Full-Scale

The full-scale adjustment can be made by applying a differential input voltage that is 1½ LSB less than the desired analog full-scale voltage range and then adjusting the magnitude of the $V_{REF}/2$ input (pin 9 or the V_{CC} supply if pin 9 is not used) for a digital output code that is just changing from 1111 1110 to 1111 1111.

Functional Description (Continued)

2.5.3 Adjusting for an Arbitrary Analog Input Voltage Range

If the analog zero voltage of the A/D is shifted away from ground (for example, to accommodate an analog input signal that does not go to ground) this new zero reference should be properly adjusted first. A $V_{IN}(+)$ voltage that equals this desired zero reference plus ½ LSB (where the LSB is calculated for the desired analog span, 1 LSB = analog span/256) is applied to pin 6 and the zero reference voltage at pin 7 should then be adjusted to just obtain the 00_{HEX} to 01_{HEX} code transition.

The full-scale adjustment should then be made (with the proper $V_{IN}(-)$ voltage applied) by forcing a voltage to the $V_{IN}(+)$ input which is given by:

$$V_{IN}(+) \text{ fs adj} = V_{MAX} - 1.5 \left[\frac{(V_{MAX} - V_{MIN})}{256} \right],$$

where:

V_{MAX} = The high end of the analog input range

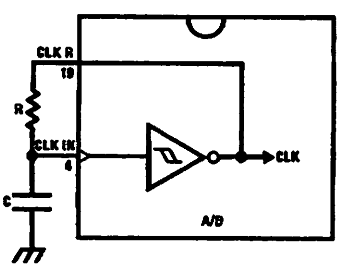
and

V_{MIN} = the low end (the offset zero) of the analog range. (Both are ground referenced.)

The $V_{REF}/2$ (or V_{CC}) voltage is then adjusted to provide a code change from FE_{HEX} to FF_{HEX}. This completes the adjustment procedure.

2.6 Clocking Option

The clock for the A/D can be derived from the CPU clock or an external RC can be added to provide self-clocking. The CLK IN (pin 4) makes use of a Schmitt trigger as shown in *Figure 6*.



$$f_{CLK} \cong \frac{1}{1.1\,RC}$$

$R \cong 10\ k\Omega$

TL/H/5671-17

FIGURE 6. Self-Clocking the A/D

Heavy capacitive or DC loading of the clock R pin should be avoided as this will disturb normal converter operation. Loads less than 50 pF, such as driving up to 7 A/D converter clock inputs from a single clock R pin of 1 converter, are allowed. For larger clock line loading, a CMOS or low power TTL buffer or PNP input logic should be used to minimize the loading on the clock R pin (do not use a standard TTL buffer).

2.7 Restart During a Conversion

If the A/D is restarted ($\overline{CS}$ and $\overline{WR}$ go low and return high) during a conversion, the converter is reset and a new conversion is started. The output data latch is not updated if the conversion in process is not allowed to be completed, therefore the data of the previous conversion remains in this latch. The $\overline{INTR}$ output simply remains at the "1" level.

2.8 Continuous Conversions

For operation in the free-running mode an initializing pulse should be used, following power-up, to ensure circuit operation. In this application, the $\overline{CS}$ input is grounded and the $\overline{WR}$ input is tied to the $\overline{INTR}$ output. This $\overline{WR}$ and $\overline{INTR}$ node should be momentarily forced to logic low following a power-up cycle to guarantee operation.

2.9 Driving the Data Bus

This MOS A/D, like MOS microprocessors and memories, will require a bus driver when the total capacitance of the data bus gets large. Other circuitry, which is tied to the data bus, will add to the total capacitive loading, even in TRI-STATE (high impedance mode). Backplane bussing also greatly adds to the stray capacitance of the data bus.

There are some alternatives available to the designer to handle this problem. Basically, the capacitive loading of the data bus slows down the response time, even though DC specifications are still met. For systems operating with a relatively slow CPU clock frequency, more time is available in which to establish proper logic levels on the bus and therefore higher capacitive loads can be driven (see typical characteristics curves).

At higher CPU clock frequencies time can be extended for I/O reads (and/or writes) by inserting wait states (8080) or using clock extending circuits (6800).

Finally, if time is short and capacitive loading is high, external bus drivers must be used. These can be TRI-STATE buffers (low power Schottky such as the DM74LS240 series is recommended) or special higher drive current products which are designed as bus drivers. High current bipolar bus drivers with PNP inputs are recommended.

2.10 Power Supplies

Noise spikes on the V_{CC} supply line can cause conversion errors as the comparator will respond to this noise. A low inductance tantalum filter capacitor should be used close to the converter V_{CC} pin and values of 1 μF or greater are recommended. If an unregulated voltage is available in the system, a separate LM340LAZ-5.0, TO-92, 5V voltage regulator for the converter (and other analog circuitry) will greatly reduce digital noise on the V_{CC} supply.

2.11 Wiring and Hook-Up Precautions

Standard digital wire wrap sockets are not satisfactory for breadboarding this A/D converter. Sockets on PC boards can be used and all logic signal wires and leads should be grouped and kept as far away as possible from the analog signal leads. Exposed leads to the analog inputs can cause undesired digital noise and hum pickup, therefore shielded leads may be necessary in many applications.

Functional Description (Continued)

A single point analog ground that is separate from the logic ground points should be used. The power supply bypass capacitor and the self-clocking capacitor (if used) should both be returned to digital ground. Any $V_{REF}/2$ bypass capacitors, analog input filter capacitors, or input signal shielding should be returned to the analog ground point. A test for proper grounding is to measure the zero error of the A/D converter. Zero errors in excess of ¼ LSB can usually be traced to improper board layout and wiring (see section 2.5.1 for measuring the zero error).

3.0 TESTING THE A/D CONVERTER

There are many degrees of complexity associated with testing an A/D converter. One of the simplest tests is to apply a known analog input voltage to the converter and use LEDs to display the resulting digital output code as shown in *Figure 7.*

For ease of testing, the $V_{REF}/2$ (pin 9) should be supplied with 2.560 V_{DC} and a V_{CC} supply voltage of 5.12 V_{DC} should be used. This provides an LSB value of 20 mV.

If a full-scale adjustment is to be made, an analog input voltage of 5.090 V_{DC} (5.120−1½ LSB) should be applied to the $V_{IN}(+)$ pin with the $V_{IN}(-)$ pin grounded. The value of the $V_{REF}/2$ input voltage should then be adjusted until the digital output code is just changing from 1111 1110 to 1111 1111. This value of $V_{REF}/2$ should then be used for all the tests.

The digital output LED display can be decoded by dividing the 8 bits into 2 hex characters, the 4 most significant (MS) and the 4 least significant (LS). Table I shows the fractional binary equivalent of these two 4-bit groups. By adding the voltages obtained from the "VMS" and "VLS" columns in Table I, the nominal value of the digital display (when

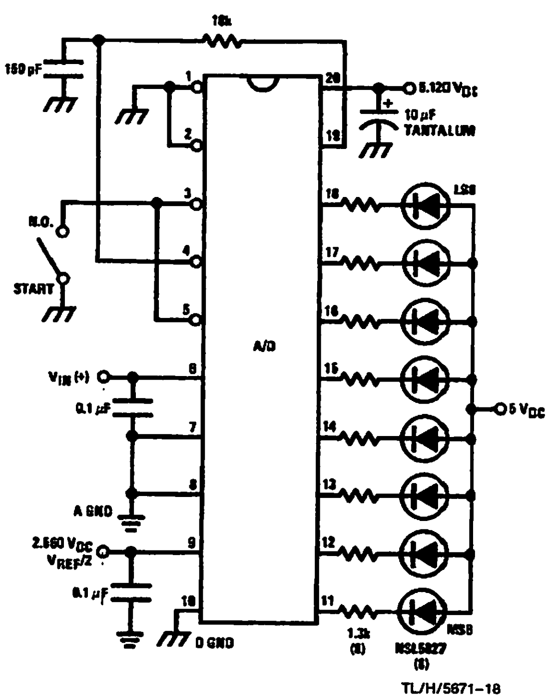


FIGURE 7. Basic A/D Tester

$V_{REF}/2$ = 2.560V) can be determined. For example, for an output LED display of 1011 0110 or B6 (in hex), the voltage values from the table are 3.520 + 0.120 or 3.640 V_{DC}. These voltage values represent the center-values of a perfect A/D converter. The effects of quantization error have to be accounted for in the interpretation of the test results.

For a higher speed test system, or to obtain plotted data, a digital-to-analog converter is needed for the test set-up. An accurate 10-bit DAC can serve as the precision voltage source for the A/D. Errors of the A/D under test can be expressed as either analog voltages or differences in 2 digital words.

A basic A/D tester that uses a DAC and provides the error as an analog output voltage is shown in *Figure 8.* The 2 op amps can be eliminated if a lab DVM with a numerical subtraction feature is available to read the difference voltage, "A−C", directly. The analog input voltage can be supplied by a low frequency ramp generator and an X-Y plotter can be used to provide analog error (Y axis) versus analog input (X axis).

For operation with a microprocessor or a computer-based test system, it is more convenient to present the errors digitally. This can be done with the circuit of *Figure 9,* where the output code transitions can be detected as the 10-bit DAC is incremented. This provides ¼ LSB steps for the 8-bit A/D under test. If the results of this test are automatically plotted with the analog input on the X axis and the error (in LSB's) as the Y axis, a useful transfer function of the A/D under test results. For acceptance testing, the plot is not necessary and the testing speed can be increased by establishing internal limits on the allowed error for each code.

4.0 MICROPROCESSOR INTERFACING

To dicuss the interface with 8080A and 6800 microprocessors, a common sample subroutine structure is used. The microprocessor starts the A/D, reads and stores the results of 16 successive conversions, then returns to the user's program. The 16 data bytes are stored in 16 successive memory locations. All Data and Addresses will be given in hexadecimal form. Software and hardware details are provided separately for each type of microprocessor.

4.1 Interfacing 8080 Microprocessor Derivatives (8048, 8085)

This converter has been designed to directly interface with derivatives of the 8080 microprocessor. The A/D can be mapped into memory space (using standard memory address decoding for $\overline{CS}$ and the $\overline{MEMR}$ and $\overline{MEMW}$ strobes) or it can be controlled as an I/O device by using the $\overline{I/O\ R}$ and $\overline{I/O\ W}$ strobes and decoding the address bits A0 → A7 (or address bits A8 → A15 as they will contain the same 8-bit address information) to obtain the $\overline{CS}$ input. Using the I/O space provides 256 additional addresses and may allow a simpler 8-bit address decoder but the data can only be input to the accumulator. To make use of the additional memory reference instructions, the A/D should be mapped into memory space. An example of an A/D in I/O space is shown in *Figure 10.*

Functional Description (Continued)

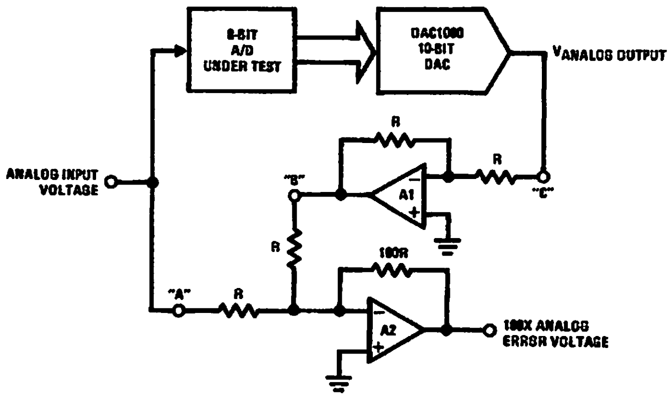


FIGURE 8. A/D Tester with Analog Error Output

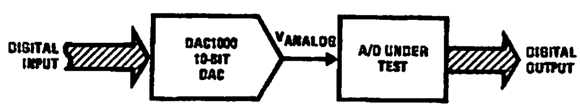


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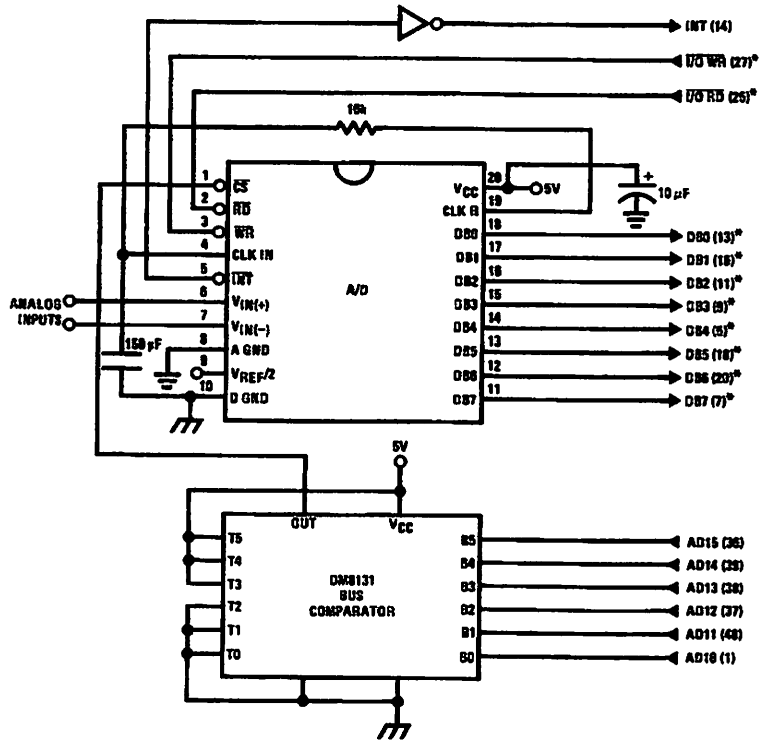
FIGURE 9. Basic "Digital" A/D Tester

TABLE I. DECODING THE DIGITAL OUTPUT LEDs

HEX	BINARY				FRACTIONAL BINARY VALUE FOR		OUTPUT VOLTAGE CENTER VALUES WITH $V_{REF}/2 = 2.560\ V_{DC}$	
					MS GROUP	LS GROUP	VMS GROUP*	VLS GROUP*
F	1	1	1	1	15/16	15/256	4.800	0.300
E	1	1	1	0	7/8	7/128	4.480	0.280
D	1	1	0	1	13/16	13/256	4.160	0.260
C	1	1	0	0	3/4	3/64	3.840	0.240
B	1	0	1	1	11/16	11/256	3.520	0.220
A	1	0	1	0	5/8	5/128	3.200	0.200
9	1	0	0	1	9/16	9/256	2/880	0.180
8	1	0	0	0	1/2	1/32	2/560	0.160
7	0	1	1	1	7/16	7/256	2.240	0.140
6	0	1	1	0	3/8	3/128	1.920	0.120
5	0	1	0	1	5/16	2/256	1.600	0.100
4	0	1	0	0	1/4	1/64	1/280	0.080
3	0	0	1	1	3/16	3/256	0.960	0.060
2	0	0	1	0	1/8	1/128	0.640	0.040
1	0	0	0	1	1/16	1/256	0.320	0.020
0	0	0	0	0			0	0

*Display Output = VMS Group + VLS Group

Functional Description (Continued)



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Note 1: *Pin numbers for the DP8228 system controller, others are INS8080A.

Note 2: Pin 23 of the INS8228 must be tied to +12V through a 1 kΩ resistor to generate the RST 7 instruction when an interrupt is acknowledged as required by the accompanying sample program.

FIGURE 10. ADC0801–INS8080A CPU Interface

SAMPLE PROGRAM FOR *FIGURE 10* ADC0801–INS8080A CPU INTERFACE

```
0038   C3 00 03   RST 7:          JMP   LD DATA
  •       •         •
  •       •         •
0100   21 00 02   START:          LXI H 0200H      ; HL pair will point to
                                                   ; data storage locations
0103   31 00 04   RETURN:         LXI SP 0400H     ; Initialize stack pointer (Note 1)
0106   7D                         MOV A, L         ; Test # of bytes entered
0107   FE 0F                      CPI 0F H         ; If # = 16. JMP to
0109   CA 13 01                   JZ CONT          ; user program
010C   D3 E0                      OUT E0 H         ; Start A/D
010E   FB                         EI               ; Enable interrupt
010F   00         LOOP:           NOP              ; Loop until end of
0110   C3 0F 01                   JMP LOOP         ; conversion
0113      •       CONT:              •
  •       •         •                •
  •       •       (User program to   •
  •       •       process data)      •
  •       •         •                •
  •       •         •                •
0300   DB E0      LD DATA:        IN E0 H          ; Load data into accumulator
0302   77                         MOV M, A         ; Store data
0303   23                         INX H            ; Increment storage pointer
0304   C3 03 01                   JMP RETURN
```

Note 1: The stack pointer must be dimensioned because a RST 7 instruction pushes the PC onto the stack.

Note 2: All address used were arbitrarily chosen.

Functional Description (Continued)

The standard control bus signals of the 8080 $\overline{CS}$, $\overline{RD}$ and $\overline{WR}$) can be directly wired to the digital control inputs of the A/D and the bus timing requirements are met to allow both starting the converter and outputting the data onto the data bus. A bus driver should be used for larger microprocessor systems where the data bus leaves the PC board and/or must drive capacitive loads larger than 100 pF.

4.1.1 Sample 8080A CPU Interfacing Circuitry and Program

The following sample program and associated hardware shown in *Figure 10* may be used to input data from the converter to the INS8080A CPU chip set (comprised of the INS8080A microprocessor, the INS8228 system controller and the INS8224 clock generator). For simplicity, the A/D is controlled as an I/O device, specifically an 8-bit bi-directional port located at an arbitrarily chosen port address, E0. The TRI-STATE output capability of the A/D eliminates the need for a peripheral interface device, however address decoding is still required to generate the appropriate $\overline{CS}$ for the converter.

It is important to note that in systems where the A/D converter is 1-of-8 or less I/O mapped devices, no address decoding circuitry is necessary. Each of the 8 address bits (A0 to A7) can be directly used as $\overline{CS}$ inputs—one for each I/O device.

4.1.2 INS8048 Interface

The INS8048 interface technique with the ADC0801 series (see *Figure 11*) is simpler than the 8080A CPU interface. There are 24 I/O lines and three test input lines in the 8048. With these extra I/O lines available, one of the I/O lines (bit 0 of port 1) is used as the chip select signal to the A/D, thus eliminating the use of an external address decoder. Bus control signals $\overline{RD}$, $\overline{WR}$ and $\overline{INT}$ of the 8048 are tied directly to the A/D. The 16 converted data words are stored at on-chip RAM locations from 20 to 2F (Hex). The $\overline{RD}$ and $\overline{WR}$ signals are generated by reading from and writing into a dummy address, respectively. A sample interface program is shown below.

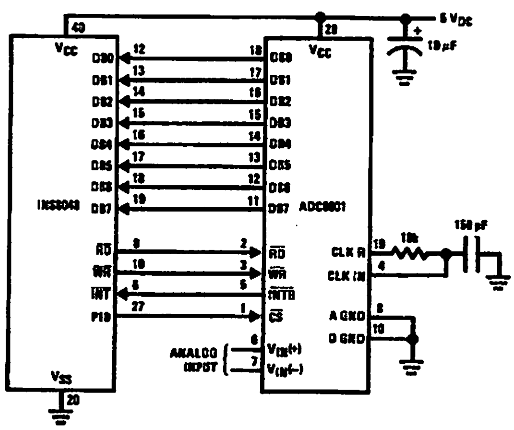

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FIGURE 11. INS8048 Interface

SAMPLE PROGRAM FOR *FIGURE 11* INS8048 INTERFACE

```
04 10                JMP     10H           : Program starts at addr 10
                     ORG     3H
04 50                JMP     50H           ; Interrupt jump vector
                     ORG     10H           ; Main program
99 FE                ANL     P1, #0FEH     ; Chip select
81                   MOVX    A, @R1        ; Read in the 1st data
                                           ; to reset the intr
89 01      START:    ORL     P1, #1        ; Set port pin high
B8 20                MOV     R0, #20H      ; Data address
B9 FF                MOV     R1, #0FFH     ; Dummy address
BA 10                MOV     R2, #10H      ; Counter for 16 bytes
23 FF      AGAIN:    MOV     A, #0FFH      ; Set ACC for intr loop
99 FE                ANL     P1, #0FEH     ; Send CS (bit 0 of P1)
91                   MOVX    @R1, A        ; Send WR out
05                   EN      I             ; Enable interrupt
96 21      LOOP:     JNZ     LOOP          ; Wait for interrupt
EA 1B                DJNZ    R2, AGAIN     ; If 16 bytes are read
00                   NOP                   ; go to user's program
00                   NOP
                     ORG     50H
81         INDATA:   MOVX    A, @R1        ; Input data, CS still low
A0                   MOV     @R0, A        ; Store in memory
18                   INC     R0            ; Increment storage counter
89 01                ORL     P1, #1        ; Reset CS signal
27                   CLR     A             ; Clear ACC to get out of
93                   RETR                  ; the interrupt loop
```

Functional Description (Continued)

4.2 Interfacing the Z-80

The Z-80 control bus is slightly different from that of the 8080. General $\overline{RD}$ and $\overline{WR}$ strobes are provided and separate memory request, $\overline{MREQ}$, and I/O request, $\overline{IORQ}$, signals are used which have to be combined with the generalized strobes to provide the equivalent 8080 signals. An advantage of operating the A/D in I/O space with the Z-80 is that the CPU will automatically insert one wait state (the $\overline{RD}$ and $\overline{WR}$ strobes are extended one clock period) to allow more time for the I/O devices to respond. Logic to map the A/D in I/O space is shown in *Figure 13*.

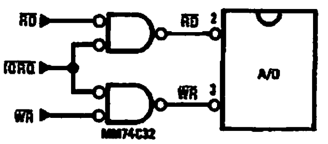

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FIGURE 13. Mapping the A/D as an I/O Device for Use with the Z-80 CPU

Additional I/O advantages exist as software DMA routines are available and use can be made of the output data transfer which exists on the upper 8 address lines (A8 to A15) during I/O input instructions. For example, MUX channel selection for the A/D can be accomplished with this operating mode.

4.3 Interfacing 6800 Microprocessor Derivatives (6502, etc.)

The control bus for the 6800 microprocessor derivatives does not use the $\overline{RD}$ and $\overline{WR}$ strobe signals. Instead it employs a single R/$\overline{W}$ line and additional timing, if needed, can be derived fom the $\phi 2$ clock. All I/O devices are memory mapped in the 6800 system, and a special signal, VMA, indicates that the current address is valid. *Figure 14* shows an interface schematic where the A/D is memory mapped in the 6800 system. For simplicity, the $\overline{CS}$ decoding is shown using ½ DM8092. Note that in many 6800 systems, an already decoded $\overline{4/5}$ line is brought out to the common bus at pin 21. This can be tied directly to the $\overline{CS}$ pin of the A/D, provided that no other devices are addressed at HX ADDR: 4XXX or 5XXX.

The following subroutine performs essentially the same function as in the case of the 8080A interface and it can be called from anywhere in the user's program.

In *Figure 15* the ADC0801 series is interfaced to the M6800 microprocessor through (the arbitrarily chosen) Port B of the MC6820 or MC6821 Peripheral Interface Adapter, (PIA). Here the $\overline{CS}$ pin of the A/D is grounded since the PIA is already memory mapped in the M6800 system and no $\overline{CS}$ decoding is necessary. Also notice that the A/D output data lines are connected to the microprocessor bus under program control through the PIA and therefore the A/D $\overline{RD}$ pin can be grounded.

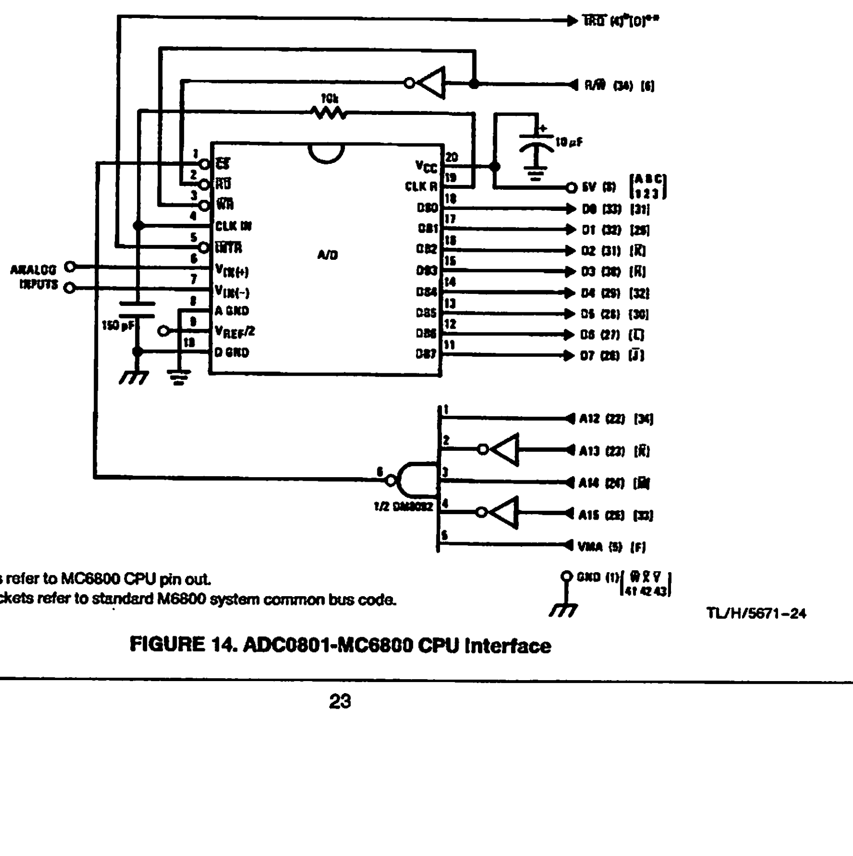
A sample interface program equivalent to the previous one is shown below *Figure 15*. The PIA Data and Control Registers of Port B are located at HEX addresses 8006 and 8007, respectively.

5.0 GENERAL APPLICATIONS

The following applications show some interesting uses for the A/D. The fact that one particular microprocessor is used is not meant to be restrictive. Each of these application circuits would have its counterpart using any microprocessor that is desired.

5.1 Multiple ADC0801 Series to MC6800 CPU Interface

To transfer analog data from several channels to a single microprocessor system, a multiple converter scheme presents several advantages over the conventional multiplexer single-converter approach. With the ADC0801 series, the differential inputs allow individual span adjustment for each channel. Furthermore, all analog input channels are sensed simultaneously, which essentially divides the microprocessor's total system servicing time by the number of channels, since all conversions occur simultaneously. This scheme is shown in *Figure 16*.



Note 1: Numbers in parentheses refer to MC6800 CPU pin out.

Note 2: Number or letters in brackets refer to standard M6800 system common bus code.

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FIGURE 14. ADC0801-MC6800 CPU Interface

SAMPLE PROGRAM FOR *FIGURE 14* ADC0801-MC6800 CPU INTERFACE

```
0010    DF 36       DATAIN   STX    TEMP2     ; Save contents of X
0012    CE 00 2C             LDX    #$002C    ; Upon IRQ low CPU
0015    FF FF F8             STX    $FFF8     ; jumps to 002C
0018    B7 50 00             STAA   $5000     ; Start ADC0801
001B    0E                   CLI
001C    3E          CONVRT   WAI              ; Wait for interrupt
001D    DE 34                LDX    TEMP1
001F    8C 02 0F             CPX    #$020F    ; Is final data stored?
0022    27 14                BEQ    ENDP
0024    B7 50 00             STAA   $5000     ; Restarts ADC0801
0027    08                   INX
0028    DF 34                STX    TEMP1
002A    20 F0                BRA    CONVRT
002C    DE 34       INTRPT   LDX    TEMP1
002E    B6 50 00             LDAA   $5000     ; Read data
0031    A7 00                STAA   X         ; Store it at X
0033    3B                   RTI
0034    02 00       TEMP1    FDB    $0200     ; Starting address for
                                              ; data storage
0036    00 00       TEMP2    FDB    $0000
0038    CE 02 00    ENDP     LDX    #$0200    ; Reinitialize TEMP1
003B    DF 34                STX    TEMP1
003D    DE 36                LDX    TEMP2
003F    39                   RTS              ; Return from subroutine
                                              ; To user's program
```

Note 1: In order for the microprocessor to service subroutines and interrupts, the stack pointer must be dimensioned in the user's program.

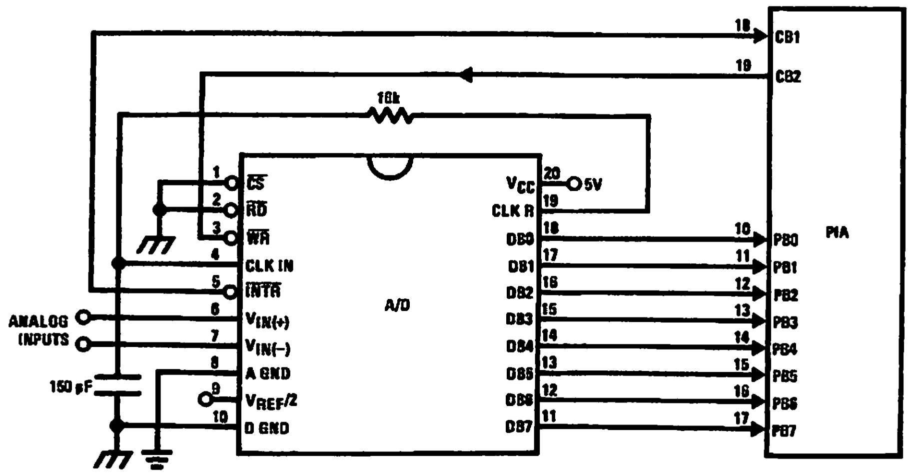

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FIGURE 15. ADC0801–MC6820 PIA Interface

Functional Description (Continued)

SAMPLE PROGRAM FOR *FIGURE 15* ADC0801–MC6820 PIA INTERFACE

```
0010   CE 00 38   DATAIN   LDX    #$0038   ; Upon IRQ low CPU
0013   FF FF F8            STX    $FFF8    ; jumps to 0038
0016   B6 80 06            LDAA   PIAORB   ; Clear possible IRQ flags
0019   4F                  CLRA
001A   B7 80 07            STAA   PIACRB
001D   B7 80 06            STAA   PIAORB   ; Set Port B as input
0020   0E                  CLI
0021   C6 34               LDAB   #$34
0023   86 3D               LDAA   #$3D
0025   F7 80 07   CONVRT   STAB   PIACRB   ; Starts ADC0801
0028   B7 80 07            STAA   PIACRB
002B   3E                  WAI             ; Wait for interrupt
002C   DE 40               LDX    TEMP1
002E   8C 02 0F            CPX    #$020F   ; Is final data stored?
0031   27 0F               BEQ    ENDP
0033   08                  INX
0034   DF 40               STX    TEMP1
0036   20 ED               BRA    CONVRT
0038   DE 40      INTRPT   LDX    TEMP1
003A   B6 80 06            LDAA   PIAORB   ; Read data in
003D   A7 00               STAA   X        ; Store it at X
003F   3B                  RTI
0040   02 00      TEMP1    FDB    $0200    ; Starting address for
                                           ; data storage
0042   CE 02 00   ENDP     LDX    #$0200   ; Reinitialize TEMP1
0045   DF 40               STX    TEMP1
0047   39                  RTS             ; Return from subroutine
                  PIAORB   EQU    $8006    ; To user's program
                  PIACRB   EQU    $8007
```

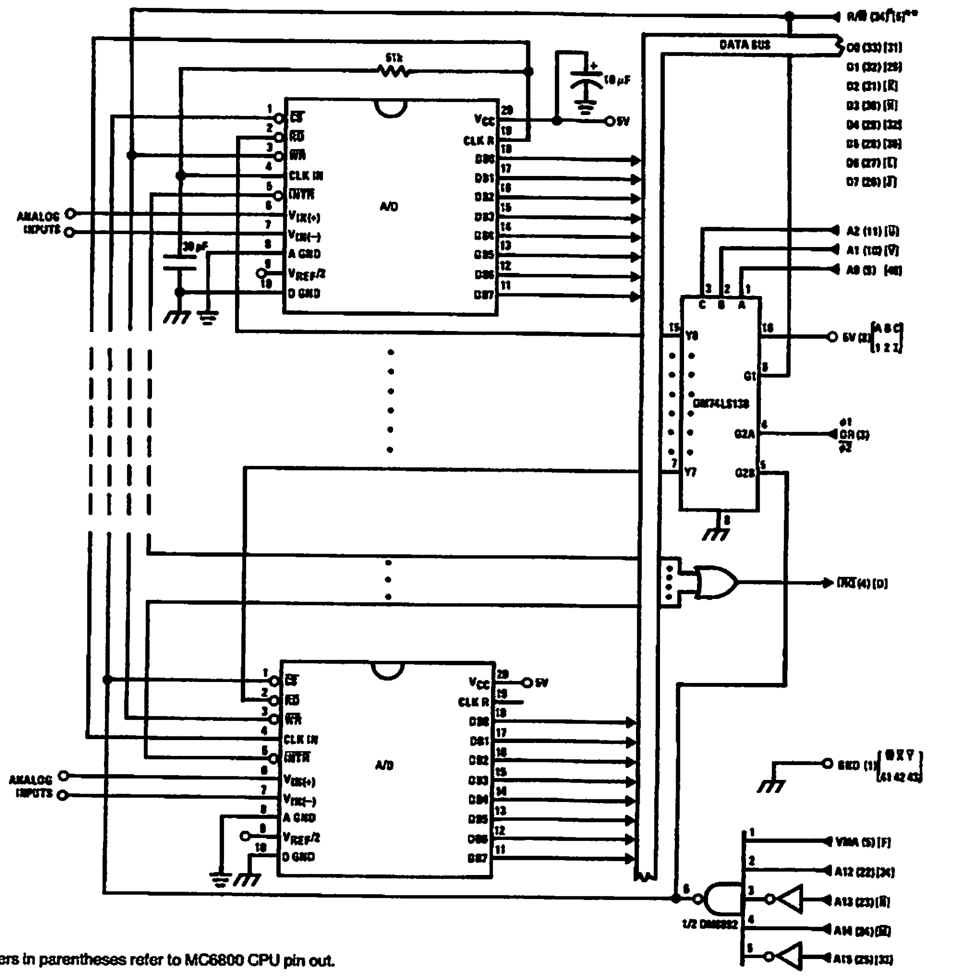
The following schematic and sample subroutine (DATA IN) may be used to interface (up to) 8 ADC0801's directly to the MC6800 CPU. This scheme can easily be extended to allow the interface of more converters. In this configuration the converters are (arbitrarily) located at HEX address 5000 in the MC6800 memory space. To save components, the clock signal is derived from just one RC pair on the first converter. This output drives the other A/Ds.

All the converters are started simultaneously with a STORE instruction at HEX address 5000. Note that any other HEX address of the form 5XXX will be decoded by the circuit, pulling all the $\overline{CS}$ inputs low. This can easily be avoided by using a more definitive address decoding scheme. All the interrupts are ORed together to insure that all A/Ds have completed their conversion before the microprocessor is interrupted.

The subroutine, DATA IN, may be called from anywhere in the user's program. Once called, this routine initializes the CPU, starts all the converters simultaneously and waits for the interrupt signal. Upon receiving the interrupt, it reads the converters (from HEX addresses 5000 through 5007) and stores the data successively at (arbitrarily chosen) HEX addresses 0200 to 0207, before returning to the user's program. All CPU registers then recover the original data they had before servicing DATA IN.

5.2 Auto-Zeroed Differential Transducer Amplifier and A/D Converter

The differential inputs of the ADC0801 series eliminate the need to perform a differential to single ended conversion for a differential transducer. Thus, one op amp can be eliminated since the differential to single ended conversion is provided by the differential input of the ADC0801 series. In general, a transducer preamp is required to take advantage of the full A/D converter input dynamic range.



Note 1: Numbers in parentheses refer to MC6800 CPU pin out.

Note 2: Numbers of letters in brackets refer to standard M6800 system common bus code.

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FIGURE 16. Interfacing Multiple A/Ds in an MC6800 System

SAMPLE PROGRAM FOR *FIGURE 16* INTERFACING MULTIPLE A/Ds IN AN MC6800 SYSTEM

ADDRESS	HEX CODE	MNEMONICS			COMMENTS
0010	DF 44	DATAIN	STX	TEMP	; Save Contents of X
0012	CE 00 2A		LDX	#$002A	; Upon $\overline{IRQ}$ LOW CPU
0015	FF FF F8		STX	$FFF8	; Jumps to 002A
0018	B7 50 00		STAA	$5000	; Starts all A/D's
001B	0E		CLI		
001C	3E		WAI		; Wait for interrupt
001D	CE 50 00		LDX	#$5000	
0020	DF 40		STX	INDEX1	; Reset both INDEX
0022	CE 02 00		LDX	#$0200	; 1 and 2 to starting
0025	DF 42		STX	INDEX2	; addresses
0027	DE 44		LDX	TEMP	
0029	39		RTS		; Return from subroutine
002A	DE 40	INTRPT	LDX	INDEX1	; INDEX1 → X
002C	A6 00		LDAA	X	; Read data in from A/D at X
002E	08		INX		; Increment X by one
002F	DF 40		STX	INDEX1	; X → INDEX1
0031	DE 42		LDX	INDEX2	; INDEX2 → X

Functional Description (Continued)

SAMPLE PROGRAM FOR *FIGURE 16* INTERFACING MULTIPLE A/Ds IN AN MC6800 SYSTEM

ADDRESS	HEX CODE		MNEMONICS		COMMENTS
0033	A7 00		STAA	X	; Store data at X
0035	8C 02 07		CPX	#$0207	; Have all A/D's been read?
0038	27 05		BEQ	RETURN	; Yes : branch to RETURN
003A	08		INX		; No : increment X by one
003B	DF 42		STX	INDEX2	; X → INDEX2
003D	20 EB		BRA	INTRPT	; Branch to 002A
003F	3B	RETURN	RTI		
0040	50 00	INDEX1	FDB	$5000	; Starting address for A/D
0042	02 00	INDEX2	FDB	$0200	; Starting address for data storage
0044	00 00	TEMP	FDB	$0000	

Note 1: In order for the microprocessor to service subroutines and interrupts, the stack pointer must be dimensioned in the user's program.

For amplification of DC input signals, a major system error is the input offset voltage of the amplifiers used for the preamp. *Figure 17* is a gain of 100 differential preamp whose offset voltage errors will be cancelled by a zeroing subroutine which is performed by the INS8080A microprocessor system. The total allowable input offset voltage error for this preamp is only 50 μV for ¼ LSB error. This would obviously require very precise amplifiers. The expression for the differential output voltage of the preamp is:

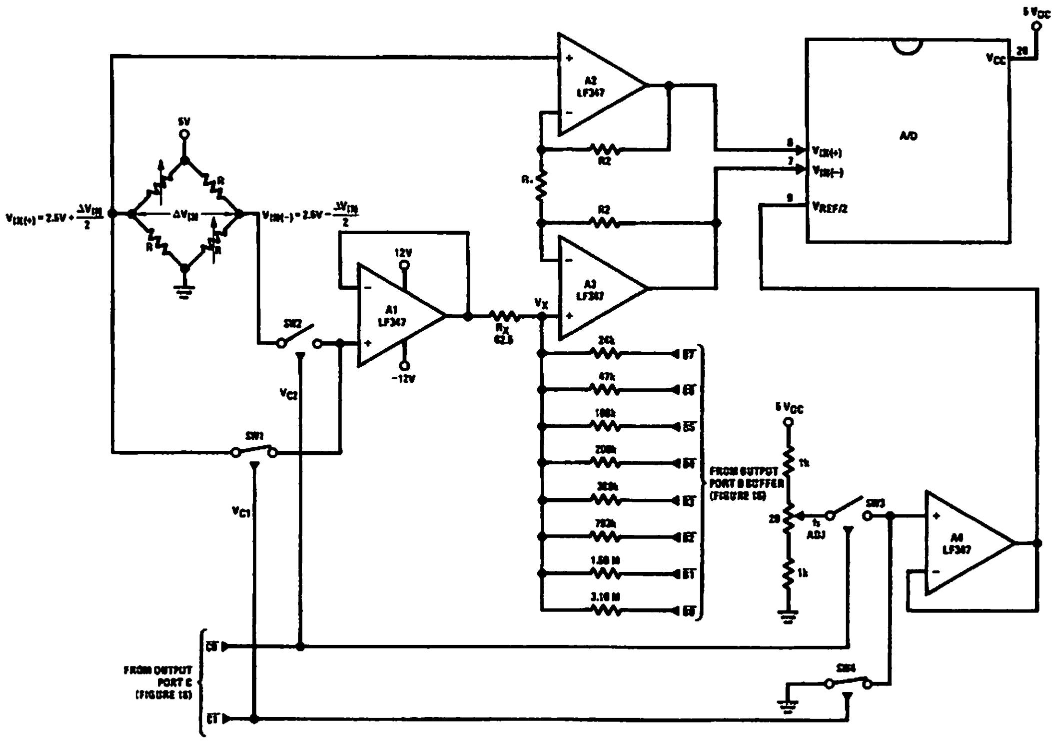
$$V_O = \underbrace{[V_{IN}(+) - V_{IN}(-)]}_{\text{SIGNAL}} \underbrace{\left[1 + \frac{2R2}{R1}\right]}_{\text{GAIN}} +$$

$$\underbrace{(V_{OS_2} - V_{OS_1} - V_{OS_3} \pm I_X R_X)}_{\text{DC ERROR TERM}} \underbrace{\left(1 + \frac{2R2}{R1}\right)}_{\text{GAIN}}$$

where I_X is the current through resistor R_X. All of the offset error terms can be cancelled by making $\pm I_X R_X = V_{OS1} + V_{OS3} - V_{OS2}$. This is the principle of this auto-zeroing scheme.

The INS8080A uses the 3 I/O ports of an INS8255 Programable Peripheral Interface (PPI) to control the auto zeroing and input data from the ADC0801 as shown in *Figure 18*. The PPI is programmed for basic I/O operation (mode 0) with Port A being an input port and Ports B and C being output ports. Two bits of Port C are used to alternately open or close the 2 switches at the input of the preamp. Switch SW1 is closed to force the preamp's differential input to be zero during the zeroing subroutine and then opened and SW2 is then closed for conversion of the actual differential input signal. Using 2 switches in this manner eliminates concern for the ON resistance of the switches as they must conduct only the input bias current of the input amplifiers.

Output Port B is used as a successive approximation register by the 8080 and the binary scaled resistors in series with each output bit create a D/A converter. During the zeroing subroutine, the voltage at V_x increases or decreases as required to make the differential output voltage equal to zero. This is accomplished by ensuring that the voltage at the output of A1 is approximately 2.5V so that a logic "1" (5V) on any output of Port B will source current into node V_X thus raising the voltage at V_X and making the output differential more negative. Conversely, a logic "0" (0V) will pull current out of node V_X and decrease the voltage, causing the differential output to become more positive. For the resistor values shown, V_X can move ±12 mV with a resolution of 50 μV, which will null the offset error term to ¼ LSB of full-scale for the ADC0801. It is important that the voltage levels that drive the auto-zero resistors be constant. Also, for symmetry, a logic swing of 0V to 5V is convenient. To achieve this, a CMOS buffer is used for the logic output signals of Port B and this CMOS package is powered with a stable 5V source. Buffer amplifier A1 is necessary so that it can source or sink the D/A output current.



Note 1: R2 = 49.5 R1

Note 2: Switches are LMC13334 CMOS analog switches.

Note 3: The 9 resistors used in the auto-zero section can be ±5% tolerance.

FIGURE 17. Gain of 100 Differential Transducer Preamp

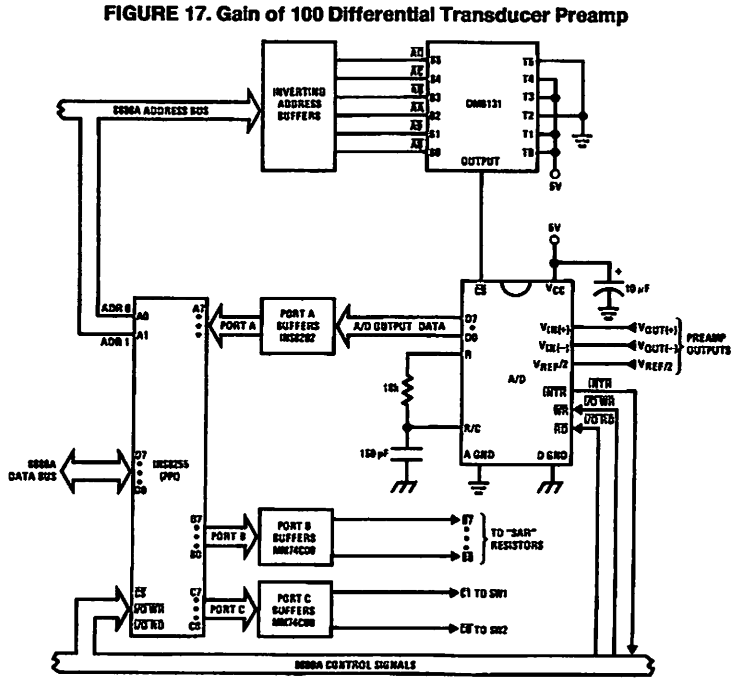


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FIGURE 18. Microprocessor Interface Circuitry for Differential Preamp

A flow chart for the zeroing subroutine is shown in *Figure 19*. It must be noted that the ADC0801 series will output an all zero code when it converts a negative input [$V_{IN}(-) \geq V_{IN}(+)$]. Also, a logic inversion exists as all of the I/O ports are buffered with inverting gates.

Basically, if the data read is zero, the differential output voltage is negative, so a bit in Port B is cleared to pull V_X more negative which will make the output more positive for the next conversion. If the data read is not zero, the output voltage is positive so a bit in Port B is set to make V_X more positive and the output more negative. This continues for 8 approximations and the differential output eventually converges to within 5 mV of zero.

The actual program is given in *Figure 20*. All addresses used are compatible with the BLC 80/10 microcomputer system. In particular:

Port A and the ADC0801 are at port address E4

Port B is at port address E5

Port C is at port address E6

PPI control word port is at port address E7

Program Counter automatically goes to ADDR:3C3D upon acknowledgement of an interrupt from the ADC0801

5.3 Multiple A/D Converters in a Z-80 Interrupt Driven Mode

In data acquisition systems where more than one A/D converter (or other peripheral device) will be interrupting program execution of a microprocessor, there is obviously a need for the CPU to determine which device requires servicing. *Figure 21* and the accompanying software is a method of determining which of 7 ADC0801 converters has completed a conversion ($\overline{INTR}$ asserted) and is requesting an interrupt. This circuit allows starting the A/D converters in any sequence, but will input and store valid data from the converters with a priority sequence of A/D 1 being read first, A/D 2 second, etc., through A/D 7 which would have the lowest priority for data being read. Only the converters whose INT is asserted will be read.

The key to decoding circuitry is the DM74LS373, 8-bit D type flip-flop. When the Z-80 acknowledges the interrupt, the program is vectored to a data input Z-80 subroutine. This subroutine will read a peripheral status word from the DM74LS373 which contains the logic state of the $\overline{INTR}$ outputs of all the converters. Each converter which initiates an interrupt will place a logic "0" in a unique bit position in the status word and the subroutine will determine the identity of the converter and execute a data read. An identifier word (which indicates which A/D the data came from) is stored in the next sequential memory location above the location of the data so the program can keep track of the identity of the data entered.

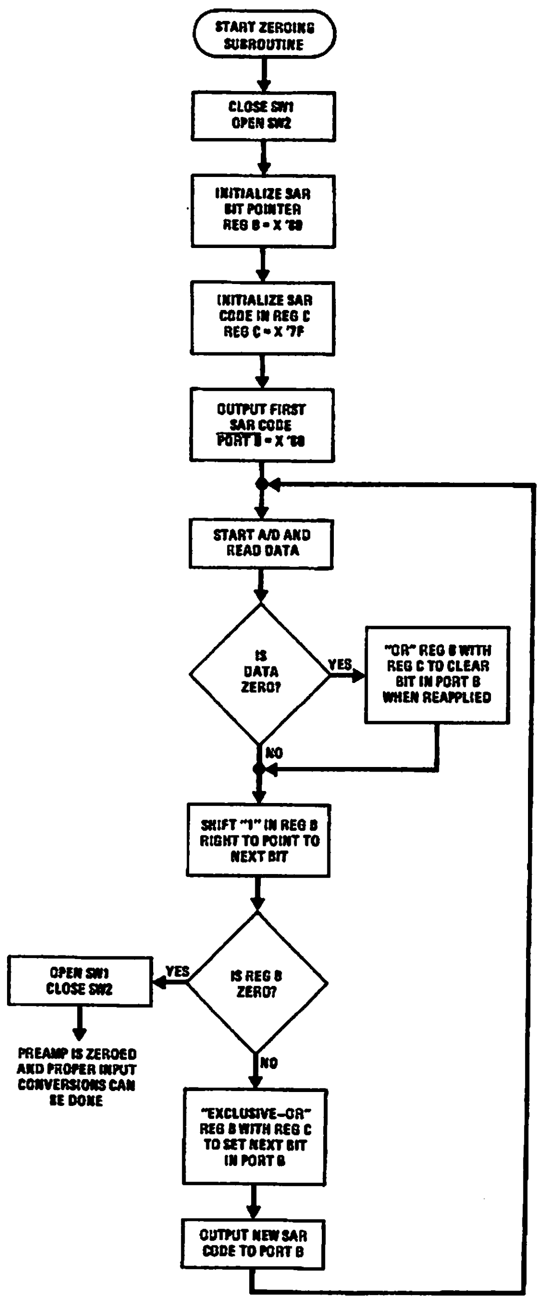

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FIGURE 19. Flow Chart for Auto-Zero Routine

```
3D00  3E90     MVI 90
3D02  D3E7     Out Control Port                                    ; Program PPI
3D04  2601     MVI H 01              Auto-Zero Subroutine
3D06  7C       MOV A,H
3D07  D3E6     OUT C                                               ; Close SW1 open SW2
3D09  0680     MVI B 80                                            ; Initialize SAR bit pointer
3D0B  3E7F     MVI A 7F                                            ; Initialize SAR code
3D0D  4F       MOV C,A               Return
3D0E  D3E5     OUT B                                               ; Port B = SAR code
3D10  31AA3D   LXI SP 3DAA           Start                         ; Dimension stack pointer
3D13  D3E4     OUT A                                               ; Start A/D
3D15  FB       IE
3D16  00       NOP                   Loop                          ; Loop until INT asserted
3D17  C3163D   JMP Loop
3D1A  7A       MOV A,D               Auto-Zero
3D1B  C600     ADI 00
3D1D  CA2D3D   JZ Set C                                            ; Test A/D output data for zero
3D20  78       MOV A,B               Shift B
3D21  F600     ORI 00                                              ; Clear carry
3D23  1F       RAR                                                 ; Shift "1" in B right one place
3D24  FE00     CPI 00                                              ; Is B zero? If yes last
3D26  CA373D   JZ Done                                             ; approximation has been made
3D29  47       MOV B,A
3D2A  C3333D   JMP New C
3D2D  79       MOV A,C               Set C
3D2E  B0       ORA B                                               ; Set bit in C that is in same
3D2F  4F       MOV C,A                                             ; position as "1" in B
3D30  C3203D   JMP Shift B
3D33  A9       XRA C                 New C                         ; Clear bit in C that is in
3D34  C30D3D   JMP Return                                          ; same position as "1" in B
3D37  47       MOV B,A               Done                          ; then output new SAR code.
3D38  7C       MOV A,H                                             ; Open SW1, close SW2 then
3D39  EE03     XRI 03                                              ; proceed with program. Preamp
3D3B  D3E6     OUT C                                               ; is now zeroed.
3D3D           •                     Normal
               •
               •
               Program for processing
               proper data values
3C3D  DBE4     IN A                  Read A/D Subroutine           ; Read A/D data
3C3F  EEFF     XRI FF                                              ; Invert data
3C41  57       MOV D,A
3C42  78       MOV A,B                                             ; Is B Reg = 0? If not stay
3C43  E6FF     ANI FF                                              ; in auto zero subroutine
3C45  C21A3D   JNZ Auto-Zero
3C48  C33D3D   JMP Normal
```

Note: All numerical values are hexadecimal representations.

FIGURE 20. Software for Auto-Zeroed Differential A/D

5.3 Multiple A/D Converters in a Z-80® Interrupt Driven Mode (Continued)

The following notes apply:

1) It is assumed that the CPU automatically performs a RST 7 instruction when a valid interrupt is acknowledged (CPU is in interrupt mode 1). Hence, the subroutine starting address of X0038.
2) The address bus from the Z-80 and the data bus to the Z-80 are assumed to be inverted by bus drivers.
3) A/D data and identifying words will be stored in sequential memory locations starting at the arbitrarily chosen address X 3E00.
4) The stack pointer must be dimensioned in the main program as the RST 7 instruction automatically pushes the PC onto the stack and the subroutine uses an additional 6 stack addresses.
5) The peripherals of concern are mapped into I/O space with the following port assignments:

HEX PORT ADDRESS	PERIPHERAL
00	MM74C374 8-bit flip-flop
01	A/D 1
02	A/D 2
03	A/D 3
04	A/D 4
05	A/D 5
06	A/D 6
07	A/D 7

This port address also serves as the A/D identifying word in the program.

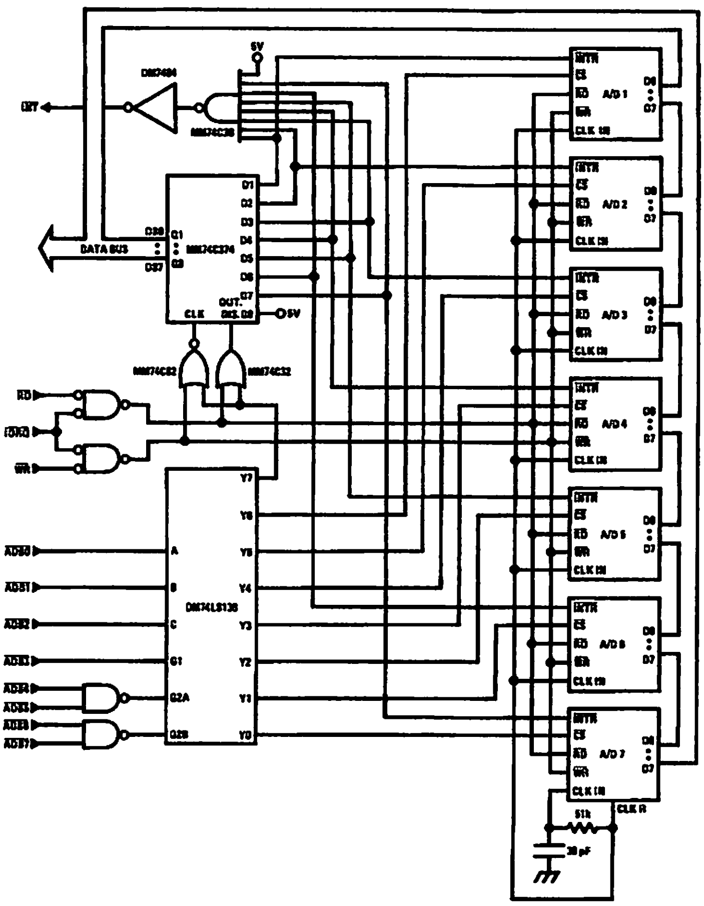

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FIGURE 21. Multiple A/Ds with Z-80 Type Microprocessor

INTERRUPT SERVICING SUBROUTINE

LOC	OBJ CODE		SOURCE STATEMENT	COMMENT
0038	E5		PUSH HL	; Save contents of all registers affected by
0039	C5		PUSH BC	; this subroutine.
003A	F5		PUSH AF	; Assumed INT mode 1 earlier set.
003B	21 00 3E		LD (HL),X3E00	; Initialize memory pointer where data will be stored.
003E	0E 01		LD C, X01	; C register will be port ADDR of A/D converters.
0040	D300		OUT X00, A	; Load peripheral status word into 8-bit latch.
0042	DB00		IN A, X00	; Load status word into accumulator.
0044	47		LD B,A	; Save the status word.
0045	79	TEST	LD A,C	; Test to see if the status of all A/D's have
0046	FE 08		CP, X08	; been checked. If so, exit subroutine
0048	CA 60 00		JPZ, DONE	
004B	78		LD A,B	; Test a single bit in status word by looking for
004C	1F		RRA	; a "1" to be rotated into the CARRY (an $\overline{\text{INT}}$
004D	47		LD B,A	; is loaded as a "1"). If CARRY is set then load
004E	DA 5500		JPC, LOAD	; contents of A/D at port ADDR in C register.
0051	0C	NEXT	INC C	; If CARRY is not set, increment C register to point
0052	C3 4500		JP,TEST	; to next A/D, then test next bit in status word.
0055	ED 78	LOAD	IN A, (C)	; Read data from interrupting A/D and invert
0057	EE FF		XOR FF	; the data.
0059	77		LD (HL),A	; Store the data
005A	2C		INC L	
005B	71		LD (HL),C	; Store A/D identifier (A/D port ADDR).
005C	2C		INC L	
005D	C3 51 00		JP,NEXT	; Test next bit in status word.
0060	F1	DONE	POP AF	; Re-establish all registers as they were
0061	C1		POP BC	; before the interrupt.
0062	E1		POP HL	
0063	C9		RET	; Return to original program

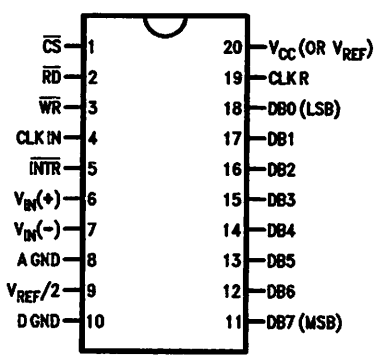
Ordering Information

TEMP RANGE		0°C TO 70°C	0°C TO 70°C	0°C TO 70°C	−40°C TO +85°C
ERROR	±¼ Bit Adjusted				ADC0801LCN
	±½ Bit Unadjusted	ADC0802LCWM	ADC0802LCV		ADC0802LCN
	±½ Bit Adjusted	ADC0803LCWM	ADC0803LCV		ADC0803LCN
	±1Bit Unadjusted	ADC0804LCWM	ADC0804LCV	ADC0804LCN	ADC0805LCN
PACKAGE OUTLINE		M20B—Small Outline	V20A—Chip Carrier	N20A—Molded DIP	

TEMP RANGE		−40°C TO +85°C	−55°C TO +125°C
ERROR	±¼ Bit Adjusted	ADC0801LCJ	ADC0801LJ
	±½ Bit Unadjusted	ADC0802LCJ	ADC0802LJ, ADC0802LJ/883
	±½ Bit Adjusted	ADC0803LCJ	
	±1Bit Unadjusted	ADC0804LCJ	
PACKAGE OUTLINE		J20A—Cavity DIP	J20A—Cavity DIP

Connection Diagrams

ADC080X
Dual-In-Line and Small Outline (SO) Packages



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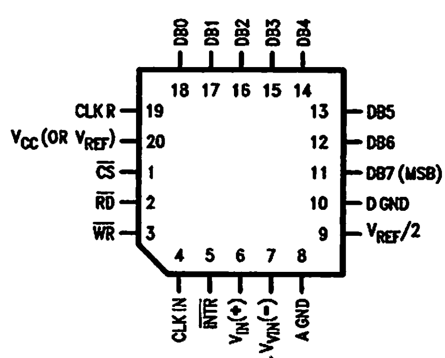
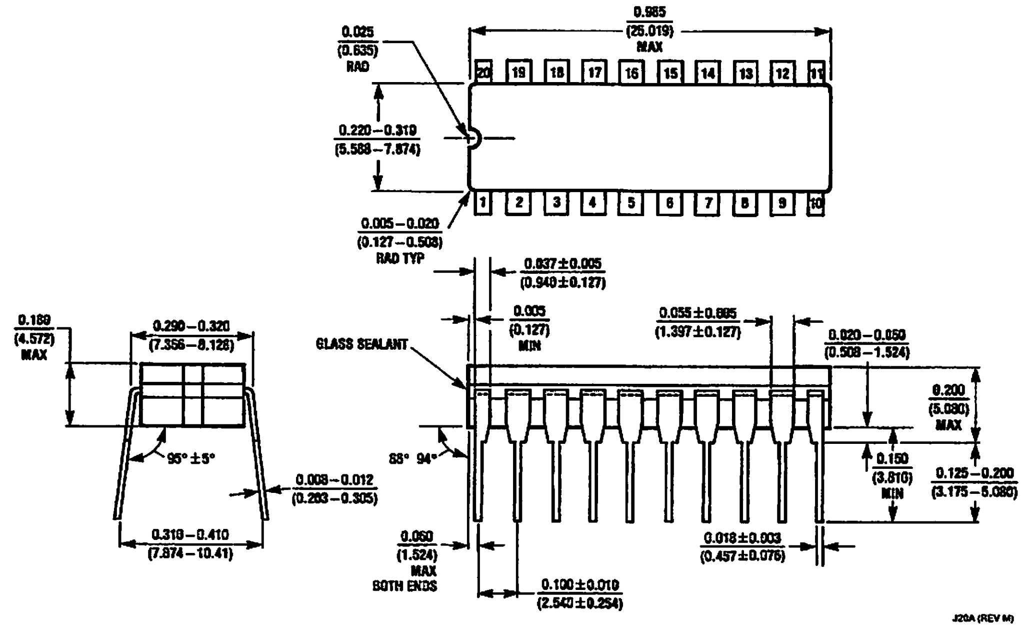
ADC080X
Molded Chip Carrier (PCC) Package



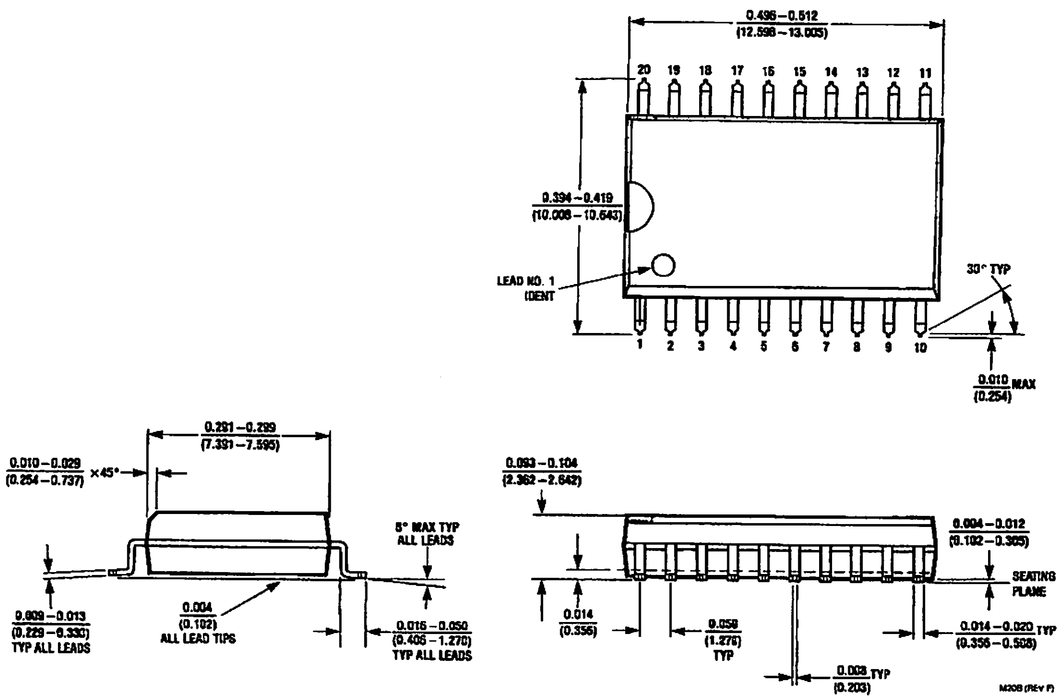
TL/H/5671-32

See Ordering Information

Physical Dimensions inches (millimeters)

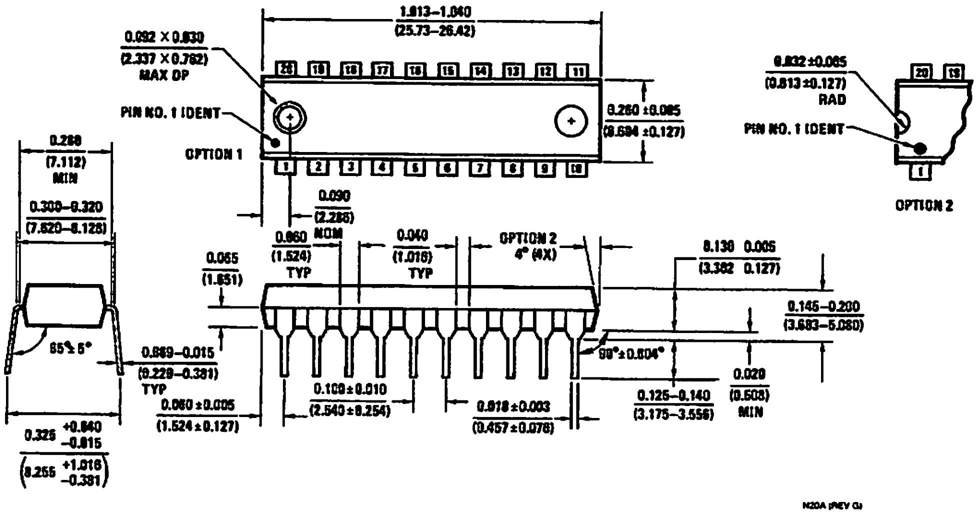


Dual-In-Line Package (J)
Order Number ADC0801LJ, ADC0802LJ, ADC0801LCJ,
ADC0802LCJ, ADC0803LCJ or ADC0804LCJ
ADC0802LJ/883 or 5962-9096601MRA
NS Package Number J20A



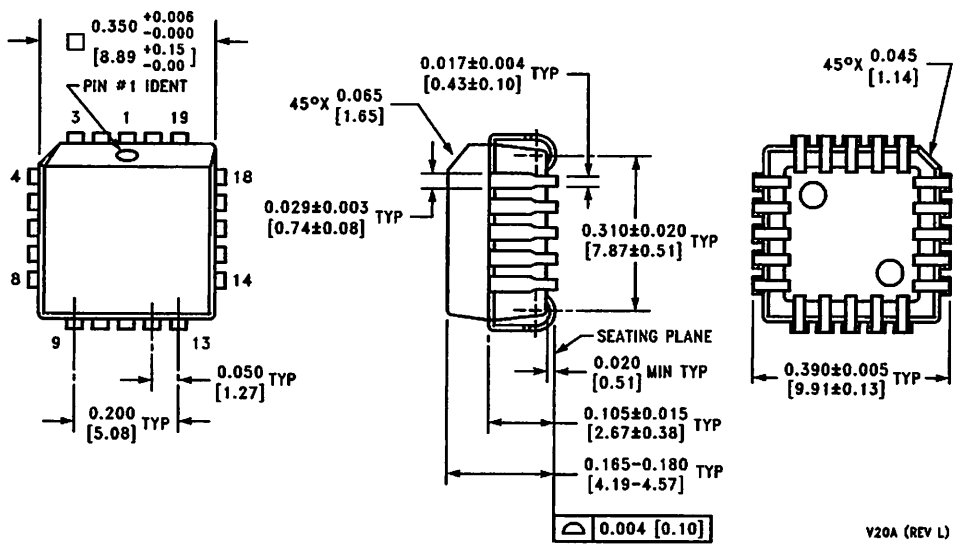
SO Package (M)
Order Number ADC0802LCWM, ADC0803LCWM or ADC0804LCWM
NS Package Number M20B

Physical Dimensions inches (millimeters) (Continued)



Molded Dual-In-Line Package (N)
Order Number ADC0801LCN, ADC0802LCN,
ADC0803LCN, ADC0804LCN or ADC0805LCN
NS Package Number N20A

Physical Dimensions inches (millimeters) (Continued)



Molded Chip Carrier Package (V)
Order Number ADC0802LCV, ADC0803LCV or ADC0804LCV
NS Package Number V20A

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SEMICONDUCTOR
SHIBA
TECHNICAL DATA

TOSHIBA PHOTOCOUPLER
TLP721F
GaAs IRED & PHOTO-TRANSISTOR

TLP721F)
OFFICE MACHINE.
SWITCHING POWER SUPPLY.

The TOSHIBA TLP721F consists of a photo-transistor optically coupled to a gallium arsenide infrared emitting diode in a four lead plastic DIP package.
All parameters are tested to the specification of TLP721.
(both condition and limits)

- Collector-Emitter Voltage : 55V (Min.)
- Current Transfer Ratio : 50% (Min.)
  Rank GB : 100% (Min.)
- UL Recognized : UL1577, File No.E67349
- BSI Approved : BS415 : 1990, BS7002 : 1989(EN60950)
  Certificate No.7364, 7365
- SEMKO Approved : SS4330784
  Certificate 9325163
- Isolation Voltage : 4000Vrms (Min.)
- Option (D4) type
  VDE Approved : DIN VDE0884 / 06.92,
  Certificate No. 74285

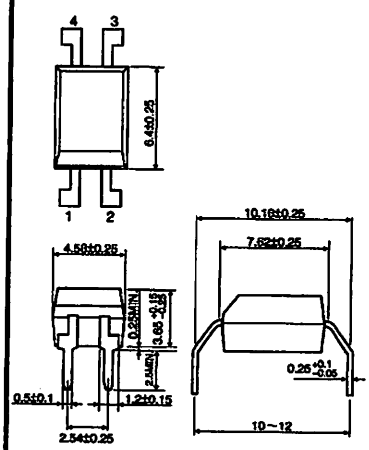
  Maximum Operating Insulation Voltage : 890VPK
  Highest Permissible Over Voltage : 6000VPK

(Note)	When a VDE0884 approved type is needed, please designate the "Option (D4)"

Creepage Distance : 8.0mm (Min.)
Clearance : 8.0mm (Min.)
Internal Creepage Path : 4.0mm (Min.)
Insulation Thickness : 0.5mm (Min.)

Conforming Safety Standards :
DIN 57 804.VDE0804 / 1.83
DIN IEC65 / VDE0860 / 8.81
DIN IEC380 / VDE0806 / 8.81
DIN IEC435 / VDE0805 / Draft Nov.84
DIN IEC601T1 / VDE0750T1 / 5.82
BS7002 : 1989 (EN60950)

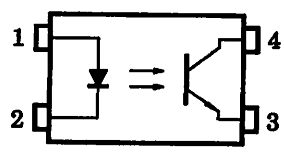
Unit in mm



JEDEC	—
EIAJ	—
TOSHIBA	11-5B202

Weight : 0.28g

PIN CONFIGURATION (TOP VIEW)



1. ANODE
2. CATHODE
3. EMITTER
4. COLLECTOR

TOSHIBA Photocoupler

TLP721(D4)SERIES

Attachment: Specifications for VDE0884 option: (D4)
Types: TLP721, TLP721F

Type designations for ' option: (D4) ', which are tested under VDE0884 requirements.
Ex.: TLP721 (D4–GR–LF4) D4: VDE0884 option
GR: CTR rank
LF4: lead bend

Note: Use TOSHIBA standard type number for safety standard application.
Ex. TLP721 (D4–GR–LF4) → TLP721

VDE0884 Isolation Characteristics

Description		Symbol	Rating	Unit
Application classification (DIN VDE0110 teil 1 / 01.89, table 1) for rated mains voltage ≤ 300 V_{rms} for rated mains voltage ≤ 600 V_{rms}			I–IV I–III	—
Climatic classification (DIN IEC68 teil 1 / 09.80)			40 / 100 / 21	—
Pollution degree (DIN VDE0110 teil 1 / 01.89)			2	—
Maximum operating insulation voltage	TLP721	V_{IORM}	630	Vpk
	TLP721F		890	
Input to output test voltage, method A $Vpr = 1.5 \times V_{IORM}$, type and sample test $t_p = 60s$, partial discharge < 5pC	TLP721	Vpr	945	Vpk
	TLP721F		1335	
Input to output test voltage, method B $Vpr = 1.875 \times V_{IORM}$, 100% production test $t_p = 1s$, partial discharge < 5pC	TLP721	Vpr	1180	Vpk
	TLP721F		1670	
Highest permissible overvoltage (transient overvoltage, $t_{pr} = 10s$)		V_{TR}	6000	Vpk
Safety limiting values (max. permissible ratings in case of fault, also refer to thermal derating curve) current (input current I_F, $P_{si} = 0$) power (output or total power dissipation) temperature		I_{si} P_{si} T_{si}	300 500 150	mA mW °C
Insulation resistance, $V_{IO} = 500V$, $Ta = 25°C$ $V_{IO} = 500V$, $Ta = T_{si}$		R_{si}	$\geq 10^{12}$ $\geq 10^{9}$	Ω

- This data sheet refers to TLP721 (D4, M), TLP721F (D4, M) that previously has a white–resin mold and have been changed. When designing new products please use black mold–resin devices.

Insulation Related Specifications

			7.62 mm pitch TLP721	10.16 mm pitch TLP721F
Minimum creepage distance	(*)	Cr	7.0 mm	8.0 mm
Minimum clearance	(*)	Cl	7.0 mm	8.0 mm
Minimum insulation thickness		ti	0.5 mm	
Comperative tracking index (DIN IEC112 / VDE0303, part 1)		CTI	175 (VDE0110 teil 1 / 01.89 group III a)	

((*) in accordance with DIN VDE0110 teil 1 / 01.89, table 2, & 4)

(*1) If a printed circuit is incorporated, the creepage distance and clearance may be reduced below this value (e. g. at a standard distance between soldering eye centres of 7.5 mm). If this is not permissible, the user shall take suitable measures.

(*2) This photocoupler is suitable for 'safe electrical isolation' only within the safety limit data. Maintenance of the safety data shall be ensured by means of protective circuits.

VDE Test sign: Marking on product for VDE0884 4

Marking on packing for VDE0884 VDE 0884

Marking example:

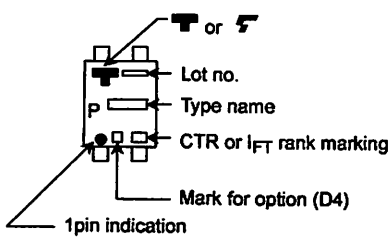


Figure 1 Partial discharge measurement procedure according to VDE0884 destructive test for qualification and sampling tests.

Method A

(for type and sampling tests,destructive tests)

t1,t2	=1 to 10s
t3,t4	=1s
tP(measuring time for partial discharge)	=50s
tb	=62s
tini	=10s

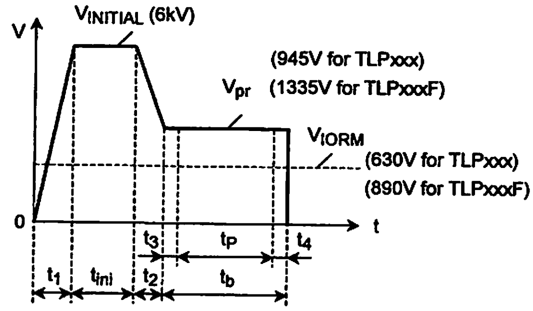


Figure 2 Partial discharge measurement procedure according to VDE0884 non–destructive test for 100% inspection.

Method B

(for sample test,non-destructive test)

t3,t4	=0.1s
tP(measuring time for partial discharge)	=1s
tb	=1.2s

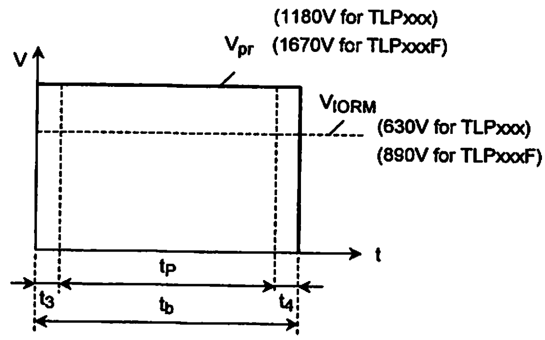
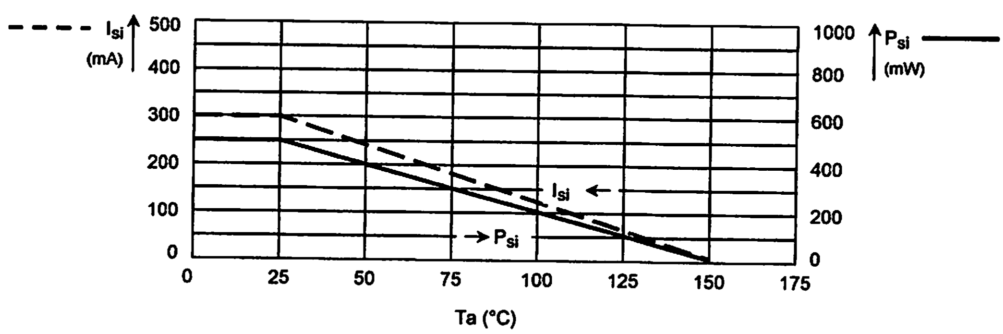


Figure 3 Dependency of maximum safety ratings on ambient temperature



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National Semiconductor

November 1994

LM741 Operational Amplifier

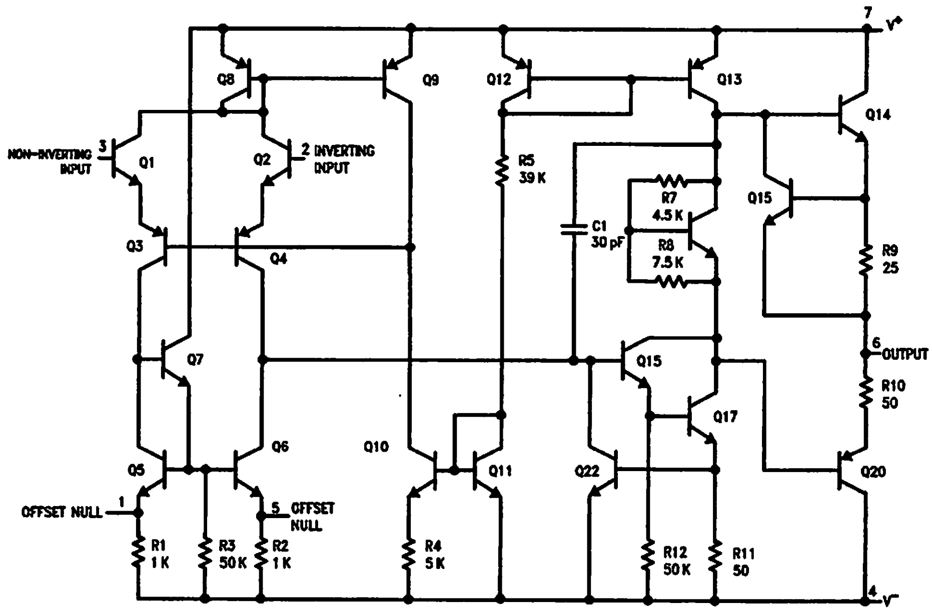
General Description

The LM741 series are general purpose operational amplifiers which feature improved performance over industry standards like the LM709. They are direct, plug-in replacements for the 709C, LM201, MC1439 and 748 in most applications.

The amplifiers offer many features which make their application nearly foolproof: overload protection on the input and output, no latch-up when the common mode range is exceeded, as well as freedom from oscillations.

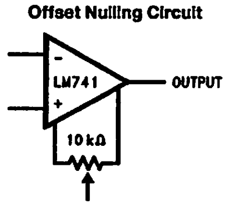
The LM741C/LM741E are identical to the LM741/LM741A except that the LM741C/LM741E have their performance guaranteed over a 0°C to +70°C temperature range, instead of −55°C to +125°C.

Schematic Diagram



TL/H/9341–1

Offset Nulling Circuit



TL/H/9341–7

RRD-B30M115/Printed in U. S. A.

Absolute Maximum Ratings

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/ Distributors for availability and specifications.
(Note 5)

	LM741A	LM741E	LM741	LM741C
Supply Voltage	±22V	±22V	±22V	±18V
Power Dissipation (Note 1)	500 mW	500 mW	500 mW	500 mW
Differential Input Voltage	±30V	±30V	±30V	±30V
Input Voltage (Note 2)	±15V	±15V	±15V	±15V
Output Short Circuit Duration	Continuous	Continuous	Continuous	Continuous
Operating Temperature Range	−55°C to +125°C	0°C to +70°C	−55°C to +125°C	0°C to +70°C
Storage Temperature Range	−65°C to +150°C	−65°C to +150°C	−65°C to +150°C	−65°C to +150°C
Junction Temperature	150°C	100°C	150°C	100°C
Soldering Information				
N-Package (10 seconds)	260°C	260°C	260°C	260°C
J- or H-Package (10 seconds)	300°C	300°C	300°C	300°C
M-Package				
Vapor Phase (60 seconds)	215°C	215°C	215°C	215°C
Infrared (15 seconds)	215°C	215°C	215°C	215°C

See AN-450 "Surface Mounting Methods and Their Effect on Product Reliability" for other methods of soldering surface mount devices.

	LM741A	LM741E	LM741	LM741C
ESD Tolerance (Note 6)	400V	400V	400V	400V

Electrical Characteristics (Note 3)

Parameter	Conditions	LM741A/LM741E			LM741			LM741C			Units
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
Input Offset Voltage	$T_A = 25°C$ $R_S \le 10\ k\Omega$ $R_S \le 50\Omega$		 0.8	 3.0		 1.0	 5.0		 2.0	 6.0	 mV mV
	$T_{AMIN} \le T_A \le T_{AMAX}$ $R_S \le 50\Omega$ $R_S \le 10\ k\Omega$			 4.0			 6.0			 7.5	 mV mV
Average Input Offset Voltage Drift				15							μV/°C
Input Offset Voltage Adjustment Range	$T_A = 25°C, V_S = \pm 20V$	±10				±15			±15		mV
Input Offset Current	$T_A = 25°C$		3.0	30		20	200		20	200	nA
	$T_{AMIN} \le T_A \le T_{AMAX}$			70		85	500			300	nA
Average Input Offset Current Drift				0.5							nA/°C
Input Bias Current	$T_A = 25°C$		30	80		80	500		80	500	nA
	$T_{AMIN} \le T_A \le T_{AMAX}$			0.210			1.5			0.8	μA
Input Resistance	$T_A = 25°C, V_S = \pm 20V$	1.0	6.0		0.3	2.0		0.3	2.0		MΩ
	$T_{AMIN} \le T_A \le T_{AMAX}$, $V_S = \pm 20V$	0.5									MΩ
Input Voltage Range	$T_A = 25°C$							±12	±13		V
	$T_{AMIN} \le T_A \le T_{AMAX}$				±12	±13					V
Large Signal Voltage Gain	$T_A = 25°C, R_L \ge 2\ k\Omega$ $V_S = \pm 20V, V_O = \pm 15V$ $V_S = \pm 15V, V_O = \pm 10V$	 50			 50	 200		 20	 200		 V/mV V/mV
	$T_{AMIN} \le T_A \le T_{AMAX}$, $R_L \ge 2\ k\Omega$, $V_S = \pm 20V, V_O = \pm 15V$ $V_S = \pm 15V, V_O = \pm 10V$ $V_S = \pm 5V, V_O = \pm 2V$	 32 10			 25			 15			 V/mV V/mV V/mV

Electrical Characteristics (Note 3) (Continued)

Parameter	Conditions	LM741A/LM741E			LM741			LM741C			Units
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
Output Voltage Swing	$V_S = \pm 20V$										
	$R_L \geq 10\ k\Omega$	±16									V
	$R_L \geq 2\ k\Omega$	±15									V
	$V_S = \pm 15V$										
	$R_L \geq 10\ k\Omega$				±12	±14		±12	±14		V
	$R_L \geq 2\ k\Omega$				±10	±13		±10	±13		V
Output Short Circuit Current	$T_A = 25°C$	10	25	35		25			25		mA
	$T_{AMIN} \leq T_A \leq T_{AMAX}$	10		40							mA
Common-Mode Rejection Ratio	$T_{AMIN} \leq T_A \leq T_{AMAX}$										
	$R_S \leq 10\ k\Omega$, $V_{CM} = \pm 12V$				70	90		70	90		dB
	$R_S \leq 50\Omega$, $V_{CM} = \pm 12V$	80	95								dB
Supply Voltage Rejection Ratio	$T_{AMIN} \leq T_A \leq T_{AMAX}$, $V_S = \pm 20V$ to $V_S = \pm 5V$										
	$R_S \leq 50\Omega$	86	96								dB
	$R_S \leq 10\ k\Omega$				77	96		77	96		dB
Transient Response	$T_A = 25°C$, Unity Gain										
Rise Time			0.25	0.8		0.3			0.3		µs
Overshoot			6.0	20		5			5		%
Bandwidth (Note 4)	$T_A = 25°C$	0.437	1.5								MHz
Slew Rate	$T_A = 25°C$, Unity Gain	0.3	0.7			0.5			0.5		V/µs
Supply Current	$T_A = 25°C$					1.7	2.8		1.7	2.8	mA
Power Consumption	$T_A = 25°C$										
	$V_S = \pm 20V$		80	150							mW
	$V_S = \pm 15V$					50	85		50	85	mW
LM741A	$V_S = \pm 20V$										
	$T_A = T_{AMIN}$			165							mW
	$T_A = T_{AMAX}$			135							mW
LM741E	$V_S = \pm 20V$										
	$T_A = T_{AMIN}$			150							mW
	$T_A = T_{AMAX}$			150							mW
LM741	$V_S = \pm 15V$										
	$T_A = T_{AMIN}$					60	100				mW
	$T_A = T_{AMAX}$					45	75				mW

Note 1: For operation at elevated temperatures, these devices must be derated based on thermal resistance, and T_j max. (listed under "Absolute Maximum Ratings"). $T_j = T_A + (\theta_{jA} P_D)$.

Thermal Resistance	Cerdip (J)	DIP (N)	HO8 (H)	SO-8 (M)
θ_{jA} (Junction to Ambient)	100°C/W	100°C/W	170°C/W	195°C/W
θ_{jC} (Junction to Case)	N/A	N/A	25°C/W	N/A

Note 2: For supply voltages less than ±15V, the absolute maximum input voltage is equal to the supply voltage.

Note 3: Unless otherwise specified, these specifications apply for $V_S = \pm 15V$, $-55°C \leq T_A \leq +125°C$ (LM741/LM741A). For the LM741C/LM741E, these specifications are limited to $0°C \leq T_A \leq +70°C$.

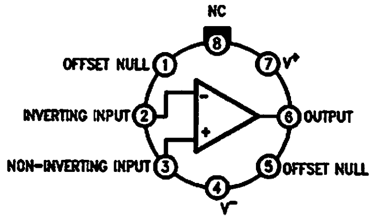
Note 4: Calculated value from: BW (MHz) = 0.35/Rise Time(µs).

Note 5: For military specifications see RETS741X for LM741 and RETS741AX for LM741A.

Note 6: Human body model, 1.5 kΩ in series with 100 pF.

Connection Diagrams

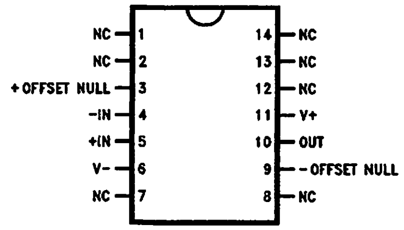
Metal Can Package



TL/H/9341-2

Order Number LM741H, LM741H/883*, LM741AH/883 or LM741CH
See NS Package Number H08C

Ceramic Dual-In-Line Package

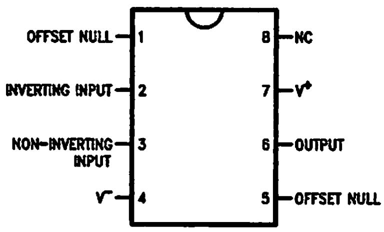


TL/H/9341-5

Order Number LM741J-14/883*, LM741AJ-14/883**
See NS Package Number J14A

*also available per JM38510/10101
**also available per JM38510/10102

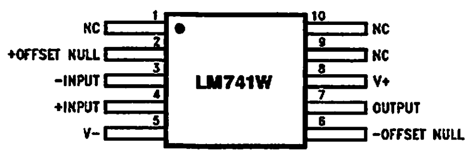
Dual-In-Line or S.O. Package



TL/H/9341-3

Order Number LM741J, LM741J/883, LM741CM, LM741CN or LM741EN
See NS Package Number J08A, M08A or N08E

Ceramic Flatpak

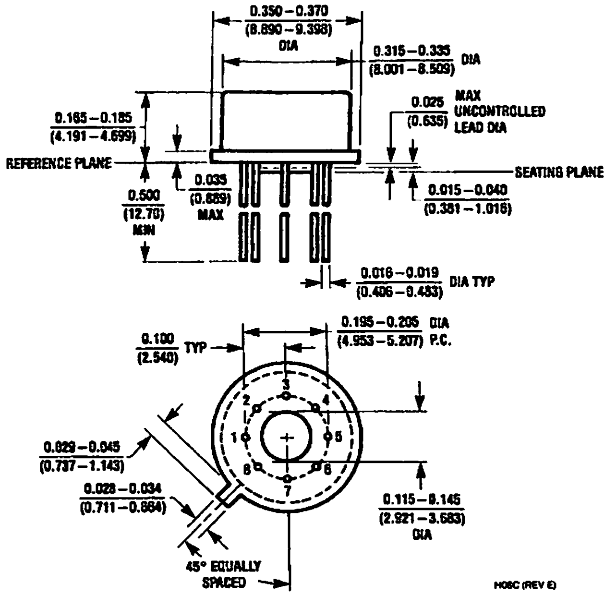


TL/H/9341-6

Order Number LM741W/883
See NS Package Number W10A

*LM741H is available per JM38510/10101

Physical Dimensions inches (millimeters)

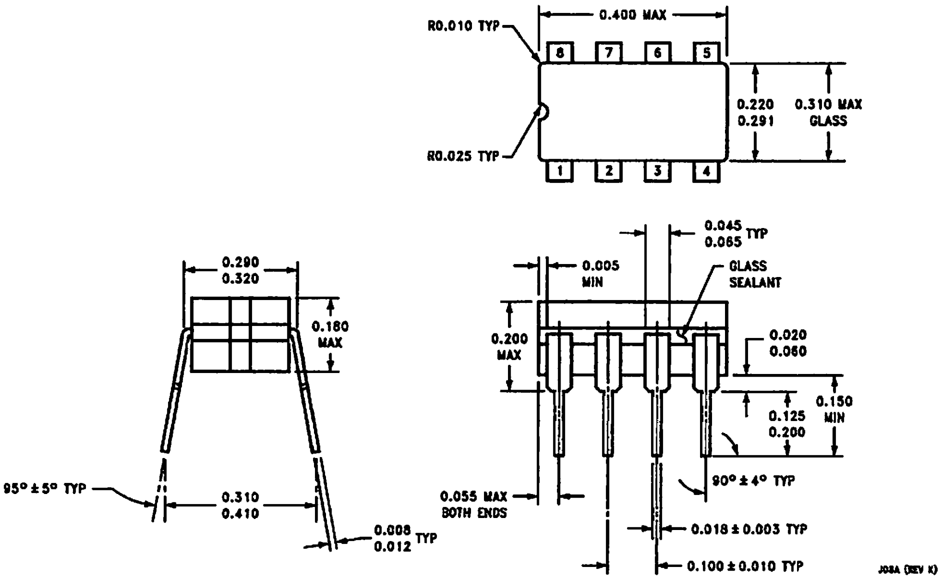


Metal Can Package (H)

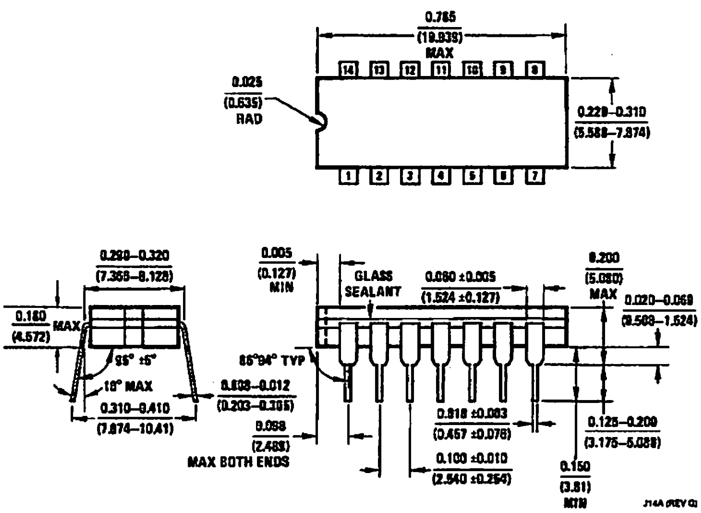
Order Number LM741H, LM741H/883, LM741AH/883, LM741CH or LM741EH

NS Package Number H08C

Physical Dimensions inches (millimeters) (Continued)

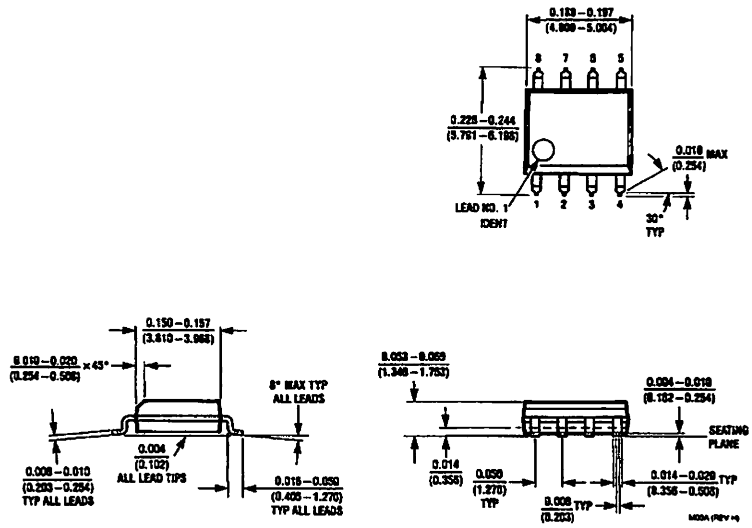


Ceramic Dual-In-Line Package (J)
Order Number LM741CJ or LM741J/883
NS Package Number J08A

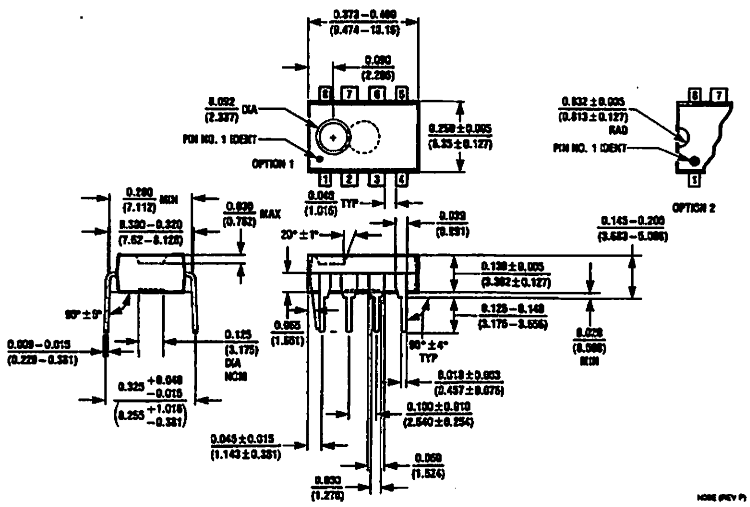


Ceramic Dual-In-Line Package (J)
Order Number LM741J-14/883 or LM741AJ-14/883
NS Package Number J14A

Physical Dimensions inches (millimeters) (Continued)

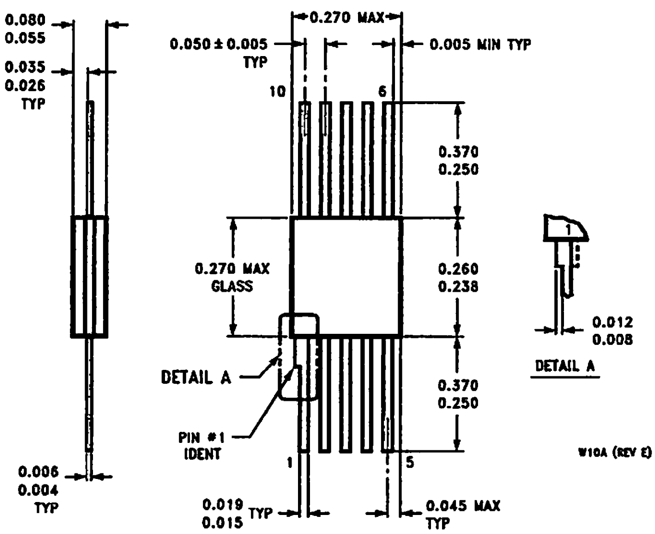


Small Outline Package (M)
Order Number LM741CM
NS Package Number M08A



Dual-In-Line Package (N)
Order Number LM741CN or LM741EN
NS Package Number N08E

Physical Dimensions inches (millimeters) (Continued)



10-Lead Ceramic Flatpak (W)
Order Number LM741W/883
NS Package Number W10A

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National Semiconductor Japan Ltd.
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Fax: 81-043-299-2408

atures

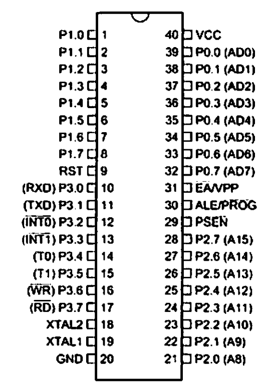
- ›mpatible with MCS-51™ Products
- ‹ Bytes of In-System Reprogrammable Flash Memory
  – Endurance: 1,000 Write/Erase Cycles
- ılly Static Operation: 0 Hz to 24 MHz
- ıree-level Program Memory Lock
- :8 x 8-bit Internal RAM
- : Programmable I/O Lines
- ‹o 16-bit Timer/Counters
- x Interrupt Sources
- ogrammable Serial Channel
- ›w-power Idle and Power-down Modes

scription

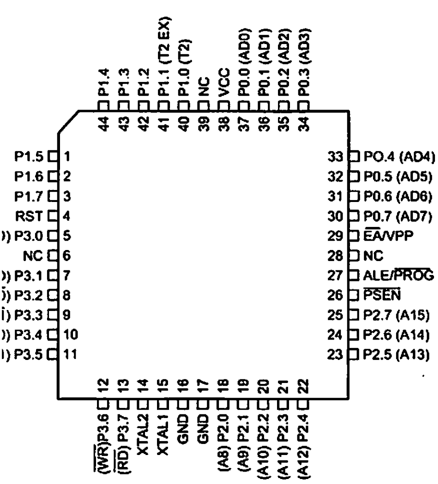
AT89C51 is a low-power, high-performance CMOS 8-bit microcomputer with 4K s of Flash programmable and erasable read only memory (PEROM). The device anufactured using Atmel's high-density nonvolatile memory technology and is patible with the industry-standard MCS-51 instruction set and pinout. The on-chip h allows the program memory to be reprogrammed in-system or by a conven- ıl nonvolatile memory programmer. By combining a versatile 8-bit CPU with Flash monolithic chip, the Atmel AT89C51 is a powerful microcomputer which provides ȷhly-flexible and cost-effective solution to many embedded control applications.

ı Configurations

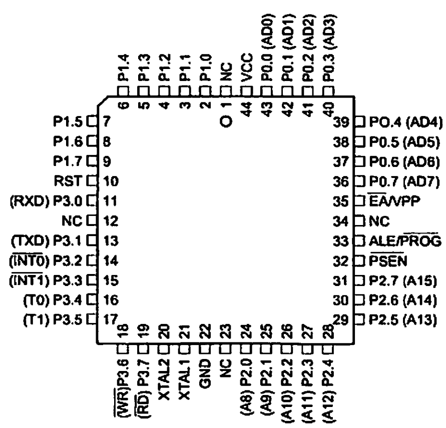
PDIP



PQFP/TQFP



PLCC



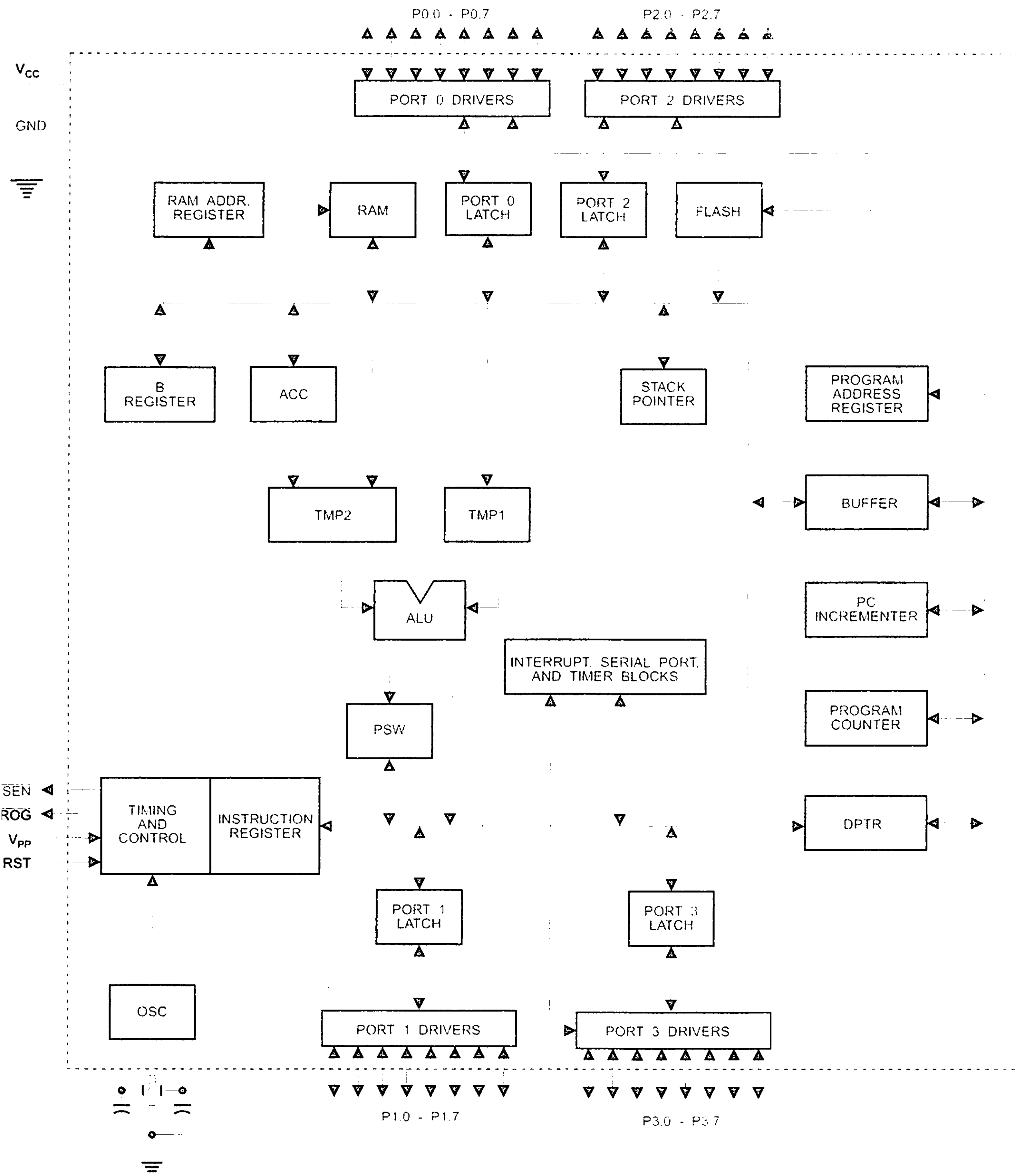
8-bit Microcontroller with 4K Bytes Flash

AT89C51

Not Recommended for New Designs. Use AT89S51.

Rev. 0265G–02/00

ock Diagram


P0.0 - P0.7
P2.0 - P2.7
VCC
GND
PORT 0 DRIVERS
PORT 2 DRIVERS
RAM ADDR. REGISTER
RAM
PORT 0 LATCH
PORT 2 LATCH
FLASH
B REGISTER
ACC
STACK POINTER
PROGRAM ADDRESS REGISTER
TMP2
TMP1
BUFFER
ALU
PC INCREMENTER
INTERRUPT, SERIAL PORT, AND TIMER BLOCKS
PSW
PROGRAM COUNTER
SEN
ROG
VPP
RST
TIMING AND CONTROL
INSTRUCTION REGISTER
DPTR
PORT 1 LATCH
PORT 3 LATCH
OSC
PORT 1 DRIVERS
PORT 3 DRIVERS
P1.0 - P1.7
P3.0 - P3.7

AT89C51 provides the following standard features: 4K s of Flash, 128 bytes of RAM, 32 I/O lines, two 16-bit r/counters, a five vector two-level interrupt architecture, l duplex serial port, on-chip oscillator and clock cir- y. In addition, the AT89C51 is designed with static logic peration down to zero frequency and supports two vare selectable power saving modes. The Idle Mode s the CPU while allowing the RAM, timer/counters, il port and interrupt system to continue functioning. The er-down Mode saves the RAM contents but freezes oscillator disabling all other chip functions until the next ware reset.

Description

ly voltage.

ınd.

0

0 is an 8-bit open-drain bi-directional I/O port. As an ut port, each pin can sink eight TTL inputs. When 1s written to port 0 pins, the pins can be used as high- dance inputs.

0 may also be configured to be the multiplexed low- r address/data bus during accesses to external pro- n and data memory. In this mode P0 has internal ps.

0 also receives the code bytes during Flash program- g, and outputs the code bytes during program ication. External pullups are required during program cation.

1

1 is an 8-bit bi-directional I/O port with internal pullups. Port 1 output buffers can sink/source four TTL inputs. n 1s are written to Port 1 pins they are pulled high by nternal pullups and can be used as inputs. As inputs, 1 pins that are externally being pulled low will source ent (I_{IL}) because of the internal pullups.

1 also receives the low-order address bytes during n programming and verification.

2

2 is an 8-bit bi-directional I/O port with internal pullups. Port 2 output buffers can sink/source four TTL inputs. n 1s are written to Port 2 pins they are pulled high by nternal pullups and can be used as inputs. As inputs, Port 2 pins that are externally being pulled low will source current (I_{IL}) because of the internal pullups.

Port 2 emits the high-order address byte during fetches from external program memory and during accesses to external data memory that use 16-bit addresses (MOVX @ DPTR). In this application, it uses strong internal pullups when emitting 1s. During accesses to external data memory that use 8-bit addresses (MOVX @ RI), Port 2 emits the contents of the P2 Special Function Register.

Port 2 also receives the high-order address bits and some control signals during Flash programming and verification.

Port 3

Port 3 is an 8-bit bi-directional I/O port with internal pullups. The Port 3 output buffers can sink/source four TTL inputs. When 1s are written to Port 3 pins they are pulled high by the internal pullups and can be used as inputs. As inputs, Port 3 pins that are externally being pulled low will source current (I_{IL}) because of the pullups.

Port 3 also serves the functions of various special features of the AT89C51 as listed below:

Port Pin	Alternate Functions
P3.0	RXD (serial input port)
P3.1	TXD (serial output port)
P3.2	$\overline{INT0}$ (external interrupt 0)
P3.3	$\overline{INT1}$ (external interrupt 1)
P3.4	T0 (timer 0 external input)
P3.5	T1 (timer 1 external input)
P3.6	$\overline{WR}$ (external data memory write strobe)
P3.7	$\overline{RD}$ (external data memory read strobe)

Port 3 also receives some control signals for Flash programming and verification.

RST

Reset input. A high on this pin for two machine cycles while the oscillator is running resets the device.

ALE/$\overline{PROG}$

Address Latch Enable output pulse for latching the low byte of the address during accesses to external memory. This pin is also the program pulse input ($\overline{PROG}$) during Flash programming.

In normal operation ALE is emitted at a constant rate of 1/6 the oscillator frequency, and may be used for external timing or clocking purposes. Note, however, that one ALE e is skipped during each access to external Data ıory.

sired, ALE operation can be disabled by setting bit 0 of location 8EH. With the bit set, ALE is active only dur- a MOVX or MOVC instruction. Otherwise, the pin is kly pulled high. Setting the ALE-disable bit has no :t if the microcontroller is in external execution mode.

N

ıram Store Enable is the read strobe to external pro- ı memory.

ın the AT89C51 is executing code from external pro- ı memory, $\overline{\text{PSEN}}$ is activated twice each machine ;, except that two $\overline{\text{PSEN}}$ activations are skipped during ı access to external data memory.

/PP

rnal Access Enable. $\overline{\text{EA}}$ must be strapped to GND in r to enable the device to fetch code from external pro- ı memory locations starting at 0000H up to FFFFH. , however, that if lock bit 1 is programmed, $\overline{\text{EA}}$ will be nally latched on reset.

;hould be strapped to V_{CC} for internal program utions.

pin also receives the 12-volt programming enable volt- (V_{PP}) during Flash programming, for parts that require olt V_{PP}.

L1

t to the inverting oscillator amplifier and input to the ıal clock operating circuit.

L2

ut from the inverting oscillator amplifier.

:illator Characteristics

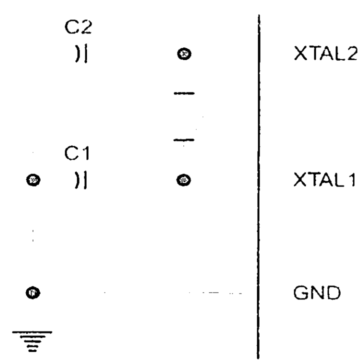
L1 and XTAL2 are the input and output, respectively, ı inverting amplifier which can be configured for use as ı-chip oscillator, as shown in Figure 1. Either a quartz :al or ceramic resonator may be used. To drive the ;e from an external clock source, XTAL2 should be left unconnected while XTAL1 is driven as shown in Figure 2. There are no requirements on the duty cycle of the external clock signal, since the input to the internal clocking circuitry is through a divide-by-two flip-flop, but minimum and maximum voltage high and low time specifications must be observed.

Idle Mode

In idle mode, the CPU puts itself to sleep while all the on-chip peripherals remain active. The mode is invoked by software. The content of the on-chip RAM and all the special functions registers remain unchanged during this mode. The idle mode can be terminated by any enabled interrupt or by a hardware reset.

It should be noted that when idle is terminated by a hard ware reset, the device normally resumes program execution, from where it left off, up to two machine cycles before the internal reset algorithm takes control. On-chip hardware inhibits access to internal RAM in this event, but access to the port pins is not inhibited. To eliminate the possibility of an unexpected write to a port pin when Idle is terminated by reset, the instruction following the one that invokes Idle should not be one that writes to a port pin or to external memory.

Figure 1. Oscillator Connections

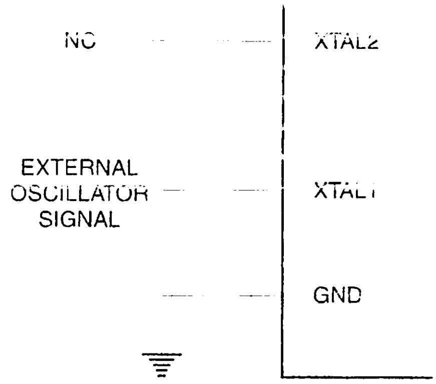


Note: C1, C2 = 30 pF ± 10 pF for Crystals
= 40 pF ± 10 pF for Ceramic Resonators

tus of External Pins During Idle and Power-down Modes

le	Program Memory	ALE	$\overline{\text{PSEN}}$	PORT0	PORT1	PORT2	PORT3
	Internal	1	1	Data	Data	Data	Data
	External	1	1	Float	Data	Address	Data
er-down	Internal	0	0	Data	Data	Data	Data
er-down	External	0	0	Float	Data	Data	Data

ıre 2. External Clock Drive Configuration



ver-down Mode

e power-down mode, the oscillator is stopped, and the ıction that invokes power-down is the last instruction uted. The on-chip RAM and Special Function Registers retain their values until the power-down mode is terminated. The only exit from power-down is a hardware reset. Reset redefines the SFRs but does not change the on-chip RAM. The reset should not be activated before V_{CC} is restored to its normal operating level and must be held active long enough to allow the oscillator to restart and stabilize.

Program Memory Lock Bits

On the chip are three lock bits which can be left unprogrammed (U) or can be programmed (P) to obtain the additional features listed in the table below.

When lock bit 1 is programmed, the logic level at the $\overline{EA}$ pin is sampled and latched during reset. If the device is powered up without a reset, the latch initializes to a random value. and holds that value until reset is activated. It is necessary that the latched value of $\overline{EA}$ be in agreement with the current logic level at that pin in order for the device to function properly.

:k Bit Protection Modes

	Program Lock Bits			
	LB1	LB2	LB3	Protection Type
1	U	U	U	No program lock features
2	P	U	U	MOVC instructions executed from external program memory are disabled from fetching code bytes from internal memory, $\overline{EA}$ is sampled and latched on reset, and further programming of the Flash is disabled
3	P	P	U	Same as mode 2, also verify is disabled
4	P	P	P	Same as mode 3, also external execution is disabled

›gramming the Flash

AT89C51 is normally shipped with the on-chip Flash ıory array in the erased state (that is, contents = FFH) ready to be programmed. The programming interface ɘpts either a high-voltage (12-volt) or a low-voltage ;) program enable signal. The low-voltage program- ȝ mode provides a convenient way to program the 9C51 inside the user's system, while the high-voltage ıramming mode is compatible with conventional third- / Flash or EPROM programmers.

AT89C51 is shipped with either the high-voltage or voltage programming mode enabled. The respective ɜide marking and device signature codes are listed in ollowing table.

	V_{PP} = 12V	V_{PP} = 5V
ı-side Mark	AT89C51 xxxx yyww	AT89C51 xxxx-5 yyww
nature	(030H) = 1EH (031H) = 51H (032H) =F FH	(030H) = 1EH (031H) = 51H (032H) = 05H

AT89C51 code memory array is programmed byte-by- in either programming mode. *To program any non- k byte in the on-chip Flash Memory, the entire memory t be erased using the Chip Erase Mode.*

ɡramming Algorithm: Before programming the 9C51, the address, data and control signals should be ıp according to the Flash programming mode table and re 3 and Figure 4. To program the AT89C51, take the ving steps.

nput the desired memory location on the address ines.

nput the appropriate data byte on the data lines.

\ctivate the correct combination of control signals.

Raise $\overline{EA}/V_{PP}$ to 12V for the high-voltage program- ning mode.

Pulse ALE/$\overline{PROG}$ once to program a byte in the Flash array or the lock bits. The byte-write cycle is self-timed and typically takes no more than 1.5 ms.

Repeat steps 1 through 5, changing the address and data for the entire array or until the end of the object file is reached.

$\overline{\text{Data}}$ Polling: The AT89C51 features $\overline{\text{Data}}$ Polling to indicate the end of a write cycle. During a write cycle, an attempted read of the last byte written will result in the complement of the written datum on PO.7. Once the write cycle has been completed, true data are valid on all outputs, and the next cycle may begin. $\overline{\text{Data}}$ Polling may begin any time after a write cycle has been initiated.

Ready/$\overline{\text{Busy}}$: The progress of byte programming can also be monitored by the RDY/$\overline{\text{BSY}}$ output signal. P3.4 is pulled low after ALE goes high during programming to indicate BUSY. P3.4 is pulled high again when programming is done to indicate READY.

Program Verify: If lock bits LB1 and LB2 have not been programmed, the programmed code data can be read back via the address and data lines for verification. The lock bits cannot be verified directly. Verification of the lock bits is achieved by observing that their features are enabled.

Chip Erase: The entire Flash array is erased electrically by using the proper combination of control signals and by holding ALE/$\overline{PROG}$ low for 10 ms. The code array is written with all "1"s. The chip erase operation must be executed before the code memory can be re-programmed.

Reading the Signature Bytes: The signature bytes are read by the same procedure as a normal verification of locations 030H, 031H, and 032H, except that P3.6 and P3.7 must be pulled to a logic low. The values returned are as follows.

(030H) = 1EH indicates manufactured by Atmel
(031H) = 51H indicates 89C51
(032H) = FFH indicates 12V programming
(032H) = 05H indicates 5V programming

Programming Interface

Every code byte in the Flash array can be written and the entire array can be erased by using the appropriate combination of control signals. The write operation cycle is self-timed and once initiated, will automatically time itself to completion.

All major programming vendors offer worldwide support for the Atmel microcontroller series. Please contact your local programming vendor for the appropriate software revision.

ısh Programming Modes

de		RST	PSEN	ALE/PROG	EA/V_{PP}	P2.6	P2.7	P3.6	P3.7
te Code Data		H	L		H/12V	L	H	H	H
ıd Code Data		H	L	H	H	L	L	H	H
te Lock	Bit - 1	H	L		H/12V	H	H	H	H
	Bit - 2	H	L		H/12V	H	H	L	L
	Bit - 3	H	L		H/12V	H	L	H	L
p Erase		H	L	(1)	H/12V	H	L	L	L
ıd Signature Byte		H	L	H	H	L	L	L	L

1. Chip Erase requires a 10 ms PROG pulse.

re 3. Programming the Flash

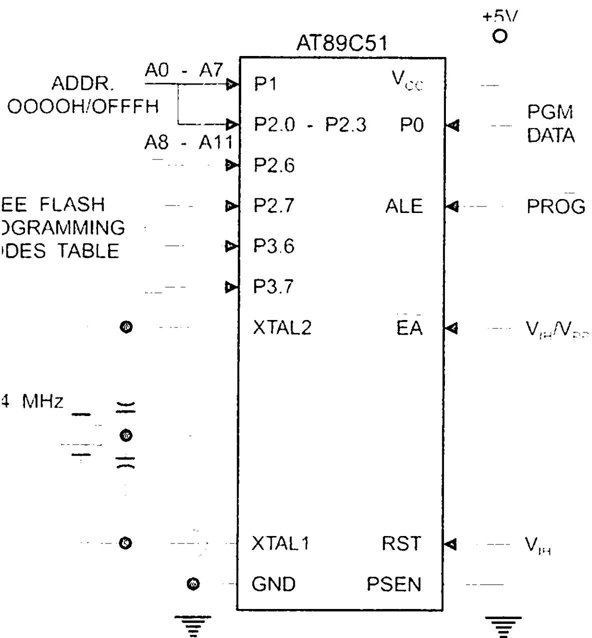
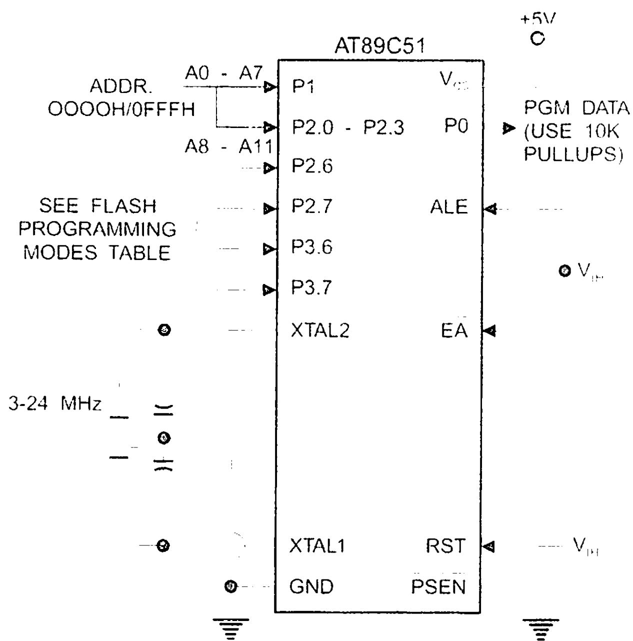
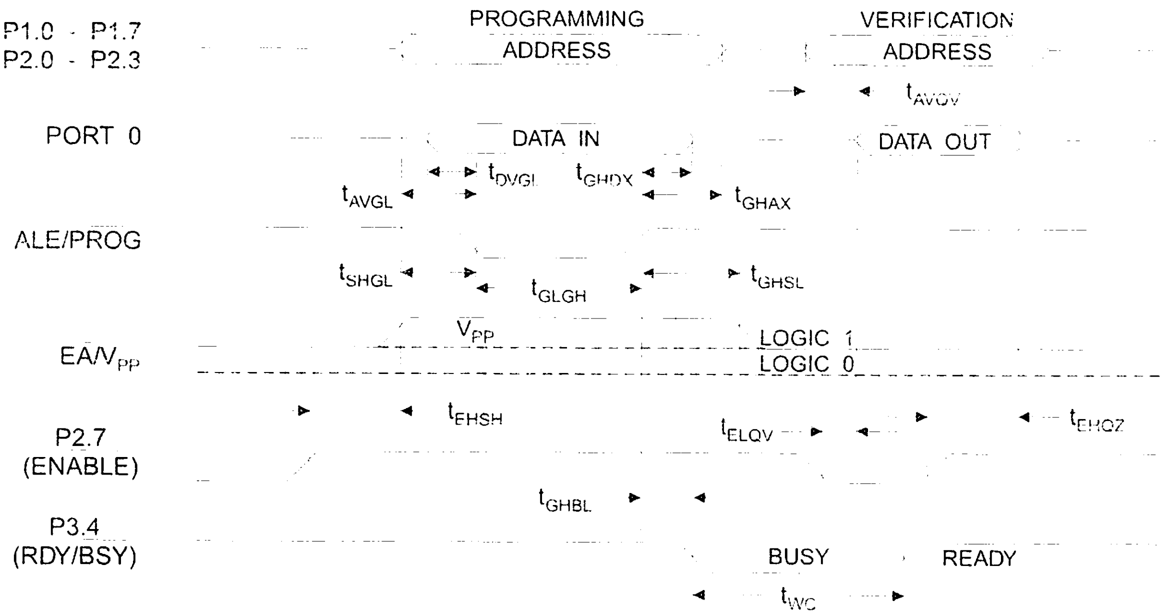


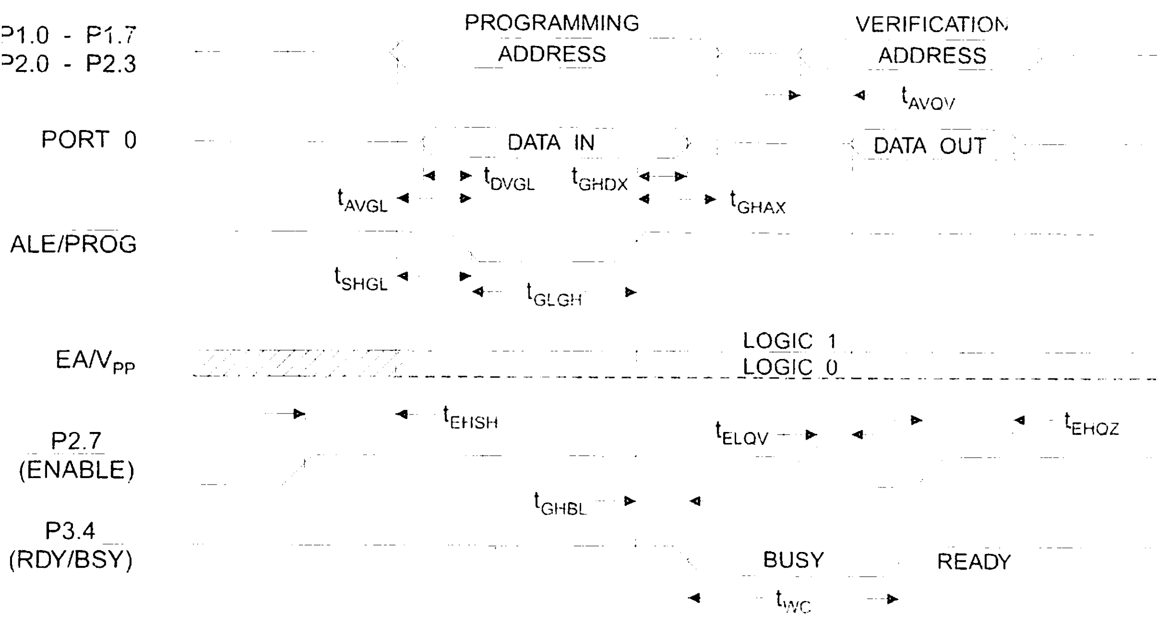
Figure 4. Verifying the Flash



sh Programming and Verification Waveforms - High-voltage Mode (V_{PP} = 12V)



sh Programming and Verification Waveforms - Low-voltage Mode (V_{PP} = 5V)



sh Programming and Verification Characteristics

0°C to 70°C, V_{CC} = 5.0 ± 10%

nbol	Parameter	Min	Max	Units
(1)	Programming Enable Voltage	11.5	12.5	V
1)	Programming Enable Current		1.0	mA
LCL	Oscillator Frequency	3	24	MHz
L	Address Setup to $\overline{PROG}$ Low	$48t_{CLCL}$		
X	Address Hold after $\overline{PROG}$	$48t_{CLCL}$		
L	Data Setup to $\overline{PROG}$ Low	$48t_{CLCL}$		
X	Data Hold after $\overline{PROG}$	$48t_{CLCL}$		
H	P2.7 ($\overline{ENABLE}$) High to V_{PP}	$48t_{CLCL}$		
L	V_{PP} Setup to $\overline{PROG}$ Low	10		µs
L(1)	V_{PP} Hold after $\overline{PROG}$	10		µs
H	$\overline{PROG}$ Width	1	110	µs
V	Address to Data Valid		$48t_{CLCL}$	
V	$\overline{ENABLE}$ Low to Data Valid		$48t_{CLCL}$	
Z	Data Float after $\overline{ENABLE}$	0	$48t_{CLCL}$	
L	$\overline{PROG}$ High to $\overline{BUSY}$ Low		1.0	µs
	Byte Write Cycle Time		2.0	ms

1. Only used in 12-volt programming mode.

solute Maximum Ratings*

erating Temperature................................. -55°C to +125°C

rage Temperature.................................... -65°C to +150°C

tage on Any Pin
ı Respect to Ground ....-1.0V to +7.0V

ximum Operating Voltage 6.6V

Output Current.. 15.0 mA

*NOTICE: Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Characteristics

-40°C to 85°C, V_{CC} = 5.0V ±20% (unless otherwise noted)

ıbol	Parameter	Condition	Min	Max	Units
	Input Low-voltage	(Except $\overline{EA}$)	-0.5	0.2 V_{CC} - 0.1	V
	Input Low-voltage ($\overline{EA}$)		-0.5	0.2 V_{CC} - 0.3	V
	Input High-voltage	(Except XTAL1, RST)	0.2 V_{CC} + 0.9	V_{CC} + 0.5	V
	Input High-voltage	(XTAL1, RST)	0.7 V_{CC}	V_{CC} + 0.5	V
	Output Low-voltage[1] (Ports 1,2,3)	I_{OL} = 1.6 mA		0.45	V
ı	Output Low-voltage[1] (Port 0, ALE, $\overline{PSEN}$)	I_{OL} = 3.2 mA		0.45	V
	Output High-voltage (Ports 1,2,3, ALE, $\overline{PSEN}$)	I_{OH} = -60 µA, V_{CC} = 5V ±10%	2.4		V
		I_{OH} = -25 µA	0.75 V_{CC}		V
		I_{OH} = -10 µA	0.9 V_{CC}		V
ı	Output High-voltage (Port 0 in External Bus Mode)	I_{OH} = -800 µA, V_{CC} = 5V ±10%	2.4		V
		I_{OH} = -300 µA	0.75 V_{CC}		V
		I_{OH} = -80 µA	0.9 V_{CC}		V
	Logical 0 Input Current (Ports 1,2,3)	V_{IN} = 0.45V		-50	µA
	Logical 1 to 0 Transition Current (Ports 1,2,3)	V_{IN} = 2V, VCC = 5V ± 10%		-650	µA
	Input Leakage Current (Port 0, $\overline{EA}$)	0.45 < V_{IN} < V_{CC}		±10	µA
;T	Reset Pull-down Resistor		50	300	KΩ
	Pin Capacitance	Test Freq. = 1 MHz, T_A = 25°C		10	pF
	Power Supply Current	Active Mode, 12 MHz		20	mA
		Idle Mode, 12 MHz		5	mA
	Power-down Mode[2]	V_{CC} = 6V		100	µA
		V_{CC} = 3V		40	µA

;: 1. Under steady state (non-transient) conditions, I_{OL} must be externally limited as follows:
Maximum I_{OL} per port pin: 10 mA
Maximum I_{OL} per 8-bit port: Port 0: 26 mA
Ports 1. 2. 3: 15 mA
Maximum total I_{OL} for all output pins: 71 mA
If I_{OL} exceeds the test condition, V_{OL} may exceed the related specification. Pins are not guaranteed to sink current greater than the listed test conditions.
2. Minimum V_{CC} for Power-down is 2V.

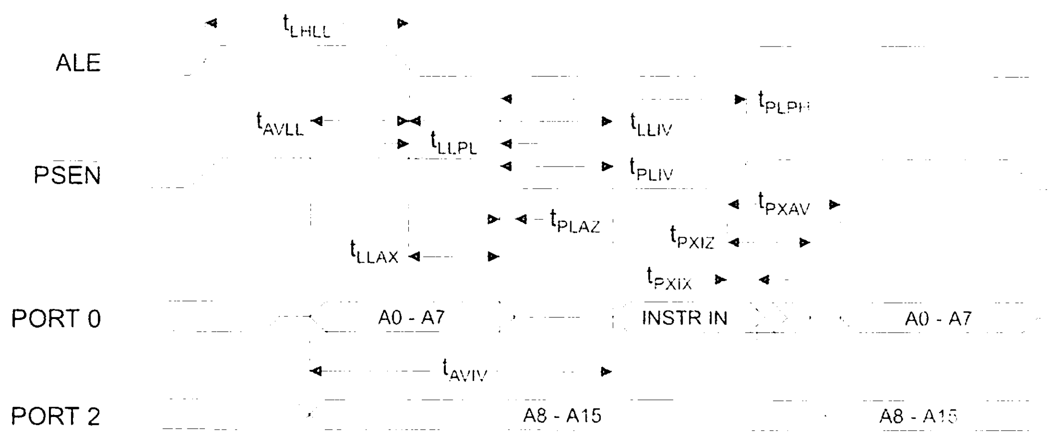
Characteristics

er operating conditions, load capacitance for Port 0, ALE/$\overline{\text{PROG}}$, and $\overline{\text{PSEN}}$ = 100 pF; load capacitance for all other uts = 80 pF.

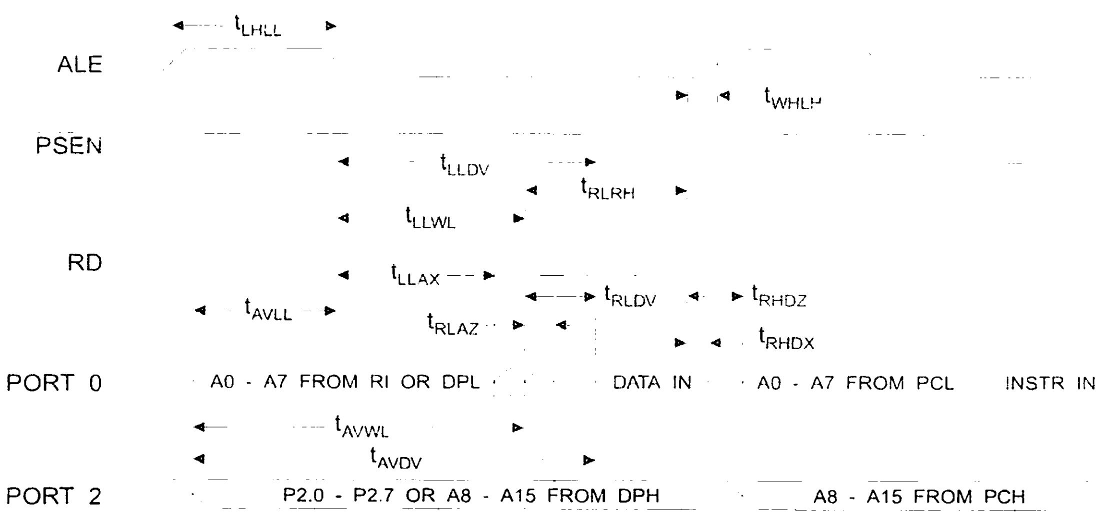
ternal Program and Data Memory Characteristics

		12 MHz Oscillator		16 to 24 MHz Oscillator		
nbol	Parameter	Min	Max	Min	Max	Units
:LCL	Oscillator Frequency			0	24	MHz
L	ALE Pulse Width	127		$2t_{CLCL}$-40		ns
L	Address Valid to ALE Low	43		t_{CLCL}-13		ns
X	Address Hold after ALE Low	48		t_{CLCL}-20		ns
/	ALE Low to Valid Instruction In		233		$4t_{CLCL}$-65	ns
L	ALE Low to $\overline{\text{PSEN}}$ Low	43		t_{CLCL}-13		ns
H	$\overline{\text{PSEN}}$ Pulse Width	205		$3t_{CLCL}$-20		ns
/	$\overline{\text{PSEN}}$ Low to Valid Instruction In		145		$3t_{CLCL}$-45	ns
(	Input Instruction Hold after $\overline{\text{PSEN}}$	0		0		ns
:	Input Instruction Float after $\overline{\text{PSEN}}$		59		t_{CLCL}-10	ns
.V	$\overline{\text{PSEN}}$ to Address Valid	75		t_{CLCL}-8		ns
/	Address to Valid Instruction In		312		$5t_{CLCL}$-55	ns
Z	$\overline{\text{PSEN}}$ Low to Address Float		10		10	ns
H	$\overline{\text{RD}}$ Pulse Width	400		$6t_{CLCL}$-100		ns
VH	$\overline{\text{WR}}$ Pulse Width	400		$6t_{CLCL}$-100		ns
V	$\overline{\text{RD}}$ Low to Valid Data In		252		$5t_{CLCL}$-90	ns
IX	Data Hold after $\overline{\text{RD}}$	0		0		ns
IZ	Data Float after $\overline{\text{RD}}$		97		$2t_{CLCL}$-28	ns
/	ALE Low to Valid Data In		517		$8t_{CLCL}$-150	ns
V	Address to Valid Data In		585		$9t_{CLCL}$-165	ns
L	ALE Low to $\overline{\text{RD}}$ or $\overline{\text{WR}}$ Low	200	300	$3t_{CLCL}$-50	$3t_{CLCL}$+50	ns
'L	Address to $\overline{\text{RD}}$ or $\overline{\text{WR}}$ Low	203		$4t_{CLCL}$-75		ns
/X	Data Valid to $\overline{\text{WR}}$ Transition	23		t_{CLCL}-20		ns
/H	Data Valid to $\overline{\text{WR}}$ High	433		$7t_{CLCL}$-120		ns
)X	Data Hold after $\overline{\text{WR}}$	33		t_{CLCL}-20		ns
Z	$\overline{\text{RD}}$ Low to Address Float		0		0	ns
.H	$\overline{\text{RD}}$ or $\overline{\text{WR}}$ High to ALE High	43	123	t_{CLCL}-20	t_{CLCL}+25	ns

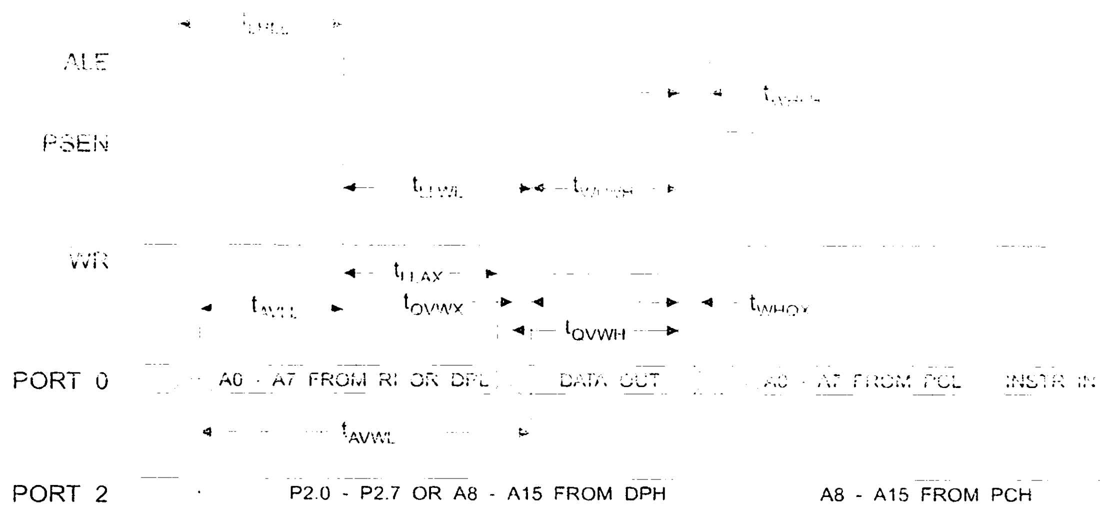
ternal Program Memory Read Cycle



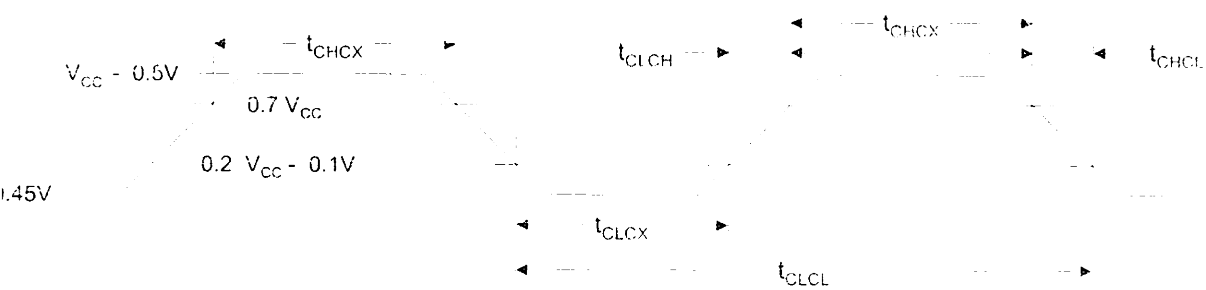
ternal Data Memory Read Cycle



ternal Data Memory Write Cycle



:ernal Clock Drive Waveforms



:ernal Clock Drive

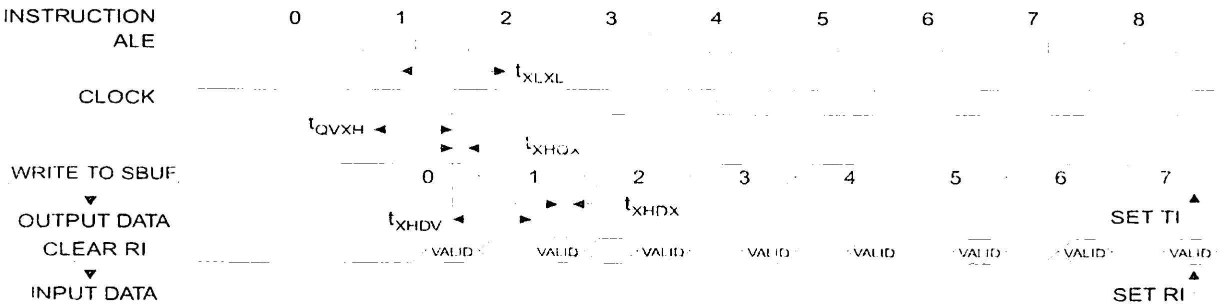
nbol	Parameter	Min	Max	Units
LCL	Oscillator Frequency	0	24	MHz
L	Clock Period	41.6		ns
X	High Time	15		ns
X	Low Time	15		ns
H	Rise Time		20	ns
L	Fall Time		20	ns

rial Port Timing: Shift Register Mode Test Conditions

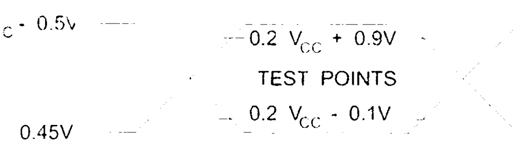
= 5.0 V ±20%; Load Capacitance = 80 pF)

nbol	Parameter	12 MHz Osc		Variable Oscillator		Units
		Min	Max	Min	Max	
L	Serial Port Clock Cycle Time	1.0		$12t_{CLCL}$		µs
H	Output Data Setup to Clock Rising Edge	700		$10t_{CLCL}-133$		ns
X	Output Data Hold after Clock Rising Edge	50		$2t_{CLCL}-117$		ns
X	Input Data Hold after Clock Rising Edge	0		0		ns
V	Clock Rising Edge to Input Data Valid		700		$10t_{CLCL}-133$	ns

ift Register Mode Timing Waveforms

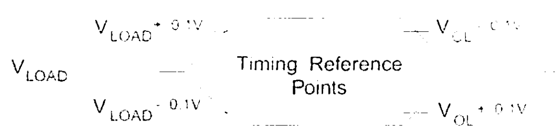


Testing Input/Output Waveforms(1)



1. AC Inputs during testing are driven at V_{CC} - 0.5V for a logic 1 and 0.45V for a logic 0. Timing measurements are made at V_{IH} min. for a logic 1 and V_{IL} max. for a logic 0.

Float Waveforms(1)



Note: 1. For timing purposes, a port pin is no longer floating when a 100 mV change from load voltage occurs. A port pin begins to float when 100 mV change from the loaded V_{OH}/V_{OL} level occurs.

dering Information

peed MHz)	Power Supply	Ordering Code	Package	Operation Range
12	5V ±20%	AT89C51-12AC	44A	Commercial
		AT89C51-12JC	44J	(0° C to 70° C)
		AT89C51-12PC	40P6	
		AT89C51-12QC	44Q	
		AT89C51-12AI	44A	Industrial
		AT89C51-12JI	44J	(-40° C to 85° C)
		AT89C51-12PI	40P6	
		AT89C51-12QI	44Q	
16	5V ±20%	AT89C51-16AC	44A	Commercial
		AT89C51-16JC	44J	(0° C to 70° C)
		AT89C51-16PC	40P6	
		AT89C51-16QC	44Q	
		AT89C51-16AI	44A	Industrial
		AT89C51-16JI	44J	(-40° C to 85° C)
		AT89C51-16PI	40P6	
		AT89C51-16QI	44Q	
20	5V ±20%	AT89C51-20AC	44A	Commercial
		AT89C51-20JC	44J	(0° C to 70° C)
		AT89C51-20PC	40P6	
		AT89C51-20QC	44Q	
		AT89C51-20AI	44A	Industrial
		AT89C51-20JI	44J	(-40° C to 85° C)
		AT89C51-20PI	40P6	
		AT89C51-20QI	44Q	
24	5V ±20%	AT89C51-24AC	44A	Commercial
		AT89C51-24JC	44J	(0° C to 70° C)
		AT89C51-24PC	40P6	
		AT89C51-24QC	44Q	
		AT89C51-24AI	44A	Industrial
		AT89C51-24JI	44J	(-40° C to 85° C)
		AT89C51-24PI	40P6	
		AT89C51-24QI	44Q	

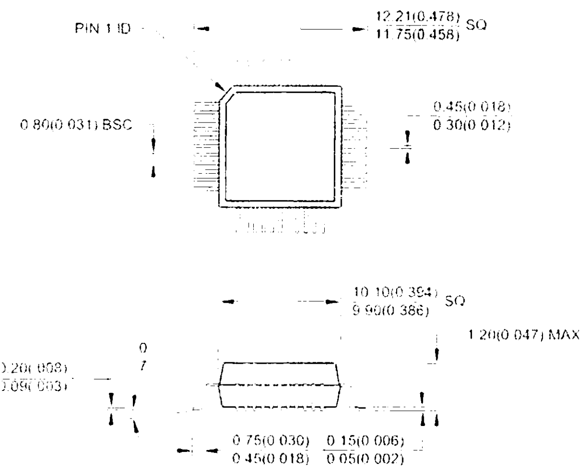
	Package Type
	44-lead, Thin Plastic Gull Wing Quad Flatpack (TQFP)
	44-lead, Plastic J-leaded Chip Carrier (PLCC)
6	40-lead, 0.600" Wide, Plastic Dual Inline Package (PDIP)
	44-lead, Plastic Gull Wing Quad Flatpack (PQFP)

:kaging Information

44A, 44-lead, Thin (1.0 mm) Plastic Gull Wing Quad Flatpack (TQFP)

Dimensions in Millimeters and (Inches)*

JEDEC STANDARD MS-026 ACB

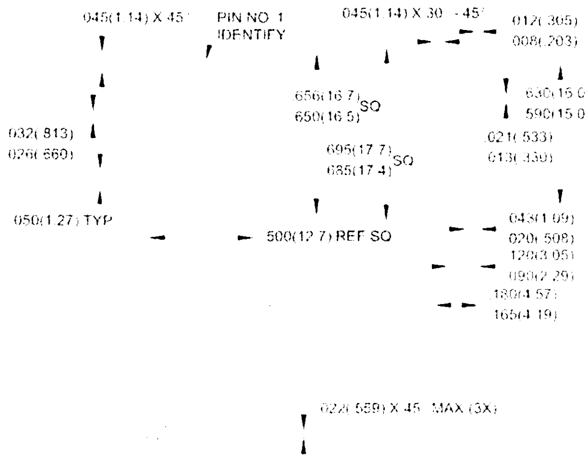


*Controlling dimension: millimeters

44J, 44-lead, Plastic J-leaded Chip Carrier (PLCC)

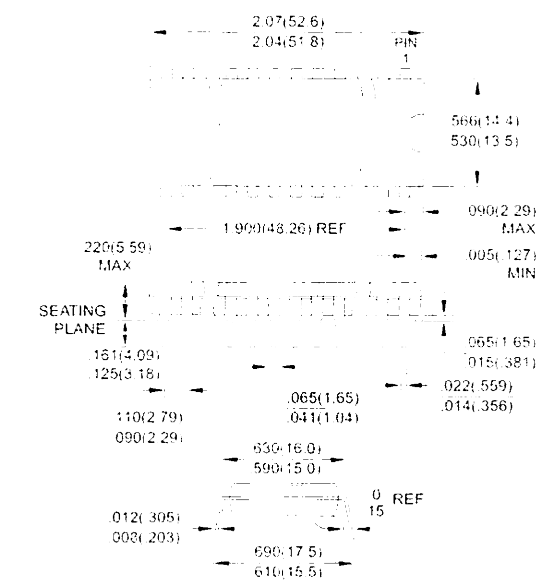
Dimensions in Inches and (Millimeters)

JEDEC STANDARD MS-018 AC



40P6, 40-lead, 0.600" Wide, Plastic Dual Inline Package (PDIP)

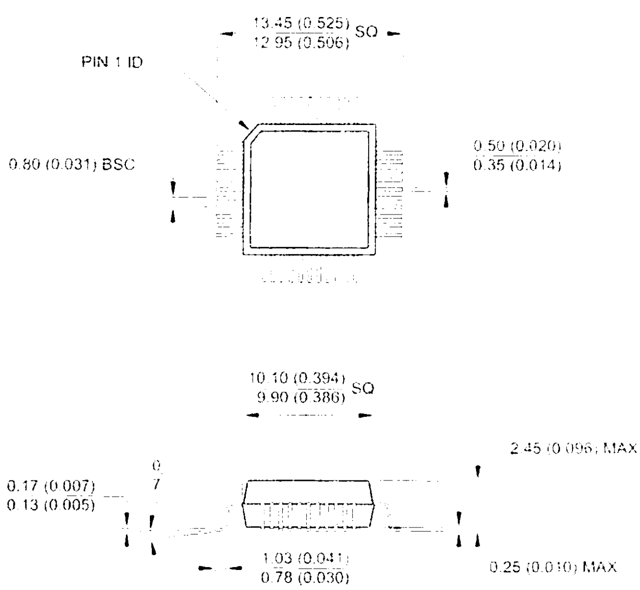
Dimensions in Inches and (Millimeters)



44Q, 44-lead, Plastic Quad Flat Package (PQFP)

Dimensions in Millimeters and (Inches)*

JEDEC STANDARD MS-022 AB



*Controlling dimension: millimeters

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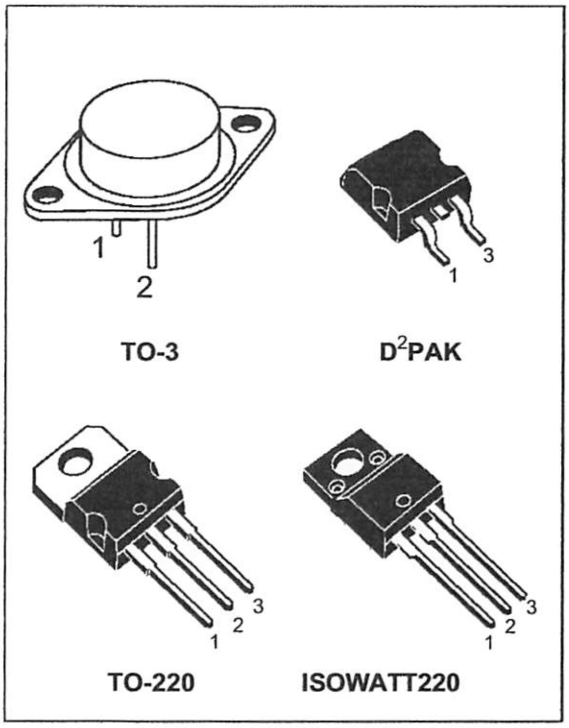
SGS-THOMSON MICROELECTRONICS

L7800 SERIES

POSITIVE VOLTAGE REGULATORS

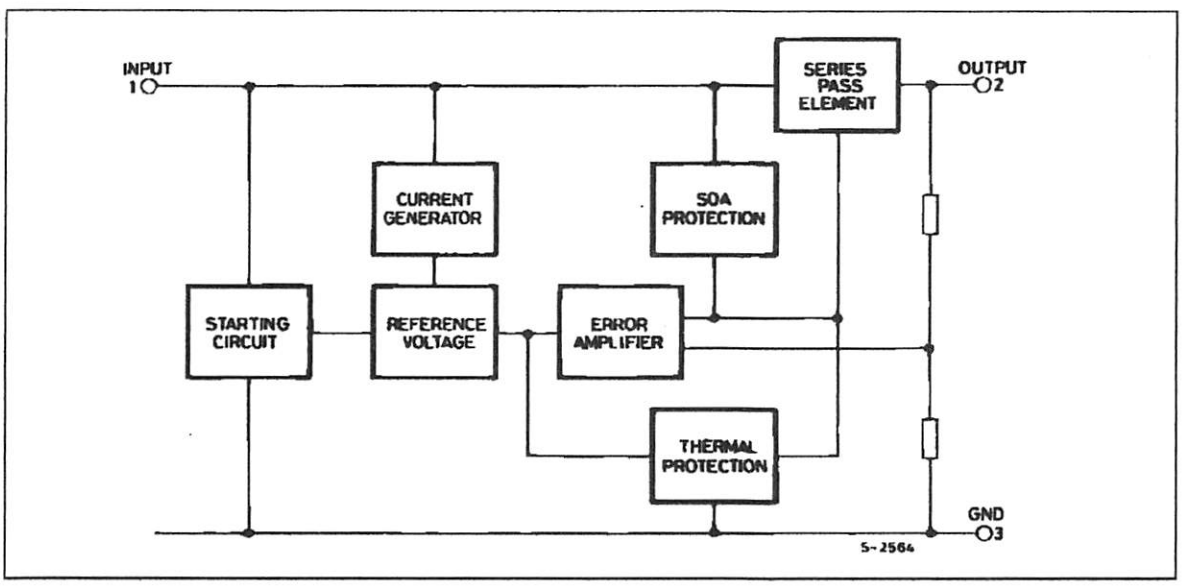
- OUTPUT CURRENT UP TO 1.5 A
- OUTPUT VOLTAGES OF 5; 5.2; 6; 8; 8.5; 9; 12; 15; 18; 24V
- THERMAL OVERLOAD PROTECTION
- SHORT CIRCUIT PROTECTION
- OUTPUT TRANSITION SOA PROTECTION



DESCRIPTION

The L7800 series of three-terminal positive regulators is available in TO-220 ISOWATT220 TO-3 and D^{2}PAK packages and several fixed output voltages, making it useful in a wide range of applications. These regulators can provide local on-card regulation, eliminating the distribution problems associated with single point regulation. Each type employs internal current limiting, thermal shut-down and safe area protection, making it essentially indestructible. If adequate heat sinking is provided, they can deliver over 1A output current. Although designed primarily as fixed voltage regulators, these devices can be used with external components to obtain adjustable voltages and currents.

BLOCK DIAGRAM



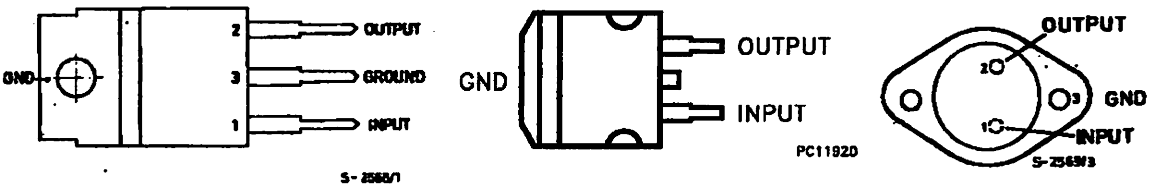
ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_i	DC Input Voltage (for V_O = 5 to 18V) (for V_O = 20, 24V)	35 40	V V
I_o	Output Current	Internally limited	
P_{tot}	Power Dissipation	Internally limited	
T_{op}	Operating Junction Temperature Range (for **L7800**) (for **L7800C**)	- 55 to 125 0 to 150	°C °C
T_{stg}	Storage Temperature Range	- 40 to 150	°C

THERMAL DATA

Symbol	Parameter		D^2PAK	TO-220	ISOWATT220	TO-3	Unit
$R_{thj-case}$	Thermal Resistance Junction-case	Max	3	3	4	4	°C/W
$R_{thj-amb}$	Thermal Resistance Junction-ambient	Max	62.5	50	60	35	°C/W

CONNECTION DIAGRAM AND ORDERING NUMBERS (top view)

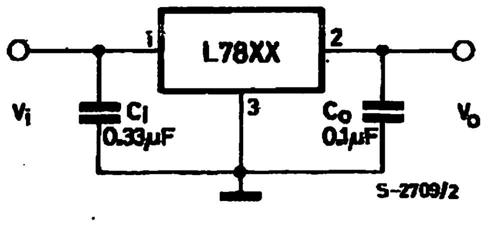


TO-220 & ISOWATT220 | D^2PAK | TO-3

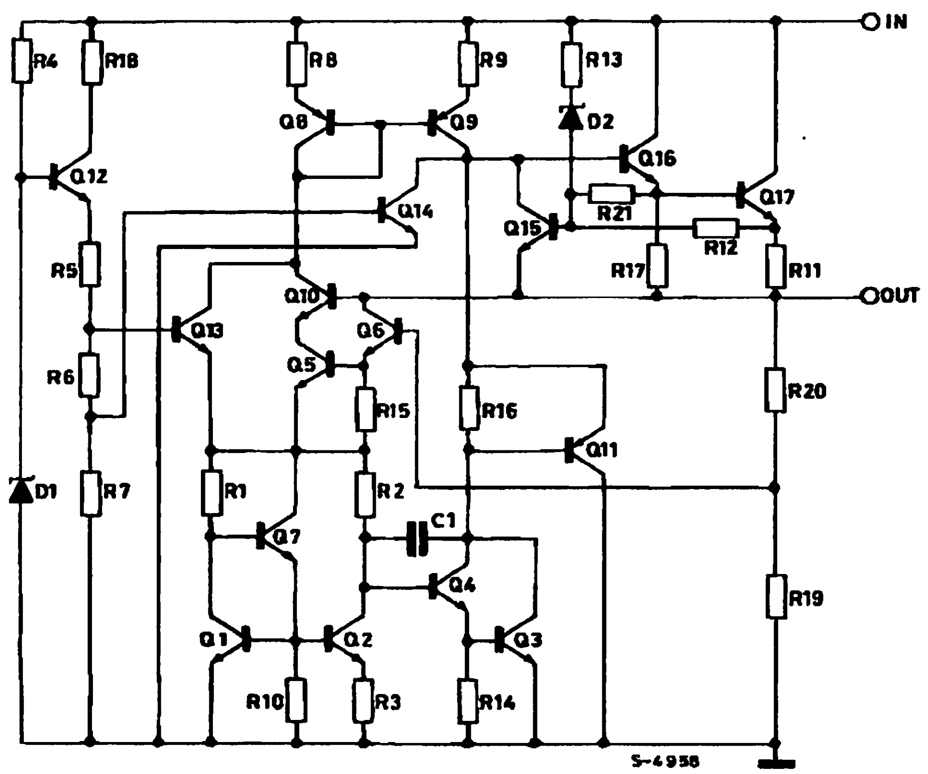
Type	TO-220	D^2PAK (*)	ISOWATT220	TO-3	Output Voltage
L7805				L7805T	5V
L7805C	L7805CV	L7805CD2T	L7805CP	L7805CT	5V
L7852C	L7852CV	L7852CD2T	L7852CP	L7852CT	5.2V
L7806				L7806T	6V
L7806C	L7806CV	L7806CD2T	L7806CP	L7806CT	6V
L7808				L7808T	8V
L7808C	L7808CV	L7808CD2T	L7808CP	L7808CT	8V
L7885C	L7885CV	L7885CD2T	L7885CP	L7885CT	8.5V
L7809C	L7809CV	L7809CD2T	L7809CP	L7809CT	9V
L7812				L7812T	12V
L7812C	L7812CV	L7812CD2T	L7812CP	L7812CT	12V
L7815				L7815T	15V
L7815C	L7815CV	L7815CD2T	L7815CP	L7815CT	15V
L7818				L7818T	18V
L7818C	L7818CV	L7818CD2T	L7818CP	L7818CT	18V
L7820				L7820T	20V
L7820C	L7820CV	L7820CD2T	L7820CP	L7820CT	20V
L7824				L7824T	24V
L7824C	L7824CV	L7824CD2T	L7824CP	L7824CT	24V

(*) AVAILABLE IN TAPE AND REEL WITH "-TR" SUFFIX

APPLICATION CIRCUIT



SCHEMATIC DIAGRAM



TEST CIRCUITS

Figure 1 : DC Parameter

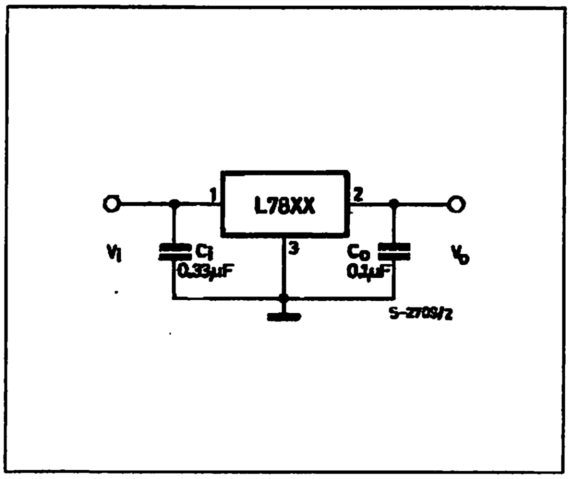


Figure 2 : Load Regulation.

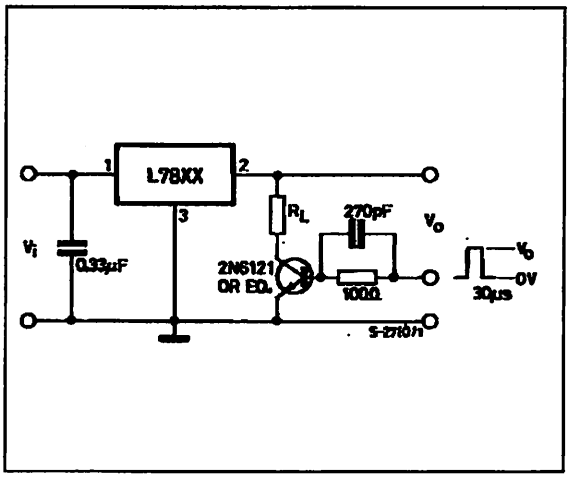
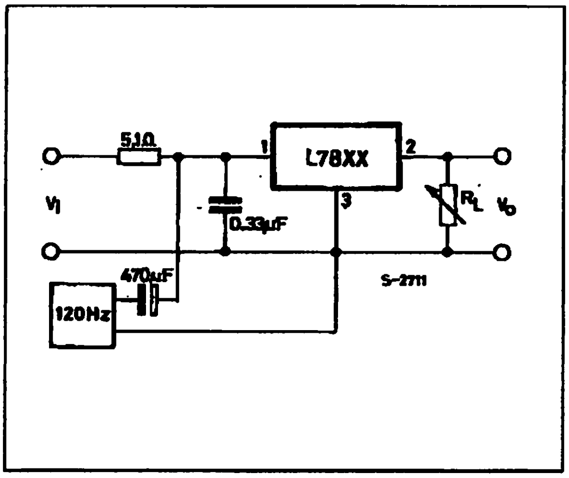


Figure 3 : Ripple Rejection.



ELECTRICAL CHARACTERISTICS FOR L7805 (refer to the test circuits, T_j = -55 to 150 °C, V_i = 10V, I_o = 500 mA, C_i = 0.33 µF, C_o = 0.1 µF unless otherwise specified)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
V_o	Output Voltage	T_j = 25 °C	4.8	5	5.2	V
V_o	Output Voltage	I_o = 5 mA to 1 A $P_o \leq$ 15 W V_i = 8 to 20 V	4.65	5	5.35	V
ΔV_o*	Line Regulation	V_i = 7 to 25 V T_j = 25 °C V_i = 8 to 12 V T_j = 25 °C		3 1	50 25	mV mV
ΔV_o*	Load Regulation	I_o = 5 to 1500 mA T_j = 25 °C I_o = 250 to 750 mA T_j = 25 °C			100 25	mV mV
I_d	Quiescent Current	T_j = 25 °C			6	mA
ΔI_d	Quiescent Current Change	I_o = 5 to 1000 mA			0.5	mA
ΔI_d	Quiescent Current Change	V_i = 8 to 25 V			0.8	mA
$\frac{\Delta V_o}{\Delta T}$	Output Voltage Drift	I_o = 5 mA		0.6		mV/°C
eN	Output Noise Voltage	B = 10Hz to 100KHz T_j = 25 °C			40	µV/V_o
SVR	Supply Voltage Rejection	V_i = 8 to 18 V f = 120 Hz	68			dB
V_d	Dropout Voltage	I_o = 1 A T_j = 25 °C		2	2.5	V
R_o	Output Resistance	f = 1 KHz		17		mΩ
I_{sc}	Short Circuit Current	V_i = 35 V T_j = 25 °C		0.75	1.2	A
I_{scp}	Short Circuit Peak Current	T_j = 25 °C	1.3	2.2	3.3	A

ELECTRICAL CHARACTERISTICS FOR L7806 (refer to the test circuits, T_j = -55 to 150 °C, V_i = 15V, I_o = 500 mA, C_i = 0.33 µF, C_o = 0.1 µF unless otherwise specified)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
V_o	Output Voltage	T_j = 25 °C	5.75	6	6.25	V
V_o	Output Voltage	I_o = 5 mA to 1 A $P_o \leq$ 15 W V_i = 9 to 21 V	5.65	6	6.35	V
ΔV_o*	Line Regulation	V_i = 8 to 25 V T_j = 25 °C V_i = 9 to 13 V T_j = 25 °C			60 30	mV mV
ΔV_o*	Load Regulation	I_o = 5 to 1500 mA T_j = 25 °C I_o = 250 to 750 mA T_j = 25 °C			100 30	mV mV
I_d	Quiescent Current	T_j = 25 °C			6	mA
ΔI_d	Quiescent Current Change	I_o = 5 to 1000 mA			0.5	mA
ΔI_d	Quiescent Current Change	V_i = 9 to 25 V			0.8	mA
$\frac{\Delta V_o}{\Delta T}$	Output Voltage Drift	I_o = 5 mA		0.7		mV/°C
eN	Output Noise Voltage	B = 10Hz to 100KHz T_j = 25 °C			40	µV/V_o
SVR	Supply Voltage Rejection	V_i = 9 to 19 V f = 120 Hz	65			dB
V_d	Dropout Voltage	I_o = 1 A T_j = 25 °C		2	2.5	V
R_o	Output Resistance	f = 1 KHz		19		mΩ
I_{sc}	Short Circuit Current	V_i = 35 V T_j = 25 °C		0.75	1.2	A
I_{scp}	Short Circuit Peak Current	T_j = 25 °C	1.3	2.2	3.3	A

* Load and line regulation are specified at constant junction temperature. Changes in V_o due to heating effects must be taken into account separately. Pulce testing with low duty cycle is used.

ELECTRICAL CHARACTERISTICS FOR L7808 (refer to the test circuits, T_j = -55 to 150 °C. V_i = 14V, I_o = 500 mA, C_i = 0.33 µF, C_o = 0.1 µF unless otherwise specified)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
V_o	Output Voltage	T_j = 25 °C	7.7	8	8.3	V
V_o	Output Voltage	I_o = 5 mA to 1 A $P_o \leq$ 15 W V_i = 11.5 to 23 V	7.6	8	8.4	V
ΔV_o*	Line Regulation	V_i = 10.5 to 25 V T_j = 25 °C V_i = 11 to 17 V T_j = 25 °C			80 40	mV mV
ΔV_o*	Load Regulation	I_o = 5 to 1500 mA T_j = 25 °C I_o = 250 to 750 mA T_j = 25 °C			100 40	mV mV
I_d	Quiescent Current	T_j = 25 °C			6	mA
ΔI_d	Quiescent Current Change	I_o = 5 to 1000 mA			0.5	mA
ΔI_d	Quiescent Current Change	V_i = 11.5 to 25 V			0.8	mA
$\frac{\Delta V_o}{\Delta T}$	Output Voltage Drift	I_o = 5 mA		1		mV/°C
eN	Output Noise Voltage	B = 10Hz to 100KHz T_j = 25 °C			40	µV/V_O
SVR	Supply Voltage Rejection	V_i = 11.5 to 21.5 V f = 120 Hz	62			dB
V_d	Dropout Voltage	I_o = 1 A T_j = 25 °C		2	2.5	V
R_o	Output Resistance	f = 1 KHz		16		mΩ
I_{sc}	Short Circuit Current	V_i = 35 V T_j = 25 °C		0.75	1.2	A
I_{scp}	Short Circuit Peak Current	T_j = 25 °C	1.3	2.2	3.3	A

ELECTRICAL CHARACTERISTICS FOR L7812 (refer to the test circuits, T_j = -55 to 150 °C, V_i = 19V, I_o = 500 mA, C_i = 0.33 µF, C_o = 0.1 µF unless otherwise specified)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
V_o	Output Voltage	T_j = 25 °C	11.5	12	12.5	V
V_o	Output Voltage	I_o = 5 mA to 1 A $P_o \leq$ 15 W V_i = 15.5 to 27 V	11.4	12	12.6	V
ΔV_o*	Line Regulation	V_i = 14.5 to 30 V T_j = 25 °C V_i = 16 to 22 V T_j = 25 °C			120 60	mV mV
ΔV_o*	Load Regulation	I_o = 5 to 1500 mA T_j = 25 °C I_o = 250 to 750 mA T_j = 25 °C			100 60	mV mV
I_d	Quiescent Current	T_j = 25 °C			6	mA
ΔI_d	Quiescent Current Change	I_o = 5 to 1000 mA			0.5	mA
ΔI_d	Quiescent Current Change	V_i = 15 to 30 V			0.8	mA
$\frac{\Delta V_o}{\Delta T}$	Output Voltage Drift	I_o = 5 mA		1.5		mV/°C
eN	Output Noise Voltage	B = 10Hz to 100KHz T_j = 25 °C			40	µV/V_O
SVR	Supply Voltage Rejection	V_i = 15 to 25 V f = 120 Hz	61			dB
V_d	Dropout Voltage	I_o = 1 A T_j = 25 °C		2	2.5	V
R_o	Output Resistance	f = 1 KHz		18		mΩ
I_{sc}	Short Circuit Current	V_i = 35 V T_j = 25 °C		0.75	1.2	A
I_{scp}	Short Circuit Peak Current	T_j = 25 °C	1.3	2.2	3.3	A

* Load and line regulation are specified at constant junction temperature. Changes in V_o due to heating effects must be taken into account separately. Pulce testing with low duty cycle is used.

ELECTRICAL CHARACTERISTICS FOR L7815 (refer to the test circuits, T_j = -55 to 150 °C, V_i = 23V, I_o = 500 mA, C_i = 0.33 µF, C_o = 0.1 µF unless otherwise specified)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
V_o	Output Voltage	T_j = 25 °C	14.4	15	15.6	V
V_o	Output Voltage	I_o = 5 mA to 1 A $P_o \leq$ 15 W V_i = 18.5 to 30 V	14.25	15	15.75	V
ΔV_o*	Line Regulation	V_i = 17.5 to 30 V T_j = 25 °C V_i = 20 to 26 V T_j = 25 °C			150 75	mV mV
ΔV_o*	Load Regulation	I_o = 5 to 1500 mA T_j = 25 °C I_o = 250 to 750 mA T_j = 25 °C			150 75	mV mV
I_d	Quiescent Current	T_j = 25 °C			6	mA
ΔI_d	Quiescent Current Change	I_o = 5 to 1000 mA			0.5	mA
ΔI_d	Quiescent Current Change	V_i = 18.5 to 30 V			0.8	mA
$\frac{\Delta V_o}{\Delta T}$	Output Voltage Drift	I_o = 5 mA		1.8		mV/°C
eN	Output Noise Voltage	B = 10Hz to 100KHz T_j = 25 °C			40	µV/V_O
SVR	Supply Voltage Rejection	V_i = 18.5 to 28.5 V f = 120 Hz	60			dB
V_d	Dropout Voltage	I_o = 1 A T_j = 25 °C		2	2.5	V
R_o	Output Resistance	f = 1 KHz		19		mΩ
I_{sc}	Short Circuit Current	V_i = 35 V T_j = 25 °C		0.75	1.2	A
I_{scp}	Short Circuit Peak Current	T_j = 25 °C	1.3	2.2	3.3	A

ELECTRICAL CHARACTERISTICS FOR L7818 (refer to the test circuits, T_j = -55 to 150 °C, V_i = 26V, I_o = 500 mA, C_i = 0.33 µF, C_o = 0.1 µF unless otherwise specified)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
V_o	Output Voltage	T_j = 25 °C	17.3	18	18.7	V
V_o	Output Voltage	I_o = 5 mA to 1 A $P_o \leq$ 15 W V_i = 22 to 33 V	17.1	18	18.9	V
ΔV_o*	Line Regulation	V_i = 21 to 33 V T_j = 25 °C V_i = 24 to 30 V T_j = 25 °C			180 90	mV mV
ΔV_o*	Load Regulation	I_o = 5 to 1500 mA T_j = 25 °C I_o = 250 to 750 mA T_j = 25 °C			180 90	mV mV
I_d	Quiescent Current	T_j = 25 °C			6	mA
ΔI_d	Quiescent Current Change	I_o = 5 to 1000 mA			0.5	mA
ΔI_d	Quiescent Current Change	V_i = 22 to 33 V			0.8	mA
$\frac{\Delta V_o}{\Delta T}$	Output Voltage Drift	I_o = 5 mA		2.3		mV/°C
eN	Output Noise Voltage	B = 10Hz to 100KHz T_j = 25 °C			40	µV/V_O
SVR	Supply Voltage Rejection	V_i = 22 to 32 V f = 120 Hz	59			dB
V_d	Dropout Voltage	I_o = 1 A T_j = 25 °C		2	2.5	V
R_o	Output Resistance	f = 1 KHz		22		mΩ
I_{sc}	Short Circuit Current	V_i = 35 V T_j = 25 °C		0.75	1.2	A
I_{scp}	Short Circuit Peak Current	T_j = 25 °C	1.3	2.2	3.3	A

* Load and line regulation are specified at constant junction temperature. Changes in V_o due to heating effects must be taken into account separately. Pulce testing with low duty cycle is used.

ELECTRICAL CHARACTERISTICS FOR L7820 (refer to the test circuits, T_j = -55 to 150 °C, V_i = 28V, I_o = 500 mA, C_i = 0.33 µF, C_o = 0.1 µF unless otherwise specified)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
V_o	Output Voltage	T_j = 25 °C	19.2	20	20.8	V
V_o	Output Voltage	I_o = 5 mA to 1 A $P_o \leq$ 15 W V_i = 24 to 35 V	19	20	21	V
ΔV_o*	Line Regulation	V_i = 22.5 to 35 V T_j = 25 °C V_i = 26 to 32 V T_j = 25 °C			200 100	mV mV
ΔV_o*	Load Regulation	I_o = 5 to 1500 mA T_j = 25 °C I_o = 250 to 750 mA T_j = 25 °C			200 100	mV mV
I_d	Quiescent Current	T_j = 25 °C			6	mA
ΔI_d	Quiescent Current Change	I_o = 5 to 1000 mA			0.5	mA
ΔI_d	Quiescent Current Change	V_i = 24 to 35 V			0.8	mA
$\frac{\Delta V_o}{\Delta T}$	Output Voltage Drift	I_o = 5 mA		2.5		mV/°C
eN	Output Noise Voltage	B = 10Hz to 100KHz T_j = 25 °C			40	µV/V_O
SVR	Supply Voltage Rejection	V_i = 24 to 35 V f = 120 Hz	58			dB
V_d	Dropout Voltage	I_o = 1 A T_j = 25 °C		2	2.5	V
R_o	Output Resistance	f = 1 KHz		24		mΩ
I_{sc}	Short Circuit Current	V_i = 35 V T_j = 25 °C		0.75	1.2	A
I_{scp}	Short Circuit Peak Current	T_j = 25 °C	1.3	2.2	3.3	A

ELECTRICAL CHARACTERISTICS FOR L7824 (refer to the test circuits, T_j = -55 to 150 °C, V_i = 33V, I_o = 500 mA, C_i = 0.33 µF, C_o = 0.1 µF unless otherwise specified)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
V_o	Output Voltage	T_j = 25 °C	23	24	25	V
V_o	Output Voltage	I_o = 5 mA to 1 A $P_o \leq$ 15 W V_i = 28 to 38 V	22.8	24	25.2	V
ΔV_o*	Line Regulation	V_i = 27 to 38 V T_j = 25 °C V_i = 30 to 36 V T_j = 25 °C			240 120	mV mV
ΔV_o*	Load Regulation	I_o = 5 to 1500 mA T_j = 25 °C I_o = 250 to 750 mA T_j = 25 °C			240 120	mV mV
I_d	Quiescent Current	T_j = 25 °C			6	mA
ΔI_d	Quiescent Current Change	I_o = 5 to 1000 mA			0.5	mA
ΔI_d	Quiescent Current Change	V_i = 28 to 38 V			0.8	mA
$\frac{\Delta V_o}{\Delta T}$	Output Voltage Drift	I_o = 5 mA		3		mV/°C
eN	Output Noise Voltage	B = 10Hz to 100KHz T_j = 25 °C			40	µV/V_O
SVR	Supply Voltage Rejection	V_i = 28 to 38 V f = 120 Hz	56			dB
V_d	Dropout Voltage	I_o = 1 A T_j = 25 °C		2	2.5	V
R_o	Output Resistance	f = 1 KHz		28		mΩ
I_{sc}	Short Circuit Current	V_i = 35 V T_j = 25 °C		0.75	1.2	A
I_{scp}	Short Circuit Peak Current	T_j = 25 °C	1.3	2.2	3.3	A

* Load and line regulation are specified at constant junction temperature. Changes in V_o due to heating effects must be taken into account separately. Pulce testing with low duty cycle is used.

ELECTRICAL CHARACTERISTICS FOR L7805C (refer to the test circuits, T_j = 0 to 125 °C, V_i = 10V, I_o = 500 mA, C_i = 0.33 µF, C_o = 0.1 µF unless otherwise specified)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
V_o	Output Voltage	T_j = 25 °C	4.8	5	5.2	V
V_o	Output Voltage	I_o = 5 mA to 1 A $P_o \leq$ 15 W V_i = 7 to 20 V	4.75	5	5.25	V
ΔV_o*	Line Regulation	V_i = 7 to 25 V T_j = 25 °C V_i = 8 to 12 V T_j = 25 °C		3 1	100 50	mV mV
ΔV_o*	Load Regulation	I_o = 5 to 1500 mA T_j = 25 °C I_o = 250 to 750 mA T_j = 25 °C			100 50	mV mV
I_d	Quiescent Current	T_j = 25 °C			8	mA
ΔI_d	Quiescent Current Change	I_o = 5 to 1000 mA			0.5	mA
ΔI_d	Quiescent Current Change	V_i = 7 to 25 V			0.8	mA
$\frac{\Delta V_o}{\Delta T}$	Output Voltage Drift	I_o = 5 mA		-1.1		mV/°C
eN	Output Noise Voltage	B = 10Hz to 100KHz T_j = 25 °C		40		µV
SVR	Supply Voltage Rejection	V_i = 8 to 18 V f = 120 Hz	62			dB
V_d	Dropout Voltage	I_o = 1 A T_j = 25 °C		2		V
R_o	Output Resistance	f = 1 KHz		17		mΩ
I_{sc}	Short Circuit Current	V_i = 35 V T_j = 25 °C		750		mA
I_{scp}	Short Circuit Peak Current	T_j = 25 °C		2.2		A

ELECTRICAL CHARACTERISTICS FOR L7852C (refer to the test circuits, T_j = 0 to 125 °C, V_i = 10V, I_o = 500 mA, C_i = 0.33 µF, C_o = 0.1 µF unless otherwise specified)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
V_o	Output Voltage	T_j = 25 °C	5.0	5.2	5.4	V
V_o	Output Voltage	I_o = 5 mA to 1 A $P_o \leq$ 15 W V_i = 8 to 20 V	4.95	5.2	5.45	V
ΔV_o*	Line Regulation	V_i = 7 to 25 V T_j = 25 °C V_i = 8 to 12 V T_j = 25 °C		3 1	105 52	mV mV
ΔV_o*	Load Regulation	I_o = 5 to 1500 mA T_j = 25 °C I_o = 250 to 750 mA T_j = 25 °C			105 52	mV mV
I_d	Quiescent Current	T_j = 25 °C			8	mA
ΔI_d	Quiescent Current Change	I_o = 5 to 1000 mA			0.5	mA
ΔI_d	Quiescent Current Change	V_i = 7 to 25 V			1.3	mA
$\frac{\Delta V_o}{\Delta T}$	Output Voltage Drift	I_o = 5 mA		-1.0		mV/°C
eN	Output Noise Voltage	B = 10Hz to 100KHz T_j = 25 °C		42		µV
SVR	Supply Voltage Rejection	V_i = 8 to 18 V f = 120 Hz	61			dB
V_d	Dropout Voltage	I_o = 1 A T_j = 25 °C		2		V
R_o	Output Resistance	f = 1 KHz		17		mΩ
I_{sc}	Short Circuit Current	V_i = 35 V T_j = 25 °C		750		mA
I_{scp}	Short Circuit Peak Current	T_j = 25 °C		2.2		A

* Load and line regulation are specified at constant junction temperature. Changes in V_o due to heating effects must be taken into account separately. Pulce testing with low duty cycle is used.

ELECTRICAL CHARACTERISTICS FOR L7806C (refer to the test circuits, T_j = 0 to 125 °C, V_i = 11V, I_o = 500 mA, C_i = 0.33 µF, C_o = 0.1 µF unless otherwise specified)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
V_o	Output Voltage	T_j = 25 °C	5.75	6	6.25	V
V_o	Output Voltage	I_o = 5 mA to 1 A $P_o \leq$ 15 W V_i = 8 to 21 V	5.7	6	6.3	V
ΔV_o*	Line Regulation	V_i = 8 to 25 V T_j = 25 °C V_i = 9 to 13 V T_j = 25 °C			120 60	mV mV
ΔV_o*	Load Regulation	I_o = 5 to 1500 mA T_j = 25 °C I_o = 250 to 750 mA T_j = 25 °C			120 60	mV mV
I_d	Quiescent Current	T_j = 25 °C			8	mA
ΔI_d	Quiescent Current Change	I_o = 5 to 1000 mA			0.5	mA
ΔI_d	Quiescent Current Change	V_i = 8 to 25 V			1.3	mA
$\frac{\Delta V_o}{\Delta T}$	Output Voltage Drift	I_o = 5 mA		-0.8		mV/°C
eN	Output Noise Voltage	B = 10Hz to 100KHz T_j = 25 °C		45		µV
SVR	Supply Voltage Rejection	V_i = 9 to 19 V f = 120 Hz	59			dB
V_d	Dropout Voltage	I_o = 1 A T_j = 25 °C		2		V
R_o	Output Resistance	f = 1 KHz		19		mΩ
I_{sc}	Short Circuit Current	V_i = 35 V T_j = 25 °C		550		mA
I_{scp}	Short Circuit Peak Current	T_j = 25 °C		2.2		A

ELECTRICAL CHARACTERISTICS FOR L7808C (refer to the test circuits, T_j = 0 to 125 °C, V_i = 14V, I_o = 500 mA, C_i = 0.33 µF, C_o = 0.1 µF unless otherwise specified)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
V_o	Output Voltage	T_j = 25 °C	7.7	8	8.3	V
V_o	Output Voltage	I_o = 5 mA to 1 A $P_o \leq$ 15 W V_i = 10.5 to 25 V	7.6	8	8.4	V
ΔV_o*	Line Regulation	V_i = 10.5 to 25 V T_j = 25 °C V_i = 11 to 17 V T_j = 25 °C			160 80	mV mV
ΔV_o*	Load Regulation	I_o = 5 to 1500 mA T_j = 25 °C I_o = 250 to 750 mA T_j = 25 °C			160 80	mV mV
I_d	Quiescent Current	T_j = 25 °C			8	mA
ΔI_d	Quiescent Current Change	I_o = 5 to 1000 mA			0.5	mA
ΔI_d	Quiescent Current Change	V_i = 10.5 to 25 V			1	mA
$\frac{\Delta V_o}{\Delta T}$	Output Voltage Drift	I_o = 5 mA		-0.8		mV/°C
eN	Output Noise Voltage	B = 10Hz to 100KHz T_j = 25 °C		52		µV
SVR	Supply Voltage Rejection	V_i = 11.5 to 21.5 V f = 120 Hz	56			dB
V_d	Dropout Voltage	I_o = 1 A T_j = 25 °C		2		V
R_o	Output Resistance	f = 1 KHz		16		mΩ
I_{sc}	Short Circuit Current	V_i = 35 V T_j = 25 °C		450		mA
I_{scp}	Short Circuit Peak Current	T_j = 25 °C		2.2		A

* Load and line regulation are specified at constant junction temperature. Changes in V_o due to heating effects must be taken into account separately. Pulce testing with low duty cycle is used.

ELECTRICAL CHARACTERISTICS FOR L7885C (refer to the test circuits, T_j = 0 to 125 °C, V_i = 14.5V, I_o = 500 mA, C_i = 0.33 µF, C_o = 0.1 µF unless otherwise specified)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
V_o	Output Voltage	T_j = 25 °C	8.2	8.5	8.8	V
V_o	Output Voltage	I_o = 5 mA to 1 A $P_o \leq$ 15 W V_i = 11 to 26 V	8.1	8.5	8.9	V
ΔV_o*	Line Regulation	V_i = 11 to 27 V T_j = 25 °C V_i = 11.5 to 17.5 V T_j = 25 °C			160 80	mV mV
ΔV_o*	Load Regulation	I_o = 5 to 1500 mA T_j = 25 °C I_o = 250 to 750 mA T_j = 25 °C			160 80	mV mV
I_d	Quiescent Current	T_j = 25 °C			8	mA
ΔI_d	Quiescent Current Change	I_o = 5 to 1000 mA			0.5	mA
ΔI_d	Quiescent Current Change	V_i = 11 to 27 V			1	mA
$\frac{\Delta V_o}{\Delta T}$	Output Voltage Drift	I_o = 5 mA		-0.8		mV/°C
eN	Output Noise Voltage	B = 10Hz to 100KHz T_j = 25 °C		55		µV
SVR	Supply Voltage Rejection	V_i = 12 to 22 V f = 120 Hz	56			dB
V_d	Dropout Voltage	I_o = 1 A T_j = 25 °C		2		V
R_o	Output Resistance	f = 1 KHz		16		mΩ
I_{sc}	Short Circuit Current	V_i = 35 V T_j = 25 °C		450		mA
I_{scp}	Short Circuit Peak Current	T_j = 25 °C		2.2		A

ELECTRICAL CHARACTERISTICS FOR L7809C (refer to the test circuits, T_j = 0 to 125 °C, V_i = 15V, I_o = 500 mA, C_i = 0.33 µF, C_o = 0.1 µF unless otherwise specified)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
V_o	Output Voltage	T_j = 25 °C	8.65	9	9.35	V
V_o	Output Voltage	I_o = 5 mA to 1 A $P_o \leq$ 15 W V_i = 11.5 to 26 V	8.55	9	9.45	V
ΔV_o*	Line Regulation	V_i = 11.5 to 26 V T_j = 25 °C V_i = 12 to 18 V T_j = 25 °C			180 90	mV mV
ΔV_o*	Load Regulation	I_o = 5 to 1500 mA T_j = 25 °C I_o = 250 to 750 mA T_j = 25 °C			180 90	mV mV
I_d	Quiescent Current	T_j = 25 °C			8	mA
ΔI_d	Quiescent Current Change	I_o = 5 to 1000 mA			0.5	mA
ΔI_d	Quiescent Current Change	V_i = 11.5 to 26 V			1	mA
$\frac{\Delta V_o}{\Delta T}$	Output Voltage Drift	I_o = 5 mA		-1.0		mV/°C
eN	Output Noise Voltage	B = 10Hz to 100KHz T_j = 25 °C		70		µV
SVR	Supply Voltage Rejection	V_i = 12 to 23 V f = 120 Hz	55			dB
V_d	Dropout Voltage	I_o = 1 A T_j = 25 °C		2		V
R_o	Output Resistance	f = 1 KHz		17		mΩ
I_{sc}	Short Circuit Current	V_i = 35 V T_j = 25 °C		400		mA
I_{scp}	Short Circuit Peak Current	T_j = 25 °C		2.2		A

* Load and line regulation are specified at constant junction temperature. Changes in V_o due to heating effects must be taken into account separately. Pulce testing with low duty cycle is used.

ELECTRICAL CHARACTERISTICS FOR L7812C (refer to the test circuits, T_j = 0 to 125 °C, V_i = 19V, I_o = 500 mA, C_i = 0.33 µF, C_o = 0.1 µF unless otherwise specified)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
V_o	Output Voltage	T_j = 25 °C	11.5	12	12.5	V
V_o	Output Voltage	I_o = 5 mA to 1 A $P_o \leq$ 15 W V_i = 14.5 to 27 V	11.4	12	12.6	V
ΔV_o*	Line Regulation	V_i = 14.5 to 30 V T_j = 25 °C V_i = 16 to 22 V T_j = 25 °C			240 120	mV mV
ΔV_o*	Load Regulation	I_o = 5 to 1500 mA T_j = 25 °C I_o = 250 to 750 mA T_j = 25 °C			240 120	mV mV
I_d	Quiescent Current	T_j = 25 °C			8	mA
ΔI_d	Quiescent Current Change	I_o = 5 to 1000 mA			0.5	mA
ΔI_d	Quiescent Current Change	V_i = 14.5 to 30 V			1	mA
$\frac{\Delta V_o}{\Delta T}$	Output Voltage Drift	I_o = 5 mA		-1		mV/°C
eN	Output Noise Voltage	B = 10Hz to 100KHz T_j = 25 °C		75		µV
SVR	Supply Voltage Rejection	V_i = 15 to 25 V f = 120 Hz	55			dB
V_d	Dropout Voltage	I_o = 1 A T_j = 25 °C		2		V
R_o	Output Resistance	f = 1 KHz		18		mΩ
I_{sc}	Short Circuit Current	V_i = 35 V T_j = 25 °C		350		mA
I_{scp}	Short Circuit Peak Current	T_j = 25 °C		2.2		A

ELECTRICAL CHARACTERISTICS FOR L7815C (refer to the test circuits, T_j = 0 to 125 °C, V_i = 23V, I_o = 500 mA, C_i = 0.33 µF, C_o = 0.1 µF unless otherwise specified)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
V_o	Output Voltage	T_j = 25 °C	14.4	15	15.6	V
V_o	Output Voltage	I_o = 5 mA to 1 A $P_o \leq$ 15 W V_i = 17.5 to 30 V	14.25	15	15.75	V
ΔV_o*	Line Regulation	V_i = 17.5 to 30 V T_j = 25 °C V_i = 20 to 26 V T_j = 25 °C			300 150	mV mV
ΔV_o*	Load Regulation	I_o = 5 to 1500 mA T_j = 25 °C I_o = 250 to 750 mA T_j = 25 °C			300 150	mV mV
I_d	Quiescent Current	T_j = 25 °C			8	mA
ΔI_d	Quiescent Current Change	I_o = 5 to 1000 mA			0.5	mA
ΔI_d	Quiescent Current Change	V_i = 17.5 to 30 V			1	mA
$\frac{\Delta V_o}{\Delta T}$	Output Voltage Drift	I_o = 5 mA		-1		mV/°C
eN	Output Noise Voltage	B = 10Hz to 100KHz T_j = 25 °C		90		µV
SVR	Supply Voltage Rejection	V_i = 18.5 to 28.5 V f = 120 Hz	54			dB
V_d	Dropout Voltage	I_o = 1 A T_j = 25 °C		2		V
R_o	Output Resistance	f = 1 KHz		19		mΩ
I_{sc}	Short Circuit Current	V_i = 35 V T_j = 25 °C		230		mA
I_{scp}	Short Circuit Peak Current	T_j = 25 °C		2.1		A

* Load and line regulation are specified at constant junction temperature. Changes in V_o due to heating effects must be taken into account separately. Pulce testing with low duty cycle is used.

ELECTRICAL CHARACTERISTICS FOR L7818C (refer to the test circuits, T_j = 0 to 125 °C, V_i = 26V, I_o = 500 mA, C_i = 0.33 µF, C_o = 0.1 µF unless otherwise specified)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
V_o	Output Voltage	T_j = 25 °C	17.3	18	18.7	V
V_o	Output Voltage	I_o = 5 mA to 1 A $P_o \leq$ 15 W V_i = 21 to 33 V	17.1	18	18.9	V
ΔV_o*	Line Regulation	V_i = 21 to 33 V T_j = 25 °C V_i = 24 to 30 V T_j = 25 °C			360 180	mV mV
ΔV_o*	Load Regulation	I_o = 5 to 1500 mA T_j = 25 °C I_o = 250 to 750 mA T_j = 25 °C			360 180	mV mV
I_d	Quiescent Current	T_j = 25 °C			8	mA
ΔI_d	Quiescent Current Change	I_o = 5 to 1000 mA			0.5	mA
ΔI_d	Quiescent Current Change	V_i = 21 to 33 V			1	mA
$\frac{\Delta V_o}{\Delta T}$	Output Voltage Drift	I_o = 5 mA		-1		mV/°C
eN	Output Noise Voltage	B = 10Hz to 100KHz T_j = 25 °C		110		µV
SVR	Supply Voltage Rejection	V_i = 22 to 32 V f = 120 Hz	53			dB
V_d	Dropout Voltage	I_o = 1 A T_j = 25 °C		2		V
R_o	Output Resistance	f = 1 KHz		22		mΩ
I_{sc}	Short Circuit Current	V_i = 35 V T_j = 25 °C		200		mA
I_{scp}	Short Circuit Peak Current	T_j = 25 °C		2.1		A

ELECTRICAL CHARACTERISTICS FOR L7820C (refer to the test circuits, T_j = 0 to 125 °C, V_i = 28V, I_o = 500 mA, C_i = 0.33 µF, C_o = 0.1 µF unless otherwise specified)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
V_o	Output Voltage	T_j = 25 °C	19.2	20	20.8	V
V_o	Output Voltage	I_o = 5 mA to 1 A $P_o \leq$ 15 W V_i = 23 to 35 V	19	20	21	V
ΔV_o*	Line Regulation	V_i = 22.5 to 35 V T_j = 25 °C V_i = 26 to 32 V T_j = 25 °C			400 200	mV mV
ΔV_o*	Load Regulation	I_o = 5 to 1500 mA T_j = 25 °C I_o = 250 to 750 mA T_j = 25 °C			400 200	mV mV
I_d	Quiescent Current	T_j = 25 °C			8	mA
ΔI_d	Quiescent Current Change	I_o = 5 to 1000 mA			0.5	mA
ΔI_d	Quiescent Current Change	V_i = 23 to 35 V			1	mA
$\frac{\Delta V_o}{\Delta T}$	Output Voltage Drift	I_o = 5 mA		-1		mV/°C
eN	Output Noise Voltage	B = 10Hz to 100KHz T_j = 25 °C		150		µV
SVR	Supply Voltage Rejection	V_i = 24 to 35 V f = 120 Hz	52			dB
V_d	Dropout Voltage	I_o = 1 A T_j = 25 °C		2		V
R_o	Output Resistance	f = 1 KHz		24		mΩ
I_{sc}	Short Circuit Current	V_i = 35 V T_j = 25 °C		180		mA
I_{scp}	Short Circuit Peak Current	T_j = 25 °C		2.1		A

* Load and line regulation are specified at constant junction temperature. Changes in V_o due to heating effects must be taken into account separately. Pulce testing with low duty cycle is used.

ELECTRICAL CHARACTERISTICS FOR L7824C (refer to the test circuits, T_j = 0 to 125 °C, V_i = 33V, I_o = 500 mA, C_i = 0.33 μF, C_o = 0.1 μF unless otherwise specified)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
V_o	Output Voltage	T_j = 25 °C	23	24	25	V
V_o	Output Voltage	I_o = 5 mA to 1 A $P_o \leq$ 15 W V_i = 27 to 38 V	22.8	24	25.2	V
ΔV_o*	Line Regulation	V_i = 27 to 38 V T_j = 25 °C V_i = 30 to 36 V T_j = 25 °C			480 240	mV mV
ΔV_o*	Load Regulation	I_o = 5 to 1500 mA T_j = 25 °C I_o = 250 to 750 mA T_j = 25 °C			480 240	mV mV
I_d	Quiescent Current	T_j = 25 °C			8	mA
ΔI_d	Quiescent Current Change	I_o = 5 to 1000 mA			0.5	mA
ΔI_d	Quiescent Current Change	V_i = 27 to 38 V			1	mA
$\frac{\Delta V_o}{\Delta T}$	Output Voltage Drift	I_o = 5 mA		-1.5		mV/°C
eN	Output Noise Voltage	B = 10Hz to 100KHz T_j = 25 °C		170		μV
SVR	Supply Voltage Rejection	V_i = 28 to 38 V f = 120 Hz	50			dB
V_d	Dropout Voltage	I_o = 1 A T_j = 25 °C		2		V
R_o	Output Resistance	f = 1 KHz		28		mΩ
I_{sc}	Short Circuit Current	V_i = 35 V T_j = 25 °C		150		mA
I_{scp}	Short Circuit Peak Current	T_j = 25 °C		2.1		A

* Load and line regulation are specified at constant junction temperature. Changes in V_o due to heating effects must be taken into account separately. Pulce testing with low duty cycle is used.

Figure 4 : Dropout Voltage vs. Junction Temperature.

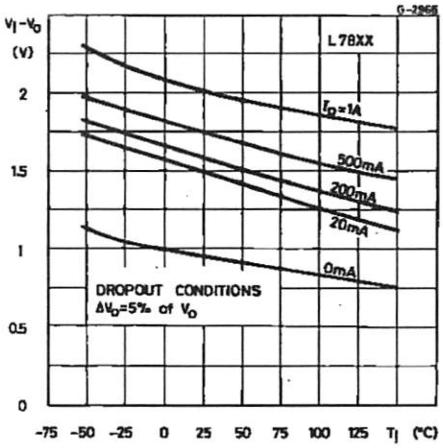


Figure 5 : Peak Output Current vs. Input/output Differential Voltage.

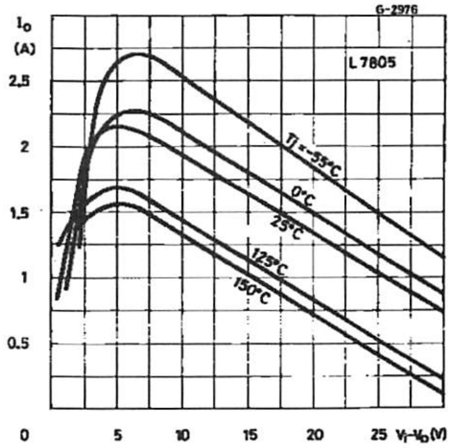


Figure 6 : Supply Voltage Rejection vs. Frequency.

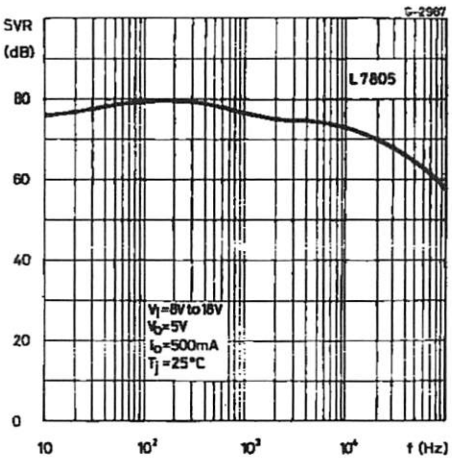


Figure 7 : Output Voltage vs. Junction Temperature.

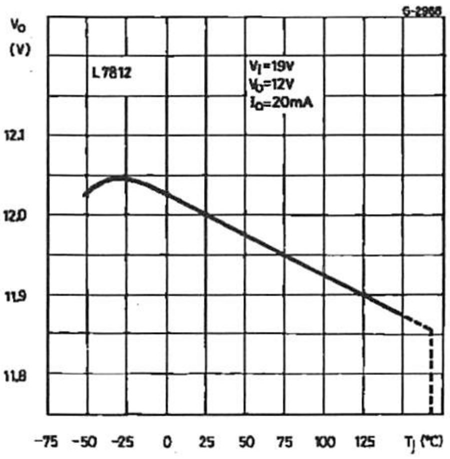


Figure 8 : Output Impedance vs. Frequency.

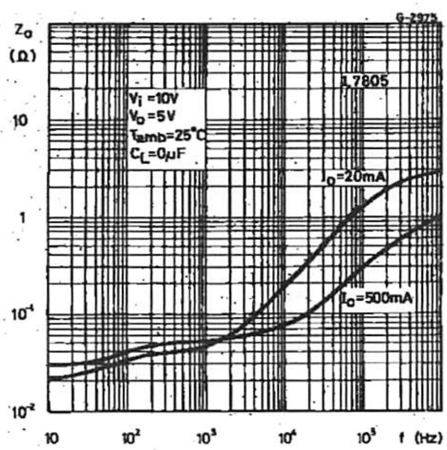


Figure 9 : Quiescent Current vs. Junction Temperature.

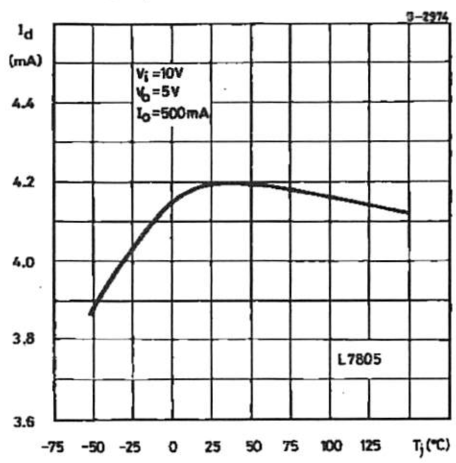


Figure 10 : Load Transient Response.

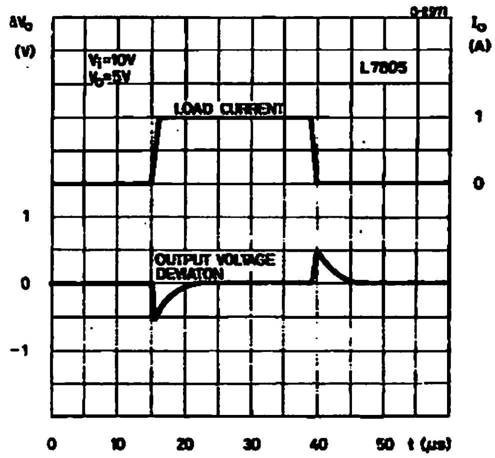


Figure 11 : Line Transient Response.

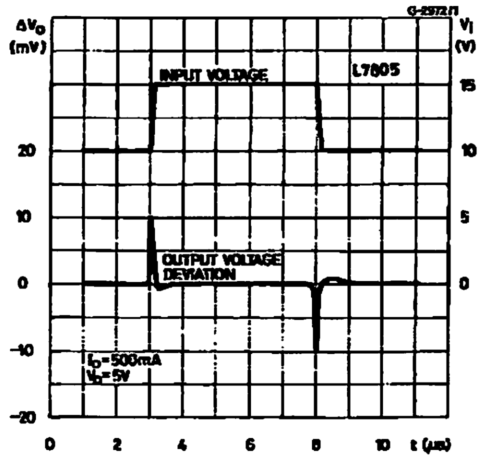


Figure 12 : Quiescent Current vs. Input Voltage.

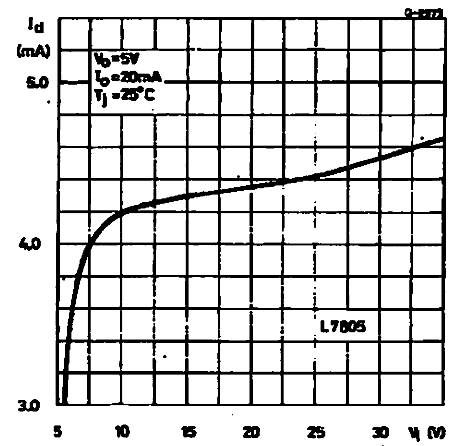


Figure 13 : Fixed Output Regulator.

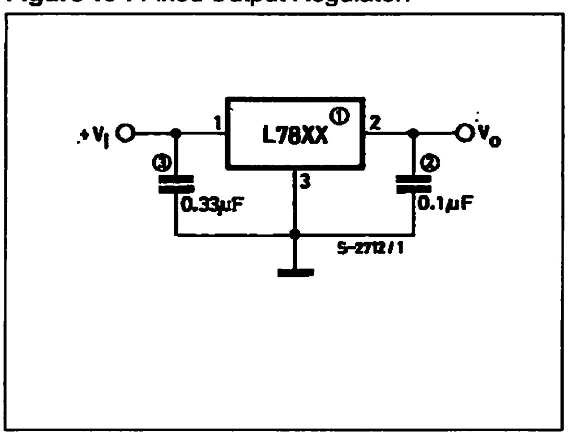
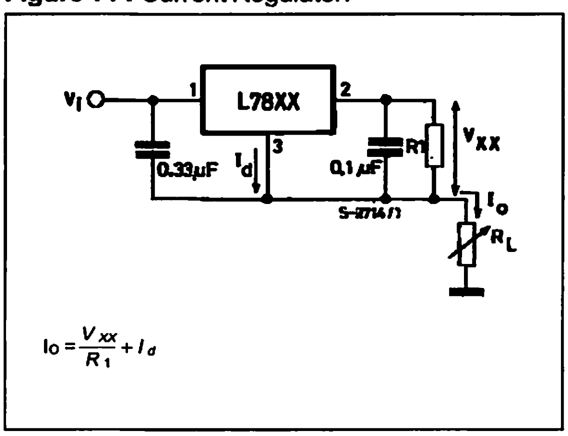


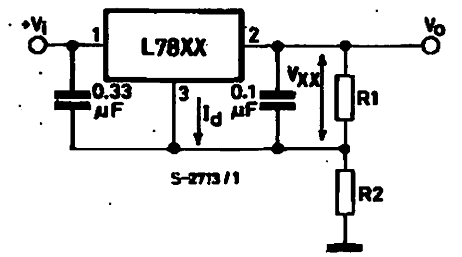
Figure 14 : Current Regulator.



NOTE:

1. To specify an output voltage, substitute voltage value for "XX".
2. Although no output capacitor is need for stability, it does improve transient response.
3. Required if cregulator is locate an appreciable distance from power supply filter.

Figure 15 : Circuit for Increasing Output Voltage.



$I_{R1} \geq 5\, I_d$

$V_O = V_{XX}(1 + \frac{R_2}{R_1}) + I_d R_2$

Figure 16 : Adjustable Output Regulator (7 to 30V).

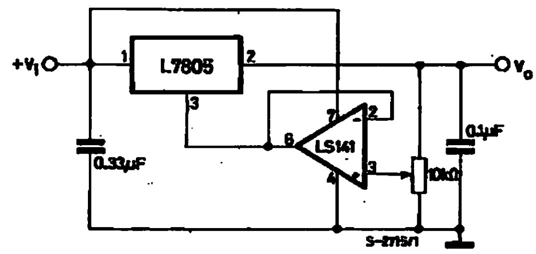
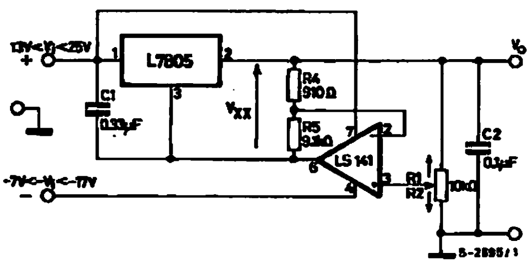
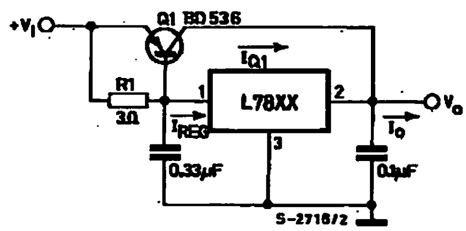


Figure 17 : 0.5 to 10V Regulator.



$VO = V_{XX}\frac{R_4}{R_1}$

Figure 18 : High Current Voltage Regulator.



$R_1 = \frac{V_{BEQ1}}{I_{REQ} - \frac{I_{Q1}}{\beta_{Q1}}}$

$I_O = I_{REG} + Q_1 (I_{REG} - \frac{V_{BEQ}}{R_1})$

Figure 19 : High Output Current with Short Circuit Protection.

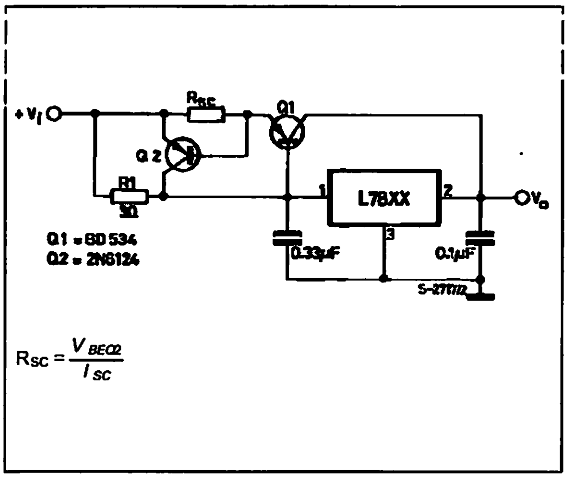


Figure 20 : Tracking Voltage Regulator

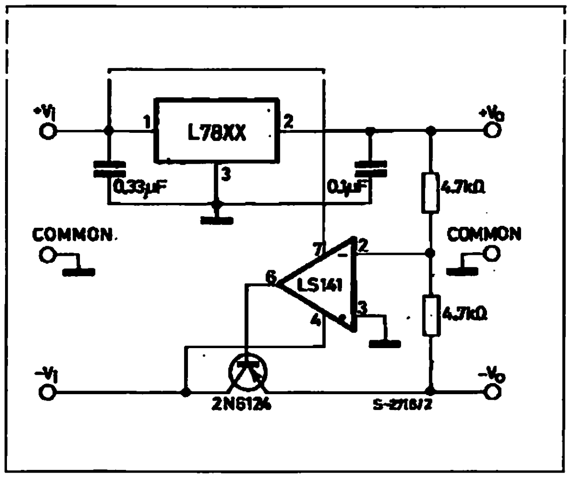
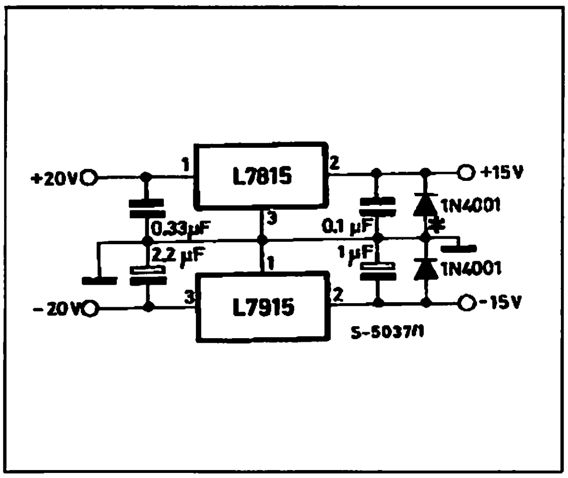


Figure 21 : Split Power Supply (± 15V – 1A).



* Against potential latch-up problems.

Figure 22 : Negative Output Voltage Circuit.

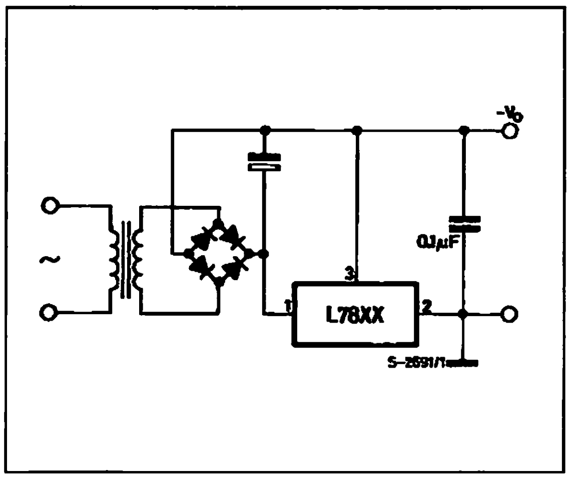


Figure 23 : Switching Regulator.

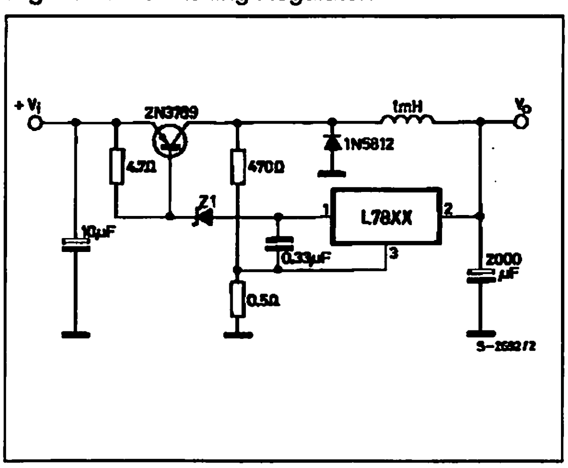


Figure 24 : High Input Voltage Circuit.

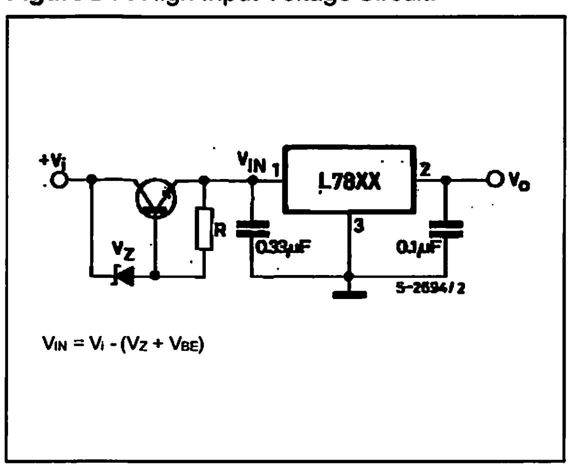


Figure 25 : High Input Voltage Circuit.

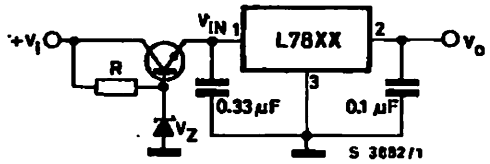


Figure 26 : High Output Voltage Regulator.

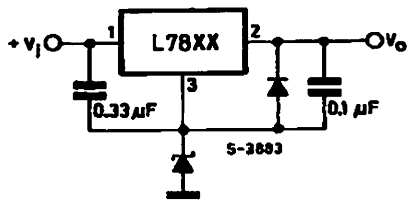
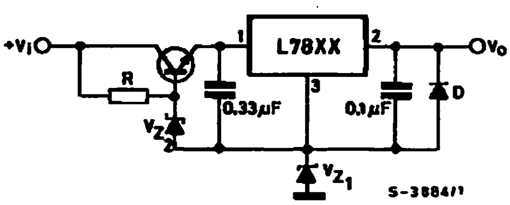
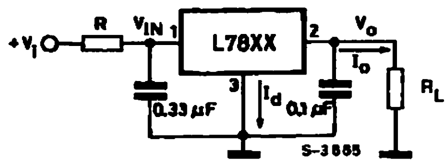


Figure 27 : High Input and Output Voltage.



$V_O = V_{XX} + V_{Z1}$

Figure 28 : Reducing Power Dissipation with Dropping Resistor.



$$R = \frac{V_{I(min)} - V_{XX} - V_{DROP(max)}}{I_{Q(max)} + I_{d(max)}}$$

Figure 29 : Remote Shutdown.

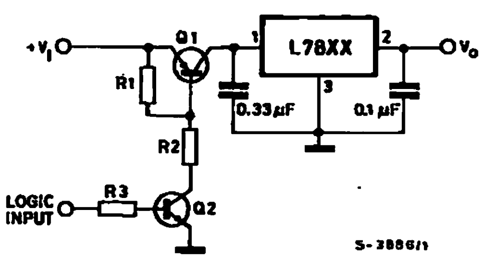
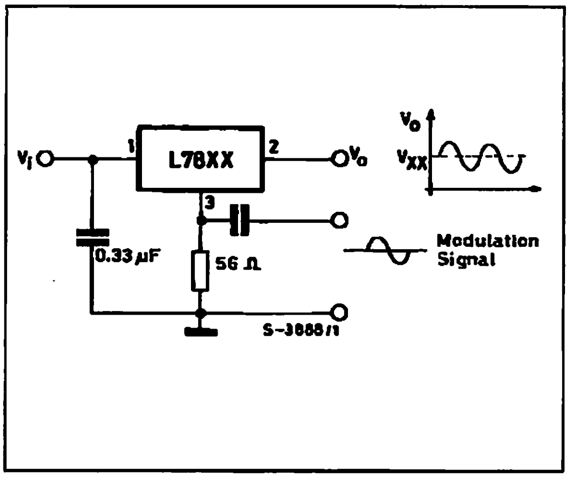
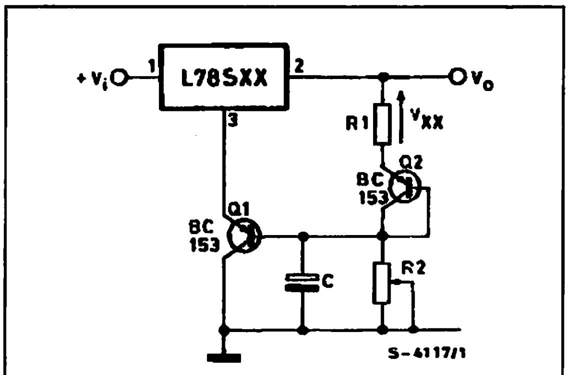


Figure 30 : Power AM Modulator (unity voltage gain, $I_o < 1A$).



NOTE: The circuit performs well up to 100KHz

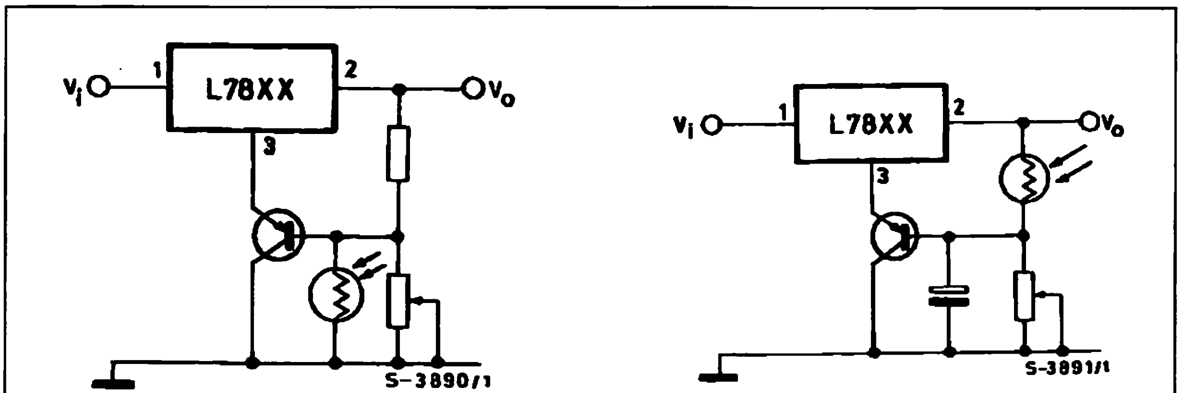
Figure 31 : Adjustable Output Voltage with Temperature Compensation.



$$V_O = V_{XX}\left(1 + \frac{R_2}{R_1}\right) + V_{BE}$$

NOTE: Q_2 is connected as a diode in order to compensate the variation of the Q_1 V_{BE} with the temperature. C allows a slow rise-time of the V_o

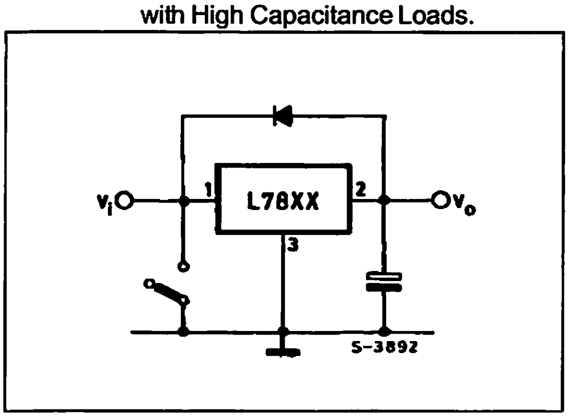
Figure 32 : Light Controllers ($V_{O\,min} = V_{XX} + V_{BE}$).



Vo falls when the light goes up

Vo rises when the light goes up

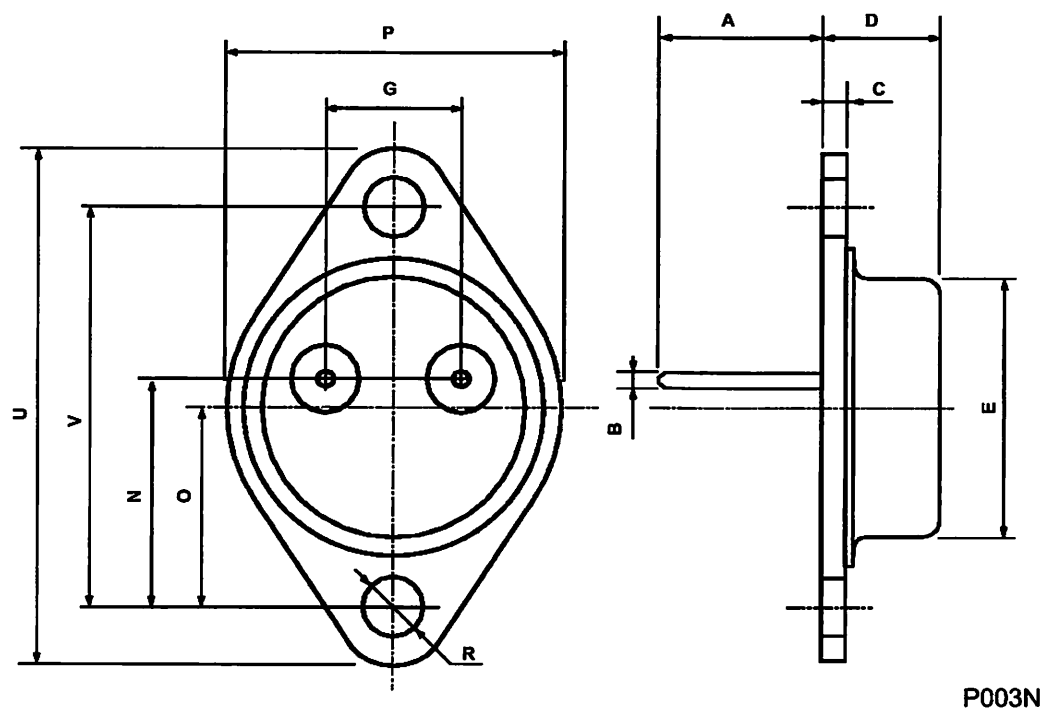
Figure 33 : Protection against Input Short-circuit with High Capacitance Loads.



Application with high capacitance loads and an output voltage greater than 6 volts need an external diode (see fig. 33) to protect the deviceagainst input short circuit. In this case the input voltage falls rapidly while the output voltage decrease slowly. The capacitance dischrges by means of the Base-Emitter junction of the series pass transistor in the regulator. If the energy is sufficently high, the transistor may be destroyed. The external diode by-passes the current from the IC to ground.

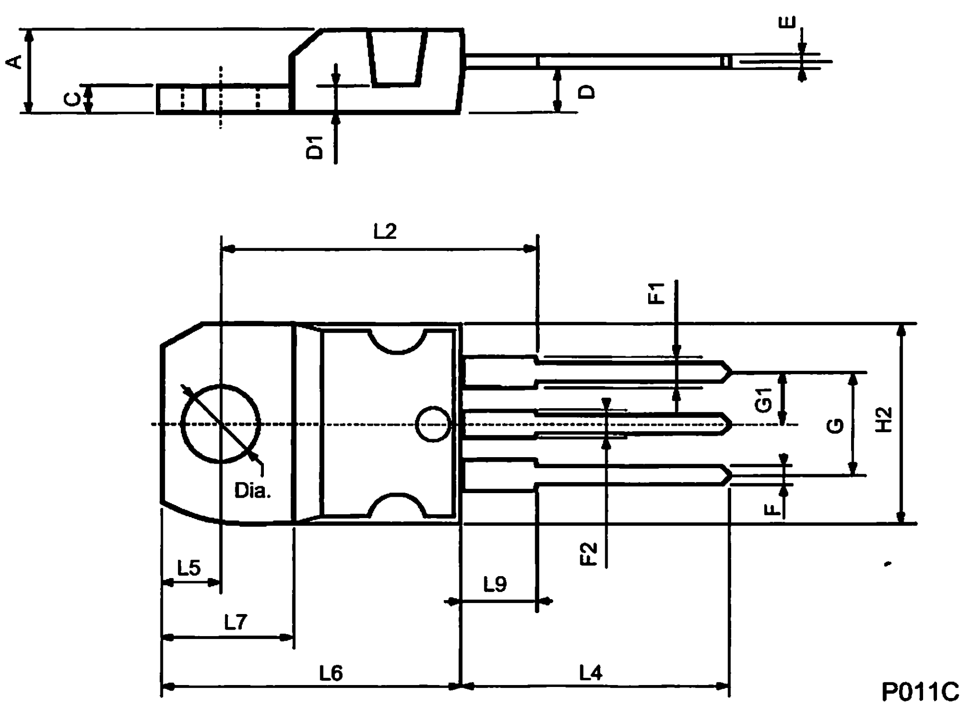
TO-3 (R) MECHANICAL DATA

DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A		11.7			0.460	
B	0.96		1.10	0.037		0.043
C			1.70			0.066
D			8.7			0.342
E			20.0			0.787
G		10.9			0.429	
N		16.9			0.665	
P			26.2			1.031
R	3.88		4.09	0.152		0.161
U			39.50			1.555
V		30.10			1.185	



TO-220 MECHANICAL DATA

DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A	4.40		4.60	0.173		0.181
C	1.23		1.32	0.048		0.051
D	2.40		2.72	0.094		0.107
D1		1.27			0.050	
E	0.49		0.70	0.019		0.027
F	0.61		0.88	0.024		0.034
F1	1.14		1.70	0.044		0.067
F2	1.14		1.70	0.044		0.067
G	4.95		5.15	0.194		0.203
G1	2.4		2.7	0.094		0.106
H2	10.0		10.40	0.393		0.409
L2		16.4			0.645	
L4	13.0		14.0	0.511		0.551
L5	2.65		2.95	0.104		0.116
L6	15.25		15.75	0.600		0.620
L7	6.2		6.6	0.244		0.260
L9	3.5		3.93	0.137		0.154
DIA.	3.75		3.85	0.147		0.151



ISOWATT220 MECHANICAL DATA

DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A	4.4		4.6	0.173		0.181
B	2.5		2.7	0.098		0.106
D	2.5		2.75	0.098		0.108
E	0.4		0.7	0.015		0.027
F	0.75		1	0.030		0.039
F1	1.15		1.7	0.045		0.067
F2	1.15		1.7	0.045		0.067
G	4.95		5.2	0.195		0.204
G1	2.4		2.7	0.094		0.106
H	10		10.4	0.393		0.409
L2		16			0.630	
L3	28.6		30.6	1.126		1.204
L4	9.8		10.6	0.385		0.417
L6	15.9		16.4	0.626		0.645
L7	9		9.3	0.354		0.366
Ø	3		3.2	0.118		0.126