PERANCANGAN DAN PEMBUATAN SISTEM PERINGATAN DINI TEHADAP BAHAYA KECEPATAN ANGIN DAN PENDETEKSI ARAH ANGIN PADA JEMBATAN SURAMADU BERBASISKAN MIKROKONTROLLER AT 89S8252

SKRIPSI

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FEBRUARI 2010

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PERANCANGAN DAN PEMBUATAN SISTEM PERINGATAN DINI TERHADAP BAHAYA KECEPATAN ANGIN DAN PENDETEKSI ARAH ANGIN PADA JEMBATAN SURAMADU BERBASISKAN MIKROKONTROLLER AT 89S8252

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PERANCANGAN DAN PEMBUATAN SISTEM PERINGATAN DINI TERHADAP BAHAYA KECEPATAN ANGIN DAN PENDETEKSI ARAH ANGIN PADA JEMBATAN SURAMADU BERBASIS MIKROKONTROLLER AT89S8252

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ABSTRAKSI

Kemajuan teknologi terutama dibidang elektronika, mendorong manusia untuk membuat peralatan elektronika tepat guna yang dapat dimanfaatkan dalam berbagai sendi kehidupan, misalnya pembuatan alat pendeteksi arah dan kecepatan angin yang berfungsi untuk peringatan dini terhadap bahaya kecepatan dan arah angin.

Penggunaan optocoupler sendiri sebagai pembaca kecepatan dan arah angin, trefick led berfungsi seperti halnya lampu lalu lintas yang ada dijalan jika berwarna hijau berarti diperbolehkan lewat jika berwarna kuning berarti hati-hati dan jika berwarna merah maka berhenti, fungsi portal sebagai penutup jikalau kondisi angin pada jembatan tidak memungkinkan untuk dilalui dan trefick led akan menyala merah.

Kata kunci: Mikrokontroller, Optocoupler, Portal, Trafick led.

KATA PENGANTAR

Dengan memanjatkan puji syukur kehadirat Allah SWT, atas limpahan Rahmat dan Hidayah-Nya, sehingga penyusun dapat menyelesaikan skripsi ini dengan judul : **" PERANCANGAN DAN PEMBUATAN SISTEM PERINGATAN DINI TERHADAP BAHAYA KECEPATAN ANGIN DAN PENDETEKSI ARAH ANGIN PADA JEMBATAN SURAMADU BERBASISKAN MIKROKONTROLLER AT89S8252 "**

Skripsi ini disusun sebagai salah satu persyaratan dalam menyelesaikan studi program strata satu (S-1) Jurusan Teknik Elektro/Konsentrasi Teknik Elektronika, Fakultas Teknologi Industri, Institut Teknologi Nasional Malang.

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8. Seluruh Dosen pengajar di Jurusan Teknik Elektronika atas segala ilmu, pengetahuan, dan pengalaman yang telah diberikan dan diajarkan
9. Teman-teman angkatan 2003 atas dukungan moril, bantuan, dan saran-saran
10. Semua pihak yang terlibat langsung maupun tidak langsung yang telah membantu terwujudnya skripsi ini.

Akhirnya penulis tidak lupa mohon maaf yang sebesar-besarnya bila dalam penulisan skripsi ini masih terdapat kesalahan baik sengaja maupun tidak disengaja. Dan akhirnya semoga skripsi ini dapat bermanfaat bagi semua pihak.

Malang, Feberuari 2010

Penulis

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Malang, Februari 2010

Penulis

DAFTAR ISI

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BAB 1
PENDAHULUAN

1.1 Latar Belakang

Di dalam perkembangannya, mikrokontroller banyak diterapkan dalam perancangan elektronika karena mikrokontroller memiliki sistem pengaturan dan pengontrolan yang otomatis dan praktis. Keefektifan mikrokontroller inilah yang diperlukan manusia dalam menunjang rutinitas, baik dalam proses produksi maupun dalam kehidupan sehari – hari pada umumnya. Seperti sistem peringatan dini bahaya kecepatan angin dan pendeteksi arah angin pada jembatan suramadu. Hal ini dimaksudkan agar pengguna jembatan terhindar dari kecelakaaan.

Pada kondisi sekarang ini kenyataannya begitu ironis seiring dengan meningkatnya pemanasan global maka akan mempengaruhi kondisi iklim yang semakain hari semakin tidak menentu, hal ini mengakibatkan sering kali terjadi kecelakaan yang disebabkan oleh faktor cuaca salah satunya faktor angin.

Untuk mengantisipasi kemungkinan terjadinya kejadian diatas salah satu cara yang menjadi alternatif adalah dengan memanfaatkan instrumen elekronika dengan perancangan tertentu. Maka alat ini diharapkan sangat membantu untuk menghindari kecelakaan pada jembatan suramdu sebagai alat peringatan dini terhadap bahaya kecepatan dan pendeteksi arah angin

1.2 Rumusan Masalah

Dalam perancangan dan pembuatan sistem peringatan dini terhadap bahaya kecepatan angin dan pendeteksi arah angin pada jembatan suramadu, maka permasalahannya adalah:

1. Bagaimana merancang dan pembuatan perangkat keras dalam metode ini
2. Bagaimana merancang dan pembuatan perangkat lunak atau *software* pada mikrokontoller yang mengadalikan semua kerja sistem

1.3 Batasan Masalah

Agar pembahasan perancanagan dan pembuatan sistem peringatan dini terhadap bahaya kecepatan angin dan pendeteksi arah angin pada jembatan suramadu berbasiskan mikrokontroller AT89S8252 maka diperlukan adanya batasan-batasan dalam pembahasannya yaitu :

1. Mikrokontroller yang digunakan AT89S8252.
2. Tidak membahas *power supply.*
3. Tidak membahas panjang kabel serial yang digunakan.
4. Tidak membahas konstruksi jembatan yang digunakan.
5. Tidak Membahas RS 485 terlalu meluas.

1.4 Tujuan

Adapun tujuan dari pembuatan alat ini adalah untuk menciptakan suatu alat yang dapat memonitoring kecepatan angin pada jembatan suramadu dan pendeteksi arah angin. Hal ini juga untuk mengurangi kecelakaan yang terjadi pada jembatan yang diakibatkan oleh faktor angin.

1.5 Metodologi Penulisan

Metode yang digunakan dalam penulisan tugas akhir ini adalah

1. Studi Pustaka

   Memperoleh data dengan cara membaca dan mempelajari buku literatur yang berhubungan dengan penyusunan skripsi ini.

2. Studi Lapangan

   Memperoleh data dengan cara praktek secara langsung untuk menunjang pembuatan alat.

3. Pengolahan Data

   Mengolah data dengan jalan membuat analisa dan menarik kesimpulan dari hasil pengujian yang ada.

1.6 Sistematika Pembahasan

Sistematika pembahasan dari skripsi ini terdiri dari pokok pembahasan yang saling berkaitan antara satu dengan lainnya, yaitu :

BAB I Pendahuluan

Pada bab ini dibahas tentang latar belakang permasalahan, rumusan masalah, batasan masalah, sistematika pembahasan dari alat yang direncanakan.

BAB II Landasan Teori

Pada bab ini dibahas tentang teori-teori yang mendukung dalam perencanaan dan pembuatan alat ini yang meliputi rangkaian AT89S82

BAB III Perencanaan Dan Pembuatan Alat

Pada bab ini dibahas tentang perencanaan dan pembuatan keseluruhan sistem perangkat keras (*hardware*) dan perangkat lunak (*software*).

BAB IV Pengujian Alat

Pada bab ini dibahas tentang proses serta hasil dari pengujian alat, yang didasarkan oleh pengukuran-pengukuran dan percobaan.

BAB V Penutup

Pada bab ini akan disampaikan kesimpulan dari perencanaan dan pembuatan sistem ini.

BAB II

LANDASAN TEORI

Landasan teori sangat membantu untuk dapat memahami suatu sistem. Landasan teori juga dapat digunakan sebagai acuan di dalam merencanakan suatu sistem. Dengan pertimbangan hal-hal tersebut, maka landasan teori merupakan bagian yang harus dipahami untuk pembahasan lebih lanjut. Dalam landasan teori ini akan dibahas teori dasar yang berhubungan dengan alat

2.1. Alat Pemantau Kecepatan dan Arah Angin

Pada umumnya alat pemantau kecepatan dan arah angin, masih menggunakan mekanik manual, dengan menggunakan perhitungan mekanik yang langsung dapat dilihat dengan visual mata kita. Oleh karena itu visual pembacaan meteran kecepatan dapat diganti dengan elektronik

Pada prinsipnya menggunakan perhitungan *counter*. Pada sensor ini menggunakan sebuah piringan berlubang, dapat dilihat pada gambar 2.1, dimana untuk mendeteksi kecepatan, perubahan kecepatan gelap-terang berhubungan dengan komponen sensor *optocoupler*. *Optocoupler* akan mengirimkan suatu pulsa cacahan. Bila cahaya yang masuk pada sensor terhalang oleh piringan maka cahaya lampu akan dipilah-pilah sehingga akan menghasilkan pulsa berurutan.

Dalam alat ini kecepatan diubah kedalam tegangan. Pada sensor kecepatan angin ini menggunakan dan memanfaakan *counter* sebagai penghitung pulsa. Yaitu *counter* sebagai alat penyimpan data atau *lach* dan *optocoupler* sebagai pendeteksi. Secara lengkap fungsi dari masing-masing komponen adalah sebagai berikut :

1. *Otocoupler* digunakan sebagai komponen penghasil pulsa yang didapatkan dari putaran baling-baling.
2. *Counter* 1 merupakan penghitung pulsa yang dihasilkan *optocoupler*.

3. *Lach* merupakan merupakan tempat penyimpanan data sementara dari *counter* 1.
4. Jari-jari baling pada umumnya antara 20 cm – 60 cm, dimana nantinya dalam perhitungan panjang keliling baling-baling dapat diubah kesatuan meter atau Km.

Rumus pada perhitungan kecepatan ini adalah :

V angin = K. A/T,

Dimana :

A = Jumblah putaran baling-baling

K = keliling baling-baling

D = Diameter baling-baling

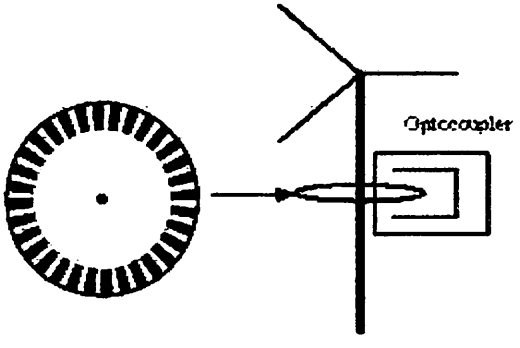
V = Kecpatan angin

T = Waktu dalam sekon

Contohnya jika baling-baling berputar sebanyak 10 kali dalam waktu 30 detik maka kecepatan angin pada waktu itu adalah, dengan asumsi gaya gesek poros dan massa baling-baling diabaikan sehingga didapatkan :

T = 30 detik,D = 20 cm, A = 10 kali, K = n x D = 3,14 x 40 cm = 1.256 m.

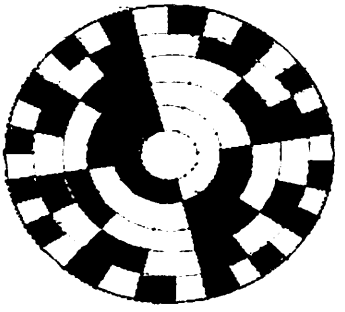
V angin= K.A/T = (1.256 x 10) / 30 = 4.18 m/detik.



Gambar 2.1 Piringan Mekanik gelap – terang

Sedangkan untuk menentukan arah angin secara elektronik terdapat bermacam-macam cara. Namun kebanyakan memiliki kerugian-kerugian, kerugian ini disebabkan oleh alat penggerak mekanik yang rumit, dapat digunakan piringan yang

dilubangi sesuai yang yang diinginkan, kemudian dikonversikan kedalam data digital, konversi itu dapat menggunakan kode biner atau menggunakan kode gray yang saling mengkonversi. Gambar piringan mekanik dapat dilihat pada gambar berikut.

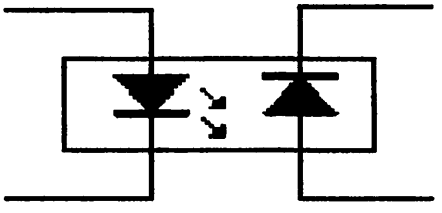


Gambar 2.2 Piringan Mekanik Arah Angin

2.2. Optocoupler.

Optocoupler (juga disebut optoisolator) merupakan sebuah divice yang memisahkan antara sumber eksitasi dan beban. Device ini terdiri dari sumber cahaya berupa LED pada sisi input dan photodiode pada sisi output. Dioda cahaya pemancar cahaya (LED) dan photodioda terpisah oleh celah pada optocoupler yang akan menghasilkan tegangan AC berupa pulsa.

Bentuk optocoupler yang dijual-belikan secara umum terdiri dari kotak plastic yang melindungi photodiode dan LED, seperti pada gambar di bawah.

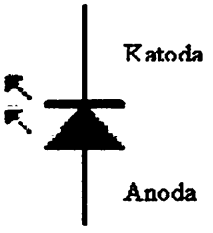


Gambar 2.3 Simbol *Optocuopler*

2.2.1. LED (*Light Emitting Diode*) Infra Red

LED infra red digunakan untuk menghasilkan sinar infra red. Prinsip kerjanya adalah, pada waktu *LED* infra red dibias foward, elektron dari pita konduksi melewati junction dan jatuh kedalamhole pita valensi, sehingga elektron-elektron tersebut memancarkan energi. Pada dioda penyearah biasa energi ini dikeluarkan sebagai

energi panas, tetapi pada *LED* infra red akan memancarkan cahaya yang tidak kelihatan, hal ini dapat dibenarkan dalam sistem tanda bahaya pencuri, penyampaian informasi rahasia dan ruang lingkup yang lain yang membutuhkan pancaran yang tidak tampak. Simbol *LED* infra red yang sering digunakan adalah :



Gambar 2.4 Simbol *LED* Infra Red

LED infra red merupakan PN junction yang memancarkan radiasi infra red yang tidak tampak oleh mata kita. Apabila pada anoda diberi tegangan positif dan katoda diberi ground, maka *LED* akan menjadi "ON" dan arus akan mengalir dari anoda ke katoda. Pada reaksi semikonduktor suatu dioda akan terjadi perpindahan elektron dari tipe N menuju tipe P dan berpindahnya hole dari tipe P ke tipe N. Proses rekombinasi antara elektron dengan *hole*, mengakibatkan pelepasan energi berupa cahaya.

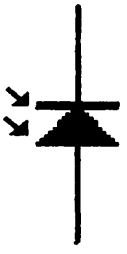
Pada *LED* infra red cahaya yang dipancarkan mempunyai panjang gelombang yang sangat kecil (0,1 mm – 1 μm), sehingga pancaran gelombang tidak tertangkap oleh manusia. Beberapa alasan dan keuntungan penggunaan spektrum infra red adalah

1. Pemancar infra red menggunakan tegangan yang kecil.
2. Mempunyai jangkauan yang cukup jauh.
3. Infra red dapat menembus kabut.
4. Tidakmengganggu pemakai udara untuk keperluan umum, sehingga tidak memerlukan ijin khusus.

2.2.2. Photo Dioda

Photo dioda ini memiliki sifat kebalikan dari *LED infra red* di atas, yang mana jenis dioda ini akan mengalirkan arus maju *forward,* saat dikenai cahaya *infra red*

padanya. Kuat arus yang mengalir juga tergantung dari kuatnya cahaya *infra red* yang jatuh pada dioda tersebut. Bila cahaya lain mengenainya maka dioda ini berfungsi sebagai sumbatan yang memiliki impedansi sangat tinggi sekali. Prinsip kerja *photo dioda* ini sama dengan *photo transistor*, hanya yang membedakan antara keduanya kalau *photo dioda* tidak mamiliki penguatan arus pada anodanya, sedangkan pada photo transistor memiliki penguatan pada arus kolektornya. Simbol pada photo dioda sama dengan *LED infra red* hanya tanda panah masuk menuju dioda, Berikut gambar dari *photo dioda* tersebut :



Gambar 2.5 Simbol *Photo Dioda*

2.3. Sistem Mikrokontroller AT89S8252

Perbedaan mendasar antara mikrokontroler dan mikroprosesor adalah mikrokontroler selain memiliki CPU juga dilengkapi memori dan input output yang merupaka kelengkapan sebagai sistem minimum mikrokomputer sehingga sebuah mikrokontroler dapat dikatakan sebagai mikrokomputer dalam keping tunggal (*Singgel Chip Mikrocomputer*) yang dapat berdiri sendiri.

Mikrokontroler AT89S8252 adalah mikrokontroler ATMEL yang kompatibel penuh dengan mikrokontroler keluarga MCS-51, membutuhkan daya rendah, memiliki performance yang tinggi dan merupakan mikrokomputer 8 bit yang dilengkapi dengan 8 KiloByte Flash memori untuk Program, 2 KiloByte EEPROM

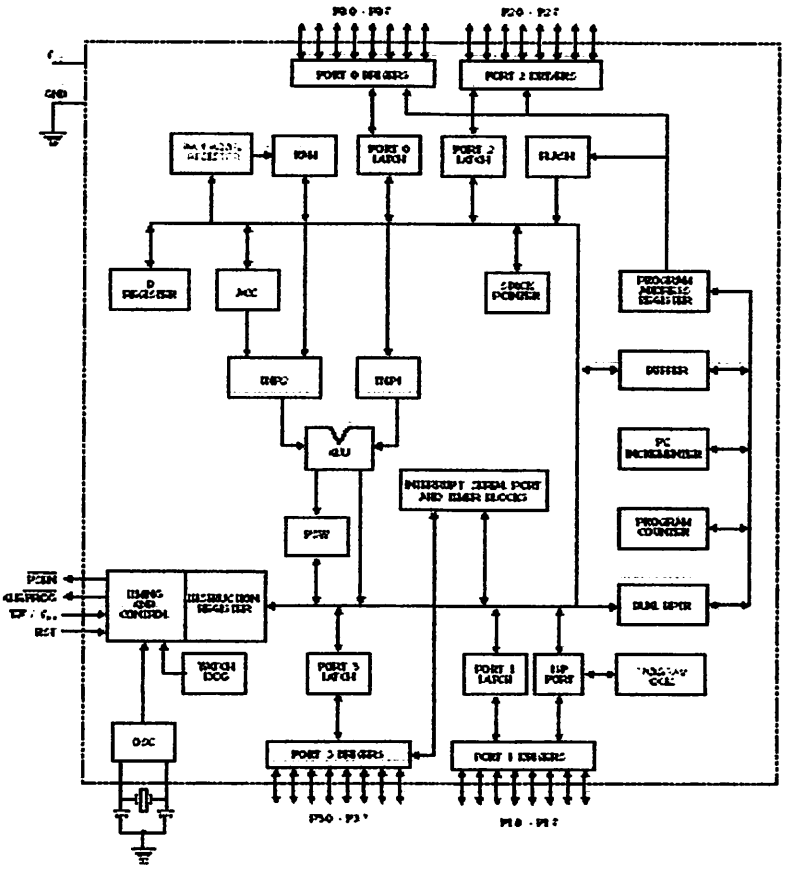
(*Electrical Eraseable and Programable Read Only Memory*) dan 256 Byte RAM internal. Program memori yang dapat diprogram ulang dalam sistem atau menggunakan programer nonvolative Memori Konvensional. Dalam sistem mikrokontroler terdapat dua hal mendasar, yaitu : Perangkat lunak dan perangkat keras yang keduanya saling terkait dan mendukung.

2.3.1. Arsitektur AT89S8252

Secara umum Mikrokontroler AT89S8252 memiliki :

- CPU 8 Bit termasuk keluarga MCS-51
- 8 Kbyte Flash Memori
- 256 Byte Internal Memori
- 32 Port I/O, Masing-masing terdiri atas 8 Jalur I/O
- 2 Timer/Counter 16 Bit
- 2 Serial Port Full Duplex
- Kecepatan pelaksanaan instruksi per siklus 1 μS pada frekuensi clock 12 Mhz.
- 2 DPTR (Data *Pointer*)
- Watchdog Timer
- Fleksibel ISP Programing

Dengan keistimewaan diatas pembuatan alat menggunakan AT89S8252 menjadi lebih sederhana dan tidak memerlukan IC pendukung yang banyak. Adapun blok diagram dari mikrokontroler AT89S8252 adalah sebagai berikut :

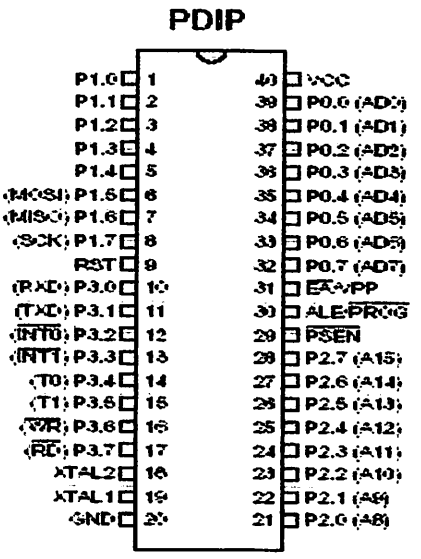


Gambar 2.6 Diagram Blok Mikrokontroler AT89S8252

(Sumber: Data Sheet Atmel AT89S8252)

2.3.2. Konfigurasi Pin-Pin Mikrokontroler AT89S8252

Mikrokontroler AT89S8252 terdiri dari 40 pin dengan konfigurasi sebagai berikut :



Gambar 2.7 Konfigurasi Pena-pena AT89S8252

(Sumber: Data Sheet Atmel AT89S8252)

Fungsi-fungsi tiap pinnya adalah sebagai berikut :

- VCC (Supply Tegangan) , pin 40
- GND (Ground), pin 20
- Port 0, pin 32-39

  Merupakan port input-output dua arah, tanpa internal pull-up dan konfigurasikan sebagai multipleks bus alamat rendah (A_0-A_7) dan data selain pengaksesan program memory dan data memory eksternal

- Port 1, pin 1-8

  Merupakan port input-output dua arah dengan internal pull-up.

- Port 2, pin 21-28

Merupakan port input-output dengan internal pull-up. Mengeluarkan alamat tinggi selama pengambilan program memori eksternal.

- Port 3, pin 10-17

  Merupakan port input-output dengan internal pull-up, dimana Port 3 juga memiliki fungsi khusus dan dapat dilihat pada tabel berikut

Tabel 2.1 Fungsi Khusus Pada Port 3

Nama Penyemat	Fungsi Khusus
Port 3.0	RxD (Port Masukan Serial)
Port 3.1	TxD (Port Keluaran Serial)
Port 3.2	/INT0 (Masukan Interupsi eksternal 0)
Port 3.3	/INT1 (Masukan Interupsi Eksternal 1)
Port 3.4	T0 (Masukkan Pewaktu Eksternal 0)
Port 3.5	T1 (Masukkan Pewaktu Ekstenal 1)
Port 3.6	/WR (Sinyal Tulis Memori Data Eksternal)
Port 3.7	/RD (Sinyal Baca Memori Data Eksternal)

(Sumber: Data Sheet Atmel AT89S8252)

- RST (Reset), pin 9

  Input Reset merupakan reset master untuk AT89S8252.

- ALE/ Prog (*Address Lacth Enable*), pin 30

  Digunakan untuk menahan alamat memori eksternal selama pelaksanaan interuksi.

- PSEN (*Program Store Enable*), pin 29

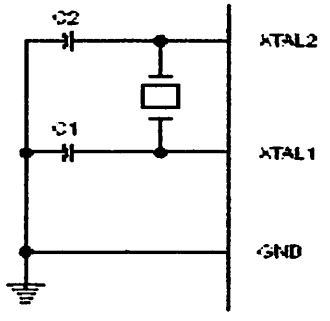
  Merupakan sinyal pengontrol yang memperbolehkan program memori eksternal masuk ke dalam bus.

- EA/VPP (*External Access*), pin 31

  Dapat diberikan logika rendah (*Ground*) atau logika tinggi (*+5 Volt*). Jika diberikan logika tinggi mak mikrokontroler akan mengakses program dari ROM internal (*EEPROM/Flash Memori*), dan jika diberikan logika rendah maka mikrokontroler akan mengakses program dari memori eksternal.

- X-TAL 1 dan X-TAL 2, pin 19,18

  Pin ini dihubungkan dengan kristal bila menggunakan osilator internal. X-TAL 1 merupakan masukan ke rangkaian osilator internal sedangkan X-TAL 2 keluaran dari rangkaian osilator internal. Untuk keperluan ini diperlukan kapasitor penstabil sebesar 30 pF . Dan nilai Dari X-TAL tersebut antara 4-24 Mhz . Untuk lebih jelasnya dapat dilihat gambar pemasangan X-TAL serta kapasitor yang digunakannya.



Gambar 2.8 Osilator Eksternal AT89S8252

(Sumber: Data Sheet Atmel AT89S8252)

2.3.3. Organisasi Memory

Organisasi memori pada mikrokontroler AT89S8252 *dapat dibagi menjadi dua* bagian besar yaitu memori program dan memori data. Pembagian tersebut didasarkan atas fungsi dari penyimpanan data maupun program. Memori program digunakan untuk menyimpan instruksi-instruksi yang akan dijalankan oleh mikrokontroler, sedangkan memori data digunakan sebagai tempat yang sedang diolah mikrokontroler.

Program mikrokontroler disimpan dalam memori program berupa ROM. Mikrokontroler AT89S8252 dilengkapi dengan ROM internal, sehingga untuk menyimpan program tidak digunakan ROM Eksternal yang terpisah dari mikrokontroler. Agar tidak menggunakan memori program eksternal, penyemat/EA dihubungkan dengan Vcc (Logika 1).

Memori program mikrokontroler menggunakan alamat 16 Bit mulai dari 0000_H – $0FFF_H$ sehingga kapasitas penyimpanan program maksimal adalah 4 Kbyte. Sinyal /PSEN (*Program Store Enable*) tidak digunakan jika digunakan memori program internal.

Selain Program mikrokontroler AT89S8252 juga memiliki data intrnal sebesar 128 *Byte* dan mampu mengakses memori data eksternal sebesar 64 Kbyte. Semua memori data internal dapat dialamati dengan data langsung atau tidak langsung. Ciri dari pengalamatan langsung adalah *operand* adalah alamat register yang berisi alamat data yang akan diolah. Sebagian memori tersebut dapat dialamati dengan pengalamatan register, dan sebagian lagi dapat dialamati dengan memori satu bit. Untuk Membaca data digunakan sinyal /RD sedangkan untuk menulis digunakan sinyal /WR.

2.3.4. SFR (*Special Fuction Register*)

Register Fungsi Khusus (*Special Fuction Register*) terletak pada 128 Byte bagian atas memori data internal dan berisi register-register untuk pelayanan lacth port, timer, program status word, control peripheral, dan sebagainya. Alamat register fungsi khusus ini ditunjukkan pada tabel 2.2

Tabel 2.2 Special Fuction Register

Simbol	Nama Register	Alamat
ACC	Accumulator	$E0_H$
B	Register B	$F0_H$
PSW	Program Status Word	$D0_H$
SP	Stack Pointer	81_H
DPTR	Data Pointer 2 Byte	
DPL	Bit Rendah	82_H
DPH	Bit Tinggi	83_H
P0	Port 0	80_H
P1	Port 1	90_H
P2	Port 2	$A0_H$
P3	Port 3	$B0_H$
IP	Interupt Periority Control	$D8_H$
IE	Interupt Enable Control	$A8_H$
TMOD	Timer/Counter Mode Control	89_H
TCON	Timer/Counter Control	88_H
TH0		$8C_H$

TL0	Timer/Counter 0 High Control	$8A_H$
TH1	Timer/Counter 0 Low Control	$8D_H$
TL1	Timer/Counter 1 High Control	$8B_H$
SCON	Timer/Counter 1 Low Control	98_H
SBUF	Serial Control	99_H
PCON	Serial Data Buffer	87_H
	Power Control	

(Sumber: Data Sheet Atmel AT89S8252)

Beberapa macam register fungsi khusus yang sering digunakan adalah sebagai berikut :

- *Accumulator* (ACC) merupakan register untuk penambahan dan pengurangan. Perintah *Mnemonic* untuk mengakses akumulator disederhanakan sebagai A.
- *Register* B Merupakan register khusus yang berfungsi melayani operasi perkalian dan pembagian.
- *Stack Pointer* (SP) merupakan register 8 bit yang dapat diletakkan di alamat manapun pada RAM internal.
- *2 Data Pinter* (DPTR) terdiri atas dua register, yaitu untuk byte tinggi (*Data Pointer High*,DPH) dan byte rendah (*Data Pointer Low*,DPL) yang berfungsi untuk mengunci alamat 16 Bit.

- *Port 0 sampai Port 3* merupakan register yang berfungsi untuk membaca dan mengeluarkan data pada port 0,1,2,3. Masing-masing register ini dapat dialamati per-byte maupun per-bit.
- Control Register terdiri dari register yang mempunyai fungsi kontrol. Untuk mengontrol sistem interupsi, terdapat dua register khusus, yaitu register IP (*Interupt Priority*) dan Register IE (*Interupt Enable*). Untuk mengontrol pelayanan timer/counter terdapat register khusus,yaitu register TCON (*Timer/Counter Control*) serta pelayanan port serial menggunakan register SCON (*Serial Port Control*).

2.3.5. Sistem Interupsi

Mikrokontroler AT89S8252 mempunyai 5 Buah sumber interupsi yang dapat membangkitkan permintaan interupsi, yaitu INT0, INT1, T1, T2 dan Port Serial.

Saat terjadinya interupsi mikrokontroler secara otomatis akan menuju ke subrutin pada alamat tersebut. Setelah interupsi selesai dikerjakan, mikrokontroler akan mengerjakan program semula. Tiap-tiap sumber interupsi dapat *enable* atau *disable* secara software.

Tingkat prioritas semua sumber interupt dapat diprogram sendiri-sendiri dengan set atau clear bit pada (*Interupt Priority*). Jika dua permintaan interupsi dengan tingkat prioritas yang berbeda diterima secara bersamaan, permintaan interupsi dengan prioritas yang sama diterima bersamaan, akan dilakukan polling untuk menentukan mana yang akan dilayani.

Tabel 2.3 Alamat Sumber Interupsi

Sumber Interupsi	Alamat Awal
Interupt Luar 0 (INT 0)	03_H
Pewaktu /Pencacah 0 (T0)	$0B_H$
Interupt Luar 1 (INT 0)	13_H
Pewaktu /Pencacah 0 (T0)	$1B_H$
Port Serial	23_H

(Sumber: Data Sheet Atmel AT89S8252)

2.4 Teori Dasar Voice Timer ISD 2590

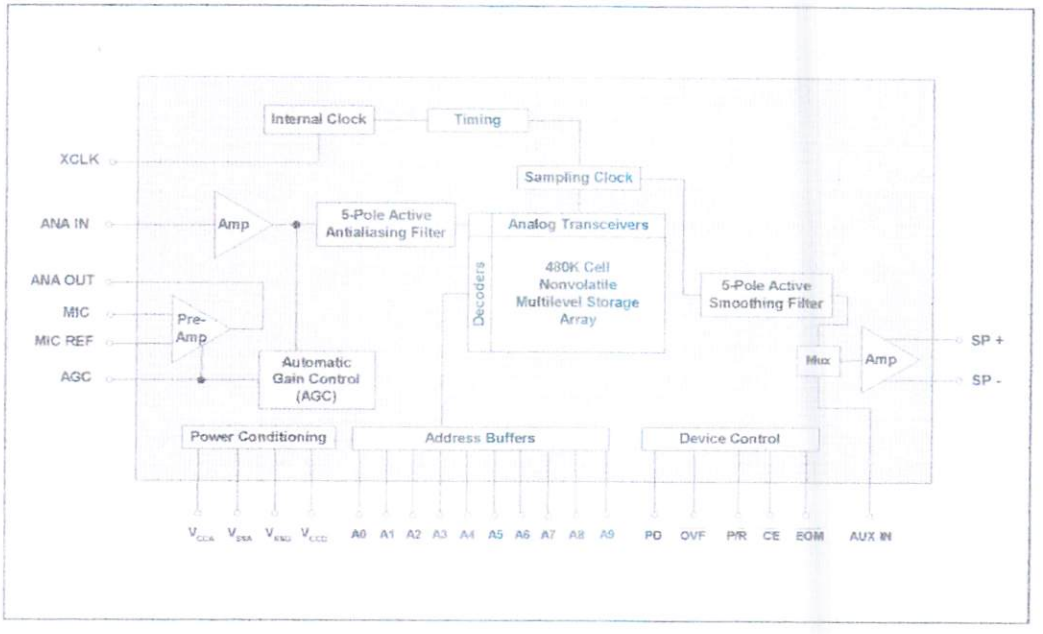
ISD 1420 (Information Storage Devices) adalah rangkaian terpadu serpi tunggal. ISD 2590 Chip Corder merupakan peralatan yang dirancang untuk merekam Seri dan memutar kembali suara dan bunyi dalam suatu chip. Suatu solusi yang tepat untuk merekam dan memutar kembali suatu pesan pendek untuk suatu aplikasi tertentu.

IC ISD 2590 mempunyai perlengkapan di dalam antara lain : Osilator internal, mikrophone pre – amplifier, gain kontrol otomatis, Filter perata dan Speaker amplifier (penguat speaker). Secara keseluruhan seri ISD 2590 dapat dilakukan sebuah perekam atau pemutar ulang pesan dengan komponen yang sederhana seperti mikropon, speaker, beberapa komponen penunjaang dan dua buah saklar tekan dan sumber tegangan. Rekaman akan disimpan dalam sel memori yang tidak mudah hilang (non – volatile), memberikan tempat penyimpanan yang masih kosong. Cara unik ini yang membuat ISD 2590 disebut Direc Analog Storage Technology (STDA)

atau teknik penyimpanan analog langsung, dengan jalan sinyal suara (voice) dan bunyi disimpan secara langsung dalam bentuk analog ke dalam memori.

Penyimpanan analog langsung memungkinkan re = produksi suara secara alami dalam bentuk satu chip tunggal. Perekaman akan berhenti bila input REC tertekan high. Tanda akhir dari pesan (end – message marker) akan otomatis terekam sesudah itu. Tanda ini juga berguna untuk memutuskan playback otmatis bila rekaman sudah habis. ISD akan langsung ke mode stand by bila REC dalam keadaan high.

ISD 2590 mempunyai waktu penyimpanan suara selama 90 detik. Susunan ISD 2590 DAST serta pin dapat dilihat pada gambar dibawah ini.



Gambar: 2.9 Blok diagram ISD 2590

Sumber : Perancangan

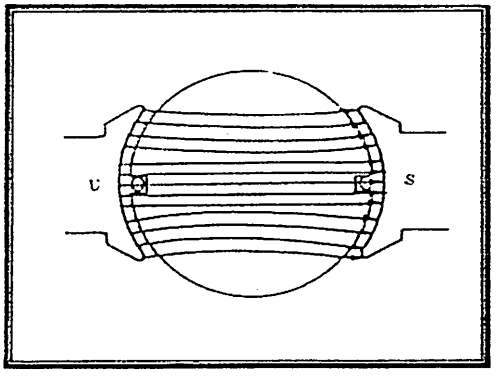
2.5. Motor DC

Motor arus searah (DC) adalah suatu mesin yang berfungsi mengubah energi listrik menjadi energi mekanik. Dasar prinsip kerja motor DC sebenarnya sangat mudah, hanya saja kita sering dibingungkan dengan konstruksi mesin yang agak rumit.

2.5.1.Prinsip kerja Motor arus searah (DC)

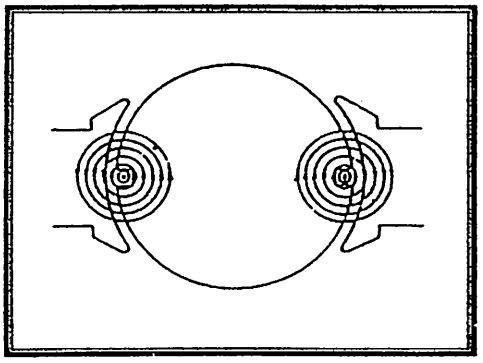
Prinsip kerja motor arus searah didasarkan pada penghantar yang membawa arus ditempatkan dalam suatu medan magnet, maka penghantar tersebut akan mengalami gaya. Gaya menimbulkan torsi yang menimbulkan torsi yang menghasilkan rotasi mekanik, sehingga motor akan berputar. Dalam sistematika kerjanya bisa disimpulkan sebagai berikut :

1. Adanya garis – garis gaya medan magnet (fluks) anatara kutub yang berada di stator
2. Penghantar dialiri arus ditempatkan pada jangkar dalam medan magnet
3. Pada penghantar timbul gaya yang menghasilkan torsi



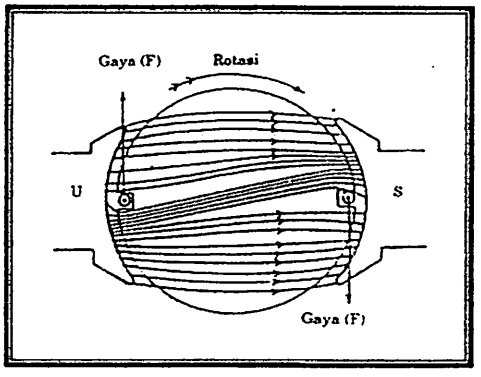
Gambar 2.10. Medan yang dihasilkan oleh kutub

Sumber : "Pengantar Teknik Tenaga Listrik" Ir.Hamzah Berahim



Gambar 2.11. Medan sebagai hasil arus yang mengalir pada penghantar

Sumber : "Pengantar Teknik Tenaga Listrik" Ir.Hamzah Berahim



Gambar 2.12. Interaksi kedua medan menghasilkan gaya

Sumber : "Pengantar Teknik Tenaga Listrik" Ir.Hamzah Berahim

Gambar 2.10 - 2.11. Terjadinya rotasi motor arus searah sebagai interaksi antara medan magnet yang dihasilkan oleh kutub pada stator dan medan magnet yang dihasilkan oleh arus yang mengalir pada penghantar

(sumber : Teknik Tenaga Listrik, "Teori Ringkas dan Penyelesaian Soal", Ir. Hamzah Berahim, 1991, Andy Offset Yogyakarta)

Ada empat persamaan yang mendasari prinsip kerja motor DC :

1. Persamaan gaya pada kawat berarus listrik dalam medan magnet.

   $$F = i (l \times B)$$

   dimana :

F = gaya pada kawat

I = arus yang mengalir pada kawat

L = panjang kawat

B = medan magnet

2. Persamaan tegangan induksi pada kawat berarus listrik yang bergerak dalam medan magnet

$$e_{ind} = (v \times B) l$$

dimana

e_{ind} = tegangan induksi pada kawat

v = kecepatan putar kawat

B = vector medan magnet

L = panjang konduktor dalam medan magnet

3. Hukum tegangan Kirchoff

$$V_b = {}_iR = e_{ind} = 0$$

$$V_b = e_{ind} + iR$$

Pada proses kerja motor DC, keempat persamaan tersebut saling terkait dan berkesinambungan. Proses kerja dapat disimpulkan sebagai berikut :

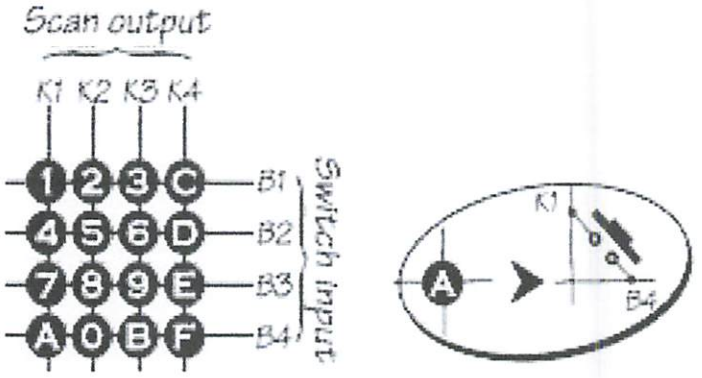
1. Penutup saklar (memberi tegangan) menghasilkan aliran listrik

$$I = V_B / R$$

2. Mengalirnya arus menghasilkan gaya pada lilitan kawat F = Bil
3. Lilitan kawat bergerak kesamping (kanan), menghasilkan tegangan induksi yang berimbas pada kecepatan
4. Tegangan induksi menaikan arus $i = (V_B - e_{ind}) / R$
5. Gaya induksi menurun (F = i l B) , sampai mendekati F = 0. Pada keadaan tersebut, $e_{ind} = V_B$, i = 0, dan lilitan berputar konstan dengan kecepatan tanpa beban $V_{SS} = V_B / B l$

2.6. KEY PAD

Matrik keypad 4x4 merupakan susunan 16 tombol membentuk keypad sebagai sarana input ke mikrokontroler, meskipun jumlah tombol ada 16 tapi hanya memerlukan 8 jalur port paralel, seperti terlihat dalam Gambar 2.13



Gambar 2.13 Matrik Keypad 4x4 (Sumber : www.alds.stts.edu)

Dalam gambar 2.8masing-masing tombol menghubungkan sebuah jalur output (K1; K2; K3 atau K4) ke sebuah jalur input (B1; B2; B3 atau B4), seperti yang digambarkan secara rinci dalam bulatan bagian kanan gambar, tombol "A" menghubungkan jalur K1 ke jalur B4.

Semua tombol mekanis yang biasa dipakai untuk keypad, saat ditekan atau saat tekanan pada tombol dilepas akan bergetar selama lebih kurang 30 sampai 50 mili-detik, sifat ini akan mengakibatkan sub-rutin pembacaan keypad merasakan adanya penekanan tombol secara berulang-ulang, meskipun sesungguhnya tombol hanya ditekan sekali saja. Gejala ini biasanya disebut sebagai bounce.

Untuk mengatasi masalah ini, setelah berhasil membaca nilai tombol yang ditekan, kontroller dipaksa "istirahat" berapa saat sampai tombol tidak bergetar, sebelum membaca tombol berikutnya.

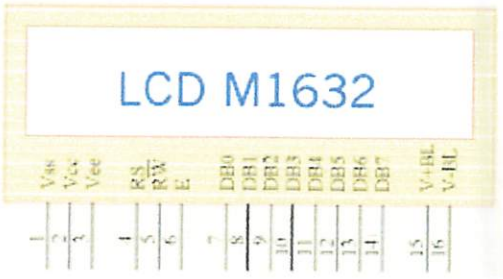
2.7. LCD *(Liquid Cristal Display)*

Liquid Cristal Display adalah modul tampilan yang mempunyai konsumsi daya yang relatif rendah dan terdapat sebuah kontroler CMOS didalamnya. Kontroler tersebut berfungsi sebagai pembangkit ROM / RAM dan *display* data RAM. Semua fungsi tampilan dikontrol oleh suatu instruksi, modul LCD dapat dengan mudah di*interface*kan dengan MPU.

LCD yang digunakan dalam skripsi ini adalah LCD yang memiliki kemampuan sebagai berikut :

- Meliputi 32 karakter yang dibagi menjadi 2 baris dengan *display dot matrik* 5 x 7 ditambah *cursor.*
- Karakter generator ROM dengan 192 karakter.
- Karakter generator RAM dengan 8 tipe karakter.
- Dilengkapi fungsi tambahan yaitu *display clear, cursor home, display ON/OFF, cursor ON/OFF, display character blink, cursor shift* dan *display shift.*
- Internal data.
- 80 x 8 *bit display* data RAM.
- Dapat diinterfacekan dengan µC 8 atau 4 *bit.*
- Internal otomatis dan *reset* pada *power ON.*
- + 5 volt *power supply* tunggal.

Gambar 2.14 di bawah ini menunjukkan LCD beserta pin – pinnya :



Gambar 2.14

Bentuk fisik dari LCD *(Liquid Cristal Display)*

Sumber: LCD *Module User Manual, Seiko Instruments Inc*

Dimana untuk definisi pin-pin yang terdapat dalam LCD *(Liquid Cristal Display)* tersebut dapat dilihat pada tabel berikut ini :

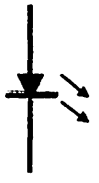
Tabel 2.4 Definisi pin-pin LCD

No	Nama Penyemat	Fungsi
1	Vss	Terminal ground
2	Vcc	Tegangan catu +5 volt
3	Vee	Drive LCD
4	RS	Sinyal pemilih register 0: Instruksi register (tulis) 1: Data Register (tulis dan baca)
5	R/W	Sinyal seleksi tulis atau baca 0: Tulis 1: Baca
6	E	Sinyal operasi awal, sinyal ini mengaktifkan data tulis dan baca
7 – 14	DB0-DB7	Merupakan saluran data, berisi perintah dan data.
15	V+ BL	Pengendali kecerahan latar belakang LCD 4 - 4,42 V dan

		50 – 500 mA
16	V-BL	Pengendali kecerahan latar belakang LCD 0 V

2.8. LAMPU TREFFIC(LED)

Cahaya ini dapat dibangkitkan melalui difusi pada dioda semi konduktor yang biasa disebut LED (*Light Emiting Dioda*). Sedangkan dioda sendiri juga banyak jenisnya termasuk yang bisa memancarkan cahaya saat dialiri arus *forward* padanya, *elektron* dari pita konduksi melewati *junction* dan jatuh kedalam *hole pita valensi*, sehingga elektron – elektron tersebut memancarkan energi. Pada dioda biasa energi ini dipancarkan melalui panas dan dioda yang tidak memancarkan cahaya contohnya *dioda zener* maupun dioda biasa. Lambang dan bentuk dari *Led* tersebut dapat dilihat pada gambar 2.15 berikut dibawah ini :



Gambar 2.15 Simbol Dari LED

2.9. RS-485

Penggerak komunikasi RS-485 adalah pembantu komunikasi serial seperti halnya RS-232 yang sudah dipakai dalam transfer data serial sekarang ini. Perbedaan antara keduanya terletak pada panjang saluran yang dipakai, maksimum bit rate, level tegangan data "1" dan "0", kebocoran daya dan masukaan penerima, mengenai perbedaan tersebut.

Panjang saluran yang di maksud adalah batas panjangnya saluran yang digunakan antara satu driver RS-485 ke driver yang lain yang masih diperbolehkan, ini berkaitan dengan kualitas data yang diterima driver penerima

. Tabel 2.5 menunjukkan karakteristik beberapa tipe komunikasi serial.

Table 2.5 karakteristik beberapa tipe komunikasi serial

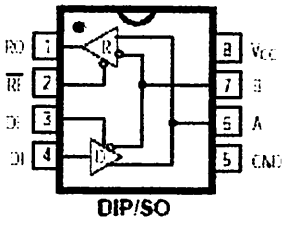
Karekteristik	RS 232	RS 485	RS 423
Saluran panjang	100ft		
Maksimum bit/detik	2×10^4	10^5	10^6
Data "1"=making	-1,5 - -36v	$V_A > V_B$	V_A = -
Data "0"=spancing	+1,5v +3,6v		
Hubungan pendek	100	100	100
Kebocoran bila daya dimatikan,maksimum tegangan yang diberikan pada yang tak diberi daya	300	100	100
Masukan penerima	1,5 Ujung tunggal	100*m*v diferensial	100*m*v diferensial

Sumber : zaks D, 1987

Untuk menampilkan data biner dibutuhkan dua besaran tegangan (V_A dan V_B). Pada RS-485/RS-422 kondisi "1" atau mark dinyatakan dengan membuat tegangan saluran B lebih besar dari saluran A(V_A dan V_B), sedangkan kondisi "0"

atau space dinyatakan dengan membuat saluran A lebih besar dari saluran B(V_A > V_B). Syaratnya tegangan antara dua saluran tersebut ($V_{A\ B}$) harus lebih besar dari 0,4 V dan lebih baik kecil dari 12 V. keuntungan transmisi *sinyal diferensial* adalah berkurangnya noise dalam satu saluran sinyal, akan berkurang secara sama pada saluran sinyal yang lain [Douglas V.Hall ,1992].

Gambar 2.16 menunjukan interface MAX 485.



Gambar 2.16 Interface MAX 485

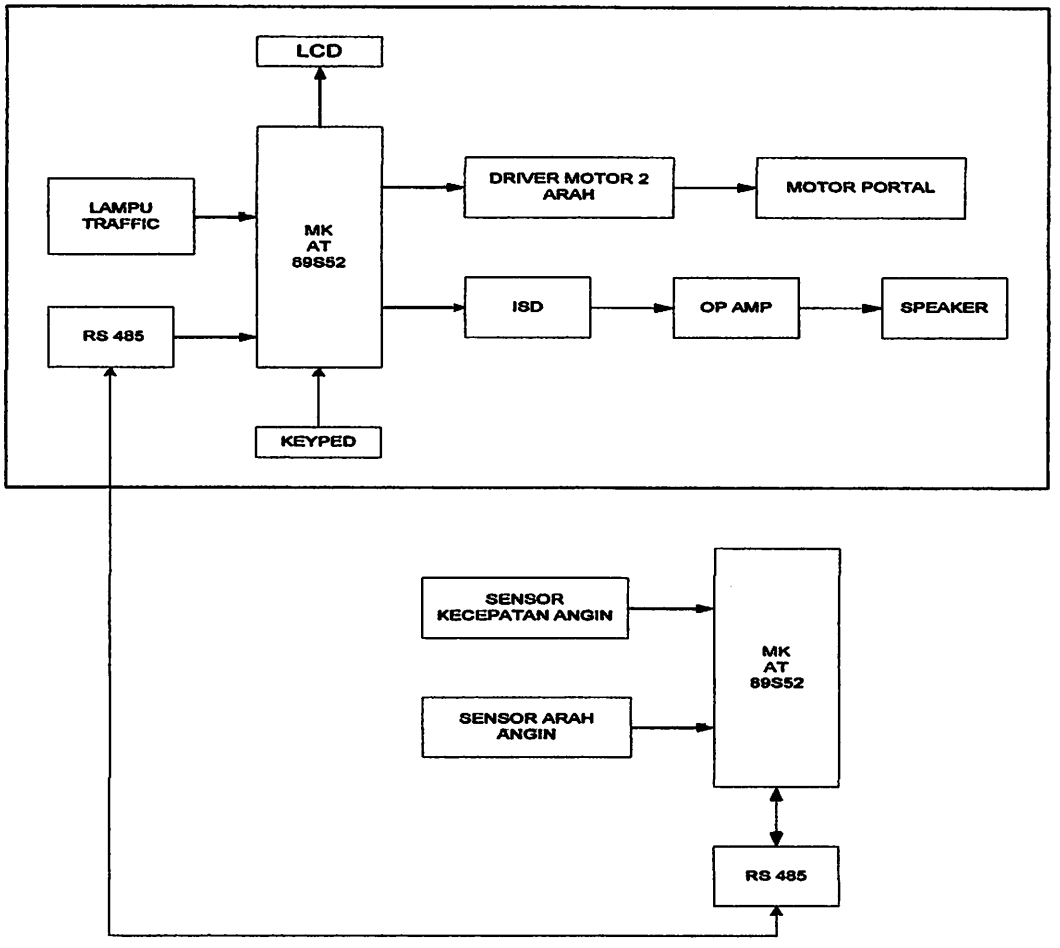
BAB III

PERANCANGAN DAN PEMBUATAN ALAT

Bab ini akan membahas tentang perencanaan dan perancangan alat yang meliputi perencanaan perangkat keras (Hardware) dan perangkat lunak (Software) dari sistem pengaturan kerja motor untuk mengatur agar bisa mebgatur naik-turunnya portal. Pengaturan sistem kerja Sensor kecepatan dan Arah Angin. Perancangan secara keseluruhan dapat dibagi menjadi dua bagian, yaitu :

1. Perancangan Hardware
2. Perancangan Software

3.1 Diagram Blok



Gambar 3.1 Diagram Blok

Fungsi dari tiap – tiap Blok dijelaskan sebagai berikut:

1. Lampu Traffic

   Berfungsi sebagai indikator adanya tanda bahaya

2. RS 485

   Berfungsi sebagai interface antara pengontrol dan alat

3. LCD

   Berfungsi sebagai tampilan batasan kecepatan angin dan arah angin

4. Keypad

   Sebagai tombol untuk setting point batasan kecepatan angin

5. Driver Motor 2 Arah

   Sebagai penguat tegangan untuk motor portal

6. Motor Portal

   Sebagai penggerak naik turun portal

7. ISD

   ISD (Information Storage Device)

   Tipe ISD 2590

   ISD ini mempunyai kemampuan daya simpan suara, selama 90 detik.

   Demikian juga untuk waktu putar ulangnya juga selama 20 detik.

   2590 mempunyai rekaman suara akan disimpan dalam sel memori yang tidak mudah hilang.

8. AMPLIFIER

   Sebagai penguat tegangan dari ISD

9. SPEAKER

   Se agai output, pemberitahuan adanya tanda bahaya sebagai hasil rekaman dari ISD.

10. Sensor Optocoupler Kecepatan Angin

    Sebagai pambaca pulsa kecepatan angin

11. Sensor Optocoupler Arah Angin

    Sebagai pembaca pulsa arah agin

12. *Mkrokonntroller* AT89S52
    Digunakan untuk mengolah data yang diterima, mengkontrol dan mengendalikan rangkaian - rangkaian yang dihubungkan dengannya

3.1.1 Cara Kerja

Sensor kecepatan dan arah angin membaca kecepatan dan arah angin yang akan dikirimkan ke mikrokontoller kemudian memproses kecepatan dan arah angin yang akan dikirim ke operator dengan mengunakan RS 485 yang berfungsi sebagai interface jaringan. Operator akan memproses data yang dikirimkan dari client, apabila data yang dikirimkan dari client melebihi seting point yang telah di tentukan, maka secara otomatis lampu traffick akan menyala merah sebagai tanda bahaya dan ISD akan memberitahukan bahwa kecepatan angin telah melampaui batas normal yang telah ditentukan dengan mengunakan speaker, maka portal akan menutup secara otomatis, ini bertanda bahwa jembatan untuk sementara tidak dapat di gunakan.

3.1.2. Sensor Kecepatan dan Arah Angin

Sensor kecepatan yang dipakai merupakan intregasi antara *optocoupler* sebagai sensor elektronik dengan piringan berputar sebagai mekaniknya. Setiap angin berhembus akan menggerakan piringan, sehingga akan berputar. *Optocupler* akan membaca setiap perubahan pada gelap/terang dipiringan dengan logika "1" dan logika "0".

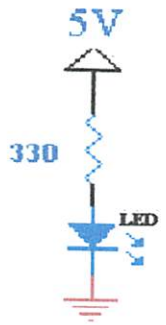
Data ini akan diolah dan disimpan pada sebuah program database.Pada perancangan ini sensor mekanik yang digunaksan adalah piringan yang di buat gelap-terang

Untuk sensor arah sensor arah angin menggunakan sensor inframerah sebagai pemancarnya sedangkan penerimanya menggunakan *photodioda*, yang kemudian diintregasikan dengan sensor mekanik berupa piringan yang berputar.piringan ini memuat 32 data digital dengan menggunakan sistem kode BCD. Dengan menggunakan 5 buah sensor *photodioda* akan mengkonversi data BCD, yang disesuaikan dengan letak arah angin, jika sensor terhalang (gelap) akan berlogika "0" sedangkan jika tidak terhalang (terang) akan berlogika "1".data berupa data 5 bit (00000,00001,00010,00011,00100, ...).

3.1.3. Perancangan Rangkian Sensor

3.1.3.1. Perencanaan Rangkaian Pemancar LED Infra Red

Led infra Red dalam hal ini berfungsi sebagai sumber cahaya yang memancarkan sinyal cahaya. Rangkain dari pemancar LED infra Red seperti pada gambar berikut :



Gambar 3.2 Rangkaian Pemancar LED Infra Red

Pada perancangan dan pembuatan perangkat keras di sini, di mana sumber tegangan Vcc yang dipakai sebesar 5V dan agar dioda infra merah dapat memancarkan sinar infra merah diperlukan arus sebesar 15mA. Sehingga R dapat dihitung dengan menggunakan rumus:

$V = I \cdot R$

Di mana :

V = sumber tegangan

I = arus

R = hambatan

Pada Infra merah :

Diketahui :

$V = 5\ V$

$R = 330\ \Omega$

$V led = 1.8\ V$

Ditanya I dan R ?

$$I = \frac{V - Vled}{R}$$

$$= \frac{5 - 1.8}{0.33}$$

$$= \frac{3.2}{0.33}$$

$$= 9.6 \text{ mA}$$

$$R = \frac{V - Vled}{I}$$

$$= \frac{5 - 1.8}{10}$$

$$= \frac{3.2}{10}$$

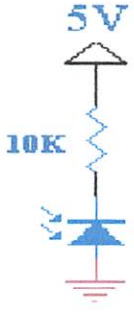
$$= 0.32K\Omega$$

$$= 320\Omega = 330\Omega$$

Karena hambatan 320 Ω di pasaran tidak ada, maka nilai R yang digunakan sebesar 330 Ω sesuai yang ada di pasaran.

3.1.3.2. Perencanaan Rangkaian Penerima Infra Red

Pada sensor arah angin digunakan photodioda sebagai penerima sinyal cahaya yang dipancarkan LED InfraRed dan photodiada dipasang piringan dimana piringan tersebut terdapat sisi gelap-terang,



Gambar 3.3 Rangkaian Penerima InfraRed

Sedangkan pada photodioda diperlukan arus sebesar 0.32 mA sehingga besarnya R dapat dihitung:

Diketahui :

$$V = 5\ V$$

$$R = 10\ k$$

$$V led = 1.8V$$

Ditanya I dan R ?

$$I = \frac{V - Vled}{R}$$

$$= \frac{5 - 1.8}{10}$$

$$= \frac{3,2}{10}$$

$$I = 0.32mA$$

$$R = \frac{V - Vled}{I}$$

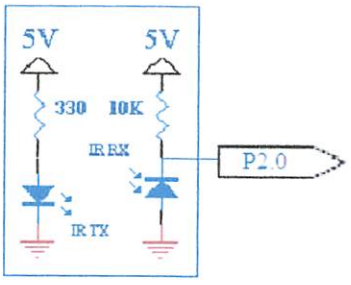
$$= \frac{5 - 1.8}{0,32}$$

$$= \frac{3.2}{0.32}$$

$$R = 10\ k$$

3.1.4. Perancanaan Rangkaian Sensor Kecepatan Angin

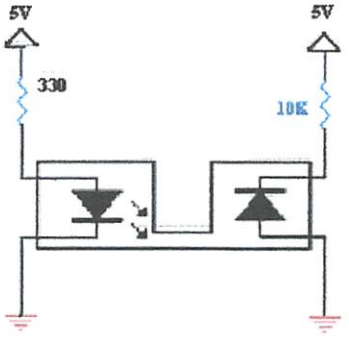
Pada perancangan rangkaian ini dihubungkan dengan kaki port 2.0 pada mikrokongroller AT89S52 client.



Gambar 3.4 Rangkaian Optocoupler Pembaca Kecepatan Angin

Rangkaian sensor yang digunakan adalah *optocopler* yang berfungsi untuk mendeteksi jumlah pulsa yang masuk dari kincir angin yang dipasang dari poros kincir angin. Rangkaian Optocoupler ini terdiri dari dioda pemancar cahaya dan Photidioda yang terpisah oleh celah, dan apabila diberi tegangan maka akan menghasilkankan tegangan output berupa pulsa.

Photodioda pada optocoupler berfungsi untuk menerima sinar dari dioda pemancar cahaya.



Gambar 3.5 Rangkaian optocoupler

Led Infra Red dalam hal ini berfungsi sebagai sumber cahaya yang memancarkan sinyal cahaya. Rangkaian dari pemancar LED Infra Red seperti pada gambar 3.5.

Rangkaian dioda pemancar cahaya (LED Infra Red) dengan Vcc = 5Volt diperlukan arus sebesar 10 mA sehingga besarnya R dapat dihitung :

Diketahui :

$V = 5\,V$

$R = 330\,\Omega$

$V led = 1.8\,V$

Ditanya I dan R ?

$$I = \frac{V - Vled}{R}$$

$$= \frac{5 - 1.8}{0.33}$$

$$= \frac{3.2}{0.33}$$

$$= 9.6\,mA$$

$$R = \frac{V - Vled}{I}$$

$$= \frac{5 - 1.8}{10}$$

$$= \frac{3.2}{10}$$

$$= 0.32K\Omega$$

$$= 320\Omega = 330\Omega$$

Karena hambatan $333\,\Omega$ di pasaran tidak ada, maka nilai R yang digunakan sebesar $330\,\Omega$ sesuai yang ada di pasaran.

Sedangkan pada photodioda diperlukan arus sebesar 0.32 mA sehingga besarnya R dapat dihitung:

Diketahui :

$$V = 5\,V$$

$$R = 10\,k$$

$$V\,led = 1.8V$$

Ditanya I dan R ?

$$I = \frac{V - Vled}{R}$$

$$= \frac{5 - 1.8}{10}$$

$$= \frac{3,2}{10}$$

$$I = 0.32mA$$

$$R = \frac{V - Vled}{I}$$

$$= \frac{5 - 1.8}{0,32}$$

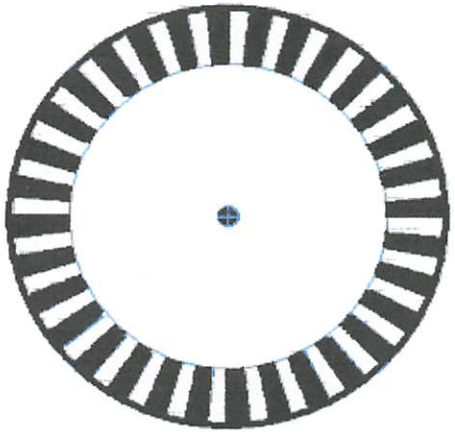
$$= \frac{3.2}{0.32}$$

$$R = 10\ k$$

3.1.5. Piringan Untuk Sensor Kecepatan Angin

Pada Optocoupler yang difungsikan sebagai pengukur kecepatan angin dipasang piringan yang berberbentuk silindris yang dibuat gelap/terang sebanyak 10 yang akan menghasilkan 10 buah pulsa keluaran dalam satu putaran. Banyaknya putaran tergantung pada kencang lambatnya angin,semakin angin bertiup, maka semakin banyak putaran dan pulsa yang di hasilkan.

Pulsa yang di hasilkan oleh Optocoupler ini akan di konterkan oleh mikrokontroller. Dari counter ini akan diketahui berapa banyak pulsa yang dihasilkan oleh piringan optocoupler yang diasumsikan sebagai kecepatan angin,Pad piringan optocoupler, lubang satu dengan lainnya mempunyai selisi beda sudut 36^0. Misalkan dalam satu lubang pada piringan 1/10 putaran kecepatan dalam satuan Km dan pengukuran ini dilakukan per detik, maka apabila dalam satuan detik hanya dihasilkan 2 pulsa keluaran, maka kecepatan angin diasumsikan sebesar 0,2 m/det.



Gambar 3.6 Piringan Sensor Untuk Kecepatan Angin

Untuk mencari kecepatan angin digunakan rumus dasar sebagai berikut :

$$V = \frac{S}{t}$$

dimana :

$t = T = \frac{60}{n.\omega}$ dan

S disini sama dengan $K = 2.\pi\, r$

Ket :

n = Jumblah sisi terang pada piringan

ω = Kecepatan sudut (rpm)

T = Pereode (detik)

K = Keliling lingkaran (m)

r = Jari-jari Piringan (m)

π = 3,14

Sehingga diperoleh persamaan kecepatan sebagai berikut :

$$V = \frac{S}{t}$$

$$V = \frac{2.\pi.r}{T}$$

Misal ω = 10 rpm ; r = 5 cm ; T = 0,1875 sec maka :

$$V = \frac{2.\pi.r}{T}$$

$$V = \frac{2x3.14x5x10^{-2}}{0{,}1875}$$

V = 8,932 m/s

3.1.6 Perancanaan Rangkain Sensor Arah Angin

Pada perancangan ini Seneor arah angin dihubungkan pada mikrokontroller:

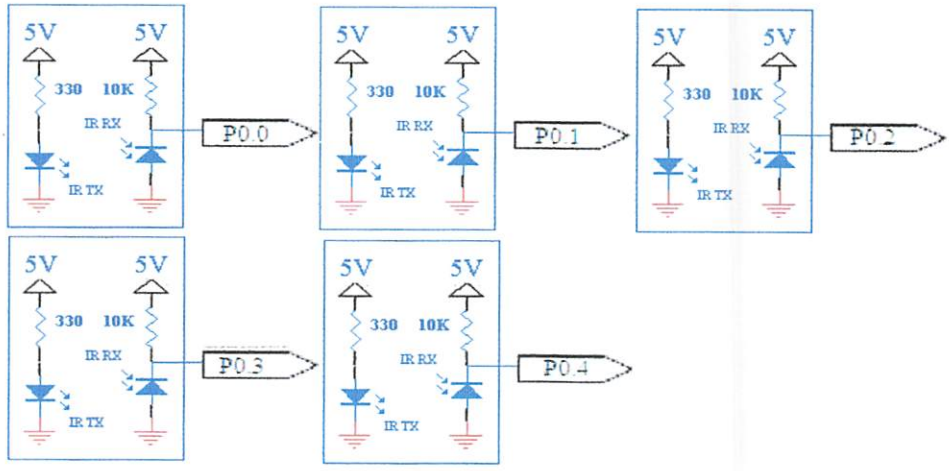
Port 0.0 (kaki 39) dihubungkan dengan Optocoupler ArahAngin

Port 0.1 (kaki 38) dihubungkan dengan Optocoupler ArahAngin

Port 0.2 (kaki 37) dihubungkan dengan Optocoupler ArahAngin

Port 0.3 (kaki 36) dihubungkan dengan Optocoupler ArahAngin

Port 0.4 (kaki 35) dihubungkan dengan Optocoupler ArahAngin



Gambar 3.7 Rangkaian Optocoupler Pembaca Arah Angin

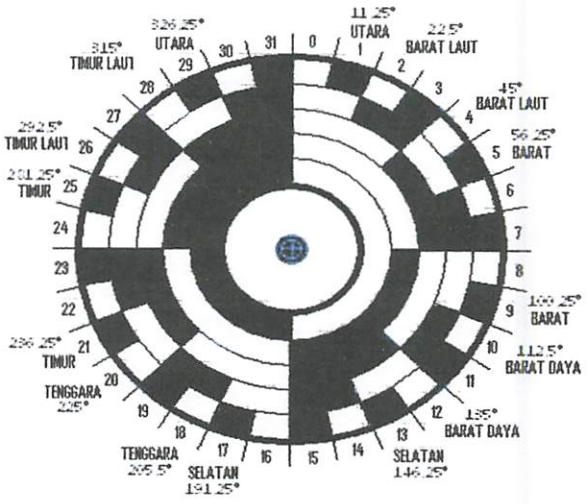
3.1.7. Piringan Untuk Sensor Arah Angin

Piringan yang dipasang pada sensor arah angin berbentuk silindris seperti sensor pada kecepatan angin, hanya bedanya piringan dibuat pola-pola pembentuk kode yang tersusun secara konsentris pada sisi piringan tersebut. Pola-pola tersebut terbentu dari segment-segment yang bergantian antara gelap dan terang pda piringan.

Piringan ini terdiri dari 5 cincin yang disusun secara dari pusat menuju kearah luar jumblah bagian gelap-terang pada cincin kosentris bertambah dalam cacahan biner pada

cincin terluar. Maka masing=masing posisi sudut dari poros penggerak akan mempunyai kombinasi kode yang berbeda.

Karena pada piringan ini dipasang 5 photodioda yang akan mendeteksi semua bilangan biner yang ada pada piringan, maka $360^0 : 2^5 = 11¼^0$. Ini berarti lubang satu dengan yang lainnya pada piringan selisih beda sudut sebesar $11¼^0$.



Gambar 3.8 Piringan Pada Sensor Arah Angin

Dari piringan diatas, maka akan didapat pengkodean arah mata angin seperti terlihat pada tabel 3.1.dibawah ini.

Tabel 3.1 Pengkodeaan Arah Angin Menggunakan Pencacah Bilangan Biner

DESIMAL	BILANGAN BINER	ARAH	SUDUT
0	0 0 0 0 0	UTARA	0^0
1	0 0 0 0 1		$11,25^0$
2	0 0 0 1 0		22.5^0
3	0 0 0 1 1	BARAT LAUT	33.75^0
4	0 0 1 0 0		45^0
5	0 0 1 0 1		$56,25^0$
6	0 0 1 1 0	BARAT	$67,5^0$
7	0 0 1 1 1		$78,75^0$
8	0 1 0 0 0		90^0
9	0 1 0 0 1		$100,25^0$
10	0 1 0 1 0		$112,5^0$

11	0 1 0 1 1	BARAT DAYA	123,75^0
12	0 1 1 0 0		135^0
13	0 1 1 0 1		146,25^0
14	0 1 1 1 0	SELATAN	157,5^0
15	0 1 1 1 1		168,75^0
16	1 0 0 0 0		180^0
17	1 0 0 0 1		191,25^0
18	1 0 0 1 0		205,5^0
19	1 0 0 1 1	TENGGARA	213,75^0
20	1 0 1 0 0		225^0
21	1 0 1 0 0		236,25
22	1 0 1 1 0	TIMUR	247,5
23	1 0 1 1 1		258,75^0
24	1 1 0 0 0		270^0
25	1 1 0 0 1		281,25^0
26	1 1 0 1 0		292,5^0
27	1 1 0 1 1	TIMUR LAUT	303,75^0
28	1 1 1 0 0		315^0
29	1 1 1 0 1		326,25^0
30	1 1 1 1 0	UTARA	337,5^0
31	1 1 1 1 1		348,75^0

3.2 Perancangan Mikrokontroller

3.2.1 Perancangan Mikrokontroller Untuk Operator

Agar sebuah mikrokontroller dapat bekerja sebagai pengontrol, maka kaki – kaki/ port mikrokontroller dihubungkan pada rangkaian – rangkaian *eksternal.* Pada perancangan untuk operator ini dipaparkan port apa saja yang akan digunakan pada mikrokontroller AT89S52 yaitu:

1. **Port 0** dihubungkan dengan ISD dan LCD
2. **Port 1** dihubungkan dengan key ped
3. **Port 2**

    Port 2.2 (kaki 23) dihubungkan dengan PD (Kaki 24) High ISD

    Port 2.3 (kaki 24) dihubungkan dengan PR (kaki 27) Start ISD

    Port 2.4 (kaki 25) dihubungkan dengan A9 (kaki 10) Low ISD

    Port 2.5 (kaki 26) dihubungkan dengan A8 (kaki 9) pada ISD

    Port 2.6 (kaki 27) dihubungkan dengan kaki 4 pada LCD

    Port 2.7 (kaki 28) dihubungkan dengan kaki 6 pada LCD

RXD (kaki 10) dihubungkan dengan R0 (Kaki 1) Pada RS485

TXD (kaki 11) dihubungkan dengan DI (Kaki 4) Pada RS485

INT0 (kaki 12) dihubungkan dengan RE dan DE Pada RS485

INT1 (kaki 13) dihubungkan dengan input2 pada driver motor L298D

T0 (kaki 14) dihubungkan dengan input1 pada driver motor L298D

T1(kaki 15) dihubungkan dengan LED warna Merah Pada traffic Lamp

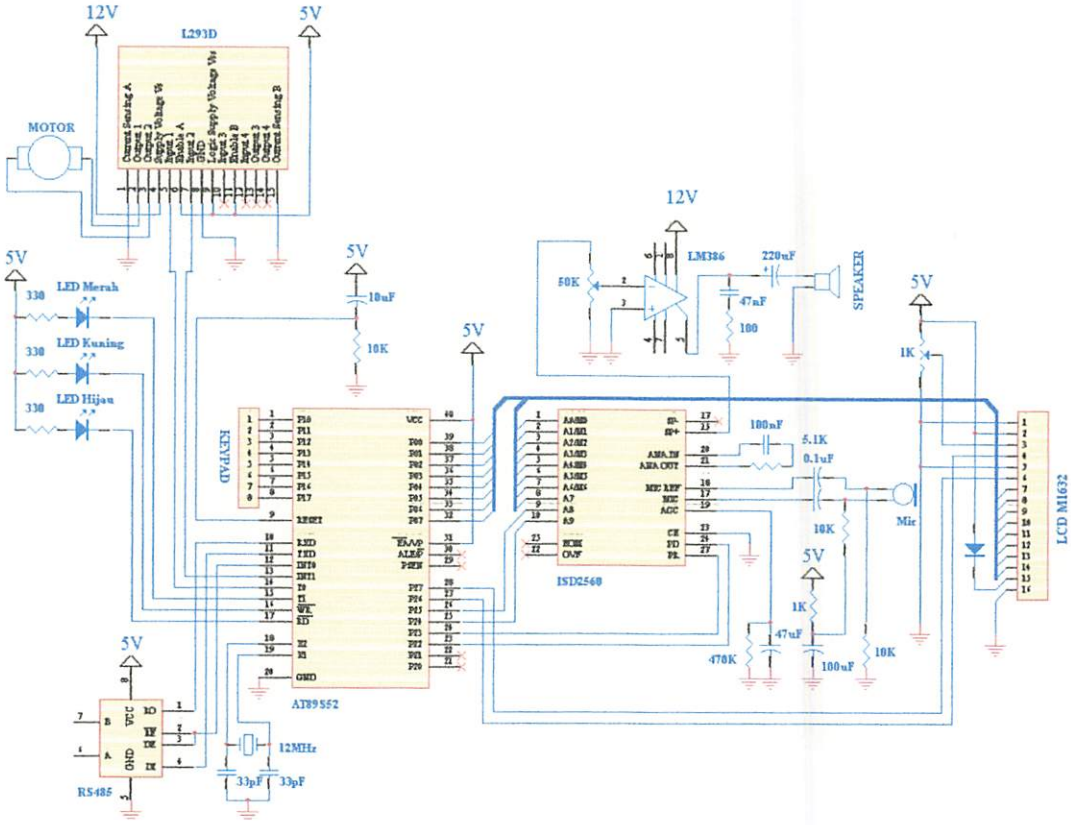
WR (kaki 15) dihubungkan dengan LED warna kuning Pada traffic Lamp

RD (kaki 15) dihubungkan dengan LED warna Hijau Pada traffic Lamp

Reset (kaki 9) dihubungkan dengan rangkaian reset

X1 (kaki 18) **X2** (kaki 19) dihubungkan dengan rangkaian osilator

EAA/P (kaki 40) Dan **VCC** (kaki 31) dihubungkan dengan tegangan 5V



Gambar 3.9 Perancangan Mikrokontroller Untuk Operator

3.2.2 Perancangan Mikrokontroller Untuk Client

Pada Rangkaian *mikrokontroler* AT89S52 untuk clien berfungsi sebagai pengolah data digital yang akan dikirimkan ke server menggunakan RS 485

Mikrokontroller untuk client ini terdapat port - port yang dihubungkan pada rangkaian pendukung yaitu:

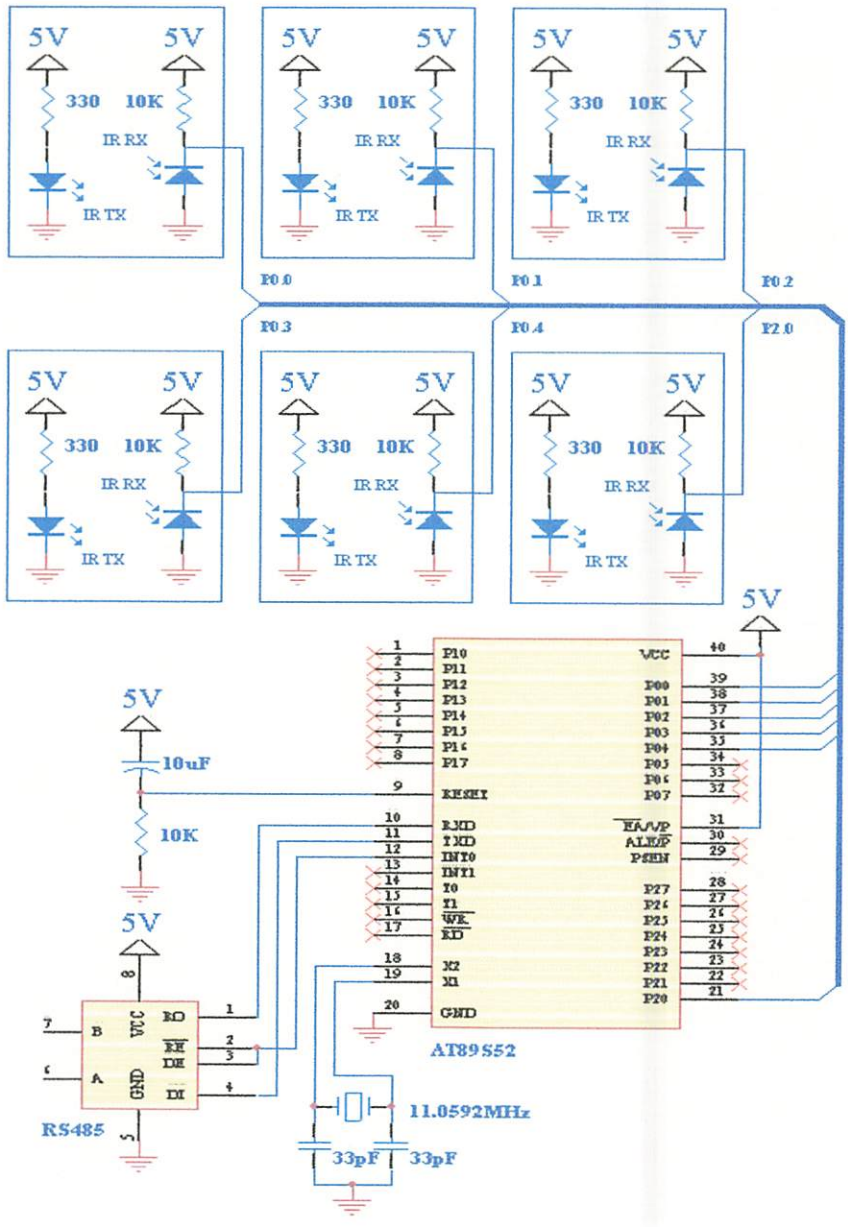
Port 0

P0.0 - P0.5 (kaki 34 - 39) dihubungkangn dengan optocoupler

RXD dihubungkan dengan RO pada RS485

TXD dihubungkan dengan DI pada RS485

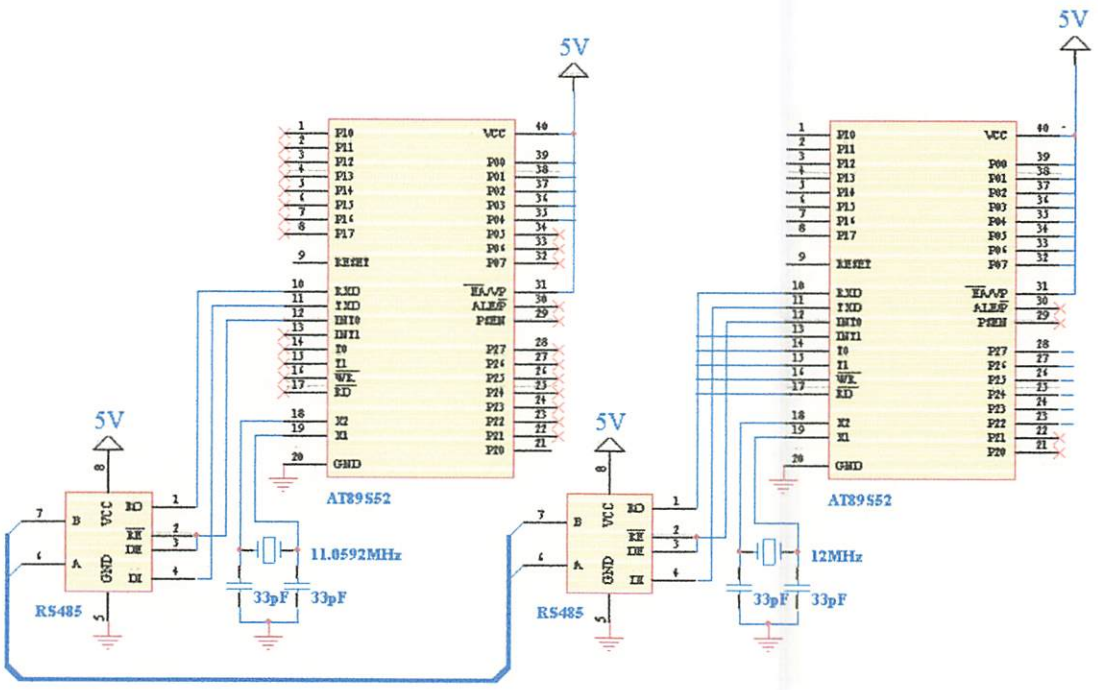
INT0 dihubungkan dengan RE dan DE pada RS485.



Gambar 3.10 Perancangan Mikrokontroller Untuk Client

3.3 Perancangan Koneksi RS 485

Pada perancangan ini digunakan komunikasi serial antara mikrokontroller AT89S52 sebagai operator dan AT89S52 sebagai clien.Pada rangakaian komunikasi serial ini terdapat masing-masing 8 kaki yang dihubungkan pada RS485 maupun pada mikrokontroller yang berfungsi sabagai pembaca dan pengirim data,yaitu:



Gambar 3.11 Perancangan koneksi RS 485

3.3.1 RS485 pada OPERATOR

Kaki 1 (RO) dihubungkan dengan RXD pada mikrokontroller

Kaki 2 (RE) dihubungkan dengan INT0 pada mikrokontroller

Kaki 3 (DE) dihubungkan dengan INT0 pada mikrokontroller

Kaki 4 (DI) dihubungkan dengan TXD pada mikrokontroller

Kaki 5 dihubungkan pada ground

Kaki 6 (A) dihubungkan dengan kaki A pada RS485 client

Kaki 7 (B) dihubungkan dengan kaki B pada RS485 client

Kaki 8 sebagai VCC

3.3.2 RS485 pada CLIENT

Kaki 1 (RO) dihubungkan dengan RXD pada mikrokontroller

Kaki 2 (RE) dihubungkan dengan INT0 pada mikrokontroller

Kaki 3 (DE) dihubungkan dengan INT0 pada mikrokontroller

Kaki 4 (DI) dihubungkan dengan TXD pada mikrokontroller

Kaki 5 dihubungkan pada ground

Kaki 6 (A) dihubungkan dengan kaki A pada RS485 client

Kaki 7 (B) dihubungkan dengan kaki B pada RS485 client

Kaki 8 sebagai VCC

3.4 Rangkaian LCD (*Liquid Crystal Display*)

LCD diperlukan untuk menampilkan nilai karakter *input* yang akan diproses dan data karakter *output* dari hasil pengukuran supaya hasil proses dan pengukuran bisa dipahami oleh manusia. Rangkaian LCD ini dalam pengoperasiannya memerlukan 8 bit data dan 3 bit kontrol. Bagian utama dari rangkaian ini adalah penampil karakter LCD 16 x 2 baris. RS (*Register Select*) dan *Enable* pada pin 4 dan pin 6 yang merupakan kontrol dari LCD. Saluran data (*data bus*) dihubungkan ke port 0 *mikrokontroller*. Untuk pin R/W akan berlogika *low* (0) apabila dihubungkan dengan *ground* maka LCD difungsikan hanya untuk menuliskan program atau data ke *display*. Untuk mengambil data dari *mikrokontroller* maka pin-pin data dihubungkan dengan *port* dari *mikrokontroller.*

Pada lembaran *datasheet* modul LCD M1632 SEIKO INSTRUMENT INC disebutkan bahwa:

Power supply LCD meliputi :

Vss = 0 V

Vcc = 5 V ± 5% (2mA)

Power supply back light :

V + BL = 4 - 4,2 V (50 sampai 200 mA)

V BL = 0 V (GND)

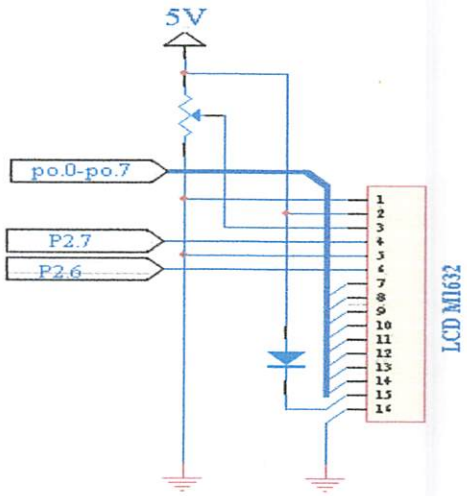
Pada input V + BL dipasang sebuah dioda 1N4001 (bahan silicon dengan Vd = 0,65 V sampai 0,7 V). tujuannya adalah didapatkan tegangan V + BL sebesar 4 - 4,2 V dengan perhitungan sebagai berikut :

$$Vcc = Vd + (V + BL)$$

$$5 = 0,7 + (V + BL)$$

$$(V + BL) = 5 - 0,7 = 4,3 \text{ Volt.}$$

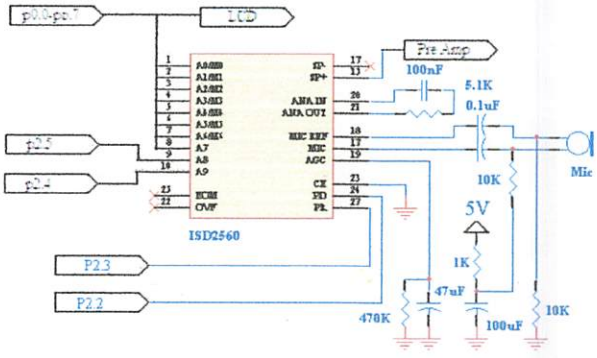
Dipilih dioda 1N4001 karena arus maksimum yang biasa dilewatkan oleh dioda ini sebesar 1A, berikut ini adalah rangkaian lengkap modul LCD yang digunakan dalam perancangan pada gambar 3.5.



Gambar 3.12 Rangkaian LCD

3.5 ISD 2590

Pada perancangan alat ini ISD (*Information Storage Divice*) yang digunakan tipe ISD 2590, dimana ISD ini mempunyai kemampuan daya simpan suara, selama 90 detik. Demikian juga untuk waktu putar ulangnya juga selama 20 detik. ISD dengan tipe 2590 mempunyai rekaman suara akan disimpan dalam sel. Memori yang tidak mudah hilang (*nonvolatile*) yang mempunyai kemampuan untuk menyimpan suara sepanjang 90 detik. Rangkaian ISD dapat dilihat pada gambar 3.6

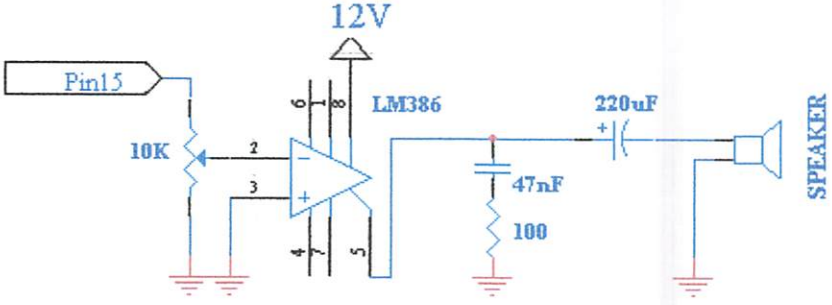


Gambar 3.13 Rangkaian ISD 2590

3.6 *Amplifier*

LM386 Adalah sebuah pengeras suara yang di rancang untuk di gunakan pada aplikasi-aplikasi bertegangan rendah. Peningkatan di buat sampai 20 pada bagian dalam untuk menjaga bagian luar tetap pada hitungan rendah, tapi tambahan sebuah resistor dan kapasitor luar antara pin 1 dan 8 akan meningkatkan tambahan terhadap nilai manapun mulai dari 20 sampai 200.

Pemakaian bereferensi-dasar sedangkan hasilnya secara otomatis membiaskan ke 1-1/2 penyedia tegangan. Penarikan/penyedotan daya diam hanya 24 miliwatts ketika sedang bekerja mulai dari sebuah penyedia 6 volt, membuat LM386 ideal untuk pengoperasian dengan baterai.



Gambar 3.14 Rangkaian Amplifier LM386

3.7 Perancangan Traffic led

Traffic led merupakan rangkaian yang berfungsi sebagai indikator pada jembatan, apakah jembatan aman untuk dilewati atau tidak. Treffic led jika berwarna hijau ini bertanda bawa jembatan aman untuk dilewati, tetapai jika berwarna merah maka jembatan tidak aman untuk dilewati, rangkaian ini dihubungkan ke mikrokontroller

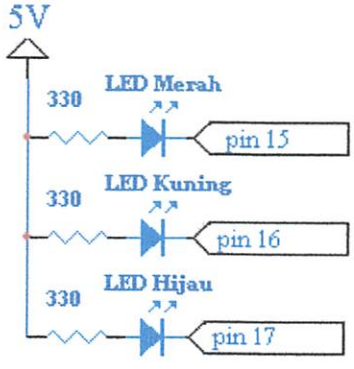
Pada traffic led memiliki 3 lampu indikator yang dihubungkan dengan mikro kontroller yaitu:

- Led merah,dihubungkan pada Port 3.5 (T1)

  memberitahukan bahwa jembatan berbahaya untuk dilewati
- Led kuning dihubungkan pada Port 3.6 (TR)

  Memberitahukan bahwa keadaan angin pada jembatan tidak terlalu baik
- Led hijau dihubungkan pada Port 3.7 (RD)

  Jembatan aman



Gambar 3.15 Rangkaian Traffic led

Menentukan R pada rangkaian traffic led

Diketahui :

V = 1.8

I = 5 sampai 15mA

Ditanya R = ?

$$R = \frac{V - Vled}{I}$$

$$= \frac{5 - 1.8}{10}$$

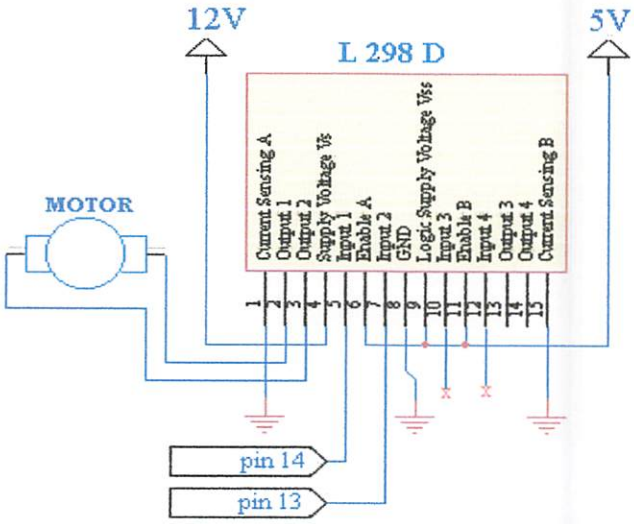
$$= \frac{3.2}{10}$$

$$= 0.32K\Omega$$

$$= 320\Omega = 330\Omega$$

Karena hambatan 333 Ω di pasaran tidak ada, maka nilai R yang digunakan sebesar 330 Ω sesuai yang ada di pasaran.

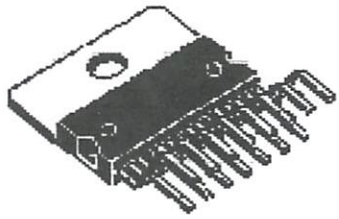
3.8 Driver Motor L298D



Gambar 3.16 Driver Motor L298D

Driver yang berfungsi mengatur pergerakan motor yang dihubungkan dengan port 3.4 (To) – port 3.5 (INT1)pada mikrokontroller.

3.10.1.Karakteristik Driver L298D



Gambar 3.17 L298D

1.Operasi tegangan hingga 46v

2.Total current DC hingga 4A

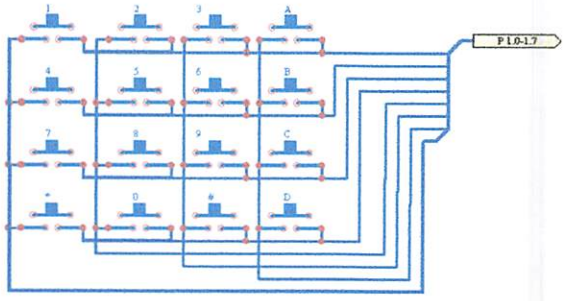
3.Overtemperatur proteksi

4.Logic"0" input hingga 1,5v

(high nois immunity)

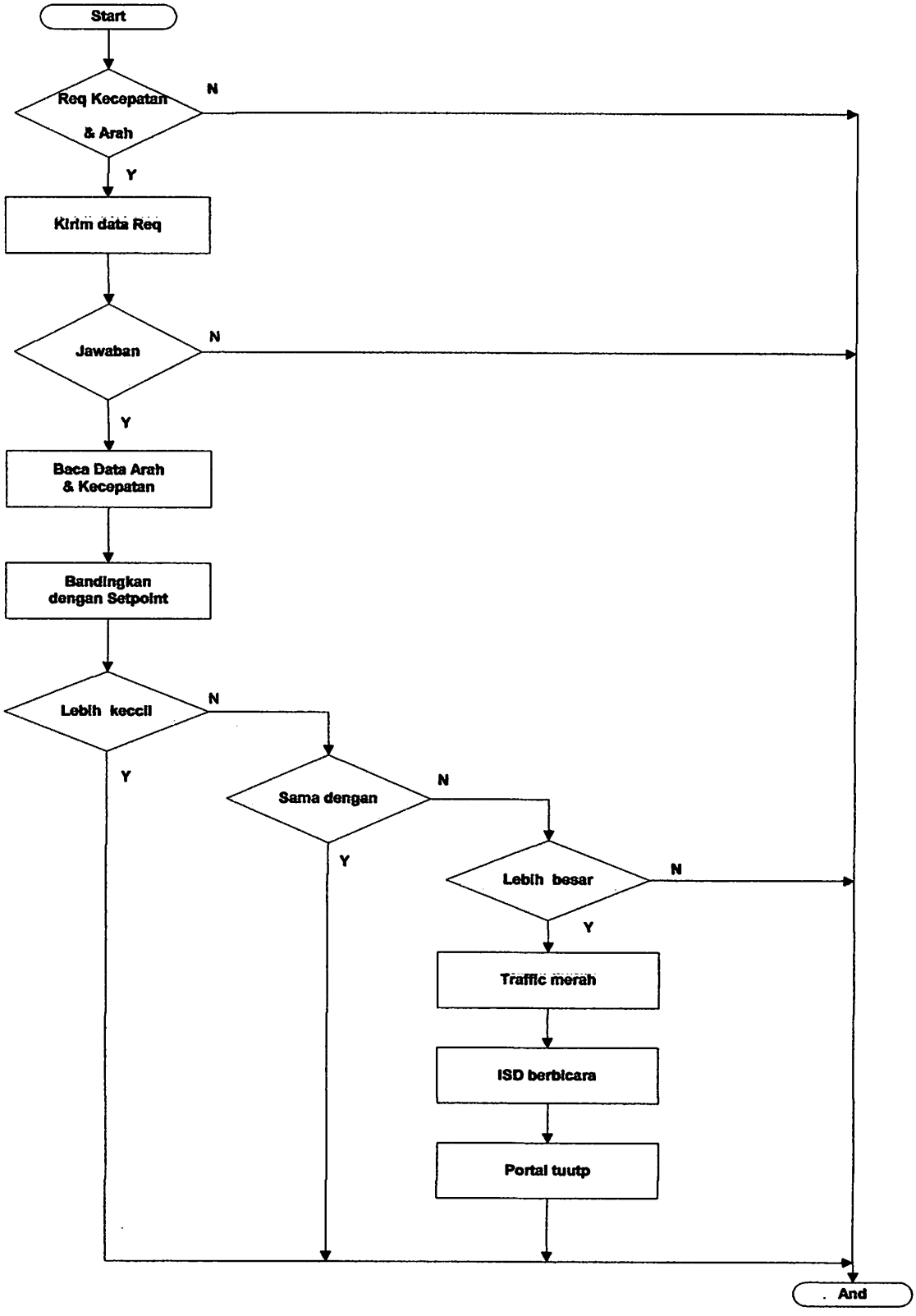
3.9 Rangkaian Keypad

Pada gambar 3.8 adalah blok diagram hubungan *keypad* dengan *mikrokontroller*. *Keypad* yang digunakan adalah *keypad matriks* 4x4. *Port* yang digunakan untuk sinyal port 1.0 – port 1.3 dari mikrokontroller masuk ke kelompok baris *keypad*, sedangkan kelompok kolom *keypad* dihubungkan ke port 1.4 – port 1.7 *mikrokontroller*. Untuk fungsi dari tombol-tombol *keypad* tergantung pada pemrogram. Berikut blok diagram dari penyambungan *keypad* ke *mikrokontroller*

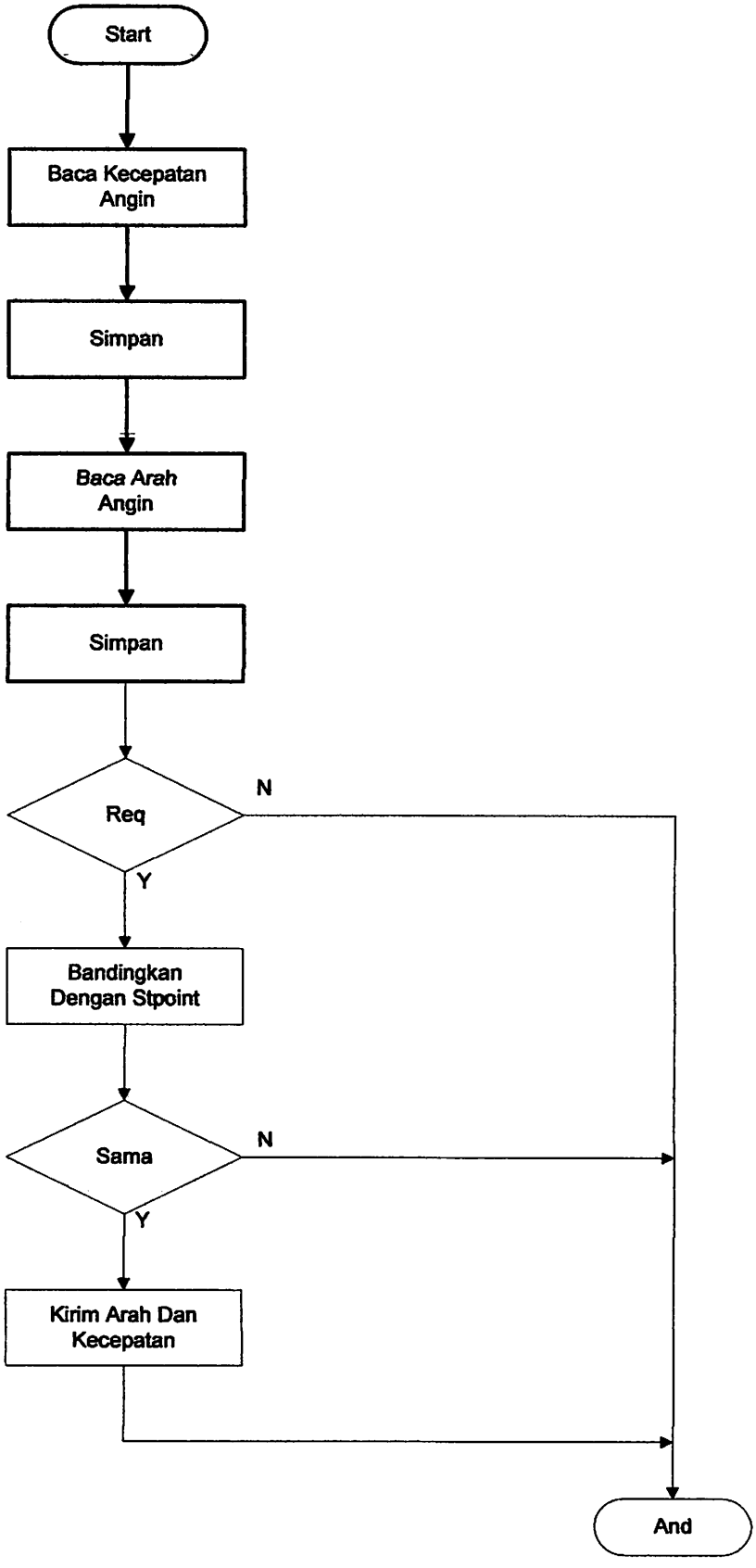


Gambar 3.18 Blok Diagram Hubungan *Keypad* Dengan *Mikrokontrolle*

3.10. Diagram Alir Sistem



Gambar 3.19 *Flowchart 1*



Gambar 3.20 *Flowchart 2*

BAB IV

PENGUJIAN DAN HASIL

Bab ini akan membahas mengenai pengujian alat yang telah dirancang. Tujuan pengujian alat ini adalah untuk mengetahui kerja dari sistem yang dibuat masing – masing blok, sehingga dapat diketahui kepresisisan kerja dari alat yang telah direncanakan. Secara umum tujuan dari pengujian tersebut adalah sebagai berikut :

1. Mengetahui proses kerja dari masing – masing rangkaian (blok).
2. Memudahkan pendataan spesifikasi alat.
3. Memudahkan perawatan dan perbaikan apabila sewaktu – sewaktu terjadi kerusakan.

Pengujian dilakukan secara berulang – ulang untuk mendapatkan hasil pengukuran yang tepat. Prosentase kesalahan antara hasil pengukuran dan hasil perhitungan dapat dicari dengan rumus sebagai berikut :

4.1 Pengujian Rangkaian Sensor Kecepatan Angin

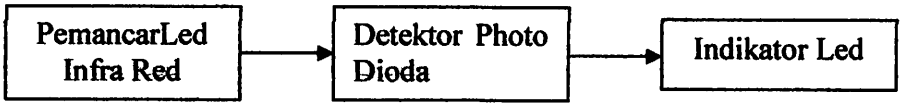
4.1.1 Tujuan Pengujian

Untuk mengetahui apakah rangkaian sensor kecepatan angin (optocoupler) ini dapat bekrja sebagaimana yang diinginkan

4.1.2 Peralatan yang digunakan

- *Indikator Led.*
- *Multimeter digital.*
- *Rangkaian Optocoupler.*
- *Catu daya 5 volt*

4.1.3 Prosedur Pengujian



Gambar 4.1Rangkaian pengujian optocoupler

1. Merangkai peralatan yang digunakan sesuai gambar 4.1
2. Memberikan catu daya 5 v pada rangkaian optocoupler
3. Mengarahkan berkas sinar ke photodiode pada jarak sekitar 2 cm
4. Mengamati keluaran indikator led

4.1.4 Hasil Pengujian

Hasil dari Pengujian Optocoupler ditunjukan pada table 4.1 berikut

Table 4.1 Hasil Pengujian Optocoupler Sensor Kecepatan Angin

Ada/Tidak Ada Halangan	Tegangan Output	Logika
Ada	4,2 V	High
Tidak	130,6 µV	Low

Photodioda akan berlogika 0 (low) jika mendapatkan halangan,dan akan berlogika 1 (high) jika tidak mendapatkan halangan

Berdasarkan hasil dari pengujian yang dilakukan,terlihat bahwa optocoupler tersebut bekerja dengan baik sesuai perencanaan.

4.2 Pengujian Sensor Arah Angin

4.2.1 Tujuan

Untuk mengetahui apakah rangkaian sensor Arah angin (optocoupler) ini dapat bekerja sebagaimana yang diinginkan

4.2.2 Peralatan yang Digunakan

- *Indikator Led.*
- *Multimeter digital.*
- *Rangkaian Optocoupler.*
- *Catu daya 5 volt.*

4.2.3 Prosedur Pengujian

Gambar 4.2 Rangkaian pengujian optocoupler

1. Merangkai peralatan yang digunakan sesuai gambar 4.2
2. Memberikan catu daya 5 v pada rangkaian optocoupler
3. Mengarahkan berkas sinar ke photodiode pada jarak sekitar 2 cm
4. Mengamati keluaran indikator led

4.2.4 Hasil Pengujian

Hasil dari Pengujian Optocoupler ditunjukan pada table 4.2 berikut

Table 4.2 Hasil pengujian optocoupler Sensor Arah Angin

Ada/Tidak Ada Halangan	Tegangan Output	Logika
Ada	4,2 V	High
Tidak	130,6 μV	Low

Photodioda akan berlogika 0 (low) jika mendapatkan halangan,dan akan berlogika 1 (high) jika tidak mendapatkan halangan

Berdasarkan hasil dari pengujian yang dilakukan,terlihat bahwa optocoupler tersebut bekerja dengan baik sesuai perencanaan.

4.3. Pengujian Rangkaian Driver Motor DC

4.3.1 Tujuan Pengujian

Untuk mengetahui apakah rangkaian driver Motor pada Driver Motor Penggerak Naik/Turun portal dapat bekerja sesuai dengan perencanaan

4.3.2 Peralatan yang Digunakan

1. *Motor DC*
2. Mikrokontroller AT89S52
3. *Multimeter digital*
4. *Power Supply* driver Motor DC
5. *Power Supply* Motor DC

4.3.3 Langkah-Langkah Pengujian

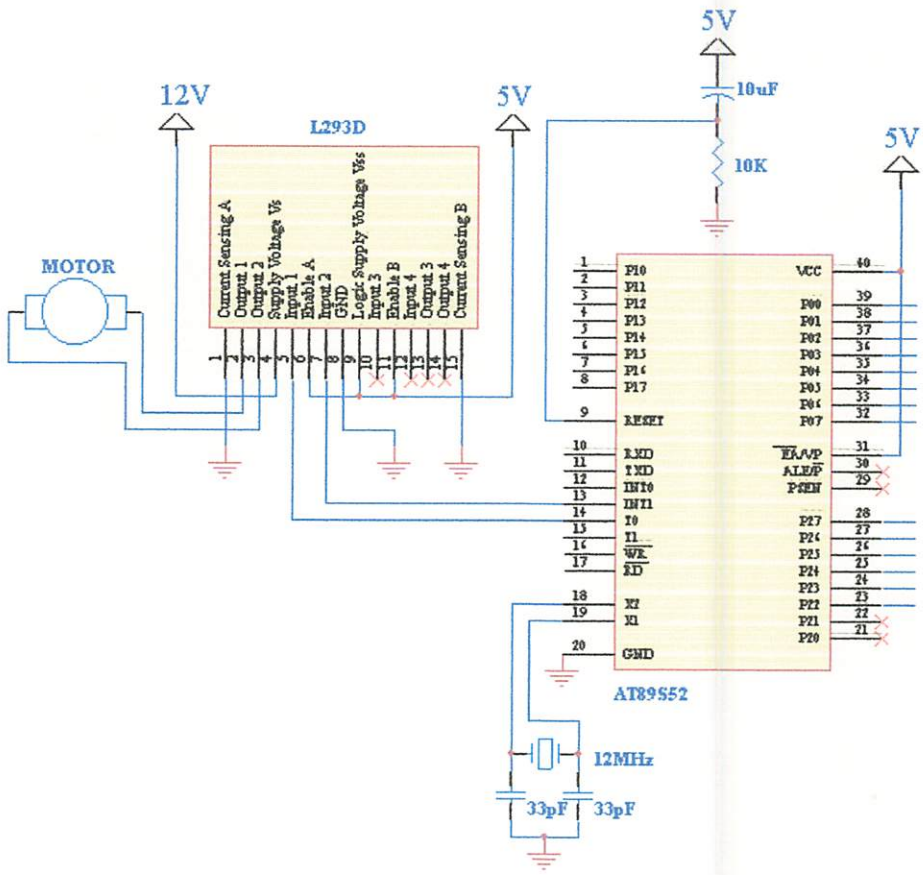
1. Alat dirangkai seperti dalam Gambar 4.3 dan memberikan logika *driver Motor.*
2. Mengukur nilai tegangan keluaran pada Motor.

3. Memberikan logika pada port driver Motor.

4. Mengukur kembali nilai tegangan keluaran pada Motor.

5. Memberikan logika tinggi pada rangkaian NIAIK/TURUN driver Motor.

6. Mengukur polaritas tegangan keluaran pada Motor dan melihat arah putar Motor DC.



Gambar 4.3 Pengujian Rangkaian Driver Motor DC

4.3.4 Hasil dan Analisis Pengujian

Tabel 4.3 Hasil Pengujian Rangkaian Driver Motor DC

Nomor	Masukan Logika pd Driver Motor DC		V out pada Motor DC	Polaritas Tegangan pd Motor DC	Arah Putaran Motor
	ON/OFF	Atas/Bawah			
1	LOW (0)	LOW (0)	0 Volt	-	-
2	HIGH (1)	LOW (0)	12 Volt	Positif	Ke Atas
3	HIGH (1)	HIGH (1)	12 Volt	Negatif	Ke Bawah

4.4 Pengujian Rangkaian Tampilan LCD

4.4.1 Tujuan

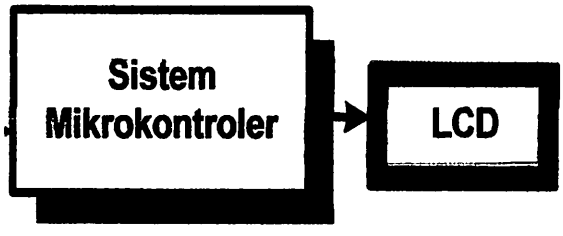
Untuk mengetahui kemampuan rangkaian tampilan yang sudah dibuat apakah dapat mendukung sistem yang direncanakan untuk menampilkan data pada LCD.

4.4.2 Peralatan yang Digunakan

1. *Power Supply* 5 Volt
2. Sistem *Mikrokontroler* dan *LCD M1632*

4.4.3 Prosedur Pengujian

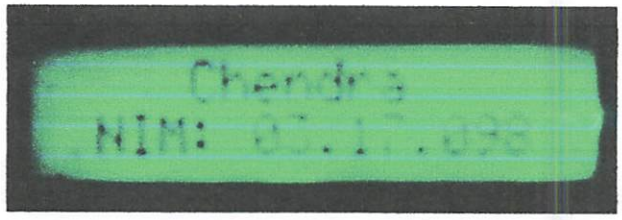
1. Menyusun rangkaian seperti dalam Gambar 4.4
2. Menjalankan program untuk menampilkan tulisan "Identitas Alat"
3. Mengamati keluaran pada LCD.



Gambar 4.4 Diagram Blok Pengujian Rangkaian Tampilan

4.4.4 Hasil dan Analisa Pengujian

Dari hasil Pengujian dapat dilihat bahwa rangkaian tampilan dapat bekerja dengan baik.



4.5 Pengujian Rangkaian *Input Keypad*

4.5.1 Tujuan

Untuk menguji apakah tombol *keypad* dapat bekerja sebagai inputan,dan mensimulasikan tombol yang ditekan melalui suara *buzzer* pada multimeter digital.

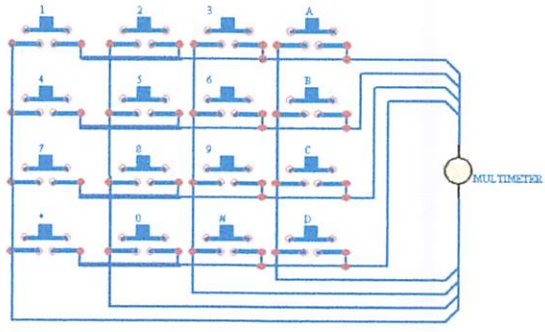
4.5.2 Peralatan yang digunakan

1. *Keypad*
2. *Multimeter*

4.5.3 Pelaksanaan Pengujian

1. Alat – alat dirangkai seperti dalam gambar 4.4
2. Menekan tombol – tombol pada *keypad* dan mengamati serta mencatat keluaran

3. Memberikan kombinasi masukan dengan menekan tombol – tombol *keypad*



Gambar 4.5 Pengujian *Keypad*

4. Memberikan kombinasi masukan dengan menekan tombol – tombol *keypad*

4.5.4. Hasil Pengujian

Tabel 4.4 Hasil Pengujian Keypad

TOMBOL	BARIS				KOLOM			
	1	2	3	4	1	2	3	4
1	1	0	0	0	1	0	0	0
2	1	0	0	0	0	1	0	0
3	1	0	0	0	0	0	1	0
A	1	0	0	0	0	0	0	1
4	0	1	0	0	1	0	0	0
5	0	1	0	0	0	1	0	0
6	0	1	0	0	0	0	1	0
B	0	1	0	0	0	0	0	1
7	0	0	1	0	1	0	0	0

8	0	0	1	0	0	1	0	0
9	0	0	1	0	0	0	1	0
C	0	0	1	0	0	0	0	1
#	0	0	0	1	1	0	0	0
0	0	0	0	1	0	1	0	0
*	0	0	0	1	0	0	1	0
D	0	0	0	1	0	0	0	1

*Keterangan : Cara membaca tabel diatas adalah jika antara baris dan kolom terhubung (1) maka akan membentuk matrik baris dan kolom sesuai penekanan tombol keypad.

Gambar 4.6 Pengecekan Jalur Keypad Dengan Multimeter.

4.5.5 Analisa Hasil Pengujian

Dari rangkaian pengujian didapatkan bahwa untuk membentuk satu karakter penekanan keypad maka baris dan kolom harus terhubung. Sebagai contoh : jika angka 1 ditekan kemudian mengeceknya menggunakan multimeter pada baris 1 dan kolom 1 maka akan terdengar suara buzzer pada multimeter,begitu seterusnya pada penekanan keypad yang lain sesuai tabel

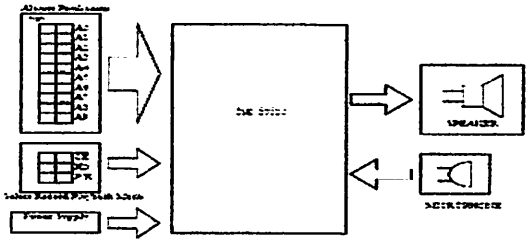
4.6. Pengujian IC Penyimpan Suara ISD 2590

4.6.1. Tujuan

Tujuan dari pengujian IC ini adalah untuk mengetahui apakah ISD2590 dapat melakukan perekaman suara dengan baik atau tidak.

4.6.2. Langkah Percobaan

1. Menghubungkan peralatan sesuai dengan blok diagram berikut :



Gambar 4.7 Diagram Blok Pengujian ISD2590

2. Pin A0 – A7 di beri logika alamat pesan yang diinginkan..
3. Mengaktifkan *Power Up Chip and select* record/playback *mode* dengan memberikan kondisi "*low*" pada pin PD.
4. Memulai perekaman dengan memberikan kondisi "*low*" pada pin P/ *R* dan *CE* .
5. Mengakiri sebuah perekaman dengan memberikan kondisi "*high*" pada pin *CE* atau PD.
6. Memulai pemutaran hasil perekaman dengan memberikan kondisi "*high*" pada pin P/ *R* dan pulsa "*low*" pada pin*CE* .

4.6.3. Hasil Pengujian

Dari hasil proses perekaman suara melalui *mic codensor* yang telah dilakukan sebelumnya, dihasilkan suara dari speaker dengan kualitas suara mendekati sebenarnya.

4.7 Pengujian Keseluruhan

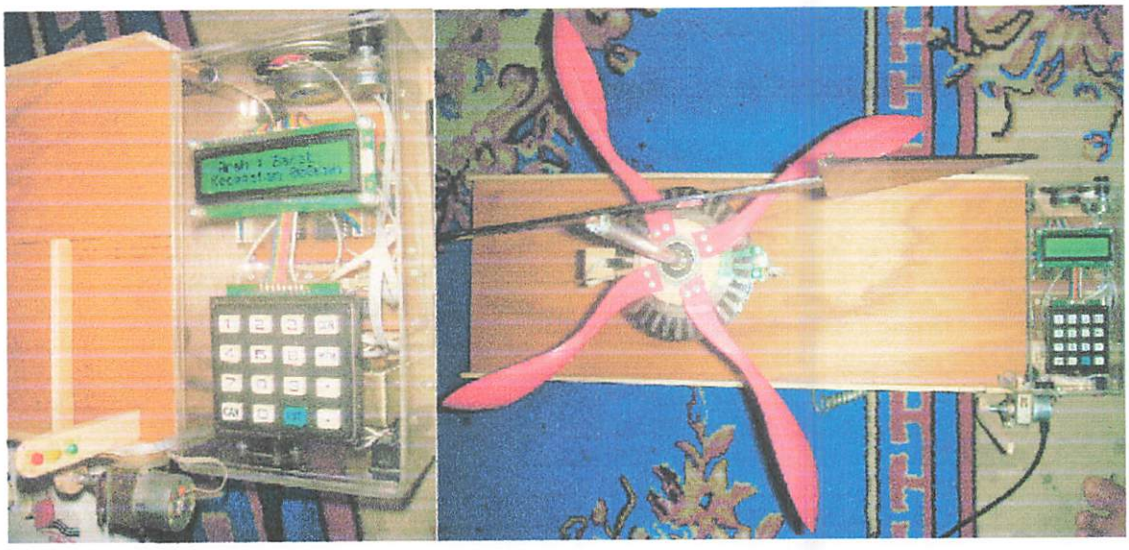
4.7.1 Pengujian Set Poin, Kecepataan dan Arah Angin

Table 4.5 Hasil pengujian perbandingan, Set Poin,Kecepatan dan Arah Angin

Arah	Kecepatan	Set point	Motor	Traffic led	ISD
Utata	5 km/jam	8 km/jam	Naik	Hijau	Off
	6 km/jam	-	-	-	-
	7 km/jam	-	-	-	-
	8 km/jam	-	-	-	-
Barat Laaut	5 km/jam	8 km/jam	Naik	Hijau	Off
	6 km/jam	-	-	-	-
	7 km/jam	-	-	-	-
	8 km/jam	8 km/jam	Naik	Hijau	Off
Barat	5 km/jam	8 km/jam	Naik	Hijau	Off
	6 km/jam	-	-	-	-
	7 km/jam	-	-	-	-
	8 km/jam	-	Turun	Merah	On
Batar daya	5 km/jam	8 km/jam	Naik	Hijau	Off
	6 km/jam	-	-	-	-
	7 km/jam	-	-	-	-
	8 km/jam	-	-	-	-
Selatan	5 km/jam	8 km/jam	Naik	Hijau	Off
	6 km/jam	-	-	-	-
	7 km/jam	-	-	-	-

	8 km/jam	-	-	-	-
Tenggara	5 km/jam	8 km/jam	Naik	Hijau	Off
	6 km/jam	-	-	-	-
	7 km/jam	-	-	-	-
	8 km/jam	-	-	-	-
Timur	5 km/jam	8 km/jam	Naik	Hijau	Off
	6 km/jam	-	-	-	-
	7 km/jam	-	-	-	-
	8 km/jam	-	Turun	Merah	On
Timur Laut	5 km/jam	8 km/jam	Naik	Hijau	Off
	6 km/jam	-	-	-	-
	7 km/jam	8 km/jam	Naik	Naik	Off
	8 km/jam	-	-	-	-

Dari hasil pengujian dapat diketahui bahwa tanda bahaya akan memberitahukan setelah diketahui kecepatan angin $\geq$ 8 km/jam dan arah angin berhembus dari arah samping (Ttimur dan Barat pada set point)



Gambar 4.8 Alat dan Portal

BAB V

PENUTUP

5.1. Kesimpulan

Dari hasil perancanagan dan pembuatan sistem peringatan dini terhadap bahaya kecepatan angin dan pendeteksi arah angin pada jembatan suramadu berbasiskan mikrokontroller AT89S8252 ini dapat diambil kesimpulan antara lain:

1. Keakurasian pengukuran arah angin di pengaruhi oleh pemasangan kincir angin dengan memperhatikan kode piringan arah angin tepat menunjukan utara sebagai acuan pertama.
2. Piringan untuk sensor arah angin dibagi dalam 32 segmen (16 sisi gelap, 16 sisi terang). Sehingga memiliki beda sudut 11,25°. Semakin kecil beda sudutnya, data yang dihasilkanakan lebih akurat.
3. Pada pengujian sensor arah angin jika ada halangan maka dihasilkan tegangan 4,44 Volt yang berlogika high, dan jika tidak ada halangan dihasilkan tegangan 075,6 µV yang berlogika low
4. Pada pengujian sensor kecepatan jika ada halangan maka dihasilkan tegangan 4,2 Volt yang berlogika high, dan jika tidak ada halangan dihasilkan tegangan 130,6 µV yang berlogika low.

5.2. Saran

- Meskipun hasil pengujian dan analisis sudah menyampai keadaan yang diharapkan namun masih banyak perbaiakan atau pengembangan yang dapat dilakukan untuk lebih meningkatkan lagi performasi alat.

- Bahan yang digunakan untuk angin diharapkan dari bahan yang ringan tapi kuat. Agar kecepatan angin keccilpun dapat terdeteksi. Dan apabila ada angin yang kecepatannya besar, kincir angin dapat menahan tidak goyang dan rusak

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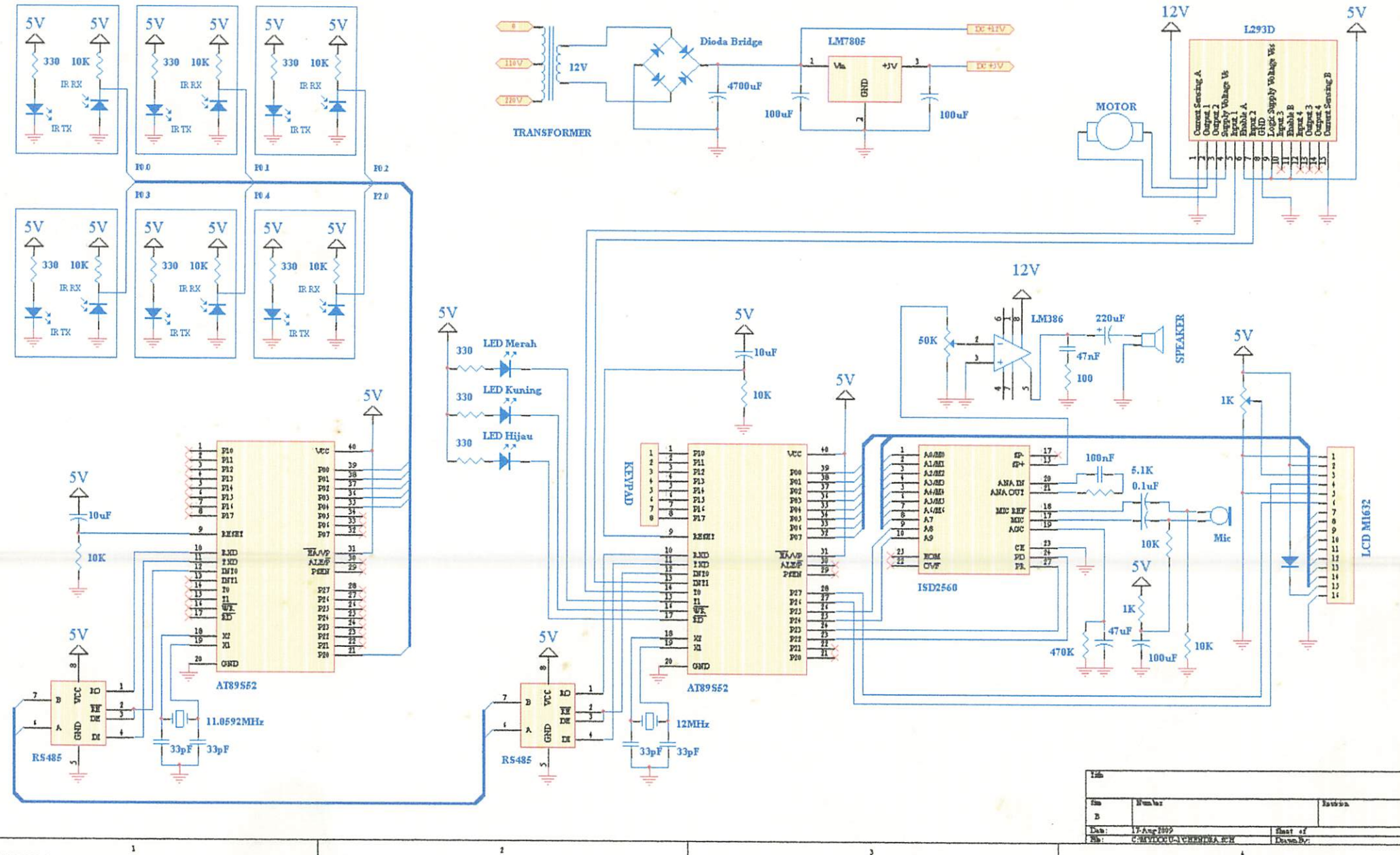
LAMPIRAN



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Jurusan Teknik Elektro S-1

LEMBAR PENGAJUAN JUDUL SKRIPSI
JURUSAN TEKNIK ELEKTRO S-1

Konsentrasi . Teknik Energi Listrik/Teknik Elektronika/Teknik Komputer & Informatika*)

1.	Nama Mahasiswa: chendra			Nim: 03.17.098
2.	Waktu Pengajuan	Tanggal: 24	Bulan: JUNI	Tahun: 2009
3.	Spesifikasi Judul (berilah tanda silang)**) a. Sistem Tenaga Elektrik b. Energi & Konversi Energi c. Tegangan Tinggi & Pengukuran d. Sistem Kendali Industri e. Elektronika & Komponen f. Elektronika Digital & Komputer g. Elektronika Komunikasi h. lainnya			
4.	Konsultasikan judul sesuai materi bidang ilmu kepada Dosen*) Ibrahim Ashari ST MT	Ketua Jurusan Ir. F. Yudi Limpraptono,MT NIP. P. 1039500274		
5.	Judul yang diajukan mahasiswa:	perancangan dan pembuatan sistem pemutus dini terhadap bahaya kebakaran dengan motor arah angin pada jembatan timbang berbasiskan mikrokontroler AT89S8252		
6.	Perubahan judul yang disetujui Dosen sesuai materi bidang ilmu	.....		
7.	Catatan:			
	Persetujuan Judul skripsi yang dikonsultasikan kepada Dosen materi bidang ilmu	Disetujui 200 Dosen M. Ibrahim Ashari, ST MT		

Perhatian:

1. Formulir pengajuan ini harap dikembalikan kepada jurusan paling lambat satu minggu setelah disetujui kelompok dosen keahlian dengan dilampirkan proposal skripsi beserta persyaratan skripsi sesuai form S-1
2. Keterangan: *) Coret yang tidak perlu
   **) dilingkari a, b, c, ...atau g sesuai bidang keahlian

Form S-2

INSTITUT TEKNOLOGI NASIONAL
Jln. Bendungan Sigura-gura No.2
MALANG

Lampiran : 1 (satu-berkas)
Pembimbing Skripsi

Kepada : Yth.Bpk. M Ibrahim Ashari,ST,MT
Dosen Institut Teknologi Nasional
MALANG

Yang bertanda tangan di bawah ini :

Nama	:Chendra
Nim	: 03 17 098
Jurusan	: Teknik Elektro S-1
Konsentrasi	: Teknik Elektronika

Dengan ini mengajukan permohonan, kiranya Bapak/Ibu Bersedia Menjadi Dosen Pembimbing Utama / ~~Pendamping~~ *), untuk penyusunan skripsi dengan judul (Proposal Terlampir):

"PERANCANGAN DAN PEMBUATAN SISTEM PERINGATAN DINI TERHADAP BAHAYA KECEPATAN ANGIN DAN PENDETEKSI ARAH ANGIN PADA JEMBATAN SURAMADU BERBASIS MIKROKONTROLLER AT89S8252"

Adapun tugas tersebut sebagai salah satu syarat untuk menempuh Ujian Akhir Sarjana Teknik
Demikian permohonan kami dan atas kesediaan Bapak/Ibu kami ucapkan terima kasih.

Malang, 25 Juni 2009

Mengatahui
Ketua Jurusan Teknik Elektro S-1

Ir. F. Yudi Limpraptono, MT
NIP.Y. 10395900274

Hormat kami,

Chendra
NIM : 03 17 098

*) coret yang tidak perlu

Form S-3a

INSTITUT TEKNOLOGI NASIONAL
Jln. Bendungan Sigura-gura No.2
MALANG

PERNYATAAN KESEDIAAN DALAM PEMBIMBINGAN SKRIPSI

Sesuai permohonan dari mahasiswa :

Nama : Chendra

Nim : 03 17 098

Semester : XII (Dua Belas)

Jurusan : Teknik Elektro S-1

Konsentrasi : Teknik Elektronika

dengan ini menyatakan bersedia / tidak bersedia *) Membimbing Skripsi dari mahasiswa tersebut dengan judul :

"PERANCANGAN DAN PEMBUATAN SISTEM PERINGATAN DINI TERHADAP BAHAYA KECEPATAN ANGIN DAN PENDETEKSI ARAH ANGIN PADA JEMBATAN SURAMADU BERBASIS MIKROKONTROLLER AT89S8252"

Demikian surat Pernyataan ini kami buat agar dapat dipergunakan seperlunya

Malang, 25Juni 2009

Kami yang membuat pernyataan,

M.Ibrahim Ashari,ST, MT
NIP.P. 1030100358

Catatan :
Setelah disetujui agar formulir ini
Diserahkan mahasiswa/i yang bersangkutan
Kepada Jurusan untuk diproses lebih lanjut
*) coret yang tidak perlu

Form S-3b

INSTITUT TEKNOLOGI NASIONAL
Jl. Raya Karanglo Km 2
MALANG

FORM BIMBINGAN SKRIPSI

Nama : Chendra
NIM : 03.17.098
Masa Bimbingan : 06 juli 2009 s/d 06 Januari 2010
Judul : Perancangan Dan Pembuatan Sistem Peringatan Dini Terhadap Bahaya Kecepatan Angin dan Pendeteksi Arah Angin Pada Jembatan Suramadu Berbasis Mikrokontroller AT98S52

NO	Tanggal	Uraian	Paraf Pembimbing
1	15 Desember 2009	acc Bab I	
2	15 Desember 2009	acc Bab II	
3	15 Desember 2009	Revisi Bab III	
4	30 des 2009	acc Bab III .	
5	7 Jan 10	Revisi Bab IV	
6	27 Jan' 10	acc Bab IV .	
7		Revisi Bab V .	
8	2 Feb '10	acc Bab V	
9			
10			

Malang,
Dosen Pembimbing

M. Ibrahim Ashari, ST, MT
NIP P. 1030100358

Form S-4b

INSTITUT TEKNOLOGI NASIONAL
FAKULTAS TEKNOLOGI INDUSTRI
JURUSAN TEKNIK ELEKTRO
JL.Raya Karanglo Km 2
MALANG

FORMULIR PERBAIKAN UJIAN SKRIPSI

Dalam pelaksanaan Ujian Skripsi Jenjang Strata 1 Jurusan Teknik Elektro Konsentrasi Teknik Elektronika, maka perlu adanya perbaikan skripsi untuk mahasiswa :

Nama : Chendra
Nim : 03.17.098
Masa Bimbingan : 06 Juni 2009 s/d 06 Januari 2010
Judul Skripsi : Perancangan dan Pembuatan Sistem Peringatan dini Terhadap Bahaya Kecepatan Angin dan Pendeteksi Arah Angin pada Jembatan Suramadu Berbasis Mikrokontroller AT98S52

No	Tanggal	Uraian	Paraf
1	17-06-2010	Latar belakang diperbaiki	
2	17-06-2010	Penulisan Laporan diperbaiki	
3	17-06-2010	Perancanagan kecepatan angin dijelaskan	
4	17-06-2010	Laporan perancangan led-led diperbaiki	
5	17-06-2010	Perancangan sensor kecepatan di anlisis jangan hanya rumus	
6	17-06-2010	Perancangnan amplifier diperbaiki	
7	17-06-2010	Kalibrasi alat	
8	17-06-2010	kesimpulan dan saran diperbaiki	

Malang, Juni 2010
Dosen Penguji II

(Irmalia S. Faradisa ST, MT)
NIP. P. 1030000365

INSTITUT TEKNOLOGI NASIONAL
FAKULTAS TEKNOLOGI INDUSTRI
JURUSAN TEKNIK ELEKTRO
JL.Raya Karanglo Km 2
MALANG

FORMULIR PERBAIKAN UJIAN SKRIPSI

Dalam pelaksanaan Ujian Skripsi Jenjang Strata 1 Jurusan Teknik Elektro Konsentrasi Teknik Elektronika, maka perlu adanya perbaikan skripsi untuk mahasiswa :

Nama : Chendra
Nim : 03.17.098
Masa Bimbingan : 06 Juni 2009 s/d 06 Januari 2010
Judul Skripsi : Perancangan dan Pembuatan Sistem Peringatan dini Terhadap Bahaya Kecepatan Angin dan Pendeteksi Arah Angin pada Jembatan Suramadu Berbasis Mikrokontroller AT98S52

No	Tanggal	Uraian	Paraf
1	17-06-2010	Perancanagn dan Analisis Perancangan	
2	17-06-2010	Pengujian diuji lagi	
3	17-06-2010	Kesimpulan Dari Hasil Pengjian	

Malang, Juni 2010
Dosen Penguji I

(I Komang Somawirata, ST, MT)
NIP. Y. 1030100361

LISTING PROGRAM

LISTING PROGRAM

```
   org   00h
    ljmp  init
;
    org   23h
    clr   ES
    jnb   RI,$
    clr   RI
    mov   A,SBUF
    mov   R7,A
    setb  ES
    reti
;
    Hibt   Bit P2.2          ; ISD address High
    ISTR   Bit P2.3          ; ISD start
    Lobt   Bit P2.4          ; ISD address Low
    ISPR   Bit P2.5          ; ISD play/record
    Rest   Bit P2.6          ; RS LCD
    Enbl   Bit P2.7          ; EN LCD
    Slct   Bit P3.2          ; select RS485
    Prtt   Bit P3.3          ; portal tutup
    Prbk   Bit P3.4          ; portal buka
    Ledm   Bit P3.5          ; led merah
    Ledk   Bit P3.6          ; led kuning
    Ledh   Bit P3.7          ; led hijau
    Stsn   Bit 20h.0         ; status sensor
```

```
Stbc   Bit 20h.1          ; status bicara
Dkp0   Equ 30h            ; register data input keypad 0
Dkp1   Equ 31h            ; register data input keypad 1
Dkp2   Equ 32h            ; register data input keypad 2
Buf0   Equ 33h            ; register data buffer 0
Buf1   Equ 34h            ; register data buffer 1
Buf2   Equ 35h            ; register data buffer 1
Dtlo   Equ 36h            ; register data address lo
Dthi   Equ 37h            ; register data address hi
Bicr   Equ 38h            ; register lama bicara
Dta0   Equ 39h            ; data adc 0
Dta1   Equ 3Ah            ; data adc 1
Dta2   Equ 3Bh            ; data adc 2
Dta3   Equ 3Ch            ; data adc 3
Dts0   Equ 3Dh            ; data suhu 0
Dts1   Equ 3Eh            ; data suhu 1
Dts2   Equ 3Fh            ; data suhu 2
Dts3   Equ 40h            ; data suhu 3
Dhld   Equ 41h
Tmot   Equ 42h
Char   Equ 43h
Darh   Equ 44h
Darc   Equ 45h
Dkec   Equ 46h
Stpn   Equ 47h
```

```
      Dly0   Equ 60h
      Dly1   Equ 61h
      Dly2   Equ 62h
      Dly3   Equ 63h
;
init:  acall  lcd_in
      acall  srl_in
      clr    Ledh
      clr    Stsn
      clr    Stbc
      mov    Stpn,#5
;
mulai: mov    DPTR,#nama
      lcall  line1
      mov    Char,#16
      lcall  tulis
      mov    DPTR,#nim
      lcall  line2
      mov    Char,#16
      lcall  tulis
      lcall  delay2
      mov    DPTR,#jurs
      lcall  line1
      mov    Char,#16
```

```
        lcall  tulis
        mov    DPTR,#univ
        lcall  line2
        mov    Char,#16
        lcall  tulis
        lcall  delay2
        sjmp   mulai
;
 stgpnt: mov    DPTR,#tpstpn
        acall  line1
        mov    Char,#16
        acall  tulis
        mov    DPTR,#tpkcpt
        acall  line2
        mov    Char,#16
        acall  tulis
        acall  tg_lps
        mov    DPTR,#angka
stpnt0: mov    P0,#0CAh
        acall  w_ins
        mov    A,Stpn
        acall  nil
        mov    P0,#0D0h
        acall  w_ins
        acall  tg_lps
```

```
stpnt1: acall  scnkpd
        cjne   R0,#10,stpnt2
        sjmp   stpnt1
stpnt2: cjne   R0,#11,stpnt3
        mov    SP,#07h
        ljmp   mulai
stpnt3: cjne   R0,#12,stpnt4
        sjmp   stpnt1
stpnt4: cjne   R0,#13,stpnt5
        sjmp   isiisd
stpnt5: cjne   R0,#14,stpnt6
        sjmp   stpnt1
stpnt6: cjne   R0,#15,stpnt7
        sjmp   stpnt1
stpnt7: cjne   R0,#16,stpnt8
        sjmp   stpnt1
stpnt8: mov    P0,#0CAh
        acall  w_ins
        mov    Buf0,R0
        mov    A,R0
        acall  wr_chr
        acall  tg_lps
        acall  tg_tkn
        mov    Buf1,R0
        mov    A,R0
```

```
      acall  wr_chr
      acall  tg_lps
      mov    A,Buf0                  ;\
      mov    B,#10                   ; |
      mul    AB                ; | pembulatan
      mov    B,Buf1                  ; |
      add    A,B               ;/
      mov    Stpn,A                  ; simpan
      ljmp   stpnt0
;
isiisd: acall  lcdclr
      mov    R1,#1
isisd0: cjne   R1,#1,isisd1
      mov    DPTR,#tpdgsr
isisd1: cjne   R1,#2,isisd2
      mov    DPTR,#tprcsr
isisd2: acall  line1
      mov    Char,#16
      acall  tulis
      acall  tg_lps
isisd3: acall  scnkpd
      cjne   R0,#15,isisd5
      dec    R1
      cjne   R1,#0,isisd4
      mov    R1,#1
```

```
isisd4: ljmp   isisd0
isisd5: cjne   R0,#16,isisd7
        inc    R1
        cjne   R1,#3,isisd6
        mov    R1,#2
isisd6: ljmp   isisd0
isisd7: cjne   R0,#11,isisd8
        mov    SP,#07h
        ljmp   mulai
isisd8: cjne   R0,#12,isisd3
isisd9: cjne   R1,#1,isisdA
        ljmp   plyisd
isisdA: cjne   R1,#2,isisd9
        ljmp   recisd
;
plyisd: mov    DPTR,#tpaddr
        acall  line2
        mov    Char,#11
        acall  tulis
        mov    DPTR,#angka
        acall  tg_tkn
        mov    Dkp0,R0
        mov    A,R0
        acall  wr_chr
        acall  tg_lps
```

```
        acall  tg_tkn
        mov    Dkp1,R0
        mov    A,R0
        acall  wr_chr
        acall  tg_lps
        acall  tg_tkn
        mov    Dkp2,R0
        mov    A,R0
        acall  wr_chr
        acall  tg_lps
plisd0: mov    DPTR,#tpdgsr
        acall  line1
        mov    Char,#16
        acall  tulis
        mov    DPTR,#tpaddr
        acall  line2
        mov    Char,#11
        acall  tulis
        mov    DPTR,#angka
        mov    A,Dkp0
        acall  wr_chr
        mov    A,Dkp1
        acall  wr_chr
        mov    A,Dkp2
        acall  wr_chr
```

```
        mov    A,#10
        acall  wr_chr
        mov    A,#10
        acall  wr_chr
plisd1: acall  scnkpd
        cjne   R0,#11,plisd2
        mov    SP,#07h                  ; reset RAM
        ljmp   mulai
plisd2: cjne   R0,#12,plisd1
        acall  lcdclr
        mov    DPTR,#tpplyg
        acall  line1
        mov    Char,#16
        acall  tulis
        acall  datadd                   ; switch data to address (dec to hex)
        mov    A,Dthi
plisd3: cjne   A,#0,plisd4
        clr    Lobt
        clr    Hibt
plisd4: cjne   A,#1,plisd5
        setb   Lobt
        clr    Hibt
plisd5: cjne   A,#2,plisd6
        clr    Lobt
        setb   Hibt
```

```
plisd6: mov    P0,Dtlo
        acall  delay0
        acall  delay0
        clr    lStr
        acall  tg_lps
        setb   lStr
        acall  tg_lps
        ljmp   plisd0
;
recisd: mov    DPTR,#tprcsr
        acall  line1
        mov    Char,#16
        acall  tulis
        mov    DPTR,#tpaddr
        acall  line2
        mov    Char,#11
        acall  tulis
        mov    DPTR,#angka
        acall  tg_tkn
        mov    Dkp0,R0
        mov    A,R0
        acall  wr_chr
        acall  tg_lps
        acall  tg_tkn
        mov    Dkp1,R0
```

```
        mov    A,R0
        acall  wr_chr
        acall  tg_lps
        acall  tg_tkn
        mov    Dkp2,R0
        mov    A,R0
        acall  wr_chr
        acall  tg_lps
rcisd0: mov    DPTR,#tprcsr
        acall  line1
        mov    Char,#16
        acall  tulis
        mov    DPTR,#tpaddr
        acall  line2
        mov    Char,#11
        acall  tulis
        mov    DPTR,#angka
        mov    A,Dkp0
        acall  wr_chr
        mov    A,Dkp1
        acall  wr_chr
        mov    A,Dkp2
        acall  wr_chr
        mov    A,#10
        acall  wr_chr
```

```
      mov    A,#10
      acall  wr_chr
;
rcisd1: acall  scnkpd
      cjne   R0,#11,rcisd2
      mov    SP,#07h                    ; reset RAM
      ljmp   mulai
rcisd2: cjne   R0,#12,rcisd1
      acall  lcdclr
      mov    DPTR,#tprcdg
      acall  line1
      mov    Char,#16
      acall  tulis
      acall  datadd                     ; switch data to address (dec to hex)
      mov    A,Dthi
rcisd3: cjne   A,#0,rcisd4
      clr    Lobt
      clr    Hibt
rcisd4: cjne   A,#1,rcisd5
      setb   Lobt
      clr    Hibt
rcisd5: cjne   A,#2,rcisd6
      clr    Lobt
      setb   Hibt
rcisd6: mov    P0,Dtlo
```

```
    acall  delay0
    acall  delay0
    clr    ISPR
    clr    IStr
    acall  tg_lps
    setb   IStr
    setb   ISPR
    acall  tg_lps
    ljmp   rcisd0
;
datadd: mov    Buf0,Dkp0          ; simpan data input keypad 0 -> Buf0
    mov    A,Dkp1                 ;\
    mov    B,#10                  ; | data input keypad 1 dikali 10
    mul    AB                     ; | ditambah dengan
    mov    B,Dkp2                 ; | data input keypad 2
    add    A,B                    ; | hasil simpan -> Buf1
    mov    Buf1,A                 ;/
    mov    Dtlo,#0                ; reset counter lo addr
    mov    Dthi,#0                ; reset counter hi addr
    mov    A,Buf0                 ;\
    cjne   A,#0,datad1            ; | cek Buf0 = 0 ?
    ljmp   datad3                 ; | tidak -> panggil subroutine cntadr
datad1: mov    R7,#100            ; | sebanyak 100 kali
datad2: acall  cntadr             ; | ulang sebanyak Buf0
    djnz   R7,datad2              ;/
```

```
      djnz   Buf0,datad1
datad3: mov    A,Buf1                  ;\
      cjne   A,#0,datad4          ; | cek Buf1 = 0 ?
      ljmp   datad5                  ; | tidak -> panggil subroutine cntadr
datad4: acall  cntadr                 ; | sebanyak Buf1
      djnz   Buf1,datad4          ; | return
datad5: ret                           ;/
;
cntadr: inc    Dtlo                   ;\
      mov    A,Dtlo                  ; | tambah Dtlo
      cjne   A,#0,cntadd          ; | cek Dtlo = 0 ?
      inc    Dthi                   ; | tambah Dthi
cntadd: ret                           ;/
;
kalbrs: lcall  lcdclr
      mov    DPTR,#tpkcpt
      lcall  line2
      mov    Char,#16
      lcall  tulis
klbrs0: lcall  bc_arh
      lcall  line1
      mov    Char,#16
      lcall  tulis
      mov    DPTR,#angka
      mov    P0,#0CAh
```

```
    lcall  w_ins
    lcall  bc_kec
    mov    A,Dkec
    lcall  nilai
    mov    P0,#0D0h
    lcall  w_ins
;
    lcall  proses                  ; analisa bahaya
    lcall  bicara                  ; analisa bicara
;
    mov    Dly3,#1
    lcall  delay3
    lcall  scnkpd
    cjne   R0,#11,klbrs0
    mov    SP,#07h
    ljmp   mulai
;
proses: mov    A,Darh
    cjne   A,#02,prses0
    ljmp   prses1
prses0: cjne   A,#06,prses2
prses1: mov    A,Dkec
    mov    B,Stpn
    div    AB
    jz     prses2
```

```
        jb     Stsn,prses3
        setb   Stsn
        clr    Ledm
        setb   Ledh
        lcall  prtttp
        ljmp   prses3
prses2: jnb    Stsn,prses3
        clr    Stsn
        setb   Ledm
        clr    Ledh
        lcall  prtbka
prses3: ret
;
bicara: jnb    Stsn,bicr00
        lcall  bcrbhy
        setb   Stbc
        ljmp   bicr01
bicr00: jnb    Stbc,bicr01
        clr    Stbc
        lcall  bcramn
        lcall  bcramn
        lcall  bcramn
bicr01: ret
;
bcrbhy: clr    Hibt                    ; address 00
```

```
    clr   Lobt
    mov   P0,#00
    clr   ISTR
    mov   Dly3,#60
    lcall delay3
    setb  ISTR
    mov   Dly3,#1
    lcall delay3
    ret
;
bcramn: clr   Hibt                    ; address 100
    clr   Lobt
    mov   P0,#100
    clr   ISTR
    mov   Dly3,#60
    lcall delay3
    setb  ISTR
    mov   Dly3,#1
    lcall delay3
    ret
;
bc_arh: mov   A,#100
    lcall kr_srl
    lcall tg_cmd
    mov   B,#4
```

```
      div   AB
      mov   Darh,A
bcarh0: cjne  A,#00,bcarh1
      mov   DPTR,#tparh0
bcarh1: cjne  A,#01,bcarh2
      mov   DPTR,#tparh1
bcarh2: cjne  A,#02,bcarh3
      mov   DPTR,#tparh2
bcarh3: cjne  A,#03,bcarh4
      mov   DPTR,#tparh3
bcarh4: cjne  A,#04,bcarh5
      mov   DPTR,#tparh4
bcarh5: cjne  A,#05,bcarh6
      mov   DPTR,#tparh5
bcarh6: cjne  A,#06,bcarh7
      mov   DPTR,#tparh6
bcarh7: cjne  A,#07,bcarh8
      mov   DPTR,#tparh7
bcarh8: ret
;
bc_kec: mov   A,#101
      lcall  kr_srl
      lcall  tg_cmd
      mov   Dkec,A
      ret
```

```
;
srl_in: acall  delay1
      mov    TMOD,#20h
      mov    TH1,#0F3h
      mov    SCON,#50h
      setb   TR1
      setb   ES
      setb   EA
      clr    Slct
      ret
;
kr_srl: setb   Slct
      lcall  delay0
      clr    ES
      mov    SBUF,A
      jnb    TI,$
      clr    TI
      setb   ES
      clr    Slct
      ret
;
tg_cmd: lcall  rstcmd
tgcmd0:          cjne   R7,#0FFh,tgcmd1
      ljmp   tgcmd0
tgcmd1: ret
```

```
;
rstcmd: mov    R7,#0FFh
        ret
;
nilai:  mov    B,#100
        div    AB
        acall  wr_chr
        mov    A,B
nil:    mov    B,#10
        div    AB
        acall  wr_chr
        mov    A,B
        acall  wr_chr
        ret
;
prtbka: clr    Prbk                    ; portal buka
        setb   Prtt
        mov    Dly3,#5
        lcall  delay3
        setb   Prbk
        setb   Prtt
        ret
;
prtttp: setb   Prbk                    ; portal tutup
        clr    Prtt
```

```
    mov   Dly3,#6
    lcall delay3
    setb  Prbk
    setb  Prtt
    ret
;
line1: mov   P0,#080h
    acall w_ins
    ret
;
line2: mov   P0,#0C0h
    acall w_ins
    ret
;
tulis: clr   A
    acall wr_chr
    inc   DPTR
    djnz  Char,tulis
    ret
;
wr_chr: movc  A,@A+DPTR
    mov   P0,A
    acall w_chr
    ret
;
```

```
w_ins: clr   Enbl
       clr   Rest
       setb  Enbl
       clr   Enbl
       acall delay0
       ret
;
w_chr: clr   Enbl
       setb  Rest
       setb  Enbl
       clr   Enbl
       acall delay0
       ret
;
lcd_in: acall delay1
       mov   P0,#01h                ; Display Clear
       acall w_ins
       mov   P0,#38h                ; Function Set
       acall w_ins
       mov   P0,#0Dh                ; Display On, Cursor, Blink
       acall w_ins
       mov   P0,#06h                ; Entry Mode
       acall w_ins
       mov   P0,#02h                ; Cursor Home
       acall w_ins
```

```
        ret
;
lcdclr: mov    P0,#01h                    ; Display Clear
        acall  w_ins
        acall  delay0
        acall  delay0
        ret
;
scnkpd: mov    R0,#10
        acall  delay0
col1:   mov    P1,#11111110b
        mov    A,P1
c1b1:   cjne   A,#11101110b,c1b2
        mov    R0,#1
c1b2:   cjne   A,#11011110b,c1b3
        mov    R0,#2
c1b3:   cjne   A,#10111110b,c1b4
        mov    R0,#3
c1b4:   cjne   A,#01111110b,col2
        mov    R0,#13
;
col2:   mov    P1,#11111101b
        mov    A,P1
c2b1:   cjne   A,#11101101b,c2b2
        mov    R0,#4
```

```
c2b2:  cjne   A,#11011101b,c2b3
       mov    R0,#5
c2b3:  cjne   A,#10111101b,c2b4
       mov    R0,#6
c2b4:  cjne   A,#01111101b,col3
       mov    R0,#14
;
col3:  mov    P1,#11111011b
       mov    A,P1
c3b1:  cjne   A,#11101011b,c3b2
       mov    R0,#7
c3b2:  cjne   A,#11011011b,c3b3
       mov    R0,#8
c3b3:  cjne   A,#10111011b,c3b4
       mov    R0,#9
c3b4:  cjne   A,#01111011b,col4
       mov    R0,#15
;
col4:  mov    P1,#11110111b
       mov    A,P1
c4b1:  cjne   A,#11100111b,c4b2
       mov    R0,#11
c4b2:  cjne   A,#11010111b,c4b3
       mov    R0,#0
c4b3:  cjne   A,#10110111b,c4b4
```

```
      mov    R0,#12
c4b4:  cjne   A,#01110111b,back
      mov    R0,#16
back:  ret
;
tg_tkn: acall  scnkpd
tg_tk0: cjne   R0,#16,tg_tk1
      ljmp   tg_tkn
tg_tk1: cjne   R0,#15,tg_tk2
      ljmp   tg_tkn
tg_tk2: cjne   R0,#14,tg_tk3
      ljmp   tg_tkn
tg_tk3: cjne   R0,#13,tg_tk4
      ljmp   tg_tkn
tg_tk4: cjne   R0,#12,tg_tk5
      ljmp   tg_tkn
tg_tk5: cjne   R0,#11,tg_tk6
      ljmp   tg_tkn
tg_tk6: cjne   R0,#10,tg_tk7
      ljmp   tg_tkn
tg_tk7: ret
;
tg_lps: acall  scnkpd
      cjne   R0,#10,tg_lps
      ret
```

```
;
delay0: djnz   Dly0,delay0
     ret
;
delay1: acall  scnkpd
     djnz   Dly1,delay1
     ret
;
delay2: mov    Dly2,#15
dely20: acall  delay1
     cjne   R0,#13,dely21
     ljmp   stgpnt
dely21: cjne   R0,#14,dely22
     ljmp   kalbrs
dely22: djnz   Dly2,dely20
     ret
;
delay3: acall  delay0
     djnz   Dly1,delay3
     djnz   Dly3,delay3
     ret
;
nama:  DB    '  Chendra   '
nim:   DB    ' NIM: 03.17.098 '
jurs:  DB    ' Teknik Elektro '
```

```
univ:  DB    '  ITN Malang  '
tpstpn: DB    '  Seting Point  '
tpkcpt: DB    'Kecepatan   Kmh'
tpdgsr: DB    ' Dengar Suara ? '
tprcsr: DB    ' Rekam Suara ?  '
tpplyg: DB    '  Playing....  '
tprcdg: DB    ' Recording....  '
tpaddr: DB    '  Address:     '
tparh0: DB    ' Arah : Utara  '
tparh1: DB    'Arah: Barat Laut'
tparh2: DB    ' Arah : Barat  '
tparh3: DB    'Arah: Barat Daya'
tparh4: DB    ' Arah : Selatan '
tparh5: DB    ' Arah : Tenggara'
tparh6: DB    ' Arah : Timur  '
tparh7: DB    'Arah: Timur Laut'
angka:  DB    '0123456789    '
;
    end
```

DATA SHEET

atures

- ompatible with MCS-51™ Products
- Bytes of In-System Reprogrammable Downloadable Flash Memory
  - SPI Serial Interface for Program Downloading
  - Endurance: 1,000 Write/Erase Cycles
- Bytes EEPROM
  - Endurance: 100,000 Write/Erase Cycles
- to 6V Operating Range
- lly Static Operation: 0 Hz to 24 MHz
- ree-level Program Memory Lock
- x 8-bit Internal RAM
- Programmable I/O Lines
- ree 16-bit Timer/Counters
- ne Interrupt Sources
- ogrammable UART Serial Channel
- I Serial Interface
- w-power Idle and Power-down Modes
- errupt Recovery From Power-down
- ogrammable Watchdog Timer
- al Data Pointer
- wer-off Flag

scription

AT89S8252 is a low-power, high-performance CMOS 8-bit microcomputer with ytes of downloadable Flash programmable and erasable read only memory and ytes of EEPROM. The device is manufactured using Atmel's high-density nonvol- memory technology and is compatible with the industry-standard 80C51 uction set and pinout. The on-chip downloadable Flash allows the program mem- to be reprogrammed in-system through an SPI serial interface or by a ventional nonvolatile memory programmer. By combining a versatile 8-bit CPU downloadable Flash on a monolithic chip, the Atmel AT89S8252 is a powerful ocomputer which provides a highly-flexible and cost-effective solution to many edded control applications.

AT89S8252 provides the following standard features: 8K bytes of downloadable , 2K bytes of EEPROM, 256 bytes of RAM, 32 I/O lines, programmable watch- timer, two data pointers, three 16-bit timer/counters, a six-vector two-level rupt architecture, a full duplex serial port, on-chip oscillator, and clock circuitry. In tion, the AT89S8252 is designed with static logic for operation down to zero fre- ncy and supports two software selectable power saving modes. The Idle Mode s the CPU while allowing the RAM, timer/counters, serial port, and interrupt sys- to continue functioning. The Power-down mode saves the RAM contents but es the oscillator, disabling all other chip functions until the next interrupt or hard- reset.

downloadable Flash can be changed a single byte at a time and is accessible gh the SPI serial interface. Holding RESET active forces the SPI bus into a serial ramming interface and allows the program memory to be written to or read from ss Lock Bit 2 has been activated.

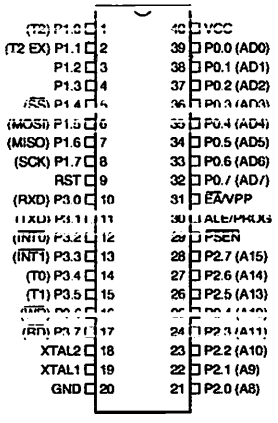
8-bit
Microcontroller with 8K Bytes Flash

AT89S8252

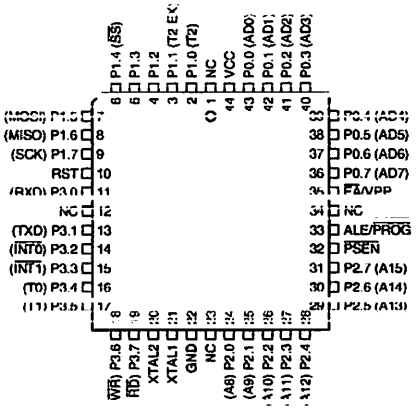
Rev. 0401E–02/00

Configurations

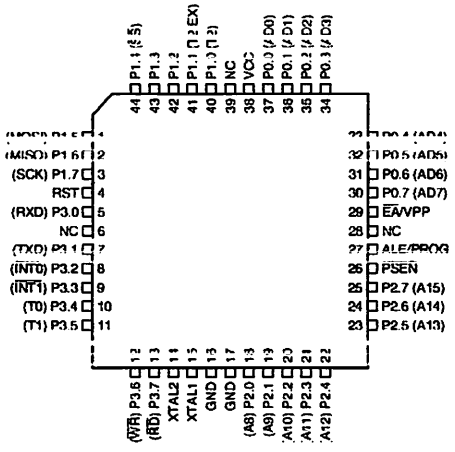
PDIP



PLCC



PQFP/TQFP



Description

ly voltage.

nd.

0

) is an 8-bit open drain bbi-didirectional I/O port. As an ut port, each pin can sink eight TTL inputs. When 1s vritten to port 0 pins, the pins can be used as high-dance inputs.

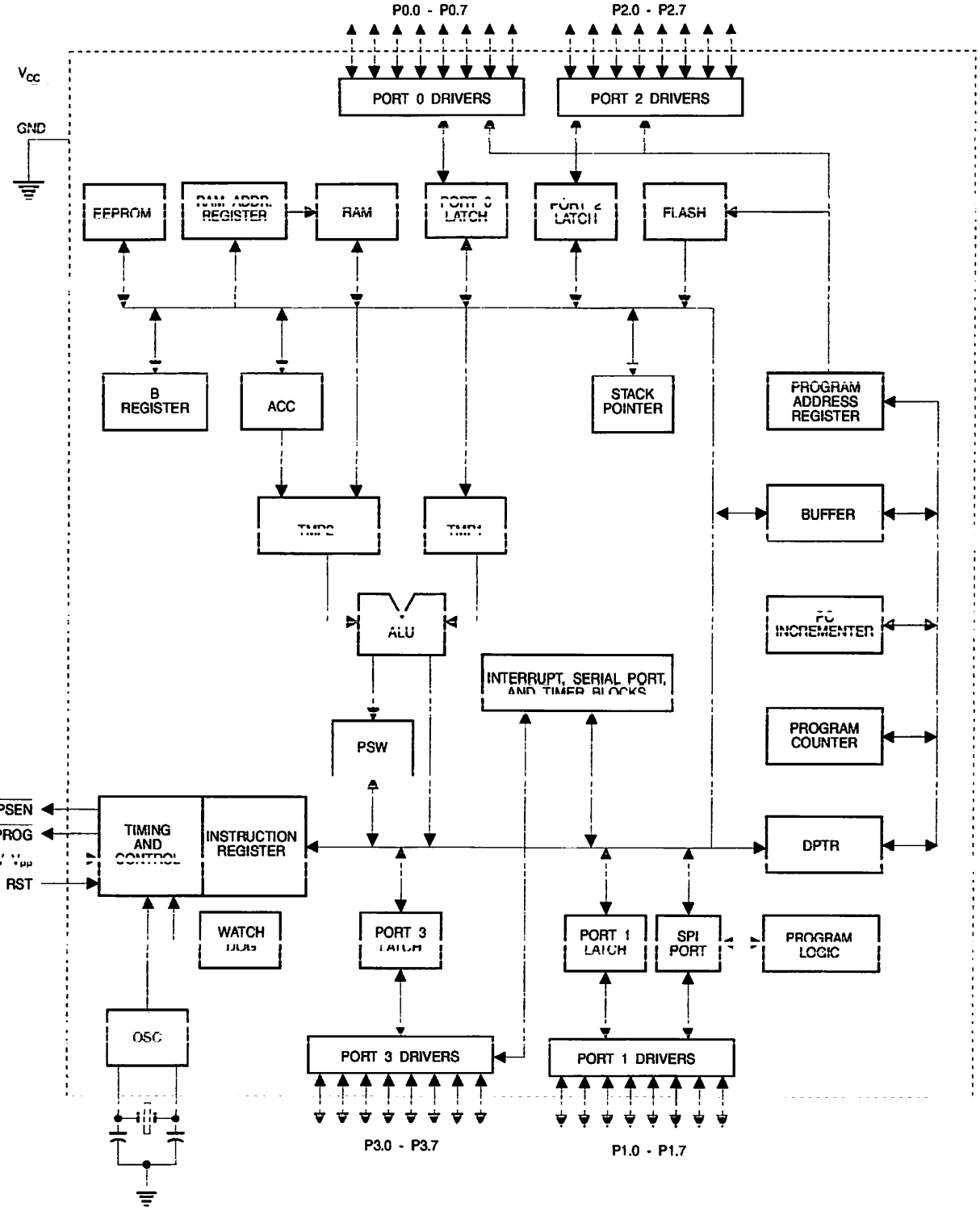
0 can also be configured to be the multiplexed low-r address/data bus during accesses to external program and data memory. In this mode, P0 has internal pullups.

Port 0 also receives the code bytes during Flash programming and outputs the code bytes during program verification. External pullups are required during program verification.

Port 1

Port 1 is an 8-bit bi-directional I/O port with internal pullups. The Port 1 output buffers can sink/source four TTL inputs. When 1s are written to Port 1 pins, they are pulled high by the internal pullups and can be used as inputs. As inputs, Port 1 pins that are externally being pulled low will source current (I_{IL}) because of the internal pullups.

ck Diagram


P0.0 - P0.7
P2.0 - P2.7
V_{CC}
GND
PORT 0 DRIVERS
PORT 2 DRIVERS
EEPROM
RAM
FLASH
B REGISTER
ACC
STACK POINTER
PROGRAM ADDRESS REGISTER
BUFFER
ALU
INTERRUPT, SERIAL PORT,
PSW
PROGRAM COUNTER
DPTR
PSEN
ALE/PROG
RST
TIMING AND
INSTRUCTION REGISTER
WATCH
PORT 3
PORT 1 LATCH
SPI PORT
PROGRAM LOGIC
OSC
PORT 3 DRIVERS
PORT 1 DRIVERS
P3.0 - P3.7
P1.0 - P1.7

e Port 1 pins provide additional functions. P1.0 and can be configured to be the timer/counter 2 external t input (P1.0/T2) and the timer/counter 2 trigger input /T2EX), respectively.

Description

ermore, P1.4, P1.5, P1.6, and P1.7 can be configured e SPI slave port select, data input/output and shift input/output pins as shown in the following table.

t Pin	Alternate Functions
)	T2 (external count input to Timer/Counter 2), clock-out
I	T2EX (Timer/Counter 2 capture/reload trigger and direction control)
;	$\overline{SS}$ (Slave port select input)
5	MOSI (Master data output, slave data input pin for SPI channel)
6	MISO (Master data input, slave data output pin for SPI channel)
'	SCK (Master clock output, slave clock input pin for SPI channel)

1 also receives the low-order address bytes during programming and verification.

2

2 is an 8-bit bi-directional I/O port with internal pullups. Port 2 output buffers can sink/source four TTL inputs. n 1s are written to Port 2 pins, they are pulled high by internal pullups and can be used as inputs. As inputs, 2 pins that are externally being pulled low will source nt (I_{IL}) because of the internal pullups.

2 emits the high order address byte during fetches external program memory and during accesses to nal data memory that use 16-bit addresses (MOVX @ R). In this application, Port 2 uses strong internal pul- when emitting 1s. During accesses to external data ory that use 8-bit addresses (MOVX @ RI), Port 2 the contents of the P2 Special Function Register.

2 also receives the high-order address bits and some ol signals during Flash programming and verification.

3

3 is an 8 bit bi-directional I/O port with internal pullups. Port 3 output buffers can sink/source four TTL inputs. n 1s are written to Port 3 pins, they are pulled high by ternal pullups and can be used as inputs. As inputs, Port 3 pins that are externally being pulled low will source current (I_{IL}) because of the pullups.

Port 3 also serves the functions of various special features of the AT89S8252, as shown in the following table.

Port 3 also receives some control signals for Flash programming and verification.

Port Pin	Alternate Functions
P3.0	RXD (serial input port)
P3.1	TXD (serial output port)
P3.2	$\overline{INT0}$ (external interrupt 0)
P3.3	$\overline{INT1}$ (external interrupt 1)
P3.4	T0 (timer 0 external input)
P3.5	T1 (timer 1 external input)
P3.6	$\overline{WR}$ (external data memory write strobe)
P3.7	$\overline{RD}$ (external data memory read strobe)

RST

Reset input. A high on this pin for two machine cycles while the oscillator is running resets the device.

ALE/$\overline{PROG}$

Address Latch Enable is an output pulse for latching the low byte of the address during accesses to external memory. This pin is also the program pulse input ($\overline{PROG}$) during Flash programming.

In normal operation, ALE is emitted at a constant rate of 1/6 the oscillator frequency and may be used for external timing or clocking purposes. Note, however, that one ALE pulse is skipped during each access to external data memory.

If desired, ALE operation can be disabled by setting bit 0 of SFR location 8EH. With the bit set, ALE is active only during a MOVX or MOVC instruction. Otherwise, the pin is weakly pulled high. Setting the ALE-disable bit has no effect if the microcontroller is in external execution mode.

$\overline{PSEN}$

Program Store Enable is the read strobe to external program memory.

When the AT89S8252 is executing code from external program memory, $\overline{PSEN}$ is activated twice each machine cycle, except that two PSEN activations are skipped during each access to external data memory.

$\overline{EA}$/VPP

External Access Enable. $\overline{EA}$ must be strapped to GND in order to enable the device to fetch code from external pro-

n memory locations starting at 0000H up to FFFFH. , however, that if lock bit 1 is programmed, $\overline{EA}$ will be nally latched on reset.

should be strapped to V_{CC} for internal program execu- s. This pin also receives the 12-volt programming ble voltage (V_{PP}) during Flash programming when 12- programming is selected.

XTAL1

Input to the inverting oscillator amplifier and input to the internal clock operating circuit.

XTAL2

Output from the inverting oscillator amplifier.

e 1. AT89S8252 SFR Map and Reset Values

8H								0FFH
0H	B 00000000							0F7H
8H								0EFH
0H	ACC 00000000							0E7H
8H								0DFH
0H	PSW 00000000					SPCR 000001XX		0D7H
8H	T2CON 00000000	T2MOD XXXXXX00	RCAP2L 00000000	RCAP2H 00000000	TL2 00000000	TH2 00000000		0CFH
0H								0C7H
8H	IP XX000000							0BFH
0H	P3 11111111							0B7H
8H	IE 0X000000		SPSR 00XXXXXX					0AFH
0H	P2 11111111							0A7H
8H	SCON 00000000	SBUF XXXXXXXX						9FH
0H	P1 11111111						WMCON 00000010	97H
8H	TCON 00000000	TMOD 00000000	TL0 00000000	TL1 00000000	TH0 00000000	TH1 00000000		8FH
0H	P0 11111111	SP 00000111	DP0L 00000000	DP0H 00000000	DP1L 00000000	DP1H 00000000	SPDR XXXXXXXX	PCON 0XXX0000	87H

ecial Function Registers

ip of the on-chip memory area called the Special Function Register (SFR) space is shown in Table 1.

that not all of the addresses are occupied, and unoc- ed addresses may not be implemented on the chip. l accesses to these addresses will in general return om data, and write accesses will have an indeterminate t.

software should not write 1s to these unlisted locations, since they may be used in future products to invoke new features. In that case, the reset or inactive values of the new bits will always be 0.

Timer 2 Registers Control and status bits are contained in registers T2CON (shown in Table 2) and T2MOD (shown in Table 9) for Timer 2. The register pair (RCAP2H, RCAP2L) are the Capture/Reload registers for Timer 2 in 16 bit capture mode or 16-bit auto-reload mode.

e 2. T2CON—Timer/Counter 2 Control Register

ON Address = 0C8H — Reset Value = 0000 0000B

ddressable

TF2	EXF2	RCLK	TCLK	EXEN2	TR2	C/$\overline{T2}$	CP/$\overline{RL2}$
7	6	5	4	3	2	1	0

bol	Function
	Timer 2 overflow flag set by a Timer 2 overflow and must be cleared by software. TF2 will not be set when either RCLK = 1 or TCLK = 1.
2	Timer 2 external flag set when either a capture or reload is caused by a negative transition on T2EX and EXEN2 = 1. When Timer 2 interrupt is enabled, EXF2 = 1 will cause the CPU to vector to the Timer 2 interrupt routine. EXF2 must be cleared by software. EXF2 does not cause an interrupt in up/down counter mode (DCEN = 1).
.K	Receive clock enable. When set, causes the serial port to use Timer 2 overflow pulses for its receive clock in serial port Modes 1 and 3. RCLK = 0 causes Timer 1 overflows to be used for the receive clock.
K	Transmit clock enable. When set, causes the serial port to use Timer 2 overflow pulses for its transmit clock in serial port Modes 1 and 3. TCLK = 0 causes Timer 1 overflows to be used for the transmit clock.
N2	Timer 2 external enable. When set, allows a capture or reload to occur as a result of a negative transition on T2EX if Timer 2 is not being used to clock the serial port. EXEN2 = 0 causes Timer 2 to ignore events at T2EX.
	Start/Stop control for Timer 2. TR2 = 1 starts the timer.
	Timer or counter select for Timer 2. C/$\overline{T2}$ = 0 for timer function. C/$\overline{T2}$ = 1 for external event counter (falling edge triggered).
RL2	Capture/Reload select. CP/$\overline{RL2}$ = 1 causes captures to occur on negative transitions at T2EX if EXEN2 = 1. CP/$\overline{RL2}$ = 0 causes automatic reloads to occur when Timer 2 overflows or negative transitions occur at T2EX when EXEN2 = 1. When either RCLK or TCLK = 1, this bit is ignored and the timer is forced to auto-reload on Timer 2 overflow.

:hdog and Memory Control Register The WMCON ;ter contains control bits for the Watchdog Timer vn in Table 3). The EEMEN and EEMWE bits are used to select the 2K bytes on-chip EEPROM, and to enable byte-write. The DPS bit selects one of two DPTR registers available.

e 3. WMCON—Watchdog and Memory Control Register

CON Address = 96H — Reset Value = 0000 0010B

PS2	PS1	PS0	EEMWE	EEMEN	DPS	WDTRST	WDTEN
7	6	5	4	3	2	1	0

ıbol	Function
	Prescaler Bits for the Watchdog Timer. When all three bits are set to "0", the watchdog timer has a nominal period of 16 ms. When all three bits are set to "1", the nominal period is 2048 ms.
MWE	EEPROM Data Memory Write Enable Bit. Set this bit to "1" before initiating byte write to on-chip EEPROM with the MOVX instruction. User software should set this bit to "0" after EEPROM write is completed.
MEN	Internal EEPROM Access Enable. When EEMEN = 1, the MOVX instruction with DPTR will access on-chip EEPROM instead of external data memory. When EEMEN = 0, MOVX with DPTR accesses external data memory.
	Data Pointer Register Select. DPS = 0 selects the first bank of Data Pointer Register, DP0, and DPS = 1 selects the second bank, DP1
TRST /BSY	Watchdog Timer Reset and EEPROM Ready/$\overline{\text{Busy}}$ Flag. Each time this bit is set to "1" by user software, a pulse is generated to reset the watchdog timer. The WDTRST bit is then automatically reset to "0" in the next instruction cycle. The WDTRST bit is Write-Only. This bit also serves as the RDY/$\overline{\text{BSY}}$ flag in a Read-Only mode during EEPROM write. RDY/$\overline{\text{BSY}}$ = 1 means that the EEPROM is ready to be programmed. While programming operations are being executed, the RDY/$\overline{\text{BSY}}$ bit equals "0" and is automatically reset to "1" when programming is completed.
TEN	Watchdog Timer Enable Bit. WDTEN = 1 enables the watchdog timer and WDTEN = 0 disables the watchdog timer.

legisters Control and status bits for the Serial Periph- nterface are contained in registers SPCR (shown in e 4) and SPSR (shown in Table 5). The SPI data bits ontained in the SPDR register. Writing the SPI data ter during serial data transfer sets the Write Collision /COL, in the SPSR register. The SPDR is double buff- for writing and the values in SPDR are not changed by t.

rupt Registers The global interrupt enable bit and the idual interrupt enable bits are in the IE register. In ion, the individual interrupt enable bit for the SPI is in PCR register. Two priorities can be set for each of the terrupt sources in the IP register.

Dual Data Pointer Registers To facilitate accessing both internal EEPROM and external data memory, two banks of 16 bit Data Pointer Registers are provided: DP0 at SFR address locations 82H-83H and DP1 at 84H-85H. Bit DPS = 0 in SFR WMCON selects DP0 and DPS = 1 selects DP1. The user should always initialize the DPS bit to the appropriate value before accessing the respective Data Pointer Register.

Power Off Flag The Power Off Flag (POF) is located at bit_4 (PCON.4) in the PCON SFR. POF is set to "1" during power up. It can be set and reset under software control and is not affected by RESET.

e 4. SPCR—SPI Control Register

CR Address = D5H — Reset Value = 0000 01XXB

SPIE	SPE	DORD	MSTR	CPOL	CPHA	SPR1	SPR0
7	6	5	4	3	2	1	0

ıbol	Function
=	SPI Interrupt Enable. This bit, in conjunction with the ES bit in the IE register, enables SPI interrupts. SPIE = 1 and ES = 1 enable SPI interrupts. SPIE = 0 disables SPI interrupts.
:	SPI Enable. SPI = 1 enables the SPI channel and connects $\overline{SS}$, MOSI, MISO and SCK to pins P1.4, P1.5, P1.6, and P1.7. SPI = 0 disables the SPI channel.
RD	Data Order. DORD = 1 selects LSB first data transmission. DORD = 0 selects MSB first data transmission.
TR	Master/Slave Select. MSTR = 1 selects Master SPI mode. MSTR = 0 selects Slave SPI mode.
)L	Clock Polarity. When CPOL = 1, SCK is high when idle. When CPOL = 0, SCK of the master device is low when not transmitting. Please refer to figure on SPI Clock Phase and Polarity Control.
HA	Clock Phase. The CPHA bit together with the CPOL bit controls the clock and data relationship between master and slave. Please refer to figure on SPI Clock Phase and Polarity Control.
R0 R1	SPI Clock Rate Select. These two bits control the SCK rate of the device configured as master. SPR1 and SPR0 have no effect on the slave. The relationship between SCK and the oscillator frequency, F_{osc}, is as follows: SPR1SPR0 SCK = F_{osc} divided by 0 0 4 0 1 16 1 0 64 1 1 128

e 5. SPSR – SPI Status Register

SR Address = AAH — Reset Value = 00XX XXXXB

SPIF	WCOL	–	–	–	–	–	–
7	6	5	4	3	2	1	0

ıbol	Function
F	SPI Interrupt Flag. When a serial transfer is complete, the SPIF bit is set and an interrupt is generated if SPIE = 1 and ES = 1. The SPIF bit is cleared by reading the SPI status register with SPIF and WCOL bits set, and then accessing the SPI data register.
OL	Write Collision Flag. The WCOL bit is set if the SPI data register is written during a data transfer. During data transfer, the result of reading the SPDR register may be incorrect, and writing to it has no effect. The WCOL bit (and the SPIF bit) are cleared by reading the SPI status register with SPIF and WCOL set, and then accessing the SPI data register.

e 6. SPDR – SPI Data Register

DR Address = 86H — Reset Value = unchanged

SPD7	SPD6	SPD5	SPD4	SPD3	SPD2	SPD1	SPD0
7	6	5	4	3	2	1	0

ta Memory – EEPROM and RAM

AT89S8252 implements 2K bytes of on-chip EEPROM ata storage and 256 bytes of RAM. The upper 128 s of RAM occupy a parallel space to the Special Func- Registers. That means the upper 128 bytes have the e addresses as the SFR space but are physically sepa- from SFR space.

n an instruction accesses an internal location above ess 7FH, the address mode used in the instruction ifies whether the CPU accesses the upper 128 bytes AM or the SFR space. Instructions that use direct essing access SFR space.

example, the following direct addressing instruction sses the SFR at location 0A0H (which is P2).

```
MOV 0A0H, #data
```

uctions that use indirect addressing access the upper bytes of RAM. For example, the following indirect essing instruction, where R0 contains 0A0H, accesses lata byte at address 0A0H, rather than P2 (whose ess is 0A0H).

```
MOV @R0, #data
```

that stack operations are examples of indirect essing, so the upper 128 bytes of data RAM are avail- as stack space.

on-chip EEPROM data memory is selected by setting EEMEN bit in the WMCON register at SFR address ion 96H. The EEPROM address range is from 000H to H. The MOVX instructions are used to access the ROM. To access off-chip data memory with the MOVX uctions, the EEMEN bit needs to be set to "0".

EEMWE bit in the WMCON register needs to be set to efore any byte location in the EEPROM can be written. software should reset EEMWE bit to "0" if no further ROM write is required. EEPROM write cycles in the l programming mode are self-timed and typically take is. The progress of EEPROM write can be monitored ading the RDY/$\overline{BSY}$ bit (read-only) in SFR WMCON. $\overline{BSY}$ = 0 means programming is still in progress and $\overline{BSY}$ = 1 means EEPROM write cycle is completed nother write cycle can be initiated.

dition, during EEPROM programming, an attempted from the EEPROM will fetch the byte being written he MSB complemented. Once the write cycle is com- d, true data are valid at all bit locations.

grammable Watchdog Timer

rogrammable Watchdog Timer (WDT) operates from dependent oscillator. The prescaler bits, PS0, PS1 S2 in SFR WMCON are used to set the period of the hdog Timer from 16 ms to 2048 ms. The available periods are shown in the following table and the actual timer periods (at V_{CC} = 5V) are within ±30% of the nominal.

The WDT is disabled by Power-on Reset and during Power-down. It is enabled by setting the WDTEN bit in SFR WMCON (address = 96H). The WDT is reset by setting the WDTRST bit in WMCON. When the WDT times out without being reset or disabled, an internal RST pulse is generated to reset the CPU.

Table 7. Watchdog Timer Period Selection

WDT Prescaler Bits			
PS2	PS1	PS0	Period (nominal)
0	0	0	16 ms
0	0	1	32 ms
0	1	0	64 ms
0	1	1	128 ms
1	0	0	256 ms
1	0	1	512 ms
1	1	0	1024 ms
1	1	1	2048 ms

Timer 0 and 1

Timer 0 and Timer 1 in the AT89S8252 operate the same way as Timer 0 and Timer 1 in the AT89C51, AT89C52 and AT89C55. For further information, see the October 1995 Microcontroller Data Book, page 2-45, section titled, "Timer/Counters."

Timer 2

Timer 2 is a 16 bit Timer/Counter that can operate as either a timer or an event counter. The type of operation is selected by bit C/$\overline{T2}$ in the SFR T2CON (shown in Table 2). Timer 2 has three operating modes: capture, auto-reload (up or down counting), and baud rate generator. The modes are selected by bits in T2CON, as shown in Table 8.

Timer 2 consists of two 8-bit registers, TH2 and TL2. In the Timer function, the TL2 register is incremented every machine cycle. Since a machine cycle consists of 12 oscillator periods, the count rate is 1/12 of the oscillator frequency.

In the Counter function, the register is incremented in response to a 1-to-0 transition at its corresponding external input pin, T2. In this function, the external input is sampled during S5P2 of every machine cycle. When the samples show a high in one cycle and a low in the next cycle, the count is incremented. The new count value appears in the register during S3P1 of the cycle following the one in which

ransition was detected. Since two machine cycles (24 lator periods) are required to recognize a 1-to-0 transi- the maximum count rate is 1/24 of the oscillator iency. To ensure that a given level is sampled at least before it changes, the level should be held for at least ull machine cycle.

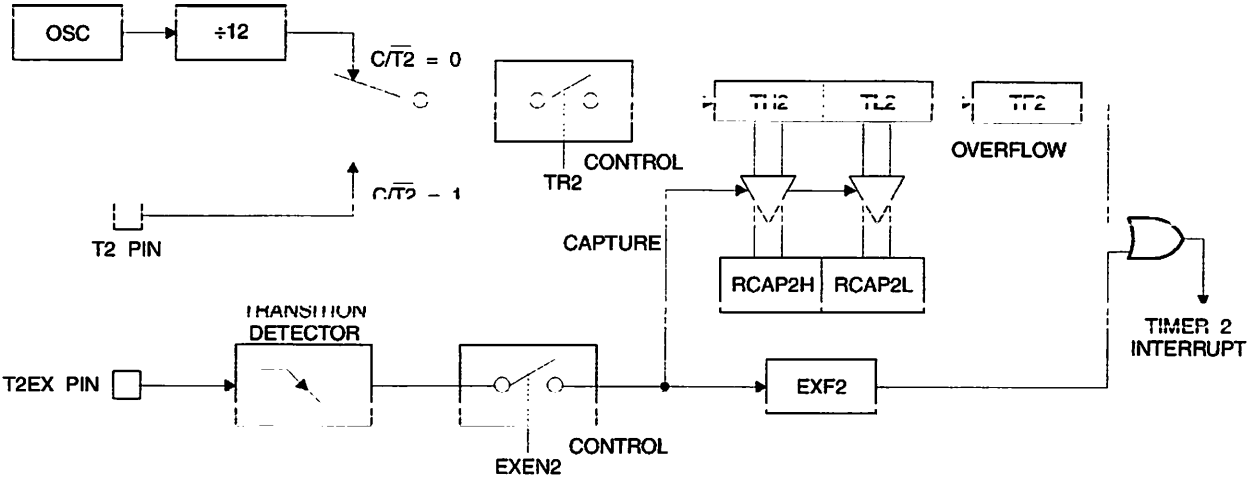
e 8. Timer 2 Operating Modes

LK + TCLK	CP/RL2	TR2	MODE
0	0	1	16-bit Auto-reload
0	1	1	16-bit Capture
1	X	1	Baud Rate Generator
X	X	0	(Off)

Capture Mode

In the capture mode, two options are selected by bit EXEN2 in T2CON. If EXEN2 = 0. Timer 2 is a 16 bit timer or counter which upon overflow sets bit TF2 in T2CON. This bit can then be used to generate an interrupt. If EXEN2 = 1, Timer 2 performs the same operation, but a 1-to-0 transition at external input T2EX also causes the current value in TH2 and TL2 to be captured into RCAP2H and RCAP2L, respectively. In addition, the transition at T2EX causes bit EXF2 in T2CON to be set. The EXF2 bit, like TF2, can generate an interrupt. The capture mode is illustrated in Figure 1.

re 1. Timer 2 in Capture Mode



o-reload (Up or Down Counter)

ır 2 can be programmed to count up or down when igured in its 16 bit auto-reload mode. This feature is ted by the DCEN (Down Counter Enable) bit located in SFR T2MOD (see Table 9). Upon reset, the DCEN bit t to 0 so that timer 2 will default to count up. When N is set, Timer 2 can count up or down, depending on alue of the T2EX pin.

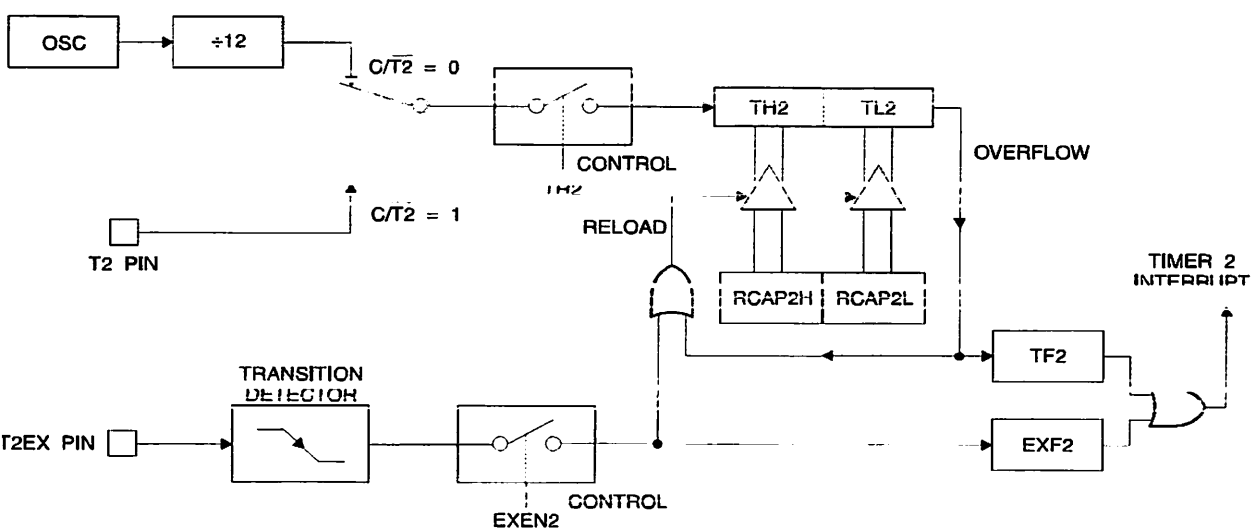
re 2 shows Timer 2 automatically counting up when N = 0. In this mode, two options are selected by bit N2 in T2CON. If EXEN2 = 0, Timer 2 counts up to FFH and then sets the TF2 bit upon overflow. The low also causes the timer registers to be reloaded with 6 bit value in RCAP2H and RCAP2L. The values in P2H and RCAP2L are preset by software. If EXEN2 = 16 bit reload can be triggered either by an overflow or by a 1-to-0 transition at external input T2EX. This transition also sets the EXF2 bit. Both the TF2 and EXF2 bits can generate an interrupt if enabled.

Setting the DCEN bit enables Timer 2 to count up or down, as shown in Figure 3. In this mode, the T2EX pin controls the direction of the count. A logic 1 at T2EX makes Timer 2 count up. The timer will overflow at 0FFFFH and set the TF2 bit. This overflow also causes the 16 bit value in RCAP2H and RCAP2L to be reloaded into the timer registers, TH2 and TL2, respectively.

A logic 0 at T2EX makes Timer 2 count down. The timer underflows when TH2 and TL2 equal the values stored in RCAP2H and RCAP2L. The underflow sets the TF2 bit and causes 0FFFFH to be reloaded into the timer registers.

The EXF2 bit toggles whenever Timer 2 overflows or underflows and can be used as a 17th bit of resolution. In this operating mode, EXF2 does not flag an interrupt.

re 2. Timer 2 in Auto Reload Mode (DCEN = 0)



9. T2MOD Timer 2 Mode Control Register

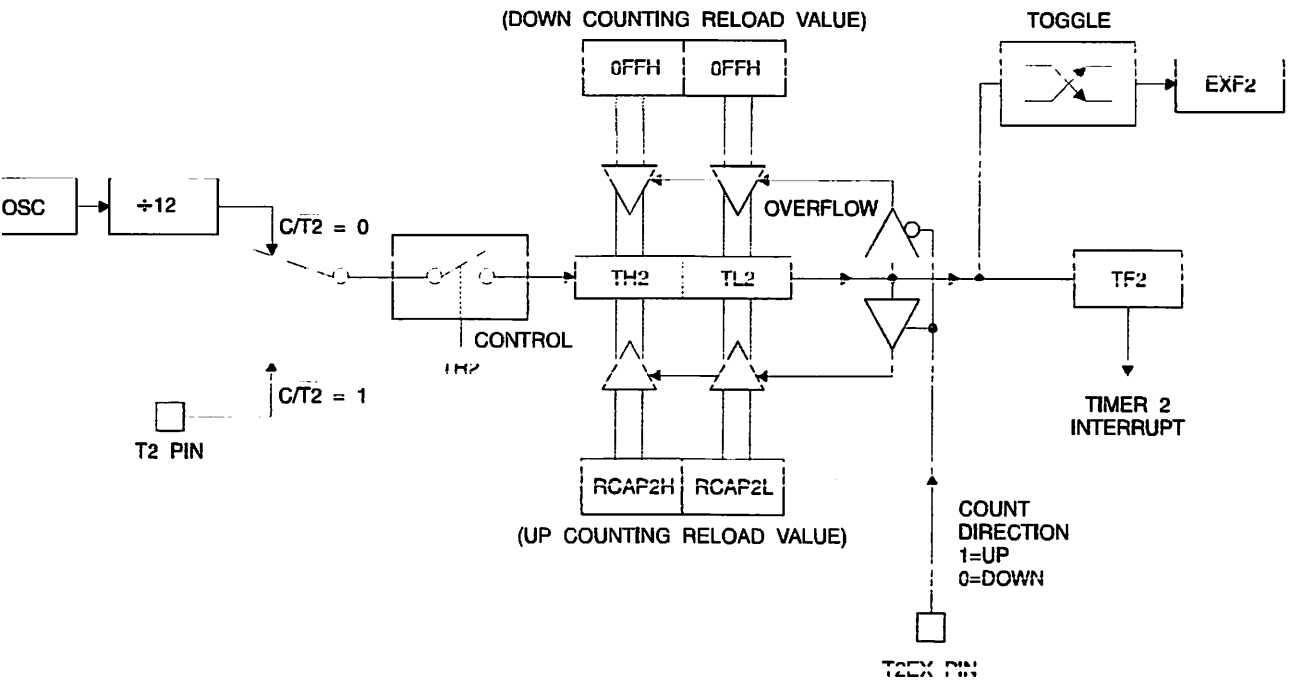
OD Address = 0C9H — Reset Value = XXXX XX00B

Bit Addressable

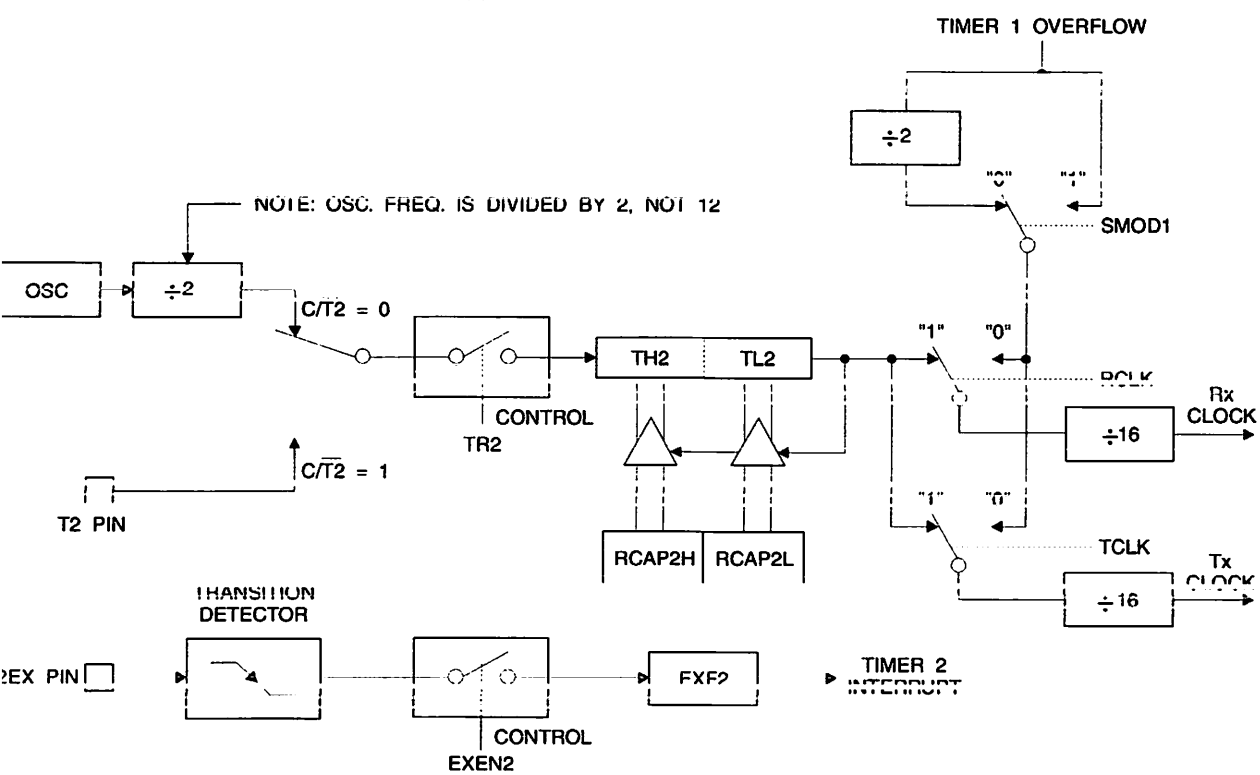
–	–	–	–	–	–	T2OE	DCEN
7	6	5	4	3	2	1	0

bol	Function
	Not implemented, reserved for future use.
E	Timer 2 Output Enable bit.
N	When set, this bit allows Timer 2 to be configured as an up/down counter.

re 3. Timer 2 Auto Reload Mode (DCEN = 1)



re 4. Timer 2 in Baud Rate Generator Mode



ıd Rate Generator

ır 2 is selected as the baud rate generator by setting K and/or RCLK in T2CON (Table 2). Note that the i rates for transmit and receive can be different if Timer ısed for the receiver or transmitter and Timer 1 is used ne other function. Setting RCLK and/or TCLK puts r 2 into its baud rate generator mode, as shown in Fig-

baud rate generator mode is similar to the auto-reload e, in that a rollover in TH2 causes the Timer 2 registers reloaded with the 16 bit value in registers RCAP2H RCAP2L, which are preset by software.

baud rates in Modes 1 and 3 are determined by Timer verflow rate according to the following equation.

$$\text{Modes 1 and 3 Baud Rates} = \frac{\text{Timer 2 Overflow Rate}}{16}$$

Timer can be configured for either timer or counter ation. In most applications, it is configured for timer ation ($C/\overline{T2} = 0$). The timer operation is different for r 2 when it is used as a baud rate generator. Normally, timer, it increments every machine cycle (at 1/12 the ator frequency). As a baud rate generator, however, it ements every state time (at 1/2 the oscillator fre-cv). The baud rate formula is given below.

$$\frac{\text{Modes 1 and 3}}{\text{Baud Rate}} = \frac{\text{Oscillator Frequency}}{32 \times [65536 - (\text{RCAP2H,RCAP2L})]}$$

e (RCAP2H, RCAP2L) is the content of RCAP2H and P2L taken as a 16 bit unsigned integer.

r 2 as a baud rate generator is shown in Figure 4. This e is valid only if RCLK or TCLK = 1 in T2CON. Note a rollover in TH2 does not set TF2 and will not gener-n interrupt. Note too, that if EXEN2 is set, a 1-to-0 ition in T2EX will set EXF2 but will not cause a reload (RCAP2H, RCAP2L) to (TH2, TL2). Thus when Timer 2 is in use as a baud rate generator, T2EX can be used as an extra external interrupt.

Note that when Timer 2 is running (TR2 = 1) as a timer in the baud rate generator mode, TH2 or TL2 should not be read from or written to. Under these conditions, the Timer is incremented every state time, and the results of a read or write may not be accurate. The RCAP2 registers may be read but should not be written to, because a write might overlap a reload and cause write and/or reload errors. The timer should be turned off (clear TR2) before accessing the Timer 2 or RCAP2 registers.

Programmable Clock Out

A 50% duty cycle clock can be programmed to come out on P1.0, as shown in Figure 5. This pin, besides being a regular I/O pin, has two alternate functions. It can be programmed to input the external clock for Timer/Counter 2 or to output a 50% duty cycle clock ranging from 61 Hz to 4 MHz at a 16 MHz operating frequency.

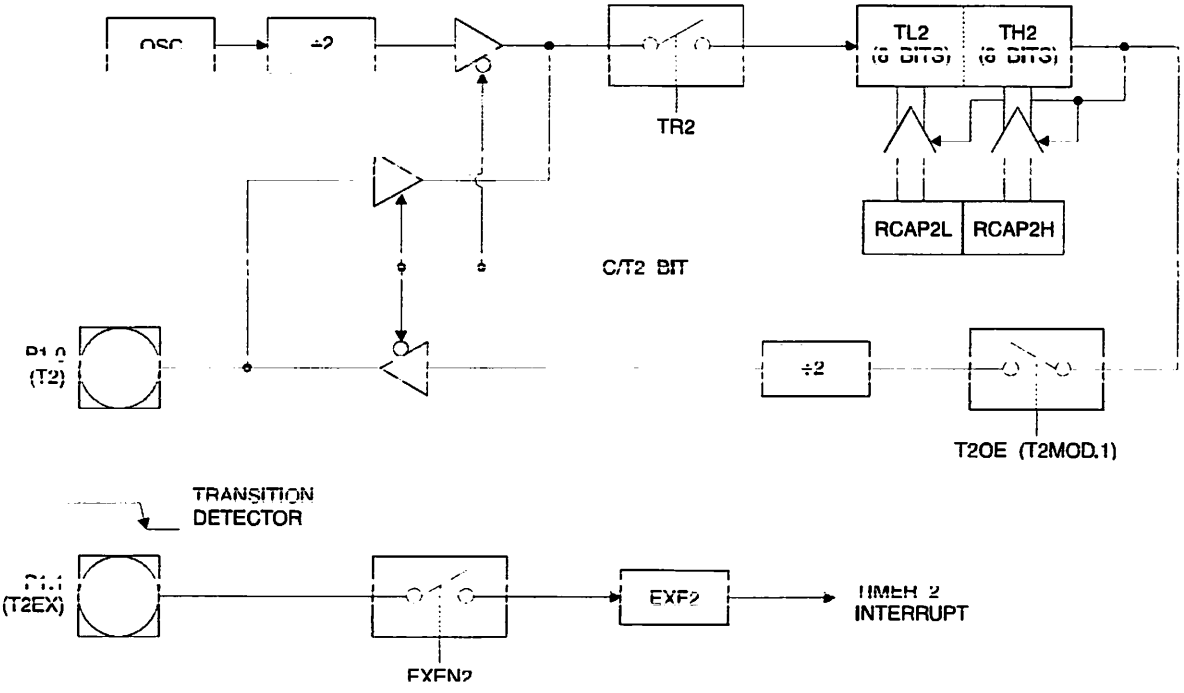
To configure the Timer/Counter 2 as a clock generator, bit $C/\overline{T2}$ (T2CON.1) must be cleared and bit T2OE (T2MOD.1) must be set. Bit TR2 (T2CON.2) starts and stops the timer.

The clock-out frequency depends on the oscillator frequency and the reload value of Timer 2 capture registers (RCAP2H, RCAP2L), as shown in the following equation.

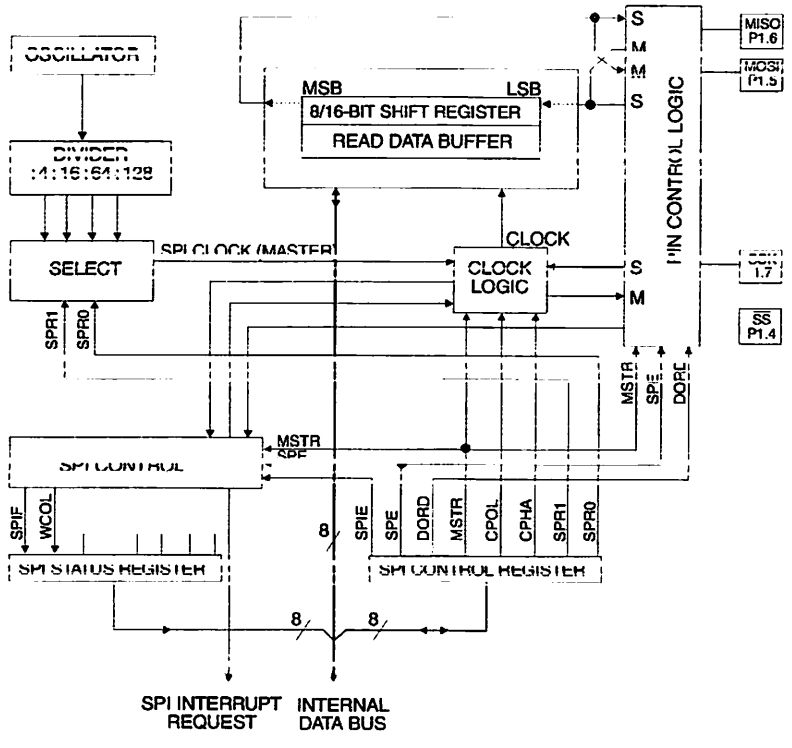
$$\text{Clock-Out Frequency} = \frac{\text{Oscillator Frequency}}{4 \times [65536 - (\text{RCAP2H,RCAP2L})]}$$

In the clock-out mode, Timer 2 rollovers will not generate an interrupt. This behavior is similar to when Timer 2 is used as a baud-rate generator. It is possible to use Timer 2 as a baud-rate generator and a clock generator simultaneously. Note, however, that the baud-rate and clock-out frequencies cannot be determined independently from one another since they both use RCAP2H and RCAP2L.

re 5. Timer 2 in Clock-out Mode



re 6. SPI Block Diagram



RT

UART in the AT89S8252 operates the same way as
UART in the AT89C51, AT89C52 and AT89C55. For
er information, see the October 1995 Microcontroller
Book, page 2-49, section titled, "Serial Interface."

ial Peripheral Interface

serial peripheral interface (SPI) allows high-speed syn-
nous data transfer between the AT89S8252 and
pheral devices or between several AT89S8252
ces. The AT89S8252 SPI features include the
wing:

ll-Duplex, 3-Wire Synchronous Data Transfer
ister or Slave Operation
MHz Bit Frequency (max.)
B First or MSB First Data Transfer
ur Programmable Bit Rates
d of Transmission Interrupt Flag

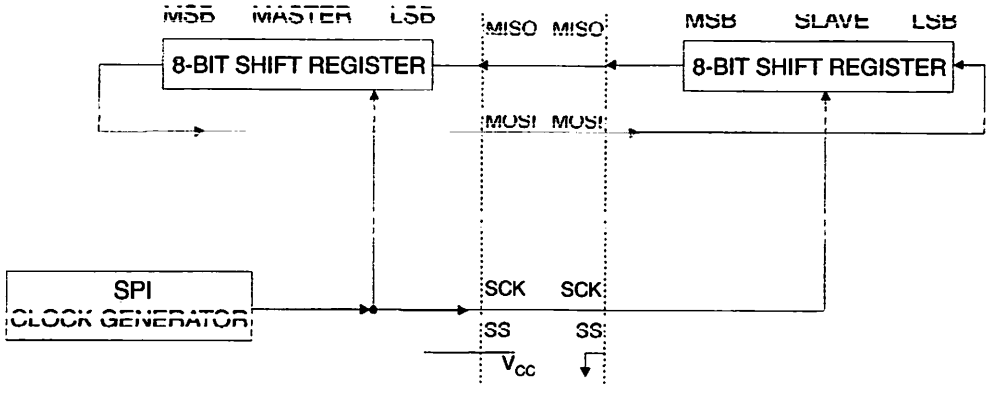
- Write Collision Flag Protection
- Wakeup from Idle Mode (Slave Mode Only)

The interconnection between master and slave CPUs with SPI is shown in the following figure. The SCK pin is the clock output in the master mode but is the clock input in the slave mode. Writing to the SPI data register of the master CPU starts the SPI clock generator, and the data written shifts out of the MOSI pin and into the MOSI pin of the slave CPU. After shifting one byte, the SPI clock generator stops, setting the end of transmission flag (SPIF). If both the SPI interrupt enable bit (SPIE) and the serial port interrupt enable bit (ES) are set, an interrupt is requested.

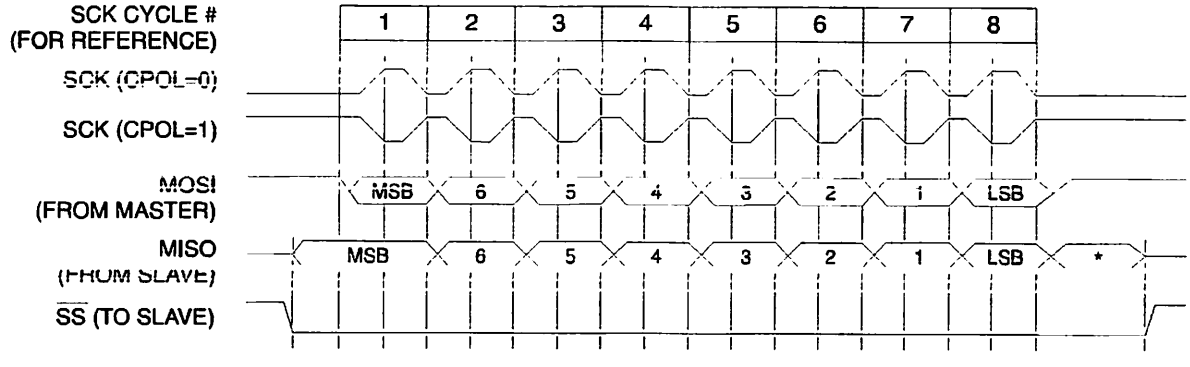
The Slave Select input, $\overline{SS}$/P1.4, is set low to select an individual SPI device as a slave. When $\overline{SS}$/P1.4 is set high, the SPI port is deactivated and the MOSI/P1.5 pin can be used as an input.

There are four combinations of SCK phase and polarity with respect to serial data, which are determined by control bits CPHA and CPOL. The SPI data transfer formats are shown in Figure 8 and Figure 9.

re 7. SPI Master-slave Interconnection

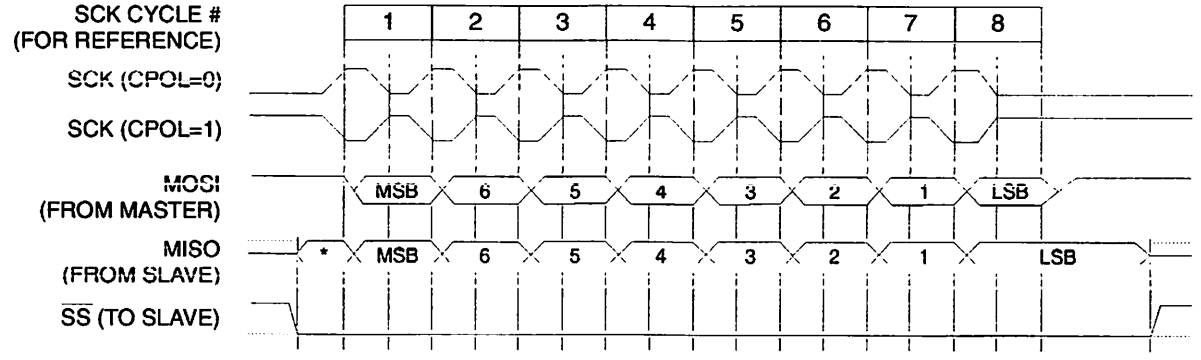


e 8. SPI transfer Format with CPHA = 0



defined but normally MSB of character just received

re 9. SPI Transfer Format with CPHA = 1



defined but normally LSB of previously transmitted character

rrupts

AT89S8252 has a total of six interrupt vectors: two nal interrupts (INT0 and INT1), three timer interrupts ers 0, 1, and 2), and the serial port interrupt. These upts are all shown in Figure 10.

of these interrupt sources can be individually enabled abled by setting or clearing a bit in Special Function ster IE. IE also contains a global disable bit, EA, which les all interrupts at once.

that Table 10 shows that bit position IE.6 is unimple- ted. In the AT89C51, bit position IE.5 is also plemented. User software should not write 1s to these positions, since they may be used in future AT89 ucts.

r 2 interrupt is generated by the logical OR of bits TF2 EXF2 in register T2CON. Neither of these flags is ed by hardware when the service routine is vectored fact, the service routine may have to determine ner it was TF2 or EXF2 that generated the interrupt, hat bit will have to be cleared in software.

Timer 0 and Timer 1 flags, TF0 and TF1, are set at of the cycle in which the timers overflow. The values len polled by the circuitry in the next cycle. However, imer 2 flag, TF2, is set at S2P2 and is polled in the cycle in which the timer overflows.

Table 10. Interrupt Enable (IE) Register

(MSB)(LSB)

EA	–	ET2	ES	ET1	EX1	ET0	EX0

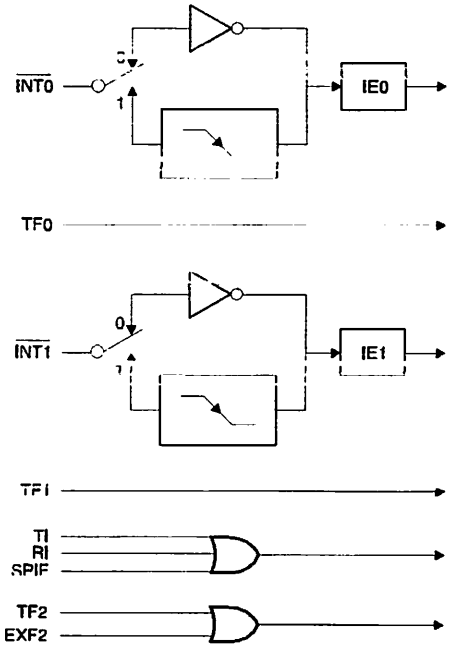
Enable Bit = 1 enables the interrupt.

Enable Bit = 0 disables the interrupt.

Symbol	Position	Function
EA	IE.7	Disables all interrupts. If EA = 0, no interrupt is acknowledged. If EA = 1, each interrupt source is individually enabled or disabled by setting or clearing its enable bit.
–	IE.6	Reserved.
ET2	IE.5	Timer 2 interrupt enable bit.
ES	IE.4	SPI and UART interrupt enable bit.
ET1	IE.3	Timer 1 interrupt enable bit.
EX1	IE.2	External interrupt 1 enable bit.
ET0	IE.1	Timer 0 interrupt enable bit.
EX0	IE.0	External interrupt 0 enable bit.

User software should never write 1s to unimplemented bits, because they may be used in future AT89 products.

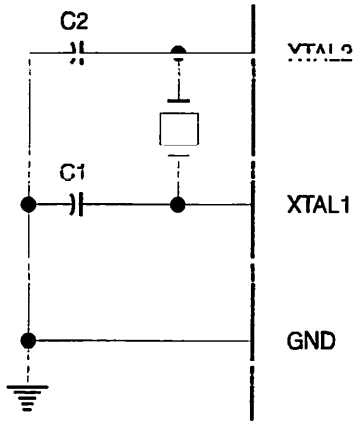
re 10. Interrupt Sources



cillator Characteristics

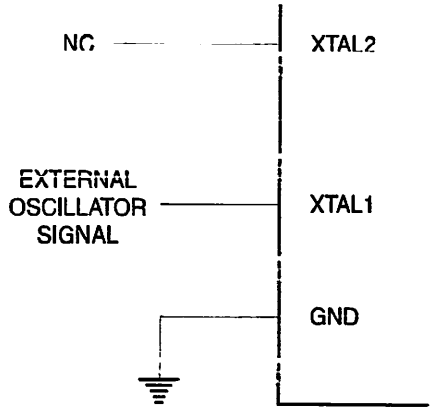
.1 and XTAL2 are the input and output, respectively, inverting amplifier that can be configured for use as i-chip oscillator, as shown in Figure 11. Either a quartz al or ceramic resonator may be used. To drive the e from an external clock source, XTAL2 should be left nnected while XTAL1 is driven, as shown in Figure 12. are no requirements on the duty cycle of the external signal, since the input to the internal clocking circuitry ough a divide-by-two flip-flop, but minimum and maxi- voltage high and low time specifications must be ved.

Figure 11. Oscillator Connections



Note: Note: C1, C2 = 30 pF ± 10 pF for Crystals
= 40 pF ± 10 pF for Ceramic Resonators

Figure 12. External Clock Drive Configuration



Mode

e mode, the CPU puts itself to sleep while all the on-peripherals remain active. The mode is invoked by are. The content of the on-chip RAM and all the special functions registers remain unchanged during this e. The idle mode can be terminated by any enabled upt or by a hardware reset.

that when idle mode is terminated by a hardware , the device normally resumes program execution from where it left off, up to two machine cycles before the internal reset algorithm takes control. On-chip hardware inhibits access to internal RAM in this event, but access to the port pins is not inhibited. To eliminate the possibility of an unexpected write to a port pin when idle mode is terminated by a reset, the instruction following the one that invokes idle mode should not write to a port pin or to external memory.

tus of External Pins During Idle and Power-down Modes

le	Program Memory	ALE	$\overline{PSEN}$	PORT0	PORT1	PORT2	PORT3
	Internal	1	1	Data	Data	Data	Data
	External	1	1	Float	Data	Address	Data
or down	Internal	0	0	Data	Data	Data	Data
er-down	External	0	0	Float	Data	Data	Data

ver-down Mode

power-down mode, the oscillator is stopped and the ction that invokes power-down is the last instruction uted. The on-chip RAM and Special Function Registers retain their values until the power-down mode is nated. Exit from power-down can be initiated either by ware reset or by an enabled external interrupt. Reset ines the SFRs but does not change the on-chip RAM. eset should not be activated before V_{CC} is restored to rmal operating level and must be held active long gh to allow the oscillator to restart and stabilize.

it power-down via an interrupt, the external interrupt be enabled as level sensitive before entering power-. The interrupt service routine starts at 16 ms (nomi-fter the enabled interrupt pin is activated.

Program Memory Lock Bits

The AT89S8252 has three lock bits that can be left unprogrammed (U) or can be programmed (P) to obtain the additional features listed in the following table.

When lock bit 1 is programmed, the logic level at the $\overline{EA}$ pin is sampled and latched during reset. If the device is powered up without a reset, the latch initializes to a random value and holds that value until reset is activated. The latched value of $\overline{EA}$ must agree with the current logic level at that pin in order for the device to function properly.

Once programmed, the lock bits can only be unprogrammed with the Chip Erase operations in either the parallel or serial modes.

k Bit Protection Modes[1][2]

Program Lock Bits			
LB1	LB2	LB3	Protection Type
U	U	U	No internal memory lock feature.
P	U	U	MOVC instructions executed from external program memory are disabled from fetching code bytes from internal memory. $\overline{EA}$ is sampled and latched on reset and further programming of the Flash memory (parallel or serial mode) is disabled.
P	P	U	Same as Mode 2, but parallel or serial verify are also disabled.
P	P	P	Same as Mode 3, but external execution is also disabled.

1. U = Unprogrammed
2. P = Programmed

gramming the Flash and EEPROM

l's AT89S8252 Flash Microcontroller offers 8K bytes
system reprogrammable Flash Code memory and 2K
of EEPROM Data memory.

AT89S8252 is normally shipped with the on-chip Flash
and EEPROM Data memory arrays in the erased
(i.e. contents = FFH) and ready to be programmed.
device supports a High-voltage (12V) Parallel pro-
ming mode and a Low-voltage (5V) Serial
amming mode. The serial programming mode pro-
a convenient way to download the AT89S8252 inside
ser's system. The parallel programming mode is com-
le with conventional third party Flash or EPROM
ammers.

Code and Data memory arrays are mapped via sepa-
address spaces in the serial programming mode. In
arallel programming mode, the two arrays occupy one
guous address space: 0000H to 1FFFH for the Code
and 2000H to 27FFH for the Data array.

Code and Data memory arrays on the AT89S8252 are
ammed byte-by-byte in either programming mode. An
erase cycle is provided with the self-timed program-
operation in the serial programming mode. There is
ed to perform the Chip Erase operation to reprogram
nemory location in the serial programming mode
s any of the lock bits have been programmed.

parallel programming mode, there is no auto-erase
. To reprogram any non-blank byte, the user needs to
ne Chip Erase operation first to erase both arrays.

iel Programming Algorithm: To program and verify
T89S8252 in the parallel programming mode, the fol-
g sequence is recommended:

ower-up sequence:

pply power between V_{CC} and GND pins.

et RST pin to "H".

pply a 3 MHz to 24 MHz clock to XTAL1 pin and wait
r at least 10 milliseconds.

et $\overline{PSEN}$ pin to "L"

LE pin to "H"

$\overline{A}$ pin to "H" and all other pins to "H".

pply the appropriate combination of "H" or "L" logic
vels to pins P2.6, P2.7, P3.6, P3.7 to select one of
ne programming operations shown in the Flash
rogramming Modes table.

pply the desired byte address to pins P1.0 to P1.7
nd P2.0 to P2.5.

pply data to pins P0.0 to P0.7 for Write Code
peration.

5. Raise $\overline{EA}/V_{PP}$ to 12V to enable Flash programming, erase or verification.
6. Pulse ALE/$\overline{PROG}$ once to program a byte in the Code memory array, the Data memory array or the lock bits. The byte-write cycle is self-timed and typically takes 1.5 ms.
7. To verify the byte just programmed, bring pin P2.7 to "L" and read the programmed data at pins P0.0 to P0.7.
8. Repeat steps 3 through 7 changing the address and data for the entire 2K or 8K bytes array or until the end of the object file is reached.
9. Power-off sequence:

   Set XTAL1 to "L".

   Set RST and $\overline{EA}$ pins to "L".

   Turn V_{CC} power off.

In the parallel programming mode, there is no auto-erase cycle and to reprogram any non-blank byte, the user needs to use the Chip Erase operation first to erase both arrays.

$\overline{Data}$ Polling: The AT89S8252 features $\overline{DATA}$ Polling to indicate the end of a write cycle. During a write cycle in the parallel or serial programming mode, an attempted read of the last byte written will result in the complement of the written datum on P0.7 (parallel mode), and on the MSB of the serial output byte on MISO (serial mode). Once the write cycle has been completed, true data are valid on all outputs, and the next cycle may begin. $\overline{DATA}$ Polling may begin any time after a write cycle has been initiated.

Ready/$\overline{Busy}$: The progress of byte programming in the parallel programming mode can also be monitored by the RDY/$\overline{BSY}$ output signal. Pin P3.4 is pulled Low after ALE goes High during programming to indicate $\overline{BUSY}$. P3.4 is pulled High again when programming is done to indicate READY.

Program Verify: If lock bits LB1 and LB2 have not been programmed, the programmed Code or Data byte can be read back via the address and data lines for verification. The state of the lock bits can also be verified directly in the parallel programming mode. In the serial programming mode, the state of the lock bits can only be verified indirectly by observing that the lock bit features are enabled.

Chip Erase: Both Flash and EEPROM arrays are erased electrically at the same time. In the parallel programming mode, chip erase is initiated by using the proper combination of control signals and by holding ALE/$\overline{PROG}$ low for 10 ms. The Code and Data arrays are written with all "1"s in the Chip Erase operation.

e serial programming mode, a chip erase operation is ed by issuing the Chip Erase instruction. In this mode, erase is self-timed and takes about 16 ms.

ig chip erase, a serial read from any address location eturn 00H at the data outputs.

il Programming Fuse: A programmable fuse is avail- to disable Serial Programming if the user needs mum system security. The Serial Programming Fuse nly be programmed or erased in the Parallel Program- Mode.

AT89S8252 is shipped with the Serial Programming e enabled.

ling the Signature Bytes: The signature bytes are by the same procedure as a normal verification of ons 030H and 031H, except that P3.6 and P3.7 must illed to a logic low. The values returned are as follows:

030H) = 1EH indicates manufactured by Atmel
031H) = 72H indicates 89S8252

gramming Interface

r code byte in the Flash and EEPROM arrays can be n, and the entire array can be erased, by using the priate combination of control signals. The write oper- cycle is self-timed and once initiated, will natically time itself to completion.

ajor programming vendors offer worldwide support for tmel microcontroller series. Please contact your local amming vendor for the appropriate software revision.

ial Downloading

The Code and Data memory arrays can be pro- med using the serial SPI bus while RST is pulled to he serial interface consists of pins SCK, MOSI (input) MISO (output). After RST is set high, the Programming le instruction needs to be executed first before pro- erase operations can be executed.

ito-erase cycle is built into the self-timed programming tion (in the serial mode ONLY) and there is no need t execute the Chip Erase instruction unless any of the its have been programmed. The Chip Erase opera- ms the content of every memory location in both the and Data arrays into FFH.

Code and Data memory arrays have separate address s:

0000H to 1FFFH for Code memory and 000H to 7FFH for Data memory.

Either an external system clock is supplied at pin XTAL1 or a crystal needs to be connected across pins XTAL1 and XTAL2. The maximum serial clock (SCK) frequency should be less than 1/40 of the crystal frequency. With a 24 MHz oscillator clock, the maximum SCK frequency is 600 kHz.

Serial Programming Algorithm

To program and verify the AT89S8252 in the serial programming mode, the following sequence is recommended:

1. Power-up sequence:
   Apply power between VCC and GND pins.
   Set RST pin to "H".
   If a crystal is not connected across pins XTAL1 and XTAL2, apply a 3 MHz to 24 MHz clock to XTAL1 pin and wait for at least 10 milliseconds.
2. Enable serial programming by sending the Programming Enable serial instruction to pin MOSI/P1.5. The frequency of the shift clock supplied at pin SCK/P1.7 needs to be less than the CPU clock at XTAL1 divided by 40.
3. The Code or Data array is programmed one byte at a time by supplying the address and data together with the appropriate Write instruction. The selected memory location is first automatically erased before new data is written. The write cycle is self-timed and typically takes less than 2.5 ms at 5V.
4. Any memory location can be verified by using the Read instruction which returns the content at the selected address at serial output MISO/P1.6.
5. At the end of a programming session, RST can be set low to commence normal operation.

Power-off sequence (if needed):

Set XTAL1 to "L" (if a crystal is not used).

Set RST to "L".

Turn V_{CC} power off.

Serial Programming Instruction

The Instruction Set for Serial Programming follows a 3-byte protocol and is shown in the following table:

truction Set

ruction	Input Format			Operation
	Byte 1	Byte 2	Byte 3	
gramming Enable	1010 1100	0101 0011	xxxx xxxx	Enable serial programming interface after RST goes high.
Erase	1010 1100	xxxx x100	xxxx xxxx	Chip erase both 8K & 2K memory arrays.
d Code Memory	aaaa a001	low addr	xxxx xxxx	Read data from Code memory array at the selected address. The 5 MSBs of the first byte are the high order address bits. The low order address bits are in the second byte. Data are available at pin MISO during the third byte.
e Code Memory	aaaa a010	low addr	data in	Write data to Code memory location at selected address. The address bits are the 5 MSBs of the first byte together with the second byte.
d Data Memory	00aa a101	low addr	xxxx xxxx	Read data from Data memory array at selected address. Data are available at pin MISO during the third byte.
e Data Memory	00aa a110	low addr	data in	Write data to Data memory location at selected address.
e Lock Bits	1010 1100	x x111	xxxx xxxx	Write lock bits. Set LB1, LB2 or LB3 = "0" to program lock bits

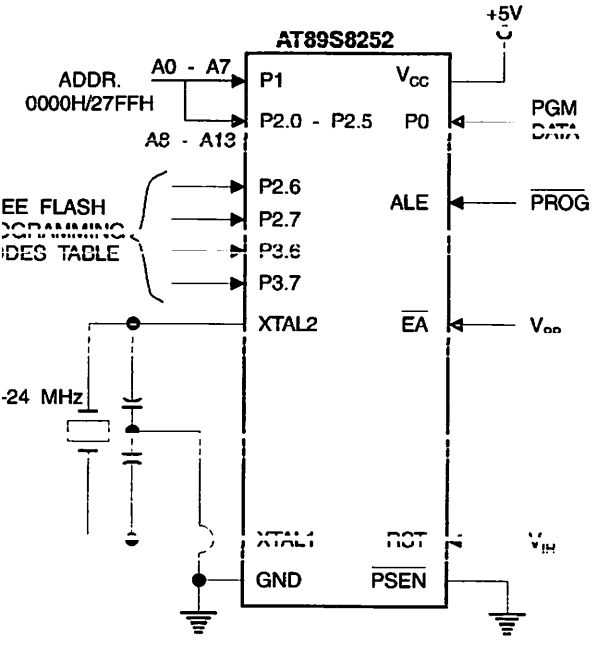
1. DATA polling is used to indicate the end of a write cycle which typically takes less than 2.5 ms at 5V.
2. "aaaaa" = high order address.
3. "x" = don't care.

sh and EEPROM Parallel Programming Modes

e	RST	PSEN	ALE/PROG	EA/V	P2.6	P2.7	P3.6	P3.7	Data I/O P0.7-0	Address P2.5-0 P1.7-0
al Prog. Modes	H	h(1)	h(1)	x						
Erase	H	L	(2)	12V	H	L	L	L	X	X
(10K bytes) Memory	H	L		12V	L	H	H	H	DIN	ADDR
(10K bytes) Memory	H	L	H	12V	L	H	H	H	DOUT	ADDR
Lock Bits:	H	L		12V	H	L	H	L	DIN	X
Bit - 1									P0.7 = 0	X
Bit - 2									P0.6 = 0	X
Bit - 3									P0.5 = 0	X
Lock Bits:	H	L	H	12V	H	H	L	L	DOUT	X
Bit - 1									@P0.2	X
Bit - 2									@P0.1	X
Bit - 3									@P0.0	X
Atmel Code	H	L	H	12V	L	L	L	L	DOUT	30H
Device Code	H	L	H	12V	L	L	L	L	DOUT	31H
Prog. Enable	H	L	(2)	12V	L	H	L	H	P0.0 = 0	X
Prog. Disable	H	L	(2)	12V	L	H	L	H	P0.0 = 1	X
Serial Prog. Fuse	H	L	H	12V	H	H	L	H	@P0.0	X

1. "h" = weakly pulled "High" internally.
2. Chip Erase and Serial Programming Fuse require a 10 ms PROG pulse. Chip Erase needs to be performed first before reprogramming any byte with a content other than FFH.
3. P0.4 is pulled Low during programming to indicate RDY/BSY.
4. "X" = don't care

re 13. Programming the Flash/EEPROM Memory



re 14. Verifying the Flash/EEPROM Memory

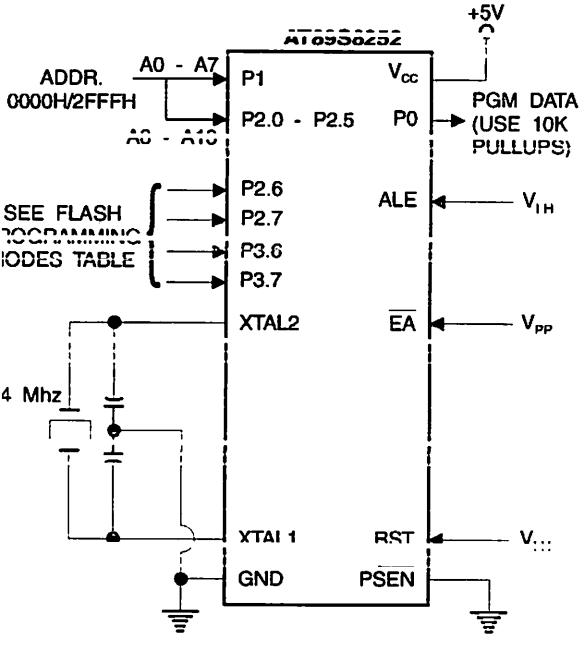
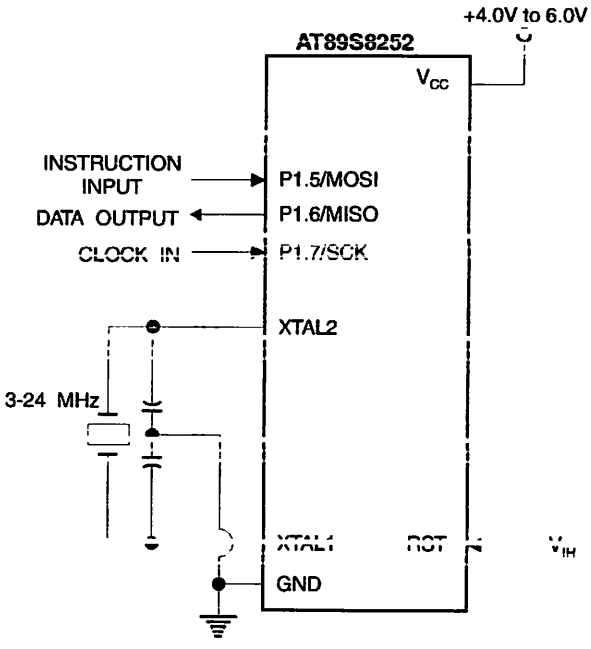


Figure 15. Flash/EEPROM Serial Downloading

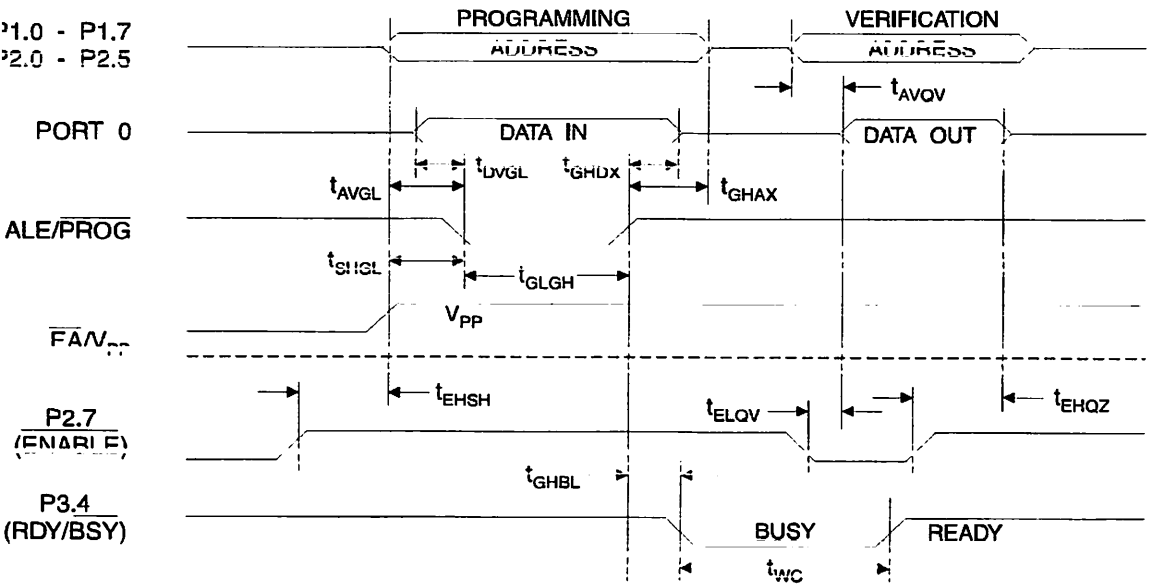


sh Programming and Verification Characteristics – Parallel Mode

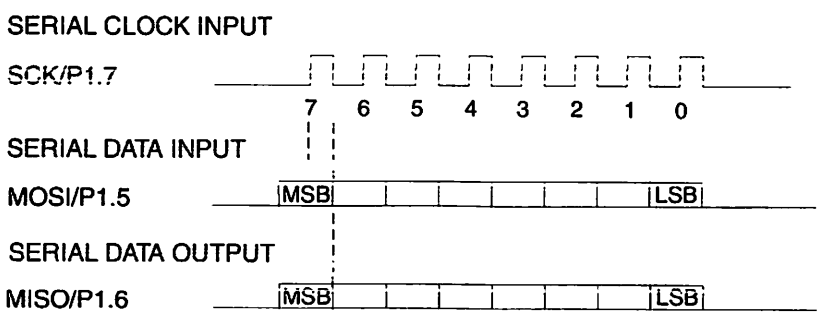
0°C to 70°C, V_{CC} = 5.0V ± 10%

ıbol	Parameter	Min	Max	Units
	Programming Enable Voltage	11.5	12.5	V
	Programming Enable Current		1.0	mA
.CL	Oscillator Frequency	3	24	MHz
-	Address Setup to $\overline{PROG}$ Low	$48t_{CLCL}$		
x	Address Hold after $\overline{PROG}$	$48t_{CLCL}$		
-	Data Setup to $\overline{PROG}$ Low	$48t_{CLCL}$		
x	Data Hold after $\overline{PROG}$	$48t_{CLCL}$		
1	P2.7 ($\overline{ENABLE}$) High to V_{PP}	$48t_{CLCL}$		
	V_{PP} Setup to $\overline{PROG}$ Low	10		µs
1	$\overline{PROG}$ Width	1	110	µs
/	Address to Data Valid		$48t_{CLCL}$	
,	ENABLE Low to Data Valid		$48t_{CLCL}$	
?	Data Float after $\overline{ENABLE}$	0	$48t_{CLCL}$	
-	$\overline{PROG}$ High to $\overline{BUSY}$ Low		1.0	µs
	Byte Write Cycle Time		2.0	ms

sh/EEPROM Programming and Verification Waveforms – Parallel Mode



ial Downloading Waveforms



;olute Maximum Ratings*

rating Temperature	-55°C to +125°C
age Temperature	-65°C to +150°C
ıge on Any Pin Respect to Ground	-1.0V to +7.0V
imum Operating Voltage	6.6V
Output Current	15.0 mA

*NOTICE: Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Characteristics

'alues shown in this table are valid for T_A = -40°C to 85°C and V_{CC} = 5.0V ± 20%, unless otherwise noted.

bol	Parameter	Condition	Min	Max	Units
	Input Low-voltage	(Except $\overline{EA}$)	-0.5	0.2 V_{CC} - 0.1	V
	Input Low-voltage ($\overline{EA}$)		-0.5	0.2 V_{CC} - 0.3	V
	Input High-voltage	(Except XTAL1, RST)	0.2 V_{CC} + 0.9	V_{CC} + 0.5	V
	Input High-voltage	(XTAL1, RST)	0.7 V_{CC}	V_{CC} + 0.5	V
	Output Low-voltage [1] (Ports 1,2,3)	I_{OL} = 1.6 mA		0.5	V
	Output Low-voltage [1] (Port 0, ALE, $\overline{PSEN}$)	I_{OL} = 3.2 mA		0.5	V
	Output High-voltage (Ports 1,2,3, ALE, $\overline{PSEN}$)	I_{OH} = -60 µA, V_{CC} = 5V ± 10%	2.4		V
		I_{OH} = -25 µA	0.75 V_{CC}		V
		I_{OH} = -10 µA	0.9 V_{CC}		V
	Output High-voltage (Port 0 in External Bus Mode)	I_{OH} = -800 µA, V_{CC} = 5V ± 10%	2.4		V
		I_{OH} = -300 µA	0.75 V_{CC}		V
		I_{OH} = -80 µA	0.9 V_{CC}		V
	Logical 0 Input Current (Ports 1,2,3)	V_{IN} = 0.45V		-50	µA
	Logical 1 to 0 Transition Current (Ports 1,2,3)	V_{IN} = 2V, V_{CC} = 5V ± 10%		-650	µA
	Input Leakage Current (Port 0, $\overline{EA}$)	0.45 < V_{IN} < V_{CC}		±10	µA
T	Reset Pull-down Resistor		50	300	KΩ
	Pin Capacitance	Test Freq. = 1 MHz, T_A = 25°C		10	pF
	Power Supply Current	Active Mode, 12 MHz		25	mA
		Idle Mode, 12 MHz		6.5	mA
	Power-down Mode [2]	V_{CC} = 6V		100	µA
		V_{CC} = 3V		40	µA

1. Under steady state (non-transient) conditions, I_{OL} must be externally limited as follows:
   Maximum I_{OL} per port pin: 10 mA
   Maximum I_{OL} per 8-bit port:
   Port 0: 26 mA
   Ports 1, 2, 3: 15 mA
   Maximum total I_{OL} for all output pins: 71 mA
   If I_{OL} exceeds the test condition, V_{OL} may exceed the related specification. Pins are not guaranteed to sink current greater than the listed test conditions.
2. Minimum V_{CC} for Power-down is 2V

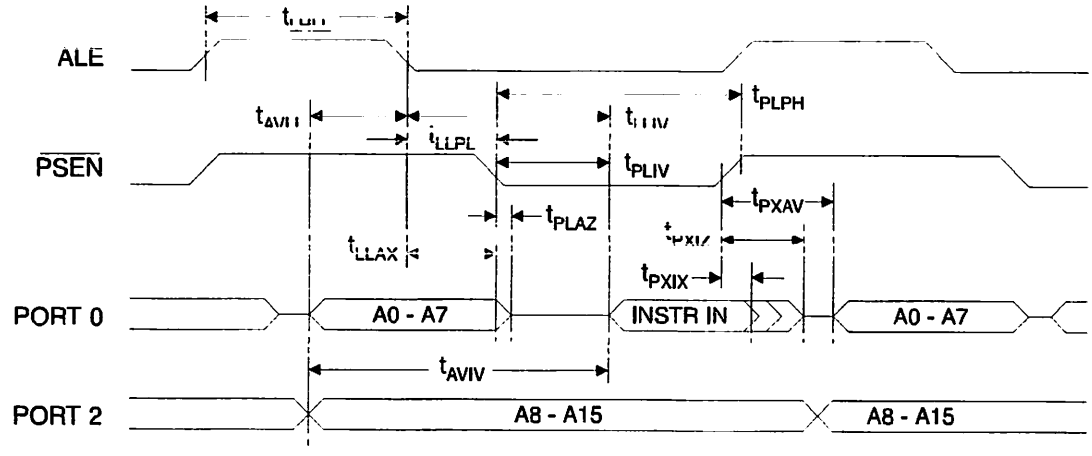
Characteristics

ɜr operating conditions, load capacitance for Port 0, ALE/$\overline{PROG}$, and $\overline{PSEN}$ = 100 pF; load capacitance for all other ...tc = 80 pF.

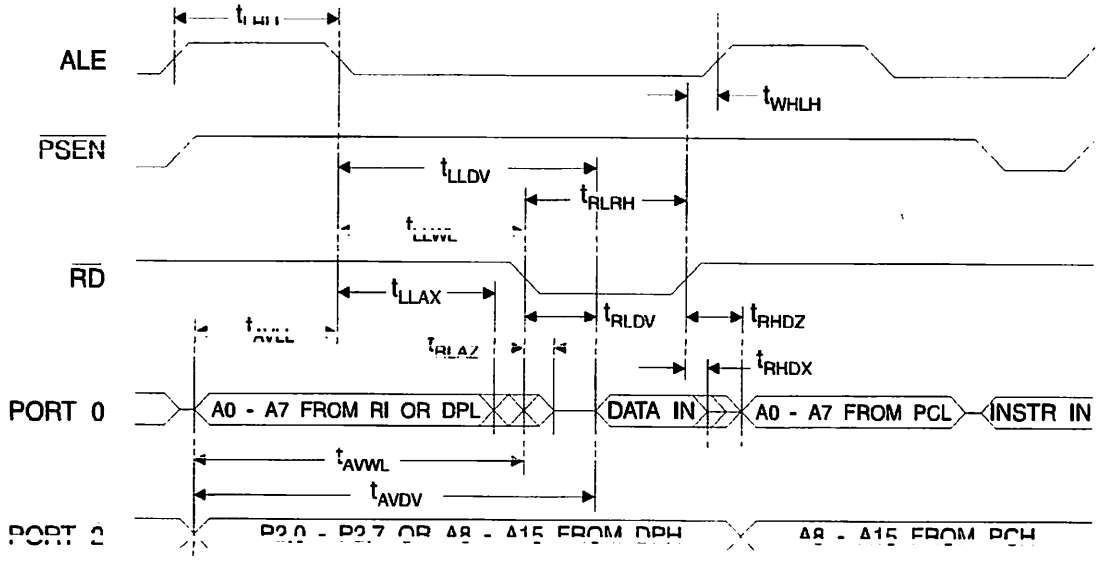
ernal Program and Data Memory Characteristics

ıbol	Parameter	Variable Oscillator		Units
		Min	Max	
CI	Oscillator Frequency	0	24	MHz
	ALE Pulse Width	$2t_{CLCL}$ - 40		ns
	Address Valid to ALE Low	t_{CLCL} - 13		ns
	Address Hold after ALE Low	t_{CLCL} - 20		ns
	ALE Low to Valid Instruction In		$4t_{CLCL}$ - 65	ns
	ALE Low to $\overline{PSEN}$ Low	t_{CLCL} - 13		ns
H	$\overline{PSEN}$ Pulse Width	$3t_{CLCL}$ - 20		ns
	$\overline{PSEN}$ Low to Valid Instruction In		$3t_{CLCL}$ - 45	ns
	Input Instruction Hold after $\overline{PSEN}$	0		ns
	Input Instruction Float after $\overline{PSEN}$		t_{CLCL} - 10	ns
	$\overline{PSEN}$ to Address Valid	t_{CLCL} - 8		ns
	Address to Valid Instruction In		$5t_{CLCL}$ - 55	ns
	$\overline{PSEN}$ Low to Address Float		10	ns
H	$\overline{RD}$ Pulse Width	$6t_{CLCL}$ - 100		ns
H	$\overline{WR}$ Pulse Width	$6t_{CLCL}$ - 100		ns
	RD Low to Valid Data In		$5t_{CLCL}$ - 90	ns
X	Data Hold after $\overline{RD}$	0		ns
	Data Float after $\overline{RD}$		$2t_{CLCL}$ - 28	ns
	ALE Low to Valid Data In		$8t_{CLCL}$ - 150	ns
	Address to Valid Data In		$9t_{CLCL}$ - 165	ns
	ALE Low to $\overline{RD}$ or $\overline{WR}$ Low	$3t_{CLCL}$ - 50	$3t_{CLCL}$ + 50	ns
	Address to $\overline{RD}$ or $\overline{WR}$ Low	$4t_{CLCL}$ - 75		ns
X	Data Valid to $\overline{WR}$ Transition	t_{CLCL} - 20		ns
H	Data Valid to $\overline{WR}$ High	$7t_{CLCL}$ - 120		ns
X	Data Hold after $\overline{WR}$	t_{CLCL} - 20		ns
	$\overline{RD}$ Low to Address Float		0	ns
H	$\overline{RD}$ or $\overline{WR}$ High to ALE High	t_{CLCL} - 20	t_{CLCL} + 25	ns

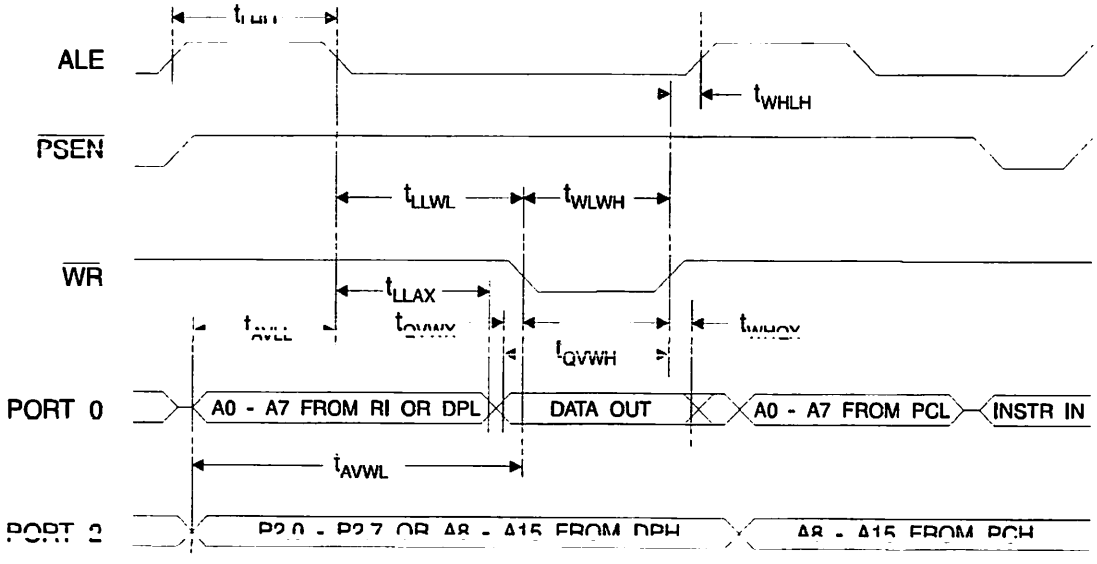
ernal Program Memory Read Cycle



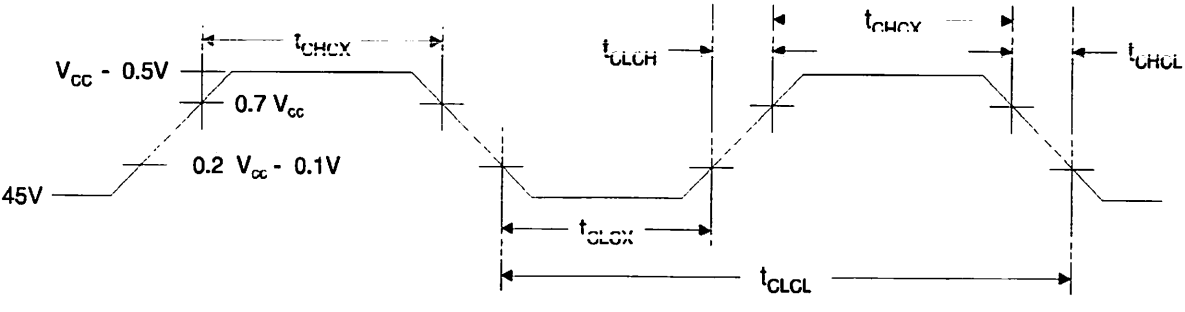
ernal Data Memory Read Cycle



ernal Data Memory Write Cycle



ernal Clock Drive Waveforms



ernal Clock Drive

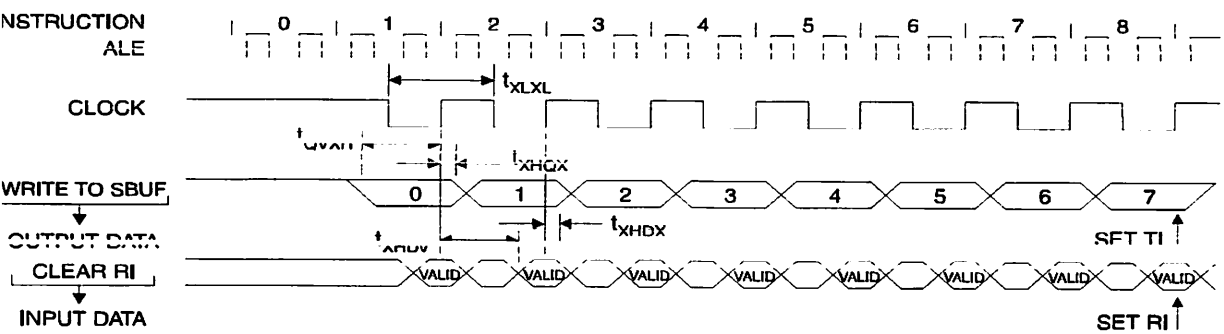
bol	Parameter	V_{CC} = 4.0V to 6.0V		Units
		Min	Max	
CL	Oscillator Frequency	0	24	MHz
	Clock Period	41.6		ns
	High Time	15		ns
	Low Time	15		ns
	Rise Time		20	ns
	Fall Time		20	ns

ial Port Timing: Shift Register Mode Test Conditions

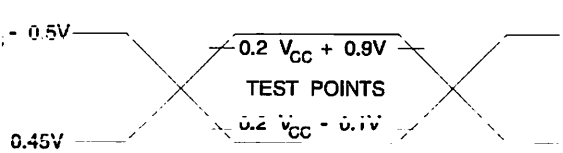
values in this table are valid for V_{CC} = 4.0V to 6V and Load Capacitance = 80 pF.

ibol	Parameter	Variable Oscillator		Units
		Min	Max	
-	Serial Port Clock Cycle Time	$12t_{CLCL}$		ns
H	Output Data Setup to Clock Rising Edge	$10t_{CLCL}$ - 133		ns
X	Output Data Hold after Clock Rising Edge	$2t_{CLCL}$ - 117		ns
K	Input Data Hold after Clock Rising Edge	0		ns
V	Clock Rising Edge to Input Data Valid		$10t_{CLCL}$ - 133	ns

ft Register Mode Timing Waveforms

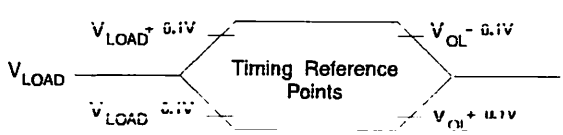


Testing Input/Output Waveforms[1]



1. AC Inputs during testing are driven at V_{CC} - 0.5V for a logic 1 and 0.45V for a logic 0. Timing measurements are made at V_{IH} min. for a logic 1 and V_{IL} max. for a logic 0.

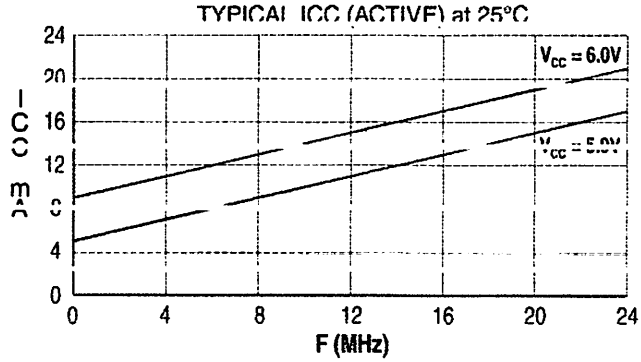
Float Waveforms[1]



Notes: 1. For timing purposes, a port pin is no longer floating when a 100 mV change from load voltage occurs. A port pin begins to float when a 100 mV change from the loaded V_{OH}/V_{OL} level occurs.

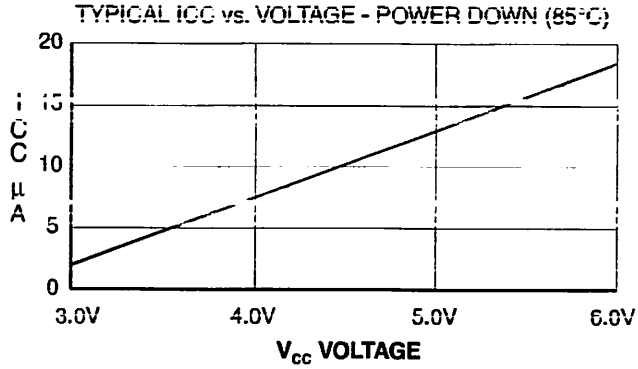
AT89S8252

TYPICAL ICC (ACTIVE) at 25°C



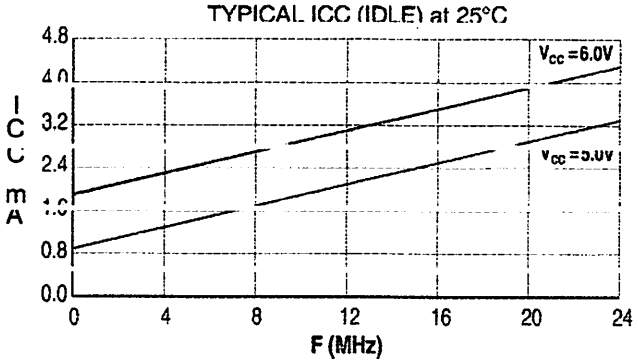
AT89S8252

TYPICAL ICC vs. VOLTAGE - POWER DOWN (85°C)



AT89S8252

TYPICAL ICC (IDLE) at 25°C



Notes: 1. XTAL1 tied to GND for Icc (power-down)
2. Lock bits programmed

ering Information

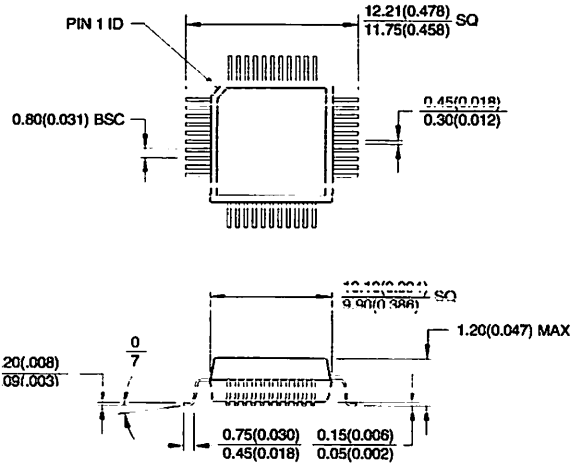
peed (MHz)	Power Supply	Ordering Code	Package	Operation Range
24	4.0V to 6.0V	AT89S8252-24AC	44A	Commercial (0°C to 70°C)
		AT89S8252-24JC	44J	
		AT89S8252-24PC	40P6	
		AT89S8252-24QC	44Q	
	4.0V to 6.0V	AT89S8252-24AI	44A	Industrial (-40°C to 85°C)
		AT89S8252-24JI	44J	
		AT89S8252-24PI	40P6	
		AT89S8252-24QI	44Q	
33	4.5V to 5.5V	AT89S8252-33AC	44A	Commercial (0°C to 70°C)
		AT89S8252-33JC	44J	
		AT89S8252-33PC	40P6	
		AT89S8252-33QC	44Q	

= Preliminary Information

	Package Type
	44-lead, Thin Plastic Gull Wing Quad Flatpack (TQFP)
	44-lead, Plastic J-leaded Chip Carrier (PLCC)
	40-lead, 0.600" Wide, Plastic Dual Inline Package (PDIP)
	44-lead, Plastic Gull Wing Quad Flatpack (PQFP)

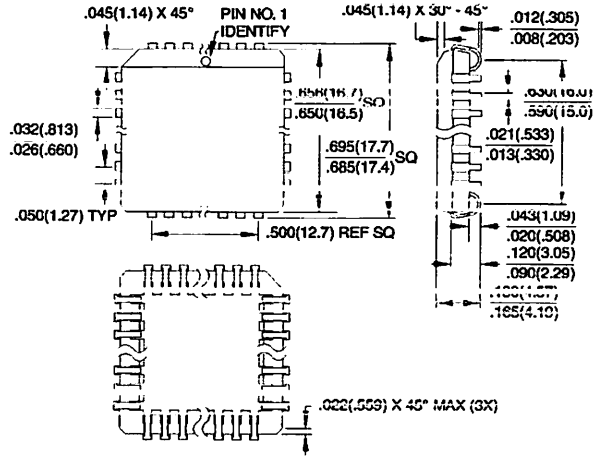
kaging Information

4A, 44-lead, Thin (1.0 mm) Plastic Gull Wing Quad
latpack (TQFP)
)imensions in Millimeters and (Inches)*
EDEC STANDARD MS-026 ACB

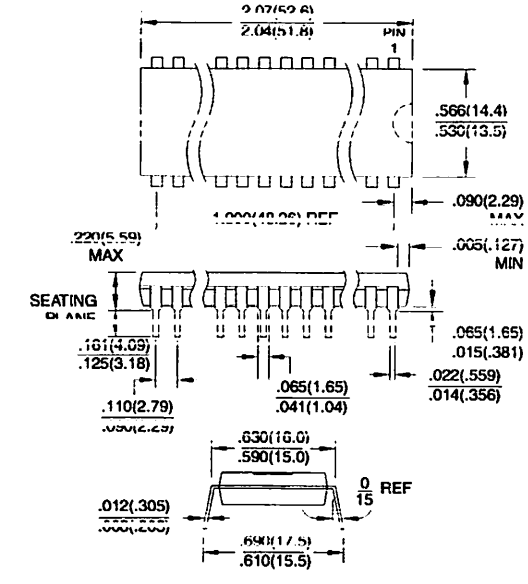


ontrolling dimension: millimeters

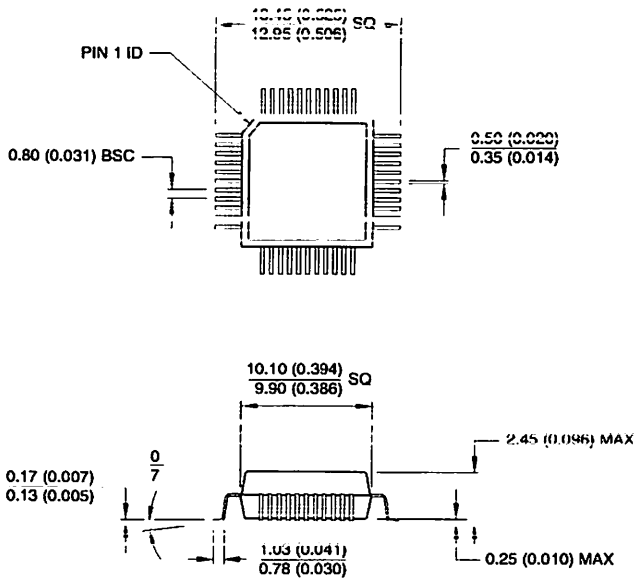
44J, 44-lead, Plastic J-leaded Chip Carrier (PLCC)
Dimensions in Inches and (Millimeters)
JEDEC STANDARD MS-018 AC



DP6, 40-lead, 0.600" Wide, Plastic Dual Inline
ackage (PDIP)
imensions in Inches and (Millimeters)



44Q, 44-lead, Plastic Quad Flat Package (PQFP)
Dimensions in Millimeters and (Inches)*
JEDEC STANDARD MS-022 AB



Controlling dimension: millimeters

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0401E–02/00/xM

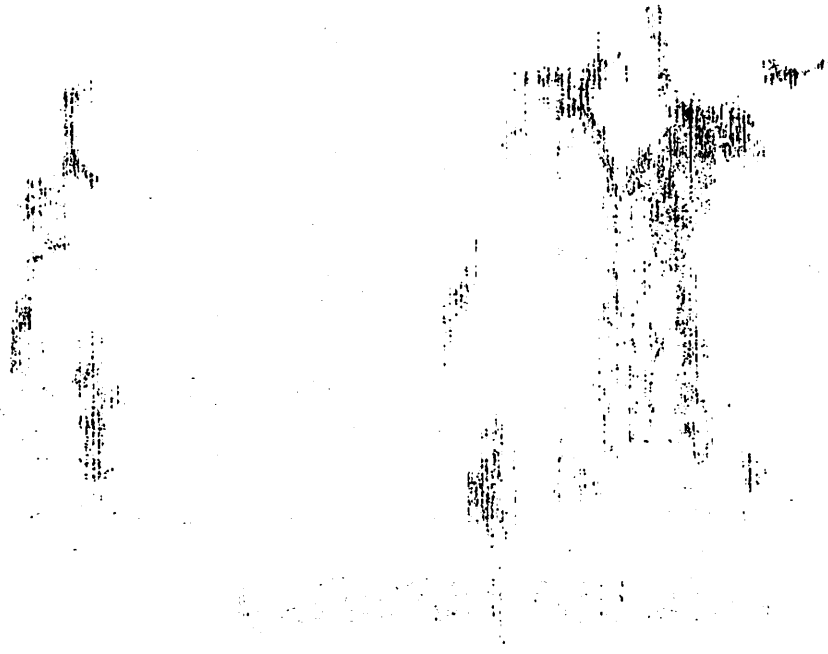
ISD2560/75/90/120

SINGLE-CHIP, MULTIPLE-MESSAGES,

VOICE RECORD/PLAYBACK DEVICE

60-, 75-, 90-, AND 120-SECOND DURATION

Publication Release Date: May 2003
Revision 1.0



Winbond Electronics Corp.

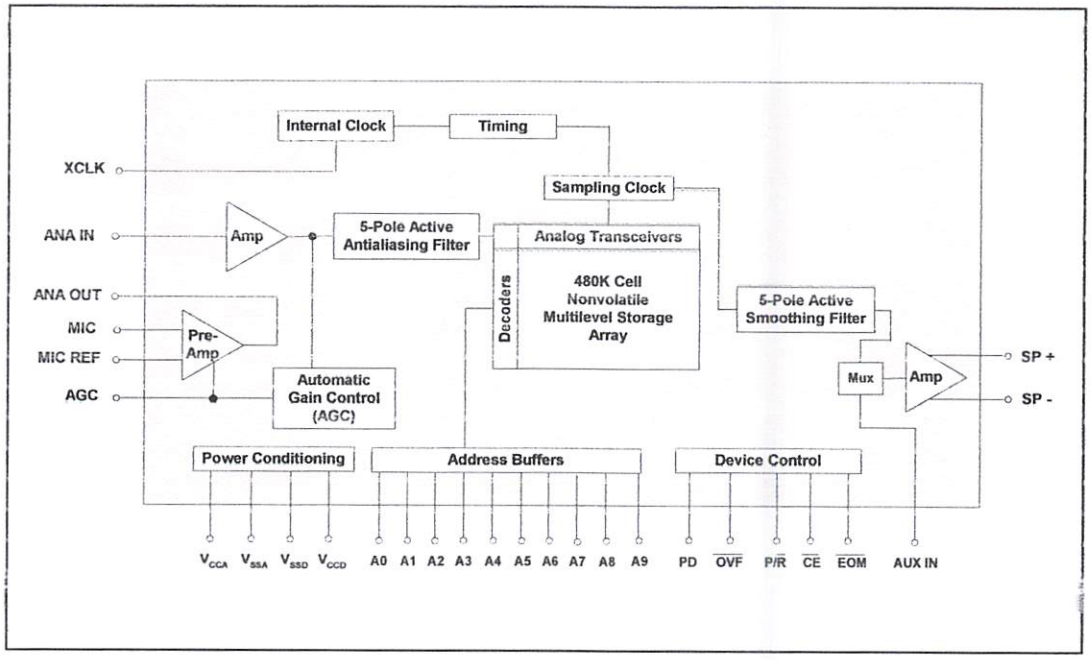
1. GENERAL DESCRIPTION

Winbond's ISD2500 ChipCorder® Series provide high-quality, single-chip, Record/Playback solutions for 60- to 120-second messaging applications. The CMOS devices include an on-chip oscillator, microphone preamplifier, automatic gain control, antialiasing filter, smoothing filter, speaker amplifier, and high density multi-level storage array. In addition, the ISD2500 is microcontroller compatible, allowing complex messaging and addressing to be achieved. Recordings are stored into on-chip nonvolatile memory cells, providing zero-power message storage. This unique, single-chip solution is made possible through Winbond's patented multilevel storage technology. Voice and audio signals are stored directly into memory in their natural form, providing high-quality, solid-state voice reproduction.

2. FEATURES

- Easy-to-use single-chip, voice record/playback solution
- High quality, natural voice/audio reproduction
- Single-chip with duration of 60, 75, 90, or 120 seconds
- Manual switch or microcontroller compatible
- Playback can be edge- or level-activated
- Directly cascadable for longer durations
- Automatic power-down (push-button mode)
  - Standby current 1 µA (typical)
- Zero-power message storage
  - Eliminates battery backup circuits
- Fully addressable to handle multiple messages
- 100-year message retention (typical)
- 100,000 record cycles (typical)
- On-chip clock source
- Programmer support for play-only applications
- Single +5 volt power supply
- Available in die form, PDIP, SOIC and TSOP packaging
- Temperature = die (0°C to +50°C) and package (0°C to +70°C)

3. BLOCK DIAGRAM



Winbond Electronics Corp.

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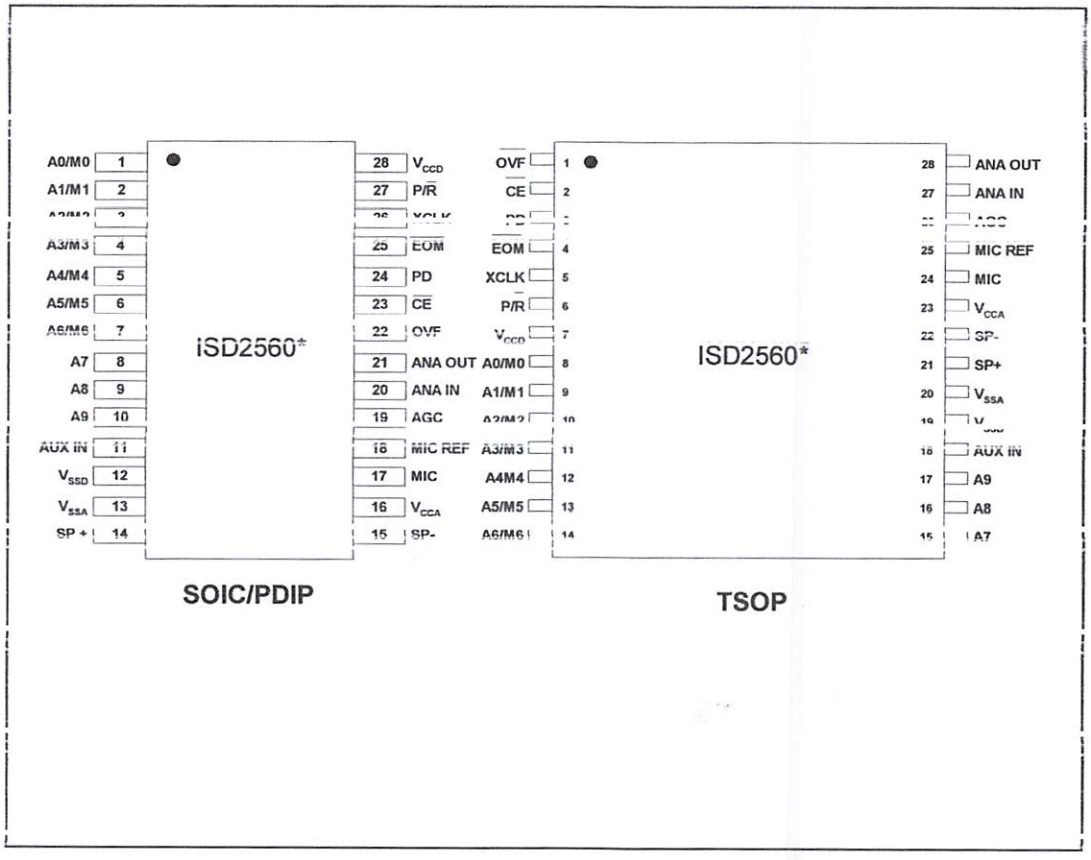
5. PIN CONFIGURATION



* Same pinouts for ISD2575 / 2590 / 25120 products

6. PIN DESCRIPTION

PIN NAME	PIN NO.		FUNCTION
	SOIC/ PDIP	TSOP	
Ax/Mx	1-10/ 1-7	8-17/ 8-14	**Address/Mode Inputs**: The Address/Mode Inputs have two functions depending on the level of the two Most Significant Bits (MSB) of the address pins (A8 and A9). If either or both of the two MSBs are LOW, the inputs are always interpreted as address bits and are used as the start address for the current record or playback cycle. The address pins are inputs only and do not output any internal address information during the operation. Address inputs are latched by the falling edge of $\overline{CE}$. If both MSBs are HIGH. the Address/Mode inputs are interpreted as Mode bits according to the Operational Mode table on page 12. There are six operational modes (M0...M6) available as indicated in the table. It is possible to use multiple operational modes simultaneously. Operational Modes are sampled on each falling edge of $\overline{CE}$, and thus Operational Modes and direct addressing are mutually exclusive.
AUX IN	11	18	**Auxiliary Input.** The Auxiliary Input is multiplexed through to the output amplifier and speaker output pins when $\overline{CE}$ is HIGH, P/$\overline{R}$ is HIGH, and playback is currently not active or if the device is in playback overflow. When cascading multiple ISD2500 devices, the AUX IN pin is used to connect a playback signal from a following device to the previous output speaker drivers. For noise considerations, it is suggested that the auxiliary input not be driven when the storage array is active.
V_{SSA}, V_{SSD}	13, 12	20, 19	**Ground**: The ISD2500 series of devices utilizes separate analog and digital ground busses. These pins should be connected separately through a low-impedance path to power supply ground.
SP+/SP-	14/15	21/22	**Speaker Outputs**: All devices in the ISD2500 series include an on-chip differential speaker driver, capable of driving 50 mW into 16 Ω from AUX IN (12.2mW from memory). [1] The speaker outputs are held at V_{SSA} levels during record and power down. It is therefore not possible to parallel speaker outputs of multiple ISD2500 devices or the outputs of other speaker drivers. [2] A single-end output may be used (including a coupling capacitor between the SP pin and the speaker). These outputs may be used individually with the output signal taken from either pin. However, the use of single-end output results in a 1 to 4 reduction in its output power.

[1] Connection of speaker outputs in parallel may cause damage to the device.
[2] Never ground or drive an unused speaker output.

PIN NAME	PIN NO.		FUNCTION
	SOIC/ PDIP	TSOP	
V_{CCA}, V_{CCD}	16, 28	23, 7	**Supply Voltage**: To minimize noise, the analog and digital circuits in the ISD2500 series devices use separate power busses. These voltage busses are brought out to separate pins and should be tied together as close to the supply as possible. In addition, these supplies should be decoupled as close to the package as possible.
MIC	17	24	**Microphone**: The microphone pin transfers input signal to the on-chip preamplifier. A built-in Automatic Gain Control (AGC) circuit controls the gain of this preamplifier from –15 to 24dB. An external microphone should be AC coupled to this pin via a series capacitor. The capacitor value, together with the internal 10 KΩ resistance on this pin, determines the low-frequency cutoff for the ISD2500 series passband. See Winbond's Application Information for additional information on low-frequency cutoff calculation.
MIC REF	18	25	**Microphone Reference**: The MIC REF input is the inverting input to the microphone preamplifier. This provides a noise-canceling or common-mode rejection input to the device when connected to a differential microphone.
AGC	19	26	**Automatic Gain Control**: The AGC dynamically adjusts the gain of the preamplifier to compensate for the wide range of microphone input levels. The AGC allows the full range of whispers to loud sounds to be recorded with minimal distortion. The "attack" time is determined by the time constant of a 5 KΩ internal resistance and an external capacitor (C2 on the schematic of Figure 5 in section 11) connected from the AGC pin to V_{SSA} analog ground. The "release" time is determined by the time constant of an external resistor (R2) and an external capacitor (C2) connected in parallel between the AGC pin and V_{SSA} analog ground. Nominal values of 470 KΩ and 4.7 µF give satisfactory results in most cases.
ANA IN	20	27	**Analog Input**: The analog input transfers analog signal to the chip for recording. For microphone inputs, the ANA OUT pin should be connected via an external capacitor to the ANA IN pin. This capacitor value, together with the 3.0 KΩ input impedance of ANA IN, is selected to give additional cutoff at the low-frequency end of the voice passband. If the desired input is derived from a source other than a microphone, the signal can be fed, capacitively coupled, into the ANA IN pin directly.
ANA OUT	21	28	**Analog Output**: This pin provides the preamplifier output to the user. The voltage gain of the preamplifier is determined by the voltage level at the AGC pin.

PIN NAME	PIN NO.		FUNCTION
	SOIC/ PDIP	TSOP	
$\overline{OVF}$	22	1	**Overflow**: This signal pulses LOW at the end of memory array, indicating the device has been filled and the message has overflowed. The $\overline{OVF}$ output then follows the $\overline{CE}$ input until a PD pulse has reset the device. This pin can be used to cascade several ISD2500 devices together to increase record/playback durations.
$\overline{CE}$	23	2	**Chip Enable**: The $\overline{CE}$ input pin is taken LOW to enable all playback and record operations. The address pins and playback/record pin ($P/\overline{R}$) are latched by the falling edge of $\overline{CE}$. $\overline{CE}$ has additional functionality in the M6 (Push-Button) Operational Mode as described in the Operational Mode section.
PD	24	3	**Power Down**: When neither record nor playback operation, the PD pin should be pulled HIGH to place the part in standby mode (see I_{SB} specification). When overflow ($\overline{OVF}$) pulses LOW for an overflow condition, PD should be brought HIGH to reset the address pointer back to the beginning of the memory array. The PD pin has additional functionality in the M6 (Push-Button) Operation Mode as described in the Operational Mode section.
$\overline{EOM}$	25	4	**End-Of-Message**: A nonvolatile marker is automatically inserted at the end of each recorded message. It remains there until the message is recorded over. The $\overline{EOM}$ output pulses LOW for a period of T_{EOM} at the end of each message. In addition, the ISD2500 series has an internal V_{CC} detect circuit to maintain message integrity should V_{CC} fall below 3.5V. In this case, $\overline{EOM}$ goes LOW and the device is fixed in Playback-only mode. When the device is configured in Operational Mode M6 (Push-Button Mode), this pin provides an active-HIGH signal, indicating the device is currently recording or playing. This signal can conveniently drive an LED for visual indicator of a record or playback operation in process.

<table>
<tr><th rowspan="2">PIN NAME</th><th colspan="2">PIN NO.</th><th rowspan="2">FUNCTION</th></tr>
<tr><th>SOIC/ PDIP</th><th>TSOP</th></tr>
<tr><td>XCLK</td><td>26</td><td>5</td><td>External Clock: The external clock input has an internal pull-down device. The device is configured at the factory with an internal sampling clock frequency centered to ±1 percent of specification. The frequency is then maintained to a variation of ±2.25 percent over the entire commercial temperature and operating voltage ranges. If greater precision is required, the device can be clocked through the XCLK pin as follows:
<table>
<tr><th>Part Number</th><th>Sample Rate</th><th>Required Clock</th></tr>
<tr><td>ISD2560</td><td>8.0 kHz</td><td>1024 kHz</td></tr>
<tr><td>ISD2575</td><td>6.4 kHz</td><td>819.2 kHz</td></tr>
<tr><td>ISD2590</td><td>5.3 kHz</td><td>682.7 kHz</td></tr>
<tr><td>ISD25120</td><td>4.0 kHz</td><td>512 kHz</td></tr>
</table>
These recommended clock rates should not be varied because the antialiasing and smoothing filters are fixed, and aliasing problems can occur if the sample rate differs from the one recommended. The duty cycle on the input clock is not critical, as the clock is immediately divided by two. If the XCLK is not used, this input must be connected to ground.</td></tr>
<tr><td>P/R</td><td>27</td><td>6</td><td>Playback/Record: The P/R input pin is latched by the falling edge of the $\overline{CE}$ pin. A HIGH level selects a playback cycle while a LOW level selects a record cycle. For a record cycle, the address pins provide the starting address and recording continues until PD or $\overline{CE}$ is pulled HIGH or an overflow is detected (i.e. the chip is full). When a record cycle is terminated by pulling PD or $\overline{CE}$ HIGH, then End-Of-Message (EOM) marker is stored at the current address in memory. For a playback cycle, the address inputs provide the starting address and the device will play until an $\overline{EOM}$ marker is encountered. The device can continue to pass an $\overline{EOM}$ marker if $\overline{CE}$ is held LOW in address mode, or in an Operational Mode. (See Operational Modes section)</td></tr>
</table>

7. FUNCTIONAL DESCRIPTION

7.1. Detailed Description

Speech/Sound Quality

The Winbond's ISD2500 series includes devices offered at 4.0, 5.3, 6.4, and 8.0 kHz sampling frequencies, allowing the user a choice of speech quality options. Increasing the duration within a product series decreases the sampling frequency and bandwidth, which affects the sound quality. Please refer to the ISD2560/75/90/120 Product Summary table below to compare the duration, sampling frequency and filter pass band.

The speech samples are stored directly into the on-chip nonvolatile memory without any digitization and compression associated like other solutions. Direct analog storage provides a very true, natural sounding reproduction of voice, music, tones, and sound effects not available with most solid state digital solutions.

Duration

To meet various system requirements, the ISD2560/75/90/120 products offer single-chip solutions at 60, 75, 90, and 120 seconds. Parts may also be cascaded together for longer durations.

TABLE 1: ISD2560/75/90/120 PRODUCT SUMMARY

Part Number	Duration (Seconds)	Input Sample Rate (kHz)	Typical Filter Pass Band * (kHz)
ISD2560	60	8.0	3.4
ISD2575	75	6.4	2.7
ISD2590	90	5.3	2.3
ISD25120	120	4.0	1.7

* -3dB roll-off point

EEPROM Storage

One of the benefits of Winbond's ChipCorder® technology is the use of on-chip nonvolatile memory, providing zero-power message storage. The message is retained for up to 100 years typically without power. In addition, the device can be re-recorded typically over 100,000 times.

Microcontroller Interface

In addition to its simplicity and ease of use, the ISD2500 series includes all the interfaces necessary for microcontroller-driven applications. The address and control lines can be interfaced to a microcontroller and manipulated to perform a variety of tasks, including message assembly, message concatenation, predefined fixed message segmentation, and message management.

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Programming

The ISD2500 series is also ideal for playback-only applications, where single or multiple messages are referenced through buttons, switches, or a microcontroller. Once the desired message configuration is created, duplicates can easily be generated via a gang programmer.

7.2. OPERATIONAL MODES

The ISD2500 series is designed with several built-in Operational Modes that provide maximum functionality with minimum external components. These modes are described in details as below. The Operational Modes are accessed via the address pins and mapped beyond the normal message address range. When the two Most Significant Bits (MSB), A8 and A9, are HIGH, the remaining address signals are interpreted as mode bits and not as address bits. Therefore, Operational Modes and direct addressing are not compatible and cannot be used simultaneously.

There are two important considerations for using Operational Modes. First, all operations begin initially at address 0 of its memory. Later operations can begin at other address locations, depending on the Operational Mode(s) chosen. In addition, the address pointer is reset to 0 when the device is changed from record to playback, playback to record (except M6 mode), or when a Power-Down cycle is executed.

Second, Operational Modes are executed when $\overline{CE}$ goes LOW. This Operational Mode remains in effect until the next LOW-going $\overline{CE}$ signal, at which point the current mode(s) are sampled and executed.

TABLE 2: OPERATIONAL MODES

Mode [1]	Function	Typical Use	Jointly Compatible [2]
M0	Message cueing	Fast-forward through messages	M4, M5, M6
M1	Delete $\overline{EOM}$ markers	Position $\overline{EOM}$ marker at the end of the last message	M3, M4, M5, M6
M2	Not applicable	Reserved	N/A
M3	Looping	Continuous playback from Address 0	M1, M5, M6
M4	Consecutive addressing	Record/playback multiple consecutive messages	M0, M1, M5
M5	$\overline{CE}$ level-activated	Allows message pausing	M0, M1, M3, M4
M6	Push-button control	Simplified device interface	M0, M1, M3

[1] Besides mode pin needed to be "1", A8 and A9 pin are also required to be "1" in order to enter into the related operational mode.

[2] Indicates additional Operational Modes which can be used simultaneously with the given mode.

7.2.1. Operational Modes Description

The Operational Modes can be used in conjunction with a microcontroller, or they can be hardwired to provide the desired system operation.

M0 – Message Cueing

Message Cueing allows the user to skip through messages, without knowing the actual physical addresses of each message. Each $\overline{CE}$ LOW pulse causes the internal address pointer to skip to the next message. This mode is used for playback only, and is typically used with the M4 Operational Mode.

M1 – Delete $\overline{EOM}$ Markers

The M1 Operational Mode allows sequentially recorded messages to be combined into a single message with only one $\overline{EOM}$ marker set at the end of the final message. When this Operational Mode is configured, messages recorded sequentially are played back as one continuous message.

M2 – Unused

When Operational Modes are selected, the M2 pin should be LOW.

M3 – Message Looping

The M3 Operational Mode allows for the automatic, continuously repeated playback of the message located at the beginning of the address space. A message can completely fill the ISD2500 device and will loop from beginning to end without $\overline{OVF}$ going LOW.

M4 – Consecutive Addressing

During normal operation, the address pointer will reset when a message is played through an $\overline{EOM}$ marker. The M4 Operational Mode inhibits the address pointer reset on $\overline{EOM}$, allowing messages to be played back consecutively.

M5 - $\overline{CE}$-Level Activated

The default mode for ISD2500 devices is for $\overline{CE}$ to be edge-activated on playback and level-activated on record. The M5 Operational Mode causes the $\overline{CE}$ pin to be interpreted as level-activated as opposed to edge-activated during playback. This is especially useful for terminating playback operations using the $\overline{CE}$ signal. In this mode, $\overline{CE}$ LOW begins a playback cycle, at the beginning of the device memory. The playback cycle continues as long as $\overline{CE}$ is held LOW. When $\overline{CE}$ goes HIGH, playback will immediately end. A new $\overline{CE}$ LOW will restart the message from the beginning unless M4 is also HIGH.

M6 – Push-Button Mode

The ISD2500 series contain a Push-Button Operational Mode. The Push-Button Mode is used primarily in very low-cost applications and is designed to minimize external circuitry and components, thereby reducing system cost. In order to configure the device in Push-Button Operational Mode, the two most significant address bits must be HIGH, and the M6 mode pin must also be HIGH. A device in this mode always powers down at the end of each playback or record cycle after $\overline{CE}$ goes HIGH.

When this operational mode is implemented, three of the pins on the device have alternate functionality as described in the table below.

TABLE 3: ALTERNATE FUNCTIONALITY IN PINS

Pin Name	Alternate Functionality in Push-Button Mode
$\overline{CE}$	Start/Pause Push-Button (LOW pulse-activated)
PD	Stop/Reset Push-Button (HIGH pulse-activated)
$\overline{EOM}$	Active-HIGH Run Indicator

$\overline{CE}$ (START/PAUSE)

In Push-Button Operational Mode, $\overline{CE}$ acts as a LOW-going pulse-activated START/PAUSE signal. If no operation is currently in progress, a LOW-going pulse on this signal will initiate a playback or record cycle according to the level on the P/$\overline{R}$ pin. A subsequent pulse on the $\overline{CE}$ pin, before an $\overline{EOM}$ is reached in playback or an overflow condition occurs, will pause the current operation, and the address counter is not reset. Another $\overline{CE}$ pulse will cause the device to continue the operation from the place where it is paused.

PD (STOP/RESET)

In Push-Button Operational Mode, PD acts as a HIGH-going pulse-activated STOP/RESET signal. When a playback or record cycle is in progress and a HIGH-going pulse is observed on PD, the current cycle is terminated and the address pointer is reset to address 0, the beginning of the message space.

$\overline{EOM}$ (RUN)

In Push-Button Operational Mode, $\overline{EOM}$ becomes an active-HIGH RUN signal which can be used to drive an LED or other external device. It is HIGH whenever a record or playback operation is in progress.

Recording in Push Button Mode

1. The PD pin should be LOW, usually using a pull-down resistor.

2. The P/$\overline{R}$ pin is taken LOW.
3. The $\overline{CE}$ pin is pulsed LOW. Recording starts, $\overline{EOM}$ goes HIGH to indicate an operation in progress.
4. When the $\overline{CE}$ pin is pulsed LOW, Recording pauses, $\overline{EOM}$ goes back LOW. The internal address pointers are not cleared, but the $\overline{EOM}$ marker is stored in memory to indicate as the message end. The P/$\overline{R}$ pin may be taken HIGH at this time. Any subsequent $\overline{CE}$ would start a playback at address 0.
5. The $\overline{CE}$ pin is pulsed LOW. Recording starts at the next address after the previous set $\overline{EOM}$ marker. $\overline{EOM}$ goes back HIGH [3]
6. When the recording sequences are finished, the final $\overline{CE}$ pulse LOW will end the last record cycle, leaving a set $\overline{EOM}$ marker at the message end. Recording may also be terminated by a HIGH level on PD, which will leave a set $\overline{EOM}$ marker.

Playback in Push-Button Mode

1. The PD pin should be LOW.
2. The P/$\overline{R}$ pin is taken HIGH.
3. The $\overline{CE}$ pin is pulsed LOW. Playback starts, $\overline{EOM}$ goes HIGH to indicate an operation in progress.
4. If the $\overline{CE}$ pin is pulsed LOW or an $\overline{EOM}$ marker is encountered during an operation, the part will pause. The internal address pointers are not cleared, and $\overline{EOM}$ goes back LOW. The P/$\overline{R}$ pin may be changed at this time. A subsequent record operation would not reset the address pointers and the recording would begin where playback ended.
5. $\overline{CE}$ is again pulsed LOW. Playback starts where it left off, with $\overline{EOM}$ going HIGH to indicate an operation in progress.
6. Playback continues as in steps 4 and 5 until PD is pulsed HIGH or overflow occurs.
7. If in overflow, pulling $\overline{CE}$ LOW will reset the address pointer and start playback from the beginning. After a PD pulse, the part is reset to address 0.

Note: Push-Button Mode can be used in conjunction with modes M0, M1, and M3.

[3] If the M1 Operational Mode pin is also HIGH, the just previously written $\overline{EOM}$ bit is erased, and recording starts at that address.

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Good Audio Design Practices

Winbond products are very high-quality single-chip voice recording and playback systems. To ensure the highest quality voice reproduction, it is important that good audio design practices on layout and power supply decoupling be followed. See Application Information or below links for details.

Good Audio Design Practices
http://www.winbond-usa.com/products/isd_products/chipcorder/applicationinfo/apin11.pdf

Single-Chip Board Layout Diagrams
http://www.winbond-usa.com/products/isd_products/chipcorder/applicationinfo/apin12.pdf

8. TIMING DIAGRAMS

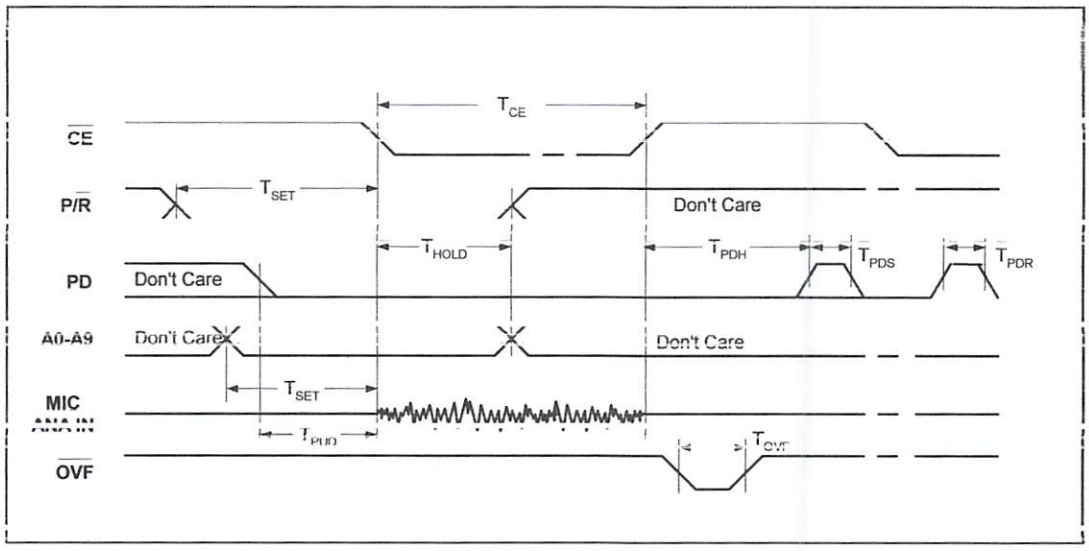

FIGURE 1: RECORD

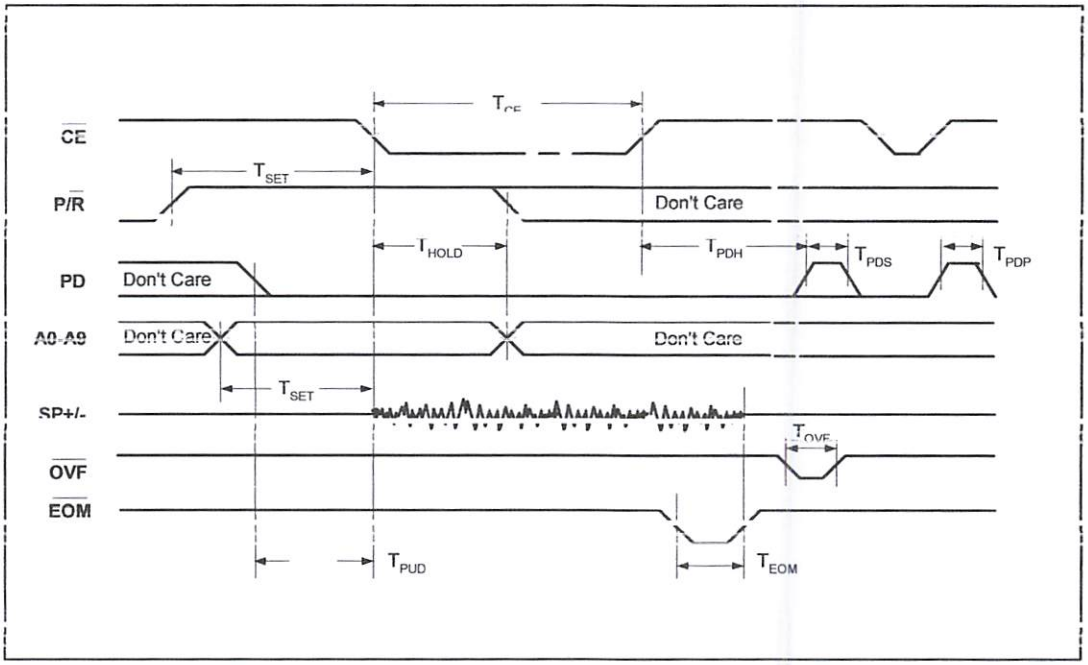

FIGURE 2: PLAYBACK

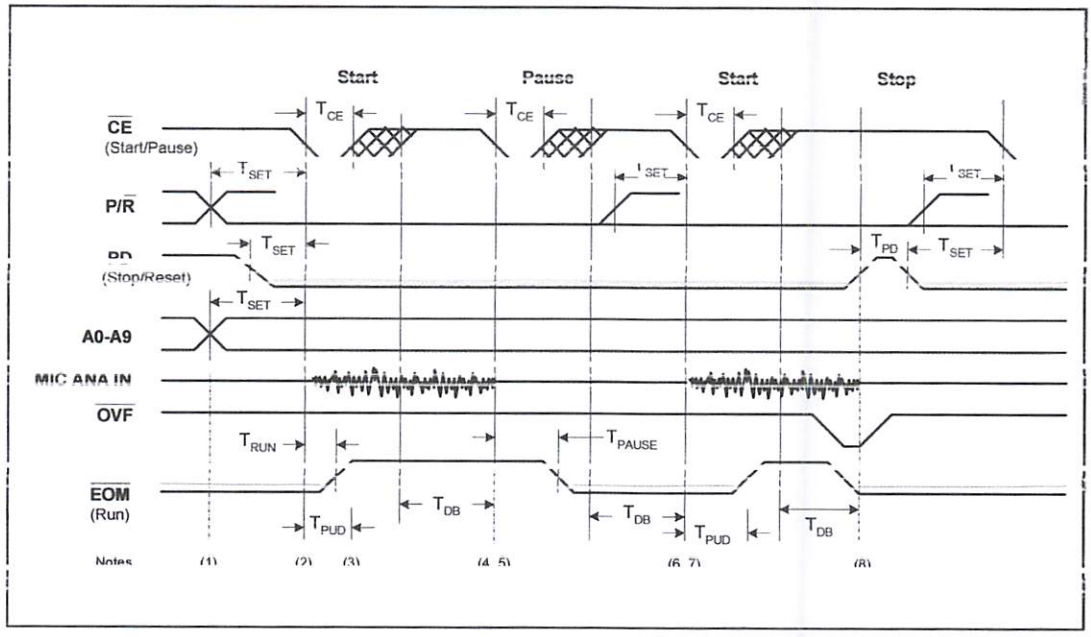

FIGURE 3: PUSH-BUTTON MODE RECORD

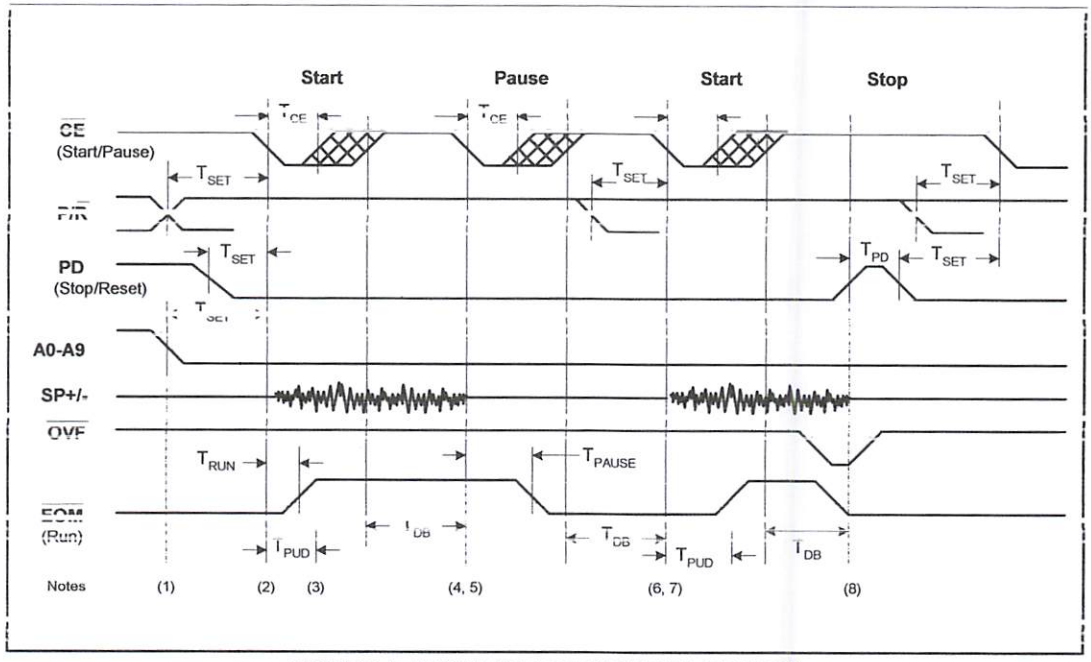

FIGURE 4: PUSH-BUTTON MODE PLAYBACK

Notes for Push-Button modes:

1. A9, A8, and A6 = 1 for push-button operation.
2. The first $\overline{CE}$ LOW pulse performs a start function.
3. The part will begin to play or record after a power-up delay T_{PUD}.
4. The part must have $\overline{CE}$ HIGH for a debounce period T_{DB} before it will recognize another falling edge of $\overline{CE}$ and pause.
5. The second $\overline{CE}$ LOW pulse, and every even pulse thereafter, performs a Pause function.
6. Again, the part must have $\overline{CE}$ HIGH for a debounce period T_{DB} before it will recognize another falling edge of $\overline{CE}$ which would restart an operation. In addition, the part will not do an internal power down until $\overline{CE}$ is HIGH for the T_{DB} time.
7. The third $\overline{CE}$ LOW pulse, and every odd pulse thereafter, performs a Resume function.
8. At any time, a HIGH level on PD will stop the current function, reset the address counter, and power down the device.

9. ABSOLUTE MAXIMUM RATINGS

TABLE 4: ABSOLUTE MAXIMUM RATINGS (DIE)

CONDITION	VALUE
Junction temperature	150°C
Storage temperature range	-65°C to +150°C
Voltage applied to any pad	(V_{SS} –0.3V) to (V_{CC} +0.3V)
Voltage applied to any pad (input current limited to ±20mA)	(V_{SS} –1.0V) to (V_{CC} +1.0V)
V_{CC} – V_{SS}	-0.3V to +7.0V

TABLE 5: ABSOLUTE MAXIMUM RATINGS (PACKAGED PARTS)

CONDITION	VALUE
Junction temperature	150°C
Storage temperature range	-65°C to +150°C
Voltage applied to any pin	(V_{SS} –0.3V) to (V_{CC} +0.3V)
Voltage applied to any pin (input current limited to ±20 mA)	(V_{SS} –1.0V) to (V_{CC} +1.0V)
Lead temperature (Soldering – 10sec)	300°C
V_{CC} – V_{SS}	-0.3V to +7.0V

Note: Stresses above those listed may cause permanent damage to the device. Exposure to the absolute maximum ratings may affect device reliability and performance. Functional operation is not implied at these conditions.

9.1 OPERATING CONDITIONS

TABLE 6: OPERATING CONDITIONS (DIE)

CONDITION	VALUE
Commercial operating temperature range	0°C to +50°C
Supply voltage (V_{CC}) [1]	+4.5V to +6.5V
Ground voltage (V_{SS}) [2]	0V

TABLE 7: OPERATING CONDITIONS (PACKAGED PARTS)

CONDITION	VALUE
Commercial operating temperature range [3]	0°C to +70°C
Supply voltage (V_{CC}) [1]	+4.5V to +5.5V
Ground voltage (V_{SS}) [2]	0V

[1] $V_{CC} = V_{CCA} = V_{CCD}$

[2] $V_{SS} = V_{SSA} = V_{SSD}$

[3] Case Temperature

10. ELECTRICAL CHARACTERISTICS

10.1. PARAMETERS FOR PACKAGED PARTS

TABLE 8. DC PARAMETERS – Packaged Parts

PARAMETER	SYMBOL	MIN[2]	TYP[1]	MAX[2]	UNITS	CONDITIONS
Input Low Voltage	V_{IL}			0.8	V	
Input High Voltage	V_{IH}	2.0			V	
Output Low Voltage	V_{OL}			0.4	V	I_{OL} = 4.0 mA
Output High Voltage	V_{OH}	V_{CC} - 0.4			V	I_{OH} = -10 µA
$\overline{OVF}$ Output High Voltage	V_{OH1}	2.4			V	I_{OH} = -1.6 mA
$\overline{EOM}$ Output High Voltage	V_{OH2}	V_{CC} – 1.0	V_{CC} - 0.8		V	I_{OH} = -3.2 mA
V_{CC} Current (Operating)	I_{CC}		25	30	mA	R_{EXT} = ∞ [3]
V_{CC} Current (Standby)	I_{SB}		1	10	µA	[3]
Input Leakage Current	I_{IL}			±1	µA	
Input Current HIGH w/Pull Down	I_{ILPD}			130	µA	Force V_{CC} [4]
Output Load Impedance	R_{EXT}	16			Ω	Speaker Load
Preamp Input Resistance	R_{MIC}	4	9	15	KΩ	MIC and MIC REF Pins
AUX IN Input Resistance	R_{AUX}	5	11	20	KΩ	
ANA IN Input Resistance	$R_{ANA\ IN}$	2.3	3	5	KΩ	
Preamp Gain 1	A_{PRE1}	21	24	26	dB	AGC = 0.0V
Preamp Gain 2	A_{PRE2}		-15	5	dB	AGC = 2.5V
AUX IN/SP+ Gain	A_{AUX}		0.98	1.0	V/V	
ANA IN to SP+/- Gain	A_{ARP}	21	23	26	dB	
AGC Output Resistance	R_{AGC}	2.5	5	9.5	KΩ	

Notes:

[1] Typical values @ T_A = 25° and V_{CC} = 5.0V.

[2] All Min/Max limits are guaranteed by Winbond via electrical testing or characterization. Not all specifications are 100 percent tested.

[3] V_{CCA} and V_{CCD} connected together.

[4] XCLK pin only.

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TABLE 9: AC PARAMETERS – Packaged Parts

CHARACTERISTIC	SYMBOL	MIN[2]	TYP[1]	MAX[2]	UNITS	CONDITIONS
Sampling Frequency	F_S					
ISD2560			8.0		kHz	[7]
ISD2575			6.4		kHz	[7]
ISD2590			5.3		kHz	[7]
ISD25120			4.0		kHz	[7]
Filter Pass Band	F_{CF}					
ISD2560			3.4		kHz	3 dB Roll-Off Point[3][8]
ISD2575			2.7		kHz	3 dB Roll-Off Point[3][8]
ISD2590			2.3		kHz	3 dB Roll-Off Point[3][8]
ISD25120			1.7		kHz	3 dB Roll-Off Point[3][8]
Record Duration	T_{REC}					
ISD2560		58.1	60.0	62.0	sec	Commercial Operation[7]
ISD2575		72.6	75.0	77.5	sec	Commercial Operation[7]
ISD2590		87.1	90.0	93.0	sec	Commercial Operation[7]
ISD25120		116.1	120.0	123.9	sec	Commercial Operation[7]
Playback Duration	T_{PLAY}					
ISD2560		58.1	60.0	62.0	sec	Commercial Operation
ISD2575		72.6	75.0	77.5	sec	Commercial Operation
ISD2590		87.1	90.0	93.0	sec	Commercial Operation
ISD25120		116.1	120.0	123.9	sec	Commercial Operation
$\overline{CE}$ Pulse Width	T_{CE}		100		nsec	
Control/Address Setup Time	T_{SET}		300		nsec	
Control/Address Hold Time	T_{HOLD}		0		nsec	
Power-Up Delay	T_{PUD}					
ISD2560		24.1	25.0	27.8	msec	Commercial Operation
ISD2575		30.2	31.3	34.3	msec	Commercial Operation
ISD2590		36.2	37.5	40.8	msec	Commercial Operation
ISD25120		48.2	50.0	53.6	msec	Commercial Operation
PD Pulse Width (record)	T_{PDR}					
ISD2560			25.0		msec	
ISD2575			31.25		msec	
ISD2590			37.5		msec	
ISD25120			50.0		msec	

TABLE 9: AC PARAMETERS – Packaged Parts (Cont'd)

CHARACTERISTIC	SYMBOL	MIN[2]	TYP[1]	MAX[2]	UNITS	CONDITIONS
PD Pulse Width (Play)	T_{PDP}					
ISD2560			12.5		msec	
ISD2575			15.625		msec	
ISD2590			18.75		msec	
ISD25120			25.0		msec	
PD Pulse Width (Static)	T_{PDS}		100		nsec	[6]
Power Down Hold	T_{PDH}		0		nsec	
$\overline{EOM}$ Pulse Width	T_{EOM}					
ISD2560			12.5		msec	
ISD2575			15.625		msec	
ISD2590			18.75		msec	
ISD25120			25.0		msec	
Overflow Pulse Width	T_{OVF}		6.5		µsec	
Total Harmonic Distortion	THD		1	2	%	@ 1 kHz
Speaker Output Power	P_{OUT}		12.2	50	mW	R_{EXT} = 16 Ω[4]
Voltage Across Speaker Pins	V_{OUT}			2.5	V p-p	R_{EXT} = 600 Ω
MIC Input Voltage	V_{IN1}			20	mV	Peak-to-Peak[5]
ANA IN Input Voltage	V_{IN2}			50	mV	Peak-to-Peak
AUX Input Voltage	V_{IN3}			1.25	V	Peak-to-Peak; R_{EXT} = 16 Ω

Notes:

[1] Typical values @ T_A = 25°C and V_{CC} = 5.0V.

[2] All Min/Max limits are guaranteed by Winbond via electrical testing or characterization. Not all specifications are 100 percent tested.

[3] Low-frequency cutoff depends upon the value of external capacitors (see Pin Descriptions)

[4] From AUX IN; if ANA IN is driven at 50 mV p-p, the P_{OUT} = 12.2 mW, typical.

[5] With 5.1 K Ω series resistor at ANA IN.

[6] T_{PDS} is required during a static condition, typically overflow.

[7] Sampling Frequency and playback Duration can vary as much as ±2.25 percent over the commercial temperature range. For greater stability, an external clock can be utilized (see Pin Descriptions)

[8] Filter specification applies to the antialiasing filter and the smoothing filter. Therefore, from input to output, expect a 6 dB drop by nature of passing through both filters.

10.1.1. Typical Parameter Variation with Voltage and Temperature (Packaged Parts)

Chart 1: Record Mode Operating Current (I_{CC})

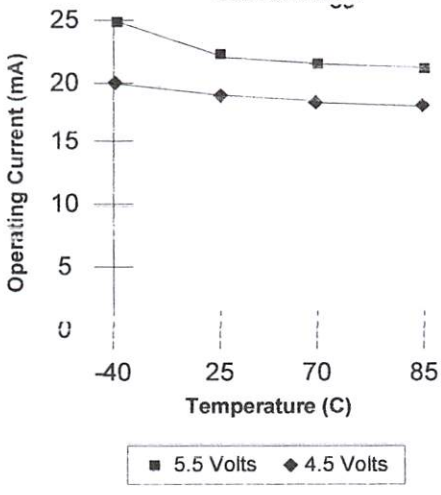


Chart 3: Standby Current (I_{SB})

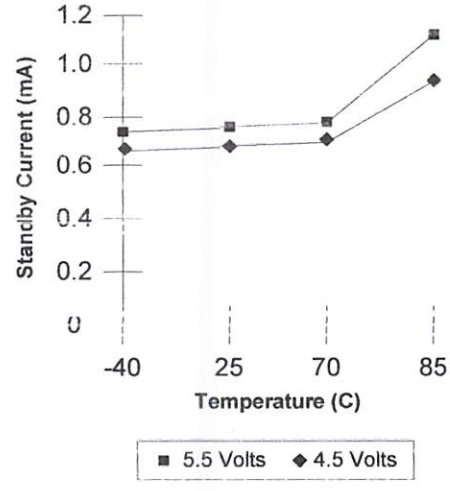


Chart 2: Total Harmonic Distortion

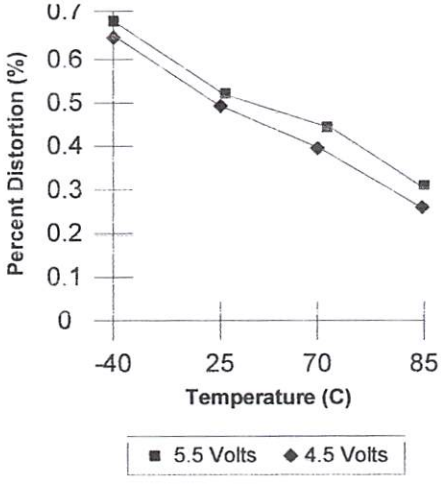
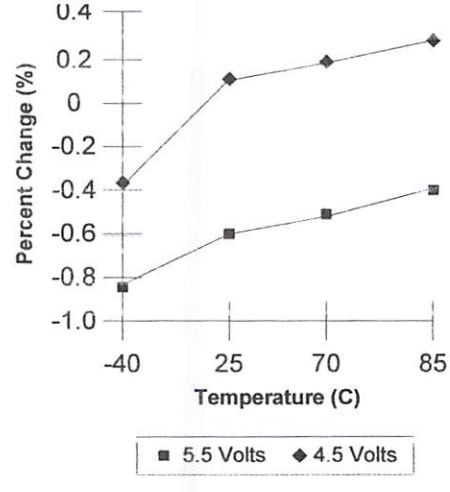


Chart 4: Oscillator Stability



10.2. PARAMETERS FOR DIE

TABLE 10: DC PARAMETERS – Die

PARAMETER	SYMBOL	MIN[2]	TYP[1]	MAX[2]	UNITS	CONDITIONS
Input Low Voltage	V_{IL}			0.8	V	
Input High Voltage	V_{IH}	2.0			V	
Output Low Voltage	V_{OL}			0.4	V	I_{OL} = 4.0 mA
Output High Voltage	V_{OH}	V_{CC} - 0.4			V	I_{OH} = -10 µA
OVF Output High Voltage	V_{OH1}	2.4			V	I_{OH} = -1.6 mA
$\overline{EOM}$ Output High Voltage	V_{OH2}	V_{CC} – 1.0	V_{CC} - 0.8		V	I_{OH} = -3.2 mA
V_{CC} Current (Operating)	I_{CC}		25	30	mA	R_{EXT} = ∞ [3]
V_{CC} Current (Standby)	I_{SB}		1	10	µA	[2]
Input Leakage Current	I_{IL}			±1	µA	
Input Current HIGH w/Pull Down	I_{ILPD}			130	µA	Force V_{CC} [4]
Output Load Impedance	R_{EXT}	16			Ω	Speaker Load
Preamp IN Input Resistance	R_{MIC}	4	9	15	KΩ	MIC and MIC REF Pads
AUX IN Input Resistance	R_{AUX}	5	11	20	KΩ	
ANA IN Input Resistance	$R_{ANA\ IN}$	2.3	3	5	KΩ	
Preamp Gain 1	A_{PRE1}	21	24	26	dB	AGC = 0.0V
Preamp Gain 2	A_{PRE2}		-15	5	dB	AGC = 2.5V
AUX IN/SP+ Gain	A_{AUX}		0.98	1.0	V/V	
ANA IN to SP+/- Gain	A_{ARP}	21	23	26	dB	
AGC Output Resistance	R_{AGC}	2.5	5	9.5	KΩ	

Notes:

[1] Typical values @ T_A = 25°C and V_{CC} = 5.0V.

[2] All Min/Max limits are guaranteed by Winbond via electrical testing or characterization. Not all specifications are 100 percent tested.

[3] V_{CCA} and V_{CCD} connected together.

[4] XCLK pad only.

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TABLE 11: AC PARAMETERS – Die

CHARACTERISTIC	SYMBOL	MIN[2]	TYP[1]	MAX[2]	UNITS	CONDITIONS
Sampling Frequency	F_S					
ISD2560			8.0		kHz	[7]
ISD2575			6.4		kHz	[7]
ISD2590			5.3		kHz	[7]
ISD25120			4.0		kHz	[7]
Filter Pass Band	F_{CF}					
ISD2560			3.4		kHz	3 dB Roll-Off Point[3][8]
ISD2575			2.7		kHz	3 dB Roll-Off Point[3][8]
ISD2590			2.3		kHz	3 dB Roll-Off Point[3][8]
ISD25120			1.7		kHz	3 dB Roll-Off Point[3][8]
Record Duration	T_{REC}					
ISD2560		58.1	60.0	62.0	sec	Commercial Operation[7]
ISD2575		72.6	75.0	77.5	sec	Commercial Operation[7]
ISD2590		87.1	90.0	93.0	sec	Commercial Operation[7]
ISD25120		116.1	120.0	123.9	sec	Commercial Operation[7]
Playback Duration	T_{PLAY}					
ISD2560		58.1	60.0	62.0	sec	Commercial Operation[7]
ISD2575		72.6	75.0	77.5	sec	Commercial Operation[7]
ISD2590		87.1	90.0	93.0	sec	Commercial Operation[7]
ISD25120		116.1	120.0	123.9	sec	Commercial Operation[7]
CE Pulse Width	T_{CE}		100		nsec	
Control/Address Setup Time	T_{SET}		300		nsec	
Control/Address Hold Time	T_{HOLD}		0		nsec	
Power-Up Delay	T_{PUD}					
ISD2560		24.1	25.0	27.8	msec	Commercial Operation
ISD2575		30.2	31.3	34.3	msec	Commercial Operation
ISD2590		36.2	37.5	40.8	msec	Commercial Operation
ISD25120		48.2	50.0	53.6	msec	Commercial Operation
PD Pulse Width (Record)	T_{PDR}					
ISD2560			25.0		msec	
ISD2575			31.25		msec	
ISD2590			37.5		msec	
ISD25120			50.0		msec	

TABLE 11: AC PARAMETERS – Die (Cont'd)

CHARACTERISTIC	SYMBOL	MIN[2]	TYP[1]	MAX[2]	UNITS	CONDITIONS
PD Pulse Width (Play)	T_{PDP}					
ISD2560			12.5		msec	
ISD2575			15.625		msec	
ISD2590			18.75		msec	
ISD25120			25.0		msec	
PD Pulse Width (Static)	T_{PDS}		100		nsec	[6]
Power Down Hold	T_{PDH}		0		nsec	
$\overline{EOM}$ Pulse Width	T_{EOM}					
ISD2560			12.5		msec	
ISD2575			15.625		msec	
ISD2590			18.75		msec	
ISD25120			25.0		msec	
Overflow Pulse Width	T_{OVF}		6.5		µsec	
Total Harmonic Distortion	THD		1	3	%	@ 1 kHz
Speaker Output Power	P_{OUT}		12.2	50	mW	R_{EXT} = 16 Ω[4]
Voltage Across Speaker Pins	V_{OUT}			2.5	V p-p	R_{EXT} = 600 Ω
MIC Input Voltage	V_{IN1}			20	mV	Peak-to-Peak[5]
ANA IN Input Voltage	V_{IN2}			50	mV	Peak-to-Peak
AUX Input Voltage	V_{IN3}			1.25	V	Peak-to-Peak; R_{EXT} = 16 Ω

Notes:

[1] Typical values @ T_A = 25°C and V_{CC} = 5.0V.

[2] All Min/Max limits are guaranteed by Winbond via electrical testing or characterization. Not all specifications are 100 percent tested.

[3] Low-frequency cutoff depends upon the value of external capacitors (see Pin Descriptions)

[4] From AUX IN; if ANA IN is driven at 50 mV p-p, the P_{OUT} = 12.2 mW, typical.

[5] With 5.1 K Ω series resistor at ANA IN.

[6] T_{PDS} is required during a static condition, typically overflow.

[7] Sampling Frequency and playback Duration can vary as much as ±2.25 percent over the commercial temperature range. For greater stability, an external clock can be utilized (see Pin Descriptions)

[8] Filter specification applies to the antialiasing filter and the smoothing filter. Therefore, from input to output, expect a 6 dB drop by nature of passing through both filters.

10.2.1. Typical Parameter Variation with Voltage and Temperature (Die)

Chart 5: Record Mode Operating Current (I_{CC})

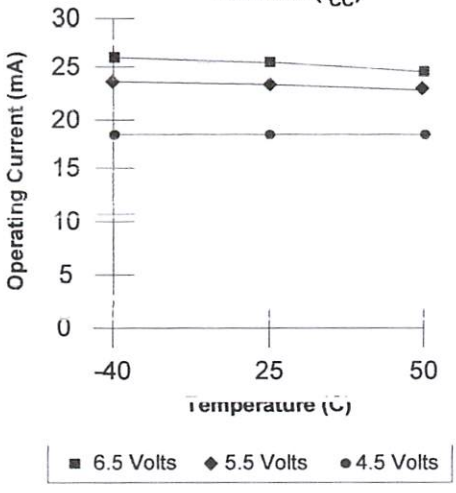


Chart 7: Standby Current (I_{SB})

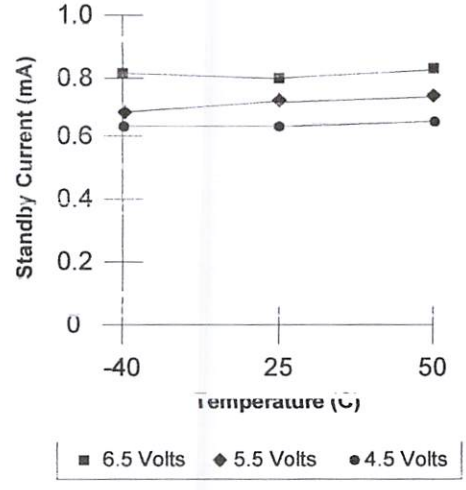


Chart 6: Total Harmonic Distortion

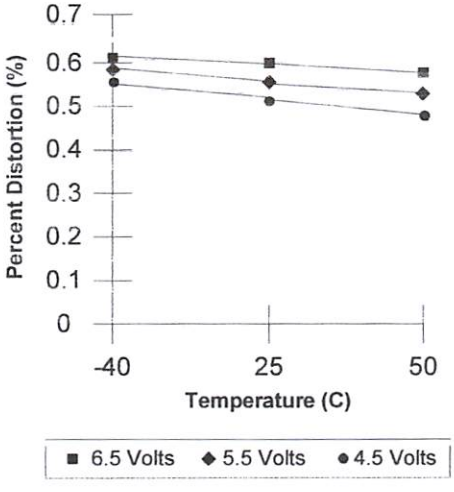
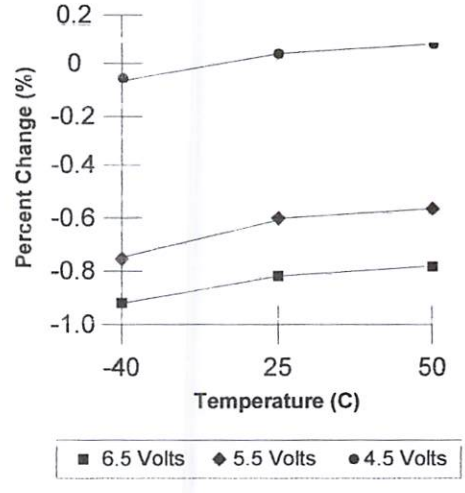


Chart 8: Oscillator Stability



10.3. PARAMETERS FOR PUSH-BUTTON MODE

TABLE 12: PARAMETERS FOR PUSH-BUTTON MODE

PARAMETER	SYMBOL	MIN[2]	TYP[1]	MAX[2]	UNITS	CONDITIONS
$\overline{CE}$ Pulse Width (Start/Pause)	T_{CE}		300		nsec	
Control/Address Setup Time	T_{SET}		300		nsec	
Power-Up Delay	T_{PUD}					
ISD2560			25.0		msec	
ISD2575			31.25		msec	
ISD2590			37.25		msec	
ISD25120			50.0		msec	
PD Pulse Width (Stop/Restart)	T_{PD}		300		nsec	
$\overline{CE}$ to $\overline{EOM}$ HIGH	T_{RUN}	25		400	nsec	
$\overline{CE}$ to $\overline{EOM}$ LOW	T_{PAUSE}	50		400	nsec	
$\overline{CE}$ HIGH Debounce	T_{DB}					
ISD2560		70		105	msec	
ISD2575		85		135	msec	
ISD2590		105		160	msec	
ISD25120		135		215	msec	

Notes:

[1] Typical values @ T_A = 25°C and V_{CC} = 5.0V.

[2] All Min/Max limits are guaranteed by Winbond via electrical testing or characterization. Not all specifications are 100 percent tested.

11. TYPICAL APPLICATION CIRCUIT

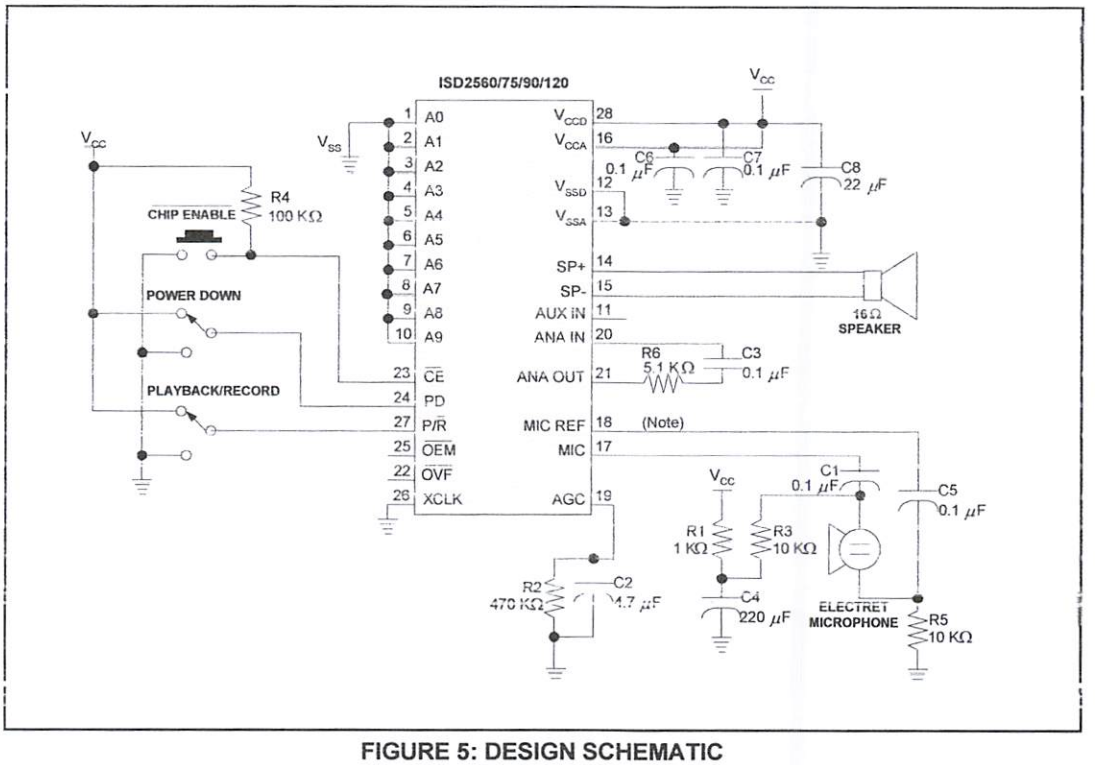


FIGURE 5: DESIGN SCHEMATIC

Note: If desired, pin 18 (PDIP package) may be left unconnected (microphone preamplifier noise will be higher). In this case, pin 18 must not be tied to any other signal or voltage. Additional design example schematics are provided below.

TABLE 13: APPLICATION EXAMPLE – BASIC DEVICE CONTROL

Control Step	Function	Action
1	Power up chip and select Record/Playback Mode	1. PD = LOW, 2. P/$\overline{R}$ = As desired
2	Set message address for record/playback	Set addresses A0-A9
3A	Begin playback	P/$\overline{R}$ = HIGH, $\overline{CE}$ = Pulse LOW
3B	Begin record	P/$\overline{R}$ = LOW, $\overline{CE}$ = LOW
4A	End playback	Automatic
4B	End record	PD or $\overline{CE}$ = HIGH

TABLE 14: APPLICATION EXAMPLE – PASSIVE COMPONENT FUNCTIONS

Part	Function	Comments
R1	Microphone power supply decoupling	Reduces power supply noise
R2	Release time constant	Sets release time for AGC
R3, R5	Microphone biasing resistors	Provides biasing for microphone operation
R4	Series limiting resistor	Reduces level to prevent distortion at higher supply voltages
R6	Series limiting resistor	Reduces level to high supply voltages
C1, C5	Microphone DC-blocking capacitor Low-frequency cutoff	Decouples microphone bias from chip. Provides single-pole low-frequency cutoff and command mode noise rejection.
C2	Attack/Release time constant	Sets attack/release time for AGC
C3	Low-frequency cutoff capacitor	Provides additional pole for low-frequency cutoff
C4	Microphone power supply decoupling	Reduces power supply noise
C6, C7, C8	Power supply capacitors	Filter and bypass of power supply

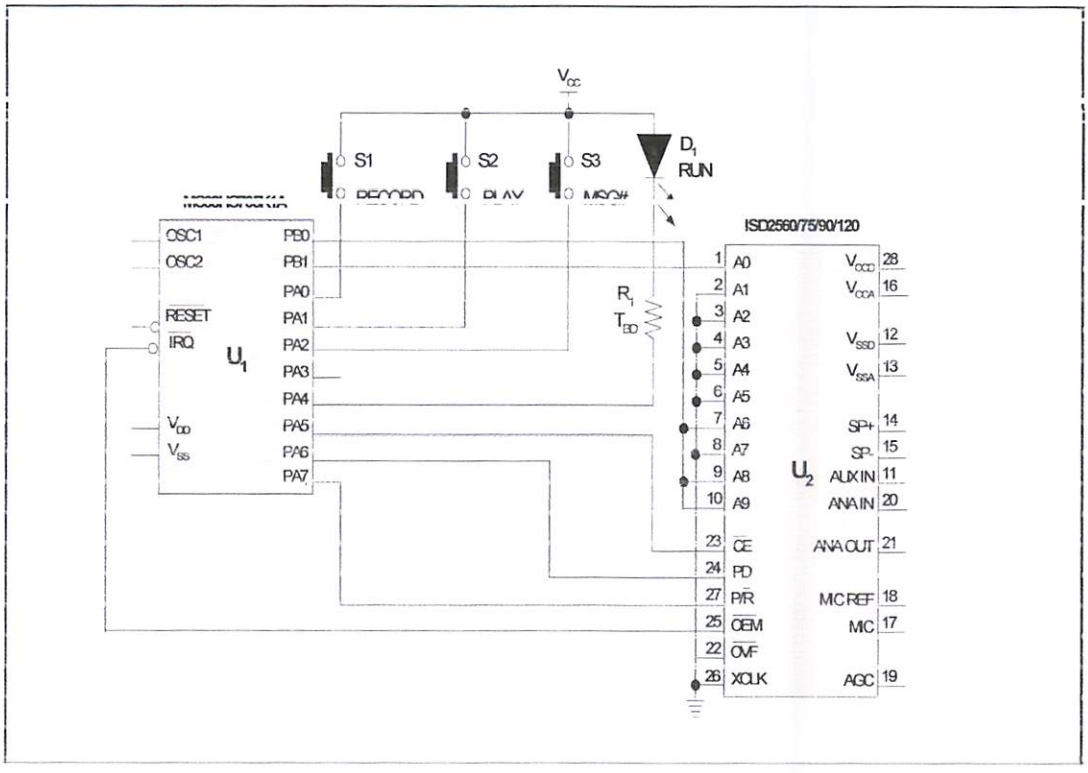


FIGURE 6: ISD2560/75/90/120 APPLICATION EXAMPLE – MICROCONTROLLER/ISD2500 INTERFACE

In this simplified block diagram of a microcontroller application, the Push-Button Mode and message cueing are used. The microcontroller is a 16-pin version with enough port pins for buttons, an LED, and the ISD2500 series device. The software can be written to use three buttons: one each for play and record, and one for message selection. Because the microcontroller is interpreting the buttons and commanding the ISD2500 device, software can be written for any function desired in a particular application.

Note: Winbond does not recommend connecting address lines directly to a microprocessor bus. Address lines should be externally latched.

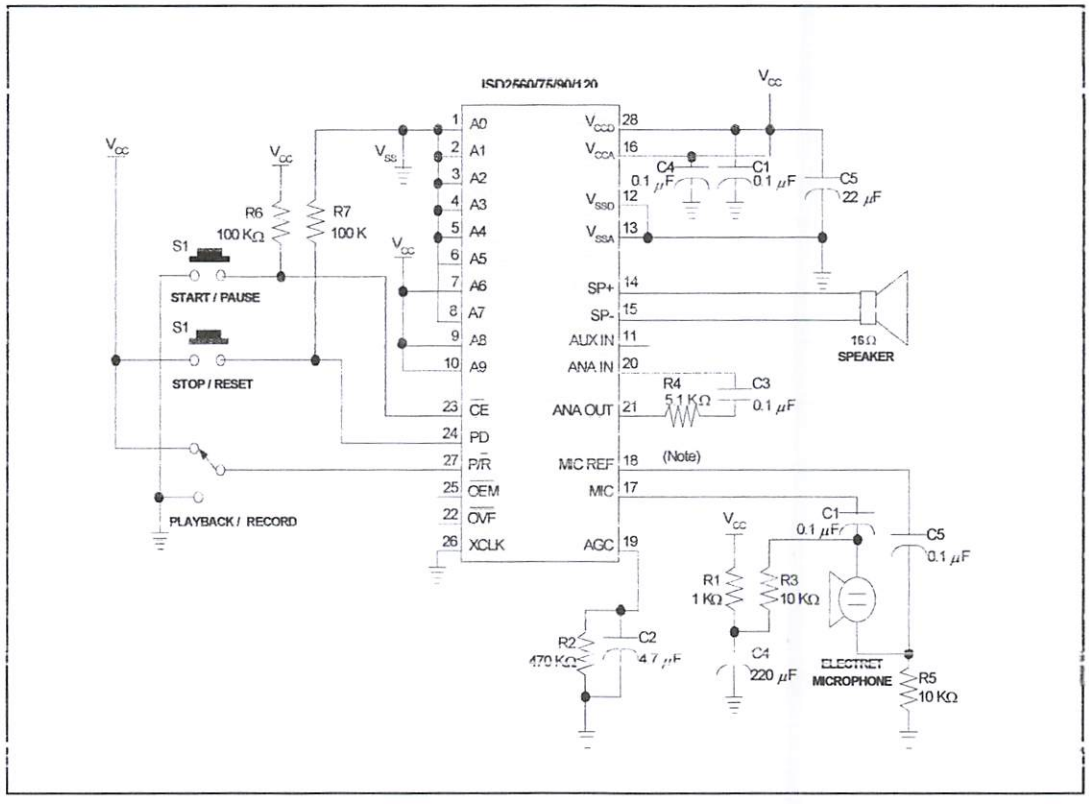


FIGURE 7: ISD2560/75/90/120 APPLICATION EXAMPLE – PUSH-BUTTON

Note: Please refer to page 13 for more details.

TABLE 15: APPLICATION EXAMPLE – PUSH-BUTTON CONTROL

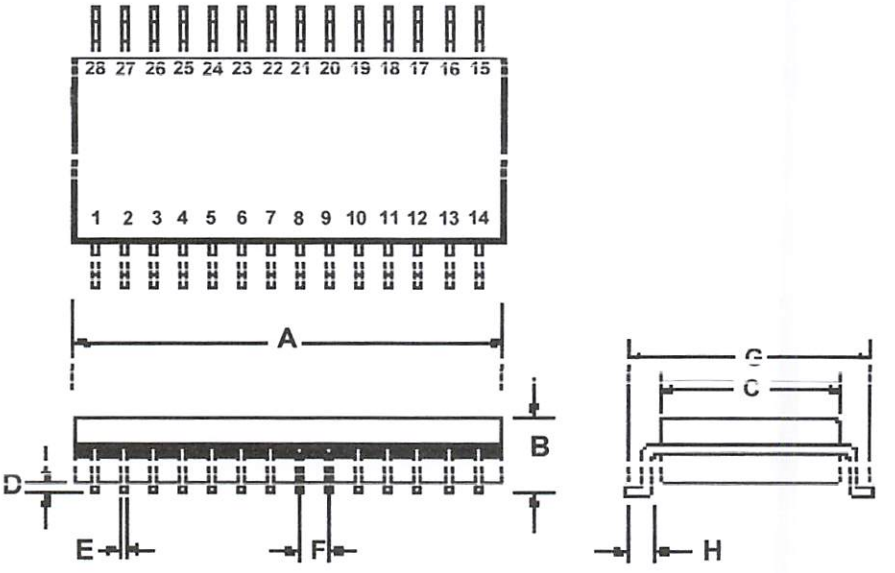
Control Step	Function	Action
1	Select Record/Playback Mode	$P/\overline{R}$ = As desired
2A	Begin playback	$P/\overline{R}$ = HIGH, $\overline{CE}$ = Pulse LOW
2B	Begin record	$P/\overline{R}$ = LOW, $\overline{CE}$ = Pulse LOW
3	Pause record or playback	$\overline{CE}$ = Pulsed LOW
4A	End playback	Automatic at $\overline{EOM}$ marker or PD = Pulsed HIGH
4B	End record	PD = Pulsed HIGH

TABLE 16: APPLICATION EXAMPLE – PASSIVE COMPONENT FUNCTIONS

Part	Function	Comments
R2	Release time constant	Sets release time for AGC
R4	Series limiting resistor	Reduces level to prevent distortion at higher supply voltages
R6, R7	Pull-up and pull-down resistors	Defines static state of inputs
C1, C4, C5	Power supply capacitors	Filters and bypass of power supply
C2	Attack/Release time constant	Sets attack/release time for AGC
C3	Low-frequency cutoff capacitor	Provides additional pole for low-frequency cutoff

12. PACKAGE DRAWING AND DIMENSIONS

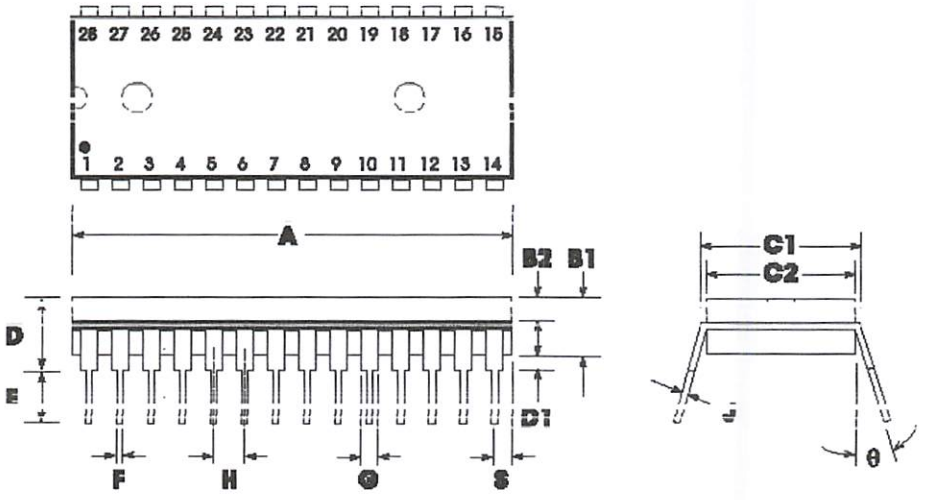
12.1. 28-LEAD 300-MIL PLASTIC SMALL OUTLINE IC (SOIC)



	INCHES			MILLIMETERS		
	Min	Nom	Max	Min	Nom	Max
A	0.701	0.706	0.711	17.81	17.93	18.06
B	0.097	0.101	0.104	2.46	2.56	2.64
C	0.292	0.296	0.299	7.42	7.52	7.59
D	0.005	0.009	0.0115	0.127	0.22	0.29
E	0.014	0.016	0.019	0.35	0.41	0.48
F		0.050			1.27	
G	0.400	0.406	0.410	10.16	10.31	10.41
H	0.024	0.032	0.040	0.61	0.81	1.02

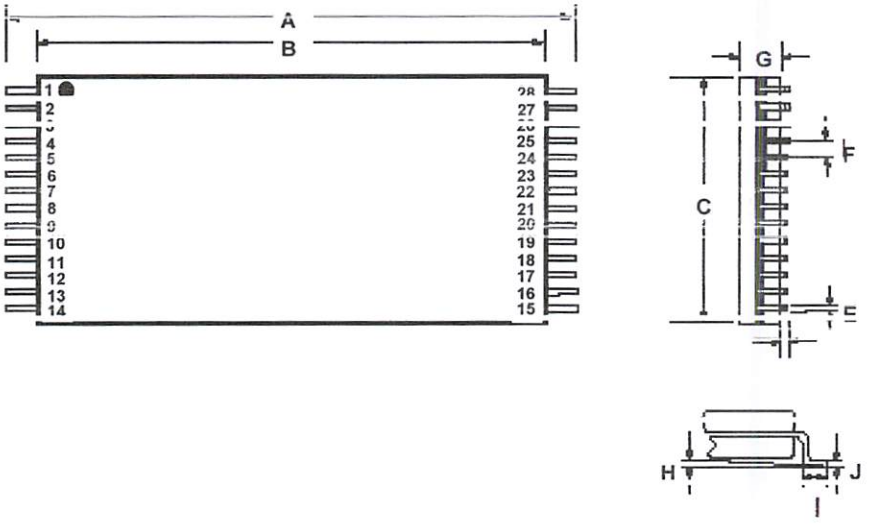
Note: Lead copianarity to be within 0.004 inches.

12.2. 28-LEAD 600-MIL PLASTIC DUAL INLINE PACKAGE (PDIP)



	INCHES			MILLIMETERS		
	Min	Nom	Max	Min	Nom	Max
A	1.445	1.450	1.455	36.70	36.83	36.96
B1		0.150			3.81	
B2	0.065	0.070	0.075	1.65	1.78	1.91
C1	0.600		0.625	15.24		15.88
C2	0.530	0.540	0.550	13.46	13.72	13.97
D			0.19			4.83
D1	0.015			0.38		
E	0.125		0.135	3.18		3.43
F	0.015	0.018	0.022	0.38	0.46	0.56
G	0.055	0.060	0.065	1.40	1.52	1.62
H		0.100			2.54	
J	0.008	0.010	0.012	0.20	0.25	0.30
S	0.070	0.075	0.080	1.78	1.91	2.03
q	0°		15°	0°		15°

12.3. 28-LEAD 8X13.4MM PLASTIC THIN SMALL OUTLINE PACKAGE (TSOP) TYPE 1



Plastic Thin Small Outline Package (TSOP) Type 1 Dimensions

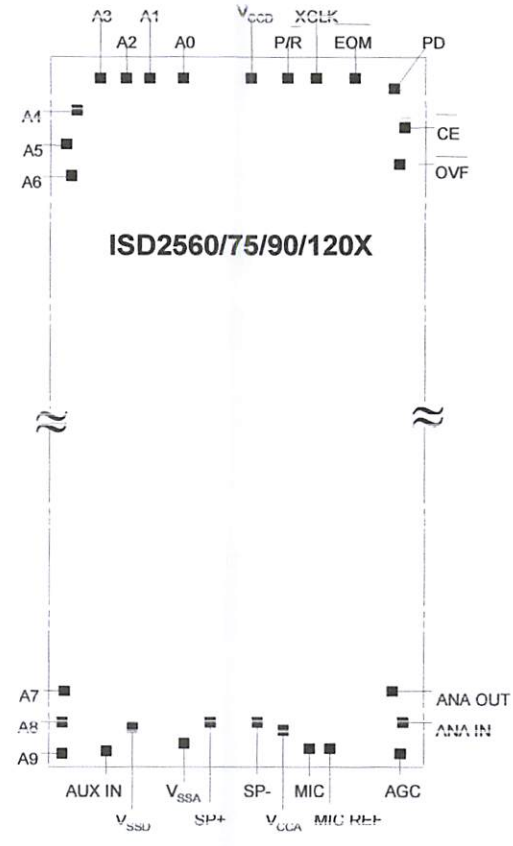
	INCHES			MILLIMETERS		
	Min	Nom	Max	Min	Nom	Max
A	0.520	0.528	0.535	13.20	13.40	13.60
B	0.461	0.465	0.469	11.70	11.80	11.90
C	0.311	0.315	0.319	7.90	8.00	8.10
D	0.002		0.006	0.05		0.15
E	0.007	0.009	0.011	0.17	0.22	0.27
F		0.0217			0.55	
G	0.037	0.039	0.041	0.95	1.00	1.05
H	0^0	3^0	6^0	0^0	3^0	6^0
I	0.020	0.022	0.028	0.50	0.55	0.70
J	0.004		0.008	0.10		0.21

Note: *Lead coplanarity to be within 0.004 inches.*

12.4. ISD2560/75/95/120 PRODUCT BONDING PHYSICAL LAYOUT (DIE) [1]

ISD2560/75/95/120

- Die Dimensions
  X: 149.5 ± 1 mils
  Y: 262.0 ± 1 mils
- Die Thickness [2]
  11.8 ± .4 mils
- Pad Opening
  111 x 111 microns
  4.4 x 4.4 mils



Notes:

[1] The backside of die is internally connected to V_{SS}. It **MUST NOT** be connected to any other potential or damage may occur.

[2] Die thickness is subject to change, please contact Winbond factory for status and availability.

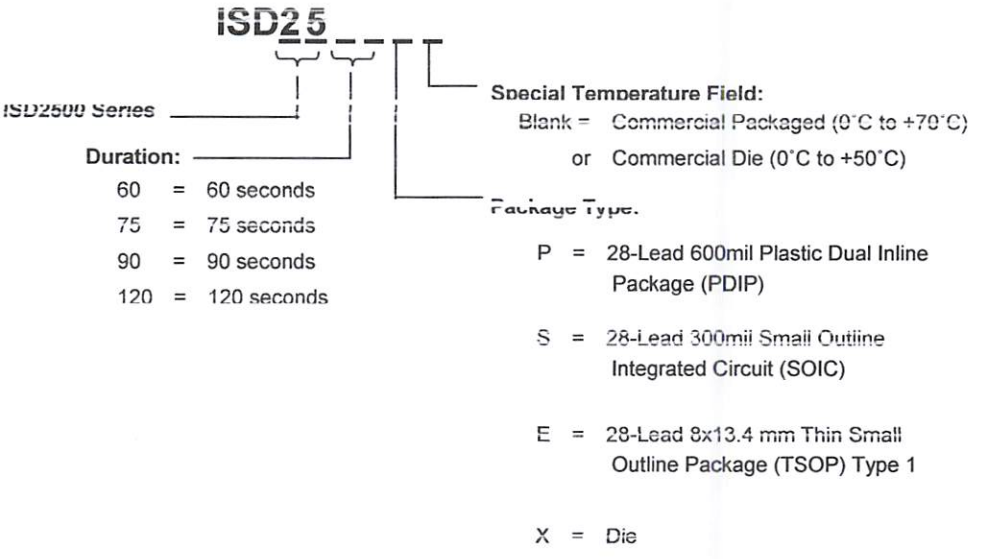
ISD2560/75/90/120 PRODUCT PAD DESIGNATIONS

(with respect to die center)

Pad	Pad Name	X Axis (µm)	Y Axis (µm)
A0	Address 0	-897.9	3135.2
A1	Address 1	-1115.4	3135.2
A2	Address 2	-1331.0	3135.2
A3	Address 3	-1544.0	3135.2
A4	Address 4	-1640.4	2888.0
A5	Address 5	-1698.2	2671.0
A6	Address 6	-1698.2	2441.5
A7	Address 7	-1731.2	-2563.2
A8	Address 8	-1731.2	-2768.4
A9	Address 9	-1731.2	-3050.8
AUX IN	Auxiliary Input	-1410.2	-3115.7
V_{SSD}	V_{SS} Digital Power Supply	-1112.4	-3096.5
V_{SSA}	V_{SS} Analog Power Supply	-408.2	-3138.9
SP+	Speaker Output +	-46.65	-3068.4
SP-	Speaker Output -	386.1	-3068.4
V_{CCA}	V_{CC} Analog Power Supply	746.9	-3110.8
MIC	Microphone Input	1101.2	-3146.0
MIC REF	Microphone Reference	1294.7	-3146.0
AGC	Automatic Gain Control	1666.4	-3130.3
ANA IN	Analog Input	1728.6	-2654.0
ANA OUT	Analog Output	1700.9	-2411.0
$\overline{OVF}$	Overflow Output	1674.6	2489.5
$\overline{CE}$	Chip Enable Input	1726.7	2824.4
PD	Power Down Input	1730.5	3094.0
$\overline{EOM}$	End of Message	1341.2	3122.1
XCLK	No Connect (optional)	986.5	3160.7
$P/\overline{R}$	Playback/Record	807.2	3163.4
V_{CCD}	V_{CC} Digital Power Supply	544.4	3159.6

13. ORDERING INFORMATION

Product Number Descriptor Key



When ordering ISD2560/75/90/120 products refer to the following part numbers which are supported in volume for this product series. Consult the local Winbond Sales Representative or Distributor for availability information.

Part Number	Part Number	Part Number	Part Number
ISD2560P	ISD2575P	ISD2590P	ISD25120P
ISD2560S	ISD2575S	ISD2590S	ISD25120S
ISD2560E	ISD2575E	ISD2590E	
ISD2560X	ISD2575X	ISD2590X	ISD25120X

For the latest product information, access Winbond's worldwide website at
http://www.winbond-usa.com

14. VERSION HISTORY

VERSION	DATE	PAGE	DESCRIPTION
0	Apr. 1998	All	Preliminary Specifications
1.0	May 2003	All	Re-format the document. Update TSOP pin configuration. Revise Overflow pad designation.

Winbond Electronics Corp.

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19-0410; Rev 3; 7/96

MAXIM

±15kV ESD-Protected, Slew-Rate-Limited, Low-Power, RS-485/RS-422 Transceivers

General Description

The MAX481E, MAX483E, MAX485E, MAX487E–MAX491E, and MAX1487E are low-power transceivers for RS-485 and RS-422 communications in harsh environments. Each driver output and receiver input is protected against ±15kV electrostatic discharge (ESD) shocks, without latchup. These parts contain one driver and one receiver. The MAX483E, MAX487E, MAX488E, and MAX489E feature reduced slew-rate drivers that minimize EMI and reduce reflections caused by improperly terminated cables, thus allowing error-free data transmission up to 250kbps. The driver slew rates of the MAX481E, MAX485E, MAX490E, MAX491E, and MAX1487E are not limited, allowing them to transmit up to 2.5Mbps.

These transceivers draw as little as 120µA supply current when unloaded or when fully loaded with disabled drivers (see *Selection Table*). Additionally, the MAX481E, MAX483E, and MAX487E have a low-current shutdown mode in which they consume only 0.5µA. All parts operate from a single +5V supply.

Drivers are short-circuit current limited, and are protected against excessive power dissipation by thermal shutdown circuitry that places their outputs into a high-impedance state. The receiver input has a fail-safe feature that guarantees a logic-high output if the input is open circuit.

The MAX487E and MAX1487E feature quarter-unit-load receiver input impedance, allowing up to 128 transceivers on the bus. The MAX488E–MAX491E are designed for full-duplex communications, while the MAX481E, MAX483E, MAX485E, MAX487E, and MAX1487E are designed for half-duplex applications. For applications that are not ESD sensitive see the pin- and function-compatible MAX481, MAX483, MAX485, MAX487–MAX491, and MAX1487.

Applications

Low-Power RS-485 Transceivers
Low-Power RS-422 Transceivers
Level Translators
Transceivers for EMI-Sensitive Applications
Industrial-Control Local Area Networks

Features

- **ESD Protection: ±15kV—Human Body Model**
- **Slew-Rate Limited for Error-Free Data Transmission (MAX483E/487E/488E/489E)**
- **Low Quiescent Current:**
  120µA (MAX483E/487E/488E/489E)
  230µA (MAX1487E)
  300µA (MAX481E/485E/490E/491E)
- **-7V to +12V Common-Mode Input Voltage Range**
- **Three-State Outputs**
- **30ns Propagation Delays, 5ns Skew (MAX481E/485E/490E/491E/1487E)**
- **Full-Duplex and Half-Duplex Versions Available**
- **Allows up to 128 Transceivers on the Bus (MAX487E/MAX1487E)**
- **Current Limiting and Thermal Shutdown for Driver Overload Protection**

Ordering Information

PART	TEMP. RANGE	PIN-PACKAGE
MAX481ECPA	0°C to +70°C	8 Plastic DIP
MAX481ECSA	0°C to +70°C	8 SO
MAX481EEPA	-40°C to +85°C	8 Plastic DIP
MAX481EESA	-40°C to +85°C	8 SO

Ordering Information continued on last page.

Selection Table

PART NUMBER	HALF/FULL DUPLEX	DATA RATE (Mbps)	SLEW-RATE LIMITED	LOW-POWER SHUTDOWN	RECEIVER/ DRIVER ENABLE	QUIESCENT CURRENT (µA)	NUMBER OF TRANSMITTERS ON BUS	PIN COUNT
MAX481E	Half	2.5	No	Yes	Yes	300	32	8
MAX483E	Half	0.25	Yes	Yes	Yes	120	32	8
MAX485E	Half	2.5	No	No	Yes	300	32	8
MAX487E	Half	0.25	Yes	Yes	Yes	120	128	8
MAX488E	Full	0.25	Yes	No	No	120	32	8
MAX489E	Full	0.25	Yes	No	Yes	120	32	14
MAX490E	Full	2.5	No	No	No	300	32	8
MAX491E	Full	2.5	No	No	Yes	300	32	14
MAX1487E	Half	2.5	No	No	Yes	230	128	8

±15kV ESD-Protected, Slew-Rate-Limited, Low-Power, RS-485/RS-422 Transceivers

ABSOLUTE MAXIMUM RATINGS

Supply Voltage (V_{CC}) 12V
Control Input Voltage ($\overline{RE}$, DE) ..... -0.5V to (V_{CC} + 0.5V)
Driver Input Voltage (DI) ..... -0.5V to (V_{CC} + 0.5V)
Driver Output Voltage (Y, Z; A, B) ..... -8V to +12.5V
Receiver Input Voltage (A, B) ..... -8V to +12.5V
Receiver Output Voltage (RO) ..... -0.5V to (V_{CC} + 0.5V)
Continuous Power Dissipation (T_A = +70°C)
8-Pin Plastic DIP (derate 9.09mW/°C above +70°C) 727mW
14-Pin Plastic DIP (derate 10.00mW/°C above +70°C) 800mW
8-Pin SO (derate 5.88mW/°C above +70°C) 471mW
14-Pin SO (derate 8.33mW/°C above +70°C) 667mW
Operating Temperature Ranges
MAX4__C__/MAX1487EC__A ..... 0°C to +70°C
MAX4__E__/MAX1487EE__A ..... -40°C to +85°C
Storage Temperature Range ..... -65°C to +160°C
Lead Temperature (soldering, 10sec) ..... +300°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC ELECTRICAL CHARACTERISTICS

(V_{CC} = 5V ±5%, T_A = T_{MIN} to T_{MAX}, unless otherwise noted.) (Notes 1, 2)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Differential Driver Output (no load)	V_{OD1}					5	V
Differential Driver Output (with load)	V_{OD2}	R = 50Ω (RS-422)		2			V
		R = 27Ω (RS-485), Figure 8		1.5		5	
Change in Magnitude of Driver Differential Output Voltage for Complementary Output States	ΔV_{OD}	R = 27Ω or 50Ω, Figure 8				0.2	V
Driver Common-Mode Output Voltage	V_{OC}	R = 27Ω or 50Ω, Figure 8				3	V
Change in Magnitude of Driver Common-Mode Output Voltage for Complementary Output States	ΔV_{OD}	R = 27Ω or 50Ω, Figure 8				0.2	V
Input High Voltage	V_{IH}	DE, DI, $\overline{RE}$		2.0			V
Input Low Voltage	V_{IL}	DE, DI, $\overline{RE}$				0.8	V
Input Current	I_{IN1}	DE, DI, $\overline{RE}$				±2	µA
Input Current (A, B)	I_{IN2}	DE = 0V; V_{CC} = 0V or 5.25V, all devices except MAX487E/MAX1487E	V_{IN} = 12V			1.0	mA
			V_{IN} = -7V			-0.8	
		MAX487E/MAX1487E, DE = 0V, V_{CC} = 0V or 5.25V	V_{IN} = 12V			0.25	mA
			V_{IN} = -7V			-0.2	
Receiver Differential Threshold Voltage	V_{TH}	-7V ≤ V_{CM} ≤ 12V		-0.2		0.2	V
Receiver Input Hysteresis	ΔV_{TH}	V_{CM} = 0V			70		mV
Receiver Output High Voltage	V_{OH}	I_O = -4mA, V_{ID} = 200mV		3.5			V
Receiver Output Low Voltage	V_{OL}	I_O = 4mA, V_{ID} = -200mV				0.4	V
Three-State (high impedance) Output Current at Receiver	I_{OZR}	0.4V ≤ V_O ≤ 2.4V				±1	µA
Receiver Input Resistance	R_{IN}	-7V ≤ V_{CM} ≤ 12V, all devices except MAX487E/MAX1487E		12			kΩ
		-7V ≤ V_{CM} ≤ 12V, MAX487E/MAX1487E		48			kΩ

DC ELECTRICAL CHARACTERISTICS (continued)

(V_{CC} = 5V ±5%, T_A = T_{MIN} to T_{MAX}, unless otherwise noted.) (Notes 1, 2)

PARAMETER	SYMBOL	CONDITIONS			MIN	TYP	MAX	UNITS
No-Load Supply Current (Note 3)	I_{CC}	MAX488E/MAX489E, DE, DI, $\overline{RE}$ = 0V or V_{CC}				120	250	µA
		MAX490E/MAX491E, DE, DI, $\overline{RE}$ = 0V or V_{CC}				300	500	
		MAX481E/MAX485E, $\overline{RE}$ = 0V or V_{CC}	DE = V_{CC}			500	900	
			DE = 0V			300	500	
		MAX1487E, $\overline{RE}$ = 0V or V_{CC}	DE = V_{CC}			300	500	
			DE = 0V			230	400	
		MAX483E/MAX487E, $\overline{RE}$ = 0V or V_{CC}	DE = V_{CC}	MAX483E		350	650	
				MAX487E		250	400	
			DE = 0V			120	250	
Supply Current in Shutdown	I_{SHDN}	MAX481E/483E/487E, DE = 0V, $\overline{RE}$ = V_{CC}				0.5	10	µA
Driver Short-Circuit Current, V_O = High	I_{OSD1}	-7V ≤ V_O ≤12V (Note 4)			35		250	mA
Driver Short-Circuit Current, V_O = Low	I_{OSD2}	-7V ≤ V_O ≤12V (Note 4)			35		250	mA
Receiver Short-Circuit Current	I_{OSR}	0V ≤ V_O ≤ V_{CC}			7		95	mA
ESD Protection		A, B, Y and Z pins, tested using Human Body Model				±15		kV

SWITCHING CHARACTERISTICS—MAX481E/MAX485E, MAX490E/MAX491E, MAX1487E

(V_{CC} = 5V ±5%, T_A = T_{MIN} to T_{MAX}, unless otherwise noted.) (Notes 1, 2)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Driver Input to Output	t_{PLH}	Figures 10 and 12, R_{DIFF} = 54Ω, C_{L1} = C_{L2} = 100pF		10	40	60	ns
	t_{PHL}			10	40	60	
Driver Output Skew to Output	t_{SKEW}	Figures 10 and 12, R_{DIFF} = 54Ω, C_{L1} = C_{L2} = 100pF			5	10	ns
Driver Rise or Fall Time	t_R, t_F	Figures 10 and 12, R_{DIFF} = 54Ω, C_{L1} = C_{L2} = 100pF	MAX481E, MAX485E, MAX1487E	3	20	40	ns
			MAX490EC/E, MAX491EC/E	5	20	25	
Driver Enable to Output High	t_{ZH}	Figures 11 and 13, C_L = 100pF, S2 closed			45	70	ns
Driver Enable to Output Low	t_{ZL}	Figures 11 and 13, C_L = 100pF, S1 closed			45	70	ns
Driver Disable Time from Low	t_{LZ}	Figures 11 and 13, C_L = 15pF, S1 closed			45	70	ns
Driver Disable Time from High	t_{HZ}	Figures 11 and 13, C_L = 15pF, S2 closed			45	70	ns
Receiver Input to Output	t_{PLH}, t_{PHL}	Figures 10 and 14, R_{DIFF} = 54Ω, C_{L1} = C_{L2} = 100pF	MAX481E, MAX485E, MAX1487E	20	60	200	ns
			MAX490EC/E, MAX491EC/E	20	60	150	
$\lvert t_{PLH} - t_{PHL} \rvert$ Differential Receiver Skew	t_{SKD}	Figures 10 and 14, R_{DIFF} = 54Ω, C_{L1} = C_{L2} = 100pF			5		ns
Receiver Enable to Output Low	t_{ZL}	Figures 9 and 15, C_{RL} = 15pF, S1 closed			20	50	ns
Receiver Enable to Output High	t_{ZH}	Figures 9 and 15, C_{RL} = 15pF, S2 closed			20	50	ns
Receiver Disable Time from Low	t_{LZ}	Figures 9 and 15, C_{RL} = 15pF, S1 closed			20	50	ns
Receiver Disable Time from High	t_{HZ}	Figures 9 and 15, C_{RL} = 15pF, S2 closed			20	50	ns
Maximum Data Rate	f_{MAX}			2.5			Mbps
Time to Shutdown	t_{SHDN}	MAX481E (Note 5)		50	200	600	ns

±15kV ESD-Protected, Slew-Rate-Limited, Low-Power, RS-485/RS-422 Transceivers

SWITCHING CHARACTERISTICS—MAX481E/MAX485E, MAX490E/MAX491E, MAX1487E (continued)

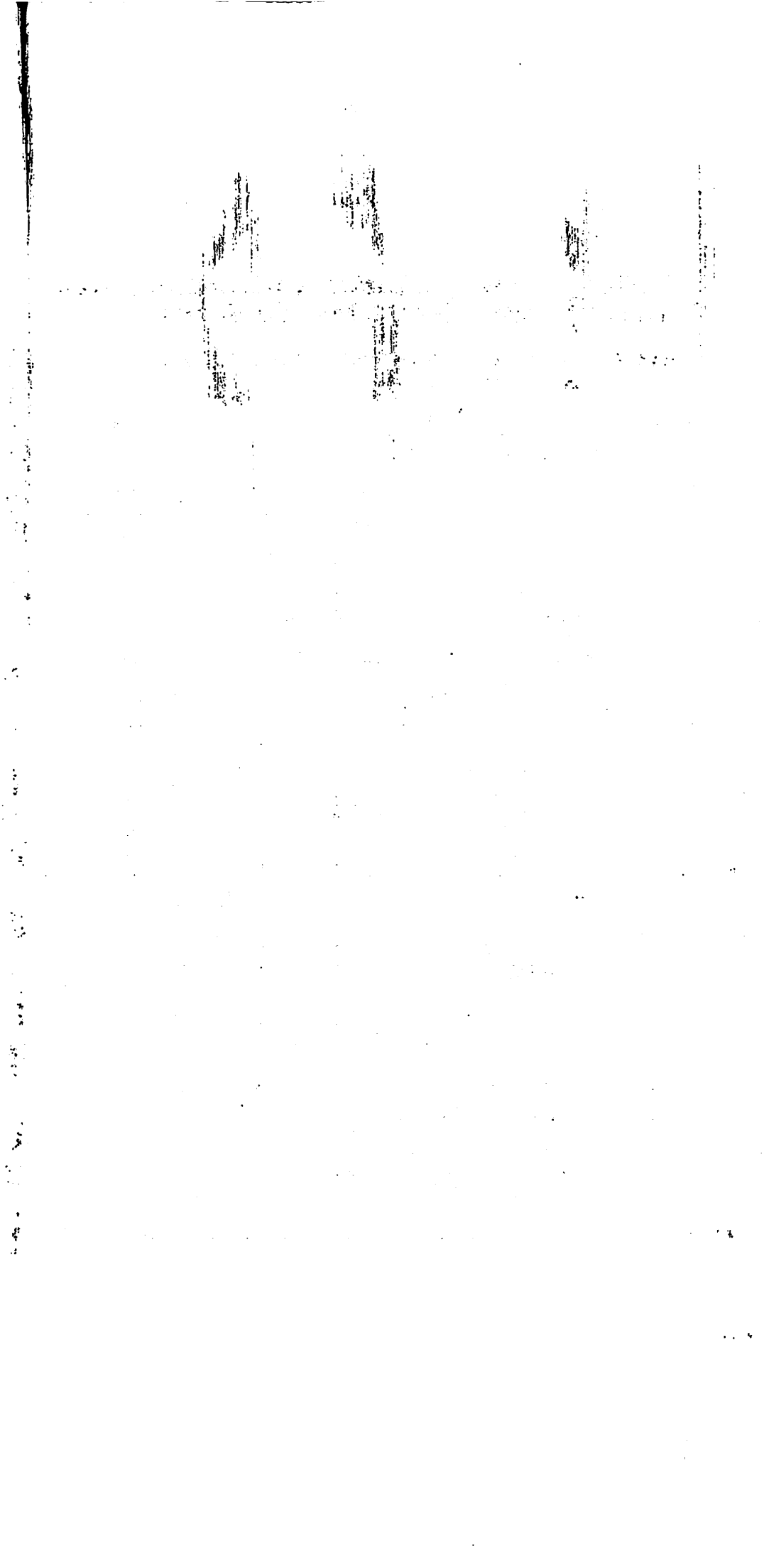
(V_{CC} = 5V ±5%, T_A = T_{MIN} to T_{MAX}, unless otherwise noted.) (Notes 1, 2)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Driver Enable from Shutdown to Output High (MAX481E)	$t_{ZH(SHDN)}$	Figures 11 and 13, C_L = 100pF, S2 closed		45	100	ns
Driver Enable from Shutdown to Output Low (MAX481E)	$t_{ZL(SHDN)}$	Figures 11 and 13, C_L = 100pF, S1 closed		45	100	ns
Receiver Enable from Shutdown to Output High (MAX481E)	$t_{ZH(SHDN)}$	Figures 9 and 15, C_L = 15pF, S2 closed, A - B = 2V		225	1000	ns
Receiver Enable from Shutdown to Output Low (MAX481E)	$t_{ZL(SHDN)}$	Figures 9 and 15, C_L = 15pF, S1 closed, B - A = 2V		225	1000	ns

SWITCHING CHARACTERISTICS—MAX483E, MAX487E/MAX488E/MAX489E

(V_{CC} = 5V ±5%, T_A = T_{MIN} to T_{MAX}, unless otherwise noted.) (Notes 1, 2)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Driver Input to Output	t_{PLH}	Figures 10 and 12, R_{DIFF} = 54Ω, C_{L1} = C_{L2} = 100pF	250	800	2000	ns
	t_{PHL}		250	800	2000	
Driver Output Skew to Output	t_{SKEW}	Figures 10 and 12, R_{DIFF} = 54Ω, C_{L1} = C_{L2} = 100pF		20	800	ns
Driver Rise or Fall Time	t_R, t_F	Figures 10 and 12, R_{DIFF} = 54Ω, C_{L1} = C_{L2} = 100pF	250		2000	ns
Driver Enable to Output High	t_{ZH}	Figures 11 and 13, C_L = 100pF, S2 closed	250		2000	ns
Driver Enable to Output Low	t_{ZL}	Figures 11 and 13, C_L = 100pF, S1 closed	250		2000	ns
Driver Disable Time from Low	t_{LZ}	Figures 11 and 13, C_L = 15pF, S1 closed	300		3000	ns
Driver Disable Time from High	t_{HZ}	Figures 11 and 13, C_L = 15pF, S2 closed	300		3000	ns
Receiver Input to Output	t_{PLH}	Figures 10 and 14, R_{DIFF} = 54Ω, C_{L1} = C_{L2} = 100pF	250		2000	ns
	t_{PHL}		250		2000	
$\lvert t_{PLH} - t_{PHL} \rvert$ Differential Receiver Skew	t_{SKD}	Figures 10 and 14, R_{DIFF} = 54Ω, C_{L1} = C_{L2} = 100pF		100		ns
Receiver Enable to Output Low	t_{ZL}	Figures 9 and 15, C_{RL} = 15pF, S1 closed		25	50	ns
Receiver Enable to Output High	t_{ZH}	Figures 9 and 15, C_{RL} = 15pF, S2 closed		25	50	ns
Receiver Disable Time from Low	t_{LZ}	Figures 9 and 15, C_{RL} = 15pF, S1 closed		25	50	ns
Receiver Disable Time from High	t_{HZ}	Figures 9 and 15, C_{RL} = 15pF, S2 closed		25	50	ns
Maximum Data Rate	f_{MAX}	t_{PLH}, t_{PHL} < 50% of data period	250			kbps
Time to Shutdown	t_{SHDN}	MAX483E/MAX487E (Note 5)	50	200	600	ns
Driver Enable from Shutdown to Output High	$t_{ZH(SHDN)}$	MAX483E/MAX487E, Figures 11 and 13, C_L = 100pF, S2 closed			2000	ns
Driver Enable from Shutdown to Output Low	$t_{ZL(SHDN)}$	MAX483E/MAX487E, Figures 11 and 13, C_L = 100pF, S1 closed			2000	ns
Receiver Enable from Shutdown to Output High	$t_{ZH(SHDN)}$	MAX483E/MAX487E, Figures 9 and 15, C_L = 15pF, S2 closed			2500	ns
Receiver Enable from Shutdown to Output Low	$t_{ZL(SHDN)}$	MAX483E/MAX487E, Figures 9 and 15, C_L = 15pF, S1 closed			2500	ns



NOTES FOR ELECTRICAL/SWITCHING CHARACTERISTICS

Note 1: All currents into device pins are positive; all currents out of device pins are negative. All voltages are referenced to device ground unless otherwise specified.

Note 2: All typical specifications are given for V_{CC} = 5V and T_A = +25°C.

Note 3: Supply current specification is valid for loaded transmitters when DE = 0V.

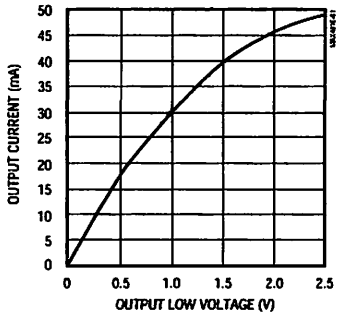
Note 4: Applies to peak current. See *Typical Operating Characteristics*.

Note 5: The MAX481E/MAX483E/MAX487E are put into shutdown by bringing $\overline{RE}$ high and DE low. If the inputs are in this state for less than 50ns, the parts are guaranteed not to enter shutdown. If the inputs are in this state for at least 600ns, the parts are guaranteed to have entered shutdown. See *Low-Power Shutdown Mode* section.

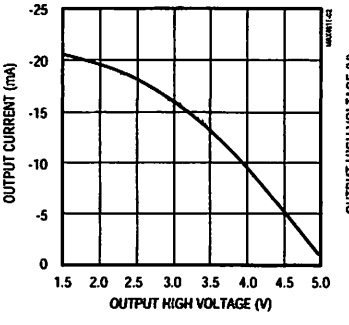
Typical Operating Characteristics

(V_{CC} = 5V, T_A = +25°C, unless otherwise noted.)

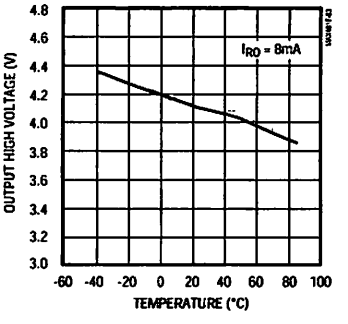
OUTPUT CURRENT vs. RECEIVER OUTPUT LOW VOLTAGE



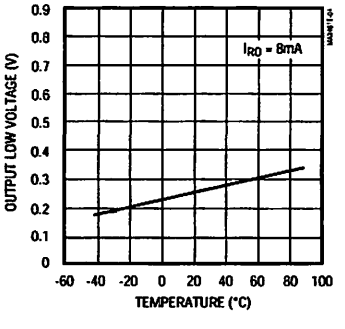
OUTPUT CURRENT vs. RECEIVER OUTPUT HIGH VOLTAGE



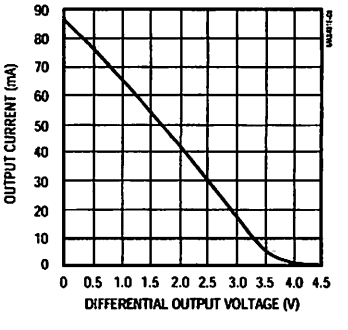
RECEIVER OUTPUT HIGH VOLTAGE vs. TEMPERATURE

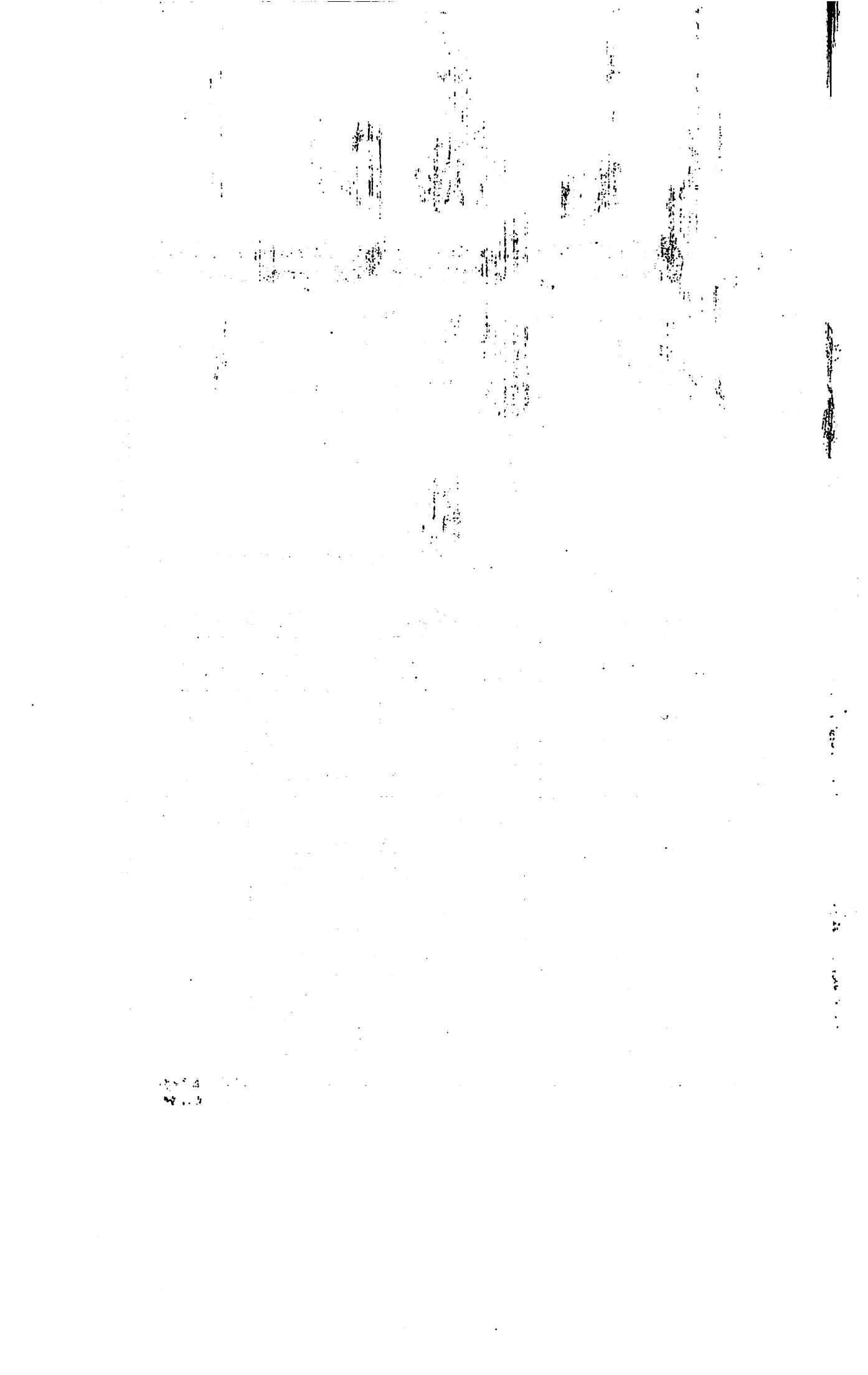


RECEIVER OUTPUT LOW VOLTAGE vs. TEMPERATURE



DRIVER OUTPUT CURRENT vs. DIFFERENTIAL OUTPUT VOLTAGE



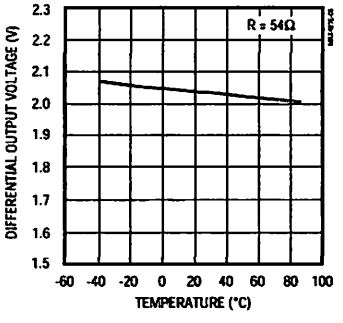


±15kV ESD-Protected, Slew-Rate-Limited, Low-Power, RS-485/RS-422 Transceivers

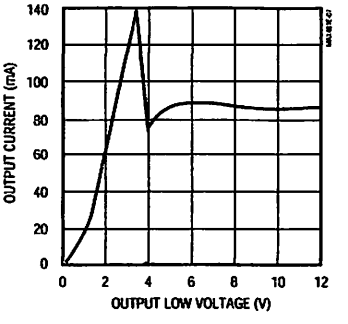
Typical Operating Characteristics (continued)

(V_{CC} = 5V, T_A = +25°C, unless otherwise noted.)

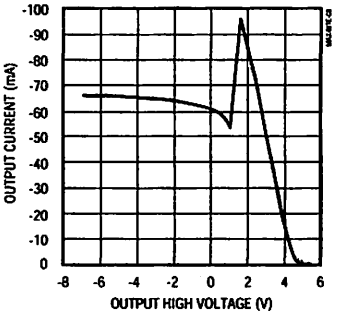
DRIVER DIFFERENTIAL OUTPUT VOLTAGE vs. TEMPERATURE



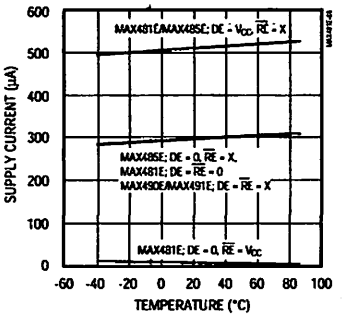
OUTPUT CURRENT vs. DRIVER OUTPUT LOW VOLTAGE



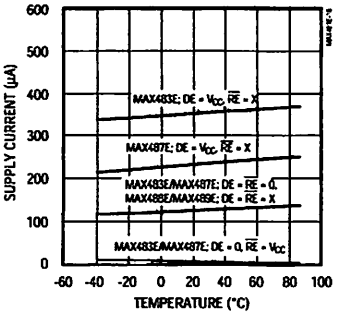
OUTPUT CURRENT vs. DRIVER OUTPUT HIGH VOLTAGE



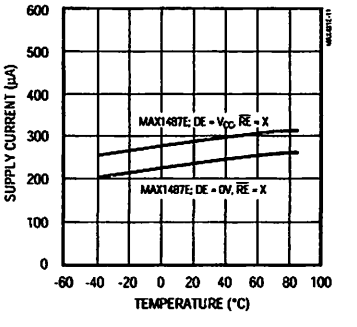
MAX481E/MAX485E/MAX490E/MAX491E SUPPLY CURRENT vs. TEMPERATURE

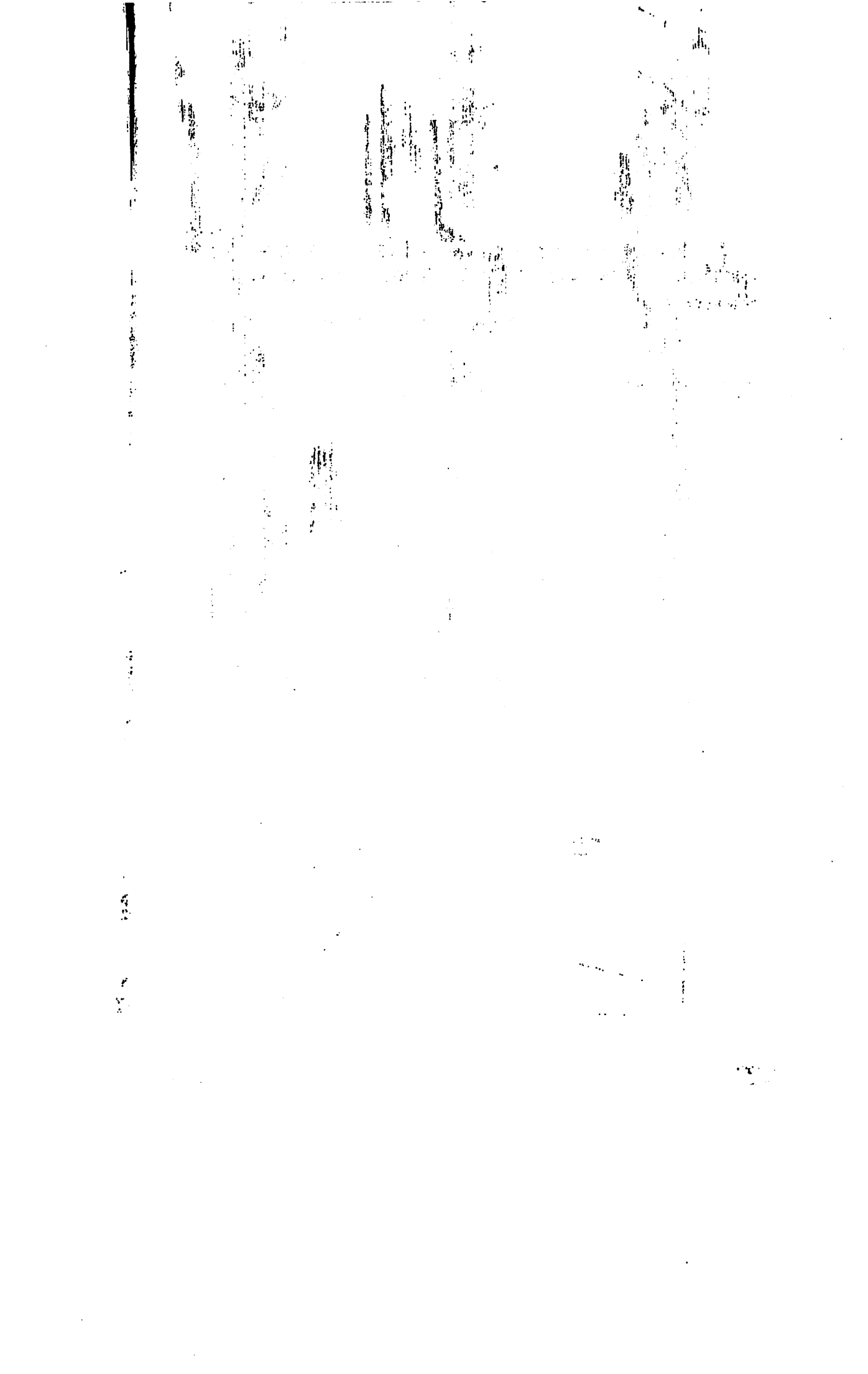


MAX483E/MAX487E–MAX489E SUPPLY CURRENT vs. TEMPERATURE



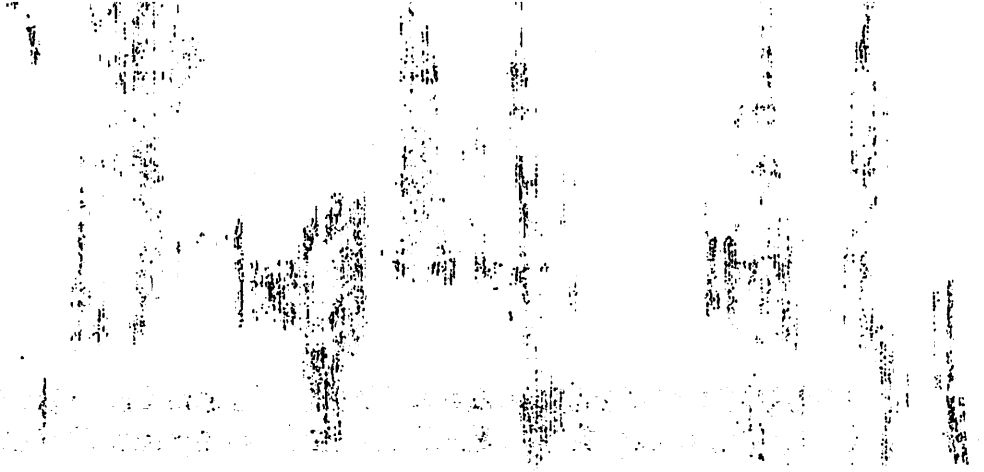
MAX1487E SUPPLY CURRENT vs. TEMPERATURE





Pin Description

PIN			NAME	FUNCTION
MAX481E/MAX483E MAX485E/MAX487E MAX1487E	MAX488E MAX490E	MAX489E MAX491E		
1	2	2	RO	Receiver Output: If A > B by 200mV, RO will be high; If A < B by 200mV, RO will be low.
2	—	3	$\overline{RE}$	Receiver Output Enable. RO is enabled when $\overline{RE}$ is low; RO is high impedance when $\overline{RE}$ is high.
3	—	4	DE	Driver Output Enable. The driver outputs, Y and Z, are enabled by bringing DE high. They are high impedance when DE is low. If the driver outputs are enabled, the parts function as line drivers. While they are high impedance, they function as line receivers if $\overline{RE}$ is low.
4	3	5	DI	Driver Input. A low on DI forces output Y low and output Z high. Similarly, a high on DI forces output Y high and output Z low.
5	4	6, 7	GND	Ground
—	5	9	Y	Noninverting Driver Output
—	6	10	Z	Inverting Driver Output
6	—	—	A	Noninverting Receiver Input and Noninverting Driver Output
—	8	12	A	Noninverting Receiver Input
7	—	—	B	Inverting Receiver Input and Inverting Driver Output
—	7	11	B	Inverting Receiver Input
8	1	14	V_{CC}	Positive Supply: $4.75V \le V_{CC} \le 5.25V$
—	—	1, 8, 13	N.C.	No Connect—not internally connected



±15kV ESD-Protected, Slew-Rate-Limited, Low-Power, RS-485/RS-422 Transceivers

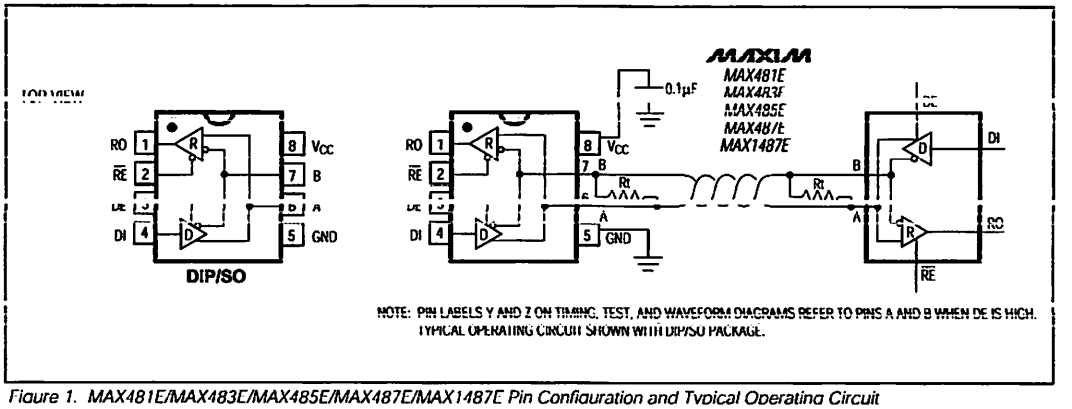


Figure 1. MAX481E/MAX483E/MAX485E/MAX487E/MAX1487E Pin Configuration and Typical Operating Circuit

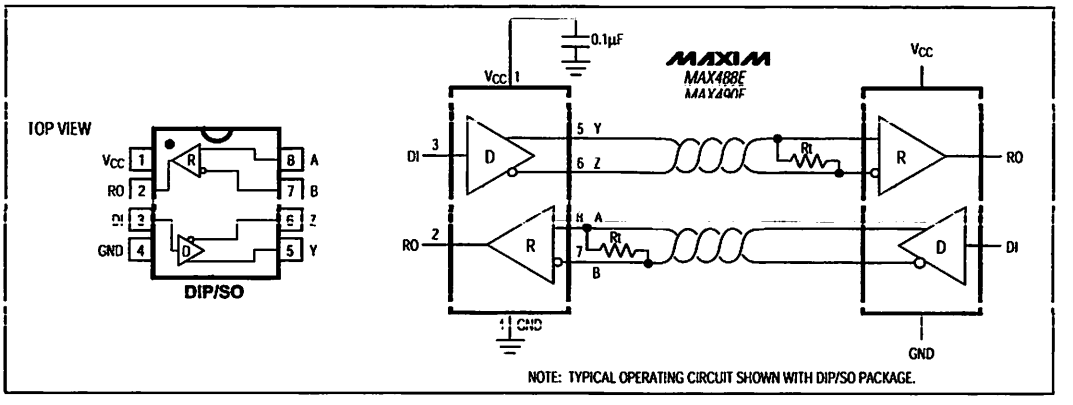


Figure 2. MAX488E/MAX490E Pin Configuration and Typical Operating Circuit

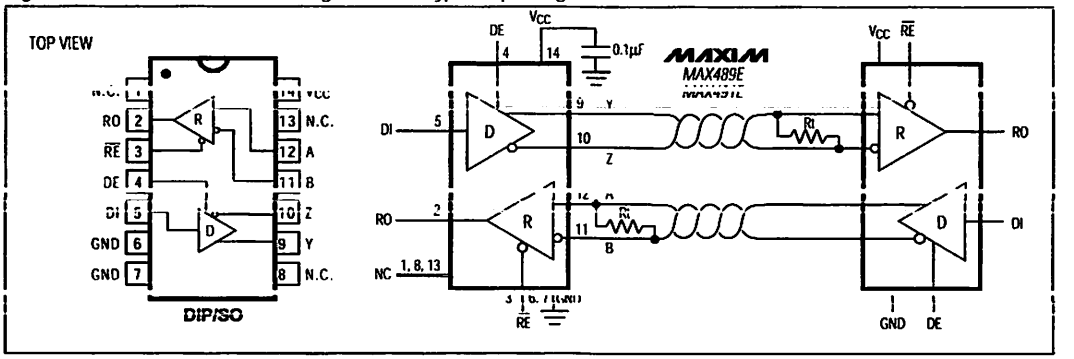


Figure 3. MAX489E/MAX491E Pin Configuration and Typical Operating Circuit

Function Tables (MAX481E/MAX483E/MAX485E/MAX487E/MAX1487E)

Table 1. Transmitting

INPUTS			OUTPUTS	
$\overline{RE}$	DE	DI	Z	Y
X	1	1	0	1
X	1	0	1	0
0	0	X	High-Z	High-Z
1	0	X	High-Z*	High-Z*

X = Don't care
High-Z = High impedance
* Shutdown mode for MAX481E/MAX483E/MAX487E

Table 2. Receiving

INPUTS			OUTPUT
$\overline{RE}$	DE	A-B	RO
0	0	≥ +0.2V	1
0	0	≤ -0.2V	0
0	0	Inputs open	1
1	0	X	High-Z*

X = Don't care
High-Z = High impedance
* Shutdown mode for MAX481E/MAX483E/MAX487E

Applications Information

The MAX481E/MAX483E/MAX485E/MAX487E–MAX491E and MAX1487E are low-power transceivers for RS-485 and RS-422 communications. These "E" versions of the MAX481, MAX483, MAX485, MAX487–MAX491, and MAX1487 provide extra protection against ESD. The rugged MAX481E, MAX483E, MAX485E, MAX487E–MAX491E, and MAX1487E are intended for harsh environments where high-speed communication is important. These devices eliminate the need for transient suppressor diodes and the associated high capacitance loading. The standard (non-"E") MAX481, MAX483, MAX485, MAX487–MAX491, and MAX1487 are recommended for applications where cost is critical.

The MAX481E, MAX485E, MAX490E, MAX491E, and MAX1487E can transmit and receive at data rates up to 2.5Mbps, while the MAX483E, MAX487E, MAX488E, and MAX489E are specified for data rates up to 250kbps. The MAX488E–MAX491E are full-duplex transceivers, while the MAX481E, MAX485E, MAX487E, and MAX1487E are half-duplex. In addition, driver-enable (DE) and receiver-enable (RE) pins are included on the MAX481E, MAX483E, MAX485E, MAX487E, MAX489E, MAX491E, and MAX1487E. When disabled, the driver and receiver outputs are high impedance.

±15kV ESD Protection

As with all Maxim devices, ESD-protection structures are incorporated on all pins to protect against electrostatic discharges encountered during handling and assembly. The driver outputs and receiver inputs have extra protection against static electricity. Maxim's engineers developed state-of-the-art structures to protect these pins against ESD of ±15kV without damage. The ESD structures withstand high ESD in all states: normal operation, shutdown, and powered down. After an ESD event, Maxim's MAX481E, MAX483E, MAX485E, MAX487E–MAX491E, and MAX1487E keep working without latchup.

ESD protection can be tested in various ways; the transmitter outputs and receiver inputs of this product family are characterized for protection to ±15kV using the Human Body Model.

Other ESD test methodologies include IEC10004-2 contact discharge and IEC1000-4-2 air-gap discharge (formerly IEC801-2).

ESD Test Conditions

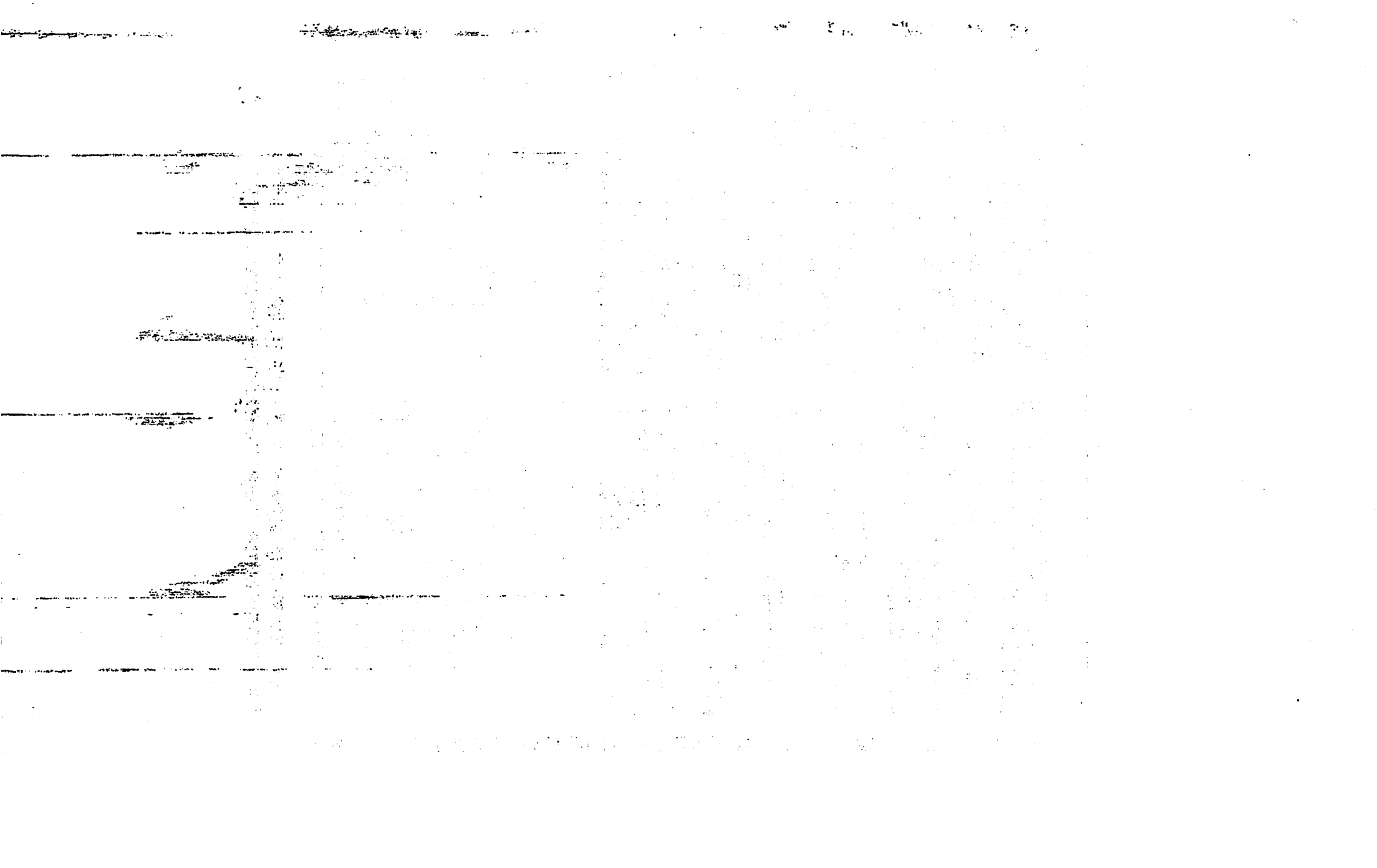
ESD performance depends on a variety of conditions. Contact Maxim for a reliability report that documents test set-up, test methodology, and test results.

Human Body Model

Figure 4 shows the Human Body Model, and Figure 5 shows the current waveform it generates when discharged into a low impedance. This model consists of a 100pF capacitor charged to the ESD voltage of interest, which is then discharged into the test device through a 1.5kΩ resistor.

IEC1000-4-2

The IEC1000-4-2 standard covers ESD testing and performance of finished equipment; it does not specifically refer to integrated circuits (Figure 6).



±15kV ESD-Protected, Slew-Rate-Limited, Low-Power, RS-485/RS-422 Transceivers

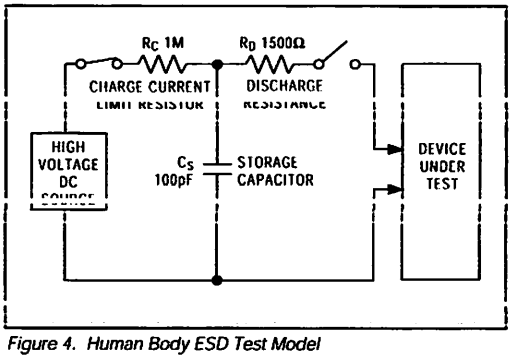


Figure 4. Human Body ESD Test Model

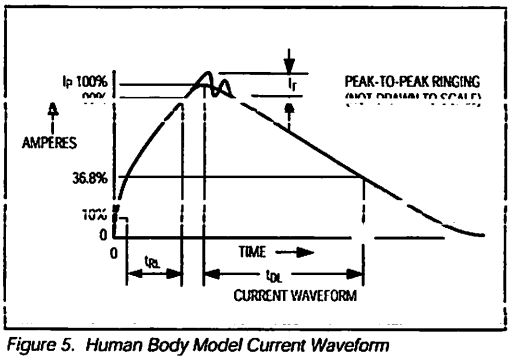


Figure 5. Human Body Model Current Waveform

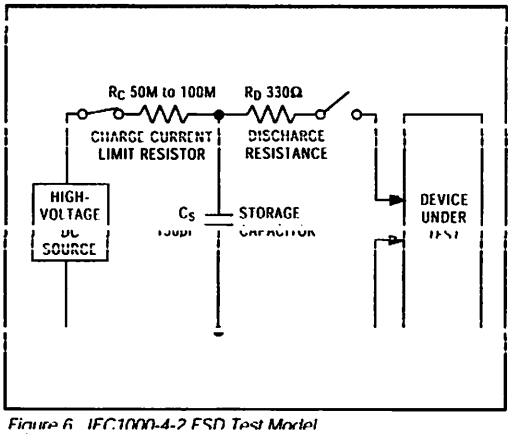


Figure 6. IEC1000-4-2 ESD Test Model

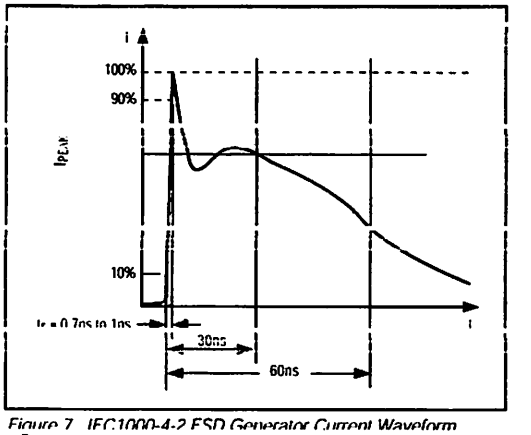


Figure 7. IEC1000-4-2 ESD Generator Current Waveform

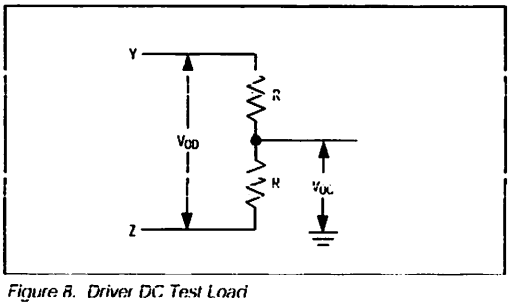


Figure 8. Driver DC Test Load

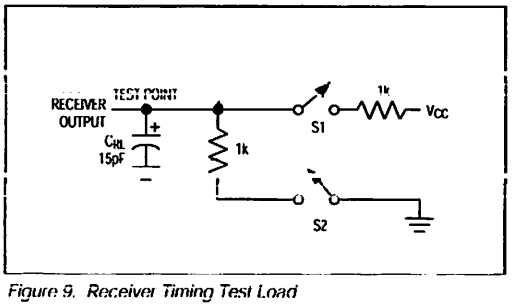
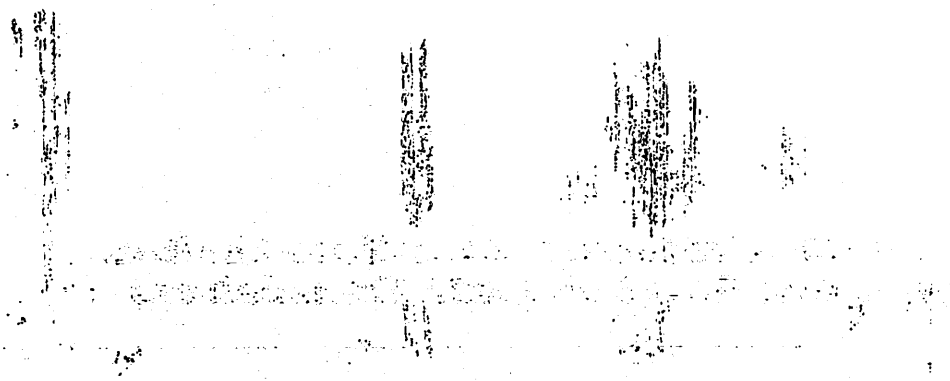


Figure 9. Receiver Timing Test Load



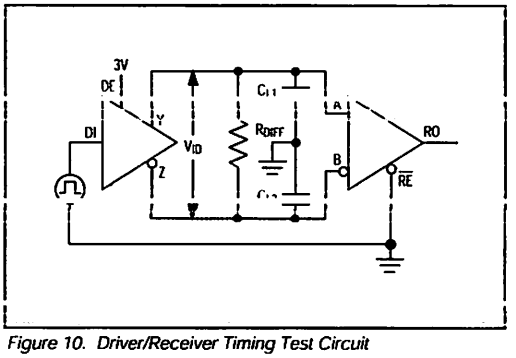


Figure 10. Driver/Receiver Timing Test Circuit

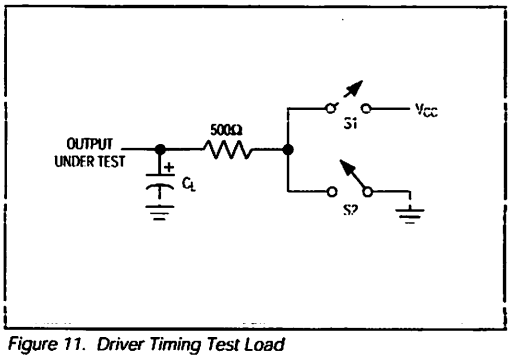


Figure 11. Driver Timing Test Load

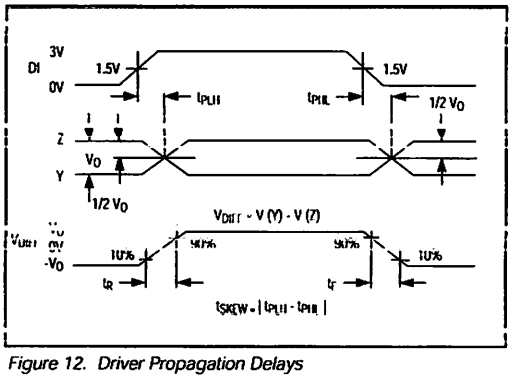


Figure 12. Driver Propagation Delays

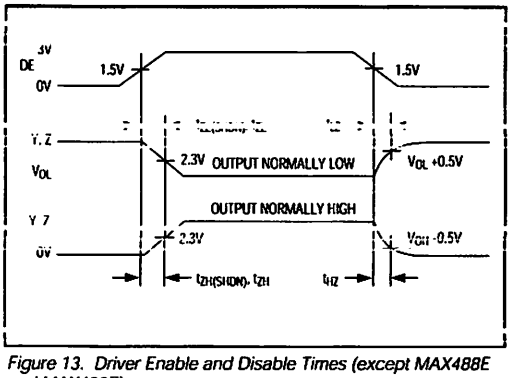


Figure 13. Driver Enable and Disable Times (except MAX488E and MAX490E)

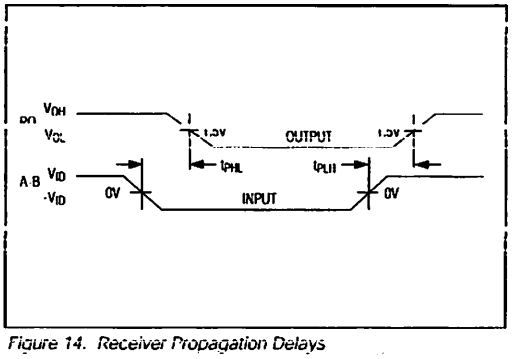


Figure 14. Receiver Propagation Delays

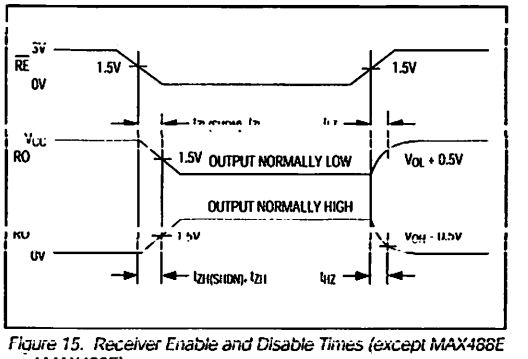


Figure 15. Receiver Enable and Disable Times (except MAX488E and MAX490E)

±15kV ESD-Protected, Slew-Rate-Limited, Low-Power, RS-485/RS-422 Transceivers

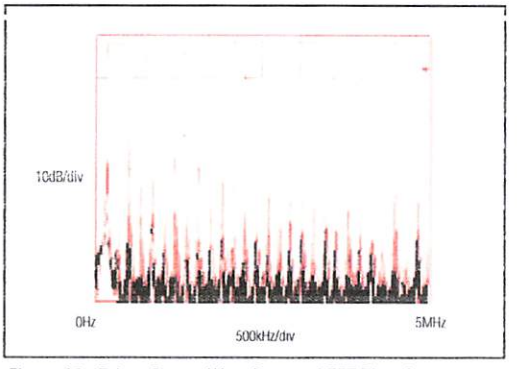


Figure 16. Driver Output Waveform and FFT Plot of MAX485E/MAX490E/MAX491E/MAX1487E Transmitting a 150kHz Signal

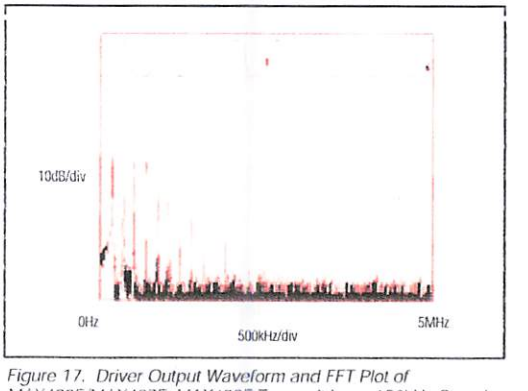


Figure 17. Driver Output Waveform and FFT Plot of MAX483E/MAX487E–MAX489E Transmitting a 150kHz Signal

The major difference between tests done using the Human Body Model and IEC1000-4-2 is higher peak current in IEC1000-4-2, because series resistance is lower in the IEC1000-4-2 model. Hence, the ESD withstand voltage measured to IEC1000-4-2 is generally lower than that measured using the Human Body Model. Figure 7 shows the current waveform for the 8kV IEC1000-4-2 ESD contact-discharge test.

The air-gap test involves approaching the device with a charged probe. The contact-discharge method connects the probe to the device before the probe is energized.

Machine Model

The Machine Model for ESD tests all pins using a 200pF storage capacitor and zero discharge resistance. Its objective is to emulate the stress caused by contact that occurs with handling and assembly during manufacturing. Of course, all pins require this protection during manufacturing—not just inputs and outputs. Therefore, after PC board assembly, the Machine Model is less relevant to I/O ports.

MAX487E/MAX1487E: 128 Transceivers on the Bus

The 48kΩ, 1/4-unit-load receiver input impedance of the MAX487E and MAX1487E allows up to 128 transceivers on a bus, compared to the 1-unit load (12kΩ input impedance) of standard RS-485 drivers (32 transceivers maximum). Any combination of MAX487E/MAX1487E and other RS-485 transceivers with a total of 32 unit loads or less can be put on the bus. The MAX481E, MAX483E, MAX485E, and MAX488E–MAX491E have standard 12kΩ receiver input impedance.

MAX483E/MAX487E/MAX488E/MAX489E: Reduced EMI and Reflections

The MAX483E and MAX487E–MAX489E are slew-rate limited, minimizing EMI and reducing reflections caused by improperly terminated cables. Figure 16 shows the driver output waveform and its Fourier analysis of a 150kHz signal transmitted by a MAX481E, MAX485E, MAX490E, MAX491E, or MAX1487E. High-frequency harmonics with large amplitudes are evident. Figure 17 shows the same information displayed for a MAX483E, MAX487E, MAX488E, or MAX489E transmitting under the same conditions. Figure 17's high-frequency harmonics have much lower amplitudes, and the potential for EMI is significantly reduced.

Low-Power Shutdown Mode (MAX481E/MAX483E/MAX487E)

A low-power shutdown mode is initiated by bringing both $\overline{RE}$ high and DE low. The devices will not shut down unless both the driver and receiver are disabled. In shutdown, the devices typically draw only 0.5µA of supply current.

$\overline{RE}$ and DE may be driven simultaneously; the parts are guaranteed not to enter shutdown if $\overline{RE}$ is high and DE is low for less than 50ns. If the inputs are in this state for at least 600ns, the parts are guaranteed to enter shutdown.

For the MAX481E, MAX483E, and MAX487E, the t_{ZH} and t_{ZL} enable times assume the part was not in the low power shutdown state (the MAX485E, MAX489E–MAX491E, and MAX1487E can not be shut down). The $t_{ZH(SHDN)}$ and $t_{ZL(SHDN)}$ enable times assume the parts were shut down (see *Electrical Characteristics*).

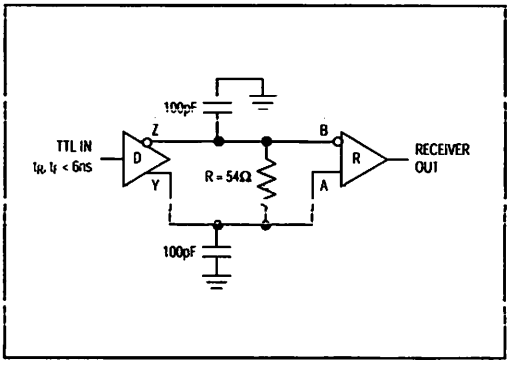


Figure 18. Receiver Propagation Delay Test Circuit

It takes the drivers and receivers longer to become enabled from the low-power shutdown state ($t_{ZH(SHDN)}$, $t_{ZL(SHDN)}$) than from the operating mode (t_{ZH}, t_{ZL}). (The parts are in operating mode if the $\overline{RE}$, DE inputs equal a logical 0,1 or 1,1 or 0, 0.)

Driver Output Protection

Excessive output current and power dissipation caused by faults or by bus contention are prevented by two mechanisms. A foldback current limit on the output stage provides immediate protection against short circuits over the whole common-mode voltage range (see *Typical Operating Characteristics*). In addition, a thermal shutdown circuit forces the driver outputs into a high impedance state if the die temperature rises excessively.

Propagation Delay

Many digital encoding schemes depend on the difference between the driver and receiver propagation delay times. Typical propagation delays are shown in Figures 19–22 using Figure 18's test circuit.

The difference in receiver delay times, t_{PLH} - t_{PHL}, is typically under 13ns for the MAX481E, MAX485E, MAX490E, MAX491E, and MAX1487E, and is typically less than 100ns for the MAX483E and MAX487E–MAX489E.

The driver skew times are typically 5ns (10ns max) for the MAX481E, MAX485E, MAX490E, MAX491E, and MAX1487E, and are typically 100ns (800ns max) for the MAX483E and MAX487E–MAX489E.

Typical Applications

The MAX481E, MAX483E, MAX485E, MAX487E–MAX491E, and MAX1487E transceivers are designed for bidirectional data communications on multipoint bus transmission lines. Figures 25 and 26 show typical network application circuits. These parts can also be used as line repeaters, with cable lengths longer than 4000 feet.

To minimize reflections, the line should be terminated at both ends in its characteristic impedance, and stub lengths off the main line should be kept as short as possible. The slew-rate-limited MAX483E and MAX487E–MAX489E are more tolerant of imperfect termination. Bypass the V_{CC} pin with 0.1µF.

Isolated RS-485

For isolated RS-485 applications, see the MAX253 and MAX1480 data sheets.

Line Length vs. Data Rate

The RS-485/RS-422 standard covers line lengths up to 4000 feet. Figures 23 and 24 show the system differential voltage for the parts driving 4000 feet of 26AWG twisted-pair wire at 110kHz into 100Ω loads.

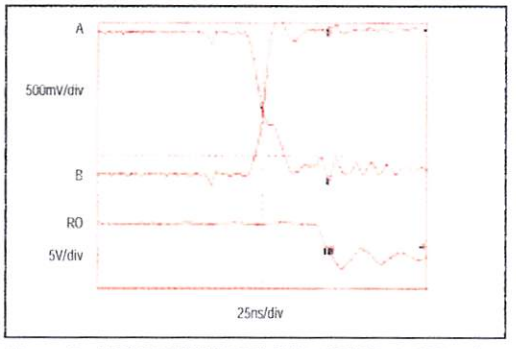


Figure 19. MAX481E/MAX485E/MAX490E/MAX1487E Receiver t_{PHL}

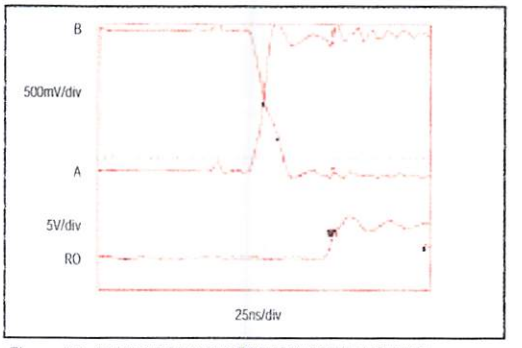


Figure 20. MAX481E/MAX485E/MAX490E/MAX491E/MAX1487E Receiver t_{PLH}

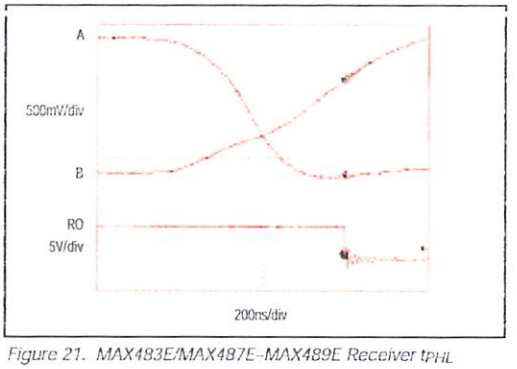


Figure 21. MAX483E/MAX487E–MAX489E Receiver t_{PHL}

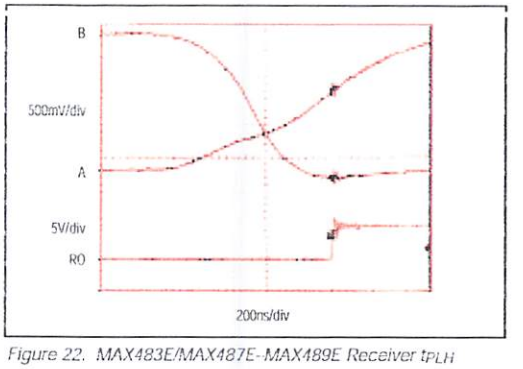


Figure 22. MAX483E/MAX487E–MAX489E Receiver t_{PLH}

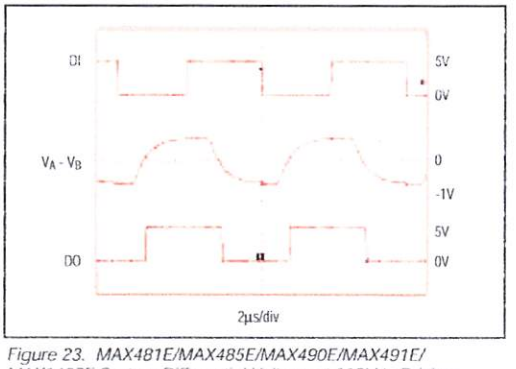


Figure 23. MAX481E/MAX485E/MAX490E/MAX491E/MAX1487E System Differential Voltage at 110kHz Driving 4000ft of Cable

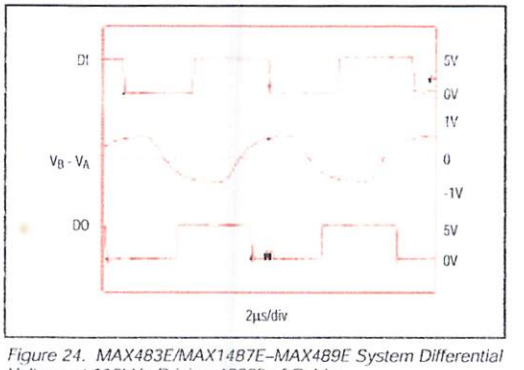


Figure 24. MAX483E/MAX1487E–MAX489E System Differential Voltage at 110kHz Driving 4000ft of Cable

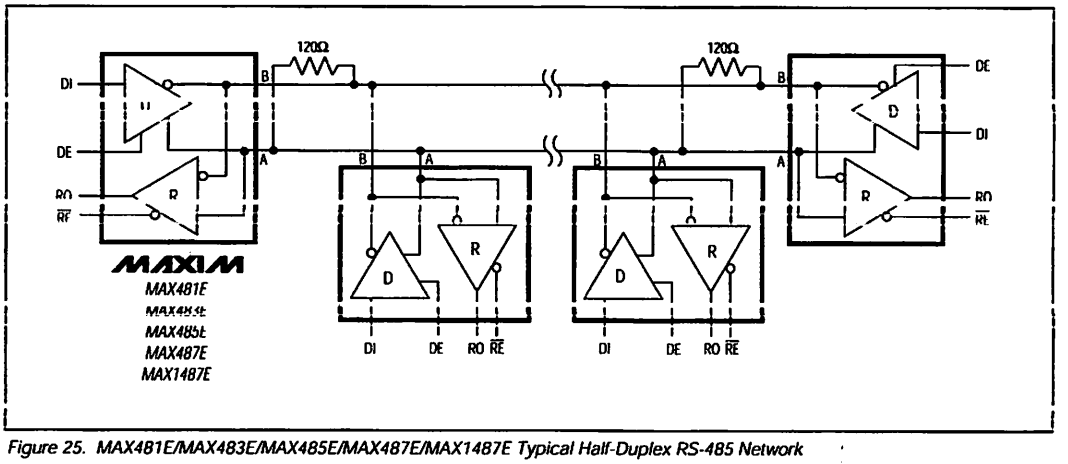


Figure 25. MAX481E/MAX483E/MAX485E/MAX487E/MAX1487E Typical Half-Duplex RS-485 Network

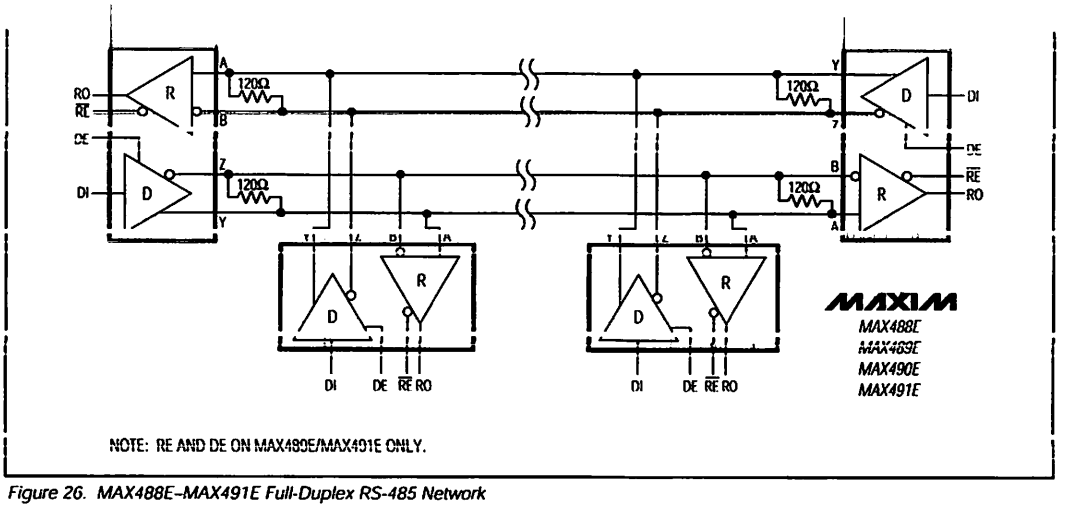


Figure 26. MAX488E–MAX491E Full-Duplex RS-485 Network

±15kV ESD-Protected, Slew-Rate-Limited, Low-Power, RS-485/RS-422 Transceivers

Ordering Information (continued)

PART	TEMP. RANGE	PIN-PACKAGE
MAX483ECPA	0°C to +70°C	8 Plastic DIP
MAX483ECSA	0°C to +70°C	8 SO
MAX483EEPA	-40°C to +85°C	8 Plastic DIP
MAX483EESA	-40°C to +85°C	8 SO
MAX485ECPA	0°C to +70°C	8 Plastic DIP
MAX485ECSA	0°C to +70°C	8 SO
MAX485EEPA	-40°C to +85°C	8 Plastic DIP
MAX485EESA	-40°C to +85°C	8 SO
MAX487ECPA	0°C to +70°C	8 Plastic DIP
MAX487ECSA	0°C to +70°C	8 SO
MAX487EEPA	-40°C to +85°C	8 Plastic DIP
MAX487EESA	-40°C to +85°C	8 SO
MAX488ECPA	0°C to +70°C	8 Plastic DIP
MAX488ECSA	0°C to +70°C	8 SO
MAX488EEPA	-40°C to +85°C	8 Plastic DIP
MAX488EESA	-40°C to +85°C	8 SO

PART	TEMP. RANGE	PIN-PACKAGE
MAX489ECPD	0°C to +70°C	14 Plastic DIP
MAX489ECSD	0°C to +70°C	14 SO
MAX489EEPD	-40°C to +85°C	14 Plastic DIP
MAX489EESD	-40°C to +85°C	14 SO
MAX490ECPA	0°C to +70°C	8 Plastic DIP
MAX490ECSA	0°C to +70°C	8 SO
MAX490EEPA	-40°C to +85°C	8 Plastic DIP
MAX490EESA	-40°C to +85°C	8 SO
MAX491ECPD	0°C to +70°C	14 Plastic DIP
MAX491ECSD	0°C to +70°C	14 SO
MAX491EEPD	-40°C to +85°C	14 Plastic DIP
MAX491EESD	-40°C to +85°C	14 SO
MAX1487ECPA	0°C to +70°C	8 Plastic DIP
MAX1487ECSA	0°C to +70°C	8 SO
MAX1487EEPA	-40°C to +85°C	8 Plastic DIP
MAX1487EESA	-40°C to +85°C	8 SO

Chip Information

TRANSISTOR COUNT: 295

National Semiconductor

August 2000

LM386
Low Voltage Audio Power Amplifier

General Description

The LM386 is a power amplifier designed for use in low voltage consumer applications. The gain is internally set to 20 to keep external part count low, but the addition of an external resistor and capacitor between pins 1 and 8 will increase the gain to any value from 20 to 200.

The inputs are ground referenced while the output automatically biases to one-half the supply voltage. The quiescent power drain is only 24 milliwatts when operating from a 6 volt supply, making the LM386 ideal for battery operation.

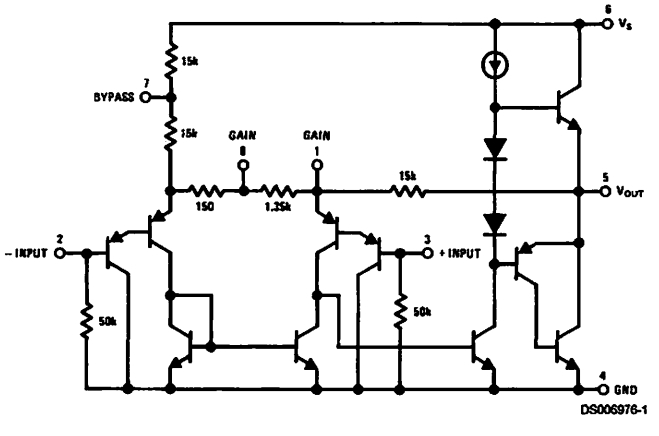
Features

- Battery operation
- Minimum external parts
- Wide supply voltage range: 4V–12V or 5V–18V
- Low quiescent current drain: 4mA
- Voltage gains from 20 to 200
- Ground referenced input
- Self-centering output quiescent voltage
- Low distortion: 0.2% (A_V = 20, V_S = 6V, R_L = 8Ω, P_O = 125mW, f = 1kHz)
- Available in 8 pin MSOP package

Applications

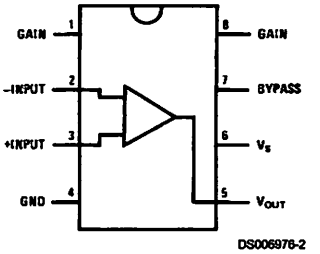
- AM-FM radio amplifiers
- Portable tape player amplifiers
- Intercoms
- TV sound systems
- Line drivers
- Ultrasonic drivers
- Small servo drivers
- Power converters

Equivalent Schematic and Connection Diagrams



DS006976-1

Small Outline, Molded Mini Small Outline, and Dual-In-Line Packages



DS006976-2

Top View
Order Number LM386M-1, LM386MM-1, LM386N-1, LM386N-3 or LM386N-4
See NS Package Number M08A, MUA08A or N08E

Absolute Maximum Ratings (Note 2)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Supply Voltage	
(LM386N-1, -3, LM386M-1)	15V
Supply Voltage (LM386N-4)	22V
Package Dissipation (Note 3)	
(LM386N)	1.25W
(LM386M)	0.73W
(LM386MM-1)	0.595W
Input Voltage	±0.4V
Storage Temperature	−65°C to +150°C
Operating Temperature	0°C to +70°C
Junction Temperature	+150°C
Soldering Information	
Dual-In-Line Package	
Soldering (10 sec)	+260°C
Small Outline Package	
(SOIC and MSOP)	
Vapor Phase (60 sec)	+215°C
Infrared (15 sec)	+220°C

See AN-450 "Surface Mounting Methods and Their Effect on Product Reliability" for other methods of soldering surface mount devices.

Thermal Resistance	
θ_{JC} (DIP)	37°C/W
θ_{JA} (DIP)	107°C/W
θ_{JC} (SO Package)	35°C/W
θ_{JA} (SO Package)	172°C/W
θ_{JA} (MSOP)	210°C/W
θ_{JC} (MSOP)	56°C/W

Electrical Characteristics (Notes 1, 2)

T_A = 25°C

Parameter	Conditions	Min	Typ	Max	Units
Operating Supply Voltage (V_S)					
LM386N-1, -3, LM386M-1, LM386MM-1		4		12	V
LM386N-4		5		18	V
Quiescent Current (I_Q)	V_S = 6V, V_{IN} = 0		4	8	mA
Output Power (P_{OUT})					
LM386N-1, LM386M-1, LM386MM-1	V_S = 6V, R_L = 8Ω, THD = 10%	250	325		mW
LM386N-3	V_S = 9V, R_L = 8Ω, THD = 10%	500	700		mW
LM386N-4	V_S = 16V, R_L = 32Ω, THD = 10%	700	1000		mW
Voltage Gain (A_V)	V_S = 6V, f = 1 kHz		26		dB
	10 µF from Pin 1 to 8		46		dB
Bandwidth (BW)	V_S = 6V, Pins 1 and 8 Open		300		kHz
Total Harmonic Distortion (THD)	V_S = 6V, R_L = 8Ω, P_{OUT} = 125 mW		0.2		%
	f = 1 kHz, Pins 1 and 8 Open				
Power Supply Rejection Ratio (PSRR)	V_S = 6V, f = 1 kHz, C_{BYPASS} = 10 µF		50		dB
	Pins 1 and 8 Open, Referred to Output				
Input Resistance (R_{IN})			50		kΩ
Input Bias Current (I_{BIAS})	V_S = 6V, Pins 2 and 3 Open		250		nA

Note 1: All voltages are measured with respect to the ground pin, unless otherwise specified.

Note 2: Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is functional, but do not guarantee specific performance limits. Electrical Characteristics state DC and AC electrical specifications under particular test conditions which guarantee specific performance limits. This assumes that the device is within the Operating Ratings. Specifications are not guaranteed for parameters where no limit is given, however, the typical value is a good indication of device performance.

Note 3: For operation in ambient temperatures above 25°C, the device must be derated based on a 150°C maximum junction temperature and 1) a thermal resistance of 107°C/W junction to ambient for the dual-in-line package and 2) a thermal resistance of 170°C/W for the small outline package.

ıpplication Hints

AIN CONTROL

› make the LM386 a more versatile amplifier, two pins (1 ıd 8) are provided for gain control. With pins 1 and 8 open e 1.35 kΩ resistor sets the gain at 20 (26 dB). If a capacitor put from pin 1 to 8, bypassing the 1.35 kΩ resistor, the ıin will go up to 200 (46 dB). If a resistor is placed in series th the capacitor, the gain can be set to any value from 20 200. Gain control can also be done by capacitively cou- ing a resistor (or FET) from pin 1 to ground.

ıditional external components can be placed in parallel th the internal feedback resistors to tailor the gain and fre- ıency response for individual applications. For example, ə can compensate poor speaker bass response by fre- ıency shaping the feedback path. This is done with a series C from pin 1 to 5 (paralleling the internal 15 kΩ resistor). ›r 6 dB effective bass boost: R ≃ 15 kΩ, the lowest value r good stable operation is R = 10 kΩ if pin 8 is open. If pins and 8 are bypassed then R as low as 2 kΩ can be used. ıis restriction is because the amplifier is only compensated r closed-loop gains greater than 9.

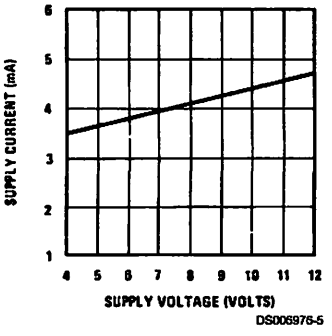
INPUT BIASING

The schematic shows that both inputs are biased to ground with a 50 kΩ resistor. The base current of the input transistors is about 250 nA, so the inputs are at about 12.5 mV when left open. If the dc source resistance driving the LM386 is higher than 250 kΩ it will contribute very little additional offset (about 2.5 mV at the input, 50 mV at the output). If the dc source resistance is less than 10 kΩ, then shorting the unused input to ground will keep the offset low (about 2.5 mV at the input, 50 mV at the output). For dc source resistances between these values we can eliminate excess offset by putting a resistor from the unused input to ground, equal in value to the dc source resistance. Of course all offset problems are eliminated if the input is capacitively coupled.

When using the LM386 with higher gains (bypassing the 1.35 kΩ resistor between pins 1 and 8) it is necessary to bypass the unused input, preventing degradation of gain and possible instabilities. This is done with a 0.1 µF capacitor or a short to ground depending on the dc source resistance on the driven input.

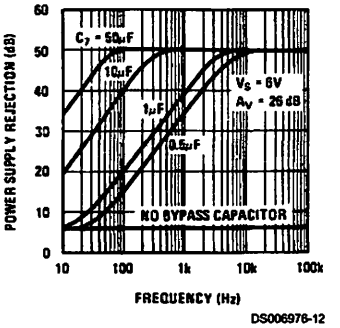
Typical Performance Characteristics

Quiescent Supply Current vs Supply Voltage



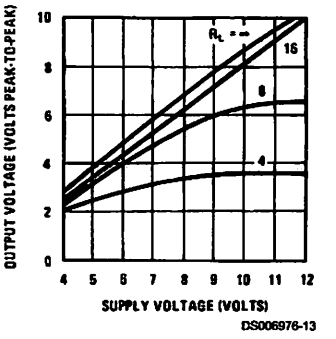
DS006976-5

Power Supply Rejection Ratio (Referred to the Output) vs Frequency



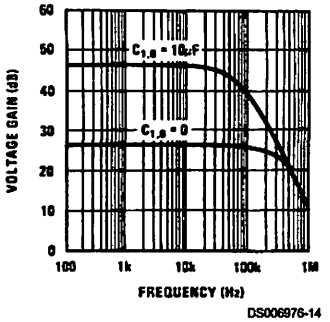
DS006976-12

Peak-to-Peak Output Voltage Swing vs Supply Voltage



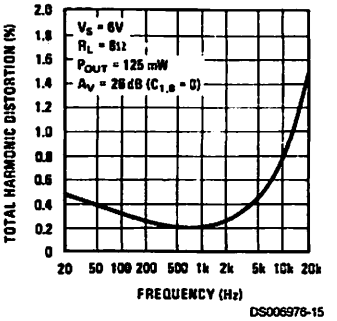
DS006976-13

Voltage Gain vs Frequency



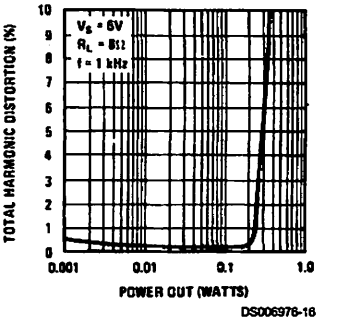
DS006976-14

Distortion vs Frequency



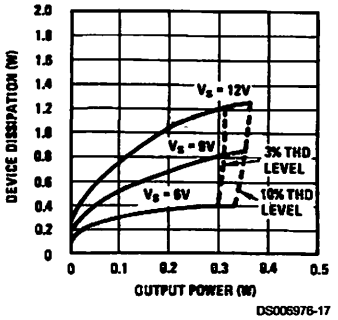
DS006976-15

Distortion vs Output Power



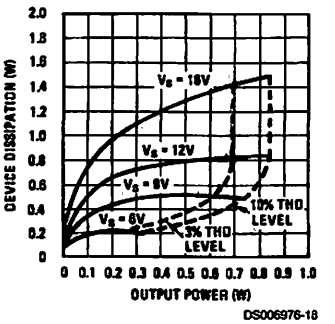
DS006976-16

Device Dissipation vs Output Power—4Ω Load



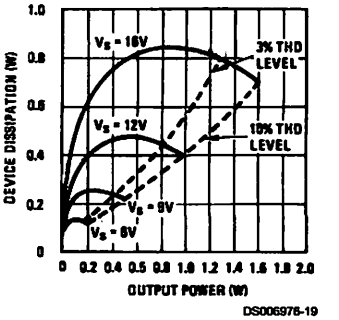
DS006976-17

Device Dissipation vs Output Power—8Ω Load



DS006976-18

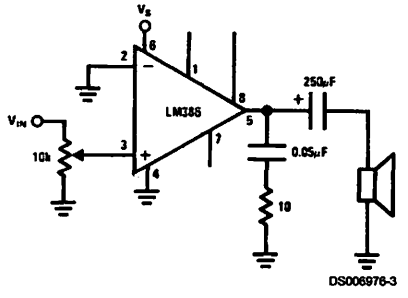
Device Dissipation vs Output Power—16Ω Load



DS006976-19

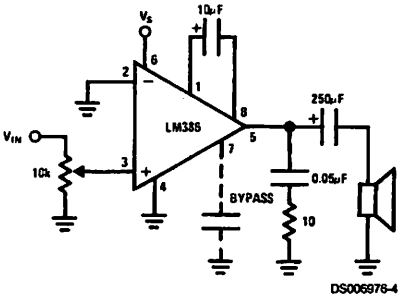
Typical Applications

Amplifier with Gain = 20 Minimum Parts



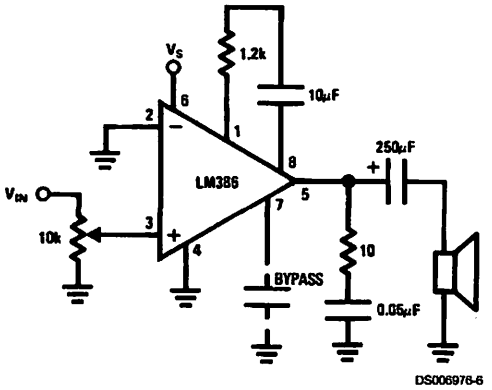
DS006976-3

Amplifier with Gain = 200



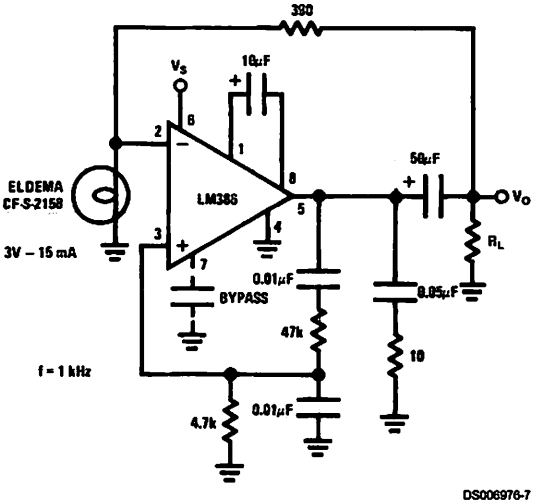
DS006976-4

Amplifier with Gain = 50



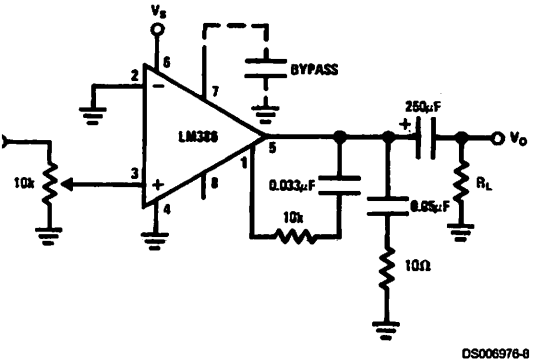
DS006976-6

Low Distortion Power Wienbridge Oscillator



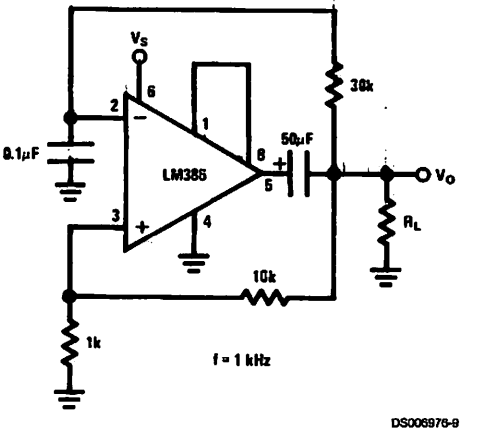
DS006976-7

Amplifier with Bass Boost



DS006976-8

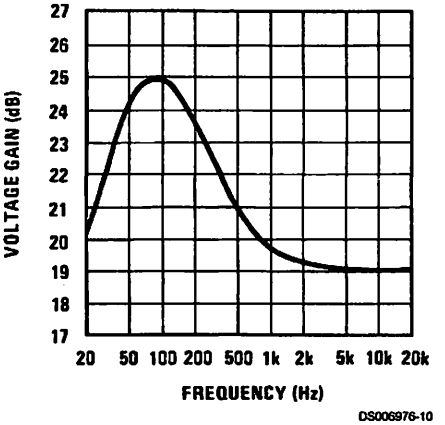
Square Wave Oscillator



DS006976-9

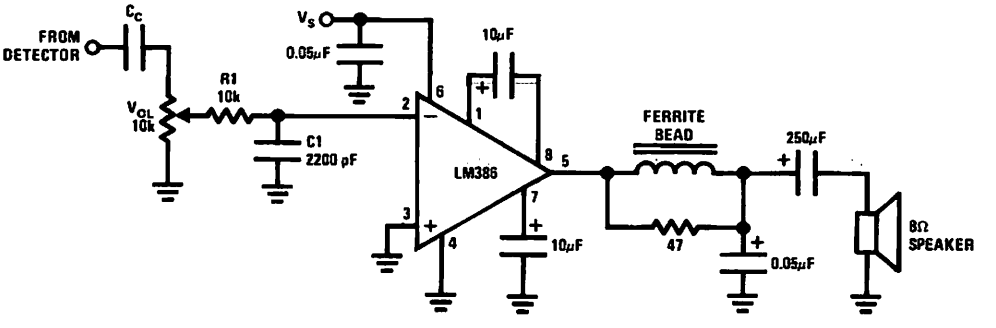
Typical Applications (Continued)

Frequency Response with Bass Boost



DS006976-10

AM Radio Power Amplifier



DS006976-11

Note 4: Twist Supply lead and supply ground very tightly.

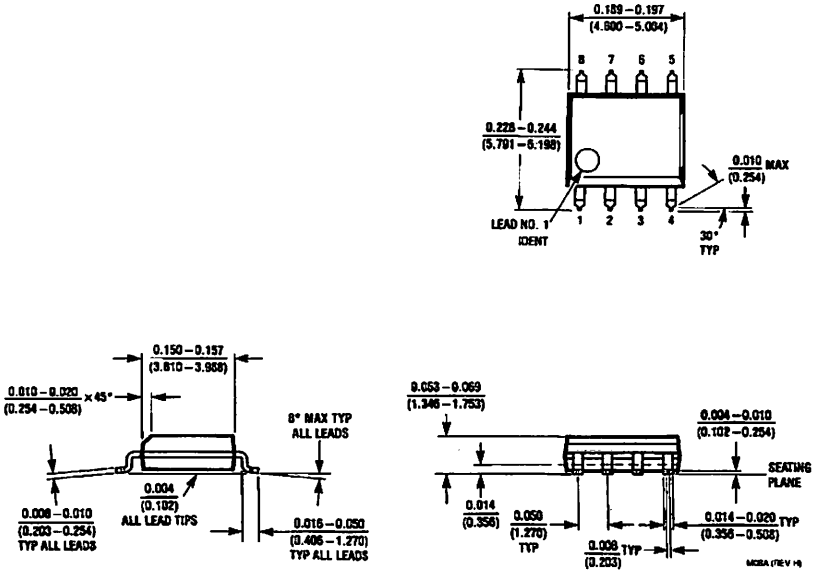
Note 5: Twist speaker lead and ground very tightly.

Note 6: Ferrite bead in Ferroxcube K5-001-001/3B with 3 turns of wire.

Note 7: R1C1 band limits input signals.

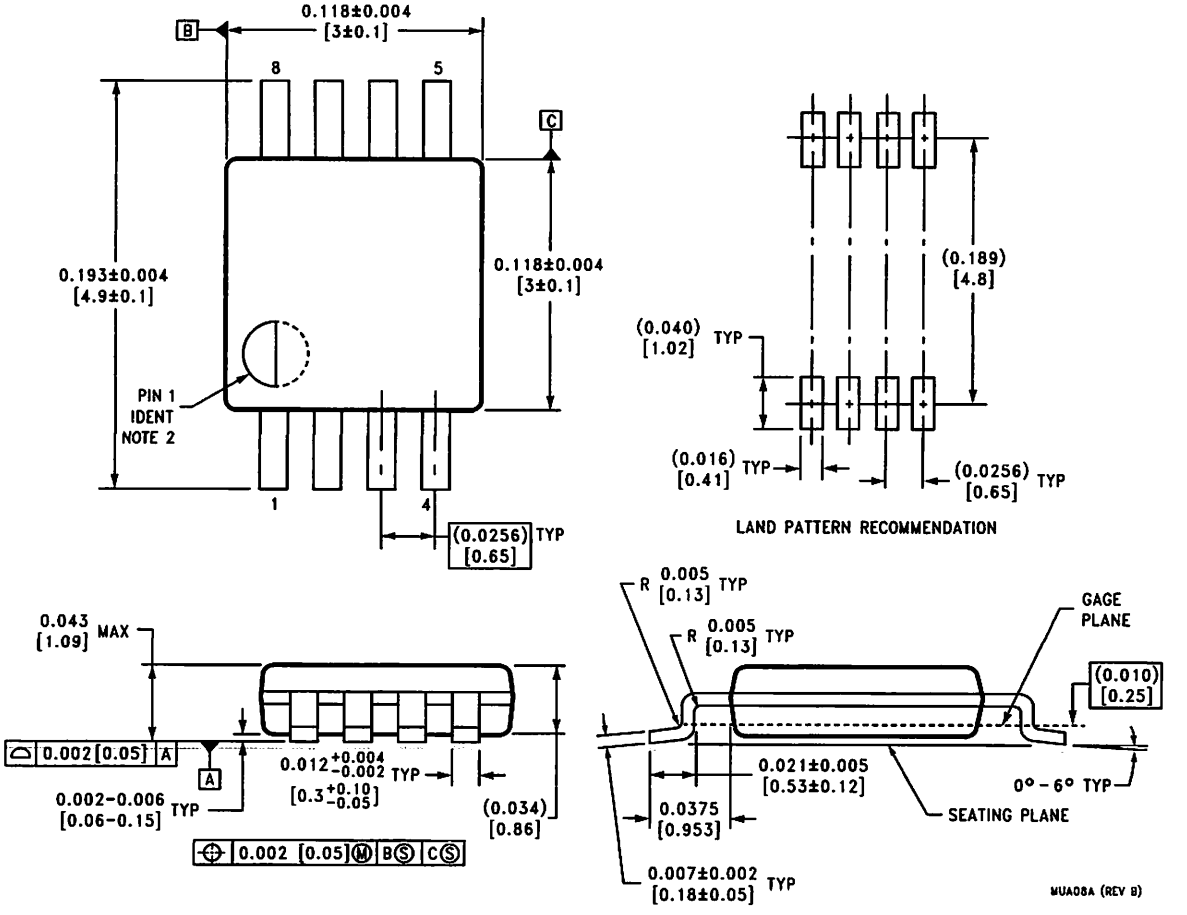
Note 8: All components must be spaced very closely to IC.

Physical Dimensions inches (millimeters) unless otherwise noted



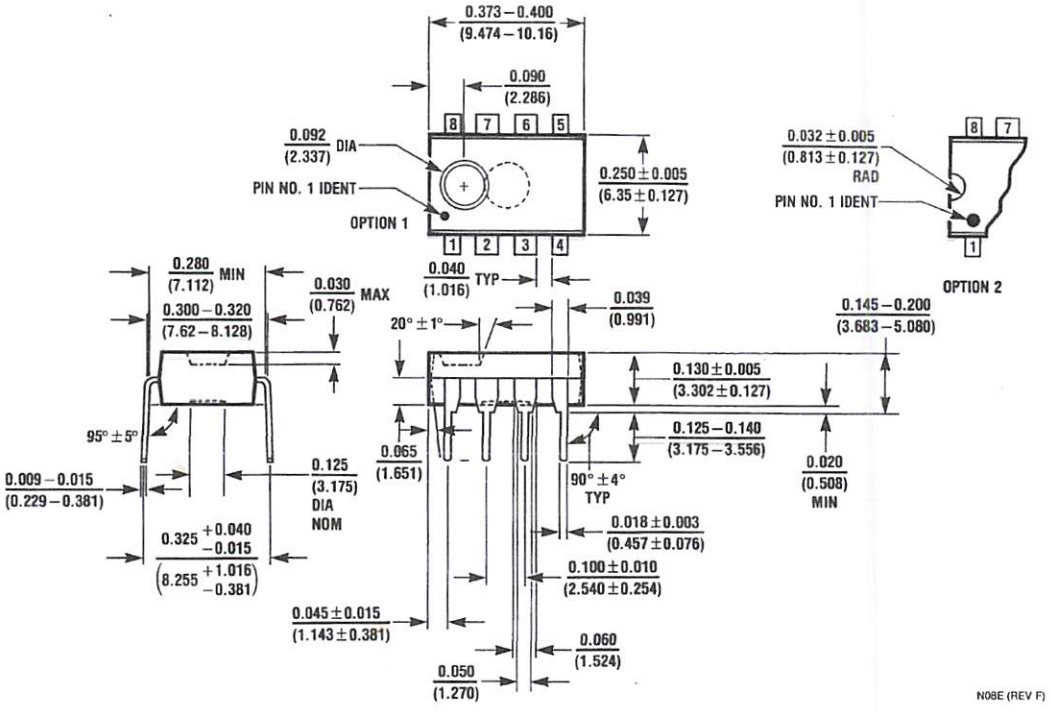
SO Package (M)
Order Number LM386M-1
NS Package Number M08A

Physical Dimensions inches (millimeters) unless otherwise noted (Continued)



8-Lead (0.118" Wide) Molded Mini Small Outline Package
Order Number LM386MM-1
NS Package Number MUA08A

Physical Dimensions inches (millimeters) unless otherwise noted (Continued)



Dual-In-Line Package (N)
Order Number LM386N-1, LM386N-3 or LM386N-4
NS Package Number N08E

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