TUGAS AKHIR

PERENCANAAN DAN PEMBUATAN KWH METER SISTEM KARTU PRABAYAR

Disusun Oleh :

Syahrurrahman

NIM : 03.52.023

KONSENTRASI TEKNIK ENERGI LISTRIK
JURUSAN TEKNIK ELEKTRO D -III
FAKULTAS TEKNOLOGI INDUSTRI
INSTITUT TEKNOLOGI NASIONAL MALANG
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LEMBAR PERSETUJUAN

PERENCANAAN DAN PEMBUATAN KWH METER SISTEM KARTU PRABAYAR

TUGAS AKHIR

Disusun dan Diajukan Sebagai Salah Satu Syarat untuk Memperoleh Gelar

Ahli MadyaTeknik Elektro

Disusun Oleh :

SYAHRURRAHMAN
03.52.023

Mengetahui,
Ketua Jurusan Teknik Elektro DIII

INSTITUT TEKNOLOGI NASIONAL MALANG FAKULTAS TEKNOLOGI INDUSTRI JURUSAN TEKNIK ELEKTRO DIPLOMA - III

Ir.H.Choirul Saleh, MT
NIP.Y. 1010088190

Disetujui,
Dosen Pembimbing

Ir. Teguh Herbasuki, MT
NIP.P. 1038900209

KONSENTRASI TEKNIK ENERGI LISTRIK
JURUSAN TEKNIK ELEKTRO DIII
FAKULTAS TEKNOLOGI INDUSTRI
INSTITUT TEKNOLOGI NASIONAL MALANG
2007

ABSTRAKSI

Perancangan dan Pembuatan KWH Meter Sistem Kartu Prabayar, Syahrurrahman, 03.52.023, Konsentrasi Teknik Energi Listrik, Jurusan Teknik Elektro DIII, Fakultas Teknologi Industri, Ir. Teguh Herbasuki, MT, Institut Teknologi Nasional Malang, 2007.

Kata Kunci : KWH Meter, PLN, Mikrokontroller.

Saat ini, untuk pencatatan pemakaian daya listrik, PLN memanfaatkan tenaga petugas PLN yang datang dari rumah kerumah, bertugas untuk mencatat nilai yang tertera pada KWH meter tiap bulannya. Setelah itu pemilik rumah harus membayar listrik pada tempat-tempat pembayaran listrik yang telah ditentukan, atau melalui fasilitas yang disediakan oleh bank (misalnya melalui *ATM*). Pencatatan seperti ini bisa saja terjadi kesalahan atau kekeliruan bahkan kecurangan dalam mencatat pemakaian daya listrik pada Kwh meter tersebut.

Berdasarkan permasalahan tersebut di atas maka diperlukan suatu alat KWH meter yang dapat ditentukan sendiri pemakaian daya listrik menggunakan *Mikrokontroller* AT89S51, dengan demikian, petugas PLN tidak perlu lagi mencatat pemakaian daya listrik dari rumah ke rumah.

Ini menjelaskan tentang implementasi sistem *Mikrokontroller* AT89S51 pada KWH meter. Metode yang digunakan dalam sistem ini adalah memasukkan sepuluh pin yang tertera di voucher pada *keypad*, yang selanjutnya *mikrokontroller* melakukan pemindahan data tersebut kepada *rangkaian panel KWH.* Untuk menghitung jumlah putaran piringan pada KWH meter dipakai sensor *optocoupler.* Selanjutnya data akan ditampilkan ke *LCD* berupa sisa KWH dan sisa pulsa. Hasil pengujian menunjukkan bahwa alat ini berjalan dengan baik.

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Malang, Maret 2007

Penulis

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BAB I

PENDAHULUAN

1.1 Latar Belakang

Di era modern ini persaingan-persaingan di bidang industri sangatlah pesat, untuk itu kadang kala masyarakat dibuat bingung untuk memilih. Khususnya di bidang kelistrikan, banyak sekali produk-produk baik itu kabel, lampu, saklar, maupun Kwh meter yang masa jenis dan beratnya sama hanya yang membedakan baik atau jeleknya suatu bahan adalah mutu dan ketahanan, tentunya yang bernilai ekonomis dan dapat dijangkau oleh masyarakat tingkat bawah.

Kwh meter sebagai alat yang dapat mengukur daya pada sistem tenaga listrik serta menghubungkan tegangan listrik dari unit tenaga listrik ke konsumen sangatlah penting, untuk itu perlu didesain dan dirancang seekonomis mungkin agar dapat memberikan keuntungan serta kemudahan bagi pengguna.

Sistem pembayaran listrik yang dilakukan di Indonesia adalah dengan menghitung daya yang terpakai, yang akan terlihat melalui KWH meter (biasa dikenal dengan meteran listrik). Ada seorang petugas untuk suatu daerah tertentu, yang datang dari rumah kerumah, bertugas untuk mencatat nilai yang tertera pada KWH meter tiap bulannya. Setelah itu pemilik rumah harus membayar listrik pada tempat-tempat pembayaran listrik yang telah ditentukan, atau melalui fasilitas yang disediakan oleh bank (misalnya melalui *ATM*).

Sistem pembayaran diatas, khususnya untuk pencatatan listrik dari rumah kerumah, memiliki beberapa kelemahan, antara lain kemungkinan kesalahan atau kekeliruan bahkan kecurangan dalam mencatat pemakaian daya listrik pada Kwh meter tersebut.

Dengan adanya hal semacam ini, penulis mencoba membuat dan merancang Kwh meter sistem kartu prabayar yang dapat ditentukan sendiri pemakaian daya listriknya sehingga konsumen tidak lagi bingung untuk memikirkan besarnya daya tagihan listrik yang harus dibayar, dilain pihak unit tenaga listrik diuntungkan pula karena tidak perlu lagi mendatangi dari rumah ke rumah untuk mencatat besarnya pemakaian daya listrik.

Kwh meter sistem kartu prabayar ini memiliki kelemahan yaitu apabila pulsa yang telah isi habis maka harus mengisinya kembali agar Kwh meter dapat berfungsi.

Jenis kartu yang digunakan pada alat ini adalah berupa Voucher dimana didalam vuocher tersebut terdapat sepuluh pin yang harus diisi melalui kayped.

1.2 Rumusan masalah.

Berdasarkan hal tersebut diatas maka timbul permasalahan seperti :

1. Bagaimana merencanakan serta membuat kwh meter sistem kartu prabayar.
2. Bagaimana menggunakan kwh meter sistem kartu prabayar.
3. Bagaimana cara mengimplementasika alat tersebut pada suatu industri ketenagalistrikan.

1.3 Batasan Masalah

Guna mencapai sasaran yang akan dibahas, serta membatasi agar tidak meluasnya masalah yang akan timbul, maka penulis membatasi masalah pada beberapa aspek yaitu :

1. Perencanaan dan pembuatan alat "Kwh meter sistem kartu prabayar".
2. Memfokuskan pada desain dan cara kerja dari alat ini berdasarkan teori yang berhubungan dengan rangkaian tersebut.
3. Alat ini hanya diterapkan pada rumah-rumah sederhana yang tidak memakai beban yang cukup besar.

1.4 Tujuan.

Merancang dan membuat alat "Kwh meter sistem kartu prabayar".adalah untuk membatasi konsumen dalam pemakaian daya listrik sesuai dengan nilai kartu yang dibeli, dilain pihak pengusaha ketenagalistrikan diuntungkan dengan pembayaran pemakaian listrik prabayar ini.

1.5 Metodologi penelitian.

Dalam merealisasikan tugas akhir ini, penulis menggunakan beberapa metode yaitu :

1) *Library research*

   Membaca buku dan mempelajarinya yang ada hubungannya dengan penyusunan tugas akhir ini.

2) *Field research*

   Yaitu memperoleh data dengan cara praktek dalam pembuatan alat.

3) Pengolahan data.

   Yaitu dengan mengolah data dengan membuat analisa secara aktual dengan menarik kesimpulan serta pengujian data yang ada.

1.6 Sistematika pembahasan

Tugas Akhir ini disusun berdasarkan beberapa teori penunjang serta bagian-bagian dari perancangan piranti sistem yang dibagi menjadi lima bab dan beberapa sub bab. Inti dari penulis dapat diuraikan sebagai berikut :

BAB I : PENDAHULUAN.

Merupakan pendahuluan yang berisikan tentang latar belakang, rumusan masalah, batasan masalah, tujuan dan metodologi penulisan serta sistematika pembahasan.

BAB II : TEORI PENUNJANG.

Membahas tentang teori dasar yang mendukung tentang rangkaian yang dipakai sebagai dasar perencanaan dan pembuatan alat yang diajukan pada Tugas Akhir ini.

BAB III : PERANCANGAN DAN PEMBUATAN ALAT.

Berisikan data-data alat yang dipakai dalam Tugas Akhir ini.

BAB IV : PENGUJIAN ALAT.

Membahas tentang pengujian peralatan secara keseluruhan.

BAB V : PENUTUP.

Berisikan kesimpulan dan saran-saran yang didapat selama perencanaan dan pembuatan alat serta kemungkinan pengembangan yang dapat dilakukan pada alat yang dirancang.

Selain beberapa bab yang telah disebutkan diatas, dalam tugas akhir ini disertakan juga beberapa lampiran mengenai rangkaian yang dipakai, dan beberapa informasi lainnya yang mendukung tugas akhir ini.

BAB II

DASAR TEORI

Bab ini akan menguraikan tentang dasar-dasar teori yang menunjang dalam perencanaan dan pembuatan Kwh meter sistem kartu prabayar. Uraian teori dalam bab ini meliputi teori IC AT89S51, Kwh meter, optocoupler, infrared , Photodioda, LCD, Keypad, dan perangkat pendukung lainnya.

2.1. Mikrokontroler AT89S51

2.1.1. Pendahuluan

Perbedaan mendasar antara mikrokontroller dan mikroprosesor terletak pada kelengkapan isinya yaitu mikrokontroller sudah dilengkapi dengan berbagai macam alat kontrol selain memiliki CPU juga dilengkapi memori(ROM & RAM) maupun input output yang merupakan kelengkapan minimum sistem sedangkan mikroprosesor kesemuanya itu tidak dimiliki secara internal melainkan terpisah. Sebuah mikrokontroller dapat dikatakan sebagai mikrokomputer dalam keping tunggal *(Singgle Chip Microcomputer)* yang dapat berdiri sendiri.

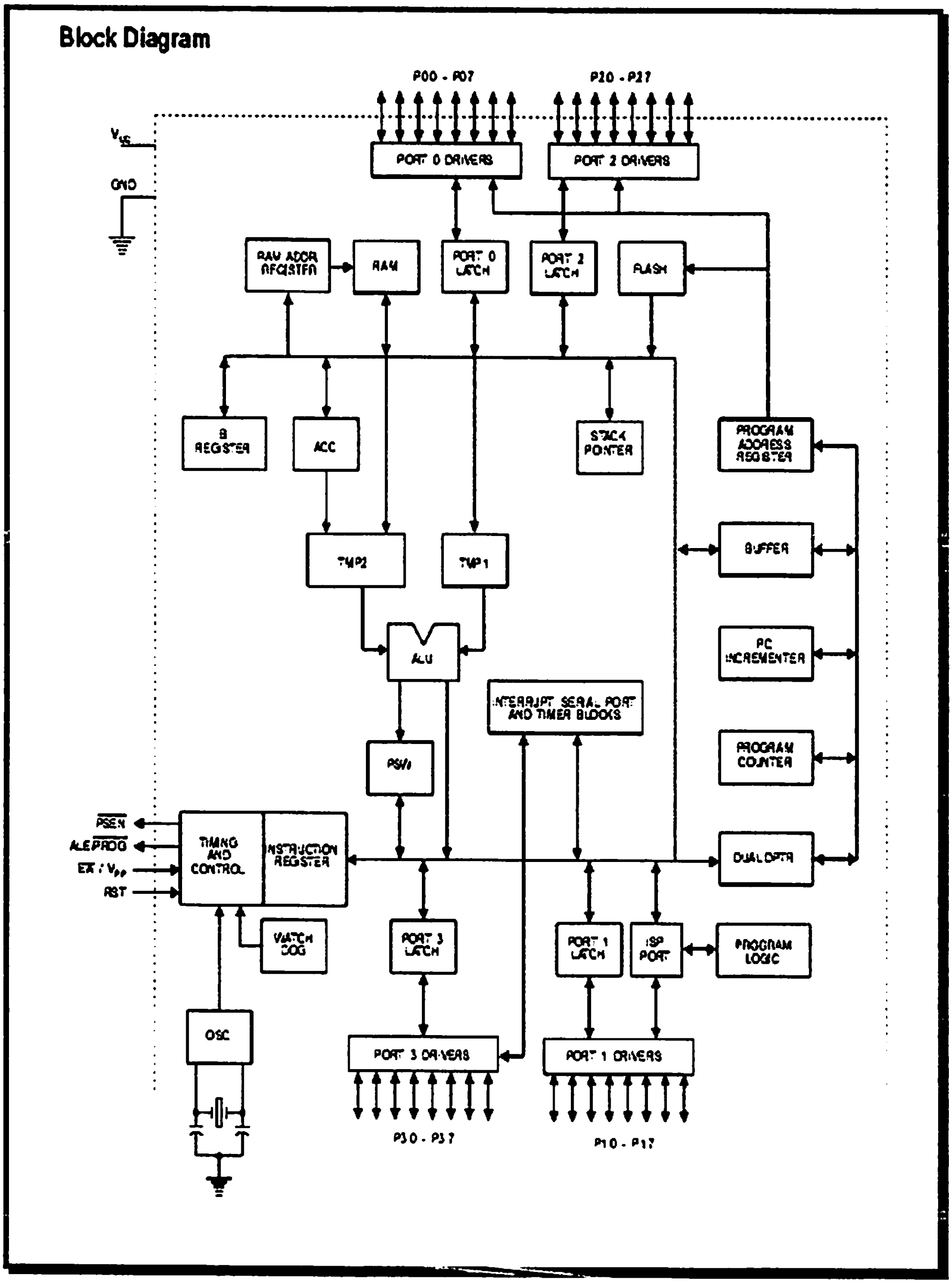
Mikrokontroller AT89S51 adalah mikrokontroller buatan ATMEL yang kompatibel penuh dengan mikrokontroler keluarga MCS-51, hanya membutuhkan daya rendah, memiliki performance yang tinggi dan merupakan mikrokomputer 8 bit yang dilengkapi 4Kbyte EEPROM *(Electrical Erasable and Programmable Read Only Memory)* dan 128 Byte RAM internal. Program memori dapat diprogram dalam sistem atau menggunakan programmer *Nonvolatile* Memory konvensional. Dalam sistem mikrokontroller terdapat dua hal yang mendasar, yaitu: perangkat lunak dan perangkat keras yang keduanya saling terkait dan mendukung.

2.1.2. Perangkat keras mikrokontroler AT89S51

Secara umum Mikrokontroller AT89S51 memiliki :

- CPU 8 bit termasuk keluarga MCS-S I
- 4 Kb Flash memory
- 128 byte Internal RAM
- 32 buah Port I/O,masing - masing terdiri atas 8 jalur I/O
- 2 Timer / counter 16 bit
- 2 Serial Port Full Duplex
- 2 DPTR *(Data pointer)*
- *System Interrupt* dengan 2 sumber *Interrupt* eksternal dan 4 sumber *Interrupt* internal.
- Fleksibel ISP Programming

Dengan keistimewaan diatas pembuatan alat menggunakan AT89S51 menjadi lebih sederhana dan tidak memeriukan IC pendukung yang banyak. Adapun blok diagram dari Mikrokontroller AT89S51 adalah sebagai berikut:



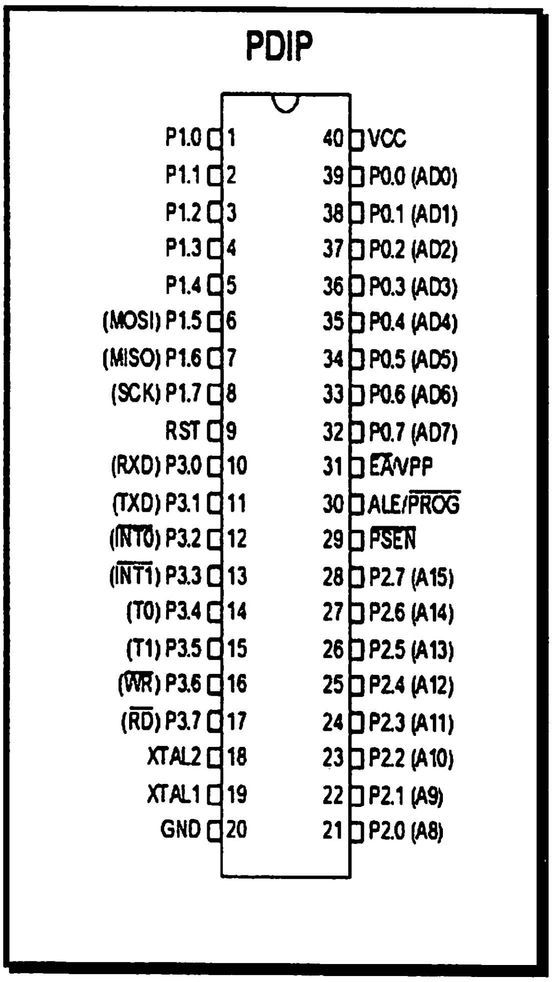
Gambar 2-1

Diagram Blok Mikrokontroller AT89S51

Sumber : Datasheet AT89S51

2.1.3. Konfigurasi Pena-Pena Mikrokontroller AT89S51

Mikrokontroller AT89S51 terdiri dari 40 pin dengan konfigurasi sebagai Berikut :



Gambar 2-2

Konfiburasi Pena-Pena AT89S51

Sumber :Datasheet AT89S51

Fungsi tiap-tiap pin-nya adalah sebagai berikut :

- VCC (Supply tegangan), pin 40
- GND (*Ground*), pin 20
- Port 0, pin 32 – 39

Merupakan port input-output dua arah, tanpa internal pull-up dan dikonfigurasikan sebagai multipleks bus alamat rendah (A_o - A7) dan data selama pengaksesan memori eksternal. Setiap pin-nya dapat mengendalikan langsung 8 beban TTL. Port 0 juga menerima dan mengeluarkan *code byte* selama proses pemrograman dan verifikasi ROM/EEPROM internal.

- Port 1, pin 1 - 8

Merupakan port input-output dua arah dengan internal pull-up yang dapat mengendalikan beban 4 TTL secara langsung dan mempunyai kegunaan lain yaitu sebagai port ISP header.

Tabel 2-1

Port ISP Header

Port Pin	Alternate Functions
P1.5	MOSI (used for In-System Programming)
P1.6	MISO (used for In-System Programming)
P1.7	SCK (used for In-System Programming)

Sumber :Datasheet AT89S51

- Port 2, pin 21 - 28

Merupakan port input-output dengan internal pull-up. Mengeluarkan alamat tinggi selama pengambilan program memori external.

- Port 3, pin 10 – 17

Merupakan port input-output dengan internal pull-up, dimana Port 3 juga memiliki fungsi khusus dan dapat dilihat pada tabel berikut ini

Tabel 2-2

Fungsi Khusus Pada Port 1

Simbol	Posisi	Nama dan arti
/RD	P3.7	*External data memori read strobe*
/WR	P3.6	*External data memori write strobe*
T1	P3.5	*Timer / counter 1 external input*
T0	P3.4	*Timer / counter 0 external input*
/INT1	P1.3	*External interrupt 1*
/INT0	P1.2	*External interrupt 0*
TXD	P1.1	*Serial data output port*
RXD	P1.0	*Serial data input port*

- RST *(Reset)*, pin 9

  Input Reset merupakan reset master untuk AT89S51.

- ALE/ Prog *(Address Latch Enable)*,pin30

  Digunakan untuk memberikan sinyal *latch* pada alamat rendah pada multipleks *bus addres* dan data.

- PSEN (*Program Store Enable)*, pin 29

  Merupakan sinyal pengontrol yang memperbolehkan program memori eksternal masuk ke dalam bus.

- EA / VPP *(External Access)*, pin 31

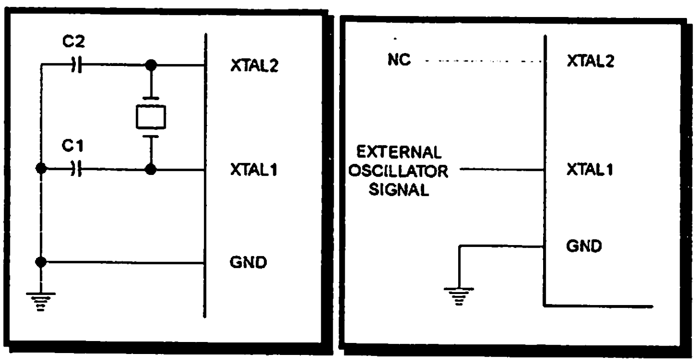
  Dapat diberikan logika rendah *(Ground)* atau logika tinggi (+5V). Jika diberikan logika tinggi maka mikrokontroller akan mengakses program dari *ROM* internal *(EEPROM / Flash Memory)*, dan jika diberikan logika rendah maka mikrokontroller akan mengakses program dari memori eksternal.

- X-TAL 1 dan X-TAL 2, pin 19,18

  Kaki ini dihubungkan dengan kristal bila menggunakan *osilator internal*. XTAL 1 merupakan *input inverting osilator amplifier* sedangkan XTAL 2 merupakan *output inverting osilator amplifier*

2.1.4. Karakteristik *Oscillator Inverting.*

XTAL 1 dan XTAL 2 secara berurutan merupakan *input* dan *output* dari sebuah *inverting amplifier* yang dapat dikonfigurasikan penggunaannya sebagai *on chip oscillator* seperti yang ditunjukkan pada gambar 2-3a dibawah ini. XTALI dan XTAL 2 ini dapat menggunakan sebuah *kristal quartz* maupun *resonator* keramik.



a) *Oscilator Connector* b) *External Clock Configuration*

Gambar 2-3

Karakteristik *Oscillator*

Sumber : Datasheet AT89S51

Untuk memberikan AT89S51 sumber *clock external.* Maka pin XTAL 2 dibiarkan tidak terhubung.dan XTAL 1 dihubungkan dengan sumber *clock external* seperti pada gambar 2-3b.

2.1.5. Organisasi Memori.

Mikrokontoller AT89S51 memiliki ruang alamat memori data dan memori program yang terpisah. Pemisahan memori program dan memori data tersebut membolehkan memori data diakses dengan alamat 8-bit, sehingga dapat dengan cepat dan mudah disimpan dan dimanipulasi oleh CPU 8-bit. Namun demikian, alamat memori data 16-bit bisa juga dihasilkan melalui register DPTR.

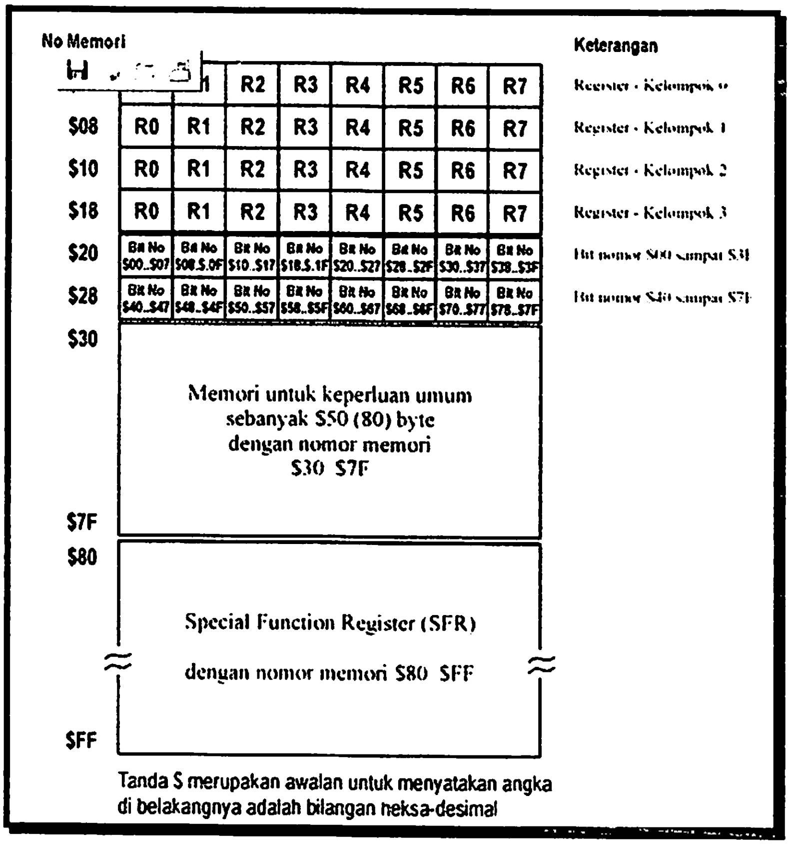
2.1.5.1. Program Memori

Program memori hanya dapat dibaca, tidak dapat ditulis. Disini tersimpan program yang akan dijalankan oleh AT89S51 dan data-data konstanta. Sinyal pembacaan EPROM eksternal adalah dari pin-PSEN. Pada AT89S51 ada dua tipe organisasi memori dari program memori, yaitu :

- Pengaksesan program memori sebagian berasal dari internal EPROM yang menempati alamat terendah dan alamat berikutnya dari EPROM eksternal. Sebagai contoh alamat 4 Kbyte program memori terendah adalah ROM internal dan alamat berikutnya adalah pada EPROM.
- Pengaksesan program memori yang semuanya dari eksternal EPROM.

2.1.5.2 Data Memori

Data memori menempati alamat yang terpisah dari program memori. Data memori merupakan tempat penyimpanan data variabel, operasi *stack* dan sebagainya. Data memori dapat dibaca dan ditulis. Sinyal pembacaan untuk emsternal RAM berasal dari pin –RD dan untuk penulisan berasal dari pin –RW. Peta data memori digambarkan sebagai berikut :



Gambar 2-4

Denah Memori Data

Sumber : www.ALDS.edu.com

Alamat 00H-FFH merupakan alamat dari internal RAM yang dapat dialamati dalam dua mode. Pada alamat 00H-7FH dapat dialamati dalam *mode direct* maupun *indirect addressing.* Alamat 80H-FFH hanya dapat dialamati dalam *mode direct addressing.* Diluar alat tersebut merupakan alamat eksternal RAM. 32 byte terendah data memori terbagi atas 4 buah bank yang masing-masing terdiri atas 8 buah register. Kombinasi dari bank ini ditentukan oleh register PSW. Register-register tersebut adalah R0 sampai R7 yang menempati alamat 00H-1FH. Diatasnya merupakan segmen bit *addresable* yang besarnya 16 byte, menempati alamat 20H sampai 2FH. Alamat berikutnya yaitu mulai 30H sampai 7FH dapat dipakai sebagai data RAM.

Setelah kondisi reset, kondisi baku register SP (*stack pointer)* akan menuju alamat 07H dan begitu program dijalankan isi register SP akan ditambah 1 (menunjuk ke alamat 08H). Dan ini merupakan register bank 1 register R0. Bila memakai lebih dari satu bank register maka SP harus diinisialisasikan kelokasi yang lain.

2.1.6. SFR *(Special Function Register)*

Register Fungsi Khusus *(Special Function Register)* terletak pada 128 byte bagian atas memori data internal dan berisi register-register untuk pelayanan latch port, timer, program status words, control peripheral, dan sebagainya. Alamat register fungsi khusus ditunjukkan pada tabel 2-3

Tabel 2-3

Special Function Register

Simbol	Nama Register	Alamat
ACC	Accumulator	E0H
B	Register B	F0H
PSW	Program Status Word	D0H
SP	Stack Pointer	81H
DPTR	Data Pointer	
DPL	Bit Rendah	82H
DPH	Bit Tinggi	83H
P0	Port 0	80H
P1	Port 1	90H
P2	Port 2	A0H
P3	Port 3	B0H
IP	Interrupt Periority Control	D8H
IE	Interrupt Enable Control	A8H
TMOD	Timer/Counter Mode Control	89H
TCON	Timer/Counter Control	88H
TH0	Timer/Counter High 0	8CH
TL0	Timer/Counter Low 0	8AH
TH1	Timer/Counter High 1	8DH
TL1	Timer/Counter Low 1	8BH
SCON	Serial Control	98H
SBUF	Serial Data Buffer	99H
PCON	Power Control	87H

Beberapa macam register fungsi khusus yang sering digunakan adalah sebagai berikut ini :

- *Accumulator* (ACC) merupakan register untuk penambahan dan pengurangan. Perintah *mnemonic* untuk mengakses akumulator disederhanakan sebagai A.
- *Register B* merupakan register khusus yang berfungsi melayani operasi perkalian dan pembagian.
- *Stack Pointer* (SP) merupakan register 8 bit yang dapat diletakkan di alamat manapun pada RAM internal.

- *2 Data Pointer* (DPTR) terdiri dari dua register, yaitu untuk byte tinggi *(Data Pointer High,* DPH) dan byte rendah *(Data Pointer Low,* DPL) yang berfungsi untuk mengunci alamat 16 bit.
- *Port 0* sampai *Port 3* merupakan register yang berfungsi untuk membaca dan mengeluarkan data pada port 0, 1, 2, 3. Masing-masing register ini dapat di alamati per-byte maupun per-bit.
- *Control Register* terdiri dari register yang mempunyai fungsi kontrol. Untuk mengontrol sistem interupsi, terdapat dua register khusus, yaitu register IP *(Interupt Priority)* dan register IE *(Interupt Enable).* Untuk mengontrol pelayanan timer/counter terdapat register khusus, yaitu register TCON *(timer/counter control)* serta pelayanan port serial menggunakan register *SCON (Serial Port Control).*

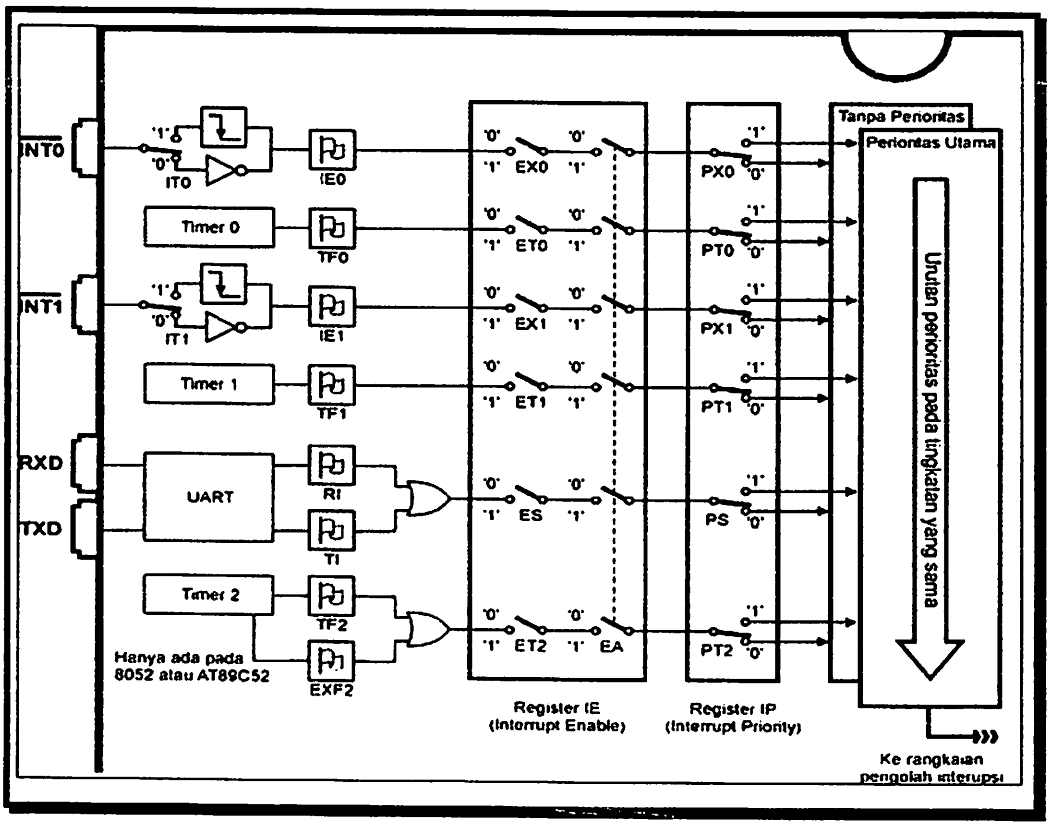
2.1.7. Sistem Interupsi

Mikrokontroller AT89S51 mempunyai 5 buah sumber interupsi yang dapat membangkitkan permintaan interupsi, yaitu INT0, INTI, T0, T1 dan Port Serial. Saat terjadinya interupsi mikrokontroller secara otomatis akan menuju ke subrutin pada alamat tersebut. Setelah interupsi selesai dikerjakan, mikrokontroller akan mengerjakan program semula. Tiap-tiap sumber interupsi dapat *enable* atau *disable* secara software.

Tingkat prioritas semua sumber *interupt* dapat diprogram sendiri-sendiri dengan *set* atau *clear* bit pada *(Interupt Priority).* Jika dua permintaan interupsi dengan tingkat prioritas yang berbeda diterima secara bersamaan, permintaan interupsi dengan prioritas tertinggi yang akan dilayani. Jika permintaan interupsi dengan prioritas yang sama diterima bersamaan, akan dilakukan polling untuk menentukan mana yang akan dilayani.

Kedudukan saklar dalam gambar dibawah ini menggambarkan kedudukan awal setelah MCS51 di-reset.Gambar ini sangat membantu saat penulisan program menyangkut interupsi.

MCS51.



Gambar 2-5

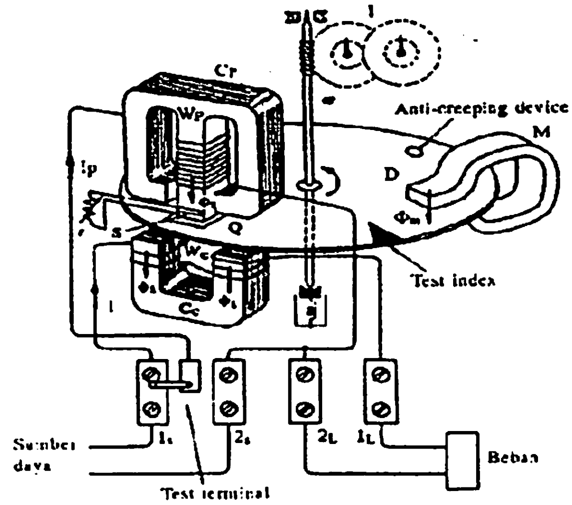
Sumber Intrupsi

Sumber : www.alds.edu.com

2.2. KWH METER.

Pemakaian energi listrik di Indonesia menggunakan satuan *kilowatt-hour* (KWH), dimana 1 KWH sama dengan 3,6 MJ. Karena itulah alat yang digunakan untuk mengukur energi pada industri dan rumah tangga dikenal dengan *watthourmeters*. Besar tagihan listrik biasanya berdasarkan pada angka-angka yang tertera pada KWH meter setiap bulanya untuk saat ini. KWH meter induksi adalah satu-satunya tipe yang digunakan pada perhitungan daya listrik rumah tangga.

Bagian-bagian utama dari sebuah KWH meter adalah kumparan tegangan, kumparan arus, sebuah piringan alumunium, sebuah magnet tetap, dan sebuah gir mekanik yang mencatat banyaknya putaran piringan. Jika meter dihubungkan ke daya satu fasa, piringan mendapat torsi yang membuatnya berputar seperti motor dengan tingkat kepresisian yang tinggi.



Gambar 2-6

Cara Kerja KWH Meter

Dari gambar 2.6. dapat dijelaskan cara kerja dari KWH meter sebagai berikut :

- Arus beban I menghasilkan fluks bolak-balik Φ_c, yang melewati piringan alumunium dan menginduksinya, sehingga menimbulkan tegangan dan *eddy current* I_f.
- Kumparan tegangan B_p juga menghasilkan fluks bolak-balik Φ_p yang meminta arus I_f. Karena piringan itu mendapat gaya, dan resultan dari torsi membuat piringan berputar.

Torsi ini sebanding dengan fluks Φ_p dan arus I_f serta harga cosinus dari sudut antaranya. Karena Φ_p dan I_f sebanding dengan tegangan E dan arus beban I , maka torsi motor sebanding dengan EI cos θ,yaitu daya aktif yang diberikan ke beban. Karena itu kecepatan putaran piringan sebanding dengan daya aktif yang terpakai. Semakin besar daya yang terpakai, kecepatan piringan semakin besar, demikian pula sebaliknya.

Secara umum perhitungan untuk daya listrik dapat di bedakan menjadi tiga macam, yaitu :

- Daya kompleks S(VA) = V.I
- Daya reaktif Q(VAR) = V.I sin θ
- Daya aktif P(Watt) = V.I cos θ

Hubungan dari ketiga daya diatas dapat dituliskan dengan menggunakan rumus sebagai berikut :

$$S = \sqrt{P^2 + Q^2}$$

$$S = \sqrt{(VI)^2}.(\sin^2 \Phi + \cos^2 \Phi)$$

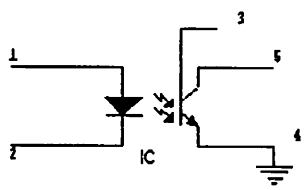
$$S = V.I$$

Dari ketiga daya diatas, yang terukur pada Kwh meter adalah daya aktif yang dinyatakan dengan satuan *Watt*. Sedangkan daya reaktif dapat diketahui besarnya dengan menggunakan alat ukur *Varmeter*. Untuk pemakaian pada rumah, biasanya hanya digunakan Kwh meter.

2.3. Optocoupler.

Kopel Optik (*optocoupler*) adalah isolator yang terhubung *optic*, merupakan gabungan LED dan *photodetector* dalam suatu rangkaian. *Optocoupler* dapat digunakan sebagai saklar apabila diberikan tegangan masuk yang sesuai.

Apabila ada arus DC yang mengalir secara *forward* (maju) melalui dioda LED, maka LED akan mengemisikan sinar infra merah kepada transistor foto NPN. Jika transistor dihubungkan ke catu daya, maka sinar ini membuat transistor menjadi on. Kegunaan dari *optocoupler* pada alat ini adalah sebagai pemberi informasi kepada mikrokontroler dengan cara memberikan logika "1" dengan tegangan 5 volt, atau logika "0" dengan tegangan 0 volt.

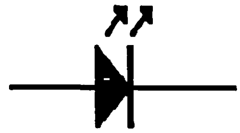


Gambar 2-7

Skema Optocoupler

2.4. Light Emitting Dioda (LED) Infra Merah

Selain oleh matahari, cahaya jenis ini dapat dibangkitkan melalui difusi pada dioda semikonduktor yang biasa disebut LED *(Light Emitting Dioda)*. Sedangkan dioda sendiri banyak jenisnya termasuk yang bisa memancarkan cahaya saat dialiri arus *forward* padanya dimana elektron dari pita konduksi melewati *junction* dan jatuh ke dalam hole pita valensi sehingga elektron-elektron tersebut memancarkan energi. Pada dioda biasa energi ini dipancarkan melalui panas. Dan dioda yang tidak memancarkan cahaya contohnya adalah dioda zener maupun dioda biasa. Simbol dari LED infra merah ini dapat dilihat pada gambar berikut :

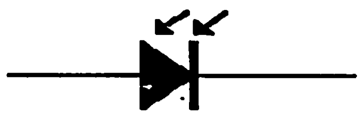


Gambar 2-8

Simbol LED Infra Merah

2.4.1 Photodioda

Photodioda memiliki sifat kebalikan dari LED infra merah di atas, dimana jenis dioda ini akan mengalirkan arus *forward* saat dikenai cahaya infra merah padanya. Kuat arus yang mengalir juga tergantung dari kuatnya cahaya infra merah yang jatuh pada dioda tersebut. Bila cahaya lain mengenainya maka dioda ini berfungsi sebagai sumbatan yang memiliki impedansi yang sangat tinggi sekali. Prinsip kerja photodioda sama dengan phototransistor. Hanya yang membedakan antara keduanya yaitu kalau photodioda tidak memiliki penguatan arus pada anodanya, sedangkan pada phototransistor memiliki penguatan pada arus kolektornya sebesar hasil kali antara "hfe" dengan kuat cahaya yang jatuh pada basis phototransistor. Simbol dari photodioda sama dengan LED infra merah yang membedakan hanya arah tanda panahnya masuk menuju dioda. Berikut adalah simbol dari photodioda :



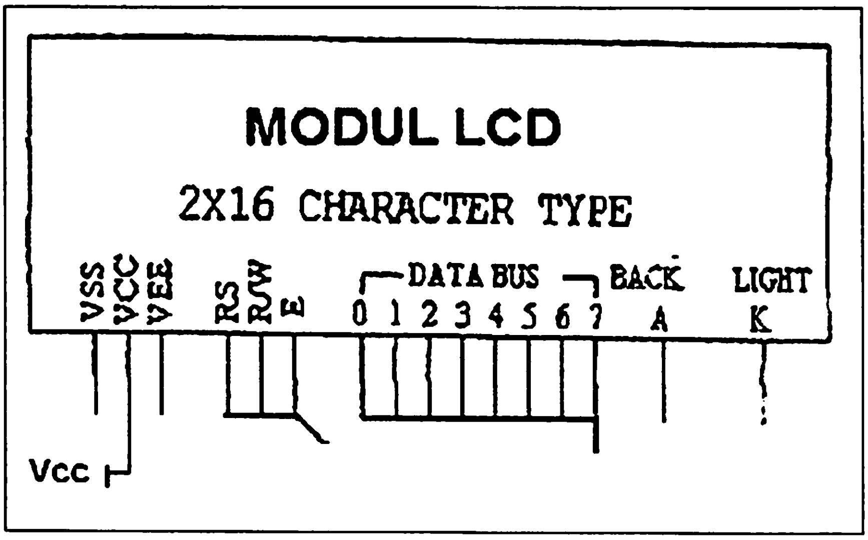
Gambar 2-9

Simbol Photodioda

2.5 LCD (Liquid Crystal Display).

Modul peraga yang digunakan dalam aplikasi ini adalah LCD modul M1632. Modul LCD ini membutuhkan daya yang kecil dan dilengkapi dengan panel LCD dengan tingkat kontras yang cukup tinggi serta pengendali LCD CMOS yang terpasang dalam modul tersebut. Pengendali mempunyai pembangkit karakter ROM/RAM dan display data RAM. Semua fungsi display diatur oleh instruksi-instruksi, sehingga modul LCD ini dapat dengan mudah dihubungkan dengan unit mikroprosesor. LCD tipe ini tersusun sebanyak dua baris dengan 16 karakter.

Masukan yang diperlukan untuk mengendalikan modul berupa bus data yang masih termutiplek dengan bus alamat serta 3 bit sinyal kontrol. Sementara pengendalian LCD dilakukan secara internal oleh kontroler yang sudah terpasang dalam modul LCD. Diagram blok untuk LCD dapat dilihat dalam Gambar 2-10



Gambar 2-10

Diagram Blok LCD M1632

Sumber: El-Tech, 1987

LCD M1632 mempunyai 16 pin atau penyemat yang mempunyai fungsi-fungsi seperti ditunjukkan dalam Tabel 2.4

Tabel 2.4

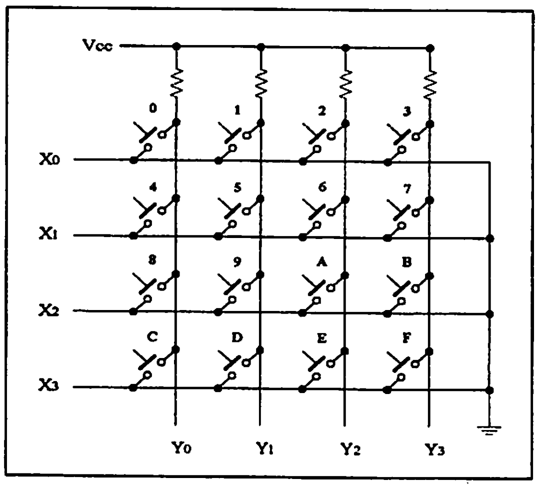
Fungsi pin-pin LCD M1632

No	Nama Penyemat	Fungsi
1	Vss	Terminal ground
2	Vcc	Tegangan catu +5 volt
3	Vee	Drive LCD
4	RS	Sinyal pemilih register 0: Instruksi register (tulis) 1: Data Register (tulis dan baca)
5	R/W	Sinyal seleksi tulis atau baca 0: Tulis 1: Baca
6	E	Sinyal operasi awal, sinyal ini mengaktifkan data tulis dan baca
7 – 14	DB0-DB7	Merupakan saluran data, berisi perintah dan data yang akan ditampilkan
15	V+ BL	Pengendali kecerahan latar belakang LCD 4 - 4,42 V dan 50 – 500 mA
16	V-BL	Pengendali kecerahan latar belakang LCD 0 V

Sumber: Seiko, 1987

2.6. Tombol Masukan (*Keypad*)

Tombol masukan merupakan suatu perangkat atau komponen ·yang memberikan masukan data melalui penekanan tombol masukan yang terdapat pada papannya. Dalam perencanaan ini, tombol masukan (*keypad*) yang digunakan adalah *keypad* matrik 4x4. *Keypad* ini berfungsi untuk memberikan masukan kepada mikrokontroler untuk melakukan operasi pengaturan manual,. Prinsip kerja keypad matrik dapat dilihat dari Gambar 2-11 :



Gambar 2-11

Keypad Dot Matrik 4x4

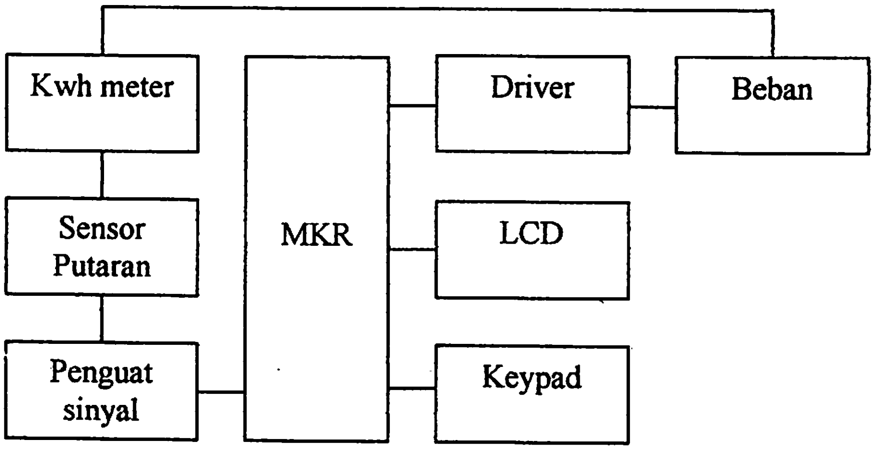
Sumber: Mazidi, 1995

Gambar 2.11 terlihat bahwa *keypad* matrik ini terdiri atas 4 lajur baris (X_0-X_3) dan 4 lajur kolom (Y_0-Y_3), dan *keypad* ini akan bekerja dengan menggunakan prinsip *scanning* pada lajur baris dan lajur kolom tersebut. Jika terdeteksi adanya persambungan antara baris dan kolom *valid*, maka data dari *keypad* tersebut akan diterjemahkan pada mikrokontroler.

BAB III

PERENCANAAN ALAT

KWH METER SISTEM KARTU PRABAYAR



Gambar 3-1

Blok Diagram Kwh Meter Sistem Kartu Prabayar

Sumber: perencanaan

Cara kerja :

1. Piringan pada Kwh meter dilubangi dengan satu lubang, ketika ada beban piringan akan berlubang.
2. Setiap perputaran dideteksi dengan lubang yang ada.
3. Pada saat optocopler terhalang, keluaran rangkaian pengkondisi sinyal logika rendah atau ligika nol.
4. Pada saat terdeteksi ada lubang, rangkaian pengkondisi sinyal logika satu
5. Logika – ligika keluaran dari rangkaian pengkondisi sinyal tadi digunakan oleh mikrokontroler untuk menghitung banyaknya kumparan-kumparan pada Kwh meter.

6. Setelah melalui perhitungan, mikrokontroler mengeluarkan data tersebut ke LCD.

7. Selain ditampilkan di LCD, hasil perhitungan tadi digunakan juga untuk membandingkan energi yang diminta dengan energi yang sudah dipakai.

8. Apabila energi yang telah dipakai lebih besar dari energi yang dipesan maka triac dinonaktifkan . Begitu juga sebaliknya.

Umum :

- KWH

  Dalam perancangan dan pembuatan alat ini KWH meter tidak dibuat sendiri, melainkan menggunakan KWH meter yang sudah ada dipasaran. KWH meter yang digunakan adalah KWH 1 fasa dimana tertulis 900 putaran per KWH. Diantara piringan KWH ini dipasang sebuah sensor optocoupler.

- Sensor Optocoupler

  Sensor Optocoupler yang digunalan adalah Tipe U, dimana terdapat sebuah photodioda dan led inframerah. Cara kerja dari optocoupler ini adalah apabila cahaya led inframerah menembus lubang pada piringan KWH maka kondisi photo-dioda mempunyai hambatan kecil, sehingga tegangan tidak dibias, melainkan mengalir ke *ground.* Akibatnya transistor berada dalam kondisi *cut off* , sehingga tegangan Vcc transistor akan mengalir ke mikrokontroler.

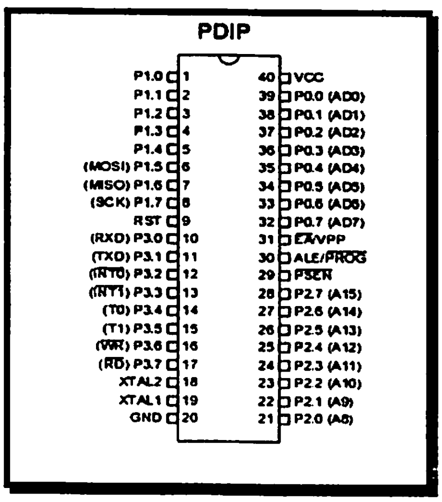
- LCD

LCD yang digunakan adalah LCD 16 X 2 berfungsi untuk menampilkan data yang diolah MC dari pembacaan optocoupler. Tampilan LCD berupa karakter dalam bentuk "jumlah KWH" dan "jumlah BEBAN" yang dipakai.

3.1. Mikrokontroler AT89S51

Mikrokontroler akan mengolah data pulsa dari keyped dan mengecek apakah data tersebut sudah sesuia dengan nomor voucer serial pulsa.

Mikrokontroller AT89S51 terdiri dari 40 pin dengan konfigurasi sebagai Berikut :



Gambar 3-2

Konfiburasi Pena-Pena AT89S51

Sumber :Datasheet AT89S51

Fungsi tiap-tiap pin-nya adalah sebagai berikut :

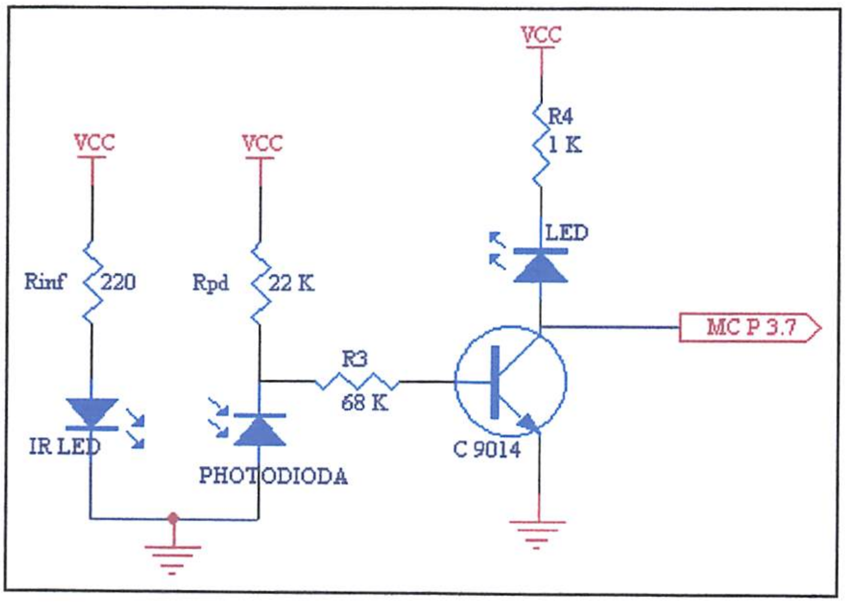
- Port 3.2 Membaca banyaknya putaran piringan pada Kwh meter.
- Port 1.7 Merupakan output data yang akan dikirim dari triac 4004.
- Port 3.7 Merupakan indicator pulsa.

Untuk menghidupkan LED didalam MOC diperlukan arus sebesar 10 mA, LED = 1,5 Volt.

$$R = \frac{5-1,5}{1.10^{-3}}$$
$$R = \frac{3,5}{1.10^{-3}}$$
$$R = \frac{3,5.10^{-3}}{1}$$
$$R = \frac{350}{1}$$
$$R = 350$$

3.2. Rangkaian Optocoupler

Optocoupler pada perencanaan alat ini, digunakan sebagai suatu piranti untuk mengambil data dari KWH meter. Optocoupler ini akan dipasang pada piringan KWH meter untuk membaca data putaran dari piringan KWH tersebut. Adapun gambar rangkaian dari optocoupler adalah sebagai berikut :



Gambar 3-3

Rangkaian Optocoupler

Sumber :Datasheet

Untuk menentukan besarnya tahanan yang digunakan pada Vcc optocoupler dapat dicari dengan cara seperti berikut :

Dari karakteristik data book $I_{INFRARED}$ = 5 - 20 mA dan tegangannya antara 1,5 – 2 V. Maka besarnya R yang digunakan adalah :

$$R_{\text{inf}} = \frac{V_{CC} - V_{\text{inf}}}{I_{\text{inf}}}$$

$$= \frac{5 - 1{,}5}{16.10^{-3}} = 218{,}75 \approx 220\ \Omega$$

3.2.1. Kondisi Photo-Dioda Tidak Mendapat Cahaya

Pada saat kondisi ini Photodioda mempunyai hambatan besar sekali sehingga tegangan dari Vcc dibias ke transistor. Arus yang melewati photo dioda max 10 mA, *Photo-diode* adalah diode yang mampu merespon pancaran cahaya.

Jika arus yang dialirkan pada *photo-dioda* sebesar 0,6 mA dan tegangannya sebesar 5 V maka diperlukan tahanan sebesar :

$$R_{pd} = \frac{Vcc}{I_{PD}}$$

$$R_{pd} = \frac{Vcc}{0{,}23x10^{-3}}$$

$$R_{pd} = 21{,}7K \approx 22K\Omega$$

Untuk mengkondisikan transistor C9014 berada dalam kondisi saturasi (Vce = 0), maka tegangan yang dibutuhkan transistor adalah (V_{photo}=2,3) :

$Vcc = V_R + V_{Photo}$

$V_R = Vcc - V_{photo}$

$V_R = 5 - 2{,}3$

$V_R = 2{,}7$ Volt

Dengan menetukan nilai Rc sebesar 1 K maka kita bisa menghitung nilai Ic :

$$I_C = \frac{V_{CC} - V_{CE}}{R_C}$$

$$= \frac{5-0}{1000}$$

$$= 5 \text{ mA}$$

Dari *data sheet* diketahui nilai βdc dari transistor C9014 = 186, maka nilai Ib dapat dicari :

$$I_B = \frac{I_C}{\beta dc}$$

$$= \frac{5mA}{186} = 27\ \mu A$$

setelah nilai I_C dan nilai I_B sudah dicari maka kita dapat mencari nilai R_B :

$$R_B = \frac{V_B - V_{be}}{Ib}$$

$$= \frac{(2,7-0,7)V}{27.10^{-6}}$$

$$= 62,9 \text{ K} \approx 68 \text{ K}\Omega$$

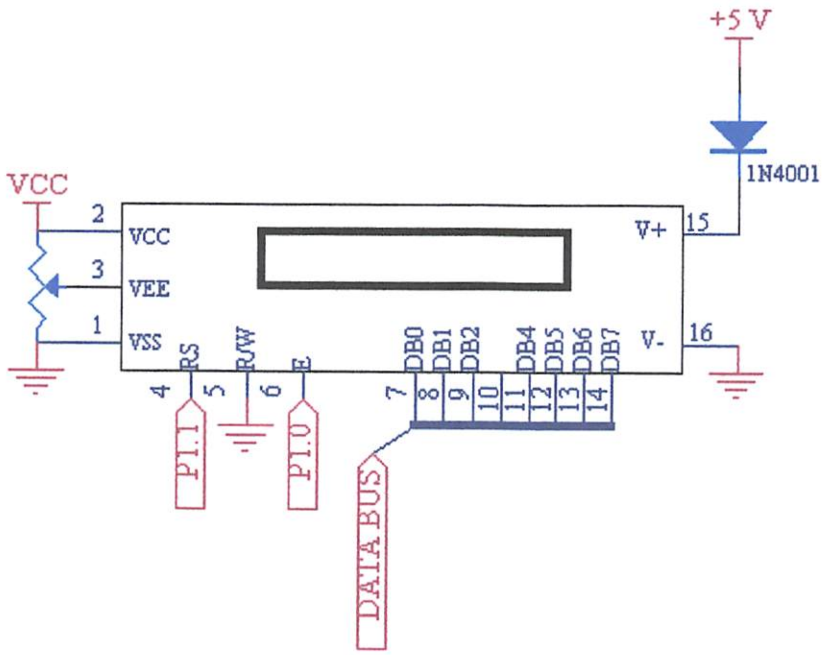
Dengan transistor berada dalam keadaan saturasi maka tegangan Vcc akan mengalir ke ground. Sehingga praktis dapat dikatakan tegangan yang mengalir menuju mikrokontroller adalah 0 V.

3.2.2. Kondisi Photo-Dioda Mendapat Cahaya

Pada saat ini kondisi ini photo-dioda mempunyai hambatan kecil, sehingga tegangasn tidak dibias, melainkan mengalir ke *ground*. Akibatnya transistor berada dalam kondisi *cut off*, sehingga tegangan Vcc transistor akan mengali ke mikrokontroller. Jadi dapat disimpulkan bahwa photo-dioda tidak mendapat cahaya maka logika mikrokontroller adalah 0 (*low*). Pada saat photodioda mendapat cahaya maka logika ke mikrokontroller adalah 1 (*high*).

3.3. Rangkaian LCD

Untuk menampilkan keluaran data berupa karakter 8 bit yang ada baik dari sisi pengirim maka diperlukan suatu komponen yaitu LCD.



Gambar 3-4

Rangkaian LCD

Sumber :Datasheet

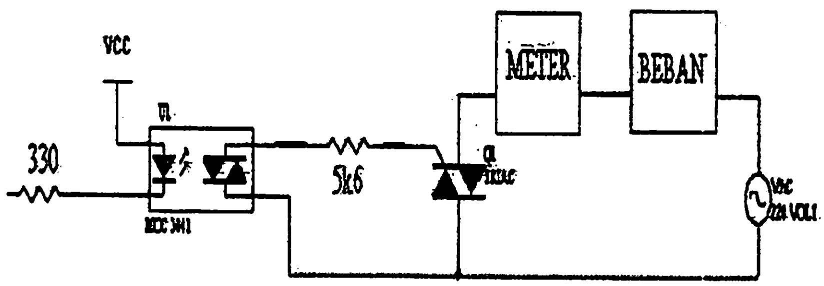
Pada gambar rangkaian LCD, pin-pin yang digunakan adalah :

- Pin 1, pin 2, dan pin 3 dihubungkan sebagai pengatur kontras tampilan.
- Pin 4 dihubungkan pada P1.1 mikrokontroler, digunakan sebagai perintah untuk memilih tulis atau kontrol LCD (hapus layer, ganti baris , dsb).
- Pin 5 dan pin 16 dihubungkan dengan ground.

- Pin 6 dihubungkan pada P1.0 mikrokontroler sebagai enable clock.
- Pin 7 sampai pin 14 dihubungkan pada P0.0 sampai P0.7 mikrokontroler sebagai input data dari mikrokontroler.
- Pin 15 dihubungkan dengan Vcc ± 5 Volt.

3.4. Rangkaian Driver Triac

Apabila mikrokontroler mengirimkan data logic nol maka optocoupler aktif sehingga memberi kontak pada G triac,maka triac tersebut akan melewatkan arus pada beban.



Gambar 3-5

Rangkaian Driver Triac

Sumber :Perencanaan

BAB IV

PENGUJIAN ALAT

Tujuan

Bab ini akan membahas tentang pengujian alat yang telah dirancang. Adapun tujuan dari pengujian ini adalah untuk mengetahui apakah hardware dan software dapat bekerja sesuai dengan kondisi yang diinginkan.

Untuk mengetahui kemampuan dan sistem kerja alat sesuai dengan program yang telah dibuat maka dilakukan pengujian pada alat dan sistem kerja alat, yang mana prosedur pengujian meliputi:

1. Pengujian Rangkaian LCD
2. Pengujian Rangkaian Optocoupler
3. Pengujian Rangkaian Driver
4. Pengujian Microkontroler.
5. Pengujian Pemakaian Pulsa.

4.1 Pengujian Rangkaian LCD

Pengujian rangkaian LCD berfungsi untuk mengetahui kemampuan rangkaian tampilan yang sudah dibuat apakah dapat mendukung sistem dengan baik sesuai dengan yang direncanakan untuk menampilkan data keluaran dari mikrokontroler ke LCD.

Peralatan yang digunakan :

- Power supply 12 volt.
- Mikrokontroler
- LCD

Langkah-langkah pengujian :

- Menyusun rangkaian seperti pada gambar dibawah :

Gambar 4.1

Blok pengujian rangkaian LCD

Sumber : *Perancangan*

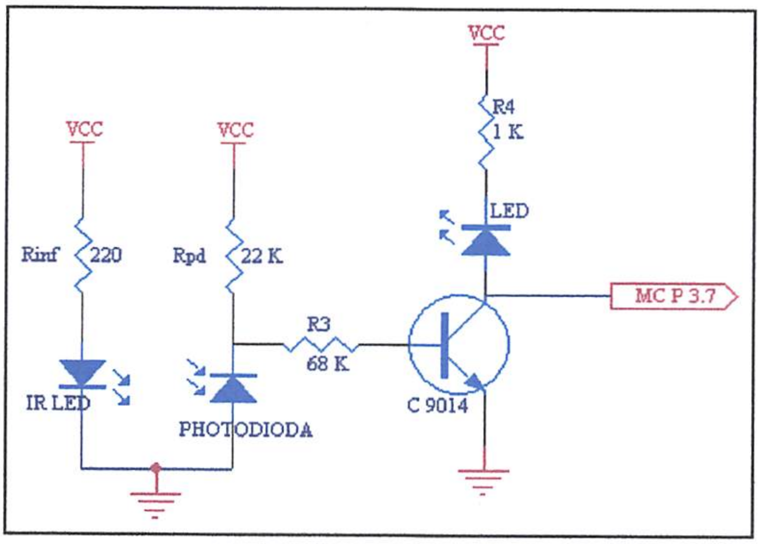
- Menjalankan program untuk menampilkan tulisan ke LCD.
- Mengamati keluaran pada LCD.

Hasil pengujian :

Hasil pengujian penyimpan data menunjukan data sebelum Power Supply dimatikan adalah 0000,026 dan setelah Power Supply dihidupkan lagi data yang tersimpan pada EEPROM yaitu 0000,026.

4.2. Pengujian Rangkaian Optocoupler

4.2.1. Pengujian Putaran Piringan Kwh Meter



Gambar 4.2

Rangkaian Optocoupler

Sumber :Datasheet

Tabel 4.1

Hasil Pengujian Sensor Optocoupler pada Lubang Piringan KWH

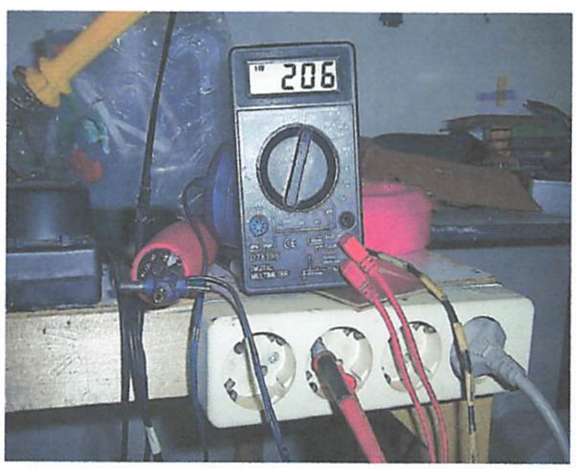
Putaran Piringan	Tampilan Led	Keluaran (volt)
Terhalang	**Nyala**	0,03
Tak Terhalang	**Mati**	4,66

Dari hasil pengujian didapat, pada saat cahaya inframerah menembus lubang pada piringan KWH maka indikator Led akan mati sedangkan tegangan yang dikeluarkan sebesar 4,66 Volt. Pada saat cahaya inframerah terhalang oleh piringan KWH maka indikator Led akan Nyala sedangkan tegangan yang dikeluarkan sebesar 0,03 Volt.

4.3. Pengujian *Driver*

Tujuan pengujian rangkaian *driver* adalah untuk mendapatkan tegangan keluaran dari *driver* tersebut, apakah mampu berfungsi untuk menghidupkan Triac sehingga pada meter dan beban terdapat arus yang mengalir. Dibawah ini gambar proses pengujian *driver*.

4.3.1. Pengujian Tegangan pada Sumber (PLN)



Gambar 4.3

Hasil Pengujian Tegangan pada Sumber (PLN)

Sumber : *Pengujian*

Pengujian tegangan pada sumber (PLN) didapat tegangan sebesar 206 Volt seperti yang tertera pada gambar 4.1 di atas.

piringan KWH maka indikator Led akan Nyala sedangkan tegangan yang dikeluarkan sebesar 0,03 Volt.

4.3. Pengujian *Driver*

Tujuan pengujian rangkaian *driver* adalah untuk mendapatkan tegangan keluaran dari *driver* tersebut, apakah mampu berfungsi untuk menghidupkan Triac sehingga pada meter dan beban terdapat arus yang mengalir. Dibawah ini gambar proses pengujian *driver*.

4.3.1. Pengujian Tegangan pada Sumber (PLN)

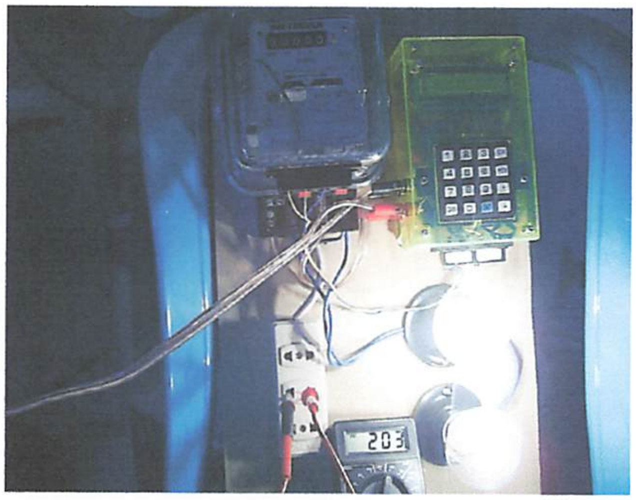
Gambar 4.3

Hasil Pengujian Tegangan pada Sumber (PLN)

Sumber : *Pengujian*

Pengujian tegangan pada sumber (PLN) didapat tegangan sebesar 206 Volt seperti yang tertera pada gambar 4.1 di atas.

4.3.2. Pengujian Tegangan pada Output Triac



Gambar 4.4

Hasil Pengujian Tegangan pada Output Triac

Sumber : *Pengujian*

Pengujian tegangan pada output triac didapat tegangan sebesar 203 Volt seperti yang tertera pada gambar 4.2

Tabel 4.2

Hasil Pengujian Tegangan Rangkaian Optocoupler

Tegangn pada Sumber (PLN)	Tegangan pada Output Triac
206 v	203 v

Pada pengujian ini terdapat perbedaan antara tegangan PLN dan tegangan Output Triac disebabkan tegangan input yang masuk ke Kwh meter sampai ke beban di pergunakan oleh Triac.

4.4. Pengujian Mikrokontroler

Tujuan pengujian Microkontroler adalah untuk mengetahui kerja Microkontroler dalam mengakses data masukan

Peralatan yang digunakan

- *PC (Personal computer).*
- Rangkaian yang sudah jadi.
- Kebel penghubung.

Langkah Pengujian

- Menghubungkan koneksi antara *softwere* komputer dengan MCU AT89S51.
- Mengaktifkan *power*.
- Memasukkan pin.

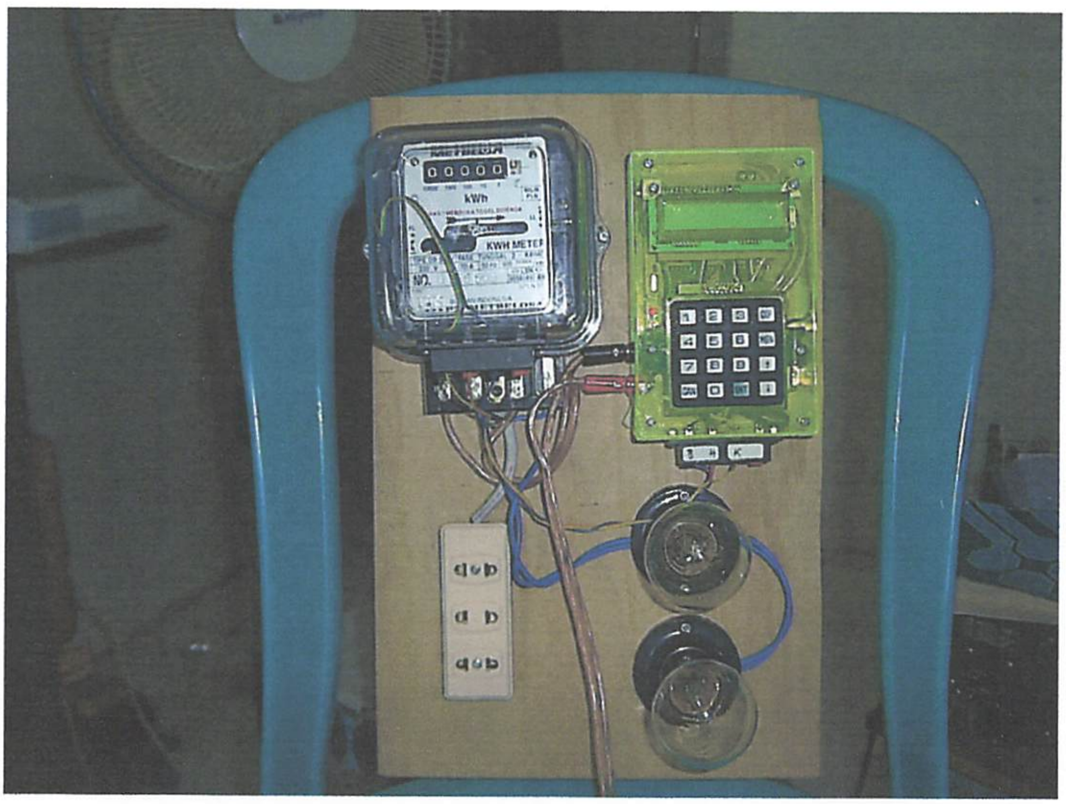
Hasil Pengujian

Hasil pengujian pin yang dimasukkan sesuai dengan yang direncanakan, jadi ini menandakan *softwere* yang dibuat sudah memenuhi ketentuan yang telah dibuat.

4.5. Pengujian Pemakaian Pulsa

Adapun langkah-langkah pengujiannya adalah sebagai berikut :

- Pertama-tama, dipastikan semua komponen telah terpasang dengan baik dan benar.
- Lampu 60 watt dan 100 watt sebagai simulasi beban, agar KWH meter dapat berputar.
- Blok rangkaian pengirim dan penerima diberi beban 5 Vol, lalu optocoupler dipasang pada simulasi KWH meter untuk membaca jumlah putarannya.



Gambar 4.5

Alat Secara Keseluruhan

Sumber : *Perencanaan*

4.5. Pengujian Pemakaian Pulsa

Adapun langkah-langkah pengujiannya adalah sebagai berikut :

- Pertama-tama, dipastikan semua komponen telah terpasang dengan baik dan benar.
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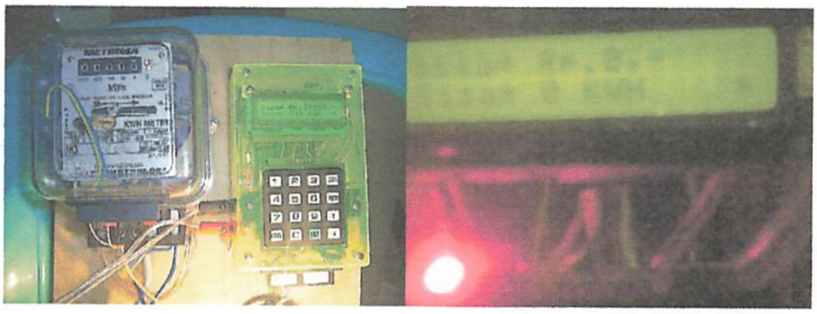
Gambar 4.5

Alat Secara Keseluruhan

Sumber : *Perencanaan*

Untuk dapat mengaktifkan Kwh meter dibutuhkan sepuluh nomor seri, berupa voucher. Apabila nomor seri tersebut sudah dipakai, maka tidak dapat dipergunakan lagi.



Gambar 4.6

Hasil Pengujian Pemakaian Pulsa

Sumber : *Pengujian*

Pulsa Rp 100,- rupiah dengan beben 650 Watt dapat dipakai selama 5 jam. Jika pulsa yang kita isi sebesar Rp 10.000,- dengan beban yang sama tanpa dimatikan, maka dapat dipakai selama 3 minggu.

Tabel 4.3

Hasil Pengujian Pemakaian Pulsa

Pulsa/Rp	**Beben**	**Jam/Hari**
Rp 100,-	650 Watt	5 jam
Rp 10.000,-	650 Watt	3 minggu

BAB V

KESIMPULAN

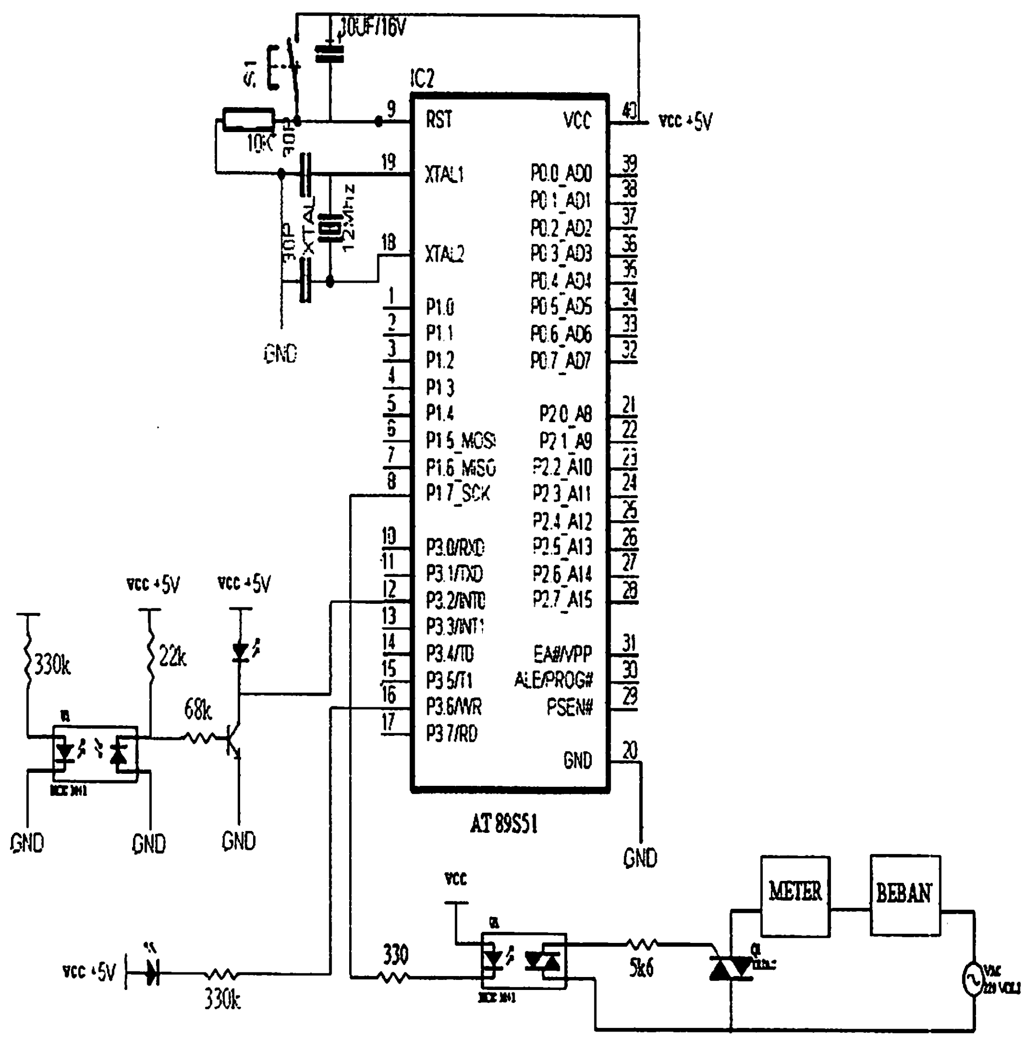
5.1. Kesimpulan

- Respon sistem sesuai dengan yang diharapkan, terbukti dengan besarnya tingkat keberhasilan pengisian dan pemakaian pulsa.
- Kesalahan yang terjadi dapat disebabkan karena harga komponen yang digunakan , maupun faktor kesalahan manusia yang terjadi dalam pengujian.

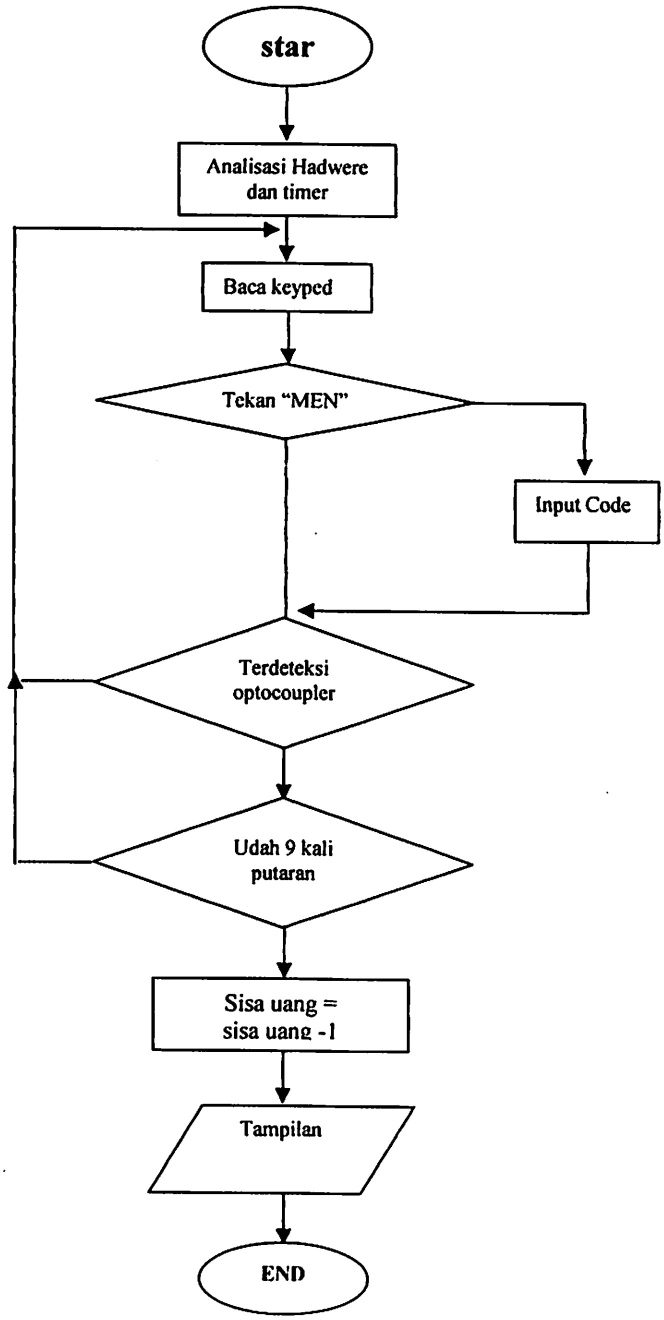
5.2. Saran

- Perhatikan masa aktif pulsa.
- Memakai komponen dengan kualitas lebih baik.
- Menambahkan jumlah pulsa agar pemakaiannya lebih lama.
- Membuat rangkaian penguat yang tepat agar dapat memperoleh hasil yang lebih baik.

Gambar Skematik Rangkaian



- Flow Chart


star
Analisasi Hadwere dan timer
Baca keyped
Tekan "MEN"
Input Code
Terdeteksi optocoupler
Udah 9 kali putaran
Sisa uang = sisa uang -1
Tampilan
END

Listing Program

```
#include <AT89x51.h>
#include "pending.c"
#include "LCDS1.c"

unsigned int ttek,sisa_duit,sisa_KWH,temp1,ttam;
unsigned char j_pulsa,i,j,keypresed,jum_kartu,jum_digit,jo;
unsigned char data_code[10],tmp_ID[10];
bit      sudahtek,EXIT,masukmenu,tondo,err_konfirmasi,pernah_hi,
         lamp_gate;

#include "key.c"


#define  pinMOC        P3_1


unsigned char  code MatrixCard[10][10] =
        {
        {'1','3','3','3','0','1','0','3','7','7'},
        {'1','8','0','5','7','7','0','6','7','7'},
        {'1','9','3','3','1','2','3','8','1','3'},
        {'1','3','3','9','5','6','5','1','0','4'},
        {'8','1','2','3','9','9','4','7','0','8'},
        {'5','2','3','9','5','0','8','1','9','4'},
        {'8','1','2','3','7','7','7','9','8','9'},
        {'5','2','3','9','8','0','3','7','0','0'},
        {'5','2','3','0','1','6','8','8','1','6'},
        {'1','3','8','7','3','6','5','3','1','1'},
        };
/*********************
prototype fungsi
*********************/
void init_hardware();
void tulisdigit(char digitnya,unsigned int dt);
void tampilan_sisa_duit();
void tampilan_sisa_KWH();
void nambah();
void confirmation();
void t_sisa();
void program_lampu();


void Ext_Int0 (void) interrupt 0
{
}
```

```
void cek_pin()
{

 if (!P3_2)
 {
  if (!masukmenu) Printxy(16,2,"*");
  if (!pernah_hi)
  {
   pernah_hi=1;
   j_pulsa++ ;
   if (j_pulsa >= 9)
   {
    j_pulsa=0;
    sisa_duit=sisa_duit-1;
   }
   t_sisa();
  }
 }
 else
 {
  pernah_hi=0;
 if (!masukmenu) Printxy(16,2," ");
 }
 if (sisa_duit==0) pinMOC=1;
}

void TimerInterrupt (void) interrupt 1 using 1
{
 TH0 = (-1000/256)-1;
 TL0 = (-1000%256)-1;
 cek_pin();
 ttek++;
 if (lamp_gate)
 {
  if (++ttam>200)
  {
   ttam=0;
   P3_7=!P3_7;
  }
 }
}
/*******************************************************************
***********/
/*              PROGRAM UTAMA                            */
/*******************************************************************
***********/
void main()
```

```
{
 Init_LCD();ClearLCD();init_hardware();
 sisa_duit=0;pinMOC=1;
 t_sisa();
 TulisRLCD(0x0C);
 while(1)
 {
  keypresed=inkey();
  if (keypresed=='M')
  {
   masukmenu=1;
   TulisRLCD(0x0E);
   nambah();
   TulisRLCD(0x0C);
   ClearLCD();
   t_sisa();
   masukmenu=0;
  }
  program_lampu();
  if (sisa_duit==0) pinMOC=1;
 }
}
/*****************************************************************
***********/


void init_hardware()
{
      EA  = 1                          ;//Aktifkan fasilitas semua interrupt
      TMOD =      0x01   ;//
      ET0  = 1                         ;//Aktifkan interupsi Timer 0
      TR0  = 1                         ;//Jalankan Timer 0
}

void tulisdigit(char digitnya,unsigned int dt)
{
 if (digitnya==2)
 {
  TulisDLCD(((dt/10)%10)|0x30);
  TulisDLCD((dt%10|0x30));
 }
 else if(digitnya==3)
 {
  TulisDLCD(((dt/100)%10)|0x30);
  TulisDLCD(((dt/10)%10)|0x30);
  TulisDLCD((dt%10|0x30));
 }
 else if(digitnya==4)
```

```
 {
  TulisDLCD(((dt/1000)%10)|0x30);
  TulisDLCD(((dt/100)%10)|0x30);
  TulisDLCD(((dt/10)%10)|0x30);
  TulisDLCD((dt%10|0x30));
 }
 else if(digitnya==5)
 {
  TulisDLCD((dt/10000)|0x30);
  TulisDLCD(((dt/1000)%10)|0x30);
  TulisDLCD(((dt/100)%10)|0x30);
  TulisDLCD(((dt/10)%10)|0x30);
  TulisDLCD((dt%10|0x30));
 }
 else
 {
  TulisDLCD((dt%10|0x30));
 }
}

void tampilan_sisa_duit()
{
 Printxy(1,1,"Sisa= Rp."); //tulisdigit(5,sisa_duit);
 if (sisa_duit>=10000) tulisdigit(5,sisa_duit);
 else if ((sisa_duit>=1000) && (sisa_duit<10000)) tulisdigit(4,sisa_duit);
 else if ((sisa_duit>=100) && (sisa_duit<1000)) tulisdigit(3,sisa_duit);
 else if ((sisa_duit>=10) && (sisa_duit<100)) tulisdigit(2,sisa_duit);
 else tulisdigit(1,sisa_duit);
 TulisDLCD(',');TulisDLCD('-');TulisDLCD(' ');
 TulisDLCD(' ');TulisDLCD(' ');TulisDLCD(' ');
 TulisDLCD(' ');TulisDLCD(' ');TulisDLCD(' ');TulisDLCD(' ');
}

void tampilan_sisa_KWH()
{
 sisa_KWH=sisa_duit/100;
 Printxy(1,2,"Sisa= ");
 if (sisa_KWH>=10000) tulisdigit(5,sisa_KWH);
 else if ((sisa_KWH>=1000) && (sisa_KWH<10000)) tulisdigit(4,sisa_KWH);
 else if ((sisa_KWH>=100) && (sisa_KWH<1000)) tulisdigit(3,sisa_KWH);
 else if ((sisa_KWH>=10) && (sisa_KWH<100)) tulisdigit(2,sisa_KWH);
 else tulisdigit(1,sisa_KWH);
 TulisDLCD(' ');TulisDLCD('K');TulisDLCD('W');TulisDLCD('H');
 TulisDLCD(' ');TulisDLCD(' ');TulisDLCD(' ');TulisDLCD(' ');
}

void LCD_input_NIK()
{
```

```
ClearLCD();
Printxy(1,1,"Code:");
Printxy(1,2,"CAN:Exit ENT:OK");
}

void nambah()
{
#define max_code  10

 masukmenu=1;
       for(j=0;j<7;j++)data_code[j] = ' ';
       LCD_input_NIK();
       i=0;
       EXIT=0;
       while(!EXIT)
       {
              keypresed = inkey();
              if(keypresed == 'N')
              {
                     EXIT = 1;
              }
              else if(keypresed == 'R')
              {
                     if (i != 0)
                     {
                            i--;
                            Gotoxy(i+7,1);TulisDLCD(' ');
                            Gotoxy(i+7,1);
                     }
              }
              else if(keypresed >= '0' && keypresed <= '9' && i<max_code)
              {
                     Gotoxy(i+7,1);TulisDLCD(keypresed);
                     data_code[i] = keypresed;
                     i++;
              }
              else if (keypresed == 'E')
              {
                     if (i < max_code)
                     {
    ClearLCD();
    Printxy(1,1,"Masukan Salah")   ;
    Tunda_mili(1000);
    LCD_input_NIK();
    i=0;
                     }
                     else
                     {
```

```
      confirmation();
      Tunda_mill(2000);
                                        EXIT=1;
                              }
                    }
                    else if (keypresed == 'C')
                    {
                     EXIT=1;
                    }
          }
}


void confirmation()
{
 tondo=0;
 err_konfirmasi=0;
 jum_kartu=0;
 while(!tondo)
 {

  if ((MatrixCard[jum_kartu][0] == data_code[0]) &&
     (MatrixCard[jum_kartu][1] == data_code[1]) &&
     (MatrixCard[jum_kartu][2] == data_code[2]) &&
     (MatrixCard[jum_kartu][3] == data_code[3]) &&
     (MatrixCard[jum_kartu][4] == data_code[4]) &&
     (MatrixCard[jum_kartu][5] == data_code[5]) &&
     (MatrixCard[jum_kartu][6] == data_code[6]) &&
     (MatrixCard[jum_kartu][7] == data_code[7]) &&
     (MatrixCard[jum_kartu][8] == data_code[8]) &&
     (MatrixCard[jum_kartu][9] == data_code[9])
     )
  {
   tondo=1;jo=jum_kartu;
  }
  jum_kartu++;
  if (jum_kartu==11)
  {
   tondo=1;err_konfirmasi=1;
  }
 }
 ClearLCD();

 if (!err_konfirmasi)
 {
  if (tmp_ID[jo]==0)
  {
   tmp_ID[jo]=1;
```

```
    if ((jo>=0) && (jo<=4)) sisa_duit=sisa_duit+10000;
    else if ((jo>4) && (jo<=7)) sisa_duit=sisa_duit+20000;
    else if ((jo>7) && (jo<=9)) sisa_duit=sisa_duit+35000;
    pinMOC=0;
    Printxy(1,1,"Kode Diterima");
   }
   else Printxy(1,1,"Kode Kadaluarsa");
  }
  else
  {
   Printxy(1,1,"Kode Ditolak");
  }
}

void t_sisa()
{
   tampilan_sisa_duit();
   tampilan_sisa_KWH();

}

void program_lampu()
{
  if (sisa_duit>500)
  {
   lamp_gate=0;
   P3_7=1;
  }
  else if ( (sisa_duit>0) && (sisa_duit<=500))
  {
   lamp_gate=1;
  }
  else if (sisa_duit==0)
  {
   lamp_gate=0;
   P3_7=0;
  }
}
```

DAFTAR PUSTAKA

1. Dr. Sapiie Soedjana – Dr. Nishino Osamu, "Pengukuran Dan Alat-alat Ukur Listrik"
2. Purnomo Hari Nanang, "Kwh Meter Sistem Kartu" 2004 (Peneliti Terdahulu)
3. Purnomo Hendro, "Kwh Meter Digital" 2003 (Peneliti Terdahulu)
4. Data Dan Persamaan Transistor, Penerbit PT.Elek Media Komputindo
5. *ATMEL AT89S51 Data Sheet*
6. *Module LCD M1632 User Manual*
7. *WWW.TEXAS INSTRUMENT Datasheet*
8. *WWW>FAIRCHILD SEMICONDUKTOR Datasheet*
9. *I/O BUS dan Motherboard*
10. *WWW.SENET.COM*

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FAKULTAS TEKNOLOGI INDUSTRI
JURUSAN TEKNIK ELEKTRO D-III

LEMBAR ASISTENSI BIMBINGAN TUGAS AKHIR

Nama : SYAHRURRAHMAN
Nim : 03.52.023
Waktu Bimbingan : 21/12/2006 s/d 21/04/2007
Judul : Perencanaan Dan Pembuatan Kwh Meter Sistem Kartu Prabayar

No	Tanggal	Materi	Paraf
	08/01/2007	Konsultasi Rangkaian Alat	
	20/01/2007	Revisi Bab I, II dan III	
	26/01/2007	ACC Bab I, II dan III	
	30/01/2007	Revisi Bab IV dan V	
	20/02/2007	ACC Bab IV dan V	
	27/02/2007	Pengujian Alat	
	28/02/2007	ACC Ujian	

Malang,07,01,2007

Mengetahui
Dosen Pembimbing

(Ir. Teguh Herbasuki, MT.)

INSTITUT TEKNOLOGI NASIONAL
FAKULTAS TEKNOLOGI INDUSTRI
JURUSAN TEKNIK ELEKTRO D-III
PROGRAM STUDI TEKNIK ENERGI LISRTIK
MALANG

BERITA ACARA UJIAN TUGAS AKHIR
FAKULTAS TEKNOLOGI INDUSTRI

Nama	: SYAHRURRAHMAN
NIM	: 03.52.032
Jurusan	: Teknik Elektro D-III
Konsentrasi	: Teknik Energi Listrik
Judul Tugas Akhir	: Perencanaan Dan Pembuatan Kwh Meter Sistem Kartu Prabayar.

Dipertahankan dihadapan Team penguji Tugas Akhir jenjang Diploma (D-III) pada :

Hari	: Rabu
Tanggal	: 21 Maret 2007
Dengan nilai	: 77,80 (B+)

Panitia Ujian Tugas Akhir

Ketua

Ir. Mochtar Asroni, MSME

Sekretaris

Ir. H Choirul Saleh, MT

Anggota Penguji

Penguji Pertama

Ir. Yunior Siahaan

Penguji Kedua

Ir. Djojo Priatmono, MT

INSTITUT TEKNOLOGI NASIONAL
FAKULTAS TEKNOLOGI INDUSTRI
JURUSAN TEKNIK ELEKTRO D-III
PROGRAM STUDI TEKNIK ENERGI LISTRIK
MALANG

LEMBAR PERBAIKAN TUGAS AKHIR

Telah dilakukan perbaikan oleh :

Nama : SYAHRURRAHMAN
NIM : 03.52.023
Jurusan : TEKNIK ELEKTRO D-III
Program Studi : ENERGI LISTRIK
Hari/Tanggal : Rabu/21 Maret 2007

No.	Materi Perbaikan	Paraf
1.	Contoh perhitungan untuk pembuktian bahwa jika pulsa Rp 100,- dengan beban 650 Watt berapakah waktunya.	[paraf]

Telah Diperiksa/Disetujui

Penguji I

Ir. Yunior Siahaan

Penguji II

Ir. Djojo Priatmono, MT

Mengetahui :
Dosen Pembimbing

Ir.Teguh Herbasuki, MT

INSTITUT TEKNOLOGI NASIONAL
FAKULTAS TEKNOLOGI INDUSTRI
JURUSAN TEKNIK ELEKTRO D-III
PROGRAM STUDI TEKNIK ENERGI LISRTIK
MALANG

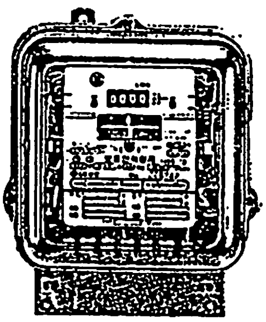
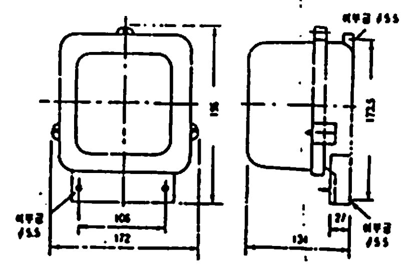
LEMBAR BIMBINGAN TUGAS AKHIR

Nama	: SYAHRURRAHMAN
NIM	: 03.52.032
Jurusan	: Teknik Elektro D-III
Program Studi	: Teknik Energi Listrik
Judul Skripsi	: Perencanaan Dan Pembuatan Kwh Meter Sistem Kartu Prabayar
Tanggal Pengajuan Tugas Ahkir	: 21 Desember 2006
Selesai Penulisan Tugas Ahkir	: 21 April 2007
Dosen Pembimbing	: Ir. Teguh Herbasuki, MT
Telah Dievaluasi Dengan Nilai	: 85

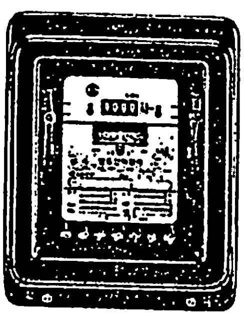
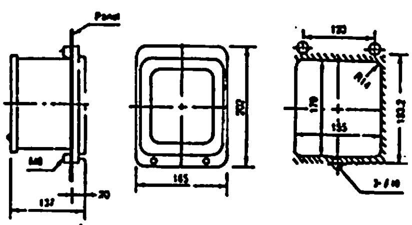
Mengetahui Ketua Jurusan Elektro D-III	Diperiksa dan disetujui Dosen Pembimbing
Ir. H Choirul Saleh, MT NIP.Y. 1010088190	Ir. Teguh Herbasuki, MT NIP.P. 1038900209

LAMPIRAN-LAMPIRAN

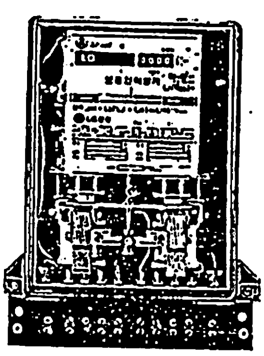
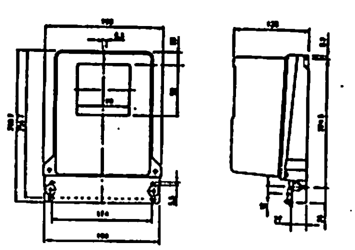
변성기부계기

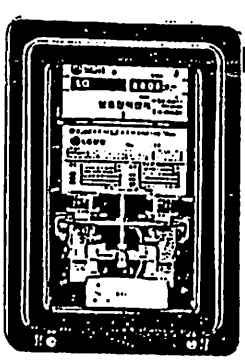
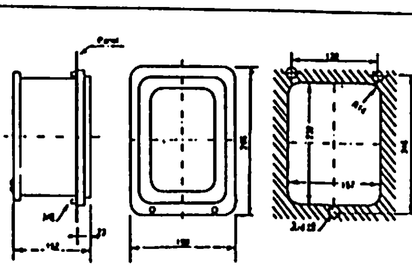
제품명	GF-72
상	3P-3W
전류(A)	5(2.5)
전압(V)	110, 220
부착방식	노출형
전력손실(VA)	5.2/4.1

제품명	GF-72Te
상	3P-3W
전류(A)	5(2.5)
전압(V)	110, 220
부착방식	매입형
전력손실(VA)	5.2/4.1

제품명	WL 42R
상	3P-4W
전류(A)	5(2.5)
전압(V)	110/190, 220/380
부착방식	노출형
전력손실(VA)	5.2/4.1

제품명	WL 42R Te
상	3P-4W
전류(A)	5(2.5)
전압(V)	110/190, 220/380
부착방식	매입형
전력손실(VA)	5.2/4.1

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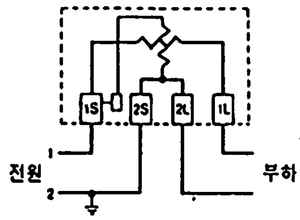
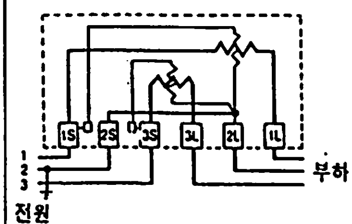
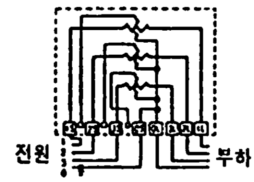
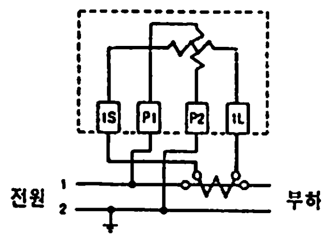
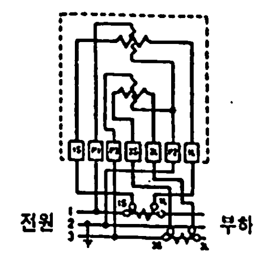
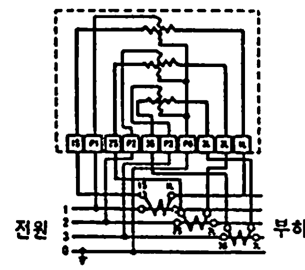
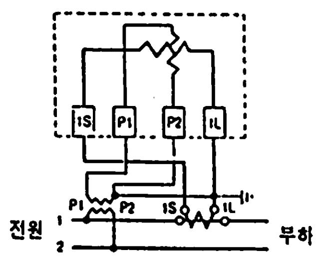
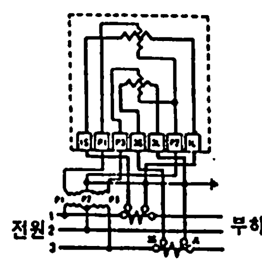
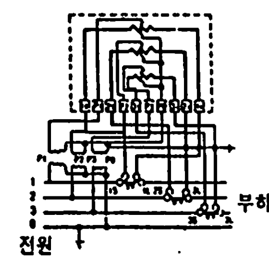
			
계기			
계기 (조합)			

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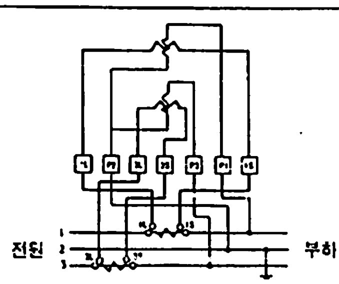
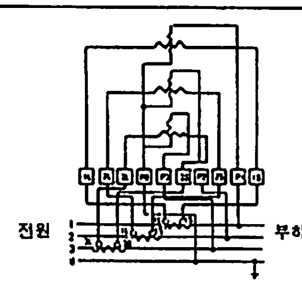
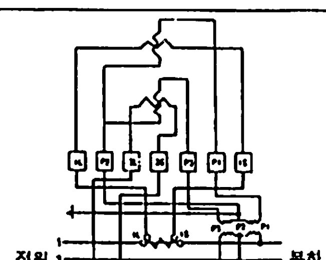
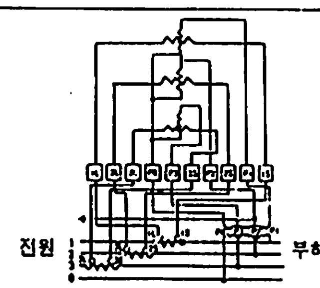
계기		
계기 (포함)		

eatures

- Compatible with MCS-51® Products
- 4K Bytes of In-System Programmable (ISP) Flash Memory
  - Endurance: 1000 Write/Erase Cycles
- 4.0V to 5.5V Operating Range
- Fully Static Operation: 0 Hz to 33 MHz
- Three-level Program Memory Lock
- 128 x 8-bit Internal RAM
- 32 Programmable I/O Lines
- Two 16-bit Timer/Counters
- Six Interrupt Sources
- Full Duplex UART Serial Channel
- Low-power Idle and Power-down Modes
- nterrupt Recovery from Power-down Mode
- Watchdog Timer
- Dual Data Pointer
- Power-off Flag
- Fast Programming Time
- Flexible ISP Programming (Byte and Page Mode)

escription

e AT89S51 is a low-power, high-performance CMOS 8-bit microcontroller with 4K tes of in-system programmable Flash memory. The device is manufactured using mel's high-density nonvolatile memory technology and is compatible with the indus--standard 80C51 instruction set and pinout. The on-chip Flash allows the program emory to be reprogrammed in-system or by a conventional nonvolatile memory pro-ammer. By combining a versatile 8-bit CPU with in-system programmable Flash on a onolithic chip, the Atmel AT89S51 is a powerful microcontroller which provides a ghly-flexible and cost-effective solution to many embedded control applications.

e AT89S51 provides the following standard features: 4K bytes of Flash, 128 bytes of AM, 32 I/O lines, Watchdog timer, two data pointers, two 16-bit timer/counters, a five-ctor two-level interrupt architecture, a full duplex serial port, on-chip oscillator, and ock circuitry. In addition, the AT89S51 is designed with static logic for operation wn to zero frequency and supports two software selectable power saving modes. e Idle Mode stops the CPU while allowing the RAM, timer/counters, serial port, and errupt system to continue functioning. The Power-down mode saves the RAM con-nts but freezes the oscillator, disabling all other chip functions until the next external errupt or hardware reset.

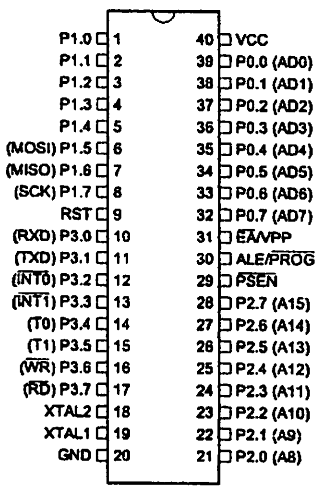
8-bit Microcontroller with 4K Bytes In-System Programmable Flash

AT89S51

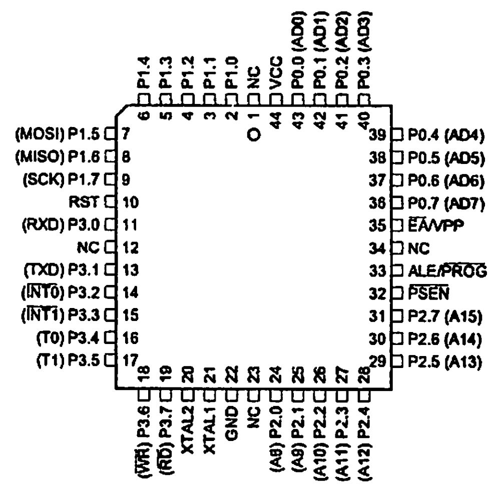
Rev. 2487A–10/01

n Configurations

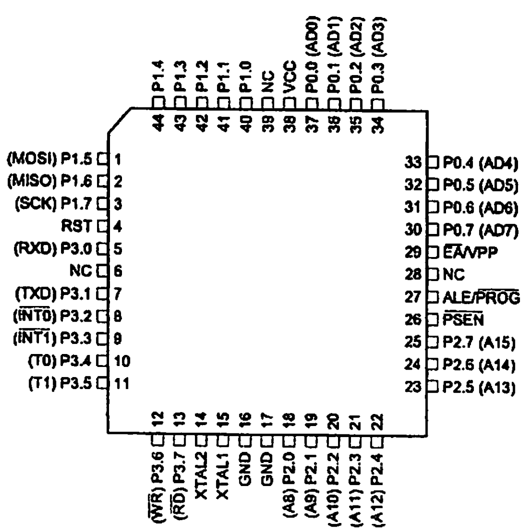
PDIP



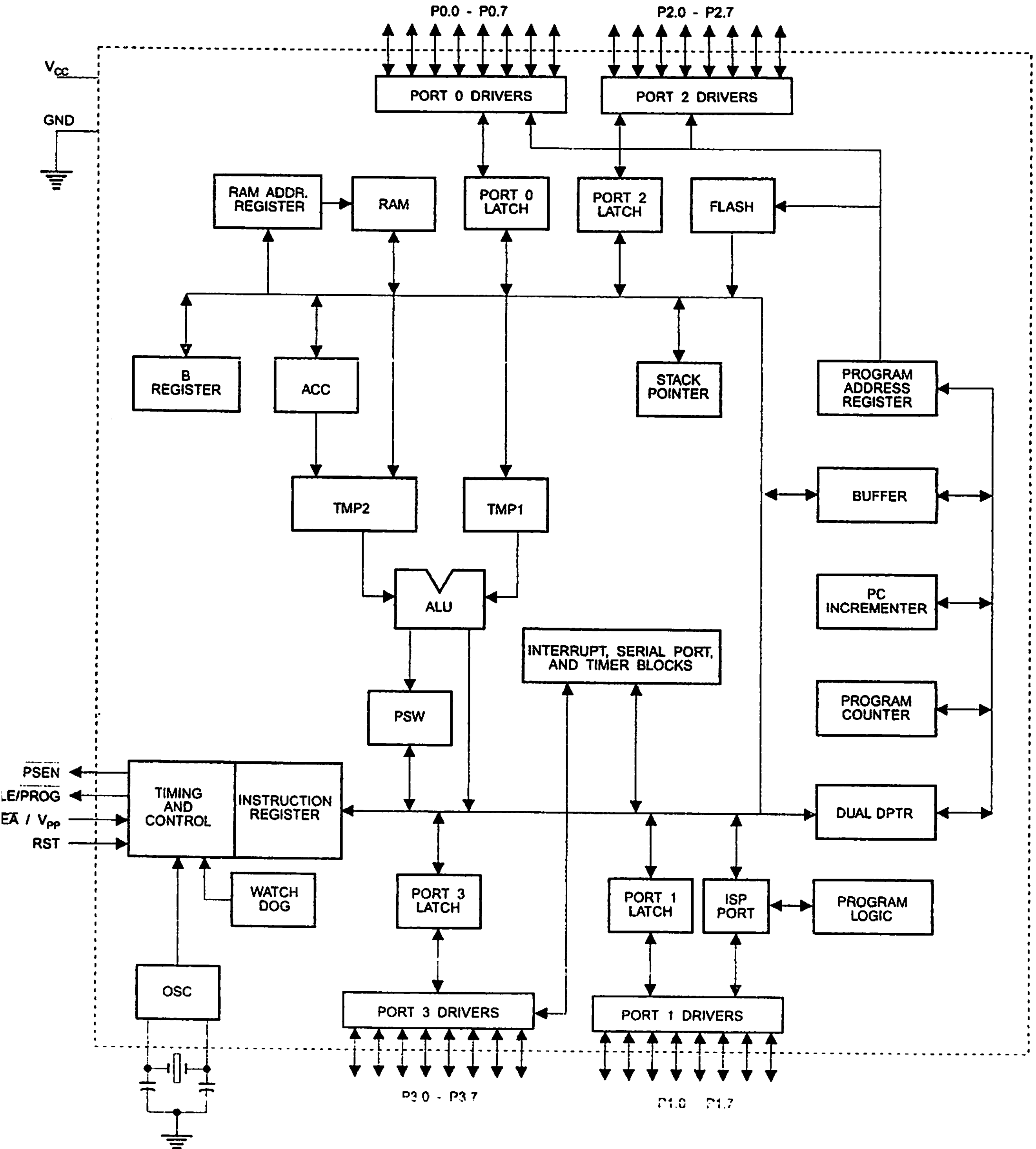
PLCC



TQFP



lock Diagram



n Description

:C

Supply voltage.

ND

Ground.

rt 0

Port 0 is an 8-bit open drain bidirectional I/O port. As an output port, each pin can sink eight TTL inputs. When 1s are written to port 0 pins, the pins can be used as high-impedance inputs.

Port 0 can also be configured to be the multiplexed low-order address/data bus during accesses to external program and data memory. In this mode, P0 has internal pull-ups.

Port 0 also receives the code bytes during Flash programming and outputs the code bytes during program verification. **External pull-ups are required during program verification.**

rt 1

Port 1 is an 8-bit bidirectional I/O port with internal pull-ups. The Port 1 output buffers can sink/source four TTL inputs. When 1s are written to Port 1 pins, they are pulled high by the internal pull-ups and can be used as inputs. As inputs, Port 1 pins that are externally being pulled low will source current (I_{IL}) because of the internal pull-ups.

Port 1 also receives the low-order address bytes during Flash programming and verification.

Port Pin	Alternate Functions
P1.5	MOSI (used for In-System Programming)
P1.6	MISO (used for In-System Programming)
P1.7	SCK (used for In-System Programming)

rt 2

Port 2 is an 8-bit bidirectional I/O port with internal pull-ups. The Port 2 output buffers can sink/source four TTL inputs. When 1s are written to Port 2 pins, they are pulled high by the internal pull-ups and can be used as inputs. As inputs, Port 2 pins that are externally being pulled low will source current (I_{IL}) because of the internal pull-ups.

Port 2 emits the high-order address byte during fetches from external program memory and during accesses to external data memory that use 16-bit addresses (MOVX @ DPTR). In this application, Port 2 uses strong internal pull-ups when emitting 1s. During accesses to external data memory that use 8-bit addresses (MOVX @ RI), Port 2 emits the contents of the P2 Special Function Register.

Port 2 also receives the high-order address bits and some control signals during Flash programming and verification.

rt 3

Port 3 is an 8-bit bidirectional I/O port with internal pull-ups. The Port 3 output buffers can sink/source four TTL inputs. When 1s are written to Port 3 pins, they are pulled high by the internal pull-ups and can be used as inputs. As inputs, Port 3 pins that are externally being pulled low will source current (I_{IL}) because of the pull-ups.

Port 3 receives some control signals for Flash programming and verification.

Port 3 also serves the functions of various special features of the AT89S51, as shown in the following table.

Port Pin	Alternate Functions
P3.0	RXD (serial input port)
P3.1	TXD (serial output port)
P3.2	$\overline{INT0}$ (external interrupt 0)
P3.3	$\overline{INT1}$ (external interrupt 1)
P3.4	T0 (timer 0 external input)
P3.5	T1 (timer 1 external input)
P3.6	$\overline{WR}$ (external data memory write strobe)
P3.7	$\overline{RD}$ (external data memory read strobe)

ST

Reset input. A high on this pin for two machine cycles while the oscillator is running resets the device. This pin drives High for 98 oscillator periods after the Watchdog times out. The DISRTO bit in SFR AUXR (address 8EH) can be used to disable this feature. In the default state of bit DISRTO, the RESET HIGH out feature is enabled.

.E/$\overline{PROG}$

Address Latch Enable (ALE) is an output pulse for latching the low byte of the address during accesses to external memory. This pin is also the program pulse input ($\overline{PROG}$) during Flash programming.

In normal operation, ALE is emitted at a constant rate of 1/6 the oscillator frequency and may be used for external timing or clocking purposes. Note, however, that one ALE pulse is skipped during each access to external data memory.

If desired, ALE operation can be disabled by setting bit 0 of SFR location 8EH. With the bit set, ALE is active only during a MOVX or MOVC instruction. Otherwise, the pin is weakly pulled high. Setting the ALE-disable bit has no effect if the microcontroller is in external execution mode.

$\overline{EN}$

Program Store Enable ($\overline{PSEN}$) is the read strobe to external program memory.

When the AT89S51 is executing code from external program memory, $\overline{PSEN}$ is activated twice each machine cycle, except that two $\overline{PSEN}$ activations are skipped during each access to external data memory.

$\overline{\ }$/VPP

External Access Enable. $\overline{EA}$ must be strapped to GND in order to enable the device to fetch code from external program memory locations starting at 0000H up to FFFFH. Note, however, that if lock bit 1 is programmed, $\overline{EA}$ will be internally latched on reset.

$\overline{EA}$ should be strapped to V_{CC} for internal program executions.

This pin also receives the 12-volt programming enable voltage (V_{PP}) during Flash programming.

'AL1

Input to the inverting oscillator amplifier and input to the internal clock operating circuit.

'AL2

Output from the inverting oscillator amplifier

pecial unction egisters

A map of the on-chip memory area called the Special Function Register (SFR) space is shown in Table 1.

Note that not all of the addresses are occupied, and unoccupied addresses may not be implemented on the chip. Read accesses to these addresses will in general return random data, and write accesses will have an indeterminate effect.

ble 1. AT89S51 SFR Map and Reset Values

0F8H									0FFH
0F0H	B 00000000								0F7H
0E8H									0EFH
0E0H	ACC 00000000								0E7H
0D8H									0DFH
0D0H	PSW 00000000								0D7H
0C8H									0CFH
0C0H									0C7H
0B8H	IP XX000000								0BFH
0B0H	P3 11111111								0B7H
0A8H	IE 0X000000								0AFH
0A0H	P2 11111111		AUXR1 XXXXXXX0				WDTRST XXXXXXXX		0A7H
98H	SCON 00000000	SBUF XXXXXXXX							9FH
90H	P1 11111111								97H
88H	TCON 00000000	TMOD 00000000	TL0 00000000	TL1 00000000	TH0 00000000	TH1 00000000	AUXR XXX00XX0		8FH
80H	P0 11111111	SP 00000111	DP0L 00000000	DP0H 00000000	DP1L 00000000	DP1H 00000000		PCON 0XXX0000	87H

User software should not write 1s to these unlisted locations, since they may be used in future products to invoke new features. In that case, the reset or inactive values of the new bits will always be 0.

Interrupt Registers: The individual interrupt enable bits are in the IE register. Two priorities can be set for each of the five interrupt sources in the IP register.

Table 2. AUXR: Auxiliary Register

AUXR Address = 8EH Reset Value = XXX00XX0B

Not Bit Addressable

	–	–	–	WDIDLE	DISRTO	–	–	DISALE
Bit	7	6	5	4	3	2	1	0

–	Reserved for future expansion
DISALE	Disable/Enable ALE
	DISALE Operating Mode
	0 ALE is emitted at a constant rate of 1/6 the oscillator frequency
	1 ALE is active only during a MOVX or MOVC instruction
DISRTO	Disable/Enable Reset out
	DISRTO
	0 Reset pin is driven High after WDT times out
	1 Reset pin is input only
WDIDLE	Disable/Enable WDT in IDLE mode
WDIDLE	
0	WDT continues to count in IDLE mode
1	WDT halts counting in IDLE mode

Dual Data Pointer Registers: To facilitate accessing both internal and external data memory, two banks of 16-bit Data Pointer Registers are provided: DP0 at SFR address locations 82H-83H and DP1 at 84H-85H. Bit DPS = 0 in SFR AUXR1 selects DP0 and DPS = 1 selects DP1. The user should always initialize the DPS bit to the appropriate value before accessing the respective Data Pointer Register.

Power Off Flag: The Power Off Flag (POF) is located at bit 4 (PCON.4) in the PCON SFR. POF is set to "1" during power up. It can be set and rest under software control and is not affected by reset.

Table 3. AUXR1: Auxiliary Register 1

AUXR1
Address = A2H

Reset Value = XXXXXXX0B

Not Bit Addressable

	–	–	–	–	–	–	–	DPS
Bit	7	6	5	4	3	2	1	0

–	Reserved for future expansion	
DPS	Data Pointer Register Select	
	DPS	
	0	Selects DPTR Registers DP0L, DP0H
	1	Selects DPTR Registers DP1L, DP1H

emory 'ganization

MCS-51 devices have a separate address space for Program and Data Memory. Up to 64K bytes each of external Program and Data Memory can be addressed.

ogram Memory

If the $\overline{EA}$ pin is connected to GND, all program fetches are directed to external memory.

On the AT89S51, if $\overline{EA}$ is connected to V_{CC}, program fetches to addresses 0000H through FFFH are directed to internal memory and fetches to addresses 1000H through FFFFH are directed to external memory.

ıta Memory

The AT89S51 implements 128 bytes of on-chip RAM. The 128 bytes are accessible via direct and indirect addressing modes. Stack operations are examples of indirect addressing, so the 128 bytes of data RAM are available as stack space.

atchdog mer 'ne-time ıabled with ɛset-out)

The WDT is intended as a recovery method in situations where the CPU may be subjected to software upsets. The WDT consists of a 14-bit counter and the Watchdog Timer Reset (WDTRST) SFR. The WDT is defaulted to disable from exiting reset. To enable the WDT, a user must write 01EH and 0E1H in sequence to the WDTRST register (SFR location 0A6H). When the WDT is enabled, it will increment every machine cycle while the oscillator is running. The WDT timeout period is dependent on the external clock frequency. There is no way to disable the WDT except through reset (either hardware reset or WDT overflow reset). When WDT overflows, it will drive an output RESET HIGH pulse at the RST pin.

;ing the WDT

To enable the WDT, a user must write 01EH and 0E1H in sequence to the WDTRST register (SFR location 0A6H). When the WDT is enabled, the user needs to service it by writing 01EH and 0E1H to WDTRST to avoid a WDT overflow. The 14-bit counter overflows when it reaches 16383 (3FFFH), and this will reset the device. When the WDT is enabled, it will increment every machine cycle while the oscillator is running. This means the user must reset the WDT at least every 16383 machine cycles. To reset the WDT the user must write 01EH and 0E1H to WDTRST. WDTRST is a write-only register. The WDT counter cannot be read or written. When WDT overflows, it will generate an output RESET pulse at the RST pin. The RESET pulse duration is 98xTOSC, where TOSC=1/FOSC. To make the best use of the WDT, it should be serviced in those sections of code that will periodically be executed within the time required to prevent a WDT reset.

DT During ›wer-down ıd Idle

In Power-down mode the oscillator stops, which means the WDT also stops. While in Power-down mode, the user does not need to service the WDT. There are two methods of exiting Power-down mode: by a hardware reset or via a level-activated external interrupt, which is enabled prior to entering Power-down mode. When Power-down is exited with hardware reset, servicing the WDT should occur as it normally does whenever the AT89S51 is reset. Exiting Power-down with an interrupt is significantly different. The interrupt is held low long enough for the oscillator to stabilize. When the interrupt is brought high, the interrupt is serviced. To prevent the WDT from resetting the device while the interrupt pin is held low, the WDT is not started until the interrupt is pulled high. It is suggested that the WDT be reset during the interrupt service for the interrupt used to exit Power-down mode.

To ensure that the WDT does not overflow within a few states of exiting Power-down, it is best to reset the WDT just before entering Power-down mode.

Before going into the IDLE mode, the WDIDLE bit in SFR AUXR is used to determine whether the WDT continues to count if enabled. The WDT keeps counting during IDLE (WDIDLE bit = 0) as the default state. To prevent the WDT from resetting the AT89S51 while in IDLE mode, the user should always set up a timer that will periodically exit IDLE, service the WDT, and reenter IDLE mode.

With WDIDLE bit enabled, the WDT will stop to count in IDLE mode and resumes the count upon exit from IDLE.

ᴬRT

The UART in the AT89S51 operates the same way as the UART in the AT89C51. For further information on the UART operation, refer to the ATMEL Web site (http://www.atmel.com). From the home page, select 'Products', then '8051-Architecture Flash Microcontroller', then 'Product Overview'.

mer 0 and 1

Timer 0 and Timer 1 in the AT89S51 operate the same way as Timer 0 and Timer 1 in the AT89C51. For further information on the timers' operation, refer to the ATMEL Web site (http://www.atmel.com). From the home page, select 'Products', then '8051-Architecture Flash Microcontroller', then 'Product Overview'.

terrupts

The AT89S51 has a total of five interrupt vectors: two external interrupts ($\overline{INT0}$ and $\overline{INT1}$), two timer interrupts (Timers 0 and 1), and the serial port interrupt. These interrupts are all shown in Figure 1.

Each of these interrupt sources can be individually enabled or disabled by setting or clearing a bit in Special Function Register IE. IE also contains a global disable bit, EA, which disables all interrupts at once.

Note that Table 4 shows that bit position IE.6 is unimplemented. In the AT89S51, bit position IE.5 is also unimplemented. User software should not write 1s to these bit positions, since they may be used in future AT89 products.

The Timer 0 and Timer 1 flags, TF0 and TF1, are set at S5P2 of the cycle in which the timers overflow. The values are then polled by the circuitry in the next cycle

Table 4. Interrupt Enable (IE) Register

(MSB) (LSB)

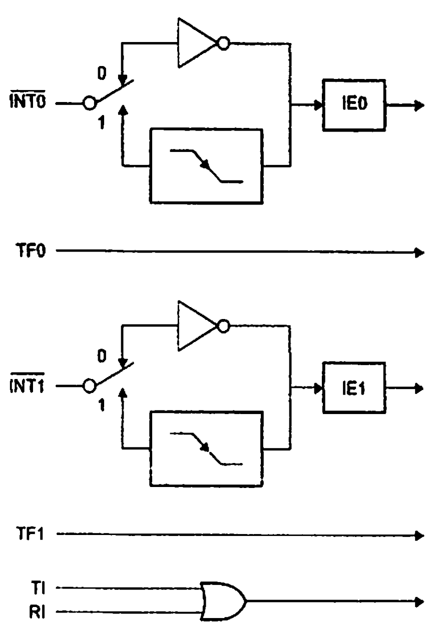
EA	–	–	ES	ET1	EX1	ET0	EX0

Enable Bit = 1 enables the interrupt.

Enable Bit = 0 disables the interrupt.

Symbol	Position	Function
EA	IE.7	Disables all interrupts. If EA = 0, no interrupt is acknowledged. If EA = 1, each interrupt source is individually enabled or disabled by setting or clearing its enable bit.
–	IE.6	Reserved
–	IE.5	Reserved
ES	IE.4	Serial Port interrupt enable bit
ET1	IE.3	Timer 1 interrupt enable bit
EX1	IE.2	External interrupt 1 enable bit
ET0	IE.1	Timer 0 interrupt enable bit
EX0	IE.0	External interrupt 0 enable bit
User software should never write 1s to reserved bits, because they may be used in future AT89 products.		

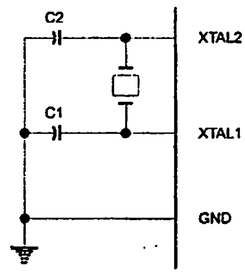
Figure 1. Interrupt Sources



Oscillator Characteristics

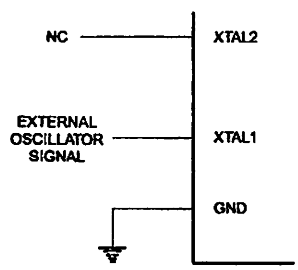
XTAL1 and XTAL2 are the input and output, respectively, of an inverting amplifier that can be configured for use as an on-chip oscillator, as shown in Figure 2. Either a quartz crystal or ceramic resonator may be used. To drive the device from an external clock source, XTAL2 should be left unconnected while XTAL1 is driven, as shown in Figure 3. There are no requirements on the duty cycle of the external clock signal, since the input to the internal clocking circuitry is through a divide-by-two flip-flop, but minimum and maximum voltage high and low time specifications must be observed.

Figure 2. Oscillator Connections



Note: C1, C2 = 30 pF ± 10 pF for Crystals = 40 pF ± 10 pF for Ceramic Resonators

Figure 3. External Clock Drive Configuration



Idle Mode

In idle mode, the CPU puts itself to sleep while all the on-chip peripherals remain active. The mode is invoked by software. The content of the on-chip RAM and all the special function registers remain unchanged during this mode. The idle mode can be terminated by any enabled interrupt or by a hardware reset.

Note that when idle mode is terminated by a hardware reset, the device normally resumes program execution from where it left off, up to two machine cycles before the internal reset algorithm takes control. On-chip hardware inhibits access to internal RAM in this event, but access to the port pins is not inhibited. To eliminate the possibility of an unexpected write to a port pin when idle mode is terminated by a reset, the instruction following the one that invokes idle mode should not write to a port pin or to external memory.

Power-down Mode

In the Power-down mode, the oscillator is stopped, and the instruction that invokes Power-down is the last instruction executed. The on-chip RAM and Special Function Registers retain their values until the Power-down mode is terminated. Exit from Power-down mode can be initiated either by a hardware reset or by activation of an enabled external interrupt into $\overline{INT0}$ or $\overline{INT1}$. Reset redefines the SFRs but does not change the on-chip RAM. The reset should not be activated before V_{CC} is restored to its normal operating level and must be held active long enough to allow the oscillator to restart and stabilize.

Table 5. Status of External Pins During Idle and Power-down Modes

Mode	Program Memory	ALE	$\overline{PSEN}$	PORT0	PORT1	PORT2	PORT3
Idle	Internal	1	1	Data	Data	Data	Data
Idle	External	1	1	Float	Data	Address	Data
Power-down	Internal	0	0	Data	Data	Data	Data
Power-down	External	0	0	Float	Data	Data	Data

ogram emory Lock ts

The AT89S51 has three lock bits that can be left unprogrammed (U) or can be programmed (P) to obtain the additional features listed in the following table.

Table 6. Lock Bit Protection Modes

Program Lock Bits				
	LB1	LB2	LB3	Protection Type
1	U	U	U	No program lock features
2	P	U	U	MOVC instructions executed from external program memory are disabled from fetching code bytes from internal memory, $\overline{EA}$ is sampled and latched on reset, and further programming of the Flash memory is disabled
3	P	P	U	Same as mode 2, but verify is also disabled
4	P	P	P	Same as mode 3, but external execution is also disabled

When lock bit 1 is programmed, the logic level at the $\overline{EA}$ pin is sampled and latched during reset. If the device is powered up without a reset, the latch initializes to a random value and holds that value until reset is activated. The latched value of $\overline{EA}$ must agree with the current logic level at that pin in order for the device to function properly.

ogramming e Flash – ırallel Mode

The AT89S51 is shipped with the on-chip Flash memory array ready to be programmed. The programming interface needs a high-voltage (12-volt) program enable signal and is compatible with conventional third-party Flash or EPROM programmers.

The AT89S51 code memory array is programmed byte-by-byte.

Programming Algorithm: Before programming the AT89S51, the address, data, and control signals should be set up according to the Flash programming mode table and Figures 13 and 14. To program the AT89S51, take the following steps:

1. Input the desired memory location on the address lines.
2. Input the appropriate data byte on the data lines.
3. Activate the correct combination of control signals.
4. Raise $\overline{EA}/V_{PP}$ to 12V.
5. Pulse ALE/$\overline{PROG}$ once to program a byte in the Flash array or the lock bits. The byte-write cycle is self-timed and typically takes no more than 50 µs. Repeat steps 1 through 5, changing the address and data for the entire array or until the end of the object file is reached.

$\overline{\text{Data}}$ Polling: The AT89S51 features $\overline{\text{Data}}$ Polling to indicate the end of a byte write cycle. During a write cycle, an attempted read of the last byte written will result in the complement of the written data on P0.7. Once the write cycle has been completed, true data is valid on all outputs, and the next cycle may begin. $\overline{\text{Data}}$ Polling may begin any time after a write cycle has been initiated.

Ready/$\overline{\text{Busy}}$: The progress of byte programming can also be monitored by the RDY/$\overline{\text{BSY}}$ output signal. P3.0 is pulled low after ALE goes high during programming to indicate $\overline{\text{BUSY}}$. P3.0 is pulled high again when programming is done to indicate READY.

Program Verify: If lock bits LB1 and LB2 have not been programmed, the programmed code data can be read back via the address and data lines for verification. The status of the individual lock bits can be verified directly by reading them back.

Reading the Signature Bytes: The signature bytes are read by the same procedure as a normal verification of locations 000H, 100H, and 200H, except that P3.6 and P3.7 must be pulled to a logic low. The values returned are as follows.

(000H) = 1EH indicates manufactured by Atmel
(100H) = 51H indicates 89S51
(200H) = 06H

Chip Erase: In the parallel programming mode, a chip erase operation is initiated by using the proper combination of control signals and by pulsing ALE/$\overline{\text{PROG}}$ low for a duration of 200 ns - 500 ns.

In the serial programming mode, a chip erase operation is initiated by issuing the Chip Erase instruction. In this mode, chip erase is self-timed and takes about 500 ms.

During chip erase, a serial read from any address location will return 00H at the data output.

ogramming e Flash – rial Mode

The Code memory array can be programmed using the serial ISP interface while RST is pulled to V_{CC}. The serial interface consists of pins SCK, MOSI (input) and MISO (output). After RST is set high, the Programming Enable instruction needs to be executed first before other operations can be executed. Before a reprogramming sequence can occur, a Chip Erase operation is required.

The Chip Erase operation turns the content of every memory location in the Code array into FFH.

Either an external system clock can be supplied at pin XTAL1 or a crystal needs to be connected across pins XTAL1 and XTAL2. The maximum serial clock (SCK) frequency should be less than 1/16 of the crystal frequency. With a 33 MHz oscillator clock, the maximum SCK frequency is 2 MHz.

rial ogramming jorithm

To program and verify the AT89S51 in the serial programming mode, the following sequence is recommended:

1. Power-up sequence:

   Apply power between VCC and GND pins.

   Set RST pin to "H".

   If a crystal is not connected across pins XTAL1 and XTAL2, apply a 3 MHz to 33 MHz clock to XTAL1 pin and wait for at least 10 milliseconds.
2. Enable serial programming by sending the Programming Enable serial instruction to pin MOSI/P1.5. The frequency of the shift clock supplied at pin SCK/P1.7 needs to be less than the CPU clock at XTAL1 divided by 16.
3. The Code array is programmed one byte at a time in either the Byte or Page mode. The write cycle is self-timed and typically takes less than 0.5 ms at 5V.
4. Any memory location can be verified by using the Read instruction that returns the content at the selected address at serial output MISO/P1.6.
5. At the end of a programming session, RST can be set low to commence normal device operation.

Power-off sequence (if needed):

Set XTAL1 to "L" (if a crystal is not used).

Set RST to "L".

Turn V_{CC} power off.

$\overline{\text{Data}}$ Polling: The $\overline{\text{Data}}$ Polling feature is also available in the serial mode. In this mode, during a write cycle an attempted read of the last byte written will result in the complement of the MSB of the serial output byte on MISO.

erial ogramming struction Set

The Instruction Set for Serial Programming follows a 4-byte protocol and is shown in Table 8 on page 18.

rogramming terface – arallel Mode

Every code byte in the Flash array can be programmed by using the appropriate combination of control signals. The write operation cycle is self-timed and once initiated, will automatically time itself to completion.

All major programming vendors offer worldwide support for the Atmel microcontroller series. Please contact your local programming vendor for the appropriate software revision.

ble 7. Flash Programming Modes

ode	V_{CC}	RST	$\overline{\text{PSEN}}$	ALE/ $\overline{\text{PROG}}$	$\overline{\text{EA}}$/ V_{PP}	P2.6	P2.7	P3.3	P3.6	P3.7	P0.7-0 Data	P2.3-0 Address	P1.7-0 Address
rite Code Data	5V	H	L	─╲_╱─ (2)	12V	L	H	H	H	H	D_{IN}	A11-8	A7-0
ead Code Data	5V	H	L	H	H	L	L	L	H	H	D_{OUT}	A11-8	A7-0
rite Lock Bit 1	5V	H	L	─╲_╱─ (3)	12V	H	H	H	H	H	X	X	X
rite Lock Bit 2	5V	H	L	─╲_╱─ (3)	12V	H	H	H	L	L	X	X	X
rite Lock Bit 3	5V	H	L	─╲_╱─ (3)	12V	H	L	H	H	L	X	X	X
ead Lock Bits 2, 3	5V	H	L	H	H	H	H	L	H	L	P0.2, P0.3, P0.4	X	X
hip Erase	5V	H	L	─╲_╱─ (1)	12V	H	L	H	L	L	X	X	X
ead Atmel ID	5V	H	L	H	H	L	L	L	L	L	1EH	0000	00H
ead Device ID	5V	H	L	H	H	L	L	L	L	L	51H	0001	00H
ead Device ID	5V	H	L	H	H	L	L	L	L	L	06H	0010	00H

tes:
1. Each $\overline{\text{PROG}}$ pulse is 200 ns - 500 ns for Chip Erase.
2. Each $\overline{\text{PROG}}$ pulse is 200 ns - 500 ns for Write Code Data.
3. Each $\overline{\text{PROG}}$ pulse is 200 ns - 500 ns for Write Lock Bits.
4. RDY/$\overline{\text{BSY}}$ signal is output on P3.0 during programming.
5. X = don't care.

Figure 4. Programming the Flash Memory (Parallel Mode)

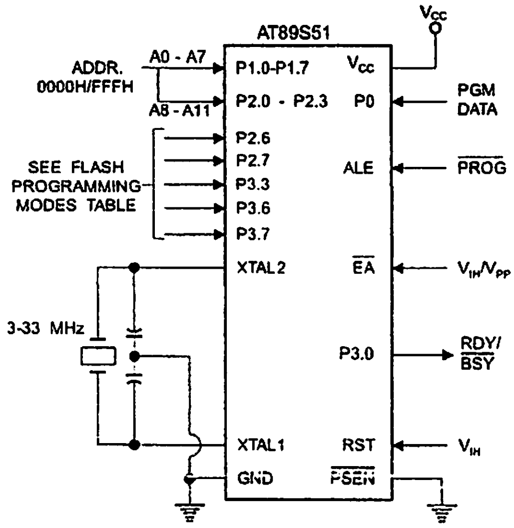
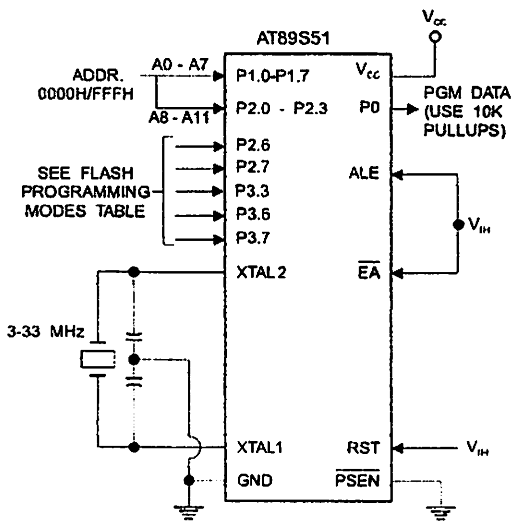


Figure 5. Verifying the Flash Memory (Parallel Mode)

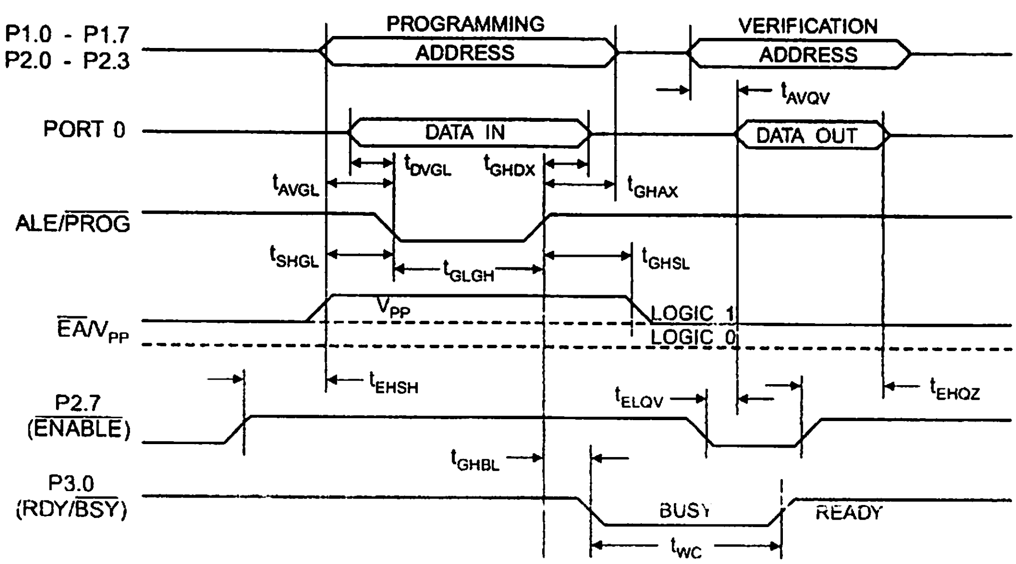


ash Programming and Verification Characteristics (Parallel Mode)

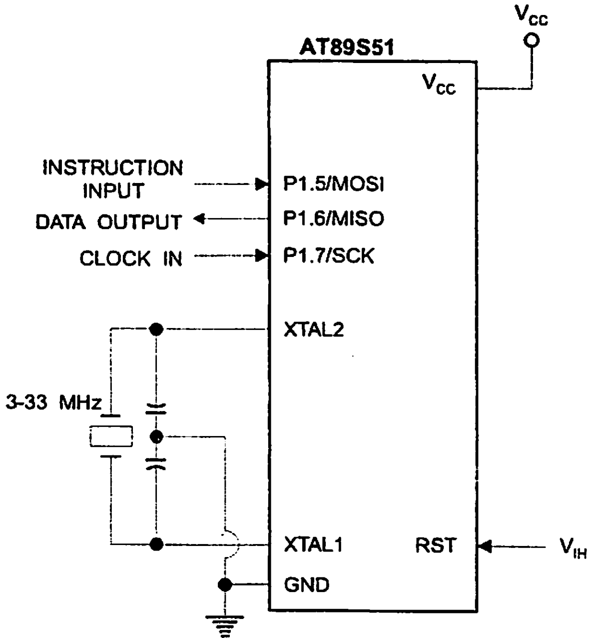
= 20°C to 30°C, V_{CC} = 4.5 to 5.5V

ymbol	Parameter	Min	Max	Units
$_{PP}$	Programming Supply Voltage	11.5	12.5	V
P	Programming Supply Current		10	mA
C	V_{CC} Supply Current		30	mA
t_{CLCL}	Oscillator Frequency	3	33	MHz
$_{VGL}$	Address Setup to $\overline{PROG}$ Low	$48t_{CLCL}$		
$_{HAX}$	Address Hold After $\overline{PROG}$	$48t_{CLCL}$		
$_{VGL}$	Data Setup to $\overline{PROG}$ Low	$48t_{CLCL}$		
$_{HDX}$	Data Hold After $\overline{PROG}$	$48t_{CLCL}$		
$_{HSH}$	P2.7 ($\overline{ENABLE}$) High to V_{PP}	$48t_{CLCL}$		
$_{HGL}$	V_{PP} Setup to $\overline{PROG}$ Low	10		µs
$_{HSL}$	V_{PP} Hold After $\overline{PROG}$	10		µs
$_{LGH}$	$\overline{PROG}$ Width	0.2	1	µs
$_{VQV}$	Address to Data Valid		$48t_{CLCL}$	
$_{LQV}$	$\overline{ENABLE}$ Low to Data Valid		$48t_{CLCL}$	
$_{HQZ}$	Data Float After $\overline{ENABLE}$	0	$48t_{CLCL}$	
$_{HBL}$	$\overline{PROG}$ High to $\overline{BUSY}$ Low		1.0	µs
C	Byte Write Cycle Time		50	µs

ure 6. Flash Programming and Verification Waveforms – Parallel Mode

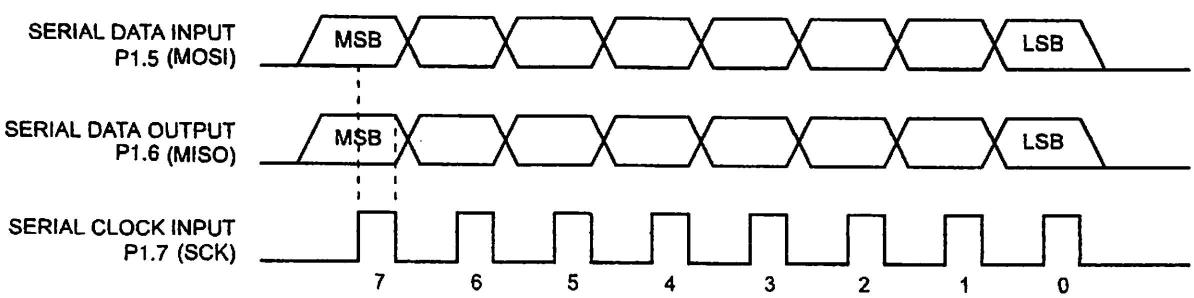


ure 7. Flash Memory Serial Downloading



ash Programming and Verification Waveforms – Serial Mode

ure 8. Serial Programming Waveforms



le 8. Serial Programming Instruction Set

struction	Instruction Format Byte 1	Byte 2	Byte 3	Byte 4	Operation
ogramming Enable	1010 1100	0101 0011	xxxx xxxx	xxxx xxxx 0110 1001 (Output)	Enable Serial Programming while RST is high
ip Erase	1010 1100	100x xxxx	xxxx xxxx	xxxx xxxx	Chip Erase Flash memory array
ead Program Memory yte Mode)	0010 0000	xxxx A11 A10 A9 A8	A7 A6 A5 A4 A3 A2 A1 A0	D7 D6 D5 D4 D3 D2 D1 D0	Read data from Program memory in the byte mode
rite Program Memory yte Mode)	0100 0000	xxxx A11 A10 A9 A8	A7 A6 A5 A4 A3 A2 A1 A0	D7 D6 D5 D4 D3 D2 D1 D0	Write data to Program memory in the byte mode
rite Lock Bits[2]	1010 1100	1110 00 B1 B2	xxxx xxxx	xxxx xxxx	Write Lock bits. See Note (2).
ead Lock Bits	0010 0100	xxxx xxxx	xxxx xxxx	xx LB3 LB2 LB1 xx	Read back current status of the lock bits (a programmed lock bit reads back as a "1")
ead Signature Bytes[1]	0010 1000	xxx A5 A4 A3 A2 A1	A0 xxx xxxx	Signature Byte	Read Signature Byte
ead Program Memory age Mode)	0011 0000	xxxx A11 A10 A9 A8	Byte 0	Byte 1... Byte 255	Read data from Program memory in the Page Mode (256 bytes)
rite Program Memory age Mode)	0101 0000	xxxx A11 A10 A9 A8	Byte 0	Byte 1... Byte 255	Write data to Program memory in the Page Mode (256 bytes)

es: 1. The signature bytes are not readable in Lock Bit Modes 3 and 4.

2. B1 = 0, B2 = 0 → Mode 1, no lock protection
B1 = 0, B2 = 1 → Mode 2, lock bit 1 activated
B1 = 1, B2 = 0 → Mode 3, lock bit 2 activated
B1 = 1, B1 = 1 → Mode 4, lock bit 3 activated

} Each of the lock bits needs to be activated sequentially before Mode 4 can be executed.

After Reset signal is high, SCK should be low for at least 64 system clocks before it goes high to clock in the enable data bytes. No pulsing of Reset signal is necessary. SCK should be no faster than 1/16 of the system clock at XTAL1.

For Page Read/Write, the data always starts from byte 0 to 255. After the command byte and upper address byte are latched, each byte thereafter is treated as data until all 256 bytes are shifted in/out. Then the next instruction will be ready to be decoded.

Serial Programming Characteristics

Figure 9. Serial Programming Timing

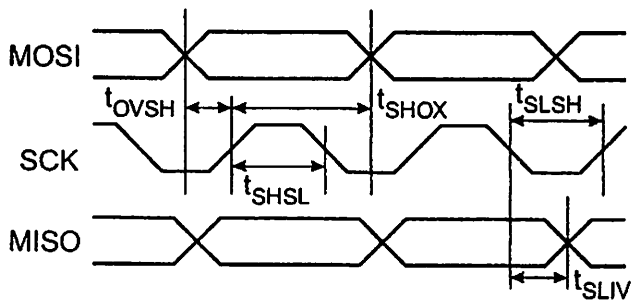


Table 9. Serial Programming Characteristics, T_A = -40° C to 85° C, V_{CC} = 4.0 - 5.5V (Unless Otherwise Noted)

Symbol	Parameter	Min	Typ	Max	Units
$1/t_{CLCL}$	Oscillator Frequency	0		33	MHz
t_{CLCL}	Oscillator Period	30			ns
t_{SHSL}	SCK Pulse Width High	8 t_{CLCL}			ns
t_{SLSH}	SCK Pulse Width Low	8 t_{CLCL}			ns
t_{OVSH}	MOSI Setup to SCK High	t_{CLCL}			ns
t_{SHOX}	MOSI Hold after SCK High	2 t_{CLCL}			ns
t_{SLIV}	SCK Low to MISO Valid	10	16	32	ns
t_{ERASE}	Chip Erase Instruction Cycle Time			500	ms
t_{SWC}	Serial Byte Write Cycle Time			64 t_{CLCL} + 400	μs

osolute Maximum Ratings*

perating Temperature	-55°C to +125°C
orage Temperature	-65°C to +150°C
oltage on Any Pin ith Respect to Ground	-1.0V to +7.0V
aximum Operating Voltage	6.6V
C Output Current	15.0 mA

*NOTICE: Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

C Characteristics

e values shown in this table are valid for T_A = -40°C to 85°C and V_{CC} = 4.0V to 5.5V, unless otherwise noted.

ymbol	Parameter	Condition	Min	Max	Units
L	Input Low Voltage	(Except $\overline{EA}$)	-0.5	0.2 V_{CC}-0.1	V
L1	Input Low Voltage ($\overline{EA}$)		-0.5	0.2 V_{CC}-0.3	V
H	Input High Voltage	(Except XTAL1, RST)	0.2 V_{CC}+0.9	V_{CC}+0.5	V
H1	Input High Voltage	(XTAL1, RST)	0.7 V_{CC}	V_{CC}+0.5	V
OL	Output Low Voltage(1) (Ports 1,2,3)	I_{OL} = 1.6 mA		0.45	V
OL1	Output Low Voltage(1) (Port 0, ALE, $\overline{PSEN}$)	I_{OL} = 3.2 mA		0.45	V
OH	Output High Voltage (Ports 1,2,3, ALE, $\overline{PSEN}$)	I_{OH} = -60 µA, V_{CC} = 5V ± 10%	2.4		V
		I_{OH} = -25 µA	0.75 V_{CC}		V
		I_{OH} = -10 µA	0.9 V_{CC}		V
OH1	Output High Voltage (Port 0 in External Bus Mode)	I_{OH} = -800 µA, V_{CC} = 5V ± 10%	2.4		V
		I_{OH} = -300 µA	0.75 V_{CC}		V
		I_{OH} = -80 µA	0.9 V_{CC}		V
	Logical 0 Input Current (Ports 1,2,3)	V_{IN} = 0.45V		-50	µA
L	Logical 1 to 0 Transition Current (Ports 1,2,3)	V_{IN} = 2V, V_{CC} = 5V ± 10%		-650	µA
I	Input Leakage Current (Port 0, $\overline{EA}$)	0.45 < V_{IN} < V_{CC}		±10	µA
RST	Reset Pulldown Resistor		50	300	KΩ
IO	Pin Capacitance	Test Freq. = 1 MHz, T_A = 25°C		10	pF
C	Power Supply Current	Active Mode, 12 MHz		25	mA
		Idle Mode, 12 MHz		6.5	mA
	Power-down Mode(2)	V_{CC} = 5.5V		50	µA

es: 1. Under steady state (non-transient) conditions, I_{OL} must be externally limited as follows:
Maximum I_{OL} per port pin: 10 mA
Maximum I_{OL} per 8-bit port:
Port 0: 26 mA Ports 1, 2, 3: 15 mA
Maximum total I_{OL} for all output pins: 71 mA
If I_{OL} exceeds the test condition, V_{OL} may exceed the related specification. Pins are not guaranteed to sink current greater than the listed test conditions.
2. Minimum V_{CC} for Power-down is 2V.

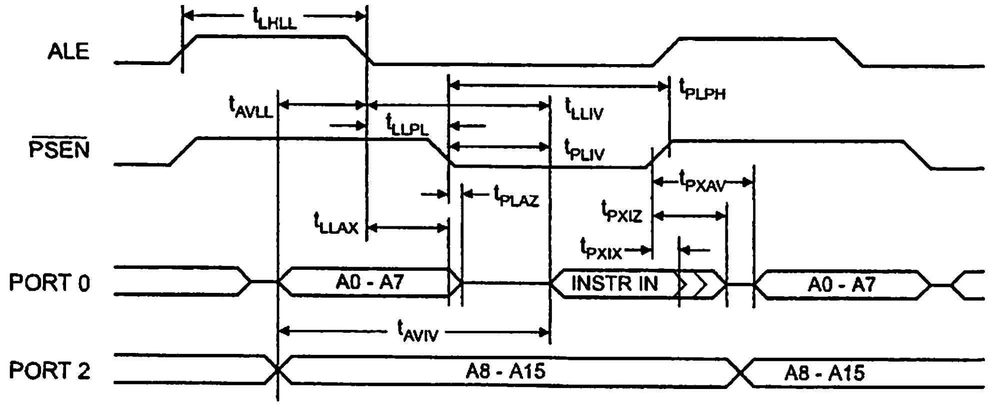
C Characteristics

der operating conditions, load capacitance for Port 0, ALE/$\overline{PROG}$, and $\overline{PSEN}$ = 100 pF; load capacitance for all other puts = 80 pF.

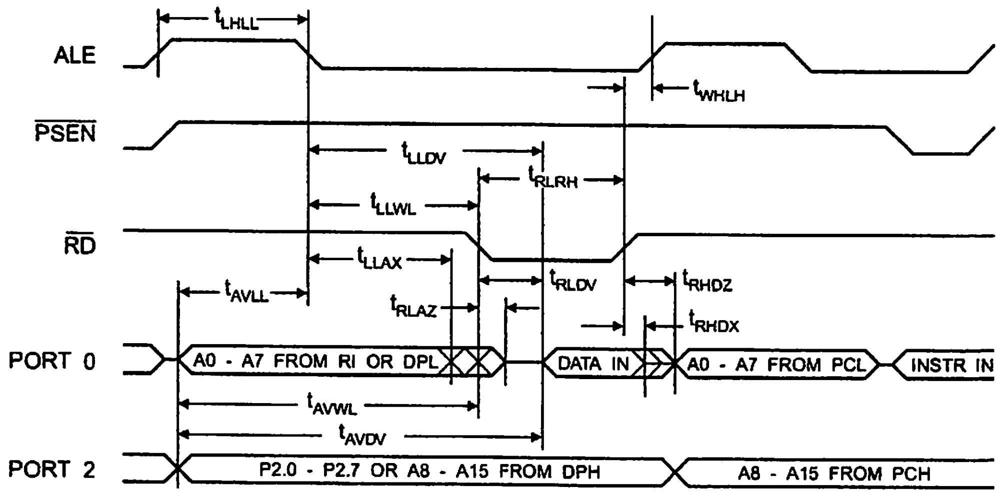
xternal Program and Data Memory Characteristics

ymbol	Parameter	12 MHz Oscillator		Variable Oscillator		Units
		Min	Max	Min	Max	
t_{CLCL}	Oscillator Frequency			0	33	MHz
HLL	ALE Pulse Width	127		$2t_{CLCL}$-40		ns
VLL	Address Valid to ALE Low	43		t_{CLCL}-25		ns
LAX	Address Hold After ALE Low	48		t_{CLCL}-25		ns
LIV	ALE Low to Valid Instruction In		233		$4t_{CLCL}$-65	ns
LPL	ALE Low to $\overline{PSEN}$ Low	43		t_{CLCL}-25		ns
LPH	$\overline{PSEN}$ Pulse Width	205		$3t_{CLCL}$-45		ns
LIV	$\overline{PSEN}$ Low to Valid Instruction In		145		$3t_{CLCL}$-60	ns
XIX	Input Instruction Hold After $\overline{PSEN}$	0		0		ns
XIZ	Input Instruction Float After $\overline{PSEN}$		59		t_{CLCL}-25	ns
XAV	$\overline{PSEN}$ to Address Valid	75		t_{CLCL}-8		ns
VIV	Address to Valid Instruction In		312		$5t_{CLCL}$-80	ns
LAZ	$\overline{PSEN}$ Low to Address Float		10		10	ns
LRH	$\overline{RD}$ Pulse Width	400		$6t_{CLCL}$-100		ns
LWH	$\overline{WR}$ Pulse Width	400		$6t_{CLCL}$-100		ns
LDV	$\overline{RD}$ Low to Valid Data In		252		$5t_{CLCL}$-90	ns
HDX	Data Hold After $\overline{RD}$	0		0		ns
HDZ	Data Float After $\overline{RD}$		97		$2t_{CLCL}$-28	ns
DV	ALE Low to Valid Data In		517		$8t_{CLCL}$-150	ns
VDV	Address to Valid Data In		585		$9t_{CLCL}$-165	ns
WL	ALE Low to $\overline{RD}$ or $\overline{WR}$ Low	200	300	$3t_{CLCL}$-50	$3t_{CLCL}$+50	ns
WL	Address to $\overline{RD}$ or $\overline{WR}$ Low	203		$4t_{CLCL}$-75		ns
VWX	Data Valid to $\overline{WR}$ Transition	23		t_{CLCL}-30		ns
VWH	Data Valid to $\overline{WR}$ High	433		$7t_{CLCL}$-130		ns
HQX	Data Hold After $\overline{WR}$	33		t_{CLCL}-25		ns
AZ	$\overline{RD}$ Low to Address Float		0		0	ns
HLH	$\overline{RD}$ or $\overline{WR}$ High to ALE High	43	123	t_{CLCL}-25	t_{CLCL}+25	ns

xternal Program Memory Read Cycle



xternal Data Memory Read Cycle



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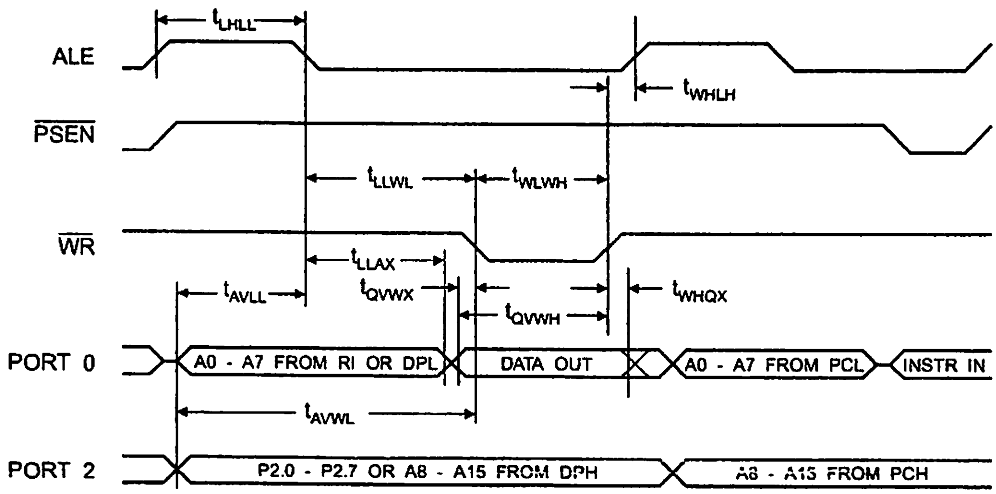
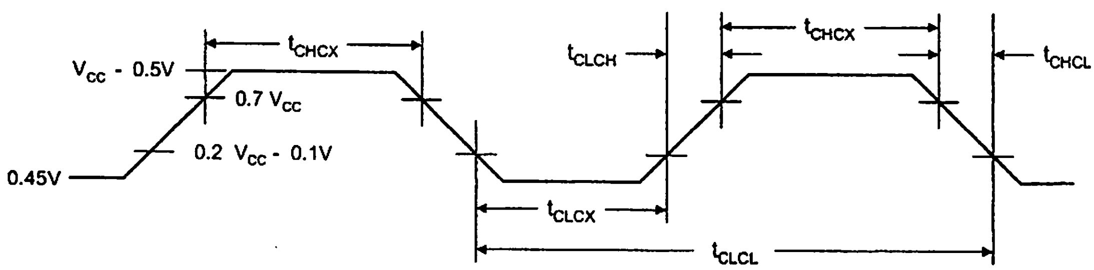
:ternal Data Memory Write Cycle



:ternal Clock Drive Waveforms



:ternal Clock Drive

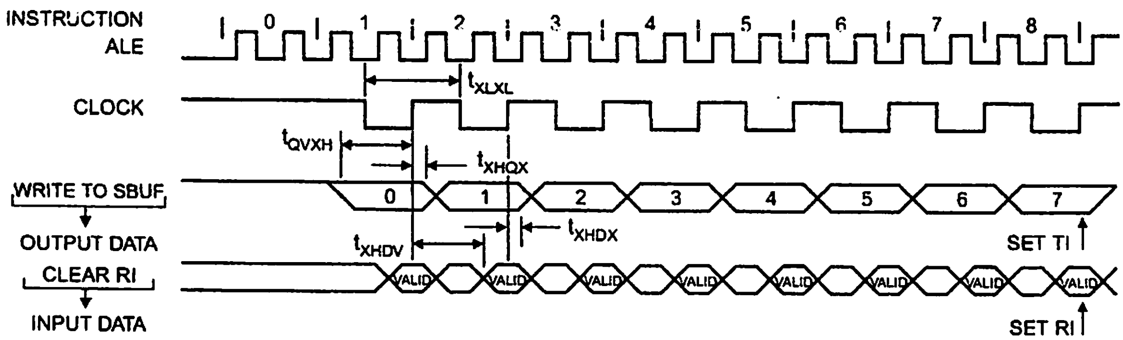
ymbol	Parameter	Min	Max	Units
'CLCL	Oscillator Frequency	0	33	MHz
.CL	Clock Period	30		ns
ICX	High Time	12		ns
.CX	Low Time	12		ns
.CH	Rise Time		5	ns
ICL	Fall Time		5	ns

›rial Port Timing: Shift Register Mode Test Conditions

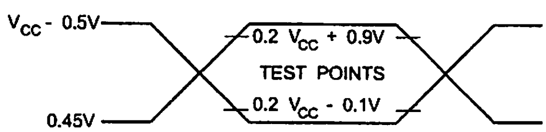
› values in this table are valid for V_{CC} = 4.0V to 5.5V and Load Capacitance = 80 pF.

›mbol	Parameter	12 MHz Osc		Variable Oscillator		Units
		Min	Max	Min	Max	
XL	Serial Port Clock Cycle Time	1.0		$12t_{CLCL}$		µs
/XH	Output Data Setup to Clock Rising Edge	700		$10t_{CLCL}$-133		ns
4QX	Output Data Hold After Clock Rising Edge	50		$2t_{CLCL}$-80		ns
4DX	Input Data Hold After Clock Rising Edge	0		0		ns
4DV	Clock Rising Edge to Input Data Valid		700		$10t_{CLCL}$-133	ns

›ift Register Mode Timing Waveforms

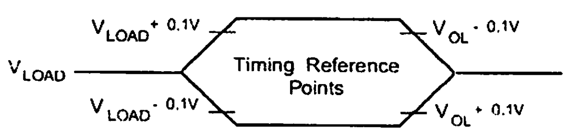


› Testing Input/Output Waveforms(1)



›: 1. AC Inputs during testing are driven at V_{CC} - 0.5V for a logic 1 and 0.45V for a logic 0. Timing measurements are made at V_{IH} min. for a logic 1 and V_{IL} max. for a logic 0.

›at Waveforms(1)



›: 1. For timing purposes, a port pin is no longer floating when a 100 mV change from load voltage occurs. A port pin begins to float when a 100 mV change from the loaded V_{OH}/V_{OL} level occurs.

'dering Information

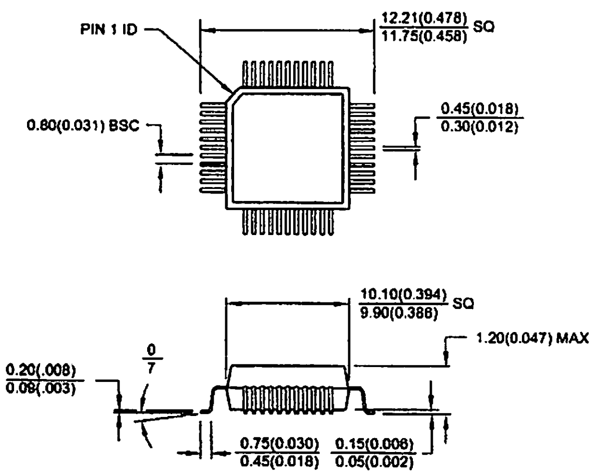
Speed (MHz)	Power Supply	Ordering Code	Package	Operation Range
24	4.0V to 5.5V	AT89S51-24AC AT89S51-24JC AT89S51-24PC	44A 44J 40P6	Commercial (0°C to 70°C)
		AT89S51-24AI AT89S51-24JI AT89S51-24PI	44A 44J 40P6	Industrial (-40°C to 85°C)
33	4.5V to 5.5V	AT89S51-33AC AT89S51-33JC AT89S51-33PC	44A 44J 40P6	Commercial (0°C to 70°C)

= Preliminary Availability

	Package Type
lA	44-lead, Thin Plastic Gull Wing Quad Flatpack (TQFP)
lJ	44-lead, Plastic J-leaded Chip Carrier (PLCC)
lP6	40-pin, 0.600" Wide, Plastic Dual Inline Package (PDIP)

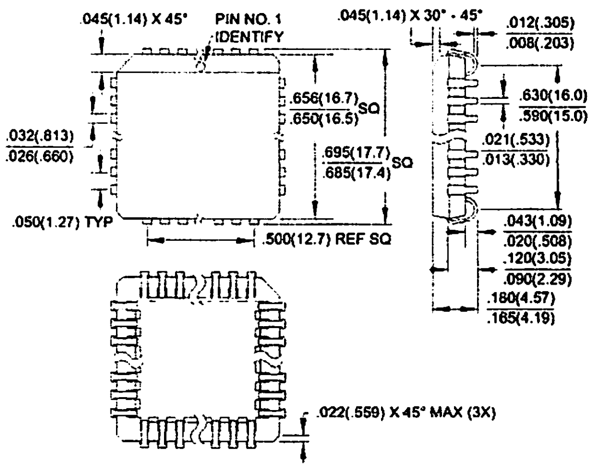
ıckaging Information

44A, 44-lead, Thin (1.0 mm) Plastic Gull Wing Quad Flat Package (TQFP)
Dimensions in Millimeters and (Inches)*

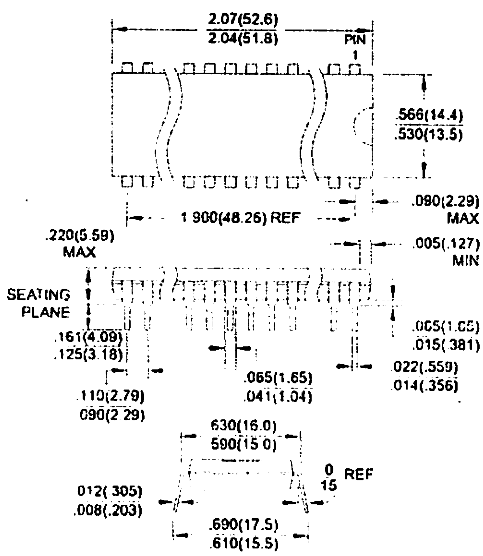


*Controlling dimension: millimeters

44J, 44-lead, Plastic J-leaded Chip Carrier (PLCC)
Dimensions in Inches and (Millimeters)



40P6, 40-pin, 0.600" Wide, Plastic Dual Inline Package (PDIP)
Dimensions in Inches and (Millimeters)
JEDEC STANDARD MS-011 AC



:mel Headquarters

ırporate Headquarters
2325 Orchard Parkway
San Jose, CA 95131
TEL (408) 441-0311
FAX (408) 487-2600

ırope
Atmel SarL
Route des Arsenaux 41
Casa Postale 80
CH-1705 Fribourg
Switzerland
TEL (41) 26-426-5555
FAX (41) 26-426-5500

ia
Atmel Asia, Ltd.
Room 1219
Chinachem Golden Plaza
77 Mody Road Tsimhatsui
East Kowloon
Hong Kong
TEL (852) 2721-9778
FAX (852) 2722-1369

pan
Atmel Japan K.K.
9F, Tonetsu Shinkawa Bldg.
1-24-8 Shinkawa
Chuo-ku, Tokyo 104-0033
Japan
TEL (81) 3-3523-3551
FAX (81) 3-3523-7581

Atmel Product Operations

Atmel Colorado Springs
1150 E. Cheyenne Mtn. Blvd.
Colorado Springs, CO 80906
TEL (719) 576-3300
FAX (719) 540-1759

Atmel Grenoble
Avenue de Rochepleine
BP 123
38521 Saint-Egreve Cedex, France
TEL (33) 4-7658-3000
FAX (33) 4-7658-3480

Atmel Heilbronn
Theresienstrasse 2
POB 3535
D-74025 Heilbronn, Germany
TEL (49) 71 31 67-25 94
FAX (49) 71 31 67 24 23

Atmel Nantes
La Chantrerie
BP 70602
44306 Nantes Cedex 3, France
TEL (33) 0 2 40 18 18 18
FAX (33) 0 2 40 18 19 60

Atmel Rousset
Zone Industrielle
13106 Rousset Cedex, France
TEL (33) 4-4253-6000
FAX (33) 4-4253-6001

Atmel Smart Card ICs
Scottish Enterprise Technology Park
East Kilbride, Scotland G75 0QR
TEL (44) 1355-357-000
FAX (44) 1355-242-743

e-mail
literature@atmel.com

Web Site
http://www.atmel.com

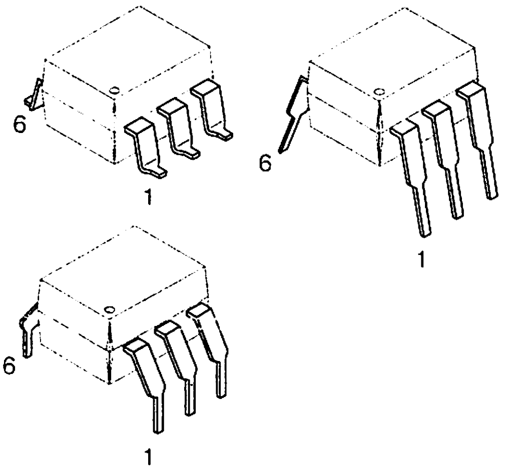
2487A–10/01/xM

AIRCHILD
:MICONDUCTOR®

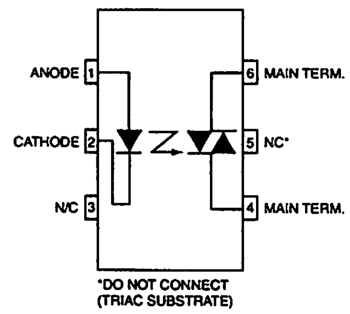
6-PIN DIP RANDOM-PHASE OPTOISOLATORS TRIAC DRIVER OUTPUT (250/400 VOLT PEAK)

C3010M MOC3011M MOC3012M MOC3020M MOC3021M MOC3022M MOC3023M

PACKAGE



SCHEMATIC



;CRIPTION

/IOC301XM and MOC302XM series are optically isolated triac driver devices. These devices contain a GaAs infrared ng diode and a light activated silicon bilateral switch, which functions like a triac. They are designed for interfacing between ·onic controls and power triacs to control resistive and inductive loads for 115 VAC operations.

\TURES

:cellent I_{FT} stability—IR emitting diode has low degradation
ɡh isolation voltage—minimum 5300 VAC RMS
ıderwriters Laboratory (UL) recognized—File #E90700
·ak blocking voltage
250V-MOC301XM
400V-MOC302XM
)E recognized (File #94766)
Ordering option V (e.g. MOC3023VM)

’LICATIONS

dustrial controls
affic lights
nding machines
lid state relay
mp ballasts

- Solenoid/valve controls
- Static AC power switch
- Incandescent lamp dimmers
- Motor control

6-PIN DIP RANDOM-PHASE OPTOISOLATORS TRIAC DRIVER OUTPUT (250/400 VOLT PEAK)

BSOLUTE MAXIMUM RATINGS (T_A = 25°C unless otherwise noted)

rameters	Symbol	Device	Value	Units
ITAL DEVICE				
›rage Temperature	T_{STG}	All	-40 to +150	°C
›erating Temperature	T_{OPR}	All	-40 to +85	°C
ad Solder Temperature	T_{SOL}	All	260 for 10 sec	°C
nction Temperature Range	T_J	All	-40 to +100	°C
›lation Surge Voltage[1] ›ak AC voltage, 60Hz, 1 sec duration)	V_{ISO}	All	7500	Vac(pk)
tal Device Power Dissipation @ 25°C	P_D	All	330	mW
›rate above 25°C			4.4	mW/°C
IITTER				
›ntinuous Forward Current	I_F	All	60	mA
›verse Voltage	V_R	All	3	V
tal Power Dissipation 25°C Ambient	P_D	All	100	mW
›rate above 25°C			1.33	mW/°C
:TECTOR				
f-State Output Terminal Voltage	V_{DRM}	MOC3010M/1M/2M MOC3020M/1M/2M/3M	250 400	V
ak Repetitive Surge Current (PW = 1 ms, 120 pps)	I_{TSM}	All	1	V
tal Power Dissipation @ 25°C Ambient	P_D	All	300	mW
›rate above 25°C			4	mW/°C

e

solation surge voltage, V_{ISO}, is an internal device dielectric breakdown rating. For this test, Pins 1 and 2 are common, and ›ins 4, 5 and 6 are common.

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.ECTRICAL CHARACTERISTICS (T_A = 25°C Unless otherwise specified)

DIVIDUAL COMPONENT CHARACTERISTICS

Parameters	Test Conditions	Symbol	Device	Min	Typ	Max	Units
IITTER							
ut Forward Voltage	I_F = 10 mA	V_F	All		1.15	1.5	V
verse Leakage Current	V_R = 3 V, T_A = 25°C	I_R	All		0.01	100	µA
TECTOR							
ak Blocking Current,Either Direction	Rated V_{DRM}, I_F = 0 (note 1)	I_{DRM}	All		10	100	nA
ak On-State Voltage,Either Direction	I_{TM} = 100 mA peak, I_F = 0	V_{TM}	All		1.8	3	V

RANSFER CHARACTERISTICS (T_A = 25°C Unless otherwise specified.)

Characteristics	Test Conditions	Symbol	Device	Min	Typ	Max	Units
D Trigger Current	Voltage = 3V (note 3)	I_{FT}	MOC3020M			30	mA
			MOC3010M			15	
			MOC3021M				
			MOC3011M			10	
			MOC3022M				
			MOC3012M			5	
			MOC3023M				
lding Current, Either Direction		I_H	All		100		µA

e

est voltage must be applied within dv/dt rating.

his is static dv/dt. See Figure 5 for test circuit. Commutating dv/dt is a function of the load-driving thyristor(s) only.

ll devices are guaranteed to trigger at an I_F value less than or equal to max I_{FT}. Therefore, recommended operating I_F lies etween max I_{FT} (30 mA for MOC3020M, 15 mA for MOC3010M and MOC3021M, 10 mA for MOC3011M and MOC3022M, mA for MOC3012M and MOC3023M) and absolute max I_F (60 mA).

Fig. 1 LED Forward Voltage vs. Forward Current

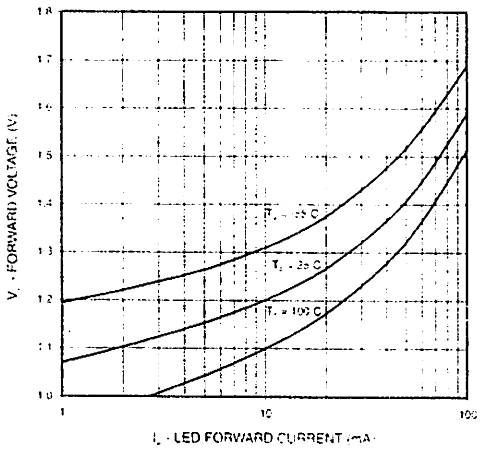


Fig. 2 On-State Characteristics

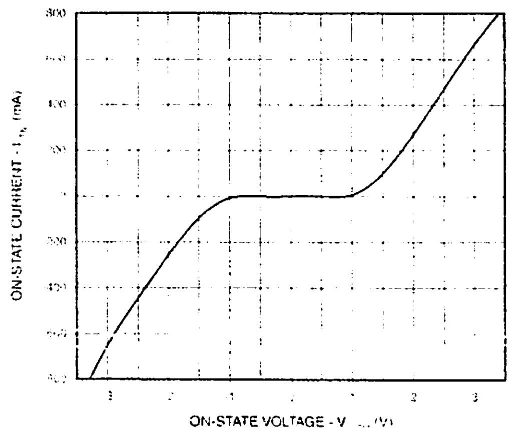


Fig. 3 Trigger Current vs. Ambient Temperature

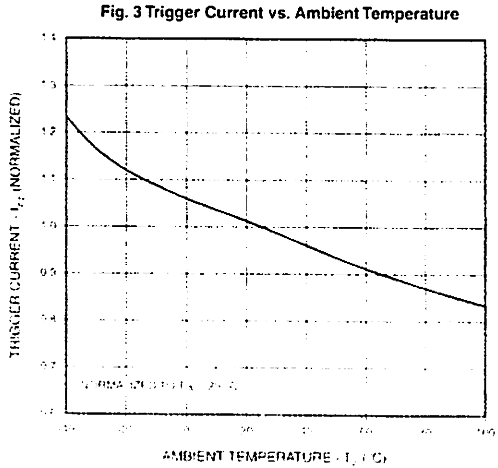


Fig. 4 LED Current Required to Trigger vs. LED Pulse Width

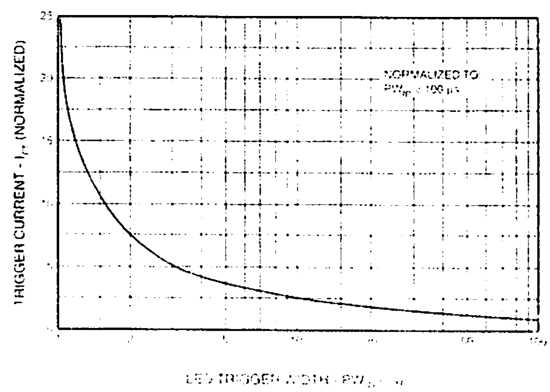


Fig. 5 dv/dt vs. Temperature

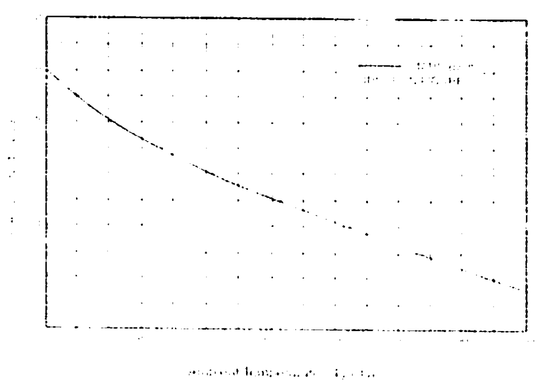
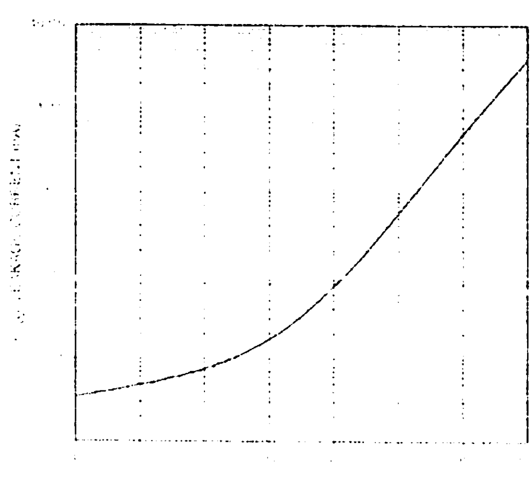
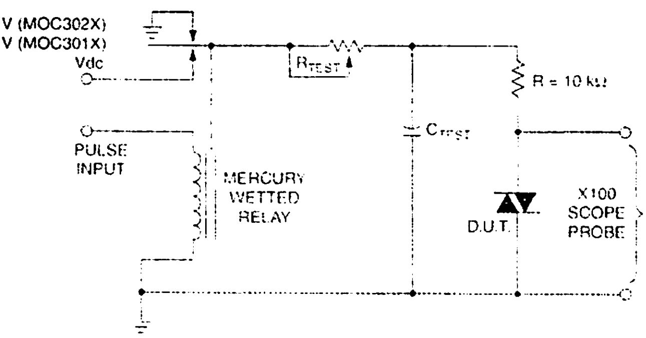


Fig 6 Leakage Current, I_{DRM} vs. Temperature



6-PIN DIP RANDOM-PHASE OPTOISOLATORS TRIAC DRIVER OUTPUT (250/400 VOLT PEAK)



1. The mercury wetted relay provides a high speed repeated pulse to the D.U.T.
2. 100x scope probes are used, to allow high speeds and voltages.
3. The worst-case condition for static dv/dt is established by triggering the D.U.T. with a normal LED input current, then removing the current. The variable R_{TEST} allows the dv/dt to be gradually increased until the D.U.T. continues to trigger in response to the applied voltage pulse, even after the LED current has been removed. The dv/dt is then decreased until the D.U.T. stops triggering. τ_{RC} is measured at this point and recorded.

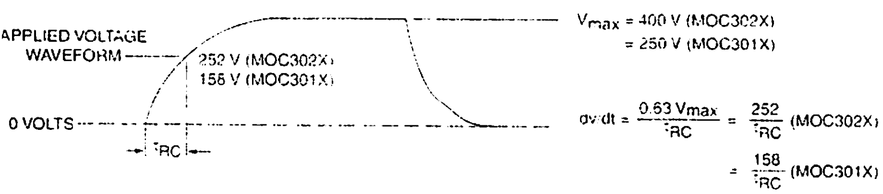


Figure 5. Static dv/dt Test Circuit

e: This optoisolator should not be used to drive a load directly.
It is intended to be a trigger device only.

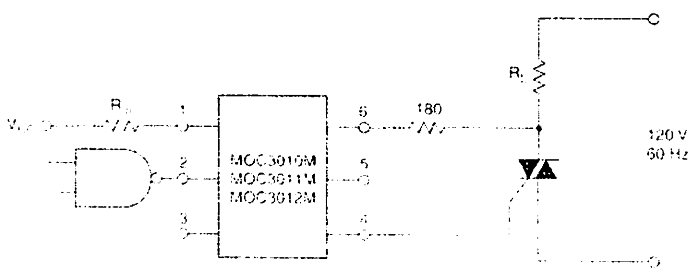


Figure 6. Resistive Load

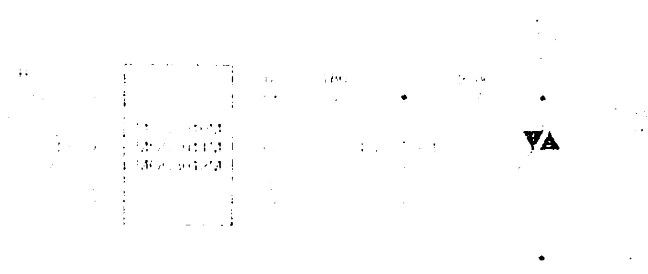


Figure 7. Inductive Load with Sensitive Gate Triac (I_{GT} 15 mA)

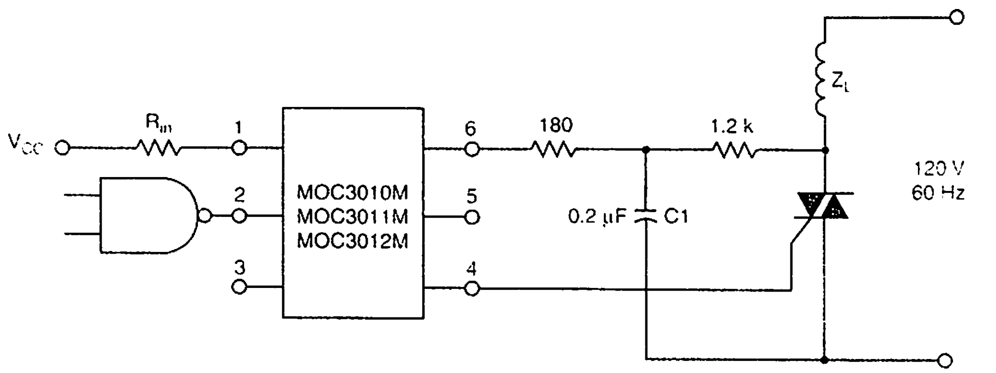
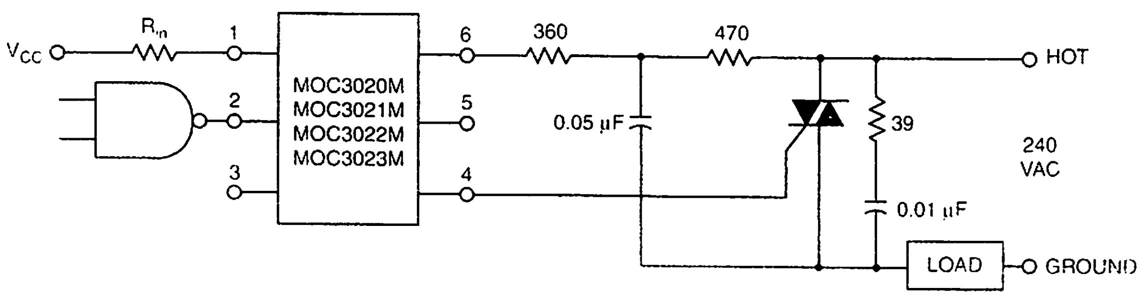


Figure 8. Inductive Load with Sensitive Gate Triac ($I_{GT} \leq 15$ mA)



In this circuit the "hot" side of the line is switched and the load connected to the cold or ground side.

The 39 ohm resistor and 0.01µF capacitor are for snubbing of the triac, and the 470 ohm resistor and 0.05 µF capacitor are for snubbing the coupler. These components may or may not be necessary depending upon the particular and load used.

Figure 9. Typical Application Circuit

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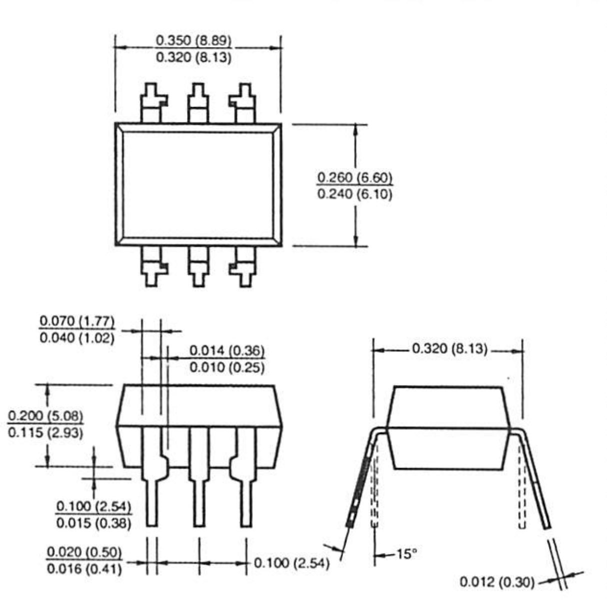
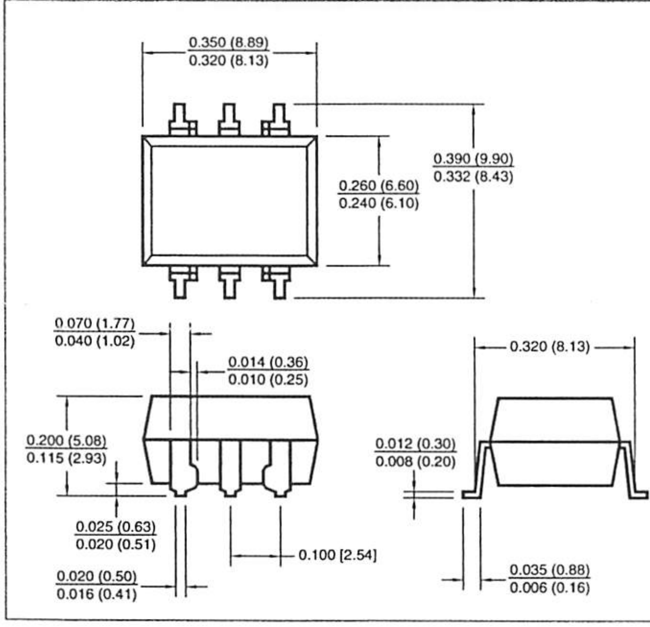
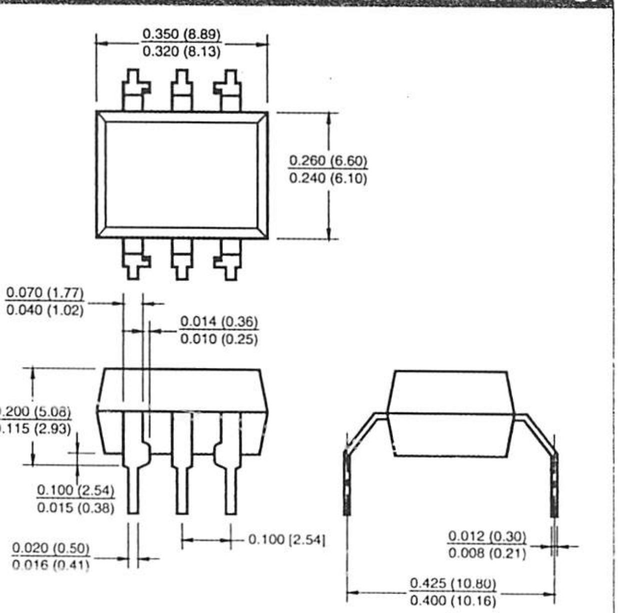
Package Dimensions (Through Hole)



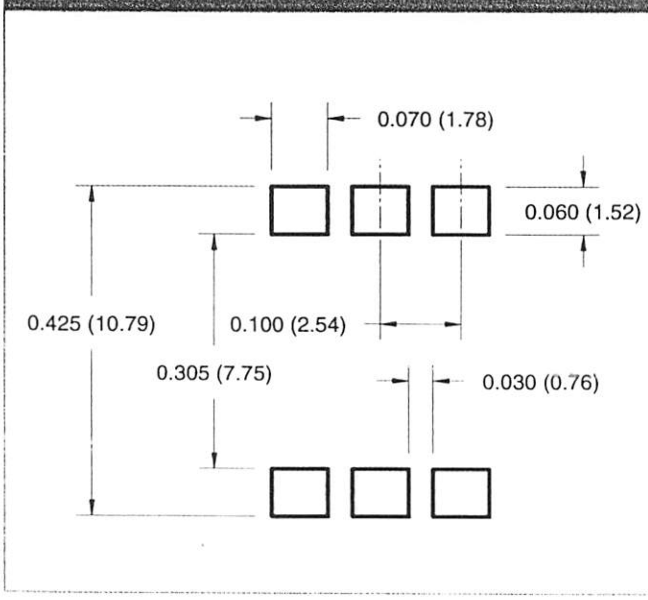
Package Dimensions (Surface Mount)



ackage Dimensions (0.4" Lead Spacing)



Recommended Pad Layout for Surface Mount Leadform



TE

limensions are in inches (millimeters)

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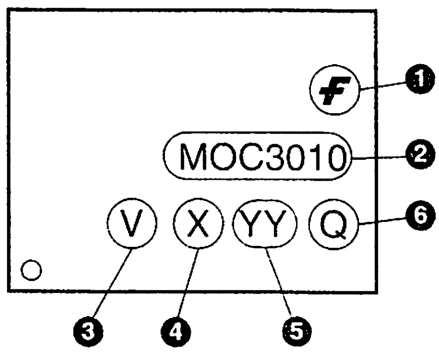
C3010M MOC3011M MOC3012M MOC3020M MOC3021M MOC3022M MOC3023M

DERING INFORMATION

tion	Order Entry Identifier	Description
	S	Surface Mount Lead Bend
?	SR2	Surface Mount; Tape and reel
	T	0.4" Lead Spacing
	V	VDE 0884
	TV	VDE 0884, 0.4" Lead Spacing
	SV	VDE 0884, Surface Mount
?V	SR2V	VDE 0884, Surface Mount, Tape & Reel

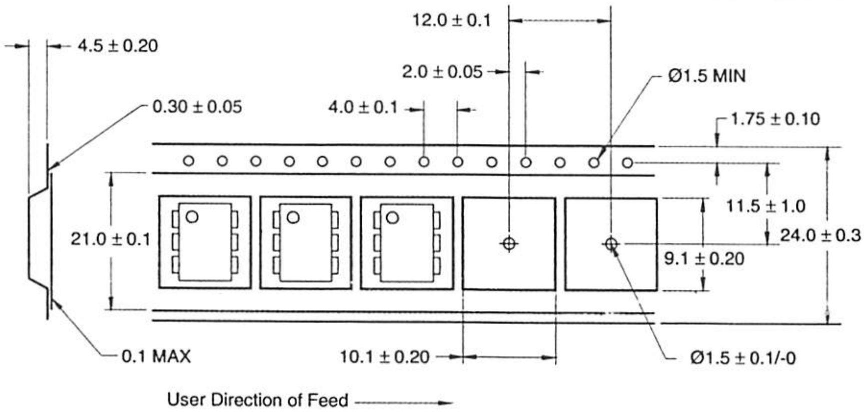
RKING INFORMATION



Definitions	
1	Fairchild logo
2	Device number
3	VDE mark (Note: Only appears on parts ordered with VDE option – See order entry table)
4	One digit year code, e.g., '3'
5	Two digit work week ranging from '01' to '53'
6	Assembly package code

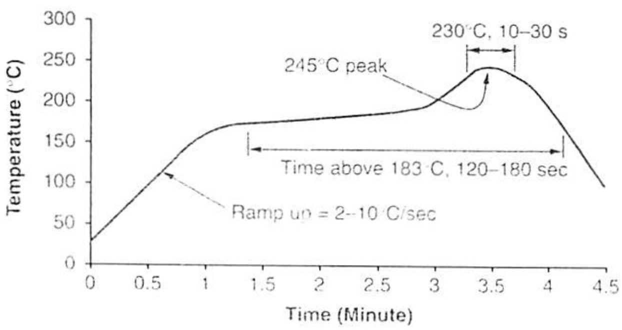
*Note – Parts that do not have the 'V' option (see definition 3 above) [illegible]

arrier Tape Specifications



TE
limensions are in inches (millimeters)

flow Profile (White Package, -M Suffix)



- Peak reflow temperature: 245°C (package surface temperature)
- Time of temperature higher than 183°C for 120–180 seconds
- One time soldering reflow is recommended

6-PIN DIP RANDOM-PHASE OPTOISOLATORS TRIAC DRIVER OUTPUT (250/400 VOLT PEAK)

)C3010M MOC3011M MOC3012M MOC3020M MOC3021M MOC3022M MOC3023M

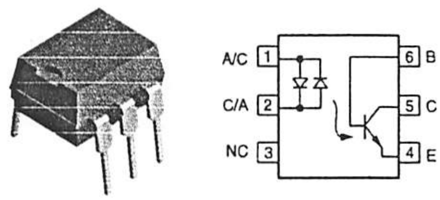
CLAIMER

: SUPPORT POLICY

Optocoupler, Phototransistor Output, AC input, With Base Connection

Features

- AC or Polarity Insensitive Input
- Built-in Reverse Polarity Input Protection
- I/O Compatible with Integrated Circuits
- Industry Standard DIP Package
- Isolation Test Voltage 5300 V_{RMS}



Agency Approvals

- UL File #E52744 System Code H or J
- CSA 93751
- BSI IEC60950 IEC60965
- DIN EN 60747-5-2(VDE0884)
  DIN EN 60747-5-5 pending
  Available with Option 1
- FIMKO

Applications

Telephone line detection
AC line motor
PLC
Instrumentation

Description

The H11AA1 is a bi-directional input optically coupled isolator consisting of two inverse parallel Gallium Arsenide infrared LEDs coupled to a silicon NPN phototransistor in a 6-pin DIP package. The H11AA1 has a minimum CTR of 20 %, a CTR symmetry of 1:3 and is designed for applications requiring detection or monitoring of AC signals.

Order Information

Part	Remarks
H11AA1	CTR > 20 %, DIP-6
H11AA1-X006	CTR > 20 %, DIP-6 400 mil (option 6)
H11AA1-X007	CTR > 20 %, SMD-6 (option 7)
H11AA1-X009	CTR > 20 %, SMD-6 (option 9)

For additional information on the available options refer to Option Information.

Absolute Maximum Ratings

T_{amb} = 25 °C, unless otherwise specified
Stresses in excess of the absolute Maximum Ratings can cause permanent damage to the device. Functional operation of the device is not implied at these or any other conditions in excess of those given in the operational sections of this document. Exposure to absolute Maximum Rating for extended periods of the time can adversely affect reliability.

Input

Parameter	Test condition	Symbol	Value	Unit
Forward continuous current		I_F	60	mA
Power dissipation		P_{diss}	100	mW
Derate linearly from 25 °C			1.3	mW/°C

itput

Parameter	Test condition	Symbol	Value	Unit
wer dissipation		P_{diss}	200	mW
rate linearly from 25 °C			2.6	mW/°C
llector-emitter breakdown voltage		BV_{CEO}	30	V
nitter-base breakdown voltage		BV_{EBO}	5.0	V
llector-base breakdown voltage		BV_{CBO}	70	V

oupler

Parameter	Test condition	Symbol	Value	Unit
lation test voltage (between nitter and detector)	Referred to standard climate 23 °C/50%RH, DIN 50014	V_{ISO}	5300	V_{RMS}
eepage			≥ 7.0	mm
earance			≥ 7.0	mm
mparative tracking index per N IEC 112/VDE 0303, part 1			175	
lation resistance	V_{IO} = 500 V, T_{amb} = 25 °C	R_{IO}	≥ 10^{12}	Ω
	V_{IO} = 500 V, T_{amb} = 100 °C	R_{IO}	≥ 10^{11}	Ω
orage temperature		T_{stg}	- 55 to + 150	°C
erating temperature		T_{amb}	- 55 to + 100	°C
ad soldering time at 260 °C		T_{sld}	10	sec.

ectrical Characteristics

$_{ib}$ = 25 °C, unless otherwise specified
imum and maximum values are testing requirements. Typical values are characteristics of the device and are the result of engineering luation. Typical values are for information only and are not part of the testing requirements.

put

Parameter	Test condition	Symbol	Min	Typ.	Max	Unit
rward voltage	I_F = ± 10 mA	V_F		1.2	1.5	V

itput

Parameter	Test condition	Symbol	Min	Typ.	Max	Unit
llector-emitter breakdown voltage	I_C = 1.0 mA	BV_{CEO}	30			V
nitter-base breakdown voltage	I_E = 100 µA	BV_{EBO}	5.0			V
llector-base breakdown voltage	I_C = 100 µA	BV_{CBO}	70			V
llector-emitter leakage current	V_{CE} = 10 V	I_{CEO}		5.0	100	nA

oupler

Parameter	Test condition	Symbol	Min	Typ.	Max	Unit
llector-emitter saturation voltage	I_F = ± 10 mA, I_C = 0.5 mA	V_{CEsat}			0.4	V

Current Transfer Ratio

Parameter	Test condition	Symbol	Min	Typ.	Max	Unit
DC Current Transfer Ratio	$I_F = \pm 10$ mA, $V_{CE} = 10$ V	CTR_{DC}	20			%
Symmetry (CTR at + 10 mA) /(CTR at - 10 mA)			0.33	1.0	3.0	

Typical Characteristics (T_{amb} = 25 °C unless otherwise specified)

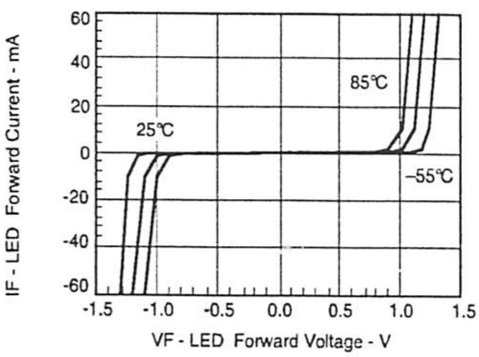


Fig. 1 LED Forward Current vs.Forward Voltage

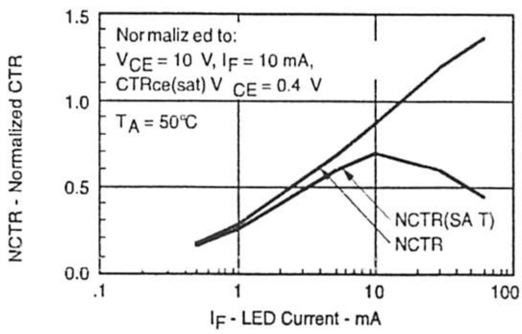


Fig. 3 Normalized Non-saturated and Saturated CTR vs. LED Current

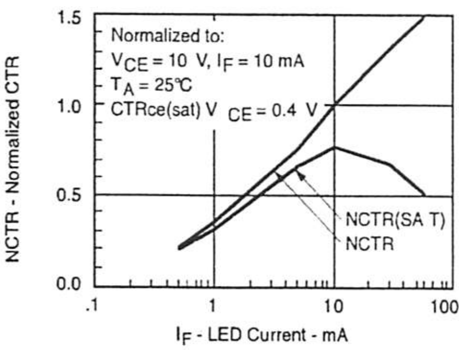


Fig. 2 Normalized Non-Saturated and Saturated CTR vs. LED Current

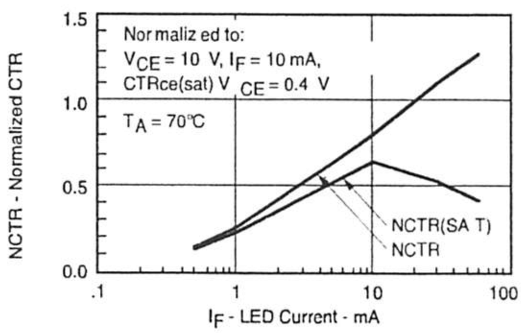
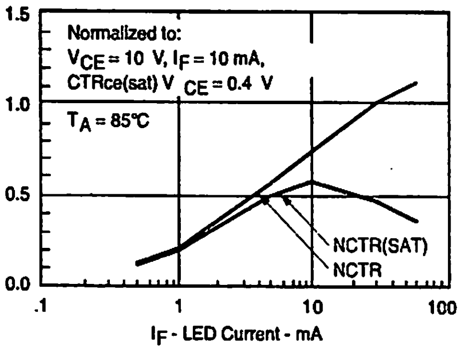


Fig. 4 Normalized Non-saturated and saturated CTR vs. LED Current



5 Normalized Non-saturated and saturated CTR vs. LED Current

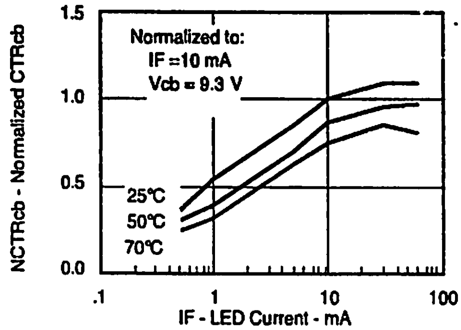
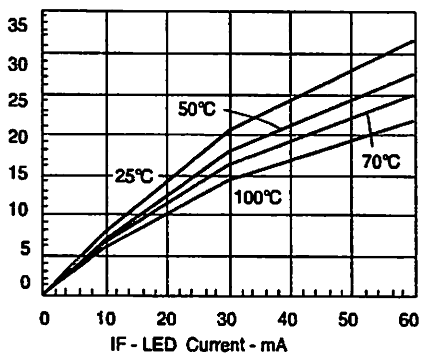


Fig. 8 Normalized CTRcb vs. LED Current and Temp.



6 Collector-Emitter Current vs. Temperature and LED Current

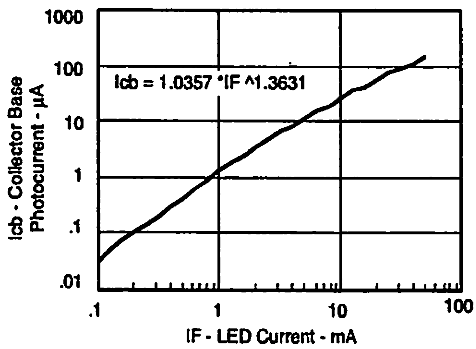
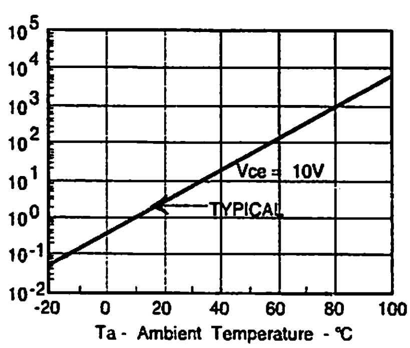


Fig. 9 Collector-Base Photocurrent vs. LED Current



7 Collector-Emitter Leakage Current vs.Temp.

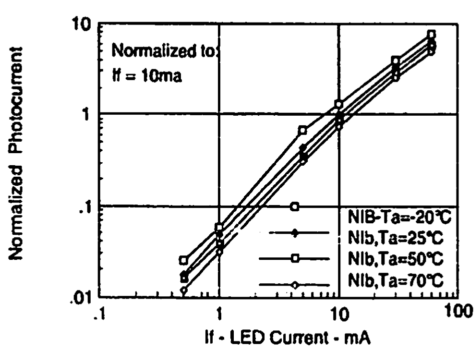


Fig. 10 Normalized Photocurrent vs. LED Current

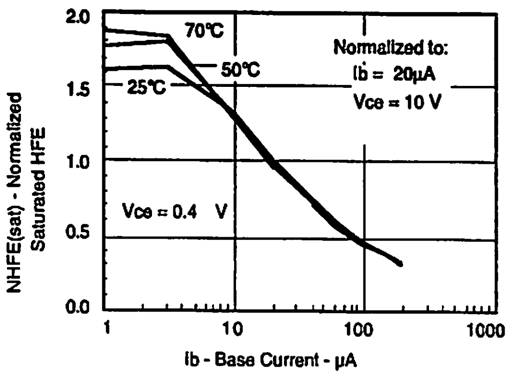


Fig. 11 Normalized Saturated HFE vs. Base Current and Temperature

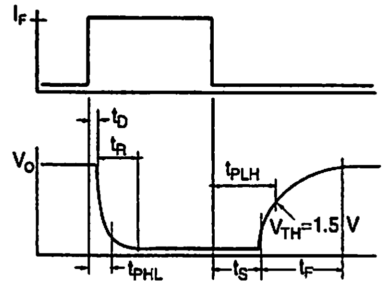


Fig. 14 Switching Waveform

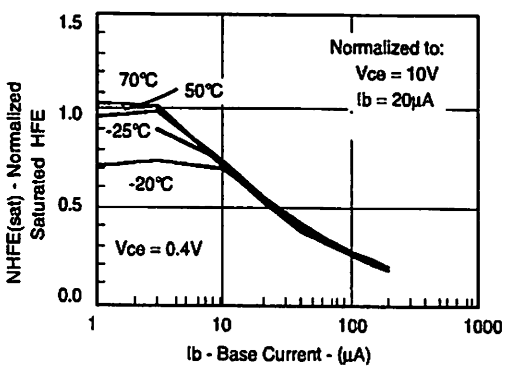


Fig. 12 Normalized Saturated HFE vs. Base Current and Temperature

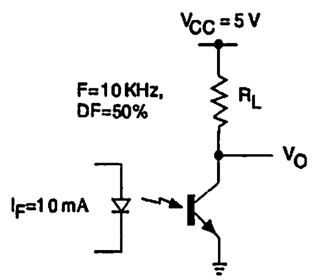


Fig. 15 Switching Schematic

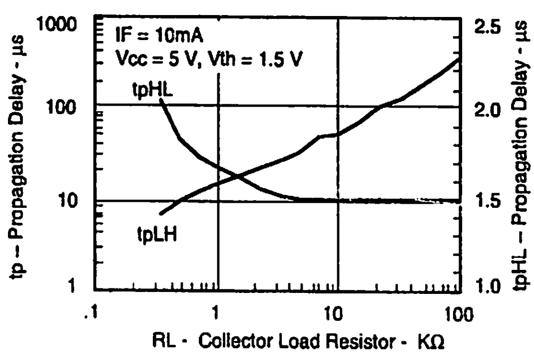
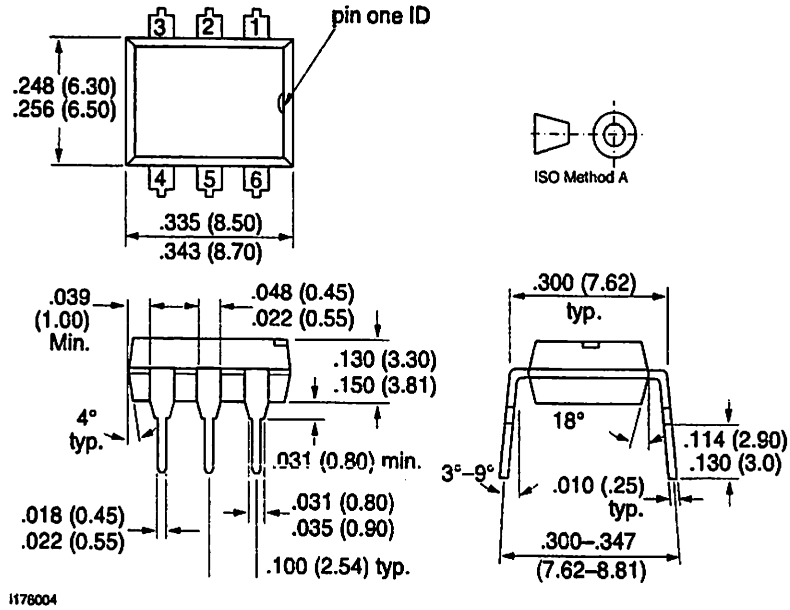
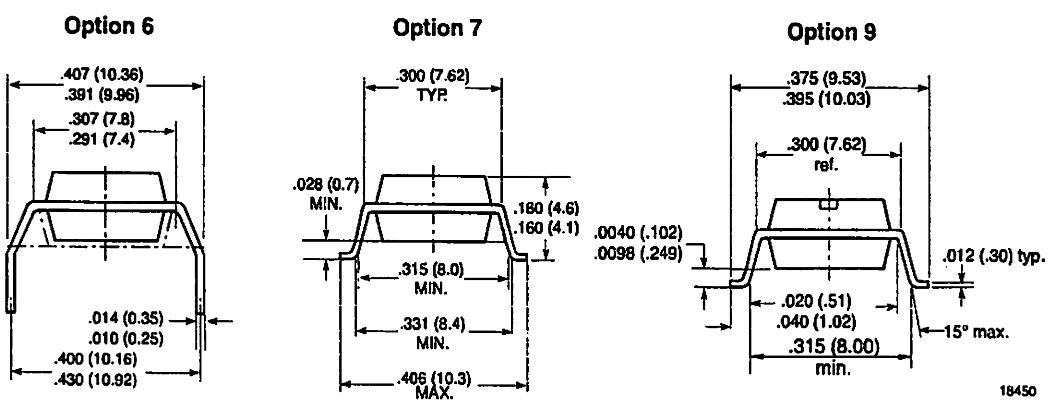


Fig. 13 Propagation Delay vs. Collector Load Resistor

ckage Dimensions in Inches (mm)





Ozone Depleting Substances Policy Statement

It is the policy of **Vishay Semiconductor GmbH** to

1. Meet all present and future national and international statutory requirements.
2. Regularly and continuously improve the performance of our products, processes, distribution and operatingsystems with respect to their impact on the health and safety of our employees and the public, as well as their impact on the environment.

It is particular concern to control or eliminate releases of those substances into the atmosphere which are known as ozone depleting substances (ODSs).

The Montreal Protocol (1987) and its London Amendments (1990) intend to severely restrict the use of ODSs and forbid their use within the next ten years. Various national and international initiatives are pressing for an earlier ban on these substances.

Vishay Semiconductor GmbH has been able to use its policy of continuous improvements to eliminate the use of ODSs listed in the following documents.

1. Annex A, B and list of transitional substances of the Montreal Protocol and the London Amendments respectively
2. Class I and II ozone depleting substances in the Clean Air Act Amendments of 1990 by the Environmental Protection Agency (EPA) in the USA
3. Council Decision 88/540/EEC and 91/690/EEC Annex A, B and C (transitional substances) respectively.

Vishay Semiconductor GmbH can certify that our semiconductors are not manufactured with ozone depleting substances and do not contain such substances.

Vishay Semiconductor GmbH, P.O.B. 3535, D-74025 Heilbronn, Germany
Telephone: 49 (0)7131 67 2831, Fax number: 49 (0)7131 67 2423

ı Infrared LED

EL NO : HIR333

Features :

- High radiant intensity
- Peak wavelength λp=850nm
- View angle 17˚
- High reliability
- 2.54mm Lead spacing

Description :

- EVERLIGHT's Infrared Emitting Diode (HIR333) is a high intensity diode, molded in a yellow transparent plastic package.
  The device is spectrally matched with phototransistor, photodiode and infrared receiver module.

Applications :

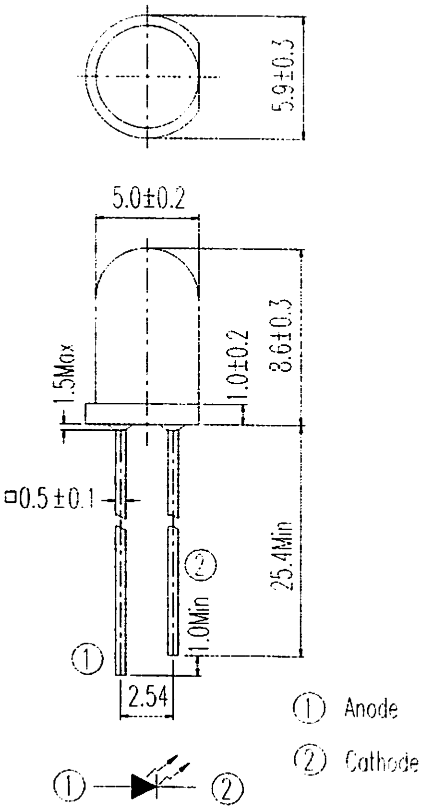
- Free air transmission system
- Optoelectronic switch
- Infrared remote control units with high power requirement
- Floppy disk drive
- Smoke detector

PART NO.	CHIP MATERIAL	LENS COLOR
HIR	GaAlAs	Yellow

ı Infrared LED

EL NO : HIR333

Package Dimensions :



Notes :

dimensions are in millimeter.
ıtruded resin under flange 1.5 mm Max.
ıd spacing is measured where the lead emerge from the package.
ıs color : Yellow transparent.
ɔve specification may be changed without notice. EVERLIGHT will reserve authority material change for above specification.
ɜse specification sheets include materials protected under copyright of EVERLIGHT poration . Please don't reproduce or cause anyone to reproduce them without ERLIGHT's consent.
en using this product , please observe the absolute maximum ratings and the tructions for use outlined in these specification sheets. EVERIGHT assumes no ponsibility for any damage resulting from use of the product which does not comply h the absolute maximum ratings and the instructions included in these specification ɜets.

n Infrared LED

EL NO : HIR333

■ Absolute Maximum Ratings at $T_A = 25$℃

Parameter	Symbol	Rating	Unit	Notice
ntinuous Forward Current	I_F	50	mA	
ak Forward Current lse width=100 μs,Duty cycle=1%	I_{FP}	1.0	A	
verse Voltage	V_R	5	V	
erating Temperature	Topr	-25 ~ +85	℃	
orage Temperature	Tstg	-40 ~ +85	℃	
ldering Temperature	Tsol	260	℃	4mm from mold body less than 5 seconds
wer Dissipation at(or below) ℃ Free Air Temperature	Pd	100	mW	

■ Electronic Optical Characteristics :

Parameter	Symbol	Min.	Typ.	Max.	Unit	Condition
diant Intensity	Ee	7.8	15.0	----	mW/sr	I_F=20mA
		----	140	----		I_F=100mA,tp=100 μs, t_p/T=0.01
		----	980	----		I_F=1A,tp=100 μs, t_p/T=0.01
ak Wavelength	λ_P	----	850	----	nm	I_F=20mA
ectral ndwidth	Δλ	---	45	---	nm	I_F=20mA
orward Voltage	V_F	---	1.45	1.65	V	I_F=20mA
		---	1.80	2.40		I_F=100mA,tp=100 μs, t_p/T=0.01
		---	4.10	5.25		I_F=1A,tp=100 μs, t_p/T=0.01
verse Current	I_R	---	---	10	μA	V_R=5V
ew Angle	2θ1/2	----	17	----	deg	I_F=20mA

n Infrared LED

EL NO : HIR333

ypical Electrical/Optical/Characteristics Curves

Fig. 1 Forward Current vs. Ambient Temperature

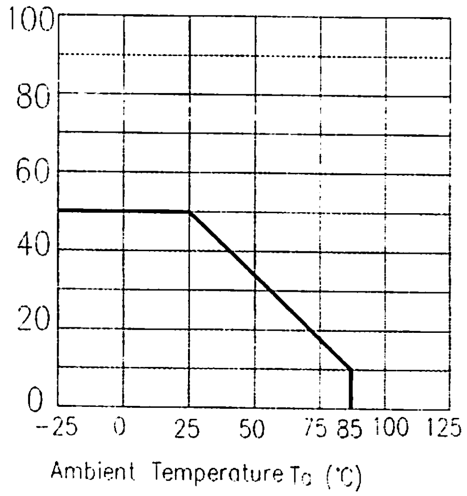


Fig. 2 Spectral Distribution

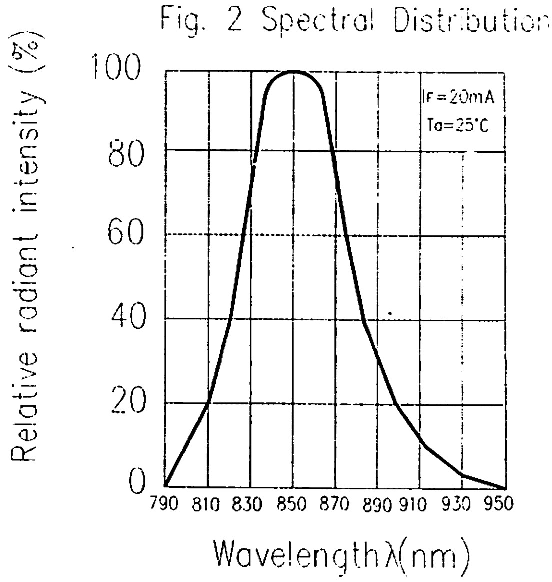


Fig. 3 Peak Emission Wavelength vs. Ambient Temperature

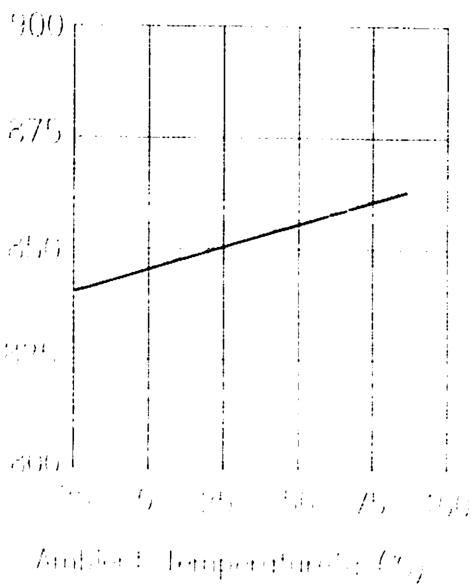
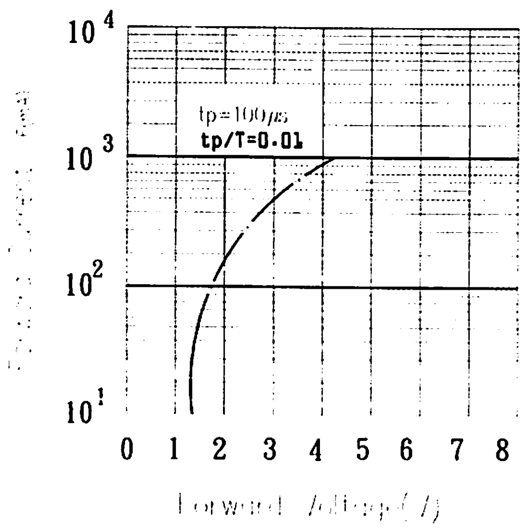


Fig. 4 Forward Current vs. Forward Voltage



n Infrared LED

)EL NO : HIR333

ypical Electrical/Optical/Characteristics Curves

Fig. 5 Relative Intensity vs. Forward Current

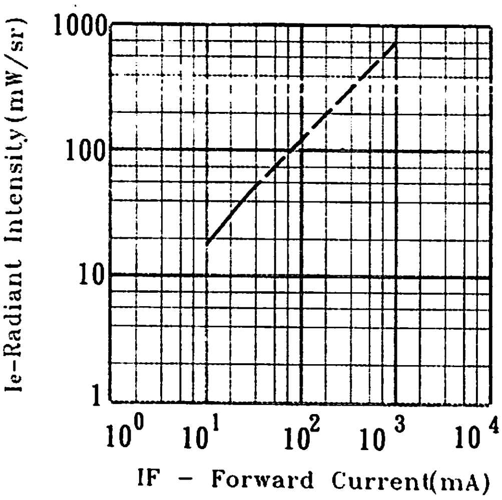


Fig. 6 Relative Radiant Intensity vs. Angular Displacement

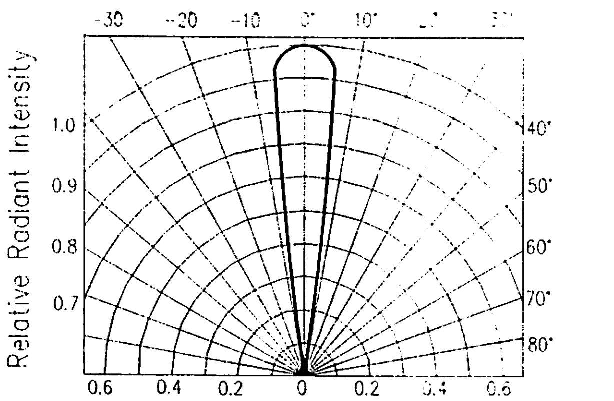


Fig. 7 Relative Intensity vs. Ambient Temperature (℃)

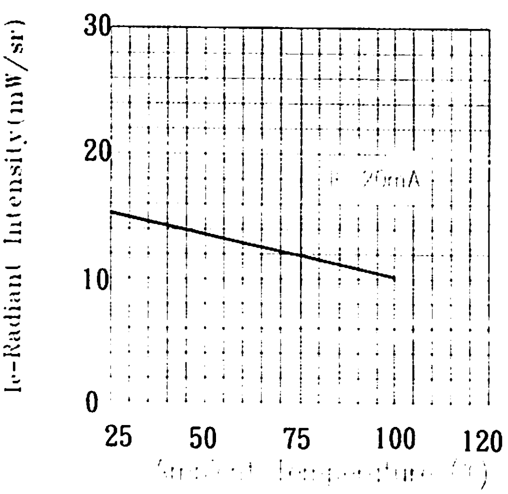
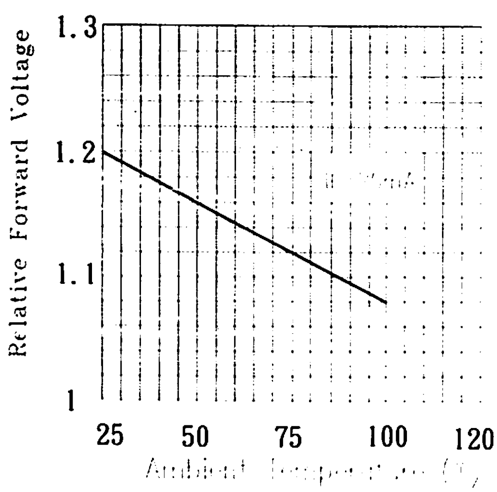


Fig. 8 Forward Current vs. Ambient Temperature (℃)



ı Infrared LED

EL NO : HIR333

■ Reliability Test Item And Condition

The reliability of products shall be satisfied with items listed below.
Confidence level:90%
LTPD:10%

NO.	Item	Test Conditions	Test Hours/ Cycles	Sample Size	Failure Judgement Criteria	Ac/Re
1	Solder Heat	TEMP : 260℃ ±5 ℃	5 secs	22 pcs	$I_R \geqq U \times 2$ $Ee \leqq L \times 0.8$ $V_F \geqq U \times 1.2$ U :Upper specification limit L :Lower specification limit	0/1
2	Temperature Cycle	H : +85℃ 30 mins ↕ 5 mins L : -55℃ 30 mins	50 cycles	22 pcs		0/1
3	Thermal Shock	H : +100℃ 5 mins ↕ 10 secs L : -10℃ 5 mins	50 cycles	22 pcs		0/1
4	High Temperature Storage	TEMP. : +100℃	1000 hrs	22 pcs		0/1
5	Low Temperature Storage	TEMP. : -55℃	1000 hrs	22 pcs		0/1
6	DC Operating Life	I_F=20mA	1000 hrs	22 pcs		0/1
7	High Temperature / High Humidity	85℃ / 85% R.H.	1000 hrs	22 pcs		0/1

n Infrared LED

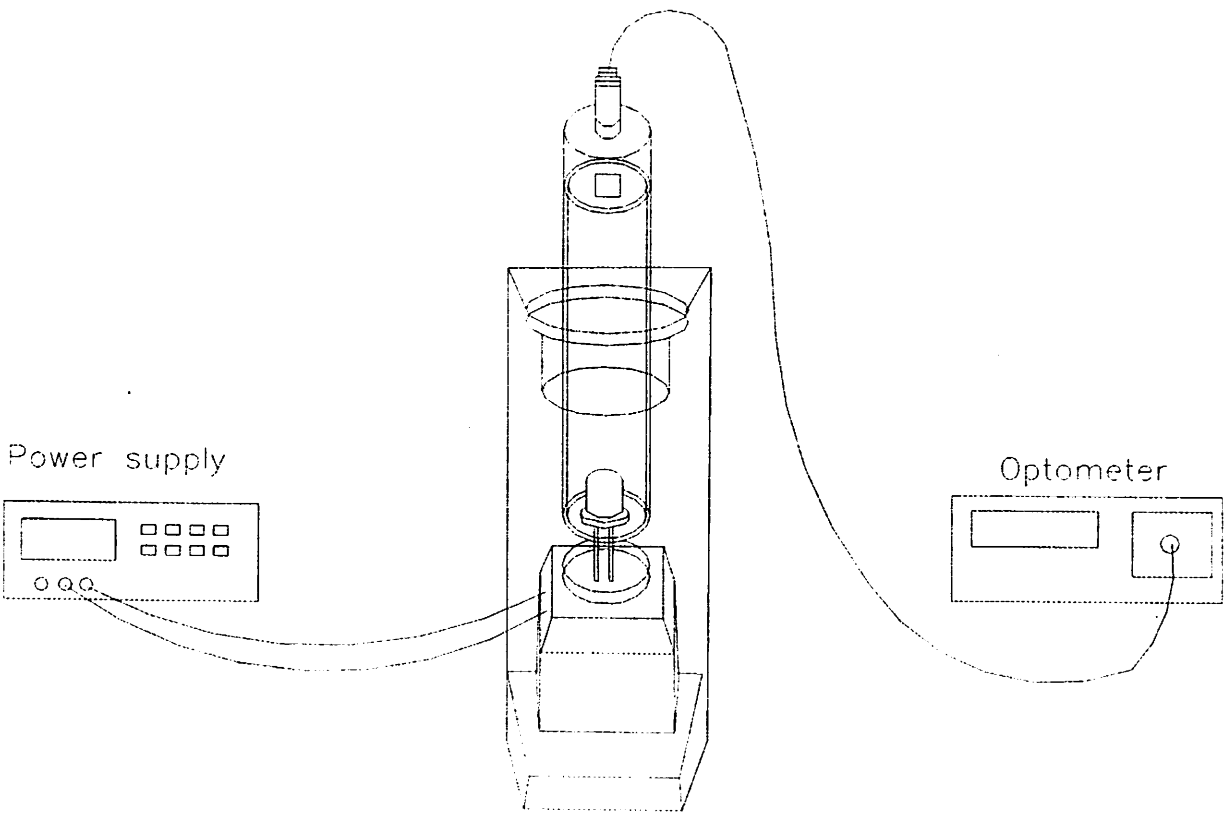
EL NO : HIR333

est Method For Power :

ondition : I_F=20 mA

est Item : Radiant Intensity

nit : mW/sr

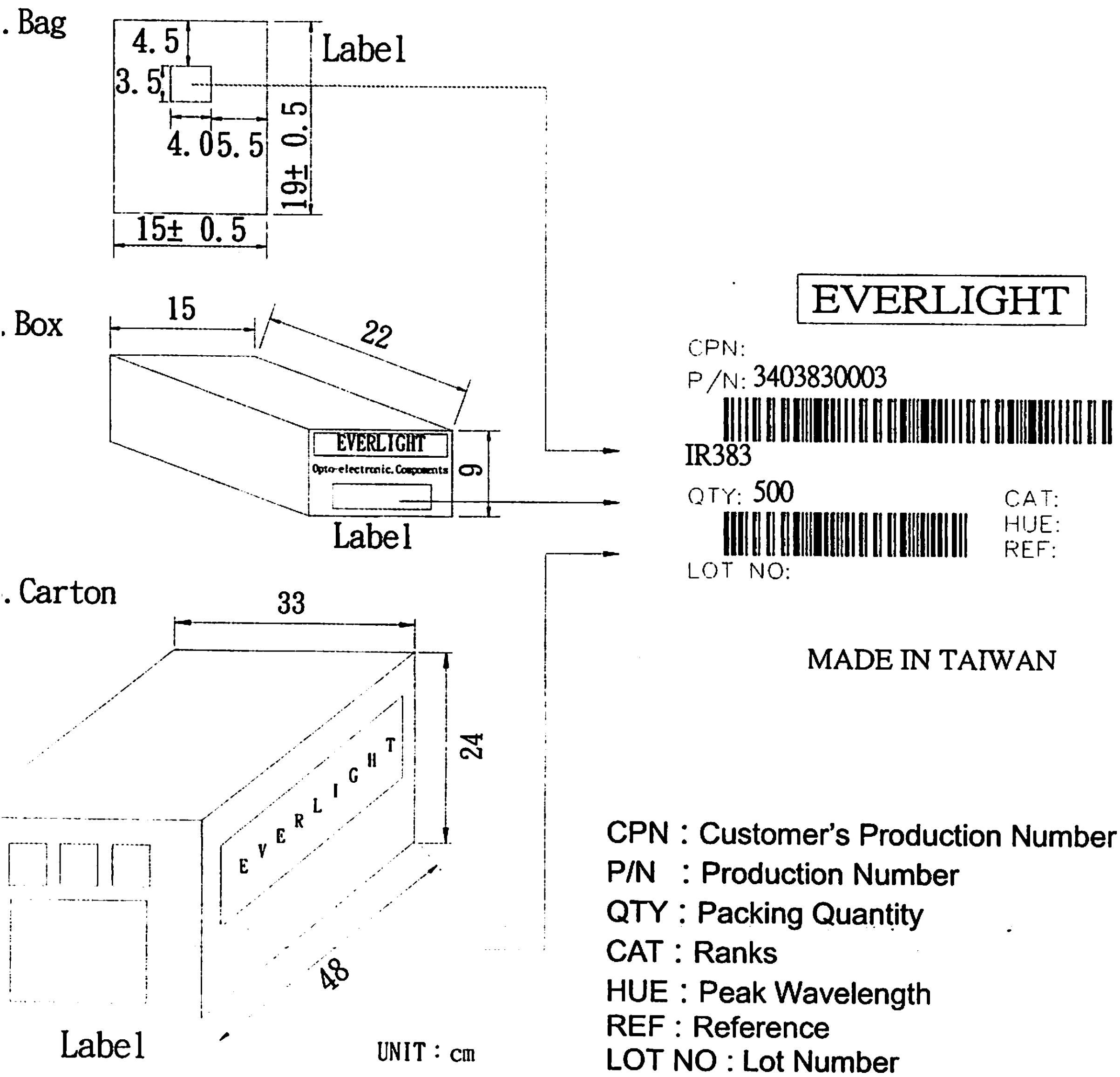


Bin Number	M	N	P	Q	R
Min	7.8	11.0	15.0	21.0	30
Max	12.5	17.6	24.0	34.0	48

n Infrared LED

EL NO : HIR333

acking Specifications



CPN : Customer's Production Number
P/N : Production Number
QTY : Packing Quantity
CAT : Ranks
HUE : Peak Wavelength
REF : Reference
LOT NO : Lot Number
MADE IN TAIWAN : Production place

acking Quantity Specification

0Pcs/1Bag，6 Bags/1Box
 Boxes/1Carton

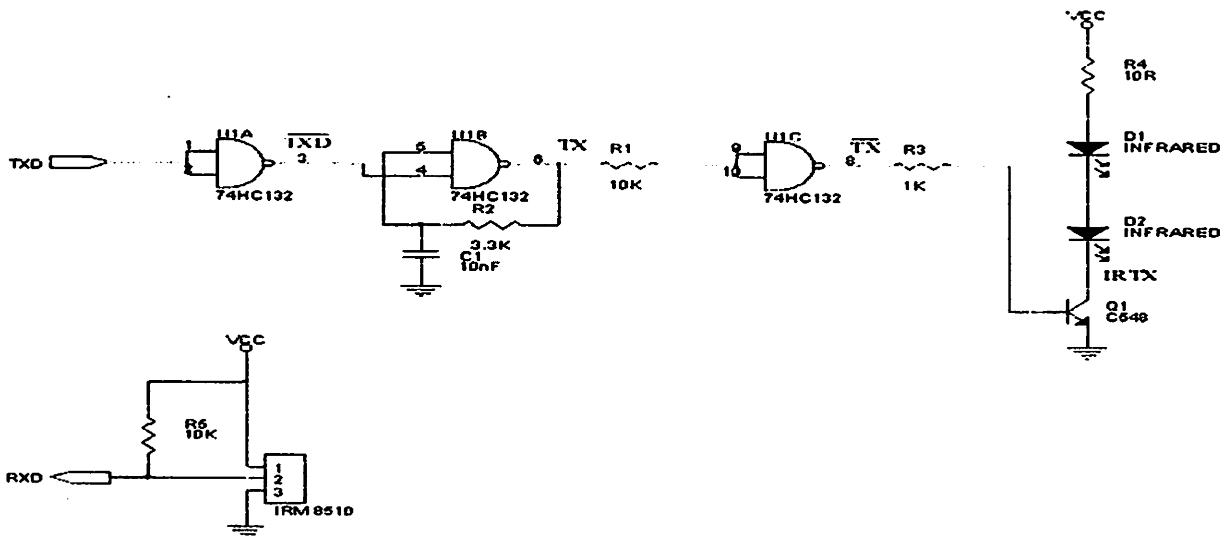
AN-006 INFRARED TRANSCEIVER

Infrared Transceiver adalah sebuah sistem yang terdiri dari Infrared Transmitter dan Infrared Receiver di mana sistem ini berfungsi untuk proses komunikasi data

Aplikasi

- Wireless Data Communication
- Alarm System
- Universal Remote Control

Deskripsi



Skema Infrared Transceiver

Untuk memperoleh jarak yang cukup jauh, Diode Infrared memerlukan sinyal dengan frekwensi 30 hingga 50 KHz. Berbeda dengan Diode LED yang hanya memerlukan level tegangan **DC** saja untuk mengaktifkan LED, Diode Infrared memerlukan sinyal **AC** dengan frekwensi **30** hingga **50 KHz** untuk mengaktifkannya. Cahaya infrared tersebut tidak dapat ditangkap oleh mata manusia, sehingga diperlukan **phototransistor** untuk mendeteksinya.

Phototransistor adalah merupakan sebuah transistor yang akan **saturasi** pada saat menerima sinar infrared dan **cut off** pada saat tidak ada sinar infrared. **IR Module** adalah sebuah rangkaian yang terdiri dari sebuah phototransistor dan filter yang terbentuk dalam satu modul di mana collector dari phototransistor adalah merupakan output dari modul ini. Pada saat phototransistor cut off maka tidak terjadi aliran arus dari **collector** menuju ke **emitter** sehingga collector yang merupakan output dari IR Module akan berkondisi high. Apabila phototransistor saturasi maka arus mengalir dari collector ke emitter dan output dari IR Module akan berkondisi low.

Transmisi data dilakukan dengan menggunakan prinsip aktif dan non aktifnya LED Infrared sebagai kondisi logic 0 dan logic 1. Seperti telah dijelaskan sebelumnya bahwa untuk mengaktifkan LED Infrared diperlukan frekwensi sebesar 30 hingga 40 KHz, maka dalam hal ini logic 0 berarti sinyal berfrekwensi 30 KHz mengalir ke LED Infrared dan logic 1 berarti tidak ada sinyal yang mengalir ke LED Infrared, hal ini seperti yang tampak pada hubungan antara TXD dan TX pada Timing Diagram berikut.

Untuk menghasilkan sinyal seperti yang tampak pada TX dibutuhkan sebuah rangkaian **modulator** yang terdiri dari sebuah gerbang dan rangkaian **R-C** sebagai **oscillator**. Gerbang tersebut menggunakan IC 74HC132 di mana pada saat pin TXD berkondisi high dan TXD berkondisi low maka output dari IC ini sesuai dengan tabel kebenaran yang ada pada data sheet adalah high. Namun bila sebaliknya TXD berkondisi high maka sesaat output dari IC ini berubah ke low sehingga capacitor C1 akan membuang muatannya melalui R1. Bila tegangan C1 terbuang hingga di bawah **tegangan ambang** 74HC132 maka input pin nomor 4 dari IC ini akan dianggap berkondisi low sehingga outputnya berubah menjadi high.

C1 kembali terisi melalui R1 hingga tegangan pada capacitor ini melebihi tegangan ambang dan input pin nomor 4 dianggap berkondisi high. Bila pada saat itu TXD masih berkondisi high maka output dari gerbang ini yaitu pin nomor 6 akan berkondisi low dan C1 kembali membuang, demikian seterusnya C1 akan terisi hingga di atas tegangan ambang 74HC132 (2,5 V) dan terbuang hingga di bawah tegangan ambang 74HC132 pula. Pengisian dan pembuangan pada C1 yang terjadi berkali-kali ini menyebabkan terjadinya osilasi dengan frekwensi yang dapat dihitung dengan menggunakan rumus berikut:

T = Waktu Pengisian C1 + Waktu Pembuangan C1

Waktu Pengisian C1 = Waktu Pembuangan C1 maka

T = 2 * Waktu Pengisian C1

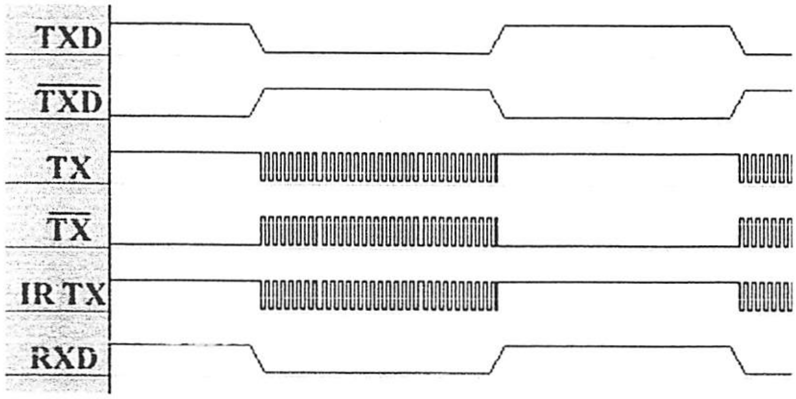
$$T = 2RC\left[\ln\left[\frac{Vs - VT-}{Vs}\right] - \ln\left[\frac{Vs - VT+}{Vs}\right]\right]$$

di mana VT- adalah batas bawah tegangan ambang 74HC132 yaitu sekitar 2 Volt dan VT+ adalah batas atas dari tegangan ambang 74HC132 yaitu sekitar 3 Volt. Dengan R sebesar 3,9K, C10nF dan Vsupply = 5Volt maka akan diperoleh harga T = 31,63 uS

$$F = \frac{1}{T}$$

F = 31,616 KHz

Jadi pada intinya apabila input TXD berkondisi high maka frekwensi oscillator sebesar 31,616 KHz yang terjadi pada pin nomor 4 akan dilewatkan ke outputnya dengan frekwensi yang sama persis, namun bila TXD berkondisi low maka osilasi pada pin nomor 4 akan berhenti dan output dari gerbang adalah high.



Timing Diagram

Ayunan sinyal berfrekwensi 31,6 KHz ini diperkuat lagi oleh gerbang lain dari 74HC132 yang dibentuk menjadi inverter dan diteruskan ke transistor BD400 yang mengalirkan sinyal-sinyal frekwensi hasil dari modulator tersebut ke Diode Infrared.

Pancaran Diode Infrared diterima oleh IR Module dan membuat output modul ini menjadi low hingga pancaran Diode Infared berhenti dan output dari modul menjadi high. Hasil output dari modul ini yaitu RXD seperti yang tampak pada timing diagram mempunyai bentuk gelombang yang sama persis dengan TXD.

Release September 2000 by Delta Electronic Group
Author: Paulus Andi Nalwan
Last Update October 2001

)hotodiodes

Features
- Low-cost visible and near-IR photodetector
- Excellent linearity in output photocurrent over 7 to 9 decades of light intensity
- Fast response times
- Available in a wide range of packages including epoxy-coated, transfer-molded, cast, and hermetic packages, as well as in chip form
- Low noise
- Mechanically rugged, yet compact and lightweight
- Available as duals, quads or as linear arrays
- Usable with almost any visible or near-infrared light source such as solid state laser diodes, neon, fluorescent, incandescent bulbs, lasers, flame sources, sunlight, etc.
- Can be designed and tested to meet the requirements of your application

Typical Applications
- Fiber-Optic Communications
- Instrumentation
- High-Speed Switching
- Spot Position Tracking and Measurement
- Photometry
- Data Transmission
- UV Light Meters
- Fluorescent Light Detection
- Laser Range Finding
- Barcode Scanning
- Laser Safety Scanning
- Distance Measurement

Datasheets available upon request

Description
PerkinElmer Optoelectronics offers a broad array of Silicon and InGaAs PIN and APDs.

InGaAs Avalanche Photodiodes
The high-quality InGaAs avalanche photodiodes (APDs) are packaged in hermetically sealed TO cans and ceramic blocks designed for the 900 to 1700 nm wavelength region.

InGaAs PIN Photodiodes
High-quality Indium Gallium Arsenide photodiodes designed for the 900 to 1700 nm wavelength region, these photodiodes are available in standard sizes ranging from 50 microns to 5 mm in diameter. Packages include ceramic submount, TO packages, and chip form.

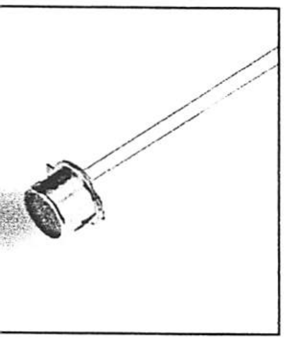
Silicon Avalanche Photodiodes
These are reliable, high-quality detectors in hermetically sealed TO packages designed for high-speed and high-gain applications. A "reach-through" structure is utilized which provides very low noise performance at high gains, and a full range of active areas is available.

Silicon PIN Photodiodes
Offered for low- to high-speed applications, these PINs are designed for the 250 nm to 1100 nm range. Standard sizes range from 100 microns to 10 mm in diameter.

Silicon PN Photodiodes
This format includes a variety of high-volume, low-cost silicon photodiodes that meet the demanding requirements of today's commercial and consumer markets.

Alternate Source/Second Source Photodiodes
PerkinElmer's nearest equivalent devices are selected on the basis of general similarity of electro-optical characteristics and mechanical configuration. Interchangeability in any particular application is not guaranteed, suitability should be determined by the customer's own evaluation.

Detector Modules
Preamplifier modules are hybrid devices with a photodiode and a matching amplifier in a compact hermetic TO package. An integral amplifier allows for better ease of use and noise bandwidth performance. 14-pin, DIL, and/or fibered packaged modules are available on a custom basis.



ım Gallium Arsenide
Photodiodes, Large-Area,
Small-Area
ım Gallium Arsenide APDs

igh Responsivity
ow Capacitance for High
andwidths
vailable in Various Hermetic
ackages

InGaAs APDs—900 nm to 1700 nm

Technical Specification

Part Number	Standard Package	Photo Sens. Diam. µm	Resp. A/W @1300 nm	Resp. A/W @1550 nm	Dark Curr. Id (nA)	Spect. Noise Curr. Dens. In (pA/√Hz)	Cap. @100 kHz Cd (pF)	Bandwidth GHz into 50 W	NEP @ 1550 nm pW/√Hz	VOP for Gain=10 V
C30644E	TO window	50	8.4	9.4	6	0.15	1	2	0.03	40-90
C30644ECER	Ceramic	50	8.4	9.4	6	0.15	0.8	2	0.03	40-90
C30645E	TO window	80	8.4	9.4	10	0.25	1.2	1	0.13	40-90
C30645ECER	Ceramic	80	8.4	9.4	10	0.25	1	1	0.13	40-90
C30662E	TO window	200	8.4	9.4	200	1.4	2.5	0.2	0.15	40-90
C30662ECER	Ceramic	200	8.4	9.4	200	1.4	2.5	0.2	0.15	40-90
C30733ECER	Ceramic	30	8.4	9.4	5	<0.1	0.25	3	0.01	40-90

Test conditions: T = 22°C

InGaAs PIN Large-Area—900 nm to 1700 nm

Technical Specification

Part Number	Standard Package	Photo Sens. Diam. mm	Resp. A/W @850 nm	Resp. A/W @1300 nm	Resp. A/W @1550 nm	Dark Curr. Id (nA)	NEP @ 1300 nm pW/√Hz	Cap. @100 kHz Cd (pF)	Bandwidth MHz into 50 W	Max. Power for .15 dB Linearity (dBm)	Bias Volt for these Specs V
C30619G	TO-18	0.5	0.2	0.86	0.95	5	<0.1	8	350	>+13	5
C30641G	TO-18	1	0.2	0.86	0.95	5	<0.1	40	75	>+13	2
C30642G	TO-5	2	0.2	0.86	0.95	10	0.1	350	20	+11	0
C30665G	TO-5	3	0.2	0.86	0.95	25	0.2	1000	3	+11	0
C30723G	TO-8	5	0.2	0.86	0.95	30	0.3	2500	2.5	+11	0

Test conditions: T = 22°C

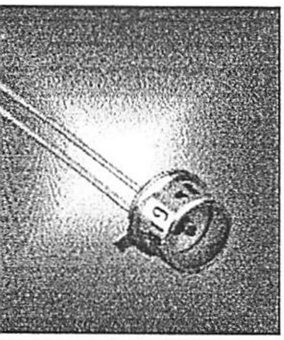
InGaAs PIN Small-Area—900 nm to 1700 nm

Technical Specification

Part Number	Standard Package	Photo Sens. Diam. µm	Resp. A/W @1300 nm	Resp. A/W @1550 nm	Dark Curr. Id (nA)	Spect. Noise Curr. Dens. In (pA/√Hz)	Cap. @100 kHz Cd (pF)	Bandwidth GHz into 50 W	NEP @ 1550 nm pW/√Hz	Bias Volt for these Specs V
C30616ECER	Ceramic	50	0.86	0.95	0.5	<0.02	0.35	>3.5	<0.02	5
C30637ECER	Ceramic	75	0.86	0.95	0.8	<0.02	0.4	3.5	<0.02	5
C30617ECER	Ceramic	100	0.86	0.95	1	<0.02	0.55	3.5	<0.02	5
C30617B	Ball lens	100	0.8	0.9	1	<0.02	0.8	3.5	<0.02	5
C30618ECER	Ceramic	350	0.86	0.95	2	0.02	4	0.8	0.02	5
C30618G	TO window	350	0.86	0.95	2	0.02	4	0.8	0.02	5

Test conditions: T = 22°C

photodiodes



on Avalanche Photodiodes
ermetically Sealed Packages

Si APD—Standard Types–400 nm to 1100 nm

Technical Specification

Part Number	Standard Package	Photo Sens. Diam. mm	Resp. 900 nm A/W	Dark Curr. Id (nA)	Spect. Noise Curr. Dens. In (pA/√Hz)	Cap. @100 kHz: Cd (pF)	Resp. Time tr (ns)	NEP @ 900 nm fW/√Hz	VOP Range V
C30817E	TO-5	0.8	75	50	0.5	2	2	7	275-425
C30872E	TO-8	3	45	100	0.5	10	2	11	275-425
C30902E	TO-18	0.5	77 (@ 830 nm)	15	0.23	1.6	0.05	3 (@ 830 nm)	180-250
C30902S	TO-18	0.5	128 (@ 830 nm)	15	0.11	1.6	0.05	0.86 (@ 830 nm)	180-250
C30916E	TO-5	1.5	70	100	0.5	3	2	8	275-425

Test conditions: T = 22°C

Si APD—Arrays Quadrant and Linear–400 nm to 1100 nm

Technical Specification

Part Number	Standard Package	Photo Sens. Diam. mm	Resp. @830 nm A/W	Dark Curr. Id (nA)	Spect. Noise Curr. Dens. In (pA/√Hz)	Cap. @100 kHz Cd (pF)	Resp. Time tr (ns)	NEP @ 830 nm fW/√Hz	VOP Range V
C30927E-01	TO-8	1.5 total	62 (@900 nm)	25	0.25	1	3	16 (@900 nm)	275-425
C30927E-02	TO-8	1.5 total	62 (@900 nm)	25	0.25	1	3	16 (@900 nm)	275-425
C30927E-03	TO-8	1.5 total	62 (@900 nm)	25	0.25	1	3	16 (@900 nm)	275-425
C30985E	Custom	0.3 pitch	31	1	0.1	0.5	2	3	250-425

Test conditions: T = 22°C

Si APD—Low Cost, High Volume–400 nm to 1000 nm

Technical Specification

Part Number	Standard Package	Photo Sens. Diam. mm	Resp. @900 nm A/W	Dark Curr. Id (nA)	Spect. Noise Curr. Dens. In (pA/√Hz)	Cap. @100 kHz Cd (pF)	Resp. Time tr (ns)	NEP @ 900 nm fW/√Hz	VOP Range V
C30724E	TO-18	0.5	9 (@ M=15)	25	0.1	1	5	11	120-200
C30724P	Plastic	0.5	9 (@ M=15)	25	0.1	1	5	11	120-200
C30737E	TO-18	0.5	47 (@ I-800 nm M=100)	20	0.3	2.5	0.3	6.4 (@ 800 nm M=100)	120-200

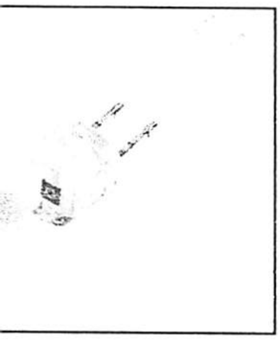
Test conditions: T = 22°C

Si APD—TE-Cooled

Technical Specification

Part Number	Standard Package	Photo Sens. Diam. mm	Resp. @830 nm A/W	Dark Curr. Id (nA)	Spect. Noise Curr. Dens. In (pA/√Hz)	Cap. @100 kHz Cd (pF)	Resp. Time tr (ns)	NEP @ 830 nm fW/√Hz	ADP VOP Range V
C30902S-TC	TO-66	0.5	128	2	0.04	1.6	0.5	0.3	160-250
C30902S-DTC	TO-66	0.5	128	1	0.02	1.6	0.5	0.16	160-250

Test conditions: T = 0°C for -TC and -20°C for -DTC   ADP VOP Range: temperature dependent



on Avalanche Photodiodes
w Cost, High Volume

Si APD—NIR-Enhanced–400 nm to 1100 nm

Technical Specification

Part Number	Standard Package	Photo Sens. Diam. mm	Resp. @1060 nm A/W	Dark Curr. Id (nA)	Spect. Noise Curr. Dens. In (pA/√Hz)	Cap. @100 kHz Cd (pF)	Resp. Time tr (ns)	NEP @ 900 nm m=15 fW/√Hz	VOP Range V
C30954E	TO-5	0.8	36	50	0.5	2	2	14	275-425
C30955E	TO-5	1.5	34	100	0.5	3	2	15	275-425
C30956E	TO-8	3	25	100	0.5	10	2	20	275-425

Test conditions: T = 22°C

Si APD—Lightpipe

Technical Specification

Part Number	Standard Package	Photo Sens. Diam. mm	Resp. @830 nm A/W	Dark Curr. Id (nA)	Spect. Noise Curr. Dens. In (pA/√Hz)	Cap. @100 kHz Cd (pF)	Resp. Time tr (ns)	NEP @ 830 nm fW/√Hz	VOP Range V
C30921E	TO-18	0.5	77	15	0.23	1.6	0.05	3	180-250
C30921S	TO-18	0.5	128	15	0.11	1.6	0.05	0.86	180-250

Test conditions: T = 22°C

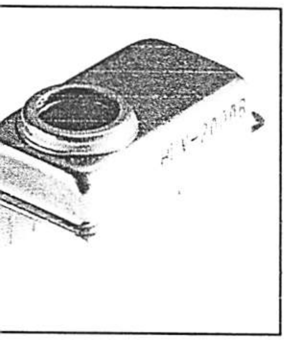
Si APD—Radiation Detection

Technical Specification

Part Number	Photo Sens. Diam. mm	Resp. A/W	Dark Curr. Id (nA)	Spect. Noise Curr. Dens. In (pA/√Hz)	Cap. @100 kHz Cd (pF)	Resp. Time tr (ns)	NEP @ Peak fW/√Hz	VOP Range V
C30626	5x5	22 (@900 nm)	250	0.5	30	5	23 (@900 nm)	275-425
C30703	10x10	16 (@530 nm)	10	0.7	120	5	40 (@530 nm)	275-425

Test conditions: T = 22°C

photodiodes



on PIN Photodiodes Modules

- road Range of Photosensitive reas
- ow Operating Voltage
- ermetically Sealed Packages

Si PINs—Window and Lightpipe Packages, Fast Response–400 nm to 1100 nm

Technical Specification

Part Number	Standard Package	Photo Sens. Diam. mm	Resp. @630 nm A/W	Dark Curr. Id nA	Spect. Noise Curr. Dens. In (fA/√Hz)	Cap. @100 kHz Cd (pF)	Resp. Time tr (ns)	NEP @ 830 nm fW/√Hz	Bias Volt for These Specs V
C30971E	TO-18	0.5	0.5	10	57	1.6	0.5	113	100
C30971EL	TO-18 Lightpipe	0.25	0.5	10	57	1.6	0.5	113	100

Test conditions: T = 22°C

Si PINs—Large Area, Fast Response–400 nm to 1100 nm

Technical Specification

Part Number	Standard Package	Photo Sens. Diam. mm	Resp. @900 nm A/W	Dark Curr. Id nA	Spect. Noise Curr. Dens. (fA/√Hz)	Cap. @100 kHz Cd (pF)	Resp. Time tr (ns)	NEP @ 900 nm fW/√Hz	Bias Volt for These Specs V
FFD-100	TO-5	2.5	0.58	2	25	8.5	3.5	44	15
FFD-200	TO-8	5.1	0.58	4	36	30	5	62	15

Test conditions: T = 22°C

Si PINs—Quadrant–220 nm to 1100 nm

Technical Specification

Part Number	Standard Package	Photo Sens. Diam. total mm	Resp. @900 nm A/W	Dark Curr. Id nA	Spect. Noise Curr. Dens. In (fA/√Hz)	Cap. @100 kHz Cd (pF)	Resp. Time tr (ns)	NEP @ 900 nm fW/√Hz	Bias Volt for These Specs V
C30845E	TO-5	8	0.6	7	47	8	6	79	45
UV-140BQ-4	TO-5	1.3x1.3 (x4)	0.58	—	4	34	<1 μsec	7	0
YAG-444-4A	Custom	11.4	0.4 @1.06 μm	40	118	9	25	295	180

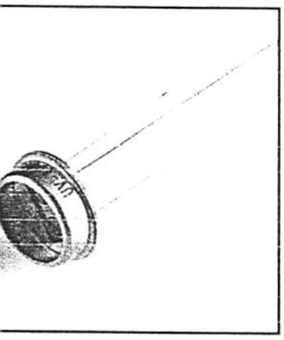
Test conditions: T = 22°C

Si PINs—Standard N-Type–400 nm to 1100 nm

Technical Specification

Part Number	Standard Package	Photo Sens. Diam. mm	Resp. @900 nm A/W	Dark Curr. Id nA	Spect. Noise Curr. Dens. In (fA/√Hz)	Cap. @100 kHz Cd (pF)	Resp. Time tr (ns)	NEP @ 900 nm fW/√Hz	Bias Volt for These Specs V
C30807E	TO-18	1	0.6	1	18	2.5	3	30	45
C30808E	TO-5	2.5	0.6	3	31	6	5	52	45
C30822E	TO-8	5	0.6	5	40	17	7	67	45
C30809E	TO-8	8	0.6	7	47	35	10	79	45
C30810E	Custom	11.4	0.6	30	98	70	12	163	45

Test conditions: T = 22°C



on PINs—UV Enhanced

Si PINs—UV Enhanced, Low Noise–220 nm to 1100 nm

Technical Specification

Part Number	Standard Package	Photo Sens. Diam. mm	Resp. A/W @250 nm	Resp. A/W @900 nm	Shunt Resis. Rd MW	Spect. Noise Curr. Dens.: In (fW/√Hz)	Cap. @100 kHz: Cd (pF)	NEP @ 900 nm fA/√Hz
UV-040BQ	TO-8	1	0.12	0.56	2000	3	25	5
UV-100BQ	TO-8	2.5	0.12	0.58	1000	4	120	7
UV-215BQ	TO-8	5.4	0.12	0.58	250	8	450	25
UV-245BQ	TO-8	4.4x4.7	0.12	0.58	375	7	375	20
UV-140BQ-2	TO-5	2.5x1.3 (x2)	0.12	0.56	1000	4	66	7
UV-140BQ-4	TO-5	1.3x1.3 (x4)	0.12	0.58	1000	4	34	7

Test conditions: T = 22°C

Si PIN Modules—Low Bandwidth–1 kHz to 50 kHz

Technical Specification

Part Number	Standard Package	Photo Sens. Diam. mm	Resp. MV/W @250 nm	Resp. MV/W @900 nm	Spect. Noise Volt. Dens. Vn (µV/√Hz)	NEP @ 900 nm pW/√Hz	Bandwidth kHz into 50 W	Bias Volt for These Specs V
HUV-2000B	Custom	5.4	24	116	2.5	0.02	2	0
HUV-1100BG	TO-5	2.5	24	116	20	0.17	20	0

Test conditions: T = 22°C

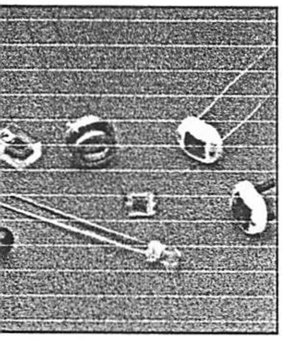
Si PIN Modules—High Bandwidth–40 MHz to 100 MHz

Technical Specification

Part Number	PIN or APD Used	Standard Package	Photo Sens. Diam. mm	Resp. kV/W @900 nm	Lin. Volt. Out Swing (V)	Spect. Noise Volt. Dens. Vn (nV/√Hz)	NEP @900 nm pW/√Hz	Bandwidth MHz (3 dB, into 50 W)	Photo. Diod. Bias Volt V
C30608E	C30971	TO-5	0.5	32 (@ 830 nm)	0.7	60	1.8 (@ 830 nm)	50	12
C30659-1550-R2A	C30662	TO-8	0.2	340 (@ 1550 nm)	2	35	0.103 (@ 1550 nm)	50	40-90
C30950E	C30817	TO-8	0.8	560	0.7	20	.036	50	275-425
C30919E	C30817	Custom	0.8	1000	0.7	25	.025	40	275-425

Test conditions: T = 22°C

photodiodes



on PN Photodiodes

e Key

	Short-Circuit Current
	H=100 fc, 2850 K
C	I_{SC} Temperature Coefficient, 2850 K
	Open-Circuit Voltage
	H=100 fc, 2850 K
OC	V_{OC} Temperature Coefficient, 2850 K
	Dark Current
	H=0, VR=10, 50, 100 V
	Shunt Resistance
	H=0, V=10 mV
	Junction Capacitance
	H=0, V=0, 3, 15 V
	Responsivity 880-940 nm
	Sensitivity @ Peak
	Spectral Application Range
	Spectral Response @ Peak
	Breakdown Voltage

e Key

	Short-Circuit Current
	H=1000 lux, 2850 K
C	I_{SC} Temperature Coefficient
	H=1000 lux, 2850 K
	Dark Current H=0, VR=100 mV
	ID Temperature Coefficient
	H=0, VR=100 mV
	Shunt Resistance
	H=0, VR=10 mV
	Junction Capacitance
	H=0, V=0 V, 1 MHz
	Sensitivity @ 400 nm
	Responsivity 400 nm, 0.18 A/W
	Rise/Fall Time @ 1 KΩ load
	VR=1 V, 830 nm
	Open-Circuit Voltage
	H=1000 lux, 2850 K
OC	V_{OC} Temperature Coefficient
	H=1000 lux, 2850 K

Silicon PN—VTP Series

Technical Specification

Part Number	I_{SC} µA	TC I_{SC} %/°C	V_{OC} mV	TC V_{OC} mV/°C	I_D nA max.	R_{SH} GΩ	C_J pF	Re A/(W/cm²)	S_R A/W	λ_{range} nm	λ_p nm	V_{BR} V
VTP100	55	0.24	300	-2	30	0.25	50 max.	0.047	0.5	725-1150	925	140
VTP100C	70	0.2	350	-2	30	0.25	50 max.	0.05	0.55	400-1150	925	140
VTP1012	17	0.2	350	-2	7	0.5	6 max.	0.011	0.55	400-1150	925	140
VTP1112	90	0.2	350	-2	7	0.5	6 max.	0.033	0.55	400-1150	925	140
VTP1188S	200	0.2	330	-2	30	67	180	—	0.55	400-1100	925	—
VTP1232	100 min.	0.2	420 min.	-2	25	—	180 max.	0.076	0.6	400-1100	920	—
VTP3310LA	36	0.2	350	-2	35	10	25 max.	0.015	0.55	400-1150	925	140
VTP3410LA	22	0.26	350	-2	35	10	25 max.	0.013	0.55	700-1150	925	140
VTP4085	200	0.2	330	-2	100	2	350	—	0.55	400-1100	925	—
VTP4085S	200	0.2	330	-2	50	4	350	—	0.55	400-1100	925	—
VTP5050	70	0.2	350	-2	18	0.25	24 max.	0.05	0.55	400-1150	925	140
VTP6060	200	0.2	350	-2	35	100	60 max.	0.14	0.55	400-1150	925	140
VTP7110	9	0.2	350	-2	35	7	25 max.	0.015	0.55	400-1150	925	140
VTP7210	7	0.26	350	-2	35	7	25 max.	0.015	0.55	700-1150	925	140
VTP7840	70	0.2	325	-2	20	0.25	40 max.	—	0.55	725-1150	925	1@10 mA
VTP8350	80	0.2	350	-2	30	100	50 max.	0.06	0.55	400-1150	925	140
VTP8440	55	0.2	350	-2	15	0.5	15 max.	0.025	0.55	400-1150	925	140
VTP8551	70	0.2	350	-2	30	0.15	50 max.	0.05	0.55	400-1150	925	140
VTP8651	55	0.24	300	-2	30	0.15	50 max.	0.045	0.5	725-1150	925	140
VTP9412	17	0.2	350	-2	7	0.4	6 max.	0.011	0.55	400-1150	925	140

Electro-optical characteristics @ 25°C

Silicon PN—VTS Series

Technical Specification

Part Number	I_{SC} mA	TC I_{SC} %/°C	I_D nA	TC I_D %/°C	R_{SH} MΩ	C_J nF	S_R A/W	Re A/(W/cm²)	t_R/t_F µsec	V_{OC} V	TC V_{OC} mV/°C
VTS 80	3	0.2	200	+11	0.3	7.5	0.2	0.7	13	0.45	-2.6
VTS 81	1.5	0.2	100	+11	0.6	3.5	0.2	0.34	6.4	0.45	-2.6
VTS 82	0.69	0.2	50	+11	1.2	1.75	0.2	0.16	3.4	0.45	-2.6
VTS 83	0.64	0.2	50	+11	1.2	1.75	0.2	0.15	3.4	0.45	-2.6
VTS 84	0.33	0.2	40	+11	1.5	1	0.2	0.07	1.8	0.45	-2.6
VTS 85	0.16	0.2	20	+11	3	0.5	0.2	0.04	1.2	0.45	-2.6
VTS 86	0.080	0.2	10	+11	6	0.25	0.2	0.02	0.75	0.45	-2.6

Electro-optical characteristics @ 25°C

e Key

Short-Circuit Current
940 nm, H=0.5 mW/cm^2 (VTD205, VTD206)
H=5 mW/cm^2, 2850 K (VTD31AA, VTB Series)
100 Lux, 2850 K (VTD34, VTD205K)
100 Lux, 2856 K (VTD206K)

C I_{SC} Temperature Coefficient
2850 K (VTD31AA, VTD34, VTD34F, VTB Series)
2856 K (VTD205, VTD205K, VTD206, VTD206K)

Open-Circuit Voltage
940 nm, H=0.5 mW/cm^2 (VTD 205, VTD205K, VTD206, VTD206K)
2850 K (VTD31AA, VTD34, VTD34F)

OC V_{OC} Temperature Coefficient
2850 K (VTD31AA, VTD34, VTD34F, VTB Series)
2856 K (VTD205, VTD205K, VTD206, VTD206K)

Dark Current
H=0, V_R=2 V (VTB Series)
H=0, V_R=10 V (VTD34, VTD34F, VTD205, VTD205K, VTD206, VTD206K, VTB100)
H=0, V_R=15 V (VTD31AA)

Shunt Resistance
H=0, V=10 mV (VTB Series)

SH R_{SH} Temperature Coefficient
H=0, V=10 mV (VTB Series)

Junction Capacitance
H=0, V_R=0 V, 1 MHz (VTD205, VTD205K, VTD206, VTD206K)
@ 1 MHz, V_R=0 V (VTD34, VTD34F)
H=0, V=0 V (VTD31AA, VTB Series)

Rise/Fall Time
@ RL=50 Ω, V_R=5 V, 850 nm (VTD205, VTD205K, VTD206, VTD206K)
@ RL=1 kΩ Lead, V_R=10 V, 833 nm (VTD34, VTD34F)

Sensitivity @ Peak
365 nm (VTB Series)

Spectral Application Range

Spectral Response @ Peak

Breakdown Voltage

Silicon PN—VTD Series

Technical Specification

Part Number	I_{sc} µA	TC I_{sc} %/°C	V_{oc} mV	TC V_{oc} mV/°C	I_D nA max.	C_J pF	t_R/t_F nsec	S_R A/W	λ_{range} nm	λ_p nm	V_{BR} V
VTD31AA	150-225	0.2	350	-2	50	500 max.	—	0.55	400-1150	860	5 min.
VTD34	70	0.2	365	-2	30	60	50	0.6	400-1100	900	40 min.
VTD34F	—	—	350	-2	30	60	50	0.6	725-1150	940	40 min.
VTD205	25	0.2	350	-2.6	30.	72	20	0.6	800-1100	925	50
VTD205K	80	0.2	365	-2.6	30	72	20	0.6	400-1100	925	50
VTD206	25	0.2	350	-2.6	30	72	20	0.6	750-1100	925	50
VTD206K	80	0.2	365	-2.6	30	72	20	0.6	400-1100	925	50

Electro-optical characteristics @ 25°C

Silicon PN—VTB Series

Technical Specification

Part Number	I_{sc} µA	TC I_{sc} %/°C	V_{oc} mV	TC V_{oc} mV/°C	I_D pA max.	R_{SH} GΩ	TC R_{SH} %/°C	C_J nF	S_R A/W	λ_{range} nm	λ_p nm	V_{BR} V
VTB100	65	0.12	490	-2	500	1.4	-8	2 max.	0.1	320-1100	920	40
VTB1012	13	0.12	490	-2	100	0.25	-8	0.31	0.09	320-1100	920	40
VTB1012B	1.3	0.02	420	-2	100	0.25	-8	0.31	—	330-720	580	40
VTB1013	13	0.12	490	-2	20	7	-8	0.31	0.09	320-1100	920	40
VTB1013B	1.3	0.02	420	-2	20	7	-8	0.31	—	330-720	580	40
VTB1112	60	0.12	490	-2	100	0.25	-8	0.31	0.19	320-1100	920	40
VTB1112B	6	0.02	420	-2	100	0.25	-8	0.31	—	330-720	580	40
VTB1113	60	0.12	490	-2	20	7	-8	0.31	0.19	320-1100	920	40
VTB1113B	6	0.02	420	-2	20	7	-8	0.31	—	330-720	580	40
VTB4051	200	0.12	490	-2	250	0.56	-8	3	0.1	320-1100	920	40
VTB5051	130	0.12	490	-2	250	0.56	-8	3	0.1	320-1100	920	40
VTB5051B	13	0.02	420	-2	250	0.56	-8	3	—	330-720	580	40
VTB5051J	130	0.12	490	-2	250	0.56	-8	3	0.1	320-1100	920	40
VTB5051UV	130	0.12	490	-2	250	0.56	-8	3	0.1	200-1100	920	40
VTB5051UVJ	130	0.12	490	-2	250	0.56	-8	3	0.1	200-1100	920	40
VTB6061	350	0.12	490	-2	2000	0.1	-8	8	0.1	320-1100	920	40
VTB6061B	35	0.02	420	-2	2000	0.1	-8	8	—	330-720	580	40
VTB6061CIE	12	—	—	—	2000	0.1	-8	8	—	475-650	555	—
VTB6061J	350	0.12	490	-2	2000	0.1	-8	8	0.1	320-1100	920	40
VTB6061UV	350	0.12	490	-2	2000	0.1	-8	8	0.1	200-1100	920	40
VTB6061UVJ	350	0.12	490	-2	2000	0.1	-8	8	0.1	200-1100	920	40
VTB8341	60	0.12	490	-2	100	1.4	-8	1	0.1	320-1100	920	40
VTB8440	45	0.12	490	-2	2000	0.07	-8	1	0.1	320-1100	920	40
VTB8440B	5	0.02	420	-2	2000	0.07	-8	1	—	330-720	580	40
VTB8441	45	0.12	490	-2	100	1.4	-8	1	0.1	320-1100	920	40
VTB8441B	5	0.02	420	-2	100	1.4	-8	1	—	330-720	580	40
VTB9412	13	0.12	490	-2	100	0.25	-8	0.31	0.09	320-1100	920	40
VTB9412B	1.3	0.02	420	-2	100	0.25	-8	0.31	—	330-720	580	40
VTB9413	13	0.12	490	-2	20	7	-8	0.31	0.09	320-1100	920	40
VTB9413B	1.3	0.02	420	-2	20	7	-8	0.31	—	330-720	580	40

WS

9014 NPN SILICON TRANSISTOR

TO—92

1.EMITTER

2.BASE

3.COLLECTOR 1 2 3

ATURES

'ower dissipation

P_{CM} : 0.4 W（Tamb=25℃）

:ollector current

I_{CM} : 0.1 A

:ollector-base voltage

$V_{(BR)CBO}$: 50 V

ECTRICAL CHARACTERISTICS（Tamb=25℃ unless otherwise specified）

Parameter	Symbol	Test conditions	MIN	TYP	MAX	UNIT
›llector-base breakdown voltage	$V(BR)_{CBO}$	Ic= 100 μA, I_E=0	50			V
›llector-emitter breakdown voltage	$V(BR)_{CEO}$	Ic= 0. 1 mA, I_B=0	45			V
nitter-base breakdown voltage	$V(BR)_{EBO}$	I_E= 100 μA, I_C=0	5			V
›llector cut-off current	I_{CBO}	V_{CB}=50 V, I_E=0			0.1	μA
›llector cut-off current	I_{CEO}	V_{CE}=35 V, I_B=0			0.1	μA
nitter cut-off current	I_{EBO}	V_{EB}= 3 V, I_C=0			0.1	μA
: current gain(note)	$H_{FE(1)}$	V_{CE}= 5 V, I_C= 1mA	60		1000	
›llector-emitter saturation voltage	$V_{CE}(sat)$	I_C= 100mA, I_B= 5 mA			0.3	V
ıse-emitter saturation voltage	$V_{BE}(sat)$	I_C= 100 mA, I_B= 5mA			1	V
ansition frequency	f_T	V_{CE}= 5 V, I_C= 10mA f =30MHz	150			MHz

LASSIFICATION OF $H_{FE(1)}$

:ank	A	B	C	D
:ange	60-150	100-300	200-600	400-1000

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00,000 Operations per Button
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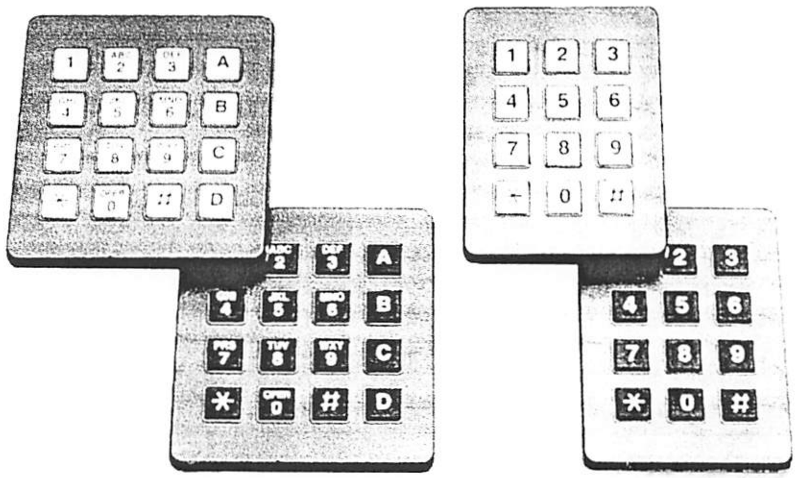
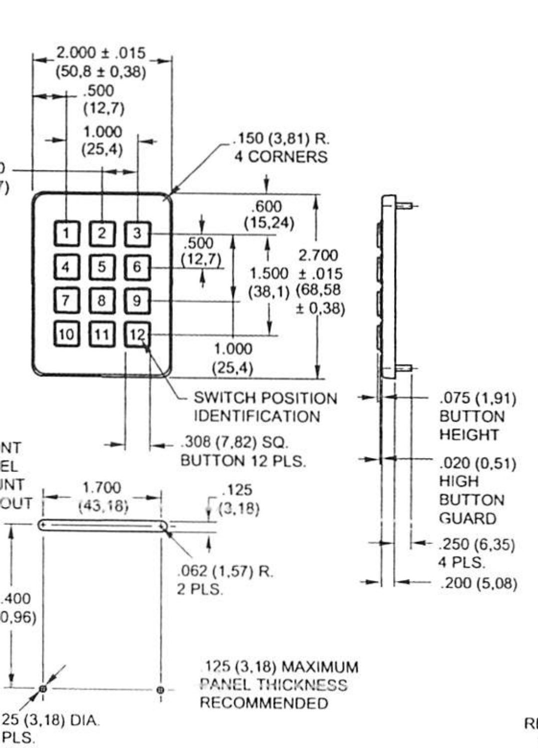
ic Inputs



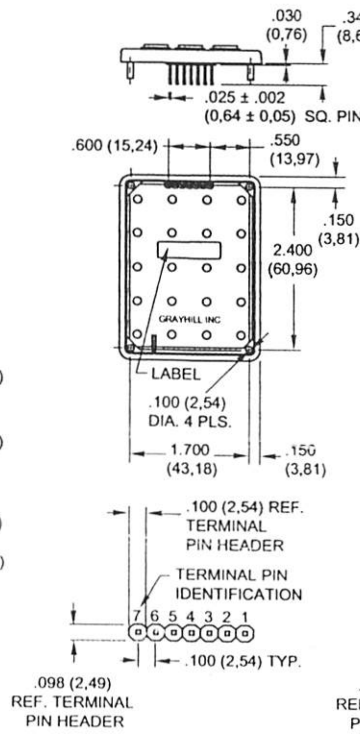
eries 96 is Grayhill's most economical 3x4 x4 keypad family. The contact system es conductive rubber to mate the priate PC board traces. Offered in matrix ry, with shielded and backlit options. Built uality component parts, the Series 96 is cted to our rigid statistical process control ure that it meets our reliability standards.

ENSIONS In inches (and millimeters)

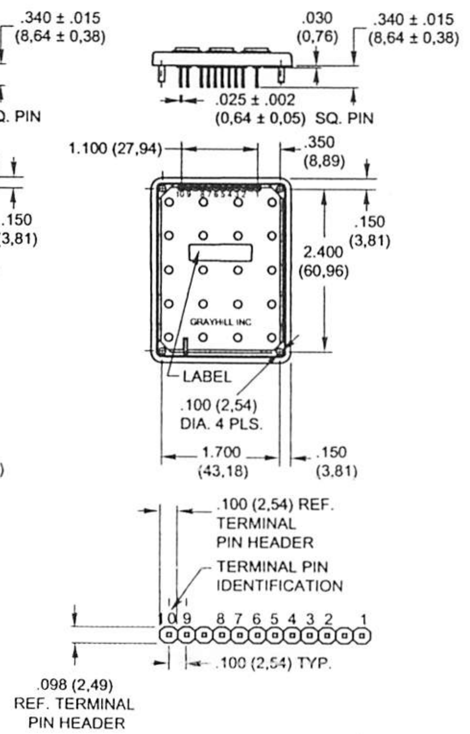
Front Mount Keyboard



Standard Versions



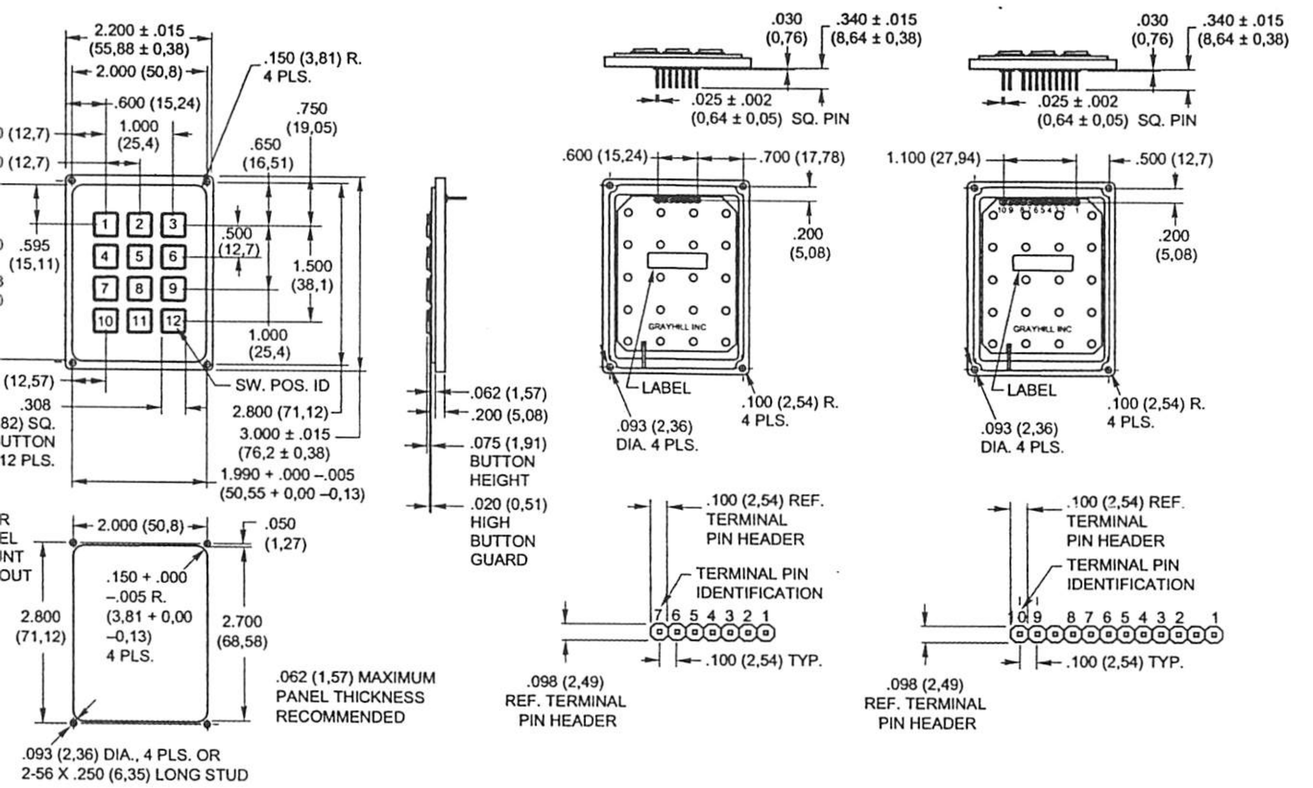
Shielded/Backlit Versions



...ENSIONS In inches (and millimeters)

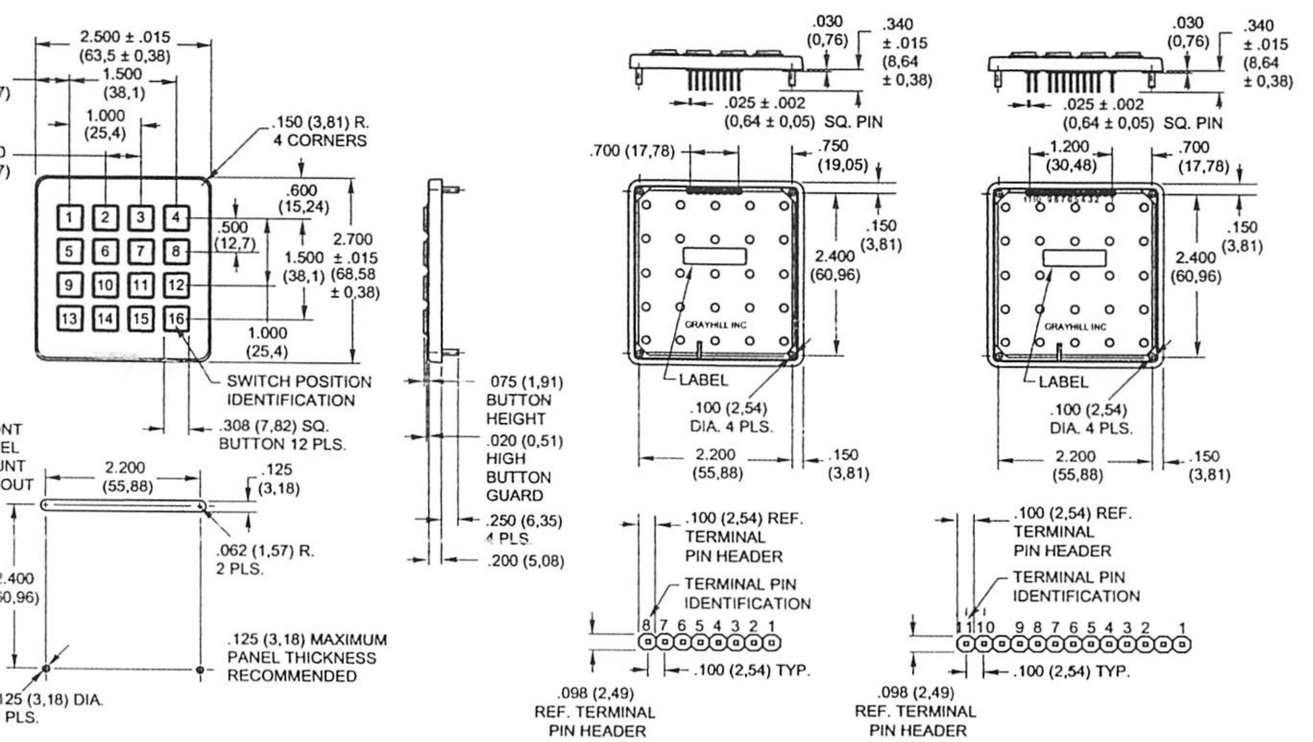
Rear Mount Keyboard

Standard Versions **Shielded/Backlit Versions**



Front Mount Keyboard

Standard Versions **Shielded/Backlit Versions**

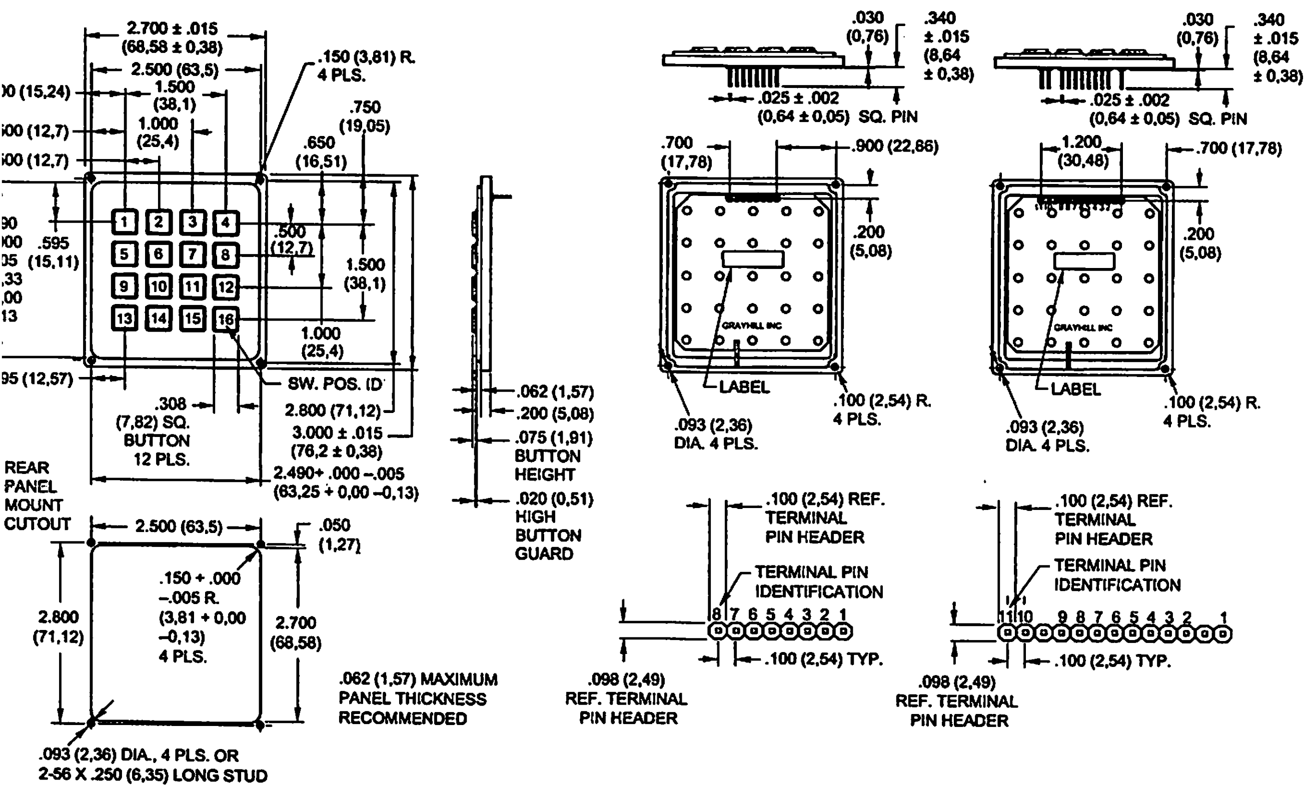


:NSIONS In inches (and millimeters)

Rear Mount Keyboard

Standard Versions

Shielded/Backlit Versions



E AND TRUTH TABLES

; in the chart indicate connected terminals when switch is closed.
ninals are identified on the keyboard.

12 Button Keypads

:4	MATRIX CODES																
	Standard							Shielded/Backlit									
	5	6	7	1	2	3	4	6	7	8	2	3	4	5	1	9	10
1	•			•				•			•						
2		•		•					•		•						
3			•	•						•	•						
4	•				•			•				•					
5		•			•				•			•					
6			•		•					•		•					
7	•					•		•					•				
8		•				•			•				•				
9			•			•				•			•				
10	•						•	•						•			
11		•					•		•					•			
12			•				•			•				•			

TERMINAL LOCATION

- Shielded keypad = Shielded
  Backlit keypad = NC
  Shielded and backlit keypad = Shielded
- Shielded keypad = NC
  Backlit keypad = EL Panel 1
  Shielded and backlit keypad = EL Panel 1
- Shielded keypad = NC
  Backlit keypad = EL Panel 2
  Shielded and backlit keypad = EL Panel 2

16 Button Keypads

4x4 BUTTON LOCATION	MATRIX CODES																		
	Standard								Shielded/Backlit										
	5	6	7	8	1	2	3	4	6	7	8	9	2	3	4	5	1	10	11
1	•				•				•				•						
2		•			•					•			•						
3			•		•						•		•						
4				•	•							•	•						
5	•					•			•					•					
6		•				•				•				•					
7			•			•					•			•					
8				•		•						•		•					
9	•						•		•						•				
10		•					•			•					•				
11			•				•				•				•				
12				•			•					•			•				
13	•							•	•							•			
14		•						•		•						•			
15			•					•			•					•			
16				•				•				•				•			

TERMINAL LOCATION

- Shielded keypad = Shielded
  Backlit keypad = NC
  Shielded and backlit keypad = Shielded
- Shielded keypad = NC
  Backlit keypad = EL Panel 1
  Shielded and backlit keypad = EL Panel 1
- Shielded keypad = NC
  Backlit keypad = EL Panel 2
  Shielded and backlit keypad = EL Panel 2

CI:'!CATIONS

g Criteria

g at 12 Vdc: 5 milliamps for .5 seconds
ct Bounce: < 12 milliseconds
ct Resistance: < 100 ohms (at stated ting force)
ge Breakdown: 250 Vac between onents
anical Operation Life: 1,000,000 tions per key
tion Resistance: > 10^{12} ohms @ 500 Vdc
Out Force Per Pin: 5 lbs.

ating Features

l: .040 minimum
ting Force: 175 ± 40 grams
ting Temperature: -30°C to +80°C

rial and Finishes

nal Pin: Phosphor bronze, solder-plated
oard: FR-4 glass cloth epoxy
d: Silicone rubber, durometer 50 ± 5
ng: ABS, cycolac "KJW"
ng Color: Black

Shielding Effectiveness

Results shown are typical for a standard Grayhill Series 84S keyboard. A conductive gasket will generally increase the shielding, depending on the size and shape of the gasket and its material. Data derived for E-Field Radiation.

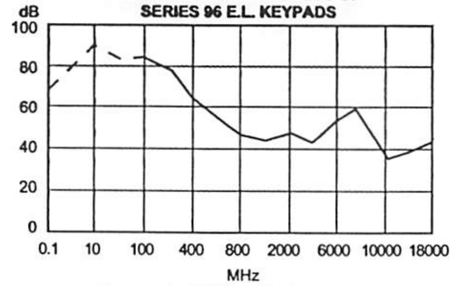
Test Method:

Measurements were made with the keyboard mounted to a brass plate, which in turn was mounted to a shielded enclosure containing the receiving equipment. A signal generator provided the frequency source that was radiated from the transmitting antenna to the enclosed receiving antenna. The spacing between antennas was maintained constant throughout the frequency range. The effectiveness rating is determined by establishing a reference reading without obstruction between the two antennas and determining the difference between that reading and the test setup reading.

Note:

When measured in actual equipment, shielding effectiveness is determined by many factors. This method accurately represents the shielding effectiveness of the Grayhill Series 84S under Ideal test conditions.

SHIELDING EFFECTIVENESS OF SERIES 96 E.L. KEYPADS



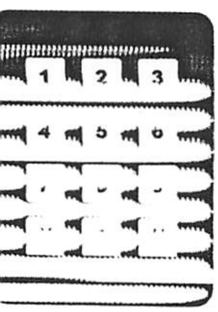
– – Represents shielding effectiveness greater than or equal to line.

Frequency M Hz	Rating in dB
0.1	≥ 66.2
10	≥ 94.8
100	90.5
400	64.2
800	42.3
2,000	40.5
6,000	33.1
10,000	34.4
18,000	37.0

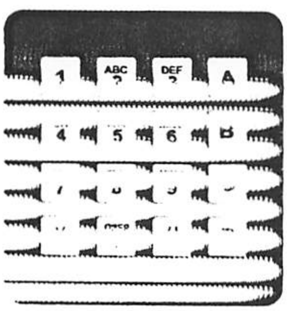
NDARD LEGENDS

ailable through Grayhill Distributors

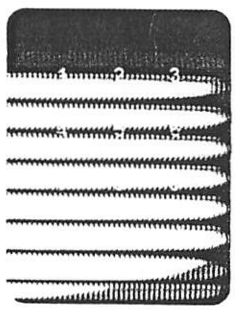
To order one of the configurations below, use the dash number shown here; select the keypad size and code, and order the part number with the appropriate legend dash number.



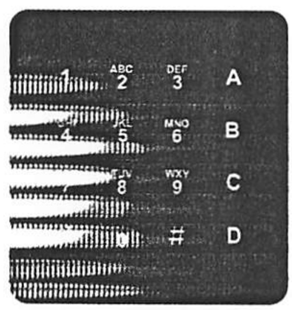
-102



-006



-152



-056

ERING INFORMATION

AB2-102-FS-EL

- **Grayhill Series Number**
- **Keyboard Size:** A = 3x4, B = 4x4
- **Circuitry:** B2 = Matrix (terminal pin header)
- **E.L. Panel Backlighting Option**
  EL = Backlit, Blank = Non-backlit
- **EMI/RFI Shielding Option**
  S = Shielded, Blank = Non-shielded
- **Mounting Option:** F = Front panel mount, R = Rear panel mount
- **Standard Legend Choices**
  12 Position legends
  102 = Black legends on a white button
  152 = White legends on a black button
  16 Position legends
  006 = Black legends on a white button
  056 = White legends on a black button

Available from your local Grayhill Distributor. For prices and discounts, contact a local Sales Office, an authorized local Distributor or Grayhill.

AN.No.1632-711E

LIQUID CRYSTAL DISPLAY MODULE

M 1 6 3 2

USER MANUAL

Seiko Instruments Inc.

PREFACE

This manual describes technical informations on functions and instructions of M1632 from Seiko Instruments Inc. Please read this instruction manual carefully to understand all the module functions and make the best use of them. Description details may be changed without notice.

Revision Record

Edition	Revision	Date
1	Original	April 1985
2	Completely revised	Jan. 1987

1. GENERAL

1.1 General

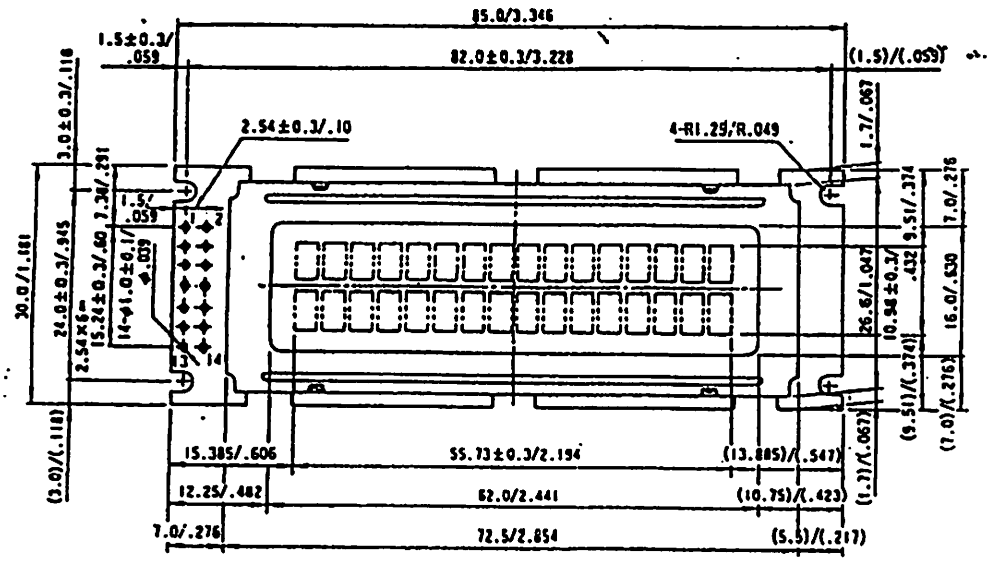
The M1632 is a low-power-consumption dot-matrix liquid crystal display (LCD) module with a high-contrast wide-view TN LCD panel and a CMOS LCD drive controller built in. The controller has a built-in character generator ROM/RAM, and display data RAM. All the display functions are controlled by instructions and the module can easily be interfaced with an MPU. This makes the module applicable to a wide range of purposes including terminal display units for microcomputers and display units for measuring gages.

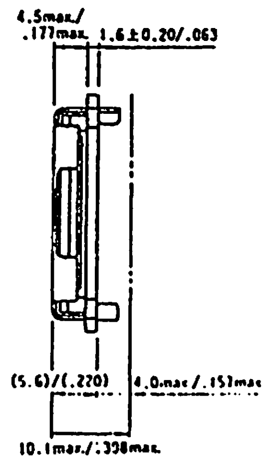
1.2 Features

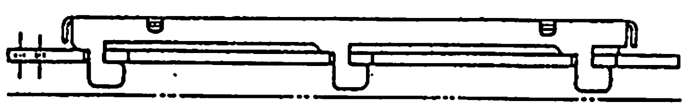
- 16-character, two-line TN liquid crystal display of 5 x 7 dot matrix + cursor
- Duty ratio: 1/16
- Character generator ROM for 192 character types.
  (character font: 5 x 7 dot matrix)
- Character generator RAM for eight character types (program write)
  (character font: 5 x 7 dot matrix)
- 80 x 8 bit display data RAM (80 characters maximum)
- Interface with four-bit and eight-bit MPUs possible
- Display data RAM and character generator RAM readable from MPU
- Many instruction functions

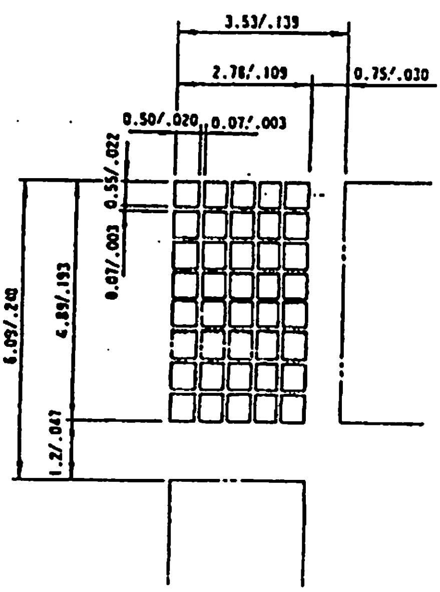
  Display Clear, Cursor Home, Display ON/OFF, Cursor ON/OFF, Display Character Blink, Cursor Shift, and Display Shift
- Built-in oscillator circuit
- +5 V single power supply
- Built-in automatic reset circuit at power-on
- CMOS process
- Operating temperature range: 0°C to 50°C

1.3 Dimensions Diagram







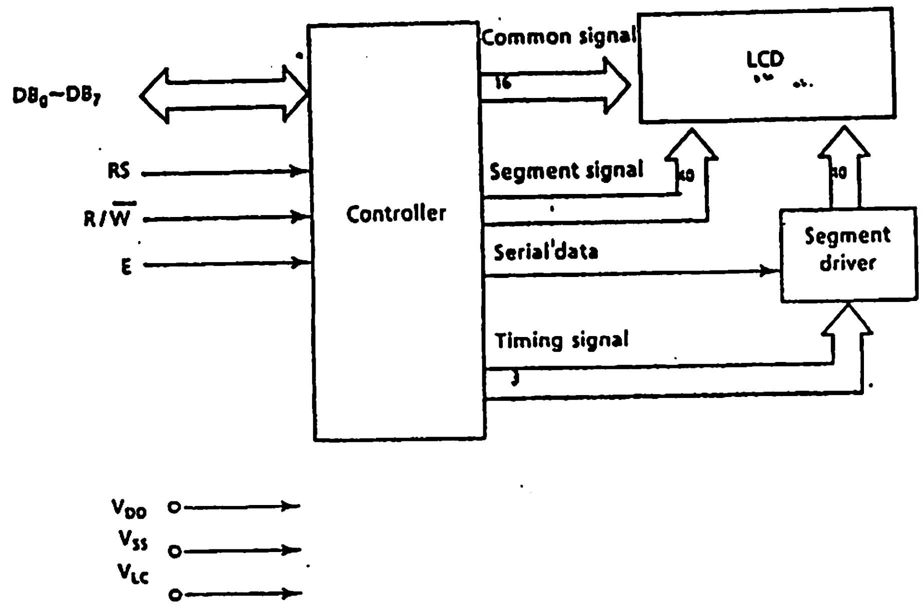


Unit : mm/inch
General tolerance : ±0.5 mm

No.	Symbol	Level	Function	
1	Vss	-	Power Supply	0V (GND)
2	Vcc	-		5V ±10%
3	Vee	-		for LCD Drive
4	RS	H/L	H: Data Input L: Instruction Input	
5	R/W	H/L	H:READ L:WRITE	
6	E	H, ⌐L	Enable Signal	
7	DB0	H/L	Data Bus	
8	DB1	H/L		
9	DB2	H/L		
10	DB3	H/L		
11	DB4	H/L		
12	DB5	H/L		
13	DB6	H/L		
14	DB7	H/L		
15	V+ BL	-	Back Light Supply	4 - 4.2V 50-200mA
16	V- BL	-		0V (GND)

Figure 1 Dimensions diagran

1.4 Block Diagram



1.5 Absolute Maximum Ratings

$V_{SS} = 0\,V$

Item	Symbol	Standard	Unit	Remarks
Power supply voltage	V_{DD}	-0.3 to $+7.0$	V	
	V_{LC}	$V_{DD}-13.5$ to $V_{DD}+0.3$	V	
Input voltage	V_{in}	-0.3 to $V_{DD}+0.3$,	V	
Operating temperature	T_{opr}	0 to +50	°C	
Storage temperature	T_{stg}	-20 to $+60$	°C	At 50% RH

1.6 Electrical Characteristics

$V_{DD} = 5\,V \pm 5\%$, $V_{SS} = 0\,V$, $T_A = 0°C$ to $50°C$

Item		Symbol	Conditions	Standard			Unit
				Min.	Typ.	Max.	
Input voltage	High	V_{IH1}		2.2	–	V_{DD}	V
	Low	V_{IL1}		0	–	0.6	V
Output voltage (TTL)	High	V_{OH1}	$-I_{OH} = 0.205$ mA	2.4	–	–	V
	Low	V_{OL1}	$I_{OL} = 1.2$ mA	–	–	0.4	V
Output voltage (CMOS)	High	V_{OH2}	$-I_{OH} = 0.04$ mA	$0.9V_{DD}$	–	–	V
	Low	V_{OL2}	$I_{OL} = 0.04$ mA	–	–	$0.1V_{DD}$	V
Power supply voltage		V_{DD}		4.75	5.00	5.25	V
		V_{LC}	$V_{DD} = 5\,V$, $T_A = 25°C$	–	0.25	–	V
Current consumption		I_{DD}		–	2.0	3.0	mA
		i_{LC}	$V_{LC} = 0.25V$	–	–	1.0	mA
Clock oscillation freq.		f_{osc}	Resistance oscillation	190	270	350	kHz

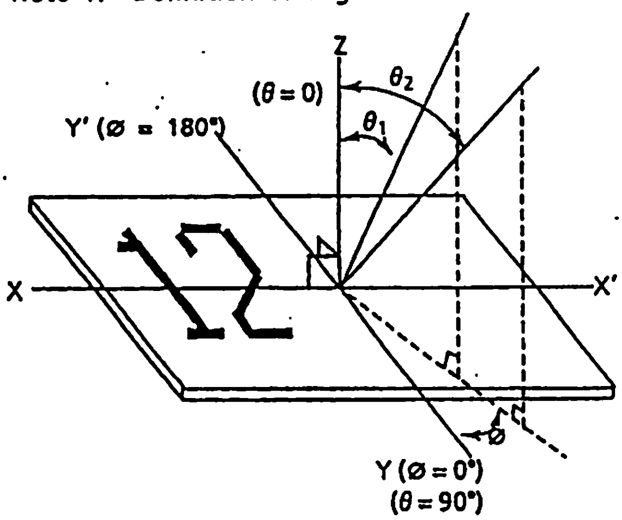
1.7 Optical Characteristics

1.7.1 Optical characteristics

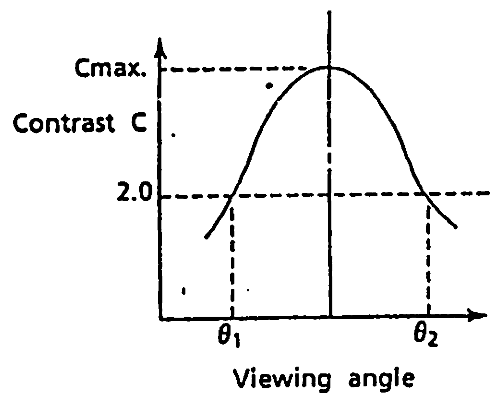
Maximum viewing angle: 6 o'clock (Ø = 0°)
T_A = 25°C, V_{opr} = 4.75 V

Item	Symbol	Conditions	Min.	Typ.	Max.	Remarks
Viewing angle	$\theta_2 - \theta_1$	C ≥ 2.0 , Ø = 0°	35	–	–	See Notes 1 and 2.
Contrast	C	θ = 25° , Ø = 0°	5	8	–	See Note 3.
Rise time	t_{on}	θ = 25° , Ø = 0°	–	60 ms	70 ms	See Note 4.
Fall time	t_{off}	θ = 25° , Ø = 0°	–	150 ms	170 ms	See Note 4.

Note 1: Definition of angles Ø and θ

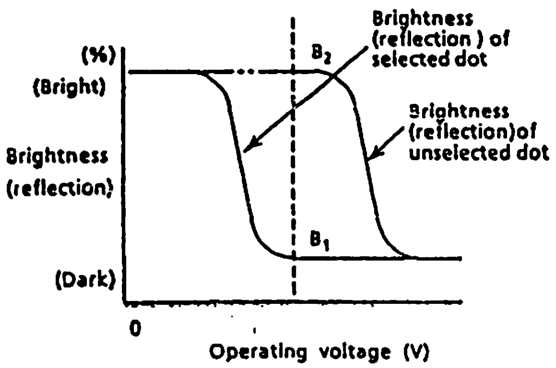


Note 2: Definition of viewing angles θ_1 and θ_2

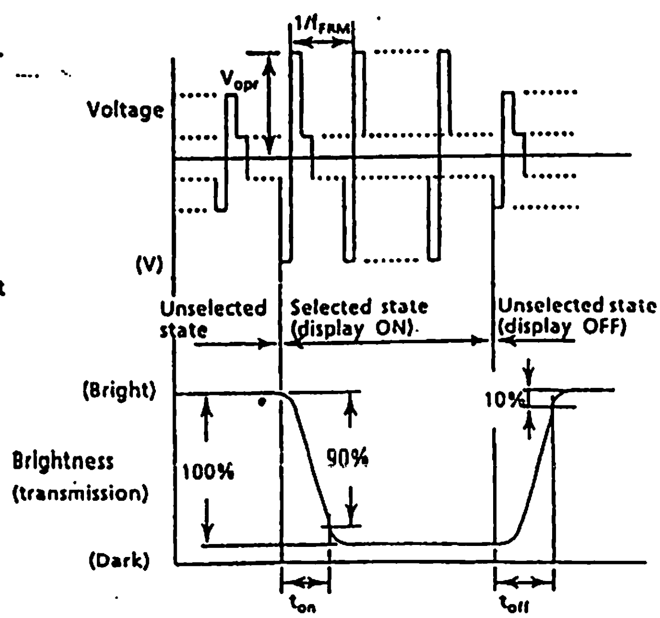


Note 3: Definition of contrast C

$$C = \frac{\text{Brightness (reflection) of unselected dot (B2)}}{\text{Brightness (reflection) of selected dot (B1)}}$$



Note 4: Definition of response time



V_{opr} : Operating voltage (V)
f_{FRM} : Frame frequency (Hz)
t_{on} : Response time (rise)(ms)
t_{off} : Response time (fall)(ms)

1.7.2 Recommended operating voltage

The viewing angle and screen contrast of the LCD panel can be varied by changing the liquid crystal operating voltage (V_{opr}), that is V_{LC}.

The optical characteristics is influenced by an ambient temperature. The recommended value of V_{opr} for an ambient temperatures are shown below.

Temperature (℃)	0	10	25	40	50
Voltage V_{opr} (V)	5.00	4.90	4.75	4.60	4.50

$V_{opr} = V_{DD} - V_{LC}$

2. OPERATING INSTRUCTIONS

2.1 Terminal Functions

Table 1 Terminal functions

Signal name	No. of terminals	I/O	Destination	Function
DB_0 to DB_3	4	I/O	MPU	Tristate bidirectional lower four data buses: Data is read from the module to the MPU or written to the module from the MPU through the buses. If the interface data is 4 bits, the signals are not used.
DB_4 to DB_7	4	I/O	MPU	Tristate bidirectional upper four data buses: Data is read from the module to the MPU or written to the module from the MPU through the buses. DB_7 is also used as a busy flag.
E	1	Input	MPU	Operation start signal: The signal activates data write or read.
R/$\overline{W}$	1	Input	MPU	Read (R) and Write ($\overline{W}$) selection signals 0 : Write 1 : Read
RS	1	Input	MPU	Register selection signals 0 : Instruction register (Write) Busy flag and address counter (Read) 1 : Data register (Write and Read)
V_{LC}	1	-	Power supply	Power supply terminal for driving liquid crystal display: The screen contrast can be varied by changing V_{LC}.
V_{DD}	1	-	Power supply	+5 V
V_{SS}	1	-	Power supply	Ground terminal: 0 V

2.2 Basic Operations

2.2.1 Registers

The controller has two kinds of eight-bit registers: the instruction register (IR) and the data register (DR). They are selected by the register select (RS) signal as shown in Table 2.

The IR stores instruction codes such as Display Clear and Cursor Shift, and the address information of display data RAM (DD RAM) and character generator RAM (CG RAM). They can be written from the MPU, but cannot be read to the MPU.

The DR temporarily stores data to be written into DD RAM or CG RAM, or read from DD RAM or CG RAM. When data is written into DD RAM or CG RAM from the MPU, the data in the DR is automatically written into DD RAM or CG RAM by internal operation. However, when data is read from DD RAM or CG RAM, the necessary data address is written into the IR. The specified data is read out to the DR and then the MPU reads it from the DR. After the read operation, the next address is set and DD RAM or CG RAM data at the address is read into the DR for the next read operation.

Table 2 Register selection

RS	R/$\overline{W}$	Operation
0	0	IR selection, IR write. Internal operation: Display clear
0	1	Busy flag (DB_7) and address counter (DB_0 to DB_6) read
1	0	DR selection, DR write. Internal operation : DR to DD RAM or CG RAM
1	1	DR selection, DR read. Internal operation : DD RAM or CG RAM to DR

2.2.2 Busy flag (BF)

The flag indicates whether the module is ready to accept the next instruction. As shown in Table 2, the signal is output to DB_7 if RS = 0 and R/$\overline{W}$ = 1. If the value is 1, the module is working internally and the instruction cannot be accepted. If the value is 0, the next instruction can be written. Therefore, the flag status needs to be checked before executing an instruction. If an instruction is executed without checking the flag status, wait for more than the execution time shown by 2.4 Instruction Outline.

2.2.3 Address counter (AC)

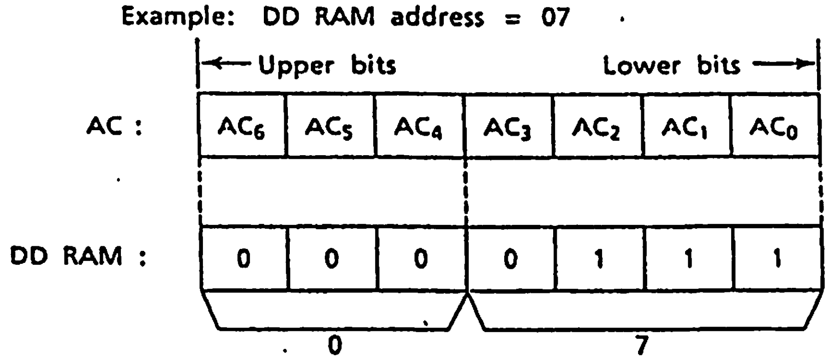
The counter specifies an address when data is written into DD RAM or CG RAM and the data stored in DD RAM or CG RAM is read out. If an Address Set instruction (for DD RAM or CG RAM) is written in the IR, the address information is transferred from the IR to the AC. When display data is written into or read from DD RAM or CG RAM, the AC is automatically incremented or decremented by one according to the Entry·Mode Set. The contents of the AC are output to DB_0 to DB_6 as shown in Table 2 if RS = 0 and $R/\overline{W}$ = 1.

2.2.4 Display data RAM (DD RAM)

DD RAM has a capacity of up to 80 × 8 bits and stores display data of 80 eight-bit character codes. Some storage areas of DD RAM which are not used for display can be used as general data RAM.

A DD RAM address to be set in the AC is expressed in hexadecimal form as follows.

Example: DD RAM address = 07



00_H to $0F_H$ of the DD RAM address is set in the line 1, and 40_H to $4F_H$ in the line 2.

Note : The addresses in the digit 16 of line 1 and the digit 1 of line 2 are not consecutive.

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	Display digit
Line 1	00	01	02	03	04	05	06	07	08	09	0A	0B	0C	0D	0E	0F	DD RAM address
Line 2	40	41	42	43	44	45	46	47	48	49	4A	4B	4C	4D	4E	4F	

If the display is shifted, DD RAM address 00_H to 27_H are displayed in line 1 and 40_H to 67_H in line 2. The following figures are examples of display shifts.

*Left shift

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	Display digit
Line 1	01	02	03	04	05	06	07	08	09	0A	0B	0C	0D	0E	0F	10	DD RAM address
Line 2	41	42	43	44	45	46	47	48	49	4A	4B	4C	4D	4E	4F	50	

*Right shift

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	Display digit
Line 1	27	00	01	02	03	04	05	06	07	08	09	0A	0B	0C	0D	0E	DD RAM address
Line 2	67	40	41	42	43	44	45	46	47	48	49	4A	4B	4C	4D	4E	

.2.5 Character generator ROM (CG ROM)

Character generator ROM generates 192 types of 5 x 7 dot-matrix character patterns from eight-bit character codes.

Table 3 shows the correspondence between the CG ROM character codes and character patterns.

.2.6 Character generator RAM (CG RAM)

CG RAM is used to create character patterns freely by programming. Eight types of character patterns can be written.

Table 4 shows the character patterns created from CG RAM addresses and data. To display a created character pattern, the character code in the left column of the table is written into DD RAM corresponding to the display position (digit). The areas not used for display are available as general data RAM.

Table 3 Correspondence between character codes and character patterns

Upper bit 4 bit / Lower bit 4 bit	0 0000	2 0010	3 0011	4 0100	5 0101	6 0110	7 0111	1010	1011	1100	1101	1110	1111
××××0000	CG RAM (1)		0	@	P	`	p		ー	タ	ミ	α	p
××××0001	(2)	!	1	A	Q	a	q	。	ア	チ	ム	ä	q
××××0010	(3)	"	2	B	R	b	r	「	イ	ツ	メ	β	θ
××××0011	(4)	#	3	C	S	c	s	」	ウ	テ	モ	ε	∞
××××0100	(5)	$	4	D	T	d	t	、	エ	ト	ヤ	μ	Ω
××××0101	(6)	%	5	E	U	e	u	・	オ	ナ	ユ	σ	ü
××××0110	(7)	&	6	F	V	f	v	ヲ	カ	ニ	ヨ	ρ	Σ
××××0111	(8)	'	7	G	W	g	w	ァ	キ	ヌ	ラ	g	π
××××1000	(1)	(	8	H	X	h	x	ィ	ク	ネ	リ	√	x̄
××××1001	(2)	)	9	I	Y	i	y	ゥ	ケ	ノ	ル	⁻¹	y
××××1010	(3)	*	:	J	Z	j	z	ェ	コ	ハ	レ	j	千
××××1011	(4)	+	;	K	[	k	{	ォ	サ	ヒ	ロ	ˣ	万
××××1100	(5)	,	<	L	¥	l	|	ャ	シ	フ	ワ	¢	円
××××1101	(6)	-	=	M	]	m	}	ュ	ス	ヘ	ン	£	÷
××××1110	(7)	.	>	N	^	n	→	ョ	セ	ホ	゛	ñ	
××××1111	(8)	/	?	O	_	o	←	ッ	ソ	マ	゜	ö	█

Table 4 Relationships between CG RAM addresses and character codes (DD RAM) and character patterns (CG RAM data)

Character code (DD RAM data) 7 6 5 4 3 2 1 0 ←Upper bit Lower bit→	CG RAM address 5 4 3 ←Upper bit	CG RAM address 2 1 0 Lower bit→	Character pattern (CG RAM data) 7 6 5 ←Upper bit	Character pattern (CG RAM data) 4 3 2 1 0 Lower bit→	
0 0 0 0 * 0 0 0	0 0 0	0 0 0	* * *	1 1 1 1 0	Example of character pattern (R)
		0 0 1		1 0 0 0 1	
		0 1 0		1 0 0 0 1	
		0 1 1		1 1 1 1 0	
		1 0 0		1 0 1 0 0	
		1 0 1		1 0 0 1 0	
		1 1 0		1 0 0 0 1	
		1 1 1	* * *	0 0 0 0 0	← Cursor position
0 0 0 0 * 0 0 1	0 0 1	0 0 0	* * *	1 0 0 0 1	Example of character pattern (¥)
		0 0 1		0 1 0 1 0	
		0 1 0		1 1 1 1 1	
		0 1 1		0 0 1 0 0	
		1 0 0		1 1 1 1 1	
		1 0 1		0 0 1 0 0	
		1 1 0		0 0 1 0 0	
		1 1 1	* * *	0 0 0 0 0	
		0 0 0	* * *		
		0 0 1			
0 0 0 0 * 1 1 1	1 1 1				
		1 0 0			
		1 0 1			
		1 1 0			
		1 1 1	* * *		

Notes:
- In CG RAM data, 1 corresponds to Selection and 0 to Non-selection on the display.
- Character code bits 0 to 2 and CG RAM address bits 3 to 5 correspond with each other (three bits, eight types).
- CG RAM address bits 0 to 2 specify a line position for a character pattern. Line 8 of a character pattern is the cursor position where the logical sum of the cursor and CG RAM data is displayed. Set the data of line 8 to 0 to display the cursor. If the data is changed to 1, one bit lights, regardless of the cursor.

The character pattern column positions correspond to CG RAM data bits 0 to 4 and bit 4 comes to the left end. CG RAM data bits 5 to 7 are not displayed but can be used as general data RAM.

When reading a character pattern from CG RAM, set to 0 all of character code bits 4 to 7. Bits 0 to 2 determine which pattern will be read out. Since bit 3 is not valid, 00_H and 08_H select the same character.

2.3 Timing Characteristics

2.3.1 Write timing characteristics

V_{DD} = 5.0 V ± 5%, V_{SS} = 0 V, T_A = 0°C to 50°C

Item		Symbol	Standard		Unit
			Min.	Max.	
Enable cycle time		t_{CYCE}	1000	–	ns
Enable pulse width	High level	PW_{EH}	450	–	ns
Enable rise and fall time		t_{Er}, t_{Ef}	–	25	ns
Setup time	RS, R/$\overline{W}$ — E	t_{AS}	140	–	ns
Address hold time		t_{AH}	10	–	ns
Data setup time		t_{DSW}	195	–	ns
Data hold time		t_H	10	–	ns

Write operation

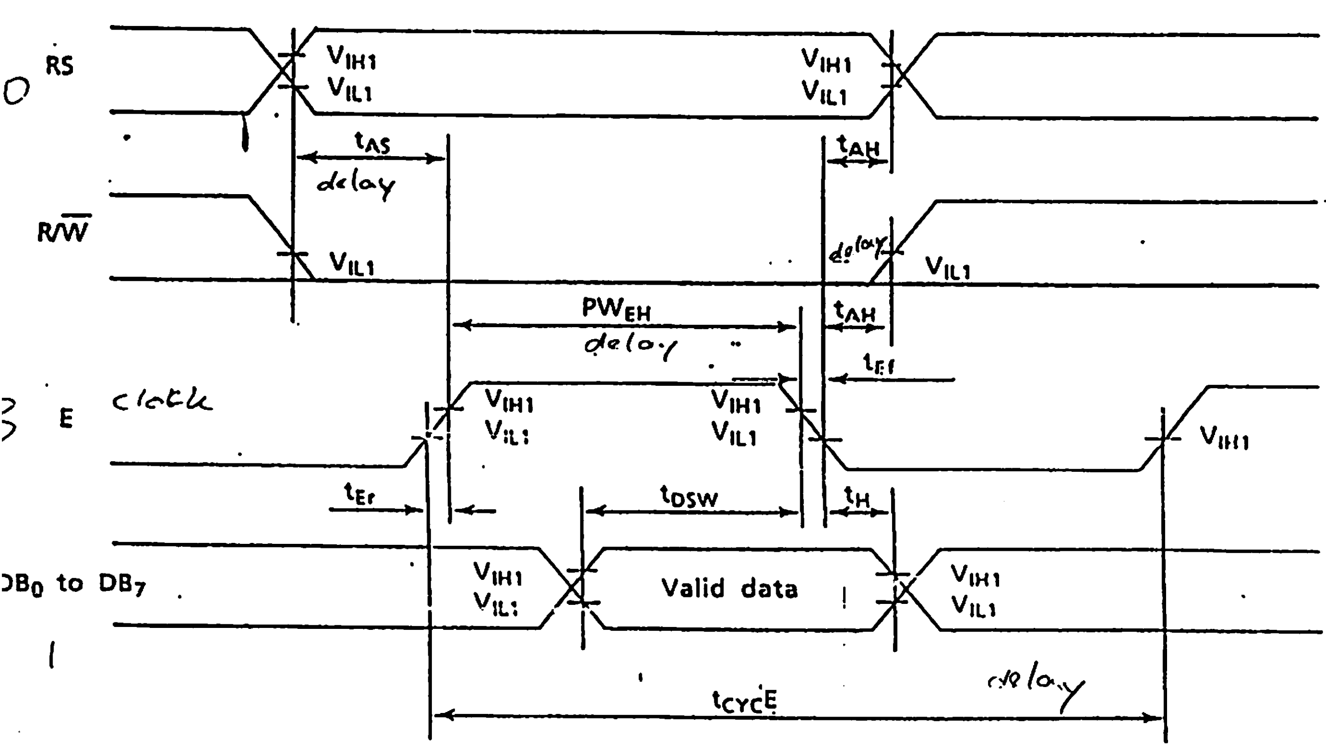


Figure 3 Data write from MPU to module

2.3.2 Read timing characteristics

$V_{DD} = 5.0\,V \pm 5\%$, $V_{SS} = 0\,V$, $T_A = 0°C$ to $50°C$

Item		Symbol	Standard		Unit
			Min.	Max.	
Enable cycle time		$t_{CYC}E$	1000	–	ns
Enable pulse width	High level	PW_{EH}	450	–	ns
Enable rise and fall time		t_{Er}, t_{Ef}	–	25	ns
Setup time	RS, R/$\overline{W}$—E	t_{AS}	140	–	ns
Address hold time		t_{AH}	10	–	ns
Data delay time		t_{DDR}	–	320	ns
Data hold time		t_H	20	–	ns

Read operation

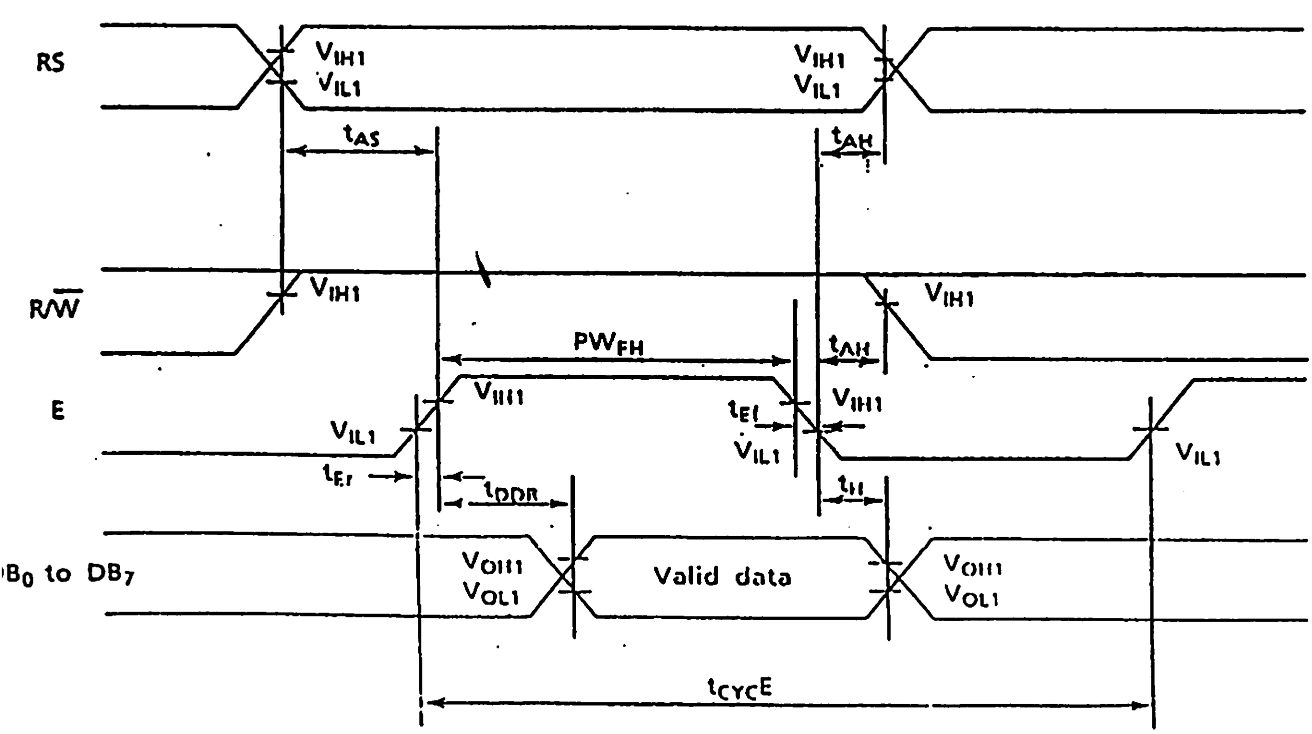


Figure 4 Data read from module to MPU

.4 Instruction Outline

Table 5 List of instructions

Instruction	Code RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	Function	Execution time
(1) Display clear	0	0	0	0	0	0	0	0	0	1	Clears all display and returns cursor to home position (address 0)	1.64 ms
(2) Cursor Home	0	0	0	0	0	0	0	0	1	*	Returns cursor to home position. Shifted display returns to home position and DD RAM contents do not change.	1.64 ms
(3) Entry Mode Set	0	0	0	0	0	0	0	1	I/D	S	Sets direction of cursor movement and whether display will be shifted when data is written or read	40 µs
(4) Display ON / OFF control	0	0	0	0	0	0	1	D	C	B	Turns ON/OFF total display (D) and cursor (C), and makes cursor position column start blinking (B)	40 µs
(5) Cursor/Display Shift	0	0	0	0	0	1	S/C	R/L	*	*	Moves cursor and shifts display without changing DD RAM contents	40 µs
(6) Function Set	0	0	0	0	1	DL	1	*	*	*	Sets interface data length (DL)	40 µs
(7) CG RAM Address Set	0	0	0	1	A_{CG}						Sets CG RAM address to start transmitting or receiving CG RAM data	40 µs
(8) DD RAM Address Set	0	0	1	A_{DD}							Sets DD RAM address to start transmitting or receiving DD RAM data	40 µs
(9) BF/Address Read	0	1	BF	AC							Reads BF indicating module in internal operation and AC contents (used for both CG RAM and DD RAM)	0 µs
(10) Data Write to CG RAM or DD RAM	1	0	Write Data								Writes data into DD RAM or CG RAM	40 µs
(11) Data Read from CG RAM or DD RAM	1	1	Read Data								Reads data from DD RAM or CG RAM	40 µs

* : Invalid bit
A_{CG} : CG RAM address
A_{DD} : DD RAM address

I/D = 1 : Increment
I/D = 0 : Decrement

S = 1 : Display shift
S = 0 : No display shift

D = 1 : Display ON
D = 0 : Display OFF

C = 1 : Cursor ON
C = 0 : Cursor OFF

B = 1 : Blink ON
B = 0 : Blink OFF

S/C = 1 : Display shift
S/C = 0 : Cursor movement

R/L = 1 : Right shift
R/L = 0 : Left shift

DL = 1 : 8 bits
DL = 0 : 4 bits

BF = 1 : Internal operation in progress
BF = 0 : Instruction can be accepted

Instruction Details

(1) Display Clear

	RS	R/$\overline{W}$	DB_7							DB_0
Code	0	0	0	0	0	0	0	0	0	1

Display Clear clears all display and returns cursor to home position (address 0).

Space code 20 (hexadecimal) is written into all the addresses of DD RAM, and DD RAM address 0 is set to the AC. If shifted, the display returns to the original position. After execution of the Display Clear instruction, the entry mode is incremented.

Note : When executing the Display Clear instruction, follow the restrictions listed in Table 6.

(2) Cursor Home

	RS	R/$\overline{W}$	DB_7							DB_0
Code	0	0	0	0	0	0	0	0	1	*

* : Invalid bit

Cursor Home returns cursor to home position (address 0).

DD RAM address 0 is set to the AC. The cursor returns to the home position. If shifted, the display returns to the original position. The DD RAM contents do not change. If the cursor or blinking is ON, it returns to the left side.

Note : When executing the Cursor Home instruction, follow the restrictions listed in Table 6.

Table 6 Restrictions on execution of Display Clear and Cursor Home instructions

Conditions of use	Restrictions
When executing the Display Clear or Cursor Home instruction when the display is shifted (after execution of Display Shift instruction)	The Cursor Home instruction should be executed again immediately after the Display Clear or Cursor Home instruction is executed. Do not leave an interval of a multiple of $400/f_{osc}$* second after the first execution. Example: 1.5 ms, 3 ms, 4.5 ms for f_{osc} = 270 kHz *f_{osc}: Oscillation frequency
When 23_H, 27_H, 63_H, or 67_H is used as a DD RAM address to execute Cursor Home instruction	Before executing the Cursor Home instruction, the data of the four DD RAM addresses given at the left should be read and saved. After execution, write the data again in DD RAM. (This restriction is necessary to prevent the contents of the DD RAM addresses from being destroyed after the Cursor Home instruction has been executed.)

(3) Entry Mode Set

	RS	R/$\overline{W}$	DB_7							DB_0
Code	0	0	0	0	0	0	0	1	I/D	S

Entry Mode Set sets the direction of cursor movement and whether display will be shifted.

I/D : The DD RAM address is incremented or decremented by one when a character code is written into or read from DD RAM. This is also true for writing into or reading from CG RAM.

When I/D = 1, the address is incremented by one and the cursor or blink moves to the right.

When I/D = 0, the address is decremented by one and the cursor or blink moves to the left.

S : If S = 1, the entire display is shifted either to the right or left for writing into DD RAM. The cursor position does not change, only the display moves. There is no display shift for reading from DD RAM.

When S = 1 and I/D = 1, the display shifts to the left.
When S = 1 and I/D = 0, the display shifts to the right.

If S = 0, the display does not shift.

(4) Display ON/OFF Control

	RS	R/$\overline{W}$	DB_7							DB_0
Code	0	0	0	0	0	0	1	D	C	B

Display ON/OFF Control turns the total display and the cursor ON and OFF, and makes the cursor position start blinking. Cursor ON/OFF and blinking is done at the column indicated by the specified DD RAM address by the AC.

D : When D = 1, the display is turned ON.
When D = 0, the display is turned OFF.
If D = 0 is used, display data remains in DD RAM. Change 0 to 1 to display data.

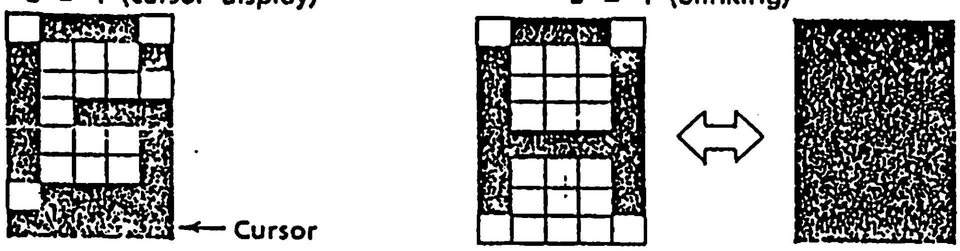
C : When C = 1, the cursor is displayed.
When C = 0, the cursor is not displayed.

The cursor is displayed in the dot line below the 5 x 7 dot-matrix character fonts. If the cursor is OFF, display data is written into DD RAM in the order specified by I/D.

B : When B = 1, the character at the cursor position starts blinking.
When B = 0, it does not blink.

For blinking, all-black dots and the character are switched about every 0.4 seconds. The cursor and blinking can be set at the same time.

Example: C = 1 (cursor display) B = 1 (blinking)



(5) Cursor/Display Shift

Code

RS	R/$\overline{W}$	DB_7							DB_0
0	0	0	0	0	1	S/C	R/L	*	*

* :Invalid bit

Cursor/Display Shift moves the cursor and shifts the display without changing the DD RAM contents.

The cursor position and the AC contents match. This instruction is available for display correction and retrieval because the cursor position or display can be shifted without writing or reading display data. Since the DD RAM capacity is 40-character and two lines, the cursor is shifted from digit 40 of line 1 to digit 1 of line 2. Displays of lines 1 and 2 are shifted at the same time. Therefore, the display pattern of line 2 is not shifted to line 1.

S/C	R/L	Operation
0	0	The cursor position is shifted to the left (the AC decrements one).
0	1	The cursor position is shifted to the right (the AC increments one).
1	0	The entire display is shifted to the left with the cursor.
1	1	The entire display is shifted to the right with the cursor.

Note: If only display shift is done, the AC contents do not change.

Function Set

	RS	R/$\overline{W}$	DB_7							DB_0
Code	0	0	0	0	1	DL	1	*	*	*

* : Invalid bit

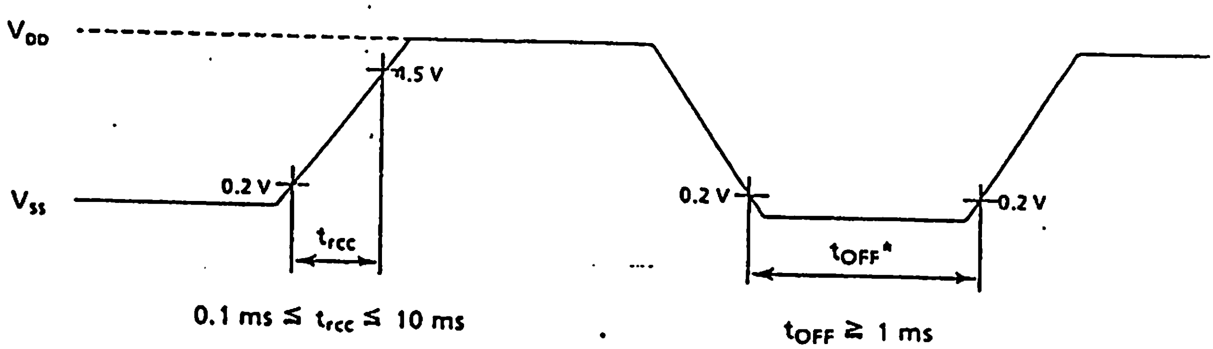
Function Set sets the interface data length.

DL : Interface data length
When DL = 1, the data length is set at eight bits (DB_7 to DB_0).
When DL = 0, the data length is set at four bits (DB_7 to DB_4).
The upper four bits are transferred first, then the lower four bits follow.

The Function Set instruction must be executed prior to all other instructions except for Busy Flag/Address Read. If another instruction is executed first, no function instruction except changing the interface data length can be executed.

Remarks: Initialization

The system is automatically initialized at power-on if the following power supply conditions are satisfied.



*t_{OFF}: Time when power supply is OFF if cut instantaneously or turned ON and OFF repeatedly

The following instructions are executed for initialization.

- 5 x 7 dot-matrix character font: 1/8 duty
- Display clear

· Function Set	DL = 1: Interface data length: 8 bits
· Display ON/OFF Control	D = 0: Display OFF C = 0: Cursor OFF B = 0: Blink OFF
· Entry mode	I/O = 1: Increment S = 0: No display shift

Since the condition is not suitable for the M1632, further function setting is necessary.

If automatic initialization is not executed because the above power supply conditions are not satisfied, use the instruction from next page on.

(a) **Interface data length : Eight bits**

Power-on

↓

Wait for 15 ms or more after V_{DD} reaches 4.5 V.

↓

RS	R/$\overline{W}$	DB_7	-	-	-	-	-	-	DB_0
0	0	0	0	1	1	*	*	*	*

The busy flag cannot be checked before the following instruction: Function Set (interface data length: 8 bits)

↓

Wait for 4.1 ms or more.

↓

RS	R/$\overline{W}$	DB_7	-	-	-	-	-	-	DB_0
0	0	0	0	1	1	*	*	*	*

The busy flag cannot be checked before the following instruction: Function Set (interface data length: 8 bits)

↓

Wait for 100 µs or more.

↓

RS	R/$\overline{W}$	DB_7	-	-	-	-	-	-	DB_0
0	0	0	0	1	1	*	*	*	*

The busy flag cannot be checked before the following instruction: Function Set (interface data length: 8 bits)

↓

RS	R/$\overline{W}$	DB_7	-	-	-	-	-	-	DB_0
0	0	0	0	1	1	1	*	*	*
0	0	0	0	0	0	1	0	0	0
0	0	0	0	0	0	0	0	0	1
0	0	0	0	0	0	0	1	I/D	S

The busy flag can be checked from the following instructions.

- Function Set
- Display OFF
- Display Clear
- Entry Mode Set

↓

End of initialization

(b) Interface data length: Four bits

Power-on

↓

Wait for 15 ms or more after V_{DD} reaches 4.5 V.

↓

RS	R/$\overline{W}$	DB_7	–	–	DB_4
0	0	0	0	1	1

The busy flag cannot be checked before the following instruction: Function Set (interface data length: 8 bits)

↓

Wait for 4.1 ms or more.

↓

RS	R/$\overline{W}$	DB_7	–	–	DB_4
0	0	0	0	1	1

The busy flag cannot be checked before the following instruction: Function Set (interface data length: 8 bits)

↓

Wait for 100 μs or more.

↓

RS	R/$\overline{W}$	DB_7	–	–	DB_4
0	0	0	0	1	1

The busy flag cannot be checked before the following instruction: Function Set (interface data length: 8 bits)

↓

RS	R/$\overline{W}$	DB_7	–	–	DB_4	
0	0	0	0	1	0	Function Set (interface data length: 4 bits)
0	0	0	0	1	0	Function Set
0	0	1	*	*	*	
0	0	0	0	0	0	Display OFF
0	0	1	0	0	0	
0	0	0	0	0	0	Display Clear
0	0	0	0	0	1	
0	0	0	0	0	0	Entry Mode Set
0	0	0	1	I/D	S	

The busy flag can be checked from the following instructions.

↓

End of initialization

(7) **CG RAM Address Set**

	RS	R/$\overline{W}$	DB_7							DB_0
Code	0	0	0	1	A	A	A	A	A	A

|←Upper bit Lower bit →|

CG RAM addresses expressed as binary AAAAAA are set to the AC. Then data in CG RAM is written from or read to the MPU.

(8) **DD RAM Address Set**

	RS	R/$\overline{W}$	DB_7							DB_0
Code	0	0	1	A	A	A	A	A	A	A

|←Upper bit Lower bit →|

DD RAM addresses expressed as binary AAAAAAA are set to the AC. Then data in DD RAM is written from or read to the MPU. The addresses used for display in line 1 (AAAAAAA) are 00_H to 27_H and those for line 2 (AAAAAAA) are 40_H to 67_H.

(9) **Busy Flag/Address Read**

	RS	R/$\overline{W}$	DB_7							DB_0
Code	0	1	BF	A	A	A	A	A	A	A

|←Upper bit Lower bit →|

The BF signal is read out, indicating that the module is working internally because of the previous instruction.

When BF = 1, the module is working internally and the next instruction cannot be accepted until the BF value becomes 0.

When BF = 0, the next instruction can be accepted.

Therefore, make sure that BF = 0 before writing the next instruction. The AC values of binary AAAAAAA are read out at the same time as reading the busy flag. The AC addresses are used for both CG RAM and DD RAM but the address set before execution of the instruction determines which address is to be used.

(10) Data Write to CG RAM or DD RAM

	RS	R/W̄	DB7							DB0
Code	1	0	D	D	D	D	D	D	D	D

|← Upper bit ... Lower bit →|

Binary eight-bit data DDDDDDDD is written into CG RAM or DD RAM. The CG RAM Address Set instruction of (7) or the DD RAM Address Set instruction of (8) before this instruction selects either RAM. After the write operation, the address and display shift are determined by the entry mode setting.

(11) Data Read from CG RAM or DD RAM

	RS	R/W̄	DB7							DB0
Code	1	1	D	D	D	D	D	D	D	D

|← Upper bit ... Lower bit →|

Binary eight-bit data DDDDDDDD is read from CG RAM or DD RAM. The CG RAM Address Set instruction of (7) or the DD RAM Address Set instruction of (8) before this instruction selects either RAM. In addition, either instruction (7) or (8) must be executed immediately before this instruction. If no address set instruction is executed before a read instruction, the first data read becomes invalid. If read instructions are executed consecutively, data is normally read from the second time. However, if the cursor is shifted by the Cursor Shift instruction when reading DD RAM, there is no need to execute an address set instruction because the Cursor Shift instruction does this.
After the read operation, the address is automatically incremented or decremented by one according to the entry mode, but the display is not shifted.

Note : The AC is automatically incremented or decremented by one according to the entry mode after a write instruction is executed to write data in CG RAM or DD RAM. However, the data of the RAM selected by the AC are not read out even if a read instruction is executed immediately afterwards.

Correct data is read out under the following conditions.

- An address set instruction is executed immediately before readout.
- For DD RAM, the Cursor Shift instruction is executed immediately before readout.
- The second, or later, instruction is executed in consecutive execution of read instructions.

6 Examples of Instruction Use

(1) Interface data length: Eight bits

No.	Instruction	Display	Operation
1	Power-on RS | R/$\overline{W}$ | DB_7 —— DB_0 / | / | /	(blank)	The built-in reset circuit initializes the module.
2	Function Set RS | R/$\overline{W}$ | DB_7 —— DB_0 0 | 0 | 0 0 1 1 1 * * *	(blank)	The interface data length is set to 8 bits. The character format becomes 5 x 7 dot-matrix at 1/16 duty cycle.
3	Display ON/OFF Control RS | R/$\overline{W}$ | DB_7 —— DB_0 0 | 0 | 0 0 0 0 1 1 1 0	_	The display and cursor are turned ON, but nothing is displayed.
4	Entry Mode Set RS | R/$\overline{W}$ | DB_7 —— DB_0 0 | 0 | 0 0 0 0 0 1 1 0	_	The address is incremented by one and the cursor shifts to the right in a write operation to internal RAM. The display is not shifted.
5	Write to CG RAM or DD RAM RS | R/$\overline{W}$ | DB_7 —— DB_0 1 | 0 | 0 1 0 0 1 1 0 0	L_	L is written. The AC is incremented by one and the cursor shifts to the right.
6	Write to CG RAM or DD RAM RS | R/$\overline{W}$ | DB_7 —— DB_0 1 | 0 | 0 1 0 0 0 0 1 1	LC_	C is written.
7	⋮	⋮	
8	Write to CG RAM or DD RAM RS | R/$\overline{W}$ | DB_7 —— DB_0 1 | 0 | 0 0 1 1 0 0 1 0	LCD MODULE M1632	2 is written in digit 16. Cursor disappears.

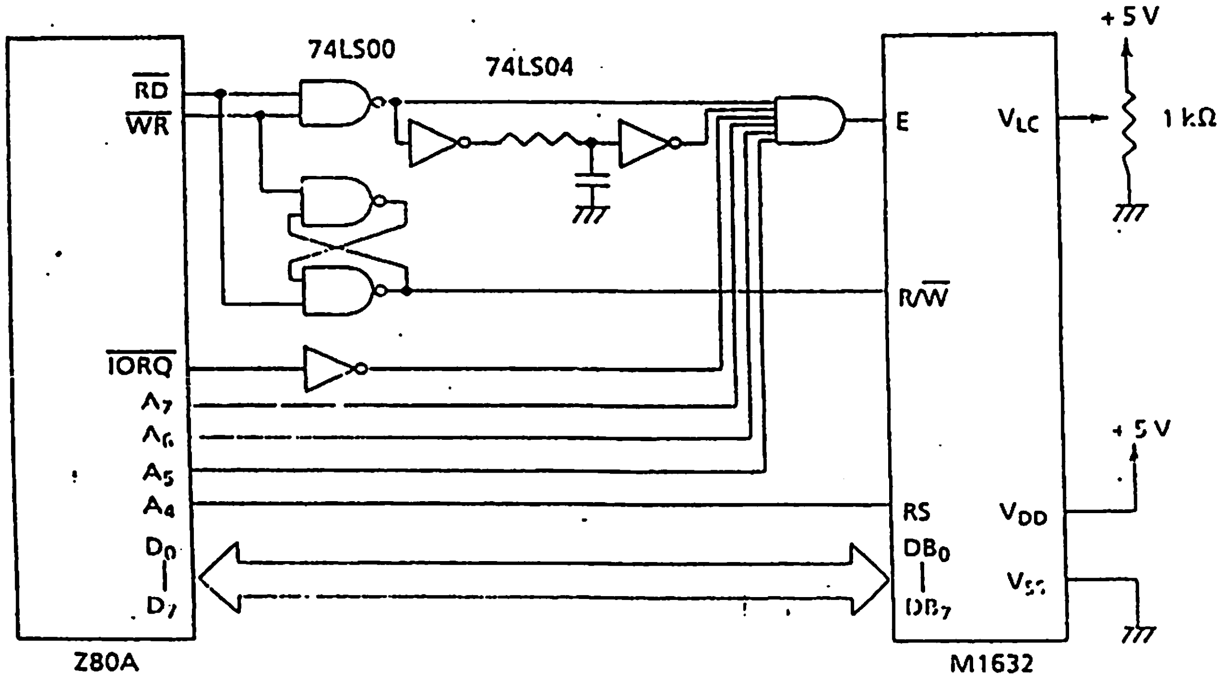
No.	Instruction	Display	Operation
9	DD RAM address set RS | R/W̄ | DB7 —— DB0 0 | 0 | 1 1 0 0 0 0 0 0	LCD MODULE M1632 _	The DD RAM address is set so that the cursor appears at digit 1 of line 2.
10	Write to CG RAM or DD RAM RS | R/W̄ | DB7 —— DB0 1 | 0 | 0 0 1 1 0 0 0 1	LCD MODULE M1632 1_	1 is written.
11	Write to CG RAM or DD RAM RS | R/W̄ | DB7 —— DB0 1 | 0 | 0 0 1 1 0 1 1 0	LCD MODULE M1632 16_	6 is written.
12	⋮	⋮	
13	Write to CG RAM or DD RAM RS | R/W̄ | DB7 —— DB0 1 | 0 | 0 1 0 1 0 0 1 1	LCD MODULE M1632 16DIGITS,2LINES	S is written.
14	DD RAM address set RS | R/W̄ | DB7 —— DB0 0 | 0 | 1 0 0 0 0 0 0 0	LCD MODULE M1632 16DIGITS,2LINES	The cursor returns to the home position.
15	Display clear RS | R/W̄ | DB7 —— DB0 0 | 0 | 0 0 0 0 0 0 0 1	_	All the display disappears and the cursor remains at the home position.
16	⋮	⋮	

(2) **Interface data length: Four bits**

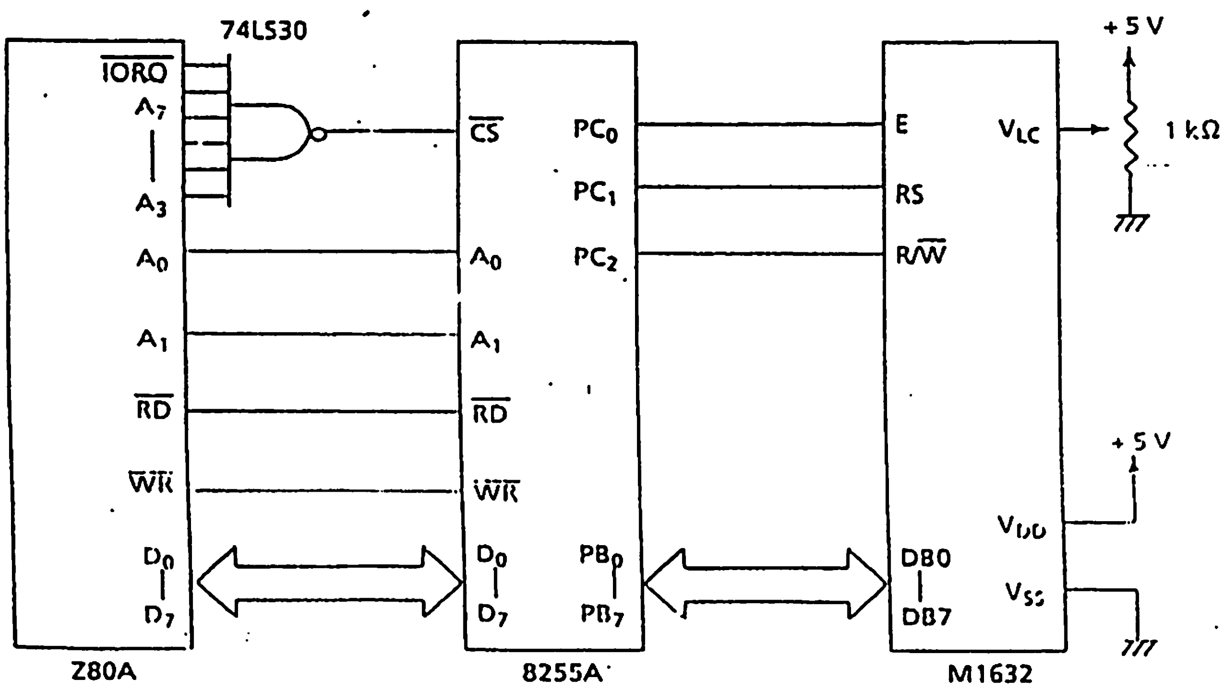
No.	Instruction	Display	Operation
1	Power-on RS | R/W | DB_7 — DB_4 / | / | /		The built-in reset circuit initializes the module.
2	Function Set RS | R/W | DB_7 — DB_4 0 | 0 | 0 0 1 0 / | / | /		Four-bit operation mode is set. *Eight-bit operation mode is set by initialization, and the instruction is executed only once.
3	Function Set RS | R/W | DB_7 — DB_4 0 | 0 | 0 0 1 0 0 | 0 | 1 * * *		The 4-bit operation mode, 1/16 duty cycle, and 5 x 7 dot-matrix character format are selected. Then 4-bit operation mode starts.
4	Display ON/OFF Control RS | R/W | DB_7 — DB_4 0 | 0 | 0 0 0 0 0 | 0 | 1 1 1 0	_	The display and cursor are turned ON, but nothing is displayed.
5	Entry Mode Set RS | R/W | DB_7 — DB_4 0 | 0 | 0 0 0 0 0 | 0 | 0 1 1 0	_	The address is incremented by one and the cursor shifts to the right in a write operation to internal RAM. The display is not shifted.
6	Write to CG RAM or DD RAM. RS | R/W | DB_7 — DB_4 1 | 0 | 0 1 0 0 1 | 0 | 1 1 0 0	L_	L is written. the AC is incremented by one and the cursor shifts to the right.

MPU Connection Diagrams

2.7.1 Z80A



2.7.2 Z80A and 8255A



:ERAL DESCRIPTION

ivated, sensitive gate triacs in a c envelope, intended for use in ral purpose bidirectional hing and phase control cations, where high sensitivity is red in all four quadrants.

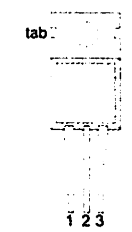
QUICK REFERENCE DATA

SYMBOL	PARAMETER	MAX.	MAX.	UNIT
	BT136-	600E	800E	
V_{DRM}	Repetitive peak off-state voltages	600	800	V
$I_{T(RMS)}$	RMS on-state current	4	4	A
I_{TSM}	Non-repetitive peak on-state current	25	25	A

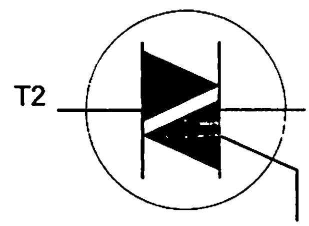
NING - TO220AB

N	DESCRIPTION
	main terminal 1
	main terminal 2
	gate
b	main terminal 2

PIN CONFIGURATION



SYMBOL



ITING VALUES

ing values in accordance with the Absolute Maximum System (IEC 134).

ABOL	PARAMETER	CONDITIONS	MIN.	MAX.		UNIT
				-600	-800	
M	Repetitive peak off-state voltages		-	600[1]	800	V
IS)	RMS on-state current	full sine wave; $T_{mb} \leq 107$ ˚C	-	4		A
	Non-repetitive peak on-state current	full sine wave; $T_j = 25$ ˚C prior to surge				
		t = 20 ms	-	25		A
		t = 16.7 ms	-	27		A
	I^2t for fusing	t = 10 ms	-	3.1		A^2s
dt	Repetitive rate of rise of on-state current after triggering	$I_{TM} = 6$ A; $I_G = 0.2$ A; $dI_G/dt = 0.2$ A/µs				
		T2+ G+	-	50		A/µs
		T2+ G-	-	50		A/µs
		T2- G-	-	50		A/µs
		T2- G+	-	10		A/µs
	Peak gate current		-	2		A
	Peak gate voltage		-	5		V
	Peak gate power		-	5		W
V)	Average gate power	over any 20 ms period	-	0.5		W
	Storage temperature		-40	150		˚C
	Operating junction temperature		-	125		˚C

ıough not recommended, off-state voltages up to 800V may be applied without damage, but the triac may h to the on-state. The rate of rise of current should not exceed 3 A/µs.

:RMAL RESISTANCES

IBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
mb	Thermal resistance junction to mounting base	full cycle	-	-	3.0	K/W
		half cycle	-	-	3.7	K/W
a	Thermal resistance junction to ambient	in free air	-	60	-	K/W

.TIC CHARACTERISTICS

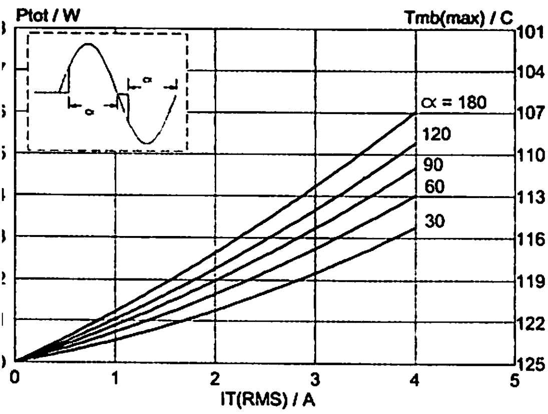
:5 °C unless otherwise stated

IBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
	Gate trigger current	V_D = 12 V; I_T = 0.1 A				
		T2+ G+	-	2.5	10	mA
		T2+ G-	-	4.0	10	mA
		T2- G-	-	5.0	10	mA
		T2- G+	-	11	25	mA
	Latching current	V_D = 12 V; I_{GT} = 0.1 A				
		T2+ G+	-	3.0	15	mA
		T2+ G-	-	10	20	mA
		T2- G-	-	2.5	15	mA
		T2- G+	-	4.0	20	mA
	Holding current	V_D = 12 V; I_{GT} = 0.1 A	-	2.2	15	mA
	On-state voltage	I_T = 5 A	-	1.4	1.70	V
	Gate trigger voltage	V_D = 12 V; I_T = 0.1 A	-	0.7	1.5	V
		V_D = 400 V; I_T = 0.1 A; T_j = 125 °C	0.25	0.4	-	V
	Off-state leakage current	$V_D = V_{DRM(max)}$; T_j = 125 °C	-	0.1	0.5	mA

IAMIC CHARACTERISTICS

:5 °C unless otherwise stated

IBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
/dt	Critical rate of rise of off-state voltage	V_{DM} = 67% $V_{DRM(max)}$; T_j = 125 °C; exponential waveform; gate open circuit	-	50	-	V/µs
	Gate controlled turn-on time	I_{TM} = 6 A; $V_D = V_{DRM(max)}$; I_G = 0.1 A; dI_G/dt = 5 A/µs	-	2	-	µs



1. Maximum on-state dissipation, P_{tot}, versus rms state current, $I_{T(RMS)}$, where α = conduction angle.

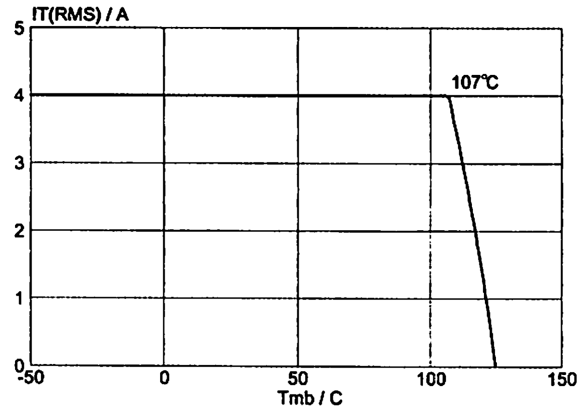
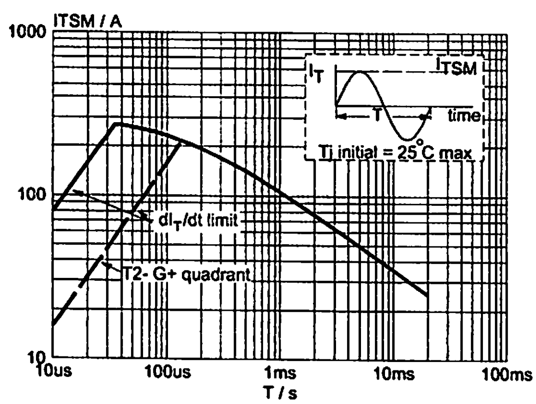


Fig.4. Maximum permissible rms current $I_{T(RMS)}$, versus mounting base temperature T_{mb}.



g.2. Maximum permissible non-repetitive peak on-state current I_{TSM}, versus pulse width t_p, for sinusoidal currents, $t_p \leq 20ms$.

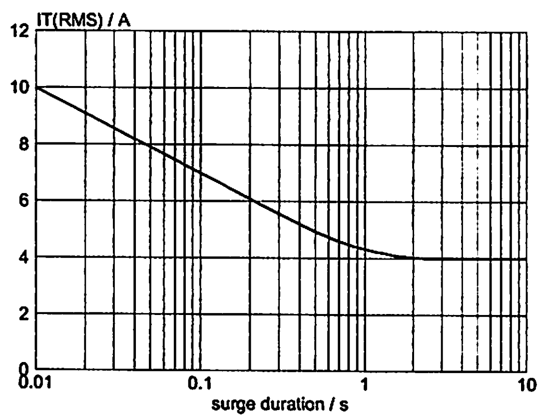
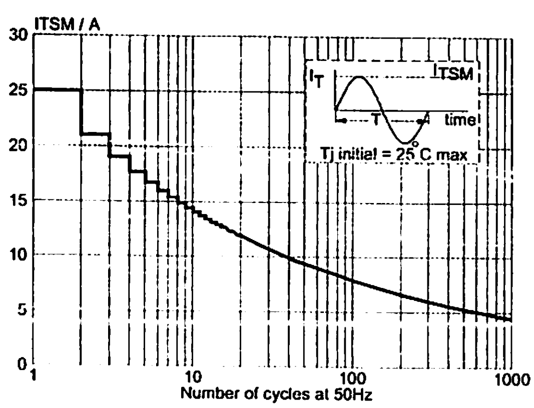


Fig.5. Maximum permissible repetitive rms on-state current $I_{T(RMS)}$, versus surge duration, for sinusoidal currents, f = 50 Hz; $T_{mb} \leq 107°C$.



g.3. Maximum permissible non-repetitive peak n-state current I_{TSM}, versus number of cycles, for sinusoidal currents, f = 50 Hz.

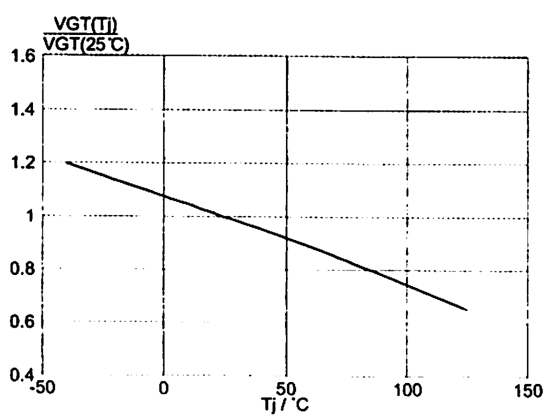


Fig.6. Normalised gate trigger voltage $V_{GT}(T_j)$/ $V_{GT}(25°C)$, versus junction temperature T_j.

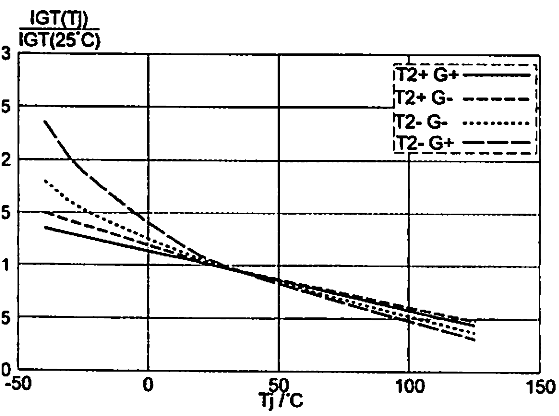


Fig.7. Normalised gate trigger current $_{GT}(T_j)/ I_{GT}(25°C)$. versus junction temperature T_j.

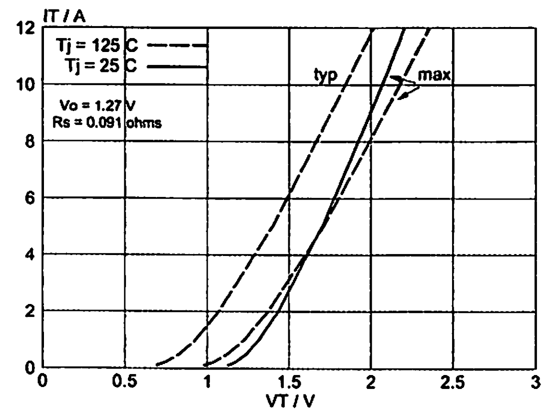
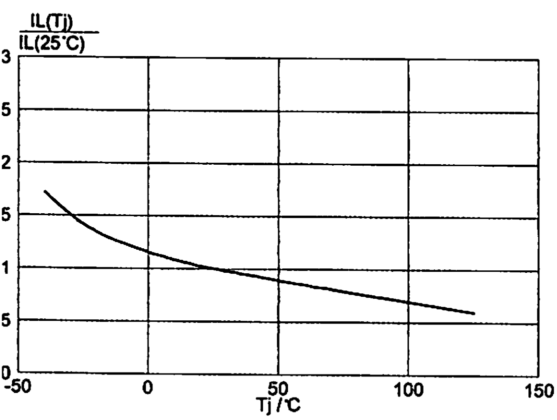


Fig.10. Typical and maximum on-state characteristic.



g.8. Normalised latching current $I_L(T_j)/ I_L(25°C)$, versus junction temperature T_j.

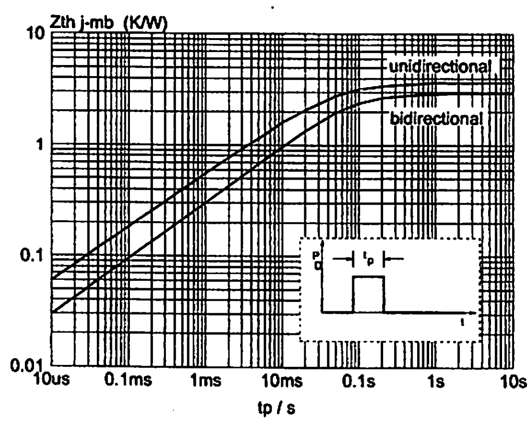
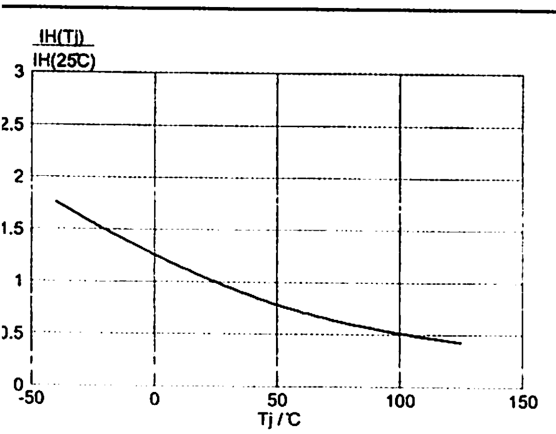


Fig.11. Transient thermal impedance $Z_{th\,j\text{-}mb}$, versus pulse width t_p.



g.9. Normalised holding current $I_H(T_j)/ I_H(25°C)$, versus junction temperature T_j.

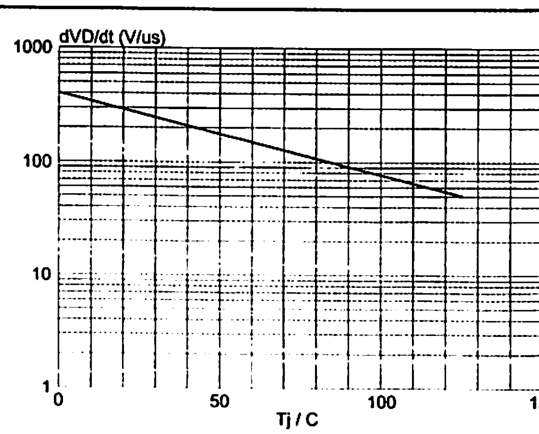


Fig.12. Typical, critical rate of rise of off-state voltage, dV_D/dt versus junction temperature T_j.

:HANICAL DATA

'ensions in mm

Mass: 2 g

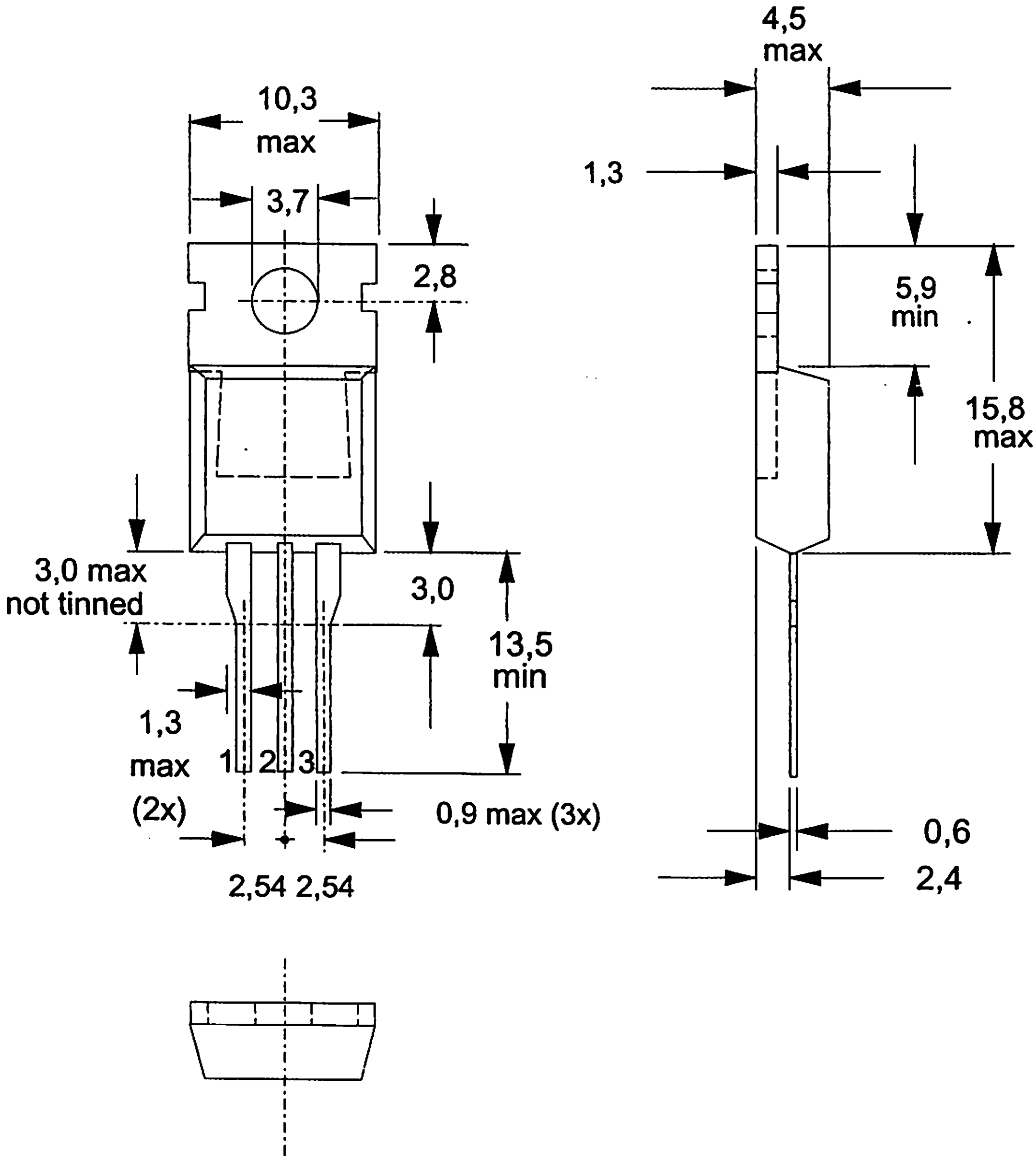


Fig.13. SOT78 (TO220AB). pin 2 connected to mounting base.

s
'fer to mounting instructions for SOT78 (TO220) envelopes.
oxy meets UL94 V0 at 1/8".

'INITIONS

ſA SHEET STATUS		
ſA SHEET ιTUS[2]	PRODUCT STATUS[3]	DEFINITIONS
ective data	Development	This data sheet contains data from the objective specification for product development. Philips Semiconductors reserves the right to change the specification in any manner without notice
liminary data	Qualification	This data sheet contains data from the preliminary specification. Supplementary data will be published at a later date. Philips Semiconductors reserves the right to change the specification without notice, in ordere to improve the design and supply the best possible product
duct data	Production	This data sheet contains data from the product specification. Philips Semiconductors reserves the right to make changes at any time in order to improve the design, manufacturing and supply. Changes will be communicated according to the Customer Product/Process Change Notification (CPCN) procedure SNW-SQ-650A

ıiting values

iting values are given in accordance with the Absolute Maximum Rating System (IEC 134). Stress above one nore of the limiting values may cause permanent damage to the device. These are stress ratings only and ration of the device at these or at any other conditions above those given in the Characteristics sections of specification is not implied. Exposure to limiting values for extended periods may affect device reliability.

ɔlication information

ere application information is given, it is advisory and does not form part of the specification.

Ξ SUPPORT APPLICATIONS

ıe products are not designed for use in life support appliances, devices or systems where malfunction of these ucts can be reasonably expected to result in personal injury. Philips customers using or selling these products se in such applications do so at their own risk and agree to fully indemnify Philips for any damages resulting such improper use or sale.

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