

SKRIPSI

ALAT PENGENDALI ON/OFF PERALATAN LISTRIK DAN KORDEN PADA RUMAH TANGGA MENGGUNAKAN REMOTE INFRA MERAH SONY BERBASIS MIKROKONTROLER AT89S52



Disusun Oleh :

HERI SUWANDONO

NIM 04.12.224

**JURUSAN TEKNIK ELEKTRO S-1
KONSENTRASI TEKNIK ELEKTRONIKA
FAKULTAS TEKNOLOGI INDUSTRI
INSTITUT TEKNOLOGI NASIONAL MALANG
2009**

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LEMBAR PERSETUJUAN

ALAT PENGENDALI ON/OFF PERALATAN LISTRIK DAN
KORDEN PADA RUMAH TANGGA MENGGUNAKAN REMOTE
INFRA MERAH SONY BERBASIS MIKROKONTROLER
AT89S52

SKRIPSI

*Disusun dan Diajukan Sebagai Salah Satu Syarat Untuk Memperoleh
Gelara Sarjana Teknik Elektronika Strata Satu (S-1)*

Disusun Oleh :
HERI SUWANDONO

NIM : 04.12.224

Diperiksa dan Disetujui

Dosen Pembimbing I

Dosen Pembimbing II


Ir. Mimien Mustikawati, MT
NIP. 1030000352


Irmalia Suryani Faradisa, ST, MT
NIP. 1030000365

Mengetahui,


Jurusan Teknik Elektro S-1



Ir. Yudi Limpraptono, MT
NIP Y. 103 950 0274

JURUSAN TEKNIK ELEKTRO S-1
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FAKULTAS TEKNOLOGI INDUSTRI
INSTITUT TEKNOLOGI NASIONAL MALANG
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ABSTRAK

ALAT PENGENDALI ON/OFF PERALATAN LISTRIK DAN KORDEN PADA RUMAH TANGGA MENGGUNAKAN REMOTE INFRA MERAH SONY BERBASIS MIKROKONTROLER AT89S52

(Heri Suwandono, 04.12.224, Teknik Elektro S-1/Elektronika)
(Fakultas Teknologi Industri, Institut Teknologi Nasional Malang)
(Dosen Pembimbing I : Ir.TH.Mimien Mustikawati, MT)
(Dosen Pembimbing II : Irmalia Suryani Faradisa, ST, MT)

Pada skripsi ini dirancang suatu alat untuk mengatur seluruh peralatan listrik yang ada didalam setiap kamar dengan menggunakan Remote infra merah Sony, cara kerja dari sistem alat ini adalah saat tombol remote ditekan, remote mengirimkan sinyal yang berupa data biner 12 bit ke sensor IRM-8510, kemudian sensor IRM-8510 menangkap dan mendeteksi sinar inframerah yang dikirimkan oleh remote dan dikirimkan ke mikrokontroler AT89S52, selanjutnya mikrokontroller menterjemahkan data dari remote dan hanya mengambil 7 bit pertama sebagai bit data sedangkan bit berikutnya tidak diambil karena hanya data address, mikrokontroler memberi perintah pada driver relay untuk mengaktifkan relay sesuai dengan tombol yang ditekan dan relay akan mengaktifkan peralatan listrik tersebut dengan indikator lampu, tetapi driver relay pada korden berfungsi untuk mengaktifkan Motor DC guna membuka dan menutup korden tersebut oleh karena itu memudahkan pemilik rumah untuk mengaktifkan peralatan listrik dan korden dengan cara menggunakan satu remote saja

Kata Kunci : *Remote Sony, Sensor IRM-8510, Mikrokontroler.*

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“ALAT PENGENDALI ON/OFF PERALATAN LISTRIK DAN KORDEN PADA RUMAH TANGGA MENGGUNAKAN REMOTE INFRA MERAH SONY BERBASIS MIKROKONTROLER AT89S52”

Pembuatan skripsi ini disusun guna memenuhi syarat kelulusan pendidikan jenjang Strata I di Institut Teknologi Nasional Malang. Dalam penyusunan skripsi ini penulis banyak mendapat bantuan baik moril maupun materiil, saran dan dorongan semangat dari berbagai pihak, untuk itu penulis mengucapkan terima kasih kepada :

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BAB I

PENDAHULUAN

1.1 Latar Belakang

Perkembangan pola pikir manusia dalam ilmu pengetahuan dan teknologi ternyata mengalami kemajuan terus menerus. Perbaikan terhadap teknologi yang sudah ada terus dilakukan agar menjadi lebih efisien. Salah satu bidang teknologi yang mengalami perkembangan lebih pesat adalah teknologi elektronika yang tidak terlepas dari tuntunan masyarakat yang terus menerus sesuai dengan kondisi dan situasi yang dihadapi.

Sistem pengaturan sangatlah perlu dilakukan di dalam ruangan rumah sehingga orang yang berada di dalam rumah akan terasa nyaman berada di rumah tersebut, pengaturan diberlakukan pada lampu, kipas angin, Tape, Lemari Es, Korden dalam ruangan rumah

Dari latar belakang di atas muncul pemikiran untuk merancang sebuah sistem yang berfungsi untuk mengatur seluruh peralatan listrik yang ada didalam setiap kamar dengan menggunakan *Remote* infra merah Sony , agar para pemilik rumah dan tamu yang menginap terasa nyaman dirumah tersebut karena tidak jauh – jauh menghidupkan atau mematikan peralatan listrik tersebut.

1.2 Rumusan Masalah

Berdasarkan latar belakang dari masalah yang di hadapi, maka dapat dirumuskan

1. Bagaimana membuat alat pengontrol peralatan rumah seperti lampu, kipas angin , Tape , Lemari Es dan Korden dengan menggunakan *Remote* Kontrol infra merah Sony
2. Bagaimana membuat perangkat lunak dengan menggunakan Program C++ untuk mengontrol peralatan rumah seperti lampu, kipas angin , Tape , Lemari Es dan Korden

1.3 Batasan Masalah

Untuk memfokuskan pembahasan maka dalam proyek ini pembahasan untuk alat ini adalah berikut :

1. Pengaturan dilakukan pada 3 buah lampu, kipas angin, Tape, Lemari Es, Korden
2. Simulasi pengaturan hanya pada 1 ruangan
3. Simulasi untuk 3 buah lampu dengan menggunakan lampu
4. Simulasi untuk kipas angin , Tape, Lemari Es digunakan lampu
5. Simulasi untuk korden menggunakan motor DC
6. Tidak membahas power supply dan motor DC

1.4 Tujuan

Tujuan yang ingin dicapai dalam pembuatan skripsi ini adalah:

Dengan dibuatnya alat pengontrol ini memudahkan pemilik rumah mengendalikan peralatan listrik dan korden dengan hanya menggunakan satu remote saja

1.5 Metodologi

Metodologi yang dipakai dalam pembuatan skripsi ini adalah:

1. Studi Literatur

Mencari referensi-referensi yang berhubungan dengan perencanaan dan pembuatan alat yang akan dibuat.

2. Penelitian Lapangan

Melakukan penelitian secara langsung mengenai objek-objek yang berhubungan langsung dengan perencanaan alat yang akan dibuat.

3. Pengolahan Data

Mengolah Data dengan jalan membuat analisa dan menarik kesimpulan dari hasil pengujian yang ada.

1.6 Sistematika Pembahasan

BAB I Pendahuluan

Menjelaskan tentang latar belakang, tujuan, permasalahan, batasan masalah, dan sistematika penulisan.

BAB II Teori Penunjang

Membahas teori yang mendukung dalam perencanaan dan pembuatan alat uji kadar formalin dalam makanan.

BAB III Perencanaan Sistem

Dalam Bab ini akan bahas mengenai perencanaan dan pembuatan tugas akhir ini yang meliputi seluruh sistem ini baik itu perangkat keras maupun perangkat lunak sistem.

BAB IV Pengujian Sistem

Dalam Bab ini membahas tentang pengujian dan hasil yang diperoleh dari sistem yang telah dibuat.

BAB V Kesimpulan dan Saran

Dalam Bab ini berisi kesimpulan-kesimpulan yang diperoleh dari perencanaan dan pembuatan tugas akhir ini serta saran-saran guna menyempurnakan dan mengembangkan sistem lebih lanjut.

BAB II

LANDASAN TEORI

2.1 Pendahuluan

Pada bab ini akan dibahas mengenai teori penunjang dari peralatan yang direncanakan. Teori penunjang ini akan membahas tentang komponen dan peralatan pendukung pada alat yang dibuat. Pokok pembahasan pada bab ini adalah :

1. *Remote Sony RM827T*
2. Sensor Inframerah 8510
3. Mikrokontroler AT89S52
4. EEPROM AT24C16
5. Driver Motor L298
6. Motor DC
7. *Limit Switch*
8. *Relay*

2.1 Inframerah

Sinar Inframerah adalah termasuk cahaya monokromatis yang tidak tampak oleh mata manusia. Spektrum frekwensi cahaya secara umum dibagi menjadi tiga bagian yaitu :

- a. Inframerah, mempunyai panjang gelombang 0,3 mm-0,7 μm .
- b. Cahaya tampak, mempunyai panjang gelombang 0,7 μm – 0,4 μm
- c. Ultraviolet, mempunyai panjang gelombang 0,4 μm – 0,03 μm

Spectrum frekwensi Inframerah yang sering digunakan 2,5.10 Hz- 2,0.10 Hz.

Gelombang elektromagnetik merupakan penyusun dari cahaya yang berada dalam spektrum elektromagnetik yang mempunyai jangkauan sangat lebar. Pada jarak yang sama, seluruh spektrum elektromagnetik tersebut mempunyai kecepatan yang sama tetapi frekwensinya berbeda sesuai dengan panjang gelombangnya.

Dalam hal ini berlaku :

$$C = \lambda \cdot f$$

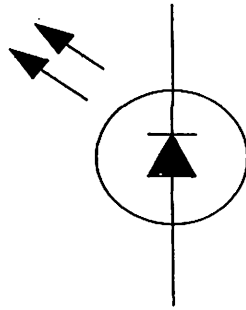
Dengan : c = kecepatan cahaya (m/s)

λ = panjang gelombang (m)

F = frekuensi (Hz)

2.2 LED Inframerah

LED Inframerah digunakan untuk menghasilkan sinar Inframerah. Prinsip kerja dari Inframerah adalah pada waktu *LED* Inframerah dibias *forward*, elektron dari pita konduksi melewati *junction* jatuh ke dalam *hole* pita *valensi*, sehingga elektron tersebut memancarkan energi. Pada dioda penyearah biasa, energi ini dipancarkan sebagai energi panas, sedangkan pada *LED* Inframerah energi ini dipancarkan sebagai cahaya.



Gambar 2.1 Simbol LED *infra* merah

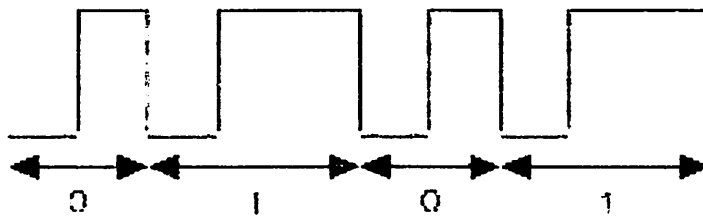
Sumber : Prinsip – prinsip Elektronika. 2004

LED Inframerah merupakan pin function yang memancarkan radiasi Inframerah yang tidak kelihatan oleh mata kita. Apabila pada anoda diberi tegangan dan katoda ke *ground* maka *LED* menjadi *ON* dan arus akan mengalir dari anoda ke katoda. Pada reaksi semikonduktor, suatu dioda akan terjadi perpindahan elektron dari N ke tipe P. Proses rekombinasi antara elektron dan *hole* menghasilkan pelepasan energi berupa pancaran cahaya.

Efisiensi pancaran cahaya akan berkurang seiring dengan berkurangnya arus input dan kenaikan suhu. Pada *LED* Inframerah, cahaya yang dipancarkan mempunyai panjang gelombang 0,3 mm – 0,7 μ m sehingga pancaran gelombang tersebut tidak tertangkap oleh mata manusia.

2.3 Metode Pengiriman Data Remote Sony RM-827T

Remote Sony RM-827S Menggunakan cahaya Inframerah sebagai media dalam mengirimkan data ke penerima. *LED* Inframerah memancarkan cahaya dengan frekuensi antara 40 KHz. Frekuensi tinggi ini dipilih agar tidak mudah *terinterferensi* dengan sumber cahaya lain. Sinyal yang dikirimkan berupa data-data biner. Pengiriman data remote *Sony RM-827T* menggunakan sistem *Pulse Coded*. Dimana pada metode *pulse coded* dari masing-masing data berubah atau bervariasi sesuai dengan logikanya. Untuk logika satu dinyatakan dengan 1 periode *low* dan 2 periode *high* atau lebar jeda adalah t dan lebar pulse adalah $2t$. Sedangkan untuk logika nol dinyatakan dengan 1 periode *low* dan 1 periode *high* atau lebar jeda sama dengan lebar pulse yaitu t . Berikut ini adalah gambar dari sinyal pada metode *pulse coded* :



Gambar 2.2 Signal *Pulse Coded*

Sumber : www.Remote control technical specification.Sony.com

Spesifikasi data pada remote Sony RM-827T :

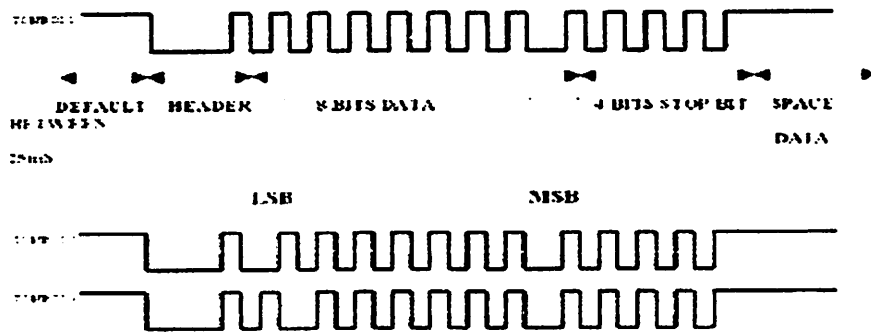
- Data kode yang dikirimkan menggunakan *pulse coded*
- Data dikirim dalam bentuk paket, setiap paket terdapat *starting bit* atau *header*, urutan data pulsa '0' dan '1' terdiri dari 12 bit dan spasi antara paket/antar *frame*
- Waktu tiap periodenya adalah 0,6 ms.
- Panjang *header* = $4T = 2,4$ ms
- Waktu tiap 1 *frame* = 45 ms.
- Logika 0 = pulsa dengan panjang T dan *space* dengan panjang T.
- Logika 1 = pulsa dengan panjang 2T dan *space* dengan panjang T.
- 7 bit pertama adalah *command* (perintah)
- 5 bit terakhir adalah *address* (alamat).

Sebelum kode dikirim, terlebih dahulu mengirimkan sinyal awal yang disebut sebagai *header*. *Header* adalah sinyal yang dikirimkan sebelum kode sebenarnya, dan juga merupakan sinyal untuk mengaktifkan penerima. *Header* selalu dikirimkan dengan lebar pulsa yang jauh lebih panjang daripada kode sebenarnya. Setelah *header* dikirimkan, baru kemudian mengirimkan kode *remote*.

Kode *remote* dibagi menjadi dua fungsi, yaitu pertama digunakan sebagai *command* atau perintah untuk melaksanakan intruksi dari *remote*. Fungsi kedua digunakan sebagai *address* atau alamat

Antara jenis remote yang satu dengan yang lainnya memiliki panjang *header* berbeda, begitu pula lebar pulsa dan jeda (*space*). Masing – masing jenis *remote* juga memiliki jumlah bit kode yang berbeda – beda

Format data remote Sony digambarkan sebagai berikut :



Gambar 2.3 Format Data Remote Sony

Sumber : <http://www.Sony.com>

Tabel 2.1 Data Remote Sony RM-827T

Sumber :<http://www.Sony.com>

Nama tombol	Data Hexa	Fungsi Tombol	Data Hexa	Fungsi Tombol	Data Hexa
Tombol 1	#080	Volume +	#093	Sharpenss -	#0A3
Tombol 2	#081	Mute	#094	TV/Video	#0A5
Tombol 3	#082	Power(toggle)	#095	Balance L	#0A6
Tombol 4	#083	Normal value	#096	Balance R	#0A7
Tombol 5	#084	Picture +	#098	Power on	#0AE
Tombol 6	#085	Picture -	#099	Power off	#0AF
Tombol 7	#086	Colour +	#09A	Input line A	#0C0
Tombol 8	#0C1	Colour -	#09B	Input line B	#0C1
Tombol 9	#088	Brightness +	#09E	Input AV	#0C2
Tombol 0	#089	Brightness -	#09F	Input digital	#0C3
Ch -	#090	Hue +	#0A0	Input Vtr	#0C5
Ch +	#091	Hue -	#0A1	Sharpenss -	#0C7
Volume +	#092	Sharpenss +	#0A2		#0A3

2.4 Sensor Inframerah 8510

IR-8510 adalah modul yang berisi rangkaian penerima sinar inframerah yang bekerja pada frekwensi 40 Khz. Gambar sensor Inframerah ditunjukkan dalam gambar dibawah ini.



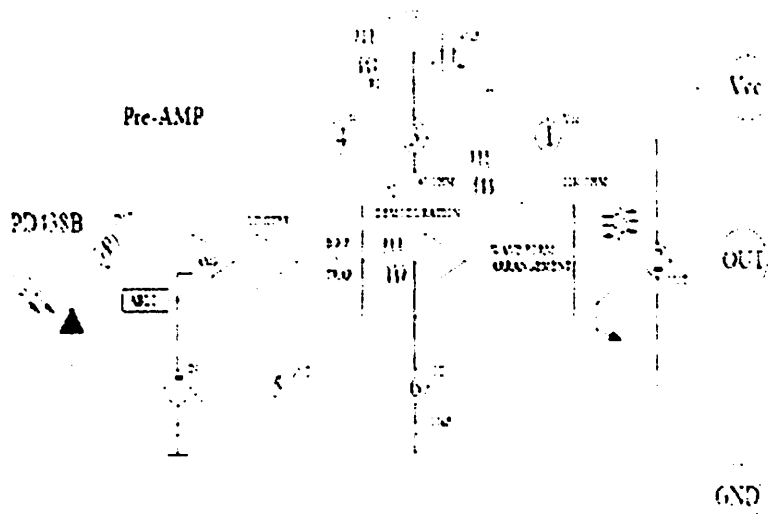
Gambar 2.4 Sensor Inframerah 8510

Sumber : <http://www.Everlightelectronic.IRM 8510.com>

Spesifikasi dari IR-8510:

- Detektor cahaya dan *preamplifier* dalam 1 paket
- *Internal filter* untuk PCM frekuensi
- Tidak mudah *terinterferensi*
- Output kompatibel dengan TTL dan CMOS
- Keluaran aktif rendah
- Konsumsi daya rendah

Modul Inframerah ini tersusun atas fotodiode, AGC (*Active Gain Control*), bandpass, demodulator, dan *control circuit*. Fotodiode digunakan sebagai detektor inframerah, kemudian sinyal keluaran tersebut dikuatkan dan dikontrol oleh AGC agar sinyal keluaran tetap konstan. Setelah dikuatkan, sinyal keluaran dihubungkan ke bandpass Filter yang berfungsi untuk meloloskan frekwensi sinyal 40 Khz dari pemancar Inframerah. Rangkaian demodulator digunakan untuk memisahkan sinyal data dari pemancar Inframerah. Sehingga keluaran dari IRM 8510 bisa langsung ke mikrokontroller.



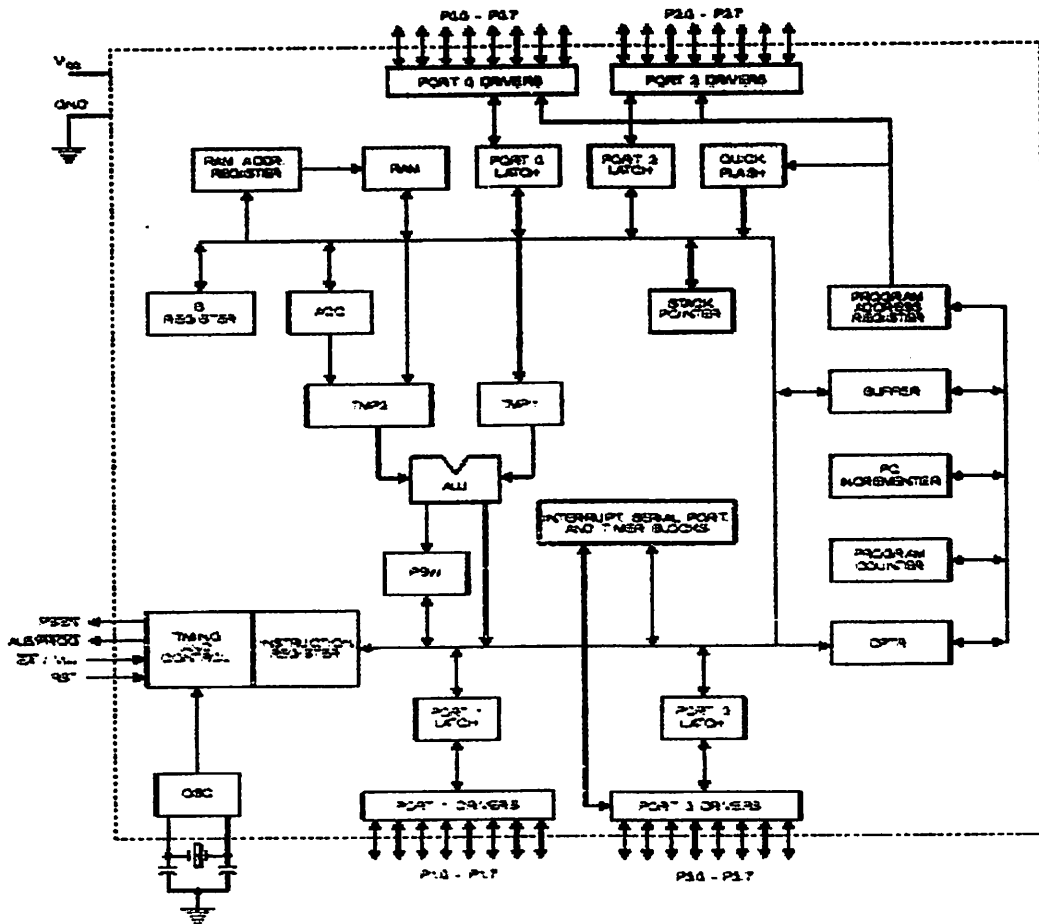
Gambar 2.5 Blok Diagram IRM-8510

Sumber : <http://www.Vishay.com>

2.5. Mikrokontroler AT89S52

AT89S52 adalah *mikrokontroller* keluaran Atmel dengan 4k *byte* Flash PEROM (*Programmable and Erasable Read Only Memory*), AT89S51 merupakan memori dengan teknologi *nonvolatile memory*, isi memori tersebut dapat diisi ulang ataupun dihapus berkali-kali. Memori ini biasa digunakan untuk menyimpan instruksi (perintah) berstandar MCS-51 *code* sehingga memungkinkan *mikrokontroller* ini untuk bekerja dalam mode *single chip operation* (mode operasi keping tunggal) yang tidak memerlukan *external memory* (memori luar) untuk menyimpan source code tersebut. Mikrokontroler AT89S52 memiliki beberapa kemampuan standar, yaitu:

1. *Central Processing Unit* (CPU) 8 bit dengan register A (*accumulator*) dan register B.
2. Memiliki 3 level *Program Memory Lock*.
3. 256 x 8 bit Internal RAM.
4. 32 *Programmabel I/O lines*.
5. 8 Kbyte of *In-System Reprogrammable Flash Memory*.
6. 3 *Timer/Counter* masing-masing 16-bit.



Gambar 2.1 Diagram Blok Arsitektur Mikrokontroler AT89S52

Sumber : <http://www.Atmel 89S52.com>

Organisasi Memori

Mikrokontroler ATMEL-51/52 mempunyai organisasi memori yang terdiri atas:

Memori Program (CODE).

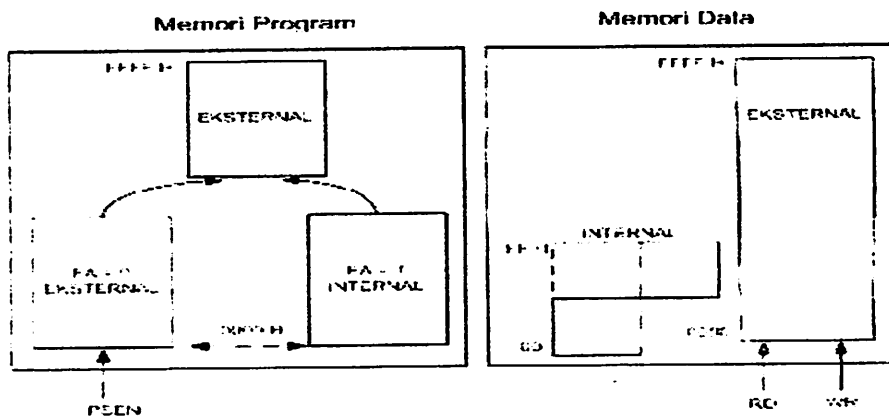
Memori Data (DATA).

Memori Data *Indirect* (IDATA).

Memori Data Pengalamatan Bit (BIT).

Memori Data External (XDATA).

Semua serpih tunggal dalam keluarga MCS-51 memiliki pembagian ruang alamat untuk program dan data. Pemisahan memori program dan memori data memperbolehkan memori data untuk diakses oleh alamat 8 bit. Sekalipun demikian, alamat data memori 16 bit dapat dihasilkan melalui register DPTR (*Data Point Register*). Memori program hanya bisa dibaca tidak bisa ditulis karena disimpan dalam EPROM. Dalam hal ini EPROM yang tersedia di dalam serpih tunggal AT89S52 sebesar 8 Kbyte



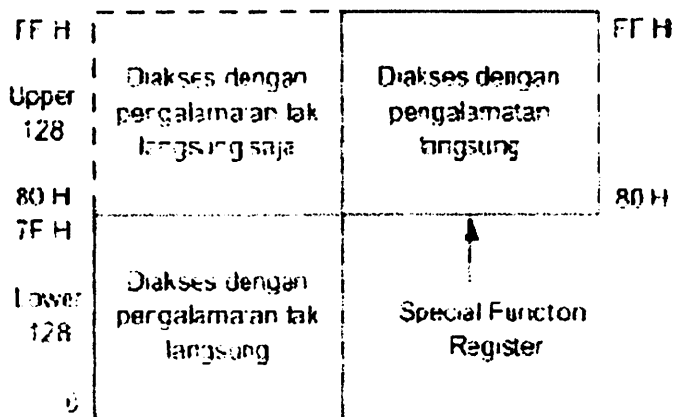
Sumber : <http://www.Atmel 89S52.com>

a. Memori Program

Pada EPROM 8 Kbyte, jika EA (*External Access*) bernilai tinggi, maka program akan menempati alamat 0000 H sampai 0FFF H secara internal. Jika EA bernilai rendah maka program akan menempati alamat 1000 H sampai FFFF H ke program eksternal.

b. Memori data

Memori data internal dipetakan seperti pada gambar di bawah ini Ruang memorinya dibagi menjadi tiga blok yaitu bagian 128 bawah, 128 atas, dan ruang SFR (*Special Function Register*)



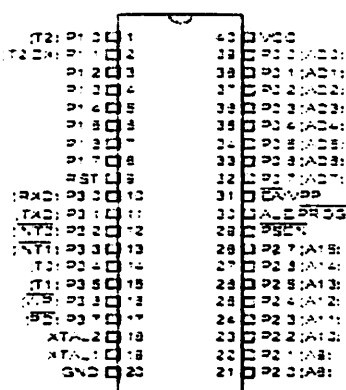
Sumber : <http://www.Atmel 89S52.com>

Bagian RAM 128 byte bawah dipetakan menjadi 32 byte bawah dikelompokkan menjadi 4 bank dan 8 register (R0 sampai R7). Pada bagian 16 byte berikutnya, di atas bank-bank register, membentuk suatu blok ruang memori yang bisa teralamat per bit (*bit addressable*).

Alamat-alamat bit ini adalah 00 H hingga 7F H. Semua byte yang berada di dalam 128 bawah dapat diakses baik secara langsung maupun tidak langsung. Bagian 128 atas hanya dapat diakses dengan pengalamatan tidak langsung. Bagian 128 atas dari RAM hanya ada di dalam piranti yang memiliki RAM 256 byte.

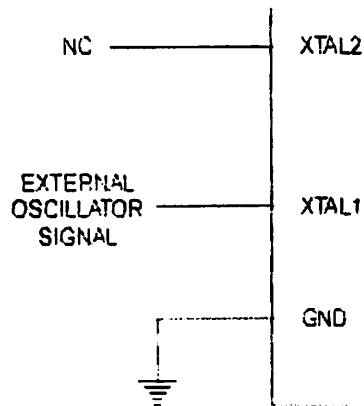
Konfigurasi Pin

Berdasarkan jumlah pin, AT89S52 memiliki 40 pin yang pada dasarnya fungsi pin-pin tersebut hampir sama pada AT89S51 hanya ada sedikit penambahan pada pin P1.0 dan P1.1 pada AT89S52.



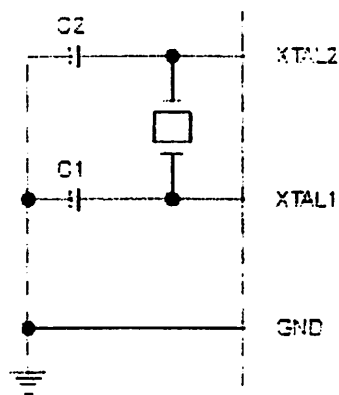
Gambar 2.2 Konfigurasi Pin Mikrokontroler AT89S52

Sumber : <http://www.Atmel 89S52.com>



Gambar 2.3 Masukan Pewaktuan Eksternal

Sumber : <http://www.Atmel 89S52.com>



Gambar 2.4 Rangkaian Pewaktuan Internal

Sumber : <http://www.Atmel 89S52.com>

Fungsi Masing-masing Pin

a. VCC

Berfungsi sebagai sumber tegangan +5volt.

b. GND

Berfungsi sebagai pentahan (Ground).

c. Port 0

Port 0 adalah masukan/keluaran (I/O) 8 bit dengan nama P0.0 - P0.7 jenisnya cerat terbuka masukan dua arah (open drain bi directional I/O port). Jika port

0 berlogika 1 maka dapat digunakan sebagai masukan yang mempunyai impedansi tinggi.

d. Port 1

Port 1 adalah masukan/keluaran 8 bit dengan nama masing-masing P1.0 – P1.7 yang bersifat dua arah. Port 1 sudah dipasang resistor *pull up* secara internal. Jika logika satu dituliskan pada port 1 maka keluaran akan berlogika satu dan digunakan sebagai masukan.

Port 1 sebagai masukan alamat rendah pada saat pemrograman memori flash internal dan verifikasi.

P1.0 untuk T2 (masukan pencacah eksternal ke *timer/counter 2*) keluaran *clock*.

P1.1 untuk T2EX (*timer/counter 2 reload trigger* dan kendali arah).

e. Port 2

Port 2 sama dengan Port 1 yaitu masukan/keluaran 8 bit dengan nama masing-masing P2.0 – P2.7 yang bersifat dua arah. Port 2 juga dipasang resistor *pull up* secara internal. Jika logika satu dituliskan pada port 2 maka keluaran akan berlogika satu dan digunakan sebagai masukan.

Port 2 juga sebagai *byte* alamat tinggi (A8 – A15) pada saat menjalankan program memori program eksternal dan mengakses data pada memori data eksternal dengan menggunakan pengalamatan 16 bit (instruksi MOVX @DPTR). Sedangkan jika menggunakan pengalamatan 8 bit (instruksi MOVX @R1) maka port 2 berisi SFR P2.

f. Port 3

Port 3 sama dengan Port 1 dan Port 2 yaitu masukan/keluaran 8 bit dengan nama masing-masing P2.0 – P2.7 yang bersifat dua arah. Port 2 juga dipasang resistor *pull up* secara internal. Jika logika satu dituliskan pada port 3 maka keluaran akan berlogika satu dan digunakan sebagai masukan.

Selain sebagai masukan/keluaran biasa, Port 3 juga mempunyai fungsi khusus sebagai berikut :

Tabel 2.2 Fungsi Khusus Port 3

Sumber : <http://www.Atmel 89S52.com>

Port	Fungsi
P3.0	RXD (Port masukan serial)
P3.1	TXD (Port keluaran serial)
P3.2	INT0 (Interupsi eksternal 0, aktif rendah)
P3.3	INT1 (Interupsi eksternal 1, aktif rendah)
P3.4	T0 (Masukan eksternal timer 0)
P3.5	T1 (Masukan eksternal timer 1)
P3.6	WR (Signal tukis untuk memori eksternal aktif rendah)
P3.7	RD (Signal baca untuk memori eksternal aktif rendah)

g. RST

RST berfungsi sebagai masukan reset. Jika RST diberi logika tinggi dalam waktu 2 siklus mesin mikrokontroler akan direset.

h. ALE/PROG

untuk menahan alamat bawah selama mengakses memori eksternal. Pin ini juga berfungsi sebagai PROG (aktif *low*) yang diaktifkan saat memprogram internal *flash* memori pada mikrokontroler (*on chip*).

i. PSEN (Program Store Enable)

sinyal yang digunakan untuk membaca, memindahkan program memori eksternal (ROM / EPROM) ke mikrokontroler (aktif *low*).

j. EA/Vpp (External Access Enable)

untuk memilih memori yang akan digunakan, memori program internal (EA = Vcc) atau memori program eksternal (EA = Vss), juga berfungsi sebagai Vpp (*programming supply voltage*) pada saat memprogram internal *flash* memori pada mikrokontroler.

k. XTAL-1

Pin 19 sebagai XTAL 1, masukan ke osilator berpenguatan tinggi, terhubung pada kristal.

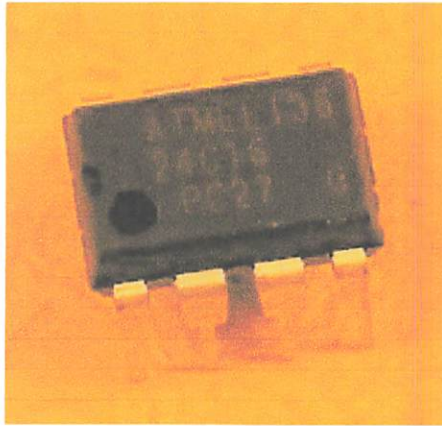
l. XTAL-2

Pin 18 sebagai XTAL 2, keluaran osilator yang terhubung pada kristal.

2.6 EEPROM AT24C16

EEPROM (*Electrically Erasable Programmable Read-Only Memory*, ditulis pula dengan **EEPROM**) adalah sejenis *chip* memori tidak-terhapus yang digunakan dalam komputer dan peralatan elektronik lain untuk menyimpan sejumlah konfigurasi data pada alat elektronik tersebut yang tetap harus terjaga meskipun sumber daya diputuskan, seperti tabel kalibrasi atau konfigurasi perangkat. Pengembangan EEPROM lebih lanjut menghasilkan bentuk yang lebih spesifik, seperti memori kilat (*flash memory*). Kelebihan utama dari EEPROM dibandingkan EPROM adalah ia dapat dihapus secara elektrik menggunakan cahaya ultraviolet sehingga prosesnya lebih cepat. Jika RAM tidak memiliki batasan dalam hal baca-tulis memori, maka EEPROM sebaliknya. Beberapa jenis EEPROM keluaran pertama hanya dapat dihapus dan ditulis ulang (erase-rewrite) sebanyak 100 kali sedangkan model terbaru bisa sampai 100.000 kali.

EEPROM yang digunakan dalam skripsi ini adalah tipe AT24C16 yang dapat melakukan penyimpanan sebesar 16 kilobit data. Dengan bentuknya yang kecil terdiri dari 8 pin, serial EEPROM ini mempunyai keunggulan dapat mengatasi keterbatasan pin yang digunakan oleh mikrokontroler AT89S52 (karena pin yang terhubung pada mikrokontroler hanya 2 pin saja yaitu pin SCL dan pin SDA).



Gambar 2.12 EEPROM 24C16

Sumber : <http://www.Atmel 24C16.com>

EEPROM AT24C16 memiliki Fitur – fitur sebagai berikut :

- Dapat bekerja pada *range* tegangan
 - a. 5 V ($VCC = 4,5 \text{ v} - 5,5 \text{ V}$)
 - b. 2,7V ($VCC = 2,7\text{V} - 5,5\text{V}$)
 - c. 2,5V ($VCC = 2,5\text{V} - 5,5\text{V}$)
 - d. 1,8V ($VCC = 1,8 - 5,5$)
- Terbagi menjadi $2048 \times 8 = 16$
- *Serial interface* 2 kabel
- *Schmitt trigger* dan input ter-filter untuk mengurangi noise
- Untuk $VCC = 5\text{V}$ bias sampai dengan frekwensi 400Khz
- Terdapat pin write protect untuk proteksi data
- Mode page write 16 byte
- Diiijinkan untuk partial page write
- Memiliki write time cycle sendiri maksimum 10 ms



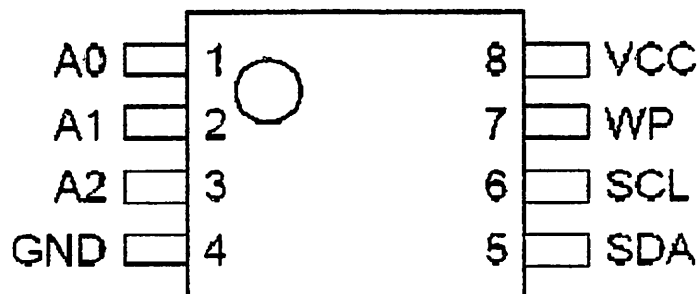
Gambar 2.13 AT3C10

Sumber: <http://www.ataintel.com>

AT3C10 memiliki fitur – fitur sebagai berikut :

- Dapat bekerja pada range tegangan
 - a. 2 V (VCC = 4.5 v – 2.5 V)
 - b. 2.7V (VCC = 2.7V – 2.5V)
 - c. 2.5V (VCC = 2.5V – 2.2V)
 - d. 1.8V (VCC = 1.8 – 2.2)
- Terbagi menjadi 2048 X 8 = 16
- Serial interface 2 kabel
- Schmitt trigger dan input ter-filter untuk mengurangi noise
- Untuk VCC = 2V bisa sampai dengan frekuensi 400KHz
- Terdapat pin write protect untuk proteksi data
- Mode page write 16 byte
- Dijalankan untuk partial page write
- Memiliki write time cycle sendiri maksimum 10 ms

- **Memiliki realibilitas tinggi :**
 - a. Dapat ditulis berulang –ulang sampai 1 juta.
 - b. Daya tahan validitas data sampai 100 tahun
 - c. Proteksi ESD lebih besar dari 30000 V.
- Dapat digunakan untuk otomotif dan peralatan –peralatan yang terhubung dengan temperature.
- Tersedia kemasan 8 pin dan 14 pin JEDEC SOIC,8 pin PDIP, Pin MSOP,8 pin TSSOP.



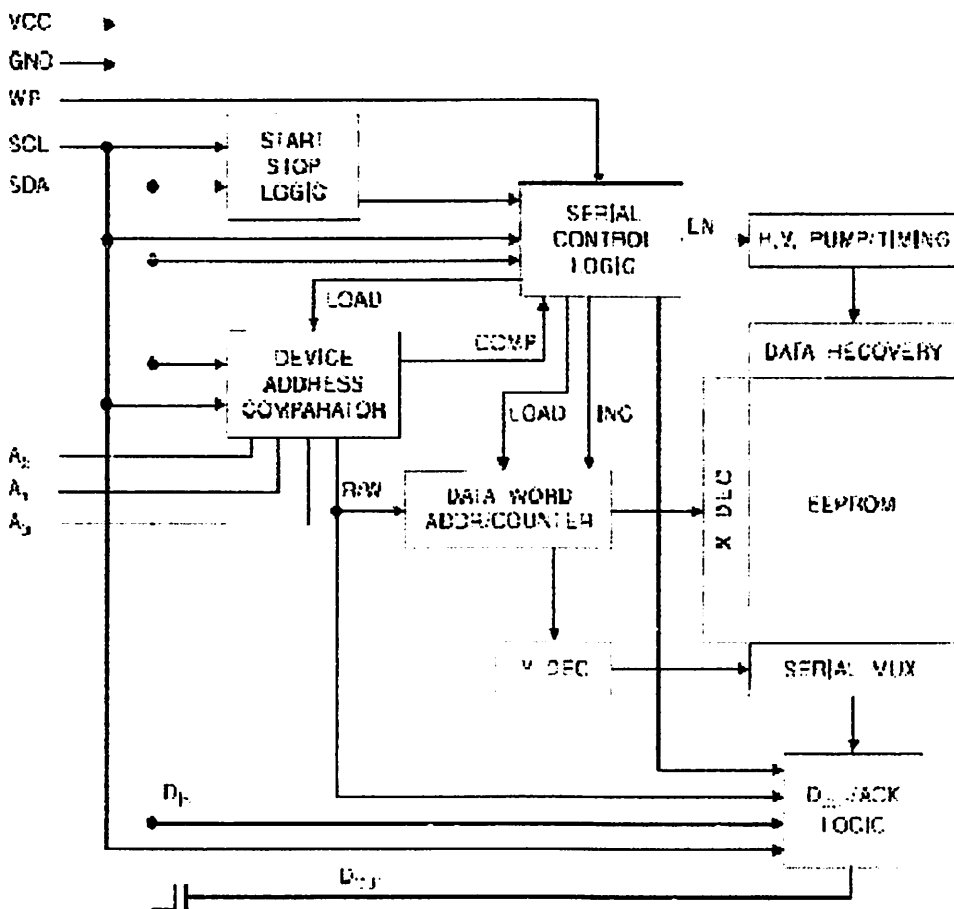
Gambar 2.13 Konfigurasi pin serial EEPROM AT24C16

Sumber : <http://www.Atmel 24C16.com>

Serial EEPROM memiliki pin sebanyak 8 buah,berikut adalah penjelasan masing – masing pin ya

- a) A0 – A2 : pin input untuk pengalamatan secara Hardware
- b) GND : Ground
- c) SDA : pin Data sebagai Transfer data
- d) SCL : pijn ini difungsikan untuk mengaktifkan clock pada serial EEPROM ini sendiri

- e) WP : pin ini berfungsi sebagai write protection pin (akan berfungsi jika dihubungkan pada Vcc). Berfungsi normal jika dihubungkan dengan ground.
- f) VCC : pin supply tegangan pada serial EEPROM 4,5 V – 5,5 V



Gambar2.1.4 Blok Diagram EEPROM AT24C16

Sumber : <http://www.Atmel24C16.com>

Serial EEPROM AT24C16 memiliki memori sebesar 16 kilobit data yang terdiri dari 8 blok pengalamatan, dari 000 b sampai 111 b (per 3bit), yang mana tiap alamat tersebut dapat menampung 256 sub alamat , dari 00000000 b sampai 11111111 b (per 8 bit), dan tiap sub alamat dapat menampung 8 bit data jadi

sebenarnya serial EEPROM ini dapat menampung $8 \times 256 \times 8$ bit data = 16,384 bit data.

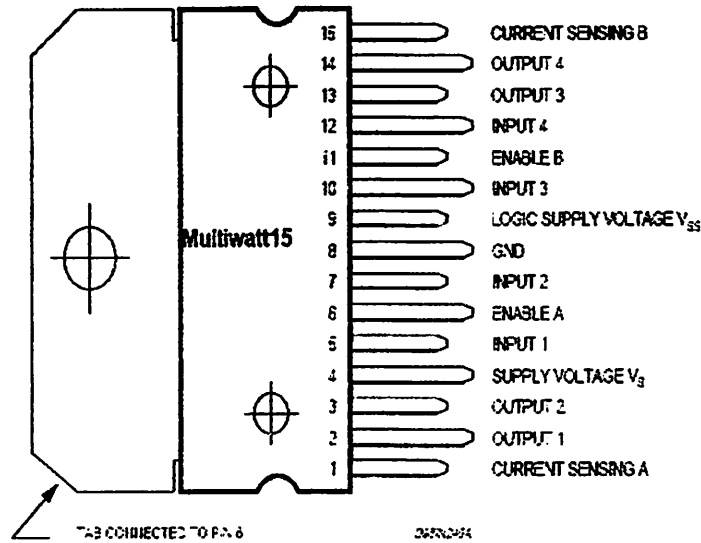
Serial EEPROM AT24C16 bekerja hanya menggunakan 2 buah pin saja, selain pin VCC dan pin Ground yaitu SCL untuk mengaktifkan clock-nya dan pin SDA sebagai pin jalur Transfer data. Penulisan / penyimpanan dan pengaksesan data selalu diawali start condition dan akhiri oleh stop condition yang diberikan pada pin SDA

2.7 Driver Motor IC L298

IC L298 merupakan Driver Motor DC yang berupa four channel driver, atau terdiri dari dua buah motor H-Bridge yang dikontrol oleh 4 bit input, ICL298 setiap channelnya memiliki arus sampai dengan 4 Ampere secara bersamaan pada tiap channelnya

Spesifikasi IC L298 sebagai berikut :

1. Total power adalah 5 Watt
2. Pick on current adalah 4 Ampere
3. Tegangan maksimum adalah 36 Volt
4. Logic Supply Voltage adalah 36 Volt
5. Input Voltage adalah 7 Volt
6. Inhibit Voltage adalah 7 Volt



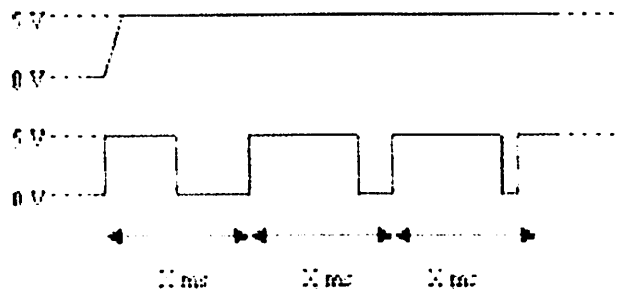
Gambar 2.13 Driver Motor L298

Sumber : <http://www.DatasheetL298.com>

Tabel 2.3 Fungsi pin – pin L298

Pin	Nama	Fungsi
1; 15	Sense A: Sense B	Diantara <i>pin sense</i> dan <i>ground</i> dihubungkan dengan resistor untuk mengatur arus pada motor
2; 3	Out 1; Out 2	<i>Output</i> dari H-Bridge A, dimana arus akan mengalir ke motor yang terkoneksi di pin kedua tersebut
4	V _s	Tegangan <i>supply</i> untuk keluaran <i>output</i> . Capacitor <i>non induktif</i> 100nF harus dihubungkan pada pin ini dan <i>ground</i>
5; 7	Input 1; Input 2	<i>Input</i> tegangan TTL untuk mengaktifkan H-Bridge A
6; 11	Enable A: Enable B	Tegangan TTL untuk mengenable input
8	GND	<i>Ground</i>
9	V _{SS}	Tegangan <i>supply</i> untuk logic blok. Capacitor 100nF harus dihubungkan antara pin ini dengan <i>ground</i>
10; 12	Input 3; Input 4	<i>Input</i> tegangan TTL untuk mengaktifkan H-Bridge B
13; 14	Out 3; Out 4	<i>Output</i> dari H-Bridge B, dimana arus akan mengalir ke motor yang terkoneksi di kedua pin tersebut

Sumber ST microelectronic, L298 Datasheet (www.alldatasheet.com)



Gambar 2.14 Timing Enable L288

Sumber : <http://www.DatasheetL293D.com>

Dengan adanya Internal diode didalam IC ini maka rangkaian yang digunakan menjadi ringkas karena tidak perlu tambahan diode eksternal.

Tabel2.4 Kondisi input IC L298

Inputs		Function
$V_{en} = H$	C = H ; D = L	Forward
	C = L ; D = H	Reverse
	C = D	Fast Motor Stop
$V_{en} = L$	C = X , D = X	Free Running Motor Stop

L = Low

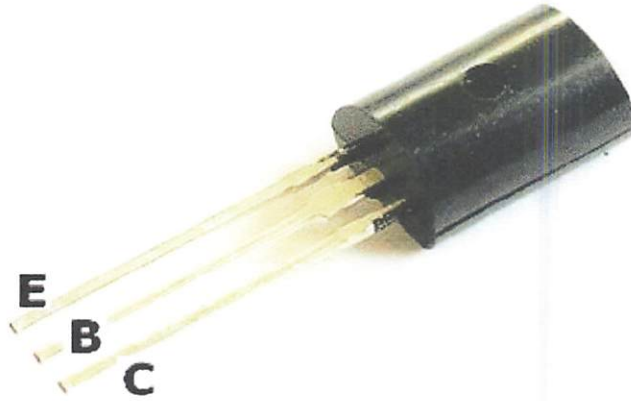
H = High

X = Don't care

Sumber : <http://www.DatasheetL293D.com>

2.8 Transistor PNP 9012

Transistor adalah alat semikonduktor yang dipakai sebagai penguat atau pemilih, dan mempunyai tiga terminal: suatu arus listrik atau tegangan listrik kecil yang dipasang pada satu terminal dapat mengontrol arus yang melewati kedua terminal lainnya.



Gambar 2.15 Transistor PNP 9012

Sumber : <http://www.ElectronicTransistor.com>

Transistor memiliki 3 terminal. Transistor biasanya dibuat dari bahan silikon atau germanium. Tiga kaki yang berlainan membentuk transistor bipolar adalah emitor, basis dan kolektor. Mereka dapat dikombinasikan menjadi jenis N-P-N atau P-N-P yang menjadi satu sebagai tiga kaki transistor. Pembiasan pada transistor dapat dilakukan dengan cara sebagai berikut:

- Bias maju (forward bias) pada hubungan emitor dan basis, dimana bahan tipe P mendapat positif dan tipe N mendapat negatif.
- Bias mundur (reverse bias) pada hubungan kolektor dan basis, dimana bahan tipe P mendapat negatif dan tipe N mendapat positif.

Transistor PNP terdiri dari selapis semikonduktor tipe-n diantara dua lapis semikonduktor tipe-p. Arus kecil yang meninggalkan basis pada moda tunggal

2.8. Transistor PNP 2012

Transistor adalah alat semikonduktor yang dipakai sebagai penguat atau pemilih dan mempunyai tiga terminal: satu arus listrik dan tegangan listrik kecil yang dipasang pada satu terminal dapat mengontrol arus yang melewati kedua terminal lainnya.



Gambar 2.13 Transistor PNP 2012

Sumber: <http://www.technicaltransistor.com>

Transistor memiliki 3 terminal. Transistor biasanya dibuat dari bahan silikon atau germanium. Tiga kaki yang berlainan membentuk transistor bipolar adalah emitor, basis dan kolektor. Mereka dapat dikombinasikan menjadi jenis N-P-N atau P-N-P yang menjadi satu sebagai tiga kaki transistor. Pembiasan pada

transistor dapat dilakukan dengan cara sebagai berikut:

- Bias maju (forward bias) pada hubungan emitor dan basis dimana bahan tipe P mendapat positif dan tipe N mendapat negatif.
- Bias mundur (reverse bias) pada hubungan kolektor dan basis dimana bahan tipe P mendapat negatif dan tipe N mendapat positif.

Transistor PNP terdiri dari selapis semikonduktor tipe-n di antara dua lapis semikonduktor tipe-p. Arus kecil yang meninggalkan basis pada mode tunggal

Tabel 2.6 Karakteristik Transistor 9012 :

Parameter	Symbol	Test conditions	MIN	TYP	MAX	UNIT
Collector-base breakdown voltage	$V(BR)_{CBO}$	$I_C = -100 \mu A, I_E = 0$	-40			V
Collector-emitter breakdown voltage	$V(BR)_{CEO}$	$I_C = -0.1 mA, I_B = 0$	-20			V
Emitter-base breakdown voltage	$V(BR)_{EBO}$	$I_E = -100 \mu A, I_C = 0$	-5			V
Collector cut-off current	I_{CBO}	$V_{CE} = -40 V, I_E = 0$			-0.1	μA
Collector cut-off current	I_{CEO}	$V_{CE} = -20 V, I_B = 0$			-0.2	μA
Emitter cut-off current	I_{EBO}	$V_{EB} = -5 V, I_C = 0$			-0.1	μA
DC current gain(note)	$h_{FE} \dots$	$V_{CE} = -1 V, I_C = -50 mA$	64		300	
	$h_{FE} \dots$	$V_{CE} = -1V, I_C = -500 mA$	40			
Collector-emitter saturation voltage	$V_{CE}(sat)$	$I_C = 500 mA, I_B = 50 mA$			-0.6	V
Base-emitter saturation voltage	$V_{BE}(sat)$	$I_C = 500 mA, I_E = -50 mA$			-1.2	V
Base-emitter voltage	V_{BE}	$I_E = -100 mA$			-1.4	V
Transition frequency	f_T	$V_{CE} = -6 V, I_C = -20 mA$ $f = 30 MHz$	150			MHz

Tabel 2.7 Klasifikasi Range Hfe(1) :

Rank	D	E	F	G	H	I
Range	64-91	73-112	96-135	112-166	144-262	190-300

Sumber : <http://www.DatasheetL293D.com>

.....

Keuntungan menggunakan transistor adalah

- a. Ukuran fisiknya kecil
- b. Tidak mudah pecah
- c. Daya listrik yang relatif rendah
- d. Efisiensi kerja relatif tinggi

Kekurangannya adalah

- a. Tidak tahan panas
- b. Tidak dapat menghasilkan frekuensi tinggi yang bertenaga besar
- c. Penguatan yang dihasilkan kecil

Tabel 2.5 Karakteristik Transistor

Symbol	Parameter	Ratings	Units
V_{CB0}	Collector-Base Voltage	-40	V
V_{CE0}	Collector-Emitter Voltage	-20	V
V_{EB0}	Emitter-Base Voltage	-5	V
I_C	Collector Current	-500	mA
P_C	Collector Power Dissipation	625	mW
T_J	Junction Temperature	150	$^{\circ}\text{C}$
T_{STG}	Storage Temperature	-55 ~ 150	$^{\circ}\text{C}$

- **Daerah mati (Cut OFF)**

Daerah mati merupakan daerah kerja saat transistor mendapat bias arus basis (I_b) > 0, maka arus kolektor dengan basis terbuka menjadi arus bocor dari basis ke emitor (ICEO). Hal yang sama dapat terjadi pada transistor hubungan kolektor-basis. Jika arus emitor sangat kecil ($I_E = 0$), emitor dalam keadaan terbuka dan arus mengalir dari kolektor ke basis (ICBO).

$$I_C = \beta I_B = 50 \times 400 \text{ uA} = 20 \text{ mA}$$

$$R_L = (V_{CC} - V_{LED} - V_{CE}) / I_C$$

- **Daerah Saturasi**

Daerah saturasi adalah mulai dari $V_{CE} = 0$ volt sampai kira-kira 0.7 volt (transistor silikon), yaitu akibat dari efek dioda kolektor-basis yang mana tegangan V_{CE} belum mencukupi untuk dapat menyebabkan aliran elektron.

- **Daerah Breakdown**

Dari kurva kolektor, terlihat jika tegangan V_{CE} lebih dari 40V, arus I_C menanjak naik dengan cepat. Transistor pada daerah ini disebut berada pada daerah breakdown. Seharusnya transistor tidak boleh bekerja pada daerah ini, karena akan dapat merusak transistor tersebut. Untuk berbagai jenis transistor nilai tegangan V_{CEmax} yang diperbolehkan sebelum breakdown bervariasi. V_{CEmax} pada databook transistor selalu dicantumkan juga.

emitor dikuatkan pada keluaran kolcktor. Dengan kata lain, transistor PNP hidup ketika basis lebih rendah daripada emitor. Tanda panah pada simbol diletakkan pada emitor dan menunjuk kedalam

- **Daerah Aktif**

Dacrah kerja transistor yang normal adalah pada dacrah aktif, dimana arus I_C Transistor dapat bekerja pada daerah aktif jika transistor mendapat arus basis (I_b) > 0 . Jika hukum Kirchhoff mengenai tegangan dan arus diterapkan pada loop kolcktor , maka dapat dipcrolch hubungan :

$$V_{CE} = V_{CC} - I_C R_C \dots\dots\dots$$

Dapat dihitung dissipasi daya transistor adalah :

$$P_D = V_{CE} \cdot I_C \dots\dots\dots$$

Rumus ini mengatakan jumlah dissipasi daya transistor adalah tegangan kolektor-emitor dikali jumlah arus yang melewatinya. Dissipasi daya ini berupa panas yang menyebabkan naiknya temperatur transistor. Umumnya untuk transistor power sangat perlu untuk mengetahui spcsifikasi $P_{D,max}$. Spcsifikasi ini menunjukkan temperatur kerja maksimum yang diperbolehkan agar transistor masih bekerja normal. Sebab jika transistor bekerja melebihi kapasitas daya $P_{D,max}$, maka transistor dapat rusak atau trbakar

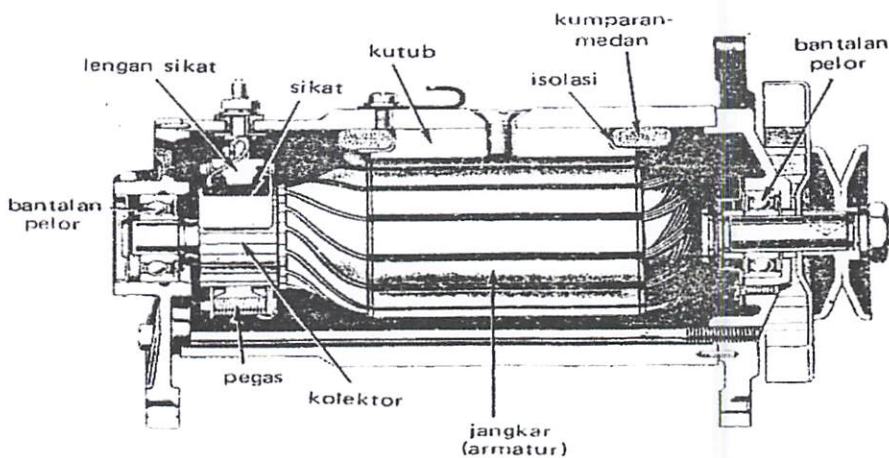
2.9 Motor DC

Pada skripsi ini motor DC digunakan sebagai penggerak korden. Prinsip kerja motor DC berdasarkan pada penghantar yang dialiri arus ditempatkan dalam suatu medan magnet sehingga penghantar tersebut akan mengalami gaya. Gaya menimbulkan torsi sehingga menghasilkan putaran. Penghantar yang berputar akan menimbulkan tegangan AC sehingga diubah menjadi tegangan DC oleh komutator dan sikat.



Gambar 2.16 Bentuk Fisik Motor DC

Sumber : Frank D. Petruzella, *Elektronik Industri*, Andi, 1996



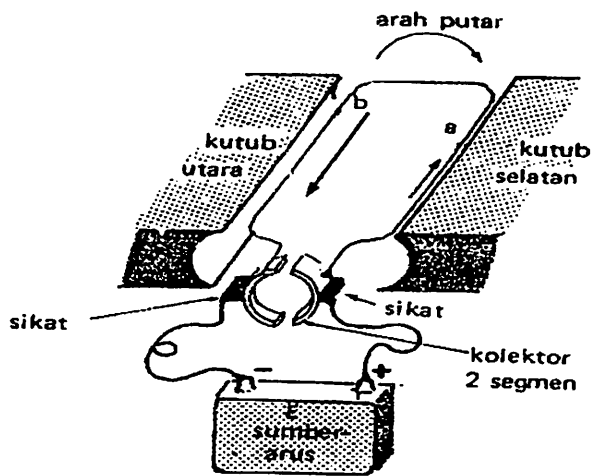
Gambar 2.17 Sebuah Motor DC

Sumber : Frank D. Petruzella, *Elektronik Industri*, Andi, 1996

Gaya-gaya yang bekerja sama kuatnya, jadi ada kopel yang bekerja pada kawat sehingga lilitan pun dapat berputar. Setelah berputar 90° arah arus berbalik, pada saat itu penghantar a dan penghantar b bertukar tempat. Akibatnya arah gerak putaran tidak berubah.

2.9.1 Cara Kerja Motor DC

Adapun cara kerja motor Dc dapat dilihat pada gambar dibawah ini:



Gambar 2.18 Dasar Kontruksi Motor DC

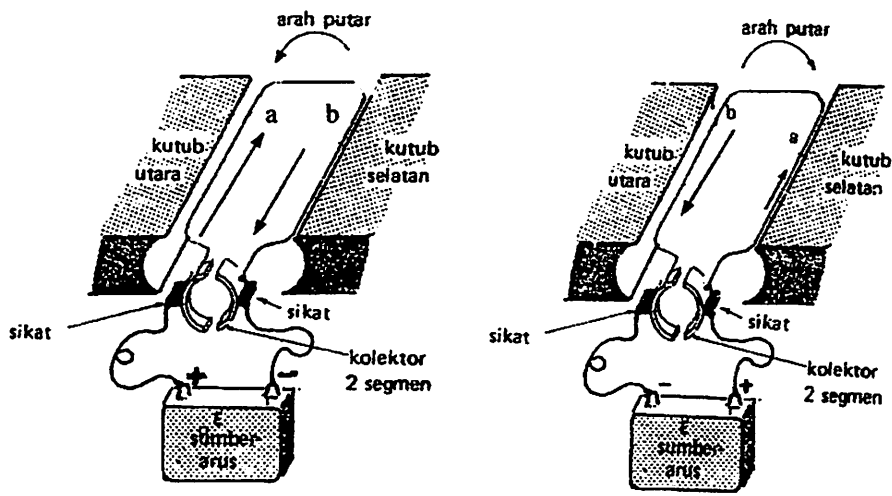
Sumber : www.HyperPhysics.com

Ada satu lilit kawat a – b berada di dalam medan magnet. Lilitan ini dapat berputar dengan bebas, lilitan ini bisasa disebut dengan jangkar (*armour*).

Pada jangkar dimasukkan arus yang berasal dari sumber (baterai) E. koneksi baterai dengan jangkar melalui sikat-sikat. Sikat-sikat ini terpasang pada sebuah cincin yang terbelah dua, yang disebut kolektir. Adapun tujuan dari kontruksi ini adalah agar lilitan kawat dapat berputar apabila ada arus listrik yang melewatinya.

Pada kawat yang berada di kanan arus mengalir dari depan ke belakang . dalam kawat yang di kiri, arus mengalir dari belakang ke depan . kawat a dan b secara berganti-gantian berada di kiri dan kanan. Karena itu arah arus di a dan arah arus di b selalu membolak balik. Pembalikan arah arus itu terjadi pada saat lilitan kawat melintasi posisi vertikal.

2.9.2 Pengendalian Arah Putaran Motor DC



Gambar 2.19 Arah Putaran Motor DC

Sumber : www.Sharon.1992

Dari gambar diatas, agar arah putaran motor dc berubah, maka polaritas tegangan pada baterai harus dibalik.

2.9.3 Jenis – jenis Motor DC

Motor DC berdasarkan jenis penguatannya terbagi menjadi 2 yaitu : motor DC penguatan terpisah dan motor DC penguatan sendiri. Penguatan pada motor DC diberikan oleh belitan medan sehingga jenis penguatan motor DC berdasarkan pada cara pemberian catu tegangan pada belitan medan yang akan menimbulkan medan magnet.

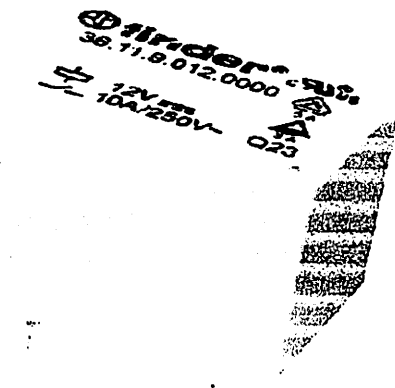
Motor DC penguatan terpisah dicatu oleh dua sumber tegangan terpisah pada belitan medan dan belitan jangkarnya. motor DC penguatan sendiri dicatu oleh satu sumber pada belitan medan dan belitan jangkarnya.

Motor DC penguatan sendiri berdasarkan cara menghubungkan belitan medan dan belitan jangkarnya menjadi tiga yaitu :

- Motor DC *shunt*, dimana belitan medan dan belitan jangkarnya dihubungkan paralel.
- Motor DC seri, belitan medan dan belitan jangkarnya dihubungkan seri.
- Motor DC *kompon* merupakan penggabungan dari motor DC *shunt* dan motor DC seri yang terbagi menjadi dua macam yaitu : kompon panjang dan kompon pendek

2.10 Relay

Relay merupakan salah satu jenis *saklar magnetic* yang dapat memutuskan atau menghubungkan kontak – kontak dengan arus yang dialirkan ke kumparan (inti). Sebuah *relay* terdiri dari satu kumparan dan inti, yang mana bila dialiri arus kumparan tersebut akan menjadi magnet dan menutup atau membuka kontak. Keuntungan *relay* adalah dapat menghubungkan daya yang besar dengan memberi daya yang kecil pada kumparannya.



Gambar 2.21 Bentuk Fisik Relay

Sumber : <http://www.omronrelay.com>.

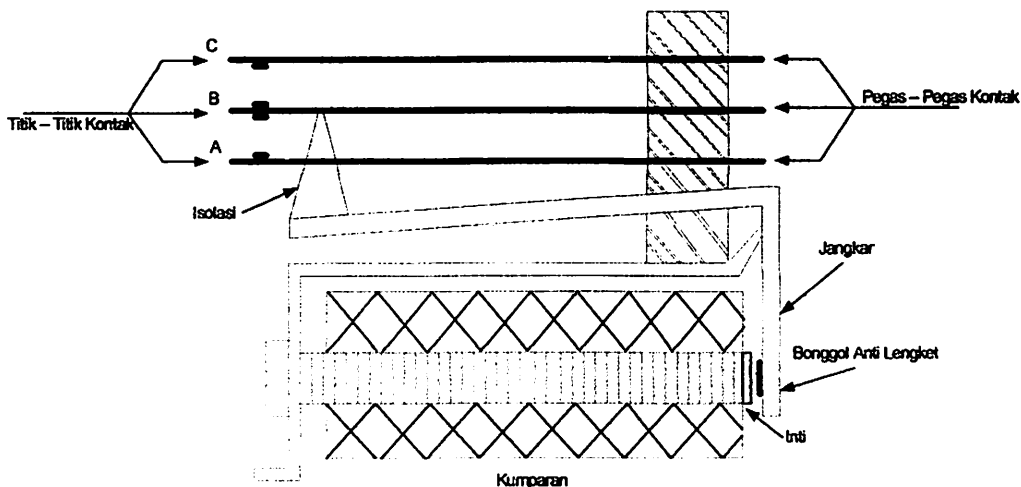
Pada dasarnya prinsip kerja *relay* sama dengan kontaktor, yaitu berfungsi untuk membuka dan menutup kontak listrik yang dikontrol dengan prinsip kerja elektromagnetik. Kerja dari *relay* tersebut adalah apabila arus mengalir di dalam kumparan yang memiliki inti besi akan menjadi magnet, maka jangkar yang terdiri dari besi lunak akan tertarik dan bergerak menggelinding pada engsel (*pivot*).

Relay dapat menggulingkan kalau gaya magnet dapat mengarahkan gaya pegas yang mengalahkannya, maka kontak pun menutup. Besarnya gaya magnet

ditentukan oleh kuat medan magnet pada celah udara antara jangkar dan inti besi, sedangkan kuat medan magnet tergantung pada jumlah lilitan kumparan dan kuat arus, kuat medan magnet ditetapkan juga oleh besar resistansi magnet dalam sirkuit kemagnetan. Kuat medan di celah udara akan semakin kuat bila letak jangkar semakin dekat dengan inti. Jarak jangkar dan inti dapat diatur dengan menyetel pencairan pegas.

Seperti halnya kontaktor, *Relay* dapat menggerakkan beberapa kontak sekaligus hanya dengan suatu kumparan jangkar.

Ada dua jenis *Relay*, yaitu : (1) *Relay* yang bekerja dengan arus bolak – balik, dan (2) *Relay* yang bekerja dengan arus searah. Jenis *Relay* yang bekerja dengan arus bolak – balik tidak bisa bekerja pada alat – alat elektronik.



Gambar 2.22 Konstruksi *Relay* Jenis Kontak Tukar

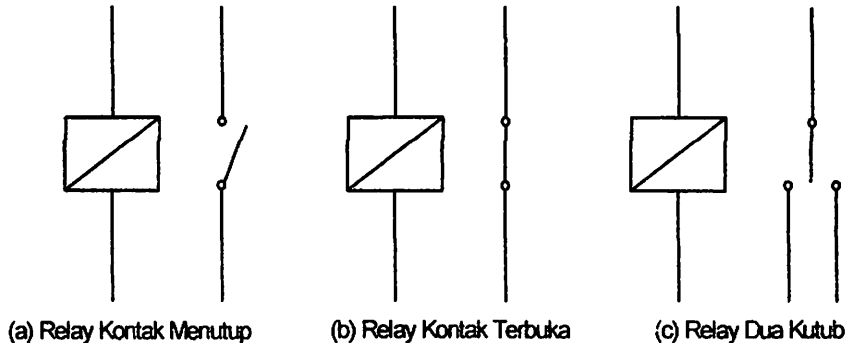
Sumber : <http://www.omronrelay.com>.

Pada gambar diatas bila kumparan dialiri arus listrik, maka akan timbul medan magnet pada lilitan tersebut. Karena adanya medan magnet ini, inti besi menjadi magnet dan menarik jangkar, sehingga kontak antara A dan B putus

(membuka), kontak B dan C menutup. Jenis *Relay* ini dinamakan dengan kontak tukar.

Jenis lain adalah jenis *Relay* dengan kontak menutup dimana apabila diberi arus listrik, maka kontak – kontaknya menutup. *Relay* dengan kontak membuka dimana

apabila kumparan *Relay* diberi arus listrik maka kontak – kontaknya akan membuka. Terdapat juga jenis *Relay* dengan dua kutub (*Bi – Polar*) dimana *Relay* ini mempunyai 2 kumparan dan 2 kondisi kerja. Bila *Relay* tidak diberi arus listrik, maka kontak B bebas, tidak menghubungkan kemana – mana. Kalau kumparan 1 terhubung dengan arus listrik, maka kontak B menghubungkan kontak A. Kalau kumparan 2 terhubung dengan arus listrik, maka kontak B terhubung dengan kontak C.



Sumber : <http://www.omronrelay.com>.

BAB III

PERENCANAAN DAN PEMBUATAN ALAT

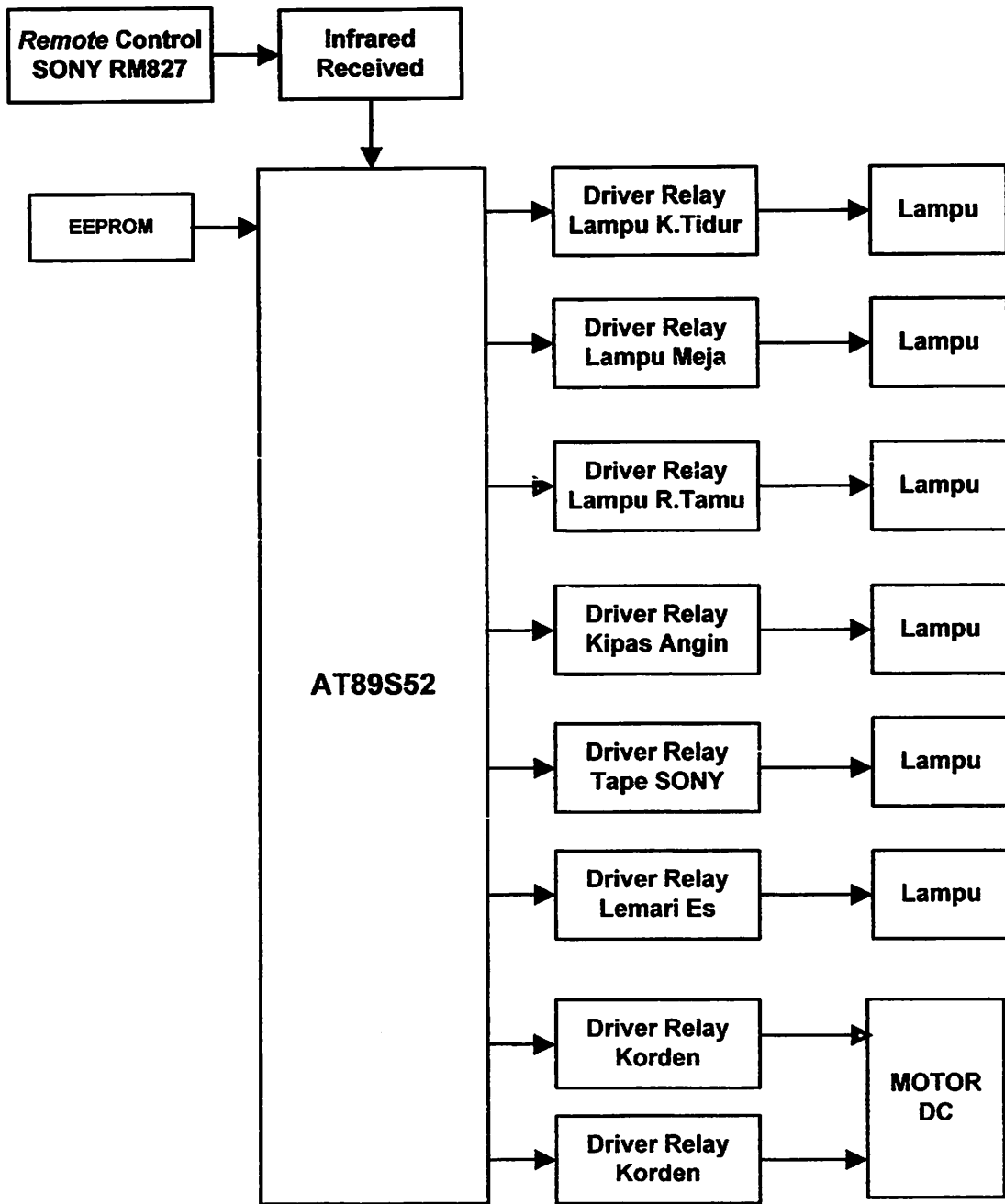
Pada bab ini dibahas tentang perencanaan dan pembuatan alat dari sistem yang direncanakan. Perencanaan dari sistem dan pembuatan alat secara garis besar dapat dibagi menjadi 2 yaitu : perencanaan perangkat keras (*Hardware*) dan perencanaan perangkat lunak (*Software*).

3.1 Perancangan Perangkat Keras (*Hardware*)

Pembuatan sistem kontrol peralatan listrik dan korden dengan memanfaatkan *Remote SONY* ini hanya dalam bentuk simulasi, dengan perencanaan dan prinsip kerja yang sesuai dengan peralatan yang sebenarnya.

Otomatisasi yang diterapkan dalam perencanaan alat ini yaitu merubah sistem yang masih manual. Komponen utama dari perangkat ini adalah Mikrokontroler AT89S52 yang berfungsi sebagai unit pengendali otomatisasi pada pengontrolan peralatan listrik dan korden pada rumah tangga. Berikut adalah blok sistem kontrol peralatan listrik dan korden pada rumah tangga

3.1.1 Blok Diagram Keseluruhan Sistem



Fungsi masing - masing diagram blok :

- **Remote kontrol Sony RM827T**

Menghasilkan kode – kode data biner untuk dikirim ke rangkaian *receiver*. Kode yang dikirimkan berupa data biner 12 bit yang terdiri dari 7 bit pertama berupa data *comand* dan 5 bit selanjutnya data *adres*. Nilai data yang dikirimkan dari masing – masing tombol sudah ditentukan oleh produsen pembuatnya.

- **Infrared Receiver**

Berfungsi untuk menangkap dan mendeteksi sinar Inframerah yang dikirimkan oleh *remote* untuk selanjutnya data-data dari *remote* dikirimkan kemikrokontroller AT 89S52

- **Mikrokontroler AT89S52**

Mikrokontroler yang digunakan disini memiliki fungsi menterjemahkan data dari *remote* dan hanya mengambil 7 bit pertama yaitu sebagai bit data. Sedangkan 5 bit berikutnya tidak diambil karena hanya data *address*.

- **EEPROM**

Berfungsi menyimpan isi data pada saat kondisi terakhir bahkan saat listrik sudah dimatikan dan isinya bisa dihapus melalui perintah elektrik

- **Driver Relay**

Berfungsi sebagai pengendali setelah mendapatkan instruksi dari mikrokontroler untuk mengaktifkan dan menonaktifkan lampu

- **Driver Relay Korden**

Berfungsi sebagai pengendali setelah mendapatkan instruksi dari mikrokontroler untuk membuka atau menutup korden

- **Lampu**

Befungsi sebagai indikator untuk mengetahui apakah alat listrik on atau off

3.1.2 Prinsip Kerja Alat

Saat tombol *remote* ditekan, *remote* mengirimkan sinyal yang berupa data biner 12 bit ke rangkaian *receiver*, kemudian rangkaian *receiver* menangkap dan mendeteksi sinar inframerah yang dikirimkan oleh *remote* dan dikirimkan ke mikrokontroler AT89S52, selanjutnya mikrokontroler menterjemahkan data dari *remote* dan hanya mengambil 7 bit pertama sebagai bit data sedangkan bit berikutnya tidak diambil karena hanya data *address*, mikrokontroler memberi perintah pada *driver relay* untuk mengaktifkan *relay* sesuai dengan tombol yang ditekan dan *relay* akan mengaktifkan peralatan listrik tersebut dengan indikator lampu, tetapi *driver relay* padakorden berfungsi untuk mengaktifkan Motor DC guna membuka dan menutup korden tersebut.

3.1.3 Penentuan Fungsi Tombol *Remote* Sony RM-827T

Nilai dari data biner yang dikirimkan oleh *Remote* Sony RM-827T sudah ditentukan besarnya oleh produsen *Sony*. Panjang *header* dan data *command* dari setiap produk *remote* *Sony* mempunyai nilai yang sama, hanya nilai data *address* yang berbeda dari setiap jenis *remote* yang disesuaikan dengan *device* pendukungnya. Dalam perancangan ini, *remote* digunakan untuk mengontrol 6 aplikasi, yaitu :

1. Lampu
2. Tape
3. Kipas Angin
4. Lemari Es
5. Korden

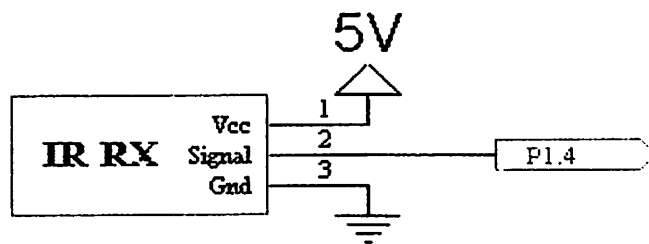
Untuk menentukan aplikasi yang diinginkan dapat dipilih melalui option-option yang terdapat pada perangkat lunak. Data yang dikirimkan ke *driver* pada semua aplikasi adalah dari data asli *remote*. tombol - tombol dari *remote* yang digunakan, ditunjukkan dalam tabel-tabel dibawah ini :

Tabel 3.1 Tombol *remote* yang dapat digunakan untuk mengontrol Aplikasi

Nama tombol	Data <i>Remote Control</i> (heksadesimal)	FUNGSI
MUTE	14	OFF Semua Lampu
POWER	54	ON Semua Lampu
DISPLAY	2E	-
1	0	ON/OFF Lampu K.Tidur
2	40	ON/OFF Lampu Meja
3	20	ON/OFF Lampu R.Tamu
4	60	ON kipas Angin
5	10	OFF Kipas Angin
6	50	ON Tape
7	30	OFF Tape
8	70	ON Lemari Es
9	8	OFF Lemari Es
1-	30	ON Korden
0	48	-
2+	58	OFF korden
SLEEP	36	-
+	17	-
-	57	-
a/b	74	-

SELECT	IF	-
PIC MODE	34	-
V+	24	-
V-	64	-
TV/VIDEO	52	-
PROG +	4	-
PROG -	44	-

3.1.4 Rangkaian Sensor IRM - 8510



Gambar 3.3 Perencanaan Rangkaian Modul Sensor IRM-8510

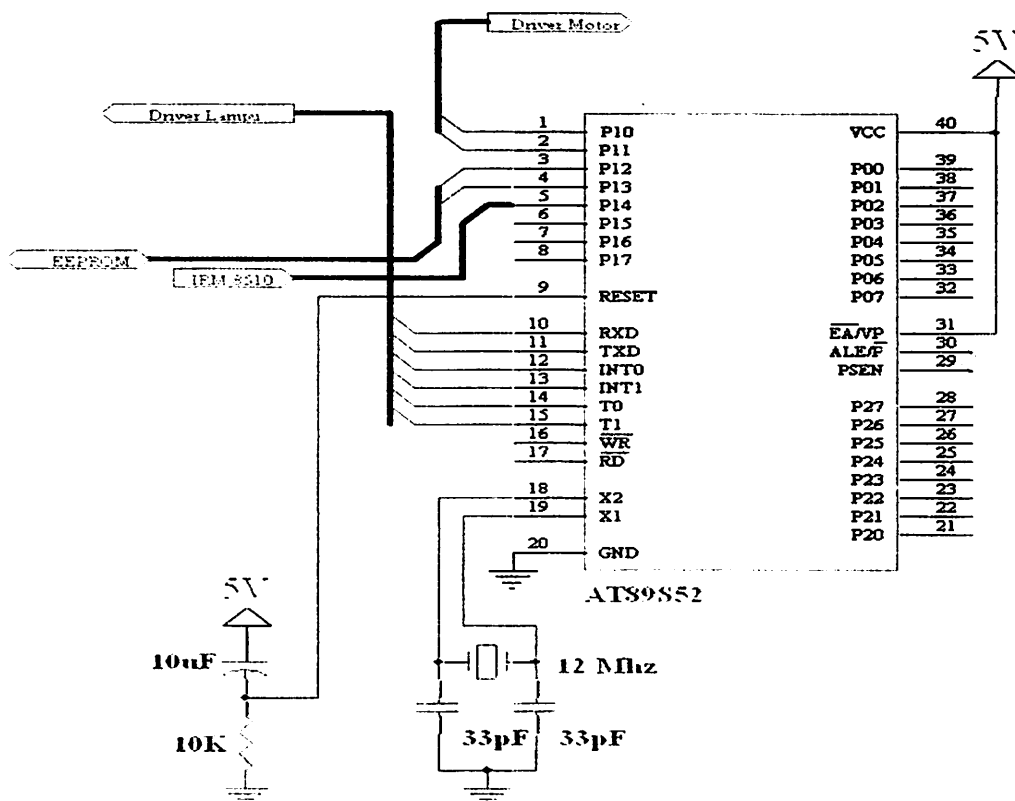
Pada aplikasi ini menggunakan sensor IRM- 8510 adalah modul yang berisi rangkaian penerima sinar inframerah yang bekerja pada frekwensi 40 Khz didalam sensor IRM 8510 terdapat fotodiode, AGC (*Active Gain Control*), bandpass, demodulator, dan *control circuit*. Fotodiode digunakan sebagai detektor inframerah, kemudian sinyal keluaran tersebut dikuatkan dan dikontrol oleh AGC agar sinyal keluaran tetap konstan. Setelah dikuatkan, sinyal keluaran dihubungkan ke bandpas Filter yang berfungsi untuk meloloskan frekwensi sinyal 40 Khz dari pemancar Inframerah. Rangkaian demodulator digunakan

untuk memisahkan sinyal data dari pemancar Inframerah. Sehingga keluaran dari IRM 8510 bisa langsung ke mikrokontroller.

. Port 1.4 sebagai inputan ke mikrokontroler AT89S52. pada sensor tersebut kaki no 1 berfungsi sebagai tegangan dari RX, pada kaki no 2 berfungsi menerima inputan sinyal dari *remote* kemudian pada kaki no 3 berfungsi sebagai ground .

3.1.5 Minimum system AT8952

Pada rangkaian kontrol ini komponen utamanya menggunakan mikrokontroler AT89S52. Sebagai tempat pengolahan data dan pengontrolan alat, pin-pin AT89S52 dihubungkan pada rangkaian pendukung membentuk suatu minimum sistem seperti ditunjukkan dalam Gambar



Gambar Perancangan Minimum Sistem AT89S52

Pin-pin mikrokontroler yang digunakan yaitu:

1. P1.0-P1.1 sebagai jalur data yang dihubungkan ke driver motor
2. P1.2 – P1.3 sebagai jalur data yang dihubungkan ke EEPROM.
3. P1.4 digunakan sebagai input dari sensor IRM 8510
4. RXD – T1 digunakan sebagai jalur data yang dihubungkan ke driver lampu
5. VCC dihubungkan dengan tegangan sebesar +5V
6. GND dihubungkan ke *ground* catu daya.
7. Reset digunakan untuk mereset program kontrol MCU, dimana MCU memiliki masukan aktif *high*.

3.1.6 Rangkaian *clock*

Kecepatan proses pengolahan data pada mikrokontroler ditentukan oleh *clock* (pewaktu) yang dikendalikan oleh mikrokontroler tersebut. Pada mikrokontroler AT89S52 terdapat *internal clock generator* yang berfungsi sebagai sumber *clock*, tapi masih memerlukan rangkaian tambahan untuk membangkitkan *clock* yang diinginkan.

Rangkaian tambahan ini terdiri atas 2 buah kapasitor dan sebuah kristal yang terangkai sedemikian rupa dan kemudian dihubungkan dengan port yang khusus tersedia pada mikrokontroler.

Dalam perancangan rangkaian ini menggunakan :

- 2 Kapasitor 33 pF. Penentuan besarnya kapasitansi disesuaikan dengan spesifikasi pada data sheet.
- Kristal 12 MHz

Dengan demikian perhitungannya dapat dilihat sebagai berikut :

$$f = 12 \text{ MHz}$$

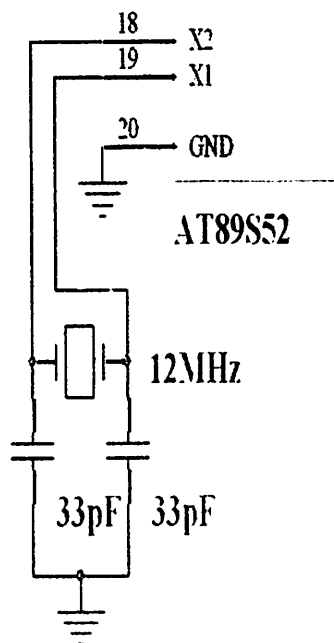
$$T = \frac{1}{f}$$

$$T = \frac{1}{12 \times 10^6}$$

karena 1 siklus mesin = 12T maka

$$1 \text{ siklus mesin} = 12 \times \frac{1}{12 \times 10^6} = 0,999 \mu\text{s}$$

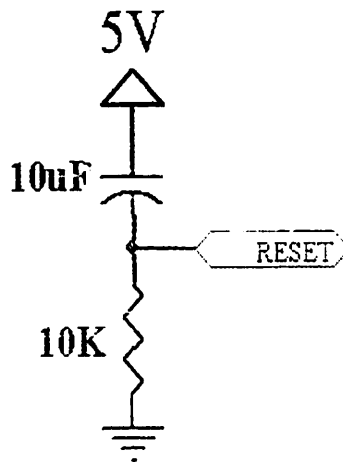
Adapun gambar rangkaian *clock* sebagai berikut :



Gambar 3.2 Rangkaian *Clock*

3.1.7 Rangkaian Reset

Reset pada mikrokontroler merupakan masukan aktif *high* '1' pulsa transisi dari rendah '0' ketinggian akan me-reset mikrokontroler menuju alamat 0000H. Pin reset dihubungkan dengan rangkaian *power-on reset* seperti pada gambar 3-3:



Gambar 3.3 Rangkaian Reset

Rangkaian *reset* bertujuan agar mikrokontroler dapat menjalankan proses dari awal. Rangkaian *reset* untuk mikrokontroler dirancang agar mempunyai kemampuan *power on reset*, yaitu *reset* yang terjadi pada saat sistem dinyalakan untuk pertama kalinya. *Reset* juga bisa dilakukan secara manual dengan menekan tombol *reset* yang berupa *switch push button*.

Rangkaian *reset* terbentuk oleh komponen resistor dan kapasitor yang sudah baku (ditetapkan oleh perusahaan pembuat IC AT89S52). Nilai resistor yang dipakai adalah $10K\Omega$ dan kapasitor $10\mu F$. Karena kristal yang digunakan mempunyai frekuensi sebesar 12 MHz, maka satu periode membutuhkan waktu sebesar :

$$T = \frac{1}{f_{XTAL}} = \frac{1}{12MHz} S = 8,333 \times 10^{-8}$$

Sehingga waktu minimal logika yang dibutuhkan untuk me-reset mikrokontroller adalah :

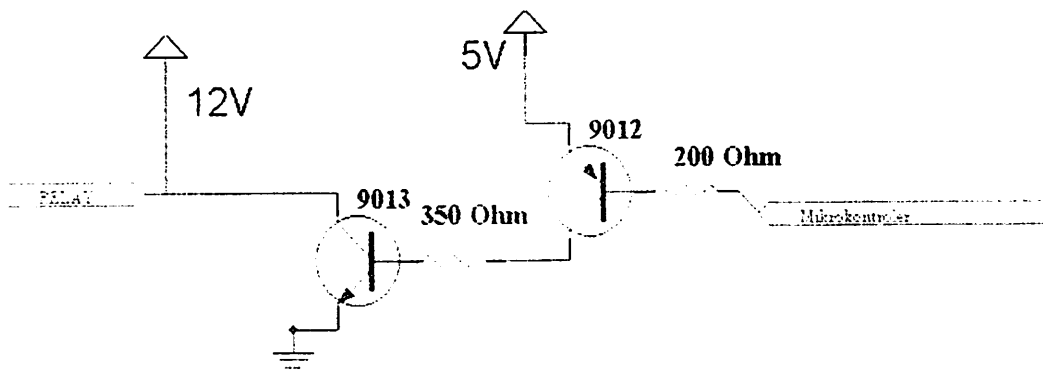
$$\begin{aligned} \text{Reset (minimal)} &= T \times \text{periode yang dibutuhkan} \\ &= 8,333 \times 10^{-8} \times 12 = 1,999 \mu s \end{aligned}$$

Jadi mikrokontroller membutuhkan waktu minimal 1,999 μs untuk me-reset. Waktu inilah yang dijadikan pedoman untuk menentukan nilai R dan C. Dengan menentukan nilai R = 10 k Ω dan C = 10 μF , maka :

$$T = 0.357 R.C = 0,357 \times 10000 \Omega \times 10.10^{-6} = 35,7 \text{ ms}$$

Jadi dengan nilai komponen R = 10 k Ω dan C = 10 μF dapat memenuhi syarat minimal untuk waktu yang dibutukan mikrokontroller

3.1.8 Rangkaian Driver lampu



Gambar 3.4 Rangkaian Driver lampu

Untuk rangkaian driver lampu digunakan transistor sebagai pengendali nyala, Prinsip kerja pada rangkaian diatas terletak pada *input* yang dibcrikan pad *basis* transistor pertama. jika basis transistor pertama mendapatkan *logic low* (*V_{eb}* 1 = 0.7 volt) sampai transistor pertama dalam keadaan *saturasi* maka arus

mengalir menuju basis transistor kedua untuk mengaktifkan transistor kedua ($V_{be2} = 0,7$ Volt). pada keadaan ini kedua transistor dalam keadaan saturasi yang menyebabkan relay aktif.

transistor 9012 dapat dipicu tegangan 5 volt dan arus maksimum sebesar 80 mA. Transistor ini mampu menghidupkan dan mematikan relay yang hanya memiliki tegangan maksimal 12 volt dengan resistansi kumparan sebesar 150Ω dapat diketahui arus relay sebesar :

$$\begin{aligned}
 I_{C2} &= \frac{V_{CC}}{R_I} \\
 &= \frac{12V}{150\Omega} \\
 &= 0,08 \text{ Ampere} = 80 \text{ mA}
 \end{aligned}$$

Dengan menggunakan transistor 9013 yang mempunyai nilai $h_{FE} = 64$, $V_{be} = 0,7$ V maka dapat dihitung arus I_{B2} dan R_{B2} yang diperlukan

$$\begin{aligned}
 I_{B2} &= \frac{I_C}{h_{FE}} \\
 &= \frac{80}{64} \\
 &= 1.25 \text{ mA}
 \end{aligned}$$

$$\begin{aligned}
 R_{B2} &= \frac{V_{in} - V_{be}}{I_b} \\
 &= \frac{5V - 0,7V}{1,25mA} \\
 &= 344 \Omega
 \end{aligned}$$

Karena nilai resistansi diatas tidak ada dipasaran maka diambil nilai resistansi yang mendekati nilai 344Ω yaitu 350Ω . Sedangkan untuk mencari R_{B1} pada transistor PNP 9012 adalah sebagai berikut :

Diketahui : $h_{FE} 9012 = 40$

$$V_{be} = 0,7 \text{ V}$$

$$I_{C1} - I_{B2} = 0,8 \text{ mA}$$

Maka I_{B1} dan R_{B1} dapat dihitung :

$$I_{B1} = \frac{I_{c1}}{H_{fe}}$$

$$= \frac{80mA}{40}$$

$$= 0,02mA$$

$$R_{B1} = \frac{V_{in} - V_{be}}{I_{b1}}$$

$$= \frac{5 - 0,7}{0.02}$$

$$= \frac{4,3}{0,02}$$

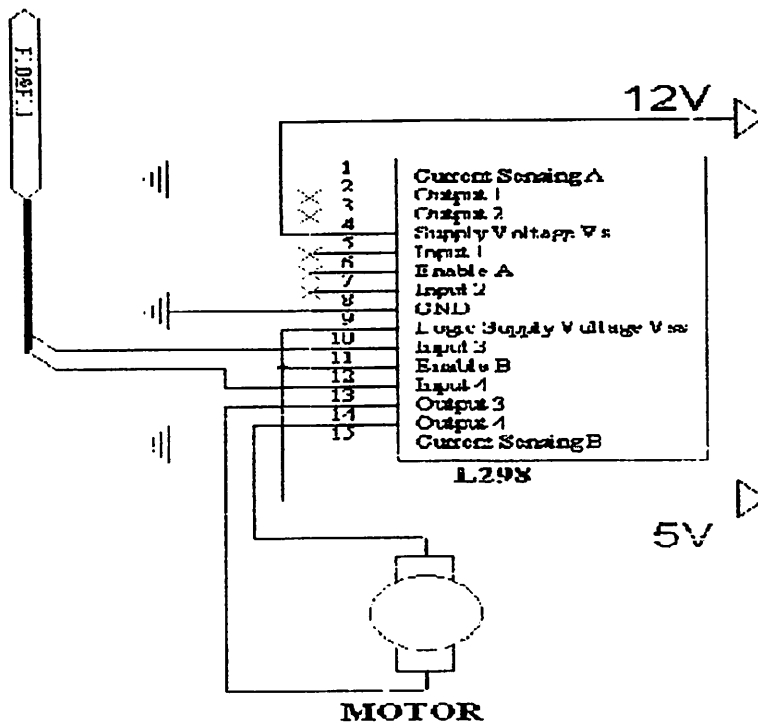
$$= 204\Omega$$

Karena nilai resistansi diatas tidak ada dipasaran maka diambil nilai resistansi yang mendekati nilai 204Ω yaitu 200Ω

Cara kerja rangkaian diatas adalah sebagai berikut :

1. Apabila kaki no 1 mendapatkan kondisi 1 maka pada kaki no 1 akan menjadi kondisi 0 akibatnya lampu no 1 akan menyala.
2. Apabila kaki no 1 mendapatkan kondisi 0 maka pada kaki no 1 akan menjadi kondisi 1 akibatnya lampu no 1 akan mati

3.1.9 Rangkain Driver Korden



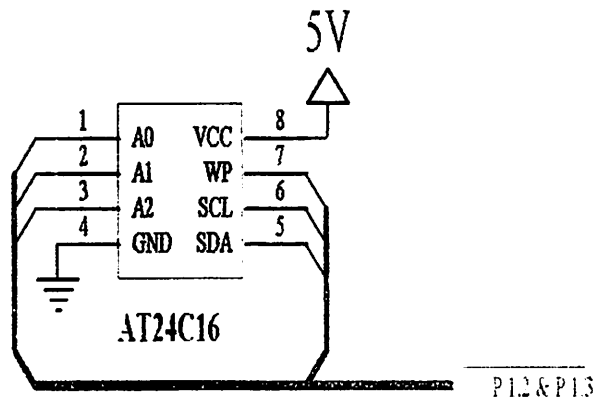
Gambar 3.5 Driver Motor

- Apabila pada driver motor mendapatkan inputan dari P1.0 dan P1.1 berupa logic 0 maka outputan dari driver tersebut sama dengan inputan yaitu 0 dan kondisi tersebut motor tidak akan bergerak.
- Apabila pada driver motor mendapatkan inputan dari P1.0 berupa logic 0 dan dari P1.1 berupa logic 1 maka outputan dari driver tersebut berupa logic 1 dan ada tegangan yang masuk sehingga kondisi motor tersebut bergerak membuka Korden.
- Apabila pada driver motor mendapatkan inputan dari P1.0 berupa logic 1 dan dari P1.1 berupa logic 0 maka outputan dari driver tersebut berupa logic 1 dan ada tegangan yang masuk kondisi motor tersebut bergerak menutup Korden.

- Apabila pada driver motor mendapatkan inputan dari P1.0 berupa logic 1 dan dari P1.1 berupa logic 1 maka outputan dari driver tersebut berupa logic 0 dan tidak ada tegangan yang masuk kondisi motor tersebut tidak akan bergerak .

3.1.10 Minimum Sistem AT24C16

Pada perancangan sistem ini digunakan *Electrically Erasable Programmable Read Only Memory* (EEPROM) AT24C16 sebagai memory tambahan, disini EEPROM berfungsi sebagai penyimpanan sementara data pada kondisi terakhir sehingga misalkan terdapat listrik padam maka EEPROM ini menyimpan data sehingga pada waktu Listrik menyala maka kondisi terakhir tersebut akan tetap seperti sebelum listrik menyala.



Gambar 3.6 Rangkaian AT24C16

- Pin 1 – Pin 8 (A0 - SDA) yaitu sebagai alamat data yang dihubungkan ke output dari port 1.2 dan port 1.3 pada mikrokontroler.

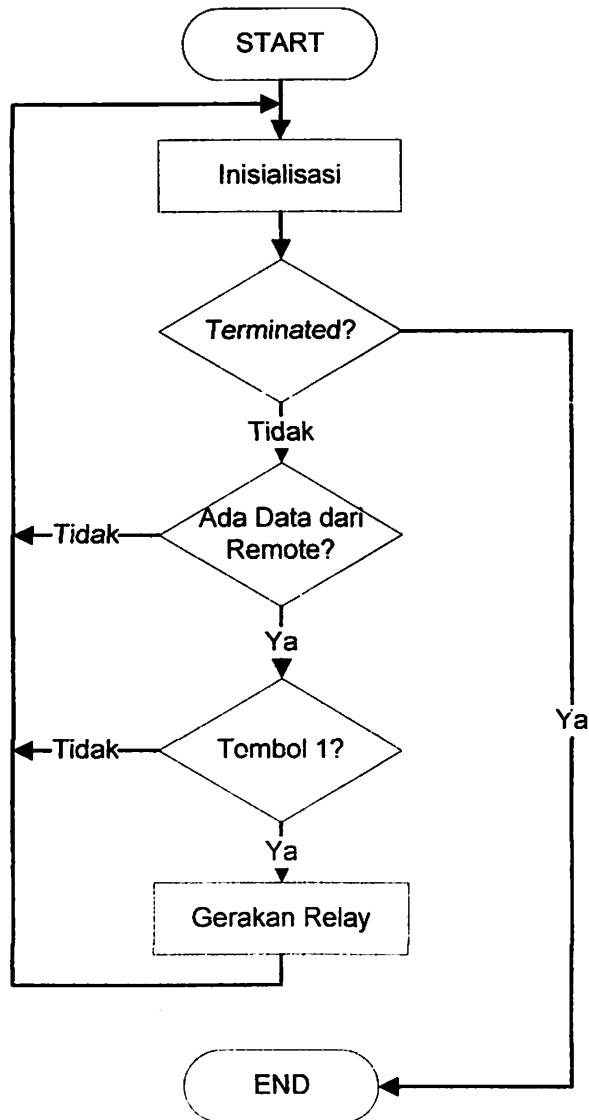
3.2 Perancangan Perangkat Lunak

Perancangan perangkat lunak (*software*) yang digunakan dalam perencanaan dan pembuatan alat akan dipaparkan dalam *flowchart* sistem secara keseluruhan..

Diagram alir atau *Flowchart* program secara keseluruhan seperti pada gambar

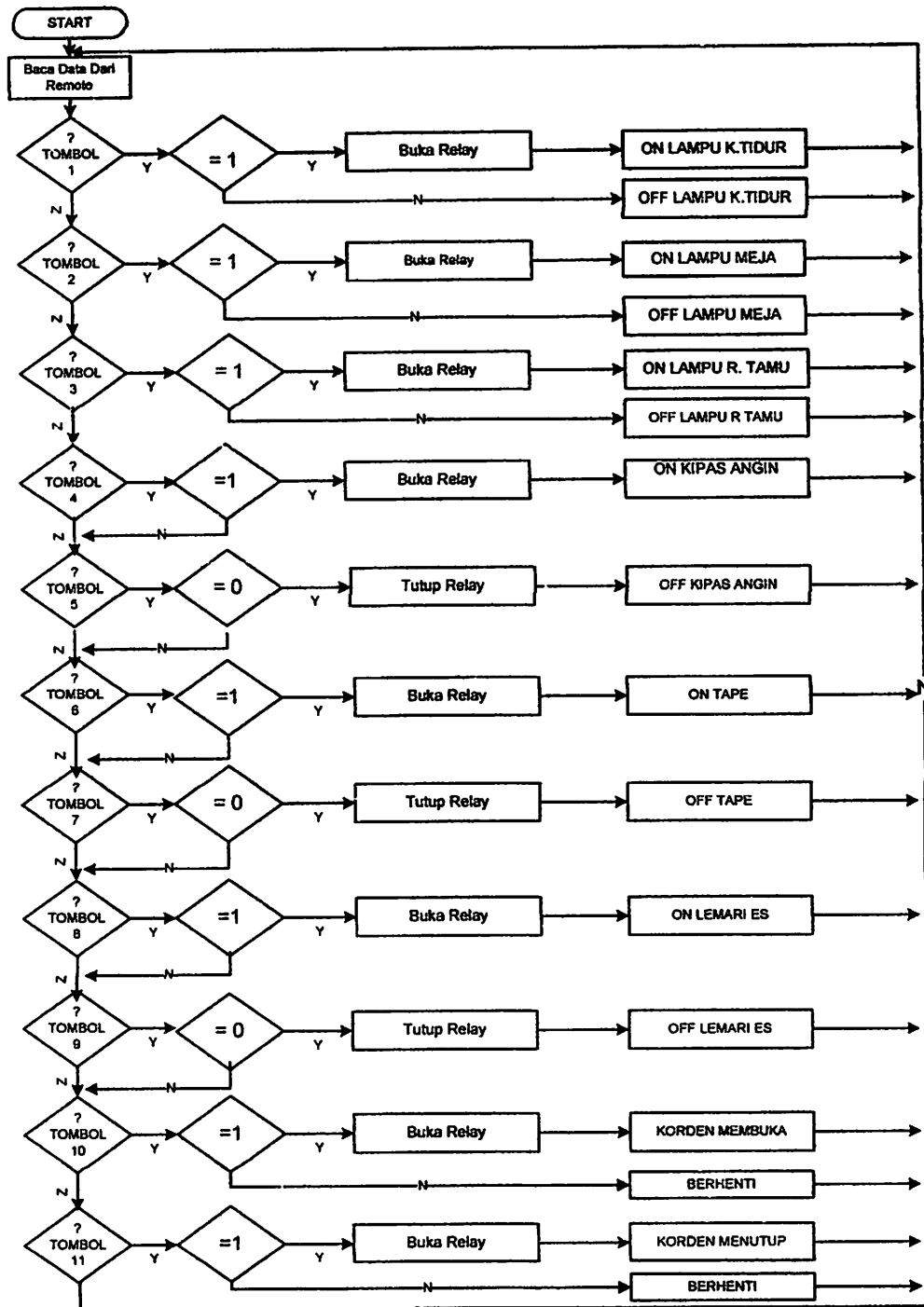
3.7:

3.2.1 Flowchart Program Utama



Gambar 3.7 Gambar Flowchart Program Utama

3.2.2 Flowchart Aplikasi



Gambar 3.8 Gambar Flowchart Aplikasi

BAB IV

PENGUJIAN DAN HASIL ANALISA

Pengujian dilakukan untuk mengetahui sejauh mana peralatan dapat bekerja sesuai dengan perencanaan. Langkah pengujian dilakukan melalui 2 tahap, yakni pengujian pada setiap blok dan pengujian pada sistem keseluruhan. Tahap pertama dimaksudkan untuk mengetahui sejauh mana blok-blok rangkaian dapat berjalan, sedangkan tahap kedua dilakukan setelah diperoleh kepastian bahwa tiap blok rangkaian telah berjalan sesuai rencana.

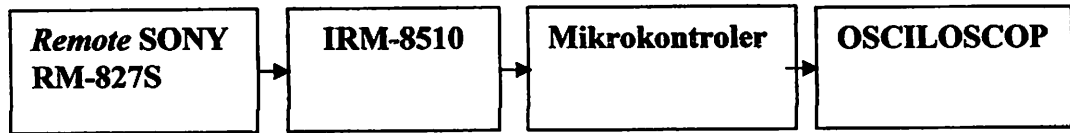
4.1. Pengujian Remote Sony RM – 827S

4.1.1. Tujuan

Untuk mengetahui nilai Data dari *Remote* Sony RM-827T dan bentuk Sinyal yang dihasilkan.

4.1.2. Peralatan yang digunakan

1. *Remote* Sony RM-827T.
2. Osciloskop
3. Fotodioda
4. Rangkaian Op-Amp(LM741)
5. Catu daya 5V.



Gambar 4.1 Rangkain pengujian *remote* Sony RM-827S

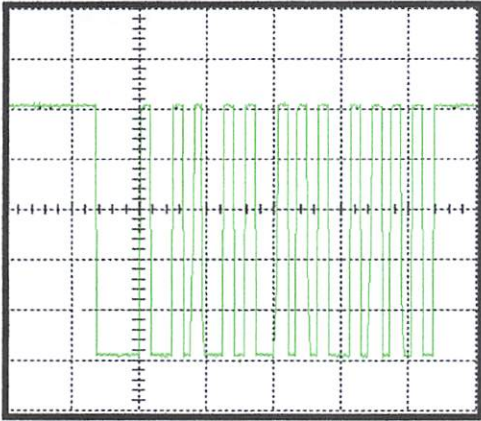
4.1.3. Langkah Pengujian

1. Merangkai rangkaian pengujian seperti pada gambar 4.1
2. Memberikan Catu Daya sebesar 5V
3. Memberikan Sinyal Masukan melalui *Remote* Sony Rm-827T dan mengatur nilai R4 untuk mendapatkan sinyal yang kuat
4. Mengambil gambar dari Osciloskop untuk setiap hasil pengujian tombol *remote* Sony RM-827T

4.1.4 Hasil Pengujian

1. Tombol = *POWER*

Data = 1010100 10000



T/Div = 1ms

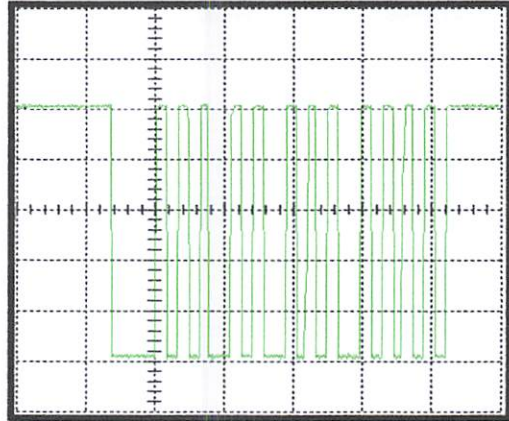
V/Div = 5V

Gambar 4.2 Hasil pengujian tombol

POWER

2. Tombol = *MUTE*

Data = 0010100 10000



T/Div = 1ms

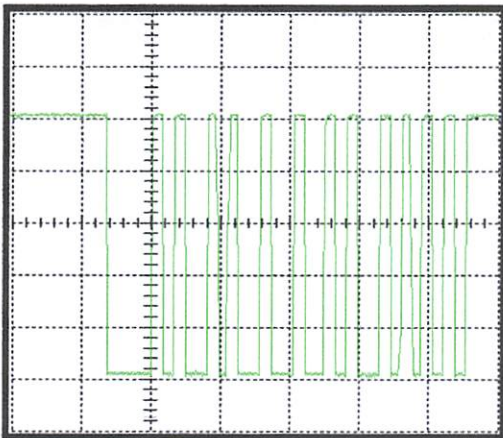
V/Div = 5V

Gambar 4.3 Hasil pengujian tombol

MUTE

3. Tombol = *DISPLAY*

Data = 0101110 10000



T/Div = 1ms

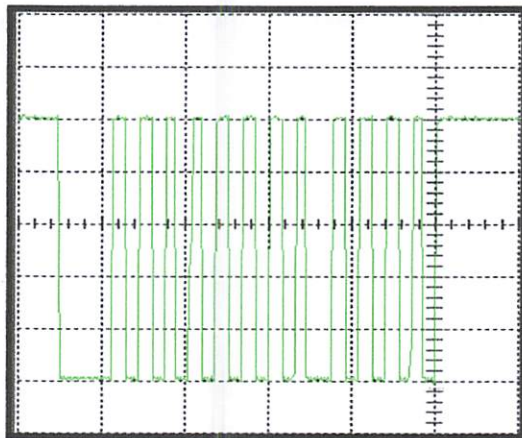
V/Div = 5V

Gambar 4.4 Hasil pengujian tombol

DISPLAY

4. Tombol = 1

Data = 0000000 10000



T/Div = 1ms

V/Div = 5V

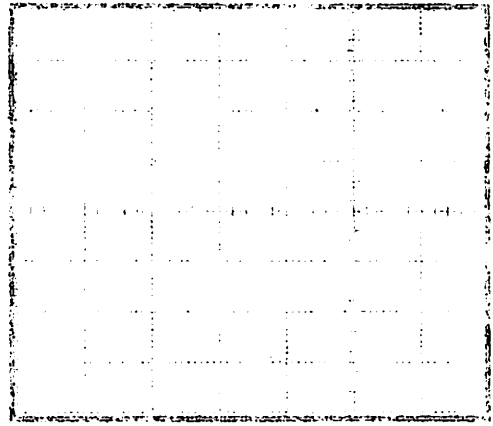
Gambar 4.5 Hasil pengujian tombol

1

4.1.4 Hasil Pengujian

1. Tombol = POWER

Data = 1010100 10000



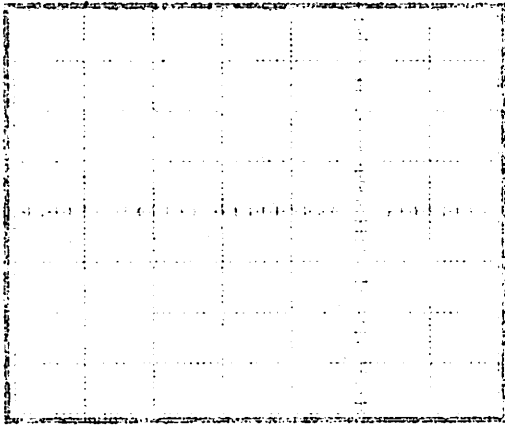
Time Div = 1ms
V-Div = 2V

Gambar 4.2 Hasil pengujian tombol

POWER

2. Tombol = WRITE

Data = 0010100 10000



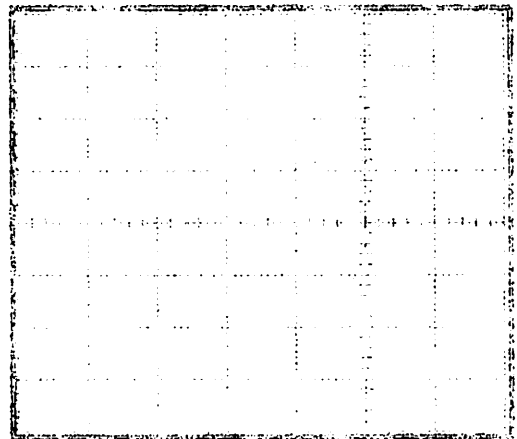
Time Div = 1ms
V-Div = 2V

Gambar 4.3 Hasil pengujian tombol

WRITE

3. Tombol = DISPLAY

Data = 0101110 10000



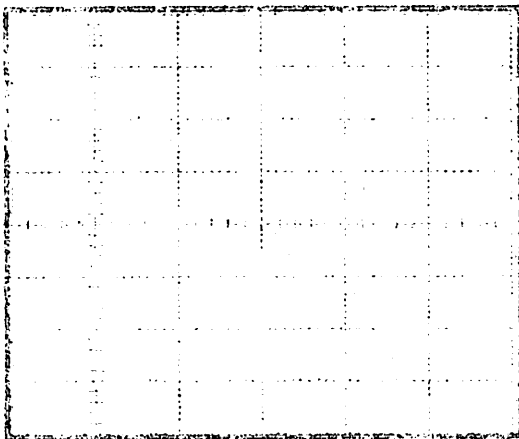
Time Div = 1ms
V-Div = 2V

Gambar 4.4 Hasil pengujian tombol

DISPLAY

4. Tombol = 1

Data = 0000000 10000



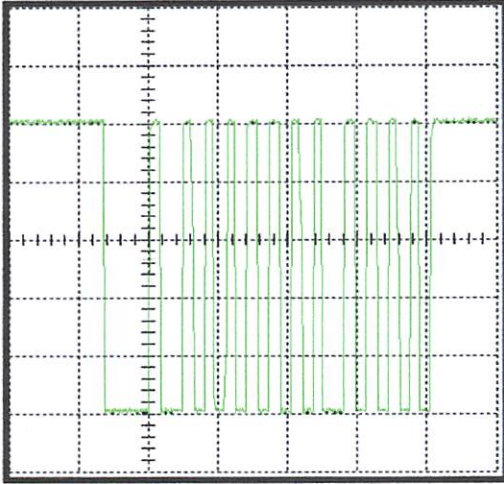
Time Div = 1ms
V-Div = 2V

Gambar 4.5 Hasil pengujian tombol

1

5. Tombol = 2

Data = 1000000 10000

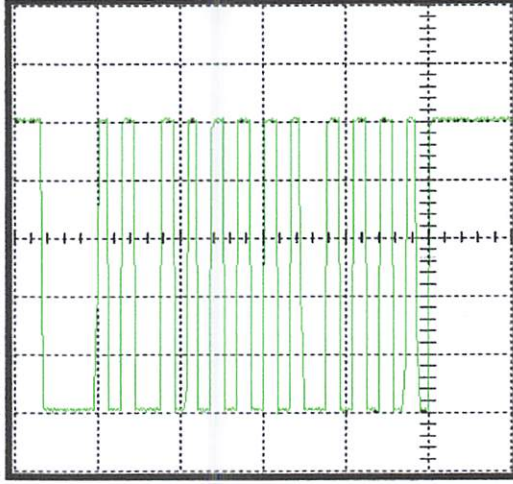


T/Div = 1ms
V/Div = 5V

Gambar 4.6 Hasil pengujian tombol 2

6. Tombol = 3

Data = 0100000 1 00

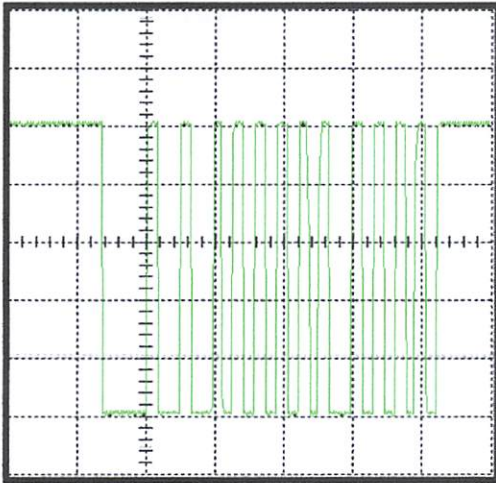


T/Div = 1ms
V/Div = 5V

Gambar 4.7 Hasil pengujian tombol 3

7. Tombol = 4

Data = 1100000 10000

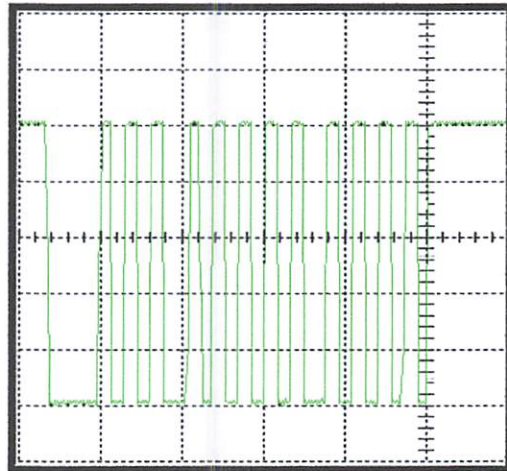


T/Div = 1ms
V/Div = 5V

Gambar 4.8 Hasil pengujian tombol 4

8. Tombol = 5

Data = 0010000 10000

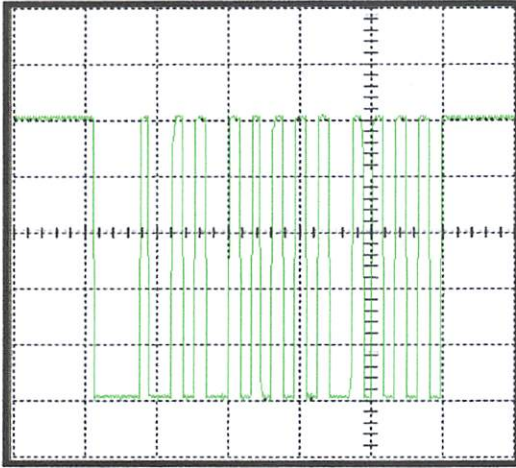


T/Div = 1ms
V/Div = 5V

Gambar 4.10 Hasil pengujian tombol 5

9. Tombol = 6

Data = 1010000 10000

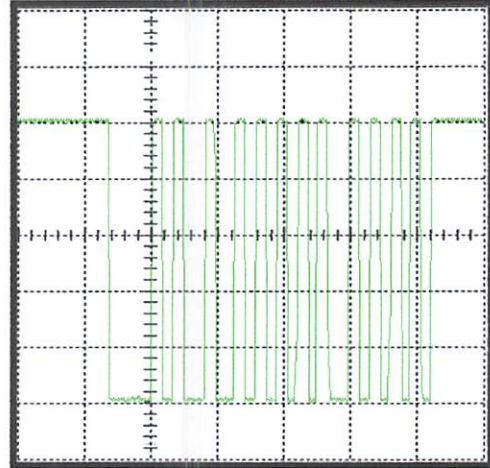


T/Div = 1ms
V/Div = 5V

Gambar 4.11 Hasil pengujian tombol 6

10. Tombol = 7

Data = 0110000 10000

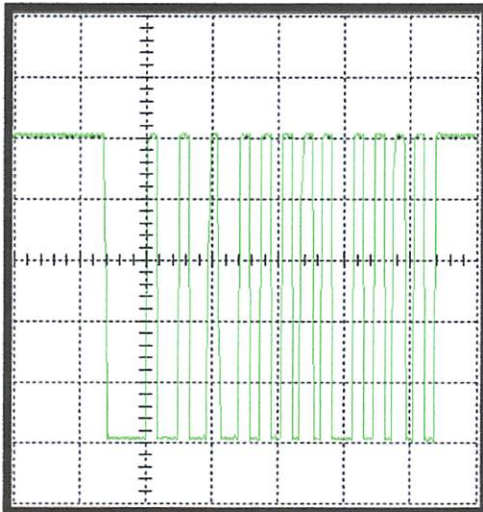


T/Div = 1ms
V/Div = 5V

Gambar 4.12 Hasil pengujian tombol 7

11. Tombol = 8

Data = 1110000 10000

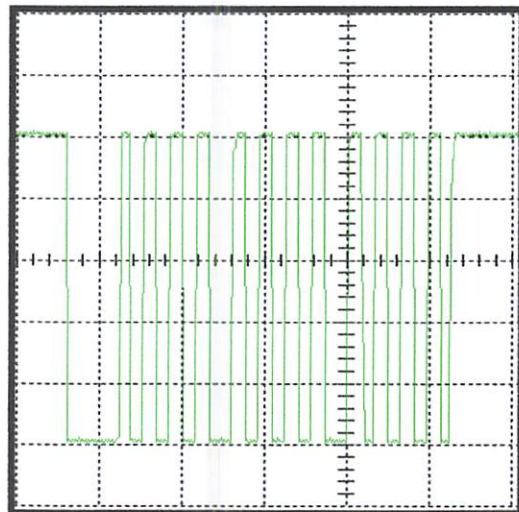


T/Div = 1ms
V/Div = 5V

Gambar 4.14 Hasil pengujian tombol 8

12. Tombol = 9

Data = 0001000 10000

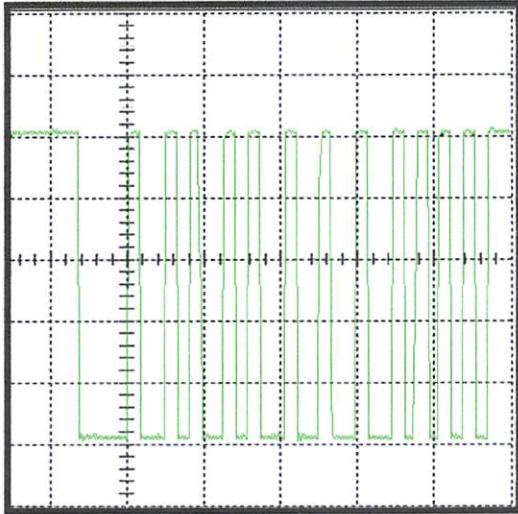


T/Div = 1ms
V/Div = 5V

Gambar 4.15 Hasil pengujian tombol 9

13. Tombol = 1-

Data = 00110000 10000



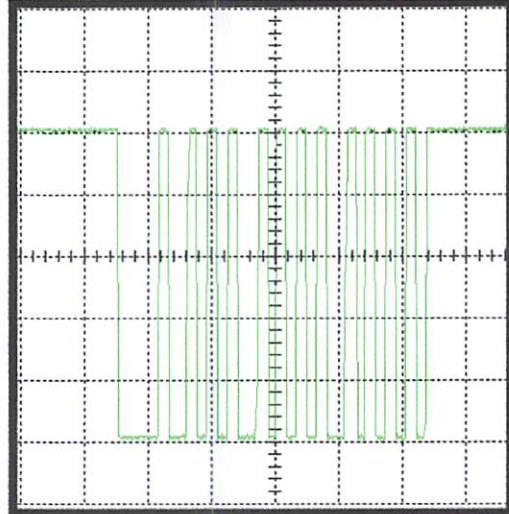
T/Div = 1ms

V/Div = 5V

Gambar 4.16 Hasil pengujian tombol 1-

14. Tombol = 0

Data = 1001000 10000



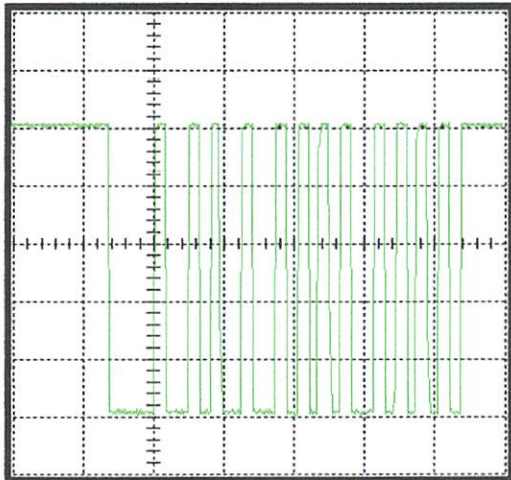
T/Div = 1ms

V/Div = 5V

Gambar 4.17 Hasil pengujian tombol 0

15. Tombol = 2-

Data = 1011000 10000



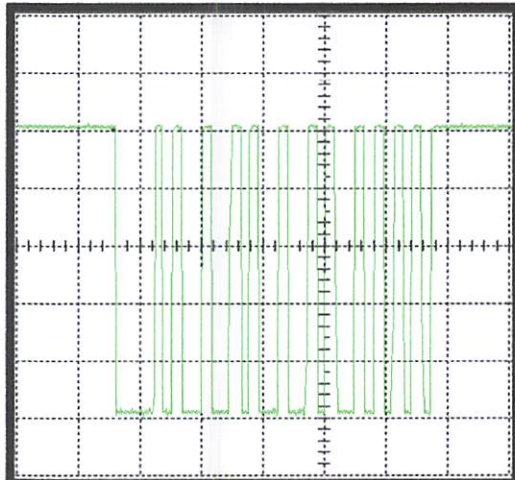
T/Div = 1ms

V/Div = 5V

Gambar 4.18 Hasil pengujian tombol 2-

16. Tombol = SLEEP

Data = 0110110 10000



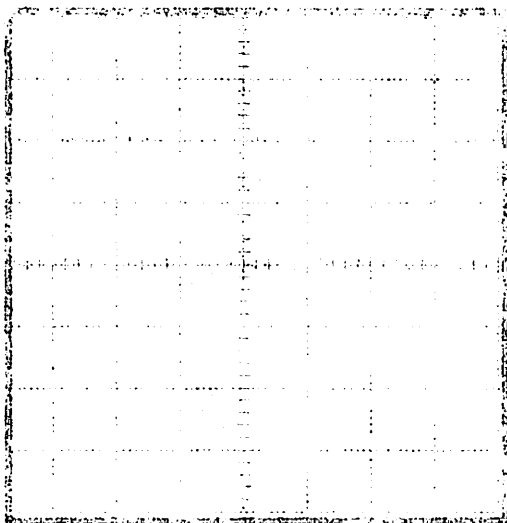
T/Div = 1ms

V/Div = 5V

Gambar 4.19 Hasil pengujian tombol
SLEEP

14. Tombol = 0

Data = 1001000 10000

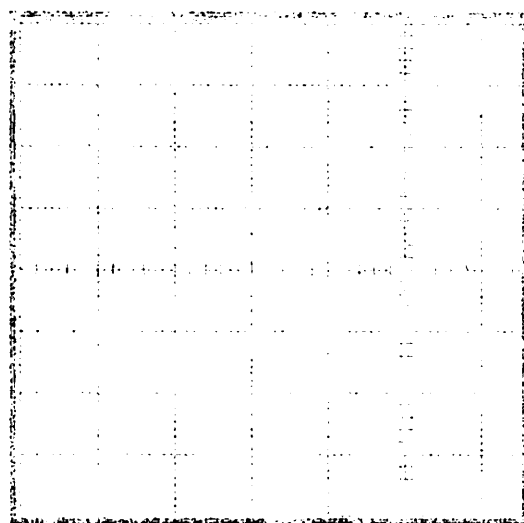


INDIC = 1ms
VINDIC = 2V

Gambar 4.17 Hasil pengujian tombol 0

13. Tombol = 1

Data = 00110000 10000

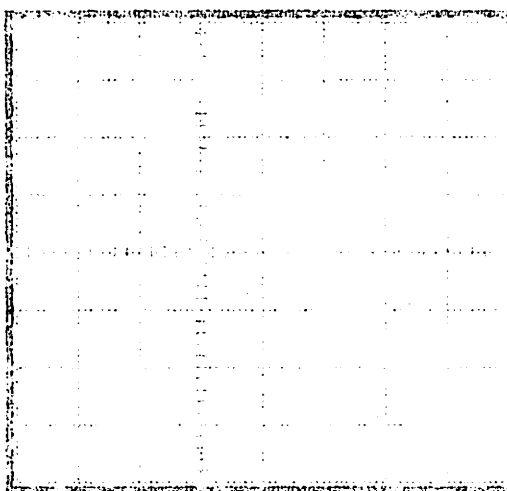


INDIC = 1ms
VINDIC = 2V

Gambar 4.16 Hasil pengujian tombol 1

16. Tombol = 2 (AKA)

Data = 0110110 10000



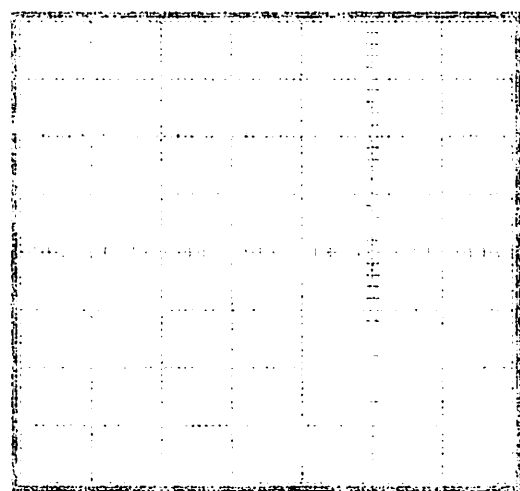
INDIC = 1ms
VINDIC = 2V

Gambar 4.19 Hasil pengujian tombol

2 (AKA)

17. Tombol = 3

Data = 1011000 10000

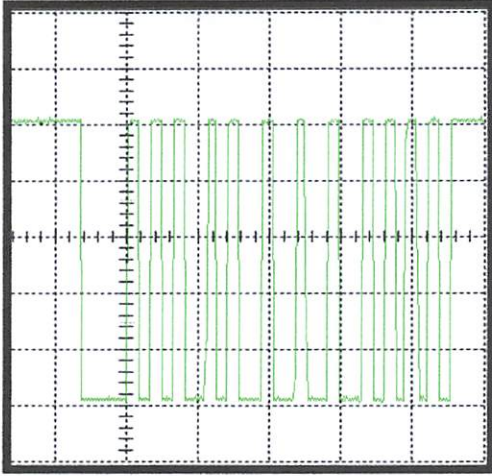


INDIC = 1ms
VINDIC = 2V

Gambar 4.18 Hasil pengujian tombol 3

17. Tombol = +

Data = 0010111 10000

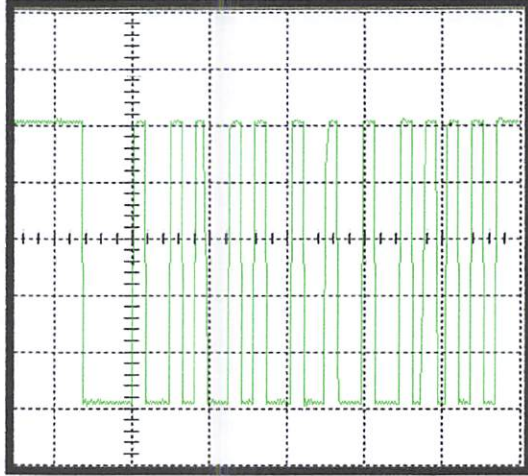


T/Div = 1ms
V/Div = 5V

Gambar 4.20 Hasil pengujian tombol +

18. Tombol = -

Data = 1010111 10000

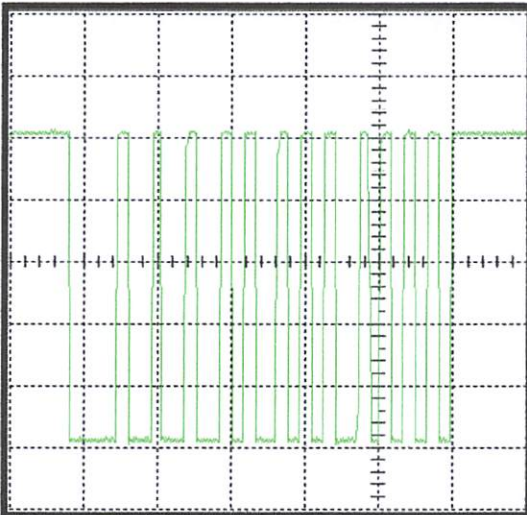


T/Div = 1ms
V/Div = 5V

Gambar 4.21 Hasil pengujian tombol -

19. Tombol = A/B

Data = 1110100 10000

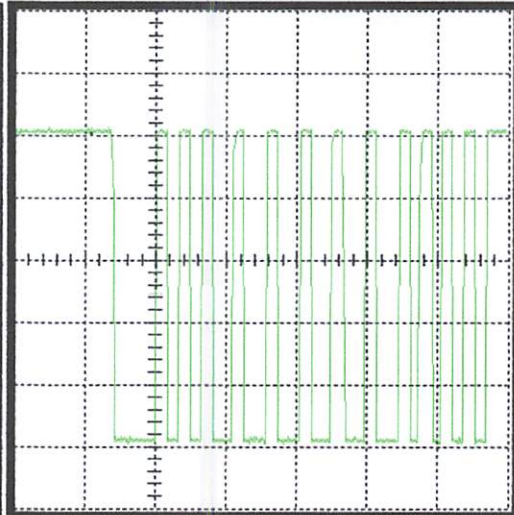


T/Div = 1ms
V/Div = 5V

Gambar 4.2 Hasil pengujian tombol A/B

20. Tombol = SELECT

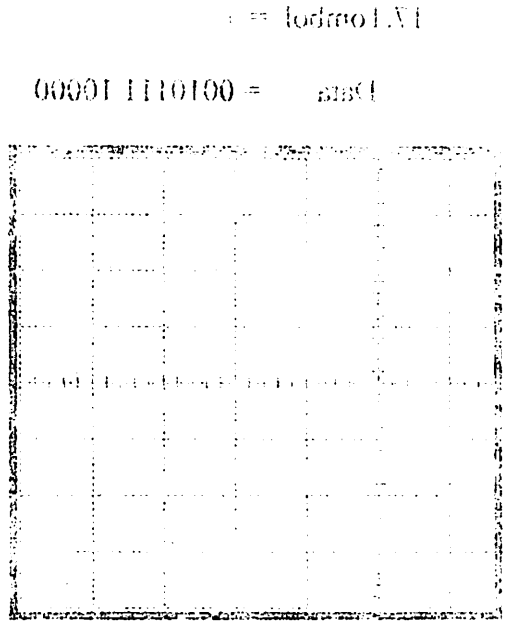
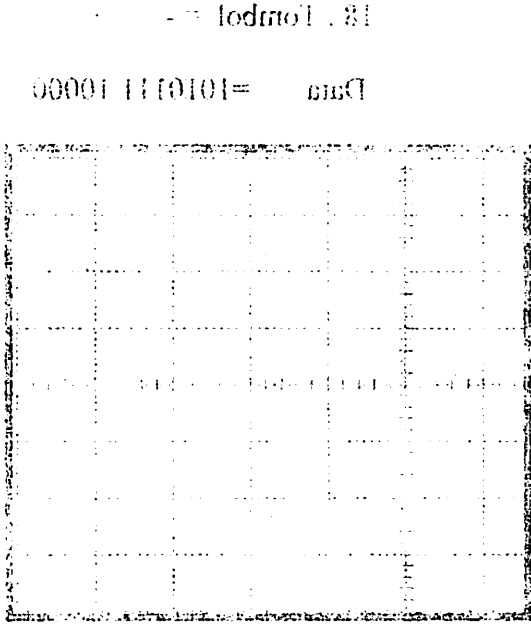
Data = 0011111 10000



T/Div = 1ms
V/Div = 5V

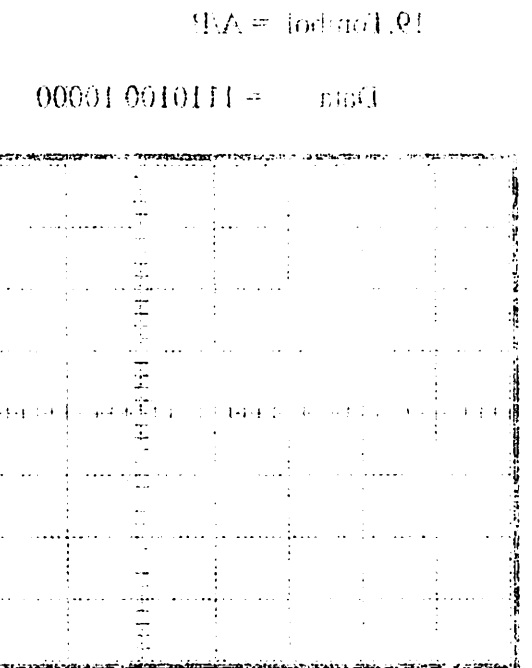
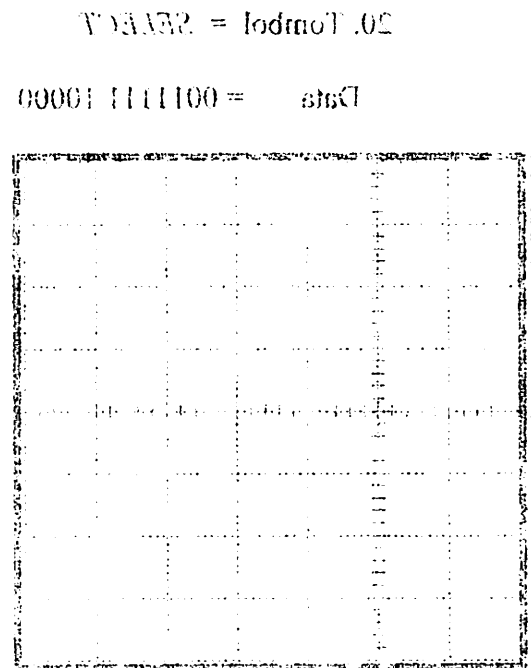
Gambar 4.3 Hasil pengujian tombol

SELECT



Gambar 4.21 Hasil pengujian tombol

Gambar 4.20 Hasil pengujian tombol =



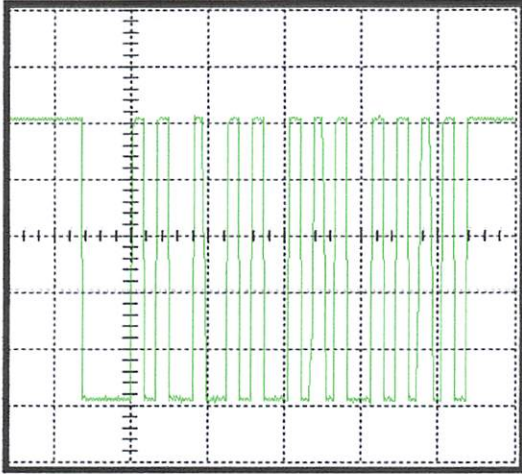
Gambar 4.3 Hasil pengujian tombol

Gambar 4.2 Hasil pengujian tombol AB1

SELECT

21. Tombol = *PIC MODE*

Data = 0110100 10000



T/Div = 1ms

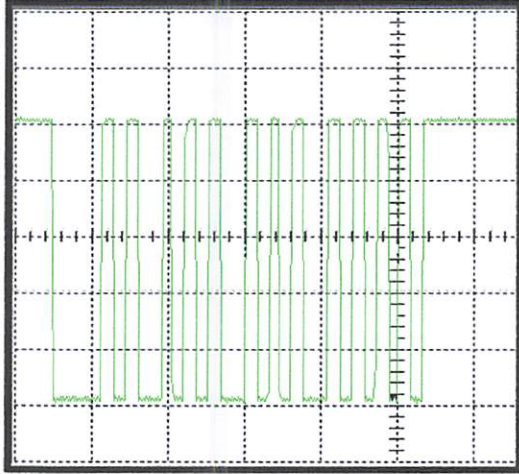
V/Div = 5V

Gambar 4.2 Hasil pengujian tombol

PIC MODE

22. Tombol = VOL +

Data = 0100100 10000



T/Div = 1ms

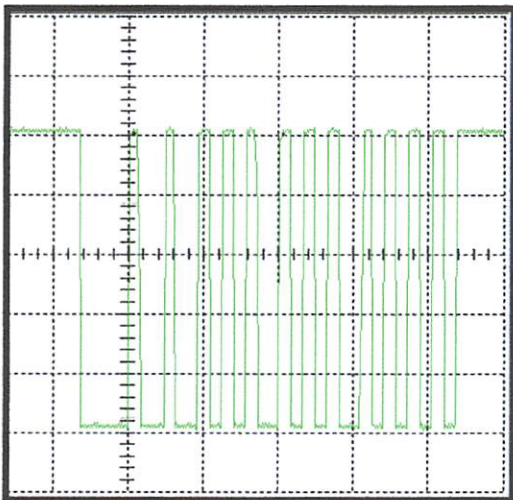
V/Div = 5V

Gambar 4.3 Hasil pengujian tombol

VOL +

23. Tombol = VOL -

Data = 1100100 10000



T/Div = 1ms

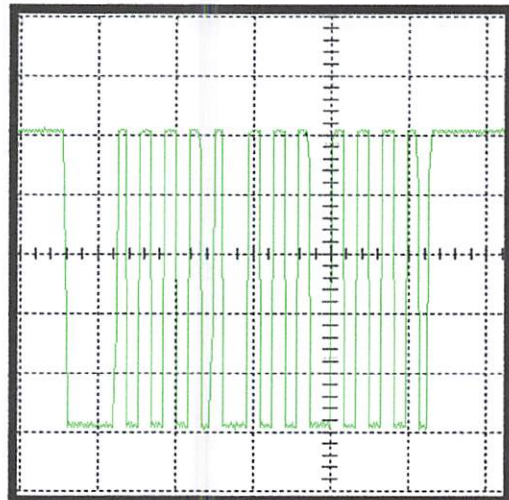
V/Div = 5V

Gambar 4.2 Hasil pengujian tombol

VOL -

24. Tombol = PROG +

Data = 0000100 10000



T/Div = 1ms

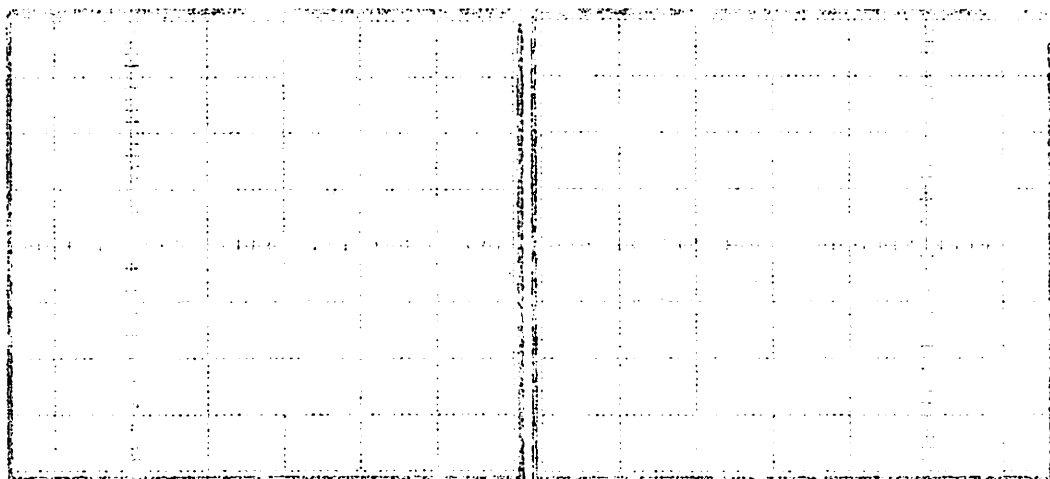
V/Div = 5V

Gambar 4.3 Hasil pengujian tombol

PROG +

21. Tombol = PWC MODE

Data = 011010010000



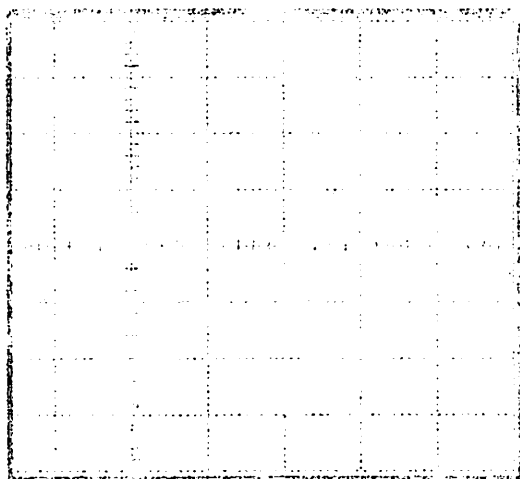
T.DIV = 1ms
V.DIV = 2V

Gambar 4.3 Hasil pengujian tombol

PWC MODE

22. Tombol = VOL +

Data = 010010010000



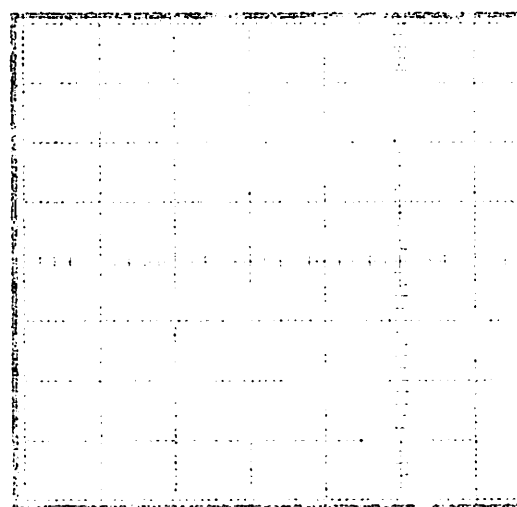
T.DIV = 1ms
V.DIV = 2V

Gambar 4.3 Hasil pengujian tombol

VOL +

23. Tombol = VOL -

Data = 110010010000



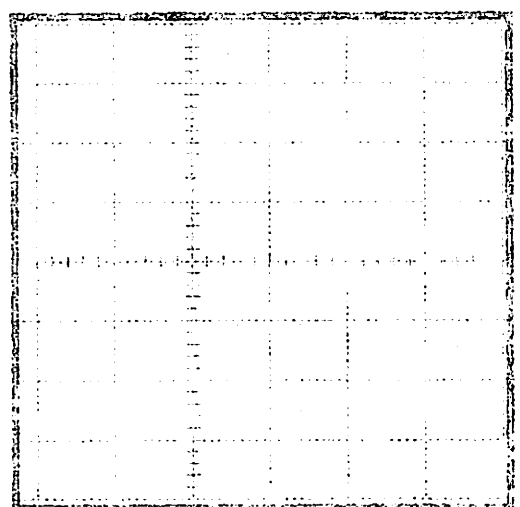
T.DIV = 1ms
V.DIV = 2V

Gambar 4.3 Hasil pengujian tombol

VOL -

24. Tombol = PROG +

Data = 000010010000



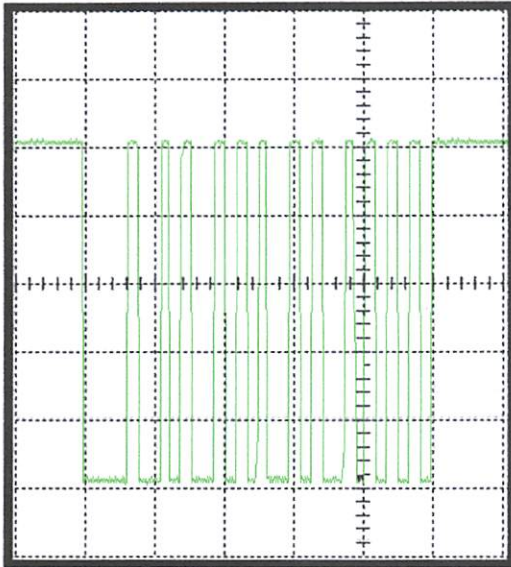
T.DIV = 1ms
V.DIV = 2V

Gambar 4.3 Hasil pengujian tombol

PROG +

25. Tombol = TV/VIDEO

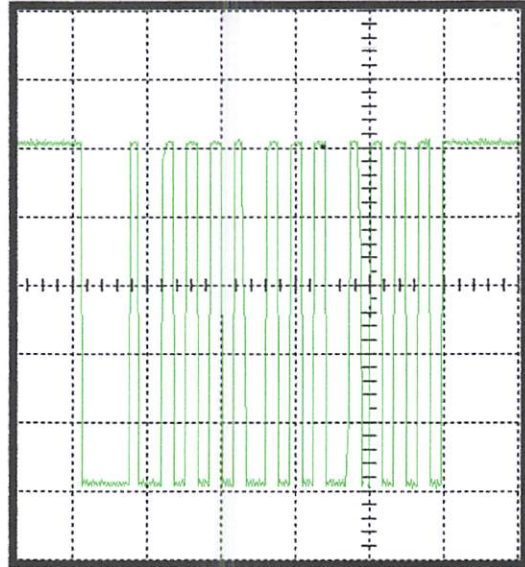
Data = 1010010 10000



T/Div = 1ms
V/Div = 5 V

26. Tombol = PROG -

Data = 1000100 10000



T/Div = 1ms
V/Div = 5 V

Gambar 4.2 Hasil pengujian tombol
TV/VIDEO

Gambar 4.3 Hasil pengujian tombol
PROG -

Dari gambar hasil pengujian diatas maka dapat diperoleh perhitungan sebagai berikut :

Untuk data :

T/Div : 1ms

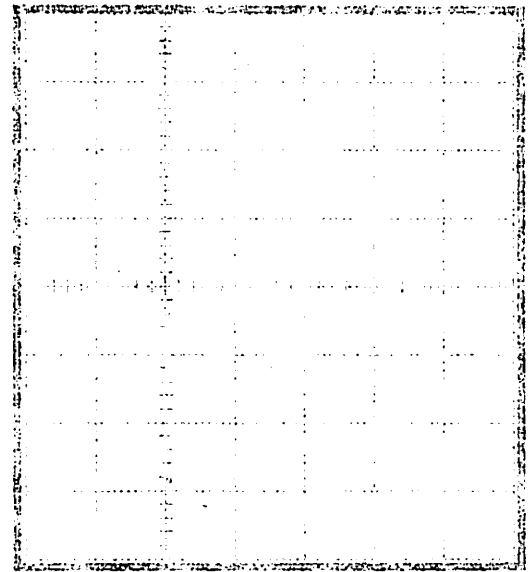
Skala tinggi gelombang : 5V

$$\begin{aligned} T &= \text{Skala gelombang} \times T/\text{Div} \\ &= 5 \times 1\text{ms} = 5 \text{ ms} \end{aligned}$$

Dari hasil perhitungan diatas maka dapat diambil kesimpulan bahwa hasil perhitungan waktu pulsa adalah sama dengan data yang sebenarnya

52. Tombol = TVAUDIO

Data = 1010010 1000



V/div = 2 V
t/div = 1 ns

Gambar 4.3 Hasil pengujian tombol

TVAUDIO

Dari gambar hasil pengujian diatas maka dapat diperoleh perhitungan sebagai berikut :

periode :

Quant data :

T/div : 1 ns

Skala tinggi gelombang : 2V

$$T = \text{Skala gelombang} \times \text{T/div}$$

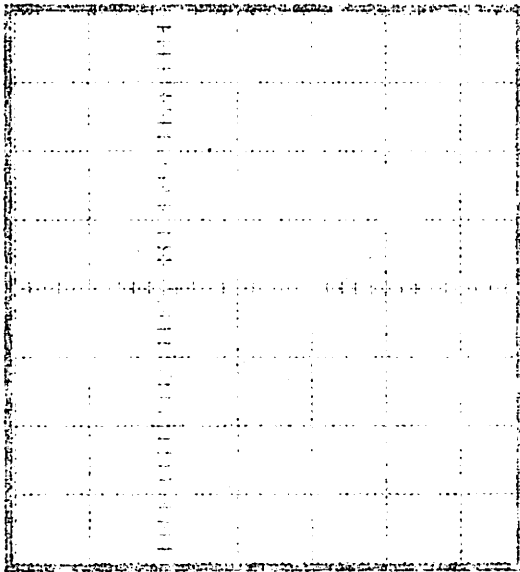
$$= 2 \times 1 \text{ ns} = 2 \text{ ns}$$

Dari hasil perhitungan diatas maka dapat diambil kesimpulan bahwa

hasil perhitungan waktu adalah sama dengan data yang sebenarnya

50. Tombol = PROG

Data = 1000100 1000



V/div = 2 V
t/div = 1 ns

Gambar 4.2 Hasil pengujian tombol

PROG

Tabel 4-1 Hasil perbandingan pengujian data asli Remote Sony RM-827S

TOMBOL	COMMAND		ADDRESS	
	lsb....msb	Data asli	Lsb....msb	Data asli
	Biner	Heksa	Biner	Desimal
MUTE	0010100	14	10000	1
POWER	1010100	54	10000	1
DISPLAY	0101110	2E	10000	1
1	0000000	0	10000	1
2	1000000	40	10000	1
3	0100000	20	10000	1
4	1100000	60	10000	1
5	0010000	10	10000	1
6	1010000	50	10000	1
7	0110000	30	10000	1
8	1110000	70	10000	1
9	0001000	8	10000	1
1-	0011000	30	10000	1
0	1001000	48	10000	1
2-	1011000	58	10000	1
SLEEP	0110110	36	10000	1
+	0010111	17	10000	1
-	1010111	57	10000	1
A/B	1110100	74	10000	1
SELECT	0011111	1F	10000	1

PIC MODE	0110100	34	10000	1
VOL +	0100100	24	10000	1
VOL -	1100100	64	10000	1
TV/VIDEO	1010010	52	10000	1
PROG +	0000100	4	10000	1
PROG -	1000100	44	10000	1

4.2 Pengukuran Lampu

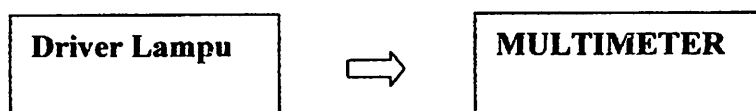
4.2.1 Tujuan

Untuk mengetahui apakah rangkaian driver lampu dapat bekerja dengan baik sesuai perencanaan.

4.2.2 Peralatan yang digunakan

1. Rangkaian Driver Lampu.
2. Digital Multimeter.
3. Catu Daya 5 V.

Langkah Pengukuran



Gambar 4.3.3 Pengukuran Driver Lampu

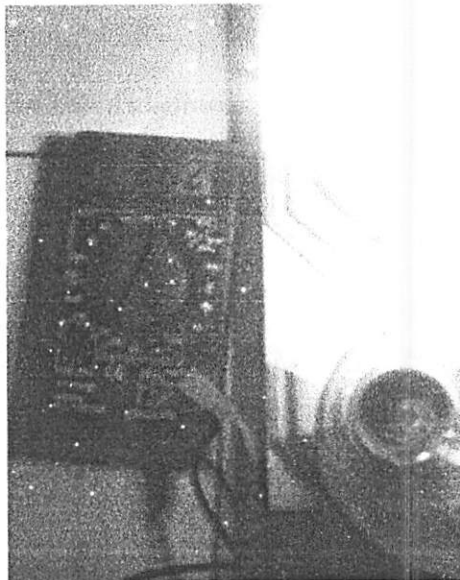
1. Menghubungkan multimeter
2. Menjalankan alat dan menunggu sampai lampu nyala.
3. Mengamati dan mencatat hasil pengukuran pada multimeter pada waktu, lampu mati maupun nyala.

Tabel 4-24 Hasil pengukuran tegangan pada Lampu

KONDISI	BESAR V
Lampu mati	0 V
Lampu Nyala	2.02 V



Gambar 4.3.8 Tampilan Lampu Pada Saat Kondisi Mati



Gambar 4.3.8 Tampilan Lampu Pada Saat Kondisi Hidup

Dari data hasil pengukuran diatas terdapat selisih nilai dari perhitungan yang sebenarnya, sehingga dicari nilai kesalahan dari rangkaian tersebut sebagai berikut

$$\begin{aligned}
 \text{Tabel : Nilai Rugi} &= \left| \frac{\text{Perhitungan} - \text{Pengukuran}}{\text{Perhitungan}} \right| \times 100\% \\
 &= \left| \frac{220V - 20,2V}{220V} \times 100\% \right| \\
 &= \left| \frac{15V}{220V} \times 100\% \right| \\
 &= 0,98\%
 \end{aligned}$$

4.3 Pengukuran Motor DC

4.3.1 Tujuan

Untuk mengetahui apakah rangkaian driver Motor DC dapat bekerja dengan baik sesuai perencanaan.

4.3.2 Peralatan yang digunakan

- 1.Rangkaian Driver Lampu.
- 2.Digital Multimeter.
- 3.Catu Daya 5 V.



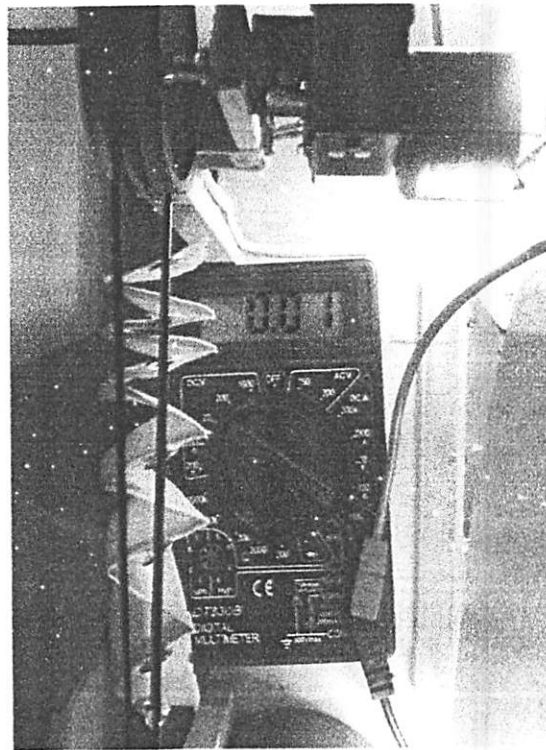
Gambar 4.3.8 Pengukuran driver motor DC

1. Menghubungkan multimeter (skala pada DC) seperti pada gambar 4.38
2. Menjalankan alat dan menunggu sampai motor DC berputar
3. Mengamati dan mencatat hasil pengukuran pada multimeter saat motor DC berputar maupun diam.

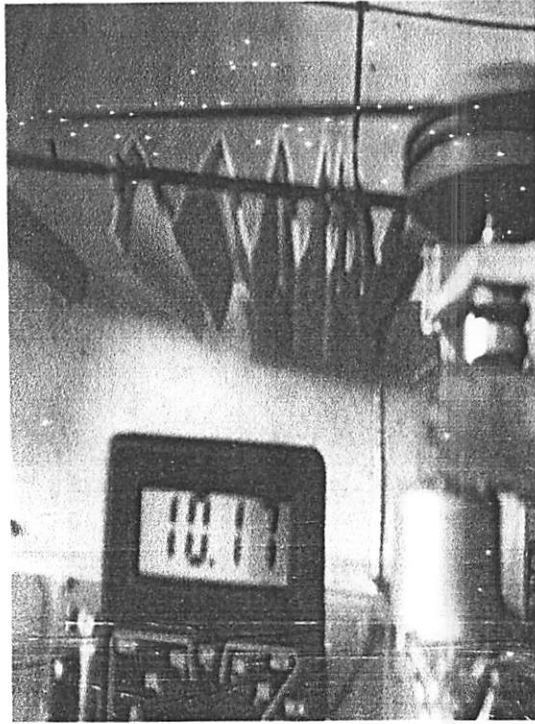
4.5.4 Hasil Pengukuran

Tabel 4-2.6 Hasil pengukuran Tegangan pada Motor DC

KONDISI	BESAR V
Motor mati	0 V
Motor jalan	10.17 V



Gambar 4.3.9 Pengujian Motor Pada Saat Kondisi Mati



Gambar 4.3.10 Pengujian Motor Pada Saat Kondisi Hidup

Dari data hasil pengukuran diatas terdapat selisih nilai dari perhitungan yang sebenarnya, sehingga dicari nilai kesalahan dari rangkaian tersebut sebagai berikut

$$\begin{aligned} \text{Nilai rugi} &= \left| \frac{\text{Perhitungan} - \text{Pengukuran}}{\text{Perhitungan}} \right| \times 100\% \\ &= \left| \frac{10,25V - 10.17V}{10,25V} \times 100\% \right| \\ &= \left| \frac{0.08V}{10,25V} \times 100\% \right| \\ &= 0,78\% \end{aligned}$$

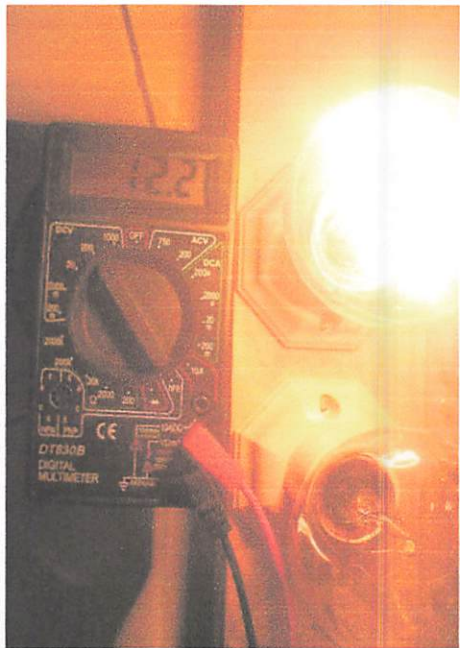
4.2.3 Hasil pengukuran

Tabel 4-3 Hasil pengukuran tegangan pada relay driver Lampu

KONDISI	BESAR V
Lampu mati	0 V
Lampu Nyala	12,2 V



Gambar 4.3.6 Tampilan Lampu Pada Saat Kondisi Mati



Gambar 4.3.7 Tampilan Lampu Pada Saat Kondisi Hidup

Tabel 4-24 Hasil pengukuran tegangan pada Lampu

KONDISI	BESAR V
Lampu mati	0 V
Lampu Nyala	2.02 V



Gambar 4.3.8 Tampilan Lampu Pada Saat Kondisi Mati



Gambar 4.3.8 Tampilan Lampu Pada Saat Kondisi Hidup

Dari data hasil pengukuran diatas terdapat selisih nilai dari perhitungan yang sebenarnya, sehingga dicari nilai kesalahan dari rangkaian tersebut sebagai berikut

$$\begin{aligned}
 \text{Tabel : Nilai Rugi} &= \left| \frac{\text{Perhitungan} - \text{Pengukuran}}{\text{Perhitungan}} \right| \times 100\% \\
 &= \left| \frac{220V - 20,2V}{220V} \times 100\% \right| \\
 &= \left| \frac{15V}{220V} \times 100\% \right| \\
 &= 0,98\%
 \end{aligned}$$

4.3 Pengukuran Motor DC

4.3.1 Tujuan

Untuk mengetahui apakah rangkaian driver Motor DC dapat bekerja dengan baik sesuai perencanaan.

4.3.2 Peralatan yang digunakan

1. Rangkaian Driver Lampu.
2. Digital Multimeter.
3. Catu Daya 5 V.



Gambar 4.3.8 Pengukuran driver motor DC

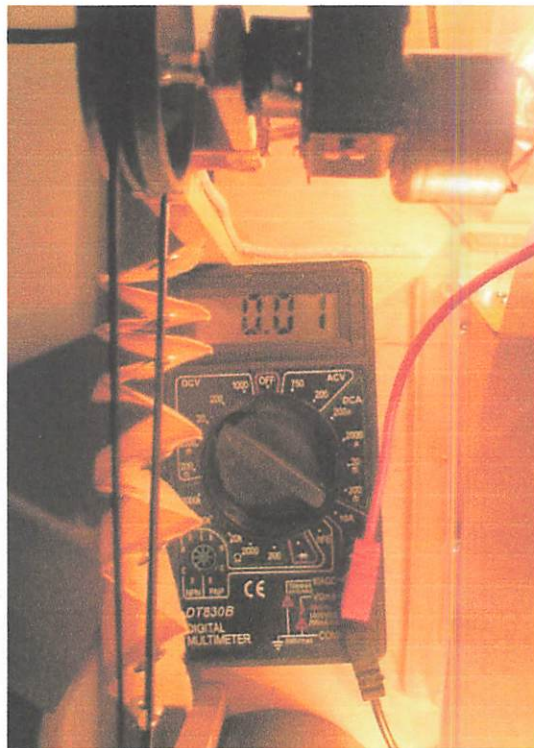
Langkah Pengujian

1. Menghubungkan multimeter (skala pada DC) seperti pada gambar 4.38
2. Menjalankan alat dan menunggu sampai motor DC berputar
3. Mengamati dan mencatat hasil pengukuran pada multimeter saat motor DC berputar maupun diam.

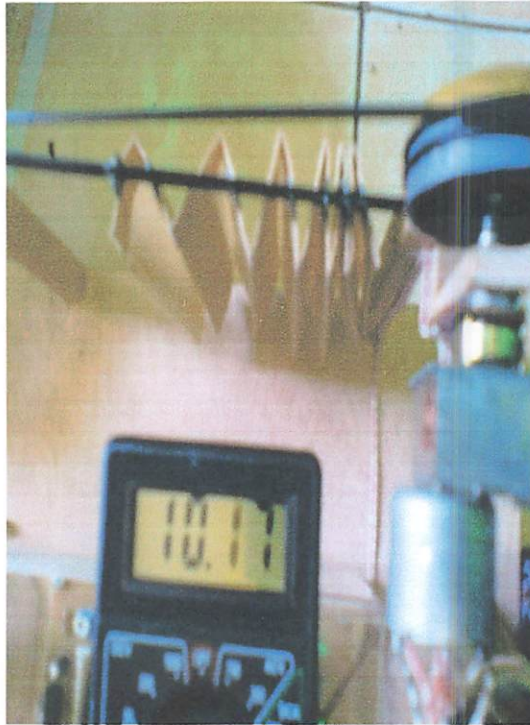
4.5.4 Hasil Pengukuran

Tabel 4-2.6 Hasil pengukuran Tegangan pada Motor DC

KONDISI	BESAR V
Motor mati	0 V
Motor jalan	10.17 V



Gambar 4.3.9 Pengujian Motor Pada Saat Kondisi Mati



Gambar 4.3.10 Pengujian Motor Pada Saat Kondisi Hidup

Dari data hasil pengukuran diatas terdapat selisih nilai dari perhitungan yang sebenarnya, sehingga dicari nilai kesalahan dari rangkaian tersebut sebagai berikut

$$\begin{aligned} \text{Nilai rugi} &= \left| \frac{\text{Perhitungan} - \text{Pengukuran}}{\text{Perhitungan}} \right| \times 100\% \\ &= \left| \frac{10,25V - 10.17V}{10,25V} \times 100\% \right| \\ &= \left| \frac{0.08V}{10,25V} \times 100\% \right| \\ &= 0,78\% \end{aligned}$$

4.4 Pengukuran secara keseluruhan



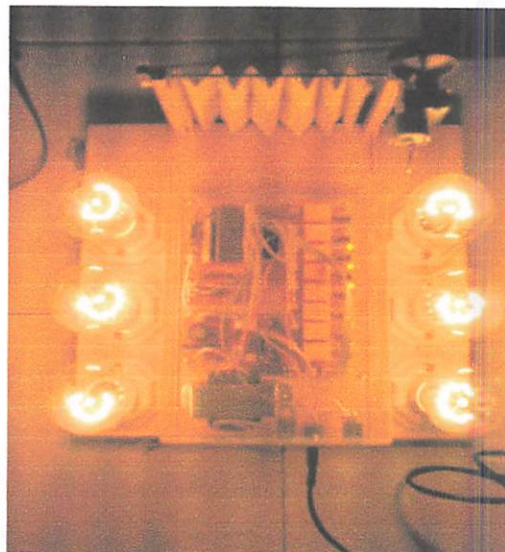
4.4.1 Peralatan yang digunakan

1. *Remote* Sony RM – 827T
2. Seluruh Rangkain dari alat. Terdiri dari rangkaian sensor IRM , Rangkaian mikrokontroler, rangkaian Driver lampu, Rangkaian Driver Motor DC
3. Catu Daya 5 V.
- 4.

4.4.2 Langkah pengujian

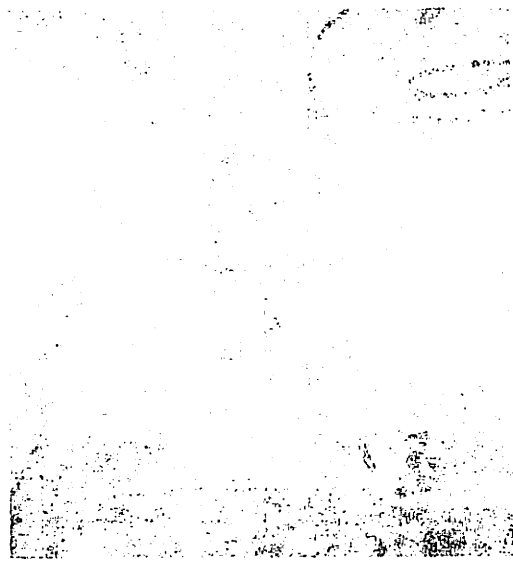
1. Merangkai seluruh rangkaian sesuai dengan perencanaan
2. Memberikan catu daya 5 V pada rangkaian
3. Memberikan sinyal masukan pada sensor dengan *remote*.

Pengujian alat keseluruhan :



Gambar 4.3.11 Tampilan Alat saat semua Lampu menyala

Տարբերակ 4.3.11.11. Ինտելիգենտ զանգի զտման և անոթի անցման



Ինտելիգենտ զանգի կոդավորումը :

- 3) Մասնավորապես զանգի անցման ինտելիգենտ զտման կոդավորումը:
- 5) Մասնավորապես զանգի անցման ինտելիգենտ զտման կոդավորումը:
- 1) Մասնավորապես զանգի անցման ինտելիգենտ զտման կոդավորումը:

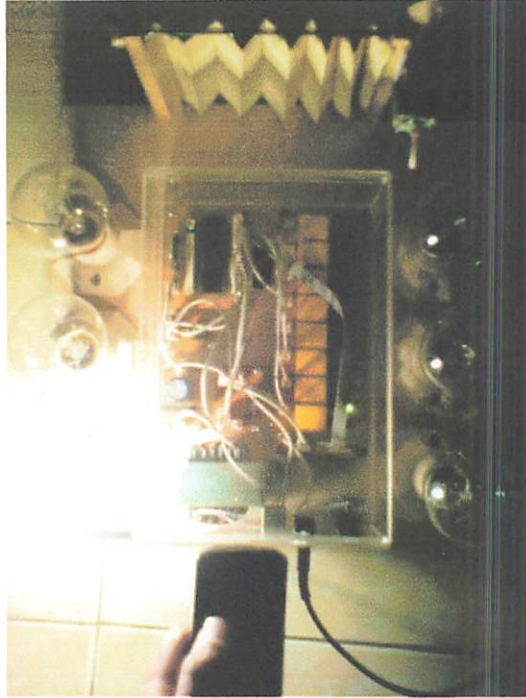
4.3.2 Ինտելիգենտ զանգի կոդավորումը

- 3) Քանի որ զանգի անցման ինտելիգենտ զտման կոդավորումը:
- 5) Քանի որ զանգի անցման ինտելիգենտ զտման կոդավորումը:
- 1) Քանի որ զանգի անցման ինտելիգենտ զտման կոդավորումը:

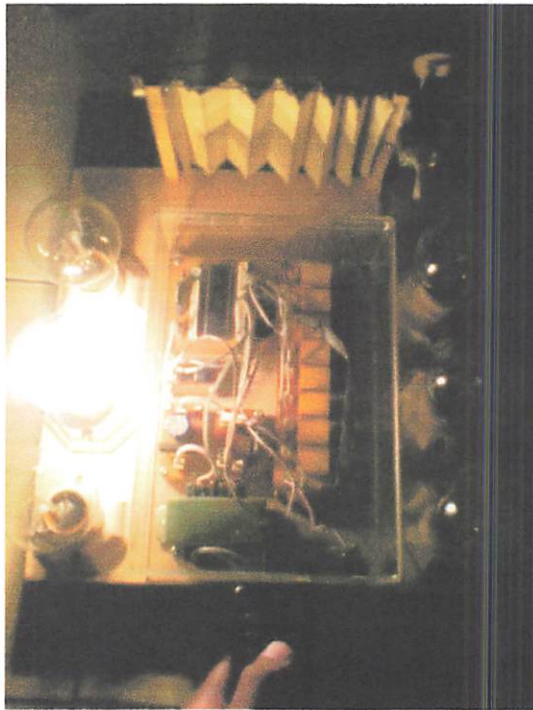
4.3.3 Ինտելիգենտ զանգի կոդավորումը



4.4 Ինտելիգենտ զանգի կոդավորումը



Gambar 4.3.12 Tampilan Alat Pada Saat tombol 1 ditekan dan lampu 1 nyala



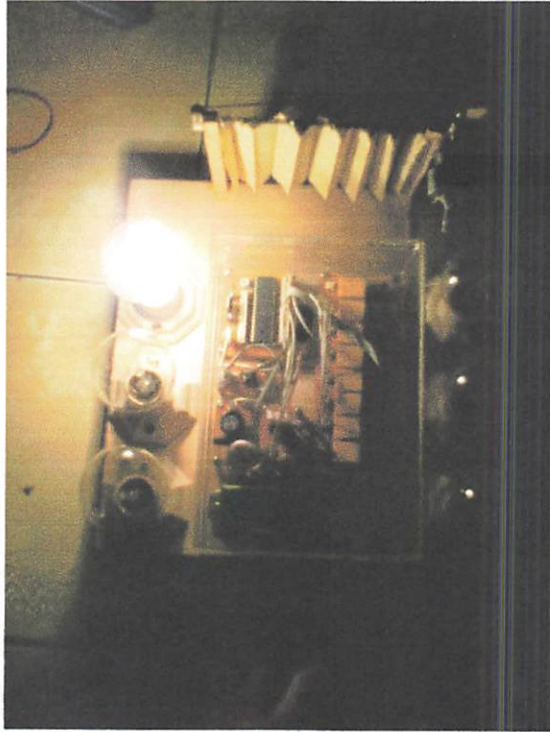
Gambar 4.3.13 Tampilan Alat Pada Saat tombol 2 ditekan dan lampu 2 nyala



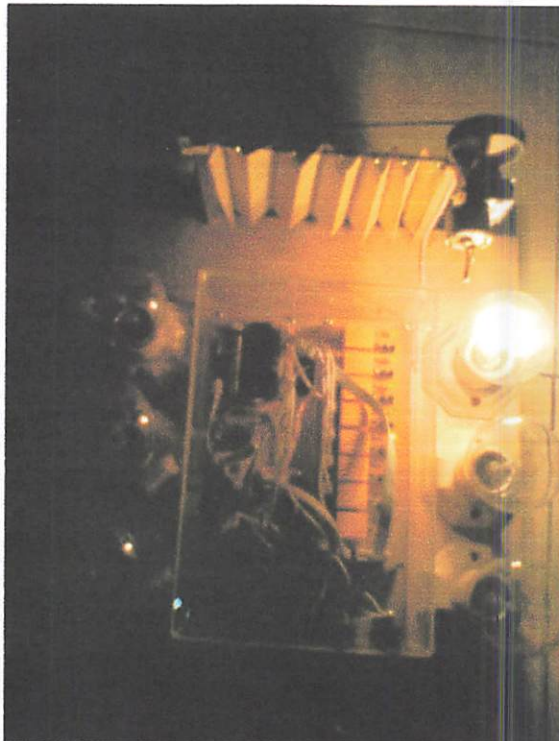
Gambar 4.3.12 Tampilan Alat Pada Saat tombol 1 ditekan dan lampu 1 nyala



Gambar 4.3.13 Tampilan Alat Pada Saat tombol 2 ditekan dan lampu 2 nyala



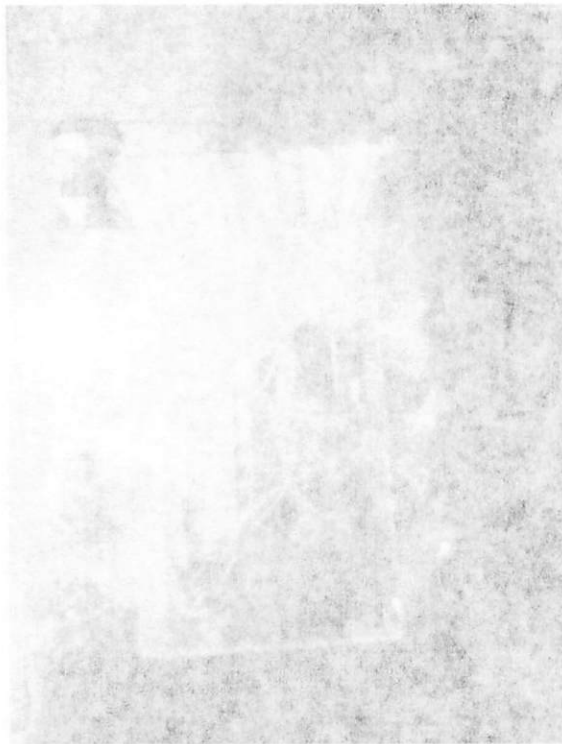
Gambar 4.3.14 Tampilan Alat Pada Saat tombol 3 ditekan dan lampu 3 nyala



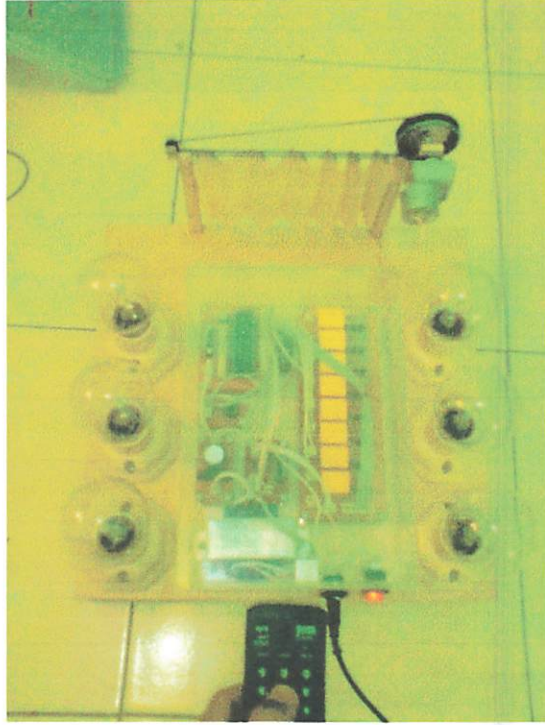
Gambar 4.3.15 Tampilan Alat Pada Saat tombol 4 ditekan dan lampu 4 nyala



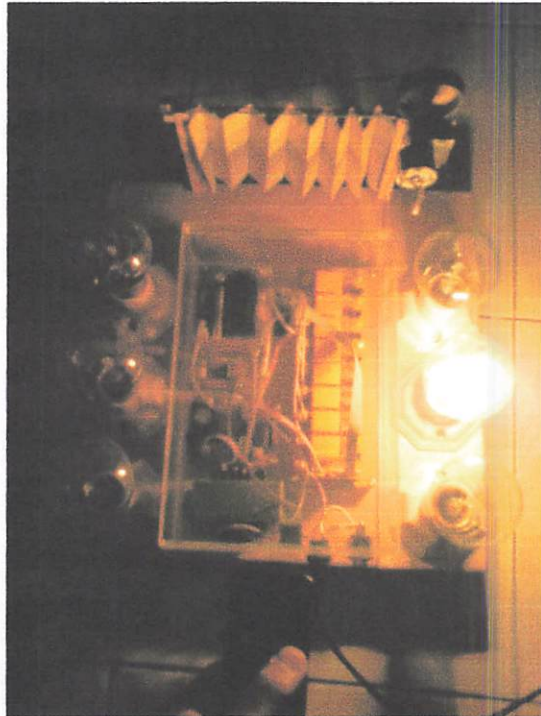
Gambar 4.3.14 Tampilan Alat Pada Saat tombol 3 ditekan dan lampu 3 nyala



Gambar 4.3.15 Tampilan Alat Pada Saat tombol 4 ditekan dan lampu 4 nyala



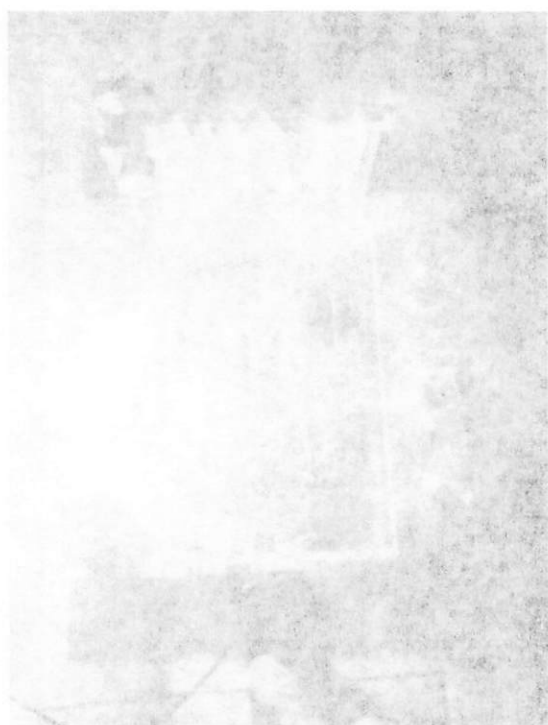
Gambar 4.3.16 Tampilan Alat Pada Saat tombol 5 ditekan dan lampu 4 mati



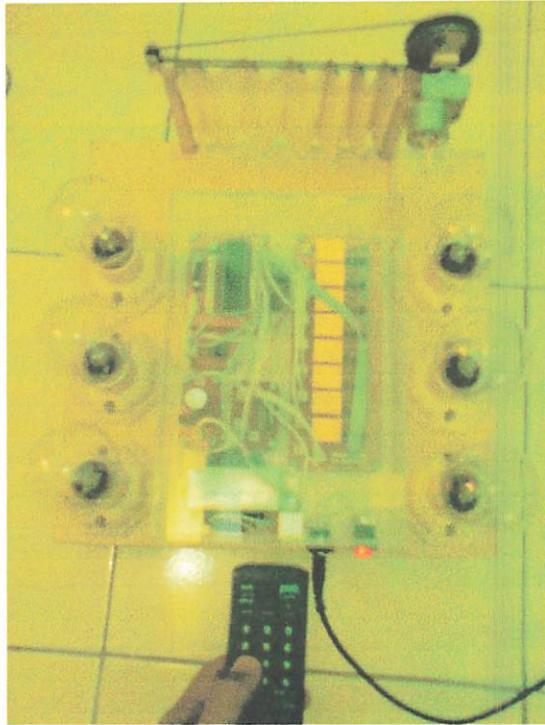
Gambar 4.3.17 Tampilan Alat Pada Saat tombol 6 ditekan dan lampu 5 nyala



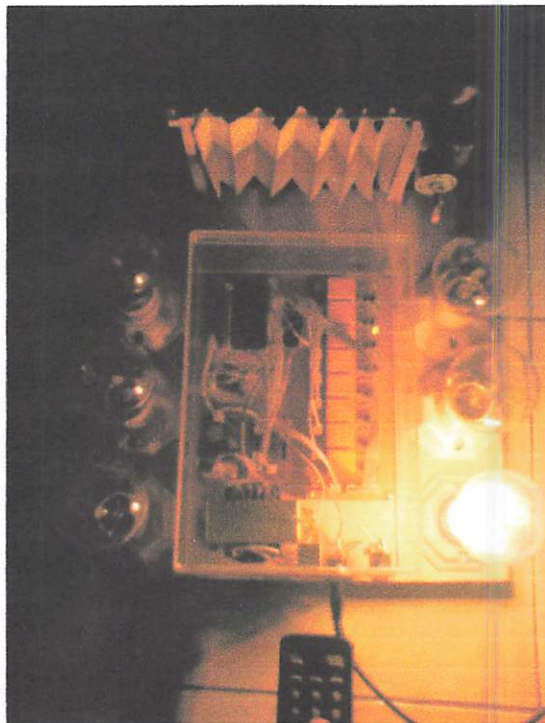
Gambar 4.3.16 Tampilan Alat Pada Saat Tombol 5 ditekan dan lampu 4 mati



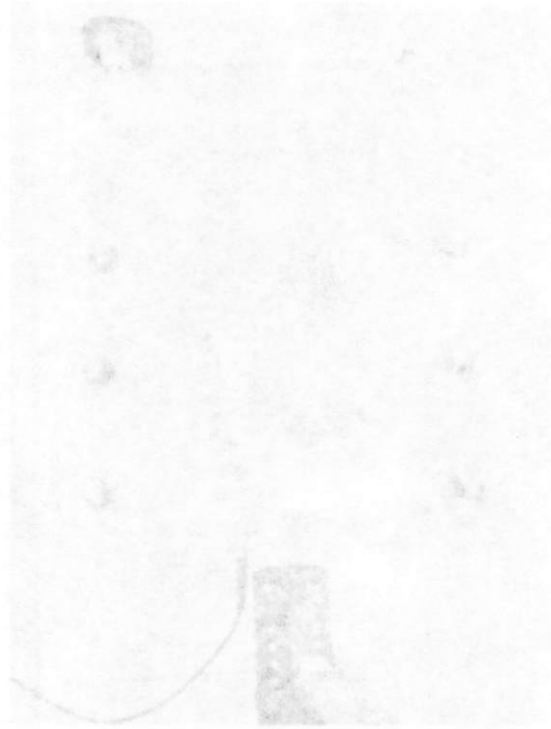
Gambar 4.3.17 Tampilan Alat Pada Saat Tombol 6 ditekan dan lampu 5 nyala



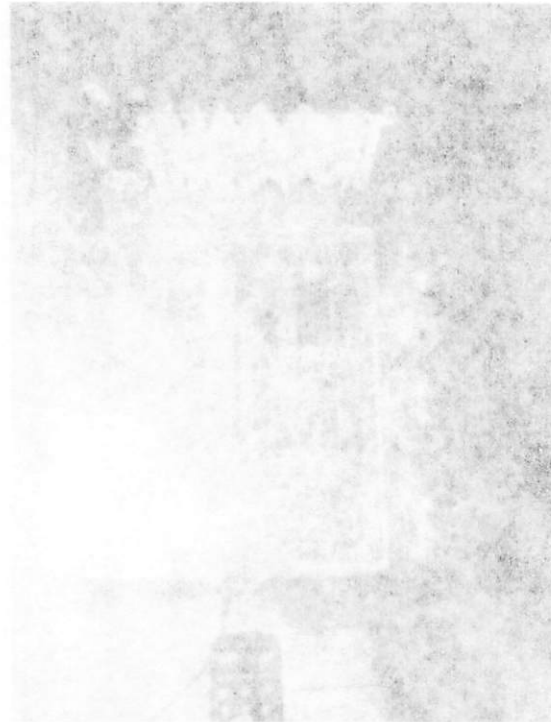
Gambar 4.3.18 Tampilan Alat Pada Saat tombol 7 ditekan dan lampu 5 mati



Gambar 4.3.19 Tampilan Alat Pada Saat tombol 8 ditekan dan lampu 6 nyala



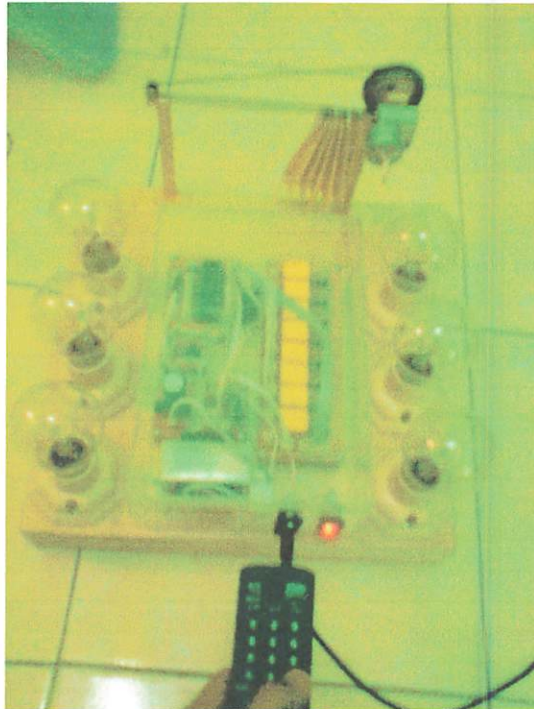
Gambar 4.3.18 Tampilan Alat Pada Saat kontrol 7 ditekkan dan lampu 5 mati



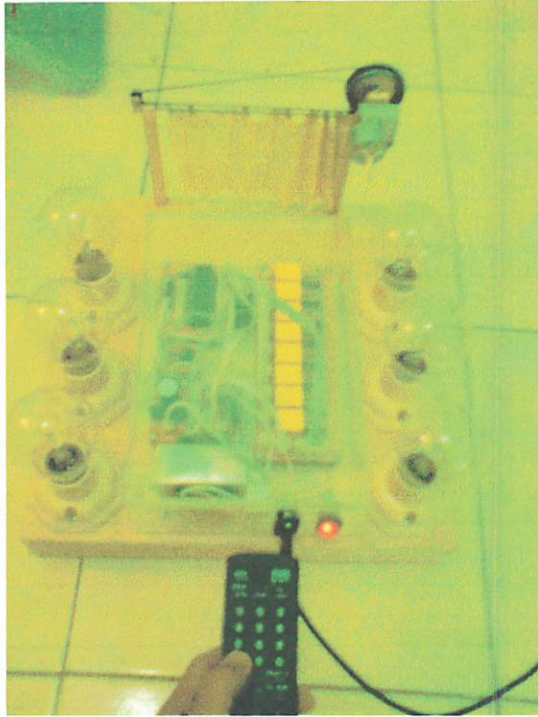
Gambar 4.3.19 Tampilan Alat Pada Saat kontrol 8 ditekkan dan lampu 6 nyala



Gambar 4.3.20 Tampilan Alat Pada Saat tombol 9 ditekan dan lampu 6 mati



Gambar 4.3.21 Tampilan Alat Pada Saat tombol 2- ditekan dan Korden membuka



Gambar 4.3.22 Tampilan Alat Pada Saat tombol 2- ditekan dan Korden menutup

Keterangan untuk masing-masing lampu :

1. lampu no 1 adalah simulasi untuk lampu kamar tidur
2. lampu no 2 adalah simulasi untuk lampu meja
3. lampu no 3 adalah simulasi untuk lampu Ruang Tamu
4. lampu no 4 adalah simulasi untuk Kipas Angin
5. lampu no 5 adalah simulasi untuk Tape
6. lampu no 6 adalah simulasi untuk lemari Es
7. Motor DC adalah simulasi untuk Korden

BAB V

PENUTUP

5.1. Kesimpulan

Dari pembuatan “Alat pengontrol peralatan listrik dan korden” ini maka dapat diambil kesimpulan sebagai berikut:

- 1) Besar tegangan keseluruhan pada saat semua driver lampu menyala yaitu 12,2V dan pada waktu lampu mati sebesar 0V, sedangkan tegangan untuk driver Motor saat motor bergerak sebesar 10,17V dan pada saat motor diam atau tidak ada tegangan sebesar 0V.
- 2) Pada pengukuran saat remote ditekan keluaran dari sensor adalah data yang diwakili oleh pulsa dimana T/Div nya = 1 ms dan V/div nya = 5 V
- 3) Dari semua pengujian dan pengukuran didapatkan error untuk tegangan pada driver relay sebesar 0,98% sedangkan untuk driver motor sebesar 0,78 %

5.2 Saran

1. Penggunaan *remote* sebaiknya bukan menggunakan *remote* merk Sony saja tetapi dicoba dengan menggunakan *remote* Televisi selain *Sony*
2. Agar dapat digunakan pada beban yang lebih besar disarankan untuk mengganti *Relay* dan dioda pada detektor arus yang mampu mengalirkan arus yang lebih besar.

Daftar Pustaka

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- [12] www.ElectronicTransistor.com



LAMPIRAN

LAMPYRAN



INSTITUT TEKNOLOGI NASIONAL
FAKULTAS TEKNOLOGI INDUSTRI
JURUSAN TEKNIK ELEKTRO S-1
KONSENTRASI TEKNIK ELEKTRONIKA

**BERITA ACARA UJIAN SKRIPSI
FAKULTAS TEKNOLOGI INDUSTRI**

Nama : Heri Suwandono
NIM : 04.12.224
Jurusan : Teknik Elektro S-1
Konsentrasi : Teknik Elektronika
Judul Skripsi : Alat Pengendali ON/OFF Peralatan Listrik Dan Korden Pada Rumah Tangga Menggunakan Remote Infra Merah Sony Berbasis Mikrokontroler AT89S52

Dipertahankan di hadapan majelis penguji Skripsi jenjang Strata satu (S-1) pada :

Hari : Selasa
Tanggal : 29 September 2009
Dengan Nilai : 73 (B+) *Bej*


Ketua Majelis Penguji

(Ir. Sidik Noertjahjono, MT)
NIP.Y.1028700163

Sekretaris Majelis Penguji



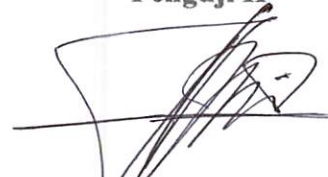
(Ir. F. Yudi Limpraptono, MT)
NIP.Y.1039500274

Penguji I



(Ir. Eko Nurcahyo)
NIP. Y. 1028700172

Penguji II

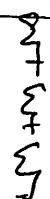


(Sotyo Hadi, ST, Msc)
NIP. Y.1039700309

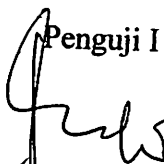


FORMULIR PERBAIKAN SKRIPSI

Nama : Heri Suwandono
 NIM : 04.12.224
 Jurusan : Teknik Elektro S-1
 Konsentrasi : Teknik Elektronika
 Judul : Alat Pengendali ON/OFF Peralatan Listrik Dan Korden Pada Rumah Tangga Menggunakan Remote Infra Merah Sony Berbasis Mikrokontroler AT89S52
 Hari / Tanggal Ujian Skripsi : Selasa / 29 September 2009

Penguji	Revisi	Paraf
Penguji I	<ul style="list-style-type: none"> - Perubahan kata "Pengontrol" menjadi "Pengendali" dan tambahan kata "ON/OFF pada judul. - Penambahan Tombol untuk kondisi ON semua dan OFF semua - Pengujian kepekaan dari Remote SONY 	

Disetujui,

Penguji I



(Ir. Eko Nurcahyo)
 NIP. Y. 1028700172

Mengetahui,

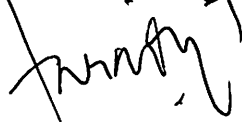
Penguji II


(Sotyo Hadi, ST, Msc)
 NIP. Y. 1039700309

Mengetahui,

Dosen Pembimbing I


(Ir. TH. Mimien Mustikawati, MT)
 NIP. Y. 1030000352

Dosen Pembimbing II


(Irmalia Suryani Faradisa, ST, MT.)
 NIP. P. 1030000365

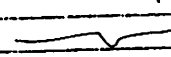


INSTITUT TEKNOLOGI NASIONAL MALANG
 FAKULTAS TEKNOLOGI INDUSTRI
 JURUSAN TEKNIK ELEKTRO

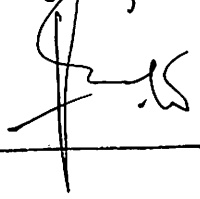
Formulir Perbaikan Ujian Skripsi

Dalam pelaksanaan Ujian Skripsi Janjang Strata 1 Jurusan Teknik Elektro Konsentrasi T. Energi Listrik / T. Elektronika / T. Infokom, maka perlu adanya perbaikan skripsi untuk mahasiswa .

NAMA : HZK S.
 NIM : 2412224
 Perbaikan meliputi :

- Tambahan oke tombol (kontrol) lampu mati semua
- (2)  hidup semua.
- Pengujian kepekaan dr remote.

Malang, 29-9-2009





FORMULIR BIMBINGAN SKRIPSI

Nama : HERI SUWANDONO
Nim : 04.12.224
Masa Bimbingan : 29 MEI 2009 s/d 29 NOVEMBER 2009
Judul Skripsi : ALAT PENGONTROL PERALATAN LISTRIK DAN KORDEN DI
DALAM RUMAH MENGGUNAKAN REMOTE INFRA MERAH SONY
BERBASIS MIKROKONTROLLER AT89S52

NO	Tanggal	Uraian	Paraf Pembimbing
1	3 - 6 - 2009	Bab I + II revisi	
2	7 - 6 - 2009	Bab I + II OK	
3	10 - 8 - 2009	Bab III + IV revisi	
4	10 - 8 - 2009	Bab III OK	
5	10 - 8 - 2009	Bab IV OK	
6	10 - 8 - 2009	Acc Seminar Hasil	
7	28 - 9 - 2009	Bab V revisi	
8	28 - 9 - 2009	Bab V OK	
9	28 - 9 - 2009	kumpre	
10			

Malang,
Dosen Pembimbing I

Ir. Mimien Mustikawati, MT
NIP. 1030000352



FORMULIR BIMBINGAN SKRIPSI

Nama : HERI SUWANDONO
Nim : 04.12.224
Masa Bimbingan : 29 MEI 2009 s/d 29 NOVEMBER 2009
Judul Skripsi : ALAT PENGONTROL PERALATAN LISTRIK DAN KORDEN DI DALAM RUMAH MENGGUNAKAN REMOTE INFRA MERAH SONY BERBASIS MIKROKONTROLLER AT89S52

NO	Tanggal	Uraian	Paraf Pembimbing
1	21/8 09	BAB I . Revisi Rumusan, Tujuan, & Btsa. Mslh.	
2		BAB II tambahkan . FRM-SSIC, L293 & active	
3		BAB III perencanaan diperbaiki	
4	31/8 09	Revisi BAB I. II, III perencanaan tata tulis TR, TR,	
5	1/9 09	Revisi perencanaan	
6	7-09-2009	ACC semua bab	
7	7-09-2009	Seminar hasil	
8	28-09-2009	Siap kompre	
9			
10			

Malang,
Dosen Pembimbing II

Irmalia Suryani Faradisa
Irmalia Suryani Faradisa, ST MT
NIP.1030100365



PERKUMPULAN PENGELOLA PENDIDIKAN UMUM DAN TEKNOLOGI NASIONAL MALANG
INSTITUT TEKNOLOGI NASIONAL MALANG

FAKULTAS TEKNOLOGI INDUSTRI
FAKULTAS TEKNIK SIPIL DAN PERENCANAAN
PROGRAM PASCASARJANA MAGISTER TEKNIK

PT. BNI (PERSERO) MALANG
BANK NIAGA MALANG

Kampus I : Jl. Bendungan Sigura-gura No. 2 Telp. (0341) 551431 (Hunting), Fax. (0341) 553015 Malang 65145
Kampus II : Jl. Raya Karanglo, Km 2 Telp. (0341) 417636 Fax. (0341) 417634 Malang

Malang, 4 Juni 2009

Nomor : ITN- 929/7/TA /2009
Lampiran :
Perihal : Bimbingan Skripsi

Kepada : Yth. Sdr. **IRMALIA SURYANI FARADISA, ST, MT**
Dosen Pembimbing
Jurusan Teknik Elektro S-1
di
Malang

Dengan hormat,
Sesuai dengan permohonan dan persetujuan dalam proposal skripsi
untuk mahasiswa:

Nama : **HERI SUWANDONO**
Nim : **04 12 224**
Fakultas : **Teknologi Industri**
Jurusan : **Teknik Elektro S-1**
Konsentrasi : **Teknik Elektronika**

Maka dengan ini pembimbingan tersebut kami serahkan sepenuhnya
kepada Saudara/i selama masa waktu 6 (enam) bulan. terhitung mulai
tanggal:

29 MEI 2009 s/d 29 NOVEMBER 2009

Sebagai satu syarat untuk menempuh Ujian sarjana.
Demikian atas perhatian serta kerjasama yang baik kami ucapkan
terima kasih



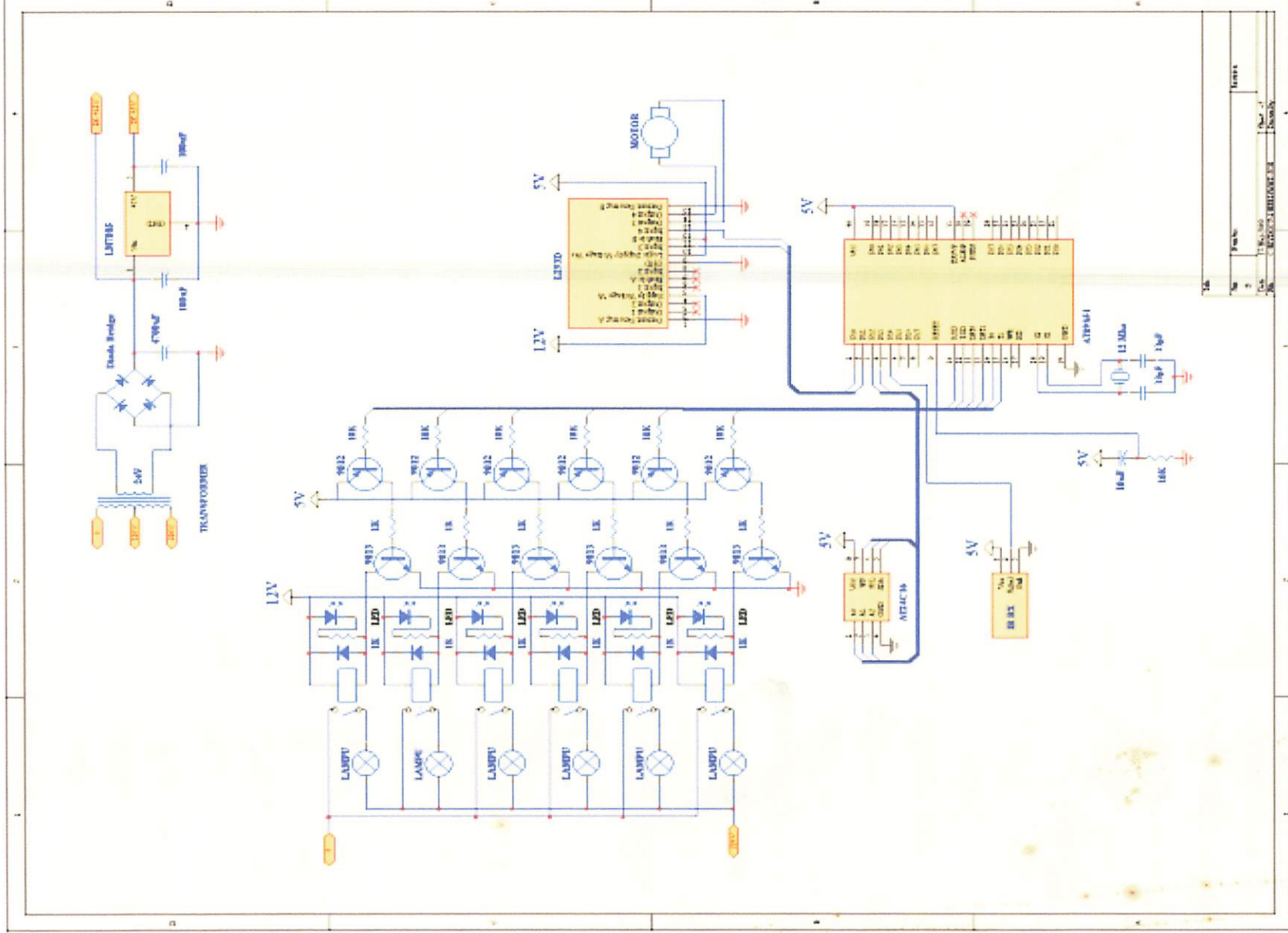
Ketua Jurusan
Teknik Elektro S-1

Ir. F. Yudi Limpraptono, MT
NIP. Y. 1039500274

Tindakan:

1. Mahasiswa yang Bersangkutan
2. Arsip

Form S-4a



No	Part	Quantity	Remarks
1	AT89C51	1	Microcontroller
2	LM7805	1	5V Regulator
3	7805	1	5V Regulator
4	9813	6	LEDs
5	LAMP	6	Lamps
6	1K	12	Resistors
7	10K	1	Resistor
8	10µF	2	Capacitors
9	100µF	1	Capacitor
10	4V Zener	1	Zener Diode
11	Transformer	1	Power Transformer
12	Motor	1	DC Motor

```

; remote type RM-827T TRINITRON
;
;      org      00h
;
Mtr0   Bit P1.0
Mtr1   Bit P1.1
ISCL   Bit P1.2           ; i2C clock
ISDA   Bit P1.3           ; I2C data
IRRX   Bit P1.4           ; infrared receiver
Rest   Bit P2.6           ; RS LCD
Enbl   Bit P2.7           ; E LCD
Rly0   Bit P3.0
Rly1   Bit P3.1
Rly2   Bit P3.2
Rly3   Bit P3.3
Rly4   Bit P3.4
Rly5   Bit P3.5

Dtrm   Equ 30h
Dtr0   Equ 31h
Dtr1   Equ 32h
Dtr2   Equ 33h
Dtr3   Equ 34h
Dtr4   Equ 35h
Dtr5   Equ 36h
Dtr6   Equ 37h
Dtr7   Equ 38h

Dlp0   Equ 40h
Dlp1   Equ 41h
Dlp2   Equ 42h
Dlp3   Equ 43h
Dlp4   Equ 44h
Dlp5   Equ 45h

Dlmp   Equ 50h
Char   Equ 51h
Dly0   Equ 52h
Dly1   Equ 53h
Dly2   Equ 54h
;
init:   lcall   lcd_in
        lcall   tmr_in
        lcall   rd_mem
        lcall   drvhdw
        ljmp    action
;
mulai:  mov     DPTR,#nama
        lcall   line1
        mov     Char,#16
        lcall   tulis
        mov     DPTR,#nim
        lcall   line2
        mov     Char,#16
        lcall   tulis
        lcall   delay2
        mov     DPTR,#jur
        lcall   line1
        mov     Char,#16
        lcall   tulis
        mov     DPTR,#univ
        lcall   line2
        mov     Char,#16
        lcall   tulis
        lcall   delay2
;

```

```

        lcall    lcdclr
        mov     DPTR,#tpdtrm
        lcall    line1
        mov     Char,#16
        lcall    tulis
        mov     DPTR,#angka
action: lcall    bc_rmt
        mov     P0,#06Dh
        lcall    w_ins
        mov     A,R0
        lcall    nilai
;
actn00: cjne    R0,#000,actn02
        jnb     Rly0,actn01
        clr     Rly0
        mov     Dlp0,#1
        ljmp    actn16
actn01: jb      Rly0,actn02
        setb    Rly0
        mov     Dlp0,#0
        ljmp    actn16
;
actn02: cjne    R0,#001,actn04
        jnb     Rly1,actn03
        clr     Rly1
        mov     Dlp1,#1
        ljmp    actn16
actn03: jb      Rly1,actn04
        setb    Rly1
        mov     Dlp1,#0
        ljmp    actn16
;
actn04: cjne    R0,#002,actn06
        jnb     Rly2,actn05
        clr     Rly2
        mov     Dlp2,#1
        ljmp    actn16
actn05: jb      Rly2,actn06
        setb    Rly2
        mov     Dlp2,#0
        ljmp    actn16
;
actn06: cjne    R0,#003,actn08
        jnb     Rly3,actn07
        clr     Rly3
        mov     Dlp3,#1
        ljmp    actn16
actn07: jb      Rly3,actn08
        setb    Rly3
        mov     Dlp3,#0
        ljmp    actn16
;
actn08: cjne    R0,#004,actn10
        jnb     Rly4,actn09
        clr     Rly4
        mov     Dlp4,#1
        ljmp    actn16
actn09: jb      Rly4,actn10
        setb    Rly4
        mov     Dlp4,#0
        ljmp    actn16
;
actn10: cjne    R0,#005,actn12
        jnb     Rly5,actn11
        clr     Rly5
        mov     Dlp5,#1

```

```

        ljmp      actn16
actn11: jb       Rly5,actn12
        setb     Rly5
        mov      Dlp5,#0
        ljmp     actn16
;
actn12: cjne    R0,#012,actn14
        clr     Mtr0
        setb    Mtr1
        lcall   delay2
        setb    Mtr0
        setb    Mtr1
        ljmp    actn16
;
actn14: cjne    R0,#013,actn16
        setb    Mtr0
        clr     Mtr1
        lcall   delay2
        setb    Mtr0
        setb    Mtr1
        ljmp    actn16
;
actn16: lcall   delay1
        lcall   wr_mem
        mov     SP,#07h
        ljmp    action
;
drvhdw: mov     A,Dlp0
        cjne    A,#0,drhd00
        setb    Rly0
drhd00: cjne    A,#1,drhd01
        clr     Rly0
;
drhd01: mov     A,Dlp1
        cjne    A,#0,drhd02
        setb    Rly1
drhd02: cjne    A,#1,drhd03
        clr     Rly1
;
drhd03: mov     A,Dlp2
        cjne    A,#0,drhd04
        setb    Rly2
drhd04: cjne    A,#1,drhd05
        clr     Rly2
;
drhd05: mov     A,Dlp3
        cjne    A,#0,drhd06
        setb    Rly3
drhd06: cjne    A,#1,drhd07
        clr     Rly3
;
drhd07: mov     A,Dlp4
        cjne    A,#0,drhd08
        setb    Rly4
drhd08: cjne    A,#1,drhd09
        clr     Rly4
;
drhd09: mov     A,Dlp5
        cjne    A,#0,drhd10
        setb    Rly5
drhd10: cjne    A,#1,drhd11
        clr     Rly5
;
drhd11: ret
;
bc_rmt: lcall   bcstrm          ; baca start remote

```

```

lcall bcbtrm ;\
mov Dtr0,A ; |
lcall bcbtrm ; |
mov Dtr1,A ; |
lcall bcbtrm ; |
mov Dtr2,A ; |
lcall bcbtrm ; |
mov Dtr3,A ; |
lcall bcbtrm ; | baca bit remote
mov Dtr4,A ; |
lcall bcbtrm ; |
mov Dtr5,A ; |
lcall bcbtrm ; |
mov Dtr6,A ; |
lcall bcbtrm ; |
mov Dtr7,#0 ; |
lcall bcbtrm ;/

```

;

```

mov R0,#0 ;\
mov A,Dtr0 ; |
lcall ckbtrm ; |
mov A,R0 ; |
RRC A ; |
mov R0,A ; |
mov A,Dtr1 ; |
lcall ckbtrm ; |
mov A,R0 ; |
RRC A ; |
mov R0,A ; |
mov A,Dtr2 ; |
lcall ckbtrm ; |
mov A,R0 ; |
RRC A ; |
mov R0,A ; |
mov A,Dtr3 ; |
lcall ckbtrm ; |
mov A,R0 ; |
RRC A ; |
mov R0,A ; | kalibrasi data remote
mov A,Dtr4 ; | ke data binary
lcall ckbtrm ; |
mov A,R0 ; |
RRC A ; |
mov R0,A ; |
mov A,Dtr5 ; |
lcall ckbtrm ; |
mov A,R0 ; |
RRC A ; |
mov R0,A ; |
mov A,Dtr6 ; |
lcall ckbtrm ; |
mov A,R0 ; |
RRC A ; |
mov R0,A ; |
mov A,Dtr7 ; |
lcall ckbtrm ; |
mov A,R0 ; |
RRC A ; |
mov R0,A ; |
ret ;/

```

;

```

ckbtrm: cjne A,#0,cbtrm0 ;\
clr C ; |
ljmp cbtrm5 ; |
cbtrm0: cjne A,#1,cbtrm1 ; |
clr C ; |

```

```

cbtrm1: ljmp    cbtrm5                ; |
        cjne   A,#2,cbtrm2          ; |
        clr    C                    ; |
        ljmp   cbtrm5                ; | remap data
cbtrm2: cjne   A,#3,cbtrm3          ; | remote
        setb   C                    ; |
        ljmp   cbtrm5                ; |
cbtrm3: cjne   A,#4,cbtrm4          ; |
        setb   C                    ; |
        ljmp   cbtrm5                ; |
cbtrm4: cjne   A,#5,cbtrm5          ; |
        setb   C                    ; |
cbtrm5: ret                          ; /
;
bcstrm: mov    TL0,#00              ; \
        mov    TH0,#00              ; |
        jb     IRRX,$               ; |
        setb   TRO                  ; |
        jnb    IRRX,$               ; |
        clr    TRO                  ; | baca start remote
        mov    A,TH0                ; |
        mov    B,#8                 ; |
        div    AB                    ; |
        jz     bcstrm               ; |
        ret                          ; /
;
cbctrm: mov    TL0,#00              ; \
        mov    TH0,#00              ; |
        jb     IRRX,$               ; |
        setb   TRO                  ; | baca bit
        jnb    IRRX,$               ; | remote
        clr    TRO                  ; |
        mov    A,TH0                ; |
        ret                          ; /
;
wr_mem: mov    A,#10100000b         ; AT24C16 write address
        lcall  adrtx                 ; address memory
        mov    A,#00                 ; data memory
        lcall  dtatx                 ; data memory
        mov    A,Dlp0                 ; data memory
        lcall  dtatx                 ; data memory
        mov    A,Dlp1                 ; data memory
        lcall  dtatx                 ; data memory
        mov    A,Dlp2                 ; data memory
        lcall  dtatx                 ; data memory
        mov    A,Dlp3                 ; data memory
        lcall  dtatx                 ; data memory
        mov    A,Dlp4                 ; data memory
        lcall  dtatx                 ; data memory
        mov    A,Dlp5                 ; data memory
        lcall  dtatx                 ; data memory
        lcall  i2cstp                ; i2c stop
        ret
;
rd_mem: mov    A,#10100000b         ; AT24C16 write address
        lcall  adrtx                 ; address memory
        mov    A,#00                 ; data memory
        lcall  dtatx                 ; data memory
        mov    A,#10100001b         ; AT24C16 read address
        lcall  adrtx                 ; terima data
        lcall  dtarx                 ; terima data
        mov    Dlp0,A                ; simpan data
        lcall  givack                ; send ack
        lcall  dtarx                 ; terima data
        mov    Dlp1,A                ; simpan data
        lcall  givack                ; send ack

```



```

        lcall    dtarx                ; terima data
        mov     Dlp2,A                ; simpan data
        lcall    givack               ; send ack
        lcall    dtarx                ; terima data
        mov     Dlp3,A                ; simpan data
        lcall    givack               ; send ack
        lcall    dtarx                ; terima data
        mov     Dlp4,A                ; simpan data
        lcall    givack               ; send ack
        lcall    dtarx                ; terima data
        mov     Dlp5,A                ; simpan data
        lcall    givack               ; send ack
        lcall    i2cstp               ; i2c stop
        ret

;
adrtx:  lcall    i2cstr               ; i2c start
        lcall    putbit              ; kirim data
        ret

;
dtatx:  lcall    putbit              ; kirim data
        ret

;
dtarx:  lcall    getbit              ; terima data
        ret

;
putbit: mov     R6,#8
putbt:  RLC     A
        mov     ISDA,C
        setb   ISCL
        clr    ISCL
        djnz   R6,putbt
        setb   ISDA
        lcall  getack
        ret

;
getbit: mov     R6,#8
getbt:  setb   ISCL
        mov     C,ISDA
        RLC    A
        clr    ISCL
        djnz   R6,getbt
        setb   ISDA
        ret

;
getack: setb   ISDA                 ; tunggu ack
        setb   ISCL                 ; \
ackbit: mov     C,ISDA              ; | D=1, C=1
        jc     ackbit                ; | tunggu D=0, C=0
        clr    ISCL                 ; /
        ret

;
givack: clr     ISDA                 ; kirim ack
        setb   ISCL                 ; \
        clr    ISCL                 ; | D=0, C=1, C=0, D=1
        setb   ISDA                 ; /
        ret

;
i2cstr: setb   ISCL                 ; i2c start
        setb   ISDA                 ; \
        clr    ISDA                 ; | C=1, D=1, D=0, C=0
        clr    ISCL                 ; /
        ret

;
i2cstp: clr     ISDA                 ; i2c stop
        setb   ISCL                 ; \ D=0, C=1, D=1, C=0
        setb   ISDA                 ; /

```

```

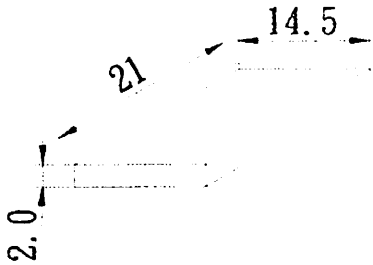
        clr     ISCL
        lcall  delay0
        ret
;
nilai:  mov     B,#100
        div   AB
        lcall  wr_chr
        mov   A,B
        mov   E,#10
        div   AB
        lcall  wr_chr
        mov   A,B
        lcall  wr_chr
        ret
;
line1:  mov     P0,#080h
        lcall  w_ins
        ret
;
line2:  mov     P0,#0C0h
        lcall  w_ins
        ret
;
tulis:  clr     A
        lcall  wr_chr
        inc   DPTR
        djnz  Char,tulis
        ret
;
wr_chr:  movc   A,@A+DPTR
        mov   P0,A
        lcall  w_chr
        ret
;
w_ins:  clr     Enbl
        clr   Rest
        setb  Enbl
        clr   Enbl
        lcall  delay0
        ret
;
w_chr:  clr     Enbl
        setb  Rest
        setb  Enbl
        clr   Enbl
        lcall  delay0
        ret
;
lcd_in: lcall  delay2
        mov   P0,#01h           ; Display Clear
        lcall  w_ins
        mov   P0,#38h         ; Function Set
        lcall  w_ins
        mov   P0,#0Dh         ; Display On, Cursor, Blink
        lcall  w_ins
        mov   P0,#06h         ; Entry Mode
        lcall  w_ins
        mov   P0,#02h         ; Cursor Home
        lcall  w_ins
        ret
;
lcdclr: mov   P0,#01h           ; Display Clear
        lcall  w_ins
        lcall  delay0
        lcall  delay0
        lcall  delay0

```

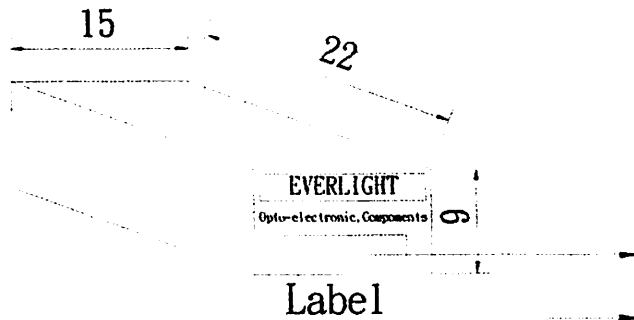
```
        ret
;
tmr_in: lcall  delay2
        mov    TMOD,#11h
        ret
;
delay0: djnz   Dly0,delay0
        ret
;
delay1: lcall  delay0
        djnz   Dly1,delay1
        ret
;
delay2: mov    Dly2,#5
dely2:  lcall  delay1
        djnz   Dly2,dely2
        ret
;
nama:   DB     ' Heri Suwandono '
nim:    DB     ' NIM: 0412224 '
jur:    DB     ' T. Elektro '
univ:   DB     ' ITN Malang '
tpdtrm: DB     'Data Remote: 000'
angka: DB     '0123456789 '
;
        end
```

Packing Specifications

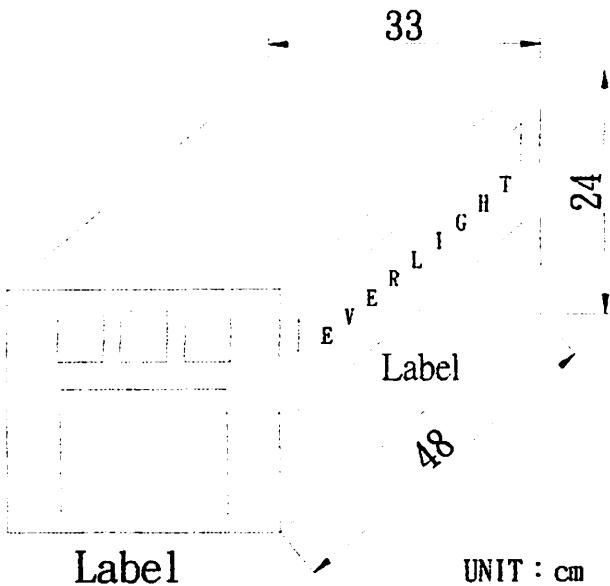
1. Plastic Case



2. Box



3. Carton



UNIT : cm

- CPN : Customer's Production Number
- P/N : Production Number
- QTY : Packing Quantity
- CAT : Ranks
- HUE : Peak Wavelength
- REF : Reference
- LOT NO : Lot Number
- MADE IN TAIWAN : Production place

Packing Quantity Specification

- 1. 40 Pcs/1Plastic Case , 4Plastic Cases/1Box
- 2. 10 Boxes/1Carton

Reliability test item and condition :

The reliability of products shall be satisfied with items listed below.

Confidence level: 90%

LTPD: 10%

Test Items	Test Conditions	Failure Judgement Criteria	Samples(n)
			Defective(c)
Operation life	Vcc=5V, Ta:25°C 1000hrs	$L_0 \leq L \times 0.8$ $L_{45} \leq L \times 0.8$ L: Lower specification limit	n=22,c=0
Temperature cycle	1 cycle -20°C +25°C +70°C (30min) 5min (30min) 50 cycle test		n=22,c=0
Thermal shock	-10°C to +70°C (5min) (10sec) (5min) 50 cycle test		n=22,c=0
High temperature storage	Temp: +70°C 1000hrs		n=22,c=0
Low temperature storage	Temp: -20°C 1000hrs		n=22,c=0
High temperature High humidity	Ta: 85°C RH:85% 1000hrs		n=22,c=0
Solder heat	Temp: 260± 5°C 5sec 4mm Form the bottom of the package.		n=22,c=0
Solderability	Temp: 230± 5°C 5sec 4mm Form the bottom of the package.		More than 90% of Lead to be covered by soldering

TYPICAL ELECTRICAL/OPTICAL/CHARACTERISTICS CURVES

Fig.-4 Relative Spectral Sensitivity vs. Wavelength

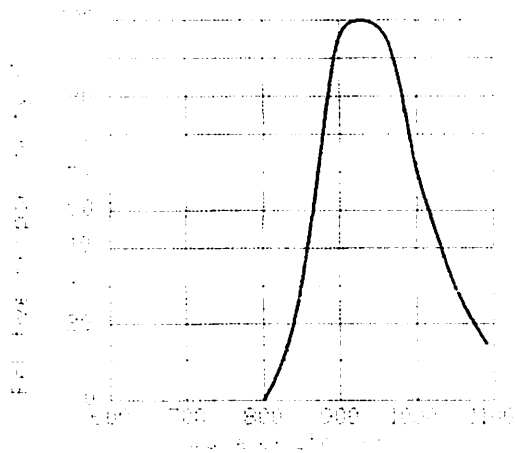


Fig.-5 Relative Transmission Distance vs. Direction

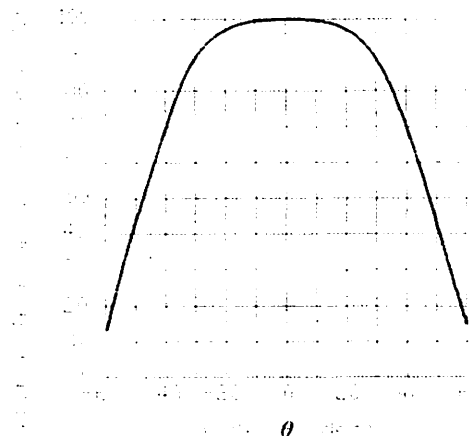


Fig.-6 Output Pulse Length vs. Arrival Distance

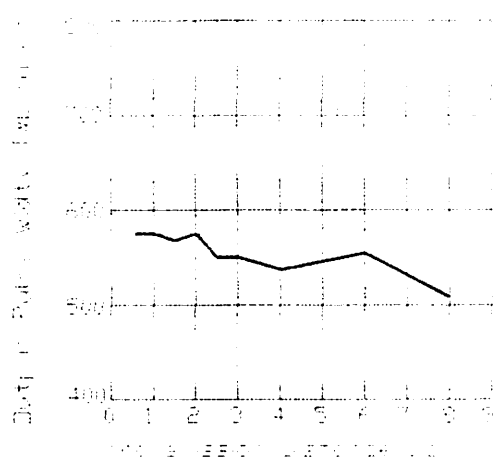


Fig.-7 Arrival Distance vs. Supply Voltage

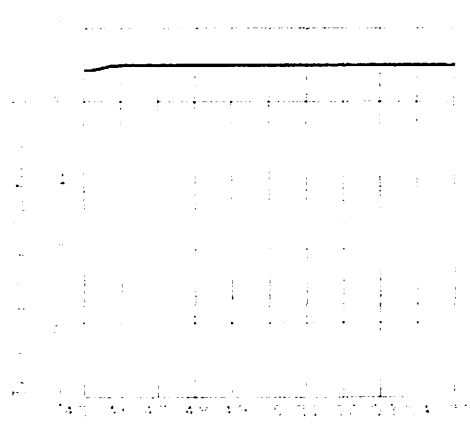


Fig.-8 Relative Transmission Distance vs. Center Carrier Frequency

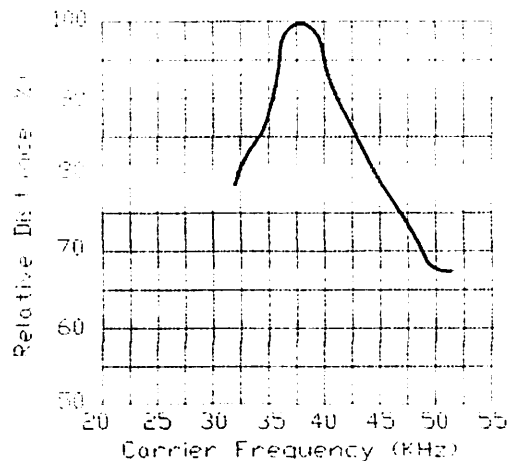
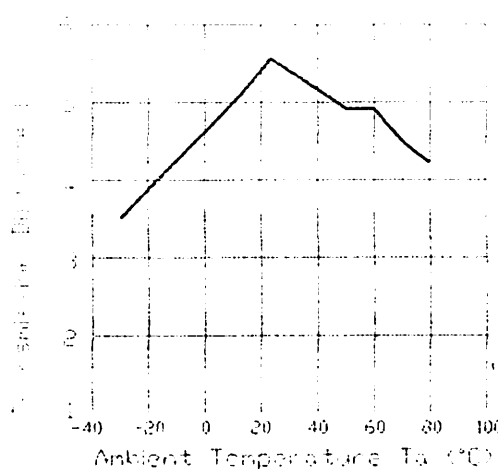


Fig.-9 Arrival Distance vs. Ambient Temperature



Module schematic & circuit :

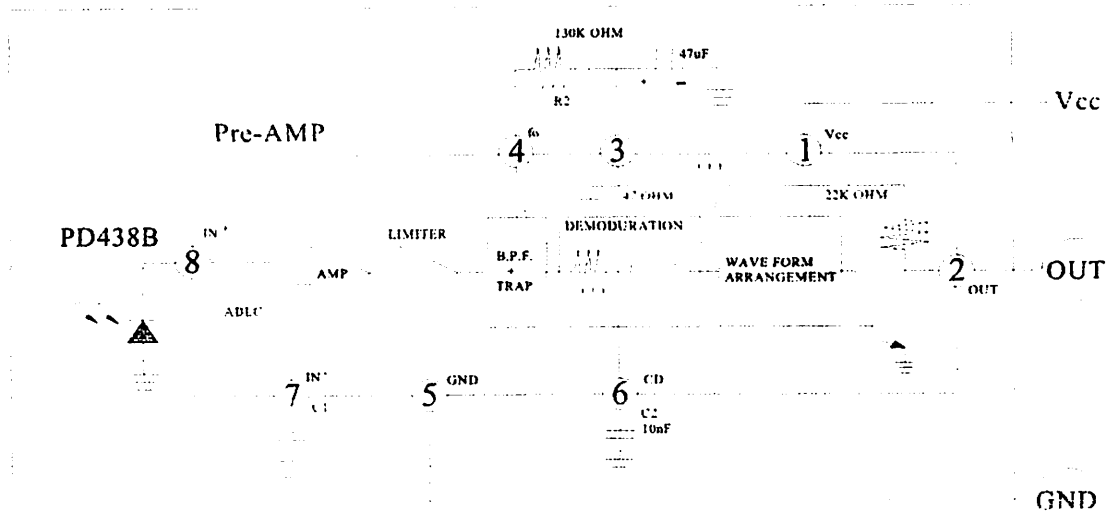


Fig.-1 Transmitter Wave Form

D.U.T Output Pulse

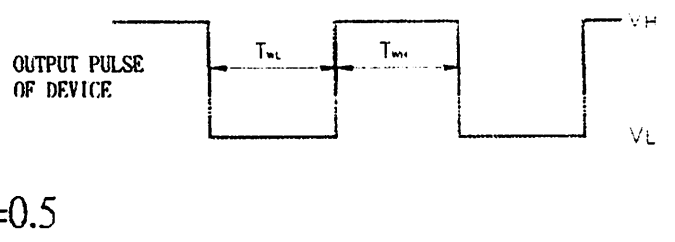
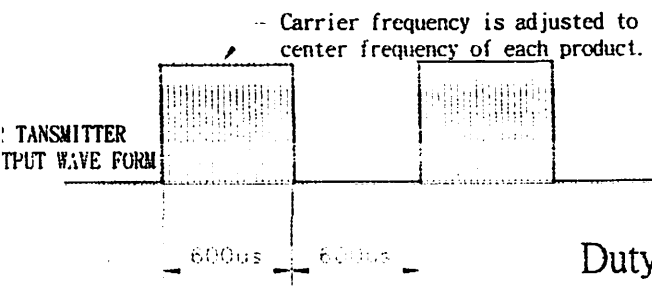
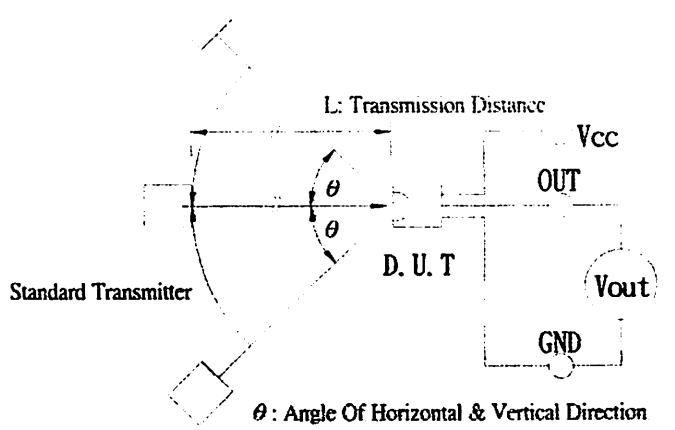
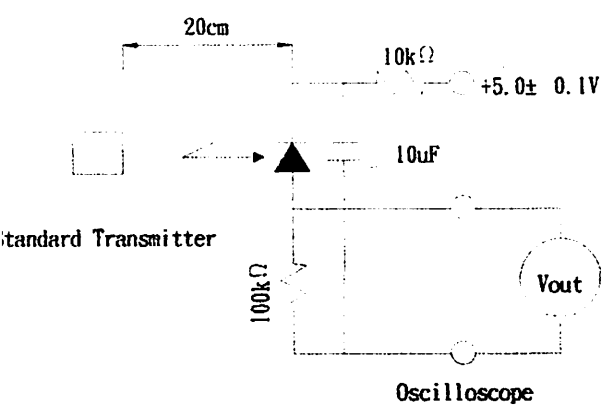


Fig.-2 Measuring Method

Fig.-3 Measuring System



■ TEST METHOD :

The specified electro-optical characteristics is satisfied under the following Conditions at the controllable distance.

① Measurement place

A place that is nothing of extreme light reflected in the room.

② External light

Project the light of ordinary white fluorescent lamps which are not high Frequency lamps and must be less then 10 Lux at the module surface.

($E_e \leq 10 \text{Lux}$)

③ Standard transmitter

A transmitter whose output is so adjusted as to $V_o = 400 \text{mVp-p}$ and the output Wave form shown in Fig.-1. According to the measurement method shown in Fig.-2 the standard transmitter is specified. However, the infrared photodiode to be used for the transmitter should be $\lambda_p = 940 \text{nm}$, $\Delta\lambda = 50 \text{nm}$. Also, photo diode is used of PD438B ($V_R = 5 \text{V}$).

(Standard light / Light source temperature 2856°K).

④ Measuring system

According to the measuring system shown in Fig.-3

Absolute maximum ratings : (Ta=25°C)

Parameter	Symbol	Ratings	Unit	Notice
Supply Voltage	Vcc	4.3~5.7	V	
Operating Temperature	Topr	-10~+60	°C	
Storage Temperature	Tstg	-20~+70	°C	
Soldering Temperature	Tsol	260	°C	4mm from mold body less than 5 seconds

Electro Optical Characteristics : (Ta=25°C)

Parameter	Symbol	MIN	TYP	MAX	Unit	Condition
Supply Voltage	Vcc	4.7	5	5.3	V	DC voltage
Supply Current	Icc	-	-	3	mA	No signal input
B.P.F Center Frequency	fo	-	37.9	-	KHz	
Peak Wavelength	λ_p	-	940	-	nm	
Transmission Distance	L ₀	5	-	-	m	At the ray axis *1
	L ₄₅	2.5	-	-		
Half Angle	θ	-	45	-	deg	
High Level Pulse Width	T _H	400	-	800	μs	At the ray axis *2
Low Level Pulse Width	T _L	400	-	800	μs	
High Level Output Voltage	V _H	4.5	-	-	V	
Low Level Output Voltage	V _L			0.5	V	

*1: The ray receiving surface at a vertex and relation to the ray axis in the range of $\phi = 0^\circ$ and $\phi = 45^\circ$.

*2: A range from 30cm to the arrival distance. Average value of 50 pulses.

Description :

1. The module is a small type infrared remote control system receiver which has been developed and designed by utilizing the latest hybrid technology.
2. This single unit type module incorporates a photo diode and a receiving preamplifier IC.
3. The demodulated output signal can directly be decoded by a microprocessor.

Feature :

1. High protection ability to EMI and metal case can be customized.
2. Mold type and metal case type to meet the design of front panel.
3. Elliptic lens to improve the characteristic against
4. Line-up for various center carrier frequencies.
5. Low voltage and low power consumption.
6. High immunity against ambient light.
7. Photodiode with integrated circuit.
8. TTL and CMOS compatibility.
9. Long reception distance.
10. High sensitivity.

Application :

1. Optical switch
2. Light detecting portion of remote control
 - AV instruments such as Audio, TV, VCR, CD, MD, etc.
 - Home appliances such as Air-conditioner, Fan , etc.
 - The other equipments with wireless remote control.
 - CATV set top boxes
 - Multi-media Equipment



EVERLIGHT ELECTRONICS CO., LTD.

Device Number: DMO-851-005 REV: 1.1

MODEL NO: IRM-8510/N ECN: _____ Page: 2/9

NOTES :

This drawing measure is a standard value. All dimensions are in millimeter.

In case of designation is tolerance $\pm 0.3\text{mm}$.

Lead spacing is measured where the lead emerge from the package.

Above specification may be changed without notice. EVERLIGHT will reserve authority on material change for above specification.

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When using this produce, please observe the absolute maximum ratings and the instructions for use outlined in these specification sheets. EVERLIGHT assumes no responsibility for any damage resulting from use of the product which does not comply with the absolute maximum ratings and the instructions included in these specification sheets.

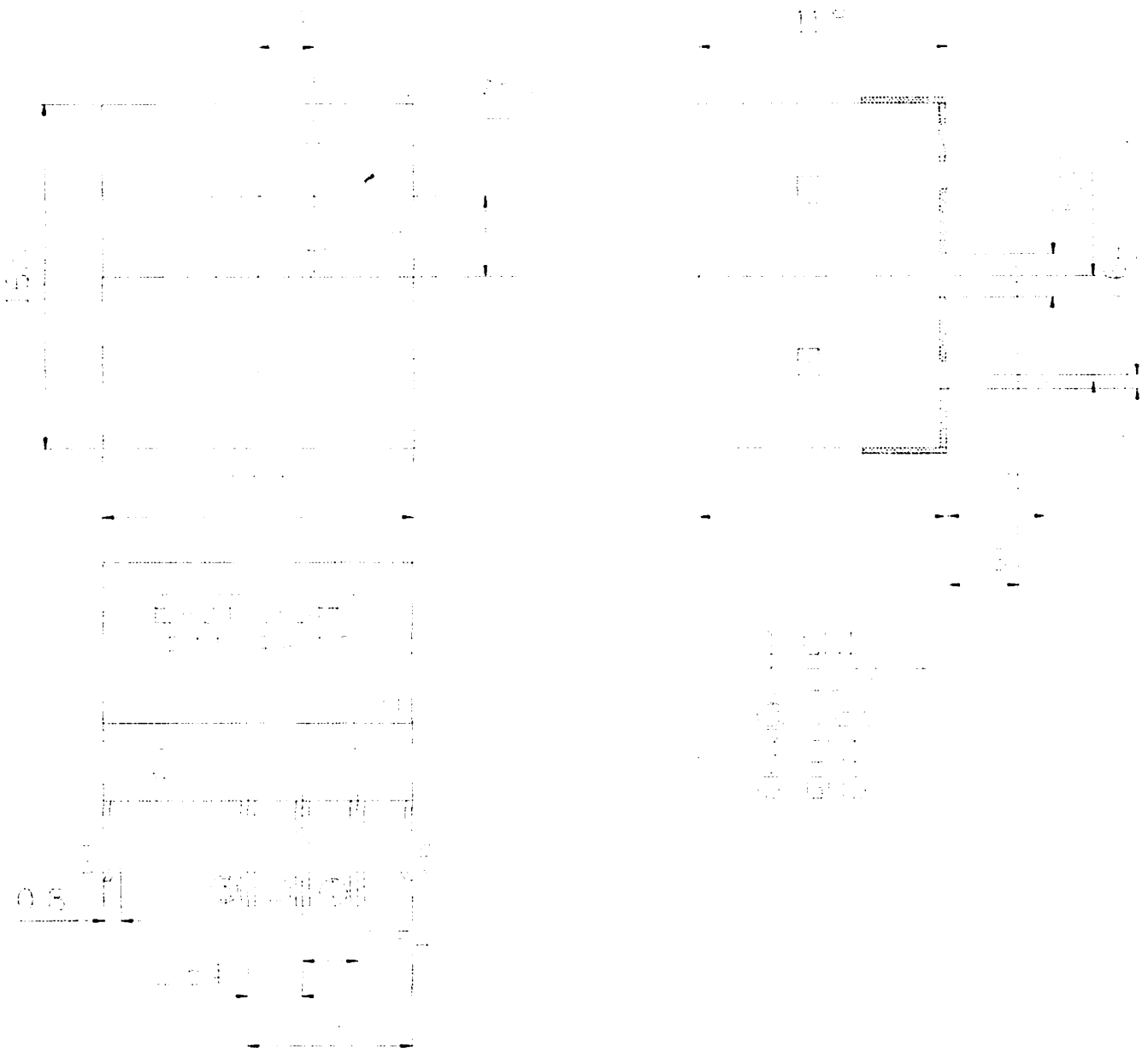


EVERLIGHT ELECTRONICS CO., LTD.

Device Number: DMO-851-005 REV: 1.1

MODEL NO: IRM-8510/N ECN: _____ Page: 1/9

PACKAGE DIMENSIONS :



OFFICE: NO 25, Lane 76, Chung Yang Rd, Sec.3 Tucheng, Taipei 236, Taiwan, R.O.C.

TEL : 886-2-2267-2000, 2266-9936 (22 Lines)

FAX : 886-2-2267-6189

<http://www.everlight.com>

Features

- Compatible with MCS-51[®] Products
- 8K Bytes of In-System Programmable (ISP) Flash Memory
- Endurance: 1000 Write/Erase Cycles
- 2.7V to 5.5V Operating Range
- Asynchronously Static Operation: 0 Hz to 33 MHz
- Three-level Program Memory Lock
- 64 x 8-bit Internal RAM
- 32 Programmable I/O Lines
- Three 16-bit Timer/Counters
- Eight Interrupt Sources
- Full Duplex UART Serial Channel
- Low-power Idle and Power-down Modes
- Interrupt Recovery from Power-down Mode
- Watchdog Timer
- Local Data Pointer
- Power-off Flag
- Fast Programming Time
- Flexible ISP Programming (Byte and Page Mode)

Description

AT89S52 is a low-power, high-performance CMOS 8-bit microcontroller with 8K bytes of in-system programmable Flash memory. The device is manufactured using Atmel's high-density nonvolatile memory technology and is compatible with the industry standard 80C51 instruction set and pinout. The on-chip Flash allows the program memory to be reprogrammed in-system or by a conventional nonvolatile memory programmer. By combining a versatile 8-bit CPU with in-system programmable Flash on a monolithic chip, the Atmel AT89S52 is a powerful microcontroller which provides a highly-flexible and cost-effective solution to many embedded control applications.

AT89S52 provides the following standard features: 8K bytes of Flash, 256 bytes of internal RAM, 32 I/O lines, Watchdog timer, two data pointers, three 16-bit timer/counters, a vector two-level interrupt architecture, a full duplex serial port, on-chip oscillator, and clock circuitry. In addition, the AT89S52 is designed with static logic for operation down to zero frequency and supports two software selectable power saving modes. The Idle Mode stops the CPU while allowing the RAM, timer/counters, serial port, and interrupt system to continue functioning. The Power-down mode saves the RAM contents but freezes the oscillator, disabling all other chip functions until the next interrupt or hardware reset.



8-bit Microcontroller with 8K Bytes In-System Programmable Flash

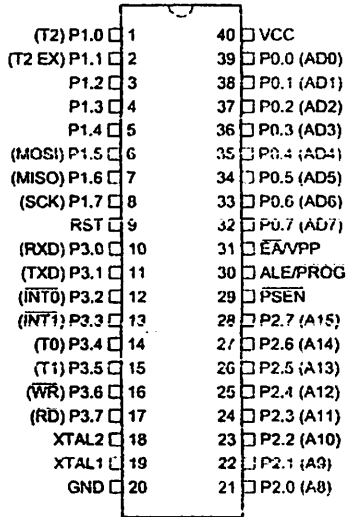
AT89S52



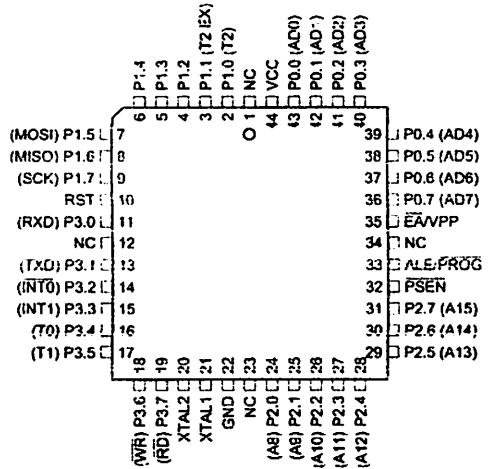


Pin Configurations

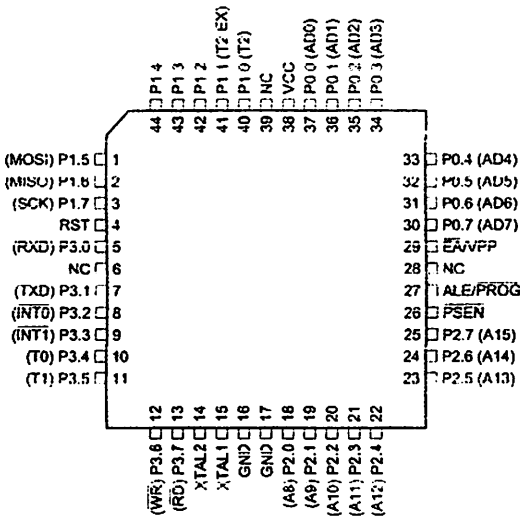
PDIP



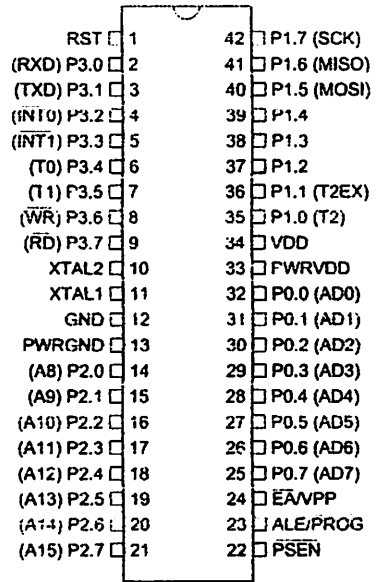
PLCC



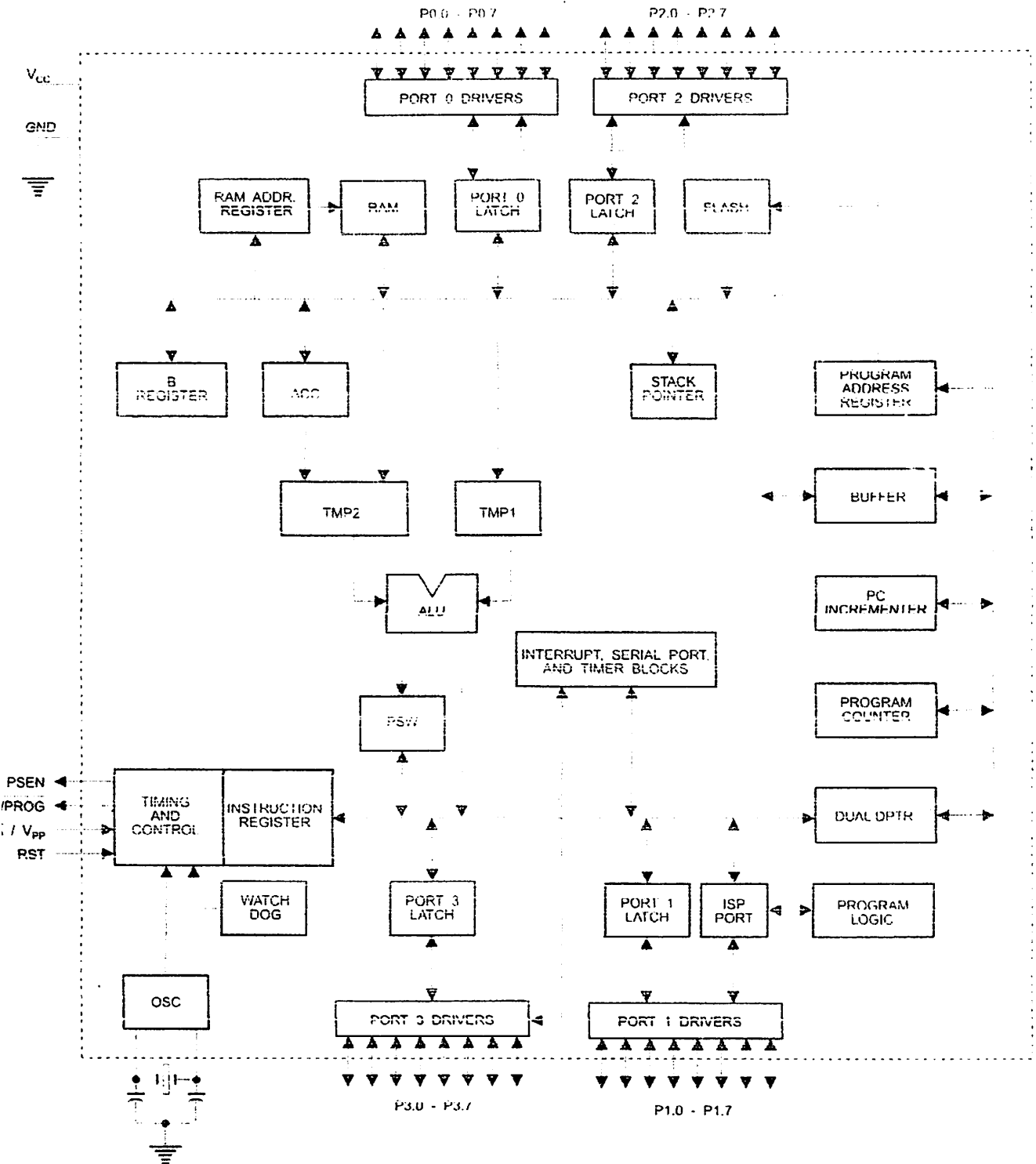
TQFP



PDIP



Block Diagram





Pin Description

V_{CC} Supply voltage.

GND Ground.

Port 0 is an 8-bit open drain bidirectional I/O port. As an output port, each pin can sink eight TTL inputs. When 1s are written to port 0 pins, the pins can be used as high-impedance inputs.

Port 0 can also be configured to be the multiplexed low-order address/data bus during accesses to external program and data memory. In this mode, P0 has internal pull-ups.

Port 0 also receives the code bytes during Flash programming and outputs the code bytes during program verification. **External pull-ups are required during program verification.**

Port 1 is an 8-bit bidirectional I/O port with internal pull-ups. The Port 1 output buffers can sink/source four TTL inputs. When 1s are written to Port 1 pins, they are pulled high by the internal pull-ups and can be used as inputs. As inputs, Port 1 pins that are externally being pulled low will source current (I_{IL}) because of the internal pull-ups.

In addition, P1.0 and P1.1 can be configured to be the timer/counter 2 external count input (P1.0/T2) and the timer/counter 2 trigger input (P1.1/T2EX), respectively, as shown in the following table.

Port 1 also receives the low-order address bytes during Flash programming and verification.

Port Pin	Alternate Functions
P1.0	T2 (external count input to Timer/Counter 2), clock-out
P1.1	T2EX (Timer/Counter 2 capture/reload trigger and direction control)
P1.5	MOSI (used for In-System Programming)
P1.6	MISO (used for In-System Programming)
P1.7	SCK (used for In-System Programming)

Port 2 is an 8-bit bidirectional I/O port with internal pull-ups. The Port 2 output buffers can sink/source four TTL inputs. When 1s are written to Port 2 pins, they are pulled high by the internal pull-ups and can be used as inputs. As inputs, Port 2 pins that are externally being pulled low will source current (I_{IL}) because of the internal pull-ups.

Port 2 emits the high-order address byte during fetches from external program memory and during accesses to external data memory that use 16-bit addresses (MOVX @ DPTR). In this application, Port 2 uses strong internal pull-ups when emitting 1s. During accesses to external data memory that use 8-bit addresses (MOVX @ RI), Port 2 emits the contents of the P2 Special Function Register.

Port 2 also receives the high-order address bits and some control signals during Flash programming and verification.

Port 3 is an 8-bit bidirectional I/O port with internal pull-ups. The Port 3 output buffers can sink/source four TTL inputs. When 1s are written to Port 3 pins, they are pulled high by the internal pull-ups and can be used as inputs. As inputs, Port 3 pins that are externally being pulled low will source current (I_{IL}) because of the pull-ups.

Port 3 receives some control signals for Flash programming and verification.

Port 3 also serves the functions of various special features of the AT89S52, as shown in the following table.

Port Pin	Alternate Functions
P3.0	RXD (serial input port)
P3.1	TXD (serial output port)
P3.2	INT0 (external interrupt 0)
P3.3	INT1 (external interrupt 1)
P3.4	T0 (timer 0 external input)
P3.5	T1 (timer 1 external input)
P3.6	\overline{WR} (external data memory write strobe)
P3.7	\overline{RD} (external data memory read strobe)

Reset input. A high on this pin for two machine cycles while the oscillator is running resets the device. This pin drives high for 98 oscillator periods after the Watchdog times out. The DISRTO bit in SFR AUXR (address 8EH) can be used to disable this feature. In the default state of bit DISRTO, the RESET HIGH out feature is enabled.

\overline{PROG}

Address Latch Enable (ALE) is an output pulse for latching the low byte of the address during accesses to external memory. This pin is also the program pulse input (\overline{PROG}) during Flash programming.

In normal operation, ALE is emitted at a constant rate of 1/6 the oscillator frequency and may be used for external timing or clocking purposes. Note, however, that one ALE pulse is skipped during each access to external data memory.

If desired, ALE operation can be disabled by setting bit 0 of SFR location 8EH. With the bit set, ALE is active only during a MOVX or MOVC instruction. Otherwise, the pin is weakly pulled high. Setting the ALE-disable bit has no effect if the microcontroller is in external execution mode.

\overline{N}

Program Store Enable (\overline{PSEN}) is the read strobe to external program memory.

When the AT89S52 is executing code from external program memory, \overline{PSEN} is activated twice each machine cycle, except that two \overline{PSEN} activations are skipped during each access to external data memory.

\overline{PP}

External Access Enable. \overline{EA} must be strapped to GND in order to enable the device to fetch code from external program memory locations starting at 0000H up to FFFFH. Note, however, that if lock bit 1 is programmed, \overline{EA} will be internally latched on reset.

\overline{EA} should be strapped to V_{CC} for internal program executions.

This pin also receives the 12-volt programming enable voltage (V_{PP}) during Flash programming.

L1

Input to the inverting oscillator amplifier and input to the internal clock operating circuit.

L2

Output from the inverting oscillator amplifier.



Special Function Registers

A map of the on-chip memory area called the Special Function Register (SFR) space is shown in Table 1.

Note that not all of the addresses are occupied, and unoccupied addresses may not be implemented on the chip. Read accesses to these addresses will in general return random data, and write accesses will have an indeterminate effect.

User software should not write 1s to these unlisted locations, since they may be used in future products to invoke new features. In that case, the reset or inactive values of the new bits will always be 0.

Timer 2 Registers: Control and status bits are contained in registers T2CON (shown in Table 2) and T2MOD (shown in Table 6) for Timer 2. The register pair (RCAP2H, RCAP2L) are the Capture/Reload registers for Timer 2 in 16-bit capture mode or 16-bit auto-reload mode.

Interrupt Registers: The individual interrupt enable bits are in the IE register. Two priorities can be set for each of the six interrupt sources in the IP register.

Table 1. AT89S52 SFR Map and Reset Values

0F8H								0FFH
0F0H	B 00000000							0F7H
0E8H								0EFH
0E0H	ACC 00000000							0E7H
0D8H								0DFH
0D0H	PSW 00000000							0D7H
0C8H	T2CON 00000000	T2MOD XXXXXX00	RCAP2L 00000000	RCAP2H 00000000	TL2 00000000	TH2 00000000		0CFH
0C0H								0C7H
0B8H	IP XX000000							0BFH
0B0H	P3 11111111							0B7H
0A8H	IE 0X000000							0AFH
0A0H	P2 11111111		AUXR1 XXXXXXXX0				WDRST XXXXXXXXX	0A7H
98H	SCON 00000000	SBUF XXXXXXXXX						9FH
90H	P1 11111111							97H
88H	TCON 00000000	TMOD 00000000	TL0 00000000	TL1 00000000	TH0 00000000	TH1 00000000	AUXR XXX00XX0	8FH
80H	P0 11111111	SP 00000111	DP0L 00000000	DP0H 00000000	DP1L 00000000	DP1H 00000000	PCON 0XXX0000	87H

2. T2CON – Timer/Counter 2 Control Register

T2CON Address = 0C8H		Reset Value = 0000 0000B						
3bit Addressable								
3bit	TF2	EXF2	RCLK	TCLK	EXEN2	TR2	C/T2	CP/RL2
	7	6	5	4	3	2	1	0

Bit	Function
7	Timer 2 overflow flag set by a Timer 2 overflow and must be cleared by software. TF2 will not be set when either RCLK = 1 or TCLK = 1.
6	Timer 2 external flag set when either a capture or reload is caused by a negative transition on T2EX and EXEN2 = 1. When Timer 2 interrupt is enabled, EXF2 = 1 will cause the CPU to vector to the Timer 2 interrupt routine. EXF2 must be cleared by software. EXF2 does not cause an interrupt in up/down counter mode (DCEN = 1).
5	Receive clock enable. When set, causes the serial port to use Timer 2 overflow pulses for its receive clock in serial port Modes 1 and 3. RCLK = 0 causes Timer 1 overflow to be used for the receive clock.
4	Transmit clock enable. When set, causes the serial port to use Timer 2 overflow pulses for its transmit clock in serial port Modes 1 and 3. TCLK = 0 causes Timer 1 overflows to be used for the transmit clock.
3	Timer 2 external enable. When set, allows a capture or reload to occur as a result of a negative transition on T2EX if Timer 2 is not being used to clock the serial port. EXEN2 = 0 causes Timer 2 to ignore events at T2EX.
2	Start/Stop control for Timer 2. TR2 = 1 starts the timer.
1	Timer or counter select for Timer 2. C/T2 = 0 for timer function. C/T2 = 1 for external event counter (falling edge triggered).
0	Capture/Reload select. CP/RL2 = 1 causes captures to occur on negative transitions at T2EX if EXEN2 = 1. CP/RL2 = 0 causes automatic reloads to occur when Timer 2 overflows or negative transitions occur at T2EX when EXEN2 = 1. When either RCLK or TCLK = 1, this bit is ignored and the timer is forced to auto-reload on Timer 2 overflow.



Table 3. AUXR: Auxiliary Register

AUXR	Address = 8EH	Reset Value = XXX00XX0B						
	Not Bit Addressable							
	-	-	-	WDIDLE	DISRTO	-	-	DISALE
Bit	7	6	5	4	3	2	1	0
	Reserved for future expansion							
DISALE	Disable/Enable ALE							
DISALE	Operating Mode							
0	ALE is emitted at a constant rate of 1/6 the oscillator frequency							
1	ALE is active only during a MOVX or MOVC instruction							
DISRTO	Disable/Enable Reset out							
DISRTO								
0	Reset pin is driven High after WDT times out							
1	Reset pin is input only							
WDIDLE	Disable/Enable WDT in IDLE mode							
WDIDLE								
0	WDT continues to count in IDLE mode							
1	WDT halts counting in IDLE mode							

Data Pointer Registers: To facilitate accessing both internal and external data memory, two banks of 16-bit Data Pointer Registers are provided: DP0 at SFR address locations 82H-83H and DP1 at 84H-85H. Bit DPS = 0 in SFR AUXR1 selects DP0 and DPS = 1 selects DP1. The user should **ALWAYS** initialize the DPS bit to the appropriate value before accessing the respective Data Pointer Register.

Power Off Flag: The Power Off Flag (POF) is located at bit 4 (PCON.4) in the PCON SFR. POF is set to "1" during power up. It can be set and reset under software control and is not affected by reset.

Table 4. AUXR1: Auxiliary Register 1

AUXR1	Address = A2H	Reset Value = XXXXXXX0B						
	Not Bit Addressable							
	-	-	-	-	-	-	-	DPS
Bit	7	6	5	4	3	2	1	0
	Reserved for future expansion							
DPS	Data Pointer Register Select							
DPS								
0	Selects DPTR Registers DP0L, DP0H							
1	Selects DPTR Registers DP1L, DP1H							

Memory Organization MCS-51 devices have a separate address space for Program and Data Memory. Up to 64K bytes each of external Program and Data Memory can be addressed.

Program Memory If the \overline{EA} pin is connected to GND, all program fetches are directed to external memory. On the AT89S52, if \overline{EA} is connected to V_{CC} , program fetches to addresses 0000H through 1FFFH are directed to internal memory and fetches to addresses 2000H through FFFFH are to external memory.

Data Memory The AT89S52 implements 256 bytes of on-chip RAM. The upper 128 bytes occupy a parallel address space to the Special Function Registers. This means that the upper 128 bytes have the same addresses as the SFR space but are physically separate from SFR space.

When an instruction accesses an internal location above address 7FH, the address mode used in the instruction specifies whether the CPU accesses the upper 128 bytes of RAM or the SFR space. Instructions which use direct addressing access the SFR space.

For example, the following direct addressing instruction accesses the SFR at location 0A0H (which is P2).

```
MOV 0A0H, #data
```

Instructions that use indirect addressing access the upper 128 bytes of RAM. For example, the following indirect addressing instruction, where R0 contains 0A0H, accesses the data byte at address 0A0H, rather than P2 (whose address is 0A0H).

```
MOV @R0, #data
```

Note that stack operations are examples of indirect addressing, so the upper 128 bytes of data RAM are available as stack space.

Watchdog Timer (Time Enabled on Reset-out)

The WDT is intended as a recovery method in situations where the CPU may be subjected to software upsets. The WDT consists of a 14-bit counter and the Watchdog Timer Reset (WDTRST) SFR. The WDT is defaulted to disable from exiting reset. To enable the WDT, a user must write 01EH and 0E1H in sequence to the WDTRST register (SFR location 0A6H). When the WDT is enabled, it will increment every machine cycle while the oscillator is running. The WDT timeout period is dependent on the external clock frequency. There is no way to disable the WDT except through reset (either hardware reset or WDT overflow reset). When WDT overflows, it will drive an output RESET HIGH pulse at the RST pin.

Enabling the WDT

To enable the WDT, a user must write 01EH and 0E1H in sequence to the WDTRST register (SFR location 0A6H). When the WDT is enabled, the user needs to service it by writing 01EH and 0E1H to WDTRST to avoid a WDT overflow. The 14-bit counter overflows when it reaches 16383 (3FFFH), and this will reset the device. When the WDT is enabled, it will increment every machine cycle while the oscillator is running. This means the user must reset the WDT at least every 16383 machine cycles. To reset the WDT the user must write 01EH and 0E1H to WDTRST. WDTRST is a write-only register. The WDT counter cannot be read or written. When WDT overflows, it will generate an output RESET pulse at the RST pin. The RESET pulse duration is $98 \times T_{OSC}$, where $T_{OSC} = 1/F_{OSC}$. To make the best use of the WDT, it should be serviced in those sections of code that will periodically be executed within the time required to prevent a WDT reset.





WDT During Power-down and Idle

In Power-down mode the oscillator stops, which means the WDT also stops. While in Power-down mode, the user does not need to service the WDT. There are two methods of exiting Power-down mode: by a hardware reset or via a level-activated external interrupt which is enabled prior to entering Power-down mode. When Power-down is exited with hardware reset, servicing the WDT should occur as it normally does whenever the AT89S52 is reset. Exiting Power-down with an interrupt is significantly different. The interrupt is held low long enough for the oscillator to stabilize. When the interrupt is brought high, the interrupt is serviced. To prevent the WDT from resetting the device while the interrupt pin is held low, the WDT is not started until the interrupt is pulled high. It is suggested that the WDT be reset during the interrupt service for the interrupt used to exit Power-down mode.

To ensure that the WDT does not overflow within a few states of exiting Power-down, it is best to reset the WDT just before entering Power-down mode.

Before going into the IDLE mode, the WDIDLE bit in SFR AUXR is used to determine whether the WDT continues to count if enabled. The WDT keeps counting during IDLE (WDIDLE bit = 0) as the default state. To prevent the WDT from resetting the AT89S52 while in IDLE mode, the user should always set up a timer that will periodically exit IDLE, service the WDT, and reenter IDLE mode.

With WDIDLE bit enabled, the WDT will stop to count in IDLE mode and resumes the count upon exit from IDLE.

UART

The UART in the AT89S52 operates the same way as the UART in the AT89C51 and AT89C52. For further information on the UART operation, refer to the ATMEL Web site (<http://www.atmel.com>). From the home page, select "Products", then "8051-Architecture Flash Microcontroller", then "Product Overview".

Timer 0 and 1

Timer 0 and Timer 1 in the AT89S52 operate the same way as Timer 0 and Timer 1 in the AT89C51 and AT89C52. For further information on the timers' operation, refer to the ATMEL Web site (<http://www.atmel.com>). From the home page, select "Products", then "8051-Architecture Flash Microcontroller", then "Product Overview".

Timer 2

Timer 2 is a 16-bit Timer/Counter that can operate as either a timer or an event counter. The type of operation is selected by bit $C/\overline{TR2}$ in the SFR T2CON (shown in Table 2). Timer 2 has three operating modes: capture, auto-reload (up or down counting), and baud rate generator. The modes are selected by bits in T2CON, as shown in Table 5. Timer 2 consists of two 8-bit registers, TH2 and TL2. In the Timer function, the TL2 register is incremented every machine cycle. Since a machine cycle consists of 12 oscillator periods, the count rate is 1/12 of the oscillator frequency.

Table 5. Timer 2 Operating Modes

RCLK +TCLK	CP/ $\overline{RL2}$	TR2	MODE
0	0	1	16-bit Auto-reload
0	1	1	16-bit Capture
1	X	1	Baud Rate Generator
X	X	0	(Off)

In the Counter function, the register is incremented in response to a 1-to-0 transition at its corresponding external input pin, T2. In this function, the external input is sampled during S5P2 of every machine cycle. When the samples show a high in one cycle and a low in the next cycle, the count is incremented. The new count value appears in the register during S3P1 of the cycle following the one in which the transition was detected. Since two machine cycles (24 oscillator periods) are required to recognize a 1-to-0 transition, the maximum count rate is 1/24 of the oscillator frequency. To ensure that a given level is sampled at least once before it changes, the level should be held for at least one full machine cycle.

Capture Mode

In the capture mode, two options are selected by bit EXEN2 in T2CON. If EXEN2 = 0, Timer 2 is a 16-bit timer or counter which upon overflow sets bit TF2 in T2CON. This bit can then be used to generate an interrupt. If EXEN2 = 1, Timer 2 performs the same operation, but a 1-to-0 transition at external input T2EX also causes the current value in TH2 and TL2 to be captured into RCAP2H and RCAP2L, respectively. In addition, the transition at T2EX causes bit EXF2 in T2CON to be set. The EXF2 bit, like TF2, can generate an interrupt. The capture mode is illustrated in Figure 1.

Auto-reload (Up or Down Counter)

Timer 2 can be programmed to count up or down when configured in its 16-bit auto-reload mode. This feature is invoked by the DCEN (Down Counter Enable) bit located in the SFR T2MOD (see Table 6). Upon reset, the DCEN bit is set to 0 so that timer 2 will default to count up. When DCEN is set, Timer 2 can count up or down, depending on the value of the T2EX pin.

Figure 1. Timer in Capture Mode

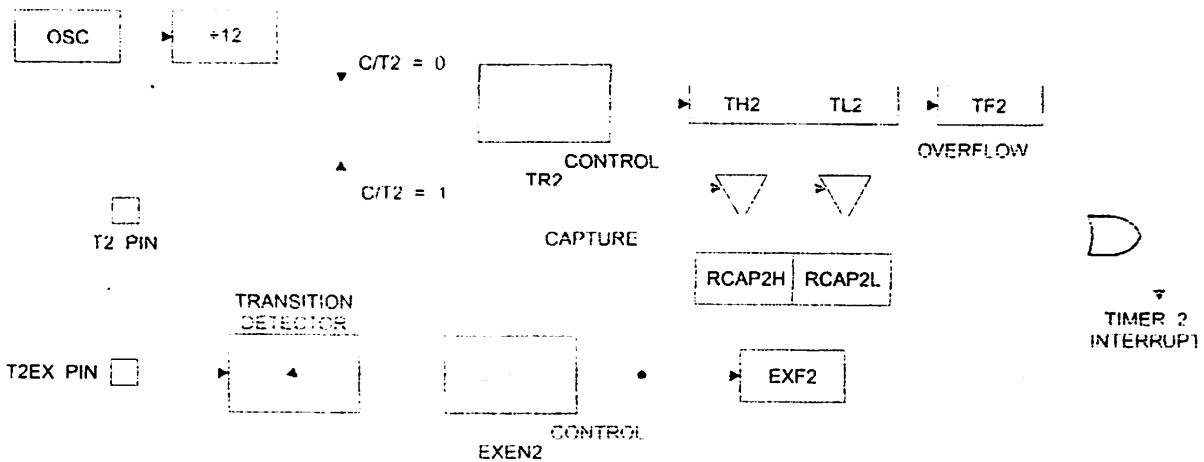




Figure 2 shows Timer 2 automatically counting up when $DCEN = 0$. In this mode, two options are selected by bit $EXEN2$ in $T2CON$. If $EXEN2 = 0$, Timer 2 counts up to $0FFFFH$ and then sets the $TF2$ bit upon overflow. The overflow also causes the timer registers to be reloaded with the 16-bit value in $RCAP2H$ and $RCAP2L$. The values in Timer in Capture Mode $RCAP2H$ and $RCAP2L$ are preset by software. If $EXEN2 = 1$, a 16-bit reload can be triggered either by an overflow or by a 1-to-0 transition at external input $T2EX$. This transition also sets the $EXF2$ bit. Both the $TF2$ and $EXF2$ bits can generate an interrupt if enabled.

Setting the $DCEN$ bit enables Timer 2 to count up or down, as shown in Figure 2. In this mode, the $T2EX$ pin controls the direction of the count. A logic 1 at $T2EX$ makes Timer 2 count up. The timer will overflow at $0FFFFH$ and set the $TF2$ bit. This overflow also causes the 16-bit value in $RCAP2H$ and $RCAP2L$ to be reloaded into the timer registers, $TH2$ and $TL2$, respectively.

A logic 0 at $T2EX$ makes Timer 2 count down. The timer underflows when $TH2$ and $TL2$ equal the values stored in $RCAP2H$ and $RCAP2L$. The underflow sets the $TF2$ bit and causes $0FFFFH$ to be reloaded into the timer registers.

The $EXF2$ bit toggles whenever Timer 2 overflows or underflows and can be used as a 17th bit of resolution. In this operating mode, $EXF2$ does not flag an interrupt.

Figure 2. Timer 2 Auto Reload Mode ($DCEN = 0$)

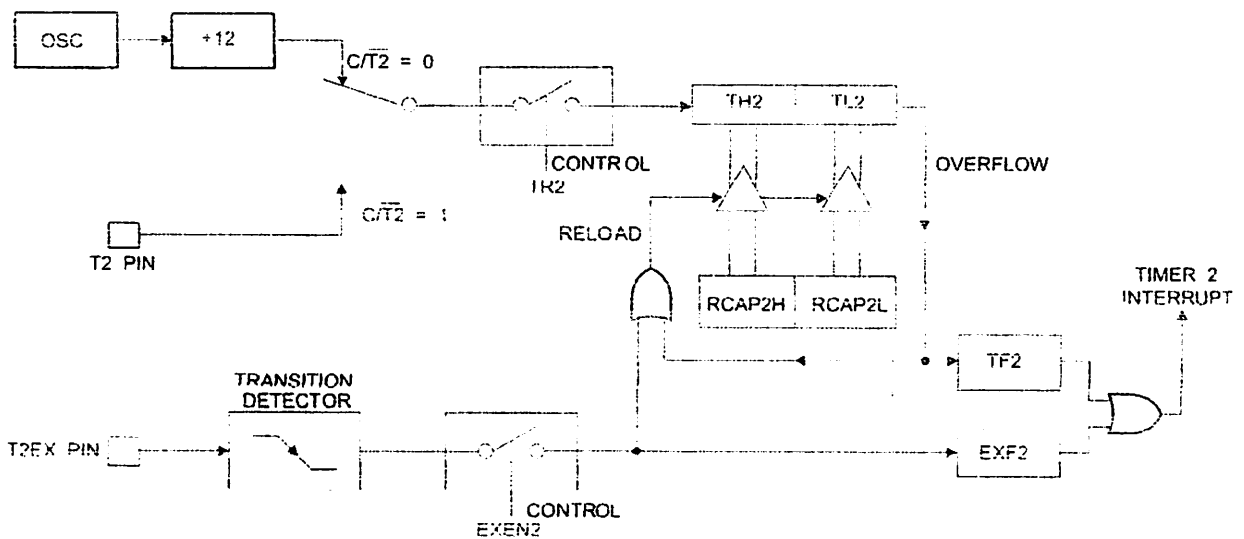
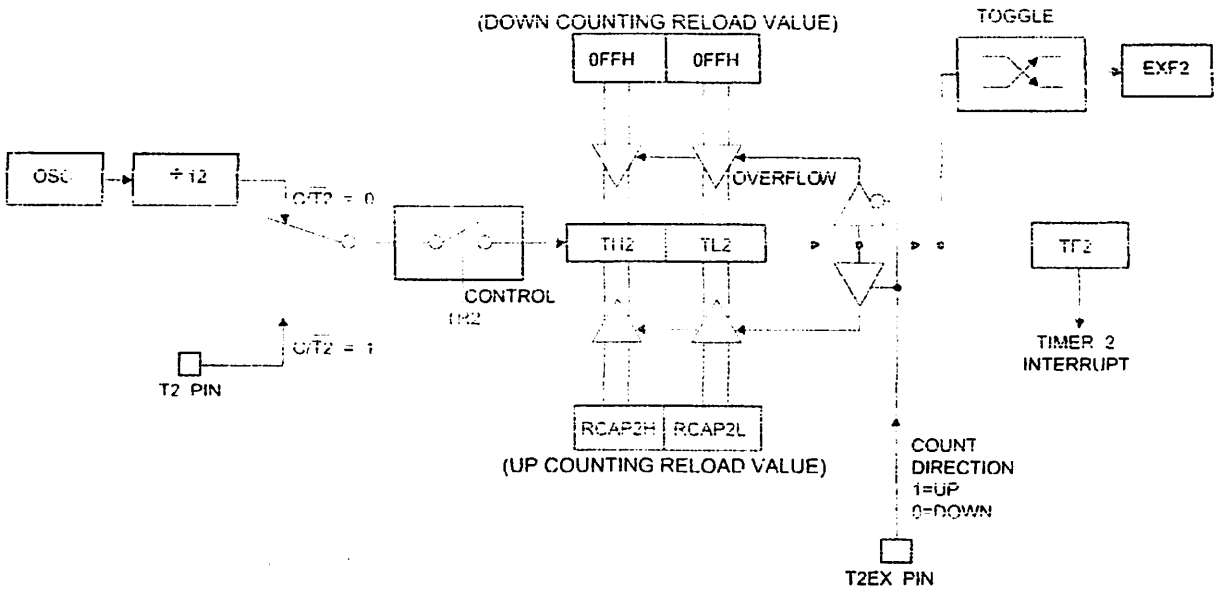


Figure 6. T2MOD – Timer 2 Mode Control Register

T2MOD Address = 0C9H						Reset Value = XXXX XX00B		
Not Bit Addressable								
Bit	7	6	5	4	3	2	T2OE 1	DCEN 0
bit 7	-	-	-	-	-	-		
bit 6	-	-	-	-	-	-		
bit 5	-	-	-	-	-	-		
bit 4	-	-	-	-	-	-		
bit 3	-	-	-	-	-	-		
bit 2	-	-	-	-	-	-		
bit 1	-	-	-	-	-	-		
bit 0	-	-	-	-	-	-		

bit	Function
7	Not implemented, reserved for future
6	Not implemented, reserved for future
5	Not implemented, reserved for future
4	Not implemented, reserved for future
3	Not implemented, reserved for future
2	Not implemented, reserved for future
1	Timer 2 Output Enable bit
0	When set, this bit allows Timer 2 to be configured as an up/down counter

Figure 3. Timer 2 Auto Reload Mode (DCEN = 1)





Baud Rate Generator

Timer 2 is selected as the baud rate generator by setting TCLK and/or RCLK in T2CON (Table 2). Note that the baud rates for transmit and receive can be different if Timer 2 is used for the receiver or transmitter and Timer 1 is used for the other function. Setting RCLK and/or TCLK puts Timer 2 into its baud rate generator mode, as shown in Figure 4.

The baud rate generator mode is similar to the auto-reload mode, in that a rollover in TH2 causes the Timer 2 registers to be reloaded with the 16-bit value in registers RCAP2H and RCAP2L, which are preset by software.

The baud rates in Modes 1 and 3 are determined by Timer 2's overflow rate according to the following equation.

$$\text{Modes 1 and 3 Baud Rates} = \frac{\text{Timer 2 Overflow Rate}}{16}$$

The Timer can be configured for either timer or counter operation. In most applications, it is configured for timer operation ($CP/\overline{TF2} = 0$). The timer operation is different for Timer 2 when it is used as a baud rate generator. Normally, as a timer, it increments every machine cycle (at $1/12$ the oscillator frequency). As a baud rate generator, however, it increments every state time (at $1/2$ the oscillator frequency). The baud rate formula is given below.

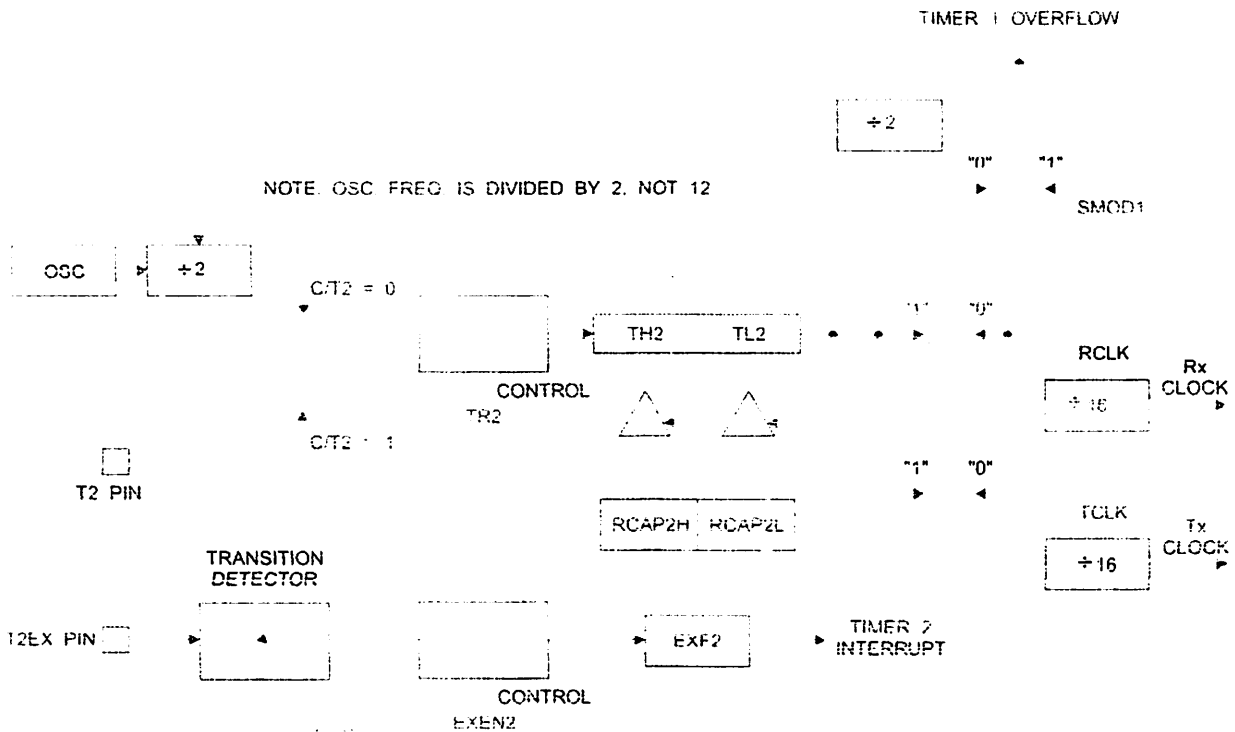
$$\frac{\text{Modes 1 and 3}}{\text{Baud Rate}} = \frac{\text{Oscillator Frequency}}{32 \times [65536 - \text{RCAP2H}, \text{RCAP2L}]}$$

where (RCAP2H, RCAP2L) is the content of RCAP2H and RCAP2L taken as a 16-bit unsigned integer.

Timer 2 as a baud rate generator is shown in Figure 4. This figure is valid only if RCLK or TCLK = 1 in T2CON. Note that a rollover in TH2 does not set TF2 and will not generate an interrupt. Note too, that if EXEN2 is set, a 1-to-0 transition in T2EX will set EXF2 but will not cause a reload from (RCAP2H, RCAP2L) to (TH2, TL2). Thus, when Timer 2 is in use as a baud rate generator, T2EX can be used as an extra external interrupt.

Note that when Timer 2 is running ($TR2 = 1$) as a timer in the baud rate generator mode, TH2 or TL2 should not be read from or written to. Under these conditions, the Timer is incremented every state time, and the results of a read or write may not be accurate. The RCAP2 registers may be read but should not be written to, because a write might overlap a reload and cause write and/or reload errors. The timer should be turned off (clear TR2) before accessing the Timer 2 or RCAP2 registers.

Figure 4. Timer 2 in Baud Rate Generator Mode



Programmable Clock Out

A 50% duty cycle clock can be programmed to come out on P1.0, as shown in Figure 5. This pin, besides being a regular I/O pin, has two alternate functions. It can be programmed to input the external clock for Timer/Counter 2 or to output a 50% duty cycle clock ranging from 61 Hz to 4 MHz (for a 16-MHz operating frequency).

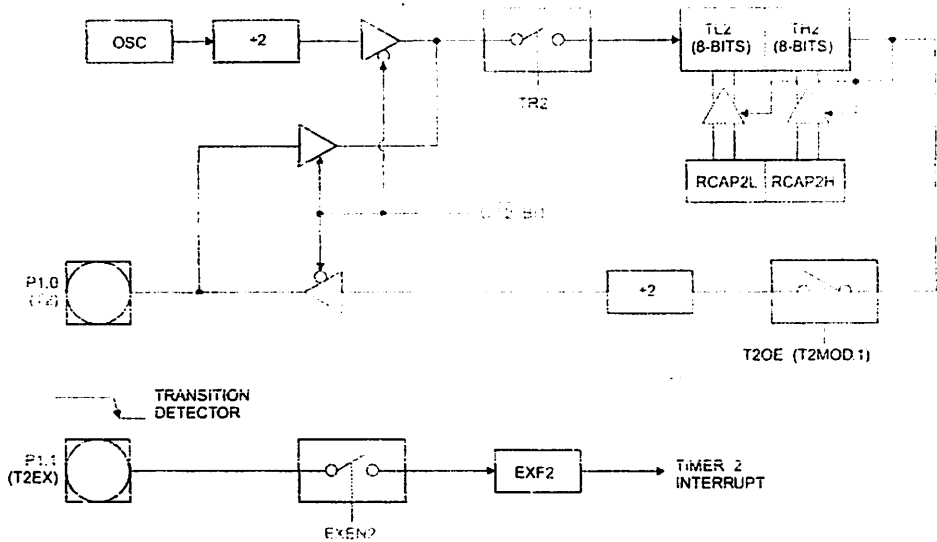
To configure the Timer/Counter 2 as a clock generator, bit $C/\overline{T}2$ (T2CON.1) must be cleared and bit T2OE (T2MOD.1) must be set. Bit TR2 (T2CON.2) starts and stops the timer.

The clock-out frequency depends on the oscillator frequency and the reload value of Timer 2 capture registers (RCAP2H, RCAP2L), as shown in the following equation.

$$\text{Clock-Out Frequency} = \frac{\text{Oscillator Frequency}}{4 \times [65536 - (\text{RCAP2H}, \text{RCAP2L})]}$$

In the clock-out mode, Timer 2 roll-overs will not generate an interrupt. This behavior is similar to when Timer 2 is used as a baud-rate generator. It is possible to use Timer 2 as a baud-rate generator and a clock generator simultaneously. Note, however, that the baud-rate and clock-out frequencies cannot be determined independently from one another since they both use RCAP2H and RCAP2L.

Figure 5. Timer 2 in Clock-Out Mode



Interrupts

The AT89S52 has a total of six interrupt vectors: two external interrupts ($\overline{INT0}$ and $\overline{INT1}$), three timer interrupts (Timers 0, 1, and 2), and the serial port interrupt. These interrupts are all shown in Figure 6.

Each of these interrupt sources can be individually enabled or disabled by setting or clearing a bit in Special Function Register IE. IE also contains a global disable bit, EA, which disables all interrupts at once.

Note that Table 5 shows that bit position IE.6 is unimplemented. User software should not write a 1 to this bit position, since it may be used in future AT89 products.

Timer 2 interrupt is generated by the logical OR of bits TF2 and EXF2 in register T2CON. Neither of these flags is cleared by hardware when the service routine is vectored to. In fact, the service routine may have to determine whether it was TF2 or EXF2 that generated the interrupt, and that bit will have to be cleared in software.

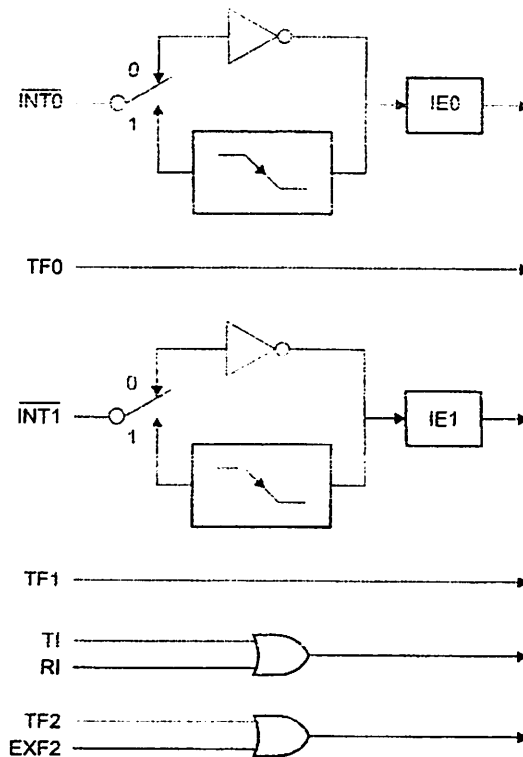
The Timer 0 and Timer 1 flags, TF0 and TF1, are set at S5P2 of the cycle in which the timers overflow. The values are then polled by the circuitry in the next cycle. However, the Timer 2 flag, TF2, is set at S2P2 and is polled in the same cycle in which the timer overflows.

Figure 7. Interrupt Enable (IE) Register

(MSB)		(LSB)					
EA	-	ET2	ES	ET1	EX1	ET0	EX0
Enable Bit = 1 enables the interrupt.							
Enable Bit = 0 disables the interrupt.							
Bit	Position	Function					
	IE.7	Disables all interrupts. If EA = 0, no interrupt is acknowledged. If EA = 1, each interrupt source is individually enabled or disabled by setting or clearing its enable bit.					
	IE.6	Reserved.					
2	IE.5	Timer 2 interrupt enable bit.					
	IE.4	Serial Port interrupt enable bit.					
1	IE.3	Timer 1 interrupt enable bit.					
1	IE.2	External interrupt 1 enable bit.					
0	IE.1	Timer 0 interrupt enable bit.					
0	IE.0	External interrupt 0 enable bit.					

Software should never write 1s to reserved bits, because they may be used in future AT89 products.

Figure 6. Interrupt Sources





Oscillator Characteristics

XTAL1 and XTAL2 are the input and output, respectively, of an inverting amplifier that can be configured for use as an on-chip oscillator, as shown in Figure 7. Either a quartz crystal or ceramic resonator may be used. To drive the device from an external clock source, XTAL2 should be left unconnected while XTAL1 is driven, as shown in Figure 8. There are no requirements on the duty cycle of the external clock signal, since the input to the internal clocking circuitry is through a divide-by-two flip-flop, but minimum and maximum voltage high and low time specifications must be observed.

Idle Mode

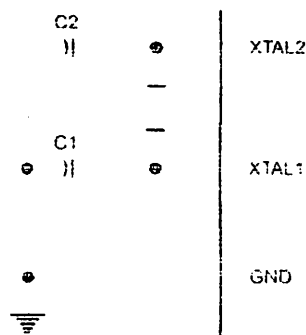
In idle mode, the CPU puts itself to sleep while all the on-chip peripherals remain active. The mode is invoked by software. The content of the on-chip RAM and all the special functions registers remain unchanged during this mode. The idle mode can be terminated by any enabled interrupt or by a hardware reset.

Note that when idle mode is terminated by a hardware reset, the device normally resumes program execution from where it left off, up to two machine cycles before the internal reset algorithm takes control. On-chip hardware inhibits access to internal RAM in this event, but access to the port pins is not inhibited. To eliminate the possibility of an unexpected write to a port pin when idle mode is terminated by a reset, the instruction following the one that invokes idle mode should not write to a port pin or to external memory.

Power-down Mode

In the Power-down mode, the oscillator is stopped, and the instruction that invokes Power-down is the last instruction executed. The on-chip RAM and Special Function Registers retain their values until the Power-down mode is terminated. Exit from Power-down mode can be initiated either by a hardware reset or by an enabled external interrupt. Reset redefines the SFRs but does not change the on-chip RAM. The reset should not be activated before V_{CC} is restored to its normal operating level and must be held active long enough to allow the oscillator to restart and stabilize.

Figure 7. Oscillator Connections



Note: 1. C1, C2 = 30 pF \pm 10 pF for Crystals
= 40 pF \pm 10 pF for Ceramic Resonators

Figure 8. External Clock Drive Configuration

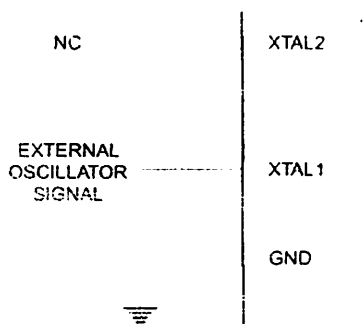


Table 8. Status of External Pins During Idle and Power-down Modes

Mode	Program Memory	ALE	$\overline{\text{PSEN}}$	PORT0	PORT1	PORT2	PORT3
Idle	Internal	1	1	Data	Data	Data	Data
Idle	External	1	1	Float	Data	Address	Data
Power-down	Internal	0	0	Data	Data	Data	Data
Power-down	External	0	0	Float	Data	Data	Data

Program Memory Lock Bits

The AT89S52 has three lock bits that can be left unprogrammed (U) or can be programmed (P) to obtain the additional features listed in the following table.

Table 9. Lock Bit Protection Modes

	Program Lock Bits			Protection Type
	LB1	LB2	LB3	
1	U	U	U	No program lock features
2	P	U	U	MOVC instructions executed from external program memory are disabled from fetching code bytes from internal memory, $\overline{\text{EA}}$ is sampled and latched on reset, and further programming of the Flash memory is disabled
3	P	P	U	Same as mode 2, but verify is also disabled
4	P	P	P	Same as mode 3, but external execution is also disabled

When lock bit 1 is programmed, the logic level at the $\overline{\text{EA}}$ pin is sampled and latched during reset. If the device is powered up without a reset, the latch initializes to a random value and holds that value until reset is activated. The latched value of $\overline{\text{EA}}$ must agree with the current logic level at that pin in order for the device to function properly.



Programming the Flash – Parallel Mode

The AT89S52 is shipped with the on-chip Flash memory array ready to be programmed. The programming interface needs a high-voltage (12-volt) program enable signal and is compatible with conventional third-party Flash or EPROM programmers.

The AT89S52 code memory array is programmed byte-by-byte.

Programming Algorithm: Before programming the AT89S52, the address, data, and control signals should be set up according to the Flash programming mode table and Figures 13 and 14. To program the AT89S52, take the following steps:

1. Input the desired memory location on the address lines.
2. Input the appropriate data byte on the data lines.
3. Activate the correct combination of control signals.
4. Raise \overline{EA}/V_{PP} to 12V.
5. Pulse ALE/\overline{PROG} once to program a byte in the Flash array or the lock bits. The byte-write cycle is self-timed and typically takes no more than 50 μ s. Repeat steps 1 through 5, changing the address and data for the entire array or until the end of the object file is reached.

Data Polling: The AT89S52 features \overline{Data} Polling to indicate the end of a byte write cycle. During a write cycle, an attempted read of the last byte written will result in the complement of the written data on P0.7. Once the write cycle has been completed, true data is valid on all outputs, and the next cycle may begin. \overline{Data} Polling may begin any time after a write cycle has been initiated.

Ready/Busy: The progress of byte programming can also be monitored by the RDY/\overline{BSY} output signal. P3.0 is pulled low after ALE goes high during programming to indicate \overline{BUSY} . P3.0 is pulled high again when programming is done to indicate \overline{READY} .

Program Verify: If lock bits LB1 and LB2 have not been programmed, the programmed code data can be read back via the address and data lines for verification. The status of the individual lock bits can be verified directly by reading them back.

Reading the Signature Bytes: The signature bytes are read by the same procedure as a normal verification of locations 000H, 100H, and 200H, except that P3.6 and P3.7 must be pulled to a logic low. The values returned are as follows.

(000H) = 1EH indicates manufactured by Atmel
(100H) = 52H indicates AT89S52
(200H) = 06H

Chip Erase: In the parallel programming mode, a chip erase operation is initiated by using the proper combination of control signals and by pulsing ALE/\overline{PROG} low for a duration of 200 ns - 500 ns.

In the serial programming mode, a chip erase operation is initiated by issuing the Chip Erase instruction. In this mode, chip erase is self-timed and takes about 500 ms.

During chip erase, a serial read from any address location will return 00H at the data output.

Programming the Shift – Serial Mode

The Code memory array can be programmed using the serial ISP interface while RST is pulled to V_{CC} . The serial interface consists of pins SCK, MOSI (input) and MISO (output). After RST is set high, the Programming Enable instruction needs to be executed first before other operations can be executed. Before a reprogramming sequence can occur, a Chip Erase operation is required.

The Chip Erase operation turns the content of every memory location in the Code array into FFH.

Either an external system clock can be supplied at pin XTAL1 or a crystal needs to be connected across pins XTAL1 and XTAL2. The maximum serial clock (SCK) frequency should be less than 1/16 of the crystal frequency. With a 33 MHz oscillator clock, the maximum SCK frequency is 2 MHz.

Serial Programming Algorithm

To program and verify the AT89S52 in the serial programming mode, the following sequence is recommended:

1. Power-up sequence:
 - Apply power between VCC and GND pins.
 - Set RST pin to "H".
 - If a crystal is not connected across pins XTAL1 and XTAL2, apply a 3 MHz to 33 MHz clock to XTAL1 pin and wait for at least 10 milliseconds.
2. Enable serial programming by sending the Programming Enable serial instruction to pin MOSI/P1.5. The frequency of the shift clock supplied at pin SCK/P1.7 needs to be less than the CPU clock at XTAL1 divided by 16.
3. The Code array is programmed one byte at a time in either the Byte or Page mode. The write cycle is self-timed and typically takes less than 0.5 ms at 5V.
4. Any memory location can be verified by using the Read instruction which returns the content at the selected address at serial output MISO/P1.6.
5. At the end of a programming session, RST can be set low to commence normal device operation.

Power-off sequence (if needed):

- Set XTAL1 to "L" (if a crystal is not used).
- Set RST to "L".
- Turn V_{CC} power off.

Data Polling: The $\overline{\text{Data}}$ Polling feature is also available in the serial mode. In this mode, during a write cycle an attempted read of the last byte written will result in the complement of the MSB of the serial output byte on MISO.



Serial Programming Instruction Set

The Instruction Set for Serial Programming follows a 4-byte protocol and is shown in Table 11.

Programming Interface – Parallel Mode

Every code byte in the Flash array can be programmed by using the appropriate combination of control signals. The write operation cycle is self-timed and once initiated, will automatically time itself to completion.

Most worldwide major programming vendors offer support for the Atmel AT89 microcontroller series. Please contact your local programming vendor for the appropriate software revision.

Table 10. Flash Programming Modes

Mode	V _{CC}	RST	PSEN	ALE/ PROG	EA/ V _{PP}	P2.6	P2.7	P3.3	P3.6	P3.7	P0.7-0 Data	P2.4-0	P1.7-0
												Address	
Write Code Data	5V	H	L	(2)	12V	L	H	H	H	H	D _{IN}	A12-8	A7-0
Read Code Data	5V	H	L	H	H	L	L	L	H	H	D _{OUT}	A12-8	A7-0
Write Lock Bit 1	5V	H	L	(3)	12V	H	H	H	H	H	X	X	X
Write Lock Bit 2	5V	H	L	(3)	12V	H	H	H	L	L	X	X	X
Write Lock Bit 3	5V	H	L	(3)	12V	H	L	H	H	L	X	X	X
Read Lock Bits 1, 2, 3	5V	H	L	H	H	H	H	L	H	L	P0.2, P0.3, P0.4	X	X
Chip Erase	5V	H	L	(1)	12V	H	L	H	L	L	X	X	X
Read Atmel ID	5V	H	L	H	H	L	L	L	L	L	1EH	X 0000	00H
Read Device ID	5V	H	L	H	H	L	L	L	L	L	52H	X 0001	00H
Read Device ID	5V	H	L	H	H	L	L	L	L	L	06H	X 0010	00H

- Notes:
1. Each **PROG** pulse is 200 ns - 500 ns for Chip Erase.
 2. Each **PROG** pulse is 200 ns - 500 ns for Write Code Data.
 3. Each **PROG** pulse is 200 ns - 500 ns for Write Lock Bits.
 4. RDY/BSY signal is output on P3.0 during programming.
 5. X = don't care.

Figure 9. Programming the Flash Memory (Parallel Mode)

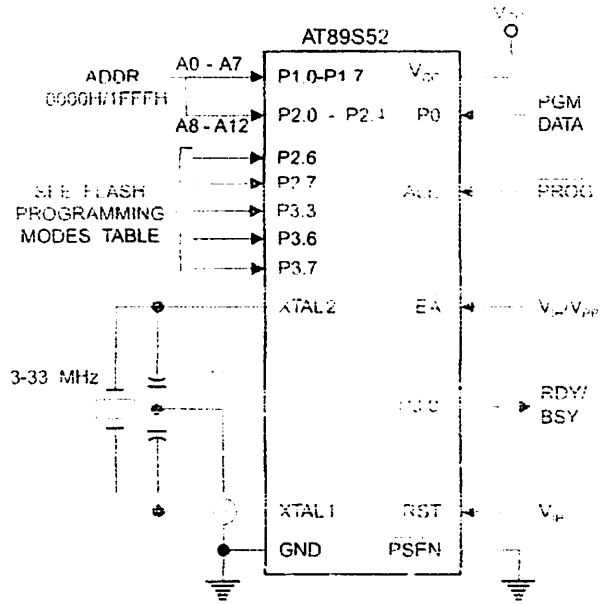
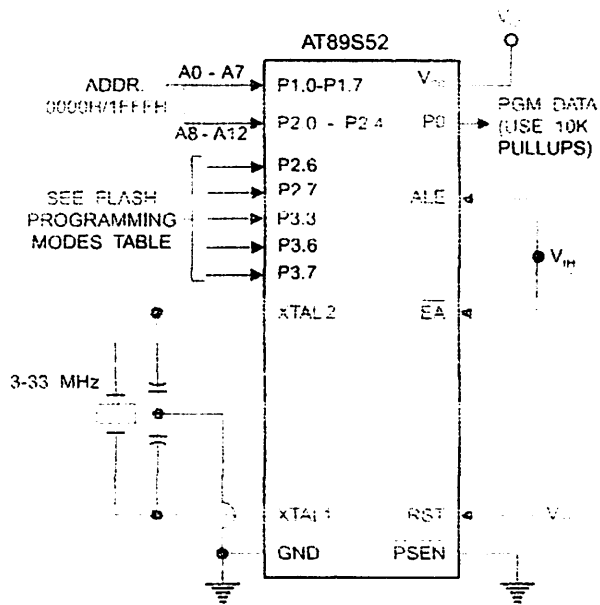


Figure 10. Verifying the Flash Memory (Parallel Mode)





Flash Programming and Verification Characteristics (Parallel Mode)

$T_A = 20^\circ\text{C to } 30^\circ\text{C}, V_{CC} = 4.5 \text{ to } 5.5\text{V}$

Symbol	Parameter	Min	Max	Units
V_{PP}	Programming Supply Voltage	11.5	12.5	V
I_{PP}	Programming Supply Current		10	mA
I_{CC}	V_{CC} Supply Current		30	mA
$1/t_{CLCL}$	Oscillator Frequency	3	33	MHz
t_{AVGL}	Address Setup to $\overline{\text{PROG}}$ Low	$48t_{CLCL}$		
t_{GHAX}	Address Hold After $\overline{\text{PROG}}$	$48t_{CLCL}$		
t_{DVGL}	Data Setup to $\overline{\text{PROG}}$ Low	$48t_{CLCL}$		
t_{GHDX}	Data Hold After $\overline{\text{PROG}}$	$46t_{CLCL}$		
t_{EHS}	P2.7 ($\overline{\text{ENABLE}}$) High to V_{PP}	$48t_{CLCL}$		
t_{SHGL}	V_{PP} Setup to $\overline{\text{PROG}}$ Low	10		μs
t_{GHSL}	V_{PP} Hold After $\overline{\text{PROG}}$	10		μs
t_{GLGH}	$\overline{\text{PROG}}$ Width	0.2	1	μs
t_{AVQV}	Address to Data Valid		$48t_{CLCL}$	
t_{ELQV}	$\overline{\text{ENABLE}}$ Low to Data Valid		$48t_{CLCL}$	
t_{EHQZ}	Data Float After $\overline{\text{ENABLE}}$	0	$48t_{CLCL}$	
t_{GHBL}	$\overline{\text{PROG}}$ High to $\overline{\text{BUSY}}$ Low		1.0	μs
t_{WC}	Byte Write Cycle Time		50	μs

Figure 11. Flash Programming and Verification Waveforms – Parallel Mode

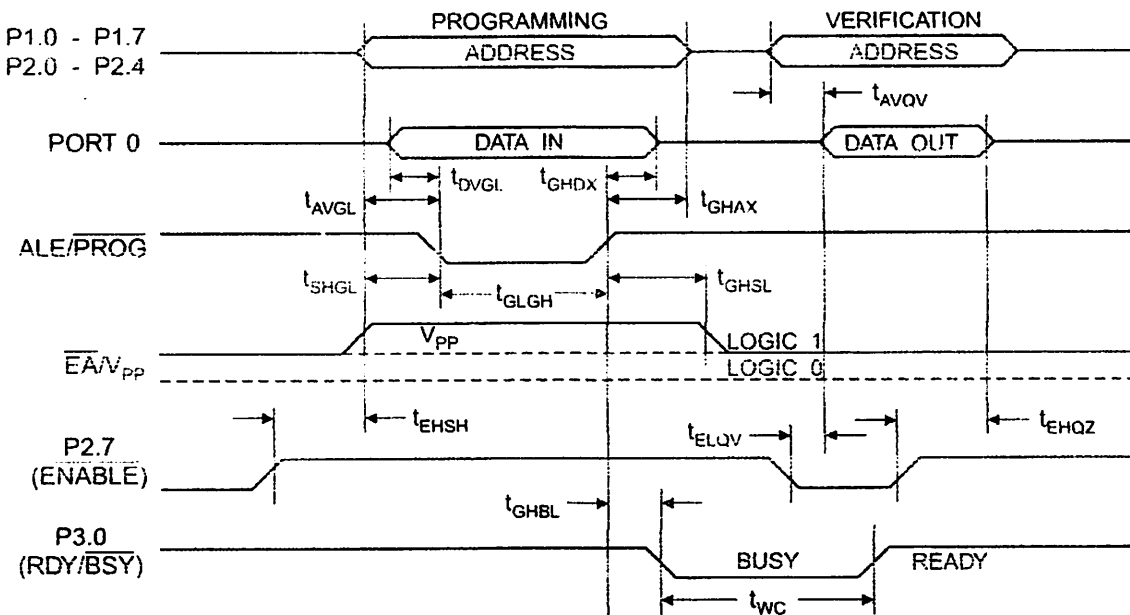
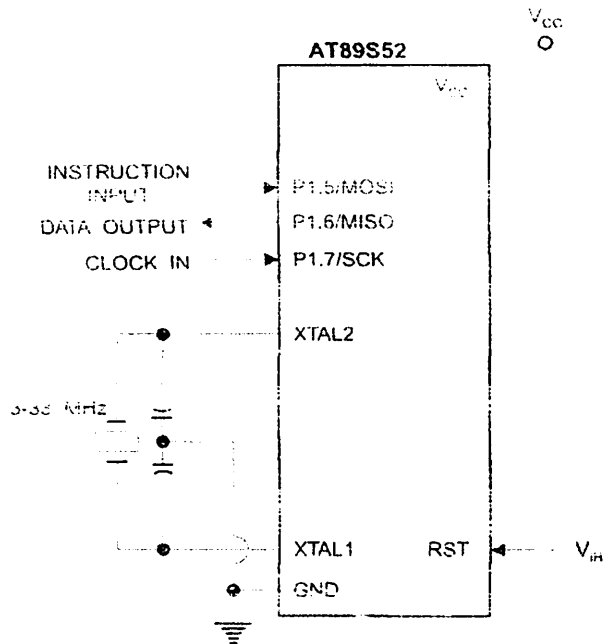


Figure 12. Flash Memory Serial Downloading



Flash Programming
 Verification
 Waveforms – Serial
 Mode

Figure 13. Serial Programming Waveforms

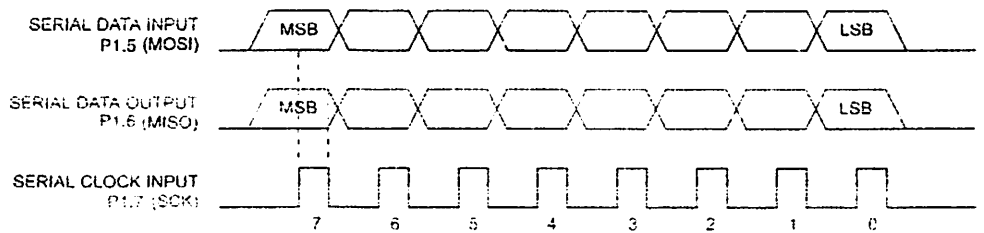




Table 11. Serial Programming Instruction Set

Instruction	Instruction Format				Operation
	Byte 1	Byte 2	Byte 3	Byte 4	
Programming Enable	1010 1100	0101 0011	xxxx xxxx	xxxx xxxx 0110 1001 (Output on MISO)	Enable Serial Programming while RST is high
Chip Erase	1010 1100	100x xxxx	xxxx xxxx	xxxx xxxx	Chip Erase Flash memory array
Read Program Memory (Byte Mode)	0010 0000	xxx A12 A11 A10 A9 A8	A7 A6 A5 A4 A3 A2 A1 A0	D7 D6 D5 D4 D3 D2 D1 D0	Read data from Program memory in the byte mode
Write Program Memory (Byte Mode)	0100 0000	xxx A12 A11 A10 A9 A8	A7 A6 A5 A4 A3 A2 A1 A0	7 6 5 4 3 2 1 0 DDDD DD	Write data to Program memory in the byte mode
Write Lock Bits ⁽¹⁾	1010 1100	1110 00 BB2	xxxx xxxx	xxxx xxxx	Write Lock bits. See Note (1).
Read Lock Bits	0010 0100	xxxx xxxx	xxxx xxxx	xxx LB3 LB2 LB1 xx	Read back current status of the lock bits (a programmed lock bit reads back as a "1")
Read Signature Bytes	0010 1000	xxx A12 A11 A10 A9 A8	A7 xxx xxx0	Signature Byte	Read Signature Byte
Read Program Memory (Page Mode)	0011 0000	xxx A12 A11 A10 A9 A8	Byte 0	Byte 1... Byte 255	Read data from Program memory in the Page Mode (256 bytes)
Write Program Memory (Page Mode)	0101 0000	xxx A12 A11 A10 A9 A8	Byte 0	Byte 1... Byte 255	Write data to Program memory in the Page Mode (256 bytes)

Note: 1. B1 = 0, B2 = 0 → Mode 1, no lock protection
 B1 = 0, B2 = 1 → Mode 2, lock bit 1 activated
 B1 = 1, B2 = 0 → Mode 3, lock bit 2 activated
 B1 = 1, B2 = 1 → Mode 4, lock bit 3 activated

Each of the lock bit modes needs to be activated sequentially before Mode 4 can be executed.

After Reset signal is high, SCK should be low for at least 64 system clocks before it goes high to clock in the enable data bytes. No pulsing of Reset signal is necessary. SCK should be no faster than 1/16 of the system clock at XTAL1.

For Page Read/Write, the data always starts from byte 0 to 255. After the command byte and upper address byte are latched, each byte thereafter is treated as data until all 256 bytes are shifted in/out. Then the next instruction will be ready to be decoded.

Serial Programming Characteristics

Figure 14. Serial Programming Timing

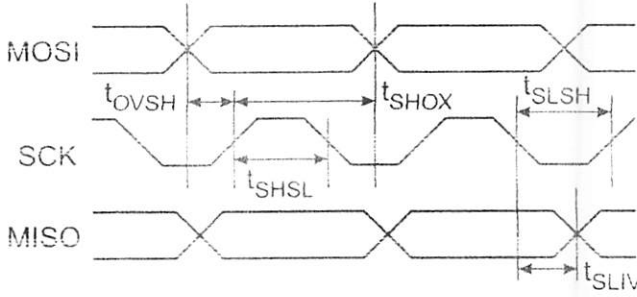


Table 12. Serial Programming Characteristics, $T_A = -40^\circ\text{C}$ to 85°C , $V_{CC} = 4.0 - 5.5\text{V}$ (Unless Otherwise Noted)

Symbol	Parameter	Min	Typ	Max	Units
f_{CLCL}	Oscillator Frequency	3		33	MHz
t_{CLCL}	Oscillator Period	30			ns
t_{GL}	SCK Pulse Width High	$8 t_{CLCL}$			ns
t_{HL}	SCK Pulse Width Low	$8 t_{CLCL}$			ns
t_{SH}	MOSI Setup to SCK High	t_{CLCL}			ns
t_{SOX}	MOSI Hold after SCK High	$2 t_{CLCL}$			ns
t_{SLV}	SCK Low to MISO Valid	10	16	32	ns
t_{ASE}	Chip Erase Instruction Cycle Time			500	ms
t_{C}	Serial Byte Write Cycle Time			$64 t_{CLCL} + 400$	μs



Absolute Maximum Ratings*

Operating Temperature.....	-55°C to +125°C
Storage Temperature.....	-65°C to +150°C
Voltage on Any Pin with Respect to Ground.....	-1.0V to +7.0V
Maximum Operating Voltage.....	6.6V
DC Output Current.....	15.0 mA

*NOTICE: Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC Characteristics

The values shown in this table are valid for $T_A = -40^\circ\text{C}$ to 85°C and $V_{CC} = 4.0\text{V}$ to 5.5V , unless otherwise noted.

Symbol	Parameter	Condition	Min	Max	Units
V_{IL}	Input Low Voltage	(Except \overline{EA})	-0.5	$0.2 V_{CC}-0.1$	V
V_{IL1}	Input Low Voltage (\overline{EA})		-0.5	$0.2 V_{CC}-0.3$	V
V_{IH}	Input High Voltage	(Except XTAL1, RST)	$0.2 V_{CC}+0.9$	$V_{CC}+0.5$	V
V_{IH1}	Input High Voltage	(XTAL1, RST)	$0.7 V_{CC}$	$V_{CC}+0.5$	V
V_{OL}	Output Low Voltage ⁽¹⁾ (Ports 1,2,3)	$I_{OL} = 1.6 \text{ mA}$		0.45	V
V_{OL1}	Output Low Voltage ⁽¹⁾ (Port 0, ALE, PSEN)	$I_{OL} = 3.2 \text{ mA}$		0.45	V
V_{OH}	Output High Voltage (Ports 1,2,3, ALE, PSEN)	$I_{OH} = -60 \mu\text{A}, V_{CC} = 5\text{V} \pm 10\%$	2.4		V
		$I_{OH} = -25 \mu\text{A}$	$0.75 V_{CC}$		V
		$I_{OH} = -10 \mu\text{A}$	$0.9 V_{CC}$		V
V_{OH1}	Output High Voltage (Port 0 in External Bus Mode)	$I_{OH} = -800 \mu\text{A}, V_{CC} = 5\text{V} \pm 10\%$	2.4		V
		$I_{OH} = -300 \mu\text{A}$	$0.75 V_{CC}$		V
		$I_{OH} = -80 \mu\text{A}$	$0.9 V_{CC}$		V
I_{IL}	Logical 0 Input Current (Ports 1,2,3)	$V_{IN} = 0.45\text{V}$		-50	μA
I_{TL}	Logical 1 to 0 Transition Current (Ports 1,2,3)	$V_{IN} = 2\text{V}, V_{CC} = 5\text{V} \pm 10\%$		-650	μA
I_{LI}	Input Leakage Current (Port 0, \overline{EA})	$0.45 < V_{IN} < V_{CC}$		± 10	μA
RRST	Reset Pulldown Resistor		50	300	K Ω
C_{IO}	Pin Capacitance	Test Freq. = 1 MHz, $T_A = 25^\circ\text{C}$		10	pF
I_{CC}	Power Supply Current	Active Mode, 12 MHz		25	mA
		Idle Mode, 12 MHz		6.5	mA
	Power-down Mode ⁽¹⁾	$V_{CC} = 5.5\text{V}$		50	μA

Notes: 1. Under steady state (non-transient) conditions, I_{OL} must be externally limited as follows:

Maximum I_{OL} per port pin: 10 mA

Maximum I_{OL} per 8-bit port:

Port 0: 26 mA Ports 1, 2, 3: 15 mA

Maximum total I_{OL} for all output pins: 71 mA

If I_{OL} exceeds the test condition, V_{OL} may exceed the related specification. Pins are not guaranteed to sink current greater than the listed test conditions.

2. Minimum V_{CC} for Power-down is 2V.

Characteristics

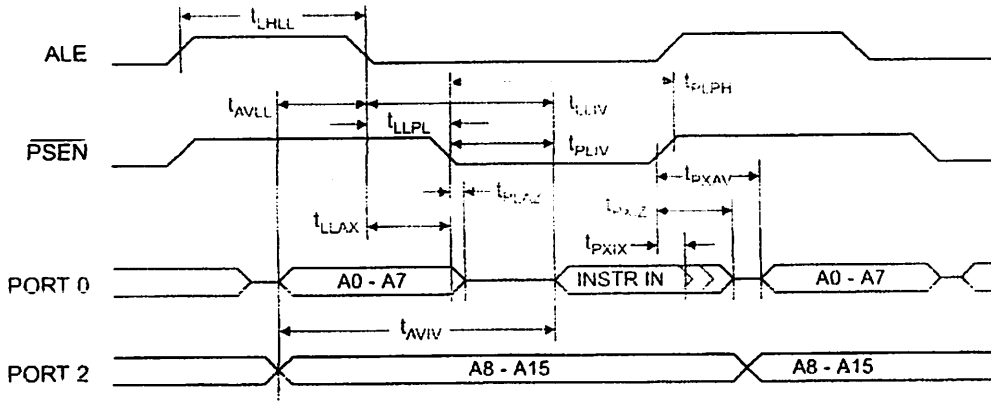
Under operating conditions, load capacitance for Port 0, ALE/PROG, and PSEN = 100 pF; load capacitance for all other ports = 80 pF.

Internal Program and Data Memory Characteristics

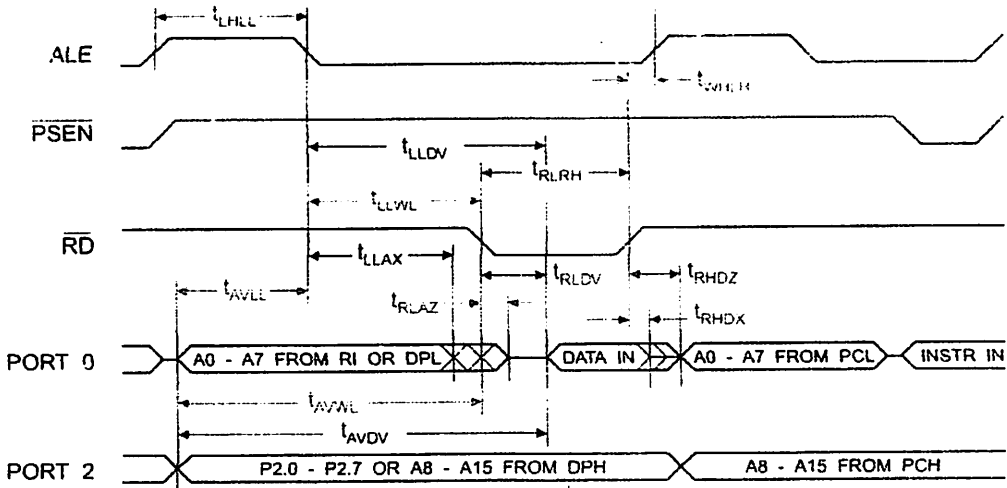
Symbol	Parameter	12 MHz Oscillator		Variable Oscillator		Units
		Min	Max	Min	Max	
f _{OSC}	Oscillator Frequency			0	33	MHz
t _{PL}	ALE Pulse Width	127		2t _{CLCL} -40		ns
t _{VL}	Address Valid to ALE Low	43		t _{CLCL} -25		ns
t _{HL}	Address Hold After ALE Low	48		t _{CLCL} -25		ns
t _{PLV}	ALE Low to Valid Instruction In		233		4t _{CLCL} -65	ns
t _{PLP}	ALE Low to PSEN Low	43		t _{CLCL} -25		ns
t _{PH}	PSEN Pulse Width	205		3t _{CLCL} -45		ns
t _{PLV}	PSEN Low to Valid Instruction In		145		3t _{CLCL} -60	ns
t _{PLX}	Input Instruction Hold After PSEN	0		0		ns
t _{PLZ}	Input Instruction Float After PSEN		59		t _{CLCL} -25	ns
t _{PLV}	PSEN to Address Valid	75		t _{CLCL} -8		ns
t _{PLV}	Address to Valid Instruction In		312		5t _{CLCL} -80	ns
t _{PLZ}	PSEN Low to Address Float		10		10	ns
t _{PH}	RD Pulse Width	400		6t _{CLCL} -100		ns
t _{PH}	WR Pulse Width	400		6t _{CLCL} -100		ns
t _{PLV}	RD Low to Valid Data In		252		5t _{CLCL} -90	ns
t _{PLX}	Data Hold After RD	0		0		ns
t _{PLZ}	Data Float After RD		97		2t _{CLCL} -28	ns
t _{PLV}	ALE Low to Valid Data In		517		8t _{CLCL} -150	ns
t _{PLV}	Address to Valid Data In		585		9t _{CLCL} -165	ns
t _{PL}	ALE Low to RD or WR Low	200	300	3t _{CLCL} -50	3t _{CLCL} +50	ns
t _{PL}	Address to RD or WR Low	203		4t _{CLCL} -75		ns
t _{PLX}	Data Valid to WR Transition	23		t _{CLCL} -30		ns
t _{PLWH}	Data Valid to WR High	433		7t _{CLCL} -130		ns
t _{PLQX}	Data Hold After WR	33		t _{CLCL} -25		ns
t _{PLAZ}	RD Low to Address Float		0		0	ns
t _{PLH}	RD or WR High to ALE High	43	123	t _{CLCL} -25	t _{CLCL} +25	ns



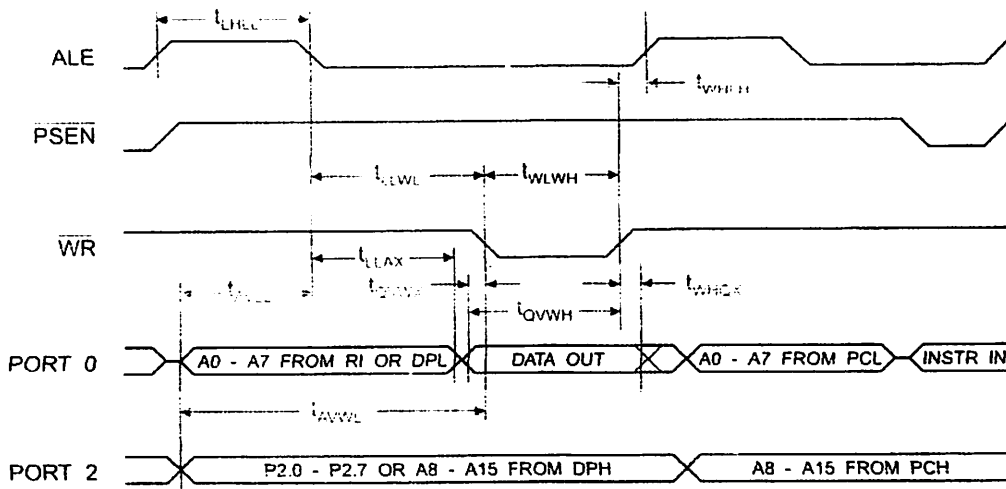
External Program Memory Read Cycle



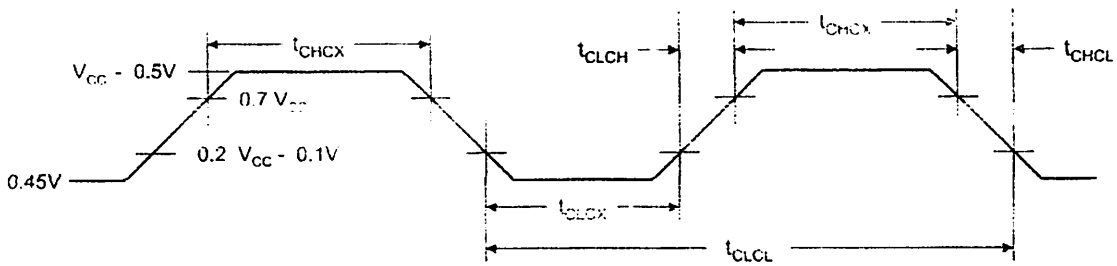
External Data Memory Read Cycle



Internal Data Memory Write Cycle



Internal Clock Drive Waveforms



Internal Clock Drive

Symbol	Parameter	Min	Max	Units
f _{CL}	Oscillator Frequency	0	33	MHz
T _{CL}	Clock Period	30		ns
t _{CHX}	High Time	12		ns
t _{CLX}	Low Time	12		ns
t _{CH}	Rise Time		5	ns
t _{CL}	Fall Time		5	ns

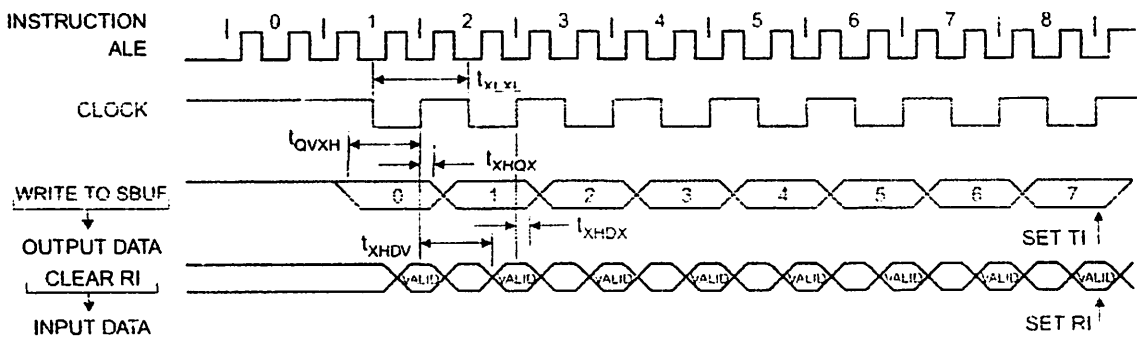


Serial Port Timing: Shift Register Mode Test Conditions

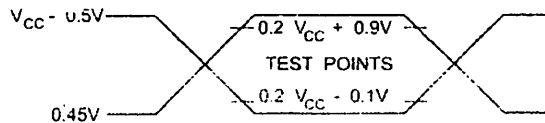
The values in this table are valid for $V_{CC} = 4.0V$ to $5.5V$ and Load Capacitance = 80 pF .

Symbol	Parameter	12 MHz Osc		Variable Oscillator		Units
		Min	Max	Min	Max	
t_{XLXL}	Serial Port Clock Cycle Time	1.0		$12t_{CLCL}$		μs
t_{QVXH}	Output Data Setup to Clock Rising Edge	700		$10t_{CLCL} - 133$		ns
t_{XHGX}	Output Data Hold After Clock Rising Edge	50		$2t_{CLCL} - 80$		ns
t_{XHDX}	Input Data Hold After Clock Rising Edge	0		0		ns
t_{XHGV}	Clock Rising Edge to Input Data Valid		700		$10t_{CLCL} - 133$	ns

Shift Register Mode Timing Waveforms

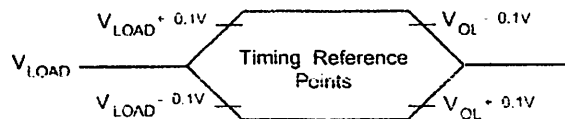


AC Testing Input/Output Waveforms⁽¹⁾



- Note: 1. AC Inputs during testing are driven at $V_{CC} - 0.5V$ for a logic 1 and $0.45V$ for a logic 0. Timing measurements are made at V_{IH} min. for a logic 1 and V_{IL} max. for a logic 0.

Float Waveforms⁽¹⁾



- Note: 1. For timing purposes, a port pin is no longer floating when a 100 mV change from load voltage occurs. A port pin begins to float when a 100 mV change from the loaded V_{OH}/V_{OL} level occurs.

Ordering Information

Speed (MHz)	Power Supply	Ordering Code	Package	Operation Range
24	4.0V to 5.5V	AT89S52-24AC	44A	Commercial (0° C to 70° C)
		AT89S52-24JC	44J	
		AT89S52-24PC	40P6	
		AT89S52-24SC	42PS6	
	4.5V to 5.5V	AT89S52-24AI	44A	Industrial (-40° C to 85° C)
		AT89S52-24JI	44J	
		AT89S52-24PI	40P6	
		AT89S52-24SI	42PS6	
33	4.5V to 5.5V	AT89S52-33AC	44A	Commercial (0° C to 70° C)
		AT89S52-33JC	44J	
		AT89S52-33PC	40P6	
		AT89S52-33SC	42PS6	

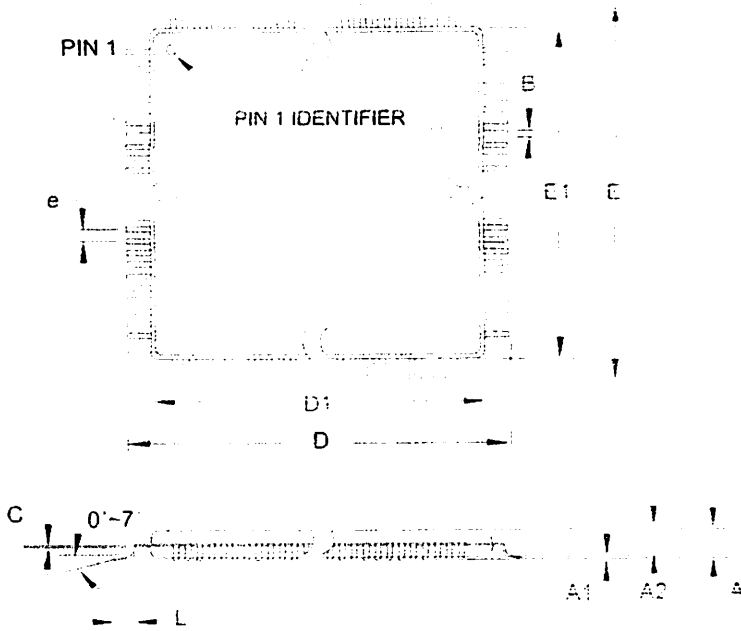
Package Type	
44	44-lead, Thin Plastic Gull Wing Quad Flatpack (TQFP)
44	44-lead, Plastic J-leaded Chip Carrier (PLCC)
40P6	40-pin, 0.600" Wide, Plastic Dual Inline Package (PDIP)
42PS6	42-pin, 0.600" Wide, Plastic Dual Inline Package (PDIP)





Packaging Information

44A – TQFP



COMMON DIMENSIONS
(Unit of Measure = mm)

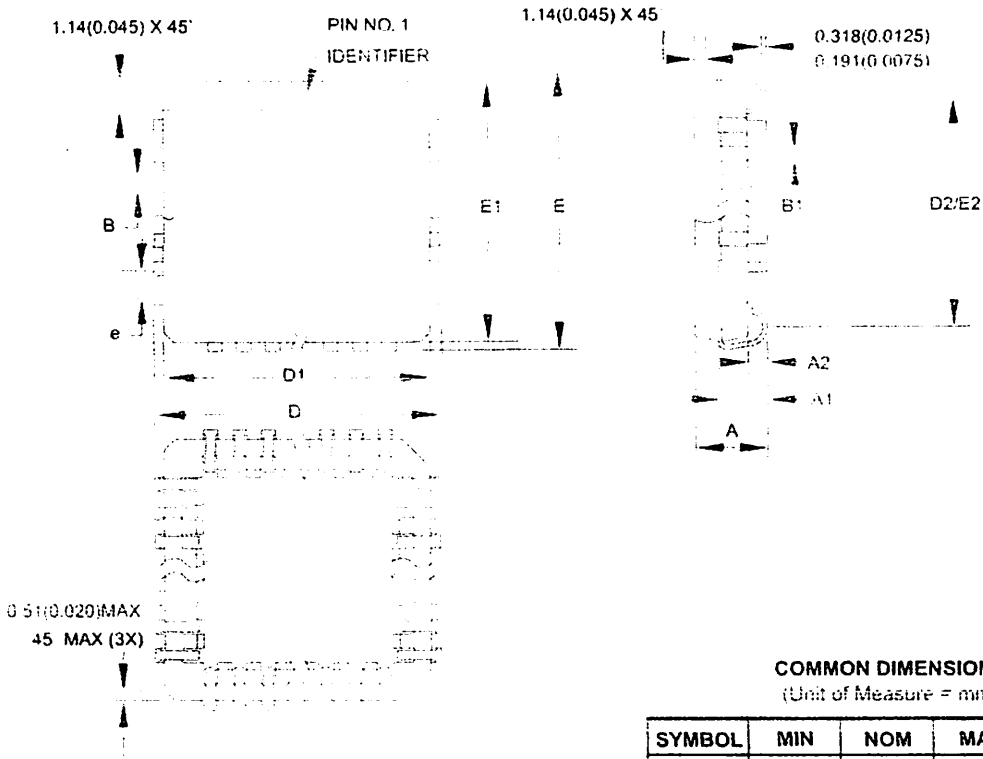
SYMBOL	MIN	NOM	MAX	NOTE
A	-	-	1.20	
A1	0.95		0.15	
A2	0.95	1.00	1.05	
D	11.75	12.00	12.25	
D1	9.90	10.00	10.10	Note 2
E	11.75	12.00	12.25	
E1	9.90	10.00	10.10	Note 2
B	0.30	-	0.45	
C	0.09	-	0.20	
L	0.45	-	0.75	
e	0.80 TYP			

- Notes:
1. This package conforms to JEDEC reference MS-026, Variation ACB.
 2. Dimensions D1 and E1 do not include mold protrusion. Allowable protrusion is 0.25 mm per side. Dimensions D1 and E1 are maximum plastic body size dimensions including mold mismatch.
 3. Lead coplanarity is 0.10 mm maximum.

10/5/2001

2325 Orchard Parkway San Jose, CA 95131	TITLE	DRAWING NO.	REV.
	44A, 44-lead, 10 x 10 mm Body Size, 1.0 mm Body Thickness, 0.8 mm Lead Pitch, Thin Profile Plastic Quad Flat Package (TQFP)	44A	B

- PLCC



COMMON DIMENSIONS
(Unit of Measure = mm)

SYMBOL	MIN	NOM	MAX	NOTE
A	4.191	-	4.572	
A1	2.266	-	3.048	
A2	0.508	-	-	
D	17.399	-	17.653	
D1	16.510	-	16.662	Note 2
E	17.399	-	17.653	
E1	16.510	-	16.662	Note 2
D2/E2	14.986	-	16.002	
B	0.660	-	0.813	
B1	0.330	-	0.533	
e	1.270 TYP			

- Notes:
1. This package conforms to JEDEC reference MS-018, Variation AC.
 2. Dimensions D1 and E1 do not include mold protrusion. Allowable protrusion is .010" (0.254 mm) per side. Dimension D1 and E1 include mold mismatch and are measured at the extreme material condition at the upper or lower parting line.
 3. Lead coplanarity is 0.004" (0.102 mm) maximum.

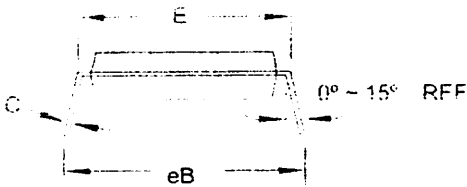
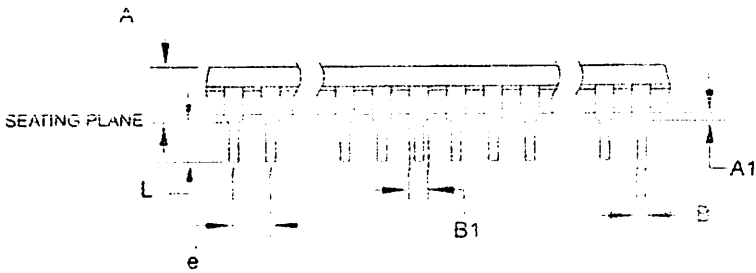
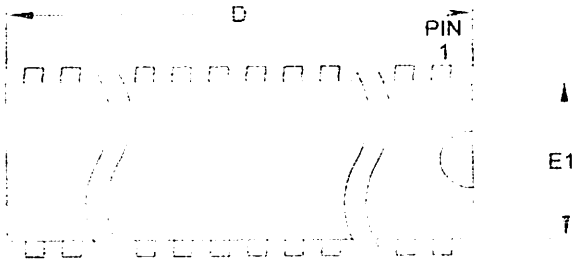
10/04/01

	2325 Orchard Parkway San Jose, CA 95131	TITLE 44J, 44-lead, Plastic J-leaded Chip Carrier (PLCC)	DRAWING NO. 44J	REV. B





40P6 – PDIP



COMMON DIMENSIONS
(Unit of Measure = mm)

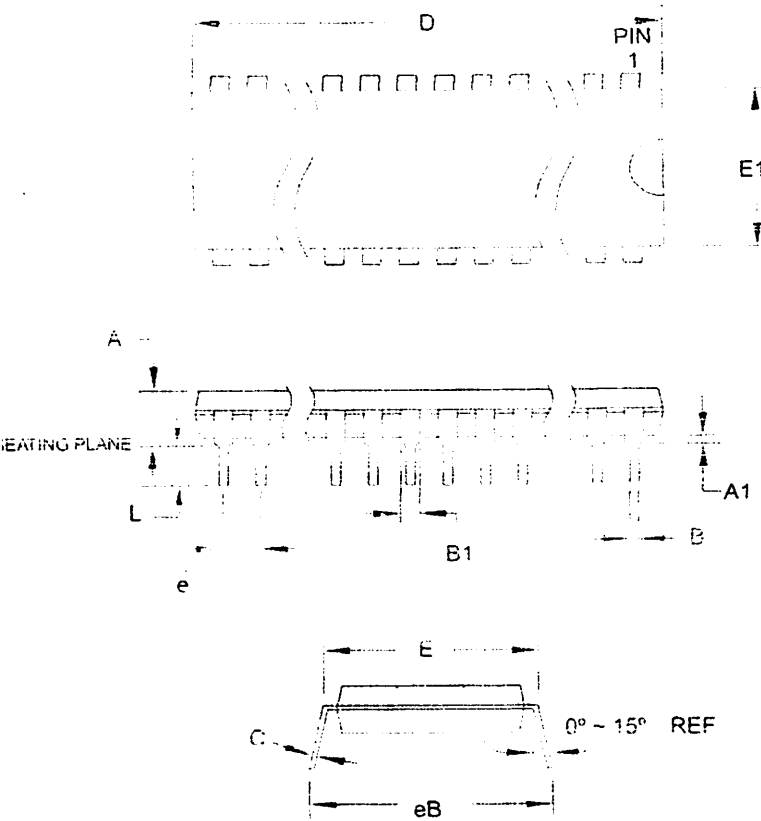
SYMBOL	MIN	NOM	MAX	NOTE
A	-	-	4.826	
A1	0.381	-	-	
D	52.070	-	52.578	Note 2
E	15.240	-	15.875	
E1	13.462	-	13.970	Note 2
B	0.356	-	0.559	
B1	1.041	-	1.651	
L	3.048	-	3.556	
C	0.203	-	0.381	
eB	15.494	-	17.526	
e	2.540 TYP			

- Notes:
1. This package conforms to JEDEC reference MS-011, Variation AC.
 2. Dimensions D and E1 do not include mold Flash or Protrusion. Mold Flash or Protrusion shall not exceed 0.25 mm (0.010").

09/28/01

2325 Orchard Parkway San Jose, CA 95131	TITLE 40P6, 40-lead (0.600"/15.24 mm Wide) Plastic Dual Inline Package (PDIP)	DRAWING NO.	REV.
		40P6	B

PS6 – PDIP



COMMON DIMENSIONS
(Unit of Measure = mm)

SYMBOL	MIN	NOM	MAX	NOTE
A	-	-	4.83	
A1	0.51	-	-	
D	36.70	-	36.96	Note 2
E	15.24	-	15.88	
E1	13.48	-	13.97	Note 2
B	0.38	-	0.56	
B1	0.76	-	1.27	
L	3.05	-	3.43	
C	0.20	-	0.30	
eB	-	-	18.55	
e	1.78 TYP			

- Notes:
1. This package conforms to JEDEC reference MS-011, Variation AC.
 2. Dimensions D and E1 do not include mold Flash or Protrusion. Mold Flash or Protrusion shall not exceed 0.25 mm (0.010").

11/6/03

2325 Orchard Parkway San Jose, CA 95131	TITLE 42PS6, 42-lead (0.600"/15.24 mm Wide) Plastic Dual Inline Package (PDIP)	DRAWING NO.	REV.
		42PS6	A



Atmel Corporation

2325 Orchard Parkway
San Jose, CA 95131, USA
Tel: 1(408) 441-0311
Fax: 1(408) 487-2600

Regional Headquarters

Europe

Atmel Sarl
Route des Arsenaux 41
Case Postale 80
CH-1705 Fribourg
Switzerland
Tel: (41) 26-426-5555
Fax: (41) 26-426-5500

Asia

Room 1219
Chinachem Golden Plaza
77 Mody Road Tsimshatsui
East Kowloon
Hong Kong
Tel: (852) 2721-9778
Fax: (852) 2722-1369

Japan

9F, Tonetsu Shinkawa Bldg.
1-24-8 Shinkawa
Chuo-ku, Tokyo 104-0033
Japan
Tel: (81) 3-3523-3551
Fax: (81) 3-3523-7581

Atmel Operations

Memory

2325 Orchard Parkway
San Jose, CA 95131, USA
Tel: 1(408) 441-0311
Fax: 1(408) 436-4314

Microcontrollers

2325 Orchard Parkway
San Jose, CA 95131, USA
Tel: 1(408) 441-0311
Fax: 1(408) 436-4314

La Chanterrie
BP 70602
44306 Nantes Cedex 3, France
Tel: (33) 2-40-18-18-18
Fax: (33) 2-40-18-19-60

ASIC/ASSP/Smart Cards

Zone Industrielle
13106 Rousset Cedex, France
Tel: (33) 4-42-53-60-00
Fax: (33) 4-42-53-60-01

1150 East Cheyenne Mtn. Blvd.
Colorado Springs, CO 80906, USA
Tel: 1(719) 576-3300
Fax: 1(719) 540-1759

Scottish Enterprise Technology Park
Maxwell Building
East Kilbride G75 0QR, Scotland
Tel: (44) 1355-803-000
Fax: (44) 1355-242-743

RF/Automotive

Theresienstrasse 2
Postfach 3535
74025 Heilbronn, Germany
Tel: (49) 71-31-67-0
Fax: (49) 71-31-67-2340

1150 East Cheyenne Mtn. Blvd.
Colorado Springs, CO 80906, USA
Tel: 1(719) 576-3300
Fax: 1(719) 540-1759

Biometrics/Imaging/Hi-Rel MPU/ High Speed Converters/RF Datacom

Avenue de Rochepleine
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38521 Saint-Egreve Cedex, France
Tel: (33) 4-76-58-30-00
Fax: (33) 4-76-58-34-80

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1919B-MICRO-11/03



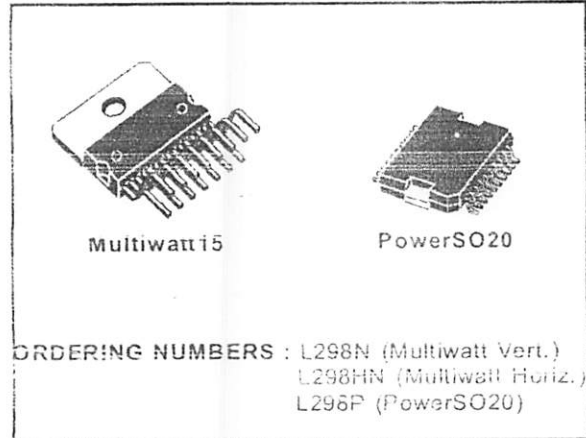
L298

DUAL FULL-BRIDGE DRIVER

- OPERATING SUPPLY VOLTAGE UP TO 46 V
- TOTAL DC CURRENT UP TO 4 A
- LOW SATURATION VOLTAGE
- OVERTEMPERATURE PROTECTION
- LOGICAL "0" INPUT VOLTAGE UP TO 1.5 V (HIGH NOISE IMMUNITY)

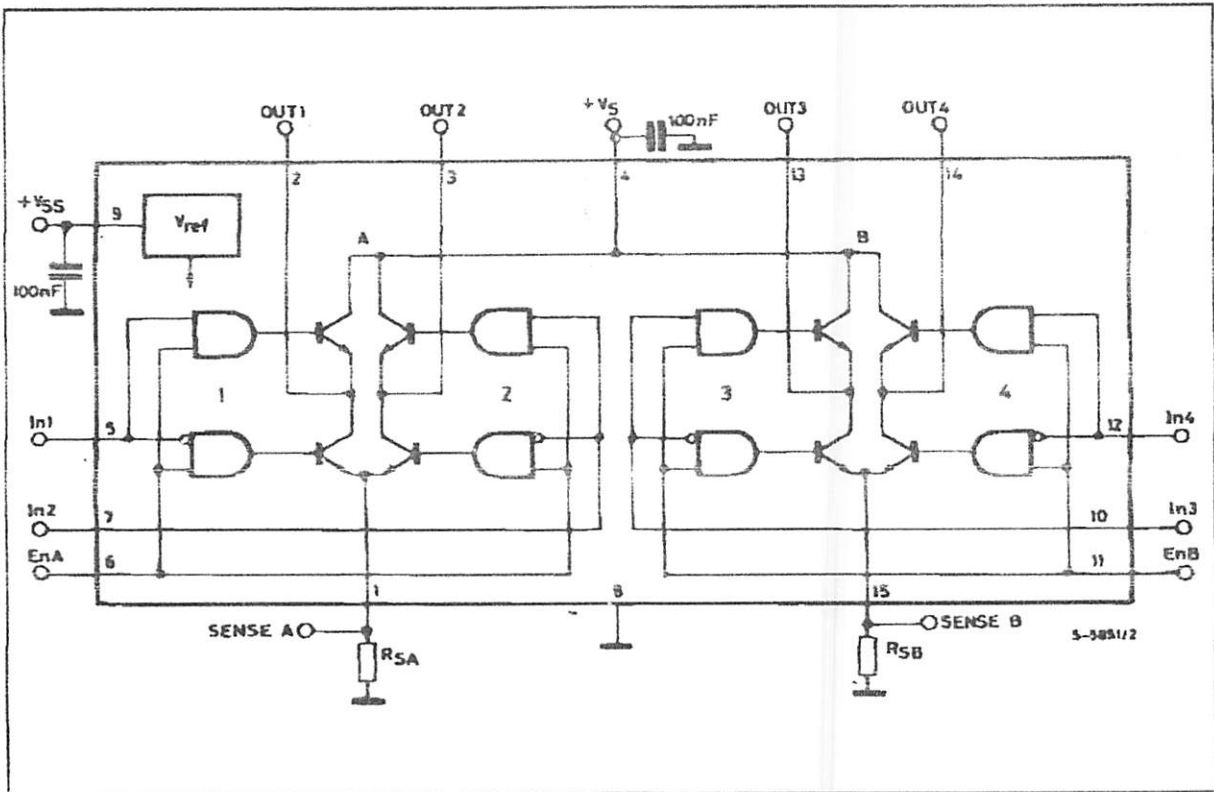
DESCRIPTION

The L298 is an integrated monolithic circuit in a 15-lead Multiwatt and PowerSO20 packages. It is a high voltage, high current dual full-bridge driver designed to accept standard TTL logic levels and drive inductive loads such as relays, solenoids, DC and stepping motors. Two enable inputs are provided to enable or disable the device independently of the input signals. The emitters of the lower transistors of each bridge are connected together and the corresponding external terminal can be used for the con-



nection of an external sensing resistor. An additional supply input is provided so that the logic works at a lower voltage.

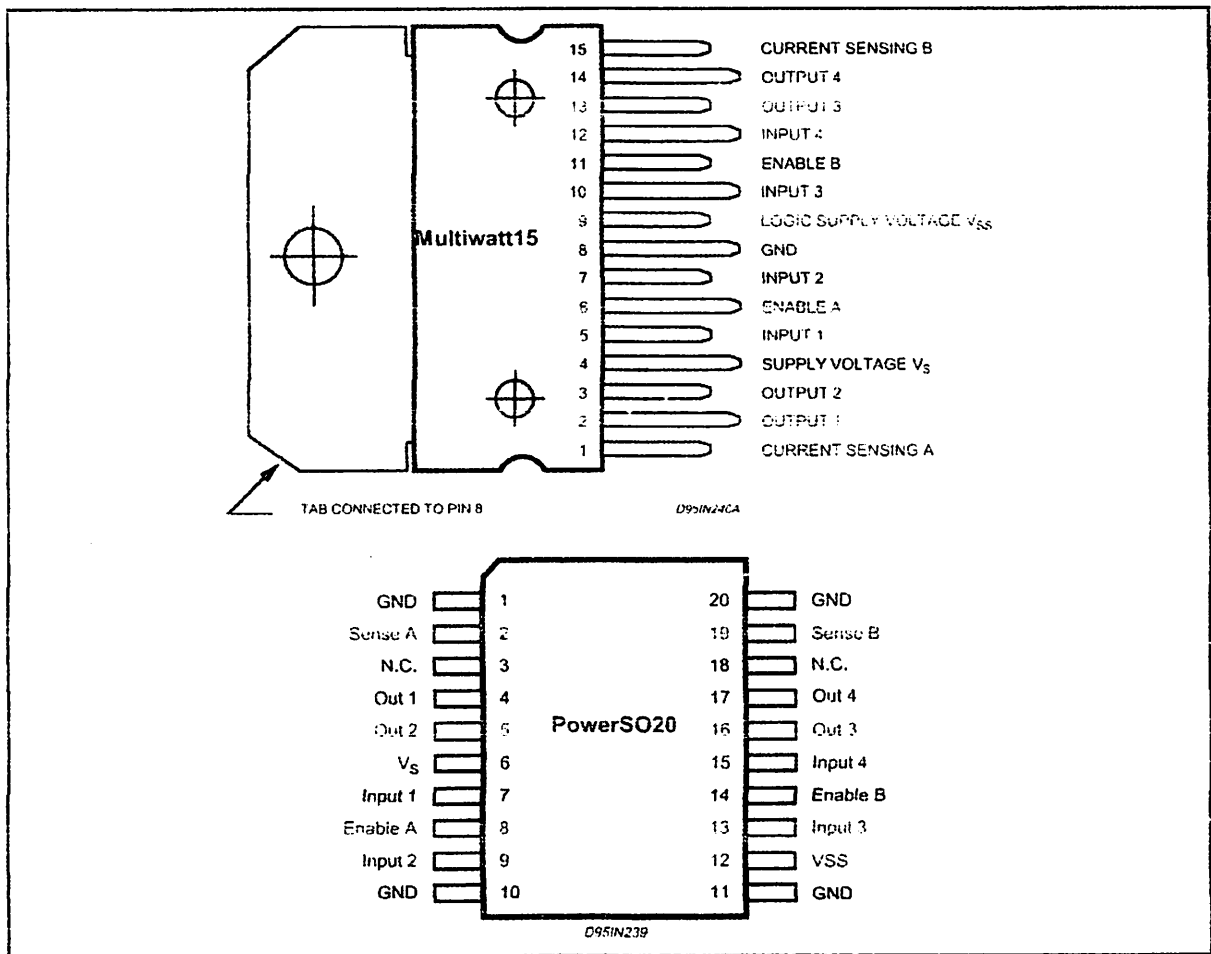
BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_S	Power Supply	50	V
V_{SS}	Logic Supply Voltage	7	V
V_I, V_{en}	Input and Enable Voltage	-0.3 to 7	V
I_O	Peak Output Current (each Channel)		
	- Non Repetitive ($t = 100\mu s$)	3	A
	- Repetitive (80% on -20% off; $t_{on} = 10ms$)	2.5	A
	-DC Operation	2	A
$V_{senc.}$	Sensing Voltage	-1 to 2.3	V
P_{tot}	Total Power Dissipation ($T_{case} = 75^\circ C$)	25	W
T_{cp}	Junction Operating Temperature	-25 to 130	$^\circ C$
T_{stg}, T_J	Storage and Junction Temperature	-40 to 150	$^\circ C$

PIN CONNECTIONS (top view)



THERMAL DATA

Symbol	Parameter		PowerSO20	Multiwatt15	Unit
$R_{th j-case}$	Thermal Resistance Junction-case	Max.	-	3	$^\circ C/W$
$R_{th j-amb}$	Thermal Resistance Junction-ambient	Max.	13 (*)	35	$^\circ C/W$

(*) Mounted on aluminum substrate



PIN FUNCTIONS (refer to the block diagram)

MW.15	PowerSO	Name	Function
1;15	2;19	Sense A; Sense B	Between this pin and ground is connected the sense resistor to control the current of the load.
2;3	4;5	Out 1; Out 2	Outputs of the Bridge A: the current that flows through the load connected between these two pins is monitored at pin 1.
4	6	V _s	Supply Voltage for the Power Output Stages. A non-inductive 100nF capacitor must be connected between this pin and ground.
5;7	7;9	Input 1; Input 2	TTL Compatible Inputs of the Bridge A.
6;11	8;14	Enable A; Enable B	TTL Compatible Enable Input: the L state disables the bridge A (enable A) and/or the bridge B (enable B).
8	1,10,11,20	GND	Ground.
9	12	V _{SS}	Supply Voltage for the Logic Blocks. A 100nF capacitor must be connected between this pin and ground.
10; 12	13;15	Input 3; Input 4	TTL Compatible Inputs of the Bridge B.
13; 14	16;17	Out 3; Out 4	Outputs of the Bridge B. The current that flows through the load connected between these two pins is monitored at pin 15.
-	3;18	N.C.	Not Connected

ELECTRICAL CHARACTERISTICS (V_s = 42V; V_{SS} = 5V, T_j = 25°C; unless otherwise specified)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
V _s	Supply Voltage (pin 4)	Operative Condition	V _{IH} +2.5		46	V
V _{SS}	Logic Supply Voltage (pin 9)		4.5	5	7	V
I _s	Quiescent Supply Current (pin 4)	V _{en} = H; I _L = 0	V _i = L	13	22	mA
			V _i = H	50	70	mA
		V _{en} = L	V _i = X		4	mA
I _{SS}	Quiescent Current from V _{SS} (pin 9)	V _{en} = H; I _L = 0	V _i = L	24	36	mA
			V _i = H	7	12	mA
		V _{en} = L	V _i = X		6	mA
V _{iL}	Input Low Voltage (pins 5, 7, 10, 12)		-0.3		1.5	V
V _{iH}	Input High Voltage (pins 5, 7, 10, 12)		2.3		V _{SS}	V
I _{iL}	Low Voltage Input Current (pins 5, 7, 10, 12)	V _i = L			-10	μA
I _{iH}	High Voltage Input Current (pins 5, 7, 10, 12)	V _i = H ≤ V _{SS} - 0.6V		30	100	μA
V _{en} = L	Enable Low Voltage (pins 6, 11)		-0.3		1.5	V
V _{en} = H	Enable High Voltage (pins 6, 11)		2.3		V _{SS}	V
I _{en} = L	Low Voltage Enable Current (pins 6, 11)	V _{er} = L			-10	μA
I _{en} = H	High Voltage Enable Current (pins 6, 11)	V _{en} = H ≤ V _{SS} - 0.6V		30	100	μA
V _{CEsat(H)}	Source Saturation Voltage	I _L = 1A	0.95	1.35	1.7	V
		I _L = 2A		2	2.7	V
V _{CEsat(L)}	Sink Saturation Voltage	I _L = 1A (5)	0.85	1.2	1.6	V
		I _L = 2A (5)		1.7	2.3	V
V _{CEsat}	Total Drop	I _L = 1A (5)	1.80		3.2	V
		I _L = 2A (5)			4.9	V
V _{sens}	Sensing Voltage (pins 1, 15)		-1 (1)		2	V

ELECTRICAL CHARACTERISTICS (continued)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
T ₁ (V)	Source Current Turn-off Delay	0.5 V _i to 0.9 I _L (2); (4)		1.5		μs
T ₂ (V)	Source Current Fall Time	0.9 I _L to 0.1 I _L (2); (4)		0.2		μs
T ₃ (V)	Source Current Turn-on Delay	0.5 V _i to 0.1 I _L (2); (4)		2		μs
T ₄ (V)	Source Current Rise Time	0.1 I _L to 0.9 I _L (2); (4)		0.7		μs
T ₅ (V)	Sink Current Turn-off Delay	0.5 V _i to 0.9 I _L (3); (4)		0.7		μs
T ₆ (V)	Sink Current Fall Time	0.9 I _L to 0.1 I _L (3); (4)		0.25		μs
T ₇ (V)	Sink Current Turn-on Delay	0.5 V _i to 0.9 I _L (3); (4)		1.6		μs
T ₈ (V)	Sink Current Rise Time	0.1 I _L to 0.9 I _L (3); (4)		0.2		μs
f _c (V)	Commutation Frequency	I _L = 2A		25	40	KHz
T ₁ (V _{en})	Source Current Turn-off Delay	0.5 V _{en} to 0.9 I _L (2); (4)		3		μs
T ₂ (V _{en})	Source Current Fall Time	0.9 I _L to 0.1 I _L (2); (4)		i		μs
T ₃ (V _{en})	Source Current Turn-on Delay	0.5 V _{en} to 0.1 I _L (2); (4)		0.3		μs
T ₄ (V _{en})	Source Current Rise Time	0.1 I _L to 0.9 I _L (2); (4)		0.4		μs
T ₅ (V _{en})	Sink Current Turn-off Delay	0.5 V _{en} to 0.9 I _L (3); (4)		2.2		μs
T ₆ (V _{en})	Sink Current Fall Time	0.9 I _L to 0.1 I _L (3); (4)		0.35		μs
T ₇ (V _{en})	Sink Current Turn-on Delay	0.5 V _{en} to 0.9 I _L (3); (4)		0.25		μs
T ₈ (V _{en})	Sink Current Rise Time	0.1 I _L to 0.9 I _L (3); (4)		0.1		μs

- 1) Sensing voltage can be -1 V for t ≤ 50 μsec; in steady state V_{en(s)} min = -0.5 V.
- 2) See fig. 2.
- 3) See fig. 4.
- 4) The load must be a pure resistor.

Figure 1 : Typical Saturation Voltage vs. Output Current.

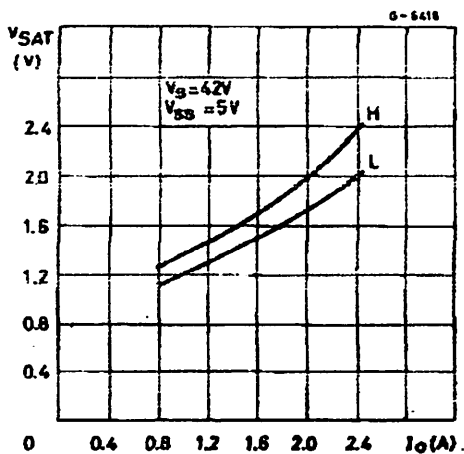
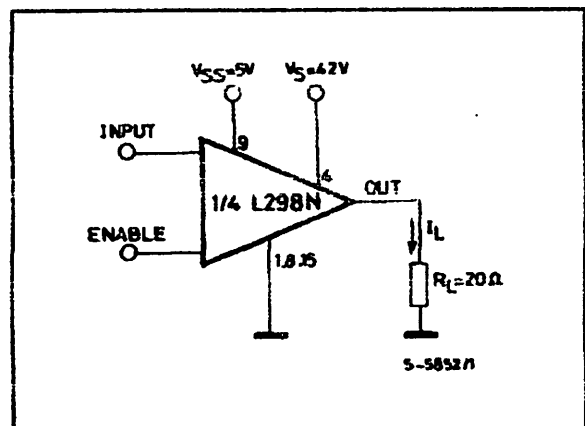


Figure 2 : Switching Times Test Circuits.



Note : For INPUT Switching, set EN = H
For ENABLE Switching, set IN = H

Figure 3 : Source Current Delay Times vs. Input or Enable Switching.

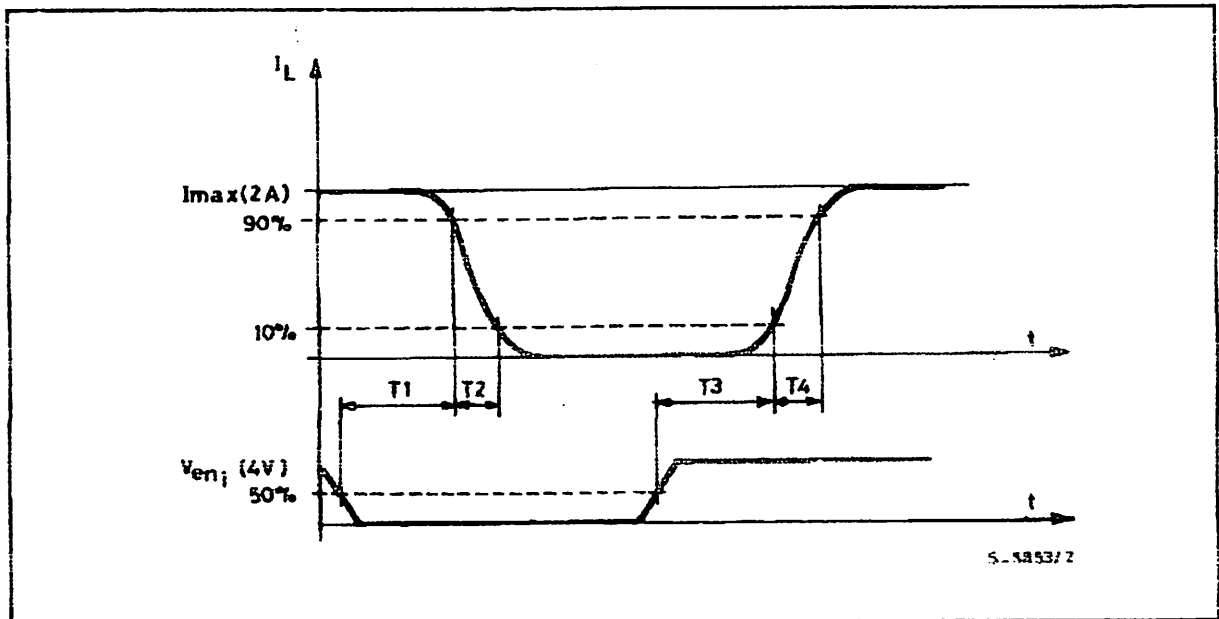
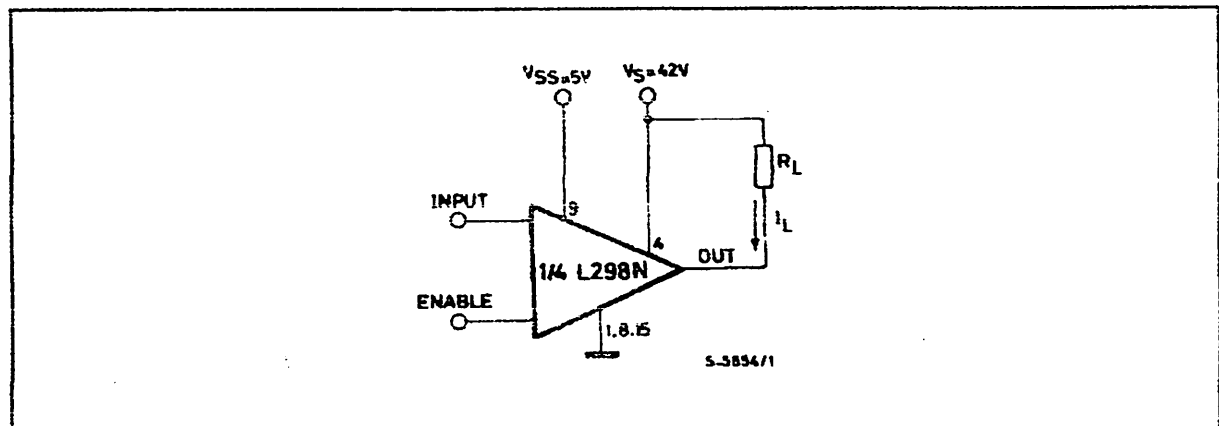


Figure 4 : Switching Times Test Circuits.



Note : For INPUT Switching, set EN = H
 For ENABLE Switching, set IN = L

Figure 5 : Sink Current Delay Times vs. Input 0 V Enable Switching.

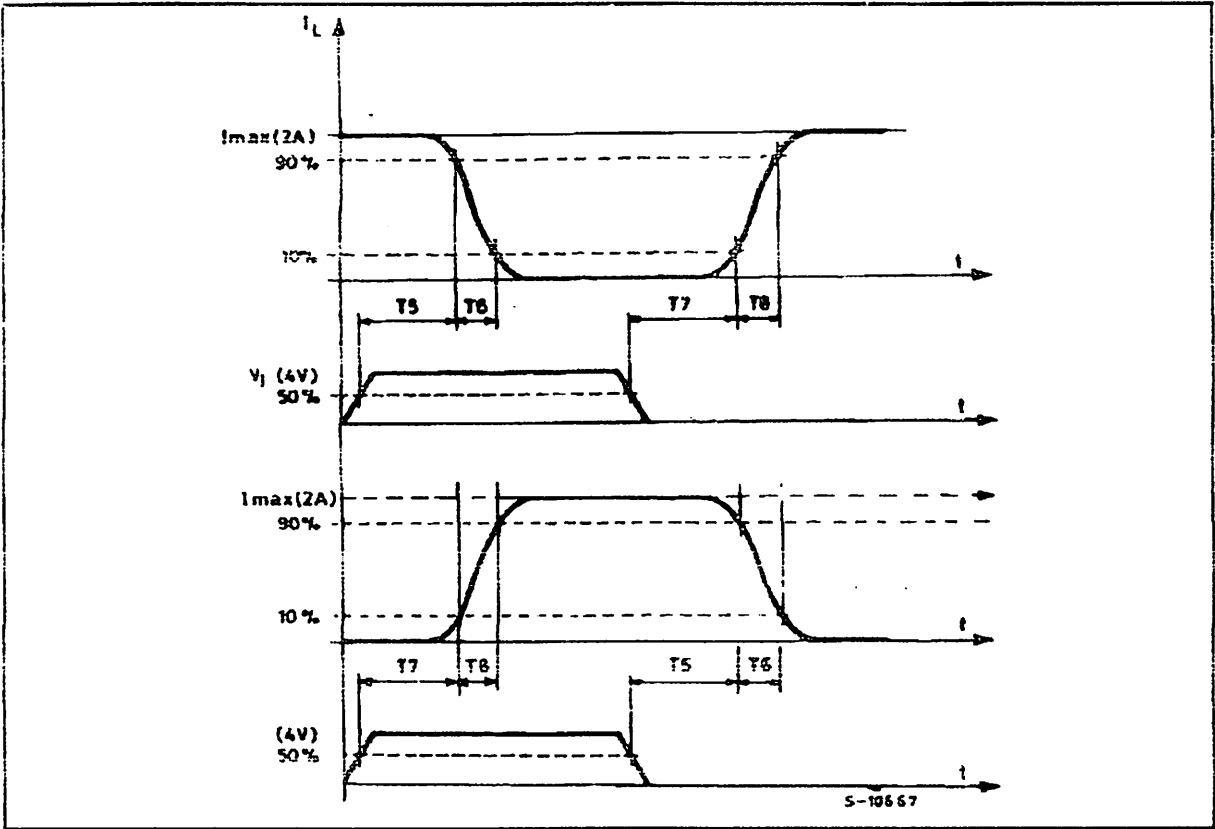


Figure 6 : Bidirectional DC Motor Control.

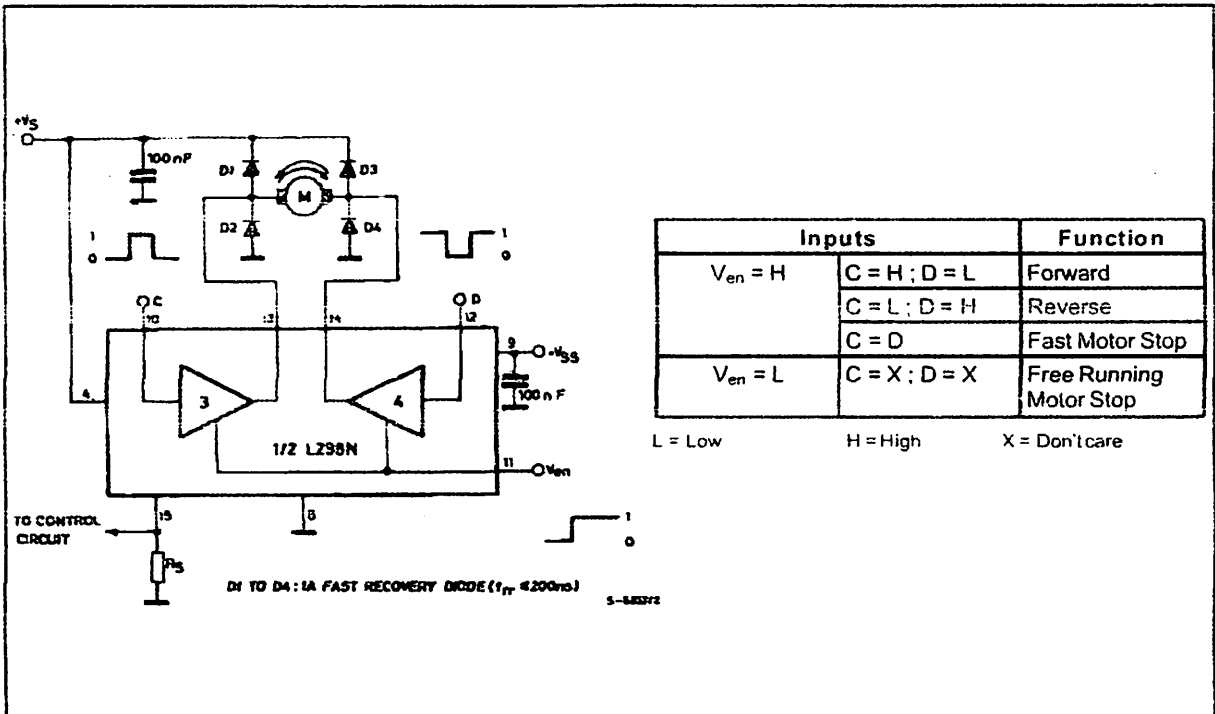
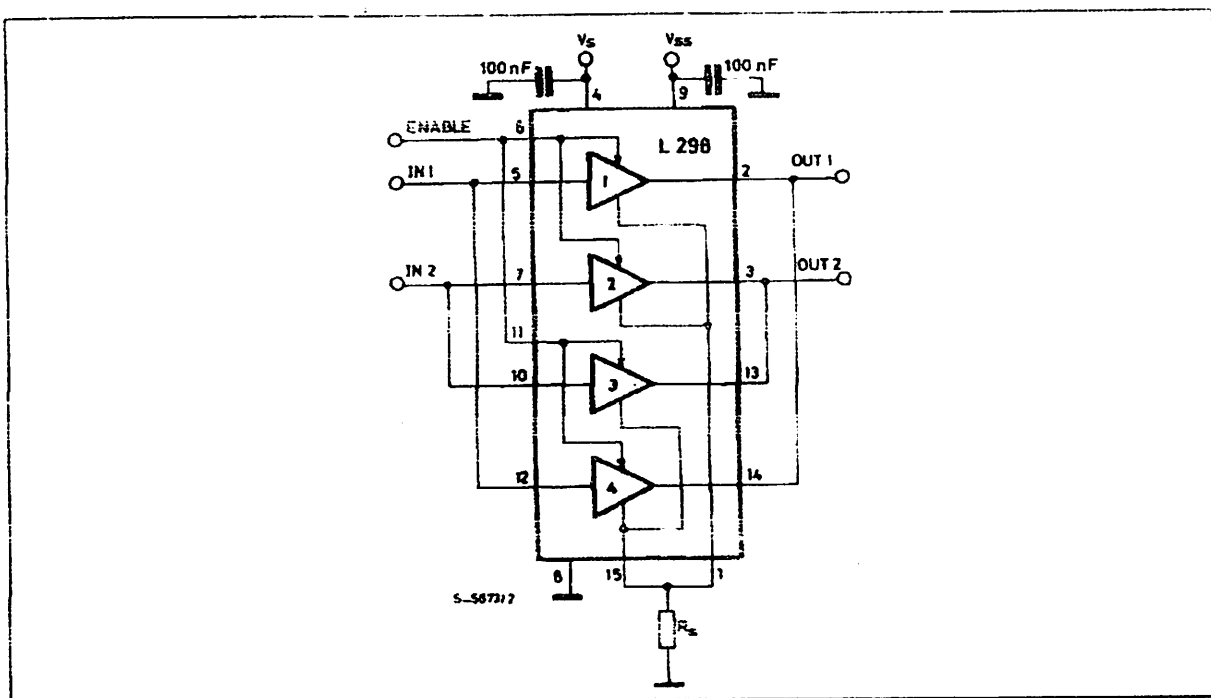


Figure 7 : For higher currents, outputs can be paralleled. Take care to parallel channel 1 with channel 4 and channel 2 with channel 3.



APPLICATION INFORMATION (Refer to the block diagram)

1.1. POWER OUTPUT STAGE

The L298 integrates two power output stages (A; B). The power output stage is a bridge configuration and its outputs can drive an inductive load in common or differential mode, depending on the state of the inputs. The current that flows through the load comes out from the bridge at the sense output: an external resistor (R_{SA} ; R_{SB}) allows to detect the intensity of this current.

1.2. INPUT STAGE

Each bridge is driven by means of four gates the input of which are In_1 ; In_2 ; EnA and In_3 ; In_4 ; EnB . The In inputs set the bridge state when The En input is high; a low state of the En input inhibits the bridge. All the inputs are TTL compatible.

2. SUGGESTIONS

A non inductive capacitor, usually of 100 nF, must be foreseen between both V_s and V_{ss} , to ground, as near as possible to GND pin. When the large capacitor of the power supply is too far from the IC, a second smaller one must be foreseen near the L298.

The sense resistor, not of a wire wound type, must be grounded near the negative pole of V_s that must be near the GND pin of the I.C.

Each input must be connected to the source of the driving signals by means of a very short path.

Turn-On and Turn-Off: Before to Turn-ON the Supply Voltage and before to Turn it OFF, the Enable input must be driven to the Low state.

3. APPLICATIONS

Fig 6 shows a bidirectional DC motor control Schematic Diagram for which only one bridge is needed. The external bridge of diodes D1 to D4 is made by four fast recovery elements ($t_{rr} \leq 200$ nsec) that must be chosen of a VF as low as possible at the worst case of the load current.

The sense output voltage can be used to control the current amplitude by chopping the inputs, or to provide overcurrent protection by switching low the enable input.

The brake function (Fast motor stop) requires that the Absolute Maximum Rating of 2 Amps must never be overcome.

When the repetitive peak current needed from the load is higher than 2 Amps, a paralleled configuration can be chosen (See Fig.7).

An external bridge of diodes are required when inductive loads are driven and when the inputs of the IC are chopped; Schottky diodes would be preferred.

L298

This solution can drive until 3 Amps In DC operation and until 3.5 Amps of a repetitive peak current.

On Fig 8 it is shown the driving of a two phase bipolar stepper motor ; the needed signals to drive the inputs of the L298 are generated, in this example, from the IC L297.

Fig 9 shows an example of P.C.B. designed for the application of Fig 8.

Figure 8 : Two Phase Bipolar Stepper Motor Circuit.

This circuit drives bipolar stepper motors with winding currents up to 2 A. The diodes are fast 2 A types.

Fig 10 shows a second two phase bipolar stepper motor control circuit where the current is controlled by the I.C. L6506.

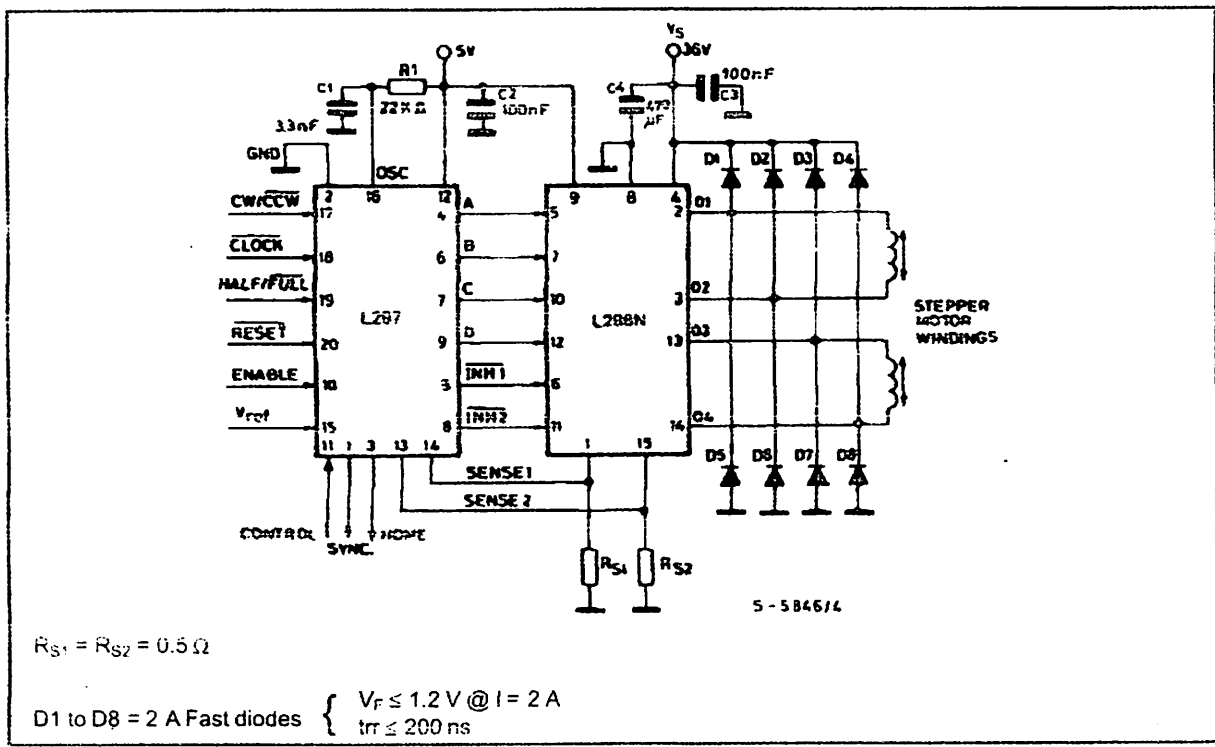


Figure 9 : Suggested Printed Circuit Board Layout for the Circuit of fig. 8 (1:1 scale).

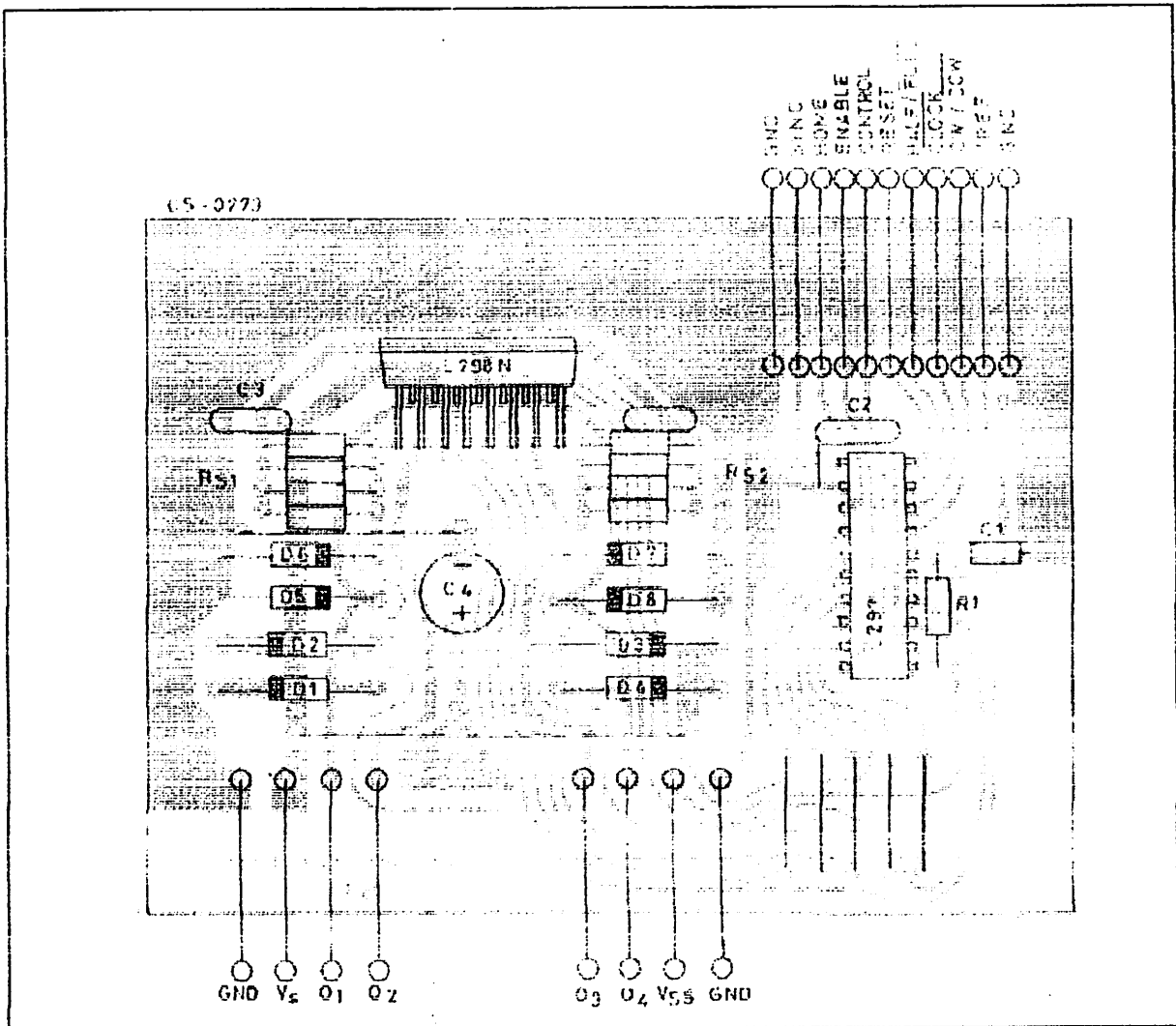
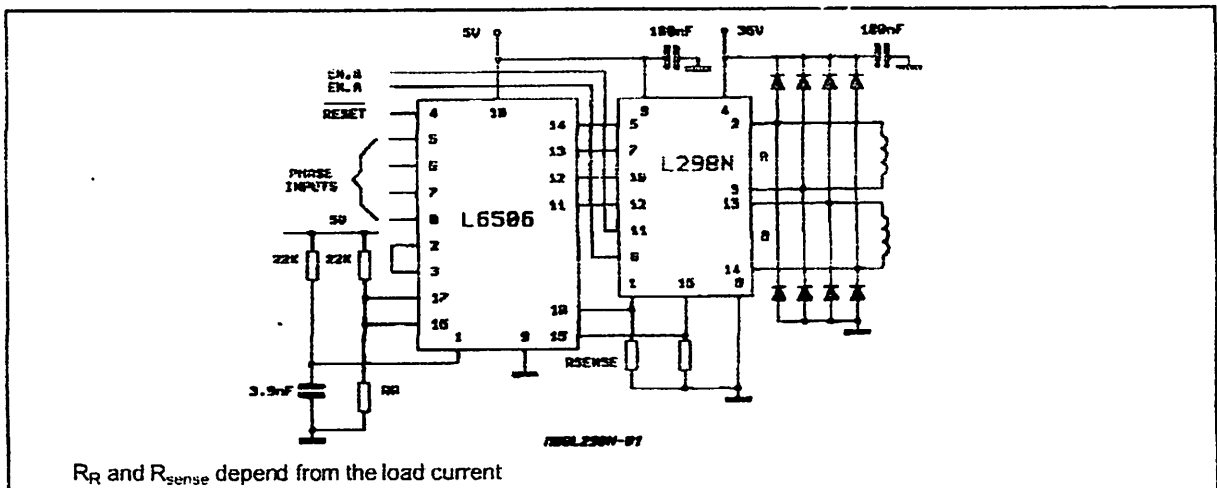
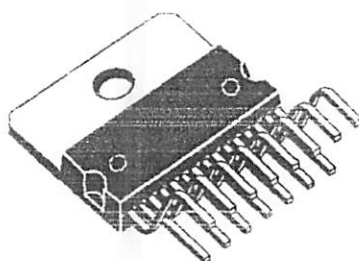


Figure 10 : Two Phase Bipolar Stepper Motor Control Circuit by Using the Current Controller L6506.

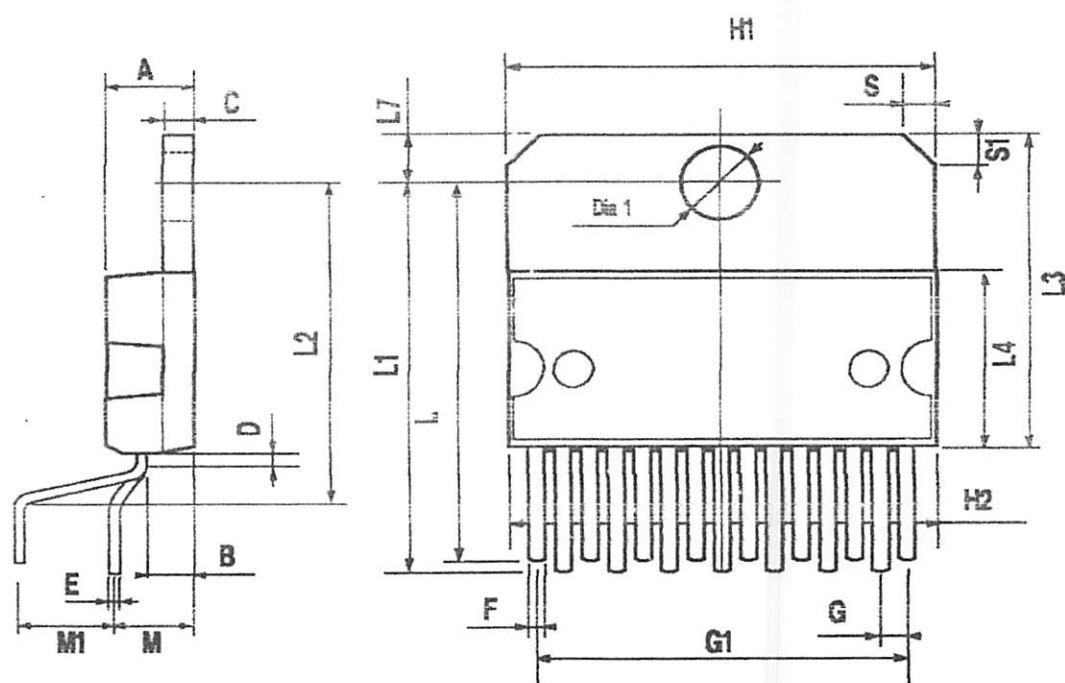


DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A			5			0.197
B			2.65			0.104
C			1.6			0.063
D		1			0.039	
E	0.49		0.55	0.019		0.022
F	0.66		0.75	0.026		0.030
G	1.02	1.27	1.52	0.040	0.050	0.060
G1	17.53	17.78	18.03	0.690	0.700	0.710
H1	19.6			0.772		
H2			20.2			0.795
L	21.9	22.2	22.5	0.862	0.874	0.886
L1	21.7	22.1	22.5	0.854	0.870	0.886
L2	17.65		18.1	0.695		0.713
L3	17.25	17.5	17.75	0.679	0.689	0.699
L4	10.3	10.7	10.9	0.406	0.421	0.429
L7	2.65		2.9	0.104		0.114
M	4.25	4.55	4.85	0.167	0.179	0.191
M1	4.63	5.08	5.53	0.182	0.200	0.218
S	1.9		2.6	0.075		0.102
S1	1.9		2.6	0.075		0.102
Dia1	3.65		3.85	0.144		0.152

OUTLINE AND MECHANICAL DATA

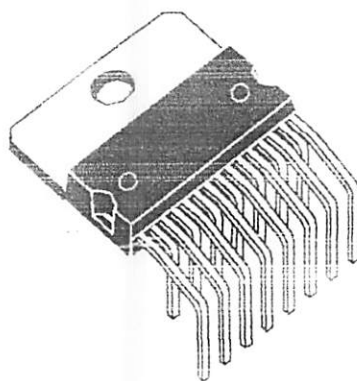


Multiwatt15 V

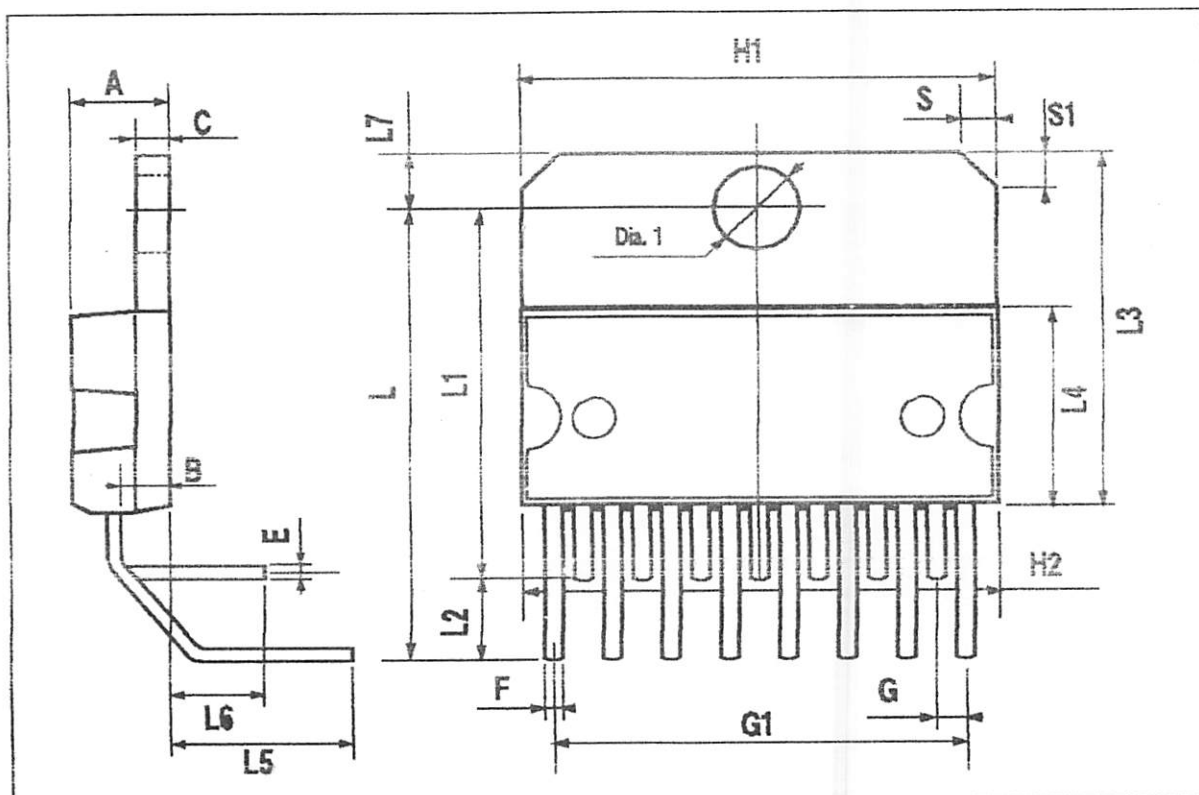


DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A			5			0.197
B			2.65			0.104
C			1.6			0.063
E	0.49		0.55	0.019		0.022
F	0.66		0.75	0.026		0.030
G	1.14	1.27	1.4	0.045	0.050	0.055
G1	17.57	17.78	17.91	0.692	0.700	0.705
H1	19.6			0.772		
H2			20.2			0.795
L		20.57			0.810	
L1		18.03			0.710	
L2		2.54			0.100	
L3	17.25	17.5	17.75	0.679	0.689	0.699
L4	10.3	10.7	10.9	0.406	0.421	0.429
L5		5.28			0.208	
L6		2.38			0.094	
L7	2.65		2.9	0.104		0.114
S	1.9		2.6	0.075		0.102
S1	1.9		2.6	0.075		0.102
Dia1	3.65		3.85	0.144		0.152

OUTLINE AND MECHANICAL DATA



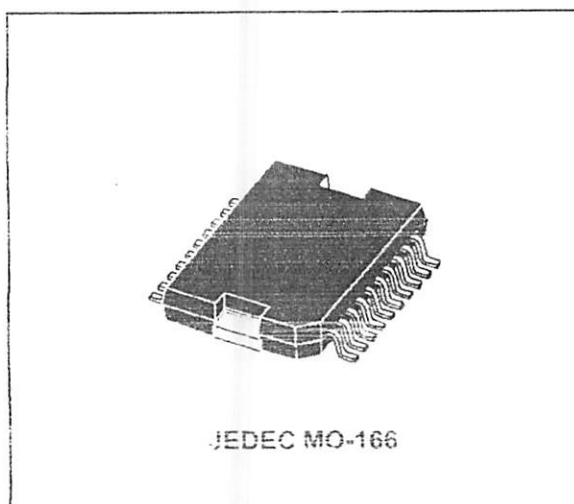
Multiwatt15 H



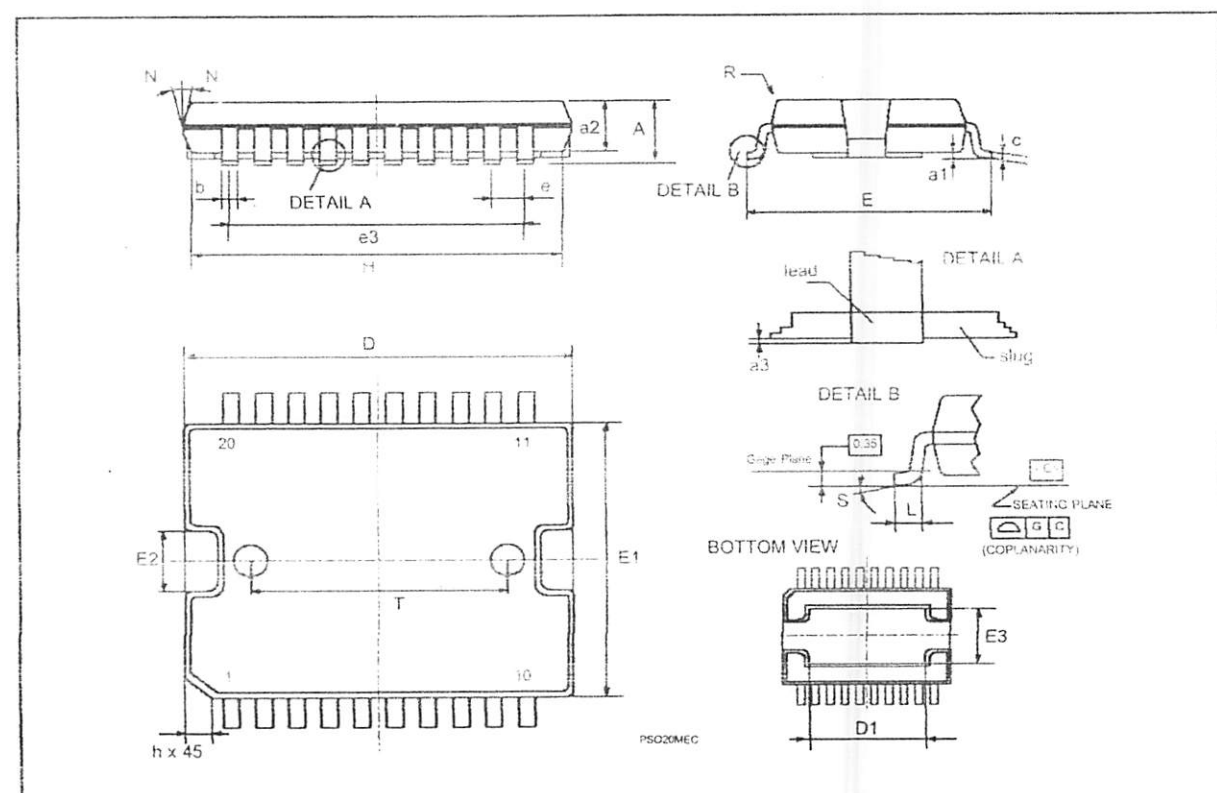
DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A			3.6			0.142
a1	0.1		0.3	0.004		0.012
a2			3.3			0.130
a3	0		0.1	0.000		0.004
b	0.4		0.53	0.016		0.021
c	0.23		0.32	0.009		0.013
D (1)	15.8		16	0.622		0.630
D1	9.4		9.8	0.370		0.386
E	13.9		14.5	0.547		0.570
e		1.27			0.050	
e3		11.43			0.450	
E1 (1)	10.9		11.1	0.429		0.437
E2			2.9			0.114
E3	5.8		6.2	0.228		0.244
G	0		0.1	0.000		0.004
H	15.5		15.9	0.610		0.626
h			1.1			0.043
L	0.8		1.1	0.031		0.043
N	10° (max.)					
S	8° (max.)					
T		10			0.394	

(1) "D and F" do not include mold flash or protrusions.
 - Mold flash or protrusions shall not exceed 0.15 mm (0.006").
 - Critical dimensions "E", "G" and "a3"

OUTLINE AND MECHANICAL DATA



PowerSO20



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Singapore - Spain - Sweden - Switzerland - United Kingdom - U.S.A.

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Features

Low-Voltage and Standard-Voltage Operation

5.0 (V_{CC} = 4.5V to 5.5V)

2.7 (V_{CC} = 2.7V to 5.5V)

2.5 (V_{CC} = 2.5V to 5.5V)

1.8 (V_{CC} = 1.8V to 5.5V)

Internally Organized 128 x 8 (1K), 256 x 8 (2K), 512 x 8 (4K),

1024 x 8 (8K) or 2048 x 8 (16K)

2-Wire Serial Interface

Write Enable Pin with Pull-Up Resistor, Filtered Inputs for Noise Suppression

Bi-Directional Data Transfer Protocol

100 kHz (1.8V, 2.5V, 2.7V) and 400 kHz (5V) Compatibility

Write Protect Pin for Hardware Data Protection

1-Byte Page (1K, 2K), 16-Byte Page (4K, 8K, 16K) Write Modes

Random Access Page Writes Are Allowed

Variable Write Cycle Time (10 ms max)

High Reliability

Endurance: 1 Million Write Cycles

Data Retention: 100 Years

ESD Protection: >3000V

Automotive Grade and Extended Temperature Devices Available

Available in 8-Pin and 14-Pin JEDEC SOIC, 8-Pin PDIP, 8-Pin MSOP, and 8-Pin TSSOP Packages

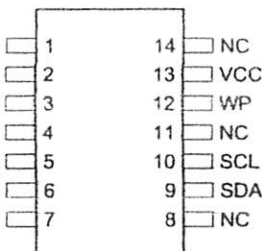
Description

The AT24C01A/02/04/08/16 provides 1024/2048/4096/8192/16384 bits of serial electrically erasable and programmable read only memory (EEPROM) organized as 128/256/512/1024/2048 words of 8 bits each. The device is optimized for use in many industrial and commercial applications where low power and low voltage operation are essential. The AT24C01A/02/04/08/16 is available in space saving 8-pin PDIP, 8-Pin MSOP, 8-Pin TSSOP, 8-Pin MSOP, 8-Pin TSSOP, 14-Pin JEDEC SOIC, 14-Pin SOIC, and 8-Pin and 14-Pin JEDEC SOIC (AT24C01A/02/04/08/16) packages and is accessed via a 2-wire serial interface. In addition, the entire family is available in 5.0V (4.5V to 5.5V), 2.7V (2.7V to 5.5V), 2.5V (2.5V to 5.5V) and 1.8V (1.8V to 5.5V) versions.

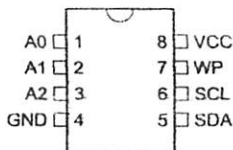
Configurations

Name	Function
A0	Address Inputs
A1	Address Inputs
A2	Address Inputs
SDA	Serial Data
SCL	Serial Clock Input
WP	Write Protect
NC	No Connect

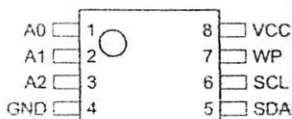
14-Pin SOIC



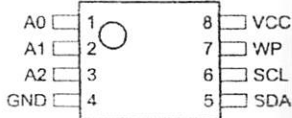
8-Pin PDIP



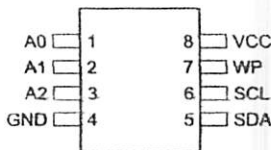
8-Pin TSSOP



8-Pin MSOP



8-Pin SOIC



2-Wire Serial EEPROM

1K (128 x 8)

2K (256 x 8)

4K (512 x 8)

8K (1024 x 8)

16K (2048 x 8)

AT24C01A
AT24C02
AT24C04
AT24C08
AT24C16



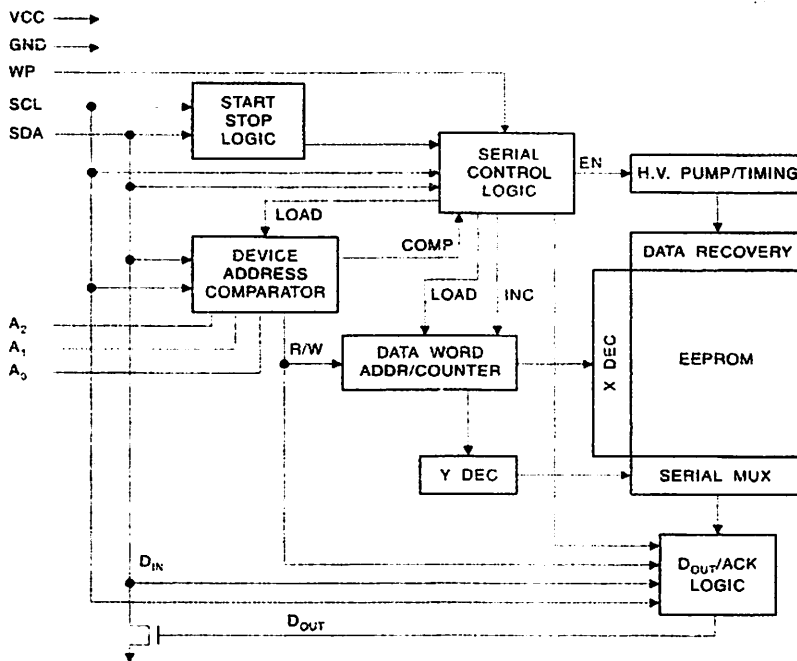


Absolute Maximum Ratings

Operating Temperature	-55°C to +125°C
Storage Temperature	-65°C to +150°C
Voltage on Any Pin Respect to Ground	-1.0V to +7.0V
Maximum Operating Voltage.....	6.25V
Maximum Output Current.....	5.0 mA

***NOTICE:** Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Block Diagram



Description

SERIAL CLOCK (SCL): The SCL input is used to positive clock data into each EEPROM device and negative clock data out of each device.

SERIAL DATA (SDA): The SDA pin is bidirectional for data transfer. This pin is open-drain driven and may be ORed with any number of other open-drain or open-drain devices.

DEVICE/PAGE ADDRESSES (A2, A1, A0): The A2, A1 and A0 pins are device address inputs that are hard wired to the device. For the AT24C01A and the AT24C02, as many as eight devices may be addressed on a single bus system. For the AT24C04, as many as four devices may be addressed on a single bus system. For the AT24C08, as many as two devices may be addressed on a single bus system. For the AT24C16, only one device may be addressed on a single bus system. Addressing is discussed in detail under the Device Addressing section).

The AT24C04 uses the A2 and A1 inputs for hard wire addressing and a total of four 4K devices may be addressed on a single bus system. The A0 pin is a no connect.

The AT24C08 only uses the A2 input for hardwire addressing and a total of two 8K devices may be addressed on a single bus system. The A0 and A1 pins are no connects.

The AT24C16 does not use the device address pins which limits the number of devices on a single bus to one. The A0, A1 and A2 pins are no connects.

WRITE PROTECT (WP): The AT24C01A/02/04/16 has a Write Protect pin that provides hardware data protection. The Write Protect pin allows normal read/write operations when connected to ground (GND). When the Write Protect pin is connected to V_{CC}, the write protection feature is enabled and operates as shown in the following table.

ID	Part of the Array Protected				
	24C01A	24C02	24C04	24C08	24C16
	Full (1K) Array	Full (2K) Array	Full (4K) Array	Normal Read/Write Operation	Upper Half (8K) Array
	Normal Read/Write Operations				

Memory Organization

AT24C01A, 1K SERIAL EEPROM: Internally organized with 28 pages of 1-byte each, the 1K requires a 7-bit data word address for random word addressing.

Capacitance⁽¹⁾

Measurable over recommended operating range from $T_A = 25^\circ\text{C}$, $f = 1.0\text{ MHz}$, $V_{CC} = +1.8\text{V}$.

Parameter	Test Condition	Max	Units	Conditions
	Input/Output Capacitance (SDA)	8	pF	$V_{I/O} = 0\text{V}$
	Input Capacitance ($A_0, A_1, A_2, \text{SCL}$)	6	pF	$V_{IN} = 0\text{V}$

1. This parameter is characterized and is not 100% tested.

Characteristics

Measurable over recommended operating range from: $T_{AI} = -40^\circ\text{C}$ to $+85^\circ\text{C}$, $V_{CC} = +1.8\text{V}$ to $+5.5\text{V}$, $T_{AC} = 0^\circ\text{C}$ to $+70^\circ\text{C}$, $V_{IN} = +1.8\text{V}$ to $+5.5\text{V}$ (unless otherwise noted).

Parameter	Test Condition	Min	Typ	Max	Units
Supply Voltage		1.8		5.5	V
Supply Voltage		2.5		5.5	V
Supply Voltage		2.7		5.5	V
Supply Voltage		4.5		5.5	V
Supply Current $V_{CC} = 5.0\text{V}$	READ at 100 kHz		0.4	1.0	mA
Supply Current $V_{CC} = 5.0\text{V}$	WRITE at 100 kHz		2.0	3.0	mA
Standby Current $V_{CC} = 1.8\text{V}$	$V_{IN} = V_{CC}$ or V_{SS}		0.6	3.0	μA
Standby Current $V_{CC} = 2.5\text{V}$	$V_{IN} = V_{CC}$ or V_{SS}		1.4	4.0	μA
Standby Current $V_{CC} = 2.7\text{V}$	$V_{IN} = V_{CC}$ or V_{SS}		1.6	4.0	μA
Standby Current $V_{CC} = 5.0\text{V}$	$V_{IN} = V_{CC}$ or V_{SS}		8.0	18.0	μA
Input Leakage Current	$V_{IN} = V_{CC}$ or V_{SS}		0.10	3.0	μA
Output Leakage Current	$V_{OUT} = V_{CC}$ or V_{SS}		0.05	3.0	μA
Input Low Level ⁽¹⁾		-0.6		$V_{CC} \times 0.3$	V
Input High Level ⁽¹⁾		$V_{CC} \times 0.7$		$V_{CC} + 0.5$	V
Output Low Level $V_{CC} = 3.0\text{V}$	$I_{OL} = 2.1\text{ mA}$			0.4	V
Output Low Level $V_{CC} = 1.8\text{V}$	$I_{OL} = 0.15\text{ mA}$			0.2	V

1. V_{IL} min and V_{IH} max are reference only and are not tested.





Characteristics

able over recommended operating range from $T_A = -40^\circ\text{C}$ to $+85^\circ\text{C}$, $V_{CC} = +1.8\text{V}$ to $+5.5\text{V}$, $CL = 1$ TTL Gate and (unless otherwise noted).

Symbol	Parameter	2.7-, 2.5-, 1.8-volt		5.0-volt		Units
		Min	Max	Min	Max	
	Clock Frequency, SCL		100		400	kHz
	Clock Pulse Width Low	4.7		1.2		μs
	Clock Pulse Width High	4.0		0.6		μs
	Noise Suppression Time ⁽¹⁾		100		50	ns
	Clock Low to Data Out Valid	0.1	4.5	0.1	0.9	μs
	Time the bus must be free before a new transmission can start ⁽¹⁾	4.7		1.2		μs
A	Start Hold Time	4.0		0.6		μs
A	Start Set-up Time	4.7		0.6		μs
T	Data In Hold Time	0		0		μs
T	Data In Set-up Time	200		100		ns
	Inputs Rise Time ⁽¹⁾		1.0		0.3	μs
	Inputs Fall Time ⁽¹⁾		300		300	ns
O	Stop Set-up Time	4.7		0.6		μs
	Data Out Hold Time	100		50		ns
	Write Cycle Time		10		10	ms
urance ⁽¹⁾	5.0V, 25°C, Page Mode	1M		1M		Write Cycles

1. This parameter is characterized and is not 100% tested.

Device Operation

CLOCK and DATA TRANSITIONS: The SDA pin is normally pulled high with an external device. Data on the SDA may change only during SCL low time periods (refer to Validity timing diagram). Data changes during SCL low periods will indicate a start or stop condition as defined below.

START CONDITION: A high-to-low transition of SDA while SCL is high is a start condition which must precede any other command (refer to Start and Stop Definition timing diagram).

STOP CONDITION: A low-to-high transition of SDA while SCL is high is a stop condition. After a read sequence, the next command will place the EEPROM in a standby power mode (refer to Start and Stop Definition timing diagram).

ACKNOWLEDGE: All addresses and data words are serially transmitted to and from the EEPROM in 8-bit words. The EEPROM sends a zero to acknowledge that it has received each word. This happens during the ninth clock cycle.

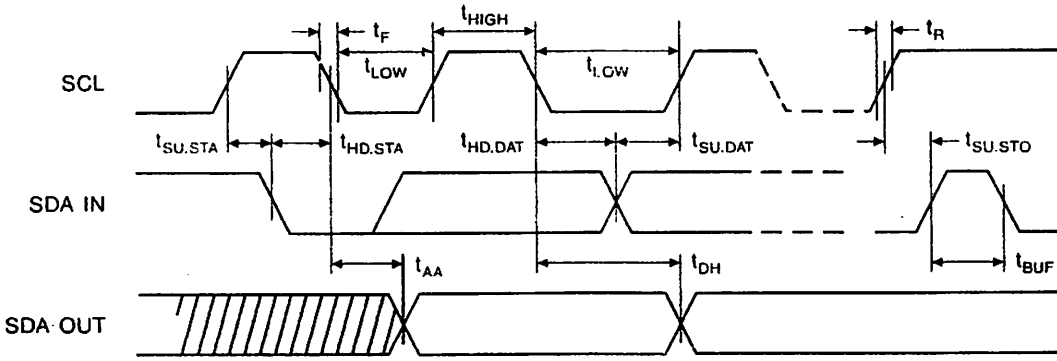
STANDBY MODE: The AT24C01A/02/04/08/16 features a low power standby mode which is enabled: (a) upon power-up and (b) after the receipt of the STOP bit and the completion of any internal operations.

MEMORY RESET: After an interruption in protocol, power loss or system reset, any 2-wire part can be reset by following these steps:

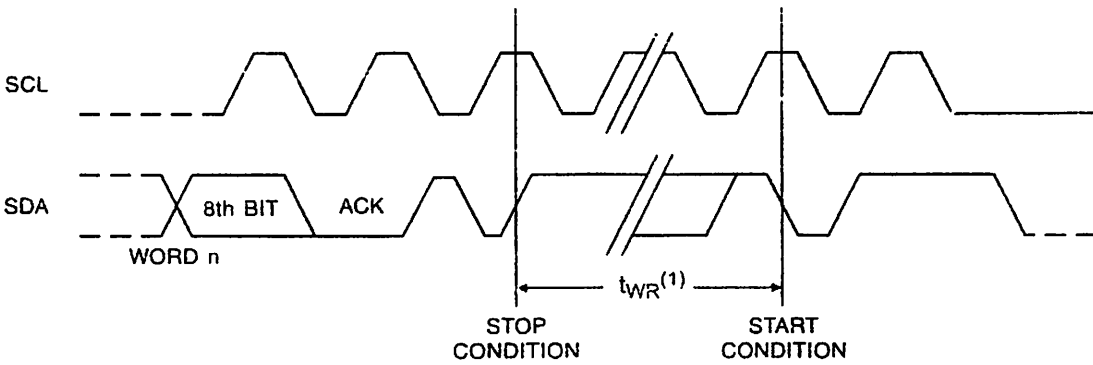
1. Clock up to 9 cycles.
2. Look for SDA high in each cycle while SCL is high.
3. Create a start condition as SDA is high.

AT24C01A/02/04/08/16

Timing
: Serial Clock, SDA: Serial Data I/O



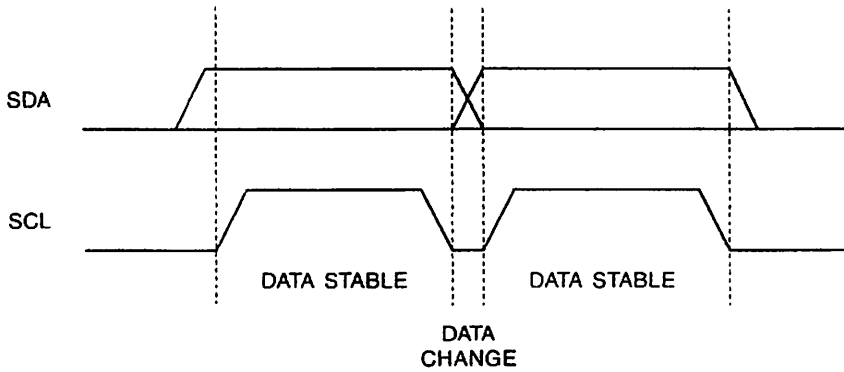
Write Cycle Timing
: Serial Clock, SDA: Serial Data I/O



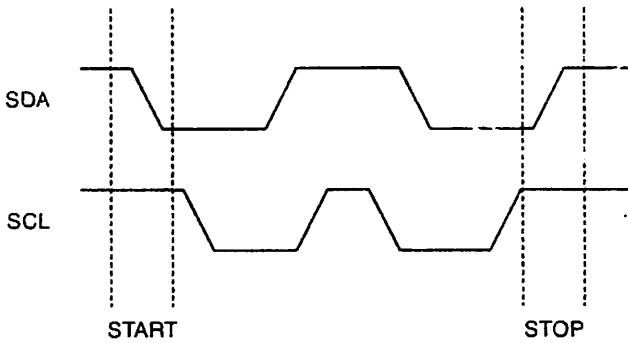
1. The write cycle time t_{WR} is the time from a valid stop condition of a write sequence to the end of the internal clear/write cycle.



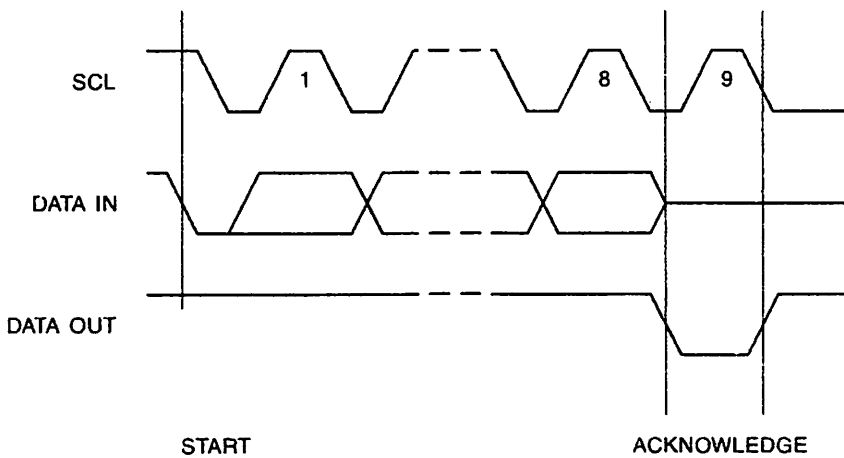
Validity



Start and Stop Definition



Without Acknowledge



Device Addressing

1K, 2K, 4K, 8K and 16K EEPROM devices all require a device address word following a start condition to address the chip for a read or write operation (refer to Figure 1).

The device address word consists of a mandatory one-bit start condition followed by a sequence for the first four most significant bits as shown in Figure 1. This is common to all the EEPROM devices.

The next 3 bits are the A2, A1 and A0 device address bits for the 1K/2K EEPROM. These 3 bits must compare to their corresponding hard-wired input pins.

The 4K EEPROM only uses the A2 and A1 device address bits with the third bit being a memory page address bit. The A0 device address bit must compare to its corresponding hard-wired input pin. The A0 pin is no connect.

The 8K EEPROM only uses the A2 device address bit with the next 2 bits being for memory page addressing. The A1 and A0 bits must compare to their corresponding hard-wired input pins. The A1 and A0 pins are no connect.

The 16K does not use any device address bits but instead the next 3 bits are used for memory page addressing. These 3 bits are the addressing bits on the 4K, 8K, and 16K devices and should be considered the most significant bits of the data word address which follows. The A0, A1 and A2 pins are no connect.

The fourth bit of the device address is the read/write operation select bit. A read operation is initiated if this bit is high and a write operation is initiated if this bit is low.

After a compare of the device address, the EEPROM will respond with a zero. If a compare is not made, the chip will return to standby state.

Write Operations

WRITE: A write operation requires an 8-bit data word address following the device address word and acknowledgment. Upon receipt of this address, the EEPROM will again respond with a zero and then clock in the next 8-bit data word. Following receipt of the 8-bit data word, the EEPROM will output a zero and the addressing sequence, such as a microcontroller, must terminate the write operation with a stop condition. At this time the EEPROM begins an internally-timed write cycle, t_{WR} , to the nonvolatile memory. All inputs are disabled during this write cycle and the EEPROM will not respond until the write is complete (refer to Figure 2).

WRITE: The 1K/2K EEPROM is capable of an 8-byte write, and the 4K, 8K and 16K devices are capable of 16-byte page writes.

The page write is initiated the same as a byte write, but the microcontroller does not send a stop condition after the first data word is clocked in. Instead, after the EEPROM

acknowledges receipt of the first data word, the microcontroller can transmit up to seven (1K/2K) or fifteen (4K, 8K, 16K) more data words. The EEPROM will respond with a zero after each data word received. The microcontroller must terminate the page write sequence with a stop condition (refer to Figure 3).

The data word address lower three (1K/2K) or four (4K, 8K, 16K) bits are internally incremented following the receipt of each data word. The higher data word address bits are not incremented, retaining the memory page row location. When the word address, internally generated, reaches the page boundary, the following byte is placed at the beginning of the same page. If more than eight (1K/2K) or sixteen (4K, 8K, 16K) data words are transmitted to the EEPROM, the data word address will "roll over" and previous data will be overwritten.

ACKNOWLEDGE POLLING: Once the internally-timed write cycle has started and the EEPROM inputs are disabled, acknowledge polling can be initiated. This involves sending a start condition followed by the device address word. The read/write bit is representative of the operation desired. Only if the internal write cycle has completed will the EEPROM respond with a zero allowing the read or write sequence to continue.

Read Operations

Read operations are initiated the same way as write operations with the exception that the read/write select bit in the device address word is set to one. There are three read operations: current address read, random address read and sequential read.

CURRENT ADDRESS READ: The internal data word address counter maintains the last address accessed during the last read or write operation, incremented by one. This address stays valid between operations as long as the chip power is maintained. The address "roll over" during a read is from the last byte of the last memory page to the first byte of the first page. The address "roll over" during a write is from the last byte of the current page to the first byte of the same page.

Once the device address with the read/write select bit set to one is clocked in and acknowledged by the EEPROM, the current address data word is serially clocked out. The microcontroller does not respond with an input zero but does generate a following stop condition (refer to Figure 4).

RANDOM READ: A random read requires a "dummy" byte write sequence to load in the data word address. Once the device address word and data word address are clocked in and acknowledged by the EEPROM, the microcontroller must generate another start condition. The microcontroller now initiates a current address read by sending a device address with the read/write select bit high. The EEPROM acknowledges the device address and serially clocks out





data word. The microcontroller does not respond with a zero but does generate a following stop condition (refer to Figure 5).

SEQUENTIAL READ: Sequential reads are initiated by either a current address read or a random address read. When the microcontroller receives a data word, it responds with an acknowledge. As long as the EEPROM receives an

acknowledge, it will continue to increment the data word address and serially clock out sequential data words. When the memory address limit is reached, the data word address will "roll over" and the sequential read will continue. The sequential read operation is terminated when the microcontroller does not respond with a zero but does generate a following stop condition (refer to Figure 6).

Figure 1. Device Address

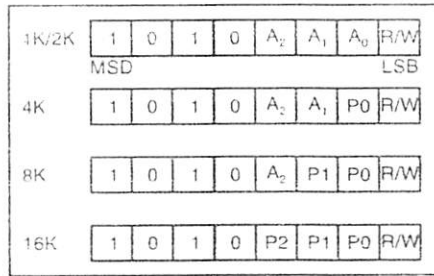


Figure 2. Byte Write

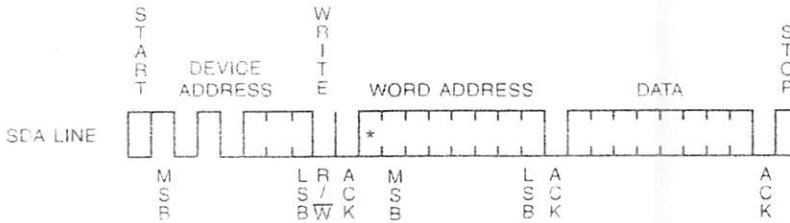
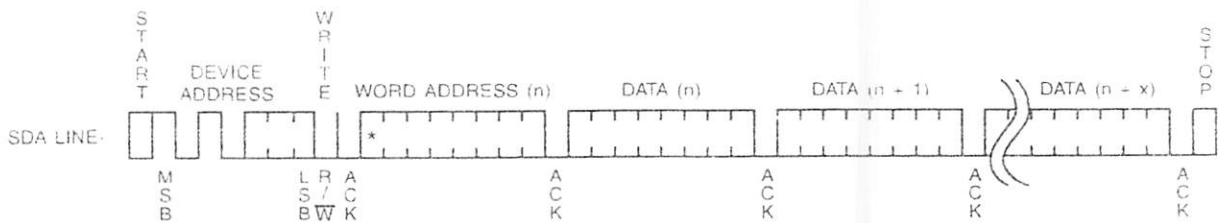


Figure 3. Page Write



(* = DON'T CARE bit for 1K)

Figure 4. Current Address Read

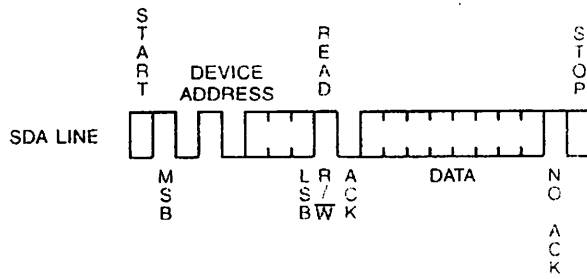
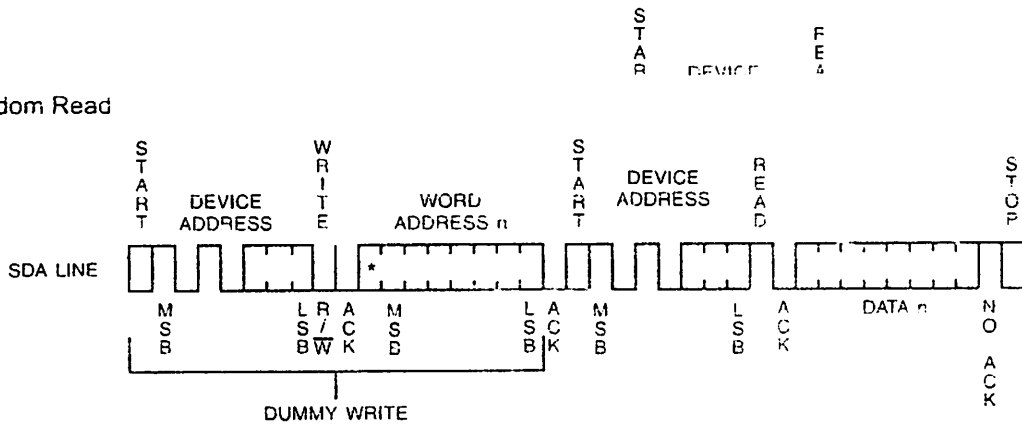
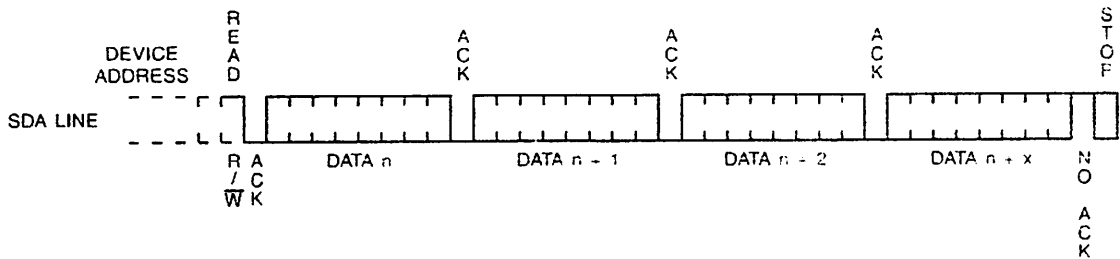


Figure 5. Random Read



(* = DON'T CARE bit for 1K)

Figure 6. Sequential Read





4C01A Ordering Information

t_{max} (ns)	I_{CC} (max) (μA)	I_{SB} (max) (μA)	f_{MAX} (kHz)	Ordering Code	Package	Operation Range
10	3000	18	400	AT24C01A-10PC	8P3	Commercial (0°C to 70°C)
				AT24C01A-10SC	8S1	
				AT24C01A-10MC	8M	
				AT24C01A-10TC	8T	
	3000	18	400	AT24C01A-10PI	8P3	Industrial (-40°C to 85°C)
				AT24C01A-10SI	8S1	
				AT24C01A-10MI	8M	
				AT24C01A-10TI	8T	
10	1500	4	100	AT24C01A-10PC-2.7	8P3	Commercial (0°C to 70°C)
				AT24C01A-10SC-2.7	8S1	
				AT24C01A-10MC-2.7	8M	
				AT24C01A-10TC-2.7	8T	
	1500	4	100	AT24C01A-10PI-2.7	8P3	Industrial (-40°C to 85°C)
				AT24C01A-10SI-2.7	8S1	
				AT24C01A-10MI-2.7	8M	
				AT24C01A-10TI-2.7	8T	

Package Type

8-Lead, 0.118" Wide, Miniature Small Outline Package (MSOP)
8-Lead, 0.300" Wide, Plastic Dual Inline Package (PDIP)
8-Lead, 0.150" Wide, Plastic Gull Wing Small Outline (JEDEC SOIC)
8-Lead, 0.170" Wide, Thin Shrink Small Outline Package (TSSOP)

Options

Standard Operation (4.5V to 5.5V)
Low Voltage (2.7V to 5.5V)
Low Voltage (2.5V to 5.5V)
Low Voltage (1.8V to 5.5V)

AT24C01A Ordering Information (Continued)

t_{WR} (max) (ms)	I_{CC} (max) (μA)	I_{SB} (max) (μA)	f_{MAX} (kHz)	Ordering Code	Package	Operation Range
10	1000	4	100	AT24C01A-10PC-2.5	8P3	Commercial (0°C to 70°C)
				AT24C01A-10SC-2.5	8S1	
				AT24C01A-10MC-2.5	8M	
				AT24C01A-10TC-2.5	8T	
	1000	4	100	AT24C01A-10PI-2.5	8P3	Industrial (-40°C to 85°C)
				AT24C01A-10SI-2.5	8S1	
				AT24C01A-10MI-2.5	8M	
				AT24C01A-10TI-2.5	8T	
10	800	3	100	AT24C01A-10PC-1.8	8P3	Commercial (0°C to 70°C)
				AT24C01A-10SC-1.8	8S1	
				AT24C01A-10MC-1.8	8M	
				AT24C01A-10TC-1.8	8T	
	800	3	100	AT24C01A-10PI-1.8	8P3	Industrial (-40°C to 85°C)
				AT24C01A-10SI-1.8	8S1	
				AT24C01A-10MI-1.8	8M	
				AT24C01A-10TI-1.8	8T	

Package Type	
8M	8-Lead, 0.118" Wide, Miniature Small Outline Package (MSOP)
8P3	8-Lead, 0.300" Wide, Plastic Dual In-line Package (PDIP)
8S1	8-Lead, 0.150" Wide, Plastic Gull Wing Small Outline (JEDEC SOIC)
8T	8-Lead, 0.170" Wide, Thin Shrink Small Outline Package (TSSOP)
Options	
Blank	Standard Operation (4.5V to 5.5V)
2.7	Low Voltage (2.7V to 5.5V)
2.5	Low Voltage (2.5V to 5.5V)
1.8	Low Voltage (1.8V to 5.5V)





AT24C02 Ordering Information

I_{CC} (max) (mA)	I_{CC} (max) (μ A)	I_{SB} (max) (μ A)	f_{MAX} (kHz)	Ordering Code	Package	Operation Range
10	3000	18	400	AT24C02-10PC	8P3	Commercial (0°C to 70°C)
				AT24C02N-10SC	8S1	
				AT24C02-10SC	14S	
				AT24C02-10MC	8M	
				AT24C02-10TC	8T	
	3000	18	400	AT24C02-10PI	8P3	Industrial (-40°C to 85°C)
				AT24C02N-10SI	8S1	
				AT24C02-10SI	14S	
				AT24C02-10MI	8M	
				AT24C02-10TI	8T	
10	1500	4	100	AT24C02-10PC-2.7	8P3	Commercial (0°C to 70°C)
				AT24C02N-10SC-2.7	8S1	
				AT24C02-10SC-2.7	14S	
				AT24C02-10MC-2.7	8M	
				AT24C02-10TC-2.7	8T	
	1500	4	100	AT24C02-10PI-2.7	8P3	Industrial (-40°C to 85°C)
				AT24C02N-10SI-2.7	8S1	
				AT24C02-10SI-2.7	14S	
				AT24C02-10MI-2.7	8M	
				AT24C02-10TI-2.7	8T	

Package Type

8-Lead, 0.118" Wide, Miniature Small Outline Package (MSOP)
8-Lead, 0.300" Wide, Plastic Dual Inline Package (PDIP)
8-Lead, 0.150" Wide, Plastic Gull Wing Small Outline (JEDEC SOIC)
8-Lead, 0.170" Wide, Thin Shrink Small Outline Package (TSSOP)
14-Lead, 0.150" Wide, Plastic Gull Wing Small Outline (JEDEC SOIC)

Options

Standard Operation (4.5V to 5.5V)
Low Voltage (2.7V to 5.5V)
Low Voltage (2.5V to 5.5V)
Low Voltage (1.8V to 5.5V)

AT24C01A/02/04/08/16

AT24C02 Ordering Information (Continued)

t_{WR} (max) (ms)	I_{CC} (max) (μ A)	I_{SB} (max) (μ A)	f_{MAX} (kHz)	Ordering Code	Package	Operation Range
10	1000	4	100	AT24C02-10PC-2.5	8P3	Commercial (0°C to 70°C)
				AT24C02N-10SC-2.5	8S1	
				AT24C02-10SC-2.5	14S	
				AT24C02-10MC-2.5	8M	
				AT24C02-10TC-2.5	8T	
10	1000	4	100	AT24C02-10PI-2.5	8P3	Industrial (-40°C to 85°C)
				AT24C02N-10SI-2.5	8S1	
				AT24C02-10SI-2.5	14S	
				AT24C02-10MI-2.5	8M	
				AT24C02-10TI-2.5	8T	
10	800	3	100	AT24C02-10PC-1.8	8P3	Commercial (0°C to 70°C)
				AT24C02N-10SC-1.8	8S1	
				AT24C02-10SC-1.8	14S	
				AT24C02-10MC-1.8	8M	
				AT24C02-10TC-1.8	8T	
10	800	3	100	AT24C02-10PI-1.8	8P3	Industrial (-40°C to 85°C)
				AT24C02N-10SI-1.8	8S1	
				AT24C02-10SI-1.8	14S	
				AT24C02-10MI-1.8	8M	
				AT24C02-10TI-1.8	8T	

Package Type

8M	8-Lead, 0.118" Wide, Miniature Small Outline Package (MSOP)
8P3	8-Lead, 0.300" Wide, Plastic Dual Inline Package (PDIP)
8S1	8-Lead, 0.150" Wide, Plastic Gull Wing Small Outline (JEDEC SOIC)
8T	8-Lead, 0.170" Wide, Thin Shrink Small Outline Package (TSSOP)
14S	14-Lead, 0.150" Wide, Plastic Gull Wing Small Outline (JEDEC SOIC)

Options

Blank	Standard Operation (4.5V to 5.5V)
-2.7	Low Voltage (2.7V to 5.5V)
-2.5	Low Voltage (2.5V to 5.5V)
-1.8	Low Voltage (1.8V to 5.5V)





4C04 Ordering Information

(max) ns)	I _{CC} (max) (μA)	I _{SB} (max) (μA)	f _{MAX} (kHz)	Ordering Code	Package	Operation Range
10	3000	18	400	AT24C04-10PC	8P3	Commercial (0°C to 70°C)
				AT24C04N-10SC	8S1	
				AT24C04-10SC	14S	
				AT24C04-10TC	8T	
	3000	18	400	AT24C04-10PI	8P3	Industrial (-40°C to 85°C)
				AT24C04N-10SI	8S1	
				AT24C04-10SI	14S	
				AT24C04-10TI	8T	
10	1500	4	100	AT24C04-10PC-2.7	8P3	Commercial (0°C to 70°C)
				AT24C04N-10SC-2.7	8S1	
				AT24C04-10SC-2.7	14S	
				AT24C04-10TC-2.7	8T	
	1500	4	100	AT24C04-10PI-2.7	8P3	Industrial (-40°C to 85°C)
				AT24C04N-10SI-2.7	8S1	
				AT24C04-10SI-2.7	14S	
				AT24C04-10TI-2.7	8T	

Package Type

- 8-Lead, 0.300" Wide, Plastic Dual Inline Package (PDIP)
- 8-Lead, 0.150" Wide, Plastic Gull Wing Small Outline (JEDEC SOIC)
- 8-Lead, 0.170" Wide, Thin Shrink Small Outline Package (TSSOP)
- 14-Lead, 0.150" Wide, Plastic Gull Wing Small Outline (JEDEC SOIC)

Options

- Standard Operation (4.5V to 5.5V)
- Low Voltage (2.7V to 5.5V)
- Low Voltage (2.5V to 5.5V)
- Low Voltage (1.8V to 5.5V)

T24C04 Ordering Information (Continued)

t_{WR} (max) (ms)	I_{CC} (max) (μA)	I_{SB} (max) (μA)	f_{MAX} (kHz)	Ordering Code	Package	Operation Range
10	1000	4	100	AT24C04-10PC-2.5	8P3	Commercial (0°C to 70°C)
				AT24C04N-10SC-2.5	8S1	
				AT24C04-10SC-2.5	14S	
				AT24C04-10TC-2.5	8T	
	1000	4	100	AT24C04-10PI-2.5	8P3	Industrial (-40°C to 85°C)
				AT24C04N-10SI-2.5	8S1	
				AT24C04-10SI-2.5	14S	
				AT24C04-10TI-2.5	8T	
10	800	3	100	AT24C04-10PC-1.8	8P3	Commercial (0°C to 70°C)
				AT24C04N-10SC-1.8	8S1	
				AT24C04-10SC-1.8	14S	
				AT24C04-10TC-1.8	8T	
	800	3	100	AT24C04-10PI-1.8	8P3	Industrial (-40°C to 85°C)
				AT24C04N-10SI-1.8	8S1	
				AT24C04-10SI-1.8	14S	
				AT24C04-10TI-1.8	8T	

Package Type

8P3	8-Lead, 0.300" Wide, Plastic Dual Inline Package (PDIP)
8S1	8-Lead, 0.150" Wide, Plastic Gull Wing Small Outline (JEDEC SOIC)
8T	8-Lead, 0.170" Wide, Thin Shrink Small Outline Package (TSSOP)
14S	14-Lead, 0.150" Wide, Plastic Gull Wing Small Outline (JEDEC SOIC)

Options

Blank	Standard Operation (4.5V to 5.5V)
-2.7	Low Voltage (2.7V to 5.5V)
-2.5	Low Voltage (2.5V to 5.5V)
-1.8	Low Voltage (1.8V to 5.5V)





4C08 Ordering Information

t _{prop} (max) (ns)	I _{CC} (max) (μA)	I _{SB} (max) (μA)	f _{MAX} (kHz)	Ordering Code	Package	Operation Range
10	3000	18	400	AT24C08-10PC	8P3	Commercial (0°C to 70°C)
				AT24C08N-10SC	8S1	
				AT24C08-10SC	14S	
				AT24C08-10TC	8T	
	3000	18	400	AT24C08-10PI	8P3	Industrial (-40°C to 85°C)
				AT24C08N-10SI	8S1	
				AT24C08-10SI	14S	
				AT24C08-10TI	8T	
10	1500	4	100	AT24C08-10PC-2.7	8P3	Commercial (0°C to 70°C)
				AT24C08N-10SC-2.7	8S1	
				AT24C08-10SC-2.7	14S	
				AT24C08-10TC-2.7	8T	
	1500	4	100	AT24C08-10PI-2.7	8P3	Industrial (-40°C to 85°C)
				AT24C08N-10SI-2.7	8S1	
				AT24C08-10SI-2.7	14S	
				AT24C08-10TI-2.7	8T	

Package Type	
	8-Lead, 0.300" Wide, Plastic Dual Inline Package (PDIP)
	8-Lead, 0.150" Wide, Plastic Gull Wing Small Outline (JEDEC SOIC)
	8-Lead, 0.170" Wide, Thin Shrink Small Outline Package (TSSOP)
	14-Lead, 0.150" Wide, Plastic Gull Wing Small Outline (JEDEC SOIC)
Options	
nk	Standard Operation (4.5V to 5.5V)
	Low Voltage (2.7V to 5.5V)
	Low Voltage (2.5V to 5.5V)
	Low Voltage (1.8V to 5.5V)

AT24C08 Ordering Information (Continued)

t_{WR} (max) (ms)	I_{CC} (max) (μA)	I_{SB} (max) (μA)	f_{MAX} (kHz)	Ordering Code	Package	Operation Range
10	1000	4	100	AT24C08-10PC-2.5	8P3	Commercial (0°C to 70°C)
				AT24C08N-10SC-2.5	8S1	
				AT24C08-10SC-2.5	14S	
				AT24C08-10TC-2.5	8T	
10	1000	4	100	AT24C08-10PI-2.5	8P3	Industrial (-40°C to 85°C)
				AT24C08N-10SI-2.5	8S1	
				AT24C08-10SI-2.5	14S	
				AT24C08-10TI-2.5	8T	
10	800	3	100	AT24C08-10PC-1.8	8P3	Commercial (0°C to 70°C)
				AT24C08N-10SC-1.8	8S1	
				AT24C08-10SC-1.8	14S	
				AT24C08-10TC-1.8	8T	
10	800	3	100	AT24C08-10PI-1.8	8P3	Industrial (-40°C to 85°C)
				AT24C08N-10SI-1.8	8S1	
				AT24C08-10SI-1.8	14S	
				AT24C08-10TI-1.8	8T	

Package Type

8P3	8-Lead, 0.300" Wide, Plastic Dual Inline Package (PDIP)
8S1	8-Lead, 0.150" Wide, Plastic Gull Wing Small Outline (JEDEC SOIC)
8T	8-Lead, 0.170" Wide, Thin Shrink Small Outline Package (TSSOP)
14S	14-Lead, 0.150" Wide, Plastic Gull Wing Small Outline (JEDEC SOIC)

Options

Blank	Standard Operation (4.5V to 5.5V)
-2.7	Low Voltage (2.7V to 5.5V)
-2.5	Low Voltage (2.5V to 5.5V)
-1.8	Low Voltage (1.8V to 5.5V)





AT24C16 Ordering Information

t_{max} (ms)	I_{CC} (max) (μA)	I_{SB} (max) (μA)	f_{MAX} (kHz)	Ordering Code	Package	Operation Range
10	3000	18	400	AT24C16-10PC	8P3	Commercial (0°C to 70°C)
				AT24C16N-10SC	8S1	
				AT24C16-10SC	14S	
				AT24C16-10TC	8T	
	3000	18	400	AT24C16-10PI	8P3	Industrial (-40°C to 85°C)
				AT24C16N-10SI	8S1	
				AT24C16-10SI	14S	
				AT24C16-10TI	8T	
10	1500	4	100	AT24C16-10PC-2.7	8P3	Commercial (0°C to 70°C)
				AT24C16N-10SC-2.7	8S1	
				AT24C16-10SC-2.7	14S	
				AT24C16-10TC-2.7	8T	
	1500	4	100	AT24C16-10PI-2.7	8P3	Industrial (-40°C to 85°C)
				AT24C16N-10SI-2.7	8S1	
				AT24C16-10SI-2.7	14S	
				AT24C16-10TI-2.7	8T	

Package Type

8-Lead, 0.300" Wide, Plastic Dual Inline Package (PDIP)
8-Lead, 0.150" Wide, Plastic Gull Wing Small Outline (JEDEC SOIC)
8-Lead, 0.170" Wide, Thin Shrink Small Outline Package (TSSOP)
14-Lead, 0.150" Wide, Plastic Gull Wing Small Outline (JEDEC SOIC)

Options

Standard Operation (4.5V to 5.5V)
Low Voltage (2.7V to 5.5V)
Low Voltage (2.5V to 5.5V)
Low Voltage (1.8V to 5.5V)

AT24C01A/02/04/08/16

AT24C16 Ordering Information (Continued)

t_{WR} (max) (ms)	I_{CC} (max) (μ A)	I_{SB} (max) (μ A)	f_{MAX} (kHz)	Ordering Code	Package	Operation Range
10	1000	4	100	AT24C16-10PC-2.5	8P3	Commercial (0°C to 70°C)
				AT24C16N-10SC-2.5	8S1	
				AT24C16-10SC-2.5	14S	
				AT24C16-10TC-2.5	8T	
	1000	4	100	AT24C16-10PI-2.5	8P3	Industrial (-40°C to 85°C)
				AT24C16N-10SI-2.5	8S1	
				AT24C16-10SI-2.5	14S	
				AT24C16-10TI-2.5	8T	
10	800	3	100	AT24C16-10PC-1.8	8P3	Commercial (0°C to 70°C)
				AT24C16N-10SC-1.8	8S1	
				AT24C16-10SC-1.8	14S	
				AT24C16-10TC-1.8	8T	
	800	3	100	AT24C16-10PI-1.8	8P3	Industrial (-40°C to 85°C)
				AT24C16N-10SI-1.8	8S1	
				AT24C16-10SI-1.8	14S	
				AT24C16-10TI-1.8	8T	

Package Type

8P3	8-Lead, 0.300" Wide, Plastic Dual Inline Package (PDIP)
8S1	8-Lead, 0.150" Wide, Plastic Gull Wing Small Outline (JEDEC SOIC)
8T	8-Lead, 0.170" Wide, Thin Shrink Small Outline Package (TSSOP)
14S	14-Lead, 0.150" Wide, Plastic Gull Wing Small Outline (JEDEC SOIC)

Options

Blank	Standard Operation (4.5V to 5.5V)
-2.7	Low Voltage (2.7V to 5.5V)
-2.5	Low Voltage (2.5V to 5.5V)
-1.8	Low Voltage (1.8V to 5.5V)



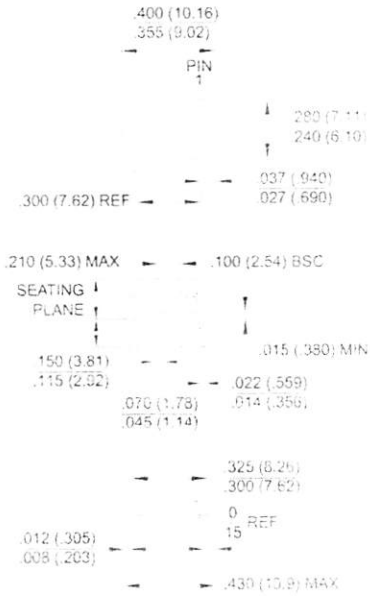


Packaging Information

P3, 8-Lead, 0.300" Wide, Plastic Dual Inline Package (PDIP)

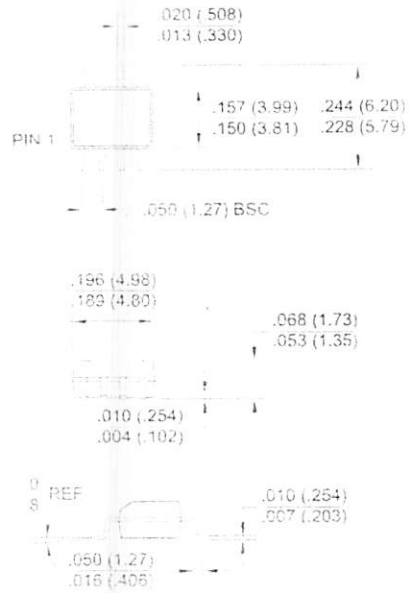
Dimensions in Inches and (Millimeters)

JEDEC STANDARD MS-001 BA



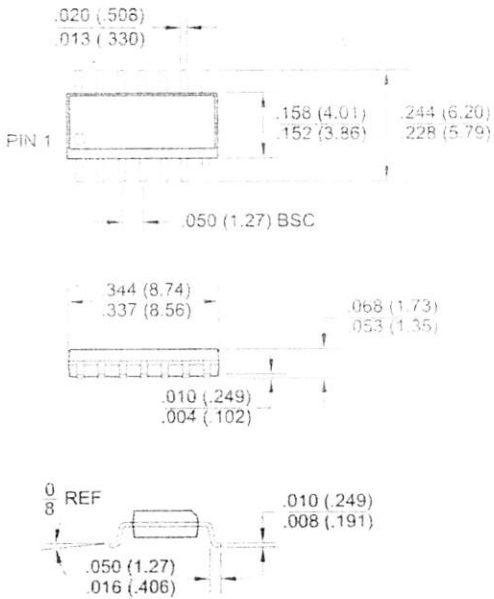
8S1, 8-Lead, 0.150" Wide, Plastic Gull Wing Small Outline (JEDEC SOIC)

Dimensions in Inches and (Millimeters)



4S, 14-Lead, 0.150" Wide, Plastic Gull Wing Small Outline (SOIC)

Dimensions in Inches and (Millimeters)



8M, 8-Lead, 0.118" Wide, Miniature Small Outline (MSOP)

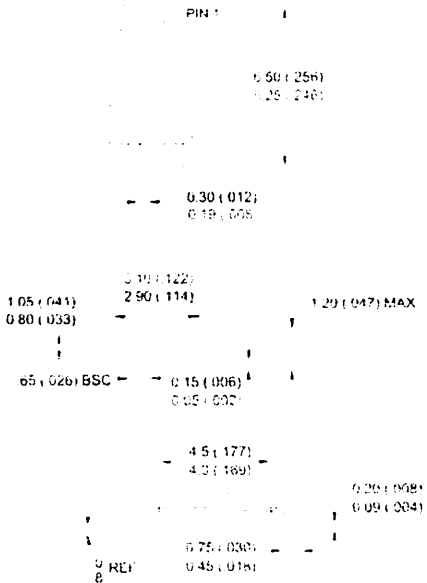
Dimensions in Millimeters and (Inches)



* Controlling dimension: millimeters

Packaging Information

8T, 8-Lead, Plastic Thin Small Outline Package (TSOP)
 Dimensions in Millimeters and (inches)*



*Controlling dimension: millimeters





Atmel Headquarters

Corporate Headquarters
25 Orchard Parkway
Framingham, MA 01901
TEL (408) 441-0311
FAX (408) 487-2600

Europe
Atmel U.K., Ltd
The Malvern Business Centre
The Malvern Way
Wotton Bassett, Surrey GU15 3YL
England
TEL (44) 1276-686677
FAX (44) 1276-686697

Atmel Asia, Ltd
Room 1219
The Metropole Golden Plaza
100 Mody Road
Tsimshatsui East
Kowloon, Hong Kong
TEL (852) 27219778
FAX (852) 27221369

Atmel Japan K.K.
The Onetsu Shinkawa Bldg., 9F
24-8 Shinkawa
Shinjuku-ku, Tokyo 104-0033
Japan
TEL (81) 3-3523-3551
FAX (81) 3-3523-7581

Atmel Operations

Atmel Colorado Springs
1150 E. Cheyenne Mtn. Blvd.
Colorado Springs, CO 80906
TEL (719) 576-3300
FAX (719) 540-1759

Atmel Rousset
Zone Industrielle
13106 Rousset Cedex, France
TEL (33) 4 42 53 60 00
FAX (33) 4 42 53 60 01

Fax-on-Demand

North America:
1-(800) 292-8635

International:
1-(408) 441-0732

e-mail
literature@atmel.com

Web Site
<http://www.atmel.com>

BBS
1-(408) 436-4309

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FAIRCHILD
SEMICONDUCTOR

SS9013

1W Output Amplifier of Portable Radios in Class B Push-pull Operation.

- High total power dissipation. ($P_T=625mW$)
- High Collector Current. ($I_C=500mA$)
- Complementary to SS9012
- Excellent h_{FE} linearity.

TO-92

1. Emitter 2. Base 3. Collector

NPN Epitaxial Silicon Transistor

Absolute Maximum Ratings $T_a=25^\circ C$ unless otherwise noted

Symbol	Parameter	Ratings	Units
V_{CBO}	Collector-Base Voltage	40	V
V_{CEO}	Collector-Emitter Voltage	20	V
V_{EBO}	Emitter-Base Voltage	5	V
I_C	Collector Current	500	mA
P_C	Collector Power Dissipation	625	mW
T_J	Junction Temperature	150	$^\circ C$
T_{STG}	Storage Temperature	-55 ~ 150	$^\circ C$

Electrical Characteristics $T_a=25^\circ C$ unless otherwise noted

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Units
BV_{CBO}	Collector-Base Breakdown Voltage	$I_C = 100\mu A, I_E = 0$	40			V
BV_{CEO}	Collector-Emitter Breakdown Voltage	$I_C = 1mA, I_B = 0$	20			V
BV_{EBO}	Emitter-Base Breakdown Voltage	$I_E = 100\mu A, I_C = 0$	5			V
I_{CBO}	Collector Cut-off Current	$V_{CB} = 25V, I_E = 0$			100	nA
I_{EBO}	Emitter Cut-off Current	$V_{EB} = 3V, I_C = 0$			100	nA
h_{FE1}	DC Current Gain	$V_{CE} = 1V, I_C = 50mA$	64	120	202	
h_{FE2}		$V_{CE} = 1V, I_C = 500mA$	40	120		
$V_{CE(sat)}$	Collector-Emitter Saturation Voltage	$I_C = 500mA, I_B = 50mA$		0.16	0.6	V
$V_{BE(sat)}$	Base-Emitter Saturation Voltage	$I_C = 500mA, I_B = 50mA$		0.91	1.2	V
$V_{BE(on)}$	Base-Emitter On Voltage	$V_{CE} = 1V, I_C = 10mA$	0.6	0.67	0.7	V

h_{FE} Classification

Classification	D	E	F	G	H
h_{FE1}	64 ~ 91	78 ~ 112	96 ~ 135	112 ~ 166	144 ~ 202

Typical Characteristics

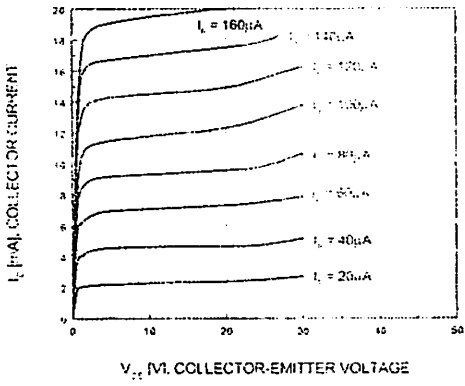


Figure 1. Static Characteristic

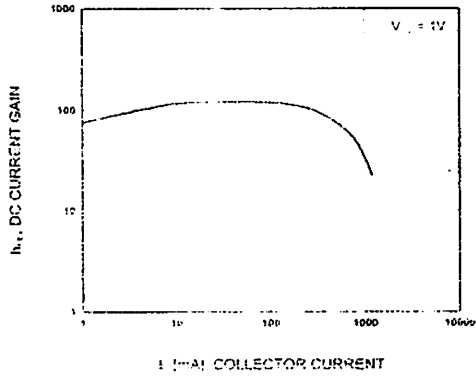


Figure 2. DC current Gain

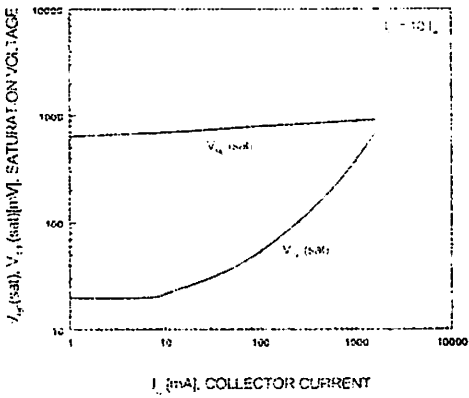


Figure 3. Base-Emitter Saturation Voltage
Collector-Emitter Saturation Voltage

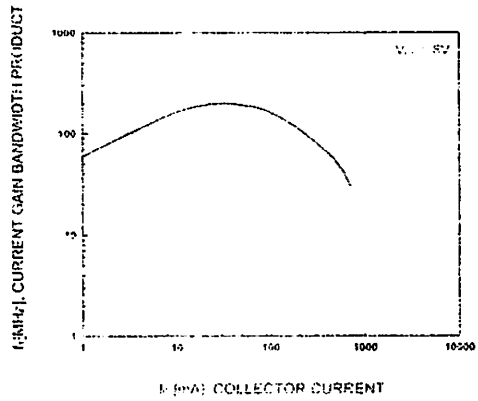
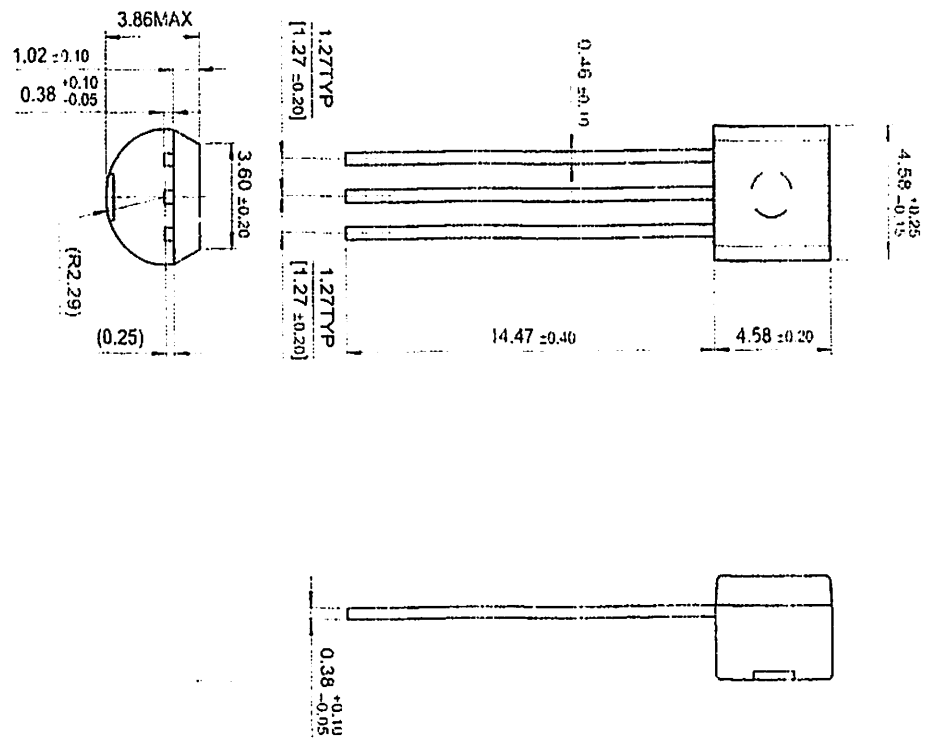


Figure 4. Current Gain Bandwidth Product

Package Dimensions

TO-92



Dimensions in Millimeters

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ChoiFET™	FASTr™	MicroFET™	PowerTrench™	SuperSOT™-6
CROSSVOLT™	FRFET™	MicroPak™	QFET™	SuperSOT™-8
DOME™	GlobalOptoisolator™	MICROWIRE™	QS™	SyncFET™
EcoSPARK™	GTO™	MSX™	QT Optoelectronics™	TinyLogic™
ECMOS™	HiSeCT™	MSXPro™	Quiet Series™	TruTranslation™
EnSigna™	IC™	OCX™	RapidConfigure™	UHC™
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The Power Franchise™	OPTOLOGIC®	OPTOPLANAR™	SILENT SWITCHER®	VCX™
Programmable Active Droop™			SMART START™	

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2. A critical component is any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

PRODUCT STATUS DEFINITIONS

Definition of Terms

Datasheet Identification	Product Status	Definition
Advance Information	Formative or In Design	This datasheet contains the design specifications for product development. Specifications may change in any manner without notice.
Preliminary	First Production	This datasheet contains preliminary data, and supplementary data will be published at a later date. Fairchild Semiconductor reserves the right to make changes at any time without notice in order to improve design.
No Identification Needed	Full Production	This datasheet contains final specifications. Fairchild Semiconductor reserves the right to make changes at any time without notice in order to improve design.
Obsolete	Not In Production	This datasheet contains specifications on a product that has been discontinued by Fairchild semiconductor. The datasheet is printed for reference information only.

1W Output Amplifier of Potable Radios in Class B Push-pull Operation.

- High total power dissipation. ($P_T=625mW$)
- High Collector Current. ($I_C = -500mA$)
- Complementary to SS9013
- Excellent h_{FE} linearity.

TO-92
1. Emitter 2. Base 3. Collector

PNP Epitaxial Silicon Transistor

Absolute Maximum Ratings $T_a=25^\circ C$ unless otherwise noted

Symbol	Parameter	Ratings	Units
V_{CBO}	Collector-Base Voltage	-40	V
V_{CEO}	Collector-Emitter Voltage	-20	V
V_{EBO}	Emitter-Base Voltage	-5	V
I_C	Collector Current	-500	mA
P_C	Collector Power Dissipation	625	mW
T_J	Junction Temperature	150	$^\circ C$
T_{STG}	Storage Temperature	-55 ~ 150	$^\circ C$

Electrical Characteristics $T_a=25^\circ C$ unless otherwise noted

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Units
BV_{CBO}	Collector-Base Breakdown Voltage	$I_C = -100\mu A, I_E = 0$	-40			V
BV_{CEO}	Collector-Emitter Breakdown Voltage	$I_C = -1mA, I_B = 0$	-20			V
BV_{EBO}	Emitter-Base Breakdown Voltage	$I_E = -100\mu A, I_C = 0$	-5			V
I_{CBO}	Collector Cut-off Current	$V_{CB} = -25V, I_E = 0$			-100	nA
I_{EBO}	Emitter Cut-off Current	$V_{EB} = -3V, I_C = 0$			-100	nA
h_{FE1}	DC Current Gain	$V_{CE} = -1V, I_C = -50mA$	64	120	202	
h_{FE2}		$V_{CE} = -1V, I_C = -500mA$	40	90		
$V_{CE(sat)}$	Collector-Emitter Saturation Voltage	$I_C = -500mA, I_B = -50mA$		-0.18	-0.6	V
$V_{BE(sat)}$	Base-Emitter Saturation Voltage	$I_C = -500mA, I_B = -50mA$		-0.95	-1.2	V
$V_{BE(on)}$	Base-Emitter On Voltage	$V_{CE} = -1V, I_C = -10mA$	-0.6	-0.67	-0.7	V

h_{FE} Classification

Classification	D	E	F	G	H
h_{FE1}	64 ~ 91	78 ~ 112	96 ~ 135	112 ~ 166	144 ~ 202

Typical Characteristics

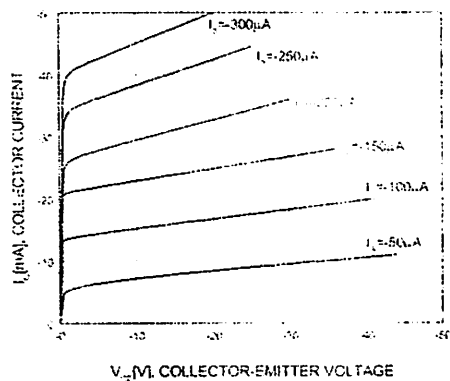


Figure 1. Static Characteristic

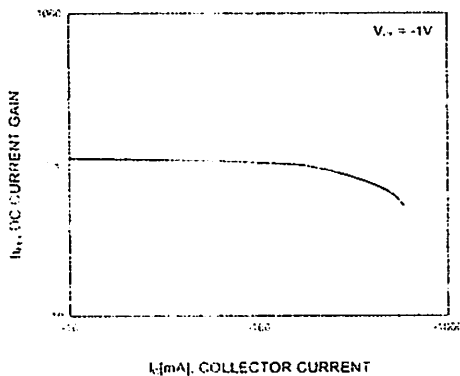


Figure 2. DC current Gain

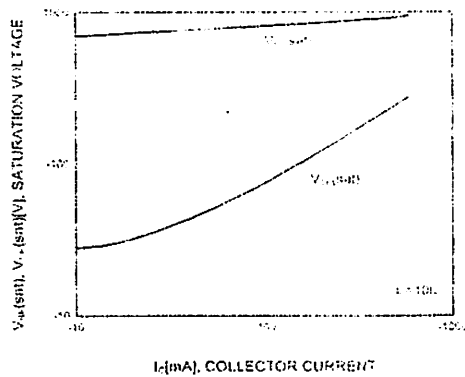


Figure 3. Base-Emitter Saturation Voltage
Collector-Emitter Saturation Voltage

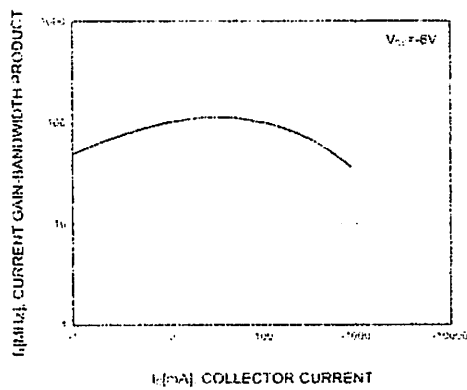
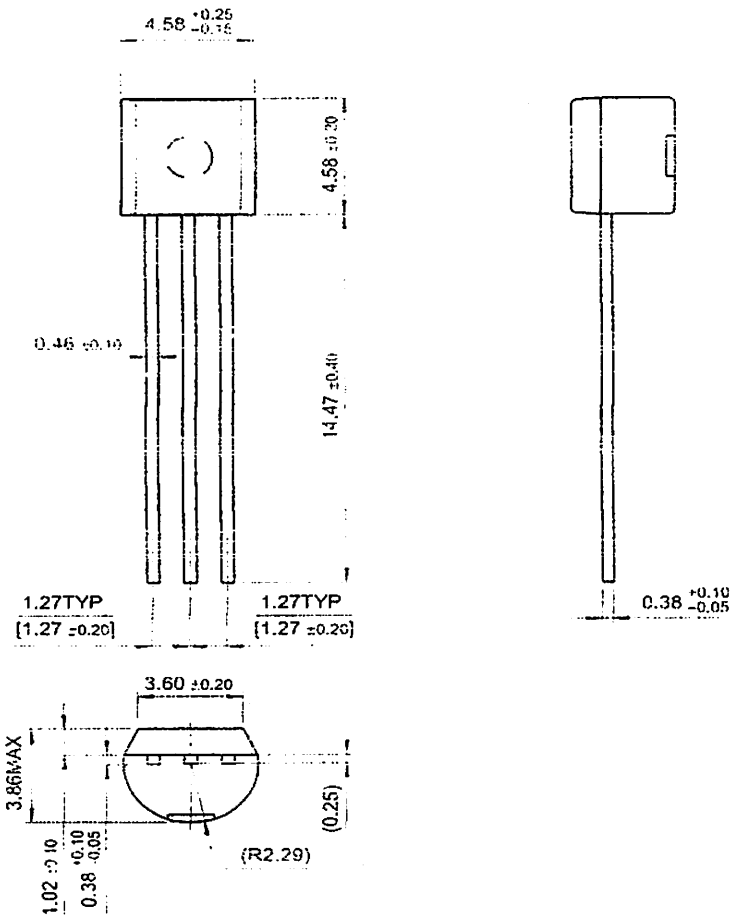


Figure 4. Current Gain Bandwidth Product

Package Dimensions

TO-92



Dimensions in Millimeters

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EnSigna™	I ² C™	OCX™	RapidConfigure™	UHC™
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2. A critical component is any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

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