SKRIPSI

PERANCANGAN DAN PEMBUATAN AMPEREMETER ARUS SEARAH DIGITAL *HALL EFFECT* SENSOR DENGAN OUTPUT SUARA

Disusun Oleh :

ADI DWI CAHYANTO
06.12.227

JURUSAN TEKNIK ELEKTRO S-1
KONSENTRASI TEKNIK ELEKTRONIKA
FAKULTAS TEKNOLOGI INDUSTRI
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2012

LEMBAR PERSETUJUAN

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Disusun dan Diajukan Sebagai Salah Satu Syarat Untuk Memperoleh Gelar Sarjana Teknik Elektronika Strata Satu (S-1)

Disusun oleh :

ADI DWI CAHYANTO

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ABSTRAK

"PERANCANGAN DAN PEMBUATAN AMPEREMETER ARUS SEARAH DIGITAL *HALL EFFECT* SENSOR DENGAN OUTPUT SUARA "

Adi Dwi Cahyanto,NIM 06.12.227
Dosen Pembimbing : M. Ibrahim Ashari,ST, MT dan Ir. Eko Nurcahyo

ABSTRAK

Pengukuran merupakan hal yang penting dalam berbagai aktivitas, hal ini berkaitan dengan kebutuhan untuk mengetahui nilai dari variable yang diukur untuk menentukan suatu tindak lanjut. Tidak semua variable dapat ditanggapi langsung oleh indra manusia, sehingga diperlukan suatu alat untuk mentranformasikan memalui sebuah fenomena fisis agar dapat dimengerti.

Skripsi ini bertujuan untuk membuat amperemeter arus searah digital dengan *Hall Effect* sensor yang memanfaatkan medan magnet akibat arus listrik. Dimana alat ukur ini memiliki pembacaan dengan ketepatan yang tinggi, karena didalamnya terdapat rangkaian low-offset linear Hall dengan satu lintasan yang terbuat dari tembaga. cara kerja sensor ini adalah arus yang dibaca mengalir melalui kabel tembaga yang terdapat didalamnya yang menghasilkan medan magnet yang di tangkap oleh integrated Hall IC dan diubah menjadi tegangan proporsional. Medan yang diterima oleh sensor *Hall Effect* akan diteruskan ke system mikrokontroller dan kemudian hasilnya ditampilkan pada penampil LCD dan suara yang terekam di ISD2590.

Kata kunci : Amperemeter Digital, Speaker.

KATA PENGANTAR

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Penulis telah berusaha semaksimal mungkin dan menyadari sepenuhnya akan keterbatasan pengetahuan dalam menyelesaikan laporan ini. Untuk itu penyusun mengharapkan saran dan kritik yang membangun dari pembaca demi kesempurnaan laporan ini.

Harapan penulis semoga laporan skripsi ini memberikan manfaat bagi perkembangan ilmu pengetahuan dan pembaca.

Malang, Februari 2012

Penulis

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BAB I
PENDAHULUAN

1.1. Latar Belakang

Manusia dalam melakukan aktivitas kehidupan sering melakukan pengukuran, hal ini berkaitan kebutuhan manusia untuk mengetahui nilai atau besaran dari variabel yang diukur. Nilai ini dipergunakan untuk melakukan perhitungan dan perencanaan dalam melakukan aktivitasnya.

Tidak semua variable dapat ditanggapi langsung oleh panca indra manusia, karena keterbatasan ini maka diperlukan suatu instrument yang dapat melakukan transformasi melalui suatu fenomena fisis sehingga memungkinkan pengamatan melalui panca indra, sebagai contoh besaran arus listrik ditransformasikan dalam besaran mekanis perubahan sudut misalnya, perubahan sudut ini berhubungan langsung besaran arus listrik yang diamati, perubahan sudut menjadi ukuran besaran arus listrik yang diukur.

Instrument adalah sebuah alat yang digunakan untuk menentukan nilai atau besaran dari suatu kuantitas atau variable. Pada sistem elektronik instrumentasi didasarkan pada prinsip-prinsip elektronika. Sistem ini dapat berupa sistem yang sederhana sampai pada sistem yang rumit namun dalam pengembangannya selalu mengarah pada keakuratan yang lebih baik. Ketelitian,sensitifitas dan resolusi pengukuran adalah hal yang sangat perlu diperhatikan,demikian juga sebab terjadinya kesalahan dalam pengukuran.

Metode pengukuran arus pada awalnya menggunakan galvanometer pegas,metode ini merupakan pelopor dari instrumentasi pegas. Pengukuran ini dapat dilakukan pada arus searah, dan pada pengukuran arus bolak-balik diperlukan beberapa penyesuaian agar metode ini dapat bekerja.

Cara pengukuran arus dengan instrument pegas memiliki kelemahan karena adanya resistansi dalam dari perangkat galvanometer yang akan mempengaruhi akurasi pengukuran terutama pada nilai arus yang kecil. Dari kelemahan ini direncanakan alternative untuk merancang alat ukur arus searah digital dengan *hall effect* sensor yang memanfaatkan medan magnet akibat arus listrik, sehingga tidak ada rangkaian yang terhubung secara elektrik antara yang diukur dengan alat ukurnya.

1.2. Tujuan

Tujuan penyusunan skripsi ini adalah merancang amperemeter arus searah yang akurat, mudah digunakan dan dibaca dengan menggunakan sensor *hall effect*.

1.3. Rumusan Masalah

Berdasarkan latar belakang yang ada, dapat dirumuskan permasalahan sebagai berikut :

a) Bagaimana merancang dan membuat amperemeter arus searah digital yang akurat.

b) Bagaimana merancang dan membuat amperemeter arus searah digital dengan metode membaca perubahan medan magnet akibat perubahan arus listrik.

c) Bagaimana merancang dan membuat amperemeter arus searah dengan penampil digital beserta suara.

1.4. Batasan Masalah

Dalam perencanaan dan pembuatan skripsi ini perlu dilakukan pembatasan masalah. Pembatasan masalah yang diajukan dalam skripsi ini antara lain :

a) Menekankan pada perancangan,pembuatan dan pembahasan sistem amperemeter arus searah digital dan suara.

b) Pembatasan arus yang diukur maksimal 5 ampere.

c) Menggunakan baterai sebagai sumber catu daya.

d) Suara yang dihasilkan oleh IC ISD2590

e) Ditampilkan dalam satuan Ampere (A) dua angka di belakang koma (,)

1.5. Metodologi

Metode yang digunakan dalam pembahasan skripsi ini adalah:

1. Studi *literature*

   Mencari referensi–referensi yang berhubungan dengan perencanaan dan pembuatan alat yang akan dibuat.

2. Perancangan Alat

   Sebelum melaksanakan pembuatan terhadap alat, dilakukan perancangan terhadap alat yang meliputi merancang rangkaian keseluruhan alat, serta perancangan terhadap *software*.

3. Pembuatan Alat.

   Pada tahap ini realisasi alat yang dibuat, dilakukan perakitan sistem terhadap seluruh hasil rancangan yang telah dibuat.

4. Pengujian Alat

   Untuk mengetahui cara kerja alat, maka dilakukan pengujian secara keseluruhan.

5. Pengolahan Data

   Mengolah data dan menganalisa hasil pengujian alat untuk membuat kesimpulan.

1.6. Sistematika Penulisan

Sistematika pembahasan perancangan dan pembuatan Amperemeter digital ini perincianya adalah sebagai berikut:

BAB I : PENDAHULUAN

Berisi latar belakang, perumusan masalah, batasan masalah dan tujuan.

BAB II : LANDASAN TEORI

Berisi teori-teori yang menunjang dalam proses pembuatan tugas akhir ini.

BAB III : METODOLOGI

Berisi tentang metode yang menjelaskan tentang sistematika berfikir dalam proses analisis dan perancangan.

BAB IV : PERENCANAAN ALAT

Berisi tentang rancangan system yang membahas bagian yang demi bagian penyusunan system baik perangkat keras maupun perangkat lunak.

BAB V : PENGUJIAN DAN ANALISIS

Berisi tentang pengujian fungsi dari rangakain yang diinginkan dan data hasil pengujian.

BAB VI : PENUTUP

Berisi tentang kesimpulan dan saran-saran tentang pengembangan perancang rangkaian selanjutnya.

BAB II
LANDASAN TEORI

2.1. Pendahuluan

Medan magnet atau bias dikatakan sebagai induksi magnetik sering disebut dengan berbagai nama: rapat fluks magnetik, kuat medan magnetik, atau intensitas medan magnet. Induksi magnetik termasuk *besaran vector* karena memiliki *besar* dan *arah*.

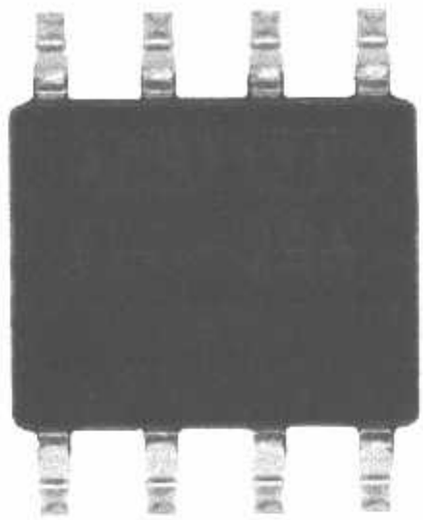
Dua ilmuwan pertama kali menyelidiki besar induksi magnetik yang ditimbulkan oleh kawat berarus adalah Biot dan Savart. Suatu daerah disekitar magnet yang masih memungkinkan terjadi daya tarik akibat magnet dikatakan sebagai medan magnet.

Pendeteksian perubahan kekuatan medan magnet cukup mudah dan tidak memerlukan apapun selain sebuah induktor yang berfungsi sebagai sensornya. Kelemahan dari detektor dengan menggunakan induktor adalah kekuatan medan magnet yang statis (kekuatan medan magnetnya tidak berubah) tidak dapat dideteksi. Oleh sebab itu diperlukan cara yang lain untuk mendeteksinya yaitu dengan sensor yang dinamakan dengan "*hall effect*" sensor. Sensor ini terdiri dari sebuah lapisan silikon yang berfungsi untuk mengalirkan arus listrik.

Sensor *hall effect* ini terdiri dari sebuah lapisan silikon dan dua buah elektroda pada masing-masing sisi silikon. Hal ini akan menghasilkan perbedaan tegangan pada outputnya ketika lapisan silikon ini dialiri oleh arus listrik. Tanpa adanya pengaruh dari medan magnet maka arus yang mengalir pada silikon tersebut akan tepat ditengah-tengah silikon dan menghasilkan tegangan yang sama antara elektroda sebelah kiri dan elektroda sebelah kanan, sehingga menghasilkan tegangan beda tegangan 0 volt pada outputnya.

2.2. *Hall Effect* Sensor

Pengukuran arus biasanya membutuhkan sebuah resistor *shunt* yaitu resistor yang dihubungkan secara seri pada beban dan mengubah aliran arus menjadi tegangan. Tegangan tersebut biasanya diumpankan ke *current transformer* terlebih dahulu sebelum masuk ke rangkaian pengkondisi signal.



Gambar.2.1. *Hall Effect* Sensor (ACS712)

Teknologi *Hall effect* yang diterapkan oleh *Allegro* menggantikan fungsi resistor *shunt* dan *current transformer* menjadi sebuah sensor dengan ukuran yang relatif jauh lebih kecil. Aliran arus listrik yang mengakibatkan medan magnet yang menginduksi bagian *dynamic offset cancellation* dari ACS712. bagian ini akan dikuatkan oleh *amplifier* dan melalui *filter* sebelum dikeluarkan melalui kaki 6 dan 7, modul tersebut membantu penggunaan untuk mempermudah instalasi arus ini ke dalam sistem.

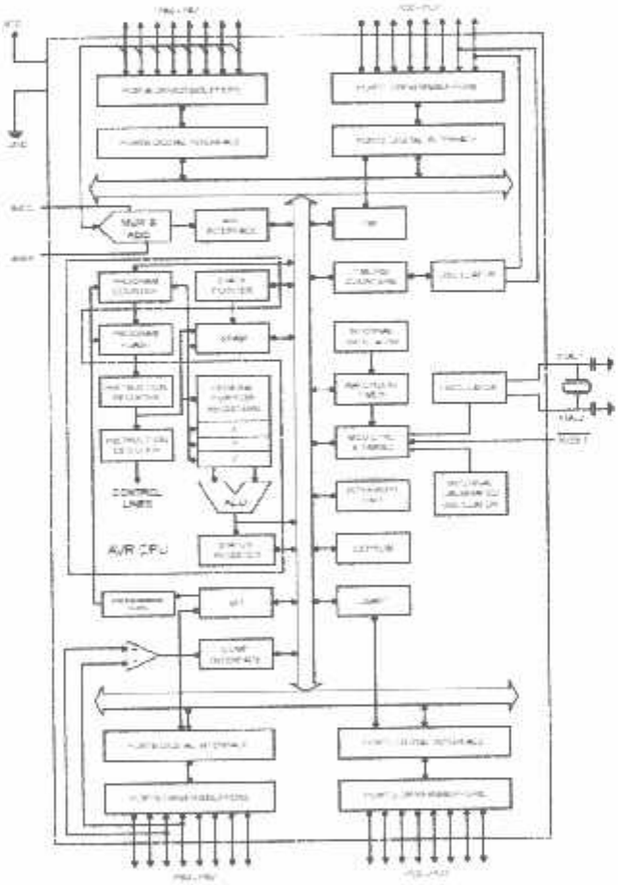
ACS712 adalah *Hall Effect* current sensor. *Hall effect* allegro ACS712 merupakan sensor yang presisi sebagai sensor arus AC atau DC dalam pembacaan arus didalam dunia industri, otomotif, komersil dan sistem-sistem komunikasi. Pada umumnya aplikasi sensor ini biasanya digunakan untuk mengontrol motor, deteksi beban listrik, switched-mode power supplies dan proteksi beban berlebih.

Sensor ini memiliki pembacaan dengan ketepatan yang tinggi, karena didalamnya terdapat rangkaian low-offset linear Hall dengan satu lintasan yang terbuat dari tembaga. cara kerja sensor ini adalah arus yang dibaca mengalir melalui kabel tembaga yang terdapat didalamnya yang menghasilkan medan magnet yang di tangkap oleh integrated Hall IC dan diubah menjadi tegangan proporsional. Ketelitian dalam pembacaan sensor dioptimalkan dengan cara pemasangan komponen yang ada didalamnya antara penghantar yang menghasilkan medan magnet dengan hall transducer secara berdekatan. Persisnya, tegangan proporsional yang rendah akan menstabilkan Bi CMOS Hall IC yang didalamnya yang telah dibuat untuk ketelitian yang tinggi oleh pabrik.

2.3. Mikrokontroller ATmega 16

AVR merupakan seri mikrokontroler CMOS 8-bit buatan Atmel, berbasis arsitektur RISC (Reduced Instruction Set Computer). Hampir semua instruksi dieksekusi dalam satu siklus clock. AVR mempunyai 32 register general-purpose, timer/counter fleksibel dengan mode compare, interrupt internal dan eksternal, serial UART, programmable Watchdog Timer, dan mode power saving, ADC dan PWM internal. AVR juga mempunyai In-System Programmable Flash on-chip yang mengijinkan memori program untuk diprogram ulang dalam sistem menggunakan hubungan serial SPI. ATMega16. ATMega16 mempunyai throughput mendekati 1 MIPS per MHz membuat disainer sistem untuk mengoptimasi konsumsi daya versus kecepatan proses.

2.3.1 Arsitektur Mikrokontroller ATMEGA 16



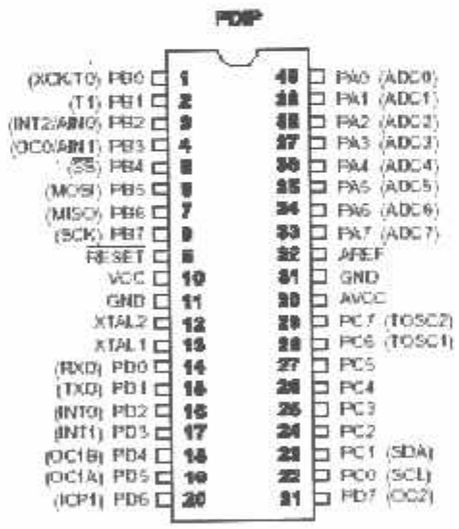
Gambar.2.2 Blok Diagram *Microcontroller* ATMEGA 16

Dari gambar 2.15 tersebut dapat dilihat bahwa ATMega16 memiliki bagian sebagai berikut :

1. Saluran I/O sebanyak 32 buah, yaitu Port A, Port B, Port C dan Port D.
2. ADC bit sebanyak 8 saluran.
3. Tiga buah *Timer/Counter* dengan kemampuan pembanding.
4. CPU yang terdiri atas 32 buah register.
5. *Watchdog Timer* dengan osilator internal.
6. SRAM sebanyak 512 byte.
7. Memori *Flash* sebesar 8 kb dengan kemampuan *Read While Write*.
8. Unit interupsi internal dan eksternal.
9. Port antarmuka SPI.
10. EEPROM sebesar 512 byte yang dapat di program saat operasi.
11. Antarmuka komparator analog.
12. Port USART untuk komunikasi serial.

2.3.2 Konfigurasi Pin ATMega 16

Konfigurasi pin ATMega 16 dapat di lihat pada gambar 2.3:



Gambar.2.3. Pin ATMEGA 16

Dari gambar tersebut dapat dijelaskan secara fungsional konfigurasi pin ATMega16 sebagai berikut :

- **VCC**

  Merupakan pin yang berfungsi sebagai pin masukan catu daya.

- **GND**

  Merupakan pin *ground*.

- **Port A (PA0...PA7)**

  Merupakan pin I/O dua arah dan pin masukan ADC.

- **Port B (PB0...PB7)**

  Merupakan pin I/O dua arah dan pin fungsi khusus, yaitu *Timer/Counter*, komparator analog dan SPI.

- **Port C (PC0...PC7)**

  Merupakan pin I/O dua arah dan pin fungsi khusus,yaitu TWI, komparator analog dan *Timer Oscilator*.

- **Port D (PD0...PD7)**

  Merupakan pin I/O dua arah dan pin fungsi khusus, yaitu komparator analog, interupsi eksternal dan komunikasi serial.

- **RESET**

  Merupakan pin yang digunakan me-reset mikrokontroler.

- **XTAL1 dan XTAL2**

  Merupakan pin masukan *clock* eksternal.

- **AVCC**

  Merupakan pin masukan tegangan untuk ADC.

- **AREF**

  Merupakan pin masukan tegangan referensi ADC.

2.3.3 *SERIAL PHERIPHERAL INTERFACE* (SPI)

Serial Pheripheral interface memungkinkan komunikasi sinkron berkecepatan tinggi antar-mikrokontroler ATMega16 atau antara ATMega16 dengan perangkat lain yang mendukung SPI.

SPI memungkinkan untuk membuat aplikasi multiprosessor. Berikut fitur dari SPI ATMega16:

1. *Full Duplex*, data transfer tak sinkron menggunakan 3 kabel
2. Operasi master atau slave

3. Data transfer awal LSB atau MSB
4. Tujuh bit rate yang dapat diprogram
5. Flag interupsi apabila transmisi data berakhir
6. Flag proteksi untuk kegagalan penulisan
7. *Wake-up from idle mode*
8. Dua kali kecepatan mode SPI master

Antarmuka tersebut memungkinkan sebuah perangkat master berhak memulai dan mengendalikan komunikasi. Perangkat lain yang menerima dan mengirimkan data kembali ke master disebut *slave*.

Inti dari komunikasi SPI adalah register geser 8 bit pada kedua piranti master dan *slave*, serta sinyal *clock* yang dibangkitkan oleh master.

Komunikasi dengan SPI membuthkan 6 jalur sinyal, yaitu:

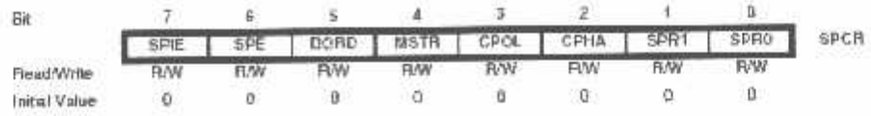
1. SCK (*Serial Clock*);yaitu sinyal clock yang menggeser bit yang hendak dituliskan ke dalam register geser terima AVR lain, dan menggeser bit yang hendak dibaca dari register geser kirim AVR lain.
2. MOSI (*Master Out Slave In*); sinyal bit data serial yang hendak dituliskan dari master ke slave
3. MISO (*Master In Slave Out*); sinyal bit data serial yang hendak dibaca dari *slave* ke master
4. SS' (*Slave Select*/aktif rendah); sinyal untuk memilih dan mengaktifkan *slave*
5. SPI memungkinkan komunikasi dengan beberapa *slave* dengan satu master
6. Pada konfigurasi master, pin SS' harus diset sebagaioutput atau dapat berupa input, tetapi harus berlogika high.

AVR ATMega16 memiliki 3 buah register I/O yang berkaitan dengan komunukasi pemakaian SPI.

1. SPI Data Register (SPDR)

Register SPDR merupakan register baca/tulis yang digunakan untruk transfer data antara register umum dengan register geser SPI.

2. SPI Control Register (SPCR)

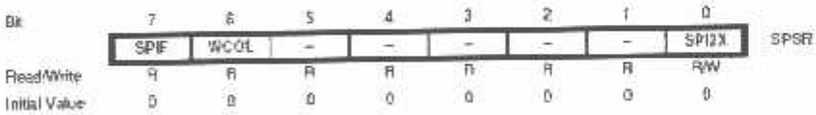


Gambar.2.4. Register kendali SPI

Penjelasan pada register SPCR adalah:

1. SPIE (SPI *Interrupt Enable*); jika bernilai 1 akan membangkitkan interupsi SPI setelah transfer data selesai
2. SPE (SPI *Enable*); untuk mengaktifkan SPI
3. DORD (*Data Order*); jika bernilai 1, maka LSB dikirim terlebih dahulu; jika bernilai 0, maka MSB dikirim dahulu
4. MSTR (*Master/Slave Select*); jika bernilai 1, maka AVR sebagai master; jika bernilai 0, maka AVR sebagai slave
5. CPOL (*Clock Polarity*) dan CPHA (*Clock Phase*); menentukan cara mencuplik data berkaitan dengan pulsa clock.
6. SPR1 dan SPR0 (SPI *Clock Rate Select*); menentukan frekuensi dari sinyal clock SCK.

3. SPI Status Register (SPSR)



Gambar.2.5. Register status SPI

Penjelasan bit pada register SPSR adalah:

1. SPIF (SPI *Interupt Flag*); akan bernilai 1 jika transfer data telah selesai,
2. WCOL (*Write Collision Flag*); akan bernilai 1 jika SPDR diisi ketika transfer data masih berlangsung,

2.3.4 ADC (*Analog Digital Converter*) pada ATMega16

Board AVR yang digunakan menggunakan chip ATMega16. IC ini mempunyai ADC (*analog to digital converter*) internal dengan fitur sebagai berikut :

- 10-bit resolution
- 65-260 µs Conversion Time
- Up to 15 kSPS at Maximum Resolution
- 8 Multiplexed Single Ended Input Channels
- Optional Left Adjusment for ADC Result Readout
- 0 - VCC ADC Input Voltage Range
- Selectable 2.56V ADC reference Voltage
- Free Running or Single Conversion Mode
- ADC Start Conversion by Auto Triggering on Interrupt Sources
- Interrupt on ADC Conversion Complete
- Sleep Mode Noise Canceler

Sinyal input dari pin ADC akan dipilih oleh multiplexer untuk diproses oleh ADC. ADC mempunyai rangkaian untuk mengambil sampel dan hold tegangan input ADC sehingga tetap konstan selama proses konversi. Adc mempunyai catu daya yang terpisah yaitu pin AVCC-AGND. Operasi ADC membutuhkan tegangan referensi Vref dan clock fade. ADC mengonversi tegangan input analog menjadi bilangan digital selebar 10-*bit*.

Sinyal input ADC tidak boleh melebihi tegangan referensi. Nilai digital sinyal input ADC untuk resolusi 10-*bit* (1023) adalah:

$$\text{Kode digital} = (\text{Vinput} / \text{Vref}) \times 1023 \qquad (2\text{-}6)$$

Untuk resolusi 8-*bit* (256):

$$\text{Kode digital} = (\text{Vinput} / \text{Vref}) \times 256 \qquad (2\text{-}7)$$

Mode operasi

1. **Mode Konversi Tunggal**

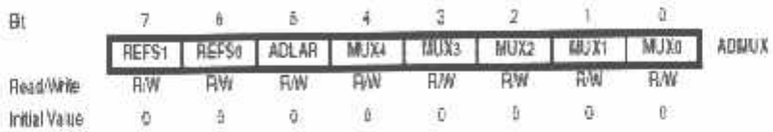
Mode konversi ini dilakukan untuk sekali pembacaan sampel tegangan input. Mode konversi tunggal dipilih dengan meng-*clear bit*-ADFR dalam register ADSCRA.

2. **Mode *Free Running***

Mode konversi ini dilakukan terus menerus sacara kontinyu. Mode free running dipilh dengan men-*set bit*-ADFR dalam register ADCSRA. Dalam mode ini ADC bekerja secara independen dari flag interupsi ADC.

2.2.4.1 Register-register untuk mengakses ADC, antara lain:

➢ **ADMUX** – ADC *Multiplexer Selection Register*



Gambar.2.6. Register ADMUX

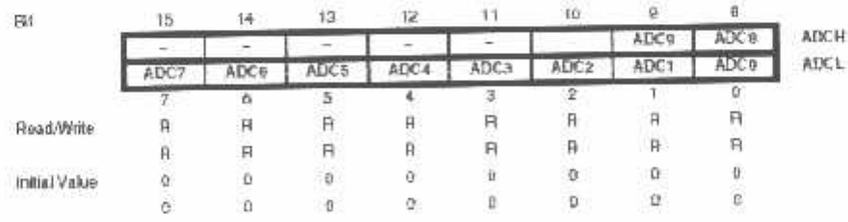
Tabel 2.1. Pemilihan Mode Tegangan Referensi ADC

REFS1	REFS0	Voltage Reference Selection
0	0	AREF, Internal Vref turned off
0	1	AVCC with external capacitor at AREF pin
1	0	Reserved
1	1	Internal 2.56V Voltage Reference with external capacitor at AREF pin

Bit 5 – ADLAR : ADC *Left Adjust Result*

Merupakan bit pemilihan mode data keluaran ADC. Bernilai awal 0 sehingga 2 bit data hasil konversinya berada di register ADCH dan 8 bit sisanya berada di register ADCL, seperti pada gambar 2.21. jika bernilai 1, maka hasilnya seperti gambar 2.7

Bila ADCLAR = 0



Gambar.2.7. Register ADCL, ADCH

Bila ADCLAR = 1

Bit	15	14	13	12	11	10	9	8	
	ADC9	ADC8	ADC7	ADC6	ADC5	ADC4	ADC3	ADC2	ADCH
	ADC1	ADC0	-	-	-	-	-	-	ADCL
	7	6	5	4	3	2	1	0	
Read/Write	R	R	R	R	R	R	R	R	
	R	R	R	R	R	R	R	R	
Initial Value	0	0	0	0	0	0	0	0	
	0	0	0	0	0	0	0	0	

Gambar.2.8. Register ADCL, ADCH

Setelah ADC selesai melakukan konversi register ADCH dan ADCL ini berisi hasil konversi. Bila *channel differensial* dipilih maka hasilnya dalam format *two's complement*. Saat ADCL dibaca, data register tidak akan meng-update data sampai ADCH dibaca. Jika hasilnya dirata kiri (*left adjust*) dan hanya butuh8-bit maka cukuplah dengan membaca ADCH. Jika butuh 10-bit, baca ADCL dahulu kemudian ADCH.

Bit 4...0 MUX[4...0] : Bit pemilih *Analog Channel* dan *Gain*

Merupakan bit pemilih saluran pembacaan ADC. Bernilai awal 00000. Untuk *mode single ended input*, MUX[4...0] bernilai dari 00000-00111.

Tabel 2.2. Tabel Pemilihan Bit Saluran Pembacaan ADC

MUX4..0	Single Ended Input	Pos Differential Input	Neg Differential Input	Gain
00000	ADC0	N/A		
00001	ADC1			
00010	ADC2			
00011	ADC3			
00100	ADC4			
00101	ADC5			
00110	ADC6			
00111	ADC7			
01000	N/A	ADC0	ADC0	10x
01001		ADC1	ADC0	10x
01010		ADC0	ADC0	200x
01011		ADC1	ADC0	200x
01100		ADC2	ADC2	10x
01101		ADC3	ADC2	10x
01110		ADC2	ADC2	200x
01111		ADC3	ADC2	200x
10000		ADC0	ADC1	1x
10001		ADC1	ADC1	1x
10010		ADC2	ADC1	1x
10011		ADC3	ADC1	1x
10100		ADC4	ADC1	1x
10101		ADC5	ADC1	1x
10110		ADC6	ADC1	1x
10111		ADC7	ADC1	1x
11000		ADC0	ADC2	1x
11001		ADC1	ADC2	1x
11010		ADC2	ADC2	1x
11011		ADC3	ADC2	1x
11100		ADC4	ADC2	1x

➢ **ADCSRA** – ADC *Control and Status Register*

Bit	7	6	5	4	3	2	1	0	
	ADEN	ADSC	ADATE	ADIF	ADIE	ADPS2	ADPS1	ADPS0	ADCSRA
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	
Initial Value	0	0	0	0	0	0	0	0	

Gambar.2.9. Register ADCSRA

Bit 7 – ADEN : ADC *Enable*

Merupakan bit pengatur aktivasi ADC. Diisi 1 untukmengaktifkan ADC, diisi 0 untuk mematikan ADC sekaligus memberhentikan konversi yang sedang berlangsung.

Bit 6 – ADSC : ADC *Start Conversion*

Pada mode *single-conversion*, set bit ini untuk memulai tiap konversi. Pada mode *free-running*, set bit ini untuk konversi pertama kalinya. Bit ADSC bila dibaca akan bernilai 1 selama proses konversi, dan bernilai 0 bila konversi selesai. Mengisi bit ini dengan nilai 0 tidak akan mempunyai dampak.

Bit 5 – ADATE : ADC *Auto Trigger Enable*

Bila bit ini diisi 1 maka *auto trigger* ADC akan diaktifkan. ADC akan memulai konversi pada saat tepi positif dari sumber sinyal *trigger* yang dipilih. Sumber sinyal *trigger* ditentukan dengan menseting bit ADTS pada register SFIOR.

Bit 4 – ADIF : ADC *Interrupt Flag*

Bit ini akan bernilai 1 pada saat ADC selesai mengkonversi dan data register telah diupdate. ADC *Conversion Complete Interrupt* akan dijalankan bila bit ADIE dan bit-I pada register SREG diset 1. ADIF akan di-clear secara hardware bila mengerjakan penanganan vektor interrupt yang bersesuaian. Alternatifnya, ADIF dapat di-clear dengan menuliskan 1. Hati-hati bila bekerja dengan *Read-Modify-Write* pada ADCSRA, interrupt yang tertunda dapat dinonaktifkan atau batal.

Bit 3 – ADIE : ADC *Interrupt Enable*

Mengisi bit ini dan bit-I pada register SREG menjadi 1 akan mengaktifkan ADC *Conversion Complete Interrupt*.

Bit 2...0 – ADPS[2...0] – Bit pemilih ADC *Prescaler*

Merupakan bit pengatur clock ADC. Bernilai awal 000. Lebih detail nilai bitnya dapat dilihat pada tabel 2.3

Tabel 2.3. Tabel Penentu Bilangan Pembagi Antara Sumber Clock XTAL ke Clock ADC

ADPS2	ADPS1	ADPS0	Division Factor
0	0	0	2
0	0	1	2
0	1	0	4
0	1	1	8
1	0	0	16
1	0	1	32
1	1	0	64
1	1	1	128

➢ **SFIOR** – *Special Function* I/O Register untuk sumber *auto trigger Bit*

Bit	7	6	5	4	3	2	1	0	
	ADTS2	ADTS1	ADTS0	–	ACME	PUD	PSR2	PSR10	SFIOR
Read/Write	R/W	R/W	R/W	R	R/W	R/W	R/W	R/W	
Initial Value	0	0	0	0	0	0	0	0	

Gambar.2.10. Register SFIOR

Bit 7:5 – ADTS2:0 : ADC *Auto Trigger Source*

Bila ADATE dalam register ADCSRA diset 1, maka nilai dalam bit-bit ini akan menentukan sumber mana yang akan mentrigger konversi ADC. Bila bit ADATE bernilai 0, maka bit-bit ini tidak akan mempunyai efek. Sebuah konversi ditrigger oleh sinyal *rising-edge* dari *interrupt flag* yang dipiih. Perlu diingat bahwa memindah sumber trigger yang di-clear ke sumber trigger lain yang diset akan menyebabkan *positive-edge* pada sinyal trigger. Bila ADEN dalam register ADCSRA diset, juga akan memulai konversi. Memindah mode *free running* tidak akan menyebabkan pulsa *trigger*, meskipun bila *flag interrupt* ADC diset.

2.3.5 EEPROM (*Electrically Erasable Programmable Read Only*)

EEPROM (*Electrically Erasable Programmable Read Only Memory*) adalah salah satu dari tiga tipe memori pada AVR. EEPROM tetap dapat menyimpan data saat tidak dicatu daya dan juga dapat diubah saat program berjalan. Kapasitas EEPROM pada ATMega16 sebesar 512 byte. Berbentuk suatu pemisahan data, di mana tiap byte dapat dibaca dan ditulis. EEPROM mempunyai kapasitas sedikitnya 100.000 siklus tulis atau penghapusan.

Untuk menulis dalam EEPROM, sebelumnya perlu ditentukan terlebih dahulu data apa yang akan ditulis serta alamat untuk menulis data tersebut. Untuk mencegah ketidaksengajaan menulis di dalam EEPROM, diperlukan prosedur untuk menulis dalam EEPROM. Proses penulisan EEPROM tidak berlangsung waktu itu juga, tetapi membutuhkan waktu sekitar 2,5 sampai 4 ms. Oleh karena alasan tersebut, program yang dibuat harus dicek terlebih dahulu apakah EEPROM telah siap untuk ditulis dengan byte data baru.

Alamat untuk byte yang akan ditulis dimasukkan ke dalam EEPROM Address Register (EEAR). Data akan diletakkan dalam EEPROM Data Register (EEDR). EECR (EEPROM *Control Register*) digunakan untuk mengontrol operasi dari EEPROM. EECR memiliki empat bit, yaitu EEMWE, EEWE, EERIE, dan EERE. Berikut penjelasan register-register pada EEPROM :

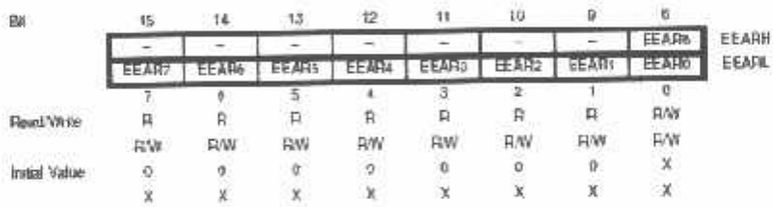
a. EEPROM *Address Register* – EEARH dan EEARL

- **Bits 15..9 – Res: *Reserved Bits***

Bit ini merupakan bit cadangan pada ATMega16 dan selalu dibaca nol.

- **Bit 8..0- EEAR8..0: EEPROM *Address***

EEPROM address register-EEARH dan EEARL menetapkan alamat EEPROM pada 512 bytes diruang EEPROM. EEPROM data byte ditujukan secara linier antara 0 dan 511. Nilai awal dari EEAR ini tak tergambarkan. Suatu nilai yang sesuai harus ditulis sebelum mengakses EEPROM.

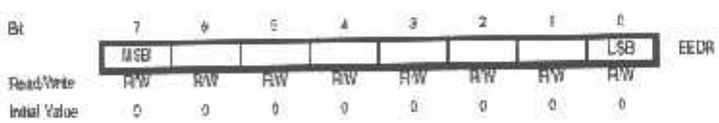


Gambar.2.11. EEPROM address register – EEARH dan EEARL

b. EEPROM *Data Register* – EEDR

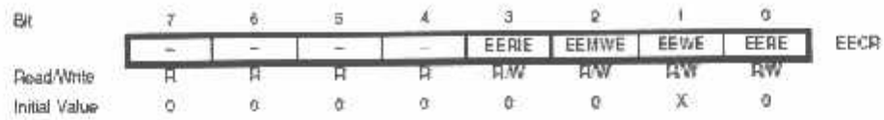
- **Bits 7..0 – EEDR7..0: EEPROM Data**

Dari operasi penulisan EEPROM, Register EEDR berisi data yang akan dituliskan di EEPROM pada alamat yang diberikan oleh register EEAR. Untuk operasi baca pada EEPROM, EEDR berisi data yang terbaca dari EEPROM pada alamat yang diberikan oleh EEAR.



Gambar.2.12. EEPROM data register – EEDR

c. **EEPROM *Control Register* – EECR**



Gambar.2.13. EEPROM Control register _ EECR

- **Bit 7..4 – Res : *Reserved Bits***

Bit ini merupakan bit cadangan pada ATMega16 dan selalu dibaca nol.

- **Bit 3 – EERIE : EEPROM *Ready Interrupt Enable***

Penulisan EERIE memungkinkan EEPROM ready interrupt jika I-Bit di dalam SREG di-set. Penulisan EERIE menjadi nol akan melumpuhkan interrupt. EEPROM ready interrupt menghasilkan suatu interrupt yang tetap ketika EEWE diclear.

- **Bit 2 – EEMWE : EEPROM *Master Write Enable***

Bit EEMWE menentukan apakah pengaturan EEWE juga digunakan apabila EEPROM siap digunakan untuk ditulisi byte. Ketika EEMWE di-set, pengaturan EEWE dengan empat siklus waktu dalam menulis data ke EEPROM pada alamat yang terpilih adalah jika EEMWE bernilai nol, pengaturan EEWE tidak akan mempunyai efek.

- **Bit 1 – EEWE : EEPROM *Write Enable***

EEPROM *Write Enable Signal* EEWE adalah penulisan *strobe* pada EEPROM. Ketika alamat dan data yang tepat telah di-set, bit EEWE harus ditulis dengan suatu nilai tertentu pada EEPROM. Bit EEMWE harus ditulis pada register data sebelum data yang sebenarnya ditulis ke EEWE, jika tidak tulisan pada EEPROM terhapus.

- **Bit 0 – EERE : EEPROM *Read Enable***

EEPROM *Read Enable Signal* EERE adalah strobe yang dibaca pada EEPROM. Ketika alamat yang benar sudah diatur di register EEAR, bit EERE harus dituliskan suatu logika untuk memicu pembacaan pada EEPROM. Akses baca EEPROM mengambil satu instruksi, dan data yang diminta akan tersedia seketika. Pemakai perlu memeriksa EEWE bit sebelum operasi baca dimulai. Jika suatu operasi penulisan sedang dalam proses, tidak menutup kemungkinan untuk membaca EEPROM, maupun untuk berubah daftar EEAR.

2.4. IC ISD 2590

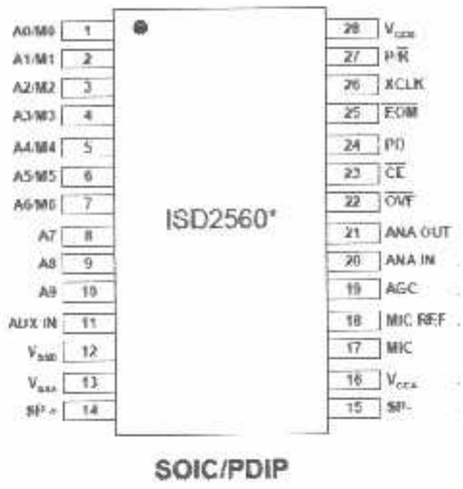
Berfungsi untuk melakukan proses perekaman suara dan proses pemutar ulangan hasil rekaman. Piranti ini hanya membutuhkan beberapa komponen pasif agar dapat melakukan kerjanya sebagai piranti dasar pengolahan suara. Dalam hal perancangan fungsi perekaman dan pemutaran hasil rekaman Model untuk menjalankan fungsi ISD2590 dipilih pada mode *push button*,yaitu pengoperasian yang didasari pada penggunaan tombol – tombol *push on* untuk menjalankan baik proses perekaman maupun pemutaran ulang. Mode ini bisa disesuaikan dengan penggunaan IC mikrokontroller sebagai pengganti saklar *push on* untuk melakukan intruksi kerja. Adapun urutan kerja pada proses *record* dan proses putar ulang, yaitu :

Proses *Record*.

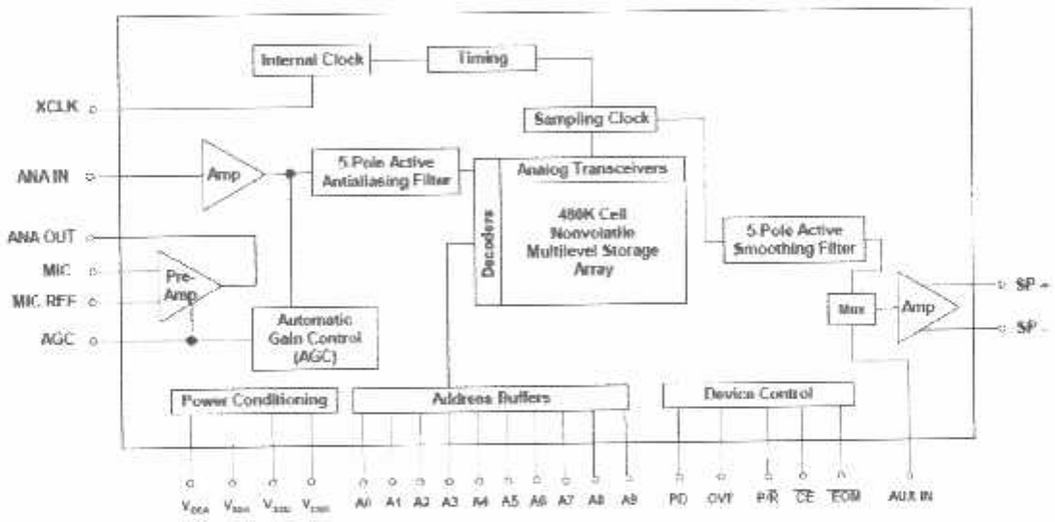
a) Pin PD (*Power Down*) diberikan kodisi*LOW*.
b) Pin P / ~ R (*Playback/Record*) diberikan kondisi *LOW*.
c) Pin CE (*Chip Enabled*) diberikan pulsa *low* (H _ L _ H) seasaat setelahpemberian pulsa, pada pin ~OEM akan bernilai *HIGH* yang menandakan proses record sedang berlangsung.
d) Untuk mengakhiri proses rekam dengan memberikan kembali pulsa *LOW* pada pin CE atau menunggu hingga durasi perekaman sesuai dengan tipe IC yang dipakai pada pin ~EOM bernilai *LOW* kembali yang menandakan proses rekam telah usai.

Proses Putar Ulang

a) Pin PD (*Power Down*) diberikan kondisi *LOW*.
b) Pin P / ~R (*playback/record*) diberikan kondisi *HIGH*.
c) Pin CE (*Chip Enabled*) diberikan pulsa *LOW* (H – L – H), sesaat setelah pemberian pulsa, pada pin ~OEM akan bernilai *HIGH* yang menandakan proses *playback* sedang berlangsung.
d) Setelah *playback* telah usai, pin ~OEMakan bernilai *LOW* kembali yang menandakan proses *playback* telah selesai.



Gambar.2.14. Pin Konfigurasi IC ISD2590



Gambar.2.15. Blok Diagram IC ISD2590

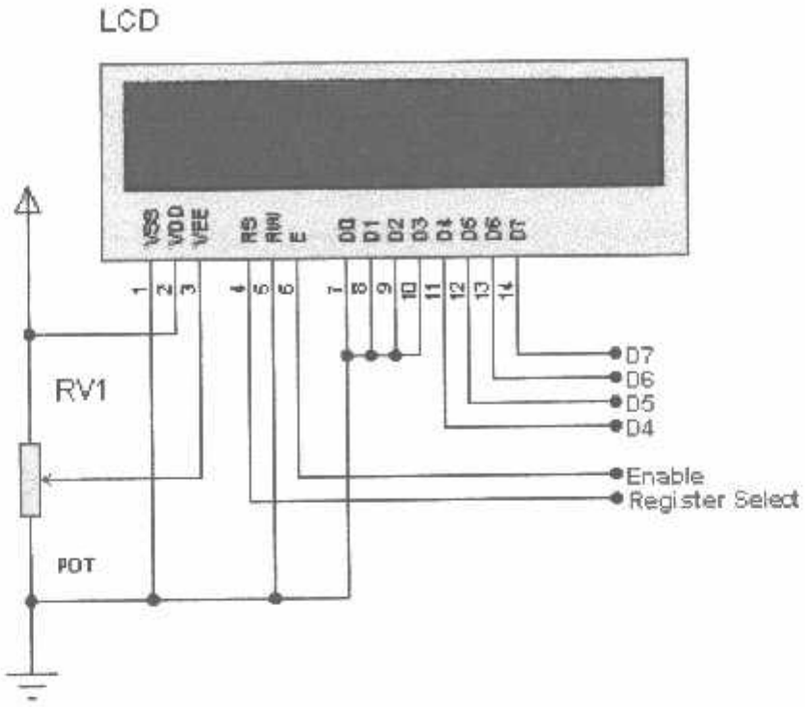
Rangkaian ini merupakan suatu rangkaian yang terdiri atas beberapa bagian yang masing-masing bagian mempunyai fungsi sendiri-sendiri akan tetapi tetap merupakan bagian yang kompleks dan saling bekerja sama. Bagian-bagian alat ini terdiri atas bagian pengindera sebagai pengaktif *relay* untuk saklar perekam suara dan lampu penerangan, dan bagian perekam suara sebagai perekam suara yang akan disimpan.

Prinsip utama dari rangkaian Aplikasi IC ISD 2590 Sebagai Pesan Pada Saklar Otomatis Lampu Penerangan bekerja atas dasar pengolahan getaran bunyi menjadi isyarat listrik. bentuk gelombang yang diciptakan. Mic kemudian mengirimkan sinyal ke VR yang akan mengatur berapa besarnya masukan yang diinginkan ke C1 yang

berfungsi sebagai kopling untuk melewatkan sinyal dan dikuatkan oleh transistor. Arus yang keluar dari C1 di groundkan tetapi sinyal tetap dipertahankan untuk melewati transistor. Keluaran dari transistor sinyal yang terbawa tegangan akan dirubah menjadi tegangan oleh dioda dan disulut ke IC 7473 yang berfungsi sebagai flip-flop. Dari IC 7473 keluaran akan berlogika 1 (high) atau 0 (low). Jika pada kondisi 1 (high) akan menyulut transistor yang akan memberi tegangan pada relay sehingga relai akan bekerja kemudian akan menghubungkan kaki pin CE pada IC ISD 2590 ke kondisi low tetapi pada pin P/A dalam kondisi 1 (high), sehingga akan memutar pesan yang telah direkam sebelumnya. Suara yang keluar merupakan hasil dari pada 1 kali proses perekaman pesan yang telah dilakukan Jika memori IC ISD yang digunakan telah penuh, telah digunakan untuk perekaman suara selama 90 detik, maka perlu di *reset* agar dapat merekam pesan saura kembali. Untuk melakukan pe-resetan, pin PD pada IC ISD diberi kondisi '1' (*high*) sesaat (*low-high-low*).

2.5. LCD(Liquid Crystal Display)

LCD (Liquid Crystal Display) atau dapat di bahasa Indonesia-kan sebagai tampilan Kristal Cair adalah suatu jenis media tampilan yang menggunakan kristal cair sebagai penampil utama. LCD bisa memunculkan gambar atau tulisan (berwarna juga bisa dong) dikarenakan terdapat banyak sekali titik cahaya (piksel) yang terdiri dari satu buah kristal cair sebagai sebuah titik cahaya. Walau disebut sebagai titik cahaya, namun kristal cair ini tidak memancarkan cahaya sendiri. Sumber cahaya di dalam sebuah perangkat LCD adalah lampu neon berwarna putih di bagian belakang susunan kristal cair tadi. Bus data LCD dihubungkan dengan Bus data *mikrokontroler*. Karena LCD dioperasikan hanya menerima data. Maka Pin R/W dihubungkan dengan *ground*. RS dihubungkan dengan pin A0 dari bus alamat *mikrokontroler*. Untuk mengatur kecerahan LCD digunakan resistor variable 10kΩ.



Gambar.2.16. Penampilan LCD dan Konfigurasi Pinnya

Masukan yang diperlukan untuk mengendalikan modul ini berupa bus data yang masih termutiplek dengan bus alamat serta 3 bit sinyal control. Pengendalian dot matrik LCD dilakukan secara internal oleh kontroler yang sudah terpasang pada modul LCD. Fungsi-fungsi pin LCD ditunjukkan dalam tabel 2.4:

Tabel.2.4. Fungsi Pin LCD

penyemat	Fungsi
DB_0-DB_7	Merupakan saluran data berisi perintah dan data yang akan dihasilkan di LCD
Enable	Sinyal operasi awal, sinyal ini mengaktifkan data tulis atau baca
R/W	Sinyal seleksi tulis atau baca 0 : tulis 1 : baca
RS	Sinyal pemilih register 0 : instruksi register (tulis) 1 : data register (baca dan tulis)
V_{EE}	Untuk mengendalikankecerahan LCD dengan mengubah-ubah nilai resistor variable yang dipasang
V_{dd}	Tegangan sumber +5V
V_{SS}	Terminal *ground*

2.6. Speaker

Speaker merupakan suatu komponen yang dapat menghasilkan suara yang mana apabila diberi tegangan pada input komponen, maka akan bekerja sesuai dengan karakteristik dari alarm yang digunakan. Dalam pembuatan proyek tugas akhir ini, penulis menggunakan "Speaker" sebagai informasi suara. Hal ini dikarenakan karakteristik dari komponen yang mudah untuk diaplikasikan dan suara yang dihasilkan relatif kuat.

Speaker merupakan sebuah komponen elektronik yang dapat mengkonversikan energi listrik menjadi suara yang di dalamnya terkandung sebuah osilator internal untuk menghasilkan suara dan pada speaker osilator yang digunakan biasanya diset pada frekuensi kerja sebesar 400 Hz.

Dalam penggunaannya dalam rangkaian, speaker dapat digunakan pada tegangan sebesar antara 6V sampai 12V dan dengan tipical arus sebesar 25 mA. Pada gambar berikut dapat dilihat simbol dari komponen speaker.

Gambar.2.17. Simbol Speaker

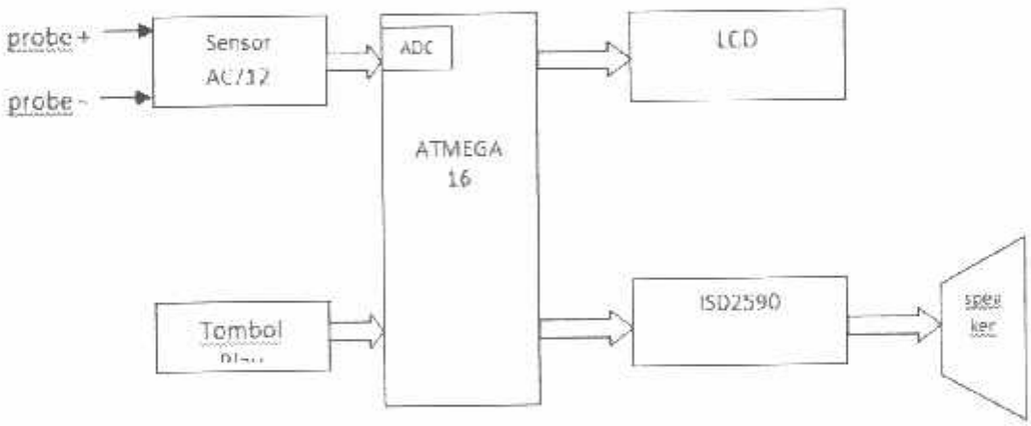
BAB III
PERANCANGAN DAN PEMBUATAN ALAT

3.1 Pendahuluan

Penyusunan skripsi ini didasarkan pada masalah yang bersifat aplikatif, yaitu perancangan dan perealisasia alat agar menghasilkan kinerja yang sesuai dengan perencanaan dan mengacu pada rumusan masalah. Data dan spesifikasi komponen yang digunakan dalam perencanaan merupakan daa sekunder yang diambil dari buku data komponen elektronika. Pemilihan komponen berdasarkan perencanaan dan disesuaikan dengan komponen yang ada di pasaran.

3.2 Perancangan dan Perealisasian Alat

Agar perancangan dan perealisasian alat berjalan secara sistematis maka perlu dirancang *blok diagram* yang menjelaskan sistem yang dirancang dibuat secara garis besar. Gambar 3.1 menunjukkan *blok diagram* sistem.



Gambar 3.1 Blok Diagram Sistem Perancangan Alat

Fungsi dari tiap tiap blok diagram dijelaskan sebagai berikut:

1. Sensor ACS712

   Sensor ACS712 merupakan sensor yang presisi sebagai sensor medan magnet pada suatu arus AC atau DC.

2. Mikrokontroller

   Mikrokontroler berfungsi sebagai pengendali serta pemroses utama dari data yang dihasilkan dan yang masuk pada pin – pin input.

3. LCD (Licuid Cyrstal Display)

   LCD berfungsi untuk menampilkan karakter hasil pemrosesan dari mikrokontroler.

4. ISD (Information Store Device) 2590

   ISD merupakan komponen berbentuk IC yang dapat menyimpan informasi dalam bentuk suara dalam jangka waktu tertentu.

5. Speaker

   Speaker merupakan sebuah komponen elektronik yang dapat mengkonversikan energi listrik menjadi suara.

Cara kerja sistem

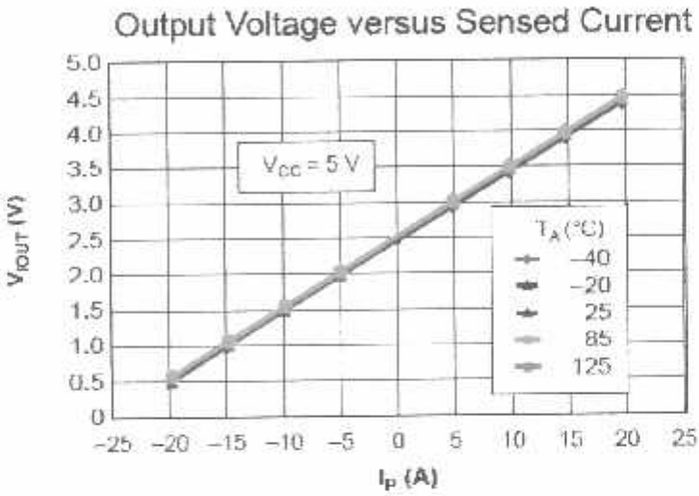
Dalam perancangan alat ini menggunakan sensor *Hall Effect* yaitu sensor yang digunakan untuk mendeteksi medan magnet. *Hall Effect* sensor akan menghasilkan sebuah tegangan yang proporsional dengan kekuatan medan magnet yang diterima oleh sensor tersebut. Arus listik tersebut akan di alirkan melalui sebuah kumparan untuk memperoleh medan magnet yang cukup. Medan magnet pada inti kumparan diterima oleh sensor,sensor akan memberikan respon keluaran berupa perubahan tegangan akibat pengaruh medan magnet.

Tegangan keluaran sensor dikuatkan pada blok pengkondisi sinyal untuk menyesuaikan dengan tegangan yang diperlukan oleh ADC system mikrokontroler. Sistem mikrokontroler mengolah data yang diterima dari pengkondisi sinyal yang berupa tegangan dengan ADC internal, mengolah dan memberikan keluaran yang ditampilkan oleh penampilan LCD, kemudian dilanjutkan lagi dengan pengolahan data yang ditampilkan oleh ISD2590 berupa suara.

3.3 Perancangan Perangkat Keras

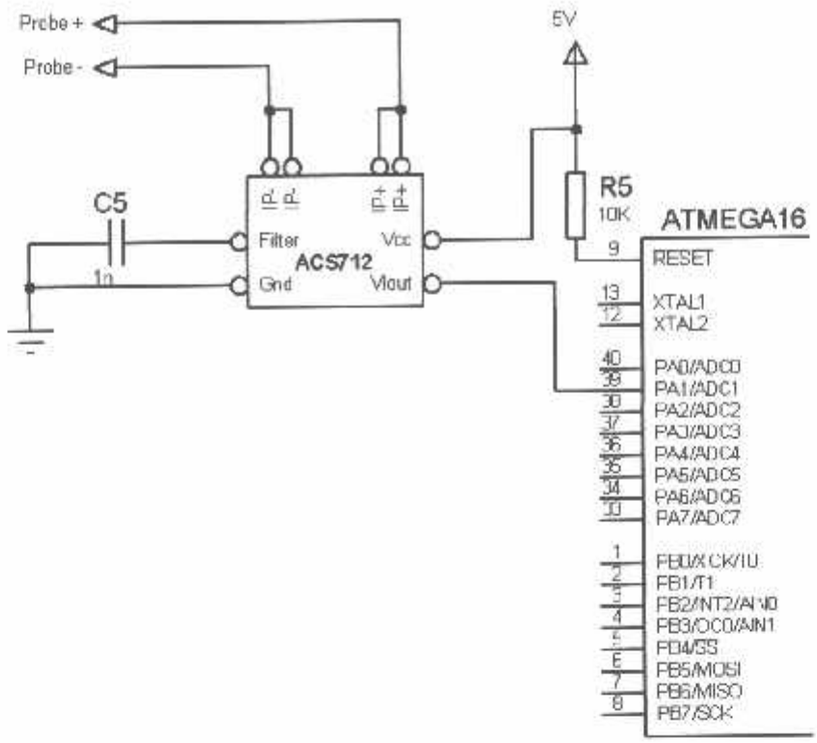
3.3.1 Perencangan Sensor ACS712

Untuk dapat membaca arus pada pengukuran arus AC dan DC sebagaimana perancangan, maka digunakan sensor arus *Hall Effect* ACS712. Sensor ACS712 berdasarkan datasheet mempunyai keluaran tegangan sebagai perwakilan arus yang terukur sensor dan mempunyai resolusi keluaran 100mV/Ampere. Grafik keluaran sensor *hall effect* terhadap perubahan besar arus (Data Sheet) ditunjukkan dalam gambar 3.1.



Grafik 3.1 Grafik Arus ACS712

Garis lurus pada grafik merupakan regresi linear yang dapat dari Data Sheet ACS712, keluaran arus pada titik 0 adalah tegangan sensor dalam kondisi tanpa beban dan menghasilkan arus 2,5A. Untuk dapat mengukur keluaran tegangan sensor ACS712, maka diperlukan ADC, dimana pada perancangan ini ADC yang digunakan adalah ADC internal dari ATMEGA16 sehingga keluaran tegangan dari sensor arus dapat diolah oleh mikrokontroller untuk kalkulasi lebih lanjut. Adapun perancangan rangkaian dan hubungan sensor terhadap ADC internal ATMEGA16 ditunjukkan sebagaimana gambar 3.2:

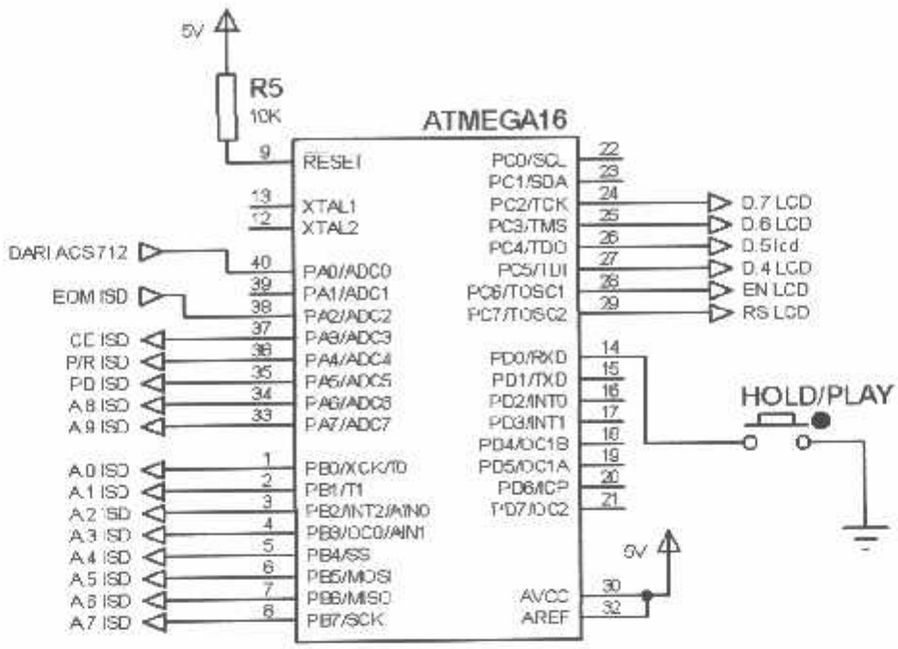


Gambar 3.2 Skematik ACS712

Nilai filter (C5) dipilih pada nilai antara 1nF hingga 10nF (berdasarkan datasheet). Filter ini digunakan untuk mereduksi riplle (noise) dari pengukuran arus.

3.3.2 Perencanaan Mikrokontroller

Konfigurasi mikrokontroller ATMEGA16 digolongkan menjadi pin sumber tegangan, pin osilator, pin control, pin I/0 dan pin untuk proses interupsi luar. Gambar 3.3 berikut merupakan konfigurasi pin ATMEGA16:



Gambar 3.3 Susunan Pin dari ATMEGA16

Fungsi dari pin-pin ATMEGA16:

a. Vcc = pin positif sumber tegangan 5V

b. Gnd = pin ground sumber tegangan

c. AREF = Analog Reference, digunakan sebagai masukan referensi input ADC internal.

d. AVCC = Analog VCC, sumber tegangan ADC internal.

c. Reset = pin masukan Reset AVR

f. Port D = pin-pin pada port D ini mempunyai 5 inputan antara lain :

- PD.0 (RXD) : Masukan penerima data serial.
- PD.1 (TXD) : Keluaran pengirim data serial
- PD.2 (INT0) : Interupsi 0 eksternal
- PD.3 (INT 1) : Interupsi 1 eksternal
- PD.4 (T0) : Masukan eksternal waktu / pencacah 0
- PD.5 (T1) : Masukan eksternal waktu / pencacah 1
- PD.6 (ICP) : Internal Comparator

g. Port B = Port B ini digunakan sebagai port input - output data dan port untuk pengisian software menggunakan ISP.

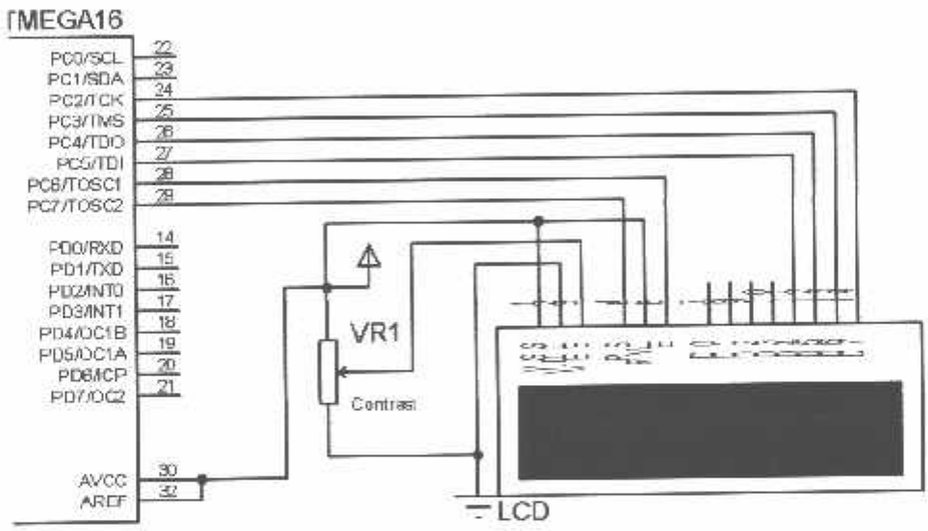
3.3.2.1 Pin-pin yang digunakan pada sistem

Pada perancangan alat ini pin pin ATMEGA16 yang digunakan adalah :

- Port A.0 – digunakan sebagai input ADC untuk pengkondisi sinyal.
- Port B.0 B.5= digunakan untuk Port LCD
- Port B.7 = digunakan LED Indikator.
- Port C.0 = digunakan sebagai output PWM atau driver TRIAC SSR.

3.3.3 Perencanaan Rangkaian LCD

Sebagai penampil informasi pengaturan seting Daya, Monitor Daya, KWH, Menu Keypad, dan lainnya pada perancangan alat ini, maka digunakan LCD sebagai penampil informasi. LCD yang digunakan adalah LCD M1632 atau 16X2 Karakter. Adapun hubungan rangkaian LCD terhadap Controller (MCU) ditunjukkan pada gambar 3.4:



Gambar 3.4 Rangkaian LCD

Potensio 10K pada rangakain LCD diatas merupakan pembagi tegangan yang dihubungkan ke pin VEE LCD. Pin ini berfungsi untuk mengatur kontras LCD sesuai keinginan. Untuk pin WR diground-kan karena sifatnya hanya menulis dari MCU ke LCD, sementara pin 15 dan 16 adalah input tegangan LED Backlight LCD, sehingga LCD dapat kelihatan terang meskipun malam hari.

3.3.4 Perencanaan Rangkaian ISD 2590

Rangkaian ini digunakan untuk menghasilkan suara yang diperlukan system agar lebih interaktif. Rangkaian ini mempergunakan komponen utama yaitu IC ISD 2590. untuk dapat memfungsikan IC ini maka diperlukan komponen tambahan .

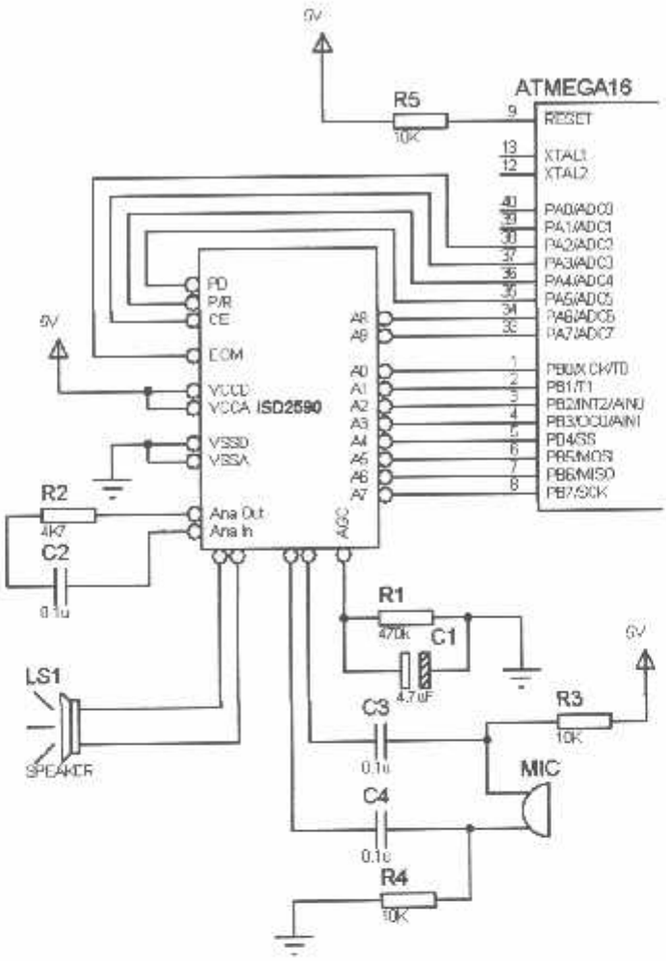
IC ISD 2590 ini memiliki kemampuan menyimpan suara selama 90 detik. Komponen ini menggunakan teknologi CMOS EEPROM ,sehingga suara yang dimasukkan dapat diubah –ubah dengan cepat .

IC ISD 2590 memiliki 200 *segment address*, sehingga resolusinya adalah 100ms . keseluruhan alamat di akses dengan 8 pin alamat A0 – A7 dengan resolusi adalah 100 ms,maka range alamat adalah 00H – A0H.

Untuk merekam pesan mulai alamat tertentu, pertama–tama pin alamat A0 – A7 diberi logika alamat yang diinginkan .Setelah itu pin REC (pin nomor 27) diberi logika alamat yang diinginkan . Saat pin REC kembali dari logika rendah ke tinggi, secara otomatis IC ISD ini akan menyisipkan tanda *end – of – message* (menandakan akhir sebuah pesan).

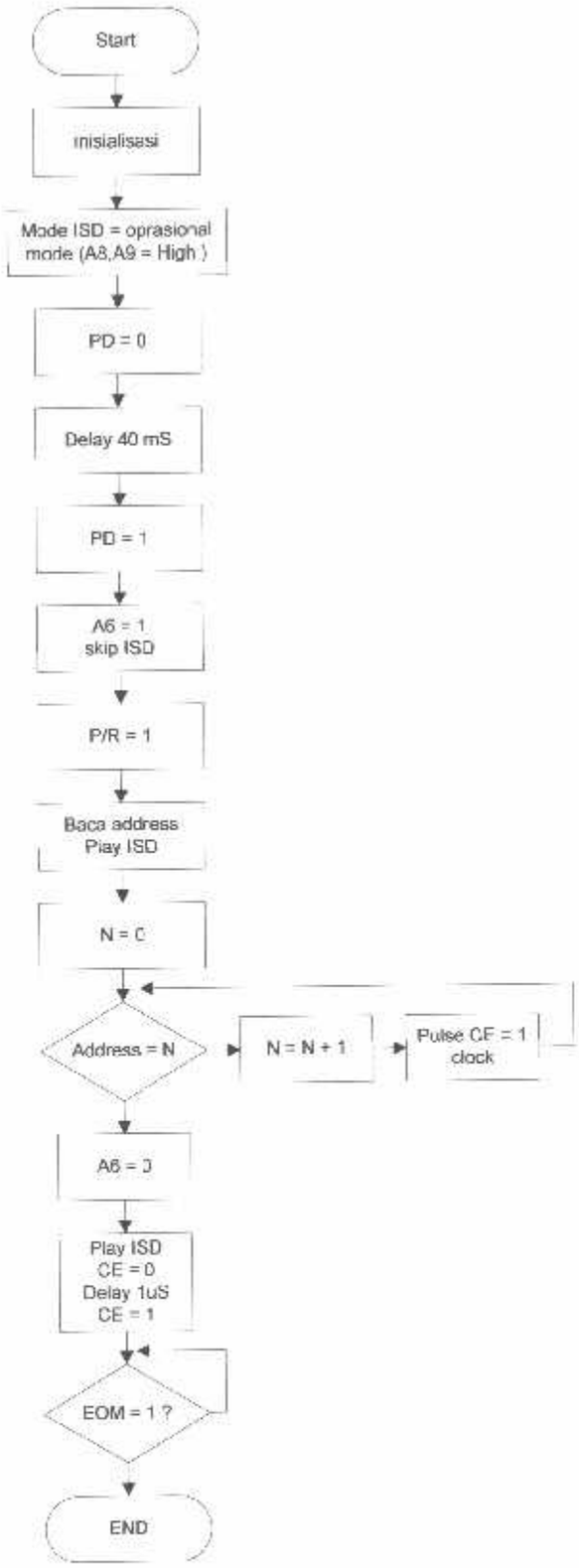
Pemutaran pesan dapat dilakukan melalui pin PLAYE dan PLAYL Pemutaran pesan aktif saat terjadi transisi ddari logika tinggi ke rendah Pada pin PLAYE dan pesan terus berputar hingga menjumpai tanda *end – of – message* . Sedangkan bila pengaktifan dilakukan melalui pin PLAYL maka pesan akan diputar selama pin ini berlogika rendah . Alamat pesan yang diputar tergantung pada pin A0 –A7.

Agar menghemat pin , pin alamat A0 – A5 IC ISD dihubunkan ke *ground* sehingga berlogika 0. Pin A6 dan A7 dihubungkan ke *port* B bit 0 dan 1. Sedangkan pengaktifan pemutaran pesan menggunakan pin PLAYE yang dihububgkan ke *port* B bit ke 2. Rangkaian unit suara (ISD) terlihat dalam gambar 3.5 :



Gambar.3.5 Skematik ISD 2590

Flowchart sistem ISD dapat dilihat pada gambar 3.6:

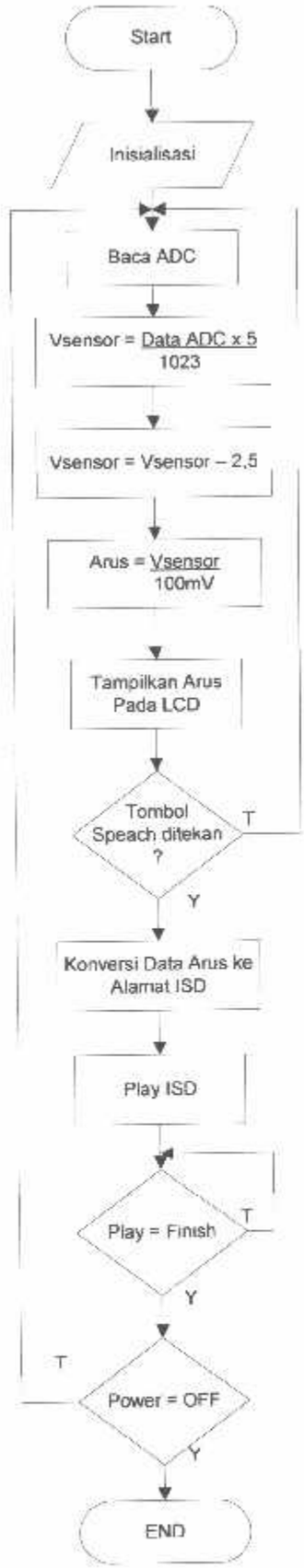


Gambar 3.6 Flowchart Sistem ISD 2590

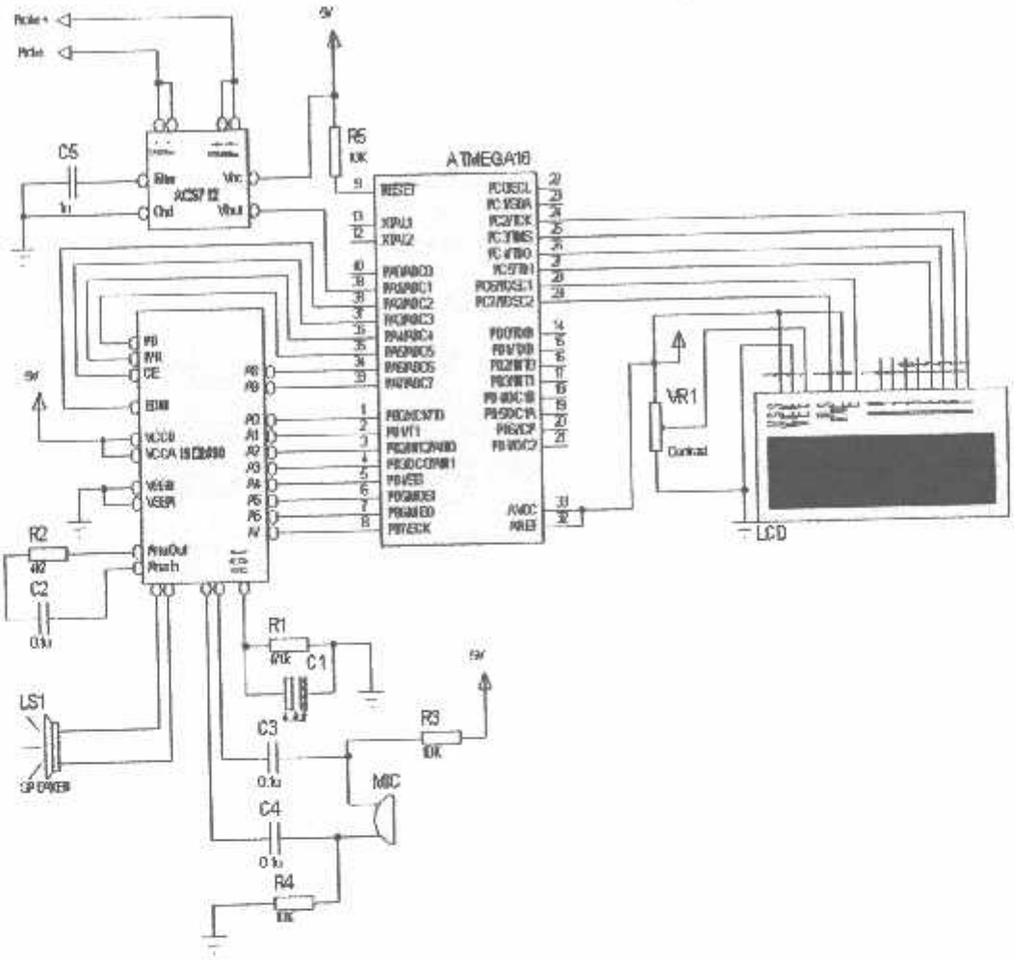
3.4 Perancangan Perangkat Lunak

Perangkat luak dirancang untuk mengatur kerja sistem mikrokontroller, Perangkat lunak adalah susunan perintah-perintah (progam) di dalam memori yang harus dilaksanakan mikrokontroller.

Progam amperemeter dengan *Hall Effect* merupakan progam yang dirancang bekerja untuk membaca data masukan ADC internal mikrokontroller, mengkonversi menjadi data digital, kemudian melakukan pengolahan data tersebut dan menampilkan dalam penampil LCD. Adapun pengolahan data yang lain yaitu dengan cara menampilkan dalam bentuk suara yang tersimpan dalam ISD, kemudian data yang ada pada ISD akan di tampilkan melalui Speaker. Berikut ini adalah diagram alir (flowchart) dari software yang dirancang.



Gambar 3.7 Flowchart Perangkat Lunak



Gambar 3.8 Gambar Rangkaian Keseluruhan Sistem

BAB IV
PENGUJIAN

4.1 Umum

Bab ini membahas pengujian dan analisis alat yang telah dirancang dari sistem yang telah dibuat. Pengujian dilakukan dengan pengukuran tiap-tiap blok dengan tujuan mengamati apakah blok-blok tersebut bekerja sesuai dengan yang direncanakan.

Pengujian dilakukan berdasarkan pada masing-masing komponen pendukung dari alat serta secara keseluruhan. Pengujian yang dilakukan adalah :

4.2 Pengujian Sensor *Hall Effect*

- **Tujuan :**

  Tujuan pengujian sensor adalah untuk mengetahui respon sensor terhadap perubahan arus yang diberikan.

- **Peralatan :**

  Peralatan yang diperlukan untuk melakukan pengujian terhadap sensor *hall effect* adalah sebagai berikut :

  - ✓ Power *supply*
  - ✓ Sensor *Hall Effect* ACS712
  - ✓ Multimeter digital

  Blok diagram pengujian sensor *Hall Effect* ditunjukkan dalam gambar 4.1.

Gambar 4.1 Blok Diagram Pengujian Sensor *Hall Effect*

- **Prosedur pengujian :**

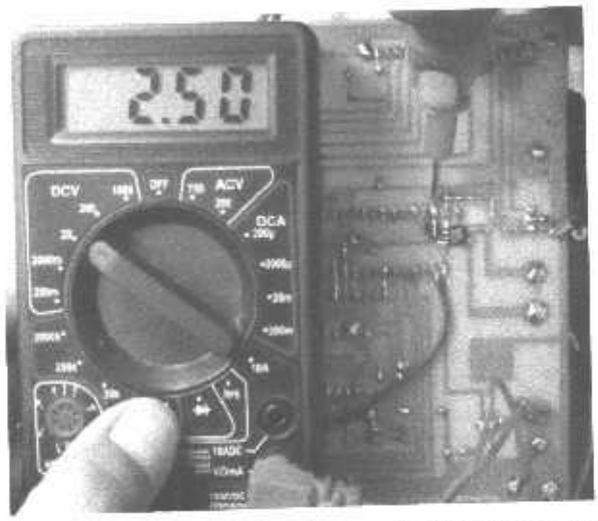
  Pengujian sensor *Hall Effect* dilakukan dengan melakukan urutan prosedur sebagai berikut :

  - ✓ Merangkai modul rangkaian seperti pada blok diagram.
  - ✓ Memberikan catu daya 5V pada rangkaian sensor.

✓ Merubah nilai arus yang dialirkan pada beban bervariasi mulai 0 sampai 1 ampere yang diakibatkan oleh perubahan arus.

- **Hasil Pengujian dan Analisa :**

Dari grafik 3.1 pada bab III kita bisa berpedoman dalam pengujian sensor *hall effect* yang akan kita buat. Keluaran sensor tanpa beban dapat dilihat pada gambar 4.2:



Gambar 4.2 Keluaran Arus Pada Sensor ACS712 tanpa beban (0A)

Adapun keluaran sensor setelah diberi beban berupa lampu sebesar 0,6 mA, sehingga dapat kita lihat perubahan arus pada gambar 4.3 dan gambar 4.4 sebagai berikut:

Gambar 4.3 Lampu 12V/0,6mA Sebagai Beban

Gambar 4.4 Keluaran Arus Pada Sensor ACS712 Setelah diberi beban (0,6mA)

Dari hasil pengujian, didapatkan keluaran sensor *hall effect* akibat perubahan arus, data hasil pengujian ditunjukkan dalam Tabel 4.1:

Tabel 4.1. Keluaran Sensor *Hall Effect* Akibat Perubahan Arus

No	Arus Beban (A)	Keluaran Sensor Hall Effect (V)	Hasil Dari Data Sheet (V)	(%) Error
1	0,00 (tanpa beban)	2,500	2,500	0
2	0,20	2,521	2,520	0,04
3	0,40	2,540	2,540	0
4	0,60	2,562	2,560	0,08
5	0,80	2,581	2,580	0,04
6	1,00	2,603	2,600	0,11

Dari hasil pengukuran didapat hasil analisa error rata-rata pada sensor arus, yaitu :

$$\text{Error Rata-rata} = \frac{\sum Error}{\sum Percobaan}$$

$$= \frac{0,27}{6}$$

$$= 0,045\ \%$$

4.3 Pengujian ADC dan Penampil LCD

- **Tujuan :**

Tujuan dari pengujian ADC dan penampil LCD adalah :

✓ Mengetahui perubahan keluaran ADC saat tegangan masukan berubah

✓ Membaca keluaran ADC pada penampil LCD

- **Peralatan :**

Peralatan yang diperlukan untuk melakukan pengujian terhadap ADC dan penampil LCD adalah sebagai berikut :

✓ Catu daya 5V

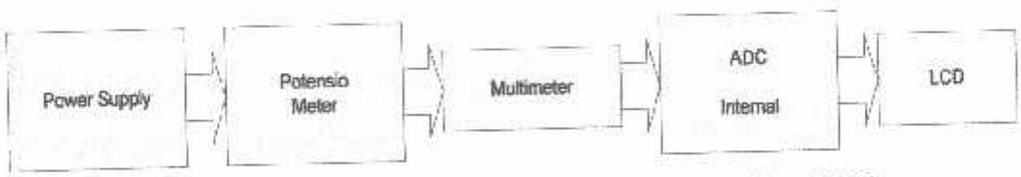
✓ Resistor variabel 1kΩ

✓ Sistem Mikrokontroller ATMega 16

✓ Penampil LCD

✓ Multimeter digital

Blok diagram pengujian ADC ditunjukkan dalam gambar 4.5:



Gambar 4.5 Blok Diagram Pengujian ADC

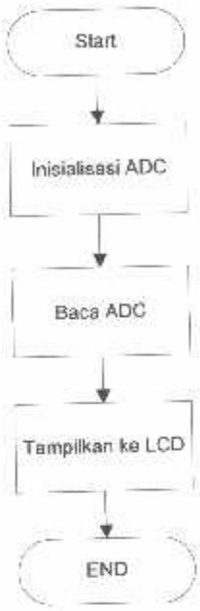
- **Prosedur :**

Pengujian ADC dan penampil LCD dilakukan dengan melakukan urutan prosedur sebagai berikut :

✓ Merangkai modul rangkaian seperti pada blok diagram.

✓ Memberikan catu daya 5V pada rangkaian.

✓ Masukkan progam baca ADC ke sistem mikrokontroller. Adapun flowchart progam adalah sebagai berikut :



Gambar 4.6 Flowchart Baca ADC

- ✓ Merubah resistor variabel untuk variasi tegangan 0 hingga 5V
- ✓ Mengamati perubahan data ADC pada penampil LCD

- **Hasil Pengujian dan Analisa :**

Dari hasil pengujian ADC sebagimana prosedur pengujian diatas, tegangan referensi menggunakan referensi sebesar 5V dengan resolusi ADC yang digunakan 10 Bit. Dengan demikian didapat data hasil pengujian sebagaimana ditunjukkan dalam Tabel 4.2:

Tabel 4.2.Pengujian ADC Dengan Perhitungan Terhadap Masukan Yang Diberikan

no	Tegangan Masukan (mV)	Data ADC
1	0	0
2	250	51,2
3	500	102,3
4	750	153,5
5	1000	204,6
6	1250	255,8
7	1500	306,9
8	1750	358,1
9	2000	409,2
10	2250	460,4

Adapun analisa hasil dari Vinput ADC 250mV pada hasil pengujian tabel4.2 dapat dihitung sebagaimana berikut:

Perhitungan ADC data ke- 5 dengan V_{in} = 1000 mV

Data ADC $= \frac{V_{in}}{V_{ref}} \times 1023$

$= \frac{1}{5} \times 1023$

$= 204.6$

Gambar 4.7 Pengujian ADC Dengan V_{in} = 1 Volt

Dengan ADC internal menggunakan resolusi 10 bit dan pengujian dilakukan dengan kenaikan 250mV. Hasil pengujian keluaran ADC menunjukkan terjadi selisih yag kecil dengan hasil perhitungan yaitu ±1 bit, selisih ini tidak memberikan pengaruh yang signifikan terhadap perancangan, sehingga ADC internal ATMega 16 disimpulkan memiliki performa yang baik. Pengujian ini juga merupakan pengujian penampilan LCD karena keluaran ADC ditampilkan pada LCD. Penampilan LCD dapat dilihat pada gambar 4.8 :

Gambar 4.8 Pengujian Penampilan LCD

4.4 Pengujian Penampil Suara ISD 2590

- **Tujuan :**

Tujuan dari pengujian sistem ini adalah mengetahui respon output suara yang dihasilkan ISD dengan mengukur tegangan speaker saat play ISD.

- **Peralatan :**

Peralatan yang diperlukan untuk melakukan pengujian penampilan suara adalah sebagai berikut :

- ✓ Power *supply*
- ✓ Rangkaian *ISD2590*
- ✓ Speaker
- ✓ Multimeter digital

- **Prosedur :**

Prosedur yang dilakukan untuk pengujian penampil suara ISD adalah dengan cara memasukkan alamat ISD, pin P/R ISD dalam kondisi High (1), kemudian memberikan pulsa pada pin CE. Selanjutnya ISD akan mem-play voice tergantung alamat yang diset. Dan output dapat diukur pada pin speaker ISD untuk mengetahui adanya sinyal suara yang sedang dimainkan. Output suara dapat diukur dalam bentuk tegangan AC.

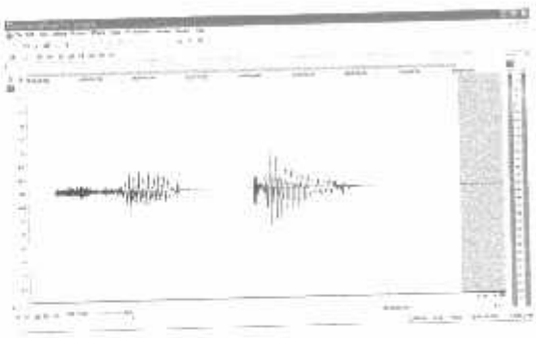
- **Hasil Pengujian dan Analisa :**

Setelah dilakukan pengujian, didapatkan hasil pengujian penampil suara yang berupa tegangan dari IC ISD. Hasil pengujian ditunjukkan dalam Tabel 4.3 :

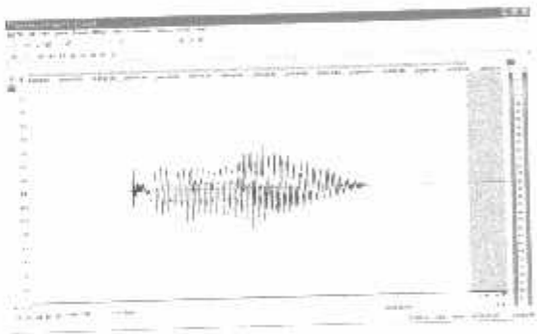
Tabel 4.3 Pengujian Penampil Suara

Time	Tegangan (V)
1 second	274 mV AC
1.5 second	322 mV AC

Dari hasil pengujian sebagimana tabel 4.3, dapat dilihat besar tegangan yang dihasilkan, seperti yang ditunjukkan pada gambar 4.9 dan gambar 4.10 :



Gambar 4.9 Sinyal dan Tegangan Speaker Pada Saat 1 Second



Gambar 4.10 Sinyal dan Tegangan Speaker Pada Saat 1.5 Second

Dari foto hasil pengujian sebagimana gambar 4.9 dan gambar 4.10 amplitudo tegangan AC yang terukur pada ouput speaker dari rangkaian ISD berkisar antara 270mV AC hingga 335mV AC. Sinyal yang terukur berubah-ubah mengikuti besar kecilnya suara yang dihasilkan ISD. Dengan demikian, pengujian ISD dinyatakan berhasil dan sesuai sebagaimana perancangan.

4.5 Pengujian Sistem Secara Keseluruhan

- **Tujuan**

Tujuan dari pengujian sistem secara keseluruhan adalah untuk mengetahui unjuk kerja dari sistem yang telah direncanakan, apakah sistem keseluruhan ini sudah dapat bekerja sesuai dengan perancangan yang ditetapkan.

- **Peralatan :**

Peralatan yang diperlukan untuk melakukan pengujian terhadap sistem secara keseluruhan adalah sebagai berikut :

- ✓ Power supply
- ✓ Multimeter digital sebagai pembanding
- ✓ Beban, berupa lampu dengan daya bervariasi
- ✓ Perangkat terangkai sensor dan sistem mokrokontroller

- **Prosedur :**

Prosedur yang dilakukan untuk pengujian system secara keseluruhan adalah dengan merangkai sistem, beban, power supply, dan multimeter sebagai pembanding, menyalakan sistem, kemudian mengalirkan arus pada beban dengan nilai bervariasi.

- **Hasil Pengujian dan Analisa :**

Setelah dilakukan pengujian, didapatkan hasil pengujian sistem kesceluruhan yang berupa tampilan besar arus terukur pada penampil LCD, hasil pengujian ditunjukkan dalam Tabel 4.4:

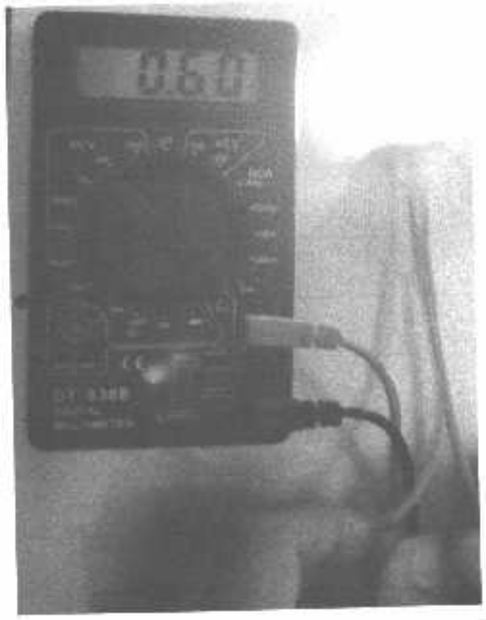
Tabel 4.4. Pengujian sistem keseluruhan

No	Arus Multimeter (A)	Tampilan Alat yang Dibuat (A)	Selisih (%)
1	0.00	0.00	0
2	0.40	0.40	0
3	0.60	0.60	0
4	1.00	1.00	0
rata-rata selisih			0

Dari tabel 4.4 dapat dilihat perbandingan antara arus dari pengukuran yang memakai multimeter digital sebagai pembangding dari alat yang dibuat dengan beban yang berbeda pada gambar 4.11, gambar 4.12, gambar 4.13 dan gambar 4.14 :

Gambar 4.11 Pengujian Dengan Multimeter Beban 1

Gambar 4.12 Pengujian Dengan Alat Yang Dibuat Beban 1



Gambar 4.13 Pengujian Dengan Multimeter Beban II

Gambar 4.14 Pengujian Dengan Alat Yang Dibuat Beban II

Dari pengujian didapatkan bahwa rata-rata selisih sekitar 0%. Hasil pengujian yang menunjukkan bahwa perubahan terkecil yang bisa dibaca adalah 0,01A pada beberapa sampel. Dari pengujian sistem secara keseluruhan tersebut mununjukkan bahwa sistem ini telah berjalan sesuai dengan yang diharapkan pada perancangan.

4.6. Spesifikasi Alat

Setelah melalui proses perencanaan dan pengujian alat, maka didapatkan spesifikasi sebagai berikut :

- Dimensi Panjang X Lebar X Tinggi alat : 17,5cm X 10,5cm X 3,5cm
- Tegangan input : DC 9V
- Sensor Arus : ACS712 (*Hall Effect*)
- Kapasitas Pengukuran 0 s/d 20 Ampere
- LCD M1632 atau 16X2 Karakter
- IC ISD2590
- Speaker

Foto Alat:

Gambar 4.15 Amperemeter Arus Searah Digital *Hall Effect* Sensor Dengan Output Suara

BAB V

PENUTUP

5.1 Kesimpulan

Setelah dilakukan proses perancangan dan pembuatan serta pegujian alat maka dapat diambil kesimpulan :

- Sensor *Hall Effect* ACS712 dapat melakukan pembacaan arus AC dan DC dengan error 0,04 %.
- Hasil pengujian ADC memiliki selisih yang kecil dengan tingkat error ±1 bit, selisih ini tidak memberikan pengaruh yang signifikan terhadap perancangan, sehingga ADC internal ATMega 16 disimpulkan memiliki performa yang baik.
- Penampil suara ISD2590 mampu mengeluarkan suara pada speaker dengan pengaturan mode dan alamat yang sesuai dengan masukan arus yang dibaca mikrokontroller ATMEGA16
- Software yang dirancang dapat melakukan konversi input ADC, kalkulasi data ADC menjadi arus dan mengolah data untuk diampilkan LCD dan ISD.

5.2 Saran

Dalam perancangan alat ini penyusun menyadari alat yang dirancang ini masih memiliki keterbatasan, untuk itu diharapkan dapat dikembangkan untuk meminimkan keterbatasan tersebut, diantaranya:

- Sensor ACS712 sangat terpengaruh oleh medan maghnet luar, sehingga menyebabkan hasil tidak akurat, untuk itu penempatan sensor pada papan PCB dan desain Box alat perlu dipertimbangkan ulang untuk menghindari hal tersebut.
- Perhatikan parameter ADC yang dipilih, masukan Vreff ADC dan kalkulasi software yang masih sering berubah-ubah pada hasil pengujian. Untuk itu diperlukan pengembangan untuk dapat menstabilkan data ADC tersebut.
- Suara yang dihasilkan masih tersendat-sendat dan lama pada saat play masing-masing alamat ISD, untuk itu pemiliha mode dan pengaturan address ISD perlu dikembangkan untuk mendapatkan kinerja yang efisien dan cepat pada proses play voice ISD.

- Daya system yang dibutuhkan sangat besar dan boros terhadap batteray, untuk itu pemilihan item-item komponen dari blok diagram perlu dikembangkan menggunakan komponen yang hemat energy.

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LAMPIRAN

PERKUMPULAN PENGELOLA PENDIDIKAN UMUM DAM TEKNOLOGI NASIONAL MALANG
INSTITUT TEKNOLOGI NASIONAL MALANG
FAKULTAS TEKNOLOGI INDUSTRI
FAKULTAS TEKNIK SIPIL DAN PERENCANAAN
PROGRAM PASCASARJANA MAGISTER TEKNIK
PT. BNI (PERSERO) MALANG
BANK NIAGA MALANG
Kampus I : Jl. Bendungan Sigura-gura No. 2 Telp. (0341) 551431 (Hunting), Fax. (0341) 553015 Malang 65145
Kampus II : Jl. Raya Karanglo, Km 2 Telp. (0341) 417636 Fax. (0341) 417634 Malang

BERITA ACARA UJIAN SKRIPSI
FAKULTAS TEKNOLOGI INDUSTRI

Nama : Adi Dwi Cahyanto

NIM : 06.12.227

Jurusan : Teknik Elektro S-1

Konsentrasi : Teknik Elektronika

Judul Skripsi : **PERANCANGAN DAN PEMBUATAN AMPEREMETER ARUS SEARAH DIGITAL HALL *EFFECT* SENSOR DENGAN OUTPUT SUARA**

Dipertahankan dihadapan Majelis Penguji Skripsi Jenjang Strata Satu (S-1) pada :

Hari : Rabu

Tanggal : 22 Februari 2012

Dengan Nilai : 84 (A)

Panitia Ujian Skripsi,

Ketua Majelis Penguji

Ir. Yusuf Ismail Nakhoda, MT
NIP.Y.1018800189

Sekretaris Majelis Penguji

Dr. Eng. Aryuanto Soetedjo, ST. MT
NIP.Y.1030800417

Anggota Penguji,

Penguji I

Teguh Herbasuki. Ir. MT
NIP.Y. 1038900209

Penguji II

Michael Ardita, ST, MT
NIP.P. 1031000434

INSTITUT TEKNOLOGI NASIONAL MALANG
FAKULTAS TEKNOLOGI INDUSTRI
JURUSAN TEKNIK ELEKTRO S-1
Jl. Karanglo KM.2 Malang

FORMULIR PERBAIKAN SKRIPSI

Nama : Adi Dwi Cahyanto
Nim : 06.12.227
Jurusan : Teknik Elektro S-1
Konsentrasi : Teknik Elektronika
Masa Bimbingan : 09 Desember 2011 – 09 Juni 2012
Judul Skripsi : **PERANCANGAN DAN PEMBUATAN AMPEREMETER ARUS SEARAH DIGITAL *HALL EFFECT* SENSOR DENGAN OUTPUT SUARA**

No	Penguji	Tanggal	Uraian	Paraf
1.	Penguji I	22 Februari 2012	1. Harap ditunjukkan apa yang dirancang (yang dihitung).	
2.	Penguji II	22 Februari 2012	1. Rumusan masalah : Tambahkan masalah "menyuarakan" display ampercmeter 2. Bab III • Perlu tambahkan pengkondisi sinyal (signal conditioner) dan perhitungan. • Offset 2,5V dari sensor perlu dimasukkan pada flowchart 3. Bab IV • Grafik dari datasheet seharusnya masuk pada bab III sebagai dasar perancangan • Pengujian suara perlu diperbaiki	

Disetujui

Penguji I

Teguh Herbasuki. Ir. MT
NIP.Y. 1038900209

Penguji II

Michael Ardita, ST, MT
NIP.P. 1031000434

Mengetahui

Dosen Pembimbing I

M. Ibrahim Ashari, ST, MT
NIP. P. 1030100358

Dosen Pembimbing II

Ir. Eko Nurcahyo
NIP.Y 1039100309

INSTITUT TEKNOLOGI NASIONAL
Jl. Raya Karanglo, KM 2
MALANG

FORMULIR BIMBINGAN SKRIPSI

Nama : Adi Dwi Cahyanto
Nim : 06.12.227
Masa Bimbingan : 9 Desember 2011 s/d 9 Juni 2012
Judul Skripsi : **Perancangan dan Pembuatan Amperemeter Arus Searah Digital *Hall Effect* Sensor Dengan Output Suara**

No	Tanggal	Uraian	Paraf Pembimbing
1	10 des 2011	Bab I acc.	
2	20 des 2011	Bab II acc	
3	22 des 2011	Bab III revisi	
4	3 jan 201	Bab IV revisi	
5	2 feb 2011	Bab V revisi	
6			
7			
8			
9			
10			

Malang, 2012
Dosen Pembimbing I

M. Ibrahim Ashari, ST, MT
NIP.P.1010100358

Form S-4b

INSTITUT TEKNOLOGI NASIONAL
Jl. Raya Karanglo, KM 2
MALANG

FORMULIR BIMBINGAN SKRIPSI

Nama : Adi Dwi Cahyanto
Nim : 06.12.227
Masa Bimbingan : 9 Desember 2011 s/d 9 Juni 2012
Judul Skripsi : **Perancangan dan Pembuatan Amperemeter Arus Searah Digital *Hall Effect* Sensor Dengan Output Suara**

No	Tanggal	Uraian	Paraf Pembimbing
1	10 des 2011	Bab I acc	
2	26 des 2011	Bab II acc	
3	28 des 2011	Bab III acc	
4	5 jan 2012	Bab IV Revisi	
5	2 Feb 2012	Bab V Revisi	
6			
7			
8			
9			
10			

Malang, 2012
Dosen Pembimbing II

Ir. Eko Nurcahyo
NIP.Y.1028700172

Form S-4b

INSTITUT TEKNOLOGI NASIONAL
Jl. Raya Karanglo, Km. 2
MALANG

PERMOHONAN PERSETUJUAN SKRIPSI

Yang betanda tangan dibawah ini :

Nama	: ADI DWI CAHYANTO
NIM	: 0612227
Semester	: 10
Fakultas	: Teknologi Industri
Jurusan	: Teknik Elektro S-1
Konsentrasi	: **TEKNIK ELEKTRONIKA**
	~~**TEKNIK ENERGI LISTRIK**~~
	~~**TEKNIK KOMPUTER DAN INFORMATIKA**~~
	~~**TEKNIK KOMPUTER**~~
	~~**TEKNIK TELEKOMUNIKASI**~~
Alamat	: Jl. Gamalama EE7 Tidar

Dengan ini kami mengajukan permohonan untuk mendapatkan persetujuan untuk membuat ***SKRIPSI Tingkat Sarjana.*** Untuk melengkapi permohonan tersebut, bersama kami lampirkan persyaratan-persyaratan yang harus dipenuhi.
Adapun persyaratan-persyaratan pengambilan ***SKRIPSI*** adalah sebagai berikut :

1. Telah melaksanakan semua praktikum sesuai dengan konsentrasinya (...✓...)
2. Telah lulus dan menyerahkan Laporan Praktek Kerja (...✓...)
3. Telah lulus seluruh mata kuliah keahlian (MKB) sesuai konsentrasinya (...✓...)
4. Telah menempuh mata kuliah ≥ 134 sks dengan IPK ≥ 2 dan tidak ada nilai E (...✓...)
5. Telah mengikuti secara aktif kegiatan seminar skripsi yang diadakan Jurusan (.......)
6. Memenuhi persyaratan administrasi (.......)

Demikian permohonan ini untuk mendapatkan penyelesaian lebih lanjut dan atas perhatiannya kami ucapkan terima kasih.

Telah diteliti kebenaran data tersebut diatas
Recording Teknik Elektro

(Pr. Hindi Nangkayani)

Malang, 31 maret 2011
Pemohon

(ADI DWI CAHYANTO)

Disetujui
Ketua Jurusan Teknik Elektro

Ir. Yusuf Ismail Nakhoda, MT
NIP. Y. 1018800189

Mengetahui
Dosen Wali

(Ir. Yusuf Ismail Nakhoda, MT)
NIP. Y. 1018800189

Catatan :
Bagi mahasiswa yang telah memenuhi persyaratan mengambil SKRIPSI agar membuat proposal dan mendapat persetujuan dari Ketua Jurusan/Sekretaris Jurusan T. Elektro S-1

1. IPK 383/ = 2.78
2. 138
3. 3 matakuliah

INSTITUT TEKNOLOGI NASIONAL MALANG
Kampus I : Jl. Bendungan Sigura-gura No.2
Kampus II: Jl. Raya Karanglo Km.2

Lampiran : 1 (satu) berkas
Pembimbing Skripsi

Kepada : Yth. Bapak **M. Ibrahim Ashari, ST, MT**
Dosen Institut Teknologi Nasional
MALANG

Yang bertanda tangan di bawah ini :

Nama	: Adi Dwi Cahyanto
Nim	: 06.12.227
Jurusan	: Teknik Elektro S-1
Konsentrasi	: **Teknik Elektronika**

Dengan ini mengajukan permohonan, kiranya Bapak bersedia menjadi Dosen Pembimbing Utama / Pendamping *), untuk penyusunan Skripsi dengan judul (proposal terlampir) :

"PERANCANGAN DAN PEMBUATAN AMPEREMETER ARUS SEARAH DIGITAL *HALL EFFECT* SENSOR DENGAN OUTPUT SUARA"

Adapun tugas tersebut sebagai salah satu syarat untuk menempuh Ujian Akhir Sarjana Teknik.
Demikian permohonan kami dan atas kesediaan Bapak kami ucapkan terima kasih.

Malang, 26 Mei 2011

Ketua
Jurusan Teknik Elektro S-1

Ir. Yusuf Ismail Nakhoda, MT
NIP. Y. 1018800189

Hormat kami,

Adi Dwi Cahyanto
NIM. 0612227

*) coret yang tidak perlu

Form S-3a

INSTITUT TEKNOLOGI NASIONAL MALANG
Kampus I : Jl. Bendungan Sigura-gura No.2
Kampus II: Jl. Raya Karanglo Km.2

Lampiran : 1 (satu) berkas
Pembimbing Skripsi

Kepada : Yth. Bapak **Ir. Eko Nurcahyo**
Dosen Institut Teknologi Nasional
MALANG

Yang bertanda tangan di bawah ini :

Nama	: Adi Dwi Cahyanto
Nim	: 06.12.227
Jurusan	: Teknik Elektro S-1
Konsentrasi	: **Teknik Elektronika**

Dengan ini mengajukan permohonan, kiranya Bapak bersedia menjadi Dosen Pembimbing Utama / Pendamping *), untuk penyusunan Skripsi dengan judul (proposal terlampir) :

"PERANCANGAN DAN PEMBUATAN AMPEREMETER ARUS SEARAH DIGITAL *HALL EFFECT* SENSOR DENGAN OUTPUT SUARA"

Adapun tugas tersebut sebagai salah satu syarat untuk menempuh Ujian Akhir Sarjana Teknik.
Demikian permohonan kami dan atas kesediaan Bapak kami ucapkan terima kasih.

Malang. 26 Mei 2011

Ketua
Jurusan Teknik Elektro S-1

Ir. Yusuf Ismail Nakhoda, MT
NIP. Y. 1018800189

Hormat kami,

Adi Dwi Cahyanto
NIM. 0612227

*) coret yang tidak perlu

Form S-3a

INSTITUT TEKNOLOGI NASIONAL MALANG
Kampus I : Jl. Bendungan Sigura-gura No.2
Kampus II: Jl. Raya Karanglo Km.2

PERNYATAAN KESEDIAAN DALAM PEMBIMBINGAN SKRIPSI

Sesuai permohonan dari mahasiswa :

Nama : Adi Dwi Cahyanto
Nim : 06.12.227
Semester : X (Sepuluh)
Jurusan : Teknik Elektro S-1
Konsentrasi : Teknik Elektronika

Dengan ini menyatakan bersedia / tidak bersedia *) membimbing Skripsi dari mahasiswa tersebut, dengan judul :

"PERANCANGAN DAN PEMBUATAN AMPEREMETER ARUS SEARAH DIGITAL *HALL EFFECT* SENSOR DENGAN OUTPUT SUARA"

Demikian surat pernyataan ini kami buat agar dapat dipergunakan seperlunya.

Malang, 26 Mei 2011

Kami yang Membuat Pernyataan,

M. Ibrahim Ashari, ST, MT
NIP. P. 1010100358

Catatan
Setelah disetujui agar formulir ini
Diserahkan mahasiswa yang bersangkutan
Kepada Jurusan untuk diproses lebih lanjut
*)coret yang tidak perlu

Form S-3b

INSTITUT TEKNOLOGI NASIONAL MALANG
Kampus I : Jl. Bendungan Sigura-gura No.2
Kampus II: Jl. Raya Karanglo Km.2

PERNYATAAN KESEDIAAN DALAM PEMBIMBINGAN SKRIPSI

Sesuai permohonan dari mahasiswa :

Nama : Adi Dwi Cahyanto
Nim : 06.12.227
Semester : X (Sepuluh)
Jurusan : Teknik Elektro S-1
Konsentrasi : Teknik Elektronika

Dengan ini menyatakan bersedia / tidak bersedia *) membimbing Skripsi dari mahasiswa tersebut, dengan judul :

"PERANCANGAN DAN PEMBUATAN AMPEREMETER ARUS SEARAH DIGITAL *HALL EFFECT* SENSOR DENGAN OUTPUT SUARA"

Demikian surat pernyataan ini kami buat agar dapat dipergunakan seperlunya.

Malang, 26 Mei 2011

Kami yang Membuat Pernyataan,

Ir. Eko Nurcahyo
NIP. Y. 1028700172

Catatan
Setelah disetujui agar formulir ini
Diserahkan mahasiswa yang bersangkutan
Kepada Jurusan untuk diproses lebih lanjut
*)coret yang tidak perlu

Form S-3b

Institut Teknologi Nasional Malang
Fakultas Teknologi Industri
Jurusan Teknik Elektro S-1

BERITA ACARA SEMINAR PROPOSAL SKRIPSI
JURUSAN TEKNIK ELEKTRO S-1

Konsentrasi : ~~Teknik Energi Listrik~~/Teknik Elektronika/ ~~Teknik Komputer & Informatika~~*)

1.	Nama Mahasiswa: ADI DWI CAHYANTO			Nim: 0612227
2.	Keterangan Pelaksanaan	Tanggal 9 Juni 2011	Waktu	Tempat Ruang:
3.	Spesifikasi Judul (berilah tanda silang)**) a. Sistem Tenaga Elektrik b. Energi & Konversi Energi c. Tegangan Tinggi & Pengukuran d. Sistem Kendali Industri	e. Elektronika & Komponen (f.) Elektronika Digital & Komputer g. Elektronika Komunikasi h. lainnya		
4.	Judul Proposal yang diseminarkan Mahasiswa	PERANCANGAN DAN PEMBUATAN AMPEREMETER ARUS SEARAH DIGITAL HALL EFFECT SENSOR DENGAN OUTPUT SUARA		
5.	Perubahan Judul yang diusulkan oleh Kelompok Dosen Keahlian			
6.	Catatan: Hall Effect di dalam prinsipnya Resolusi pengukuran 0 – 5 A -> ada ... dipikirkan ... keliniearan			
	Catatan:			
	Persetujuan Judul Skripsi			
7.	Disetujui, Dosen Keahlian I [signature]	Disetujui, Dosen Keahlian II [signature] Setyohadi, ST		
	Mengetahui, Ketua Jurusan, [signature] Ir. Yusuf Ismail Nakhoda, MT NIP.Y. 1018800189	Disetujui, Calon Dosen Pembimbing ybs Pembimbing I [signature] M. Ibrahim A	Pembimbing II	

Perhatian:
1. Keterangan: *) Coret yang tidak perlu
**) dilingkari a, b, c, ... atau g sesuai bidang keahlian

PERKUMPULAN PENGELOLA PENDIDIKAN UMUM DAN TEKNOLOGI NASIONAL MALANG
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FAKULTAS TEKNOLOGI INDUSTRI
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BANK NIAGA MALANG
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Kampus II : Jl. Raya Karanglo, Km 2 Telp. (0341) 417636 Fax. (0341) 417634 Malang

Malang, 14 Juni 2011

Nomor : **ITN- 304/7/TA /2011**
Lampiran :
Perihal : ***Bimbingan Skripsi***

Kepada : Yth. Sdr. **M. IBRAHIM ASHARI, ST, MT**
Dosen Pembimbing
Jurusan Teknik Elektro S-1
di
Malang

Dengan hormat,
Sesuai dengan permohonan dan persetujuan dalam proposal skipsi untuk mahasiswa:

Nama	: **ADI DWI CAHYANTO**
Nim	: **06 12 227**
Fakultas	: **Teknologi Industri**
Jurusan	: **Teknik Elektro S-1**
Konsentrasi	: **Teknik Elektronika S-1**

Maka dengan ini pembimbingan tersebut kami serahkan sepenuhnya kepada Saudara/i selama masa waktu 6 (enam) bulan, terhitung mulai tanggal:

09 JUNI 2011 s/d 09 DESEMBER 2011

Sebagai satu syarat untuk menempuh Ujian sarjana.
Demikian atas perhatian serta kerjasama yang baik kami ucapkan terima kasih

Ketua Jurusan
Teknik Elektro S-1

Ir. Yusuf Ismail Nakhoda, MT
NIP. Y. 1018800189

Tindasan:
1. Mahasiswa yang Bersangkutan
2. Arsip

Form S-4a

PERKUMPULAN PENGELOLA PENDIDIKAN UMUM DAN TEKNOLOGI NASIONAL MALANG
INSTITUT TEKNOLOGI NASIONAL MALANG
FAKULTAS TEKNOLOGI INDUSTRI
FAKULTAS TEKNIK SIPIL DAN PERENCANAAN
PROGRAM PASCASARJANA MAGISTER TEKNIK

PT. BNI (PERSERO) MALANG
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Kampus II : Jl. Raya Karanglo, Km 2 Telp. (0341) 417636 Fax. (0341) 417634 Malang

Malang, 14 Juni 2011

Nomor : **ITN- 305/7/TA /2011**
Lampiran :
Perihal : ***Bimbingan Skripsi***

Kepada : Yth. Sdr. **IR. EKO NURCAHYO**
Dosen Pembimbing
Jurusan Teknik Elektro S-1
di
Malang

Dengan hormat,
Sesuai dengan permohonan dan persetujuan dalam proposal skipsi untuk mahasiswa:

Nama	: **ADI DWI CAHYANTO**
Nim	: **06 12 227**
Fakultas	: **Teknologi Industri**
Jurusan	: **Teknik Elektro S-1**
Konsentrasi	: **Teknik Elektronika S-I**

Maka dengan ini pembimbingan tersebut kami serahkan sepenuhnya kepada Saudara/i selama masa waktu 6 (enam) bulan, terhitung mulai tanggal:

09 JUNI 2011 s/d 09 DESEMBER 2011

Sebagai satu syarat untuk menempuh Ujian sarjana.
Demikian atas perhatian serta kerjasama yang baik kami ucapkan terima kasih

Ketua Jurusan
Teknik Elektro S-1

Ir. Yusuf Ismail Nakhoda, MT
NIP. Y. 1018800189

Tindasan:
1. Mahasiswa yang Bersangkutan
2. Arsip

Form S-4a

LISTING PROGAM

```
'$sim
$regfile = "m16def.dat"
$crystal = 4000000

'Const Koma = 28

A0 Alias Portd.7
A1 Alias Portd.6
A2 Alias Portd.5
A3 Alias Portd.4
A4 Alias Portd.3
A5 Alias Portd.2
A6 Alias Portd.1
A7 Alias Portd.0
A8 Alias Portb.7
A9 Alias Portb.6

Play_rec Alias Portc.0
Eom Alias Pinc.1
Pd Alias Portb.2
Ce Alias Portb.3
Ovf Alias Pinb.4
Tombol_record Alias Pinb.1
Tombol_play Alias Pinb.0
Porta = &HFF
Portb = &HFF
Portc = &HFF
Portd = &HFF

Config A0 = Output
Config A1 = Output
Config A2 = Output
Config A3 = Output
Config A4 = Output
Config A5 = Output
Config A6 = Output
Config A7 = Output
Config A8 = Output

Config Play_rec = Output                                    'EOM
Config Portc.1 = Input
Config Pd = Output
Config Ce = Output                                          'ovf
Config Portb.4 = Input
Config Portb.0 = Input
Config Portb.1 = Input

Gosub Operational_mode

Const Belas = 12
Const Puluh = 13
Const Koma = 14
Const Miliamper = 15
Const Amper = 16
Const Minus = 17

Positif Alias 1
Negatif Alias 0

Config Lcdpin = Pin , Db4 = Portc.5 , Db5 = Portc.4 , Db6 = Portc.3 , Db7 =
Portc.2 , E = Portc.6 , Rs = Portc.7
Config Lcd = 16 * 2                                         'konfigurasi lcd 16*2

Config Adc = Single , Prescaler = Auto , Reference = Avcc

Start Adc
```

```
Enable Interrupts

Dim Data_adc As Word , Channel As Byte , Data_port As Byte , I As Integer
Dim Vamp As Single , Count_play As Integer , Count_rec As Integer
Dim Alamat_isd As Byte , Address As Byte , Arus As String * 8 , Temp As String *
2 , Hasil As String * 6
Dim Puluhan As Byte , Satuan As Byte , Tempw As Word
Dim Kalkulasi As Single , Flag As Bit
Dim Temps As String * 6
Cursor Off Noblink

Cls
Lcd "ADI DWI CAHYANTO"
Lowerline
Lcd "NIM:0612227  ITN"
Wait 2
Channel = 0
Cls
Lcd "Amperemeter      "
Lowerline
Lcd "Hall Effect      "
Wait 1
Cls
Lcd "  AMPERE METER  "
Lowerline
Lcd "Arus:     "
Do
      Locate 2 , 6
      Kalkulasi = 0
      For I = 1 To 100
         Data_adc = Getadc(channel)
         Vamp = Data_adc * 5
         Vamp = Vamp / 1024
         Kalkulasi = Kalkulasi + Vamp
      Next
      Kalkulasi = Kalkulasi / 100
      Temps = Fusing(vamp , "#.##")
      Vamp = Val(temps)

      Vamp = Kalkulasi - 2.5269
      Vamp = Vamp / 0.1                          'ACS 712-20A
      If Vamp <= 0.04 And Vamp >= -0.03 Then Vamp = 0
      Arus = Fusing(vamp , "#.##")
      Lcd Arus ; " A." ; Spc(4)
      If Tombol_play = 0 Then
         Hasil = ""
         Temp = Left(arus , 1)
         If Temp = "-" Then
            Flag = Negatif
            I = 2
         Else
            Flag = Positif
            I = 1
         End If

         Do
            Temp = Mid(arus , I , 1)
            I = I + 1
            If Temp <> "." Then Hasil = Hasil + Temp
         Loop Until Temp = "."
         Puluhan = Val(hasil)                                    'depan koma
         Hasil = Right(arus , 2)                                 '
         Satuan = Val(hasil)

         Gosub Cek_flag                                          'cek plus minus flag
```

```
        Alamat_isd = Puluhan
        Gosub Voice_play
        If Satuan <> 0 Then
           Address = Koma
           Gosub Play

           Alamat_isd = Satuan
           Gosub Voice_play
        End If
        Address = Amper                                    'mili amper
        Gosub Play

    End If
    Waitms 400
Loop

Cek_flag:
   If Flag = Negatif Then
      Address = Minus
      Gosub Play
   End If
Return

Voice_play:
      If Alamat_isd <= 11 Then
         Address = Alamat_isd
         Gosub Play
      Elseif Alamat_isd > 11 And Alamat_isd < 20 Then
         Address = Alamat_isd - 10
         Gosub Play
         Address = Belas
         Gosub Play
      Elseif Alamat_isd >= 20 And Alamat_isd < 100 Then
         If Alamat_isd >= 20 And Alamat_isd < 30 Then
            Address = 2
            Puluhan = Alamat_isd - 20
         End If
         If Alamat_isd >= 30 And Alamat_isd < 40 Then
            Address = 3
            Puluhan = Alamat_isd - 30
         End If
         If Alamat_isd >= 40 And Alamat_isd < 50 Then
            Address = 4
            Puluhan = Alamat_isd - 40
         End If
         If Alamat_isd >= 50 And Alamat_isd < 60 Then
            Address = 5
            Puluhan = Alamat_isd - 50
         End If
         If Alamat_isd >= 60 And Alamat_isd < 70 Then
            Address = 6
            Puluhan = Alamat_isd - 60
         End If
         If Alamat_isd >= 70 And Alamat_isd < 80 Then
            Address = 7
            Puluhan = Alamat_isd - 70
         End If
         If Alamat_isd >= 80 And Alamat_isd < 90 Then
            Address = 8
            Puluhan = Alamat_isd - 80
         End If
         If Alamat_isd >= 90 And Alamat_isd < 100 Then
         Address = 9
         Puluhan = Alamat_isd - 90
         End If
         Lowerline
'         Lcd Address ; ":"
```

```
         Gosub Play                                    'play address
         Address = Puluh
         Gosub Play
'         Lcd Address ; ":"

         If Puluhan <> 0 Then
            Address = Puluhan
'            Lcd Address ; ":"
            Gosub Play
         End If
      End If
Return

Operational_mode:
   Set Ce
   Set Pd
   Set Play_rec
   Waitms 10
   Reset A0
   Reset A1
   Reset A2
   Reset A3
   Reset A4
   Reset A5
   Set A6
   Reset A7
   Set A8
   Set A9
   Waitms 10
   Count_rec = 0
Return

Record:
   Reset Ce
   Waitus 1
   Set Ce
   Do
   Loop Until Tombol_record = 1
   'pause /EOM
   Reset Ce
   Waitus 1
   Set Ce
   Waitms 10
Return

Play:
   Set Pd
   Waitms 20
   Reset Pd
   Waitms 20
   Count_play = 0
   Set A0
   While Count_play < Address
      Reset Ce
      Waitus 1
      Set Ce
      Waitms 45
      Incr Count_play
   Wend
   Reset A0
    Reset Ce
   Waitus 1
   Set Ce
   Waitms 40
   Do
   Loop Until Eom = 0
Return
```

ACS712

Fully Integrated, Hall Effect-Based Linear Current Sensor IC with 2.1 kVRMS Isolation and a Low-Resistance Current Conductor

Features and Benefits

- Low-noise analog signal path
- Device bandwidth is set via the new FILTER pin
- 5 µs output rise time in response to step input current
- 80 kHz bandwidth
- Total output error 1.5% at $T_A = 25°C$
- Small footprint, low-profile SOIC8 package
- 1.2 mΩ internal conductor resistance
- 2.1 kVRMS minimum isolation voltage from pins 1-4 to pins 5-8
- 5.0 V, single supply operation
- 66 to 185 mV/A output sensitivity
- Output voltage proportional to AC or DC currents
- Factory-trimmed for accuracy
- Extremely stable output offset voltage
- Nearly zero magnetic hysteresis
- Ratiometric output from supply voltage

TÜV America
Certificate Number:
U8V 06 05 54214 010

Package: 8 Lead SOIC (suffix LC)

Approximate Scale 1:1

Description

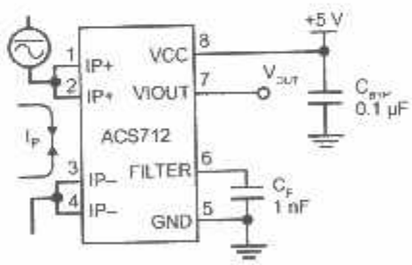
The Allegro® ACS712 provides economical and precise solutions for AC or DC current sensing in industrial, commercial, and communications systems. The device package allows for easy implementation by the customer. Typical applications include motor control, load detection and management, switch-mode power supplies, and overcurrent fault protection. The device is not intended for automotive applications.

The device consists of a precise, low-offset, linear Hall circuit with a copper conduction path located near the surface of the die. Applied current flowing through this copper conduction path generates a magnetic field which the Hall IC converts into a proportional voltage. Device accuracy is optimized through the close proximity of the magnetic signal to the Hall transducer. A precise, proportional voltage is provided by the low-offset, chopper-stabilized BiCMOS Hall IC, which is programmed for accuracy after packaging.

The output of the device has a positive slope (>$V_{IOUT(Q)}$) when an increasing current flows through the primary copper conduction path (from pins 1 and 2, to pins 3 and 4), which is the path used for current sampling. The internal resistance of this conductive path is 1.2 mΩ typical, providing low power loss. The thickness of the copper conductor allows survival of

Continued on the next page...

Typical Application



Application 1. The ACS712 outputs an analog signal, V_{OUT}, that varies linearly with the uni- or bi-directional AC or DC primary sampled current, I_P, within the range specified. C_F is recommended for noise management, with values that depend on the application.

Description (continued)

the device at up to 5× overcurrent conditions. The terminals of the conductive path are electrically isolated from the signal leads (pins 5 through 8). This allows the ACS712 to be used in applications requiring electrical isolation without the use of opto-isolators or other costly isolation techniques.

The ACS712 is provided in a small, surface mount SOIC8 package. The leadframe is plated with 100% matte tin, which is compatible with standard lead (Pb) free printed circuit board assembly processes. Internally, the device is Pb-free, except for flip-chip high-temperature Pb-based solder balls, currently exempt from RoHS. The device is fully calibrated prior to shipment from the factory.

Selection Guide

Part Number	Packing*	T_A (°C)	Optimized Range, I_P (A)	Sensitivity, Sens (Typ) (mV/A)
ACS712ELCTR-05B-T	Tape and reel, 3000 pieces/reel	–40 to 85	±5	185
ACS712ELCTR-20A-T	Tape and reel, 3000 pieces/reel	–40 to 85	±20	100
ACS712ELCTR-30A-T	Tape and reel, 3000 pieces/reel	–40 to 85	±30	66

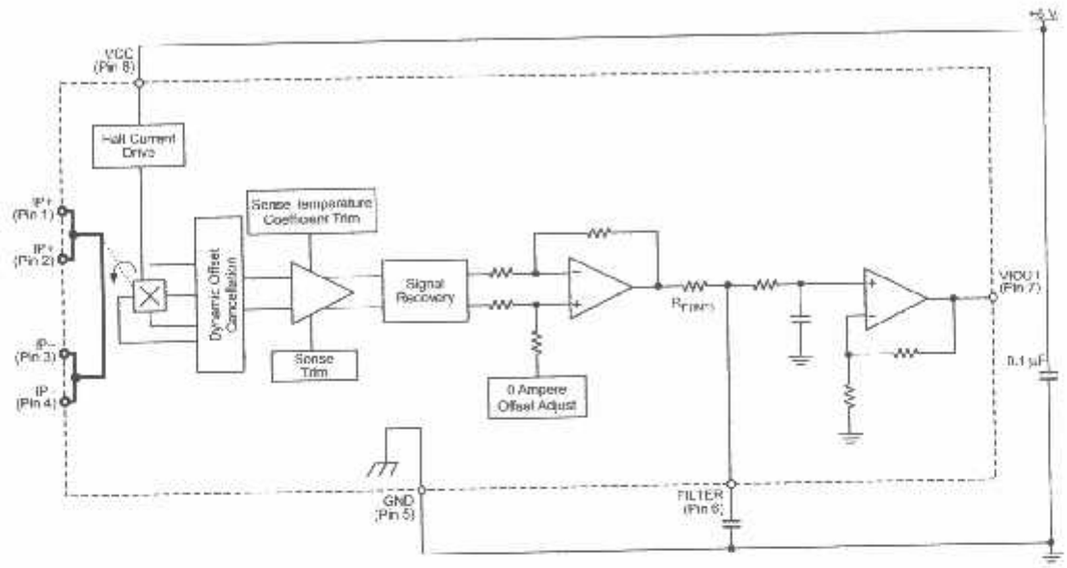
*Contact Allegro for additional packing options.

Absolute Maximum Ratings

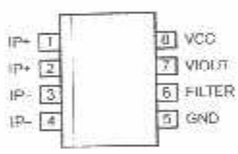
Characteristic	Symbol	Notes	Rating	Units
Supply Voltage	V_{CC}		8	V
Reverse Supply Voltage	V_{RCC}		–0.1	V
Output Voltage	V_{IOUT}		8	V
Reverse Output Voltage	V_{RIOUT}		–0.1	V
Reinforced Isolation Voltage	V_{ISO}	Pins 1-4 and 5-8; 60 Hz, 1 minute, T_A=25°C	2100	VAC
		Maximum working voltage according to UL60950-1	184	V_{peak}
Basic Isolation Voltage	$V_{ISO(bsc)}$	Pins 1-4 and 5-8; 60 Hz, 1 minute, T_A=25°C	1500	VAC
		Maximum working voltage according to UL60950-1	354	V_{peak}
Output Current Source	$I_{IOUT(Source)}$		3	mA
Output Current Sink	$I_{IOUT(Sink)}$		10	mA
Overcurrent Transient Tolerance	I_P	1 pulse, 100 ms	100	A
Nominal Operating Ambient Temperature	T_A	Range E	–40 to 85	°C
Maximum Junction Temperature	T_J(max)		165	°C
Storage Temperature	T_{stg}		–65 to 170	°C

Parameter	Specification
Fire and Electric Shock	CAN/CSA-C22.2 No. 60950-1-03 UL 60950-1:2003 EN 60950-1:2001

Functional Block Diagram



Pin-out Diagram



Terminal List Table

Number	Name	Description
1 and 2	IP+	Terminals for current being sampled; fused internally
3 and 4	IP–	Terminals for current being sampled; fused internally
5	GND	Signal ground terminal
6	FILTER	Terminal for external capacitor that sets bandwidth
7	VIOUT	Analog output signal
8	VCC	Device power supply terminal

COMMON OPERATING CHARACTERISTICS[1] over full range of T_A, C_F = 1 nF, and V_{CC} = 5 V, unless otherwise specified

Characteristic	Symbol	Test Conditions	Min.	Typ.	Max.	Units
ELECTRICAL CHARACTERISTICS						
Supply Voltage	V_{CC}		4.5	5.0	5.5	V
Supply Current	I_{CC}	V_{CC} = 5.0 V, output open	–	10	13	mA
Output Capacitance Load	C_{LOAD}	VIOUT to GND	–	–	10	nF
Output Resistive Load	R_{LOAD}	VIOUT to GND	4.7	–	–	kΩ
Primary Conductor Resistance	$R_{PRIMARY}$	T_A = 25°C	–	1.2	–	mΩ
Rise Time	t_r	I_P = I_P(max), T_A = 25°C, C_{OUT} = open	–	5	–	µs
Frequency Bandwidth	f	–3 dB, T_A = 25°C; I_P is 10 A peak-to-peak	–	80	–	kHz
Nonlinearity	E_{LIN}	Over full range of I_P	–	1.5	–	%
Symmetry	E_{SYM}	Over full range of I_P	98	100	102	%
Zero Current Output Voltage	$V_{IOUT(Q)}$	Bidirectional; I_P = 0 A, T_A = 25°C	–	V_{CC} × 0.5	–	V
Power-On Time	t_{PO}	Output reaches 90% of steady-state level, T_J = 25°C, 20 A present on leadframe	–	35	–	µs
Magnetic Coupling[2]			–	12	–	G/A
Internal Filter Resistance[3]	$R_{F(INT)}$			1.7		kΩ

[1]Device may be operated at higher primary current levels, I_P, and ambient, T_A, and internal leadframe temperatures, T_A, provided that the Maximum Junction Temperature, T_J(max), is not exceeded.

[2]1 G = 0.1 mT.

[3]$R_{F(INT)}$ forms an RC circuit via the FILTER pin.

COMMON THERMAL CHARACTERISTICS[1]

			Min.	Typ.	Max.	Units
Operating Internal Leadframe Temperature	T_A	E range	–40	–	85	°C
					Value	Units
Junction-to-Lead Thermal Resistance[2]	$R_{\theta JL}$	Mounted on the Allegro ASEK 712 evaluation board			5	°C/W
Junction-to-Ambient Thermal Resistance	$R_{\theta JA}$	Mounted on the Allegro 85-0322 evaluation board, includes the power consumed by the board			23	°C/W

[1]Additional thermal information is available on the Allegro website.

[2]The Allegro evaluation board has 1500 mm² of 2 oz. copper on each side, connected to pins 1 and 2, and to pins 3 and 4, with thermal vias connecting the layers. Performance values include the power consumed by the PCB. Further details on the board are available from the Frequently Asked Questions document on our website. Further information about board design and thermal performance also can be found in the Applications Information section of this datasheet.

x05B PERFORMANCE CHARACTERISTICS[1] T_A = –40°C to 85°C, C_F = 1 nF, and V_{CC} = 5 V, unless otherwise specified

Characteristic	Symbol	Test Conditions	Min.	Typ.	Max.	Units
Optimized Accuracy Range	I_P		–5	–	5	A
Sensitivity	Sens	Over full range of I_P, T_A = 25°C	180	185	190	mV/A
Noise	$V_{NOISE(PP)}$	Peak-to-peak, T_A = 25°C, 185 mV/A programmed Sensitivity, C_F = 47 nF, C_{OUT} = open, 2 kHz bandwidth	–	21	–	mV
Zero Current Output Slope	$\Delta I_{OUT(Q)}$	T_A = –40°C to 25°C	–	–0.26	–	mV/°C
		T_A = 25°C to 150°C	–	–0.08	–	mV/°C
Sensitivity Slope	ΔSens	T_A = –40°C to 25°C	–	0.054	–	mV/A/°C
		T_A = 25°C to 150°C	–	–0.008	–	mV/A/°C
Total Output Error[2]	E_{TOT}	I_P = ±5 A, T_A = 25°C	–	±1.5	–	%

[1]Device may be operated at higher primary current levels, I_P, and ambient temperatures, T_A, provided that the Maximum Junction Temperature, $T_{J(max)}$, is not exceeded.

[2]Percentage of I_P, with I_P = 5 A. Output filtered.

x20A PERFORMANCE CHARACTERISTICS[1] T_A = –40°C to 85°C, C_F = 1 nF, and V_{CC} = 5 V, unless otherwise specified

Characteristic	Symbol	Test Conditions	Min.	Typ.	Max.	Units
Optimized Accuracy Range	I_P		–20	–	20	A
Sensitivity	Sens	Over full range of I_P, T_A = 25°C	96	100	104	mV/A
Noise	$V_{NOISE(PP)}$	Peak-to-peak, T_A = 25°C, 100 mV/A programmed Sensitivity, C_F = 47 nF, C_{OUT} = open, 2 kHz bandwidth	–	11	–	mV
Zero Current Output Slope	$\Delta I_{OUT(Q)}$	T_A = –40°C to 25°C	–	–0.34	–	mV/°C
		T_A = 25°C to 150°C	–	–0.07	–	mV/°C
Sensitivity Slope	ΔSens	T_A = –40°C to 25°C	–	0.017	–	mV/A/°C
		T_A = 25°C to 150°C	–	–0.004	–	mV/A/°C
Total Output Error[2]	E_{TOT}	I_P = ±20 A, T_A = 25°C	–	±1.5	–	%

[1]Device may be operated at higher primary current levels, I_P, and ambient temperatures, T_A, provided that the Maximum Junction Temperature, T_J(max), is not exceeded.

[2]Percentage of I_P, with I_P = 20 A. Output filtered.

x30A PERFORMANCE CHARACTERISTICS[1] T_A = –40°C to 85°C, C_F = 1 nF, and V_{CC} = 5 V, unless otherwise specified

Characteristic	Symbol	Test Conditions	Min.	Typ.	Max.	Units
Optimized Accuracy Range	I_P		–30	–	30	A
Sensitivity	Sens	Over full range of I_P, T_A = 25°C	63	66	69	mV/A
Noise	$V_{NOISE(PP)}$	Peak-to-peak, T_A = 25°C, 66 mV/A programmed Sensitivity, C_F = 47 nF, C_{OUT} = open, 2 kHz bandwidth	–	7	–	mV
Zero Current Output Slope	$\Delta I_{OUT(Q)}$	T_A = –40°C to 25°C	–	–0.35	–	mV/°C
		T_A = 25°C to 150°C	–	–0.08	–	mV/°C
Sensitivity Slope	ΔSens	T_A = –40°C to 25°C	–	0.007	–	mV/A/°C
		T_A = 25°C to 150°C	–	–0.002	–	mV/A/°C
Total Output Error[2]	E_{TOT}	I_P = ±30 A, T_A = 25°C	–	±1.5	–	%

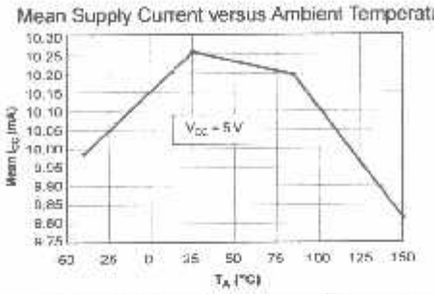
[1]Device may be operated at higher primary current levels, I_P, and ambient temperatures, T_A, provided that the Maximum Junction Temperature, T_J(max), is not exceeded.

[2]Percentage of I_P, with I_P = 30 A. Output filtered.

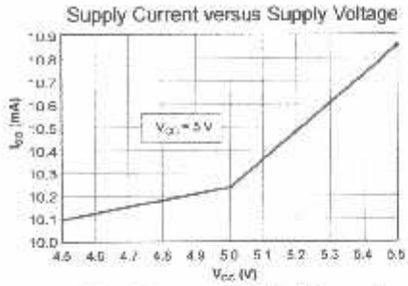
Characteristic Performance

I_P = 5 A, unless otherwise specified

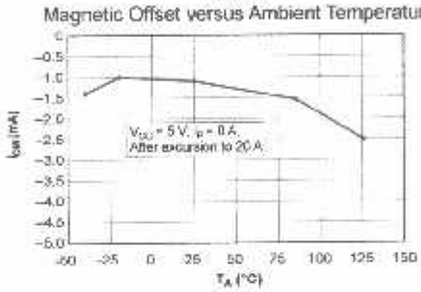
Mean Supply Current versus Ambient Temperature



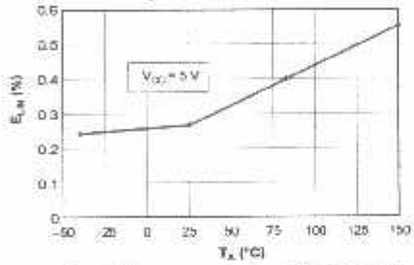
Supply Current versus Supply Voltage



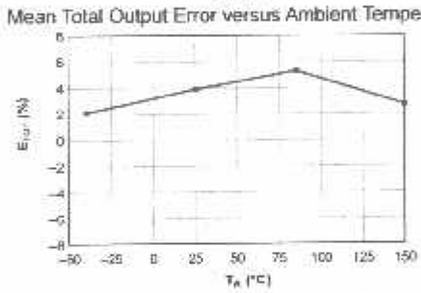
Magnetic Offset versus Ambient Temperature



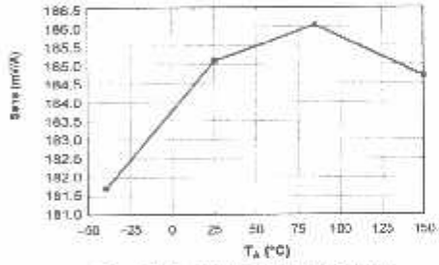
Nonlinearity versus Ambient Temperature



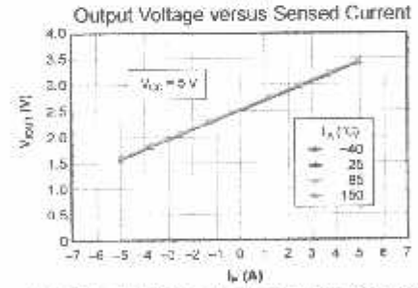
Mean Total Output Error versus Ambient Temperature



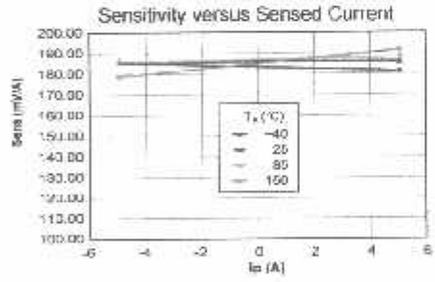
Sensitivity versus Ambient Temperature



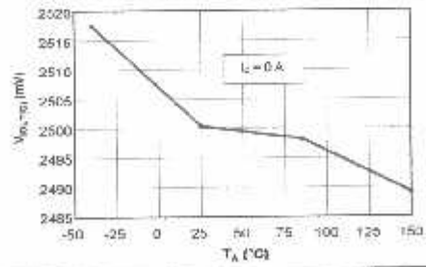
Output Voltage versus Sensed Current



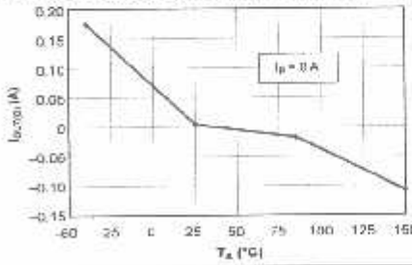
Sensitivity versus Sensed Current



0 A Output Voltage versus Ambient Temperature



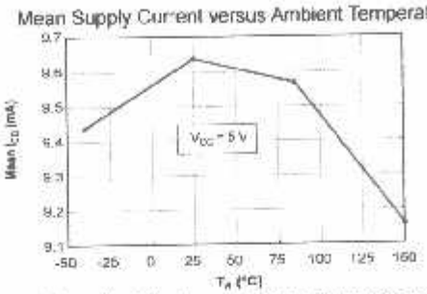
0 A Output Voltage Current versus Ambient Temperature



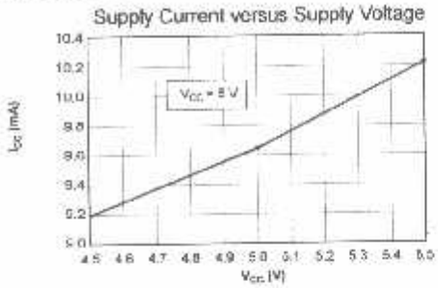
Characteristic Performance

I_P = 20 A, unless otherwise specified

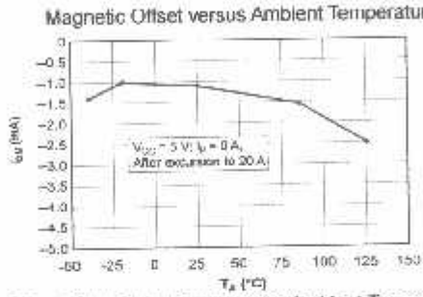
Mean Supply Current versus Ambient Temperature



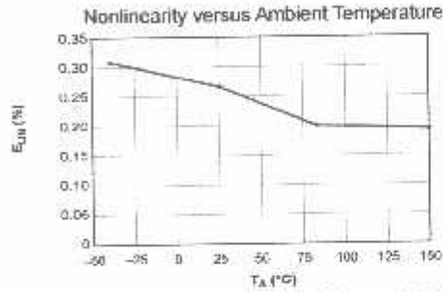
Supply Current versus Supply Voltage



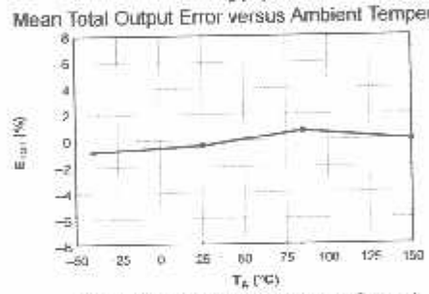
Magnetic Offset versus Ambient Temperature



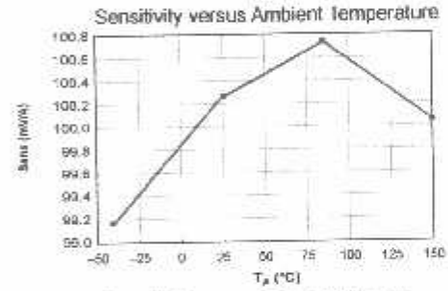
Nonlinearity versus Ambient Temperature



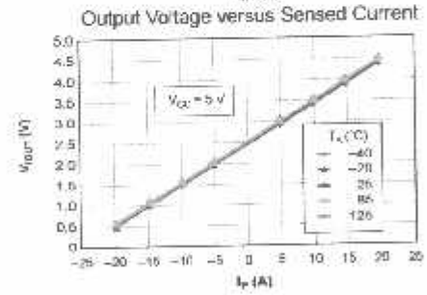
Mean Total Output Error versus Ambient Temperature



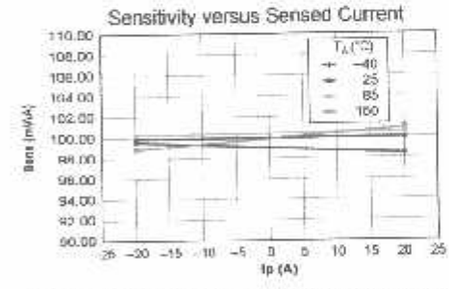
Sensitivity versus Ambient Temperature



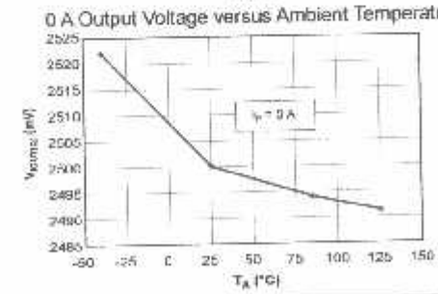
Output Voltage versus Sensed Current



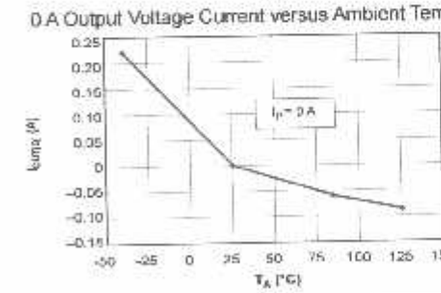
Sensitivity versus Sensed Current



0 A Output Voltage versus Ambient Temperature



0 A Output Voltage Current versus Ambient Temperature

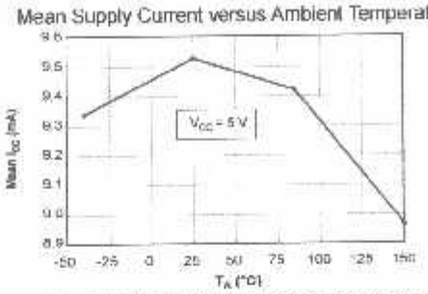


Allegro MicroSystems, Inc.
115 Northeast Cutoff
Worcester, Massachusetts 01615-0036 U.S.A.
1.508.853.5000 www.allegromicro.com

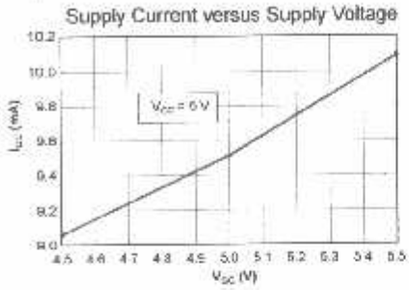
Characteristic Performance

I_P = 30 A, unless otherwise specified

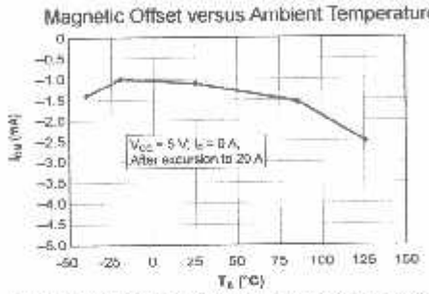
Mean Supply Current versus Ambient Temperature



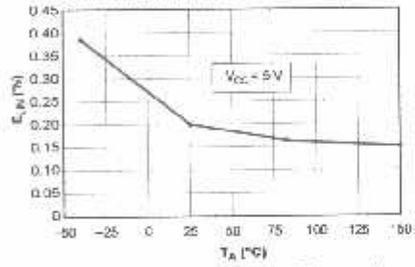
Supply Current versus Supply Voltage



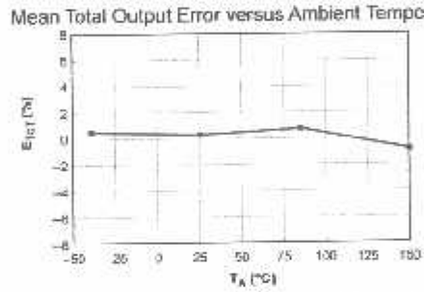
Magnetic Offset versus Ambient Temperature



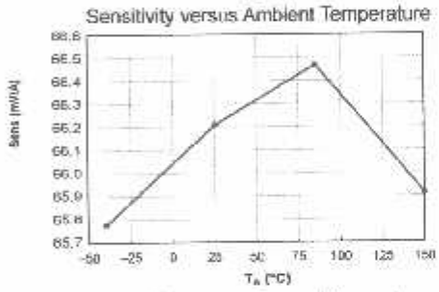
Nonlinearity versus Ambient Temperature



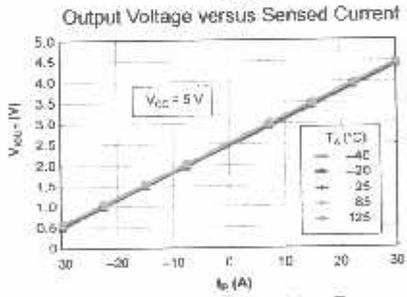
Mean Total Output Error versus Ambient Temperature



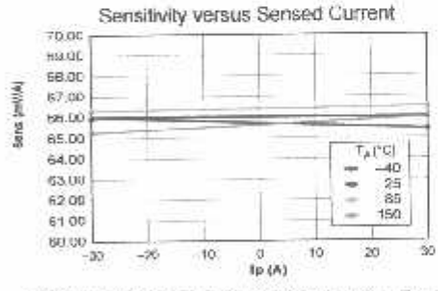
Sensitivity versus Ambient Temperature



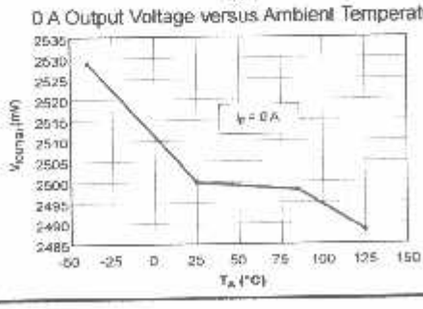
Output Voltage versus Sensed Current



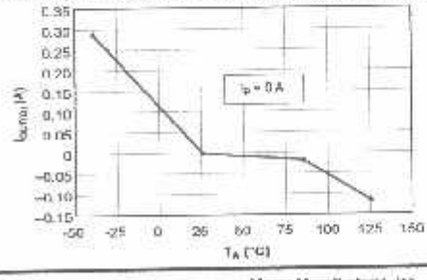
Sensitivity versus Sensed Current



0 A Output Voltage versus Ambient Temperature



0 A Output Voltage Current versus Ambient Temperature



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Definitions of Accuracy Characteristics

Sensitivity (Sens). The change in device output in response to a 1 A change through the primary conductor. The sensitivity is the product of the magnetic circuit sensitivity (G/A) and the linear IC amplifier gain (mV/G). The linear IC amplifier gain is programmed at the factory to optimize the sensitivity (mV/A) for the full-scale current of the device.

Noise (V_{NOISE}). The product of the linear IC amplifier gain (mV/G) and the noise floor for the Allegro Hall effect linear IC (≈1 G). The noise floor is derived from the thermal and shot noise observed in Hall elements. Dividing the noise (mV) by the sensitivity (mV/A) provides the smallest current that the device is able to resolve.

Linearity (E_{LIN}). The degree to which the voltage output from the IC varies in direct proportion to the primary current through its full-scale amplitude. Nonlinearity in the output can be attributed to the saturation of the flux concentrator approaching the full-scale current. The following equation is used to derive the linearity:

$$100 \left\{ 1 - \left[\frac{\Delta \text{ gain} \times \% \text{ sat} \left(V_{IOUT\_full\text{-}scale\ amperes} - V_{IOUT(Q)} \right)}{2 \left(V_{IOUT\_half\text{-}scale\ amperes} - V_{IOUT(Q)} \right)} \right] \right\}$$

where $V_{IOUT\_full\text{-}scale\ amperes}$ = the output voltage (V) when the sampled current approximates full-scale $\pm I_P$.

Symmetry (E_{SYM}). The degree to which the absolute voltage output from the IC varies in proportion to either a positive or negative full-scale primary current. The following formula is used to derive symmetry:

$$100 \left(\frac{V_{IOUT\_+\ full\text{-}scale\ amperes} - V_{IOUT(Q)}}{V_{IOUT(Q)} - V_{IOUT\_-full\text{-}scale\ amperes}} \right)$$

Quiescent output voltage ($V_{IOUT(Q)}$). The output of the device when the primary current is zero. For a unipolar supply voltage, it nominally remains at $V_{CC}/2$. Thus, V_{CC} = 5 V translates into $V_{IOUT(Q)}$ = 2.5 V. Variation in $V_{IOUT(Q)}$ can be attributed to the resolution of the Allegro linear IC quiescent voltage trim and thermal drift.

Electrical offset voltage (V_{OE}). The deviation of the device output from its ideal quiescent value of $V_{CC}/2$ due to nonmagnetic causes. To convert this voltage to amperes, divide by the device sensitivity, Sens.

Accuracy (E_{TOT}). The accuracy represents the maximum deviation of the actual output from its ideal value. This is also known as the total output error. The accuracy is illustrated graphically in the output voltage versus current chart at right.

Accuracy is divided into four areas:

- **0 A at 25°C.** Accuracy at the zero current flow at 25°C, without the effects of temperature.
- **0 A over Δ temperature.** Accuracy at the zero current flow including temperature effects.
- **Full-scale current at 25°C.** Accuracy at the the full-scale current at 25°C, without the effects of temperature.
- **Full-scale current over Δ temperature.** Accuracy at the full-scale current flow including temperature effects.

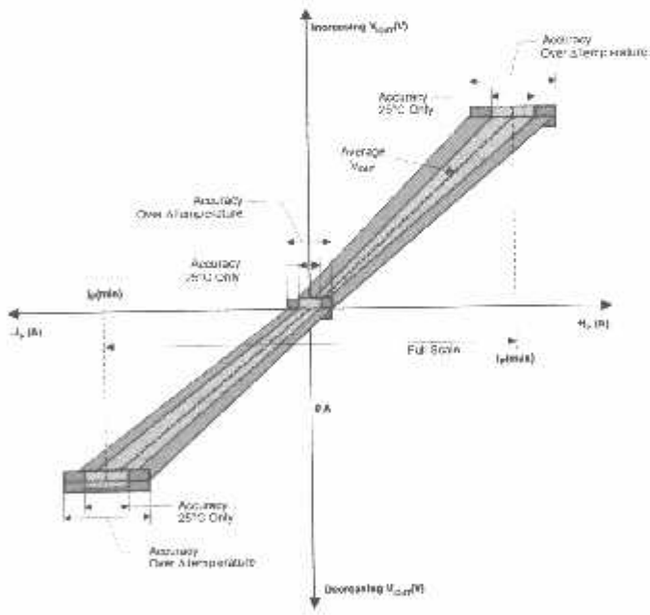
Ratiometry. The ratiometric feature means that its 0 A output, $V_{IOUT(Q)}$, (nominally equal to $V_{CC}/2$) and sensitivity, Sens, are proportional to its supply voltage, V_{CC}. The following formula is used to derive the ratiometric change in 0 A output voltage, $\Delta V_{IOUT(Q)RAT}$ (%).

$$100 \left(\frac{V_{IOUT(Q)VCC} / V_{IOUT(Q)5V}}{V_{CC} / 5\text{ V}} \right)$$

The ratiometric change in sensitivity, $\Delta Sens_{RAT}$ (%), is defined as:

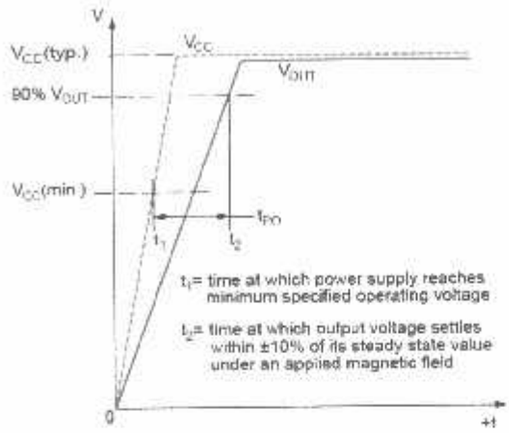
$$100 \left(\frac{Sens_{VCC} / Sens_{5V}}{V_{CC} / 5\text{ V}} \right)$$

Output Voltage versus Sampled Current
Accuracy at 0 A and at Full-Scale Current

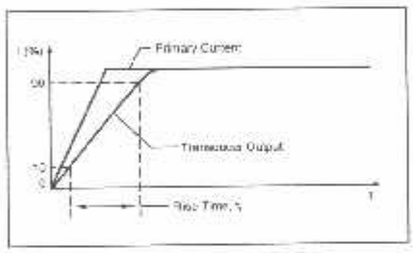


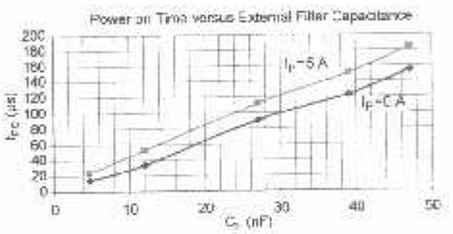
Definitions of Dynamic Response Characteristics

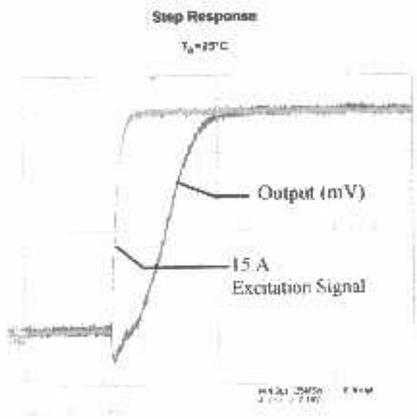
Power-On Time (t_{PO}). When the supply is ramped to its operating voltage, the device requires a finite time to power its internal components before responding to an input magnetic field. Power-On Time, t_{PO}, is defined as the time it takes for the output voltage to settle within ±10% of its steady state value under an applied magnetic field, after the power supply has reached its minimum specified operating voltage, V_{CC}(min), as shown in the chart at right.

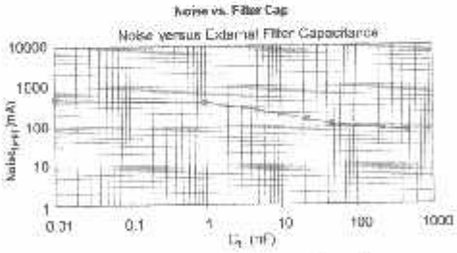


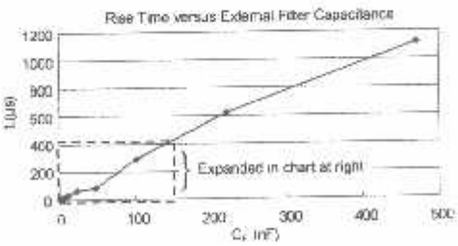
Rise time (t_r). The time interval between a) when the device reaches 10% of its full scale value, and b) when it reaches 90% of its full scale value. The rise time to a step response is used to derive the bandwidth of the device, in which $f(-3\ dB) = 0.35/t_r$. Both t_r and $t_{RESPONSE}$ are detrimentally affected by eddy current losses observed in the conductive IC ground plane.



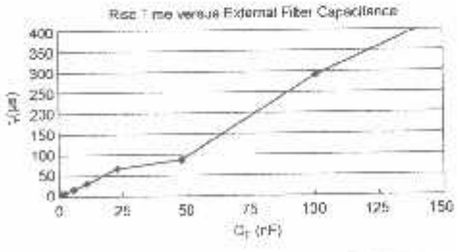








C_F (nF)	t_r (µs)
0	6.6
1	7.7
4.7	17.4
10	32.1
22	68.2
47	88.2
100	291.3
220	623.0
470	1120.0



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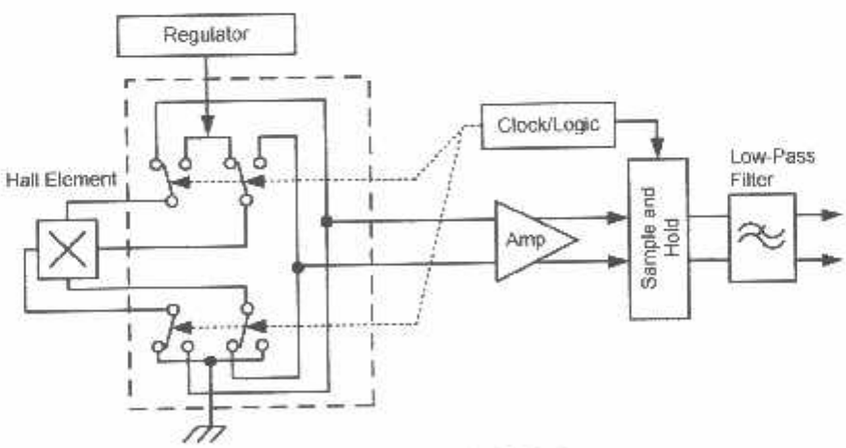
Chopper Stabilization Technique

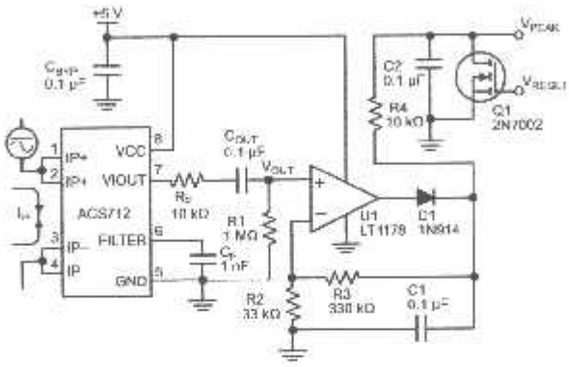
Chopper Stabilization is an innovative circuit technique that is used to minimize the offset voltage of a Hall element and an associated on-chip amplifier. Allegro patented a Chopper Stabilization technique that nearly eliminates Hall IC output drift induced by temperature or package stress effects. This offset reduction technique is based on a signal modulation-demodulation process. Modulation is used to separate the undesired DC offset signal from the magnetically induced signal in the frequency domain. Then, using a low-pass filter, the modulated DC offset is suppressed while the magnetically induced signal passes through the filter. As a result of this chopper stabilization approach, the output voltage from the Hall IC is desensitized to the effects of temperature and mechanical stress. This technique produces devices that have an extremely stable Electrical Offset Voltage, are immune to thermal stress, and have precise recoverability after temperature cycling.

This technique is made possible through the use of a BiCMOS process that allows the use of low-offset and low-noise amplifiers in combination with high-density logic integration and sample and hold circuits.

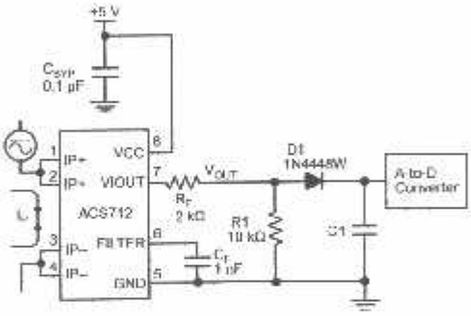


Concept of Chopper Stabilization Technique

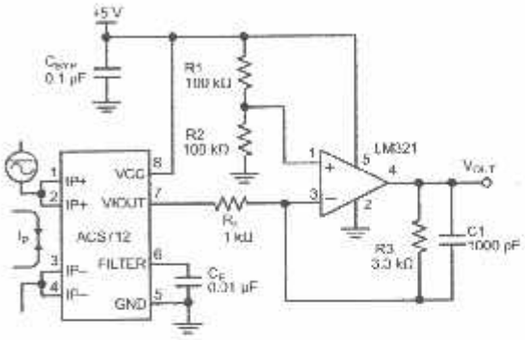
Typical Applications



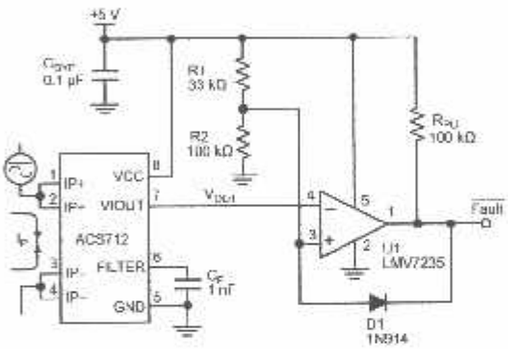
Application 2. Peak Detecting Circuit



Application 4. Rectified Output. 3.3 V scaling and rectification application for A-to-D converters. Replaces current transformer solutions with simpler ACS circuit. C1 is a function of the load resistance and filtering desired. R1 can be omitted if the full range is desired.



Application 3. This configuration increases gain to 610 mV/A (tested using the ACS712ELC-05A).



Application 5. 10 A Overcurrent Fault Latch. Fault threshold set by R1 and R2. This circuit latches an overcurrent fault and holds it until the 5 V rail is powered down.

Improving Sensing System Accuracy Using the FILTER Pin

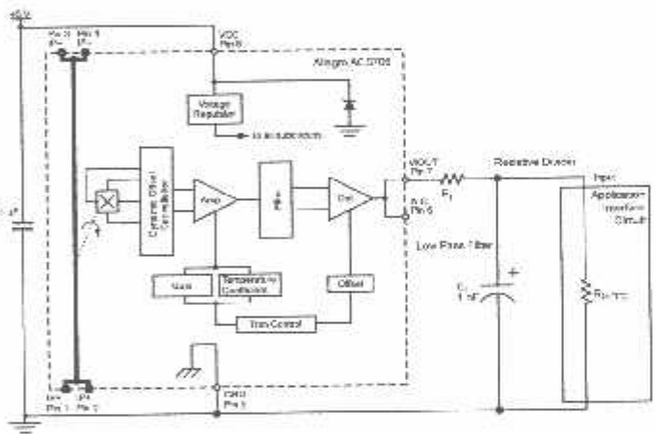
In low-frequency sensing applications, it is often advantageous to add a simple RC filter to the output of the device. Such a low-pass filter improves the signal-to-noise ratio, and therefore the resolution, of the device output signal. However, the addition of an RC filter to the output of a sensor IC can result in undesirable device output attenuation — even for DC signals.

Signal attenuation, ΔV_{ATT}, is a result of the resistive divider effect between the resistance of the external filter, R_F (see Application 6), and the input impedance and resistance of the customer interface circuit, R_{INTFC}. The transfer function of this resistive divider is given by:

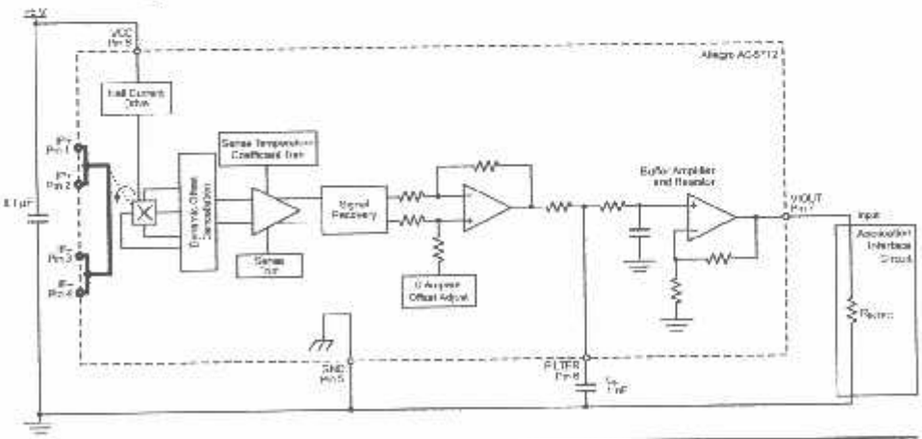
$$\Delta V_{ATT} = V_{IOUT}\left(\frac{R_{INTFC}}{R_F + R_{INTFC}}\right) .$$

Even if R_F and R_{INTFC} are designed to match, the two individual resistance values will most likely drift by different amounts over temperature. Therefore, signal attenuation will vary as a function of temperature. Note that, in many cases, the input impedance, R_{INTFC}, of a typical analog-to-digital converter (ADC) can be as low as 10 kΩ.

The ACS712 contains an internal resistor, a FILTER pin connection to the printed circuit board, and an internal buffer amplifier. With this circuit architecture, users can implement a simple RC filter via the addition of a capacitor, C_F (see Application 7) from the FILTER pin to ground. The buffer amplifier inside of the ACS712 (located after the internal resistor and FILTER pin connection) eliminates the attenuation caused by the resistive divider effect described in the equation for ΔV_{ATT}. Therefore, the ACS712 device is ideal for use in high-accuracy applications that cannot afford the signal attenuation associated with the use of an external RC low-pass filter.



Application 6. When a low pass filter is constructed externally to a standard Hall effect device, a resistive divider may exist between the filter resistor, R_F, and the resistance of the customer interface circuit, R_{INTFC}. This resistive divider will cause excessive attenuation, as given by the transfer function for ΔV_{ATT}.



Application 7. Using the FILTER pin provided on the ACS712 eliminates the attenuation effects of the resistor divider between R_F and R_{INTFC}, shown in Application 6.

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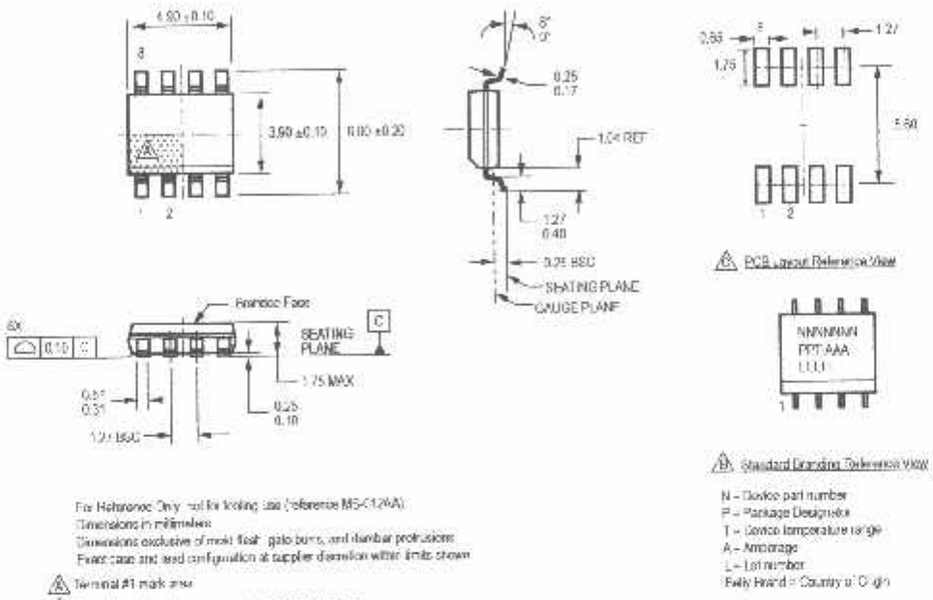
Package LC, 8-pin SOIC



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www.allegromicro.com

Features

- High-performance, Low-power Atmel® AVR® 8-bit Microcontroller
- Advanced RISC Architecture
  - 131 Powerful Instructions – Most Single-clock Cycle Execution
  - 32 x 8 General Purpose Working Registers
  - Fully Static Operation
  - Up to 16 MIPS Throughput at 16 MHz
  - On-chip 2-cycle Multiplier
- High Endurance Non-volatile Memory segments
  - 16 Kbytes of In-System Self-programmable Flash program memory
  - 512 Bytes EEPROM
  - 1 Kbyte Internal SRAM
  - Write/Erase Cycles: 10,000 Flash/100,000 EEPROM
  - Data retention: 20 years at 85°C/100 years at 25°C[1]
  - Optional Boot Code Section with Independent Lock Bits
    In-System Programming by On-chip Boot Program
    True Read-While-Write Operation
  - Programming Lock for Software Security
- JTAG (IEEE std. 1149.1 Compliant) Interface
  - Boundary-scan Capabilities According to the JTAG Standard
  - Extensive On-chip Debug Support
  - Programming of Flash, EEPROM, Fuses, and Lock Bits through the JTAG Interface
- Peripheral Features
  - Two 8-bit Timer/Counters with Separate Prescalers and Compare Modes
  - One 16-bit Timer/Counter with Separate Prescaler, Compare Mode, and Capture Mode
  - Real Time Counter with Separate Oscillator
  - Four PWM Channels
  - 8-channel, 10-bit ADC
    8 Single-ended Channels
    7 Differential Channels in TQFP Package Only
    2 Differential Channels with Programmable Gain at 1x, 10x, or 200x
  - Byte-oriented Two-wire Serial Interface
  - Programmable Serial USART
  - Master/Slave SPI Serial Interface
  - Programmable Watchdog Timer with Separate On-chip Oscillator
  - On-chip Analog Comparator
- Special Microcontroller Features
  - Power-on Reset and Programmable Brown-out Detection
  - Internal Calibrated RC Oscillator
  - External and Internal Interrupt Sources
  - Six Sleep Modes: Idle, ADC Noise Reduction, Power-save, Power-down, Standby and Extended Standby
- I/O and Packages
  - 32 Programmable I/O Lines
  - 40-pin PDIP, 44-lead TQFP, and 44-pad QFN/MLF
- Operating Voltages
  - 2.7V - 5.5V for ATmega16L
  - 4.5V - 5.5V for ATmega16
- Speed Grades
  - 0 - 8 MHz for ATmega16L
  - 0 - 16 MHz for ATmega16
- Power Consumption @ 1 MHz, 3V, and 25°C for ATmega16L
  - Active: 1.1 mA
  - Idle Mode: 0.35 mA
  - Power-down Mode: < 1 µA

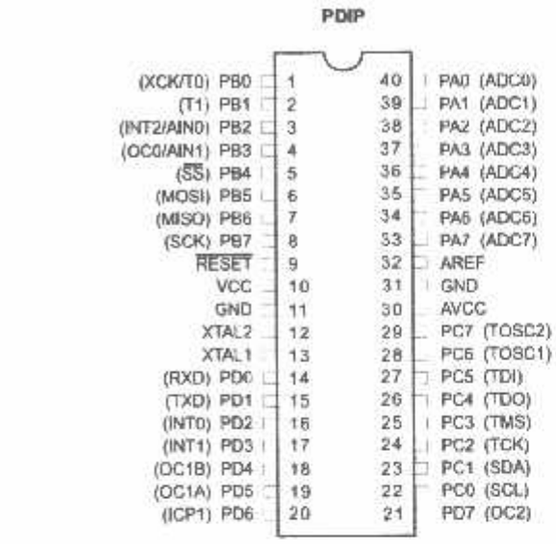
8-bit AVR® Microcontroller with 16K Bytes In-System Programmable Flash

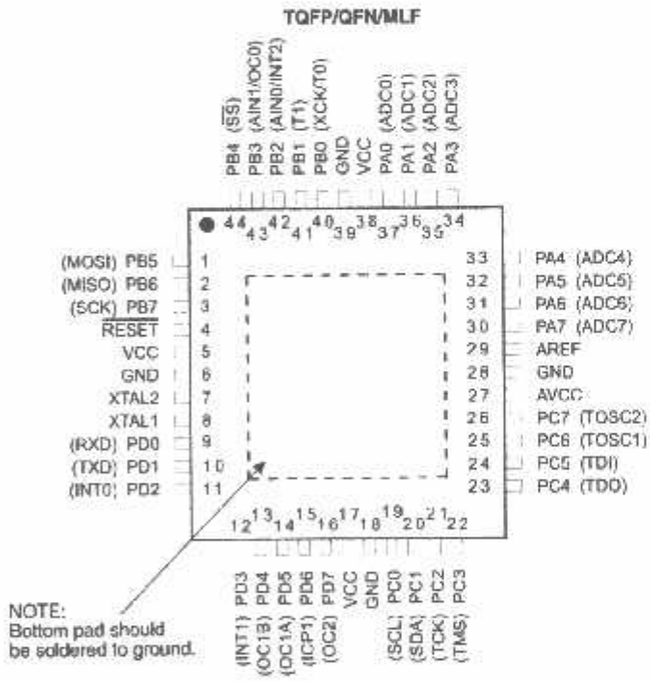
ATmega16
ATmega16L

Rev. 2466T–AVR–07/10

Pin Configurations

Figure 1. Pinout ATmega16





Disclaimer

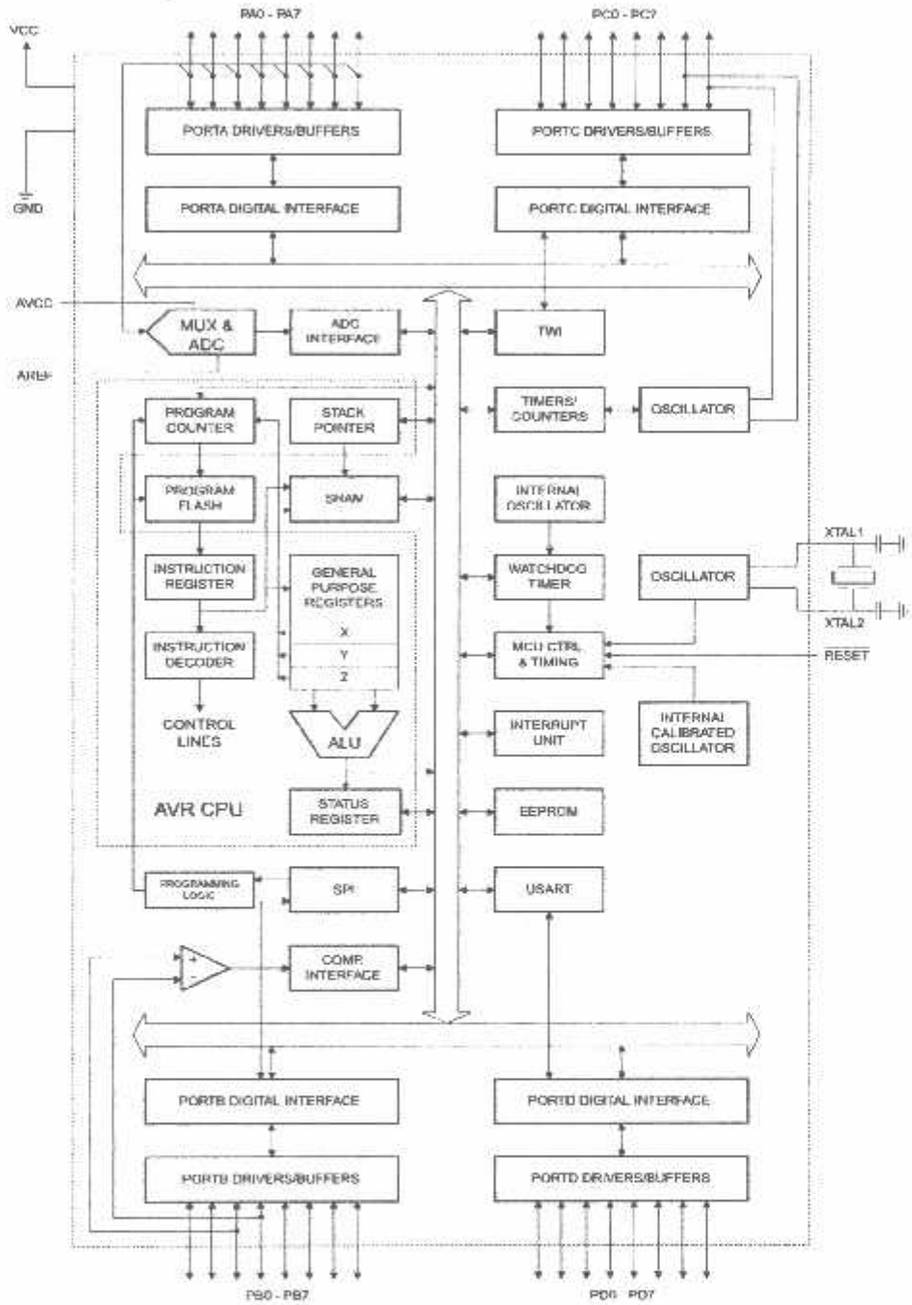
Typical values contained in this datasheet are based on simulations and characterization of other AVR microcontrollers manufactured on the same process technology. Min and Max values will be available after the device is characterized.

Overview

The ATmega16 is a low-power CMOS 8-bit microcontroller based on the AVR enhanced RISC architecture. By executing powerful instructions in a single clock cycle, the ATmega16 achieves throughputs approaching 1 MIPS per MHz allowing the system designer to optimize power consumption versus processing speed.

Block Diagram

Figure 2. Block Diagram



The AVR core combines a rich instruction set with 32 general purpose working registers. All the 32 registers are directly connected to the Arithmetic Logic Unit (ALU), allowing two independent registers to be accessed in one single instruction executed in one clock cycle. The resulting architecture is more code efficient while achieving throughputs up to ten times faster than conventional CISC microcontrollers.

The ATmega16 provides the following features: 16 Kbytes of In-System Programmable Flash Program memory with Read-While-Write capabilities, 512 bytes EEPROM, 1 Kbyte SRAM, 32 general purpose I/O lines, 32 general purpose working registers, a JTAG interface for Boundary-scan, On-chip Debugging support and programming, three flexible Timer/Counters with compare modes, Internal and External Interrupts, a serial programmable USART, a byte oriented Two-wire Serial Interface, an 8-channel, 10-bit ADC with optional differential input stage with programmable gain (TQFP package only), a programmable Watchdog Timer with Internal Oscillator, an SPI serial port, and six software selectable power saving modes. The Idle mode stops the CPU while allowing the USART, Two-wire interface, A/D Converter, SRAM, Timer/Counters, SPI port, and interrupt system to continue functioning. The Power-down mode saves the register contents but freezes the Oscillator, disabling all other chip functions until the next External Interrupt or Hardware Reset. In Power-save mode, the Asynchronous Timer continues to run, allowing the user to maintain a timer base while the rest of the device is sleeping. The ADC Noise Reduction mode stops the CPU and all I/O modules except Asynchronous Timer and ADC, to minimize switching noise during ADC conversions. In Standby mode, the crystal/resonator Oscillator is running while the rest of the device is sleeping. This allows very fast start-up combined with low-power consumption. In Extended Standby mode, both the main Oscillator and the Asynchronous Timer continue to run.

The device is manufactured using Atmel's high density nonvolatile memory technology. The On-chip ISP Flash allows the program memory to be reprogrammed in-system through an SPI serial interface, by a conventional nonvolatile memory programmer, or by an On-chip Boot program running on the AVR core. The boot program can use any interface to download the application program in the Application Flash memory. Software in the Boot Flash section will continue to run while the Application Flash section is updated, providing true Read-While-Write operation. By combining an 8-bit RISC CPU with In-System Self-Programmable Flash on a monolithic chip, the Atmel ATmega16 is a powerful microcontroller that provides a highly-flexible and cost-effective solution to many embedded control applications.

The ATmega16 AVR is supported with a full suite of program and system development tools including: C compilers, macro assemblers, program debugger/simulators, in-circuit emulators, and evaluation kits.

Pin Descriptions

VCC

Digital supply voltage.

GND

Ground.

Port A (PA7..PA0)

Port A serves as the analog inputs to the A/D Converter.

Port A also serves as an 8-bit bi-directional I/O port, if the A/D Converter is not used. Port pins can provide internal pull-up resistors (selected for each bit). The Port A output buffers have symmetrical drive characteristics with both high sink and source capability. When pins PA0 to PA7 are used as inputs and are externally pulled low, they will source current if the internal pull-up resistors are activated. The Port A pins are tri-stated when a reset condition becomes active, even if the clock is not running.

Port B (PB7..PB0)

Port B is an 8-bit bi-directional I/O port with internal pull-up resistors (selected for each bit). The Port B output buffers have symmetrical drive characteristics with both high sink and source capability. As inputs, Port B pins that are externally pulled low will source current if the pull-up resistors are activated. The Port B pins are tri-stated when a reset condition becomes active, even if the clock is not running.

Port B also serves the functions of various special features of the ATmega16 as listed on page 58.

Port C (PC7..PC0)

Port C is an 8-bit bi-directional I/O port with internal pull-up resistors (selected for each bit). The Port C output buffers have symmetrical drive characteristics with both high sink and source capability. As inputs, Port C pins that are externally pulled low will source current if the pull-up resistors are activated. The Port C pins are tri-stated when a reset condition becomes active, even if the clock is not running. If the JTAG interface is enabled, the pull-up resistors on pins PC5(TDI), PC3(TMS) and PC2(TCK) will be activated even if a reset occurs.

Port C also serves the functions of the JTAG interface and other special features of the ATmega16 as listed on page 61.

Port D (PD7..PD0)

Port D is an 8-bit bi-directional I/O port with internal pull-up resistors (selected for each bit). The Port D output buffers have symmetrical drive characteristics with both high sink and source capability. As inputs, Port D pins that are externally pulled low will source current if the pull-up resistors are activated. The Port D pins are tri-stated when a reset condition becomes active, even if the clock is not running.

Port D also serves the functions of various special features of the ATmega16 as listed on page 63.

$\overline{\text{RESET}}$

Reset Input. A low level on this pin for longer than the minimum pulse length will generate a reset, even if the clock is not running. The minimum pulse length is given in Table 15 on page 38. Shorter pulses are not guaranteed to generate a reset.

XTAL1

Input to the inverting Oscillator amplifier and input to the internal clock operating circuit.

XTAL2

Output from the inverting Oscillator amplifier.

AVCC

AVCC is the supply voltage pin for Port A and the A/D Converter. It should be externally connected to V_{CC}, even if the ADC is not used. If the ADC is used, it should be connected to V_{CC} through a low-pass filter.

AREF

AREF is the analog reference pin for the A/D Converter.

Resources

A comprehensive set of development tools, application notes and datasheets are available for download on http://www.atmel.com/avr.

Data Retention

Reliability Qualification results show that the projected data retention failure rate is much less than 1 PPM over 20 years at 85°C or 100 years at 25°C.

About Code Examples

This documentation contains simple code examples that briefly show how to use various parts of the device. These code examples assume that the part specific header file is included before compilation. Be aware that not all C Compiler vendors include bit definitions in the header files and interrupt handling in C is compiler dependent. Please confirm with the C Compiler documentation for more details.

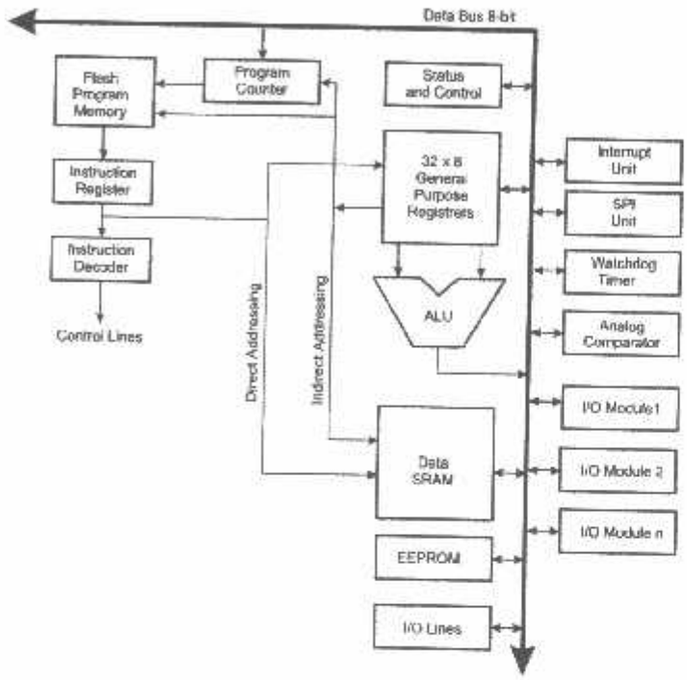
AVR CPU Core

Introduction

This section discusses the AVR core architecture in general. The main function of the CPU core is to ensure correct program execution. The CPU must therefore be able to access memories, perform calculations, control peripherals, and handle interrupts.

Architectural Overview

Figure 3. Block Diagram of the AVR MCU Architecture



In order to maximize performance and parallelism, the AVR uses a Harvard architecture – with separate memories and buses for program and data. Instructions in the program memory are executed with a single level pipelining. While one instruction is being executed, the next instruction is pre-fetched from the program memory. This concept enables instructions to be executed in every clock cycle. The program memory is In-System Reprogrammable Flash memory.

The fast-access Register File contains 32 × 8-bit general purpose working registers with a single clock cycle access time. This allows single-cycle Arithmetic Logic Unit (ALU) operation. In a typical ALU operation, two operands are output from the Register File, the operation is executed, and the result is stored back in the Register File – in one clock cycle.

Six of the 32 registers can be used as three 16-bit indirect address register pointers for Data Space addressing – enabling efficient address calculations. One of the these address pointers can also be used as an address pointer for look up tables in Flash Program memory. These added function registers are the 16-bit X-register, Y-register, and Z-register, described later in this section.

The ALU supports arithmetic and logic operations between registers or between a constant and a register. Single register operations can also be executed in the ALU. After an arithmetic operation, the Status Register is updated to reflect information about the result of the operation.

Program flow is provided by conditional and unconditional jump and call instructions, able to directly address the whole address space. Most AVR instructions have a single 16-bit word format. Every program memory address contains a 16-bit or 32-bit instruction.

Program Flash memory space is divided in two sections, the Boot program section and the Application Program section. Both sections have dedicated Lock bits for write and read/write protection. The SPM instruction that writes into the Application Flash memory section must reside in the Boot Program section.

During interrupts and subroutine calls, the return address Program Counter (PC) is stored on the Stack. The Stack is effectively allocated in the general data SRAM, and consequently the Stack size is only limited by the total SRAM size and the usage of the SRAM. All user programs must initialize the SP in the reset routine (before subroutines or interrupts are executed). The Stack Pointer SP is read/write accessible in the I/O space. The data SRAM can easily be accessed through the five different addressing modes supported in the AVR architecture.

The memory spaces in the AVR architecture are all linear and regular memory maps.

A flexible interrupt module has its control registers in the I/O space with an additional global interrupt enable bit in the Status Register. All interrupts have a separate interrupt vector in the interrupt vector table. The interrupts have priority in accordance with their interrupt vector position. The lower the interrupt vector address, the higher the priority.

The I/O memory space contains 64 addresses for CPU peripheral functions as Control Registers, SPI, and other I/O functions. The I/O Memory can be accessed directly, or as the Data Space locations following those of the Register File, $20 - $5F.

ALU – Arithmetic Logic Unit

The high-performance AVR ALU operates in direct connection with all the 32 general purpose working registers. Within a single clock cycle, arithmetic operations between general purpose registers or between a register and an immediate are executed. The ALU operations are divided into three main categories – arithmetic, logical, and bit-functions. Some implementations of the architecture also provide a powerful multiplier supporting both signed/unsigned multiplication and fractional format. See the "Instruction Set" section for a detailed description.

Status Register

The Status Register contains information about the result of the most recently executed arithmetic instruction. This information can be used for altering program flow in order to perform conditional operations. Note that the Status Register is updated after all ALU operations, as specified in the Instruction Set Reference. This will in many cases remove the need for using the dedicated compare instructions, resulting in faster and more compact code.

The Status Register is not automatically stored when entering an interrupt routine and restored when returning from an interrupt. This must be handled by software.

The AVR Status Register – SREG – is defined as:

Bit	7	6	5	4	3	2	1	0	
	I	T	H	S	V	N	Z	C	SREG
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	
Initial Value	0	0	0	0	0	0	0	0	

- **Bit 7 – I: Global Interrupt Enable**

The Global Interrupt Enable bit must be set for the interrupts to be enabled. The individual interrupt enable control is then performed in separate control registers. If the Global Interrupt Enable Register is cleared, none of the interrupts are enabled independent of the individual interrupt enable settings. The I-bit is cleared by hardware after an interrupt has occurred, and is set by the RETI instruction to enable subsequent interrupts. The I-bit can also be set and cleared by the application with the SEI and CLI instructions, as described in the instruction set reference.

- **Bit 6 – T: Bit Copy Storage**

The Bit Copy instructions BLD (Bit LoaD) and BST (Bit STore) use the T-bit as source or destination for the operated bit. A bit from a register in the Register File can be copied into T by the BST instruction, and a bit in T can be copied into a bit in a register in the Register File by the BLD instruction.

- **Bit 5 – H: Half Carry Flag**

The Half Carry Flag H indicates a Half Carry in some arithmetic operations. Half Carry is useful in BCD arithmetic. See the "Instruction Set Description" for detailed information.

- **Bit 4 – S: Sign Bit, S = N ⊕ V**

The S-bit is always an exclusive or between the Negative Flag N and the Two's Complement Overflow Flag V. See the "Instruction Set Description" for detailed information.

- **Bit 3 – V: Two's Complement Overflow Flag**

The Two's Complement Overflow Flag V supports two's complement arithmetics. See the "Instruction Set Description" for detailed information.

- **Bit 2 – N: Negative Flag**

The Negative Flag N indicates a negative result in an arithmetic or logic operation. See the "Instruction Set Description" for detailed information.

- **Bit 1 – Z: Zero Flag**

The Zero Flag Z indicates a zero result in an arithmetic or logic operation. See the "Instruction Set Description" for detailed information.

- **Bit 0 – C: Carry Flag**

The Carry Flag C indicates a carry in an arithmetic or logic operation. See the "Instruction Set Description" for detailed information.

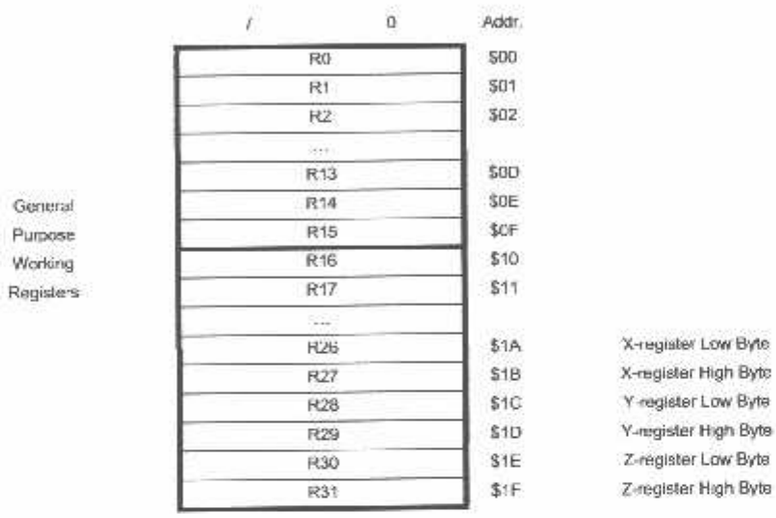
General Purpose Register File

The Register File is optimized for the AVR Enhanced RISC instruction set. In order to achieve the required performance and flexibility, the following input/output schemes are supported by the Register File:

- One 8-bit output operand and one 8-bit result input
- Two 8-bit output operands and one 8-bit result input
- Two 8-bit output operands and one 16-bit result input
- One 16-bit output operand and one 16-bit result input

Figure 4 shows the structure of the 32 general purpose working registers in the CPU.

Figure 4. AVR CPU General Purpose Working Registers



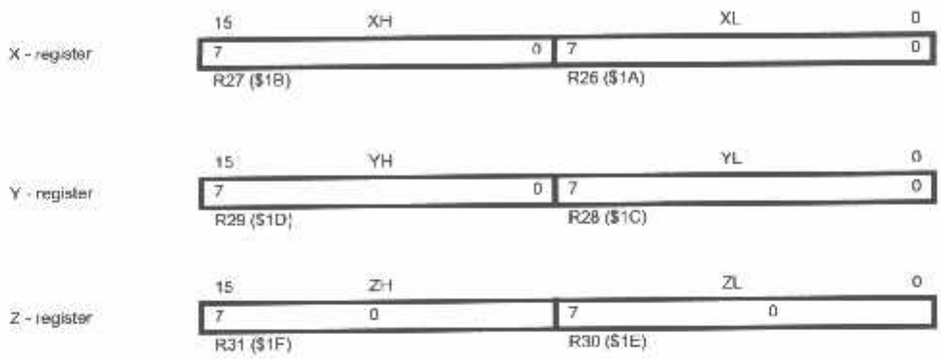
Most of the instructions operating on the Register File have direct access to all registers, and most of them are single cycle instructions.

As shown in Figure 4, each register is also assigned a data memory address, mapping them directly into the first 32 locations of the user Data Space. Although not being physically implemented as SRAM locations, this memory organization provides great flexibility in access of the registers, as the X-, Y-, and Z-pointer Registers can be set to index any register in the file.

The X-register, Y-register and Z-register

The registers R26..R31 have some added functions to their general purpose usage. These registers are 16-bit address pointers for indirect addressing of the Data Space. The three indirect address registers X, Y, and Z are defined as described in Figure 5.

Figure 5. The X-register, Y-register, and Z-register



In the different addressing modes these address registers have functions as fixed displacement, automatic increment, and automatic decrement (see the Instruction Set Reference for details).

Stack Pointer

The Stack is mainly used for storing temporary data, for storing local variables and for storing return addresses after interrupts and subroutine calls. The Stack Pointer Register always points to the top of the Stack. Note that the Stack is implemented as growing from higher memory locations to lower memory locations. This implies that a Stack PUSH command decreases the Stack Pointer. If software reads the Program Counter from the Stack after a call or an interrupt, unused bits (15:13) should be masked out.

The Stack Pointer points to the data SRAM Stack area where the Subroutine and Interrupt Stacks are located. This Stack space in the data SRAM must be defined by the program before any subroutine calls are executed or interrupts are enabled. The Stack Pointer must be set to point above $60. The Stack Pointer is decremented by one when data is pushed onto the Stack with the PUSH instruction, and it is decremented by two when the return address is pushed onto the Stack with subroutine call or interrupt. The Stack Pointer is incremented by one when data is popped from the Stack with the POP instruction, and it is incremented by two when data is popped from the Stack with return from subroutine RET or return from interrupt RETI.

The AVR Stack Pointer is implemented as two 8-bit registers in the I/O space. The number of bits actually used is implementation dependent. Note that the data space in some implementations of the AVR architecture is so small that only SPL is needed. In this case, the SPH Register will not be present.

Bit	15	14	13	12	11	10	9	8	
	SP15	SP14	SP13	SP12	SP11	SP10	SP9	SP8	SPH
	SP7	SP6	SP5	SP4	SP3	SP2	SP1	SP0	SPL
	7	6	5	4	3	2	1	0	
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	
	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	
Initial Value	0	0	0	0	0	0	0	0	
	0	0	0	0	0	0	0	0	

Instruction Execution Timing

This section describes the general access timing concepts for instruction execution. The AVR CPU is driven by the CPU clock clk_{CPU}, directly generated from the selected clock source for the chip. No internal clock division is used.

Figure 6 shows the parallel instruction fetches and instruction executions enabled by the Harvard architecture and the fast-access Register File concept. This is the basic pipelining concept to obtain up to 1 MIPS per MHz with the corresponding unique results for functions per cost, functions per clocks, and functions per power-unit.

Figure 6. The Parallel Instruction Fetches and Instruction Executions

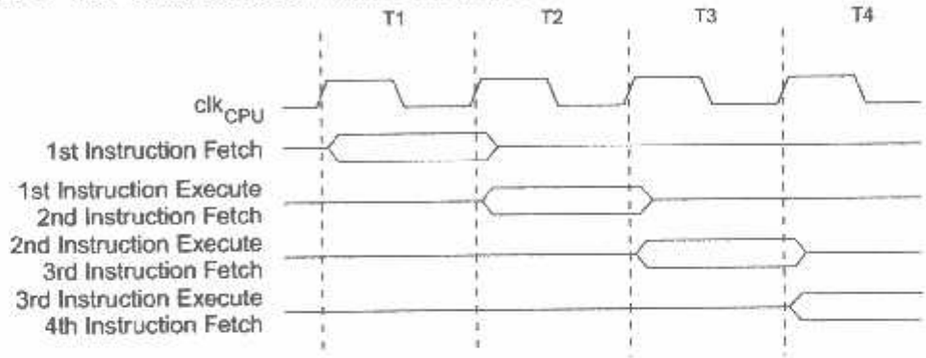
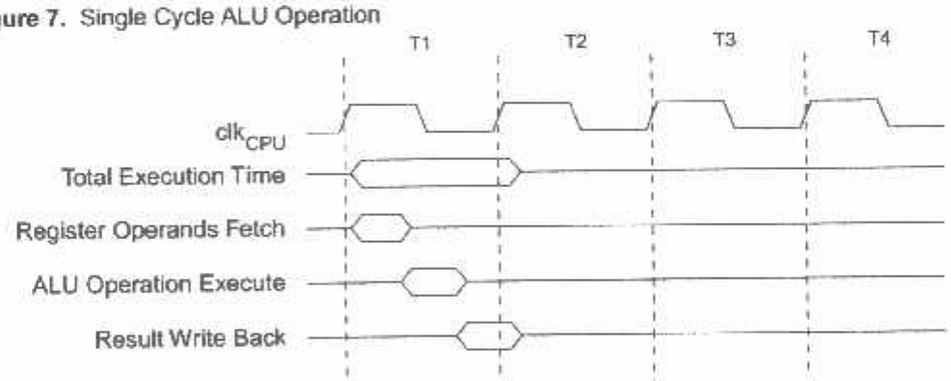


Figure 7 shows the internal timing concept for the Register File. In a single clock cycle an ALU operation using two register operands is executed, and the result is stored back to the destination register.

Figure 7. Single Cycle ALU Operation



Reset and Interrupt Handling

The AVR provides several different interrupt sources. These interrupts and the separate reset vector each have a separate program vector in the program memory space. All interrupts are assigned individual enable bits which must be written logic one together with the Global Interrupt Enable bit in the Status Register in order to enable the interrupt. Depending on the Program Counter value, interrupts may be automatically disabled when Boot Lock bits BLB02 or BLB12 are programmed. This feature improves software security. See the section "Memory Programming" on page 259 for details.

The lowest addresses in the program memory space are by default defined as the Reset and Interrupt Vectors. The complete list of vectors is shown in "Interrupts" on page 45. The list also determines the priority levels of the different interrupts. The lower the address the higher is the priority level. RESET has the highest priority, and next is INT0 – the External Interrupt Request

0. The Interrupt Vectors can be moved to the start of the Boot Flash section by setting the IVSEL bit in the General Interrupt Control Register (GICR). Refer to "Interrupts" on page 45 for more information. The Reset Vector can also be moved to the start of the boot Flash section by programming the BOOTRST Fuse, see "Boot Loader Support – Read-While-Write Self-Programming" on page 246.

When an interrupt occurs, the Global Interrupt Enable I-bit is cleared and all interrupts are disabled. The user software can write logic one to the I-bit to enable nested interrupts. All enabled interrupts can then interrupt the current interrupt routine. The I-bit is automatically set when a Return from Interrupt instruction – RETI – is executed.

There are basically two types of interrupts. The first type is triggered by an event that sets the Interrupt Flag. For these interrupts, the Program Counter is vectored to the actual Interrupt Vector in order to execute the interrupt handling routine, and hardware clears the corresponding Interrupt Flag. Interrupt Flags can also be cleared by writing a logic one to the flag bit position(s) to be cleared. If an interrupt condition occurs while the corresponding interrupt enable bit is cleared, the Interrupt Flag will be set and remembered until the interrupt is enabled, or the flag is cleared by software. Similarly, if one or more interrupt conditions occur while the Global Interrupt Enable bit is cleared, the corresponding Interrupt Flag(s) will be set and remembered until the global interrupt enable bit is set, and will then be executed by order of priority.

The second type of interrupts will trigger as long as the interrupt condition is present. These interrupts do not necessarily have Interrupt Flags. If the interrupt condition disappears before the interrupt is enabled, the interrupt will not be triggered.

When the AVR exits from an interrupt, it will always return to the main program and execute one more instruction before any pending interrupt is served.

Note that the Status Register is not automatically stored when entering an interrupt routine, nor restored when returning from an interrupt routine. This must be handled by software.

When using the CLI instruction to disable interrupts, the interrupts will be immediately disabled. No interrupt will be executed after the CLI instruction, even if it occurs simultaneously with the CLI instruction. The following example shows how this can be used to avoid interrupts during the timed EEPROM write sequence.

Assembly Code Example

```
in  r16, SREG       ; store SREG value
cli     ; disable interrupts during timed sequence
sbi EECR, EEMWE     ; start EEPROM write
sbi EECR, EEWE
out SREG, r16       ; restore SREG value (I-bit)
```

C Code Example

```
char cSREG;
cSREG = SREG;  /* store SREG value */
/* disable interrupts during timed sequence */
_CLI();
EECR |= (1<<EEMWE); /* start EEPROM write */
EECR |= (1<<EEWE);
SREG = cSREG; /* restore SREG value (I-bit) */
```

When using the SEI instruction to enable interrupts, the instruction following SEI will be executed before any pending interrupts, as shown in this example.

Assembly Code Example

```
sei   ; set global interrupt enable
sleep ; enter sleep, waiting for interrupt
; note: will enter sleep before any pending
; interrupt(s)
```

C Code Example

```
_SEI(); /* set global interrupt enable */
_SLEEP(); /* enter sleep, waiting for interrupt */
/* note: will enter sleep before any pending interrupt(s) */
```

Interrupt Response Time

The interrupt execution response for all the enabled AVR interrupts is four clock cycles minimum. After four clock cycles the program vector address for the actual interrupt handling routine is executed. During this four clock cycle period, the Program Counter is pushed onto the Stack. The vector is normally a jump to the interrupt routine, and this jump takes three clock cycles. If an interrupt occurs during execution of a multi-cycle instruction, this instruction is completed before the interrupt is served. If an interrupt occurs when the MCU is in sleep mode, the interrupt execution response time is increased by four clock cycles. This increase comes in addition to the start-up time from the selected sleep mode.

A return from an interrupt handling routine takes four clock cycles. During these four clock cycles, the Program Counter (two bytes) is popped back from the Stack, the Stack Pointer is incremented by two, and the I-bit in SREG is set.

AVR ATmega16 Memories

This section describes the different memories in the ATmega16. The AVR architecture has two main memory spaces, the Data Memory and the Program Memory space. In addition, the ATmega16 features an EEPROM Memory for data storage. All three memory spaces are linear and regular.

In-System Reprogrammable Flash Program Memory

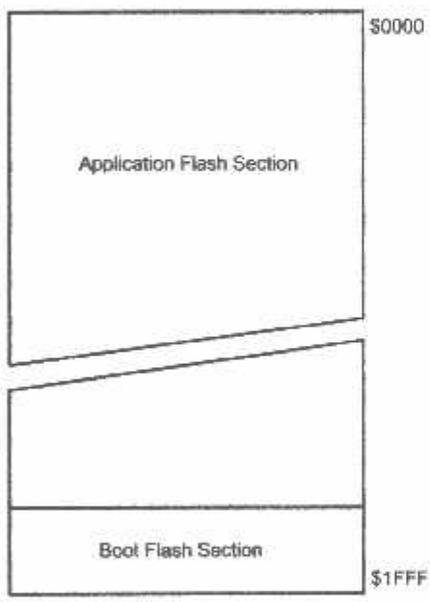
The ATmega16 contains 16 Kbytes On-chip In-System Reprogrammable Flash memory for program storage. Since all AVR instructions are 16 or 32 bits wide, the Flash is organized as 8K × 16. For software security, the Flash Program memory space is divided into two sections, Boot Program section and Application Program section.

The Flash memory has an endurance of at least 10,000 write/erase cycles. The ATmega16 Program Counter (PC) is 13 bits wide, thus addressing the 8K program memory locations. The operation of Boot Program section and associated Boot Lock bits for software protection are described in detail in "Boot Loader Support – Read-While-Write Self-Programming" on page 246. "Memory Programming" on page 259 contains a detailed description on Flash data serial downloading using the SPI pins or the JTAG interface.

Constant tables can be allocated within the entire program memory address space (see the LPM – Load Program Memory Instruction Description).

Timing diagrams for instruction fetch and execution are presented in "Instruction Execution Timing" on page 13.

Figure 8. Program Memory Map



SRAM Data Memory

Figure 9 shows how the ATmega16 SRAM Memory is organized.

The lower 1120 Data Memory locations address the Register File, the I/O Memory, and the internal data SRAM. The first 96 locations address the Register File and I/O Memory, and the next 1024 locations address the internal data SRAM.

The five different addressing modes for the data memory cover: Direct, Indirect with Displacement, Indirect, Indirect with Pre-decrement, and Indirect with Post-increment. In the Register File, registers R26 to R31 feature the indirect addressing pointer registers.

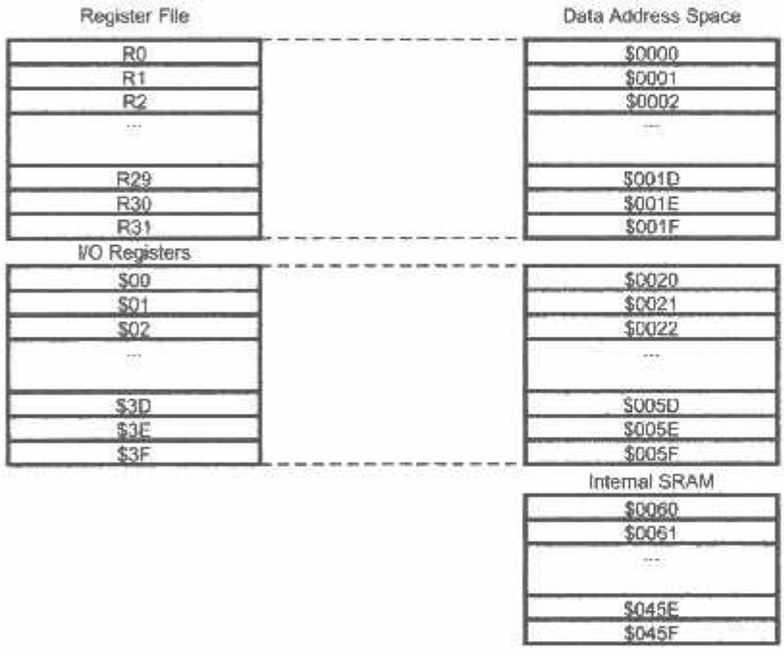
The direct addressing reaches the entire data space.

The Indirect with Displacement mode reaches 63 address locations from the base address given by the Y-register or Z-register.

When using register indirect addressing modes with automatic pre-decrement and post-increment, the address registers X, Y, and Z are decremented or incremented.

The 32 general purpose working registers, 64 I/O Registers, and the 1024 bytes of internal data SRAM in the ATmega16 are all accessible through all these addressing modes. The Register File is described in "General Purpose Register File" on page 11.

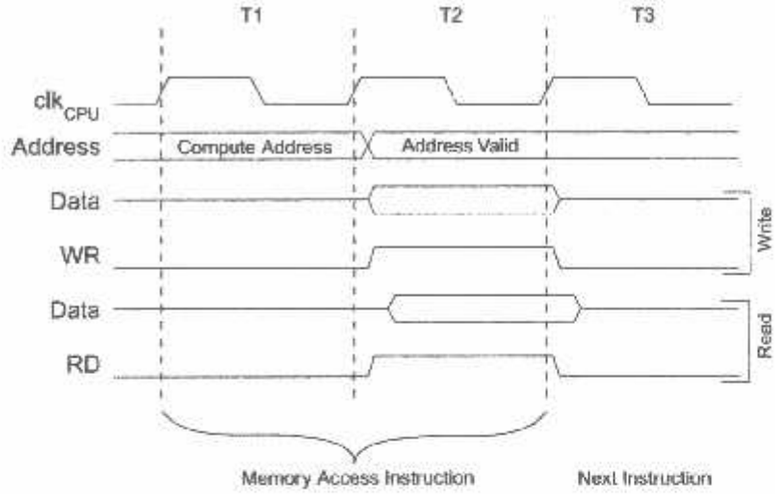
Figure 9. Data Memory Map



Data Memory Access Times

This section describes the general access timing concepts for internal memory access. The internal data SRAM access is performed in two clk_{CPU} cycles as described in Figure 10.

Figure 10. On-chip Data SRAM Access Cycles



EEPROM Data Memory

The ATmega16 contains 512 bytes of data EEPROM memory. It is organized as a separate data space, in which single bytes can be read and written. The EEPROM has an endurance of at least 100,000 write/erase cycles. The access between the EEPROM and the CPU is described in the following, specifying the EEPROM Address Registers, the EEPROM Data Register, and the EEPROM Control Register.

For a detailed description of SPI, JTAG, and Parallel data downloading to the EEPROM, see page 273, page 278, and page 262, respectively.

EEPROM Read/Write Access

The EEPROM Access Registers are accessible in the I/O space.

The write access time for the EEPROM is given in Table 1. A self-timing function, however, lets the user software detect when the next byte can be written. If the user code contains instructions that write the EEPROM, some precautions must be taken. In heavily filtered power supplies, V_{CC} is likely to rise or fall slowly on Power-up/down. This causes the device for some period of time to run at a voltage lower than specified as minimum for the clock frequency used. See "Preventing EEPROM Corruption" on page 22 for details on how to avoid problems in these situations.

In order to prevent unintentional EEPROM writes, a specific write procedure must be followed. Refer to the description of the EEPROM Control Register for details on this.

When the EEPROM is read, the CPU is halted for four clock cycles before the next instruction is executed. When the EEPROM is written, the CPU is halted for two clock cycles before the next instruction is executed.

The EEPROM Address Register – EEARH and EEARL

Bit	15	14	13	12	11	10	9	8	
	–	–	–	–	–	–	–	EEAR8	EEARH
	EEAR7	EEAR6	EEAR5	EEAR4	EEAR3	EEAR2	EEAR1	EEAR0	EEARL
	7	6	5	4	3	2	1	0	
Read/Write	R	R	R	R	R	R	R	R/W	
	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	
Initial Value	0	0	0	0	0	0	0	X	
	X	X	X	X	X	X	X	X	

- **Bits 15..9 – Res: Reserved Bits**

These bits are reserved bits in the ATmega16 and will always read as zero.

- **Bits 8..0 – EEAR8..0: EEPROM Address**

The EEPROM Address Registers – EEARH and EEARL – specify the EEPROM address in the 512 bytes EEPROM space. The EEPROM data bytes are addressed linearly between 0 and 511. The initial value of EEAR is undefined. A proper value must be written before the EEPROM may be accessed.

The EEPROM Data Register – EEDR

Bit	7	6	5	4	3	2	1	0	
	MSB							LSB	EEDR
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	
Initial Value	0	0	0	0	0	0	0	0	

- **Bits 7..0 – EEDR7.0: EEPROM Data**

For the EEPROM write operation, the EEDR Register contains the data to be written to the EEPROM in the address given by the EEAR Register. For the EEPROM read operation, the EEDR contains the data read out from the EEPROM at the address given by EEAR.

The EEPROM Control Register – EECR

Bit	7	6	5	4	3	2	1	0	
	–	–	–	–	EERIE	EEMWE	EEWE	EERE	EECR
Read/Write	R	R	R	R	R/W	R/W	R/W	R/W	
Initial Value	0	0	0	0	0	0	X	0	

- **Bits 7..4 – Res: Reserved Bits**

These bits are reserved bits in the ATmega16 and will always read as zero.

- **Bit 3 – EERIE: EEPROM Ready Interrupt Enable**

Writing EERIE to one enables the EEPROM Ready Interrupt if the I bit in SREG is set. Writing EERIE to zero disables the interrupt. The EEPROM Ready interrupt generates a constant interrupt when EEWE is cleared.

- **Bit 2 – EEMWE: EEPROM Master Write Enable**

The EEMWE bit determines whether setting EEWE to one causes the EEPROM to be written. When EEMWE is set, setting EEWE within four clock cycles will write data to the EEPROM at the selected address If EEMWE is zero, setting EEWE will have no effect. When EEMWE has been written to one by software, hardware clears the bit to zero after four clock cycles. See the description of the EEWE bit for an EEPROM write procedure.

- **Bit 1 – EEWE: EEPROM Write Enable**

The EEPROM Write Enable Signal EEWE is the write strobe to the EEPROM. When address and data are correctly set up, the EEWE bit must be written to one to write the value into the EEPROM. The EEMWE bit must be written to one before a logical one is written to EEWE, otherwise no EEPROM write takes place. The following procedure should be followed when writing the EEPROM (the order of steps 3 and 4 is not essential):

1. Wait until EEWE becomes zero.
2. Wait until SPMEN in SPMCR becomes zero.
3. Write new EEPROM address to EEAR (optional).
4. Write new EEPROM data to EEDR (optional).
5. Write a logical one to the EEMWE bit while writing a zero to EEWE in EECR.
6. Within four clock cycles after setting EEMWE, write a logical one to EEWE.

The EEPROM can not be programmed during a CPU write to the Flash memory. The software must check that the Flash programming is completed before initiating a new EEPROM write. Step 2 is only relevant if the software contains a Boot Loader allowing the CPU to program the Flash. If the Flash is never being updated by the CPU, step 2 can be omitted. See "Boot Loader Support – Read-While-Write Self-Programming" on page 246 for details about boot programming.

Caution: An interrupt between step 5 and step 6 will make the write cycle fail, since the EEPROM Master Write Enable will time-out. If an interrupt routine accessing the EEPROM is interrupting another EEPROM Access, the EEAR or EEDR reGister will be modified, causing the interrupted EEPROM Access to fail. It is recommended to have the Global Interrupt Flag cleared during all the steps to avoid these problems.

When the write access time has elapsed, the EEWE bit is cleared by hardware. The user software can poll this bit and wait for a zero before writing the next byte. When EEWE has been set, the CPU is halted for two cycles before the next instruction is executed.

- **Bit 0 – EERE: EEPROM Read Enable**

The EEPROM Read Enable Signal – EERE – is the read strobe to the EEPROM. When the correct address is set up in the EEAR Register, the EERE bit must be written to a logic one to trigger the EEPROM read. The EEPROM read access takes one instruction, and the requested data is available immediately. When the EEPROM is read, the CPU is halted for four cycles before the next instruction is executed.

The user should poll the EEWE bit before starting the read operation. If a write operation is in progress, it is neither possible to read the EEPROM, nor to change the EEAR Register.

The calibrated Oscillator is used to time the EEPROM accesses. Table 1 lists the typical programming time for EEPROM access from the CPU.

Table 1. EEPROM Programming Time

Symbol	Number of Calibrated RC Oscillator Cycles[1]	Typ Programming Time
EEPROM write (from CPU)	8448	8.5 ms

Note: 1. Uses 1 MHz clock, independent of CKSEL Fuse setting.

The following code examples show one assembly and one C function for writing to the EEPROM. The examples assume that interrupts are controlled (for example by disabling interrupts globally) so that no interrupts will occur during execution of these functions. The examples

ChipCorder®
TECHNOLOGY BY ISD

ISD2560/75/90/120 Products

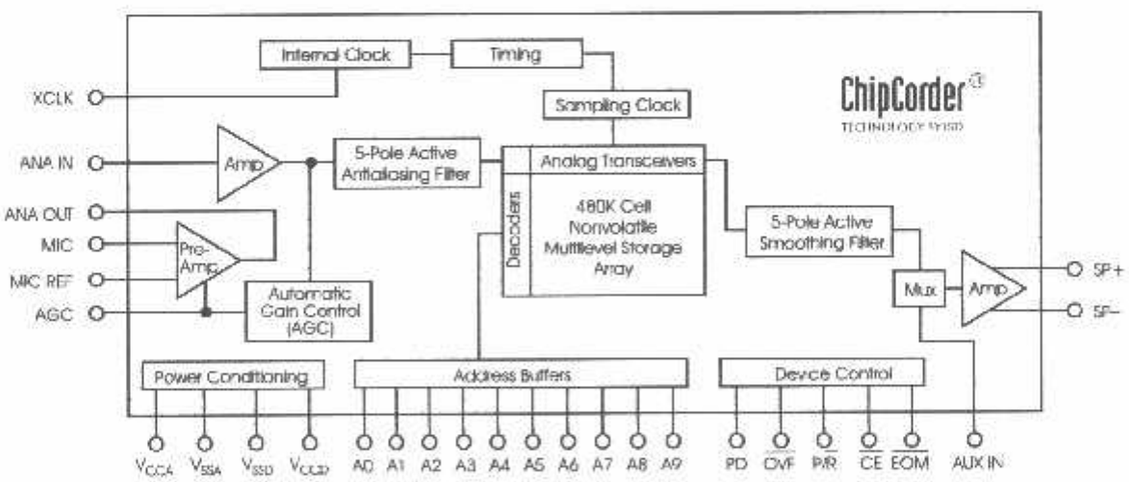
Single-Chip Voice Record/Playback Devices 60-, 75-, 90-, and 120-Second Durations

GENERAL DESCRIPTION

Information Storage Devices' ISD2500 ChipCorder® Series provides high-quality, single-chip record/playback solutions for 60- to 120-second messaging applications. The CMOS devices include an on-chip oscillator, microphone preamplifier, automatic gain control, antialiasing filter, smoothing filter, speaker amplifier, and high density multilevel storage array. In addition, the ISD2500 is microcontroller compatible, allowing complex messaging and addressing to be achieved.

Recordings are stored in on-chip nonvolatile memory cells, providing zero-power message storage. This unique, single-chip solution is made possible through ISD's patented multilevel storage technology. Voice and audio signals are stored directly into memory in their natural form, providing high-quality, solid-state voice reproduction.

Figure i: ISD2560/75/90/120 Device Block Diagram



FEATURES

- Easy-to-use single-chip voice record/ playback solution
- High-quality, natural voice/audio reproduction
- Manual switch or microcontroller compatible playback can be edge- or level-activated
- Single-chip durations of 60, 75, 90, and 120 seconds
- Directly cascadable for longer durations
- Automatic Power-Down (Push-Button Mode)
  - Standby current 1 µA (typical)
- Zero-power message storage
  - Eliminates battery backup circuits
- Fully addressable to handle multiple messages
- 100-year message retention (typical)
- 100,000 record cycles (typical)
- On-chip clock source
- Programmer support for play-only applications
- Single +5 volt power supply
- Available in die form, DIP, SOIC, and TSOP packaging

Table i: ISD2560/75/90/120 Product Summary

Part Number	Duration (Seconds)	Input Sample Rate (KHz)	Typical Filter Pass Band (KHz)
ISD2560	60	8.0	3.4
ISD2575	75	6.4	2.7
ISD2590	90	5.3	2.3
ISD25120	120	4.0	1.7

DETAILED DESCRIPTION

SPEECH/SOUND QUALITY

The ISD2500 series includes devices offered at 4.0, 5.3, 6.4, and 8.0 KHz sampling frequencies, allowing the user a choice of speech quality options. Increasing the duration within a product series decreases the sampling frequency and bandwidth, which affects sound quality. Please refer to the ISD2560/75/90/120 Product Summary table on page *ii* to compare filter pass band and product durations.

The speech samples are stored directly into on-chip nonvolatile memory without the digitization and compression associated with other solutions. Direct analog storage provides a very true, natural sounding reproduction of voice, music, tones, and sound effects not available with most solid-state digital solutions.

DURATION

To meet end system requirements, the ISD2500 series offers single-chip solutions at 60, 75, 90, and 120 seconds. Parts may also be cascaded together for longer durations.

EEPROM STORAGE

One of the benefits of ISD's ChipCorder technology is the use of on-chip nonvolatile memory, providing zero-power message storage. The message is retained for up to 100 years typically without power. In addition, the device can be re-recorded typically over 100,000 times.

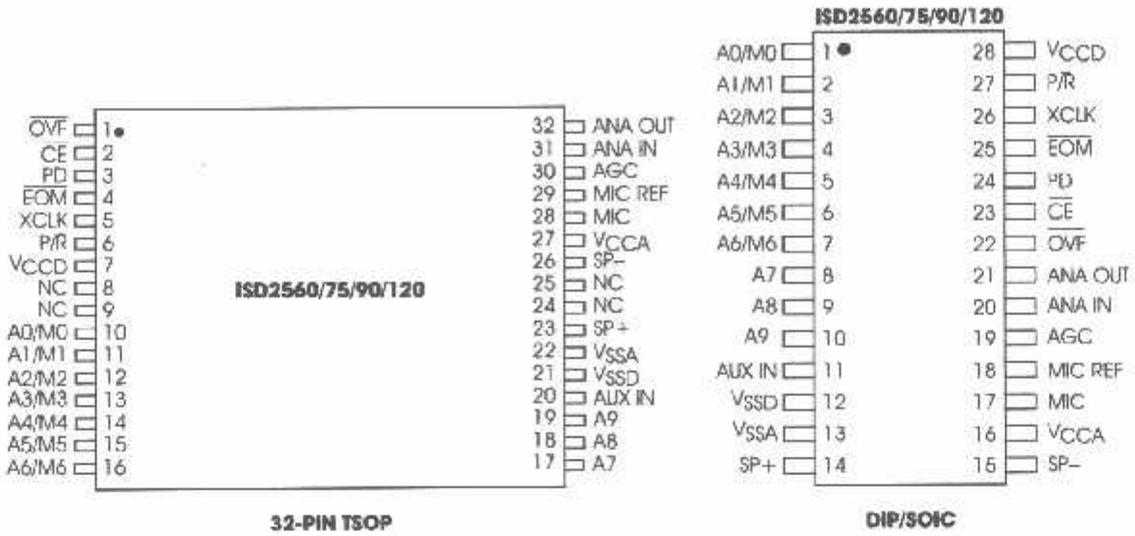
MICROCONTROLLER INTERFACE

In addition to its simplicity and ease of use, the ISD2500 series includes all the interfaces necessary for microcontroller-driven applications. The address and control lines can be interfaced to a microcontroller and manipulated to perform a variety of tasks, including message assembly, message concatenation, predefined fixed message segmentation, and message management.

PROGRAMMING

The ISD2500 series is also ideal for playback-only applications, where single or multiple messages are referenced through buttons, switches, or a microcontroller. Once the desired message configuration is created, duplicates can easily be generated via an ISD programmer.

Figure 1: ISD2560/75/90/120 Device Pinouts



PIN DESCRIPTIONS

VOLTAGE INPUTS (V_{CCA}, V_{CCD})

To minimize noise, the analog and digital circuits in the ISD2500 series devices use separate power busses. These voltage busses are brought out to separate pins and should be tied together as close to the supply as possible. In addition, these supplies should be decoupled as close to the package as possible.

GROUND INPUTS (V_{SSA}, V_{SSD})

The ISD2500 series of devices utilizes separate analog and digital ground busses. These pins should be connected separately through a low-impedance path to power supply ground.

POWER DOWN INPUT (PD)

When not recording or playing back, the PD pin should be pulled HIGH to place the part in a very low power mode (see I_{SB} specification). When overflow ($\overline{OVF}$) pulses LOW for an overflow condition, PD should be brought HIGH to reset the address pointer back to the beginning of the record/playback space. The PD pin has additional functionality in the M6 (Push-Button) Operational Mode described later in the Operational Mode section.

CHIP ENABLE INPUT ($\overline{CE}$)

The $\overline{CE}$ pin is taken LOW to enable all playback and record operations. The address inputs and playback/record input (P/$\overline{R}$) are latched by the falling edge of CE. CE has additional functionality in the M6 (Push-Button) Operational Mode described later in the Operational Mode section.

PLAYBACK/RECORD INPUT (P/$\overline{R}$)

The P/$\overline{R}$ input is latched by the falling edge of the $\overline{CE}$ pin. A HIGH level selects a playback cycle while a LOW level selects a record cycle. For a record cycle, the address inputs provide the starting address and recording continues until PD or $\overline{CE}$ is pulled HIGH or an overflow is detected (i.e. the chip is full). When a record cycle is terminated by pulling PD or $\overline{CE}$ HIGH, an End-Of-Message ($\overline{EOM}$) marker is stored at the current address in memory. For a playback cycle, the address inputs provide the starting address and the device will play until an $\overline{EOM}$ marker is encountered. The device can continue past an $\overline{EOM}$ marker in an Operational Mode, or if $\overline{CE}$ is held LOW in address mode. (See page 5 for more Operational Modes).

END-OF-MESSAGE / RUN OUTPUT ($\overline{EOM}$)

A nonvolatile marker is automatically inserted at the end of each recorded message. It remains there until the message is recorded over. The EOM output pulses LOW for a period of T_{EOM} at the end of each message.

In addition, the ISD2500 series has an internal V_{CC} detect circuit to maintain message integrity should V_{CC} fall below 3.5 V. In this case, $\overline{EOM}$ goes LOW and the device is fixed in playback-only mode.

When the device is configured in Operational Mode M6 (Push-Button Mode), this pin provides an active-HIGH RUN signal, indicating the device is currently recording or playing. This signal can conveniently drive an LED for a visual indicator of a record or playback operation in process.

OVERFLOW OUTPUT ($\overline{OVF}$)

This signal pulses LOW at the end of memory space, indicating the device has been filled and the message has overflowed. The $\overline{OVF}$ output then follows the $\overline{CE}$ input until a PD pulse has reset the device. This pin can be used to cascade several ISD2500 devices together to increase record/playback durations.

MICROPHONE INPUT (MIC)

The microphone input transfers it's signal to the on-chip preamplifier. An on-chip Automatic Gain Control (AGC) circuit controls the gain of this preamplifier from –15 to 24 dB. An external microphone should be AC coupled to this pin via a series capacitor. The capacitor value, together with the internal 10 KΩ resistance on this pin, determines the low-frequency cutoff for the ISD2500 series passband. See Application Information for additional information on low-frequency cutoff calculation.

MICROPHONE REFERENCE INPUT (MIC REF)

The MIC REF input is the inverting input to the microphone preamplifier. This provides a noise-canceling or common-mode rejection input to the device when connected to a differential microphone.

AUTOMATIC GAIN CONTROL INPUT (AGC)

The AGC dynamically adjusts the gain of the preamplifier to compensate for the wide range of microphone input levels. The AGC allows the full range of whispers to loud sounds to be recorded with minimal distortion. The "attack" time is determined by the time constant of a 5 KΩ internal resistance and an external capacitor (C2 on the schematic on page 18) connected from the AGC pin to V_{SSA} analog ground. The "release" time is determined by the time constant of an external resistor (R2) and an external capacitor (C2) connected in parallel between the AGC Pin and V_{SSA} analog ground. Nominal values of 470 KΩ and 4.7 μF give satisfactory results in most cases.

ANALOG OUTPUT (ANA OUT)

This pin provides the preamplifier output to the user. The voltage gain of the preamplifier is determined by the voltage level at the AGC pin.

ANALOG INPUT (ANA IN)

The analog input pin transfers its signal to the chip for recording. For microphone inputs, the ANA OUT pin should be connected via an external capacitor to the ANA IN pin. This capacitor value, together with the 3.0 KΩ input impedance of ANA IN, is selected to give additional cutoff at the low-frequency end of the voice passband. If the desired input is derived from a source other than a microphone, the signal can be fed, capacitively coupled, into the ANA IN pin directly.

EXTERNAL CLOCK INPUT (XCLK)

The external clock input for the ISD2500 devices has an internal pull-down device. These devices are configured at the factory with an internal sampling clock frequency centered to ±1 percent of specification. The frequency is then maintained to a variation of ±2.25 percent over the entire commercial temperature and operating voltage ranges. The internal clock has a ±5 percent tolerance over the industrial temperature and voltage range. A regulated power supply is recommended for industrial temperature range parts. If greater precision is required, the device can be clocked through the XCLK pin as follows:

Table 1: External Clock Sample Rates

Part Number	Sample Rate	Required Clock
ISD2560	8.0 KHz	1024 KHz
ISD2575	6.4 KHz	819.2 KHz
ISD2590	5.3 KHz	682.7 KHz
ISD25120	4.0 KHz	512 KHz

These recommended clock rates should not be varied because the antialiasing and smoothing filters are fixed, and aliasing problems can occur if the sample rate differs from the one recommended. The duty cycle on the input clock is not critical, as the clock is immediately divided by two. **If the XCLK is not used, this input must be connected to ground.**

SPEAKER OUTPUTS (SP+/SP–)

All devices in the ISD2500 series include an on-chip differential speaker driver, capable of driving 50 mW into 16 Ω from AUX IN (12.2 mW from memory).

The speaker outputs are held at V_{SSA} levels during record and power down. It is therefore not possible to parallel speaker outputs of multiple ISD2500 devices or the outputs of other speaker drivers.

NOTE *Connection of speaker outputs in parallel may cause damage to the device.*

A single output may be used alone (including a coupling capacitor between the SP pin and the speaker). These outputs may be used individually with the output signal taken from either pin. Using the differential outputs results in a 4 to 1 improvement in output power.

NOTE *Never ground or drive an unused speaker output.*

AUXILIARY INPUT (AUX IN)

The Auxiliary Input is multiplexed through to the output amplifier and speaker output pins when $\overline{CE}$ is HIGH, P/$\overline{R}$ is HIGH, and playback is currently not active or if the device is in playback overflow. When cascading multiple ISD2500 devices, the AUX IN pin is used to connect a playback signal from a following device to the previous output speaker drivers. For noise considerations, it is suggested that the auxiliary input not be driven when the storage array is active.

ADDRESS/MODE INPUTS (AX/MX)

The Address/Mode inputs have two functions depending on the level of the two Most Significant Bits (MSB) of the address (A8 and A9).

If either or both of the two MSBs are LOW, the inputs are all interpreted as address bits and are used as the start address for the current record or playback cycle. The address pins are inputs only and do not output internal address information as the operation progresses. Address inputs are latched by the falling edge of CE.

If both MSBs are HIGH, the Address/Mode inputs are interpreted as Mode bits according to the Operational Mode table. There are six Operational Modes (M0..M6) available as indicated in the table. It is possible to use multiple Operational Modes simultaneously. Operational Modes are sampled on each falling edge of $\overline{CE}$, and thus Operational Modes and direct addressing are mutually exclusive.

OPERATIONAL MODES

The ISD2500 series is designed with several built-in Operational Modes that provide maximum functionality with minimum additional components. These are described in detail below. The Operational Modes use the address pins on the ISD2500 devices, but are mapped outside the valid address range. When the two Most Significant Bits (MSBs) are HIGH (A8 and A9), the remaining address signals are interpreted as mode bits and not as address bits. Therefore, Operational Modes and direct addressing are not compatible and cannot be used simultaneously.

There are two important considerations for using Operational Modes. First, all operations begin initially at address 0, which is the beginning of the ISD2500 address space. Later operations can begin at other address locations, depending on the Operational Mode(s) chosen. In addition, the address pointer is reset to 0 when the device is changed from record to playback, playback to record (except M6 mode), or when a Power-Down cycle is executed.

Second, Operational Modes are executed when CE goes LOW and the two MSBs are HIGH. This Operational Mode remains in effect until the next LOW-going CE signal, at which point the current address/mode levels are sampled and executed.

Table 2: Operational Modes Table

Mode Control	Function	Typical Use	Jointly Compatible[1]
M0	Message cueing	Fast-forward through messages	M4, M5, M6
M1	Delete $\overline{EOM}$ markers	Position $\overline{EOM}$ marker at the end of the last message	M3, M4, M5, M6
M2	Not applicable	Reserved	N/A
M3	Looping	Continuous playback from Address 0	M1, M5, M6
M4	Consecutive addressing	Record/play multiple consecutive messages	M0, M1, M5
M5	$\overline{CE}$ level-activated	Allows message pausing	M0, M1, M3, M4
M6	Push-button control	Simplified device interface	M0, M1, M3

1. *Additional Operational Modes can be used simultaneously with the given mode.*

OPERATIONAL MODES DESCRIPTION

The Operational Modes can be used in conjunction with a microcontroller, or they can be hard-wired to provide the desired system operation.

M0 — MESSAGE CUEING

Message Cueing allows the user to skip through messages, without knowing the actual physical addresses of each message. Each $\overline{CE}$ LOW pulse causes the internal address pointer to skip to the next message. This mode should be used for playback only, and is typically used with the M4 Operational Mode.

M1 — DELETE $\overline{EOM}$ MARKERS

The M1 Operational Mode allows sequentially recorded messages to be combined into a single message with only one $\overline{EOM}$ marker set at the end of the final message. When this Operational Mode is configured, messages recorded sequentially are played back as one continuous message.

M2 — UNUSED

When Operational Modes are selected, the M2 pin should be LOW.

M3 — MESSAGE LOOPING

The M3 Operational Mode allows for the automatic, continuously repeated playback of the message located at the beginning of the address space. A message can completely fill the ISD2500 device and will loop from beginning to end without $\overline{OVF}$ going LOW.

M4 — CONSECUTIVE ADDRESSING

During normal operations, the address pointer will reset when a message is played through to an $\overline{EOM}$ marker. The M4 Operational Mode inhibits the address pointer reset on $\overline{EOM}$, allowing messages to be played back consecutively.

M5 — $\overline{CE}$-LEVEL ACTIVATED

The default mode for ISD2500 devices is for $\overline{CE}$ to be edge-activated on playback and level-activated on record. The M5 Operational Mode causes the $\overline{CE}$ pin to be interpreted as level-activated as opposed to edge-activated during playback. This is specifically useful for terminating playback operations using the $\overline{CE}$ signal.

In this mode, $\overline{CE}$ LOW begins a playback cycle, at the beginning of the device memory. The playback cycle continues as long as $\overline{CE}$ is held LOW. When $\overline{CE}$ goes HIGH, playback will immediately end. A new $\overline{CE}$ LOW will restart the message from the beginning unless M4 is also HIGH.

M6 — PUSH-BUTTON MODE

The ISD2500 series of devices contain a Push-Button Operational Mode. The Push-Button mode is used primarily in very low-cost applications and is designed to minimize external circuitry and components, thereby reducing system cost. In order to configure the device in Push-Button Operational Mode, the two most significant address bits must be HIGH, and the M6 mode pin must also be HIGH. A device in this mode always powers down at the end of each playback or record cycle after $\overline{CE}$ goes HIGH.

When this Operational Mode is implemented, several of the pins on the device have alternate functionality:

Table 3: Alternate Functionality in Pins

Pin Name	Alternate Functionality in Push-Button Mode
$\overline{CE}$	Start/Pause Push-Button (LOW pulse-activated)
PD	Stop/Reset Push-Button (HIGH pulse activated)
$\overline{EOM}$	Active-HIGH Run Indicator

$\overline{CE}$ PIN (START/PAUSE)

In Push-Button Operational Mode, $\overline{CE}$ acts as a LOW-going pulse-activated START/PAUSE signal. If no operation is currently in progress, a LOW-going pulse on this signal will initiate a playback or a record cycle according to the level on the P/$\overline{R}$ pin. A subsequent pulse on the $\overline{CE}$ pin, before an End-Of-Message is reached in playback or an overflow condition occurs, will cause the device to pause. The address counter is not reset, and another $\overline{CE}$ pulse will cause the device to continue the operation from the place where it was paused.

PD PIN (STOP/RESET)

In push-button Operational Mode, PD acts as a HIGH-going pulse-activated STOP/RESET signal. When a playback or record cycle is in progress and a HIGH-going pulse is observed on PD, the current cycle is terminated and the address pointer is reset to address 0, the beginning of the message space.

$\overline{EOM}$ PIN (RUN)

In Push-Button Operational Mode, $\overline{EOM}$ becomes an active-HIGH RUN signal which can be used to drive an LED or other external device. It is HIGH whenever a record or playback operation is in progress.

Recording in Push-Button Mode

1. The PD pin should be LOW, usually using a pull-down resistor.
2. The P/$\overline{R}$ pin is taken LOW.
3. The $\overline{CE}$ pin is pulsed LOW. Recording starts, $\overline{EOM}$ goes HIGH to indicate an operation in progress.
4. The $\overline{CE}$ pin is pulsed LOW. Recording pauses. $\overline{EOM}$ goes back LOW. The internal address pointers are not cleared, but an EOM marker is stored in memory to point to the message end. The P/$\overline{R}$ pin may be taken HIGH at this time. Any subsequent $\overline{CE}$ would start a playback at address 0.
5. The $\overline{CE}$ pin is pulsed LOW. Recording starts at the next address after the previous set EOM marker. $\overline{EOM}$ goes back HIGH.

NOTE *If the M1 Operational Mode pin is also HIGH, the just previously written EOM bit is erased, and recording starts at that address.)*

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6. When the recording sequences are finished, the final $\overline{CE}$ pulse LOW will end the last record cycle, leaving a set $\overline{EOM}$ marker at the message end. Recording may also be terminated by a HIGH level on PD, which will leave a set EOM marker.

Playback in Push-Button Mode

1. The PD pin should be LOW.
2. The P/$\overline{R}$ pin is taken HIGH.
3. The $\overline{CE}$ pin is pulsed LOW. Playback starts, $\overline{EOM}$ goes HIGH to indicate an operation in progress.
4. If the $\overline{CE}$ pin is pulsed LOW or an EOM marker is encountered during an operation, the part will pause. The internal address pointers are not cleared, and $\overline{EOM}$ goes back LOW. The P/$\overline{R}$ pin may be changed at this time. A subsequent record operation would not reset the address pointers and the recording would begin where playback ended.
5. $\overline{CE}$ is again pulsed LOW. Playback starts where it left off, with $\overline{EOM}$ going HIGH to indicate an operation in progress.
6. Playback continues as in steps 4 and 5 until PD is pulsed HIGH or overflow occurs.
7. If in overflow, pulling $\overline{CE}$ LOW will reset the address pointer and start playback from the beginning. After a PD pulse, the part is reset to address 0.

NOTE *Push-button mode can be used in conjunction with modes M0, M1, and M3.*

GOOD AUDIO DESIGN PRACTICES

ISD products are very high-quality single-chip voice recording and playback systems. To ensure the highest quality voice reproduction, it is important that good audio design practices on layout and power supply decoupling be followed. See the ISD Application Notes in this book for details.

ISD1000A COMPATIBILITY

The ISD2500 series of devices is designed to provide upward compatibility with the ISD1000A family. When designing with the ISD2500 series, the following differences should be noted.

ADDRESSING

The ISD2560/75/90/120 devices have 480K storage cells designed to provide 60 seconds of storage at a sampling rate of 8.0 KHz. This is approximately four times the storage of the ISD1000A family. To enable the same addressing resolution, two additional address pins have been added. The address space of each device is divisible into 600 increments with valid addressing from 00 to 257 Hex. Some higher addresses are mapped into the Operational Modes. All other addresses are invalid.

OVERFLOW

The ISD1000A series combined two functions on the $\overline{EOM}$ pin: end-of-message indication and overflow. The ISD2500 separates these two functions. Pin 25 (PDIP package) remains as $\overline{EOM}$, but outputs only the EOM signal indication. Pin 22 (PDIP package) becomes $\overline{OVF}$ and pulses LOW only when the device reaches its end of memory, or is "full." This change allows easy message cueing and addressability across device boundaries. This also means that the M2 Operational Mode found in the ISD1000A family is not implemented in the ISD2500 series.

PUSH-BUTTON MODE

The ISD2500 series includes an additional Operational Mode called Push-Button mode. This provides an alternative interface to the record and playback functions of the part. The $\overline{CE}$ and PD pins become redefined as edge-activated "push-buttons." A pulse on $\overline{CE}$ initiates a cycle, and if triggered again, pauses the current cycle without resetting the address pointer (i.e., a Start or Pause function). PD stops any current cycle and resets the address pointer to the beginning of the message space (i.e., a Stop and Reset function). Additionally, the $\overline{EOM}$ pin functions as an active-HIGH run indicator, and can be used to drive an LED indicating a record or playback operation is in progress. Devices in the Push-Button mode cannot be cascaded.

LOOPING MODE

The ISD2500 series can loop with a message that completely fills the memory space.

NOTE *Additional descriptions of ISD2500 device functionality and application examples are provided in the ISD Application Notes in this book.*

TIMING DIAGRAMS

Figure 2: Record

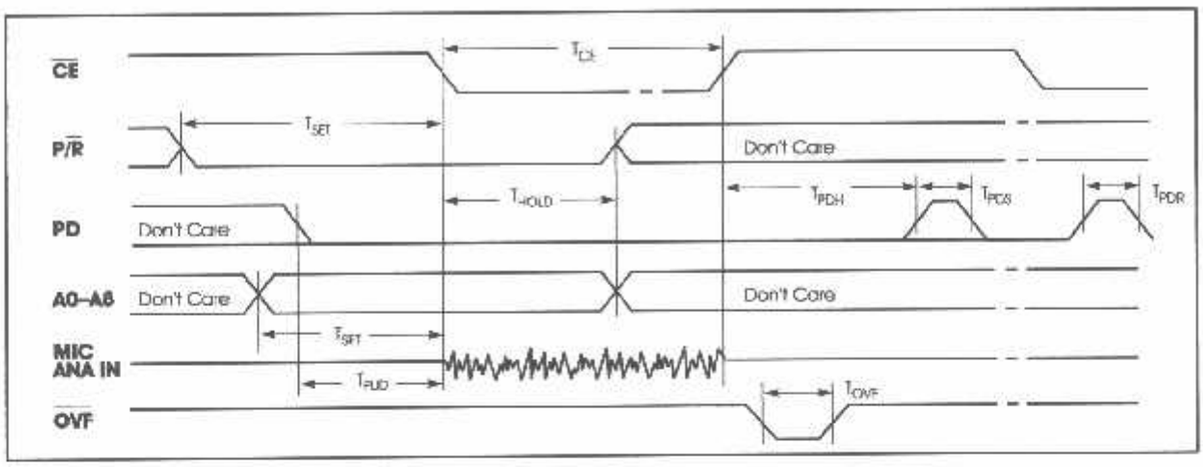


Figure 3: Playback

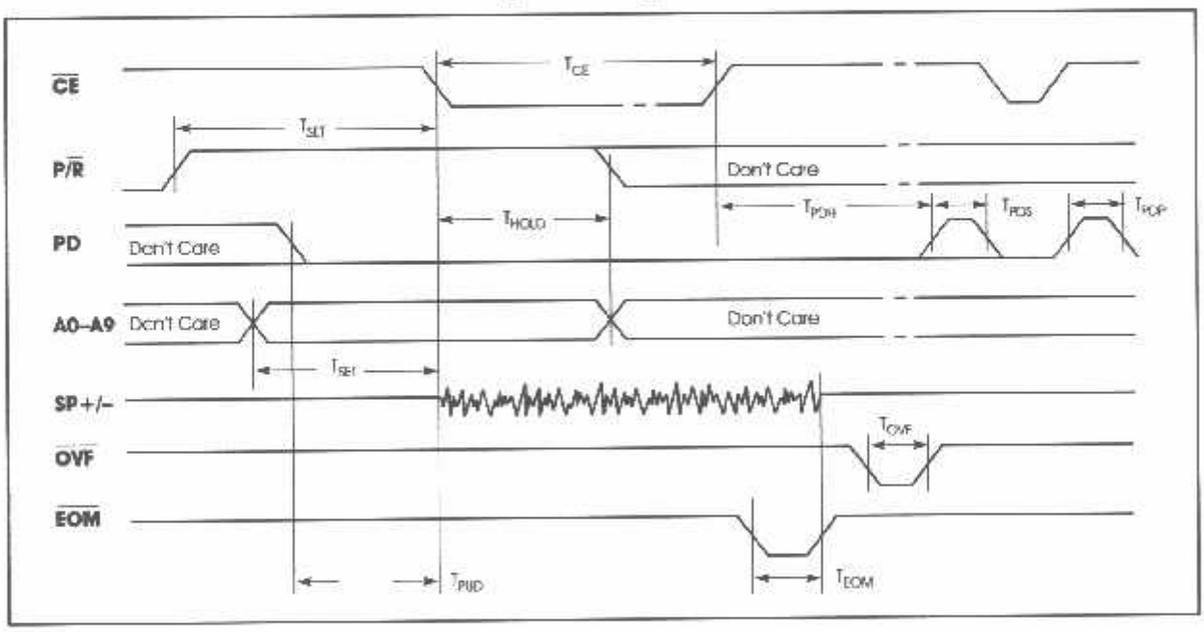


Table 4: Absolute Maximum Ratings (Packaged Parts)[1]

Condition	Value
Junction temperature	150°C
Storage temperature range	-65°C to +150°C
Voltage applied to any pin	(V_{SS} - 0.3 V) to (V_{CC} + 0.3 V)
Voltage applied to any pin (Input current limited to ±20 mA)	(V_{SS} - 1.0 V) to (V_{CC} + 1.0 V)
Lead temperature (soldering - 10 seconds)	300°C
V_{CC} - V_{SS}	-0.3 V to +7.0 V

1. *Stresses above those listed may cause permanent damage to the device. Exposure to the absolute maximum ratings may affect device reliability. Functional operation is not implied at these conditions.*

Table 5: Operating Conditions (Packaged Parts)

Condition	Value
Commercial operating temperature range[1]	0°C to +70°C
Industrial operating temperature range[1]	
Supply voltage (V_{CC})[2]	+4.5 V to +5.5 V
Ground voltage (V_{SS})[3]	0 V

1. *Case temperature.*
2. *$V_{CC} = V_{CCA} = V_{CCD}$.*
3. *$V_{SS} = V_{SSA} = V_{SSD}$.*
4. *Consult factory.*

Table 6: DC Parameters (Packaged Parts)

Symbol	Parameters	Min[2]	Typ[1]	Max[2]	Units	Conditions
V_{IL}	Input Low Voltage			0.8	V	
V_{IH}	Input High Voltage	2.0			V	
V_{OL}	Output Low Voltage			0.4	V	I_{OL} = 4.0 mA
V_{OH}	Output High Voltage	V_{CC}-0.4			V	I_{OH} = -10 µA
V_{OH1}	$\overline{OVF}$ Output High Voltage	2.4			V	I_{OH} = -1.6 mA
V_{OH2}	$\overline{EOM}$ Output High Voltage	V_{CC} - 1.0	V_{CC} - 0.8		V	I_{OH} = -3.2 mA
I_{CC}	V_{CC} Current (Operating)		25	30	mA	$R_{EXT} = \infty$ [3]
I_{SB}	V_{CC} Current (Standby)		1	10	µA	[3]
I_{IL}	Input Leakage Current			±1	µA	
I_{ILPD}	Input Current HIGH w/Pull Down			130	µA	Force V_{CC} [4]
R_{EXT}	Output Load Impedance	16			Ω	Speaker Load
R_{MIC}	Preamp In Input Resistance	4	9	15	KΩ	MIC and MIC REF Pins
R_{AUX}	AUX INPUT Resistance	5	11	20	KΩ	

Table 6: DC Parameters (Packaged Parts)

Symbol	Parameters	Min(2)	Typ (1)	Max(2)	Units	Conditions
$R_{ANA\ IN}$	ANA IN Input Resistance	2.3	3	5	KΩ	
A_{PRE1}	Preamp Gain 1	21	24	26	dB	AGC = 0.0 V
A_{PRE2}	Preamp Gain 2		-15	5	dB	AGC = 2.5 V
A_{AUX}	AUX IN/SP+ Gain		0.98	1.0	V/V	
A_{ARP}	ANA IN to SP+/- Gain	21	23	26	dB	
R_{ACC}	AGC Output Resistance	2.5	5	9.5	KΩ	

1. *Typical values @ T_A = 25°C and 5.0 V.*
2. *All Min/Max limits are guaranteed by ISD via electrical testing or characterization. Not all specifications are 100 percent tested.*
3. *V_{CCA} and V_{CXD} connected together.*
4. *XCLK pin only.*

Table 7: AC Parameters (Packaged Parts)

Symbol	Characteristic		Min(2)	Typ (1)	Max(2)	Units	Conditions
F_S	Sampling Frequency	ISD2560		8.0		KHz	(7)
		ISD2575		6.4		KHz	(7)
		ISD2590		5.3		KHz	(7)
		ISD25120		4.0		KHz	(7)
F_{CF}	Filter Pass Band	ISD2560		3.4		KHz	3 dB Roll-Off Point (3) (8)
		ISD2575		2.7		KHz	3 dB Roll-Off Point (3) (8)
		ISD2590		2.3		KHz	3 dB Roll-Off Point (3) (8)
		ISD25120		1.7		KHz	3 dB Roll-Off Point (3) (8)
T_{REC}	Record Duration	ISD2560	58.1	60.0	62.0	sec	Commercial Operation(7)
		ISD2560	56.5	60.0	63.8	sec	Industrial Operation(7)
		ISD2575	72.6	75.0	77.5	sec	Commercial Operation(7)
		ISD2575	70.7	75.0	79.7	sec	Industrial Operation(7)
		ISD2590	87.1	90.0	93.0	sec	Commercial Operation(7)
		ISD25120	116.1	120.0	123.9	sec	Commercial Operation(7)
T_{PLAY}	Playback Duration	ISD2560	58.1	60.0	62.0	sec	Commercial Operation
		ISD2560	56.5	60.0	63.8	sec	Industrial Operation
		ISD2575	72.6	75.0	77.5	sec	Commercial Operation
		ISD2575	70.7	75.0	79.7	sec	Industrial Operation
		ISD2590	87.1	90.0	93.0	sec	Commercial Operation
		ISD25120	116.1	120.0	123.9	sec	Commercial Operation
T_{CE}	$\overline{CE}$ Pulse Width			100		nsec	
T_{SET}	Control/Address Setup Time			300		nsec	
T_{HOLD}	Control/Address Hold Time			0		nsec	

Table 7: AC Parameters (Packaged Parts)

Symbol	Characteristic		Min[2]	Typ [1]	Max[2]	Units	Conditions
T_{PLD}	Power-Up Delay	ISD2560	24.1	25.0	27.8	msec	Commercial Operation
		ISD2560	23.5		28.5	msec	Industrial Operation
		ISD2575	30.2	31.3	34.3	msec	Commercial Operation
		ISD2575	29.3	31.3	35.2	msec	Industrial Operation
		ISD2590	36.2	37.5	40.8	msec	Commercial Operation
		ISD25120	48.2	50.0	53.6	msec	Commercial Operation
T_{PDR}	PD Pulse Width Record	ISD2560		25		msec	
		ISD2575		31.25		msec	
		ISD2590		37.5		msec	
		ISD25120		50.0		msec	
T_{PDP}	PD Pulse Width Play	ISD2560		12.5		msec	
		ISD2575		15.625		msec	
		ISD2590		18.75		msec	
		ISD25120		25.0		msec	
T_{PDS}	PD Pulse Width Static			100		nsec	(6)
T_{PDH}	Power Down Hold			0		nsec	
T_{EOM}	$\overline{EOM}$ Pulse Width	ISD2560		12.5		msec	
		ISD2575		15.625		msec	
		ISD2590		18.75		msec	
		ISD25120		25.0		msec	
T_{OVF}	Overflow Pulse Width			6.5		µsec	
THD	Total Harmonic Distortion			1	2	%	@ 1 KHz
P_{OUT}	Speaker Output Power			12.2	50	mW	R_{EXT} = 16 Ω [4]
V_{OUT}	Voltage Across Speaker Pins				2.5	V p-p	R_{EXT} = 600 Ω
V_{IN1}	MIC Input Voltage				20	mV	Peak-to-Peak [5]
V_{IN2}	ANA IN Input Voltage				50	mV	Peak-to-Peak
V_{IN3}	Aux Input Voltage				1.25	V	Peak-to-Peak; R_{EXT} = 16 Ω

1. *Typical values @ T_A = 25°C and 5.0 V.*
2. *All Min/Max limits are guaranteed by ISD via electrical testing or characterization. Not all specifications are 100 percent tested.*
3. *Low-frequency cutoff depends upon the value of external capacitors (see Pin Descriptions).*
4. *From AUX IN; if ANA IN is driven at 50 mV p-p, the P_{OUT} = 12.2 mW, typical.*
5. *With 5.1 KΩ series resistor at ANA IN.*
6. *T_{PDS} is required during a static condition, typically overflow.*
7. *Sampling Frequency and playback Duration can vary as much as ±2.25 percent over the commercial temperature range and voltage range and ±5 percent over the industrial temperature and voltage range. For greater stability, an external clock can be utilized (see Pin Descriptions).*
8. *Filter specification applies to both the antialiasing filter and the smoothing filter. Therefore, from input to output, expect a 6 dB drop by nature of passing through both filters.*

TYPICAL PARAMETER VARIATION WITH VOLTAGE AND TEMPERATURE (PACKAGED PARTS)

Chart 1: Record Mode Operating Current (I_{CC})

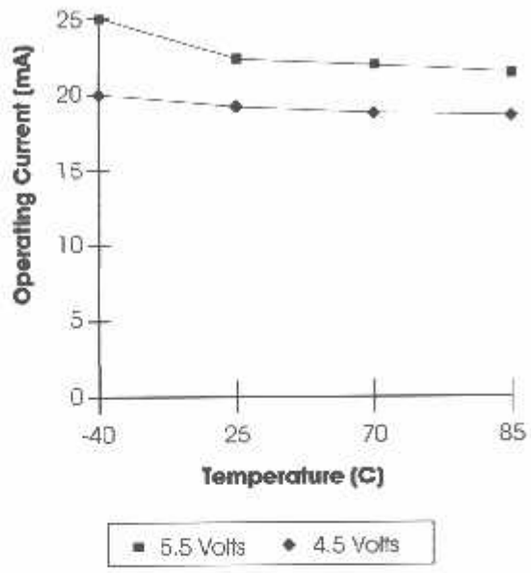


Chart 2: Total Harmonic Distortion

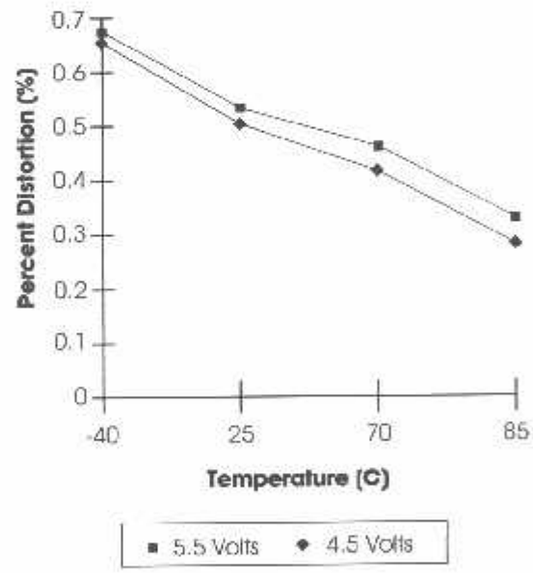


Chart 3: Standby Current (I_{SB})

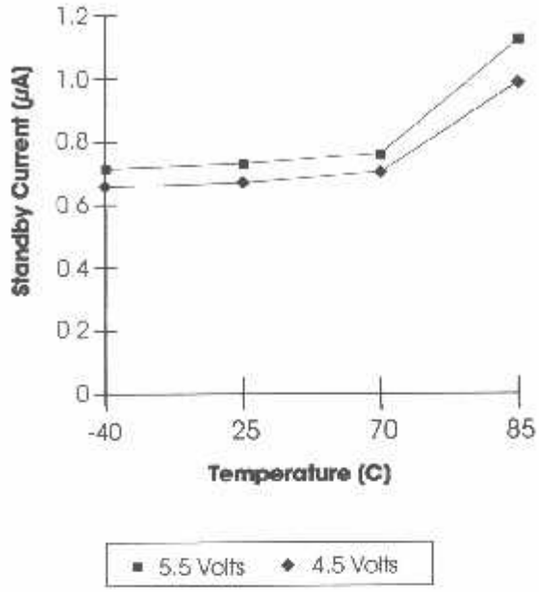


Chart 4: Oscillator Stability

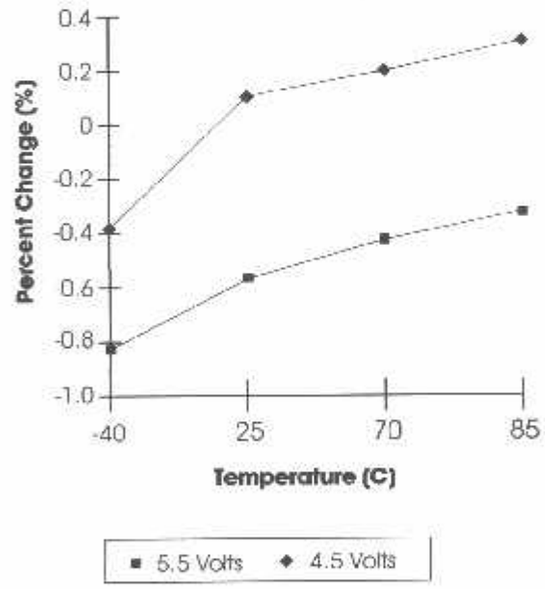


Table 8: Absolute Maximum Ratings (Die)[1]

Condition	Value
Junction temperature	150°C
Storage temperature range	–65°C to +150°C
Voltage applied to any pad	(V_{SS} – 0.3 V) to (V_{CC} + 0.3 V)
Voltage applied to any pad (Input current limited to ±20 mA)	(V_{SS} –1.0 V) to (V_{CC} + 1.0 V)
V_{CC} – V_{SS}	–0.3 V to +7.0 V

1. *Stresses above those listed may cause permanent damage to the device. Exposure to the absolute maximum ratings may affect device reliability. Functional operation is not implied at these conditions.*

Table 9: Operating Conditions (Die)

Condition	Value
Commercial operating temperature range	0°C to +50°C
Supply voltage (V_{CC})[1]	+4.5 V to +6.5 V
Ground voltage (V_{SS})[2]	0 V

1. $V_{CC} = V_{CCA} = V_{CCD}$
2. $V_{SS} = V_{SSA} = V_{SSD}$

Table 10: DC Parameters (Die)

Symbol	Parameters	Min[2]	Typ[1]	Max[2]	Units	Conditions
V_{IL}	Input Low Voltage			0.8	V	
V_{IH}	Input High Voltage	2.0			V	
V_{OL}	Output Low Voltage			0.4	V	I_{OL} = 4.0 mA
V_{OH}	Output High Voltage	V_{CC} – 0.4			V	I_{OH} = –10 µA
V_{OH1}	$\overline{OVF}$ Output High Voltage	2.4			V	I_{OH} = –1.6 mA
V_{OH2}	$\overline{EOM}$ Output High Voltage	V_{CC} – 1.0	V_{CC} – 0.8		V	I_{OH} = –3.2 mA
I_{CC}	V_{CC} Current (Operating)		25	30	mA	$R_{EXT} = \infty$ [3]
I_{SB}	V_{CC} Current (Standby)		1	10	µA	[2]
I_{IL}	Input Leakage Current			±1	µA	
I_{LPD}	Input Current HIGH with Pull Down			130	µA	Force V_{CC} [4]
R_{EXT}	Output Load Impedance	16			Ω	Speaker Load
R_{MIC}	Preamp In Input Resistance	4	9	15	KΩ	MIC and MIC REF Pads
R_{AUX}	AUX INput Resistance	5	11	20	KΩ	
$R_{ANA\ IN}$	ANA IN Input Resistance	2.3	3	5	KΩ	
A_{PRE1}	Preamp Gain 1	21	24	26	dB	AGC = 0.0 V

Table 10: DC Parameters (Die)

Symbol	Parameters	Min[2]	Typ [1]	Max[2]	Units	Conditions
A_{PRE2}	Preamp Gain 2		-15	5	dB	ACC – 2.5 V
A_{AUX}	AUX IN/SP+ Gain		0.98	1.0	V/V	
A_{ARP}	ANA IN to SP+/- Gain	21	23	26	dB	
R_{AGC}	AGC Output Resistance	2.5	5	9.5	KΩ	

1. *Typical values @ T_A = 25°C and 5.0 V.*
2. *All Min/Max limits are guaranteed by ISD via electrical testing or characterization. Not all specifications are 100 percent tested.*
3. *V_{CCA} and V_{CCD} connected together.*
4. *XCLK pad only.*

Table 11: AC Parameters (Die)

Symbol	Characteristic		Min[2]	Typ [1]	Max[2]	Units	Conditions
F_S	Sampling Frequency	ISD2560		8.0		KHz	[7]
		ISD2575		6.4		KHz	[7]
		ISD2590		5.3		KHz	[7]
		ISD25120		4.0		KHz	[7]
F_{CF}	Filter Pass Band	ISD2560		3.4		KHz	3 dB Roll-Off Point [3] [8]
		ISD2575		2.7		KHz	3 dB Roll-Off Point [3] [8]
		ISD2590		2.3		KHz	3 dB Roll-Off Point [3] [8]
		ISD25120		1.7		KHz	3 dB Roll-Off Point [3] [8]
T_{REC}	Record Duration	ISD2560	58.1	60.0	62.0	sec	Commercial Operation [7]
		ISD2575	72.6	75.0	77.5	sec	Commercial Operation [7]
		ISD2590	87.1	90.0	93.0	sec	Commercial Operation [7]
		ISD25120	116.1	120.0	123.9	sec	Commercial Operation [7]
T_{PLAY}	Playback Duration	ISD2560	58.1	60.0	62.0	sec	Commercial Operation [7]
		ISD2575	72.6	75.0	77.5	sec	Commercial Operation [7]
		ISD2590	87.1	90.0	93.0	sec	Commercial Operation [7]
		ISD25120	116.1	120.0	123.9	sec	Commercial Operation [7]
T_{CE}	$\overline{CE}$ Pulse Width			100		nsec	
T_{SET}	Control/Address Setup Time			300		nsec	
T_{HOLD}	Control/Address Hold Time			0		nsec	
T_{PUD}	Power-Up Delay	ISD2560	24.1	25.0	27.8	msec	Commercial Operation
		ISD2575	30.2	31.3	34.3	msec	Commercial Operation
		ISD2590	36.2	37.5	40.8	msec	Commercial Operation
		ISD25120	48.2	50.0	53.6	msec	Commercial Operation

Table 11: AC Parameters (Die)

Symbol	Characteristic		Min[2]	Typ [1]	Max[2]	Units	Conditions
T_{PDR}	PD Pulse Width Record	ISD2560		25		msec	
		ISD2575		31.25		msec	
		ISD2590		37.5		msec	
		ISD25120		50.0		msec	
T_{PDP}	PD Pulse Width Play	ISD2560		12.5		msec	
		ISD2575		15.625		msec	
		ISD2590		18.75		msec	
		ISD25120		25.0		msec	
T_{PDS}	PD Pulse Width Static			100		nsec	[6]
T_{PDH}	Power Down Hold			0		nsec	
T_{EOM}	$\overline{EOM}$ Pulse Width	ISD2560		12.5		msec	
		ISD2575		15.625		msec	
		ISD2590		18.75		msec	
		ISD25120		25.0		msec	
T_{OVF}	Overflow Pulse Width			6.5		µsec	
THD	Total Harmonic Distortion			1	3	%	@ 1 KHz
P_{OUT}	Speaker Output Power			12.2	50	mW	R_{EXT} = 16 Ω[4]
V_{OUT}	Voltage Across Speaker Pins				2.5	V p-p	R_{EXT} = 600 Ω
V_{IN1}	MIC Input Voltage				20	mV	Peak-to-Peak [5]
V_{IN2}	ANA IN Input Voltage				50	mV	Peak-to-Peak
V_{IN3}	Aux Input Voltage				1.25	V	Peak-to-Peak; R_{EXT} = 16 Ω

1. *Typical values @ T_A = 25°C and 5.0 V.*
2. *All Min./Max limits are guaranteed by ISD via electrical testing or characterization. Not all specifications are 100 percent tested.*
3. *Low-frequency cutoff depends upon the value of external capacitors (see Pin Descriptions).*
4. *From AUX IN; if ANA IN is driven at 50 mV p-p, the P_{OUT} = 12.2 mW, typical.*
5. *With 5.1 KΩ series resistor at ANA IN.*
6. *T_{PDS} is required during a static condition, typically overflow.*
7. *Sampling Frequency and playback Duration can vary as much as +2.25 percent over the commercial temperature range and voltage range. For greater stability, an external clock can be utilized (see Pin Descriptions).*
8. *Filter specification applies to the antialiasing filter and the smoothing filter.*

TYPICAL PARAMETER VARIATION WITH VOLTAGE AND TEMPERATURE (DIE)

Chart 5: Record Mode Operating Current (I_{CC})

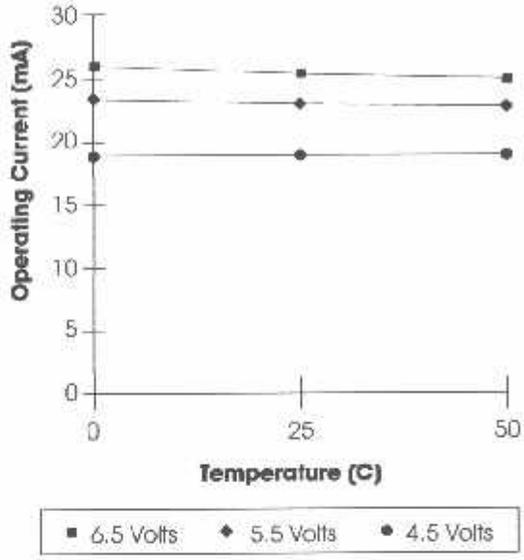


Chart 7: Standby Current (I_{SB})

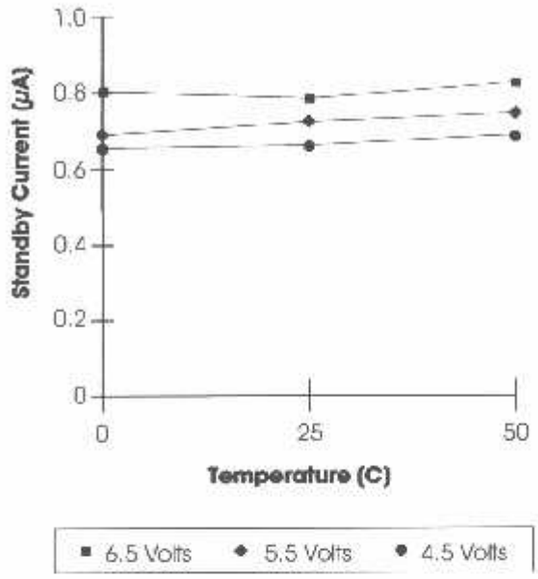


Chart 6: Total Harmonic Distortion

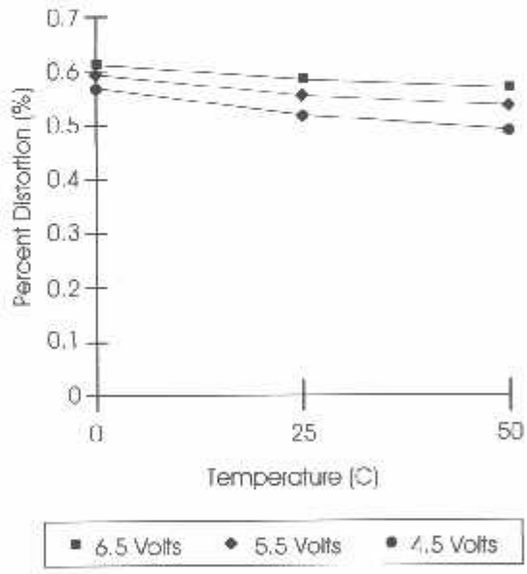


Chart 8: Oscillator Stability

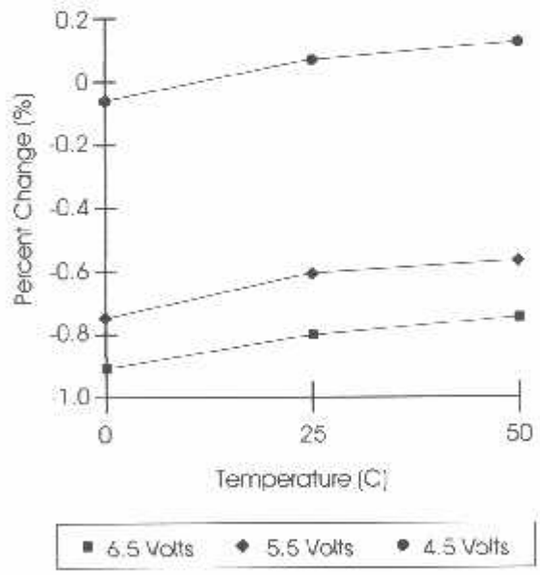
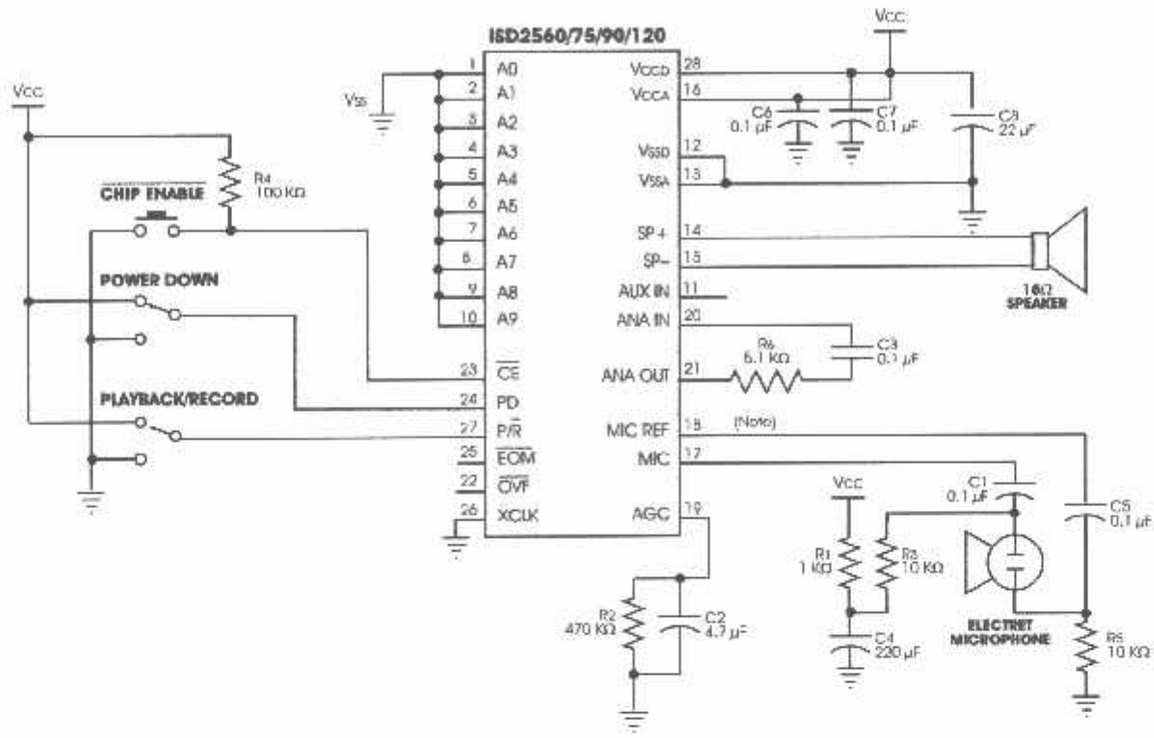


Figure 4: ISD2560/75/90/120 Application Example—Design Schematic



NOTE: *If desired, pin 18 (PDIP package) may be left unconnected (microphone preamplifier noise will be higher). In this case, pin 18 must not be tied to any other signal or voltage. Additional design example schematics are provided in the Application Notes in this book.*

Table 12: Application Example—Basic Device Control

Control Step	Function	Action
1	Power up chip and select record/playback mode	(1.) PD = LOW, (2.) P/$\overline{R}$ = As desired
2	Set message address for record/playback	Set addresses A0–A9
3A	Begin playback	P/$\overline{R}$ = HIGH, $\overline{CE}$ = Pulsed LOW
3B	Begin record	P/$\overline{R}$ = LOW, $\overline{CE}$ = LOW
4A 4B	End playback End record	Automatic PD or $\overline{CE}$ = HIGH

Table 13: Application Example—Passive Component Functions

Part	Function	Comments
R1	Microphone power supply decoupling	Reduces power supply noise
R2	Release time constant	Sets release time for AGC
R3, R5	Microphone biasing resistors	Provides biasing for microphone operation
R4	Series limiting resistor	Reduces level to prevent distortion at higher supply voltages.
R6	Series limiting resistor	Reduces level to high supply voltages
C1, C5	Microphone DC-blocking capacitor Low-frequency cutoff	Decouples microphone bias from chip. Provides single-pole low frequency cutoff and common mode noise rejection.
C2	Attack/Release time constant	Sets attack/release time for AGC
C3	Low-frequency cutoff capacitor	Provides additional pole for low-frequency cutoff
C4	Microphone power supply decoupling	Reduces power supply noise
C6, C7, C8	Power supply capacitors	Filter and bypass of power supply

EXPLANATION

In this simplified block diagram of a microcontroller application, the Push-Button mode and message cueing are used. The microcontroller is a 16-pin version with enough port pins for buttons, an LED, and the ISD2500 series device. The software can be written to use three buttons: one each for play and record, and one for message selection. Because the microcontroller is interpreting the buttons and commanding the ISD2500 device, software can be written for any functions desired in a particular application.

NOTE *ISD does not recommend connecting address lines directly to a microprocessor bus. Address lines should be externally latched.*

Figure 5: ISD2560/75/90/120 Application Example—Microcontroller/ISD2500 Interface

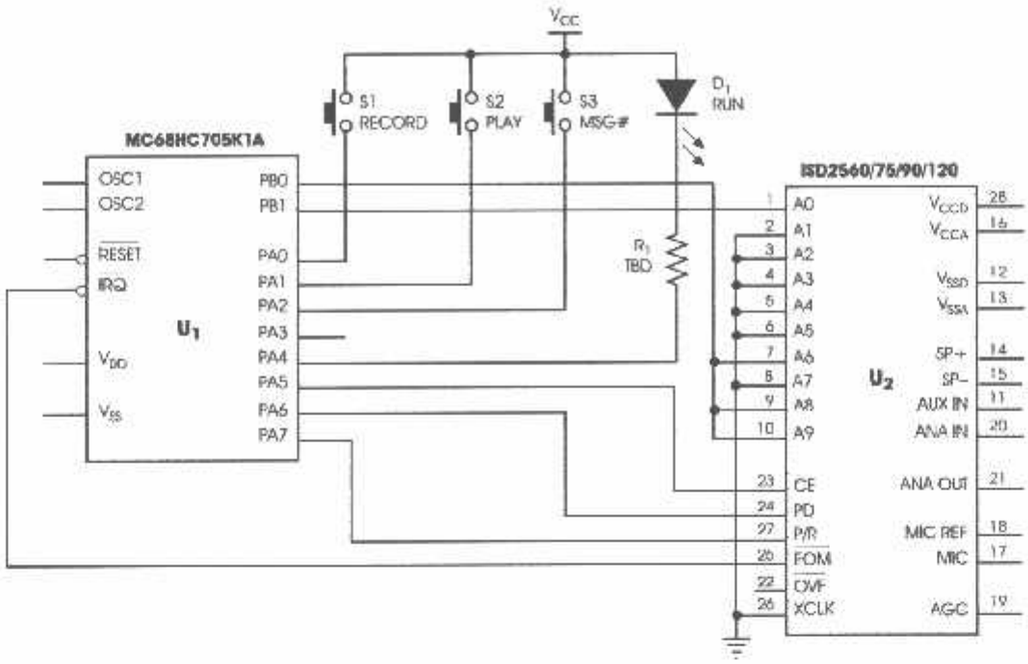
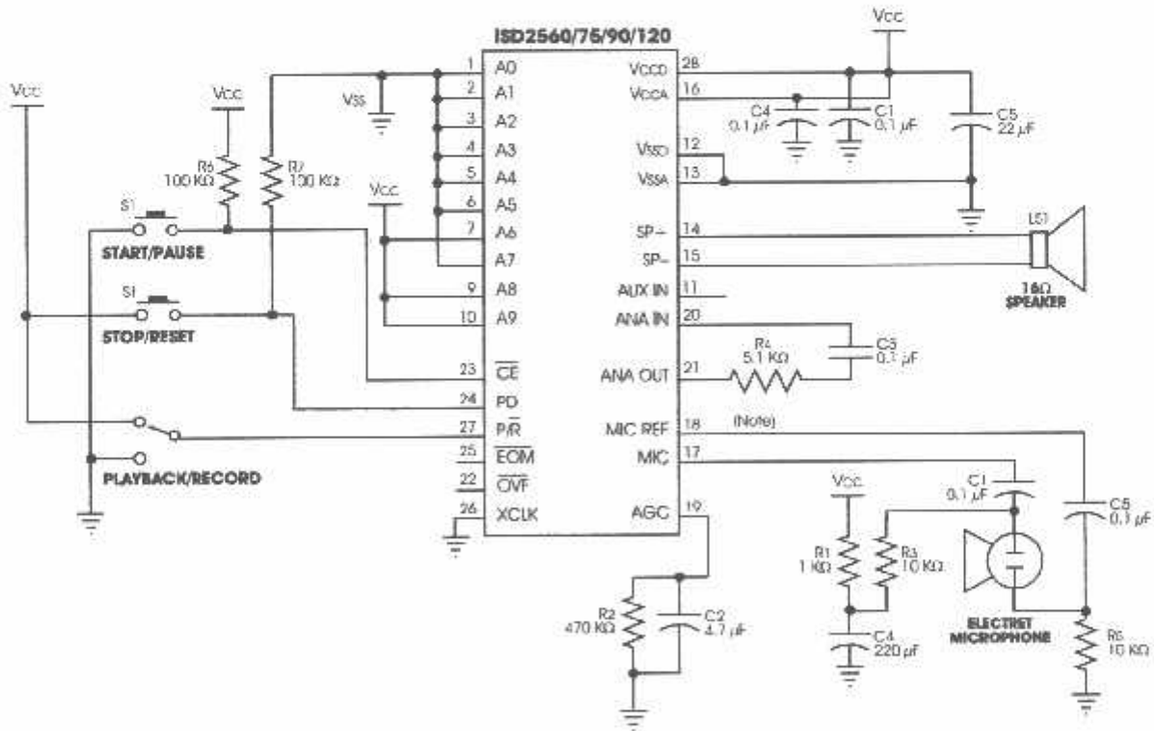


Figure 6: ISD2500 Application Example—Push-Button



NOTE: *Please refer to Application Information.*

Table 14: Application Example—Push-Button Control

Control Step	Function	Action
1	Select record/playback mode	P/$\overline{R}$ – As desired
2A 2B	Begin playback Begin record	P/$\overline{R}$ = HIGH, $\overline{CE}$ = Pulsed LOW P/$\overline{R}$ = LOW, $\overline{CE}$ = Pulsed LOW
3	Pause record or playback	$\overline{CE}$ – Pulsed LOW
4A 4B	End playback End record	Automatic at $\overline{EOM}$ marker or PD – Pulsed HIGH PD = Pulsed HIGH

Table 15: Application Example—Passive Component Functions

Part	Function	Comments
R2	Release time constant	Sets release time for AGC
R4	Series limiting resistor	Reduces level to prevent distortion at higher supply voltages
R6, R7	Pull-up and pull-down resistors	Defines static state of inputs
C1, C4, C5	Power supply capacitors	Filters and bypass of power supply
C2	Attack/Release time constant	Sets attack/release time for AGC
C3	Low-frequency cutoff capacitor	Provides additional pole for low-frequency cutoff

Table 16: Push-Button Parameters

Symbol	Characteristic		Min	Typ (1)	Max	Units	Conditions
T_{CE}	$\overline{CE}$ Pulse Width [Start/Pause]			300		nsec	
T_{SET}	Control/Address Setup Time			300		nsec	
T_{PUD}	Power-Up Delay	ISD2560 ISD2575 ISD2590 ISD25120		25 31.25 37.25 50.0		msec msec msec msec	
T_{PD}	PD Pulse Width [Stop/Reset]			300		nsec	
T_{RUN}	$\overline{CE}$ to $\overline{EOM}$ HIGH		25		400	nsec	
T_{PALSL}	$\overline{CE}$ to $\overline{EOM}$ LOW		50		400	nsec	
T_{DB}	$\overline{CE}$ HIGH Debounce	ISD2560 ISD2575 ISD2590 ISD25120	70 85 105 135		105 135 160 215	msec msec msec msec	

PUSH-BUTTON TIMING DIAGRAMS

Figure 7: Push-Button Mode Record

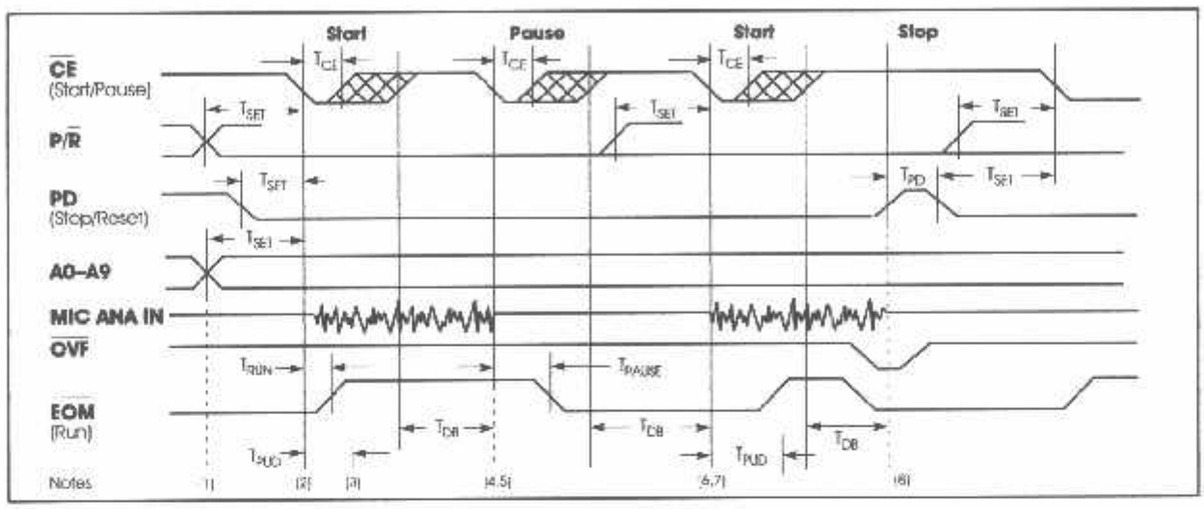
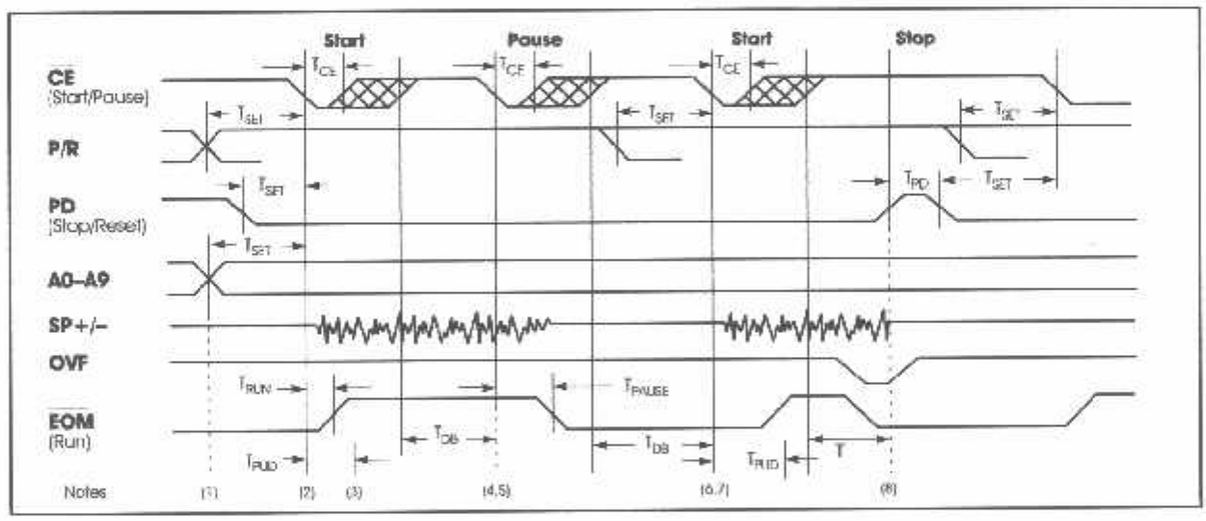


Figure 8: Push-Button Mode Playback



1. *A9, A8, and A6 = 1 for push-button operation.*
2. *The first $\overline{CE}$ LOW pulse performs a Start function.*
3. *The part will begin to play or record after a power-up delay T_{PUD}.*
4. *The part must have $\overline{CE}$ HIGH for a debounce period TDB before it will recognize another falling edge of $\overline{CE}$ and pause.*
5. *The second $\overline{CE}$ LOW pulse, and every even pulse thereafter, performs a Pause function.*
6. *Again, the part must have $\overline{CE}$ HIGH for a debounce period TDB before it will recognize another falling edge of $\overline{CE}$, which would restart an operation. In addition, the part will not do an internal power down until $\overline{CE}$ is HIGH for the TDB time.*
7. *The third $\overline{CE}$ LOW pulse, and every odd pulse thereafter, performs a Resume function.*
8. *At any time, a HIGH level on PD will stop the current function, reset the address counter, and power down the device.*

DEVICE PHYSICAL DIMENSIONS

Figure 9: 28-Lead 8x13.4mm Plastic Thin Small Outline Package (TSOP) Type I (E)

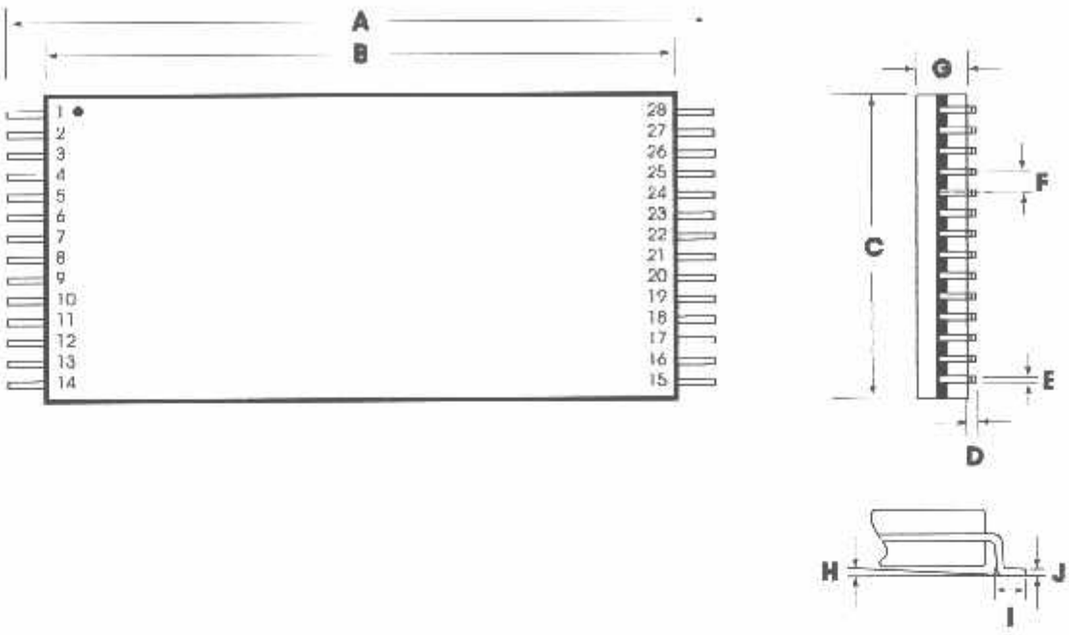


Table 17: Plastic Thin Small Outline Package (TSOP) Type I (E) Dimensions

	INCHES			MILLIMETERS		
	Min	Nom	Max	Min	Nom	Max
A	0.520	0.528	0.535	13.20	13.40	13.60
B	0.461	0.465	0.469	11.70	11.80	11.90
C	0.311	0.315	0.319	7.90	8.00	8.10
D	0.002		0.006	0.05		0.15
E	0.007	0.009	0.011	0.17	0.22	0.27
F		0.0217			0.55	
G	0.037	0.039	0.041	0.95	1.00	1.05
H	0°	3°	6°	0°	3°	6°
I	0.020	0.022	0.028	0.50	0.55	0.70
J	0.004		0.008	0.10		0.21

NOTE: *Lead coplanarity to be within 0.004 inches.*

Figure 10: 28-Lead 0.600-Inch Plastic Dual Inline Package (PDIP) (P)

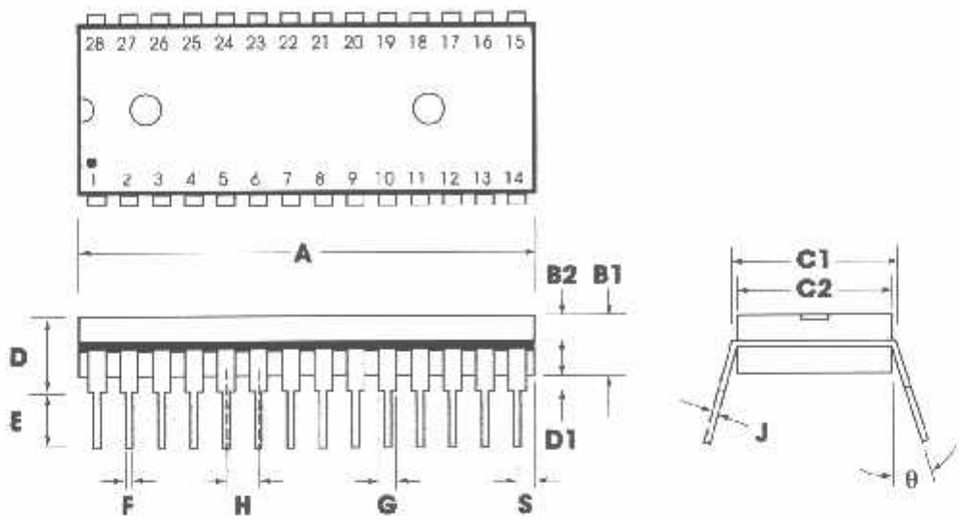


Table 18: Plastic Dual Inline Package (PDIP) (P) Dimensions

	INCHES			MILLIMETERS		
	Min	Nom	Max	Min	Nom	Max
A	1.445	1.450	1.455	36.70	36.83	36.96
B1		0.150			3.81	
B2	0.065	0.070	0.075	1.65	1.78	1.91
C1	0.600		0.625	15.24		15.88
C2	0.530	0.540	0.550	13.46	13.72	13.97
D			0.19			4.83
D1	0.015			0.38		
E	0.125		0.135	3.18		3.43
F	0.015	0.018	0.022	0.38	0.46	0.56
G	0.055	0.060	0.065	1.40	1.52	1.65
H		0.100			2.54	
J	0.008	0.010	0.012	0.20	0.25	0.30
S	0.070	0.075	0.080	1.78	1.91	2.03
q	0°		15°	0°		15°

NOTE: *Lead coplanarity to be within 0.004 inches.*

Figure 11: 32-Lead 8x20mm Plastic Thin Small Outline Package (TSOP) Type I (T)

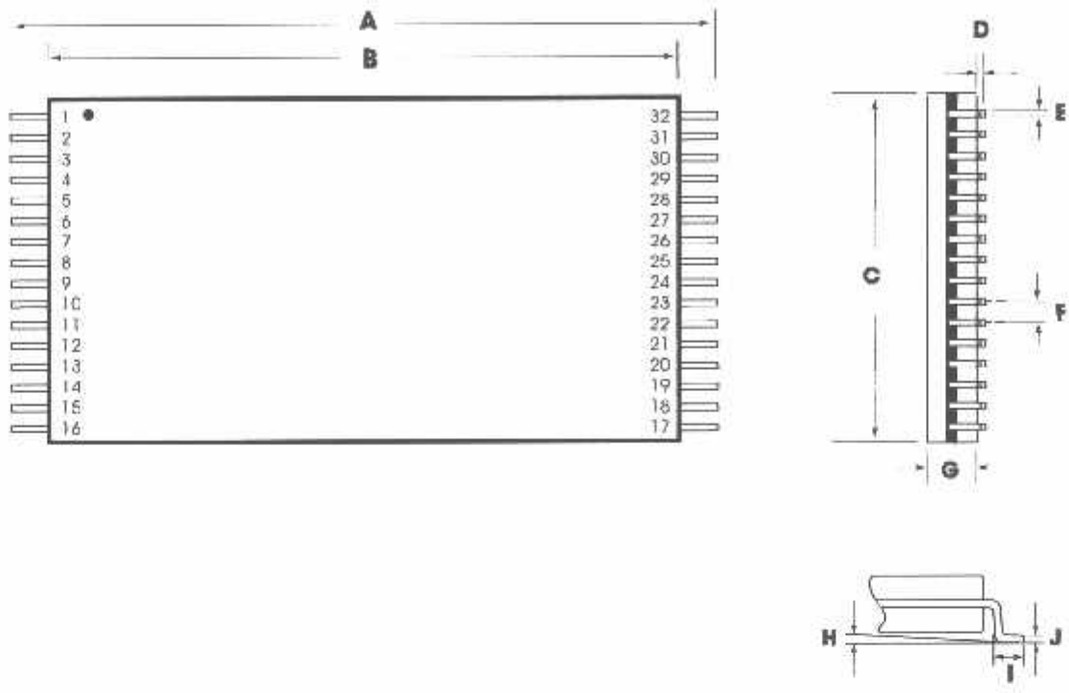


Table 19: Plastic Thin Small Outline Package (TSOP) Type I (T) Dimensions

	INCHES			MILLIMETERS		
	Min	Nom	Max	Min		Max
A	0.780	0.787	0.795	19.80	20.00	20.20
B	0.720	0.724	0.728	18.30	18.40	18.50
C	0.311	0.315	0.319	7.90	8.00	8.10
D	0.002		0.006	0.05		0.15
E	0.006	0.009	0.011	0.17	0.22	0.27
F		0.0197			0.50	
G	0.037	0.039	0.041	0.95	1.00	1.05
H	0°	3°	5°	0°	3°	5°
I	0.020	0.024	0.028	0.50	0.60	0.70
J	0.004		0.008	0.10		0.21

NOTE: *Lead coplanarity to be within 0.002 inches.*

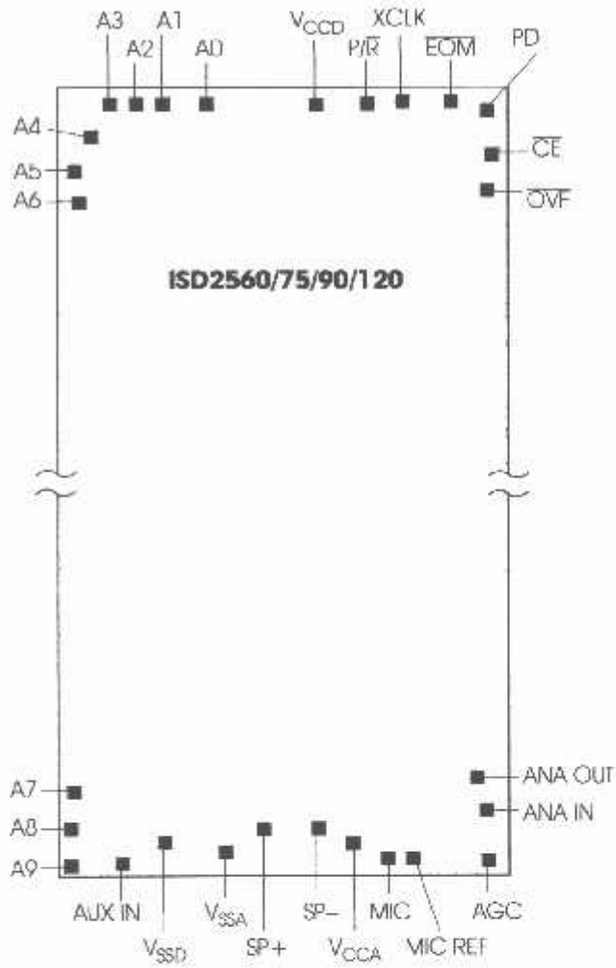
Figure 12: ISD2560/75/90/120 Products *Current* Bonding Physical Layout[1] (Unpackaged Die)

ISD2560/75/90/12[2]

I. Die Dimensions
X: 187 ±1 mils
Y: 399 ±1 mils

II. Die Thickness[2]
17.5 −1 mils

III. Pad Opening
109 x 109 microns
4.3 x 4.3 mils



1. *The backside of die is internally connected to V_{SS}. It **MUST NOT** be connected to any other potential or damage may occur.*
2. *Die thickness is subject to change, please contact ISD factory for status.*

Table 20: ISD2560/75/90/120 Products *Current* PIN/PAD Designations, with Respect to Die Center (µm)

Pin	Pin Name	X Axis	Y Axis
A0	Address 0	-1148.9	4898.2
A1	Address 1	-1406.9	4898.2
A2	Address 2	-1661.9	4898.2
A3	Address 3	-1916.9	4898.2
A4	Address 4	-2069.9	4608.2
A5	Address 5	-2194.9	4358.2
A6	Address 6	-2194.9	4108.2
A7	Address 7	-2194.9	-4212.3
A8	Address 8	-2194.9	-4456.3
A9	Address 9	-2076.4	-4897.3
AUX IN	Auxiliary Input	-1607.9	-4868.3
V_{SSD}	V_{SS} Digital Power Supply	-1343.9	-4850.8
V_{SSA}	V_{SS} Analog Power Supply	-551.9	-4834.8
SP+	Speaker Output +	-111.4	-4790.8
SP-	Speaker Output -	425.6	-4790.8
V_{CCA}	V_{CC} Analog Power Supply	865.1	-4848.32
MIC	Microphone Input	1320.7	-4897.3
MIC REF	Microphone Reference	1605.1	-4897.3
AGC	Automatic Gain Control	1877.6	-4871.3
ANA IN	Analog Input	2202.11	-4269.8
ANA OUT	Analog Output	2123.1	-3910.8
$\overline{OVF}$	Overflow Output	2142.6	4154.7
$\overline{CE}$	Chip Enable Input	2202.1	4558.7
PD	Power Down Input	2048.1	4898.2
$\overline{EOM}$	End of Message	1648.1	4865.7
XCLK	No Connect (optional)	1221.1	4898.2
P/$\overline{R}$	Playback/Record	965.6	4898.2
V_{CCD}	V_{CC} Digital Power Supply	646.1	4895.7

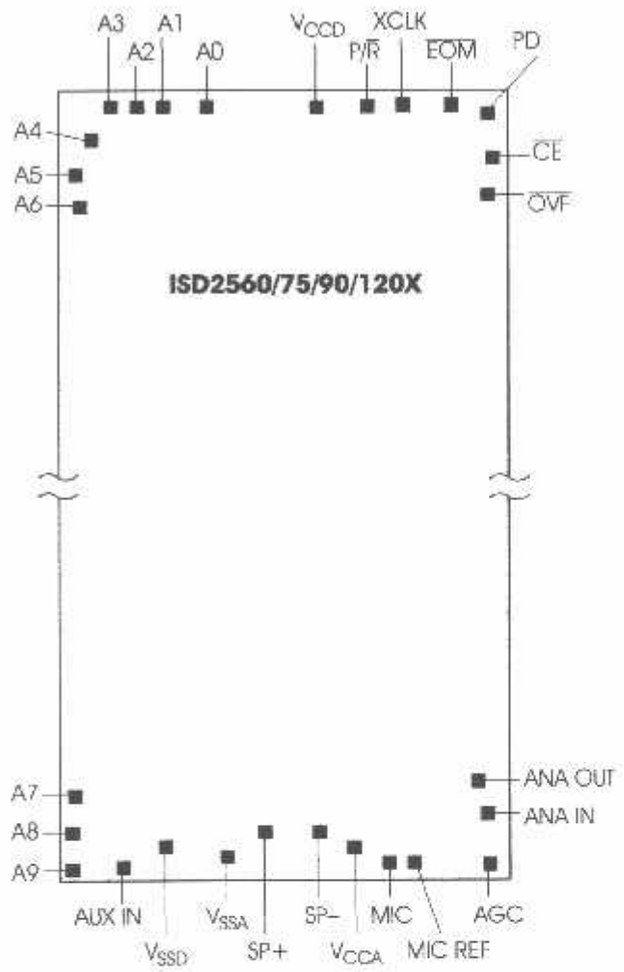
Figure 13: ISD2560/75/90/120 Products *Future* Bonding Physical Layout[1] (Unpackaged Die)

ISD2560/75/90/120X[2]

I. Die Dimensions
X: 149.5 ±1 mils
Y: 262.0 ±1 mils

II. Die Thickness[2]
11.8 ±.4 mils

III. Pad Opening
111 x 111 microns
4.4 x 4.4 mils



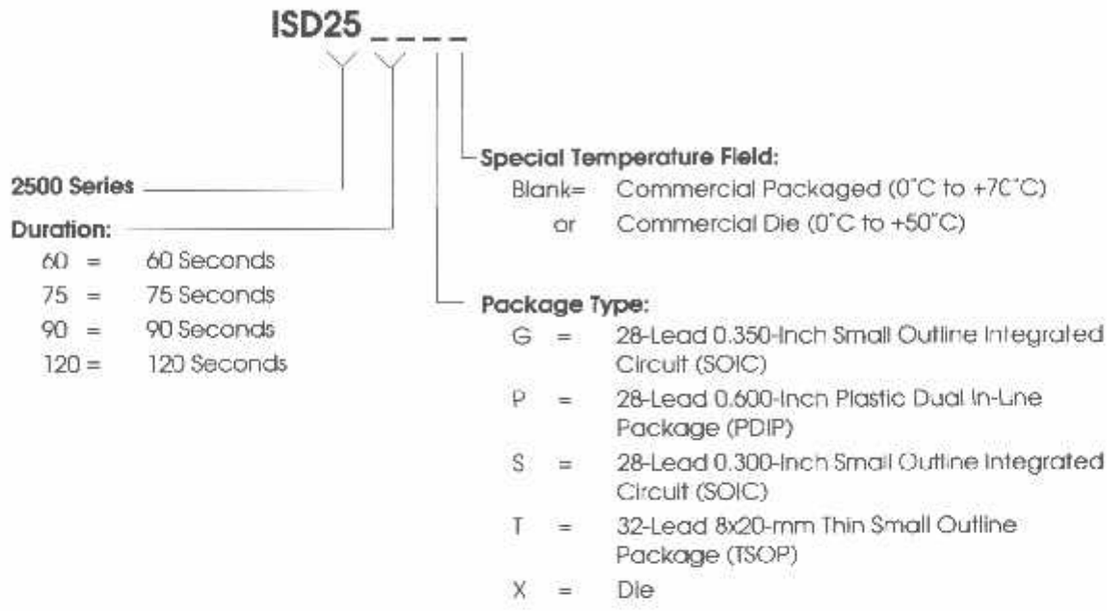
1. *The backside of die is internally connected to V_{SS}. It **MUST NOT** be connected to any other potential or damage may occur.*
2. *Die thickness is subject to change, please contact ISD factory for status and availability.*

Table 21: ISD2560/75/90/120 Products *Future* PIN/PAD Designations, with Respect to Die Center (µm)

Pin	Pin Name	X Axis	Y Axis
A0	Address 0	-897.9	3135.2
A1	Address 1	-1115.4	3135.2
A2	Address 2	-1331.0	3135.2
A3	Address 3	-1544.0	3135.2
A4	Address 4	-1640.4	2868.9
A5	Address 5	-1698.2	2671.0
A6	Address 6	-1698.2	2441.5
A7	Address 7	-1731.2	-2583.2
A8	Address 8	-1731.2	-2768.4
A9	Address 9	-1731.2	-3050.8
AUX IN	Auxiliary Input	-1410.1	-3115.7
V_{SSD}	V_{SS} Digital Power Supply	-1112.8	-3096.2
V_{SSA}	V_{SS} Analog Power Supply	-407.8	-3138.5
SP+	Speaker Output +	-47.4	-3067.7
SP-	Speaker Output -	386.9	-3067.7
V_{CCA}	V_{CC} Analog Power Supply	746.5	-3110.4
MIC	Microphone Input	1101.2	-3146.0
MIC REF	Microphone Reference	1294.7	-3146.0
AGC	Automatic Gain Control	1666.4	-3130.3
ANA IN	Analog Input	1728.6	-2654.0
ANA OUT	Analog Output	1700.9	-2411.0
$\overline{OVF}$	Overflow Output	1340.9	3121.7
$\overline{CE}$	Chip Enable Input	1726.7	2824.4
PD	Power Down Input	1730.5	3094.0
$\overline{EOM}$	End of Message	1340.9	3121.7
XCLK	No Connect (optional)	986.5	3160.7
P/$\overline{R}$	Playback/Record	807.2	3163.4
V_{CCD}	V_{CC} Digital Power Supply	544.7	3159.2

ORDERING INFORMATION

Product Number Descriptor Key



When ordering ISD2560/75/90/120 products, please refer to the following valid part numbers.

Part Number	Part Number	Part Number	Part Number
ISD2560G	ISD2575G	ISD2590G	ISD25120G
ISD2560P	ISD2575P	ISD2590P	ISD25120P
ISD2560S	ISD2575S	ISD2590S	ISD25120X
ISD2560T	ISD2575T	ISD2590T	
ISD2560X	ISD2575X	ISD2590X	

For the latest product information, access ISD's worldwide website at http://www.isd.com.