SKRIPSI

PERENCANAAN DAN PEMBUATAN OSILOSKOP BERBASIS KOMPUTER

Disusun Oleh:

WANDA DWI CAHYADI

NIM : 04.12.275

KONSENTRASI TEKNIK ELEKTRONIKA

JURUSAN TEKNIK ELEKTRO S-1

FAKULTAS TEKNOLOGI INDUSTRI

INSTITUT TEKNOLOGI NASIONAL MALANG

2009

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PERENCANAAN DAN PEMBUATAN OSILOSKOP BERBASIS KOMPUTER

SKRIPSI

Disusun dan Diajukan Sebagai Salah Satu Syarat Untuk Memperoleh Gelar Sarjana Teknik Elektronika Strata Satu (S-1)

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PERENCANAAN DAN PEMBUATAN OSILOSKOP BERBASIS KOMPUTER

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Abstraksi

Osiloskop ini terdiri dari rangkaian pemrosesan sinyal dan pengubah nilai analog ke digital. Untuk tampilannya digunakan computer dengan interface port parallel. Prinsip kerjanya adalah dengan memproses sinyal – sinyal analog yang kemudian di ubah kedalam nilai – nilai digital. Nilai – nilai digital tersebut dikirim kekomputer dan ditampilkan bentuk gelombangnya.

Rangkaian pemrosesan sinyal ini terdiri dari rangkaian penyearah gelombang penuh presisi dan rangkaian pensampling sinyal (sample and hold). Nilai – nilai analog tersebut kemudian diubah ke bentuk digital agar dapat diproses oleh computer. Nilai – nilai digital tersebut mewakili bentuk gelombang yang terjadi pada tampilan di konputer. Setelah pengujian, dapat diambil kesimpulan bahwa alat ini masih memiliki error karena noise dari komponen maupun rangkaian yang digunakan.

Kata Kunci *: Osiloskop, sine wave, ADC 0804.*

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Pembuatan skripsi ini disusun guna memenuhi syarat akhir kelulusan pendidikan jenjang Strata 1 di Institut Teknologi Nasional Malang. Dalam penyusunan skripsi ini penulis banyak mendapat bantuan baik moril maupun materil, saran dan dorongan semangat dari berbagai pihak, untuk itu penulis mengucapkan terima kasih kepada :

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Akhir kata, penulis mohon maaf kepada semua pihak bilamana selama penyusunan skripsi ini penyusun membuat kesalahan secara tidak sengaja dan semoga skripsi ini dapat bermanfaat bagi kita semua.

Malang, Agustus 2009

Penulis

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BAB I
PENDAHULUAN

1.1 Latar belakang

Perkembangan ilmu pengetahuan dan teknologi memudahan aktivitas manusia dalam berbagai aspek kchidupan. Salah satunya adalah osiloskop. Osiloskop adalah alat ukur besaran listrik yang dapat memetakan sinyal listrik. Osiloskop sangat penting untuk analisa rangkaian elektronik.

Setiap orang biasanya ingin mengetahui hal – hal yang belum pernah di cobanya. Banyak mahasiswa yang ingin mengetahui bagaimana prinsip kerja dari rangkaiannya, bagaimana bentuk gelombang dari rangkaian yang ia punya dan analisa – analisa yang lainnya tetapi tidak dapat di coba dikarenakan tidak mempunyai alat. Sebagai contoh saja bila kita ingin mengetahui bentuk gelombang dari suatu rangkaian, sangat kurang efisiennya bila kita ingin mencoba tetapi harus membeli osiloskop terlebih dahulu yang harganya relative mahal. Keterbatasan tersebut dapat membuat kita menjadi tidak ingin untuk melakukan percobaan lebih jauh..

Osiloskop digital pada umumnya, dalam menampilkan bentuk gelombang terlebih dahulu mensampling atau mencuplik sinyal analog dan menyimpan demikian banyak nilai dan kemudian berhenti. Nilai-nilai tegangan tersebut disimpan bersama sama dengan skala waktu gelombangnya di memori. Dengan menggunakan ADC (Analog to Digital Converter) nilai – nilai tegangan yang dicuplik diubah ke besaran digital. Pada prinsipnya, osiloskop digital hanya mencuplik dan menyimpan demikian

banyak nilai dan kemudian berhenti. Ia mengulang proses ini lagi dan lagi sampai dihentikan. Bentuk gelombang yang ditampilkan oleh osiloskop biasanya adalah berbentuk sinus, kotak, segitiga dan gergaji tergantung inputan yang diberikan. Gelombang sinus adalah gelombang yang paling hakiki yang dapat menyusun berbagai bentuk gelombang lainnya. Sebagai contoh gelombang kotak/persegi, pada dasarnya juga adalah terdiri dari gelombang sinus dengan frekuensi tertentu sebagai frekuensi *fundamental* ditambah dengan sangat banyak gelombang – gelombang harmoninya. Dengan mengetahui prinsip tersebut penulis mencoba membuat osiloskop sederhana tentunya dengan harga yang murah dan dengan komponen – komponen yang mudah di dapat.

1.2 Rumusan Masalah

Dari latar belakang di atas maka permasalahan dari sekripsi ini adalah :

1. Bagaimana mengolah nilai – nilai analog menjadi besaran digital.
2. Bagaimana membuat program agar dapat mengambil outputan dari *hardware* yang kemudian dapat di tampilkan di computer.

1.3 Batasan Masalah

Permasalahan dari skripsi ini dibatasi pada :

1. Tegangan yang akan di ukur adalah 0 – 5 volt.
2. Bentuk gelombang yang akan di tampilkan hanya gelombang sinus.
3. Osiloskop hanya mempunyai 1 channel.

4. Frekuensi yang digunakan 1 Khz.

1.4 Tujuan

Tujuan dari skripsi ini adalah membuat osiloskop sederhana dengan komponen – komponen yang mudah di dapat dan memudahkan dalam menganalisa bentuk gelombang.

1.5 Metodologi

Metodologi dari proyek akhir ini adalah :

1. *Studi Literature.*

   Ini merupakan tahap awal mempelajari materi – materi yang akan digunakan pada proyek akhir ini, dalam hal ini cara kerja osilloskop.

2. Perancangan *Hardware.*

   Perancangan hardware adalah menggabungkan rangkaian – rangkaian yang di perlukan sehingga menjadi osilloskop. Adapun rangkaian yang di gunakan yaitu rangkaian penyearah gelombang penuh presisi, rangkaian *sampling and hold*, rangkaian ADC 0804 dan rangkaian *Multiplexer*.

3. Perancangan Perangkat Lunak.

   Ini adalah suatu perancangan program untuk menampilkan bentuk gelombang di computer menggunakan program delphi7.

4. Pengujian dan Analisa.

Setelah *hardware* dan *software* selesai di buat, maka dilakukan pengujian dengan berbagai percobaan dan menganalisanya.

1.6 Sistematika Pembahasan

Bab I : Bab ini berisi tentang pendahuluan yang terdiri dari latar belakang, permasalahan, batasan masalah, tujuan, metodologi dan sistematika pembahasan.

Bab II : Bab ini menjelaskan teori penunjang yang dijadikan landasan dan rujukan perhitungan dalam mengerjakan skripsi ini, antara lain pemrosesan sinyal, *Sample and Hold, Analog to Digital Converter* (ADC), *port parallel, Multiplexer* .

Bab III : Bab ini membahas tentang perencanaan dan pembuatan *hardware* dan *software* osiloskop.

Bab IV : Bab ini membahas tentang pengujian system osilloskop yang telah di buat.

Bab V : Bab ini berisi penutup yang meliputi kesimpulan dari keseluruhan pengerjaan skripsi dan saran – saran untuk memperbaiki kelemahan system yang di buat demi pengembangan dan penyempurnaan di waktu mendatang.

BAB II
DASAR TEORI

2.1. Pendahuluan

Pada bab ini akan dibahas mengenai teori penunjang dari peralatan yang direncanakan. Pokok pembahasan pada bab ini adalah

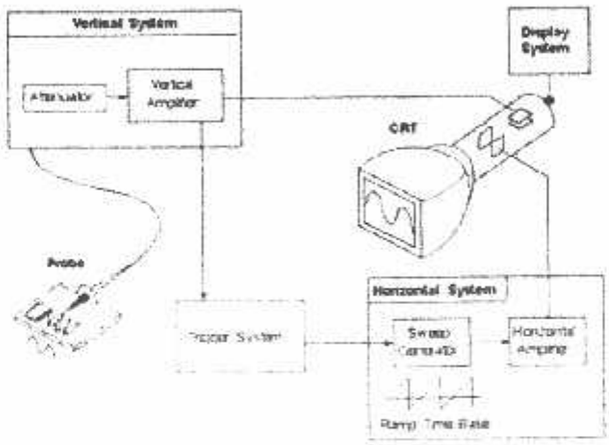
1. Osiloskop *Analog* dan *Digital*..
2. Penyearah Gelombang Penuh Presisi.
3. *Sample and Hold*
4. *Analog to Digital Converter* (ADC) 0804
5. *Multiplexer.*
6. *Port Parallel.*

2.2 Osiloskop *Analog* dan *Digital.*

Dalam bidang elektronika, osiloskop merupakan instrumen ukur yang memiliki posisi yang sangat vital mengingat sifatnya yang mampu menampilkan bentuk gelombang yang dihasilkan oleh rangkaian yang sedang diamati. Dewasa ini secara prinsip ada dua tipe osiloskop, yakni tipe analog (ART - analog real time oscilloscope,) dan tipe digital (DSO - digital storage osciloscope), masing-masing memiliki kelebihan dan keterbatasan.

1. **Osiloskop *Analog***

Cara kerja dari osiloskop analog adalah sinyal tegangan mengalir dari probe menuju ke pengaturan vertikal dari sebuah sistem osiloskop (Vertical System) seperti terlihat pada gambar 2.1. Sebuah *Attenuator* akan melemahkan sinyal tegangan masukan sedangkan *Amplifier* akan menguatkan sinyal tegangan masukan. Pengaturan ini ditentukan pada saat menggerakkan kenop "Volt/Div" pada *user interface* Osiloskop.



Gambar 2.1 Prinsip Kerja Osiloskop Analog
Sumber : materi-elektro-osiloskop-oscilloscope.html

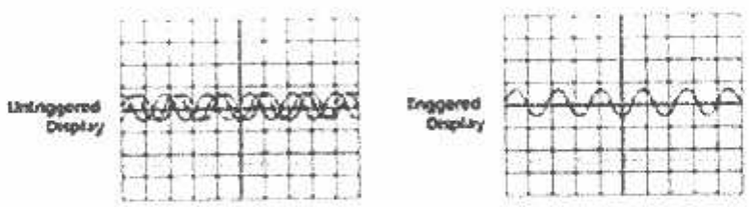
Tegangan yang keluar dari sistem vertikal lalu diteruskan menuju *Pelat Defleksi vertikal* pada sebuah *CRT (Catode Ray Tube)* , sinyal tegangan yang dimasukkan ke pelat ini nantinya akan digunakan oleh CRT untuk menggerakkan berkas – berkas elektron secara bidang vertikal saja (Ke atas atau ke bawah). Sampai pada penjelasan ini dapat di simpulkan bahwa *vertical system* pada osiloskop analog adalah untuk mengatur penampakan *amplitudo* dari sinyal yang diamati.

Kemudian sinyal masuk ke dalam plat *defleksi vertikal*. Sinyal tegangan yang teraplikasikan disini menyebabkan berkas – berkas elektron bergerak. Tegangan positif mengakibatkan berkas elektron bergerak keatas, sedangkan tegangan negatif menyebabkan elektron terdorong kebawah

Sinyal yang keluar dari *vertikal sytem* tadi juga diarahkan kc *trigger system* untuk memicu *sweep* generator dalam menciptakan apa yang disebut dengan "*Horizontal Sweep*".

Pengaturan beberapa kali elektron bergerak menyebrangi layar inilah yang dapat kita anggap sebagai pengaturan periode / frekuensi yang tampak pada layar, bentuk konkretnya adalah saat kita menggerakkan kenop Time/Div pada Osiloskop.

Bersama, pengaturan bidang vertikal dan horizontal ahirnya dapat merepresentasikan sinyal tegangan yang diamati kedalam bentuk grafik seperti pada gambar 2.2.



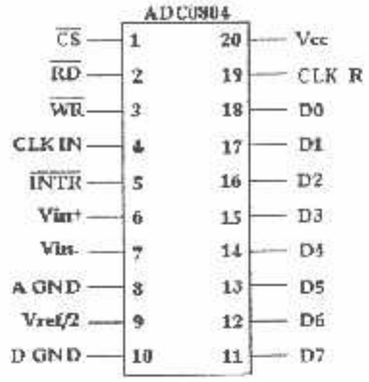
Gambar 2.2 bentuk geombang hasil dari bidang vertikal dan horizontal
Sumber : materi-elektro-osiloskop-oscilloscope.html

2. Osiloskop *Digital*

Dalam sebagian besar osiloskop digital, sinyal masukan yang sedang diukur pertama kali akan melewati sebuah pelemah (*attenuator*) dan penguat depan (*preamplifier*). Bagian-bagian ini memang serupa dengan bagian pada osiloskop analog, yang merupakan bagian kecil fungsi analog dari sebuah osiloskop *digital*. Pemberhentian sinyal yang berikutnya adalah pada ADC (*analog todigital conversion*) yang tak terdapat pada osiloskop analog. Setelah sinyal masukan di sampling (diambil nilainya dengan dicuplik secara berkala), data – data tersebut lalu di digitalkan dan kemudian disimpan bersama skala waktu gelombangnya di dalam memori. Pada prinsipnya osiloskop digital hanya menyuplik dan menyimpan demikian banyak nilai kemudian berhenti. Proses ini diulangi terus sampai osiloskop dimatikan.

2.3 ADC (*Analog to Digital Converter*)

Analog to Digital Converter (ADC) adalah sebuah piranti yang dirancang untuk mengubah besaran *analog* menjadi besaran *digital*. IC ADC 0804 dianggap dapat memenuhi kebutuhan dari rangkaian yang akan dibuat. IC jenis ini bekerja secara cermat dengan menambahkan sedikit komponen sesuai dengan spesifikasi yang harus diberikan dan dapat mengkonversikan secara cepat suatu masukan tegangan. Hal-hal yang juga perlu diperhatikan dalam penggunaan ADC ini adalah tegangan maksimum yang dapat dikonversikan oleh ADC dari rangkaian pengkondisi sinyal, resolusi, pewaktu eksternal ADC, tipe keluaran, ketepatan dan waktu konversinya.

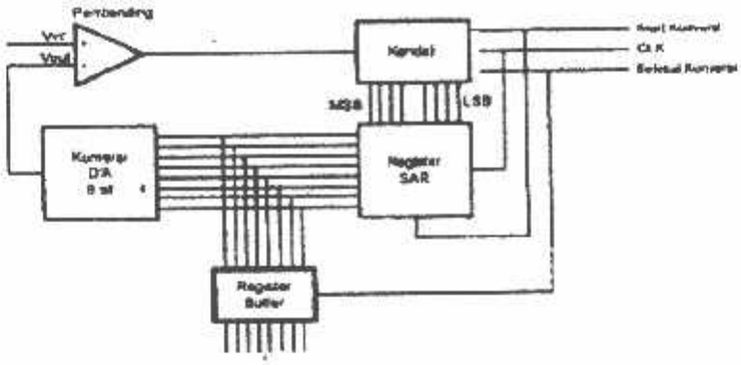


Gambar 2.3 Konfigurasi PIN ADC 0804
Sumber : www.datasheet.com

Beberapa karakteristik penting ADC:

1. Waktu konversi
2. Resolusi
3. Ketidaklinieran
4. Akurasi.

Ada banyak cara yang dapat digunakan untuk mengubah sinyal analog menjadi sinyal digital yang nilainya proposional. Jenis ADC yang biasa digunakan dalam perancangan adalah jenis *successive approximation convertion* atau pendekatan bertingkat yang memiliki waktu konversi jauh lebih singkat dan tidak tergantung pada nilai masukan analognya atau sinyal yang akan diubah. Dalam Gambar 2-2 memperlihatkan diagram blok ADC tersebut.



Gambar 2.4 Diagram Blok ADC
Sumber : www.datasheet.com

Secara singkat prinsip kerja dari konverter A/D adalah semua bit-bit diset kemudian diuji, dan bilamana perlu sesuai dengan kondisi yang telah ditentukan. Dengan rangkaian yang paling cepat, konversi akan diselesaikan sesudah 8 clock, dan keluaran D/A merupakan nilai analog yang ekivalen dengan nilai register SAR.

Apabila konversi telah dilaksanakan, rangkaian kembali mengirim sinyal selesai konversi yang berlogika rendah. Sisi turun sinyal ini akan menghasilkan data digital yang ekivalen ke dalam register buffer. Dengan demikian, keluaran digital akan tetap tersimpan sekalipun akan di mulai siklus konversi yang baru.

IC ADC 0804 mempunyai dua masukan analog, Vin (+) dan Vin (-), sehingga dapat menerima masukan diferensial. Masukan analog sebenarnya (Vin) sama dengan selisih antara tegangan-tegangan yang dihubungkan dengan ke dua pin masukan yaitu Vin= Vin (+) – Vin (-). Kalau masukan analog berupa tegangan tunggal, tegangan ini harus dihubungkan dengan Vin (+), sedangkan Vin (-) digroundkan. Untuk operasi normal, ADC 0804 menggunakan Vcc = +5 Volt sebagai tegangan referensi. Dalam

hal ini jangkauan masukan analog mulai dari 0 Volt sampai 5 Volt (skala penuh), karena IC ini adalah SAC 8-bit, resolusinya akan sama dengan

$$\text{Resolusi} = \left(\frac{\text{tegangan skala penuh}}{2^n - 1}\right) = \frac{5\ \text{Volt}}{255} = 19{,}6\ \text{mVolt}$$

(n menyatakan jumlah bit keluaran biner IC *analog to digital converter*)

IC ADC 0804 memiliki generator *clock internal* yang harus diaktifkan dengan menghubungkan sebuah resistor eksternal (R) antara pin CLK OUT dan CLK IN serta sebuah kapasitor *eksternal* (C) antara CLK IN dan *ground digital*. Frekuensi clock yang diperoleh di pin CLK OUT sama dengan :

$$f = \frac{0{,}91}{RC}$$

Untuk sinyal clock ini dapat juga digunakan sinyal eksternal yang dihubungkan ke pin CLK IN. ADC 0804 memilik 8 keluaran digital sehingga dapat langsung dihubungkan dengan saluran data mikrokomputer. Masukan (chip select, aktif rendah) digunakan untuk mengaktifkan ADC 0804. Jika berlogika tinggi, ADC 0804 tidak aktif (disable) dan semua keluaran berada dalam keadaan impedansi tinggi.

Masukan (*write atau start convertion*) digunakan untuk memulai proses konversi. Untuk itu harus diberi pulsa logika 0. Sedangkan keluaran (*interrupt atauend of convertion*) menyatakan akhir konversi. Pada saat dimulai konversi, akan berubah ke logika 1. Di akhir konversi akan kembali ke logika 0.

2.3.1 Mode Operasi ADC0804

1. Mode Opersi Kontinyu

Agar ADC0804 dapat dioperasikan pada mode operasi kontinyu (proses membaca terus menerus dan tanpa proses operasi jabat tangan), maka penyemat CS dan RD ditanahkan, sedangkan penyemat WR dan INTR tidak dihubungkan kemanapun. Prinsip kerja operasi kontinyu ini yaitu ADC akan memulai konversi ketika INTR kembali tidak aktif (logika '1'). Setelah proses konversi selesai, INTR akan aktif (logika '0'). Untuk memulai konversi pertama kali WR harus ditanahkan terlebih dahulu, hal ini digunakan untuk mereset SAR. Namun pada konversi berikutnya untuk mereset SAR dapat menggunakan sinyal INTR saat aktif (logika '0') dan mulai konversi saat tidak aktif (logika '1').

Ketika selesai konversi data hasil konversi akan dikeluarkan secara langsung dari buffer untuk dibaca karena RD ditanahkan. Saat sinyal INTR aktif, sinyal ini digunakan untuk me-reset SAR. Saat INTR kembali tidak aktif (logika '1') proses konversi dimulai kembali.

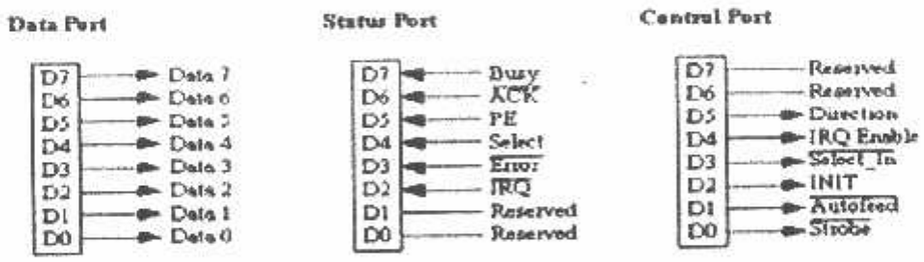
2. Mode Operasi Hand-Shaking

ADC0804 dioperasikan pada *mode hand shaking* . Agar ADC dapat bekerja, CS harus berlogika '0'. Ketika WR berlogika '0', register SAR akan direset, sedangkan ketika sinyal WR kembali '1', maka proses konversi segera dimulai. Selama konversi sedang berlangsung, sinyal INTR akan tidak aktif (berlogika '1'), sedangkan saat konversi selesai ditandai dengan aktifnya sinyal INTR (logika '0').

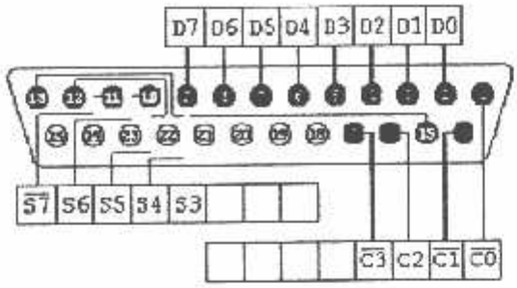
Setelah proses konversi selesai data hasil konversi tetap tertahan pada buffer ADC. Data hasil konversi tersebut akan dikeluarkan dengan mengirim sinyal RD berlogika '0'. Setelah adanya sinyal sinyal RD ini, maka sinyal INTR kembali tidak aktif.

2.4 Parallel Port DB25

Parallel port adalah port yang paling banyak digunakan dalam *interfacing* dengan berbagai macam peralatan *eksternal*. Secara umum parallel port terdiri dari 4 jalur kontrol, 5 jalur status dan 8 jalur data seperti ditunjukkan dalam Gambar 2.3. Hubungan pengkabelan yang umum digunakan yaitu konektor tipe DB25 seperti ditunjukkan dalam Gambar 2.4. Konektor DB25 merupakan konektor yang paling banyak dijumpai pada paralel port PC, sedangkan *konektor centronic* dijumpai pada printer.



Gambar 2.5 Port-port dalam Paralel Port
Sumber : www.datasheet.com



Gambar 2.6 Susunan pin *eksternal soket* DB-25 female pada port parallel PC IBM
Sumber : www.datasheet.com

Gambar 2.7 Bentuk Fisik DB-25
Sumber : www.datasheet.com

Paralel port yang telah distandarisasi dibawah standard IEEE 1284, pertama diperkenalkan pada tahun 1994. Standard tersebut didefinisikan dalam 5 mode operasi, yaitu:

1. Mode kompabilitas (*Compability Mode*)
2. Mode 4 bit (*Nibble Mode*)
3. Mode 8 bit (*Byte Mode*)
4. Mode parallel port lanjutan (*Enhanced Paralel Port-EPP*)
5. Mode kapabilitas diperluas (*Extended Capability Port-ECP*)

Konfigurasi parallel port

Tabel 2-1 Pin Out Parallel Port

PIN NO.	FUNCTION	TYPE
1.	STROBE	CONTROL
2.	DATA BIT 0	OUTPUT
3.	DATA BIT 1	OUTPUT
4.	DATA BIT 2	OUTPUT
5.	DATA BIT 3	OUTPUT
6.	DATA BIT 4	OUTPUT
7.	DATA BIT 5	OUTPUT
8.	DATA BIT 6	OUTPUT
9	DATA BIT 7	OUTPUT
10.	ACKNOWLEDGE	STATUS
11.	BUSY	STATUS
12.	PE: PAPER TRAY EMPTY	STATUS
13.	PRINTER ON-LINE	STATUS
14.	AUTO LINEFEED AFTER (CR) CARRIAGE RETURN	CONTROL
15.	PRINTER ERROR	STATUS
16.	INITIALIZE PRINTER	CONTROL
17.	SELECT/DESELECT PRINTER	CONTROL
18-25.	UNUSED/GROUND	

Sumber : www.datasheet.com

Tabel Pengalamatan Parallel Port

Table 2-2 Port Data

Offset	Name	Read/Write	Bit No.	Properties
Base + 0	Data Port	Write (Note-1)	Bit 7	Bit 7
			Bit 6	Data 6
			Bit 5	Data 5
			Bit 4	Data 4
			Bit 3	Data 3
			Bit 2	Data 2
			Bit 1	Data 1
			Bit 0	Data 0

Sumber : www.datasheet.com

Table 2-4 Port Status

Offset	Name	Read/Write	Bit No.	Properties
Base + 1	Status Port	Read Only	Bit 7	Busy
			Bit 6	Ack
			Bit 5	Paper Out
			Bit 4	Select In
			Bit 3	Error
			Bit 2	IRQ (Not)
			Bit 1	Reserved
			Bit 0	Reserved

Sumber : www.datasheet.com

Table 2-5 Port Kontrol

Offset	Name	Read/Write	Bit No.	Properties
Base + 2	Control Port	Read/Write	Bit 7	Unused
			Bit 6	Unused
			Bit 5	Enable Bi-Directional Port
			Bit 4	Enable IRQ Via Ack Line
			Bit 3	Select Printer
			Bit 2	Initialize Printer (Reset)
			Bit 1	Auto Linefeed
			Bit 0	Strobe

Sumber : www.datasheet.com

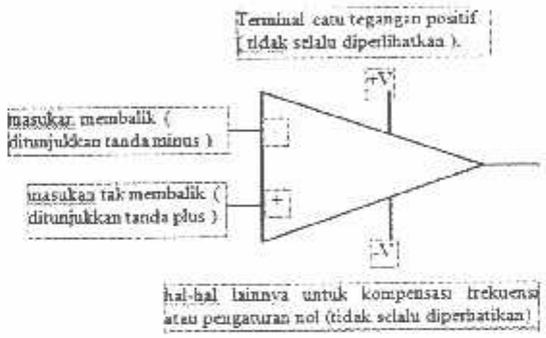
2.5 *Operasional Amplifier* (Penguat Operasi)

Penguat operasional atau op-amp adalah rangkaian elektronik yang dirancang secara khusus sehingga dengan manambahkan komponen luar sedikit saja dapat dipakai untuk berbagai keperluan. Dengan teknologi rangkaian terpadu (IC) yang telah ditingkatkan, op-amp dalam bentuk kemasan IC menjadi jauh lebih mudah dan murah dan amat luas pemakaiannya.

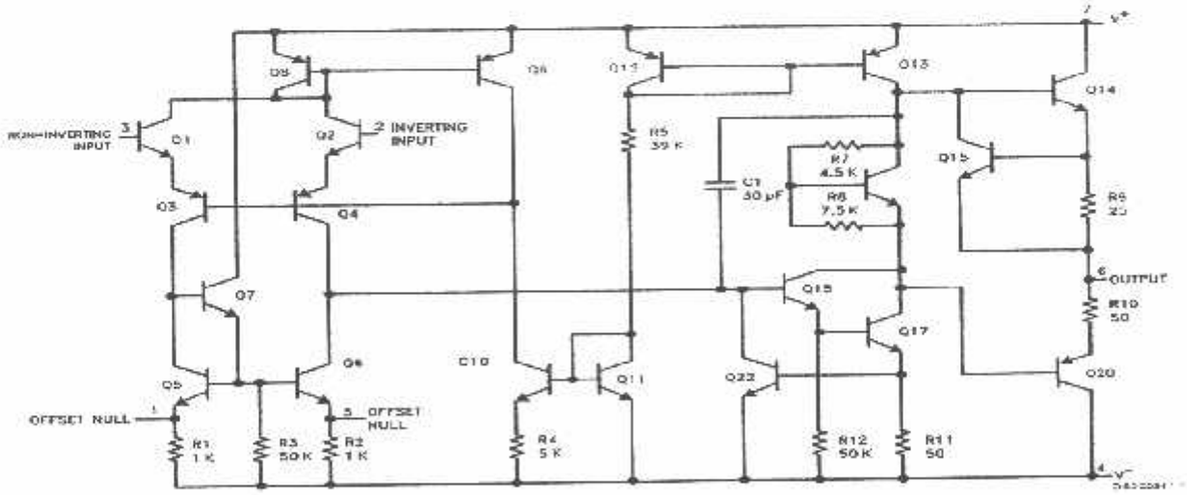
Op-amp IC adalah piranti solid state yang mampu mengindra dan memperkuat sinyal masuk baik AC maupun DC. Op-amp dirancang untuk melaksanakan tugas-tugas matematis seperti pengurangan, penjumlahan, perkalian dan pembagian. Harganya yang murah, mudah diganti-ganti, dan sifatnya yang dapat di andalakan telah memperluas penggunaannya.

Op-amp mempunyai lima terminal dasar: dua untuk supply daya, dua untuk isyarat masukan, dan satu untuk keluaran.

Gambar 2.6 merupakan simbol skema op-amp mempunyai dua input Input membalik (inverting) atau (-) dan input tak membalik (non inverting) atau (+). Mempunyai satu output. Op-amp umumnya diberi daya oleh catu daya berpolaritas kembar, biasanya dalam daerah ± 5 hingga ± 15 volt. Namun dalam praktek jalur hubungan catu daya biasanya dihilangkan. Hubungan daya mudah dipahami, hubungan-hubungan kaki lainnya belum tentu terpakai semuanya.



Gambar 2.8 Simbol Skematis Op-Amp standart
Sumber : www.elektronika.com



Gambar 2.9 Skematic Diagram Op-Amp 741
Sumber : www.elektronika.com

Tipe op-amp atau nomor produk berada ditengah-tengah segitiga. Idealnya penguatan op-amp adalah tak berhingga, namun kenyataan penguatan op-amp hanya mencapai kurang lebih 200.000 dalam modus lup terbuka. Dalam keadaan demikian tidak ada umpan balik dari keluaran menuju masukan. Dalam rangkaian praktisnya, ada perbedaan tegangan sedikit saja pada masukan-masukannya akan menyebabkan tegangan keluaran berayun menuju tegangan maksimum catu.

Tegangan maksimum keluaran lebih 90% tegangan catu, karena ada tegangan jatuh internal pada op-amp. Keluaran dikatakan barada dalam keadaan saturasi (jenuh), dan dapat dinyatakan (salah satu) sebagai $+V_{sat}$ atau $-V_{sat}$. Sebagai contoh, rangkaian op-amp dalam modus lup terbuka dengan catu $\pm$ 15V akan menghasilkan ayunan keluaran antara –13,5V sampai +13,5V. Dengan tipe rangkaian seperti ini op-amp akan tidak stabil, keluaran akan 0 volt untuk selisih masukan 0 volt juga, tapi bila ada sedikit beda tegangan pada masukan-masukannya, maka keluaran akan berada pada salah satu dari kedua level tegangan diatas. Modus lup terbuka terutama dijumpai pada rangkaian pembanding tegangan.

Keserbagunaan op-amp dibuktikan dalam penerapannya pada berbagai tipe rangkain dalam modus lup tertutup. Komponen-komponen luar di gunakan untuk memberikan umpan balik keluaran pada masukan pembalik.

Penguatan lup tertutup dapat dikendalikan pada suatu nilai tertentu dalam rangkaian praktis. Perbandingan resistansi R_f terhadap R_{in} menentukan penguatan rangkaian-rangkaian.

Bila R_f dan R_m sama besar, maka penguatan sama dengan satu. Hubungan langsung dari keluaran menuju masukan juga menghasilkan penguatan satu.

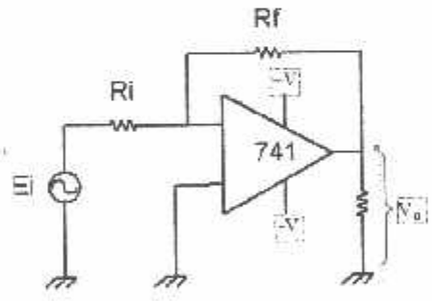
2.5.1 *Inferting Amplifier* (Penguat membalik)

Pada gambar 2.7 adalah merupakan op-amp yang terangkai sebagai penguat inverting. Sinyal input disuapkan ke input inverting (-) op-amp melalui tahanan R_i yang disebut elemen input. Tahanan R_f merupakan elemen umpan balik. Tegangan antara input (+) dan (-) pada dasarnya sama dengan 0V. Penurunan tegangan melalui R_i adalah E_i. Arus I yang mengalir melalui R_i adalah $I = \frac{E_i}{R_i}$

Seluruh masukan I mengalir melalui R_f, disebabkan jumlah yang dialirkan oleh terminal masukan (-) nya dapat diabaikan. Arus yang melalui R_f ditentukan oleh R_i dan E_i, dan bukan oleh R_f V_f atau op-ampnya.

Penurunan tegangan yang melalui R_f adalah

$$V_{Rf} = I \times R_f = \frac{E_i}{R_i} R_f$$



Gambar 2.10 Penguat *inverting*
Sumber : www.elektronika.com

Satu ujung R_f dan satu ujung R_L beban telah dihubungkan. Tegangan dari hubungan tersebut ke ground adalah V_0. ujung R_f dan R_L yang lain berada pada posisi ground. Karena itu, V_0 menyamai V_{Rf} dan menambah tanda minus.

Sehingga akan didapat :

$$V_0 = E_i \frac{R_f}{R_I}$$

Gain untaian tertutup dari penguat tersebut sebagai A_{cL}. adalah

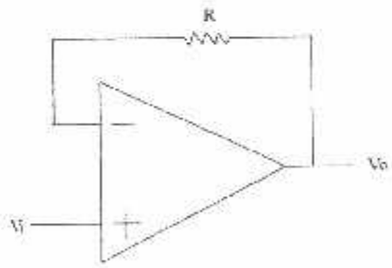
$$A_{cL} = \frac{V_0}{E_i} = \frac{R_f}{R_i}$$

Tanda minus menandakan bahwa polaritas keluaran V_0 terbalik terhadap input

E_i. Olch karenanya rangkaian tersebut dinamakan rangkaian pembalik.

2.5.2 *Buffer*

Rangkaian buffer adalah rangkaian yang inputnya sama dengan hasil outputnya. Dalam hal ini seperti rangkaian common colektor yaitu berpenguatan = 1. Rangkaiannya seperti pada gambar 2.8

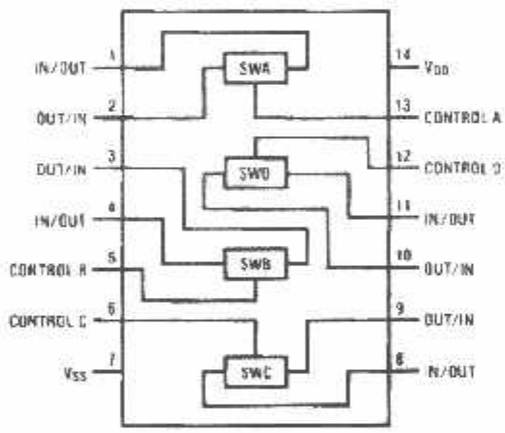


Gambar 2.11 Rangkaian Buffer
Sumber : Rangkaian Op-Amp.pdf

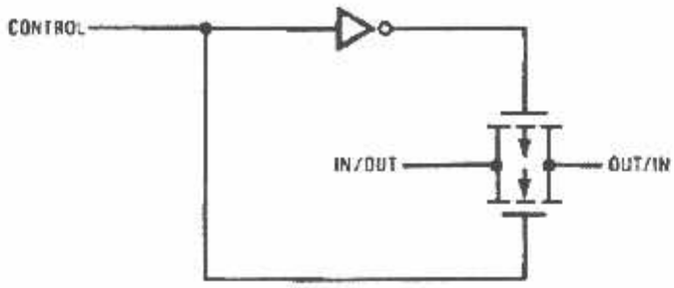
Nilai R yang terpasang gunanya untuk membatasi arus yang di keluarkan. Besar nilainya tergantung dari indikasi dari komponennya, biasanya tidak dipasang alias arus dimaksimalkan sesuai dengan kemampuan op-ampnya.

2.6 CD 4016

Type series CD4016 adalah *switch* yang di gunakan untuk transmisi atau *multiplexing* dari sinyal digital atau analog. Di dalam IC tersebut terdapat 4 switch yang mana masing-masing switch terdiri satu masukan dan satu keluaran yang mempunyai satu pengontrol masuk yang secara serempak menyimpangkan kedua-duanya 0 dan 1. Kedua kondisi tersebut di dalam switch dinyatakan dengan " ON " atau " OFF ".



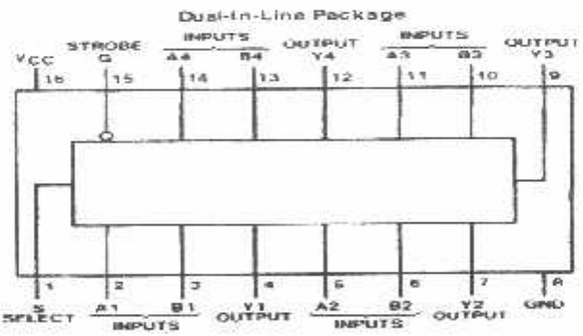
Gambar 2.12 Konfigurasi Pin CD 4016
Sumber : www.datasheet.com



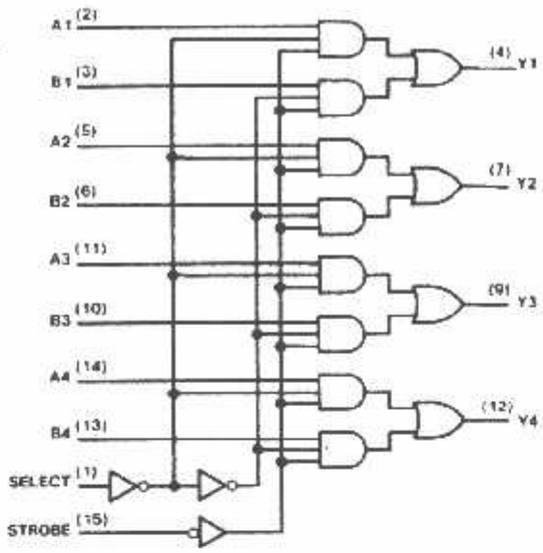
Gambar 2.13 Skematik Diagram IC CD 4016BC
Sumber : www.datasheet.com

2.7 *Multiplexer* IC 74LS157

IC 74LS157 adalah IC *multiplexer* yang mempunyai 8bit inputan dan 8bit outputan. Keluaran 8bit tersebut di bagi per 4bit – 4bit. Pada outputan multiplexer ini dikontrol oleh satu pengontrol yang jika saat diberi logika h*igh* maka outputan 4bit pertama atau 4bit nilai rendah (LSB) yang akan dikeluarkan. Jika diberi logika *high* berikutnya maka 4bit kedua atau 4bit MSB yang akan dikeluarkan.



Gambar 2.14 konfigurasi IC 74ls157
Sumber : www.datasheet.com



Gambar 2.15 Diagram Logic dari IC 74ls157
Sumber : www.datasheet.com

Pin 2,5,11,14 sebagai inputan 4 bit LSB.

Pin 3,6,10,13 sebagai input 4 bit MSB.

Pin 1 sebagai pengontrol keluaran data 4bit.

Pin 15 sebagai *strobe Ground.*

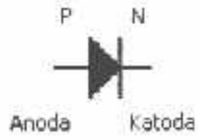
Pin 4,7,9,12 sebagai outputan 4 bit.

Pin 8 sebagai *ground.*

Pin 16 sebagai Vcc.

2.8 Dioda

Dioda merupakan salah satu komponen elektronika yang termasuk komponen aktif. Dibawah ini merupakan gambar yang melambangkan dioda penyearah.



Gambar 2.16 Simbol Dioda

Sisi P disebut Anoda dan sisi N disebut Katoda. Lambang dioda seperti anak panah yang arahnya dari sisi P ke sisi N. Karenanya ini mengingatkan kita pada arus konvensional mudah mengalir dari sisi P ke sisi N.

Dalam pendekatan dioda ideal, dioda dianggap sebagai sebuah saklar tertutup jika diberi bias forward dan sebagai saklar terbuka jika diberi bias reverse. Artinya secara ideal, dioda berlaku seperti konduktor sempurna (tegangan nol) jika dibias forward dan seperti isolator sempurna (arus nol) saat dibias reverse.

Untuk pendekatan kedua, dibutuhkan tegangan sebesar 0,7 V sebelum dioda silikon konduksi dengan baik. Dioda dapat digambarkan sebagai suatu saklar yang diseri dengan tegangan penghambat 0,7 V. Apabila tegangan sumber lebih besar dari 0,7 V maka saklar akan tertutup. Sebaliknya apabila tegangan sumber lebih kecil dari 0,7 V maka saklar akan terbuka.

BAB III
PERANCANGAN DAN PEMBUATAN ALAT

3.1. Pendahuluan

Pada bab ini akan dibahas perancangan dan pembuatan alat. Pembahasan akan dilakukan pada setiap blok rangkaian, cara kerja masing-masing blok rangkaian, perhitungan dan fungsi masing-masing blok rangkaian tersebut. Secara garis besar terdapat dua bagian perangkat yang ada yaitu :

- Perancangan perangkat keras *(Hardware).*
- Perancangan perangkat lunak *(Software).*

Pada perancangan perangkat keras akan meliputi seluruh blok rangkaian yang digunakan pada sistem ini. Pada perancangan perangkat lunak akan meliputi diagram alir dan *software* secara umum. Akan tetapi kedua perangkat ini dalam kerjanya akan saling menunjang satu sama lain.

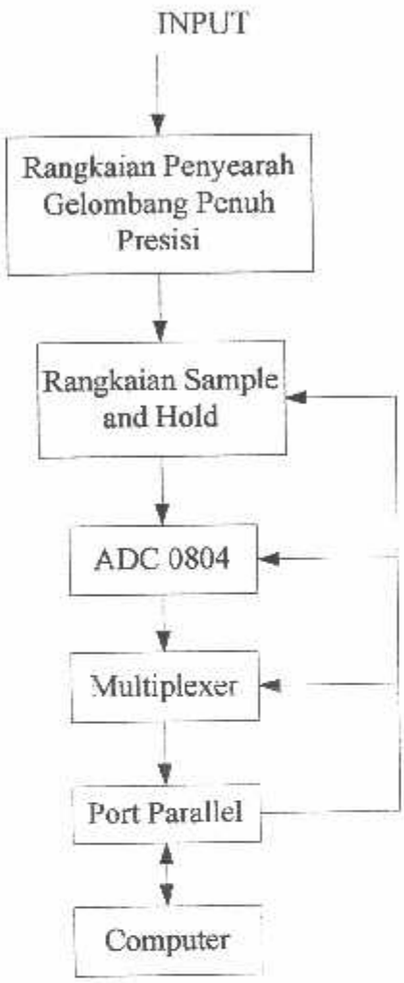
Pada perangkat keras sendiri terdiri dari beberapa rangkaian antara lain. rangkaian penyearah gelombang penuh presisi, rangkaian *sample and hold*, rangkaian *Analog to Digital Converter* (ADC), *Multiplexer*, dan *parallel interface*. Pada perancangan perangkat lunak akan meliputi diagram alir dan *software* secara umum.

3.2. Perancangan Perangkat Keras

Perancangan perangkat keras yang direncanakan meliputi, blok diagram kesceluruhan dan prinsip kerja alat, pembuatan skema seluruh rangkaian yang

direncanakan, penghitungan nilai komponen yang digunakan, dan perakitan seluruh komponen.

3.2.1 Blok Diagram



Gambar 3.1 Diagram Blok Sistem

Fungsi masing – masing diagram blok :

- **Rangkaian Penyearah Presisi Gelombang Penuh**

  Berfungsi untuk menyearahkan sinyal dan tegangan dibawah batas tegangan dioda.

- **Rangkaian *Sample and Hold***

  Berfungsi sebagai switch transmisi sinyal analog dan digital.

- **ADC 0804**

  Berfungsi sebagai pengubah nilai – nilai analog ke nilai – nilai digital.

- ***Multiplexer* 74LS157**

  Berfungsi sebagai outputan 8 bit yang di interface kan kekomputer secara 4bit – 4bit.

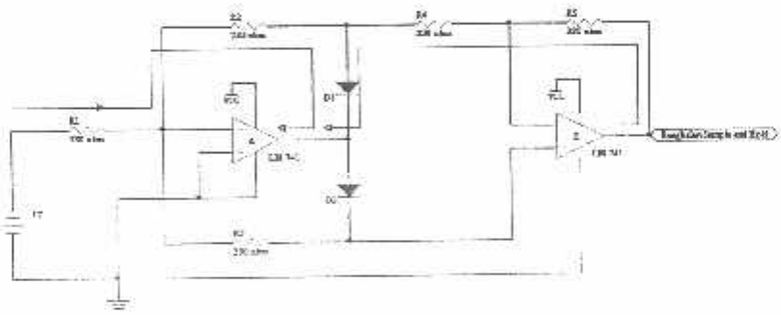
3.2.2. Prinsip Kerja Hardware

Tegangan 0 – 5 volt dilewatkan rangkaian penyearah gelombang penuh presisi dimaksudkan agar tegangan dibawah 0,6 volt dapat disearahkan oleh dioda. Untuk mengkonversi nilai analog, ADC membutuhkan tegangan yang stabil dan beberapa waktu yang ditentukan, maka digunakan rangkaian *sample and hold*. Rangkaian ini akan menyampling masukan analog dan melakukan hold konstan sampai masukan berikutnya. Rangkaian ini akan melakukan hold sampling pada kapasitor berkualitas tinggi, yang di *buffer* oleh sebuah penguat operasional.

ADC akan memulai pengkonversian setelah pin WR diberi pulsa high. Setelah pengkonversian selesai, pin INTR yang sering disebut juga EOC (End Of Conversion) akan mengeuarkan pulsa aktif sehingga bias menjadi pemicu bagi pin RD untuk memulai membaca hasil konversi. Pin RD akan memulai membaca hasil konversi setelah diberi pulsa high.

Ic multiplexer akan menerima inputan 8 bit dari ADC yang kemudian di interface kan melalui parallel port ke komputer. Data 8 bit tersebut akan di interface kan 4bit – 4bit secara bergantian dengan dikontrol melalui pin select. Program Delphi akan membaca nilai 4bit pertama sebagai nilai bit LSB (Least Significant Bit). Kemudian membaca data 4bit selanjutnya sebagai nilai bit MSB (Most Significant Bit). Kemudian lewat software pergantian data 4bit tadi akan di rekonturksi ulang menjadi 8 bit kembali.

3.2.3. Rangkaian Penyearah Gelombang Penuh Presisi



Gambar 3.2 Rangkaian Penyearah Gelombang Penuh Presisi

Rangkaian ini mempergunakan tahanan – tahanan yang sama dan mempunyai resistansi masukan yang sama. Adapun komponen lain yang digunakan adalah 2 buah diode dan 2 buah Op – Amp. Gambar 3.3 memperlihatkan arah arus dan polaritas tegangan untuk isyarat – isyarat masukan positif. Diode 1 dialiri sedemikian rupa schingga dua *op-amp* A dan B bekerja sbagai pembalik dan Vo – $+E_1$. Tahanan – tahanan pada rangkaian ini ditetapkan sebesar 330 ohm dan menggunakan diode 1A.

Pada gambar terlihat arah arus melewati R_1. Dengan menggunakan rumus hukum ohm maka :

$$I = \frac{E1}{R1} \quad \text{..... (3.1)}$$

$$= \frac{5\ volt}{330} = 15\ \text{mA}$$

Setelah melewati R_1 kemudian menuju kc R_2. Arus yang melalui R_2 ditentukan oleh R_1 dan E_1, sehingga penurunan tegangan yang melalui R_2 adalah :

$$V_{R2} = I \times R_2 = \frac{E1}{R1} \times R_2 \quad \text{..... (3.2)}$$

$V_{R2} = 15 \times 330 = 49{,}5$ volt

Untuk outputan (Vo) dari penguat inverting dapat dihitung dengan rumus :

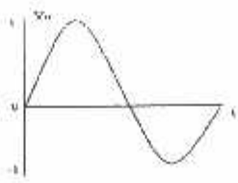
$$Vo = E_1 \frac{R_2}{R_1} \quad \text{..... (3.4)}$$

$$= 5 \frac{330}{330}$$

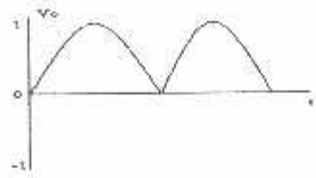
$= -5$ volt

Jadi Vi sama dengan Vo yaitu 1 volt. Tanda minus menandakan bahwa polaritas keluaran V_0 terbalik terhadap input.

Pada rangkaian terdapat 2 buah dioda yang berfungsi sebagai penyearah. Berikut adalah gambar bentuk gelombang yang telah disearahkan.



A

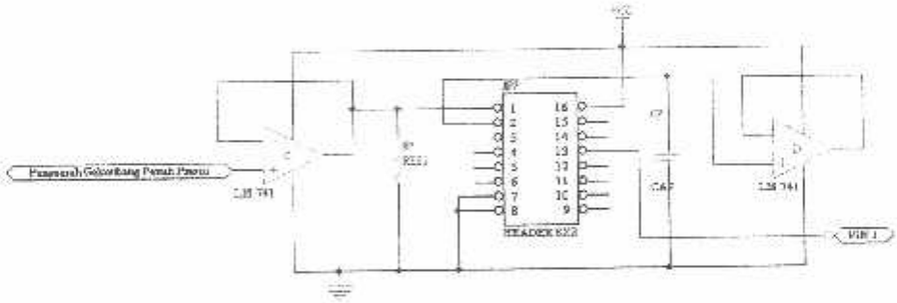


B

Gambar A menunjukkan gelombang yang belum disearahkan atau gelombang inputnya dan gambar B merupakan gelombang yang telah disearahkan oleh penyearah gelombang penuh.

3.3.3 Rangkaian Sample and Hold

Rangkaian ini terdiri dari 2 op – amp LM 741 yang berfungsi sebagai buffer dan IC CD 4016 yang digunakan mensample and hold sinyal. Gambar 3.4 merupakan rangkaian sample and hold.

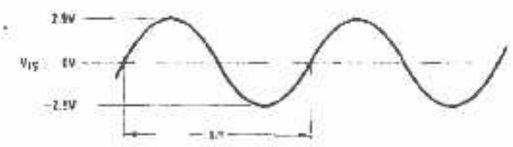


Gambar 3.3 Rangkaian Sample and Hold

IC CD 4016 merupakan *Quad Bilateral Switch* (4 tombol saklar) yang masing – masing saklar mempunyai satu pengontrol. Kelebihan IC ini adalah dapat

mensampling sinyal analog dan melakukan hold konstan sampai proses penyamplingan berikutnya.

Berikut adalah bentuk gelombang yang disampling



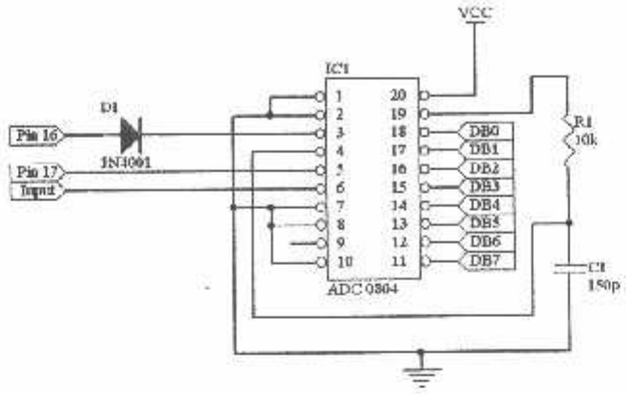
Gambar 3.4 hasil penyamplingan

3.3.4 Rangkaian *Analog to Digital Converter* (ADC) 0804

ADC 0804 menggunakan Vcc = +5 Volt sebagai tegangan referensi. Dalam hal ini jangkauan masukan analog mulai dari 0 Volt sampai 5 Volt (skala penuh), karena IC ini adalah SAC 8-bit, resolusinya akan sama dengan

$$\text{Resolusi} = \left(\frac{\text{tegangan skala penuh}}{2^n - 1}\right) = \frac{5\ \text{Volt}}{255} = 19{,}6\ \text{mVolt}$$

(n menyatakan jumlah bit keluaran biner IC *analog to digital converter*)



Gambar 3.5 Rangkaian ADC 0804

Nilai high untuk keluaran ADC 8 bit adalah 11111111 atau hexanya adalah FF atau sama dengan 255 byte. 1 bit berarti 255 / 8. Untuk mengetahui nilai digital saat tegangan 1,2,3,4, dan 5 volt dapat menggunakan perhitungan sebagai berikut :

Tegangan referensi : 5

255 / 5 = 51

- Untuk tegangan 1 volt : 51 x 1 = 51

  Binernya = 00110011

  Hexanya = 33

- Untuk tegangan 2 volt : 51 x 2 = 102

  Binernya = 01100110

  Hexanya = 66

- Untuk tegangan 3 volt : 51 x 3 = 153

  Binernya = 10011001

  Hexanya = 99

- Untuk tegangan 4 volt : 51 x 4 = 204

  Binernya – 11001100

  Hexanya = CC

- Untuk tegangan 5 volt : 51 x 5 = 255

  Binernya = 11111111

  Hexanya = FF

Berikut ini adalah tabel biner dan hexa untuk data 4 bit.

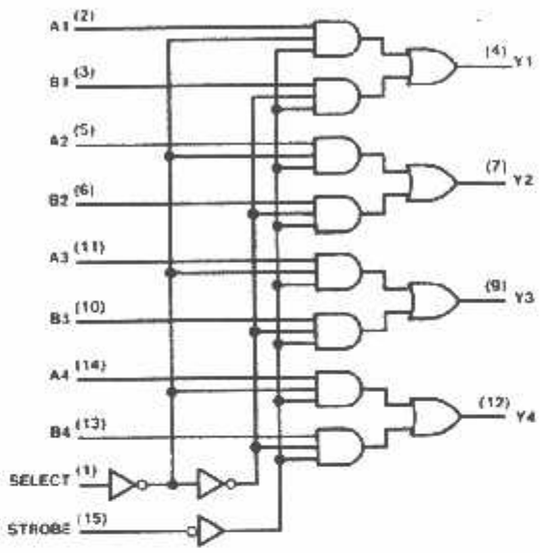
Table 3-1 Tabel Kebenaran

Decimal	Biner	hexa
1	0001	1
2	0010	2
3	0011	3
4	0100	4
5	0101	5
6	0110	6
7	0111	7
8	1000	8
9	1001	9
10	1010	A
11	1011	B
12	1100	C
13	1101	D
14	1110	E
15	1111	F

3.3.5 Rangkaian Multiplexer

Prinsip kerja dari rangkaian ini adalah saat pin 1 (strobe) diberi kondisi *high* maka IC akan mengambil data melalui pin 2(A1), 5(A2), 11(A3) dan 14(A4). Pada

saat pin 1 diberi kondisi high kembali maka IC akan mengambil data yang terdapat pada pin 3(B1), 5(B2), 10(B3) dan 13(B4). Untuk pengiriman datanya per 4 bit. Kemudian dengan software data 4bit – 4bit tersebut di kontruksi ulang menjadi 8bit.



Gambar 3.6 Diagram Logic dari IC 74LS157

BAB IV

PENGUJIAN ALAT

Tujuan pengujian alat ini adalah untuk menentukan apakah alat yang telah dibuat berfungsi dengan baik dan sesuai dengan perancangan. Pengujian dilakukan dengan cara menguji rangkaian setiap blok secara terpisah. Pengujian setiap blok ini dilakukan untuk mempermudah analisis apabila alat ini tidak bekerja sesuai dengan perancangan.

Dalam pelaksanaan pengujian dilakukan dengan dua cara yaitu secara perangkat keras dan perangkat lunak. Secara perangkat keras dilakukan melalui pemeriksaan sambungan pengawatan dan pengukuran dengan alat ukur. Sedangkan pengujian perangkat lunak, pengujian dilakukan melalui pembuatan *software* dan hasilnya diamati pada computer. Pengujian ini dibagi menjadi:

1. Pengujian Rangkaian Penyearah Gelombang Penuh Presisi.
2. Pengujian Rangkaian ADC 0804.
3. Pengujian Keseluruhan.

4.1 Pengujian Rangkaian Penyearah Gelombang Penuh Presisi.

4.1.1 Tujuan

Untuk mengetahui sinyal saat tegangan diatas dan dibawah batas tegangan diode dan untuk mengetahui apakah Op – Amp dapat bekerja dengan baik.

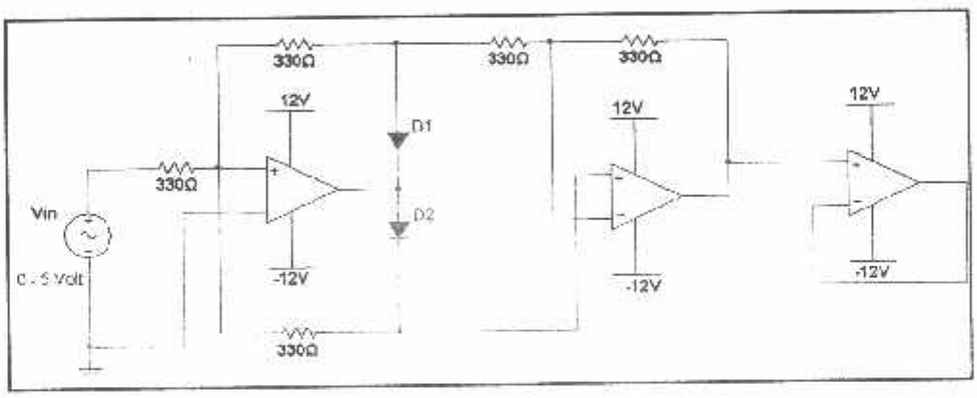
4.1.2 Peralatan yang digunakan

1. Rangkaian Penyearah Penyearah Gelombang Penuh Presisi.
2. Osiloskop.
3. Multimeter Digital.
4. Tegangan AC 0 – 5 volt.

4.1.3 Prosedure Pengujian

Langkah – langkah pengujian adalah sebagai berikut :

1. Merangkai rangkaian penyearah gelombang penuh presisi seperti pada gambar 4.1.

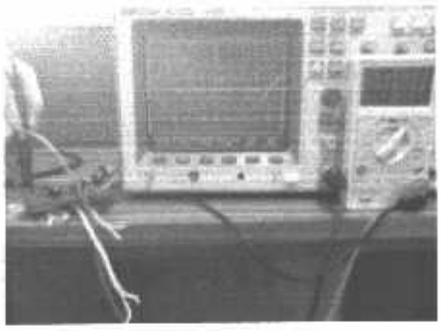


Gambar 4.1 Rangkaian Penyearah Gelombang Penuh Presisi

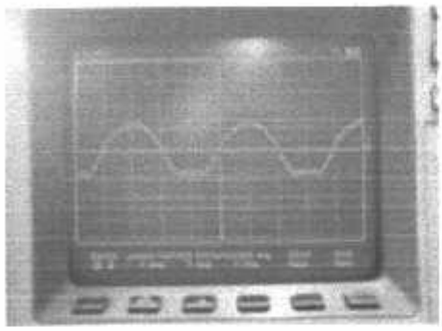
2. Memberikan Inputan sebesar 0 – 5 volt.
3. Menghubungkan multimeter dan osiloskop pada tegangan inputan, rangkaian penguat inverting dan rangkaian buffer secara bergantian guna mengetahui tegangan yang akan diukur dan mengetahui bagaimana bentuk gelombangnya.
4. Hasil pengujian terdapat pada multimeter digital dan osiloskop.

4.1.4 Hasil Pengujian

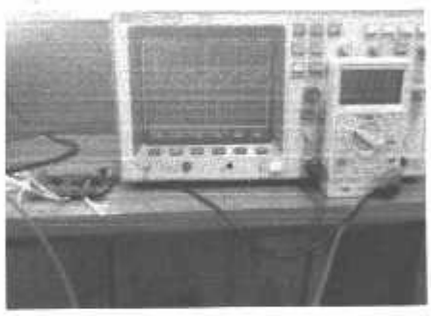
Gambar 4.2 merupakan hasil pengujian untuk tegangan input 4 volt



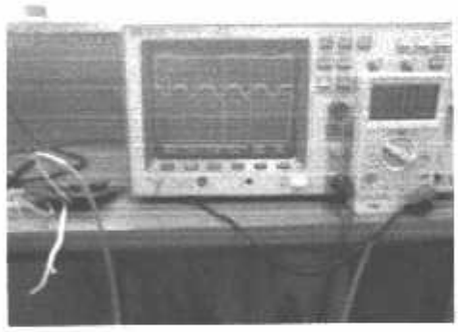
Gambar 4.2a Hasil dari Pengukuran Tegangan Input



Gambar 4.2b Hasil dari Pengukuran Rangkaian Inverting ke-1

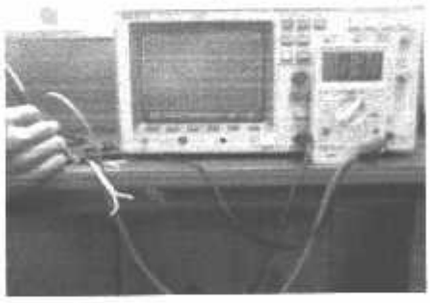


Gambar 4.2c Hasil dari Pengukuran Rangkaian Inverting ke-2

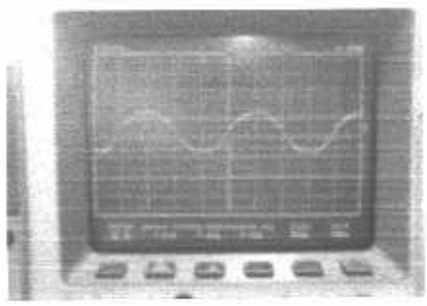


Gambar 4.2d Hasil dari Pengukuran Rangkaian Buffer

Gambar 4.3 merupakan hasil pengujian untuk tegangan input 3 volt

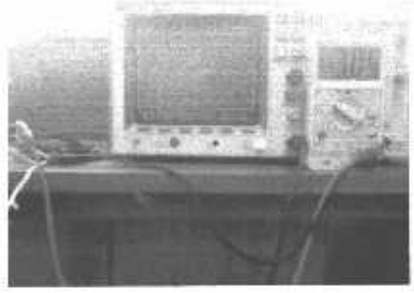


Gambar 4.3a Hasil dari Pengukuran Tegangan Input



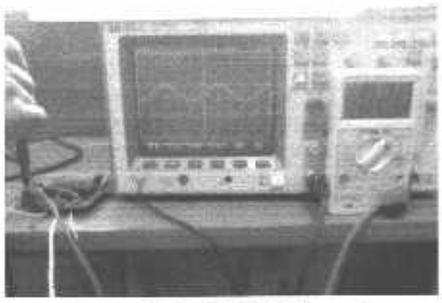
Gambar 4.3b Hasil dari Pengukuran Rangkaian Inverting ke-1

Gambar 4.3c Hasil dari Pengukuran Rangkaian Inverting ke-2

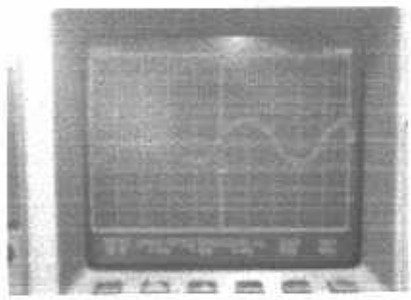


Gambar 4.4 Hasil dariPengukuran Rangkaian Buffer

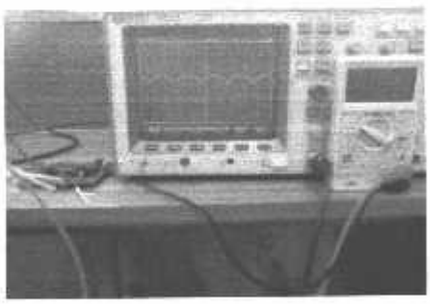
Gambar 4.4 merupakan hasil pengujian untuk tegangan input 2 volt



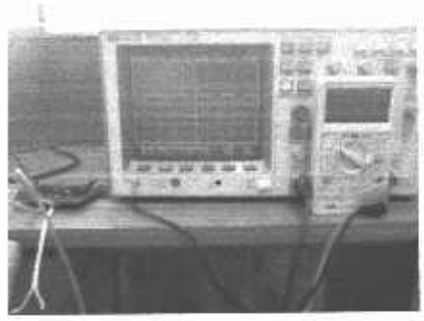
Gambar 4.4a Hasil dari Pengukuran Tegangan Input



Gambar 4.4b Hasi dari pengukuran Rangkaian Inverting ke-1



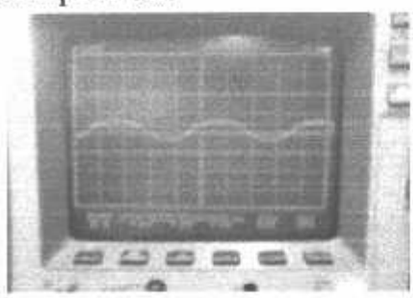
Gambar 4.4c Hasil dari pengukuran Rangkaian Inverting ke-2



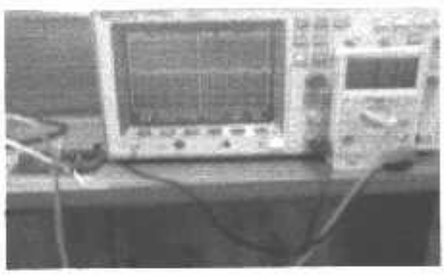
Gambar 4.4d Hasil dari Pengukuran Rangkaian Buffer

Gambar 4.5 merupakan hasil pengujian untuk tegangan input 1 volt

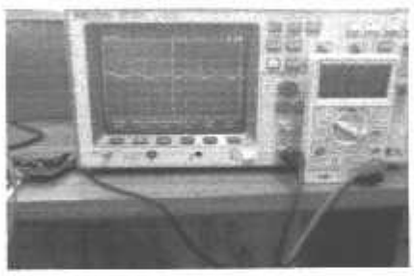
Gambar 4.5a Hasil dari pengukuran Tegangan Input



Gambar 4.5b Hasil dari Pengukuran Rangkaian Inverting ke-1



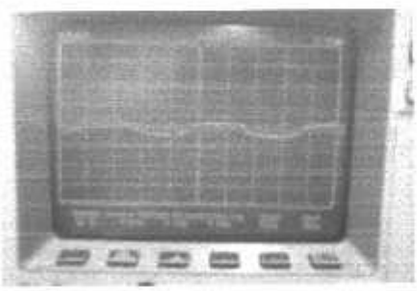
Gambar 4.5c Hasil dari Pengukuran Rangkaian Inverting ke-2



Gambar 4.5d Hasil dari Pengukuran Rangkaian Buffer

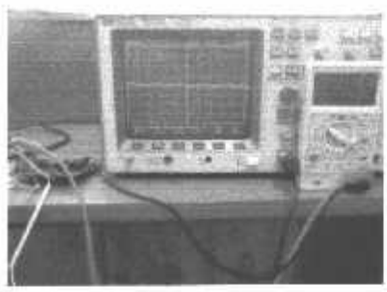
Gambar 4.6 merupakan hasil pengujian untuk tegangan input 0,5 volt

Gambar 4.6a Hasil dari Pengukuran Tegangan Input



Gambar 4.6b Hasil dari Pengukuran Rangkaian Inverting ke-1

Gambar 4.6c Hasil dari Pengukuran Rangkaian Inverting ke-2



Gambar 4.6d Hasil dari Pengukuran Rangkaian Buffer

Table 4-1 Hasil Pengujian Rangkaian Penyearah Gelombang Penuh Presisi

NO.	Tegangan Input	Vout Inverting ke-1		Vout Inverting ke-2		Vout Buffer		Error %
		Pengukuran	Perhitungan	Pengukuran	Perhitungan	Pengukuran	Perhitungan	
1.	5 volt	4,00 volt	4,95 volt	4,50 volt	4,80 volt	4,48 volt	4,80 volt	8,6 %
2.	4 volt	3,33 volt	3,96 volt	3,90 volt	3,66 volt	3,89 volt	3,89 volt	7,6 %
3.	3 volt	2,60 volt	2,97 volt	3,00 volt	3,02 volt	3,00 volt	3,00 volt	4,3 %
4.	2 volt	1,90 volt	1,89 volt	2,09 volt	2,40 volt	2,09 volt	2,09 volt	2,1 %
5.	1 volt	1,20 volt	0,99 volt	1,18 volt	1,28 volt	1,18 volt	1,18 volt	1,2 %
6.	0,4 volt	0,80 volt	0,39 volt	0.63 volt	0,71 volt	0.63 volt	0,63 volt	1,5 %

Berikut Perhitungannya :

- Vout perhitungan pada rangkaian inverting ke-1 untuk tegangan 5 volt :

$$I = \frac{}{}$$

$$= \frac{}{} = 15 \text{ mA}$$

$$Vo = I \times R_2 = 0.012 \times 330 = 4.95 \text{ volt}$$

➢ Persentase Error :

$$\% \text{ Error} = \frac{Data\ Pengujian - Data\ Perhitungan}{Data\ Perhitungan} \ x\ 100\%$$

$$\% \text{ Error} = \frac{4,90 - 4,95}{4,95} \ x\ 100\% = 19\ \%$$

➢ Vout perhitungan pada rangkaian inverting ke-2:

Pada perhitungan rangkaian inverting yang ke-2 menggunakan rumus differencial dikarenakan inputan (+) dan (-) sama – sama mendapatkan inputan. Maka digunakan rumus :

$$\text{Vout} = \frac{R2}{R1}(v2 - v1)$$

$$= \frac{330}{330}(1,90 - (-1,90))$$

$$= 1 + (3,8) = 4,80 \text{ volt}$$

➢ Persentase Error :

$$\% \text{ Error} = \frac{Data\ Pengujian - Data\ Perhitungan}{Data\ Perhitungan} \ x\ 100\%$$

$$\% \text{ Error} = \frac{4,50 - 4,80}{4,80} \ x\ 100\% \ -6,2\ \%$$

➢ Vout pada rangkaian buffer :

Vout = Vin

4,80 = 4,80 volt

➢ Persentase Error :

$$\% \text{ Error} = \frac{Data\ Pengujian - Data\ Perhitungan}{Data\ Perhitungan} \ x\ 100\%$$

$$\% \text{ Error} = \frac{4{,}40 \;\; 4{,}00}{4{,}80} \; x \; 100\% \; = 0{,}8\,\%$$

4.1.4 Analisa Hasil Pengujian Rangkaian Penyearah Gelombang Penuh Presisi

Dari hasil pangujian diatas didapatkan error yang besar dikarenakan berbagai kemungkinan antara lain komponen – komponen yang digunakan. Pada bentuk sinyal tidak sempurna dikarenakan keluaran LM 741 yang tidak dapat mengeluarkan bentuk sinyal yang sempurna.

4.1.5 Kesimpulan

Dari pengujian diatas dapat diambil kesimpulan antara lain :

1. Pemrosesan sinyal dapat dihasilkan pada frekuensi antara 20 hz – 1Khz.
2. Tegangan 0,1 volt – 0,6 volt atau dibawah tegangan dioda dapat diproses pembentukan sinyalnya.

4.2 Pengujian ADC 0804

4.2.1 Tujuan

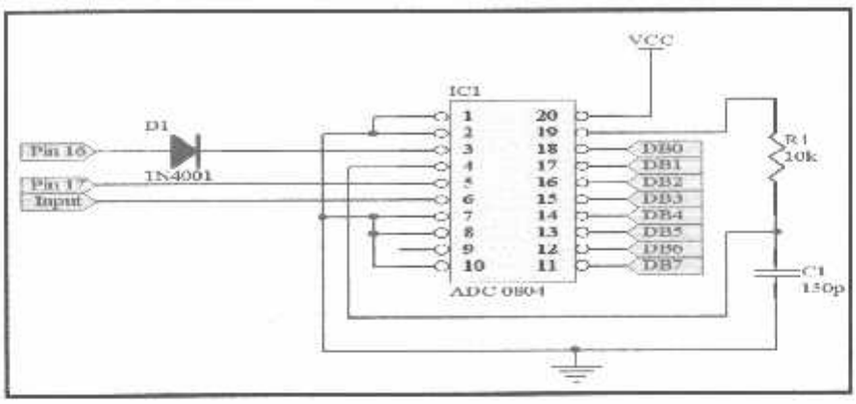
Untuk mengetahui apakah ADC 0804 yang digunakan dapat bekerja dengan baik atau tidak dan untuk mengetahui hasilnya berupa tampilan LED.

4.2.2 Peralatan yang digunakan

1. Rangkaian ADC 0804.
2. 8 buah Led.
3. Multimeter Digital.

4.2.3 Prosedure Pengujian

1. Merangkai rangkaian ADC 0804 seperti pada gambar

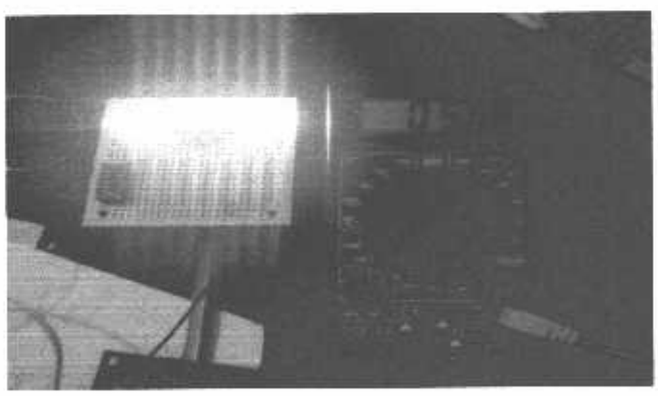


Gambar 4.7 rangkaian ADC 0804

2. Menghubungkan inputan dc pada pin 6 sebagai inputan.
3. Pengujian menggunkan tegangan 5 volt untuk inputannya.

4.2.4 Hasil Pengujian

Gambar 4.8 adalah hasil dari pengujian ADC 0804 untuk tegangan 5 volt



Gambar 4.8 Hasil Pengujian ADC 0804 menggunakan 8 buah LED

Perhitungan tegangan analog ke digital :

Tegangan referensi : 5

255 / 5 = 51

Tegangan inputan sebesar 5 volt :

51 x 5 = 255

Binernya = 11111111 (nyala semua)

Hexanya = FF

4.2.5 Analisa Hasil Pengujian Rangkaian ADC 0804

Pada pengujian rangkaian ADC 0804 data analog yang di inputkan sebesar 5 volt dapat di konversi dengan baik sehingga nilai biner dan hexa-nya sesuai pada table kebenaran yaitu 11111111 atau FF.

4.2.6 Kesimpulan

1. ADC 0804 hanya dapat membaca atau mengkonversi tegangan analog sebesar 5 volt.
2. Nilai tegangan di atas 5 volt di anggap sebagai tegangan 5 volt.

4.3 Pengujian Keseluruhan

4.3.1 Tujuan

Pengujian keseluruhan bertujuan untuk mengetahui apakah alat keseluruhan dapat di aplikasikan ke computer.

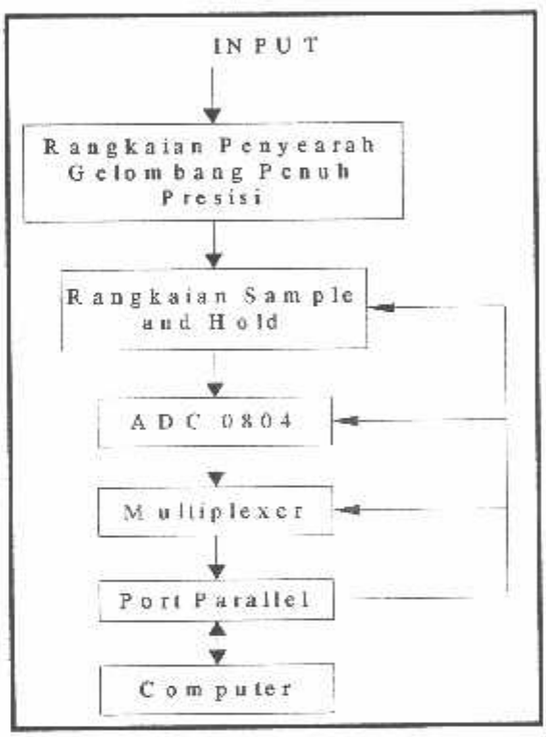
4.3.2 Peralatan yang di gunakan

1. Rangkaian Penyearah Gelombang Penuh Presisi.

2. Rangkaian Sample and Hold.
3. Rangkaian ADC 0804.
4. Rangkaian Multiplexer.
5. Multimeter
6. Computer

4.3.3 Prosedure Pengujian

1. Merangkai blok pengujian alat seperti pada gambar 4.9 berikut:

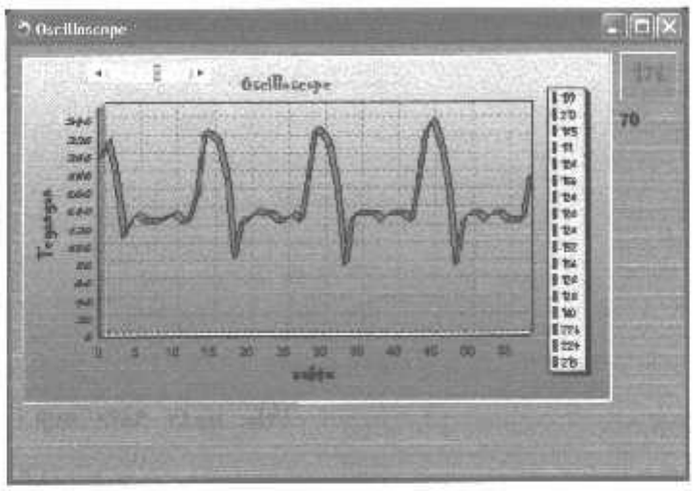


Gambar 4.9 Rangkaian blok keseluruhan

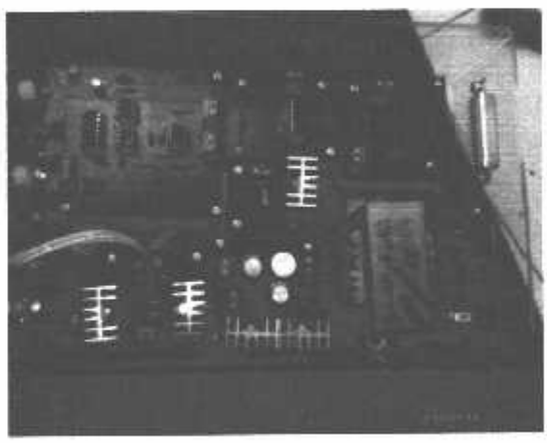
2. Memberikan suplay tegangan 0 – 5 volt sebagai inputannya
3. Menjalankan program di computer.

4. Tekan tombol RUN untuk menjalankan.
5. Tampilan hasil terdapat pada computer.

Berikut adalah hasil tampilan pada computer :



Gambar 4.10 hasil pengujian pada komputer



Gambar 4.11 Kesceluruhan Alat

4.3.4 Kesimpulan Hasil Pengujian Alat Keseluruhan

Dari hasil pengujian diatas bentuk gelombang yang ditampilan pada computer berbeda dengan percobaan yang dilakukan menggunakan osiloskop biasanya. Besarnya error yang terdapat pada rangkaian penyearah gelombang penuh presisi dapat mempengaruhi hasil pada pengujian alat dan noise – noise yang timbul dari berbagai keadaan seperti noise dari rangkaian itu sendiri atau dari suara – suara dan dari computer yang digunakan.

BAB V

PENUTUP

5.1 Kesimpulan

Berdasarkan hasil pengujian dan analisis alat maka dapat ditarik kesimpulan sebagai berikut:

1. Untuk Rangkaian Penyearah Gelombang Penuh Presisi.
   - Rangkaian dapat memproses gelombang di bawah tegangan diode yaitu di bawah 0,6 volt.
   - Nilai outputan dengan inputan mempunyai error yang cukup besar.
   - Gelombang yang telah disearahkan mempunyai bentuk yang tidak cacat.
2. Untuk Rangkaian ADC 0804.
   - Hasil pengkonversian dari ADC sesuai dengan inputannya.
   - ADC 0804 hanya dapat mengkonversi nilai tegangan sebesar 0 – 5 volt
3. Untuk Keseluruhan Alat
   - Program yang di buat dapat menampilan outputan dari ADC 0804.
   - Hasil yang ditampilan ke computer kurang sesuai dengan yang di tampilan pada osiloskop sesungguhnya.
   - Noise – noise perbedaan tegangan input dan out put yang cukup jauh.

5.2 SARAN

Untuk pengembangan selanjutnya, penulis memberikan saran sebagai berikut :

1. Pemrosesan sinyal di butuhkan komponen yang baik agar hasil pada computer dapat terlihat dengan baik.
2. Outputan sinyal tidak hanya satu channel saja agar dapat melihat perbandingan sinyal antara inputan dengan outputan.
3. Pada program dapat digunakan komponen Delphi yang lebih baik agar dalam menampilkan sinyal tidak cacat.

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LAMPIRAN

INSTITUT TEKNOLOGI NASIONAL
FAKULTAS TEKNOLOGI INDUSTRI
JURUSAN TEKNIK ELEKTRO S-1
KONSENTRASI TEKNIK ELEKTRONIKA

FORMULIR PERBAIKAN SKRIPSI

Nam : Wanda Dwi Cahyadi

NIM : 04.12.275

Jurusan : Teknik Elektro S-1

Konsentrasi : Teknik Elektronika

Judul : PERENCANAAN DAN PEMBUATAN OSILOSKOP BERBASIS KOMPUTER

Hari / Tanggal Ujian Skripsi : Selasa / 06 Oktober 2009

No	Tanggal	Uraian	Paraf
1	06/10/2009	- Blok diagram - Perbandingan hasil program dengan osiloskop	

Disetujui,

Penguji I

(Joseph Dedy Irawan, ST, MT)
NIP. 132315178

Mengetahui,

Penguji II

(Sotyohadi, ST, MSc)
NIP.Y.1039700309

Mengetahui,

Dosen Pembimbing

(Irmalia S. Faradisa, ST. MT)
NIP.P. 1030000365

INSTITUT TEKNOLOGI NASIONAL
JL. RAYA KARANGLO, KM 2
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FORMULIR BIMBINGAN SKRIPSI

Nama : WANDA DWI CAHYADI
Nim : 04 12 275
Masa Bimbingan : 8 JUNI 2009 s/d 8 DESEMBER 2009
Judul Skripsi : PERENCANAAN DAN PEMBUATAN OSILOSKOP BERBASIS KOMPUTER

NO	TANGGAL	URAIAN	PARAF PEMBIMBING
1.	20/8 09	Revisi BAB I Cari teori tts osiloskop	
2.	3/9 09	Acc BAB I Revisi Bab II	
3.		BAB II → Dioda	
4.	4/9 09	Acc BAB II	
5.	5/9 09	Acc Smua hasil	
6.			
7.			
8.			
9.			
10.			

Malang,
Dosen Pembmbing.

IRMALIA SURYANI FARADISA, ST . MT
NIP. P. 1030000365

Form S-4 B

INSTITUT TEKNOLOGI NASIONAL MALANG
FAKULTAS TEKNOLOGI INDUSTRI
JURUSAN TEKNIK ELEKTRO

Formulir Perbaikan Ujian Skripsi

Dalam pelaksanaan Ujian Skripsi Jenjang Strata 1 Jurusan Teknik Elektro Konsentrasi T. Energi Listrik / T. Elektronika / T.Infokom, maka perlu adanya perbaikan skripsi untuk mahasiswa :

NAMA : WANDA OWI
NIM : 0412275
Perbaikan meliputi :

-) BLOK DIAGRAM
-) PENAMBAHAN HASIL PROGRAM dgn OSILOSCOPE

Malang, 200

( )

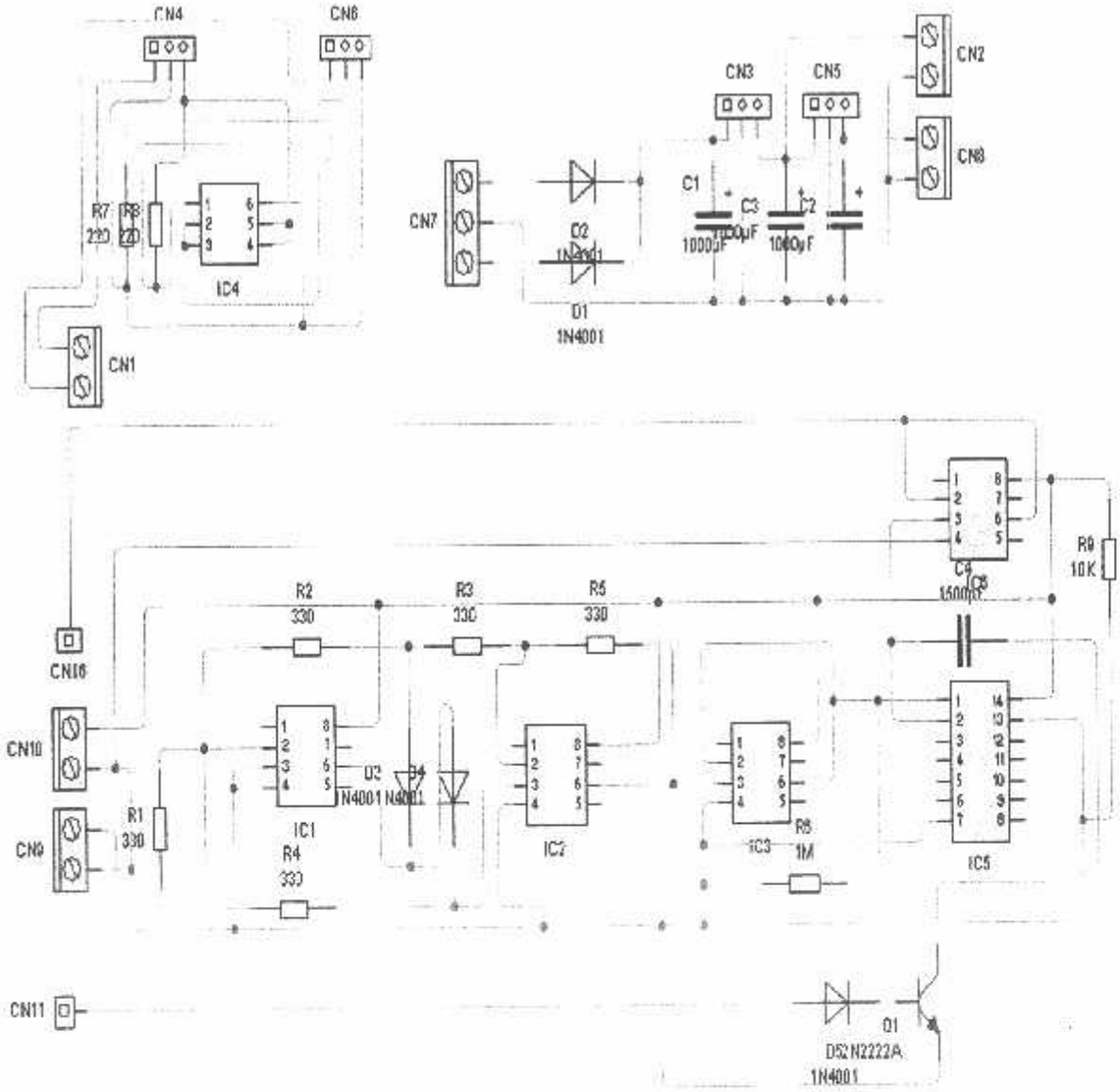
1

Listing program

```
unit Unit1;

interface

uses
  Windows, Messages, SysUtils, Variants, Classes, Graphics, Controls, Forms,
  Dialogs, ExtCtrls, TeEngine, Series, TeeProcs, Chart, SmallPort, StdCtrls,
  Buttons, SUIButton;

type
  TForm1 = class(TForm)
    Chart1: TChart;
    Series1: TLineSeries;
    Panel1: TPanel;
    SmallPort1: TSmallPort;
    suiImageButton1: TsuiImageButton;
    suiImageButton2: TsuiImageButton;
    suiImageButton3: TsuiImageButton;
    procedure pin2;
    procedure pin9;
    procedure pin16;
    procedure pin17;
    procedure Button1Click(Sender: TObject);
    procedure Button2Click(Sender: TObject);
    procedure FormCreate(Sender: TObject);
    procedure BitBtn1Click(Sender: TObject);
    procedure suiImageButton1Click(Sender: TObject);
    procedure suiImageButton2Click(Sender: TObject);
    procedure suiImageButton3Click(Sender: TObject);
  private
    { Private declarations }
  public
    { Public declarations }
  end;
 var
  Form1: TForm1;
  hasil,a,tampung:byte;
  i:integer;
  selesai:boolean;
const
  LPT_data    =$378;
  LPT_status =$379;
  LPT_kontrol=$37A;

implementation

{$R *.dfm}

procedure delay(lama:longint);
var
   ref : longint;
begin
   ref:=gettickcount;
   repeat
     application.ProcessMessages;
```

```
   until ((getTickCount - ref) >= lama)
end;

procedure TForm1.pin17;
begin
  tampung:=SmallPort1.ReadByte(lpt_kontrol);
  tampung:=tampung or $08;
  SmallPort1.WriteByte(lpt_kontrol,tampung);
end;

procedure TForm1.pin16;
begin
  tampung:=SmallPort1.ReadByte(lpt_kontrol);
  tampung:=tampung and $04;
  SmallPort1.WriteByte(lpt_kontrol,tampung);
end;

procedure TForm1.pin2;
begin
  tampung:=SmallPort1.ReadByte(LPT_data);
  tampung:=tampung and $01;
  SmallPort1.WriteByte(lpt_kontrol,tampung);
end;

procedure TForm1.pin9;
begin
  tampung:=SmallPort1.ReadByte(LPT_data);
  tampung:=tampung and $80;
  SmallPort1.WriteByte(lpt_kontrol,tampung);
end;

procedure TForm1.Button1Click(Sender: TObject);
begin
selesai:=false;
  series1.Clear;
  i:=0;
  repeat
   pin2;
   a:=smallport1.ReadByte(LPT_status) and $F0;
   a:=a shr 4;

   pin9;
   a:=a or (smallport1.ReadByte(LPT_status) and $F0);
   hasil:= a xor $88;
   panel1.Caption:=InttoStr(hasil);
   delay(200);

   with chart1 do
     with series1 do
       addxy(i,hasil,'',clblue);
   inc(i);
  until ((i=100) or (selesai=true));

end;

procedure TForm1.Button2Click(Sender: TObject);
begin
```

```
selesai:=true;
end;


procedure TForm1.FormCreate(Sender: TObject);
begin
close;
end;

procedure TForm1.BitBtn1Click(Sender: TObject);
begin
Close;
end;

procedure TForm1.suiImageButton1Click(Sender: TObject);
begin
selesai:=false;
  series1.Clear;
  i:=0;
  repeat
   pin2;
   a:=smallport1.ReadByte(LPT_status) and $F0;
   a:=a shr 4;

   pin9;
   a:=a or (smallport1.ReadByte(LPT_status) and $F0);
   hasil:= a xor $88;
   panel1.Caption:=InttoStr(hasil);
   delay(200);

   with chart1 do
     with series1 do
       addxy(i,hasil,'',clblue);
   inc(i);
  until ((i=100) or (selesai=true));

end;

procedure TForm1.suiImageButton2Click(Sender: TObject);
begin
 selesai:=true;
end;

procedure TForm1.suiImageButton3Click(Sender: TObject);
begin
close;
end;

end.
```


CN4
CN6
CN3
CN5
CN2
CN8
CN7
C1
C3
C2
1000uF
1000uF
1000uF
D2
1N4001
D1
1N4001
R7
220
R8
220
IC4
CN1
R9
10K
C4
C5
R2
330
R3
330
R5
330
CN10
CN9
CN11
R1
330
R4
330
IC1
IC2
IC3
IC5
R6
1M
D2
1N4001
D1
D52N2222A
1N4001

National Semiconductor

November 1999

ADC0801/ADC0802/ADC0803/ADC0804/ADC0805 8-Bit µP Compatible A/D Converters

General Description

The ADC0801, ADC0802, ADC0803, ADC0804 and ADC0805 are CMOS 8-bit successive approximation A/D converters that use a differential potentiometric ladder—similar to the 256R products. These converters are designed to allow operation with the NSC800 and INS8080A derivative control bus with TRI-STATE output latches directly driving the data bus. These A/Ds appear like memory locations or I/O ports to the microprocessor and no interfacing logic is needed.

Differential analog voltage inputs allow increasing the common-mode rejection and offsetting the analog zero input voltage value. In addition, the voltage reference input can be adjusted to allow encoding any smaller analog voltage span to the full 8 bits of resolution.

Features

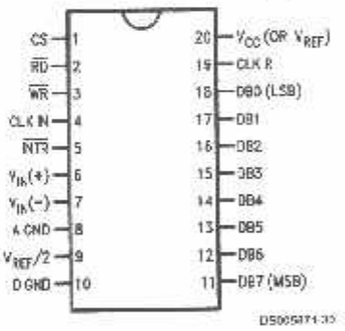
- Compatible with 8080 µP derivatives—no interfacing logic needed - access time - 135 ns
- Easy interface to all microprocessors, or operates "stand alone"
- Differential analog voltage inputs
- Logic inputs and outputs meet both MOS and TTL voltage level specifications
- Works with 2.5V (LM336) voltage reference
- On-chip clock generator
- 0V to 5V analog input voltage range with single 5V supply
- No zero adjust required
- 0.3" standard width 20-pin DIP package
- 20-pin molded chip carrier or small outline package
- Operates ratiometrically or with 5 V_{DC}, 2.5 V_{DC}, or analog span adjusted voltage reference

Key Specifications

■ Resolution	8 bits
■ Total error	±¼ LSB, ±½ LSB and ±1 LSB
■ Conversion time	100 µs

Connection Diagram

ADC080X
Dual-In-Line and Small Outline (SO) Packages



DS005671-35

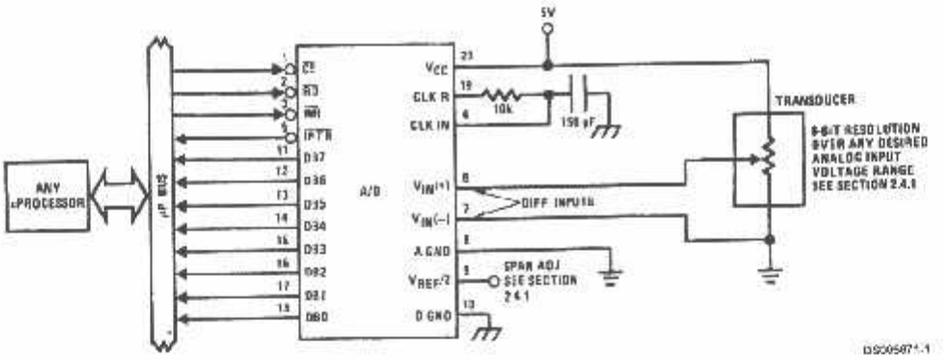
See Ordering Information

Ordering Information

TEMP RANGE		0°C TO 70°C	0°C TO 70°C	−40°C TO +85°C
ERROR	±¼ Bit Adjusted			ADC0801LCN
	±½ Bit Unadjusted	ADC0802LCWM		ADC0802LCN
	±½ Bit Adjusted			ADC0803LCN
	±1Bit Unadjusted	ADC0804LCWM	ADC0804LCN	ADC0805LCN/ADC0804LCJ
PACKAGE OUTLINE		M20B—Small Outline	N20A—Molded DIP	

Z-80® is a registered trademark of Zilog Corp.

Typical Applications



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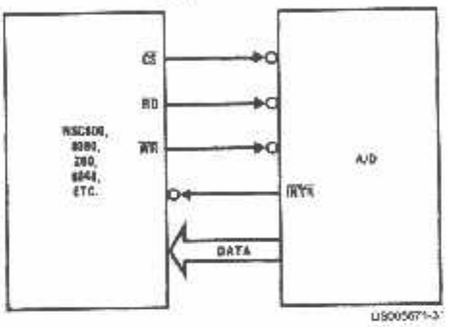
8080 Interface



DS005671-3

Error Specification (Includes Full-Scale, Zero Error, and Non-Linearity)			
Part Number	Full-Scale Adjusted	$V_{REF}/2$=2.500 V_{DC} (No Adjustments)	$V_{REF}/2$=No Connection (No Adjustments)
ADC0801	±¼ LSB		
ADC0802		±½ LSB	
ADC0803	±½ LSB		
ADC0804		±1 LSB	
ADC0805			±1 LSB

AC Electrical Characteristics (Continued)

The following specifications apply for V_{CC}=5 V_{DC} and $T_{MIN} \leq T_A \leq T_{MAX}$ unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Units
C_{OUT}	TRI-STATE Output Capacitance (Data Buffers)			5	7.5	pF
CONTROL INPUTS [Note: CLK IN (Pin 4) is the input of a Schmitt trigger circuit and is therefore specified separately]						
V_{IN} (1)	Logical "1" Input Voltage (Except Pin 4 CLK IN)	V_{CC}=5.25 V_{DC}	2.0		15	V_{DC}
V_{IN} (0)	Logical "0" Input Voltage (Except Pin 4 CLK IN)	V_{CC}=4.75 V_{DC}			0.8	V_{DC}
I_{IN} (1)	Logical "1" Input Current (All Inputs)	V_{IN}=5 V_{DC}		0.005	1	μA_{DC}
I_{IN} (0)	Logical "0" Input Current (All Inputs)	V_{IN}=0 V_{DC}	−1	−0.005		μA_{DC}
CLOCK IN AND CLOCK R						
V_T+	CLK IN (Pin 4) Positive Going Threshold Voltage		2.7	3.1	3.5	V_{DC}
V_T−	CLK IN (Pin 4) Negative Going Threshold Voltage		1.5	1.8	2.1	V_{DC}
V_H	CLK IN (Pin 4) Hysteresis (V_T+)−(V_T−)		0.6	1.3	2.0	V_{DC}
V_{OUT} (0)	Logical "0" CLK R Output Voltage	I_O=360 µA V_{CC}=4.75 V_{DC}			0.4	V_{DC}
V_{OUT} (1)	Logical "1" CLK R Output Voltage	I_O=−360 µA V_{CC}=4.75 V_{DC}	2.4			V_{DC}
DATA OUTPUTS AND $\overline{INTR}$						
V_{OUT} (0)	Logical "0" Output Voltage Data Outputs $\overline{INTR}$ Output	 I_{OUT}=1.6 mA, V_{CC}=4.75 V_{DC} I_{OUT}=1.0 mA, V_{CC}=4.75 V_{DC}			 0.4 0.4	 V_{DC} V_{DC}
V_{OUT} (1)	Logical "1" Output Voltage	I_O=−360 µA, V_{CC}=4.75 V_{DC}	2.4			V_{DC}
V_{OUT} (1)	Logical "1" Output Voltage	I_O=−10 µA, V_{CC}=4.75 V_{DC}	4.5			V_{DC}
I_{OUT}	TRI-STATE Disabled Output Leakage (All Data Buffers)	V_{OUT}=0 V_{DC} V_{OUT}=5 V_{DC}	−3		 3	μA_{DC} μA_{DC}
I_{SOURCE}		V_{OUT} Short to Gnd. T_A=25°C	4.5	6		mA_{DC}
I_{SINK}		V_{OUT} Short to V_{CC}. T_A=25°C	9.0	16		mA_{DC}
POWER SUPPLY						
I_{CC}	Supply Current (Includes Ladder Current) ADC0801/02/03/04LCJ/05 ADC0804LCN/LCWM	f_{CLK}=640 kHz, $V_{REF}/2$=NC, T_A=25°C and $\overline{CS}$ =5V		 1.1 1.9	 1.8 2.5	 mA mA

Note 1: Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. DC and AC electrical specifications do not apply when operating the device beyond its specified operating conditions.

Note 2: All voltages are measured with respect to Gnd, unless otherwise specified. The separate A Gnd point should always be wired to the D Gnd.

Note 3: A zener diode exists, internally, from V_{CC} to Gnd and has a typical breakdown voltage of 7 V_{DC}.

Note 4: For $V_{IN}(-) \geq V_{IN}(+)$ the digital output code will be 0000 0000. Two on-chip diodes are tied to each analog input (see block diagram) which will forward conduct for analog input voltages one diode drop below ground or one diode drop greater than the V_{CC} supply. Be careful, during testing at low V_{CC} levels (4.5V), as high level analog inputs (5V) can cause this input diode to conduct—especially at elevated temperatures, and cause errors for analog inputs near full-scale. The spec allows 50 mV forward bias of either diode. This means that as long as the analog V_{IN} does not exceed the supply voltage by more than 50 mV, the output code will be correct. To achieve an absolute 0 V_{DC} to 5 V_{DC} input voltage range will therefore require a minimum supply voltage of 4.950 V_{DC} over temperature variations, initial tolerance and loading.

Note 5: Accuracy is guaranteed at f_{CLK} = 640 kHz. At higher clock frequencies accuracy can degrade. For lower clock frequencies, the duty cycle limits can be extended so long as the minimum clock high time interval or minimum clock low time interval is no less than 275 ns.

Note 6: With an asynchronous start pulse, up to 8 clock periods may be required before the internal clock phases are proper to start the conversion process. The start request is internally latched, see *Figure 4* and section 2.0.

AC Electrical Characteristics (Continued)

Note 7: The $\overline{CS}$ input is assumed to bracket the $\overline{WR}$ strobe input and therefore timing is dependent on the $\overline{WR}$ pulse width. An arbitrarily wide pulse width will hold the converter in a reset mode and the start of conversion is initiated by the low to high transition of the $\overline{WR}$ pulse (see timing diagrams).

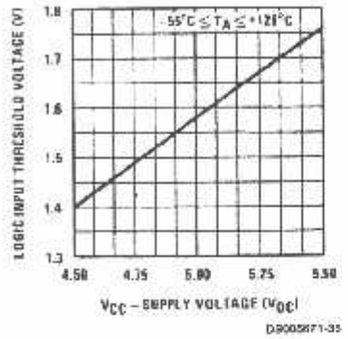
Note 8: None of these A/Ds requires a zero adjust. (see section 2.5.1). To obtain zero code at other analog input voltages see section 2.5 and *Figure 7*.

Note 9: The $V_{REF}/2$ pin is the center point of a two-resistor divider connected from V_{CC} to ground. In all versions of the ADC0801, ADC0802, ADC0803, and ADC0805, and in the ADC0804LCJ, each resistor is typically 16 kΩ. In all versions of the ADC0804 except the ADC0804LCJ, each resistor is typically 2.2 kΩ.

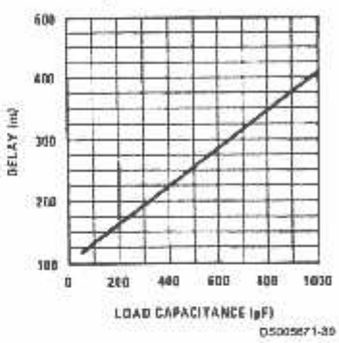
Note 10: Human body model, 100 pF discharged through a 1.5 kΩ resistor.

Typical Performance Characteristics

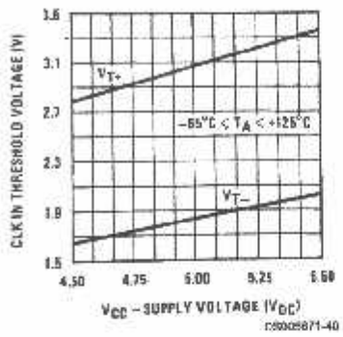
Logic Input Threshold Voltage vs. Supply Voltage



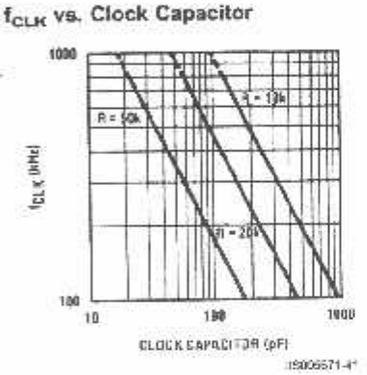
Delay From Falling Edge of RD to Output Data Valid vs. Load Capacitance



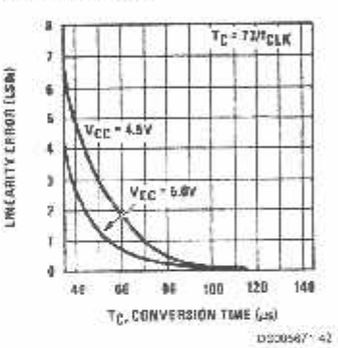
CLK IN Schmitt Trip Levels vs. Supply Voltage



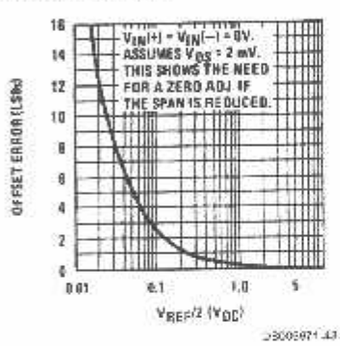
f_{CLK} vs. Clock Capacitor



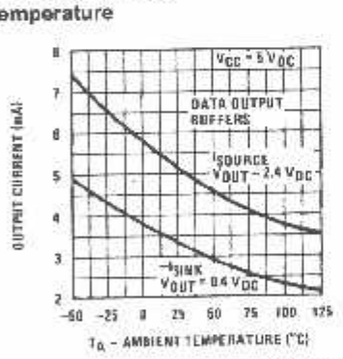
Full-Scale Error vs Conversion Time



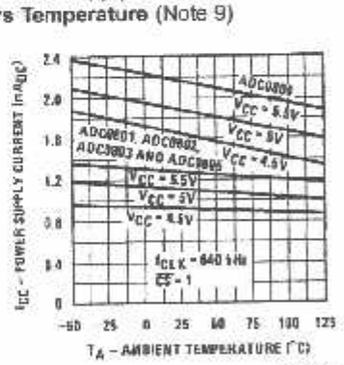
Effect of Unadjusted Offset Error vs. $V_{REF}/2$ Voltage



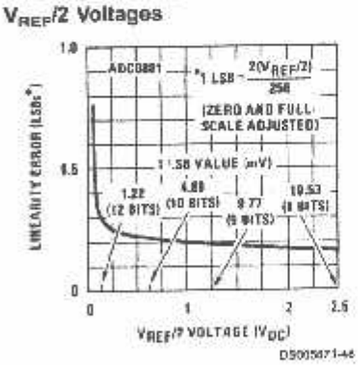
Output Current vs Temperature



Power Supply Current vs Temperature (Note 9)

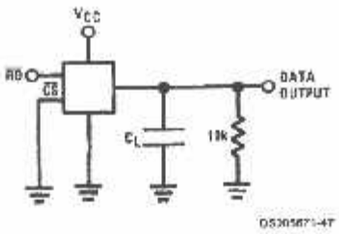


Linearity Error at Low $V_{REF}/2$ Voltages

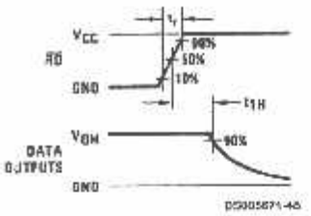


TRI-STATE Test Circuits and Waveforms

t_{1H}

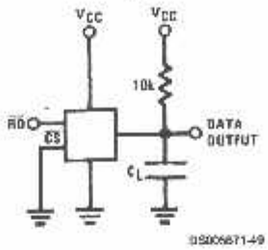


t_{1H}, C_L=10 pF

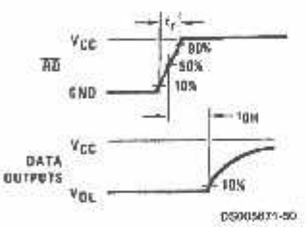


t_r=20 ns

t_{0H}

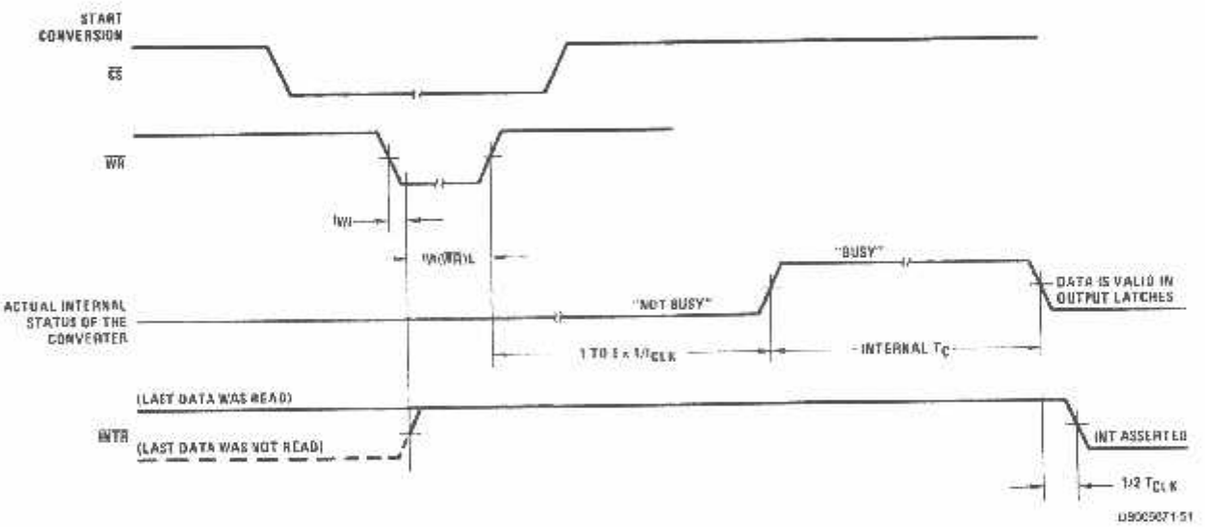


t_{0H}, C_L=10 pF



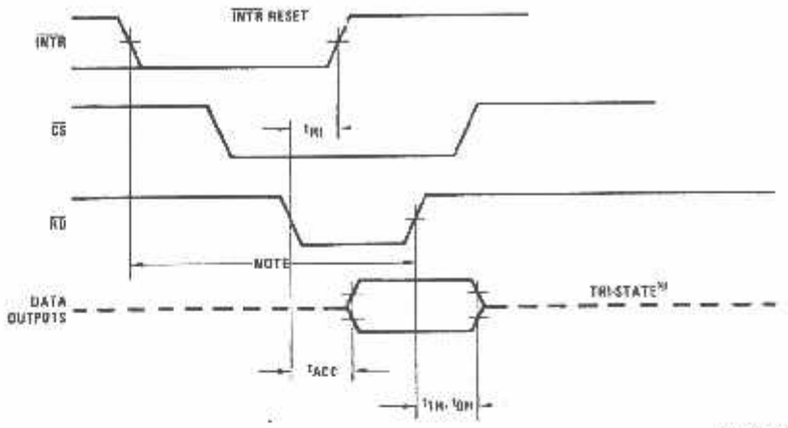
t_r=20 ns

Timing Diagrams (All timing is measured from the 50% voltage points)



Timing Diagrams (All timing is measured from the 50% voltage points) (Continued)

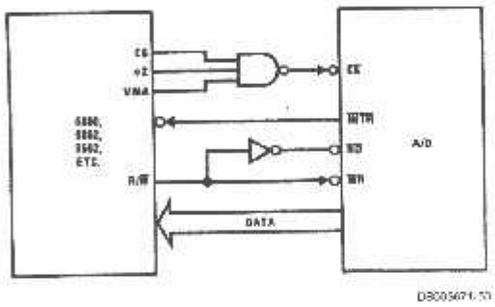
Output Enable and Reset with $\overline{INTR}$



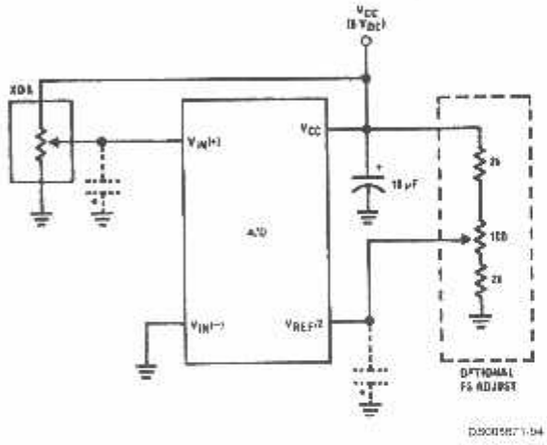
Note: Read strobe must occur 8 clock periods ($8/f_{CLK}$) after assertion of interrupt to guarantee reset of $\overline{INTR}$.

Typical Applications

6800 Interface



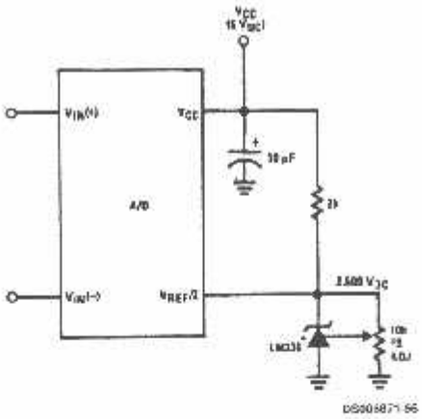
Ratiometeric with Full-Scale Adjust



Note: before using caps at V_{IN} or $V_{REF}/2$, see section 2.3.2 Input Bypass Capacitors.

Typical Applications (Continued)

Absolute with a 2.500V Referencc



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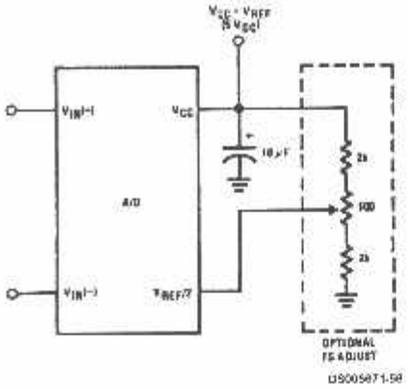
*For low power, see also LM385–2.5

Absolute with a 5V Reference



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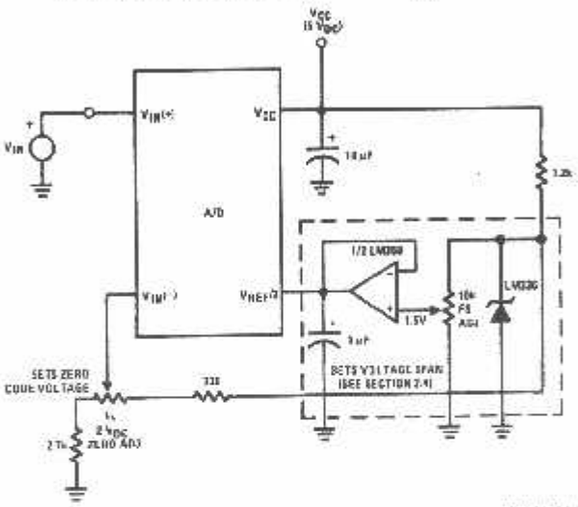
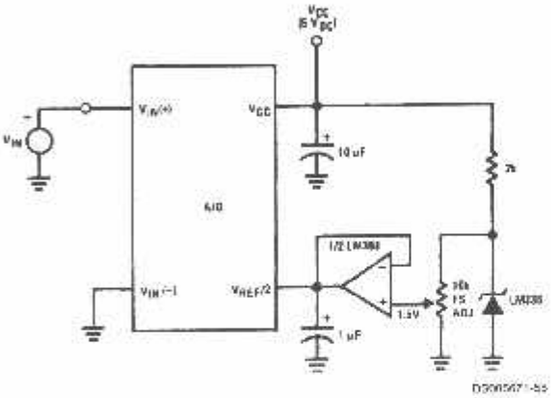
Zero-Shift and Span Adjust: 2V ≤ V_{IN} ≤ 5V

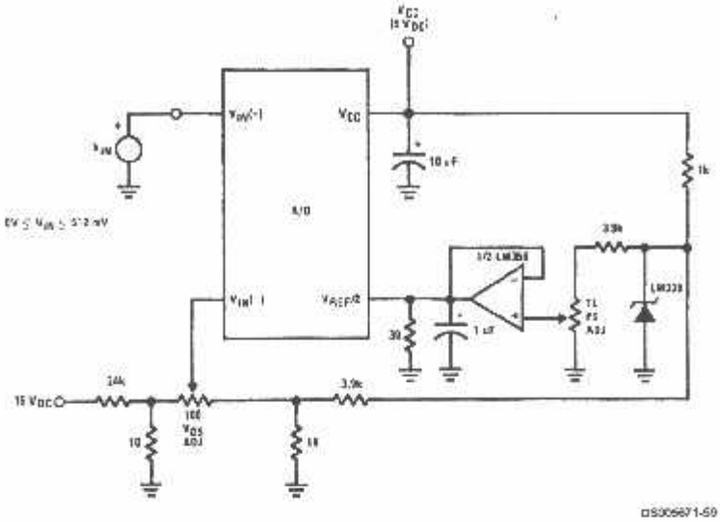


Span Adjust: 0V ≤ V_{IN} ≤ 3V



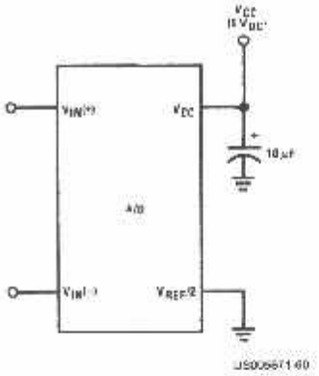
Typical Applications (Continued)

Directly Converting a Low-Level Signal



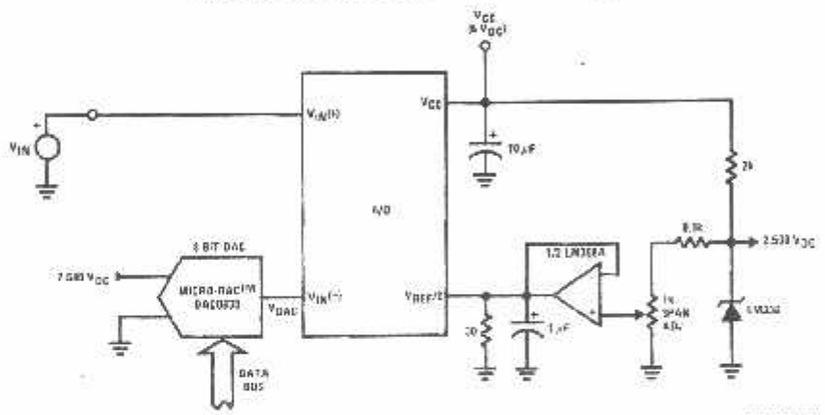
$V_{REF}/2 = 256$ mV

A µP Interfaced Comparator



For:
$V_{IN}(+) > V_{IN}(-)$
Output=FF_{HEX}
For:
$V_{IN}(+) < V_{IN}(-)$
Output=00_{HEX}

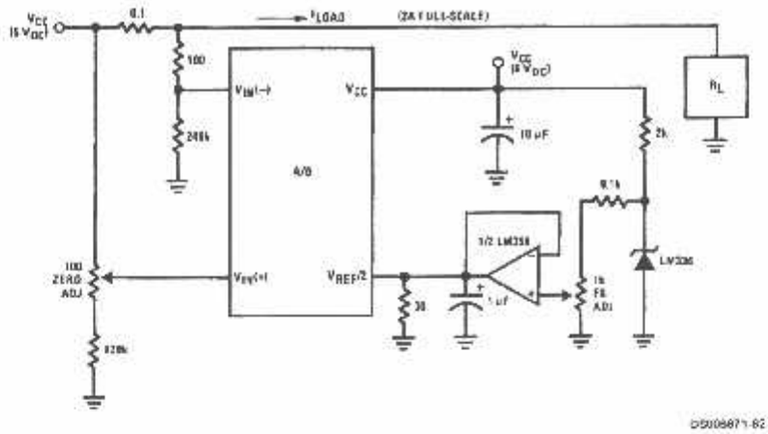
1 mV Resolution with µP Controlled Range



$V_{REF}/2 = 128$ mV
1 LSB = 1 mV
$V_{DAC} \leq V_{IN} \leq (V_{DAC} + 256$ mV)
$0 \leq V_{DAC} < 2.5V$

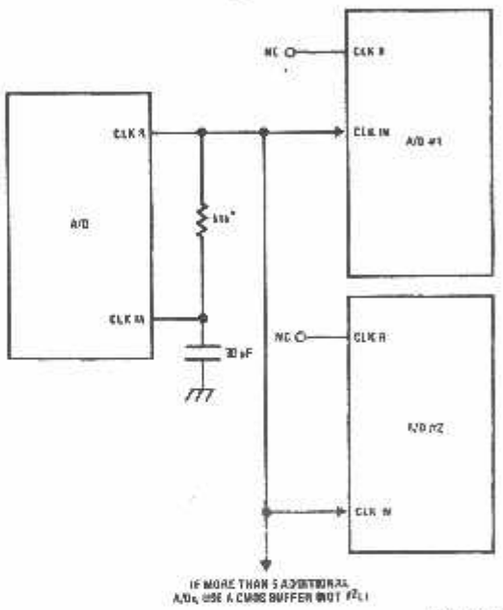
Typical Applications (Continued)

Digitizing a Current Flow



DS005671-82

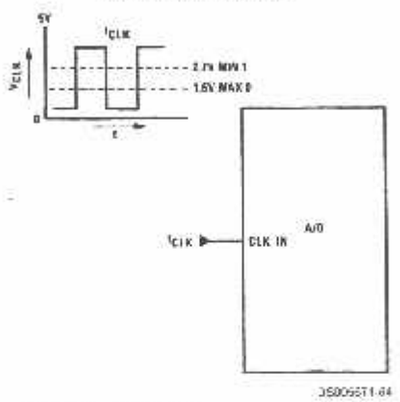
Self-Clocking Multiple A/Ds



DS005671-59

* Use a large R value to reduce loading at CLK R output.

External Clocking

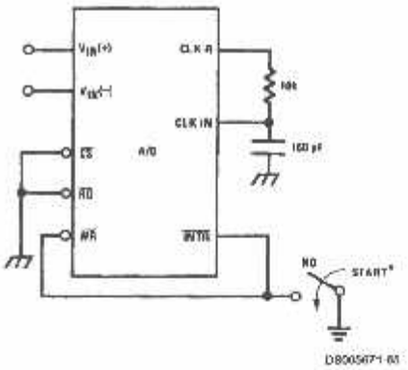


DS005671-84

100 kHz≤f_{CLK}≤1460 kHz

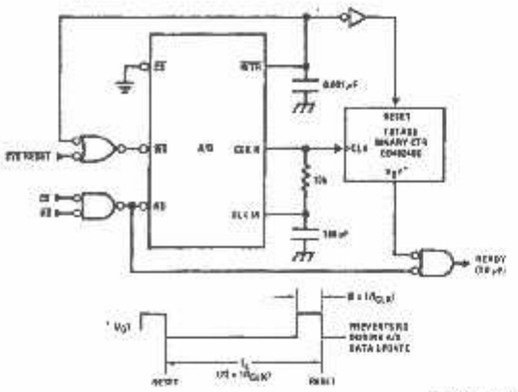
Typical Applications (Continued)

Self-Clocking in Free-Running Mode

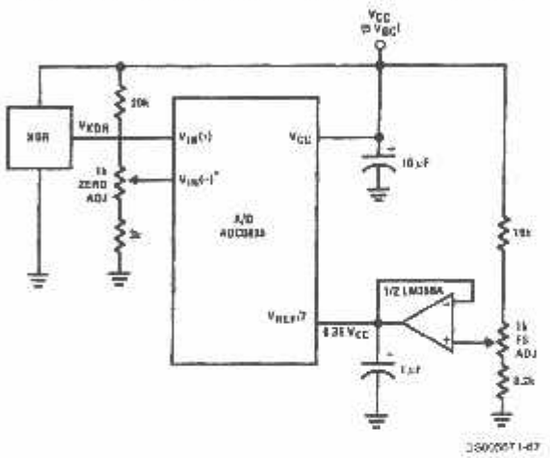


*After power-up, a momentary grounding of the $\overline{WR}$ input is needed to guarantee operation.

µP Interface for Free-Running A/D

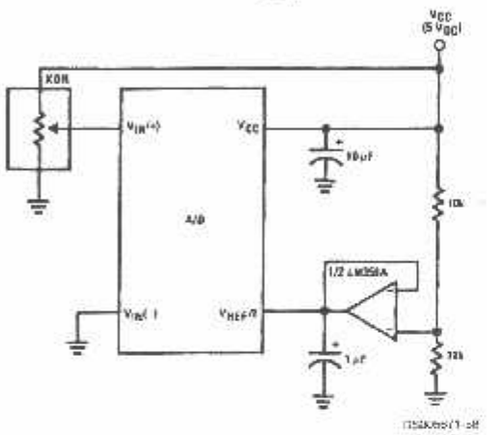


Operating with "Automotive" Ratiometric Transducers

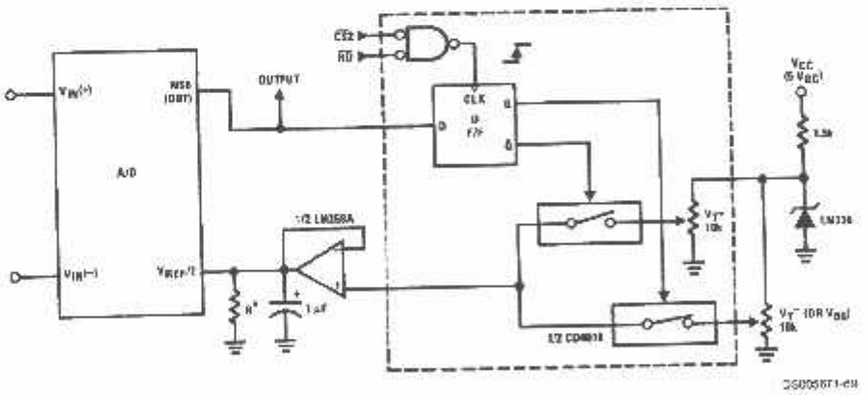


*$V_{IN}(-)=0.15\ V_{CC}$
15% of $V_{CC} \leq V_{XDR} \leq 85\%$ of V_{CC}

Ratiometric with $V_{REF}/2$ Forced



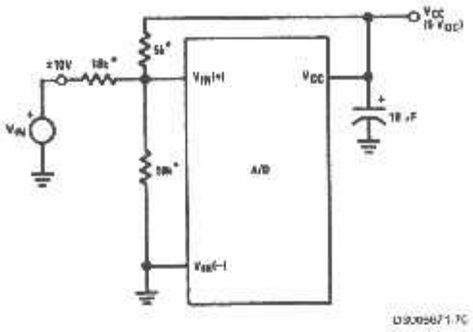
µP Compatible Differential-Input Comparator with Pre-Set V_{OS} (with or without Hysteresis)



*See *Figure 5* to select R value
DB7="1" for $V_{IN}(+) > V_{IN}(-)+(V_{REF}/2)$
Omit circuitry within the dotted area if hysteresis is not needed

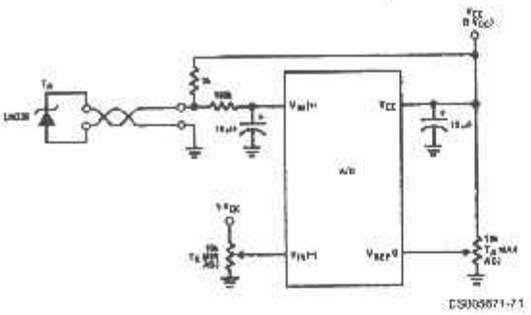
Typical Applications (Continued)

Handling ±10V Analog Inputs

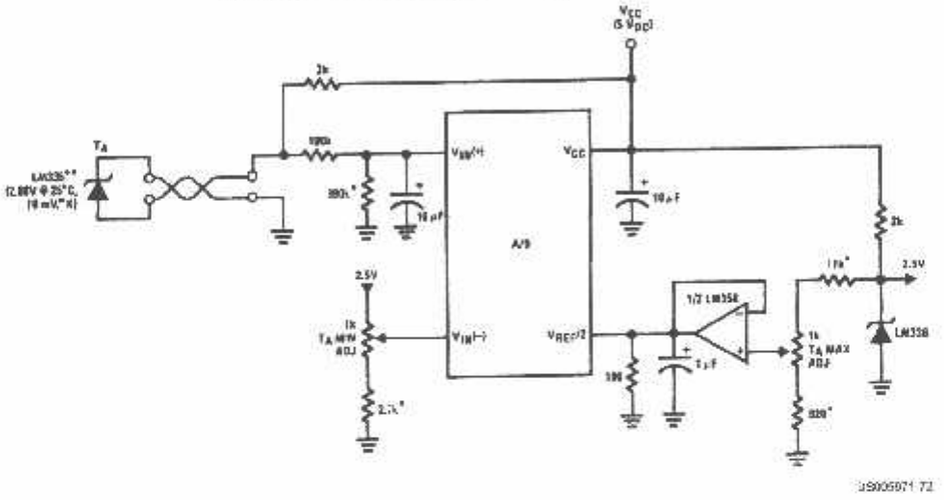


*Beckman Instruments #694-3-R10K resistor array

Low-Cost, µP Interfaced, Temperature-to-Digital Converter



µP Interfaced Temperature-to-Digital Converter

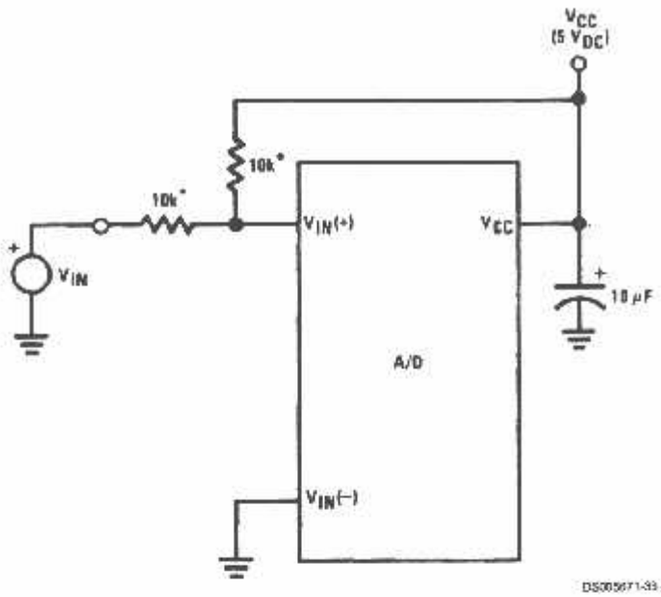


*Circuit values shown are for $0°C \leq T_A \leq +125°C$

**Can calibrate each sensor to allow easy replacement, then A/D can be calibrated with a pre-set input voltage.

Typical Applications (Continued)

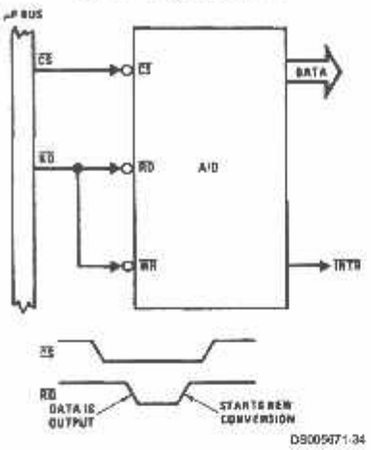
Handling ±5V Analog Inputs



DS005671-33

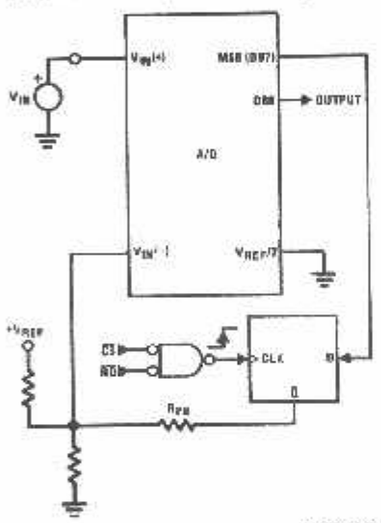
*Bookman Instruments #894-3-R10K resistor array

Read-Only Interface



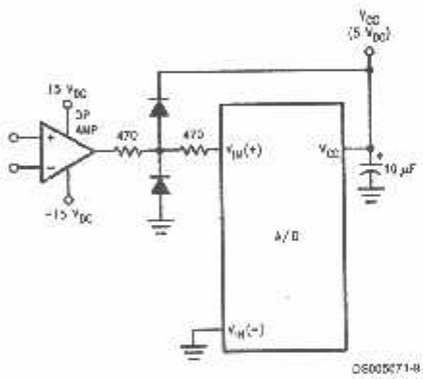
DS005671-34

µP Interfaced Comparator with Hysteresis



DS005671-35

Protecting the Input

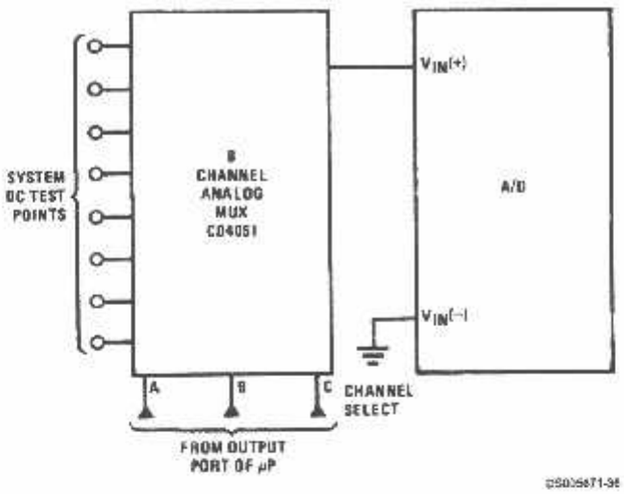


DS005671-8

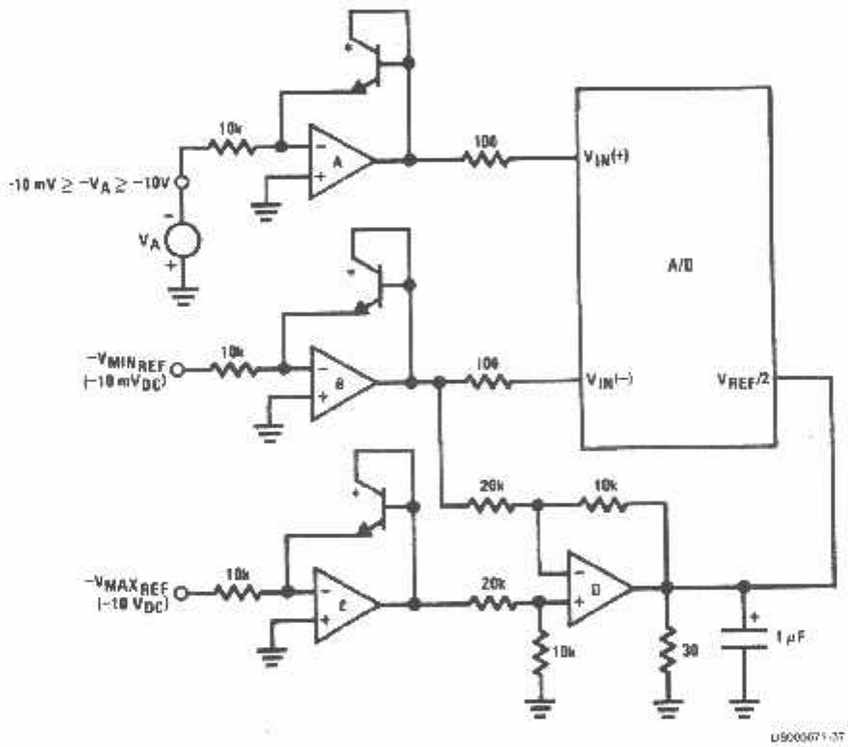
Diodes are 1N914

Typical Applications (Continued)

Analog Self-Test for a System



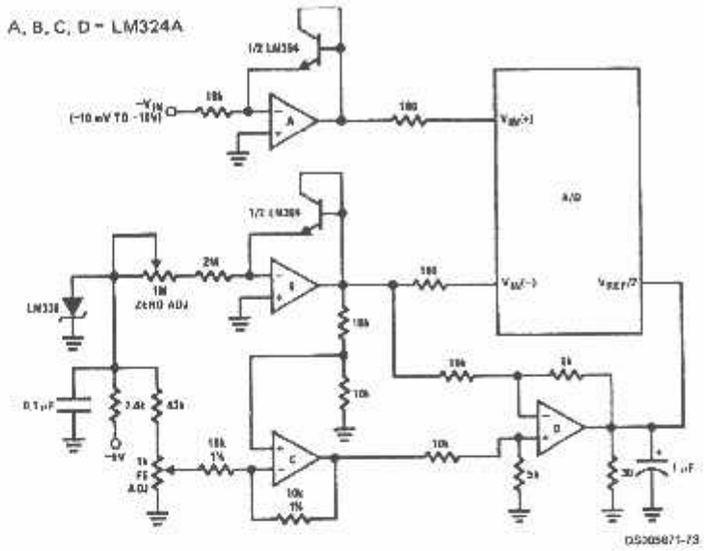
A Low-Cost, 3-Decade Logarithmic Converter



*LM389 transistors
A, B, C, D = LM324A quad op amp

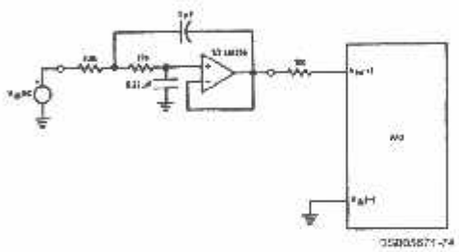
Typical Applications (Continued)

3-Decade Logarithmic A/D Converter



DS005671-73

Noise Filtering the Analog Input



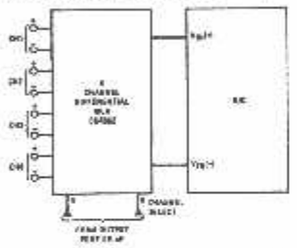
DS005671-74

f_C = 20 Hz

Uses Chebyshev implementation for steeper roll-off unity-gain, 2nd order, low-pass filter

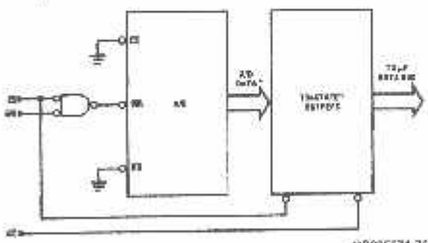
Adding a separate filter for each channel increases system response time if an analog multiplexer is used

Multiplexing Differential Inputs



DS005671-75

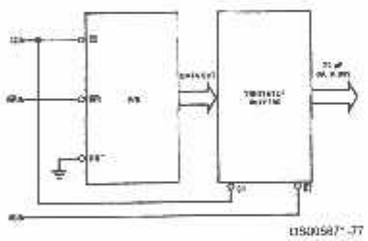
Output Buffers with A/D Data Enabled



DS005671-76

*A/D output data is updated 1 CLK period prior to assertion of $\overline{INTR}$

Increasing Bus Drive and/or Reducing Time on Bus

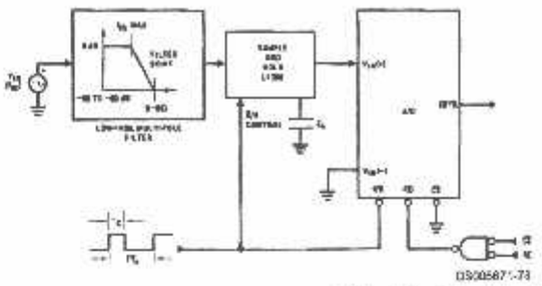


DS005671-77

*Allows output data to set-up at falling edge of $\overline{CS}$

Typical Applications (Continued)

Sampling an AC Input Signal

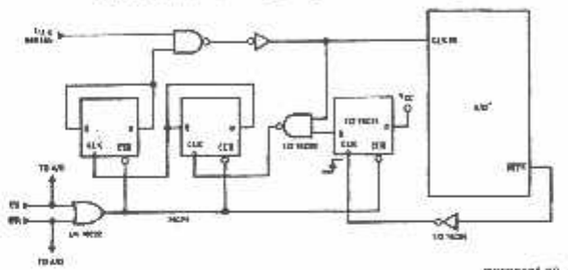


DS005671-73

Note 11: Oversample whenever possible (keep fs > 2[f−60]) to eliminate input frequency folding (aliasing) and to allow for the skirt response of the filter.

Note 12: Consider the amplitude errors which are introduced within the passband of the filter.

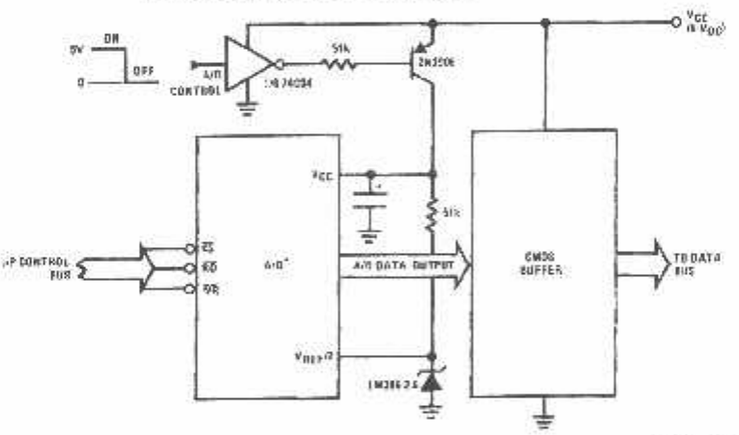
70% Power Savings by Clock Gating



DS005671-79

(Complete shutdown takes ≈ 30 seconds.)

Power Savings by A/D and V_{REF} Shutdown



DS005671-80

*Use ADC0801, 02, 03 or 05 for lowest power consumption.
Note: Logic inputs can be driven to V_{CC} with A/D supply at zero volts.
Buffer prevents data bus from overdriving output of A/D when in shutdown mode.

Functional Description

1.0 UNDERSTANDING A/D ERROR SPECS

A perfect A/D transfer characteristic (staircase waveform) is shown in *Figure 1*. The horizontal scale is analog input voltage and the particular points labeled are in steps of 1 LSB (19.53 mV with 2.5V tied to the $V_{REF}/2$ pin). The digital output codes that correspond to these inputs are shown as D−1, D, and D+1. For the perfect A/D, not only will center-value (A−1, A, A+1, ...) analog inputs produce the correct output digital codes, but also each riser (the transitions between adjacent output codes) will be located ±½ LSB away from each center-value. As shown, the risers are ideal and have no width. Correct digital output codes will be provided for a range of analog input voltages that extend

Functional Description (Continued)

±½ LSB from the ideal center-values. Each tread (the range of analog input voltage that provides the same digital output code) is therefore 1 LSB wide.

Figure 2 shows a worst case error plot for the ADC0801. All center-valued inputs are guaranteed to produce the correct output codes and the adjacent risers are guaranteed to be no closer to the center-value points than ±¼ LSB. In other words, if we apply an analog input equal to the center-value ±¼ LSB, *we guarantee* that the A/D will produce the correct digital code. The maximum range of the position of the code transition is indicated by the horizontal arrow and it is guaranteed to be no more than ½ LSB.

The error curve of *Figure 3* shows a worst case error plot for the ADC0802. Here we guarantee that if we apply an analog input equal to the LSB analog voltage center-value the A/D will produce the correct digital code.

Next to each transfer function is shown the corresponding error plot. Many people may be more familiar with error plots than transfer functions. The analog input voltage to the A/D is provided by either a linear ramp or by the discrete output steps of a high resolution DAC. Notice that the error is continuously displayed and includes the quantization uncertainty of the A/D. For example the error at point 1 of *Figure 1* is +½ LSB because the digital code appeared ½ LSB in advance of the center-value of the tread. The error plots always have a constant negative slope and the abrupt upside steps are always 1 LSB in magnitude.

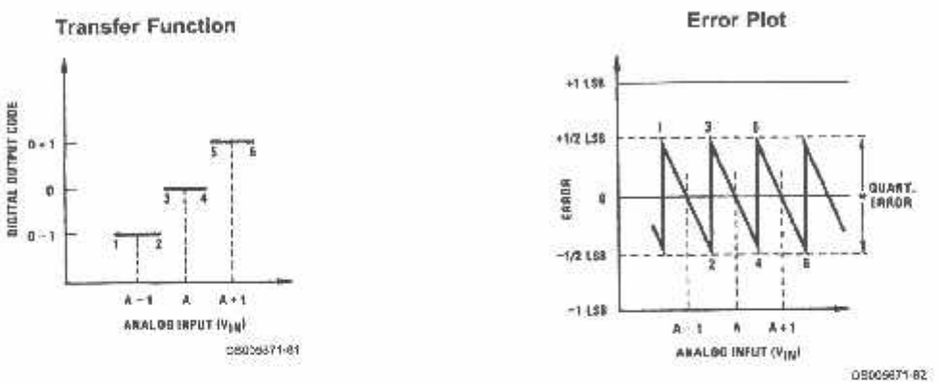


FIGURE 1. Clarifying the Error Specs of an A/D Converter Accuracy=±0 LSB: A Perfect A/D

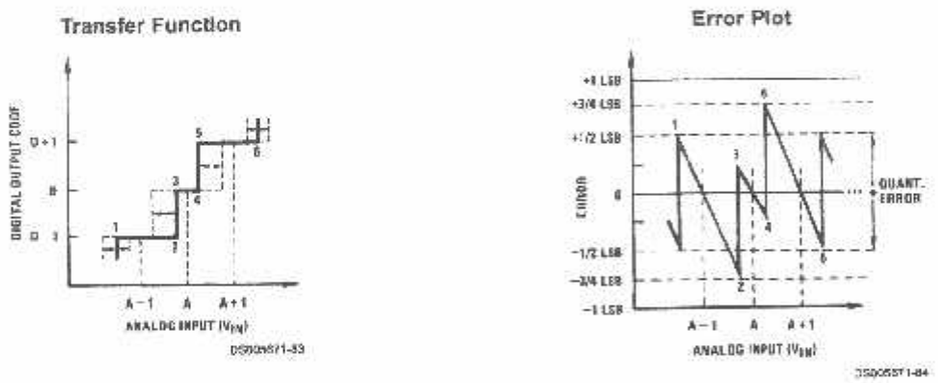


FIGURE 2. Clarifying the Error Specs of an A/D Converter Accuracy=±¼ LSB

Functional Description (Continued)

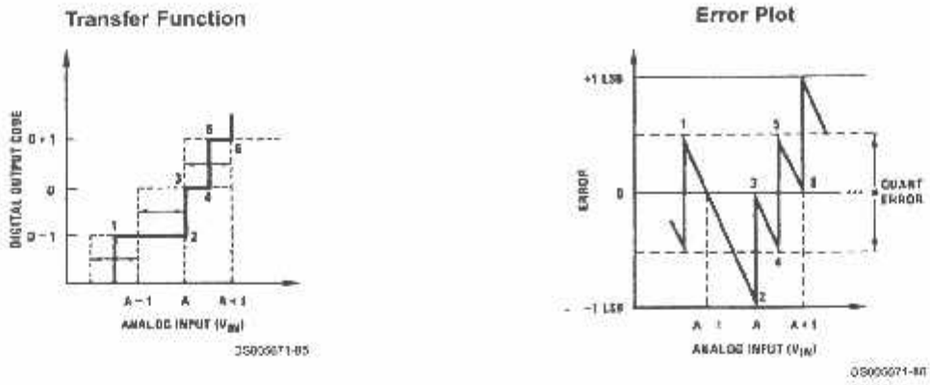


FIGURE 3. Clarifying the Error Specs of an A/D Converter
Accuracy=±½ LSB

2.0 FUNCTIONAL DESCRIPTION

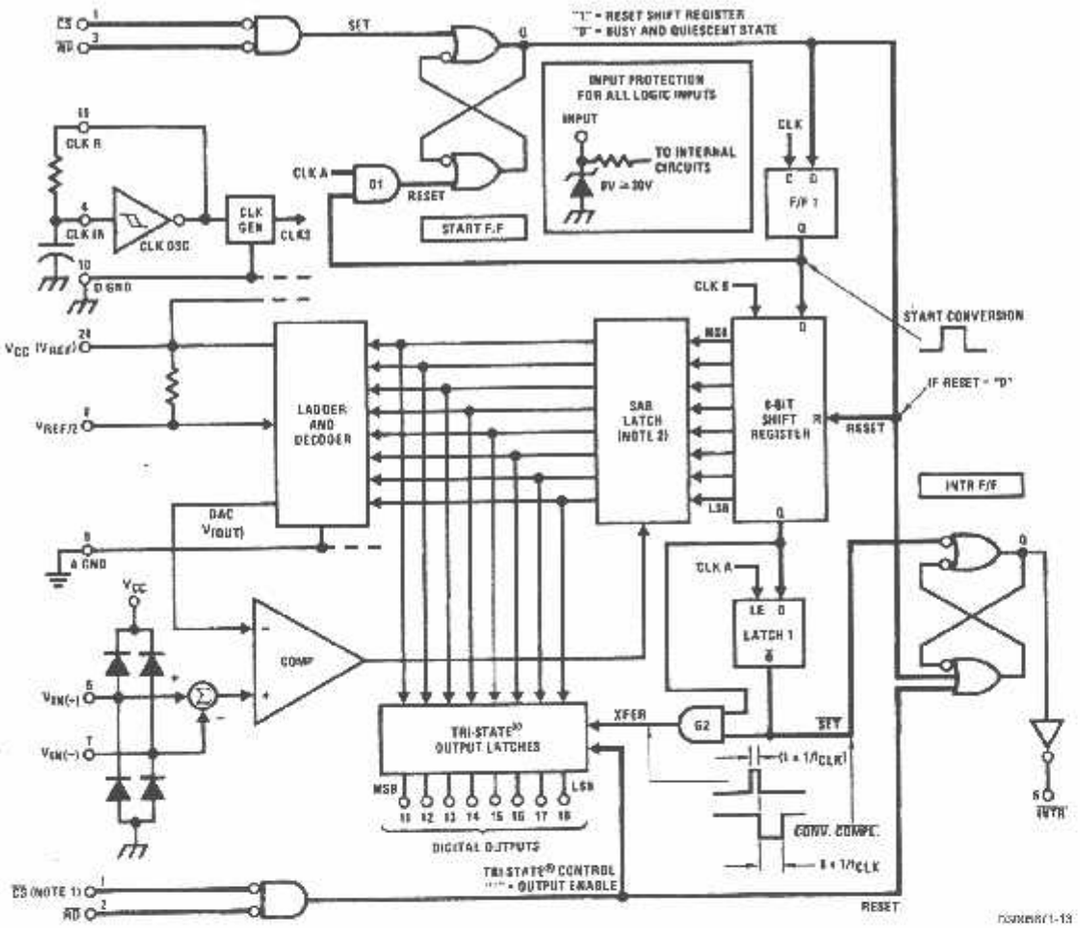
The ADC0801 series contains a circuit equivalent of the 256R network. Analog switches are sequenced by successive approximation logic to match the analog difference input voltage $[V_{IN}(+) - V_{IN}(-)]$ to a corresponding tap on the R network. The most significant bit is tested first and after 8 comparisons (64 clock cycles) a digital 8-bit binary code (1111 1111 = full-scale) is transferred to an output latch and then an interrupt is asserted ($\overline{INTR}$ makes a high-to-low transition). A conversion in process can be interrupted by issuing a second start command. The device may be operated in the free-running mode by connecting $\overline{INTR}$ to the $\overline{WR}$ input with $\overline{CS}$ =0. To ensure start-up under all possible conditions, an external $\overline{WR}$ pulse is required during the first power-up cycle.

On the high-to-low transition of the $\overline{WR}$ input the internal SAR latches and the shift register stages are reset. As long as the $\overline{CS}$ input and $\overline{WR}$ input remain low, the A/D will remain in a reset state. *Conversion will start from 1 to 8 clock periods after at least one of these inputs makes a low-to-high transition.*

A functional diagram of the A/D converter is shown in *Figure 4*. All of the package pinouts are shown and the major logic control paths are drawn in heavier weight lines.

The converter is started by having $\overline{CS}$ and $\overline{WR}$ simultaneously low. This sets the start flip-flop (F/F) and the resulting "1" level resets the 8-bit shift register, resets the Interrupt (INTR) F/F and inputs a "1" to the D flop, F/F1, which is at the input end of the 8-bit shift register. Internal clock signals then transfer this "1" to the Q output of F/F1. The AND gate, G1, combines this "1" output with a clock signal to provide a reset signal to the start F/F. If the set signal is no longer present (either $\overline{WR}$ or $\overline{CS}$ is a "1") the start F/F is reset and the 8-bit shift register then can have the "1" clocked in, which starts the conversion process. If the set signal were to still be present, this reset pulse would have no effect (both outputs of the start F/F would momentarily be at a "1" level) and the 8-bit shift register would continue to be held in the reset mode. This logic therefore allows for wide $\overline{CS}$ and $\overline{WR}$ signals and the converter will start after at least one of these signals returns high and the internal clocks again provide a reset signal for the start F/F.

Functional Description (Continued)



Note 13: $\overline{CS}$ shown twice for clarity.

Note 14: SAR = Successive Approximation Register

FIGURE 4. Block Diagram

After the "1" is clocked through the 8-bit shift register (which completes the SAR search) it appears as the input to the D-type latch, LATCH 1. As soon as this "1" is output from the shift register, the AND gate, G2, causes the new digital word to transfer to the TRI-STATE output latches. When LATCH 1 is subsequently enabled, the Q output makes a high-to-low transition which causes the INTR F/F to set. An inverting buffer then supplies the $\overline{INTR}$ input signal.

Note that this $\overline{SET}$ control of the INTR F/F remains low for 8 of the external clock periods (as the internal clocks run at 1/8 of the frequency of the external clock). If the data output is continuously enabled ($\overline{CS}$ and $\overline{RD}$ both held low), the $\overline{INTR}$ output will still signal the end of conversion (by a high-to-low transition), because the $\overline{SET}$ input can control the Q output of the INTR F/F even though the RESET input is constantly at a "1" level in this operating mode. This $\overline{INTR}$ output will therefore stay low for the duration of the $\overline{SET}$ signal, which is 8 periods of the external clock frequency (assuming the A/D is not started during this interval).

When operating in the free-running or continuous conversion mode ($\overline{INTR}$ pin tied to $\overline{WR}$ and $\overline{CS}$ wired low—see also section 2.8), the START F/F is SET by the high-to-low transition of the $\overline{INTR}$ signal. This resets the SHIFT REGISTER which causes the input to the D-type latch, LATCH 1, to go low. As the latch enable input is still present, the $\overline{Q}$ output will go high, which then allows the INTR F/F to be RESET. This reduces the width of the resulting $\overline{INTR}$ output pulse to only a few propagation delays (approximately 300 ns).

When data is to be read, the combination of both $\overline{CS}$ and $\overline{RD}$ being low will cause the INTR F/F to be reset and the TRI-STATE output latches will be enabled to provide the 8-bit digital outputs.

2.1 Digital Control Inputs

The digital control inputs ($\overline{CS}$, $\overline{RD}$, and $\overline{WR}$) meet standard T^2L logic voltage levels. These signals have been renamed when compared to the standard A/D Start and Output Enable labels. In addition, these inputs are active low to allow an easy interface to microprocessor control busses. For non-microprocessor based applications, the $\overline{CS}$ input (pin 1) can be grounded and the standard A/D Start function is obtained by an active low pulse applied at the $\overline{WR}$ input (pin 3) and the Output Enable function is caused by an active low pulse at the $\overline{RD}$ input (pin 2).

Functional Description (Continued)

2.2 Analog Differential Voltage Inputs and Common-Mode Rejection

This A/D has additional applications flexibility due to the analog differential voltage input. The $V_{IN}(-)$ input (pin 7) can be used to automatically subtract a fixed voltage value from the input reading (tare correction). This is also useful in 4 mA–20 mA current loop conversion. In addition, common-mode noise can be reduced by use of the differential input.

The time interval between sampling $V_{IN}(+)$ and $V_{IN}(-)$ is 4-½ clock periods. The maximum error voltage due to this slight time difference between the input voltage samples is given by:

$$\Delta V_a(MAX) = (V_P)(2\pi f_{cm})\left(\frac{4.5}{f_{CLK}}\right)$$

where:

ΔV_a is the error voltage due to sampling delay

V_P is the peak value of the common-mode voltage

f_{cm} is the common-mode frequency

As an example, to keep this error to ¼ LSB (~5 mV) when operating with a 60 Hz common-mode frequency, f_{cm}, and using a 640 kHz A/D clock, f_{CLK}, would allow a peak value of the common-mode voltage, V_P, which is given by:

$$V_P = \frac{[\Delta V_{a(MAX)}\,(f_{CLK})]}{(2\pi f_{cm})\,(4.5)}$$

or

$$V_P = \frac{(5 \times 10^{-3})\,(640 \times 10^3)}{(6.28)\,(60)\,(4.5)}$$

which gives

$V_P \approx 1.9V$.

The allowed range of analog input voltages usually places more severe restrictions on input common-mode noise levels.

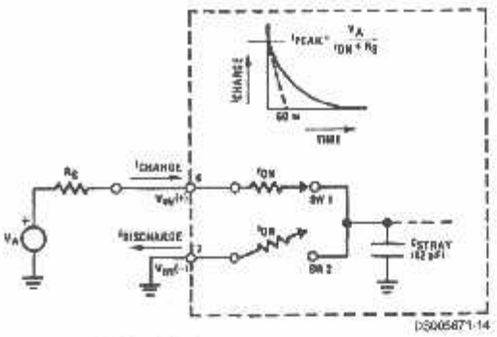
An analog input voltage with a reduced span and a relatively large zero offset can be handled easily by making use of the differential input (see section 2.4 Reference Voltage).

2.3 Analog Inputs

2.3 1 Input Current

Normal Mode

Due to the internal switching action, displacement currents will flow at the analog inputs. This is due to on-chip stray capacitance to ground as shown in *Figure 5*.



r_{ON} of SW 1 and SW 2 = 5 kΩ

r_{ON} C_{STRAY} = 5 kΩ x 12 pF = 60 ns

FIGURE 5. Analog Input Impedance

The voltage on this capacitance is switched and will result in currents entering the $V_{IN}(+)$ input pin and leaving the $V_{IN}(-)$ input which will depend on the analog differential input voltage levels. These current transients occur at the leading edge of the internal clocks. They rapidly decay and *do not cause errors* as the on-chip comparator is strobed at the end of the clock period.

Fault Mode

If the voltage source applied to the $V_{IN}(+)$ or $V_{IN}(-)$ pin exceeds the allowed operating range of V_{CC}+50 mV, large input currents can flow through a parasitic diode to the V_{CC} pin. If these currents can exceed the 1 mA max allowed spec, an external diode (1N914) should be added to bypass this current to the V_{CC} pin (with the current bypassed with this diode, the voltage at the $V_{IN}(+)$ pin can exceed the V_{CC} voltage by the forward voltage of this diode).

2.3.2 Input Bypass Capacitors

Bypass capacitors at the inputs will average these charges and cause a DC current to flow through the output resistances of the analog signal sources. This charge pumping action is worse for continuous conversions with the $V_{IN}(+)$ input voltage at full-scale. For continuous conversions with a 640 kHz clock frequency with the $V_{IN}(+)$ input at 5V, this DC current is at a maximum of approximately 5 µA. Therefore, *bypass capacitors should not be used at the analog inputs or the $V_{REF}/2$ pin* for high resistance sources (> 1 kΩ). If input bypass capacitors are necessary for noise filtering and high source resistance is desirable to minimize capacitor size, the detrimental effects of the voltage drop across this input resistance, which is due to the average value of the input current, can be eliminated with a full-scale adjustment while the given source resistor and input bypass capacitor are both in place. This is possible because the average value of the input current is a precise linear function of the differential input voltage.

2.3.3 Input Source Resistance

Large values of source resistance where an input bypass capacitor is not used, *will not cause errors* as the input currents settle out prior to the comparison time. If a low pass filter is required in the system, use a low valued series resistor (≤ 1 kΩ) for a passive RC section or add an op amp RC active low pass filter. For low source resistance applications, (≤ 1 kΩ), a 0.1 µF bypass capacitor at the inputs will prevent noise pickup due to series lead inductance of a long

Functional Description (Continued)

wire. A 100Ω series resistor can be used to isolate this capacitor—both the R and C are placed outside the feedback loop—from the output of an op amp, if used.

2.3.4 Noise

The leads to the analog inputs (pins 6 and 7) should be kept as short as possible to minimize input noise coupling. Both noise and undesired digital clock coupling to these inputs can cause system errors. The source resistance for these inputs should, in general, be kept below 5 kΩ. Larger values of source resistance can cause undesired system noise pickup. Input bypass capacitors, placed from the analog inputs to ground, will eliminate system noise pickup but can create analog scale errors as these capacitors will average the transient input switching currents of the A/D (see section 2.3.1.). This scale error depends on both a large source resistance and the use of an input bypass capacitor. This error can be eliminated by doing a full-scale adjustment of the A/D (adjust $V_{REF}/2$ for a proper full-scale reading—see section 2.5.2 on Full-Scale Adjustment) with the source resistance and input bypass capacitor in place.

2.4 Reference Voltage

2.4.1 Span Adjust

For maximum applications flexibility, these A/Ds have been designed to accommodate a 5 V_{DC}, 2.5 V_{DC} or an adjusted voltage reference. This has been achieved in the design of the IC as shown in *Figure 6*.

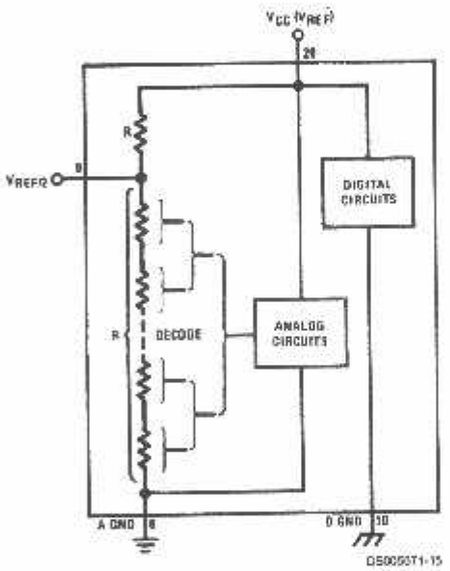


FIGURE 6. The $V_{REFERENCE}$ Design on the IC

Notice that the reference voltage for the IC is either ½ of the voltage applied to the V_{CC} supply pin, or is equal to the voltage that is externally forced at the $V_{REF}/2$ pin. This allows for a ratiometric voltage reference using the V_{CC} supply, a 5 V_{DC} reference voltage can be used for the V_{CC} supply or a voltage less than 2.5 V_{DC} can be applied to the $V_{REF}/2$ input for increased application flexibility. The internal gain to the $V_{REF}/2$ input is 2, making the full-scale differential input voltage twice the voltage at pin 9.

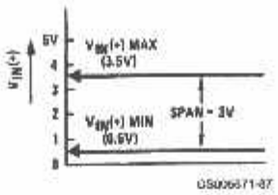
An example of the use of an adjusted reference voltage is to accommodate a reduced span—or dynamic voltage range of the analog input voltage. If the analog input voltage were to range from 0.5 V_{DC} to 3.5 V_{DC}, instead of 0V to 5 V_{DC}, the span would be 3V as shown in *Figure 7*. With 0.5 V_{DC} applied to the $V_{IN}(-)$ pin to absorb the offset, the reference voltage can be made equal to ½ of the 3V span or 1.5 V_{DC}. The A/D now will encode the $V_{IN}(+)$ signal from 0.5V to 3.5 V with the 0.5V input corresponding to zero and the 3.5 V_{DC} input corresponding to full-scale. The full 8 bits of resolution are therefore applied over this reduced analog input voltage range.

2.4.2 Reference Accuracy Requirements

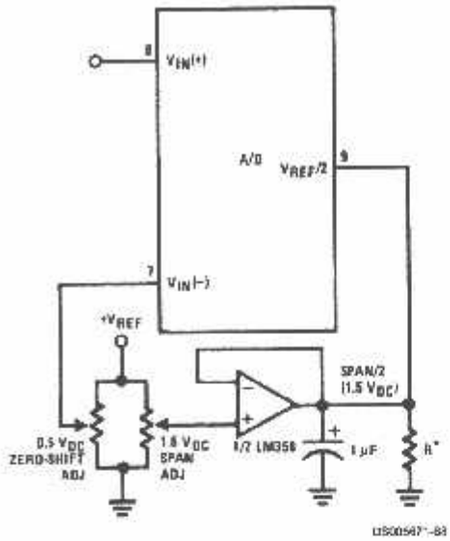
The converter can be operated in a ratiometric mode or an absolute mode. In ratiometric converter applications, the magnitude of the reference voltage is a factor in both the output of the source transducer and the output of the A/D converter and therefore cancels out in the final digital output code. The ADC0805 is specified particularly for use in ratiometric applications with no adjustments required. In absolute conversion applications, both the initial value and the temperature stability of the reference voltage are important factors in the accuracy of the A/D converter. For $V_{REF}/2$ voltages of 2.4 V_{DC} nominal value, initial errors of ±10 mV_{DC} will cause conversion errors of ±1 LSB due to the gain of 2 of the $V_{REF}/2$ input. In reduced span applications, the initial value and the stability of the $V_{REF}/2$ input voltage become even more important. For example, if the span is reduced to 2.5V, the analog input LSB voltage value is correspondingly reduced from 20 mV (5V span) to 10 mV and 1 LSB at the $V_{REF}/2$ input becomes 5 mV. As can be seen, this reduces the allowed initial tolerance of the reference voltage and requires correspondingly less absolute change with temperature variations. Note that spans smaller than 2.5V place even tighter requirements on the initial accuracy and stability of the reference source.

In general, the magnitude of the reference voltage will require an initial adjustment. Errors due to an improper value of reference voltage appear as full-scale errors in the A/D transfer function. IC voltage regulators may be used for references if the ambient temperature changes are not excessive. The LM336B 2.5V IC reference diode (from National Semiconductor) has a temperature stability of 1.8 mV typ (6 mV max) over $0°C \le T_A \le +70°C$. Other temperature range parts are also available.

Functional Description (Continued)



a) Analog Input Signal Example



*Add if $V_{REF}/2 \leq 1$ V_{DC} with LM358 to draw 3 mA to ground.

b) Accommodating an Analog Input from 0.5V (Digital Out = 00_{HEX}) to 3.5V (Digital Out=FF_{HEX})

FIGURE 7. Adapting the A/D Analog Input Voltages to Match an Arbitrary Input Signal Range

2.5 Errors and Reference Voltage Adjustments

2.5.1 Zero Error

The zero of the A/D does not require adjustment. If the minimum analog input voltage value, $V_{IN(MIN)}$, is not ground, a zero offset can be done. The converter can be made to output 0000 0000 digital code for this minimum input voltage by biasing the A/D $V_{IN}(-)$ input at this $V_{IN(MIN)}$ value (see Applications section). This utilizes the differential mode operation of the A/D.

The zero error of the A/D converter relates to the location of the first riser of the transfer function and can be measured by grounding the V_{IN} (−) input and applying a small magnitude positive voltage to the V_{IN} (+) input. Zero error is the difference between the actual DC input voltage that is necessary to just cause an output digital code transition from 0000 0000 to 0000 0001 and the ideal ½ LSB value (½ LSB = 9.8 mV for $V_{REF}/2$=2.500 V_{DC}).

2.5.2 Full-Scale

The full-scale adjustment can be made by applying a differential input voltage that is 1½ LSB less than the desired analog full-scale voltage range and then adjusting the magnitude of the $V_{REF}/2$ input (pin 9 or the V_{CC} supply if pin 9 is not used) for a digital output code that is just changing from 1111 1110 to 1111 1111.

2.5.3 Adjusting for an Arbitrary Analog Input Voltage Range

If the analog zero voltage of the A/D is shifted away from ground (for example, to accommodate an analog input signal that does not go to ground) this new zero reference should be properly adjusted first. A $V_{IN}(+)$ voltage that equals this desired zero reference plus ½ LSB (where the LSB is calculated for the desired analog span, 1 LSB=analog span/256) is applied to pin 6 and the zero reference voltage at pin 7 should then be adjusted to just obtain the 00_{HEX} to 01_{HEX} code transition.

The full-scale adjustment should then be made (with the proper $V_{IN}(-)$ voltage applied) by forcing a voltage to the $V_{IN}(+)$ input which is given by:

$$V_{IN}(+)\text{fs adj} = V_{MAX} - 1.5\left[\frac{(V_{MAX} - V_{MIN})}{256}\right]$$

where:

V_{MAX}=The high end of the analog input range

and

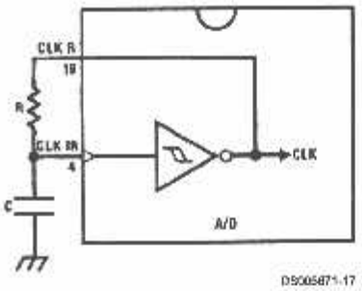
V_{MIN}=the low end (the offset zero) of the analog range. (Both are ground referenced.)

The $V_{REF}/2$ (or V_{CC}) voltage is then adjusted to provide a code change from FE_{HEX} to FF_{HEX}. This completes the adjustment procedure.

2.6 Clocking Option

The clock for the A/D can be derived from the CPU clock or an external RC can be added to provide self-clocking. The CLK IN (pin 4) makes use of a Schmitt trigger as shown in *Figure 8*.

Functional Description (Continued)



D5005871-17

$$f_{CLK} \simeq \frac{1}{1.1\,RC}$$

$R \simeq 10\ k\Omega$

FIGURE 8. Self-Clocking the A/D

Heavy capacitive or DC loading of the clock R pin should be avoided as this will disturb normal converter operation. Loads less than 50 pF, such as driving up to 7 A/D converter clock inputs from a single clock R pin of 1 converter, are allowed. For larger clock line loading, a CMOS or low power TTL buffer or PNP input logic should be used to minimize the loading on the clock R pin (do not use a standard TTL buffer).

2.7 Restart During a Conversion

If the A/D is restarted ($\overline{CS}$ and $\overline{WR}$ go low and return high) during a conversion, the converter is reset and a new conversion is started. The output data latch is not updated if the conversion in process is not allowed to be completed, therefore the data of the previous conversion remains in this latch. The $\overline{INTR}$ output simply remains at the "1" level.

2.8 Continuous Conversions

For operation in the free-running mode an initializing pulse should be used, following power up, to ensure circuit operation. In this application, the $\overline{CS}$ input is grounded and the $\overline{WR}$ input is tied to the $\overline{INTR}$ output. This $\overline{WR}$ and $\overline{INTR}$ node should be momentarily forced to logic low following a power-up cycle to guarantee operation.

2.9 Driving the Data Bus

This MOS A/D, like MOS microprocessors and memories, will require a bus driver when the total capacitance of the data bus gets large. Other circuitry, which is tied to the data bus, will add to the total capacitive loading, even in TRI-STATE (high impedance mode). Backplane bussing also greatly adds to the stray capacitance of the data bus.

There are some alternatives available to the designer to handle this problem. Basically, the capacitive loading of the data bus slows down the response time, even though DC specifications are still met. For systems operating with a relatively slow CPU clock frequency, more time is available in which to establish proper logic levels on the bus and therefore higher capacitive loads can be driven (see typical characteristics curves).

At higher CPU clock frequencies time can be extended for I/O reads (and/or writes) by inserting wait states (8080) or using clock extending circuits (6800).

Finally, if time is short and capacitive loading is high, external bus drivers must be used. These can be TRI-STATE buffers (low power Schottky such as the DM74LS240 series is recommended) or special higher drive current products which are designed as bus drivers. High current bipolar bus drivers with PNP inputs are recommended.

2.10 Power Supplies

Noise spikes on the V_{CC} supply line can cause conversion errors as the comparator will respond to this noise. A low inductance tantalum filter capacitor should be used close to the converter V_{CC} pin and values of 1 µF or greater are recommended. If an unregulated voltage is available in the system, a separate LM340LAZ-5.0, TO-92, 5V voltage regulator for the converter (and other analog circuitry) will greatly reduce digital noise on the V_{CC} supply.

2.11 Wiring and Hook-Up Precautions

Standard digital wire wrap sockets are not satisfactory for breadboarding this A/D converter. Sockets on PC boards can be used and all logic signal wires and leads should be grouped and kept as far away as possible from the analog signal leads. Exposed leads to the analog inputs can cause undesired digital noise and hum pickup, therefore shielded leads may be necessary in many applications.

A single point analog ground that is separate from the logic ground points should be used. The power supply bypass capacitor and the self-clocking capacitor (if used) should both be returned to digital ground. Any $V_{REF}/2$ bypass capacitors, analog input filter capacitors, or input signal shielding should be returned to the analog ground point. A test for proper grounding is to measure the zero error of the A/D converter. Zero errors in excess of ¼ LSB can usually be traced to improper board layout and wiring (see section 2.5.1 for measuring the zero error).

3.0 TESTING THE A/D CONVERTER

There are many degrees of complexity associated with testing an A/D converter. One of the simplest tests is to apply a known analog input voltage to the converter and use LEDs to display the resulting digital output code as shown in *Figure 9*.

For ease of testing, the $V_{REF}/2$ (pin 9) should be supplied with 2.560 V_{DC} and a V_{CC} supply voltage of 5.12 V_{DC} should be used. This provides an LSB value of 20 mV.

If a full-scale adjustment is to be made, an analog input voltage of 5.090 V_{DC} (5.120–1½ LSB) should be applied to the $V_{IN}(+)$ pin with the $V_{IN}(-)$ pin grounded. The value of the $V_{REF}/2$ input voltage should then be adjusted until the digital output code is just changing from 1111 1110 to 1111 1111. This value of $V_{REF}/2$ should then be used for all the tests.

The digital output LED display can be decoded by dividing the 8 bits into 2 hex characters, the 4 most significant (MS) and the 4 least significant (LS). *Table 1* shows the fractional binary equivalent of these two 4-bit groups. By adding the voltages obtained from the "VMS" and "VLS" columns in *Table 1*, the nominal value of the digital display (when $V_{REF}/2$ = 2.560V) can be determined. For example, for an output LED display of 1011 0110 or B6 (in hex), the voltage values from the table are 3.520 + 0.120 or 3.640 V_{DC}. These voltage values represent the center-values of a perfect A/D converter. The effects of quantization error have to be accounted for in the interpretation of the test results.

Functional Description (Continued)

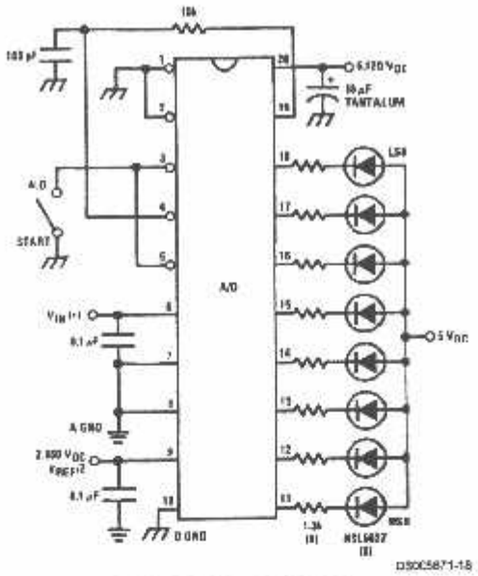


FIGURE 9. Basic A/D Tester

For a higher speed test system, or to obtain plotted data, a digital-to-analog converter is needed for the test set-up. An accurate 10-bit DAC can serve as the precision voltage source for the A/D. Errors of the A/D under test can be expressed as either analog voltages or differences in 2 digital words.

A basic A/D tester that uses a DAC and provides the error as an analog output voltage is shown in *Figure 8*. The 2 op amps can be eliminated if a lab DVM with a numerical subtraction feature is available to read the difference voltage, "A–C", directly. The analog input voltage can be supplied by a low frequency ramp generator and an X-Y plotter can be used to provide analog error (Y axis) versus analog input (X axis).

For operation with a microprocessor or a computer-based test system, it is more convenient to present the errors digitally. This can be done with the circuit of *Figure 11*, where the output code transitions can be detected as the 10-bit DAC is incremented. This provides ¼ LSB steps for the 8-bit A/D under test. If the results of this test are automatically plotted with the analog input on the X axis and the error (in LSB's) as the Y axis, a useful transfer function of the A/D under test results. For acceptance testing, the plot is not necessary and the testing speed can be increased by establishing internal limits on the allowed error for each code.

4.0 MICROPROCESSOR INTERFACING

To dicuss the interface with 8080A and 6800 microprocessors, a common sample subroutine structure is used. The microprocessor starts the A/D, reads and stores the results of 16 successive conversions, then returns to the user's program. The 16 data bytes are stored in 16 successive memory locations. All Data and Addresses will be given in hexadecimal form. Software and hardware details are provided separately for each type of microprocessor.

4.1 Interfacing 8080 Microprocessor Derivatives (8048, 8085)

This converter has been designed to directly interface with derivatives of the 8080 microprocessor. The A/D can be mapped into memory space (using standard memory address decoding for $\overline{CS}$ and the $\overline{MEMR}$ and $\overline{MEMW}$ strobes) or it can be controlled as an I/O device by using the $\overline{I/O}$ R and $\overline{I/O}$ W strobes and decoding the address bits A0 → A7 (or address bits A8 → A15 as they will contain the same 8-bit address information) to obtain the $\overline{CS}$ input. Using the I/O space provides 256 additional addresses and may allow a simpler 8-bit address decoder but the data can only be input to the accumulator. To make use of the additional memory reference instructions, the A/D should be mapped into memory space. An example of an A/D in I/O space is shown in *Figure 12*.

Functional Description (Continued)

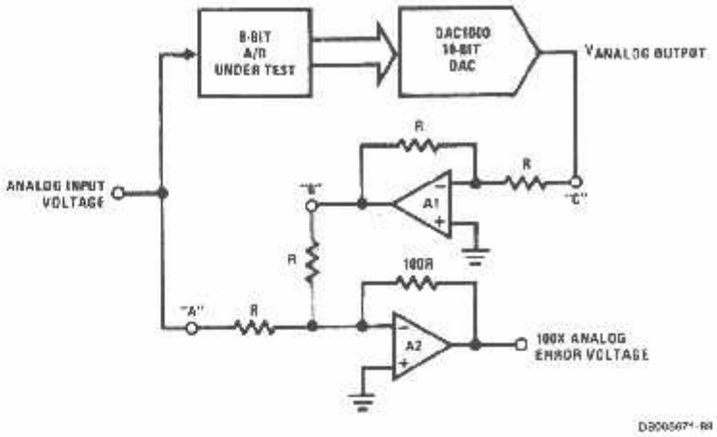


FIGURE 10. A/D Tester with Analog Error Output

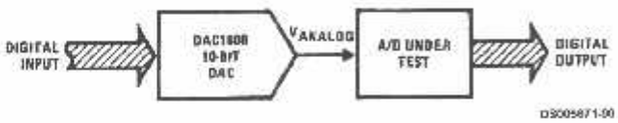


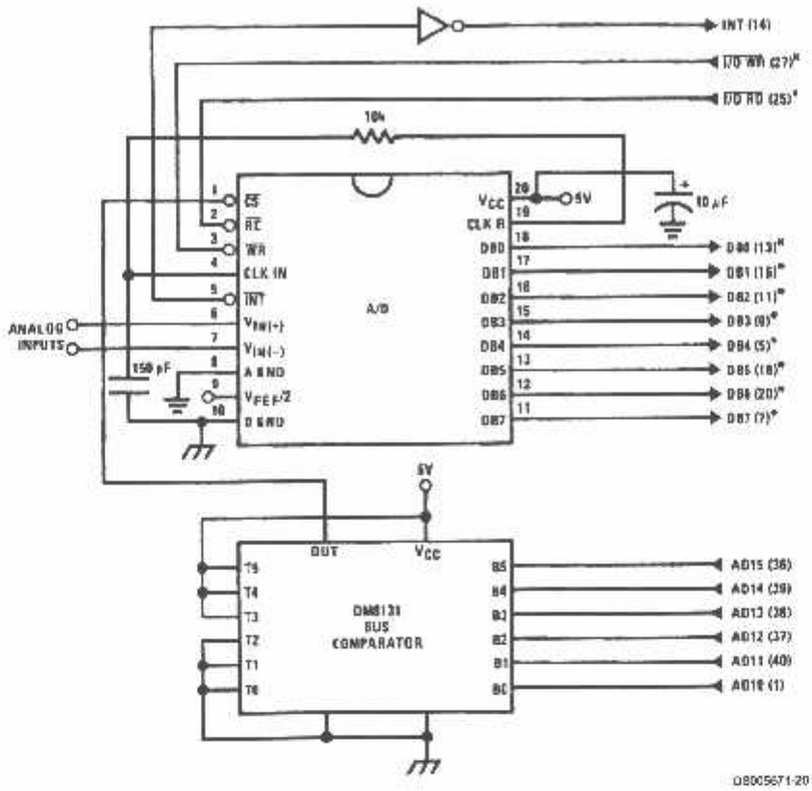
FIGURE 11. Basic "Digital" A/D Tester

TABLE 1. DECODING THE DIGITAL OUTPUT LEDs

HEX	BINARY				FRACTIONAL BINARY VALUE FOR		OUTPUT VOLTAGE CENTER VALUES WITH $V_{REF}/2$=2.560 V_{DC}	
					MS GROUP	LS GROUP	VMS GROUP (Note 15)	VLS GROUP (Note 15)
F	1	1	1	1	15/16	15/256	4.800	0.300
E	1	1	1	0	7/8	7/128	4.480	0.280
D	1	1	0	1	13/16	13/256	4.160	0.260
C	1	1	0	0	3/4	3/64	3.840	0.240
B	1	0	1	1	11/16	11/256	3.520	0.220
A	1	0	1	0	5/8	5/128	3.200	0.200
9	1	0	0	1	9/16	9/256	2.880	0.180
8	1	0	0	0	1/2	1/32	2.560	0.160
7	0	1	1	1	7/16	7/256	2.240	0.140
6	0	1	1	0	3/8	3/128	1.920	0.120
5	0	1	0	1	5/16	2/256	1.600	0.100
4	0	1	0	0	1/4	1/64	1.280	0.080
3	0	0	1	1	3/16	3/256	0.960	0.060
2	0	0	1	0	1/8	1/128	0.640	0.040
1	0	0	0	1	1/16	1/256	0.320	0.020
0	0	0	0	0			0	0

Note 15: Display Output=VMS Group + VLS Group

Functional Description (Continued)



D0005671-20

Note 16: *Pin numbers for the OP8228 system controller, others are INS8080A.

Note 17: Pin 23 of the INS8228 must be tied to +12V through a 1 kΩ resistor to generate the RST 7 instruction when an interrupt is acknowledged as required by the accompanying sample program.

FIGURE 12. ADC0801_INS8080A CPU Interface

Functional Description (Continued)

SAMPLE PROGRAM FOR *Figure 12* ADC0801–INS8080A CPU INTERFACE

```
0038    C3 00 03    RST 7:          JMP     LD DATA
  •       •           •
  •       •           •
0100    21 00 02    START:          LXI H 0200H         ; HL pair will point to
                                                        ; data storage locations
0103    31 00 04    RETURN:         LXI SP 0400H        ; Initialize stack pointer (Note 1)
0106    7D                          MOV A, L            ; Test # of bytes entered
0107    FE 0F                       CPI 0F H            ; If # = 16, JMP to
0109    CA 13 01                    JZ CONT             ; user program
010C    D3 E0                       OUT E0 H            ; Start A/D
010E    FB                          EI                  ; Enable interrupt
010F    00          LOOP:           NOP                 ; Loop until end of
0110    C3 0F 01                    JMP LOOP            ; conversion
0113      •           CONT:           •
  •       •           •               •
  •       •           (User program to    •
  •       •           process data)       •
  •       •           •               •
  •       •           •               •
0300    DB E0       LD DATA:        IN E0 H             ; Load data into accumulator
0302    77                          MOV M, A            ; Store data
0303    23                          INX H               ; Increment storage pointer
0304    C3 03 01                    JMP RETURN
```

DS005671-46

Note 18: The stack pointer must be dimensioned because a RST 7 instruction pushes the PC onto the stack.

Note 19: All address used were arbitrarily chosen.

The standard control bus signals of the 8080 $\overline{CS}$, $\overline{RD}$ and $\overline{WR}$) can be directly wired to the digital control inputs of the A/D and the bus timing requirements are met to allow both starting the converter and outputting the data onto the data bus. A bus driver should be used for larger microprocessor systems where the data bus leaves the PC board and/or must drive capacitive loads larger than 100 pF.

4.1.1 Sample 8080A CPU Interfacing Circuitry and Program

The following sample program and associated hardware shown in *Figure 12* may be used to input data from the converter to the INS8080A CPU chip set (comprised of the INS8080A microprocessor, the INS8228 system controller and the INS8224 clock generator). For simplicity, the A/D is controlled as an I/O device, specifically an 8-bit bi-directional port located at an arbitrarily chosen port address, E0. The TRI-STATE output capability of the A/D eliminates the need for a peripheral interface device, however address decoding is still required to generate the appropriate $\overline{CS}$ for the converter.

It is important to note that in systems where the A/D converter is 1-of-8 or less I/O mapped devices, no address decoding circuitry is necessary. Each of the 8 address bits (A0 to A7) can be directly used as $\overline{CS}$ inputs—one for each I/O device.

4.1.2 INS8048 Interface

The INS8048 interface technique with the ADC0801 series (see *Figure 13*) is simpler than the 8080A CPU interface. There are 24 I/O lines and three test input lines in the 8048. With these extra I/O lines available, one of the I/O lines (bit 0 of port 1) is used as the chip select signal to the A/D, thus eliminating the use of an external address decoder. Bus control signals $\overline{RD}$, $\overline{WR}$ and $\overline{INT}$ of the 8048 are tied directly to the A/D. The 16 converted data words are stored at on-chip RAM locations from 20 to 2F (Hex). The $\overline{RD}$ and $\overline{WR}$ signals are generated by reading from and writing into a dummy address, respectively. A sample interface program is shown below.

Functional Description (Continued)

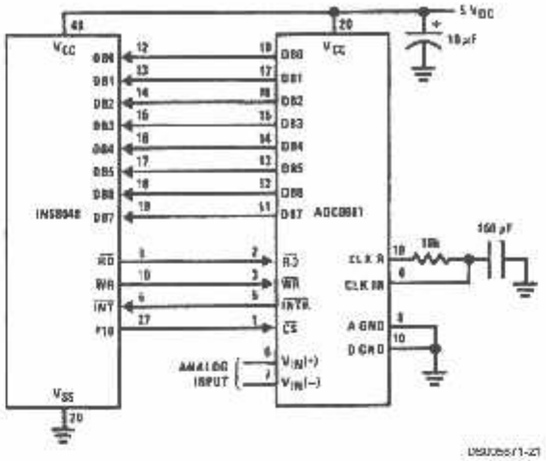


FIGURE 13. INS8048 Interface

SAMPLE PROGRAM FOR *Figure 13* INS8048 INTERFACE

```
04 10                  JMP     10H          ;Program starts at addr 10
                       ORG     3H
04 50                  JMP     50H          ;Interrupt jump vector
                       ORG     10H          ;Main program
99 FE                  ANL     P1, #0FEH    ;Chip select
81                     MOVX    A, @R1       ;Read in the 1st data
                                            ;to reset the intr
89 01        START:    ORL     P1, #1       ;Set port pin high
B8 20                  MOV     R0, #20H     ;Data address
B9 FF                  MOV     R1, #0FFH    ;Dummy address
BA 10                  MOV     R2, #10H     ;Counter for 16 bytes
23 FF        AGAIN:    MOV     A, #0FFH     ;Set ACC for intr loop
99 FE                  ANL     P1, #0FEH    ;Send CS (bit 0 of P1)
91                     MOVX    @R1, A       ;Send WR out
05                     EN      I            ;Enable interrupt
96 21        LOOP:     JNZ     LOOP         ;Wait for interrupt
EA 18                  DJNZ    R2, AGAIN    ;If 16 bytes are read
00                     NOP                  ;go to user's program
00                     NOP
                       ORG     50H
81           INDATA:   MOVX    A, @R1       ;Input data, CS still low
A0                     MOV     @R0, A       ;Store in memory
18                     INC     R0           ;Increment storage counter
89 01                  ORL     P1, #1       ;Reset CS signal
27                     CLR     A            ;Clear ACC to get out of
93                     RETR                 ;the interrupt loop
```

4.2 Interfacing the Z-80

The Z-80 control bus is slightly different from that of the 8080. General $\overline{RD}$ and $\overline{WR}$ strobes are provided and separate memory request, $\overline{MREQ}$, and I/O request, $\overline{IORQ}$, signals are used which have to be combined with the generalized strobes to provide the equivalent 808C signals. An advantage of operating the A/D in I/O space with the Z-80 is that the CPU will automatically insert one wait state (the $\overline{RD}$ and $\overline{WR}$ strobes are extended one clock period) to allow more time for the I/O devices to respond. Logic to map the A/D in I/O space is shown in *Figure 14*.

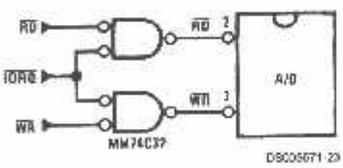


FIGURE 14. Mapping the A/D as an I/O Device for Use with the Z-80 CPU

Additional I/O advantages exist as software DMA routines are available and use can be made of the output data transfer which exists on the upper 8 address lines (A8 to

Functional Description (Continued)

A15) during I/O input instructions. For example, MUX channel selection for the A/D can be accomplished with this operating mode.

4.3 Interfacing 6800 Microprocessor Derivatives (6502, etc.)

The control bus for the 6800 microprocessor derivatives does not use the $\overline{RD}$ and $\overline{WR}$ strobe signals. Instead it employs a single R/$\overline{W}$ line and additional timing, if needed, can be derived fom the $\phi 2$ clock. All I/O devices are memory mapped in the 6800 system, and a special signal, VMA, indicates that the current address is valid. *Figure 15* shows an interface schematic where the A/D is memory mapped in the 6800 system. For simplicity, the $\overline{CS}$ decoding is shown using ½ DM8092. Note that in many 6800 systems, an already decoded $\overline{4/5}$ line is brought out to the common bus at pin 21. This can be tied directly to the $\overline{CS}$ pin of the A/D, provided that no other devices are addressed at HX ADDR: 4XXX or 5XXX.

The following subroutine performs essentially the same function as in the case of the 8080A interface and it can be callec from anywhere in the user's program.

In *Figure 16* the ADC0801 series is interfaced to the M6800 microprocessor through (the arbitrarily chosen) Port B of the MC6820 or MC6821 Peripheral Interface Adapter, (PIA). Here the $\overline{CS}$ pin of the A/D is grounded since the PIA is already memory mapped in the M6800 system and no $\overline{CS}$ decoding is necessary. Also notice that the A/D output data lines are connected to the microprocessor bus under program control through the PIA and therefore the A/D $\overline{RD}$ pin can be grounded.

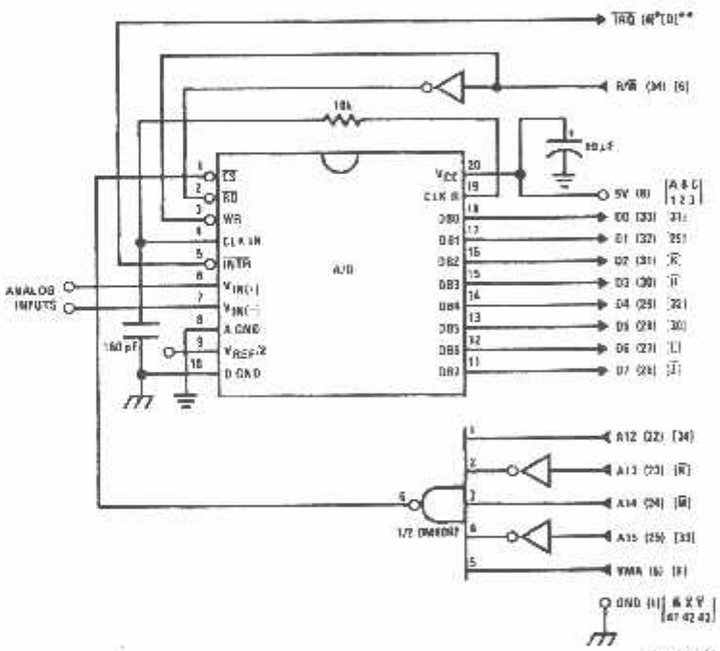
A sample interface program equivalent to the previous one is shown below *Figure 16*. The PIA Data and Control Registers of Port B are located at HEX addresses 8006 and 8007, respectively.

5.0 GENERAL APPLICATIONS

The following applications show some interesting uses for the A/D. The fact that one particular microprocessor is used is not meant to be restrictive. Each of these application circuits would have its counterpart using any microprocessor that is desired.

5.1 Multiple ADC0801 Series to MC6800 CPU Interface

To transfer analog data from several channels to a single microprocessor system, a multiple converter scheme presents several advantages over the conventional multiplexer single-converter approach. With the ADC0801 series, the differential inputs allow individual span adjustment for each channel. Furthermore, all analog input channels are sensed simultaneously, which essentially divides the microprocessor's total system servicing time by the number of channels, since all conversions occur simultaneously. This scheme is shown in *Figure 17*.



Note 20: Numbers in parentheses refer to MC6800 CPU pin out.

Note 21: Number or letters in brackets refer to standard M6800 system common bus code.

FIGURE 15. ADC0801-MC6800 CPU Interface

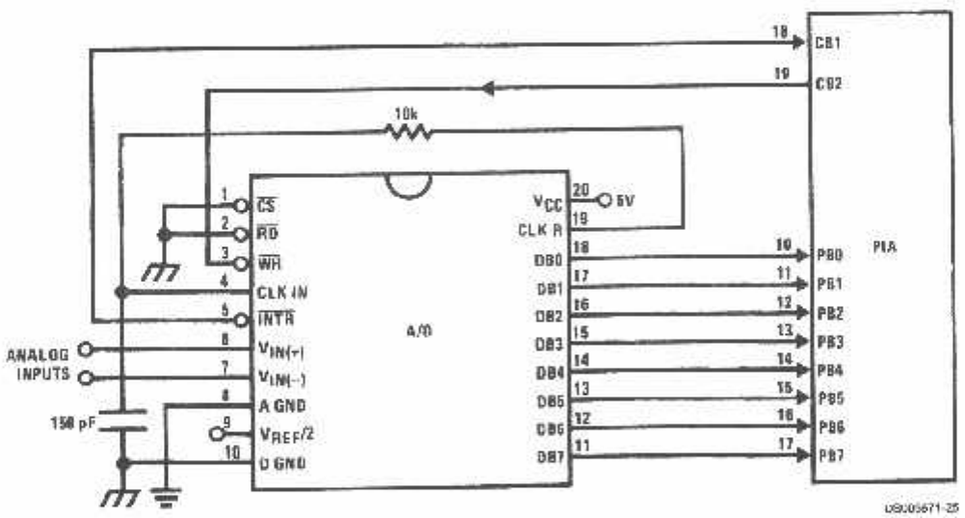
Functional Description (Continued)

SAMPLE PROGRAM FOR *Figure 15* ADC0801-MC6800 CPU INTERFACE

```
0010  DF 36     DATAIN  STX   TEMP2    ; Save contents of X
0012  CE 00 2C         LDX   #$002C     ; Upon IRQ low CPU
0015  FF FF F8         STX   $FFF8      ; jumps to 002C
0018  B7 50 00         STAA  $5000      ; Start ADC0801
001B  0E               CLI
001C  3E       CONVRT  WAI              ; Wait for interrupt
001D  DE 34            LDX   TEMP1
001F  8C 02 0F         CPX   #$020F     ; Is final data stored?
0022  27 14            BEQ   ENDP
0024  B7 50 00         STAA  $5000      ; Restarts ADC0801
0027  08               INX
0028  DF 34            STX   TEMP1
002A  20 F0            BRA   CONVRT
002C  DE 34     INTRPT  LDX   TEMP1
002E  B6 50 00         LDAA  $5000      ; Read data
0031  A7 00            STAA  X          ; Store it at X
0033  3B               RTI
0034  02 00     TEMP1   FDB   $0200      ; Starting address for
                                        ; data storage
0036  00 00     TEMP2   FDB   $0000
0038  CE 02 00  ENDP    LDX   #$0200     ; Reinitialize TEMP1
003B  DF 34            STX   TEMP1
003D  DE 36            LDX   TEMP2
003F  39               RTS              ; Return from subroutine
                                        ; To user's program
```

DS009671-A1

Note 22: In order for the microprocessor to service subroutines and interrupts, the stack pointer must be dimensioned in the user's program.



DS009671-25

FIGURE 16. ADC0801–MC6820 PIA Interface

Functional Description (Continued)

SAMPLE PROGRAM FOR *Figure 16* ADC0801–MC6820 PIA INTERFACE

```
0010  CE 00 38   DATAIN   LDX   #$0038   ; Upon IRQ low CPU
0013  FF FF F8           STX   $FFF8     ; jumps to 0038
0016  B6 80 06           LDAA  PIAORB    ; Clear possible IRQ flags
0019  4F                 CLRA
001A  B7 80 07           STAA  PIACRB
001D  B7 80 06           STAA  PIAORB    ; Set Port B as input
0020  0E                 CLI
0021  C6 34              LDAB  #$34
0023  86 3D              LDAA  #$3D
0025  F7 80 07   CONVRT  STAB  PIACRB    ; Starts ADC0801
0028  B7 80 07           STAA  PIACRB
002B  3E                 WAI             ; Wait for interrupt
002C  DE 40              LDX   TEMP1
002E  8C 02 0F           CPX   #$020F    ; Is final data stored?
0031  27 0F              BEQ   ENDP
0033  08                 INX
0034  DF 40              STX   TEMP1
0036  20 ED              BRA   CONVRT
0038  DE 40      INTRPT  LDX   TEMP1
003A  B6 80 06           LDAA  PIAORB    ; Read data in
003D  A7 00              STAA  X         ; Store it at X
003F  3B                 RTI
0040  02 00      TEMP1   FDB   $0200     ; Starting address for
                                         ; data storage
0042  CE 02 00   ENDP    LDX   #$0200    ; Reinitialize TEMP1
0045  DF 40              STX   TEMP1
0047  39                 RTS             ; Return from subroutine
                 PIAORB  EQU   $8006     ; To user's program
                 PIACRB  EQU   $8007
```

DS005671-A2

The following schematic and sample subroutine (DATA IN) may be used to interface (up to) 8 ADC0801's directly to the MC6800 CPU. This scheme can easily be extended to allow the interface of more converters. In this configuration the converters are (arbitrarily) located at HEX address 5000 in the MC6800 memory space. To save components, the clock signal is derived from just one RC pair on the first converter. This output drives the other A/Ds.

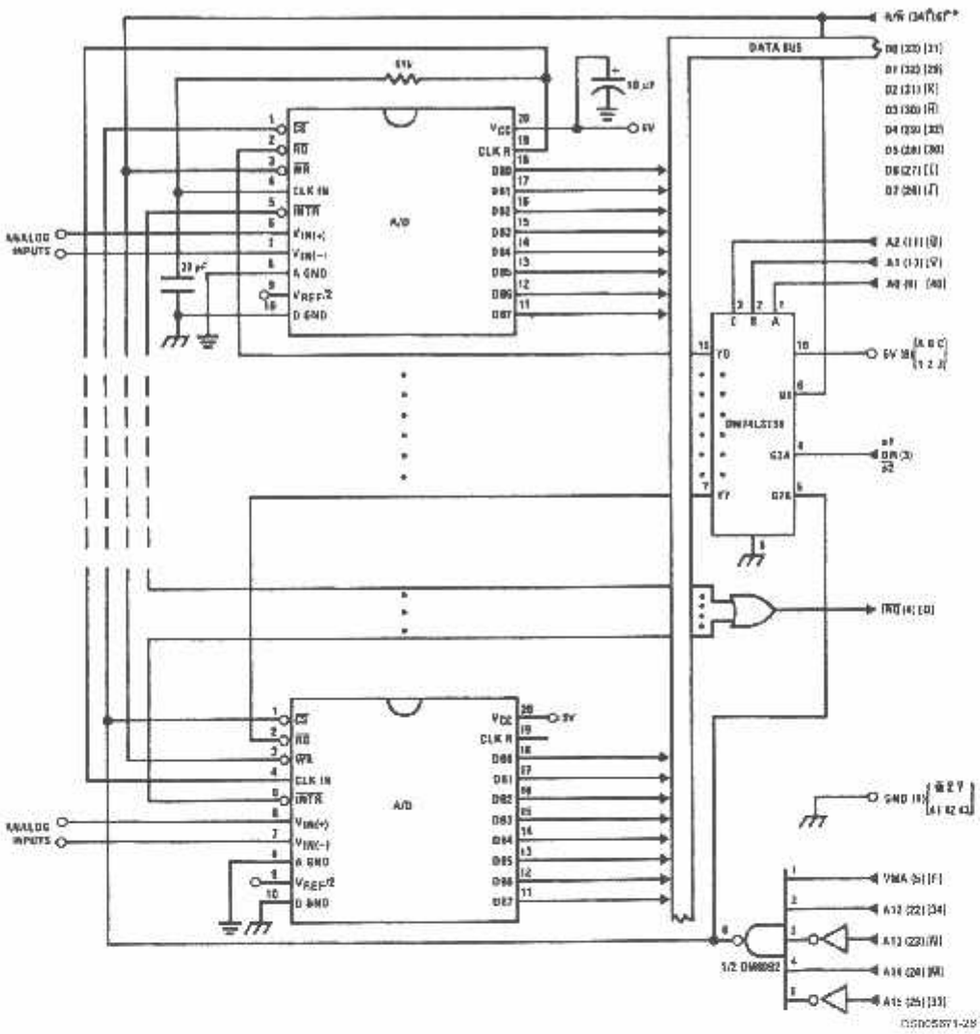
All the converters are started simultaneously with a STORE instruction at HEX address 5000. Note that any other HEX address of the form 5XXX will be decoded by the circuit, pulling all the $\overline{CS}$ inputs low. This can easily be avoided by using a more definitive address decoding scheme. All the interrupts are ORed together to insure that all A/Ds have completed their conversion before the microprocessor is interrupted.

The subroutine, DATA IN, may be called from anywhere in the user's program. Once called, this routine initializes the CPU, starts all the converters simultaneously and waits for the interrupt signal. Upon receiving the interrupt, it reads the converters (from HEX addresses 5000 through 5007) and stores the data successively at (arbitrarily chosen) HEX addresses 0200 to 0207, before returning to the user's program. All CPU registers then recover the original data they had before servicing DATA IN.

5.2 Auto-Zeroed Differential Transducer Amplifier and A/D Converter

The differential inputs of the ADC0801 series eliminate the need to perform a differential to single ended conversion for a differential transducer. Thus, one op amp can be eliminated since the differential to single ended conversion is provided by the differential input of the ADC0801 series. In general, a transducer preamp is required to take advantage of the full A/D converter input dynamic range.

Functional Description (Continued)



Note 23: Numbers in parentheses refer to MC6800 CPU pin out.

Note 24: Numbers of letters in brackets refer to standard M6800 system common bus code.

FIGURE 17. Interfacing Multiple A/Ds in an MC6800 System

Functional Description (Continued)

SAMPLE PROGRAM FOR *Figure 17* INTERFACING MULTIPLE A/D's IN AN MC6800 SYSTEM

ADDRESS	HEX CODE		MNEMONICS		COMMENTS
0010	DF 44	DATAIN	STX	TEMP	; Save Contents of X
0012	CE 00 2A		LDX	#$002A	; Upon $\overline{IRQ}$ LOW CPU
0015	FF FF F8		STX	$FFF8	; Jumps to 002A
0018	B7 50 00		STAA	$5000	; Starts all A/D's
001B	0E		CLI		
001C	3E		WAI		; Wait for interrupt
001D	CE 50 00		LDX	#$5000	
0020	DF 40		STX	INDEX1	; Reset both INDEX
0022	CE 02 00		LDX	#$0200	; 1 and 2 to starting
0025	DF 42		STX	INDEX2	; addresses
0027	DE 44		LDX	TEMP	
0029	39		RTS		; Return from subroutine
002A	DE 40	INTRPT	LDX	INDEX1	; INDEX1 → X
002C	A6 00		LDAA	X	; Read data in from A/D at X
002E	08		INX		; Increment X by one
002F	DF 40		STX	INDEX1	; X → INDEX1
0031	DE 42		LDX	INDEX2	; INDEX2 → X

DS005671-A3

SAMPLE PROGRAM FOR *Figure 17* INTERFACING MULTIPLE A/D's IN AN MC6800 SYSTEM

ADDRESS	HEX CODE		MNEMONICS		COMMENTS
0033	A7 00		STAA	X	; Store data at X
0035	8C 02 07		CPX	#$0207	; Have all A/D's been read?
0038	27 05		BEQ	RETURN	; Yes: branch to RETURN
003A	08		INX		; No: increment X by one
003B	DF 42		STX	INDEX2	; X → INDEX2
003D	20 EB		BRA	INTRPT	; Branch to 002A
003F	3B	RETURN	RTI		
0040	50 00	INDEX1	FDB	$5000	; Starting address for A/D
0042	02 00	INDEX2	FDB	$0200	; Starting address for data storage
0044	00 00	TEMP	FDB	$0000	

DS005671-A4

Note 25: In order for the microprocessor to service subroutines and interrupts, the stack pointer must be dimensioned in the user's program.

For amplification of DC input signals, a major system error is the input offset voltage of the amplifiers used for the preamp. *Figure 18* is a gain of 100 differential preamp whose offset voltage errors will be cancelled by a zeroing subroutine which is performed by the INS8080A microprocessor system. The total allowable input offset voltage error for this preamp is only 50 µV for ¼ LSB error. This would obviously require very precise amplifiers. The expression for the differential output voltage of the preamp is:

$$V_O = \underbrace{[V_{IN}(+) - V_{IN}(-)]}_{\text{SIGNAL}} \underbrace{\left[1 + \frac{2R2}{R1}\right]}_{\text{GAIN}} +$$

$$\underbrace{(V_{OS_2} - V_{OS_1} - V_{OS_3} \pm I_X R_X)}_{\text{DC ERROR TERM}} \underbrace{\left(1 + \frac{2R2}{R1}\right)}_{\text{GAIN}}$$

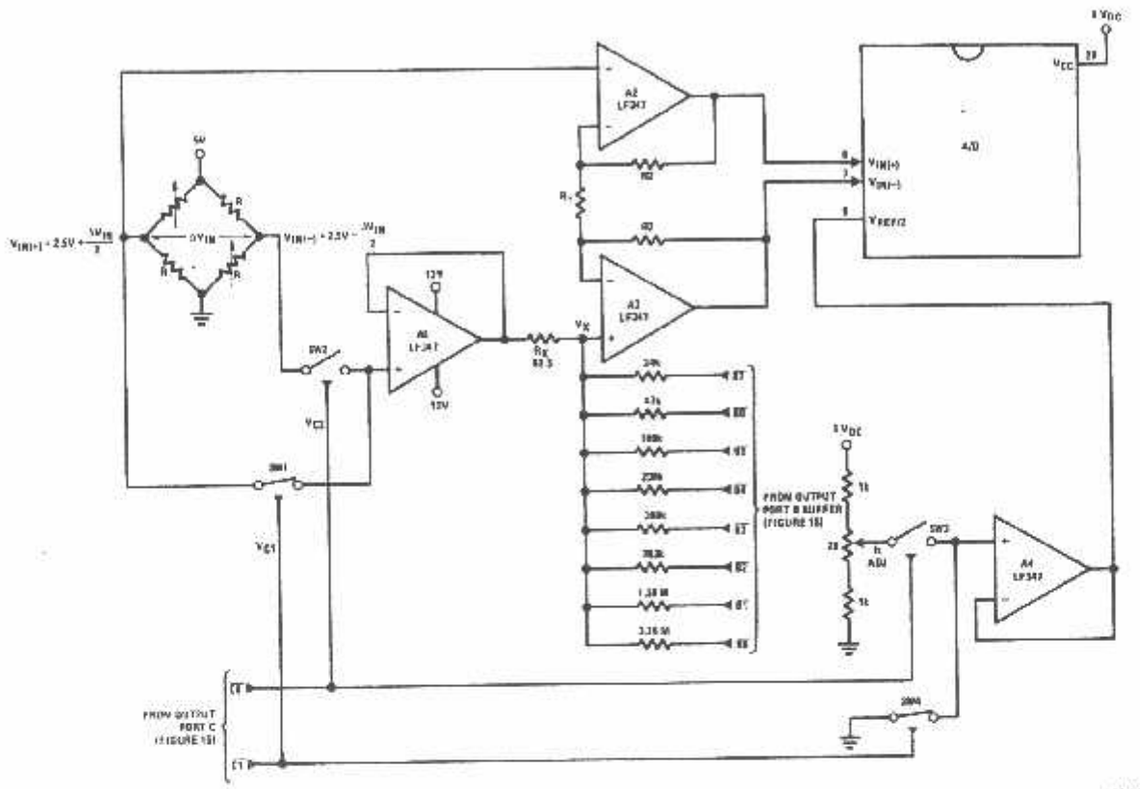
where I_X is the current through resistor R_X. All of the offset error terms can be cancelled by making $\pm I_X R_X = V_{OS1} + V_{OS3} - V_{OS2}$. This is the principle of this auto-zeroing scheme.

The INS8080A uses the 3 I/O ports of an INS8255 Programable Peripheral Interface (PPI) to control the auto zeroing and input data from the ADC0801 as shown in *Figure 18*. The PPI is programmed for basic I/O operation (mode 0) with Port A being an input port and Ports B and C being output ports. Two bits of Port C are used to alternately open or close the 2 switches at the input of the preamp. Switch SW1 is closed to force the preamp's differential input to be zero during the zeroing subroutine and then opened and SW2 is then closed for conversion of the actual differential input signal. Using 2 switches in this manner eliminates concern for the ON resistance of the switches as they must conduct only the input bias current of the input amplifiers.

Output Port B is used as a successive approximation register by the 8080 and the binary scaled resistors in series with each output bit create a D/A converter. During the zeroing subroutine, the voltage at V_x increases or decreases as required to make the differential output voltage equal to zero. This is accomplished by ensuring that the voltage at the output of A1 is approximately 2.5V so that a logic "1" (5V) on

Functional Description (Continued)

any output of Port B will source current into node V_X thus raising the voltage at V_X and making the output differential more negative. Conversely, a logic "0" (0V) will pull current out of node V_X and decrease the voltage, causing the differential output to become more positive. For the resistor values shown, V_X can move ±12 mV with a resolution of 50 µV, which will null the offset error term to ¼ LSB of full-scale for the ADC0801. It is important that the voltage levels that drive the auto-zero resistors be constant. Also, for symmetry, a logic swing of 0V to 5V is convenient. To achieve this, a CMOS buffer is used for the logic output signals of Port B and this CMOS package is powered with a stable 5V source. Buffer amplifier A1 is necessary so that it can source or sink the D/A output current.



DS005671-01

Note 26: R2 = 49.5 R1

Note 27: Switches are LMC13334 CMOS analog switches.

Note 28: The 9 resistors used in the auto-zero section can be ±5% tolerance

FIGURE 18. Gain of 100 Differential Transducer Preamp

Functional Description (Continued)

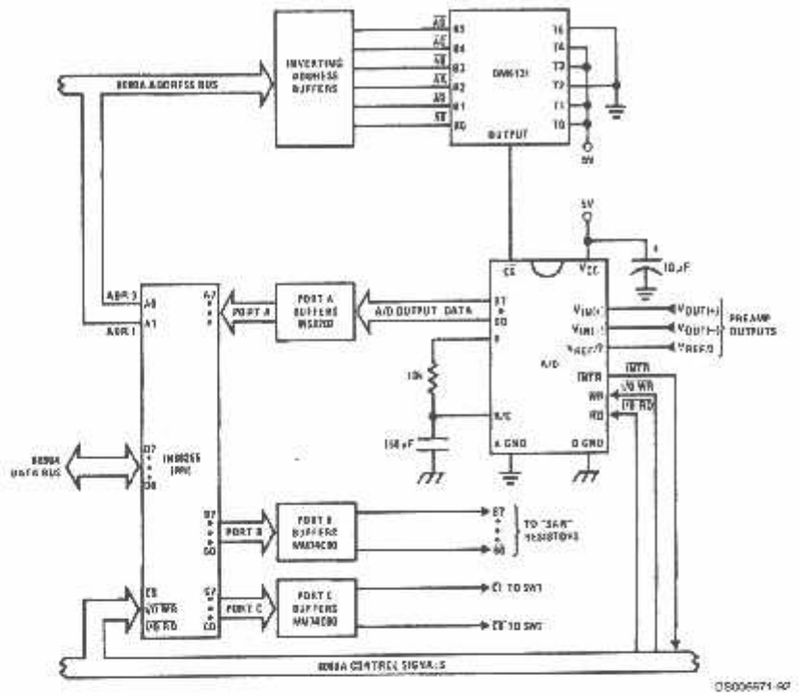


FIGURE 19. Microprocessor Interface Circuitry for Differential Preamp

A flow chart for the zeroing subroutine is shown in *Figure 20*. It must be noted that the ADC0801 series will output an all zero code when it converts a negative input [$V_{IN}(-) \geq V_{IN}(+)$]. Also, a logic inversion exists as all of the I/O ports are buffered with inverting gates.

Basically, if the data read is zero, the differential output voltage is negative, so a bit in Port B is cleared to pull V_X more negative which will make the output more positive for the next conversion. If the data read is not zero, the output voltage is positive so a bit in Port B is set to make V_X more positive and the output more negative. This continues for 8 approximations and the differential output eventually converges to within 5 mV of zero.

The actual program is given in *Figure 21*. All addresses used are compatible with the BLC 80/10 microcomputer system. In particular:

Port A and the ADC0801 are at port address E4

Port B is at port address E5

Port C is at port address E6

PPI control word port is at port address E7

Program Counter automatically goes to ADDR:3C3D upon acknowledgement of an interrupt from the ADC0801

5.3 Multiple A/D Converters in a Z-80 Interrupt Driven Mode

In data acquisition systems where more than one A/D converter (or other peripheral device) will be interrupting program execution of a microprocessor, there is obviously a need for the CPU to determine which device requires servicing. *Figure 22* and the accompanying software is a method of determining which of 7 ADC0801 converters has completed a conversion ($\overline{INTR}$ asserted) and is requesting an interrupt. This circuit allows starting the A/D converters in any sequence, but will input and store valid data from the converters with a priority sequence of A/D 1 being read first, A/D 2 second, etc., through A/D 7 which would have the lowest priority for data being read. Only the converters whose INT is asserted will be read.

The key to decoding circuitry is the DM74LS373, 8-bit D type flip-flop. When the Z-80 acknowledges the interrupt, the program is vectored to a data input Z-80 subroutine. This subroutine will read a peripheral status word from the DM74LS373 which contains the logic state of the $\overline{INTR}$ outputs of all the converters. Each converter which initiates an interrupt will place a logic "0" in a unique bit position in the status word and the subroutine will determine the identity of the converter and execute a data read. An identifier word (which indicates which A/D the data came from) is stored in the next sequential memory location above the location of the data so the program can keep track of the identity of the data entered.

Functional Description (Continued)

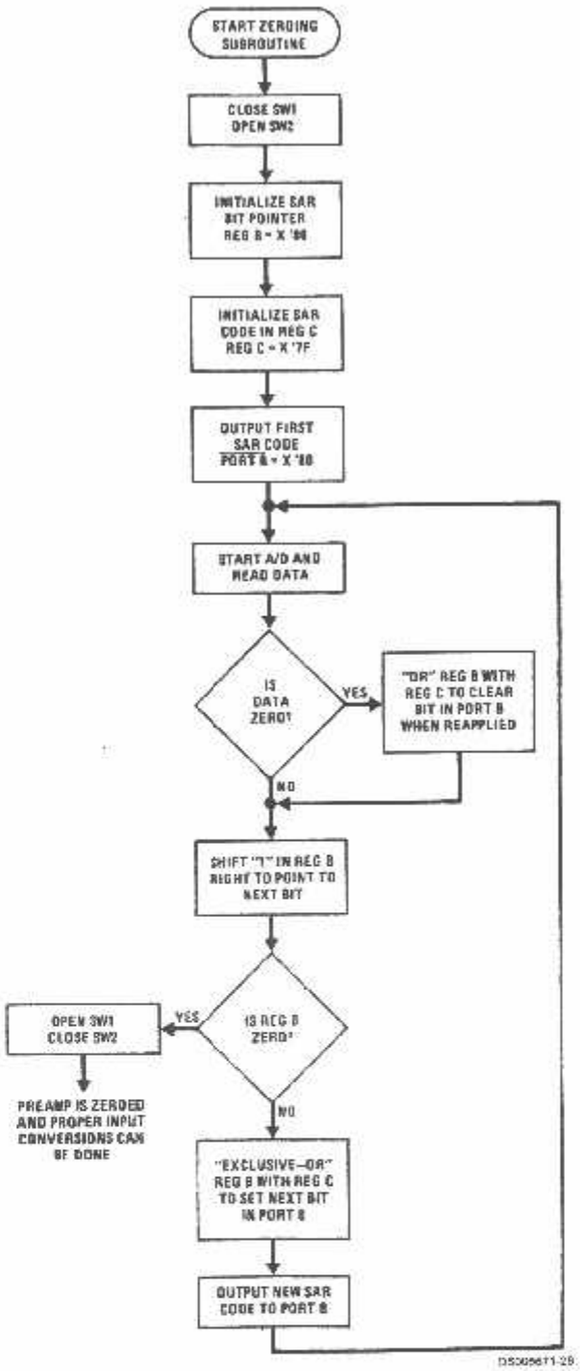


FIGURE 20. Flow Chart for Auto-Zero Routine

Functional Description (Continued)

```
3D00  3E90     MVI 90
3D02  D3E7     Out Control Port                ;Program PPI
3D04  2601     MVI H 01        Auto-Zero Subroutine
3D06  7C       MOV A,H
3D07  D3E6     OUT C                          ;Close SW1 open SW2
3D09  0680     MVI B 80                       ;Initialize SAR bit pointer
3D0B  3E7F     MVI A 7F                       ;Initialize SAR code
3D0D  4F       MOV C,A         Return
3D0E  D3E5     OUT B                          ;Port B = SAR code
3D10  31AA3D   LXI SP 3DAA     Start          ;Dimension stack pointer
3D13  D3E4     OUT A                          ;Start A/D
3D15  FB       IE
3D16  00       NOP             Loop           ;Loop until INT asserted
3D17  C3163D   JMP Loop
3D1A  7A       MOV A,D         Auto-Zero
3D1B  C600     ADI 00
3D1D  CA2D3D   JZ Set C                       ;Test A/D output data for zero
3D20  78       MOV A,B         Shift B
3D21  F600     ORI 00                         ;Clear carry
3D23  1F       RAR                            ;Shift "1" in B right one place
3D24  FE00     CPI 00                         ;Is B zero? If yes last
3D26  CA373D   JZ Done                        ;approximation has been made
3D29  47       MOV B,A
3D2A  C3333D   JMP New C
3D2D  79       MOV A,C         Set C
3D2E  B0       ORA B                          ;Set bit in C that is in same
3D2F  4F       MOV C,A                        ;position as "1" in B
3D30  C3203D   JMP Shift B
3D33  A9       XRA C           New C          ;Clear bit in C that is in
3D34  C30D3D   JMP Return                     ;same position as "1" in B
3D37  47       MOV B,A         Done           ;then output new SAR code.
3D38  7C       MOV A,H                        ;Open SW1, close SW2 then
3D39  EE03     XRI 03                         ;proceed with program. Preamp
3D3B  D3E6     OUT C                          ;is now zeroed.
3D3D           •               Normal
               •
               •
               Program for processing
               proper data values
3C3D  DBE4     IN A            Read A/D Subroutine  ;Read A/D data
3C3F  EEFF     XRI FF                         ;Invert data
3C41  57       MOV D,A
3C42  78       MOV A,B                        ;Is B Reg = 0? If not stay
3C43  E6FF     ANI FF                         ;in auto zero subroutine
3C45  C21A3D   JNZ Auto-Zero
3C48  C33D3D   JMP Normal
```

L9005671-45

Note 29: All numerical values are hexadecimal representations.

FIGURE 21. Software for Auto-Zeroed Differential A/D

5.3 Multiple A/D Converters in a Z-80 Interrupt Driven Mode (Continued)

The following notes apply:

- It is assumed that the CPU automatically performs a RST 7 instruction when a valid interrupt is acknowledged (CPU is in interrupt mode 1). Hence, the subroutine starting address of X0038.
- The address bus from the Z-80 and the data bus to the Z-80 are assumed to be inverted by bus drivers.
- A/D data and identifying words will be stored in sequential memory locations starting at the arbitrarily chosen address X 3E00.
- The stack pointer must be dimensioned in the main program as the RST 7 instruction automatically pushes the PC onto the stack and the subroutine uses an additional 6 stack addresses.
- The peripherals of concern are mapped into I/O space with the following port assignments:

Functional Description (Continued)

HEX PORT ADDRESS	PERIPHERAL
00	MM74C374 8-bit flip-flop
01	A/D 1
02	A/D 2
03	A/D 3
04	A/D 4
05	A/D 5
06	A/D 6
07	A/D 7

This port address also serves as the A/D identifying word in the program.

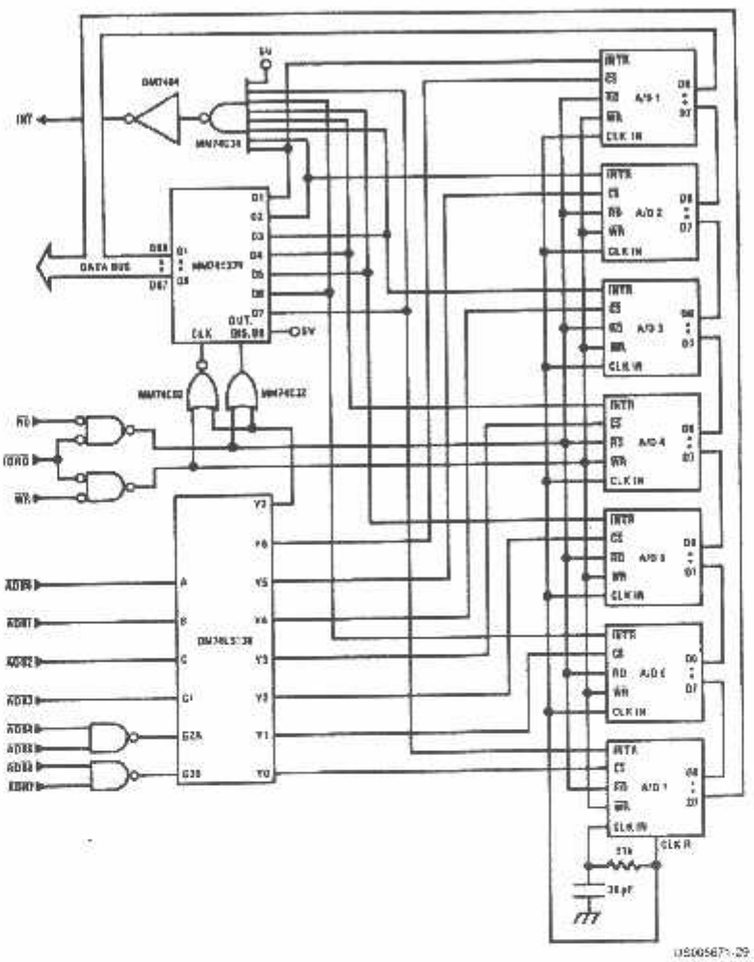


FIGURE 22. Multiple A/Ds with Z-80 Type Microprocessor

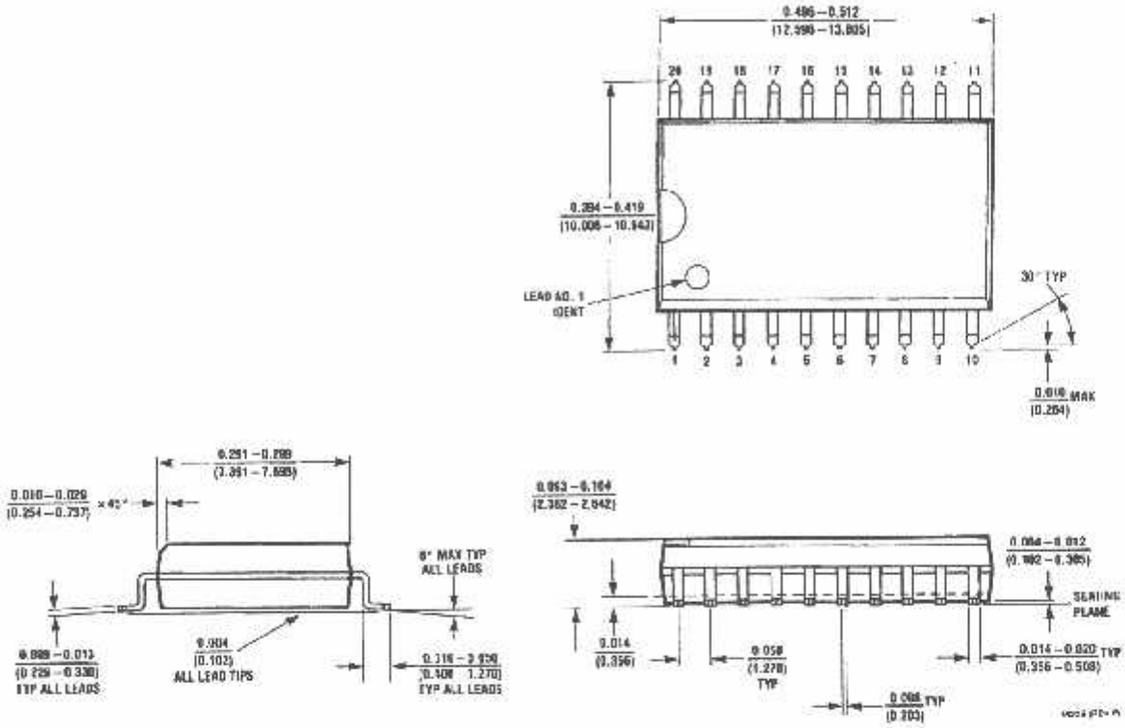
Functional Description (Continued)

INTERRUPT SERVICING SUBROUTINE

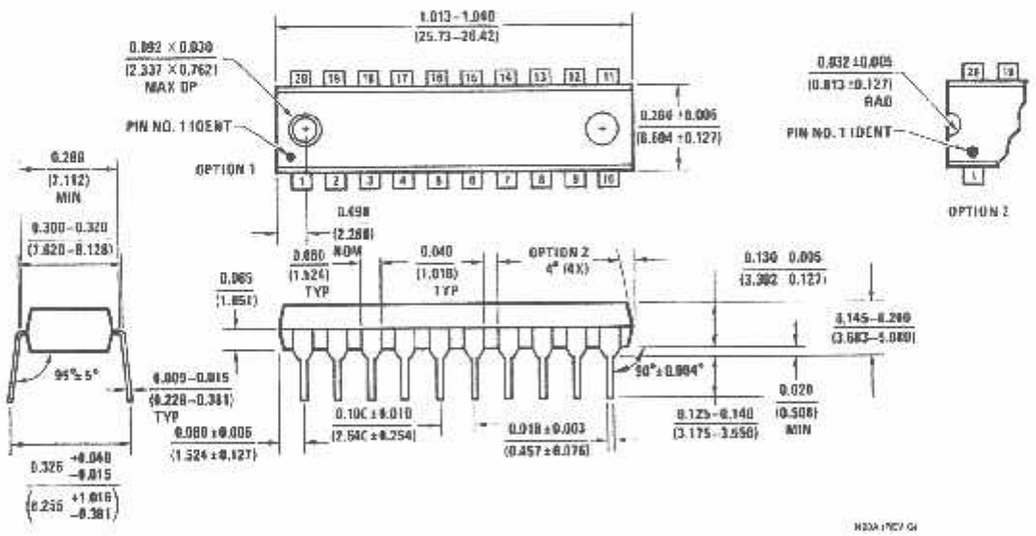
LOC	OBJ CODE		SOURCE STATEMENT	COMMENT
0038	E5		PUSH HL	;Save contents of all registers affected by
0039	C5		PUSH BC	;this subroutine.
003A	F5		PUSH AF	;Assumed INT mode 1 earlier set.
003B	21 00 3E		LD (HL),X3E00	;Initialize memory pointer where data will be stored.
003E	0E 01		LD C, X01	;C register will be port ADDR of A/D converters.
0040	D300		OUT X00, A	;Load peripheral status word into 8-bit latch.
0042	DB00		IN A, X00	;Load status word into accumulator.
0044	47		LD B,A	;Save the status word.
0045	79	TEST	LD A,C	;Test to see if the status of all A/D's have
0046	FE 08		CP, X08	;been checked. If so, exit subroutine
0048	CA 60 00		JPZ, DONE	
004B	78		LD A,B	;Test a single bit in status word by looking for
004C	1F		RRA	;a "1" to be rotated into the CARRY (an $\overline{INT}$
004D	47		LD B,A	;is loaded as a "1"). If CARRY is set then load
004E	DA 5500		JPC, LOAD	;contents of A/D at port ADDR in C register.
0051	0C	NEXT	INC C	;If CARRY is not set, increment C register to point
0052	C3 4500		JP,TEST	;to next A/D, then test next bit in status word.
0055	ED 78	LOAD	IN A, (C)	;Read data from interrupting A/D and invert
0057	EE FF		XOR FF	;the data.
0059	77		LD (HL),A	;Store the data
005A	2C		INC L	
005B	71		LD (HL),C	;Store A/D identifier (A/D port ADDR).
005C	2C		INC L	
005D	C3 51 00		JP,NEXT	;Test next bit in status word.
0060	F1	DONE	POP AF	;Re-establish all registers as they were
0061	C1		POP BC	;before the interrupt.
0062	E1		POP HL	
0063	C9		RET	;Return to original program

DS005671-A8

Physical Dimensions inches (millimeters) unless otherwise noted



SO Package (M)
Order Number ADC0802LCWM or ADC0804LCWM
NS Package Number M20B



Molded Dual-In-Line Package (N)
Order Number ADC0801LCN, ADC0802LCN,
ADC0803LCN, ADC0804LCN or ADC0805LCN
NS Package Number N20A

Notes

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CD4016BC
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General Description

The CD4016BC is a quad bilateral switch intended for the transmission or multiplexing of analog or digital signals. It is pin-for-pin compatible with CD4066BC.

Features

- Wide supply voltage range: 3V to 15V
- Wide range of digital and analog switching: ±7.5 V_{PEAK}
- "ON" Resistance for 15V operation: 400Ω (typ)
- Matched "ON" Resistance over 15V signal input:
  ΔR_{ON} = 10Ω (typ)
- High degree of linearity:
  0.4% distortion (typ)
  @ f_{IS} = 1 kHz, V_{IS} = 5 V_{p-p},
  $V_{DD}-V_{SS}$ = 10V, R_L = 10 kΩ
- Extremely low "OFF" switch leakage:
  0.1 nA (typ.)
  @ $V_{DD} - V_{SS}$ = 10V
  T_A = 25°C
- Extremely high control input impedance: 10^{12}Ω (typ)
- Low crosstalk between switches:
  −50 dB (typ.)
  @ f_{IS} = 0.9 MHz, R_L = 1 kΩ
- Frequency response, switch "ON": 40 MHz (typ)

Applications

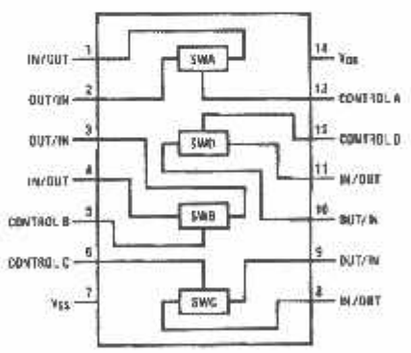
- Analog signal switching/multiplexing
  - Signal gating
  - Squelch control
  - Chopper
  - Modulator/Demodulator
  - Commutating switch
- Digital signal switching/multiplexing
- CMOS logic implementation
- Analog-to-digital/digital-to-analog conversion
- Digital control of frequency, impedance, phase and analog-signal gain

Ordering Code:

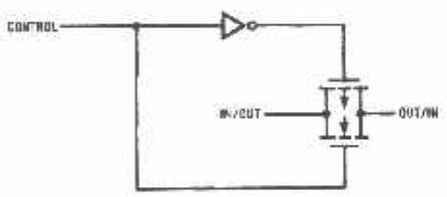
Order Number	Package Number	Package Description
CD4016BCM	M14A	14-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-012, 0.150" Narrow
CD4016BCN	N14A	14-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300" Wide

Devices also available in Tape and Reel. Specify by appending the letter suffix "X" to the ordering code.

Connection Diagram



Schematic Diagram



Absolute Maximum Ratings (Note 1)

(Note 2)

V_{DD} Supply Voltage	−0.5V to +18V
V_{IN} Input Voltage	−0.5V to V_{DD} + 0.5V
T_S Storage Temperature Range	−65°C to +150°C
Power Dissipation (P_D)	
Dual-In-Line	700 mW
Small Outline	500 mW
Lead Temperature	
(Soldering, 10 seconds)	260°C

Recommended Operating Conditions (Note 2)

V_{DD} Supply Voltage	3V to 15V
V_{IN} Input Voltage	0V to V_{DD}
T_A Operating Temperature Range	−55°C to +125°C

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. They are not meant to imply that the devices should be operated at these limits. The tables of "Recommended Operating Conditions" and "Electrical Characteristics" provide conditions for actual device operation.

Note 2: V_{SS} = 0V unless otherwise specified.

DC Electrical Characteristics (Note 2)

Symbol	Parameter	Conditions	−55°C		25°C			+125°C		Units
			Min	Max	Min	Typ	Max	Min	Max	
I_{DD}	Quiescent Device Current	V_{DD} = 5V, V_{IN} = V_{DD} or V_{SS}		0.25		0.01	0.25		7.5	µA
		V_{DD} = 10V, V_{IN} = V_{DD} or V_{SS}		0.5		0.01	0.5		15	µA
		V_{DD} = 15V, V_{IN} = V_{DD} or V_{SS}		1.0		0.01	1.0		30	µA
Signal Inputs and Outputs										
R_{ON}	"ON" Resistance	R_L = 10kΩ to (V_{DD} − V_{SS})/2								
		V_C = V_{DD}, V_{IS} = V_{SS} or V_{DD}								
		V_{DD} = 10V		600		250	660		960	Ω
		V_{DD} = 15V		360		200	400		600	Ω
		R_L = 10kΩ to (V_{DD} − V_{SS})/2								
		V_C = V_{DD}								
		V_{DD} = 10V, V_{IS} = 4.75 to 5.25V		1370		850	2000		2600	Ω
		V_{DD} = 15V, V_{IS} = 7.25 to 7.75V		775		400	850		1230	Ω
ΔR_{ON}	Δ"ON" Resistance Between any 2 of 4 Switches (In Same Package)	R_L = 10kΩ to (V_{DD} − V_{SS})/2								
		V_C = V_{DD}, V_{IS} = V_{SS} to V_{DD}								
		V_{DD} = 10V				15				Ω
		V_{DD} = 15V				10				Ω
I_{IS}	Input or Output Leakage Switch "OFF"	V_C = 0, V_{DD} = 15V		±50		±0.1	±50		±500	nA
		V_{IS} = 0V or 15V,								
		V_{OS} = 15V or 0V								
Control Inputs										
V_{ILC}	LOW Level Input Voltage	V_{IS} = V_{SS} and V_{DD}								
		V_{OS} = V_{DD} and V_{SS}								
		I_{IS} = ±10 µA								
		V_{DD} = 5V		0.9			0.7		0.5	V
		V_{DD} = 10V		0.9			0.7		0.5	V
		V_{DD} = 15V		0.9			0.7		0.5	V
V_{IHC}	HIGH Level Input Voltage	V_{DD} = 5V	3.5		3.5			3.5		V
		V_{DD} = 10V	7.0		7.0			7.0		V
		V_{DD} = 15V	11.0		11.0			11.0		V
		(Note 3) and Table 1								
I_{IN}	Input Current	V_{CC} − V_{SS} = 15V		±0.1		$+10^{-5}$	+0.1		±1.0	µA
		$V_{DD} \geq V_{IS} \geq V_{SS}$								
		$V_{DD} \geq V_C \geq V_{SS}$								

Note 3: If the switch input is held at V_{DD}, V_{IHC} = the control input level that will cause the switch output to meet the standard "B" series V_{OH} and I_{OH} output levels. If the analog switch input is connected to V_{SS}, V_{IHC} is the control input level — which allows the switch to sink standard "B" series I_{OH} HIGH level current, and still maintain a $V_{OL} \leq$ "B" series. These currents are shown in Table 1

AC Electrical Characteristics (Note 4)

$T_A = 25°C$, $t_r = t_f = 20$ ns and $V_{SS} = 0V$ unless otherwise specified

Symbol	Parameter	Conditions	Min	Typ	Max	Units
t_{PHL}, t_{PLH}	Propagation Delay Time	$V_C = V_{DD}$, $C_L = 50$ pF, (Figure 1)				
	Signal Input to Signal Output	$R_L = 200k$				
		$V_{DD} = 5V$		56	100	ns
		$V_{DD} = 10V$		27	50	ns
		$V_{DD} = 15V$		20	40	ns
t_{PZH}, t_{PZL}	Propagation Delay Time	$R_L = 1.0$ kΩ, $C_L = 50$ pF, (Figure 2, Figure 3)				
	Control Input to Signal	$V_{DD} = 5V$		20	50	ns
	Output HIGH Impedance to	$V_{DD} = 10V$		18	40	ns
	Logical Level	$V_{DD} = 15V$		17	35	ns
t_{PHZ}, t_{PLZ}	Propagation Delay Time	$R_L = 1.0$ kΩ, $C_L = 50$ pF, (Figure 2, Figure 3)				
	Control Input to Signal	$V_{DD} = 5V$		15	40	ns
	Output Logical Level to	$V_{DD} = 10V$		11	25	ns
	HIGH Impedance	$V_{DD} = 15V$		10	22	ns
	Sine Wave Distortion	$V_C = V_{DD} = 5V$, $V_{SS} = -5$		0.4		%
		$R_L = 10$ kΩ, $V_{IS} = 5$ V_{P-P}, f = 1 kHz				
		(Figure 4)				
	Frequency Response — Switch	$V_C = V_{DD} = 5V$, $V_{SS} = -5V$,		40		MHz
	"ON" (Frequency at −3 dB)	$R_L = 1$ kΩ, $V_{IS} = 5$ V_{P-P},				
		20 Log_{10} V_{OS}/V_{OS} (1 kHz) = dB,				
		(Figure 4)				
	Feedthrough — Switch "OFF"	$V_{DD} = 5V$, $V_C = V_{SS} = -5V$,		1.25		MHz
	(Frequency at −50 dB)	$R_L = 1$ kΩ, $V_{IS} = 5$ V_{P-P},				
		20 Log_{10} (V_{OS}/V_{IS}) = −50 dB,				
		(Figure 4)				
	Crosstalk Between Any Two	$V_{DD} = V_{C(A)} = 5V$, $V_{SS} = V_{C(B)} = -5V$		0.9		MHz
	Switches (Frequency at −50 dB)	$R_L = 1$ kΩ$V_{IS(A)} = 5$ V_{P-P},				
		20 Log_{10} ($V_{OS(B)}/V_{OS(A)}$) = −50 dB,				
		(Figure 5)				
	Crosstalk; Control Input to	$V_{DD} = 10V$, $R_L = 10$ kΩ		150		mV_{P-P}
	Signal Output	$R_{IN} = 1$ kΩ, $V_{CC} = 10V$ Square Wave,				
		$C_L = 50$ pF (Figure 6)				
	Maximum Control Input	$R_L = 1$ kΩ, $C_L = 50$ pF, (Figure 7)				
		$V_{CS(f)} = ½ V_{CS}$ (1 kHz)				
		$V_{CC} = 5V$		6.5		MHz
		$V_{CC} = 10V$		8.0		MHz
		$V_{CC} = 15V$		9.0		MHz
C_{IS}	Signal Input Capacitance			4		pF
C_{OS}	Signal Output Capacitance	$V_{CC} = 10V$		4		pF
C_{IOS}	Feedthrough Capacitance	$V_C = 0V$		0.2		pF
C_{IN}	Control Input Capacitance			5	7.5	pF

Note 4: AC Parameters are guaranteed by DC correlated testing.

Note 5: These devices should not be connected to circuits with the power "ON".

Note 6: In all cases, there is approximately 5 pF of probe and jig capacitance on the output; however, this capacitance is included in C_L wherever it is specified.

Note 7: V_{IS} is the voltage at the input pin and V_{OS} is the voltage at the output pin. V_C is the voltage at the control input.

AC Test Circuits and Switching Time Waveforms

FIGURE 1. t_{PLH}, t_{PLH} Propagation Delay Time Control to Signal Output

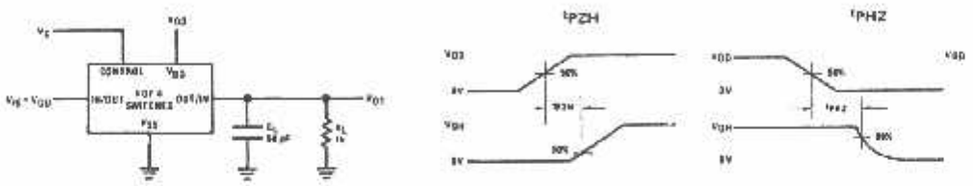


FIGURE 2. t_{PZH}, t_{PHZ} Propagation Delay Time Control to Signal Output

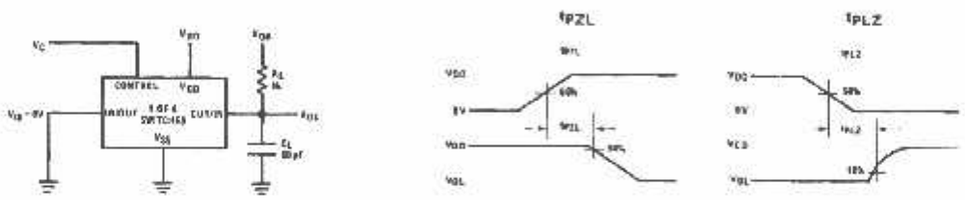
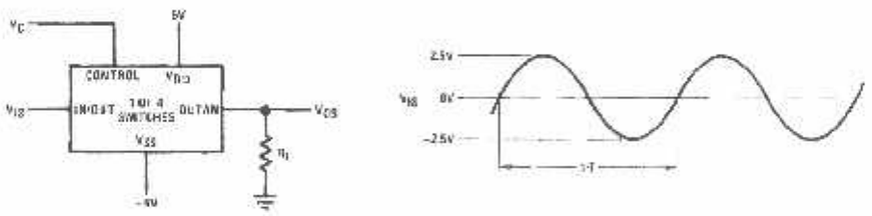


FIGURE 3. t_{PZH}, t_{PHZ} Propagation Delay Time Control to Signal Output



$V_C = V_{DD}$ for distortion and frequency response tests

$V_C = V_{SS}$ for feedthrough test

FIGURE 4. Sine Wave Distortion, Frequency Response and Feedthrough

AC Test Circuits and Switching Time Waveforms (Continued)

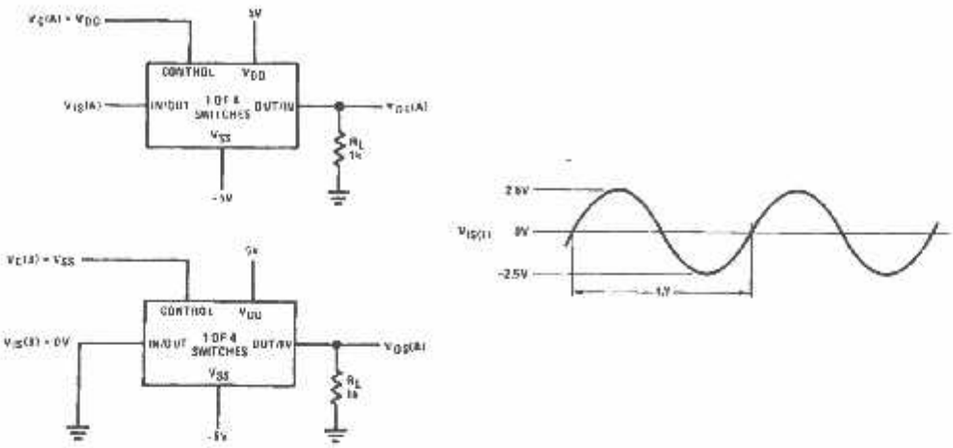


FIGURE 5. Crosstalk Between Any Two Switches

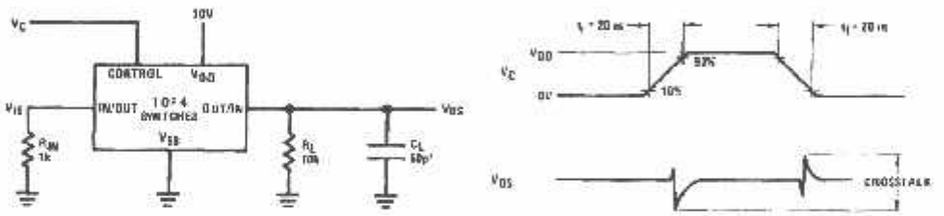


FIGURE 6. Crosstalk — Control to Input Signal Output

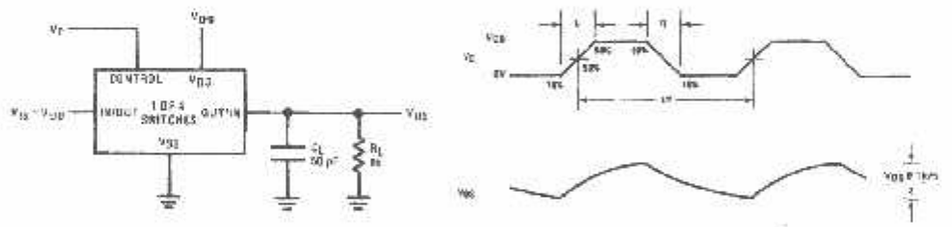


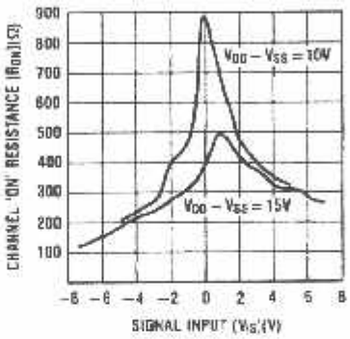
FIGURE 7. Maximum Control Input Frequency

TABLE 1. CD4016B Switch Test Conditions for V_{IHC}

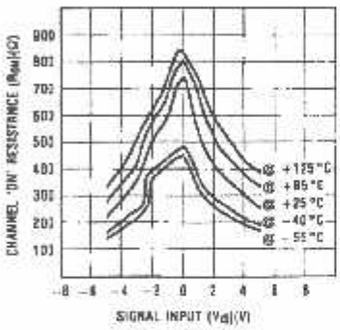
Temperature Range	V_{DD}	Switch Input V_{IS}	Switch Input I_{IS} (mA)			Switch Output V_{OS}(V)	
			−40°C	25°C	+85°C	Min	Max
COMMERCIAL	5	0	0.2	0.16	0.12		0.4
	5	5	−0.2	−0.16	−0.12	4.6	
	10	0	0.5	0.4	0.3		0.5
	10	10	−0.5	−0.4	−0.3	9.5	
	15	0	1.4	1.2	1.0		1.5
	15	15	−1.4	−1.2	−1.0	13.5	

Typical Performance Characteristics

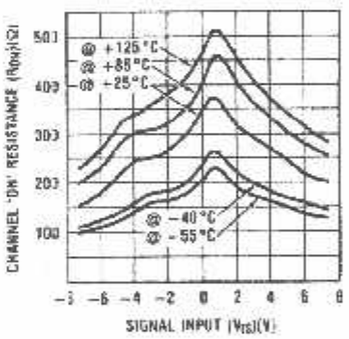
'ON' Resistance vs. Signal Voltage $T_A = 25°C$



'ON' Resistance Temperature Variation for $V_{DD} - V_{SS} = 10V$

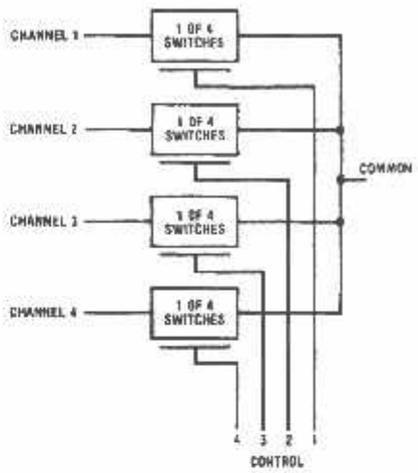


'ON' Resistance Temperature Variation for $V_{DD} - V_{SS} = 15V$

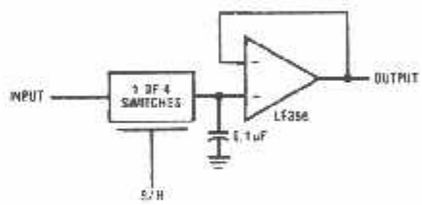


Typical Applications

4 Input Multiplexer



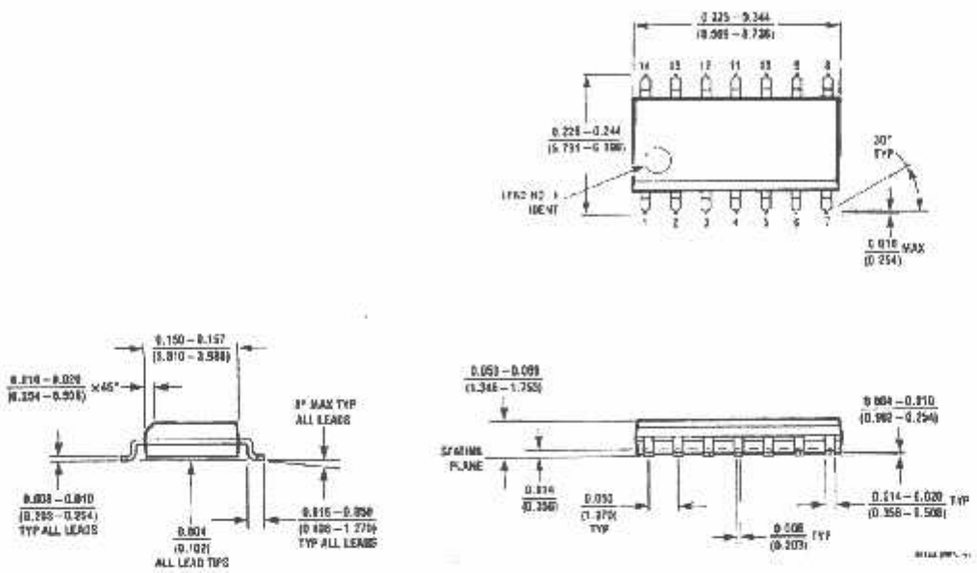
Sample/Hold Amplifier



Special Considerations

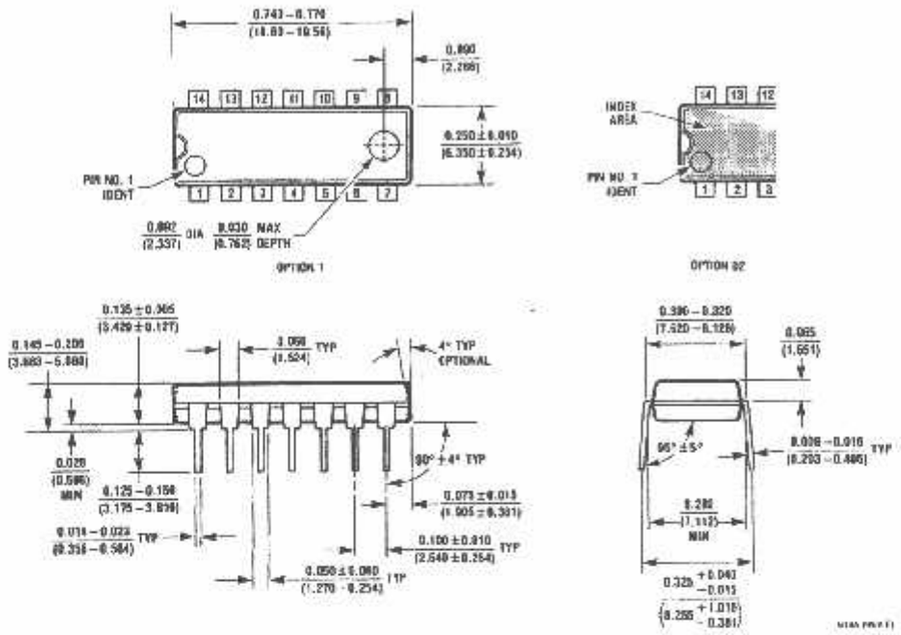
The CD4016B is composed of 4, two-transistor analog switches. These switches do not have any linearization or compensation circuitry for "R_{ON}" as do the CD4066B's. Because of this, the special operating considerations for the CD4066B do not apply to the CD4016B, but at low supply voltages, ≤5V, the CD4016B's On Resistance becomes non-linear. It is recommended that at 5V, voltages on the in/out pins be maintained within about 1V of either V_{DD} or V_{SS}; and that at 3V the voltages on the in/out pins should be at V_{DD} or V_{SS} for reliable operation.

Physical Dimensions inches (millimeters) unless otherwise noted



14-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-012, 0.150" Narrow
Package Number M14A

Physical Dimensions inches (millimeters) unless otherwise noted (Continued)



14-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300" Wide
Package Number N14A

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2. A critical component in any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

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Low power quad op amps

LM124/224/324/324A/ SA534/LM2902

DESCRIPTION

The LM124/SA534/LM2902 series consists of four independent, high-gain, internally frequency-compensated operational amplifiers designed specifically to operate from a single power supply over a wide range of voltages.

UNIQUE FEATURES

In the linear mode, the input common-mode voltage range includes ground and the output voltage can also swing to ground, even though operated from only a single power supply voltage.

The unity gain crossover frequency and the input bias current are temperature-compensated.

FEATURES

- Internally frequency-compensated for unity gain
- Large DC voltage gain: 100dB
- Wide bandwidth (unity gain): 1MHz (temperature-compensated)
- Wide power supply range Single supply: $3V_{DC}$ to $30V_{DC}$ or dual supplies: $\pm1.5V_{DC}$ to $\pm15V_{DC}$
- Very low supply current drain: essentially independent of supply voltage (1mW/op amp at $+5V_{DC}$)
- Low input biasing current: $45nA_{DC}$ (temperature-compensated)
- Low input offset voltage: $2mV_{DC}$ and offset current: $5nA_{DC}$
- Differential input voltage range equal to the power supply voltage
- Large output voltage: $0V_{DC}$ to V_{CC}-$1.5V_{DC}$ swing

PIN CONFIGURATION

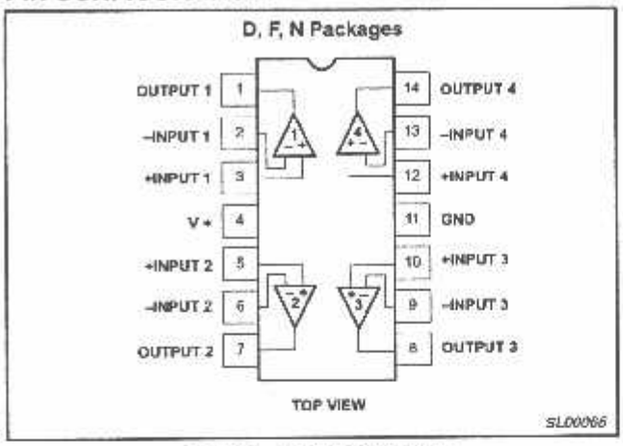


Figure 1. Pin Configuration

ORDERING INFORMATION

DESCRIPTION	TEMPERATURE RANGE	ORDER CODE	DWG #
14-Pin Plastic Dual In-Line Package (DIP)	-55°C to +125°C	LM124N	SOT27-1
14-Pin Ceramic Dual In-Line Package (CERDIP)	-55°C to +125°C	LM124F	0581B
14-Pin Plastic Dual In-Line Package (DIP)	-25°C to +85°C	LM224N	SOT27-1
14-Pin Ceramic Dual In-Line Package (CERDIP)	-25°C to +85°C	LM224F	0581B
14-Pin Plastic Small Outline (SO) Package	-25°C to +85°C	LM224D	SOT108-1
14-Pin Plastic Dual In-Line Package (DIP)	0°C to +70°C	LM324N	SOT27-1
14-Pin Ceramic Dual In-Line Package (CERDIP)	0°C to +70°C	LM324F	0581B
14-Pin Plastic Small Outline (SO) Package	0°C to +70°C	LM324D	SOT108-1
14-Pin Plastic Dual In-Line Package (DIP)	0°C to +70°C	LM324AN	SOT27-1
14-Pin Plastic Small Outline (SO) Package	0°C to +70°C	LM324AD	SOT108-1
14-Pin Plastic Dual In-Line Package (DIP)	-40°C to +85°C	SA534N	SOT27-1
14-Pin Ceramic Dual In-Line Package (CERDIP)	-40°C to +85°C	SA534F	0581B
14-Pin Plastic Small Outline (SO) Package	-40°C to +85°C	SA534D	SOT108-1
14-Pin Plastic Small Outline (SO) Package	-40°C to +125°C	LM2902D	SOT108-1
14-Pin Plastic Dual In-Line Package (DIP)	-40°C to +125°C	LM2902N	SOT27-1

ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Supply voltage	32 or ±16	V_{DC}
V_{IN}	Differential input voltage	32	V_{DC}
V_{IN}	Input voltage	-0.3 to +32	V_{DC}
P_D	Maximum power dissipation, T_A=25°C (still-air)[1]		
	N package	1420	mW
	F package	1190	mW
	D package	1040	mW
	Output short-circuit to GND one amplifier[2] V_{CC}<15V_{DC} and T_A=25°C	Continuous	
I_{IN}	Input current (V_{IN}<-0.3V)[3]	50	mA
T_A	Operating ambient temperature range		
	LM324/A	0 to +70	°C
	LM224	-25 to +85	°C
	SA534	-40 to +85	°C
	LM2902	-40 to +125	°C
	LM124	-55 to +125	°C
T_{STG}	Storage temperature range	-65 to +150	°C
T_{SOLD}	Lead soldering temperature (10sec max)	300	°C

NOTES:

1. Derate above 25°C at the following rates:
   F package at 9.5mW/°C
   N package at 11.4mW/°C
   D package at 8.3mW/°C
2. Short-circuits from the output to V_{CC}+ can cause excessive heating and eventual destruction. The maximum output current is approximately 40mA, independent of the magnitude of V_{CC}. At values of supply voltage in excess of +15V_{DC} continuous short-circuits can exceed the power dissipation ratings and cause eventual destruction.
3. This input current will only exist when the voltage at any of the input leads is driven negative. It is due to the collector-base junction of the input PNP transistors becoming forward biased and thereby acting as input bias clamps. In addition, there is also lateral NPN parasitic transistor action on the IC chip. This action can cause the output voltages of the op amps to go to the V+ rail (or to ground for a large overdrive) during the time that the input is driven negative.

DC ELECTRICAL CHARACTERISTICS

V_{CC}=5V, T_A=25°C unless otherwise specified.

SYMBOL	PARAMETER	TEST CONDITIONS	LM124/LM224			LM324/SA534/LM2902			UNIT
			Min	Typ	Max	Min	Typ	Max	
V_{OS}	Offset voltage[1]	R_S=0Ω		±2	±5		±2	+7	mV
		R_S=0Ω, over temp.			±7			+9	
$\Delta V_{OS}/\Delta T$	Temperature drift	R_S=0Ω, over temp.		7			7		µV/°C
I_{BIAS}	Input current[2]	$I_{IN}(+)$ or $I_{IN}(-)$		45	150		45	250	nA
		$I_{IN}(+)$ or $I_{IN}(-)$, over temp		40	300		40	500	
$\Delta I_{BIAS}/\Delta T$	Temperature drift	Over temp.		50			50		pA/°C
I_{OS}	Offset current	$I_{IN}(+)-I_{IN}(-)$		±3	±30		±5	±50	nA
		$I_{IN}(+)-I_{IN}(-)$, over temp.			±100			±150	
$\Delta I_{OS}/\Delta T$	Temperature drift	Over temp.		10			10		pA/°C
V_{CM}	Common-mode voltage range[3]	V_{CC}≤30V	0		V_{CC}-1.5	0		V_{CC}-1.5	V
		V_{CC}≤30V, over temp.	0		V_{CC}-2	0		V_{CC}-2	
CMRR	Common-mode rejection ratio	V_{CC}=30V	70	85		65	70		dB
V_{OUT}	Output voltage swing	R_L=2kΩ, V_{CC}=30V, over temp.	26			26			V
V_{OH}	Output voltage high	R_L≤10kΩ, V_{CC}=30V, over temp.	27	28		27	28		V
V_{OL}	Output voltage low	R_L≤10kΩ, over temp.		5	20		5	20	mV
I_{CC}	Supply current	R_L=∞, V_{CC}=30V, over temp.		1.5	3		1.5	3	mA
		R_L=∞, over temp.		0.7	1.2		0.7	1.2	
A_{VOL}	Large-signal voltage gain	V_{CC}=15V (for large V_O swing), R_L≥2kΩ	50	100		25	100		V/mV
		V_{CC}=15V (for large V_O swing), R_L≥2kΩ, over temp.	25			15			
	Amplifier-to-amplifier coupling[5]	f=1kHz to 20kHz, input referred		-120			-120		dB
PSRR	Power supply rejection ratio	R_S≤0Ω	65	100		65	100		dB
I_{OUT}	Output current source	V_{IN}+=+1V, V_{IN}-=0V, V_{CC}=15V	20	40		20	40		mA
		V_{IN}+=+1V, V_{IN}-=0V, V_{CC}=15V, over temp.	10	20		10	20		
	Output current sink	V_{IN}-=+1V, V_{IN}+=0V, V_{CC}=15V	10	20		10	20		
		V_{IN}-=+1V, V_{IN}+=0V, V_{CC}=15V, over temp.	5	8		5	8		
		V_{IN}-=+1V, V_{IN}+=0V, V_O=200mV	12	50		12	50		µA
I_{SC}	Short-circuit current[4]		10	40	60	10	40	60	mA
GBW	Unity gain bandwidth			1			1		MHz
SR	Slew rate			0.3			0.3		V/µs
V_{NOISE}	Input noise voltage	f=1kHz		40			40		nV/√Hz
V_{DIFF}	Differential input voltage[5]				V_{CC}			V_{CC}	V

DC ELECTRICAL CHARACTERISTICS (Continued)

V_{CC}=5V, T_A=25°C unless otherwise specified.

SYMBOL	PARAMETER	TEST CONDITIONS	LM324A			UNIT
			Min	Typ	Max	
V_{OS}	Offset voltage[1]	R_S=0Ω		±2	±3	mV
		R_S=0Ω, over temp.			±5	
$\Delta V_{OS}/\Delta T$	Temperature drift	R_S=0Ω, over temp.		7	30	µV/°C
I_{BIAS}	Input current[2]	$I_{IN}(+)$ or $I_{IN}(-)$		45	100	nA
		$I_{IN}(+)$ or $I_{IN}(-)$, over temp.		40	200	
$\Delta I_{BIAS}/\Delta T$	Temperature drift	Over temp.		50		pA/°C
I_{OS}	Offset current	$I_{IN}(+)-I_{IN}(-)$		±5	±30	nA
		$I_{IN}(+)-I_{IN}(-)$, over temp.			±75	
$\Delta I_{OS}/\Delta T$	Temperature drift	Over temp.		10	300	pA/°C
V_{CM}	Common-mode voltage range[3]	V_{CC}≤30V	0		V_{CC}-1.5	V
		V_{CC}≤30V, over temp.	0		V_{CC}-2	V
CMRR	Common-mode rejection ratio	V_{CC}=30V	65	85		dB
V_{OUT}	Output voltage swing	R_L=2kΩ, V_{CC}=30V, over temp.	26			V
V_{OH}	Output voltage high	R_L≤10kΩ, V_{CC}=30V, over temp.	27	28		V
V_{OL}	Output voltage low	R_L≤10kΩ, over temp.		5	20	mV
I_{CC}	Supply current	R_L=∞ V_{CC}=30V, over temp.		1.5	3	mA
		R_L=∞, over temp.		0.7	1.2	mA
A_{VOL}	Large-signal voltage gain	V_{CC}=15V (for large V_O swing), R_L≥2kΩ	25	100		V/mV
		V_{CC}=15V (for large V_O swing), R_L≥2kΩ, over temp.	15			V/mV
	Amplifier-to-amplifier coupling[5]	f=1kHz to 20kHz, input referred		-120		dB
PSRR	Power supply rejection ratio	R_S≤0Ω	65	100		dB
I_{OUT}	Output current source	V_{IN}+=+1V, V_{IN}-=0V, V_{CC}=15V	20	40		mA
		V_{IN}+=+1V, V_{IN}-=0V, V_{CC}=15V, over temp.	10	20		mA
	Output current sink	V_{IN}-=+1V, V_{IN}+=0V, V_{CC}=15V	10	20		mA
		V_{IN}-=+1V, V_{IN}+=0V, V_{CC}=15V, over temp.	5	8		mA
		V_{IN}-=+1V, V_{IN}+=0V, V_O=200mV	12	50		µA
I_{SC}	Short-circuit current[4]		10	40	60	mA
V_{DIFF}	Differential input voltage[3]				V_{CC}	V
GBW	Unity gain bandwidth			1		MHz
SR	Slew rate			0.3		V/µs
V_{NOISE}	Input noise voltage	f=1kHz		40		nV/√Hz

NOTES:

1. V_O = 1.4V_{CC}, R_S=0Ω with V_{CC} from 5V to 30V and over full input common-mode range (0V_{DC}+ to V_{CC} -1.5V).
2. The direction of the input current is out of the IC due to the PNP input stage. This current is essentially constant, independent of the state of the output so no loading change exists on the input lines.
3. The input common-mode voltage or either input signal voltage should not be allowed to go negative by more than 0.3V. The upper end of the common-mode voltage range is V_{CC} -1.5, but either or both inputs can go to +32V without damage.
4. Short-circuits from the output to V_{CC} can cause excessive heating and eventual destruction. The maximum output current is approximately 40mA independent of the magnitude of V_{CC}. At values of supply voltage in excess of +15V_{DC}, continuous short-circuits can exceed the power dissipation ratings and cause eventual destruction. Destructive dissipation can result from simultaneous shorts on all amplifiers.
5. Due to proximity of external components, insure that coupling is not originating via stray capacitance between these external parts. This typically can be detected as this type of coupling increases at higher frequencies.

EQUIVALENT CIRCUIT

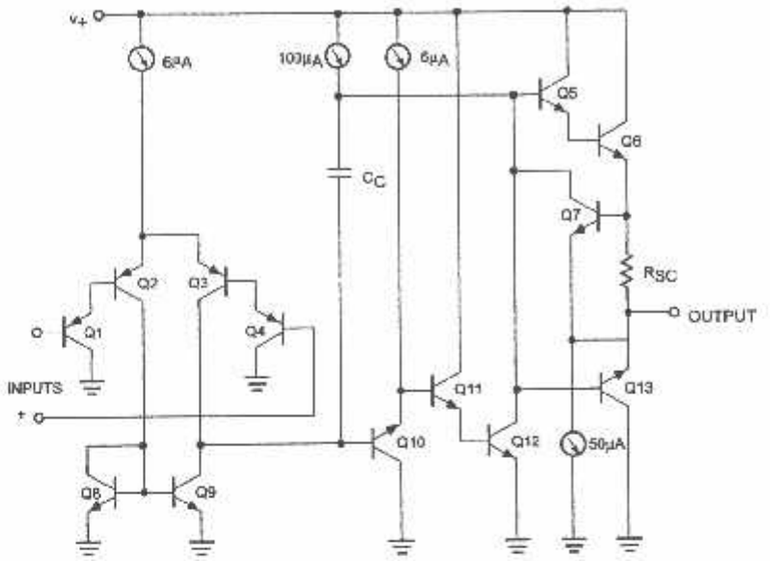


Figure 2. Equivalent Circuit

TYPICAL PERFORMANCE CHARACTERISTICS

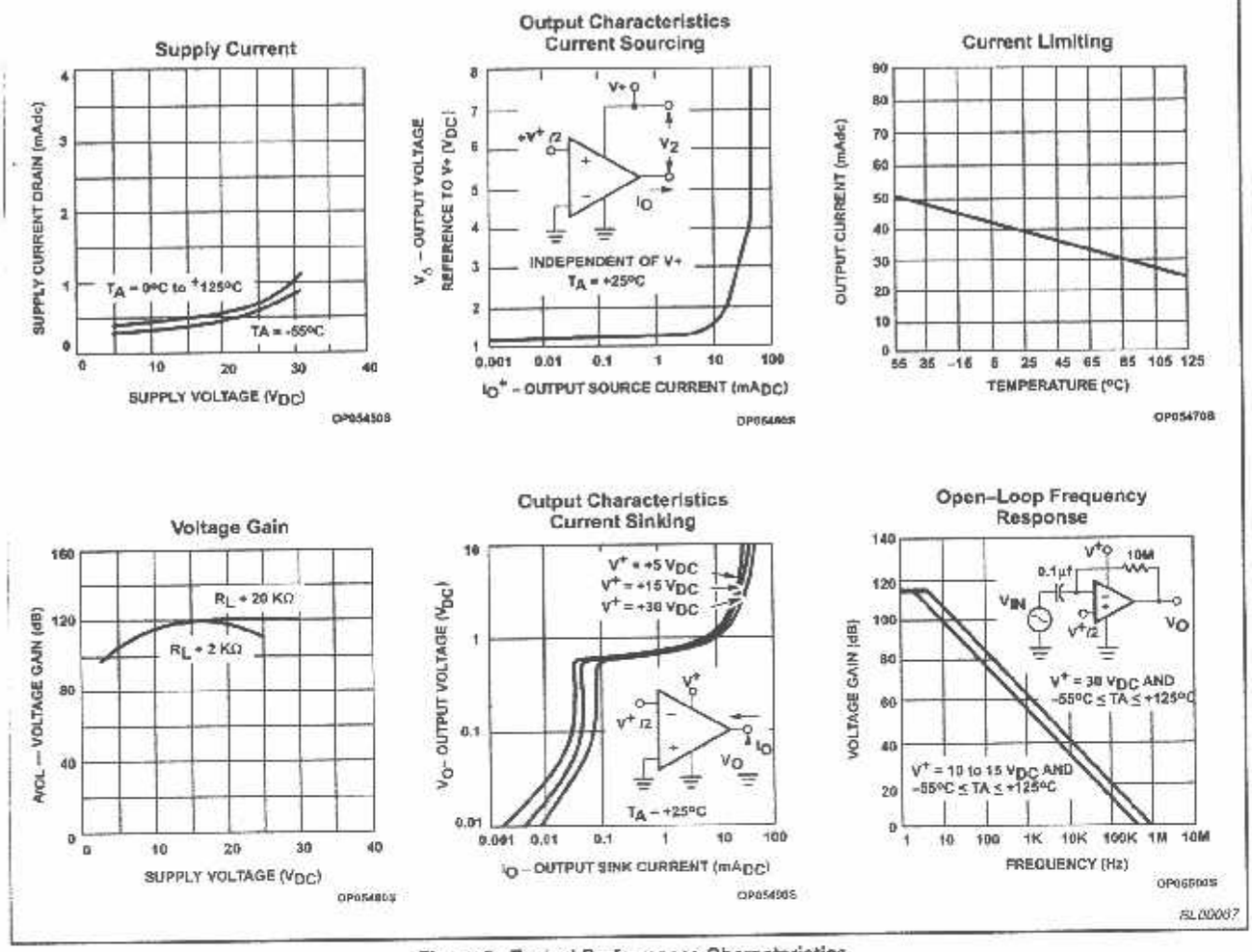


Figure 3. Typical Performance Characteristics

TYPICAL PERFORMANCE CHARACTERISTICS (Continued)

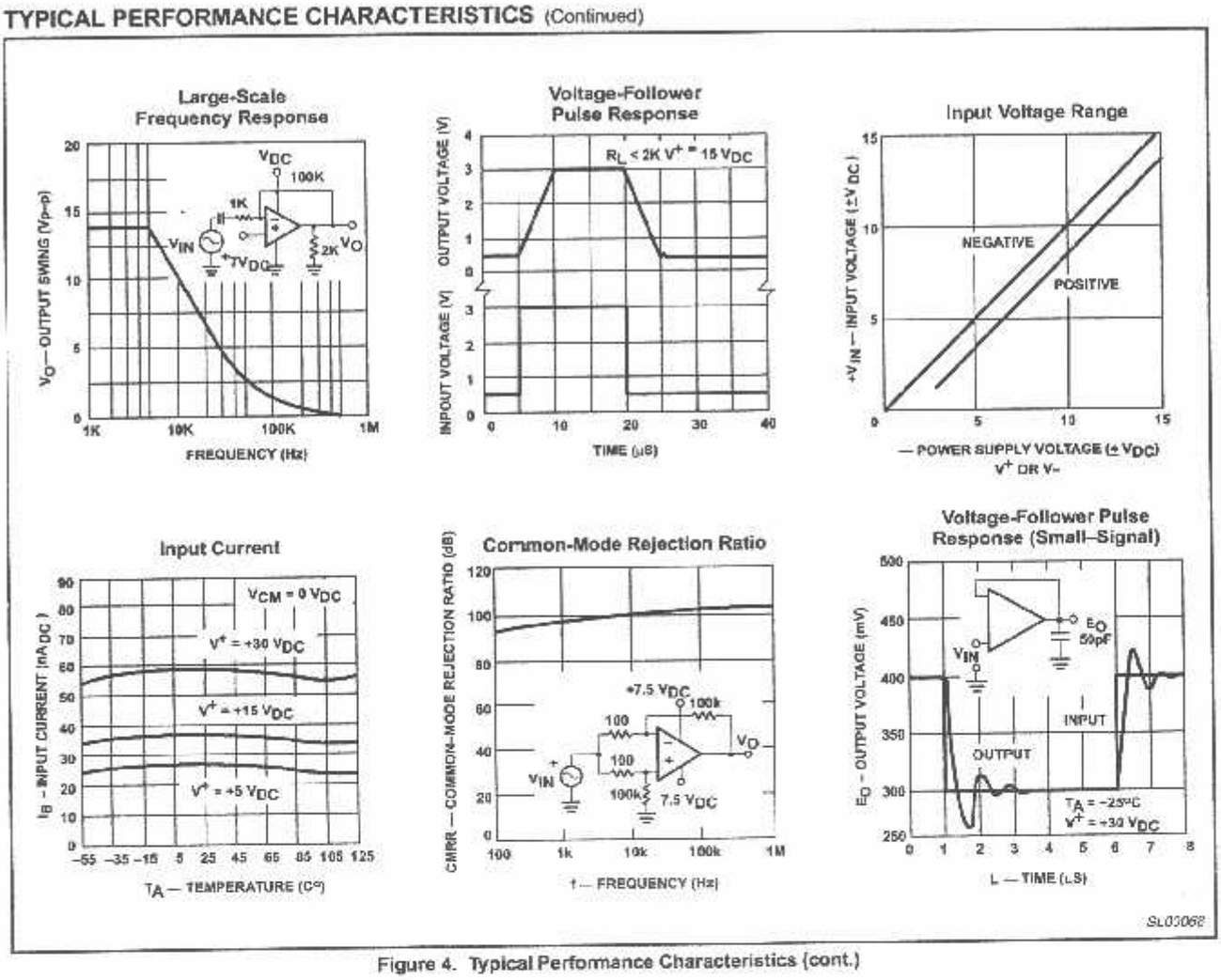


Figure 4. Typical Performance Characteristics (cont.)

TYPICAL APPLICATIONS

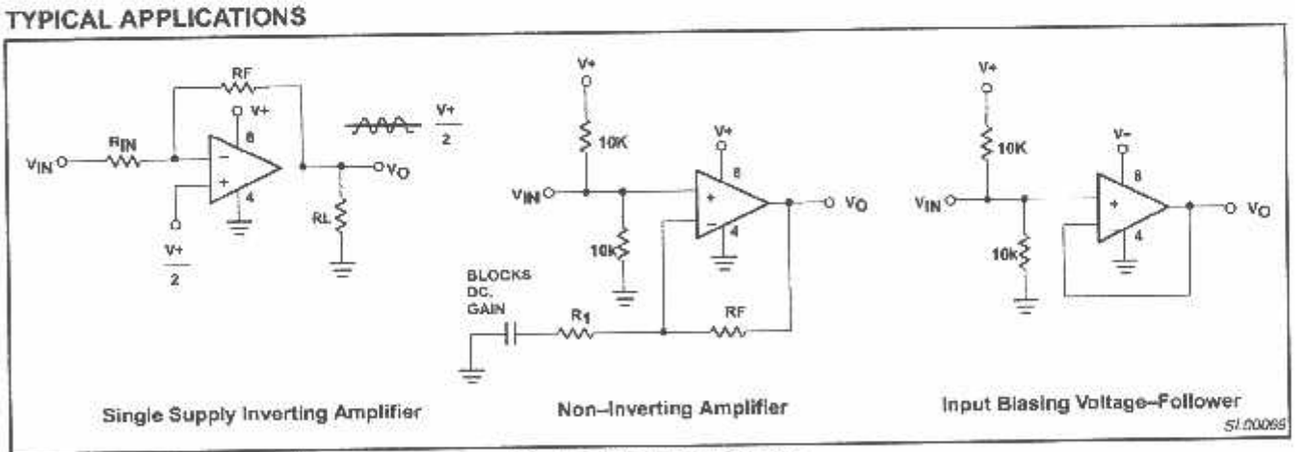


Figure 5. Typical Applications

National Semiconductor

June 1989

54157/DM54157/DM74157
Quad 2-Line to 1-Line Data Selectors/Multiplexers

General Description

These data selectors/multiplexers contain inverters and drivers to supply full on-chip data selection to the four output gates. A separate strobe input is provided. A 4-bit word is selected from one of two sources and is routed to the four outputs.

Features

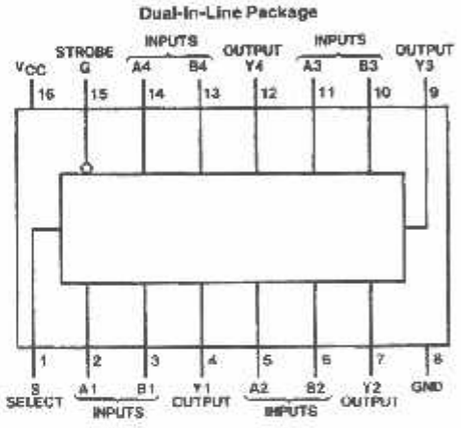
- Buffered inputs and outputs
- Typical propagation time 9 ns
- Typical power dissipation 150 mW
- Alternate Military/Aerospace device (54157) is available. Contact a National Semiconductor Sales Office/ Distributor for specifications.

Applications

- Expand any data input point
- Multiplex dual data buses
- Generate four functions of two variables (one variable is common)
- Source programmable counters

Connection Diagram

Dual-In-Line Package



TL/F/5950–1

Order Number 54157DMQB, 54157FMQB, DM54157J, DM54157W or DM74157N
See NS Package Number J16A, N16E or W16A

Function Table

Inputs				Output Y
Strobe	Select	A	B	
H	X	X	X	L
L	L	L	X	L
L	L	H	X	H
L	H	X	L	L
L	H	X	H	H

H = High Level, L = Low Level, X = Don't Care

RRD-B30M105/Printed in U. S. A.

Absolute Maximum Ratings (Note)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage	7V
Input Voltage	5.5V
Operating Free Air Temperature Range	
DM54 and 54	−55°C to +125°C
DM74	0°C to +70°C
Storage Temperature Range	−65°C to +150°C

Note: *The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.*

Recommended Operating Conditions

Symbol	Parameter	DM54157			DM74157			Units
		Min	Nom	Max	Min	Nom	Max	
V_{CC}	Supply Voltage	4.5	5	5.5	4.75	5	5.25	V
V_{IH}	High Level Input Voltage	2			2			V
V_{IL}	Low Level Input Voltage			0.8			0.8	V
I_{OH}	High Level Output Current			−0.8			−0.8	mA
I_{OL}	Low Level Output Current			16			16	mA
T_A	Free Air Operating Temperature	−55		125	0		70	°C

Electrical Characteristics over recommended operating free air temperature range (unless otherwise noted)

Symbol	Parameter	Conditions		Min	Typ (Note 1)	Max	Units
V_I	Input Clamp Voltage	V_{CC} = Min, I_I = −12 mA				−1.5	V
V_{OH}	High Level Output Voltage	V_{CC} = Min, I_{OH} = Max, V_{IL} = Max, V_{IH} = Min		2.4	3.4		V
V_{OL}	Low Level Output Voltage	V_{CC} = Min, I_{OL} = Max, V_{IH} = Min, V_{IL} = Max				0.4	V
I_I	Input Current @ Max Input Voltage	V_{CC} = Max, V_I = 5.5V				1	mA
I_{IH}	High Level Input Current	V_{CC} = Max, V_I = 2.4V				40	µA
I_{IL}	Low Level Input Current	V_{CC} = Max, V_I = 0.4V				−1.6	mA
I_{OS}	Short Circuit Output Current	V_{CC} = Max (Note 2)	DM54	−20		−55	mA
			DM74	−18		−55	
I_{CC}	Supply Current	V_{CC} = Max (Note 3)			30	48	mA

Note 1: All typicals are at V_{CC} = 5V, T_A = 25°C.

Note 2: Not more than one output should be shorted at a time.

Note 3: I_{CC} is measured with 4.5V applied to all inputs and all outputs open.

Switching Characteristics at V_{CC} = 5V and T_A = 25°C (See Section 1 for Test Waveforms and Output Load)

Symbol	Parameter	From (Input) To (Output)	R_L = 400Ω, C_L = 15 pF		Units
			Min	Max	
t_{PLH}	Propagation Delay Time Low to High Level Output	Data to Y		14	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	Data to Y		14	ns
t_{PLH}	Propagation Delay Time Low to High Level Output	Strobe to Y		20	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	Strobe to Y		21	ns
t_{PLH}	Propagation Delay Time Low to High Level Output	Select to Y		23	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	Select to Y		27	ns

Logic Diagram

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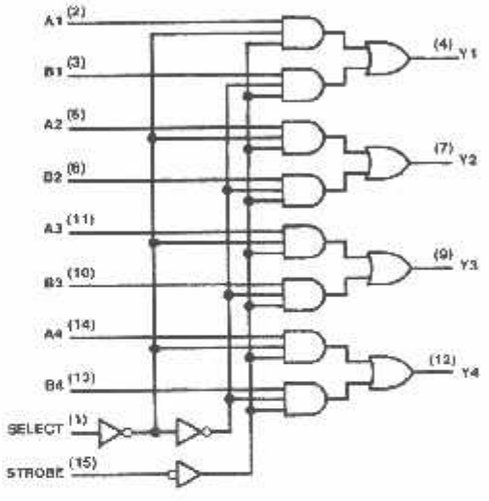
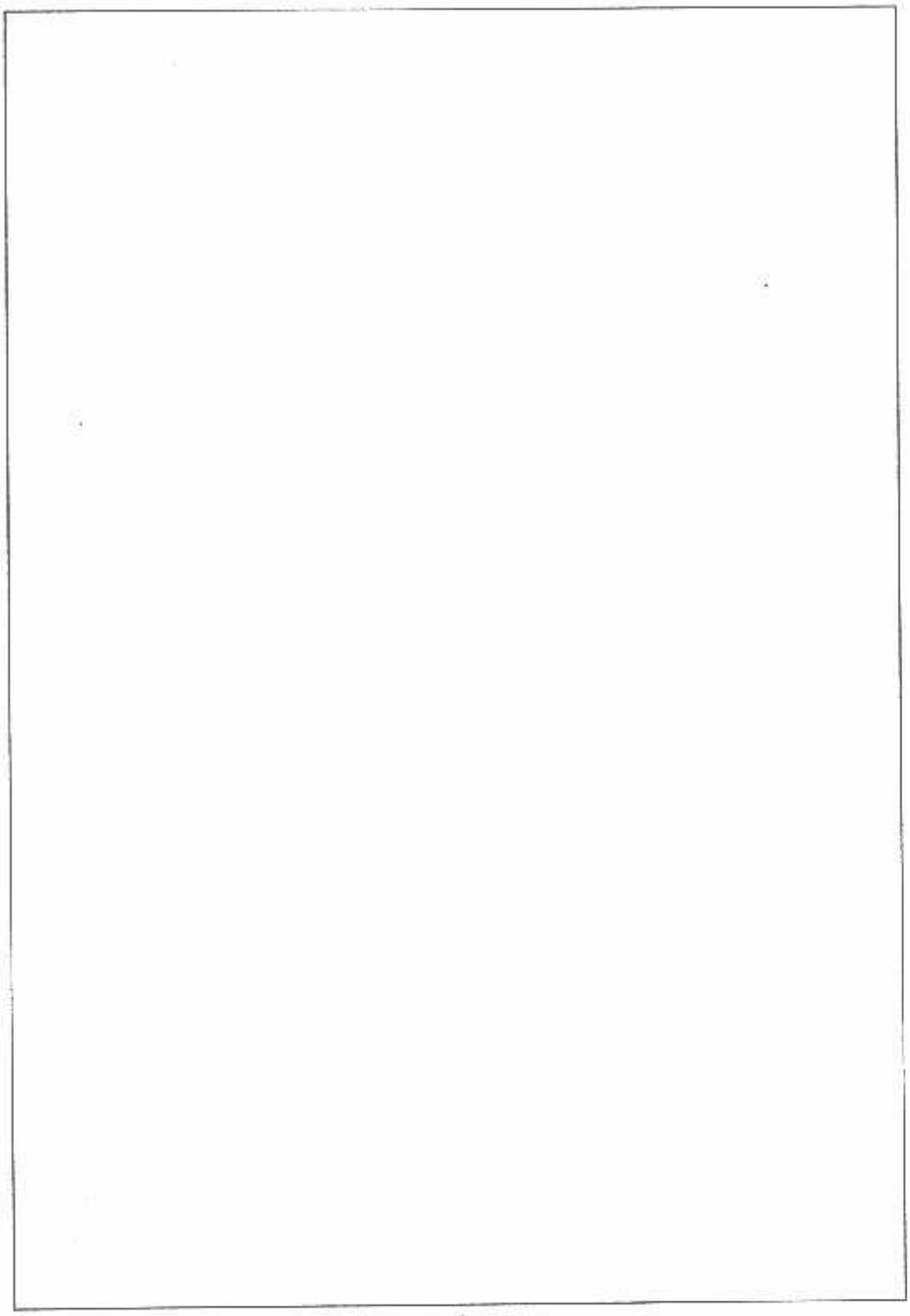
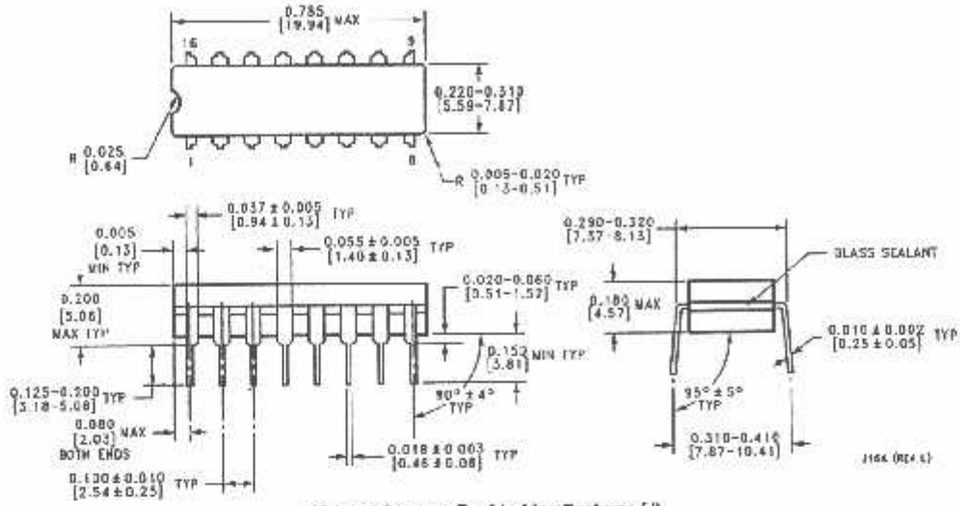


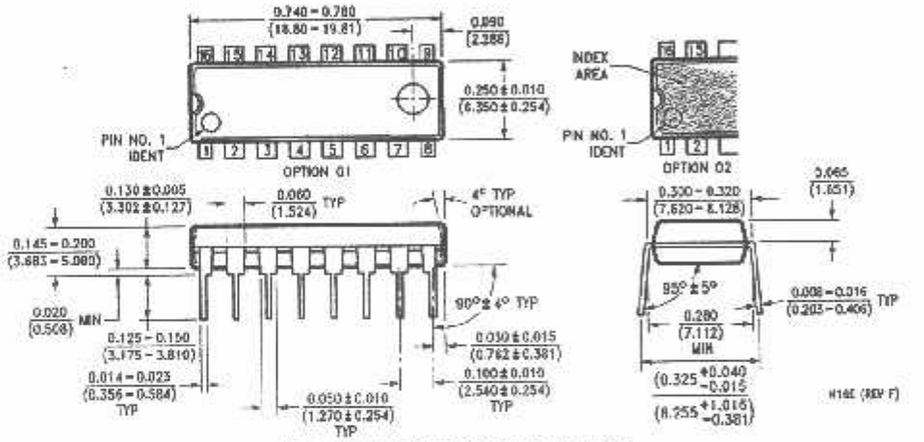
TL/F/8958–2



Physical Dimensions inches (millimeters)

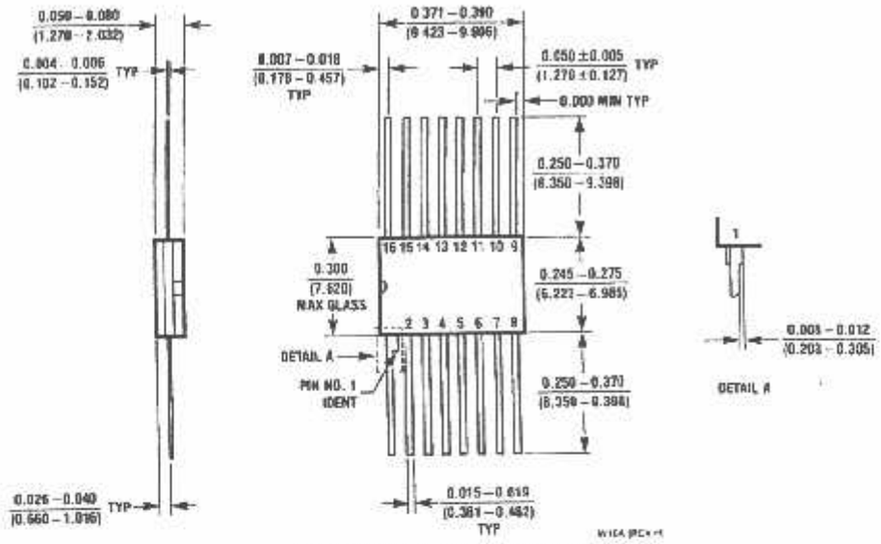


16-Lead Ceramic Dual-In-Line Package (J)
Order Number 54157W or DM54157J
NS Package Number J16A



16-Lead Molded Dual-In-Line Package (N)
Order Number DM74157N
NS Package Number N16E

Physical Dimensions inches (millimeters) (Continued)



16-Lead Ceramic Flat Package (W)
Order Number 54157FMQB or DM54157W
NS Package Number W16A

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