

**KONSENTRASI TEKNIK ELEKTRONIKA D III
JURUSAN TEKNIK ELEKTRO D III
FAKULTAS TEKNOLOGI INDUSTRI
INSTITUT TEKNOLOGI NASIONAL MALANG**



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**PERANCANGAN DAN PEMBUATAN ALAT
PENGHITUNG WAKTU TEMPUH DAN KECEPATAN
PADA PERLOMBAAN DRAG RACE**

**Disusun Oleh :
Andri Dwi Arianto
Nim 05.52.205**

2009

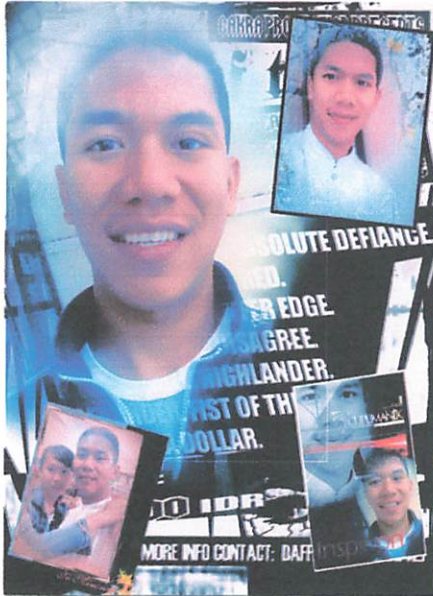
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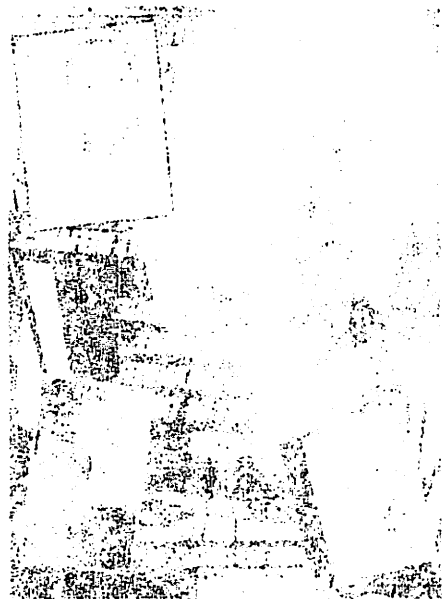
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بِسْمِ اللَّهِ الرَّحْمَنِ الرَّحِيمِ

" Dengan Menyebut Nama Allah Yang Maha Pengasih Lagi Maha Penyayang"

Assalamu'allaikum Wr. Wb.

Pertama kali saya mengucapkan syukur kepada Allah SWT yang telah mewujudkan ide dan keinginan saya untuk menyelesaikan Tugas Akhir kuliah. Semoga semua Maha mendengar, pengasih lagi Maha penyayang bagi semua umatNYA.

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Wa'allaikumsalam Wr. Wb.



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INSTITUT TEKNOLOGI NASIONAL MALANG**

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JURUSAN TEKNIK ELEKTRO D III
FAKULTAS TEKNOLOGI INDUSTRI
INSTITUT TEKNOLOGI NASIONAL MALANG
2009

PERANCANGAN DAN PEMBUATAN ALAT PENGHITUNG WAKTU TEMPUH DAN KECEPATAN PADA PERLOMBAAN DRAG RACE

ABSTRAK

Drag race adalah salah satu contoh olah raga balap motor yang sering diadakan dan banyak diminati di Indonesia. Pada saat perlombaan berlangsung, kesalahan perhitungan waktu tempuh yang dilakukan oleh para juri sering terjadi. Hal ini karena alat penghitung waktu yang digunakan masih bersifat manual. Oleh karena itu perlu dilakukan penelitian dan pembuatan simulasi terhadap perlombaan tersebut. Tujuan dari penelitian ini adalah untuk merancang dan membuat alat penghitung waktu tempuh secara otomatis berbasis mikrokontroler.

Perancangan dan pembuatan alat penghitung waktu tempuh secara otomatis ini menggunakan mikrokontroler sebagai kontroler, *infrared* sebagai komunikasi data dan komponen-komponen lain yang mendukung seperti LCD, *keypad*, *tone decoder* dan regulator. Alat ini didasarkan pada kerja sensor *infrared*, jika terhalang benda maka akan memberikan logika nol dan logika satu saat sensor tidak terhalang yang berfungsi sebagai masukan terhadap mikrokontroler. Alat tersebut disimulasikan pada perlombaan *drag race* dengan jarak 2,01 meter, mengacu pada ukuran jarak sebenarnya yaitu sebesar 201 meter. Berdasarkan hasil penelitian diperoleh bahwa alat penghitung waktu tempuh ini memiliki ketelitian lebih tinggi daripada alat penghitung waktu tempuh manual (*stopwatch*).

Kata Kunci : *LCD, Keypad, Tone Decoder, Infrared, Mikrokontroler.*

Source: *Journal of the American Statistical Association*, 1997, 92, 1033-1046.

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KATA PENGANTAR

Atas Berkat Rahmat Allah Yang Maha Kuasa, sehingga penulis dapat menyelesaikan laporan Tugas Akhir dengan judul :

PERANCANGAN DAN PEMBUATAN ALAT PENGHITUNG WAKTU TEMPUH DAN KECEPATAN PADA PERLOMBAAN DRAG RACE

Pembuatan Tugas Akhir ini disusun guna memenuhi syarat akhir kelulusan pendidikan jenjang Diploma III di Institut Teknologi Nasional Malang. Laporan Tugas Akhir ini merupakan tanggung jawab tertulis atas ilmu pengetahuan yang didapat selama penyusun mengikuti kuliah.

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Malang, 2009

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BAB I

PENDAHULUAN

1.1. Latar Belakang

Balap motor merupakan olahraga yang cukup diminati di Indonesia. Banyak daerah yang sering mengadakan balap motor tiap minggunya. Balap motor yang diadakan bermacam-macam. Banyaknya jenis balap motor dibedakan berdasarkan jenis dan bentuk motor yang digunakan. *Road race*, *drag race*, *motorcross* dan *grasstrack* adalah contoh sebagian jenis-jenis balap motor yang sering diadakan. Jenis balap motor yang paling sering diadakan adalah *drag race*. Perbedaan *drag race* dengan balap motor yang lain adalah balap motor ini memiliki dua jalur lintasan lurus dengan jarak lintasan yang pendek, yaitu 402 meter atau 201 meter. (Wikipedia Indonesia, 2007_)

Kenyataan yang ada dalam perlombaan dalam tingkat pemula sebagai berikut : Alat yang digunakan masih manual dan memerlukan orang yang mengoperasikan dari start sampai finis, data pengukuran bisa dimanipulasi sehingga tidak sesuai dengan kebenaran, pengoperasian alat pengukur waktu dapat menguntungkan salah satu pihak, menyita waktu dan tenaga bagi mereka yang menggunakan karena dalam perhitungan waktu orang yang mengukur tidak dapat leluasa untuk meninggalkan tempat perlombaan sebelum perlombaan selesai atau sudah ada yang melewati garis finis, alat pengukuran waktu sangat tergantung pada kecermatan orang yang menggunakan karena harus dituntut cermat dan teliti.

Harapan yang diinginkan dalam pembuatan system pengukuran waktu berbasis *Mikrokontroler AT89S51* sebagai berikut :

Alat ini dapat digunakan sebagai alternative pilihan dalam pengukuran waktu disbanding alat – alat lain yang masih manual, bekerja secara otomatis dengan sensor yang dipakai sehingga lebih cermat, tepat dan teliti juga tidak menyita waktu, tenaga dan biaya yang banyak bagi yang menggunakan, lebih efisien, praktis dan akurat, data hasil pengukuran tidak bisa dimanipulasi, pengoperasian alat ini sangat simple.

Untuk mengetahui pemenang pada perlombaan *drag race* pihak juri menggunakan *stopwatch* atau alat penghitung waktu digital lain sebagai alat untuk menghitung waktu tempuh peserta lomba. Tetapi masing-masing alat penghitung waktu tersebut memiliki kelemahan. Dengan *stopwatch*, kemungkinan kesalahan terjadi karena ketidaktepatan waktu yang dilakukan oleh juri pada saat mengoperasikan *stopwatch*. Sedangkan alat penghitung waktu digital memiliki harga sewa yang tinggi.

Berdasarkan kelemahan tersebut di atas, maka dibutuhkan suatu alat penghitung waktu tempuh dan kecepatan yang memiliki nilai ketepatan tinggi dengan harga relatif rendah sehingga dapat digunakan pada *event drag race*.

1.2. Rumusan Masalah

Dengan uraian singkat yang ada pada sub bab latar belakang di atas, maka rumusan masalah yang muncul adalah sebagai berikut:

1. Bagaimana membuat alat penghitung waktu tempuh dan kecepatan yang digunakan pada perlombaan *drag race* dengan mikrokontroler.
2. Bagaimana membuat program untuk mengetahui nilai waktu tempuh dan kecepatan dengan nilai jarak yang sudah diketahui.
3. Bagaimana membuat simulasi dari alat penghitung waktu tempuh dan kecepatan pada perlombaan *drag race*.

1.3. Tujuan

Tujuan dari penelitian ini adalah untuk merancang dan membuat alat penghitung waktu tempuh dan kecepatan secara otomatis berbasis mikrokontroler dan menggunakan *infrared*.

1.4. Batasan Masalah

Luasnya cakupan masalah yang muncul dari pembuatan alat ini dan keterbatasan kemampuan yang dimiliki, maka perlu adanya batasan masalah, yaitu sebagai berikut:

1. Parameter fisis yang dihitung adalah waktu dan kecepatan mobil peserta pada perlombaan *drag race* secara bergantian.
2. Perhitungan nilai waktu tempuh dan kecepatan dilakukan untuk satu kali pencapaian dari garis *start* menuju garis *finish*.
3. Jarak tempuh dalam simulasi *drag race* ini adalah sebesar 2,01 meter mengacu pada ukuran sebenarnya yaitu 201 meter.

1.5. Metodologi Penelitian

Untuk mempermudah dan memperjelas pembahasan dari laporan tugas akhir ini, penulis menerapkan system penulisan seperti di bawah ini :

BAB I : PENDAHULUAN

Berisi latar belakang permasalahan, rumusan masalah, tujuan pembahasan, batasan masalah metodologi penelitian dan sistematika penulisan.

BAB II : LANDASAN TEORI

Membahas tentang teori dasar rangkaian yang digunakan, Mikrokontroler, hardware dan teori dasar alat – alat pendukung lainnya.

BAB III : PERANCANGAN DAN PEMBUATAN ALAT

Membahas tentang perencanaan dan pembuatan alat pengukur jarak, kecepatan dan waktu pada drag race dengan menggunakan mikrokontroler AT 89S51.

BAB IV : HASIL DAN PEMBAHASAN

Menjelaskan tentang pengoperasian alat, pengujian alat, hasil perhitungan dari alat penghitung waktu tempuh dan kecepatan pada perlombaan *drag race* dan pembahasan.

BAB V : PENUTUP

Merupakan kesimpulan dari pembahasan bab – bab sebelumnya dan kemungkinan pengembangan alat.

1.6. Manfaat Kontribusi

Manfaat dari pembuatan alat dan simulasi pada perlombaan *drag race* adalah membuat alat penghitung waktu tempuh dan kecepatan yang sederhana tetapi dapat memberikan hasil yang memiliki nilai ketepatan yang tinggi.

BAB II

LANDASAN TEORI

2.1. Sensor

Sensor adalah alat yang digunakan untuk mendeteksi dan sering berfungsi untuk mengukur magnitude tertentu. Sensor adalah jenis transduser yang digunakan untuk mengubah variasi mekanis, magnetis, panas, sinar dan kimia menjadi tegangan dan arus listrik. Sensor biasanya dikategorikan melalui pengukur dan memegang peranan penting dalam pengendalian proses produksi modern.

2.1.1. *Infrared (Inframerah)*

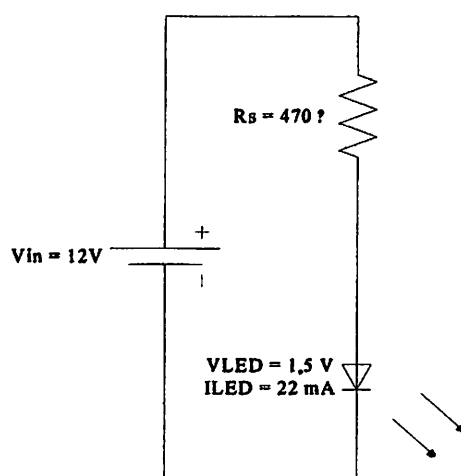
Merupakan komponen elektronika yang memancarkan cahaya inframerah. Sinar inframerah yang dipancarkan oleh pemancar tentunya mempunyai aturan tertentu agar data yang dipancarkan dapat diterima dengan baik oleh penerima. Oleh karena itu baik pemancar maupun penerima harus mempunyai aturan yang sama dalam mentransmisikan dan menerima sinyal tersebut.

2.1.2. *Light Emitting Diode (LED) Infrared*

Dioda pancar cahaya (LED) adalah dioda semikonduktor khusus yang dirancang untuk memancarkan cahaya apabila arus melaluinya. Apabila diberi bias

maju, energi elektron yang mengalir melewati tahanan sambungan diubah langsung menjadi energi cahaya.

Karena LED adalah dioda, maka arus hanya akan mengalir apabila LED dihubungkan dengan bias maju. LED harus dioperasikan di dalam ukuran kerja tegangan dan arus tertentu untuk mencegah kerusakan yang tidak dapat diubah lagi. Sebagian besar LED membutuhkan 1,5 sampai 2,2 volt untuk memberi bias maju dan dapat mengatasi dengan aman arus sebesar 20 sampai 30 mA. LED biasanya dihubungkan seri dengan tahanan yang membatasi tegangan dan arus pada nilai yang dikehendaki seperti pada Gambar 2.1.

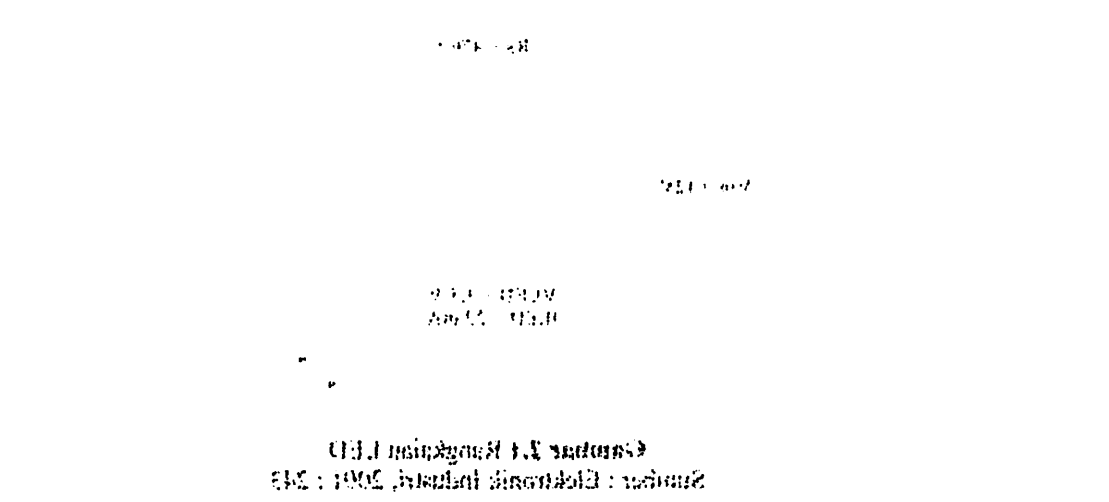


Gambar 2.1 Rangkaian LED
Sumber : Elektronik Industri, 2001 : 243

Keuntungan utama penggunaan LED sebagai sumber cahaya dibandingkan dengan bola lampu cahaya biasa adalah penggunaan daya yang jauh lebih rendah, jauh lebih lama umurnya dan beroperasi dengan kecepatan tinggi. Dioda silikon konvensional merubah energi menjadi panas. Jenis dioda ini disebut dioda yang memancarkan inframerah (IRED).

misal energi elektron yang mengalir melalui sambungan diarahkan langsung menjadi energi cahaya.

Material LED adalah dioda, maka arus hanya akan mengalir apabila LED dihubungkan dengan bias maju. LED harus diposisikan di dalam ukuran keping tegangan dan area tertentu untuk mencapai kemampuan yang tidak dapat dihindari lagi. Sebagai contoh LED membutuhkan 1.2 sampai 2.5 volt untuk mencapai bias maju dan dapat beroperasi dengan arus sebesar 20 sampai 30 mA. LED biasanya dihubungkan seri dengan tabung yang memiliki tegangan dan arus pada nilai yang dibicarakan seperti pada Gambar 3.1.



Konsumsi tenaga penggunaan LED sebagai sumber cahaya dibandingkan dengan bola lampu biasa adalah penggunaan daya yang jauh lebih rendah. Hal ini karena LED memiliki efisiensi yang lebih tinggi. Dioda silikon konvensional menjadi energi menjadi panas, tetapi dioda dioda yang menggunakan insulator (HELED).

2.1.3. Dioda

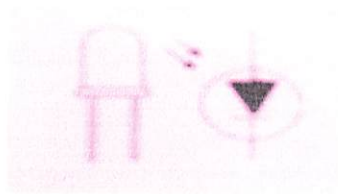
Dioda merupakan salah satu komponen semikonduktor. Fungsi Dioda adalah sebagai penyearah tegangan AC menjadi tegangan DC atau power supply DC. Arah arus yang mengalir dalam dioda adalah dari Anoda ke Katoda.



Gambar 2.2 Symbol Dioda

2.1.4. Photodioda

Photodioda merupakan suatu dioda yang peka terhadap cahaya. Suatu sumber cahaya menghasilkan energi panas begitu pula dengan inframerah. Photodioda lebih peka menangkap radiasi dari sinar inframerah. Ketika energi cahaya dengan gelombang jatuh pada sambungan photodioda, arus mengalir dalam sirkuit eksternal sehingga bekerja sebagai generator arus.



Gambar 2.3 Symbol Photodioda

2.2. Tone Decoder (LM567)

Rangkaian LM567 terdiri dari detektor arus (I) dan Q yang digerakkan oleh tegangan yang dikontrol oleh osilator yang menentukan pusat frekuensi dari *decoder*. Komponen eksternal digunakan untuk menentukan frekuensi pusat, *bandwidth* dan *output delay*.

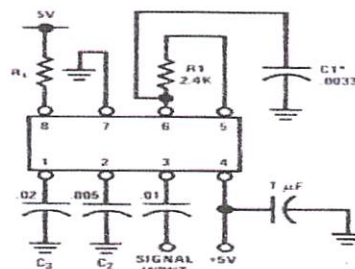
Fitur-fitur yang disediakan oleh LM567: (Sumber : www.national.com, 1999 : 1)

- Batasan frekuensi dari 20 sampai 1 dengan resistor eksternal
- Keluaran logik yang *compatible* dengan 100mA
- *Bandwidth* yang dapat disesuaikan dari 0 sampai dengan 14%
- Tidak terpengaruh oleh *noise* dan sinyal yang tinggi
- Frekuensi pusat yang dapat disesuaikan dari 0,01 Hz sampai dengan 500 kHz

Aplikasi-aplikasi yang dimiliki LM567:

- *Tone decoding*
- Osilator yang teliti
- *Monitoring* dan kontrol frekuensi
- Demodulasi *band* FSK yang lebar
- Kontrol ultrasonik
- *Carrier* kontrol *remote* tertentu
- *Communications paging decoders*

Tone decoder LM567 ditunjukkan pada Gambar 2.3.



Gambar 2.3 *Tone Decoder* LM567

Sumber : www.national.com, 1999 : 6

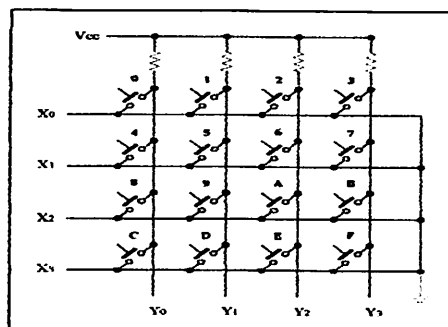
Fungsi dari masing-masing pin adalah:

- Pin 1, 2 terhubung ke *ground* dan kapasitor C_2 dan C_3
- Pin 3 sebagai sinyal *input* dari IR RX (penerima)
- Pin 4 terhubung dengan sumber tegangan sebesar +5V dan kapasitor $1\mu\text{F}$
- Pin 5 terhubung dengan R_1 sebesar $2,4\text{k}\Omega$
- Pin 6 terhubung dengan kapasitor C_1
- Pin 7 terhubung ke *ground*
- Pin 8 terhubung ke sumber tegangan +5V dan R_L

2.3. Keypad 4x4

Dalam perencanaan ini, tombol masukan (*keypad*) yang digunakan adalah *keypad* matrik 4x4. *Keypad* ini berfungsi untuk memberikan masukan kepada mikrokontroler untuk melakukan operasi pengaturan manual, masukan data berupa sembarang tombol untuk *mereset* data pada LCD atau menampilkan *record* yang tersimpan pada mikrokontroler.

Prinsip kerja *keypad* matrik dapat dilihat dari Gambar 2.4.



Gambar 2.4 Keypad dot matrik 4x4

Sumber: Mazidi, 1995: 277

Gambar 2.4 terlihat bahwa *keypad* matrik ini terdiri atas 4 lajur baris (X_0 - X_3) dan 4 lajur kolom (Y_0 - Y_3), dan *keypad* ini akan bekerja dengan menggunakan prinsip *scanning* pada lajur baris dan lajur kolom tersebut. Jika terdeteksi adanya persambungan antara baris dan kolom *valid*, maka data dari *keypad* tersebut akan diterjemahkan pada mikrokontroler.

2.4. Mikrokontroler AT 89S51

Adalah mikrokomputer CMOS 8 bit dengan 4 KB *In-System Programmable Flash* (ISP). Istilah *In-System Programmable* berarti tanpa mencabut dari rangkaian aplikasi, chip dapat diprogram atau diprogram ulang, dengan menghubungkan 4 pin (+1 ground) ke rangkaian programmer (yaitu MOSI pada pin 6, MISO pada pin 7, RST pada pin 9 dan SCK pada pin 8). Mikrokontroler berteknologi *memory non-volatile* berkerapatan tinggi dari Atmel ini kompatibel dengan mikrokontroler MCS-51 (seperti mikrokontroler 8031 yang terkenal dan banyak digunakan beberapa waktu lalu) yang telah menjadi standar industri, baik dalam jumlah pin IC maupun set instruksinya.

Fitur-fitur yang disediakan oleh mikrokontroler produksi Atmel ini adalah sebagai berikut: (sumber : <http://www.atmel.com>, 2001 : 1)

1. 4K bytes flash memory
2. 128 bytes RAM
3. 32 port I/O
4. Watchdog timer
5. Dua buah data pointer
6. 2x 16 bit timer/counter

Gambar 2.4 terlihat bahwa keypad matrik ini terdiri atas 4 baris baris (X_1-X_4) dan 4 kolom kolom (Y_1-Y_4). dan keypad ini akan bekerja dengan menggunakan prinsip scanning baris baris baris dan kolom kolom. Jika terdeteksi adanya pemencatan antara baris dan kolom (nilai), maka data dari keypad tersebut akan diterjemahkan pada mikrokontroler.

2.4. Mikrokontroler AT 89C21

Adalah mikrokontroler CMOS 8 bit dengan 4 Kbit ke-2 program programable flash (EEP) adalah ke-2 program programable memori internal yang digunakan aplikasi chip dapat diprogram ulang dengan menggunakan 4 pin (+1 ground) ke konfigurasi programmer (yaitu MC01 pada pin 6, VCC pada pin 7, RST pada pin 9 dan GND pada pin 2). Mikrokontroler berkekuatan menengah, yang memiliki kemampuan tinggi dan sangat baik untuk digunakan mikrokontroler MC2-31 (kecepatan mikrokontroler 1001 yang rendah dan sangat tinggi untuk beberapa waktu) yang telah menjadi standar industri, baik dalam bentuk pin IC maupun set instruksinya.

Fitur-fitur yang disediakan oleh mikrokontroler produksi Atmel ini adalah

sebagai berikut : <http://www.atmel.com> (2001 : 1)

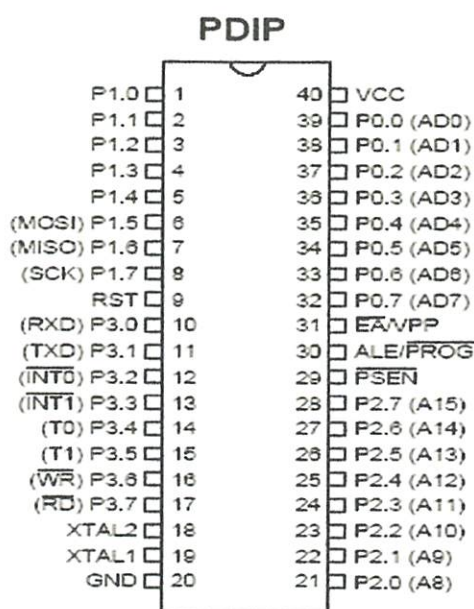
1. 4K bytes flash memory
2. 128 bytes RAM
3. 13 pins I/O
4. Watchdog timer
5. On-chip data pointer
6. 2x 16 bit timer-counter

7. 5 titik dengan 2 level interupsi arsitektur
8. *Full duplex serial port*
9. *On-Chip* osilator
10. *Clock circuit*

Kelebihan lain yang dimiliki adalah AT89S51 didesain dengan mode *static logic* yaitu untuk operasi penurunan frekuensi sampai 0 dan mampu melakukan pemilihan dua *software* untuk mode *power saving*. Kondisi *idle* adalah kondisi dimana CPU dihentikan sementara dan yang diperbolehkan untuk melanjutkan adalah RAM, timer/counter, *serial port* dan interupsi *system*. Pada saat mode *power down*, CPU menyimpan isi dari RAM tetapi menurunkan suhu pada osilator dan menonaktifkan semua chip sampai *external* interupsi selanjutnya atau *reset hardware* dilakukan.

2.4.1. Organisasi dan arsitektur AT89S51

Arsitektur dari mikrokontroler AT89S51 dapat dilihat pada Gambar 2.5.



Gambar 2.5 Pin Konfigurasi Mikrokontroler AT89S51

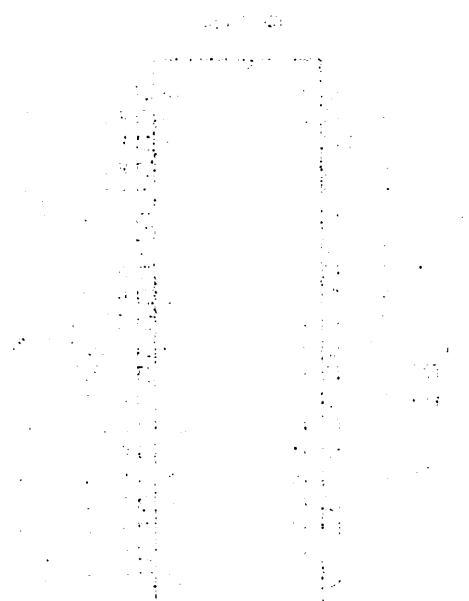
Sumber : <http://www.atmel.com>, 2001 : 2

7. 2 bit dengan 2 level interrupt master
8. Full duplex serial port
9. On-Chip oscillator
10. Clock output

Kelompok lain yang dimiliki adalah AT89C21 diberikan dengan mode write logic yaitu untuk operasi penulisan memori sampai 0 dan mampu melakukan penulisan dan pembacaan mode write. Kondisi write adalah kondisi dimana CPU diberikan alamat dan yang diperbolehkan untuk melakukan adalah RAM mikrokontroler, read port dan interrupt system. Pada saat mode write, CPU mempunyai isi dari RAM tetapi menunjukkan akan pada register dan menunjukkan secara chip sampai interrupt sehingga akan bisa melakukan dilakukan.

2.4.1. Organisasi dan arsitektur AT89C21

Arsitektur dari mikrokontroler AT89C21 dapat dilihat pada Gambar 2.5.



Gambar 2.5. Organisasi mikrokontroler AT89C21

Konfigurasi pin pada mikrokontroler AT89S51:

1. VCC (power supply)
2. GND (ground)
3. Port 0 (port 0.0 0.7)

8 bit *port* I/O dua arah bertipe *open drain* (saluran terbuka). Sebagai *port output*, setiap pin dapat menyerap arus (*sink*) 8 masukan TTL (sekitar 3.8 mA). Pada saat “1” dituliskan ke pin *port* 0, maka pin-pin pada *port* 0 dapat digunakan sebagai tahanan *input* yang tinggi. *Port* 0 dapat juga dikonfigurasi sebagai bus alamat/data bagian rendah (*low byte*) selama pengaksesan *external* program dan data *memory*.

4. Port 1 (port 1.0 1.7)

8 bit *port* I/O dua arah dengan *internal pull up*. Penyangga keluaran (*output buffer*) dari *port* 1 dapat menyerap/menghasilkan arus 4 TTL *input* (sekitar 1.6mA). *Port* ini mempunyai *internal pull up* dan berfungsi sebagai *output* dengan memberikan logika 1. Sebagai *input*, *port* 1 harus diberikan logika 0 karena sifatnya yang *internal pull up*. *Port* 1 juga dapat menerima *low order byte* alamat selama proses *flash programming* dan verifikasi. *Port* ini juga memiliki fungsi alternatif, yaitu pada *port* 1.5 sebagai MOSI (digunakan pada *In-System Programming*), *port* 1.6 sebagai MISO (digunakan pada *In-System Programming*) dan *port* 1.7 sebagai SCK (digunakan pada *In-System Programming*).

5. Port 2 (port 2.0 2.7)

8 bit *port* I/O dua arah dengan *internal pull up*. *Output buffer* dari *port* 2 dapat menghasilkan 4 TTL *input*. Ketika perintah penulisan dilakukan ke *port* ini, pin-pin pada *port* 2 di pull-up menjadi kondisi 1 yang dilakukan oleh *internal pull up* dan dapat digunakan sebagai *inputan*. *Port* 2 berfungsi sebagai I/O biasa atau *high order address*, pada saat mengakses memori secara 16 bit (Movx @DPTR). Pada saat mengakses memori secara 8 bit (Mov @Rn), *port* ini akan mengeluarkan sisi dari *Special Function Register*.

6. Port 3

8 bit *port* I/O dua arah (*bi-directional*) dengan *internal pull up*. *Output buffer* dari *port* 3 dapat memasukkan 4 TTL *input*. Ketika logika 1 ditulis ke pin dari *port* 3, pin dari *port* 3 di pull-up oleh *internal pull up* dan dapat digunakan sebagai *input*. *Port* 3 menerima beberapa sinyal kontrol untuk *flash programming* dan verifikasi. *Port* 3 juga menyediakan fungsi dari fitur-fitur tambahan dari AT89S51, seperti yang ada pada Tabel 2.1.

Tabel 2.1 Fungsi Tambahan dari Port 3

Port Pin	Fungsi Tambahan
P 3.0	RXD (<i>serial input port</i>)
P 3.1	TXD (<i>serial output port</i>)
P 3.2	INT0 (<i>external interupsi 0</i>)
P 3.3	INT1 (<i>external interupsi 1</i>)
P 3.4	T0 (<i>timer 0 external input</i>)
P 3.5	T1 (<i>timer 1 external input</i>)
P 3.6	WR (<i>external data memory write strobe</i>)
P 3.7	RD (<i>external data memory read strobe</i>)

Sumber : <http://www.atmel.com>, 2001 : 5

7. RST

Reset akan aktif dengan memberikan *input 1 (high)* selama 2 siklus mesin selama osilator bekerja.

8. ALE/ $\overline{PROG}$

Pin ini dapat berfungsi sebagai *Address Latch Enable (ALE)* yang menghasilkan pulsa-pulsa untuk mengancing (*latch*) *byte* rendah alamat pada saat mengakses memori *external*. Sedangkan pada saat *flash programming (PROG)* berfungsi sebagai masukan pulsa. Pada operasi normal, ALE akan mengeluarkan sinyal *clock* sebesar 1/16 frekuensi kristal (*oscillator*), kecuali pada saat mengakses memori *external*. Sinyal *clock* pada saat ini dapat pula di-*disable* dengan men-*set* bit 0 *Special Function Register* lokasi 8Eh.

Table 2.1. Fungsi Transmisi dari Port 2

Port Pin	Fungsi Transmisi
P.2.0	RXD (Serial Input Port)
P.2.1	TXD (Serial Output Port)
P.2.2	INT0 (Interrupt Input 0)
P.2.3	INT1 (Interrupt Input 1)
P.2.4	T0 (Timer 0 External Input)
P.2.5	T1 (Timer 1 External Input)
P.2.6	WR (External Memory Access Strobe)
P.2.7	R1 (External Memory Access Strobe)

Sumber : *Microcontroller 2001* : 3

5. RST

Renov akan aktif dengan membalikan byte 1 (high) saluran 2 saluran mesin
saluran saluran kontrol.

8. ALE/PROG

Pin ini dapat berfungsi sebagai Address Latch Enable (ALE) yang
menghasilkan pulsa-pulsa untuk menginisiasi (latch) data ke dalam alamat pada
satu perangkat memori eksternal. Sedangkan pada saat high programming
(PROG) berfungsi sebagai masukan pulsa. Pada operasi normal, ALE akan
menghasilkan sinyal clock sebesar 1/10 frekuensi kristal (crystal/10). Untuk
pada saat program memori external, signal clock pada pin ini dapat pada the
clock dengan mem-zat pin 0 special function pin yang telah RST.

9. $\overline{PSEN}$

Program Store Enable adalah sinyal membaca ke *external program memory*. Saat AT89S51 mengeksekusi program dari *external program memory*, $\overline{PSEN}$ diaktifkan setiap 2 siklus kecuali dua aktivasi $\overline{PSEN}$ tidak dilakukan/dilompati saat mengakses *external data memory*.

10. $\overline{EA} / V_{PP}$

Pada kondisi *low*, pin ini akan berfungsi sebagai $\overline{EA}$ yaitu mikrokontroler akan menjalankan program yang ada pada memori eksternal setelah sistem di *reset*. Jika berkondisi *high*, pin ini akan berfungsi untuk menjalankan program yang ada pada memori *internal*. Pada saat *flash programming* pin ini akan mendapat tegangan 12 Volt (V_{PP}).

11. XTAL1

Masukan ke *inverting* osilator amplifier dan masukan ke *internal clock operating circuit*.

12. XTAL2

Keluaran dari *inverting* osilator amplifier. Semua mikrokontroler 51 Atmel memiliki osilator *on-chip*, yang dapat digunakan sebagai sumber detak (*clock*) ke CPU. Untuk menghubungkannya, hubungkan sebuah resonator kristal atau keramik di antara kaki-kaki XTAL1 dan XTAL2 pada mikrokontroler dan hubungkan kapasitornya ke ground seperti pada Gambar 2.6.

матрицы $\mathbf{K}$ и $\mathbf{L}$ по формулам

բանալիք որ առաջ բերէր: ԻՆՎԵՆ ԳՈՒ ԻՆՎԵՆ Ինչո՞ւ սիրաբանութիւն զո՞ւ
ՇԿՐՒ Բարեկ. անհրաժեշտութեանը արժանաւոր չարաւոր ինչո՞ւ որո՞ւ
անսովոր օգնելու օւժ-հանձն չաւի՞ր զո՞ւր որմանքսն չարսնիւ չարաւոր գտիւք (հազա՞) ԲՆ

Հայաստանի գյուղատնտեսական օգնության ջանքերի կոորդինացիայի 21 խումբ

Մ.Է.ԼՎԻՏ

SECRET

Указание по вопросам содержания, что указывается по данному делу.

[XIV]

លេខប្រតិបត្តិការ ២៩០២ : ២៩.២.២០២២

[illegible]

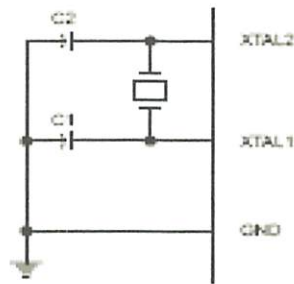
Бүгд хамтдаа үнэ-хэргийг эргэлтэд оруулан шалгахыг зорьж байна.

10. УТ, А-ийг

2001 HUGHES/2002 COLEMAN, Q565 WASHINGTON:

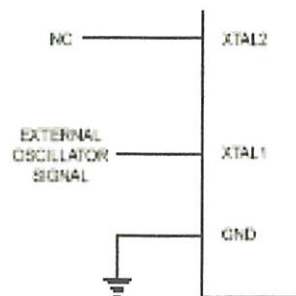
[illegible]

PROBLEM 2: Find the area of the region bounded by the curves $y = x^2$ and $y = 2x - x^2$.



Gambar 2.6 XTAL1 dan XTAL 2 Sebagai Koneksi Osilator
 Sumber : <http://www.atmel.com>, 2001 : 11

Untuk mengoperasikan sebuah alat melalui sumber *clock* eksternal, maka XTAL2 harus tidak terhubung selama XTAL1 beroperasi, seperti pada Gambar 2.7.



Gambar 2.7 XTAL1 dan XTAL2 Sebagai Konfigurasi *External Clock Drive*
 Sumber : <http://www.atmel.com>, 2001 : 11

2.4.2. Blok Diagram AT89S51

Dengan keistimewaan yang ada pada AT89S51, pembuatan alat penghitung waktu tempuh dan kecepatan menjadi lebih sederhana dan tidak memerlukan IC pendukung yang banyak. Boleh dikatakan mikrokontroler ini mempunyai keistimewaan di bidang perangkat keras. Blok diagram dari mikrokontroler AT89S51 diperlihatkan pada Gambar 2.8.

Gambar 3.6 XTA11 dan XTA12 sebagai Koneksi Keleburan
Sumber : [11] 2001

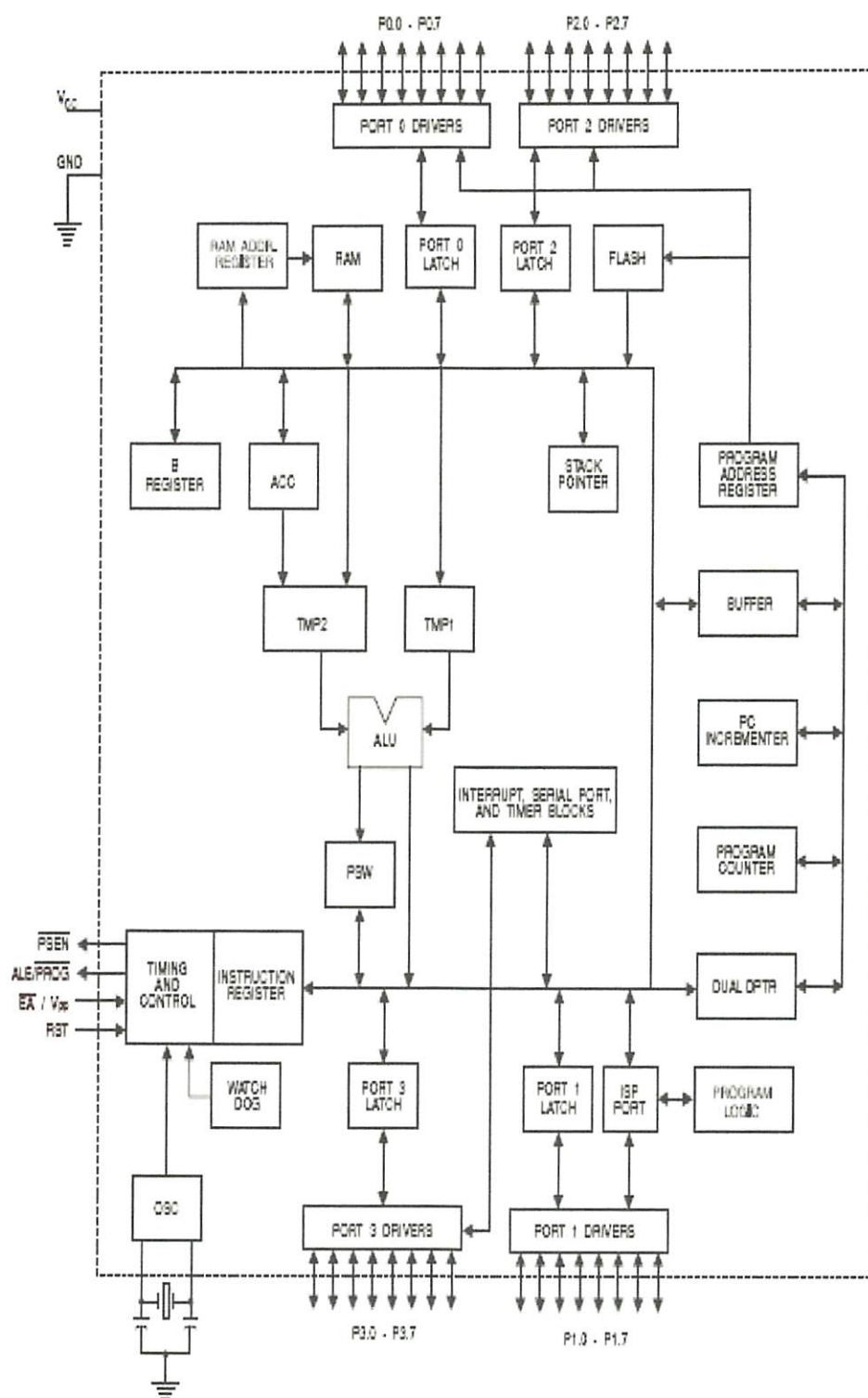
Guna memperjelas skema atau menjadi sumber daya eksternal maka

XTA12 pada tidak terdapat skema XTA11 terdapat seperti pada Gambar 3.7.

Gambar 3.7 XTA11 dan XTA12 sebagai Koneksi Keleburan
Sumber : [11] 2001

3.1.3 Blok Diagram AT89251

Untuk kegunaan yang ada pada AT89251, penggunaan ini penting untuk setiap dan kegunaan menjadi lebih sederhana dan tidak memerlukan IC. Keleburan yang banyak. Blok diagram mikrokontroler ini menunjukkan kegunaan di bidang perantara ke. Blok diagram dan mikrokontroler AT89251 diberikan pada Gambar 3.8.



Gambar 2.8 Blok Diagram Mikrokontroler AT89S51

Sumber : <http://www.atmel.com>, 2001 : 3

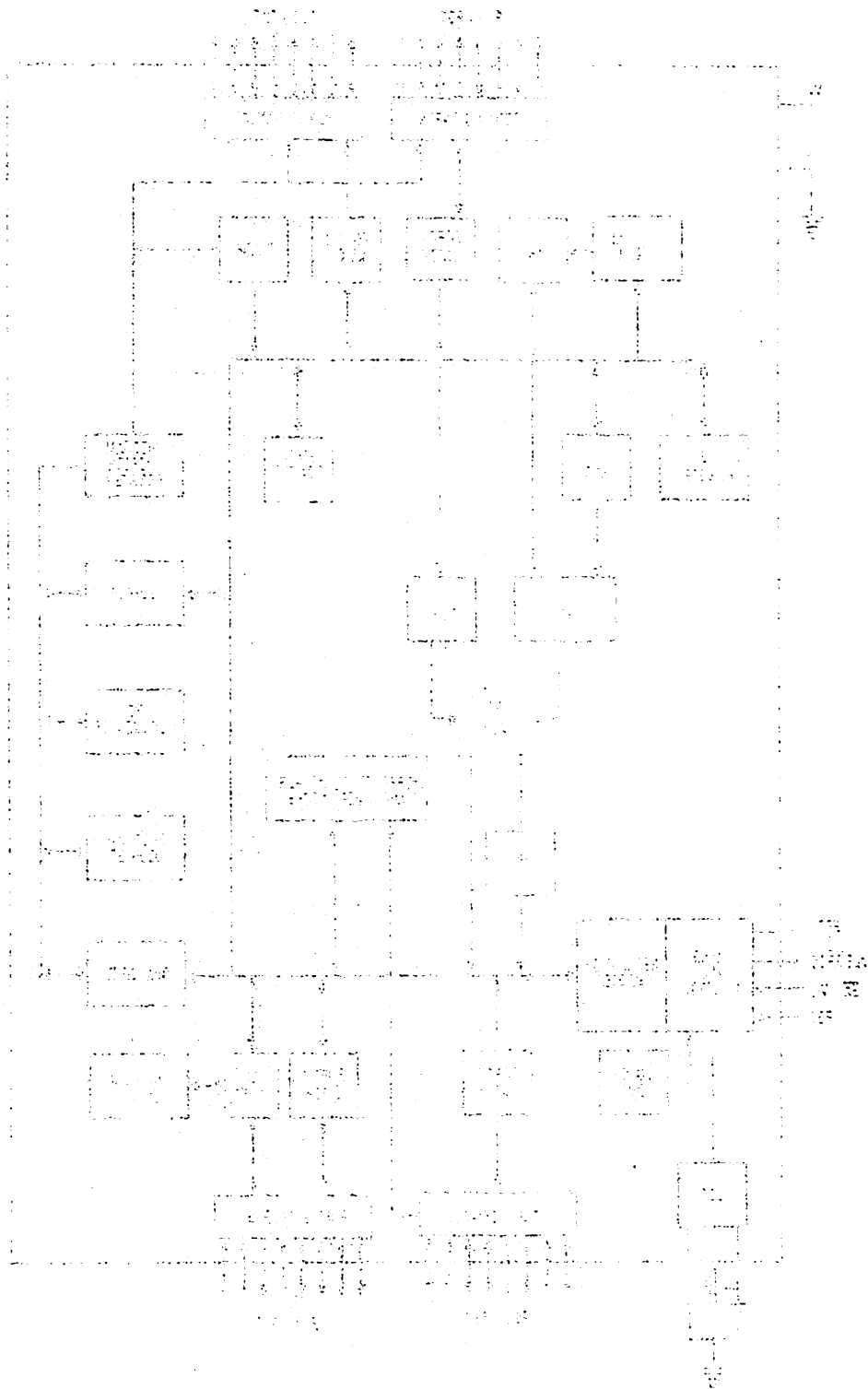


Diagram 2.8 Block Diagram of the Z80-based microcomputer system
 (Source: [illegible] 1981, p. 100)

2.4.3. SFR (Special Function Register)

Gambaran dari area chip *memory* dinamakan *Special Function Register* (SFR) seperti yang ditunjukkan pada Tabel 2.2.:

Tabel 2.2 Tabel SFR

0F3H								0FFH
0F0H	B 00000000							0F7H
0E3H								0EFH
0E0H	ACC 00000000							0E7H
0D3H								0DFH
0D0H	PSW 00000000							0D7H
0C3H								0CFH
0C0H								0C7H
0B3H	IP XX000000							0BFH
0B0H	P3 11111111							0B7H
0A3H	IE 0X000000							0AFH
0A0H	P2 11111111	AUXR1 XXXXXXXX				WDTRST XXXXXXXX		0A7H
93H	SCON 00000000	SBUF XXXXXXXX						9FH
90H	P1 11111111							97H
83H	TCON 00000000	TMOD 00000000	TLO 00000000	TL1 00000000	TH0 00000000	TH1 00000000	AUXR XXXX0XXX	8FH
80H	P0 11111111	SP 00000111	DPOL 00000000	DP0H 00000000	DP1L 00000000	DP1H 00000000		87H
							PCON 0XXX0000	

Sumber : <http://www.atmel.com>, 2001 : 6

Interupsi register adalah *individual* interupsi yang meng-*enable* kan bit-bit yang ada di IE register. Dua prioritas (prioritas tinggi dan prioritas rendah) dapat diset untuk setiap dari lima buah sumber interupsi yang ada dalam IP register.

Special Function Register (Register Fungsi Khusus), memori yang berisi register-register yang mempunyai fungsi-fungsi khusus yang disediakan oleh mikrokontroler tersebut, seperti timer, serial dan lain-lain.

(Continued from page 120) (continued)

Table 1.1. (continued)

Table 1.1. (continued)

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Source: U.S. Census Bureau.

... (text continues) ...

Berikut ini penjelasan singkat tentang fungsi SFR:

- **ACC (Akumulator)**

ACC atau akumulator yang menempati lokasi E0H digunakan sebagai register untuk penyimpanan data sementara, dalam program, intruksi mengacunya sebagai register A (bukan ACC).

- **Register B**

Register B (lokasi F0H) digunakan selama operasi perkalian dan pembagian, untuk instruksi lain dapat diperlakukan sebagai register *scratch pad* (“papan coret-core””) lainnya.

- **PSW(Program Status Word)**

Register PSW (lokasi D0H) berisi bit-bit status yang berkaitan dengan kondisi CPU saat itu. Status yang tersimpan dalam PSW meliputi : *carry bit*, *the auxiliary carry* (untuk operasi BCD), dua bit pemilih bank register, *overflow flag*, sebuah bit paritas dan dua *flag* status yang bisa didefinisikan sendiri (*user definable*).

- **Stack Pointer (SP)**

Stack Pointer (lokasi 81H) merupakan register dengan panjang 8-bit, digunakan dalam proses simpan dan ambil dari/ke *stack* (tumpukan). Nilainya akan dinaikkan sebelum data disimpan menggunakan instruksi *PUSH* dan *CALL*. Walau *stack* bisa menempati lokasi dimana saja dalam RAM, register SP akan selalu diinisialisasi ke 07H setelah adanya *reset*, hal ini menyebabkan *stack* berawal dilokasi 08H.

- **Data Pointer (DPTR)**

Register data pointer atau DPTR untuk *byte* tinggi (DPH) dan *byte* rendah (DPL) yang masing-masing berada dilokasi 82H dan 83H, bersama-sama membentuk register yang mampu menyimpan alamat 16-bit. Dapat dimanipulasi sebagai register 16-bit atau sebagai dua register 8-bit yang terpisah.

- **Port 0, port 1, port 2 dan port 3**

P0, P1, P2 dan P3 masing-masing menempati lokasi 80H, 90H, A0H dan B0H merupakan pengunci-pengunci (*latches*), yang digunakan untuk menyimpan data yang akan dibaca atau ditulis ke/dari *port* untuk masing-masing *port* 0, *port* 1, *port* 2 dan *port* 3.

- **Serial Data Buffer (SBUF)**

SBUF atau *serial data buffer* (lokasi 99H) sebenarnya terdiri dari dua register yang terpisah, yaitu register penyangga pengirim (*transmit buffer*) dan penyangga penerima (*receive buffer*). Pada saat data disalin ke SBUF, maka data sesungguhnya dikirim ke penyangga pengirim dan sekaligus mengawali transmisi data serial. Sedangkan pada saat data disalin dari SBUF, maka sebenarnya data tersebut berasal dari penyangga penerima.

- **Timer Register**

Pasangan register (TH0, TL0) dilokasi 8CH dan 8AH, (TH1, TL1) dilokasi 8DH dan 8BH merupakan register-register pencacah 16-bit untuk masing-masing timer 0 dan timer 1. TL0, TH0, TL1 dan TH1 dipakai untuk membentuk pencacah biner Timer 0 dan Timer 1. Kapasitas keempat register tersebut masing-masing 8 bit, bisa disusun menjadi empat macam mode pencacah biner.

• Data Pointer (DPTR)

Register data pointer atau DPTR untuk byte tinggi (DPH) dan byte rendah (DPL). Yang masing-masing berada di lokasi 82H dan 83H. Berasasamaan memfungsikan register yang memiliki menunjukkan alamat 16-bit. Dapat dioperasikan sebagai register 16-bit atau sebagai dua register 8-bit yang terpisah.

• Port 0, Port 1, Port 2 dan Port 3

P0, P1, P2 dan P3 masing-masing menunjukkan lokasi 80H, 81H, 82H dan 83H merupakan bus-bus-bus (bus) yang digunakan untuk menunjukkan data yang akan dibaca atau ditulis ke/dari bus untuk masing-masing port 0, port 1, port 2 dan port 3.

• Serial I/O Buffer (SBUF)

SBUF atau serial I/O buffer (lokasi 90H) sebenarnya terdiri dari dua register yang terpisah, yaitu register penerima (receive buffer) dan register pemancar (transmit buffer). Pada saat data dikirim ke SBUF, maka data akan langsung dikirim ke bus-bus yang digunakan dan sebaliknya menerima data serial. Sedangkan pada saat data dikirim dari SBUF, maka sebenarnya data tersebut berasal dari bus-bus yang pemancar.

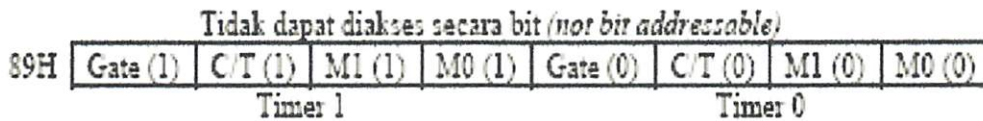
• Timer Register

Program register (TH0, TL0) di lokasi 84H dan 85H (TH1, TL1) di lokasi 86H dan 87H merupakan register-register beracak 16-bit untuk masing-masing timer 0 dan timer 1. TH0, TL0, TH1 dan TL1 diberikan untuk membandingkan dengan timer 0 dan timer 1. Kapasitas counter register tersebut masing-masing 8 bit, bisa digunakan untuk menghitung mode beracak timer.

- **Control Register**

Register IP, IE, TMOD (*Timer Mode Register*, memori data internal alamat 89H, tidak bisa dialamati per bit), TCON (*Timer Control Register*, memori data internal alamat 88H, bisa dialamati per bit), SCON dan PCON berisi bit-bit kontrol dan status untuk sistem interupsi.

Register TMOD seperti pada Gambar 2.9.

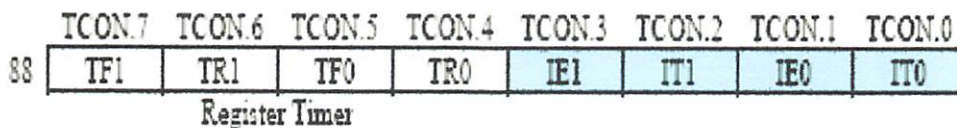


Gambar 2.9 Susunan bit dalam register TMOD
 Sumber : <http://www.delta-electronics.com>, 2001 : 1

Susunan bit pada TMOD yang harus di *set*:

- Gate: Timer akan berjalan bila bit ini set dan INT0 (untuk Timer 0) atau INT1 (untuk Timer 1) berkondisi high
- C/T: 1 = Counter, 0 = Timer
- M1 & M0: Untuk memilih mode timer

Register TCON ditunjukkan pada Gambar 2.10.



Gambar 2.10 Susunan bit dalam register TCON
 Sumber : <http://www.delta-electronics.com>, 2001 : 1

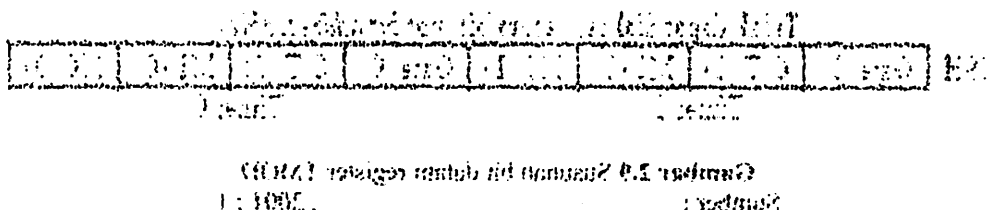
Pada register ini, hanya 4 bit saja yaitu TCON.4, TCON.5, TCON.6 dan TCON.7 saja yang mempunyai fungsi berhubungan dengan timer.

Pengaturan bit pada register TCON ini adalah:

• **Control Register**

Register IP, IE, TMR0 (Timer Above Register), mengatur dan interval alarm 88H, bisa diabaikan per bit. TMR0 (Timer Above Register), mengatur dan interval alarm 88H, bisa diabaikan per bit. SCOR dan PCOR berisi bit-bit kontrol dan status untuk interval.

Register TMR0 seperti pada (gambar 3.9).



Gambar 3.9 Struktur bit dalam register TMR0
Sumber : [10]

Struktur bit pada TMR0 yang harus di set:

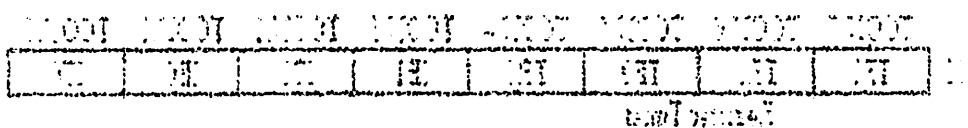
• **Timer 0 akan berjalan bila bit ini set dan INT0 (untuk Timer 0) atau**

INT1 (untuk Timer 1) berkebalikan high

• **CVT: 1 = Counter, 0 = Timer**

• **M1 & M0: Untuk memilih mode timer**

Register TCON ditunjukkan pada (gambar 3.10).



Gambar 3.10 Struktur bit dalam register TCON
Sumber : [10]

Pada register ini, bagian 4 bit saja yaitu TCON4, TCON5, TCON6, dan

TCON7 saja yang mempunyai fungsi berhubungan dengan timer.

Pengaturan bit pada register TCON ini adalah:

- TCON.7 atau TF1: Timer 1 *Overflow* Flag yang akan set bila timer *overflow*. Bit ini dapat di-clear oleh *software* atau oleh *hardware* pada saat program menuju ke alamat yang ditunjuk oleh interrupt vector.
- TCON.6 atau TR1:1 = Timer 1 aktif, 0 = Timer 1 non aktif
- TCON.5 atau TF0: Timer 0 *Overflow* Flag yang akan set bila timer *overflow*. Bit ini dapat di-clear oleh *software* atau oleh *hardware* pada saat program menuju ke alamat yang ditunjuk oleh interrupt vector.
- TCON.4 atau TR0: 1 = Timer 0 aktif, 0 = Timer 0 non aktif

- **Watch Dog Timer (WDTRST)**

WDT bertujuan untuk *me-recovery* CPU. WDT terdiri dari 14 bit *counter* dan *Watch Dog Timer Reset* (WDTRST) SFR. Fungsi WDT adalah untuk *disable reset*.

Untuk meng-*enable* kan WDT, *user* harus menulis 01EH dan 0E1H dalam antrian ke register WDTRST (lokasi di SFR 0A6H). Ketika WDT *enable*, hal ini akan mengakibatkan kenaikan *cycle* ketika osilator sedang *running*. Masa WDT habis akan tergantung pada *external clock* frekuensi. Tidak ada jalan lain untuk *disable* kan WDT kecuali melalui *reset* (*hardware reset* atau *WDT overflow reset*). Ketika WDT *overflow*, hal ini akan menyebabkan *output reset* pada keadaan logika tinggi yang artinya terjadinya *reset* pada pin RST.

2.4.4. Organisasi *Memory*

MCS-51 memiliki *space address* untuk program dan data *memory*. Sampai dengan 64 KB untuk setiap *external* program dan data *memory* yang dapat dialamati.

Program *memory*, jika pin EA dihubungkan ke GND (*ground*), maka semua program langsung tersimpan ke *external memory*. Pada AT89S51, jika EA dihubungkan ke Vcc, maka program langsung tersimpan ke *internal memory* yang beralamatkan 0000H sampai dengan FFFFH

Data *memory*, AT89S51 memiliki 128 *byte* RAM. 128 *byte* tersebut dapat diakses secara *direct* (langsung) atau *indirect addressing mode* (tidak langsung). Sebagai contoh dari pengalamatan secara tidak langsung (*indirect addressing mode*) adalah operasi *stack*, sehingga 128 *byte* data dari RAM tersedia untuk *stack*.

2.4.5. Interupsi

AT89S51 memiliki 5 interupsi, yaitu : dua *external* interupsi (INT0 dan INT1), dua timer interupsi (T0 dan T1) dan *serial port* interupsi. Setiap interupsi di atas dapat meng-*enable* atau men-*disable* secara manual dengan men-*setting* atau menghapus satu bit pada IE di SFR. IE merupakan global bit *disable* yang dapat men-*disable* kan semua interupsi. *Flag* timer 0 dan timer 1 (TF0 dan TF1) di *set* pada S5P2 dari *cycle* jika timer *overflow*.

Register IE ditunjukkan pada Tabel 2.3 :

Tabel 2.3 Tabel IE Register

(MSB)				(LSB)			
EA	-	-	ES	ET1	EX1	ET0	EX0
Enable Bit = 1 enables the interrupt.							
Enable Bit = 0 disables the interrupt.							

Symbol	Position	Function
EA	IE.7	Disables all interrupts. If EA = 0, no interrupt is acknowledged. If EA = 1, each interrupt source is individually enabled or disabled by setting or clearing its enable bit.
-	IE.6	Reserved
-	IE.5	Reserved
ES	IE.4	Serial Port interrupt enable bit
ET1	IE.3	Timer 1 interrupt enable bit
EX1	IE.2	External interrupt 1 enable bit
ET0	IE.1	Timer 0 interrupt enable bit
EX0	IE.0	External interrupt 0 enable bit
User software should never write 1s to reserved bits, because they may be used in future AT92 products.		

Sumber : <http://www.atmel.com>, 2001 : 10

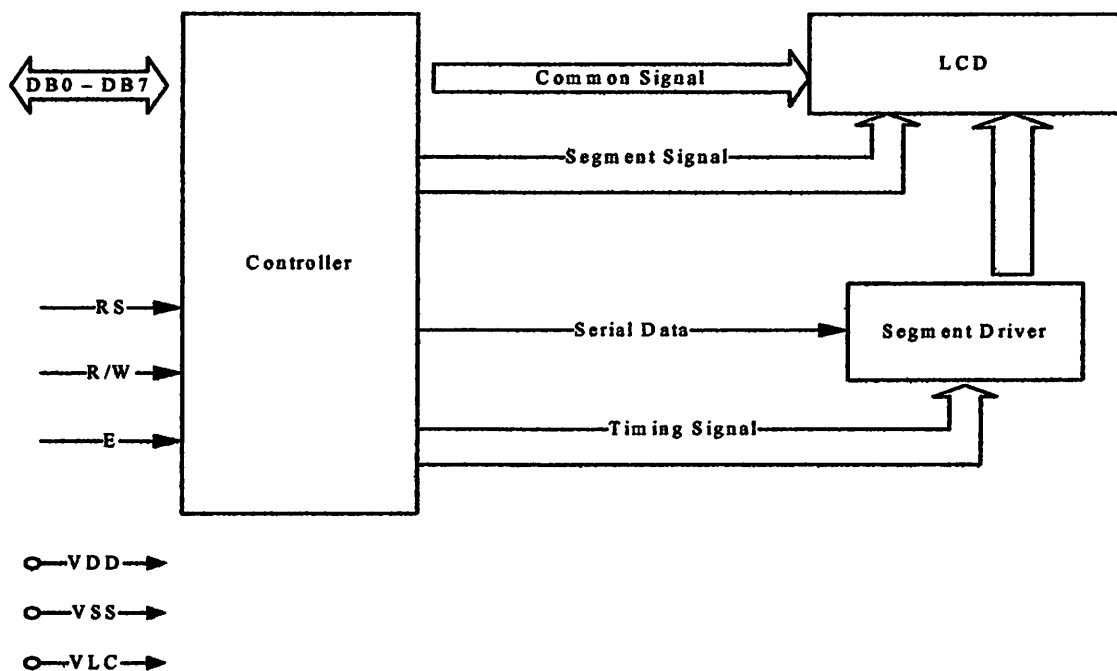
2.5. LCD (*Liquid Crystal Display*)

LCD yang digunakan adalah Seiko tipe M1632 adalah LCD dot matrik yang membutuhkan daya yang rendah dengan kontras warna yang tinggi dengan penggunaan layar TN panel dan sudah dilengkapi dengan CMOS LCD drive kontroler. Kontroler tersebut dibuat pada karakter generator ROM/RAM dan *display* data RAM. Semua fungsi tampilan diatur oleh instruksi dan modulnya dapat diinterface-kan dengan MPU (Mikroprosesor Unit). Blok diagram dari LCD dapat dilihat pada Gambar 2.11.

Register II diunduh pada Tabel 2.3 :

Tabel 2.3 Tabel II Register

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Gambar 2.11 Blok Diagram LCD M1632
Sumber : Seiko, 1987; 3

Fitur-fitur yang dimiliki adalah sebagai berikut:

1. 16 karakter dengan 2 baris TN LCD dengan 5x7 dot matrik dan cursor.
2. Rasio 1/16.
3. Karakter generator ROM untuk 192 jenis karakter (dengan ukuran huruf 5x7 dot matrik).
4. Karakter generator RAM untuk 8 jenis karakter (program penulisan) (dengan ukuran huruf 5x7 dot matrik).
5. Tampilan data RAM 80x8 (maksimum 80 karakter).
6. Dengan *interface* 4 bit dan 8 bit ke MPU.
7. Tampilan data RAM dan karakter generator RAM dapat dibaca dari MPU.
8. Instruksi yang dapat dilakukan : *Display clear*, *cursor home*, *display ON/OFF*, *cursor ON/OFF*, *display karakter blink*, *cursor shift* dan *display shift*.

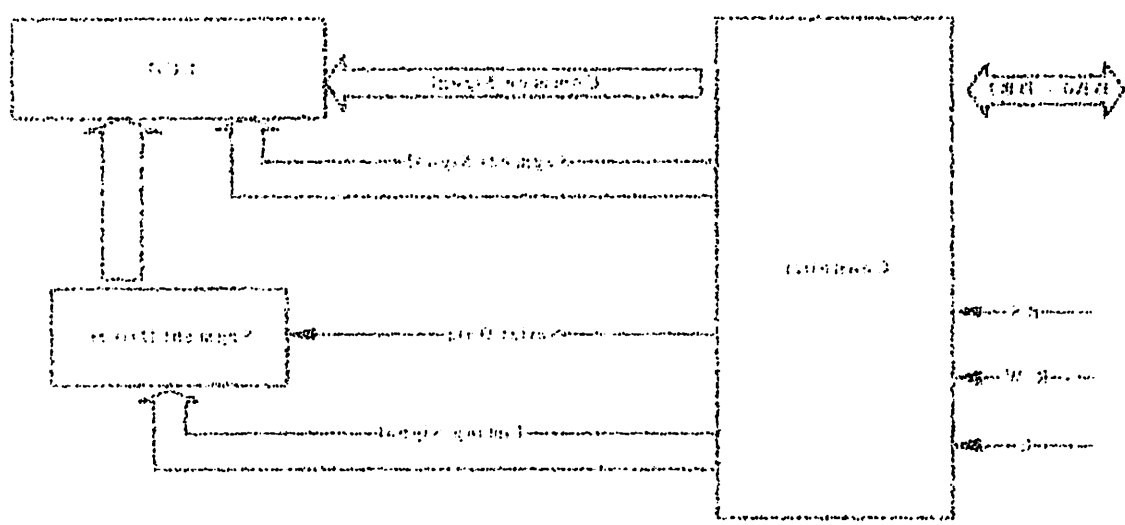


Diagram 2.11 Blok Diagram CPU dan Memori
Sumber: (Sugeng, 2007: 1)

Diagram yang menunjukkan blok-blok sistem komputer

1. CPU (Central Processing Unit) yang terdiri dari ALU (Arithmetic Logic Unit) dan CU (Control Unit).
2. RAM (Random Access Memory).
3. Karakteristik RAM untuk 1024 jenis karakter dengan alamat bus 20 bit.
4. Karakteristik RAM untuk 8 jenis karakter dengan bus 8 bit.
5. Karakteristik RAM untuk 256 jenis karakter dengan bus 8 bit.
6. Karakteristik RAM untuk 256 jenis karakter dengan bus 8 bit.
7. Karakteristik RAM untuk 256 jenis karakter dengan bus 8 bit.
8. Karakteristik RAM untuk 256 jenis karakter dengan bus 8 bit.

9. Dilengkapi *circuit* osilator.
10. *Single power supply* +5 V.
11. Dilengkapi dengan otomatis *reset* pada saat *power-on*.
12. Proses CMOS.
13. Kisaran suhu pada LCD 0°C to 50°C.

Operasi-operasi yang dimiliki LCD adalah:

- Register

Kontroler pada LCD memiliki dua jenis register 8 bit, yaitu *instruction* register (IR) dan data register (DR). Dua register tersebut dipilih melalui sinyal yang dikirim oleh register *select* (RS) seperti ditunjukkan pada Tabel 2.4.

Tabel 2.4 Register Selection

RS	R/W	Operation
0	0	Seleksi IR, IR <i>write display clear</i>
0	1	<i>Busy Flag</i> (DB7), <i>address counter</i> (DB0-DB7) <i>read</i>
1	0	Seleksi DR, DR <i>write</i>
1	1	Seleksi DR, DR <i>read</i>

Sumber : Seiko, 1987 : 8

IR menyimpan kode-kode instruksi seperti *display clear* dan *cursor shift*, *address information* dari *display data RAM* (DD RAM) dan *character generator RAM* (CG RAM). Kode-kode instruksi tersebut dapat ditulis dari MPU tetapi tidak dapat dibaca dari MPU.

DR menyimpan data untuk ditulis ke DD RAM atau CG RAM atau dibaca dari DD RAM atau CG RAM. Ketika data ditulis ke DD RAM atau CG RAM dari MPU, data pada DR secara otomatis ditulis ke DD RAM atau CG RAM melalui *internal operation*. Walaupun ketika data dibaca dari DD RAM

- 9. Ditampilkan secara online.
 - 10. Supply power supply +5 V.
 - 11. Ditampilkan dengan otomatis every pada saat power-on.
 - 12. Proses CMOS.
 - 13. Kisanan suhu pada LCD 0°C to 50°C.
- Operasi-operasi yang dimiliki LCD adalah:

• Register

Kontroler pada LCD memiliki dua jenis register & bit yaitu instruction register (IR) dan data register (DR). Dua register tersebut dipilih melalui sinyal yang ditulis oleh register select (RS) seperti ditunjukkan pada Tabel 2.4.

Tabel 2.4 Register Selection

RS	RAV	Operation
0	0	Select IR, IR write display clear
0	1	Busy Flag (DB7), address counter (DB0-DB7) read
1	0	Select DR, DR write
1	1	Select DR, DR read

Number : 2010, 1987 : 8

IR menyimpan kode-kode instruksi seperti display clear dan cursor shift. address information dari display data RAM (DD RAM) dan character generator RAM (CG RAM). Kode-kode instruksi tersebut dapat ditulis dari MPU tetapi tidak dapat dibaca dari MPU.

DR menyimpan data untuk ditulis ke DD RAM atau CG RAM atau dibaca dari DD RAM atau CG RAM. Ketika data ditulis ke DD RAM atau CG RAM dari MPU, data pada DR secara otomatis ditulis ke DD RAM atau CG RAM melalui internal operation. Walaupun ketika data dibaca dari DD RAM

atau CG RAM, alamat data tetap ditulis ke IR. Data yang dibaca oleh DR kemudian akan dibaca oleh MPU. Setelah operasi *read*, alamat berikutnya di *set* dan data yang ada di alamat DD RAM atau CG RAM dibaca oleh DR untuk operasi *read* selanjutnya.

- *Busy Flag* (BF)

Flag mengindikasikan apakah modul telah siap untuk menerima instruksi berikutnya. Seperti yang ditunjukkan pada TABEL 2.4, sinyal tersebut adalah keluaran menuju DB7 jika RS=0 dan R/W=1. Jika nilai sinyal tersebut 1, modul akan melakukan kerja internal dan instruksi tidak dapat diterima. Jika nilai sinyal tersebut adalah 0 maka instruksi berikutnya dapat ditulis. Oleh karena itu status *flag* tersebut harus dicek sebelum mengeksekusi sebuah instruksi. Jika sebuah instruksi dieksekusi tanpa mengecek status *flag* tersebut maka akan dilakukan proses menunggu untuk waktu yang lebih lama dari *execution time* (1.64 ms).

- *Address Counter* (AC)

Counter menghususkan sebuah alamat saat data ditulis ke DD RAM atau CG RAM dan data disimpan di DD RAM atau CG RAM untuk dibaca. Jika sebuah alamat memberikan instruksi (untuk DD RAM atau CG RAM) yang ditulis di IR, maka informasi alamat dikirim dari IR menuju AC. Ketika *display* data ditulis pada atau dibaca dari DD RAM atau CG RAM, maka secara otomatis AC mengalami kenaikan atau penurunan satu angka menurut *Entry Mode Set*. Isi AC adalah keluaran dari DB0 sampai DB6 seperti yang ditunjukkan pada TABEL 2.4 jika RS=0 dan R/W=1.

dan CG RAM, alamat data tetap ditulis ke IR. Data yang dibaca oleh DR kemudian akan ditulis oleh MFC. Setelah operasi selesai, alamat bus yang di tulis ke data yang ada di alamat DD RAM atau CG RAM dibaca oleh DR untuk operasi yang selanjutnya.

• Bus Vag (V)

Bus mengindikasikan apakah modul telah siap untuk menerima instruksi berikutnya. Seperti yang ditunjukkan pada TABLE 2.4, sinyal tersebut adalah kolerasi antara DB7 jika RS=0 dan RW=1. Jika nilai sinyal tersebut 1, modul akan melakukan kerja internal dan instruksi tidak dapat diterima. Jika nilai sinyal tersebut adalah 0 maka instruksi berikutnya akan ditulis. Oleh karena itu status Vag tersebut harus di cek sebelum menggunakan sebuah instruksi. Jika sebuah instruksi dieksekusi tanpa mengecek status Vag tersebut maka akan dilakukan proses menunggu untuk waktu yang lebih lama dari menunggu bus (1.64 ms).

• Address Counter (AC)

Counter menginformasikan sebuah alamat saat data ditulis ke DD RAM atau CG RAM dan data diambil dari DD RAM atau CG RAM untuk dibaca. Jika sebuah alamat memberikan instruksi (untuk DD RAM atau CG RAM) yang ditulis di IR, maka informasi alamat dikirim dari IR menuju AC. Ketika akses data ditulis pada bus dibaca dari DD RAM atau CG RAM, maka secara otomatis AC menginformasikan akan pemberian satu angka menuju Vag, block 2.4.1a. AC adalah keluaran dari DB0 sampai DB6 seperti yang ditunjukkan pada

TABLE 2.4 jika RS=0 dan RW=1.

- ***Display Data RAM (DD RAM)***

DD RAM memiliki kapasitas sampai 80 x 8 bit dan menyimpan *display* data dari 80-8 bit kode-kode karakter. Beberapa tempat penyimpanan dari DD RAM tidak dapat digunakan untuk menampilkan, dapat dipakai sebagai *general data RAM*.

Sebuah alamat DD RAM yang di *set* pada AC ditampilkan dalam bentuk heksadesimal. Alamat DD RAM 00H sampai 0FH berada pada *line* satu dan 40H sampai dengan 4FH berada pada *line* dua.

- ***Character Generator ROM (CG ROM)***

Character generator ROM menghasilkan 192 tipe dari 5 x 7 dot matrik pola karakter dari delapan bit karakter kode.

- ***Character Generator RAM (CG RAM)***

CG RAM digunakan untuk membuat karakter bebas dengan pemrograman. Delapan tipe dari pola karakter dapat ditulis.

berfungsi untuk mengatur arus yang masuk ke busbar busbar

CC KVM digunakan untuk mengatur busbar busbar busbar

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Konfigurasi pin-pin LCD M1632 ditunjukkan pada Tabel 2.5.

Tabel 2.5 Konfigurasi Pin-pin LCD M1632

No. pin	Nama Penyemat	Fungsi
1	Vss	Terminal <i>ground</i>
2	Vcc	Tegangan catu +5 Volt
3	Vee	Penyetelan kontras pada tampilan LCD
4	RS	Sinyal pemilih register: 0: instruksi register (tulis) 1: data register (baca dan tulis)
5	R/W	Sinyal seleksi tulis atau baca 0: tulis 1: baca
6	E	Sinyal operasi awal, sinyal ini mengaktifkan data tulis dan baca
7-14	DB0-DB7	Merupakan saluran data, berisi perintah dan data yang akan ditampilkan
15	V+BL	Pengendali kecerahan latar belakang LCD 4-4,42 volt dan 50-500 mA
16	V-BL	Pengendali kecerahan latar belakang LCD 0 volt

Sumber : Seiko, 1987 ; 2

2.6 Regulator LM7805

MC78XX/LM78XX/MC78XXA adalah salah satu seri dari tiga terminal regulator positif yang tersedia pada paket TO-220/D-PAK dan memiliki beberapa tegangan keluaran bernilai tetap yang berguna untuk banyak aplikasi. Setiap jenis dari MC78XX/LM78XX/MC78XXA meningkatkan kinerja dari *internal current*

Konfigurasi pin-pin LCD M1632 ditunjukkan pada Tabel 3.2.
Tabel 3.2 Konfigurasi Pin-pin LCD M1632

No. pin	Nama Pin	Fungsi
1	Vss	Terminal ground
2	Vcc	Tegangan +5 Voh
3	Vce	Pengaturan kontras pada tampilan LCD
4	RS	Signal perintah register: 0: instruksi register (init) 1: data register (data dan tulis)
5	R/W	Signal select tulis atau baca 0: tulis 1: baca
6	E	Signal operasi read, write dan mengaktifkan data tulis dan baca
7-14	DB0-DB7	Menerima status data, berisi perintah dan data yang akan diproses
15	V-BL	Pengaturan kecerahan latar belakang LCD 4-14 Voh dan 50-500 mA
16	V-BL	Pengaturan kecerahan latar belakang LCD 0 Voh

Sumber: [28], [29], [30]

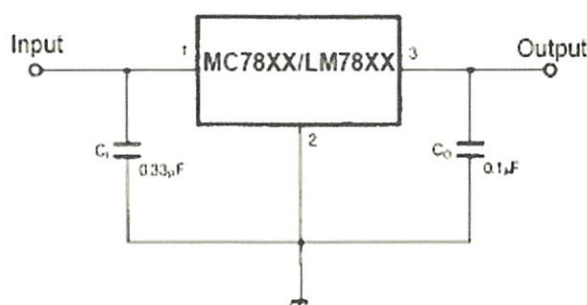
3.2 Regulator LM7805

MC78XXLM78XX/MC78XX adalah salah satu seri dari tiga terminal regulator positif yang tersedia pada paket TO-18/TO-9/TO-18 yang memiliki beberapa tegangan keluaran berbeda untuk berbagai aplikasi. Seris ini juga dapat MC78XXLM78XX/MC78XX menggunakan kinerja dan secara umum

limiting, yang meliputi penurunan suhu panas dan *safe operating area protection*, dan hal-hal tersebut tidak dapat diganggu. Jika membutuhkan suhu panas, maka MC78XX/LM78XX/MC78XXA dapat mengirim arus keluaran sebesar 1A. Meskipun didesain sebagai regulator tegangan yang *fix*, alat ini dapat ditambah dengan komponen eksternal untuk mendapatkan tegangan yang sesuai dan hal-hal yang dibutuhkan lainnya seperti pada Gambar 2.12.

Fitur-fitur yang disediakan LM7805:

- Keluaran hingga 1A
- Keluaran tegangan dari 5, 6, 8, 9, 10, 12, 15, 18, 24V
- *Thermal Overload Protection*
- *Short Circuit Protection*
- *Output Transistor Safe Operating Area Protection*

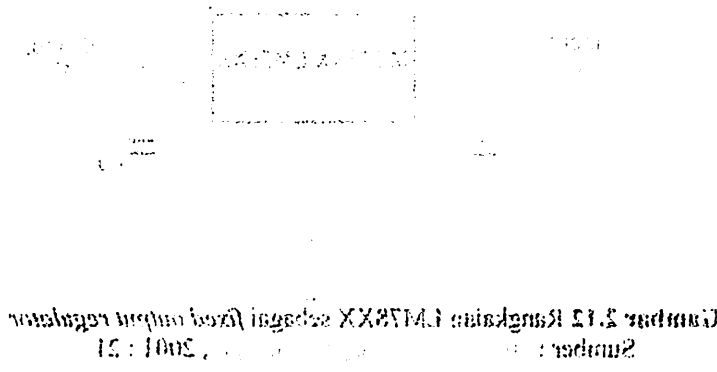


Gambar 2.12 Rangkaian LM78XX sebagai *fixed output regulator*
 Sumber : <http://www.fairchildsemi.com>, 2001 : 21

Unitnya yang meliputi pemutus tenaga dan safe operating area protection dan half-bridge tersebut tidak dapat digantikan jika membutuhkan suhu panas, maka MC78XXLM78XXVMC78XX dapat mengganti arus keluaran sebesar 1A. Mekanisme didesain sebagai regulator tegangan yang V_{in} alat ini dapat ditambahi dengan komponen eksternal untuk mendapatkan tegangan yang sesuai dan half-bridge yang dibutuhkan lainnya seperti pada Gambar 2.13.

Fitur-fitur yang disediakan LM7802:

- Keluaran hingga 1A
- Keluaran tegangan dari 2,5V, 8V, 10V, 15V, 18V, 24V
- Thermal Overload Protection
- Short Current Protection
- Output Transistor Safe Operating Area Protection



BAB III

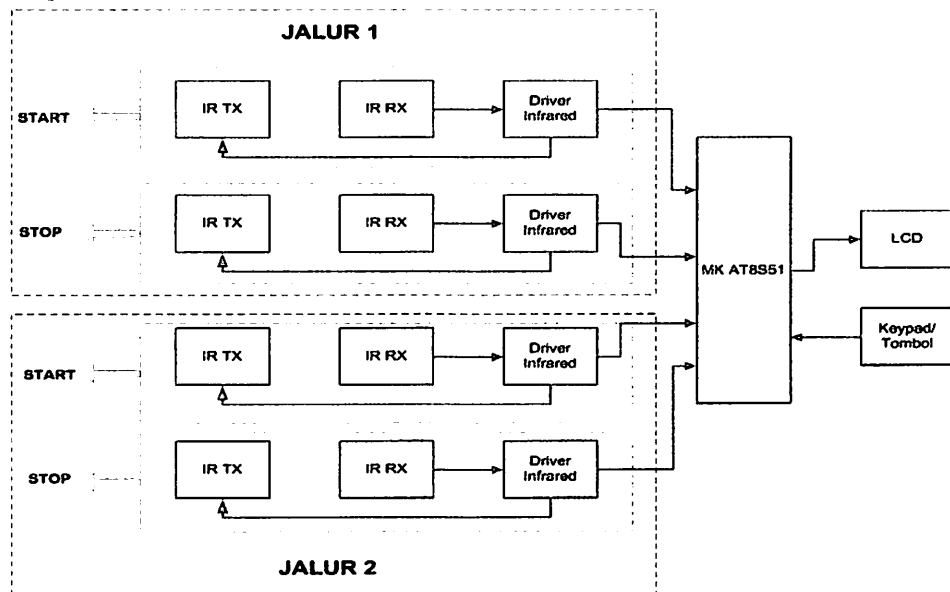
PERANCANGAN DAN PEMBUATAN ALAT

3.1. Blok Diagram dan Prinsip Kerja

Dalam membuat suatu alat penghitung waktu tempuh ini, hendaknya terlebih dahulu dibuat perancangan. Fungsi dibuatnya perancangan adalah supaya alat yang akan dibuat sesuai dengan dasar tujuan dan manfaat untuk membuat alat penghitung waktu tempuh ini. Dalam penelitian ini perancangan tersebut meliputi perancangan blok diagram dan prinsip kerja.

Setelah membuat blok diagram dan prinsip kerja, maka dapat diketahui komponen-komponen yang dibutuhkan untuk mendukung pembuatan alat ini dan program untuk mengontrol alat tersebut.

Blok diagram dari alat penghitung waktu tempuh dan kecepatan ini seperti ditunjukkan pada Gambar 3.1:



Gambar 3.1 Blok Diagram Alat Penghitung Waktu dan Kecepatan

III. HASIL

PERANCANGAN DAN PEMBAHASAN

3.1. Blok Diagram dan Prinsip Kerja

Salah satu tujuan utama dari penelitian ini adalah untuk mengetahui bagaimana proses pengolahan data yang dilakukan oleh sistem. Untuk mengetahui proses pengolahan data yang dilakukan oleh sistem, maka akan dibuat diagram alir yang menunjukkan urutan kerja sistem. Diagram alir ini akan menunjukkan urutan kerja sistem yang akan dilakukan oleh sistem. Diagram alir ini akan menunjukkan urutan kerja sistem yang akan dilakukan oleh sistem.

Salah satu blok diagram dan prinsip kerja yang akan dilakukan oleh sistem adalah untuk mengetahui bagaimana proses pengolahan data yang dilakukan oleh sistem. Diagram alir ini akan menunjukkan urutan kerja sistem yang akan dilakukan oleh sistem.

Blok diagram dan prinsip kerja yang akan dilakukan oleh sistem adalah untuk mengetahui bagaimana proses pengolahan data yang dilakukan oleh sistem.

3.2. Pembahasan

Penjelasan dari blok diagram di atas adalah:

1. *Infrared* (terdiri dari *infrared transmitter*/IR TX dan *infrared receiver*/IR RX) dipasang pada masing-masing jalur dan tiap garis *start* dan garis *finish*.
2. *Driver infrared* berfungsi supaya data yang di *transmisi* kan melalui *infrared* tidak terpengaruh oleh cahaya apapun.
3. Data dari rangkaian *infrared* dikirim ke mikrokontroler untuk diproses.
4. *Output* dari mikrokontroler ditampilkan pada LCD (*Liquid Crystal Digital*).
5. Keypad digunakan untuk meng-*clear* LCD atau melihat isi data yang tersimpan di RAM.

Prinsip kerja alat penghitung waktu tempuh dan kecepatan ini adalah pada saat perlombaan ini dimulai. Dimulainya perlombaan *drag race* ini ditandai dengan menyalanya lampu hijau. Jika lampu yang menyala adalah merah maka perlombaan *drag race* belum dimulai. Ketika perlombaan belum dimulai dan salah satu peserta lomba melewati *infrared* yang ada pada garis *start* maka *infrared* akan memberikan data berupa logika 1 dan diproses di mikrokontroler kemudian menampilkannya dalam bentuk pesan pada LCD.

Jika peserta tidak ada yang melakukan pelanggaran, maka perhitungan waktu dihitung pada saat para peserta melewati *infrared* pada garis *start*. Perhitungan waktu berhenti ketika masing-masing peserta melewati *infrared* pada garis *finish*. Besar nilai kecepatan dari dua peserta lomba dihitung berdasarkan pembagian jarak lintasan (2.01 meter) dengan waktu tempuh. Setelah diketahui besar kecepatan yang diperoleh dari masing-masing peserta lomba, maka dapat diketahui pemenang dari lomba *drag race* tersebut.

Penelitian dari blok diagram di atas adalah:

1. *Hydrex* terdiri dari *Hydrex Transmitter* (TX dan *Hydrex Receiver* (RX)) dipasang pada masing-masing jalur dan tiap garis awal dan garis akhir.
2. *Hydrex* *Hydrex* berfungsi sebagai data yang di transmit kan melalui *Hydrex* tidak terpengaruh oleh cahaya apapun.
3. Data dari rangkaian *Hydrex* dikirim ke mikrokontroler untuk diproses.
4. *Hydrex* dan mikrokontroler ditambhkan pada LCD (*Liquid Crystal Display*).
5. Keyboard digunakan untuk meng-*view* LCD akan terlihat isi data yang disimpan di RAM.

Prinsip kerja alat penghitung waktu tempuh dan kecepatan ini adalah pada saat pertandingan ini dimulai. Dimulainya pertandingan awal akan ini ditandai dengan menyalaunya lampu hijau. Jika lampu yang menyala adalah merah maka pertandingan awal akan belum dimulai. Ketika pertandingan belum dimulai dan salah satu peserta lomba melewati *Hydrex* yang ada pada garis awal maka *Hydrex* akan memberikan data berupa logika 1 dan diproses di mikrokontroler kemudian menyimpannya dalam bentuk memori pada LCD.

Jika peserta tidak ada yang melakukan pelanggaran maka perhitungan waktu dihitung pada saat para peserta melewati *Hydrex* pada garis awal. Perhitungan waktu berhenti ketika masing-masing peserta melewati *Hydrex* pada garis akhir. Jika nilai kecepatan dari dua peserta lomba dihitung berdasarkan pembagian jarak lintasan (50 meter) dengan waktu tempuh. Setelah diketahui hasil kecepatan yang diperoleh dari masing-masing peserta lomba maka dapat diketahui pemenang dari lomba yang diadakan.

3.2. Perancangan Perangkat Keras (*Hardware*)

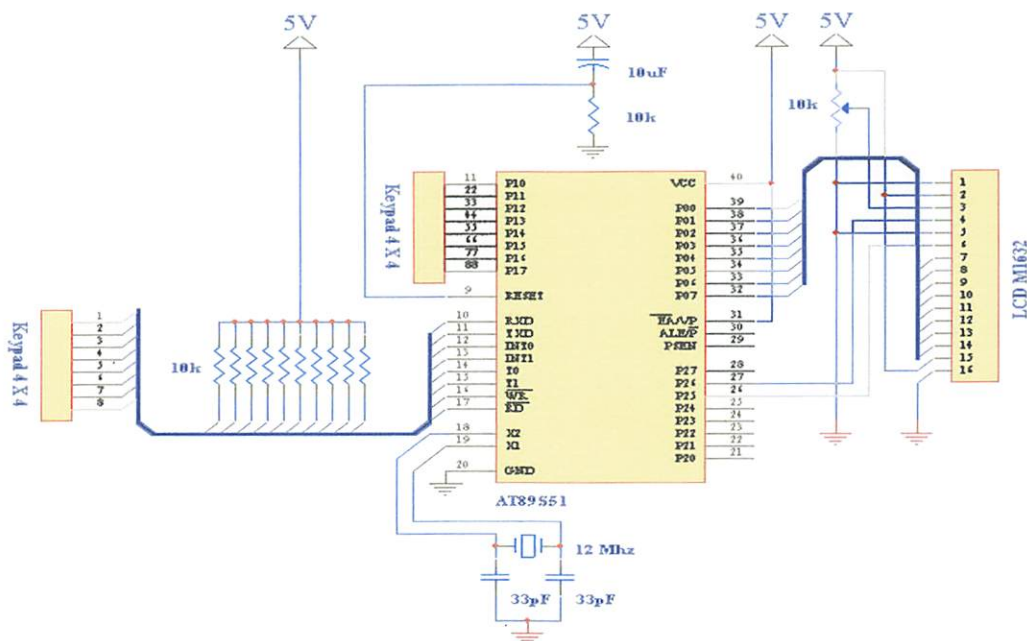
Untuk perancangan perangkat keras, komponen atau rangkaian yang dibutuhkan untuk membuat alat penghitung waktu tempuh dan kecepatan ini adalah rangkaian mikrokontroler, rangkaian sensor inframerah, rangkaian *driver* inframerah, rangkaian regulator, rangkaian *keypad* dan rangkaian LCD.

3.2.1. Perancangan Sistem Berbasis Mikrokontroler AT89S51

Fungsi mikrokontroler dalam perancangan alat penghitung waktu tempuh dan kecepatan adalah sebagai komponen utama untuk melakukan perhitungan yang dilakukan.

Rangkaian minimum dari mikrokontroler ini terdiri dari 3 buah kapasitor, satu buah IC mikrokontroler, satu buah resistor dan satu buah kristal. Dua buah kapasitor dihubungkan oleh pin X1 dan X2 yang masing-masing sebesar 33pF dan satu buah kristal sebesar 12Mhz yang disebut sebagai rangkaian osilator. Satu buah kapasitor sebesar 10μF dan satu buah resistor sebesar 10k dihubungkan dengan pin *RESET*. IC mikrokontroler digunakan sebagai sistem kontrol alat penghitung waktu tempuh dan kecepatan ini. Masukan dari *infrared* dan *keypad* dihubungkan ke IC mikrokontroler yang nantinya akan diproses.

Port-port yang digunakan dalam membuat alat ini, yaitu: port 3.0 sebagai masukan dari *infrared*, port 1.0 – port 1.7 sebagai masukan dari *keypad*, port 0.0 – port 0.7 sebagai *output* ke LCD, port 2.5 dan port 2.6 dihubungkan ke pin 6 dan pin 5 dari LCD sebagai E (*enable*) dan RS (*reset*) pada LCD. Rangkaian mikrokontroler pada alat penghitung waktu tempuh dan kecepatan otomatis ini dapat dilihat pada Gambar 3.2.



Gambar 3.2 Rangkaian Mikrokontroler AT89S51

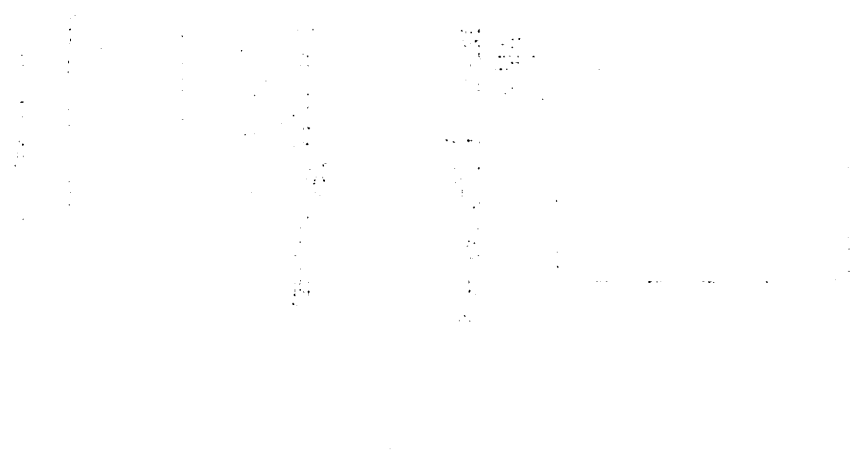
3.2.1.1. Pengaturan *Timer*

Untuk mengatur kerja *Timer/Counter* tersebut digunakan dua register tambahan yang dipakai bersama *Timer 0* dan *Timer 1*. Cara kerja dari register *Timer/Counter* terlihat pada Gambar 3.3. Register tersebut adalah TCON dan TMOD. Untuk mengaktifkan *Timer*, atur susunan bit pada TCON dan TMOD. Pada TCON yang perlu di *set* adalah:

- Bit TFx = 1 jika pencacah biner yang terhubung mengalami *overflow*. Untuk meng-nolkan TFx, maka harus diberi instruksi CLR TFx.
- Bit TRx = 0 pencacah biner berhenti melakukan pencacahan. Bila bit gate pada register TMOD = 1, maka saluran pulsa diatur bersama TRx dan sinyal pada kaki INT0 dan INT1.

Bit yang perlu di *set* untuk register TMOD adalah:

- Bit M0/M1 digunakan untuk memilih mode *Timer*.



Gambar 3.2. Blok diagram AT91SAM7A1

3.2.1.1. Penggunaan Timer

Untuk mengkonfigurasi timer counter tersebut digunakan dua register konfigurasi yang diberikan bernama `TIMER_0` dan `TIMER_1`. Cara kerja dari register `TIMER_COUNTER` terlihat pada Gambar 3.2. Register tersebut adalah `TCR` dan `TMOD`. Untuk mengkonfigurasi timer akan ada dua `TCR` dan `TMOD`. Pada

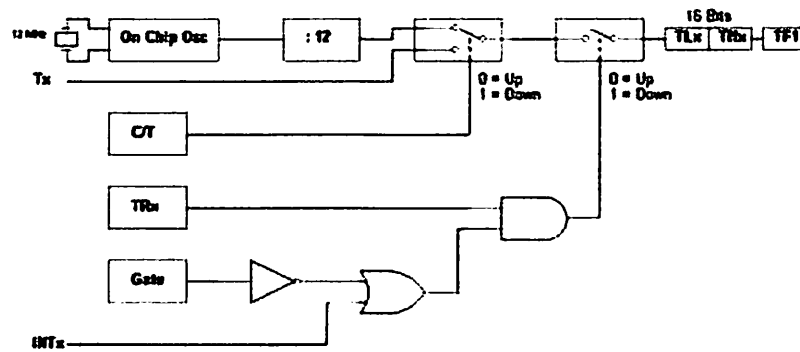
`TCR` yang perlu di set adalah:

- Bit `TRZ = 1` jika penanda timer yang terhubung dengan `TCR` untuk mengkonfigurasi `TRZ` maka harus diberi instruksi `CLR TRZ`.
- Bit `TRZ = 0` penanda timer berhenti melakukan penandaan. Bila bit `TRZ` pada register `TMOD = 1` maka seluruh pulsa dari `TRZ` dan sinyal pada kaki `INT0` dan `INT1`.

Bit yang perlu di set untuk register `TMOD` adalah:

- Bit `MMIO` digunakan untuk memilih mode timer.

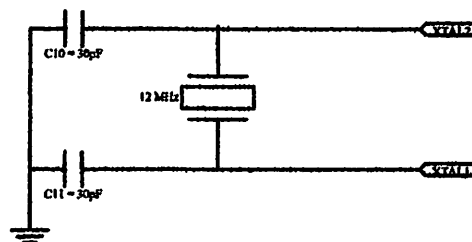
- Bit $C/T = 0$ maka sinyal detak diperoleh dari osilator kristal yang frekuensinya sudah dibagi 12. $C/T = 1$ maka sinyal detak diperoleh dari kaki Tx.
- Bit $gate = 0$ saluran sinyal detak hanya diatur oleh TRx. Bila $gate = 1$, kaki INTx yang dipakai untuk mengatur saluran sinyal detak.



Gambar 3.3 Cara Kerja Timer

3.2.1.2. Rangkaian Osilator

Rangkaian osilator kristal yang dipergunakan adalah seperti pada Gambar 3.4.



Gambar 3.4 Rangkaian Osilator Kristal

Rangkaian ini berfungsi sebagai sumber detak sinyal kepada AT89S51. Kristal yang terpasang menggunakan frekuensi 12MHz, sementara nilai kapasitansi C10 dan C11 sebesar 30pF, yang sesuai dengan ketentuan ATMEL.

o Bit CNT = 0 maka sinyal detak diproses dan osilator kristal yang frekuensinya sudah dibagi 12. CNT = 1 maka sinyal detak diproses dan kaki TX.

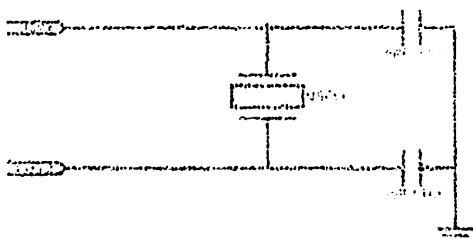
o Bit gate = 0 saluran sinyal detak hanya dikirim oleh TRX. Jika gate = 1, kaki INTX yang dipakai untuk mengirim saluran sinyal detak.

Gambar 3.3 Cara Kerja Tower

3.2.1.2. Rangkaian Osilator

Rangkaian osilator kristal yang dipergunakan adalah seperti

pada Gambar 3.4.



Gambar 3.4 Rangkaian Osilator Kristal

Rangkaian ini berfungsi sebagai sumber detak sinyal kepada AT89C51.

Kristal yang terpasang menggunakan frekuensi 12MHz, sementara nilai kapasitansi

C10 dan C11 sebesar 30pF, yang sesuai dengan ketentuan ATME1.

3.2.1.3. Rangkaian Reset

Untuk me-reset mikrokontroler AT89S51, maka pin RST diberikan logika tinggi selama sekurang-kurangnya dua siklus mesin (24 periode osilator). Untuk membangkitkan sinyal *reset*, kapasitor dihubungkan dengan Vcc dan sebuah resistor yang dihubungkan ke *ground*.

Karena kristal yang digunakan mempunyai frekuensi sebesar 11,0592MHz, maka satu periode dapat dihitung dengan persamaan:

$$T = \frac{1}{f_{XTAL}} = \frac{1}{11,0592MHz} s = 9,042 \times 10^{-8} s$$

Sehingga waktu minimal logika tinggi yang dibutuhkan untuk me-reset mikrokontroler dapat dihitung dengan persamaan:

$$\begin{aligned} t_{reset(min)} &= T \times \text{periode yang dibutuhkan} \\ &= 9,042 \times 10^{-8} \times 24 \\ &= 2,17 \mu s \end{aligned}$$

Jadi mikrokontroler membutuhkan waktu minimal 2,17 μs untuk me-reset. Waktu minimal inilah yang dijadikan pedoman untuk menentukan nilai R dan C. Dapat ditentukan nilai R = 8,2k Ω dan C = 10 μF dengan persamaan:

$$t = 0,357 \times R \times C = 0,357 \times 8200\Omega \times 10 \times 10^{-6} = 29,274ms$$

Dengan nilai komponen R = 8,2k Ω dan C = 10 μF maka hal ini dapat memenuhi syarat minimal untuk waktu yang dibutuhkan oleh mikrokontroler.

3.2.1.3. Rangkaian Reser

Untuk mem-reset mikrokontroler AT89C21, maka pin RST diberikan logika tinggi selama selang-kurangnya dua siklus mesin (24 periode osilator). Untuk membangkitkan sinyal reset, kapasitor dihubungkan dengan Vcc dan sebuah resistor yang dihubungkan ke ground.

Karena kristal yang digunakan mempunyai frekuensi sebesar 11,059374MHz, maka satu periode dapat dihitung dengan persamaan:

$$T = \frac{1}{f_{\text{osc}}} = \frac{1}{11,059374\text{MHz}} = 9,042 \times 10^{-8} \text{ s}$$

Sehingga waktu minimal logika tinggi yang dibutuhkan untuk mem-reset mikrokontroler dapat dihitung dengan persamaan:

$$t_{\text{reset}} = T \times \text{periode yang dibutuhkan}$$

$$= 9,042 \times 10^{-8} \times 24$$

$$= 2,17 \text{ ns}$$

Jadi mikrokontroler membutuhkan waktu minimal 2,17 ns untuk mem-reset. Waktu minimal inilah yang dijadikan pedoman untuk menentukan nilai R dan C. Dapat ditentukan nilai R = 8,2k Ω dan C = 10pF dengan persamaan:

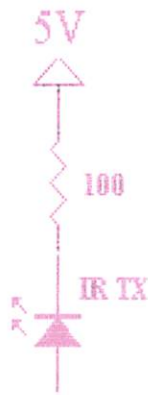
$$t = 0,327 \times R \times C = 0,327 \times 8200 \times 10 \times 10^{-6} = 26,734\text{ms}$$

Dengan nilai komponen R = 8,2k Ω dan C = 10pF, maka hal ini dapat memenuhi syarat minimal untuk waktu yang dibutuhkan oleh mikrokontroler.

3.2.2. Rangkaian *Infrared*

3.2.2.1. Rangkaian Pemancar (*Transmitter*)

Rangkaian pemancar berfungsi untuk memancarkan sinar *infrared* dengan bantuan LED yang memancarkan *infrared* (IRED), yang nantinya diterima oleh rangkaian penerima *infrared*. Gambar 3.5 menunjukkan rangkaian pemancar *infrared*.



Gambar 3.5 Rangkaian Pemancar *Infrared*

Mengacu pada Gambar rangkaian di atas, agar dioda inframerah dapat memancarkan sinar inframerah diperlukan arus sebesar 20 mA dan tegangan (V_{IR}) sebesar 1,2 Volt.

Maka dapat dihitung besarnya R_s sebagai berikut :

$$R_s = \frac{V_{cc} - V_{IR}}{I}$$

$$R_s = \frac{5 - 1,2}{20 \times 10^{-3}}$$

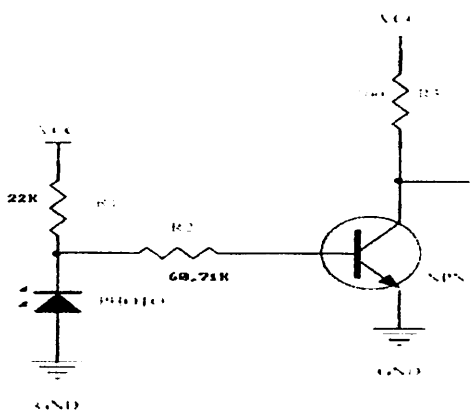
$$R_s = \frac{3,8}{20 \times 10^{-3}}$$

$R_s = 190\ \Omega \cong 220\Omega$

Jadi resistor yang terpasang pada rangkaian pemancar adalah 220 Ω .

3.2.2.2. Rangkaian Penerima (Receiver)

Rangkaian penerima berfungsi untuk menerima sinyal *infrared* dari pemancar *infrared*, sinyal *infrared* diterima oleh fotodioda dan digunakan untuk membias transistor yang difungsikan sebagai saklar (*switching*). Output dari rangkaian ini berupa tegangan. Gambar 3.6 menunjukkan rangkaian penerima *infrared*.



Gambar 3.6 Rangkaian Penerima *Infrared*

Karena transistor dioperasikan untuk saklar (*switching*) maka dioperasikan pada dua titik kerja, yaitu : pada titik saturasi atau pada titik sumbat (*cut off*). Jadi perhitungan nilai resistor yang terpasang pada rangkaian penerima sinyal *infrared* adalah sebagai berikut:

- **Kondisi Pertama, pada saat IR LED tidak terhalang benda**
Pada saat IR LED RX tidak terhalang dilakukan pengukuran untuk melihat arus. Arus itu memiliki nilai $I_{R1}=0,12\text{mA}$, maka menurut persamaan :

$$V_{CC} = V_{fd} + I_{R1}R_1$$

Untuk rangkaian ini didesain V_{fd} adalah 2,4V

$$5 = 2,4 + I_{R1}R_1$$

Kemudian sesuai dengan persamaan:

$$R_1 = \frac{V_{CC} - V_{fd}}{I_{R1}}$$

$$R_1 = \frac{5 - 2,4}{0,12mA}$$

$$R_1 = 21666\Omega \cong 22K\Omega$$

Ditentukan besar $R_3 = 100 \Omega$ dan $V_{CE} = 2,7$. Dengan diketahuinya $R_3 = R_C$, maka nilai I_C adalah:

$$I_C.R_C + V_{CE} - V_{CC} = 0$$

$$I_C = \frac{V_{CC} - V_{CE}}{R_C}$$

$$I_C = \frac{5 - 2,7}{100}$$

$$I_C = 23 \times 10^{-3} A$$

Dengan hfe minimum 60 maka dalam perancangan dapat digunakan hfe 100 agar transistor bekerja optimal, maka besar arus basis:

$$I_B = \frac{I_C}{hfe}$$

$$I_B = \frac{23 \times 10^{-3} A}{60}$$

$$= 0,383mA$$

$$V_{CE} = V_{CC} + I_{C1}R_1$$

Untuk mengkasim ini diberikan V_{CE} adalah 2,4V

$$2 = 2,4 + I_{C1}R_1$$

Kemudian sesuai dengan persamaan:

$$R_1 = \frac{V_{CE} - V_{CC}}{I_{C1}}$$

$$R_1 = \frac{2 - 2,4}{0,12mA}$$

$$R_1 = 3166\Omega \approx 32K\Omega$$

Ditentukan besar $R_2 = 100\Omega$ dan $V_{CE} = 2,7$ Dengan dikatakannya $R_1 = R_2$ maka

nilai I_C adalah:

$$I_C R_C + V_{CE} - V_{CC} = 0$$

$$I_C = \frac{V_{CC} - V_{CE}}{R_C}$$

$$I_C = \frac{2 - 2,7}{100}$$

$$I_C = 2310^{-4}A$$

Dengan I_C minimum 60 maka dalam perhitungan dapat digunakan I_C 100

agar transistor bekerja optimal maka besar arus basis:

$$I_B = \frac{I_C}{\beta_{DC}}$$

$$I_B = \frac{2310^{-4}}{60}$$

$$= 0,382mA$$

Kemudian mencari nilai $R_2=R_B$ yaitu dengan persamaan :

$$I_B = \frac{V_{BB} - V_{BE}}{R_B}$$

$$V_{BB} = V_{fd}$$

$$V_{fd} = I_B R_2 + V_{BE}$$

$$I_B R_2 = V_{fd} - V_{BE}$$

$$R_2 = \frac{V_{fd} - V_{BE}}{I_B}$$

$$R_2 = \frac{2,4 - 0,7}{0,383mA}$$

$$R_2 = 4,43K\Omega$$

- **Kondisi kedua , pada saat IR LED terhalang benda**

Sesuai dengan persamaan di atas, maka:

$$I_B = \frac{V_{BB} - V_{BE}}{R_B}$$

$$V_{CC} = V_{BB}, R_B = R_1 + R_2$$

$$I_B = \frac{V_{CC} - V_{BE}}{R_B}$$

$$V_{CC} = I_B R_B + V_{BE}$$

$$V_{CC} = I R_1 + I R_2 + V_{BE}$$

$$V_{CC} = I R_1 + I R_2 + V_{BE}$$

$$V_{CC} = I(R_1 + R_2) + V_{BE}$$

$$V_{CC} = I(21,6K\Omega + 4,43K\Omega) + V_{BE}$$

Kemudian mencari nilai R_2 dari persamaan :

$$I_B = \frac{I_{BB} - I_{BE}}{R_B}$$

$$V_{BE} = V_{CE}$$

$$V_{CE} = I_B R_2 + V_{BE}$$

$$I_B R_2 = V_{CE} - V_{BE}$$

$$R_2 = \frac{V_{CE} - V_{BE}}{I_B}$$

$$R_2 = \frac{3,4 - 0,7}{0,78mA}$$

$$R_2 = 4,43K\Omega$$

• Kemudian kedua , pada saat IR LED terbalik benda

Sesuai dengan persamaan di atas maka:

$$I_B = \frac{I_{BB} - I_{BE}}{R_B}$$

$$V_{CE} = V_{BE} , R_B = R_1 + R_2$$

$$I_B = \frac{I_{CC} - V_{BE}}{R_B}$$

$$V_{CE} = I_B R_B + V_{BE}$$

$$V_{CE} = I_B (R_1 + R_2) + V_{BE}$$

$$V_{CE} = I_B (R_1 + R_2) + V_{BE}$$

$$V_{CE} = I_B (R_1 + R_2) + V_{BE}$$

$$V_{CE} = I_B (21,6K\Omega + 4,43K\Omega) + V_{BE}$$

$$I = I_B = \frac{V_{CC} - V_{BE}}{(21,6K\Omega + 4,43K\Omega)}$$

$$I = I_B = \frac{5 - 0,7}{(20,03K\Omega)}$$

$$I = I_B = 0,215mA$$

Maka didapatkan nilai I_C dengan persamaan:

$$I_C = I_B \cdot h_{fe}$$

$$I_C = 0,215mA \times 100$$

$$I_C = 21,5mA$$

Maka nilai V_{CE} (nilai masukan ke mikrokontroler) menurut persamaan adalah:

$$I_C \cdot R_C + V_{CE} - V_{CC} = 0$$

$$R_C = R_3$$

$$V_{CC} = I_C R_3 + V_{CE}$$

$$V_{CE} = V_{CC} - I_C \cdot R_3$$

$$V_{CE} = 5 - (21,5 \times 10^{-3} A \times 100\Omega)$$

$$V_{CE} = 5 - 2,15V$$

Rangkaian *infrared* yang digunakan untuk membuat alat penghitung waktu tempuh dan kecepatan, terdiri dari *infrared transmitter* (IR TX) dan *infrared receiver* (IR RX), rangkaian *comparator* dan rangkaian LM567 (*tone decoder*) seperti pada Gambar 3.7. Cahaya yang diterima oleh IR TX akan dipancarkan kembali ke IR RX dalam bentuk cahaya.

$$1 = \lambda_5 = \frac{10^{-1} - 10^{-2}}{(21,6 \times 10^{-3} + 4,4 \times 10^{-3})}$$

$$1 = \lambda_6 = \frac{2 - 0,7}{(20,0 \times 10^{-3})}$$

$$1 = \lambda_7 = 0,212 \text{ ms}$$

Maka diperoleh nilai λ_i dengan persamaan:

$$\lambda_1 = 1,9 \text{ ms}$$

$$\lambda_2 = 0,212 \text{ ms} \times 100$$

$$\lambda_3 = 21,2 \text{ ms}$$

Maka nilai K_{FB} (nilai masukan ke mikrokontroler) menurut persamaan adalah:

$$K_{FB} R_{FB} + V_{FB} \cdot V_{FB} = 0$$

$$K_{FB} = K_{FB}$$

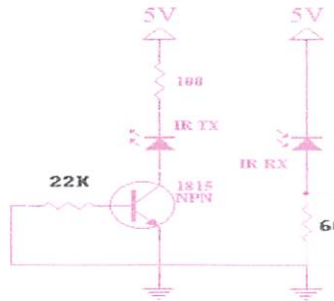
$$K_{FB} = K_{FB} + K_{FB}$$

$$K_{FB} = K_{FB} - K_{FB}$$

$$K_{FB} = 2 - (21,2 \times 10^{-3} \times 100000)$$

$$K_{FB} = 2 - 2120$$

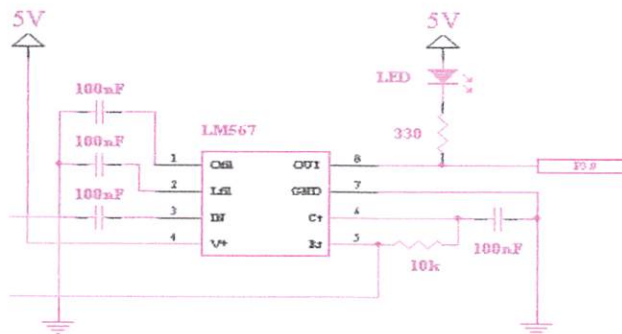
Rangkaian infrared yang digunakan untuk membuat alat penghitung waktu terputih dan kesepatan, terdiri dari infrared transmitter (IR TX) dan infrared receiver (IR RX), rangkaian comparator dan rangkaian LM567 (voice decoder) seperti pada Gambar 3.1. Caraaya yang diterima oleh IR TX akan dipancarkan kembali ke IR RX dalam bentuk cahaya.



Gambar 3.7 Rangkaian *Infrared*

3.2.3 Rangkaian LM567 (*Tone Decoder*)

Rangkaian ini berfungsi untuk mengubah energi cahaya menjadi frekuensi. Data yang diterima adalah dalam bentuk cahaya yang kemudian diubah menjadi frekuensi oleh LM567 (*tone decoder*). Cahaya diubah dalam bentuk frekuensi supaya pada saat pengiriman data dari *infrared*, data yang diterima tidak dipengaruhi oleh cahaya apapun (*driver infrared*). Rangkaian *tone decoder* yang digunakan terlihat pada Gambar 3.8.



Gambar 3.8 *Tone Decoder*

Alasan pemakaian LM567 pada rangkaian sensor antara lain :

- *Drag race* dalam perlombaan kondisinya selalu diluar ruangan atau tempat terbuka sehingga cuaca dalam perlombaan tidak menentu.
- Dibuatkan *driver* yang tidak terpengaruh terhadap cahaya.
- Photodiode yang dipakai berbasis *frekwensi*.

Frekuensi pusat dari *tone decoder* adalah sama dengan frekuensi pada VCO, yaitu:

$$f_o \cong \frac{1}{1,1.R_1.C_1} = \frac{1}{1,1.10k\Omega.0,1\mu F} = 1kHz$$

Ukuran *bandwidth* dapat dihitung dengan:

$$BW = 1070 \sqrt{\frac{V_i}{f_o.C_2}} \% \text{ dari } f_o$$

Dimana:

V_i = tegangan *input* (volts rms), $V_i \leq 200$ mV

C_2 = kapasitor pada pin 2 (μF)

Data *input* yang masuk melalui pin 3 kemudian dibandingkan dengan frekuensi pusat *tone decoder* ($f_o=1kHz$). Setelah dibandingkan dengan f_o , jika data *inputan* sama dengan f_o maka data dikuatkan oleh *transistor* NPN 1815. Setelah dikuatkan, data dikirim ke IR TX kemudian mengirimkannya kembali ke IR RX dan begitu seterusnya hingga data yang diperoleh tidak sama dengan f_o . Jika data *inputan* tidak sama dengan f_o , maka akan menghasilkan *output* melalui pin 8 dan dihubungkan dengan port 3.0 dari mikrokontroler. *Tone decoder* bersifat aktif rendah.

3.2.4. Rangkaian *Keypad*

Input dari *keypad* berfungsi untuk meng-clear LCD atau untuk melihat isi dari *record* atau data waktu dan kecepatan. Port yang digunakan untuk menghubungkan *keypad* dengan mikrokontroler adalah port 1.0 – port 1.7 seperti pada Gambar 3.9.

Responansi pusat dari tone oscillator adalah sama dengan Responansi pada 1000

misal:

$$X_c = \frac{1}{11.8 \times 10^3 \times 11.1047201 \mu F} = 1642$$

Ukuran Responansi dapat dihitung dengan:

$$BW = 1000 \times \frac{1}{Q} \text{ dan } Q = \frac{f}{\Delta f}$$

Dimana:

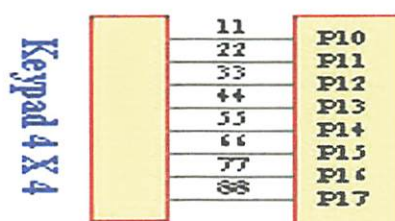
Δf = lebar pita (Hz) $\Delta f = 200 \text{ mV}$

Q = responansi pada pin 2 (Hz)

Data yang masuk melalui pin 3 kemudian dibandingkan dengan Responansi pusat tone oscillator ($f=1KHz$). Setelah dibandingkan dengan f_c jika data nyaman sama dengan f_c maka data diberikan oleh Responansi pada 1000. Setelah diberikan, data dikirim ke IR TX kemudian menginformasikan kembali ke IR RX dan bagian selanjutnya hingga data yang diberikan tidak sama dengan f_c jika data nyaman tidak sama dengan f_c maka akan mengaktifkan output melalui pin 2 dan dihubungkan dengan port 2.0 dari mikrokontroler. Tone oscillator tersebut aktif sendiri.

3.3.4. Keunggulan Kelemahan

Kelebihan dari keypad berbasis mikrokontroler LCD atau untuk melihat isi data secara real time dan kegunaan lain yang digunakan untuk menghubungkan keypad dengan mikrokontroler adalah port I/O – port I/O dapat dihubungkan dengan 2.5.



Gambar 3.9 Rangkaian Keypad

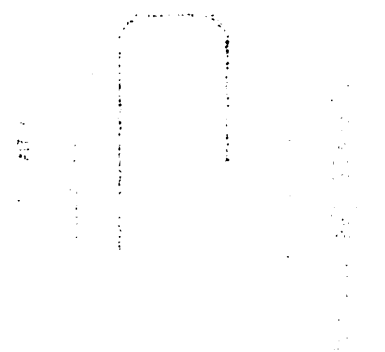
3.2.5. Rangkaian LCD (*Liquid Crystal Display*)



Gambar 3.9 Hubungan Konsentrasi

3.3.5. Karakteristik LCR (Liquid Crystal Display)

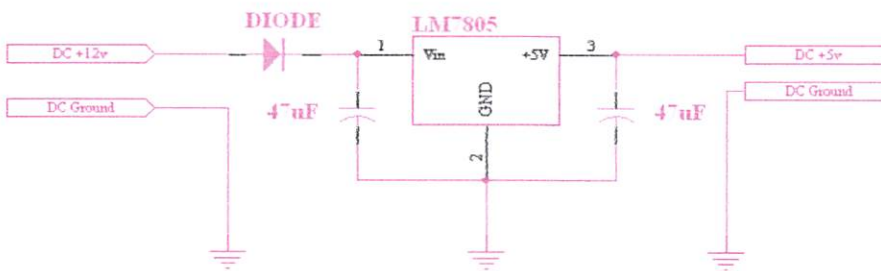
Dalam penelitian ini penelitian waktu respon dan kestabilan pada perbedaan voltase LCR (Liquid Crystal Display) bertujuan untuk mengetahui waktu dari mikrokontroler yang diberikan perintah dengan kestabilan dan waktu yang dibutuhkan masing-masing peserta lomba. LCR memiliki 16 pin yang digunakan untuk mengendalikannya dengan mikrokontroler. Karakteristik yang LCR memiliki akan memberikan data melalui pin 7-14 yang dihubungkan ke port 0.5 – port 0.7 dan RS (pin 4) dihubungkan ke port 2.0. Komandasi E (pin 6) yang merupakan sinyal aktif rendah dihubungkan ke port 2.2. Perancangan LCR dihubungkan pada Gambar 3.10.



Gambar 3.10 Perancangan LCR 1601

3.2.6. Rangkaian Regulator

Rangkaian ini berfungsi sebagai penyeimbang tegangan. Berapapun besar sumber tegangan yang masuk, akan diseimbangkan menjadi 5V. Rangkaian ini tersusun dari satu buah diode, LM7805 dan dua buah kapasitor (yang masing-masing bernilai sebesar $47\mu\text{F}$) seperti pada Gambar 3.11.

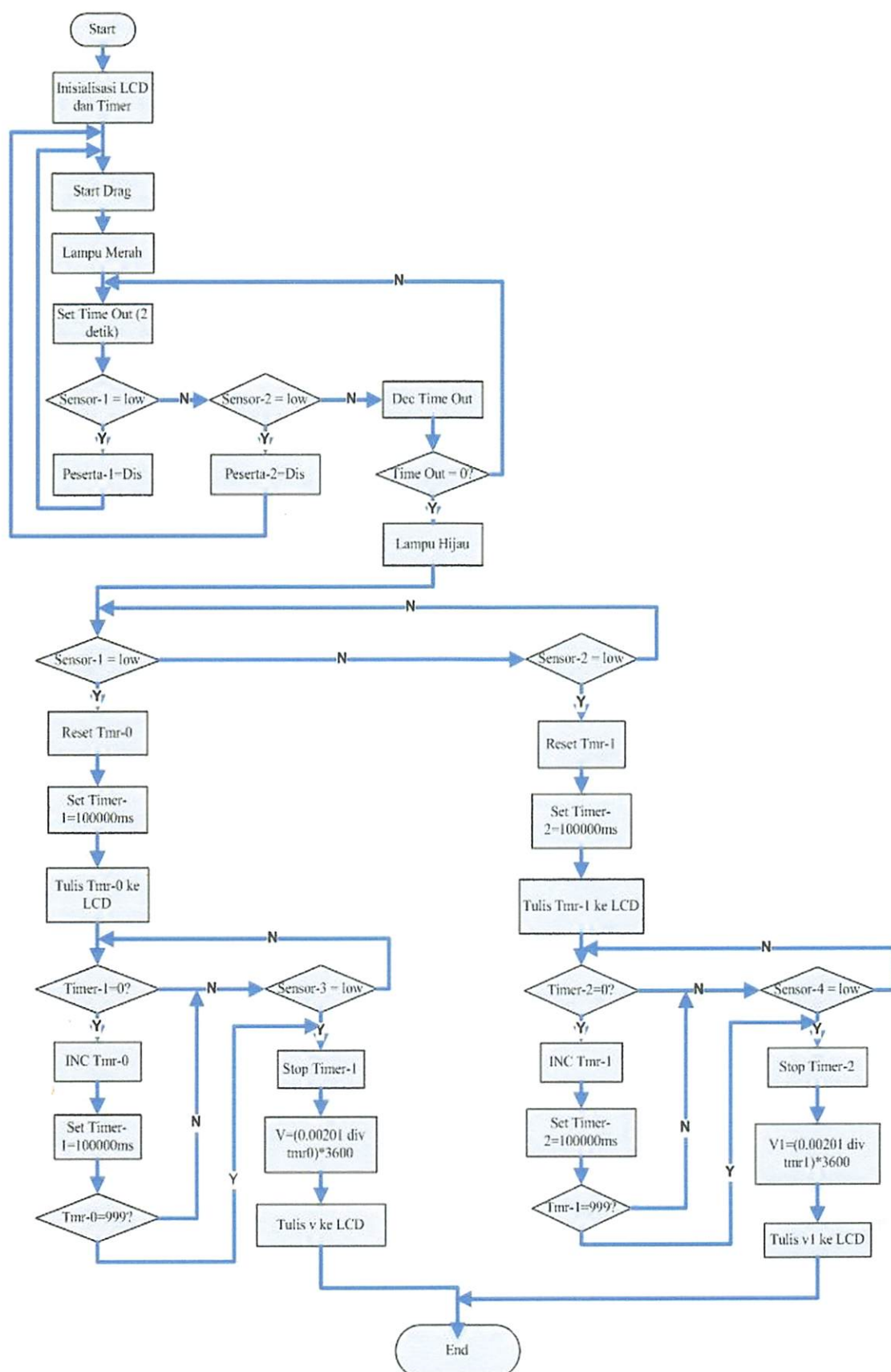


Gambar 3.11 Rangkaian Regulator

Diode berfungsi menyalurkan arus secara searah. Kemudian tegangan yang masuk dikenali sebagai V_{in} . V_{in} yang masuk akan distabilkan oleh kapasitor-kapasitor yang ada. Setelah distabilkan maka keluaran tegangan yang dihasilkan sebesar +5V.

3.3. Perancangan Perangkat Lunak (Software)

Perancangan perangkat lunak (*software*) menjelaskan bagaimana merancang program untuk menjalankan alat penghitung waktu tempuh dan kecepatan ini. Perancangan perangkat lunak yang digunakan berupa *flowchart* seperti yang ada pada Gambar 3.12.



Gambar 3.12 Flowchart Cara Kerja Alat

Penjelasan dari *flowchart* di atas adalah:

1. Alat diberikan sumber tegangan.
2. Inisialisasi LCD dan *Timer*.
3. Perlombaan dimulai.
4. Lampu merah menyala dengan waktu tunda selama dua detik kemudian lampu hijau menyala.
5. Selama waktu tunda (*delay*), akan dilakukan pengecekan pada masing-masing sensor *start* untuk mengetahui peserta yang melakukan pencurian *start*. Jika sensor satu pada jalur satu sama dengan nol, maka peserta pada jalur satu melakukan pencurian *start* dengan menampilkan pesan diskualifikasi pada LCD. Jika sensor satu tidak sama dengan nol maka dilakukan pengecekan terhadap sensor 2. Jika sensor dua pada jalur dua sama dengan nol maka pesan akan muncul pada LCD untuk peserta dua. Jika sensor tidak sama dengan nol, maka *time out* dikurangi satu. Jika *time out* sama dengan nol maka akan melanjutkan aba-aba perlombaan, yaitu menunggu menyala lampu hijau.
6. Dilakukan pengecekan pada sensor satu yang ada pada jalur satu apakah dalam kondisi nol. Jika sensor tersebut dalam kondisi nol maka *Timer* satu mulai menghitung waktu.
7. Jika sensor satu tidak dalam kondisi nol maka dilakukan pengecekan pada sensor dua yang ada pada jalur dua. Jika sensor dua dalam kondisi nol maka *Timer* dua untuk jalur dua mulai menghitung waktu.
8. Jika sensor dua tidak dalam kondisi nol maka akan dilakukan pengecekan pada sensor satu dan begitu seterusnya.

Penjelasan dari Algoritma di atas adalah:

1. Alat diberikan sumber tegangan.
2. Inisialisasi LCC dan Timer.
3. Perhitungan dimulai.
4. Langkah awal menyala dengan waktu tunda selama dua detik kemudian lampu hijau menyala.
5. Selama waktu tunda (delay) akan dilakukan pengisian pada motor-motor sensor awal untuk mengetahui benda yang melakukan pemenuhan awal. Jika sensor satu pada jalur satu sama dengan nol, maka benda pada jalur satu melakukan pemenuhan awal dengan memanfaatkan busa diskontinuasi pada LCC. Jika sensor satu tidak sama dengan nol maka dilakukan pengisian terhadap sensor 2. Jika sensor dua pada jalur dua sama dengan nol maka busa akan muncul pada LCC untuk busa dua. Jika sensor tidak sama dengan nol, maka busa dua dikurangi satu. Jika busa dua sama dengan nol maka akan melakukan aba-aba berikutnya. Jalur berikutnya menyala hijau.
6. Dilakukan pengisian pada sensor satu yang ada pada jalur satu apakah dalam kondisi nol. Jika sensor tersebut dalam kondisi nol maka Timer satu mulai menghitung waktu.
7. Jika sensor satu tidak dalam kondisi nol maka dilakukan pengisian pada sensor dua yang ada pada jalur dua. Jika sensor dua dalam kondisi nol maka Timer dua untuk jalur dua mulai menghitung waktu.
8. Jika sensor dua tidak dalam kondisi nol maka akan dilakukan pengisian pada sensor satu dan begitu seterusnya.

9. Setelah *Timer* satu mulai menghitung waktu, kemudian dilakukan pengecekan terhadap sensor dua apakah dalam kondisi nol. Jika sensor dua dalam kondisi satu maka dilakukan pengecekan terhadap sensor tiga yang ada pada garis *finish*. Jika sensor tiga dalam kondisi nol maka *Timer* satu akan berhenti menghitung waktu. Jika sensor tiga dalam kondisi satu maka dilakukan pengecekan terhadap sensor dua.
10. Setelah *Timer* dua mulai menghitung waktu, kemudian dilakukan pengecekan terhadap sensor satu apakah dalam kondisi nol. Jika sensor satu dalam kondisi satu maka dilakukan pengecekan terhadap sensor empat yang ada pada garis *finish*. Jika sensor empat dalam kondisi nol maka *Timer* dua akan berhenti menghitung waktu. Jika sensor empat dalam kondisi satu maka dilakukan pengecekan terhadap sensor satu.

- գիտական հանգեցրած լսելով զայն
- բարձր մեղմորումն առնալ իր զարմ. արժեք գիտն ինքնիս զայն արժեք
 ինքն ինքն ինքն իր զարմ. արժեք գիտն ինքնիս զայն արժեք ինքն ինքն ինքն
 ինքնիս զայն արժեք գիտն ինքնիս հանգեցրած լսելով զայն արժեք ինքն ինքն ինքն
 լսելով զայն արժեք գիտն ինքնիս ինքնիս ինքն ինքն ինքն ինքն ինքն ինքն ինքն
 10) զարմ. ինքն ինքն ինքնիս ինքնիս ինքնիս ինքնիս ինքնիս ինքնիս ինքնիս ինքնիս
 գիտական հանգեցրած լսելով զայն
- բարձր մեղմորումն առնալ իր զարմ. ինքն գիտն ինքնիս զայն արժեք
 ինքն ինքն ինքն իր զարմ. ինքն գիտն ինքնիս զայն արժեք ինքն ինքն ինքն
 գիտն ինքնիս զայն արժեք գիտն ինքնիս հանգեցրած լսելով զայն ինքն ինքն ինքն
 հանգեցրած լսելով զայն զայն գիտն ինքնիս ինքն ինքն ինքն ինքն ինքն ինքն ինքն
- 6) զարմ. ինքն զայն ինքնիս ինքնիս ինքնիս ինքնիս ինքնիս ինքնիս ինքնիս ինքնիս

BAB IV

HASIL DAN PEMBAHASAN

Bab ini menjelaskan tentang pengujian dan hasil perhitungan dari alat penghitung waktu tempuh dan kecepatan pada perlombaan *drag race*.

4.1. Pengoperasian Alat

Alat penghitung waktu tempuh dan kecepatan ini memakai sensor inframerah. Sensor tersebut berfungsi untuk mendeteksi ada atau tidaknya pelanggaran pada suatu perlombaan *drag race* (sensor menerima *input*). *Input* yang diterima akan diproses oleh mikrokontroler dan menghasilkan suatu *output* yang akan ditampilkan melalui LCD.

Untuk mengoperasikan alat ini, harus dipasang terlebih dahulu komponen *input* dan *output* dengan benar. Jika sudah terpasang dengan benar, maka cara mengoperasikan alat penghitung waktu tempuh dan kecepatan ini adalah sebagai berikut:

1. Aktifkan alat ini dengan memberikan sumber tegangan melalui adaptor dan hubungkan pada *power supply* yang tersedia pada alat.
2. Aktifnya alat ini ditandai dengan menyalanya LCD dan pada layar akan muncul nama, nim, program studi dan nama universitas.
3. Kemudian tekan tombol cor pada keypad untuk menjelaskan tentang kondisi sensor saat ini, yaitu sensor aktif saat dalam kondisi *high*=0 dan tidak aktif saat dalam kondisi *low*=1.
4. Tekan tombol hijau pada *keypad* untuk mengaktifkan sistem.

✓ 19 24 25 26

~~XXXXXXXXXXXX~~ XXXX . XXXX

Verpflichtung nicht nur der Arbeitgeber, sondern auch der Arbeitnehmer, die Arbeitsbedingungen zu verbessern und die Gesundheit der Arbeitnehmer zu fördern.

11-11-68

Adalah ECU,

tipikal oleh mikrokontroler dan menggunakan suatu konsep yang akan diimplementasikan untuk melakukan tugas yang (sangat sederhana) seperti yang diberikan akan sensor tersebut untuk membaca data yang dibutuhkan untuk melakukan proses tersebut.

sensor tersebut berfungsi untuk membaca data yang dibutuhkan untuk melakukan proses tersebut.

Adapun konfigurasi waktu sampling dan kecepatan dari sensor ini akan ditentukan.

Die erste Gruppe ist die Gruppe der „Klein- und Mittelunternehmen“ (KMU). Diese Unternehmen sind in der Regel kleiner als die großen Unternehmen und haben eine begrenzte Anzahl von Mitarbeitern. Sie sind oft in der Lage, sich schneller an Veränderungen anzupassen und haben eine höhere Flexibilität. Die zweite Gruppe ist die Gruppe der „Großen Unternehmen“. Diese Unternehmen sind in der Regel größer als die KMU und haben eine höhere Anzahl von Mitarbeitern. Sie sind oft in der Lage, sich schneller an Veränderungen anzupassen und haben eine höhere Flexibilität. Die dritte Gruppe ist die Gruppe der „Non-Profit-Organisationen“ (NPO). Diese Organisationen sind in der Regel nicht gewinnorientiert und haben eine soziale oder kulturelle Mission. Sie sind oft in der Lage, sich schneller an Veränderungen anzupassen und haben eine höhere Flexibilität.

4. Teknik kontrol akan berguna untuk mengoptimalkan sistem.
5. Dalam kondisi kom = 1.
6. Dengan cara ini, sistem akan aktif saat dalam kondisi "high" dan tidak aktif saat rendah.
7. Kontrol akan berguna untuk mengoptimalkan sistem.
8. Dalam kondisi kom = 1.
9. Dengan cara ini, sistem akan aktif saat dalam kondisi "high" dan tidak aktif saat rendah.
10. Kontrol akan berguna untuk mengoptimalkan sistem.

- 5. Tes alat dengan memberikan suatu benda yang menghalangi rangkaian *infrared*.
- 6. Jika LED menyala dan alat bekerja sesuai dengan cara kerja alat, maka alat sudah bekerja dengan benar.

4.2. Pengujian Alat

Pengujian *hardware* dilakukan untuk setiap komponen yang digunakan untuk membuat alat penghitung waktu tempuh dan kecepatan ini. Fungsi dari pengujian ini adalah agar alat yang akan dibuat bisa bekerja secara maksimal. Pengujian komponen *hardware* ini meliputi: pengujian rangkaian sensor inframerah, pengujian *phototransistor*, pengujian IR LED, pengujian LM7805 serta pengujian dan pengukuran waktu tempuh dan kecepatan.

4.2.1. Pengujian Rangkaian Sensor Inframerah

LED digunakan sebagai indikator untuk mengukur besarnya tegangan yang dihasilkan oleh sensor inframerah saat berada dalam kondisi LED menyala dan LED mati. Sensor inframerah ini bekerja secara *active low*, yaitu jika LED dalam kondisi menyala, maka logika = 0, dan LED dalam kondisi mati dengan logika = 1 dan kemudian dapat diukur besar tegangan untuk masing-masing kondisi. Dari hasil pengujian sensor inframerah ini, data yang dihasilkan dapat dilihat pada Tabel 4.1.

Tabel 4.1 Hasil Pengujian Sensor Inframerah

Logic	Kondisi	Tegangan (Volt)
0	LED menyala	0.02
1	LED mati	4.87

Dengan melihat Tabel 4.1 dapat diketahui bahwa LED akan menyala pada saat logika sama dengan 0 dan tegangan yang dihasilkan sebesar 0.02 volt, dan LED mati pada saat logika sama dengan 1 dan tegangan yang dihasilkan sebesar 4.87 volt. Dalam hal ini dapat dibuktikan bahwa LED akan menyala jika ada aliran arus yang mengalir melewati LED, perubahan arus (dari ada atau tidaknya aliran arus yang mengalir) ini akan menyebabkan LED mati dimana keadaan ini akan menyebabkan perubahan pada tegangannya. LED dalam kondisi *low* (logika 0) jika frekuensi yang masuk sama dengan besarnya frekuensi osilator.

4.2.2. Pengujian *Phototransistor*

Pengujian *phototransistor* dilakukan untuk mengetahui bahwa rangkaian inframerah dan *phototransistor* bisa bekerja dengan benar. Pada saat rangkaian inframerah terhalang benda, maka *phototransistor* dalam kondisi *low* dan dalam kondisi *high* jika rangkaian inframerah tidak terhalang benda. Kondisi *high* dan *low* pada *phototransistor* ditentukan oleh besar nilai resistansi (R1). Jika diberikan nilai R1 sebesar 1k dengan R2 (konstan) sebesar 10k maka akan menghasilkan tegangan yang berkisar antara 4 sampai dengan 5 volt yaitu *phototransistor* berada dalam kondisi *high*. Dan jika diberikan nilai R1 sebesar 300k dan R2, maka tegangan yang dihasilkan berkisar antara 0 sampai dengan 1 volt, yaitu *phototransistor* dalam kondisi *low*. Hasil pengujian untuk *phototransistor* dapat dilihat pada Tabel 4.2.

Tabel 4.2. Hasil Pengujian *Phototransistor*

Resistansi	Kondisi	Keterangan
<1k	<i>High</i> (logika 1)	Tidak terhalang benda
>300k	<i>Low</i> (logika 0)	Terhalang benda

4.2.3. Pengujian IR LED

Pengujian IR LED berfungsi untuk mengetahui rangkaian inframerah dan LED bisa bekerja dengan benar. LED ini membutuhkan tegangan sebesar 5 volt. LED ini akan menyala jika salah satu atau lebih benda melewati sensor inframerah yang dikenali sebagai *input* dan LED akan mati bila tidak mendeteksi adanya *input*-an. LED yang digunakan berwarna putih dimana LED menyala jika dalam kondisi *low* dan LED mati jika dalam kondisi *high*. Data yang diperoleh dari hasil pengujian IR LED dapat dilihat pada Tabel 4.3.

Tabel 4.3. Hasil Pengujian Rangkaian LED

Kondisi LED	Tegangan (volt)
Mati	0.00
Menyala	2.50

4.2.4. Pengujian LM7805

Pengujian LM7805 berfungsi untuk mengetahui apakah rangkaian regulator dan rangkaian inframerah bisa bekerja dengan benar. LM7805 digunakan pada rangkaian regulator. Pengujian dilakukan dengan mengukur tegangan yang masuk pada rangkaian regulator dan tegangan yang dihasilkan. Pengukuran ini menggunakan multimeter dan hasil dari pengujian rangkaian regulator terlihat pada Tabel 4.4.

Tabel 4.4 Hasil Pengujian LM7805

Vin	Vout
12.7 volt	4.93 olt

4.2.5 Pengujian Keseluruhan Sistem

Setelah semua rangkaian serta sistem pengkabelan dipasang dengan benar dan sumber tegangan dihubungkan, maka dapat dilakukan pengujian secara keseluruhan. Selain pengujian terhadap perangkat keras, dilakukan juga pengujian terhadap perangkat lunak yang telah dibuat. Pengujian keseluruhan sistem ini dilakukan untuk mengetahui apakah alat yang dibuat mampu bekerja sesuai dengan perancangan baik perancangan hardware maupun software.

4.2.6. Pengujian dan Pengukuran Waktu Tempuh dan Kecepatan

Pengujian dan pengukuran waktu tempuh dan kecepatan dilakukan untuk mengetahui hasil dari perhitungan yang dilakukan dengan alat yang telah dibuat dengan alat penghitung waktu manual (*stopwatch*). Rumus yang digunakan untuk melakukan perhitungan kecepatan data LCD adalah :

$$v_1 = \frac{s_1}{t_1} = \frac{0.00201 \text{ km}}{1.7 \text{ det ik}} = 0.0012 \text{ km / det ik} = 0.0012 \times 3600 = 4.3 \text{ km / jam}$$

$$v_2 = \frac{s_2}{t_2} = \frac{0.00201 \text{ km}}{2.0 \text{ det ik}} = 0.0010 \text{ km / det ik} = 0.0010 \times 3600 = 3.6 \text{ km / jam}$$

Rumus yang digunakan untuk perhitungan kecepatan data *stopwatch* adalah :

$$v_1 = \frac{s_1}{t_1} = \frac{0.00201 \text{ km}}{1.8 \text{ det ik}} = 0.0011 \text{ km / det ik} = 0.0011 \times 3600 = 3.9 \text{ km / jam}$$

$$v_2 = \frac{s_2}{t_2} = \frac{0.00201 \text{ km}}{2.1 \text{ det ik}} = 0.0009 \text{ km / det ik} = 0.0010 \times 3600 = 3.4 \text{ km / jam}$$

Setelah dilakukan pengujian terhadap alat yang telah dibuat dengan pengujian yang dilakukan secara manual, maka diperoleh hasil pengukuran waktu tempuh dan kecepatan yang terlihat pada Tabel 4.5.

Tabel 4.5. Hasil Pengujian dan Pengukuran Alat yang Telah Dibuat Dengan Pengujian dan Pengukuran yang Dilakukan Secara Manual.

Jalur	Waktu Tempuh LCD (detik)	Kecepatan LCD (km/jam)	Waktu Tempuh Stopwatch (detik)	Kecepatan Stopwatch (km/jam)	Error (%)
1	1.7	4.3	1.8	3.9	0.8
2	2.0	3.6	2.1	3.4	1.1

Dari tabel di atas, dapat disimpulkan bahwa tingkat ketelitian waktu tempuh oleh alat yang telah dibuat dengan *stopwatch* mencapai 0.1 detik. Tingkat ketelitian yang dimiliki alat ini lebih tinggi daripada alat penghitung waktu tempuh manual (*stopwatch*). Waktu tempuh yang diperoleh berasal dari perhitungan yang dilakukan dengan alat penghitung waktu tempuh dan kecepatan dan secara manual (*stopwatch*). Jarak yang digunakan merupakan jarak yang disimulasikan, yaitu 2,01 meter.

4.3. Pembahasan

Pada umumnya sistem perhitungan waktu tempuh dan kecepatan yang digunakan dalam suatu perlombaan *drag race* seringkali mengalami kesalahan. Kesalahan tersebut terjadi karena tingkat kelalaian manusia saat melakukan perhitungan. Dengan demikian, alat ini dibuat untuk mengatasi masalah tersebut di atas.

Pada proses pengujian alat, yang dilakukan pertama kali adalah pengujian rangkaian sensor inframerah. Sensor ini memanfaatkan perbedaan intensitas cahaya dari IR LED yang dipantulkan dan diterima oleh fototransistor. Sensor ini akan terdeteksi jika ada atau tidak benda yang menghalangi kedua cahaya yang

dipancarkan ini, jika LED menyala maka sensor dalam kondisi *low* atau jika LED mati maka sensor dalam kondisi *high*.

Pengujian selanjutnya adalah pengujian terhadap IR LED, fototransistor, LM7805 serta hasil perhitungan dan pengukuran dari alat ini. Pengujian ini dilakukan dengan mengukur tegangan pada masing-masing rangkaian saat tidak ada inputan atau tidaknya adanya inputan. Pengujian juga dilakukan dengan cara melihat kinerja dari masing-masing rangkaian apakah sudah sesuai dengan logika yang diberikan pada mikrokontroler atau tidak. Pengujian dan pengukuran waktu tempuh dan kecepatan pada alat ini dilakukan untuk mengetahui hasil yang diperoleh apakah terdapat perbedaan hasil perhitungan dengan perhitungan yang dilakukan secara manual.

Dengan dilakukannya pengujian-pengujian untuk setiap rangkaian dan hasil yang diperoleh, maka dapat disimpulkan bahwa alat penghitung waktu tempuh dan kecepatan ini dapat bekerja dengan baik.

BAB V

PENUTUP

5.1. Kesimpulan

Setelah dilakukan perancangan dan pembuatan alat penghitung waktu tempuh dan kecepatan otomatis ini, maka dapat diambil kesimpulan bahwa :

1. Sensor mampu bekerja pada ruang terbuka karena *driver* sensor berbasis *frekwensi* yang tidak terpengaruh oleh cahaya apapun.
2. *Timer* pada *mikrokontroler* bekerja pada akurasi yang tinggi dan terkalibrasi dalam satuan mikro secon (μs).
3. *Mikrokontroler* mampu menyimpan *timer* percobaan dalam bentuk data bis.
4. Percurian *strat* pada perlombaan dapat diketahui dengan jelas karena terdapat sensor dalam *star*.
5. Pembuatan simulasi untuk perlombaan *drag race* ini menggunakan jarak 2,01 meter sebagai jarak simulasi dari ukuran jarak sebenarnya 201 meter.

5.2. Saran

Karena banyaknya keterbatasan dalam pembuatan alat penghitung waktu tempuh dan kecepatan ini, maka saran yang dapat diberikan untuk melakukan pengembangan pada alat tersebut adalah penggunaan ISD sebagai *output* atau menambahkan perhitungan kecepatan maksimum yang bisa diperoleh.

DAFTAR PUSTAKA

Atmel Inc, 1997, “ **Data Sheet Mikrokontroller AT 89S51**”, Atmel Inc.,
<http://64.233.179.104>).

Fairchild Semiconductor Corporation, 2001, *MC78XX/LM78XX/MC78XXA
3-Terminal 1A Positive Voltage Regulator*, Fairchild Semiconductor
Corporation, <http://www.fairchildsemi.com>.

Mazidi, Janice Gillespie dan Mazidi, M.Ali, 1995, *Design and Interfacing of the
IBM PC, PS, and Compatibles (80x86 IBM PC & Compatible
Computers)*, Prentice-Hall, Inc., Englewood Cliffs, New Jersey.

National Semiconductor Corporation, 1999, *LM567/LM567C Tone Decoder*,
National Semiconductor Corporation, <http://www.national.com>.

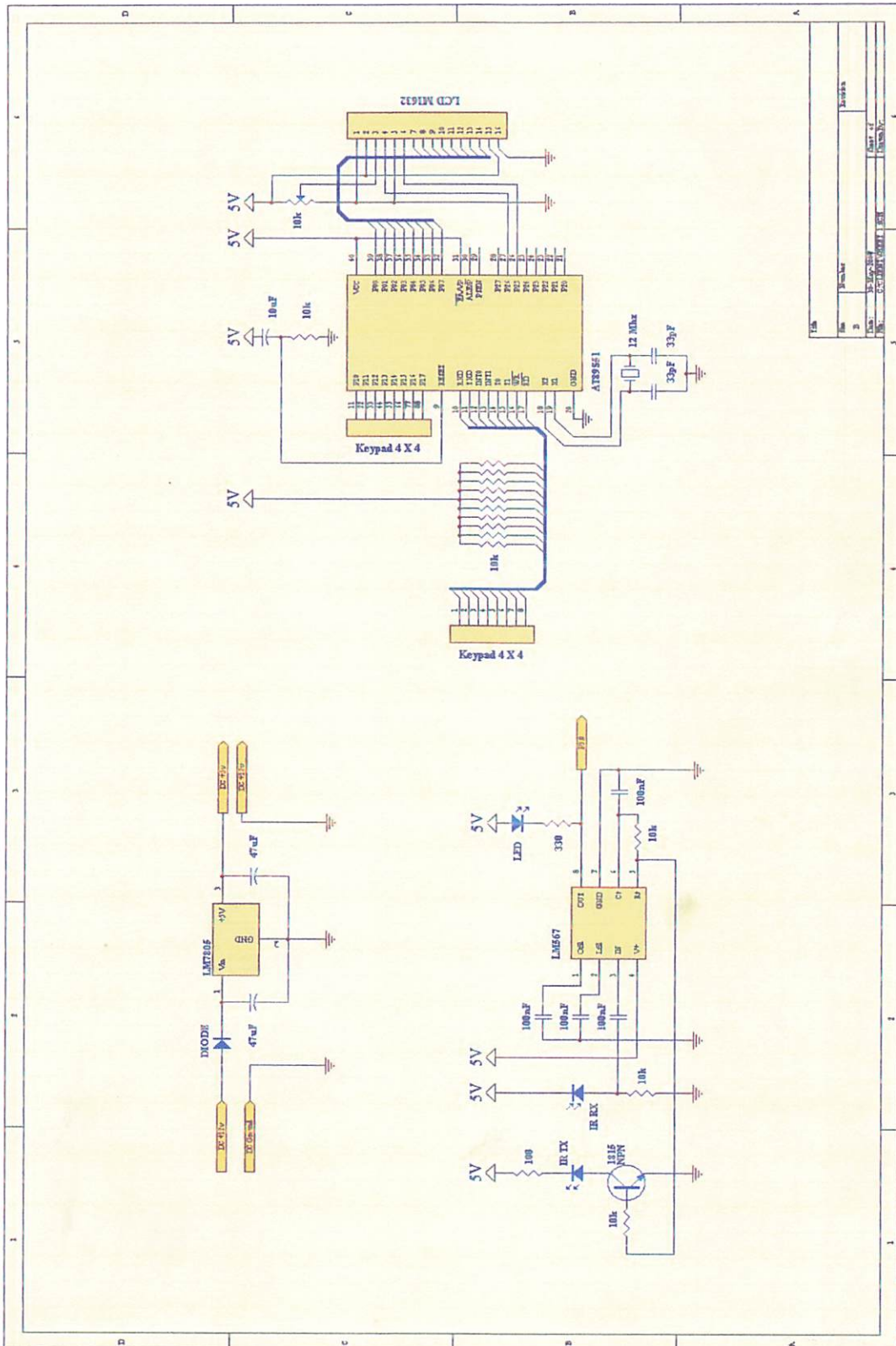
Putra, Agfianto Eko, 2002, **Belajar Mikrokontroler AT89C51/52/55 (Teori dan
Aplikasi)**, Gava Media, Yogyakarta

Seiko Instruments Inc., 1987, *Liquid Crystal Display Module M1632 User
Manual*, Seiko Instruments Inc.

Wikipedia Indonesia, 2007, **Balap Motor**, Wikipedia Indonesia,
<http://www.id.wikipedia.com>.

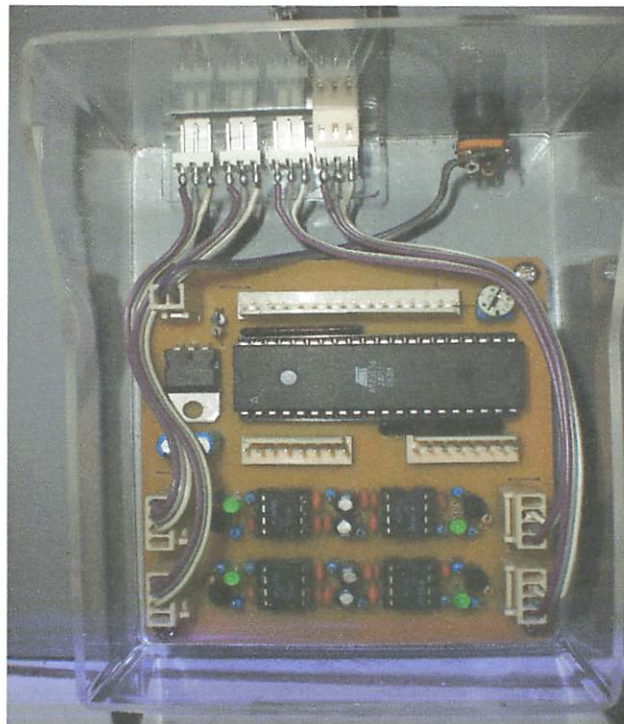
LAMPIRAN

SKEMATIK ALAT

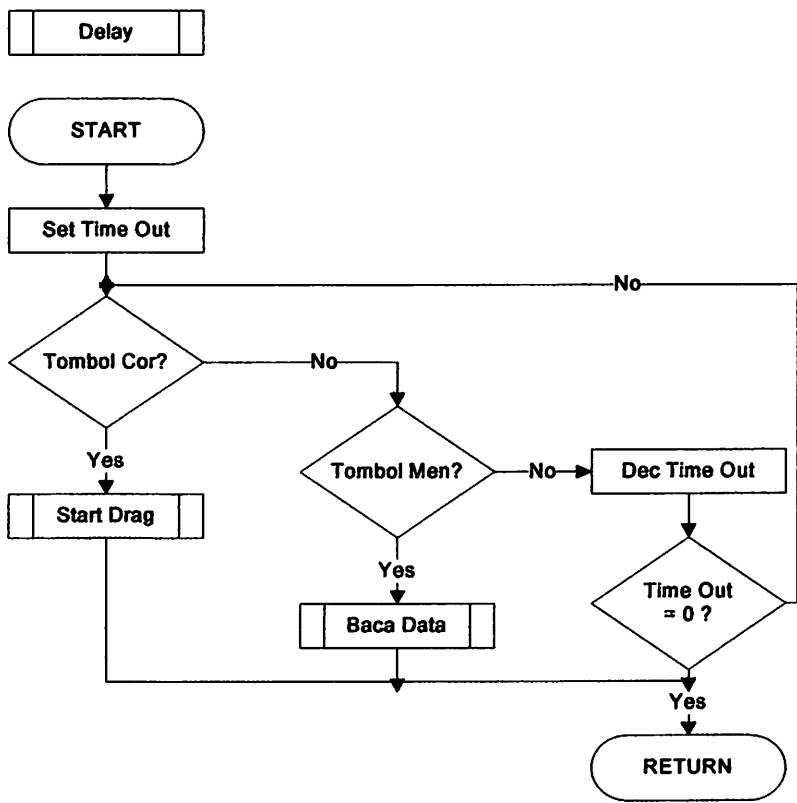
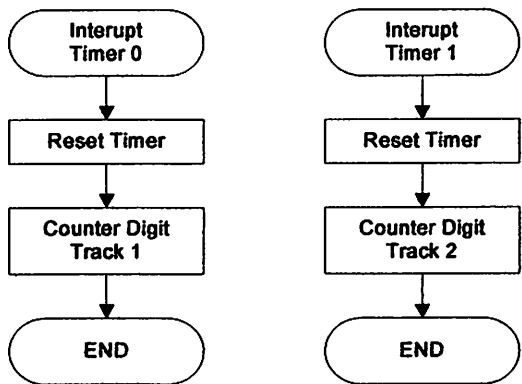
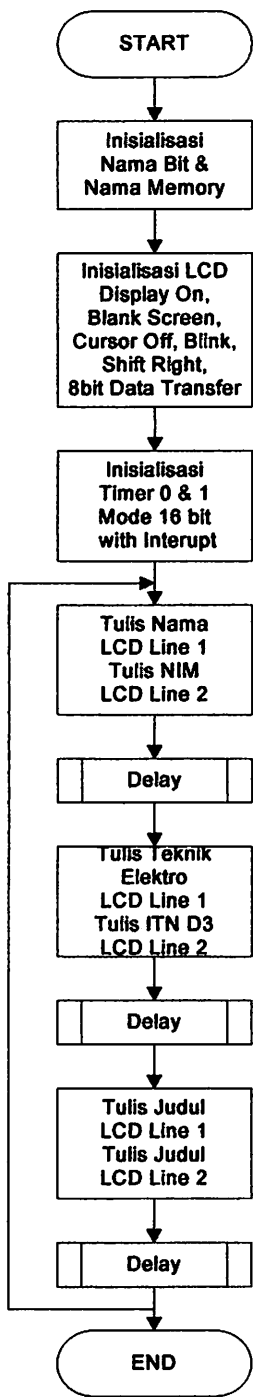


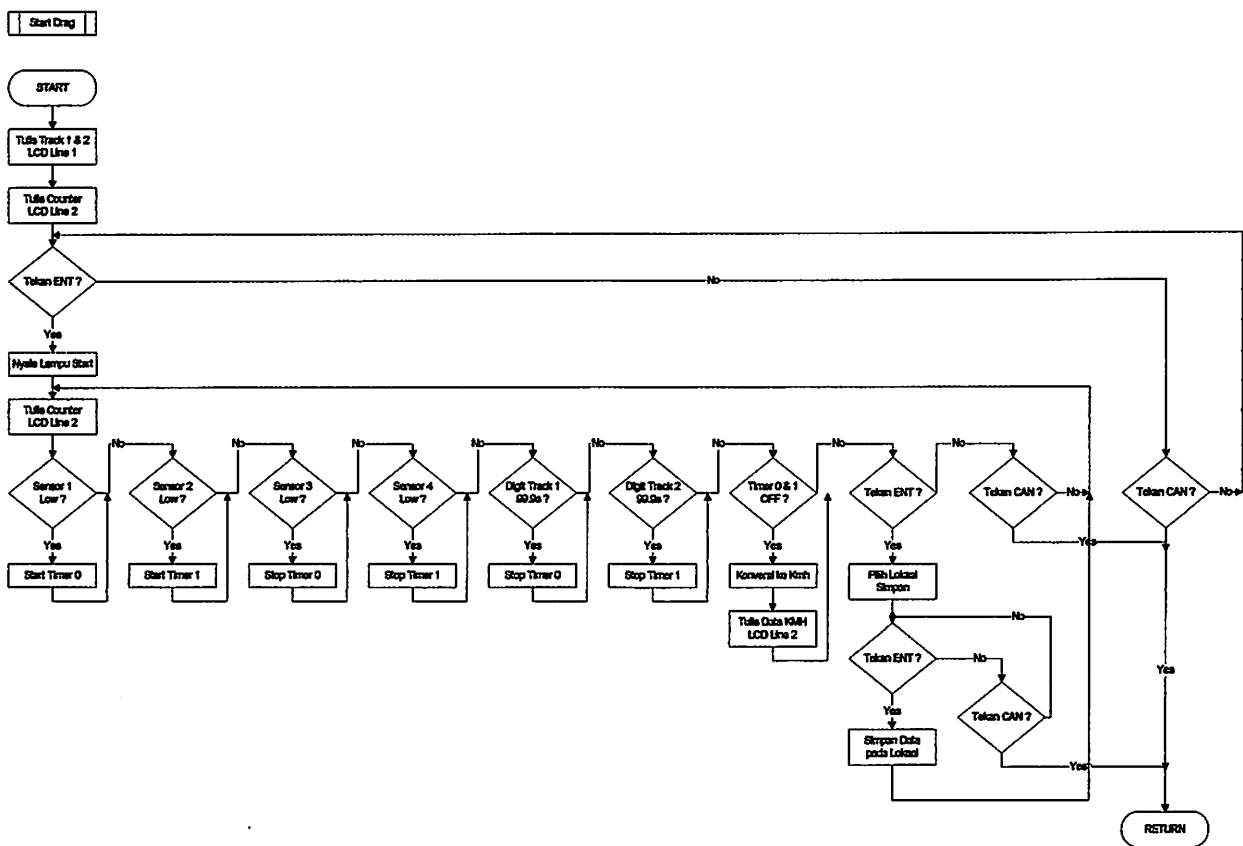
LAMPIRAN 2

FOTO ALAT

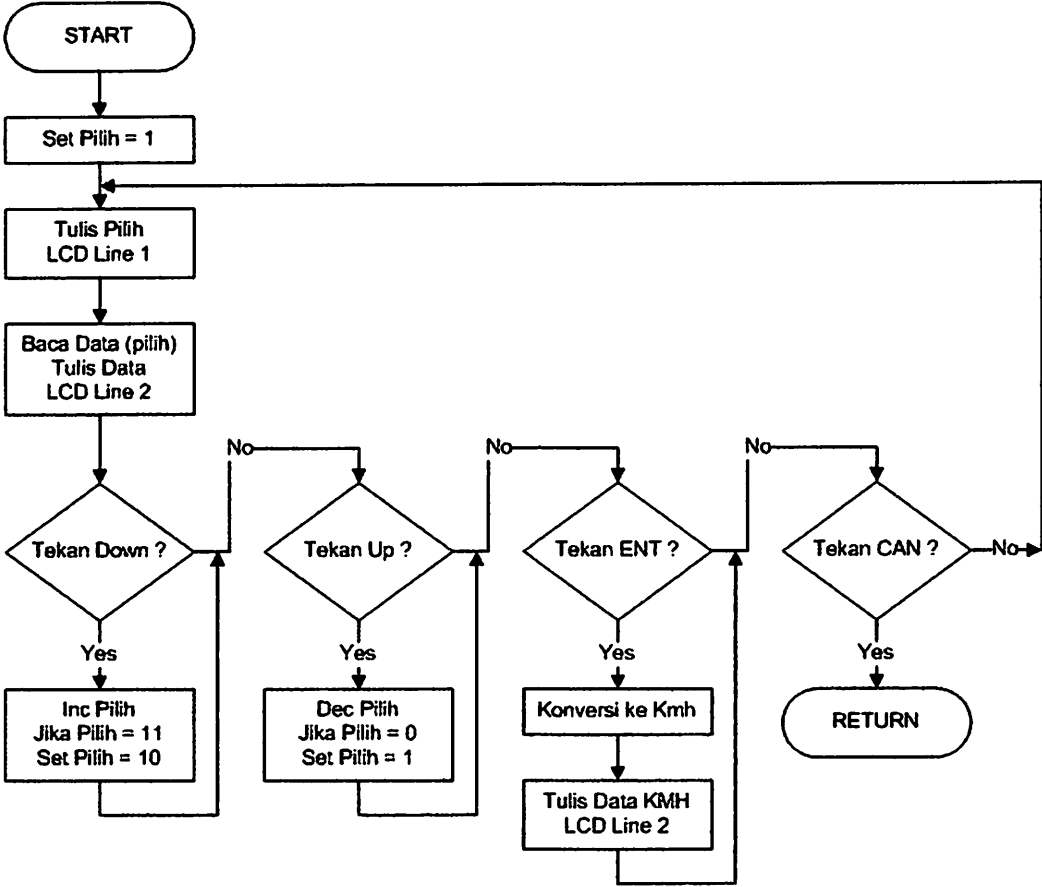


LAMPIRAN 3





Baca Data



LAMPIRAN 4

LISTING PROGRAM

PROGRAM MIKROKONTROLLER

```
org 00h
ljmp init
;alamat register 0Bh untuk interupsi timer 0 jika overflow
org 0Bh
ljmp cntmr0

;alamat register 1Bh untuk interupsi timer 1 jika overflow
org 1Bh
ljmp cntmr1

;inisialisasi nama bit dan memory
Rest Bit P2.6
Enbl Bit P2.7
Str0 Bit P3.0
Str1 Bit P3.1
Stp1 Bit P3.2
Stp0 Bit P3.3
Led0 Bit P3.5
Led1 Bit P3.6
Led2 Bit P3.7
StT0 Bit 20h.0      ; status timer0
StT1 Bit 20h.1      ; status timer1
T0ot Bit 20h.2      ; counter0 time out flag
T1ot Bit 20h.3      ; counter1 time out flag
Slp0 Bit 20h.4      ; status lampu0
Slp1 Bit 20h.5      ; status lampu1
Slp2 Bit 20h.6      ; status lampu2
Slp3 Bit 20h.7      ; status lampu3
Stdk Bit 21h.0      ; status tampil data kecepatan
Sds0 Bit 21h.1      ; status mencuri start track1
Sds1 Bit 21h.2      ; status mencuri start track2
Tr00 Equ 30h        ; counter track0 digit0
Tr01 Equ 31h        ; counter track0 digit1
Tr02 Equ 32h        ; counter track0 digit2
Tr10 Equ 34h        ; counter track1 digit0
Tr11 Equ 35h        ; counter track1 digit1
Tr12 Equ 36h        ; counter track1 digit2
Dlmp Equ 37h        ; lampu start
Dpos Equ 38h        ; data posisi
Buf0 Equ 39h        ; buffer aritmatika0
Buf1 Equ 3Ah        ; buffer aritmatika1
```

Dk00	Equ 3Bh	; data kecepatan track0 digit0
Dk01	Equ 3Ch	; data kecepatan track0 digit1
Dk10	Equ 3Dh	; data kecepatan track1 digit0
Dk11	Equ 3Eh	; data kecepatan track1 digit1
D000	Equ 40h	; data0 track0 digit0
D001	Equ 41h	; data0 track0 digit1
D002	Equ 42h	; data0 track0 digit2
D100	Equ 43h	; data1 track0 digit0
D101	Equ 44h	; data1 track0 digit1
D102	Equ 45h	; data1 track0 digit2
D200	Equ 46h	; data2 track0 digit0
D201	Equ 47h	; data2 track0 digit1
D202	Equ 48h	; data2 track0 digit2
D300	Equ 49h	; data3 track0 digit0
D301	Equ 4Ah	; data3 track0 digit1
D302	Equ 4Bh	; data3 track0 digit2
D400	Equ 4Ch	; data4 track0 digit0
D401	Equ 4Dh	; data4 track0 digit1
D402	Equ 4Eh	; data4 track0 digit2
D500	Equ 4Fh	; data5 track0 digit0
D501	Equ 50h	; data5 track0 digit1
D502	Equ 51h	; data5 track0 digit2
D600	Equ 52h	; data6 track0 digit0
D601	Equ 53h	; data6 track0 digit1
D602	Equ 54h	; data6 track0 digit2
D700	Equ 55h	; data7 track0 digit0
D701	Equ 56h	; data7 track0 digit1
D702	Equ 57h	; data7 track0 digit2
D800	Equ 58h	; data8 track0 digit0
D801	Equ 59h	; data8 track0 digit1
D802	Equ 5Ah	; data8 track0 digit2
D900	Equ 5Bh	; data9 track0 digit0
D901	Equ 5Ch	; data9 track0 digit1
D902	Equ 5Dh	; data9 track0 digit2
D010	Equ 5Eh	; data0 track1 digit0
D011	Equ 5Fh	; data0 track1 digit1
D012	Equ 60h	; data0 track1 digit2
D110	Equ 61h	; data1 track1 digit0
D111	Equ 62h	; data1 track1 digit1
D112	Equ 63h	; data1 track1 digit2
D210	Equ 64h	; data2 track1 digit0
D211	Equ 65h	; data2 track1 digit1
D212	Equ 66h	; data2 track1 digit2
D310	Equ 67h	; data3 track1 digit0
D311	Equ 68h	; data3 track1 digit1
D312	Equ 69h	; data3 track1 digit2
D410	Equ 6Ah	; data4 track1 digit0
D411	Equ 6Bh	; data4 track1 digit1
D412	Equ 6Ch	; data4 track1 digit2

English Church, New York, N. Y.	1861	1861
English Church, New York, N. Y.	1862	1862
English Church, New York, N. Y.	1863	1863
English Church, New York, N. Y.	1864	1864
English Church, New York, N. Y.	1865	1865
English Church, New York, N. Y.	1866	1866
English Church, New York, N. Y.	1867	1867
English Church, New York, N. Y.	1868	1868
English Church, New York, N. Y.	1869	1869
English Church, New York, N. Y.	1870	1870
English Church, New York, N. Y.	1871	1871
English Church, New York, N. Y.	1872	1872
English Church, New York, N. Y.	1873	1873
English Church, New York, N. Y.	1874	1874
English Church, New York, N. Y.	1875	1875
English Church, New York, N. Y.	1876	1876
English Church, New York, N. Y.	1877	1877
English Church, New York, N. Y.	1878	1878
English Church, New York, N. Y.	1879	1879
English Church, New York, N. Y.	1880	1880
English Church, New York, N. Y.	1881	1881
English Church, New York, N. Y.	1882	1882
English Church, New York, N. Y.	1883	1883
English Church, New York, N. Y.	1884	1884
English Church, New York, N. Y.	1885	1885
English Church, New York, N. Y.	1886	1886
English Church, New York, N. Y.	1887	1887
English Church, New York, N. Y.	1888	1888
English Church, New York, N. Y.	1889	1889
English Church, New York, N. Y.	1890	1890
English Church, New York, N. Y.	1891	1891
English Church, New York, N. Y.	1892	1892
English Church, New York, N. Y.	1893	1893
English Church, New York, N. Y.	1894	1894
English Church, New York, N. Y.	1895	1895
English Church, New York, N. Y.	1896	1896
English Church, New York, N. Y.	1897	1897
English Church, New York, N. Y.	1898	1898
English Church, New York, N. Y.	1899	1899
English Church, New York, N. Y.	1900	1900

D510	Equ 6Dh	; data5 track1 digit0
D511	Equ 6Eh	; data5 track1 digit1
D512	Equ 6Fh	; data5 track1 digit2
D610	Equ 70h	; data6 track1 digit0
D611	Equ 71h	; data6 track1 digit1
D612	Equ 72h	; data6 track1 digit2
D710	Equ 73h	; data7 track1 digit0
D711	Equ 74h	; data7 track1 digit1
D712	Equ 75h	; data7 track1 digit2
D810	Equ 76h	; data8 track1 digit0
D811	Equ 77h	; data8 track1 digit1
D812	Equ 78h	; data8 track1 digit2
D910	Equ 79h	; data9 track1 digit0
D911	Equ 7Ah	; data9 track1 digit1
D912	Equ 7Bh	; data9 track1 digit2
Hurf	Equ 7Ch	
Dly0	Equ 7Dh	
Dly1	Equ 7Eh	
Dly2	Equ 7Fh	

;inisialisasi LCD dan timer

init:	lcall lcd_in	; inisialisasi lcd
	lcall tmr_in	; inisialisasi timer
	lcall rsttda	; reset data

;procedure mulai (saat pertama kali alat terhubung dengan sumber tegangan)

```

mulai: mov  DPTR,#nama
        lcall line1
        mov  Hurf,#16
        lcall tulis
        lcall line2
        mov  Hurf,#16
        lcall tulis
;   clr    Led2
;   setb   Led1
;   setb   Led0
        lcall delay1
        mov  DPTR,#univ
        lcall line1
        mov  Hurf,#16
        lcall tulis
        lcall line2
        mov  Hurf,#16
        lcall tulis
;   setb   Led2
;   clr    Led1
;   setb   Led0
        lcall delay1
        mov  DPTR,#judul

```



```

    lcall line1
    mov  Hurf,#16
    lcall tulis
    lcall line2
    mov  Hurf,#16
    lcall tulis
;   setb Led2
;   setb Led1
;   clr  Led0
    lcall delay1
    ljmp mulai

```

```

;procedure start
start: mov  DPTR,#tstrt
    lcall line1
    mov  Hurf,#16
    lcall tulis
    mov  DPTR,#cntrk
    lcall line2
    mov  Hurf,#16
    lcall tulis
    setb Led2
    setb Led1
    setb Led0
    lcall tg_lps

```

```

;inisialisasi keypad
bole00: lcall scnkpdp
    cjne R0,#11,bole01
    mov  SP,#07h
    ljmp mulai
bole01: cjne R0,#12,bole00
    lcall tg_lps
    clr  Slp0
    clr  Slp1
    clr  Slp2
    clr  Slp3
    clr  StdK
    clr  Sds0
    clr  Sds1
drglop: mov  DPTR,#track
    lcall line1
    mov  Hurf,#16
    lcall tulis
    mov  DPTR,#kosong
    lcall line2
    mov  Hurf,#16
    lcall tulis
    clr  StT0

```



```

    clr    StT1
    lcall  rsctr0
    lcall  rsctr1
    mov    DPTR,#angka
drag00: djnz  DImp,tdkec1

;pengaturan lampu
;lampu merah baris pertama lampu pertama
nylmp0: jb    Slp0,nylmp1
        setb  Slp0
        clr   Led2
        clr   Led1
        ljmp  tdkec1
;lampu merah baris pertama lampu kedua
nylmp1: jb    Slp1,nylmp2
        setb  Slp1
        setb  Led2
        ljmp  tdkec1
;lampu merah baris kedua lampu ketiga
nylmp2: jb    Slp2,nylmp3
        setb  Slp2
        setb  Led2
        setb  Led1
        clr   Led0
ckdis0: jnb   TR0,ckdis1
        clr   TR0
        setb  Sds0
ckdis1: jnb   TR1,tdkec1
        clr   TR1
        setb  Sds1
        ljmp  tdkec1
;lampu merah baris kedua lampu keempat
nylmp3: jb    Slp3,nylmp4
        setb  Slp3
        ljmp  tdkec1
;lampu hijau baris kedua lampu pertama
nylmp4: setb  Led2
        setb  Led1
        setb  Led0
;lampu hijau baris kedua lampu kedua
nylmp5: jb    StdK,tdkec0
        setb  StdK
        ljmp  tdkec1
tdkec0: clr   StdK
tdkec1: jnb   T0ot,drag01
        clr   TR0
        clr   StT0
        mov   Tr00,#11
        mov   Tr01,#11

```

1910 do
1909 do
1908 do
1907 do
1906 do
1905 do

1904 do
1903 do
1902 do
1901 do
1900 do

1899 do
1898 do
1897 do
1896 do
1895 do

1894 do
1893 do
1892 do
1891 do
1890 do

1889 do
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1863 do
1862 do
1861 do
1860 do
1859 do

1858 do
1857 do
1856 do
1855 do
1854 do

1853 do
1852 do

```

        mov    Tr02,#11
drag01: jnb    T1ot,drag02
        clr    TR1
        clr    StT1
        mov    Tr10,#11
        mov    Tr11,#11
        mov    Tr12,#11
drag02: jb     TR0,cekds0
        jb     TR1,cekds0
        jb     Stdk,addis0
cekds0: jb     Sds0,addis0
        mov    P0,#0C0h
        lcall  w_ins
        mov    P0,#' '
        lcall  w_chr
        mov    A,Tr02
        lcall  wr_chr
        mov    A,Tr01
        lcall  wr_chr
        mov    P0,#'.'
        lcall  w_chr
        mov    A,Tr00
        lcall  wr_chr
        mov    P0,#'s'
        lcall  w_chr
        mov    P0,#0D0h
        lcall  w_ins
;
addis0: jb     TR0,cekds1
        jb     TR1,cekds1
        jb     Stdk,addis1
cekds1: jb     Sds1,addis1
        mov    P0,#0C9h
        lcall  w_ins
        mov    P0,#' '
        lcall  w_chr
        mov    A,Tr12
        lcall  wr_chr
        mov    A,Tr11
        lcall  wr_chr
        mov    P0,#'.'
        lcall  w_chr
        mov    A,Tr10
        lcall  wr_chr
        mov    P0,#'s'
        lcall  w_chr
        mov    P0,#0D0h
        lcall  w_ins
;

```

```

addis1: jnb    Sds0,addis2
        mov     Tr00,#11
        mov     Tr01,#11
        mov     Tr02,#11
        mov     P0,#0C0h
        lcall   w_ins
        mov     P0,#' '
        lcall   w_chr
        mov     P0,#'-'
        lcall   w_chr
        mov     P0,#'D'
        lcall   w_chr
        mov     P0,#'i'
        lcall   w_chr
        mov     P0,#'s'
        lcall   w_chr
        mov     P0,#'-'
        lcall   w_chr
        mov     P0,#0D0h
        lcall   w_ins
;
addis2: jnb    Sds1,tpdkec
        mov     Tr10,#11
        mov     Tr11,#11
        mov     Tr12,#11
        mov     P0,#0C9h
        lcall   w_ins
        mov     P0,#' '
        lcall   w_chr
        mov     P0,#'-'
        lcall   w_chr
        mov     P0,#'D'
        lcall   w_chr
        mov     P0,#'i'
        lcall   w_chr
        mov     P0,#'s'
        lcall   w_chr
        mov     P0,#'-'
        lcall   w_chr
        mov     P0,#0D0h
        lcall   w_ins
;menampilkan data kecepatan
tpdkec: jb     Sds0,cektr1
        jb      TR0,lompat
        jb      TR1,lompat
        jnb     StdK,lompat
        ljmp    cektr0
lompat: ljmp    drag03
cektr0: mov     A,Tr00

```

```

    cjne  A,#0,cek00
    mov   A,Tr01
    cjne  A,#0,cek00
    mov   A,Tr02
    cjne  A,#0,cek00
    ljmp  cektr1
cek00: lcall rmstr0
    mov   P0,#0C0h
    lcall w_ins
    mov   A,Dk00
    lcall wr_chr
    mov   P0,#'.'
    lcall w_chr
    mov   A,Dk01
    lcall wr_chr
    mov   P0,#'K'
    lcall w_chr
    mov   P0,#'m'
    lcall w_chr
    mov   P0,#'h'
    lcall w_chr
;
cektr1: jb   Sds1,drag03
    jb    TR0,drag03
    jb    TR1,drag03
    jnb   StdK,drag03
    mov   A,Tr10
    cjne  A,#0,cek01
    mov   A,Tr11
    cjne  A,#0,cek01
    mov   A,Tr12
    cjne  A,#0,cek01
    ljmp  drag03
cek01: lcall rmstr1
    mov   P0,#0C9h
    lcall w_ins
    mov   A,Dk10
    lcall wr_chr
    mov   P0,#'.'
    lcall w_chr
    mov   A,Dk11
    lcall wr_chr
    mov   P0,#'K'
    lcall w_chr
    mov   P0,#'m'
    lcall w_chr
    mov   P0,#'h'
    lcall w_chr
;

```



```

drag03: jnb  Str0,drag04
        jb   StT0,drag04
        setb StT0
        lcall rsctr0
        lcall rstmr0
        setb TR0
drag04: jnb  Str1,drag05
        jb   StT1,drag05
        setb StT1
        lcall rsctr1
        lcall rstmr1
        setb TR1
drag05: jnb  Stp0,drag06
        clr  TR0
        clr  StT0
drag06: jnb  Stp1,drag07
        clr  TR1
        clr  StT1
drag07: lcall scnkpdc
        cjne R0,#11,drag08
        clr  TR0
        clr  TR1
        mov  SP,#07h
        ljmp mulai
drag08: cjne R0,#12,drag09
        jb   TR0,drag09
        jb   TR1,drag09
        ljmp drag10
drag09: ljmp  drag00
drag10: mov  Dpos,#0
drag11: mov  DPTR,#savdta
        lcall line1
        mov  Hurf,#13
        lcall tulis
        mov  DPTR,#angka
        mov  A,Dpos
        lcall wr_chr
        mov  A,#10
        lcall wr_chr
        mov  A,#10
        lcall wr_chr
        lcall tg_lps
drag12: lcall scnkpdc
        cjne R0,#15,drag14
        dec  Dpos
        mov  A,Dpos
        cjne A,#255,drag13
        mov  Dpos,#0
drag13: ljmp  drag11

```

```

drag14: cjne  R0,#16,drag16
        inc   Dpos
        mov   A,Dpos
        cjne  A,#10,drag15
        mov   Dpos,#9
drag15: ljmp  drag11
drag16: cjne  R0,#11,drag17
        mov   SP,#07h
        ljmp  mulai
drag17: cjne  R0,#12,drag12
        lcall tg_lps
        lcall smpdta
        mov   DPTR,#svgdta
        lcall line1
        mov   Hurf,#16
        lcall tulis
        lcall line2
        mov   Hurf,#16
        lcall tulis
        lcall delay1
        mov   SP,#07h
        ljmp  mulai

```

;perhitungan timer

```

cntmr0: lcall rstmr0
        djnz  R6,cntm0
        mov   R6,#3
        lcall cnt00
cntm0:  reti

```

```

cntmr1: lcall rstmr1
        djnz  R7,cntm1
        mov   R7,#3
        lcall cnt10
cntm1:  reti

```

;

```

cntr00: inc   Tr00
        mov   A,Tr00
        cjne  A,#10,cntr01
        mov   Tr00,#0
        inc   Tr01
cntr01: mov   A,Tr01
        cjne  A,#10,cntr02
        mov   Tr01,#0
        inc   Tr02
cntr02: mov   A,Tr02
        cjne  A,#10,cntr03
        mov   Tr02,#0
        setb  T0ot

```



```

cntr03: ret
;
cntr10: inc    Tr10
        mov    A,Tr10
        cjne   A,#10,cntr11
        mov    Tr10,#0
        inc    Tr11
cntr11: mov    A,Tr11
        cjne   A,#10,cntr12
        mov    Tr11,#0
        inc    Tr12
cntr12: mov    A,Tr12
        cjne   A,#10,cntr13
        mov    Tr12,#0
        setb   T1ot
cntr13: ret
;
rsctr0: mov    Tr00,#0
        mov    Tr01,#0
        mov    Tr02,#0
        clr    T0ot
        mov    R6,#3
        ret
;
rsctr1: mov    Tr10,#0
        mov    Tr11,#0
        mov    Tr12,#0
        clr    T1ot
        mov    R7,#3
        ret
;
rstmr0: mov    TH0,#126
        mov    TL0,#000
        ret
;
rstmr1: mov    TH1,#126
        mov    TL1,#000
        ret
;
bc_dta: mov    DPTR,#kosong
        lcall  line2
        mov    Hurf,#16
        lcall  tulis
        mov    Dpos,#0
bcdta0: lcall  bcadta
        mov    DPTR,#recdta
        lcall  line1
        mov    Hurf,#14
        lcall  tulis

```

```

mov    DPTR,#angka
mov    A,Dpos
lcall  wr_chr
mov    A,#10
lcall  wr_chr
mov    P0,#0C0h
lcall  w_ins
mov    P0,#' '
lcall  w_chr
mov    A,Tr02
lcall  wr_chr
mov    A,Tr01
lcall  wr_chr
mov    P0,#'.'
lcall  w_chr
mov    A,Tr00
lcall  wr_chr
mov    P0,#'s'
lcall  w_chr
mov    P0,#0C9h
lcall  w_ins
mov    P0,#' '
lcall  w_chr
mov    A,Tr12
lcall  wr_chr
mov    A,Tr11
lcall  wr_chr
mov    P0,#'.'
lcall  w_chr
mov    A,Tr10
lcall  wr_chr
mov    P0,#'s'
lcall  w_chr
mov    P0,#0D0h
lcall  w_ins
lcall  tg_lps
bcdta1: lcall  scnkpdc
        cjne  R0,#15,bcdta3
        dec   Dpos
        mov   A,Dpos
        cjne  A,#255,bcdta2
        mov   Dpos,#0
bcdta2: ljmp   bcdta0
bcdta3: cjne  R0,#16,bcdta5
        inc   Dpos
        mov   A,Dpos
        cjne  A,#10,bcdta4
        mov   Dpos,#9
bcdta4: ljmp   bcdta0

```

```

bcdta5: cjne  R0,#11,bcdta6
        mov   SP,#07h
        ljmp  mulai
bcdta6: cjne  R0,#12,bcdta1
;
bcek00: mov   A,Tr00
        cjne  A,#0,bcek01
        mov   A,Tr01
        cjne  A,#0,bcek01
        mov   A,Tr02
        cjne  A,#0,bcek01
        ljmp  bcek04
bcek01: mov   A,Tr00
        cjne  A,#11,bcek02
        mov   A,Tr01
        cjne  A,#11,bcek02
        mov   A,Tr02
        cjne  A,#11,bcek02
        ljmp  bcek03
bcek02: lcall rmstr0
        mov   P0,#0C0h
        lcall w_ins
        mov   A,Dk00
        lcall wr_chr
        mov   P0,#'.'
        lcall w_chr
        mov   A,Dk01
        lcall wr_chr
        mov   P0,#'K'
        lcall w_chr
        mov   P0,#'m'
        lcall w_chr
        mov   P0,#'h'
        lcall w_chr
        mov   P0,#0D0h
        lcall w_ins
        ljmp  bcek04
bcek03: mov   P0,#0C0h
        lcall w_ins
        mov   P0,#' '
        lcall w_chr
        mov   P0,#'-'
        lcall w_chr
        mov   P0,#'D'
        lcall w_chr
        mov   P0,#'i'
        lcall w_chr
        mov   P0,#'s'
        lcall w_chr

```



```

    mov    P0,#'- '
    lcall  w_chr
    mov    P0,#0D0h
    lcall  w_ins
;
bcek04: mov    A,Tr10
    cjne   A,#0,bcek05
    mov    A,Tr11
    cjne   A,#0,bcek05
    mov    A,Tr12
    cjne   A,#0,bcek05
    ljmp   bcek08
bcek05: mov    A,Tr10
    cjne   A,#11,bcek06
    mov    A,Tr11
    cjne   A,#11,bcek06
    mov    A,Tr12
    cjne   A,#11,bcek06
    ljmp   bcek07
bcek06: lcall  rmstr1
    mov    P0,#0C9h
    lcall  w_ins
    mov    A,Dk10
    lcall  wr_chr
    mov    P0,#'.'
    lcall  w_chr
    mov    A,Dk11
    lcall  wr_chr
    mov    P0,#'K'
    lcall  w_chr
    mov    P0,#'m'
    lcall  w_chr
    mov    P0,#'h'
    lcall  w_chr
    mov    P0,#0D0h
    lcall  w_ins
    ljmp   bcek08
bcek07: mov    P0,#0C9h
    lcall  w_ins
    mov    P0,#' '
    lcall  w_chr
    mov    P0,#'- '
    lcall  w_chr
    mov    P0,#'D'
    lcall  w_chr
    mov    P0,#'i'
    lcall  w_chr
    mov    P0,#'s'
    lcall  w_chr

```

```

    mov    P0,#'-
    lcall  w_chr
    mov    P0,#0D0h
    lcall  w_ins
bcek08: lcall tg_lps
    ljmp   bcdta0
;
bcdta: mov    A,Dpos
    cjne   A,#0,bcadt0
    mov     Tr00,D000
    mov     Tr01,D001
    mov     Tr02,D002
    mov     Tr10,D010
    mov     Tr11,D011
    mov     Tr12,D012
bcdt0: cjne   A,#1,bcadt1
    mov     Tr00,D100
    mov     Tr01,D101
    mov     Tr02,D102
    mov     Tr10,D110
    mov     Tr11,D111
    mov     Tr12,D112
bcdt1: cjne   A,#2,bcadt2
    mov     Tr00,D200
    mov     Tr01,D201
    mov     Tr02,D202
    mov     Tr10,D210
    mov     Tr11,D211
    mov     Tr12,D212
bcdt2: cjne   A,#3,bcadt3
    mov     Tr00,D300
    mov     Tr01,D301
    mov     Tr02,D302
    mov     Tr10,D310
    mov     Tr11,D311
    mov     Tr12,D312
bcdt3: cjne   A,#4,bcadt4
    mov     Tr00,D400
    mov     Tr01,D401
    mov     Tr02,D402
    mov     Tr10,D410
    mov     Tr11,D411
    mov     Tr12,D412
bcdt4: cjne   A,#5,bcadt5
    mov     Tr00,D500
    mov     Tr01,D501
    mov     Tr02,D502
    mov     Tr10,D510
    mov     Tr11,D511

```

```

    mov    Tr12,D512
bcadt5: cjne  A,#6,bcad6
    mov    Tr00,D600
    mov    Tr01,D601
    mov    Tr02,D602
    mov    Tr10,D610
    mov    Tr11,D611
    mov    Tr12,D612
bcadt6: cjne  A,#7,bcad7
    mov    Tr00,D700
    mov    Tr01,D701
    mov    Tr02,D702
    mov    Tr10,D710
    mov    Tr11,D711
    mov    Tr12,D712
bcadt7: cjne  A,#8,bcad8
    mov    Tr00,D800
    mov    Tr01,D801
    mov    Tr02,D802
    mov    Tr10,D810
    mov    Tr11,D811
    mov    Tr12,D812
bcadt8: cjne  A,#9,bcad9
    mov    Tr00,D900
    mov    Tr01,D901
    mov    Tr02,D902
    mov    Tr10,D910
    mov    Tr11,D911
    mov    Tr12,D912
bcadt9: ret
;procedure untuk menyimpan data
smpdta: mov    A,Dpos
    cjne  A,#0,smpdt0
    mov    D000,Tr00
    mov    D001,Tr01
    mov    D002,Tr02
    mov    D010,Tr10
    mov    D011,Tr11
    mov    D012,Tr12
smpdt0: cjne  A,#1,smpdt1
    mov    D100,Tr00
    mov    D101,Tr01
    mov    D102,Tr02
    mov    D110,Tr10
    mov    D111,Tr11
    mov    D112,Tr12
smpdt1: cjne  A,#2,smpdt2
    mov    D200,Tr00
    mov    D201,Tr01

```

```
    mov    D202,Tr02
    mov    D210,Tr10
    mov    D211,Tr11
    mov    D212,Tr12
smpdt2: cjne A,#3,smpdt3
    mov    D300,Tr00
    mov    D301,Tr01
    mov    D302,Tr02
    mov    D310,Tr10
    mov    D311,Tr11
    mov    D312,Tr12
smpdt3: cjne A,#4,smpdt4
    mov    D400,Tr00
    mov    D401,Tr01
    mov    D402,Tr02
    mov    D410,Tr10
    mov    D411,Tr11
    mov    D412,Tr12
smpdt4: cjne A,#5,smpdt5
    mov    D500,Tr00
    mov    D501,Tr01
    mov    D502,Tr02
    mov    D510,Tr10
    mov    D511,Tr11
    mov    D512,Tr12
smpdt5: cjne A,#6,smpdt6
    mov    D600,Tr00
    mov    D601,Tr01
    mov    D602,Tr02
    mov    D610,Tr10
    mov    D611,Tr11
    mov    D612,Tr12
smpdt6: cjne A,#7,smpdt7
    mov    D700,Tr00
    mov    D701,Tr01
    mov    D702,Tr02
    mov    D710,Tr10
    mov    D711,Tr11
    mov    D712,Tr12
smpdt7: cjne A,#8,smpdt8
    mov    D800,Tr00
    mov    D801,Tr01
    mov    D802,Tr02
    mov    D810,Tr10
    mov    D811,Tr11
    mov    D812,Tr12
smpdt8: cjne A,#9,smpdt9
    mov    D900,Tr00
    mov    D901,Tr01
```



```
    mov    D902,Tr02
    mov    D910,Tr10
    mov    D911,Tr11
    mov    D912,Tr12
smpdt9: ret
;procedure untuk mereset data
rsttdta: mov    D000,#0
    mov    D001,#0
    mov    D002,#0
    mov    D100,#0
    mov    D101,#0
    mov    D102,#0
    mov    D200,#0
    mov    D201,#0
    mov    D202,#0
    mov    D300,#0
    mov    D301,#0
    mov    D302,#0
    mov    D400,#0
    mov    D401,#0
    mov    D402,#0
    mov    D500,#0
    mov    D501,#0
    mov    D502,#0
    mov    D600,#0
    mov    D601,#0
    mov    D602,#0
    mov    D700,#0
    mov    D701,#0
    mov    D702,#0
    mov    D800,#0
    mov    D801,#0
    mov    D802,#0
    mov    D900,#0
    mov    D901,#0
    mov    D902,#0
    mov    D010,#0
    mov    D011,#0
    mov    D012,#0
    mov    D110,#0
    mov    D111,#0
    mov    D112,#0
    mov    D210,#0
    mov    D211,#0
    mov    D212,#0
    mov    D310,#0
    mov    D311,#0
    mov    D312,#0
    mov    D410,#0
```



```

mov D411,#0
mov D412,#0
mov D510,#0
mov D511,#0
mov D512,#0
mov D610,#0
mov D611,#0
mov D612,#0
mov D710,#0
mov D711,#0
mov D712,#0
mov D810,#0
mov D811,#0
mov D812,#0
mov D910,#0
mov D911,#0
mov D912,#0
ret

```

```
;
```

```

rmstr0: mov  A,Tr01          ;\
mov  B,#10                  ;|
mul  AB                     ;| Tr01 dikali 10
mov  B,Tr00                 ;| ditambah Tr00
add  A,B                     ;| simpan di Buf0
mov  Buf0,A                 ;/
mov  R0,Tr02                ;\
mov  R1,#000h               ;|
mov  R2,#64h                 ;|
mov  R3,#000h               ;| Tr02 dikali 100
lcall mul16                  ;| ditambah Buf0
mov  R2,Buf0                 ;| hasil simpan di Buf0 - Buf1
mov  R3,#000h               ;|
lcall add16                  ;|
mov  Buf0,R0                 ;|
mov  Buf1,R1                 ;/
mov  R0,#010h               ;\
mov  R1,#00Eh               ;|
mov  R2,Buf0                 ;|
mov  R3,Buf1                 ;| 3600 dibagi Buf0 - Buf1
lcall div16                  ;| dikali 20
mov  R2,#014h               ;|
mov  R3,#000h               ;|
lcall mul16                  ;/
mov  R2,#064h               ;\
mov  R3,#000h               ;| hasil dibagi 100
lcall div16                  ;/
mov  A,R0                    ;\
mov  B,#10                   ;| hasil dibagi 10
div  AB                      ;| hasil disimpan Dk00

```



```

        mov     Dk00,A                ;| hasil disimpan Dk01
        mov     Dk01,B                ;/
        ret

;
rmstr1: mov     A,Tr11                ;\
        mov     B,#10                 ;|
        mul     AB                     ;| Tr01 dikali 10
        mov     B,Tr10                ;| ditambah Tr00
        add     A,B                   ;| simpan di Buf0
        mov     Buf0,A                ;/
        mov     R0,Tr12               ;\
        mov     R1,#000h              ;|
        mov     R2,#64h               ;|
        mov     R3,#000h              ;| Tr02 dikali 100
        lcall   mul16                 ;| ditambah Buf0
        mov     R2,Buf0               ;| hasil simpan di Buf0 - Buf1
        mov     R3,#000h              ;|
        lcall   add16                 ;|
        mov     Buf0,R0               ;|
        mov     Buf1,R1               ;/
        mov     R0,#010h              ;\
        mov     R1,#00Eh              ;|
        mov     R2,Buf0               ;|
        mov     R3,Buf1               ;| 3600 dibagi Buf0 - Buf1
        lcall   div16                 ;| dikali 201
        mov     R2,#0C8h              ;|
        mov     R3,#000h              ;|
        lcall   mul16                 ;/
        mov     R2,#0E8h              ;\
        mov     R3,#003h              ;| hasil dibagi 1000
        lcall   div16                 ;/
        mov     A,R0                  ;\
        mov     B,#10                 ;| hasil dibagi 10
        div     AB                     ;| hasil disimpan Dk00
        mov     Dk10,A                ;| hasil disimpan Dk01
        mov     Dk11,B                ;/
        ret

;
line1: mov     P0,#080h
        lcall   w_ins
        ret

;
line2: mov     P0,#0C0h
        lcall   w_ins
        ret

;
tulis: clr     A
        movc    A,@A+DPTR
        mov     P0,A

```

```

    inc    DPTR
    lcall  w_chr
    djnz   Hurf,tulis
    ret

;
wr_chr:  movc  A,@A+DPTR
        mov   P0,A
        lcall w_chr
        ret

;
w_ins:  clr   Enbl
        clr   Rest
        setb  Enbl
        clr   Enbl
        lcall jeda
        ret

;
w_chr:  clr   Enbl
        setb  Rest
        setb  Enbl
        clr   Enbl
        lcall jeda
        ret

;
lcd_in: lcall delays
        mov   P0,#01h           ; Display Clear
        lcall w_ins
        mov   P0,#38h           ; Function Set
        lcall w_ins
        mov   P0,#0Dh           ; Display On, Cursor, Blink
        lcall w_ins
        mov   P0,#06h           ; Entry Mode
        lcall w_ins
        mov   P0,#02h           ; Cursor Home
        lcall w_ins
        lcall delays
        ret

;
tmr_in: mov   TMOD,#11h         ; timer 0 & 1 mode 16 bit
        setb  ET0
        setb  ET1
        setb  EA
        lcall delays
        ret

;scan keypad atau pengenalan tombol keypad
scnkpd: mov   R0,#10
        lcall jeda
coll:  mov   P1,#11111110b
        mov   A,P1

```

```

c1b1: cjne A,#11101110b,c1b2
      mov R0,#1
c1b2: cjne A,#11011110b,c1b3
      mov R0,#2
c1b3: cjne A,#10111110b,c1b4
      mov R0,#3
c1b4: cjne A,#01111110b,col2
      mov R0,#13
;
col2: mov P1,#11111101b
      mov A,P1
c2b1: cjne A,#11101101b,c2b2
      mov R0,#4
c2b2: cjne A,#11011101b,c2b3
      mov R0,#5
c2b3: cjne A,#10111101b,c2b4
      mov R0,#6
c2b4: cjne A,#01111101b,col3
      mov R0,#14
;
col3: mov P1,#11111011b
      mov A,P1
c3b1: cjne A,#11101011b,c3b2
      mov R0,#7
c3b2: cjne A,#11011011b,c3b3
      mov R0,#8
c3b3: cjne A,#10111011b,c3b4
      mov R0,#9
c3b4: cjne A,#01111011b,col4
      mov R0,#15
;
col4: mov P1,#11110111b
      mov A,P1
c4b1: cjne A,#11100111b,c4b2
      mov R0,#11
c4b2: cjne A,#11010111b,c4b3
      mov R0,#0
c4b3: cjne A,#10110111b,c4b4
      mov R0,#12
c4b4: cjne A,#01110111b,back
      mov R0,#16
back: ret
;waktu tunggu jika akan menekan suatu tombol dari keypad
tg_tkn: lcall scnkp
      lcall jeda
tg_tk0: cjne R0,#16,tg_tk1
      ljmp tg_tkn
tg_tk1: cjne R0,#15,tg_tk2
      ljmp tg_tkn

```



```

tg_tk2: cjne R0,#14,tg_tk3
        ljmp tg_tkn
tg_tk3: cjne R0,#13,tg_tk4
        ljmp tg_tkn
tg_tk4: cjne R0,#12,tg_tk5
        ljmp tg_tkn
tg_tk5: cjne R0,#11,tg_tk6
        ljmp tg_tkn
tg_tk6: cjne R0,#10,tg_tk7
        ljmp tg_tkn
tg_tk7: ret
; jika keypad dilepas setelah ditekan
tg_lps: lcall scnkp
        cjne R0,#10,tg_lps
        ret
;
jeda: djnz Dly0,$
      ret
;
delays: lcall scnkp
        cjne R0,#13,dlys0
        ljmp start
dlys0: cjne R0,#14,dlys1
        ljmp bc_dta
dlys1: djnz Dly1,delays
      ret
;
delayl: mov Dly2,#15
dlyl: lcall delays
      djnz Dly2,dlyl
      ret
;
delay: lcall jeda
      djnz Dly1,delay
      ret
;
delayx: mov Dly2,#10
dlyx: djnz Dly1,$
      djnz Dly0,dlyx
      djnz Dly2,dlyx
      ret
;
nama: DB ' Andri Dwi '
      DB ' NIM : 0552205 '
univ: DB ' Teknik Elka D3 '
      DB ' ITN Malang '
judul: DB ' Ukur Kecepatan '
      DB ' Kendaraan Drag '
tstrt: DB ' Start '

```

1. The first part of the report
describes the general situation
of the country and the
main problems facing it.
It also mentions the
main achievements of the
government in the past
year.
2. The second part of the report
describes the main problems
facing the country and
the government's plans to
solve them.
3. The third part of the report
describes the main achievements
of the government in the
past year.
4. The fourth part of the report
describes the main problems
facing the country and
the government's plans to
solve them.
5. The fifth part of the report
describes the main achievements
of the government in the
past year.
6. The sixth part of the report
describes the main problems
facing the country and
the government's plans to
solve them.
7. The seventh part of the report
describes the main achievements
of the government in the
past year.
8. The eighth part of the report
describes the main problems
facing the country and
the government's plans to
solve them.
9. The ninth part of the report
describes the main achievements
of the government in the
past year.
10. The tenth part of the report
describes the main problems
facing the country and
the government's plans to
solve them.

```

track: DB    'Track 1 Track 2'
cntrk: DB    '00.0s 00.0s '
savdta: DB    ' Save Data: '
svgdta: DB    ' Saving Data! '
plwait: DB    ' Plese wait ... '
recdta: DB    ' Record Data: '
kosong: DB    '          '
angka: DB    '0123456789 -DIS '

```

```

;
add16: anl    PSW,#0E7h
        mov    A,R0
        add    A,R2
        mov    R0,A
        mov    A,R1
        addc   A,R3
        mov    R1,A
        mov    C,OV
        ret

```

```

;
sub16: anl    PSW,#0E7h
        mov    A,R0
        clr    C
        subb   A,R2
        mov    R0,A
        mov    A,R1
        subb   A,R3
        mov    R1,A
        mov    C,OV
        ret

```

```

;
mul16: anl    PSW,#0E7h
        lcall  cr0r1
        lcall  cr2r3
        lcall  umul16
        lcall  mr0r3
        ret

```

```

;
umul16: push   B
        push   DPL
        mov    A,R0
        mov    B,R2
        mul    AB
        push   Acc
        push   B
        mov    A,R0
        mov    B,R3
        mul    AB
        pop    00h
        add    A,R0

```

```

    mov    R0,A
    clr    A
    addc   A,B
    mov    DPL,A
    mov    A,R2
    mov    B,R1
    mul    AB
    add    A,R0
    mov    R0,A
    mov    A,DPL
    addc   A,B
    mov    DPL,A
    clr    A
    addc   A,#0
    push   Acc
    mov    A,R3
    mov    B,R1
    mul    AB
    add    A,DPL
    mov    R2,A
    pop    Acc
    addc   A,B
    mov    R3,A
    mov    R1,00h
    pop    00h
    pop    DPL
    pop    B
    ret

;
div16: anl    PSW,#0E7h
    mov    A,R3
    orl    A,R2
    jnz    divok
    setb   C
    ret

;
divok: push   DPL
    push   DPH
    push   B
    lcall  cr0r1
    lcall  cr2r3
    lcall  udiv16
    lcall  mr0r1
    clr    C
    pop    B
    pop    DPH
    pop    DPL
    ret
;

```

```

udiv16: mov    R7,#0
        mov    R6,#0
        mov    B,#16
;
divlop: clr    C
        mov    A,R0
        rlc    A
        mov    R0,A
        mov    A,R1
        rlc    A
        mov    R1,A
        mov    A,R6
        rlc    A
        mov    R6,A
        mov    A,R7
        rlc    A
        mov    R7,A
        mov    A,R6
        clr    C
        subb   A,R2
        mov    DPL,A
        mov    A,R7
        subb   A,R3
        mov    DPH,A
        cpl    C
        jnc    div_1
        mov    R7,DPH
        mov    R6,DPL
;
div_1:  mov    A,R4
        rlc    A
        mov    R4,A
        mov    A,R5
        rlc    A
        mov    R5,A
        djnz   B,divlop
        mov    A,R5
        mov    R1,A
        mov    A,R4
        mov    R0,A
        mov    A,R7
        mov    R3,A
        mov    A,R6
        mov    R2,A
        ret
;
mr0r1: jb     21h,mr0r1b
        jb     22h,mr0r1a
        ret

```

```
;
mr0r1b: jnb  22h,mr0r1a
        ret
```

```
;
mr0r1a: mov  A,R0
        cpl  A
        add  A,#1
        mov  R0,A
        mov  A,R1
        cpl  A
        addc A,#0
        mov  R1,A
        ret
```

```
;
mr0r3:  jb   21h,mr0r3b
        jb   22h,mr0r3a
        ret
```

```
;
mr0r3b: jnb  22h,mr0r3a
        ret
```

```
;
mr0r3a: mov  A,R0
        cpl  A
        add  A,#1
        mov  R0,A
        mov  A,R1
        cpl  A
        addc A,#0
        mov  R1,A
        mov  A,R2
        cpl  A
        addc A,#0
        mov  R2,A
        mov  A,R3
        cpl  A
        addc A,#0
        mov  R3,A
        ret
```

```
;
cr2r3:  mov  A,R3
        jb   Acc.7,c1a
        clr  22h
        ret
```

```
;
c1a:    setb 22h
        mov  A,R2
        cpl  A
        add  A,#1
        mov  R2,A
```

```
    mov    A,R3
    cpl    A
    addc   A,#0
    mov    R3,A
    ret
;
cr0r1: mov    A,R1
      jb     Acc.7,c0a
      clr    21h
      ret
;
c0a:  setb    21h
      mov    A,R0
      cpl    A
      add    A,#1
      mov    R0,A
      mov    A,R1
      cpl    A
      addc   A,#0
      mov    R1,A
      ret
;
end
```

Lampiran : 1(satu) berkas Proposal

Perihal : Permohonan Kesediaan Dosen Pembimbing

Kepada : Yth. Bapak/Ibu. Bambang Prio Hartono,ST,MT
Institut Teknologi Nasional Malang
di
M a l a n g

Dengan hormat,

Kami yang bertanda tangan dibawah ini :

N a m a : Andri Dwi Arianto

No. Mahasiswa : 0552205

Program Studi : Teknik Elektro D-III

Dengan ini mengajukan permohonan, sekiranya Bapak/Ibu bersedia menjadi Dosen Pembimbing, untuk penyusunan Tugas Akhir .

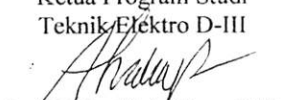
Judul Tugas Akhir : ..Perancangan dan Pembuatan Alat Penghitung Waktu Tempuh dan
..Kecepatan pada Perlombaan Drag Race.....

Adapun tugas tersebut adalah salah satu syarat untuk menempuh Ujian Tugas Akhir Program D-III.

Demikian permohonan kami dan atas kesediaan Bapak/Ibu kami ucapkan terima kasih.

Mengetahui

Ketua Program Studi
Teknik Elektro D-III


Ir. H. Taufik Hidayat, MT
NIP.Y. 1018700151

Malang, 25 Pebruari 2009



____Andri Dwi Arianto____

KESEDIAAN PEMBIMBING TUGAS AKHIR

Sesuai permohonan dari mahasiswa :

N a m a : Andri Dwi Arianto
No. Mahasiswa : 0552205
Program Studi : Teknik Elektro D-III
Judul Tugas Akhir : Perancangan dan Pembuatan Alat Penghitung Waktu Tempuh dan
Kecepatan pada Perlombaan Drag Race.....
.....
.....

Bahwa kami bersedia membimbing Tugas Akhir dari mahasiswa tersebut.

Jangka waktu penyelesaian Tugas Akhir selama 4 (empat) bulan mulai tanggal
10/02/2009 s/d 10/06/2009 dan apabila dalam jangka waktu tersebut belum selesai maka tugas akhir
tersebut dinyatakan **GUGUR**

Malang, 25 Pebruari 2009

Dosen Pembimbing;



Bambang Prio Hartono,ST,MT

NIP. 1028700172

Nb :

Setelah disetujui agar formulir ini diserahkan Mahasiswa
yang bersangkutan kepada sekretaris jurusan Teknik
Elektro D-III



(PERSERO) MALANG
K NIAGA MALANG

YAYASAN PENDIDIKAN UMUM DAN TEKNOLOGI NASIONAL
INSTITUT TEKNOLOGI NASIONAL MALANG

FAKULTAS TEKNOLOGI INDUSTRI
FAKULTAS TEKNIK SIPIL DAN PERENCANAAN
PROGRAM PASCASARJANA MAGISTER TEKNIK

KAMPUS : Jl. Bendungan Sigura-gura No. 2 Telp. (0341) 551431(Hunting) Fax. (0341) 553015 Malang 65145

UT - 3

Nomor : 112/EL-09/TA/2009
Lampiran : -
Perihal : Bimbingan Tugas Akhir

Kepada : Yth. Bambang Prio Hartono,ST,MT
Dosen Institut Teknologi Nasional
Malang

Dengan Hormat,

Sesuai dengan permohonan persetujuan dalam Tugas Akhir untuk mahasiswa:

N a m a : Andri Dwi Arianto
No. Mahasiswa : 0552205
Program Studi : Teknik Elektro D-III
Judul Tesis : Perancangan dan Pembuatan Alat Penghitung Waktu Tempuh dan
Kecepatan pada Perlombaan Drag Race

Maka dengan ini pembimbingan Tugas Akhir tersebut kami serahkan sepenuhnya kepada saudara, terhitung mulai tanggal 10/02/2009 s/d 10/06/2009

Demikian agar maklum dan atas perhatian serta bantuannya kami ucapkan terima kasih.

Malang, 25 Pebruari 2009
Ketua Program Studi
Teknik Elektro D-III

Ir. H. Taufik Hidayat,MT

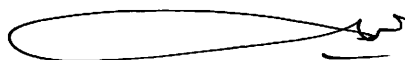
NIP. 1018700151

LEMBAR ASISTENSI

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 Jurusan : Teknik Elektronika D III
 Dosen Pembimbing : Bambang Prio H, ST. MT
 Judul Tugas Akhir : " Perancangan dan Pembuatan Alat Penghitung Waktu
 Tempuh dan Kecepatan Pada Perlombaan Drag Race "

No.	Hari/Tanggal	Materi Konsultasi	Paraf
1.	14-02-2009	Judul TA; Abstrak; Bab I	
2.	17-02-2009	Bab II sampai Bab V	
3.	19-02-2009	Daftar pustaka dan Lampiran	
4.	23-02-2009	Acc Judul; Abstrak	
5.	26-02-2009	Acc Bab I, Bab II	
6.	05-03-2009	Acc Bab III	
7.	10-03-2009	Acc Bab IV	
8.	11-03-2009	Acc Bab V	
9.	14-03-2009	Acc Daftar pustaka dan Lampiran	

Menyetujui
 Dosen Pembimbing



(BAMBANG PRIO H, ST. MT)

LEMBAR PERBAIKAN TUGAS AKHIR

NAMA : ANDRI DWI ARIANTO

NIM : 05.52.205

JURUSAN : TEKNIK ELEKTRO D – III

**JUDUL TA : PERANCANGAN DAN PEMBUATAN ALAT PENGHITUNG WAKTU
TEMPUH DAN KECEPATAN PADA PERLOMBAAN DRAG RACE.**

HARI, TANGGAL : SELASA, 24 MARET 2009

No.	Materi Perbaikan	Paraf
1.	Bab II ditambahkan photodiode dan diode	
2.	Pengujian ditambahkan dicari error	
3.	Kesimpulan diambil dari Bab IV dari sana dilihat tujuan tercapai tidaknya	
4.	Perancangan sensor diganti, disesuaikan dengan alat lalu dijelaskan	
5.	Perancangan disesuaikan dengan alat	

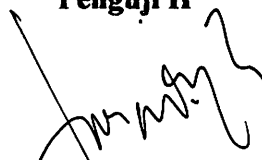
Telah Diperiksa / Disetujui :

Penguji I



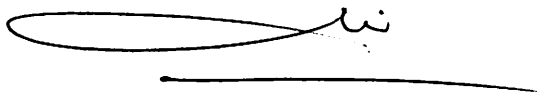
I Komang Somawirata, ST, MT
NIP. P 103 0100 361

Penguji II



Irmalia Suryani, F, ST, MT
NIP. P 103 0100 365

Dosen Pembimbing



Bambang Prio H, ST, MT
NIP. Y 102 8400 082

BERITA ACARA UJIAN TUGAS AKHIR
FAKULTAS TEKNOLOGI INDUSTRI

NAMA : ANDRI DWI ARIANTO
NIM : 05.52.205
JURUSAN : TEKNIK ELEKTRO D-III
JUDUL SKRIPSI : PERANCANGAN DAN PEMBUATAN ALAT
PENGHITUNG WAKTU TEMPUH DAN
KECEPATAN PADA PERLOMBAAN DRAG RACE.

Dipertahankan di hadapan Tim Penguji Tugas Akhir Jenjang Program Diploma Tiga
(D-III) Pada :

HarilTanggal : Selasa, 24 Maret 2009

Dengan Nilai : 78,25 (B+) *10*

Panitia Ujian Tugas Akhir



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Sekretaris

A blue ink signature of Ir. H. Taufik Hidayat, MT, written in a cursive style.

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Anggota Penguji

Penguji I

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Penguji II

A blue ink signature of Irmalia Suryani, F, ST, MT, written in a cursive style.

Irmalia Suryani, F, ST, MT
NIP. P 103 0100 365

Features

- Compatible with MCS-51® Products
- 4K Bytes of In-System Programmable (ISP) Flash Memory
 - Endurance: 1000 Write/Erase Cycles
- 0V to 5.5V Operating Range
- Fully Static Operation: 0 Hz to 33 MHz
- Three-level Program Memory Lock
- 128 x 8-bit Internal RAM
- 32 Programmable I/O Lines
- Two 16-bit Timer/Counters
- Six Interrupt Sources
- Full Duplex UART Serial Channel
- Low-power Idle and Power-down Modes
- Interrupt Recovery from Power-down Mode
- Watchdog Timer
- Two Data Pointers
- Power-off Flag
- Fast Programming Time
- Flexible ISP Programming (Byte and Page Mode)

Description

The AT89S51 is a low-power, high-performance CMOS 8-bit microcontroller with 4K bytes of in-system programmable Flash memory. The device is manufactured using Atmel's high-density nonvolatile memory technology and is compatible with the industry-standard 80C51 instruction set and pinout. The on-chip Flash allows the program memory to be reprogrammed in-system or by a conventional nonvolatile memory programmer. By combining a versatile 8-bit CPU with in-system programmable Flash on a monolithic chip, the Atmel AT89S51 is a powerful microcontroller which provides a highly-flexible and cost-effective solution to many embedded control applications.

The AT89S51 provides the following standard features: 4K bytes of Flash, 128 bytes of internal RAM, 32 I/O lines, Watchdog timer, two data pointers, two 16-bit timer/counters, a five-vector two-level interrupt architecture, a full duplex serial port, on-chip oscillator, and clock circuitry. In addition, the AT89S51 is designed with static logic for operation down to zero frequency and supports two software selectable power saving modes. The Idle Mode stops the CPU while allowing the RAM, timer/counters, serial port, and interrupt system to continue functioning. The Power-down mode saves the RAM contents but freezes the oscillator, disabling all other chip functions until the next external interrupt or hardware reset.



8-bit Microcontroller with 4K Bytes In-System Programmable Flash

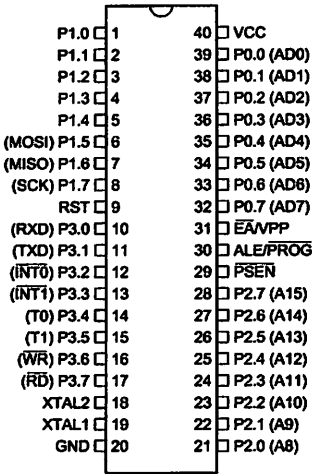
AT89S51

Rev. 2487A-10/01

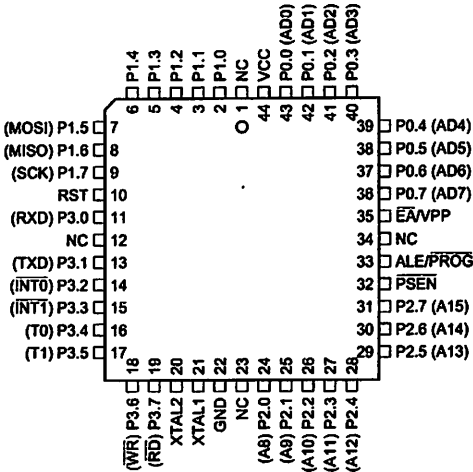


Configurations

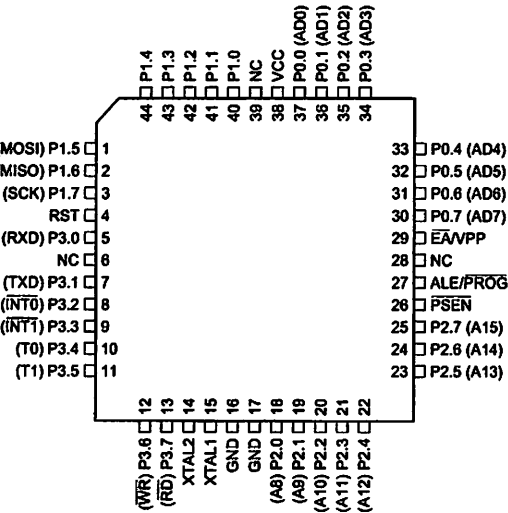
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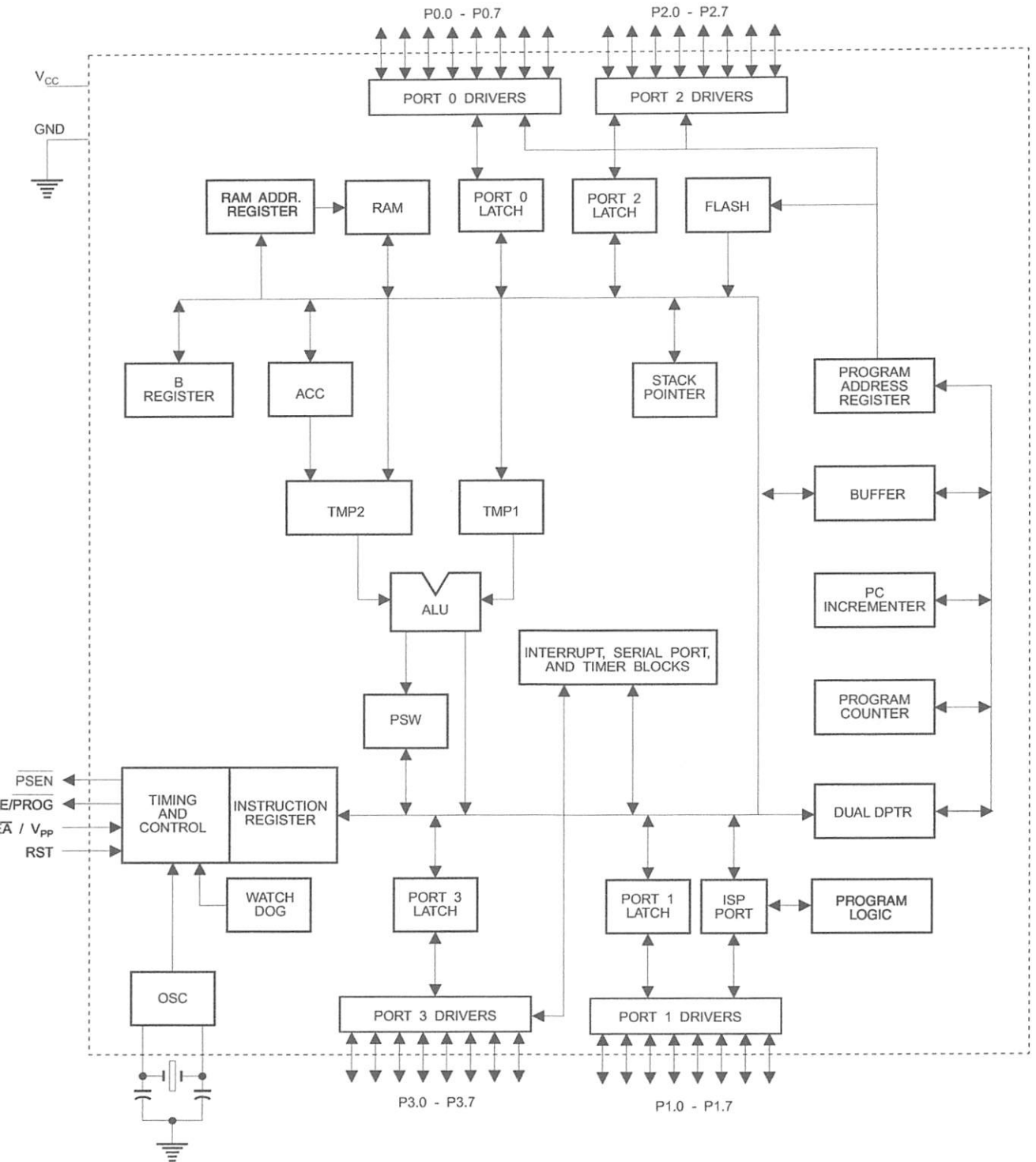
PLCC



TQFP



Block Diagram





Description

C

Supply voltage.

D

Ground.

Port 0

Port 0 is an 8-bit open drain bidirectional I/O port. As an output port, each pin can sink eight TTL inputs. When 1s are written to port 0 pins, the pins can be used as high-impedance inputs.

Port 0 can also be configured to be the multiplexed low-order address/data bus during accesses to external program and data memory. In this mode, P0 has internal pull-ups.

Port 0 also receives the code bytes during Flash programming and outputs the code bytes during program verification. **External pull-ups are required during program verification.**

Port 1

Port 1 is an 8-bit bidirectional I/O port with internal pull-ups. The Port 1 output buffers can sink/source four TTL inputs. When 1s are written to Port 1 pins, they are pulled high by the internal pull-ups and can be used as inputs. As inputs, Port 1 pins that are externally being pulled low will source current (I_{IL}) because of the internal pull-ups.

Port 1 also receives the low-order address bytes during Flash programming and verification.

Port Pin	Alternate Functions
P1.5	MOSI (used for In-System Programming)
P1.6	MISO (used for In-System Programming)
P1.7	SCK (used for In-System Programming)

Port 2

Port 2 is an 8-bit bidirectional I/O port with internal pull-ups. The Port 2 output buffers can sink/source four TTL inputs. When 1s are written to Port 2 pins, they are pulled high by the internal pull-ups and can be used as inputs. As inputs, Port 2 pins that are externally being pulled low will source current (I_{IL}) because of the internal pull-ups.

Port 2 emits the high-order address byte during fetches from external program memory and during accesses to external data memory that use 16-bit addresses (MOVX @ DPTR). In this application, Port 2 uses strong internal pull-ups when emitting 1s. During accesses to external data memory that use 8-bit addresses (MOVX @ RI), Port 2 emits the contents of the P2 Special Function Register.

Port 2 also receives the high-order address bits and some control signals during Flash programming and verification.

Port 3

Port 3 is an 8-bit bidirectional I/O port with internal pull-ups. The Port 3 output buffers can sink/source four TTL inputs. When 1s are written to Port 3 pins, they are pulled high by the internal pull-ups and can be used as inputs. As inputs, Port 3 pins that are externally being pulled low will source current (I_{IL}) because of the pull-ups.

Port 3 receives some control signals for Flash programming and verification.

Port 3 also serves the functions of various special features of the AT89S51, as shown in the following table.

Port Pin	Alternate Functions
P3.0	RXD (serial input port)
P3.1	TXD (serial output port)
P3.2	$\overline{\text{INT0}}$ (external interrupt 0)
P3.3	$\overline{\text{INT1}}$ (external interrupt 1)
P3.4	T0 (timer 0 external input)
P3.5	T1 (timer 1 external input)
P3.6	$\overline{\text{WR}}$ (external data memory write strobe)
P3.7	$\overline{\text{RD}}$ (external data memory read strobe)

Reset input. A high on this pin for two machine cycles while the oscillator is running resets the device. This pin drives High for 98 oscillator periods after the Watchdog times out. The DISRTO bit in SFR AUXR (address 8EH) can be used to disable this feature. In the default state of bit DISRTO, the RESET HIGH out feature is enabled.

Address Latch Enable (ALE) is an output pulse for latching the low byte of the address during accesses to external memory. This pin is also the program pulse input ($\overline{\text{PROG}}$) during Flash programming.

In normal operation, ALE is emitted at a constant rate of 1/6 the oscillator frequency and may be used for external timing or clocking purposes. Note, however, that one ALE pulse is skipped during each access to external data memory.

If desired, ALE operation can be disabled by setting bit 0 of SFR location 8EH. With the bit set, ALE is active only during a MOVX or MOVC instruction. Otherwise, the pin is weakly pulled high. Setting the ALE-disable bit has no effect if the microcontroller is in external execution mode.

Program Store Enable ($\overline{\text{PSEN}}$) is the read strobe to external program memory.

When the AT89S51 is executing code from external program memory, $\overline{\text{PSEN}}$ is activated twice each machine cycle, except that two $\overline{\text{PSEN}}$ activations are skipped during each access to external data memory.

External Access Enable. $\overline{\text{EA}}$ must be strapped to GND in order to enable the device to fetch code from external program memory locations starting at 0000H up to FFFFH. Note, however, that if lock bit 1 is programmed, $\overline{\text{EA}}$ will be internally latched on reset.

$\overline{\text{EA}}$ should be strapped to V_{CC} for internal program executions.

This pin also receives the 12-volt programming enable voltage (V_{PP}) during Flash programming.

Input to the inverting oscillator amplifier and input to the internal clock operating circuit.

Output from the inverting oscillator amplifier





Special
Function
Registers

A map of the on-chip memory area called the Special Function Register (SFR) space is shown in Table 1.

Note that not all of the addresses are occupied, and unoccupied addresses may not be implemented on the chip. Read accesses to these addresses will in general return random data, and write accesses will have an indeterminate effect.

Table 1. AT89S51 SFR Map and Reset Values

00H								0FFH
01H	B 00000000							0F7H
02H								0EFH
03H	ACC 00000000							0E7H
04H								0DFH
05H	PSW 00000000							0D7H
06H								0CFH
07H								0C7H
08H	IP XX000000							0BFH
09H	P3 11111111							0B7H
0AH	IE 0X000000							0AFH
0BH	P2 11111111		AUXR1 XXXXXX0				WDRST XXXXXXX	0A7H
0CH	SCON 00000000	SBUF XXXXXXXX						9FH
0DH	P1 11111111							97H
0EH	TCON 00000000	TMOD 00000000	TL0 00000000	TL1 00000000	TH0 00000000	TH1 00000000	AUXR XXX00XX0	8FH
0FH	P0 11111111	SP 00000111	DP0L 00000000	DP0H 00000000	DP1L 00000000	DP1H 00000000		PCON 0XXX0000 87H

User software should not write 1s to these unlisted locations, since they may be used in future products to invoke new features. In that case, the reset or inactive values of the new bits will always be 0.

Interrupt Registers: The individual interrupt enable bits are in the IE register. Two priorities can be set for each of the five interrupt sources in the IP register.

Table 2. AUXR: Auxiliary Register

AUXR		Address = 8EH				Reset Value = XXX00XX0B		
Not Bit Addressable								
Bit	7	6	5	4	3	2	1	0
	-	-	-	WDIDLE	DISRTO	-	-	DISALE
-	Reserved for future expansion							
DISALE	Disable/Enable ALE							
	DISALE							
	Operating Mode							
0	ALE is emitted at a constant rate of 1/6 the oscillator frequency							
1	ALE is active only during a MOVX or MOVC instruction							
DISRTO	Disable/Enable Reset out							
	DISRTO							
0	Reset pin is driven High after WDT times out							
1	Reset pin is input only							
WDIDLE	Disable/Enable WDT in IDLE mode							
WDIDLE								
0	WDT continues to count in IDLE mode							
1	WDT halts counting in IDLE mode							

Dual Data Pointer Registers: To facilitate accessing both internal and external data memory, two banks of 16-bit Data Pointer Registers are provided: DP0 at SFR address locations 82H-83H and DP1 at 84H-85H. Bit DPS = 0 in SFR AUXR1 selects DP0 and DPS = 1 selects DP1. The user should always initialize the DPS bit to the appropriate value before accessing the respective Data Pointer Register.





Power Off Flag: The Power Off Flag (POF) is located at bit 4 (PCON.4) in the PCON SFR. POF is set to “1” during power up. It can be set and rest under software control and is not affected by reset.

Table 3. AUXR1: Auxiliary Register 1

AUXR1

Address = A2H

Reset Value = XXXXXX0B

Not Bit
Addressable

Bit	7	6	5	4	3	2	1	DPS
	–	–	–	–	–	–	–	

– Reserved for future expansion

DPS Data Pointer Register Select

DPS

0 Selects DPTR Registers DP0L, DP0H

1 Selects DPTR Registers DP1L, DP1H

Memory organization

MCS-51 devices have a separate address space for Program and Data Memory. Up to 64K bytes each of external Program and Data Memory can be addressed.

Program Memory

If the $\overline{EA}$ pin is connected to GND, all program fetches are directed to external memory. On the AT89S51, if $\overline{EA}$ is connected to V_{CC} , program fetches to addresses 0000H through FFFH are directed to internal memory and fetches to addresses 1000H through FFFFH are directed to external memory.

Data Memory

The AT89S51 implements 128 bytes of on-chip RAM. The 128 bytes are accessible via direct and indirect addressing modes. Stack operations are examples of indirect addressing, so the 128 bytes of data RAM are available as stack space.

Watchdog timer enabled with reset-out)

The WDT is intended as a recovery method in situations where the CPU may be subjected to software upsets. The WDT consists of a 14-bit counter and the Watchdog Timer Reset (WDTRST) SFR. The WDT is defaulted to disable from exiting reset. To enable the WDT, a user must write 01EH and 0E1H in sequence to the WDTRST register (SFR location 0A6H). When the WDT is enabled, it will increment every machine cycle while the oscillator is running. The WDT timeout period is dependent on the external clock frequency. There is no way to disable the WDT except through reset (either hardware reset or WDT overflow reset). When WDT overflows, it will drive an output RESET HIGH pulse at the RST pin.

Using the WDT

To enable the WDT, a user must write 01EH and 0E1H in sequence to the WDTRST register (SFR location 0A6H). When the WDT is enabled, the user needs to service it by writing 01EH and 0E1H to WDTRST to avoid a WDT overflow. The 14-bit counter overflows when it reaches 16383 (3FFFH), and this will reset the device. When the WDT is enabled, it will increment every machine cycle while the oscillator is running. This means the user must reset the WDT at least every 16383 machine cycles. To reset the WDT the user must write 01EH and 0E1H to WDTRST. WDTRST is a write-only register. The WDT counter cannot be read or written. When WDT overflows, it will generate an output RESET pulse at the RST pin. The RESET pulse duration is 98xTOSC, where TOSC=1/FOSC. To make the best use of the WDT, it

should be serviced in those sections of code that will periodically be executed within the time required to prevent a WDT reset.

WDT During Power-down and Idle

In Power-down mode the oscillator stops, which means the WDT also stops. While in Power-down mode, the user does not need to service the WDT. There are two methods of exiting Power-down mode: by a hardware reset or via a level-activated external interrupt, which is enabled prior to entering Power-down mode. When Power-down is exited with hardware reset, servicing the WDT should occur as it normally does whenever the AT89S51 is reset. Exiting Power-down with an interrupt is significantly different. The interrupt is held low long enough for the oscillator to stabilize. When the interrupt is brought high, the interrupt is serviced. To prevent the WDT from resetting the device while the interrupt pin is held low, the WDT is not started until the interrupt is pulled high. It is suggested that the WDT be reset during the interrupt service for the interrupt used to exit Power-down mode.

To ensure that the WDT does not overflow within a few states of exiting Power-down, it is best to reset the WDT just before entering Power-down mode.

Before going into the IDLE mode, the WDIDLE bit in SFR AUXR is used to determine whether the WDT continues to count if enabled. The WDT keeps counting during IDLE (WDIDLE bit = 0) as the default state. To prevent the WDT from resetting the AT89S51 while in IDLE mode, the user should always set up a timer that will periodically exit IDLE, service the WDT, and reenter IDLE mode.

With WDIDLE bit enabled, the WDT will stop to count in IDLE mode and resumes the count upon exit from IDLE.

UART

The UART in the AT89S51 operates the same way as the UART in the AT89C51. For further information on the UART operation, refer to the ATMEL Web site (<http://www.atmel.com>). From the home page, select 'Products', then '8051-Architecture Flash Microcontroller', then 'Product Overview'.

Timer 0 and 1

Timer 0 and Timer 1 in the AT89S51 operate the same way as Timer 0 and Timer 1 in the AT89C51. For further information on the timers' operation, refer to the ATMEL Web site (<http://www.atmel.com>). From the home page, select 'Products', then '8051-Architecture Flash Microcontroller', then 'Product Overview'.

Interrupts

The AT89S51 has a total of five interrupt vectors: two external interrupts ($\overline{INT0}$ and $\overline{INT1}$), two timer interrupts (Timers 0 and 1), and the serial port interrupt. These interrupts are all shown in Figure 1.

Each of these interrupt sources can be individually enabled or disabled by setting or clearing a bit in Special Function Register IE. IE also contains a global disable bit, EA, which disables all interrupts at once.

Note that Table 4 shows that bit position IE.6 is unimplemented. In the AT89S51, bit position IE.5 is also unimplemented. User software should not write 1s to these bit positions, since they may be used in future AT89 products.

The Timer 0 and Timer 1 flags, TF0 and TF1, are set at S5P2 of the cycle in which the timers overflow. The values are then polled by the circuitry in the next cycle



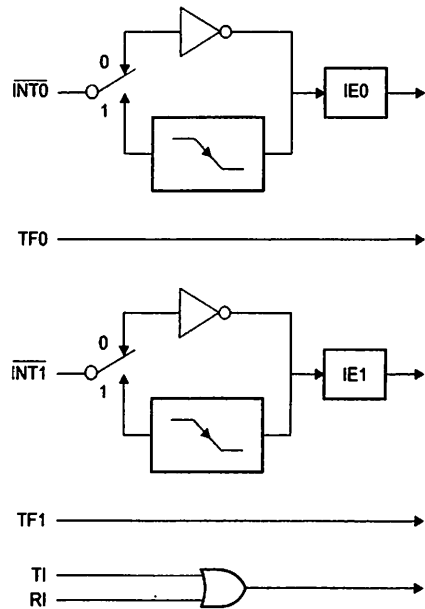
Table 4. Interrupt Enable (IE) Register

(MSB)				(LSB)			
EA	—	—	ES	ET1	EX1	ET0	EX0
Enable Bit = 1 enables the interrupt.							
Enable Bit = 0 disables the interrupt.							

Symbol	Position	Function
EA	IE.7	Disables all interrupts. If EA = 0, no interrupt is acknowledged. If EA = 1, each interrupt source is individually enabled or disabled by setting or clearing its enable bit.
—	IE.6	Reserved
—	IE.5	Reserved
ES	IE.4	Serial Port interrupt enable bit
ET1	IE.3	Timer 1 interrupt enable bit
EX1	IE.2	External interrupt 1 enable bit
ET0	IE.1	Timer 0 interrupt enable bit
EX0	IE.0	External interrupt 0 enable bit

User software should never write 1s to reserved bits, because they may be used in future AT89 products.

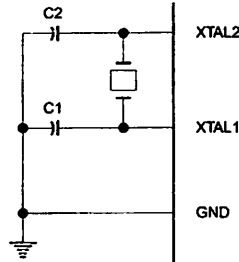
Figure 1. Interrupt Sources



Oscillator Characteristics

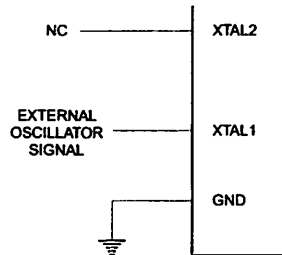
XTAL1 and XTAL2 are the input and output, respectively, of an inverting amplifier that can be configured for use as an on-chip oscillator, as shown in Figure 2. Either a quartz crystal or ceramic resonator may be used. To drive the device from an external clock source, XTAL2 should be left unconnected while XTAL1 is driven, as shown in Figure 3. There are no requirements on the duty cycle of the external clock signal, since the input to the internal clocking circuitry is through a divide-by-two flip-flop, but minimum and maximum voltage high and low time specifications must be observed.

Figure 2. Oscillator Connections



Note: C1, C2 = 30 pF $\pm$ 10 pF for Crystals = 40 pF $\pm$ 10 pF for Ceramic Resonators

Figure 3. External Clock Drive Configuration



Idle Mode

In idle mode, the CPU puts itself to sleep while all the on-chip peripherals remain active. The mode is invoked by software. The content of the on-chip RAM and all the special function registers remain unchanged during this mode. The idle mode can be terminated by any enabled interrupt or by a hardware reset.

Note that when idle mode is terminated by a hardware reset, the device normally resumes program execution from where it left off, up to two machine cycles before the internal reset algorithm takes control. On-chip hardware inhibits access to internal RAM in this event, but access to the port pins is not inhibited. To eliminate the possibility of an unexpected write to a port pin when idle mode is terminated by a reset, the instruction following the one that invokes idle mode should not write to a port pin or to external memory.

Power-down Mode

In the Power-down mode, the oscillator is stopped, and the instruction that invokes Power-down is the last instruction executed. The on-chip RAM and Special Function Registers retain their values until the Power-down mode is terminated. Exit from Power-down mode can be initiated either by a hardware reset or by activation of an enabled external interrupt into $\overline{\text{INT0}}$ or $\overline{\text{INT1}}$. Reset redefines the SFRs but does not change the on-chip RAM. The reset should not be activated before V_{CC} is restored to its normal operating level and must be held active long enough to allow the oscillator to restart and stabilize.



Table 5. Status of External Pins During Idle and Power-down Modes

Mode	Program Memory	ALE	$\overline{\text{PSEN}}$	PORT0	PORT1	PORT2	PORT3
Idle	Internal	1	1	Data	Data	Data	Data
Idle	External	1	1	Float	Data	Address	Data
Power-down	Internal	0	0	Data	Data	Data	Data
Power-down	External	0	0	Float	Data	Data	Data

The AT89S51 has three lock bits that can be left unprogrammed (U) or can be programmed (P) to obtain the additional features listed in the following table.

Table 6. Lock Bit Protection Modes

Program Lock Bits				Protection Type
	LB1	LB2	LB3	
1	U	U	U	No program lock features
2	P	U	U	MOVC instructions executed from external program memory are disabled from fetching code bytes from internal memory, $\overline{\text{EA}}$ is sampled and latched on reset, and further programming of the Flash memory is disabled
3	P	P	U	Same as mode 2, but verify is also disabled
4	P	P	P	Same as mode 3, but external execution is also disabled

When lock bit 1 is programmed, the logic level at the $\overline{\text{EA}}$ pin is sampled and latched during reset. If the device is powered up without a reset, the latch initializes to a random value and holds that value until reset is activated. The latched value of $\overline{\text{EA}}$ must agree with the current logic level at that pin in order for the device to function properly.

The AT89S51 is shipped with the on-chip Flash memory array ready to be programmed. The programming interface needs a high-voltage (12-volt) program enable signal and is compatible with conventional third-party Flash or EPROM programmers.

The AT89S51 code memory array is programmed byte-by-byte.

Programming Algorithm: Before programming the AT89S51, the address, data, and control signals should be set up according to the Flash programming mode table and Figures 13 and 14. To program the AT89S51, take the following steps:

1. Input the desired memory location on the address lines.
2. Input the appropriate data byte on the data lines.
3. Activate the correct combination of control signals.
4. Raise $\overline{\text{EA}}/\text{V}_{\text{PP}}$ to 12V.
5. Pulse $\text{ALE}/\overline{\text{PROG}}$ once to program a byte in the Flash array or the lock bits. The byte-write cycle is self-timed and typically takes no more than 50 μs . Repeat steps 1 through 5, changing the address and data for the entire array or until the end of the object file is reached.

Data Polling: The AT89S51 features Data Polling to indicate the end of a byte write cycle. During a write cycle, an attempted read of the last byte written will result in the complement of the written data on P0.7. Once the write cycle has been completed, true data is valid on all outputs, and the next cycle may begin. Data Polling may begin any time after a write cycle has been initiated.

Ready/Busy: The progress of byte programming can also be monitored by the RDY/BSY output signal. P3.0 is pulled low after ALE goes high during programming to indicate BUSY. P3.0 is pulled high again when programming is done to indicate READY.

Program Verify: If lock bits LB1 and LB2 have not been programmed, the programmed code data can be read back via the address and data lines for verification. The status of the individual lock bits can be verified directly by reading them back.

Reading the Signature Bytes: The signature bytes are read by the same procedure as a normal verification of locations 000H, 100H, and 200H, except that P3.6 and P3.7 must be pulled to a logic low. The values returned are as follows.

(000H) = 1EH indicates manufactured by Atmel
(100H) = 51H indicates 89S51
(200H) = 06H

Chip Erase: In the parallel programming mode, a chip erase operation is initiated by using the proper combination of control signals and by pulsing ALE/PROG low for a duration of 200 ns - 500 ns.

In the serial programming mode, a chip erase operation is initiated by issuing the Chip Erase instruction. In this mode, chip erase is self-timed and takes about 500 ms.

During chip erase, a serial read from any address location will return 00H at the data output.

Programming Flash – Serial Mode

The Code memory array can be programmed using the serial ISP interface while RST is pulled to V_{CC}. The serial interface consists of pins SCK, MOSI (input) and MISO (output). After RST is set high, the Programming Enable instruction needs to be executed first before other operations can be executed. Before a reprogramming sequence can occur, a Chip Erase operation is required.

The Chip Erase operation turns the content of every memory location in the Code array into FFH.

Either an external system clock can be supplied at pin XTAL1 or a crystal needs to be connected across pins XTAL1 and XTAL2. The maximum serial clock (SCK) frequency should be less than 1/16 of the crystal frequency. With a 33 MHz oscillator clock, the maximum SCK frequency is 2 MHz.

Serial Programming Algorithm

To program and verify the AT89S51 in the serial programming mode, the following sequence is recommended:

1. Power-up sequence:
Apply power between VCC and GND pins.
Set RST pin to "H".
If a crystal is not connected across pins XTAL1 and XTAL2, apply a 3 MHz to 33 MHz clock to XTAL1 pin and wait for at least 10 milliseconds.
2. Enable serial programming by sending the Programming Enable serial instruction to pin MOSI/P1.5. The frequency of the shift clock supplied at pin SCK/P1.7 needs to be less than the CPU clock at XTAL1 divided by 16.
3. The Code array is programmed one byte at a time in either the Byte or Page mode. The write cycle is self-timed and typically takes less than 0.5 ms at 5V.
4. Any memory location can be verified by using the Read instruction that returns the content at the selected address at serial output MISO/P1.6.
5. At the end of a programming session, RST can be set low to commence normal device operation.



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$$\begin{aligned} \text{formulę } q_1 \text{ wyrażającą stan: } \text{pewność} \text{ H21} = (\text{H21})_1 \\ \text{H2155 oznaczałom H12} = (\text{H12})_1 \\ \text{H125} = (\text{H12})_1 \end{aligned}$$

En el primer y segundo alínea de la sentencia se afirma que el demandado no es responsable de los daños causados por el accidente, lo que resulta contrario a lo establecido en el artículo 1.155 del Código de Comercio, que establece que el propietario de un vehículo es responsable de los daños causados por el mismo, a menos que demuestre que el accidente fue causado por un tercero. En consecuencia, la sentencia es contraria a lo establecido en el artículo 1.155 del Código de Comercio.

and 1992 would have been higher if more data had been available.

highly also act as H₂O molecule receptor, which has been taken as basis into account

[illegible]

HSE

and 100% of our respondents reported that they had experienced at least one of the following symptoms: fatigue, difficulty concentrating, and/or difficulty sleeping. The most common symptom was fatigue, reported by 80% of respondents. The second most common symptom was difficulty concentrating, reported by 60% of respondents. The third most common symptom was difficulty sleeping, reported by 40% of respondents.

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[illegible]

ANAL. Calcd for $C_{10}H_{12}O$: C, 88.10%; H, 11.90%. Found: C, 88.1%; H, 11.9%. IR (KBr): 3400 (broad), 1640 (strong), 1600 (strong), 1580 (strong), 1540 (strong), 1490 (strong), 1470 (strong), 1450 (strong), 1430 (strong), 1410 (strong), 1390 (strong), 1370 (strong), 1350 (strong), 1330 (strong), 1310 (strong), 1290 (strong), 1270 (strong), 1250 (strong), 1230 (strong), 1210 (strong), 1190 (strong), 1170 (strong), 1150 (strong), 1130 (strong), 1110 (strong), 1090 (strong), 1070 (strong), 1050 (strong), 1030 (strong), 1010 (strong), 990 (strong), 970 (strong), 950 (strong), 930 (strong), 910 (strong), 890 (strong), 870 (strong), 850 (strong), 830 (strong), 810 (strong), 790 (strong), 770 (strong), 750 (strong), 730 (strong), 710 (strong), 690 (strong), 670 (strong), 650 (strong), 630 (strong), 610 (strong), 590 (strong), 570 (strong), 550 (strong), 530 (strong), 510 (strong), 490 (strong), 470 (strong), 450 (strong), 430 (strong), 410 (strong), 390 (strong), 370 (strong), 350 (strong), 330 (strong), 310 (strong), 290 (strong), 270 (strong), 250 (strong), 230 (strong), 210 (strong), 190 (strong), 170 (strong), 150 (strong), 130 (strong), 110 (strong), 90 (strong), 70 (strong), 50 (strong), 30 (strong), 10 (strong), 0 (strong).

[illegible]

The following table shows the results of the regression analysis for the dependent variable "Percentage of respondents who agree with the statement: 'The government should do more to help the poor'".

10. The defendant shall not be liable for any damages, including but not limited to, special damages, consequential damages, or punitive damages, arising out of or from the use of the software, whether or not such damages are foreseeable.

Researcher's conceptual objectives should reflect the project's primary goals and objectives. It should be clear that the researcher's conceptual objectives should be derived from the project's primary goals and objectives.



Power-off sequence (if needed):

Set XTAL1 to "L" (if a crystal is not used).

Set RST to "L".

Turn V_{CC} power off.

Data Polling: The Data Polling feature is also available in the serial mode. In this mode, during a write cycle an attempted read of the last byte written will result in the complement of the MSB of the serial output byte on MISO.

The Instruction Set for Serial Programming follows a 4-byte protocol and is shown in Table 8 on page 18.

Serial Programming Instruction Set

Parallel Mode

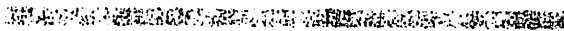
Every code byte in the Flash array can be programmed by using the appropriate combination of control signals. The write operation cycle is self-timed and once initiated, will automatically time itself to completion.

All major programming vendors offer worldwide support for the Atmel microcontroller series. Please contact your local programming vendor for the appropriate software revision.

Table 7. Flash Programming Modes

Operation	V_{CC}	RST	$\overline{PSEN}$	ALE/ PROG	$\overline{EA}/V_{PP}$	P2.6	P2.7	P3.3	P3.6	P3.7	P0.7-0 Data	P2.3-0	P1.7-0
												Address	
Write Code Data	5V	H	L		12V	L	H	H	H	H	D_{IN}	A11-8	A7-0
Erase Code Data	5V	H	L	H	H	L	L	L	H	H	D_{OUT}	A11-8	A7-0
Write Lock Bit 1	5V	H	L		12V	H	H	H	H	H	X	X	X
Write Lock Bit 2	5V	H	L		12V	H	H	H	L	L	X	X	X
Write Lock Bit 3	5V	H	L		12V	H	L	H	H	L	X	X	X
Erase Lock Bits 1-3	5V	H	L	H	H	H	H	L	H	L	P0.2, P0.3, P0.4	X	X
Chip Erase	5V	H	L		12V	H	L	H	L	L	X	X	X
Read Atmel ID	5V	H	L	H	H	L	L	L	L	L	1EH	0000	00H
Read Device ID	5V	H	L	H	H	L	L	L	L	L	51H	0001	00H
Read Device ID	5V	H	L	H	H	L	L	L	L	L	06H	0010	00H

- Notes:
1. Each $\overline{PROG}$ pulse is 200 ns - 500 ns for Chip Erase.
 2. Each $\overline{PROG}$ pulse is 200 ns - 500 ns for Write Code Data.
 3. Each $\overline{PROG}$ pulse is 200 ns - 500 ns for Write Lock Bits.
 4. RDY/BSY signal is output on P3.0 during programming.
 5. X = don't care.



Abstract: 1. 2009.12.16 10:10:00

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Positive relationships between family and biological characteristics were observed primarily among higher SES mothers, but not among lower SES mothers, and for children's problem behaviors, not for children's social skills.

Figure 1. The effect of the number of trials on the number of correct responses. The number of correct responses was plotted against the number of trials for each condition. The number of correct responses increased with the number of trials for all conditions. The number of correct responses was highest for the condition with the highest number of trials (10 trials) and lowest for the condition with the lowest number of trials (2 trials).

[illegible]

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Figure 4. Programming the Flash Memory (Parallel Mode)

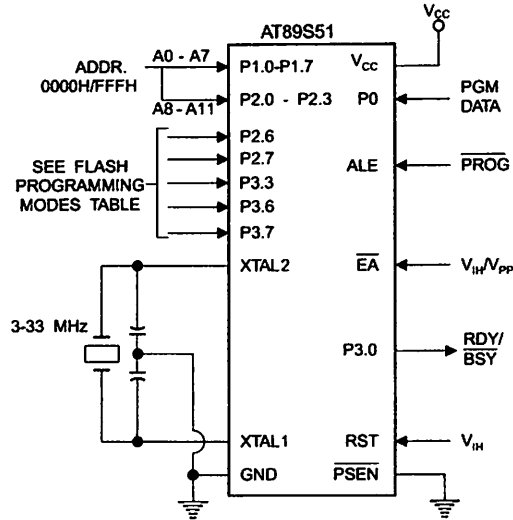
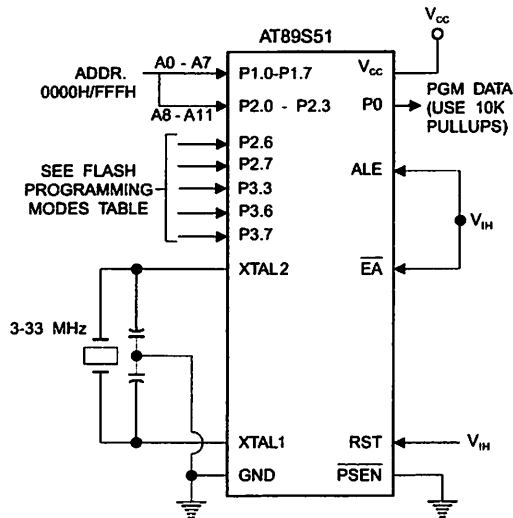


Figure 5. Verifying the Flash Memory (Parallel Mode)



1960/1961 (1960/1961) 1960/1961 (1960/1961) 1960/1961 (1960/1961)

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Flash Programming and Verification Characteristics (Parallel Mode)

$T = 20^{\circ}\text{C to } 30^{\circ}\text{C}$, $V_{CC} = 4.5 \text{ to } 5.5\text{V}$

Symbol	Parameter	Min	Max	Units
V_P	Programming Supply Voltage	11.5	12.5	V
I_P	Programming Supply Current		10	mA
I_{CC}	V_{CC} Supply Current		30	mA
f_{CLCL}	Oscillator Frequency	3	33	MHz
t_{AVGL}	Address Setup to $\overline{\text{PROG}}$ Low	$48t_{CLCL}$		
t_{GHAX}	Address Hold After $\overline{\text{PROG}}$	$48t_{CLCL}$		
t_{SHGL}	Data Setup to $\overline{\text{PROG}}$ Low	$48t_{CLCL}$		
t_{GHDX}	Data Hold After $\overline{\text{PROG}}$	$48t_{CLCL}$		
t_{ELSH}	P2.7 ($\overline{\text{ENABLE}}$) High to V_{PP}	$48t_{CLCL}$		
t_{AVGL}	V_{PP} Setup to $\overline{\text{PROG}}$ Low	10		μs
t_{HSL}	V_{PP} Hold After $\overline{\text{PROG}}$	10		μs
t_{GLGH}	$\overline{\text{PROG}}$ Width	0.2	1	μs
t_{AVQV}	Address to Data Valid		$48t_{CLCL}$	
t_{ELQV}	$\overline{\text{ENABLE}}$ Low to Data Valid		$48t_{CLCL}$	
t_{EHQZ}	Data Float After $\overline{\text{ENABLE}}$	0	$48t_{CLCL}$	
t_{HBL}	$\overline{\text{PROG}}$ High to $\overline{\text{BUSY}}$ Low		1.0	μs
t_{WC}	Byte Write Cycle Time		50	μs

Figure 6. Flash Programming and Verification Waveforms – Parallel Mode

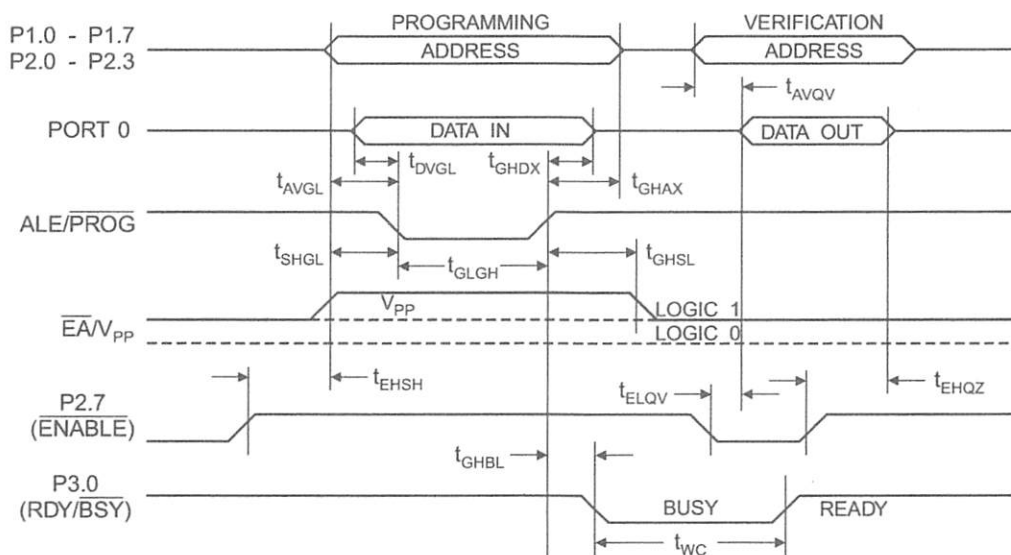
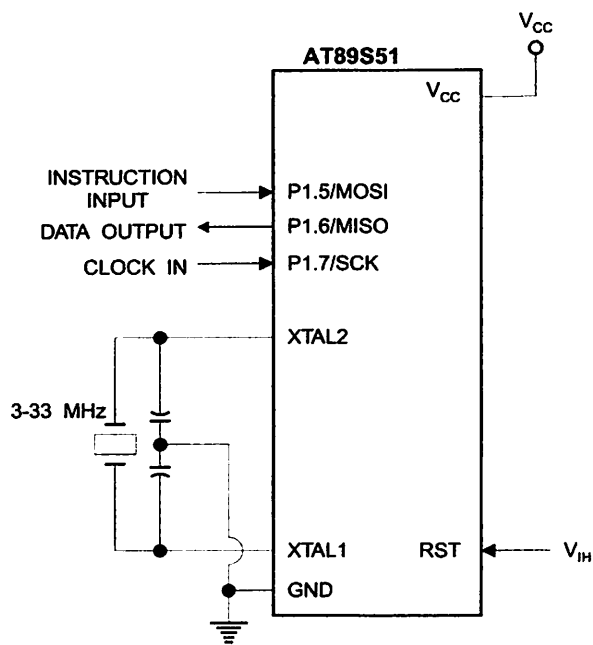


Figure 7. Flash Memory Serial Downloading



Flash Programming and Verification Waveforms – Serial Mode

Figure 8. Serial Programming Waveforms

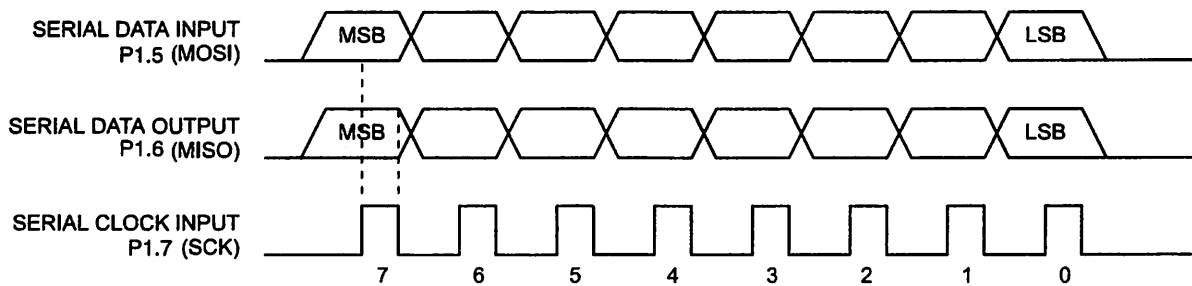


Table 8. Serial Programming Instruction Set

Instruction	Instruction Format				Operation
	Byte 1	Byte 2	Byte 3	Byte 4	
Programming Enable	1010 1100	0101 0011	xxxx xxxx	xxxx xxxx 0110 1001 (Output)	Enable Serial Programming while RST is high
Chip Erase	1010 1100	100x xxxx	xxxx xxxx	xxxx xxxx	Chip Erase Flash memory array
Read Program Memory (Byte Mode)	0010 0000	xxxx A ₁₁ A ₁₀ A ₉ A ₈	A ₇ A ₆ A ₅ A ₄ A ₃ A ₂ A ₁ A ₀	A ₇ A ₆ A ₅ A ₄ A ₃ A ₂ A ₁ A ₀	Read data from Program memory in the byte mode
Write Program Memory (Byte Mode)	0100 0000	xxxx A ₁₁ A ₁₀ A ₉ A ₈	A ₇ A ₆ A ₅ A ₄ A ₃ A ₂ A ₁ A ₀	A ₇ A ₆ A ₅ A ₄ A ₃ A ₂ A ₁ A ₀	Write data to Program memory in the byte mode
Write Lock Bits ⁽²⁾	1010 1100	1110 00 B ₁ B ₂	xxxx xxxx	xxxx xxxx	Write Lock bits. See Note (2).
Read Lock Bits	0010 0100	xxxx xxxx	xxxx xxxx	xx B ₃ B ₂ B ₁ B ₀ xx	Read back current status of the lock bits (a programmed lock bit reads back as a "1")
Read Signature Bytes ⁽¹⁾	0010 1000	xxx A ₅ A ₄ A ₃ A ₂ A ₁	A ₀ xxx xxxx	Signature Byte	Read Signature Byte
Read Program Memory (Page Mode)	0011 0000	xxxx A ₁₁ A ₁₀ A ₉ A ₈	Byte 0	Byte 1... Byte 255	Read data from Program memory in the Page Mode (256 bytes)
Write Program Memory (Page Mode)	0101 0000	xxxx A ₁₁ A ₁₀ A ₉ A ₈	Byte 0	Byte 1... Byte 255	Write data to Program memory in the Page Mode (256 bytes)

Notes: 1. The signature bytes are not readable in Lock Bit Modes 3 and 4.

2. B₁ = 0, B₂ = 0 → Mode 1, no lock protection
 B₁ = 0, B₂ = 1 → Mode 2, lock bit 1 activated
 B₁ = 1, B₂ = 0 → Mode 3, lock bit 2 activated
 B₁ = 1, B₂ = 1 → Mode 4, lock bit 3 activated

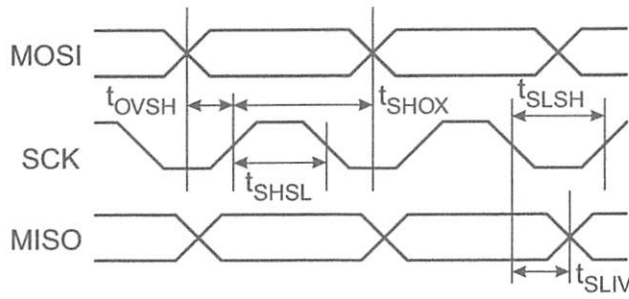
Each of the lock bits needs to be activated sequentially before Mode 4 can be executed.

After Reset signal is high, SCK should be low for at least 64 system clocks before it goes high to clock in the enable data bytes. No pulsing of Reset signal is necessary. SCK should be no faster than 1/16 of the system clock at XTAL1.

For Page Read/Write, the data always starts from byte 0 to 255. After the command byte and upper address byte are latched, each byte thereafter is treated as data until all 256 bytes are shifted in/out. Then the next instruction will be ready to be decoded.

Serial Programming Characteristics

Figure 9. Serial Programming Timing

Table 9. Serial Programming Characteristics, $T_A = -40^\circ\text{C}$ to 85°C , $V_{CC} = 4.0 - 5.5\text{V}$ (Unless Otherwise Noted)

Symbol	Parameter	Min	Typ	Max	Units
$1/t_{CLCL}$	Oscillator Frequency	0		33	MHz
t_{CLCL}	Oscillator Period	30			ns
t_{SHSL}	SCK Pulse Width High	$8 t_{CLCL}$			ns
t_{SLSH}	SCK Pulse Width Low	$8 t_{CLCL}$			ns
t_{OVSH}	MOSI Setup to SCK High	t_{CLCL}			ns
t_{SHOX}	MOSI Hold after SCK High	$2 t_{CLCL}$			ns
t_{SLIV}	SCK Low to MISO Valid	10	16	32	ns
t_{ERASE}	Chip Erase Instruction Cycle Time			500	ms
t_{SWC}	Serial Byte Write Cycle Time			$64 t_{CLCL} + 400$	μs

Absolute Maximum Ratings*

Operating Temperature.....	-55°C to +125°C
Storage Temperature.....	-65°C to +150°C
Voltage on Any Pin with Respect to Ground.....	-1.0V to +7.0V
Maximum Operating Voltage	6.6V
Maximum Output Current.....	15.0 mA

***NOTICE:** Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Characteristics

Values shown in this table are valid for $T_A = -40^{\circ}\text{C}$ to 85°C and $V_{CC} = 4.0\text{V}$ to 5.5V , unless otherwise noted.

Symbol	Parameter	Condition	Min	Max	Units
	Input Low Voltage	(Except $\overline{\text{EA}}$)	-0.5	$0.2 V_{CC}-0.1$	V
I_{IL}	Input Low Voltage ($\overline{\text{EA}}$)		-0.5	$0.2 V_{CC}-0.3$	V
	Input High Voltage	(Except XTAL1, RST)	$0.2 V_{CC}+0.9$	$V_{CC}+0.5$	V
I_{IH}	Input High Voltage	(XTAL1, RST)	$0.7 V_{CC}$	$V_{CC}+0.5$	V
	Output Low Voltage ⁽¹⁾ (Ports 1,2,3)	$I_{OL} = 1.6 \text{ mA}$		0.45	V
I_{OL}	Output Low Voltage ⁽¹⁾ (Port 0, ALE, $\overline{\text{PSEN}}$)	$I_{OL} = 3.2 \text{ mA}$		0.45	V
	Output High Voltage (Ports 1,2,3, ALE, $\overline{\text{PSEN}}$)	$I_{OH} = -60 \mu\text{A}, V_{CC} = 5\text{V} \pm 10\%$	2.4		V
I_{OH}		$I_{OH} = -25 \mu\text{A}$	$0.75 V_{CC}$		V
		$I_{OH} = -10 \mu\text{A}$	$0.9 V_{CC}$		V
	Output High Voltage (Port 0 in External Bus Mode)	$I_{OH} = -800 \mu\text{A}, V_{CC} = 5\text{V} \pm 10\%$	2.4		V
I_{OH}		$I_{OH} = -300 \mu\text{A}$	$0.75 V_{CC}$		V
		$I_{OH} = -80 \mu\text{A}$	$0.9 V_{CC}$		V
	Logical 0 Input Current (Ports 1,2,3)	$V_{IN} = 0.45\text{V}$		-50	μA
	Logical 1 to 0 Transition Current (Ports 1,2,3)	$V_{IN} = 2\text{V}, V_{CC} = 5\text{V} \pm 10\%$		-650	μA
	Input Leakage Current (Port 0, $\overline{\text{EA}}$)	$0.45 < V_{IN} < V_{CC}$		± 10	μA
RST	Reset Pulldown Resistor		50	300	$\text{K}\Omega$
	Pin Capacitance	Test Freq. = 1 MHz, $T_A = 25^{\circ}\text{C}$		10	pF
	Power Supply Current	Active Mode, 12 MHz		25	mA
		Idle Mode, 12 MHz		6.5	mA
	Power-down Mode ⁽²⁾	$V_{CC} = 5.5\text{V}$		50	μA

Notes: 1. Under steady state (non-transient) conditions, I_{OL} must be externally limited as follows:

Maximum I_{OL} per port pin: 10 mA

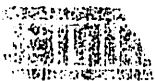
Maximum I_{OL} per 8-bit port:

Port 0: 26 mA Ports 1, 2, 3: 15 mA

Maximum total I_{OL} for all output pins: 71 mA

If I_{OL} exceeds the test condition, V_{OL} may exceed the related specification. Pins are not guaranteed to sink current greater than the listed test conditions.

2. Minimum V_{CC} for Power-down is 2V.



Agilent Technologies

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Characteristics

The Agilent 1100 Series is a high-performance liquid chromatography (HPLC) system designed for the analysis of a wide range of samples. It features a robust and reliable design, with a long service life and low maintenance requirements. The system is equipped with a variety of detectors, including UV-Vis, fluorescence, and refractive index, to meet your specific analytical needs. It also offers a range of optional accessories, such as autosamplers and guard columns, to enhance its performance and versatility. The Agilent 1100 Series is a cost-effective solution for laboratories looking to improve their HPLC capabilities.

Agilent Technologies is a leading provider of analytical instruments and solutions for a wide range of industries. Our products and services are designed to help you improve your productivity, reduce costs, and ensure the highest quality of your results.

Model	Detector	Flow Rate	Injection Volume	Sample Capacity	Operating Temperature	Dimensions	Weight
1100A	UV-Vis	0.1-1.0 mL/min	1-100 µL	100 µL	10-40 °C	100 x 100 x 100 mm	10 kg
1100B	Fluorescence	0.1-1.0 mL/min	1-100 µL	100 µL	10-40 °C	100 x 100 x 100 mm	10 kg
1100C	Refractive Index	0.1-1.0 mL/min	1-100 µL	100 µL	10-40 °C	100 x 100 x 100 mm	10 kg
1100D	UV-Vis	0.1-1.0 mL/min	1-100 µL	100 µL	10-40 °C	100 x 100 x 100 mm	10 kg
1100E	Fluorescence	0.1-1.0 mL/min	1-100 µL	100 µL	10-40 °C	100 x 100 x 100 mm	10 kg
1100F	Refractive Index	0.1-1.0 mL/min	1-100 µL	100 µL	10-40 °C	100 x 100 x 100 mm	10 kg
1100G	UV-Vis	0.1-1.0 mL/min	1-100 µL	100 µL	10-40 °C	100 x 100 x 100 mm	10 kg
1100H	Fluorescence	0.1-1.0 mL/min	1-100 µL	100 µL	10-40 °C	100 x 100 x 100 mm	10 kg
1100I	Refractive Index	0.1-1.0 mL/min	1-100 µL	100 µL	10-40 °C	100 x 100 x 100 mm	10 kg
1100J	UV-Vis	0.1-1.0 mL/min	1-100 µL	100 µL	10-40 °C	100 x 100 x 100 mm	10 kg
1100K	Fluorescence	0.1-1.0 mL/min	1-100 µL	100 µL	10-40 °C	100 x 100 x 100 mm	10 kg
1100L	Refractive Index	0.1-1.0 mL/min	1-100 µL	100 µL	10-40 °C	100 x 100 x 100 mm	10 kg
1100M	UV-Vis	0.1-1.0 mL/min	1-100 µL	100 µL	10-40 °C	100 x 100 x 100 mm	10 kg
1100N	Fluorescence	0.1-1.0 mL/min	1-100 µL	100 µL	10-40 °C	100 x 100 x 100 mm	10 kg
1100O	Refractive Index	0.1-1.0 mL/min	1-100 µL	100 µL	10-40 °C	100 x 100 x 100 mm	10 kg
1100P	UV-Vis	0.1-1.0 mL/min	1-100 µL	100 µL	10-40 °C	100 x 100 x 100 mm	10 kg
1100Q	Fluorescence	0.1-1.0 mL/min	1-100 µL	100 µL	10-40 °C	100 x 100 x 100 mm	10 kg
1100R	Refractive Index	0.1-1.0 mL/min	1-100 µL	100 µL	10-40 °C	100 x 100 x 100 mm	10 kg
1100S	UV-Vis	0.1-1.0 mL/min	1-100 µL	100 µL	10-40 °C	100 x 100 x 100 mm	10 kg
1100T	Fluorescence	0.1-1.0 mL/min	1-100 µL	100 µL	10-40 °C	100 x 100 x 100 mm	10 kg
1100U	Refractive Index	0.1-1.0 mL/min	1-100 µL	100 µL	10-40 °C	100 x 100 x 100 mm	10 kg
1100V	UV-Vis	0.1-1.0 mL/min	1-100 µL	100 µL	10-40 °C	100 x 100 x 100 mm	10 kg
1100W	Fluorescence	0.1-1.0 mL/min	1-100 µL	100 µL	10-40 °C	100 x 100 x 100 mm	10 kg
1100X	Refractive Index	0.1-1.0 mL/min	1-100 µL	100 µL	10-40 °C	100 x 100 x 100 mm	10 kg
1100Y	UV-Vis	0.1-1.0 mL/min	1-100 µL	100 µL	10-40 °C	100 x 100 x 100 mm	10 kg
1100Z	Fluorescence	0.1-1.0 mL/min	1-100 µL	100 µL	10-40 °C	100 x 100 x 100 mm	10 kg

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Characteristics

Under operating conditions, load capacitance for Port 0, ALE/ $\overline{\text{PROG}}$, and $\overline{\text{PSEN}}$ = 100 pF; load capacitance for all other ports = 80 pF.

Internal Program and Data Memory Characteristics

Symbol	Parameter	12 MHz Oscillator		Variable Oscillator		Units
		Min	Max	Min	Max	
CLCL	Oscillator Frequency			0	33	MHz
CLL	ALE Pulse Width	127		$2t_{\text{CLCL}}-40$		ns
CLL	Address Valid to ALE Low	43		$t_{\text{CLCL}}-25$		ns
CLL	Address Hold After ALE Low	48		$t_{\text{CLCL}}-25$		ns
CLV	ALE Low to Valid Instruction In		233		$4t_{\text{CLCL}}-65$	ns
CLL	ALE Low to $\overline{\text{PSEN}}$ Low	43		$t_{\text{CLCL}}-25$		ns
CLPH	$\overline{\text{PSEN}}$ Pulse Width	205		$3t_{\text{CLCL}}-45$		ns
CLV	$\overline{\text{PSEN}}$ Low to Valid Instruction In		145		$3t_{\text{CLCL}}-60$	ns
CLX	Input Instruction Hold After $\overline{\text{PSEN}}$	0		0		ns
CLZ	Input Instruction Float After $\overline{\text{PSEN}}$		59		$t_{\text{CLCL}}-25$	ns
CLAV	$\overline{\text{PSEN}}$ to Address Valid	75		$t_{\text{CLCL}}-8$		ns
CLV	Address to Valid Instruction In		312		$5t_{\text{CLCL}}-80$	ns
CLAZ	$\overline{\text{PSEN}}$ Low to Address Float		10		10	ns
CLRH	$\overline{\text{RD}}$ Pulse Width	400		$6t_{\text{CLCL}}-100$		ns
CLWH	$\overline{\text{WR}}$ Pulse Width	400		$6t_{\text{CLCL}}-100$		ns
CLDV	$\overline{\text{RD}}$ Low to Valid Data In		252		$5t_{\text{CLCL}}-90$	ns
CLDX	Data Hold After $\overline{\text{RD}}$	0		0		ns
CLDZ	Data Float After $\overline{\text{RD}}$		97		$2t_{\text{CLCL}}-28$	ns
CLDV	ALE Low to Valid Data In		517		$8t_{\text{CLCL}}-150$	ns
CLDV	Address to Valid Data In		585		$9t_{\text{CLCL}}-165$	ns
CLVL	ALE Low to $\overline{\text{RD}}$ or $\overline{\text{WR}}$ Low	200	300	$3t_{\text{CLCL}}-50$	$3t_{\text{CLCL}}+50$	ns
CLWL	Address to $\overline{\text{RD}}$ or $\overline{\text{WR}}$ Low	203		$4t_{\text{CLCL}}-75$		ns
CLWX	Data Valid to $\overline{\text{WR}}$ Transition	23		$t_{\text{CLCL}}-30$		ns
CLWH	Data Valid to $\overline{\text{WR}}$ High	433		$7t_{\text{CLCL}}-130$		ns
CLQX	Data Hold After $\overline{\text{WR}}$	33		$t_{\text{CLCL}}-25$		ns
CLAZ	$\overline{\text{RD}}$ Low to Address Float		0		0	ns
CLLH	$\overline{\text{RD}}$ or $\overline{\text{WR}}$ High to ALE High	43	123	$t_{\text{CLCL}}-25$	$t_{\text{CLCL}}+25$	ns

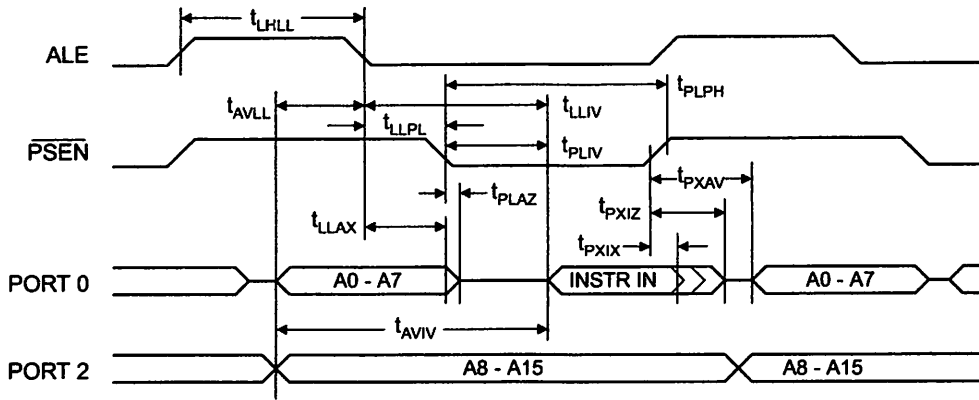


1. General information and background for the project, including the name of the project, the sponsor, the date of the report, and the name of the author.

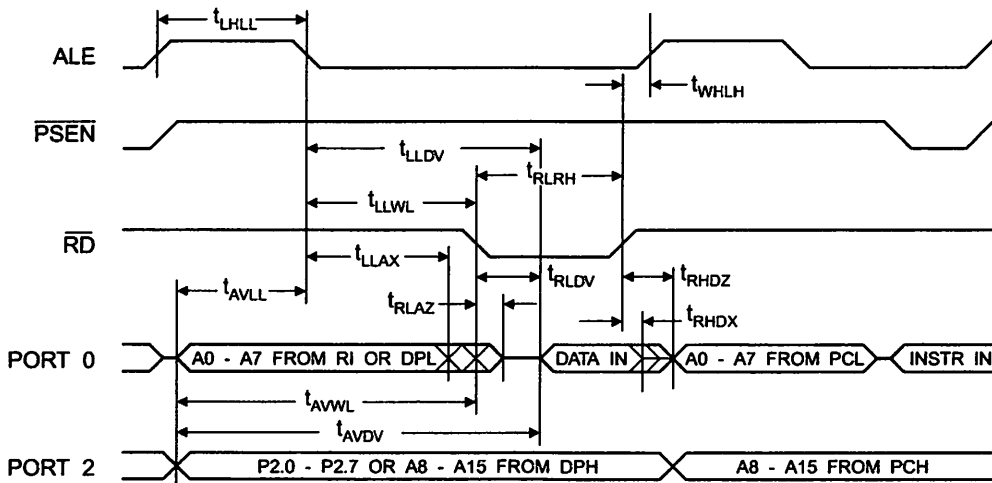
General Information and Background

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2. Sponsor	2. Sponsor		2. Sponsor
3. Date of Report	3. Date of Report		3. Date of Report
4. Author	4. Author		4. Author
5. Title	5. Title		5. Title
6. Abstract	6. Abstract		6. Abstract
7. Introduction	7. Introduction		7. Introduction
8. Objectives	8. Objectives		8. Objectives
9. Methodology	9. Methodology		9. Methodology
10. Results	10. Results		10. Results
11. Discussion	11. Discussion		11. Discussion
12. Conclusion	12. Conclusion		12. Conclusion
13. References	13. References		13. References
14. Appendix	14. Appendix		14. Appendix
15. Glossary	15. Glossary		15. Glossary
16. Bibliography	16. Bibliography		16. Bibliography
17. Index	17. Index		17. Index
18. Summary	18. Summary		18. Summary
19. Acknowledgments	19. Acknowledgments		19. Acknowledgments
20. Notes	20. Notes		20. Notes
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22. Tables	22. Tables		22. Tables
23. Equations	23. Equations		23. Equations
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25. Abbreviations	25. Abbreviations		25. Abbreviations
26. Acronyms	26. Acronyms		26. Acronyms
27. Units	27. Units		27. Units
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96. Conversions	96. Conversions		96. Conversions
97. Definitions	97. Definitions		97. Definitions
98. References	98. References		98. References
99. Appendix	99. Appendix		99. Appendix
100. Glossary	100. Glossary		100. Glossary

Internal Program Memory Read Cycle



Internal Data Memory Read Cycle

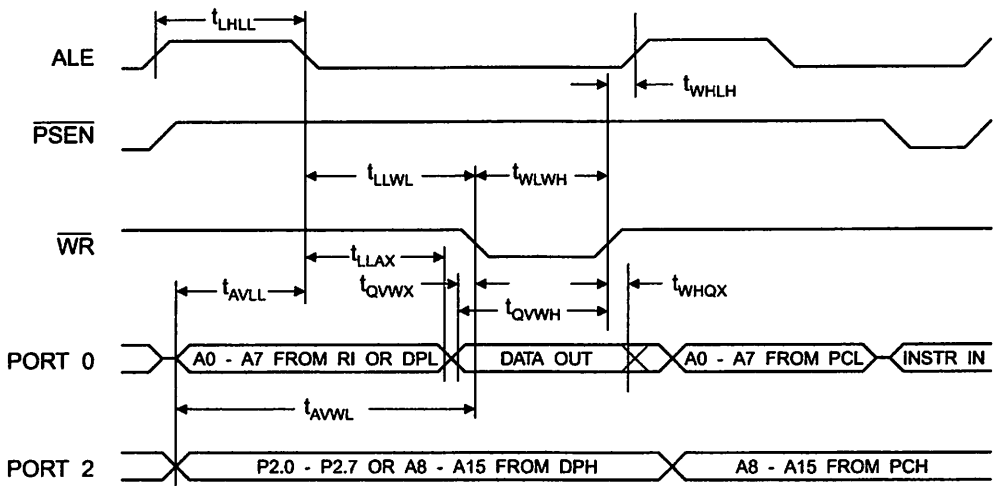


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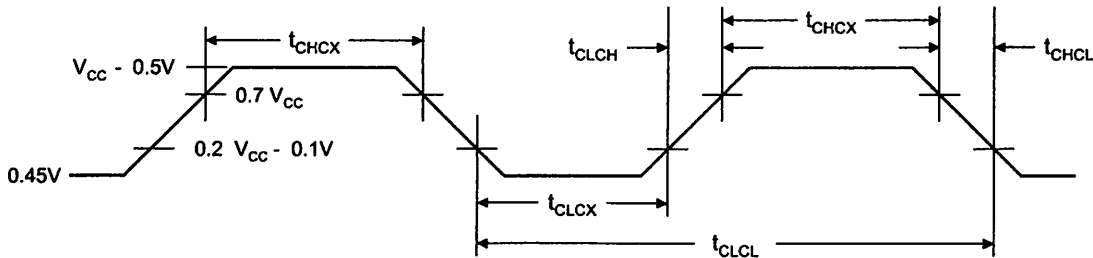
along with general and limited

FOIA b 7 - D

Internal Data Memory Write Cycle



Internal Clock Drive Waveforms



Internal Clock Drive

Symbol	Parameter	Min	Max	Units
f_{CLCL}	Oscillator Frequency	0	33	MHz
T_{CL}	Clock Period	30		ns
t_{CHCX}	High Time	12		ns
t_{CLCX}	Low Time	12		ns
t_{CH}	Rise Time		5	ns
t_{CL}	Fall Time		5	ns

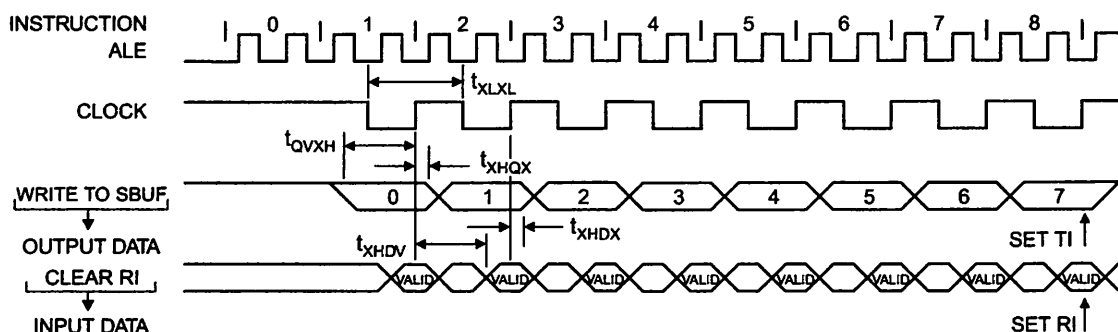


Serial Port Timing: Shift Register Mode Test Conditions

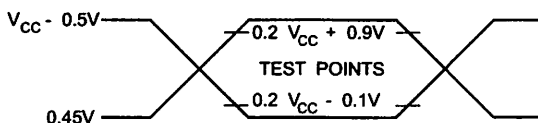
values in this table are valid for $V_{CC} = 4.0V$ to $5.5V$ and Load Capacitance = 80 pF.

Symbol	Parameter	12 MHz Osc		Variable Oscillator		Units
		Min	Max	Min	Max	
	Serial Port Clock Cycle Time	1.0		$12t_{CLCL}$		μs
t_{4}	Output Data Setup to Clock Rising Edge	700		$10t_{CLCL}-133$		ns
t_{K}	Output Data Hold After Clock Rising Edge	50		$2t_{CLCL}-80$		ns
t_{K}	Input Data Hold After Clock Rising Edge	0		0		ns
t_{7}	Clock Rising Edge to Input Data Valid		700		$10t_{CLCL}-133$	ns

8.1.1 16-bit Register Mode Timing Waveforms

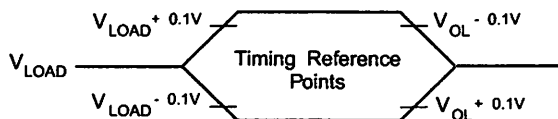


Testing Input/Output Waveforms⁽¹⁾

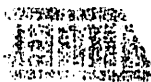


1. AC Inputs during testing are driven at $V_{CC} - 0.5V$ for a logic 1 and $0.45V$ for a logic 0. Timing measurements are made at V_{IH} min. for a logic 1 and V_{IL} max. for a logic 0.

at Waveforms⁽¹⁾



1. For timing purposes, a port pin is no longer floating when a 100 mV change from load voltage occurs. A port pin begins to float when a 100 mV change from the loaded V_{OH}/V_{OL} level occurs.



enrollment test about halfway into permit no. 151

Fig. 108 = $\frac{\text{concentration of bacteria}}{\text{volume of water}} \times 100$ = number of bacteria per milliliter of water

[illegible]

overly sensitive patient should be kept in the

Amesbury Hospital

ly. In order to estimate the sampling error of the gross value added (GVA) data, the sampling error of the input data is estimated by using the following formula:

Continued on next page

^a $\chi^2_{(1)} = 0.96$, $p = 0.33$. ^b $\chi^2_{(1)} = 0.87$, $p = 0.35$.

ALL INFORMATION CONTAINED HEREIN IS UNCLASSIFIED DATE 06-08-2007 BY 60322 UCBAW

• • • • •

Ordering Information

Speed (MHz)	Power Supply	Ordering Code	Package	Operation Range
24	4.0V to 5.5V	AT89S51-24AC	44A	Commercial (0° C to 70° C)
		AT89S51-24JC	44J	
		AT89S51-24PC	40P6	
		AT89S51-24AI	44A	Industrial (-40° C to 85° C)
		AT89S51-24JI	44J	
		AT89S51-24PI	40P6	
33	4.5V to 5.5V	AT89S51-33AC	44A	Commercial (0° C to 70° C)
		AT89S51-33JC	44J	
		AT89S51-33PC	40P6	

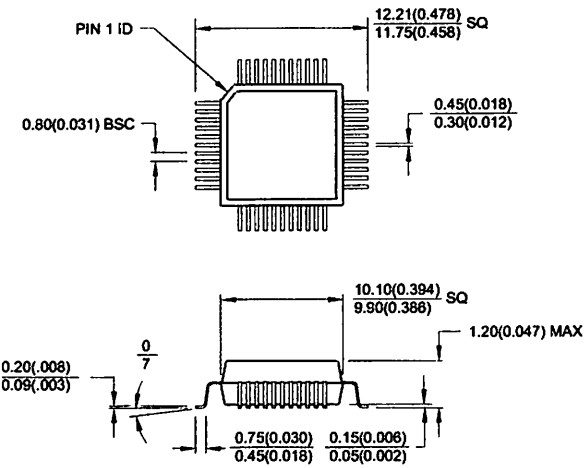
= Preliminary Availability

Package Type	
A	44-lead, Thin Plastic Gull Wing Quad Flatpack (TQFP)
J	44-lead, Plastic J-leaded Chip Carrier (PLCC)
P6	40-pin, 0.600" Wide, Plastic Dual Inline Package (PDIP)



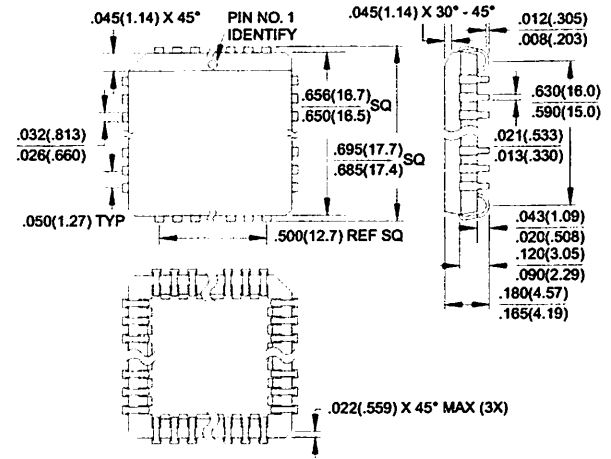
Packaging Information

44A, 44-lead, Thin (1.0 mm) Plastic Gull Wing Quad Flat Package (TQFP)
 Dimensions in Millimeters and (Inches)*

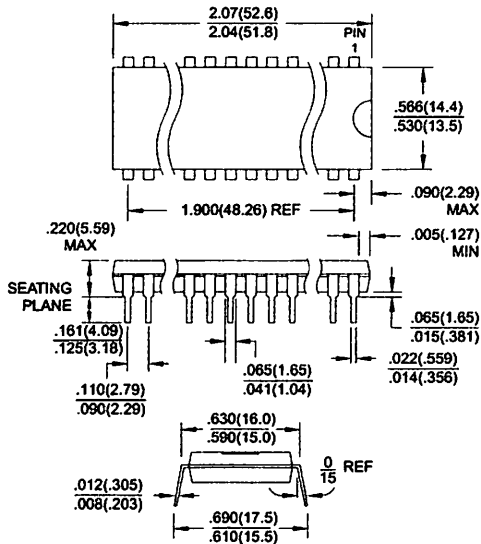


*Controlling dimension: millimeters

44J, 44-lead, Plastic J-leaded Chip Carrier (PLCC)
 Dimensions in Inches and (Millimeters)



40P6, 40-pin, 0.600" Wide, Plastic Dual Inline Package (PDIP)
 Dimensions in Inches and (Millimeters)
 JEDEC STANDARD MS-011 AC



7-10000

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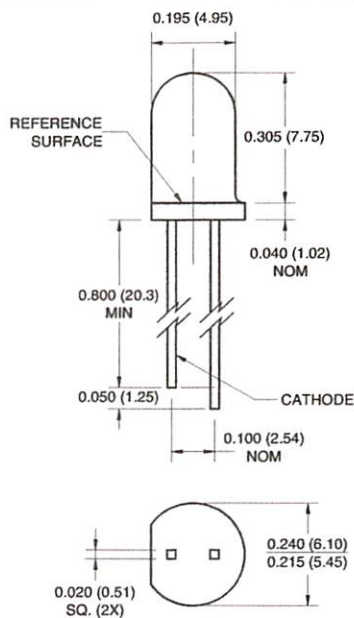
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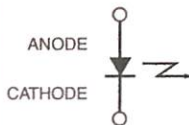
QED233

QED234

PACKAGE DIMENSIONS



SCHEMATIC



ES:
 Dimensions for all drawings are in inches (mm).
 Tolerance of $\pm .010$ (.25) on all non-nominal dimensions
 unless otherwise specified.

DESCRIPTION

QED233 / QED234 is a 940 nm GaAs / AlGaAs LED encapsulated in a clear untinted, plastic T-1 3/4 package.

FEATURES

- Wavelength: 940 nm
- Semiconductor material: GaAs with AlGaAs window
- Package type: T-1 3/4 (5mm lens diameter)
- Associated Photosensor: QSD122/123/124
- Beam Emission Angle, 40°
- Output Power
- Package material and color: Clear, untinted, plastic
- Suitable for remote control applications

QED233

QED234

ABSOLUTE MAXIMUM RATINGS (T _A = 25°C unless otherwise specified)			
Parameter	Symbol	Rating	Unit
Operating Temperature	T _{OPR}	-40 to +100	°C
Storage Temperature	T _{STG}	-40 to +100	°C
Soldering Temperature (Iron) ^(2,3,4)	T _{SOL-I}	240 for 5 sec	°C
Soldering Temperature (Flow) ^(2,3)	T _{SOL-F}	260 for 10 sec	°C
Continuous Forward Current	I _F	100	mA
Reverse Voltage	V _R	5	V
Power Dissipation ⁽¹⁾	P _D	200	mW
Peak Forward Current	I _{FP}	1.5	A

1. Derate power dissipation linearly 2.67 mW/°C above 25°C.
2. Soldering flux is recommended.
3. Ethanol or isopropyl alcohols are recommended as cleaning agents.
4. Soldering iron 1/16" (1.6mm) minimum from housing.
5. Pulse conditions; tp = 100 µs, T = 10 ms.

ELECTRICAL / OPTICAL CHARACTERISTICS (T _A = 25°C)							
PARAMETER	TEST CONDITIONS	DEVICE	SYMBOL	MIN	TYP	MAX	UNITS
Emission Wavelength	I _F = 20 mA	ALL	λ _{PE}	—	940	—	nm
Spectral Bandwidth	I _F = 20 mA	ALL	—	50	—	nm	
Temp. Coefficient of λ _{PE}	I _F = 100 mA	ALL	TC _λ	—	0.2	—	nm/K
Emission Angle	I _F = 100 mA	ALL	2Θ _{1/2}	—	40	—	Deg.
Forward Voltage	I _F = 100 mA, tp = 20 ms	ALL	V _F	—	—	1.6	V
Temp. Coefficient of V _F	I _F = 100 mA	ALL	TC _V	—	-1.5	—	mV/K
Reverse Current	V _R = 5 V	ALL	I _R	—	—	10	µA
Radiant Intensity	I _F = 100 mA, tp = 20 ms	QED233	I _E	10	—	50	mW/sr
		QED234		27	—	—	
Temp. Coefficient of I _E	I _F = 20 mA	ALL	TC _I	—	-0.6	—	%/K
Rise Time	I _F = 100 mA	ALL	t _r	—	1000	—	ns
Fall Time		ALL	t _f	—	1000	—	

QED233

QED234

TYPICAL PERFORMANCE CURVES TBD

Fig. 1 Normalized Radiant Intensity vs. Forward Current

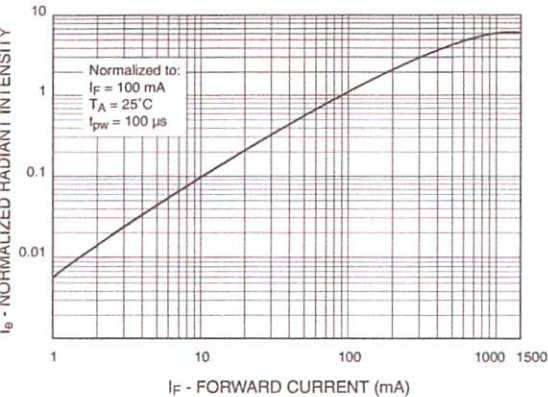


Fig. 2 Forward Voltage Vs. Ambient Temperature

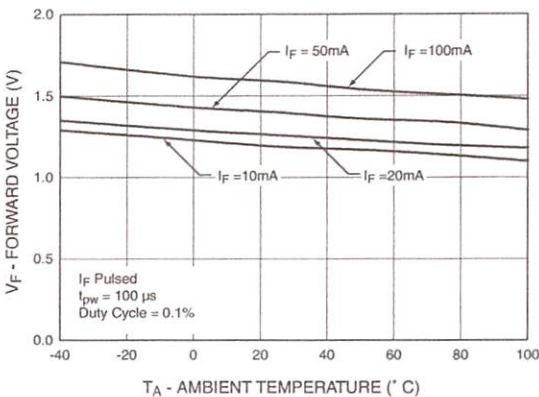


Fig. 3 Normalized Radiant Intensity vs. Wavelength

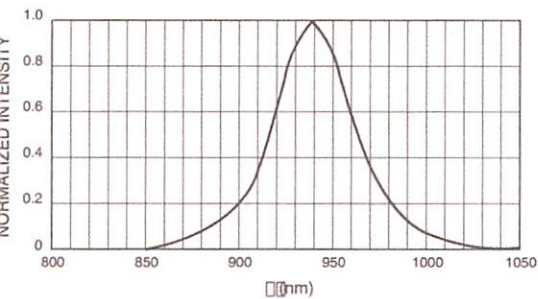


Fig. 4 Radiation Diagram

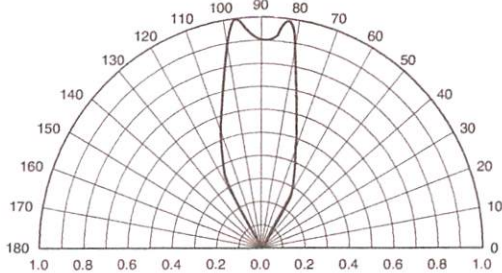
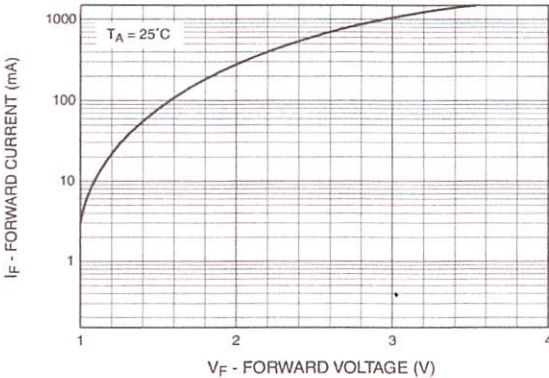


Fig. 5 Forward Current vs. Forward Voltage



QED233

QED234

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1. A life support device or system is a device or system which, (a) are intended for surgical implant into the body, or (b) support or sustain life, and (c) whose failure to perform when properly used in accordance with instructions for use provided in the labeling, can be reasonably expected to result in a significant injury of the user.
2. A critical component is any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.



80C31BH/80C51BH/87C51 MCS® 51 CHMOS SINGLE-CHIP 8-BIT MICROCONTROLLER

Automotive

- Extended Automotive Temperature Range (–40°C to +125°C Ambient)
- High Performance CHMOS Process
- Power Control Modes
- 4 Kbyte On-Chip ROM/EPROM
- 128 x 8-bit RAM
- 32 Programmable I/O Lines
- Two 16-Bit Timer/Counters
- 5 Interrupt Sources
- Quick-Pulse EPROM Programming
- 2-Level Program Memory Lock EPROM
- Boolean Processor
- Programmable Serial Port
- TTL- and CMOS-Compatible Logic Levels
- 64K External Program Memory Space
- 64K External Data Memory Space
- IDLE and POWER DOWN Modes
- ONCE Mode Facilitates System Testing
- Available in 12 MHz and 16 MHz Versions
- Available in PLCC and DIP Packages

(See Packaging Specification, Order #231368)

The MCS® 51 CHMOS microcontroller products are fabricated on Intel's reliable CHMOS process and are functionally compatible with the standard MCS 51 HMOS microcontroller products. This technology combines the high speed and density characteristics of HMOS with the low power attributes of CHMOS. This combination expands the effectiveness of the powerful MCS 51 microcontroller architecture and instruction set.

Like the MCS 51 HMOS microcontroller versions, the MCS 51 CHMOS microcontroller products have the following features: 4 Kbytes of EPROM/ROM (87C51/80C51BH respectively); 128 bytes of RAM; 32 I/O lines; two 16-bit timer/counters; a five-source two-level interrupt structure; a full duplex serial port; and on-chip oscillator and clock circuitry. In addition, the MCS 51 CHMOS microcontroller products exhibit low operating power, along with two software selectable modes of reduced activity for further power reduction—Idle and Power Down.

The Idle mode freezes the CPU while allowing the RAM, timer/counters, serial port, and interrupt system to continue functioning. The Power Down mode saves the RAM contents but freezes the oscillator, causing all other chip functions to be inoperative.

The 87C51 is the EPROM version of the 80C51BH. It contains 4 Kbytes of on-chip program memory that can be electrically programmed, and can be erased by exposure to ultraviolet light. The 87C51 EPROM array uses a modified Quick-Pulse Programming algorithm, by which the entire 4 Kbyte array can be programmed in about 12 seconds.

NOTICE:

This datasheet contains information on products in full production. Specifications within this datasheet are subject to change without notice. Verify with your local Intel sales office that you have the latest datasheet before finalizing a design.

*Other brands and names are the property of their respective owners.

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January 1985

Order Number: 270419-007

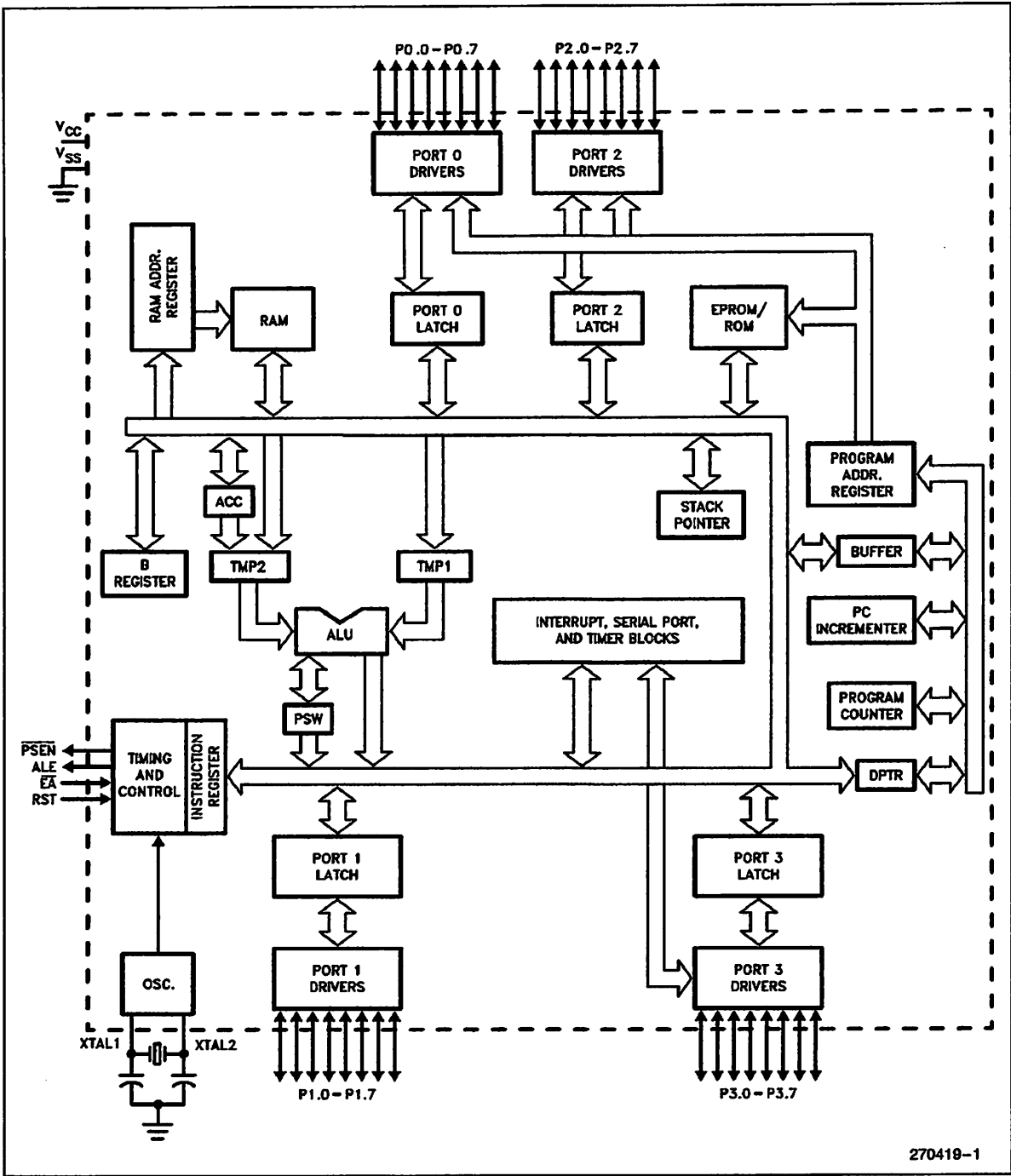


Figure 1. MCS® 51 Microcontroller Architectural Block Diagram

80C31BH/80C51BH/87C51
PRODUCT OPTIONS

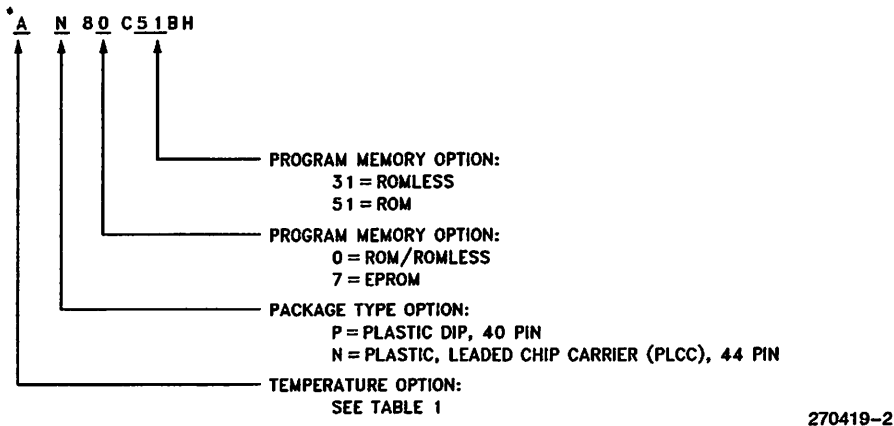
Intel's extended and automotive temperature range products are designed to meet the needs of those applications whose operating requirements exceed commercial standards.

With the extended temperature range option, operational characteristics are guaranteed over the temperature range of -40°C to +85°C ambient. For the

automotive temperature range option, operational characteristics are guaranteed over the temperature range of -40°C to +125°C ambient.

The automotive and extended temperature versions of the MCS 51 microcontroller product families are available with or without burn-in options as listed in Table 1.

As shown in Figure 2, temperature, burn-in, and package options are identified by a one- or two-letter prefix to the part number.



***Example:**
AN80C51 indicates an automotive temperature range version of the 80C51 in a PLCC package with 4 Kbyte ROM program memory.

Figure 2. MCS® 51 Microcontroller Product Family Nomenclature

Table 1. Temperature Options

Temperature Classification	Temperature Designation	Operating Temperature °C Ambient	Burn-In Options
Extended	T	-40 to +85	Standard
	L	-40 to +85	Extended
Automotive	A	-40 to +125	Standard
	B	-40 to +125	Extended

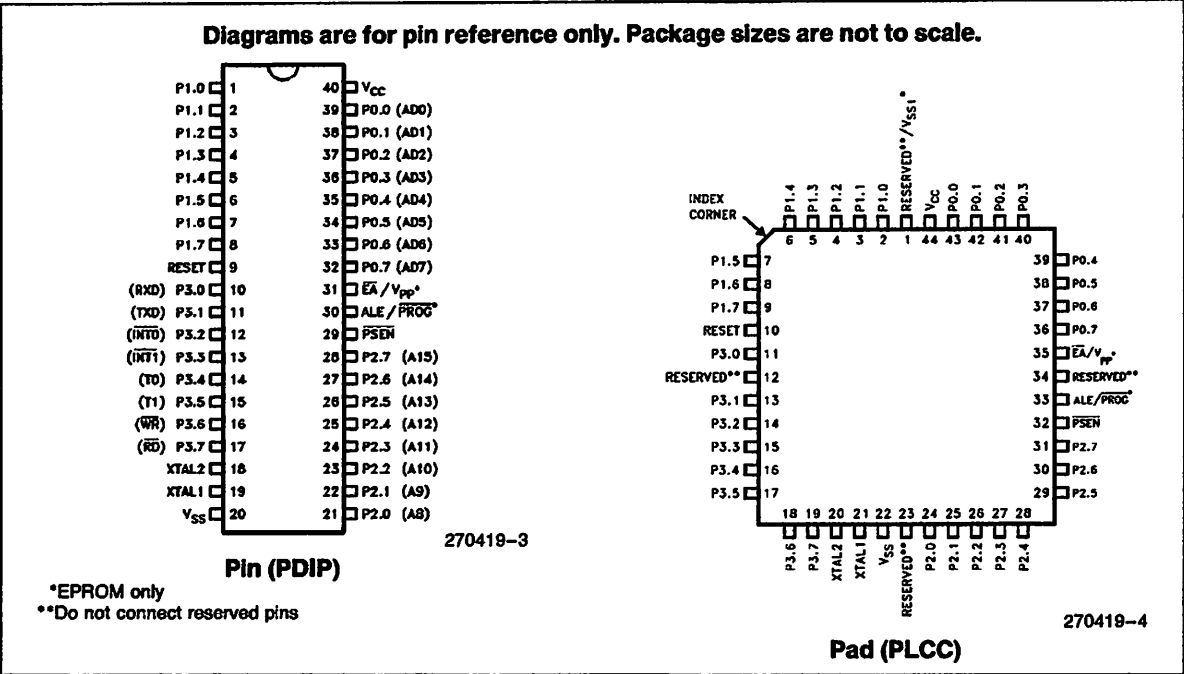


Figure 3. Pin Connections

PIN DESCRIPTION

V_{CC}: Supply voltage during normal, Idle, and Power Down operations.

V_{SS}: Circuit ground.

V_{SS1}: V_{SS1}—(EPROM PLCC only) secondary ground. Provided to reduce ground bounce and improve power supply bypassing.

NOTE:

This pin is not a substitute for the V_{SS} pin (pin 22). For ROM and ROMless, pin 1 is reserved—do not connect.

Port 0: Port 0 is an 8-bit open drain bidirectional I/O port. As an output port each pin can sink 8 LS TTL inputs. Port 0 pins that have 1s written to them float, and in that state can be used as high-impedance inputs.

Port 0 is also the multiplexed low-order address and data bus during accesses to external memory. In this application it uses strong internal pullups when emitting 1s.

Port 0 also receives the code bytes during EPROM programming, and outputs the code bytes during program verification. External pullups are required during program verification.

Port 1: Port 1 is an 8-bit bidirectional I/O port with internal pullups. Port 1 pins that have 1s written to them are pulled high by the internal pullups, and in that state can be used as inputs. As inputs, Port 1 pins that are externally being pulled low will source

current (I_{IL}, on the datasheet) because of the internal pullups.

Port 1 also receives the low-order address bytes during EPROM programming and program verification.

Port 2: Port 2 is an 8-bit bidirectional I/O port with internal pullups. Port 2 pins that have 1s written to them are pulled high by the internal pullups, and in that state can be used as inputs. As inputs, Port 2 pins that are externally being pulled low will source current (I_{IL}, on the data sheet) because of the internal pullups.

Port 2 emits the high-order address byte during fetches from external Program memory and during accesses to external Data Memory that use 16-bit address (MOVX @DPTR). In this application it uses strong internal pullups when emitting 1s.

During accesses to external Data Memory that use 8-bit addresses (MOVX @Ri), Port 2 emits the contents of the P2 Special Function Register.

Port 2 also receives some control signals and the high-order address bits during EPROM programming and program verification.

Port 3: Port 3 is an 8-bit bidirectional I/O port with internal pullups. Port 3 pins that have 1s written to them are pulled high by the internal pullups, and in that state can be used as inputs. As inputs, Port 3 pins that are externally being pulled low will source current (I_{IL}, on the datasheet) because of the pullups.

Port 3 also serves the functions of various special features of the MCS 51 microcontroller family, as listed below:

Pin	Name	Alternate Function
P3.0	RXD	Serial Input Line
P3.1	TXD	Serial Output Line
P3.2	INT0	External Interrupt 0
P3.3	INT1	External Interrupt 1
P3.4	T0	Timer 0 External Input
P3.5	T1	Timer 1 External Input
P3.6	WR	External Data Memory Write Strobe
P3.7	RD	External Data Memory Read Strobe

Port 3 also receives some control signals for EPROM programming and program verification.

RESET: Reset input. A logic high on this pin for two machine cycles while the oscillator is running resets the device. An internal pulldown resistor permits a power-on reset to be generated using only an external capacitor to V_{CC} .

ALE/PROG (EPROM Only): Address Latch Enable output signal for latching the low byte of the address during accesses to external memory. This pin is also the program pulse input ($\overline{PROG}$) during EPROM programming.

In normal operation ALE is emitted at a constant rate of 1/6 the oscillator frequency, and may be used for external timing or clocking purposes. Note, however, that one ALE pulse is skipped during each access to external Data Memory.

PSEN: Program Store Enable is the Read strobe to External Program Memory. When the 87C51/80C51BH is executing from Internal Program Memory, PSEN is inactive (high). When the device is executing code from External Program Memory, PSEN is activated twice each machine cycle, except that two PSEN activations are skipped during each access to External Data Memory.

$\overline{EA}/V_{pp}$: External Access enable. $\overline{EA}$ must be strapped to V_{SS} in order to enable the 87C51/80C51BH to fetch code from External Program Memory locations starting at 0000H up to 0FFFFH. [Note, however, that if either of the Lock Bits is programmed, the logic level at $\overline{EA}$ is internally latched during reset.] (EPROM only.)

$\overline{EA}$ must be strapped to V_{CC} for internal program execution.

V_{pp} (EPROM Only): This pin also receives the 12.75V programming supply voltage (V_{pp}) during EPROM programming.

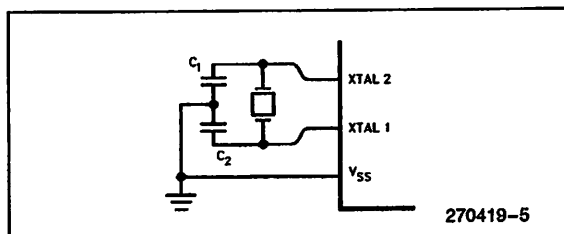


Figure 4. Using the On-Chip Oscillator

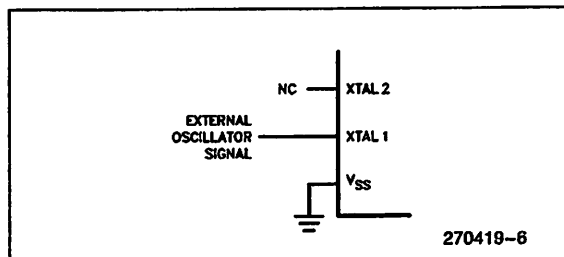


Figure 5. External Clock Drive

XTAL1: Input to the inverting oscillator amplifier and input to the internal clock generating circuits.

XTAL2: Output from the inverting oscillator amplifier.

OSCILLATOR CHARACTERISTICS

XTAL1 and XTAL2 are the input and output, respectively, of an inverting amplifier which can be configured for use as an on-chip oscillator, as shown in Figure 4.

To drive the device from an external clock source, XTAL1 should be driven, while XTAL2 is left unconnected, as shown in Figure 5. There are no requirements on the duty cycle of the external clock signal, since the input to the internal clocking circuitry is through a divide-by-two flip-flop, but minimum and maximum high and low times specified on the Data-sheet must be observed.

IDLE MODE

In Idle Mode, the CPU puts itself to sleep while all the on-chip peripherals remain active. The mode is invoked by software. The content of the on-chip RAM and all the Special Functions Registers remain unchanged during this mode. The Idle Mode can be terminated by any enabled interrupt or by a hardware reset.

It should be noted that when Idle is terminated by a hardware reset, the device normally resumes program execution, from where it left off, up to two machine cycles before the internal reset algorithm takes control. On-chip hardware inhibits access to



Table 2. Status of the External Pins During Idle and Power Down

Mode	Program Memory	ALE	$\overline{\text{PSEN}}$	PORT0	PORT1	PORT2	PORT3
Idle	Internal	1	1	Data	Data	Data	Data
Idle	External	1	1	Float	Data	Address	Data
Power Down	Internal	0	0	Data	Data	Data	Data
Power Down	External	0	0	Float	Data	Data	Data

NOTE:
For more detailed information on the reduced power modes refer to current Embedded Applications Handbook, and Application Note AP-252, "Designing with the 80C51BH."

internal RAM in this event, but access to the port pins is not inhibited. To eliminate the possibility of an unexpected write to a port pin when Idle is terminated by reset, the instruction following the one that invokes Idle should not be one that writes to a port pin or to external memory.

POWER DOWN MODE

In the Power Down mode the oscillator is stopped, and the instruction that invokes Power Down is the last instruction executed. The on-chip RAM and Special Function Registers retain their values until the Power Down mode is terminated.

The only exit from Power Down is a hardware reset. Reset redefines the SFRs but does not change the on-chip RAM. The reset should not be activated before V_{CC} is restored to its normal operating level and must be held active long enough to allow the oscillator to restart and stabilize.

DESIGN CONSIDERATIONS

- At power on, the voltage on V_{CC} and RST must come up at the same time for a proper start-up.
- Before entering the Power Down mode the contents of the Carry Bit and B.7 must be equal.
- When the Idle mode is terminated by a hardware reset, the device normally resumes program execution, from where it left off, up to two machine cycles before the internal reset algorithm takes control. On-chip hardware inhibits access to internal RAM in this event, but access to the port pins in not inhibited. To eliminate the possibility of an unexpected write when Idle is terminated by reset, the instruction following the one that invokes Idle should not be one that writes to a port pin or to external memory.
- An external oscillator may encounter as much as a 100 pF load at XTAL1 when it starts up. This is due to interaction between the amplifier and its feedback capacitance. Once the external signal meets the V_{IL} and V_{IH} specifications the capacitance will not exceed 20 pF.
- For EPROM versions exposure to light when the device is in operation may cause logic errors. For this reason, it is suggested that an opaque label be placed over the window when the die is exposed to ambient light.





PROGRAM MEMORY LOCK
(EPROM Only)

The 87C51 contains two program memory lock schemes: Encrypted Verify and Lock Bits.

Encrypted Verify: The 87C51 implements a 32-byte EPROM array that can be programmed by the customer, and which can then be used to encrypt the program code bytes during EPROM verification. The EPROM verification procedure is performed as usual, except that each code byte comes out logically X-NORed with one of the 32 key bytes. The key bytes are gone through in sequence. Therefore, to read the ROM code, one has to know the 32 key bytes in their proper sequence.

Lock Bits: Also on the chip are two Lock Bits which can be left unprogrammed (U) or can be programmed (P) to obtain the following additional features:

Bit 1	Bit 2	Additional Features
U	U	none
P	U	- Externally fetched code can not access internal Program Memory. - Further programming disabled.
U	P	(Reserved for Future definition.)
P	P	- Externally fetched code can not access internal Program Memory. - Further programming disabled. - Program verification is disabled.

When Lock Bit 1 is programmed, the logic level at the EA pin is sampled and latched during reset. If the device is powered up without a reset, the latch initializes to a random value, and holds that value until reset is activated. It is necessary that the latched value of EA be in agreement with the current logic level at that pin in order for the device to function properly.

ONCE MODE

The ONCE ("on-circuit emulation") mode facilitates testing and debugging of systems using the 87C51 without the 87C51 having to be removed from the circuit. The ONCE mode is invoked by:

1. Pull ALE low while the device is in reset and PSEN is high;
2. Hold ALE low as RST is deactivated.

While the device is in ONCE mode, the Port 0 pins go into a float state, and the other port pins and ALE and PSEN are weakly pulled high. The oscillator circuit remains active. While the 87C51 is in this mode, an emulator or test CPU can be used to drive the circuit. Normal operation is restored when a normal reset is applied.

ABSOLUTE MAXIMUM RATINGS*

Ambient Temperature Under Bias – 40°C to + 125°C
 Storage Temperature – 65°C to + 150°C
 Voltage on $\overline{EA}/V_{PP}$ Pin to V_{SS} 0V to + 13.0V
 Voltage on Any Other Pin to V_{SS} .. – 0.5V to + 6.5V
 I_{OL} per I/O pin 15 mA
 Power Dissipation..... 1.5W
 (Based on package heat transfer limitations, not device power consumption).
 Typical Junction Temperature (T_J) + 135°C
 (Based upon ambient temperature at + 125°C)
 Typical Thermal Resistance Junction-to-Ambient (θ_{JA}):
 PDIP 75°C/W
 PLCC..... 46°C/W

NOTICE: This is a production data sheet. The specifications are subject to change without notice.

**WARNING: Stressing the device beyond the "Absolute Maximum Ratings" may cause permanent damage. These are stress ratings only. Operation beyond the "Operating Conditions" is not recommended and extended exposure beyond the "Operating Conditions" may affect device reliability.*

DC CHARACTERISTICS:

(T_A = – 40°C to + 125°C; V_{CC} = 5V $\pm$ 10% (5V $\pm$ 20% EPROM Only); V_{SS} = 0V)

Symbol	Parameter	Min	Typ(1)	Max (87C51/80C51BH)	Unit	Test Conditions
V_{IL}	Input Low Voltage (Except $\overline{EA}$)	– 0.5		$0.2 V_{CC} - 0.25$	V	
V_{IL1}	Input Low Voltage to $\overline{EA}$	0		$0.2 V_{CC} - 0.45$	V	
V_{IH}	Input High Voltage (Except XTAL1, RST)	$0.2 V_{CC} + 1.0$		$V_{CC} + 0.5$	V	
V_{IH1}	Input High Voltage (XTAL1, RST)	$0.7 V_{CC} + 0.1$		$V_{CC} + 0.5$	V	
V_{OL}	Output Low Voltage (Ports 1, 2, 3)			0.45(7)	V	$I_{OL} = 1.6 \text{ mA}^{(2)}$
V_{OL1}	Output Low Voltage (Port 0, ALE, $\overline{PSEN}$)			0.45(7)	V	$I_{OL} = 3.2 \text{ mA}^{(2)}$
V_{OH}	Output High Voltage (Ports 1, 2, 3, ALE, $\overline{PSEN}$)	2.4			V	$I_{OH} = -60 \mu\text{A}$
		$0.9 V_{CC}$			V	$I_{OH} = -10 \mu\text{A}$
V_{OH1}	Output High Voltage (Port 0 in External Bus Mode)	2.4			V	$I_{OH} = -800 \mu\text{A}$
		$0.9 V_{CC}$			V	$I_{OH} = -80 \mu\text{A}^{(3)}$
I_{IL}	Logical 0 Input Current (Ports 1, 2, 3)			– 75	μA	$V_{IN} = 0.45 \text{ V}$
I_{TL}	Logical 1-to-0 transition current (Ports 1, 2, 3)			– 750	μA	(4)
I_{LI}	Input Leakage Current (Port 0)			± 10	μA	$V_{IN} = V_{IL} \text{ or } V_{IH}$
I_{CC}	Power Supply Current: Active Mode @ 12 MHz (5) Idle Mode @ 12 MHz (5) Power Down Mode		11.5	25/20	mA	(6) $V_{CC} = 2.2\text{V to } 5.5\text{V}$
			1.3	6/5	mA	
			3	100/75	μA	
RRST	Internal Reset Pulldown Resistor	50		300	K Ω	
CIO	Pin Capacitance			10	pF	

NOTES:

1. "Typicals" are based on a limited number of samples taken from early manufacturing lots and are not guaranteed. The values listed are at room temp, 5V.
2. Capacitive loading on Ports 0 and 2 may cause spurious noise pulses to be superimposed on the V_{OL} s of ALE and Ports 1 and 3. The noise is due to external bus capacitance discharging into the Port 0 and Port 2 pins when these pins make 1-to-0 transitions during bus operations. In the worst cases (capacitive loading > 100pF), the noise pulse on the ALE pin may exceed 0.8V. In such cases it may be desirable to qualify ALE with a Schmitt Trigger, or use an address latch with a Schmitt Trigger STROBE input.
3. Capacitive loading on Ports 0 and 2 may cause the V_{OH} on ALE and $\overline{PSEN}$ to momentarily fall below the $0.9 V_{CC}$ specification when the address bits are stabilizing.

NOTES: (Continued)

4. Pins of Ports 1, 2 and 3 source a transition current when they are being externally driven from 1 to 0. The transition current reaches its maximum value when V_{IN} is approximately 2V.

5. $ICCMAX$ at other frequencies is given by:

Active Mode: 87C51 $ICCMAX = 0.94 \times FREQ + 13.71$

80C51BH $ICCMAX = 1.47 \times FREQ + 2.36$

Idle Mode: $ICCMAX = 0.14 \times FREQ + 3.81$

where $FREQ$ is the external oscillator frequency in MHz. $ICCMAX$ is given in mA. See Figure 6.

3. See Figures 7 through 10 for I_{CC} test conditions. Minimum V_{CC} for Power Down is 2.0V.

7. Under steady state (non-transient) conditions, I_{OL} must be externally limited as follows:

Maximum I_{OL} per port pin:

10 mA

Maximum I_{OL} per 8-bit port

Port 0: 26 mA

Ports 1, 2, and 3: 15 mA

Maximum total I_{OL} for all output pins:

71 mA

If I_{OL} exceeds the test condition, V_{OL} may exceed the related specification. Pins are not guaranteed to sink current greater than the listed test conditions.

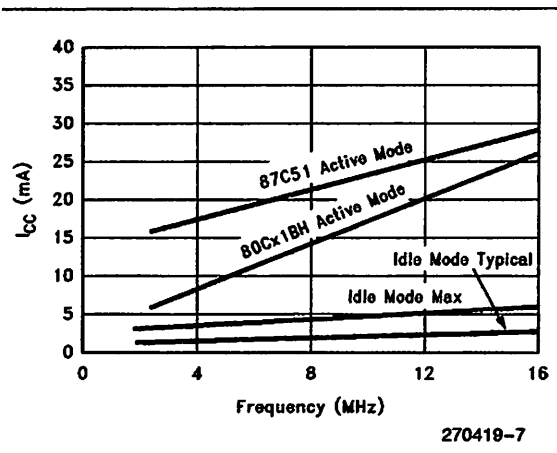


Figure 6. I_{CC} vs. $FREQ$. Valid only within frequency specifications of the device under test.

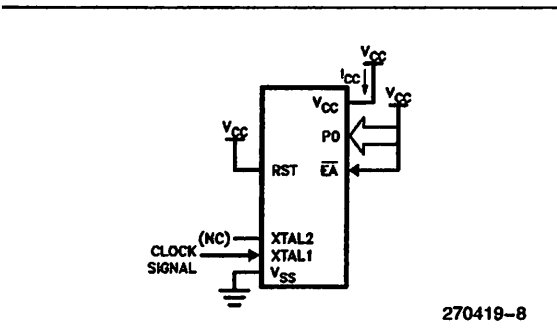


Figure 7. I_{CC} Test Condition, Active Mode. All other pins are disconnected.

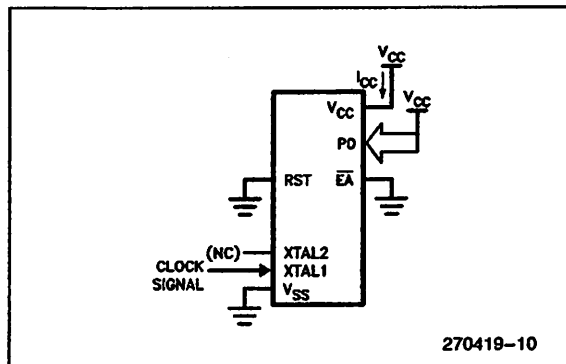


Figure 8. I_{CC} Test Condition, Idle Mode. All other pins are disconnected.

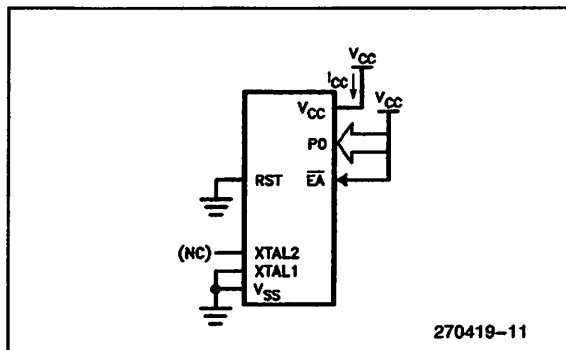


Figure 9. I_{CC} Test Condition, Power Down Mode. All other pins are disconnected.

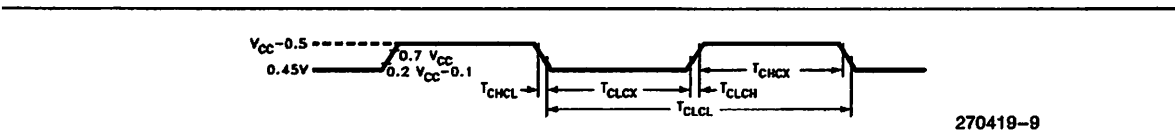


Figure 10. Clock Signal Waveform for I_{CC} tests in Active and Idle Modes. $T_{CHCL} = T_{CHCL} = 5$ ns.



EXPLANATION OF THE AC SYMBOLS

Each timing symbol has 5 characters. The first character is always a 'T' (stands for time). The other characters, depending on their positions, stand for the name of a signal or the logical status of that signal. The following is a list of all the characters and what they stand for.

- A:Address.
- C:Clock.
- D:Input data.
- H:Logic level HIGH.
- I:Instruction (program memory contents).

- L:Logic level LOW, or ALE.
- P:PSEN.
- Q:Output data.
- R:RD signal.
- T:Time.
- V:Valid.
- W:WR signal.
- X:No longer a valid logic level.
- Z:Float.

For example,

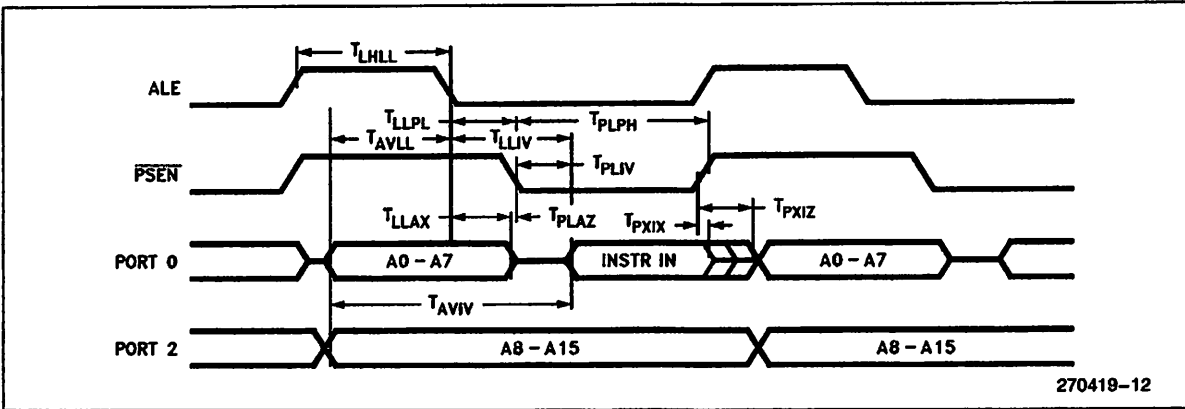
- T_{AVLL} = Time from Address Valid to ALE Low.
- T_{LLPL} = Time from ALE Low to PSEN Low.

AC CHARACTERISTICS: (T_A = -40°C to +125°C; V_{CC} = 5V ±10% (5V ±20% EPROM Only); V_{SS} = 0V; Load Capacitance for Port 0, ALE, and PSEN = 100 pF; Load Capacitance for All Other Outputs = 80 pF)

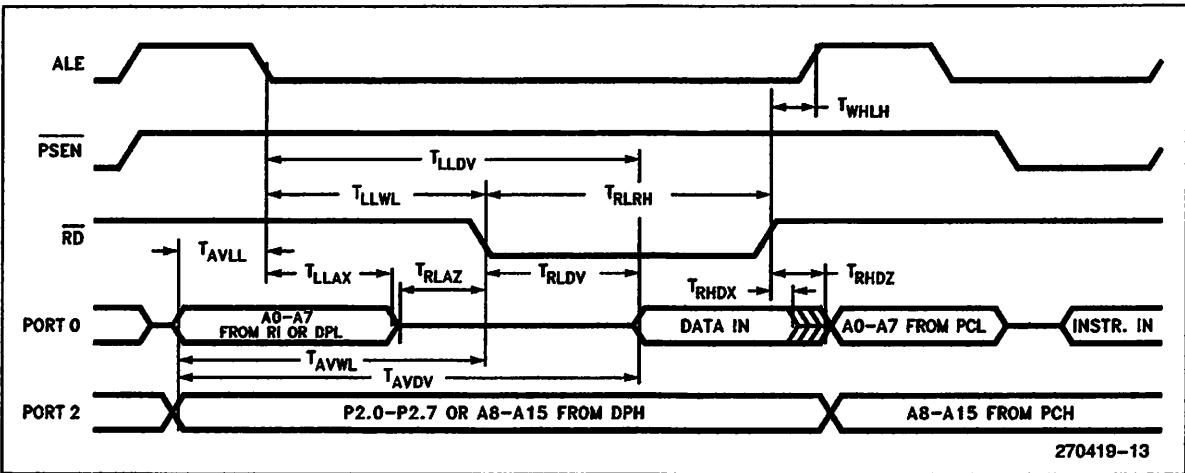
EXTERNAL PROGRAM AND DATA MEMORY CHARACTERISTICS

Symbol	Parameter	12 MHz Osc		Variable Oscillator		Units
		Min	Max	Min	Max	
1/T _{CLCL}	Oscillator Frequency 87C51/80C51BH/80C31BH			3.5	12-16	MHz
T _{LHLL}	ALE Pulse Width	127		2T _{CLCL} - 40		ns
T _{AVLL}	Address Valid to ALE Low	28		T _{CLCL} - 55		ns
T _{LLAX}	Address Hold After ALE Low	48		T _{CLCL} - 35		ns
T _{LLIV}	ALE Low to Valid Instr In		224		4T _{CLCL} - 110	ns
T _{LLPL}	ALE Low to PSEN Low	43		T _{CLCL} - 40		ns
T _{PLPH}	PSEN Pulse Width	205		3T _{CLCL} - 45		ns
T _{PLIV}	PSEN Low to Valid Instr In		135		3T _{CLCL} - 115	ns
T _{PXIX}	Input Instr Hold After PSEN	0		0		ns
T _{PXIZ}	Input Instr Float After PSEN		59		T _{CLCL} - 25	ns
T _{AVIV}	Address Valid to Valid Instr In		312		5T _{CLCL} - 105	ns
T _{PLAZ}	PSEN Low to Address Float		10		10	ns
T _{RLRH}	RD Pulse Width	400		6T _{CLCL} - 100		ns
T _{WLWH}	WR Pulse Width	400		6T _{CLCL} - 100		ns
T _{RLDV}	RD Low to Valid Data In		252		5T _{CLCL} - 165	ns
T _{RHDX}	Data Hold After RD High	0		0		ns
T _{RHDZ}	Data Float After RD High		97		2T _{CLCL} - 70	ns
T _{LLDV}	ALE Low to Valid Data In		517		8T _{CLCL} - 150	ns
T _{AVDV}	Address Valid to Valid Data In		585		9T _{CLCL} - 165	ns
T _{LLWL}	ALE Low to RD or WR Low	200	300	3T _{CLCL} - 50	3T _{CLCL} + 50	ns
T _{AVWL}	Address Valid to RD or WR Low	203		4T _{CLCL} - 130		ns
T _{QVWX}	Data Valid to WR Transition	23		T _{CLCL} - 60		ns
T _{WHQX}	Data Hold After WR High	33		T _{CLCL} - 50		ns
T _{RLAZ}	RD Low to Address Float		0		0	ns
T _{WHLH}	RD or WR High to ALE High	43	123	T _{CLCL} - 40	T _{CLCL} + 40	ns

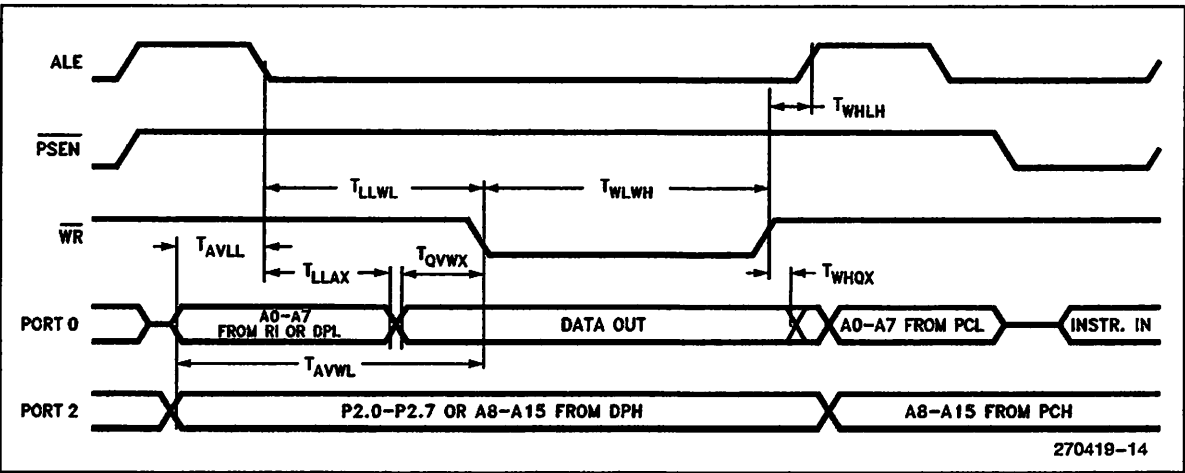
EXTERNAL PROGRAM MEMORY READ CYCLE



EXTERNAL DATA MEMORY READ CYCLE



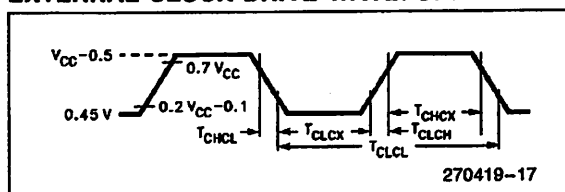
EXTERNAL DATA MEMORY WRITE CYCLE



EXTERNAL CLOCK DRIVE

Symbol	Parameter	Min	Max	Units
1/T _{CLCL}	Oscillator Frequency	3.5 3.5	12 16	MHz
T _{CHCX}	High Time	20		ns
T _{CLCX}	Low Time	20		ns
T _{CLCH}	Rise Time		20	ns
T _{CHCL}	Fall Time		20	ns

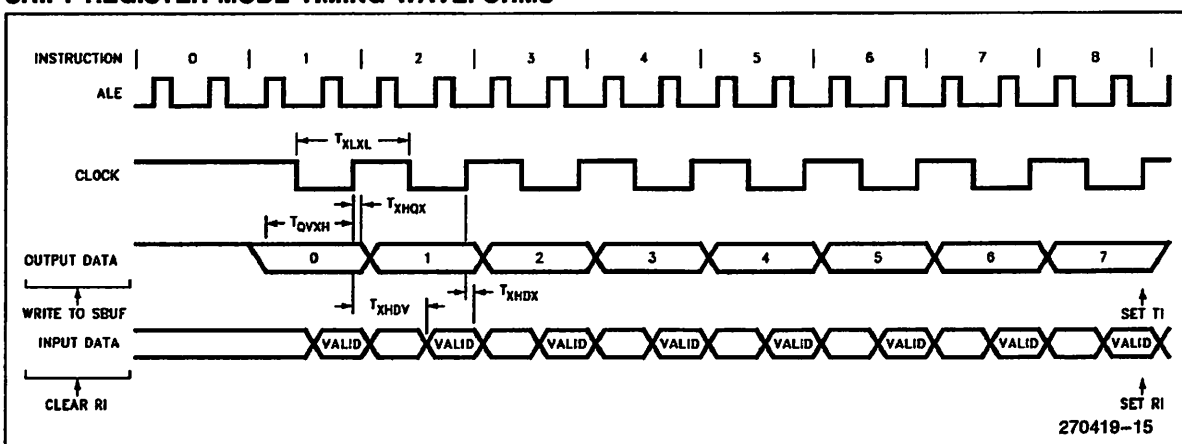
EXTERNAL CLOCK DRIVE WAVEFORM



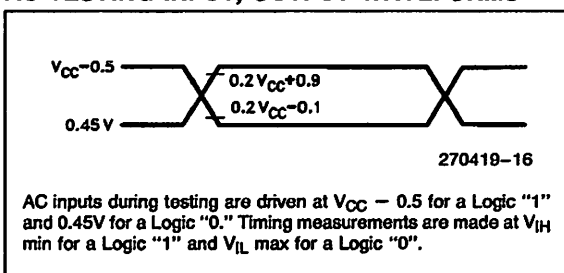
SERIAL PORT TIMING—SHIFT REGISTER MODE

Symbol	Parameter	12 MHz Oscillator		Variable Oscillator		Units
		Min	Max	Min	Max	
T _{XLXL}	Serial Port Clock Cycle Time	1.0		12T _{CLCL}		μs
T _{QVXH}	Output Data Setup to Clock Rising Edge	700		10T _{CLCL} - 133		ns
T _{XHQX}	Output Data Hold After Clock Rising Edge	50		2T _{CLCL} - 117		ns
T _{XHDX}	Input Data Hold After Clock Rising Edge	0		0		ns
T _{XHNV}	Clock Rising Edge to Input Data Valid		700		10T _{CLCL} - 133	ns

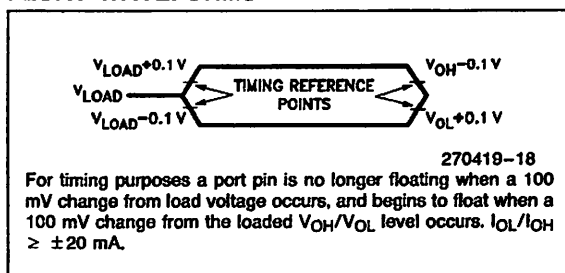
SHIFT REGISTER MODE TIMING WAVEFORMS



AC TESTING INPUT, OUTPUT WAVEFORMS



FLOAT WAVEFORMS



PROM CHARACTERISTICS (PROM Only)

The 87C51 is programmed by a modified Quick-Pulse Programming algorithm. It differs from older methods in the value used for V_{pp} (Programming Supply Voltage) and in the width and number of the ALE/PROG pulses.

The 87C51 contains two signature bytes that can be read and used by an EPROM programming system

to identify the device. The signature bytes identify the device as an 87C51 manufactured by Intel.

Table 3 shows the logic levels for reading the signature byte, and for programming the Program Memory, the Encryption Table, and the Lock Bits. The circuit configuration and waveforms for Quick-Pulse Programming are shown in Figures 11 and 12. Figure 13 shows the circuit configuration for normal Program Memory verification.

Table 3. EPROM Programming Modes

MODE	RST	PSEN	ALE/ PROG	EA/ V _{pp}	P2.7	P2.6	P3.7	P3.6
Read Signature	1	0	1	1	0	0	0	0
Program Code Data	1	0	0*	V _{pp}	1	0	1	1
Verify Code Data	1	0	1	1	0	0	1	1
Pgm Encryption Table	1	0	0*	V _{pp}	1	0	1	0
Pgm Lock Bit 1	1	0	0*	V _{pp}	1	1	1	1
Pgm Lock Bit 2	1	0	0*	V _{pp}	1	1	0	0

NOTES:

* = Valid high for that pin

" = Valid low for that pin

V_{pp} = 12.75V ± 0.25V

V_{cc} = 5V ± 20% during programming and verification

ALE/PROG receives 25 programming pulses while V_{pp} is held at 12.75V. Each programming pulse is low for 100 μs (10 μs) and high for a minimum of 10 μs.

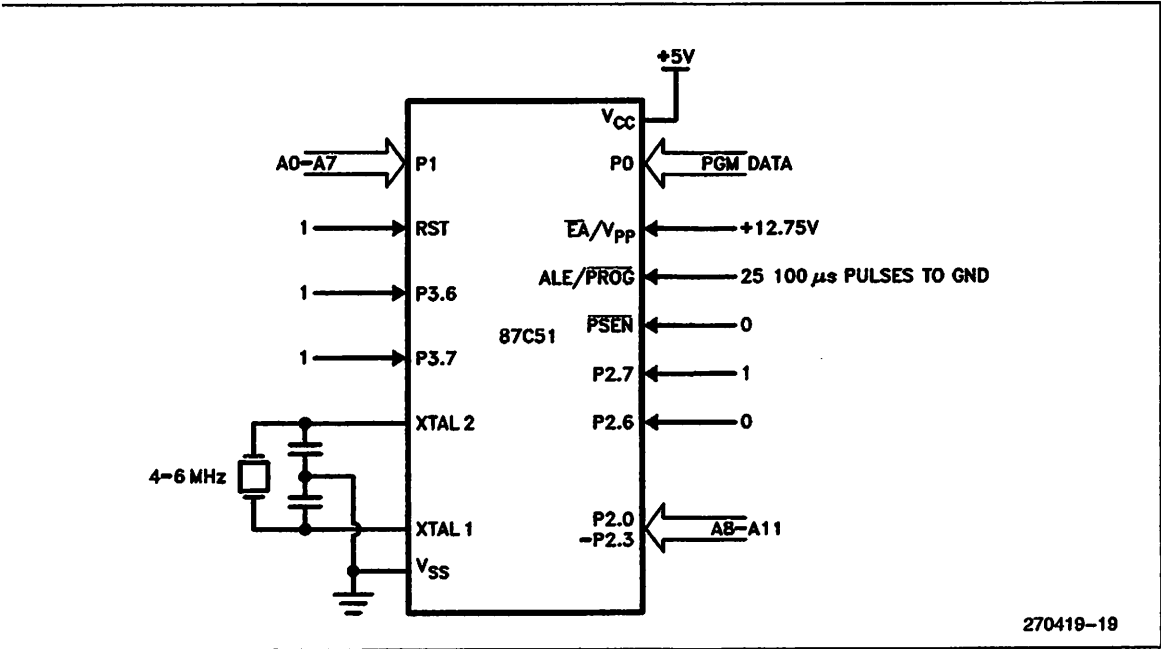


Figure 11. Programming Configuration

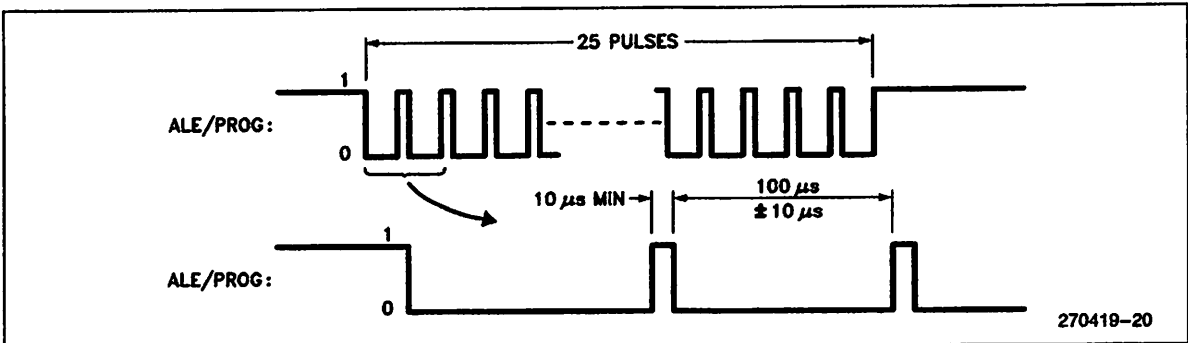


Figure 12. PROG Waveforms

Quick-Pulse Programming (EPROM Only)

The setup for Microcontroller Quick-Pulse Programming is shown in Figure 11. Note that the 87C51 is running with a 4 to 6 MHz oscillator. The reason the oscillator needs to be running is that the device is executing internal address and program data transfers.

The address of the EPROM location to be programmed is applied to Ports 1 and 2, as shown in Figure 11. The code byte to be programmed into that location is applied to Port 0. RST, PSEN, and pins of Ports 2 and 3 specified in Table 3 are held at the "Program Code Data" levels indicated in Table 2. Then ALE/PROG is pulsed low 25 times as shown in Figure 12.

To program the Encryption Table, repeat the 25-pulse programming sequence for addresses 0

through 1FH, using the "Pgm Encryption Table" levels. Don't forget that after the Encryption Table is programmed, verify cycles will produce only encrypted data.

To program the Lock Bits, repeat the 25-pulse programming sequence using the "Pgm Lock Bit" levels. After one Lock Bit is programmed, further programming of the Code Memory and Encryption Table is disabled. However, the other Lock Bit can still be programmed.

Note that the $\overline{EA}/V_{PP}$ pin must not be allowed to go above the maximum specified V_{PP} level for any amount of time. Even a narrow glitch above that voltage level can cause permanent damage to the device. The V_{PP} source should be well regulated and free of glitches and overshoot.

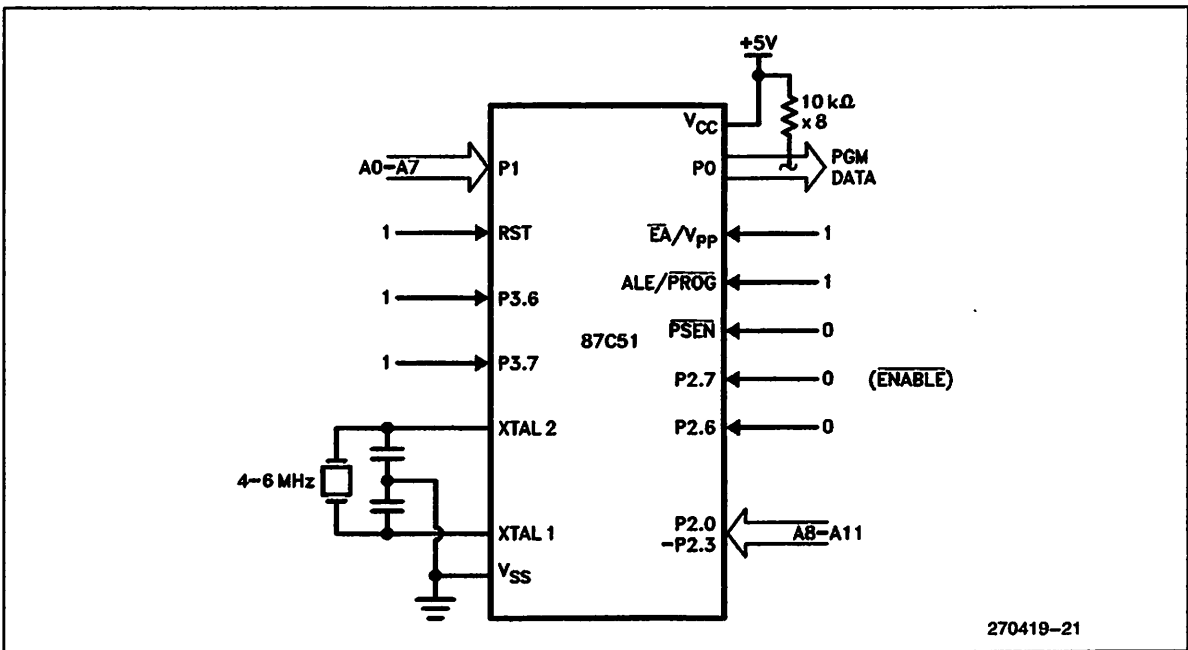


Figure 13. Program Verification



Program Verification
(EPROM Only)

If Lock Bit 2 has not been programmed, the on-chip Program Memory can be read out for program verification. The address of the Program Memory location to be read is applied to Ports 1 and 2 as shown in Figure 13. The other pins are held at the “Verify Code Data” levels indicated in Table 3. The contents of the addressed location will be emitted on Port 0. External pullups are required on Port 0 for this operation. Detailed timing specifications are shown in later sections of this datasheet.

If the Encryption Table has been programmed, the data presented at Port 0 will be the Exclusive NOR of the program byte with one of the encryption bytes. The user will have to know the Encryption Table contents in order to correctly decode the verification data. The Encryption Table itself can not be read out.

Reading the Signature Bytes
(EPROM Only)

The signature bytes are read by the same procedure as a normal verification of locations 030H and 031H, except that P3.6 and P3.7 need to be pulled to a logic low. The values returned are:

- (030H) = 89H indicates manufactured by Intel
- (031H) = 57H indicates 87C51

Program/Verify Algorithms
(EPROM Only)

Any algorithm in agreement with the conditions listed in Table 3, and which satisfies the timing specifications, is suitable.

Erasure Characteristics
(EPROM Only)

Erasure of the EPROM begins to occur when the chip is exposed to light with wavelengths shorter than approximately 4,000 Angstroms. Since sunlight and fluorescent lighting have wavelengths in this range, exposure to these light sources over an extended time (about 1 week in sunlight, or 3 years in room level fluorescent lighting) could cause inadvertent erasure. If an application subjects the device to this type of exposure, it is suggested that an opaque label be placed over the window.

The recommended erasure procedure is exposure to ultraviolet light (at 2537 Angstroms) to an integrated dose of at least 15 W-sec/cm². Exposing the EPROM to an ultraviolet lamp of 12,000 μW/cm² rating for 30 minutes, at a distance of about 1 inch, should be sufficient.

Erasure leaves the array in an all 1s state.

EPROM PROGRAMMING AND VERIFICATION CHARACTERISTICS:

(T_A = 21°C to 27°C, V_{CC} = 5V ±20%, V_{SS} = 0V)

Symbol	Parameter	Min	Max	Units
V _{PP}	Programming Supply Voltage	12.5	13.0	V
I _{PP}	Programming Supply Current		50	mA
1/T _{CLCL}	Oscillator Frequency	4	6	MHz
T _{AVGL}	Address Setup to $\overline{\text{PROG}}$ Low	48T _{CLCL}		
T _{GHAX}	Address Hold After $\overline{\text{PROG}}$	48T _{CLCL}		
T _{DVGL}	Data Setup to $\overline{\text{PROG}}$ Low	48T _{CLCL}		
T _{GHDX}	Data Hold After $\overline{\text{PROG}}$	48T _{CLCL}		
T _{ESHSH}	P2.7 ($\overline{\text{ENABLE}}$) High to V _{PP}	48T _{CLCL}		
T _{SHGL}	V _{PP} Setup to $\overline{\text{PROG}}$ Low	10		μs
T _{GHSL}	V _{PP} Hold After $\overline{\text{PROG}}$	10		μs
T _{GLGH}	$\overline{\text{PROG}}$ Width	90	110	μs
T _{AVQV}	Address to Data Valid		48T _{CLCL}	
T _{ELQV}	$\overline{\text{ENABLE}}$ Low to Data Valid		48T _{CLCL}	
T _{EHQZ}	Data Float After $\overline{\text{ENABLE}}$	0	48T _{CLCL}	
T _{GHGL}	$\overline{\text{PROG}}$ High to $\overline{\text{PROG}}$ Low	10		μs

The diagram illustrates the timing for the 270418-22 device, divided into two main phases: PROGRAMMING and VERIFICATION.

PROGRAMMING Phase:

- P1.0-P1.7 and P2.0-P2.3:** These lines provide the ADDRESS.
- PORT 0:** Provides DATA IN. It shows 25 PULSES.
- ALE/PROG:** This signal is active during programming. It shows a series of pulses. Key timing parameters include:
 - T_{OVGL} : Overlap time from address to data.
 - T_{AVGL} : Average pulse width.
 - T_{GHDX} and T_{GHAX} : High-level pulse widths.
 - T_{SHGL} : Setup time before the first pulse.
 - T_{GLGH} : Pulse period.
 - T_{GHGL} : High-level pulse width.
 - T_{OVSL} : Overlap time after the last pulse.
- EA/V_{pp}:** This signal is driven to LOGIC 1 during programming.
- P2.7 (ENABLE):** This signal is active (low) during programming. Key timing parameters include:
 - T_{DSH} : Delay from enable to start of programming.
 - T_{ELOY} : Delay from enable to end of programming.

VERIFICATION Phase:

- P1.0-P1.7 and P2.0-P2.3:** These lines provide the ADDRESS.
- PORT 0:** Provides DATA OUT.
- ALE/PROG:** This signal is active during verification. Key timing parameters include:
 - T_{AVQV} : Average pulse width.
- EA/V_{pp}:** This signal is driven to LOGIC 1 during verification.
- P2.7 (ENABLE):** This signal is active (low) during verification. Key timing parameters include:
 - T_{EHQZ} : Delay from enable to end of verification.

Timing Parameters:

- T_{OVGL} : Overlap time from address to data.
- T_{AVGL} : Average pulse width.
- T_{GHDX} and T_{GHAX} : High-level pulse widths.
- T_{SHGL} : Setup time before the first pulse.
- T_{GLGH} : Pulse period.
- T_{GHGL} : High-level pulse width.
- T_{OVSL} : Overlap time after the last pulse.
- T_{DSH} : Delay from enable to start of programming.
- T_{ELOY} : Delay from enable to end of programming.
- T_{AVQV} : Average pulse width.
- T_{EHQZ} : Delay from enable to end of verification.

Logic Levels:

- LOGIC 1:** High level.
- LOGIC 0:** Low level.

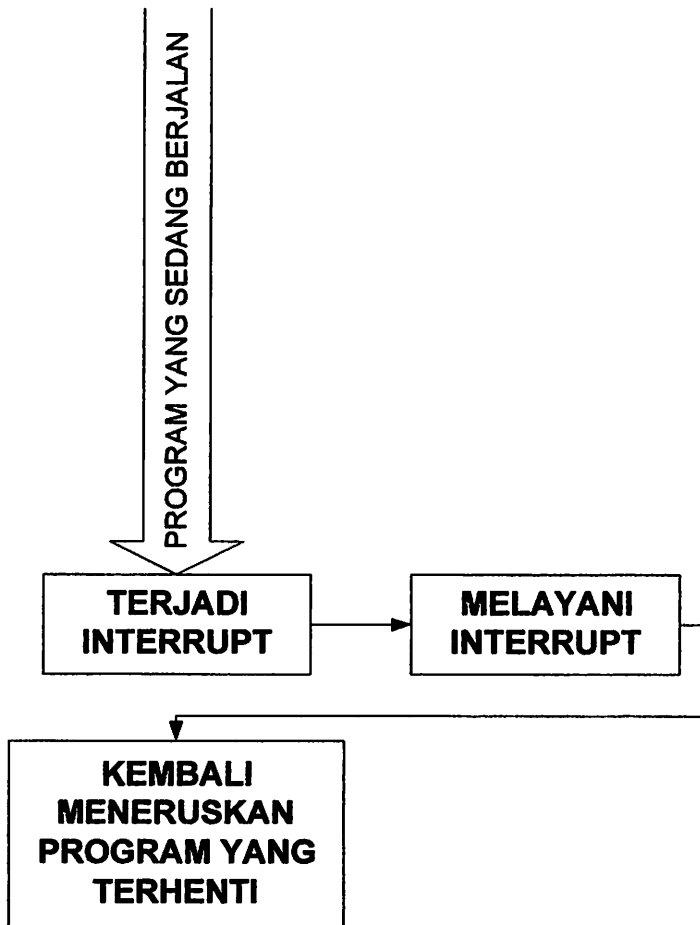
270418-22

1. Maximum I_{OL} per I/O pin added.
2. Note 7 on Maximum Current Specifications added to DC Characteristics.
3. Datasheet Revision Summary added.

1. Interrupt

Interrupt adalah suatu kejadian atau peristiwa yang menyebabkan mikrokontroler berhenti sejenak untuk melayani interrupt tersebut. Program yang dijalankan pada saat melayani interrupt disebut **Interrupt Service Routine**. Analoginya adalah sebagai berikut, seseorang sedang mengetik laporan, mendadak telephone berdering dan menginterruptsi orang tersebut sehingga menghentikan pekerjaan mengetik dan mengangkat telephone. Setelah pembicaraan telephone yang dalam hal ini adalah merupakan analogi dari Interrupt Service Routine selesai maka orang tersebut kembali meneruskan pekerjaannya mengetik.

Demikian pula pada sistem mikrokontroler yang sedang menjalankan programnya, saat terjadi interrupt, program akan berhenti sesaat, melayani interrupt tersebut dengan menjalankan program yang berada pada alamat yang ditunjuk oleh vektor dari interrupt yang terjadi hingga selesai dan kembali meneruskan program yang terhenti oleh interrupt tadi. Seperti yang terlihat Gambar 4.1, sebuah program yang seharusnya berjalan terus lurus, tiba-tiba terjadi interrupt dan harus melayani interrupt tersebut terlebih dahulu hingga selesai sebelum ia kembali meneruskan pekerjaannya.



Gambar 4.1
Interrupt

Proses yang dilakukan oleh mikrokontroler saat melayani interrupt adalah sebagai berikut:

Proses yang terjadi saat mikrokontroler melayani interrupt adalah sebagai berikut:

- Instruksi terakhir yang sedang dijalankan diselesaikan terlebih dahulu
- Program Counter (alamat dari instruksi yang sedang berjalan) disimpan ke stack
- Interrupt Status disimpan secara internal
- Interrupt dilayani sesuai peringkat dari interrupt (lihat Interrupt Priority)
- Program Counter terisi dengan alamat dari vector interrupt (lihat Interrupt Vector) sehingga mikrokontroler langsung menjalankan program yang terletak pada vector interrupt

Program pada vector interrupt biasanya diakhiri dengan instruksi RETI di mana pada saat ini proses yang terjadi pada mikrokontroler adalah sebagai berikut:

- Program Counter diisi dengan alamat yang tersimpan dalam stack pada saat interrupt terjadi sehingga mikrokontroler kembali meneruskan program di lokasi saat interrupt terjadi
- Interrupt Status dikembalikan ke kondisi terakhir sebelum terjadi interrupt

4.1. Enable Interrupt

Dalam suatu kondisi dapat juga dibutuhkan suatu program yang sedang berjalan tidak boleh diinterrupt, untuk itu 89C51 mempunyai lima buah interrupt yang masing-masing dapat dienable ataupun disable satu per satu. Pengaturan enable dan disable interrupt dilakukan pada Register Interrupt Enable yang terletak pada alamat A8H.

A8H	EA			ES	ET1	EX1	ET0	EX0
	IE.7			IE.4	IE.3	IE.2	IE.1	IE.0

EA: Disable semua interrupt apabila bit ini clear. Bila bit ini clear, maka apapun kondisi bit lain dalam register ini, semua interrupt tidak akan dilayani, oleh karena itu untuk mengaktifkan salah satu interrupt, bit ini harus set

ES: Enable/disable Serial Port Interrupt, set = enable, clear = disable
Apabila Serial Port Interrupt aktif maka interrupt akan terjadi setiap ada data yang masuk ataupun keluar melalui serial port yang membuat Flag RI (Receive Interrupt Flag) ataupun TI (Transmit Interrupt Flag).

ET1: Enable/disable Timer 1 Interrupt, set = enable, clear = disable
Apabila interrupt ini enable maka interrupt akan terjadi pada saat Timer 1 overflow.

EX1: Enable/disable External Interrupt 1, set = enable, clear = disable
Apabila interrupt ini enable maka interrupt akan terjadi pada saat terjadi pulsa low pada INT1

ET0: Enable/disable Timer 0 Interrupt, set = enable, clear = disable

Apabila interrupt ini enable maka interrupt akan terjadi pada saat Timer 0 overflow.

EX0: Enable/disable External Interrupt 0, set = enable, clear = disable
Apabila interrupt ini enable maka interrupt akan terjadi pada saat terjadi pulsa low pada INT0

4.2. Status Interrupt

Status-status interrupt dari 89C51 terletak pada Register TCON yaitu

INT0: Bit IE0, clear oleh hardware saat interrupt terjadi pada mode aktif level

INT1: Bit IE1, clear oleh hardware saat interrupt terjadi pada mode aktif level

Timer 0: Bit TF0, clear oleh hardware saat interrupt terjadi

Timer 1 : Bit TF1, clear oleh hardware saat interrupt terjadi

Serial Port (TXD) : Bit TI, clear oleh software

Serial Port (RXD) : Bit RI, clear oleh software

External Interrupt 0 maupun External Interrupt 1 dapat diatur menjadi aktif level maupun aktif transisi dengan mengubah bit IT0 atau IT1 pada Register TCON

External Interrupt akan bekerja secara aktif level bila bit ITx (x = 0 untuk INT0 dan x = 1 untuk INT1) berkondisi low dan bekerja secara aktif transisi bila bit ITx berkondisi high.

4.3. Interrupt Priority

Dalam melayani interrupt, mikrokontroler bekerja berdasarkan prioritas yang dapat diatur pada Register Interrupt Priority.

IP0 atau PX0 untuk External Interrupt 0

IP1 atau PT0 untuk Timer 0 Interrupt

IP2 atau PX1 untuk External Interrupt 1

IP3 atau PT1 untuk Timer 1 Interrupt

IP4 atau PS untuk Serial Interrupt

Bit-bit ini akan berkondisi set apabila interrupt yang diaturnya ditempatkan pada prioritas yang tinggi. Interrupt dengan prioritas yang tinggi dapat meng-interrupt interrupt lain yang mempunyai prioritas lebih rendah, sedangkan interrupt dengan prioritas tinggi itu sendiri tidak dapat di interrupt oleh interrupt lain.

Apabila terjadi lebih dari satu interrupt yang mempunyai prioritas yang sama secara bersamaan, maka prioritas akan diatur secara *polling* mulai dari:

- External Interrupt 0
- Timer 0 Interrupt
- External Interrupt 1
- Timer 1 Interrupt
- Serial Interrupt

4.3. Interrupt Vector

Interrupt Vector adalah harga yang disimpan ke Program Counter pada saat terjadi interrupt sehingga program akan menuju ke alamat yang ditunjukkan oleh Program Counter. Pada saat program menuju ke alamat yang ditunjuk oleh Interrupt Vector maka flag-flag yang set karena terjadinya interrupt akan di-clear kecuali RI dan TI.

Kelima interrupt dan system reset dari 89C51 mempunyai Vector masing-masing yang dapat dilihat pada Tabel 4.1

Table 4.1
Interrupt Vector

INTERRUPT	FLAG	ALAMAT VEKTOR
System Reset	RST	0000H
External Interrupt 0	I E0	0003H
Timer 0	TF0	000BH
External Interrupt 1	I E1	0013H
Timer 1	TF1	001BH
Serial Port	RI atau TI	0023H

Masing-masing alamat vektor mempunyai jarak yang berdekatan sehingga akan timbul masalah bila diperlukan sebuah Interrupt Service Routine yang cukup panjang, misalnya hendak digunakan External Interrupt 0 dan Timer 0 dalam satu sistem, maka bila Interrupt Service Routine untuk External Interrupt 0 diletakkan pada alamat 0003H dan Interrupt Service Routine untuk Timer 0 diletakkan pada alamat 000BH akan terjadi bentrok alamat antara kedua Interrupt Service Routine ini apabila tidak dilakukan suatu trik berikut yang terlihat pada listing berikut.

```
Listing 4.1
ORG 0000H
LJMP Start
ORG 0003H
LJMP Int0
ORG 000BH
LJMP Timer0
.....
.....
.....
Start:
.....
..... ;Main Program
.....

Int0:
.....
..... ;Int0 ISR
.....
RETI

Timer0:
.....
..... ;Timer 0 ISR
.....
RETI
```

Jadi pada listing ini, saat terjadi interrupt Program Counter memang tetap berisi nilai dari Interrupt Vector sehingga program juga meloncat ke alamat tersebut, namun karena di alamat tersebut sudah diletakkan instruksi untuk meloncat ke label yang lain seperti Int0 untuk External Interrupt 0 Service Routine maka tidak akan terjadi bentrok alamat antara kedua Interrupt Service Routine ini.

LM567/LM567C Tone Decoder

General Description

The LM567 and LM567C are general purpose tone decoders designed to provide a saturated transistor switch to ground when an input signal is present within the passband. The circuit consists of an I and Q detector driven by a voltage controlled oscillator which determines the center frequency of the decoder. External components are used to independently set center frequency, bandwidth and output delay.

Features

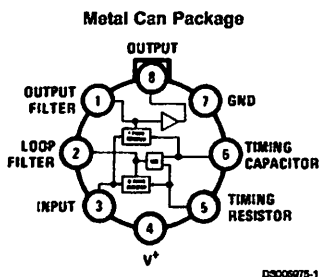
- 20 to 1 frequency range with an external resistor
- Logic compatible output with 100 mA current sinking capability
- Bandwidth adjustable from 0 to 14%

- High rejection of out of band signals and noise
- Immunity to false signals
- Highly stable center frequency
- Center frequency adjustable from 0.01 Hz to 500 kHz

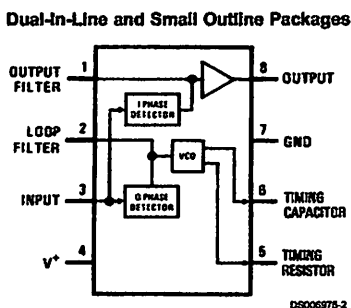
Applications

- Touch tone decoding
- Precision oscillator
- Frequency monitoring and control
- Wide band FSK demodulation
- Ultrasonic controls
- Carrier current remote controls
- Communications paging decoders

Connection Diagrams



Top View
Order Number LM567H or LM567CH
See NS Package Number H08C



Top View
Order Number LM567CM
See NS Package Number M08A
Order Number LM567CN
See NS Package Number N08E

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage Pin	9V
Power Dissipation (Note 2)	1100 mW
V_{DS}	15V
V_{S1}	-10V
V_{S2}	$V_{S1} + 0.5V$
Storage Temperature Range	-65°C to +150°C

Operating Temperature Range

LM567H	-55°C to +125°C
LM567CH, LM567CM, LM567CN	0°C to +70°C

Soldering Information

Dual-In-Line Package	
Soldering (10 sec.)	260°C
Small Outline Package	
Vapor Phase (60 sec.)	215°C
Infrared (15 sec.)	220°C

See AN-450 "Surface Mounting Methods and Their Effect on Product Reliability" for other methods of soldering surface mount devices.

Electrical Characteristics

AC Test Circuit, $T_A = 25^\circ\text{C}$, $V^+ = 5V$

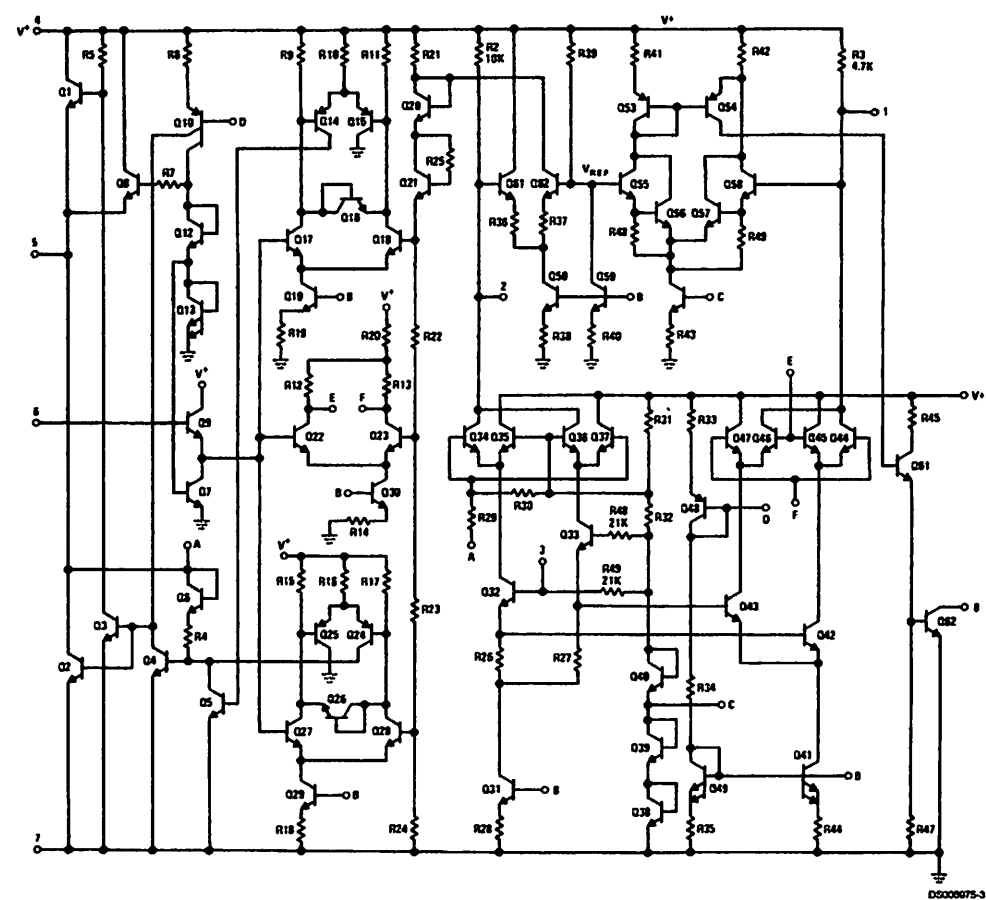
Parameters	Conditions	LM567			LM567C/LM567CM			Units
		Min	Typ	Max	Min	Typ	Max	
Power Supply Voltage Range		4.75	5.0	9.0	4.75	5.0	9.0	V
Power Supply Current Quiescent	$R_L = 20k$		6	8		7	10	mA
Power Supply Current Activated	$R_L = 20k$		11	13		12	15	mA
Input Resistance		18	20		15	20		k Ω
Smallest Detectable Input Voltage	$I_L = 100\text{ mA}$, $f_i = f_o$		20	25		20	25	mVrms
Largest No Output Input Voltage	$I_C = 100\text{ mA}$, $f_i = f_o$	10	15		10	15		mVrms
Largest Simultaneous Outband Signal to Inband Signal Ratio			6			6		dB
Minimum Input Signal to Wideband Noise Ratio	$B_n = 140\text{ kHz}$		-6			-6		dB
Largest Detection Bandwidth		12	14	16	10	14	18	% of f_o
Largest Detection Bandwidth Skew			1	2		2	3	% of f_o
Largest Detection Bandwidth Variation with Temperature			± 0.1			± 0.1		%/°C
Largest Detection Bandwidth Variation with Supply Voltage	4.75-6.75V		± 1	± 2		± 1	± 5	%V
Highest Center Frequency		100	500		100	500		kHz
Center Frequency Stability (4.75-5.75V)	$0 < T_A < 70$ $-55 < T_A < +125$		35 ± 60 35 ± 140			35 ± 60 35 ± 140		ppm/°C ppm/°C
Center Frequency Shift with Supply Voltage	4.75V-6.75V 4.75V-9V		0.5 2.0	1.0 2.0		0.4 2.0	2.0 2.0	%/V %/V
Fastest ON-OFF Cycling Rate			$f_o/20$			$f_o/20$		
Output Leakage Current	$V_{DS} = 15V$		0.01	25		0.01	25	μA
Output Saturation Voltage	$e_i = 25\text{ mV}$, $I_{DS} = 30\text{ mA}$ $e_i = 25\text{ mV}$, $I_{DS} = 100\text{ mA}$		0.2 0.6	0.4 1.0		0.2 0.6	0.4 1.0	V
Output Fall Time			30			30		ns
Output Rise Time			150			150		ns

Note 1: Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is functional, but do not guarantee specific performance limits. Electrical Characteristics state DC and AC electrical specifications under particular test conditions which guarantee specific performance limits. This assumes that the device is within the Operating Ratings. Specifications are not guaranteed for parameters where no limit is given, however, the typical value is a good indication of device performance.

Note 2: The maximum junction temperature of the LM567 and LM567C is 150°C. For operating at elevated temperatures, devices in the TO-5 package must be derated based on a thermal resistance of 150°C/W, junction to ambient or 45°C/W, junction to case. For the DIP the device must be derated based on a thermal resistance of 110°C/W, junction to ambient. For the Small Outline package, the device must be derated based on a thermal resistance of 160°C/W, junction to ambient.

Note 3: Refer to RETS567X drawing for specifications of military LM567H version.

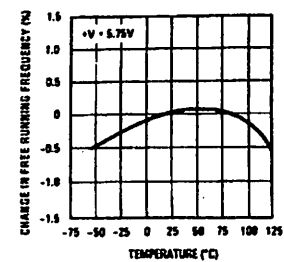
Schematic Diagram



DS000975-3

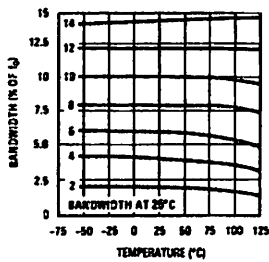
Typical Performance Characteristics

Typical Frequency Drift



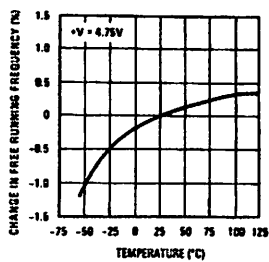
DS000975-10

Typical Bandwidth Variation



DS000975-11

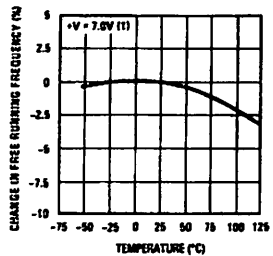
Typical Frequency Drift



DS000975-12

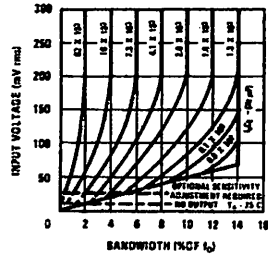
Typical Performance Characteristics (Continued)

Typical Frequency Drift



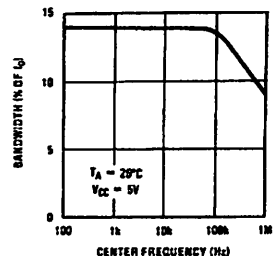
DS000975-13

Bandwidth vs Input Signal Amplitude



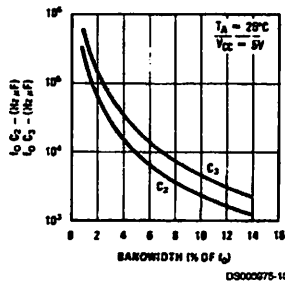
DS000975-14

Largest Detection Bandwidth



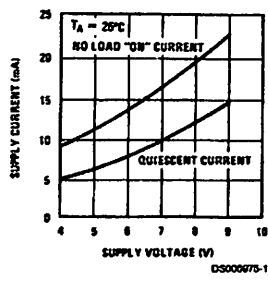
DS000975-15

Detection Bandwidth as a Function of C_2 and C_3



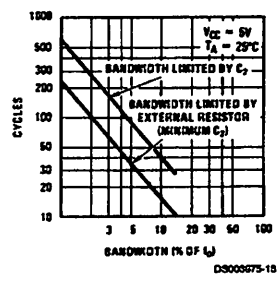
DS000975-16

Typical Supply Current vs Supply Voltage



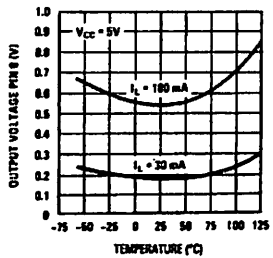
DS000975-17

Greatest Number of Cycles Before Output



DS000975-18

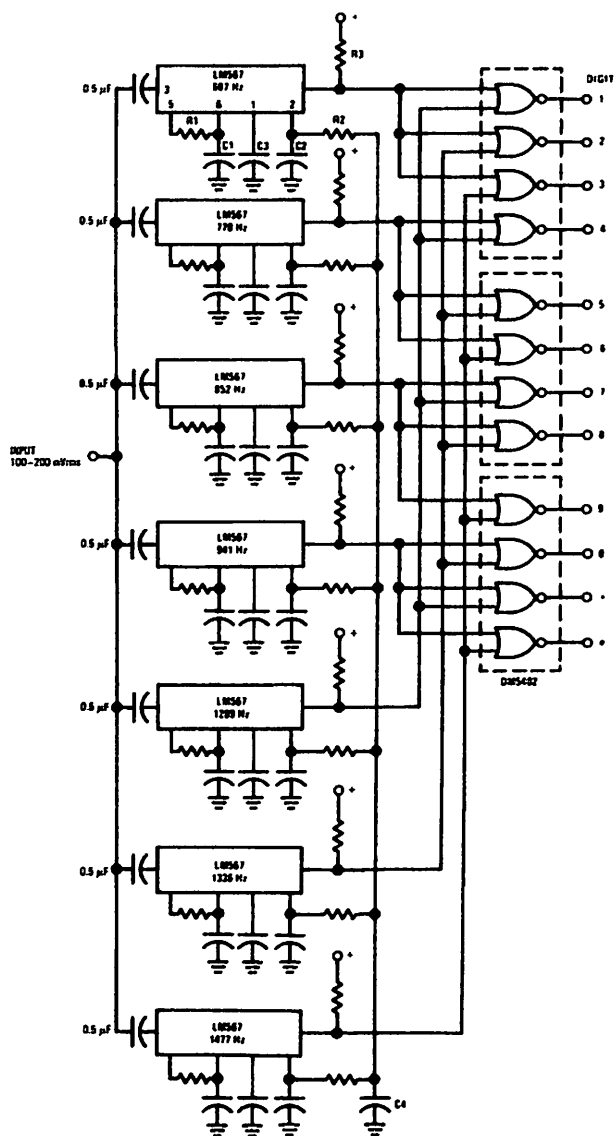
Typical Output Voltage vs Temperature



DS000975-19

Typical Applications

Touch-Tone Decoder



Component values (typ)

R1 6.8 to 15k

R2 4.7k

R3 20k

C1 0.10 mfd

C2 1.0 mfd 6V

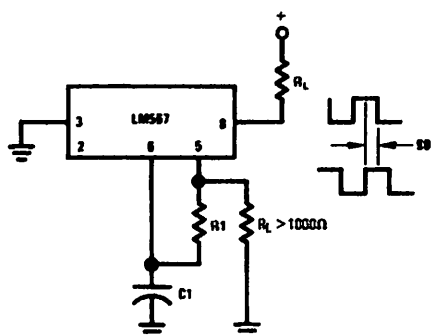
C3 2.2 mfd 6V

C4 250 mfd 6V

D-S006275-5

Typical Applications (Continued)

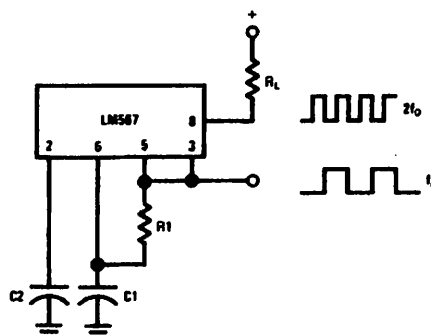
Oscillator with Quadrature Output



DS000075-6

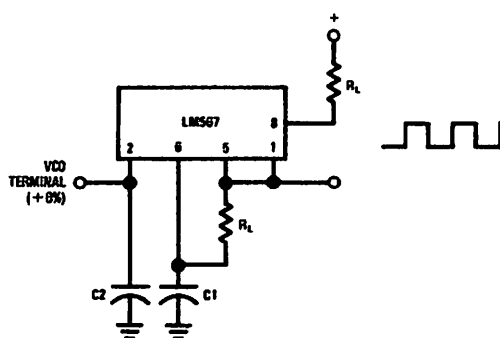
Connect Pin 3 to 2.6V to Invert Output

Oscillator with Double Frequency Output



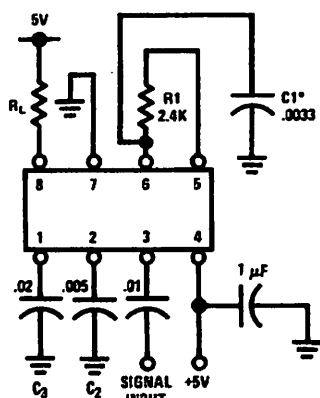
DS000075-7

Precision Oscillator Drive 100 mA Loads



DS000075-8

AC Test Circuit



DS000075-9

$f_0 = 100 \text{ kHz} \pm 5\%$

*Note: Adjust for $f_0 = 100 \text{ kHz}$.

Applications Information

The center frequency of the tone decoder is equal to the free running frequency of the VCO. This is given by

$$f_0 \approx \frac{1}{1.1 R_1 C_1}$$

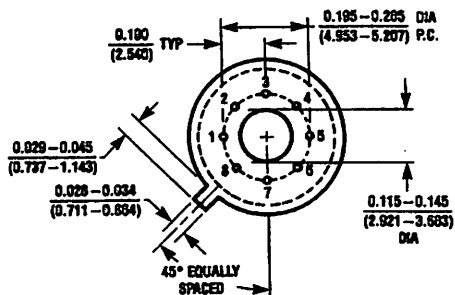
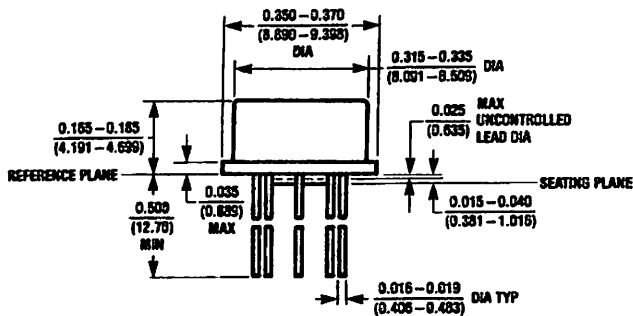
The bandwidth of the filter may be found from the approximation

$$BW = 1070 \sqrt{\frac{V_i}{f_0 C_2}} \text{ in } \% \text{ of } f_0$$

Where:

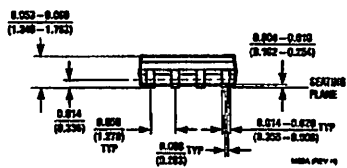
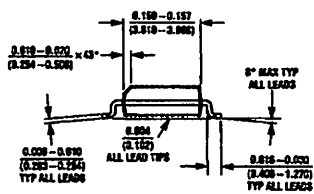
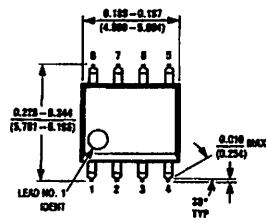
V_i = Input voltage (volts rms), $V_i \leq 200 \text{ mV}$

C_2 = Capacitance at Pin 2 (μF)

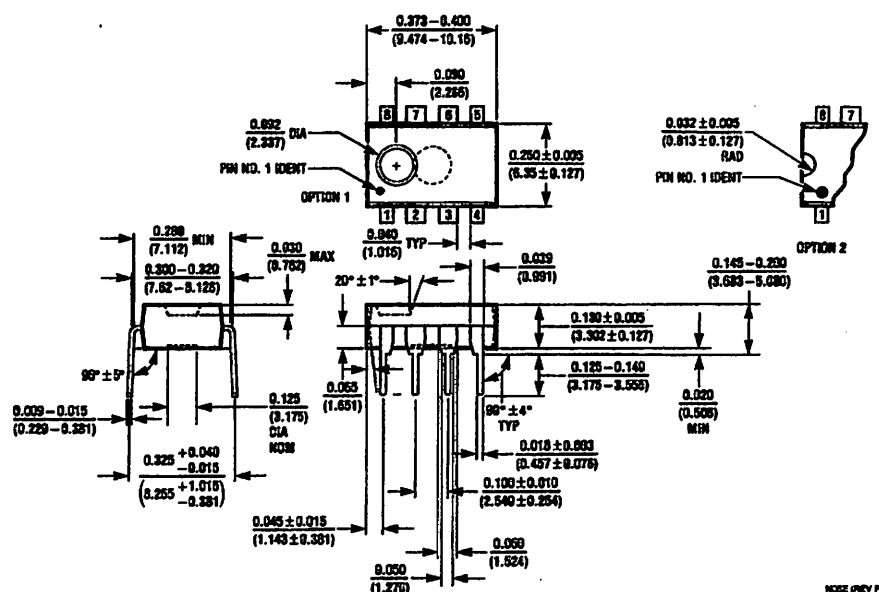
Physical Dimensions inches (millimeters) unless otherwise noted

H03C (REV 12)

Metal Can Package (H)
Order Number LM567H or LM567CH
NS Package Number H08C



**Small Outline Package (M)
Order Number LM567CM
NS Package Number M08A**

Physical Dimensions inches (millimeters) unless otherwise noted (Continued)

Molded Dual-In-Line Package (N)
Order Number LM567CN
NS Package Number N08E

LIFE SUPPORT POLICY

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2. A critical component is any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.



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MC78XX/LM78XX/MC78XXA

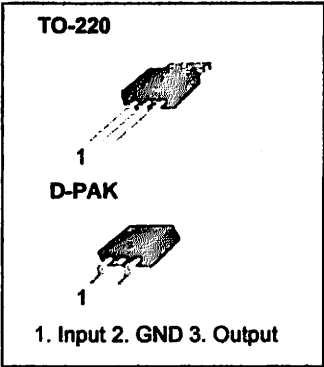
3-Terminal 1A Positive Voltage Regulator

Features

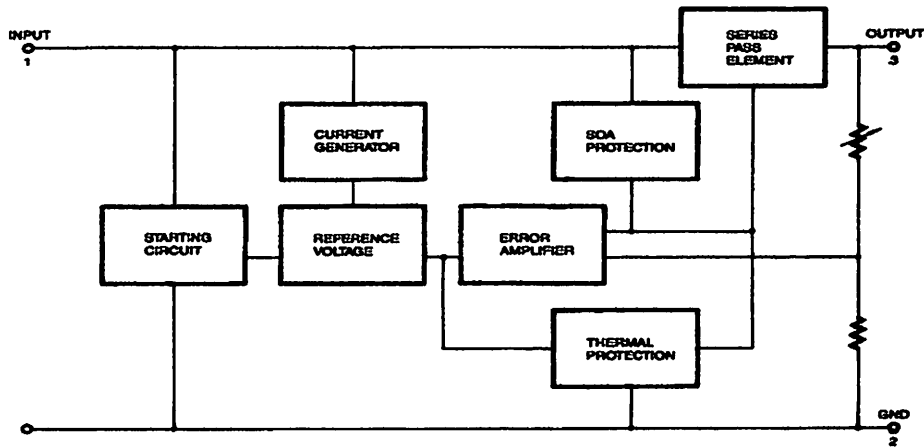
- Output Current up to 1A
- Output Voltages of 5, 6, 8, 9, 10, 12, 15, 18, 24V
- Thermal Overload Protection
- Short Circuit Protection
- Output Transistor Safe Operating Area Protection

Description

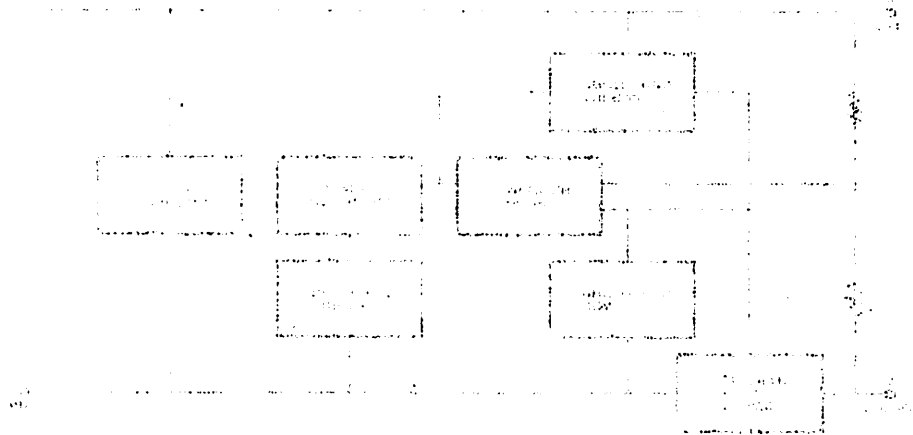
The MC78XX/LM78XX/MC78XXA series of three terminal positive regulators are available in the TO-220/D-PAK package and with several fixed output voltages, making them useful in a wide range of applications. Each type employs internal current limiting, thermal shut down and safe operating area protection, making it essentially indestructible. If adequate heat sinking is provided, they can deliver over 1A output current. Although designed primarily as fixed voltage regulators, these devices can be used with external components to obtain adjustable voltages and currents.



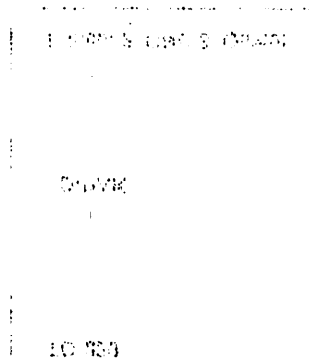
Internal Block Diagram



Rev. 1.0.1



FUNCTIONAL BLOCK DIAGRAM



- Functional Block Diagram
- Functional Block Diagram
- Functional Block Diagram
- Functional Block Diagram
- Functional Block Diagram

FUNCTIONAL

FUNCTIONAL

FUNCTIONAL BLOCK DIAGRAM

FUNCTIONAL BLOCK DIAGRAM

Absolute Maximum Ratings

Parameter	Symbol	Value	Unit
Input Voltage (for $V_O = 5V$ to $18V$) (for $V_O = 24V$)	V_I	35	V
	V_I	40	V
Thermal Resistance Junction-Cases (TO-220)	$R_{\theta JC}$	5	$^{\circ}C/W$
Thermal Resistance Junction-Air (TO-220)	$R_{\theta JA}$	65	$^{\circ}C/W$
Operating Temperature Range	TOPR	0 ~ +125	$^{\circ}C$
Storage Temperature Range	TSTG	-65 ~ +150	$^{\circ}C$

Electrical Characteristics (MC7805/LM7805)

Refer to test circuit ,0°C < T_J < 125°C, I_O = 500mA, V_I = 10V, C_I= 0.33μF, C_O= 0.1μF, unless otherwise specified)

Parameter	Symbol	Conditions		MC7805/LM7805			Unit
				Min.	Typ.	Max.	
Output Voltage	V_O	$T_J = +25^{\circ}C$		4.8	5.0	5.2	V
		$5.0mA \leq I_O \leq 1.0A, P_O \leq 15W$ $V_I = 7V$ to $20V$		4.75	5.0	5.25	
Line Regulation (Note1)	Regline	$T_J = +25^{\circ}C$	$V_O = 7V$ to $25V$	-	4.0	100	mV
			$V_I = 8V$ to $12V$	-	1.6	50	
Load Regulation (Note1)	Regload	$T_J = +25^{\circ}C$	$I_O = 5.0mA$ to $1.5A$	-	9	100	mV
			$I_O = 250mA$ to $750mA$	-	4	50	
Quiescent Current	I_Q	$T_J = +25^{\circ}C$		-	5.0	8.0	mA
Quiescent Current Change	ΔI_Q	$I_O = 5mA$ to $1.0A$		-	0.03	0.5	mA
		$V_I = 7V$ to $25V$		-	0.3	1.3	
Output Voltage Drift	$\Delta V_O / \Delta T$	$I_O = 5mA$		-	-0.8	-	mV/ $^{\circ}C$
Output Noise Voltage	V_N	$f = 10Hz$ to $100KHz, T_A = +25^{\circ}C$		-	42	-	$\mu V/V_O$
Ripple Rejection	RR	$f = 120Hz$ $V_O = 8V$ to $18V$		62	73	-	dB
Dropout Voltage	V_{Drop}	$I_O = 1A, T_J = +25^{\circ}C$		-	2	-	V
Output Resistance	r_O	$f = 1KHz$		-	15	-	m Ω
Short Circuit Current	I_{SC}	$V_I = 35V, T_A = +25^{\circ}C$		-	230	-	mA
Peak Current	I_{PK}	$T_J = +25^{\circ}C$		-	2.2	-	A

note:

. Load and line regulation are specified at constant junction temperature. Changes in V_O due to heating effects must be taken into account separately. Pulse testing with low duty is used.

Electrical Characteristics (MC7806)

Refer to test circuit ,0°C < T_J < 125°C, I_O = 500mA, V_I =11V, C_I= 0.33μF, C_O= 0.1μF, unless otherwise specified)

Parameter	Symbol	Conditions		MC7806			Unit
				Min.	Typ.	Max.	
Output Voltage	V _O	T _J =+25 °C		5.75	6.0	6.25	V
		5.0mA ≤ I _O ≤ 1.0A, P _O ≤ 15W V _I = 8.0V to 21V		5.7	6.0	6.3	
Line Regulation (Note1)	Regline	T _J =+25 °C	V _I = 8V to 25V	-	5	120	mV
			V _I = 9V to 13V	-	1.5	60	
Load Regulation (Note1)	Regload	T _J =+25 °C	I _O =5mA to 1.5A	-	9	120	mV
			I _O =250mA to750A	-	3	60	
Quiescent Current	I _Q	T _J =+25 °C		-	5.0	8.0	mA
Quiescent Current Change	ΔI _Q	I _O = 5mA to 1A		-	-	0.5	mA
		V _I = 8V to 25V		-	-	1.3	
Output Voltage Drift	ΔV _O /ΔT	I _O = 5mA		-	-0.8	-	mV/ °C
Output Noise Voltage	V _N	f = 10Hz to 100KHz, T _A =+25 °C		-	45	-	μV/V _O
Ripple Rejection	RR	f = 120Hz V _I = 9V to 19V		59	75	-	dB
Dropout Voltage	V _{Drop}	I _O = 1A, T _J =+25 °C		-	2	-	V
Output Resistance	r _O	f = 1KHz		-	19	-	mΩ
Short Circuit Current	I _{SC}	V _I = 35V, T _A =+25 °C		-	250	-	mA
Peak Current	I _{PK}	T _J =+25 °C		-	2.2	-	A

note:

. Load and line regulation are specified at constant junction temperature. Changes in V_O due to heating effects must be taken into account separately. Pulse testing with low duty is used.

Electrical Characteristics (MC7808)

Refer to test circuit ,0°C < T_J < 125°C, I_O = 500mA, V_I =14V, C_I= 0.33μF, C_O= 0.1μF, unless otherwise specified)

Parameter	Symbol	Conditions		MC7808			Unit
				Min.	Typ.	Max.	
Output Voltage	V _O	T _J =+25 °C		7.7	8.0	8.3	V
		5.0mA ≤ I _O ≤ 1.0A, P _O ≤ 15W V _I = 10.5V to 23V		7.6	8.0	8.4	
Line Regulation (Note1)	Regline	T _J =+25 °C	V _I = 10.5V to 25V	-	5.0	160	mV
			V _I = 11.5V to 17V	-	2.0	80	
Load Regulation (Note1)	Regload	T _J =+25 °C	I _O = 5.0mA to 1.5A	-	10	160	mV
			I _O = 250mA to 750mA	-	5.0	80	
Quiescent Current	I _Q	T _J =+25 °C		-	5.0	8.0	mA
Quiescent Current Change	ΔI _Q	I _O = 5mA to 1.0A		-	0.05	0.5	mA
		V _I = 10.5A to 25V		-	0.5	1.0	
Output Voltage Drift	ΔV _O /ΔT	I _O = 5mA		-	-0.8	-	mV/ °C
Output Noise Voltage	V _N	f = 10Hz to 100KHz, T _A =+25 °C		-	52	-	μV/V _O
Ripple Rejection	RR	f = 120Hz, V _I = 11.5V to 21.5V		56	73	-	dB
Dropout Voltage	V _{Drop}	I _O = 1A, T _J =+25 °C		-	2	-	V
Output Resistance	r _O	f = 1KHz		-	17	-	mΩ
Short Circuit Current	I _{SC}	V _I = 35V, T _A =+25 °C		-	230	-	mA
Peak Current	I _{PK}	T _J =+25 °C		-	2.2	-	A

note:

. Load and line regulation are specified at constant junction temperature. Changes in V_O due to heating effects must be taken into account separately. Pulse testing with low duty is used.

Electrical Characteristics (MC7809)

Refer to test circuit ,0°C < T_J < 125°C, I_O = 500mA, V_I =15V, C_I= 0.33μF, C_O= 0.1μF, unless otherwise specified)

Parameter	Symbol	Conditions		MC7809			Unit
				Min.	Typ.	Max.	
Output Voltage	V _O	T _J =+25°C		8.65	9	9.35	V
		5.0mA ≤ I _O ≤1.0A, P _O ≤15W V _I = 11.5V to 24V		8.6	9	9.4	
Line Regulation (Note1)	Regline	T _J =+25°C	V _I = 11.5V to 25V	-	6	180	mV
			V _I = 12V to 17V	-	2	90	
Load Regulation (Note1)	Regload	T _J =+25°C	I _O = 5mA to 1.5A	-	12	180	mV
			I _O = 250mA to 750mA	-	4	90	
Quiescent Current	I _Q	T _J =+25°C		-	5.0	8.0	mA
Quiescent Current Change	ΔI _Q	I _O = 5mA to 1.0A		-	-	0.5	mA
		V _I = 11.5V to 26V		-	-	1.3	
Output Voltage Drift	ΔV _O /ΔT	I _O = 5mA		-	-1	-	mV/ °C
Output Noise Voltage	V _N	f = 10Hz to 100KHz, T _A =+25 °C		-	58	-	μV/V _O
Ripple Rejection	RR	f = 120Hz V _I = 13V to 23V		56	71	-	dB
Dropout Voltage	V _{Drop}	I _O = 1A, T _J =+25°C		-	2	-	V
Output Resistance	r _O	f = 1KHz		-	17	-	mΩ
Short Circuit Current	I _{SC}	V _I = 35V, T _A =+25°C		-	250	-	mA
Peak Current	I _{PK}	T _J = +25°C		-	2.2	-	A

Note:

. Load and line regulation are specified at constant junction temperature. Changes in V_O due to heating effects must be taken into account separately. Pulse testing with low duty is used.

Electrical Characteristics (MC7810)

Refer to test circuit ,0°C< T_J < 125°C, I_O = 500mA, V_I =16V, C_I= 0.33μF, C_O=0.1μF, unless otherwise specified)

Parameter	Symbol	Conditions		MC7810			Unit
				Min.	Typ.	Max.	
Output Voltage	V _O	T _J =+25 °C		9.6	10	10.4	V
		5.0mA ≤ I _O ≤1.0A, P _O ≤15W V _I = 12.5V to 25V		9.5	10	10.5	
Line Regulation (Note1)	Regline	T _J =+25°C	V _I = 12.5V to 25V	-	10	200	mV
			V _I = 13V to 25V	-	3	100	
Load Regulation (Note1)	Regload	T _J =+25°C	I _O = 5mA to 1.5A	-	12	200	mV
			I _O = 250mA to 750mA	-	4	400	
Quiescent Current	I _Q	T _J =+25°C		-	5.1	8.0	mA
Quiescent Current Change	ΔI _Q	I _O = 5mA to 1.0A		-	-	0.5	mA
		V _I = 12.5V to 29V		-	-	1.0	
Output Voltage Drift	ΔV _O /ΔT	I _O = 5mA		-	-1	-	mV/°C
Output Noise Voltage	V _N	f = 10Hz to 100KHz, T _A =+25 °C		-	58	-	μV/V _O
Ripple Rejection	RR	f = 120Hz V _I = 13V to 23V		56	71	-	dB
Dropout Voltage	V _{Drop}	I _O = 1A, T _J =+25 °C		-	2	-	V
Output Resistance	r _O	f = 1KHz		-	17	-	mΩ
Short Circuit Current	I _{SC}	V _I = 35V, T _A =+25 °C		-	250	-	mA
Peak Current	I _{PK}	T _J =+25 °C		-	2.2	-	A

ote:

. Load and line regulation are specified at constant junction temperature. Changes in V_O due to heating effects must be taken into account separately. Pulse testing with low duty is used.

Electrical Characteristics (MC7812)

Refer to test circuit ,0°C < T_J < 125°C, I_O = 500mA, V_I =19V, C_I= 0.33μF, C_O=0.1μF, unless otherwise specified)

Parameter	Symbol	Conditions		MC7812			Unit
				Min.	Typ.	Max.	
Output Voltage	V _O	T _J =+25 °C		11.5	12	12.5	V
		5.0mA ≤ I _O ≤1.0A, P _O ≤15W V _I = 14.5V to 27V		11.4	12	12.6	
Line Regulation (Note1)	Regline	T _J =+25 °C	V _I = 14.5V to 30V	-	10	240	mV
			V _I = 16V to 22V	-	3.0	120	
Load Regulation (Note1)	Regload	T _J =+25 °C	I _O = 5mA to 1.5A	-	11	240	mV
			I _O = 250mA to 750mA	-	5.0	120	
Quiescent Current	I _Q	T _J =+25 °C		-	5.1	8.0	mA
Quiescent Current Change	ΔI _Q	I _O = 5mA to 1.0A		-	0.1	0.5	mA
		V _I = 14.5V to 30V		-	0.5	1.0	
Output Voltage Drift	ΔV _O /ΔT	I _O = 5mA		-	-1	-	mV/ °C
Output Noise Voltage	V _N	f = 10Hz to 100KHz, T _A =+25 °C		-	76	-	μV/V _O
Ripple Rejection	RR	f = 120Hz V _I = 15V to 25V		55	71	-	dB
Dropout Voltage	V _{Drop}	I _O = 1A, T _J =+25 °C		-	2	-	V
Output Resistance	r _O	f = 1KHz		-	18	-	mΩ
Short Circuit Current	I _{SC}	V _I = 35V, T _A =+25 °C		-	230	-	mA
Peak Current	I _{PK}	T _J = +25 °C		-	2.2	-	A

note:

. Load and line regulation are specified at constant junction temperature. Changes in V_O due to heating effects must be taken into account separately. Pulse testing with low duty is used.

Electrical Characteristics (MC7815)

Refer to test circuit ,0°C < T_J < 125°C, I_O = 500mA, V_I =23V, C_I= 0.33μF, C_O=0.1μF, unless otherwise specified)

Parameter	Symbol	Conditions		MC7815			Unit
				Min.	Typ.	Max.	
Output Voltage	V _O	T _J =+25 °C		14.4	15	15.6	V
		5.0mA ≤ I _O ≤ 1.0A, P _O ≤ 15W V _I = 17.5V to 30V		14.25	15	15.75	
Line Regulation (Note1)	Regline	T _J =+25 °C	V _I = 17.5V to 30V	-	11	300	mV
			V _I = 20V to 26V	-	3	150	
Load Regulation (Note1)	Regload	T _J =+25 °C	I _O = 5mA to 1.5A	-	12	300	mV
			I _O = 250mA to 750mA	-	4	150	
Quiescent Current	I _Q	T _J =+25 °C		-	5.2	8.0	mA
Quiescent Current Change	ΔI _Q	I _O = 5mA to 1.0A		-	-	0.5	mA
		V _I = 17.5V to 30V		-	-	1.0	
Output Voltage Drift	ΔV _O /ΔT	I _O = 5mA		-	-1	-	mV/°C
Output Noise Voltage	V _N	f = 10Hz to 100KHz, T _A =+25 °C		-	90	-	μV/V _O
Ripple Rejection	RR	f = 120Hz V _I = 18.5V to 28.5V		54	70	-	dB
Dropout Voltage	V _{Drop}	I _O = 1A, T _J =+25 °C		-	2	-	V
Output Resistance	r _O	f = 1KHz		-	19	-	mΩ
Short Circuit Current	I _{SC}	V _I = 35V, T _A =+25 °C		-	250	-	mA
Peak Current	I _{PK}	T _J =+25 °C		-	2.2	-	A

ote:

. Load and line regulation are specified at constant junction temperature. Changes in V_O due to heating effects must be taken into account separately. Pulse testing with low duty is used.

Electrical Characteristics (MC7818)

Refer to test circuit ,0°C < T_J < 125°C, I_O = 500mA, V_I =27V, C_I= 0.33μF, C_O=0.1μF, unless otherwise specified)

Parameter	Symbol	Conditions		MC7818			Unit
				Min.	Typ.	Max.	
Output Voltage	V _O	T _J =+25 °C		17.3	18	18.7	V
		5.0mA ≤ I _O ≤1.0A, P _O ≤15W V _I = 21V to 33V		17.1	18	18.9	
Line Regulation (Note1)	Regline	T _J =+25 °C	V _I = 21V to 33V	-	15	360	mV
			V _I = 24V to 30V	-	5	180	
Load Regulation (Note1)	Regload	T _J =+25 °C	I _O = 5mA to 1.5A	-	15	360	mV
			I _O = 250mA to 750mA	-	5.0	180	
Quiescent Current	I _Q	T _J =+25 °C		-	5.2	8.0	mA
Quiescent Current Change	ΔI _Q	I _O = 5mA to 1.0A		-	-	0.5	mA
		V _I = 21V to 33V		-	-	1	
Output Voltage Drift	ΔV _O /ΔT	I _O = 5mA		-	-1	-	mV/°C
Output Noise Voltage	V _N	f = 10Hz to 100KHz, T _A =+25 °C		-	110	-	μV/V _O
Ripple Rejection	RR	f = 120Hz V _I = 22V to 32V		53	69	-	dB
Dropout Voltage	V _{Drop}	I _O = 1A, T _J =+25 °C		-	2	-	V
Output Resistance	r _O	f = 1KHz		-	22	-	mΩ
Short Circuit Current	I _{SC}	V _I = 35V, T _A =+25 °C		-	250	-	mA
Peak Current	I _{PK}	T _J =+25 °C		-	2.2	-	A

Note:

1. Load and line regulation are specified at constant junction temperature. Changes in V_O due to heating effects must be taken into account separately. Pulse testing with low duty is used.

Electrical Characteristics (MC7824)

Refer to test circuit ,0°C < T_J < 125°C, I_O = 500mA, V_I =33V, C_I= 0.33μF, C_O=0.1μF, unless otherwise specified)

Parameter	Symbol	Conditions		MC7824			Unit
				Min.	Typ.	Max.	
Output Voltage	V _O	T _J =+25 °C		23	24	25	V
		5.0mA ≤ I _O ≤ 1.0A, P _O ≤ 15W V _I = 27V to 38V		22.8	24	25.25	
Line Regulation (Note1)	Regline	T _J =+25 °C	V _I = 27V to 38V	-	17	480	mV
			V _I = 30V to 36V	-	6	240	
Load Regulation (Note1)	Regload	T _J =+25 °C	I _O = 5mA to 1.5A	-	15	480	mV
			I _O = 250mA to 750mA	-	5.0	240	
Quiescent Current	I _Q	T _J =+25 °C		-	5.2	8.0	mA
Quiescent Current Change	ΔI _Q	I _O = 5mA to 1.0A		-	0.1	0.5	mA
		V _I = 27V to 38V		-	0.5	1	
Output Voltage Drift	ΔV _O /ΔT	I _O = 5mA		-	-1.5	-	mV/°C
Output Noise Voltage	V _N	f = 10Hz to 100KHz, T _A =+25 °C		-	60	-	μV/V _O
Ripple Rejection	RR	f = 120Hz V _I = 28V to 38V		50	67	-	dB
Dropout Voltage	V _{Drop}	I _O = 1A, T _J =+25 °C		-	2	-	V
Output Resistance	r _O	f = 1KHz		-	28	-	mΩ
Short Circuit Current	I _{SC}	V _I = 35V, T _A =+25 °C		-	230	-	mA
Peak Current	I _{PK}	T _J =+25 °C		-	2.2	-	A

note:

. Load and line regulation are specified at constant junction temperature. Changes in V_O due to heating effects must be taken into account separately. Pulse testing with low duty is used.

Electrical Characteristics (MC7805A)

Refer to the test circuits. 0°C < T_J < 125°C, I_O = 1A, V_I = 10V, C_I = 0.33μF, C_O = 0.1μF, unless otherwise specified)

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
Output Voltage	V _O	T _J = +25 °C	4.9	5	5.1	V
		I _O = 5mA to 1A, P _O ≤ 15W V _I = 7.5V to 20V	4.8	5	5.2	
Line Regulation (Note1)	Regline	V _I = 7.5V to 25V I _O = 500mA	-	5	50	mV
		V _I = 8V to 12V	-	3	50	
		T _J = +25 °C	V _I = 7.3V to 20V	5	50	
			V _I = 8V to 12V	1.5	25	
Load Regulation (Note1)	Regload	T _J = +25 °C I _O = 5mA to 1.5A	-	9	100	mV
		I _O = 5mA to 1A	-	9	100	
		I _O = 250mA to 750mA	-	4	50	
Quiescent Current	I _Q	T _J = +25 °C	-	5.0	6	mA
Quiescent Current Change	ΔI _Q	I _O = 5mA to 1A	-	-	0.5	mA
		V _I = 8 V to 25V, I _O = 500mA	-	-	0.8	
		V _I = 7.5V to 20V, T _J = +25 °C	-	-	0.8	
Output Voltage Drift	ΔV/ΔT	I _O = 5mA	-	-0.8	-	mV/°C
Output Noise Voltage	V _N	f = 10Hz to 100KHz T _A = +25 °C	-	10	-	μV/V _O
Ripple Rejection	RR	f = 120Hz, I _O = 500mA V _I = 8V to 18V	-	68	-	dB
Dropout Voltage	V _{Drop}	I _O = 1A, T _J = +25 °C	-	2	-	V
Output Resistance	r _O	f = 1KHz	-	17	-	mΩ
Short Circuit Current	I _{SC}	V _I = 35V, T _A = +25 °C	-	250	-	mA
Peak Current	I _{PK}	T _J = +25 °C	-	2.2	-	A

ote:

. Load and line regulation are specified at constant junction temperature. Change in V_O due to heating effects must be taken into account separately. Pulse testing with low duty is used.

Electrical Characteristics (MC7806A)

Refer to the test circuits. 0°C < T_J < 125°C, I_O = 1A, V_I = 11V, C_I = 0.33μF, C_O = 0.1μF, unless otherwise specified)

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
Output Voltage	V _O	T _J = +25 °C	5.58	6	6.12	V
		I _O = 5mA to 1A, P _O ≤ 15W V _I = 8.6V to 21V	5.76	6	6.24	
Line Regulation (Note1)	Regline	V _I = 8.6V to 25V I _O = 500mA	-	5	60	mV
		V _I = 9V to 13V	-	3	60	
		T _J = +25 °C	V _I = 8.3V to 21V		5	60
			V _I = 9V to 13V		1.5	30
Load Regulation (Note1)	Regload	T _J = +25 °C I _O = 5mA to 1.5A	-	9	100	mV
		I _O = 5mA to 1A	-	4	100	
		I _O = 250mA to 750mA	-	5.0	50	
Quiescent Current	I _Q	T _J = +25 °C	-	4.3	6	mA
Quiescent Current Change	ΔI _Q	I _O = 5mA to 1A	-	-	0.5	mA
		V _I = 9V to 25V, I _O = 500mA	-	-	0.8	
		V _I = 8.5V to 21V, T _J = +25 °C	-	-	0.8	
Output Voltage Drift	ΔV/ΔT	I _O = 5mA	-	-0.8	-	mV/°C
Output Noise Voltage	V _N	f = 10Hz to 100KHz T _A = +25 °C	-	10	-	μV/V _O
Ripple Rejection	RR	f = 120Hz, I _O = 500mA V _I = 9V to 19V	-	65	-	dB
Dropout Voltage	V _{Drop}	I _O = 1A, T _J = +25 °C	-	2	-	V
Output Resistance	r _O	f = 1KHz	-	17	-	mΩ
Short Circuit Current	I _{SC}	V _I = 35V, T _A = +25 °C	-	250	-	mA
Peak Current	I _{PK}	T _J = +25 °C	-	2.2	-	A

ote:

. Load and line regulation are specified at constant junction temperature. Change in V_O due to heating effects must be taken into account separately. Pulse testing with low duty is used.

Electrical Characteristics (MC7808A)

Refer to the test circuits. $0^{\circ}\text{C} < T_J < 125^{\circ}\text{C}$, $I_O = 1\text{A}$, $V_I = 14\text{V}$, $C_I = 0.33\mu\text{F}$, $C_O = 0.1\mu\text{F}$, unless otherwise specified)

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
Output Voltage	V_O	$T_J = +25^{\circ}\text{C}$	7.84	8	8.16	V
		$I_O = 5\text{mA to } 1\text{A}$, $P_O \leq 15\text{W}$ $V_I = 10.6\text{V to } 23\text{V}$	7.7	8	8.3	
Line Regulation (Note1)	Regline	$V_I = 10.6\text{V to } 25\text{V}$ $I_O = 500\text{mA}$	-	6	80	mV
		$V_I = 11\text{V to } 17\text{V}$	-	3	80	
		$T_J = +25^{\circ}\text{C}$	$V_I = 10.4\text{V to } 23\text{V}$	-	6	80
			$V_I = 11\text{V to } 17\text{V}$	-	2	40
Load Regulation (Note1)	Regload	$T_J = +25^{\circ}\text{C}$ $I_O = 5\text{mA to } 1.5\text{A}$	-	12	100	mV
		$I_O = 5\text{mA to } 1\text{A}$	-	12	100	
		$I_O = 250\text{mA to } 750\text{mA}$	-	5	50	
Quiescent Current	I_Q	$T_J = +25^{\circ}\text{C}$	-	5.0	6	mA
Quiescent Current Change	ΔI_Q	$I_O = 5\text{mA to } 1\text{A}$	-	-	0.5	mA
		$V_I = 11\text{V to } 25\text{V}$, $I_O = 500\text{mA}$	-	-	0.8	
		$V_I = 10.6\text{V to } 23\text{V}$, $T_J = +25^{\circ}\text{C}$	-	-	0.8	
Output Voltage Drift	$\Delta V/\Delta T$	$I_O = 5\text{mA}$	-	-0.8	-	mV/ $^{\circ}\text{C}$
Output Noise Voltage	V_N	$f = 10\text{Hz to } 100\text{KHz}$ $T_A = +25^{\circ}\text{C}$	-	10	-	$\mu\text{V}/V_O$
Ripple Rejection	RR	$f = 120\text{Hz}$, $I_O = 500\text{mA}$ $V_I = 11.5\text{V to } 21.5\text{V}$	-	62	-	dB
Dropout Voltage	V_{Drop}	$I_O = 1\text{A}$, $T_J = +25^{\circ}\text{C}$	-	2	-	V
Output Resistance	r_O	$f = 1\text{KHz}$	-	18	-	$\text{m}\Omega$
Short Circuit Current	I_{SC}	$V_I = 35\text{V}$, $T_A = +25^{\circ}\text{C}$	-	250	-	mA
Peak Current	I_{PK}	$T_J = +25^{\circ}\text{C}$	-	2.2	-	A

Note:

Load and line regulation are specified at constant junction temperature. Change in V_O due to heating effects must be taken into account separately. Pulse testing with low duty is used.

Electrical Characteristics (MC7809A)

Refer to the test circuits. 0°C < T_J < 125°C, I_O = 1A, V_I = 15V, C_I = 0.33μF, C_O = 0.1μF, unless otherwise specified)

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
Output Voltage	V _O	T _J = +25 °C	8.82	9.0	9.18	V
		I _O = 5mA to 1A, P _O ≤ 15W V _I = 11.2V to 24V	8.65	9.0	9.35	
Line Regulation (Note1)	Regline	V _I = 11.7V to 25V I _O = 500mA	-	6	90	mV
		V _I = 12.5V to 19V	-	4	45	
		T _J = +25 °C	V _I = 11.5V to 24V	6	90	
			V _I = 12.5V to 19V	2	45	
Load Regulation (Note1)	Regload	T _J = +25 °C I _O = 5mA to 1.0A	-	12	100	mV
		I _O = 5mA to 1.0A	-	12	100	
		I _O = 250mA to 750mA	-	5	50	
Quiescent Current	I _Q	T _J = +25 °C	-	5.0	6.0	mA
Quiescent Current Change	ΔI _Q	V _I = 11.7V to 25V, T _J = +25 °C	-	-	0.8	mA
		V _I = 12V to 25V, I _O = 500mA	-	-	0.8	
		I _O = 5mA to 1.0A	-	-	0.5	
Output Voltage Drift	ΔV/ΔT	I _O = 5mA	-	-1.0	-	mV/ °C
Output Noise Voltage	V _N	f = 10Hz to 100KHz T _A = +25 °C	-	10	-	μV/V _O
Ripple Rejection	RR	f = 120Hz, I _O = 500mA V _I = 12V to 22V	-	62	-	dB
Dropout Voltage	V _{Drop}	I _O = 1A, T _J = +25 °C	-	2.0	-	V
Output Resistance	r _O	f = 1KHz	-	17	-	mΩ
Short Circuit Current	I _{SC}	V _I = 35V, T _A = +25 °C	-	250	-	mA
Peak Current	I _{PK}	T _J = +25 °C	-	2.2	-	A

Note:

1. Load and line regulation are specified at constant junction temperature. Change in V_O due to heating effects must be taken into account separately. Pulse testing with low duty is used.

Electrical Characteristics (MC7810A)

Refer to the test circuits. 0°C < T_J < 125°C, I_O = 1A, V_I = 16V, C_I = 0.33μF, C_O = 0.1μF, unless otherwise specified)

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
Output Voltage	V _O	T _J = +25 °C	9.8	10	10.2	V
		I _O = 5mA to 1A, P _O ≤ 15W V _I = 12.8V to 25V	9.6	10	10.4	
Line Regulation (Note1)	Regline	V _I = 12.8V to 26V I _O = 500mA	-	8	100	mV
		V _I = 13V to 20V	-	4	50	
		T _J = +25 °C	V _I = 12.5V to 25V	8	100	
			V _I = 13V to 20V	3	50	
Load Regulation (Note1)	Regload	T _J = +25 °C I _O = 5mA to 1.5A	-	12	100	mV
		I _O = 5mA to 1.0A	-	12	100	
		I _O = 250mA to 750mA	-	5	50	
Quiescent Current	I _Q	T _J = +25 °C	-	5.0	6.0	mA
Quiescent Current Change	ΔI _Q	V _I = 13V to 26V, T _J = +25 °C	-	-	0.5	mA
		V _I = 12.8V to 25V, I _O = 500mA	-	-	0.8	
		I _O = 5mA to 1.0A	-	-	0.5	
Output Voltage Drift	ΔV/ΔT	I _O = 5mA	-	-1.0	-	mV/ °C
Output Noise Voltage	V _N	f = 10Hz to 100KHz T _A = +25 °C	-	10	-	μV/V _O
Ripple Rejection	RR	f = 120Hz, I _O = 500mA V _I = 14V to 24V	-	62	-	dB
Dropout Voltage	V _{Drop}	I _O = 1A, T _J = +25 °C	-	2.0	-	V
Output Resistance	r _O	f = 1KHz	-	17	-	mΩ
Short Circuit Current	I _{SC}	V _I = 35V, T _A = +25 °C	-	250	-	mA
Peak Current	I _{PK}	T _J = +25 °C	-	2.2	-	A

note:

. Load and line regulation are specified at constant junction temperature. Change in V_O due to heating effects must be taken into account separately. Pulse testing with low duty is used.

Electrical Characteristics (MC7812A)

Refer to the test circuits. 0°C < T_J < 125°C, I_O = 1A, V_I = 19V, C_I = 0.33µF, C_O = 0.1µF, unless otherwise specified)

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
Output Voltage	V _O	T _J = +25 °C	11.75	12	12.25	V
		I _O = 5mA to 1A, P _O ≤ 15W V _I = 14.8V to 27V	11.5	12	12.5	
Line Regulation (Note1)	Regline	V _I = 14.8V to 30V I _O = 500mA	-	10	120	mV
		V _I = 16V to 22V	-	4	120	
		T _J = +25 °C	V _I = 14.5V to 27V	10	120	
			V _I = 16V to 22V	3	60	
Load Regulation (Note1)	Regload	T _J = +25 °C I _O = 5mA to 1.5A	-	12	100	mV
		I _O = 5mA to 1.0A	-	12	100	
		I _O = 250mA to 750mA	-	5	50	
Quiescent Current	I _Q	T _J = +25 °C	-	5.1	6.0	mA
Quiescent Current Change	ΔI _Q	V _I = 15V to 30V, T _J = +25 °C	-		0.8	mA
		V _I = 14V to 27V, I _O = 500mA	-		0.8	
		I _O = 5mA to 1.0A	-		0.5	
Output Voltage Drift	ΔV/ΔT	I _O = 5mA	-	-1.0	-	mV/°C
Output Noise Voltage	V _N	f = 10Hz to 100KHz T _A = +25 °C	-	10	-	µV/V _O
Ripple Rejection	RR	f = 120Hz, I _O = 500mA V _I = 14V to 24V	-	60	-	dB
Dropout Voltage	V _{Drop}	I _O = 1A, T _J = +25 °C	-	2.0	-	V
Output Resistance	r _O	f = 1KHz	-	18	-	mΩ
Short Circuit Current	I _{SC}	V _I = 35V, T _A = +25 °C	-	250	-	mA
Peak Current	I _{PK}	T _J = +25 °C	-	2.2	-	A

ote:

. Load and line regulation are specified at constant junction temperature. Change in V_O due to heating effects must be taken into account separately. Pulse testing with low duty is used.

Electrical Characteristics (MC7815A)

Refer to the test circuits. 0°C < T_J < 125°C, I_O = 1A, V_I = 23V, C_I = 0.33µF, C_O = 0.1µF, unless otherwise specified)

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
Output Voltage	V _O	T _J = +25 °C	14.7	15	15.3	V
		I _O = 5mA to 1A, P _O ≤ 15W V _I = 17.7V to 30V	14.4	15	15.6	
Line Regulation (Note1)	Regline	V _I = 17.9V to 30V I _O = 500mA	-	10	150	mV
		V _I = 20V to 26V	-	5	150	
		T _J = +25 °C	V _I = 17.5V to 30V	11	150	
			V _I = 20V to 26V	3	75	
Load Regulation (Note1)	Regload	T _J = +25 °C I _O = 5mA to 1.5A	-	12	100	mV
		I _O = 5mA to 1.0A	-	12	100	
		I _O = 250mA to 750mA	-	5	50	
Quiescent Current	I _Q	T _J = +25 °C	-	5.2	6.0	mA
Quiescent Current Change	ΔI _Q	V _I = 17.5V to 30V, T _J = +25 °C	-	-	0.8	mA
		V _I = 17.5V to 30V, I _O = 500mA	-	-	0.8	
		I _O = 5mA to 1.0A	-	-	0.5	
Output Voltage Drift	ΔV/ΔT	I _O = 5mA	-	-1.0	-	mV/°C
Output Noise Voltage	V _N	f = 10Hz to 100KHz T _A = +25 °C	-	10	-	µV/V _O
Ripple Rejection	RR	f = 120Hz, I _O = 500mA V _I = 18.5V to 28.5V	-	58	-	dB
Dropout Voltage	V _{Drop}	I _O = 1A, T _J = +25 °C	-	2.0	-	V
Output Resistance	r _O	f = 1KHz	-	19	-	mΩ
Short Circuit Current	I _{SC}	V _I = 35V, T _A = +25 °C	-	250	-	mA
Peak Current	I _{PK}	T _J = +25 °C	-	2.2	-	A

Note:

Load and line regulation are specified at constant junction temperature. Change in V_O due to heating effects must be taken into account separately. Pulse testing with low duty is used.

Electrical Characteristics (MC7818A)

Refer to the test circuits. 0°C < T_J < 125°C, I_O = 1A, V_I = 27V, C_I = 0.33μF, C_O = 0.1μF, unless otherwise specified)

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
Output Voltage	V _O	T _J = +25 °C	17.64	18	18.36	V
		I _O = 5mA to 1A, P _O ≤ 15W V _I = 21V to 33V	17.3	18	18.7	
Line Regulation (Note1)	Regline	V _I = 21V to 33V I _O = 500mA	-	15	180	mV
		V _I = 21V to 33V	-	5	180	
		T _J = +25 °C	V _I = 20.6V to 33V	-	15	180
			V _I = 24V to 30V	-	5	90
Load Regulation (Note1)	Regload	T _J = +25 °C I _O = 5mA to 1.5A	-	15	100	mV
		I _O = 5mA to 1.0A	-	15	100	
		I _O = 250mA to 750mA	-	7	50	
Quiescent Current	I _Q	T _J = +25 °C	-	5.2	6.0	mA
Quiescent Current Change	ΔI _Q	V _I = 21V to 33V, T _J = +25 °C	-	-	0.8	mA
		V _I = 21V to 33V, I _O = 500mA	-	-	0.8	
		I _O = 5mA to 1.0A	-	-	0.5	
Output Voltage Drift	ΔV/ΔT	I _O = 5mA	-	-1.0	-	mV/ °C
Output Noise Voltage	V _N	f = 10Hz to 100KHz T _A = +25 °C	-	10	-	μV/V _O
Ripple Rejection	RR	f = 120Hz, I _O = 500mA V _I = 22V to 32V	-	57	-	dB
Dropout Voltage	V _{Drop}	I _O = 1A, T _J = +25 °C	-	2.0	-	V
Output Resistance	r _O	f = 1KHz	-	19	-	mΩ
Short Circuit Current	I _{SC}	V _I = 35V, T _A = +25 °C	-	250	-	mA
Peak Current	I _{PK}	T _J = +25 °C	-	2.2	-	A

ote:

. Load and line regulation are specified at constant junction temperature. Change in V_O due to heating effects must be taken into account separately. Pulse testing with low duty is used.

Electrical Characteristics (MC7824A)

Refer to the test circuits. 0°C < T_J < 125°C, I_O = 1A, V_I = 33V, C_I = 0.33μF, C_O = 0.1μF, unless otherwise specified)

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit	
Output Voltage	V _O	T _J =+25 °C	23.5	24	24.5	V	
		I _O = 5mA to 1A, P _O ≤15W V _I = 27.3V to 38V	23	24	25		
Line Regulation (Note1)	Regline	V _I = 27V to 38V I _O = 500mA	-	18	240	mV	
		V _I = 21V to 33V	-	6	240		
		T _J =+25 °C	V _I = 26.7V to 38V	-	18		240
			V _I = 30V to 36V	-	6		120
Load Regulation (Note1)	Regload	T _J =+25 °C I _O = 5mA to 1.5A	-	15	100	mV	
		I _O = 5mA to 1.0A	-	15	100		
		I _O = 250mA to 750mA	-	7	50		
Quiescent Current	I _Q	T _J =+25 °C	-	5.2	6.0	mA	
Quiescent Current Change	ΔI _Q	V _I = 27.3V to 38V, T _J =+25 °C	-	-	0.8	mA	
		V _I = 27.3V to 38V, I _O = 500mA	-	-	0.8		
		I _O = 5mA to 1.0A	-	-	0.5		
Output Voltage Drift	ΔV/ΔT	I _O = 5mA	-	-1.5	-	mV/ °C	
Output Noise Voltage	V _N	f = 10Hz to 100KHz T _A = 25 °C	-	10	-	μV/V _O	
Ripple Rejection	RR	f = 120Hz, I _O = 500mA V _I = 28V to 38V	-	54	-	dB	
Dropout Voltage	V _{Drop}	I _O = 1A, T _J =+25 °C	-	2.0	-	V	
Output Resistance	r _O	f = 1KHz	-	20	-	mΩ	
Short Circuit Current	I _{SC}	V _I = 35V, T _A =+25 °C	-	250	-	mA	
Peak Current	I _{PK}	T _J =+25 °C	-	2.2	-	A	

Note:

Load and line regulation are specified at constant junction temperature. Change in V_O due to heating effects must be taken into account separately. Pulse testing with low duty is used.

Typical Performance Characteristics

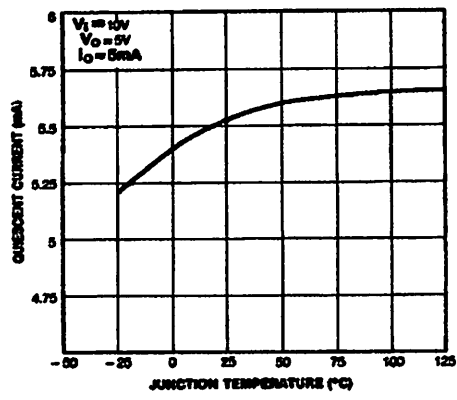


Figure 1. Quiescent Current

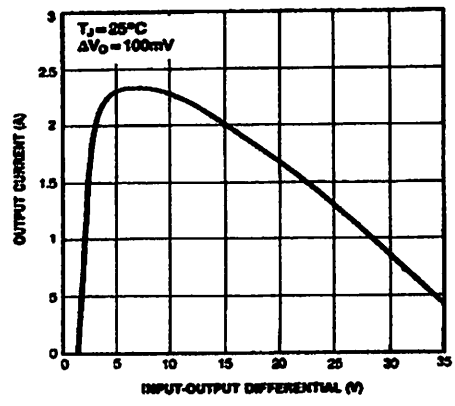


Figure 2. Peak Output Current

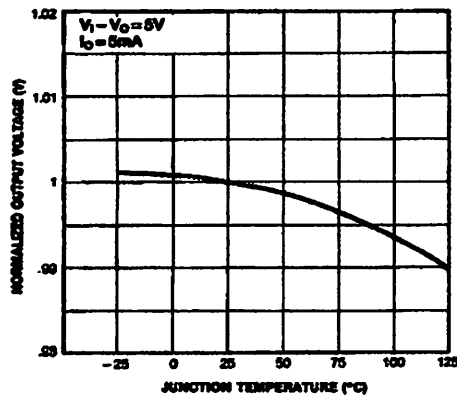


Figure 3. Output Voltage

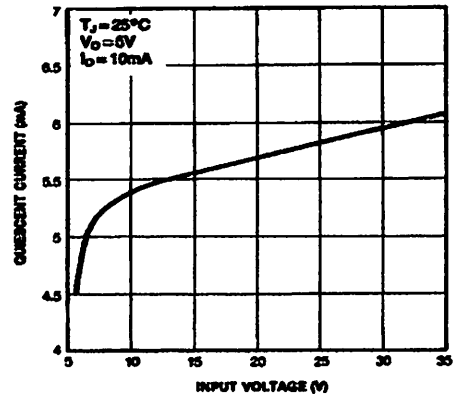


Figure 4. Quiescent Current

Typical Applications

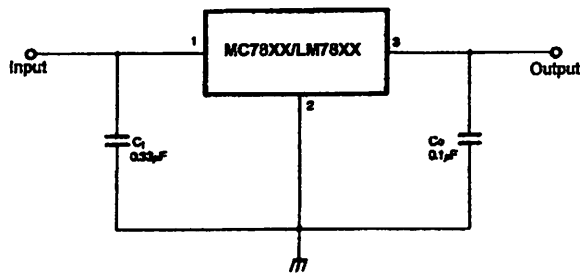


Figure 5. DC Parameters

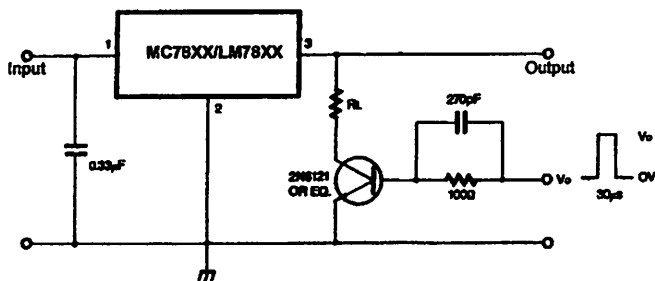


Figure 6. Load Regulation

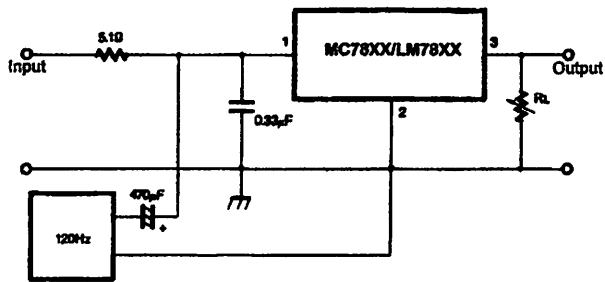


Figure 7. Ripple Rejection

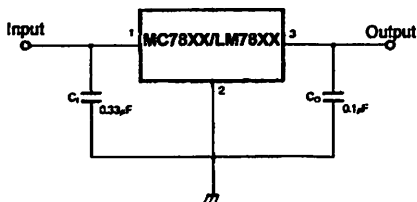


Figure 8. Fixed Output Regulator

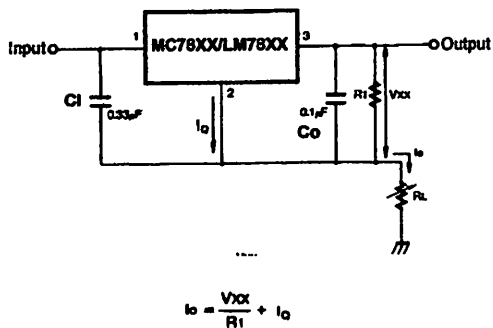
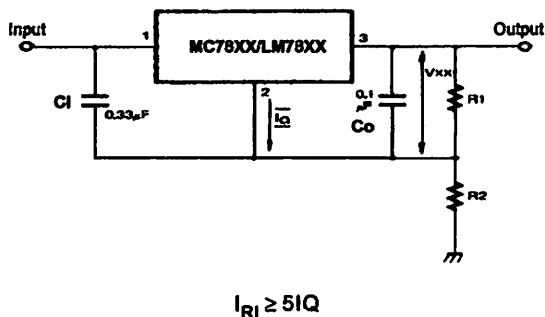


Figure 9. Constant Current Regulator

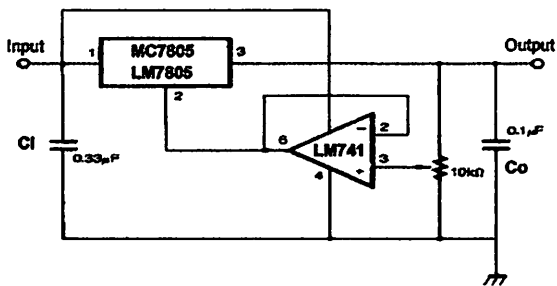
otes:

-) To specify an output voltage, substitute voltage value for "XX." A common ground is required between the input and the Output voltage. The input voltage must remain typically 2.0V above the output voltage even during the low point on the input ripple voltage.
-) C1 is required if regulator is located an appreciable distance from power Supply filter.
-) Co improves stability and transient response.



$$V_O = V_{XX}(1+R_2/R_1)+I_Q R_2$$

Figure 10. Circuit for Increasing Output Voltage



$$V_O = V_{XX}(1+R_2/R_1)+I_Q R_2$$

Figure 11. Adjustable Output Regulator (7 to 30V)

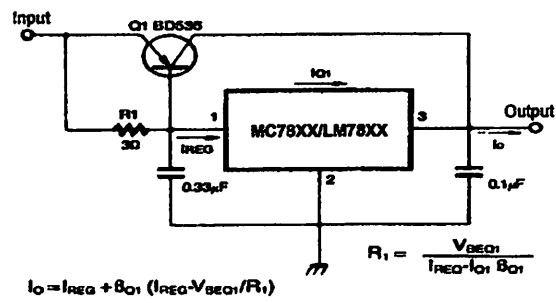


Figure 12. High Current Voltage Regulator

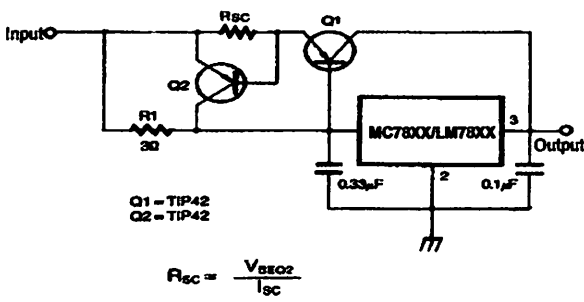


Figure 13. High Output Current with Short Circuit Protection

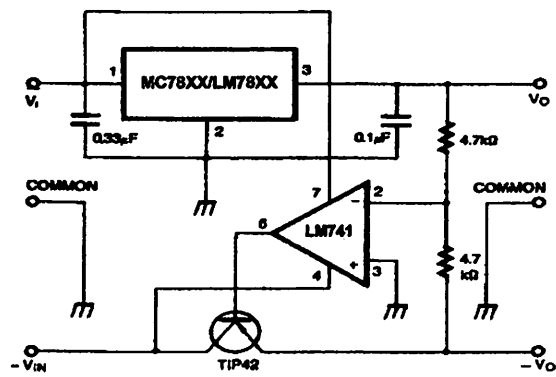


Figure 14. Tracking Voltage Regulator

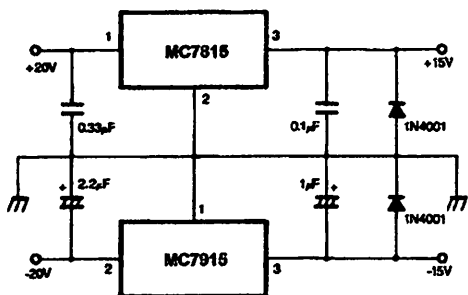


Figure 15. Split Power Supply (±15V-1A)

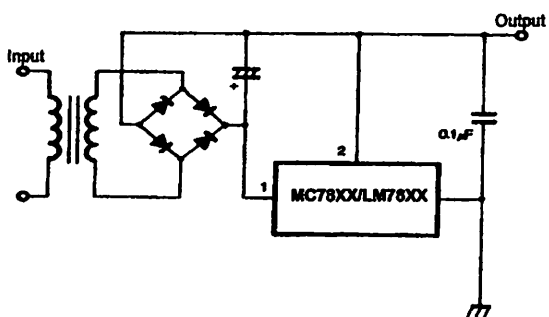


Figure 16. Negative Output Voltage Circuit

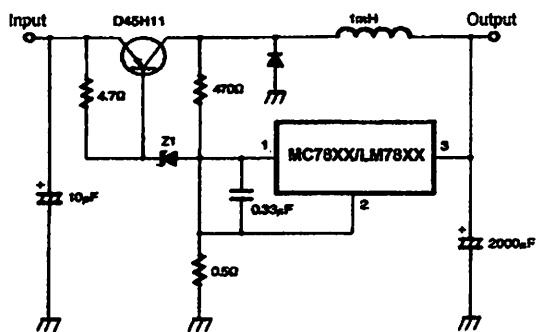
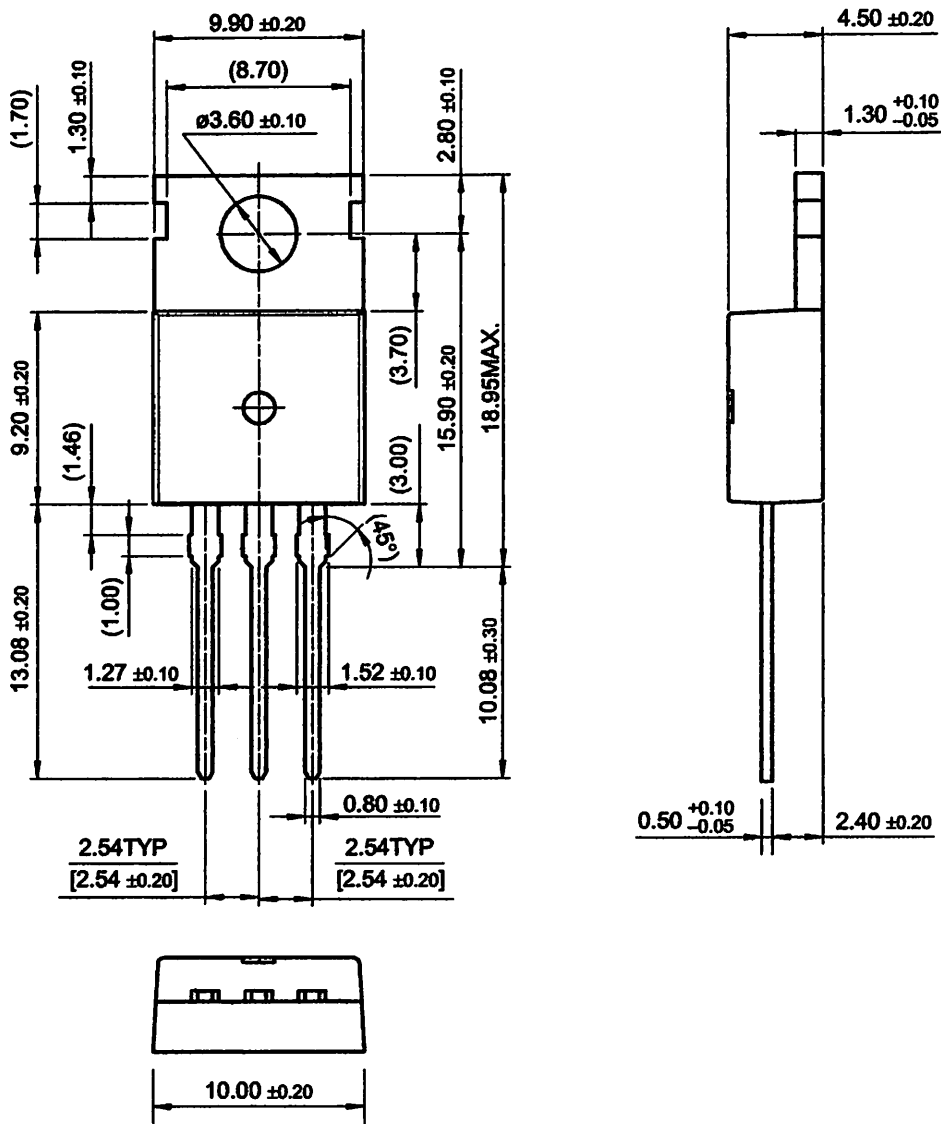


Figure 17. Switching Regulator

Mechanical Dimensions

Package

TO-220



D-PAK



Ordering Information

Product Number	Output Voltage Tolerance	Package	Operating Temperature
LM7805CT	±4%	TO-220	0 ~ + 125°C

Product Number	Output Voltage Tolerance	Package	Operating Temperature
MC7805CT	±4%	TO-220	0 ~ + 125°C
MC7806CT			
MC7808CT			
MC7809CT			
MC7810CT			
MC7812CT			
MC7815CT			
MC7818CT			
MC7824CT			
MC7805CDT		D-PAK	
MC7806CDT			
MC7808CDT			
MC7809CDT			
MC7810CDT			
MC7812CDT			
MC7805ACT	±2%	TO-220	
MC7806ACT			
MC7808ACT			
MC7809ACT			
MC7810ACT			
MC7812ACT			
MC7815ACT			
MC7818ACT			
MC7824ACT			

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2. A critical component in any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.



M1632

LIQUID CRYSTAL DISPLAY MODULE

USER'S MANUAL

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Seiko Instruments

M1635

LIQUID CRYSTAL DISPLAY MODULE

USER'S MANUAL

GENERAL

1.1 General

The M1632 is a low-power-consumption dot-matrix liquid crystal display (LCD) module with a high-contrast wide-view LCD panel and a CMOS LCD drive controller built in. The controller has a built-in character generator ROM/RAM, and display data RAM. All the display functions are controlled by instructions and the module can easily be interfaced with an MPU. This makes the module applicable to a wide range of purposes including terminal display units for microcomputers and display units for measuring gages.

1.2 Features

- 16-character, two-line liquid crystal display of 5 x 7 dot matrix + cursor
- Duty ratio: 1/16
- Character generator ROM for 192 character types (character font: 5 x 7 dot matrix)
- Character generator RAM for eight character types (program write) (character font: 5 x 7 dot matrix)
- 80 x 8 bit display data RAM (80 characters maximum)
- Interface with four-bit and eight-bit MPUs possible
- Display data RAM and character generator RAM readable from MPU
- Many instruction functions

Display Clear, Cursor Home, Display ON/OFF, Cursor ON/OFF, Display Character Blink, Cursor Shift, and Display Shift

- Built-in oscillator circuit
- +5 V single power supply
- Built-in automatic reset circuit at power-on
- CMOS process
- Operating temperature range: 0°C to 50°C

- Operating temperature range: 0°C to 20°C
- CMOS process
- Built-in automatic reset circuit at power-on
- +2 V single power supply
- Built-in oscillator circuit

Character Bank, Cursor Shift and Display Shift
Display Clear, Cursor Home, Display On/Off, Cursor On/Off, Display

- Many instruction functions
- Display data RAM and character generator RAM loadable from MPU
- Interface with four-bit and eight-bit MPUs possible
- 80 x 8 bit display data RAM (80 characters maximum)
(character font: 2 x 7 dot matrix)
- Character generator RAM for eight character types (program write)
(character font: 2 x 7 dot matrix)
- Character generator ROM for 128 character types
- Duty ratio: 1/16
- 16-character, two-line liquid crystal display of 2 x 7 dot matrix + cursor

1.3 Features

units for measuring power
range of functions including terminal display units for microcomputers and display
can easily be interfaced with an MPU. This makes the module applicable to a wide
data RAM. All the display functions are controlled by instructions and the module
can be controlled by a built-in character generator ROM (RAM) and display
module with a high-contrast wide-view LCD panel and a CMOS LCD drive controller.
The M1632 is a low-power-consumption dot-matrix liquid crystal display (LCD)

1.4 General

GENERAL

1.3 Block Diagram

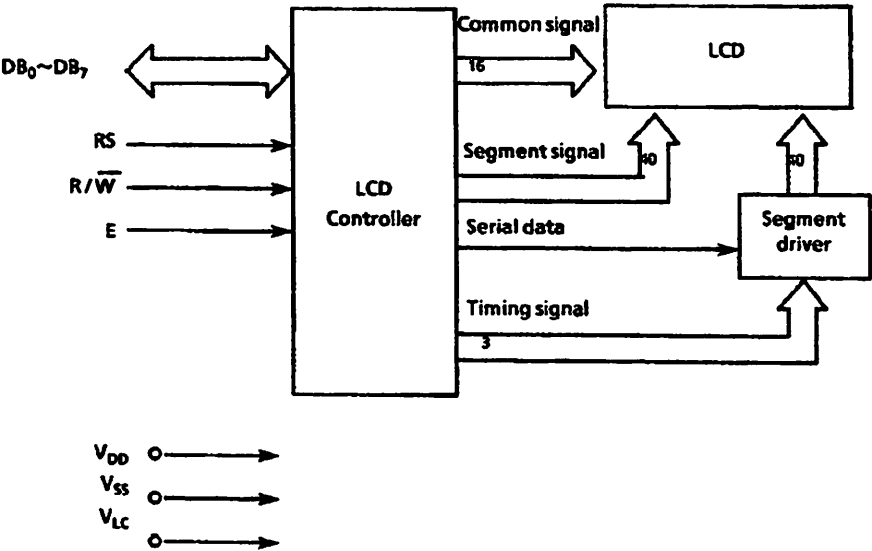


Figure 1

1.4 Absolute Maximum Ratings

$V_{SS} = 0\text{ V}$

Item	Symbol	Standard	Unit	Remarks
Power supply voltage	V_{DD}	$-0.3\text{ to }+7.0$	V	
	V_{LC}	$V_{DD} - 13.5\text{ to }V_{DD} + 0.3$	V	
Input voltage	V_{in}	$-0.3\text{ to }V_{DD} + 0.3$	V	
Operating temperature	T_{opr}	$0\text{ to }+50$	°C	
Storage temperature	T_{stg}	$-20\text{ to }+60$	°C	At 50% RH

1.5 Electrical Characteristics

$V_{DD} = 5\text{ V} \pm 5\%$, $V_{SS} = 0\text{ V}$, $T_a = 0^\circ\text{C to }50^\circ\text{C}$

Item		Symbol	Condition	Min.	Typ.	Max.	Unit
Input voltage*	High	V_{IH1}		2.2	–	V_{DD}	V
	Low	V_{IL1}		0	–	0.6	V
Output voltage**	High	V_{OH1}	$-I_{OH} = 0.205\text{ mA}$	2.4	–	–	V
	Low	V_{OL1}	$I_{OL} = 1.2\text{ mA}$	–	–	0.4	V
Power supply voltage		V_{DD}		4.75	5.00	5.25	V
		$V_{DD}-V_{LC}$		1.5	–	–	V
Current consumption		I_{DD}		–	2.0	3.0	mA
		I_{LC}	$V_{LC} = 0.25\text{ V}$	–	0.2	1.0	mA
Clock oscillation freq.		f_{osc}	Resistance oscillation	190	270	350	kHz

* Applied to DB₀ to DB₇, E, $\overline{R/W}$, and RS
** Applied to DB₀ to DB₇

Remark: Recommended operating voltage

The viewing angle and screen contrast of the LCD panel can be varied by changing the liquid crystal operating voltage (V_{opr}), that is V_{LC} .
The optical characteristics is influenced by an ambient temperature. The recommended value of V_{opr} for an ambient temperatures are shown below.

Temperature (°C)	0	10	25	40	50
V_{opr} (V)	5.00	4.90	4.75	4.60	4.50

$V_{opr} = V_{DD} - V_{LC}$

1.4 Absolute Maximum Ratings

$V_{22} = 0V$

Item	Symbol	Standard	Unit	Remarks
Power supply voltage	V_{DD}	$-0.3V \sim +7.5V$	V	
Input voltage	V_{in}	$V_{DD} - 1.5V \sim V_{DD} + 0.3V$	V	
Output voltage	V_{out}	$-0.3V \sim V_{DD} + 0.3V$	V	
Operating temperature	T_{op}	$0^{\circ}C \sim +50^{\circ}C$	$^{\circ}C$	
Storage temperature	T_{stg}	$-20^{\circ}C \sim +80^{\circ}C$	$^{\circ}C$	at 20W RH

1.5 Electrical Characteristics

$V_{DD} = 5V \pm 5\%, V_{22} = 0V, T_a = 0^{\circ}C \sim 50^{\circ}C$

Item		Symbol	Condition	Min	Typ	Max	Unit
Input voltage*	High	V_{IH}		2.2	-	-	V
	Low	V_{IL}		0	-	0.8	V
Output voltage*	High	V_{OH}	$I_{OH} = 0.10mA$	2.4	-	-	V
	Low	V_{OL}	$I_{OL} = 1.2mA$	-	-	0.4	V
Power supply voltage		V_{DD}		4.75	5.00	5.25	V
		V_{DD-1}		1.2	-	-	V
Current consumption	IDD			-	2.0	3.0	mA
	Ic		$V_{CE} = 0.25V$	-	0.7	1.0	mA
Dist. oscillation freq	fosc		Resonance oscillation	180	270	380	kHz

* Applied to DB9 to DB7, E, RWV, and R2
** Applied to DB9 to DB7

Remark: Recommended operating voltage

The viewing angle and screen contrast of the LCD panel can be varied by changing the liquid crystal operating voltage (V_{op}), that is V_{CE} .
The optical characteristics is influenced by an ambient temperature. The recommended value of V_{op} for an ambient temperatures are shown below.

V_{op} (V)	Temperature (°C)
2.00	0
4.50	10
4.75	25
4.80	40
4.50	50

$V_{op} = V_{DD} - V_{CE}$

1.6 Timing Characteristics

1.6.1 Write operation

$V_{DD} = 5.0V \pm 5\%$, $V_{SS} = 0V$, $T_a = 0^{\circ}C$ to $50^{\circ}C$

Item		Symbol	Min.	Max.	Unit
Enable cycle time		t_{CYCE}	1000	–	ns
Enable pulse width	High level	PW_{EH}	450	–	ns
Enable rise and fall time		t_{Er}, t_{Ef}	–	25	ns
Setup time	$RS, R/\overline{W} \rightarrow E$	t_{AS}	140	–	ns
Address hold time		t_{AH}	10	–	ns
Data setup time		t_{DSW}	195	–	ns
Data hold time		t_H	10	–	ns

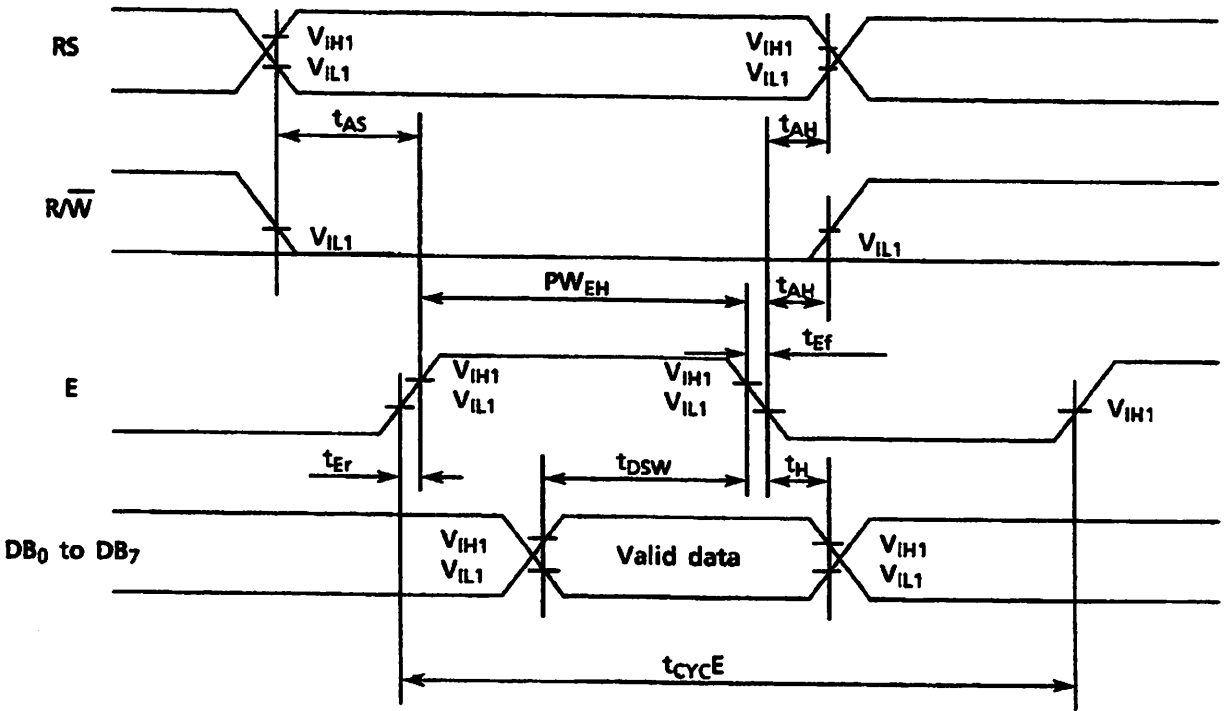
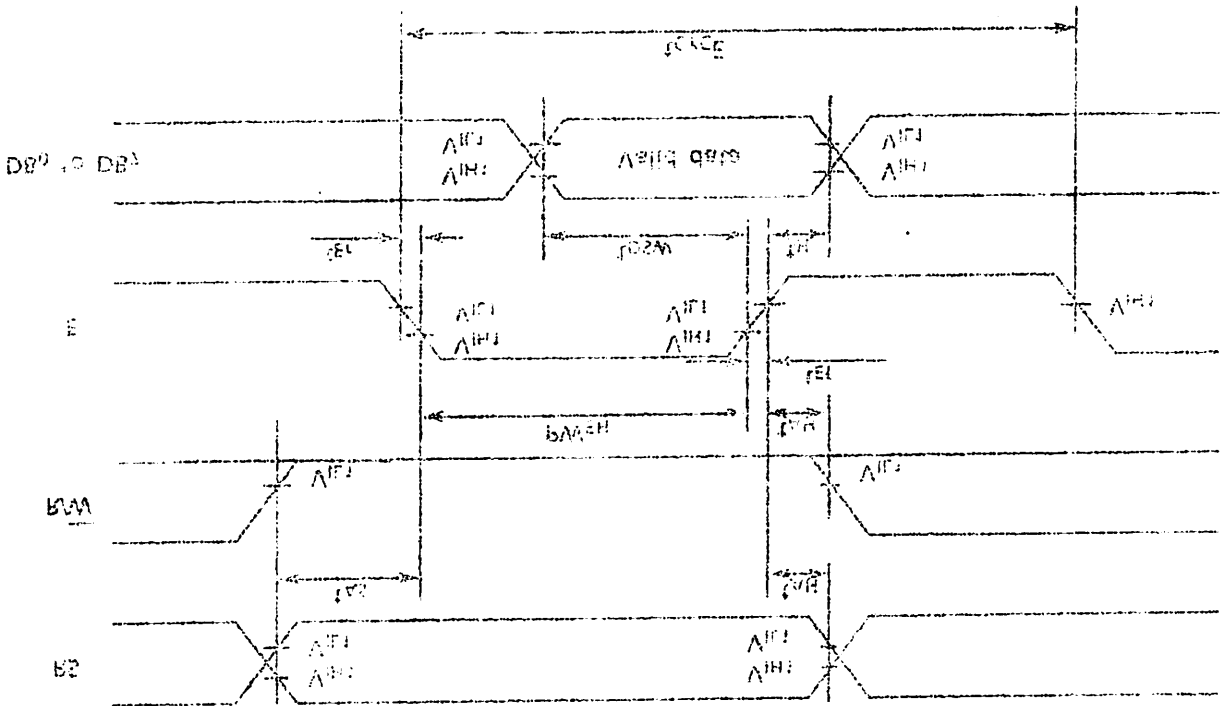


Figure 2 Data write from MPU to module

Figure 3 Data write from MB0 to memory



Data hold time	tH	10	-	ns
Data setup time	tDSM	120	-	ns
Address hold time	tAH	10	-	ns
Setup time	B2, B0 → E	140	-	ns
Enable rise and fall time	tEHL	-	50	ns
Enable pulse width	High level	tDWH	620	ns
Enable cycle time	tCYC	1000	-	ns
Power	2.5V/10V	Min	Max	Unit

$$V_{DD} = 2.0V \pm 20\%, V_{SS} = 0V, T = 0^\circ C \text{ to } 20^\circ C$$

1.6.1 Write operation

1.6 Timing Characteristics

1.6.2 Read operation

$V_{DD} = 5.0V \pm 5\%$, $V_{SS} = 0V$, $T_a = 0^{\circ}C$ to $50^{\circ}C$

Item		Symbol	Min.	Max.	Unit
Enable cycle time		t_{CYCE}	1000	–	ns
Enable pulse width	High level	PW_{EH}	450	–	ns
Enable rise and fall time		t_{Er}, t_{Ef}	–	25	ns
Setup time	$RS, \overline{R/W} \rightarrow E$	t_{AS}	140	–	ns
Address hold time		t_{AH}	10	–	ns
Data delay time		t_{DDR}	–	320	ns
Data hold time		t_H	20	–	ns

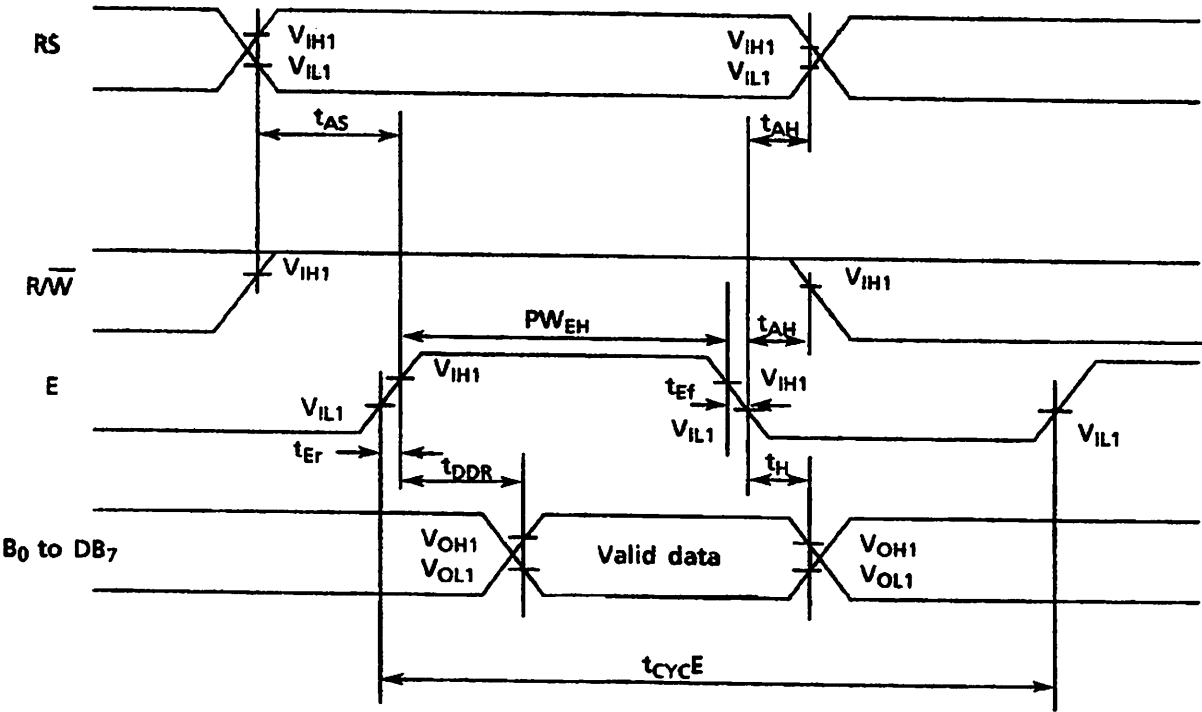


Figure 3 Data read from module to MPU

1.7 Optical Characteristics

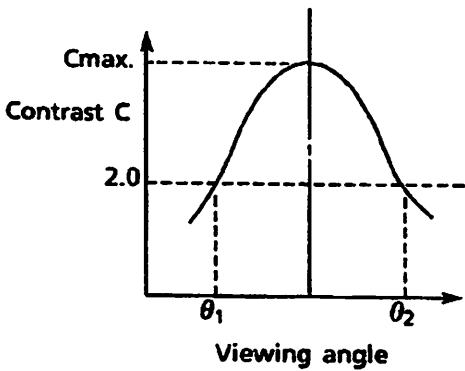
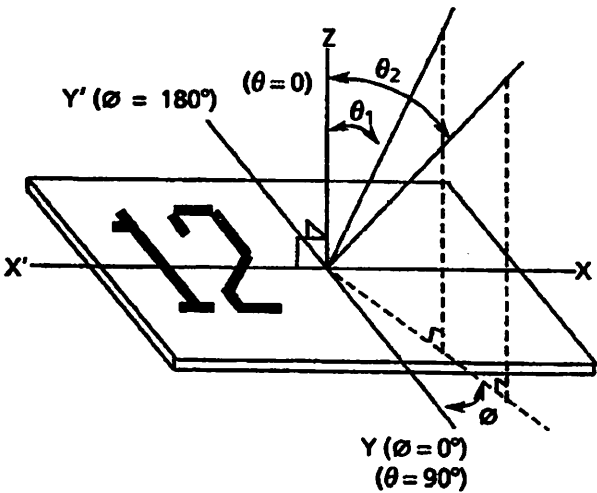
1.7.1 Optical characteristics (TN LCD)

Viewing angle: 6 o'clock ($\varnothing = 0^\circ$)
 $T_a = 25^\circ\text{C}$, $V_{opr} = 4.75\text{ V}$

Item	Symbol	Conditions	Min.	Typ.	Max.	Remarks
Viewing angle	$\theta_2 - \theta_1$	$C \geq 2.0$, $\varnothing = 0^\circ$	35	-	-	See Notes 1 and 2.
Contrast	C	$\theta = 25^\circ$, $\varnothing = 0^\circ$	5	8	-	See Note 3.
Response time (rise)	t_{on}	$\theta = 25^\circ$, $\varnothing = 0^\circ$	-	60 ms	70 ms	See Note 4.
Response time (fall)	t_{off}	$\theta = 25^\circ$, $\varnothing = 0^\circ$	-	150 ms	170 ms	See Note 4.

Note 1: Definition of angles $\varnothing$ and θ

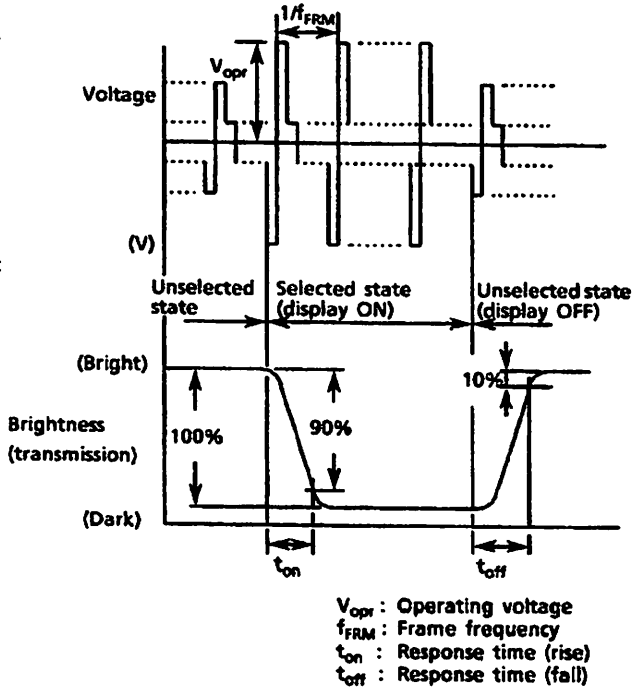
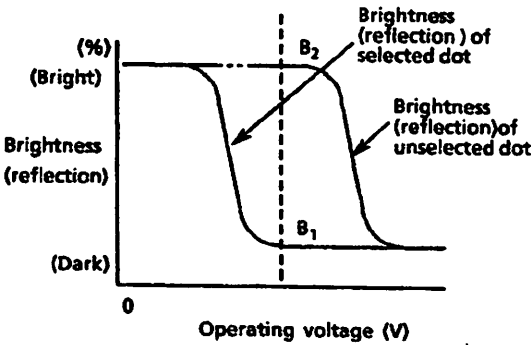
Note 2: Definition of viewing angles θ_1 and θ_2



Note 3: Definition of contrast C

Note 4: Definition of response time

$$C = \frac{\text{Brightness (reflection) of unselected dot (B2)}}{\text{Brightness (reflection) of selected dot (B1)}}$$



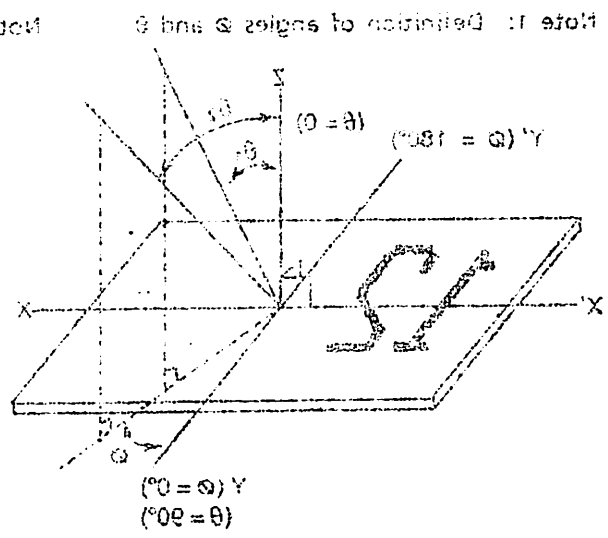
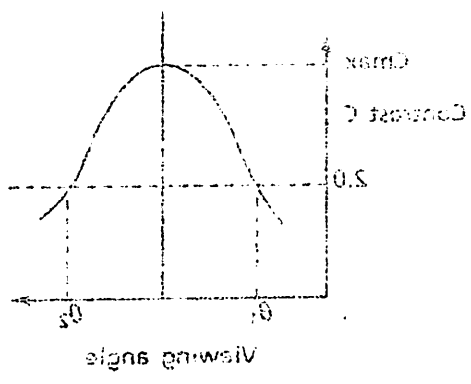
1.7 Optical Characteristics

1.7.1 Optical characteristics (TN LCD)

Item	Symbol	Conditions	Min	Typ	Max	Remarks
Viewing angle	$\theta_x - \theta_y$	$\theta = 25^\circ, \phi = 0^\circ$	38	-	-	See Note 1 and 2
Contrast	C	$\theta = 25^\circ, \phi = 0^\circ$	5	9	-	See Note 3
Response time (rise)	t_{on}	$\theta = 25^\circ, \phi = 0^\circ$	-	60 ms	70 ms	See Note 4
Response time (fall)	t_{off}	$\theta = 25^\circ, \phi = 0^\circ$	-	120 ms	170 ms	See Note 4

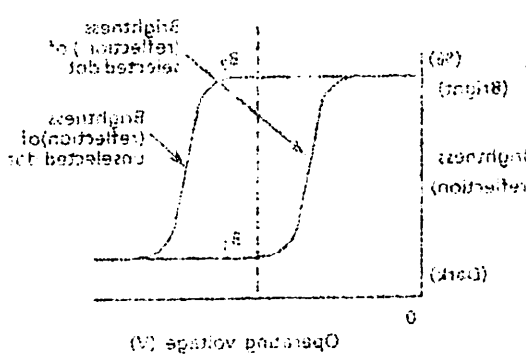
Viewing angle: ϕ (clock) ($\phi = 0^\circ$)
 $\theta = 25^\circ, V_{rms} = 4.5V$

Note 2: Definition of viewing angles θ_x and θ_y

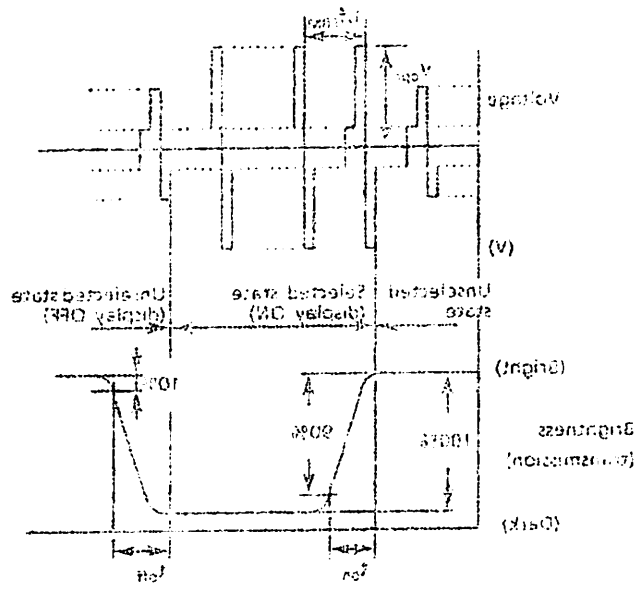


Note 3: Definition of contrast C

$$C = \frac{\text{Brightness (reflected) of unrelated dot (B2)}}{\text{Brightness (reflected) of related dot (B1)}}$$

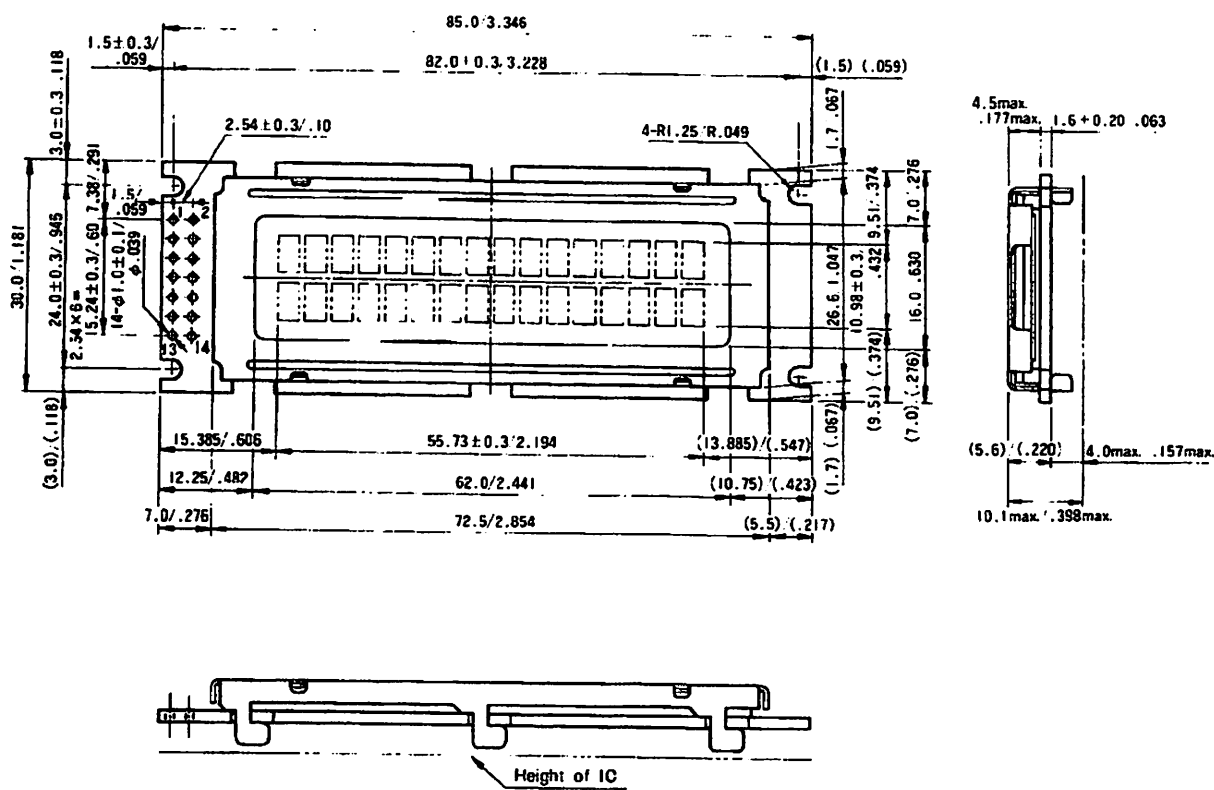


Note 4: Definition of response time



V_{rms} : Operated voltage
 f_{frame} : Frame frequency
 t_{on} : Response time (rise)
 t_{off} : Response time (fall)

1.8 Dimensions



Unit : mm/inch
General tolerance : $\pm 0.5 \text{ mm}$

I/O terminal symbol

No.	Symbol
1	DB ₇
2	DB ₆
3	DB ₅
4	DB ₄
5	DB ₃
6	DB ₂
7	DB ₁
8	DB ₀
9	E
10	R/W
11	RS
12	V _{LC}
13	V _{SS}
14	V _{DD}

Figure 4

. OPERATING INSTRUCTIONS

2.1 Terminal Functions

Table 1 Terminal functions

Signal name	No. of terminals	I/O	Destination	Function
DB ₀ to DB ₃	4	I/O	MPU	Tristate bidirectional lower four data buses: Data is read from the module to the MPU or written to the module from the MPU through the buses. If the interface data is 4 bits, the signals are not used.
DB ₄ to DB ₇	4	I/O	MPU	Tristate bidirectional upper four data buses: Data is read from the module to the MPU or written to the module from the MPU through the buses. DB ₇ is also used as a busy flag.
E	1	Input	MPU	Operation start signal: The signal activates data write or read.
R/W	1	Input	MPU	Read (R) and Write ($\overline{W}$) selection signals 0 : Write 1 : Read
RS	1	Input	MPU	Register selection signals 0 : Instruction register (Write) Busy flag and address counter (Read) 1 : Data register (Write and Read)
V _{LC}	1	—	Power supply	Power supply terminal for driving liquid crystal display: The screen contrast can be varied by changing V _{LC} .
V _{DD}	1	—	Power supply	+5V
V _{SS}	1	—	Power supply	Ground terminal: 0V

OPERATING INSTRUCTIONS

2.1 Terminal Functions

Table 1 Terminal functions

Signal name	No. of pins	I/O	Destination	Function
DB0 to DB3	4	I/O	MPU	Tristate bidirectional lower four data buses: Data is read from the module to the MPU or written to the module from the MPU through the buses. If the interface data is 4 bits, the signals are not used.
DB4 to DB7	4	I/O	MPU	Tristate bidirectional upper four data buses: Data is read from the module to the MPU or written to the module from the MPU through the buses. DB7 is also used as a busy flag.
E	1	input	MPU	Operation start signal. The signal activates data write or read.
R/W	1	input	MPU	Read (R) and Write (W) selection signals 0 : Write 1 : Read
R2	1	input	MPU	Register selection signals 0 : instruction register (Write) Busy flag and address counter (Read) 1 : Data register (Write and Read)
VLC	1	-	Power supply	Power supply terminal for driving liquid crystal display. The screen contrast can be varied by changing VLC.
Vcc	1	-	Power supply	+ 5 V
Vss	1	-	Power supply	Ground terminal. 0 V

2 Basic Operations

2.2.1 Registers

The controller has two kinds of eight-bit registers: the instruction register (IR) and the data register (DR). They are selected by the register select (RS) signal as shown in Table 2.

The IR stores instruction codes such as Display Clear and Cursor Shift, and the address information of display data RAM (DD RAM) and character generator RAM (CG RAM). They can be written from the MPU, but cannot be read to the MPU.

The DR temporarily stores data to be written into DD RAM or CG RAM, or read from DD RAM or CG RAM. When data is written into DD RAM or CG RAM from the MPU, the data in the DR is automatically written into DD RAM or CG RAM by internal operation. However, when data is read from DD RAM or CG RAM, the necessary data address is written into the IR. The specified data is read out to the DR and then the MPU reads it from the DR. After the read operation, the next address is set and DD RAM or CG RAM data at the address is read into the DR for the next read operation.

Table 2 Register selection

RS	$\overline{R/W}$	Operation
0	0	IR selection, IR write. Internal operation : Display clear
0	1	Busy flag (DB ₇) and address counter (DB ₀ to DB ₆) read
1	0	DR selection, DR write. Internal operation : DR to DD RAM or CG RAM
1	1	DR selection, DR read. Internal operation : DD RAM or CG RAM to DR

2.2.2 Busy flag (BF)

The flag indicates whether the module is ready to accept the next instruction. As shown in Table 2, the signal is output to DB₇ if RS = 0 and $\overline{R/W}$ = 1. If the value is 1, the module is working internally and the instruction cannot be accepted. If the value is 0, the next instruction can be written. Therefore, the flag status needs to be checked before executing an instruction. If an instruction is executed without checking the flag status, wait for more than the execution time shown by 2.4 Instruction Outline.

the execution time shown by 3.4 Instruction Outline.
Instruction is executed without checking the flag status, wait for more than
the flag status needs to be checked before executing an instruction. If an
accepted. If the value is 0, the next instruction can be written. Therefore,
value is 1, the module is working internally and the instruction cannot be
as shown in Table 3, the signal is output to DB₁ if $RS = 0$ and $R\overline{W} = 1$. If the
the flag indicates whether the module is ready to accept the next instruction.

3.3.3 Busy flag (BF)

1	0	DB selection: DB ready	internal operation: DD RAM or CC RAM to DB
1	0	DB selection: DB write	internal operation: DB to DD RAM or CC RAM
0	1	busy flag (DB ₁) and address counter (DB ₀ to DB ₆) ready	
0	0	is selection: is write	internal operation: display clear
RS	$R\overline{W}$	Operation	

Table 3 Register selection

is read into the DB for the next read operation.
operation, the next address is set and DD RAM or CC RAM data at the address
read out to the DB and then the MPU reads it from the DB. After the read
RAM, the necessary data address is written into the IB. The specified data is
RAM by internal operation. However, when data is read from DD RAM or CC
from the MPU, the data in the DB is automatically written into DD RAM or CC
from DD RAM or CC RAM. When data is written into DD RAM or CC RAM
the DB temporarily stores data to be written into DD RAM or CC RAM, or read

MPU.

RAM (CC RAM). They can be written from the MPU, but cannot be read to the
address information of display data RAM (DD RAM) and character generator.
The IB stores instruction codes such as Display Clear and Cursor Shift, and the

as shown in Table 3.

and the data register (DB). They are selected by the register select (RS) signal.
The controller has two kinds of eight-bit registers: the instruction register (IR)

3.3.1 Registers

3 Basic Operations

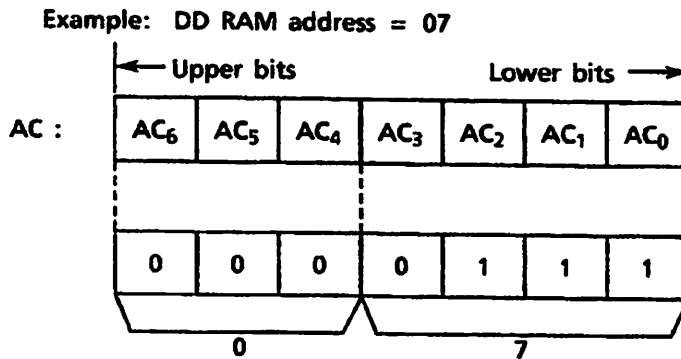
2.2.3 Address counter (AC)

The counter specifies an address when data is written into DD RAM or CG RAM and the data stored in DD RAM or CG RAM is read out. If an Address Set instruction (for DD RAM or CG RAM) is written in the IR, the address information is transferred from the IR to the AC. When display data is written into or read from DD RAM or CG RAM, the AC is automatically incremented or decremented by one according to the Entry Mode Set. The contents of the AC are output to DB₀ to DB₆ as shown in Table 2 if RS = 0 and $\overline{R/W} = 1$.

2.2.4 Display data RAM (DD RAM)

DD RAM has a capacity of up to 80×8 bits and stores display data of 80 eight-bit character codes. Some storage areas of DD RAM which are not used for display can be used as general data RAM.

A DD RAM address to be set in the AC is expressed in hexadecimal form as follows.



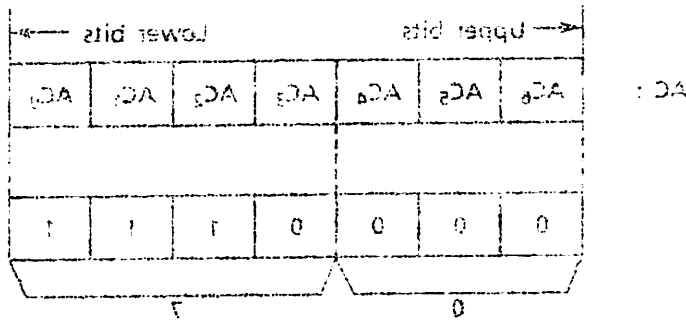
3.2.3 Address counter (AC)

The counter specifies an address when data is written into DD RAM or CG RAM and the data stored in DD RAM or CG RAM is read out. If an Address Set instruction (for DD RAM or CG RAM) is written in the IR, the address information is transferred from the IR to the AC. When display data is written into or read from DD RAM or CG RAM, the AC is automatically incremented or decremented by one according to the Entry Mode Set. The contents of the AC are output to DB₄ to DB₈ as shown in Table 2 if RS = 0 and $\overline{R\overline{W}} = 1$.

3.2.4 Display data RAM (DD RAM)

DD RAM has a capacity of up to 80×8 bits and stores display data of 80 eight-bit character codes. Some storage areas of DD RAM which are not used for display can be used as general data RAM. A DD RAM address to be set in the AC is expressed in hexadecimal form as follows.

Example: DD RAM address = 07



DD RAM addresses 00H to 0FH are set in the line 1, and 40H to 4FH in the line 2.

Note : The addresses in the digit 16 of line 1 and the digit 1 of line 2 are not consecutive.

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	Display digit
Line 1	00	01	02	03	04	05	06	07	08	09	0A	0B	0C	0D	0E	0F	DD RAM address
Line 2	40	41	42	43	44	45	46	47	48	49	4A	4B	4C	4D	4E	4F	

If the display is shifted, DD RAM addresses 00H to 27H are displayed in line 1 and 40H to 67H in line 2. The following figures are examples of display shifts.

*Left shift

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	Display digit
Line 1	01	02	03	04	05	06	07	08	09	0A	0B	0C	0D	0E	0F	10	DD RAM address
Line 2	41	42	43	44	45	46	47	48	49	4A	4B	4C	4D	4E	4F	50	

*Right shift

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	Display digit
Line 1	27	00	01	02	03	04	05	06	07	08	09	0A	0B	0C	0D	0E	DD RAM address
Line 2	67	40	41	42	43	44	45	46	47	48	49	4A	4B	4C	4D	4E	

2.5 Character generator ROM (CG ROM)

Character generator ROM generates 192 types of 5 x 7 dot-matrix character patterns from eight-bit character codes.

Table 3 shows the correspondence between the CG ROM character codes and character patterns.

2.6 Character generator RAM (CG RAM)

CG RAM is used to create character patterns freely by programming. Eight types of character patterns can be written.

Table 4 shows the character patterns created from CG RAM addresses and data. To display a created character pattern, the character code in the left column of the table is written into DD RAM corresponding to the display position (digit). The areas not used for display are available as general data RAM.

DD RAM addresses 00H to 07H are set in the line 1, and 40H to 47H in the line 2.

Note : The addresses in the digit 18 of line 1 and the digit 1 of line 2 are not consecutive.

Line	Display digit																	
	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18
Line 1	00	01	02	03	04	05	06	07	08	09	0A	0B	0C	0D	0E	0F		
Line 2	40	41	42	43	44	45	46	47	48	49	4A	4B	4C	4D	4E	4F		

If the display is shifted, DD RAM addresses 00H to 3FH are displayed in line 1 and 40H to 67H in line 2. The following figures are examples of display shifts.

"Left shift"

Line	Display digit																	
	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18
Line 1	01	02	03	04	05	06	07	08	09	0A	0B	0C	0D	0E	0F			
Line 2	41	42	43	44	45	46	47	48	49	4A	4B	4C	4D	4E	4F	50		

"Right shift"

Line	Display digit																	
	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18
Line 1	10	00	01	02	03	04	05	06	07	08	09	0A	0B	0C	0D	0E		
Line 2	50	40	41	42	43	44	45	46	47	48	49	4A	4B	4C	4D	4E		

2.5 Character generator ROM (CG ROM)

Character generator ROM generates 182 types of 2 x 7 dot-matrix character patterns from eight-bit character codes.

Table 3 shows the correspondence between the CG ROM character codes and character patterns.

2.6 Character generator RAM (CG RAM)

CG RAM is used to create character patterns freely by programming. Right types of character patterns can be written.

Table 4 shows the character patterns created from CG RAM addresses and data. To display a created character pattern, the character code in the left column of the table is written into DD RAM corresponding to the display position (digit). The areas not used for display are available as general data RAM.

Table 3 Correspondence between character codes and character patterns

Upper 4 bits Lower 4 bits	0000	0010	0011	0100	0101	0110	0111	1010	1011	1100	1101	1110	1111
x x x x 0000	CG RAM (1)		0	1	2	3	4	5	6	7	8	9	A
x x x x 0001	(2)	:	;	4	5	6	7	8	9	A	B	C	D
x x x x 0010	(3)	"	2	3	4	5	6	7	8	9	A	B	C
x x x x 0011	(4)	#	3	4	5	6	7	8	9	A	B	C	D
x x x x 0100	(5)	*	4	5	6	7	8	9	A	B	C	D	E
x x x x 0101	(6)	%	5	6	7	8	9	A	B	C	D	E	F
x x x x 0110	(7)	&	6	7	8	9	A	B	C	D	E	F	G
x x x x 0111	(8)	'	7	8	9	A	B	C	D	E	F	G	H
x x x x 1000	(1)	(	8	9	A	B	C	D	E	F	G	H	I
x x x x 1001	(2)	)	9	A	B	C	D	E	F	G	H	I	J
x x x x 1010	(3)	*	#	J	K	L	M	N	O	P	Q	R	S
x x x x 1011	(4)	+	\$	K	L	M	N	O	P	Q	R	S	T
x x x x 1100	(5)	;	<	L	M	N	O	P	Q	R	S	T	U
x x x x 1101	(6)	---	=	M	N	O	P	Q	R	S	T	U	V
x x x x 1110	(7)	::	>	N	O	P	Q	R	S	T	U	V	W
x x x x 1111	(8)	/	?	O	P	Q	R	S	T	U	V	W	X

Table 3 Correspondence between character codes and character patterns

Lower 4 bits	Upper 4 bits																
		0000	0010	0011	0100	0101	0110	0111	1010	1011	1100	1101	1110	1111			
x x x x 0000	CG RAM (1)																
	(2)	!	!	!	!	!	!	!	!	!	!	!	!	!			
x x x x 0010	(3)	"	"	"	"	"	"	"	"	"	"	"	"	"			
	(4)	#	#	#	#	#	#	#	#	#	#	#	#	#			
x x x x 0011	(5)	\$	\$	\$	\$	\$	\$	\$	\$	\$	\$	\$	\$	\$			
	(6)	%	%	%	%	%	%	%	%	%	%	%	%	%			
x x x x 0101	(7)	&	&	&	&	&	&	&	&	&	&	&	&	&			
	(8)	'	'	'	'	'	'	'	'	'	'	'	'	'			
x x x x 0110	(9)	(	(	(	(	(	(	(	(	(	(	(	(	(			
	(10)	)	)	)	)	)	)	)	)	)	)	)	)	)			
x x x x 0111	(11)	*	*	*	*	*	*	*	*	*	*	*	*	*			
	(12)	+	+	+	+	+	+	+	+	+	+	+	+	+			
x x x x 1001	(13)	,	,	,	,	,	,	,	,	,	,	,	,	,			
	(14)	-	-	-	-	-	-	-	-	-	-	-	-	-			
x x x x 1101	(15)	.	.	.	.	.	.	.	.	.	.	.	.	.			
	(16)	/	/	/	/	/	/	/	/	/	/	/	/	/			
x x x x 1111	(17)	:	:	:	:	:	:	:	:	:	:	:	:	:			
	(18)	;	;	;	;	;	;	;	;	;	;	;	;	;			

Table 4 Relationships between CG RAM addresses and character codes (DD RAM) and character patterns (CG RAM data)

Character code (DD RAM data)	CG RAM address	Character pattern (CG RAM data)
7 6 5 4 3 2 1 0 ← Upper bit Lower bit →	5 4 3 2 1 0 ← Upper bit Lower bit →	7 6 5 4 3 2 1 0 ← Upper bit Lower bit →
0 0 0 0 * 0 0 0	0 0 0	
0 0 0 0 * 0 0 1	0 0 1	
0 0 0 0 * 1 1 1	1 1 1	

tes: • In CG RAM data, 1 corresponds to Selection and 0 to Non-selection on the display.

- Character code bits 0 to 2 and CG RAM address bits 3 to 5 correspond with each other (three bits, eight types).
- CG RAM address bits 0 to 2 specify a line position for a character pattern. Line 8 of a character pattern is the cursor position where the logical sum of the cursor and CG RAM data is displayed. Set the data of line 8 to 0 to display the cursor. If the data is changed to 1, one bit lights, regardless of the cursor.
- The character pattern column positions correspond to CG RAM data bits 0 to 4 and bit 4 comes to the left end. CG RAM data bits 5 to 7 are not displayed but can be used as general data RAM.
- When reading a character pattern from CG RAM, set to 0 all of character code bits 4 to 7. Bits 0 to 2 determine which pattern will be read out. Since bit 3 is not valid, 00H and 08H select the same character.

1.3 Instruction Outline

Table 5 List of instructions

Instruction	Code										Function	Execution time [#]
	RS	R/W	DB ₇	DB ₆	DB ₅	DB ₄	DB ₃	DB ₂	DB ₁	DB ₀		
(1) Display clear	0	0	0	0	0	0	0	0	0	1	Clears all display and returns cursor to home position (address 0)	1.64 ms
(2) Cursor Home	0	0	0	0	0	0	0	0	1	*	Returns cursor to home position. Shifted display returns to home position and DD RAM contents do not change.	1.64 ms
(3) Entry Mode Set	0	0	0	0	0	0	0	1	I/D	S	Sets direction of cursor movement and whether display will be shifted when data is written or read	40 μs
(4) Display ON/OFF control	0	0	0	0	0	0	1	D	C	B	Turns ON/OFF total display (D) and cursor (C), and makes cursor position column start blinking (B)	40 μs
(5) Cursor/Display Shift	0	0	0	0	0	1	S/C	R/L	*	*	Moves cursor and shifts display without changing DD RAM contents	40 μs
(6) Function Set	0	0	0	0	1	DL	N	F	*	*	Sets interface data length (DL), the number of display lines (N), and character fonts (F)	40 μs
(7) CG RAM Address Set	0	0	0	1	A _{CG}						Sets CG RAM address to start transmitting or receiving CG RAM data	40 μs
(8) DD RAM Address Set	0	0	1	A _{DD}							Sets DD RAM address to start transmitting or receiving DD RAM data	40 μs
(9) BF/Address Read	0	1	BF	AC							Reads BF indicating module in internal operation and AC contents (used for both CG RAM and DD RAM)	0 μs
(10) Data Write to CG RAM or DD RAM	1	0	Write Data								Writes data into DD RAM or CG RAM	40 μs
(11) Data Read from CG RAM or DD RAM	1	1	Read Data								Reads data from DD RAM or CG RAM	40 μs

- * : Invalid bit

A_{CG}: CG RAM address

A_{DD}: DD RAM address

AC: Address counter
- I/D = 1 : Increment

I/D = 0 : Decrement
- B = 1 : Blink ON

B = 0 : Blink OFF
- N = 1 : 2 lines

N = 0 : 1 line
- S = 1 : Display shift

S = 0 : No display shift
- S/C = 1 : Display shift

S/C = 0 : Cursor movement
- F = 1 : 5×10 dot matrix

F = 0 : 5×7 dot matrix
- D = 1 : Display ON

D = 0 : Display OFF
- R/L = 1 : Right shift

R/L = 0 : Left shift
- BF = 1 : Internal operation in progress

BF = 0 : Instruction can be accepted
- C = 1 : Cursor ON

C = 0 : Cursor OFF
- DL = 1 : 8 bits

DL = 0 : 4 bits

[#] An execution time indicates maximum value when f_{osc} is 250 kHz. It changes at the inverse proportion of f_{osc}.

Table 2 List of instructions

Instruction	Code	Function										Execution time
		OP	RD	WR	OP	RD	WR	OP	RD	WR	OP	
(1) Display clear	0	0	0	0	0	0	0	0	0	0	0	10ms
(2) Cursor home	2	0	0	0	0	0	0	0	0	0	0	10ms
(3) Entry mode set	3	0	0	0	0	0	0	0	0	0	0	40µs
(4) Display ON/OFF control	4	0	0	0	0	0	0	0	0	0	0	40µs
(5) Cursor display shift	5	0	0	0	0	0	0	0	0	0	0	40µs
(6) Function set	6	0	0	0	0	0	0	0	0	0	0	40µs
(7) CG RAM Address set	7	0	0	0	0	0	0	0	0	0	0	40µs
(8) CG RAM Address set	8	0	0	0	0	0	0	0	0	0	0	40µs
(9) Address Read	9	0	0	0	0	0	0	0	0	0	0	40µs
(10) Data Write to CG RAM or DD RAM	10	0	0	0	0	0	0	0	0	0	0	40µs
(11) Data Read from CG RAM or DD RAM	11	0	0	0	0	0	0	0	0	0	0	40µs

AC : Address counter
VDD : CG RAM address
VDD : DD RAM address
RD = 1 : Increment
RD = 0 : Decrement
WR = 1 : Increment
WR = 0 : Decrement
OP = 1 : Display ON
OP = 0 : Display OFF
C = 1 : Cursor ON
C = 0 : Cursor OFF
D = 1 : Display ON
D = 0 : Display OFF
2 = 0 : No display shift
2 = 1 : Display shift
XC = 0 : Cursor movement
XC = 1 : Display shift
BF = 1 : Internal operation in progress
BF = 0 : Instruction can be accepted
D = 1 : 8 bit
D = 0 : 4 bit
N = 1 : 5 lines
N = 0 : 1 line

* An execution time indicates maximum value when f_{osc} is 520 KHz. It changes at the inverse proportion of f_{osc}.

Instruction Details

(1) Display Clear

	RS	RAW	DB ₇							DB ₀
Code	0	0	0	0	0	0	0	0	0	1

Display Clear clears all display and returns cursor to home position (address 0). Space code 20 (hexadecimal) is written into all the addresses of DD RAM, and DD RAM address 0 is set to the AC. If shifted, the display returns to the original position. After execution of the Display Clear instruction, the entry mode is incremented.

Note : When executing the Display Clear instruction, follow the restrictions listed in Table 6.

(2) Cursor Home

	RS	RAW	DB ₇							DB ₀
Code	0	0	0	0	0	0	0	0	1	*

* : Don't care bit

Cursor Home returns cursor to home position (address 0). DD RAM address 0 is set to the AC. The cursor returns to the home position. If shifted, the display returns to the original position. The DD RAM contents do not change. If the cursor or blinking is ON, it returns to the left side.

Note : When executing the Cursor Home instruction, follow the restrictions listed in Table 6.

Table 6 Restrictions on execution of Display Clear and Cursor Home instructions

Conditions of use	Restrictions
When executing the Display Clear or Cursor Home instruction when the display is shifted (after execution of Display Shift instruction)	The Cursor Home instruction should be executed again immediately after the Display Clear or Cursor Home instruction is executed. Do not leave an interval of a multiple of $400/f_{osc}$ second after the first execution. Example: 1.5 ms, 3 ms, 4.5 ms for $f_{osc} = 270$ kHz * f_{osc} : Oscillation frequency
When 23 _H , 27 _H , 63 _H , or 67 _H is used as a DD RAM address to execute Cursor Home instruction	Before executing the Cursor Home instruction, the data of the four DD RAM addresses given at the left should be read and saved. After execution, write the data again in DD RAM. (This restriction is necessary to prevent the contents of the DD RAM addresses from being destroyed after the Cursor Home instruction has been executed.)

(3) Entry Mode Set

	RS	R/W	DB ₇							DB ₀
Code	0	0	0	0	0	0	0	1	I/D	S

Entry Mode Set sets the direction of cursor movement and whether display will be shifted.

I/D : The DD RAM address is incremented or decremented by one when a character code is written into or read from DD RAM. This is also true for writing into or reading from CG RAM.

When I/D = 1, the address is incremented by one and the cursor or blink moves to the right.

When I/D = 0, the address is decremented by one and the cursor or blink moves to the left.

S : If S = 1, the entire display is shifted either to the right or left for writing into DD RAM. The cursor position does not change, only the display moves. There is no display shift for reading from DD RAM.

When S = 1 and I/D = 1, the display shifts to the left.

When S = 1 and I/D = 0, the display shifts to the right.

If S = 0, the display does not shift.

(4) Display ON/OFF Control

	RS	R/W	DB ₇							DB ₀
Code	0	0	0	0	0	0	1	D	C	B

Display ON/OFF Control turns the total display and the cursor ON and OFF, and makes the cursor position start blinking. Cursor ON/OFF and blinking is done at the column indicated by the specified DD RAM address by the AC.

D : When D = 1, the display is turned ON.

When D = 0, the display is turned OFF.

If D = 0 is used, display data remains in DD RAM. Change 0 to 1 to display data.

C : When C = 1, the cursor is displayed.

When C = 0, the cursor is not displayed.

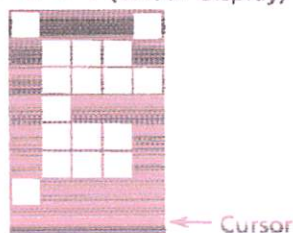
The cursor is displayed in the dot line below the character fonts.

B : When B = 1, the character at the cursor position starts blinking.

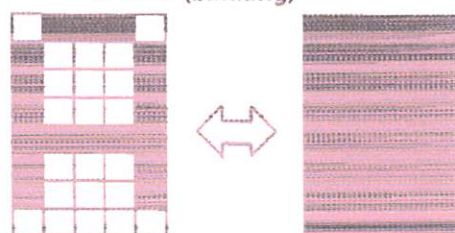
When B = 0, it does not blink.

For blinking, all-black dots and the character are switched about every 0.4 seconds when f_{osc} is 250 kHz. The cursor and blinking can be set at the same time.

Example: C = 1 (cursor display)



B = 1 (blinking)



(5) Cursor/Display Shift

	RS	R/W	DB ₇							DB ₀	
Code	0	0	0	0	0	1	S/C	R/L	*	*	* : Don't care bit

Cursor/Display Shift moves the cursor and shifts the display without changing the DD RAM contents.

The cursor position and the AC contents match. This instruction is available for display correction and retrieval because the cursor position or display can be shifted without writing or reading display data. Since the DD RAM capacity is 40-character by two lines, the cursor is shifted from digit 40 of line 1 to digit 1 of line 2. Displays of lines 1 and 2 are shifted at the same time. Therefore, the display pattern of line 2 is not shifted to line 1.

S/C	R/L	Operation
0	0	The cursor position is shifted to the left (the AC decrements one)
0	1	The cursor position is shifted to the right (the AC increments one)
1	0	The entire display is shifted to the left with the cursor
1	1	The entire display is shifted to the right with the cursor

Note: If only display shift is done, the AC contents do not change.

(6) Function Set

	RS	R/W	DB ₇							DB ₀	
Code	0	0	0	0	1	DL	N	F	*	*	* : Don't care bit

Function Set sets the interface data length, the number of display lines, and the character font.

DL : Interface data length

When DL = 1, the data length is set at eight bits (DB₇ to DB₀).

When DL = 0, the data length is set at four bits (DB₇ to DB₄).

The upper four bits are transferred first, then the lower four bits follow.

N : Number of display lines

When N = 1, the display line is set to two lines.

When N = 0, the display line is set to one line.

For M1632, set N to 1.

F : Character font

When F = 1, the character font is set to 5×10 dot matrix.

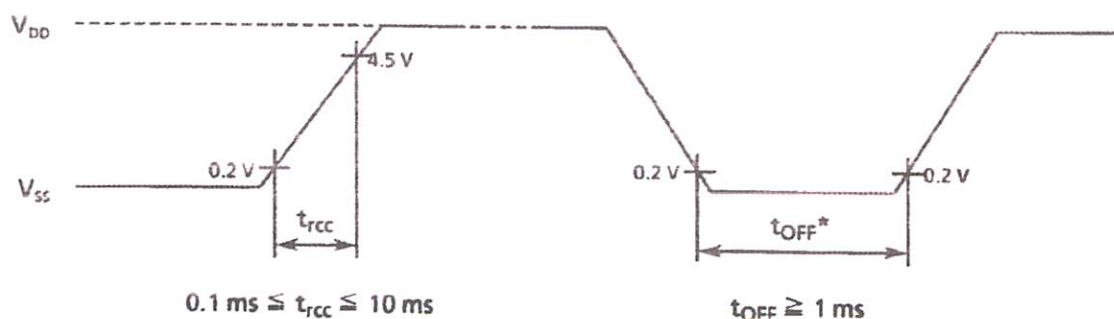
When F = 0, the character font is set to 5×7 dot matrix.

If N is set to 1, F becomes "Don't care bit". For M1632, set F to 0 or 1.

The Function Set instruction must be executed prior to all other instructions except for Busy Flag/Address Read. If another instruction is executed first, no function instruction except changing the interface data length can be executed.

Remarks: Initialization**1. Automatic initialization**

The system is automatically initialized at power-on if the following power supply conditions are satisfied.



* t_{OFF} : Time when power supply is OFF if cut instantaneously or turned ON and OFF repeatedly

The following instructions are executed for initialization.

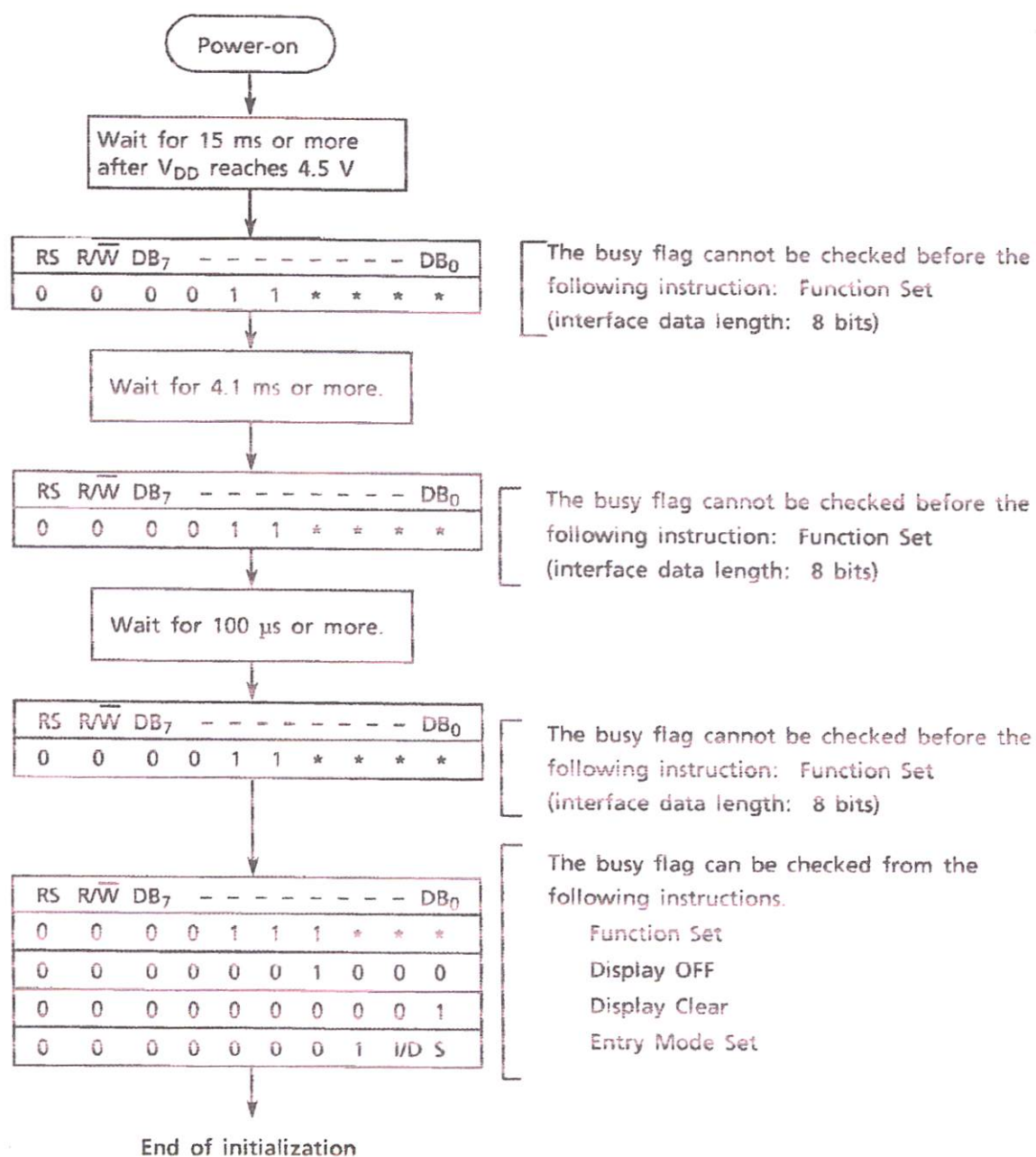
- Display Clear
- Function Set
 - DL = 1: Interface data length: Eight bits
 - N=0: One line display
 - F=0: Character font: 5×7 dot matrix
- Display ON/OFF Control
 - D = 0: Display OFF
 - C = 0: Cursor OFF
 - B = 0: Blink OFF
- Entry Mode Set
 - I/O = 1: Increment
 - S = 0: No display shift

Since the condition is not suitable for the M1632, further Function Set instruction is necessary.

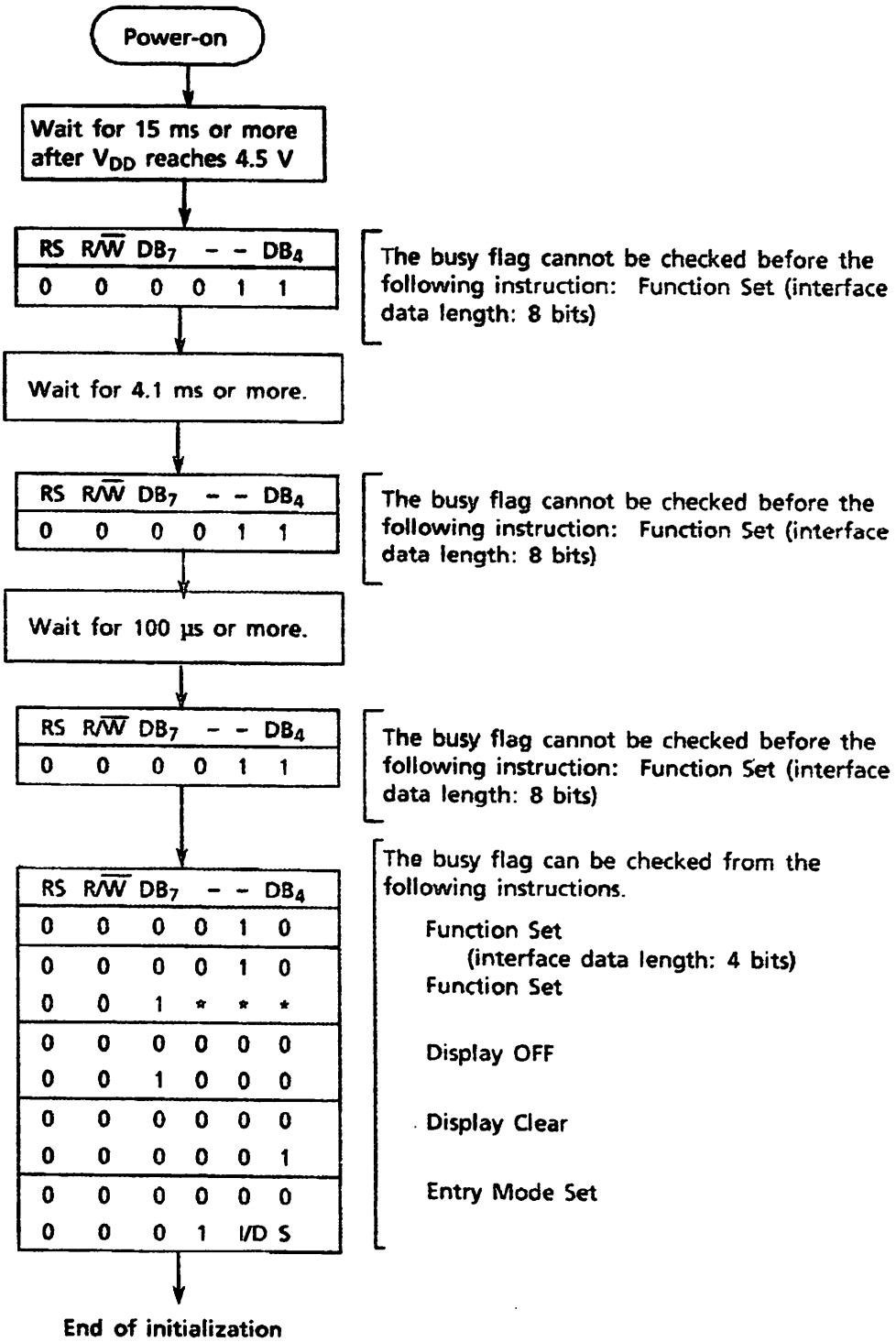
Initialization by instructions

If automatic initialization is not executed because the above power supply conditions are not satisfied, use the following instructions. Since it is unknown whether the interface data length is set to eight bits or four bits at power on, execute Function Set twice to set the interface data length to eight bits. And then for setting the required interface data length execute further Function Set instruction.

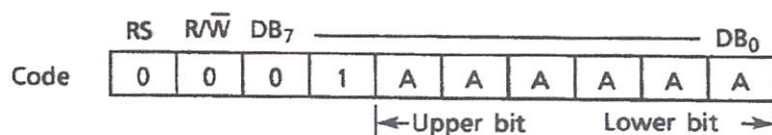
(a) Interface data length : Eight bits



(b) Interface data length: Four bits

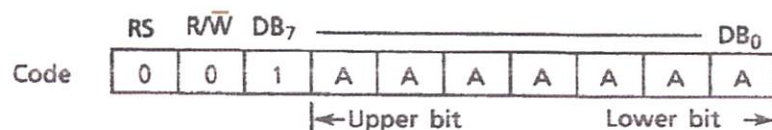


(7) CG RAM Address Set



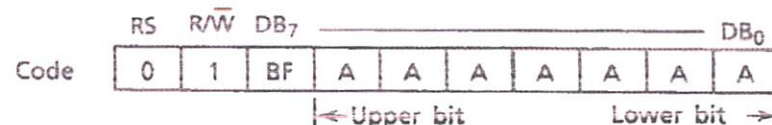
CG RAM addresses expressed as binary AAAAAA are set to the AC. Then data in CG RAM is written from or read to the MPU.

(8) DD RAM Address Set



DD RAM addresses expressed as binary AAAAAAA are set to the AC. Then data in DD RAM is written from or read to the MPU. The addresses used for display in line 1 (AAAAAAA) are 00H to 27H and those for line 2 (AAAAAAA) are 40H to 67H.

(9) Busy Flag/Address Read



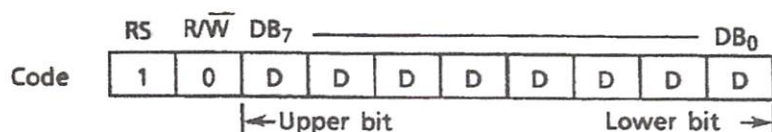
The BF signal is read out, indicating that the module is working internally because of the previous instruction.

When BF = 1, the module is working internally and the next instruction cannot be accepted until the BF value becomes 0.

When BF = 0, the next instruction can be accepted.

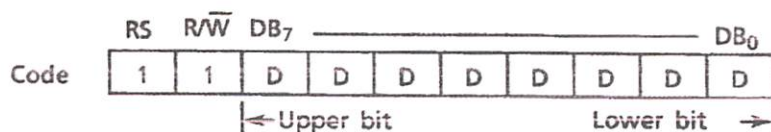
Therefore, make sure that BF = 0 before writing the next instruction. The AC values of binary AAAAAAA are read out at the same time as reading the busy flag. The AC addresses are used for both CG RAM and DD RAM but the address set before execution of the instruction determines which address is to be used.

(10) Data Write to CG RAM or DD RAM



Binary eight-bit data DDDDDDDD is written into CG RAM or DD RAM. The CG RAM Address Set instruction of (7) or the DD RAM Address Set instruction of (8) before this instruction selects either RAM. After the write operation, the address and display shift are determined by the entry mode setting.

(11) Data Read from CG RAM or DD RAM



Binary eight-bit data DDDDDDDD is read from CG RAM or DD RAM. The CG RAM Address Set instruction of (7) or the DD RAM Address Set instruction of (8) before this instruction selects either RAM. In addition, either instruction (7) or (8) must be executed immediately before this instruction. If no address set instruction is executed before a read instruction, the first data read becomes invalid. If read instructions are executed consecutively, data is normally read from the second time. However, if the cursor is shifted by the Cursor Shift instruction when reading DD RAM, there is no need to execute an address set instruction because the Cursor Shift instruction does this.

After the read operation, the address is automatically incremented or decremented by one according to the entry mode, but the display is not shifted.

Note : The AC is automatically incremented or decremented by one according to the entry mode after a write instruction is executed to write data in CG RAM or DD RAM. However, the data of the RAM selected by the AC are not read out even if a read instruction is executed immediately afterwards.

Correct data is read out under the following conditions.

- An address set instruction is executed immediately before readout.
- For DD RAM, the Cursor Shift instruction is executed immediately before readout.
- The second, or later, instruction is executed in consecutive execution of read instructions.

5 Examples of Instruction Use

2.5.1 Interface data length: Eight bits

No.	Instruction	Display	Operation										
1	Power-on <table><tr><td>RS</td><td>R/W</td><td>DB₇</td><td>—</td><td>DB₀</td></tr><tr><td></td><td></td><td colspan="3"></td></tr></table>	RS	R/W	DB ₇	—	DB ₀							The built-in reset circuit initializes the module.
RS	R/W	DB ₇	—	DB ₀									
2	Function Set <table><tr><td>RS</td><td>R/W</td><td>DB₇</td><td>—</td><td>DB₀</td></tr><tr><td>0</td><td>0</td><td>0</td><td>0 1 1 1</td><td>* * *</td></tr></table>	RS	R/W	DB ₇	—	DB ₀	0	0	0	0 1 1 1	* * *		The interface data length is set to 8 bits. The character format becomes 5 x 7 dot-matrix at 1/16 duty cycle.
RS	R/W	DB ₇	—	DB ₀									
0	0	0	0 1 1 1	* * *									
3	Display ON/OFF Control <table><tr><td>RS</td><td>R/W</td><td>DB₇</td><td>—</td><td>DB₀</td></tr><tr><td>0</td><td>0</td><td>0</td><td>0 0 0 1</td><td>1 1 0</td></tr></table>	RS	R/W	DB ₇	—	DB ₀	0	0	0	0 0 0 1	1 1 0		The display and cursor are turned ON, but nothing is displayed.
RS	R/W	DB ₇	—	DB ₀									
0	0	0	0 0 0 1	1 1 0									
4	Entry Mode Set <table><tr><td>RS</td><td>R/W</td><td>DB₇</td><td>—</td><td>DB₀</td></tr><tr><td>0</td><td>0</td><td>0</td><td>0 0 0 0</td><td>1 1 0</td></tr></table>	RS	R/W	DB ₇	—	DB ₀	0	0	0	0 0 0 0	1 1 0		The address is incremented by one and the cursor shifts to the right in a write operation to internal RAM. The display is not shifted.
RS	R/W	DB ₇	—	DB ₀									
0	0	0	0 0 0 0	1 1 0									
5	Write to CG RAM or DD RAM <table><tr><td>RS</td><td>R/W</td><td>DB₇</td><td>—</td><td>DB₀</td></tr><tr><td>1</td><td>0</td><td>0</td><td>1 0 0 1</td><td>1 0 0</td></tr></table>	RS	R/W	DB ₇	—	DB ₀	1	0	0	1 0 0 1	1 0 0		L is written. The AC is incremented by one and the cursor shifts to the right.
RS	R/W	DB ₇	—	DB ₀									
1	0	0	1 0 0 1	1 0 0									
6	Write to CG RAM or DD RAM <table><tr><td>RS</td><td>R/W</td><td>DB₇</td><td>—</td><td>DB₀</td></tr><tr><td>1</td><td>0</td><td>0</td><td>1 0 0 0</td><td>0 0 1 1</td></tr></table>	RS	R/W	DB ₇	—	DB ₀	1	0	0	1 0 0 0	0 0 1 1		C is written.
RS	R/W	DB ₇	—	DB ₀									
1	0	0	1 0 0 0	0 0 1 1									
7													
8	Write to CG RAM or DD RAM <table><tr><td>RS</td><td>R/W</td><td>DB₇</td><td>—</td><td>DB₀</td></tr><tr><td>1</td><td>0</td><td>0</td><td>0 1 1 0</td><td>0 0 1 0</td></tr></table>	RS	R/W	DB ₇	—	DB ₀	1	0	0	0 1 1 0	0 0 1 0		2 is written in digit 16. Cursor disappears.
RS	R/W	DB ₇	—	DB ₀									
1	0	0	0 1 1 0	0 0 1 0									

3.	Instruction	Display	Operation								
0	DD RAM address set <table><tr><td>RS</td><td>R/W</td><td>DB₇</td><td>DB₀</td></tr><tr><td>0</td><td>0</td><td>1 1 0 0 0 0 0 0</td><td></td></tr></table>	RS	R/W	DB ₇	DB ₀	0	0	1 1 0 0 0 0 0 0		LCD MODULE M1632 —	The DD RAM address is set so that the cursor appears at digit 1 of line 2.
RS	R/W	DB ₇	DB ₀								
0	0	1 1 0 0 0 0 0 0									
0	Write to CG RAM or DD RAM <table><tr><td>RS</td><td>R/W</td><td>DB₇</td><td>DB₀</td></tr><tr><td>1</td><td>0</td><td>0 0 1 1 0 0 0 1</td><td></td></tr></table>	RS	R/W	DB ₇	DB ₀	1	0	0 0 1 1 0 0 0 1		LCD MODULE M1632 1—	1 is written.
RS	R/W	DB ₇	DB ₀								
1	0	0 0 1 1 0 0 0 1									
1	Write to CG RAM or DD RAM <table><tr><td>RS</td><td>R/W</td><td>DB₇</td><td>DB₀</td></tr><tr><td>1</td><td>0</td><td>0 0 1 1 0 1 1 0</td><td></td></tr></table>	RS	R/W	DB ₇	DB ₀	1	0	0 0 1 1 0 1 1 0		LCD MODULE M1632 16—	6 is written.
RS	R/W	DB ₇	DB ₀								
1	0	0 0 1 1 0 1 1 0									
2											
3	Write to CG RAM or DD RAM <table><tr><td>RS</td><td>R/W</td><td>DB₇</td><td>DB₀</td></tr><tr><td>1</td><td>0</td><td>0 1 0 1 0 0 1 1</td><td></td></tr></table>	RS	R/W	DB ₇	DB ₀	1	0	0 1 0 1 0 0 1 1		LCD MODULE M1632 16DIGITS, 2LINES	5 is written.
RS	R/W	DB ₇	DB ₀								
1	0	0 1 0 1 0 0 1 1									
4	DD RAM address set <table><tr><td>RS</td><td>R/W</td><td>DB₇</td><td>DB₀</td></tr><tr><td>0</td><td>0</td><td>1 0 0 0 0 0 0 0</td><td></td></tr></table>	RS	R/W	DB ₇	DB ₀	0	0	1 0 0 0 0 0 0 0		LCD MODULE M1632 16DIGITS, 2LINES	The cursor returns to the home position.
RS	R/W	DB ₇	DB ₀								
0	0	1 0 0 0 0 0 0 0									
5	Display clear <table><tr><td>RS</td><td>R/W</td><td>DB₇</td><td>DB₀</td></tr><tr><td>0</td><td>0</td><td>0 0 0 0 0 0 0 1</td><td></td></tr></table>	RS	R/W	DB ₇	DB ₀	0	0	0 0 0 0 0 0 0 1		—	All the display disappears and the cursor remains at the home position.
RS	R/W	DB ₇	DB ₀								
0	0	0 0 0 0 0 0 0 1									
6											

2.5.2 Interface data length: Four bits

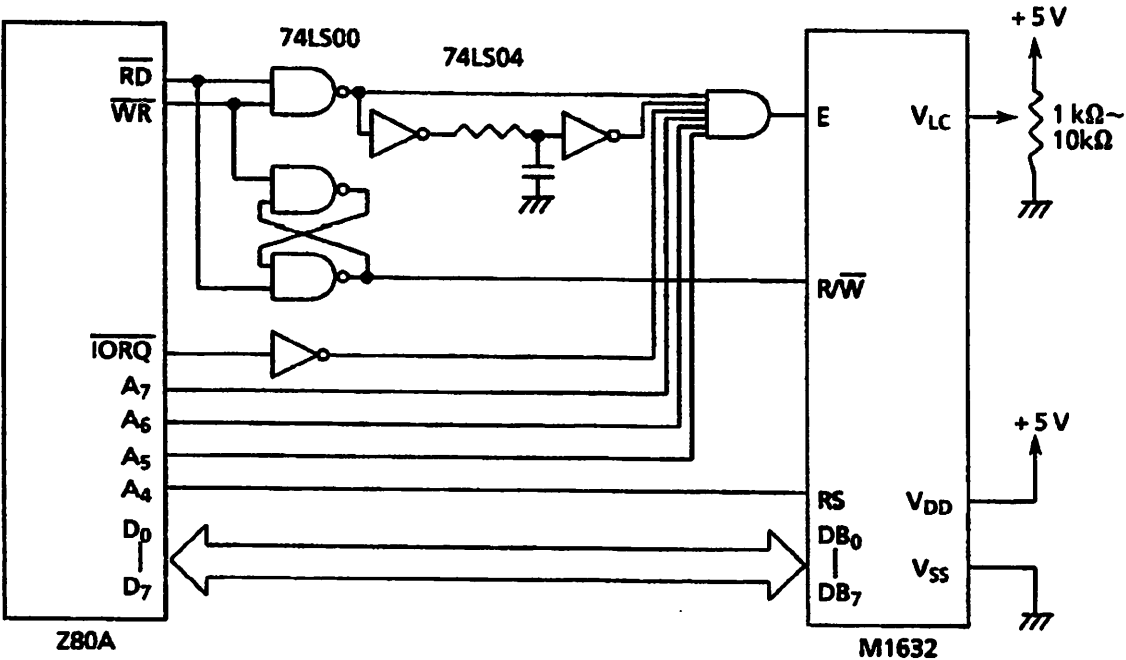
No.	Instruction	Display	Operation											
1	Power-on <table><tr><td>RS</td><td>R/W</td><td>DB₇ — DB₄</td></tr><tr><td>/</td><td>/</td><td>/</td></tr></table>	RS	R/W	DB ₇ — DB ₄	/	/	/	<table><tr><td></td></tr><tr><td></td></tr></table>			The built-in reset circuit initializes the module.			
RS	R/W	DB ₇ — DB ₄												
/	/	/												
2	Function Set <table><tr><td>RS</td><td>R/W</td><td>DB₇ — DB₄</td></tr><tr><td>0</td><td>0</td><td>0 0 1 0</td></tr><tr><td>/</td><td>/</td><td>/</td></tr></table>	RS	R/W	DB ₇ — DB ₄	0	0	0 0 1 0	/	/	/	<table><tr><td></td></tr><tr><td></td></tr></table>			Four-bit operation mode is set. *Eight-bit operation mode is set by initialization, and the instruction is executed only once.
RS	R/W	DB ₇ — DB ₄												
0	0	0 0 1 0												
/	/	/												
3	Function Set <table><tr><td>RS</td><td>R/W</td><td>DB₇ — DB₄</td></tr><tr><td>0</td><td>0</td><td>0 0 1 0</td></tr><tr><td>0</td><td>0</td><td>1 * * *</td></tr></table>	RS	R/W	DB ₇ — DB ₄	0	0	0 0 1 0	0	0	1 * * *	<table><tr><td></td></tr><tr><td></td></tr></table>			The 4-bit operation mode, 1/16 duty cycle, and 5 x 7 dot-matrix character format are selected. Then 4-bit operation mode starts.
RS	R/W	DB ₇ — DB ₄												
0	0	0 0 1 0												
0	0	1 * * *												
4	Display ON/OFF Control <table><tr><td>RS</td><td>R/W</td><td>DB₇ — DB₄</td></tr><tr><td>0</td><td>0</td><td>0 0 0 0</td></tr><tr><td>0</td><td>0</td><td>1 1 1 0</td></tr></table>	RS	R/W	DB ₇ — DB ₄	0	0	0 0 0 0	0	0	1 1 1 0	<table><tr><td>—</td></tr><tr><td></td></tr></table>	—		The display and cursor are turned ON, but nothing is displayed.
RS	R/W	DB ₇ — DB ₄												
0	0	0 0 0 0												
0	0	1 1 1 0												
—														
5	Entry Mode Set <table><tr><td>RS</td><td>R/W</td><td>DB₇ — DB₄</td></tr><tr><td>0</td><td>0</td><td>0 0 0 0</td></tr><tr><td>0</td><td>0</td><td>0 1 1 0</td></tr></table>	RS	R/W	DB ₇ — DB ₄	0	0	0 0 0 0	0	0	0 1 1 0	<table><tr><td>—</td></tr><tr><td></td></tr></table>	—		The address is incremented by one and the cursor shifts to the right in a write operation to internal RAM. The display is not shifted.
RS	R/W	DB ₇ — DB ₄												
0	0	0 0 0 0												
0	0	0 1 1 0												
—														
6	Write to CG RAM or DD RAM <table><tr><td>RS</td><td>R/W</td><td>DB₇ — DB₄</td></tr><tr><td>1</td><td>0</td><td>0 1 0 0</td></tr><tr><td>1</td><td>0</td><td>1 1 0 0</td></tr></table>	RS	R/W	DB ₇ — DB ₄	1	0	0 1 0 0	1	0	1 1 0 0	<table><tr><td>L —</td></tr><tr><td></td></tr></table>	L —		L is written. the AC is incremented by one and the cursor shifts to the right.
RS	R/W	DB ₇ — DB ₄												
1	0	0 1 0 0												
1	0	1 1 0 0												
L —														
7														

2.2.2 Interface data length: Four bits

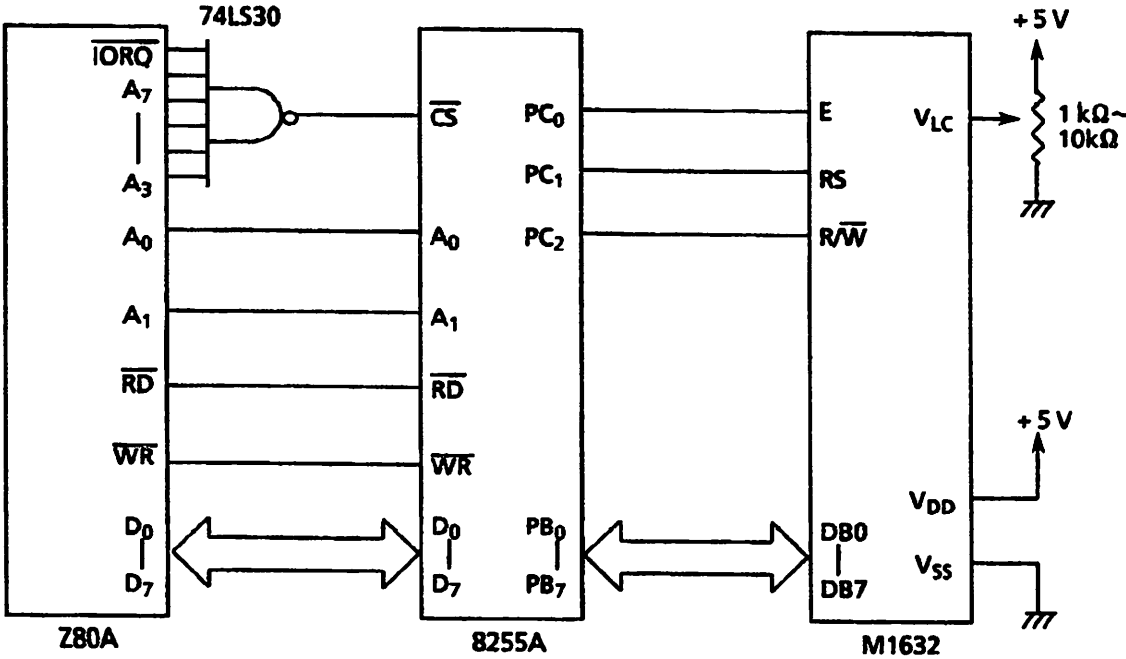
No.	Instruction	Display	Operation																			
1	<table><tr><td>RS</td><td>R/W</td><td>DB₇ — DB₄</td></tr><tr><td>0</td><td>0</td><td>0</td></tr><tr><td>0</td><td>0</td><td>0</td></tr><tr><td>0</td><td>0</td><td>0</td></tr><tr><td>0</td><td>0</td><td>0</td></tr></table>	RS	R/W	DB ₇ — DB ₄	0	0	0	0	0	0	0	0	0	0	0	0	<table><tr><td></td><td></td></tr><tr><td></td><td></td></tr></table>					The built-in reset circuit initializes the module.
RS	R/W	DB ₇ — DB ₄																				
0	0	0																				
0	0	0																				
0	0	0																				
0	0	0																				
2	<table><tr><td>RS</td><td>R/W</td><td>DB₇ — DB₄</td></tr><tr><td>0</td><td>0</td><td>0</td></tr><tr><td>0</td><td>0</td><td>0</td></tr><tr><td>0</td><td>0</td><td>0</td></tr><tr><td>0</td><td>0</td><td>0</td></tr></table>	RS	R/W	DB ₇ — DB ₄	0	0	0	0	0	0	0	0	0	0	0	0	<table><tr><td></td><td></td></tr><tr><td></td><td></td></tr></table>					Four-bit operation mode is set. "Eight-bit operation mode" is set by initialization, and the instruction is executed only once.
RS	R/W	DB ₇ — DB ₄																				
0	0	0																				
0	0	0																				
0	0	0																				
0	0	0																				
3	<table><tr><td>RS</td><td>R/W</td><td>DB₇ — DB₄</td></tr><tr><td>0</td><td>0</td><td>0</td></tr><tr><td>0</td><td>0</td><td>0</td></tr><tr><td>0</td><td>0</td><td>0</td></tr><tr><td>0</td><td>0</td><td>0</td></tr></table>	RS	R/W	DB ₇ — DB ₄	0	0	0	0	0	0	0	0	0	0	0	0	<table><tr><td></td><td></td></tr><tr><td></td><td></td></tr></table>					The 4-bit operation mode, 1/16 duty cycle, and 2 x 7 dot-matrix character format are selected. Then 4-bit operation mode starts.
RS	R/W	DB ₇ — DB ₄																				
0	0	0																				
0	0	0																				
0	0	0																				
0	0	0																				
4	<table><tr><td>RS</td><td>R/W</td><td>DB₇ — DB₄</td></tr><tr><td>0</td><td>0</td><td>0</td></tr><tr><td>0</td><td>0</td><td>0</td></tr><tr><td>0</td><td>0</td><td>0</td></tr><tr><td>0</td><td>0</td><td>0</td></tr></table>	RS	R/W	DB ₇ — DB ₄	0	0	0	0	0	0	0	0	0	0	0	0	<table><tr><td></td><td></td></tr><tr><td></td><td></td></tr></table>					The display and cursor are turned ON, but nothing is displayed.
RS	R/W	DB ₇ — DB ₄																				
0	0	0																				
0	0	0																				
0	0	0																				
0	0	0																				
5	<table><tr><td>RS</td><td>R/W</td><td>DB₇ — DB₄</td></tr><tr><td>0</td><td>0</td><td>0</td></tr><tr><td>0</td><td>0</td><td>0</td></tr><tr><td>0</td><td>0</td><td>0</td></tr><tr><td>0</td><td>0</td><td>0</td></tr></table>	RS	R/W	DB ₇ — DB ₄	0	0	0	0	0	0	0	0	0	0	0	0	<table><tr><td></td><td></td></tr><tr><td></td><td></td></tr></table>					The address is incremented by one and the cursor shifts to the right in a write operation to internal RAM. The display is not shifted.
RS	R/W	DB ₇ — DB ₄																				
0	0	0																				
0	0	0																				
0	0	0																				
0	0	0																				
6	<table><tr><td>RS</td><td>R/W</td><td>DB₇ — DB₄</td></tr><tr><td>1</td><td>0</td><td>0</td></tr><tr><td>0</td><td>0</td><td>0</td></tr><tr><td>0</td><td>0</td><td>0</td></tr><tr><td>0</td><td>0</td><td>0</td></tr></table>	RS	R/W	DB ₇ — DB ₄	1	0	0	0	0	0	0	0	0	0	0	0	<table><tr><td></td><td></td></tr><tr><td></td><td></td></tr></table>					1 is written to the AD0. The cursor shifts to the right.
RS	R/W	DB ₇ — DB ₄																				
1	0	0																				
0	0	0																				
0	0	0																				
0	0	0																				
7																						

MPU Connection Diagrams

.6.1 Z80A

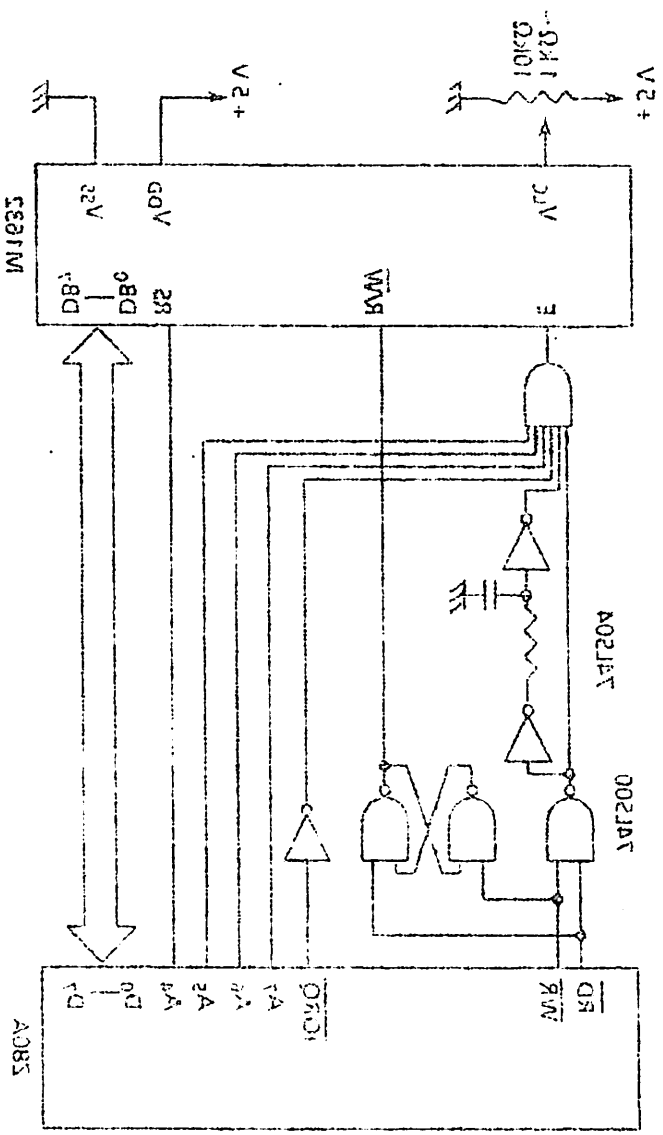


.6.2 Z80A and 8255A

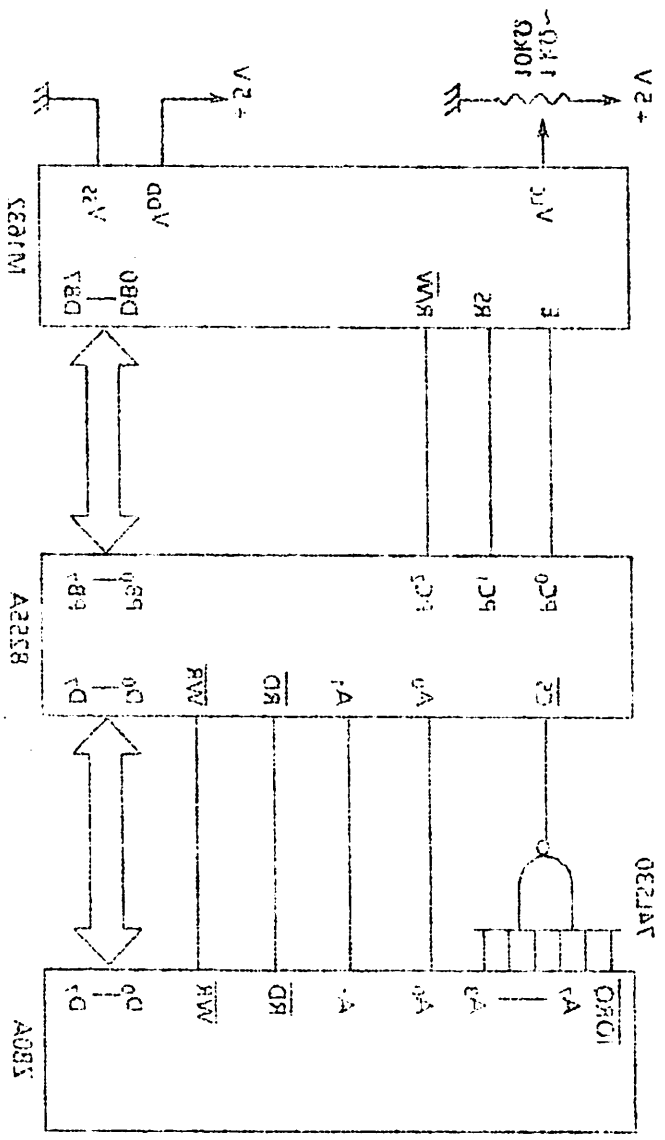


Вспомогательное устройство

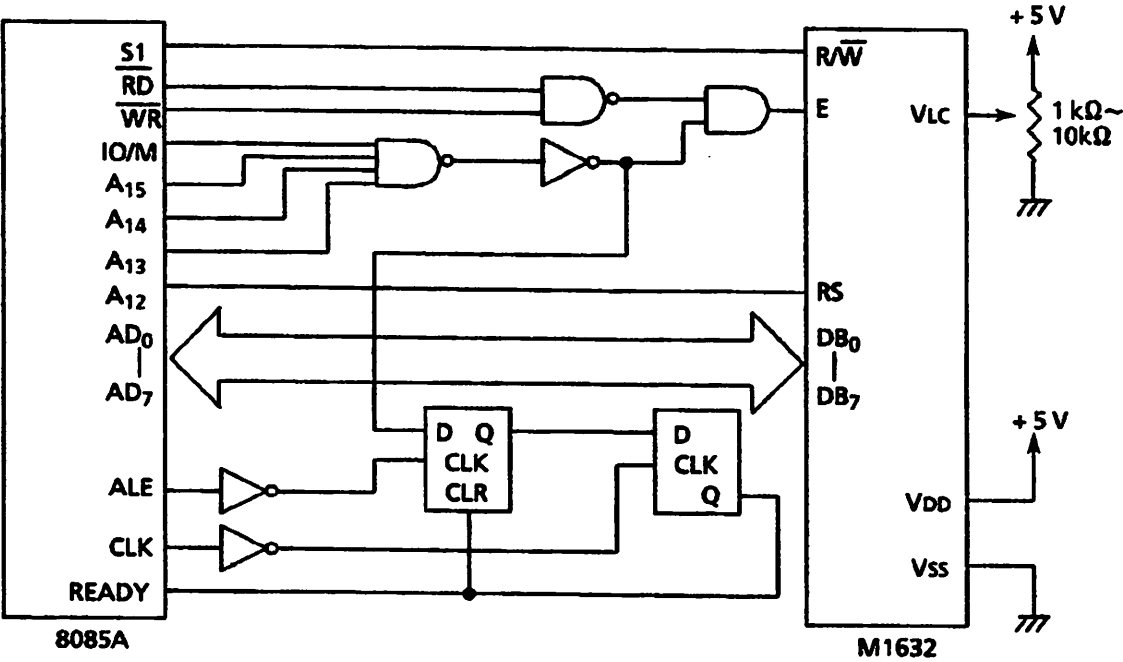
A08X L.8.



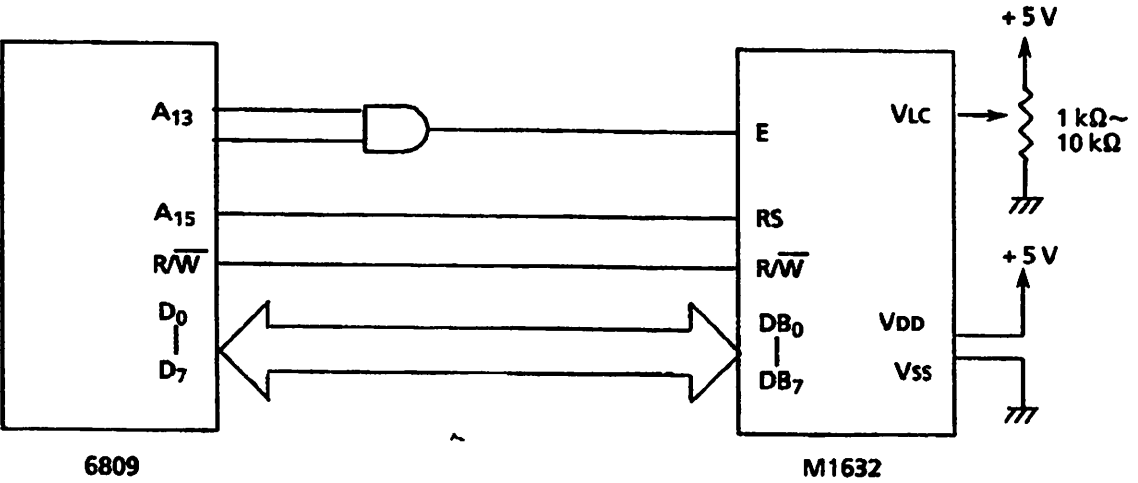
A2258 при A08X L.8.



2.6.3 8085A



2.6.4 6809



NOTES

Safety

- If the LCD panel breaks, be careful not to get the liquid crystal in your mouth. If the liquid crystal touches your skin or clothes, wash it off immediately using soap and plenty of water.

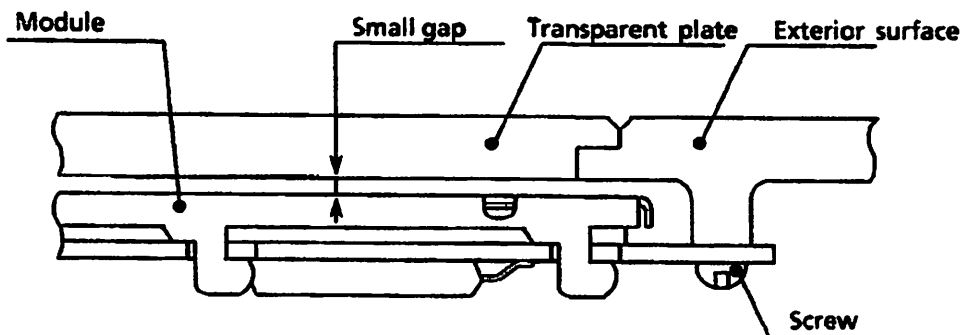
Handling

- Avoid static electricity as this can damage the CMOS LSI.
- The LCD panel is plate glass; do not hit or crush it.
- Do not remove the panel or frame from the module.
- The polarizer of the display is very fragile; handle it very carefully.

Mounting and esign

- Mount the module by using the specified mounting part and holes.
- Connect a 10- μ F capacitor between the power supply terminals to eliminate noise.
- To protect the module from external pressure, place a transparent plates (e.g. acrylic or glass), leaving a small gap, over the display surface, frame, and polarizer.

☆ Example



- Design the system so that no input signal is given unless the power-supply voltage is applied.
- Keep the module dry. Avoid condensation, otherwise the transparent electrodes may break.

NOTES

Safety

- If the LCD panel breaks, be careful not to get the liquid crystal in your mouth. If the liquid crystal reaches your skin or clothes, wash it off immediately using soap and plenty of water.

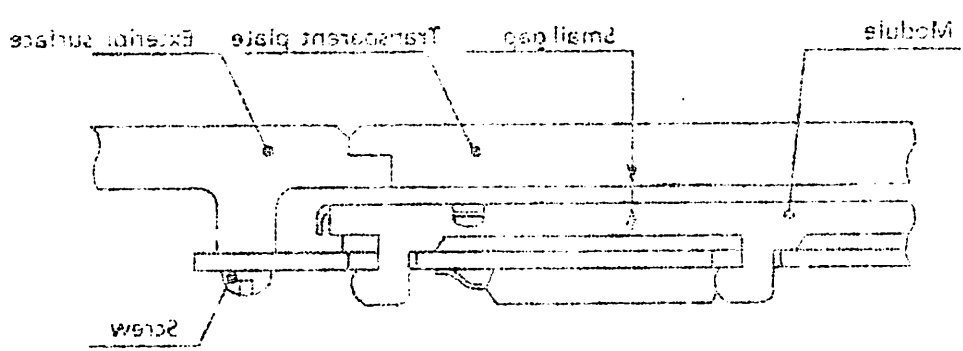
Handling

- Avoid static electricity as this can damage the CMOS LSI.
- The LCD panel is plate glass; do not hit or crush it.
- Do not remove the panel or frame from the module.
- The polarizer of the display is very fragile; handle it very carefully.

Mounting and wiring

- Mount the module by using the specified mounting part and holes.
- Connect a 10- μ F capacitor between the power supply terminals to eliminate noise.
- To protect the module from external pressure, place a transparent plate (e.g. acrylic or glass), leaving a small gap, over the display surface, frame, and polarizer.

Example



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Storage

- Store the module in a dark place where the temperature is $25^{\circ}\text{C} \pm 10^{\circ}\text{C}$ and the humidity below 65% RH.
- Do not store the module near organic solvents or corrosive gases.
- Do not crush, shake, or jolt the module (including accessories).

Cleaning

- Do not wipe the polarizer with a dry cloth, as it may scratch the surface.
- Wipe the module gently with a soft cloth soaked with a petroleum benzine.
- Do not use ketonic solvents (ketone and acetone) or aromatic solvents (toluene and xylene), as they may damage the polarizing plate.

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